TELEDYNE COMPONENTS

1992 DATA BOOK

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COMPONENTS

ANALOG SIGNAL
PROCESSING

DMOS

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POWER ICs

SENSORS

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Section 1

Display A/D Converters

2-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **Drives 2-1/2 Digit LED Displays**
- **Internal Voltage Reference .... 150 ppm/°C Max**
- **Low Supply Current .... 2 mA Max**
- **Ratiometric Measurements**
- **Auto-Zero Cycle Eliminates External Trimmers**
- **Dynamic Range .... ±200 Counts**
- **Multiple Package Options**
  - **— Low-Cost 40-Pin Package**
  - **— 44-Pin Plastic Flat Package**
  - **— 44-Pin PLCC Package**

GENERAL DESCRIPTION

The TC807 is a 2-1/2 digit analog-to-digital converter (ADC) designed to drive standard 7-segment LED displays without external drive electronics.

This 0.5% resolution converter is ideal for low-cost pressure, temperature, pH or flow-rate indicators.

The TC807 features differential inputs and references for ratiometric readings. An auto-zero cycle eliminates external offset adjustment potentiometers.

This dual-slope converter automatically rejects 50-, 60- and 400-Hz line frequency interference signals. Polarity information is displayed, giving the device a ±200 count dynamic range.

Overall system cost is reduced by incorporating a low-temperature coefficient voltage reference on-chip.

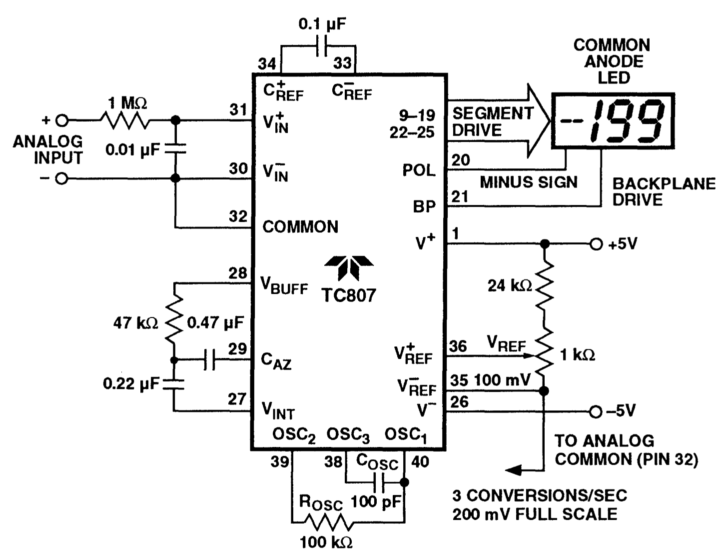
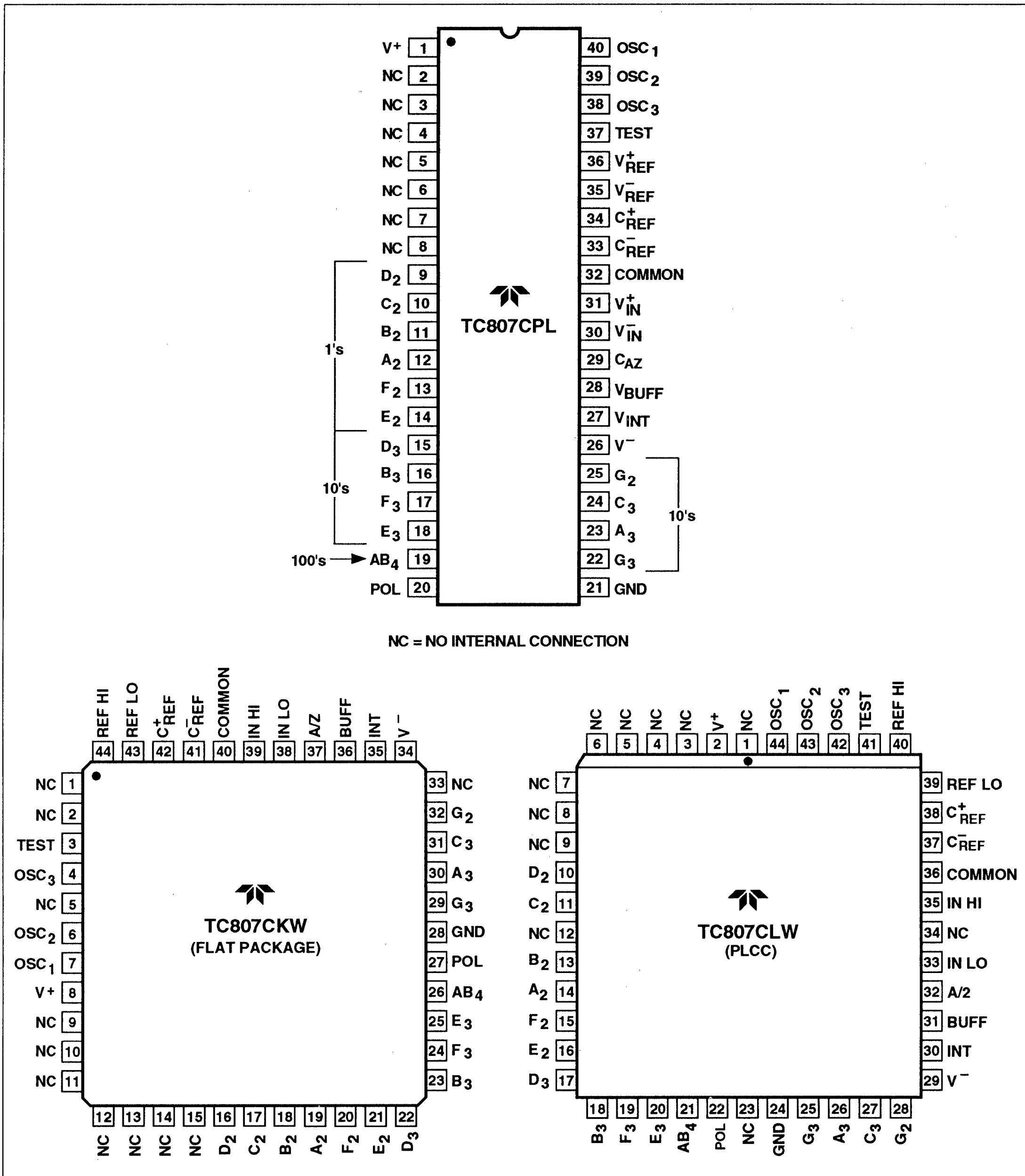


Figure 1. Typical Operating Circuit

PIN CONFIGURATIONS



2-1/2 DIGIT
ANALOG-TO-DIGITAL CONVERTER

TC807

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC807CPL	40-Pin Plastic DIP	0°C to +70°C
TC807CKW	44-Pin Plastic Flat	0°C to +70°C
TC807CLW	44-Pin PLCC	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V^+ .... +6V
- V^- .... –9V

Analog Input Voltage (Either Input) (Note 1) .... V^+ to V^-
Reference Input Voltage (Either Input) .... V^+ to V^-
Clock Input .... GND to V^+
Power Dissipation (Note 2) .... 800 mW
Operating Temperature Range .... 0°C to +70°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 60 Sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, f_{CLK} = 48 kHz, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV	–0	±0	+0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF} V_{REF} = 100 mV	99	99/100	100	Digital Reading
Roll-Over Error (Difference in Reading for Equal Positive and Negative Reading Near Full Scale)	$-V_{IN} = +V_{IN} \approx$ 200 mV	–1	±0.2	+1	Counts
Linearity (Max Deviation from Best Straight Line Fit)	Full Scale = 200 mV or Full Scale = 2V	–1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 3)	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200 mV	—	50	—	µV/V
Noise (Peak-Peak Value Not Exceeded 95% of Time)	V_{IN} = 0V, Full Scale = 200 mV	—	15	—	µV
Leakage Current at Input	V_{IN} = 0V	—	1	25	pA
Zero Reading Drift	V_{IN} = 0V	—	0.2	5	µV/°C
Supply Current (Does Not Include LED Current)	V_{IN} = 0V	—	0.8	2	mA
Internal Voltage Reference (Analog Common Potential with Respect to Positive Supply)	25 kW Between Common and Positive Supply	2.7	3.05	3.35	V
Temperature Coefficient of Analog Common (With Respect to Positive Supply)	25 kW Between Common and Positive Supply 0°C ≤ T_A ≤ 70°C	—	20	150	ppm/°C
Segment Sinking Current (Except Pin 19)	V^+ = 5V, Segment Voltage = 3V	4	8	—	mA
Segment Sinking Current, Pin 19	V^+ = 5V, Segment Voltage = 3V	8	16	—	mA

NOTES: 1. Input voltages may exceed supply voltages, provided input current is limited to ±100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to PC board.
3. Refer to "Differential Input" discussion.

PIN DESCRIPTION

40-Pin DIP Pin Number	Name	Description
1	V^+	Positive supply voltage.
2	NC	No connection.
3	NC	No connection.
4	NC	No connection.
5	NC	No connection.
6	NC	No connection.
7	NC	No connection.
8	NC	No connection.
9	D_1	Activates the D section of the units display.
10	C_1	Activates the C section of the units display.
11	B_1	Activates the B section of the units display.
12	A_1	Activates the A section of the units display.
13	F_1	Activates the F section of the units display.
14	E_1	Activates the E section of the units display.
15	D_2	Activates the D section of the tens display.
16	B_2	Activates the B section of the tens display.
17	F_2	Activates the F section of the tens display.
18	E_2	Activates the E section of the tens display.
19	AB_3	Activates both halves of the "1" in the hundreds display.
20	POL	Activates the negative polarity display.
21	GND	Digital ground.
22	G_2	Activates the G section of the tens display.
23	A_2	Activates the A section of the tens display.
24	C_2	Activates the C section of the tens display.
25	G_1	Activates the G section of the ones display.
26	V^-	Negative power supply voltage.
27	V_{INT}	Integrator output. Connection point for integration capacitor. See "Integrating Capacitor" for additional details.
28	V_{BUFF}	Integration resistor connection. Use a 47 kΩ resistor for 200 mV full-scale range and a 470 kΩ resistor for 2V full-scale range.
29	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 µF capacitor for 200 mV full scale, and a 0.47 µF capacitor for 2V full scale. See "Auto-Zero Capacitor" for more details.
30	V_{IN}^-	The analog low input is connected to this pin.
31	V_{IN}^+	The analog high input is connected to this pin.
32	COMMON	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See "Analog Common" for more details. It also acts as a reference voltage source.
33	C_{REF}^-	See pin 34.
34	C_{REF}^+	A 0.1 µF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1 µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	V_{REF}^-	See pin 36.
36	V_{REF}^+	The analog input required to generate a full-scale output (199 counts). Place 100 mV between pins 35 and 36 for 200 mV full scale. Place 1V between pins 35 and 36 for 2V full scale. See "Reference Voltage."

PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number	Name	Description
37	TEST	Lamp test. When pulled high (to V+), all segments will be turned on and the display should read "–188". It may also be used as a negative supply for externally-generated decimal points. See "Test" for additional information.
38	OSC_3	See pin 40.
39	OSC_2	See pin 40.
40	OSC_1	Pins 40, 39, and 38 make up the oscillator section. For a 48 kHz clock (three readings per second), connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor.The 100 kΩ resistor is held to pin 39 and the 100 pF capacitor is tied to pin 38.

ANALOG SECTION

Figure 2 is a block diagram of the TC807. Each measurement cycle is divided into three phases: (1) auto-zero (A-Z), (2) signal integration (SI), and (3) reference integration (RI). The conversion rate is set by the clock oscillator frequency and is independent of the analog input amplitude.

Auto-Zero Cycle

During the auto-zero cycle, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero-input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The offset error referred to the input is less than 10 μV.

The auto-zero cycle length is 4000 to 12,000 clock cycles.

Signal-Integrate Cycle

The auto-zero loop is opened, the internal short removed, and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The signal integration period is 4000 cycles. The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 1000,$$

where f_{OSC} = external clock frequency.

The differential input voltage must be within the device's common-mode range (1V of either supply) when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of the signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference-Integrate Cycle

The final phase is reference integrate or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously charged reference capacitor. Circuitry within the chip ensures the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal, and is between 0 and 8000 clock cycles. The digital reading displayed is:

$$100 \times \frac{V_{IN}}{V_{REF}} .$$

DIGITAL SECTION

The TC807 contains all the segment drivers necessary to directly drive a 2-1/2 digit LED display. The segment is typically 8 mA. The 100's output (pin 19) sinks current from two LED segments, and has a 16-mA drive capability. The TC807 is designed to drive common anode LED displays. (See Figure 2.)

The polarity indication is "ON" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

The display font is shown in Figure 3.

System Timing

The oscillator frequency is ÷4 prior to clocking the internal decade counters. The three-phase measurement cycle takes a total of 16,000 clock pulses.

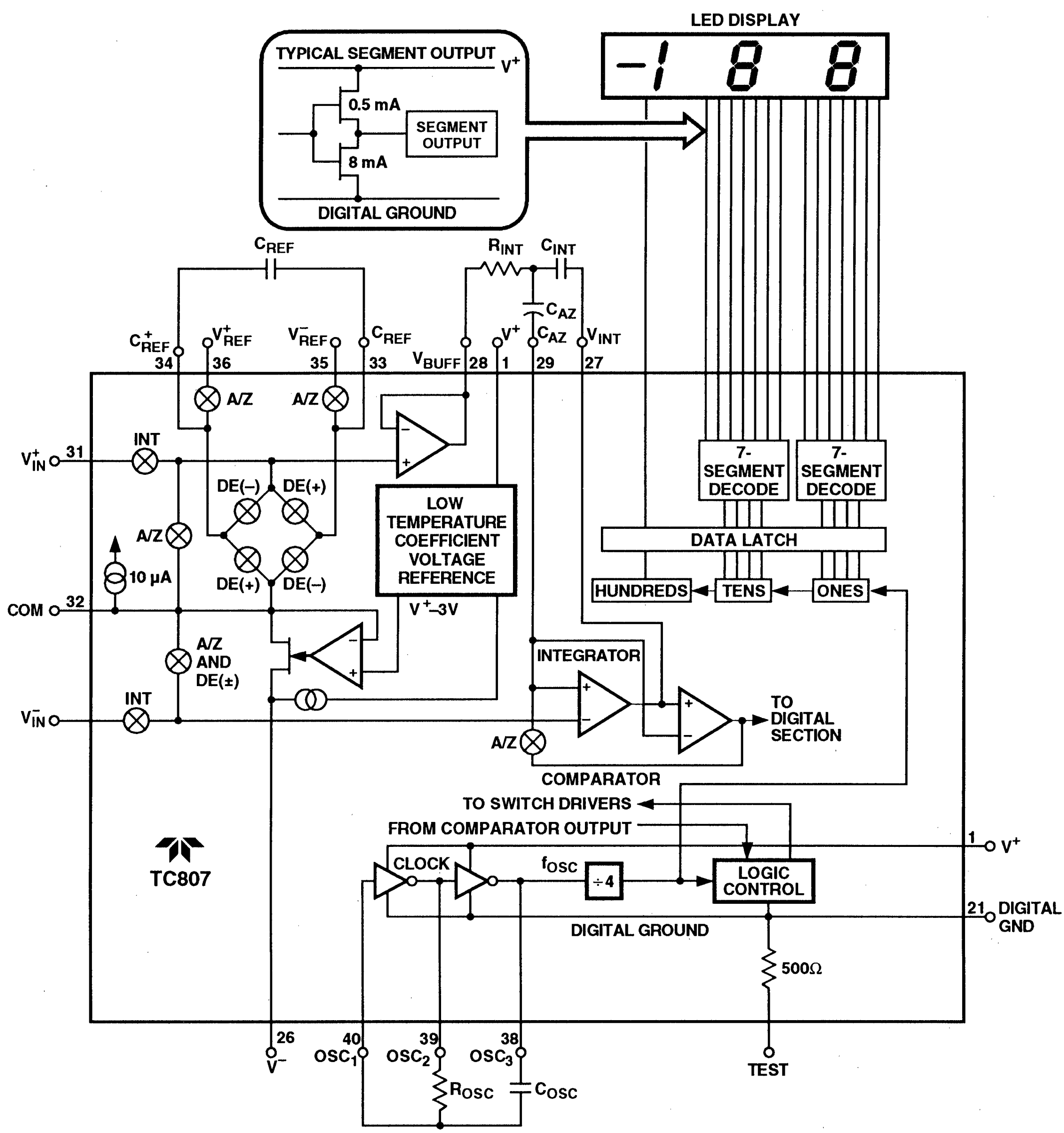


Figure 2. Block Diagram

Each phase of the measurement cycle has the following length:

(1) Auto-Zero Phase: 4000 to 12,000 clock pulses — For signals less than full-scale, the auto-zero phase is assigned the unused reference integrate time period.

(2) Signal Integrate: 4000 clock pulses — This time period is fixed. The integration period is:

$$t_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right],$$

where f_{OSC} is the externally set clock frequency.

(3) Reference Integrate: 0 to 8000 clock pulses.

Component Value Selection

Auto-Zero Capacitor (C_{AZ})

The C_{AZ} size has some influence on system noise. A 0.47 µF capacitor is recommended for 200 mV full scale. A 0.047 µF capacitor is adequate for 2V full-scale applications. A Mylar-type dielectric capacitor is adequate.

Reference Voltage Capacitor (C_{REF})

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 µF capacitor is acceptable when V_{IN}^- is tied to analog common. If a large common-mode voltage exists ($V_{REF}^- \neq$ analog common) and the application requires a 200-mV full scale, increase C_{REF} to 1 µF. Roll-over error will be held to less than 0.5 count. A Mylar-type dielectric capacitor is adequate.

Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case, a ±2V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz), a 0.22 µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}},$$

where: f_{OSC} = Clock frequency at pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing.

C_{INT} must have low dielectric absorption to minimize roll-over error. An inexpensive polypropylene capacitor is recommended.

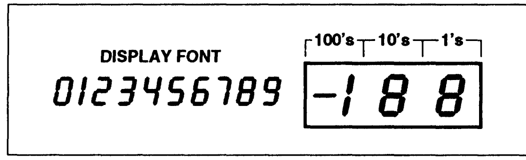


Figure 3. Display Font and Segment Assignment

Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 100 µA. The integrator and buffer can supply 20 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full scale, R_{INT} is 47 kΩ. A 2V full scale requires 470 kΩ.

Component Value	Nominal Full-Scale Voltage	
	200 mV	2V
C_{AZ}	0.47 µF	0.047 µF
R_{INT}	47 kΩ	470 kΩ
C_{INT}	0.22 µF	0.22 µF

NOTE: f_{OSC} = 48 kHz (3 readings/second)

Oscillator Components

R_{OSC} (pin 40 to pin 38) should be 100 kΩ. C_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}.$$

For f_{OSC} of 48 kHz, C_{OSC} is 100 pF, nominally.

Note that f_{OSC} is ÷4 to generate the TC807 internal control clock.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33-1/3 kHz, etc., should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc., would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (280 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200 mV	100 mV
2V	1V

*$V_{FS} = 2\ V_{REF}$

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. For example, assume a pressure transducer output for 200 lb/in.^{2} is 400 mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

The internal voltage reference potential available at analog common is normally used to supply the converter's reference. This potential is stable whenever the supply potential is greater than approximately 7V. In applications where an externally-generated reference voltage is desired, refer to Figure 4.

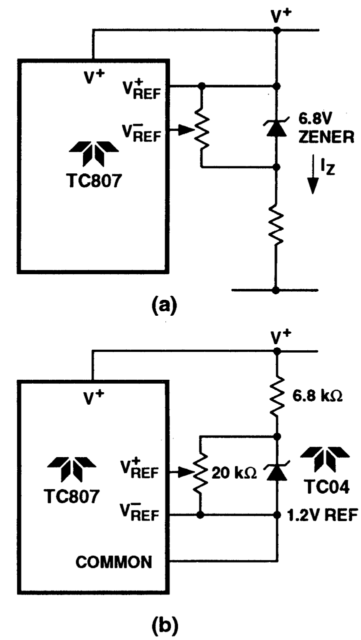


Figure 4. External Reference

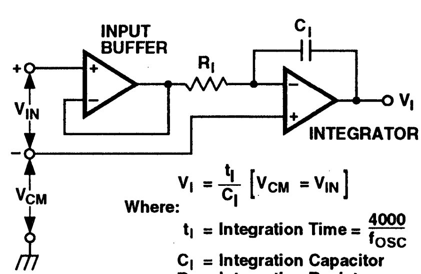
DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs

V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30)

The TC807 is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is V^+ –1V to V^- +1V. Common-mode voltages are removed from the system when the TC807 operates from a floating power source (isolated from measured system) and V_{IN}^- is connected to analog common.

In systems where common-mode voltages exist, the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 5). For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increasing linearity errors.



$$V_I = \frac{t_I}{C_I}\left[V_{CM} = V_{IN}\right]$$

Where:
t_I = Integration Time = $\frac{4000}{f_{OSC}}$
C_I = Integration Capacitor
R_I = Integration Resistor

Figure 5. Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)

Differential Reference

V_{REF}^+ (Pin 36), V_{REF}^- (Pin 39)

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent roll-over errors being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance.

Analog Common

Analog COMMON (pin 32) is set at a voltage potential approximately 3V below V^+. The potential is guaranteed to be between 2.7V and 3.35V below V^+. Analog common is tied internally to an N-channel FET capable of sinking 30 mA. This FET will hold the common line at 3V should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 10 μA. Therefore, analog common is easily pulled to a more negative voltage (i.e., below V^+-3V).

The TC807 connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero cycle. During the reference-integrate phase, V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converter's 86-dB common-mode rejection ratio. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to $V_{IN}-$.

Analog common serves to set the analog section reference or common point. The common potential has a 0.001%/% voltage coefficient and 15Ω output impedance.

With sufficiently high total supply voltage ($V^+-V^->7V$), analog common is a very stable potential with excellent temperature stability (typically 20 ppm/°C). This potential can be used to generate reference voltage.

If analog common is connected to power ground, the internal reference is disabled. An external reference is required when analog common is connected to power ground.

Test

TEST (pin 37) potential is 5V less than V^+. If test is pulled high (to V^+), all segments plus the minus sign will be activated.

The test pin will sink about 10 mA when pulled to V^+.

POWER SUPPLIES

The TC807 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors, and an inexpensive IC. (See Figure 6.)

In selected applications, a negative supply is not required. The conditions to use a single +5V supply are:

(1) The input signal can be referenced to the center of the common-mode range of the converter.

(2) The signal is less than ±1.5V.

(3) An external reference is used.

(4) The TC7660 DC-to-DC converter may also be used to generate –5V from +5V (Figure 7).

Ratiometric Resistance Measurements

True differential input and differential reference make ratiometric readings possible. Typically, in a ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 100. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 100.$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

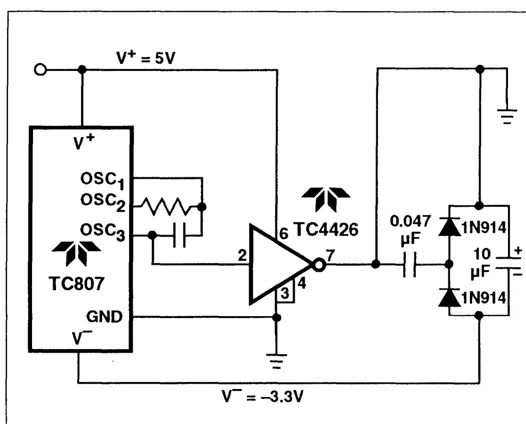


Figure 6. Generating Negative Supply From +5V

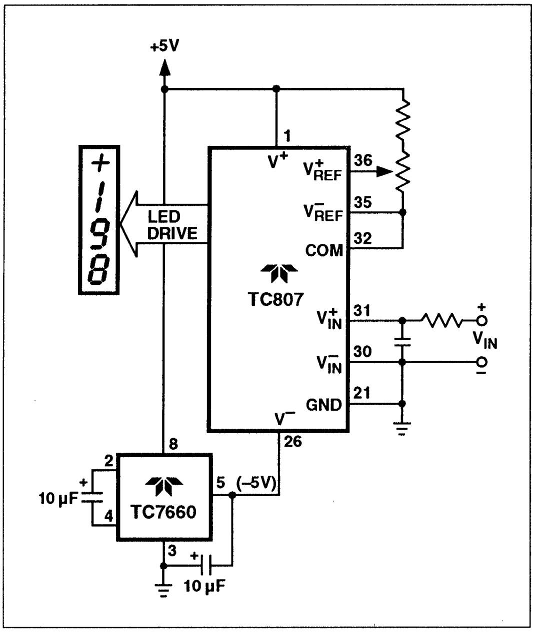


Figure 7. Negative Power Supply Generation With TC7660

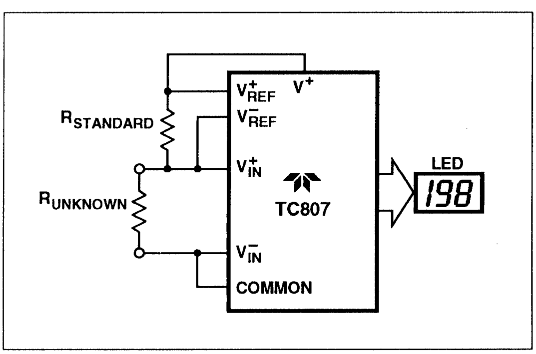


Figure 8. Low Parts Count Ratiometric Resistance Measurement

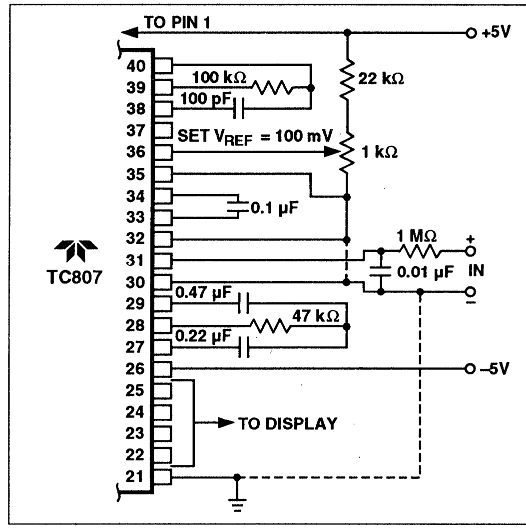


Figure 9. Internal Reference (200 mV Full Scale, 3 RPS, V_{IN}^- Tied to Ground for Single-Ended Inputs)

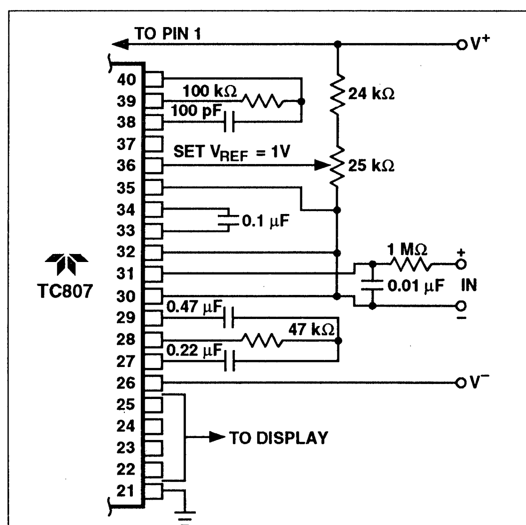


Figure 10. Recommended Component Values for 2V Full Scale

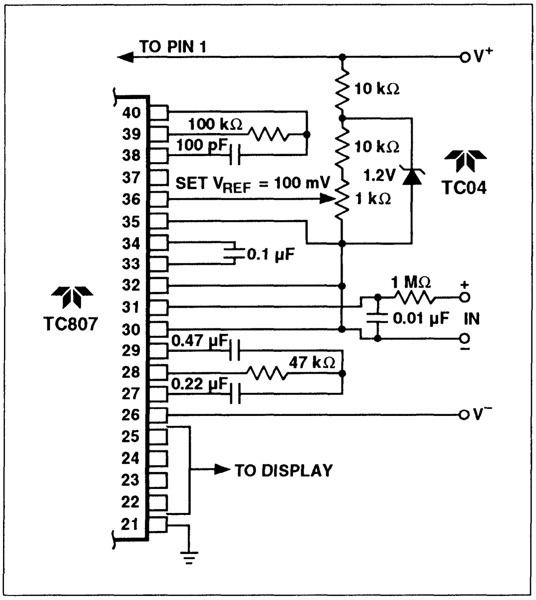


Figure 11. TC807 With a 1.25V External Band-Gap Reference (V_{IN}^- Tied to Common)

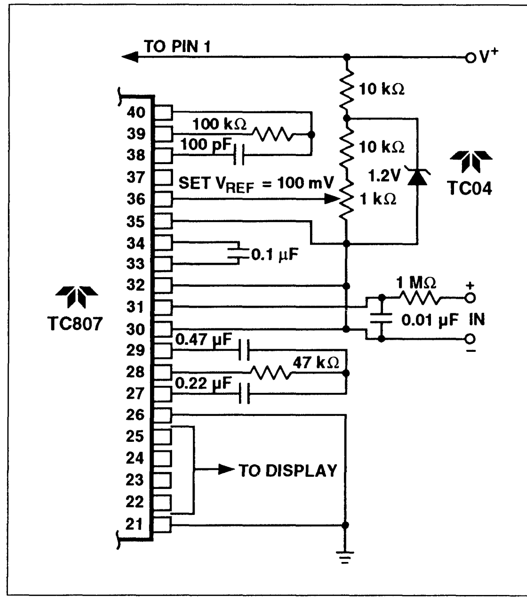


Figure 12. TC807 Operated From Single +5V Supply (An External Reference Must Be Used in This Application)

NOTES

3-1/2 DIGIT A/D CONVERTER WITH HOLD AND DIFFERENTIAL REFERENCE INPUTS

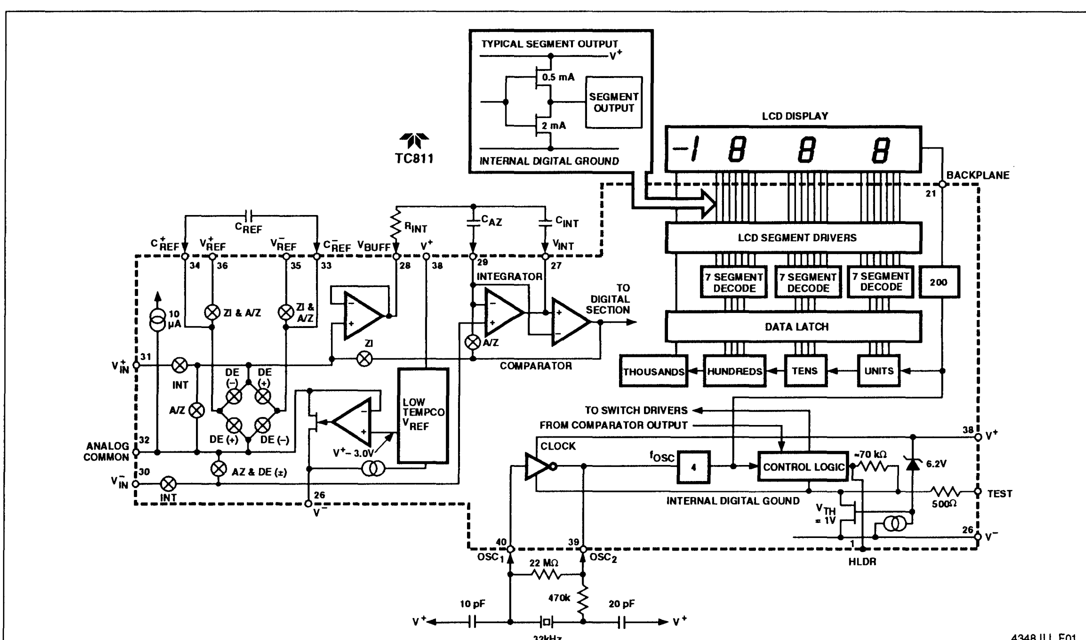
FEATURES

- Differential Reference Input
- Display Hold Function
- Fast Over-Range Recovery, Guaranteed Next Reading Accuracy
- Low Temperature Drift Internal Reference 35 ppm/°C (Typ)
- Guaranteed Zero Reading With Zero Input
- Low Noise .... 15 μV_{p-p}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- High Impedance Differential Input
- Low Input Leakage Current....................... 1 pA Typ
  10 pA Max
- Direct LCD Drive—No External Components
- Precision Null Detection with True Polarity at Zero
- Crystal Clock Oscillator
- Available in DIP, Compact Flat Package or PLCC
- Convenient 9V Battery Operation with Low Power Dissipation (600μA Typical, 1mW Maximum)

TYPICAL APPLICATIONS

- Thermometry
- Digital Meters
  - — Voltage/Current/Power
  - — pH Measurement
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity
  - — Humidity
  - — Position
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Digital Scales
- Process Monitors
- Gaussometers
- Photometers

FUNCTIONAL DIAGRAM



3-1/2 DIGIT A/D CONVERTER WITH HOLD AND DIFFERENTIAL REFERENCE INPUTS

TC811

GENERAL DESCRIPTION

The TC811 is a low power, 3-1/2 digit, LCD display analog-to-digital converter. This device incorporates both a display hold feature and differential reference inputs. A crystal oscillator, which only requires two pins, permits added features while retaining a 40-pin package. An additional feature is an "Integrator Output Zero" phase which guarantees rapid input overrange recovery.

The TC811 display hold (HLDR) function can be used to "freeze" the LCD display. The displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The TC811 also includes a differential reference for easy ratiometric measurements. Circuits which use the 7106/26/36 can easily be upgraded to include the hold function with the TC811.

The TC811 has an improved internal zener reference voltage circuit which maintains the Analog Common temperature drift to 35ppm/°C (typical) and 75ppm/°C (maximum). This represents an improvement of two to four times over similar 3-1/2 digit converters, eliminating the need for a costly, space consuming external reference source.

The TC811 limits linearity error to less than one count on both the 200mV and the 2.00V full-scale ranges. Rollover error—the difference in readings for equal magnitude but opposite polarity input signals—is below ±1 count. High impedance differential inputs offer 1pA leakage currents and a $10^{12}\Omega$ input impedance. The $15\mu V_{p-p}$ noise performance guarantees a "rock solid" reading. The Auto Zero cycle guarantees a zero display readout for a zero volt input.

The single chip CMOS TC811 incorporates all the active devices for a 3-1/2 digit analog to digital converter to directly drive an LCD display. Onboard oscillator, precision voltage reference and display segment and backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution (0.05%) indicating meter requires only a TC811, an LCD display, five resistors, six capacitors, a crystal, and a 9V battery. Compact, hand held multimeter designs benefit from the Teledyne Semiconductor small footprint package option.

The TC811 uses a dual slope conversion technique which will reject interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400Hz line frequency signals are present.

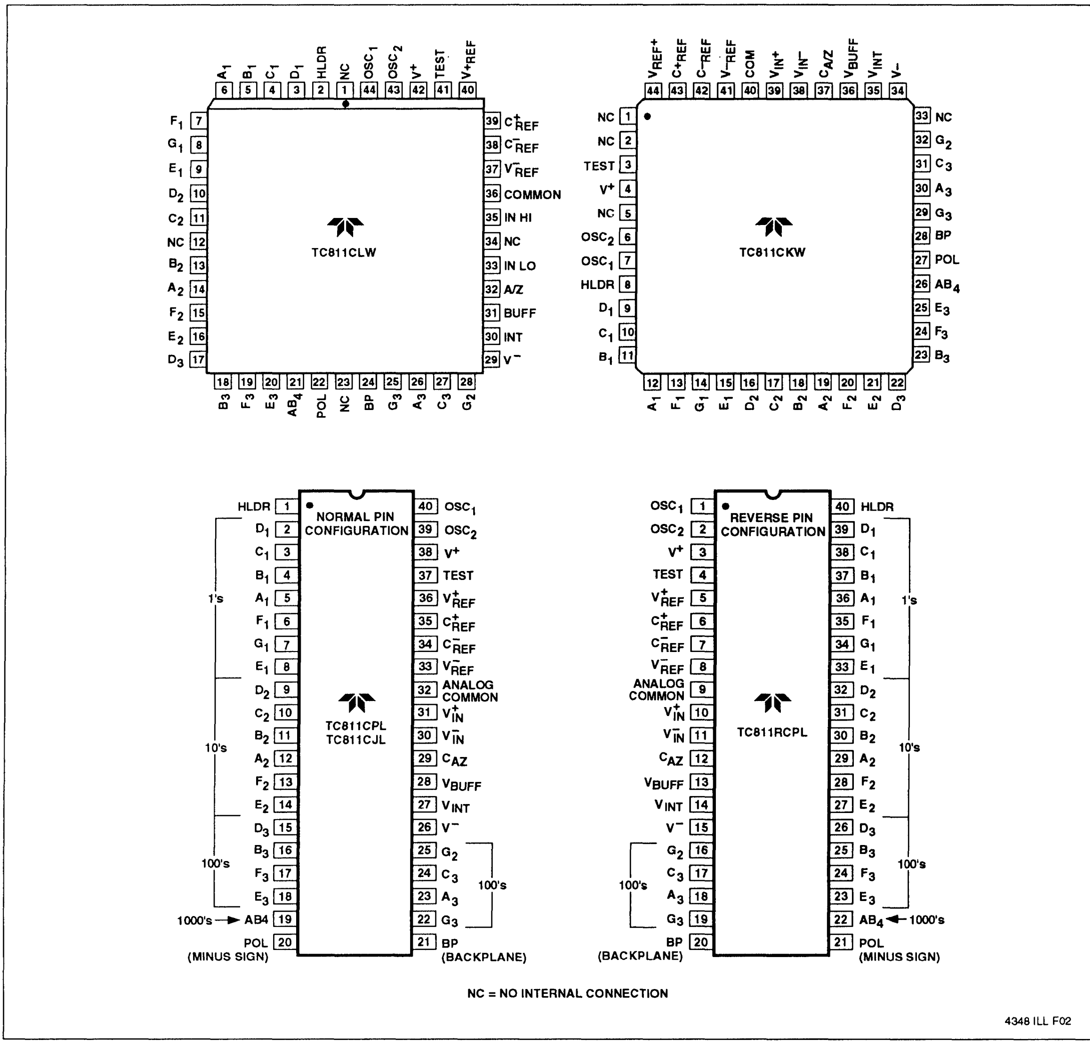
ORDERING INFORMATION

Part No.	Package	Temperature Range	V_{REF} TempCo
TC811CPL	40-Pin Plastic	0° to 70°C	75 ppm/°C Max
TC811RCPL[1]	40-Pin Plastic	0° to 70°C	75 ppm/°C Max
TC811IJL	40-Pin CerDIP	–25° to 85°C	100 ppm/°C Max
TC811CKW	44-Pin Flat	0° to +70°C	75 ppm/°C Max
TC811CLW	44-Pin PLCC	0° to +70°C	75 ppm/°C Max

NOTES: 1. Reversed pin-out

3-1/2 DIGIT A/D CONVERTER WITH HOLD AND DIFFERENTIAL REFERENCE INPUTS

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V–) 15V
Analog Input voltage (Either Input)[1] .... V+ to V–
Reference Input Voltage .... V+ to V–
Clock Input .... TEST to V+
Power Dissipation[2]
  CerDIP Package (J) .... 1000 mW
  Plastic Package (P, K) .... 800 mW
  Plastic Leaded Chip Carrier (L) .... 800 mW
Operating Temperature Range
  Commercial Package (C) .... 0°C to +70°C
  Industrial Package (I) .... –25°C to +85°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (soldering, 60 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{Supply} = 9V, f_{CLOCK} = 32.768kHz, and T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
—	Zero Input Reading	V_{IN} = 0V V_{FS} = 200mV	–000.0	±000.0	+000.0	Digital Reading
—	Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ 70°C	—	0.2	1	µV/°C
—	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
NL	Linearity Error	V_{FS} = 200mV or 2.000V	–1	±0.2	+1	Counts
E_R	Roll Over Error	V_{IN}– = V_{IN}+ ≈ 200mV	–1	±0.2	+1	Counts
e_N	Noise	V_{IN} = 0V, V_{FS} = 200mV	—	15	—	μV_{P-P}
I_L	Input Leakage Current	V_{IN} = 0V	—	1	10	pA
CMRR	Common-Mode Rejection	V_{CM} = ±1V, V_{IN} = 0V, V_{FS} = 200mV	—	50	—	µV/V
TC_{SF}	Scale Factor Temperature Coefficient	V_{IN} = 199mV, 0°C ≤ T_A ≤ 70°C (ext. V_{REF} tc = 0ppm)	—	1	5	ppm/°C
Analog Common Section						
V_{CTC}	Analog Common Temperature Coefficient	250KΩ from V+ to Analog Common 0°C ≤ T_A ≤ 70°C "C" Commercial "I" Industrial	— —	35 35	75 100	ppm/°C ppm/°C
V_C	Analog Common Voltage	250KΩ from V+ to Analog Common	2.7	3.05	3.35	Volts
Hold Pin Input Section						
	Input Resistance	Pin 1 to Pin 37	—	70	—	kΩ
V_{IL}	Input Low Voltage	Pin 1	—	—	Test +1.5	V
V_{IH}	Input High Voltage	Pin 1	V+ –1.5	—	—	V
LCD Drive Section[3]						
V_{SD}	LCD Segment Drive Voltage	V+ to V– = 9V	4	5	6	V_{P-P}
V_{SD}	LCD Backplane Drive Voltage	V+ to V– = 9V	4	5	6	V_{P-P}
Power Supply						
I_{SUP}	Power Supply Current	V_{IN} = 0V, V+ to V– = 9V				
		f_{OSC} = 16kHz	—	70	100	µA
		f_{OSC} = 48kHz	—	90	125	µA

NOTES: 1. Input voltages may exceed supply voltages when input current is limited to100µA.
2. Dissipation rating assumes device is mounted with all leads soldered to a printed circuit board.
3. Backplane drive is in phase with the segment drive for "segment off" 180° out of phase for "segment on." Frequency is 20 times the conversion rate. Average DC component is less than 50mV.

PIN DESCRIPTION

40-Pin DIP	44-Pin PLCC	Name	Function
1	2	HLDR	Hold pin, logic 1 holds present display reading
2	3	D_1	Activates the D section of the units display
3	4	C_1	Activates the C section of the units display
4	5	B_1	Activates the B section of the units display
5	6	A_1	Activates the A section of the units display
6	7	F_1	Activates the F section of the units display
7	8	G_1	Activates the G section of the units display
8	9	E_1	Activates the E section of the units display
9	10	D_2	Activates the D section of the tens display
10	11	C_2	Activates the C section of the tens display
11	13	B_2	Activates the B section of the tens display
12	14	A_2	Activates the A section of the tens display
13	15	F_2	Activates the F section of the tens display
14	16	E_2	Activates the E section of the tens display
15	17	D_3	Activates the D section of the hundreds display
16	18	B_3	Activates the B section of the hundreds display
17	19	F_3	Activates the F section of the hundreds display
18	20	E_3	Activates the E section of the hundreds display
19	21	AB_4	Activates both halves of the 1 in the thousands display
20	22	POL	Activates the negative polarity display
21	24	BP	Backplane drive output
22	25	G_3	Activates the G section of the hundreds display
23	26	A_3	Activates the A section of the hundreds display
24	27	C_3	Activtes the C section of the hundreds display
25	28	G_2	Activates the G section of the tens display
26	29	V–	Negative power supply voltage
27	30	V_{INT}	Integrator output, connection for C_{INT}
28	31	V_{BUFF}	Buffer output, connection for R_{INT}
29	32	C_{AZ}	Integrator input, connection for C_{AZ}
30	33	$V_{IN}-$	Analog input low
31	35	$V_{IN}+$	Analog input high
32	36	COM	Analog Common: Internal zero reference
33	37	$V_{REF}-$	Reference input low
34	38	$C_{REF}-$	Negative connection for reference capacitor
35	39	$C_{REF}+$	Positive connection for reference capacitor
36	40	$V_{REF}+$	Reference input high
37	41	TEST	All LCD segment test when pulled high (V^+)
38	42	V+	Positive power supply voltage
39	43	OSC_2	Crystal oscillator output
40	44	OSC_1	Crystal oscillator input

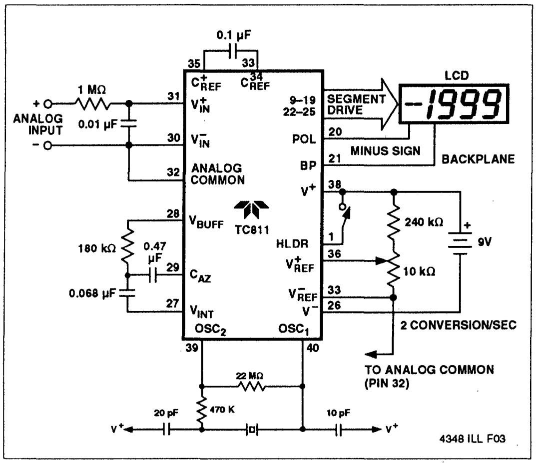


Figure 1 Typical Operating Circuit

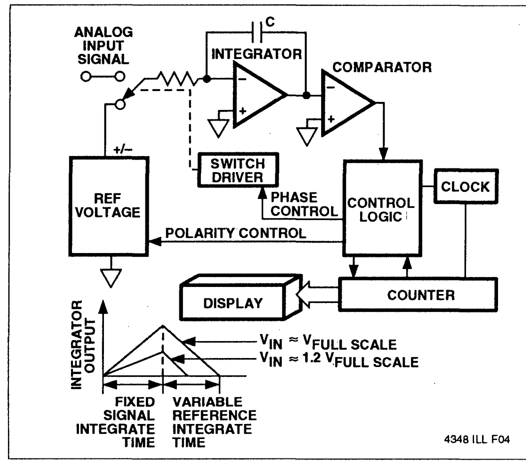


Figure 2 Basic Dual Slope Converter

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC811 is a dual slope, integrating analog-to-digital converter. An understanding of the dual slope conversion technique will aid the user in following the detailed TC811 theory of operation following this section. A conventional dual slope converter measurement cycle has two distinct phases:

1) Input Signal Integration
2) Reference Voltage Integration (Deintegration)

Referring to Fig 2, the unknown input signal to be converted is integrated from zero for a fixed time period (T_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (deintegration) time (T_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

In a simple dual slope converter, a complete conversion requires the integrator output to "ramp-up" from zero and "ramp-down" back to zero. A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}}\int_0^{t_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where:

V_{REF} = Reference voltage
t_{INT} = Integration Time
t_{DEINT} = Deintegration Time

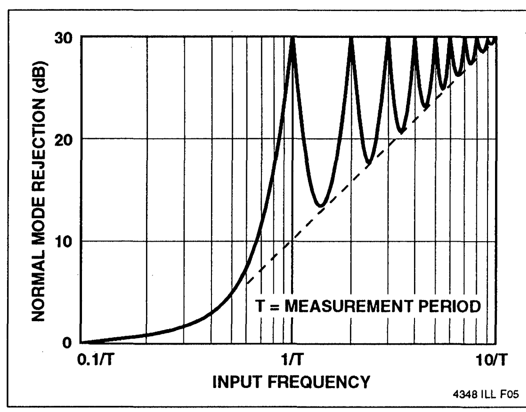


Figure 3 Normal-Mode Rejection of Dual Slope Converter

For a constant V_{INT}:

$$V_{IN} = V_{REF}\left[\frac{t_{DEINT}}{t_{INT}}\right]$$

Accuracy in a dual slope converter is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit of the dual slope technique is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integration ADCs immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated. (see Fig 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60Hz power line period.

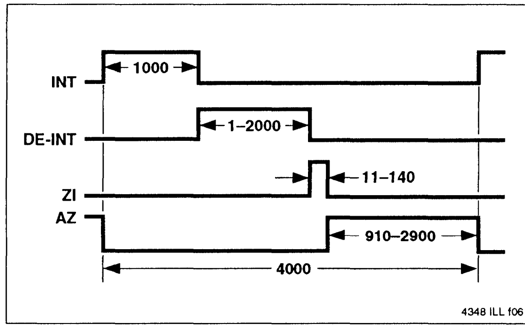


Figure 4a Conversion Timing During Normal Operation

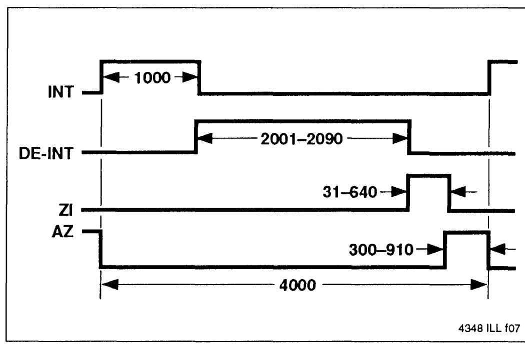


Figure 4b Conversion Timing During Overrange Operation

THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual-slope cycles discussed above, the TC811 design incorporates an "Integrator Output Zero" cycle and an "Auto Zero" cycle. These additional cycles ensure the integrator starts at 0V (even after a severe over-range conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Integrator Output Zero Cycle
(2) Auto Zero Cycle
(3) Signal Integrate Cycle
(4) Reference Deintegrate Cycle

Integrator Output Zero Cycle

This phase guarantees that the integrator output is at zero volts before the system zero phase is entered, ensuring that the true system offset voltages will be compensated for even after an over-range conversion. The duration of this phase is variable, being a function of the number of counts (clock cycles) required for deintegration.

The Integrator Output Zero cycle will last from 11 to 140 counts for non-over-range conversions and from 31 to 640 counts for over-range conversions.

Auto Zero Cycle

During the Auto Zero cycle, the differential input signal is disconnected from the measurement circuit by opening internal analog switches and the internal nodes are shorted to Analog Common (0V ref.) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The Auto Zero cycle residual is typically 10 to 15μV.

The Auto Zero duration is from 910 to 2,900 counts for non-over-range conversions and from 300 to 910 counts for over-range conversions.

Signal Integration Cycle

Upon completion of the Auto Zero cycle, the Auto Zero loop is opened and the internal differential inputs connect to $V_{IN}+$ and $V_{IN}-$. The differential input signal is then integrated for a fixed time period which, in the TC811 is 1000 counts (4000 clock periods). The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{INT} = \frac{4000}{f_{OSC}}$$

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground).

If the converter and measured system do not share the same power supply common, as in battery powered applications, $V_{IN}-$ should be tied to Analog Common.

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication in that signals less than 1 LSB are correctly determined. This allows precision null detection which is limited only by device noise and Auto Zero residual offsets.

Reference Integrate (Deintegrate) Cycle

The reference capacitor, which was charged during the Auto Zero cycle, is connected to the input of the integrating amplifier. The internal sign logic insures that the polarity of the reference voltage is always connected in the phase which is opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate which is determined by the reference potential.

The amount of time required (T_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration cycle:

$$T_{DEINT} = \frac{R_{INT}\, C_{INT}\, V_{INT}}{V_{REF}}$$

The digital reading displayed Is:

$$\text{Digital Count} = 1000\ \frac{V_{IN}+ - V_{IN}-}{V_{REF}}$$

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

1) Auto Zero: 300 to 2900 Counts
2) Signal Integrate: 1000 Counts

This time period is fixed. The integration period is:

$$T_{INT} = \frac{4000}{f_{OSC}} = 1000 \text{ Counts}$$

Where f_{OSC} is the crystal oscillator frequency.

3) Reference Integrate: 0 to 2000 Counts
4) Integrator Output Zero: 11 to 640 Counts

The TC811 can replace the ICL7106/26/36 in circuits which require both the hold function and a differential reference. The TC811 offers a greatly improved internal reference temperature coefficient, which can often eliminate the need for an external reference. Some minor component changes are required to upgrade existing designs, reduce power dissipation, and improve the overall performance. (see Oscillator Components)

Digital Section

The TC811 contains all the segment drivers necessary to directly drive a 3-1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal the segment of "OFF". An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If $V_{IN}+$ and $V_{IN}-$ are reversed then this indicator would reverse.

TEST Function (TEST)

On the TC811, when TEST is pulled to a logical "HIGH", all segments are turned "ON". The display will read "-1888". During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and segment drive assignment are shown in Figure 5.

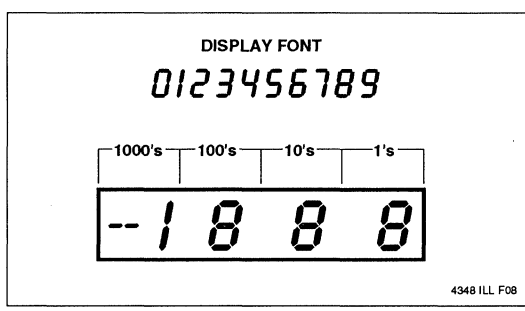


Figure 5 Display FONT and Segment Assignment

HOLD Reading Input (HLDR)

When HLDR is at a logic "HI" the latch will not be updated. Conversions will continue but will not be updated until HLDR is returned to "LOW". To continuously update the display, connect HLDR to ground or leave it open. This input is CMOS compatible and has an internal resistance of 70KΩ (typical) tied to TEST.

COMPONENT VALUE SELECTION

Auto Zero Capacitor - C_{AZ}

The value of the Auto Zero capacitor (C_{AZ}) has some influence on system noise. A 0.47µF capacitor is recommended for 200mV full-scale applications where 1LSB is 100µV. A 0.10µF capacitor should be used for 2.0V full-scale applications. A capacitor with low dielectric absorption (Mylar) is required.

Reference Voltage Capacitor -C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1µF capacitor is typical. If the application requires a sensitivity of 200mV full-scale, increase C_{REF} to 1.0µF. Rollover error will be held to less than 1/2 count. A good quality, low leakage capacitor, such as Mylar, should be used.

Integrating Capacitor - C_{INT}

CINT should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case a ±2V integrator output swing is optimum when the analog input is near full-scale. For 2 or 2.5 reading/second (f_{OSC} = 32kHz or 40kHz) and V_{FS} = 200mV, a .068µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing. An exact expression for C_{INT} is :

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT}\ R_{INT}\ f_{OSC}}$$

where:
f_{OSC} = Clock frequency at Pin 39
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor -R_{INT}

The input buffer amplifier and integrator are designed with class A output stages which have idling currents of 6µA. The integrator and buffer can supply 1µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200mV full-scale, R_{INT} should be about 180kΩ. A 2.0V full-scale requires abut 1.8MΩ.

Oscillator Components

The internal oscillator has been designed to operate with a quartz crystal, such as the Statek CX-1V series. Such crystals are very small and are available in a variety of standard frequencies. Note that f_{OSC} is divided by four to generate the TC811 internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of ac-line noise pickup, a 40kHz crystal should be used. This frequency will yield an integration period of 100ms and will reject both 50Hz and 60Hz noise. For prototyping or cost-sensitive applications a 32.768kHz watch crystal can be used, and will produce about 25dB of line-noise rejection. Other crystal frequencies, from 16kHz to 48kHz, can also be used.

Pins 39 and 40 make up the oscillator section of the TC811. Figures 6a and 6b show some typical conversion rate component values.

The LCD backplane frequency is derived by dividing the oscillator frequency by 800. Capacitive loading of the LCD may compromise display performance if the oscillator is run much over 48KHz.

Reference Voltage (V_{REF})

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

In some applications a scale factor other than unity may exist, such as between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400mV for 2000lb/in^2. Rather than dividing the input voltage by two, the reference voltage should be set to 200mV. This permits the transducer input to be used directly.

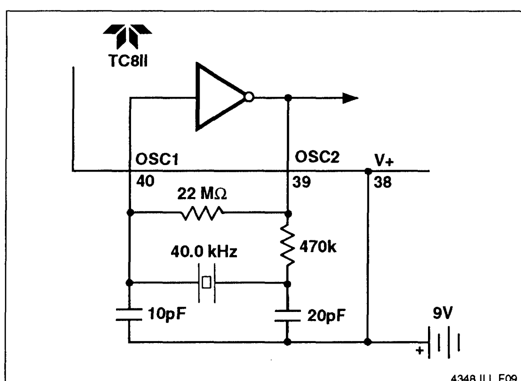


Figure 6a TC811 Oscillator

Oscillator Freq. (kHz)	Full-Scale Voltage (V_{FS})			
	200mV		2.0V	
	RINT	CINT	RINT	CINT
32.768	180k	0.068µF	1.8M	0.068µF
40	150k	0.068µF	1.5M	0.068µF

Figure 6b

DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs (V_{IN}+ (Pin 31), V_{IN}– (Pin 30))

The TC811 is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V+ – 1.0 to V– + 1.5V. Common-mode voltages are removed from the system when the TC811 operates from a battery or floating power source (isolated from measured system) and V_{IN}– is connected to Analog Common. (see Fig 8)

In systems where common-mode voltages exist, the 86dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 8). For such applications the integrator output swing can be reduced below the recommended 2.0V full-scale swing. The integrator output will swing within 0.3V of V+ or V– without increased linearity error.

Reference (V_{REF}+ (Pin 36), V_{REF}– (Pin 33))

Unlike the ICL7116, the TC811 has a differential reference as well as the "hold" function. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors such as load cells and temperature sensors. The TC811 is ideally suited to applications in handheld multimeters, panel meters, and portable instrumentation. The reference voltage can be generated anywhere within the V+ to V– power supply range.

To prevent rollover type errors from being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance. A 0.1µF capacitor is a typical value.

The TC811 offers a significantly improved Analog Common temperature coefficient. This provides a very stable voltage suitable for use as a voltage reference. The temperature coefficient of Analog Common is typically 35ppm/°C.

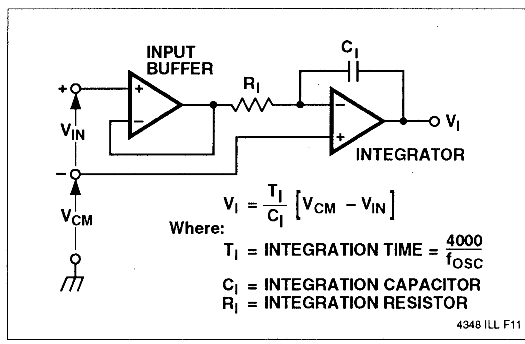


Figure 8 Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

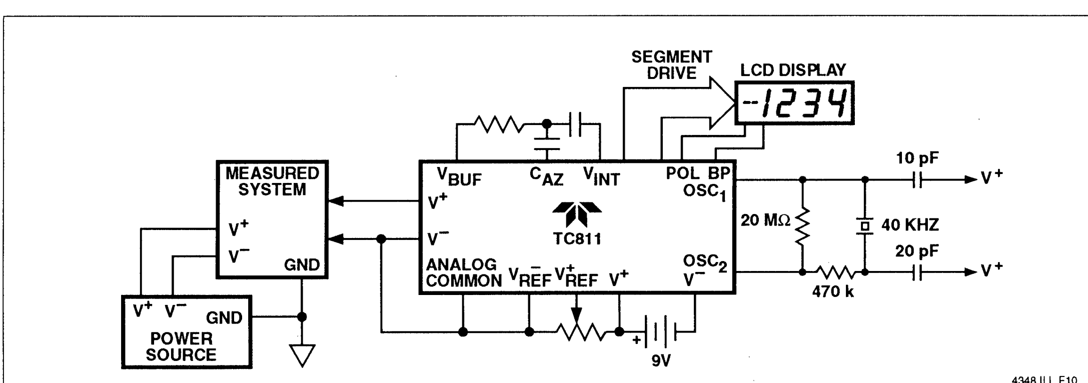


Figure 7 Common-Mode Voltage Removed in Battery Operation With V_{IN}– = Analog Common

Analog Common (Pin 32)

The Analog Common pin is set at a voltage potential approximately 3.0V below V+. This potential is guaranteed to be between 2.70V and 3.35V below V+. Analog common is tied internally to an N channel FET capable of sinking 100μA. This FET will hold the common line at 3.0V below V+ should an external load attempt to pull the common line toward V+. Analog common source current is limited to 1μA. Analog common is therefore easily pulled to a more negative voltage (i.e. below V+ – 3.0V).

The TC811 connects the internal $V_{IN}+$ and $V_{IN}-$ inputs to Analog Common during the Auto Zero cycle. During the reference integrate phase $V_{IN}-$ is connected to Analog Common. If $V_{IN}-$ is not externally connected to Analog Common, a common-mode voltage exists. This is rejected by the converter's 86dB common-mode rejection ratio. In battery powered applications, Analog Common and $V_{IN}-$ are usually connected, removing common-mode voltage concerns. In systems where $V_{IN}-$ is connected to the power supply ground or to a given voltage, Analog Common should be connected to $V_{IN}-$.

The Analog Common pin serves to set the analog section reference or common point. The TC811 is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC811 power source. The Analog Common potential of V+ – 3.0V gives a 7V end of battery life voltage. The analog common potential has a voltage coefficient of 0.001%/%.

With a sufficiently high total supply voltage (V+ – V– > 7.0V), Analog Common is a very stable potential with excellent temperature stability (typically 35ppm/°C). This potential can be used to generate the TC811 reference voltage. An external voltage reference will be unnecessary in most cases because of the 35ppm/°C temperature coefficient. See TC811 Internal Voltage Reference discussion.

TEST (Pin 37)

The TEST pin potential is 5V less the V+. TEST may be used as the negative power supply connection when interfacing the TC811 to external CMOS logic. The TEST pin is tied to the internally generated negative logic supply through a 500Ω resistor. The TEST pin may be used to sink up to 1mA. See the applications section for additional information on using TEST as a negative digital logic supply.

If TEST is pulled "HIGH" (V+), all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes, because when TEST is pulled to V+, the LCD Segments are impressed with a DC voltage which may cause damage to the LCD.

APPLICATIONS INFORMATION

Decimal Point and Annunciator Drive

The TEST pin is connected to the internally generated digital logic supply ground through a 500Ω resistor. The TEST pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1mA should be supplied by the TEST pin. The TEST pin potential is approximately 5V below V+.

Internal Voltage Reference

The TC811 Analog Common voltage temperature stability has been significantly improved. This improved device can be used to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed, however, noise performance will be improved by increasing C_{AZ} (See Auto Zero Capacitor section). Fig 10 shows Analog Common supplying the necessary voltage reference for the TC811.

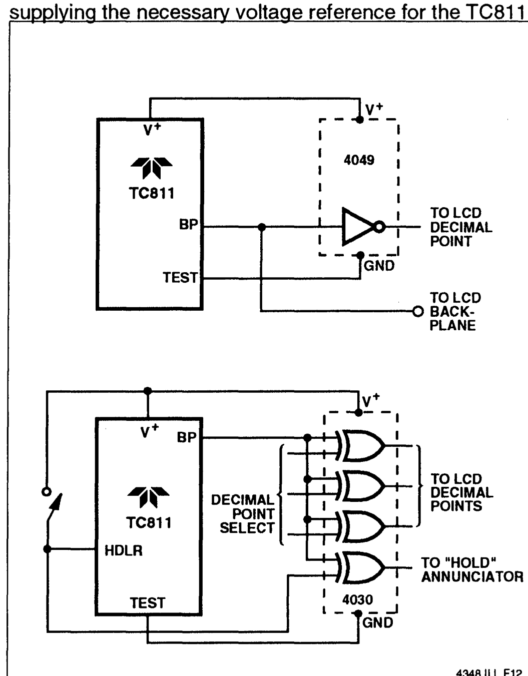


Figure 9 Display Annunciator Drivers

Liquid Crystal Display Sources

Several LCD manufactures supply standard LCD displays to interface with the TC811 3-1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415-347-9916	FE 0801, FE 0203
EPSON	3415 Kashikawa St., Torrence, CA 90505 212-534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414-648-2361	3902, 3933, 3903

*NOTE: Contact LCD manufacturer for full product listing/specifications.

Oscillator Crystal Source

Manufacturer	Address/Phone	Representative Part Numbers
STATEK	512 N-Main Orange, CA 92668 714-639-7810	CX-1V 40.0

Ratiometric Resistance Measurements

The TC811 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 11). The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

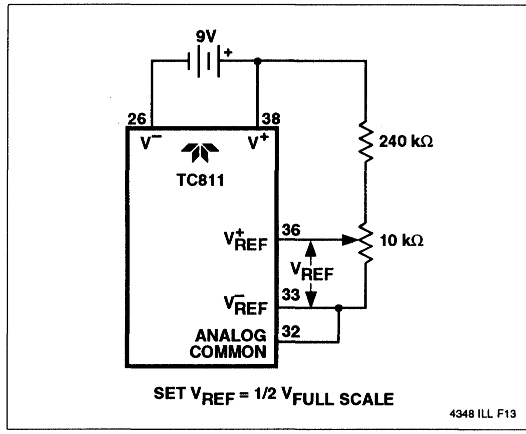


Figure 10 TC811 Internal Voltage Reference Connection

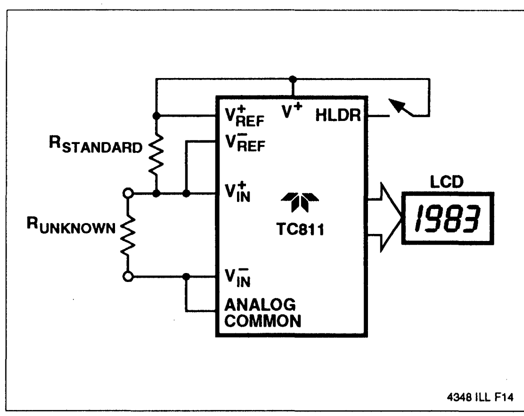


Figure 11 Low Parts Count Ratio Metric Resistance Measurement

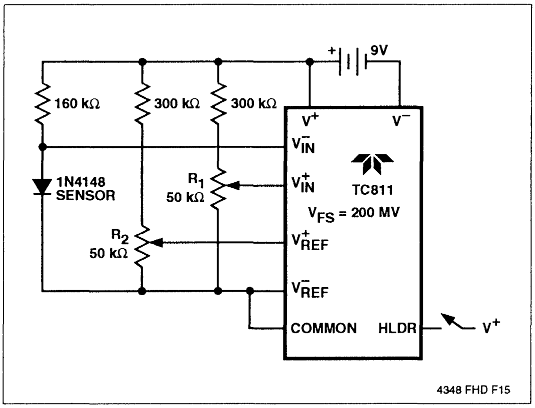


Figure 12 Temperature Sensor

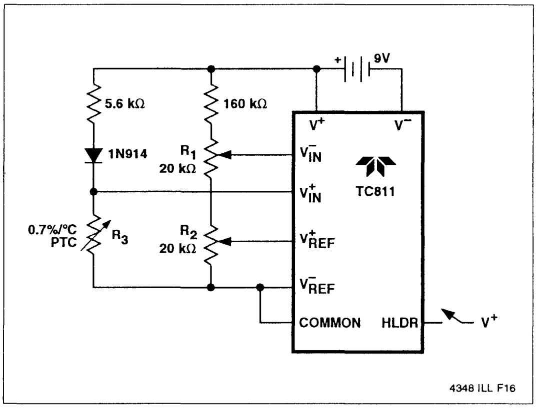


Figure 13 Positive Temperature Coefficient Resistor Temperature Sensor

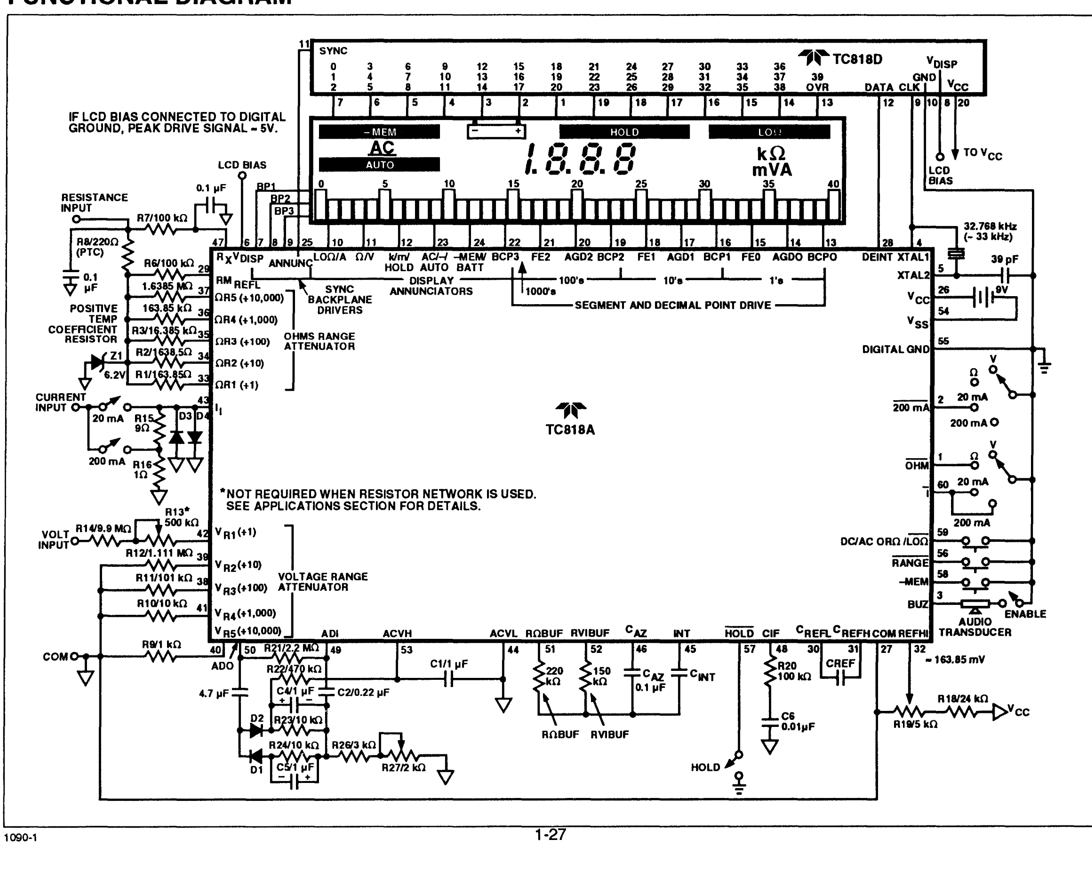
NOTES

AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH 3-1/2 DIGIT AND BAR-GRAPH DISPLAYS

FEATURES

- 3-1/2 Digit Numeric Plus 40-Segment Bar-Graph LCD Drivers
- Annunciator Outputs Permit Customizing of LCD
- 2-Chip Set, Surface-Mounted
  - — 60-Pin Flat Package
  - — 20-Pin Small Outline (SO)
- Auto-Range Operation for AC and DC Voltage and Resistance Measurements
- Two User-Selected AC/DC Current Ranges .... 20 mA and 200 mA
- 22 Operating Ranges
  - — 9 DC/AC Voltage
  - — 4 AC/DC Current
  - — 9 Resistance and Low-Power Ohms
- Display Hold Function
- 3-1/2 Digit Resolution in Auto-Range Mode ... 1/2000
- Extended Resolution in Manual Range Mode 1/3000
- Memory Mode for Relative Measurements .... ±5% F.S.
- Internal AC-to-DC Conversion Op Amp
- Triplex LCD Drive for Decimal Points, Digits, Bar-Graphs, and Annunciators
- Continuity Detection and Piezoelectric Transducer Driver
- Low-Drift Internal Reference .... 75 ppm/°C
- 9V Battery Operation .... 10 mW
- Low Battery Detection and LCD Annunciator

FUNCTIONAL DIAGRAM



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AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH 3-1/2 DIGIT AND BAR-GRAPH DISPLAYS

TC818

GENERAL DESCRIPTION

The TC818 is a 2-chip integrating analog-to-digital converter (ADC) with 3-1/2 digit numeric and 40-segment bar-graph LCD drivers, automatic ranging, and single 9V battery operation. The TC818 chip set (consisting of the TC818A and TC818D), combines the precision of a numeric display with the quick recognition of a bar-graph. The numeric display is driven by the TC818A, which also includes the ADC. The bar-graph display is driven by the TC818D.

The 40-segment bar-graph display provides "quick-look" perception of amplitude. Recognizing trends is also easier with a bar-graph, making TC818-based instruments valuable in nulling, tuning, calibration, and similar applications. On the other hand, the numeric display provides 0.05% resolution and a full set of annunciators that spell out the TC818's many operating modes.

Automatic range selection is provided for both voltage (DC and AC) and ohms (high and low power) measurements. Expensive and bulky mechanical range switches are not required. Five full-scale ranges are available, with automatic selection of external volt/ohm attenuators over a 1 to 10,000 range. Two current ranges, 20 mA and 200 mA, can be manually selected. The auto-range feature can be bypassed, allowing input attenuator selection through a single line input.

During manual mode operation, resolution is extended to 3000 counts full-scale. Extended resolution is also available during 2000 kΩ and 2000V full-scale auto-range operation. The extended range operation is indicated by a flashing 1 MSD and by the fully-extended bar-graph.

The TC818 includes an AC-to-DC converter for AC voltage and current measurements. Only external diodes/resistors/capacitors are required. Other features include a memory mode, low-battery detection, display $\overline{\text{HOLD}}$ input, and continuity buzzer driver.

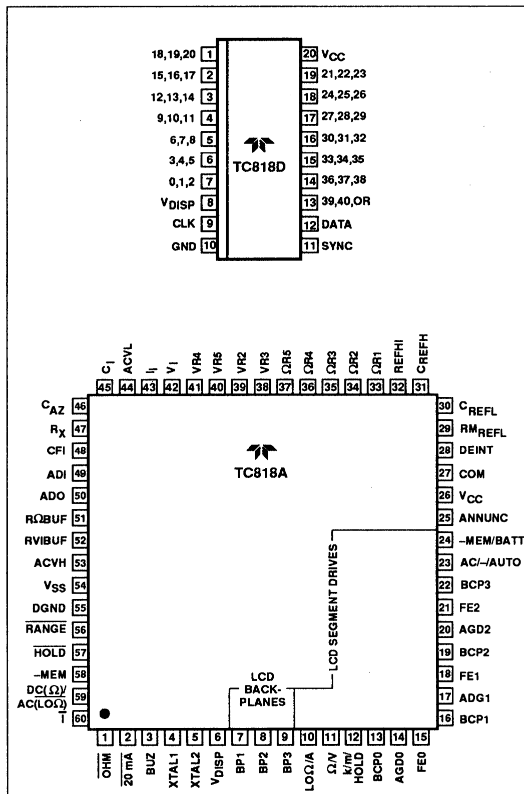
The 3-1/2 digit numeric display includes a full set of annunciators. Decimal points are adjusted as automatic or manual range changes occur, and voltage, current, and ohms operating modes are displayed. Additional annunciators are activated for manual, auto, memory, $\overline{\text{HOLD}}$, AC, low-power ohms, and low-battery conditions.

The TC818 is available in a surface-mounted chip set, with the TC818A in a 60-pin flat package and the TC818D in a 20-pin small outline (SO) package. Combining numeric and bar-graph display drivers, single 9V battery operation, internal range switching, and compact surface mounting, the TC818 is ideal for advanced portable instruments.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC818ACBQ	60-Pin Plastic Flat	0°C to +70°C
TC818DCOP	20-Pin SO	0°C to +70°C

PIN CONFIGURATIONS



AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH 3-1/2 DIGIT AND BAR-GRAPH DISPLAYS

ABSOLUTE MAXIMUM RATINGS

TC818A

Supply Voltage ....+15V
Analog Input Voltage .... V_{CC} to V_{SS}
Reference Input Voltage .... V_{CC} to V_{SS}
Voltage at Pin 43 ....Common ±0.7V
Power Dissipation ....800 mW

TC818D

Supply Voltage ....+6V
Digital Input Voltage .... V_{CC} to GND
Power Dissipation ....500 mW

Both Devices

Operating Temperature Range ....0°C to +70°C
Storage Temperature Range..................–65°C to +150°C
Lead Temperature (Soldering, 60 sec)..................+300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 9V, T_A = +25°C, Figure 1 Test Circuit

Symbol	Parameter	Test Conditions	TC818A Min	TC818A Typ	TC818A Max	Unit
	Zero Input Reading	200 mV Range Without 10 MΩ Resistor 200 mV Range With 10 MΩ Resistor 20 mA and 200 mA Range	–0000 –0001 –0000	0000 — 0000	+0000 +0001 +0000	Digital Reading
RE	Roll-Over Error	200 mV Range Without 10 MΩ Resistor 200 mV Range With 10 MΩ Resistor 20 mA and 200 mA Range	— — —	— — —	±1 ±3 ±1	Counts
NL	Linearity Error	Best Case Straight Line	—	—	±1	Count
I_{IN}	Input Leakage Current		—	—	10	pA
e_N	Input Noise	BW = 0.1 to 10 Hz	—	20	—	μV_{P-P}
	AC Frequency Response	±1% Error ±5% Error	— —	40 to 500 40 to 2000	— —	Hz
	Open Circuit Voltage for Ohm Measurements	Excludes 200Ω Range	—	570	660	mV
	Open Circuit Voltage for $\overline{LO}$ Ohm Measurements	Excludes 200Ω Range	—	285	350	mV
V_{COM}	Analog Common Voltage	(V_{CC} – V_{COM})	2.8	3	3.3	V
V_{CTC}	Common Voltage Temperature Coefficient		—	—	50	ppm/°C
		Display Multiplex Rate	—	100	—	Hz
V_{IL}	Low Logic Input	$\overline{20mA}$, AC, I, $\overline{LO\Omega}$, HOLD Range, –MEM, Ohms (Relative to DIGITAL GND, Pin 55)	—	—	1	V
	Logic 1 Pull-Up	$\overline{20\ mA}$, AC, I, $\overline{LO\Omega}$, HOLD Range, –MEM, Ohms (Relative to DIGITAL GND, Pin 55)	—	25	—	µA
V_{OL}	Low Logic Output	ANNUNC, DEINT; I_L = 100 µA	—	DGND+0.1	—	V
V_{OH}	High Logic Output	ANNUNC, DEINT; I_L = 100 µA	—	V_{CC}–0.1	—	V
	Buzzer Driver Frequency		—	4	—	kHz
	Low Battery Flag Voltage	V_{CC} to V_{SS}	6.3	6.6	7	V
	Operating Supply Current		—	0.8	1.5	mA

ELECTRICAL CHARACTERISTICS: V_{CC} = 5V, GND = 0V, T_A = +25°C

Symbol	Parameter	Test Conditions	TC818D Min	TC818D Typ	TC818D Max	Unit
V_{IH}	High Logic Input		2.5	—	—	V
V_{IL}	Low Logic Input		—	—	1	V
I_{IL}	Logic Input Current	V_{CC} ˜ V_{IN} ˜ GND	—	0.01	10	nA
	Display Multiplex Rate		—	100	—	Hz
	Operating Supply Current		—	40	100	µA

TC818A PIN DESCRIPTION

Pin No. (Quad Flat Package)	Symbol	Description
1	$\overline{\text{OHM}}$	Logic input. "0" (digital ground) for resistance measurement.
2	$\overline{\text{20 mA}}$	Logic Input. "0" (digital ground) for 20 mA full-scale current measurement.
3	BUZ	Buzzer. Audio frequency, 4 kHz, output for continuity indication during resistance measurement. A noncontinuous 4 kHz signal is output to indicate an input overrange during voltage or current measurements.
4	XTAL1	32.768 kHz crystal connection and clock output to drive TC818D.
5	XTAL2	32.768 kHz crystal connection.
6	V_{DISP}	Sets peak LCD drive signal: $V_P = V_{CC} = V_{DISP}$. V_{DISP} may also be used to compensate for temperature variation of LCD crystal threshold voltage.
7	BP1	LCD backplane #1.
8	BP2	LCD backplane #2.
9	BP3	LCD backplane #3.
10	LOΩ/A	LCD annunciator segment drive for low ohms resistance measurement and current measurement.
11	Ω/A	LCD annunciator segment drive for resistance measurement and current measurement.
12	k/m/HOLD	LCD annunciator segment drive for k ("kilo-Ohms"), m ("milli-Amps" and "milli-Volts") and HOLD mode.
13	BCP0 (Ones Digit)	LCD segment drive for "b," "c" segments and decimal point of least significant digit (LSD).
14	ADG0	LCD segment drive for "a," "g," "d" segments of LSD.
15	FE0	LCD segment drive for "f" and "e" segments of LSD.
16	BCP1	LCD segment drive for "b," "c" segments and decimal point of second LSD.
17	ADG1	LCD segment drive for "a," "g," "d" segments of second LSD.
18	FE1	LCD segment drive for "f" and "e" segments of second LSD.
19	BCP2	LCD segment drive for "b," "c" segments and decimal point of third LSD (hundreds digit).
20	ADG2	LCD segment drive for "a," "g," "d" segments of third LSD.
21	FE2	LCD segment drive for "f" and "e" segments of third LSD.
22	BCP3	LCD segment drive for "b," "c" segments and decimal point of MSD (thousands digit).
23	AC/–/AUTO	LCD annunciator segment drive for AC measurements, polarity, and auto-range operation.
24	–MEM/BATT	LCD annunciator segment drive for low-battery indication and memory (relative measurement).
25	ANNUNC	Square-wave output at the backplane frequency, synchronized to BP1. ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off. ANNUNC is also used to synchronize the TC818A and TC818D backplanes.
26	V_{CC}	Positive battery supply connection.
27	COM	Analog circuit ground reference point. Nominally 3V below V_{CC}.
28	DEINT	Deintegrate output. Transmits the A/D conversion result to the bar-graph LCD driver. (See text.)
29	RM_{REFL}	Ratiometric (resistance measurement) reference low voltage.
30	C_{REFL}	Reference capacitor negative terminal, $C_{REF} = 0.1\ \mu F$.
31	C_{REFH}	Reference capacitor positive terminal, $C_{REF} = 0.1\ \mu F$.
32	REFHI	Reference voltage for voltage and current measurement. Nominally 163.85 mV.
33	ΩR1	Standard resistor connection for 200Ω full-scale.
34	ΩR2	Standard resistor connection for 2000Ω full-scale.
35	ΩR3	Standard resistor connection for 20 kΩ full-scale.
36	ΩR4	Standard resistor connection for 200 kΩ full-scale.

TC818A PIN DESCRIPTION (Cont.)

Pin No. (Quad Flat Package)	Symbol	Description
37	ΩR5	Standard resistor connection for 2000 kΩ full-scale.
38	VR3	Voltage measurement ÷100 attenuator.
39	VR2	Voltage measurement ÷10 attenuator.
40	VR5	Voltage measurement ÷10,000 attenuator.
41	VR4	Voltage measurement ÷1000 attenuator.
42	V_I	Unknown voltage input ÷ attenuator.
43	I_I	Unknown current input.
44	ACVL	Low output of AC-to-DC converter.
45	C_I	Integrator capacitor connection. Nominally 0.1 µF. (Must have low dielectric absorption. Polypropylene dielectric suggested.)
46	C_{AZ}	Auto-zero capacitor connection. Nominally 0.1 µF.
47	R_X	Unknown resistance input.
48	CFI	Input filter connection.
49	ADI	Negative input of internal AC-to-DC operational amplifier.
50	ADO	Output of internal AC-to-DC operational amplifier.
51	RΩBUF	Active buffer output for resistance measurement. Integration resistor connection. Nominally 220 kΩ.
52	RVIBUF	Active buffer output for voltage and current measurement. Integration resistor connection. Nominally 150 kΩ.
53	ACVH	Positive output of AC-to-DC converter.
54	V_{SS}	Negative supply connection. Connect to negative terminal of 9V battery.
55	DGND	Internal logic digital ground. Ground connection for the TC818D, and the logic "0" level. Nominally 4.7V below V_{CC}.
56	$\overline{\text{RANGE}}$	Input to set manual operation and change ranges.
57	$\overline{\text{HOLD}}$	Input to hold display. Connect to DGND to "freeze" display.
58	–MEM	Input to enter memory measurement mode for relative measurements. The two LSD's are stored and subtracted from future measurements.
59	DC (Ω)/ AC ($\overline{\text{LO}\Omega}$)	Input that selects AC or DC option during voltage/current measurements. For resistance measurements, the ohms or low power (voltage) ohms option can be selected.
60	$\overline{\text{I}}$	Input to select measurement. Connect to logic "0" (digital ground) for current measurement.

TC818D PIN DESCRIPTION

Pin No. (20-Pin SO)	Symbol	Description
1	18, 19, 20	Segments 18, 19, 20 of LCD.
2	15, 16, 17	Segments 15, 16, 17 of LCD.
3	12, 13, 14	Segments 12, 13, 14 of LCD.
4	9, 10, 11	Segments 9, 10, 11 of LCD.
5	6, 7, 8	Segments 6, 7, 8 of LCD.
6	3, 4, 5	Segments 3, 4, 5 of LCD.
7	0, 1, 2	Segments 0, 1, 2 of LCD.
8	V_{DISP}	Sets peak LCD voltage drive level. Connect to V_{DISP} of TC818A, or to GND of TC818D.
9	CLK	Clock input. Connect to XTAL1 output of TC818A.
10	GND	Digital ground. Connect to DGND of TC818A.
11	SYNC	Display SYNC input. Synchronizes backplanes of the TC818A and TC818D. Connect to ANNUNC output of TC818A.
12	DATA	Data input. Pulses at the CLK input are counted while DATA is logic high. Connect to DEINT output of TC818A.
13	39, 40, OR	Segments 39, 40 and overrange of LCD.
14	36, 37, 38	Segments 36, 37, 38 of LCD.
15	33, 34, 35	Segments 33, 34, 35 of LCD.
16	30, 31, 32	Segments 30, 31, 32 of LCD.
17	27, 28, 29	Segments 27, 28, 29 of LCD.
18	24, 25, 26	Segments 24, 25, 26 of LCD.
19	21, 22, 23	Segments 21, 22, 23 of LCD.
20	V_{CC}	Power supply input. Connect to V_{CC} of TC818A.

THEORY OF OPERATION

The TC818 consists of two CMOS integrated circuits. The TC818A incorporates an auto-ranging ADC and drivers for a 3-1/2 digit LCD, while the TC818D provides data formatting and drivers for a 40-segment bar-graph display. Both integrated circuits are required to form a complete measurement system.

During each A/D conversion cycle, data is transferred from the TC818A to the TC818D. Therefore, the bar-graph display will track the numeric (3-1/2 digit) display. The exact relationship between numeric display counts and bar-graph segments displayed is shown in Table I. Both displays are updated at the same rate. When the TC818A is in its extended resolution mode (3000 counts, maximum), the bar-graph will display all 40 bars continuously.

Analog-to-Digital Converter (ADC)

The TC818A includes an integrating ADC with auto-ranging resolution of 2000 counts and manual range resolution of 3000 counts. Figure 1 shows a simplified schematic of the analog section. In auto-ranging mode, internal logic will adjust the input voltage or ohms attenuators so that measurements will always be made in the appropriate range. Measurement ranges, logic control inputs, 3-1/2 digit LCD formatting, and other features are identical to the TC815 auto-ranging A/D converter. However, the TC818A is not pin-compatible with, and is not a replacement for, the TC815.

A display annunciator output (ANNUNC) can be used to customize the LCD. ANNUNC is a square wave at the backplane frequency. Connecting an annunciator segment to the ANNUNC driver turns the segment on; connecting the segment to its backplane turns it off.

Bar-Graph Driver

The TC818D includes a counter and data latch, clock divider, and triplex LCD bar-graph formatting and display functions. A block diagram of the TC818D and connections between the TC818A and TC818D is shown in Figure 2. The TC818D does not require a separate power supply, since it is powered from V_{CC} and digital ground of the TC818A.

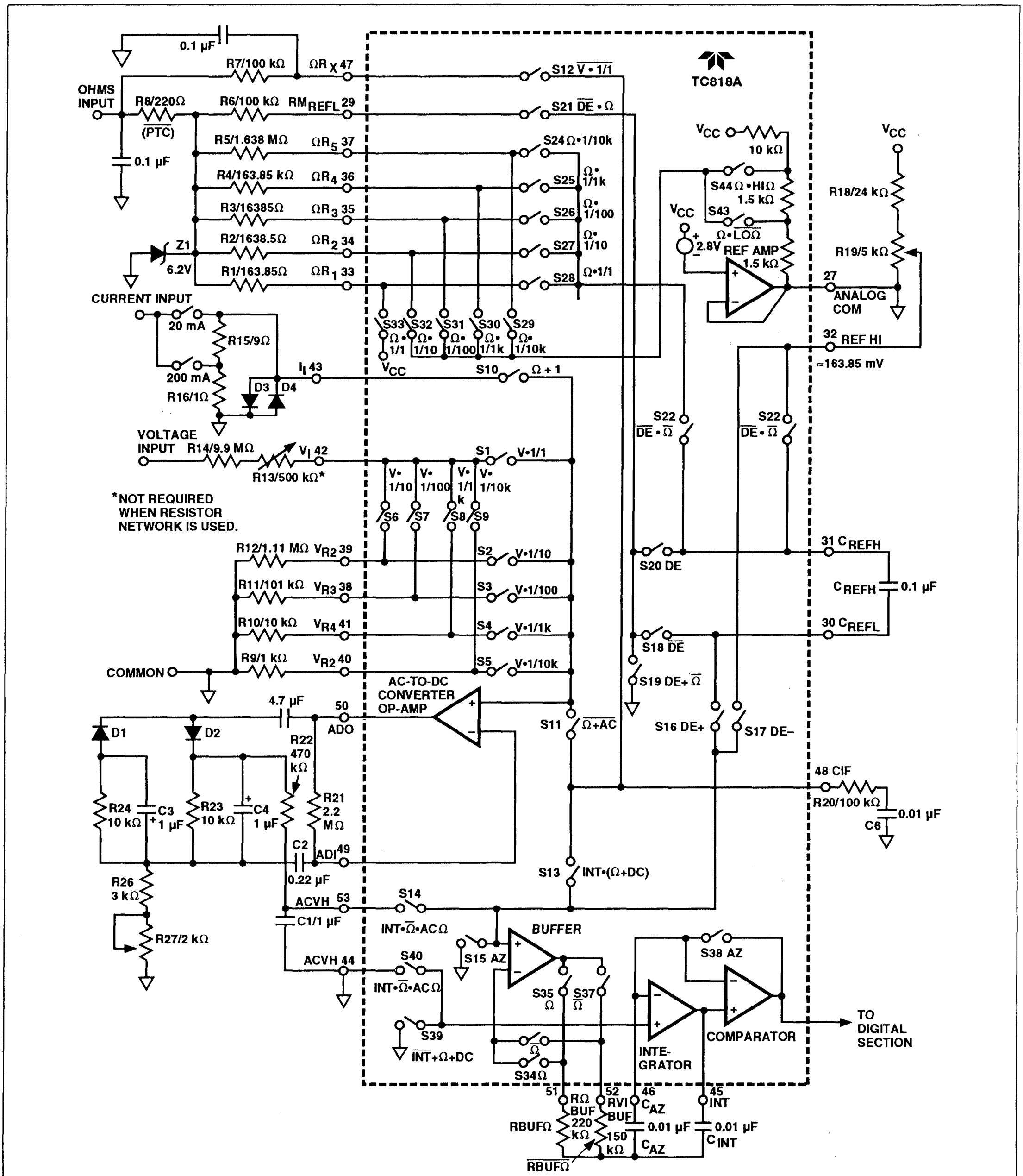


Figure 1 TC818A Analog Section

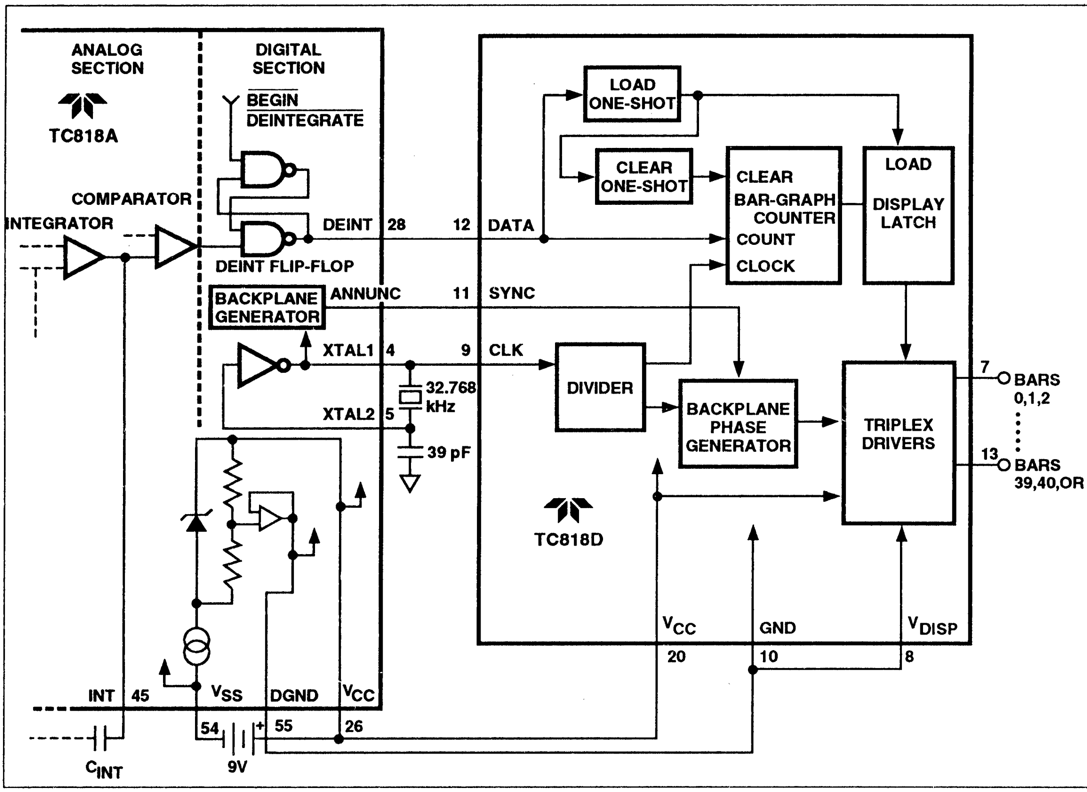


Figure 2 Interface Between TC818A and TC818D

When the TC818D DATA input goes to a logic high, pulses are counted at the CLK input. A clock divider scales clock pulses so that the number of LCD bar-graph segments is proportional to the numeric display (see Table I).

When the DATA input goes low, the counter contents are transferred to a display latch. Then the bar-graph counter is reset to zero in preparation for the next A/D conversion cycle.

The CLK input is also divided to produce the triplex LCD drivers. The backplane and segment driver waveforms are the same voltage levels as the TC818A. However, the TC818D segment driver waveforms are less complicated than those of the TC818A, because adjacent bar-graph segments are either on or off.

The SYNC input permits synchronizing display backplanes. By connecting the ANNUNC output of the TC818A to the SYNC input of the TC818D, the two sets of LCD drivers will be synchronized. This feature permits the use of an LCD with only one set of backplane drivers and saves three pin connections to the display.

LCD backplane and segment drive voltages are set by the voltage between V_{CC} and V_{DISP} pins. In most cases, V_{DISP} will be connected to GND and the LCD drive voltage will be about 5V. If V_{DISP} is not connected to GND, then V_{DISP} of the TC818D must be connected to V_{DISP} of the TC818A.

Data Transfer

Analog conversion results are transferred from the TC818A to the TC818D via two pins, DEINT and XTAL1. DEINT is a TC818A output with a pulse width proportional to the analog voltage being measured. DEINT goes to a logic high at the beginning of the TC818A deintegrate cycle, and goes low at the comparator zero-crossing (end of conversion).

Timing of the DEINT pulse width is derived from the TC818A's XTAL1 output, which provides a 32.768 kHz clock. The number of clock pulses occurring while DEINT is high determines the number of bar-graph segments displayed. The relationship between numeric display counts and bar-graph segments is shown in Table I.

Resistance, Voltage, Current Measurement Selection

The TC818 is designed to measure voltage, current, and resistance. Auto-ranging is available for resistance and voltage measurements. The $\overline{\text{OHM}}$ (pin 1) and $\overline{\text{I}}$ (pin 60) input controls are normally pulled internally to V_{CC}.

By tying these pins to DGND (pin 55), the TC818 is configured internally to measure resistance, voltage, or current. The required signal combinations are shown in Table II.

Table I. TC818A Numeric Display vs TC818D Bar-Graph Segments

Numeric Reading	Bar-Graph Segments
0–24	0
25–74	1
75–124	2
•	•
•	•
•	•
((50*N)–25) to ((50*N)+24) (where 1 ≤ N ≤ 40)	N
•	•
•	•
•	•
1975–2024*	40
>2024*	OVR

*Readings >1999 will only occur in manual or expanded resolution modes.

Table II. TC818 Measurement Selection Logic

Function Select Pin $\overline{\text{OHM}}$ (Pin 1)	$\overline{\text{I}}$ (Pin 60)	Selected Measurement
0	0	Voltage
0	1	Resistance
1	0	Current
1	1	Voltage

0 = Digital Ground 1 = Floating or Tied to V_{CC}

NOTES: 1. $\overline{\text{OHM}}$ and $\overline{\text{I}}$ are normally pulled internally high to V_{CC} (pin 26). This is considered a logic "1".
2. Logic "0" is the potential at digital ground (pin 55).

Resistance Measurements — Ohms and Low Power Ohms

The TC818 can be configured to reliably measure in-circuit resistances shunted by semiconductor junctions. The TC818 low-power ohms measurement mode limits the probe open circuit voltage. This prevents semiconductor junctions in the measured system from turning on.

In the resistance measurement mode, the $\Omega/\overline{\text{LO}\Omega}$ (pin 59) input selects the low-power ohms measurement mode. For low-power ohms measurements, $\Omega/\overline{\text{LO}\Omega}$ (pin 59) is momentarily brought low to digital ground potential. The TC818 sets up for a low-power ohms measurement with a maximum open circuit probe voltage of 0.35V above analog common. In the low-power ohms mode, an LCD annunciator, $\overline{\text{LO}\Omega}$, will be activated. On power-up, the low-power ohms mode is not active.

If the manual operating mode has been selected, toggling $\Omega/\overline{\text{LO}\Omega}$ resets the TC818 back to auto-range mode. In manual mode, the decision to make a normal or low-power ohms measurement should be made before selecting the desired range.

The low-power ohms measurement is not available on the 200Ω full-scale range. Open-circuit voltage on this range is below 2.8V.

The standard resistance values are listed in Table III.

Table III. Ohms Range Ladder Network

Full-Scale Range	Standard Resistance	Low-Power Ohms Mode
200Ω	163.85Ω (R1)	No
2000Ω	1638.5Ω (R2)	Yes
20 kΩ	16,385Ω (R3)	Yes
200 kΩ	163,850Ω (R4)	Yes
2000 kΩ	1,638,500Ω (R5)	Yes

R8, a positive temperature coefficient resistor, and the 6.2V zener, Z1, provide input voltage protection during ohms measurement.

Ratiometric Resistance Measurements

The TC818 measures resistance ratiometrically. Accuracy is set by the external standard resistors connected to pins 33 through 37. A low-power ohms mode may be selected on all but the 200Ω full-scale range. The low-power ohms mode limits the voltage applied to the measured system. This allows accurate "in-circuit" measurements when a resistor is shunted by semiconductor junctions.

Full auto-ranging is provided. External precision standard resistors are automatically switched to provide the proper range.

Figure 3 is a detailed block diagram of the TC818 configured for ratiometric resistance measurements. During the signal integrate phase the reference capacitor charges to a voltage inversely proportional to the measured resistance, R_X. Figure 4 shows that the conversion accuracy relies only on the accuracy of the external standard resistors.

Normally, the required accuracy of the standard resistances will be dictated by the accuracy specifications of the user's end product. Table IV gives the equivalent ohms per count for various full-scale ranges to allow users to judge the required resistor accuracy.

Table IV. Reference Resistors

Full-Scale Range (Ω)	Reference Resistor	Ω/Count
200	163.85	0.1
2k	1638.5	1
20k	16385	10
200k	163,850	100
2M	1,638,500	1000

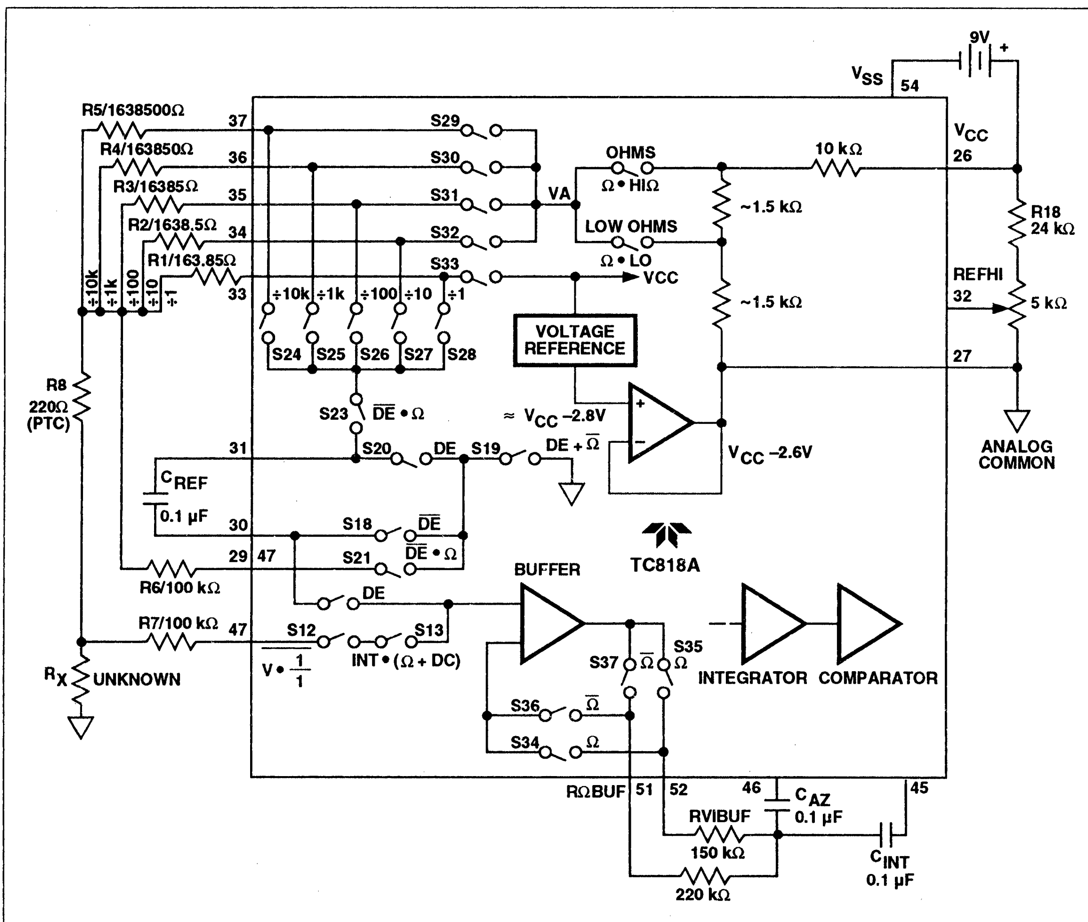
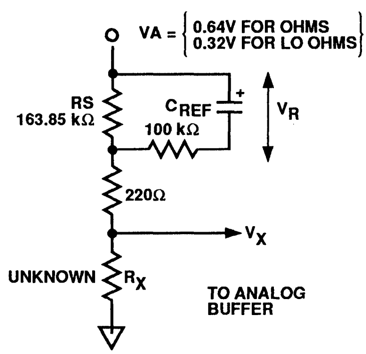


Figure 3 Ratiometric Resistance Measurement Functional Diagram

AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH 3-1/2 DIGIT AND BAR-GRAPH DISPLAYS



Example: 200 kΩ Full-Scale Measurement

(a) $V_R = \dfrac{163.85\ k\Omega}{163.85 + 220 + R_X}\ 3\ 0.64$

(b) $V_X = \dfrac{R_X}{163.85\ k\Omega + 220\Omega + R_X}\ 3\ 0.64$

(c) "Ramp-Up Voltage" = "Ramp-Down Voltage"

$$\therefore \frac{V_X}{R_I\,C_I} 3\ t_I = \frac{V_R}{R_I\,C_I} t_{DE}$$

where:
R_I = Integrating Resistor, t_I = Integrate Time
C_I = Integrating Capacitor, t_{DE} = Deintegrate Time

(d) $R_X = 163.85 \left(\dfrac{t_{DE}}{t_I} \right)$

Independent of R_I, C_I or internal voltage reference.

Figure 4 Resistance Measurement Accuracy Set by External Standard Resistor

Voltage Measurement

Resistive dividers are automatically changed to provide in-range readings for 200 mV to 2000V full-scale readings (Figure 1). The input resistance is set by external resistors R14/R13. The divider leg resistors are R9–R12. The divider leg resistors give a 200 mV signal at V_I (pin 42) for full-scale voltages from 200 mV to 2000V.

For applications that do not require a 10 MW input impedance, the divider network impedances may be lowered. This will reduce voltage offset errors induced by switch leakage currents.

Current Measurement

The TC818 measures current only under manual range operation. The two user-selectable, full-scale ranges are 20 mA and 200 mA. Select the current measurement mode by holding the I input (pin 60) low at digital ground potential. The $\overline{\text{OHM}}$ input (pin 1) is left floating or tied to the positive supply.

Two ranges are possible. The 200 mA full-scale range is selected by connecting the $\overline{\text{20 mA}}$ input (pin 2) to digital ground. If left floating, the 200 mA full-scale range is selected.

External current-to-voltage conversion resistors are used at the current input (I_I, pin 43). For 20 mA measurements, a 10Ω resistor is used. The 200 mA range requires a 1Ω resistor. Full scale is 200 mV

Printed circuit board trace resistance between analog common and R16 must be minimized. In the 200 mA range, for example, a 0.05Ω trace resistance causes a 5% current-to-voltage conversion error at I_I (pin 43).

The extended resolution measurement option operates during current measurements.

To minimize roll-over error, the potential difference between ANALOG COM (pin 27) and system common must be minimized.

AC-to-DC Measurements

In voltage and current measurements, the TC818 can be configured for AC measurements. An on-chip operational amplifier and external rectifier components perform the AC-to-DC conversion.

When power is first applied, the TC818 enters the DC measurement mode. For AC measurements (current or voltage), AC/DC (pin 59) is momentarily brought low to digital ground potential; the TC818 sets-up for AC measurements and the AC liquid crystal display annunciator activates. Toggling AC/DC low again returns the TC818 to DC operation.

If manual operating mode has been selected, toggling AC/DC resets the TC818 back to auto-range mode. In manual mode operation, AC or DC should be selected first, then the desired range.

The minimum AC full-scale voltage range is 2V. The DC full-scale minimum voltage is 200 mV.

AC current measurements are available on the 20 mA and 200 mA full-scale ranges.

Conversion Timing

The TC818 uses the conventional dual-slope integrating conversion technique with an added phase that automatically eliminates zero offset errors. The TC818 gives a zero reading with a 0V input.

This device is designed to operate with a low-cost, readily-available 32.768 kHz crystal. It serves as a time-base oscillator crystal in many digital clocks. (See external crystal sources, page 18.)

The external clock is divided by two. The internal clock frequency is 16.348 kHz, giving a clock period of 61.04 µs. The total conversion — auto-zero phase, signal integrate, and reference deintegrate — requires 8000 clock periods (or 488.3 ms). There are approximately two complete conversions per second.

The integration time is fixed at 1638.5 clock periods (or 100 ms), giving a rejection of 50/60 Hz AC line noise.

The maximum reference deintegrate time, representing a full-scale analog input, is 3000 clock periods (or 183.1 ms) during manual extended resolution operation. The 3000 counts are available in manual mode, extended resolution operation only. In auto-ranging mode, the maximum deintegrate time is 2000 clock periods. The 1000 clock periods are added to the auto-zero phase. An auto-ranging or manual conversion takes 8000 clock periods. After a zero crossing is detected in the reference deintegrate mode, the auto-zero phase is entered.

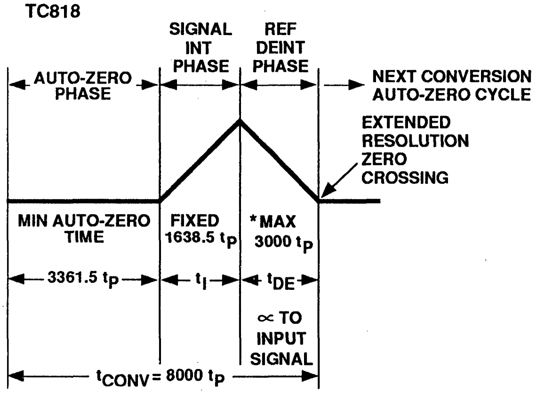
Figure 5 shows the basic TC818 timing relationships.

Manual Range Selection

The TC818's voltage and resistance auto-ranging feature can be disabled by momentarily bringing RANGE (pin 56) to digital ground potential (pin 55). When the change from auto to manual ranging occurs, the first manual range selected is the last range in the auto-ranging mode.

The TC818's power-up circuit initially selects auto-range operation. Once the manual-range option is entered, range changes are made by momentarily grounding the RANGE control input. The TC818 remains in the manual-range mode until the measurement function (voltage or resistance) or measurement option (AC/DC, $\Omega/\overline{LO\Omega}$) changes, causing the TC818 to return to auto-ranging operation.

TC818



*IN AUTO-RANGE OPERATION, MAXIMUM IS 2000 tP AND MINIMUM AUTO-ZERO TIME IS 4361.5 t_P.

External Crystal = 32.768 kHz

Internal Clock Period = t_P = 2/32.768 = 61.04 µs

Total Conversion Time = t_{CONV} = 8000 (t_P)
= 488.3 ms ≈ 2 conv/sec

Integration Time = t_I = 1638.5 (t_P) = 100 ms

Maximum Reference Deintegrate Time
= t_{DE} = 3000 (t_P) = 183.1 ms (manual, extended resolution)
= 2000 (t_P) = 122.1 ms (auto-range)

Minimum Auto-Zero Time
= (8000–3000–1638.5) (t_P) = 205.1 ms (manual, extended resolution)
= (8000–2000–1638.5) (t_P) = 266.2 ms (auto-range)

Figure 5 Basic TC818 Conversion Timing

The "Auto" LCD annunciator driver is active only in the auto-range mode.

Figure 6 shows typical operation where the manual range selection option is used. Also shown is the extended resolution display format.

Extended Resolution Manual Operation

When operated in the manual-range mode, the TC818 extends resolution by 50% for current, voltage, and resistance measurements. Resolution increases to 3000 counts from 2000 counts. The extended resolution feature operates only in the 2000 kΩ and 2000V ranges during auto-range operation.

In the extended resolution operating mode, readings above 1999 are displayed with a blinking "1" most significant digit. The blinking "1" should be interpreted as the digit 2. The three least significant digits display data normally. The bar-graph LCD will be fully extended.

An input overrange condition causes the most significant digit (MSD) to blink and sets the three least significant digits (LSDs) to display "000." The buzzer output is enabled for input voltage and current signals with readings greater than 2000 counts in both manual- and auto-range operations.

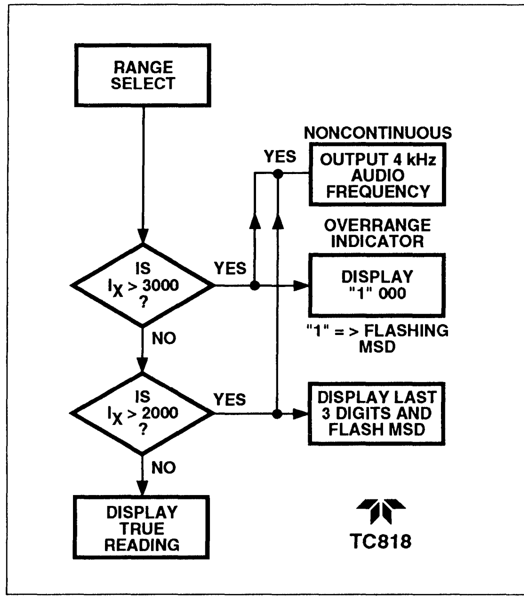


Figure 7 Manual Range Selection; Current Measurement

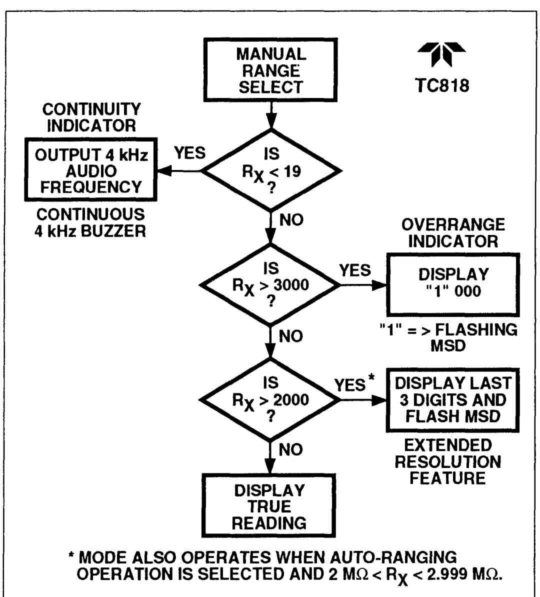


Figure 6 Manual Range Selection; Resistance Measurement

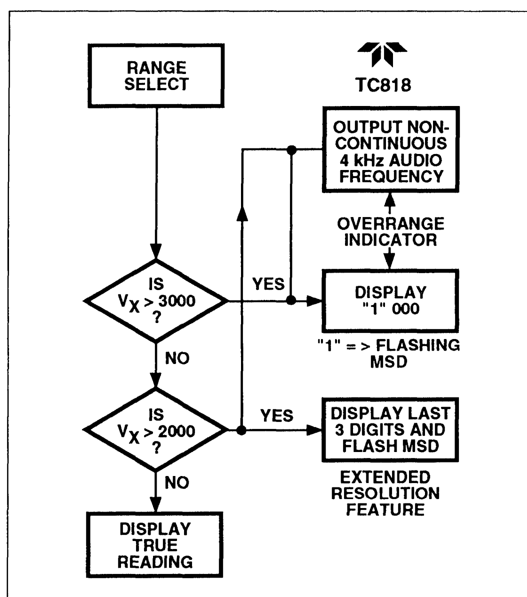


Figure 8 Manual Range Selection; Voltage Measurement

For resistance measurements, the buzzer signal does not indicate an overrange condition. The buzzer is used to indicate continuity. Continuity is defined as a resistance reading less than 19 counts.

–MEM Operating Mode

Bringing –MEM (Pin 58) momentarily low configures the "–MEM" operating mode. The –MEM LCD annunciator becomes active. In this operating mode subsequent measurements are made relative to the last two digits (≤ 99) displayed at the time MEM is low. This represents 5% of full-scale. The last two significant digits are stored and subtracted from all the following input conversions.

A few examples clarify operation:

Example 1: *In Auto-Ranging*

R_I (N) = 18.21 kΩ (20 kΩ Range) ≥ Display 18.21 kΩ
MEM ≥ Store 0.21 kΩ

R_I (N + 1) = 19.87 kΩ (20 kΩ Range)
≥ Display 19.87 – 0.21 = 19.66 kΩ

R_I (N + 2) = 22.65 kΩ (200 kΩ Range)
≥ Display 22.7 kΩ and MEM Disappears

Example 2: *In Fixed Range 200Ω Full Scale*

R_I (N) = 18.2Ω ≥ Display 18.2Ω
MEM ≥ Store 8.2Ω

R_I (N + 1) = 36.7Ω
≥ Display 36.7 – 8.2 = 28.5Ω

R_I (N + 2) = 5.8Ω
≥ Display 5.8 – 8.2 = –2.4Ω*

*Will display minus resistance if following input is less than offset stored at fixed range.

Example 3: *In Fixed Range 20V Full Scale*

V_I (N) = 0.51V ≥ Display 0.51V
MEM ≥ Store 0.51V

V_I (N + 1) = 3.68V
≥ Display 3.68 – 0.51 = 3.17V

V_I (N + 2) = 0.23V
≥ Display 0.23 – 0.51 = –0.28V

V_I (N + 3) = –5.21V
≥ Display –5.21 – 0.51 = –5.72V

On power-up the, –MEM mode is not active. Once the –MEM is entered, bringing MEM low again returns the TC818 to normal operation.

The –MEM mode is also cancelled whenever the measurement type (resistance, voltage, current, AC/DC, Ω/$\overline{\text{LO}\Omega}$) or range is changed. The LCD –MEM annunciator will be off in normal operation.

In auto-range operation, if the following input signal cannot be converted on the same range as the stored value, the –MEM mode is cancelled. The LCD annunciator is turned off.

The –MEM operating mode can be very useful in resistance measurements where lead length resistance would cause measurement errors.

Automatic Range Selection Operation

When power is first applied, the TC818 enters the auto-range operating state. The auto-range mode may be entered from manual mode by changing the measurement function (resistance or voltage) or by changing the measurement option (AC/DC, Ω/$\overline{\text{LO}\Omega}$).

The automatic voltage range selection begins on the most sensitive scale first: 200 mV for DC or 2V for AC measurements. The voltage range selection flow chart is given in Figure 9.

Internal input protection diodes to V_{CC} (pin 26) and V_{SS} (pin 54) clamp the input voltage. The external 10 MΩ input resistance (see R14 and R13, Functional Diagram) limits current safely in an overrange condition.

The voltage range selection is designed to maximize resolution. For input signals less than 9% of full scale (count reading <180), the next most sensitive range is selected.

An overrange voltage input condition is flagged, whenever the internal count exceeds 2000, by activating the buzzer output (pin 3). This 4 kHz signal can directly drive a piezoelectric acoustic transducer. An out-of-range input signal causes the 4 kHz signal to be on for 122 ms, off for 122 ms, on for 122 ms, and off for 610 ms (see Figure 15).

During voltage auto-range operation, the extended resolution feature operates on the 2000V range only. (See extended resolution operating mode discussion.)

The resistance auto-range selection procedure is shown in Figure 10. The 200Ω range is the first range selected unless the low ohms resistance measurement option is selected. In low ohms operation, the first full-scale range tried is 2 kΩ.

The resistance range selected maximizes sensitivity. If the conversion results in a reading less than 180, the next most sensitive full-scale range is tried.

If the conversion is less than 19 in auto-range operation, a continuous 4 kHz signal is output at BUZ (pin 3). An overrange input does not activate the buzzer.

AUTO-RANGING ANALOG-TO-DIGITAL CONVERTER WITH 3-1/2 DIGIT AND BAR-GRAPH DISPLAYS

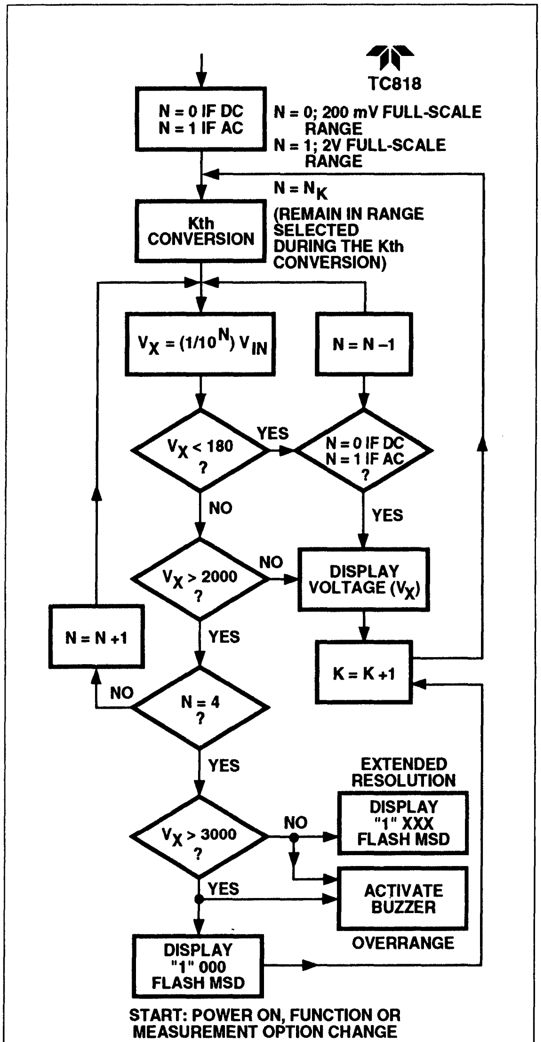


Figure 9 Auto-Range Operation; Voltage Measurement

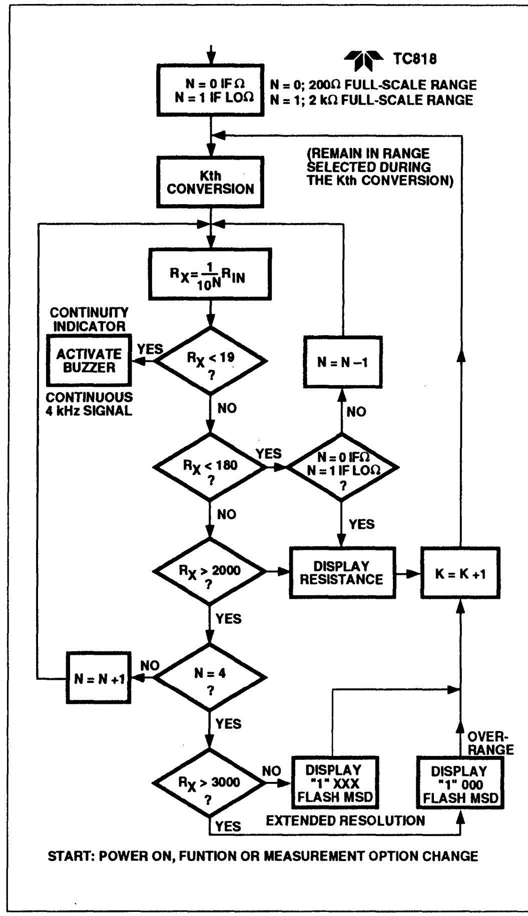


Figure 10 Auto-Range Operation; Resistance Measurement

Out-of-range input conditions are displayed by a blinking MSD with the three LSDs set to "000," and by the fully extended bar-graph.

The extended resolution feature operates only on the 200 kΩ and 2000V full-scale ranges during auto-range operation. A blinking "1" most significant digit is interpreted as the digit 2. The three LSDs display data normally.

Low-Battery Detection Circuit

The TC818 contains a low-battery detector. When the 9V battery supply has been depleted to a 7V nominal value, the LCD low-battery annunciator is activated.

The low-battery detector is shown in Figure 11. The low-battery annunciator is guaranteed to remain OFF with the battery supply greater than 7V. The annunciator is guaranteed to be ON before the supply battery has reached 6.3V.

Triplex Liquid Crystal Display (LCD) Drive

The TC818 directly drives a triplexed LCD using 1/3 bias drive. All numeric data, decimal point, polarity, and function annunciator drive signals are developed by the TC818A. The bar-graph data are developed to the TC818D. A direct connection to a triplex LCD is possible without external drive electronics. Standard and custom LCDs are readily available from LCD manufacturers.

The LCDs must be driven with an AC signal having a zero DC component, for long display life. The liquid crystal polarization is a function of the RMS voltage appearing across the backplane and segment driver. The peak drive signal applied to the LCD is:

$V_{CC} - V_{DISP}$

For example, if V_{DISP} is set at a potential 3V below V_{CC}, the peak drive signal is:

$V_P = V_{CC} - V_{DISP} = 3V$

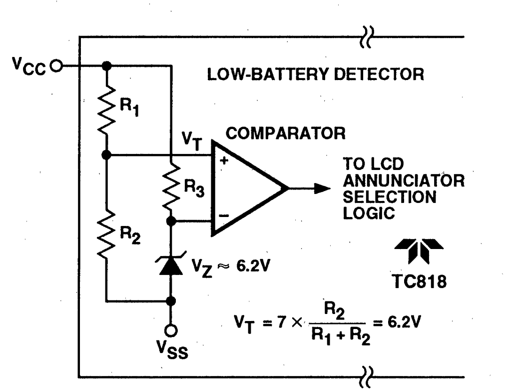


Figure 11 Low-Battery Detector

An "OFF" LCD segment has an RMS voltage of $V_P/3$ across it or 1V. An "ON" segment has a 0.63 V_P signal across it or 1.92V for $V_{CC} - V_{DISP} = 3V$.

Since the V_{DISP} pin is available, the user may adjust the "ON" and "OFF" LCD levels for various manufacturer's displays by changing V_P signal across it or 1.92V for $V_{CC} - V_{DISP} = 3V$.

"OFF" segments may become visible at high LCD operating temperatures. A voltage with a –5 to –20 mV/°C temperature coefficient can be applied to V_{DISP} to accommodate the liquid crystal temperature operating characteristics, if necessary.

The TC818A and TC818D internally generate two intermediate LCD drive potentials (V_H and V_L) from resistive dividers (Figure 12) between V_{CC} and V_{DISP}. The ladder impedance is approximately 150 kΩ. This drive method is commonly known as 1/3 bias. With V_{DISP} connected to digital ground, $V_P \approx 5V$.

The intermediate levels are needed so that drive signals giving RMS "ON" and "OFF" levels can be generated. Figure 13 shows a typical drive signal and the resulting waveforms for "ON" and "OFF" RMS voltage levels across a selected numeric LCD element.

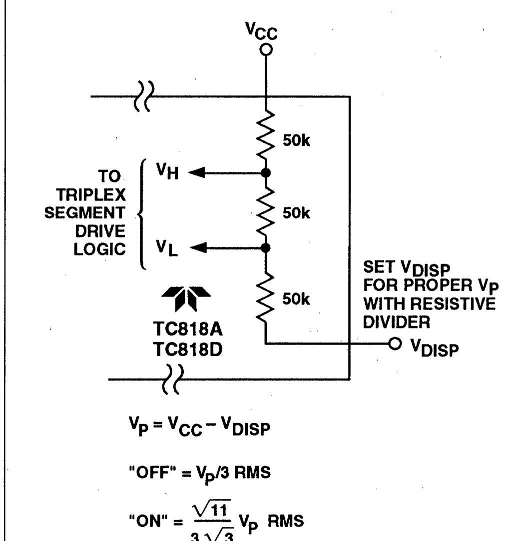


Figure 12 1/3 Bias LCD Drive

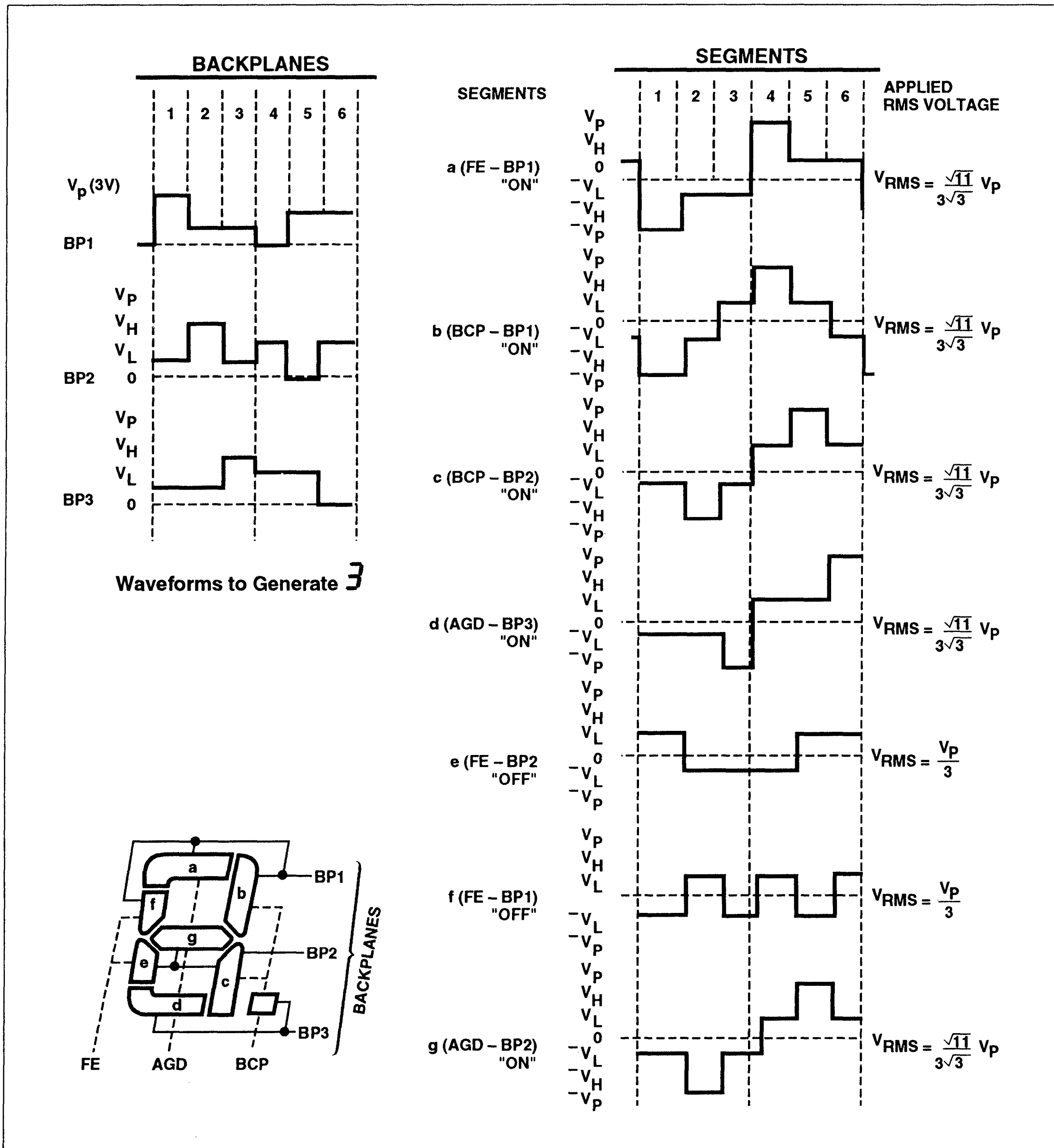


Figure 13 Triplex LCD Drive Waveforms

Liquid Crystal Displays (LCDs)

Most users design their own custom LCD. However, for prototyping purposes, a standard display is available from Varitronix, Ltd. The prototype display configuration is shown in Figure 14.

- Varitronix Ltd.
  9/F Liven House, 61-63, King Yip Street
  Kwun Tjong, Hong Kong
  Tel: 3-410286
  Telex: 36643 VTRAX HX
  FAX: 852-3-439555

  Part No. VIM-328-DP
- USA Office:
  VL Electronics Inc.
  3171 Los Feliz Blvd, #303
  Los Angeles, CA 0039
  Tel: (213) 738-8700

External Crystal

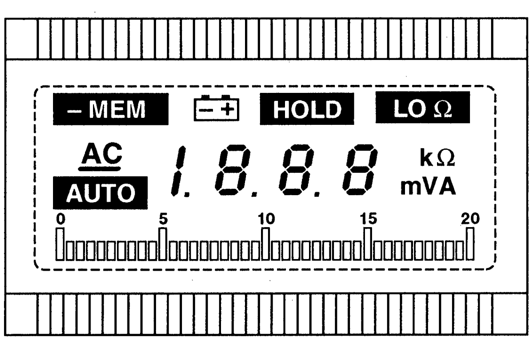
The TC818 is designed to operate with a 32,768 Hz crystal. This frequency is internally divided by two to give a 61.04 μs clock period. One conversion takes 8000 clock periods or 488.3 ms (≈2 conversions/second). Integration time is 1638.5 clock periods or 100 ms.

The 32 kHz quartz crystal is readily available and inexpensive. The 32 kHz crystal is commonly used in digital clocks and counters.

Several crystal sources exist. A partial listing is:

- Statek Corporation
  512 N. Main
  Orange, CA 92668
  (714) 639-7810
  TWX: 910-593-1355
  Telex: 67-8394
- Daiwa Sinku Corporation
  1389, Shinzaike – AZA-Kono
  Hirakacho, Kakogawa Hyogo, Japan
  Tel: 0794-26-3211
- International Piezo LTD
  24-26 Sze Shan Street
  Yau Ton, Hong Kong
  TLX: 35454 XTAL HZ
  Tel: 3-3501151

Contact manufacturer for full specifications.



PAD	BP1	BP2	BP3	PAD	BP1	BP2	BP3
1	—	—	SCALE	19	—	—	BP3
2	X0	X1	X2	20	—	BP2	—
3	X5	X4	X3	21	BP1	—	—
4	X6	X7	X8	22	—	LOΩ	A
5	X11	X10	X9	23	—	Ω	V
6	X12	X13	X14	24	HOLD	k	m
7	X17	X16	X15	25	4B	4C	—
8	X18	X19	X20	26	4A	4G	4D
9	X23	X22	X21	27	4F	4E	—
10	X24	X25	X26	28	3B	3C	3P
11	X29	X28	X27	29	3A	3G	3D
12	X30	X31	X32	30	3F	3E	—
13	X35	X34	X33	31	2B	2C	2P
14	X36	X37	X38	32	2A	2G	2D
15	—	X40	X39	33	2A	2G	2D
16	BP1	—	—	34	1B	1C	1P
17	—	BP2	—	35	Z	–MEM	—
18	—	—	BP3	36	AC	y	AUTO

Figure 14 Typical LCD Configuration, TC818 Triplex

"Buzzer" Drive Signal

The BUZ output (pin 3) will drive a piezoelectric audio transducer. The signal is activated to indicate an input overrange condition for current and voltage measurements or continuity during resistance measurements.

During a resistance measurement, a reading less than 19 on any full-scale range causes a continuous 4 kHz signal to be output. This is used as a continuity indication.

A voltage or current input measurement overrange is indicated by a noncontinuous 4 kHz signal at the BUZ output. The LCD most significant digit also flashes and the three least significant digits are set to display zero. The buzzer drive signal for overrange is shown in Figure 15. The BUZ output is active for any reading over 2000 counts in both manual and auto-range operation. The buzzer is activated during an extended resolution measurement.

The BUZ signal swings from V_{CC} (pin 26) to DGND (pin 55). The signal is at V_{CC} when not active.

The BUZ output is also activated for 15 ms whenever a range change is made in auto-range or manual operation. Changing the type of measurement (voltage, current, or resistance), or measurement option (AC/DC, $\Omega/\overline{LO\Omega}$), also activates the buzzer output for 15 ms. A range change during a current measurement will not activate the buzzer output.

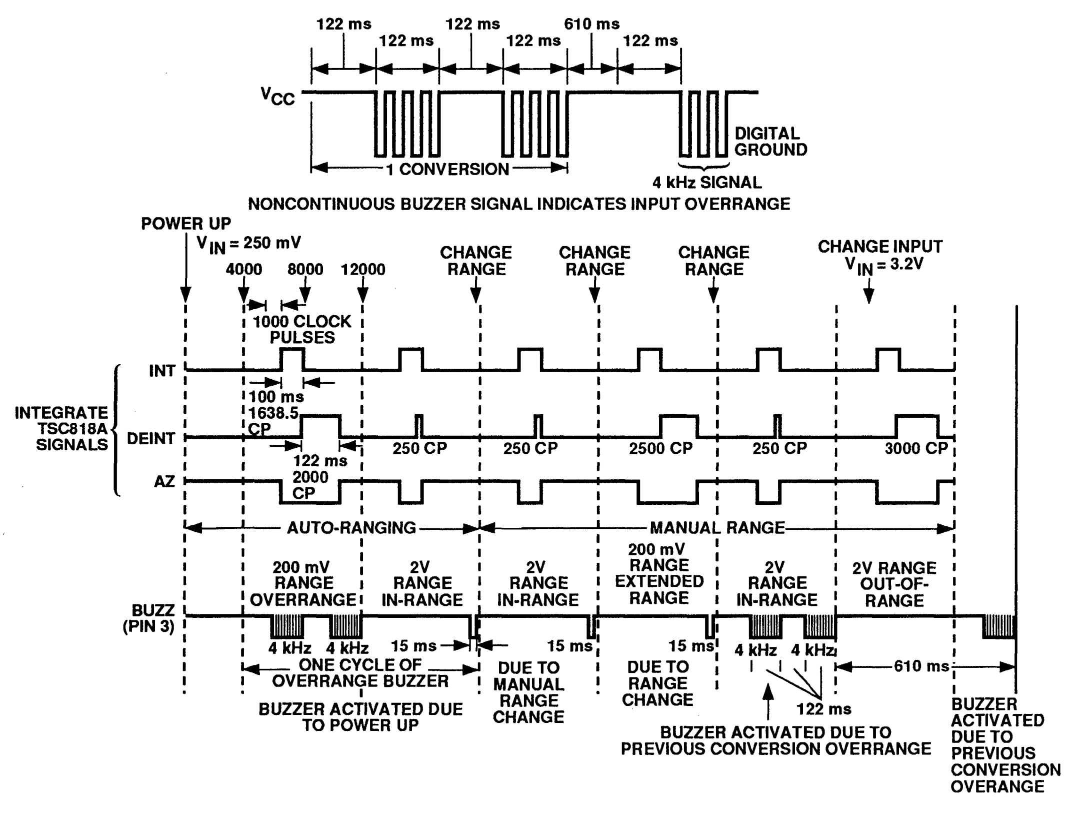


Figure 15 TC818 Timing Waveform for Buzzer Output

Vendors for piezoelectric audio transducers are:

- Gulton Industries
  Piezo Products Division
  212 Durham Avenue
  Metuchen, New Jersey 08840
  (201) 548-2800
  Typical P/Ns: 102-95NS, 101-FB-00
- Taiyo Yuden (USA) Inc.
  Arlington Center
  714 West Algonquin Road
  Arlington Heights, Illinois 60005
  Typical P/Ns: CB27BB, CB20BB, CB355BB

Display Decimal Point Selection

The TC818 provides a decimal point LCD drive signal. The decimal point position is a function of the selected full-scale range, as shown in Table V.

Table V. Decimal Point Selection

	1 *	9 *	9 * 9
Full-Scale Range	**DP3**	**DP2**	**DP1**
2000V, 2000 kΩ	OFF	OFF	OFF
200V, 200 kΩ	OFF	OFF	ON
20V, 20 kΩ	OFF	ON	OFF
2V, 2 kΩ	ON	OFF	OFF
200V, 200Ω	OFF	OFF	ON
200 mV, 200Ω	OFF	OFF	ON
20 mA	OFF	ON	OFF
200 mA	OFF	OFF	ON

AC-to-DC Converter Operational Amplifier

The TC818 contains an on-chip operational amplifier that may be connected as a rectifier for AC-to-DC voltage and current measurements. Typical operational amplifier characteristics are:

- Slew Rate: 1 V/µs
- Unity-Gain Bandwidth: 0.4 MHz
- Open-Loop Gain: 44 dB
- Output Voltage Swing (Load = 10 kΩ) ±1.5V
  (Referenced to Analog Common)

When the AC measurement option is selected, the input buffer receives an input signal through switch S14 rather than switch S11 (see Figure 1). With external circuits, the AC operating mode can be used to perform other types of functions within the constraints of the internal operational amplifier. External circuits that perform true RMS conversion or a peak hold function are typical examples.

Component Selection

Integration Resistor Selection

The TC818 automatically selects one of two external integration resistors. RVIBUF (pin 52) is selected for voltage and current measurement. RWBUF (pin 51) is selected for resistance measurements.

RVIBUF Selection (Pin 52)

In auto-range operation, the TC818 operates with a 200 mV maximum full-scale potential at V_I (pin 42). Resistive dividers at VR2 (pin 39), VR3 (pin 38), VR4 (pin 41), and VR5 (pin 40) are automatically switched to maintain the 200 mV full-scale potential.

In manual mode, the extended operating mode is activated giving a 300 mV full-scale potential at V_I (pin 42).

The integrator output swing should be maximized, but saturations must be avoided. The integrator will swing within 0.45V of V_{CC} (pin 26) and 0.5V of V_{SS} (pin 54) without saturating. A ±2V swing is suggested. The value of RVIBUF is easily calculated, assuming a worst-case extended resolution input signal:

$$\text{RVIBUF} = \frac{V_{MAX}\,(t_I)}{V_{INT}\,(C_I)} \approx 150\ \text{k}\Omega$$

where:

V_{INT} = Integrator swing = ±2V
t_I = Integration time = 100 ms
C_I = Integration capacitor = 0.1 µF
V_{MAX} = Maximum input at V_I = 300 mV

RWBUF Selection (Pin 51)

In ratiometric resistance measurements, the signal at R_X (pin 47) is always positive with respect to analog common. The integrator swings negative.

The worst-case integrator swing is for the 200Ω range with the manual, extended resolution option.

The input voltage, V_X (pin 47) is easily calculated (Figure 16):

$$\text{R}\Omega\text{BUF} = \frac{(V_{CC} - V_{ANCOM})\,R_X}{(R_X + R_S + R_1 + R_S)} = 0.63\text{V}$$

where:

V_{ANCOM} = Potential at analog common ≈ 2.7V
R_S = 220Ω
R_I = 163.85Ω
R_X = 300Ω
R_S = Internal switch 33 resistance ≈ 600Ω

For a 3.1V integrator swing, the value of RΩBUF is easily calculated:

$$R\Omega BUF = \frac{(V_X\ Max)\ (t_I)}{C_I\ (V_{INT})} \approx 220\ k\Omega$$

where:

V_{INT} = Integrator swing = 3.1V
t_I = Integration time = 100 ms
C_I = Integration capacitor = 0.1 μF
R_X Max = 300Ω
V_X Max = 700 mV

With a low battery voltage of 6.6V, analog common will be approximately 3.6V above the negative supply terminal. With the integrator swinging down from analog common toward the negative supply, a 3.1V swing will set the integrator output to 0.5V above the negative supply.

Capacitors — C_{INT}, C_{AZ} and C_{REF}

The integration capacitor, C_{INT}, must have low dielectric absorption. A 0.1 μF polypropylene capacitor is suggested. The auto-zero capacitor, C_{AZ}, and reference capacitor, C_{REF}, should be selected for low leakage and dielectric absorption. Polystyrene capacitors are good choices.

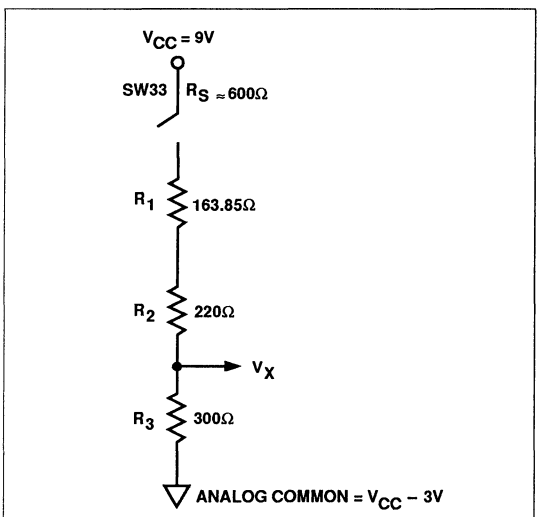


Figure 16 RΩBUF Calculation (200Ω Manual Operation)

Reference Voltage Adjustment

The TC818 contains a low temperature drift internal voltage reference. The analog common potential (pin 27) is established by this reference. Maximum drift is a low 75 ppm/°C. Analog common is designed to be approximately 2.6V below V_{CC} (pin 26). A resistive divider (R18/R19, Functional Diagram) sets the TC818 reference input voltage (REFHI, pin 32) to approximately 163.85 mV.

With an input voltage near full scale on the 200 mV range, R19 is adjusted for the proper reading.

Display Hold Feature

The LCD will not be updated when $\overline{HOLD}$ (pin 57) is connected to GND (pin 55). Conversions are made, but the display is not updated. A $\overline{HOLD}$ mode LCD annunciator is activated when $\overline{HOLD}$ is low.

The LCD $\overline{HOLD}$ annunciator is activated through the triplex LCD driver signal at pin 12.

Flat Package Socket

Sockets suitable for prototype work are available. A USA source is:

- Nepenthe Distribution
  2471 East Bayshore, Suite 520
  Palo Alto, CA 94303
  (415) 856-9332
  TWX: 910-373-2060
  "CBQ" Socket, Part No. IC51-064-042

Resistive Ladder Networks

Resistor attenuator networks for voltage and resistance measurements are available from:

- Caddock Electronics
  1717 Chicago Avenue
  Riverside, CA 92507
  Tel: (714) 788-1700
  TWX: 910-332-6108

Attenuator Accuracy	Attenuator Type	Caddock Part Number
0.1%	Voltage	1776-C441
0.25%	Voltage	1776-C44
0.25%	Resistance	T1794-204-1

NOTES

TELEDYNE COMPONENTS

1

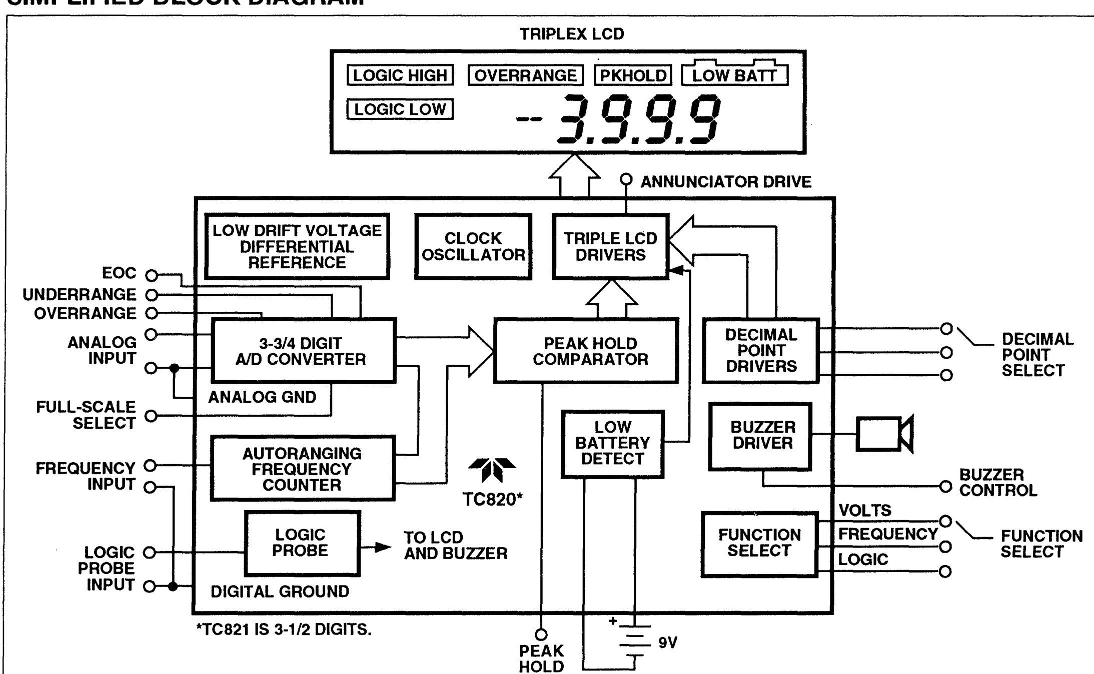
(3-3/4 DIGIT) TC820
(3-1/2 DIGIT) TC821

DISPLAY A/D CONVERTERS WITH FREQUENCY COUNTER AND LOGIC PROBE

FEATURES

- Multiple-Function Measurement System
  - — Analog-to-Digital Converter
  - — Frequency Counter
  - — Logic Probe
- Frequency Counter
  - — Measures Input Frequency to 4 MHz
  - — Auto-Ranging Over Four-Decade Range
- Logic Probe Inputs
  - — Two LCD Annunciators
  - — Buzzer Drive
- Peak Reading Hold With LCD Annunciator
- 3-3/4 Digit (3999 Maximum) Resolution (TC820)
- 3-1/2 Digit (1999 Maximum) Resolution (TC821)
- Low Noise A/D Converter
  - — Differential Inputs, 1 pA Bias Current
  - — Differential Reference for Ratiometric Ohms
  - — On-Chip Voltage Reference, 50 ppm/°C Drift
- No External LCD Drivers Required
  - — Full 3-3/4 Digit Display
  - — Displays "OL" for Input Overrange
  - — Three Decimal Point and Polarity Drivers
  - — LCD Annunciator Drive
  - — Adjustable LCD Drive Voltage
- Low Battery Detect With LCD Annunciator
- On-Chip Buzzer Driver and Control Input
- Control Input Changes Full Scale Range by 10:1
- Data Hold Input
- Underrange and Overrange Outputs
- Multiple Package Options
  - — 40-Pin DIP
  - — 44-Pin Flat Package or PLCC

SIMPLIFIED BLOCK DIAGRAM



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TC820 (3-3/4 DIGIT)
TC821 (3-1/2 DIGIT)

GENERAL DESCRIPTION

The TC820 is a 3-3/4 digit measurement system combining an integrating analog-to-digital converter, frequency counter, and logic level tester in a single 40-pin package. The TC820 supersedes the TC7106 in new designs by improving performance and reducing system cost. The TC820 adds features that are difficult, expensive, or impossible to provide with older A/D converters (see the competitive evaluation). The high level of integration permits TC820-based instruments to deliver higher performance and more features, while actually reducing parts count.

Fabricated in low-power CMOS, the TC820 directly drives a 3-3/4 digit (3999 maximum) LCD. The TC821 includes all features of the TC820, but with a resolution of 3-1/2 digits (1999 maximum).

With a maximum range of 3999 counts, the TC820 provides 10 times greater resolution in the 200 mV to 400 mV range than traditional 3-1/2 digit meters. An auto-zero cycle guarantees a zero reading with a 0V input. CMOS processing reduces analog input bias current to only 1 pA. Rollover error, the difference in readings for equal magnitude but opposite polarity input signals, is less than ±1 count. Differential reference inputs permit ratiometric measurements for ohms or bridge transducer applications.

The TC820's frequency counter option simplifies design of an instrument well-suited to both analog and digital troubleshooting: voltage, current, and resistance measurements, plus precise frequency measurements to 4 MHz (higher frequencies can be measured with an external prescaler), and a simple logic probe. The frequency counter will automatically adjust its range to match the input frequency, over a four-decade range.

Two logic level measurement inputs permit a TC820-based meter to function as a logic probe. When combined with external level shifters, the TC820 will display logic levels on the LCD and also turn on a piezoelectric buzzer when the measured logic level is low.

Other TC 820 features simplify instrument design and reduce parts count. On-chip decimal point drivers are included, as is a low battery detection annunciator. A piezoelectric buzzer can be controlled with an external switch or by the logic probe inputs. Two oscillator options are provided: A crystal can be used if high accuracy frequency measurements are desired, or a simple RC option can be used for low-end instruments.

A "peak reading hold" input allows the TC820 to retain the highest A/D or frequency reading. This feature is useful in measuring motor starting current, maximum temperature, and similar applications.

A family of instruments can be created with the TC821 and TC820. No additional design effort is required to create instruments with 3-1/2 and 3-3/4 digit resolution. The TC821 can also reduce parts count in existing high-end 7106-type designs.

The TC820 and TC821 operate from a single 9V battery, with typical power of 10 mW. Packages include a 40-pin DIP, 44-pin plastic flat package, and 44-pin PLCC.

COMPETITIVE EVALUATION

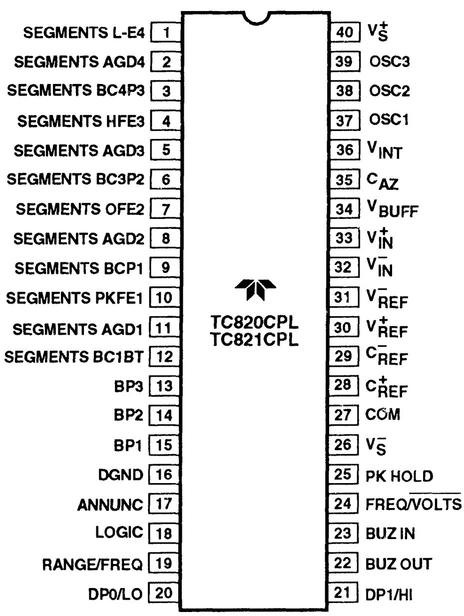
Features	TC820	7106
3-3/4 Digit Resolution	Yes	No
Auto-Ranging Frequency Counter	Yes	No
Logic Probe	Yes	No
Decimal Point Drive	Yes	No
Peak Reading Hold (Frequency or Voltage)	Yes	No
Display Hold	Yes	No
Simple 10:1 Range Change	Yes	No
Buzzer Drive	Yes	No
Low Battery Detection With Annunciator	Yes	No
Overrange Detection With Annunciator	Yes	No
Low Drift Reference	Yes	No
Underrange/Overrange Logic Output	Yes	No
Input Overload Display	"OL"	"1"
LCD Annunciator Driver	Yes	No
LCD Drive Type	Triplexed	Direct
LCD Pin Connections	15	24
LCD Elements	36	23

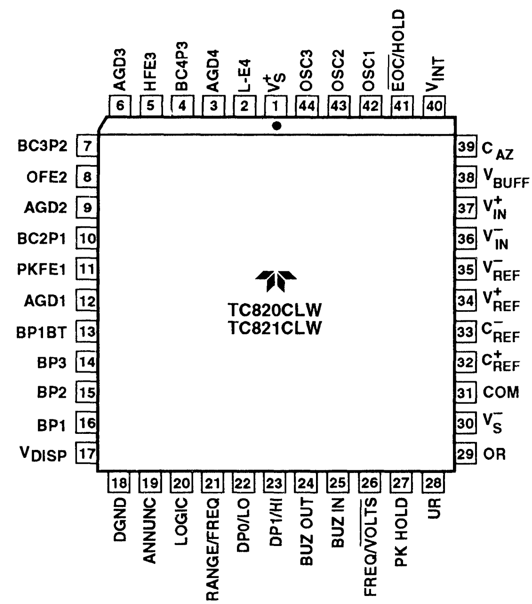
DISPLAY A/D CONVERTERS WITH FREQUENCY COUNTER AND LOGIC PROBE

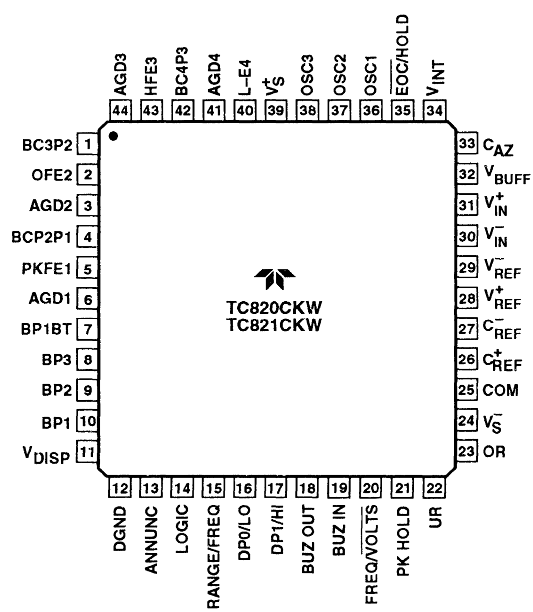
1

TC820 (3-3/4 DIGIT) TC821 (3-1/2 DIGIT)

PIN CONFIGURATIONS







TC820 (3-3/4 DIGIT)
TC821 (3-1/2 DIGIT)

ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage (V_S^+ to GND) 15V
Analog Input Voltage (Either Input) (Note 1) ..... V_S^+ to V_S^-
Reference Input Voltage (Either Input) .... V_S^+ to V_S^-
Digital Inputs .... V_S^+ to DGND
V_{DISP} .... V_S^+ to DGND –0.3V
Power Dissipation, Plastic Package (Note 2) .... 800 mW
Operating Temperature Range
"C" Devices .... 0°C to +70°C
"E" Devices .... –40°C to +85°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

Static-sensitive devices. Unused devices should be stored in conductive material to protect against static discharge and static fields

NOTES:
1. Input voltages may exceed the supply voltages provided that input current is limited to ±100 µA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.
3. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 9V, T_A = 25°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
	Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV (V_{FS} = 200 mV for TC821)	–000	±000	+000	Digital Reading
RE	Roll-Over Error	V_{IN} = ±390 mV Full-Scale = 400 mV (V_{IN} = ±190 mV, V_{FS} = 200 mV for TC821)	–1	±0.2	+1	Counts
NL	Nonlinearity (Maximum Deviation From Best Straight Line Fit)	Full-Scale = 400 mV (V_{FS} = 200 mV for TC821)	–1	±0.2	+1	Count
	Ratiometric Reading	V_{IN} = V_{REF}, TC820 V_{IN} = V_{REF}, TC821	1999 999	1999/2000 999/1000	2000 1000	Digital Reading
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 400 mV (V_{FS} = 200 mV for TC820)	—	50	—	µV/V
VCMR	Common-Mode Voltage Range	Input High, Input Low	V_S^-+1.5	—	V_S^+–1	V
e_N	Noise (P-P Value Not Exceeded 95% of Time)	V_{IN} = 0V Full-Scale = 400 mV (V_{FS} = 200 mV for TC820)	—	15	—	µV
I_{IN}	Input Leakage Current	V_{IN} = 0V T_A = 25°C 0°C ≤ T_A ≤ +70°C –40°C ≤ T_A ≤ +85°C	 — — —	 1 20 100	 10 — —	 pA
V_{COM}	Analog Common Voltage	25 kΩ Between Common and V_S^+ (V_S^+ – V_{COM})	3.15	3.3	3.45	V
V_{CTC}	Common Voltage Temperature Coefficient	25 kΩ Between Common and V_S^+ 0°C ≤ T_A ≤ +70°C –40°C ≤ T_A ≤ +85°C	 — —	 35 50	 50 —	ppm/°C
TC_{ZS}	Zero Reading Drift	V_{IN} = 0V 0°C ≤ T_A ≤ +70°C –40°C ≤ T_A ≤ +85°C	—	0.2 1	—	µV/°C
TC_{FS}	Scale Factor Temperature Coefficient	V_{IN} = 399 mV (V_{IN} = 199 mV for TC821) 0°C ≤ T_A ≤ +70°C –40°C ≤ T_A ≤ +85°C Ext Ref = 0 ppm/°C	 — —	 1 5	 5 —	ppm/°C

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_S	Supply Current	V_{IN} = 0V	—	1	1.5	mA
	Peak-to-Peak Backplane Drive Voltage	V_S = 9V V_{DISP} = DGND	4.5	4.7	5.3	V
	Buzzer Frequency	f_{OSC} = 40 kHz	—	5	—	kHz
	Counter Timebase Period	f_{OSC} = 40 kHz	—	1	—	Second
	Low Battery Flag Voltage	V_S^+ to V_S^-	6.7	7	7.3	V
V_{IL}	Input Low Voltage		—	—	DGND+1.5	V
V_{IH}	Input High Voltage		V_S^+–1.5	—	—	V
V_{OL}	Output Low Voltage, UR, OR Outputs	I_L = 50 µA	—	—	DGND+0.4	V
V_{OL}	Output High Voltage, UR, OR Outputs	I_L = 50 µA	V_S^+–1.5	—	—	V
	Control Pin Pull-Down Current	$V_{IN} = V_S^+$	—	5	—	µA

PIN DESCRIPTION

Pin No. (40-Pin Packagel)	Pin No. (44-Pin Flat Package)	Symbol	Description
1	40	L-E4	LCD segment driver for L ("logic low"), polarity, and "e" segment of most significant digit (MSD).
2	41	AGD4	LCD segment drive for "a," "g," and "d" segments of MSD.
3	42	BC4P3	LCD segment drive for "b" and "c" segments of MSD and decimal point 3.
4	43	HFE3	LCD segment drive for H ("logic high"), and "f" and "e" segments of third LSD.
5	44	AGD3	LCD segment drive for "a," "g," and "d" segments of third LSD.
6	1	BC3P2	LCD segment drive for "b" and "c" segments of third LSD and decimal point 2.
7	2	OFE2	LCD segment drive for "overrange," and "f" and "e" segments of second LSD.
8	3	AGD2	LCD segment drive for "a," "g," and "d" segments of second LSD.
9	4	BC2P1	LCD segment drive for "b " and "c" segments of second LSD and decimal point 1.
10	5	PKFE1	LCD segment drive for "hold peak reading," and "f" and "e" segments of LSD.
11	6	AGD1	LCD segment drive for "a," "g," and "d" segments of LSD.
12	7	BC1BT	LCD segment drive for "b" and "c" segments of LSD and "low battery."
13	8	BP3	LCD backplane #3.
14	9	BP2	LCD backplane #2.
15	10	BP1	LCD backplane #1.
—	11	V_{DISP}	Sets peak LCD drive signal: $V_{PEAK} = (V_S^+) - V_{DISP}$. V_{DISP} may also be used to compensate for temperature variation of LCD crystal threshold voltage.
16	12	DGND	Internal logic digital ground, the logic "0" level. Nominally 4.7V below V_S^+.
17	13	ANNUNC	Square-wave output at the backplane frequency, synchronized to BP1. ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off.

PIN DESCRIPTION (Cont.)

Pin No. (40-Pin Packagel)	Pin No. (44-Pin Flat Package)	Symbol	Description
18	14	LOGIC	Logic mode control input. When connected to V_S^+, the converter is in logic mode. The LCD displays "OL" and the decimal point inputs control the "high" and "low" annunciators. When the "low" annunciator is on, the buzzer will also be on. When unconnected or connected to DGND, the TC820 is in the voltage/frequency measurement mode. This pin has a 5 µA internal pull-down to DGND.
19	15	RANGE/ FREQ	Dual-purpose input. In range mode, when connected to V_S^+, the integration time will be 200 counts instead of 2000 counts (100 instead of 1000 counts for TC821), and the LCD will display the analog input divided by 10. (See text for limitation with TC820.) In frequency mode, this pin is the frequency input. A digital signal applied to this pin will be measured with a 1-second time base. There is an internal 5 µA pull-down to DGND.
20	16	DP0/LO	Dual-purpose input. Decimal point select input for voltage measurements. In logic mode, connecting this pin to V_S^+ will turn on the "low" LCD segment. There is an internal 5 µA pull-down to DGND in volts mode only. Decimal point logic: DP1 DP0 Decimal Point Selected 0 0 None 0 1 DP1 1 0 DP2 1 1 DP3
21	17	DP1/HI	Dual-purpose input. Decimal point select input for voltage measurements. In logic mode, connecting this pin to V_S^+ will turn on the "high" LCD segment. There is an internal 5 µA pull-down to DGND in volts mode only.
22	18	BUZOUT	Buzzer output. Audio frequency, 5 kHz, output which drives a piezoelectric buzzer.
23	19	BUZIN	Buzzer control input. Connecting BUZIN to V_S^+ turns the buzzer on. BUZIN is logically ORed (internally) with the "logic level low" input. There is an internal 5 µA pull-down to DGND.
24	20	FREQ/ $\overline{\text{VOLTS}}$	Voltage or frequency measurement select input. When unconnected, or connected to DGND, the A/D converter function is active. When connected to V_S^+, the frequency counter function is active. This pin has an internal 5 µA pull-down to DGND.
25	21	PKHOLD	Peak hold input. When connected to V_S^+, the converter will only update the display if a new conversion value is greater than the preceding value. Thus, the peak reading will be stored and held indefinitely. When unconnected, or connected to DGND, the converter will operate normally. This pin has an internal 5 µA pull-down to DGND.
	22	UR	Underrange output. This output will be high when the digital reading is 380 counts or less (≤180 counts for TC821).
	23	OR	Overrange output. This output will be high when the analog signal input is greater than full scale. The LCD will display "OL" when the input is overranged.
26	24	V_S^-	Negative supply connection. Connect to negative terminal of 9V battery.
27	25	COM	Analog circuit ground reference point. Nominally 3.3V below V_S^+.
28	26	C_{REF}^+	Positive connection for reference capacitor.
29	27	C_{REF}^-	Negative connection for reference capacitor.
30	28	V_{REF}^+	High differential reference input connection.
31	29	V_{REF}^-	Low differential reference input connection.
32	30	V_{IN}^-	Low analog input signal connection.

PIN DESCRIPTION (Cont.)

Pin No. (40-Pin Packagel)	Pin No. (44-Pin Flat Package)	Symbol	Description
33	31	V_{IN}^+	High analog input signal connection.
34	32	V_{BUFF}	Buffer output. Connect to integration resistor.
35	33	C_{AZ}	Auto-zero capacitor connection.
36	34	V_{INT}	Integrator output. Connect to integration capacitor.
	35	$\overline{EOC}$/ HOLD	Bidirectional pin. Pulses low (i.e., from V_S^+ to DGND) at the end of each conversion. If connected to V_S^+, conversions will continue, but the display is not updated.
37	36	OSC1	Crystal oscillator (input) connection.
38	37	OSC2	Crystal oscillator (output) connection.
39	38	OSC3	RC oscillator connection.
40	39	V_S^+	Positive power supply connection, typically 9V.

ORDERING INFORMATION

Surface-Mount Devices

Part No.	Resolution	Package	Temperature Range
TC820CKW	3-3/4 Digits	44-Pin Plastic Flat Package	0°C to +70°C
TC820CLW	3-3/4 Digits	44-Pin Plastic Leaded Chip Carrier (PLCC)	0°C to +70°C
TC820EKW	3-3/4 Digits	44-Pin Plastic Flat Package	−40°C to +85°C
TC820ELW	3-3/4 Digits	44-Pin Plastic Leaded Chip Carrier (PLCC)	−40°C to +85°C
TC821CKW	3-1/2 Digits	44-Pin Plastic Flat Package	0°C to +70°C
TC821CLW	3-1/2 Digits	44-Pin Plastic Leaded Chip Carrier (PLCC)	0°C to +70°C
TC821EKW	3-1/2 Digits	44-Pin Plastic Flat Package	−40°C to +85°C
TC821ELW	3-1/2 Digits	44-Pin Plastic Leaded Chip Carrier (PLCC)	−40°C to +85°C

40-Pin DIPs

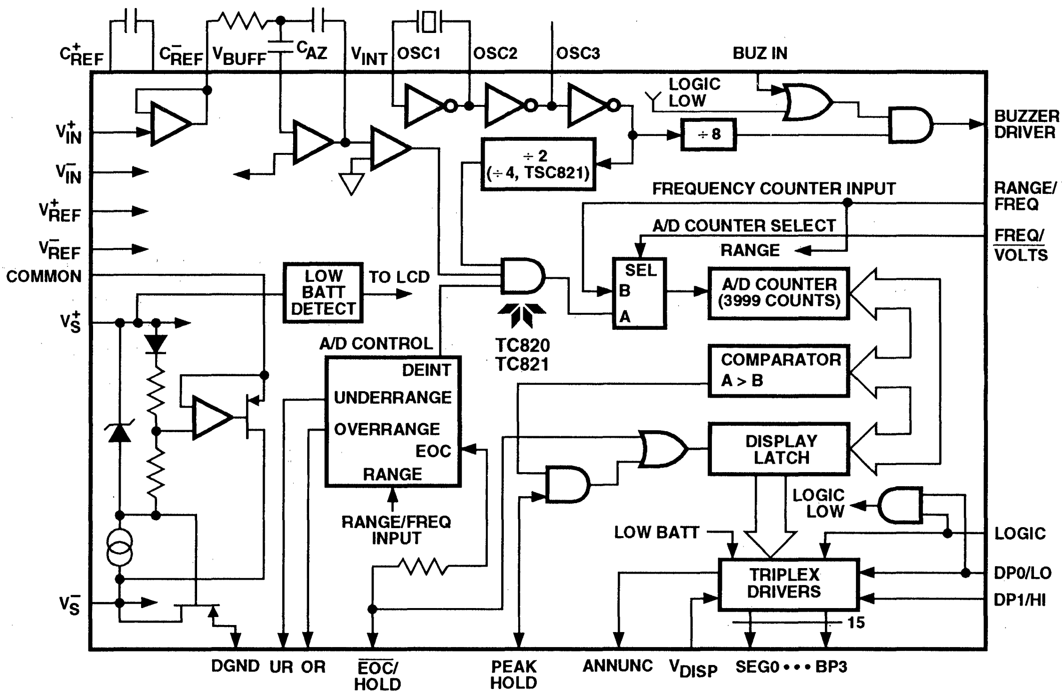
Part No.	Resolution	Temperature Range
TC820CPL	3-3/4 Digits	0°C to +70°C
TC820EPL	3-3/4 Digits	−40°C to +85°C
TC821CPL	3-1/2 Digits	0°C to +70°C
TC821EPL	3-1/2 Digits	−40°C to +85°C

TC820/TC821 Comparison

	Device	
Feature	TC820	TC821
Resolution	3-3/4 Digits	3-1/2 Digits
All Other Features (Counter, Logic, etc.)	Yes	Yes

TC820 (3-3/4 DIGIT)
TC821 (3-1/2 DIGIT)

FUNCTIONAL DIAGRAM



DISPLAY A/D CONVERTERS WITH FREQUENCY COUNTER AND LOGIC PROBE

TC820 (3-3/4 DIGIT)
TC821 (3-1/2 DIGIT)

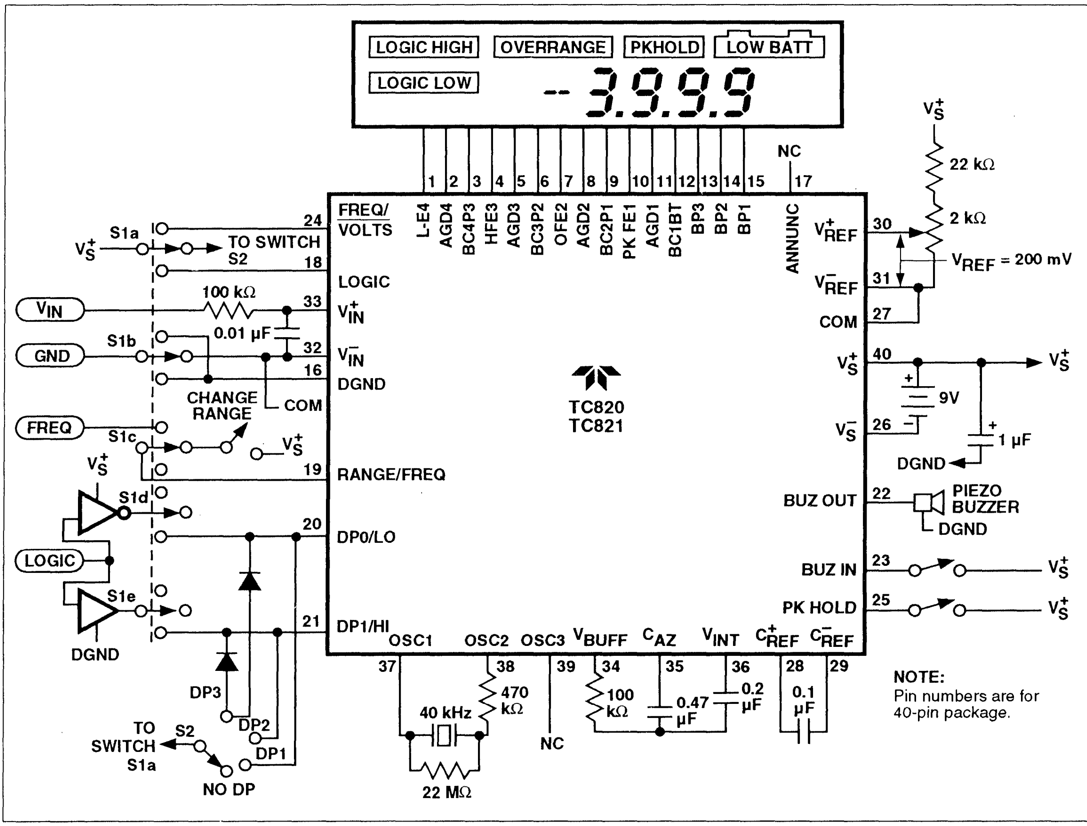


Figure 1. Typical Operating Circuit

FEATURES

The TC820 and TC821 combine the features of an analog-to-digital converter (ADC), frequency counter, and logic probe, in a single CMOS-integrated circuit. All of the TC820 features are shown graphically in the functional diagram. With on-chip voltage reference and LCD drive circuitry, the TC820 simplifies the design of multi-mode measurement instruments.

The TC820 has a resolution of 3-3/4 digits (3999 maximum), while the TC821 has a resolution of 3-1/2 digits (1999 maximum). The features of both converters are the same, so that both 3-3/4 digit and 3-1/2 digit designs can be produced with only one PC board design. The differences between the TC820 and the TC821 primarily affect system timing, and are noted in the appropriate sections of the data sheet.

GENERAL THEORY OF OPERATION

Dual-Slope conversion Principles

The TC820 analog-to-digital converter operates on the principle of dual-slope integration. An understanding of the dual-slope conversion technique will aid the user in following the detailed TC820 theory of operation following this section. A conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input Signal Integration
(2) Reference Voltage Integration (Deintegration)

Referring to Figure 2, the unknown input signal to be converted is integrated from zero for a fixed time period (t_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated

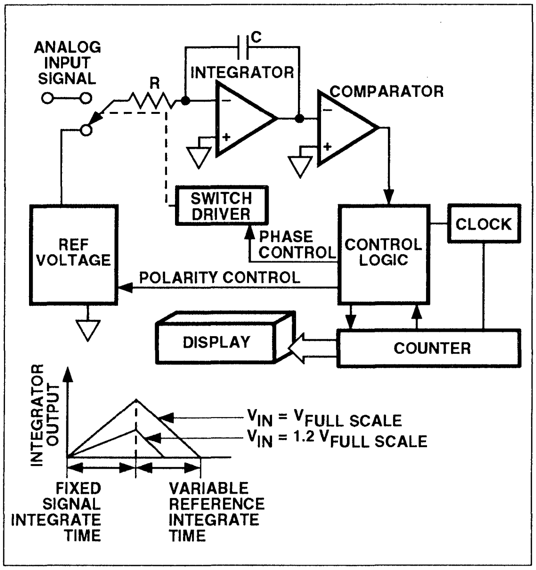


Figure 2. Basic Dual-Slope Converter

until the integrator output voltage returns to zero. The reference integration (deintegration) time (T_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" from zero and "ramp-down" back to zero. A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{R_{INT}\,C_{INT}} \int_0^{t_{INT}} V_{IN}\,(t)\,dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where: V_{REF} = Reference voltage
t_{INT} = Integration time
t_{DEINT} = Deintegration time

For a constant t_{INT}:

$$V_{IN} = V_{REF} \times \frac{t_{DEINT}}{t_{INT}}$$

Accuracy in a dual-slope converter is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit of the dual-slope technique is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods, making integrating ADCs immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated (Figure 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period.

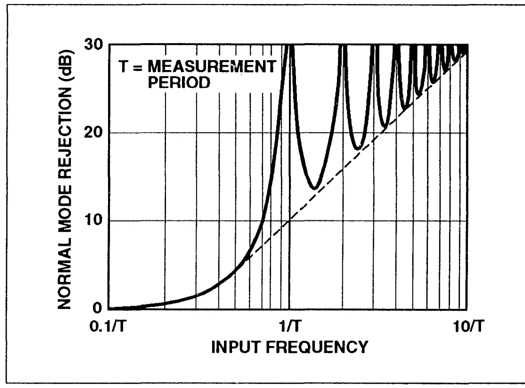


Figure 3. Normal-Mode Rejection of Dual-Slope Converter

TSC820 THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual-slope phases discussed above, the TC820 design incorporates a "zero integrator output" phase and an "auto-zero" phase. These additional phases ensure that the integrator starts at 0V (even after a severe overrange conversion), and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Zero Integrator Output
(2) Auto-Zero
(3) Signal Integrate
(4) Reference Deintegrate

Zero Integrator Output Phase

This phase guarantees that the integrator output is at 0V before the system zero phase is entered, ensuring that the true system offset voltages will be compensated for even after an overrange conversion. The duration of this phase is 500 counts plus the unused deintegrate counts, for both the TC820 and TC821.

Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the measurement circuit by opening internal analog switches, and the internal nodes are shorted to Analog Common (0V ref) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The auto-zero phase residual is typically 10 µV to 15 µV. The auto-zero duration is 1500 counts (750 counts for TC821).

Signal Integration Phase

Upon completion of the auto-zero phase, the auto-zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is then integrated for a fixed time period, which is 2000 counts (4000 clock periods) in the TC820, and 1000 counts (4000 clock periods) in the TC821. The externally-set clock frequency is divided by two (TC820) or four (TC821) before clocking the internal counters. The integration time period is:

$$t_{INT} = \frac{4000}{f_{OSC}}$$

Note that for the same clock frequency, the TC820 and TC821 have the same signal integration time. Therefore, the noise rejection performance of the two converters will be the same.

The differential input voltage must be within the device's common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, as in battery-powered applications, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integration phase. The sign bit is a "true polarity" indication in that signals less than 1 LSB are correctly determined. This allows precision null detection that is limited only by device noise and auto-zero residual offsets.

Reference Integrate (Deintegrate) Phase

The reference capacitor, which was charged during the auto-zero phase, is connected to the input of the integrating amplifier. The internal sign logic ensures the polarity of the reference voltage is always connected in the phase opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate determined by the reference potential.

The amount of time required (T_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration phase:

$$t_{DEINT} = \frac{R_{INT}\, C_{INT}\, V_{INT}}{V_{REF}}$$

The digital reading displayed by the TC820 is:

$$\text{Digital Count} = 2000\ \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

For the TC821, the digital reading displayed is:

$$\text{Digital Count} = 1000\ \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

System Timing

The oscillator frequency is divided by 2 (4 for TC821) prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 8000 (4000) counts or 16000 (16000) clock pulses. The 8000 (4000) count phase is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

Conversion Phase	TC820	TC821	Units
1) Auto-Zero:	1500	500	Counts
2) Signal Integrate:[1,2]	2000	1000	Counts
3) Reference Integrate:	1 to 4001	1 to 2001	Counts
4) Integrator Output Zero:	499 to 4499	499 to 2499	Counts

NOTES: 1. This time period is fixed. The integration period for the TC820 is:

$$t_{INT\ (TC820)} = \frac{4000}{f_{OSC}} = 2000\ \text{counts}$$

For the TC821, the integration period is:

$$t_{INT\ (TC821)} = \frac{4000}{f_{OSC}} = 1000\ \text{counts}$$

where f_{OSC} is the clock oscillator frequency.

2. Times shown are the RANGE/FREQ at logic low (normal operation). When RANGE/FREQ is logic high, signal integrate times are 200 counts for TC820 and 100 counts for TC821. See "10:1 Range Change" section.

Input Overrange

When the analog input is greater than full scale, the LCD will display "OL" and the "OVERRANGE" LCD annunciator will be on.

Peak Reading Hold

The TC820 provides the capability of holding the highest (or peak) reading. Connecting the PK HOLD input to V_S^+ enables the peak hold feature. At the end of each conversion the contents of the TC820 counter is compared to the contents of the display register. If the new reading is higher than the reading being displayed, the higher reading is transferred to the display register. A "higher" reading is defined as the reading with the higher absolute value.

The peak reading is held in the display register so the reading will not "droop" or slowly decay with time. The held reading will be retained until a higher reading occurs, the PK HOLD input is disconnected from V_S^+, or power is removed.

The peak signal to be measured must be present during the TC820 signal integrate period. The TC820 does not perform transient peak detection of the analog input signal. However, in many cases, such as measuring temperature or electric motor starting current, the TC820 "acquisition time" will not be a limitation. If true peak detection is required, a simple circuit will suffice. See the applications section for details.

The peak reading function is also available when the TC820 is in the frequency counter mode. The counter autoranging feature is disabled when peak reading hold is selected.

10:1 Range Change

The analog input full-scale range can be changed with the RANGE/FREQ input. Normally, RANGE/FREQ is held low by an internal pulldown. Connecting this pin to V_S^+ will increase the full-scale voltage by a factor of 10. No external component changes are required.

The RANGE/FREQ input operates by changing the integrate period. When RANGE/FREQ is connected to V_S^+, the signal integration phase of the conversion is reduced by a factor of 10 (i.e., from 2000 counts to 200 counts).

For the TC821 (3-1/2 digit) ADC, the RANGE/FREQ input can be used to select between 200 mV and 2V full scale. For the TC820, however, the 10:1 range change will result in ±4V full scale. This full-scale range will exceed the common-mode range of the input buffer when operating from a 9V battery. If range changing is required for the TC820, a higher supply voltage can be provided or the input voltage can be divided by 2 externally.

Frequency Counter

In addition to serving as an analog-to-digital converter, the TC820 internal counter can also function as a frequency counter (Figure 4). In the counter mode, pulses at the RANGE/FREQ input will be counted and displayed.

The frequency counter derives its time base from the clock oscillator. The counter time base is:

$$t_{COUNT} = \frac{f_{OSC}}{40{,}000}$$

Thus, the counter will operate with a 1-second time base when a 40 kHz oscillator is used. The frequency counter accuracy is determined by the oscillator accuracy. For accurate frequency measurements, a crystal oscillator is recommended.

The frequency counter will automatically select the proper range. Auto-range operation extends over four decades, from 3.999 kHz to 3.999 MHz (1.999 kHz to 1.999 MHz for TC821). Decimal points are set automatically in the frequency mode (Figure 5).

The logic switching levels of the RANGE/FREQ input are CMOS levels. For best counter operation, an external buffer is recommended. See the applications section for details.

Logic Probe

The TC820 can also function as a simple logic probe (Figure 6). This mode is selected when the LOGIC input is high. Two dual-purpose pins, which normally control the decimal points, are used as logic inputs. Connecting either input to a logic high level will turn on the corresponding LCD annunciator. When the "low" annunciator is on the buzzer will be on. As with the frequency counter input, external level shifters/buffers are recommended for the logic probe inputs.

When the logic probe function is selected while FREQ/$\overline{\text{VOLTS}}$ is low (A/D mode), the ADC will remain in the auto-zero mode. The LCD will read "OL" and all decimal points will be off (Figure 7).

If the logic probe is active while FREQ/$\overline{\text{VOLTS}}$ is high (counter mode), the frequency counter will continue to operate. The display will read "OL" but the decimal points will be visible. If the logic probe input is also connected to the RANGE/FREQ input, bringing the LOGIC input low will immediately display the frequency at the logic probe input.

Analog Pin Functional Description

Differential Signal Inputs (V_{IN}^+), (V_{IN}^-)

The TC820 is designed with true differential inputs, and accepts input signals within the input stage common-mode voltage (V_{CM}) range. The typical range is V_S^+ –1V to V_S^- +1.5V. Common-mode voltages are removed from the system when the TC820 operates from a battery or floating power source (isolated from measured system) and V_S^- is connected to analog common. (See Figure 8.)

DISPLAY A/D CONVERTERS WITH FREQUENCY COUNTER AND LOGIC PROBE

TC820 (3-3/4 DIGIT)
TC821 (3-1/2 DIGIT)

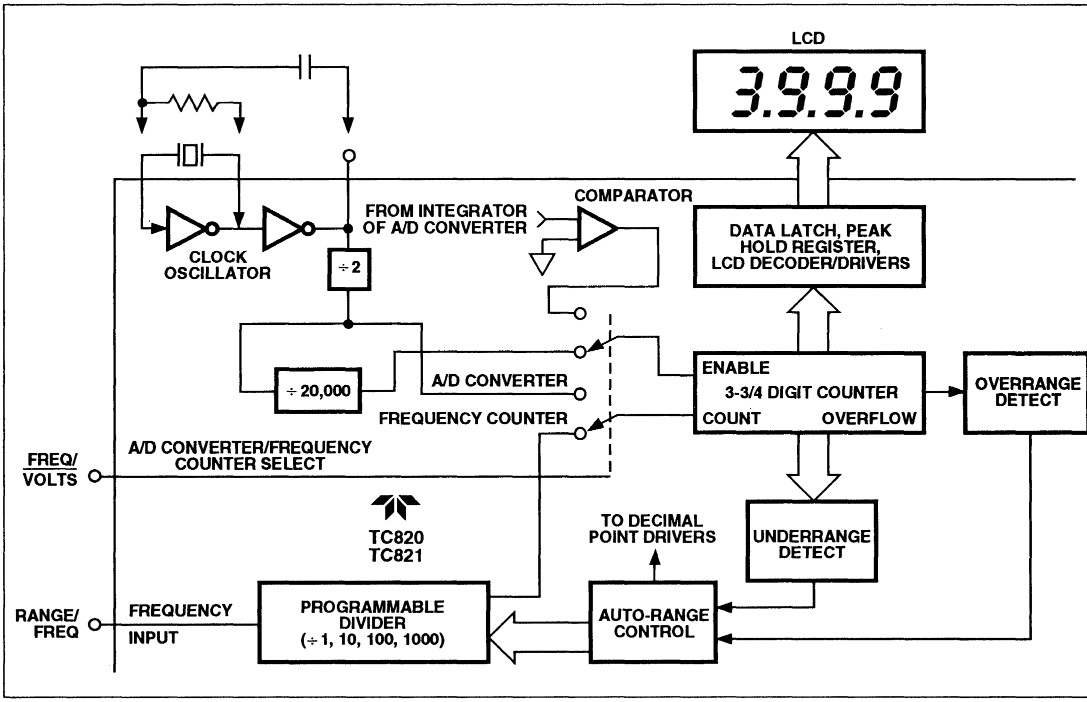


Figure 4. TC820 Counter Operation

3.9.9.9	
DP3 DP2 DP1	
f_{IN}	DECIMAL POINT
0 Hz – 3999 Hz	DP3
4 kHz – 39.99 kHz	DP2
40 kHz – 399.9 kHz	DP1
≥ 400 kHz	NONE

Figure 5. TC820 Auto-Range Decimal Point Selection vs Frequency Counter Input

In systems where common-mode voltages exist, the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large, positive V_{CM} exists in conjunction with a full-scale, negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 9). For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V_S^+ or V_S^- without increased linearity error.

Reference (V_S^+, V_S^-)

The TC820 reference, like the analog signal input, has true differential inputs. In addition, the reference voltage can be generated anywhere within the power supply voltage of the converter. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors, such as load cells and temperature sensors.

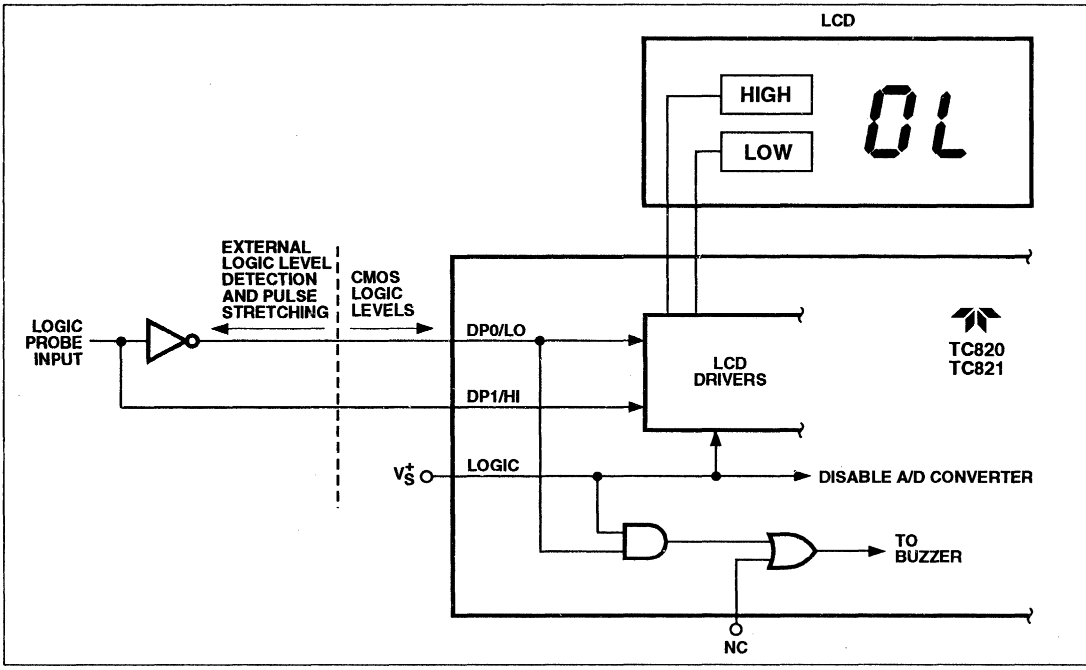


Figure 6. Logic Probe Simplified Schematic

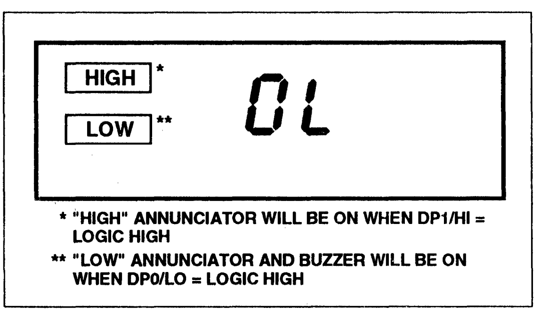


Figure 7. LCD During Logic Probe Operation

To prevent roll-over-type errors from being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance. A 0.1 µF capacitor is typical.

The TC820 offers a significantly improved analog common temperature coefficient, providing a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is typically 35 ppm/°C.

Analog Common

The analog common pin is set at a voltage potential approximately 3.3V below V_S^+. This potential is guaranteed to be between 3.15V and 3.45V below V_S^+. Analog common is tied internally to an N-channel FET capable of sinking 3 mA. This FET will hold the common line at 3.3V below V_S^+ should be an external load attempt to pull the common line toward V_S^+. Analog common source current is limited to 12 µA, and is therefore easily pulled to a more negative voltage (i.e., below V_S^+ –3.3V).

The TC820 connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero cycle. During the reference integrate phase, V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converter's 86 dB common-mode rejection ratio. In battery-powered applications, analog common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference or common point. The TC820 is specifically designed to operate from a battery or in any measurement

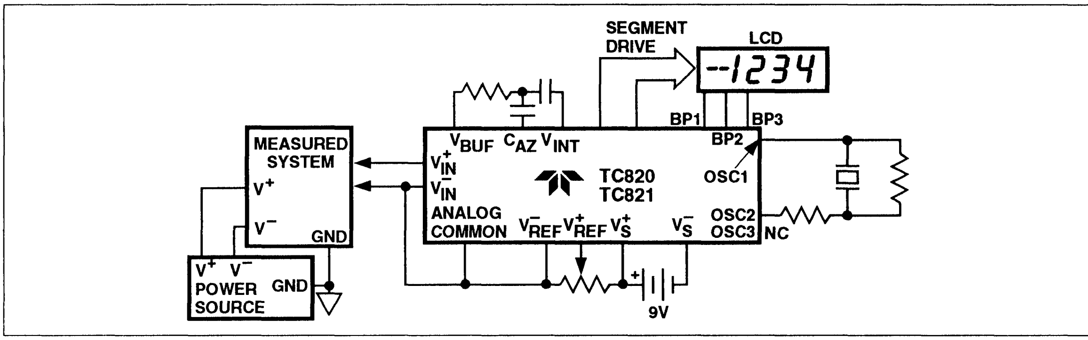


Figure 8. Common-Mode Voltage Removed in Battery Operation With V_{IN}^- = Analog Common

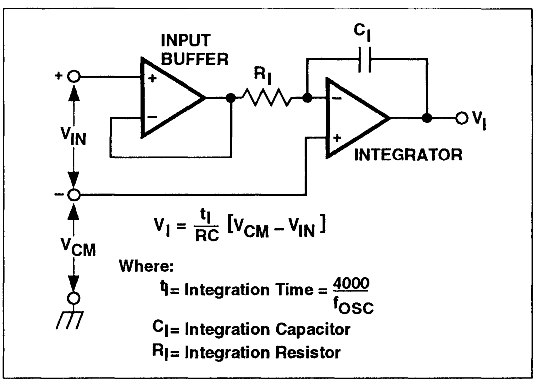


Figure 9. Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)

system where input signals are not referenced (float) with respect to the TC820 power source. The analog common potential of V_S^+ –3.3V gives a 7V end-of-battery-life voltage. The analog common potential has a voltage coefficient of 0.001%/%.

With a sufficiently high total supply voltage ($V_S^+ - V_S^-$ > 7V), analog common is a very stable potential with excellent temperature stability (typically 35 ppm/°C). This potential can be used to generate the TC820 reference voltage. An external voltage reference will be unnecessary in most cases, because of the 35 ppm/°C temperature coefficient. See the applications section for details.

Function Control Input Pin Functional Description

The TC820 operating modes are selected with the function control inputs. The control input truth table is shown in Table I. The high logic threshold is ≥V_S^+ –1.5V and the low logic level is ≤DGND +1.5V.

Table I. TC820 Control Input Truth Table

Logic Input			
FREQ/$\overline{\text{VOLTS}}$	RANGE/FREQ	LOGIC	TC820/821 Function
X	X	1	Logic Probe
0	0	0	A/D Converter, $V_{FULL\ SCALE} = 2 \times V_{REF}$
0	1	0	A/D Converter, $V_{FULL\ SCALE} = 20 \times V_{REF}$
1	Frequency Counter Input	0	Frequency Counter

NOTES: 1. Logic "0" = DGND
2. Logic "1" = V_S^+

FREQ/$\overline{\text{VOLTS}}$

This input determines whether the TC820 is in the analog-to-digital conversion mode or in the frequency counter mode. When FREQ/$\overline{\text{VOLTS}}$ is connected to V_S^+, the TC820 will measure frequency at the RANGE/FREQ input. When unconnected, or connected to DGND, the TC820 will operate as an analog-to-digital converter. This input has an internal 5 µA pull-down to DGND.

LOGIC

The LOGIC input is used to activate the logic probe function. When connected to V_S^+, the TC820 will enter the logic probe mode. The LCD will show "OL" and all decimal points will be off. The decimal point inputs directly control "high" and "low" display annunciators. When LOGIC is unconnected, or connected to DGND, the TC820 will perform analog-to-digital or frequency measurements as selected by the FREQ/$\overline{\text{VOLTS}}$ input. The LOGIC input has an internal 5 µA pull-down to DGND.

RANGE/FREQ

The function of this dual-purpose pin is determined by the FREQ/$\overline{\text{VOLTS}}$ input. When FREQ/$\overline{\text{VOLTS}}$ is connected to V_S^+, RANGE/FREQ is the input for the frequency counter function. Pulses at this input are counted with a time base equal to $f_{OSC}/40{,}000$. Since this input has CMOS input levels (V_S^+ −1.5V and DGND +1.5V), an external buffer is recommended.

When the TC820 analog-to-digital converter function is selected, connecting RANGE/FREQ to V_S^+ will divide the integration time by 10. Therefore, the RANGE/FREQ input can be used to perform a 10:1 range change without changing external components.

DP0/LO, DP1/HI

The function of these dual-purpose pins is determined by the LOGIC input. When the TC820 is in the analog-to-digital converter mode, these inputs control the LCD decimal points. The decimal point truth table is shown in Table II. These inputs have internal 5 μA pull-downs to DGND when the voltage/frequency measurement mode is active.

Table II. TC820 Decimal Point Truth Table

Decimal Point Inputs		
DP1	DP0	LCD
0	0	3999
0	1	399.9
1	0	39.99
1	1	3.999

Connecting the LOGIC input to V_S^+ places the TC820 in the logic probe mode. In this mode, the DP0/LO and DP1/HI inputs control the LCD "low" and "high" annunciators directly. When DP1/HI is connected to V_S^+, the "high" annunciator will turn on. When DP0/LO is connected to V_S^+, the "low" annunciator and the buzzer will turn on. The internal pull-downs on these pins are disabled when the logic probe function is selected.

These inputs have CMOS logic switching thresholds. For optimum performance as a logic probe, external level shifters are recommended. See the applications section for details.

BUZ IN

This input controls the TC820 on-chip buzzer driver. Connecting BUZ IN to V_S^+ will turn the buzzer on. There is an external pull-down to DGND. BUZ IN can be used with external circuitry to provide additional functions, such as a fast, audible continuity indication.

Additional Features

The TC820 and TC821 are available in 40-pin and 44-pin packages. Several additional features are available in the 44-pin package.

$\overline{\text{EOC}}$/HOLD

$\overline{\text{EOC}}$/HOLD is a dual-purpose, bidirectional pin. As an output, this pin goes low for 10 clock cycles at the end of each conversion. This pulse latches the conversion data into the display driver section of the TC820.

$\overline{\text{EOC}}$/HOLD can be used to hold (or "freeze") the display. Connecting this pin to V_S^+ inhibits the display update process. Conversions will continue, but the display will not change. $\overline{\text{EOC}}$/HOLD will hold the display reading for either analog-to-digital or frequency measurements.

The input/output structure of the $\overline{\text{EOC}}$/HOLD pin is shown in Figure 10. The output drive current is only a few microamps, so $\overline{\text{EOC}}$/HOLD can easily be overdriven by an open-collector logic gate, as well as a FET, bipolar transistor, or mechanical switch. When used as an output, $\overline{\text{EOC}}$/HOLD will have a slow rise and fall time due to the limited output current drive. A CMOS Schmitt trigger buffer is recommended.

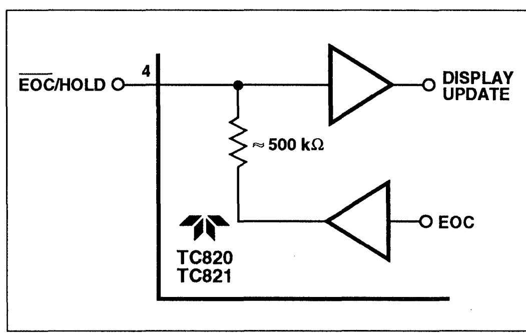


Figure 10. $\overline{\text{EOC}}$/HOLD Pin Schematic

Overrange (OR), Underrange (UR)

The OR output will be high when the analog input signal is greater than full scale (3999 counts for TC820 and 1999 counts for TC821). The UR output will be high when the display reading is 380 counts or less (≤180 counts for TC821).

The OR and UR outputs can be used to provide an auto-ranging meter function. By logically ANDing these outputs with the inverted $\overline{\text{EOC}}$/HOLD output, a single pulse will be generated each time an underranged or overranged conversion occurs (Figure 11).

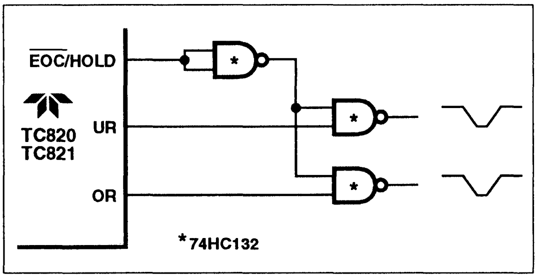


Figure 11. Generating Underrange and Overrange Pulses

V_{DISP}

The V_{DISP} input sets the peak-to-peak LCD drive voltage. In the 40-pin package, V_{DISP} is connected internally to DGND, providing a typical LCD drive voltage of 5 V_{P-P}. The 44-pin package includes a separate V_{DISP} input for applications requiring a variable or temperature-compensated LCD drive voltage. See the applications information for suggested circuits.

APPLICATIONS INFORMATION

Power Supplies

The TC820 is designed to operate from a single power supply such as a 9V battery (Figure 12). The converter will operate over a range of 7V to 15V. For battery operation, analog common (COM) provides a common-mode bias voltage (see analog common discussion in the theory of operation section). However, measurements cannot be referenced to battery ground. To do so will exceed the negative common-mode voltage limit.

A battery with voltage between 3.5V and 7V can be used to power the TC820, when used with a voltage doubler, as shown in Figure 13. The voltage doubler uses the TC7660 and two external capacitors. With this configuration measurements can be referenced either to Analog Common or to battery ground.

Digital Ground (DGND)

Digital ground is generated from an internal zener diode (Figure 14). The voltage between V_S^+ and DGND is the internal supply voltage for the digital section of the TC820. DGND will sink a minimum of 3 mA.

DGND establishes the low logic level reference for the TC820 mode select inputs, and for the frequency and logic probe inputs. The DGND pin can be used as the negative supply for external logic gates, such as the logic probe buffers. To ensure correct counter operation at high frequency, connect a 1 µF capacitor from DGND to V_S^+.

DGND also provides the drive voltage for the LCD. The TC820 40-pin package internally connects the LCD V_{DISP} pin to DGND, and provides an LCD drive voltage of about 5 V_{P-P}. In the 44-pin package, connecting the V_{DISP} pin to DGND will provide a 5V LCD drive voltage.

Digital Input Logic Levels

Logic levels for the TC820 digital inputs are referenced to V_S^+ and DGND. The high-level threshold is V_S^+ –1.5V and the low logic level is DGND +1.5V. In most cases,

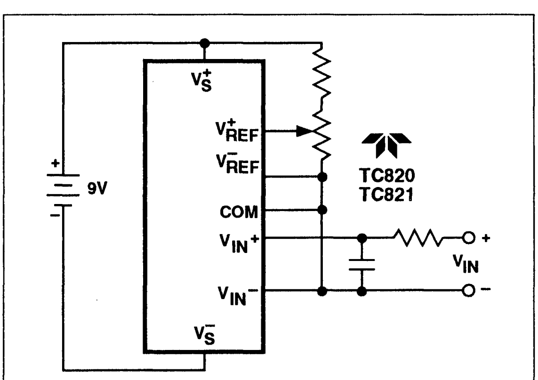


Figure 12. Powering the TC820/821 From a Single 9V Battery

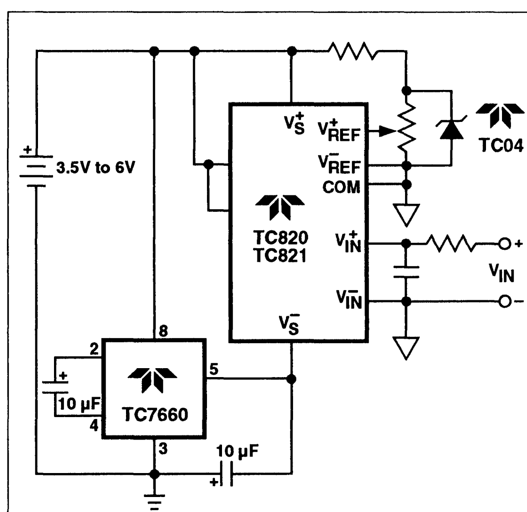


Figure 13. Powering the TC820/821 From a Low-Voltage Battery

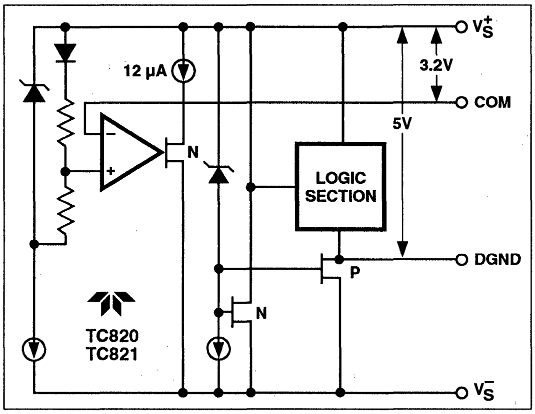


Figure 14. DGND and COM Outputs

digital inputs will be connected directly to V_S^+ with a mechanical switch. CMOS gates can also be used to control the logic inputs, as shown in the logic probe inputs section.

Clock Oscillator

The TC820 oscillator can be controlled with either a crystal or with an inexpensive resistor-capacitor combination. The crystal circuit, shown in Figure 15, is recommended when high accuracy is required in the frequency counter mode. The 40 kHz crystal is a standard frequency for ultrasonic alarms, and will provide a 1-second time base for the counter or 2.5 analog-to-digital conversions per second. Consult the crystal manufacturer for detailed applications information.

Where low cost is important, the R-C circuit of Figure 16 can be used. The frequency of this circuit will be approximately:

$$f_{OSC} = \frac{0.3}{RC}$$

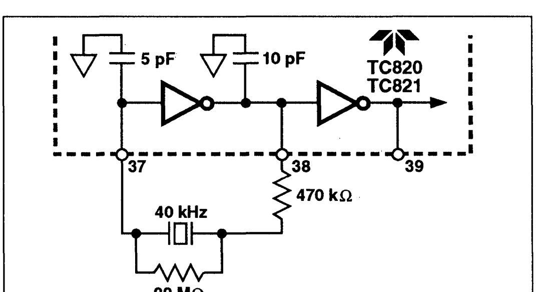


Figure 15. Suggested Crystal Oscillator Circuit

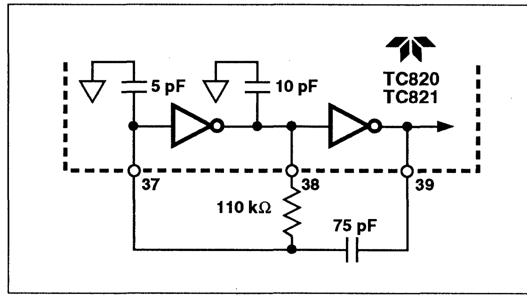


Figure 16. R-C Oscillator Circuit

Typical values are R = 10 kΩ and C = 68 pF. The resistor value should be ≥100 kΩ. For accurate frequency measurement, an R-C oscillator frequency of 40 kHz is required.

System Timing

All system timing is derived from the clock oscillator. The clock oscillator is divided by 2 (4 for TC821) prior to clocking the A/D counters. The clock is also divided by 8 to drive the buzzer, by 240 to generate the LCD backplane frequency, and by 40,000 for the frequency counter time base. A simplified diagram of the system clock is shown in Figure 17.

Component Value Selection

Auto Zero Capacitor — C_{AZ}

The value of the auto-zero capacitor (C_{AZ}) has some influence on system noise. A 0.47 µF capacitor is recommended; a low dielectric absorption capacitor (Mylar) is required.

Reference Voltage Capacitor — C_{REF}

The reference voltage capacitor used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 µF capacitor is typical. A good quality, low leakage capacitor (such as Mylar) should be used.

Integrating Capacitor — C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case, a ±2V integrator output swing is optimum when the analog input is near full scale. For 2.5 readings/second (f_{OSC} = 40 kHz) and V_{FS} = 400 mV, a 0.22 µF value is suggested. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to

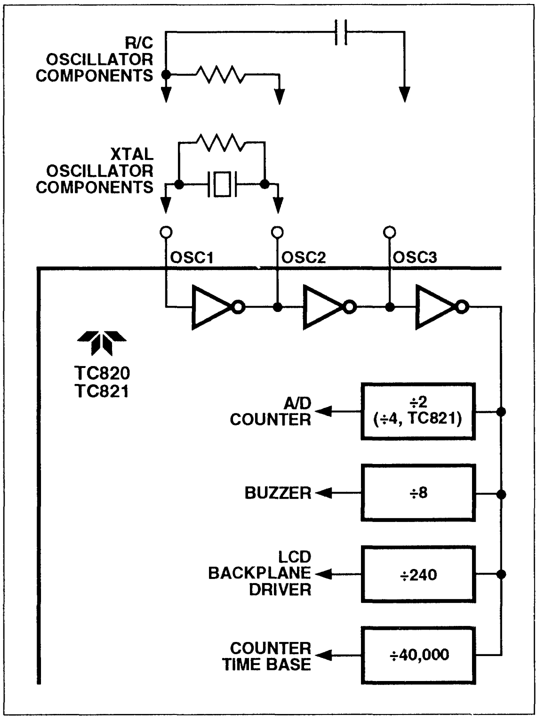


Figure 17. System Clock Generation

maintain the nominal ±2V integrator swing. An exact expression for C_{INT} is:

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT}\ R_{INT}\ f_{OSC}}$$

where: f_{OSC} = Clock frequency
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor — R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The integrator and buffer can supply 40 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 400 mV full scale, R_{INT} should be about 100 kΩ.

Reference Voltage Selection

A full-scale reading (4000 counts for TC820 and 2000 counts for TC821) requires the input signal be twice the reference voltage.

Table III. Reference Voltage Selection

Full-Scale Input Voltage (V_{FS}) (Note 1)	TC820 V_{REF}	TC820 Resolution	TC821 V_{REF}	TC821 Resolution
200 mV	Note 2		100 mV	100 µV
400 mV	200 mV	100 µV	200 mV	200 µV
1V	500 mV	250 µV	500 mV	500 µV
2V (Notes 3, 4)	1V	500 µV	1V	1 mV

NOTES:
1. TC820/821 in A/D converter mode, RANGE/FREQ = logic low.
2. Not recommended.
3. V_{FS} > 2V may exceed the input common mode range. See "10:1 Range Change" section.
4. Full-scale voltage values are not limited to the values shown. For example, TC820 V_{FS} can be any value from 400 mV to 2V.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, that a pressure transducer output is 800 mV for 4000 lb/in². Rather than dividing the input voltage by two, the reference voltage should be set to 400 mV. This permits the transducer input to be used directly.

The internal voltage reference potential available at analog common will normally be used to supply the converter's reference voltage. This potential is stable whenever the supply potential is greater than approximately 7V. The low-battery detection circuit and analog common operate from the same internal reference. This ensures that the low-battery annunciator will turn on at the time the internal reference begins to lose regulation.

The TC820 can also operate with an external reference. Figure 18 shows internal and external reference applications.

Ratiometric Resistance Measurements

The TC820 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 19). The voltage developed across the unknown is applied to the input and voltages across the known resistor

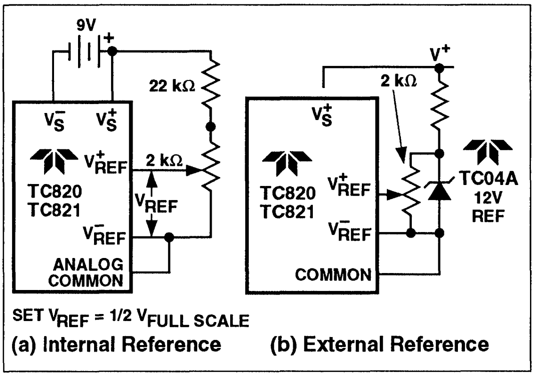


Figure 18. Reference Voltage Connections

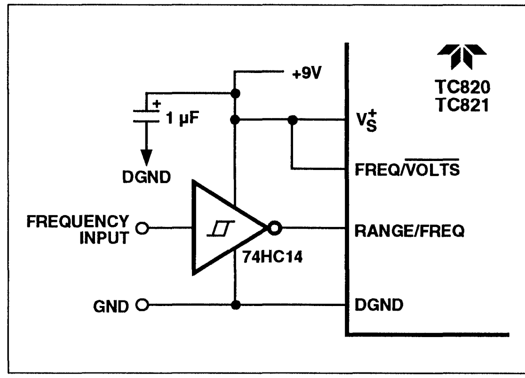


Figure 20. Frequency Counter External Buffer

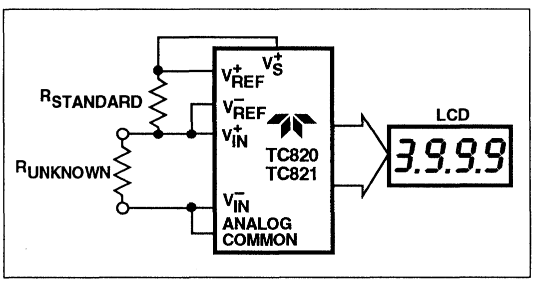


Figure 19. Low Parts Count Ratiometric Resistance Measurement

applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 2000 (1000 for TC821). The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 2000$$

The display will overrange for values of $R_{UNKNOWN} \geqslant 2 \times R_{STANDARD}$.

Buffering the FREQ Input

When the FREQ/$\overline{\text{VOLTS}}$ input is high and the LOGIC input is low, the TC820 will count pulses at the RANGE/FREQ input. The time base will be $f_{OSC}/40{,}000$, or 1 second with a 40 kHz clock. The signal to be measured should swing from V_S^+ to DGND. The RANGE/FREQ input has CMOS input levels without hysteresis. For best results, especially with low-frequency sine-wave inputs, an external buffer with hysteresis should be added. A typical circuit is shown in Figure 20.

Logic Probe Inputs

The DP0/LO and DP1/HI inputs provide the logic probe inputs when the LOGIC input is high. Driving either DP0/LO or DP1/HI to a logic high will turn on the appropriate LCD annunciator. When DP0/LO is high, the buzzer will be on.

To provide a "single input" logic probe function, external buffers should be used. A simple circuit is shown in Figure 21. This circuit will turn the appropriate annunicator on for high and low level inputs.

If carefully controlled logic thresholds are required, a window comparator can be used. Figure 22 shows a typical circuit. This circuit will turn on the high or low annunciators when the logic thresholds are exceeded, but the resistors connected from DP0/LO and DP1/HI to DGND will turn both annunciators off when the logic probe is unconnected.

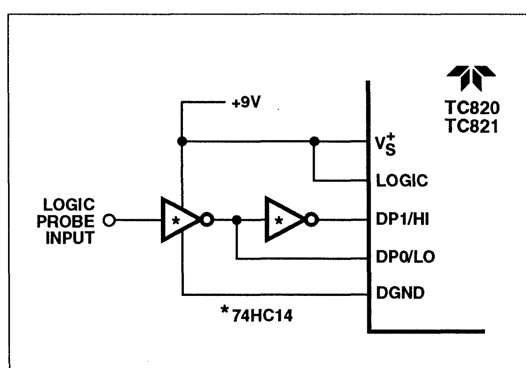
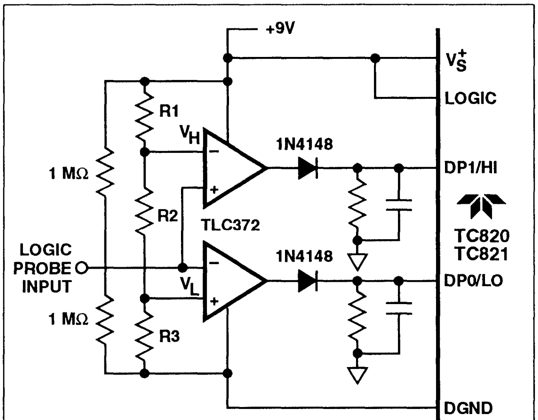


Figure 21. Simple External Logic Probe Buffer



NOTE: Select R1, R2, R3 for desired logic thresholds.

Figure 22. Window Comparator Logic Probe

The TC820 logic inputs are not latched internally, so pulses of short duration will usually be difficult or impossible to see. To display short pulses properly, the input pulse should be "stretched." The circuit of Figure 22 shows capacitors added across the input pull-down resistors to stretch the input pulse and permit viewing short-duration input pulses.

External Peak Detection

The TC820 will hold the highest A/D conversion or frequency reading indefinitely when the PK HOLD input is connected to V_S^+. However, the analog peak input must be present during the A/D converter's signal integrate period. For slowly changing signals, such as temperature, the peak reading will be properly converted and held.

If rapidly changing analog signals must be held, an external peak detector should be added. An inexpensive circuit can be made from an op-amp and a few discrete components, as shown in Figure 23. The droop rate of the external peak detector should be adjusted so that the held voltage will not decay below the desired accuracy level during the converter's 400 ms conversion time.

Liquid Crystal Display (LCD)

The TC820 drives a triplex (multiplexed 3:1) LCD with three backplanes. The LCD can include decimal points, polarity sign, and annunciators for overrange, peak hold, high and low logic levels, and low battery. Table IV shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 240.

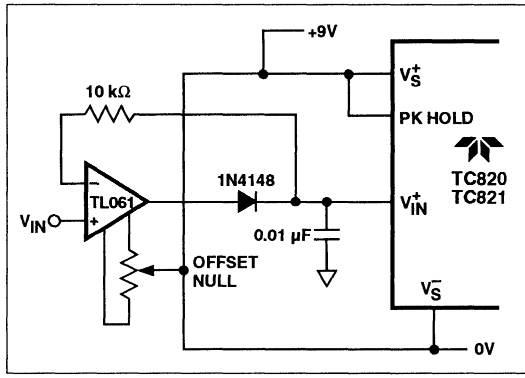


Figure 23. External Peak Detector

Backplane waveforms are shown in Figure 24. These appear on outputs BP1, BP2, and BP3. They remain the same regardless of the segments being driven.

Other display output lines have waveforms that vary depending on the displays values. Figure 25 shows a set of waveforms for the a, g, d outputs of one digit for several combinations of "on" segments.

Table IV. LCD Backplane and Segment Assignments

40-Pin DIP Pin No.	44-Pin Flat Pkg Pin No.	LCD Display Pin No.	BP1	BP2	BP3
1	40	3	LOW	"—"	E4
2	41	4	A4	G4	D4
3	42	5	B4	C4	DP3
4	43	6	HIGH	F3	E3
5	44	7	A3	G3	D3
6	1	8	B3	C3	DP2
7	2	9	OVER	F2	E2
8	3	10	A2	G2	D2
9	4	11	B2	C2	DP1
10	5	12	PEAK	F1	E1
11	6	13	A1	G1	D1
12	7	14	B1	C1	BATT
13	8	2,16*	—	—	BP3
14	9	1	—	BP2	—
15	10	15	BP1	—	—

*Connect both pins 2 and 16 of LCD to TC820 BP3 output.

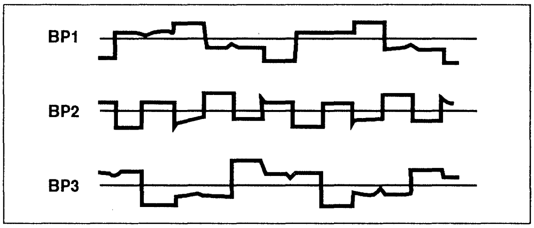


Figure 24. Backplane Waveforms

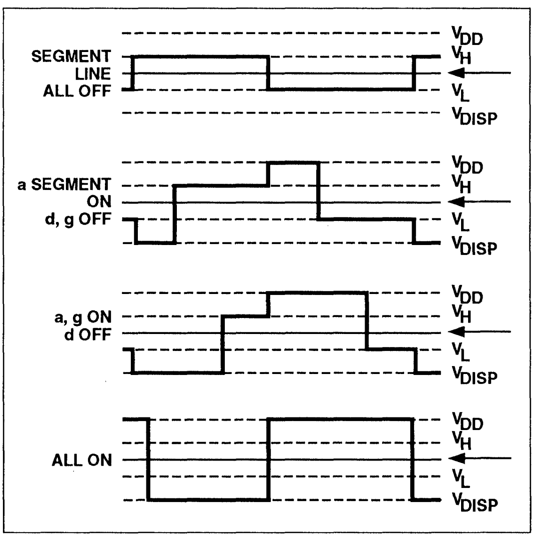


Figure 25. Typical Display Output Waveforms

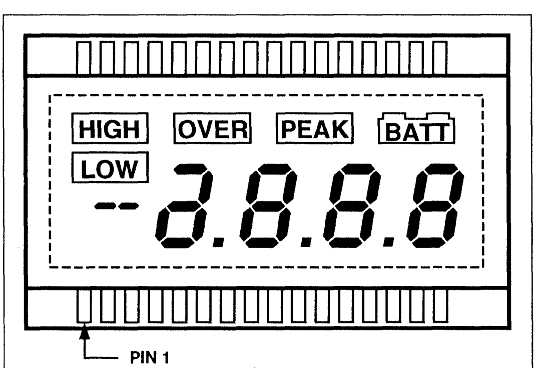


Figure 26. Typical TC820/821 LCD

LCD Source

Although most users will design their own custom LCD, a standard display for the TC820 (Figure 26), Part No. ST-1355-M1, is available from:

Crystaloid (USA)	Crystaloid (Europe)
Crystaloid Electronics	Rep France
P.O. Box 628	102, rue des Nouvelles
5282 Hudson Dr.	F92150 Suresnes
Hudson, OH 44238	France
Phone: (216) 655-2429	Phone: 33-1-42 04 29 25
Fax: (216) 655-2176	Fax: 33-1-45 06 46 99

This display can also be used with the TC821.

Annunciator Output

The annunciator output is a square wave running at the backplane frequency (for example, 167 Hz when $f_{OSC} = 40$ kHz). The peak-to-peak amplitude is equal to ($V_S^+ - V_{DISP}$). Connecting an annunciator of the LCD to the annunciator output turns it on; connecting it to its backplane turns it off.

LCD Drive Voltage (V_{DISP})

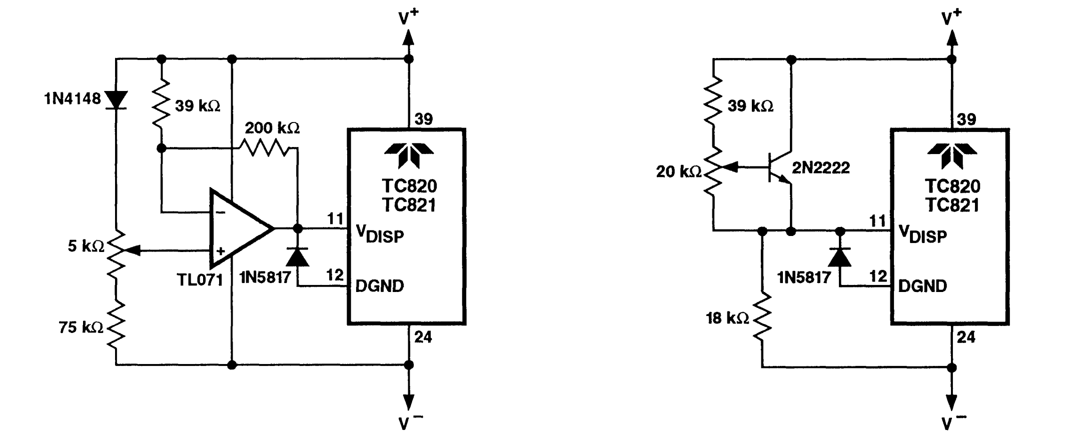
The peak-to-peak LCD drive voltage is equal to ($V_S^+ - V_{DISP}$). In the 40-pin dual-in-line package (DIP), V_{DISP} is internally connected to DGND, providing a typical LCD drive voltage of 5 $V_{P\text{-}P}$.

For applications with a wide temperature range, some LCDs require that the drive levels vary with temperature to maintain good viewing angle and display contrast. In this case, the TC820 44-pin package provides a pin connection for V_{DISP}. Figure 27 shows TC820 circuits that can be adjusted to give a temperature compensation of about 10 mV/°C between V_S^+ and V_{DISP}. The diode between GND and V_{DISP} should have a low turn-on voltage because V_{DISP} cannot exceed 0.3V below GND.

Crystal Source

Two sources of the 40 kHz crystal are:

Statek Corp	SPK Electronics
512 N. Main St	2F-1, No. 312, Sec 4,
Orange, CA 92668	Jen Ai Rd
Phone: (714) 639-7810	Taipei, Taiwan R.O.C.
Fax: (714) 997-1256	Phone: (02) 754-2677
Part #: CX-1V-40.0	Fax: 886-2-708-4124
	Part#: QRT-38-40.0 kHz



NOTE: Pin numbers shown are for 44-pin flat package.

Figure 27. Temperature-Compensating Circuits

NOTES

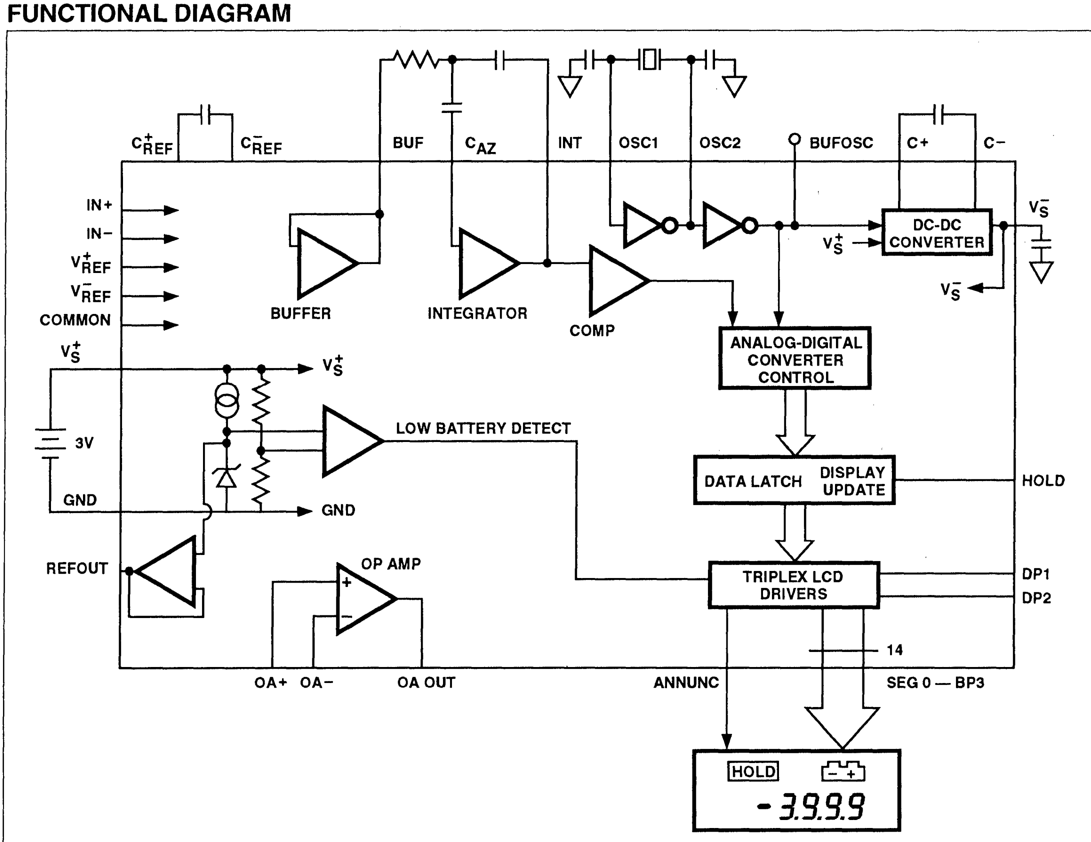
TC822
TC823

3-3/4 DIGIT LCD ANALOG TO DIGITAL CONVERTER

FEATURES

- 3-3/4 Digit (3999 maximum) Resolution
- 3V Battery Operation
  - — On-Chip DC-to-DC Converter
- Low Power Operation
  - — Supply Current 400 μA Typical
- Differential Signal Inputs
- Differential Reference Inputs
- LCD with Triplexed drive
  - — 3-3/4 Digit Resolution
  - — 3 Decimal Points
  - — LCD Annunciator Driver Output
  - — Low-battery and Hold Annunciators
- Op-amp for AC-to-DC Converter
- Display HOLD with LCD Annunciator
- Low-battery Detect with LCD Annunciator
- On-chip Band-gap Reference
- Crystal Oscillator
- 40-Pin DIP or 44-Pin Flat Package

FUNCTIONAL DIAGRAM



3-3/4 DIGIT LCD ANALOG TO DIGITAL CONVERTER

TC822
TC823

GENERAL DESCRIPTION

The TC822 is a 3-3/4 digit LCD analog-to-digital converter ADC which operates from a single 3V battery. Product designs utilizing the TC822 offer higher performance, lower parts count and smaller size than 7106-based designs, while the 3V battery permits a wide variety of packaging options.

All active components necessary to construct a 0.025% resolution measurement system are included on the TC822. Only external resistors and capacitors, an LCD and a battery are required.

The TC822 includes features which must be added externally with ADCs such as the 7106. LCD decimal point drivers, low-battery detection, and data hold function with LCD annunciator are all on chip. No external exclusive-OR gates are required. An operational amplifier, which can be used for an AC-to-DC converter or resistance measurement current source, is also included.

Differential signal inputs with 1 pA leakage simplify system design. Differential reference inputs permit ratiometric measurements, while retaining the data HOLD function. Either the internal 1.3V band-gap reference or an external reference can be used.

The TC822 LCD drive includes 3-3/4 digits, decimal points, and HOLD and low-battery annunciators. The triplexed LCD requires only 14 interconnects, which increases reliability and simplifies mechanical design.

Package options include a 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC), and compact flat packages. The many on-chip features of the TC822, combined with the compact flat package and 3V battery, permit the design of very small, high quality, economical instruments.

The TC823 offers all the features of the TC822, but with a resolution of 3-1/2 digits.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_S^+ to GND) .... +4.7V
Analog Input Voltage (either input) .... V_S^+ to V_S^-
(Note 1)
Reference Input Voltage (either input) .... V_S^+ to V_S^-
Op Amp Input Voltage (either input) .... V_S^+ to V_S^-
Digital Inputs .... V_S^+ to GND
Power Dissipation, Plastic Package .... 800 mW
Operating Temperature Range
C Devices .... 0°C to +70°C
E Devices .... -40°C to +85°C
Storage Temperature Range .... -65°C to +150°C
Lead Soldering Temperature (10 sec) .... +300°C

NOTES:
1. Input voltages may exceed the supply voltages provided that input current is limited to ±100 µA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.
3. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.
4. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.

ORDERING INFORMATION

Part No.	Resolution Digits	44-Pin Plastic Flat Package	44-Pin Plastic Leaded Chip (PLCC)	40-Pin Plastic DIP	Temperature Range
TC822CKW	3-3/4	X			0°C to +70°C
TC822CLW	3-3/4		X		0°C to +70°C
TC822CPL	3-3/4			X	0°C to +70°C
TC822EKW	3-3/4	X			–40°C to +85°C
TC822ELW	3-3/4		X		–40°C to +85°C
TC822EPL	3-3/4			X	–40°C to +85°C
TC823CKW	3-1/2	X			0°C to +70°C
TC823CLW	3-1/2		X		0°C to +70°C
TC823CPL	3-1/2			X	0°C to +70°C
TC823EKW	3-1/2	X			–40°C to + 85°C
TC823ELW	3-1/2		X		–40°C to +85°C
TC823EPL	3-1/2			X	–40°C to + 85°C

3-3/4 DIGIT LCD
ANALOG TO DIGITAL CONVERTER

TC822
TC823

ELECTRICAL CHARACTERISTICS: $V_S = 3.0$ V, $T_A = 25°$ C, Figure 1 Test Circuit

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Input						
	Zero Input Reading	$V_{IN} = 0.0V$ Full-Scale = 400 mV	–0000	0000	+0000	Digital Reading
RE	Roll-Over Error	$V_{IN} = \pm 390$ mV Full-Scale = 400 mV	–1	±0.2	+1	Counts
NL	Non-Linearity (Max Deviation from Best Straight Line Fit)	Full-Scale = 400 mV	–1	±0.2	+1	Count
	Ratiometric Reading	$V_{IN} = V_{REF}$	1999	1999/ 2000	2000	Digital Reading
E_N	Noise (p-p value not exceeded 95% of time)	$V_{IN} = 0.0V$ Full-Scale = 400 mV	—	15	—	µV
I_{IN}	Input Leakage Current	$V_{IN} = 0.0$ V $T_A = 25°C$ $0°C \le T_A \le +70°C$ $-40°C \le T_A \le +85°C$	 — — —	 — 20 100	 10 100 250	 pA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 0.2V$, $V_{IN} = 0.0$ V Full-Scale= 400 mV	—	50	—	µV/V
V_{CMR}	Common-Mode Voltage Range	Input High, Input Low $V_{IN} = 0.0V$, Full-Scale = 400 mV	GND –0.5	—	GND +0.5	V
TC_{ZS}	Zero Reading Drift	$V_{IN} = 0.0V$ $0°C \le T_A \le +70°C$ $-40°C \le T_A \le +85°C$ Ext. Ref. 0 ppm/°C	 — —	 0.2 1	 — —	 µV/°C
TC_{FS}	Scale Factor Temperature Coefficient	$V_{IN} = 399$ mV $0°C \le T_A \le +70°C$ $-40°C \le T_A \le +85°C$ Ext. Ref. 0 ppm/°C	 — —	 ±1 ±5	 ±5 ±25	 ppm/°C
	Input Voltage Range	V_{IN}^+, V_{IN}^- Normal Mode + Common-Mode Voltage	GND –0.5	—	GND +0.5	V
Reference						
V_{REF}	Reference Voltage	$I_L = 25$ µA (V_{REF}-GND)	1.25	1.3	1.45	V
TCV_{REF}	Reference Voltage Temperature Coefficient	$0°C \le T_A \le +70°C$	—	50	—	ppm/°C
Op-Amp						
V_{IOA}	Op-Amp Input Offset Voltage	$V_S = 3V$	—	±10	—	mV
	Op-Amp Input Voltage Range		—	±2	—	V
	Op-Amp Unity Gain Frequency		—	0.6	—	MHz
	Op-Amp Output Voltage Swing	$R_L = 100$ kΩ to GND	—	±2.5	—	V
	Op-Amp Slew Rate	$R_L = 100$ kΩ to GND, CL = 50 pF	—	1	—	V/µs

ELECTRICAL CHARACTERISTICS (Cont.): V_S = 3.0 V, T_A = 25° C, Figure 1 Test Circuit

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Digital						
V_{IL}	Input Low Voltage	DP1, DP2, HOLD	—	—	GND +0.5	V
V_{IH}	Input High Voltage	DP1, DP2, HOLD	V_S^+ –0.5	—	—	V
	Control Pin Pulldown Current	$V_{IN} = V_S^+$	—	3	—	μA
	LCD Drive Voltage	$2V \le V_S^+ \le 4V$	3.1	3.2	3.3	V p-p
Power Supply						
I_S	Supply Current	V_{IN} = 0.0V V_S^+ =3.0 V	—	400	600	μA
	Supply Operating Voltage Range	V_S^+ to GND	2	—	4	V
	Low-Battery Flag Voltage	V_S^+ to GND	2.15	2.25	2.45	V

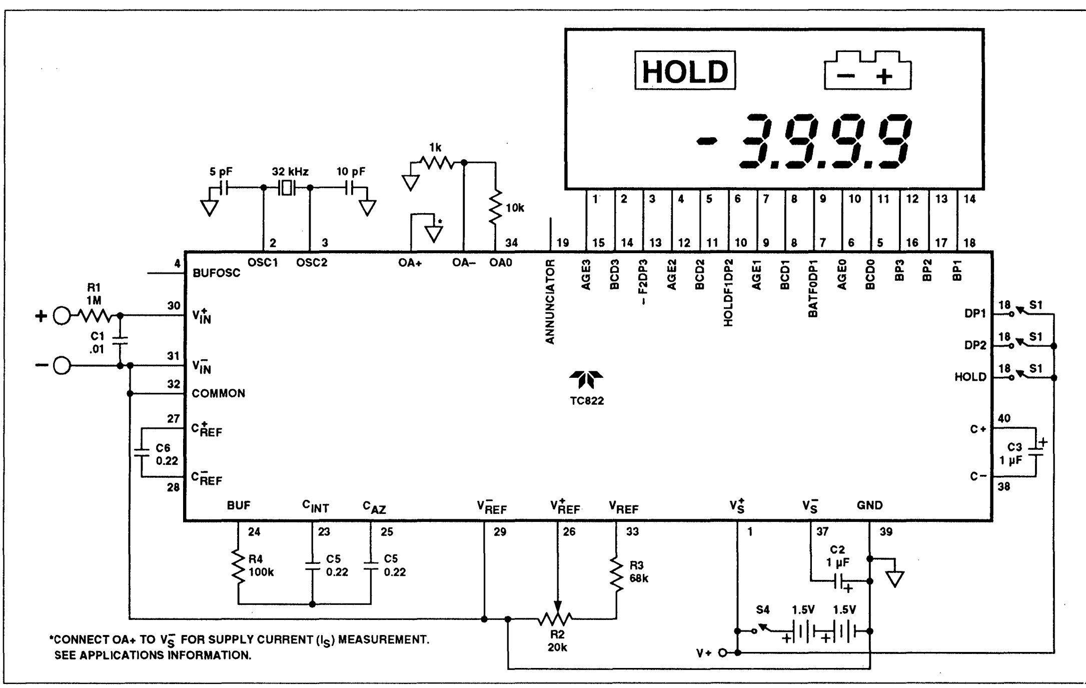
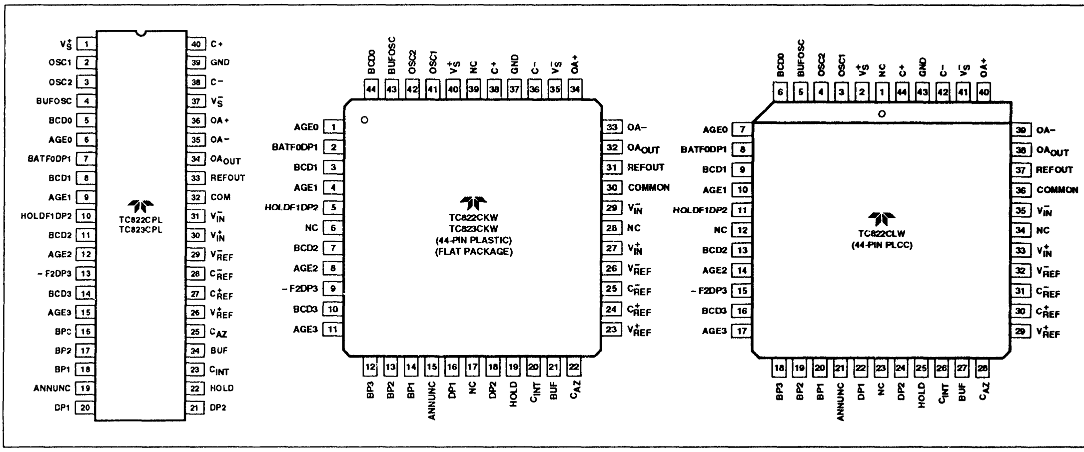


Figure 1 Test Circuit

3-3/4 DIGIT LCD ANALOG TO DIGITAL CONVERTER

TC822 TC823

PIN CONFIGURATIONS



PRELIMINARY PIN DESCRIPTION AND FUNCTION, TC822 3-3/4 DIGIT A-D CONVERTER, 3V OPERATION

Pin No. (40-Pin Package)	Symbol	Description
1	V_S^+	Positive battery supply connection. Typically 3V.
2	OSC1	Oscillator connection.
3	OSC2	Oscillator connection.
4	BUFOSC	Buffered oscillator output.
5	BCD0	LCD segment drive for 'b', 'c', and 'd' segments of least significant digit (LSD).
6	AGE0	LCD segment drive for 'a', 'g', and 'e' segments of LSD.
7	BATF0DP1	LCD segment drive for LOW-BATTERY, 'f' segment of LSD, and decimal point 1.
8	BCD1	LCD segment drive for 'b', 'c', and 'd' segments of 2nd LSD.
9	AGE1	LCD segment drive for 'a', 'g', and 'e' segments of 2nd LSD.
10	HOLDF1DP2	LCD segment drive for 'data hold', 'f' segment of 2nd LSD, and decimal point 2.
11	BCD2	LCD segment drive for 'b', 'c', and 'd' segments of 3rd LSD.
12	AGE2	LCD segment drive for 'a', 'g', and 'e' segments of 3rd LSD.
13	–F2DP3	LCD segment drive for 'polarity', 'f' segment of 3rd LSD, and decimal point 3.
14	BCD3	LCD segment drive for 'b', 'c', and 'd' segments of most significant digit (MSD).
15	AGE3	LCD segment drive for 'a', 'g', and 'e' segments of MSD.
16	BP3	LCD backplane #3.
17	BP2	LCD backplane #2.
18	BP1	LCD backplane #1.
19	ANNUNC	Square wave output at the backplane frequency, synchronized to BP1. ANNUNC can be used to control display annunciators. Connecting an LCD segment to ANNUNC turns it on; connecting it to its backplane turns it off.
20	DP1	Decimal Point select input.
21	DP2	Decimal Point select input.
22	HOLD	Hold input. Connecting this pin to V_S^+ will 'freeze' the LCD.

PRELIMINARY PIN DESCRIPTION AND FUNCTION, TC822 3-3/4 DIGIT A-D CONVERTER, 3V OPERATION (Cont.)

Pin No. (40-Pin Package)	Symbol	Description
23	C_{INT}	Integrator output. Connect to integration capacitor.
24	BUF	Buffer output. Connect to integration resistor.
25	C_{AZ}	Autozero capacitor connection.
26	V_{REF}^+	High differential reference input connection.
27	C_{REF}^+	Positive connection for reference capacitor.
28	C_{REF}^-	Negative connection for reference capacitor.
29	V_{REF}^-	Low differential reference input connection.
30	V_{IN}^+	High analog input signal connection.
31	V_{IN}^-	Low analog input signal connection.
32	COM	Analog circuit ground reference point.
33	REFOUT	Output of 1.3V voltage reference.
34	OA_{OUT}	Output of uncommitted operational amplifier.
35	OA-	Inverting input of uncommitted operational amplifier.
36	OA+	Noninverting input of uncommitted operational amplifier.
37	V_S^-	Output of DC-to-DC converter. Connect a 1 μF capacitor from this pin to power ground.
38	C–	Capacitor connection for DC-to-DC converter.
39	GND	Power ground.
40	C+	Capacitor connection for DC-to-DC converter.

FEATURES

The TC822 and TC823 are high-resolution analog-to-digital converters which include all of the active components required to build a typical digital multimeter or other measurement instrument. The on-chip op-amp can be configured as a sensor amplifier, AC-to-DC converter, or resistance measurement current source. The LCD includes decimal points, low-battery detection, and data hold annunciators. A DC-to-DC converter permits operation from a single 3V battery. With on-chip voltage reference and LCD drive circuitry, the TC822 simplifies the design of multi-mode measurement instruments.

The TC822 has a resolution of 3-3/4 digits (3999, maximum) while the TC823 has a resolution of 3-1/2 digits (1999, maximum). The features of both converters are the same, so that both 3-3/4 digit and 3-1/2 digit designs can be produced with only one basic design. The differences between the TC822 and the TC823 primarily affect system timing, and are noted in the ADC System Timing section of the data sheet.

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC822 ADC operates on the principle of dual-slope integration. An understanding of the dual-slope conversion technique will aid the user in following the detailed TC822 theory of operation following this section. A conventional dual-slope converter measurement cycle has two distinct phases:

1) Input Signal Integration
2) Reference Voltage Integration (Deintegration)

Referring to Figure 2, the unknown input signal to be converted is integrated from zero for a fixed time period (t_{INT}), measured by counting clock pulses. A constant reference voltage of the opposite polarity is then integrated until the integrator output voltage returns to zero. The reference integration (deintegration) time (t_{DEINT}) is then directly proportional to the unknown input voltage (V_{IN}).

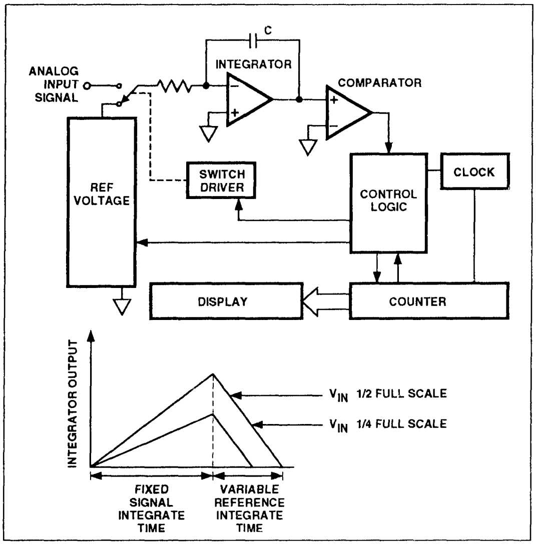


Figure 2 Basic Dual-Slope Converter

In a simple dual-slope converter, a complete conversion requires the integrator output to 'ramp-up' from zero and 'ramp-down' back to zero. A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}C_{INT}}\int_0^{t_{INT}} V_{IN}(t)dt = \frac{V_{REF}t_{DEINT}}{R_{INT}C_{INT}}$$

where: V_{REF} = Reference Voltage
t_{INT} = Integration Time
t_{DEINT} = Deintegration Time

For a constant T_{INT}:

$$V_{IN} = V_{REF} \bullet \frac{t_{DEINT}}{t_{INT}}$$

Accuracy in a dual-slope converter is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. An inherent benefit of the dual-slope technique is noise immunity. Noise spikes are integrated, or averaged, to zero during the integration periods, making integrating ADCs immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals, with frequency components at multiples of the averaging (integrating) period, will be attenuated (see Figure 3). Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period.

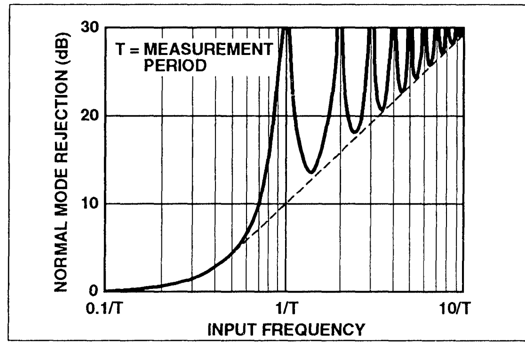


Figure 3 Normal-Mode Rejection of Dual-Slope Converter

TC822 ADC THEORY OF OPERATION

Analog Section

In addition to the basic integrate and deintegrate dual-slope phases discussed above, the TC822 design incorporates a 'Zero Integrator Output' phase and an 'Auto Zero' phase. These additional phases ensure that the integrator starts at zero volts (even after a severe over-range conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

1) Zero Integrator Output Phase
2) Auto Zero Phase
3) Signal Integrate Phase
4) Reference Deintegrate Phase

Zero Integrator Output Phase

This phase guarantees that the integrator output is at zero volts after an overrange input occurs. Thus, the next reading after an overranged reading will be correct. The ZI phase duration varies from 0 to 600 counts.

Auto Zero Phase

During the Auto Zero phase, the differential input signal is disconnected from the measurement circuit by opening internal analog switches and the internal nodes are shorted to Analog Common (0 volt ref) to establish a zero input condition. Additional analog switches close a feedback loop around the integrator and comparator to permit comparator offset voltage error compensation. A voltage established on C_{AZ} then compensates for internal device offset voltages during the measurement cycle. The Auto Zero phase residual is typically 10 to 15 μV. The Auto Zero duration is 1600 counts, plus the ZI counts if an overrange did not occur, plus unused deintegration counts. Thus, the AZ phase can occupy from 1600 to 6000 counts (600 to 3000 counts for TC823).

Signal Integration Phase

Upon completion of the Auto Zero phase, the Auto Zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is then integrated for a fixed time period, which in the TC822 is 2000 counts (4000 clock periods) and in the TC823 is 1000 counts (4000 clock periods). The externally set clock frequency is divided by two (TC822) or four (TC823) before clocking the internal counters. The integration time period is:

$$t_{INT} = \frac{4000}{f_{OSC}}$$

Note that, for the same clock frequency, the TC822 and TC823 will have the same signal integration time. Therefore, the noise rejection performance of the two converters will be the same.

Polarity is determined at the end of signal integration phase. The sign bit is a 'true polarity' indication in that signals less than 1 LSB are correctly determined. This allows precision null detection which is limited only by device noise and Auto Zero residual offsets.

Reference Integrate (Deintegrate) Phase

The reference capacitor, which was charged during the Auto Zero phase, is connected to the input of the integrating amplifier. The internal sign logic insures that the polarity of the reference voltage is always connected in the phase which is opposite to that of the input voltage. This causes the integrator to ramp back to zero at a constant rate which is determined by the reference potential.

The amount of time required (t_{DEINT}) for the integrating amplifier to reach zero is directly proportional to the amplitude of the voltage that was put on the integrating capacitor (V_{INT}) during the integration phase:

$$t_{DINT} = \frac{R_{INT} \bullet C_{INT} \bullet V_{INT}}{V_{REF}}$$

The digital reading displayed by the TC822 is:

$$\text{Digital Count} = 2000 \bullet \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

For the TC823, the digital reading displayed is:

$$\text{Digital Count} = 1000 \bullet \frac{V_{IN}^+ - V_{IN}^-}{V_{REF}}$$

ADC System Timing

The oscillator frequency is divided by 2 (4 for TC823) prior to clocking the internal decade counters. The four phase measurement cycle takes a total of 8000 (4000) counts or 16000 (16000) clock pulses. The 8000 (4000) count phase is independent of input signal magnitude or polarity.

Each phase of the measurement cycle has the following length:

Conversion Phase	TC822	TC823	
1) Auto Zero	1600 to 5999	600 to 2999	Counts
2) Signal Integrate*	2000	1000	Counts
3) Reference Integrate	1 to 4000	1 to 2000	Counts
4) Integrator Output Zero	0 to 400	0 to 400	Counts

* This time period is fixed. The integration period for the TC822 is:

$$t_{INT\ (TC822)} = \frac{4000}{f_{OSC}} = 2000 \text{ Counts}$$

For the TC823, the integration period is:

$$t_{INT\ (TC823)} = \frac{4000}{f_{OSC}} = 1000 \text{ Counts}$$

where f_{OSC} is the clock oscillator frequency.

ANALOG PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs (V_{IN}^+, V_{IN}^-)

The TC822 is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The maximum input voltage range, which includes normal-mode + common-mode signals, is ±0.5V.

Common-mode voltages are removed from the system when V_{IN}^- is connected to Analog Common. The TC822's on-chip DC-to-DC converter eliminates most common-mode difficulties and permits measurements where measurement and power grounds cannot be isolated. (see Figure 4)

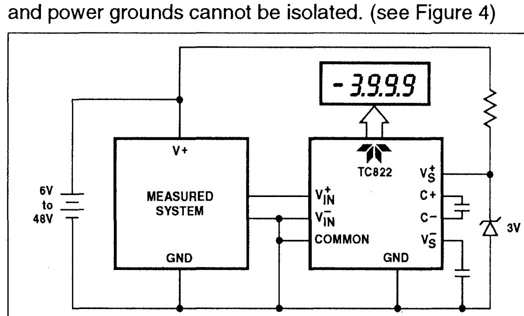


Figure 4 DC-to-DC Converter Permits Ground Referenced Measurements

Common-mode voltages with respect to power GND do, however, affect the integrator output level. The user must be particularly careful that the integrator does not saturate when at minimum battery voltage. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 5). For such applications the integrator output swing can be reduced below the recommended 1.5V full-scale swing. The integrator output will swing within 0.3V of V_S^+ or V_S^- without increased linearity error.

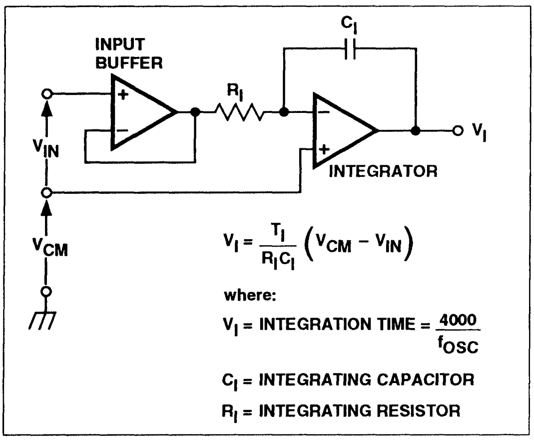


Figure 5 Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Reference Inputs (V_{REF}^+, V_{REF}^-)

The TC822 reference, like the analog signal input, has true differential inputs. In addition, the reference voltage can be generated anywhere within the power supply voltage of the converter. The differential reference inputs permit ratiometric measurements and simplify interfacing with sensors such as load cells and temperature sensors.

Reference Output (REFOUT)

This pin is the buffered output of the internal CMOS band-gap reference. The output voltage is typically 1.3V above power GND, with a load current of 25 µA. The temperature coefficient of REFOUT is typically 50 ppm/°C.

Analog Common

The TC822 connects the internal V_{IN}^+ and V_{IN}^- inputs to Analog Common during the Auto Zero cycle. During the reference integrate phase V_{IN}^- is connected to Analog Common. If V_{IN}^- is not externally connected to Analog Common, a common-mode voltage exists. This is rejected by the converter's 86 dB common-mode rejection ratio. In battery powered applications, Analog Common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, Analog Common should be connected to V_{IN}^-.

The Analog Common pin serves to set the analog section reference or common point. The TC822 is specifically designed to operate from a battery or in any measurement system where input signals are referenced to the TC822 power source, so Analog Common is normally connected to power GND.

DIGITAL PIN FUNCTIONAL DESCRIPTION

DP1, DP2

These inputs control the LCD decimal points. The decimal point truth table is shown in Table 1. These inputs have internal 3 µA pulldowns to DGND.

Table 1 TC822 Decimal Point Truth Table

Decimal Point DP2	Inputs DP1	LCD
0	0	3999
0	1	399.9
1	0	39.99
1	1	3.999

Hold

HOLD can be used to hold or 'freeze' the display. Connecting this pin to V_S^+ inhibits the display update process. Conversions will continue, but the display will not change.

APPLICATIONS INFORMATION

Power Supplies

The TC822 is designed to operate from a 3V battery, but will operate over a range of 2.0 to 4.0V. An on-chip DC-to-DC converter converts the +3V supply to –3V, which permits bipolar input voltages to be converted. Measurements are referenced to battery ground, so that the TC822/823 are ideal for applications such as measuring battery voltage, battery charging current, etc.

Op-Amp Power Supply Current

The op-amp of the TC822 has a low-distortion class A output, which is biased at 100 µA. To reduce supply current when the op-amp is not being used, connect the non-inverting input to V_S^-, as shown in Figures 6 and 11. When the op-amp is used, supply current will increase by about 200 µA.

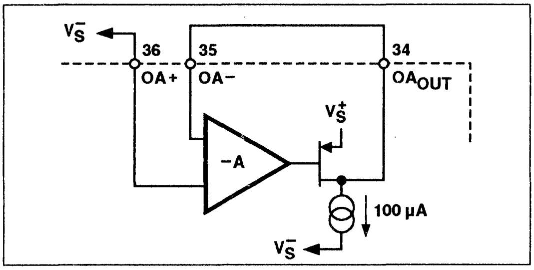


Figure 6 Simplified Op-Amp Output Schematic

Clock Oscillator

The crystal oscillator circuit is shown in Figure 7. An inexpensive 32.768 kHz watch crystal gives about 27 dB noise rejection at 60 Hz, while a 40 kHz crystal (used in ultrasonic alarms) will almost totally reject 50 and 60 Hz noise.

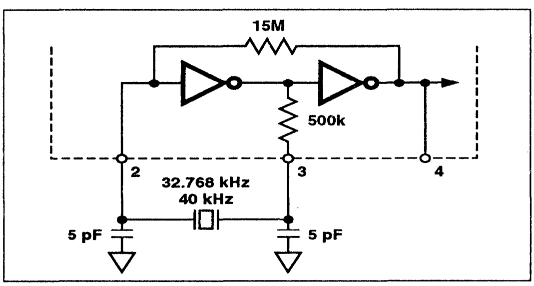


Figure 7 Crystal Oscillator Circuit

System Clock

All system timing is derived from the clock oscillator. The clock oscillator is divided by two (four for TC823) prior to clocking the A/D counters. The clock is also divided by 4 to drive the DC-to-DC converter, and by 768 to generate the LCD backplane frequency. A simplified diagram of the system clock is shown in Figure 8.

COMPONENT VALUE SELECTION

Auto Zero Capacitor - C_{AZ}

The size of the Auto Zero capacitor (C_{AZ}) has some effect on system noise. A 0.22 µF capacitor is recommended. A capacitor with low dielectric absorption (polyester) is required.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate

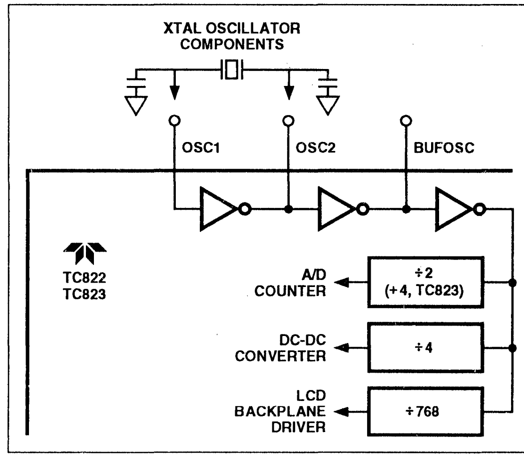


Figure 8 System Clock Generation

cycle is stored on C_{REF}. A 0.22 µF capacitor is typical. A good quality, low leakage capacitor, such as polyester, should be used.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference. For this case a ±1.5 V integrator output swing is optimum when the analog input is near full-scale. For 2.5 readings/second (f_{OSC} = 40 kHz) and V_{FS} = 400 mV, a 0.27 µF value is suggested. For a 32.768 kHz crystal, use 0.22 µF. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±1.5V integrator swing. An exact expression for C_{INT} is:

$$C_{INT} = \frac{4000\ V_{FS}}{V_{INT} \bullet R_{INT} \bullet f_{OSC}}$$

where: f_{OSC} = Clock frequency
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize roll-over error. A polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The integrator and buffer can supply 5 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 400 mV full-scale, R_{INT} should be about 100 kΩ.

Reference Voltage Selection

A full scale reading (4000 counts for TC822 and 2000 counts for TC823) requires that the input signal be twice the reference voltage. For example, a 400 mV full scale TC822 requires a reference voltage of 200 mV.

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, that a pressure transducer output is 500 mV for 4000 lb/in^2. Rather than dividing the input voltage by 1.25, the reference voltage should be set to 250 mV. This permits the transducer input to be used directly. For best results, full scale voltage should be limited to 500 mV.

The TC822 can also operate with an external reference. Figure 9 shows internal and external reference applications.

Ratiometric Resistance Measurements

The TC822 true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current is passed through the pair (Figure 10). The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the input voltage will equal the reference voltage and the display will read 2000 (1000 for TC823). The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \bullet 2000$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$

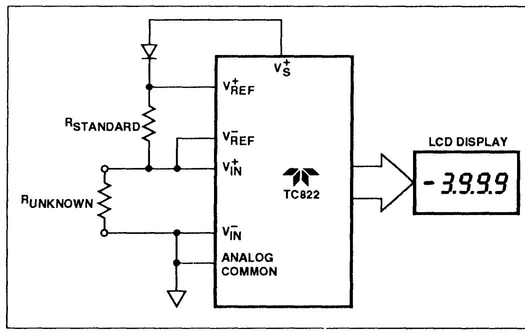


Figure 10 Low Parts Count Ratiometric Resistance Measurement

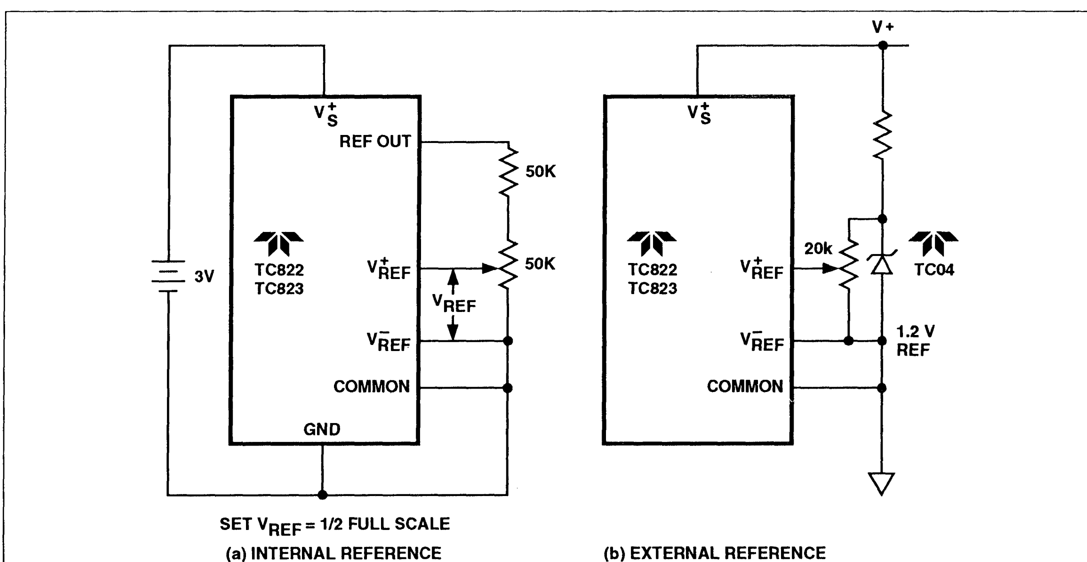


Figure 9 Internal and External Reference Applications

AC-to-DC Converter

The on-chip op amp of the TC822/823 can be combined with external components to convert an AC voltage into a DC voltage. Figure 11 shows a typical circuit.

LCD

The TC822 drives a triplex (multiplexed 3:1) liquid crystal display with three backplanes. The LCD includes decimal points, polarity sign, and annunciators for data hold and low-battery. Table 2 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 768.

Table 2 LCD Pin Assignment, TC822

Pin	COM1	COM2	COM3
1	COM1	—	—
2	—	COM2	—
3	—	—	COM3
4	B0	C0	D0
5	A0	G0	E0
6	BATTERY	F0	P1
7	B1	C1	D1
8	A1	G1	E1
9	HOLD	F1	P2
10	B2	C2	D2
11	A2	G2	E2
12	Y	F2	P3
13	B3	C3	D3
14	A3	G3	E3
15	—	—	—
16	—	—	—
17	—	—	—
18	—	—	—

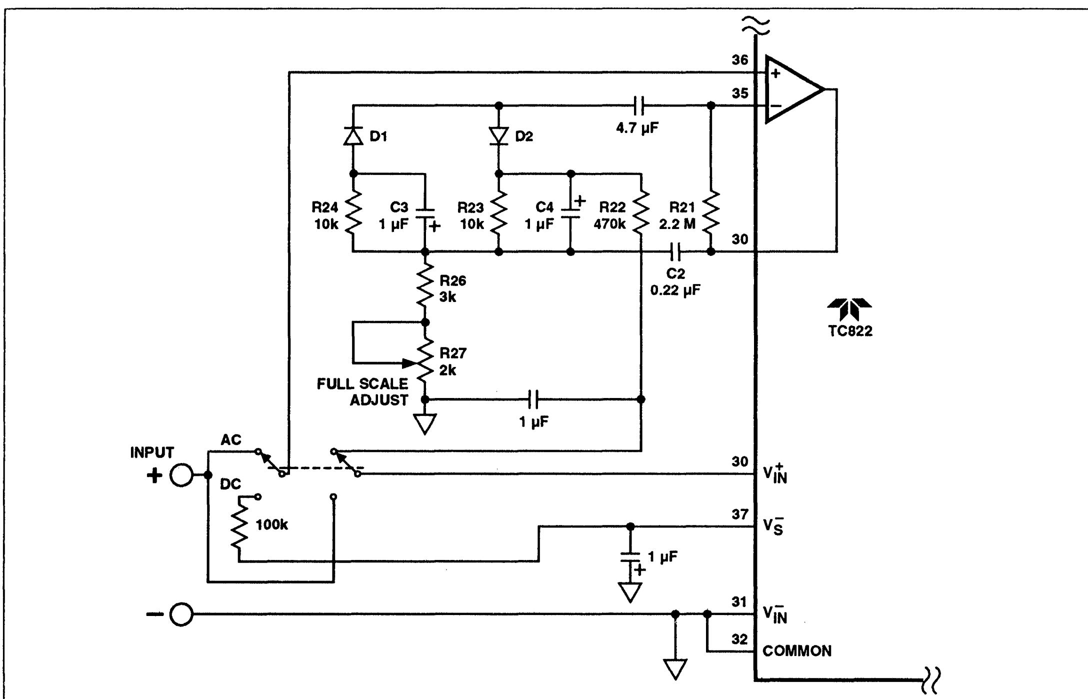


Figure 11 Low Cost AC-to-DC Converter

Backplanes waveforms are shown in Figure 12. These appear on outputs BP1, BP2, and BP3. They remain the same regardless of the segments being driven.

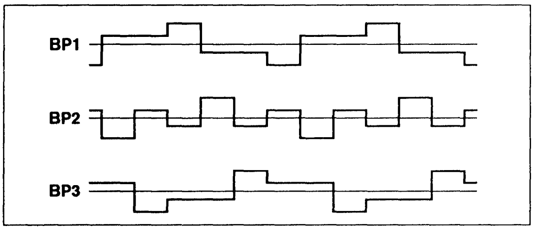


Figure 12 Backplane Waveforms

Other display output lines have waveforms that vary depending on the displays values. Figure 13 shows a set of waveforms for the AGE outputs of one digit for several combinations of 'on' segments.

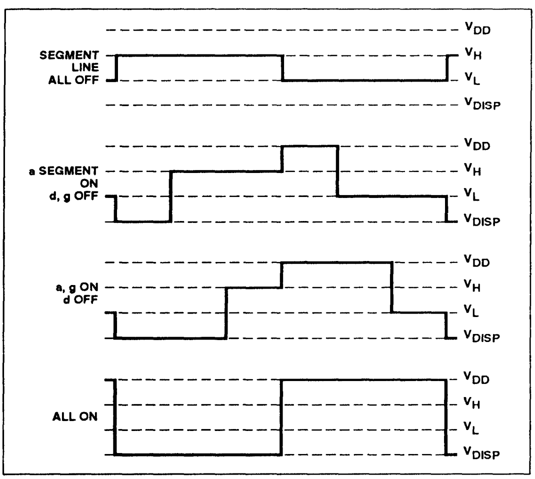


Figure 13 Typical Display Output Waveforms

LCD Source

Although most users will design their own custom LCD, a standard display for the TC822 is available. Figure 14 shows a display, part No. VIM428-DP, available from Varitronix.

Varitronix (USA)	Varitronix
VL Electronics	9/F Liven House
3171 Los Feliz Blvd	61-63 King Yip Street
Suite 303	Kwun Tjong
Los Angeles, CA 90039	Hong Kong
Tel: (312) 661-8883	Tel: 3-410286
FAX: (213) 663-3711	FAX: 3-439555
Part No.:jg VIM428-DP	

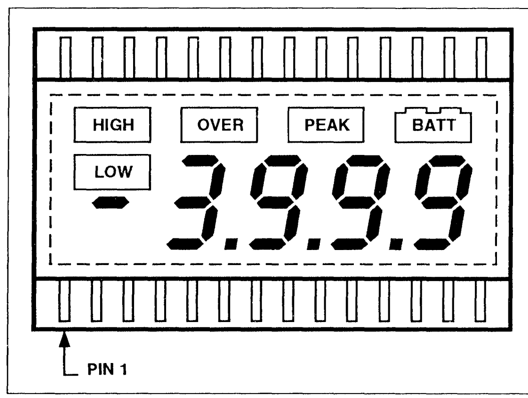


Figure 14 Typical TC822/823 LCD

Annunciator Output

The annunciator output is a square wave running at the backplane frequency (for example, 52 Hz when f_{OSC} = 40 kHZ). The peak-to-peak amplitude is the same as the backplane and segment driver outputs. Connecting an annunciator of the LCD to the annunciator output turns it on; connecting it to its backplane turns it off.

LCD Drive Voltage

The peak-to-peak LCD drive voltage is typically 3.2 Vpp. This voltage will remain stable until the battery voltage falls below the point where the low-battery flag turns on (about 2.1V).

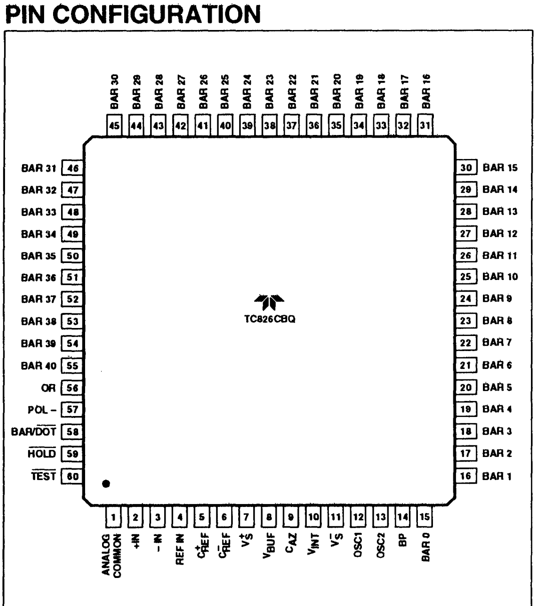
NOTES

A/D CONVERTER WITH BAR GRAPH DISPLAY OUTPUT

FEATURES

- **Bipolar A/D Conversion**
- **2.5% Resolution**
- **Direct LCD Display Drive**
- **'Thermometer' Bar or Dot Display**
- **40 Data Segments Plus Zero**
- **Overrange Plus Polarity Indication**
- **Precision On–Chip Reference .... 35 ppm/°C**
- **Differential Analog Input**
- **Low Input Leakage .... 10 pA**
- **Display Flashes on Overrange**
- **Display Hold Mode**
- **Auto–Zero Cycle Eliminates Zero Adjust Potentiometer**
- **9V Battery Operation**
- **Low Power Consumption .... 1.1 mW**
- **20 mV to 2.0 V Full–Scale Operation**
- **Non–Multiplexed LCD Drive for Maximum Viewing Angle**

PIN CONFIGURATION



GENERAL DESCRIPTION

In many applications a graphical display is preferred over a digital display. Knowing a process or system operates, for example, within design limits is more valuable than a direct system variable readout. A bar or moving dot display supplies information precisely without requiring further interpretation by the viewer.

The TC826 is a complete analog–to–digital converter with direct liquid crystal (LCD) display drive. The 40 LCD data segments plus zero driver give a 2.5% resolution bar display. Full–scale differential input voltage range extends from 20 mV to 2V. The TC826 sensitivity is 500 µv. A low drift 35 ppm/°C internal reference, LCD backplane oscillator and driver, input polarity LCD driver, and overrange LCD driver make designs simple and low cost. The CMOS design required only 125 µA from a 9V battery. In +5V systems a TC7660 DC to DC converter can supply the –5V supply. The differential analog input leakage is a low 10 pA.

Two display formats are possible. The BAR mode display is like a 'thermometer' scale. The LCD segment driver that equals the input plus all below it are on. The DOT mode activates only the segment equal to the input. In either mode the polarity signal is active for negative input signals. An overrange input signal causes the display to flash and activates the overrange annunciator. A hold mode can be selected that freezes the display and prevents updating.

The dual slope integrating conversion method with auto–zero phase maximizes noise immunity and eliminates zero–scale adjustment potentiometers. Zero–scale drift is a low 5 µV/°C. Conversion rate is typically 5 per second and is adjustable by a single external resistor.

A compact, 0.5" square, flat package minimizes PC board area. The high pin count LSI package makes multiplexed LCD displays unnecessary. Low cost, direct drive LCD displays offer the widest viewing angle and are readily available. A standard display is available now for TC826 prototyping work.

ORDERING INFORMATION

Part No.	Package	Temperature
TC826CBQ	60–Pin Plastic Quad Flat Package Formed Leads	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(1) .... V+ to V–
Package Power Dissipation
Flat Package .... 500 mW
Operating Temperature
'C' Devices .... 0°C to +70°C
Storage Temperature .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... 300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS:

unless otherwise stated V_S = 9V; ROSC = 430 kΩ; T_A = 25°C; Full–Scale = 20 mV.

No.	Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
1	—	Zero Input	V_{IN} = 0.0V	–0	±0	+0	Display
2	—	Zero Reading Drift	V_{IN} = 0.0V $0°C \le T_A \le 70°C$	—	0.2	1	µV/°C
3	NL	Linearity Error	Max Deviation From Best Straight Line	–1	0.5	+1	Count
4	—	Rollover Error	$-V_{IN} = +V_{IN}$	–1	0	+1	Count
5	EN	Noise	V_{IN} = 0V	—	60	—	μV_{P-P}
6	ILK	Input Leakage Current	V_{IN} = 0V	—	10	20	pA
7	CMRR	Common–Mode Rejection Ratio	VCM = ±1V V_{IN} = 0V	—	50	—	µV/V
8	—	Scale Factor Temperature Coefficient	$0 \le T_A \le 70°C$ External Ref. Temperature Coefficient = 0 ppm/°C	—	1	—	ppm/°C
9	VCTC	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ $0°C \le T_A \le 70°C$	—	35	100	ppm/°C
10	—	Analog Common Voltage	250 kΩ Between Common and V_S^+	2.7	2.9	3.35	V
11	VSD	LCD Segment Drive Voltage		4	5	6	V_{P-P}
12	VBD	LCD Backplane Drive Voltage		4	5	6	V_{P-P}
13	—	Power Supply Current		—	125	175	µA

NOTES:
1. Input voltages may exceed the supply voltages when the input current is limited to 100 µA.
2. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.
3. Backplane drive is in phase with segment drive for 'off' segment and 180°C out of phase for 'on' segment. Frequency is 10 times conversion rate.
4. Logic input pins 58, 59, and 60 should be connected through 1 MΩ series resistors to V_S^- for logic 0.

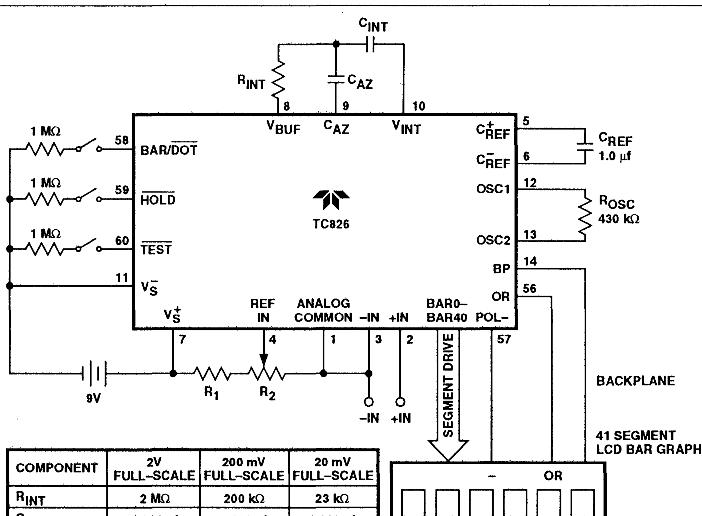
PIN DESCRIPTION AND FUNCTION

Pin No.	Name	Description
1	Analog Common	Establishes the internal analog ground point. Analog common is set to 2.9V below the positive supply by an internal zener reference circuit. The voltage difference beween V_S^+ and analog–common can be used to supply the TC826 voltage reference input at REF IN (Pin 4).
2	+IN	Positive analog signal input.
3	–In	Negative analog signal input.
4	REF IN	Reference voltage positive input. Measured relative ato analog–common. REF IN ≈ Full–Scale/2.
5	C_{REF} +	Reference capacitor connection.
6	C_{REF} –	Reference capacitor connection.
7	V_S^+	Positive supply terminal.
8	VBUF	Buffer output. Integration resistor connection.
9	CAZ	Negative comparator input. Auto–zero capacitor connection.
10	VINT	Integrator output. Integration capacitor connection.
11	VS–	Negative supply terminal.
12	OSC1	Oscillator resistor (R_{OSC}) connection.
13	OSC2	Oscillator resistor (R_{OSC}) connection.
14	BP	LCD Backplane driver.
15	BAR 0	LCD Segment driver: Bar 0
16	1	1
17	2	2
18	3	3
19	4	4
20	5	5
21	6	6
22	7	7
23	8	8
24	9	9
25	10	10
26	11	11
27	12	12
28	13	13
29	14	14
30	15	15
31	16	16
32	17	17
33	18	18
34	19	19
35	20	20
36	21	21
37	22	22
38	23	23
39	24	24
40	25	25
41	26	26
42	27	27
43	28	28

TC826

PIN DESCRIPTION AND FUNCTION (Cont.)

Pin No.	Name	Description
44	BAR 29	LCD Segment driver: Bar 29
45	30	30
46	31	31
47	32	32
48	33	33
49	34	34
50	35	35
51	36	36
52	37	37
53	38	38
54	39	39
55	40	40
56	OR	LCD segment driver that indicated input out–of–range condition.
57	POL–	LCD segment driver that indicates input signal is negative.
58	BAR / $\overline{\text{DOT}}$	Input logic signal that selects bar or dot display format. Normally in bar mode. Connect to V_S^- through 1MΩ resistor for Dot format.
59	$\overline{\text{HOLD}}$	Input logic signal that prevents display from changing. Pulled high internally to inactive state. Connect to V_S^- through 1MΩ series resistor for HOLD mode operation.
60	$\overline{\text{TEST}}$	Input logic signal. Sets TC805 to BAR display mode. Bar 0 to 40, plus OR flash on and off. The POL– LCD driver is on. Pulled high internally to inactive state. Connect to V_S^- with 1 MΩ series resistor to activate.



COMPONENT	2V FULL–SCALE	200 mV FULL–SCALE	20 mV FULL–SCALE
R_{INT}	2 MΩ	200 kΩ	23 kΩ
C_{INT}	0.033 µf	0.033 µf	0.033 µf
C_{REF}	1 µf	1 µf	1 µf
C_{AZ}	0.068 µf	0.068 µf	0.014 µf

$R_1 + R_2 = 250$ kΩ

Figure 1 Typical TC826 Circuit Connection

A/D CONVERTER WITH BAR GRAPH DISPLAY OUTPUT

DUAL SLOPE CONVERSION PRINCIPLES

The TC826 is a dual slope, integrating analog–to–digital converter. The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (TSI). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (TRI). (Figure 2).

In a simple dual slope converter a complete conversion requires the integrator output to 'ramp–up' and 'ramp–down'.

A simple mathematical equation relates the input signal reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R T_{RI}}{RC}$$

Where:

V_R = Reference Voltage

V_{SI} = Signal Integration Time (Fixed)

T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}: $V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. (Figure 3.)

The TC826 converter improves the conventional dual slope conversion technique by incorporating an auto-zero phase. This phase eliminates zero-scale offset errors and drift. A potentiometer is not required to obtain a zero output for zero input.

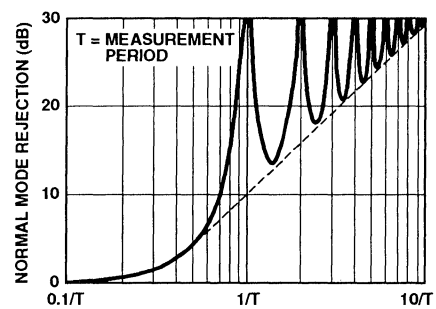


Figure 3 Normal-Mode Rejection of Dual Slope Converter

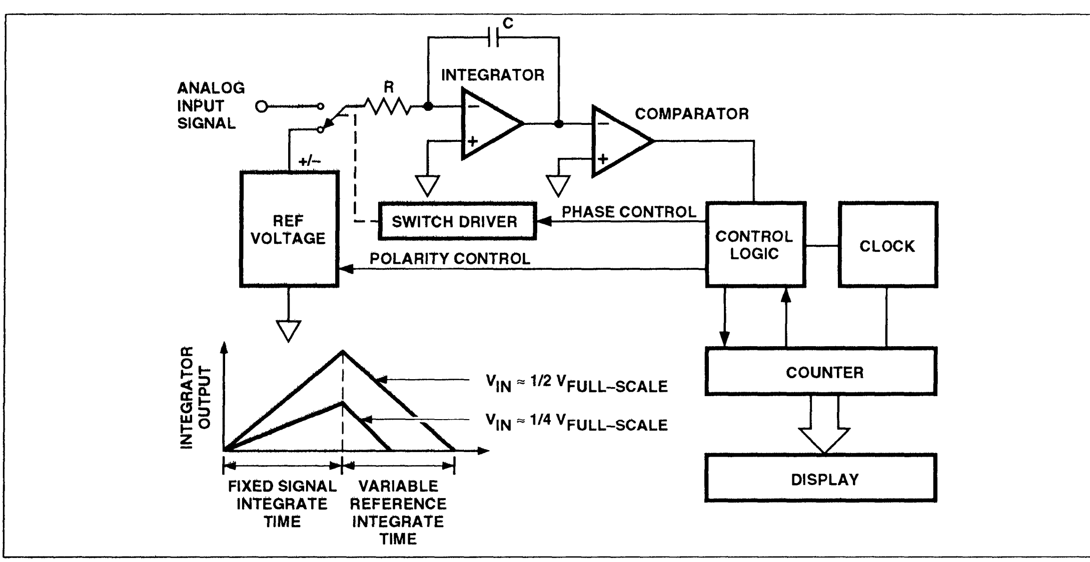


Figure 2 Basic Dual Slope Converter

THEORY OF OPERATION

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed above, the TC826 incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference cycle. (Figures 4 and 5.)

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (internal analog ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on CAZ compensates for device offset voltages.

The auto-zero cycle length is 19 counts minimum. Unused time in the deintegrate cycle is added to the auto-zero cycle.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to +IN and –IN. The differential input signal is integrated for a fixed time period. The TC826 signal integration period is 20 clock periods or counts. The externally set clock frequency is divided by 32 before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{32}{F_{OSC}} \times 20$$

Where:
F_{OSC} = External Clock Frequency

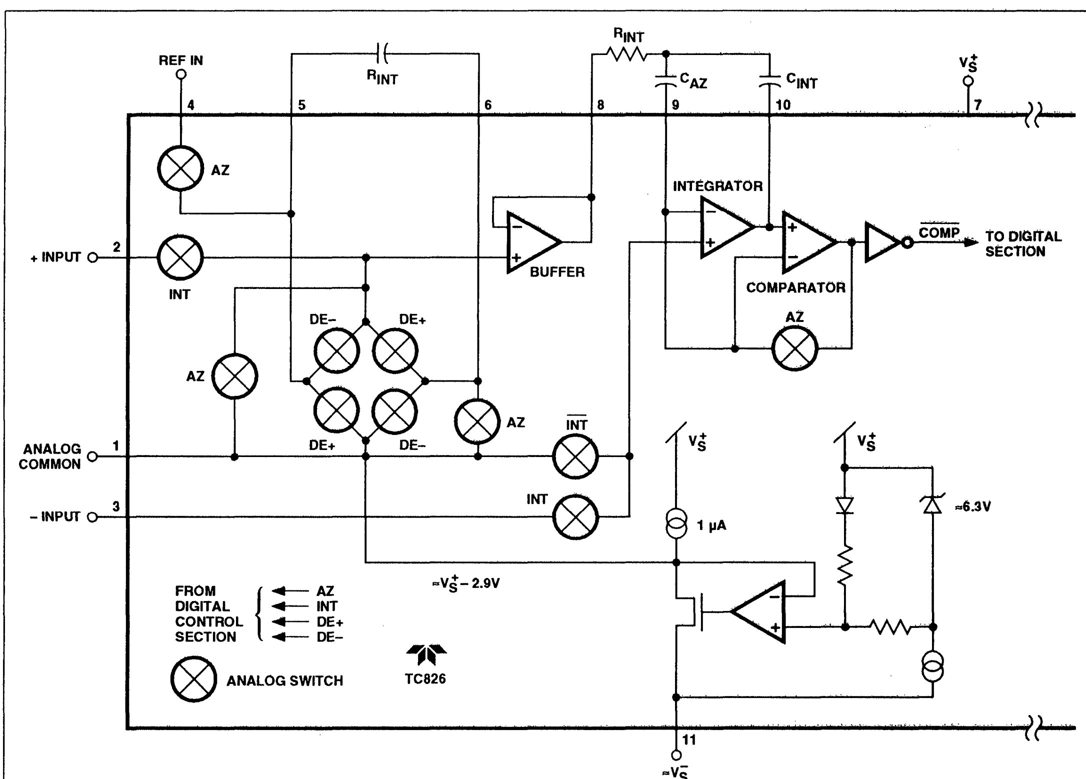


Figure 4 TC826 Analog Section

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, –IN should be tied to analog-common. This is the usual connection for battery operated systems. Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and system noise.

Reference Integrate Cycle

The final phase is reference integrate or deintegrate. – IN is internally connected to analog common and +IN is connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 40 counts. The digital reading displayed is:

$$20 = \frac{V_{IN}}{V_{REF}}$$

System Timing

The oscillator frequency is divided by 32 propr to clocking the internal counters. The three phase measurement cycle takes a total of 80 clock pulses. The 80 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 19 to 59 Counts
  For signals less than full-scale the auto-zero is assigned the unused reference integrate time period.
- Signal Integrate: 20 Counts
  This time period is fixed. The integration period is:

  $$T_{SI} = 20\left[\frac{32}{F_{OSC}}\right]$$

  Where F_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 41 Counts

Reference Voltage Selection

A full-scale reading requires the input signal be twice the reference voltage. The reference potential is measured between REF IN (Pin 4) and Analog-Common (Pin 1).

Required Full-Scale Voltage	V_{REF}
20 mV	10 mV
2V	1V

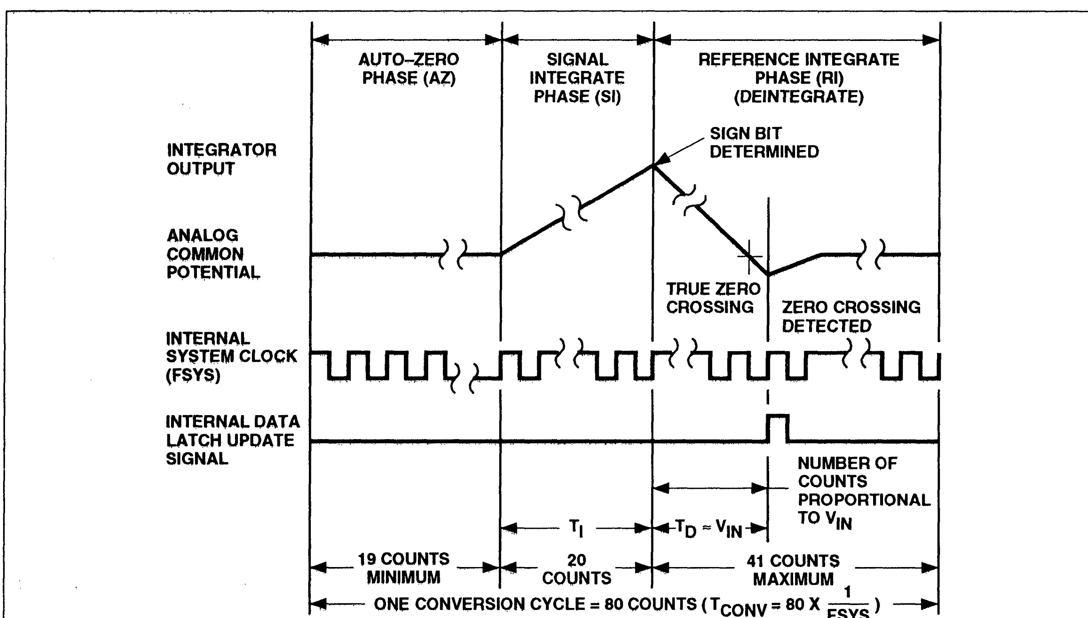


Figure 5 TC826 Conversion Has Three Phases

The internal voltage reference potential availabe at analog-common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7V. In applications where an externally generated reference voltage is desired refer to Figure 6.

The reference voltage is adjusted with a near full-scale input signal. Adjust for proper LCD display readout.

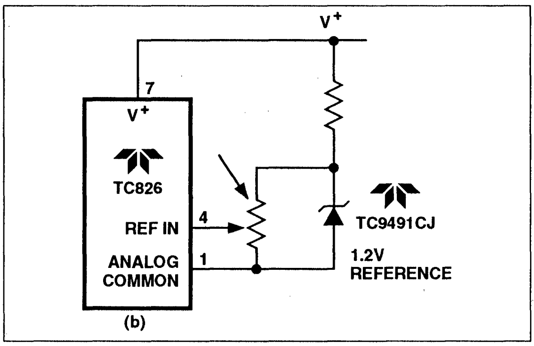


Figure 6 External Reference

Components Value Selection

Integrating Resistor (RINT)

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 1 μA drive durrent with minimal linearity error. RINT is easily calculated for a 1 μA full-scale current:

$$R_{INT} = \frac{\text{Full-Scale Input Voltage (V)}}{1 \times 10^{-6}} = \frac{VFS}{1 \times 10^{-6}}$$

Where VFS = Full-Scale Analog Input

Integrating Capacitor (CINT)

The integrating capacitor should be slected to maximize intgrator output swing. The integrator output will swing to within 0.4V of V_S^+ or V_S^- without saturating.

The integrating capacitor is easily calculated:

$$CINT = \frac{VFS}{RINT}\left(\frac{640}{FOSC \times VINT}\right)$$

Where : VINT = Integrator Swing
FOSC = Oscillator Frequency

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested.

Auto-Zero Capacitor (CAZ)

CAZ should be 2–3 times larger than the integration capacitor. A polypropylene capacitor is suggested. Typical values from 0.14 μF to 0.068 μF are satisfactory.

Reference Capacitor (CREF)

A 1 μF capacitor is suggested. Low leakage capacitors such as polypropylene are recommended.

Several capacitor/resistor combinations for common full-scale input conditions are given in Table 1.

Table 1 Suggested Component Values

Component	2V Full-Scale $V_{REF} \approx 1V$	200 mV Full-Scale $V_{REF} \approx 100$ mV	20 mV Full-Scale $V_{REF} \approx 10$ mV
R_{INT}	2 MΩ	200 kΩ	20 kΩ
C_{INT}	0.033 μF	0.033 μF	0.033 μF
C_{REF}	1 μF	1 μF	1 μF
C_{AZ}	0.068 μF	0.068 μF	0.14 μF
R_{OSC}	430 kΩ	430 kΩ	430 kΩ

NOTES: Approximately 5 conversions/second.

Differential Signal Inputs

The TC826 is designed with true differential inputs and accepts input signals within the input stage common–mode voltage range (VCM). The typical range is $V^+ - 1$ to $V^- + 1V$. Common–mode voltages are removed from the system when the TC826 operates from a battery or floating power source (Isolated from measured system) and –IN is connected to analog–common (V_{COM}).

In systems where common–mode rejection ratio minimizes error. Common–mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full–scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM}. For such applications, the integrator output swing can be reduced below the recommended 2V full–scale swing. The integrator output will swing within 0.3V of V_S^+ or V_S^- without increased linearity error.

Digital Section

The TC826 contains all the segment drivers necessary to drive a liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 256. A 430 kΩ osc gets the backplane frequency to approximately 55 Hz with a 5V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is 'OFF'. An out–of–phase segment drive signal causes the segment to be 'ON' or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment drive, –POL, is 'ON' for negative analog inputs. If +IN and –IN are reversed this indicator would reverse. The TC826 transfer function is shown in Figure 7.

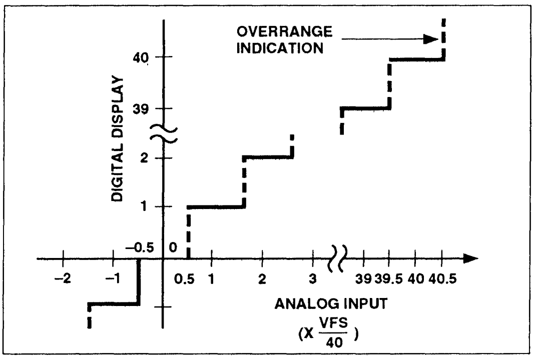


Figure 7 TC826 Transfer Function

BAR / $\overline{\text{DOT}}$ Input (Pin 58)

The BAR / $\overline{\text{DOT}}$ input allows the user to select the display format. The TC826 powers up in the BAR mode. Select the DOT display format by connecting BAR / $\overline{\text{DOT}}$ to the negative supply (Pin 11) through a 1 MΩ resistor.

$\overline{\text{HOLD}}$ Input (Pin 59)

The TC826 data ouput latches are not updated at the end of each conversion if $\overline{\text{HOLD}}$ is tied to the negative supply (Pin 11) through a 1 MΩ series resistor. The LCD display continously displays the previous conversion results.

The $\overline{\text{HOLD}}$ pin is normally pulled high by an internal pull-up.

$\overline{\text{TEST}}$ Input (Pin 59)

The TC826 enters a test mode with the $\overline{\text{TEST}}$ input connected to the negative supply (Pin 11). The connection must be made through a 1 MΩ resistor. The $\overline{\text{TEST}}$ input is normally internally pulled high. A low input sets the output data latch to all ones. The BAR display mode is set. The 41 LCD output segments (zero plus 40 data segments) and overrange annuniciator flash on and off at 1/4 the conversion rate. The polarity annunciator (POL–) segment will be on but not flashing

Overrange Display Operation (OR, Pin 56)

An out–of–range input signal will be indicated on the LCD display by the OR annunciator driver (Pin 56) becoming active.

In the BAR display format the 41 bar segments and the overrange annunciator, OR, will flash ON and OFF. The flash rate is on fourth the conversion rate (FOSC/2560).

In the DOT display mode, OR flashes and all other data segment drivers are off.

Polarity Indication (POL–Pin 57)

The TC826 converts and displays data for positive and negative input signals. The POL–LCD segment driver (Pin 57) is active for negative signals.

Oscillator Operation

The TC826 external oscillator frequency, FOSC, is set by resistor ROSC connected between pins 12 and 13. The oscillator frequency vs. resistance curve is shown in Figure 8.

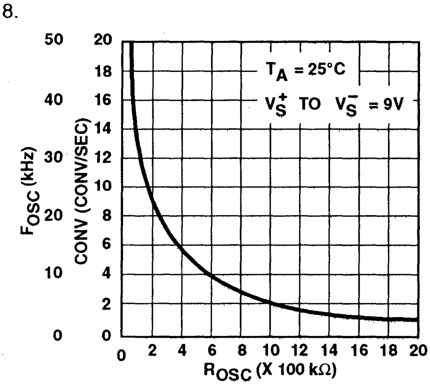


Figure 8 Oscillator Frequency vs. ROSC

FOSC is divided by 32 to provide an internal system clock, FYSY. Each conversion requires 80 internal clock cycles. The internal system clock is divided by 8 to provide the LCD backplane drive frequency. The display flash rate during an input out-of-range signal is set by dividing FSYS by 320. (See Figure 9.)

The internal oscillator may be bypassed by driving OSCI (Pin 12) with an external signal generator. OSC2 (Pin 13) should be left unconnected.

The oscillator should swing from V_S^+ to V_S^- in single supply operation (Figure 10A). In dual supply operation the signal should swing from power supply ground to V_S^+.

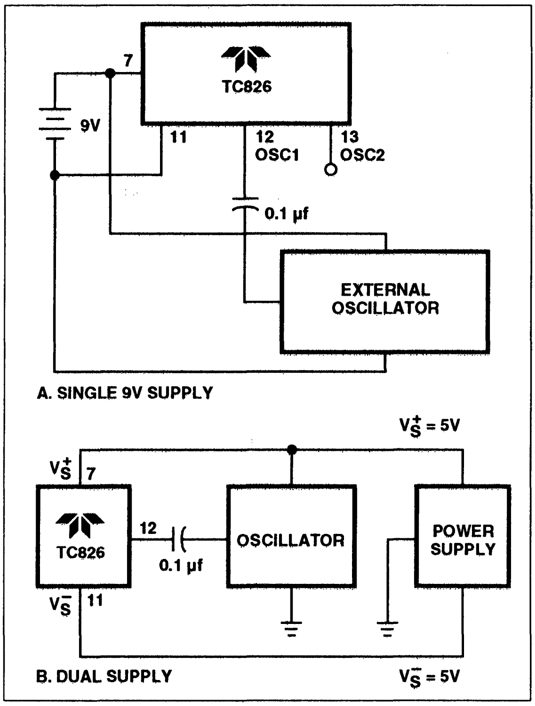


Figure 10 External Oscillator Connection

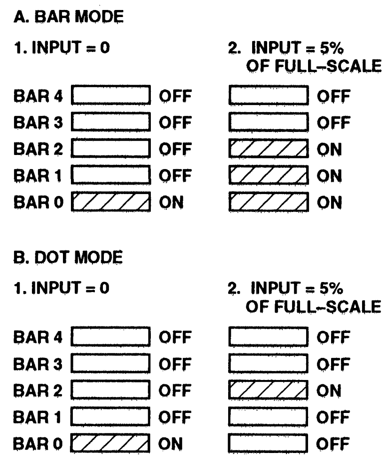


Figure 11 Disp;ay Option Formats

LCD Display Format

The input signal can be displayed in two formats (Figure 11). The BAR / $\overline{\text{DOT}}$ input (Pin 58) selects the format. The TC826 measurement cycle operates indentically for either mode.

BAR Format

The TC826 power-ups in the BAR mode. BAR / $\overline{\text{DOT}}$ is pulled high internally. This display format is similar to a thermometer display. All bars/LCD segments, including zero, below the bar/LCD segment equaling the input signal level are on. A half-scale input signal, for example, would be displayed with BAR 0 to BAR 20 on.

DOT Format

By connecting BAR / $\overline{\text{DOT}}$ to V_S^- through a 1 MΩ resistor the DOT mode is selected. Only the BAR LCD segment equaling the input signal is on. The zero segment is on for zero input.

This mode is useful for moving cursor or 'needle' applications.

LCD DISPLAYS

Most end products will use a custom LCD display for final production. Custom LCD displays are low cost and available from all manufacturers. The TC826 interfaces to non-multiplexed LCD displays. A backplane driver is included on chip.

To speed initial evaluation and prototype work a standard TC826 LCD display is available from Varitronix.

Varitronix Ltd.
9/F Linen House, 61-63, King Yip Street
Kwun Tjong, Hong Kong
Telex: 36643 VTRAX HX

USA Office:
VL Electronics Inc.
3161 Los Feliz Blvd., Suite 303
Los Angeles, CA 90039
Tel: 213/661-8883
Telex: 821554

- Part No.: VBG412-1 (Pin Connectors)
- Part No.: VBG412-2 (Elastomer Connectors)

Other standard LCD displays suitable for development work are available in both linear and circular formats. One manufacturer is:

UCE Inc.
24 Fitch Street
Norwalk, CT 06855
Tel: 203/838-7509

- Part No. 5040: 50 segment circular display with 3 didgit numeric scale.
- Part No. 5020: 50 segment linear display.

LCD BACKPLANE DRIVER (PIN 14)

Additional drive electronics is not required to interface the TC826 to an LCD display. The TC826 has an on-chip backplane generator and driver. The backplane frequency is:

$$FBP = FOSC/256$$

Figure 12 gives typical backplane driver rise/fall time v. backplane capacitance.

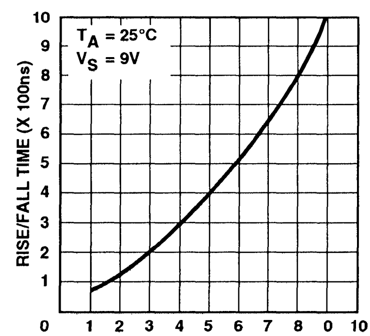


Figure 12 Backplane Driver Rise/Fall Time vs. Capacitance

FLAT PACKAGE SOCKET

Sockets suitable for prototype work are available. A USA source is:

Nepenthe Distribution
2471 East Bayshore, Suite 520
Palo Alto, CA 94303
Tel: 415/856-9332
Telex: 910/373-2060

'BQ' Socket Part No.: IC51-064-042 BQ

NOTES

TELEDYNE COMPONENTS

1

PERSONAL COMPUTER DATA ACQUISITION ADC

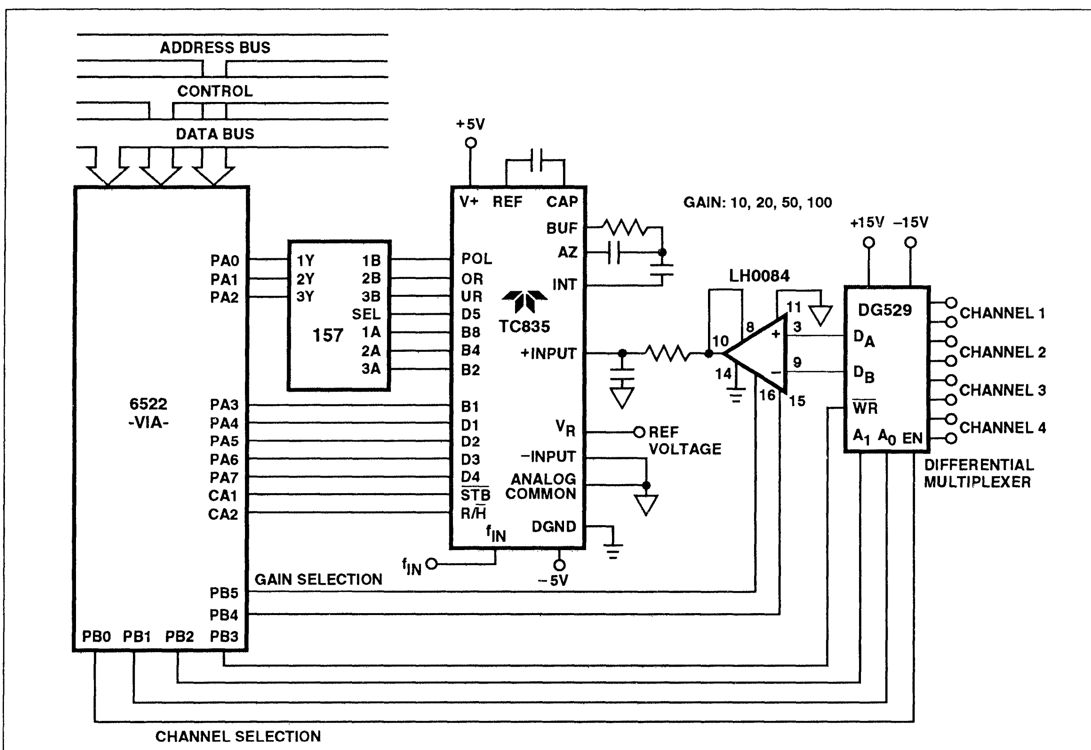
FEATURES

- Guaranteed 200 kHz Operation
- Guaranteed Zero Reading for 0V Input
- Input Sensitivity .... 100 μV
- Multiplexed BCD Data Output
- No Sample and Hold Required
- UART and Microprocessor Interface
- Blinking Display Indicates Overrange
- Control Outputs for Auto-Ranging
- Available in PLCC and Surface-Mount Packages
- Low-Power CMOS Technology
- Pin Compatible With TC7135, ICL7135, MAX7135 and SI7135
- Single 5V Operation With TC7660 DC-to-DC Converter
- Extended Temperature Range Operation .... –40°C to +85°C

APPLICATIONS

- Personal Computer Data Acquisition
- Scales
- Panel Meters
- Digital Pressure Meters
- Chemical Concentration
- Temperature
- Process Variable Measurement
  - — Flow Rate
  - — Temperature
  - — Speed
  - — Concentration
- Electrostatic Field Measurement
- Voltage, Resistance, Current Measurements
- Light Intensity
- Toxic Level Measurement
- HP-IL Bus Instrumentation

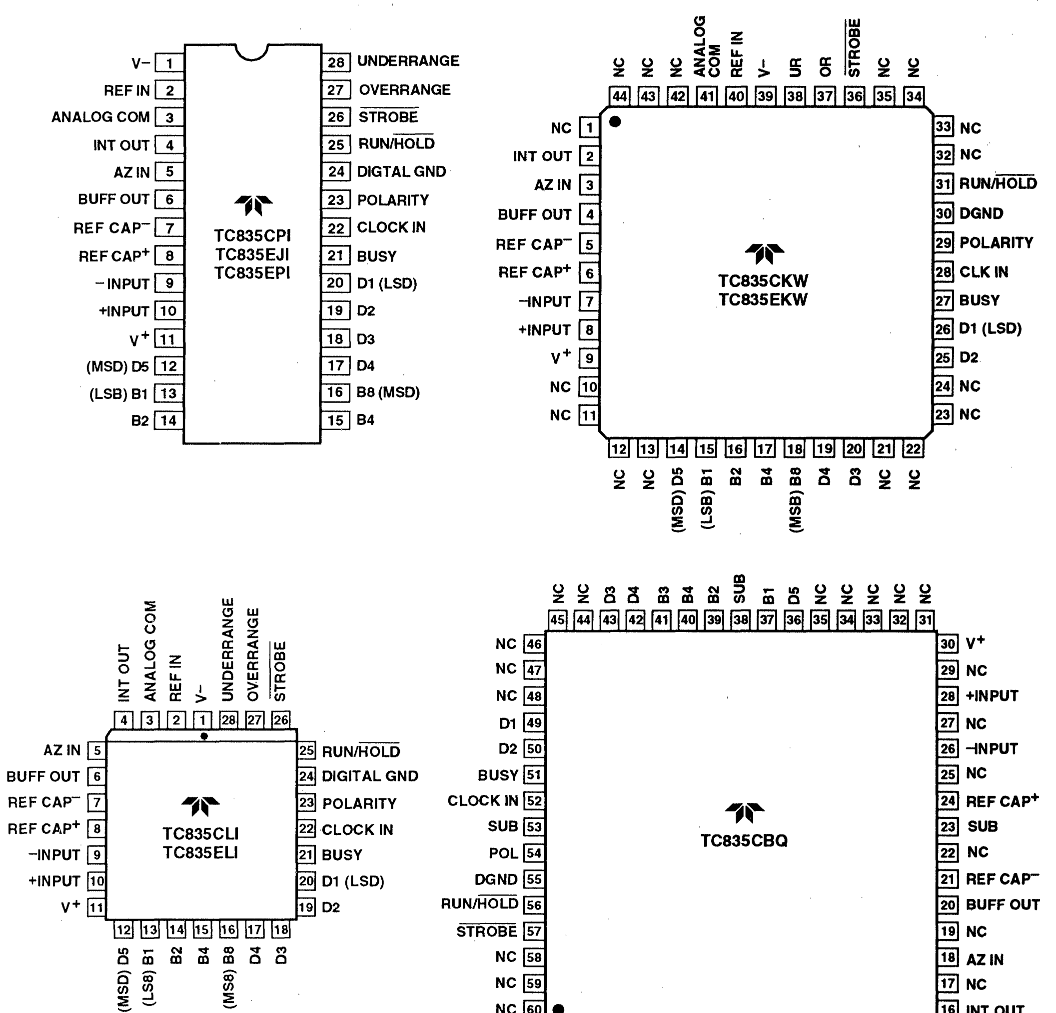
TYPICAL APPLICATION



1095-1

TC835

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

PERSONAL COMPUTER DATA ACQUISITION ADC

TC835

GENERAL DESCRIPTION

The TC835 is a low-power, 4-1/2 digit (0.005% resolution), BCD analog-to-digital converter (ADC) that has been characterized for 200 kHz clock rate operation. The five conversions per second rate is nearly twice as fast as the ICL7135 or TC7135.

The multiplexed BCD data output is perfect for interfacing to personal computers. The low-cost, greater than 14-bit high-resolution, and 100 μV sensitivity makes the TC835 the most cost-effective data converter available today.

The TC835 (like the TC7135) does not use the external diode-resistor roll-over error compensation circuits required by the ICL7135. This improves circuit density and simplifies circuit board layout.

The device incorporates "integrator output zero" and "auto-zero" phases on each conversion cycle, guaranteeing a stable zero output for 0V input, even when operated at the higher clock rate.

Microprocessor-based data acquisition systems are supported by the BUSY and $\overline{\text{STROBE}}$ outputs, along with the RUN/$\overline{\text{HOLD}}$ input of the TC835. The overrange, underrange, busy, and run/hold control functions and multiplexed BCD data outputs make the TC835 the ideal converter for μP-based scales and measurement systems and intelligent panel meters. (See Application Notes 16 and 17 for microprocessor interface techniques.)

The TC835 interfaces with full-function LCD and LED display decoder/drivers (TC7211A or TC7212A). The UNDERRANGE and OVERRANGE outputs may be used to implement an auto-ranging scheme or special display functions.

This device is pin compatible with, and incorporates all the features of, the popular TC7135 and ICL7135. The performance of existing designs may be upgraded to faster conversion rates by lowering the value of the integrating capacitor and increasing the clock frequency (see "Component Selection").

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC835CPI	28-Pin Plastic	0°C to +70°C
TC835CKW	44-Pin Flat	0°C to +70°C
TC835CLI	28-Pin PLCC	0°C to +70°C
TC835CBQ	60-Pin Flat	0°C to +70°C
TC835EJI	28-Pin CerDIP	–40°C to +85°C
TC835EPI	28-Pin Plastic	–40°C to +85°C
TC835EKW	44-Pin Flat	–40°C to +85°C
TC835ELI	28-Pin PLCC	–40°C to +85°C

NOTE: Tape and reel available for 44-pin flat and 28-pin PLCC packages.

TC835

ABSOLUTE MAXIMUM RATINGS (Note 1)

Positive Supply Voltage .... +6V
Negative Supply Voltage .... –9V
Analog Input Voltage (Pin 9 or 10) .... V^+ to V^- (Note 2)
Reference Input Voltage (Pin 2) .... V^+ to V^-
Clock Input Voltage .... 0V to V^+
Operating Temperature Range .... 0°C to +70°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Package Power Dissipation
CerDIP (J) 1W
Plastic (P) 0.8W

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, f_{CLOCK} = 200 kHz, V^+ = +5V, V^- = –5V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog						
	Display Reading With Zero Volt Input	Notes 3 and 4	–0.0000	±0.0000	+0.0000	Display Reading
TC_Z	Zero Reading Temperature Coefficient	V_{IN} = 0V Note 5	—	0.5	2	µV/°C
TC_{FS}	Full-Scale Temperature Coefficient	V_{IN} = 2V Notes 5 and 6	—	—	5	ppm/°C
NL	Nonlinearity Error	Note 7	—	0.5	1	Count
DNL	Differential Linearity Error	Note 7	—	0.01	—	LSB
	Display Reading in Ratiometric Operation	$V_{IN} = V_{REF}$ Note 3	+0.9997	+0.9998	+1.0000	Display Reading
±FSE	± Full-Scale Symmetry Error (Roll-Over Error)	$-V_{IN} = +V_{IN}$ Note 8	—	0.5	1	Count
I_{IN}	Input Leakage Current	Note 4	—	1	10	pA
e_N	Noise	Peak-to-Peak Value Not Exceeded 95% of Time	—	15	—	μV_{P-P}
Digital						
I_{IL}	Input Low Current	V_{IN} = 0V	—	10	100	µA
I_{IH}	Input High Current	V_{IN} = +5V	—	0.08	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	—	0.2	0.4	V
V_{OH}	Output High Voltage					
	B_1, B_2, B_4, B_8, D_1–D_5	I_{OH} = 1 mA	2.4	4.4	5	V
	Busy, Polarity, Overrange, Underrange, Strobe	I_{OH} = 10 µA	4.9	4.99	5	V
f_{CLK}	Clock Frequency	Note 10	0	200	1200	kHz
Power Supply						
V^+	Positive Supply Voltage		4	5	6	V
V^-	Negative Supply Voltage		–3	–5	–8	V
I^+	Positive Supply Current	f_{CLK} = 0 Hz	—	1	3	mA
I^-	Negative Supply Current	f_{CLK} = 0 Hz	—	0.7	3	mA
PD	Power Dissipation	f_{CLK} = 0 Hz	—	8.5	30	mW

NOTES:
1. Functional operation is not implied.
2. Limit input current to under 100 µA if input voltages exceed supply voltage.
3. Full-scale voltage = 2V.
4. V_{IN} = 0V.
5. 0°C ≤ T_A ≤ +70°C.
6. External reference temperature coefficient less than 0.01 ppm/°C.
7. –2V ≤ V_{IN} ≤ +2v. Error of reading from best fit straight line.
8. $|V_{IN}|$ = 1.9959.
9. Test circuit shown in Figure 1.
10. Specification related to clock frequency range over which the TC835 correctly performs its various functions. Increased errors result at higher operating frequencies.

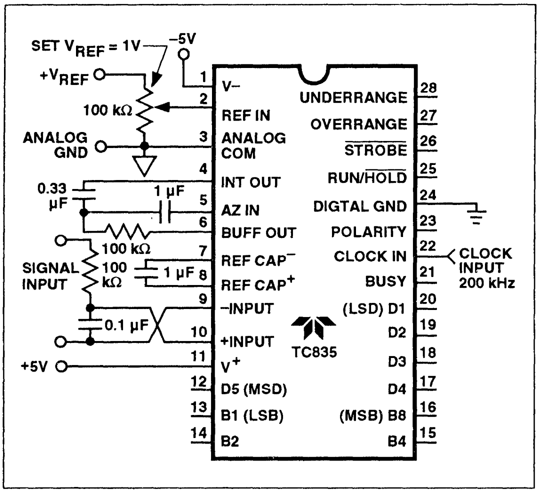


Figure 1 Test Circuit

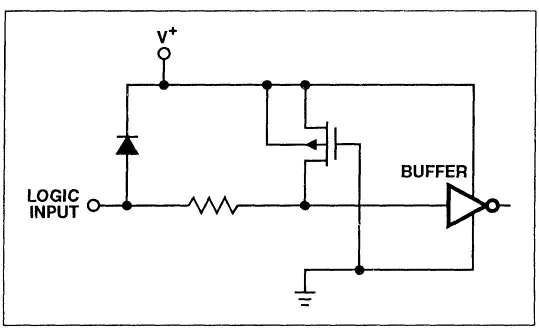


Figure 2 Digital Logic Input

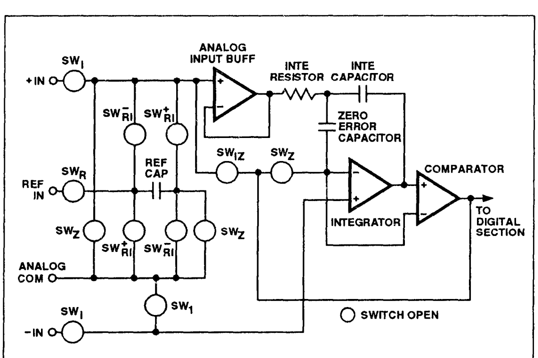


Figure 3A Analog Circuit Function Diagram

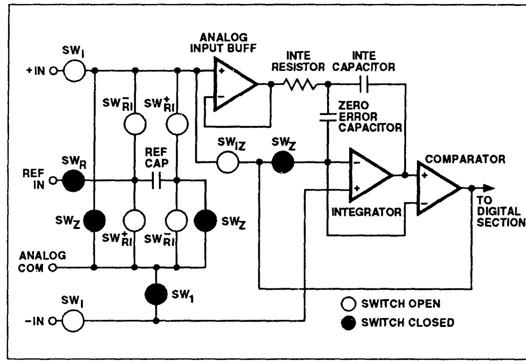


Figure 3B System Zero Phase

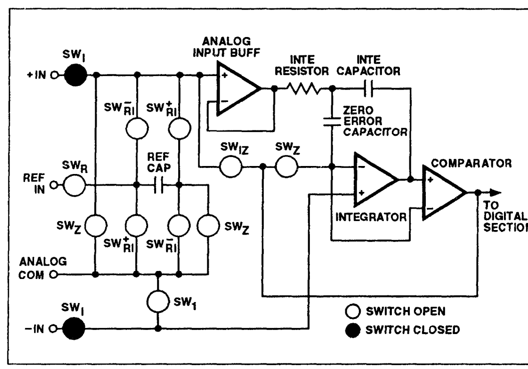


Figure 3C Input Signal Integration Phase

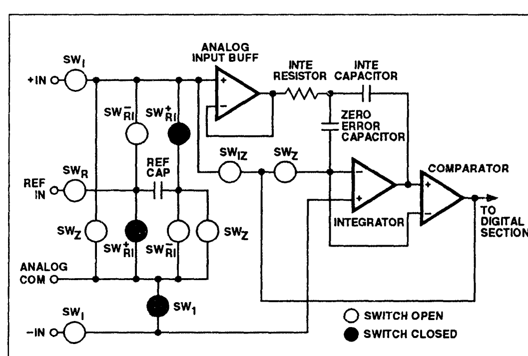


Figure 3D Reference Voltage Integration Cycle

TC835

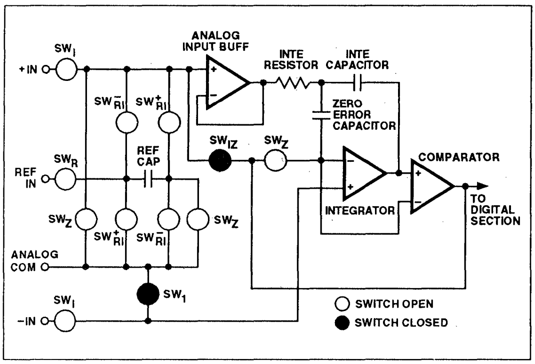


Figure 3E Integrator Output Zero Phase

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC835 is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following the detailed TC835 operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration
(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right].$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated, or averaged, to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. (See Figure 4.)

TC835 Operational Theory

The TC835 incorporates a system zero phase and integrator output voltage zero phase to the normal two-phase dual-slope measurement cycle. Reduced system errors, fewer calibration steps, and a shorter overrange recovery time result.

The TC835 measurement cycle contains four phases:

(1) System zero
(2) Analog input signal integration
(3) Reference voltage integration
(4) Integrator output zero

Internal analog gate status for each phase is shown in Table I.

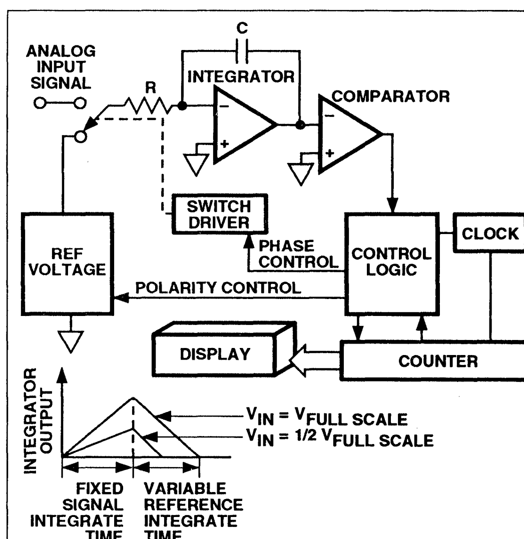


Figure 4 Basic Dual-Slope Converter

Table I. Internal Analog Gate Status

Conversion Cycle Phase	Internal Analog Gate Status SW_I	SW_{RI}^{+}	SW_{RI}^{-}	SW_Z	SW_R	SW_1	SW_{IZ}	Reference Schematic
System Zero				Closed	Closed	Closed		3A
Input Signal Integration	Closed							3B
Reference Voltage Integration		Closed*				Closed		3C
Integrator Output Zero						Closed	Closed	3D

***NOTE:** Assumes a positive polarity input signal. SW_{RI}^{-} would be closed for a negative input signal.

System Zero (Figure 3B)

During this phase, errors due to buffer, integrator, and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to ANALOG COMMON. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator, and comparator offset voltages.

Analog Input Signal Integration (Figure 3C)

The TC835 integrates the differential voltage between the +INPUT and −INPUT pins. The differential voltage must be within the device common-mode range; −1V from either supply rail, typically.

The input signal polarity is determined at the end of this phase.

Reference Voltage Integration (Figure 3D)

The previously-charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The digital reading displayed is:

$$\text{Reading} = 10{,}000 \left[\frac{\text{Differential Input}}{V_{REF}}\right].$$

Integrator Output Zero (Figure 3E)

This phase guarantees the integrator output is at 0V when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists, the phase is extended to 6200 clock cycles.

Analog Section Functional Description

Differential Inputs
(+INPUT, Pin 10 and −INPUT, Pin 9)

The TC835 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.5V below the positive supply to 1V above the negative supply. Within this common-mode voltage range, an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full-scale swing, with some loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

ANALOG COMMON Input (Pin 3)

ANALOG COMMON is used as the −INPUT return during auto-zero and deintegrate. If −INPUT is different from ANALOG COMMON, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, −INPUT will be set at a fixed, known voltage (power supply common, for instance). In this application, ANALOG COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to ANALOG COMMON.

REFERENCE Voltage Input (REF IN, Pin 2)

The REF IN input must be a positive voltage with respect to ANALOG COMMON. Two reference voltage circuits are shown in Figure 5.

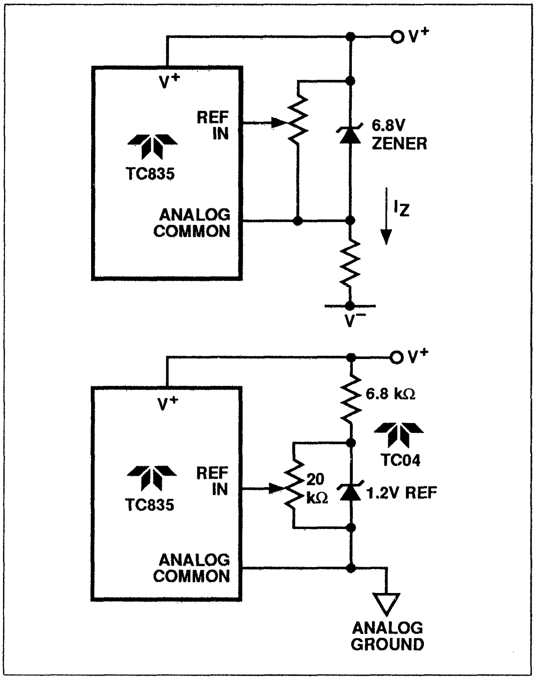


Figure 5 Using an External Reference

Digital Section Functional Description

The major digital subsystems within the TC835 are illustrated in Figure 6, with timing relationships shown in Figure 7. The multiplexed BCD output data can be displayed on LCD or LED display with the TC7211A (LCD) or TC7212A (LED) 4-digit display drivers.

The digital section is best described through a discussion of the control signals and data outputs.

RUN/$\overline{\text{HOLD}}$ Input (Pin 25)

When left open, this pin assumes a logic "1" level. With a R/$\overline{\text{H}}$ = 1, the TC835 performs conversions continuously, with a new measurement cycle beginning every 40,002 clock pulses.

When R/$\overline{\text{H}}$ changes to a logic "0," the measurement cycle in progress will be completed, and data held and displayed as long as the logic "0" condition exists.

A positive pulse (>300 ns) at R/$\overline{\text{H}}$ initiates a new measurement cycle. The measurement cycle in progress when R/$\overline{\text{H}}$ initially assumed the logic "0" state must be completed before the positive pulse can be recognized as a single conversion run command.

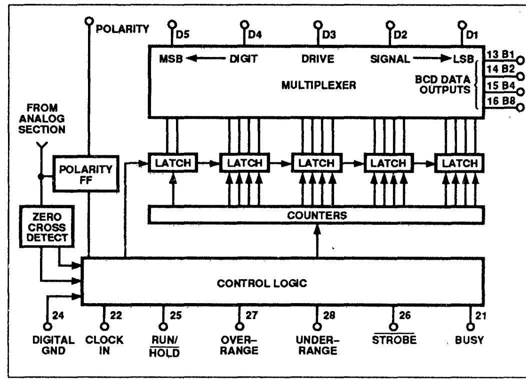


Figure 6 Digital Section Functional Diagram

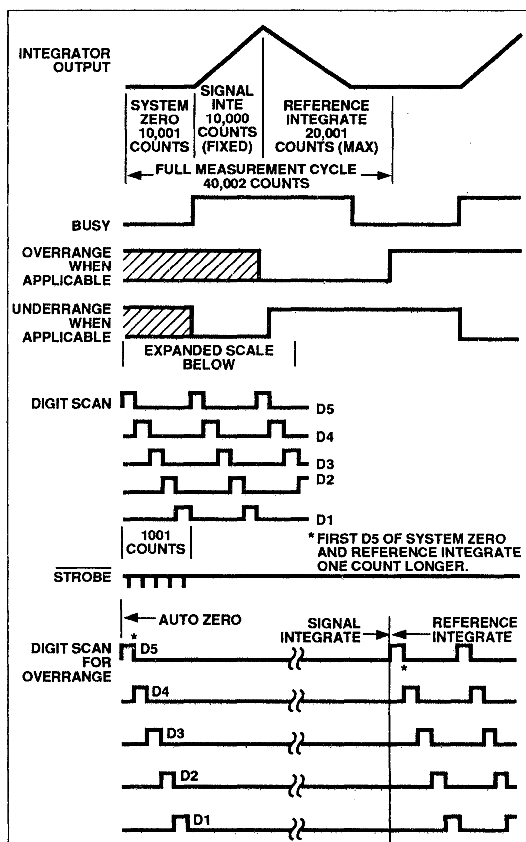


Figure 7 Timing Diagrams for Outputs

The new measurement cycle begins with a 10,001-count auto-zero phase. At the end of this phase the busy signal goes high.

$\overline{\text{STROBE}}$ Output (Pin 26)

During the measurement cycle, the $\overline{\text{STROBE}}$ control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_5, Figure 8).

D_5 (MSD) goes high for 201 counts when the measurement cycles end. In the center of the D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first $\overline{\text{STROBE}}$ occurs for one-half clock pulse. After the D_5 digit strobe, D_4 goes high for 200 clock pulses. The $\overline{\text{STROBE}}$ goes low 100 clock pulses after D_4 goes high. This continues through the D_1 digit drive pulse.

The digit drive signals will continue to permit display scanning. $\overline{\text{STROBE}}$ pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active low $\overline{\text{STROBE}}$ pulses aid BCD data transfer to UARTs, processors and external latches. (See Application Note 16.)

BUSY Output (Pin 21)

At the beginning of the signal-integration phase, BUSY goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to the logic "0" state after the measurement cycle ends in an overrange condition. The internal display latches are loaded during the first clock pulse after BUSY, and are latched at the clock pulse end. The BUSY signal does not go high at the beginning of the measurement cycle, which starts with the auto-zero cycle.

OVERRANGE Output (Pin 27)

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses, the OVERRANGE output is set to a logic "1." The overrange output register is set when BUSY goes low, and is reset at the beginning of the next reference-integration phase.

UNDERRANGE Output (Pin 28)

If the output count is 9% of full scale or less (≤1800 counts), the underrange register bit is set at the end of BUSY. The bit is set low at the next signal-integration phase.

POLARITY Output (Pin 23)

A positive input is registered by a logic "1" polarity signal. The polarity bit is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

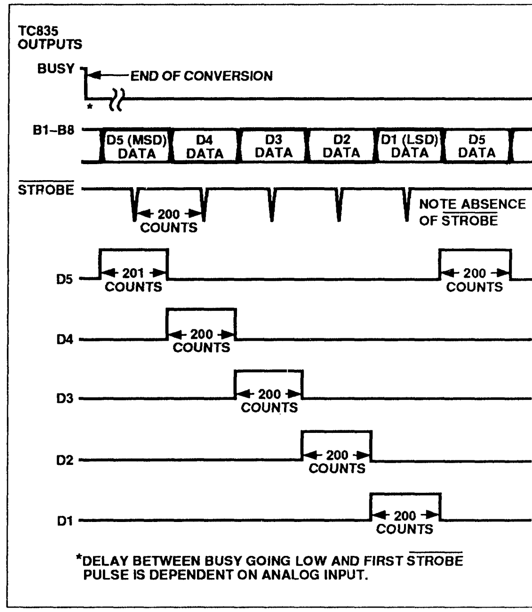


Figure 8 Strobe Signal Pulses Low Five Times per Conversion

The polarity bit is valid even for a zero reading. Signals less than the converter's LSB will have the signal polarity determined correctly. This is useful in null applications.

DIGIT Drive Outputs (Pins 12, 17, 18, 19 and 20)

Digit drive signals are positive-going signals. The scan sequence is D_5 to D_1. All positive pulses are 200 clock pulses wide, except D_5, which is 201 clock pulses wide.

All five digits are scanned continuously, unless an overrange condition occurs. In an overrange condition, all digit drives are held low from the final $\overline{\text{STROBE}}$ pulse until the beginning of the next reference-integrate phase. The scanning sequence is then repeated. This provides a blinking visual display indication.

BCD Data Outputs (Pins 13, 14, 15 and 16)

The binary coded decimal (BCD) bits B_8, B_4, B_2, B_1, are positive-true logic signals. The data bits become active simultaneously with the digit drive signals. In an overrange condition, all data bits are at a logic "0" state.

APPLICATIONS INFORMATION

Component Value Selection

The integrating resistor is determined by the full-scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage, with 100 μA of quiescent current. A 20 μA drive current gives negligible linearity errors. Values of 5 μA to 40 μA give good results. The exact value of an integrating resistor for a 20 μA current is easily calculated.

$$R_{INT} = \frac{\text{full-scale voltage}}{20\ \mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing that ensures the tolerance build-up will not saturate the integrator swing (approximately 0.3V from either supply). For ±5V supplies and ANALOG COMMON tied to supply ground, a ±3.5V to ±4V full-scale integrator swing is adequate. A 0.10 μF to 0.47 μF is recommended. In general, the value of C_{INT} is given by:

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\ \mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent rollover or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half-scale 0.9999. any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitors

The size of the auto-zero capacitor has some influence on the noise of the system. A large capacitor reduces the noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference capacitor and auto-zero capacitor are only important at power-on, or when the circuit is recovering from an overload. Smaller or cheaper capacitors can be used if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high-quality reference be used where high-accuracy absolute measurements are being made. Suitable references are:

Part Type	Manufacturer
TC04A	Teledyne Components
TC8069	

Conversion Timing

Line Frequency Rejection

A signal integration period at a multiple of the 60 Hz line frequency will maximize 60 Hz "line noise" rejection.

A 200 kHz clock frequency will reject 60 Hz and 400 Hz noise. This corresponds to five readings per second.

Conversion Rate vs Clock Frequency

Oscillator Frequency (kHz)	Conversion Rate (Conv/Sec)
100	2.5
120	3
200	5
300	7.5
400	10
800	20
1200	30

Oscillator Frequency (kHz)	Line Frequency Rejection 60 Hz	50 Hz	400 Hz
50.000	•	•	•
53.333	—	—	•
66.667	•	—	•
80.000	—	—	•
83.333	—	•	•
100.000	•	•	•
125.000	—	•	•
133.333	—	—	•
166.667	—	—	•
200.000	•	—	•
250.000	—	•	•

The conversion rate is easily calculated:

$$\text{Conversion Rate (Readings 1/sec)} = \frac{\text{Clock Frequency (Hz)}}{4000}$$

Power Supplies and Grounds

Power Supplies

The TC835 is designed to work from ±5V supplies. For single +5V operation, a TC7660 can provide a –5V supply.

Grounding

Systems should use separate digital and analog ground systems to avoid loss of accuracy.

Displays and Driver Circuits

Teledyne Components manufactures two display decoder/driver circuits to interface the TC835 to an LCD or LED display. Each drive has 28 outputs for driving four 7-segment digit displays.

Device	Package	Description
TC7211AIPL	40-Pin Epoxy	4-Digit LCD Driver/Decoder
TC7212AIPL	40-Pin Epoxy	4-Digit LED Driver/Decoder

Several sources exist for LCD and LED display:

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Rd. Palo Alto, CA 94304	LED
Litronix, Inc.	19000 Homestead Rd. Cupertino, CA 94010	LED
AND	770 Airport Blvd. Burlingame, CA 94010	LCD and LED
Epson America, Inc.	3415 Kanhi Kawa St. Torrence, CA 90505	LCD

High-Speed Operation

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 µs delay, and at a clock frequency of 200 kHz (5 µs period), half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50 µV input, 1 to 2 with 150 µV, 2 to 3 at 250 µV, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 200 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the nonlinearity and noise do not increase substantially with frequency, clock rates of up to ~1 MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 200 kHz without this error, however, by using a low-value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second-order breaks will cause significant nonlinearities in the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

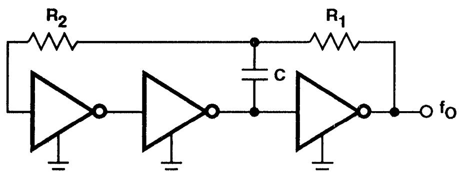
Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of the reference integrate (deintegrate) phase. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto-zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate, so that true ratiometric readings result.

TC835

TYPICAL APPLICATION DIAGRAMS

RC Oscillator Circuit



GATES ARE 74C04

1. $f_O = \dfrac{1}{2\,C(0.41\,R_P + 0.7\,R_1)}$, $R_P = \dfrac{R_1\,R_2}{R_1 + R_2}$

   a. If $R_1 = R_2 = R_1$, $f \cong 0.55/RC$

   b. If $R_2 >> R_1$, $f \cong 0.45/R_1C$

   c. If $R_2 >> R_1$, $f \cong 0.72/R_1C$

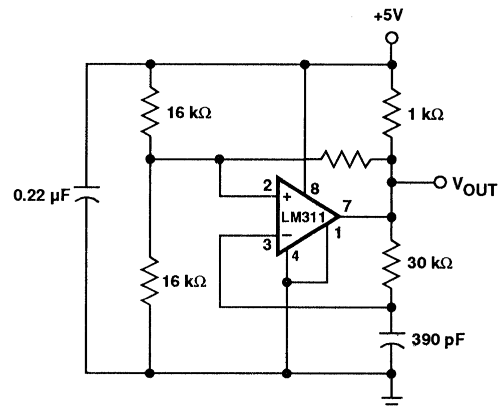
2. Examples:

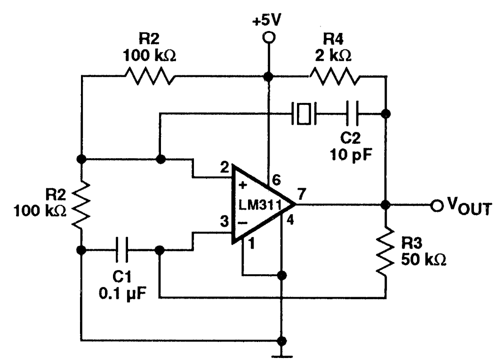
   a. $f = 120$ kHz, $C = 420$ pF
      $R_1 = R_2 \approx 10.9$ kΩ

   b. $f = 120$ kHz, $C = 420$ pF, $R_2 = 50$ kΩ
      $R_1 = 8.93$ kΩ

   c. $f = 120$ kHz, $C = 220$ pF, $R_2 = 5$ kΩ
      $R_1 = 27.3$ kΩ

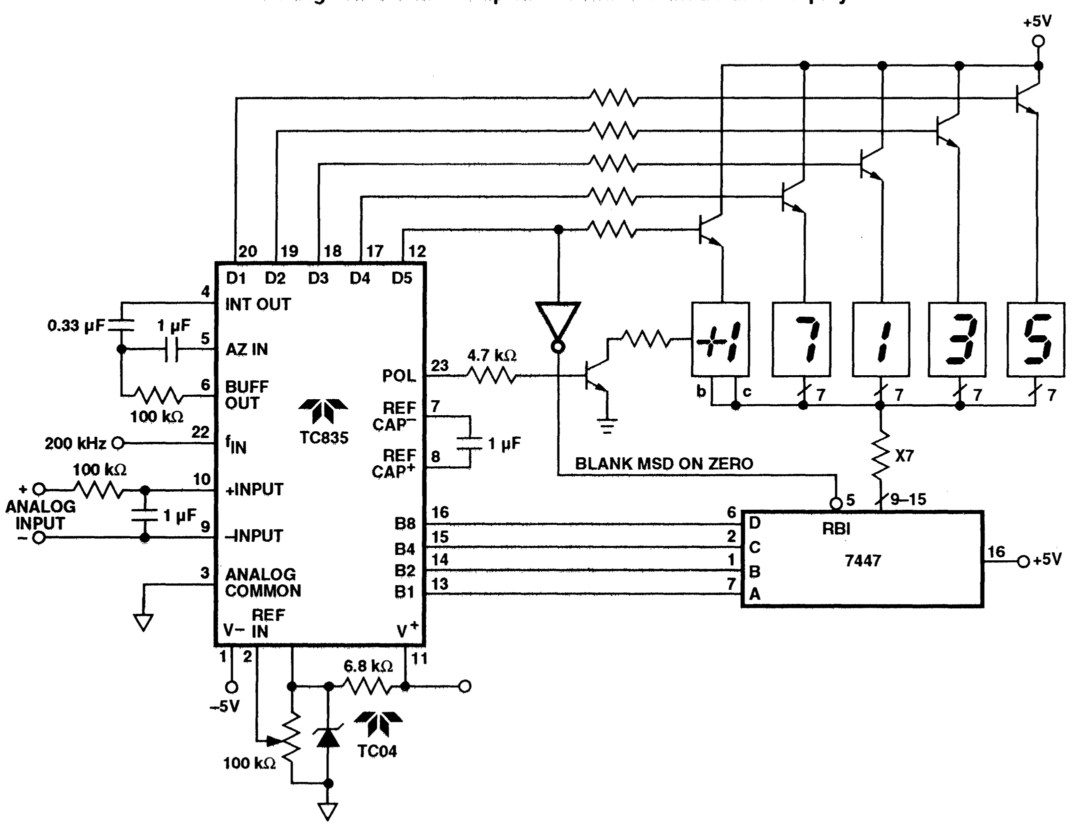
Comparator Clock Circuits





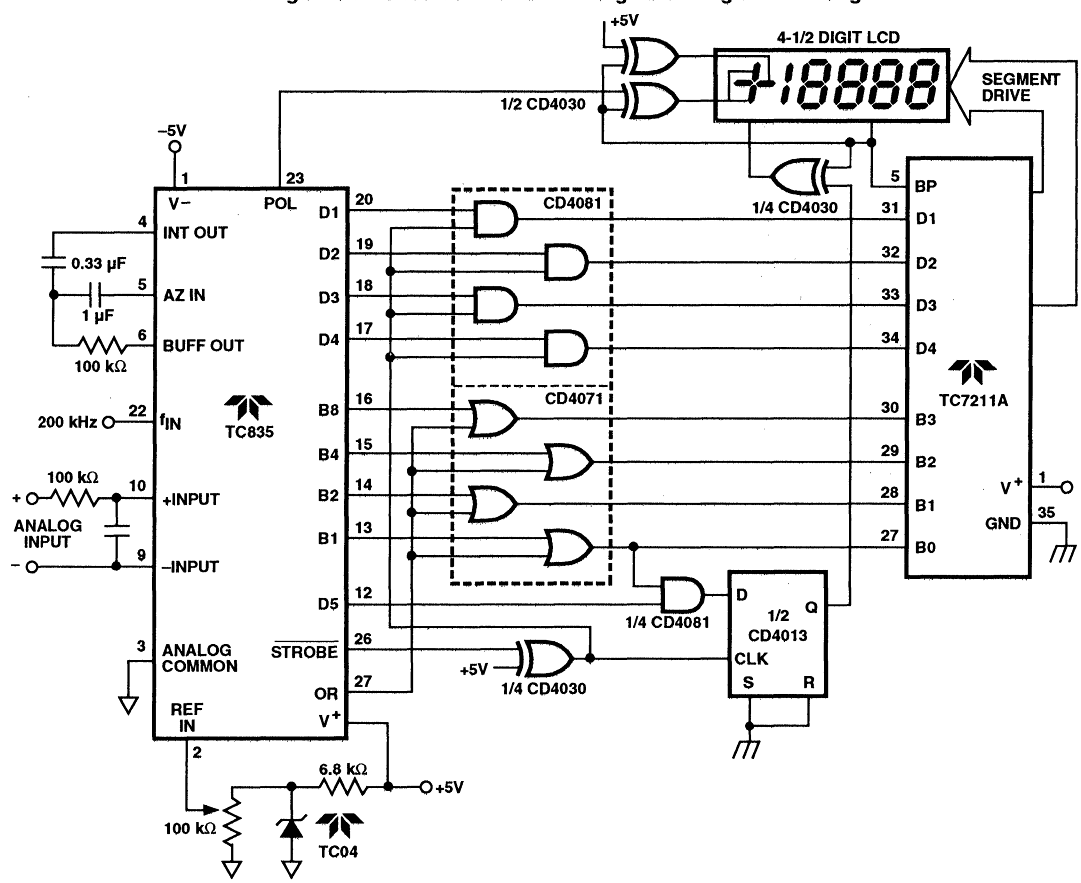
TYPICAL APPLICATIONS DIAGRAMS (Cont.)

4-1/2 Digit ADC With Multiplexed Common Anode LED Display



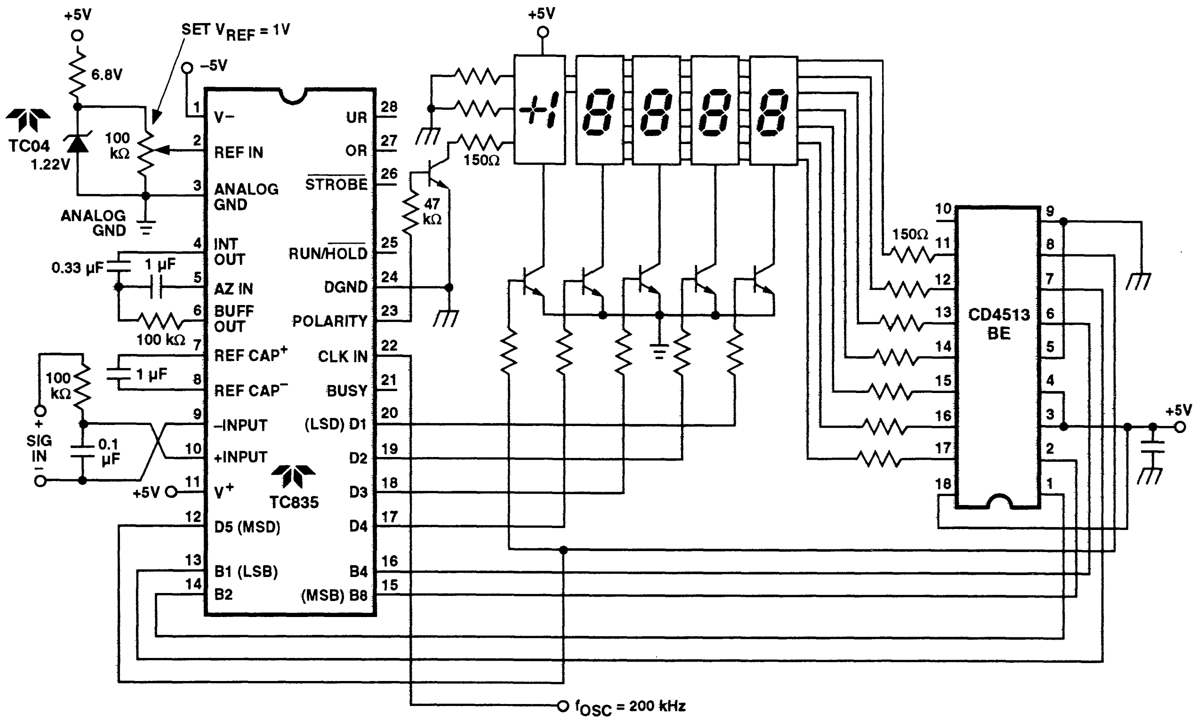
TYPICAL APPLICATIONS DIAGRAMS (Cont.)

4-1/2 Digit ADC Interfaced to LCD With Digit Blanking on Overrange



TYPICAL APPLICATIONS DIAGRAMS (Cont.)

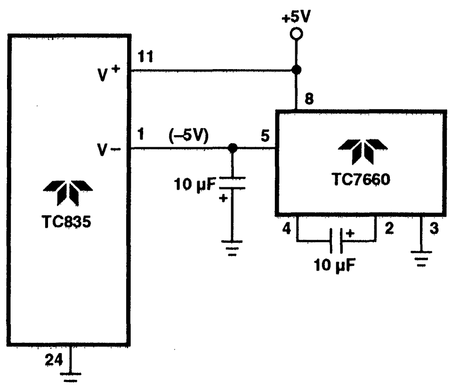
4-1/2 Digit ADC with Multiplexed Common Cathode LED Display



TC835

TYPICAL APPLICATIONS DIAGRAMS (Cont.)

Negative Supply Voltage Generator



TELEDYNE COMPONENTS

TC7106/7106A
TC7107/7107A

3-1/2 DIGIT A/D CONVERTER

FEATURES

- Internal Reference with Low Temperature Drift .... 20 ppm/°C Typical
  50 ppm/°C Maximum
- Drives LCD (TC7106) or LED (TC7107) Display Directly
- Guaranteed Zero Reading With Zero Input
- Low Noise for Stable Display
- Auto-Zero Cycle Eliminates Need for Zero Adjustment
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TC7106A)
- High Impedance CMOS Differential Inputs .... $10^{12}\Omega$
- Differential Reference Inputs Simplify Ratiometric Measurements
- Low Power Operation .... 10 mW
- Available in 60-Pin Plastic Flat Package

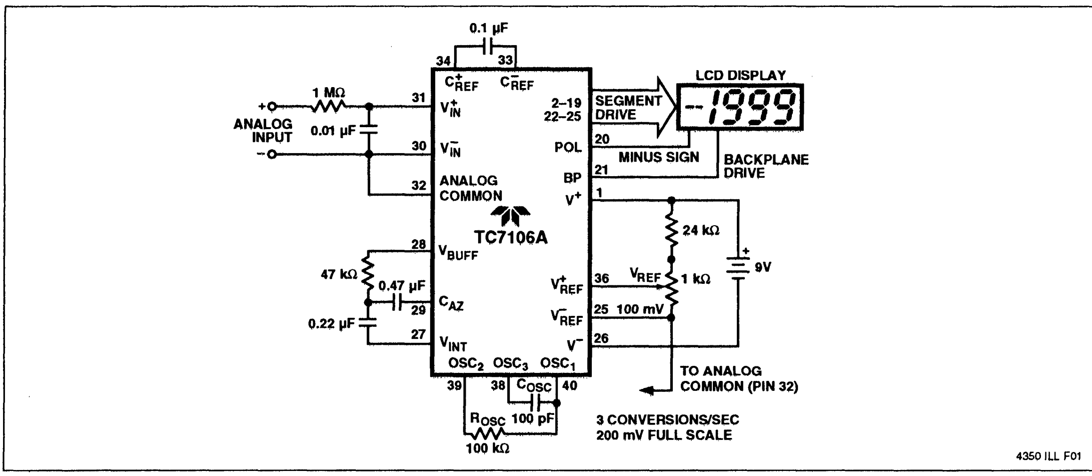


Figure 1 TC7106A Typical Operating Circuit

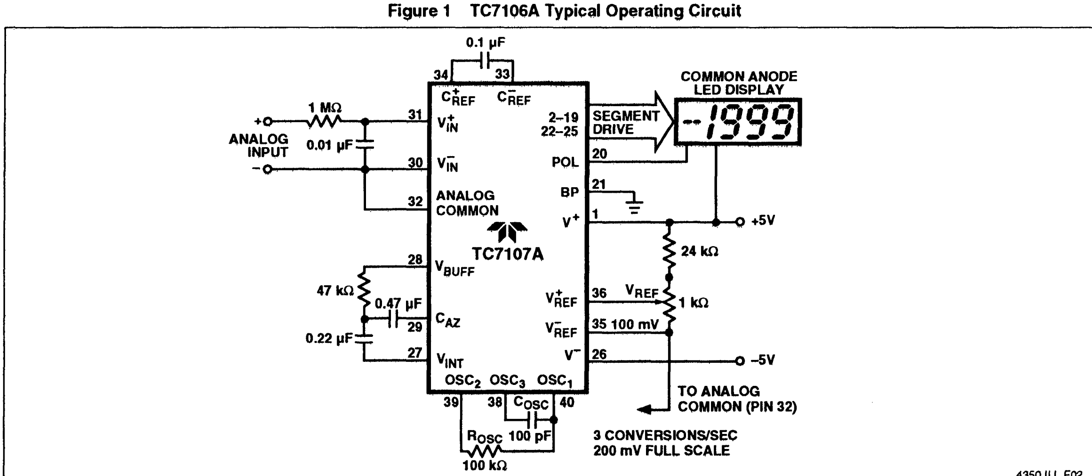


Figure 2 TC7107A Typical Operating Circuit

TC7106/7106A
TC7107/7107A

GENERAL DESCRIPTION

The TC7106A and TC7107A 3-1/2 digit direct display drive analog-to-digital converters allow existing 7106/7107 based systems to be upgraded. Each device offers a precision internal voltage reference featuring a 20 ppm/°C maximum temperature drift coefficient. This represents a 4 to 7 times improvement over similar 3-1/2 digit converters. Existing 7106 and 7107 based systems may be upgraded without changing external passive component values. The need for a costly, space consuming external reference is removed. The TC7107A drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment. A low cost, high resolution indicating meter requires only a display, four resistors, and four capacitors. The TC7106A low power drain and 9 V battery operation make it suitable for portable applications.

The TC7106A/TC7107A reduces linearity error to less than 1 count. Rollover error—the difference in readings for equal magnitude but opposite polarity input signals—is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

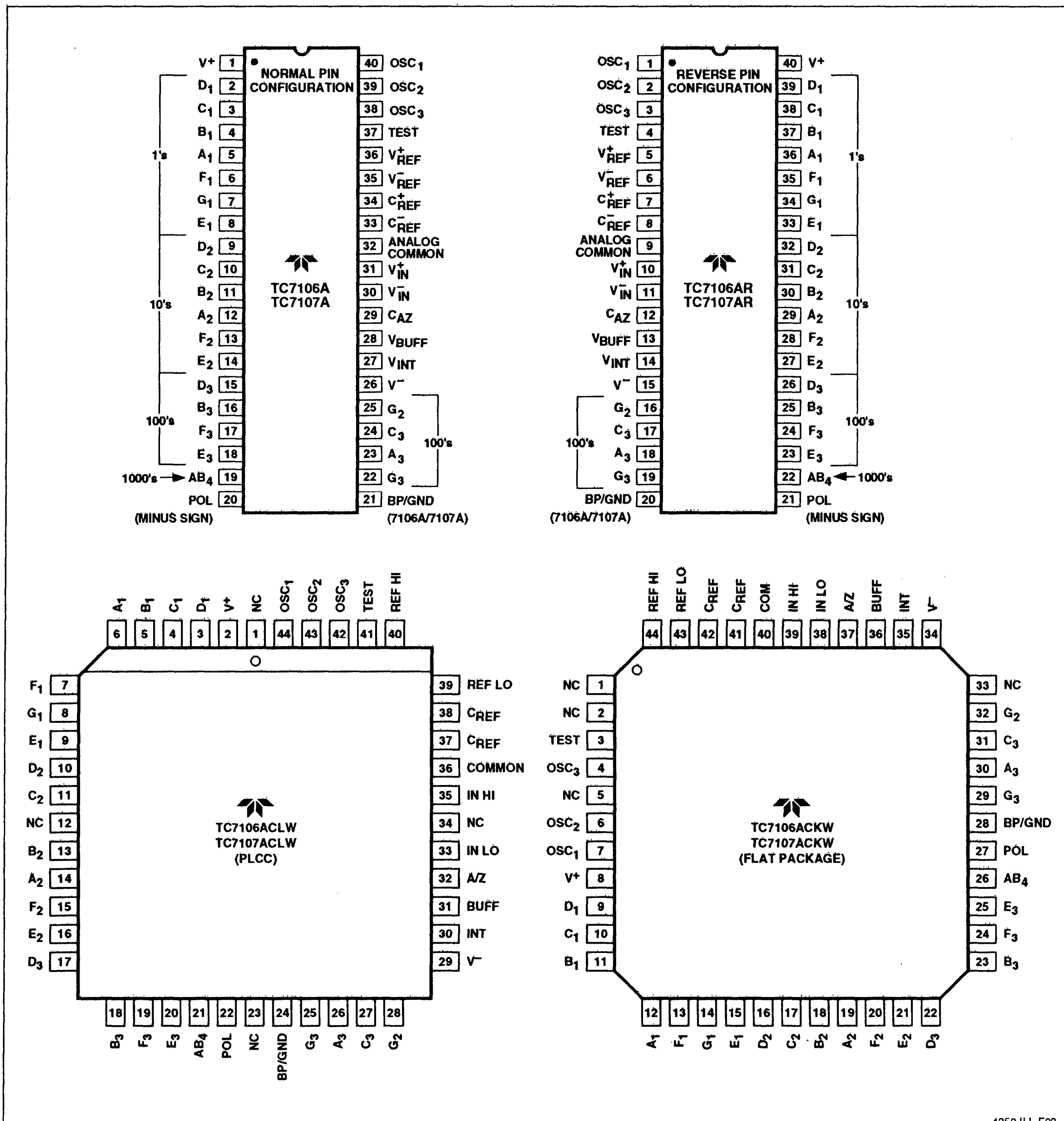
The TC7106A/TC7107A dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TC7106A/TC7107A are available in a small 60-pin flat package for compact designs. DIP devices are offered in an industrial temperature range.

ORDERING INFORMATION

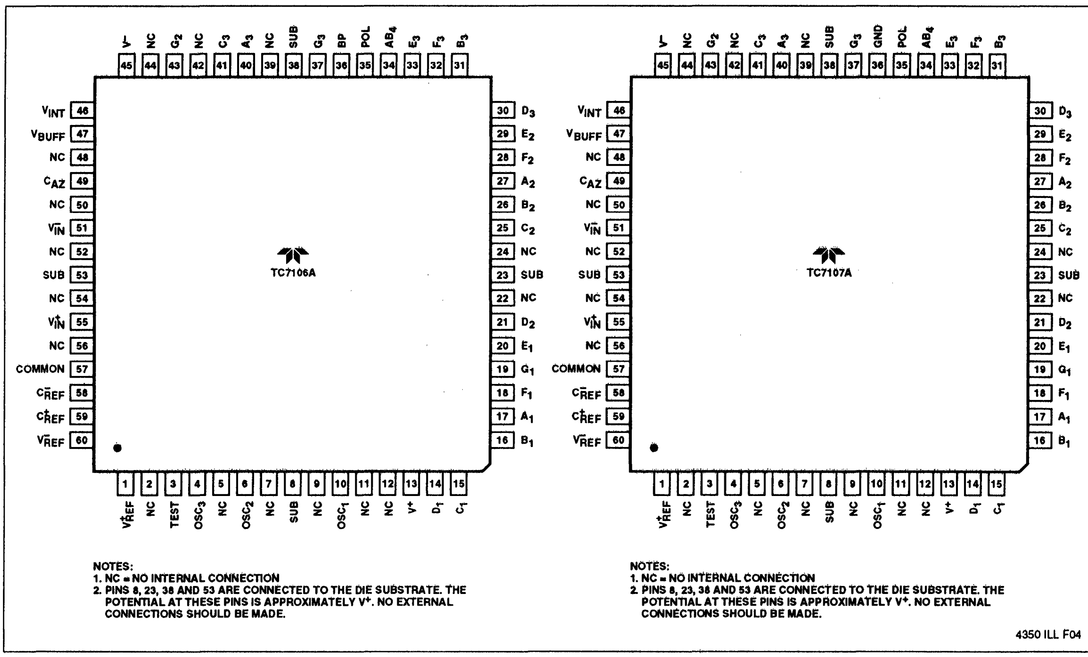
Part No.	Package	Pin Layout	Temperature Range	Display Drive
TC7106CPL	40-Pin Plastic DIP	Normal	0°C to +70°C	LCD
TC7106RCPL	40-Pin Plastic DIP	Reverse	0°C to +70°C	LCD
TC7106IJL	40-Pin CerDIP	Normal	–25°C to +85°C	LCD
TC7106CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TC7106CKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LCD
TC7106CLW	44-Pin PLCC	—	0°C to +70°C	LCD
TC7107CPL	40-Pin Plastic DIP	Normal	0°C to +70°C	LED
TC7107RCPL	40-Pin Plastic DIP	Reverse	0°C to +70°C	LED
TC7107IJL	40-Pin CerDIP	Normal	–25°C to +85°C	LED
TC7107CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TC7107CKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LED
TC7107CLW	44-Pin PLCC	—	0°C to +70°C	LED
TC7106ACPL	40-Pin Plastic DIP	Normal	0°C to +70°C	LCD
TC7106ARCPL	40-Pin Plastic DIP	Reverse	0°C to +70°C	LCD
TC7106AIJL	40-Pin CerDIP	Normal	–25°C to +85°C	LCD
TC7106ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TC7106ACKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LCD
TC7106ACLW	44-Pin PLCC	—	0°C to +70°C	LCD
TC7107ACPL	40-Pin Plastic DIP	Normal	0°C to +70°C	LED
TC7107ARCPL	40-Pin Plastic DIP	Reverse	0°C to +70°C	LED
TC7107AIJL	40-Pin CerDIP	Normal	–25°C to +85°C	LED
TC7107ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TC7107ACKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LED
TC7107ACLW	44-Pin PLCC	—	0°C to +70°C	LED

PIN CONFIGURATIONS



TC7106/7106A
TC7107/7107A

PIN CONFIGURATIONS (Cont.)



ABSOLUTE MAXIMUM RATINGS*

TC7106A

Supply Voltage (V^+ to V^-) .... 15 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) .... V^+ to V^-
Clock Input .... Test to V^+
Power Dissipation (Note 2)
  CerDIP Package .... 1000 mW
  Plastic Package .... 800 mW
Operating Temperature
  "C" Devices .... 0°C to +70°C
  "I" Devices .... –25°C to +85°C
Storage Temperature .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... 300°C

TC7107A

Supply Voltage
  V+ .... +6 V
  V– .... –9 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) .... V^+ to V^-
Clock Input .... GND to V+
Power Dissipation (Note 2)
  CerDIP PAckage .... 1000 mW
  Plastic Package .... 800 mW
Operating Temperature
  "C" Devices .... 0°C to +70°C
  "I" Devices .... –25°C to +85°C
Storage Temperature .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... 300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

Characteristics	Conditions	TC811 Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	–000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF} V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \cong 200$ mV	–1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	–1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200.0 mV	—	50	—	µV/V
Noise (Pk – Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	µV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C	—	0.2	1	µV/°C
	V_{IN} = 0 V "I" Device = –25°C to +85°C	—	1.0	2	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm°C)	—	1	5	ppm/°C
	V_{IN} = 199.0 mV "I" Device = –25°C to +85°C	—	—	20	ppm/°C
Supply Current (Does Not Include LED Current For TC7107A)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25kΩ Between Common and Pos. Supply	2.7	3.05	3.35	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25kΩ Between Common and Pos. Supply 0°C ≤ T_A ≤ 70°C "C," Industrial Temp. Range Devices	—	20	50	ppm/°C
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25kΩ Between Common and Pos. Supply 0°C ≤ T_A ≤ 85°C "I," Industrial Temp. Range Devices	—	—	75	ppm/°C
TC7106A ONLY Pk – Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TC7106A ONLY Pk – Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TC7107A ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TC7107A ONLY Segment Sinking Current (Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ±100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply to both the TC7106A and TC7107A at TA = 25°, f_{CLOCK} = 48 kHz. TC7106A is tested in the circuit of Figure 1. TC7107A is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.

TC7106/7106A
TC7107/7107A

PIN DESCRIPTION

40-Pin DIP Pin Number (Normal)	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the tens display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP GND	LCD Backplane drive output (TC7106A). Digital ground (TC7107A).
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for more details
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ resistor for a 200 mV full-scale range and a 470 kΩ resistor for 2V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.47-µF capacitor for 200 mV full scale, and a 0.047-µF capacitor for 2V full scale. See Paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The analog low input is connected to this pin.
31	(10)	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. It also acts as a reference voltage source. See paragraph on ANALOG COMMON for more details.
33	(8)	58	C_{REF}^-	See pin 34.

PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number (Normal)	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
34	(7)	59	C^{+}_{REF}	A 0.1-µF capacitor is used in most applications. If a large common-mode voltage exists (for example, the V^{-}_{IN} pin is not at analog common), and a 200-mV scale is used, a 1-µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	(6)	60	V^{-}_{REF}	See pin 36.
36	(5)	1	V^{+}_{REF}	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1V between pins 35 and 36 for 2V full scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^{+}) all segments will be turned on and the display should read –1888. It may also be used as a negative supply for externally-generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48-kHz clock (3 readings per section), connect pin 40 to the junction of a 100-kΩ resistor and a 100-pF capacitor. The 100-kΩ resistor is tied to pin 39 and the 100-pF capacitor is tied to pin 38.

General Theory of Operation
Dual Slope Conversion Principles

The TC7106A and TC7107A are dual slope, integrating analog-to-digital converters. An understanding of the dual slope conversion technique will aid in following the detailed operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). (Figure 3A).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_{0}^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

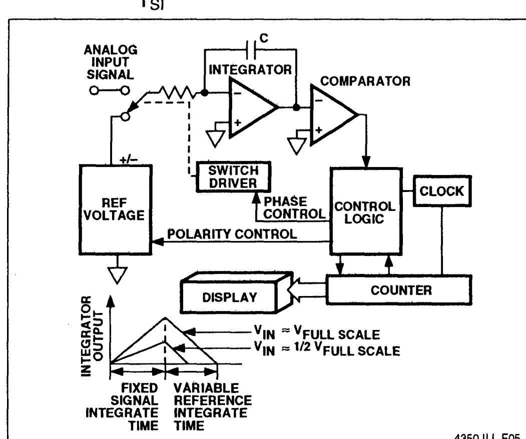


Figure 3A Basic Dual Slope Converter

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environment. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period. (Figure 3B)

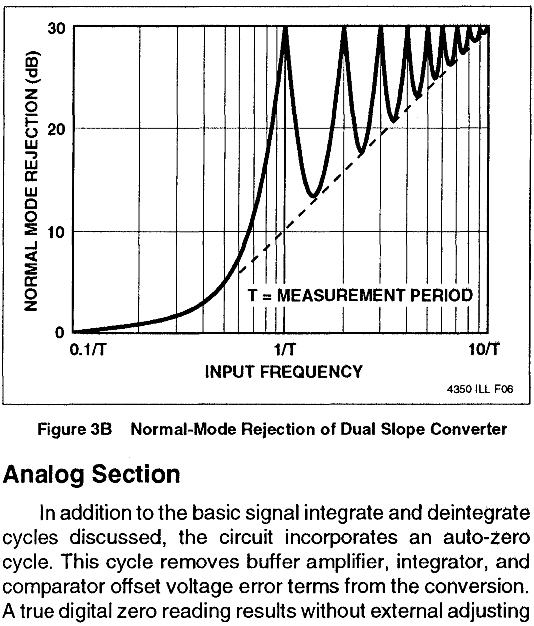


Figure 3B Normal-Mode Rejection of Dual Slope Converter

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed, the circuit incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto zero, signal integrate and reference integrate cycle.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The offset error referred to the input is less than 10 µV.

The auto-zero cycle length is 1000 to 3000 counts.

Signal Integrate Cycle

The auto-zero loop in opened, the internal differential inputs connect to V_{IN}^{+} and V_{IN}^{-}. The differential input signal is integrated for a fixed time period. The signal integration period is 1000 counts. The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 1000$$

where:

f_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range (1 V of either supply) when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^{-} should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

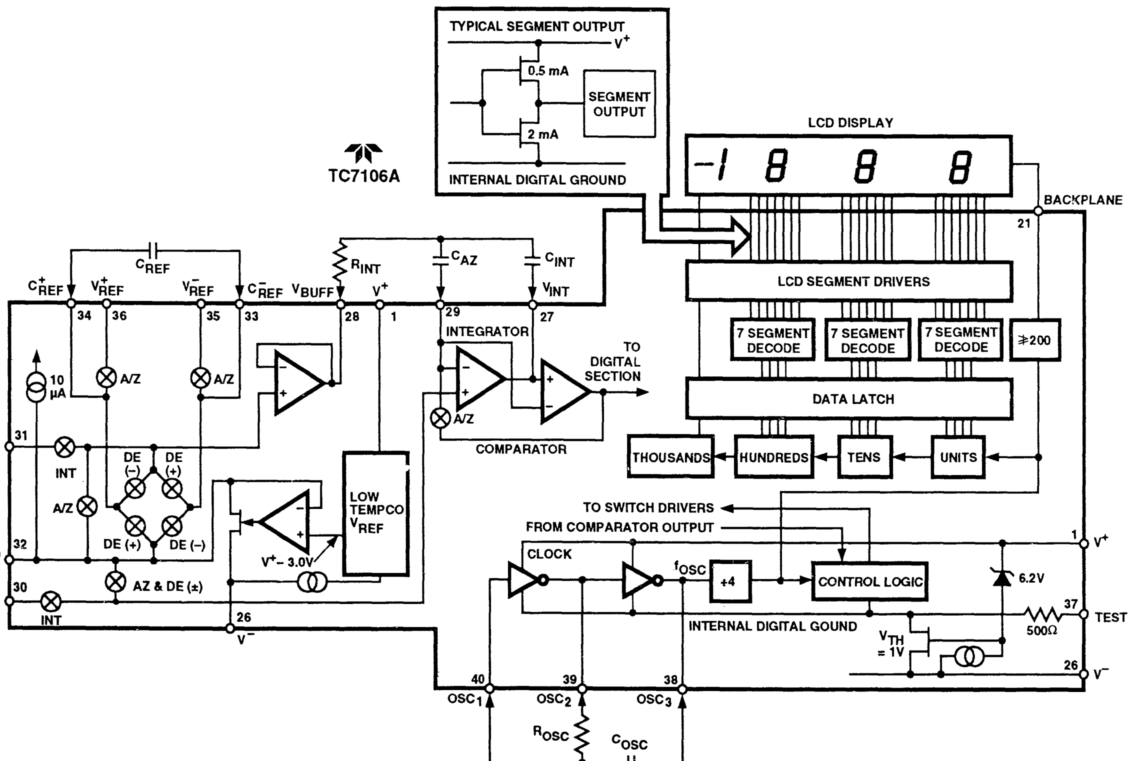
Reference Integrate Cycle

The final phase is reference integrate or de-integrate. V_{IN}^{-} is internally connected to analog common and V_{IN}^{+} is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Digital Section (TC7106A)

The TC7106A (Figure 5) contains all the segment drivers necessary to directly drive a 3 1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^{+} and V_{IN}^{-} are reversed this indicator would reverse.



4350 ILL F07

Figure 5 TC7106A Block Diagram

TC7106/7106A
TC7107/7107A

On the TC7106A when the test pin is pulled to V+ all segments are turned "ON." The display reads –1888. During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and the segment drive assignment are shown in Figure 6.

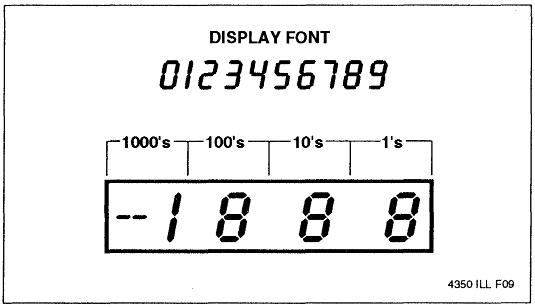


Figure 6 Display FONT and Segment Assignment

In the TC7106A an internal digital ground is generated from a 6 volt zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the backplane voltage is switched.

Digital Section (TC7107A)

Figure 7 shows the TC7107A. It is identical to the TC7106A except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TC7107A is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

The display font is the same as the TC7106A.

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The three phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 1000 to 3000 Counts
  (4000 to 12000 Clock Pulses)
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 1000 Counts
  (4000 Clock Pulses)
  This time period is fixed. The integration period is:

$$T_{SI} = 4000 \left[\frac{1}{f_{OSC}} \right]$$

  Where f_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 2000 Counts
  (0 to 8000 Clock Pulses)

The TC7106A/7107A are drop in replacements for the 7106/7107 parts. External component value changes are not required to benefit from the low drift internal reference.

Clock Circuit

Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

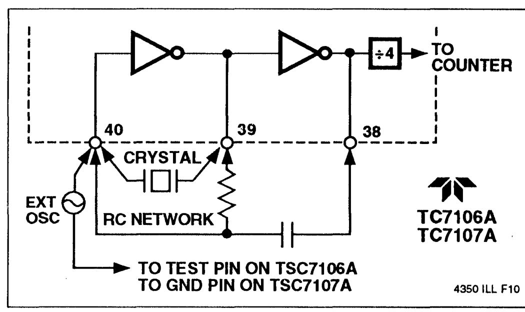


Figure 8 Clock Circuits

Component Value Selection
Auto-Zero Capacitor – C_{AZ}

The C_{AZ} capacitor size has some influence on system noise. A 0.47 µF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 µV. A 0.047 µF capacitor is adequate for 2.0 V full-scale applications. A mylar type dielectric capacitor is adequate.

Reference Voltage Capacitor – C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 µF capacitor is acceptable when V_{IN}^- is tied to analog common. If a large common-mode voltage exists ($V_{REF}^- \neq$ analog common) and the application requires a 200 mV full-scale increase C_{REF} to 1.0 µF. Rollover error will be held to less than 0.5 count. A mylar type dielectric capacitor is adequate.

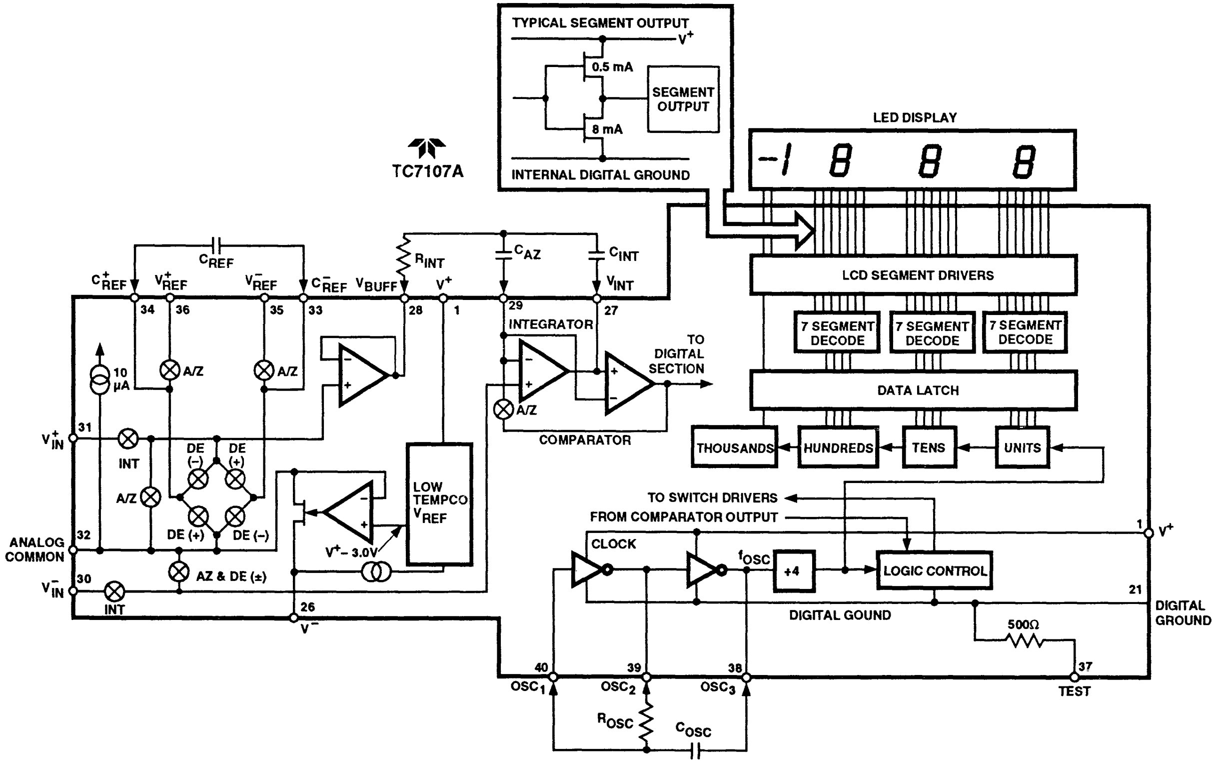


Figure 7 TC7107A Block Diagram

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Integrating Capacitor – C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TC7106A/7107A superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case a ±2 V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz) a 0.22 µF value is suggested. If a different oscillator frequency is used C_{INT} must be changed in inverse proportion to maintain the nominal ±2 V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize rollover error. An inexpensive polypropylene capacitor is recommended.

INTEGRATING RESISTOR – R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 100 µA. The integrator and buffer can supply 20 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full-scale R_{INT} is 47 kΩ. A 2.0 V full-scale requires 470 kΩ.

Component	Nominal Full-Scale Voltage	
Value	200.0 mV	2.000 V
C_{AZ}	0.47 µF	0.047 µF
R_{INT}	47 kΩ	470 kΩ
C_{INT}	0.22 µF	0.22 µF

Note: 1. f_{OSC} = 48 kHz (3 readings/sec)

Oscillator Components

R_{OSC} (Pin 40 to Pin 39) should be 100 kΩ. C_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

For f_{OSC} of 48 kHz, C_{OSC} is 100 pF nominally.

Note that f_{OSC} is divided by four to generate the TC7106A internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 Khz, 66 2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200.0 mV	100.0 mV
2.000 V	1.000 V

* $V_{FS} = 2\ V_{REF}$

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in^2. Rather than dividing the input voltage by two the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

The internal voltage reference potential available at analog common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7 V. In applications where externally generated reference voltage is desired refer to Figure 9.

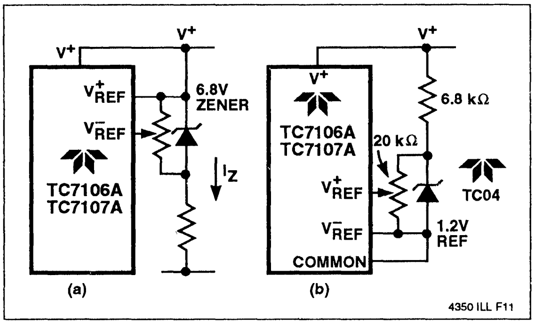


Figure 9 External Reference

Device Pin Functional Description

Differential Signal Inputs

(V^+_{IN} (Pin 31), V^-_{IN} (Pin 30))

The TC7106A/7017A is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is V^+ −1.0 to V^- +1 V. Common-mode voltages are removed from the system when the TC7106A/TC7107A operates from a battery or floating power source (isolated from measured system) and V^-_{IN} is connected to analog common (V_{COM}): See Figure 10.

In systems where common-mode voltages exist in 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 11). For such applications the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V^+ or V^- without increasing linearity errors.

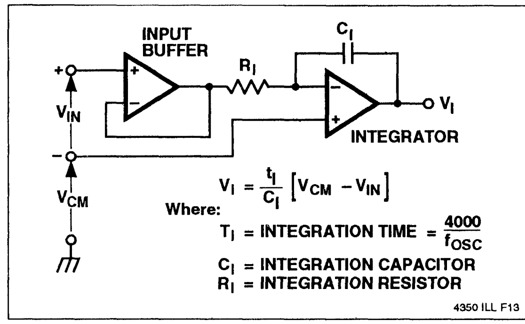


Figure 11 Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Differential Reference

(V^+_{REF} (Pin 36), V^-_{REF} (Pin 35))

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors being induced by large common-mode voltages C_{REF} should be large compared to stray node capacitance.

The TC7106A/TC7107A circuits have significantly lower analog common temperature coefficient. This potential gives a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is 20 ppm/°C typically.

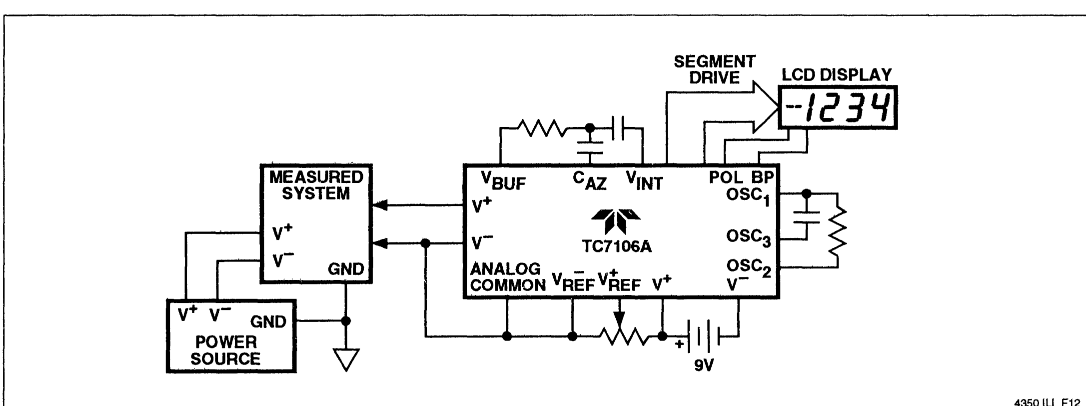


Figure 10 Common-Mode Voltage Removed in Battery Operation with V^-_{IN} = Analog Common

Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0 V below V^+. The potential is guaranteed to be between 2.7 V and 3.35 V below V^+. Analog common is tied internally to the N channel FET capable of sinking 20 mA. This FET will hold the common line at 3.0 V should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 10 μA. Analog common is therefore easily pulled to a more negative voltage (i.e., below V^+ –3.0 V).

The TC7106A connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero cycle. During the reference integrate phase V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converters 86 dB common-mode rejection ratio. In battery operation analog common and V_{IN}^- are usually connected removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference or common point. The TC7106A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC7106A power source. The analog common potential of V^+ –3.0 V gives a 6 V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and a 15 Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- > 7.0$ V) analog common is a very stable potential with excellent temperature stability—typically 20 ppm/°C. This potential can be used to generate the reference voltage. An external voltage reference will be unnecessary in most cases because of the 50 ppm/°C maximum temperature coefficient. See Internal Voltage Reference discussion.

Test (Pin 37)

The test pin potential is 5 V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally generated negative logic supply (Internal Logic Ground) through a 500Ω resistor in the TC7106A. The test pin load should be no more than 1mA .

If test is pulled to V^+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes with the TC7106A. With Test = V^+ the LCD Segments are impressed with a DC voltage which will destroy the LCD.

The test pin will sink about 10 mA when pulled to V^+.

Internal Voltage Reference Stability

The analog common voltage temperature stability has been significantly improved (Figure 12). The "A" version of the industry standard circuits allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 13 shows analog common supplying the necessary voltage reference for the TC7106A/TC7107A.

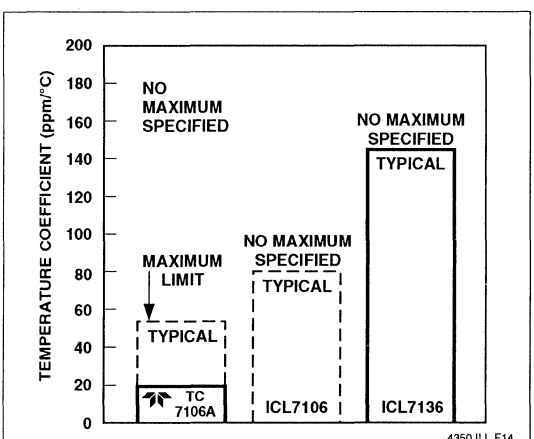


Figure 12 Analog CommonTemperature Coefficient

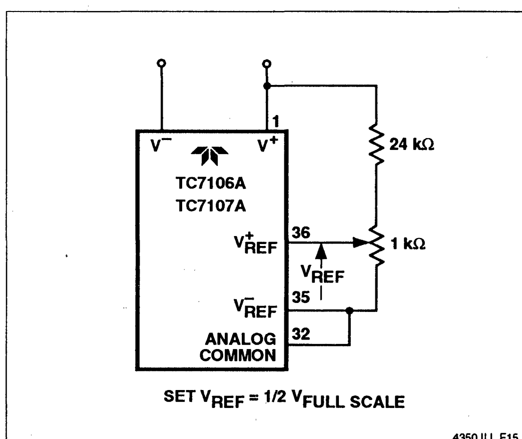


Figure 13 Internal Voltage Reference Connection

Power Supplies

The TC7107A is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors, and an inexpensive IC. (Figure 14)

In selected applications a negative supply is not required. The conditions to use a single +5V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5V.
- An external reference is used.

The TSC7660 DC to DC converter may be used to generate –5 V from +5 V (Figure 15).

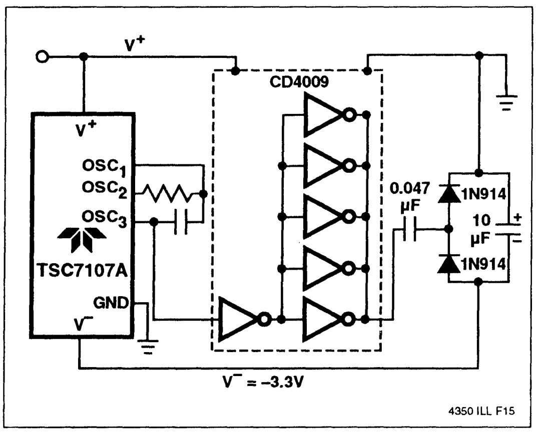


Figure 14 Generating Negative Supply From +5 V

TC7107 Power Dissipation Reduction

The TC7107A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TC7107A package power dissipation is reduced.

Figure 16 is a photograph of a curve-trace display showing the relationship between output current and output voltage for a typical TC7107CPL. Since a typical LED has 1.8 volts across it at 7 mA, and its common anode is connected to +5 V, the TC7107A output is at 3.2 V. (point A on Figure 15). Maximum power dissipation is 8.1 mA x 3.2 V x 24 segments = 622 mW.

Notice, however, that once the TC7107A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B in Figure 16) results in 7.7 mA of LED current,

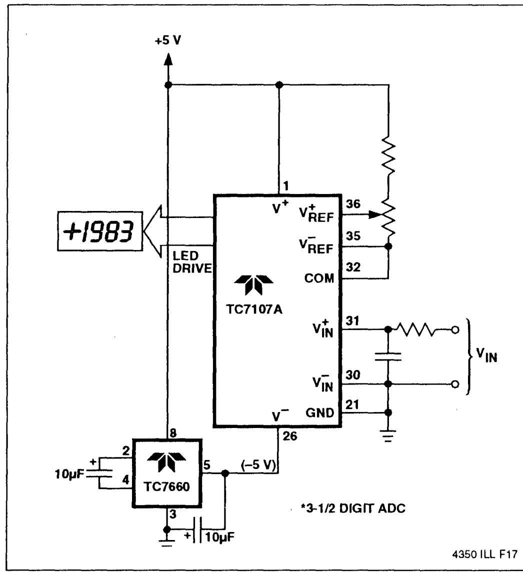


Figure 15 Negative Power Supply Generation with TC7660

only a 5 percent reduction. Maximum power dissipation is only 7.7 mA x 2.5 V x 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA x 2.2 V x 24 = 385 mW).

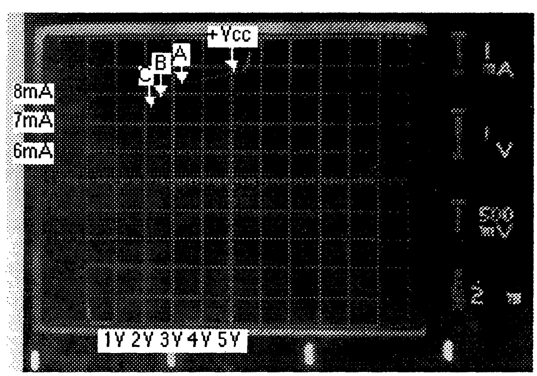


Figure 16 TC7107A Output Current vs Output Voltage

TC7106/7106A
TC7107/7107A

Reduced power dissipation is very easy to obtain. Figure 17 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TC7107A). The resistor will reduce the TC7107A output voltage, when all 24 segments are "ON," to point "C" of Figure 16. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

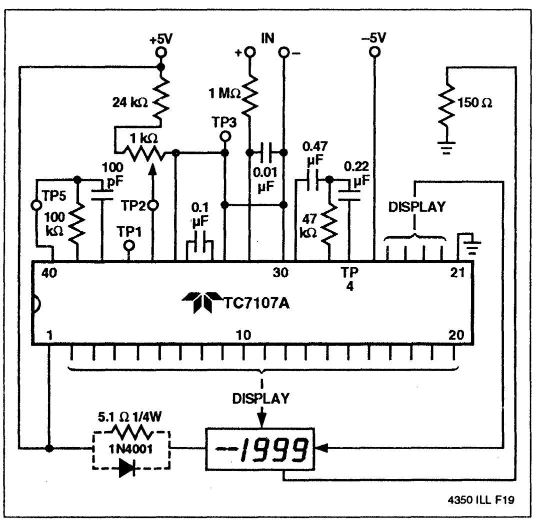


Figure 17 Diode or Resistor Limits Package Power Dissipation

APPLICATIONS INFORMATION
LIQUID CRYSTAL DISPLAY SOURCES

Several LCD manufacturers supply standard LCD displays to interface with the TC7106A 3 1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note: 1. Contact LCD manufacturer for full product listing/ specifications.

Light Emitting Diode Display Sources

Several LED manufacturers supply seven segment digits with and without decimal point annunciators for the TC7107A.

Manufacturer	Address	Display Type
Hewlett-Packard Components	640 Page Mill Rd. Palo Alto, CA 94304	LED
And	770 Airport Blvd. Burlingame, CA 94010	LED

Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500 Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5 V below V^+.

Ratiometric Resistance Measurements

The true differential input and differential reference make ratiometric reading possible. Typically in a ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

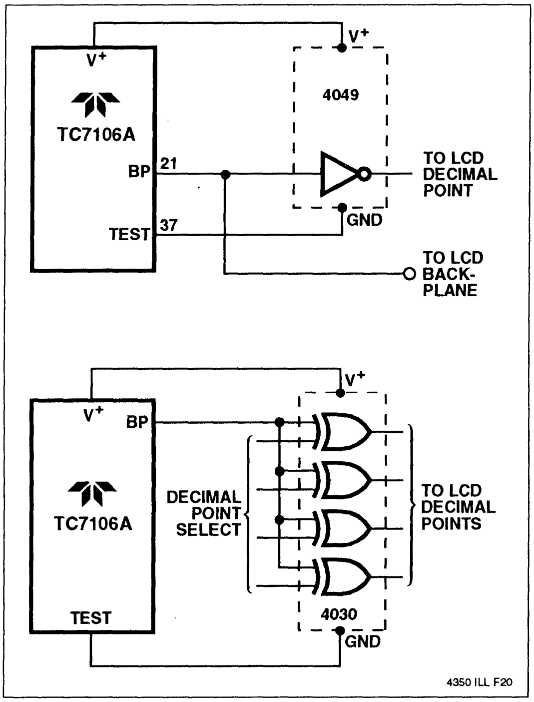


Figure 18 Decimal Point Drive Using Test as Logic Ground

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor is applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

The display will overrange for R Unknown ≥ 2 x R standard.

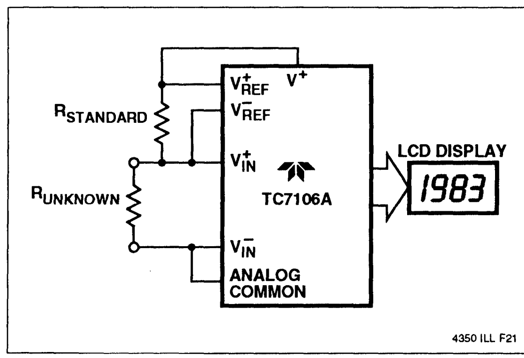


Figure 19 Low Parts Count Ratiometric Resistance Measurement

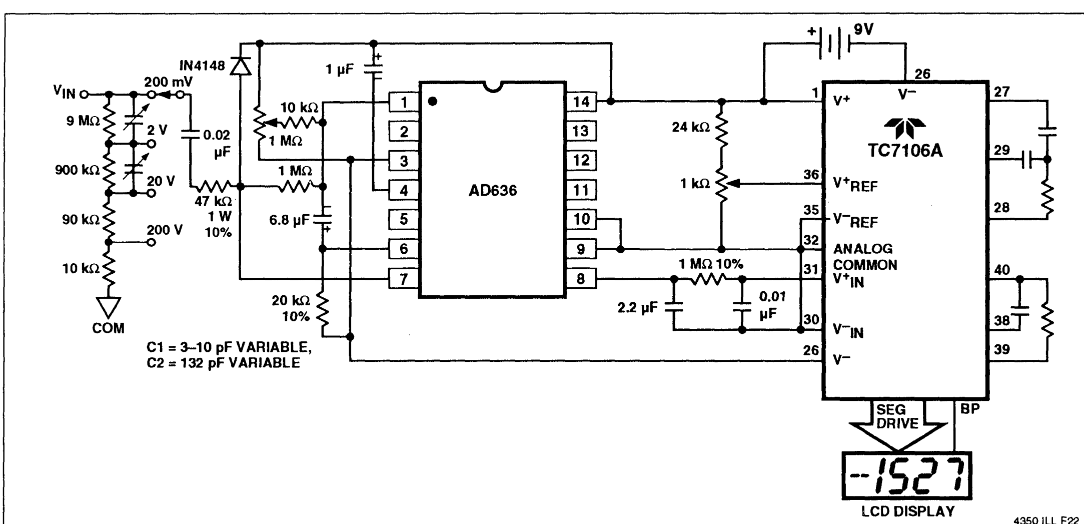


Figure 20 3 1/2 Digit True RMS AC DMM

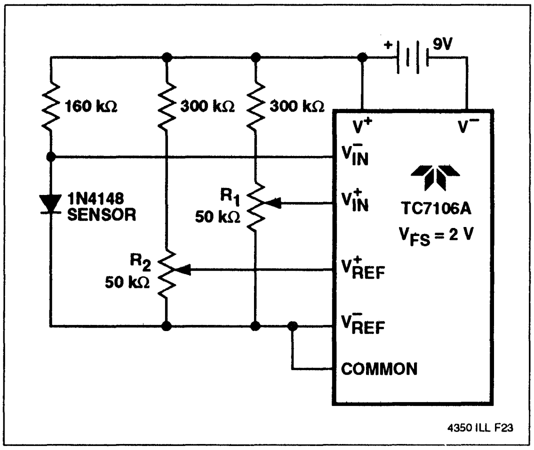


Figure 21 Temperature Sensor

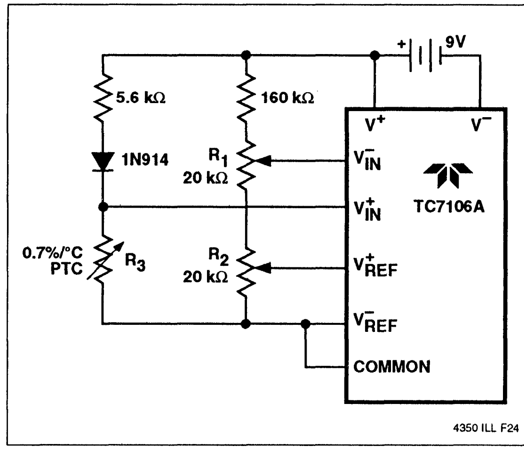


Figure 22 Positive Temperature Coefficient Resistor Temperature Sensor

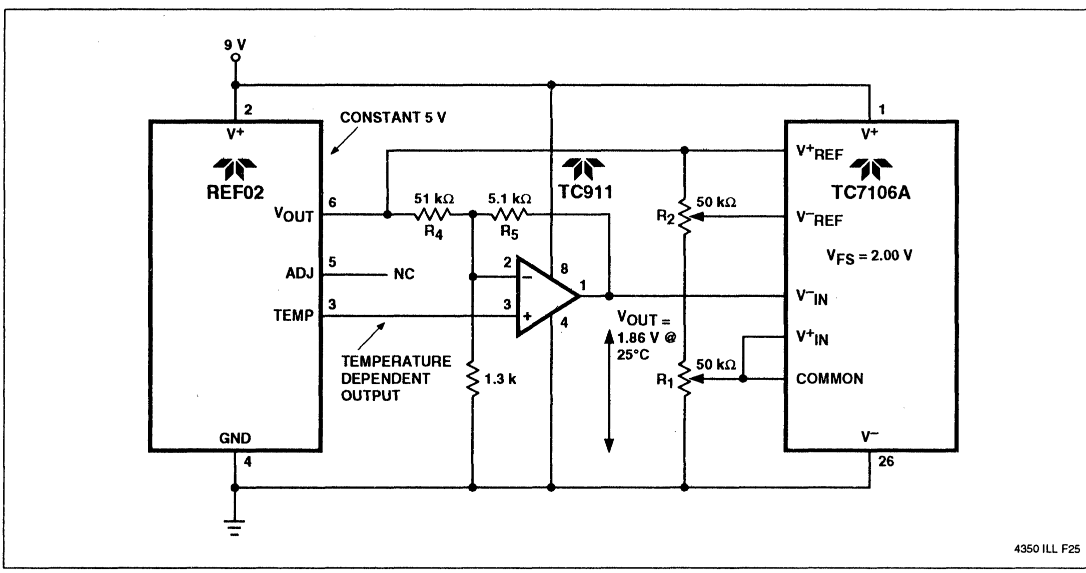


Figure 23 Integrated Circuit Temperature Sensor

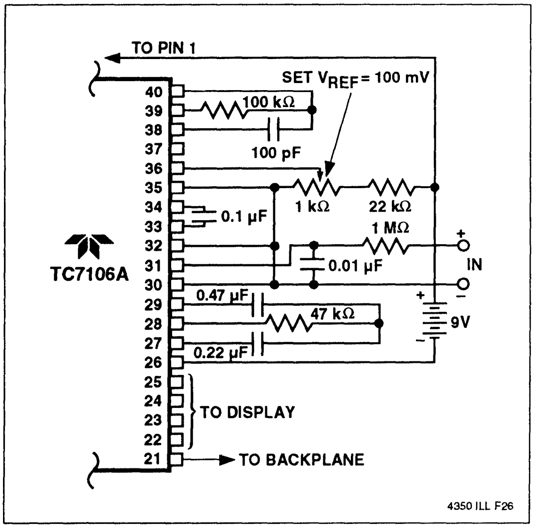


Figure 24 TC7106A Using the Internal Reference. (200 mV Full-Scale, 3 RPS).

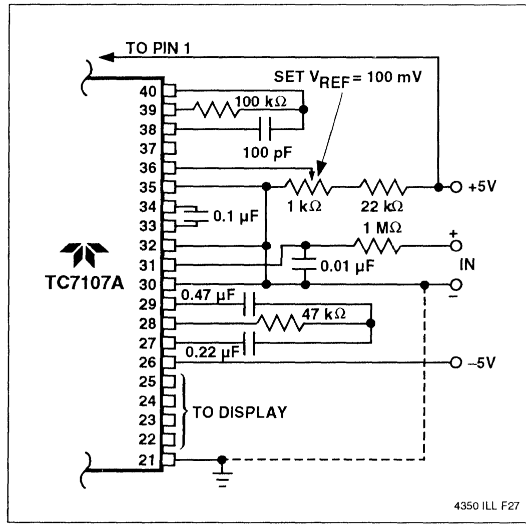


Figure 25 TC7107A Internal Reference (200 mV Full-Scale, 3 RPS, $V_{\overline{IN}}$ Tied to GND for Single Ended Inputs).

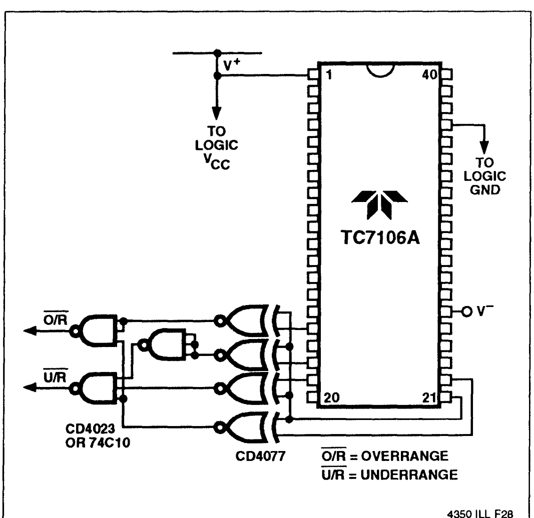


Figure 26 Circuit for Developing Underrange and Overrange Signals from TC7106A Outputs.

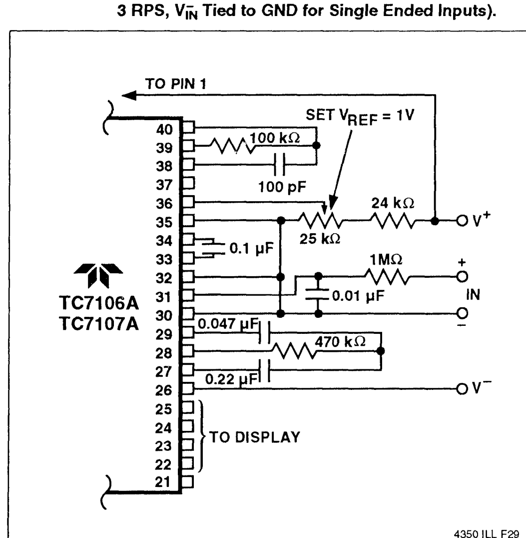


Figure 27 TC7106A/TC7107A: Recommended Component Values for 2.00 V Full-Scale

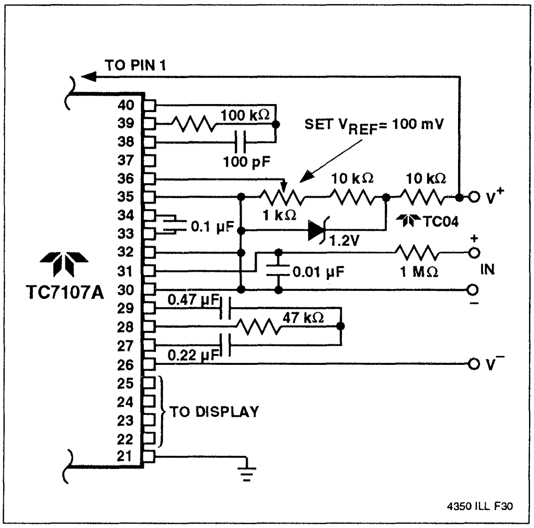


Figure 28 TC7107A With a 1.2 V External Band-Gap Reference. (V^-_{IN} Tied to Common.)

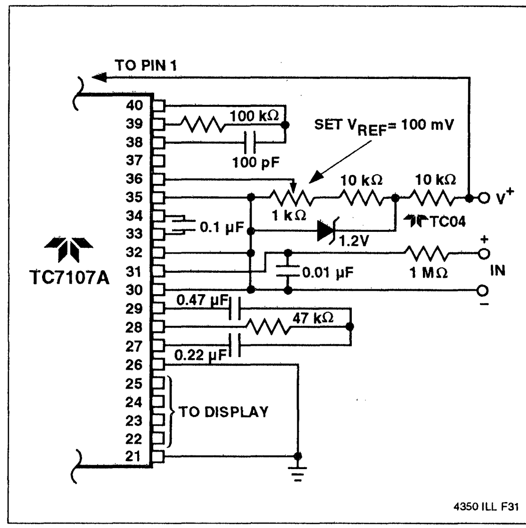


Figure 29 TC7107A Operated from Single +5 V Supply An External Reference Must Be Used in This Application.

TELEDYNE COMPONENTS

TC7116 TC7117
TC7116A TC7117A

3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTERS WITH HOLD

FEATURES

- Low Temperature Drift Internal Reference
  - TC7116/TC7117 .... 80 ppm/°C Typ
  - TC7116A/TC7117A .... 20 ppm/°C Typ
- Display Hold Function
- Directly Drives LCD or LED Display
- Guaranteed Zero Reading With Zero Input
- Low Noise for Stable Display ....2V or 200 mV Full-Scale Range (FSR)
- Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer
- True Polarity Indication for Precision Null Applications
- Convenient 9V Battery Operation (TC7116/TC7116A)
- High Impedance CMOS Differential Inputs ...$10^{12}\Omega$
- Low Power Operation .... 10 mW

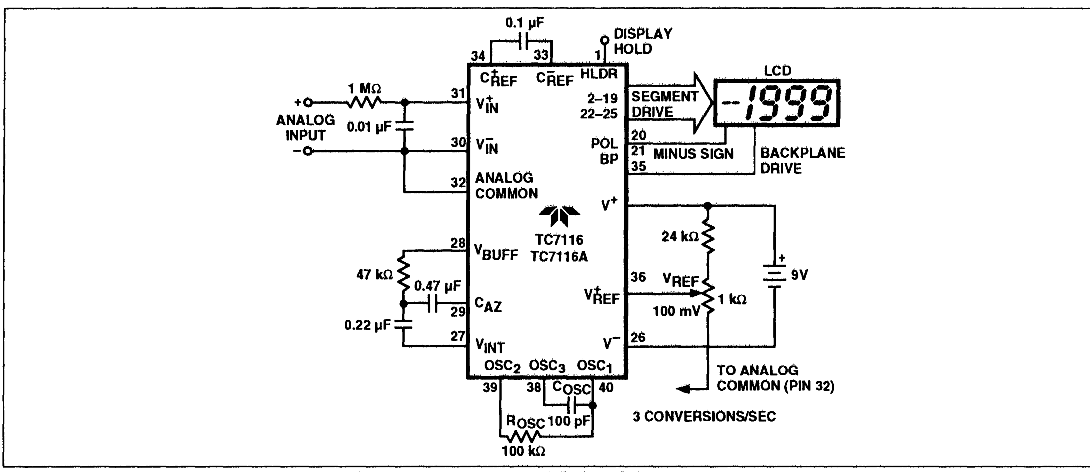


Figure 1 Typical TC7116/TC7116A Operating Circuit

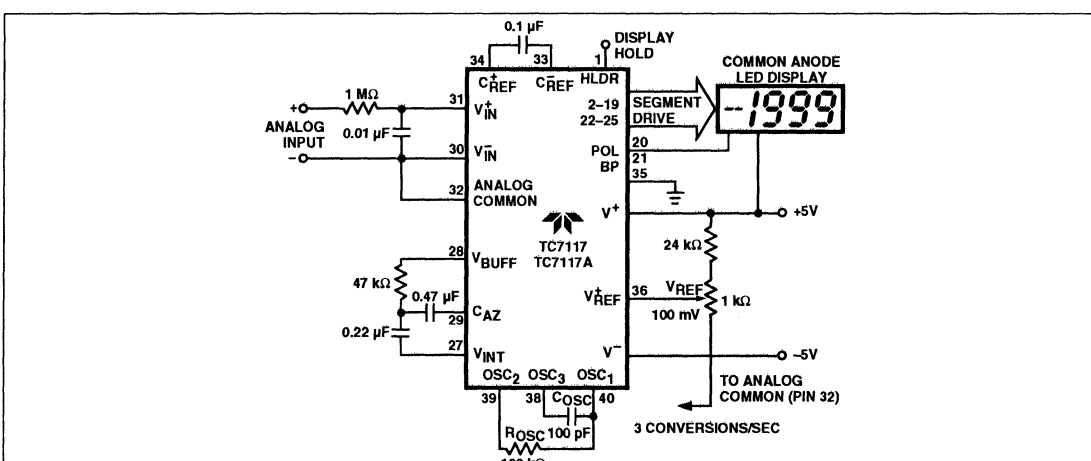


Figure 2 Typical TC7117/TC7117A Operating Circuit

TC7116 TC7117
TC7116A TC7117A

GENERAL DESCRIPTION

The TC7116A and TC7117A feature a precision, low-drift internal reference, and are functionally identical to the TC7116/TC7117. A low-drift external reference is not normally required with the TC7116A/TC7117A.

The TC7116A/TC7117A are 3-1/2 digit CMOS analog-to-digital converters (ADCs) containing all the active components necessary to construct a 0.05% resolution measurement system. Seven-segment decoders, polarity and digit drivers, voltage reference, and clock circuit are integrated on-chip. The TC7116A drives liquid crystal displays (LCDs) and includes a backplane driver. The TC7117A drives common anode light emitting diode (LED) displays directly with an 8-mA drive current per segment.

These devices incorporate a display hold (HLDR) function. The displayed reading remains indefinitely, as long as HLDR is held high. Conversions continue, but output data display latches are not updated. The reference low input ($V_{\overline{REF}}$) is not available as it is with the TC7106/7107. $V_{\overline{REF}}$ is tied internally to analog common in the TC7116A/7117A devices.

The TC7116A/7117A reduces linearity error to less than 1 count. Roll-over error (the difference in readings for equal magnitude but opposite polarity input signals) is below ±1 count. High-impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a 0V input.

The TC7116A/7117A dual-slope conversion technique automatically rejects interference signals if the converter's integration time is set to a multiple of the interference period. This is especially useful in industrial measurement environments where 50-Hz, 60-Hz, and 400-Hz line frequency signals are present.

The TC7116A/7117A are available in a small, 60-pin flat package for compact designs. Standard devices are offered in an industrial temperature range and with 160-hour burn-in at +125°C.

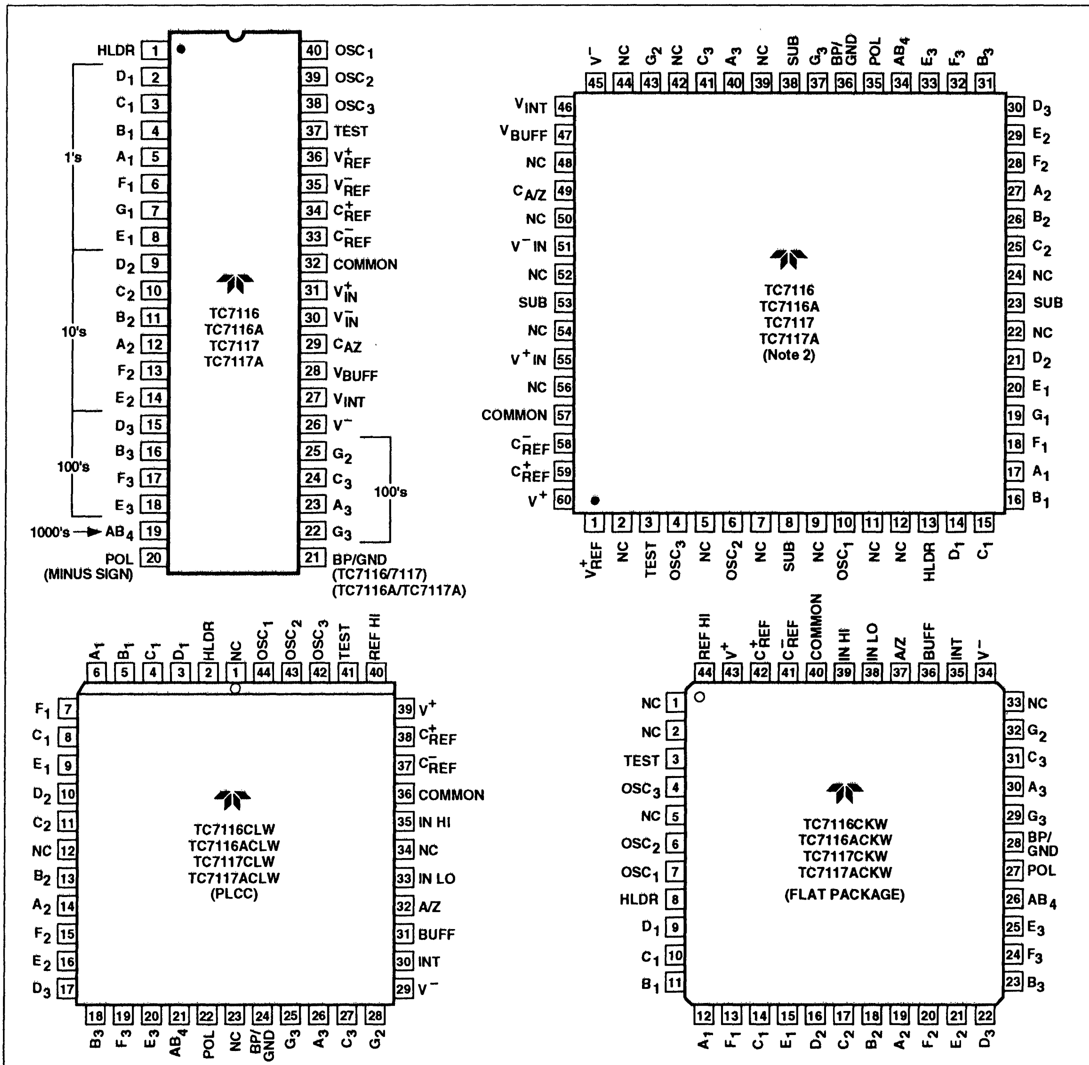
ORDERING INFORMATION

Part No.	Package	Temperature Range	Reference Temperature Coefficient	Display Drive
TC7116CPL	40-Pin Plastic DIP	0°C to +70°C	80 ppm/°C	LCD
TC7116ACPL	40-Pin Plastic DIP	0°C to +70°C	35 ppm/°C	LCD
TC7116IPL	40-Pin Plastic DIP	–25°C to +85°C	80 ppm/°C	LCD
TC7116CJL	40-Pin CerDIP	0°C to +70°C	80 ppm/°C	LCD
TC7116IJL	40-Pin CerDIP	–25°C to +85°C	80 ppm/°C	LCD
TC7116AIJL	40-Pin CerDIP	–25°C to +85°C	35 ppm/°C	LCD
TC7116CBQ	60-Pin Plastic Flat	0°C to +70°C	80 ppm/°C	LCD
TC7116ACBQ	60-Pin Plastic Flat	0°C to +70°C	35 ppm/°C	LCD
TC7116CKW	44-Pin Plastic Flat	0°C to +70°C	80 ppm/°C	LCD
TC7116ACKW	44-Pin Plastic Flat	0°C to +70°C	35 ppm/°C	LCD
TC7116CLW	44-Pin PLCC	0°C to +70°C	80 ppm/°C	LCD
TC7116ACLW	44-Pin PLCC	0°C to +70°C	35 ppm/°C	LCD
TC7117CPL	40-Pin Plastic DIP	0°C to +70°C	80 ppm/°C	LED
TC7117ACPL	40-Pin Plastic DIP	0°C to +70°C	35 ppm/°C	LED
TC7117IPL	40-Pin Plastic DIP	–25°C to +85°C	80 ppm/°C	LED
TC7117CJL	40-Pin CerDIP	0°C to +70°C	80 ppm/°C	LED
TC7117IJL	40-Pin CerDIP	–25°C to +85°C	80 ppm/°C	LED
TC7117AIJL	40-Pin CerDIP	–25°C to +85°C	35 ppm/°C	LED
TC7117CBQ	60-Pin Plastic Flat	0°C to +70°C	80 ppm/°C	LED
TC7117ACBQ	60-Pin Plastic Flat	0°C to +70°C	35 ppm/°C	LED
TC7117CKW	44-Pin Plastic Flat	0°C to +70°C	80 ppm/°C	LED
TC7117ACKW	44-Pin Plastic Flat	0°C to +70°C	35 ppm/°C	LED
TC7117CLW	44-Pin PLCC	0°C to +70°C	80 ppm/°C	LED
TC7117ACLW	44-Pin PLCC	0°C to +70°C	35 ppm/°C	LED

3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTERS WITH HOLD

TC7116 TC7117
TC7116A TC7117A

PIN CONFIGURATIONS



NOTES:
1. NC = No internal connection.
2. Pins 8, 23, 38, and 53 are connected to the die substrate. The potential at these pins is approximately V+. No external connections should be made.

TC7116 TC7117
TC7116A TC7117A

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage
- TC7116/TC7116A: V^+ to V^- .... ±15V
- TC7117/TC7117A: V^+ to GND .... +6V
- V^- to GND .... –9V

Analog Input Voltage (Either Input) (Note 1) .... V^+ to V^-
Reference Input Voltage (Either Input) .... V^+ to V^-
Clock Input
- TC7116/TC7116A .... TEST to V^+
- TC7117/TC7117A .... GND to V^+

Power Dissipation (Note 2)
- CerDIP .... 1000 mW
- Plastic .... 800 mW

Operating Temperature
- "C" Device .... 0°C to +70°C
- "I" Device .... –25°C to +85°C

Storage Temperature .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... 300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV	—	±0	—	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in Reading for Equal Positive and Negative Readings Near Full Scale)	$-V_{IN} = +V_{IN} \cong$ 200 mV or ≈ 2V	–1	±0.2	+1	Counts
Linearity (Maximum Deviation From Best Straight Line Fit)	Full Scale = 200 mV or 2V	–1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200 mV	—	50	—	µV/V
Noise (Peak-to-Peak Value Not Exceeded 95% of Time)	V_{IN} = 0V Full Scale = 200 mV	—	15	—	µV
Leakage Current at Input	V_{IN} = 0V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0V "C" Device: 0°C to +70°C "I" Device: –25°C to +85°C	 — —	 0.2 1	 1 2	 µV/°C µv/°C
Scale Factor Temperature Coefficient	V_{IN} = 199 mV "C" Device: 0°C to +70°C (Ext Ref = 0 ppm/°C) "I" Device: –25°C to +85°C	 — —	 1 —	 5 20	 ppm/°C ppm/°C
Input Resistance, Pin 1	Note 6	30	70	—	kΩ
V_{IL}, Pin 1	TC7116A Only	—	—	Test +1.5	V
V_{IL}, Pin 1	TC7117A Only	—	—	GND +1.5	V
V_{IH}, Pin 1	Both	V^+ –1.5	—	—	V
Supply Current (Does Not Include LED Current for 7117A)	V_{IN} = 0V	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Positive Supply)	25 kΩ Between Common and Positive Supply	2.4	3.05	3.35	V
Temperature Coefficient of Analog Common (With Respect to Positive Supply)	"C" Device: 0°C to +70°C TC7116A/TC7117A TC7116/TC7117	 — —	 20 80	 50 —	 ppm/°C ppm/°C
Temperature Coefficient of Analog Common (With Respect to Positive Supply)	"I" Device: –25°C to +85°C 25 kΩ Between Common and Positive Supply (TC7116A/TC7117A)	—	—	75	ppm/°C

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Test Conditions	Min	Typ	Max	Unit
TC7116/TC7116A ONLY Peak-to-Peak Segment Drive Voltage	V^+ to $V^- = 9V$ (Note 5)	4	5	6	V
TC7116/TC7116A ONLY Peak-to-Peak Backplane Drive Voltage	V^+ to $V^- = 9V$ (Note 5)	4	5	6	V
TC7117/TC7117A ONLY Segment Sinking Current (Except Pin 19)	$V^+ = 5V$ Segment Voltage = 3V	5	8	—	mA
TC7117/TC7117A ONLY Segment Sinking Current (Pin 19 Only)	$V^+ = 5V$ Segment Voltage = 3V	10	16	—	mA

NOTES:
1. Input voltages may exceed supply voltages, provided input current is limited to ±100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply at $T_A = +25°C$, $f_{CLOCK} = 48$ kHz. TC7116/TC7116A are tested in the circuit of Figure 1. TC7117/TC7117A are tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in-phase with segment drive for "off" segment, 180° out-of-phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. The TC7116/TC7116A logic inputs have an internal pull-down resistor connected from HLDR, pin 1 to TEST, pin 37. The TC7117/TC7117A logic inputs have an internal pull-down resistor connected from HLDR, pin 1 to GND, pin 21.

PIN DESCRIPTION

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
1	13	HLDR	Hold pin, Logic 1 holds present display reading.
2	14	D_1	Activates the D section of the units display.
3	15	C_1	Activates the C section of the units display.
4	16	B_1	Activates the B section of the units display.
5	17	A_1	Activates the A section of the units display.
6	18	F_1	Activates the F section of the units display.
7	19	G_1	Activates the G section of the units display.
8	20	E_1	Activates the E section of the units display.
9	21	D_2	Activates the D section of the tens display.
10	25	C_2	Activates the C section of the tens display.
11	26	B_2	Activates the B section of the tens display.
12	27	A_2	Activates the A section of the tens display.
13	28	F_2	Activates the F section of the tens display.
14	29	E_2	Activates the E section of the tens display.
15	30	D_3	Activates the D section of the hundreds display.
16	31	B_3	Activates the B section of the hundreds display.
17	32	F_3	Activates the F section of the hundreds display.
18	33	E_3	Activates the E section of the hundreds display.
19	34	AB_4	Activates both halves of the 1 in the thousands display.
20	35	POL	Activates the negative polarity display.
21	36	BP GND	LCD backplane drive output (TC7116/TC7116A). Digital ground (TC7117/TC7117A).
22	37	G_3	Activates the G section of the hundreds display.
23	40	A_3	Activates the A section of the hundreds display.

PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
1	13	HLDR	Hold pin, Logic 1 holds present display reading.
24	41	C_3	Activates the C section of the hundreds display.
25	43	G_2	Activates the G section of the tens display.
26	45	V^-	Negative power supply voltage.
27	46	V_{INT}	Integrator output. Connection point for integration capacitor. See Integration Capacitor section for additional details.
28	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ resistor for 200 mV full-scale range and a 470 kΩ resistor for 2V full-scale range.
29	49	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.47 µF capacitor for 200 mV full scale and a 0.047 µF capacitor for 2V full scale. See Auto-Zero Capacitor paragraph for more details.
30	51	V_{IN}^-	The analog low input is connected to this pin.
31	55	V_{IN}^+	The analog high input is connected to this pin.
32	57	ANALOG	This pin is primarily used to set the analog common-mode COMMON voltage for battery operation or in systems where the input signal is referenced to the power supply. See Analog Common paragraph for more details. It also acts as a reference voltage source.
33	58	C_{REF}^-	See pin 34.
34	59	C_{REF}^+	A 0.1 µF capacitor is used in most applications. If a large, common-mode voltage exists (e.g., the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1 µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	60	V^+	Positive power supply voltage.
36	1	V_{REF}^+	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 32 and 36 for 199.9 mV full scale. Place 1V between pins 32 and 36 for 2V full scale. See paragraph on Reference Voltage.
37	3	TEST	Lamp test. When pulled high (to V^+), all segments will be turned on and the display should read −1888. It may also be used as a negative supply for externally-generated decimal points. See Test paragraph for more details.
38	4	OSC_3	See pin 40.
39	6	OSC_2	See pin 40.
40	10	OSC_1	Pins 40, 39 and 38 make up the oscillator section. For a 48 kHz clock (3 readings per sec), connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTERS WITH HOLD

TC7116 TC7117 TC7116A TC7117A

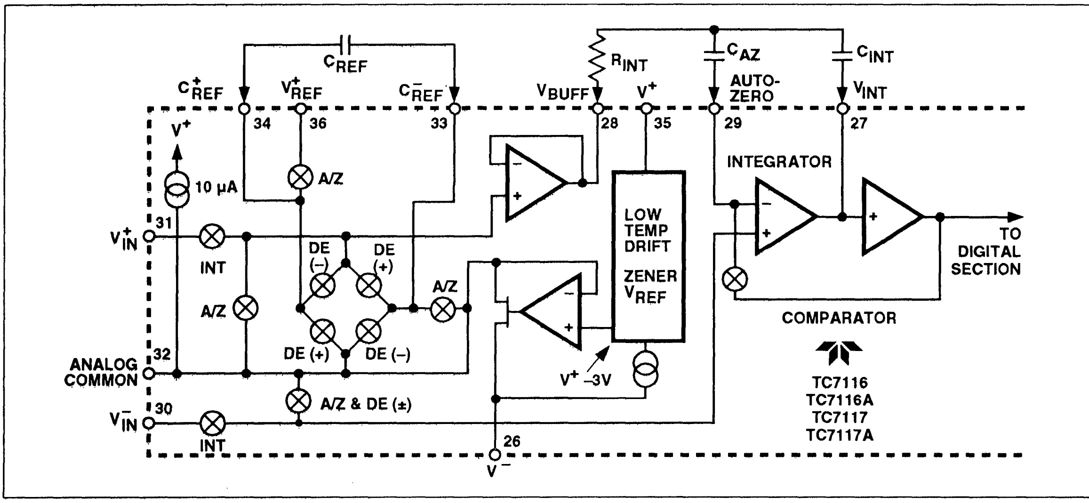


Figure 3 Analog Section of TC7116/TC7116A and TC7117/TC7117A

ANALOG SECTION

Figure 3 shows the block diagram of the analog section for the TC7116/TC7116A and TC7117/TC7117A. Each measurement cycle is divided into three phases: (1) auto-zero (A-Z), (2) signal integrate (INT), and (3) reference integrate (REF) or deintegrate (DE).

Auto-Zero Phase

High and low inputs are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor (C_{AZ}) to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, A-Z accuracy is limited only by system noise. The offset referred to the input is less than 10 µV.

Signal-Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal high and low inputs are connected to the external pins. The converter then integrates the differential voltages between V^{+}_{IN} and V^{-}_{IN} for a fixed time. This differential voltage can be within a wide common-mode range; 1V of either supply. However, if the input signal has no return with respect to the converter power supply, V^{-}_{IN} can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate, or deintegrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}.$$

Reference

The positive reference voltage (V^{+}_{REF}) is referenced to analog common.

Differential Input

This input can accept differential voltages anywhere within the common-mode range of the input amplifier or, specifically, from 1V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86 dB, typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to ensure the integrator output does not saturate. A worst-case condition would be a large, positive common-mode voltage with a near full-scale negative differential input voltage. The negative-input signal drives the integrator positive when most of its swing has been used up by the

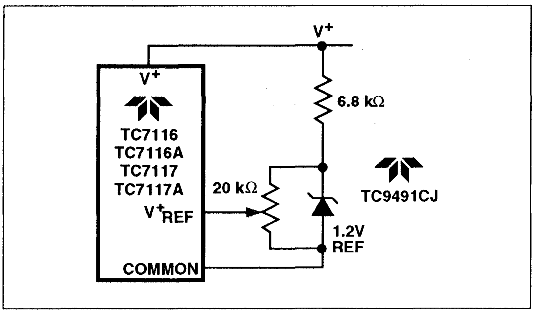


Figure 4 Using an External Reference

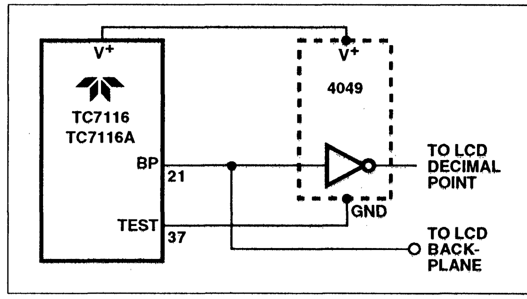


Figure 5 Simple Inverter for Fixed Decimal Point

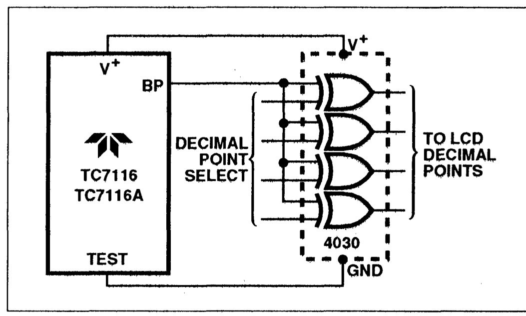


Figure 6 Exclusive "OR" Gate for Decimal Point Drive

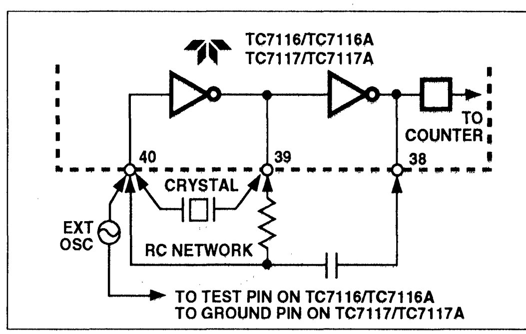


Figure 7 Clock Circuits

positive common-mode voltage. For these critical applications, the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TC7116/TC7116A) or for any system where the input signals are floating with respect to the power supply. The analog common pin sets a voltage approximately 2.8V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog common has some attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the analog common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≅15Ω), and a temperature coefficient of less than 20 ppm/°C, typically, and 50 ppm maximum. The TC7116/TC7117 temperature coefficients are typically 80 ppm/°C.

An external reference may be used, if necessary, as shown in Figure 4.

Analog common is also used as $V_{\overline{IN}}$ return during auto-zero and deintegrate. If $V_{\overline{IN}}$ is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications, $V_{\overline{IN}}$ will be set at a fixed, known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage; if it can be conveniently referenced to analog common it should be, since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 3V below the positive supply (when a load is trying to pull the analog common line positive). However, there is only 10 μA of source current, so analog common may easily be tied to a more negative voltage, thus overriding the internal reference.

Test

The test pin serves two functions. On the TC7117/TC7117A, it is coupled to the internally-generated digital supply through a 500Ω resistor. Thus, it can be used as a negative supply for externally-generated segment drivers, such as decimal points or any other presentation the user may want to include on the LCD. (Figures 5 and 6 show such an application.) No more than a 1 mA load should be applied.

The second function is a "lamp test." When test is pulled high (to V+), all segments will be turned on and the display should read –1888. The test pin will sink about 10 mA under these conditions.

DIGITAL SECTION

Figures 8 and 9 show the digital section for TC7116/TC7116A and TC7117/TC7117A, respectively. For the TC7116/TC7116A (Figure 8), an internal digital ground is generated from a 6V zener diode and a large P-channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency ÷800. For 3 readings per second, this is a 60-Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude, and are in-phase with BP when OFF, but out-of-phase when ON. In all cases, negligible DC voltage exists across the segments.

Figure 9 is the digital section of the TC7117/TC7117A. It is identical to the TC7116/TC7116A, except the regulated supply and BP drive have been eliminated, and the segment drive is typically 8 mA. The 1000's output (pin 19) sinks current from two LED segments, and has a 16-mA drive capability. The TC7117/TC7117A are designed to drive common anode LED displays.

In both devices, the polarity indication is ON for analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

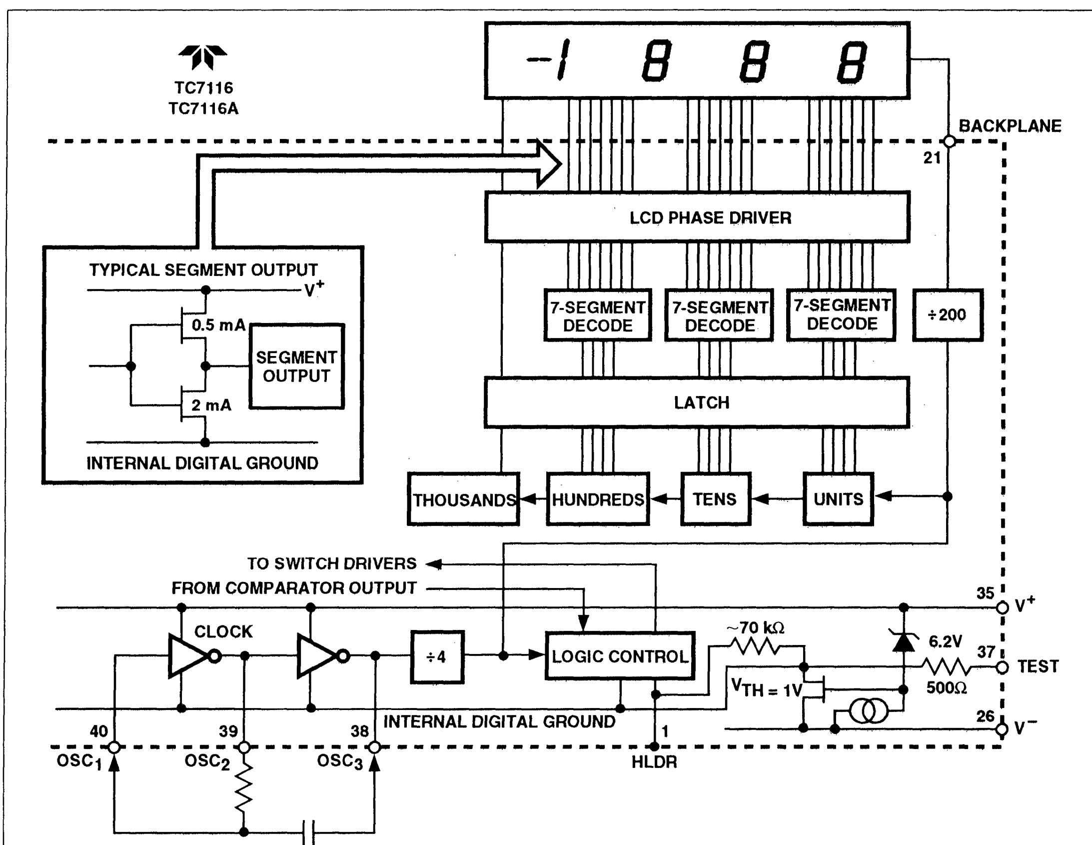


Figure 8 TC7116/TC7116A Digital Section

System Timing

The clocking method used for the TC7116/TC7116A and TC7117/TC7117A is shown in Figure 9. Three clocking methods may be used:

(1) An external oscillator connected to pin 40.
(2) A crystal between pins 39 and 40.
(3) An RC network using all three pins.

The oscillator frequency is ÷4 before it clocks the decade counters. It is then further divided to form the three convert-cycle phases: signal integrate (1000 counts), reference deintegrate (0 to 2000 counts), and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For 3 readings per second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60-Hz pickup, the signal-integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings per second) will reject both 50 Hz and 60 Hz (also 400 Hz and 440 Hz).

HOLD Reading Input

When HLDR is at a logic HIGH the latch will not be updated. Analog-to-digital conversions will continue but will not be updated until HLDR is returned to LOW. To continuously update the display, connect to test (TC7116/TC7116A) or ground (TC7117/TC7117A), or disconnect. This input is CMOS compatible with 70 kΩ typical resistance to test (TC7116/TC7116A) or ground (TC7117/TC7117A).

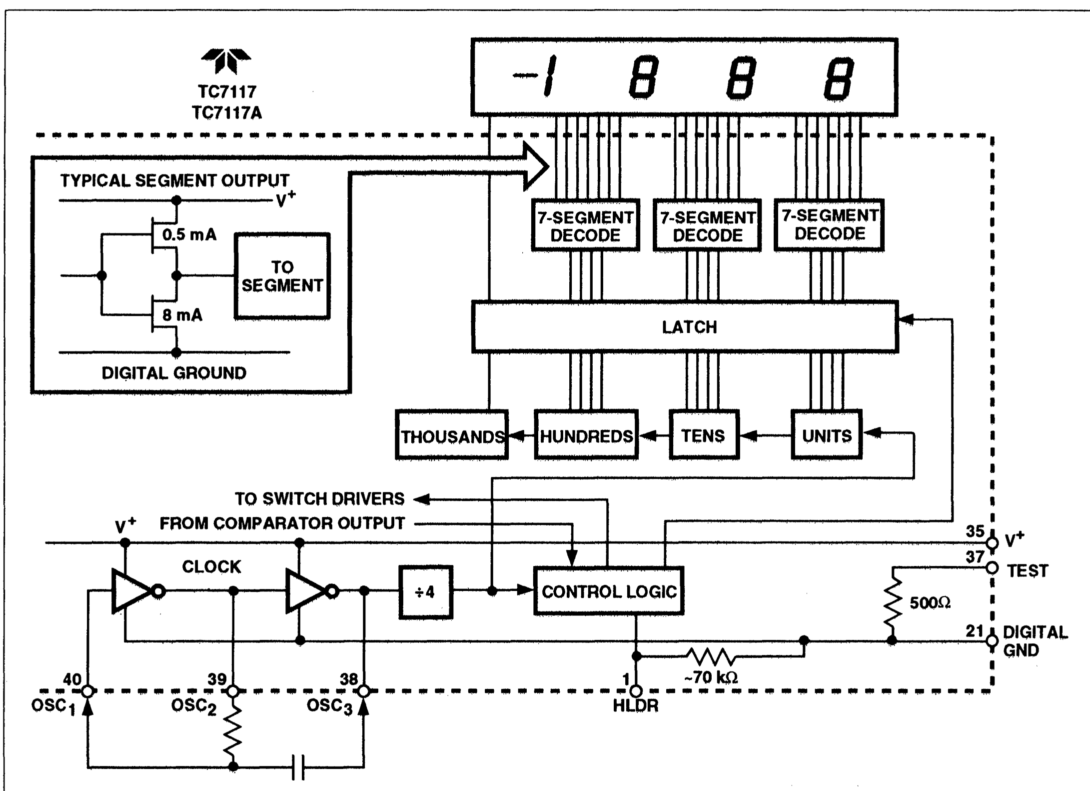


Figure 9 TC7117/TC7117A Digital Section

COMPONENT VALUE SELECTION

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on system noise. For 200 mV full scale, where noise is very important, a 0.47 μF capacitor is recommended. On the 2V scale, a 0.047 μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e., the V_{IN}^- pin is not at analog common), and a 200-mV scale is used, a larger value is required to prevent roll-over error. Generally, 1 μF will hold the roll-over error to 0.5 count in this instance.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approximately 0.3V from either supply). In the TC7116/TC7116A or the TC7117/TC7117A, when the analog common is used as a reference, a nominal ±2V full- scale integrator swing is acceptable. For the TC7117/TC7117A, with ±5V supplies and analog common tied to supply ground, a ±3.5V to ±4V swing is nominal. For 3 readings per second (48 kHz clock), nominal values for C_{INT} are 0.22 μ1F and 0.10 μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 470 kΩ is near optimum and, similarly, 47 kΩ for 200 mV full scale.

Oscillator Components

For all frequency ranges, a 100-kΩ resistor is recommended; the capacitor is selected from the equation:

$$f = \frac{45}{RC}.$$

For 48 kHz clock (3 readings per second), C = 100 pF.

Reference Voltage

To generate full-scale output (2000 counts), the analog input required is $V_{IN} = 2\ V_{REF}$. Thus, for the 200 mV and 2V scale, V_{REF} should equal 100 mV and 1V, respectively. In many applications, where the ADC is connected to a transducer, a scale factor exists between the input voltage and the digital reading. For instance, in a measuring system the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 200 mV, the designer should use the input voltage directly and select V_{REF} = 350 mV. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The TC7117/TC7117A, with ±5V supplies, can accept input signals up to ±4V. Another advantage of this system is when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^+ and analog common, and the variable (or fixed) offset voltage between analog common and V_{IN}^-.

TC7117/TC7117A POWER SUPPLIES

The TC7117/TC7117A are designed to operate from ±5V supplies. However, if a negative supply is not available, it can be generated with a TC7660 DC-to-DC converter and two capacitors. Figure 10 shows this application.

In selected applications, negative supply is not required. The conditions to use a single +5V supply are:

(1) The input signal can be referenced to the center of the common-mode range of the converter.
(2) The signal is less than ±1.5V.
(3) An external reference is used.

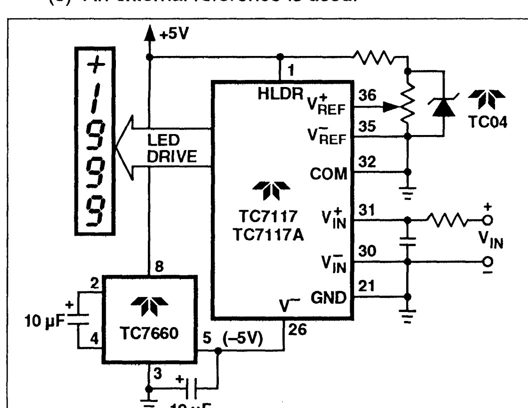


Figure 10 Negative Power Supply Generation With TC7660

TYPICAL APPLICATIONS

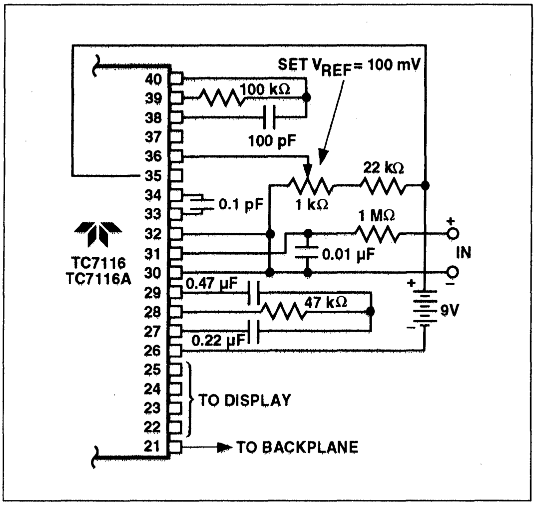


Figure 11 TC7116/TC7116A Using the Internal Reference (200 mV Full Scale, 3 RPS)

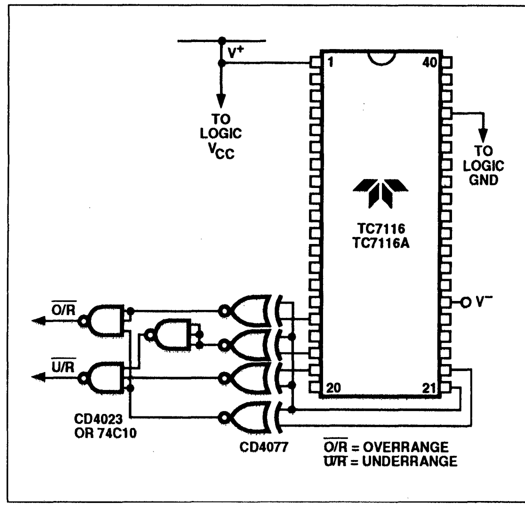


Figure 13 Circuit for Developing Underrange and Overrange Signals from TC7116/TC7116A Outputs

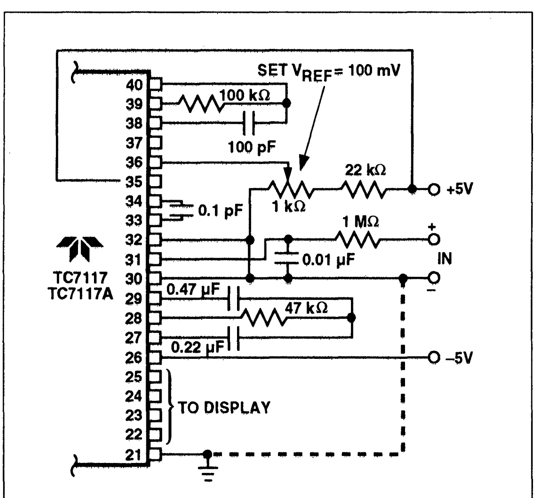


Figure 12 TC7117/TC7117A Internal Reference (200 mV Full Scale, 3 RPS, V_{IN} Tied to GND for Single-Ended Inputs.)

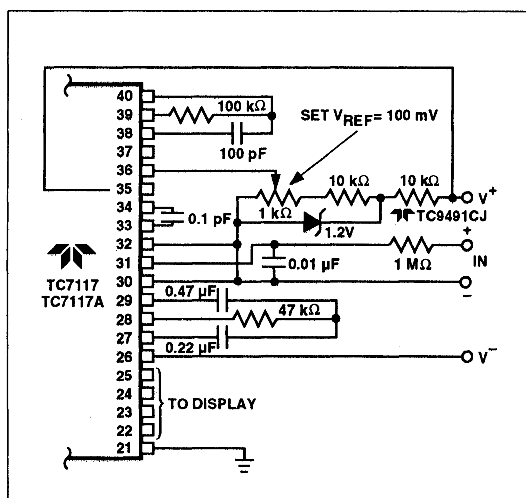


Figure 14 TC7117/TC7117A With a 1.2V External Band-Gap Reference (V_{IN} Tied to Common)

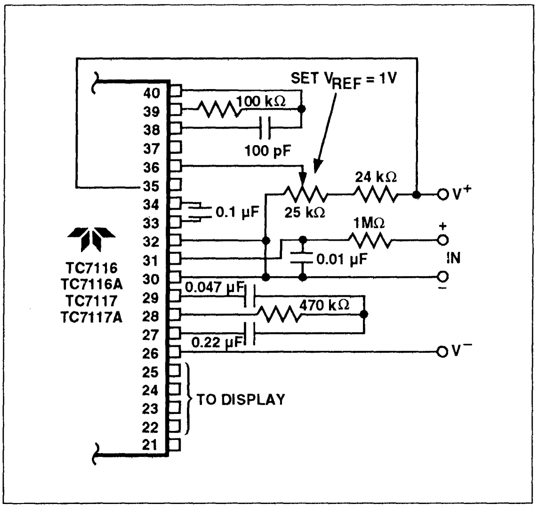


Figure 15 Recommended Component Values for 2V Full Scale (TC7116/TC7116A and TC7117/TC7117A)

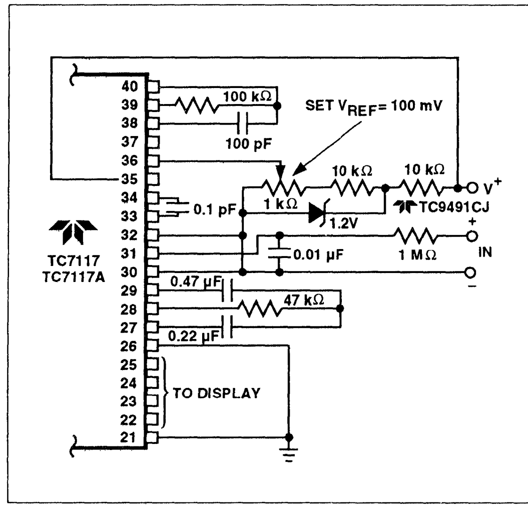


Figure 16 TC7117/TC7117A Operated from Single +5V Supply (An External Reference Must Be Used in This Application.)

APPLICATIONS INFORMATION

The TC7117/TC7117A sink the LED display current, causing heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation, such variations can be reduced. By reducing the LED common anode voltage, the TC7117/TC7117A package power dissipation is reduced.

Figure 17 is a curve-tracer display showing the relationship between output current and output voltage for typical TC7117CPL/TC7117ACPL devices. Since a typical LED has 1.8V across it at 8 mA and its common anode is connected to +5V, the TC7117/TC7117A output is at 3.2V (Point A, Figure 17). Maximum power dissipation is 8.1 mA × 3.2V × 24 segments = 622 mW.

However, notice that once the TC7117/TC7117A's output voltage is above 2V, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7V (Point B Figure 17) results in 7.7 mA of LED current, only a 5% reduction. Maximum power dissipation is now only 7.7 mA × 2.5V × 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1V (Point C) reduces LED current by 10% (7.3 mA), but power dissipation by 38% (7.3 mA × 2.2V × 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Figure 18 shows two ways: Either a 5.1Ω, 1/4W resistor, or a 1A diode placed in series with the display (but not in series with the TC7117/TC7117A). The resistor reduces the TC7117/TC7117A's output voltage (when all 24 segments are ON) to Point C of Figure 17. When segments turn off, the output voltage will increase. The diode, however, will result in a relatively steady output voltage, around Point B.

In addition to limiting maximum power dissipation, the resistor reduces change in power dissipation as the display changes. The effect is caused by the fact that, as fewer segments are ON, each ON output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display), the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

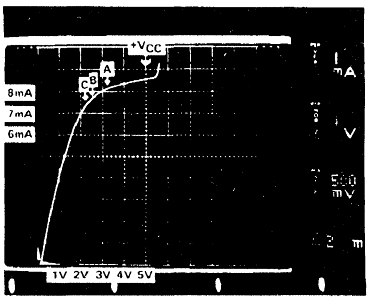


Figure 17 TC7117/TC7117A Output Current vs Output Voltage

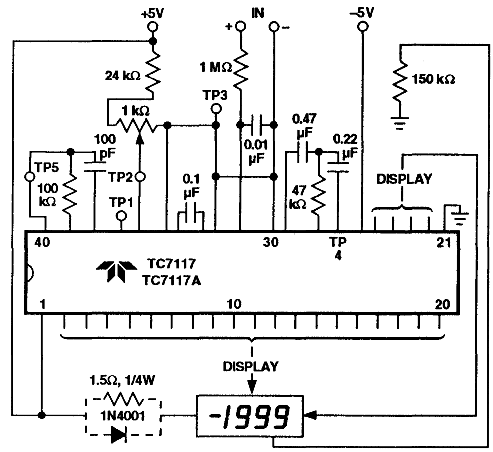


Figure 18 Diode or Resistor Limits Package Power Dissipation

3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

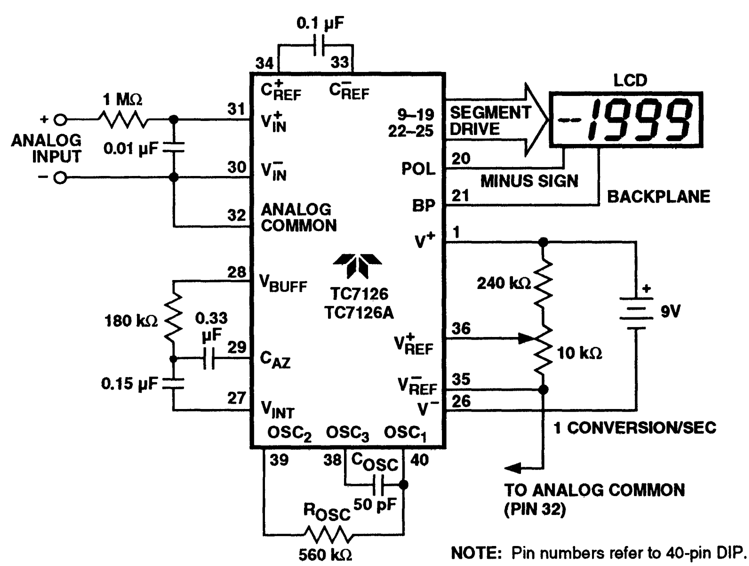
FEATURES

- Low Temperature Drift Internal Reference
  - TC7126 .... 80 ppm/°C Typ
  - TC7126A .... 35 ppm/°C Typ
- Guaranteed Zero Reading With Zero Input
- Low Noise .... 15 µV_{P-P}
- High Resolution 0.05%
- Wide Dynamic Range .... 72 dB
- Low Input Leakage Current .... 1 pA Typ
  10 pA Max
- Direct LCD Drive — No External Components
- Precision Null Detectors With True Polarity at Zero
- High-Impedance Differential Input
- Convenient 9V Battery Operation With Low Power Dissipation .... 500 µΩ Typ
  900 µΩ Max
- Internal Clock Circuit
- Improved Drop-In Replacement for ICL7126 That Offers Low Analog Common Voltage Drift
- Available in Compact Flat Package
- Industrial Temperature Range Device Available

TYPICAL APPLICATIONS

- Thermometry
- Bridge Readouts
  - — Strain Gauges
  - — Load Cells
  - — Null Detectors
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity/Level
  - — Humidity
  - — Position
- Digital Scales
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Gaussometers
- Photometers

TYPICAL OPERATING CIRCUIT



NOTE: Pin numbers refer to 40-pin DIP.

TC7126
TC7126A

GENERAL DESCRIPTION

The TC7126A features a precision, low-drift internal voltage reference and is functionally identical to the TC7126. A low-drift external reference is not normally required with the TC7126A.

The TC7126A is a 3-1/2 digit CMOS analog-to-digital converter (ADC) containing all the active components necessary to construct a 0.05% resolution measurement system. Seven-segment decoders, digit and polarity drivers, voltage reference, and clock circuit are integrated on-chip. The TC7126A directly drives a liquid crystal display (LCD), and includes a backplane driver.

A low-cost, high-resolution indicating meter requires only a display, four resistors, and four capacitors. The TC7126A's extremely low power drain and 9V battery operation make it ideal for portable applications.

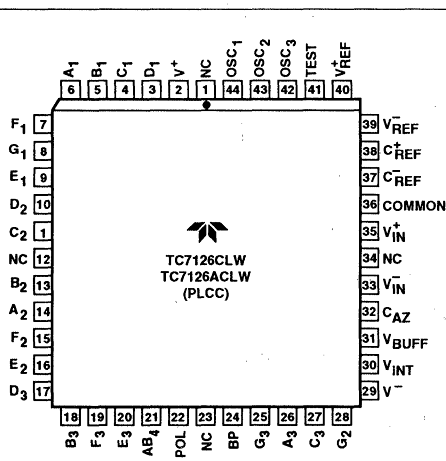
The TC7126A reduces linearity error to less than 1 count. Roll-over error (the difference in readings for equal magnitude but opposite polarity input signals) is below ±1 count. High-impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The 15 $\mu V_{P\text{-}P}$ noise performance guarantees a "rock solid" reading, and the auto-zero cycle guarantees a zero display reading with a 0V input.

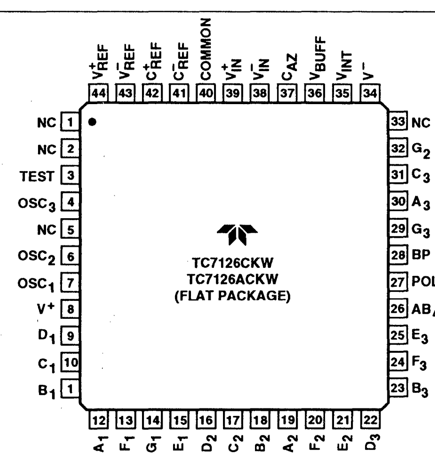
The TC7126A's dual-slope conversion technique automatically rejects interference signals if the converter's integration time is set to a multiple of the interference period. This is especially useful in industrial measurement environments where 50-Hz, 60-Hz, and 400-Hz line frequency signals are present.

ORDERING INFORMATION

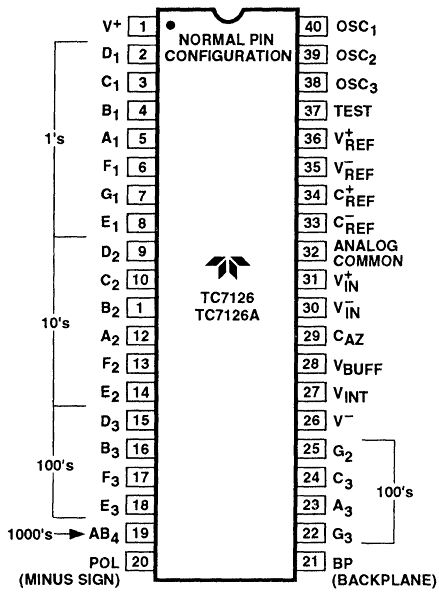
Part No.	Package	Pin Layout	Temp Range	Ref Tempco (Max)
TC7126CPL	40-Pin Plastic DIP	Normal	0°C to +70°C	80 ppm/°C
TC7126ACPL	40-Pin Plastic DIP	Normal	0°C to +70°C	35 ppm/°C
TC7126RCPL	40-Pin Plastic DIP	Reversed	0°C to +70°C	80 ppm/°C
TC7126ARCPL	40-Pin Plastic DIP	Reversed	0°C to +70°C	35 ppm/°C
TC7126IPL	40-Pin Plastic DIP		–25°C to +85°C	80 ppm/°C
TC7126CJL	40-CerDIP		0°C to +70°C	80 ppm/°C
TC7126IJL	40-CerDIP		–25°C to +85°C	80 ppm/°C
TC7126AIJL	40-CerDIP		–25°C to +85°C	35 ppm/°C
TC7126CBQ	60-Pin Plastic Flat		0°C to +70°C	80 ppm/°C
TC7126ACBQ	60-Pin Plastic Flat		0°C to +70°C	35 ppm/°C
TC7126CKW	44-Pin Plastic Flat		0°C to +70°C	80 ppm/°C
TC7126ACKW	44-Pin Plastic Flat		0°C to +70°C	35 ppm/°C
TC7126CLW	44-Pin PLCC		0°C to +70°C	80 ppm/°C
TC7126ACLW	44-Pin PLCC		0°C to +70°C	35 ppm/°C

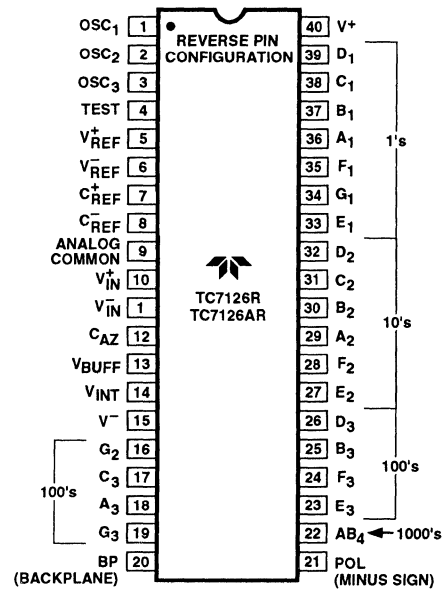
PIN CONFIGURATIONS



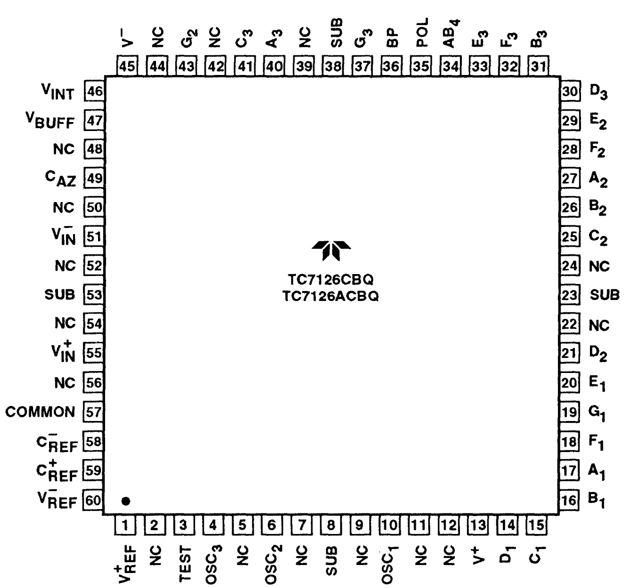


PIN CONFIGURATIONS (Cont.)





NC = NO INTERNAL CONNECTION



NOTES:
1. NC = No internal connection.
2. Pins 8, 23, 38 and 53 are connected to the die substrate. The potential at these pins is approximately V^+. No external connections should be made.

TC7126
TC7126A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) .... +15V
Analog Input Voltage (Either Input) (Note 1) .... V^+ to V^-
Reference Input Voltage (Either Input) .... V^+ to V^-
Clock Input .... TEST to V^+
Operating Temperature Range
C Devices .... 0°C to +70°C
I Devices .... −25°C to +85°C
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... +300°C

Power Dissipation (Note 2)
CerDIP (J) .... 1000 mW
Plastic DIP (P) .... 800 mW
Plastic Flat Package, PLCC (B, K, L) .... 500 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = +9V, f_{CLK} = 16 kHz, and T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
	Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV	−000.0	±000.0	+000.0	Digital Reading
	Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C	—	0.2	1	µV/°C
	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
NL	Linearity Error	Full Scale = 200 mV or 2V Max Deviation From Best Fit Straight Line	−1	±0.2	1	Count
	Roll-Over Error	$-V_{IN}$ = $+V_{IN}$ ≈ 200 mV	−1	±0.2	1	Count
e_N	Noise	V_{IN} = 0V, Full Scale = 200 mV	—	15	—	μV_{P-P}
I_L	Input Leakage Current	V_{IN} = 0V	—	1	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200 mV	—	50	—	µV/V
	Scale Factor Temperature Coefficient	V_{IN} = 199 mV, 0°C ≤ T_A ≤ +70°C Ext Ref Temp Coeff = 0 ppm/°C	—	1	5	ppm/°C
Analog Common						
V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ 0°C ≤ T_A ≤ +70°C ("C" Devices):				
		TC7126	—	80	—	ppm/°C
		TC7126A	—	35	75	ppm/°C
		−25°C ≤ T_A ≤ +85°C ("I" Device): TC7126A	—	35	100	ppm/°C
V_C	Analog Common Voltage	250 kΩ Between Common and V^+	2.7	3.05	3.35	V
LCD Drive						
V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
V_{BD}	LCD Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
Power Supply						
I_S	Power Supply Current	V_{IN} = 0V, V^+ to V^- = 9V (Note 6)	—	55	100	µA

NOTES:
1. Input voltage may exceed supply voltages when input current is limited to 100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to PC board.
3. Refer to "Differential Input" discussion.
4. Backplane drive is in-phase with segment drive for "off" segment and 180° out-of-phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
5. See "Typical Operating Circuit."
6. During auto-zero phase, current is 10–20 µA higher. A 48 kHz oscillator increases current by 8 µA (typical). Common current not included.

PIN DESCRIPTION

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the tens display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP	Backplane drive output.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build-up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See "Integrating Capacitor" section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 180 kΩ resistor for a 200 mV full-scale range and a 1.8 MΩ resistor for a 2V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.33 μF capacitor for 200 mV full scale, and a 0.033 μF capacitor for 2V full scale. See paragraph on auto-zero capacitor for more details.
30	(11)	51	V_{IN}^-	The low input signal is connected to this pin.
31	(10)	55	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	57	ANALOG COMMON	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on analog common for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.

PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
34	(7)	59	C_{REF}^+	A 0.1 µF capacitor is used in most applications. If a large common-mode voltage exists (for example, the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1 µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.
36	(5)	1	V_{REF}^+	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full scale. Place 1V between pins 35 and 36 for 2V full scale. See paragraph on reference voltage.
37	(4)	3	TEST	Lamp test. When pulled high (to V+), all segments will be turned on and the display should read –1888. It may also be used as a negative supply for externally-generated decimal points. See paragraph under test for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39 and 38 make up the oscillator section. For a 48 kHz clock (3 readings per second), connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC7126A is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following detailed TC7126A operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period (t_{SI}), measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (t_{RI}).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

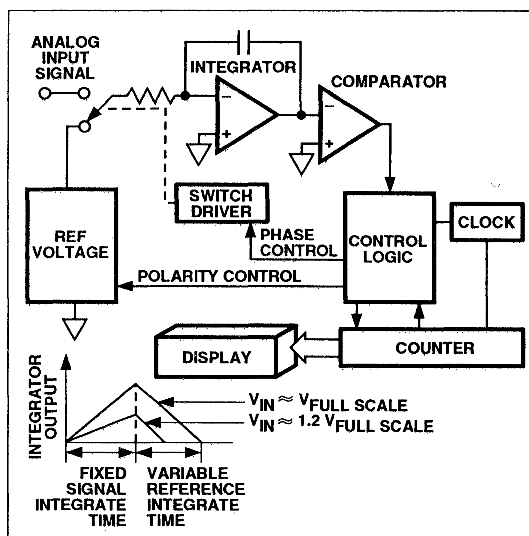


Figure 1 Basic Dual-Slope Converter

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\, t_{RI}}{RC},$$

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

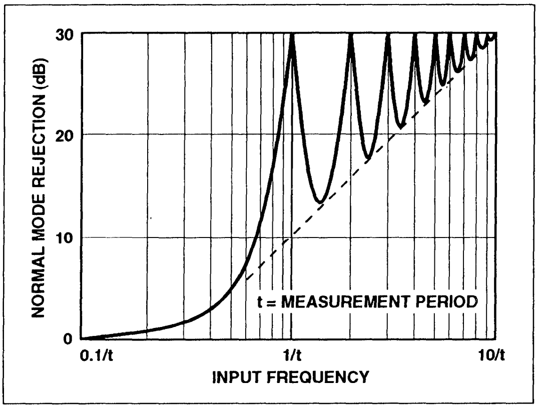


Figure 2 Normal-Mode Rejection of Dual-Slope Converter

For a constant V_{IN}:

$$V_{IN} = V_R \left[\frac{t_{RI}}{t_{SI}} \right].$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50 Hz/60 Hz power line period.

ANALOG SECTION

In addition to the basic integrate and deintegrate dual-slope cycles discussed above, the TC7126A design incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three phases:

(1) Auto-zero phase
(2) Signal integrate phase
(3) Reference integrate phase

Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero phase residual is typically 10 μV to 15 μV.

The auto-zero cycle length is 1000 to 3000 clock periods.

Signal Integration Phase

The auto-zero loop is entered and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The TC7126A signal integration period is 1000 clock periods, or counts. The externally-set clock frequency is ÷4 before clocking the internal counters. The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 1000,$$

where f_{OSC} = external clock frequency.

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Phase

The third phase is reference integrate, or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously-charged reference capacitor. Circuitry within the chip ensures the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 internal clock periods. The digital reading displayed is:

$$1000 \frac{V_{IN}}{V_{REF}}$$

DIGITAL SECTION

The TC7126A contains all the segment drivers necessary to directly drive a 3-1/2 digit LCD. An LCD backplane driver is included. The backplane frequency is the external clock frequency ÷800. For 3 conversions per second the backplane frequency is 60 Hz with a 5V nominal amplitude.

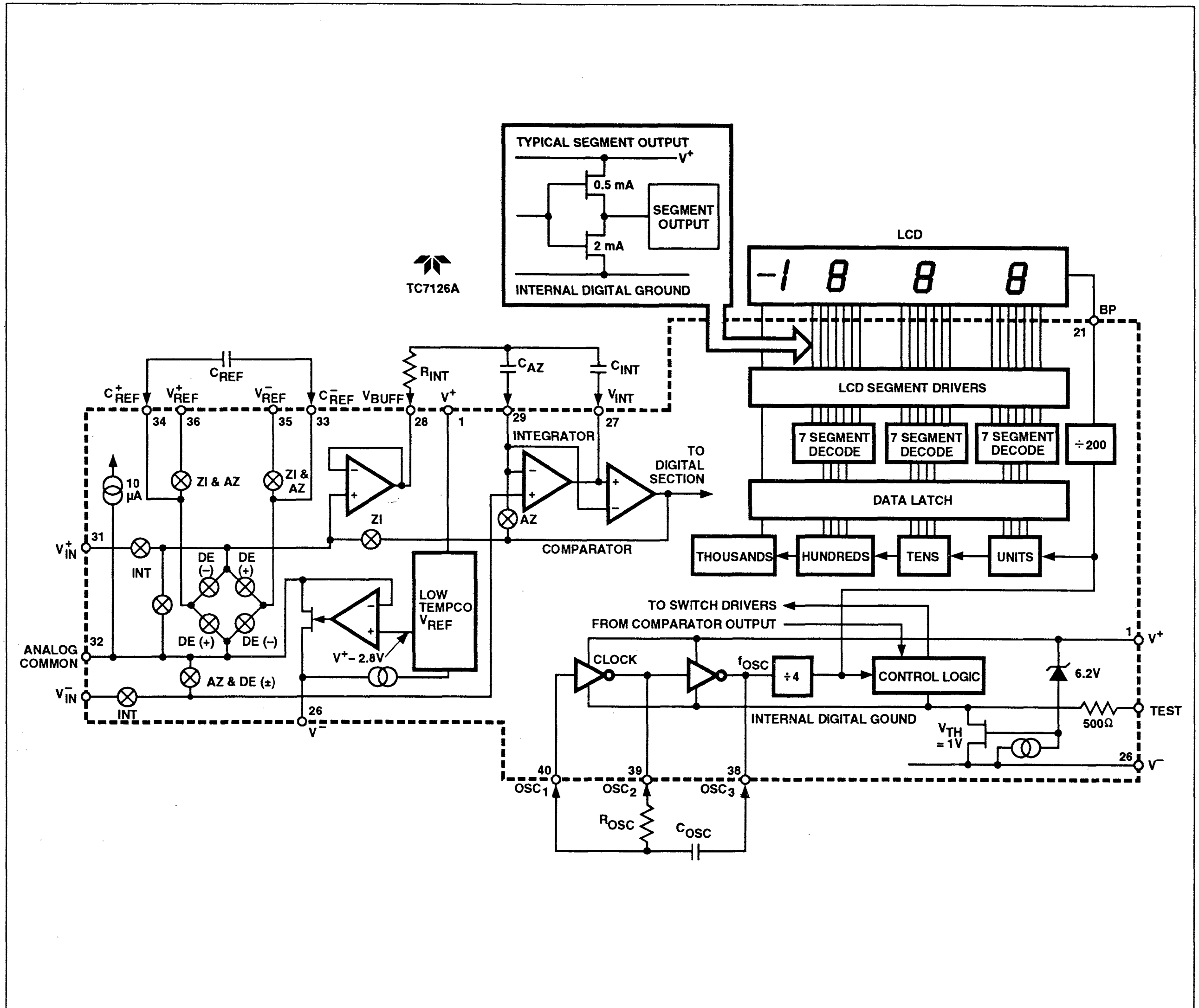


Figure 3 TC7126A Block Diagram

When a segment driver is in-phase with the backplane signal, the segment is "OFF." An out-of-phase segment drive signal causes the segment to be "ON," or visible. This AC drive configuration results in negligible DC voltage across each LCD segment, ensuring long LCD life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed, this indicator would reverse.

On the TC7126A, when the test pin is pulled to V^+, all segments are turned "ON." The display reads –1888. During this mode, LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes; LCDs may be destroyed if operated with DC levels for extended periods.

The display font and segment drive assignment are shown in Figure 4.

System Timing

The oscillator frequency is ÷4 prior to clocking the internal decade counters. The three-phase measurement cycle takes a total of 4000 counts (16,000 clock pulses). The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

(1) Auto-zero phase: 1000 to 3000 counts (4000 to 12,000 clock pulses)

For signals less than full scale, the auto-zero phase is assigned the unused reference integrate time period.

(2) Signal integrate: 1000 counts (4000 clock pulses)

This time period is fixed. The integration period is:

$$t_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right],$$

where f_{OSC} is the externally-set clock frequency.

(3) Reference integrate: 0 to 2000 counts (0 to 8000 clock pulses)

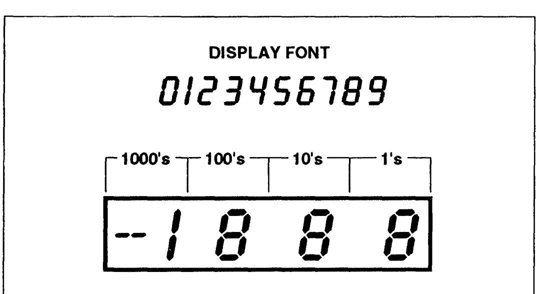


Figure 4 Display Font and Segment Assignment

The TC7126A is a drop-in replacement for the TC7126 and ICL7126 that offers a greatly improved internal reference temperature coefficient. No external component value changes are required to upgrade existing designs.

COMPONENT VALUE SELECTION

Auto-Zero Capacitor (C_{AZ})

The C_{AZ} size has some influence on system noise. A 0.33 µF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 µV. A 0.033 µF capacitor is adequate for 2V full-scale applications. A Mylar-type dielectric capacitor is adequate.

Reference Voltage Capacitor (C_{REF})

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate phase is stored on C_{REF}. A 0.1 µF capacitor is acceptable when V_{REF}^- is tied to analog common. If a large common-mode voltage exists ($V_{REF}^- \neq$ analog common) and the application requires a 200 mV full scale, increase C_{REF} to 1 µF. Roll-over error will be held to less than 0.5 count. A Mylar-type dielectric capacitor is adequate.

Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TC7126A's superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case, a ±2V full-scale integrator output swing is satisfactory. For 3 readings per second (f_{OSC} = 48 kHz), a 0.047 µF value is suggested. For 1 reading per second, 0.15 µF is recommended. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}},$$

where: f_{OSC} = Clock frequency at pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing.

At 3 readings per second, a 750Ω resistor should be placed in series with C_{INT}. This increases accuracy by compensating for comparator delay. C_{INT} must have low dielectric absorption to minimize roll-over error. An inexpensive polypropylene capacitor is recommended.

Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 6 μA. The integrator and buffer can supply 1 μA drive current with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that PC board leakage currents induce errors. For a 200 mV full scale, R_{INT} is 180 kΩ. A 2V full scale requires 1.8 MΩ.

Component Value	Nominal Full-Scale Voltage 200 mV	2V
C_{AZ}	0.33 μF	0.033 μF
R_{INT}	180 kΩ	1.8 MΩ
C_{INT}	0.047 μF	0.047 μF

NOTE: f_{OSC} = 48 kHz (3 readings per sec).

Oscillator Components

C_{OSC} should be 50 pF; R_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC} .$$

For a 48 kHz clock (3 conversions per second), R = 180 kΩ.

Note that f_{OSC} is ÷4 to generate the TC7126A's internal clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings per second) will reject both 50 Hz and 60 Hz (also 400 Hz and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200 mV	100 mV
2V	1V

*$V_{FS} = 2\ V_{REF}$.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output for 2000 lb/in.^{2} is 400 mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used where a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature-measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

DEVICE PIN FUNCTIONAL DESCRIPTION

(Pin Numbers Refer to 40-Pin DIP)

Differential Signal Inputs

V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30)

The TC7126A is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). Typical range is V^+ –1V to V^- +1V. Common-mode voltages are removed from the system when the TC7126A operates from a battery or floating power source (isolated from measured system), and V_{IN}^- is connected to analog common (V_{COM}). (See Figure 5.)

In systems where common-mode voltages exist, the TC7126A's 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (see Figure 6.) For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increased linearity error.

Differential Reference

V_{REF}^+ (Pin 36), V_{REF}^- (Pin 35)

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent roll-over type errors being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance.

The TC7126A offers a significantly improved analog common temperature coefficient. This potential provides a very stable voltage, suitable for use as a voltage reference. The temperature coefficient of analog common is typically 35 ppm/°C for the TC7126A and 80 ppm/°C for the TC7126.

ANALOG COMMON (Pin 32)

The analog common pin is set at a voltage potential approximately 3V below V^+. The potential is guaranteed to be between 2.7V and 3.35V below V^+. Analog common is tied internally to an N-channel FET capable of sinking 100 μA. This FET will hold the common line at 3V should an

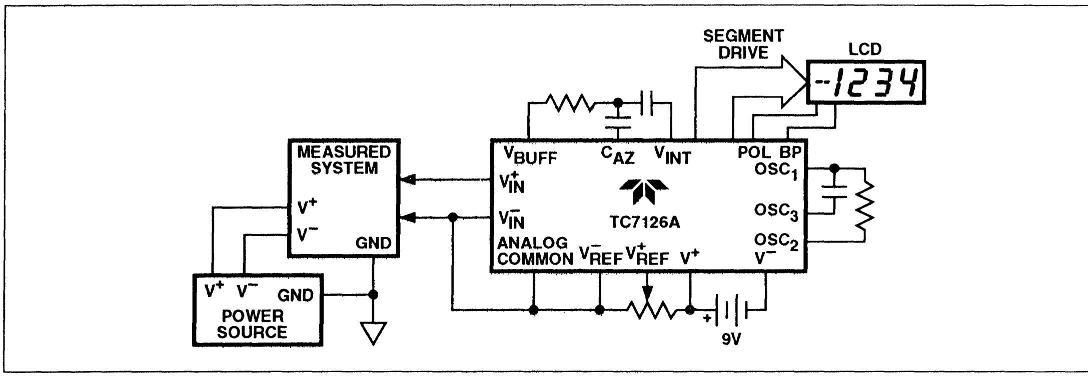


Figure 5 Common-Mode Voltage Removed in Battery Operation With V_{IN} = Analog Common

external load attempt to pull the common line toward V^+. Analog common source current is limited to 1 µA. Therefore, analog common is easily pulled to a more negative voltage (i.e., below V^+ −3V).

The TC7126A connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero phase. During the reference-integrate phase, V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists, but is rejected by the converter's 86 dB common-mode rejection ratio. In battery operation, analog common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference, or common point. The TC7126A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC7126A's power source. The analog

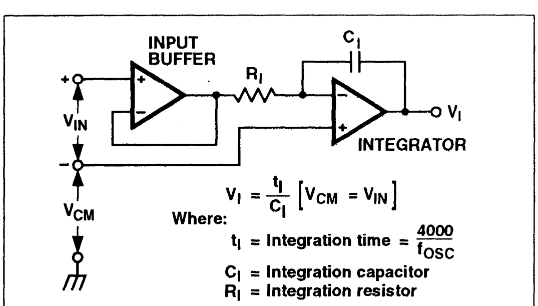


Figure 6 Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)

common potential of V^+ −3V gives a 7V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and a 15Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- > 7V$), analog common is a very stable potential with excellent temperature stability (typically 35 ppm/°c). This potential can be used to generate the TC7126A's reference voltage. An external voltage reference will be unnecessary in most cases because of the 35 ppm/°C temperature coefficient. See "TC7126A Internal Voltage Reference" discussion.

TEST (Pin 37)

The test pin potential is 5V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally-generated negative logic supply through a 500Ω resistor. The test pin load should not be more than 1 mA. See "Digital Section" for additional information on using test as a negative digital logic supply.

If test is pulled high (to V^+), all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes. With TEST= V^+, the LCD segments are impressed with a DC voltage which will destroy the LCD.

TC7126A Internal Voltage Reference

The TC7126A's analog common voltage temperature stability has been significantly improved (Figure 7). The "A" version of the industry-standard TC7126 device allows users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 10 shows analog common supplying necessary voltage reference for the TC7126A.

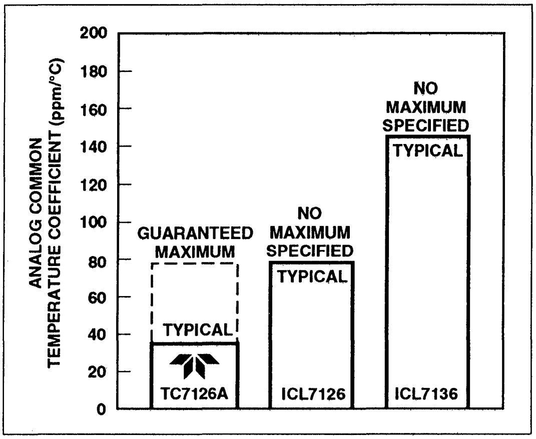


Figure 7 Analog Common Temperature Coefficient

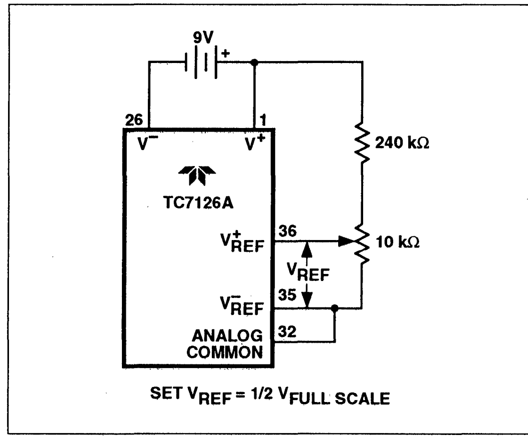


Figure 8 TC7126A Internal Voltage Reference Connection

APPLICATIONS INFORMATION

Liquid Crystal Display Sources

Several manufacturers supply standard LCDs to interface with the TC7126A 3-1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415-347-9916	FE 0801, FE 0203
VGI, Inc.	1800 Vernon St., Ste. 2 Roseville, CA 95678 916-783-7878	I1048, I1126
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414-648-2361	3902, 3933, 3903

***NOTE:** Contact LCD manufacturer for full product listing/specifications.

Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5V below V^+.

Flat Package

The TC7126A is available in an epoxy 60-pin formed leads flat package. A test socket for the TC7126ACBQ device is available:

Part No. IC 51-42
Manufacturer: Yamaichi
Distribution: Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, CA 94043
(415) 856-9332

Ratiometric Resistance Measurements

The TC7126A's true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately-defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000.$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

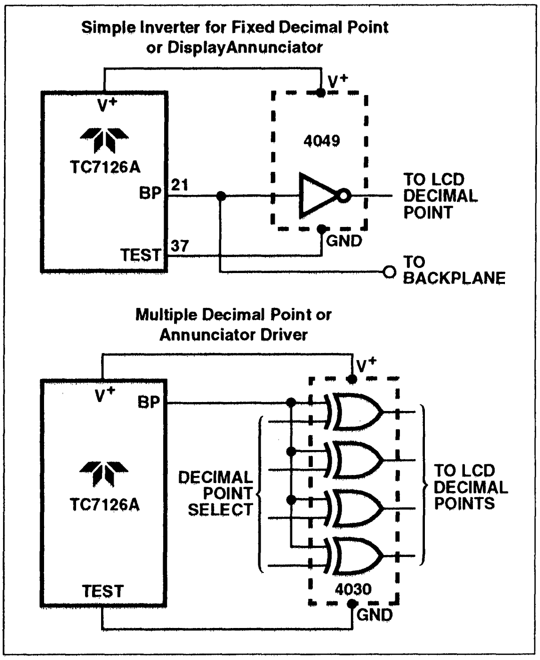


Figure 9 Decimal Point and Annunciator Drives

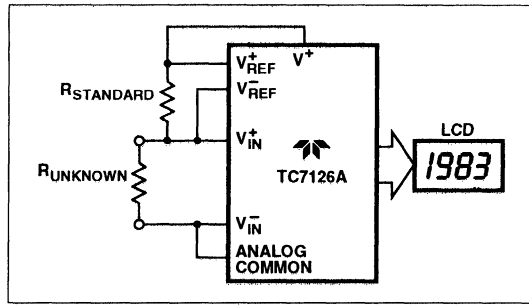


Figure 10 Low Parts Count Ratiometric Resistance Measurement

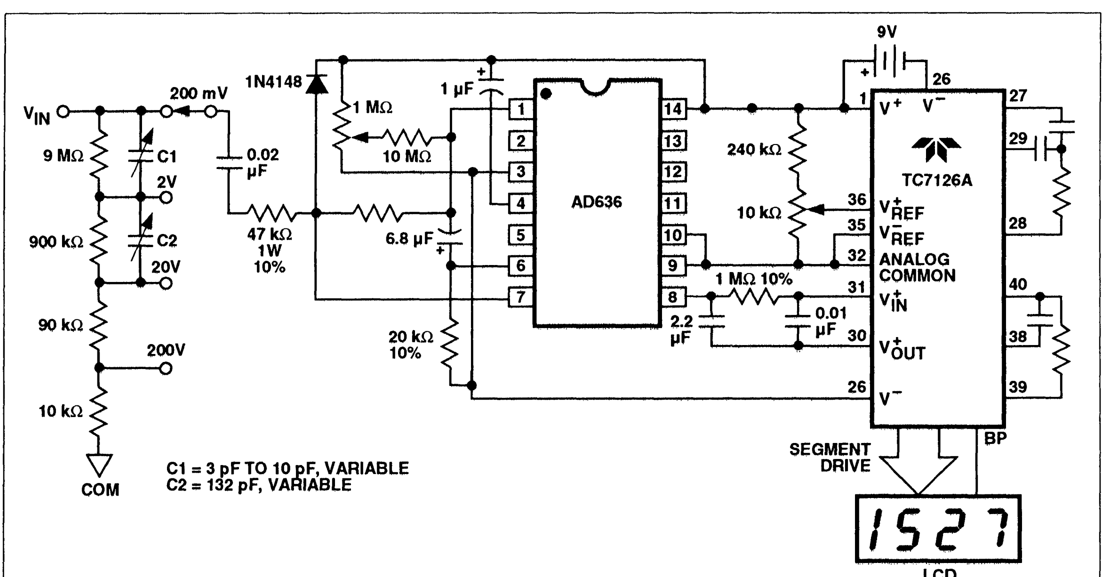


Figure 11 3-1/2 Digit True RMS AC DMM

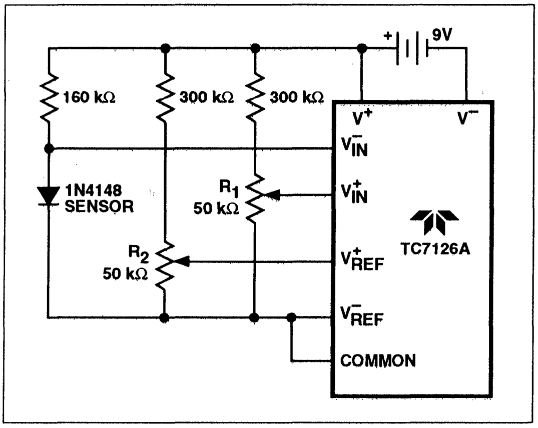


Figure 12 Temperature Sensor

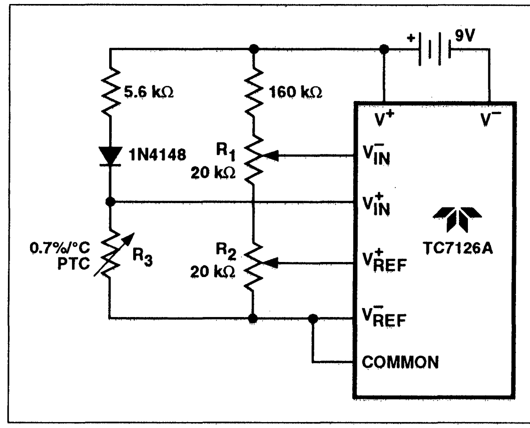


Figure 13 Positive Temperature Coefficient Resistor Temperature Sensor

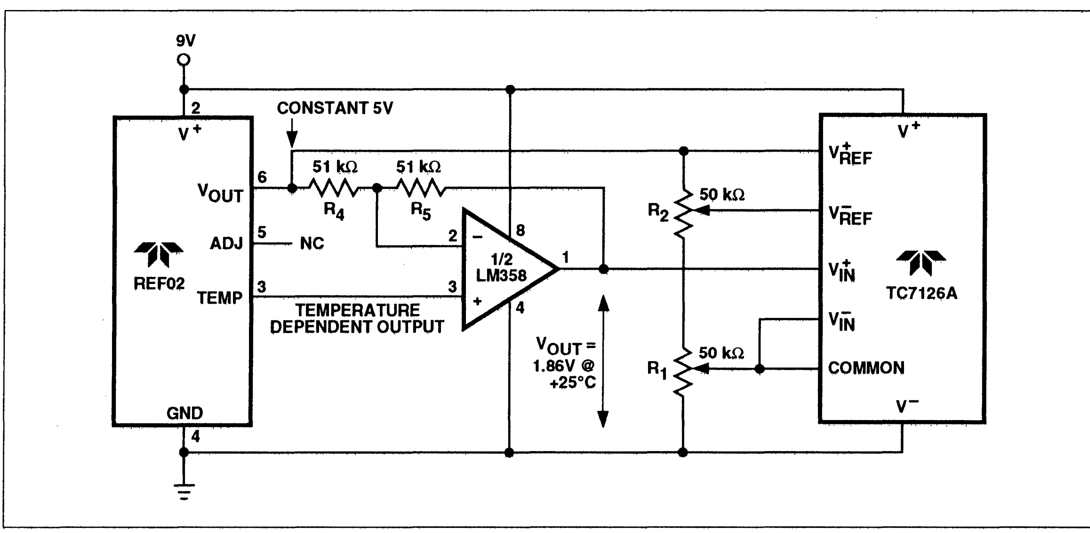


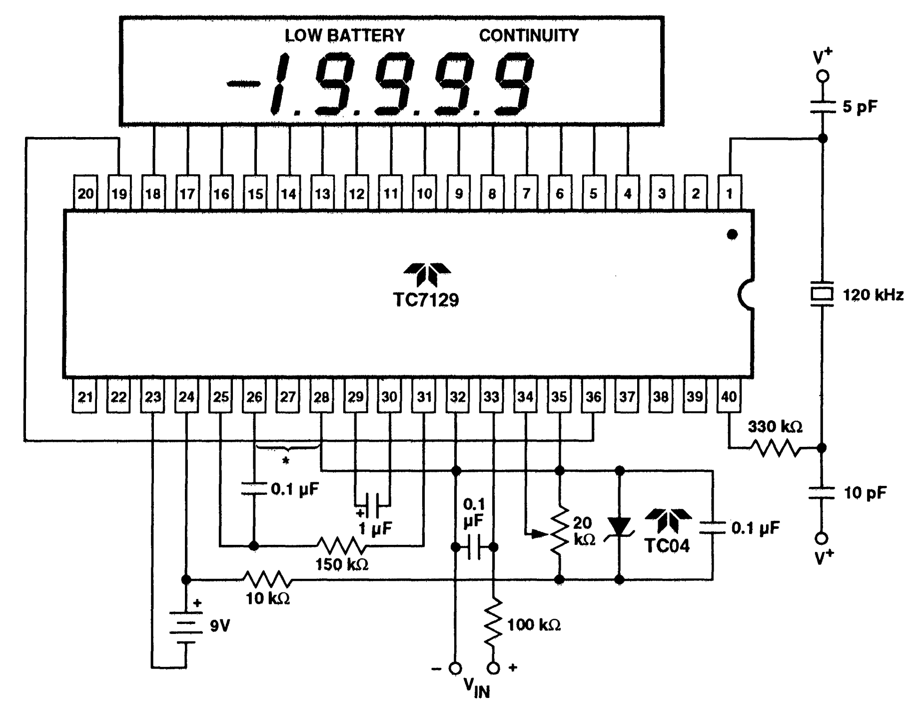
Figure 14 Integrated Circuit Temperature Sensor

4-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER WITH ON-CHIP LCD DRIVERS

FEATURES

- Count Resolution .... ±19,999
- Resolution on 200 mV Scale .... 10 µV
- True Differential Input and Reference
- Low Power Consumption .... 500 µA at 9V
- Direct LCD Driver for:
  - 4-1/2 Digits
  - Decimal Points
  - Low-Battery Indicator
  - Continuity Indicator
- Overrange and Underrange Outputs
- Range Select Input 10:1
- High Common-Mode Rejection Ratio .... 110 dB
- External Phase Compensation Not Required

TYPICAL OPERATING CIRCUIT



* NOTE: RC network between pins 26 and 28 is not required.

TC7129

GENERAL DESCRIPTION

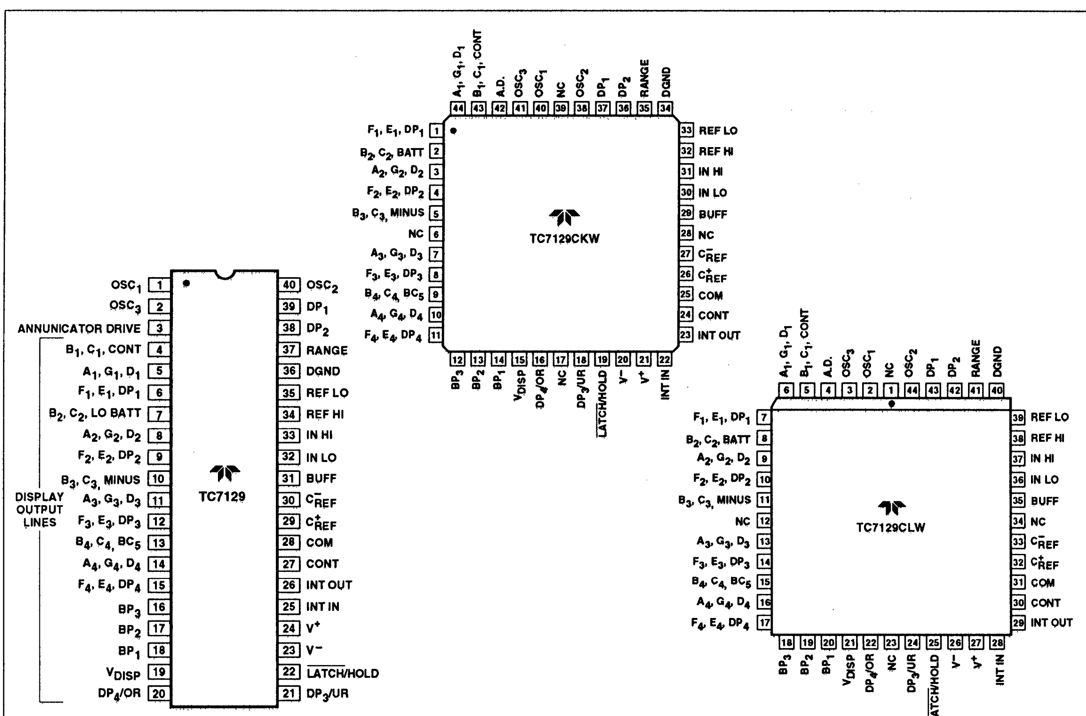
The TC7129 is a 4-1/2 digit analog-to-digital converter (ADC) that directly drives a multiplexed liquid crystal display (LCD). Fabricated in high-performance, low-power CMOS, the TC7129 ADC is designed specifically for high-resolution, battery-powered digital multimeter applications. A complete analog measurement instrument requires only the TC7129, a few passive components, a reference, an LCD, and a battery. Power consumption is low, only 500 μA from a 9V battery. The traditional dual-slope method of A/D conversion has been enhanced with a successive integration technique to produce readings accurate to better than 0.005% of full scale, and resolution down to 10 μV per count.

The TC7129 includes features important to multimeter applications. It detects and indicates low-battery condition. A continuity output drives an annunciator on the display, and can be used with an external driver to sound an audible alarm. Overrange and underrange outputs and a range-change input provide the ability to create auto-ranging instruments. For snapshot readings, the TC7129 includes a latch-and-hold input to freeze the present reading. This combination of features makes the TC7129 the ideal choice for full-featured multimeter and digital measurement applications.

ORDERING INFORMATION

Part No.	Pin Layout	Package	Temperature Range
TC7129CPL	Normal	40-Pin Plastic DIP	0°C to +70°C
TC7129RCPL	Reversed	40-Pin Plastic DIP	0°C to +70°C
TC7129CJL	Normal	40-Pin CerDIP	0°C to +70°C
TC7129CKW	Formed	44-Pin Plastic Flat	0°C to +70°C
TC7129CLW	—	44-Pin PLCC	0°C to +70°C
TC7129CBQ	Formed	60-Pin Plastic Flat	0°C to +70°C

PIN CONFIGURATIONS



4-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER WITH ON-CHIP LCD DRIVERS

TC7129

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) .... +15V
Reference Voltage (REF HI or REF LO) .... V^+ to V^-
Input Voltage (IN HI or IN LO) (Note 1) .... V^+ to V^-
V_{DISP} .... V^+ to DGND −0.3V
Digital Input, Pins
1, 2, 19, 20, 21, 22, 27, 37, 39, 40 .... DGND to V^+
Analog Input, Pins 25, 29, 30 .... V^+ to V^-
Power Dissipation Plastic Package (Note 2) .... 800 mW
Operating Temperature Range .... 0°C to +70°C
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Notes: Input voltages may exceed supply voltages, provided input current is limited to ±400 µA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1 mA.
Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V^+ to V^- = 9V, V_{REF} = 1V, T_A = +25°C, f_{CLK} = 120 kHz, unless otherwise indicated. Pin numbers refer to 40-pin DIP.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
	Zero Input Reading	V_{IN} = 0V, 200 mV Scale	−0000	0000	+0000	Counts
	Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C	—	±0.5	—	µV/°C
	Ratiometric Reading	V_{IN} = V_{REF} = 1000 mV, Range = 2V	9997	9999	10000	Counts
	Range Change Accuracy	V_{IN} = 0.1V on Low Range ÷V_{IN} = 1V on High Range	0.9999	1.0000	1.0001	Ratio
RE	Roll-Over Error	$-V_{IN}$ = $+V_{IN}$ = 199 mV	—	1	2	Counts
NL	Linearity Error	200 mV Scale	—	1	—	Counts
CMRR	Common-Mode Rejection Ratio	V_{CM} = 1V, V_{IN} = 0V, 200 mV Scale	—	110	—	dB
CMVR	Common-Mode Voltage Range	V_{IN} = 0V 200 mV Scale	— —	(V^-) +1.5 (V^+) −1	— —	V V
e_N	Noise (Peak-to-Peak Value Not Exceeded 95% of Time)	V_{IN} = 0V 200 mV Scale	—	14	—	μV_{P-P}
I_{IN}	Input Leakage Current	V_{IN} = 0V, Pins 32, 33	—	1	10	pA
	Scale Factor Temperature Coefficient	V_{IN} = 199 mV, 0°C < T_A < +70°C External V_{REF} = 0 ppm/°C	—	2	7	ppm/°C
Power						
V_{COM}	Common Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
	Common Sink Current Common Source Current	ΔCommon = +0.1V ΔCommon = −0.1V	— —	0.6 10	— —	mA µA
DGND	Digital Ground Voltage	V^+ to Pin 36, V^+ to V^- = 9V	4.5	5.3	5.8	V
	Sink Current	ΔDGND = +0.5V	—	1.2	—	mA
	Supply Voltage Range	V^+ to V^-	6	9	12	V
I_S	Supply Current Excluding Common Current	V^+ to V^- = 9V	—	0.5	1	mA
f_{CLK}	Clock Frequency		—	120	360	kHz
	V_{DISP} Resistance	V_{DISP} to V^+	—	50	—	kΩ
	Low-Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
Digital						
	Continuity Comparator Threshold Voltages	V_{OUT} Pin 27 = High V_{OUT} Pin 27 = Low	100 —	200 200	— 400	mV mV
	Pull-Down Current	Pins 37, 38, 39	—	2	10	µA
	"Weak Output" Current Sink/Source	Pins 20, 21 Sink/Source Pin 27 Sink/Source	— —	3/3 3/9	— —	µA µA
	Pin 22 Source Current Pin 22 Sink Current		— —	40 3	— —	µA µA

TC7129

PIN DESCRIPTIONS (Pin Numbers Refer to 40-Pin DIP)

Pin	Name	Function
1	OSC_1	Input to first clock inverter.
2	OSC_3	Output of second clock inverter.
3	AUNUNCIATOR DRIVE	Backplane square-wave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, D_4, G_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP_3	Backplane #3 output to display.
17	BP_2	Backplane #2 output to display.
18	BP_1	Backplane #1 output to display.
19	V_{DISP}	Negative rail for display drivers.
20	DP_4/OR	Input: When HI, turns on most significant decimal point. Output: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	Input: Second most significant decimal point on when HI. Output: Pulled HI when result count is less than ±1000.
22	$\overline{LATCH}$/HOLD	Input: When floating, ADC operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the deintegrate phase of cycle. Output: Negative-going edge occurs when the data latches are updated. Can be used for converter status signal.
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal and positive rail for display drivers.
25	INT IN	Input to integrator amplifier.
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	Input: When LO, continuity flag on the display is off. When HI, continuity flag is on. Output: HI when voltage between inputs is less than +200 mV. LO when voltage between inputs is more than +200 mV.
28	COMMON	Sets common-mode voltage of 3.2V below V^+ for DE, 10X, etc. Can be used as preregulator for external reference.
29	C_{REF}^+	Positive side of external reference capacitor.
30	C_{REF}^-	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference voltage input terminal.
36	DGND	Internal ground reference for digital section. See "±5V Power Supply" paragraph.
37	RANGE	3 µA pull-down for 200 mV scale. Pulled HI externally for 2V scale.
38	DP_2	Internal 3 µA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3 µA pull-down. When HI, decimal point 1 will be on.
40	OSC_2	Output of first clock inverter. Input of second clock inverter.

COMPONENT SELECTION

The TC7129 is designed to be the heart of a high-resolution analog measurement instrument. The only additional components required are a few passive elements, a voltage reference, an LCD, and a power source. Most component values are not critical; substitutes can be chosen based on the information given below.

The basic circuit for a digital multimeter application is shown in Figure 1. See "Special Applications" for variations. Typical values for each component are shown. The sections below give component selection criteria.

Oscillator (X_{OSC}, C_{O1}, C_{O2}, R_O)

The primary criterion for selecting the crystal oscillator is to chose a frequency that achieves maximum rejection of line-frequency noise. To do this, the integration phase should last an integral number of line cycles. The integration phase of the TC7129 is 10,000 clock cycles on the 200 mV range and 1000 clock cycles on the 2V range. One clock cycle is equal to two oscillator cycles. For 60 Hz rejection, the oscillator frequency should be chosen so the period of one line cycle equals the integration time for the 2V range:

$$1/60 \text{ second} = 16.7 \text{ ms} = \frac{1000 \text{ clock cycles} * 2 \text{ osc cycles/clock cycle}}{\text{oscillator frequency}},$$

giving an oscillator frequency of 120 kHz. A similar calculation gives an optimum frequency of 100 kHz for 50 Hz rejection.

The resistor and capacitor values are not critical; those shown work for most applications. In some situations, the capacitor values may have to be adjusted to compensate for parasitic capacitance in the circuit. The capacitors can be low-cost ceramic devices.

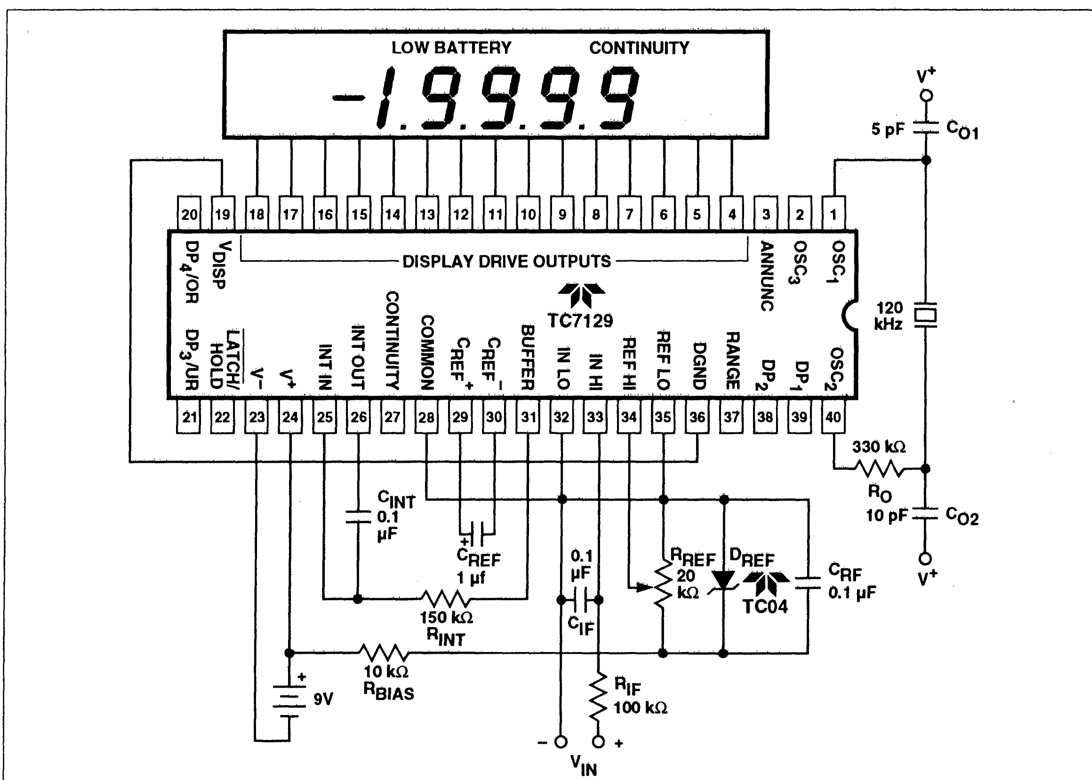


Figure 1 Standard Circuit

Some applications can use a simple RC network instead of a crystal oscillator. The RC oscillator has more potential for jitter, especially in the least significant digit. See "RC Oscillator."

Integrating Resistor (R_{INT})

The integrating resistor sets the charging current for the integrating capacitor. Choose a value that provides a current between 5 μA and 20 μA at 2V, the maximum full-scale input. The typical value chosen gives a charging current of 13.3 μA:

$$I_{CHARGE} = \frac{2V}{150\ k\Omega}\ 13.3\ \mu A$$

Too high a value for R_{INT} increases the sensitivity to noise pickup and increases errors due to leakage current. Too low a value degrades the linearity of the integration, leading to inaccurate readings.

Integrating Capacitor (C_{INT})

The charge stored in the integrating capacitor during integrate phase is directly proportional to the input voltage. The primary selection criterion for C_{INT} is to choose a value that gives the highest voltage swing while remaining within the high-linearity portion of the integrator output range. An integrator swing of 2V is the recommended value. The capacitor value can be calculated from the equation:

$$C_{INT} = \frac{t_{INT} * I_{INT}}{V_{SWING}},$$

where t_{INT} is the integration time.

Using the values derived above (assuming 60 Hz operation), the equation becomes:

$$C_{INT} = \frac{16.7\ ms * 13.3\ \mu A}{2V} = 0.1\ \mu F.$$

The capacitor should have low dielectric absorption to ensure good integration linearity. Polypropylene and Teflon capacitors are usually suitable. A good measurement of the dielectric absorption is to connect the reference capacitor across the inputs by connecting:

Pin to Pin
20 → 33 (C_{REF}^{+} to IN HI)
30 → 32 (C_{REF}^{-} to IN LO)

A reading between 10,000 and 9998 is acceptable; anything lower indicates unacceptable high dielectric absorption.

Reference Capacitor (C_{REF})

The reference capacitor stores the reference voltage during several phases of the measurement cycle. Low leakage is the primary selection criterion for this component. The value must be high enough to offset the effect of stray capacitance at the capacitor terminals. A value of at least 1 μF is recommended.

Voltage Reference (D_{REF}, R_{REF}, R_{BIAS}, C_{RF})

A TC04 band-gap reference provides a high-stability voltage reference of 1.25V. The reference potentiometer (R_{REF}) provides an adjustment for adjusting the reference voltage; any value above 20 kW is adequate. The bias resistor (R_{BIAS}) limits the current through D_{REF} to less than 150 μA. The reference filter capacitor (C_{RF}) forms an RC filter with R_{BIAS} to help eliminate noise.

Input filter (R_{IF}, C_{IF})

For added stability, an RC input noise filter is usually included in the circuit. The input filter resistor value should not exceed 100 kW. A typical RC time constant value is 16.7 ms to help reject line-frequency noise. The input filter capacitor should have low leakage for high-impedance input.

Battery

The typical circuit uses a 9V battery as a power source. Any value between 6V and 12V can be used. For operation from batteries with voltages lower than 6V and for operation from power supplies, see "Powering the TC7129."

SPECIAL APPLICATIONS

The TC7129 as a Replacement Part

The TC7129 is a direct pin-for-pin replacement part for the Intersil ICL7129. Note, however, that the Intersil part requires a capacitor and resistor between pins 26 and 28 for phase compensation. Since the TC7129 uses internal phase compensation, these parts are not required and, in fact, **must be removed** from the circuit for stable operation.

Powering the TC7129

While the most common power source for the TC7129 is a 9V battery, there are other possibilities. Some of the more common ones are explained below.

±5V Power Supply

Measurements are made with respect to power supply ground. DGND (pin 36) is set internally to about 5V less than v^+ (pin 24); it is not intended as a power supply input and must not be tied directly to power supply ground. (It can be used as a reference for external logic, as explained in "Connecting to External Logic." (See Figure 2.)

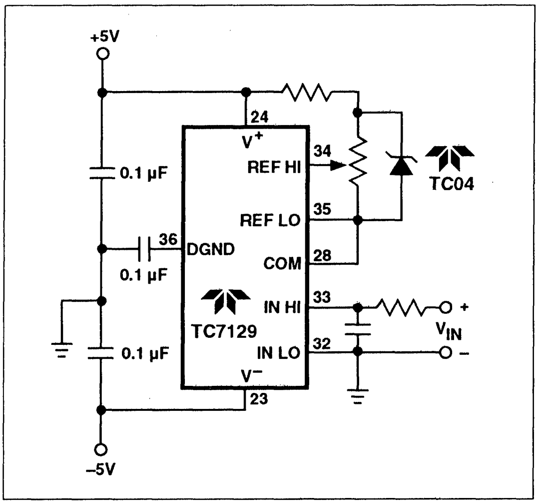


Figure 2 Powering the TC7129 From a ±5V Power Supply

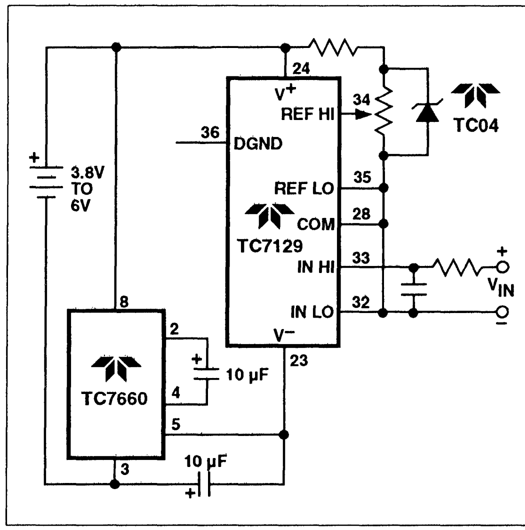


Figure 3 Powering the TC7129 From a Low-Voltage Battery

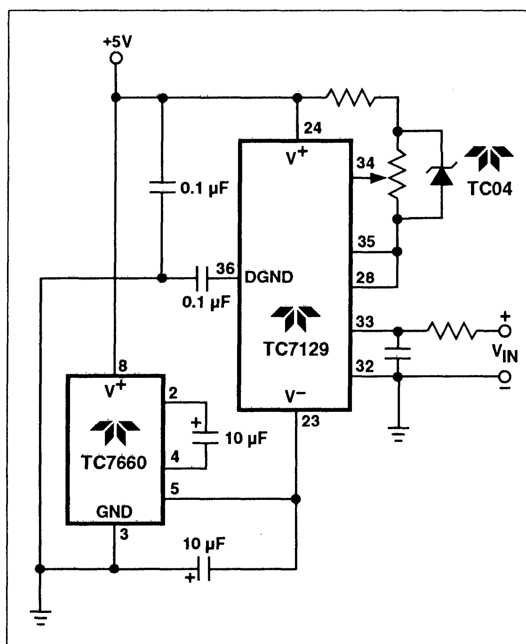


Figure 4 Powering the TC7129 From a +5V Power Supply

Low-Voltage Battery Source

A battery with voltage between 3.8V and 6V can be used to power the TC7129 when used with a voltage-doubler circuit as shown in Figure 3. The voltage doubler uses the TC7660 DC-to-DC voltage converter and two external capacitors.

+5V Power Supply

Measurements are made with respect to power supply ground. COMMON (pin 28) is connected to REF LO (pin 35). A voltage doubler is needed, since the supply voltage is less than 6V minimum needed by the TC7129. DGND (pin 36) must be isolated from power supply ground. (See Figure 4.)

Connecting to External Logic

External logic can be directly referenced to DGND (pin 36), provided the supply current of the external logic does not exceed the sink current of DGND (Figure 5). A safe value for DGND sink current is 1.2 mA. If the sink current is expected to exceed this value, a buffer is recommended. (See Figure 6.)

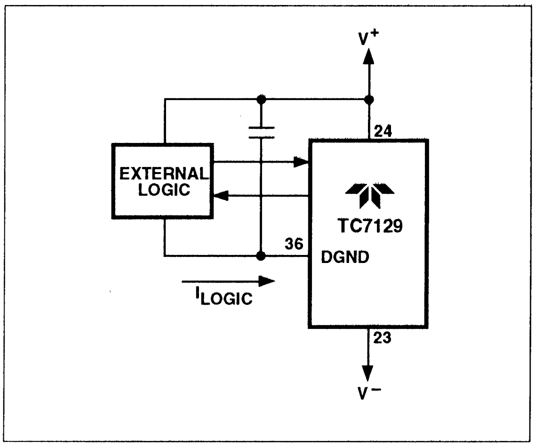


Figure 5 External Logic Referenced Directly to DGND

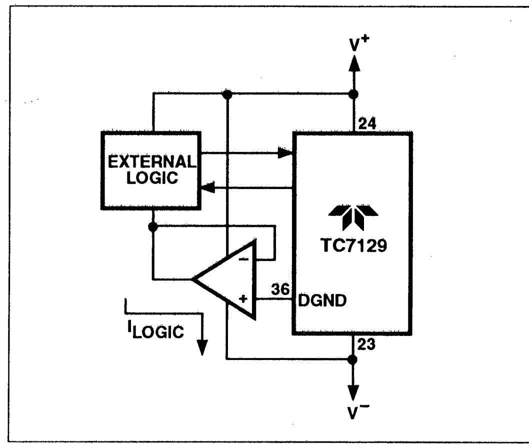


Figure 6 External Logic Referenced to DGND With Buffer

Temperature Compensation

For most applications, V_{DISP} (pin 19) can be connected directly to DGND (pin 36). For applications with a wide temperature range, some LCDs require the drive levels vary with temperature to maintain good viewing angle and display contrast. Figure 7 shows two circuits that can be adjusted to give temperature compensation of about 10 mV/°C between V+ (pin 24) and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage because V_{DISP} cannot exceed 0.3V below DGND.

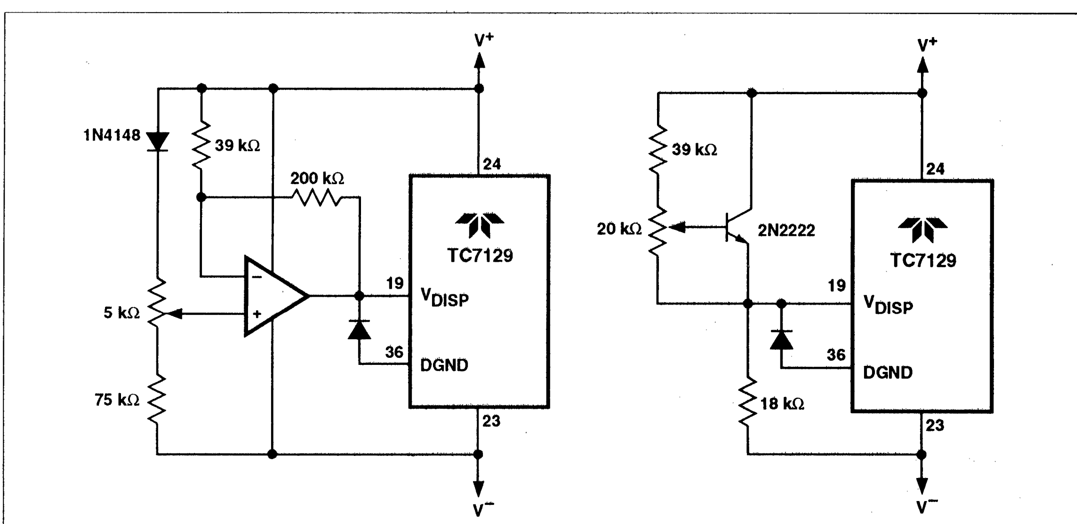


Figure 7 Temperature Compensating Circuits

4-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER WITH ON-CHIP LCD DRIVERS

RC Oscillator

For applications in which 3-1/2 digit (100 μV) resolution is sufficient, an RC oscillator is adequate. A recommended value for the capacitor is 51 pF. Other values can be used as long as they are sufficiently larger than the circuit parasitic capacitance. The resistor value is calculated from:

$$R = \frac{0.45}{freq * C}$$

For 120 kHz frequency and C = 51 pF, the calculated value of R is 75 kW. The RC oscillator and the crystal oscillator circuits are shown in Figure 8.

Measuring Techniques

Two important techniques are used in the TC7129: successive integration and digital auto-zeroing. Successive integration is a refinement to the traditional dual-slope conversion technique.

Dual-Slope Conversion

A dual-slope conversion has two basic phases: integrate and deintegrate. During the integrate phase, the input signal is integrated for a fixed period of time; the integrated voltage level is thus proportional to the input voltage. During the deintegrate phase, the integrated voltage is ramped down at a fixed slope, and a counter counts the clock cycles until the integrator voltage crosses zero. The count is a measurement of the time to ramp the integrated voltage to zero, and is therefore proportional to the input voltage being measured. This count can then be scaled and displayed as a measurement of the input voltage. Figure 9 shows the phases of the dual-slope conversion.

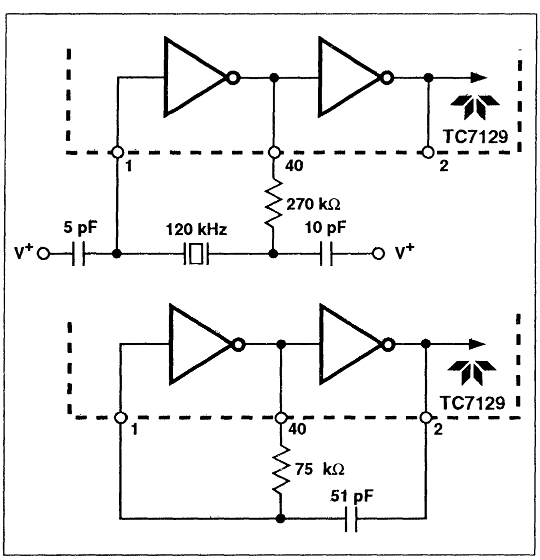


Figure 8 Oscillator Circuits

The dual-slope method has a fundamental limitation. The count can only stop on a clock cycle, so that measurement accuracy is limited to the clock frequency. In addition, a delay in the zero-crossing comparator can add to the inaccuracy. Figure 10 shows these errors in an actual measurement.

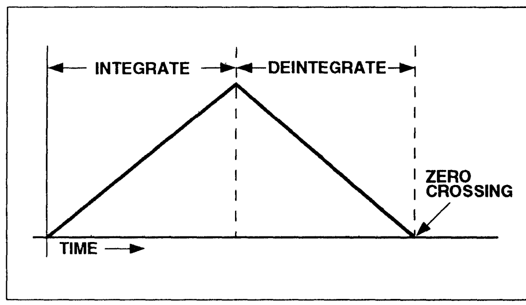


Figure 9 Dual-Slope Conversion

Successive Integration

The successive integration technique picks up where dual-slope conversion ends. The overshoot voltage shown in Figure 10, called the "integrator residue voltage," is measured to obtain a correction to the initial count. Figure 11 shows the cycles in a successive integration measurement.

The waveform shown is for a negative input signal. The sequence of events during the measurement cycle is:

Phase	Description
INT_1	Input signal is integrated for fixed time. (1000 clock cycles on 2V scale, 10,000 on 200 mV)
DE_1	Integrator voltage is ramped to zero. Counter counts up until zero crossing to produce reading accurate to 3-1/2 digits. Residue represents an overshoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE_2	Integrator voltage is ramped to zero. Counter counts down until zero crossing to correct reading to 4-1/2 digits. Residue represents an undershoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE_3	Integrator voltage is ramped to zero. Counter counts up until zero crossing to correct reading to 5-1/2 diigits. Residue is discarded.

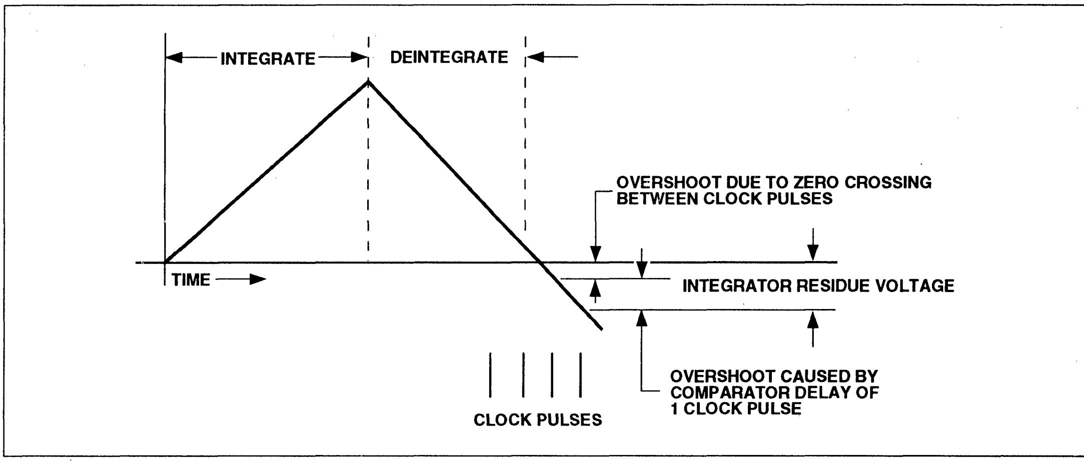


Figure 10 Accuracy Errors in Dual-Slope Conversion

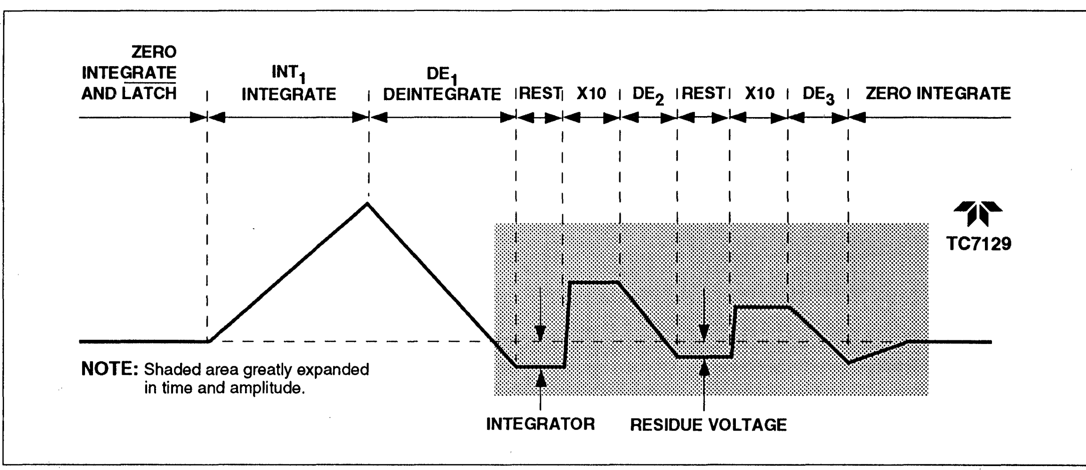


Figure 11 Integrator Waveform

Digital Auto-Zeroing

To eliminate the effect of amplifier offset errors, the TC7129 uses a digital auto-zeroing technique. After the input voltage is measured as described above, the measurement is repeated with the inputs shorted internally. The reading with inputs shorted is a measurement of the internal errors and is subtracted from the previous reading to obtain a corrected measurement. Digital auto-zeroing eliminates the need for an external auto-zeroing capacitor used in other ADCs.

Inside the TC7129

Figure 12 shows a simplified block diagram of the TC7129.

Integrator Section

The integrator section includes the integrator, comparator, input buffer amplifier, and analog switches used to change the circuit configuration during the separate measurement phases described earlier.

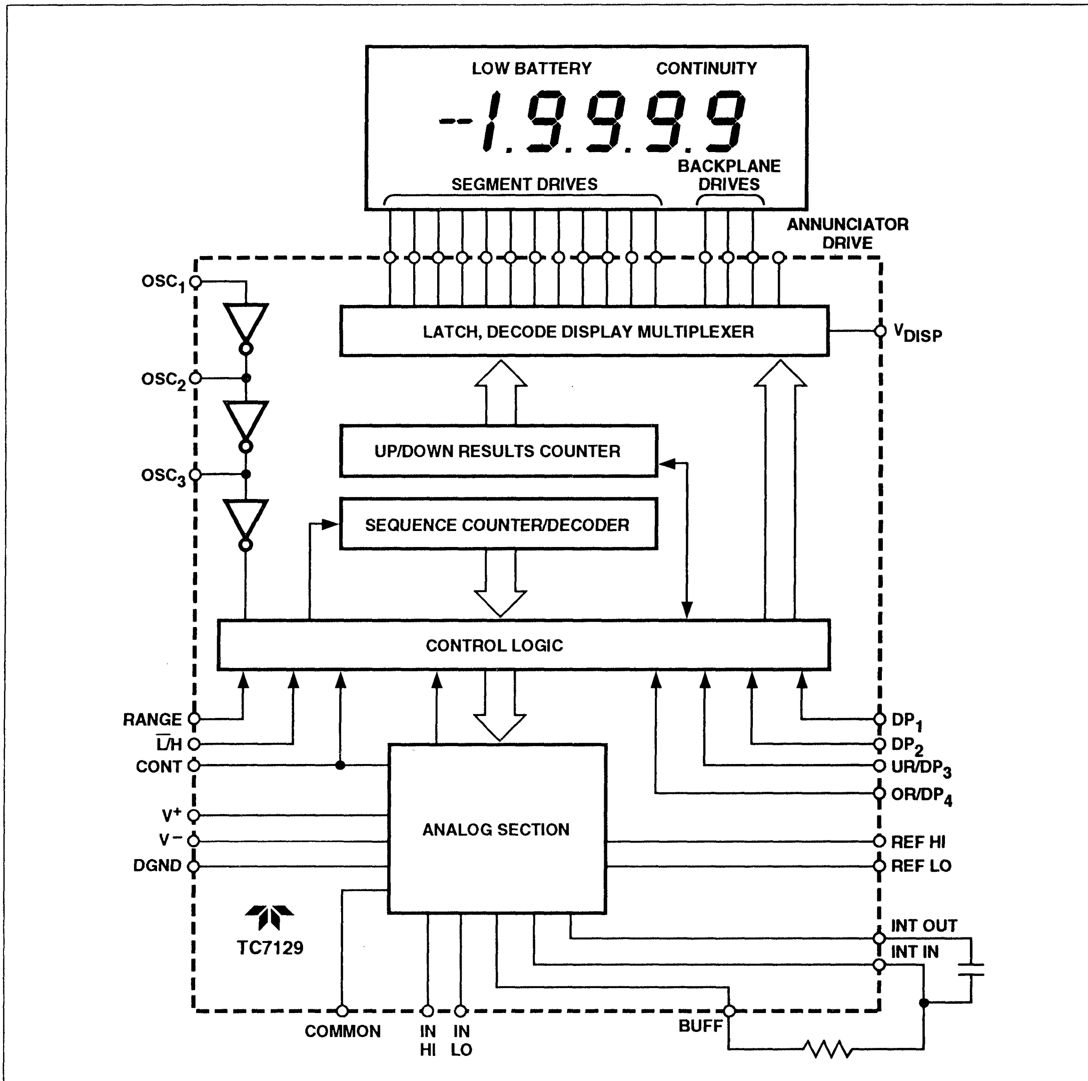


Figure 12 Functional Diagram

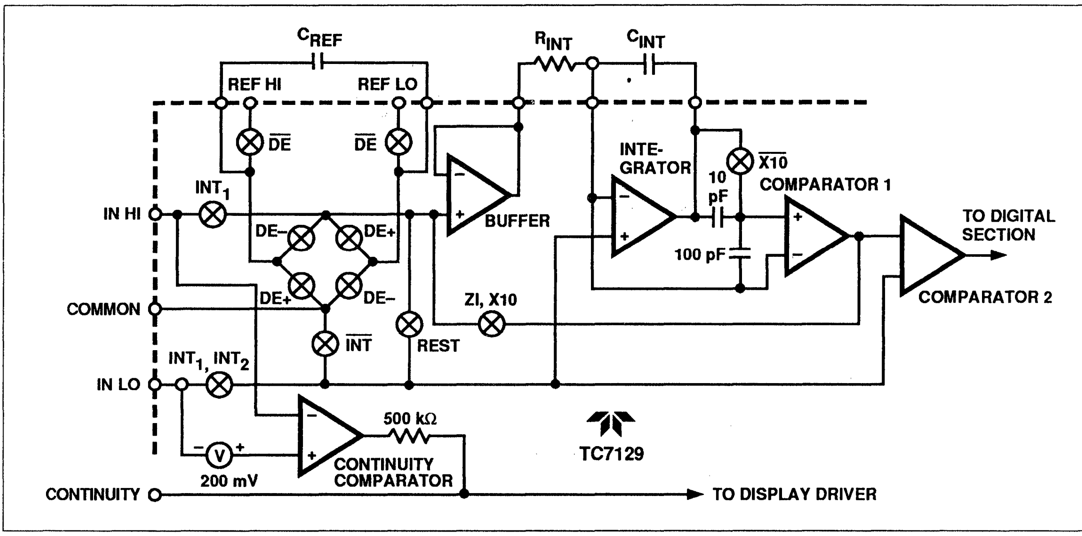


Figure 13 Integrator Block Diagram

Table I. Switch Legends

Label	Meaning
$\overline{DE}$	Open during all deintegrate phases.
DE–	Closed during all deintegrate phases when input voltage is negative.
DE+	Closed during all deintegrate phases when input voltage is positive.
INT_1	Closed during the first integrate phase (measurement of the input voltage).
INT_2	Closed during the second integrate phase (measurement of the amplifier offset).
$\overline{INT}$	Open during both integrate phases.
REST	Closed during the rest phase.
ZI	Closed during the zero-integrate phase.
X10	Closed during the X10 phase.
$\overline{X10}$	Open during the X10 phase.

The buffer amplifier has a common-mode input voltage range from 1.5V above V^- to 1V below V^+. The integrator amplifier can swing to within 0.3V of the rails, although for best linearity the swing is usually limited to within 1V. Both amplifiers can supply up to 80 μA of output current, but should be limited to 20 μA for good linearity.

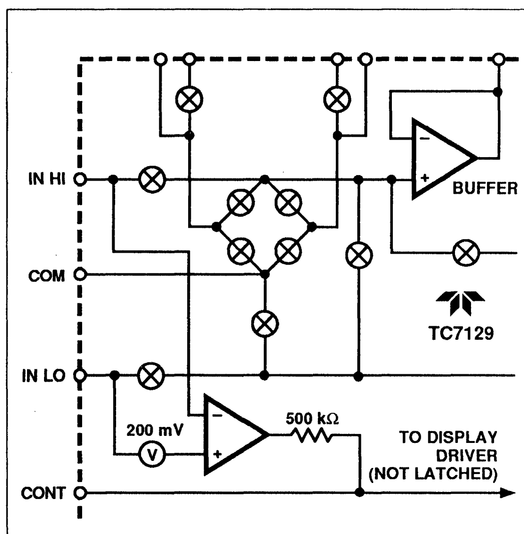


Figure 14 Continuity Indicator Circuit

Continuity Indicator

A comparator with a 200 mV threshold is connected between IN HI (pin 33) and IN LO (pin 32). Whenever the voltage between inputs is less than 200 mV, the CONTINUITY output (pin 27) will be pulled high, activating the continuity annunciator on the display. The continuity pin can also be used as an input to drive the continuity annunciator directly from an external source. A schematic of the input/output nature of this pin is shown in Figure 15.

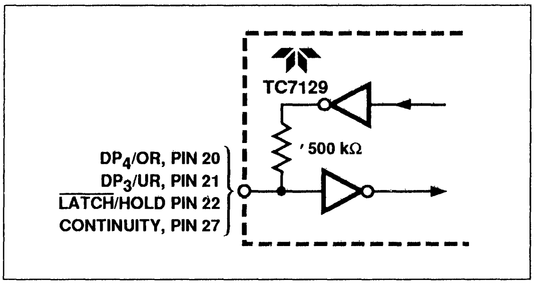


Figure 15 Input/Output Pin Schematic

Common and Digital Ground

The common and digital ground (DGND) outputs are generated from internal zener diodes. The voltage between V^+ and DGND is the internal supply voltage for the digital section of the TC7129. Common can source approximately 12 μA; DGND has essentially no source capability.

Low Battery

The low battery annunciator turns on when supply voltage between V^+ and V^- drops below 6.8V. The internal zener has a threshold of 6.3V. When the supply voltage drops below 6.8V, the transistor tied to V^- turns off, pulling the "Low Battery" point high. (See Figure 16.)

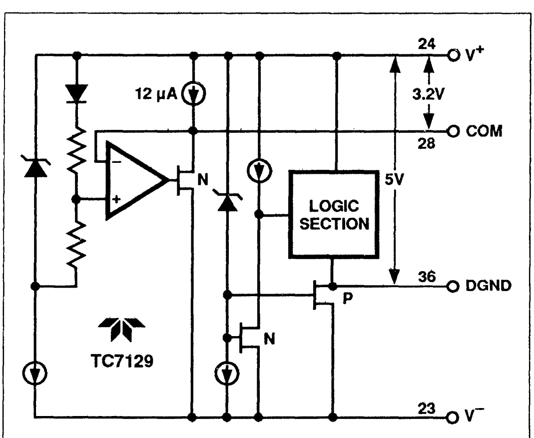


Figure 16 Digital Ground (DGND) and Common Outputs

Sequence and Results Counter

A sequence counter and associated control logic provide signals that operate the analog switches in the integrator section. The comparator output from the integrator gates the results counter. The results counter is a six-section up/down decade counter which holds the intermediate results from each successive integration.

Overrange and Underrange Outputs

When the results counter holds a value greater than ±19,999, the DP_4/OR output (pin 20) is driven high. When the results counter value is less than ±1000, the DP_3/UR output (pin 21) is driven high. Both signals are valid on the falling edge of $\overline{\text{LATCH}}$/HOLD ($\overline{\text{L}}$/H) and do not change until the end of the next conversion cycle. The signals are updated at the end of each conversion unless the $\overline{\text{L}}$/H input (pin 22) is held high. Pins 20 and 21 can also be used as inputs for external control of decimal points 3 and 4. Figure 15 shows a schematic of the input/output nature of these pins.

Latch/Hold

The $\overline{\text{L}}$/H output goes low during the last 100 cycles of each conversion. This pulse latches the conversion data into the display driver section of the TC7129. This pin can also be used as an input. When driven high, the display will not be updated; the previous reading is displayed. When driven low, the display reading is not latched; the sequence counter reading will be displayed. Since the counter is counting much faster than the backplanes are being updated, the reading shown in this mode is somewhat erratic.

Display Driver

The TC7129 drives a triplexed LCD with three backplanes. The LCD can include decimal points, polarity sign, and annunciators for continuity and low battery. Figure 17 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 1200. This results in a backplane drive frequency of 100 Hz for 60 Hz operation (120 kHz crystal) and 83.3 Hz for 50 Hz operation (100 kHz crystal).

Backplane waveforms are shown in Figure 18. These appear on outputs BP_1, BP_2, BP_3 (pins 16, 17, and 18). They remain the same regardless of the segments being driven.

Other display output lines (pins 4 through 15) have waveforms that vary depending on the displayed values. Figure 19 shows a set of waveforms for the A, G, D outputs (pins 5, 8, 11, and 14) for several combinations of "on" segments.

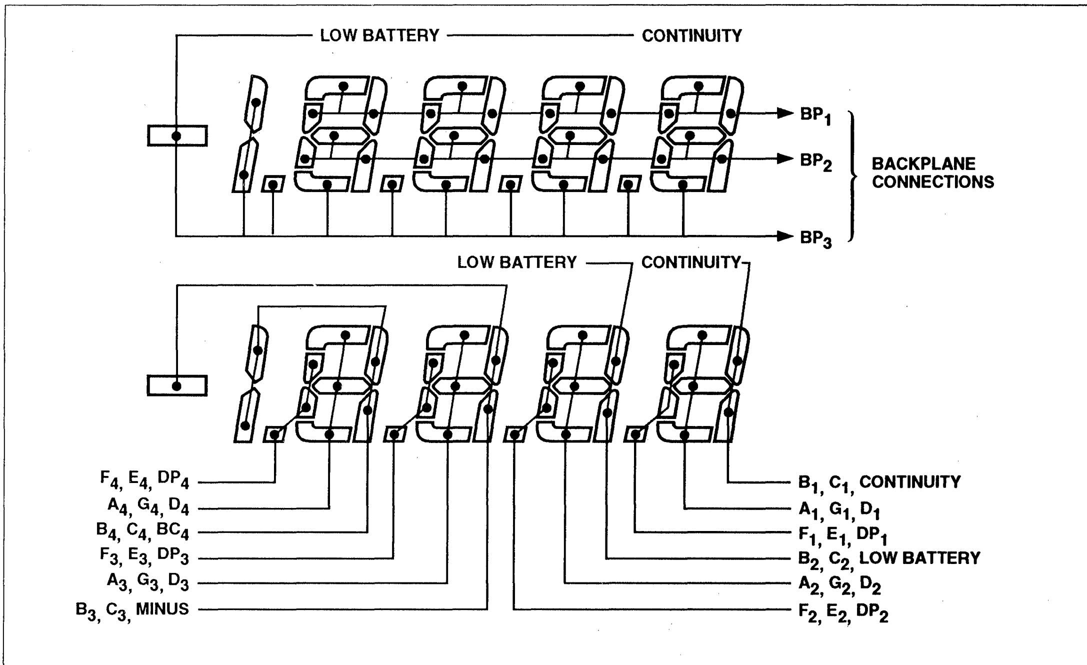


Figure 17 Display Segment Assignments

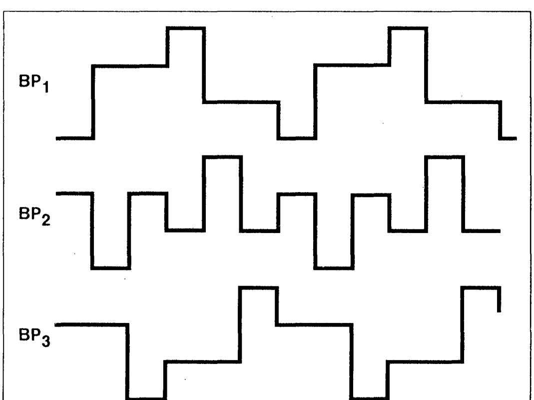


Figure 18 Backplane Waveforms

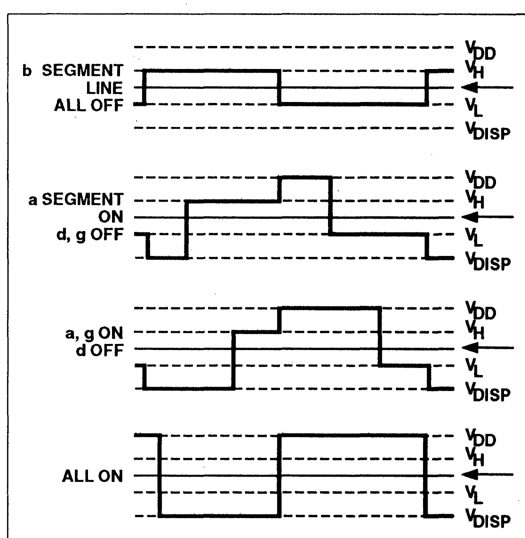


Figure 19 Typical Display Output Waveforms

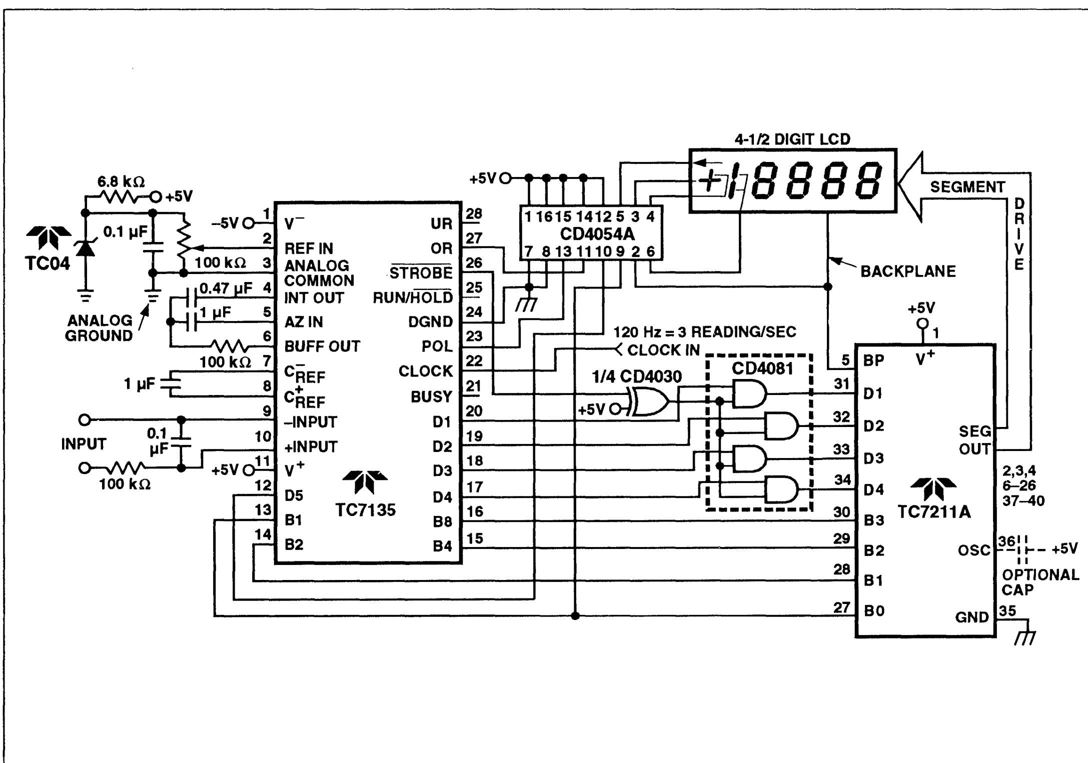
The ANNUNCIATOR DRIVE output (pin 3) is a squarewave running at the backplane frequency (100 Hz or 83.3 Hz), with a peak-to-peak voltage equal to DGND voltage. Connecting an annunciator to pin 3 turns it on; connecting it to its backplane turns it off.

4-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER

FEATURES

- Low Roll-Over Error ....±1 Count Max
- Guaranteed Nonlinearity Error ....±1 Count Max
- Guaranteed Zero Reading for 0V Input
- True Polarity Indication at Zero for Null Detection
- Multiplexed BCD Data Output
- TTL-Compatible Outputs
- Differential Input
- Control Signals Permit Interface to UARTs and μProcessors
- Auto-Ranging Supported With Overrange and Underrange Signals
- Blinking Display Visually Indicates Overrange Condition
- Low Input Current ....1 pA
- Low Zero Reading Drift ....2 μV/°C
- Interfaces to TC7211A (LCD) and TC7212A (LED) Display Drivers
- Available in DIP and Surface-Mount Packages

TYPICAL 4-1/2 DIGIT DVM WITH LCD



1080-1

TC7135

GENERAL DESCRIPTION

The TC7135 4-1/2 digit analog-to-digital converter (ADC) offers 50 ppm (1 part in 20,000) resolution with a maximum nonlinearity error of 1 count. An auto-zero cycle reduces zero error to below 10 µV and zero drift to 0.5 µV/°C. Source impedance errors are minimized by a 10 pA maximum input current. Roll-over error is limited to ±1 count.

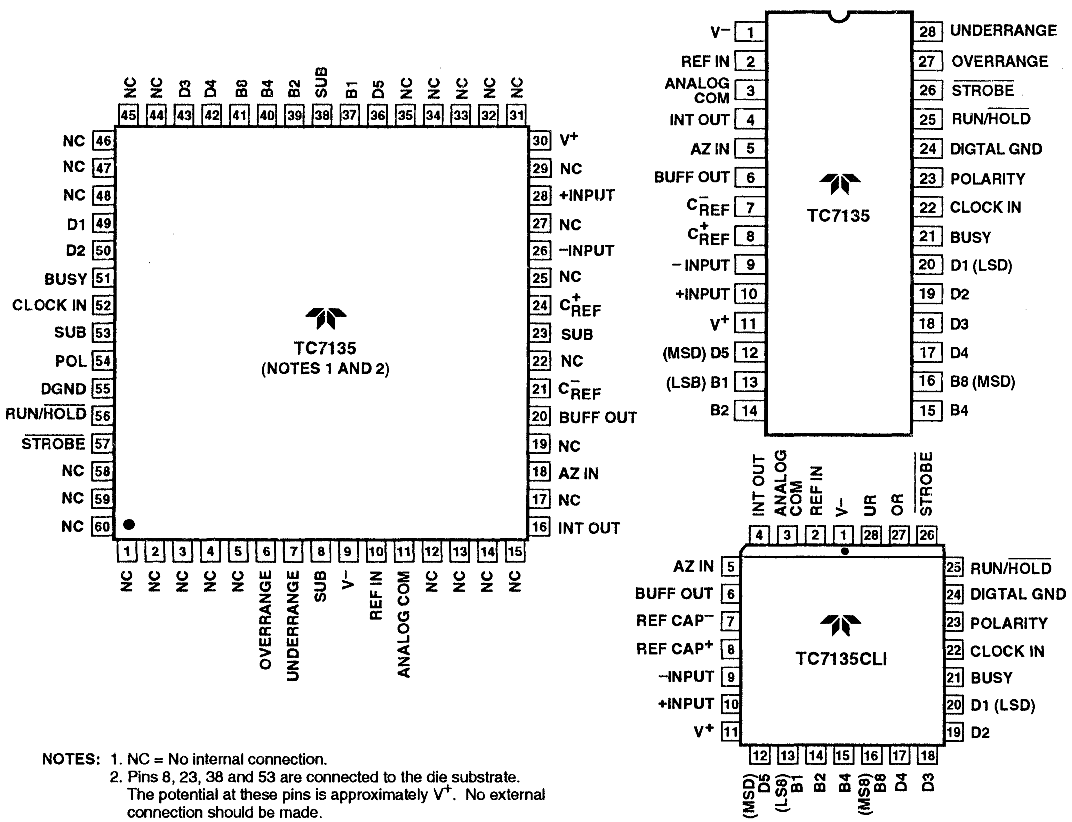
By combining the TC7135 with a TC7211A (LCD) or TC7212A (LED) driver, a 4-1/2 digit display DVM or DPM can be constructed. Overrange and underrange signals support automatic range switching and special display blanking/flashing applications.

Microprocessor-based measurement systems are supported by BUSY, $\overline{\text{STROBE}}$, and RUN/$\overline{\text{HOLD}}$ control signals. Remote data acquisition systems with data transfer via UARTs are also possible. The additional control pins and multiplexed BCD outputs make the TC7135 the ideal converter for display or microprocessor-based measurement systems.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7135CJI	28-Pin CerDIP	0°C to +70°C
TC7135CPI	28-Pin Plastic DIP	0°C to +70°C
TC7135CBQ	60-Pin Plastic Flat Package With Formed Leads	0°C to +70°C
TC7135CLI	28-Pin PLCC	0°C to +70°C

PIN CONFIGURATIONS



NOTES: 1. NC = No internal connection.
2. Pins 8, 23, 38 and 53 are connected to the die substrate. The potential at these pins is approximately V+. No external connection should be made.

4-1/2 DIGIT
ANALOG-TO-DIGITAL CONVERTER

TC7135

ABSOLUTE MAXIMUM RATINGS (Note 1)

Positive Supply Voltage ....+6V
Negative Supply Voltage ....–9V
Analog Input Voltage (Pin 9 or 10).......... V^+ to V^- (Note 2)
Reference Input Voltage (Pin 2) .... V^+ to V^-
Clock Input Voltage .... 0V to V^+
Operating Temperature Range .... 0°C to +70°C
Storage Temperature Range.................. –65°C to +160°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Package Power Dissipation
CerDIP (J) 1W
Plastic (P) 0.8W

Static-sensitive device. Unused devices must be stored in conductive material to protect them from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, f_{CLOCK} = 120 kHz, V^+ = +5V, V^- = –5V (Figure 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog						
	Display Reading With Zero Volt Input	Notes 2 and 3	–0.0000	±0.0000	+0.0000	Display Reading
TC_Z	Zero Reading Temperature Coefficient	V_{IN} = 0V Note 4	—	0.5	2	µV/°C
TC_{FS}	Full-Scale Temperature Coefficient	V_{IN} = 2V Notes 4 and 5	—	—	5	ppm/°C
NL	Nonlinearity Error	Note 6	—	0.5	1	Count
DNL	Differential Linearity Error	Note 6	—	0.01	—	LSB
	Display Reading in Ratiometric Operation	$V_{IN} = V_{REF}$ Note 2	+0.9998	+0.9999	+1.0000	Display Reading
±FSE	± Full-Scale Symmetry Error (Roll-Over Error)	$-V_{IN} = +V_{IN}$ Note 7	—	0.5	1	Count
I_{IN}	Input Leakage Current	Note 3	—	1	10	pA
V_N	Noise	Peak-to-Peak Value Not Exceeded 95% of Time	—	15	—	$µV_{P-P}$
Digital						
I_{IL}	Input Low Current	V_{IN} = 0V	—	10	100	µA
I_{IH}	Input High Current	V_{IN} = +5V	—	0.08	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	—	0.2	0.4	V
V_{OH}	Output High Voltage B_1, B_2, B_4, B_8, D_1–D_5 Busy, Polarity, Overrange, Underrange, Strobe	 I_{OH} = 1 mA I_{OH} = 10 µA	 2.4 4.9	 4.4 4.99	 5 5	 V V
f_{CLK}	Clock Frequency	Note 8	0	120	1200	kHz
Power Supply						
V^+	Positive Supply Voltage		4	5	6	V
V^-	Negative Supply Voltage		–3	–5	–8	V
I^+	Positive Supply Current	f_{CLK} = 0 Hz	—	1	3	mA
I^-	Negative Supply Current	f_{CLK} = 0 Hz	—	0.7	3	mA
PD	Power Dissipation	f_{CLK} = 0 Hz	—	8.5	30	mW

NOTES:
1. Limit input current to under 100 µA if input voltages exceed supply voltage.
2. Full-scale voltage = 2V.
3. V_{IN} = 0V.
4. 0°C ≤ T_A ≤ +70°C.
5. External reference temperature coefficient less than 0.01 ppm/°C.
6. –2V ≤ V_{IN} ≤ +2V. Error of reading from best fit straight line.
7. $|V_{IN}|$ = 1.9959.
8. Specification related to clock frequency range over which the TC7135 correctly performs its various functions. Increased errors result at higher operating frequencies.

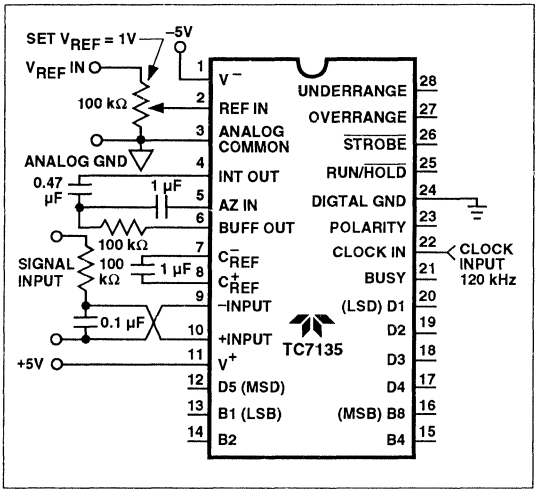


Figure 1. Test Circuit

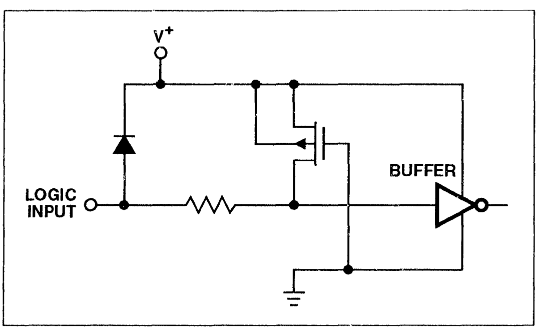


Figure 2. Digital Logic Input

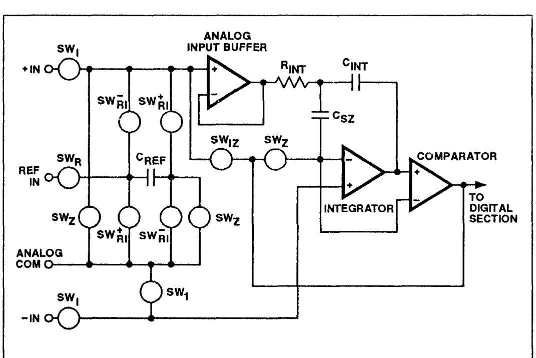


Figure 3A. Internal Analog Switches

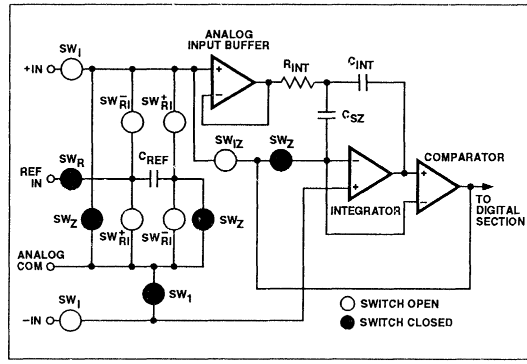


Figure 3B. System Zero Phase

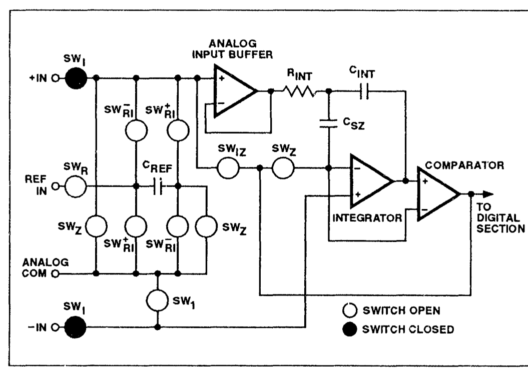


Figure 3C. Input Signal Integration Phase

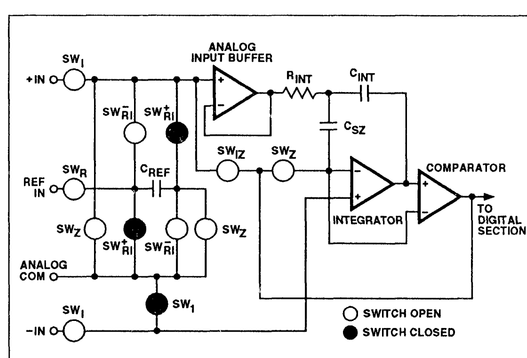


Figure 3D. Reference Voltage Integration Phase

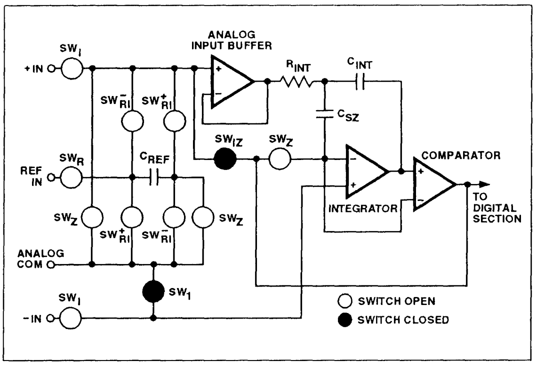


Figure 3E. Integrator Output Zero Phase

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC7135 is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following detailed TC7135 operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

where:

V_R = Reference voltage

t_{SI} = Signal integration time (fixed)

t_{RI} = Reference voltage integration time (variable).

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right].$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. (See Figure 4.)

TC7135 Operational Theory

The TC7135 incorporates a system zero phase and integrator output voltage zero phase to the normal two-phase dual-slope measurement cycle. Reduced system errors, fewer calibration steps, and a shorter overrange recovery time result.

The TC7135 measurement cycle contains four phases:

(1) System zero

(2) Analog input signal integration

(3) Reference voltage integration

(4) Integrator output zero

Internal analog gate status for each phase is shown in Table I.

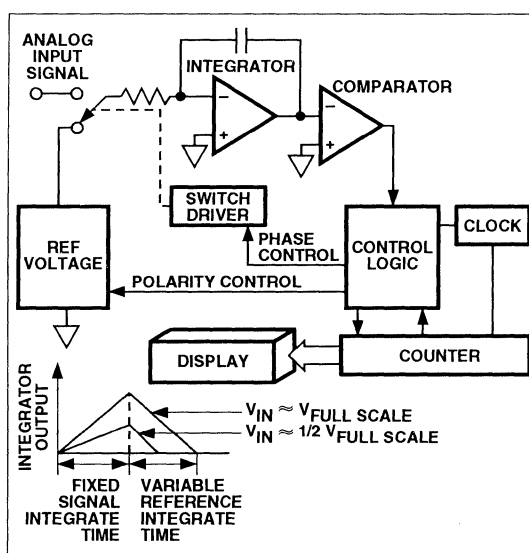


Figure 4. Basic Dual-Slope Converter

Table I. Internal Analog Gate Status

Conversion Cycle Phase	Internal Analog Gate Status SW_I	SW_{RI}^+	SW_{RI}^-	SW_Z	SW_R	SW_1	SW_{IZ}	Reference Schematic
System Zero				Closed	Closed	Closed		3B
Input Signal Integration	Closed							3C
Reference Voltage Integration		Closed*				Closed		3D
Integrator Output Zero						Closed	Closed	3E

***NOTE:** Assumes a positive polarity input signal. SW_{RI}^- would be closed for a negative input signal.

System Zero Phase

During this phase, errors due to buffer, integrator, and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With zero input voltage, the integrator output remains at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} with a voltage to compensate for buffer amplifier, integrator, and comparator offset voltages. (See Figure 3B.)

Analog Input Signal Integration Phase

The TC7135 integrates the differential voltage between the +INPUT and –INPUT. The differential voltage must be within the device's common-mode range; –1V from either supply rail, typically.

The input signal polarity is determined at the end of this phase. (See Figure 3C)

Reference Voltage Integration Phase

The previously-charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. (See Figure 3D.) The digital reading displayed is:

$$\text{Reading} = 10{,}000 \left[\frac{\text{Differential Input}}{V_{REF}}\right].$$

Integrator Output Zero Phase

This phase guarantees the integrator output is at 0V when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists, the phase is extended to 6200 clock cycles. (See Figure 3E.)

Analog Section Functional Description

Differential Inputs

The TC7135 operates with differential voltages (+INPUT, pin 10 and –INPUT, pin 9) within the input amplifier common-mode range which extends from 1V below the positive supply to 1V above the negative supply. Within this common-mode voltage range, an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage and must not be allowed to saturate. A worst-case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications, the integrator swing can be reduced to less than the recommended 4V full-scale swing, with some loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

ANALOG COMMON (pin 3) is used as the –INPUT return during the auto-zero and deintegrate phases. If –INPUT is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, –INPUT will be set at a fixed known voltage (power supply common, for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog common.

Reference Voltage

The reference voltage input (REF IN, pin 2) must be a positive voltage with respect to analog common. Two reference voltage circuits are shown in Figure 5.

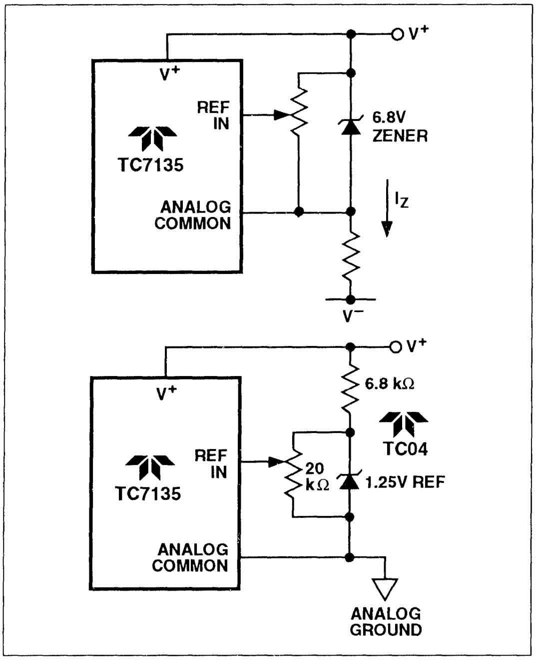


Figure 5. Using an External Reference Voltage

Digital Section Functional Description

The major digital subsystems within the TC7135 are illustrated in Figure 6, with timing relationships shown in Figure 7. The multiplexed BCD output data can be displayed on an LCD or LED display with the TC7211A (LCD) or TC7212A (LED) 4-digit display drivers.

The digital section is best described through a discussion of the control signals and data outputs.

RUN/$\overline{\text{HOLD}}$ Input

When left open, the RUN/$\overline{\text{HOLD}}$ (R/$\overline{\text{H}}$) input (pin 25) assumes a logic "1" level. With R/$\overline{\text{H}}$ = 1, the TC7135 performs conversions continuously, with a new measurement cycle beginning every 40,002 clock pulses.

When R/$\overline{\text{H}}$ changes to logic "0," the measurement cycle in progress will be completed, and data held and displayed, as long as the logic "0" condition exists.

A positive pulse (>300 ns) at R/$\overline{\text{H}}$ initiates a new measurement cycle. The measurement cycle in progress when R/$\overline{\text{H}}$ initially assumed logic "0" must be completed before the positive pulse can be recognized as a single conversion run command.

The new measurement cycle begins with a 10,001-count auto-zero phase. At the end of this phase, the busy signal goes high.

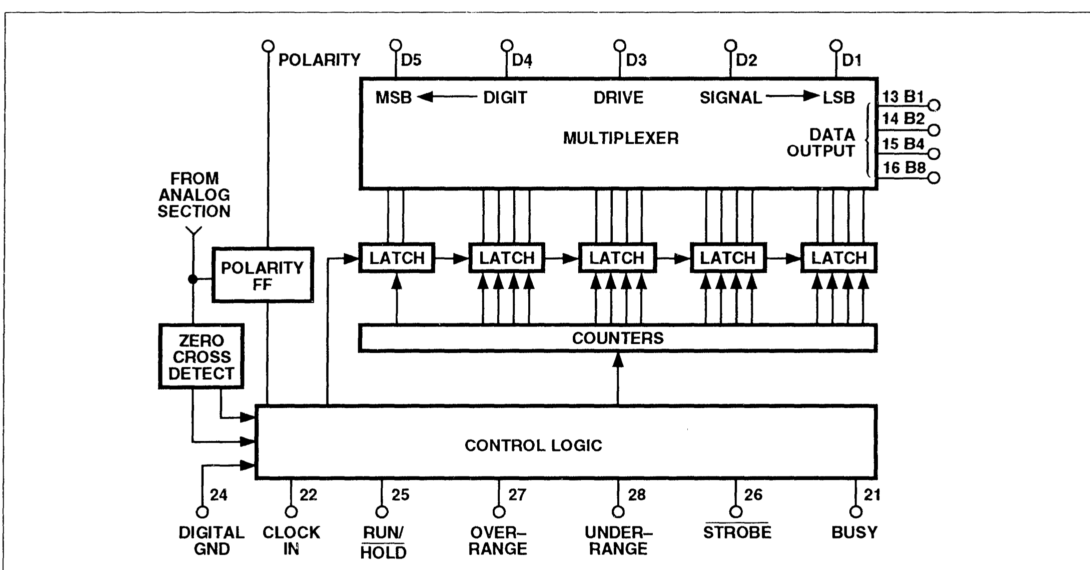


Figure 6. Digital Section Functional Diagram

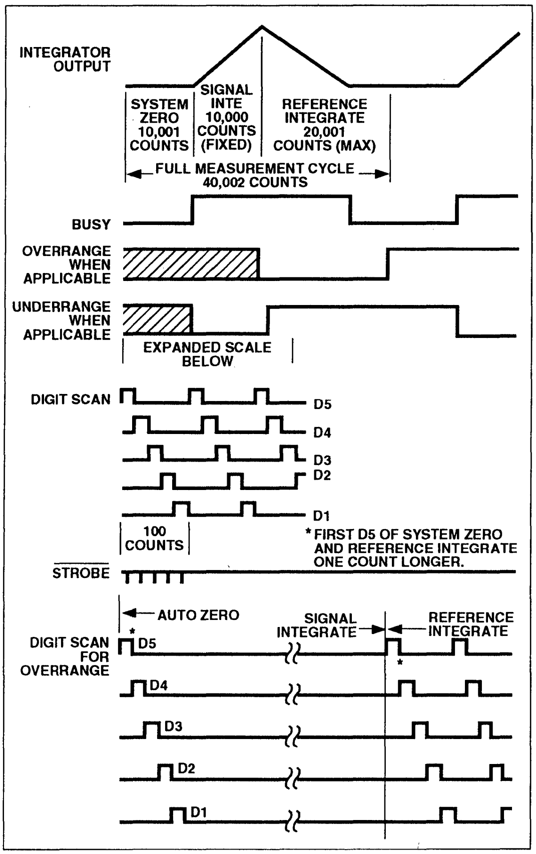


Figure 7. Timing Diagrams for Outputs

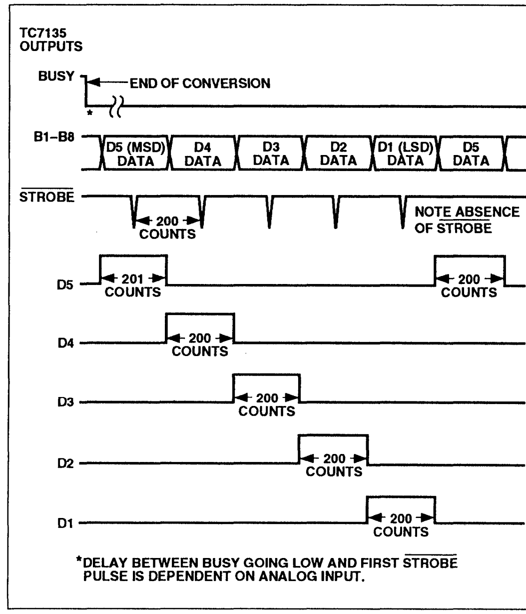


Figure 8. Strobe Signal Pulses Low Five Times per Conversion

$\overline{\text{STROBE}}$ Output

During the measurement cycle, the $\overline{\text{STROBE}}$ output (pin 26) control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_4 and D_5; see Figure 8).

D_5 goes high for 201 counts when the measurement cycles end. In the center of D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first $\overline{\text{STROBE}}$ occurs for one-half clock pulse. After D_5 strobe, D_4 goes high for 200 clock pulses. $\overline{\text{STROBE}}$ goes low 100 clock pulses after D_4 goes high. This continues through the D_1 drive pulse.

The digit drive signals will continue to permit display scanning. $\overline{\text{STROBE}}$ pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active-low $\overline{\text{STROBE}}$ pulses aid BCD data transfer to UARTs, microprocessors, and external latches. (See Application Note AN-16.)

BUSY Output

At the beginning of the signal-integration phase, BUSY (pin 21) goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to logic "0" after the measurement cycle ends in an overrange condition. The internal display latches are loaded during the first clock pulse after BUSY and are latched at the clock pulse end. The BUSY signal does not go high at the beginning of the measurement cycle, which starts with the auto-zero phase.

OVERRANGE Output

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses, the OVERRANGE output (pin 27) is set to logic "1." The OVERRANGE output register is set when BUSY goes low and reset at the beginning of the next reference-integration phase.

UNDERRANGE Output

If the output count is 9% of full scale or less ($\leq$1800 counts), the UNDERRANGE output (pin 28) register bit is set at the end of BUSY. The bit is set low at the next signal-integration phase.

POLARITY Output

A positive input is registered by a logic "1" polarity signal. The POLARITY output (pin 23) is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

The POLARITY bit is valid even for a zero reading. Signals less than the converter's LSB will have the signal polarity determined correctly. This is useful in null applications.

Digit Drive Outputs

Digit drive outputs are positive-going signals. Their scan sequence is D_5, D_4, D_3, D_2 and D_1 (pins 12, 17, 18, 19 and 20, respectively). All positive signals are 200 clock pulses wide, except D_5, which is 201 clock pulses.

All five digits are continuously scanned, unless an overrange condition occurs. In an overrange condition, all digit drives are held low from the final $\overline{\text{STROBE}}$ pulse until the beginning of the next reference-integrate phase. The scanning sequence is then repeated, providing a blinking visual display.

BCD Data Outputs

The binary coded decimal (BCD) outputs, B_8, B_4, B_2 and B_1 (pins 16, 15, 14 and 13, respectively) are positive true-logic signals. They become active simultaneously with digit drive signals. In an overrange condition, all data bits are logic "0".

APPLICATIONS INFORMATION

Component Value Selection

Integrating Resistor

The integrating resistor (R_{INT}) is determined by the full-scale input voltage and output current of the buffer used to charge the integrator capacitor (C_{INT}). Both the buffer amplifier and the integrator have a Class A output stage, with 100 μA of quiescent current. A 20 μA drive current gives negligible linearity errors. Values of 5 μA to 40 μA give good results. The exact value of R_{INT} for a 20 μA current is easily calculated:

$$R_{INT} = \frac{\text{Full-scale voltage}}{20\ \mu A}.$$

Integrating Capacitor

The product of R_{INT} and C_{INT} should be selected to give the maximum voltage swing to ensure tolerance build-up will not saturate integrator swing (approximately 0.3V from either supply). For ±5V supplies, and analog common tied to supply ground, a ±3.5V to ±4V full-scale integrator swing is adequate. A 0.10 μF to 0.47 μF is recommended. In general, the value of C_{INT} is given by:

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\ \mu A)}{\text{Integrator output voltage swing}}.$$

A very important characteristic of the C_{INT} is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half-scale 0.9999. Any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitors

The size of the auto-zero capacitor (C_{AZ}) has some influence on system noise. A large capacitor reduces noise. The reference capacitor (C_{REF}) should be large enough such that stray capacitance from its nodes to ground is negligible.

The dielectric absorption of C_{REF} and C_{AZ} is only important at power-on, or when the circuit is recovering from an overload. Smaller or cheaper capacitors can be used if accurate readings are not required during the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in overall absolute accuracy of the converter. Therefore, it is recommended that high-quality references be used where high-accuracy, absolute measurements are being made. Suitable references are:

Part Type	Manufacturer
TC04	Teledyne Components
MP5010	Teledyne Components

Conversion Timing

Line Frequency Rejection

A signal-integration period at a multiple of the 60 Hz line frequency will maximize 60 Hz "line noise" rejection.

A 100 kHz clock frequency will reject 50 Hz, 60 Hz and 400 Hz noise, corresponding to 2.5 readings per second.

Table II. Line Frequency Rejection

Oscillator Frequency (kHz)	Frequency Rejected (Hz)
300, 200, 150, 120, 100, 40, 33-1/3	60
250, 166-2/3, 125, 100	50
100	50, 60, 400

Table III. Conversion Rate vs Clock Frequency

Conversion Rate (Conv/Sec)	Clock Frequency (kHz)
2.5	100
3.0	120
5.0	200
7.5	300
10.0	400
20.0	800
30.0	1200

Displays and Driver Circuits

Teledyne Components manufactures three display decoder/driver circuits to interface the TC7135 to LCDs or LED displays. Each driver has 28 outputs for driving four 7-segment digit displays. The TC700A features increased LED segment drive current for greater display brightness.

Device	Package	Description
TC7211AIPL	40-Pin Epoxy	4-Digit LCD Driver/Encoder
TC7212AIPL	40-Pin Epoxy	4-Digit LED Driver/Encoder

Several sources exist for LCDs and LED displays.

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Road Palo Alto, CA 94304	LED
AND	770 Airport Blvd. Burlingame, CA 94010	LCD and LED
Epson America, Inc.	3415 Kanhi Kawa St. Torrance, CA 90505	LCD

High-Speed Operation

The maximum conversion rate of most dual-slope ADCs is limited by frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 μs delay, and at a clock frequency of 160 kHz (6 μs period), half of the first reference integrate clock period is lost in delay. This means the meter reading will change from 0 to 1 with a 50 μV input, 1 to 2 with 150 μV, 2 to 3 with 250 μV, etc. This transition at mid-point is considered desirable by most users; however, if clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications, where the input signal is always of one polarity, comparator delay need not be a limitation. Since nonlinearity and noise do not increase substantially with frequency, clock rates up to ~1 MHz may be used. For a fixed clock frequency, the extra count (or counts) caused by comparator delay will be constant and can be digitally subtracted.

The clock frequency may be extended above 160 kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage onto the integrator output at the beginning of reference-integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated for and maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second-order breaks will cause significant nonlinearities during the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the applications section. The multiplexed output means if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates data once every clock pulse after transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of the reference integrate (deintegrate) phase. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto-zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate, so true ratiometric readings result.

Generating a Negative Supply

A negative voltage can be generated from the positive supply by using a TC7660. (See Figure 9.)

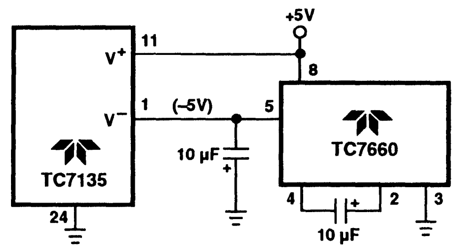
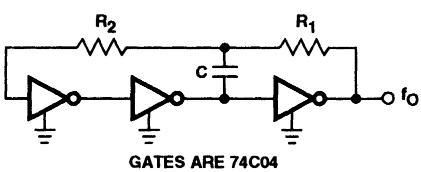


Figure 9. Negative Supply Voltage Generator

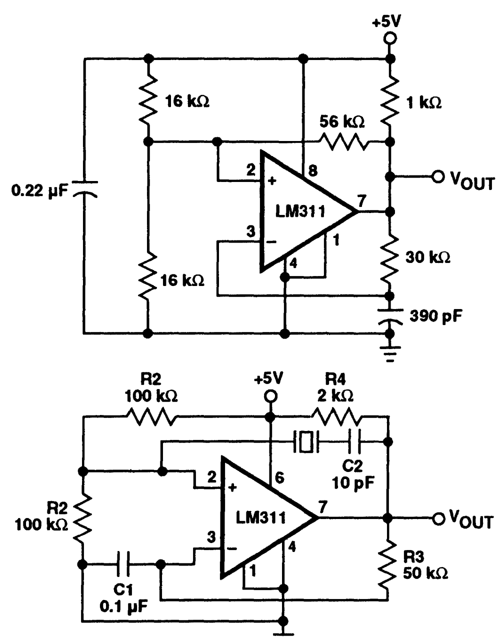
TYPICAL APPLICATIONS DIAGRAMS

RC Oscillator Circuit



1. $f_O \approx \dfrac{1}{2\,C[0.41\,R_P + 0.70\,R_1]}$, $R_P = \dfrac{R_1\,R_2}{R_1 + R_2}$
   a. If $R = R_1 = R_2$, $f \cong 0.55/RC$
   b. If $R_2 >> R_1$, $f \cong 0.45/R_1C$
   c. If $R_2 << R_1$, $f \cong 0.72/R_1C$
2. Examples:
   a. $f = 120$ kHz, $C = 420$ pF
      $R_1 = R_2 \approx 10.9$ kΩ
   b. $f = 120$ kHz, $C = 420$ pF, $R_2 = 50$ kΩ
      $R_1 = 8.93$ kΩ
   c. $f = 120$ kHz, $C = 220$ pF, $R_2 = 5$ kΩ
      $R_1 = 27.3$ kΩ

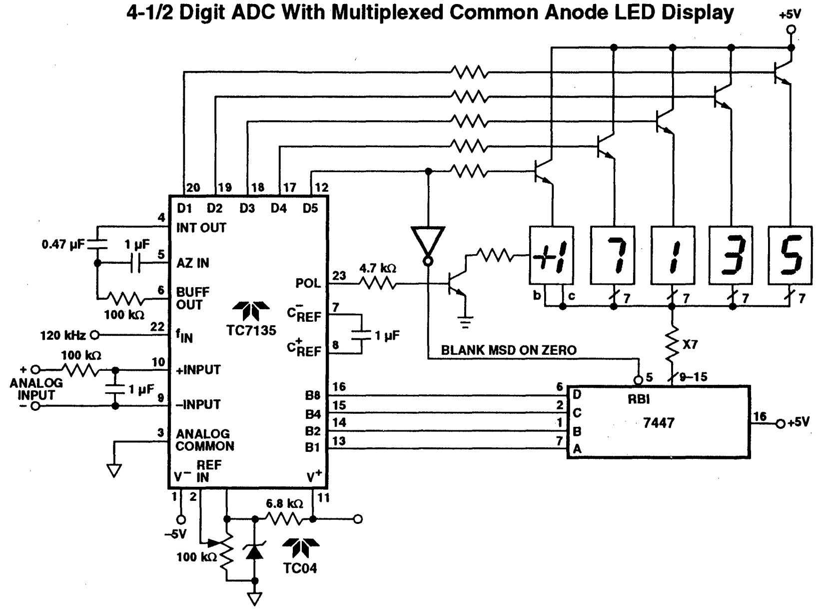
Comparator Clock Circuit



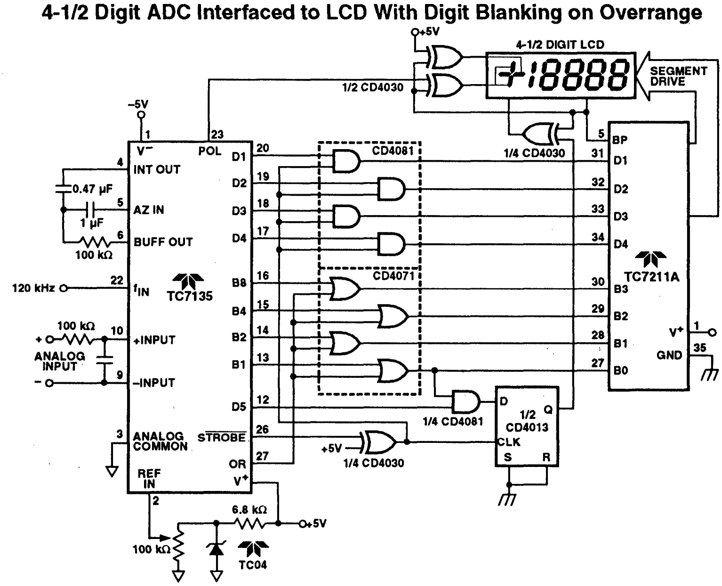
TC7135

TYPICAL APPLICATIONS DIAGRAMS (Cont.)

4-1/2 Digit ADC With Multiplexed Common Anode LED Display

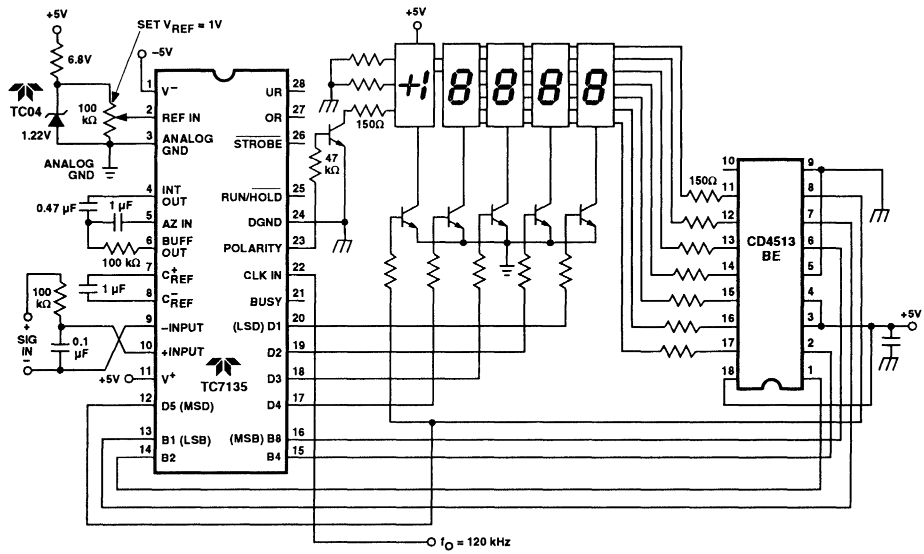


4-1/2 Digit ADC Interfaced to LCD With Digit Blanking on Overrange

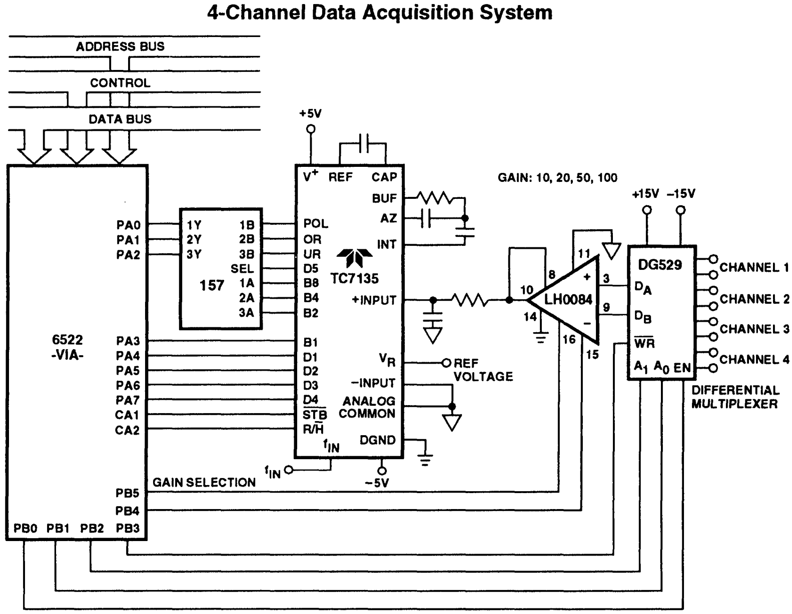


TYPICAL APPLICATIONS DIAGRAMS (Cont.)

4-1/2 Digit ADC With Multiplexed Common Cathode LED Display



4-Channel Data Acquisition System



NOTES

LOW POWER, 3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTERS

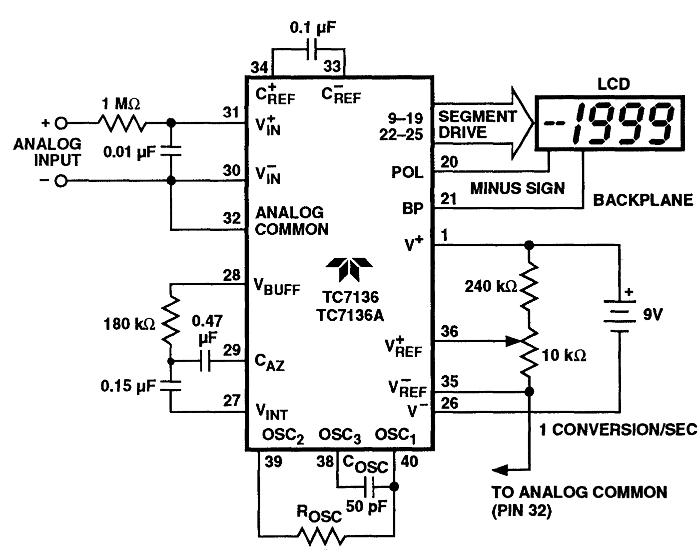
FEATURES

- Fast Overrange Recovery, Guaranteed First Reading Accuracy
- Low Temperature Drift Internal Reference
  - TC7136 .... 70 ppm/°C Typ
  - TC7136A .... 35 ppm/°C Typ
- Guaranteed Zero Reading With Zero Input
- Low Noise .... 15 μV_{P-P}
- High Resolution 0.05%
- Wide Dynamic Range .... 72 dB
- Low Input Leakage Current .... 1 pA Typ, 10 pA Max
- Direct LCD Drive — No External Components
- Precision Null Detectors With True Polarity at Zero
- High-Impedance Differential Input
- Convenient 9V Battery Operation With Low Power Dissipation .... 500 µW Typ, 900 µW Max
- Internal Clock Circuit
- Available in Compact Flat Package or PLCC
- Industrial Temperature Range Device Available

TYPICAL APPLICATIONS

- Thermometry
- Bridge Readouts
  - — Strain Gauges
  - — Load Cells
  - — Null Detectors
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity/Level
  - — Humidity
  - — Position
- Digital Scales
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Gaussometers
- Photometers

TYPICAL OPERATING CIRCUIT



LOW POWER, 3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTERS

TC7136
TC7136A

GENERAL DESCRIPTION

The TC7136 and TC7136A are low-power, 3-1/2 digit, liquid crystal display (LCD), analog-to-digital converters (ADCs). These devices incorporate an "integrator output zero" phase which guarantees overrange recovery. The performance of existing TC7126, TC7126A and ICL7126-based systems may be upgraded with minor changes to external, passive components.

The TC7136A has an improved internal zener reference voltage circuit which maintains the analog common temperature drift to 35 ppm/°C (typical) and 75 ppm/°C (maximum). This represents an improvement of two to four times over similar 3-1/2 digit converters. The costly, space-consuming external reference source may be removed.

The TC7136 limits linearity error to less than 1 count on 200 mV or 2V full-scale ranges. Roll-over error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High-impedance differential inputs offer 1 pA leakage currents and a $10^{12}\Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display readout for a 0V input.

The single-chip CMOS TC7136 incorporates all the active devices for a 3-1/2 digit ADC to directly drive an LCD. The internal oscillator, precision voltage reference, and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low-cost, high-resolution (0.05%) indicating meter requires only a display, four resistors, four capacitors and a 9V battery. The flat package option eases the mechanical design of low-cost, hand-held multimeters.

The TC7136A dual-slope conversion technique rejects interference signals if the converter's integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50 Hz, 60 Hz, and 400 Hz line frequency signals are present.

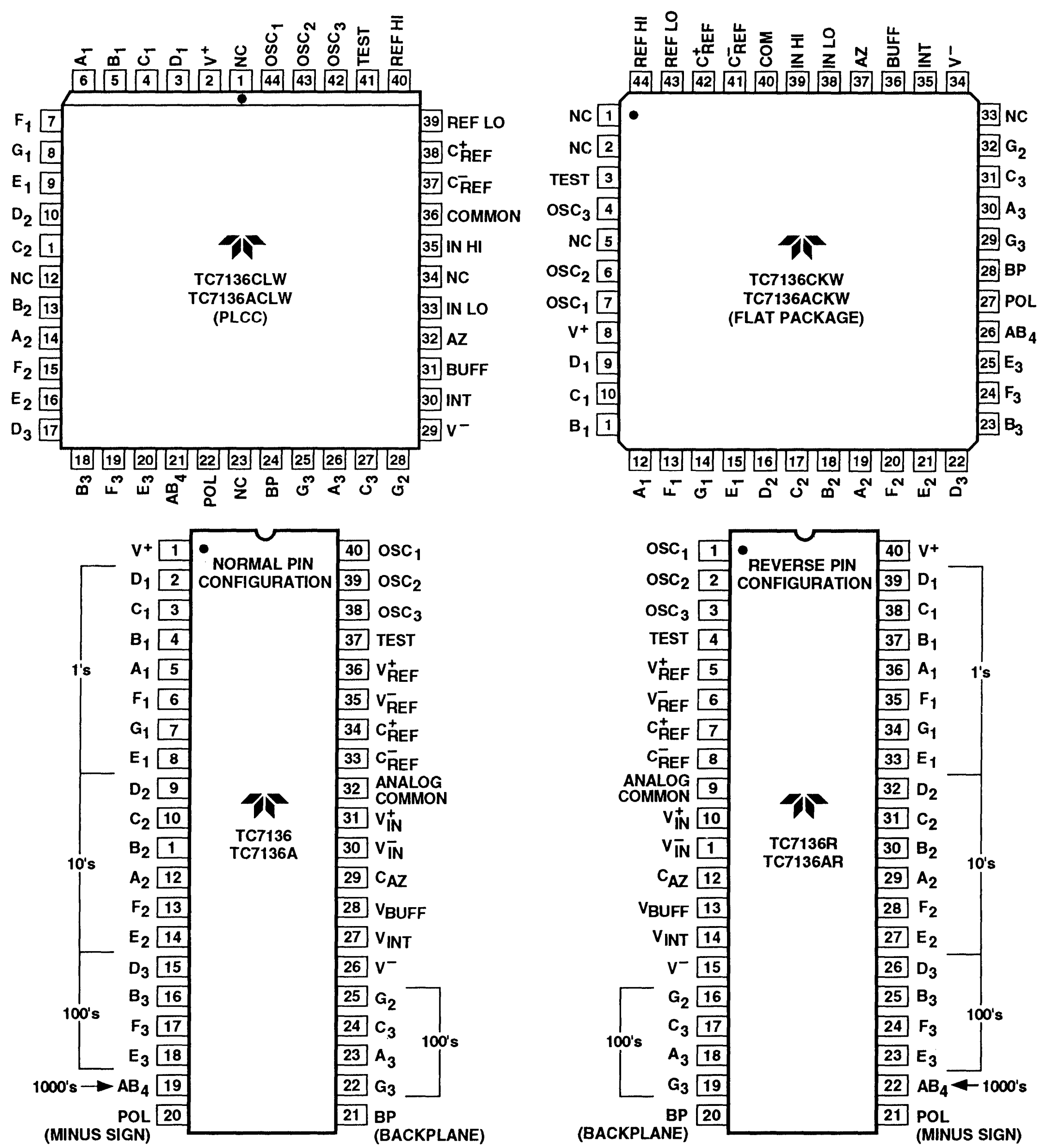
ORDERING INFORMATION

Part No.	Package	Pin Layout	Temperature Range	Reference Temperature Coefficient (Max)
TC7136ACPL	40-Pin Plastic DIP	Normal	0°C to +70°C	75 ppm/°C
TC7136CPL				150 ppm/°C
TC7136ARCPL	40-Pin Plastic DIP	Reversed	0°C to +70°C	75 ppm/°C
TC7136RCPL				150 ppm/°C
TC7136 AIJL	40-Pin CerDIP	Normal	–25°C to +85°C	100 ppm/°C
TC7136IJL				150 ppm/°C
TC7136ACKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	75 ppm/°C
TC7136CKW				150 ppm/°C
TC7136ACLW	44-Pin PLCC		0°C to +70°C	75 ppm/°C
TC7136CLW				150 ppm/°C

LOW POWER, 3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTERS

TC7136
TC7136A

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

TC7136
TC7136A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) ....+15V
Analog Input Voltage (Either Input) (Note 1) .... V^+ to V^-
Reference Input Voltage (Either Input) .... V^+ to V^-
Clock Input .... TEST to V^+
Power Dissipation (Note 2)
CerDIP (J) .... 1000 mW
Plastic DIP (P) .... 800 mW
Flat Package (K, L) .... 500 mW
Operating Temperature Range
C Devices .... 0°C to +70°C
I Devices .... –25°C to +85°C

Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 9V, f_{CLK} = 16 kHz, and T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
	Zero Input Reading	V_{IN} = 0V Full Scale = 200 mV	–000.0	±000.0	+000.0	Digital Reading
	Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C	—	0.2	1	µV/°C
	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
NL	Nonlinearity Error	Full Scale = 200 mV or 2V Max Deviation From Best Straight Line	–1	±0.2	1	Count
	Roll-Over Error	$-V_{IN}$ = $+V_{IN}$ ≈ 200 mV	–1	±0.2	1	Count
e_N	Noise	V_{IN} = 0V, Full Scale = 200 mV	—	15	—	μV_{P-P}
I_L	Input Leakage Current	V_{IN} = 0V	—	1	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200 mV	—	50	—	µV/V
	Scale Factor Temperature Coefficient	V_{IN} = 199 mV, 0°C ≤ T_A ≤ +70°C Ext Ref Temp Coeff = 0 ppm/°C	—	1	5	ppm/°C
Analog Common						
V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ 0°C ≤ T_A ≤ +70°C TC7136A "C" Commercial Temp TC7136 Range Devices	— —	35 70	75 150	ppm/°C ppm/°C
		–25°C ≤ T_A ≤ +85°C TC7136A "I" Industrial Temp TC7136 Range Devices	— —	35 70	100 150	ppm/°C ppm/°C
V_C	Analog Common Voltage	250 kW Between Common and V^+	2.7	3.05	3.35	V
LCD Drive						
V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
V_{BD}	LCD Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V_{P-P}
Power Supply						
I_S	Power Supply Current	V_{IN} = 0V, V^+ to V^- = 9V (Note 6)	—	70	100	µA

NOTES:
1. Input voltages may exceed supply voltages when input current is limited to 100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to PC board.
3. Refer to "Differential Input" discussion.
4. Backplane drive is in-phase with segment drive for "off" segment and 180° out-of-phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
5. See "Typical Operating Circuit".
6. A 48 kHz oscillator increases current by 20 µA (typical). Common current not included.

LOW POWER, 3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTERS

PIN DESCRIPTION

40-Pin DIP Pin Number Normal	(Reverse)	Name	Description
1	(40)	V^+	Positive supply voltage.
2	(39)	D_1	Activates the D section of the units display.
3	(38)	C_1	Activates the C section of the units display.
4	(37)	B_1	Activates the B section of the units display.
5	(36)	A_1	Activates the A section of the units display.
6	(35)	F_1	Activates the F section of the units display.
7	(34)	G_1	Activates the G section of the units display.
8	(33)	E_1	Activates the E section of the units display.
9	(32)	D_2	Activates the D section of the tens display.
10	(31)	C_2	Activates the C section of the tens display.
11	(30)	B_2	Activates the B section of the tens display.
12	(29)	A_2	Activates the A section of the tens display.
13	(28)	F_2	Activates the F section of the tens display.
14	(27)	E_2	Activates the E section of the tens display.
15	(26)	D_3	Activates the D section of the hundreds display.
16	(25)	B_3	Activates the B section of the hundreds display.
17	(24)	F_3	Activates the F section of the hundreds display.
18	(23)	E_3	Activates the E section of the hundreds display.
19	(22)	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	POL	Activates the negative polarity display.
21	(20)	BP	Backplane drive output.
22	(19)	G_3	Activates the G section of the hundreds display.
23	(18)	A_3	Activates the A section of the hundreds display.
24	(17)	C_3	Activates the C section of the hundreds display.
25	(16)	G_2	Activates the G section of the tens display.
26	(15)	V^-	Negative power supply voltage.
27	(14)	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build-up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See Integrating Capacitor section for additional details.
28	(13)	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 1.8 MΩ for 2V full-scale range.
29	(12)	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full scale, and a 0.1 μF capacitor for a 2V full scale. See paragraph on Auto-Zero Capacitor for more details.
30	(11)	V_{IN}^-	The low input signal is connected to this pin.
31	(10)	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	ANALOG COMMON	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on Analog Common for more details. It also acts as a reference voltage source.
33	(8)	C_{REF}^-	See pin 34.

PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	Name	Description
34	(7)	C_{REF}^{+}	A 0.1 µF capacitor is used in most applications. If a large common-mode voltage exists (for example, the V_{IN}^{-} pin is not at analog common), and a 200 mV scale is used, a 1 µF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	(6)	V_{REF}^{-}	See pin 36.
36	(5)	V_{REF}^{+}	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full scale. Place 1V between pins 35 and 36 for 2V full scale. See paragraph on Reference Voltage.
37	(4)	TEST	Lamp test. When pulled high (to V^{+}) all segments will be turned on and the display should read –1888. It may also be used as a negative supply for externally-generated decimal points. See paragraph under Test for additional information.
38	(3)	OSC_3	See pin 40.
39	(2)	OSC_2	See pin 40.
40	(1)	OSC_1	Pins 40, 39 and 38 make up the oscillator section. For a 48 kHz clock (3 readings per second) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC7136A is a dual-slope, integrating analog-to-digital converter. An understanding of the dual-slope conversion technique will aid in following detailed TC7136A operational theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period (t_{SI}), measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (t_{RI}).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\, t_{RI}}{RC},$$

where:

V_R = Reference voltage
t_{SI} = Signal integration time (fixed)
t_{RI} = Reference voltage integration time (variable).

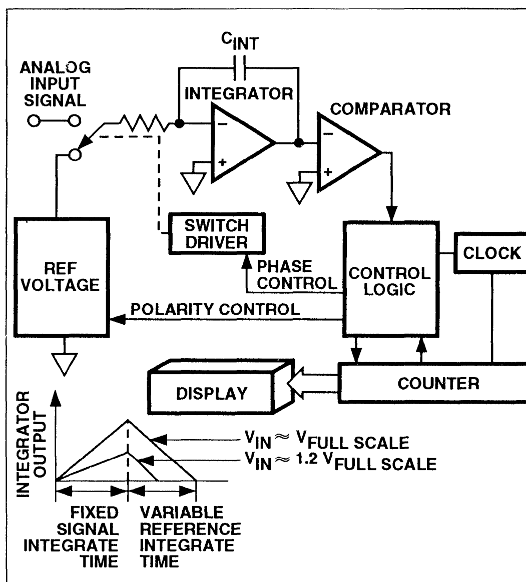


Figure 1 Basic Dual-Slope Converter

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{t_{RI}}{t_{SI}}\right].$$

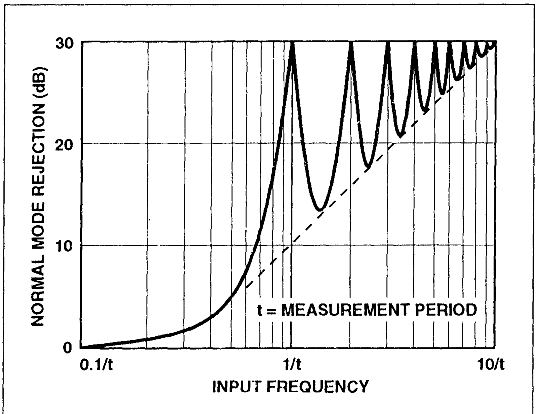


Figure 2 Normal-Mode Rejection of Dual-Slope Converter

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50 Hz/60 Hz power line period.

ANALOG SECTION

In addition to the basic integrate and deintegrate dual-slope cycles discussed above, the TC7136 and TC7136A designs incorporate an "integrator output-zero cycle" and an "auto-zero cycle." These additional cycles ensure the integrator starts at 0V (even after a severe overrange conversion) and that all offset voltage errors (buffer amplifier, integrator and comparator) are removed from the conversion. A true digital zero reading is assured without any external adjustments.

A complete conversion consists of four distinct phases:

(1) Integrator output-zero phase
(2) Auto-zero phase
(3) Signal integrate phase
(4) Reference deintegrate phase

Integrator Output-Zero Phase

This phase guarantees the integrator output is at 0V before the system-zero phase is entered. This ensures that true system offset voltages will be compensated for even after an overrange conversion. The count for this phase is a function of the number of counts required by the deintegrate phase.

The count lasts from 11 to 140 counts for non-overrange conversions and from 31 to 640 counts for overrange conversions.

Auto-Zero Phase

During the auto-zero phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero phase residual is typically 10 µV to 15 µV.

The auto-zero duration is from 910 to 2900 counts for non-overrange conversions and from 300 to 910 counts for overrange conversions.

Signal Integration Phase

The auto-zero loop is entered and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The TC7136A signal integration period is 1000 clock periods or counts. The externally-set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 1000,$$

where f_{OSC} = external clock frequency.

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication, in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Phase

The third phase is reference integrate or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously-charged reference capacitor. Circuitry within the chip ensures the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to

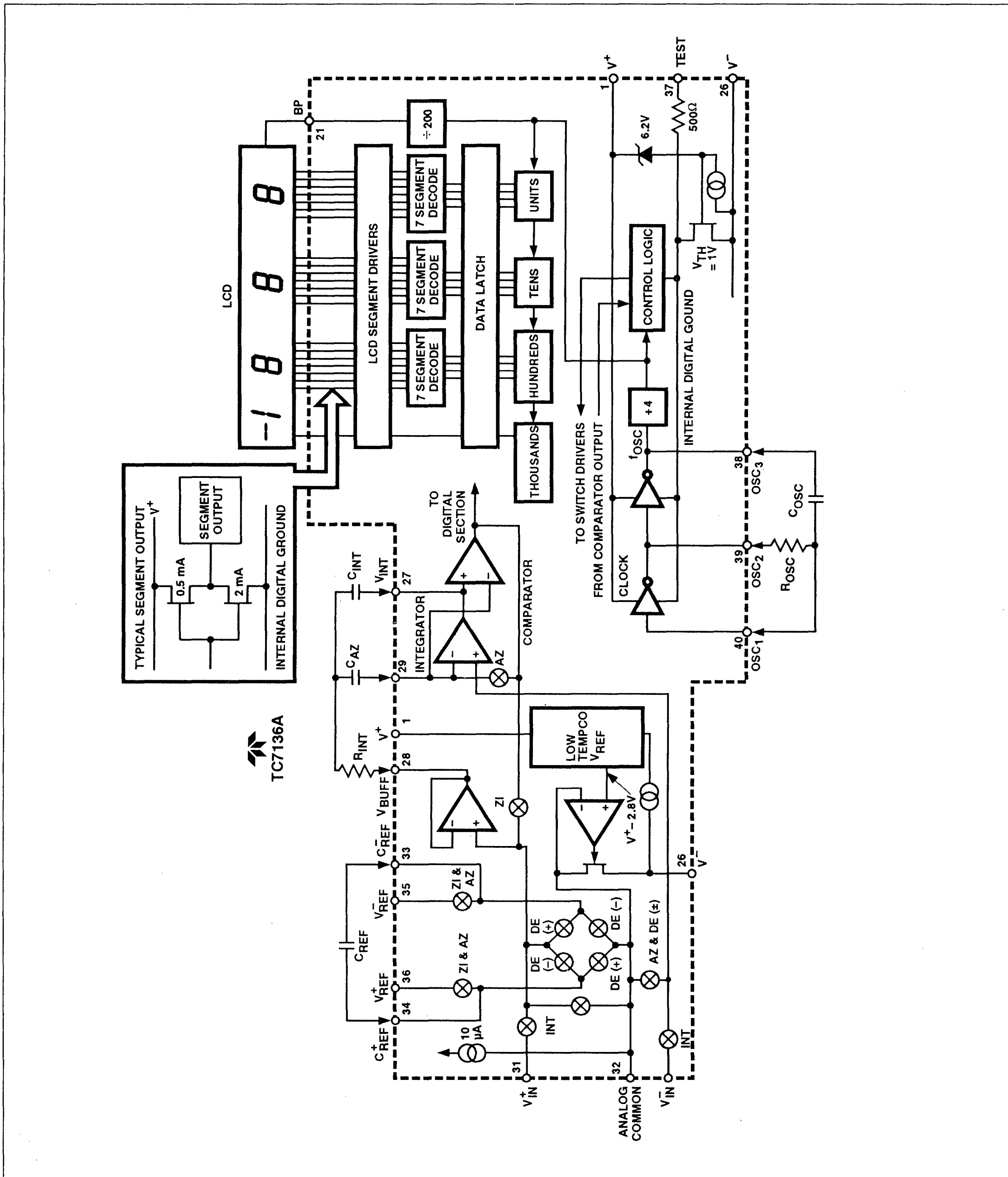


Figure 3 TC7136A Block Diagram

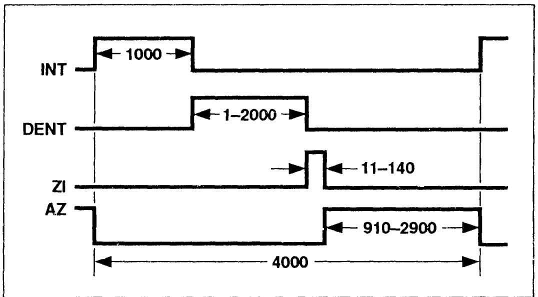


Figure 4 Conversion Timing During Normal Operation

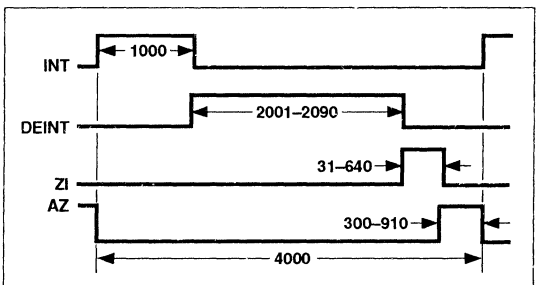


Figure 5 Conversion Timing During Overrange Operation

return to zero is proportional to the input signal and is between 0 and 2000 internal clock periods. The digital reading displayed is

$$1000 \frac{V_{IN}}{V_{REF}}$$

DIGITAL SECTION

The TC7136A contains all the segment drivers necessary to directly drive a 3-1/2 digit LCD. An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions per second the backplane frequency is 60 Hz with a 5V nominal amplitude. When a segment driver is in-phase with the backplane signal, the segment is "OFF." An out-of-phase segment drive signal causes the segment to be "ON," or visible. This AC drive configuration results in negligible DC voltage across each LCD segment, ensuring long LCD life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed, this indicator would reverse.

On the TC7136A, when the test pin is pulled to V^+, all segments are turned "ON." The display reads −1888. During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCDs may be destroyed if operated with DC levels for extended periods.

The display font and segment drive assignment are shown in Figure 6.

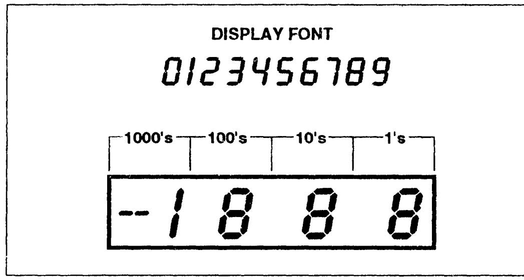


Figure 6 Display FONT and Segment Assignment

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The four-phase measurement cycle takes a total of 4000 counts, or 16,000 clock pulses. The 4000-count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

(1) Auto-zero phase: 3000 to 2900 counts
(1200 to 11,600 clock pulses)

(2) Signal integrate: 1000 counts
(4000 clock pulses)

This time period is fixed. The integration period is:

$$t_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right],$$

where f_{OSC} is the externally-set clock frequency.

(3) Reference integrate: 0 to 2000 counts

(4) Zero integrator: 11 to 640 counts

The TC7136 is a drop-in replacement for the TC7126 and ICL7126. The TC7136A offers a greatly-improved internal reference temperature coefficient. Minor component value changes are required to upgrade existing designs and improve the noise performance.

COMPONENT VALUE SELECTION

Auto-Zero Capacitor (C_{AZ})

The C_{AZ} capacitor size has some influence on system noise. A 0.47 µF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 µV. A 0.1 µF capacitor is adequate for 2V full-scale applications. A Mylar-type dielectric capacitor is adequate.

Reference Voltage Capacitor (C_{REF})

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate phase is stored on C_{REF}. A 0.1 μF capacitor is acceptable when V_{REF}^- is tied to analog common. If a large common-mode voltage exists ($V_{REF}^- \neq$ analog common) and the application requires a 200 mV full scale, increase C_{REF} to 1 μF. Roll-over error will be held to less than 0.5 count. A Mylar-type dielectric capacitor is adequate.

Integrating Capacitor (C_{INT})

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Analog common will normally supply the differential voltage reference this case, a ±2V full-scale integrator output swing is satisfactory. For 3 readings per second (f_{OSC} = 48 kHz) a 0.047 μF value is suggested. For one reading per second, 0.15 μF is recommended. If a different oscillator frequency is used, C_{INT} must be changed in inverse proportion to maintain the nominal ±2V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}},$$

where: f_{OSC} = Clock frequency at pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing.

C_{INT} must have low dielectric absorption to minimize roll-over error. An inexpensive polypropylene capacitor is recommended.

Integrating Resistor (R_{INT})

The input buffer amplifier and integrator are designed with Class A output stages. The output stage idling current is 6 μA. The integrator and buffer can supply 1 μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region, but not so large that PC board leakage currents induce errors. For a 200 mV full scale, R_{INT} is 180 kΩ. A 2V full scale requires 1.8 MΩ.

Component	Nominal Full-Scale Voltage	
Value	200 mV	2V
C_{AZ}	0.47 μF	0.1 μF
R_{INT}	180 kΩ	1.8 MΩ
C_{INT}	0.047 μF	0.047 μF

NOTE: f_{OSC} = 48 kHz (3 readings per sec). R_{OSC} = kΩ, C_{OSC} = 50 pF.

Oscillator Components

C_{OSC} should be 50 pF. R_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}.$$

Note that f_{OSC} is ÷4 to generate the TC7136A's internal clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings per second) will reject both 50 Hz and 60 Hz (also 400 Hz and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200 mV	100 mV
2V	1V

*$V_{FS} = 2\ V_{REF}$.

In some applications, a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output for 2000 lb/in.^{2} is 400 mV. Rather than dividing the input voltage by two, the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

DEVICE PIN FUNCTIONAL DESCRIPTION

Differential Signal Inputs

V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30)

The TC7136A is designed with true differential inputs and accepts input signals within the input stage common-mode voltage range (V_{CM}). The typical range is $V^+ - 1V$ to $V^- + 1V$. Common-mode voltages are removed from the system when the TC7136A operates from a battery or floating power source (isolated from measured system), and V_{IN}^- is connected to analog common (V_{COM}). (See Figure 7.)

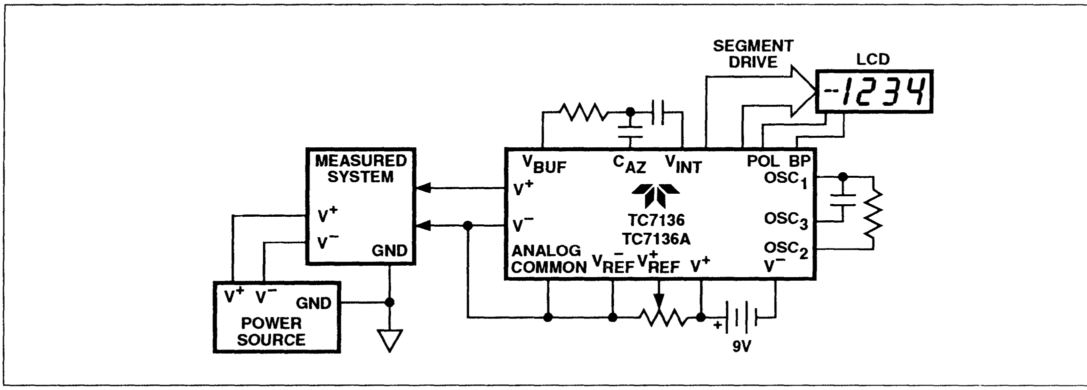


Figure 7 Common-Mode Voltage Removed in Battery Operation With V_{IN} = Analog Common

In systems where common-mode voltages exist, the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. A worst-case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (see Figure 8.) For such applications, the integrator output swing can be reduced below the recommended 2V full-scale swing. The integrator output will swing within 0.3V of V^+ or V^- without increased linearity error.

Differential Reference

V_{REF}^+ (Pin 36), V_{REF}^- (Pin 35)

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent roll-over type errors being induced by large common-mode voltages, C_{REF} should be large compared to stray node capacitance.

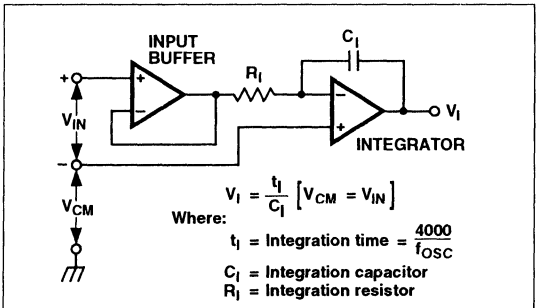


Figure 8 Common-Mode Voltage Reduces Available Integrator Swing ($V_{COM} \neq V_{IN}$)

The TC7136A offers a significantly improved analog common temperature coefficient. This potential provides a very stable voltage, suitable for use as a voltage reference. The temperature coefficient of analog common is typically 35 ppm/°C.

ANALOG COMMON (Pin 32)

The analog common pin is set at a voltage potential approximately 3V below V^+. The potential is guaranteed to be between 2.7V and 3.35V below V^+. Analog common is tied internally to an N-channel FET capable of sinking 100μA. This FET will hold the common line at 3V below V^+ if an external load attempts to pull the common line toward V^+. Analog common source current is limited to 1 μA. Analog common is therefore easily pulled to a more negative voltage (i.e., below V^+ –3V).

The TC7136A connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero phase. During the reference-integrate phase, V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists, but is rejected by the converter's 86 dB common-mode rejection ratio. In battery operation, analog common and V_{IN}^- are usually connected, removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference, or common point. The TC7136A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC7136A power source. The analog common potential of V^+ –3V gives a 7V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient.

With sufficiently high total supply voltage ($V^+ - V^- > 7V$), analog common is a very stable potential with excellent temperature stability (typically 35 ppm/°c). This potential can be used to generate the TC7136A's reference voltage. An external voltage reference will be unnecessary in most cases because of the 35 ppm/°C temperature coefficient. See TC7136A Internal Voltage Reference discussion.

TEST (Pin 37)

The test pin potential is 5V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally-generated negative logic supply through a 500Ω resistor. The test pin load should not be more than 1 mA. See the Applications Section for additional information on using test as a negative digital logic supply.

If test is pulled high (to V^+), all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes. With Test = V^+, the LCD segments are impressed with a DC voltage which will destroy the LCD.

TC7136A Internal Voltage Reference

The TC7136 analog common voltage temperature stability has been significantly improved (Figure 9). The "A" version of the industry-standard TC7136 device allows users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed; however, noise performance will be improved by increasing C_{AZ}. (See Auto-Zero Capacitor section.) Figure 10 shows analog common supplying necessary voltage reference for the TC7136A.

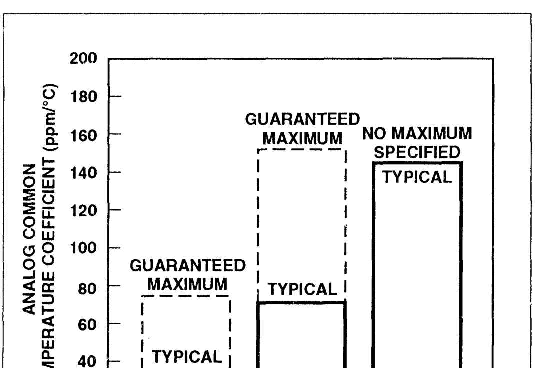


Figure 9 Analog Common Temperature Coefficient

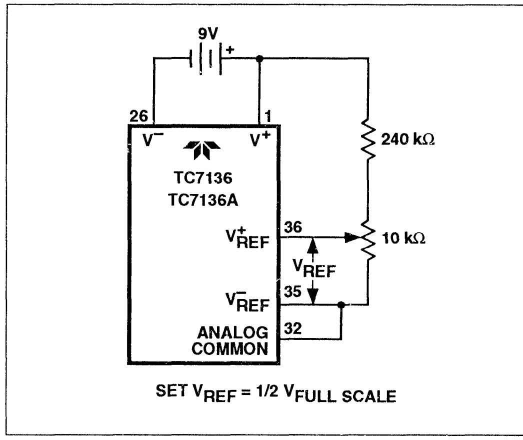


Figure 10 TC7136A Internal Voltage Reference Connection

APPLICATIONS INFORMATION

Liquid Crystal Display Sources

Several manufacturers supply standard LCDs to interface with the TC7136A 3-1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers*
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216-655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415-347-9916	FE 0801, FE 0203
VGI, Inc.	1800 Vernon St., Ste. 2 Roseville, CA 95678 916-783-7878	I1048, I1126
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414-648-2361	3902, 3933, 3903

***NOTE:** Contact LCD manufacturer for full product listing/specifications.

Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5V below V^+.

Ratiometric Resistance Measurements

The TC7136A's true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately-defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed reading} = \frac{R_{UNKNOWN}}{R_{STANDARD}} \times 1000.$$

The display will overrange for $R_{UNKNOWN} \geq 2 \times R_{STANDARD}$.

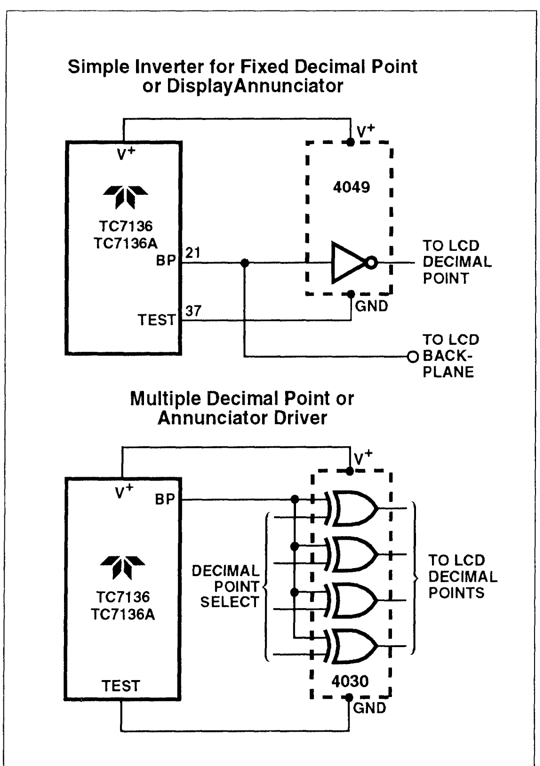


Figure 11 Decimal Point and Annunciator Drives

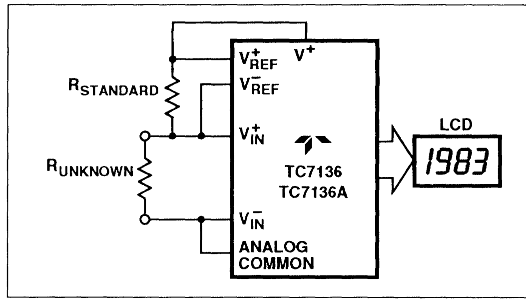


Figure 12 Low Parts Count Ratiometric Resistance Measurement

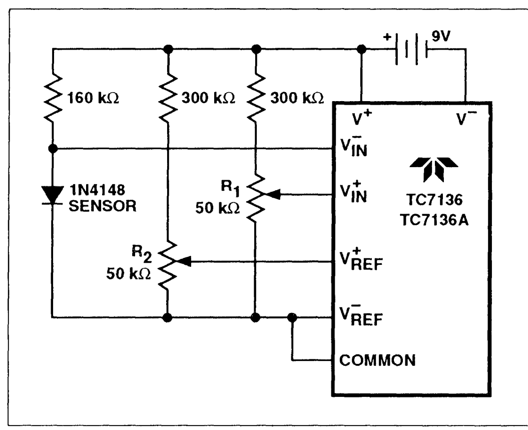


Figure 13 Temperature Sensor

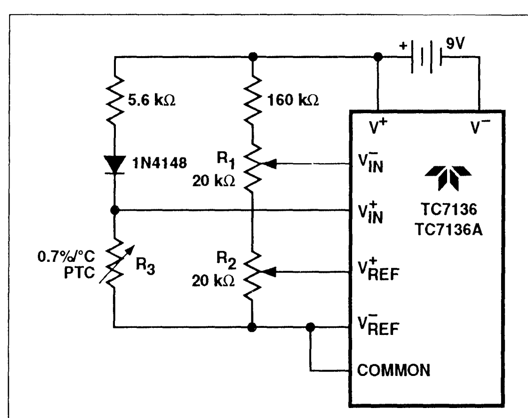


Figure 14 Positive Temperature Coefficient Resistor Temperature Sensor

NOTES

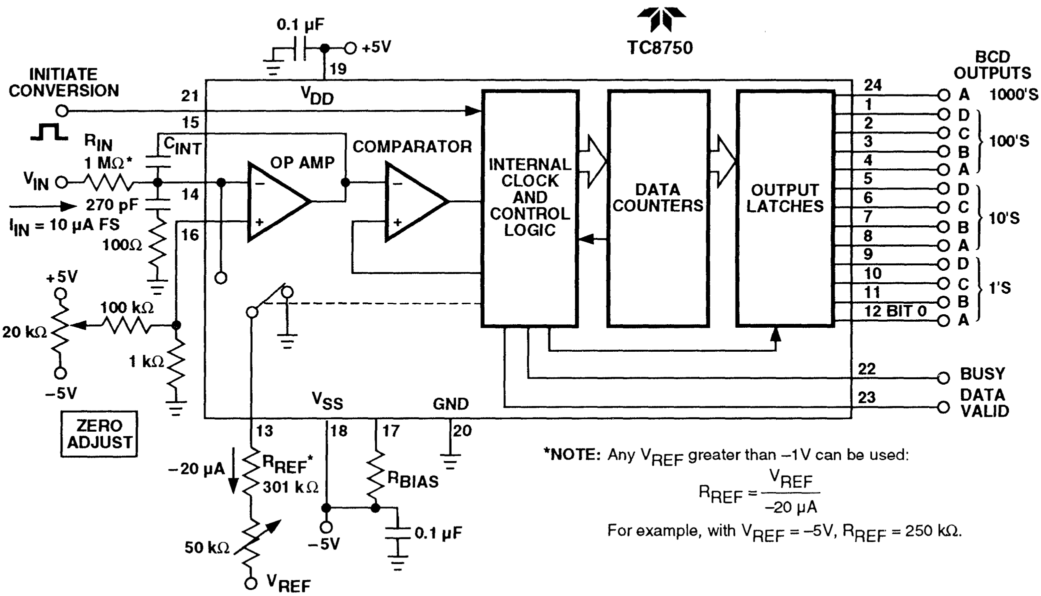
TELEDYNE COMPONENTS

3-1/2 DIGIT ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL BDC OUTPUT

FEATURES

- High Accuracy, 3-1/2 Digit Resolution With <±0.025% Error
- Military Temperature Range Devices
- Monotonic Performance
  - No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation ....20 mW Typ
- Contains All Required Active Elements
  - Needs Only Passive Support Components, Reference Voltage, and Dual Power Supplies
- High Stability Over Full Temperature Range
  - Gain Temperature Coefficient ... <25 ppm/°C Typ
  - Zero Drift .... <30 μV/°C Typ
  - Differential Nonlinearity Drift ... <2.5 ppm/°C Typ
- Latched Parallel BDC Outputs
- LPTTL and CMOS Compatible Outputs and Control Inputs
- Strobed or Free-Running Conversion
- Infinite Input Range
  - Any Positive Voltage Can Be Applied via a Scaling Resistor

TEST CIRCUIT



*NOTE: Any V_{REF} greater than –1V can be used:

$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example, with V_{REF} = –5V, R_{REF} = 250 kΩ.

3-1/2 DIGIT ADC WITH PARALLEL BDC OUTPUT

TC8750

GENERAL DESCRIPTION

The TC8750 is a 3-1/2 digit, monolithic CMOS analog-to-digital converter. Fully self-contained in a single 24-pin dual-in-line package, the converter requires only passive support components, voltage or current references, and power supplies.

Conversion is performed by an incremental charge-balancing technique which has inherently high accuracy, linearity, and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current. The number of pulses (charge increments) needed to maintain the amplifier summing junction near zero are counted. At the end of conversion, the total count is latched into the digital outputs in a 3-1/2 digit, parallel BDC digit format.

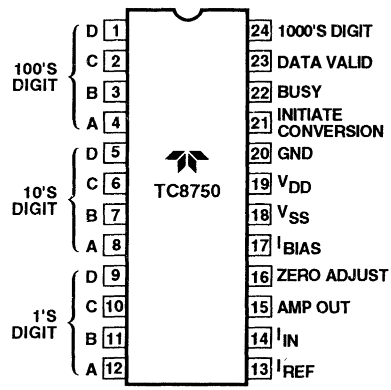
ORDERING INFORMATION

Part No.	Package	Temperature Range
TC8750CPG	24-Pin Plastic DIP	0°C to +70°C
TC8750EHG	24-Pin CerDIP	–40°C to +85°C
TC8750MHG	24-Pin CerDIP	–55°C to +125°C

HANDLING PRECAUTIONS

CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power-on" conditions, as high transients may cause permanent damage.

PIN CONFIGURATION



3-1/2 DIGIT ADC WITH PARALLEL BDC OUTPUT

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, V_{DD} = +5V, V_{SS} = –5V, V_{GND} = 0V, V_{REF} = –6.4V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = +25°C unless full temperature range is specified (–55°C to +125°C for MH package, –40°C to +85°C for EH package, 0° to +70°C for CP package).

Parameter	Definition	Conditions	Min	Typ	CP/EH Max	MH Max	Unit
Accuracy							
Resolution Accuracy	BCD Word Length of Digital Output		3-1/2 (1999 Counts)	—	—	—	Digits
Relative Accuracy	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input		—	—	0.025	0.025	%
Differential Nonlinearity	Deviation From 1 LSB Between Transition Points		—	—	—	0.025	%
Differential Nonlinearity Temperature Drift	Variation in Differential Nonlinearity Due to Temperature Change	Full Temperature Range	—	±2.5	±5	±5	ppm/°C
Gain Variance	Variation From Exact (Compensate By Trimming R_{IN} or R_{REF})		—	±2	±5	±5	% of Nominal
Gain Temperature Drift	Variation In A Due to Temperature Change	Full Temperature Range	—	±25	±75	±80	ppm/°C
Zero Offset	Correction at Zero Adjust to Give Zero Output When Input is Zero	I_{IN} = 0	—	±10	±50	±50	mV
Zero Temperature Drift	Variation in Zero Offset Due to Temperature Change	Full Temperature Range	—	±3	±5	±8	ppm/°C
Analog Input (See Note)							
I_{IN} Full Scale	Full-Scale Analog Input Current to Achieve Specified Activity		—	10	—	—	µA
I_{REF}	Reference Current Input to Achieve Specified Accuracy		—	–20	—	—	µA
Digital Input							
$V_{IN}^{(1)}$	Logical "1" Input Threshold Current to Achieve Specified Activity		—	10	—	—	µA
$V_{IN}^{(0)}$	Logical "0" Input Threshold for Initiate Conversion Input	Full Temperature Range	—	—	1.5	1.5	V
Digital Output							
$V_{OUT}^{(1)}$	Logical "1" Output Voltage for Digits Out, Busy, and Data Valid Outputs	Full Temperature Range I_{OUT} = –10 µA I_{OUT} = –500 µA	4.5	—	—	—	V
$V_{OUT}^{(0)}$	Logical "0" Output Voltage for Digits Out, Busy, and Data Valid Outputs	Full Temperature Range V_{DD} = 4.75V I_{OUT} = 500 µA	—	—	0.4	0.4	V
Dynamic							
Conversion Time	Time Required to Perform One Complete A/D Conversion	Full Temperature Range	—	10	12	12	ms

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Definition	Conditions	Min	Typ	CP/EH Max	MH Max	Unit
Dynamic (Cont.)							
Conversion Rate in Free-Run Mode		$V_{INT\ CONV}$ = +5V	84	100	—	—	Conv per sec
Minimum Pulse Width for Initiate Conversion		Full Temperature Range	500	—	—	—	ns
Supply Current							
I_{DD} Quiescent (H Package)	Current Required From Positive Supply During Operation	Full Temperature Range	—	1.4	2.5	3.5	mA
(P Package)		$V_{INT\ CONV}$ = 0V	—	1.4	5		mA
I_{SS} Quiescent (H Package)	Current Required From Negative Supply During Operation	Full Temperature Range	—	−1.6	−2.5	−3.5	mA
(P Package)		$V_{INT\ CONV}$ = 0V	—	−1.6	−5		mA
Supply Sensitivity	Change in Full-Scale Gain vs Supply Voltage Change	V_{DD} ± 1V, V_{SS} ±1V	—	±0.5	±1	±1	%/V
$\lvert V_{DD} \rvert = \lvert V_{SS} \rvert$ = 5V ±1V	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies		±0.05	±0.1	±0.1	±0.1	%/V

NOTE: I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

CIRCUIT DESCRIPTION

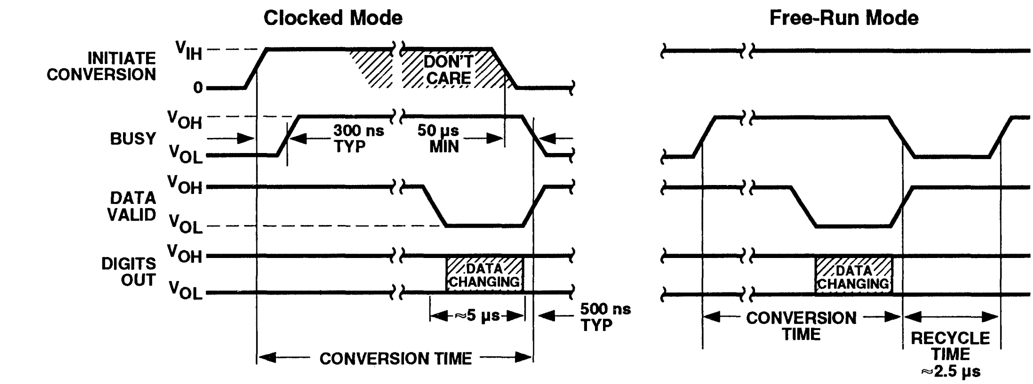
During conversion, the sum of a continuous current (I_{IN}) and pulses of a reference current (I_{REF}) are integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge is counted and the result (in BCD) is latched into the outputs at the end of conversion.

The conversion contains two counters and a clock, in addition to an operational amplifier, comparator, latching, output buffers, and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine.

The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times I_{REF} is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 µs (times given are appropriate) start-up cycle begins. The integrating capacitor is discharged and both counters are reset during this start-up period. Conversion begins at the end of the reset pulse and ends with a pulse generated by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 µs shutdown cycle. During the shutdown cycle, Data Valid goes low for 5 µs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

TIMING DIAGRAMS



NOTE: Rise and fall times = 200 ns typical, C_L = 50 pF.

PIN FUNCTIONS

Initiate Conversion Input

Accepts CMOS and most 5V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 µA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 µs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 µA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 µs before the completion of a conversion cycle. During this 5 µs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Output (1's, 10's, 100's, 1000's)

The BDC digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

APPLICATIONS INFORMATION

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \bullet A \bullet R_{REF}}{R_{IN} \bullet V_{REF}}$$

$$A = 4128$$

where digital counts is the value of the BCD output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Output
$V_{IN} \leq$ Full Scale	1100110011001
= Full Scale –1 LSB	1100110011001
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

External Component Selection

Obtaining a high-accuracy conversion system depends on the voltage regulation of V_{REF}, and thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. Supply connections V_{DD} and V_{SS} should have bypass capacitors of 0.1 µF or larger value right at the device pins.

R_{IN}, R_{REF}

Values of these components are chosen to give a full-scale input current of approximately 10 µA and a reference current of approximately –20 µA.

$$R_{IN} \approx \frac{V_{IN} \text{ Full Scale}}{10\ \mu A} \qquad R_{REF} \approx \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \approx \frac{10V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \approx \frac{-6.4V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations; the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} full scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the TC8750 are based on R_{BIAS} = 100 kΩ ±10%, unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and supply current. By decreasing R_{BIAS}, the ADC will convert much faster and the supply current will be much higher (e.g., when R_{BIAS} = 20 kΩ, the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA). Likewise, if R_{BIAS} is increased, the conversion time will be longer and the supply current will be much lower. (e.g., when R_{BIAS} = 1 MΩ, the conversion time will be six times longer, and the supply current is now reduced to 0.5 mA).

For details of this relationship, refer to the typical performance curves in Application Note 9.

R_{DAMP}

Exact value not critical, but should have a nominal value of 100Ω ±10%. Locate close to pin 14.

C_{DAMP}

Exact value not critical, but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

Exact value not critical, but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded, Locate as close as possible to pins 14 and 15.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5V are recommended with 0.05% line and load regulation and 0.1 µF decoupling capacitors.

Adjustment Procedure

The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e., below zero and above full scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

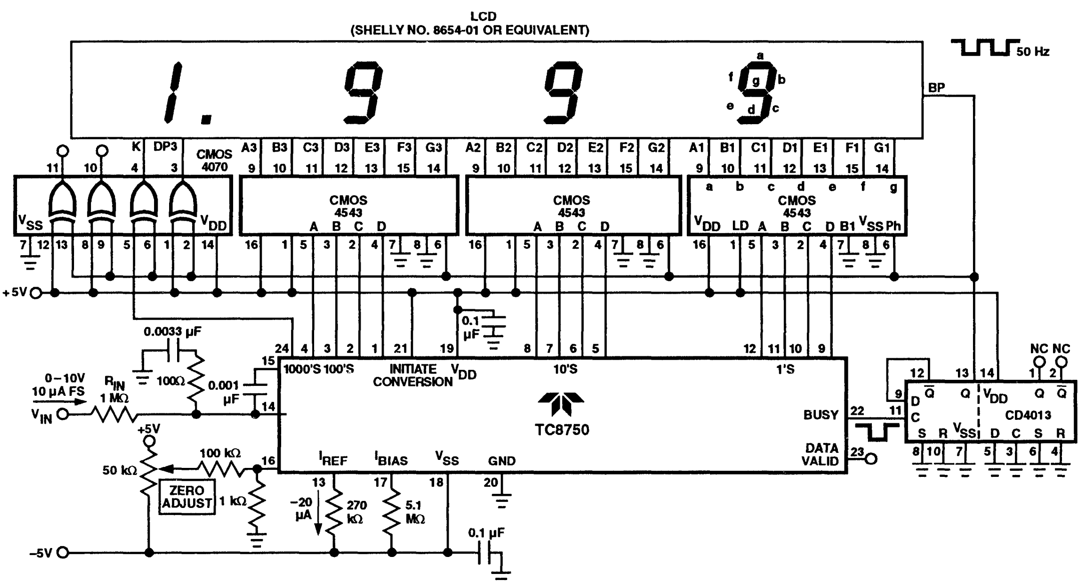
1. Set the initiate conversion control high to provide free-run operation, and verify that converter is operating.
2. Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
3. For full scale adjustment, set V_{IN} to the full scale value less 1-1/2 LSB, and trim the gain adjust circuit for a 1100110011000 to 1100110011001 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

3-1/2 DIGIT ADC WITH PARALLEL BDC OUTPUT

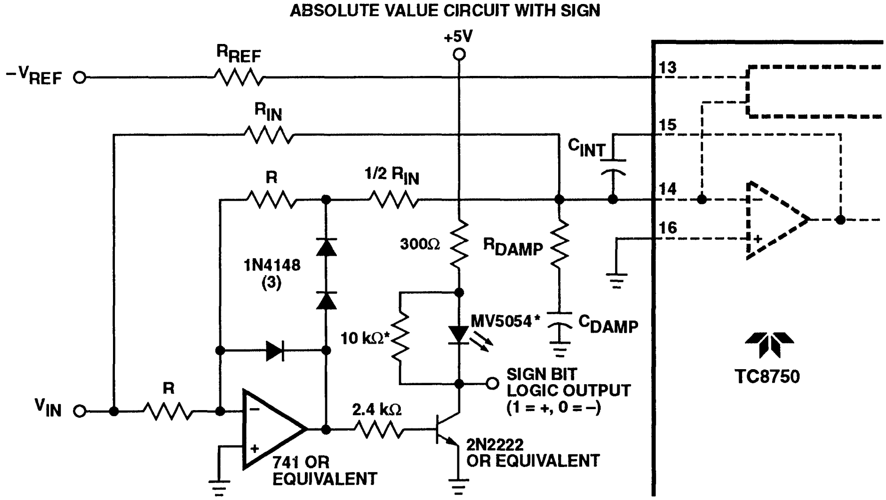
APPLICATION/DESIGN CIRCUITS

3-1/2 ADC With LCD



Bipolar Operation (+ and – Inputs)

ABSOLUTE VALUE CIRCUIT WITH SIGN

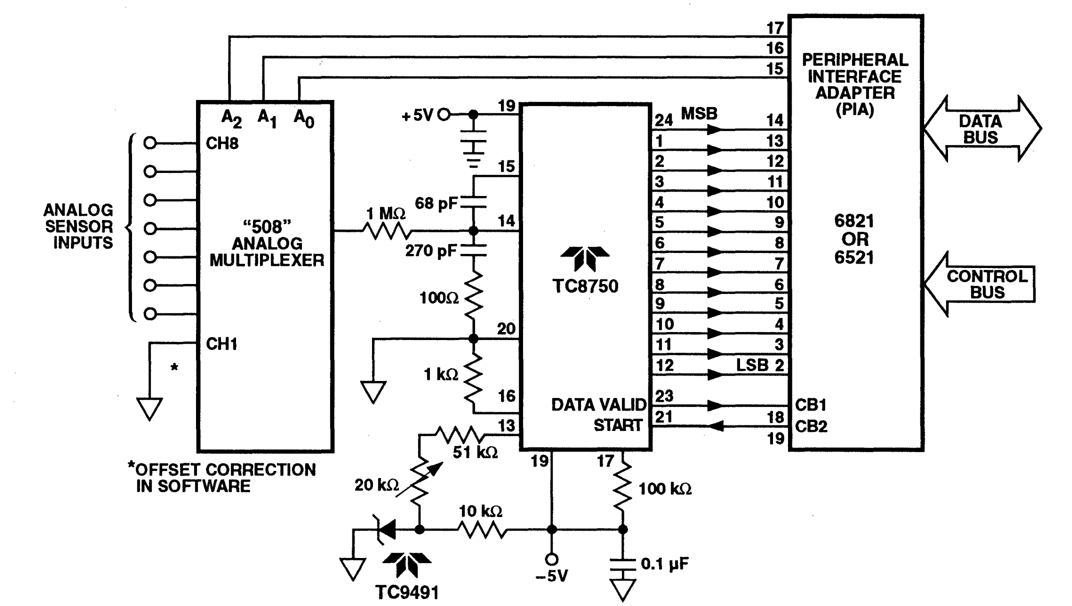


*Optional visual indication of negative input.

NOTE: Values for R should be between 10 kΩ and 100 kΩ.

APPLICATION/DESIGN CIRCUITS (Cont.)

Microprocessor-Based ADC System



TELEDYNE COMPONENTS

TC14433
TC14433A
TC14433B

3-1/2 DIGIT ADC

FEATURES

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999V and 199.9 mV
- Up to 25 Conversions Per Second
- Z_{IN} > 1000M Ohms
- Single Positive Voltage Reference
- Auto-Polarity and Auto-Zero
- Overrange and Underrange Signals Available
- Operates in Auto-Ranging Circuits
- Uses On-Chip System Clock or External Clock
- Wide Supply Range: e.g., ±4.5V to ±8V
- Available in Surface-Mount Packages

APPLICATIONS

- Portable Instruments
- Digital Voltmeters
- Digital Panel Meters
- Digital Scales
- Digital Thermometers
- Remote A/D Sensing Systems
- MPU Systems
- See Application Notes 19 and 21

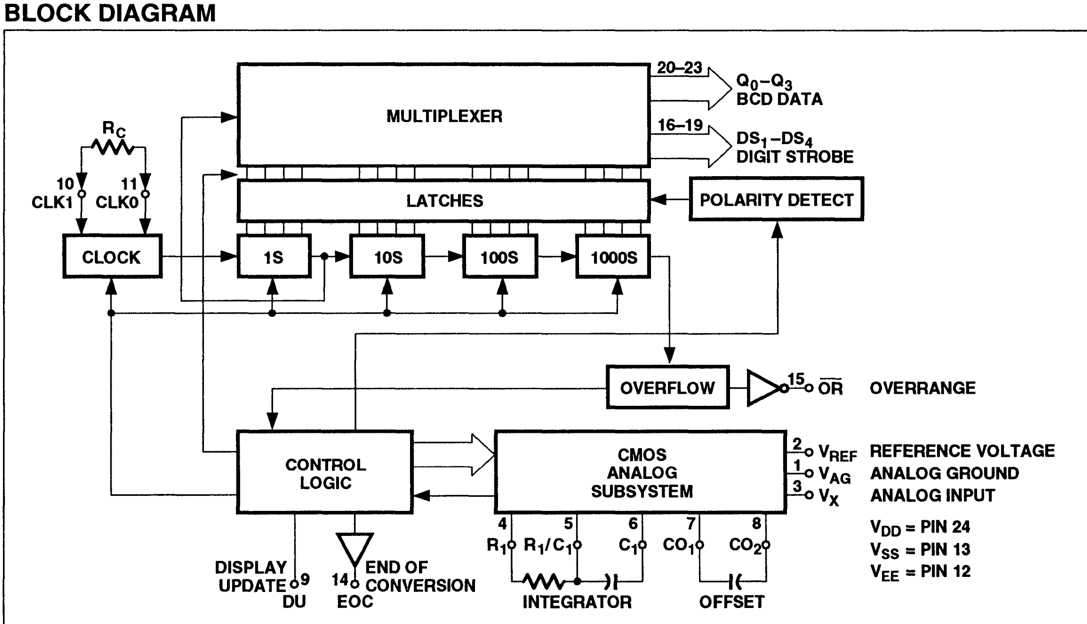
GENERAL DESCRIPTION

The TC1433 is a low power, high-performance, monolithic CMOS 3-1/2 digit A/D converter. The TC14433 combines both analog and digital circuits on a single IC, thus minimizing the number of external components. This dual-slope A/D converter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full-scale voltage range of this ratiometric IC extends from 199.9 millivolts to 1.999 volts. The TC14433B can operate over a wide range of power supply voltages, including batteries and standard 5-volt supplies.

The TC14433 will interface with the TC7211A (LCD)and TC7212A (LED) display drivers.

The TC14433A/B feature improved performance over the industry standard TC14433. Rollover, which is the measurement of identical positive and negative signals, is guaranteed to have the same reading within one count for the TC14433A, and within four counts for the TC14433B. Power consumption of the TC14433A/B is typically 4 mW, approximately one-half that of the industry standard TC14433.

BLOCK DIAGRAM



TC14433
TC14433A
TC14433B

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD} to V_{EE}	–0.5 to +18	Vdc
Voltage, Any Pin, Referenced to V_{EE}	V	–0.5 to V_{DD} +0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 or V_{EE})

Parameter	Symbol	Value	Unit
DC Supply Voltage:			
V_{DD} to Analog Ground	V_{DD}	+5 to +8	Vdc
V_{EE} to Analog Ground	V_{EE}	–2.8 to –8	Vdc
Clock Frequency	f_{CLK}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 to ±20%	μF

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(C_I = 0.1 μF mylar, R_I = 470 kΩ at V_{REF} = 2V, R_I = 27 kΩ at V_{REF} = 200 mV, C_O = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

Characteristic	Symbol	V_{DD}	V_{EE}	–40°C		25°C			85°C		Unit
		Vdc	Vdc	Min	Max	Min	Typ	Max	Min	Max	
Analog Input											
Rollover Error (Difference in reading for equal positive and	14433A			—	—	–1	—	+1	—	—	Counts
negative reading near full-scale)	14433B			—	—	–4	—	+4	—	—	
$-V_{IN} = +V_{IN}$: 200 mV Full-Scale	14433			—	—	—	—	—	—	—	
Linearity Output Reading (Note 1)	—										
(V_{REF} = 2V)		5	–5	—	—	–0.05	+0.05	+0.05	—	—	%rdg
(V_{REF} = 200 mV)		5	–5	—	—	–1 count	—	+1 count	—	—	
Stability Output Reading (Note 2)	—										
(V_X = 1.99V, V_{REF} = 2V)		5	–5	—	—	—	—	2	—	—	LSD
(V_X = 199 mV, V_{REF} = 200 mV)		5	–5	—	—	—	—	3	—	—	LSD
Zero Output Reading (V_X = 0V, V_{REF} = 2V)	—	5	–5	—	—	—	0	0	—	—	LSD
Bias Current:											
Analog Input	—	5	–5	—	—	—	±20	±100	—	—	pA
Reference Input	—	5	–5	—	—	—	±20	±100	—	—	pA
Analog Ground	—	5	–5	—	—	—	±20	±500	—	—	pA
Common-Mode Rejection (V_X = 1.4V, V_{REF} = 2V, f_{OC} = 32 kHz)		5	–5	—	—	—	65	—	—	—	dB
Digital											
Output Voltage — Pins 14 to 23											
(V_{SS} = 0V) "0" Level	V_{OL}	5	–5	—	0.05	—	0	0.05	—	0.05	V
"1" Level	V_{OH}	5	–5	4.95	—	4.95	5	—	4.95	—	V
(V_{SS} = –5V) "0" Level	V_{OL}	5	–5	—	–4.95	—	–5	–4.95	—	–4.95	V
"1" Level	V_{OH}	5	–5	4.95	—	4.95	5	—	4.95	—	V

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	–40°C Min	–40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Output Current — Pins 14 to 23											
(V_{SS} = 0V)											
(V_{OH} = 4.6V) Source	I_{OH}	5	–5	–0.25	—	–0.2	–0.36	—	–0.14	—	mA
(V_{OL} = 0.4V) Sink	I_{OL}	5	–5	0.64	—	0.51	0.88	—	0.36	—	mA
(V_{SS} = 0V)											
(V_{OH} = 5V) Source	I_{OH}	5	–5	–0.62	—	–0.5	–0.9	—	–0.35	—	mA
(V_{OL} = –4.5V) Sink	I_{OL}	5	–5	1.6	—	1.3	2.25	—	0.9	—	mA
Clock Frequency (R_C = 300 kΩ)	f_{CLK}	5	–5	—	—	—	66	—	—	—	kHz
Input Current — DU	I_{DU}	5	–5	—	±0.3	—	±0.00001	±0.3	—	±1	µA
Power											
Quiescent Current		5	–5	—	3.7	—	0.4	2	—	1.6	mA
(V_{DD} to V_{EE}, I_{SS} = 0) 14433A/B	I_Q	8	–8	—	7.4	—	1.4	4	—	3.2	mA
14433	I_Q	5	–5	—	3.7	—	0.9	2	—	1.6	mA
		8	–8	—	7.4	—	1.8	4	—	3.2	mA
Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2V)	—	5	–5	—	—	—	0.5	—	—	—	mV/V

NOTES: 1. Accuracy — The accuracy of the meter at full-scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full-scale and zero is defined as the linearity specification.
2. Three LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.
3. Pin numbers refer to 24-pin DIP.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC14433AEPG TC14433BEPG TC14433EPG	24-Pin Plastic DIP	–40°C to +85°C
TC14433EJG TC14433EJG TC14433EJG	24-Pin CerDIP	–40°C to +85°C
TC14433ELI	28-Pin PLCC	-40°C to +85°C
TC14433AELI	28-Pin PLCC	-40°C to +85°C

Part No.	Package	Temperature Range
TC14433EBQ TC14433EBQ	60-Pin Plastic Flat Package: Formed Leads	–40°C to +85°C

TC14433
TC14433A
TC14433B

TYPICAL CHARACTERISTICS

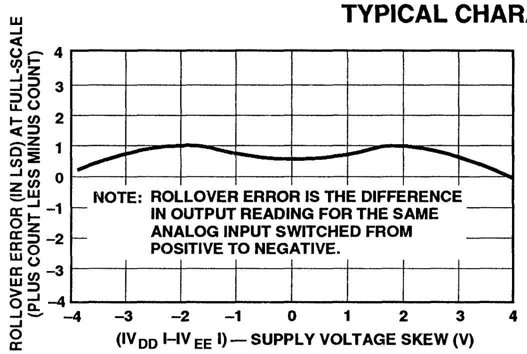


Figure 1. Typical Rollover Error vs Power Supply Skew

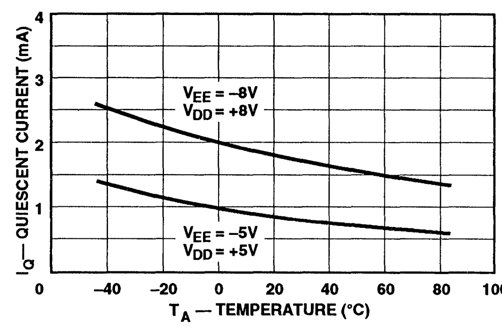


Figure 2. Typical Quiescent Power Supply Current vs Temperature

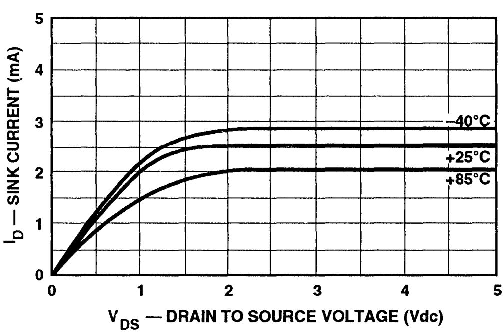


Figure 3. Typical N-Channel Sink Current at V_{DD}–V_{SS} = 5 Volts

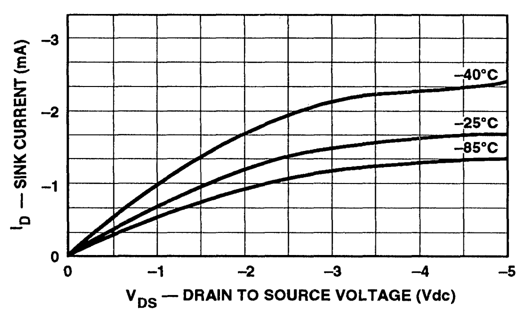


Figure 4. Typical P-Channel Source Current at V_{DD}–V_{SS} = 5 Volts

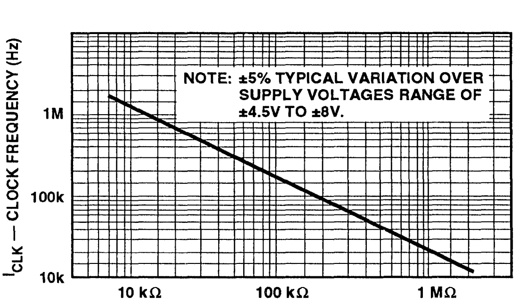


Figure 5. Typical Clock Frequency vs Resistor (R_C)

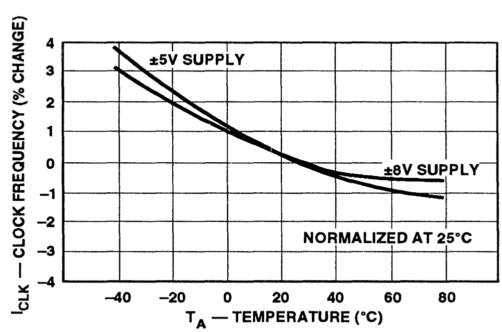


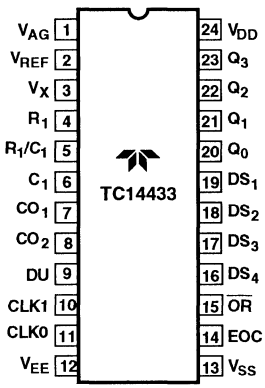
Figure 6. Typical % Change of Clock Frequency vs Temperature

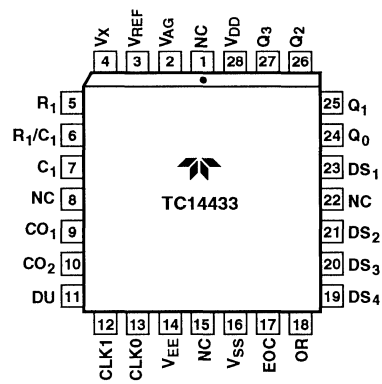
$$\text{CONVERSION RATE} = \frac{\text{CLOCK FREQUENCY}}{16{,}400} \pm 1.5\%$$

$$\text{MULTIPLEX RATE} = \frac{\text{CLOCK FREQUENCY}}{80}$$

TC14433
TC14433A
TC14433B

PIN CONFIGURATIONS



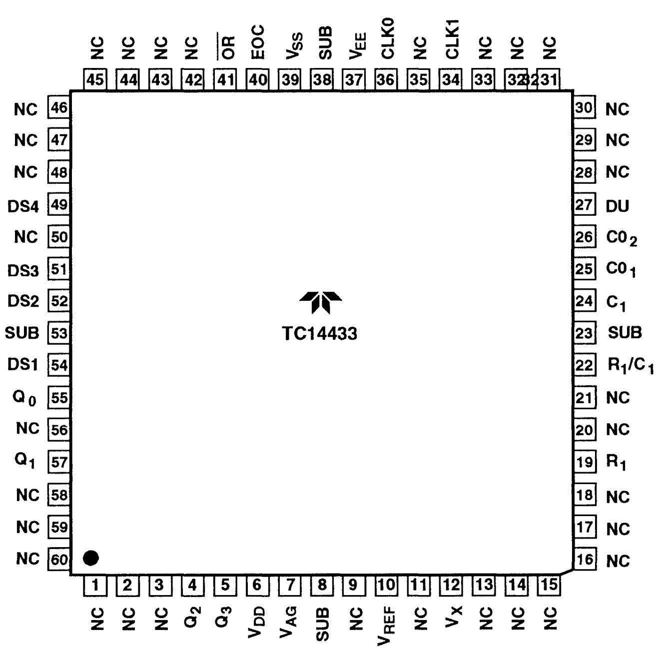


$$R_1 = \frac{V_X\,(max)}{C_1}\ 3\ \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X\,(max) - 0.5$$

$$T = 4000\ 3\ \frac{1}{f_{CLK}}$$

WHERE:
R_1 IS IN kΩ
V_{DD} IS THE VOLTAGE AT PIN 24 REFERENCED TO V_{AG}
V_X IS THE VOLTAGE AT PIN 3 REFERENCED TO V_{AG}
f_{CLK} IS THE CLOCK FREQUENCY AT PIN 10 IN kHz



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE.
THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

TC14433
TC14433A
TC14433B

PIN DESCRIPTIONS

Pin No. 60-Pin FP	Pin No. 24-Pin DIP	Symbol	Description
7	1	V_{AG}	This is the analog ground; it has a high input impedance — This pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
10	2	V_{REF}	Reference voltage — Full-scale output is equal to the voltage applied to V_{REF}. Therefore, full-scale voltage of 1.999V requires 2V reference and 199.9 mV full-scale requires a 200 mV reference. V_{REF} functions as system reset also. When switched to V_{EE}, the system is reset to the beginning of the conversion cycle.
12	3	V_X	The unknown input voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratiometric A/D conversion.
19	4	R_1	These pins are for external components used for the integration function in the dual slope conversion. Typical values are 0.1 µF (mylar) capacitor for C_1.
22	5	R_1/C_1	R_1 = 470 kΩ (resistor) for 2V full-scale.
24	6	C_1	R_1 = 27 kΩ (resistor) for 200 mV full-scale. Clock frequency of 66 kHz gives 250 ms conversion time. See equation below for calculation of integrator component values.
25	7	CO_1	These pins are used for connecting the offset correction capacitor. The recommended value
26	8	CO_2	is 0.1 µF.
27	9	DU	Display update input pin — When DU is connected to the EOC output every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU prior to the ramp-down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
34	10	CLK_1	Clock input pins — The TC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency.
36	11	CLK_0	A crystal or OC circuit may be inserted in lieu of a resistor for improved stability. CLK_1, the clock input, can be driven from an external clock source, which need only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300 kΩ resistor yields a clock frequency of about 66 kHz. (See typical characteristic curves; see Figure 9 for alternate circuits.)
37	12	V_{EE}	Negative power current — Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.
39	13	V_{SS}	Negative power supply for output circuitry — This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between the V_{DD} –3 volts and V_{EE}.
40	14	EOC	End of conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one-half the period of the system clock.
41	15	OR	Overrange pin — Normally this pin is set high. When V_X exceeds V_{REF} the OR pin is low.
49	16	DS_4	Digit select pins — The digit select output goes high when the respective digit is selected. The MSD (1/2 digit) turns on immediately after an EOC pulse.
51	17	DS_3	The remaining digits turn on in sequence from MSD to LSD.
52	18	DS_2	To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included.
54	19	DS_1	Clock frequency divided by 80 equals multiplex rate. For example, a system clock of 60 kHz gives a multiplex rate of 0.8 kHz.
5	20	Q_0	See Figure 12 for digit select timing diagram.
4	21	Q_1	BCD data output pins — Multiplexed BCD outputs contain three full digits of information during digit select DS_2, DS_3, DS_4.
57	22	Q_2	During DS_1, the 1/2 digit, overrange, underrange and polarity information is available.
55	23	Q_3	Refer to truth table.
6	24	V_{DD}	Positive power supply — This is the most positive power supply pin.

CIRCUIT DESCRIPTION

The TC14433 CMOS IC becomes a modified dual-slope A/D with a minimum of external components. This IC has the customary CMOS digital logic circuitry, as well as CMOS analog circuitry. It provides the user with digital functions (such as counters, latches, multiplexers) and analog functions (such as operational amplifiers and comparators) on a single chip.

Features of this system include auto-zero, high input impedances and auto-polarity. Low power consumption and a wide range of power supply voltages are also advantages of this CMOS device. The system's auto-zero function compensates for the offset voltage of the internal amplifiers and comparators. In this "ratiometric system," the output reading is the ratio of the unknown voltage to the reference voltage, where a ratio of 1 is equal to the maximum count of 1999. It takes approximately 16,000 clock periods to complete one conversion cycle. Each conversion cycle may be divided into 6 segments. Figure 7 shows the conversion cycle in 6 segments for both positive and negative inputs.

Segment 1 — The offset capacitor (C_0), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. However, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 — During this segment, the integrator output decreases to the comparator threshold voltage. At this time, a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the auto-zero process. The time for this segment is variable and less than 800 clock periods.

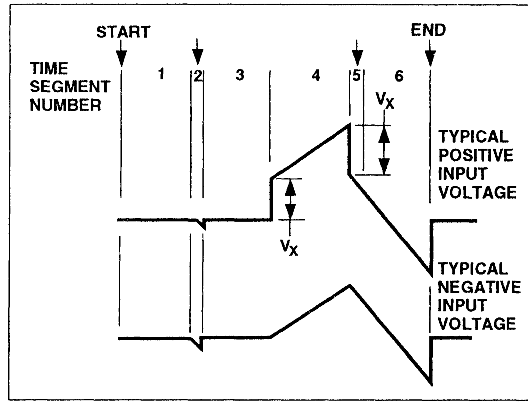


Figure 7. Integrator Waveforms at Pin 6

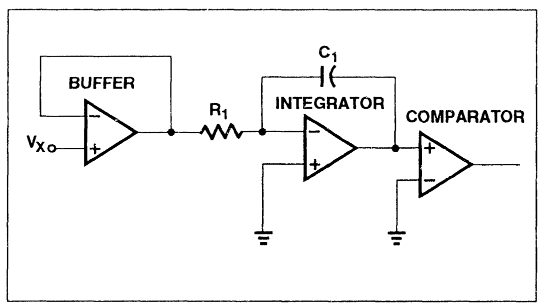


Figure 8. Equivalent Circuit Diagrams of the Analog Section During Segment 4 of the Timing Cycle

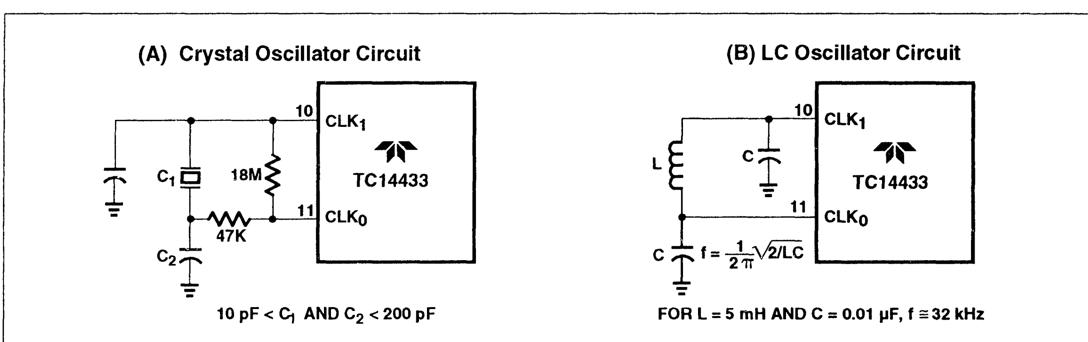


Figure 9. Alternate Oscillator Circuits

Segment 3 — This segment of the conversion cycle is the same as Segment 1.

Segment 4 — Segment 4 is an up-going ramp cycle with the unknown input voltage (V_x) as the input to the integrator. Figure 8 shows the equivalent configuration of the analog section of the TC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 — This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

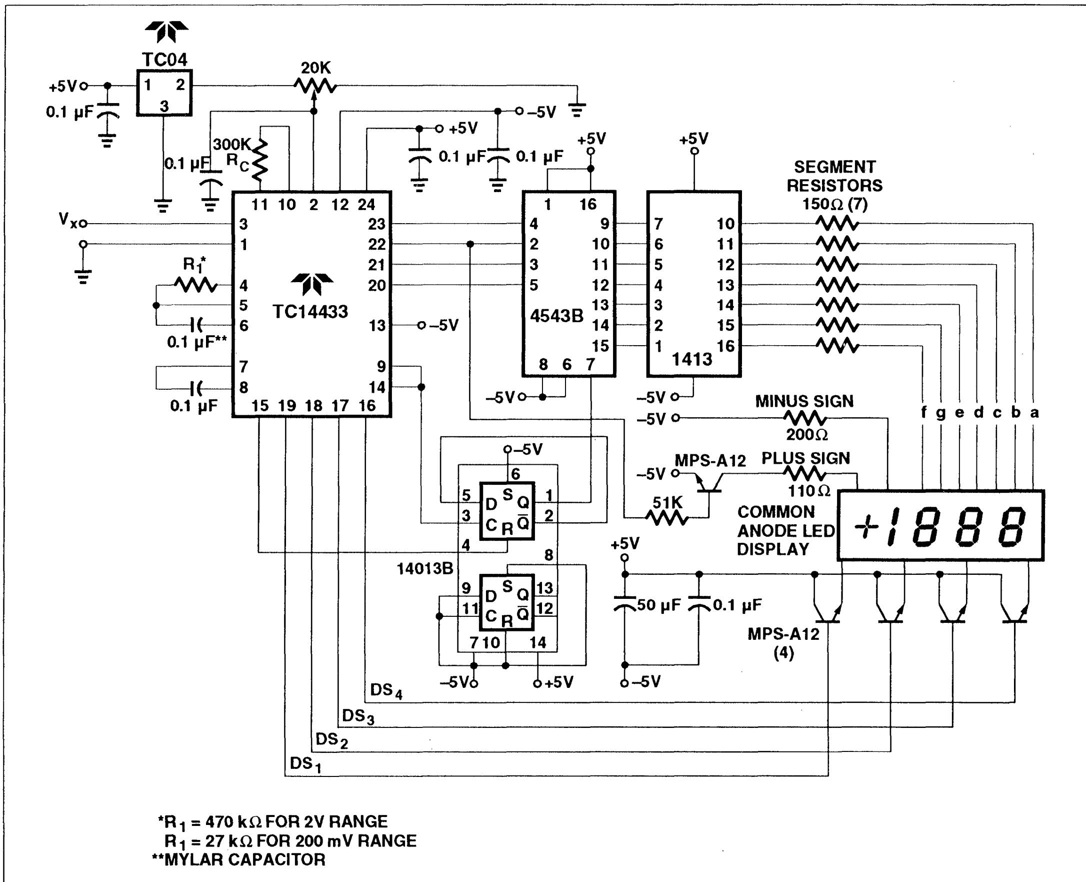


Figure 10. 3-1/2 Digit Voltmeter Common-Anode Displays, Flashing Overrange

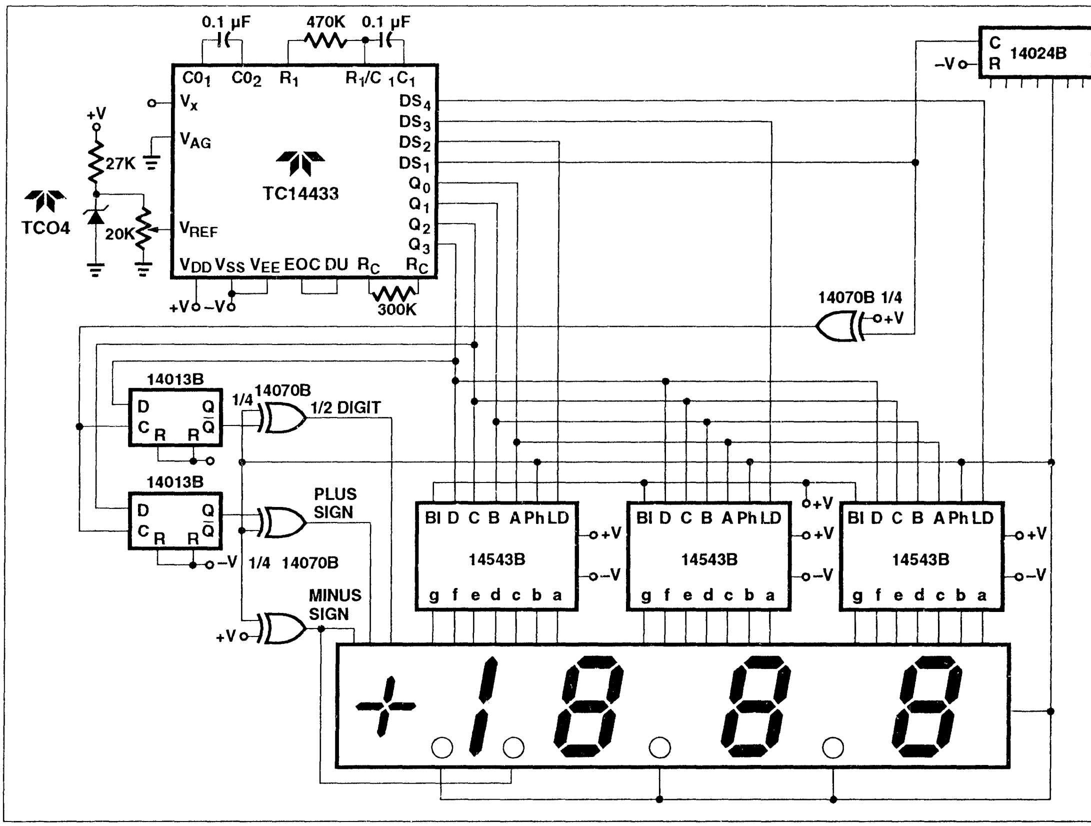


Figure 11. 3-1/2 Digit Voltmeter with LCD Display

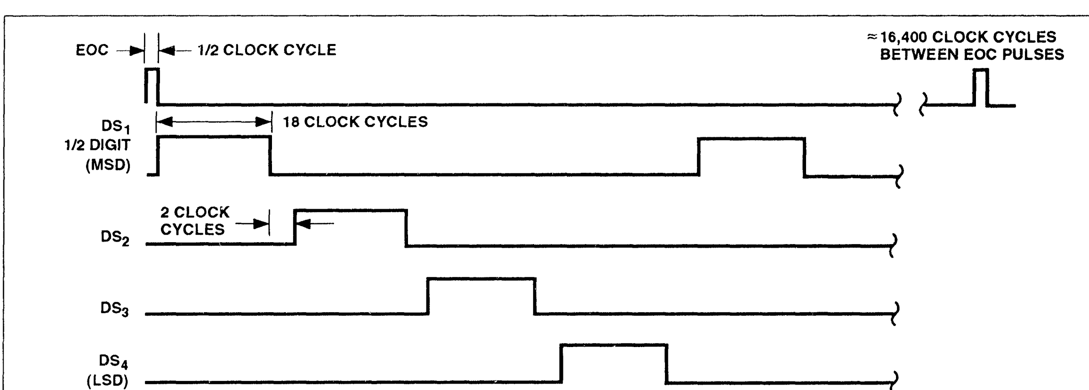


Figure 12. Digit Select Timing Diagram

TC14433
TC14433A
TC14433B

APPLICATIONS INFORMATION

Figure 10 is an example of a 3-1/2 digit voltmeter using the TC14433 with common-anode displays. This system requires a 2.5V reference. Full-scale may be adjusted to 1.999V or 199.9 mV. Input overrange is indicated by flashing a display. This display uses LEDs with common anode digit lines. Power supply for this system is shown as a dual ±5V supply; however, the TC14433 will operate over a wide voltage range (see recommended operating conditions, page 2).

The circuit in Figure 11 shows a 3-1/2 digit LCD voltmeter. The 14024B provides the low frequency square wave signal drive to the LCD backplane. Dual power supplies are shown here; however, one supply may be used when V_{SS} is connected to V_{EE}. In this case, V_{AG} must be at least 2.8V above V_{EE}.

When only segments b and c of the decoder are connected to the 1/2 digit of the display, 4, 0, 7 and 3 appear as 1.

The overrange indication (Q_3 = 0 and Q_0 = 1) occurs when the count is greater than 1999; e.g., 1.999V for a reference of 2V. The underrange indication, useful for auto-ranging circuits, occurs when the count is less than 180; e.g., 0.180V for a reference of 2V.

CAUTION

If the most significant digit is connected to a display other than a "1" only, such as a full digit display, segments other than b and c must be disconnected. The BCD to 7-segment decoder must blank on BCD inputs 1010 to 1111.

Figure 14 is an example of a 3-1/2 digit LED voltmeter with a minimum of external components (only 11 additional components). In this circuit, the 14511B provides the segment drive and the 75492 or 1413 provides sink for digit current. Display is blanked during the overrange condition.

TRUTH TABLE

Coded Condition of MSD	Q_3	Q_2	Q_1	Q_0	BCD to 7-Segment Decoding
+0	1	1	1	0	Blank
−0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
−0 UR	1	0	1	1	Blank
+1	0	1	0	0	4–1 Hook up
−1	0	0	0	0	0–1 only
+1 OR	0	1	1	1	7–1 segments
−0 OR	0	0	1	1	3–1 b and c to MSD

NOTES:

Q_3 — 1/2 digit, low for "1", high for "0"
Q_2 — Polarity: "1" = positive, "0" = negative
Q_0 — Out of range condition exists if Q_0 = 1. When used in conjunction with Q_3, the type of out of range condition is indicated; i.e., Q_3 = 0 → OR or Q_3 = 1 → UR.

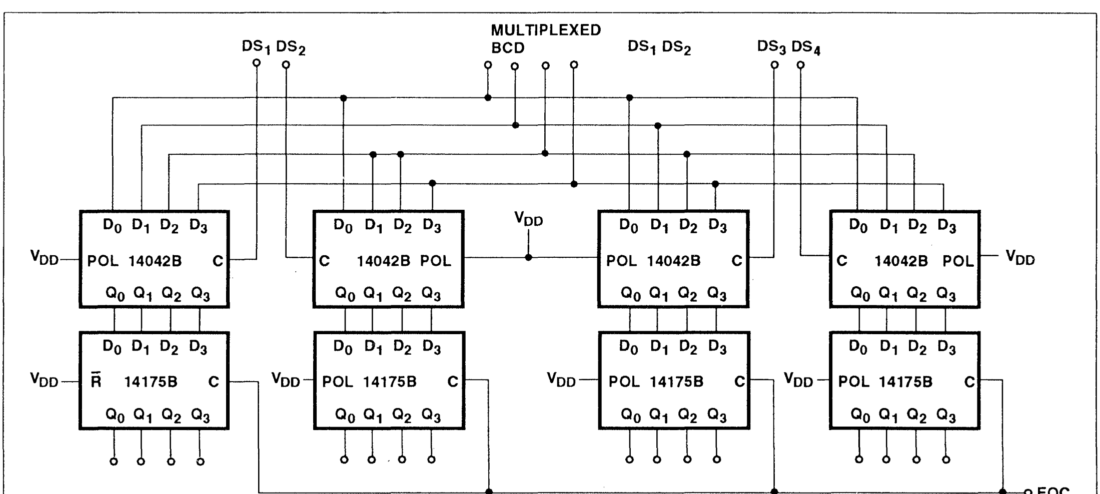
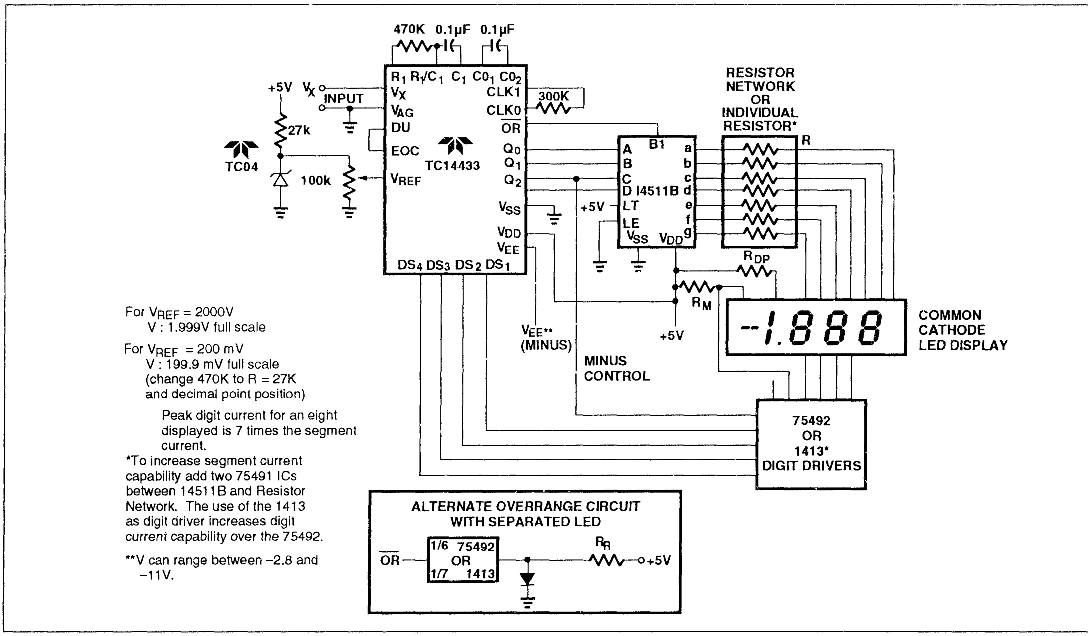


Figure 13. Demultiplexing for TC14433 BCD Data



For V_{REF} = 2000V
V : 1.999V full scale
For V_{REF} = 200 mV
V : 199.9 mV full scale
(change 470K to R = 27K and decimal point position)

Peak digit current for an eight displayed is 7 times the segment current.

*To increase segment current capability add two 75491 ICs between 14511B and Resistor Network. The use of the 1413 as digit driver increases digit current capability over the 75492.

**V can range between –2.8 and –11V.

Figure 14. 3-1/2 Digit Voltmeter with Low Component Count Using Common Cathode Displays

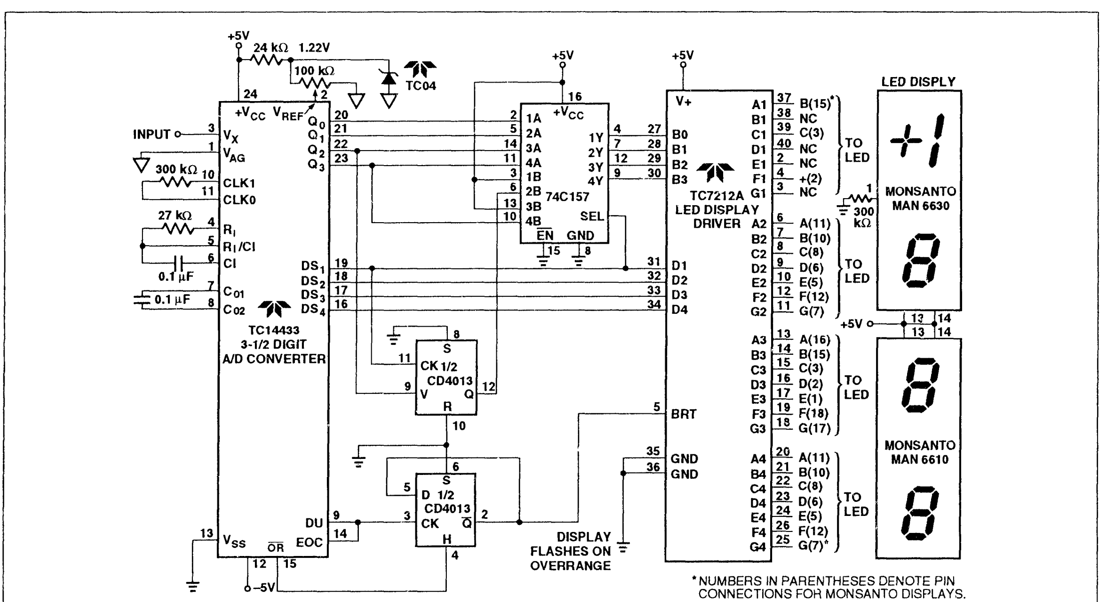


Figure 15. TC7212A Interface to TC14433 3-1/2 Digit ADC

NOTES

Section 2

Binary A/D Converters

INTEGRATING CONVERTER ANALOG PROCESSORS

FEATURES

- **Resolution .... Up to 16 Bits + Sign (TC500A)**
- **Differential Analog Input**
- **Differential Reference**
- **Low Linearity Error 0.003%**
- **Fast Zero-Crossing Comparator .... 4 µs**
- **Low Power Dissipation .... 10 mW**
- **Auto-Zero Cycle Eliminates Zero-Scale Error and Drift**
- **Zero Integrator Phase Speeds Recovery From Overrange Input Signals**
- **Automatic Internal Polarity Detection**
- **Low Input Current .... 15 pA Max**
- **Wide Analog Input Voltage .... ±4.2V**
- **Microprocessor Control of Dual-Slope ADC Conversion**

IMPROVED PERFORMANCE

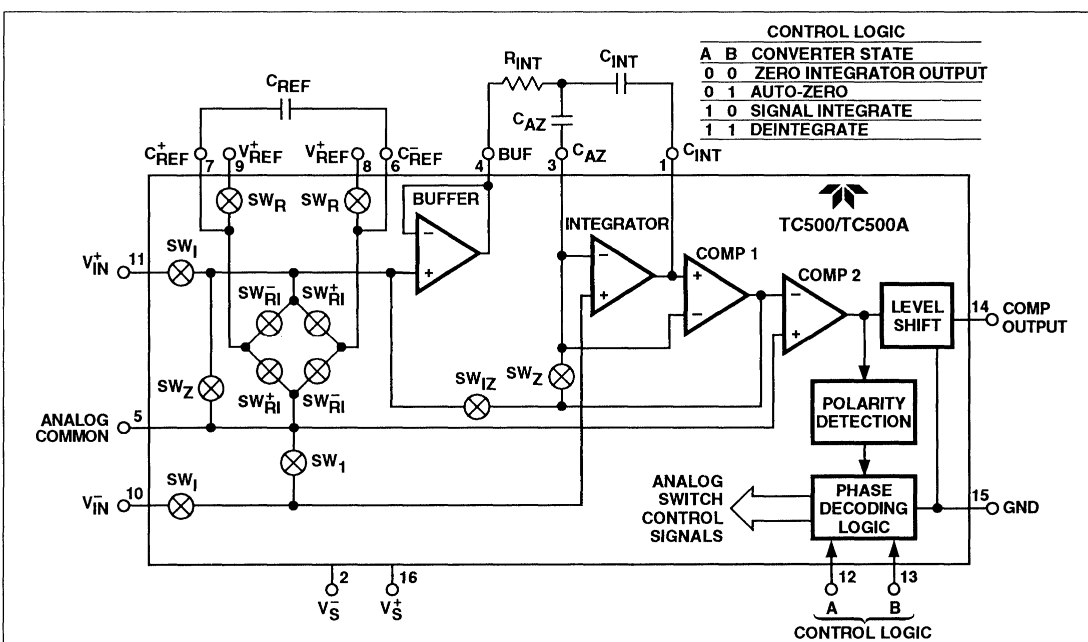
The TC500A is an improved version of the popular TC500. The improvements allow up to 16 bits of resolution (plus sign) or faster conversion times for lower resolution applications.

GENERAL DESCRIPTION

The CMOS TC500/TC500A contain all the analog circuits needed to construct an integrating analog-to-digital converter. The analog input buffer, integrator, analog switches, comparator and phase control logic are all on chip.

The dual-slope converter uses time to quantize the analog input signal. A microprocessor and software routine perform the digital function of "counting clocks" for the dual-slope integrating converter process. The user can control resolution and conversion speed through software. The TC500/TC500A analog building block can be used to construct a fast or high-resolution converter by modifying software routines.

FUNCTIONAL DIAGRAM



TC500
TC500A

A microprocessor controls the TC500/TC500A through the A and B logic input signals. Four phases are possible: auto-zero, signal integrate, reference integrate (deintegrate), and integrator zero output.

The TC500/TC500A comparator's output provides polarity and integrator zero-crossing information. The comparator output is always low when the integrator crosses zero during the deintegrate phase. This signals the end of a conversion to the processor.

A precision, dual-slope integrating converter with automatic zero-scale offset voltage and drift correction requires only a reference, three capacitors, a resistor and a controller. The TC500/TC500A contain the analog circuits needed to construct a dual-slope integrating converter with an auto-zero phase. A zero-integrator output phase can be selected to eliminate errors caused by out-of-range input signals. The zero-integrator phase greatly improves recovery after an overrange conversion.

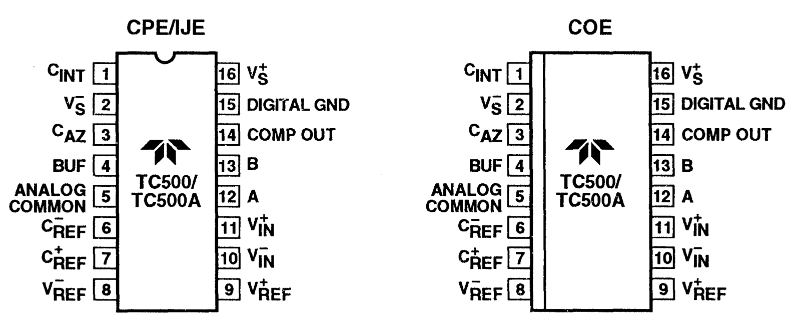
The CMOS TC500/TC500A operate from ±5V supplies. Power dissipation is only 10 mW. Leakage currents at the differential inputs are a low 10 pA. The TC500/TC500A differential reference inputs allow easy ratiometric measurements.

Although the TC500A is pin-for-pin compatible with the TC500, some programming constraints are imposed. (See "Integrator Output Zero.")

ORDERING INFORMATION

Part No.	Package	Temperature Range	System Resolution
TC500ACPE	16-Pin Plastic DIP	0°C to +70°C	16-Bit (30 ppm)
TC500AIJE	16-Pin CerDIP	–25°C to +85°C	16-Bit (30 ppm)
TC500ACOE	16-Pin SO	0°C to +70°C	16-Bit (30 ppm)
TC500CPE	16-Pin Plastic DIP	0°C to +70°C	4-1/2 Digits (50 ppm)
TC500IJE	16-Pin CerDIP	–25°C to +85°C	4-1/2 Digits (50 ppm)
TC500COE	16-Pin SO	0°C to +70°C	4-1/2 Digits (50 ppm)

PIN CONFIGURATIONS



INTEGRATING CONVERTER ANALOG PROCESSORS

TC500 TC500A

ABSOLUTE MAXIMUM RATINGS

Supply (V_S^+ to V_S^-) .... +18V
Positive Supply Voltage (V_S^+ to GND) .... +12V
Negative Supply Voltage (V_S^- to GND) .... –12V
Analog Input Voltage (V_{IN}^+ or V_{IN}^-) .... V_S^+ to V_S^-
Logic Input Voltage .... V_S^+ +0.3V to GND –0.3V
Package Power Dissipation 0.5W
Ambient Operating Temperature Range
  Plastic Package (C) .... 0°C to +70°C
  CerDIP Package (I) .... –25°C to +85°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, V_S = ±5V, unless otherwise specified. C_{AZ} = C_{REF} = 0.1 µF.

Symbol	Parameter	Test Conditions	TC500 Min	TC500 Typ	TC500 Max	TC500A Min	TC500A Typ	TC500A Max	Unit
Analog									
	Resolution	Note 1	—	—	50	—	—	30	ppm
ZSE	Zero-Scale Error	Note 1	—	—	0.005	—	—	0.003	%
ENL	End Point Linearity	Note 1	—	0.005	0.01	—	0.005	0.01	%
NL	Best Case Straight Line Linearity	Notes 1 and 2	—	—	0.005	—	—	0.003	%
DNL	Differential Nonlinearity		—	—	0.0025	—	—	0.0025	%
TC_{ZS}	Zero-Scale Temperature Coefficient	Over Operating Temperature Range	—	1	2	—	1	2	µV/°C
SYE	Full-Scale Symmetry Error (Roll-Over Error)		—	—	0.01	—	—	0.006	%
	Ratiometric Reading	$V_{IN} = V_{REF}$ = 1V	—	—	0.035	—	—	0.035	%
FS_{TC}	Full-Scale Temperature Coefficient	Over Operating Temperature Range External Reference TC = 0 ppm/°C	—	—	10	—	—	10	ppm/°C
I_{IN}	Input Current	V_{IN} = 0V	—	6	15	—	6	15	pA
CMRR	Common-Mode Rejection Ratio	$-1V \leq V_{CM} \leq 1V$	—	80	—	—	80	—	dB
V_{CMR}	Common-Mode Voltage Range	V_S = ±5V	V_S^- +1.5	—	V_S^+ –1.5	V_S^- +1.5	—	V_S^+ –1.5	V
	Integrator Output Swing	V_S = ±5V	—	—	±4.1	—	—	±4.1	V
	Analog Input Signal Range		V_S^- +0.8	—	V_S^+ –0.8	V_S^- +0.8	—	V_S^+ –0.8	V
e_N	Noise	V_{IN} = 0V	—	30	—	—	30	—	μV_{P-P}
Digital									
	Reference Input Signal Range		V_S^- +1	—	V_S^+ –1	V_S^- +1	—	V_S^+ –1	V
V_{OH}	Comparator Logic 1, Output High	I_{SOURCE} = 800 µA	4	—	—	4	—	—	V
V_{OL}	Comparator Logic 0, Output Low	I_{SINK} = 4 mA	—	—	0.4	—	—	0.4	V
V_{IH}	Logic 1, Input High Voltage		3.5	—	—	3.5	—	—	V
V_{IL}	Logic 0, Input Low Voltage		—	—	1	—	—	1	V
I_L	Logic Input Current	Logic 1 or 0	—	0.05	—	—	0.05	—	µA
t_D	Comparator Delay		—	4	—	—	4	—	µs

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	TC500 Min	TC500 Typ	TC500 Max	TC500A Min	TC500A Typ	TC500A Max	Unit
Power									
I_S	Supply Current	$V_S = \pm 5V$, A = 1, B = 1	—	1	1.5	—	1	1.5	mA
P_D	Power Dissipation	$V_S = \pm 5V$	—	—	15	—	—	15	mW
V_S^+	Positive Supply Operating Voltage Range		4	—	10	4	—	10	V
V_S^-	Negative Supply Operating Voltage Range		–3	—	–8	–3	—	–8	V
$V_S^+ - V_S^-$	Supply Operating Voltage Range		7	—	15	7	—	15	V

NOTES: 1. Integrate time ≥200 ms, auto-zero time ≥100 ms, V_{INT} (peak) ≈ 4V.
2. End point linearity at ±1/4, ±1/2, ±3/4 FS after full-scale adjustment.

OPERATIONAL THEORY

The TC500 and TC500A are dual-slope, integrating analog processors which are used with a microprocessor to generate analog-to-digital conversions of up to 16 bits of resolution. Although the TC500 and TC500A are virtually the same, the TC500A is recommended for applications requiring more than 14 bits of resolution.

The TC500 and TC500A incorporate a system zero phase and integrator output voltage zero phase, in addition to the normal two-phase, dual-slope measurement cycle. Reduced system errors, fewer calibration steps, and shorter overrange recovery time result.

The TC500 and TC500A measurement cycle can use all four phases, if desired.

(1) Auto zero

(2) Analog input signal integration

(3) Reference voltage integration (deintegrate)

(4) Integrator output zero

Internal analog gate status is shown in Table I for each phase (see the functional diagram).

Auto-Zero Phase

During this phase, errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

Analog Input Signal Integration Phase

The TC500/TC500A integrate the differential voltage between the (+) and (–) inputs. The differential voltage must be within the device's common-mode range.

The input signal polarity is normally checked via software at the end of this phase.

Table I. Internal Analog Gate Status

Conversion Phase	SW_I	SW_{RI}^+	SW_{RI}^-	SW_Z	SW_R	SW_1	SW_{IZ}
Auto-Zero (A=0, B=1)				Closed	Closed	Closed	
Input Signal Integration (A=1, B=0)	Closed						
Reference Voltage Deintegration (A=1, B=1)		Closed*				Closed	
Integrator Output Zero (A=0, B=0)					Closed	Closed	Closed

*Assumes a positive polarity input signal. SW_{RI}^- would be closed for a negative input signal.

Reference Voltage Deintegration Phase

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero.

Integrator Output Zero Phase

This phase guarantees the integrator output is at 0V when the system zero phase is entered and that the true system offset voltages are compensated. This phase is used at the end of the reference voltage deintegration (DEINT) phase and SHOULD be used for all TC500/TC500A applications. This phase MUST be used for resolutions of more than 14 bits. If this phase is not used, the value of the auto-zero capacitor (C_{AZ}) must be about 23 the value of the integration capacitor (C_{INT}) to reduce the effects of charge-sharing. The integrator output zero phase should be programmed to operate until the output of the comparator returns "high" (1) or for fixed time of about 2 ms.

ANALOG SECTION

Differential Inputs (V_{IN}^+ [Pin 11], V_{IN}^- [Pin 10])

The TC500/TC500A operate with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.8V below positive supply to 0.8V above negative supply. Within this common-mode voltage range, a common-mode rejection is typically 80 dB. Full accuracy is maintained, however, when the inputs are no less than 1.5V from either supply.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large, positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications, the integrator swing can be reduced. The integrator output can swing within 0.9V of either supply without loss of linearity.

Analog Common (Pin 5)

Analog common is used as V_{IN} return during system-zero and reference deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, V_{IN}^- will be set at a fixed known voltage (i.e., power supply common). A common-mode voltage will exist when V_{IN}^- is not connected to analog common.

Differential Reference
(V_{REF}^+ [Pin 9], V_{REF}^- [Pin 8])

The reference voltage can be generated anywhere within 1V of the power supply voltage of the converter. Roll-over error is caused by the reference capacitor losing or gaining charge due to stray capacitance on its nodes. The difference in reference for (+) or (–) input voltages will cause a roll-over error. This error can be minimized by using a large reference capacitor in comparison to the stray capacitance.

Phase Control Inputs (A [Pin 12], B [Pin 13])

The A, B unlatched logic inputs select the TC500/TC500A operating phase. The A, B inputs are normally driven by a microprocessor I/O port or peripheral I/O chip.

Comparator Output

By monitoring the comparator output during the fixed-signal integrate time, the input signal polarity can be determined by the microprocessor controlling the conversion. The comparator output is high for positive signals and low for negative signals during the signal-integrate phase.

During the reference deintegrate phase, the comparator output will make a high-to-low transition as the integrator output ramp crosses zero. The transition is used to signal the processor that the conversion is complete.

The internal comparator delay is 4 μs, typically.

Figure 1 shows the comparator output for large positive and negative signal inputs. For signal inputs at or near zero volts, however, the integrator swing is nonexistent. If common-mode noise is present, the comparator can switch several times during the signal-integrate period. To ensure that the polarity reading is correct, the comparator output should be read and stored at the end of signal integrate.

A "low" (0) on the TC500/TC500A comparator, during the deintegrate phase, signals the processor that the conversion is complete.

The comparator output is undefined during the auto-zero and the integrator output zero phases.

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC500 is an integrating analog-to-digital converter building block. An understanding of the dual-slope conversion technique will aid in following the detailed TC500A operation theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

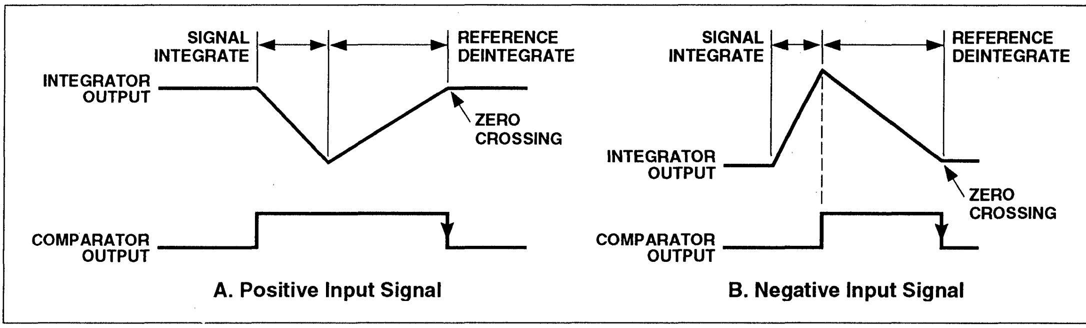


Figure 1. Comparator Output

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The TC500/TC500A automatically switch in the proper polarity reference signal. The reference integration time is directly proportional to the input signal (Figure 2).

In a simple dual-slope converter, a complete conversion requires the integrator output to "ramp-up" and "ramp-down." The TC500/TC500A comparator zero-crossing signals the processor to indicate the deintegrate cycle is complete.

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{R_{INT}\,C_{INT}} \int_0^{t_{INT}} V_{IN}(t)\,dt = \frac{V_{REF}\,t_{DEINT}}{R_{INT}\,C_{INT}}$$

where:

V_{REF} = Reference voltage
t_{INT} = Signal integration time (fixed)
t_{DEINT} = reference voltage integration time (variable)

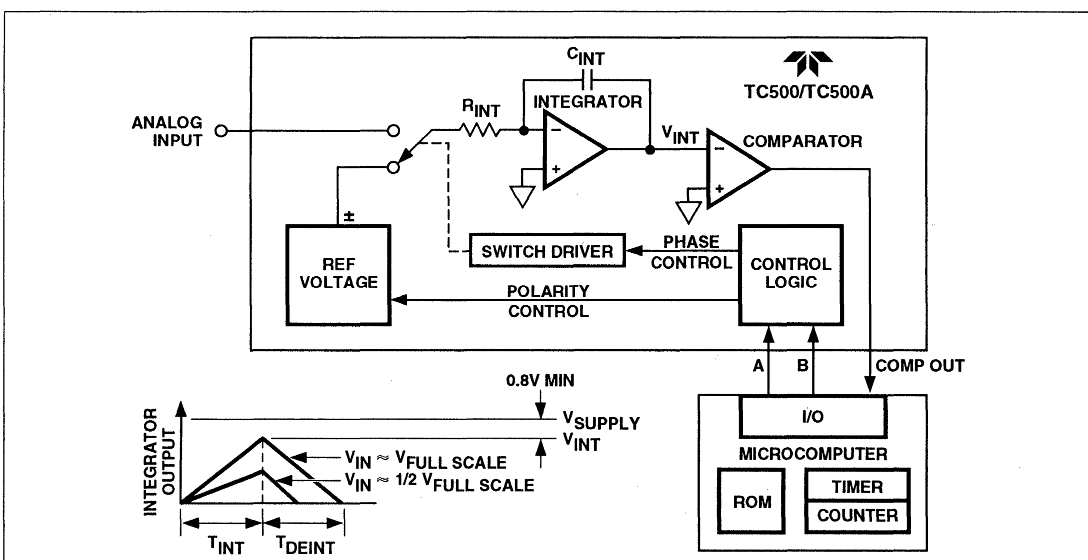


Figure 2. Basic Dual-Slope Converter

For a constant V_{IN}:

$$V_{IN} = V_{REF} \frac{t_{DEINT}}{t_{INT}}$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle.

An inherent benefit is noise immunity. Input noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague succesive approximation converters in high-noise environments.

Integrating converters provide noise rejection automatically with at least a 20-dB/decade attenuation rate. Interference signals with frequencies at integral multiples of the integration period are, theoretically, completely removed. This intuitively makes sense, since the average value of a sine wave of frequency (1/t) averaged over a period (t) is zero.

Integrating converters often establish the integration period to reject 50/60 Hz line frequency interference signals. The ability to reject such signals is shown by a normal mode rejection plot (Figure 3). Normal mode rejection is practically set to 50 to 65 dB, since the line frequency can deviate by a few tenths of a percent (Figure 4).

Criteria for C_{AZ} and C_{REF}

$$C_{AZ} \approx C_{REF} \approx \frac{2^N\, t_{INT}\, (V_{INT} + V_{REF})\, I_{LEAKAGE}}{V_{INT}\, V_{REF}}$$

where:

N = resolution (bits)
$I_{LEAKAGE} \approx 15$ pA
V_{INT} (see Figure 2)

This equation is for reference only. Use 0.1 µF capacitor for all applications that have 8 or more conversions per second. Use a 0.22 µF capacitor for 3 to 7 conversions per second, and a 0.47 µF capacitor for 2 or less conversions per second.

COMPONENT VALUE SELECTION

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 20-µA drive current with minimal linearity error. R_{INT} is easily calculated for a 20-µA full-scale current:

$$R_{INT}\,(M\Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{20} \quad \pm 20\%$$

For loop stability, R_{INT} should be $\geq$50 kΩ.

Reference Capacitor (C_{REF})

A 0.1-µF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitors (such as polypropylene) are required.

Auto-Zero Capacitor (C_{AZ})

A 0.1-µF polypropylene capacitor is suggested.

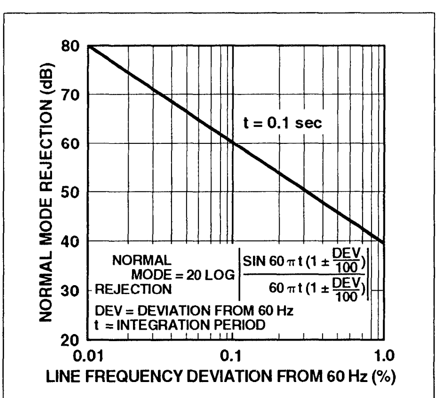


Figure 3. Normal Mode Rejection vs Input Frequency

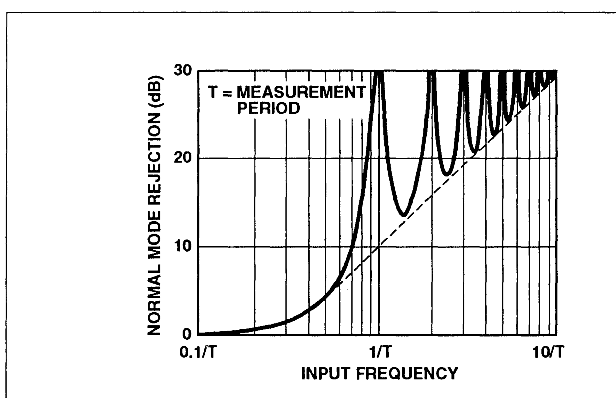


Figure 4. Intregrating Converter Normal Mode Rejection vs 60 Hz Line Frequency Variations

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.8V of V_S^+ or V_S^- without saturating.

Using the suggested 20-µA full-scale buffer output current, the integrating capacitor is easily calculated:

$$C_{INT} = \frac{(t_{INT})\,(V_{FS})}{(V_{INT})\,(R_{INT})} \approx 5\ t_{INT}\ (\mu F)$$

where:

t_{INT} = Integration period
V_{FS} = Full-scale input voltage
V_{INT} = Integrator output voltage swing

A very important integrating capacitor characteristic is dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polyester and polycarbonate capacitors may also be used in less critical applications.

The threshold noise (N_{TH}) is the algebraic sum of the integrator noise and the comparator noise. This value is typically about 30 µV. The graph shows how the value of the reference voltage can influence the results of the final count.

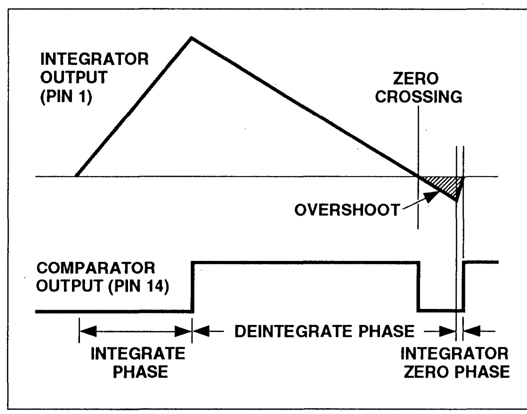
Errors caused by the low-frequency buffer noise may be reduced by increased integration times.

Signal-to-Noise Ratio

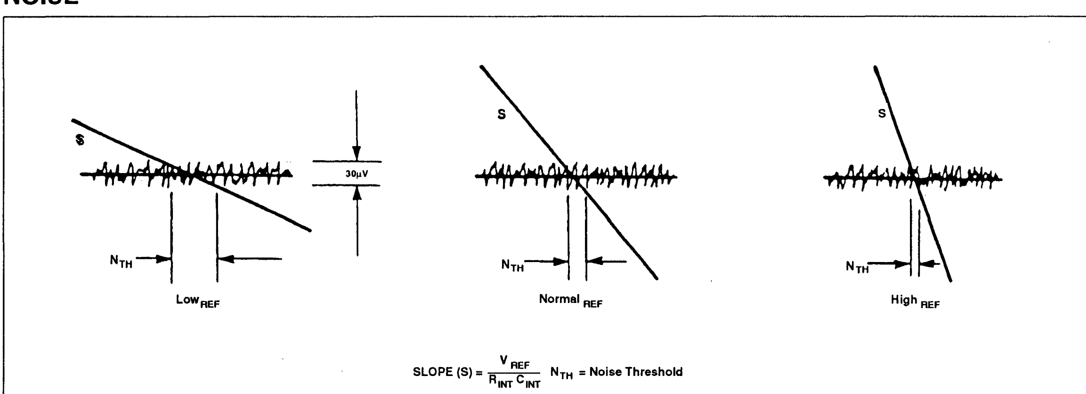
$$S/N\ (dB) = 20\ \text{Log}\left(\frac{V_{IN}}{30\ \mu V} \bullet \frac{t_{INT}}{R_{INT} \bullet C_{INT}}\right)$$

The maximum performance of the TC500/TC500A require that overshoot at the end of the deintegration phase be minimized. Also, the integrator zero phase may be terminated as soon as the comparator output returns to "high" (1).

OVERSHOOT

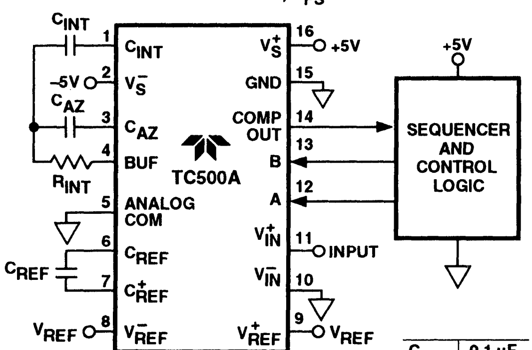


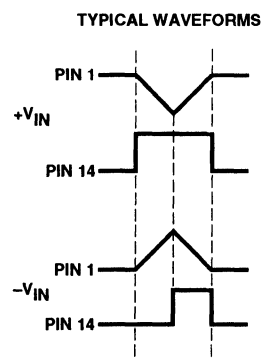
NOISE



TC500A DESIGN EXAMPLE (See "Component Selection Example")

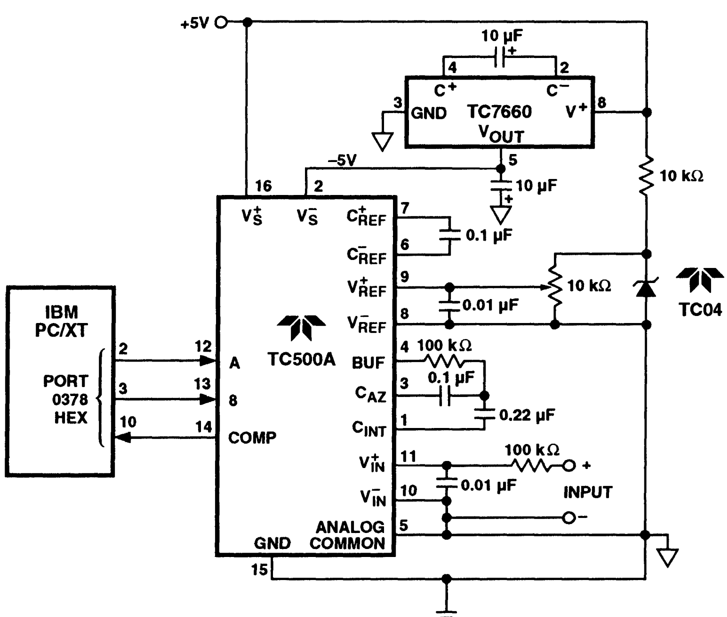
TIMING CONDITIONS: A) AZ PLUS ZI .... 10,000 CLOCK PERIODS (40 ms)
B) INT .... 10,000 CLOCK PERIODS (40 ms)
C) DEINT .... V_{IN} (V) 10,000 CLOCK PERIODS (14 bits)
D) CLOCK PERIOD .... 4 µs
E) V_{FS} .... ±2.5V





C_{INT}	0.1 µF
R_{INT}	250 kΩ
C_{AZ}	0.1 µF
C_{REF}	0.1 µF

TC500A TO IBM PC/XT PRINTER PORT



Interrupt Operation

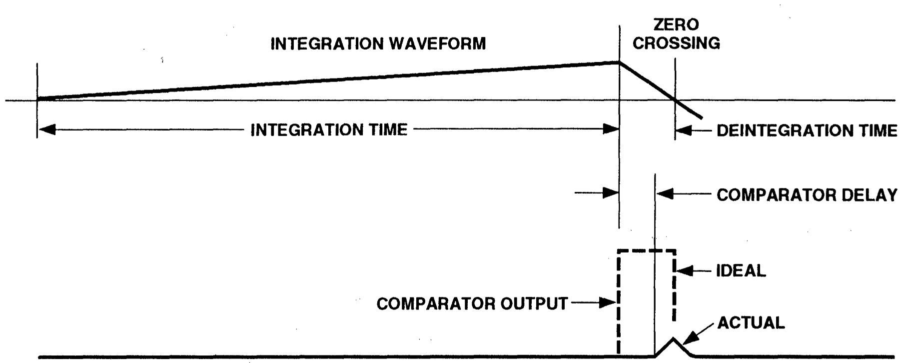
The comparator output stays low during the Integration phase (A=1, B=0) whenever the input polarity is negative. In those cases where the input polarity is negative AND very near zero, the zero-crossing occurs before the comparator has had a chance to go positive. Thus, no negative-edge will be generated and the microprocessor will not be interrupted.

With a negative input voltage very near zero, the output of the comparator does not have enough time to get full positive. This anomaly is caused by the comparator delay and rise time limitations.

One solution to overcome this condition is to have the microprocessor monitor the comparator output. It can then end the deintegration phase as soon as it sees a zero.

Another solution is to have the microprocessor enable the interrupt and look at the comparator output. If the output is high, the interrupt will be properly triggered. If the output is low, end the deintegration phase and disable the interrupt.

Either solution will produce reliable low voltage conversions.



Rate of Conversion

The conversion times for the TC500/TC500A are a function of many variables and constants. The dominate component is C_{INT}:

$$\text{Conversion Time (sec)} = 0.4 \times C_{INT}\,(\mu F) \times (2 + (V_{IN}/V_{REF}))$$

The assumptions for this equation are suggested but not strictly required. They are:

Auto-zero time (T_{AZ}) = Integration time (T_{NT})
Peak integration voltage (V_{INT}) = 4V
Maximum buffer current ($V_{IN(MAX)}/R_{INT}$) = 20 μA

Component Selection Example

Known:
1) Supply voltage for TC500A (V_{SUP})
2) Maximum input voltage ($V_{IN(MAX)}$)
3) Integration time (T_{INT})
4) Output resolution (bits) (N)
5) Clock period (t_{CLOCK})

Assume:
$V_{SUP} = \pm5V$ — $V_{SUP} = |V_{SUP}|$
$V_{IN(MAX)} = \pm2.5V$ — $V_{IN(MAX)} = |V_{IN(MAX)}|$
$T_{INT} = 40$ ms
N = 14 bits
$t_{CLOCK} = 4\ \mu s$

Step 1: Calculate R_{INT} $\quad R_{INT} = \dfrac{V_{IN(MAX)}}{I_{BUF(MAX)}}$

Where $I_{BUF(MAX)} \approx 20\ \mu A$

$$R_{INT} = \frac{2.5V}{20\ \mu A} = 125K$$

Use 130K

$$\therefore I_{BUF} = \frac{2.5V}{130K} = 19.2\ \mu A$$

Step 2: Calculate C_{INT} $\quad C_{INT} = \dfrac{T_{INT}\ I_{BUF(MAX)}}{V_{INT}}$

Where $V_{INT} = V_{SUP} - 1V = 4V$

$$C_{INT} = \frac{40\text{ ms } 19.2\ \mu A}{4V} = 0.192\ \mu F$$

Use 0.2 µF

Step 3: Calculate V_{REF} $\quad V_{REF} = \dfrac{V_{INT}\ C_{INT}\ R_{INT}}{T_{DEINT}}$

Where $T_{DEINT} = 2^N\ t_{CLOCK}$

$$V_{REF} = \frac{4V \bullet 0.2\ \mu F \bullet 130K}{2^N\ t_{CLOCK}} = 1.587...V$$

Step 4: Calculate integrate count $\quad K_{INT} = \dfrac{T_{INT}}{t_{CLOCK}}$

Where R_{INT} $\dfrac{40\text{ ms}}{4\ \mu s} = 10{,}000$ Counts

Results: $K_{DEINT} = V_{IN}\ \dfrac{K_{INT}}{V_{REF}} = V_{IN}\ \dfrac{10{,}000}{1.587...V}$

Where K_{DEINT} = Number of clock periods during T_{DEINT}

Normalization

The reference voltage can be adjusted to scale the deintegrate count to be directly equivalent to the input voltage.

Since: $\dfrac{K_{INT}}{V_{REF}}$ = Counts/Volt

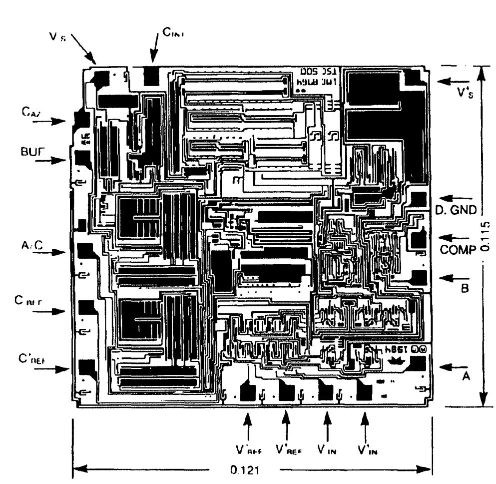
If: V_{REF} is adjusted such that

$$V_{REF} = \frac{10000\text{ Counts}}{10000\text{ Counts/Volt}} = \frac{K_{INT}}{10000\text{ Counts/Volt}} = 1V$$

Then: $K_{DEINT} = \dfrac{V_{IN}}{100\ \mu V}$ and $N \approx 14.61$ Bits

e.g., If K_{DEINT} = 18357 Counts, then V_{IN} = 1.8357V

BONDING DIAGRAM



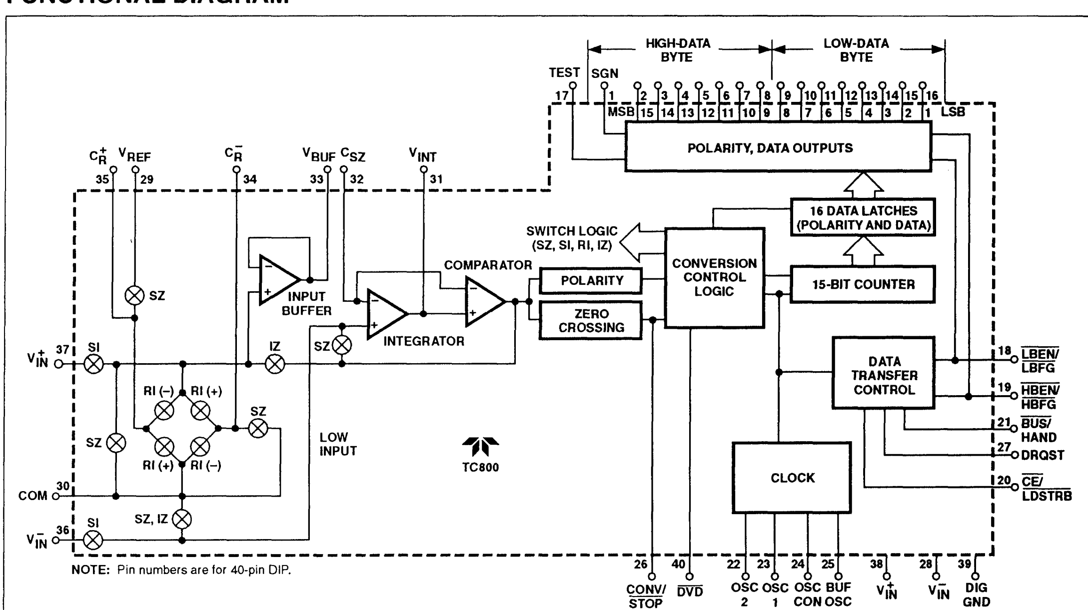
NOTES

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

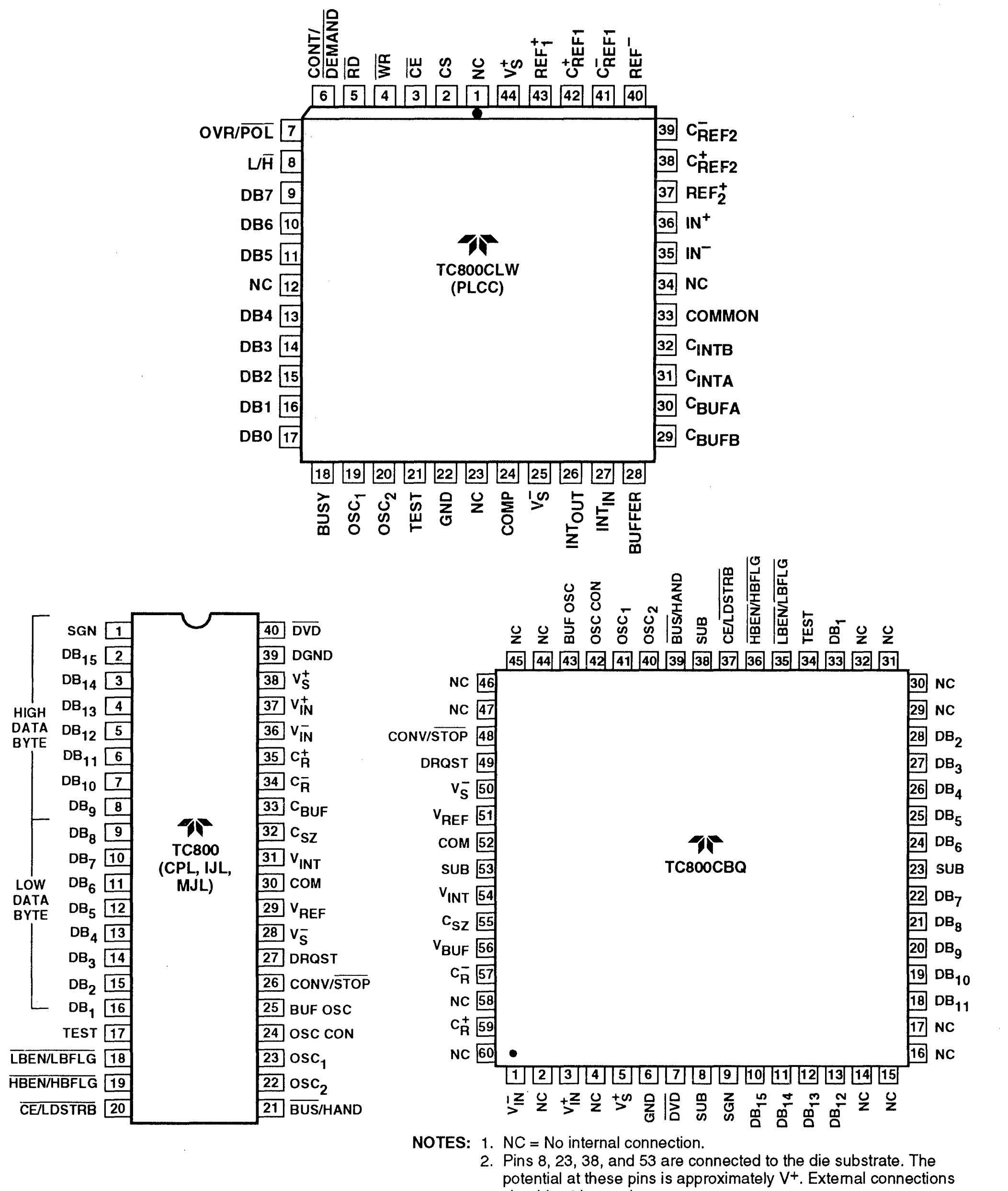
FEATURES

- 15-Bit Resolution Plus Sign Bit
- Dynamic Range .... 96 dB
- Integrating Dual-Slope Converter
  - Monotonic
  - Eliminates 50/60 Hz 'Line' Interference
  - High-Noise Immunity
  - Auto-Zero Cycle Eliminates Trimming
  - Incorporates Integrator Zero Cycle for Fast Overload Recovery
- Three-State Data Bit/Sign Outputs
  - 8-Bit or 16-Bit Parallel Data Transfer to µProcessor Bus
- UART Control Signals
  - Serial Data Transmission
  - 'Handshake' Data Transfer
  - Distributed Control Systems
  - Fiber-Optic Transmission Systems
- Easy Conversion Cycle Monitoring and Control
  - Data Valid Output Signal
  - Continuous or Convert-on-Command Operation
- High-Impedance Differential Input
  - Maximum Input Current .... 15 pA
- Low Input Noise .... 15 μV_{P-P}
- On-Chip Crystal Oscillator for 2.5 Conversions/Sec
  - f_{XTAL} = 2.4576 MHz
  - Integration Period (Rejects 50, 60, 400 Hz Interference Signals) .... 100 ms
- Supply Operation .... ±5V
  - Low Power Dissipation .... 20 mW
- Static-Discharge Protected Inputs
- Available in 60-Pin Flat Package

FUNCTIONAL DIAGRAM



PIN CONFIGURATIONS



NOTES: 1. NC = No internal connection.
2. Pins 8, 23, 38, and 53 are connected to the die substrate. The potential at these pins is approximately V+. External connections should not be made.

15-BIT PLUS SIGN, INTEGRATING ANALOG-TO-DIGITAL CONVERTER

GENERAL DESCRIPTION

The TC800 is a 15-bit plus sign, integrating analog-to-digital converter (ADC). It improves conventional two-cycle, dual-slope conversion by incorporating system zero and integrator output zero phases. Offset error sources are automatically zeroed and overrange recovery time is reduced. The integrating conversion technique is immune to noise spikes that introduce conversion errors in successive approximation converters.

The externally-adjustable clock allows integration periods which are integral multiples of 50 Hz or 60 Hz, for maximum power-line noise rejection. Using the 2.4576 MHz crystal oscillator mode (2.5 conversions/sec), 50 Hz, 60 Hz, and 400 Hz signals are rejected.

Microprocessor interface signals support 1-byte (16-bit) or 2-byte (8-bit) parallel data transfers. A 'handshake' operating mode supports serial data transmission via a UART. A serial count output is derived by gating the clock signal with data valid ($\overline{DVD}$). The count output pulses may be used in serial fiber-optic transmission systems.

The high-impedance differential inputs, 5 pA input leakage current, 16-bit dynamic range, and interface control signals make the high-resolution TC800 the ideal analog-to-digital converter for process control, data logging and 'intelligent' measurement systems.

See TC850 data sheet for applications requiring fast conversion rates.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC800CPL	40-Pin Plastic DIP	0°C to +70°C
TC800IJL	40-Pin CerDIP	–25°C to +85°C
TC800MJL	40-Pin CerDIP	–55°C to +125°C
TC800CLW	44-Pin Plastic Leaded Chip Carrier	0°C to +70°C
TC800CBQ	60-Pin Plastic Flat (Formed Leads)	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_S^+ to GND) .... +6.2V
Negative Supply Voltage (V_S^- to GND) .... –9V
Analog Input Voltage (V_{IN}^+ or V_{IN}^-) .... V_S^+ to V_S^-
Voltage Reference Input (V_{REF}) .... V_S^+ to V_S^-
Logic Input Voltage .... V_S^+ +0.3V to GND –0.3V
Package Power Dissipation
  CerDIP .... 1W @ +85°C
  Plastic Packages .... 0.5W @ +70°C
Ambient Operating Temperature Range
  Plastic DIP (CPL, CBQ) .... 0°C to +70°C
  PLCC (CLW) .... 0°C to +70°C
  CerDIP (IJL) .... –25°C to +85°C
  (MJL) .... –55°C to +125°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$, Conversion Rate = 2.5 Conversion/sec, Crystal Frequency = 2.4576 MHz, $T_A = +25°C$, Full-Scale Voltage = 3.2768V (Notes 1 and 3).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog Input						
Zero-Scale Error		$V_{IN} = 0V$	—	—	±0.5	LSB
NL	Nonlinearity	Best Straight Line — Full Scale ≤ V_{IN} ≤ +Full Scale	—	1.3	2	LSB
		End Point — Full Scale≤ V_{IN} ≤ +Full Scale	—	2.8	—	LSB
DNL	Differential Nonlinearity		—	—	±0.5	LSB
I_{IN}	Input Current	$V_{IN} = 0V$, $T_A = +25°C$	—	5	15	pA
		0°C ≤ T_A ≤ +70°C	—	25	125	pA
		–25°C ≤ T_A ≤ +85°C	—	70	175	pA
		–55°C ≤ T_A ≤ +125°C	—	2.5	7.5	nA
V_{CMR}	Common-Mode Input Range	Over Operating Temperature Range	V_S^-+1.5	—	V_S^+–1	V
CMRR	Common-Mode Rejection Ratio	$V_{IN} = 0V$, $V_{CM} = \pm 1V$	—	80	—	μV/V
	Full-Scale Gain Temperature Coefficient	External Ref Temperature Coefficient = 0 ppm/°C 0°C ≤ T_A ≤ +70°C	—	1.5	5	ppm/°C
	Zero-Scale Error Temperature Coefficient	$V_{IN} = 0V$ 0°C ≤ T_A ≤ +70°C	—	0.8	2	μV/°C
	Full-Scale Magnitude Symmetry Error	$V_{IN} = 3.27V$	—	—	2	LSB
e_N	Input Noise	Not Exceeded 95% of Time	—	15	—	μV_{P-P}
Digital						
Conversion Speed			—	2.5	—	Conv/sec
V_{OH}	Output High Voltage	$I_O = 100\ \mu A$	3.5	4.4	—	V
V_{OL}	Output Low Voltage	$I_O = 1.6$ mA (Note 2)	—	0.18	0.4	V
I_{OP}	Output Leakage Current	High-Impedance State	—	0.1	1	μA
I_{CP}	Control Pin Pull-Up Current	Pins 18, 19, 20; $I_O = 750\ \mu A$ Pin 21 = 0V, $V_O = 2V$	—	5	—	μA
V_{IH}	Input High Voltage	Pins 18–21, 26, 27	2.5	—	—	V
V_{IL}	Input Low Voltage	Pins 18–21, 26, 27	—	—	1	V

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Digital (Cont.)						
I_{IP}	Input Pin Pull-Up Current	Pins 26, 27; V = 2V	—	5	—	µA
		Pins 17, 24; V = 2V	—	25	—	µA
I_{ID}	Input Pin Pull-Down Current	Pin 21, V = 3V	—	5	—	µA
I_{OSC1}	Oscillator Output Current	V_O = 2.5V	—	1	—	mA
I_{BUFOSC}	Buffered Oscillator	V_O = 2.5V Output Current	—	5	—	mA
C_{IN}	Input Capacitance	Pins 18, 19	—	—	50	pF
t_{PW}	$\overline{\text{BUS}}$/ HAND Control Pin Minimum Pulse Width	Pin 21	70	—	—	ns
t_{WBE}	Byte-Enable Pulse Width	Note 1	350	200	—	ns
t_{WCE}	Chip-Enable Pulse Width	Note 1	400	250	—	ns
t_{ABE}	Byte-Enable Access Time	Note 1	—	200	350	ns
t_{ACE}	Chip-Enable Access Time	Note 1	—	250	400	ns
t_{DHB}	Data Hold From	Note 1 Byte-Enable Change	—	140	300	ns
t_{DHC}	Data Hold From	Note 1 Chip-Enable Change	—	240	400	ns
Power						
I_S^+	Positive Supply Current		—	2	3.5	mA
I_S^-	Negative Supply Current		—	2	3.5	mA

NOTES: 1. Parallel data transfer ($\overline{\text{BUS}}$/HAND = 0). See Figures 8 and 9.
2. For pins 18–20, I_O = 750 µA.
3. Crystal source (2.4576 MHz): DIGI-KEY Corp., Highway 32 South, P.O. Box 677, Thief River Falls, MN 56701-9988, Phone 1-800-344-4539, Part No. X047.

PIN DESCRIPTION

Pin No. (40-Pin)	Pin No. (60-Pin)	Symbol	Description (Pin designations refer to 40-Pin DIP)
1	9	SGN	Sign Bit: 1 = positive input. The input signal polarity is determined at the end of the signal-integrate phase.
2	10	DB_{15}	Data Bit 15 (MSB)
3	11	DB_{14}	Data Bit 14
4	12	DB_{13}	Data Bit 13
5	13	DB_{12}	Data Bit 12
6	18	DB_{11}	Data Bit 11
7	19	DB_{10}	Data Bit 10
8	20	DB_9	Data Bit 9
9	21	DB_8	Data Bit 8
10	22	DB_7	Data Bit 7
11	24	DB_6	Data Bit 6
12	25	DB_5	Data Bit 5
13	26	DB_4	Data Bit 4
14	27	DB_3	Data Bit 3
15	28	DB_2	Data Bit 2
16	33	DB_1	Data Bit 1 (LSB)

Three-State Output Data Bits

NOTE: DB_{15}–DB_1 are at logic '1' for an overrange conversion.

PIN DESCRIPTION (Cont.)

Pin No. (40-Pin)	Pin No. (60-Pin)	Symbol	Description (Pin designations refer to 40-Pin DIP)
17	34	TEST	Test = 0V; Data outputs forced to logic '1' and clock is disabled. Test = V^+; Counter latches enabled.
18	35	$\overline{\text{LBEN}}$ / $\overline{\text{LBFLG}}$ (Input/Output)	A low data byte enable input or flag output, depending on $\overline{\text{BUS}}$/ HAND (pin 21) status. (1) $\overline{\text{BUS}}$/ HAND = 0: With pin 21 low and $\overline{\text{CE}}$/ $\overline{\text{LDSTRB}}$ = 0 (pin 20), data bits 8 through 1 (pins 9–16) are output when $\overline{\text{LBEN}}$ = 0. (2) $\overline{\text{BUS}}$/ HAND = 1: Valid data on pins 9–16 is indicated by flag output, $\overline{\text{LBFLG}}$ = 0.
19	36	$\overline{\text{HBEN}}$/ $\overline{\text{HBFLG}}$ (Input/Output)	A high data byte enable input or flag output, depending on $\overline{\text{BUS}}$/ HAND (pin 21) status. (1) $\overline{\text{BUS}}$/ HAND = 0: With pin 21 low and $\overline{\text{CE}}$/ $\overline{\text{LDSTRB}}$ = 0 (pin 20), the high data byte (sign bit plus data bits 15–9) are output when $\overline{\text{HBEN}}$ = 0. (2) $\overline{\text{BUS}}$/ HAND = 1: Valid data on pins 1–8 is indicated by flag output, HBLFG = 0.
20	37	$\overline{\text{CE}}$/ $\overline{\text{LDSTRB}}$ (Input/Output)	(1) $\overline{\text{BUS}}$/ HAND = 0: $\overline{\text{CE}}$ is master chip enable. With $\overline{\text{CE}}$ = 1, sign bit plus data bits 15–1 are disabled (high-impedance state). $\overline{\text{CE}}$ = 0 enables outputs and data is transferred under control of $\overline{\text{LBEN}}$ and $\overline{\text{HBEN}}$.

CE	$\overline{\text{LBEN}}$	$\overline{\text{HBEN}}$	Function
0	0	1	Low Data Byte Output
0	1	0	High Data Byte Output
0	0	0	Low + High Data Byte Output
0	1	1	High-Impedance State

Pin No. (40-Pin)	Pin No. (60-Pin)	Symbol	Description (Pin designations refer to 40-Pin DIP)
			(2) $\overline{\text{BUS}}$/ HAND = 1: $\overline{\text{LDSTRB}}$ is a load strobe output sign. In the handshake mode, $\overline{\text{LDSTRB}}$ = 0 instructs the receiving device to accept data.
21	39	$\overline{\text{BUS}}$/ HAND	(1) $\overline{\text{BUS}}$ = 0: Parallel output data mode, where $\overline{\text{CE}}$, $\overline{\text{HBEN}}$, and $\overline{\text{LBEN}}$ directly control the 16 data bits. (2) HAND = 1: $\overline{\text{LDSTRB}}$, $\overline{\text{LBFLG}}$, $\overline{\text{HBFLG}}$ are used in the handshake data transfer mode. (3) HAND = (pulsed high): Causes entry into handshake mode for UART interfacing.
22	40	OSC_2	Oscillator input.
23	41	OSC_1	Oscillator output.
24	42	OSC CON	Selects internal oscillator structure. (1) OSC CON = 1: RC oscillator. Internal clock frequency is same frequency and duty cycle as BUF OSC. (2) OSC CON = 0: Crystal oscillator. Internal clock frequency is frequency at BUF OSC 415.
25	43	BUF OSC	Buffered oscillator output
26	48	CONVERT / $\overline{\text{STOP}}$	CONVERT = 1: Conversions performed continuously. $\overline{\text{STOP}}$ = 0: Conversion process stops 7 counts before entering signal-integrate phase. The conversion in progress when $\overline{\text{STOP}}$ = 0 is completed.
27	49	DRQST	Data request signal. Used in handshake mode to indicate an external device is ready to accept data. If DRQST is not used, connect to V_S^+.
28	50	V_S^-	Negative power supply.
29	51	V_{REF}	Voltage reference input.
30	52	COM	Analog common. The TC800 is auto-zeroed to the analog common potential.
31	54	V_{INT}	Integrator output.
32	55	C_{SZ}	System-zero capacitor.
33	56	V_{BUF}	Output of input signal buffer.
34	57	C_R^-	Negative Reference capacitor.

PIN DESCRIPTION (Cont.)

Pin No. (40-Pin)	Pin No. (60-Pin)	Symbol	Description (Pin designations refer to 40-Pin DIP)
35	59	C_R^+	Positive Reference capacitor.
36	1	V_{IN}^-	Negative differential analog input.
37	3	V_{IN}^+	Positive differential analog input.
38	5	V_S^+	Positive power supply
39	6	GND	Digital ground. Ground return point for digital logic.
40	7	$\overline{DVC}$	Data valid signal. $\overline{DVC}$ = 1 during signal-integrate and reference-integrate phases until data is latched. $\overline{DVC}$ = 0 when in auto-zero phase; data does not change.

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles

The TC800 is a dual-slope, integrating ADC. An understanding of the dual-slope conversion technique will aid in following the detailed operation theory.

The conventional dual-slope converter measurement cycle has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration).

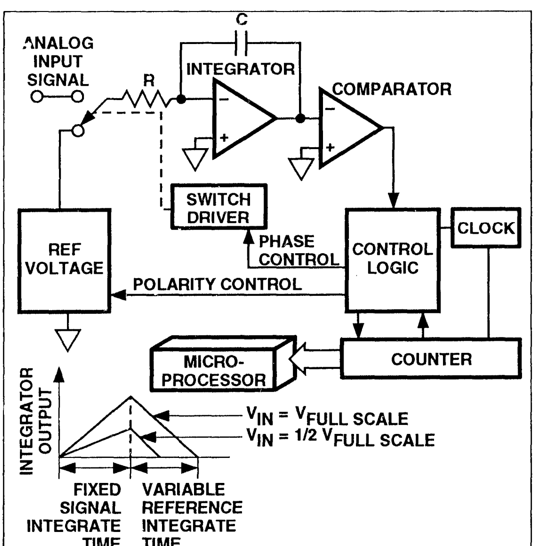


Figure 1 Basic Dual-Slope Converter

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity, constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter (Figure 1), a complete conversion requires the integrator output to 'ramp-up' and 'ramp-down.'

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. Noise immunity is an inherent benefit. Noise spikes are integrated, or averaged, to zero during integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments.

A simple mathematical equation related the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R t_{RI}}{RC}$$

where: V_R = Reference voltage
t_{SI} = Signal integration time
t_{RI} = Reference voltage integration time (variable)

For a constant V_{IN}:

$$V_{IN} = V_R \left[\frac{t_{RI}}{t_{SI}}\right]$$

ANALOG SECTION DESCRIPTION

System-Zero Phase

During system-zero phase (Figure 2), errors due to buffer, integrator, and comparator offset voltages are compensated for by charging system-zero capacitor (C_{SZ}) with a compensating error voltage. With zero input voltage, the integrator output remains at zero.

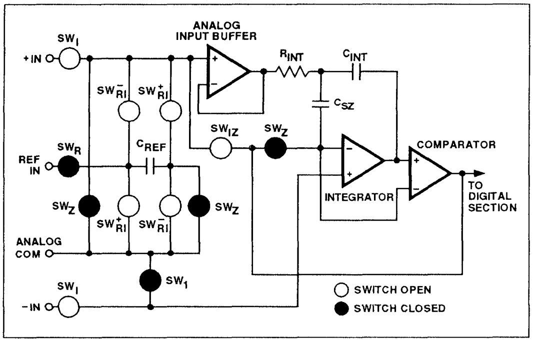


Figure 2 System-Zero Phase

The external input signal is disconnected from internal circuitry by opening two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges C_{SZ} with a voltage to compensate for buffer amplifier, integrator, and comparator offset voltages.

Input Signal-Integration Phase

The TC800 integrates differential voltage between the (+) and (–) inputs (Figure 3). The differential voltage must be within the device common-mode range; 1V from either supply rail, typically. The input signal is integrated for 16,384 clock cycles.

The input signal polarity is determined at the end of the phase.

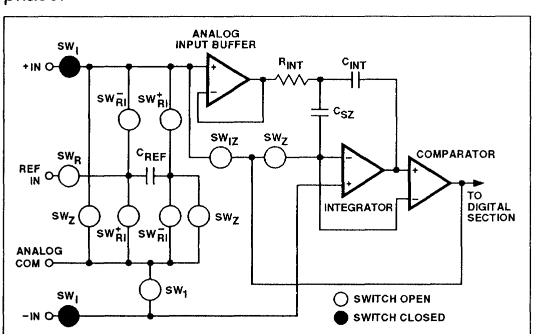


Figure 3 Input Signal Integration Phase

Reference Voltage Integration Phase

The previously-charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The time for the output to return to zero is proportional to the input signal magnitude. The phase lasts for a maximum of 32,768 clock periods. (See Figure 4.)

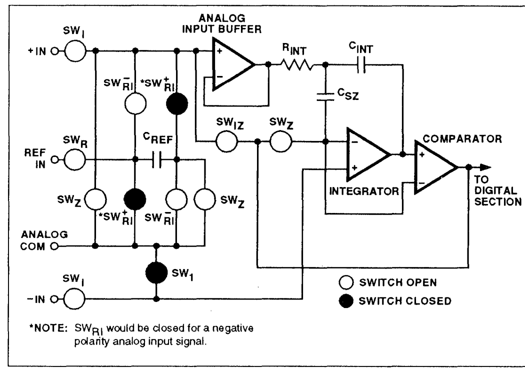


Figure 4 Reference Voltage Integration Phase

Integrator Output Zero Phase

This phase guarantees the integrator output is at 0V when the system-zero phase is entered and that true system offset voltages are compensated for. This phase normally lasts 4096 clock cycles. (See Figure 5.)

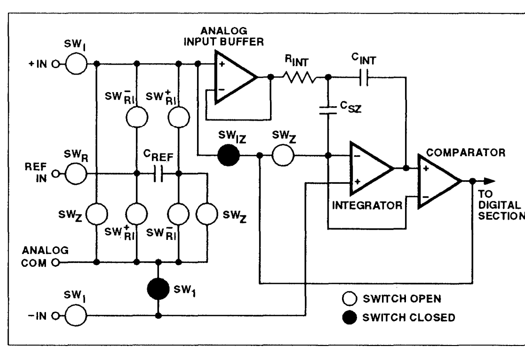


Figure 5 Integrator Output Zero Phase

Differential Inputs
V_{IN}^+ (Pin 37) and V_{IN}^- (Pin 36)

The TC800 operates with differential voltages within the input amplifier common-mode range, extending from 1V below V_{IN}^+ to 1V above V_{IN}^-. Within this common-mode voltage range, an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used by the positive common-mode voltage. For these critical applications, the integrator output swing can be reduced to within 0.4V of either supply without loss of linearity.

Analog Common

Analog common (COM, pin 30) is used as the V_{IN}^- return during system-zero and reference-integrate phases. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications, V_{IN}^- will be set at a fixed, known voltage (power supply common, for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog common.

DIGITAL SECTION DESCRIPTION

Digital Control Signals

$\overline{\text{BUS}}$ / HAND

The $\overline{\text{BUS}}$ / HAND input (pin 21) selects parallel bus data transfer mode or handshake transfer mode. An internal pull-down resistor guarantees parallel mode operation when the input pin is open. The handshake mode allows serial data transmission with a UART. In parallel mode, the TC800 outputs data under control of the $\overline{\text{HBEN}}$ (pin 19), $\overline{\text{LBEN}}$ (pin 18), and $\overline{\text{CE}}$ (pin 20) signals. In the handshake mode, the TC800 output signals communicate with peripheral devices to control data transmission.

For $\overline{\text{BUS}}$ = 0, $\overline{\text{HBEN}}$, $\overline{\text{LBEN}}$, and $\overline{\text{CE}}$ input signals control data transmission. Figures 8 and 9 show typical timing relationships and operation. The $\overline{\text{HBEN}}$, $\overline{\text{LBEN}}$, and $\overline{\text{CE}}$ signals are asynchronous to the internal conversion clock. Output data is immediately accessed. To avoid accessing data as updates are occurring, the data valid (DVD, pin 40) signal can be used as an enable signal. Data will not change if DVD = 0.

In handshake mode, two data transfer methods are possible. If HAND is pulsed high (HAND = ⎍) for a minimum of 70 ns, the TC800 enters the handshake mode. If HAND = 1 continuously, the parallel mode is not re-entered, and a handshake data transfer will occur at the end of each conversion cycle.

The $\overline{\text{BUS}}$ / HAND input configures dual-purpose pins 18, 19, and 20 as inputs or outputs. In conjunction with the data request input signal, handshake data transfer is controlled by output signals $\overline{\text{LBFLG}}$, $\overline{\text{HBFLG}}$, and $\overline{\text{LDSTRB}}$. (See Table I.)

Data Request Input

The data request (DRQST, pin 27) input is used only in the handshake data transfer mode. DRQST = 1 indicates an external receiving device is ready to accept data from the TC800. It serves as a send data command. When $\overline{\text{BUS}}$ / HAND = 0, DRQST should be tied to V_S^+.

Table I (Pin designations refer to 40-Pin DIP)

	Pin Description		
Operating Mode	**$\overline{\text{LBEN}}$ / $\overline{\text{LBFLG}}$ (Pin 18)**	**$\overline{\text{HBEN}}$ / $\overline{\text{HBFLG}}$ (Pin 19)**	**$\overline{\text{CE}}$ / $\overline{\text{LDSTRB}}$ (Pin 20)**
Bus Transfer Mode $\overline{\text{BUS}}$/ HAND = 0	$\overline{\text{LBEN}}$: Low data byte enable input. Logic '0' activates low-order data (DB_8–DB_1) if $\overline{\text{CE}}$ = 0.	$\overline{\text{HBEN}}$: High data byte enable input. Logic '0' activates the high order data (SGN, DB_{15}–DB_9) if $\overline{\text{CE}}$ = 0.	$\overline{\text{CE}}$: Master output enable input. When $\overline{\text{CE}}$ = 1 outputs SGN, DB_{15}–DB_1 are disabled and in a high-impedance state
Handshake Transfer Mode $\overline{\text{BUS}}$/ HAND = 1 or ⎍	$\overline{\text{LBFLG}}$: Low data byte flag output. Indicates output data is DB_8–DB_1.	$\overline{\text{HBFLG}}$: High data byte flag output. Indicates output data is DB_{15}–DB_9.	$\overline{\text{LDSTRB}}$: Load strobe output signal. A logic '0' or falling edge indicates valid data is present at the output.

CONV / $\overline{\text{STOP}}$ Input

The CONV / $\overline{\text{STOP}}$ input (pin 26) is pulled high through an internal pull-up resistor. If CONV / $\overline{\text{STOP}}$ = 1, or is left open, the TC800 continuously performs conversions. Each measurement cycle is 65,536 counts long. The measurement cycle time for one conversion is:

$$\text{Time Conversion (ms)} = \frac{65.536}{f_{CLK}\ (\text{kHz})},$$

where f_{CLK} = Internal clock frequency.

If CONV / $\overline{\text{STOP}}$ = 0 during reference-integrate phase and after zero-crossing has been detected, the integrator-zero phase is immediately entered and completed. This eliminates the time spent in the reference-integrate phase after the output data latches are updated.

If CONV / $\overline{\text{STOP}}$ remains low, the TC800 will wait in the system-zero phase. The signal-integrate phase begins 7 clock counts after a CONV = 1 signal is detected. The CONV / $\overline{\text{STOP}}$ signal is detected synchronously with the internal clock. The system-zero phase should last a minimum of 70 ms. (See Figures 6 and 7 for CONV / $\overline{\text{STOP}}$ conversion timing diagrams.)

If CONV / $\overline{\text{STOP}}$ goes low and remains low during the system-zero phase, the TC800 will stop at the end of the phase and wait for CONV = 1. The signal-integrate phase will start 7 clock counts after CONV = 1 is detected.

TEST Input

When TEST (pin 17) = 1, the counter data latches are enabled. When TEST = 0, the counter outputs are forced to a logic '1' state and the internal clock is disabled. When TEST is returned to logic '1' and one clock pulse is applied, all counter outputs are clocked low.

Data Valid

Data valid ($\overline{\text{DVD}}$, pin 40) = 1 at the start of signal integrate and $\overline{\text{DVD}}$ = 0 one-half clock period after new data is stored in the data latches. Since $\overline{\text{DVD}}$ is always low when data is not changing, the signal may be used as a 'Data Valid Flag.' (See Figures 6 and 7 for timing relationships.)

DATA OUTPUT DESCRIPTION

Parallel Mode Data Interface

With BUS / $\overline{\text{HAND}}$ = 0, the sign and data bits are controlled by the $\overline{\text{CE}}$, $\overline{\text{LBEN}}$, and $\overline{\text{HBEN}}$ inputs. All three have internal pull-up resistors. Inactive data bits are in a high-impedance state.

The $\overline{\text{HBEN}}$ signal controls the most significant data bytes (SGN, DB_{15}–DB_9). $\overline{\text{LBEN}}$ controls the least significant data bytes (DB_8–DB_1).

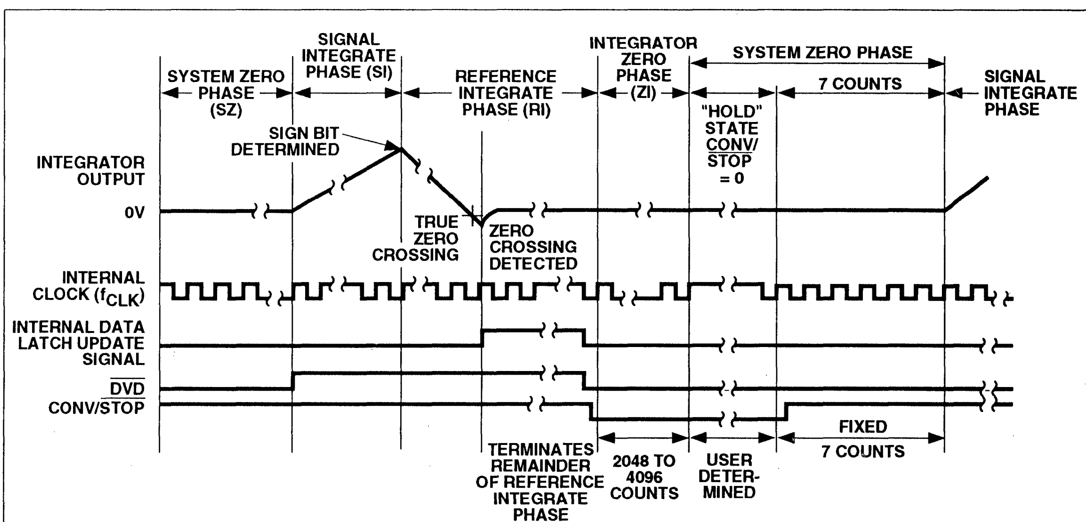


Figure 6 Convert-on-Command Operation (CONV / $\overline{\text{STOP}}$ = 0 After Zero Crossing Detected)

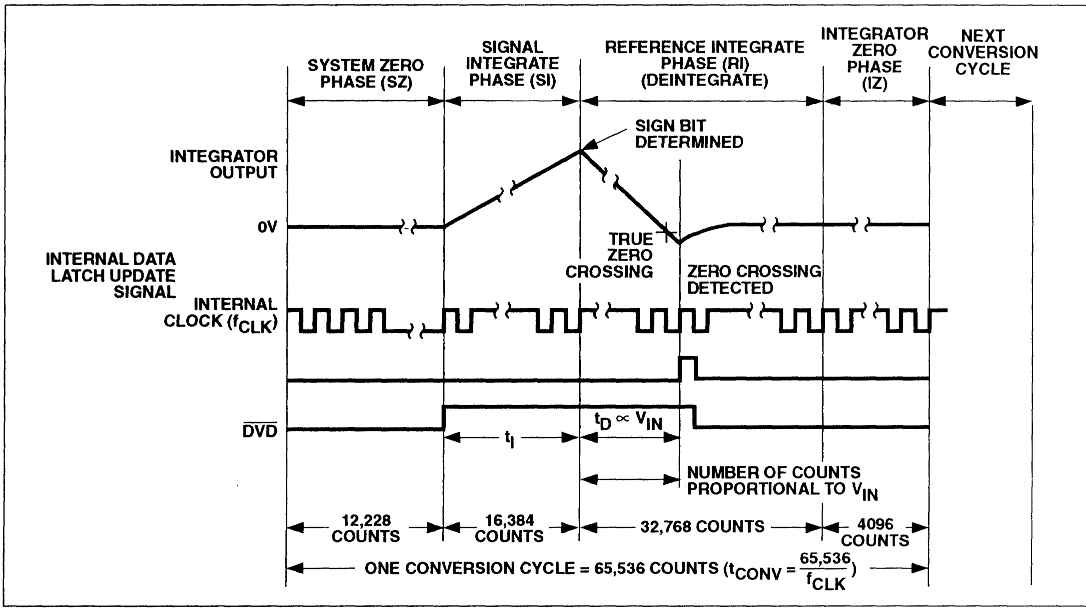


Figure 7 Continuous Conversion (CONV / $\overline{\text{STOP}}$ = 1)

Table II

CE	$\overline{\text{HBEN}}$	$\overline{\text{LBEN}}$	High Data Byte (SGN, DB_{15}–DB_9)	Low Data Byte (DB_8–DB_1)
1	X	X	Inactive (High Z State)	Inactive (High Z State)
0	0	0	Active	Active
0	0	1	Active	Inactive (High Z State)
0	1	0	Inactive (High Z State)	Active
0	1	1	Inactive (High Z State)	Inactive High Z State)

NOTE: X = 1 or 0.

The $\overline{\text{HBEN}}$, $\overline{\text{LBEN}}$, and $\overline{\text{CE}}$ inputs are asynchronous with the internal conversion clock. Output data is immediately available. To avoid accessing data as updates occur, the $\overline{\text{DVD}}$ input can control data access. Data will not change if DVD = 0.

Handshake Mode Data Transfer

The TC800 actively controls data transfer to peripherals through the handshake data transfer mode. In the handshake mode, pins 18, 19, and 20 ($\overline{\text{LBFLG}}$, $\overline{\text{HBFLG}}$, and LDSTRB) are TTL-compatible outputs. The LDSTRB signal indicates valid data is available for the peripheral. The LBFLG and HBFLG signals indicate which data byte is being transferred. The data request signal (DRQST, pin 27) informs the TC800 a peripheral is ready to accept data. A complete cycle transfers two 8-bit bytes.

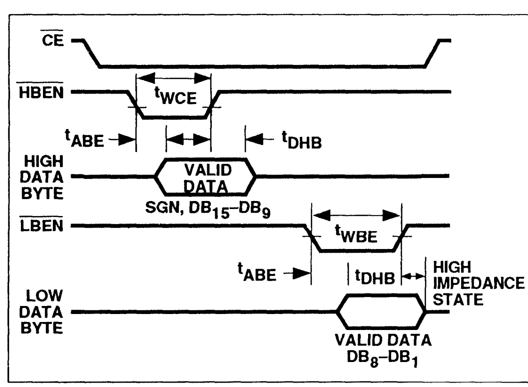


Figure 8 Parallel Data Transfer (Two 8-Bit Bytes)

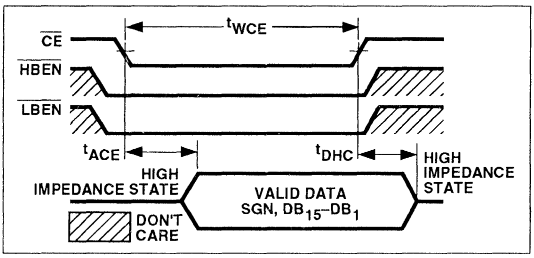


Figure 9 Parallel Data Transfer (16-Bit Bytes)

The $\overline{\text{BUS}}$ / HAND signal is ignored after the handshake mode is entered. Conversions continue, but data latch updating is inhibited until the TC800 transfers two data bytes and clears the internal mode latch.

The handshake mode is entered in two ways:

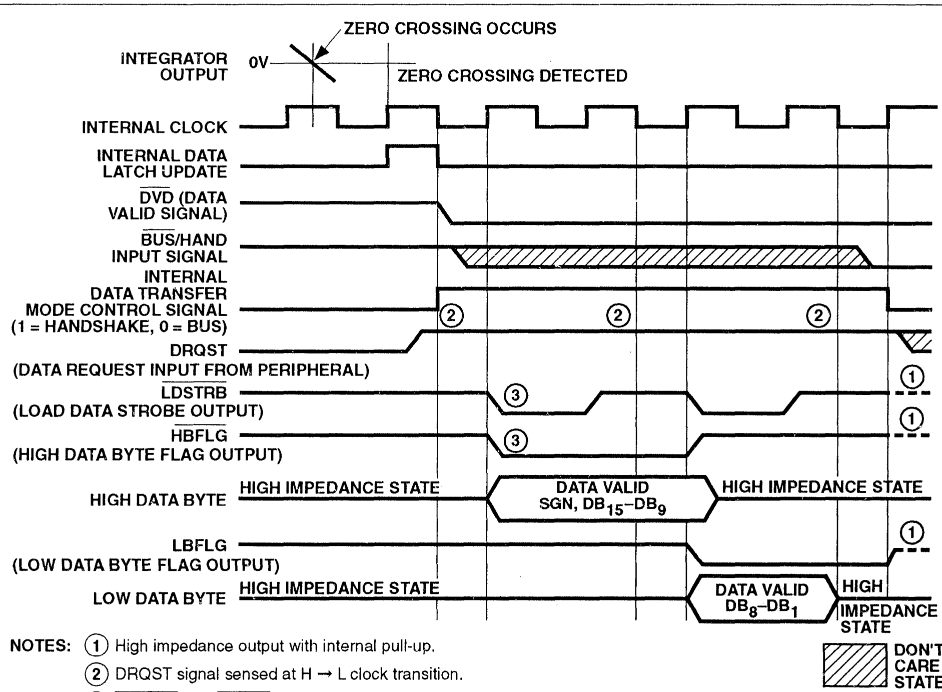
(1) Set $\overline{\text{BUS}}$ / HAND = 1

(2) Pulse $\overline{\text{BUS}}$ / HAND High (__┌┐__)

$\overline{\text{BUS}}$ / HAND = 1

With $\overline{\text{BUS}}$ / HAND = 1, the TC800 enters the handshake mode after data is stored in the output data latches. Once the handshake mode internal latch signal is set, the $\overline{\text{BUS}}$ / HAND signal is ignored. The DRQST signal controls data transfer to the external requesting peripheral. Figure 10 shows the timing diagram for the data transfer with $\overline{\text{BUS}}$ / HAND = 1 (throughout the transfer). Note that DRQST = 1 throughout the transfer. The data transfer rate is set by the TC800 internal clock. A complete data transfer occurs in 4 clock periods after a DRQST = 1 is detected on a high-to-low internal clock-edge transition.

For peripherals that cannot accept data at the TC800 clock rate, the DRQST input can be used to delay the transmit sequence. This mode is useful in interfacing to UARTs. Figure 11 shows a typical UART interface.



NOTES: (1) High impedance output with internal pull-up.
(2) DRQST signal sensed at H → L clock transition.
(3) $\overline{\text{LDSTRB}}$ and $\overline{\text{HBFLG}}$ become active at first L → H clock transition after DRQST is sensed H.

Figure 10 Data Trasfer With $\overline{\text{BUS}}$/HAND = 1

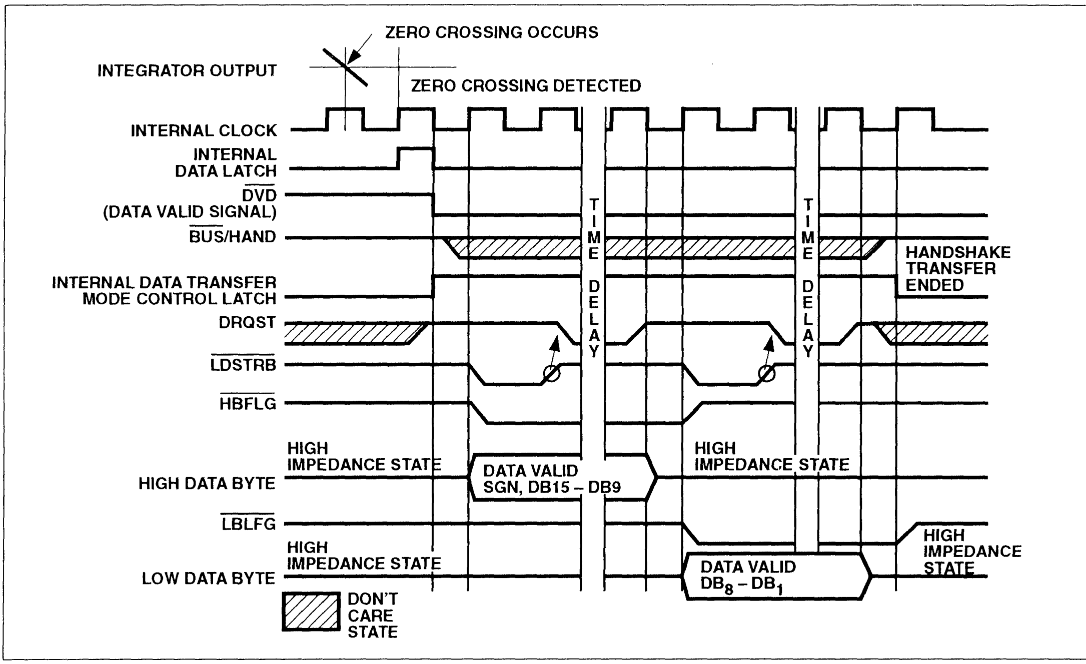
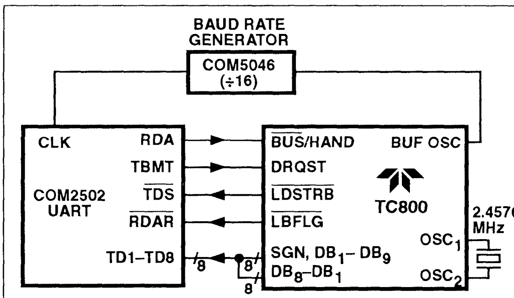


Figure 11A Typical UART Interface Timing With DRQST Signal Controlling Data Transfer Timing

The UART data transfer sequence begins with DRQST = 1, indicating the UART transmitter buffer register is empty (TBMT = 1). LDSTRB and HBFLG become active when DRQST is sensed synchronously. The high-order data byte is stored in the UART transmitter buffer register when LDSTRB = 1. This occurs one clock period after DRQST is sensed. The DRQST signal (TBMT) goes low, halting the cycle with the SGN and DBN_{15}–DB_9 data bits active. After the UART transfers the received data to the transmitter register, DRQST (TBMT) goes high. On the first high-to-low internal clock transition, the high data byte is disabled and one-half clock period later HBFLG = 1. Concurrently, LDSTRB = 0 and DB_8–DB_1 become active. One clock period later, LDSTRB = 1 and the low data byte is clocked into the UART transmitter buffer register; DRQST goes low. When DRQST returns high, it is sensed on the first TC800 internal clock high-to-low edge transition, thus causing all outputs to be disabled. One-half clock period later the internal handshake mode latch is cleared and LDSTRB = HBFLG = LBFLG = 1. The outputs remain active as long as BUS / HAND = 1.



RDA = Receiver Data Available (Set high when character received and transferred to receiver buffer register.)

TBMT = Transmitter Buffer Empty (Set high when transmitter buffer register available for loading new data.)

TDS = Transmitter Data Strobe (Low level input transfers data into transmitter register.)

RDAR = Receiver Data Available Reset (Low level resets RDA output to low level.)

Figure 11B Typical UART to TC800 Connection

BUS / HAND = (Pulse High)

The TC800 outputs every conversion (except those completed during a handshake transfer) with BUS / HAND held high. Handshake output sequences on demand are possible by triggering the BUS / HAND control input with a low-to-high edge. Figure 12 shows a typical data transfer. The output cycle is controlled by the DRQST input signal. The complete 2-byte data transfer can take any length of time. Conversions are made, and the DVD and CONV / STOP inputs function normally, but new data will not be latched until the handshake mode is terminated.

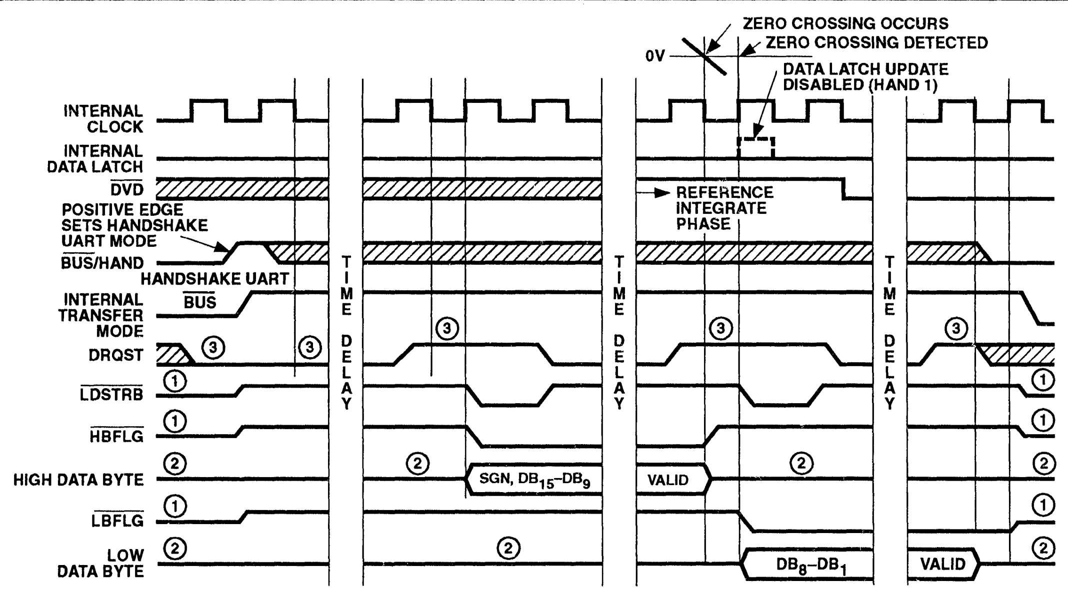
Oscillator Control and Operation

The OSC CON input (pin 24) configures the internal oscillator as a crystal or RC oscillator. OSC CON = 1 establishes the RC oscillator; R should be 50 kW or larger. The internal clock matches the frequency and phase of the BUF OSC (pin 25) signal. In the crystal oscillator mode (OSC CON = 0), a 415 is between the buffered oscillator output and the internal clock. The internal oscillator may be overdriven by driving OSC_1 (pin 23). The OSC CON pin controls whether the internal clock is 415. (See Table III.)

Table III

Oscillator Type	OSC CON (Pin 24)	Internal Clock Frequency	Signal Integration Time	Conversion Cycle Time
RC	V_S^+ or Open	0.45/RC	$16{,}384\left(\frac{RC}{0.45}\right)$	$\frac{RC}{0.45}(65{,}536)$
Crystal	Ground	f_{XTAL} 415	$16{,}384\left(\frac{15}{f_{XTAL}}\right)$	$\frac{15}{f_{XTAL}}(65{,}536)$

NOTES:
1. f_{XTAL} = crystal frequency (2.4576 MHz)
2. Internal clock frequency = 163.8 kHz
3. Signal integration time = 1000 ms
4. Conversion cycle time = 400 ms (2.5 conversions/sec)



NOTES: (1) High impedance state with resistive pull up.
(2) High impedance state.
(3) DRQST input sensed.
(4) Output sequence greater than conversion cycle.

Figure 12 Handshake Output on Command (DRQST Signal Controls Transfer)

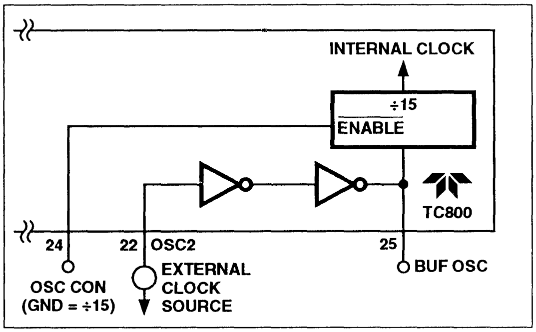


Figure 13 External Oscillator Control

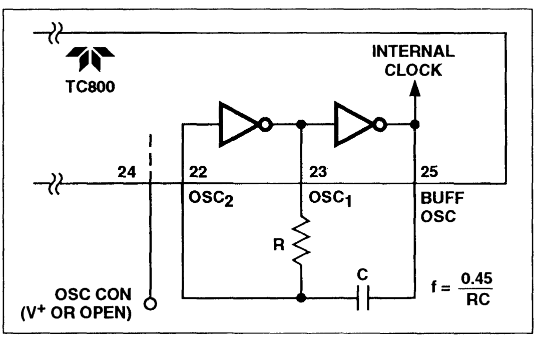


Figure 14 Internal RC Oscillator Configuration

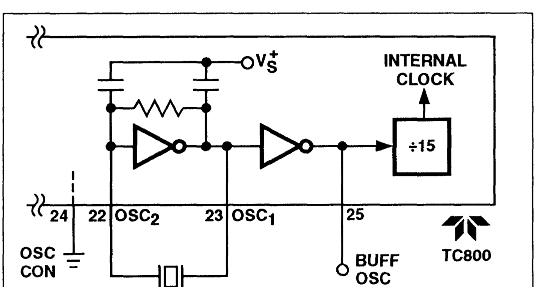


Figure 15 Internal Crystal Oscillator Configuration

Component Value Selection

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal Class A output stage amplifiers supply a 20 μA drive current with minimal linearity error. R_{INT} is easily calculated for a 20 μA full-scale current:

$$R_{INT}\ (\text{M}\Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{20}$$

Full-Scale Input Voltage (V_{FS})	R_{INT}
3.2768	160 kW
4.0000	200 kW

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4V of V_S^+ or V_S^- without saturating. With ±5V power supplies and analog common connected to supply ground, a 3.5V to 4.3V swing is adequate.

Using the suggested 20 μA full-scale buffer output current, the integrating capacitor is easily calculated:

$$C_{INT}\ (\mu\text{F}) = \frac{16{,}384\left(\frac{1}{f_{CLK}\ (\text{kHz})}\right)20\ \mu\text{A}}{\text{Integrator Output Voltage Swing (V)}},$$

where f_{CLK} = Internal clock frequency.

For 2.5 conv/sec, the internal clock frequency is 163.8 kHz. The TC800 operates at 2.5 conv/sec with an external crystal equal to 2.4576 MHz. A 0.47 μF capacitor is recommended.

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested. The outer foil of C_{INT} should be connected to pin 31.

System Zero Capacitor (C_{SZ})

A 1 μF polypropylene capacitor is suggested. The inner foil should be connected to C_{SZ} (pin 32).

Reference Capacitor (C_{REF})

A 1 μF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitors such as polypropylene or Teflon® should be used.

Reference Voltage

The analog input required to generate the 32,768 full-scale count is $V_{IN} = 2\ V_{REF}$. The reference voltage source should be selected for temperature stability. The TC800 provides 30 ppm resolution. With a 5 ppm/°C reference, a 6° change will introduce a 1-bit absolute error. A stable reference must be used where ambient temperature is controlled and accurate absolute measurements are needed.

The reference voltage input must be a positive voltage with respect to analog common. Reference voltage circuits are shown in Figure 16.

Delay Resistor (R_S)

The R_S, C_{INT} combination compensates for comparator delay time. With a 0.47 µF integrating capacitor, a 20W series resistor is suggested.

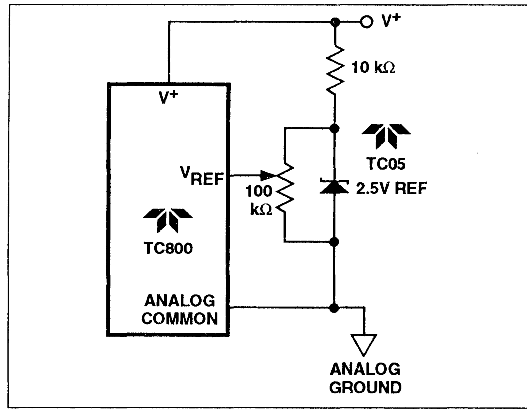
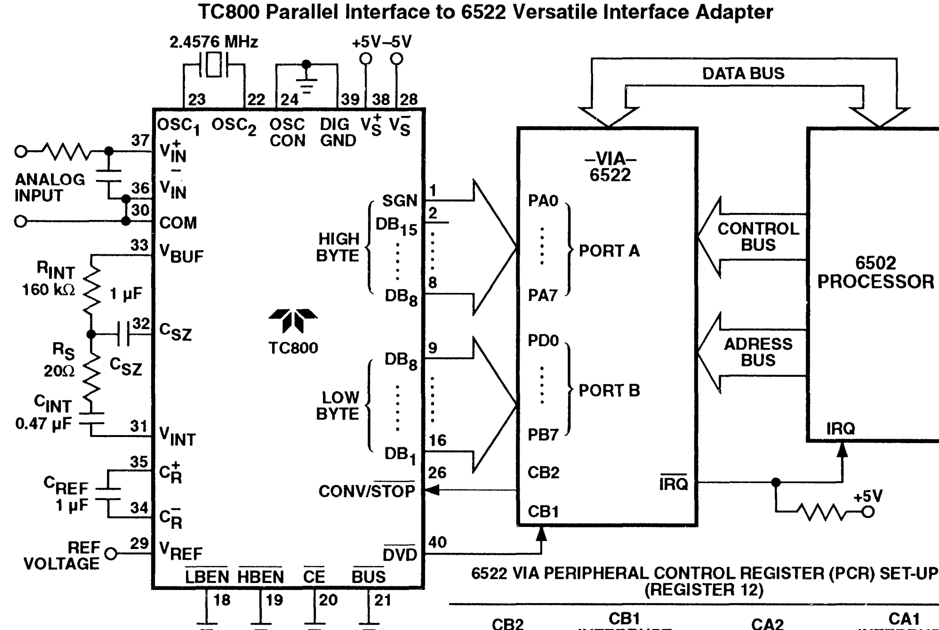


Figure 16 Reference Voltage Circuits

TYPICAL APPLICATIONS

TC800 Parallel Interface to 6522 Versatile Interface Adapter



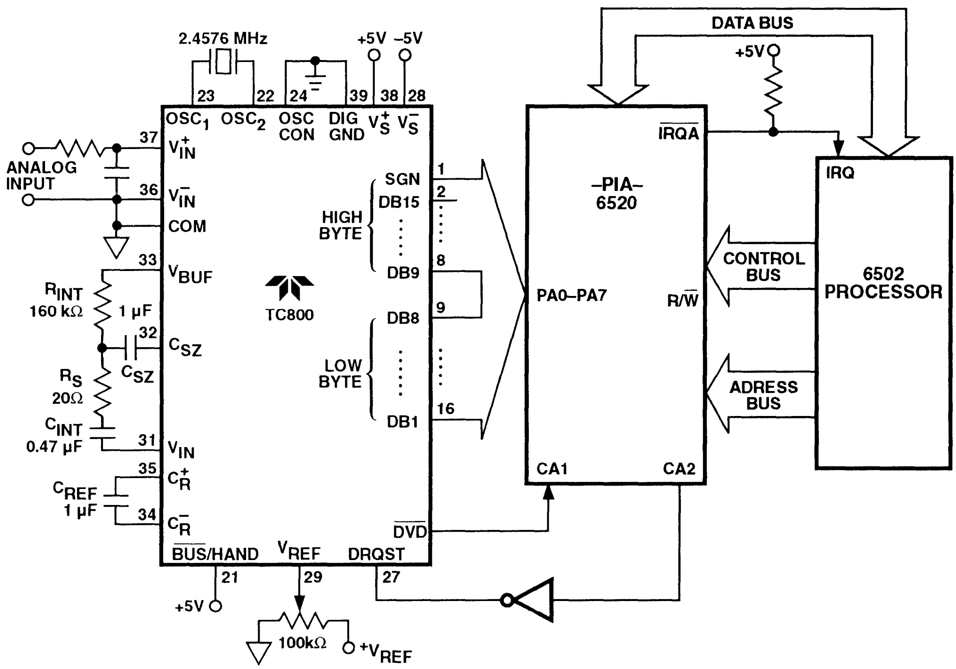
6522 VIA PERIPHERAL CONTROL REGISTER (PCR) SET-UP (REGISTER 12)

CB2 CONTROL		CB1 INTERRUPT CONTROL	CA2 CONTROL			CA1 INTERRUPT CONTROL
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0/1*	–	–	–	–	–

***NOTE:** May be programmed for convert on command or continuous conversions.

TYPICAL APPLICATIONS (Cont.)

TC800 Interface to 6520 VIA



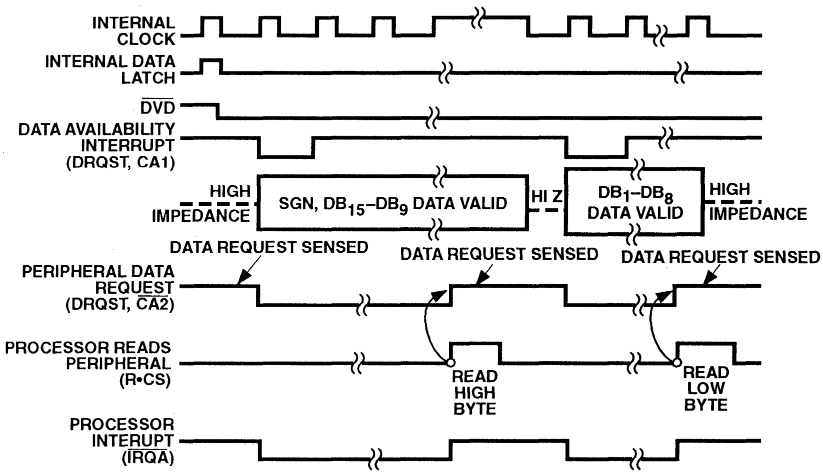
6520 PIA CONTROL REGISTER A (CRA) SET-UP

IRQA1	IRQA2	CA2 CONTROL			DDRA ACCESS	CA1 CONTROL	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	1	0	0	0	0	1
Set by a negative CA1 transmission. reset by a read port A operation.		CA2 is set high on negative CA1 transmission. A port A read operation sets CA2 low.			Port A conf-gured as input.	IRQA output enabled — goes low when Bit 7 in CRA is set by negative transition of signal on CA1.	

TC800

TYPICAL APPLICATIONS (Cont.)

TC800 to 6520 Peripheral Interface Adapter Handshake Timing Diagram



NOTE: Data from every conversion is transmitted in 2 bytes.
(Data read cycle is less than conversion time.)

12-BIT µP-COMPATIBLE MULTIPLEXED A/D CONVERTER

FEATURES

- **12-bit Plus Sign, High Accuracy A/D Converter**
- **Up to 30 Conversions per Second**
- **Selectable Conversion Rate**
- **On-Board Analog Mux .... 4 or 8 Channel**
- **Very Fast Overload Recovery**
- **High Impedance Differential Input**
- **Low Noise CMOS Design .... 15µV$_{p-p}$**
- **Analog Mux Expansion Capability**
- **Low Input Leakage Current, 10pA (Max)**
- **Flexible Digital and µProcessor Interfacing**
- **Internal Reference Regulator, 50ppm/°C**
- **Power Up to Known State**
- **Crystal Controlled Clock Circuit**
- **Available in Compact Flat Package or PLCC**
- **Industrial Temperature Range Device Available**

GENERAL DESCRIPTION

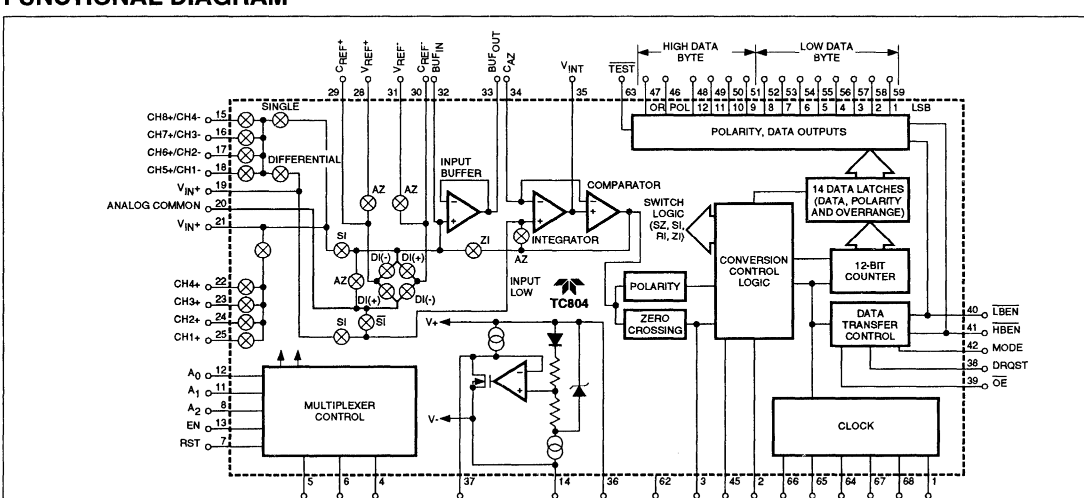
The TC804 is a 12-bit (plus sign and over-range) analog to digital converter. It is equivalent to the popular TC7109A except that the TC804 incorporates an on-board analog multiplexer which may be configured for either 4 or 8 channel operation under software control. The TC804 represents the latest technology in multi-slope, high noise immunity, integrating A/D conversion. The advanced CMOS design offers very low power consumption and high reliability.

The TC804 provides two very flexible modes of digital interfacing to fit a variety of system configurations. The Handshake Mode supports either fast or slow UART interfacing with either triggered or continuous operation. The Direct Output Mode supports microprocessor systems that use a direct bus architecture with either an 8-bit or 16-bit data bus structure.

TYPICAL APPLICATIONS

- **Process Control**
  - **—Flow Measurement**
  - **—Leak Detection**
  - **—pH Measurement**
  - **—Pressure**
  - **—Temperature**
  - **—Viscosity**
  - **—Position**
- **Data Acquisition**
- **Environmental Monitoring**
- **Portable Instrumentation**
- **Power Supply Monitoring**
- **Medical Monitoring**
- **Scales and Balances**
- **Photo-Voltaic Instruments**

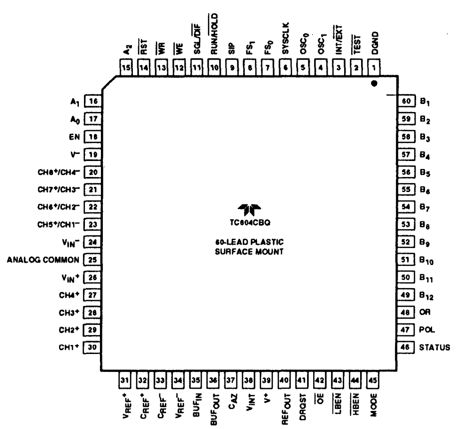
FUNCTIONAL DIAGRAM

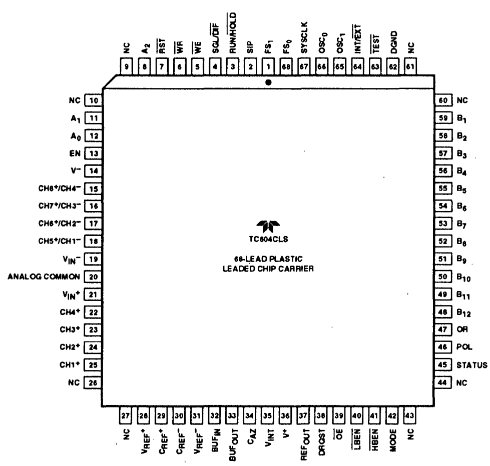


NOTE: Pin numbers are for 68-pin PLCC package.

TC804

PIN CONFIGURATIONS





NC = NO INTERNAL CONNECTION

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC804CLS	68-pin PLCC	0°C to +70°C
TC804CBQ	60-pin Plastic Surface Mount	0°C to +70°C
TC804ILS	68-pin PLCC	−25°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V+) .... +6.2V
Negative Supply Voltage (V−) .... −9.0V
Analog Input Voltage Range (Note 1) .... V+ to V−
Reference Input Voltage Range .... V+ to V−
Digital Input or Output
(Note 2) .... V+ to DGND − 0.3
Power Dissipation (Note 3) .... 1W @ +85°C
Operating Temperature
Commercial .... 0°C to 70°C
Industrial .... −25°C to +85°C
Storage Temperature .... −65°C to +150°C
Lead Temperature (60 sec.) .... +300°C

NOTE: All devices contain diodes to protect inputs against damage due to high-static voltages or electric fields. However, it is advised precautions be taken not to exceed maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (V_{DD} or GND). Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

NOTES:
1. Input voltages may exceed supply voltages if input current is limited to ±100 µA.
2. Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latch-up. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TC804 before its power supply is established. In multiple supply systems, the supply to the device should be activated first.
3. This limit refers to that of the package and will not occur during normal operation.

ELECTRICAL CHARACTERISTICS: V+ = 5V, V– = –5V, 15 Conversions/Sec, 1MHz Crystal, T_A = 25°C (unless otherwise noted)

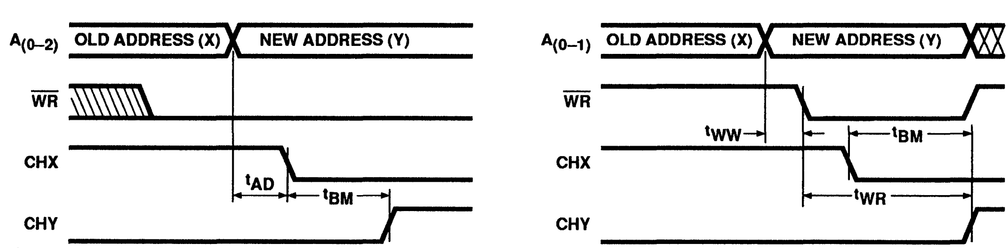
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog Multiplexer Section						
$r_{DS}ON$	On Resistance		—	5.0	7.5	KΩ
		–25°C ≤ T_A ≤ 85°C	—	7.0	10	
t_{BM}	Break-before-Make		250	450	—	nSec
t_{AD}	Address Delay, Transparent		—	150	180	nSec
t_{WW}	Address Set-up, Write		50	—	70	nSec
t_{WR}	Write Delay		—	600	650	nSec
		–25°C ≤ T_A ≤ 85°C	—	650	750	
CORR	Channel Off Rejection Ratio	f_{IN} = 10Hz	—	100	—	dB
Converter Section						
	Zero Input Reading	V_{IN} = 0, V_{FS} = 409.6mV	000_{16}	000_{16}	000_{16}	Count
	Ratiometric Reading	V_{IN} = V_{REF} = 204.8mV		$7FF_{16}$		Count
NLE	Non-linearity Error	V_{FS} = 204.8 or 409.6mV	–1	±0.2	1	Count
ROE	Roll-over Error	V_{FS} = 204.8 or 409.6mV	–1	±0.2	1	Count
CMRR	Common-mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V	—	50	100	µV/V
V_{CMR}	Common-mode Voltage Range		V– +1.5	—	V+ –1.5	V
V_n	Noise (aver. pk–pk)		—	15	50	µV
I_{IL}	Input Leakage Current	T_A = 25°C	—	20	45	pA
		0°C ≤ T_A ≤ 70°C	—	100	200	
		–25°C≤ T_A ≤ 85°C	—	150	300	
TC_O	Zero Reading Drift	0°C ≤ T_A ≤ 70°C	—	0.2	1.0	µV/°C
		–25°C ≤ T_A ≤ 85°C	—	0.8	2.0	
TC_{FS}	Full-scale Gain Tempco	0°C ≤ T_A ≤ 70°C	—	1	5	ppm/°C
		–25°C ≤ T_A ≤ 85°C	—	7	15	
	Over Range Recovery (Next Conversion)	V_{FS} = 204.8mV	—	±1	±2	Count
Supply/Reference Section						
V+	Positive Supply Voltage		4.5	5.0	5.5	V
V–	Negative Supply Voltage		–4.5	–5.0	–5.5	V
I+	Supply Current V+ to GND		—	1.5	2.0	mA
		–25°C ≤ T_A ≤ 85°C	—	2.0	2.5	
I–	Supply Current V– to GND		—	–1.5	–2.0	mA
		–25°C ≤ T_A ≤ 85°C	—	–2.0	–2.5	
V_{REF}	Reference Voltage	(w/ respect to V+)	–2.8	–3.0	–3.2	V
TC_{REF}	Reference Voltage Tempco	0° ≤ TA ≤ 70°C	—	25	50	ppm/°C
		–25°C ≤ T_A ≤ 85°C	—	30	75	
Digital Section						
V_{OH}	Output High (SYSCLK, SIP)	I_{OL} = –100µA	—	4.5	—	V
V_{OH}	Output High (B_1–B_{12}, OR, POL, STATUS)	I_{OL} = –100µA	3.5	4.7	—	V
V_{OL}	Output Low (SYSCLK, SIP)	I_{OL} = 0.5mA	—	0.2	—	V
V_{OL}	Output Low (B_1–B_{12}, OR, POL STATUS)	I_{OL} = 1.6mA	—	0.2	0.4	V
I_{OL}	Output Leakage (High Impedance)	B_1–B_{12}, OR, STATUS	—	.01	1.0	µA

TC804

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Digital Section (Cont.)						
	Control I/O Loading	$\overline{LBEN}$, $\overline{HBEN}$, $\overline{OE}$	—	—	50	pF
V_{IH}	Input High Voltage		2.5	—	—	V
V_{IL}	Input Low Voltage		—	—	1	V
I_{PU}	Input Pull-up Current $\overline{TEST}$	(All except $\overline{TEST}$)	— —	30 100	— —	μA μA
I_{PD}	Input Pull-down Current Mode		—	30	—	μA
t_W	Mode Input Pulse Width $\overline{WR}$, $\overline{WE}$		—	50	—	nSec
Oscillator Section						
f_{OSC}	Frequency of Oscillation		0.8	1.0	5.0	MHz
OSC_{OH}	Output Current High		—	1	2.0	mA
OSC_{OL}	Output Current Low		—	1.5	3.0	mA

ANALOG MULTIPLEXER TIMING DIAGRAM



Transparent Mode

Write Mode

PIN DESCRIPTION

60-Pin Flat Pack	68-Pin PLCC	Symbol	Description
1	62	DGND	Digital Ground, 0V, Ground return for all input and output logic.
2	63	$\overline{TEST}$	Input HIGH—Normal operation, Input LOW—Force all bits high. (For test purposes only.)
3	64	INT/$\overline{EXT}$	Oscillator Select: Input HIGH—Select Crystal Oscillator Input LOW—Select External Oscillator Input
4	65	OSC_1	Crystal or Clock input
5	66	OSC_0	Crystal
6	67	SYSCLK	System Clock—buffered system clock output
7	68	FS_0	Conversion Rate (Bit 0)
8	1	FS_1	Conversion Rate (Bit 1)
9	2	SIP	Signal Integrate Phase
10	3	RUN/$\overline{HOLD}$	Run or Hold: Input HIGH—Performs continuous conversions, Input LOW—Converter will stop in Auto-Zero.
11	4	SGL/$\overline{DIF}$	Analog Mux Mode: Input HIGH—Select 8 Channel, Single-ended, Input LOW—Select 4 Channel, Differential.
12	5	$\overline{WE}$	Write Enable: Input HIGH—Multiplexer Address Write Disabled, Input LOW—Multiplexer Address Write Enabled
13	6	$\overline{WR}$	Write: Input HIGH—Multiplexer Address Latched, Input LOW—Multiplexer Address Enabled
14	7	$\overline{RST}$	Reset Latch: Input HIGH—Multiplexer Enabled, Input LOW—Multiplexer Disabled
15	8	A_2	Analog Multiplexer Address (Bit 2, Latchable)
16	11	A_1	Analog Multiplexer Address (Bit 1, Latchable)
17	12	A_0	Analog Multiplexer Address (Bit 0, Latchable)
18	13	EN	Analog Multiplexer Enable (Address Qualifier, Latchable)
19	14	V–	Negative Supply Voltage
20	15	CH8+/CH4–	Analog High (Chan. 8)/Analog Low (Chan. 4)
21	16	CH7+/CH3–	Analog High (Chan. 7)/Analog Low (Chan. 3)
22	17	CH6+/CH2–	Analog High (Chan. 6)/Analog Low (Chan. 2)
23	18	CH5+/CH1–	Analog High (Chan. 5)/Analog Low (Chan. 1)
24	19	$V_{IN}-$	Mux Out/Analog in (Low)
25	20	ANALOG COMMON	Internal ground reference for analog circuits
26	21	$V_{IN}+$	Mux Out/Analog In (High)
27	22	CH4+	Analog High (Chan. 4)
28	23	CH3+	Analog High (Chan. 3)
29	24	CH2+	Analog High (Chan. 2)
30	25	CH1+	Analog High (Chan. 1)
31	28	$V_{REF}+$	Reference Voltage High
32	29	$C_{REF}+$	Reference Capacitor High
33	30	$C_{REF}-$	Reference Capacitor Low
34	31	$V_{REF}-$	Reference Voltage Low
35	32	BUF_{IN}	Buffer Input
36	33	BUF_{OUT}	Buffer Output
37	34	C_{AZ}	Auto Zero Capacitor

TC804

PIN DESCRIPTION (Cont.)

60-Pin Flat Pack	68-Pin PLCC	Symbol	Description
38	35	V_{INT}	Integrator Output
39	36	V+	Positive Supply Voltage
40	37	REF_{OUT}	Reference Output
41	38	DRQST	Data Request, Input [2]
42	39	$\overline{OE}$	Output Enable, Input[1]/Output[2]
43	40	$\overline{LBEN}$	Low Byte Enable, Input[1]/Output[2]
44	41	$\overline{HBEN}$	High Byte Enable, Input[1]/Output[2]
45	42	MODE	Mode Select, Input: LOW—Direct Output Mode[1] HIGH—Hand Shake Mode[2]
46	45	STATUS	Status Bit, Output: HIGH during Integrate and Deintegrate until data is latched, LOW during Auto-Zero and Integrate-Zero
47	46	POL	Polarity Bit, Output: HIGH—Positive, LOW—Negative
48	47	OR	Over Range Bit, Output: HIGH—Overrange, LOW—Non-Overrange
49	48	B_{12}	Data Bit 12 (Most Significant Data Bit)
50	49	B_{11}	Data Bit 11
51	50	B_{10}	Data Bit 10
52	51	B_9	Data Bit 9
53	52	B_8	Data Bit 8 (STATUS in High Byte of 8-bit BUS Mode. See Text)
54	53	B_7	Data Bit 7
55	54	B_6	Data Bit 6
56	55	B_5	Data Bit 5
57	56	B_4	Data Bit 4
58	57	B_3	Data Bit 3
59	58	B_2	Data Bit 2
60	59	B_1	Data Bit 1, (Least Significant Bit)

NOTES: 1. Direct Output Mode (MODE = 0)
2. Handshake Mode (Mode = 1)

MODE SELECTION AND DATA TRANSFER INTERFACING (All pin references are to PLCC package)

The direct output mode is a fully complemented microprocessor interface which can support either an 8 or 16 bit data bus. The microprocessor programming has direct control over the data transfer technique. The status bit (STATUS) from the TC804 supplies the information to the microprocessor to insure proper timing and data handling.

The TC804 will be in the direct output mode as long as the MODE input is LOW. An internal pull-down resistor insures that this is the default mode if it is left unconnected.

When the TC804 is in the indirect mode, OUTPUT ENABLE (OE), LOW BYTE ENABLE (LBEN) and HIGH BYTE ENABLE (HBEN) become inputs. These inputs are then used to control the data transfer. The DATA REQUEST (DRQST) input is not used and should be tied HIGH. (see "DIRECT Interfacing")

Direct Output Mode Data Transfer

The low order byte (bits 1 through 8) and the high order byte (bits 9 through 12 plus the polarity and overrange bits) are accessible under control of OE (pin 38), LBEN (pin 40) and HBEN (pin 41). These three inputs are all active LOW. Internal pullup resistors are provided for an inactive HIGH when left open. A LOW on OE will permit a LOW on input HBEN and/or LBEN to output data to the bus. A LOW on HBEN selects the 6-bit high data byte, a LOW on LBEN selects the 8-bit low data byte and a LOW on both HBEN and LBEN selects the whole 14-bit data word.

The access of data should be synchronized with the conversion cycle by monitoring the STATUS output (pin 45). This will prevent accessing the data while it is being updated. Status can also be read on the B8 output when HBEN is low and LBEN is high.

INTERFACING

Direct Mode

Combinations of chip enable and byte enable control signals which may be used when interfacing the TC804 to parallel data lines are shown in Figure 2. The OE input may be tied low, allowing either byte to be controlled by its own enable (Figure 2A). Figure 2B shows the HBEN and LBEN as flag inputs, and OE as a master enable, which could be the READ strobe available from most microprocessors. Figure 2C shows a configuration where the two byte enables are connected together. The OE is a chip select, and the HBEN and LBEN may be used as a second chip select or connected to ground.

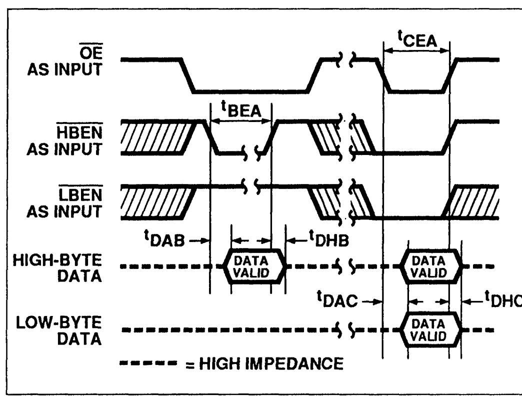


Figure 1 TC804 Direct Mode Output Timing

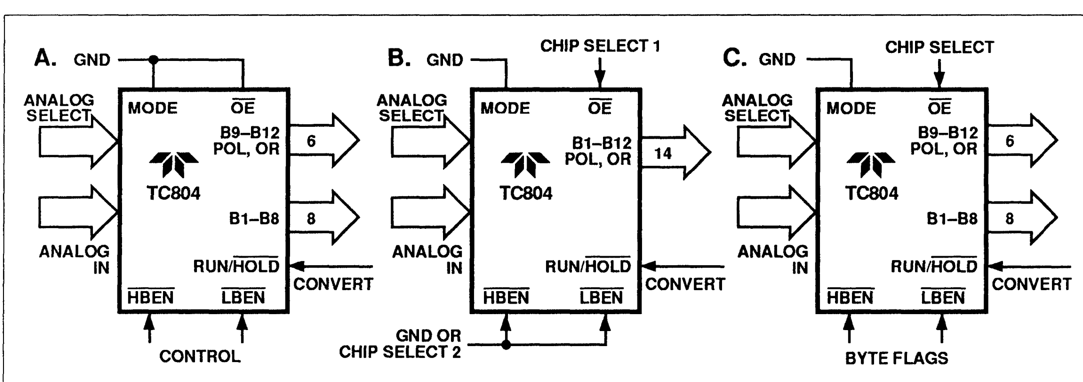


Figure 2 Direct Mode Chip and Byte Enable Combinations

DIRECT MODE TRUTH TABLE

Inputs					Outputs		
MODE	DRQST*	$\overline{OE}$	$\overline{LBEN}$	$\overline{HBEN}$	STATUS	B_1–B_8	B_9–B_{12}, OR, POL
0	1	1	X	X	1	high Z	high Z
0	1	0	0	0	0	low byte	high byte
0	1	0	1	0	0	high Z**	high byte
0	1	0	0	1	0	low byte	high Z
0	1	X	1	1	0	high Z	high Z

*DRQST should be tied high.

**Output B8 is active, and reflects the converter status. This permits the status to be monitored without requiring a separate μP input pin for the STATUS output (pin 45).

Table 1. TC804 Direct Mode Timing Requirements

Symbol	Description	Min	Typ	Max	Units
t_{BEA}	Byte Enable Width	200	500		ns
t_{DAB}	Data Access Time From Byte Enable		150	300	ns
t_{DHB}	Data Hold Time From Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	300	500		ns
t_{DAC}	Data Access Time From Chip Enable		200	400	ns
t_{DHC}	Data Hold Time From Chip Enable		200	400	ns

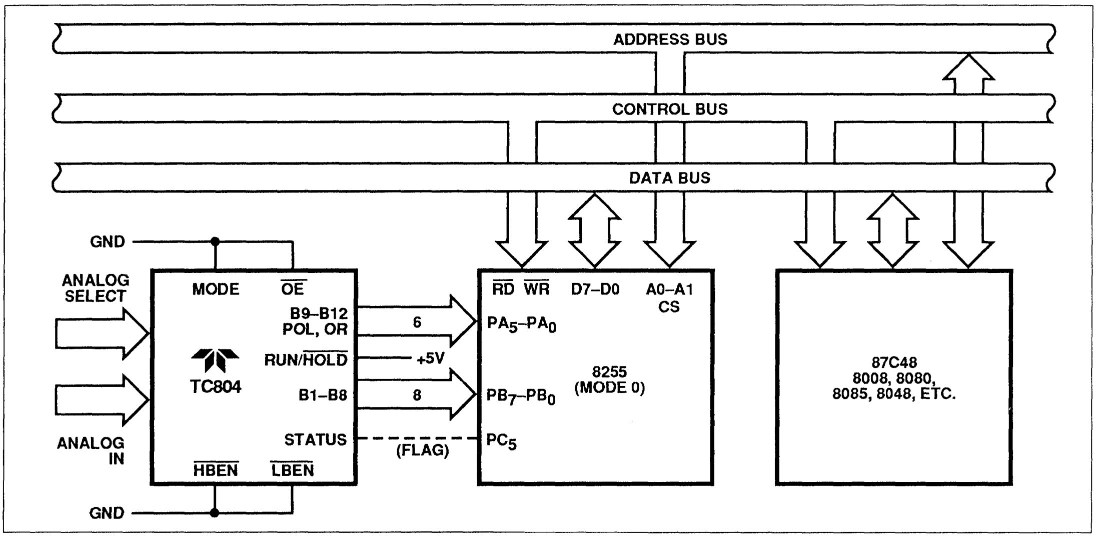


Figure 3 Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputer

Handshake Mode (MODE = 1 or $\sqcap$)

The handshake mode is an alternative means of interfacing the TC804 to digital systems. It provides a means for having the TC804 become active in controlling the flow of data. This mode allows a direct interface between the TC804 and standard UART's with no external logic required. The TC804 provides all the control and flag signals necessary to sequence the data into the UART and initiate the serial transmission.

The handshake mode is activated when the MODE input pin is held high. The data transfer sequence is started at the end of the conversion cycle and after new data has been stored in the output latches.

The data transfer sequence may also be initiated at any time during the conversion cycle by a positive going pulse applied to the MODE pin. If the low to high transition occurs while new data is being stored, the entry into the handshake mode is delayed until the data is stable.

Whenever the handshake mode has been activated, OUTPUT ENABLE ($\overline{OE}$), LOW BYTE ENABLE ($\overline{LBEN}$) and HIGH BYTE ENABLE ($\overline{HBEN}$) become outputs. These outputs are then used to "talk to" the UART. The DATA REQUEST (DRQST) input is used by the UART to transfer data. (see "UART Interfacing")

Handshake Mode Data Transfer

The TC804 actively controls the data transfer to peripherals through the handshake data transfer mode. In this mode, $\overline{OE}$ (pin 38), $\overline{LBEN}$ (pin 40) and $\overline{HBEN}$ (pin 41) are each TTL compatible outputs. A LOW on $\overline{OE}$ signals that valid data is available for the peripheral. A LOW on $\overline{HBEN}$ or $\overline{LBEN}$ indicates which data byte is being transferred. A HIGH input to the TC804 on DRQST (pin 38) initializes the data transfer. The high byte is transferred first followed by the low byte. Data DRQST may be taken LOW to delay the transfer between data bytes.

Handshake output sequences may be performed on demand by triggering the converter into handshake mode with a low to high edge on the MODE input. A handshake output sequence triggered is shown in Figure 5. The DRQST input is low when the converter enters handshake mode. The whole output sequence is controlled by the DRQST input, and the sequence for the first (high order) byte is similar to the sequence for the second byte.

These diagrams also show that the output sequence can take longer than a conversion cycle. New data will not be latched when the handshake mode is still in progress and is therefore lost.

HANDSHAKE MODE TRUTH TABLE

Inputs		Outputs					
MODE[1]	DRQST	$\overline{OE}$[2]	$\overline{LBEN}$	$\overline{HBEN}$	STATUS	B_1–B_8	B_9–B_{12}, OR, POL
1	0	1	1	1	1	high Z	high Z
X	1	⎍	1	0	0	high Z	high byte
X	0	1	1	0	0	High Z	high byte
X	1	⎍	0	1	0	low byte	high Z
X	1	1	1	1	0	high Z	high Z

NOTES: 1. MODE pulsed high or held high
2. Data strobe

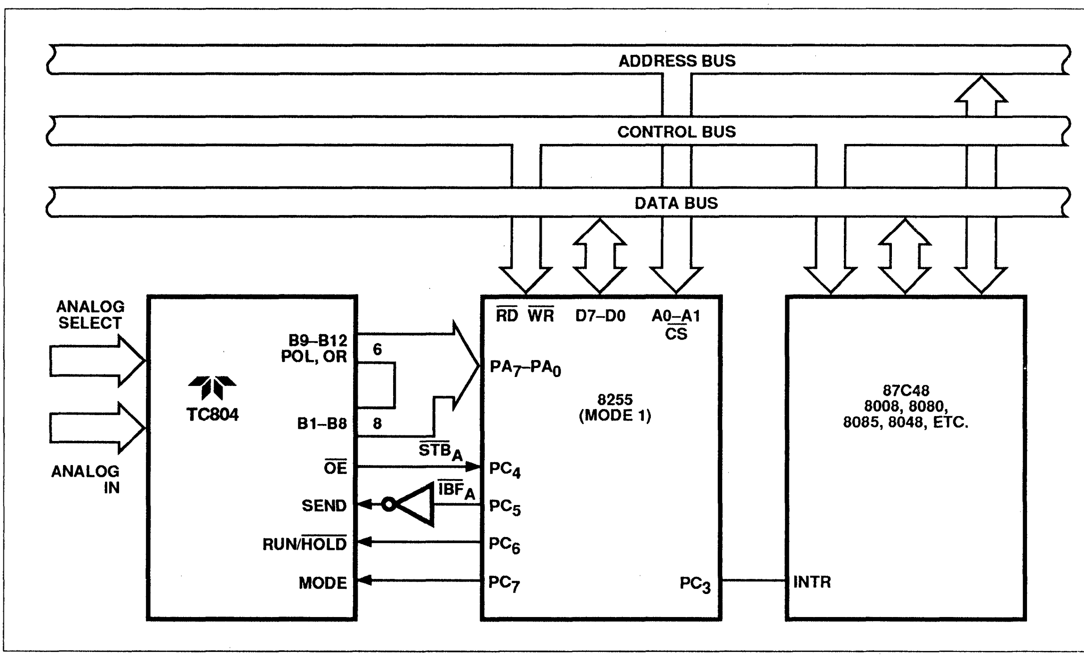


Figure 4 Handshake Interface—TC804 to MCS-48, -80, -85

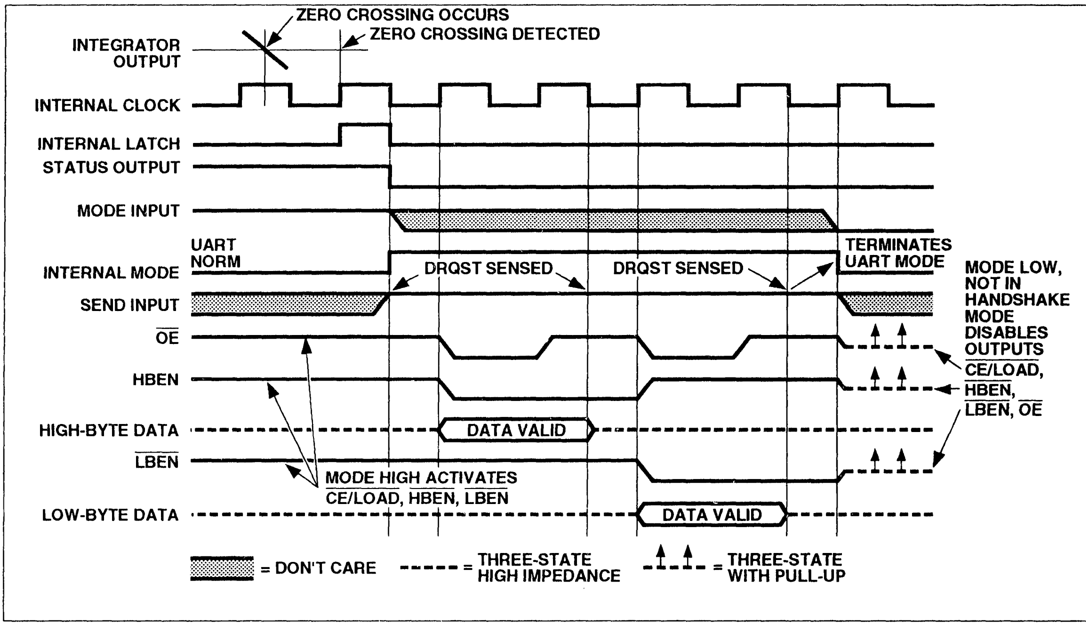


Figure 5 TC804 Handshake with DRQST Input Held Positive

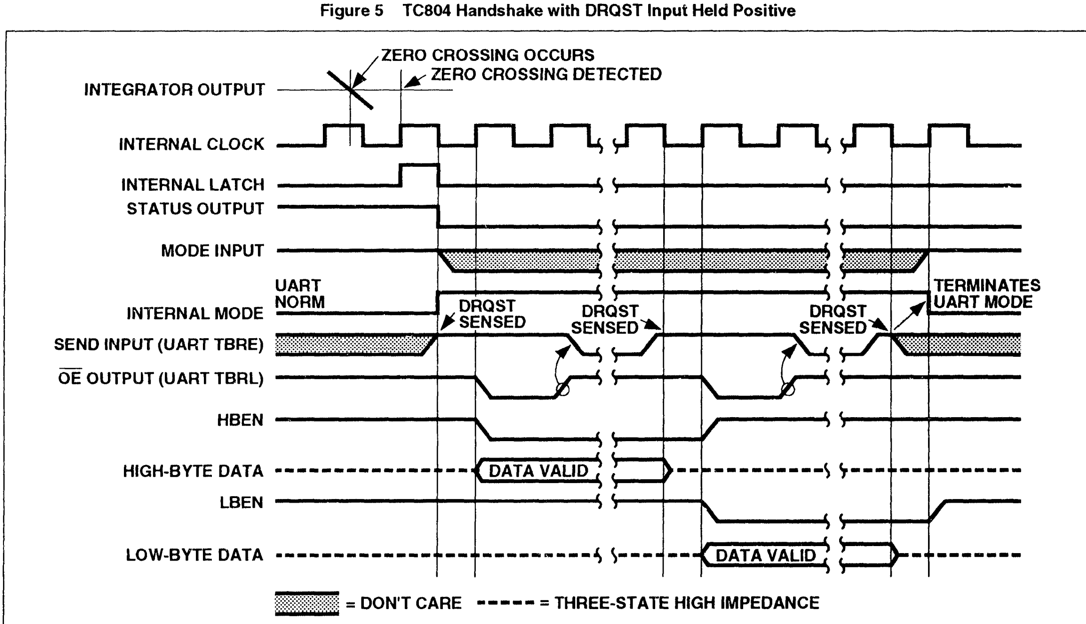


Figure 6 TC804 Handshake—Typical UART Interface Timing

TC804 ANALOG MULTIPLEXER

The on-board analog multiplexer can be configured for eight channel, single-ended input or for four channel, differential input. The signal/differential input (SIG/$\overline{DIF}$) selects the configuration. The eight channel mode is selected when SIG/$\overline{DIF}$ (pin 4) is tied HIGH and the four channel mode is selected when SIG/$\overline{DIF}$ is tied LOW. Either mode of operation permits both latched and transparent addressing.

A LOW on the reset input ($\overline{RST}$) or writing a low into the enable input (EN) opens all (4 or 8) channels which permits direct input through the dedicated analog inputs (V_{IN}+ and V_{IN}–). An external analog multiplexer may be used instead of the internal multiplexer or in conjunction with it. (See "Analog Multiplexer Expansion").

ANALOG MULTIPLEXER TRUTH TABLE

SGL/$\overline{DIF}$	$\overline{WE}$	$\overline{WR}$	$\overline{RST}$	EN	A_2	A_1	A_0	Converter Input		Note
X	X	X	0	X	X	X	X	V_{IN}+	V_{IN}–	(1)
X	0	0	X	0	X	X	X	V_{IN}+	V_{IN}–	(1)
X	X	1	1	X	X	X	X	no change		(2)
X	1	X	1	X	X	X	X	no change		(2)

X = don't care

NOTES: 1. Analog multiplexer disables. V_{IN}+ and V_{IN}– are inputs to the A/D converter.
2. Analog channel address is latched. V_{IN}+ and V_{IN}– are the outputs of the multiplexer as well as the inputs to the A/D converter. The multiplexer channel selection cannot be changed if either $\overline{WE}$ or $\overline{WR}$ is HIGH.

EIGHT CHANNEL OPERATION (SGL/$\overline{DIF}$ = 1)

Each of the single-ended inputs is referenced to V_{IN}– and must comply with the same common-mode input.

SGL/$\overline{DIF}$	$\overline{WE}$	$\overline{WR}$	$\overline{RST}$	EN	A_2 A_1 A_0	Converter Input	
1	0	0	1	1	3-bit address	CHN+	V_{IN}–
1	0	$\uparrow$	1	1	3-bit address	CHN+	V_{IN}–
1	$\uparrow$	0	1	1	3-bit address	CHN+	V_{IN}–

N = 1 thru 8 (A_0, A_1, A_2)

FOUR CHANNEL OPERATION (SGL/$\overline{DIF}$ = 0)

Bit 3 of the multiplexer address (A_2) has no function when the four channel mode is selected. Each input is independently differential and may have different common-mode offsets.

SGL/$\overline{DIF}$	$\overline{WE}$	$\overline{WR}$	$\overline{RST}$	EN	A_2	A_1 A_0	Converter Input	
0	0	0	1	1	X	2-bit address	CHN+	CHN–
0	0	$\uparrow$	1	1	X	2-bit address	CHN+	CHN–
0	$\uparrow$	0	1	1	X	2-bit address	CHN+	CHN–

X = don't care, N = 1 thru 4 (A_0, A_1)

ANALOG MULTIPLEXER ADDRESSING (all pin references are to PLCC package)

Single-Ended/Differential (SIG/$\overline{\text{DIF}}$, pin 4)

If SIG/$\overline{\text{DIF}}$ is HIGH then the 8-channel, single-ended mode is selected. If SIG/$\overline{\text{DIF}}$ is LOW then the 4-channel, differential mode is selected.

The analog multiplexer has an internal address demultiplexer which is configured as either a "2 of 8" for 4-channel operation or as a "1 of 8" for 8-channel operation.

Write ($\overline{\text{WR}}$, pin 6)

The $\overline{\text{WR}}$ input may be held LOW in order to employ transparent address operation. In transparent operation, the multiplexer switches respond directly to the inputs on the address lines (A_0, A_1, A_2) and Enable input (EN, pin 13).

The "latched" mode is entered whenever $\overline{\text{WR}}$ goes HIGH. The inputs on the address lines have no effect on the multiplexer switches until $\overline{\text{WR}}$ is pulsed LOW. These address lines may now be used for another purpose.

Write Enable ($\overline{\text{WE}}$, pin 5)

The $\overline{\text{WE}}$ input must be LOW in order for the $\overline{\text{WR}}$ input to be enabled. The $\overline{\text{WE}}$ and $\overline{\text{WR}}$ inputs are AND'ed internally.

Enable (EN, pin 13)

The EN input is like an address input in that it may also be latched in by a LOW to HIGH transition on the $\overline{\text{WR}}$ input.

Reset ($\overline{\text{RST}}$, pin 7)

The $\overline{\text{RST}}$ input overrides all other inputs to the analog multiplexer. All of the multiplexer switches are open whenever $\overline{\text{RST}}$ is LOW.

ANALOG MULTIPLEXER EXPANSION

The analog multiplexer section of the TC804 may be expanded by using an external multiplexer either in conjunction with, or instead of, the internal multiplexer.

The external multiplexer may be selected at any time when the internal multiplexer is disconnected:

A LOW on the $\overline{\text{RST}}$ input or writing a logic LOW into the enable bit (EN, $\overline{\text{WR}}$, and $\overline{\text{WE}}$ are LOW) will disconnect the internal multiplexer output from the analog input to the TC804 converter.

If an external analog multiplexer is to be used alone then $\overline{\text{RST}}$ should be tied LOW. If an external analog multiplexer is to be used in conjunction with the on-board multiplexer, EN should be used to switch between multiplexers.

ANALOG SECTION (all pin references are to PLCC package)

The analog section of the TC804 will perform conversions at a rate determined by the clock frequency and the inputs to the Conversion Rate Selection (bit 0, pin 7 and bit 1, pin 8). (See Conversion Rate table page 20).

Each measurement cycle is divided into four phases. They are: 1) Auto-Zero (AZ), 2) Signal Integrate (INT), 3) Reference Deintegrate (DE) and 4) Zero Integrate (ZI).

1) Auto-Zero

The Auto-Zero phase has a duration of from 2048 to 6144 counts. During this phase, the analog input signal and reference voltage are disconnected from the analog section. The Auto-Zero capacitor (C_{AZ}) is charged to a value which represents the total system offsets. The charge on C_{AZ} will then be used to compensate the input during the signal integrate (INT) and the reference deintegrate (DE) phases.

This phase is also used to charge the reference capacitor (C_{REF}) to the value of the reference voltage.

2) Signal Integrate

The Signal Integrate phase is selected for 2048 counts (Integrate Count). During this phase, the analog input signal is connected to the input of the buffer amplifier. The integrating amplifier will charge the integrate capacitor (C_{INT}) at a rate determined by the value of the input signal.

At the end of the signal integrate phase, the voltage on C_{INT} will be equal to:

$$V_{INT} = V_{IN} \times \frac{\text{Integrate Count} \times f_{CLOCK}}{R_{INT} \cdot C_{INT}} \quad \text{(equ 1)}$$

3) Reference Deintegrate

The length of the Reference Deintegrate phase is determined by the absolute value of the voltage on C_{INT} at the end of the Signal Integrate phase, (i.e. V_{INT}). The reference capacitor (C_{REF}) is connected to the input of the buffer amplifier in the opposite phase of the input signal. The integrating amplifier will then cause the integrate capacitor (C_{INT}) to start discharging at a constant rate. This rate is determined by the value of the reference voltage. The 12-bit counter counts clock pulses during this phase and stops when C_{INT} is fully discharged (i.e. zero-crossing).

The final count of the 12-bit counter is the binary value of the input signal and is equal to:

$$\text{Deintegrate Count} = \frac{V_{INT}}{V_{REF}} \times \frac{R_{INT} \cdot C_{INT}}{f_{CLOCK}} \quad \text{(equ 2)}$$

4) Zero Integrate

The Zero-Integrate phase is invoked only when an overrange has occurred. It has a duration of up to 1024 counts. This phase is used to completely discharge C_{AZ} and C_{INT} prior to the Auto-Zero phase. This insures that there is no residual charge on either capacitor which may cause a false auto-zero.

Dual Slope Conversion Equation
(combine equ 1 and equ 2)

$$\text{Deintegrate Count} = \frac{V_{IN}}{V_{REF}} \times \text{Integrate Count}$$

DETAILED DESCRIPTION

Analog Section

The Functional Diagram shows a block diagram of the Analog Section of the TC804. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle), when the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V+. Each measurement cycle is divided into four phases as shown in Figure 8. They are: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), (3) Reference Deintegrate (DE), and (4) Zero Integrator (ZI).

Auto-Zero Phase (AZ)

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. The offset referred to the input is less than 10μV.

Signal Integrate Phase (SI)

The buffer and integrator inputs are removed from COMMON and connected to input high and input low. The auto-zero loop is opened. The auto-zero capacitor is placed in series in the loop to provide an equal and opposite compensating offset voltage. The differential voltage between input high and input low is integrated for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined. If the input signal has no return to the converter power supply, input low can be tied to analog common to establish the correct common-mode voltage.

De-Integrate Phase (DI)

Input high is connected across the previously charged reference capacitor and input low is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established by AUTO-ZERO) with a fixed slope. The time, represented by the number of clock periods counted for the output to return to zero, is proportional to the input signal.

Zero-Integrator Phase (ZI)

The ZI phase only occurs when an input overrange condition exists. The function of the ZI phase is to eliminate residual charge on the integrator capacitor after an overrange measurement. Unless removed, the residual charge will be transferred to the auto-zero capacitor and cause an error in the succeeding conversion.

The ZI phase virtually eliminates hysteresis or "cross talk" in multiplexed systems. An overrange input on one channel will not cause an error on the next channel measured. This feature is especially useful in thermocouple measurements, where unused (or broken thermocouple) inputs are pulled to the positive supply rail.

During ZI, the reference capacitor is charged to the reference voltage. The signal inputs are disconnected from the buffer and integrator. The comparator output is connected to the buffer input, causing the integrator output to be driven rapidly to 0V (Figure 8). The ZI phase only occurs following an overrange and lasts for a maximum of 1024 clock periods.

Differential Input

The TC804 has been optimized for operation with analog-common near digital ground. With +5V and –5V power supplies, a full ±4V full-scale integrator swing maximizes the analog section's performance.

A typical CMRR of 86dB is achieved for input differential voltages anywhere within the typical common-mode range of 1.0 Volts below the positive supply to 1.5 Volts above the negative supply. However, for optimum performance the $V_{IN}+$ and $V_{IN}-$ inputs should not come within 2V of either supply rail. Since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator does not saturate. A worst case condition is near a full-scale negative differential input voltage with a large positive common-mode voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. In such cases, the integrator swing can be reduced to less than the recommended ±4V full-scale value, with some loss of accuracy. The integrator output can swing to within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. Rollover voltage is the main source of common-mode error. It is caused by the reference capacitor losing or gaining charge due to stray capacity on its nodes. With a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called upon to deintegrate a positive signal and lose charge (decrease voltage) when called upon to deintegrate a negative input signal. This difference in reference for (+) or (–) input voltage will cause a roll-over error. This error can be held to less than 0.5 count worst case by using a large reference capacitor in comparison to the stray capacitance. To minimize roll-over error from these above sources keep the reference common-mode voltage near or at analog common.

Digital Section

The digital section is shown in the block diagram, (Figure 9), and includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, UART handshake logic, polarity, overrange and control logic.

Inputs driven from TTL gates should have 3–5KΩ pull-up resistors added for maximum noise immunity. For minimum power consumption, all inputs should swing from GND (low) to V+ (high).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 8. The signal may be used as a "data valid" flag to drive interrupts, or for monitoring the status of the converter. (Data will not change while STATUS is low). Status is also output on Data Bit 8, when the TC804 is in direct mode (Mode = 0, $\overline{\text{LBEN}}$ = 1, $\overline{\text{HBEN}}$ = 0).

MODE Input

The output mode of the converter is controlled by the MODE Input. The converter is in its "Direct" output mode, when the MODE pin is low or left open. The output data is directly accessible under the control of the chip and byte enable inputs (this input is provided with a pull-down resistor to ensure a low level when the pin is left open). When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is kept high, the converter will output data in the handshake mode at the end of every conversion cycle. With MODE = 0 (Direct BUS Transfer) the DRQST input should be tied to V+. (See Handshake Mode Section).

RUN/$\overline{\text{HOLD}}$ Input

With RUN/$\overline{\text{HOLD}}$ high or open, the circuit operates normally as a dual slope A/D as shown in Figure 8. Conversion cycles operate continuously with the output latches updated after zero crossing in the deintegrate mode. An internal pull-up resistor is provided to insure a high level with an open input.

The RUN/$\overline{\text{HOLD}}$ may be used to shorten conversion time. If the RUN/$\overline{\text{HOLD}}$ goes low at anytime after zero crossing in the de-integrate mode, the circuit will jump to auto-zero and eliminate that portion of time normally spent in de-integrate.

If RUN/$\overline{\text{HOLD}}$ stays or goes low the conversion will complete with minimum time in de-integrate. It will stay in auto-zero for the minimum time and wait in auto-zero for a high in the RUN/$\overline{\text{HOLD}}$ input. As shown in Figure 10, the STATUS output will go high seven clock periods after RUN/$\overline{\text{HOLD}}$ is changed to high, and the converter will begin the integrate phase of the next conversion.

The RUN/$\overline{\text{HOLD}}$ input allows controlled conversion interface. The converter may be held at idle in auto-zero with RUN/$\overline{\text{HOLD}}$ low. The conversion is started when RUN/$\overline{\text{HOLD}}$ goes high and the new data is valid when the STATUS output goes low (or is transferred to the UART—see Handshake Mode). Run/$\overline{\text{HOLD}}$ may now go low, terminating deintegrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion. Conversion time can be minimized by ensuring RUN/$\overline{\text{HOLD}}$ goes low during deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the Buffered Oscillator output. In this mode, the input value measured determines the conversion time.

Signal Integrate Phase (SIP) Output

The SIP output is high when the TC804 is in the Signal integrate phase of a conversion. SIP should be used to control multiplexer address changes. The falling edge of SIP indicates that the TC804 has completed signal integration for the current conversion cycle, and that the analog input can be changed. Changing the multiplexer address on the falling edge of SIP will guarantee maximum analog input signal settling time before the next conversion.

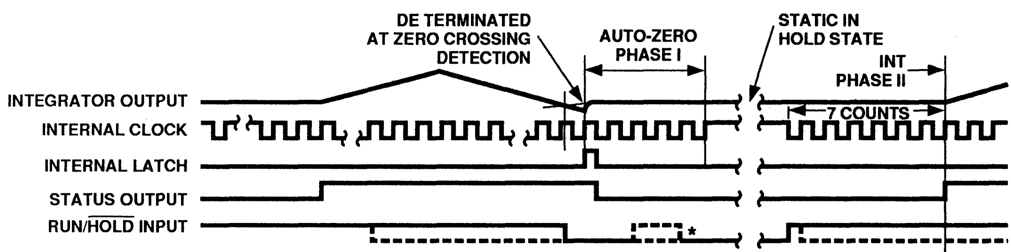
Oscillator

The TC804 is designed to operate with an internal crystal oscillator or with an external clock. The oscillator mode is selected with the INT/$\overline{\text{EXT}}$ input. A programmable divider permits control of the conversion rate, using hardware or software, over a range of 8 to 1.

For external oscillator operation, the INT/$\overline{\text{EXT}}$ input is connected to DGND. The external oscillator is connected to the OSC1 input, as shown in Figure 10. The oscillator signal should swing from DGND to V+. The ADC system clock frequency will be the oscillator frequency divided by the value selected by the frequency select divider.

Connecting INT/$\overline{\text{EXT}}$ to V+ enables the internal crystal oscillator. Two on-chip capacitors and a feedback device are added to the oscillator, as shown in Figure 11. A crystal is then connected to the OSC1 and OSC0 inputs. In this configuration, the oscillator will operate with most crystals in the 1 to 5 MHz range.

The conversion rate is pin programmable, using the FS0 and FS1 inputs. The frequency select divider will divide the oscillator frequency by 2, 4, 8 or 16. The buffered ADC system clock is available at the SYSCLK output. Divider values can be hard-wired or jumper selected, or can be controlled by software via two bits of a µP output port. The divider truth table is shown in Figure 12.



***NOTE:** RUN/$\overline{\text{HOLD}}$ input is ignored until end of auto-zero phase.

Figure 7 TC804 RUN/HOLD Operation

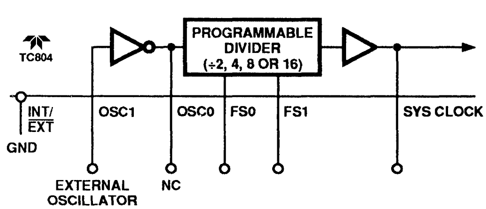


Figure 10 External Oscillator Connection

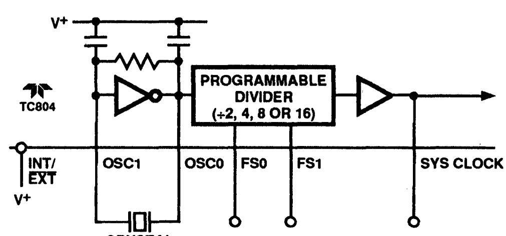


Figure 11 TC804 Crystal Oscillator

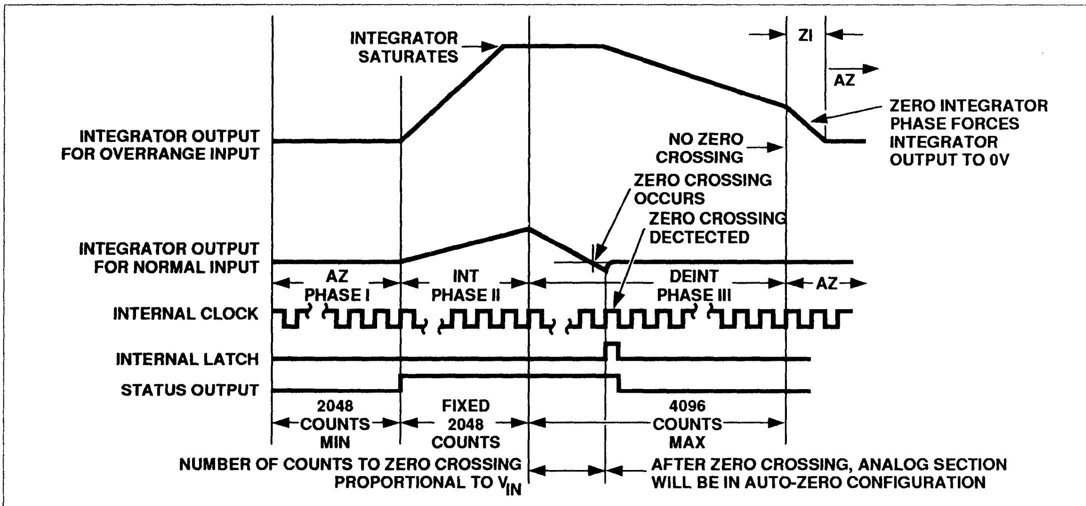


Figure 8 Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

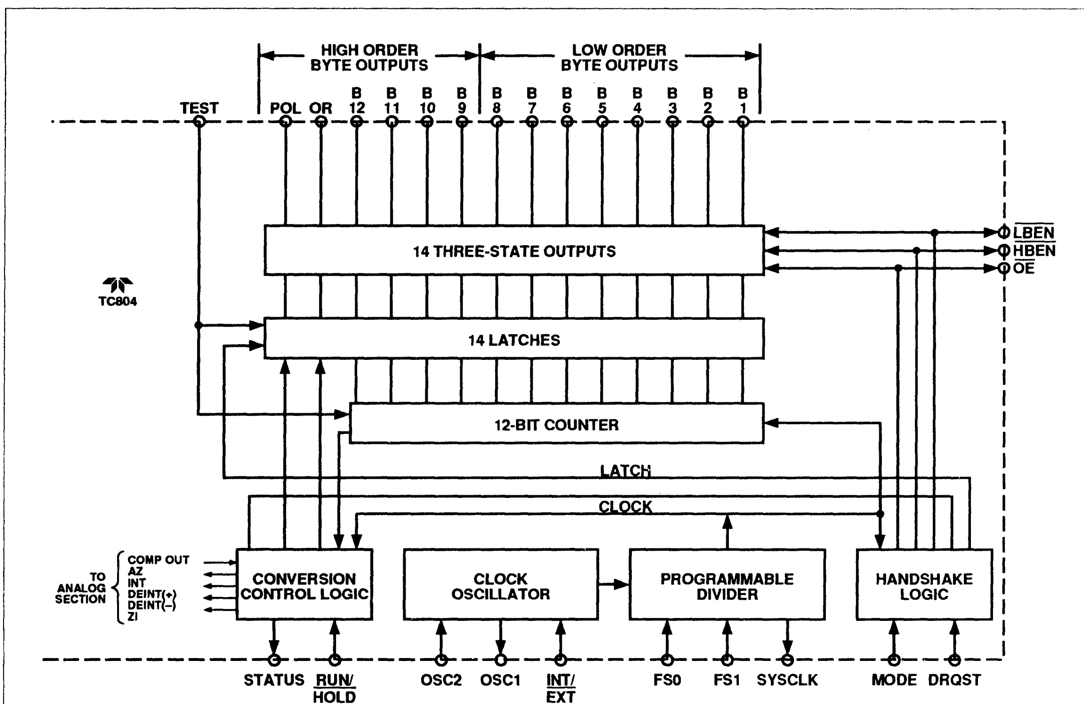


Figure 9 Digital Section

Test Input

The counter and its outputs may be tested easily. When the TEST input is connected to DGND, the internal clock is disabled, and the counter outputs are all forced into the high state. When the input returns to the 1/2 (V+ – DGND) voltage or to V+ and one clock is input, the counter outputs will all be clocked to the low state.

The counter output latches are enabled when the TEST input is taken to a level halfway between V+ and DGND allowing the counter contents to be examined anytime.

Component Value Selection

The integrator output swing for full-scale should be as large as possible. For example, with ±5V supplies and ANALOG COMMON connected to DGND, the nominal integrator output swing at full-scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly effecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common-mode voltage range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For large common-mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, ±6V supplies may be used.

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing that will not saturate the integrator to within 0.3V from either supply. A ±3.5V to ±4V integrator output swing is nominal for the TC804 with ±5V supplies and ANALOG COMMON connected to DGND. For 7-1/2 conversions per second (61.72Hz internal clock frequency) nominal values C_{INT} and C_{AZ} are 0.15µF and 0.33µF, respectively. These values should be changed if different clock frequencies are used to maintain the integrator output voltage swing. The value of C_{INT} is given by:

$$C_{INT} = \frac{(2048 \times \text{Clock Period})\ (20\mu A)}{\text{Integrator Output Voltage Swing } (V_{INT})}$$

Integrating Converter Features

The output of integrating A/D converters represents the integral or average of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter will average the effects of noise. A second important characteristic is that time is used to quantise the answer, resulting in extremely small non-linearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise. (Figure 13.)

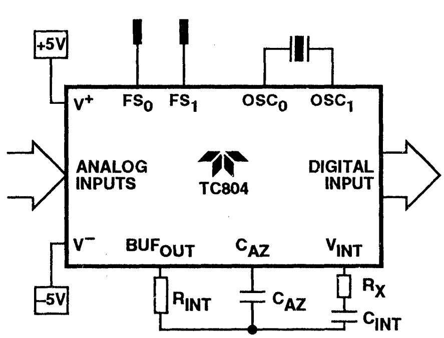


Figure 12 Recommended Component Values for VFS = 409.6mV. (See Table Following Page.)

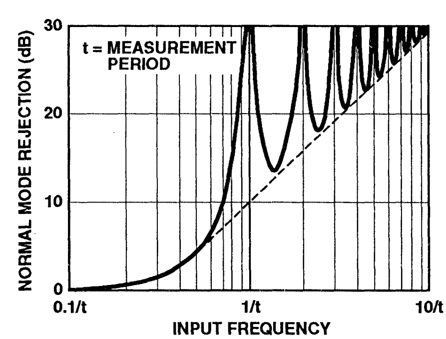


Figure 13 Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency.

Conversion Rate	FS_1	FS_0	R_{INT}	C_{AZ}	C_{INT}	R_X
60 Conv/Sec	0	0	24K	.033μ	.015μ	50Ω
30 Conv/Sec	0	1	24K	.068μ	.033μ	50Ω
15 Conv/Sec	1	0	24K	0.15μ	.068μ	50Ω
7.5 Conv/Sec	1	1	20K	0.33μ	0.15μ	0Ω

Multiply RINT by ≈50 for VFS = 2.048V.

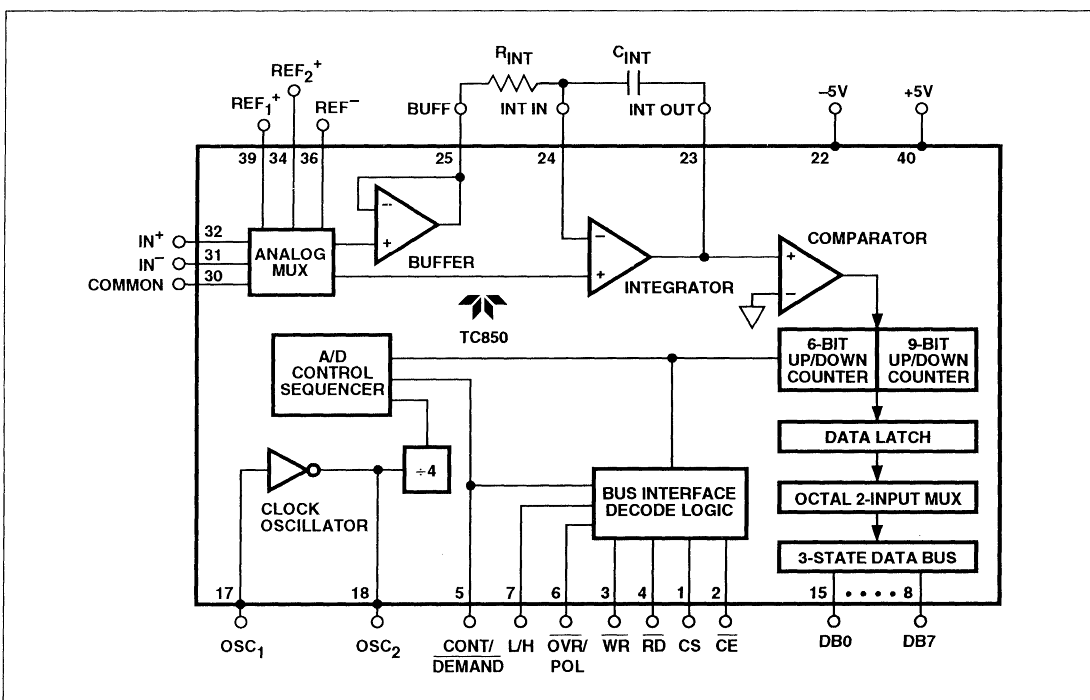
NOTES

15-BIT, FAST-INTEGRATING CMOS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 15-bit Resolution Plus Sign Bit
- Up to 40 Conversions per Second
- 12 Conversions per Second Guaranteed
- Integrating ADC Technique
  - — Monotonic
  - — High Noise Immunity
  - — Auto-Zeroed Amplifiers Eliminate Offset Trimming
- Wide Dynamic Range .... 96 dB
- Low Input Bias Current .... 30 pA
- Low Input Noise .... 30 μV_{P-P}
- Sensitivity .... 100 μV
- Flexible Operational Control
  - — Continuous or On-Demand Conversions
  - — Data Valid Output
- Bus Compatible, 3-State Data Outputs
  - — 8-Bit Data Bus
  - — Simple μP Interface
  - — Two Chip Enables
  - — Read ADC Result Like Memory
- ±5V Power Supply Operation .... 20 mW
- 40-Pin Dual-in-Line or 44-Pin PLCC Packages

FUNCTIONAL DIAGRAM



TC850

GENERAL DESCRIPTION

The TC850 is a monolithic CMOS analog-to-digital converter (ADC) with resolution of 15 bits plus sign. It combines a chopper-stabilized buffer and integrator with a unique multiple-slope integration technique that increases conversion speed. The result is 16 times improvement in speed over previous 15-bit, monolithic integrating ADCs (from 2.5 conversions per sec up to 40 per sec). Faster conversion speed is especially welcome in systems with human interface, such as digital scales.

The TC850 incorporates an ADC and a μP-compatible digital interface. Only a voltage reference and a few noncritical passive components are required to form a complete 15-bit plus sign ADC.

CMOS processing provides the TC850 with high-impedance differential inputs. Input bias current is typically only 30 pA, permitting direct interface to sensors. Input sensitivity of 100 μV per least significant bit (LSB) eliminates the need for precision external amplifiers. The internal amplifiers are auto-zeroed, guaranteeing a zero digital output with 0V analog input. Zero adjustment potentiometers or calibrations are not required.

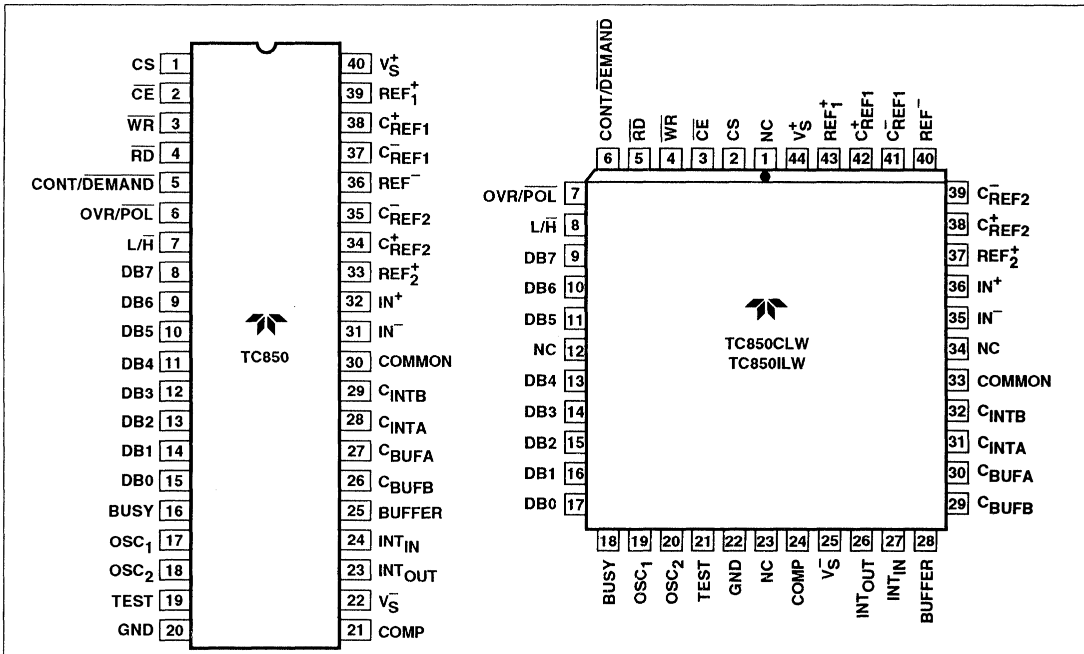
The TC850 outputs data on an 8-bit, 3-state bus. Digital inputs are CMOS compatible; outputs are TTL/CMOS compatible. Chip-enable and byte-select inputs combined with an end-of-conversion output ensures easy interfacing to a wide variety of microprocessors. Conversions can be performed continuously or on command. In continuous mode, data is read as three consecutive bytes and manipulation of address lines is not required.

Operating from ±5V supplies, the TC850 dissipates only 20 mW. It is packaged in 40-pin plastic or ceramic dual-in-line packages (DIPs) and in a 44-pin plastic leaded chip carrier (PLCC), surface-mount package.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC850CLW	44-Pin PLCC	0°C to +70°C
TC850CPL	40-Pin Plastic DIP	0°C to +70°C
TC850ILW	44-Pin PLCC	–25°C to +85°C
TC850IJL	40-Pin CerDIP	–25°C to +85°C

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

15-BIT, FAST-INTEGRATING CMOS ANALOG-TO-DIGITAL CONVERTER

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_S^+ to GND) .... +6V
Negative Supply Voltage (V_S^- to GND) .... –9V
Analog Input voltage (IN^+ or IN^-) .... V_S^+ to V_S^-
Voltage Reference Input
(REF_1^+, REF_1^-, REF_2^+) .... V_S^+ to V_S^-
Logic Input Voltage .... V_S^+ +0.3V to GND –0.3V
Current Into Any Pin .... 10 mA
While Operating .... 100 µA
Ambient Operating Temperature Range
C Device .... 0°C to +70°C
I Device .... –25°C to +85°C

Lead Temperature (Soldering, 10 sec) .... +300°C
Package Power Dissipation
CerDIP .... 1W @ +85°C
Plastic DIP .... 0.5W @ +70°C
Plastic PLCC Package .... 0.5W @ +70°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = ±5V, f_{CLK} = 61.44 kHz, V_{FS} = 3.2768V, T_A = 25°C, Fig. 1 Test Circuit

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Zero-Scale Error	V_{IN} = 0V		±0.25	±0.5	LSB
	End Point Linearity Error	$-V_{FS} \le V_{IN} \le +V_{FS}$	—	±1	±2	LSB
	Differential Nonlinearity		—	±0.1	±0.5	LSB
I_{IN}	Input Leakage Current	V_{IN} = 0V, T_A = 25°C 0°C ≤ T_A ≤ +70°C –25° ≤ T_A ≤ +85°C	— — —	30 — 1.1	75 — 3	pA nA
V_{CMR}	Common-Mode Voltage Range	Over Operating Temperature Range	V_S^- +1.5	—	V_S^+ –1.5	V
CMRR	Common-Mode Rejection Ratio	V_{IN} = 0V, V_{CM} = ±1V	—	80	—	dB
	Full-Scale Gain Temperature Coefficient	External Ref Temperature Coefficient = 0 ppm/°C 0°C ≤ T_A ≤ +70°C	—	2	5	ppm/°C
	Zero-Scale Error Temperature Coefficient	V_{IN} = 0V 0°C ≤ T_A ≤ +70°C	—	0.3	2	µV/°C
	Full-Scale Magnitude Symmetry Error	V_{IN} = ±3.275V	—	0.5	2	LSB
e_N	Input Noise	Not Exceeded 95% of Time	—	30	—	μV_{P-P}
I_S^+	Positive Supply Current		—	2	3.5	mA
I_S^-	Negative Supply Current		—	2	3.5	mA
V_{OH}	Output High Voltage	I_O = 500 µA	3.5	4.9	—	V
V_{OL}	Output Low Voltage	I_O = 1.6 mA	—	0.15	0.4	V
I_{OP}	Output Leakage Current	Pins 8–15, High-Impedance State	—	0.1	1	µA
V_{IH}	Input High Voltage	Note 3	3.5	2.3	—	V
IL	Input Low Voltage	Note 3	—	2.1	1	V
I_{PU}	Input Pull-Up Current	Pins 2, 3, 4, 6, 7; V_{IN} = 0V	—	4	—	µA
I_{PD}	Input Pull-Down Current	Pins 1, 5; V_{IN} = 5V	—	14	—	µA
I_{OSC}	Oscillator Output Current	Pin 18, V_{OUT} = 2.5V	—	140	—	µA
C_{IN}	Input Capacitance	Pins 1–7, 17	—	1	—	pF
C_{OUT}	Output Capacitance	Pins 8–15, High-Impedance State	—	15	—	pF
t_{CE}	Chip-Enable Access Time	CS or $\overline{CE}$, $\overline{RD}$ = Low (Note 1)	—	230	450	ns
t_{RE}	Read-Enable Access Time	CS = High, $\overline{CE}$ = Low (Note 1)	—	190	450	ns
t_{DHC}	Data Hold From CS or $\overline{CE}$	$\overline{RD}$ = Low (Note 1)	—	250	450	ns
t_{DHR}	Data Hold From $\overline{RD}$	CS = High, $\overline{CE}$ = Low (Note 1)	—	210	450	ns
t_{OP}	OVR/$\overline{POL}$ Data Access Time	CS = High, $\overline{CE}$ = Low, $\overline{RD}$ = Low (Note 1)	—	140	300	ns

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{LH}	Low/High Byte Access Time	CS = High, $\overline{CE}$ = Low, $\overline{RD}$ = Low (Note 1)	—	140	300	ns
	Clock Setup Time	Positive or Negative Pulse Width	100	—	—	ns
t_{WRE}	$\overline{RD}$ Minimum Pulse Width	CS = High, $\overline{CE}$ = Low (Note 2)	450	230	—	ns
t_{WRD}	$\overline{RD}$ Minimum Delay Time	CS = High, $\overline{CE}$ = Low (Note 2)	150	50	—	ns
t_{WWR}	$\overline{WR}$ Minimum Pulse Width	CS = High, $\overline{CE}$ = Low, Demand Mode	75	25	—	ns
	Clock Setup Time	Positive or Negative Pulse Width	100			ns

NOTES: 1. Demand mode, CONT/$\overline{DEMAND}$ = low. Figure 10 timing diagram. C_L = 100 pF.
2. Continuous mode, CONT/$\overline{DEMAND}$ = high. Figure 12 timing diagram.
3. Digital inputs have CMOS logic levels and internal pull-up/pull-down resistors. For TTL compatibility, external pull-up resistors to V_{CC} are recommended.

PIN DESCRIPTIONS

40-Pin DIP Pin No.	Symbol	Description
1	CS	Chip select, active high. Logically ANDed with $\overline{CE}$ to enable read and write inputs. (See note 4.)
2	$\overline{CE}$	Chip enable, active low. (See note 5.)
3	$\overline{WR}$	Write input, active low. When chip is selected (CS = high and $\overline{CE}$ = low) and in demand mode (CONT/$\overline{DEMAND}$ = low), a logic low on $\overline{WR}$ starts a conversion. (See note 4.)
4	$\overline{RD}$	Read input, active low. When CS = high and $\overline{CE}$ = low, a logic low on $\overline{RD}$ enables the 3-state data outputs. (See note 5.)
5	CONT/$\overline{DEMAND}$	Conversion control input. When CONT/$\overline{DEMAND}$ = low, conversions are initiated by the $\overline{WR}$ input. When CONT/$\overline{DEMAND}$ = high, conversions are performed continuously. (See note 4.)
6	OVR/$\overline{POL}$	Overrange/polarity data-select input. When making conversions in the demand mode (CONT/$\overline{DEMAND}$ = low), OVR/$\overline{POL}$ controls the data output on DB7 when the high-order byte is active. (See note 5.)
7	L/$\overline{H}$	Low/high byte-select input. When CONT/$\overline{DEMAND}$ = low, this input controls whether low-byte or high-byte data is enabled on DB0 through DB7. (See note 5.)
8	DB7	Most significant data bit output. When reading the A/D conversion result, the polarity, overrange, and DB7 data are output on this pin. (See text.)
9–15	DB6–DB0	Data outputs DB6–DB0. 3-state, bus compatible.
16	BUSY	A/D conversion status output. BUSY goes to a logic high at the beginning of the deintegrate phase and goes low when conversion is complete. The falling edge of BUSY can be used to generate a µP interrupt.
17	OSC_1	Crystal oscillator connection or external oscillator input.
18	OSC_2	Crystal oscillator connection.
19	TEST	For factory testing purposes only. Do not make external connection to this pin.
20	DGND	Digital ground connection.
21	COMP	Connection for comparator auto-zero capacitor. Bypass to V_S^- with 0.1 µF.
22	V_S^-	Negative power supply connection, typically –5V.
23	INT_{OUT}	Output of the integrator amplifier. Connect to C_{INT}.
24	INT_{IN}	Input to the integrator amplifier. Connect to summing node of R_{INT} and C_{INT}.
25	BUFFER	Output of the input buffer. Connect to R_{INT}.
26	C_{BUFB}	Connection for buffer auto-zero capacitor. Bypass to V_S^- with 0.1 µF.
27	C_{BUFA}	Connection to buffer auto-zero capacitor. Bypass to V_S^- with 0.1 µF.
28	C_{INTA}	Connection for integrator auto-zero capacitor. Bypass to V_S^- with 0.1 µF.
29	C_{INTB}	Connection for integrator auto-zero capacitor. Bypass to V_S^- with 0.1 µF.
30	COMMON	Analog common.
31	IN^-	Negative differential analog input.

PIN DESCRIPTIONS

40-Pin DIP Pin No.	Symbol	Description
30	COMMON	Analog common.
33	REF_2^+	Positive input for reference voltage V_{REF2}. ($V_{REF2} = V_{REF1}/64$)
34	C_{REF2}^+	Positive connection for V_{REF2} reference capacitor.
35	C_{REF2}^-	Negative connection for V_{REF2} reference capacitor.
36	REF^-	Negative input for reference voltages.
37	C_{REF1}^-	Negative connection for V_{REF1} reference capacitor.
38	C_{REF1}^+	Positive connection for V_{REF1} reference capacitor.
39	REF_1^+	Positive input for V_{REF1}.
40	V_S^+	Positive power supply connection, typically +5V.

NOTES: 4. This pin incorporates a pull-down resistor to DGND.
5. This pin incorporates a pull-up resistor to V_S^+.

THEORY OF OPERATION

The TC850 is a multiple-slope, integrating analog-to-digital converter (ADC). The multiple-slope conversion process, combined with chopper-stabilized amplifiers, results in a significant increase in ADC speed, while maintaining very high resolution and accuracy.

Dual-Slope Conversion Principles

The conventional dual-slope converter measurement cycle (shown in Figure 2A) has two distinct phases:

(1) Input signal integration

(2) Reference voltage integration (deintegration)

The input signal being converted is integrated for a fixed time period, measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual-slope converter, complete conversion requires the integrator output to "ramp-up" and "ramp-down." Most dual-slope converters add a third phase, auto-zero. During auto-zero, offset voltages of the input buffer, integrator, and comparator are nulled, thereby eliminating the need for zero-offset adjustments.

Dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values, as long as they are stable during a measurement cycle. By converting the unknown analog input voltage into an easily-measured function of time, the dual-slope converter reduces the need for expensive, precision passive components.

Noise immunity is an inherent benefit of the integrating conversion method. Noise spikes are integrated, or averaged, to zero during the integration period. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments.

A simple mathematical equation relates the input signal, reference voltage, and integration time:

$$\frac{1}{RC}\int_0^{t_{SI}} V_{IN}(t)\,dt = \frac{V_R\,t_{RI}}{RC},$$

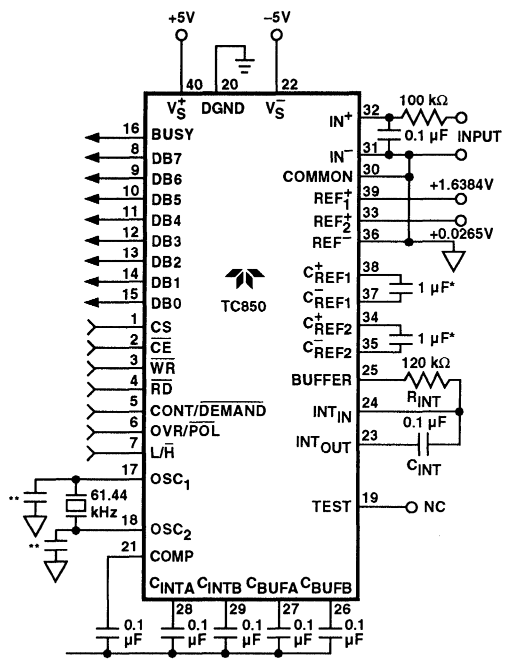
where: V_R = Reference voltage
t_{SI} = Signal integration time (fixed)
t_{RI} = Reference voltage integration time (variable).

Multiple-Slope Conversion Principles

One limitation of the dual-slope measurement technique is conversion speed. In a typical dual-slope method, the auto-zero and integrate times are each one-half of the deintegrate time. For a 15-bit conversion, $2^{14} + 2^{14} + 2^{15}$ (65,536) clock pulses are required for auto-zero, integrate, and deintegrate phases, respectively. The large number of clock cycles effectively limits the conversion rate to about 2.5 conversions per second, when a typical analog CMOS fabrication process is used.

The TC850 uses a multiple-slope conversion technique to increase conversion speed (Figure 2B). This technique makes use of a two-slope deintegration phase and permits 15-bit resolution up to 40 conversions per second.

During the TC850's deintegration phase, the integration capacitor is rapidly discharged to yield a resolution of 9 bits. At this point, some charge will remain on the capacitor. This remaining charge is then slowly deintegrated, producing an additional 6 bits of resolution. The result is 15 bits of resolution achieved with only $2^9 + 2^6$ (512 + 64, or 576) clock pulses for deintegration. A complete conversion cycle occupies only 1280 clock pulses.



NOTES: Unless otherwise specified, all 0.1 µF capacitors are film dielectric. Ceramic capacitors are not recommended.
NC = No internal connection.
* Polypropylene capacitors.
** 100 pF Mica capacitors.

Figure 1 Standard Circuit Configuration

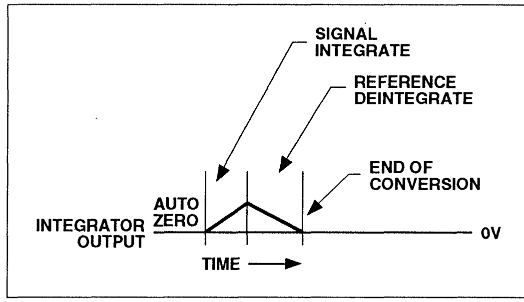


Figure 2A Dual-Slope ADC Cycle

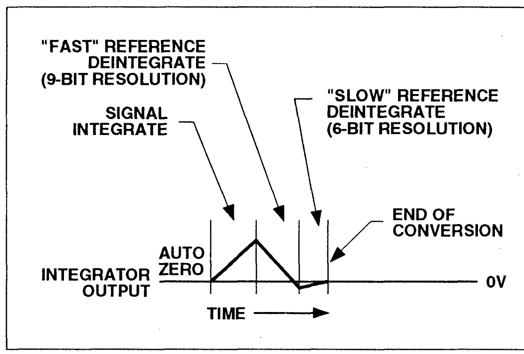


Figure 2B "Fast-Slow" Reference Deintegrate Cycle

In order to generate "fast-slow" integration phases, two voltage references are required. The primary reference (V_{REF1}) is set to one-half of the full-scale voltage (typically V_{REF1} = 1.6384V, and V_{FS} = 3.2768V). The secondary voltage reference (V_{REF2}) is set to $V_{REF1}/64$ (typically 25.6 mV). To maintain 15-bit linearity, a tolerance of 0.5% for V_{REF2} is recommended.

ANALOG SECTION DESCRIPTION

The TC850 analog section consists of an input buffer amplifier, integrator amplifier, comparator, and analog switches. A simplified block diagram is shown in Figure 3.

Conversion Timing

Each conversion consists of three phases: (1) Zero Integrator, (2) Signal Integrate, and (3) Reference Integrate (or Deintegrate). Each conversion cycle requires 1280 internal clock cycles (Figure 4).

Zero-Integrator Phase

During the zero-integrator phase, the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero-input condition. At the same time, a feedback loop is closed around the input buffer, integrator, and comparator. The feedback loop ensures the integrator output is near 0V before the signal-integrate phase begins.

During this phase, a chopper-stabilization technique is used to cancel offset errors in the input buffer, integrator, and comparator. Error voltages are stored on the C_{BUFF}, C_{INT}, and COMP capacitors. The zero-integrate phase requires 246 clock cycles.

Signal-Integrate Phase

The zero-integrator loop is opened and the internal differential inputs are connected to IN^+ and IN^-. The differential input signal is integrated for a fixed time period. The TC850 signal-integrate period is 256 clock periods, or counts. The crystal oscillator frequency is ÷4 before clocking the internal counters.

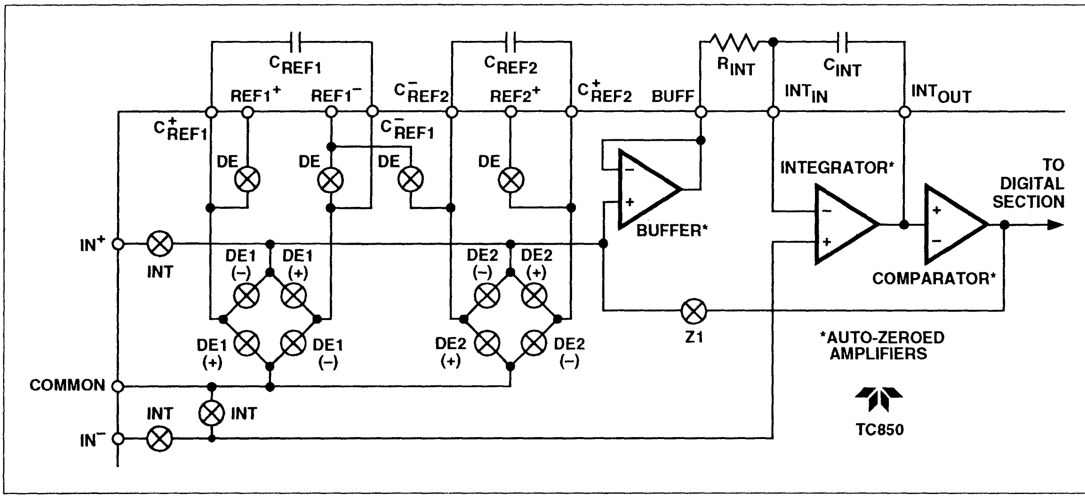


Figure 3 Analog Section Simplified Schematic

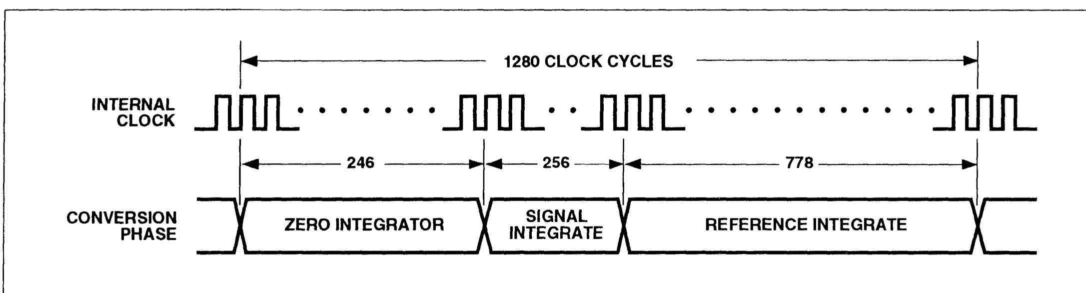


Figure 4 Conversion Timing

The integration time period is:

$$t_{SI} = \frac{4}{f_{OSC}} \times 256$$

Reference-Integrate Phase

During reference-integrate phase, the charge stored on the integrator capacitor is discharged. The time required to discharge the capacitor is proportional to the analog input voltage.

The reference integrate phase is divided into three subphases: (1) fast, (2) slow, and (3) overrange deintegrate.

During fast deintegrate, V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously-charged reference capacitor (C_{REF1}). The integrator capacitor is rapidly discharged for a maximum of 512 internal clock pulses, yielding 9 bits of resolution.

During the slow deintegrate phase, the internal V_{IN}^+ node is now connected to the C_{REF2} capacitor, and the residual charge on the integrator capacitor is further discharged a maximum of 64 clock pulses. At this point, the analog input voltage has been converted with 15 bits of resolution.

If the analog input is greater than full scale, the TC850 performs up to three overrange deintegrate subphases. Each subphase occupies a maximum of 64 clock pulses. The overrange feature permits analog inputs up to 192 LSBs greater than full scale to be correctly converted. This feature permits the user to digitally null up to 192 counts of input offset, while retaining full 15-bit resolution.

In addition to 512 counts of fast, 64 counts of slow, and 192 counts of overrange deintegrate, the reference-integrate phase uses 10 clock pulses to permit internal nodes to settle. Therefore, the reference integrate cycle occupies 778 clock pulses.

Pin Description (Analog)

Differential Inputs (IN^+ and IN^-)

The analog signal to be measured is applied at the IN^+ and IN^- inputs. The differential input voltage must be within the common-mode range of the converter. The input common-mode range extends from V_S^+ −1.5V to V_S^- +1.5V. Within this common-mode voltage range, an 86 dB CMRR is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large, positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its available swing has been used up by the positive common-mode voltage. For applications where maximum common-mode range is critical, integrator swing can be reduced. The integrator output can swing within 0.4V of either supply without loss of linearity.

Differential Reference (V_{REF})

The TC850 requires two reference voltage sources in order to generate the "fast-slow" deintegrate phases. The main voltage reference (V_{REF1}) is applied between the REF_1^+ and REF^- pins. The secondary reference (V_{REF2}) is applied between the REF_2^+ and REF^- pins.

The reference voltage inputs are fully differential, and the reference voltage can be generated anywhere within the power supply voltage of the converter. However, to minimize roll-over error, especially at high conversion rates, keep the reference common-mode voltage (i.e., REF^-) near or at the analog common potential. All voltage reference inputs are high impedance. Average reference input current is typically only 30 pA.

Analog Common (COMMON)

Analog common is used as the IN^- return during the zero-integrator and deintegrate phases of each conversion. If IN^- is at a different potential than analog common, a common-mode voltage exists in the system. This signal is rejected by the 86 dB CMRR of the converter. However, in most applications, IN^- will be set at a fixed, known voltage (power supply common, for instance). In this case, analog common should be tied to the same point so that the common-mode voltage is eliminated.

DIGITAL SECTION DESCRIPTION

The TC850 digital section consists of two sets of conversion counters, control and sequencing logic, clock oscillator and divider, data latches, and an 8-bit, 3-state interface bus. A simplified schematic of the bus interface logic is shown in Figure 5.

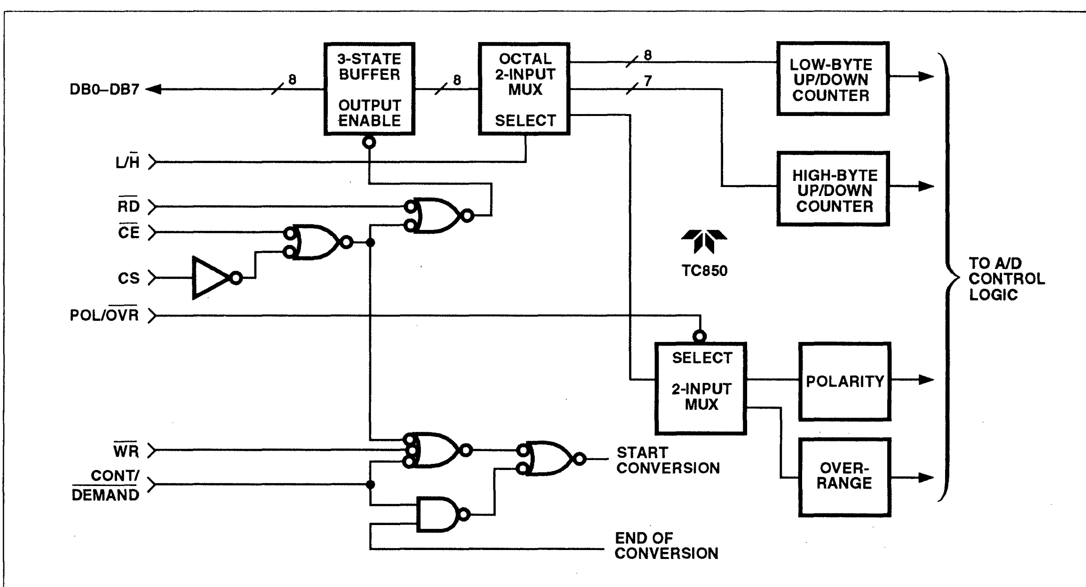


Figure 5 Bus Interface Simplified Schematic

Clock Oscillator

The TC850 includes a crystal oscillator on-chip. All that is required is to connect a crystal across OSC_1 and OSC_2 pins, and to add two inexpensive capacitors (Figure 1). The oscillator output is ÷4 prior to clocking the A/D internal counters. For example, a 100 kHz crystal produces a system clock frequency of 25 kHz. Since each conversion requires 1280 clock periods, in this case the conversion rate will be 25,000/1280, or 19.5 conversions per second.

In most applications, however, an external clock is divided down from the microprocessor clock. In this case, the OSC_1 pin is used as the external oscillator input and OSC_2 is left unconnected. The external clock driver should swing from digital ground to V_S^+. The ÷4 function is active for both external clock and crystal oscillator operations.

Digital Operating Modes

Two modes of operation are available with the TC850, continuous conversions and on-demand. The operating mode is controlled by the CONT/$\overline{\text{DEMAND}}$ input. The bus interface method is different for continuous and demand modes of operation.

Demand Mode Operation

When CONT/$\overline{\text{DEMAND}}$ is low, the TC850 performs one conversion each time the chip is selected and the $\overline{\text{WR}}$ input is pulsed low. Data is valid on the falling edge of the BUSY output and can be accessed using the interface truth table (Table I).

Continuous Mode Operation

When CONT/$\overline{\text{DEMAND}}$ is high, the TC850 continuously performs conversions. Data will be valid on the falling edge of the BUSY output, and remains valid for 443-1/2 clock cycles.

The low/high (L/$\overline{\text{H}}$) byte-select and overrange/polarity (OVR/$\overline{\text{POL}}$) inputs are disabled during continuous mode operation. Data must be read in three consecutive bytes, as shown in Table I.

NOTE: In continuous mode, the conversion result must be read within 443-1/2 clock cycles of the BUSY output falling edge. After this time (i.e., 1/2 clock cycle before BUSY goes high) the internal counters are reset and the data is lost.

Table I. Bus Interface Truth Table

$\overline{\text{CE}}$•CS	$\overline{\text{RD}}$	CONT/$\overline{\text{DEMAND}}$	L/$\overline{\text{H}}$	OVR/$\overline{\text{POL}}$	DB7	DB6–DB0
Pins 1 and 2	**Pin 4**	**Pin 5**	**Pin 7**	**Pin 6**	**Pin 8**	**Pin 9–Pin 15 (Note 1)**
0	0	0	0	0	"1" = Input Positive	Data Bits 14–8
0	0	0	0	1	"1" = Input Overrange (Note 2)	Data Bits 14–8
0	0	0	1	X	Data Bit 7	Data Bits 6–0
0	0	1	X	X	Note 3	
0	1	X	X	X	High-Impedance State	
1	X	X	X	X	High-Impedance State	

NOTES: 1. Pin numbers refer to 40-pin DIP.

2. Extended overrange operation: Although rated at 15 bits (±32,767 counts) of resolution, the TC850 provides an additional 191 counts above full scale. For example, with a full-scale input of 3.2768V, the maximum analog input voltage which will be properly converted is 3.2958V. The extended resolution is signified by the overrange bit being high and the low-order byte contents being between 0 and 190. For example, with a full-scale voltage of 3.2768V:

V_{IN}	Overrange Bit	Low Byte	Data Bits 14–8
3.2767V	Low	255_{10}	127_{10}
3.2768V	High	000_{10}	0_{10}
3.2769V	High	001_{10}	0_{10}
3.2867V	High	099_{10}	0_{10}

3. Continuous mode data transfer:
   a. In continuous mode, data MUST be read in three sequential bytes after the BUSY output goes low:
      (1) The first byte read will be the high-order byte, with DB7 = polarity.
      (2) The second byte read will contain the low-order byte.
      (3) The third byte read will again be the high-order byte, but with DB7 = overrange.
   b. All three data bytes must be read within 443-1/2 clock cycles after the falling edge of BUSY.
   c. The $\overline{\text{RD}}$ input must go high after each byte is read, so that the internal byte counter will be incremented. However, the CS and $\overline{\text{CE}}$ inputs can remain enabled through the entire data transfer sequence.

Pin Description (Digital)

Chip Select and Chip Enable (CS and $\overline{CE}$)

The CS and $\overline{CE}$ inputs permit easy interfacing to a variety of digital bus systems. $\overline{CE}$ is active low while CS is active high. These inputs are logically ANDed internally and are used to enable the $\overline{RD}$ and $\overline{WR}$ inputs.

Write Enable Input ($\overline{WR}$)

The write input is used to initiate a conversion when the TC850 is in demand mode. CS and $\overline{CE}$ must be active for the $\overline{WR}$ input to be recognized. The status of the data bus is meaningless during the $\overline{WR}$ pulse, because no data is actually written into the TC850.

Read Enable Input ($\overline{RD}$)

The read input, combined with CS and $\overline{CE}$, enables the 3-state data bus outputs. Also, in continuous mode, the rising edge of the $\overline{RD}$ input activates an internal byte counter to sequentially read the three data bytes.

Low/High Byte Select (L/$\overline{H}$)

The L/$\overline{H}$ input determines whether the low (least significant) byte or high (most significant) byte of data is placed on the 3-state data bus. This input is meaningful only when the TC850 is in the demand mode. In the continuous mode, data must be read in three predetermined bytes, so the L/$\overline{H}$ input is ignored.

Overrange/Polarity Bit Select (OVR/$\overline{POL}$)

The TC850 provides 15 bits of resolution, plus polarity and overrange bits. Thus, 17 bits of information must be transferred on an 8-bit data bus. To accomplish this, the overrange and polarity bits are multiplexed onto data bit DB7 of the most significant byte. When OVR/$\overline{POL}$ is high, DB7 of the high byte contains the overrange status (high = analog input overrange, low = input within full scale). When OVR/$\overline{POL}$ is low, DB7 is high for positive analog input polarity and low for negative polarity. The OVR/$\overline{POL}$ input is meaningful only when CS, $\overline{CE}$, and $\overline{RD}$ are active, and L/$\overline{H}$ is low (i.e., the most significant byte is selected). OVR/$\overline{POL}$ is ignored when the TC850 is in continuous mode.

Continuous/Demand Mode Input (CONT/$\overline{DEMAND}$)

This input controls the TC850 operating mode. When CONT/$\overline{DEMAND}$ is high, the TC850 performs conversions continuously. In continuous mode, data must be read in the prescribed sequence shown in Table I. Also, all three data bytes must be read within 443-1/2 internal clock cycles after the BUSY output goes low. After 443-1/2 clock cycles data will be lost.

When CONT/$\overline{DEMAND}$ is low, the TC850 begins a conversion each time CS and $\overline{CE}$ are active and $\overline{WR}$ is pulsed low. The conversion is complete and data can be read after the falling edge of the BUSY output. In demand mode, data can be read in any sequence, and remains valid until WR is again pulsed low.

Busy Output (BUSY)

The BUSY output is used to convey an end-of-conversion to external logic. BUSY goes high at the beginning of the deintegrate phase and goes low at the end of the conversion cycle. Data is valid on the falling edge of BUSY. The output-high period is fixed at 836 clock periods, regardless of the analog input value. BUSY is active during continuous and demand mode operation.

This output can also be used to generate an end-of-conversion interrupt in µP-based systems. Noninterrupt-driven systems can poll BUSY to determine when data is valid.

ANALOG SECTION APPLICATIONS

Component Selection

Reference Voltage

The typical value for reference voltage V_{REF1} is 1.6384V. This value yields a full-scale voltage of 3.2768V and resolution of 100 µV per step. The V_{REF2} value is derived by dividing V_{REF1} by 64. Thus, typical V_{REF2} value is 1.6384V/64, or 25.6 mV. The V_{REF2} value should be adjusted within ±1% to maintain 15-bit accuracy for the total conversion process; i.e.,

$$V_{REF2} = \frac{V_{REF1}}{64} \pm 1\%.$$

The reference voltage is not limited to exactly 1.6384V, however, because the TC850 performs a ratiometric conversion. Therefore, the conversion result will be:

$$\text{Digital counts} = \frac{V_{IN}}{V_{REF1}} \bullet 16384.$$

The full-scale voltage can range from 3.2V to 3.5V. Full-scale voltages of less than 3.2V will result in increased noise in the least significant bits, while a full-scale above 3.5V will exceed the input common-mode range.

Integration Resistor

The TC850 buffer supplies 25 µA of integrator charging current with minimal linearity error. R_{INT} is easily calculated:

$$R_{INT} = \frac{V_{FULL\ SCALE}}{25\ \mu A}$$

For a full-scale voltage of 3.2768V, values of R_{INT} between 120 kΩ and 150 kΩ are acceptable.

Integration Capacitor

The integration capacitor should be selected to produce an integrator swing of ≈4V at full scale. The capacitor value is easily calculated:

$$C = \frac{V_{FS}}{R_{INT}} \bullet \frac{4 \bullet 256}{4V \bullet f_{CLOCK}},$$

where f_{CLOCK} is the crystal or external oscillator frequency and V_{FS} is the maximum input voltage.

The integration capacitor should be selected for low dielectric absorption to prevent roll-over errors. A polypropylene, polyester or polycarbonate dielectric capacitor is recommended.

Reference Capacitors

The reference capacitors require a low leakage dielectric, such as polypropylene, polyester or polycarbonate. A value of 1 µF is recommended for operation over the temperature range. If high-temperature operation is not required, the C_{REF} values can be reduced.

Auto-Zero Capacitors

Five capacitors are required to auto-zero the input buffer, integrator amplifier, and comparator. Recommended capacitors are 0.1 µF film dielectric (such as polyester or polypropylene). Ceramic capacitors are not recommended.

DIGITAL SECTION APPLICATION

Oscillator

The TC850 may operate with a crystal oscillator. The crystal selected should be designed for a Pierce oscillator, such as an AT-cut quartz crystal. The crystal oscillator schematic is shown in Figure 6.

Since low frequency crystals are very large and ceramic resonators are too lossy, the TC850 clock should be derived from an external source, such as a microprocessor clock. The clock should be input on the OSC_1 pin and no connection should be made to the OSC_2 pin. The external clock should swing between DGND and V_S^+.

Since oscillator frequency is ÷4 internally and each conversion requires 1280 internal clock cycles, the conversion time will be:

$$\text{Conversion time} = f_{CLOCK} \times 4 \times 1280.$$

An important advantage of the integrating ADC is the ability to reject periodic noise. This feature is most often used to reject line frequency (50 Hz or 60 Hz) noise. Noise rejection is accomplished by selecting the integration period equal to one or more line frequency cycles. The desired clock frequency is selected as follows:

$$f_{CLOCK} = f_{NOISE} \times 4 \times 256,$$

where f_{NOISE} is the noise frequency to be rejected, 4 represents the clock divider, and 256 is the number of integrate cycles.

For example, 60 Hz noise will be rejected with a clock frequency of 61.44 kHz, giving a conversion rate of 12 conversions/sec. Integer submultiples of 61.44 kHz (such as 30.72 kHz, etc.) will also reject 60 Hz noise. For 50 Hz noise rejection, a 51.2 kHz frequency is recommended.

If noise rejection is not important, other clock frequencies can be used. The TC850 will typically operate at conversion rates ranging from 3 to 40 conversions/sec, corresponding to oscillator frequencies from 15.36 kHz to 204.8 kHz.

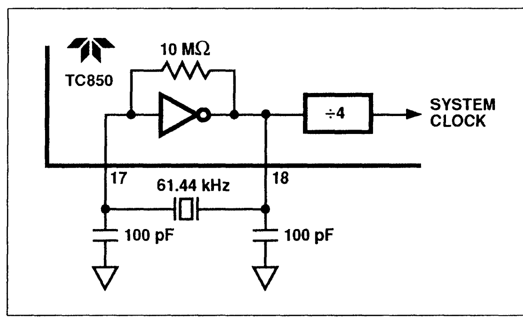


Figure 6 Crystal Oscillator Schematic

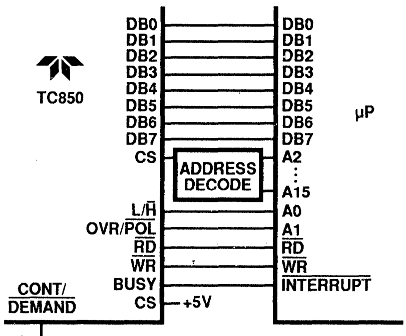
Data Bus Interfacing

The TC850 provides an easy and flexible digital interface. A 3-state data bus and six control inputs permit the TC850 to be treated as a memory device, in most applications. The conversion result can be accessed over an 8-bit bus or via a µP I/O port.

A typical µP bus interface for the TC850 is shown in Figure 7. In this example, the TC850 operates in the demand mode, and conversion begins when a write operation is performed to any decoded address space. The BUSY output interrupts the µP at the end-of-conversion.

The A/D conversion result is read as three memory bytes. The two LSBs of the address bus select high/low byte and overrange/polarity bit data, while high-order address lines enable the $\overline{CE}$ input.

Figure 8 shows a typical interface to a µP I/O port or single-chip µC. The TC850 operates in the continuous mode, and can either interrupt the µC/µP or be polled with an input pin.



ADDRESS	DATA BUS
x 00	HIGH BYTE AND POLARITY
x 01	LOW BYTE
x 10	HIGH BYTE AND OVERRANGE

Figure 7 Interface to Typical μP Data Bus

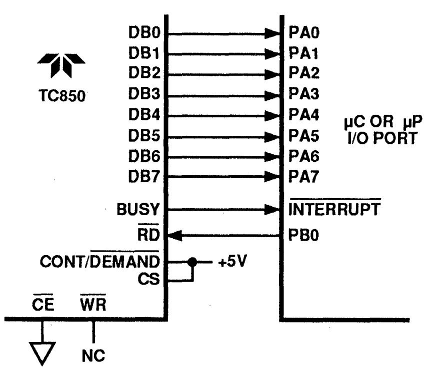


Figure 8 Interface to Typical μP I/O Port or Single-Chip μC

Since the PA0–PA7 inputs are dedicated to reading A/D data, the A/D CS/$\overline{\text{CE}}$ inputs can be enabled continuously. In continuous mode, data must be read in 3 bytes, as shown in Table I. The required $\overline{\text{RD}}$ pulses are provided by a μC/μP output pin.

The circuit of Figure 8 can also operate in the demand mode, with the start-up conversion strobe generated by a μC/μP output pin. In this case, the L/$\overline{\text{H}}$ and CONT/$\overline{\text{DEMAND}}$ inputs can be controlled by I/O pins and the $\overline{\text{RD}}$ input connected to digital ground.

Demand Mode Interface Timing

When CONT/$\overline{\text{DEMAND}}$ input is low, the TC850 performs a conversion each time $\overline{\text{CE}}$ and CS are active and $\overline{\text{WR}}$ is strobed low.

The demand mode conversion timing is shown in Figure 9. BUSY goes low and data is valid 1155 clock pulses after $\overline{\text{WR}}$ goes low. After BUSY goes low, 125 additional clock cycles are required before the next conversion cycle will begin.

Once conversion is started, $\overline{\text{WR}}$ is ignored for 1100 internal clock cycles. After 1100 clock cycles, another $\overline{\text{WR}}$ pulse is recognized and initiates a new conversion when the present conversion is complete. A negative edge on $\overline{\text{WR}}$ is required to begin conversion. If $\overline{\text{WR}}$ is held low, conversions will not occur continuously.

The A/D conversion data is valid on the falling edge of BUSY, and remains valid until one-half internal clock cycle before BUSY goes high on the succeeding conversion. BUSY can be monitored with an I/O pin to determine end of conversion, or to generate a μP interrupt.

In demand mode, the three data bytes can be read in any desired order. The TC850 is simply regarded as three bytes of memory and accessed accordingly. The bus output timing is shown in Figure 10.

Continuous Mode Interface Timing

When the CONT/$\overline{\text{DEMAND}}$ input is high, the TC850 performs conversions continuously. Data will be valid on the falling edge of BUSY, and all three bytes must be read within 443-1/2 internal clock cycles of BUSY going low. The timing diagram is shown in Figure 11.

In continuous mode, OVR/$\overline{\text{POL}}$ and L/$\overline{\text{H}}$ byte-select inputs are ignored. The TC850 automatically cycles through three data bytes, as shown in Table I. Bus output timing in the continuous mode is shown in Figure 12.

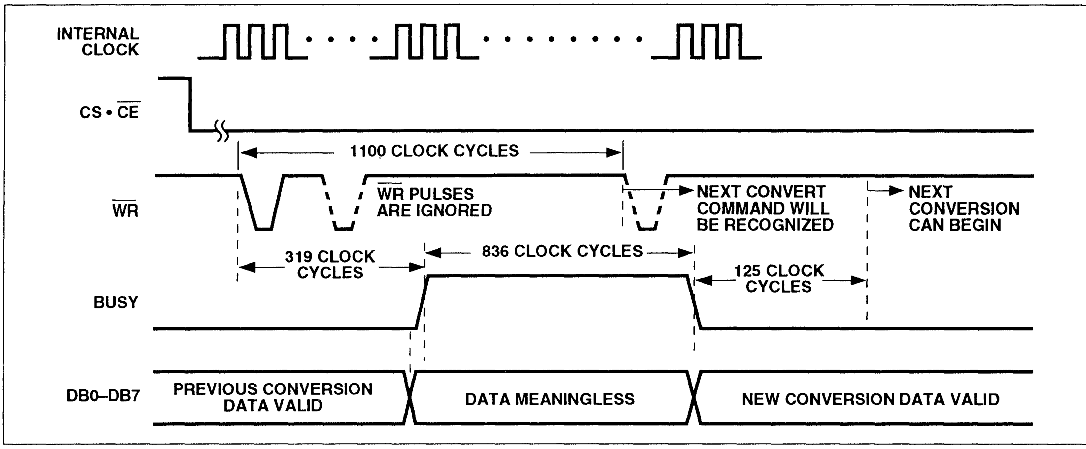
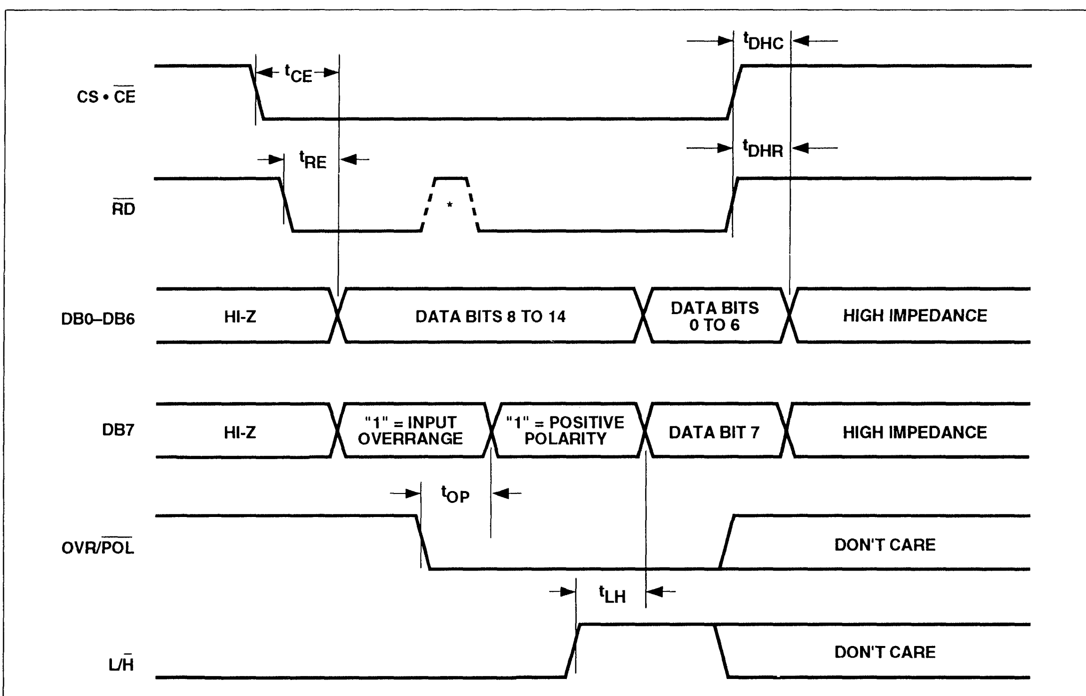


Figure 9 Conversion Timing, Demand Mode



NOTE: CONT/$\overline{DEMAND}$ = LOW

* $\overline{RD}$ (as well as CS and $\overline{CE}$) can go HIGH after each byte is read (i.e., in a µP bus interface) or remain LOW during the entire DATA–READ sequence (i.e., µP I/O port interface).

Figure 10 Bus Output Timing, Demand Mode

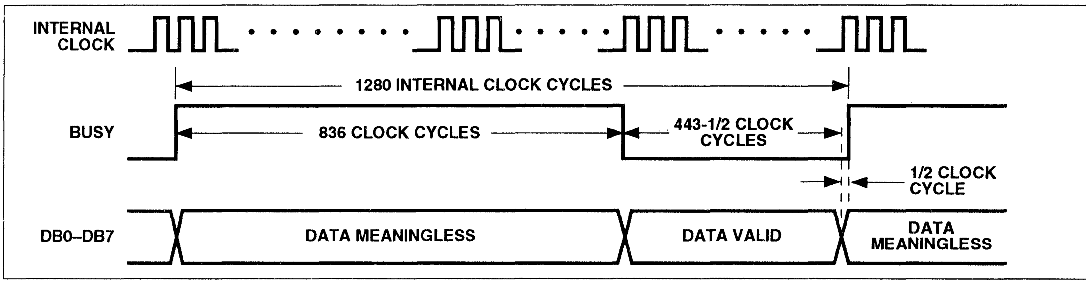


Figure 11 Conversion Timing, Continuous Mode

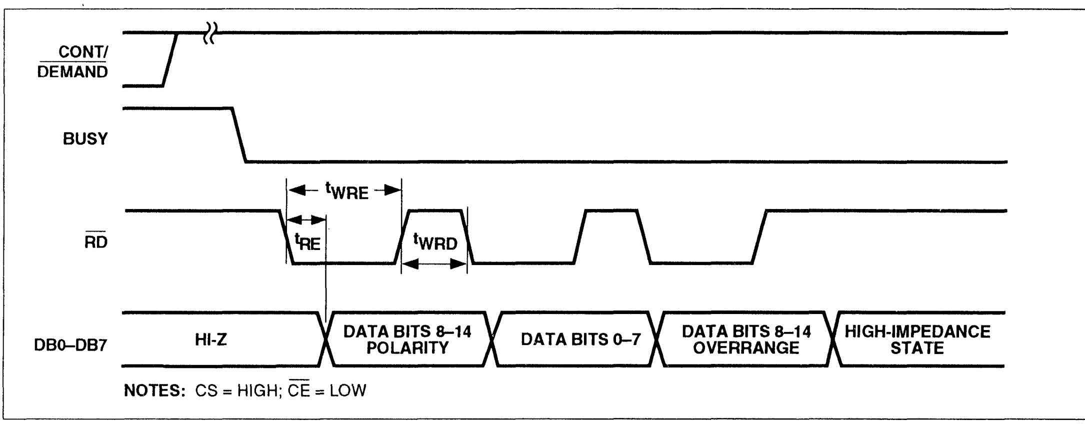


Figure 12 Bus Output Timing, Continuous Mode

12-BIT μP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **Zero-Integrator Cycle for Fast Recovery From Input Overloads**
- **Eliminates Cross Talk in Multiplexed Systems**
- **12-Bit Plus Sign Integrating A/D Converter With Overrange Indication**
- **Sign Magnitude Coding Format**
- **True Differential Signal Input and Differential Reference Input**
- **Low Noise .... 15 μV_{P-P} Typ**
- **High Normal Mode Noise and Line Frequency Rejection**
- **Input Current .... 1 pA Typ**
- **No Zero Adjustment**
- **TTL-Compatible, Byte-Organized Tri-State Outputs**
- **UART Handshake Mode for Simple Serial Data Transmission**
- **Power Dissipation .... Less Than 20 mW Typ**
- **Internal Voltage Reference**

GENERAL DESCRIPTION

The TC7109A is a 12-bit plus sign, CMOS low-power analog-to-digital converter (ADC). Only eight passive components and a crystal are required to form a complete dual-slope integrating ADC.

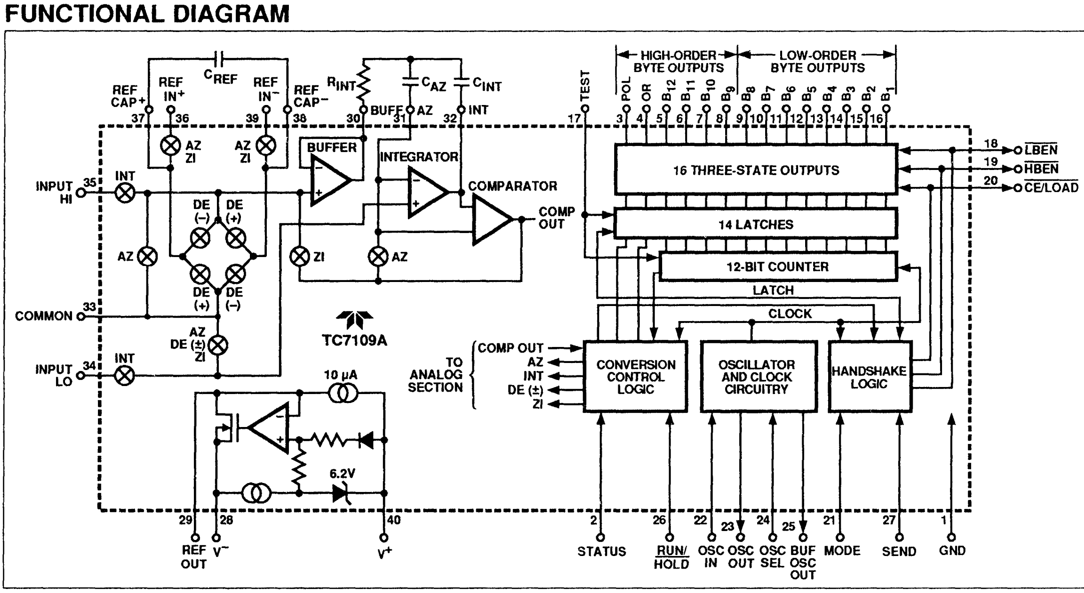
The improved V_{OH} source current TC7109A has features that make it an attractive per-channel alternative to analog multiplexing for many data acquisition applications. These features include typical input bias current of 1 pA, drift of less than 1 μV/°C, input noise typically 15 μV_{P-P}, and auto-zero. True differential input and reference allow measurement of bridge-type transducers such as load cells, strain gauges, and temperature transducers.

The TC7109A provides a versatile digital interface. In the direct mode, chip select and high/low byte enables control parallel bus interface. In the handshake mode, the TC7109A will operate with industry-standard UARTs in controlling serial data transmission — ideal for remote data logging. Control and monitoring of conversion timing is provided by the RUN/$\overline{\text{HOLD}}$ input and STATUS output.

For applications requiring more resolution, see the TC500, 15-bit plus sign ADC data sheet.

The TC7109A has improved overrange recovery performance and higher output drive capability than the original TC7109. All new (or existing) designs should specify the TC7109A wherever possible.

FUNCTIONAL DIAGRAM



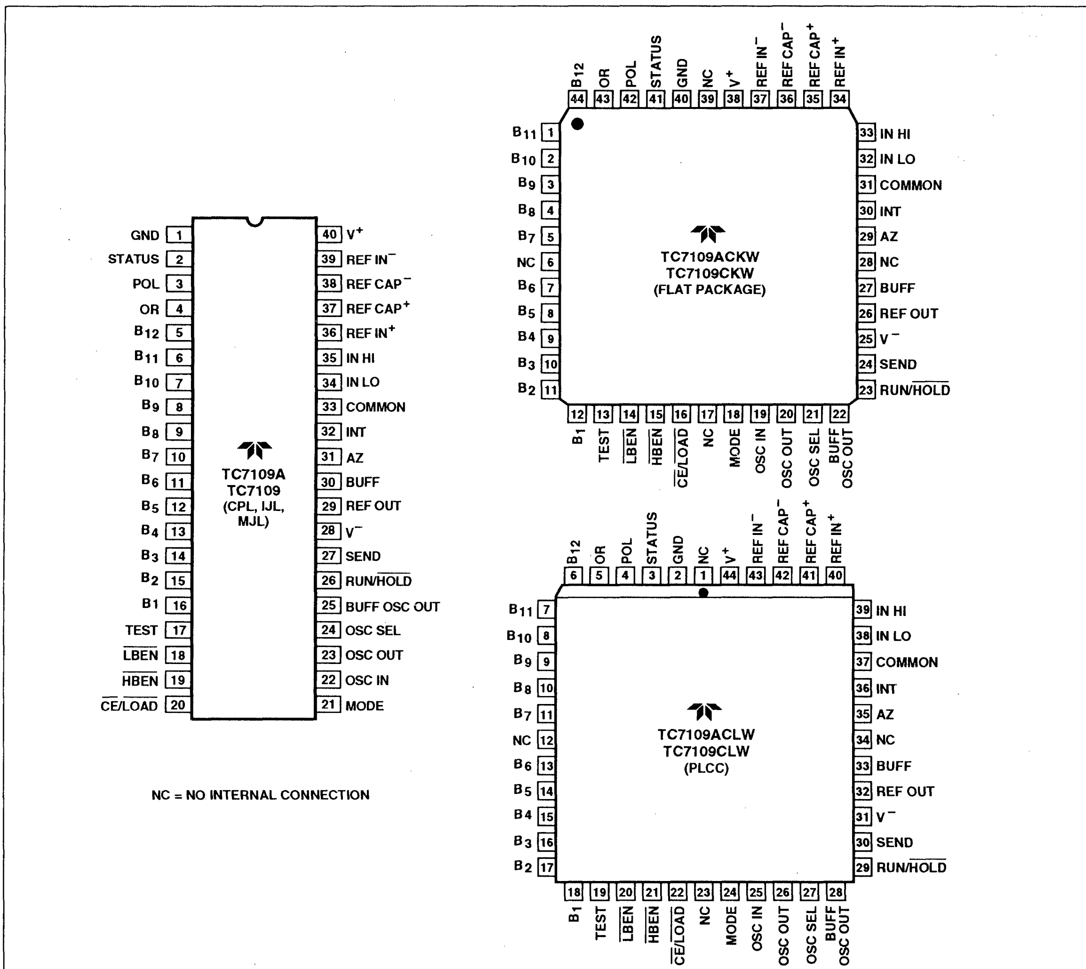
TC7109
TC7109A

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7109ACPL	40-Pin Plastic DIP	0°C to +70°C
TC7109ACKW	44-Pin Flat	0°C to +70°C
TC7109ACLW	44-Pin PLCC	0°C to +70°C
TC7109AIJL	40-Pin CerDIP	–25°C to +85°C
TC7109AMJL	40-Pin CerDIP	–55°C to +125°C

Part No.	Package	Temperature Range
TC7109CPL	40-Pin Plastic DIP	0°C to +70°C
TC7109CKW	44-Pin Flat	0°C to +70°C
TC7109CLW	44-Pin PLCC	0°C to +70°C
TC7109IJL	40-Pin CerDIP	–25°C to +85°C
TC7109MJL	40-Pin CerDIP	–55°C to +125°C

PIN CONFIGURATIONS



12-BIT μP-COMPATIBLE ANALOG-TO-DIGITAL CONVERTERS

TC7109 TC7109A

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) .... +6.2V
Negative Supply voltage (GND to V^-) .... –9V
Analog Input Voltage (Low to High) (Note 1) .... V^+ to V^-
Reference Input Voltage (Low to High (Note 1) ..... V^+ to V^-
Digital Input Voltage (Pins 2–27) (Note 2) .... GND –0.3V
Power Dissipation (Note 3)
    Ceramic Package .... 1W at +85°C
    Plastic Package .... 500 mW at +70°C
Operating Temperature Range
    Plastic Package (C) .... 0°C to +70°C
    Ceramic Package (I) .... –25°C to +85°C
    (M) .... –55°C to +125°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

NOTES: 1. Input voltages may exceed supply voltages if input current is limited to ±100 μA.
2. Connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latch-up. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TC7109A before its power supply is established. In multiple supply systems, the supply to the device should be

ELECTRICAL CHARACTERISTICS: All parameters with V^+ = +5V, V^- = –5V, GND = 0V, T_A = +25°C, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Analog						
	Overload Recovery Time (TC7109A)			0	1	Measurement Cycle
	Zero Input Reading	V_{IN} = 0V Full Scale = 409.6 mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
	Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 204.8 mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
NL	Nonlinearity (Max Deviation From Best Straight Line Fit)	Full Scale = 409.6 mV to 2.048V Over Full Operating Temperature Range	–1	±0.2	+1	Count
	Roll-Over Error (Difference in Reading for Equal Positive and Negative Inputs Near (Full Scale)	Full Scale = 409.6 mV to 2.048V Over Full Operating Temperature Range	–1	±0.02	+1	Count
CMRR	Input Common-Mode Rejection Ratio	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6 mV		50		μV/V
V_{CMR}	Common-Mode Voltage Range	Input High, Input Low, and Common Pins	V^-+1.5		V^+–1	V
e_N	Noise (P-P Value Not Exceeded 95% of Time)	V_{IN} = 0V Full Scale = 409.6 mV		15		μV
I_{IN}	Leakage Current at Input	V_{IN}, All Packages: +25°C C Device: 0°C ¶ T_A ¶ +70°C I Device: –25°C ¶ T_A ¶ +85°C M Device: –55°C ¶ T_A ¶ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
TC_{ZS}	Zero Reading Drift	V_{IN} = 0V		0.2	1	μV/°C
TC_{FS}	Scale-Factor Temperature Coefficient	V_{IN} = 408.9 mV = >7770_8 Reading, Ext Ref = 0 ppm/°C		1	5	μV/°C
I^+	Supply Current (V^+ to GND)	V_{IN} = 0V, Crystal Oscillator 3.58 MHz Test Circuit		700	1500	μA
I_S	Supply Current (V^+ to V^-)	Pins 2–21, 25, 26, 27, 29 Open		700	1500	μA

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{REF}	Ref Out Voltage	Referenced to V^+, 25 kΩ Between V^+ and Ref Out	–2.4	–2.8	–3.2	V
TC_{REF}	Ref Out Temperature Coefficient	25 kΩ Between V^+ and Ref Out 0°C ¶ T_A ¶ +70°C		80		ppm/°C
Digital						
V_{OH}	Output High Voltage	TC7109: I_{OUT} = 100 μA TC7109A: I_{OUT} = 700 μA Pins 2–16, 18, 19, 20	3.5	4.3		V
V_{OL}	Output Low Voltage	I_{OUT} = 1.6 mA		0.2	0.4	V
	Output Leakage Current	Pins 3–16 High Impedance		±0.01	±1	μA
	Control I/O Pull-Up Current	Pins 18, 19, 20 V_{OUT} = V^+–3V Mode Input at GND		5		μA
	Control I/O Loading	$\overline{HBEN}$, Pin 19; $\overline{LBEN}$, Pin 18			50	pF
V_{IH}	Input High Voltage	Pins 18–21, 26, 27 Referenced to GND	2.5			V
V_{IL}	Input Low Voltage	Pins 18-21, 26, 27 Referenced to GND			1	V
	Input Pull-Up Current	Pins 26, 27; V_{OUT} = V^+–3V Pins 17, 24; V_{OUT} = V^+–3V		5 25		μA μA
	Input Pull-Down Current	Pin 21; V_{OUT} = GND = +3V		1		μA
	Oscillator Output Current, High	V_{OUT} = 2.5V		1		mA
	Oscillator Output Current, Low	V_{OUT} = 2.5V		1.5		mA
	Buffered Oscillator Output Current, High	V_{OUT} = 2.5V		2		mA
	Buffered Oscillator Output Current, Low	V_{OUT} = 2.5V		5		mA
t_W	Mode Input Pulse Width		60			ns

HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes, or other conducting material. Use proper anti-static handling procedures. Do not connect in circuits under "power-on" conditions, as high transients may cause permanent damage.

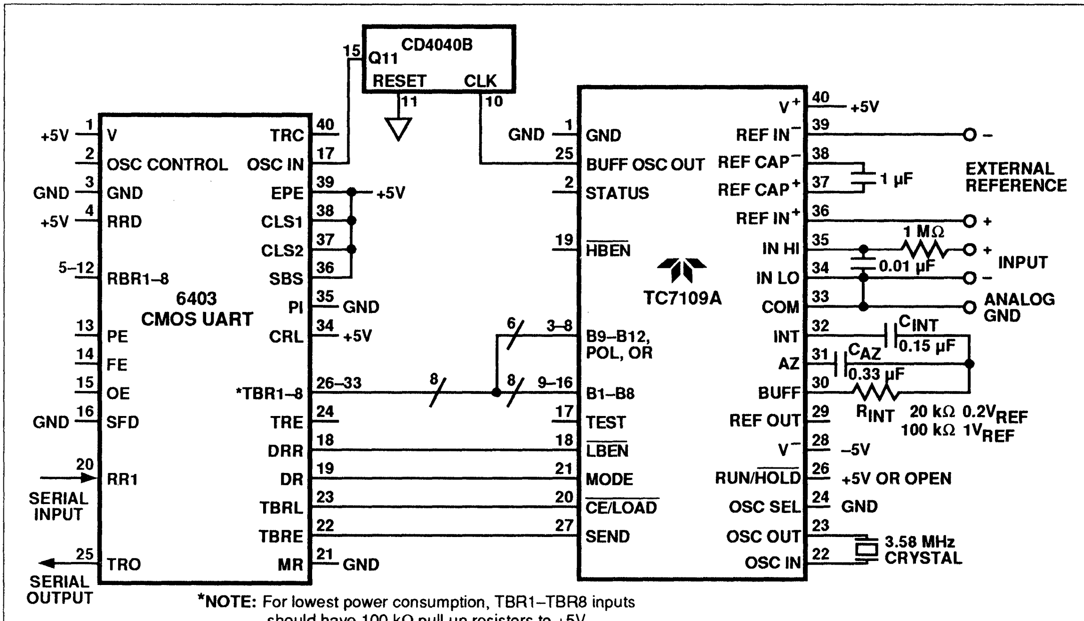
PIN DESCRIPTION

40-Pin DIP Pin Number	Name	Description	
1	GND	Digital ground, 0V, ground return for all digital logic.	
2	STATUS	Output high during integrate and deintegrate until data is latched. Output low when analog section is in auto-zero or zero-integrator configuration.	
3	POL	Polarity — High for positive input.	All Three-State Data Bits
4	OR	Overrange — High if overranged.	
5	B_{12}	Bit 12 (Most Significant Bit)	
6	B_{11}	Bit 11	
7	B_{10}	Bit 10	
8	B_9	Bit 9	
9	B_8	Bit 8	
10	B_7	Bit 7	
11	B_6	Bit 6	
12	B_5	Bit 5	
13	B_4	Bit 4	
14	B_3	Bit 3	
15	B_2	Bit 2	
16	B_1	Bit 1 (Least Significant Bit)	
17	TEST	Input High — Normal operation. Input Low — Forces all bit outputs high. **Note:** This input is used for test purposes only.	
18	$\overline{\text{LBEN}}$	Low-Byte Enable — With MODE (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates low-order byte outputs, B1–B8. With MODE (Pin 21) high, this pin serves as low-byte flag output used in handshake mode. See Figures 7, 8, and 9.	
19	$\overline{\text{HBEN}}$	High-Byte Enable — With MODE (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates high-order byte outputs, B9–B12, POL, OR. With MODE (Pin 21) high, this pin serves as high-byte flag output used in handshake mode. See Figures 7, 8, and 9.	
20	$\overline{\text{CE/LOAD}}$	Chip Enable/Load — With MODE (Pin 21) low, $\overline{\text{CE/LOAD}}$ serves as a master output enable. When high, B1–B12, POL, OR outputs are disabled. When MODE (Pin 21) is high, a load strobe is used in handshake mode. See Figure 7, 8, and 9.	
21	MODE	Input Low — Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode and output of data as in Figure 9. Input High — Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversions completion.	
22	OSC IN	Oscillator Input	
23	OSC OUT	Oscillator Output	
24	OSC SEL	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. Input low configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.	
25	BUF OSC OUT	Buffered Oscillator Output	
26	RUN/$\overline{\text{HOLD}}$	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed; converter will stop in auto-zero seven counts before integrate.	
27	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Connect to V+ if not used.	
28	V^-	Analog Negative Supply — Nominally –5V with respect to GND (Pin 1).	
29	REF OUT	Reference Voltage Output — Nominally 2.8V down from V^+ (Pin 40).	

PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number	Name	Description
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Node — Inside foil of C_{AZ}.
32	INTEGRATOR	Integrator Output — Outside foil of C_{INT}.
33	COMMON	Analog Common — System is auto-zeroed to COMMON.
34	INPUT LOW	Differential Input Low Side
35	INPUT HIGH	Differential Input High Side
36	REF IN +	Differential Reference Input Positive
37	REF CAP +	Reference Capacitor Positive
38	REF CAP –	Reference Capacitor Negative
39	REF IN –	Differential Reference Input Negative
40	V+	Positive Supply Voltage — Nominally +5V with respect to GND (Pin 1).

NOTE: All digital levels are positive true.



***NOTE:** For lowest power consumption, TBR1–TBR8 inputs should have 100 kΩ pull-up resistors to +5V.

Figure 1 TC7109A UART Interface (Send Any Word to UART to Transmit Latest Result)

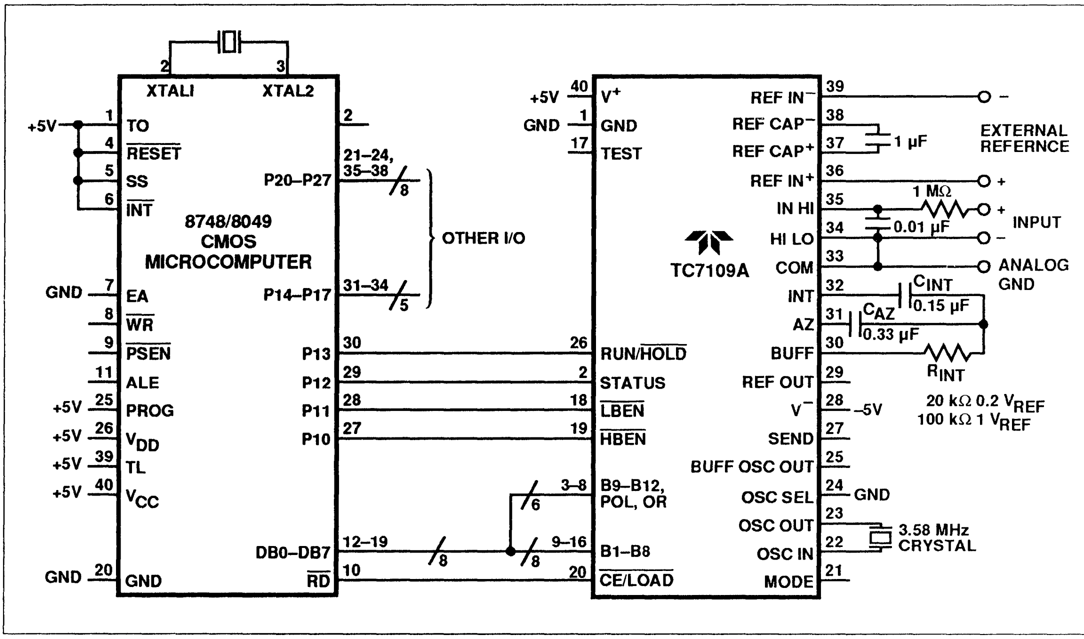


Figure 2 TC7109A Parallel Interface With 8048/8049 Microcomputer

DETAILED DESCRIPTION

Analog Section

The functional diagram shows a block diagram of the analog section of the TC7109A. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle), when the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V+. Each measurement cycle is divided into four phases, as shown in Figure 3. They are: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), (3) Reference Deintegrate (DE), and (4) Zero Integrator (ZI).

Auto-Zero Phase

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 µV.

Signal-Integrate Phase

The buffer and integrator inputs are removed from common and connected to input high and input low. The auto-zero loop is opened. The auto-zero capacitor is placed in series in the loop to provide an equal and opposite compensating offset voltage. The differential voltage between input high and input low is integrated for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined. If the input signal has no return to the converter's power supply, input low can be tied to analog common to establish the correct common-mode voltage.

Deintegrate Phase

Input high is connected across the previously-charged reference capacitor and input low is internally connected to analog common. Circuitry within the chip ensures the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established by auto-zero) with a fixed slope. The time, represented by the number of clock periods counted for the output to return to zero, is proportional to the input signal.

Zero-Integrator Phase

The ZI phase only occurs when an input overrange condition exists. The function of the ZI phase is to eliminate residual charge on the integrator capacitor after an overrange measurement. Unless removed, the residual charge will be transferred to the auto-zero capacitor and cause an error in the succeeding conversion.

The ZI phase virtually eliminates hysteresis or "cross talk" in multiplexed systems. An overrange input on one channel will not cause an error on the next channel measured. This feature is especially useful in thermocouple measurements, where unused (or broken thermocouple) inputs are pulled to the positive supply rail.

During ZI, the reference capacitor is charged to the reference voltage. The signal inputs are disconnected from the buffer and integrator. The comparator output is connected to the buffer input, causing the integrator output to be driven rapidly to 0V (Figure 3). The ZI phase only occurs following an overrange and lasts for a maximum of 1024 clock periods.

Differential Input

The TC7109A has been optimized for operation with analog common near digital ground. With +5V and –5V power supplies, a full ±4V full-scale integrator swing maximizes the analog section's performance.

A typical CMRR of 86 dB is achieved for input differential voltages anywhere within the typical common-mode range of 1V below the positive supply to 1.5V above the negative supply. However, for optimum performance the IN HI and IN LO inputs should not come within 2V of either supply rail. Since the integrator also swings with the common-mode voltage, care must be exercised to ensure the integrator output does not saturate. A worst-case condition is near a full-scale negative differential input voltage with a large positive common-mode voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. In such cases, the integrator swing can be reduced to less than the recommended ±4V full-scale value, with some loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. Roll-over voltage is the main source of common-mode error, caused by the reference capacitor losing or gaining charge due to stray capacity on its nodes. With a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called upon to deintegrate a positive signal and lose charge (decrease voltage) when called upon to deintegrate a negative input signal. This difference in reference for (+) or (–) input voltage will cause a roll-over error. This error can be held to less than 0.5 count worst case by using a large reference capacitor in comparison to the stray capacitance. To minimize roll-over error from these sources, keep the reference common-mode voltage near or at analog common.

Digital Section

The digital section is shown in the block diagram (Figure 4) and includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL compatible three-state output drivers, UART handshake logic, polarity, overrange, and control logic. Logic levels are referred to as "low" or "high."

Inputs driven from TTL gates should have 3 kW to 5 kW pull-up resistors added for maximum noise immunity. For minimum power consumption, all inputs should swing from GND (low) to V^+ (high).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of signal integrate and goes low one-half clock period after new data from the conversion has been stored in the output latches (see Figure 3). The signal may be used as a "data valid" flag to drive interrupts, or for monitoring the status of the converter. (Data will not change while status is low.)

MODE Input

The output mode of the converter is controlled by the MODE input. The converter is in its "direct" output mode, when the MODE input is low or left open. The output data is directly accessible under the control of the chip and byte enable inputs (this input is provided with a pull-down resistor to ensure a low level when the pin is left open). When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in 2 bytes, then returns to "direct" mode. When the MODE input is kept high, the converter will output data in the handshake mode at the end of every conversion cycle. With MODE = 0 (direct bus transfer), the send input should be tied to V^+. (See "Handshake Mode.")

RUN/$\overline{\text{HOLD}}$ Input

With the RUN/$\overline{\text{HOLD}}$ input high, or open, the circuit operates normally as a dual-slope ADC, as shown in Figure 3. Conversion cycles operate continuously with the output latches updated after zero crossing in the deintegrate mode. An internal pull-up resistor is provided to ensure a high level with an open input.

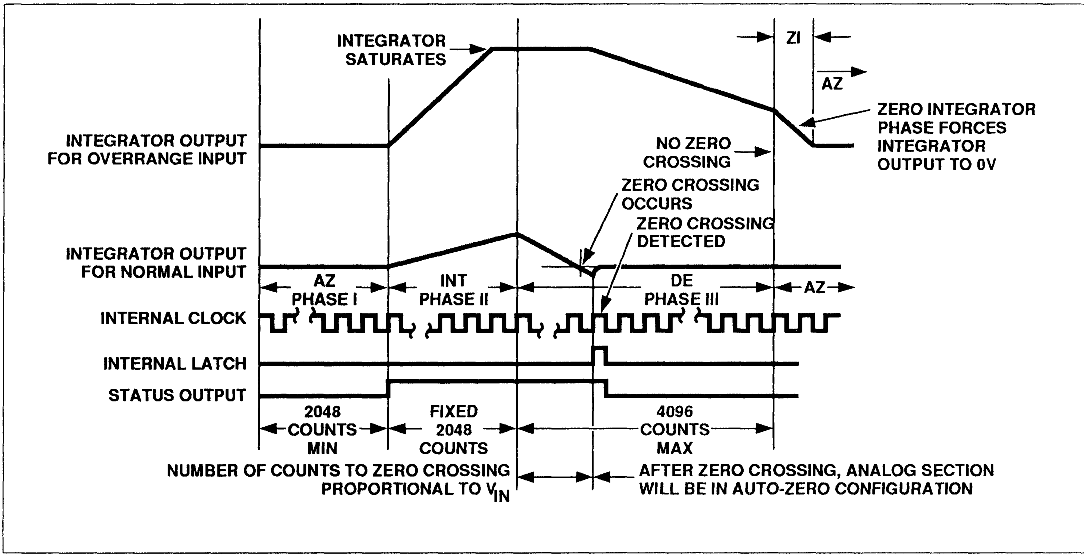


Figure 3 Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

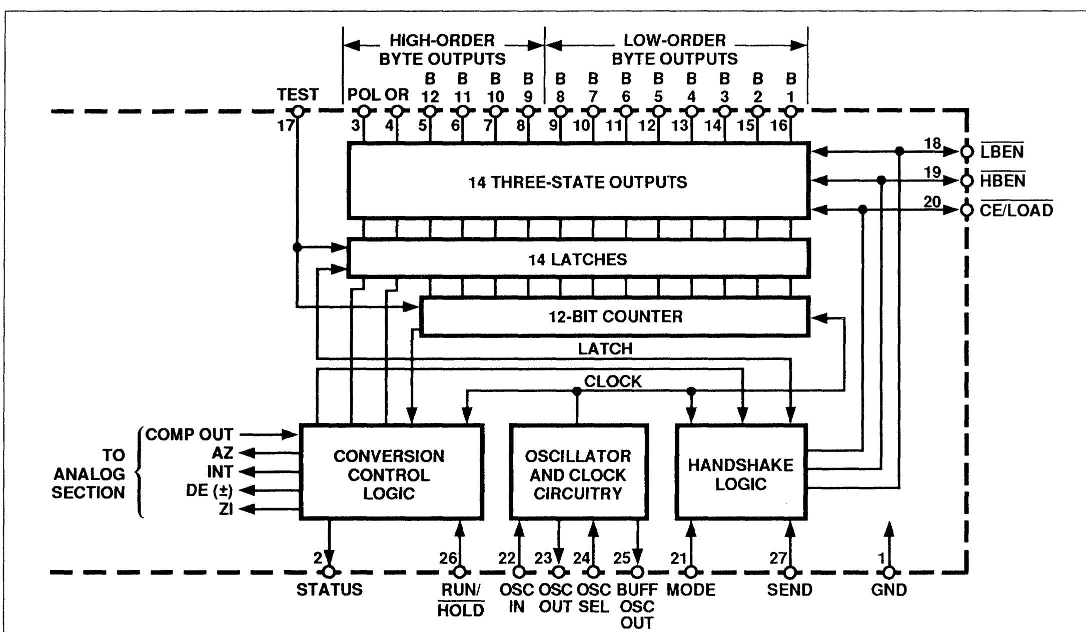


Figure 4 Digital Section

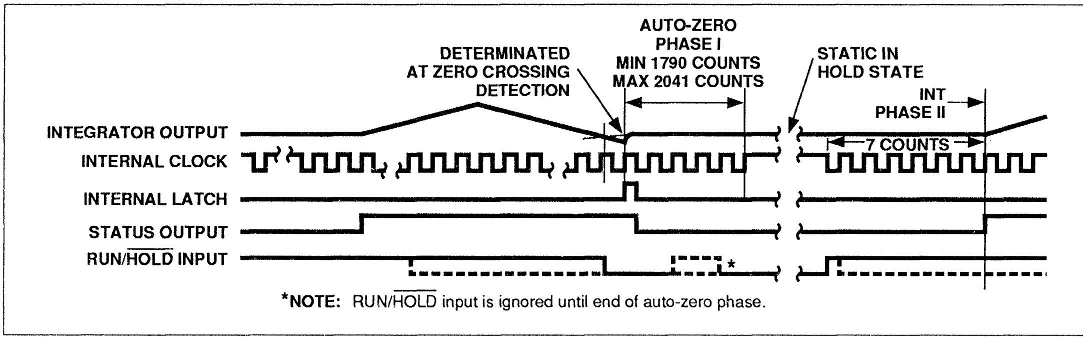


Figure 5 TC7109A RUN/HOLD Operation

The RUN/HOLD input may be used to shorten conversion time. If RUN/HOLD goes low any time after zero crossing in the deintegrate mode, the circuit will jump to auto-zero and eliminate that portion of time normally spent in deintegrate.

If RUN/HOLD stays or goes low, the conversion will complete with minimum time in deintegrate. It will stay in auto-zero for the minimum time and wait in auto-zero for a high at the RUN/HOLD input. As shown in Figure 5, the STATUS output will go high 7 clock periods after RUN/HOLD is changed to high, and the converter will begin the integrate phase of the next conversion.

The RUN/HOLD input allows controlled conversion interface. The converter may be held at idle in auto-zero with RUN/HOLD low. The conversion is started when RUN/HOLD goes high, and the new data is valid when the STATUS output goes low (or is transferred to the UART; see "Handshake Mode"). RUN/HOLD may now go low, terminating deintegrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion. Conversion time can be minimized by ensuring RUN/HOLD goes low during deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/HOLD input can be provided by connecting it to the buffered oscillator output. In this mode, the input value measured determines the conversion time.

Direct Mode

The data outputs (bits 1 through 8, low-order bytes; bits 9 through 12, polarity and overrange high-order bytes) are accessible under control of the byte and chip enable terminals as inputs with the MODE pin at a low level. These three inputs are all active low. Internal pull-up resistors are provided for an inactive high level when left open. When chip enable is low, a byte-enable input low will allow the outputs of the byte to become active. A variety of parallel data accessing techniques may be used, as shown in the "Interfacing" section. (See Figure 6 and Table I.)

The access of data should be synchronized with the conversion cycle by monitoring the STATUS output. This prevents accessing data while it is being updated and eliminates the acquisition of erroneous data.

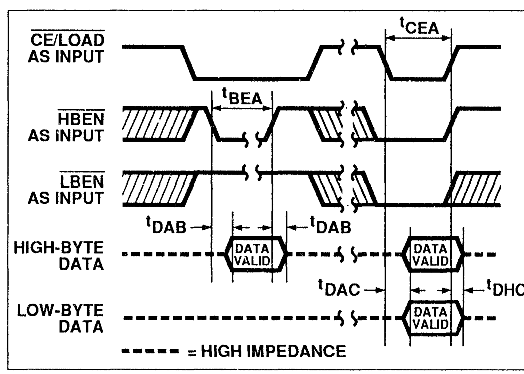


Figure 6 TC7109A Direct Mode Output Timing

Table I TC7109A Direct Mode Timing Requirements

Symbol	Description	Min	Typ	Max	Units
t_{BEA}	Byte Enable Width	200	500		ns
t_{DAB}	Data Access Time From Byte Enable		150	300	ns
t_{DHB}	Data Hold Time From Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	300	500		ns
t_{DAC}	Data Access Time From Chip Enable		200	400	ns
t_{DHC}	Data Hold Time From Chip Enable		200	400	ns

Handshake Mode

An alternative means of interfacing the TC7109A to digital systems is provided when the handshake output mode of the TC7109A becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode allows a direct interface between the TC7109A and industry-standard UARTs with no external logic required. The TC7109A provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form when triggered into the handshake mode. The cost of designing remote data acquisition stations is reduced using serial data transmission to minimize the number of lines to the central controlling processor.

The MODE input controls the handshake mode. When the MODE input is held high, the TC7109A enters the handshake mode after new data has been stored in the output latches at the end of every conversion performed (see Figures 7 and 8). Entry into the handshake mode may be triggered on demand by the MODE input. At any time during the conversion cycle, the low-to-high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. The MODE input is ignored in the handshake mode, and until the converter completes the output cycle and clears the handshake mode, data updating will be inhibited (see Figure 9).

When the MODE input is high or when the converter enters the handshake mode, the chip and byte enable inputs become TTL-compatible outputs which provide the output cycle control signals (see Figures 7, 8 and 9).

The SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data in the handshake mode. The sequence of the output cycle with SEND held high is shown in Figure 7. The handshake mode (internal MODE high) is entered after the data latch pulse (the $\overline{\text{CE/LOAD}}$, $\overline{\text{LBEN}}$ and $\overline{\text{HBEN}}$ terminals are active as outputs since MODE remains high).

The high level at the SEND input is sensed on the same high-to-low internal clock edge. On the next low-to-high internal clock edge, the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled and the $\overline{\text{CE/LOAD}}$ and the $\overline{\text{HBEN}}$ outputs assume a low level. The $\overline{\text{CE/LOAD}}$ output remains low for one full internal clock period only; the data outputs remain active for 1-1/2 internal clock periods; and the high-byte enable remains low for 2 clock periods. The $\overline{\text{CE/LOAD}}$ output low level or low-to-high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{\text{CE/LOAD}}$ and $\overline{\text{LBEN}}$ while the low-order byte outputs (bits 1 through 8) are activated. When both bytes are sent, the handshake mode is terminated. The typical UART interfacing timing is shown in Figure 8. The SEND input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows an industry-standard HD6403 or CDP1854 CMOS UART to interface to serial data channels. The SEND input to the TC7109A is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{\text{CE/LOAD}}$ input of the TC7109A drives the TBRL (Transmitter Buffer Register Load) input to the UART. The eight transmitter buffer register inputs accept the parallel data outputs. With the UART transmitter buffer register empty, the SEND input will be high when the handshake mode is entered after new data is stored. The high-order byte outputs become active and the $\overline{\text{CE/LOAD}}$ and $\overline{\text{HBEN}}$ inputs will go low after SEND is sensed. When $\overline{\text{CE/LOAD}}$ goes high at the end of one clock period, the high-order byte data is clocked into the UART transmitter buffer register. The UART TBRE output will go low, which halts the output cycle with the $\overline{\text{HBEN}}$ output low, and the high-order byte outputs active. When the UART has transferred the data to the transmitter register and cleared the transmitter buffer register, the TBRE returns high. The high-order byte outputs are disabled on the next TC7109A internal clock high-to-low edge, and one-half internal clock later, the $\overline{\text{HBEN}}$ output returns high. The $\overline{\text{CE/LOAD}}$ and $\overline{\text{LBEN}}$ outputs go low at the same time as the low-order byte outputs become active. When the $\overline{\text{CE/LOAD}}$ returns high at the end of one clock period, the low-order data is clocked into the UART transmitter buffer register, and TBRE again goes low. The next TC7109A internal clock high-to-low edge will sense when TBRE returns to a high, disabling the data inputs. One-half internal clock later, the handshake mode is cleared, and the $\overline{\text{CE/LOAD}}$, $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ terminals return high and stay active, if MODE still remains high.

Handshake output sequences may be performed on demand by triggering the converter into handshake mode with a low-to-high edge on the MODE input. A handshake output sequence triggered is shown in Figure 9. The SEND input is low when the converter enters handshake mode. The whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte.

Figure 9 also shows that the output sequence can take longer than a conversion cycle. New data will not be latched when the handshake mode is still in progress and is therefore lost.

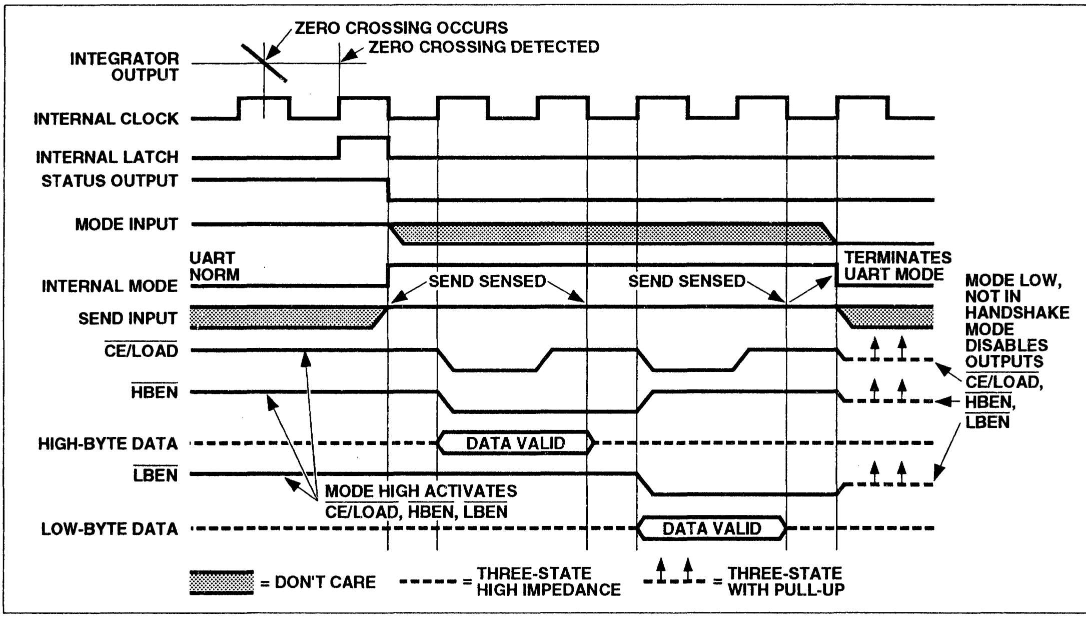


Figure 7 TC7109A Handshake With Send Input Held Positive

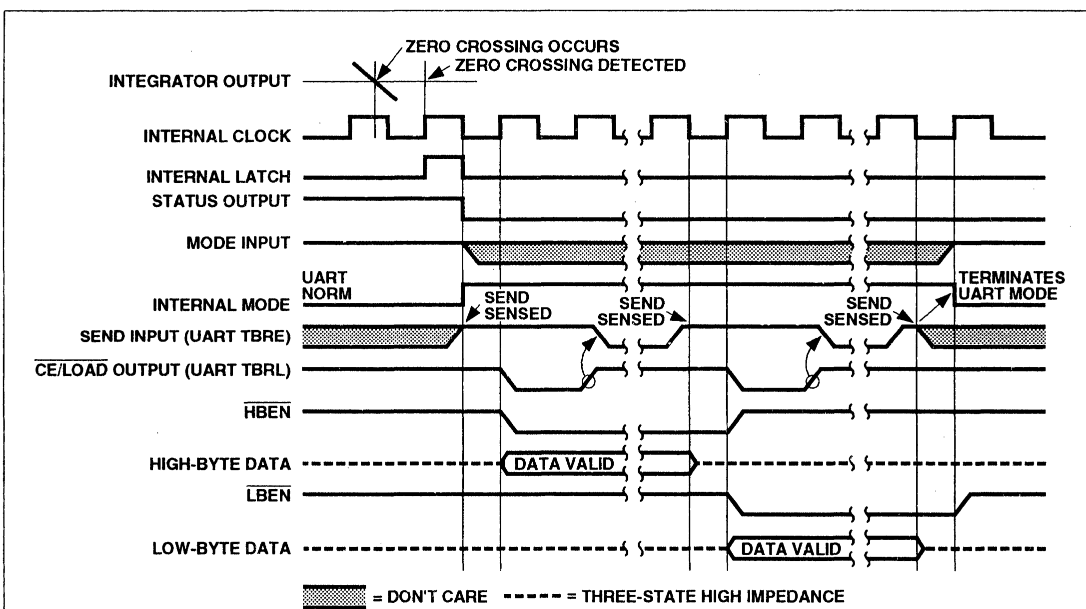


Figure 8 TC7109A Handshake — Typical UART Interface Timing

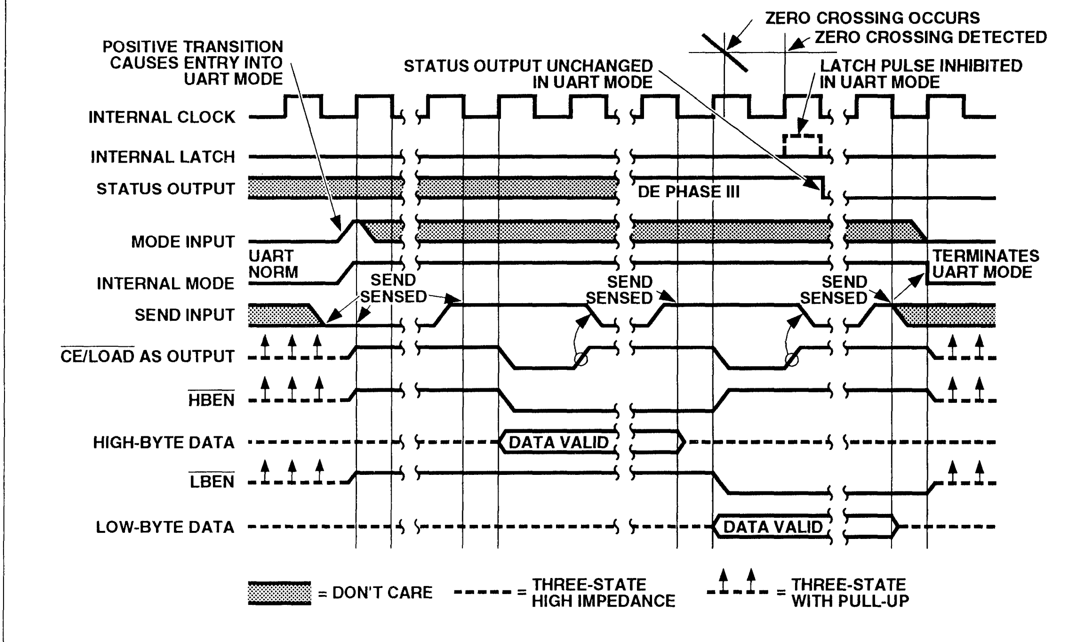


Figure 9 TC7109A Handshake Triggered by MODE Input

Oscillator

The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input optimizes the internal configuration of the oscillator for RC or crystal operation. The OSCILLATOR SELECT input is provided with a pull-up resistor. When the OSCILLATOR SELECT input is high or left open, the oscillator is configured for RC operation. The internal clock will be the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. Connect the resistor and capacitor as in Figure 10. The circuit will oscillate at a frequency given by $f = 0.45/RC$. A 100 kΩ resistor is recommended for useful ranges of frequency. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60 Hz period for optimum 60 Hz line rejection.

With OSCILLATOR SELECT input low, two on-chip capacitors and a feedback device are added to the oscillator. In this configuration, the oscillator will operate with most crystals in the 1 to 5 MHz range with no external components (Figure 11). The OSCILLATOR SELECT input low inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. A 3.58 MHz TV crystal gives a division ratio providing an integration time given by:

$$t = (2048 \text{ clock periods}) \frac{58}{3.58 \text{ MHz}} = 33.18 \text{ ms}$$

The error is less than 1% from two 60 Hz periods, or 33.33 ms, which will give better than 40 dB, 60 Hz rejection. The converter will operate reliably at conversion rates up to 30 per second, corresponding to a clock frequency of 245.8 kHz.

When the oscillator is to be overdriven, the OSCILLATOR OUTPUT should be left open, and the overdriving signal should be applied at the OSCILLATOR INPUT. The internal clock will be of the same duty cycle, frequency and phase as the input signal. When the OSCILLATOR SELECT is at GND, the clock will be 1/58 of the input frequency.

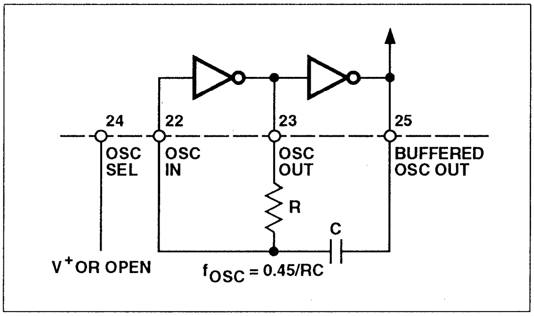


Figure 10 TC7109A RC Oscillator

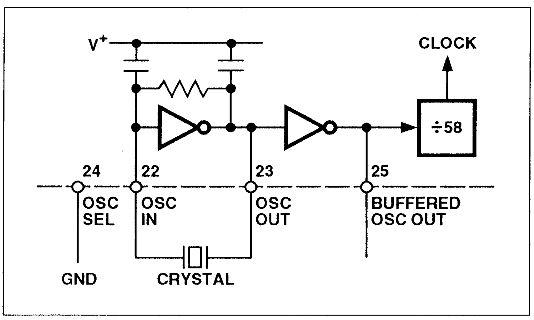


Figure 11 TC7109A Crystal Oscillator

Test Input

The counter and its outputs may be tested easily. When the TEST input is connected to GND, the internal clock is disabled and the counter outputs are all forced into the high state. When the input returns to the 1/2 (V^+–GND) voltage or to V^+ and one clock is input, the counter outputs will all be clocked to the low state.

The counter output latches are enabled when the TEST input is taken to a level halfway between V^+ and GND, allowing the counter contents to be examined anytime.

Component Value Selection

The integrator output swing for full-scale should be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full-scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly effecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common-mode voltage range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and roll-over errors will be slightly worse than in the ±4V case. For large common-mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and roll-over errors. To improve performance, ±6V supplies may be used.

Integrating Capacitor

The integrating capacitor, C_{INT}, should be selected to give the maximum integrator output voltage swing that will not saturate the integrator to within 0.3V from either supply. A ±3.5V to ±4V integrator output swing is nominal for the TC7109A, with ±5V supplies and analog common connected to GND. For 7-1/2 conversions per second (61.72 kHz internal clock frequency), nominal values C_{INT} and C_{AZ} are 0.15 μF and 0.33 μF, respectively. These values should be changed if different clock frequencies are used to maintain the integrator output voltage swing. The value of C_{INT} is given by:

$$C_{INT} = \frac{(2048 \times \text{Clock Period})\ (20\ \mu A)}{\text{Integrator Output Voltage Swing}}$$

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors give undetectable errors, at reasonable cost, up to +85°C. Teflon® capacitors are recommended for the military temperature range. While their dielectric absorption characteristics vary somewhat between units, devices may be selected to less than 0.5 count of error due to dielectric absorption.

Integrating Resistor

The integrator and buffer amplifiers have a class A output stage with 100 μA of quiescent current. They supply 20 μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2.048V full-scale a 100 kΩ resistor is recommended and for 409.6 mV full-scale a 20 kΩ resistor is recommended. R_{INT} may be selected for other values of full scale by:

$$R_{INT} = \frac{\text{Full-Scale Voltage}}{20\ \mu A}$$

Auto-Zero Capacitor

As the auto-zero capacitor is made large, the system noise is reduced. Since the TC7109A incorporates a zero integrator cycle, the size of the auto-zero capacitor does not affect overload recovery. The optimal value of the auto-zero capacitor is between 2 and 4 times C_{INT}. A typical value for C_{AZ} is 0.33 μF.

The inner foil of C_{AZ} should be connected to pin 31 and the outer foil to the RC summing junction. The inner foil of C_{INT} should be connected to the RC summing junction and the outer foil to pin 32 for best rejection of stray pickups. For low leakage at temperatures above +85°C, use Teflon capacitors.

Reference Capacitor

A 1 μF capacitor is recommended for most circuits. However, where a large common-mode voltage exists, a larger value is required to prevent roll-over error (e.g., the reference low is not analog common), and a 409.6 mV scale is used. The roll-over error will be held to 0.5 count with a 10 μF capacitor. For temperatures above +80°C use Teflon or equivalent capacitors for their low leakage characteristics.

Reference Voltage

To generate full-scale output of 4096 counts, the analog input required is $V_{IN} = 2\ V_{REF}$. For 409.6 mV full scale, use a reference of 204.8 mV. In many applications, where the ADC is connected to a transducer, a scale factor will exist between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage for the transducer is 700 mV. Instead of dividing the input down to 409.6 mV, the designer should use the input voltage directly and select V_{REF} = 350 mV. Suitable values for integrating resistor and capacitor would be 34 kΩ and 0.15 μF. This makes the system slightly quieter and also avoids a divider network on the input. Another advantage of this system occurs when temperature and weight measurements with an offset or tare are desired for non-zero input. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. In processor-based systems using the TC7109A, it may be more desirable to use software and perform this type of scaling or tare subtraction digitally.

Reference Sources

A major factor in the absolute accuracy of the ADC is the stability of the reference voltage. The 12-bit resolution of the TC7109A is one part in 4096, or 244 ppm. Thus, for the on-board reference temperature coefficient of 70 ppm/°C, a temperature difference of 3°C will introduce a one-bit absolute error. Where the ambient temperature is not controlled, or where high-accuracy absolute measurements are being made, it is recommended an external high-quality reference be used.

A reference output (pin 29) is provided which may be used with a resistive divider to generate a suitable reference voltage (20 mA may be sunk without significant variation in output voltage). A pull-up bias device is provided which sources about 10 μA. The output voltage is nominally 2.8V below V^+. When using the on-board reference, REF OUT (pin 29) should be connected to REF^- (pin 39), and REF^+ should be connected to the wiper of a precision potentiometer between REF OUT and V^+. The test circuit shows the circuit for a 204.8 mV reference, generated by a 2 kΩ precision potentiometer in series with a 24 kΩ fixed resistor.

Interfacing

Direct Mode

Combinations of chip-enable and byte-enable control signals which may be used when interfacing the TC7109A to parallel data lines are shown in Figure 12. The $\overline{\text{CE}}$/LOAD input may be tied low, allowing either byte to be controlled by its own enable (Figure 12A). Figure 12B shows the $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ as flag inputs, and $\overline{\text{CE}}$/LOAD as a master enable, which could be the READ strobe available from most microprocessors. Figure 12C shows a configuration where the two byte enables are connected together. The $\overline{\text{CE}}$/LOAD is a chip enable, and the $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ may be used as a second chip enable, or connected to ground. The 14 data outputs will be enabled at the same time. In the direct MODE, SEND should be tied to V^+.

Figure 13 shows interfacing several TC7109A's to a bus, ganging the $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ signals to several converters together, and using the $\overline{\text{CE}}$/LOAD input to select the desired converter.

Figures 14–19 give practical circuits utilizing the parallel three-state output capabilities of the TC7109A. Figure 14 shows parallel interface to the Intel MCS-48, -80 and -85 systems via an 8255 PPI, where the TC7109A data outputs are active at all times. The 8155 I/O ports may be used in an identical manner. This interface can be used in a read-after-update sequence, as shown in Figure 15. The data is accessed by the high-to-low transition of the STATUS driving an interrupt to the microprocessor.

The RUN/$\overline{\text{HOLD}}$ input is also used to initiate conversions under software control. Figure 16 gives an interface to Motorola MC6800 or MOS Technology MCS650X system.

An interrupt is generated through the Control Register B, CB1 line from the high-to-low transition of the STATUS output. The RUN/$\overline{\text{HOLD}}$ pin is controlled by CB2 through Control Register B, allowing software control of conversions.

Direct interfacing to most microprocessor busses is easily accomplished through the three-state output of the TC7109A.

Figures 1, 17 and 18 are typical connection diagrams. To ensure requirements for setup and hold times, minimum pulse widths, and the drive limitations on long busses are met, it is necessary to carefully consider the system timing in this type of interface. This type of interface is used when the memory peripheral address density is low, providing simple address decoding. Interrupt handling can be simplified by using an interface to reduce the component count.

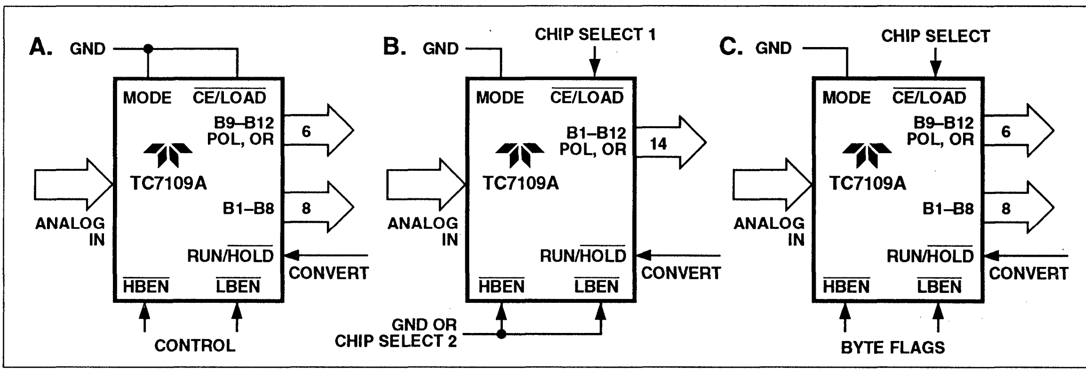


Figure 12 Direct Mode Chip and Byte Enable Combinations

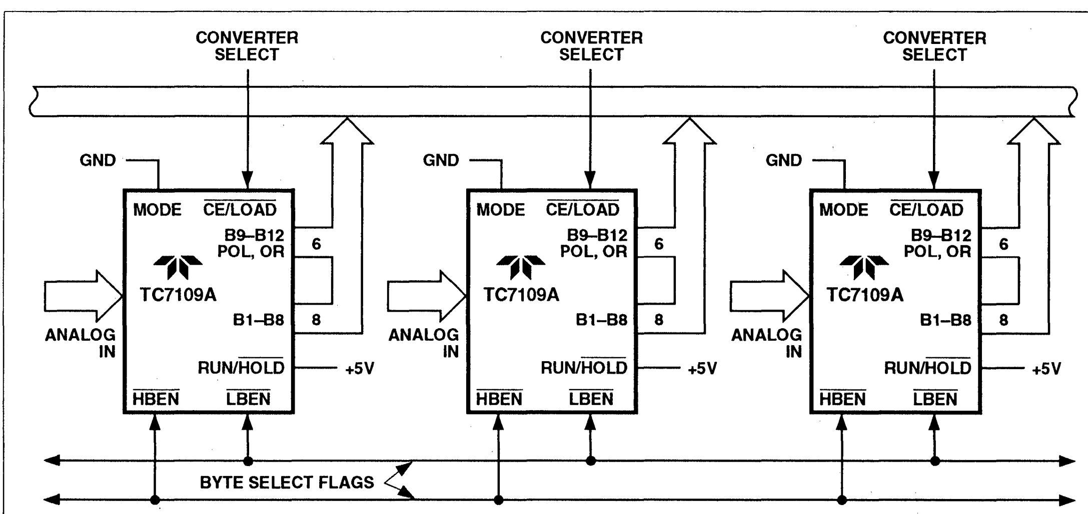


Figure 13 Three-Stating Several TC7109A's to a Small Bus

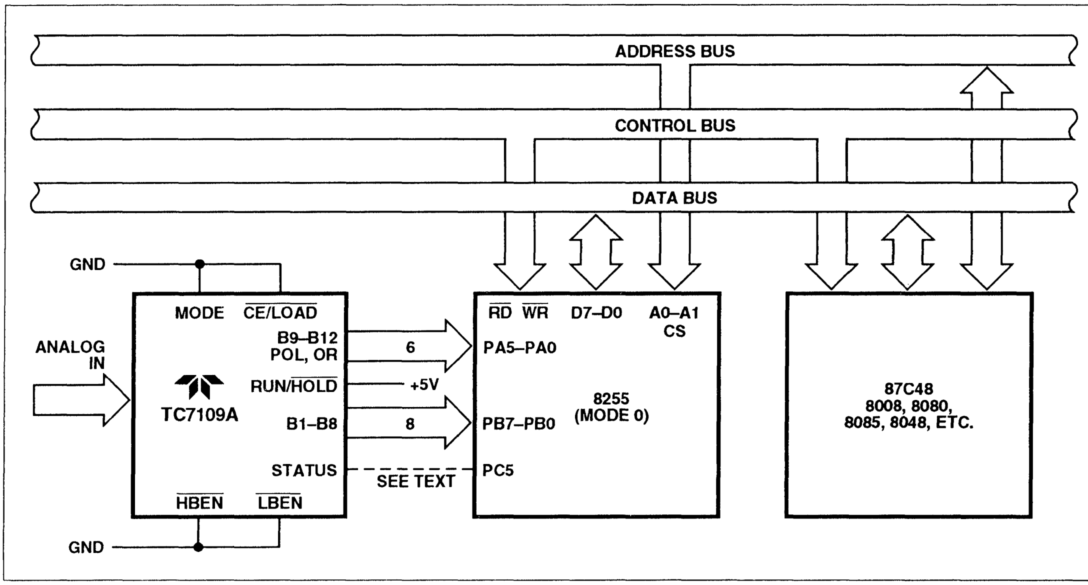


Figure 14 Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputers

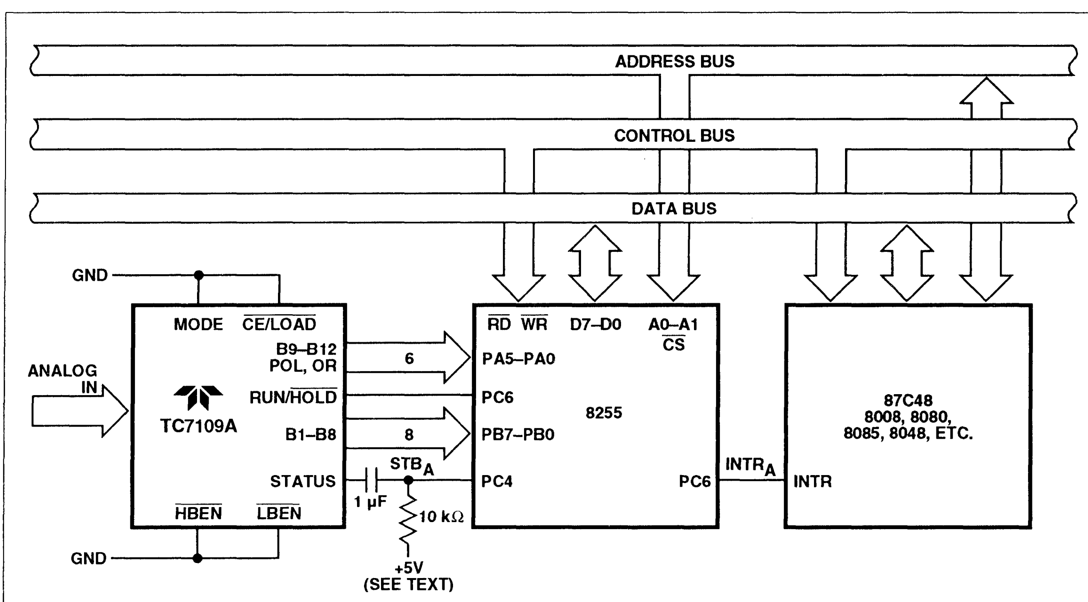


Figure 15 Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputers With Interrupt

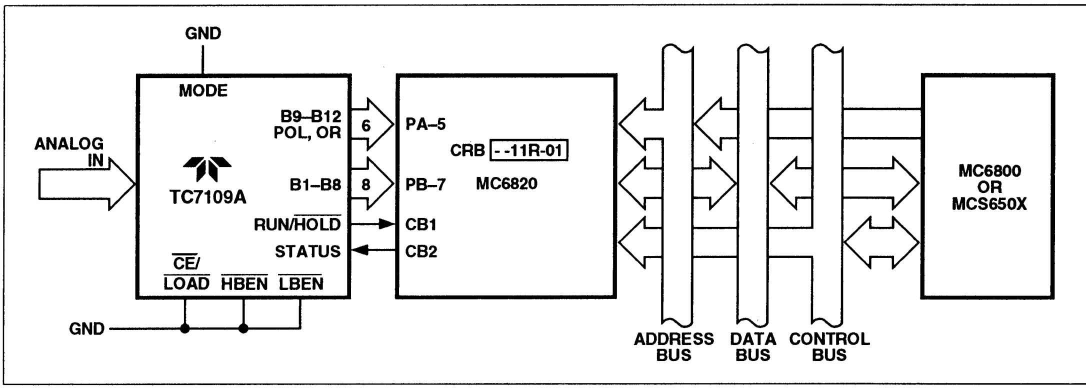


Figure 16 Full-Time Parallel Interface to MC6800 or MCS650X Microprocessor

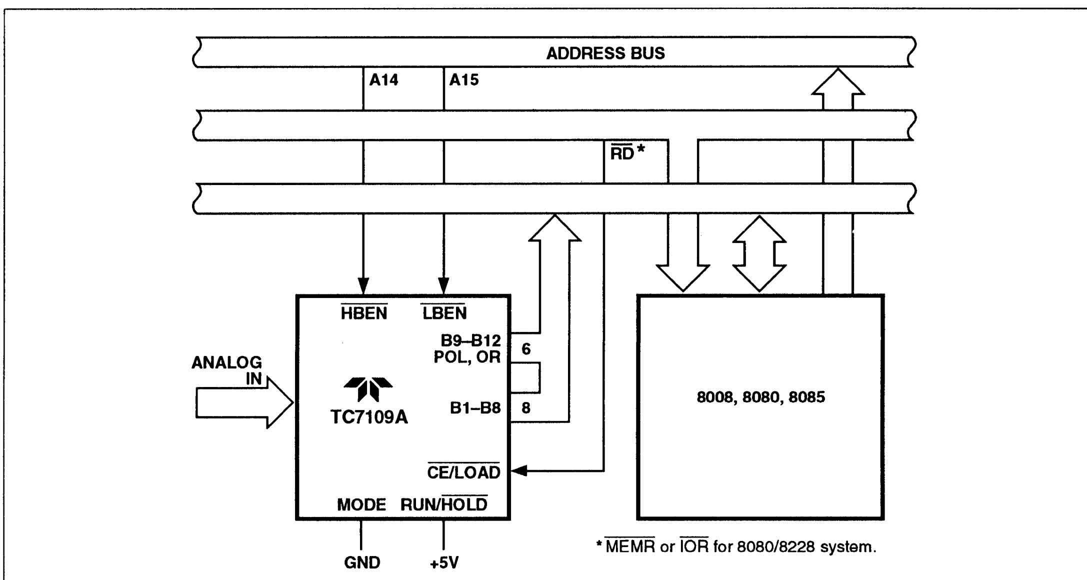


Figure 17 TC7109A Direct Interface to 8080/8085

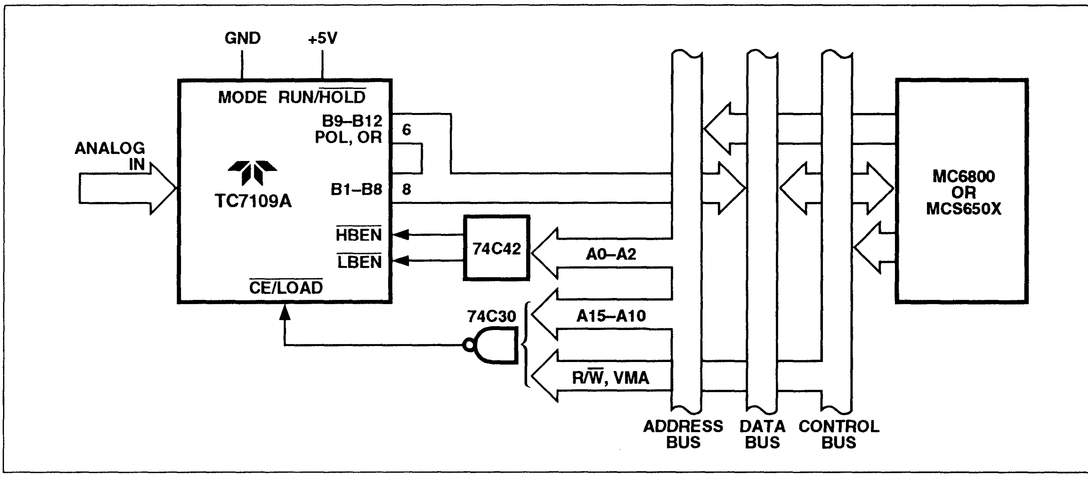


Figure 18 TC7109A Direct Interface to MC6800 Bus

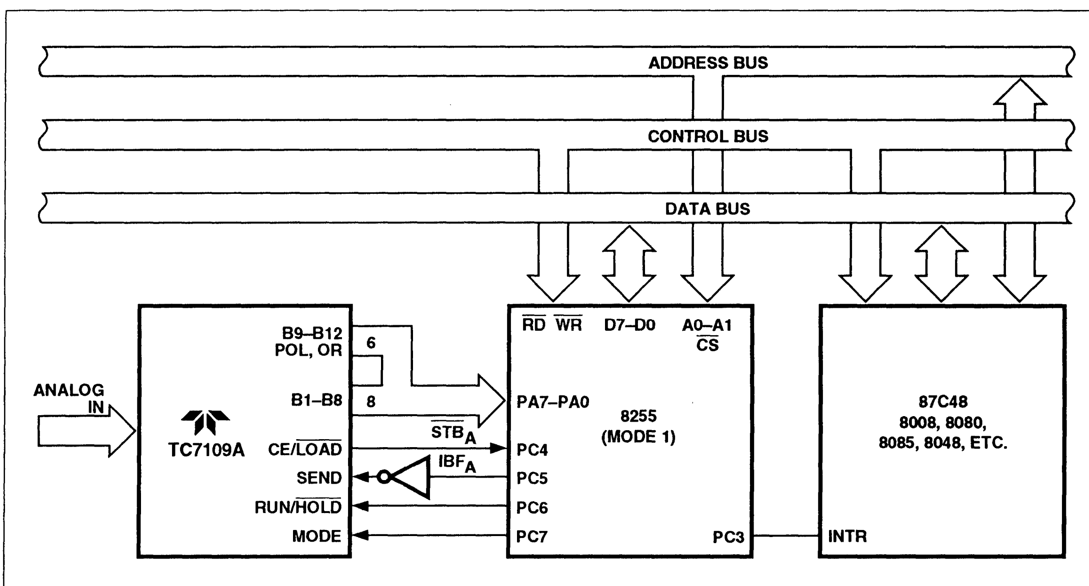


Figure 19 TC7109A Handshake Interface to MCS-48, -80, -85 Microcomputers

Handshake Mode

The handshake mode provides an interface to a wide variety of external devices. The byte enables may be used as byte identification flags or as load enables and external latches may be clocked by the rising edge of $\overline{CE}$/LOAD. A handshake interface to Intel microprocessors using an 8255 PPI is shown in Figure 19. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the TC7109A, and using the $\overline{CE/LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 8255 IBF flag is low and the TC7109A is in handshake mode, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which, when executed, will result in the data being read. The IBF will be reset low when the byte is read, causing the TC7109A to sequence into the next byte. The MODE input to the TC7109A is connected to the control line on the PPI.

The data from every conversion will be sequenced in two bytes in the system, if this output is left high, or tied high separately. (The data access must take less time than a conversion.) The output sequence can be obtained on demand if this output is made to go from low to high. and the interrupt may be used to reset the MODE bit.

Conversions may be obtained on command under software control by driving the RUN/$\overline{HOLD}$ input to the TC7109A by a bit of the 8255. Another peripheral device may be serviced by the unused port of the 8255. The 8155 may be used in a similar manner. The MCS650X microprocessors are shown in Figure 20 with MODE and RUN/$\overline{HOLD}$ tied high to save port outputs.

The handshake mode is particularly useful for directly interfacing to industry-standard UARTs (such as Western Digital TR1602), providing a means of serially transmitting converted data with minimum component count.

A typical UART connection is shown in Figure 1. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go high. The MODE input to the TC7109A goes high, triggering the TC7109A into handshake mode. The high-order byte is output to the UART and when the UART has transferred the data to the Transmitter register, TBRE (SEND) goes high again, $\overline{LBEN}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the TC7109A to the UART.

An extension of the typical connection to several TC7109A's with one UART is shown in Figure 21. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. Up to eight TC7109A's may interface with one UART, with no external components. Up to 256 converters may be accessed on one serial line with additional components.

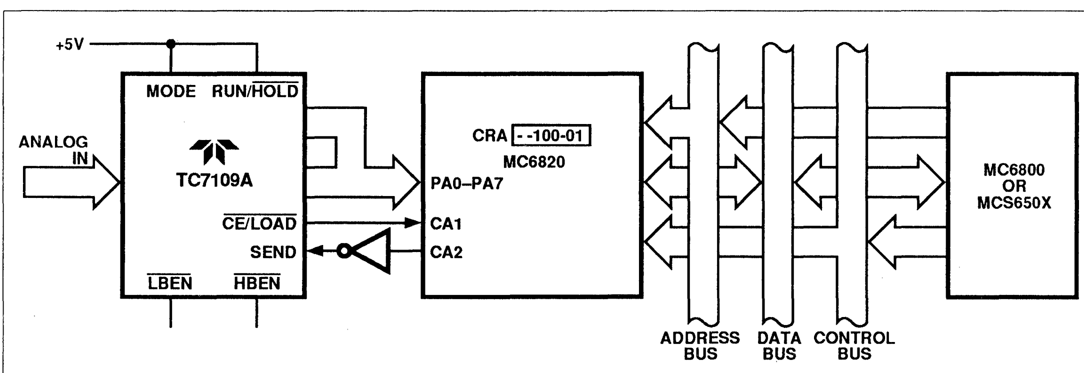


Figure 20 TC7109A Handshake Interface to MCS-6800, MCS650X Microprocessors

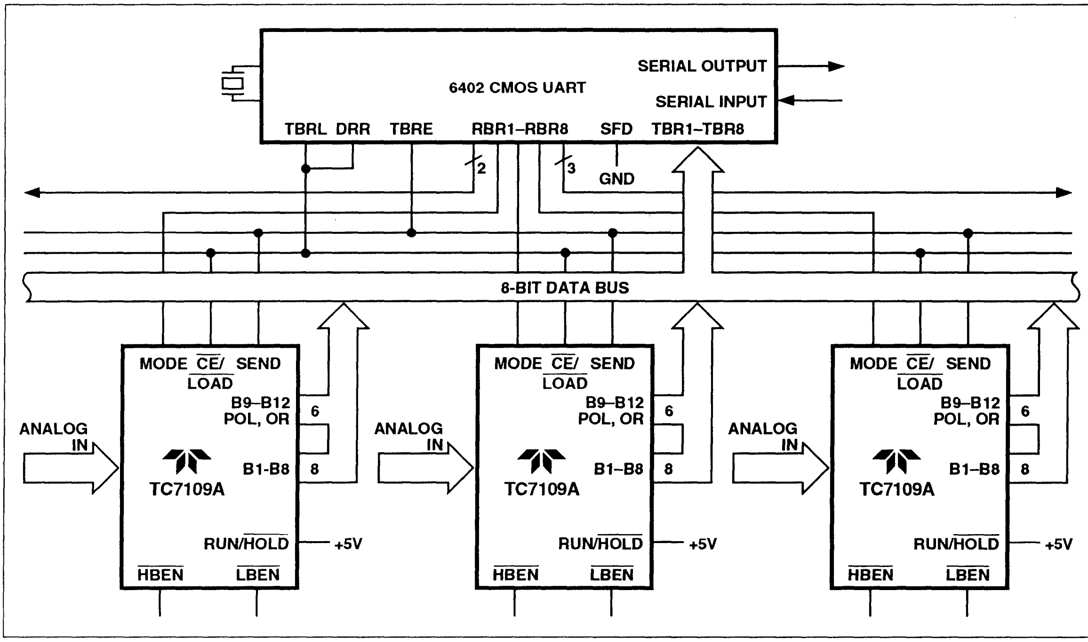


Figure 21 Handshake Interface for Multiplexed Converters

Integrating Converter Features

The output of integrating ADCs represents the integral, or average, of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter averages the effects of noise. A second important characteristic is that time is used to quantize the answer, resulting in extremely small, nonlinearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise (Figure 22).

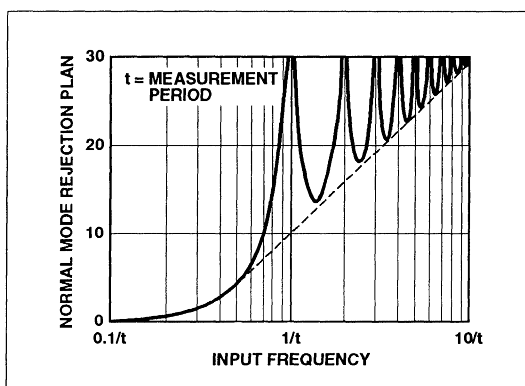
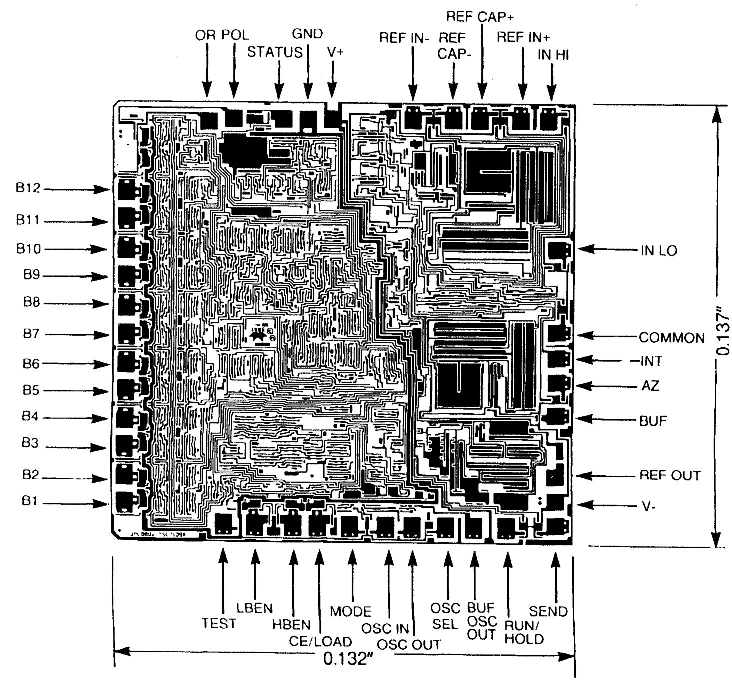


Figure 22 Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency

TC7109
TC7109A

BONDING DIAGRAM



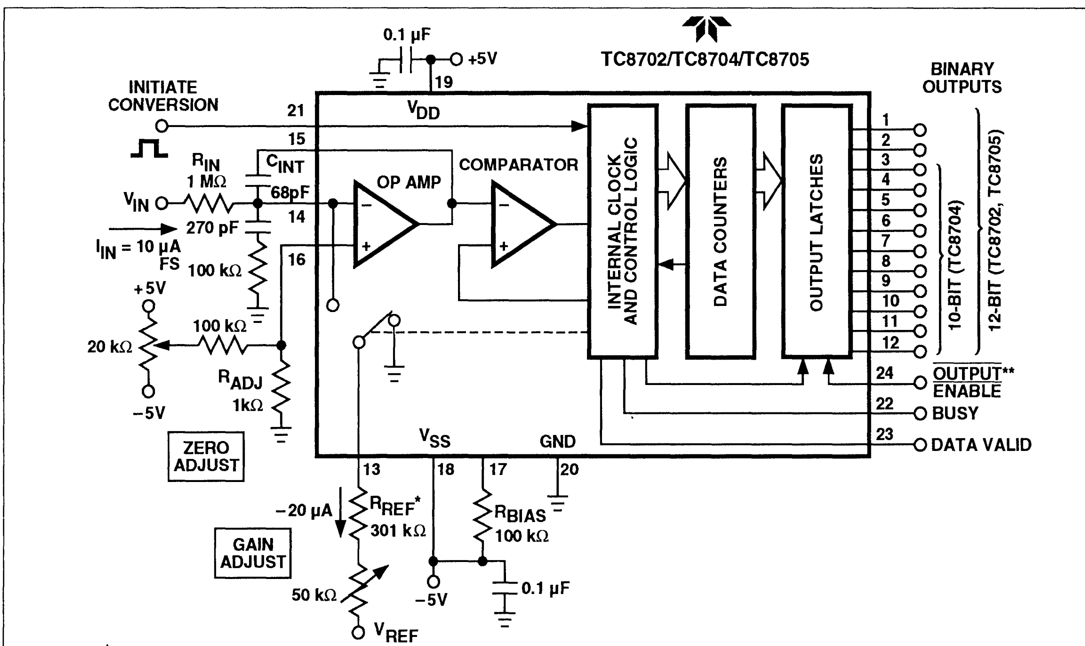
TC8702
TC8704
TC8705

BINARY OUTPUT ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- High Accuracy — Up to 12-Bit Resolution With <±1/2 LSB Error
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation ....20 mW Typ
- Contains All Required Active Elements — Needs Only Passive Support Components, Reference Voltage, and Dual-Power Supply
- High Stability Over Full Temperature Range
  - — Gain Temperature Coefficient ...<25 ppm/°C Typ
  - — Zero Drift ....<30 µV/°C Typ
  - — Differential Nonlinearity Drift.....<25 ppm/°C Typ
- Latched Parallel Binary Outputs
- Three-State, Bus Compatible Outputs (TC8704 and TC8705)
- LPTTL, 74LS, CMOS Compatible Outputs and Control Inputs
- Strobed or Free-Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

TEST CIRCUIT



NOTES: *Any V_{REF} greater than −1V can be used:

$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example, with V_{REF} = −5V, R_{REF} = 250 kΩ

**No connection for TC8702.

4344 ILL F01

TC8702
TC8704
TC8705

BINARY OUTPUT ANALOG-TO-DIGITAL CONVERTERS

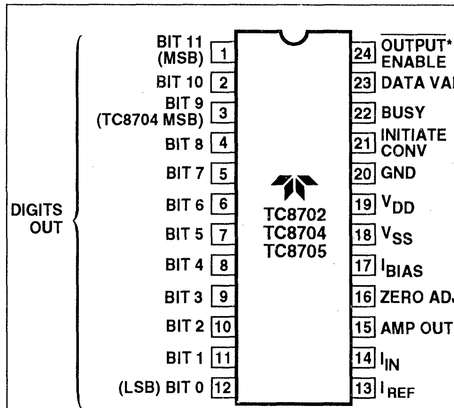
GENERAL DESCRIPTION

The TC8702/TC8704/TC8705 are 10- and 12-bit monolithic CMOS analog-to-digital converters (ADCs). Fully self-contained in a single 24-pin dual-in-line package, each converter requires only passive support components, reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero are counted. At the end of conversion, the total count is latched into the digital outputs as a 10- or 12-bit binary word.

The TC8704/8705 features a three-state output bus controlled by an output enable input. The output enable control switches to a high impedance or off-state when held high. The off-state allows bus-organized output connections. On the TC8702, outputs are always active.

PIN CONFIGURATION



NOTE: Do not make connections to pins 1 or 2 on TC8704. These pins are internally connected.

* No connection for TC8702

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ORDERING INFORMATION

Part No.	Previous Part No.	Resolution	Conversion Time (ms)	Package	Temperature Range
TC8702EHG	TSC8702CN	12-Bit	20	24-Pin CerDIP	–40°C to +85°C
TC8702MJG	TSC8702CN	12-Bit	20	24-Pin CerDIP	–55°C to +125°C
TC8704CPG	TSC8704CJ	10-Bit	5	24-Pin Plastic DIP	0°C to +70°C
TC8704EJG	TSC8704CL	10-Bit	5	24-Pin CerDIP	–40°C to +85°C
TC8704MJG	TSC8704BL	10-Bit	5	24-Pin CerDIP	–55°C to +125°C
TC8705CPG	TSC8705CJ	12-Bit	20	24-Pin Plastic DIP	0°C to +70°C
TC8705EHG	TSC8705CL	12-Bit	20	24-Pin CerDIP	–40°C to +85°C
TC8705MHG	TSC8705BL	12-Bit	20	24-Pin CerDIP	–55°C to +125°C

BINARY OUTPUT ANALOG-TO-DIGITAL CONVERTERS

TC8702 TC8704 TC8705

ABSOLUTE MAXIMUM RATINGS

$V_{DD} - V_{SS}$ .... +18V
I_{IN} .... ±10 mA
I_{REF} .... ±10 mA
Digital Input Voltage .... –0.3V to V_{DD} +0.3V
Operating V_{DD} and V_{SS} Range .... +3.5V to +7V
Storage Temperature Range .... –65°C to +150°C
Operating Temperature Range
CPG .... 0°C to +70°C
EJG .... –40°C to +85°C
MJG, MHG .... –55°C to +125°C

Package Dissipation .... 500 mW
Lead Temperature (Soldering, 10 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{DD} = +5V, V_{SS} = –5V, V_{GND} = 0, V_{REF} = –6.4V, R_{BIAS} = 100 kΩ, test circuit shown, unless otherwise specified. T_A = +25°C unless full temperature range is specified (–55°C to +125°C for MJG and MHG packages, –40°C to +85°C for EJG package, 0°C to +70°C for CPG package).

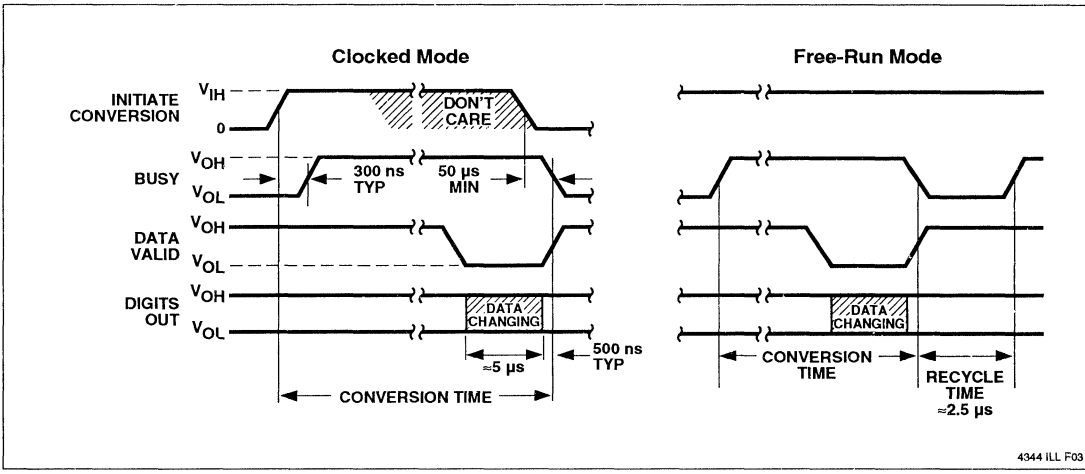
Parameter	Test Conditions	Definition	Min	Typ	CP/EJ Max	MJ/MH Max	Unit
Accuracy							
Resolution Accuracy							
TC8704		Binary Word Length of	10	—	—	—	Bits
TC8702/TC8705		Digital Output	12	—	—	—	Bits
Relative Accuracy		Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	±1/4	±1/2	±1/2	LSB
		(TC8705CPG Only)	—	1	±1.5	—	LSB
Differential Nonlinearity		Deviation From 1 LSB Between Transition Points	—	±1/4	±1/2	±1/2	LSB
Differential Nonlinearity Temperature Drift	Full Temperature Range	Variation in Differential Nonlinearity Due to Temperature Change	—	±2.5	±5	±5	ppm/°C
Gain Variance		Variation From Exact A (Compensate by Trimming R_{IN} or R_{REF})	—	±2	±5	±5	% of Nominal
Gain Temperature Drift	Full Temperature Range	Variation in A Due to Temperature Change	—	±25	±75	±80	ppm/°C
Zero Offset	I_{IN} = 0, C_{INT} = 68 pF, R_{ADJ} = 1 kΩ (See Test Circuit)	Correction at Zero Adjust to Give Zero Output When Input is Zero	—	±10	±50	±50	mV
Zero Temperature Drift	Full Temperature Range	Variation in Zero Offset Due to Temperature Change	—	±3	±5	±8	ppm/°C
Analog Input (See Note)							
I_{IN} Full Scale		Full-Scale Analog Input Current to Achieve Specified Accuracy	—	10	—	—	μA
I_{REF}		Reference Current Input to Achieve Specified Accuracy	—	–20	—	—	μA
Digital Input							
$V_{IN}^{(1)}$	Full Temperature Range	Logic "1" Input Threshold for Initiate Conversion Input	3.5	—	—	—	V
$V_{IN}^{(0)}$	Full Temperature Range	Logic "0" Input Threshold for Initiate Conversion Input	—	—	1.5	1.5	V

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Test Conditions	Definition	Min	Typ	CP/EJ Max	MJ/MH Max	Unit
Propagation Delay							
Output Enable (TC8704, TC8705)	C_L = 100 pF, R_L = 1 kΩ	t_{PLH}, t_{PHL}	—	500	—	1000	ns
Digital Output							
$I_{O(OFF)}$ (TC8704, TC8705)	OE = 3.5V 0.4V < V_C < 2.4V	Off-State Output Current	—	0.1	±10	±10	µA
$V_{OUT}^{(1)}$	Full Temperature Range, I_{OUT} = –10 µA I_{OUT} = –500 µA	Logic "1" Output Voltage for Digits Out, Busy, and Data Valid Outputs	4.5 2.4	— —	— —	— —	V V
$V_{OUT}^{(0)}$	Full Temperature Range, V_{DD} = 4.75V I_{OUT} = 500 µA	Logic "0" Output Voltage for Digits Out, Busy, and Data Valid Outputs	—	—	0.4	0.4	V
Dynamic							
Conversion Time TC8704 TC8702, TC8705	Full Temperature Range	Time Required to Perform One Complete A/D Conversion	 — —	 5 20	 6 24	 6 24	 ms ms
Conversion Rate in Free-Run Mode TC8704 TC8702, TC8705	$V_{INT\ CONV}$ = +5V		 167 42	 200 50	 — —	 — —	 sec
Minimum Pulse Width for Initiate Conversion	Full Temperature Range		500	—	—	—	ns
Supply Current							
I_{DD} Quiescent J/H Packages P Package	Full Temperature Range, $V_{INT\ CONV}$ = 0V	Current Required From Positive Supply During Operation	 — —	 1.4 1.4	 2.5 5	 3.5 —	 mA mA
I_{SS} Quiescent J/H Packages P Package	Full Temperature Range, $V_{INT\ CONV}$ = 0V	Current Required From Negative Supply During Operation	 — —	 –1.6 –1.6	 –2.5 –5	 –3.5 —	 mA mA
Supply Sensitivity	V_{DD} ±1V, V_{SS} ±1V	Change in Full-Scale Gain vs Supply Voltage Change	—	±0.5	±1	±1	%/V
	$\lvert V_{DD}\rvert = \lvert V_{SS}\rvert$ = 5V ±1V	Change in full-Scale Gain vs Supply Voltage Change for Tracking Supplies	—	±0.05	±0.1	±0.1	%/V

NOTE: I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See "Test Circuit."

TIMING DIAGRAMS



CIRCUIT DESCRIPTION

During conversion, the sum of a continuous current (I_{IN}) and pulses of a reference current (I_{REF}) is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the output of the integrator near zero. Thus, the charge from the continuous I_{IN} is balanced against the pulses of I_{REF}. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in binary) is latched into the outputs at the end of the conversion.

The converter contains two counters and a clock, in addition to an operational amplifier, comparator, latching output buffers, and housekeeping logic. One counter is a clock counter which starts counting clock pulses after a reset pulse; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times I_{REF} is switched into the summing input of the amplifier during the period defined by the clock counter.

When the initiate conversion input is strobed with a positive signal, the busy line latches high and a 10 µs (times given are approximate) start-up cycle begins. The integrating capacitor is discharged and both counters are reset during this start-up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 µs shutdown cycle. During the shutdown cycle, data valid goes low for 5 µs. This binary sequence is shown in the timing diagrams. Busy is true high and, when the circuit is busy, initiate conversion has no effect and may be high or low. Data valid is also true high. The data from a conversion remains valid for as long as power is applied to the circuit or until data valid falls at the end of a subsequent conversion, at which time the output data is updated to reflect the latest conversion.

PIN FUNCTIONS

Initiate Conversion Input

Accepts CMOS and most +5V logic inputs. Applying a logic "1" to the initiate conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the initiate conversion pin is disabled until conversion is complete. Two modes of operation are permitted: clocked or free-running. For clocked operation, the initiate conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation, the initiate conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low-power TTL (can sink and source 500 µA). A logic "1" output on the busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates conversion is complete and the result has been latched at the digit out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the busy output will remain low for approximately 2.5 μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low-power TTL (can sink and source 50 μA). A logic "1" output at the data valid pin indicates the digits out pins are latched with the result of the last conversion cycle. The data valid output goes to logic "0" approximately 5 μs before the completion of a conversion cycle. During this 5 μs interval new data is being transferred to the digits out pins, and the digits out are not valid.

Digits Out

The binary digit outputs (Bit 0 . . . Bit 11) which are the result of the A/D conversion. These outputs are CMOS logic and low-power TTL compatible.

APPLICATIONS INFORMATION

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital counts} = \frac{V_{IN} \bullet A \bullet R_{REF}}{R_{IN} \bullet V_{REF}},$$

A = 2064 for TC8704; 8208 for TC8702/TC8705

where digital counts is the value of the binary output word presented at digits out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Outputs MSB LSB
$V_{IN} \leq$ Full Scale	1 . . . 111 . . . 1
= Full Scale –1 LSB	1 . . . 111 . . . 1
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection

Obtaining a high-accuracy conversion system depends on the voltage regulation of V_{REF} and thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. Supply connections V_{DD} and V_{SS} should have bypass capacitors of 0.1 μF value, or larger, at the device pins.

R_{IN}, R_{REF}

Values of these components are chosen to give a full-scale input current of approximately 10 μA and a reference current of approximately –20 μA:

$$R_{IN} \cong \frac{V_{IN}\ \text{Full Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}.$$

Examples:

$$R_{IN} \cong \frac{10V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} full scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high-accuracy applications because of their thermal stability and low-noise generation.

R_{BIAS}

Specifications for the TC87XX are based on R_{BIAS} = 100 kΩ ±10%, unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS}, the A/D will convert much faster and the supply current will be higher. For example, when R_{BIAS} is 20kΩ, the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA. Likewise, if R_{BIAS} is increased, the conversion time will be longer and the supply current will be much lower. For example, when R_{BIAS} = 1 MΩ, the conversion time will be six times longer, and supply current is now reduced to 0.5 mA. For details of this relationship, refer to AN–9 typical performance curves.

R_{DAMP}

The exact value is not critical, but should have a nominal value of 100Ω ±10%. Locate close to pin 14.

C_{DAMP}

The exact value is not critical, but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

The exact value is not critical, but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14 and 15.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5V are recommended, with 0.05% line and load regulation, and 0.1 μF decoupling capacitors.

Adjustment Procedure

The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e., below zero and above full scale), it is recommended transition points be used in setting the zero and full-scale values. The recommended procedure is:

(1) Set initiate conversion control high to provide free-run operation and verify converter is operating.

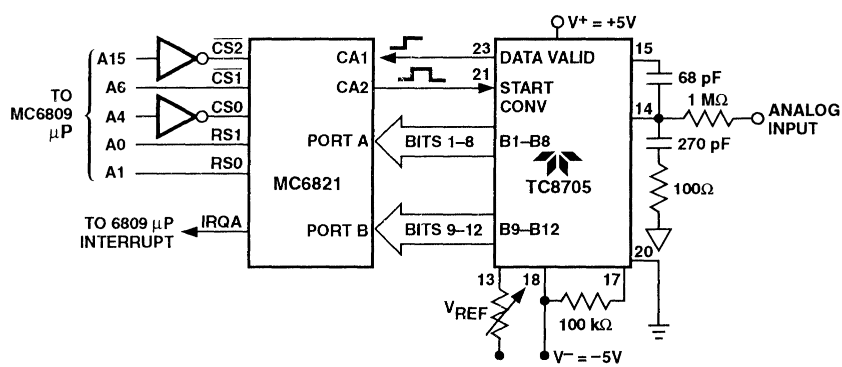
(2) Set V_{IN} to +1/2 LSB and trim the zero-adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.

(3) For full-scale adjustment, set V_{IN} to the full-scale value less 1-1/2 LSB and trim the gain-adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

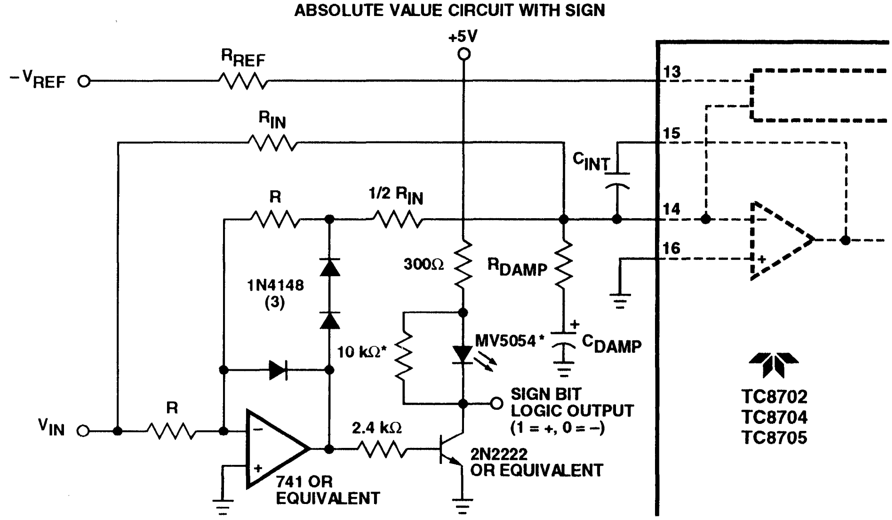
TYPICAL APPLICATION/DESIGN CIRCUITS

TC8705 Interface to MC6821 PIA



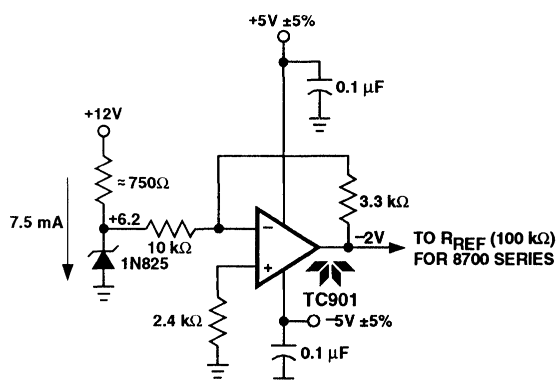
TYPICAL APPLICATION/DESIGN CIRCUITS (Cont.)

Bipolar Operation (+ and – Inputs)



*Optional visual indication of negative input.
NOTE: Values for R should be between 10 kΩ and 100 kΩ.

Reference Voltage Supply



NOTE: V_{REF} = 2V using voltages derived from 8080A µP.

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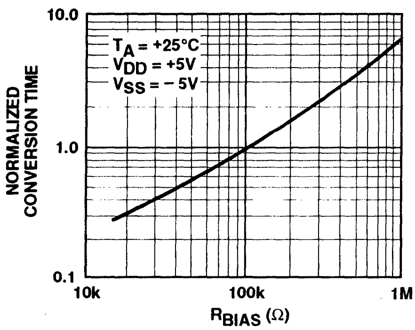
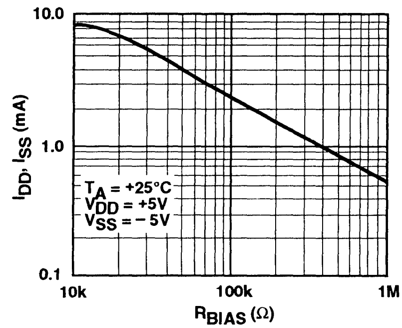
TYPICAL PERFORMANCE CURVES

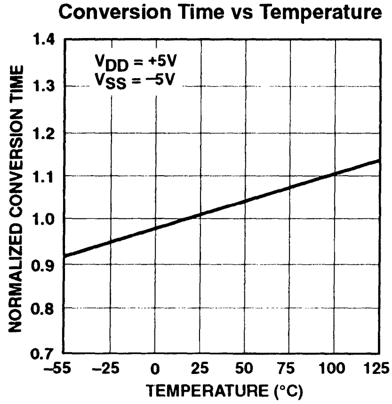
Conversion Time vs R_{BIAS}



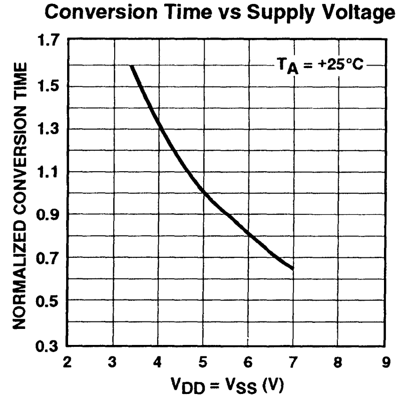
Supply Current vs R_{BIAS}



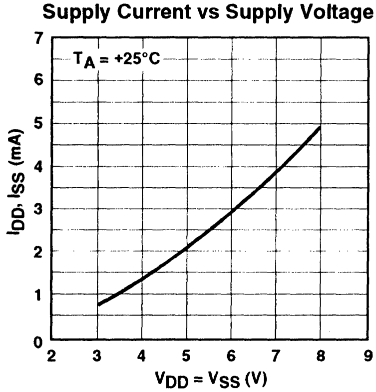
Conversion Time vs Temperature



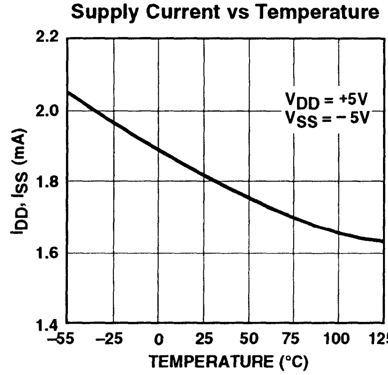
Conversion Time vs Supply Voltage



Supply Current vs Supply Voltage



Supply Current vs Temperature



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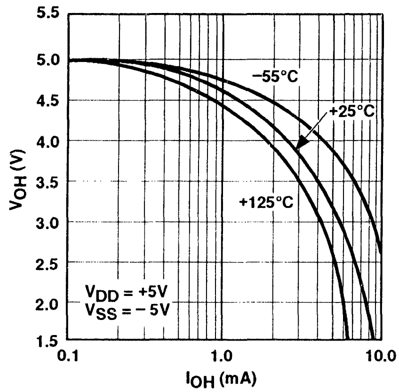
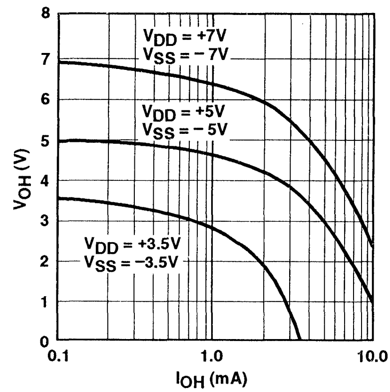
TYPICAL PERFORMANCE CURVES (Cont.)

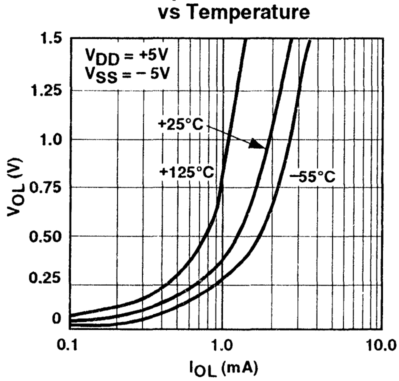
Output Source Current vs Temperature



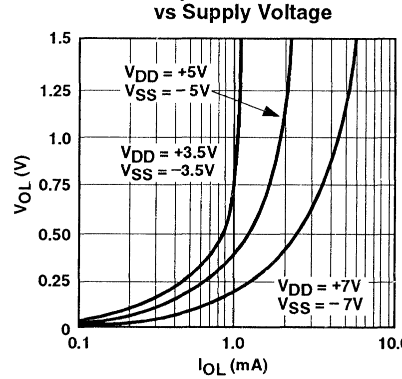
Output Source Current vs Supply Voltage



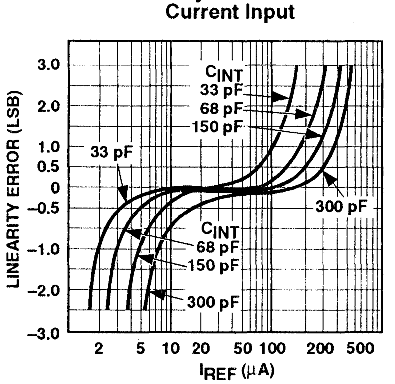
Output Sink Current vs Temperature



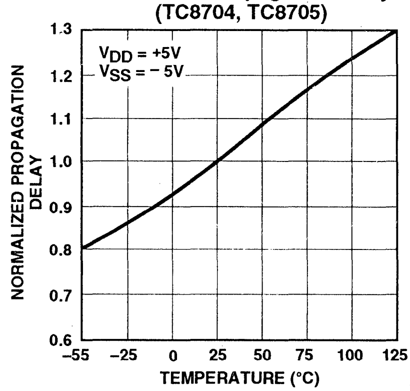
Output Sink Current vs Supply Voltage



Linearity vs Reference Current Input



Three-State Propagation Delay (TC8704, TC8705)



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Section 3

Voltage-to-Frequency/ Frequency-to-Voltage Converters

TELEDYNE COMPONENTS

4731
4733

3

HIGH-RELIABILITY HYBRID VOLTAGE-TO-FREQUENCY CONVERTERS

FEATURES

- **Power Supply Range** .... ±9V to ±18V
- **Ultra-Linear**
- **Overrange** 100%
- **Dynamic Range** .... 126 dB
- **Common-Mode Rejection Ratio** .... 60 dB
- **Low Full-Scale Drift**
- **Low Zero-Offset Voltage Drift**
- **TTL, CMOS, HNIL Compatible Output**

APPLICATIONS

- **No Drift Integrate/Hold**
- **High Common-Mode Voltage Isolation**
- **2-Wire Digital Transmission**
- **20-Bit Analog-to-Digital Converters**
- **Optical Data Link**

GENERAL DESCRIPTION

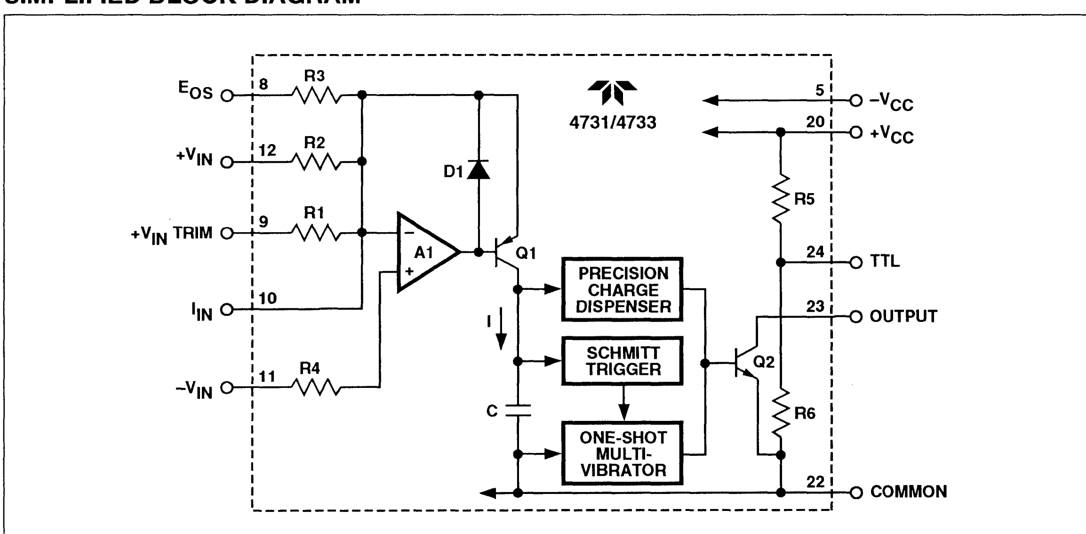
The 4731 and 4733 low-drift voltage-to-frequency (V-to-F) converters produce output pulse trains whose repetition rate is a precision linear function of the input voltage. These low-drift, ultra-linear devices can handle positive, negative and differential input signals, and can operate with a wide range of power supply voltages.

With 126 dB of dynamic range, 70 dB CMRR, and 100% overrange, these devices provide linear operation with input voltages from ±10 µV to +20V. Their current input pin (actually the summing point of an op amp) can resolve currents as low as 1000 pA, making it possible to operate with full-scale input voltages from less than 250 mV to greater than 100V.

Their 0.002% nonlinearity is the equivalent of 16-bit end-point linearity. Differential nonlinearity and dynamic range approach 20 bits.

The 4731 and 4733 are packaged in 24-pin hermetic metal packages. Standard devices are specified for 0°C to +70°C operation. The High Reliability (HR) versions are specified for –55°C to +125°C operation.

SIMPLIFIED BLOCK DIAGRAM

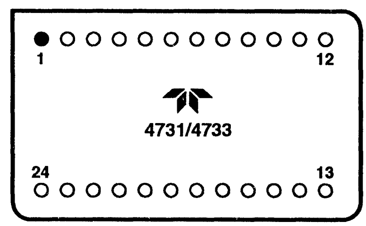


1061-1

PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	NC	24	TTL
2	NC	23	f_{OUT}
3	NC	22	COMMON
4	NC	21	NC
5	$-V_{cc}$	20	$+V_{CC}$
6	NC	19	NC
7	NC	18	NC
8	E_{OS}	17	NC
9	$+V_{IN}$ TRIM	16	NC
10	I_{IN}	15	NC
11	$-V_{IN}$	14	NC
12	$+V_{IN}$	13	NC

NC = No internal connection



ABSOLUTE MAXIMUM RATINGS

V_{CC} Power Supplies .... ±18V
$+V_{IN}$ Positive Input Voltage (Note 1) .... ±21V
$-V_{IN}$ Negative Input Voltage .... $\pm V_{CC}$
V_{ID} Differential Input Voltage (Note 1) .... V_{CC}
I_{IN} Current Input .... 210 μA
T_C Specified Temperature Range (Case)
4731/4733 .... 0°C to +70°C
4731-HR/4733-HR .... –55°C to +125°C
T_{STG} Storage Temperature Range ..... –65°C to +150°C

ELECTRICAL CHARACTERISTICS: T_C = +25°C, $\pm V_{CC}$ = ±15V, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
$+V_{IN}$	Positive Input Voltage		—	10	20	V
$-V_{IN}$	Negative Input Voltage		-8	–10	—	V
V_{CM}	Common-Mode Input Voltage		-7	—	+7	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±6V, V_{DIFF} = 0.5V	60	—	—	dB
V_{ID}	Differential Input Voltage	Referenced to $-V_{IN}$ (Note 1)	—	10	—	V
I_{IN}	Current Input Range		.001	—	120	μA
	Input Dynamic Range		100	—	—	dB
V_{OS}	Input Offset Voltage	Adjustable to Zero	—	±1	±5	mV
V_{OS}/TC	Input Offset Voltage vs Temperature	–25°C to +85°C	—	±6	±20	μV/°C
		+25°C to +125°C } Typical for standard	—	±20	±100	μV/°C
		+25°C to –55°C } tested for HR	—	±20	±50	μV/°C
R_{+IN}	$+V_{IN}$ Input Impedance		75	100	125	kΩ
R_{-IN}	$-V_{IN}$ Input Impedance		10	100	—	MΩ
$R_{I\ IN}$	Current Input Impedance	Virtual Ground	—	<0.1	—	Ω

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
Output							
V_{OH}	Output High Voltage		I_{OH} = 4 mA	**2.4**	—	**5.0**	**V**
V_{OL}	Output Low Voltage		I_{OL} = −16 mA	—	—	**0.4**	**V**
R_O	Output Impedance			2.8	3.5	4.2	kΩ
Transfer							
f_{OUT}	Output Frequency		ΔV_{IN} Equals $V_{IN} - (-V_{IN})$	$[\Delta V_{IN} \times fA] \div 10V$			kHz
				$[I_{IN} \times fA] \div I_{FS}$			kHz
fA	Scaling Frequency	4731	Adjustable to Typical	**9.95**	**10**	**10.05**	**kHz**
		4733	Adjustable to Typical	**99.5**	**100**	**100.5**	**kHz**
fA/TC	fA vs Temperature	4731	-55°C to +125°C	—	±8	±50	ppm/°C
			-25°C to +85°C	—	±7	±25	ppm/°C
		4733	-55°C to +125°C	—	±12	±50	ppm/°C
			-25°C to +85°C	—	±10	±30	ppm/°C
	fA vs Time	Per Day		—	±10	—	ppm/D
		Per Month		—	±30	—	ppm/M
I_{FS}	Full-Scale Current			75	100	125	µA
I_{FS}/TC	I_{FS} vs Temperature	4731	+25°C to +85°C	—	±4	—	ppm/°C
			+25°C to −25°C	—	±7	—	ppm/°C
		4733	+25°C to +85°C	—	±6	—	ppm/°C
			+25°C to −25°C	—	±10	—	ppm/°C
	I_{FS} vs Time	Per Day		—	±10	—	ppm/D
		Per Month		—	±30	—	ppm/M
$+V_{INLE}$	$+V_{IN}$ Linearity Error (Note 2)		V_{IN} = 100 µV to 12V	**—**	**±0.002**	**±0.005**	**%FS**
			−55°C to +125°C } Tested for	**—**	**±0.005**	**±0.03**	**%FS**
			−25°C to +125°C } HR only	**—**	**±0.005**	**±0.01**	**%FS**
$-V_{INLE}$	$-V_{IN}$ Linearity Error (Note 2)		V_{IN} = −100 µV to ($-V_{CC}$ +7V)	—	±0.01	±0.02	%FS
I_{INLE}	I_{IN} Linearity Error (Note 2)		I_{IN} = 1 nA to 120 µA	—	±0.002	±0.005	%FS
t_{PW}	Output Pulse Width	4731		10	—	30	µs
		4733		1	—	3	µs
	Warm-Up Time		0.01% Accuracy	—	1	—	s
			0.002% Accuracy	—	100	—	s
Dynamic							
t_S	Settling Time			1 to 2 Pulses@New Freq+(5 µs)			
	Overload Recovery		ΔV_{IN} = 100V to 10V or ΔI_{IN} = 1 mA to 0.1 mA	—	0.14	1	ms
Power Supplies							
V_{CC}	Voltage Range			±9	±15	±18	V
	Voltage Asymmetry		$\lvert V_{CC}\rvert - \lvert -V_{CC}\rvert$	—	—	±2	V
I_{CC}	Quiescent Current			**—**	**±17**	**±25**	**mA**
$PSRR_1$	f_A vs Power Supplies			—	±10	±20	ppm/%
$PSRR_2$	I_{FS} vs Power Supplies			—	±10	±20	ppm/%
$PSRR_3$	V_{OS} vs Power Supplies		Constant Voltage at Pin 8	—	±3	±20	µV/%

NOTES: 1. $+V_{IN}$ has a 100 kΩ internal resistor and a 210 µA maximum input current limit. The voltage input, if current-limited by a series input resistor, is virtually unlimited.
2. Linearity specifications apply only after offset and gain have been trimmed to nominal.
3. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

THEORY OF OPERATION

To take maximum advantage of the 4731/4733's versatility, a functional block diagram and theory of operation are provided herein. With this information, input and output circuitry is easily modified to handle virtually any input signal or output load.

The 4731 and 4733 are free-running (astable), voltage-controlled multivibrators (see Block Diagram). The effective currents from the four inputs ($+V_{IN}$, $+V_{IN}$ TRIM, $+I_{IN}$ and E_{OS}) are summed at the inverting input of op-amp A1. A1 and transistor Q1 form a precision current pump, producing current (I). Current charges capacitor C at a rate which is a precise linear function of the device's input signal.

When the voltage impressed on C (due to I) reaches a fixed precision threshold, the Schmitt trigger output changes state and triggers the one-shot (monostable) multivibrator, which in turn produces a single constant-width output pulse. This pulse performs two functions. Amplified by Q2, it is the output of the V-to-F converter and also activates the precision charge dispenser (PCD). The PCD discharges C to the same "zero" level every time an output pulse is produced. Thus, capacitor C is repeatedly charged and discharged between two precise voltages at a rate which is a linear function of the device's voltage and/or current input signal. This action produces the waveforms shown in the timing diagram of Figure 11.

TRIM THEORY

The V-to-F input circuit zero and full-scale trim are performed at the input circuit amp A1 (see block diagram). The user may treat the V-to-F input as an operational amplifier, within certain limits.

No signal combination should be applied to the V-to-F inputs which will drive the A1 output positive. A frequency output will not result if total current into the V-to-F positive inputs (A1, summing point) becomes negative with respect to the V-to-F negative input. If this occurs, D1 becomes forward-biased, Q1 will cut off, and current (I) and f_{OUT} will be zero.

The inherent input current full-scale factor is 100 μA ±25% for a full-scale output. All current adjustment trimming must take this ±25% tolerance into account. Resistor R1 (see block diagram) is factory laser trimmed so that a full-scale input to $+V_{IN}$ TRIM (pin 9) produces an output 101% ±0.5% of nominal full scale; i.e., a +10V input to $+V_{IN}$ TRIM of the 4731 produces a 10.1 kHz ±0.05 kHz output. Resistor R2 is factory trimmed so that $+V_{IN}$ is within ±0.5% of nominal full scale; i.e., a +10V input to $+V_{IN}$ of the 4731 produces a 10 kHz ±0.05 kHz output. Both $+V_{IN}$ and $+V_{IN}$ TRIM inputs are trimmed with and specified for V_{CC} = ±15V at 25°C.

Basic Connections

The 4731 and 4733 are factory trimmed and operate as specified without additional components. Figures 1 and 2 illustrate the basic connections for positive or negative input signals and also show the optional offset adjustment connection. Pin 9 ($+V_{IN}$ TRIM) and pin 12 ($+V_{IN}$) are inputs for positive voltage signals. $+V_{IN}$ is used when accuracy to ±0.1% full scale is acceptable or when external components cannot be accommodated. $+V_{IN}$ TRIM is used when greater full-scale accuracy is required because it allows the use of an external trim adjustment potentiometer. Pin 10 (I_{IN}) is a direct input to the input amplifier summing junction, and is used to input positive-current signals. Its full-scale accuracy is limited to ±25% of the inherent input current full-scale factor mentioned earlier. Pin 11 ($-V_{IN}$) can be used to input negative voltage signals, as shown in Figure 2.

Zero and Full-Scale Trim

When greater accuracy is required, input offset voltage (E_{OS}) is trimmed to zero. For positive inputs only, full-scale output frequency (f_{OUT}) is trimmed to 10 kHz or 100 kHz, depending on the device being used, with external potentiometers (illustrated in Figures 1 and 2). Note that full-scale trim components should have temperature coefficients similar to the full-scale TC of the device being used.

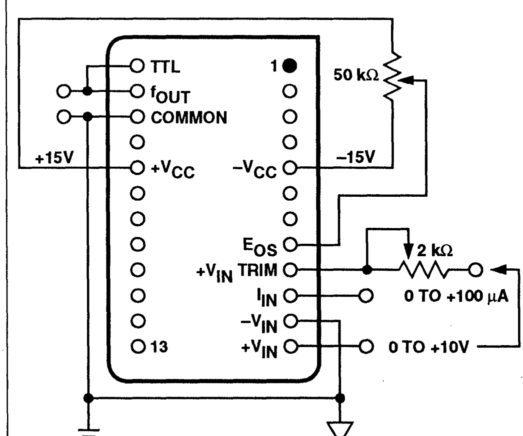


Figure 1. Positive Voltage/Current Inputs

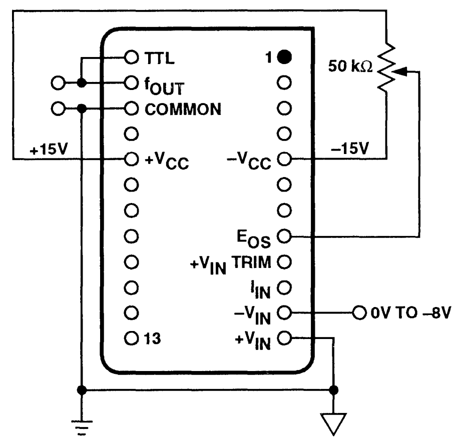


Figure 2. Negative Voltage Input

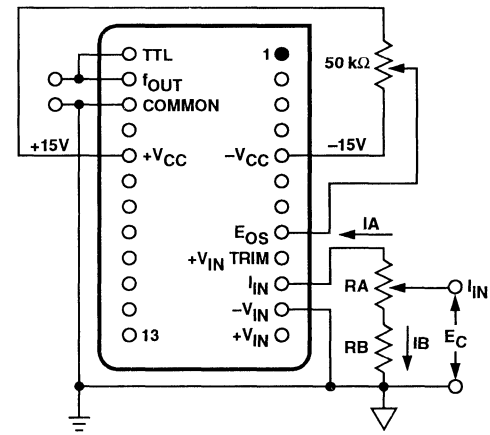


Figure 3. Zero and Full-Scale Trim for Positive Input Currents

TRIM PROCEDURES

1. Apply 10 mV between $+V_{IN}$ and ground. Adjust the 50 kΩ potentiometer to set f_{OUT} equal to 10 Hz (4731) or 100 Hz (4733).
2. Apply +10V between $+V_{IN}$ and ground. Adjust R1 to set f_{OUT} equal to 10 kHz (4731) or 100 kHz (4733).
3. Repeat (1) and (2) until zero and full scale are set precisely. **Note:** Zero is set at 10 Hz to 100 Hz out for 10 mV in, because it is impractical to measure 0 Hz out for 0V in.

Full-scale accuracy for $+I_{IN}$ is ±25%. Greater accuracy is obtained by using the full-scale and zero trim circuit shown in Figure 3. Resistor dividers RA and RB are only used when the actual input current is greater than that necessary to produce a nominal full-scale output frequency.

FULL-SCALE FACTOR CHANGE

The specified input voltage full-scale factor for the 4731 and 4733 is 9.9V ±0.5% with respect to $-V_{IN}$ (or +100 μA ±25% I_{IN}) to produce a full-scale output frequency. Many applications require a full-scale output for other (larger or smaller) full-scale input signals or input polarities. Figures 4, 5 and 6 illustrate how to operate with such input signals.

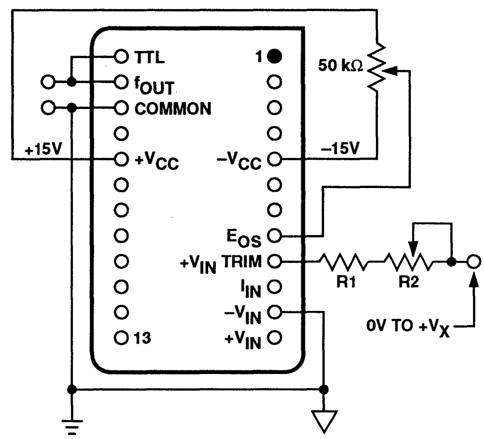
–8V > V_{IN} > +10V

This series of V-to-F converters can be operated with input voltages greater than +10V by connecting a fixed resistor and trim potentiometer in series with the $+V_{IN}$ or $+V_{IN}$ TRIM inputs (see Figure 4). The same effect can be realized by using a properly selected series resistor and inputting the signal to the current input ($+I_{IN}$). For inputs more negative than –8V, the attenuator network of Figure 5 performs well. For either positive or negative inputs the zero trim and other adjustments remain the same as in Figures 1 and 2.

–10V < Full-Scale V_{IN} < +10V

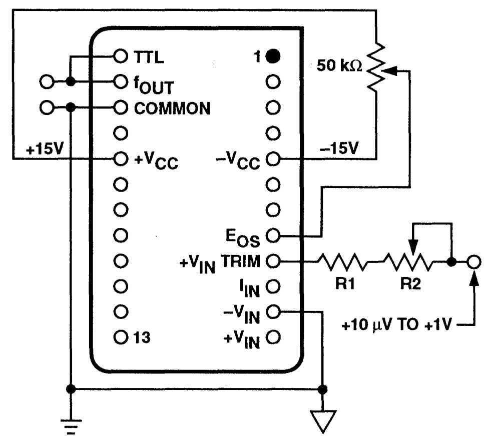
If full-scale input voltage is between +10 μV and +1V, the full-scale output is set to nominal full scale by using the current-input terminal with a series resistor, as shown in Figure 6.

If full-scale input signal is between –10V and –10 μV, a low-drift amplifier (such as the 1435) should be used to amplify the signal full scale to –10V, or even +10V, and then apply the signal as usual (i.e., Figures 1 and 2). This preamplification technique can also be used with positive input signals.



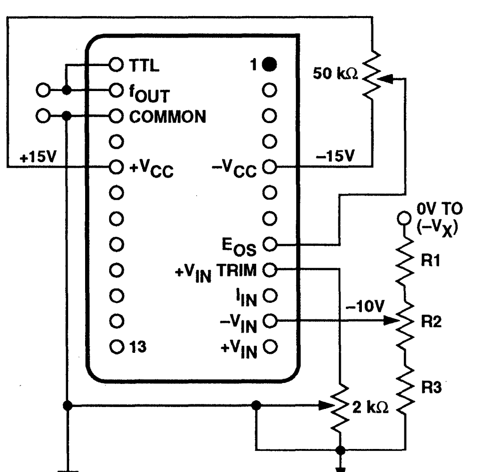
R1 ≈ 4R2
R1 + R2 = [(V_X÷10) × 100 kΩ] – 100 kΩ

Figure 4. Full Scale $+V_{IN}$ Greater Than +10V



R1 = R2
R1 + R2 = ($V_{FULL\text{-}SCALE}$ ÷ $I_{FULL\text{-}SCALE}$) Ω

Figure 6. Full-Scale Output for Less Than Full-Scale Input



Attenuator R1, R2, R3 reduces large negative input voltages to range of -VIN.

Figure 5. Full-Scale Input More Negative Than –8V

Reduced Full-Scale f_{OUT}

In some applications, a reduced full-scale output frequency is required when the input signal is ±10V or greater. The circuits of Figures 4 and 5 show attenuation of an overrange input signal can also be used to attenuate a nominal ±10V input signal below ±10V, thereby reducing the full-scale f_{OUT} below nominal 10 kHz to 100 kHz.

To make maximum use of the device's dynamic range, the input signal should be conditioned to ±10V full scale and a binary (or BCD) frequency divider (counter) should be connected to the output. Any TTL, CMOS, or HNIL device may be used, from a simple ÷10 unit (such as the TTL 54/74 90A), to a programmable divider (such as the CMOS CD4059), which can divide by any number from 3 to 15,999.

If the V-to-F output is set at its nominal full scale, the output of the counter (shown in Figure 7) will be 1 kHz (4731) or 10 kHz (4733). Likewise, the minimum output frequency will be 1 MHz or 10 MHz, respectively.

Full-Scale Input Currents Greater Than +100 μA

If the full-scale input current is greater than nominal, the "current splitter" circuit of Figure 8 can be used. As noted in Figure 3, the voltage developed at the wiper of potentiometer RA must be less than the compliance voltage of the

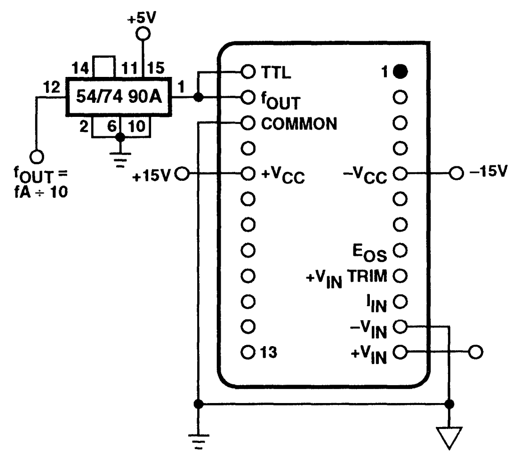
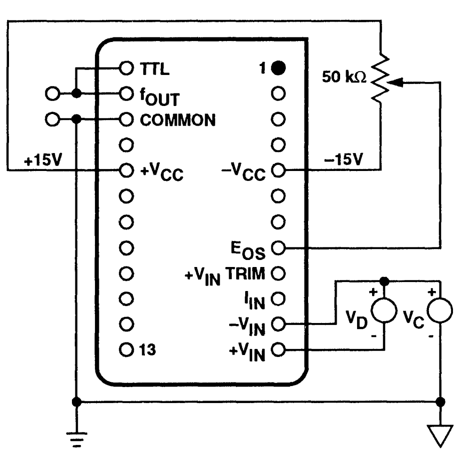


Figure 7. Reduced Full-Scale Output for $V_{IN} \geq 10V$



V_D = Differential Voltage
V_C = Common-Mode Voltage
$f_{out} = (V_D \div 10) \times f_A$

Figure 8. Definition of Differential and Common-Mode Input Voltages

current source. A negative-input current can be conditioned by passing it through a resistor connected between $-V_{IN}$ and signal common, thereby producing a negative voltage. The compliance voltage of the current source must be greater than the maximum voltage developed across the resistor.

The best way to condition current signals is with the classic op-amp current-to-voltage converter circuit. With this circuit and the "right" amplifier, virtually any current (even femtoamps) will provide a positive or negative 10V full-scale input to the V-to-F without compliance voltage problems.

Differential Inputs

The $+V_{IN}$ and $-V_{IN}$ terminals represent true differential inputs capable of accepting signals from a balanced line, a thermistor bridge or a signal source sitting at a common-mode voltage. The device's differential input eliminates the need for a differential preamplifier.

To use the voltage inputs differentially, some simple conventions (definitions) must be observed. Illustrated in Figure 8, they are:

1. Common-mode voltage (CMV) is defined as the voltage between $\pm V_{CC}$ common and $-V_{IN}$.
2. $+V_{IN}$ must always be positive with respect to $-V_{IN}$.
3. CMV range is typically between $+V_{CC}-4V$ and $-V_{CC}+5V$.
4. The differential (floating, balanced) signal source must be returned to $\pm V_{CC}$ common and must not create voltages exceeding the limits set in (1), (2) or (3).
5. $f_{OUT} = (+V_{IN}) - (-V_{IN}) \times fA/10V$ fA
   = 10 kHz (4731)
   = 100 kHz (4733)

Operation With Bipolar Input Signals

The V-to-F converter cannot operate with bipolar (i.e., –5V to +5V) input signals when connected as shown in Figures 1 and 2. To handle bipolar inputs it is necessary to offset the zero (i.e., produce a pulse train out for "zero" volts in).

For example, if $+V_{IN}$ is connected to 0V and $-V_{IN}$ is connected to a fixed –5V, the device's output will be "offset" to either 5 kHz (4731) or 50 kHz (4733) for a 0V input. If $+V_{IN}$ is –5V, f_{OUT} will be 0 Hz; if $+V_{IN}$ is 0V, f_{OUT} is 5 kHz or 50 kHz; if $+V_{IN}$ is +5V, f_{OUT} is 10 kHz or 100 kHz.

The offset may be performed at $+V_{IN}$ (pin 12) and the signal applied to either $-V_{IN}$ (pin 11) or I_{IN} (pin 10); or I_{IN} may be used to inject the fixed offset. Offsetting may be combined with all of the adjustment techniques, shown in Figures 1 through 10, to provide signal conditioning for almost any practical input signal.

Eliminating Common-Mode Signals

An input signal is often a small voltage change impressed on a larger fixed voltage. This situation is handled by nulling (offsetting) the DC or unchanging component of the input signal at one input and adjusting the full-scale gain factor at another, so the variable portion of the input signal causes f_{OUT} to cover the full excursion from 0 Hz to full scale; i.e., an input signal that is a voltage varying between +4V and +6V. To implement offsetting, connect $+V_{IN}$ to –4V. Since the actual signal is 2V (6V–4V), connect it to $+I_{IN}$ in series with resistor and trim potentiometer chosen to generate 100 μA of input current from the 2V signal (see Figure 5).

When input varies between +5V and +15V (signal = 10V), implement offsetting by connecting $-V_{IN}$ to +5V and apply the signal to $+V_{IN}$. Trim the V-to-F per Figure 1. If the input varies between +30V and +50V (signal = 20V), implement offsetting by connecting –30V to $+I_{IN}$ through a 150 kΩ resistor and series potentiometer. Connect the 20V signal to $+V_{IN}$ or $+V_{IN}$ TRIM.

Operation With Fast Signals

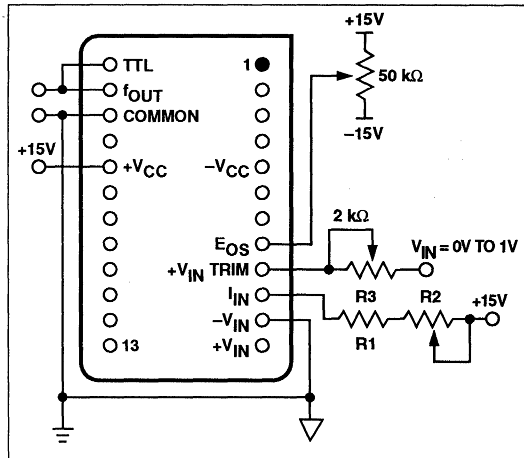
A V-to-F application may require operation with rapidly changing input signals. For example, the output of a load cell may change from 0 to full scale (or full scale to 0) in 1 ms. To accurately handle this signal, the output of the V-to-F converter must be able to change faster than the input.

The basic response (or settling time) of the V-to-F converter for voltage inputs is one period of the new frequency +5 μs. Response time is either 1s (4731) or 0.1s (4733) +5 μs.

Using the 4731 as an example: When the input changes from 0V to 10V, the new frequency is 10 kHz, one period is 100 μs, and response time is 105 μs. However, if the signal changes from full scale to 0V, the new period is much longer than the required 1 ms (theoretically it is infinite).

If the V-to-F output is to change in 1 ms, the output frequency for 0V in must be offset to a new frequency, the period of which is less than the 1 ms required for the application described. The full-scale value of the input signal is adjusted so the V-to-F converter will operate between the chosen offset or zero frequency and the maximum full-scale frequency.

In Figure 9 a 4731 is offset so that a 0V to +1V signal produces an output which varies between 9 kHz and 10 kHz with a response time of 116 μs (maximum) in either direction. Offsetting the V-to-F output range in this manner has the effect of reducing the settling/response time to the required level.



R1 = 4R2
R1 + R2 ≈ 167.7 kΩ
Set R2 so f_{out} = 9kHz for 0V input
Set R3 so f_{out} = 10kHz for 1V input

Figure 9. Frequency Offsetting to Decrease Settling Time

TTL Output Characteristics

The TTL-level pulse train from the V-to-F converter is designed to drive at least one TTL load over the power supply range +9V to +18V. At +15V, it can drive 10 TTL loads. The output circuit (see block diagram) is a single transistor (Q2) connected as a saturated switch with pull-up resistor (R5). When Q2 is on, the output is at "zero" volts. When Q2 is off, the output voltage is ($+V_{CC} \div 3$), assuming pins 23 and 24 are connected together. (If pin 23 is not connected to pin 24, an external divider must be provided which will determine the high output voltage.)

CMOS or HNIL Logic

The 4731 and 4733 output circuits are easily adapted to drive CMOS or HNIL. It is only necessary to parallel R5 (see block diagram) with a 1 kΩ resistor. This additional pull-up resistor also decreases pulse rise time, enabling these devices to drive larger capacitive loads. If pin 23 is not connected to pin 24, an external divider must be provided.

Output Protection

The V-to-F output (collector of Q2) may be shorted to ground indefinitely without damage; however, since Q2 is ON most of the time, a short to $+V_{CC}$ will cause certain catastrophic failure in about 5s. A short to TTL (pin 24) and $-V_{CC}$ (pin 5) simultaneously will cause instant catastrophic failure.

Square-Wave Output

The outputs of the 4731 and 4733 are a train of pulses 20 μs or 2 μs wide, respectively (see Figure 11). A symmetrical (square wave) output for driving highly capacitive or noisy transmission lines can be obtained with a D-type or JK flip-flop, as shown in Figure 10. The square-wave output has a frequency equal to 1/2 the V-to-F output frequency.

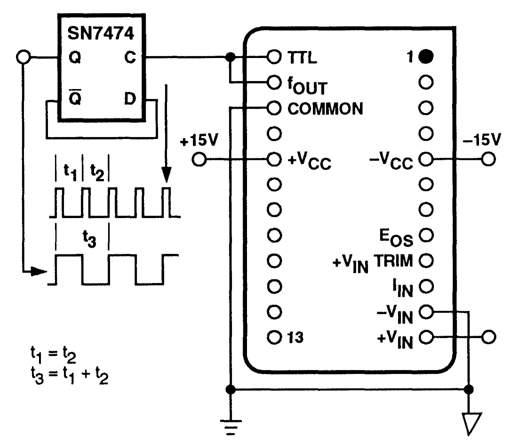
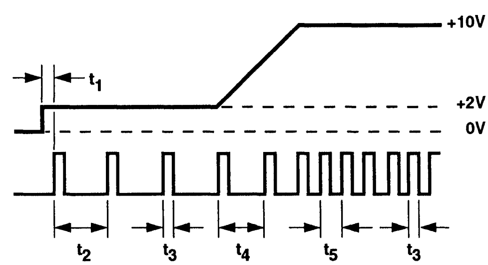


Figure 10. Square-Wave Output Using D-Type Flip-Flop



TYPICAL TIMING (μs)					
	t_1	t_2	t_3	t_4	t_5
4731	0 to 500	500	20	≈200	100
4733	0 to 50	50	2	≈30	10

Figure 11. Typical Timing Relationships

NOTES

TELEDYNE COMPONENTS

HIGH-RELIABILITY HYBRID FREQUENCY-TO-VOLTAGE CONVERTER

FEATURES

- Wide Power Supply Range ....±12V to ±18V
- Nonlinearity ....±0.008% FS Max
- Accepts Any Input Waveshape
- High Noise Immunity
- Low Full-Scale Drift
- Low Offset-Voltage Drift

APPLICATIONS

- Measure Flow, RPM, Frequency
- Demodulate FM
- Use With V-to-F Converter
- Low-Cost FM Telemetry
- DC Response Magnetic Tape Recording
- Multi-Decade Range Phase Lock Loops
- Fiber-Optic Data Link

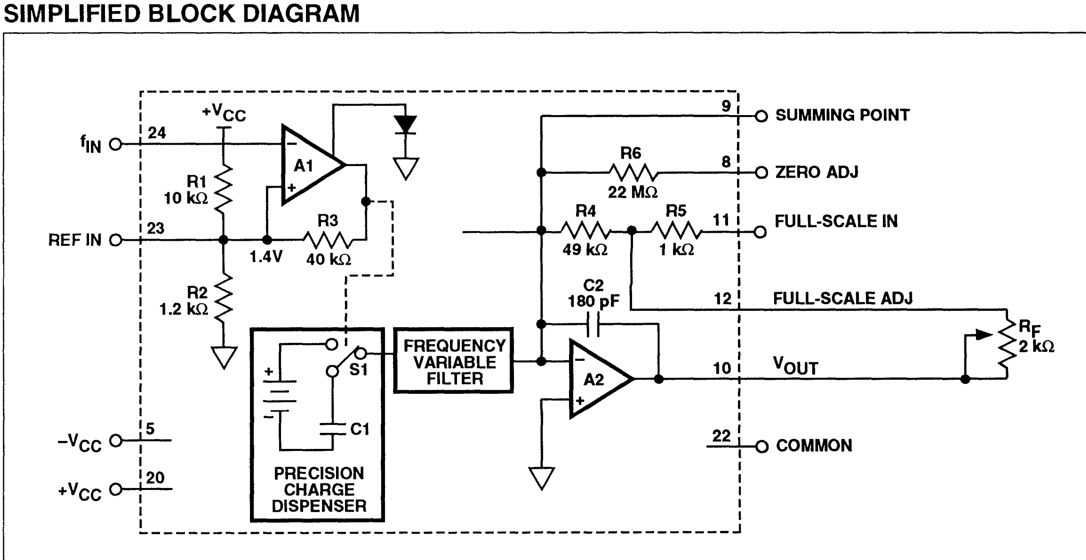
GENERAL DESCRIPTION

The 4736 is an ultra-linear, low-drift frequency-to-voltage (F-to-V) converter which produces an output voltage linearly proportional to input frequency, regardless of input waveshape. Designed to satisfy a multitude of precision system requirements, the 4736 represents an invaluable tool for the advancement of data acquisition and signal processing technology.

The superior specifications of the 4736 allow it to be used in the most critical frequency conversion applications. Common tasks include monitoring/controlling the pulsed output of a motor or flowmeter.

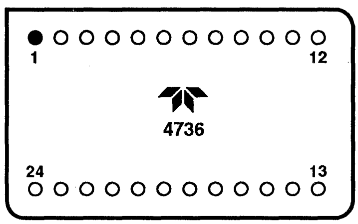
The standard 4736 is packaged in a 24-pin dual-in-line metal package and is specified for 0°C to +70°C operation. For high-reliability applications, the 4736-HR is specified for –55°C to +125°C operation.

SIMPLIFIED BLOCK DIAGRAM



4736

PIN CONFIGURATION



Pin No.	Designation	Pin No.	Designation
1	NC	24	f_{IN}
2	NC	23	REF INPUT
3	NC	22	COMMON
4	NC	21	NC
5	$-V_{CC}$	20	$+V_{CC}$
6	NC	19	NC
7	NC	18	NC
8	ZERO ADJUST	17	NC
9	SUMMING POINT	16	NC
10	OUTPUT	15	NC
11	FULL-SCALE INPUT	14	NC
12	FULL-SCALE ADJ.	13	NC

NC = No internal connection

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Power Supplies	±22V
V_{IN}	Input Voltage	$\pm V_{CC}$ to ±15V
V_{ID}	Differential Input Voltage	±12V
V_{REF}	Reference Voltage	±12V
T_C	Specified Temperature Range (Case)	
	4736	0°C to +70°C
	4736-HR	–55°C to +125°C
T_{STG}	Storage Temperature Range	–65°C to +150°C
T_S	Lead Temperature (Soldering, 0.06" from pkg., < 10 sec)	260°C
	Unit Weight	11.2g Typ

HIGH-RELIABILITY HYBRID FREQUENCY-TO-VOLTAGE CONVERTER

ELECTRICAL CHARACTERISTICS: $T_C = +25°C$, $\pm V_{CC} = \pm 15V$, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
f_{IN}	Frequency Input Range		0	1	1.3	MHz
	Input Waveform		—	Any	—	—
t_{PW}	Input Pulse Width	$V_{IH} = 2V$	75	—	—	ns
V_{IH}	Input High Voltage		2	—	12	V
V_{IL}	Input Low Voltage		–12	—	0.8	V
V_{INT+}	Threshold, Positive-Going Pulses	Typically 1.4V ±200 mV	0.8	1.4	2.2	V
	Threshold, External Set Range		—	—	±12	V
	Hysteresis		300	400	500	mV
	Hysteresis, External Set Range		0	400	—	mV
R_{IN}	Input Impedance		—	100‖4	—	GΩ‖pF
Output						
V_O	Full-Scale Output Voltage	Pin 10 Shorted to Pin 11	**9.99**	**10**	**10.01**	V
$V_{O\,ADJ}$	V_O Adjustable Full-Scale Voltage	Pin 10 Shorted to Pin 12	9.97	9.9	10.03	V
V_O/TC	V_O Full Scale vs Temperature	0°C to +70°C (Standard)	—	±40	±50	ppm/°C
		–55°C to +125°C (HR)	—	±70	±100	ppm/°C
V_{OS}	Output Offset Voltage	$f_{IN} = 0$ Hz	**—**	**±1**	**±5**	mV
V_{OS}/TC	V_{OS} Voltage vs Temperature	0°C to +70°C (Standard)	—	±20	±50	µV/°C
		–55°C to +125°C (HR)	—	±30	±80	µV/°C
V_{OLE}	V_O Linearity Error	1.1 kHz to 1 MHz	**—**	**±0.003**	**±0.008**	%FS
V_{OLE}/TC	V_{OLE} Over Temperature	1.1 kHz to 1 MHz, 0°C to +70°C (Standard)	—	±0.005	±0.015	%FS
		1.1 kHz to 1 MHz, –55°C to +125°C (HR)	**—**	**±0.008**	**±0.05**	%FS
	V_O Ripple Voltage	$f_{IN} = 100$ Hz	—	80	200	mV_{P-P}
		$f_{IN} = 100$ kHz	—	450	700	mV_{P-P}
		$f_{IN} = 1$ MHz	—	80	150	mV_{P-P}
	V_O vs Time	Per Day	—	±20	—	µV/D
		Per Week	—	±60	—	µV/W
$PSRR_1$	V_O Zero vs Power Supplies }	±Vps from ±13V to ±17V referred	**—**	**±10**	**±20**	µV/%ΔVps
$PSRR_2$	V_O Full Scale vs Power Supplies }	to Vps = ±15V	—	±40	±80	ppm/%ΔVps
I_O	Output Current	Not Short-Circuit Protected	**–2/+20**	**—**	**—**	mA
R_O	Output Impedance		—	—	0.05	Ω
Transfer						
	Ideal Transfer Function	fA = 1 MHz		$[f_{IN} \div fA] \times 10V$		V
Dynamic						
RC	Response Time, Internal Filter		—	9	—	µs
t_{SR}	Step Response Time to 0.5 %FS	0 Hz to 1 MHz Step, $R_L = 500\Omega$	—	60	—	µs
		1 MHz to 200 kHz Step, $R_L = 500\Omega$	—	70	—	µs
		1 MHz to 0 Hz Step, $R_L = 500\Omega$	—	95	—	µs
Power Supplies						
V_{CC}	Voltage Range		±13	±15	±17	V
I_{CC}	Quiescent Current		**—**	**±28**	**±35**	mA
PD	Power Dissipation		—	1050	—	mW

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested at +25°C. HR versions have I_O, V_{OLE}/TC, V_O, V_{OS} and V_{OS}/TC tested at -55°C, +25°C and +125°C. Standard parts are tested at room temperature only. Other min/max parameters are guaranteed by design.

4736

THEORY OF OPERATION

The 4736 F-to-V converter is an example of a sophisticated concept implemented in a low-cost, highly reliable device (see block diagram). The input is a comparator (A1) whose output switches between +1V and −14V each time the voltage between f_{IN} (pin 24) and REF IN (pin 23) reverses polarity. Two consecutive reversals are interpreted as one cycle (or pulse) of input frequency.

Each reversal causes a solid-state switch (S1) to alternately connect capacitor C1 to a precision reference voltage and then, through a frequency-variable filter, to the summing point of op-amp A2. Each time C1 is connected to the reference voltage, a fixed amount of charge (Q) is dumped into C1 according to the equation Q = CV.

When C1 is connected to the summing point of A2, it discharges and the resulting current is converted to a voltage. The higher the input frequency, the greater the average current into the summing point. A2 is a current-to-voltage converter, where:

$$V_{OUT} = -(I \times R_F)$$

Therefore, V_{OUT} is a function of the discharge current from C1, the frequency of discharge, and the feedback resistor. C2 filters the current pulses from C1 to minimize output voltage ripple.

When used as shown in Figure 1, the 4736 operates as specified with no additional components.

Input Threshold

The f_{IN} (A1) input comparator's threshold is preset at +1.4V to provide maximum noise immunity when operating with TTL levels and has approximately 400 mV of hysteresis. It can operate with signals of any waveshape which vary about this threshold; for example, a 0V to 2V square wave or a $\pm5V_{P-P}$ sine wave. Each alternate threshold crossing is recognized as one cycle (or pulse) of input frequency.

The threshold level at which comparator A1 switches is set to 1.4V by resistors R1, R2 and R3. The threshold level can be modified by inputting a voltage to REF IN. The threshold will be equal to the voltage input to pin 23. This voltage should not exceed 12V, or internal damage will occur.

The comparator hysteresis (400 mV) can be reduced by connecting REF IN to COMMON (pin 22) with a resistor (see "Operation with HNIL or CMOS Logic" following).

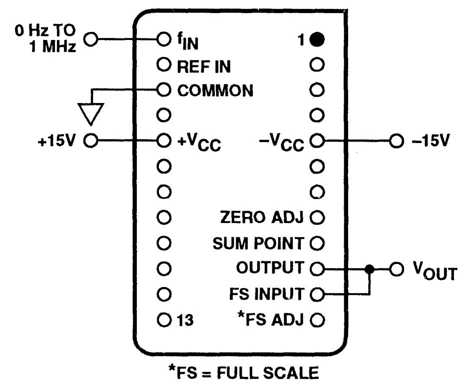


Figure 1. Basic Operational Connections

Output Circuit

The 4736 output is an inverting op amp. The output voltage is set by connecting the OUTPUT (pin 10) to FULL-SCALE IN (pin 11) or FULL-SCALE ADJ (pin 12). These are the gain-setting inputs, feedback paths, for amplifier A2.

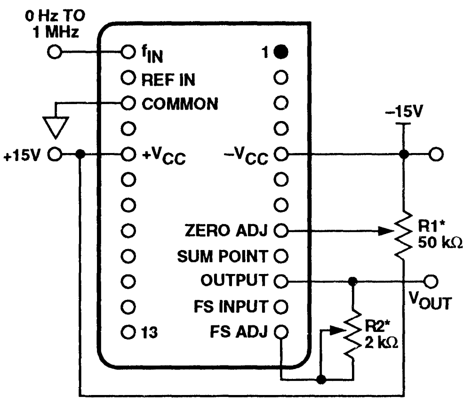
Pin 11 is the nominal feedback connection. The internal resistor is factory trimmed to approximately 49.5 kΩ and produces a +10V ±0.1% output for a 1 MHz input frequency. Use this input when accuracy to ±0.1% full scale is sufficient or when external components cannot be tolerated. Use pin 12 when greater accuracy is required, as it allows use of an external trim (see Figure 2).

The feedback resistor from pin 12 is approximately 495Ω (or 1%) less than nominal. Connecting a 1 kΩ potentiometer between the output and pin 12 allows the user to fine-tune the output accuracy over a ±1% range.

Trim Procedure

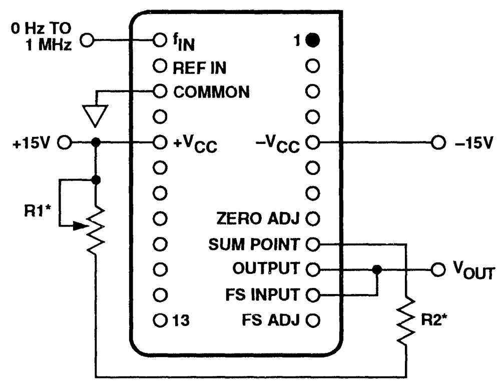
Referring to Figure 2:

1. Connect f_{IN} to COMMON and adjust R1 for 0V output.
2. Connect f_{IN} to a frequency source set at 1 MHz and adjust R2 for 10V output.
3. Repeat steps (1) and (2) until zero and full scale are set.



*R1 and R2 should have low temperature coefficient.

Figure 2. Zero and Full-Scale Trim



*R1 + R2 = $V_{CC} \div (V_{OFF} \times$ Offset-Scale Factor)

Figure 3. Output Offset of −5V to Provide 0V to +5V for 500 kHz to 1 MHz Input Frequency

Output Offsetting

Many frequency-to-voltage applications measure a range of frequencies that do not include zero, but require zero volts out for a particular frequency input. For example, the pulse train from a tachometer in a motor speed-control circuit might range between 500,000 and 1,000,000 pulses per second which would normally generate +5V to +10V from the 4736.

To obtain a 0V to +5V output range the 4736 must be offset by −5V. This is done by injecting a current of approximately +50 μA into the SUMMING POINT (pin 9).

The offset-adjust scale factor is −10 μA/V ±25%. Offset adjust can be implemented, as shown in Figure 3, by connecting a potentiometer or fixed resistor between the SUMMING POINT and $+V_{CC}$ (pin 20). The resistor value can be calculated:

$$
\begin{aligned}
R &= V_{CC} \div [V_{OFF} \times \text{Offset Scale Factor}] \\
&= 15 \div [5 \times 0.00001] \\
&= 300\ \text{k}\Omega
\end{aligned}
$$

If a bipolar output voltage of −2.5V to +2.5V is required for a 500 kHz to 1 MHz input, the output may be offset a total of −7.5V by the same method.

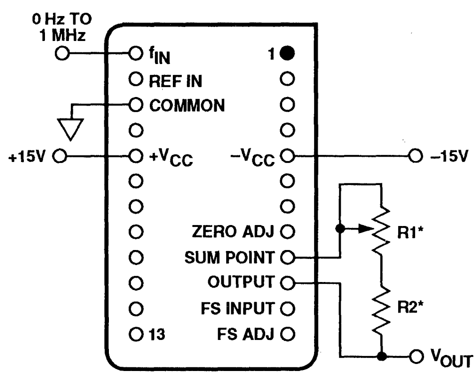
Scale Expansion and Output Offset

If an application requires a full-scale (0V to +10V) output for a less than full-scale range of input frequencies, the full-scale factor can be expanded by increasing the feedback resistor for A2. This is done by adding a series resistor to the internal feedback resistors. Another method is not to use the internal resistors and to add an external resistor between the SUMMING POINT and the OUTPUT (see Figure 4). The value for the total feedback resistance needed, regardless of which method you choose, is:

$$
\begin{aligned}
R_F &= G \times 100{,}000 \\
&= [\Delta V_{OUT} \div \Delta f_{IN}\ (\text{in kHz})] \times 100{,}000 \\
&= [10 \div 500] \times 100{,}000 \\
&= 2\ \text{k}\Omega\ (\pm 25\%)
\end{aligned}
$$

If this technique is used, be sure to account for the 4736's output compliance range. For example, at G = 2, a 500 kHz input produces +10V output, and a 1 MHz input demands a +20V output which will overrange the output of the 4736. The output must be offset by −10V.

Be aware that the offset scale factor must be divided by the gain factor (G) that you have determined. Therefore, to offset the output by −10V you must drive ([−10 μA/V ÷ Gain of 2] × −10V) = +50 μA/V into the summing point.



*R1 + R2 = (5 x 10[10]) ÷ Desired Full-Scale in Hz

Figure 4. Custom Full-Scale Factor

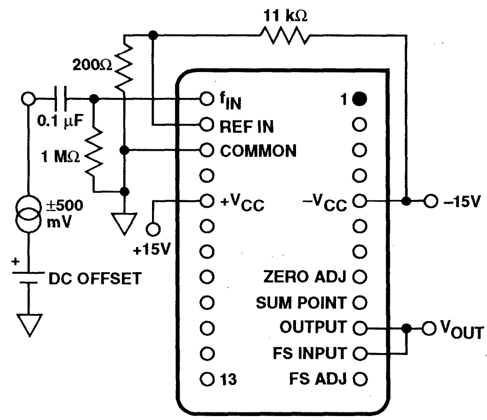


Figure 5. Input Conditioned for Small AC Signal with DC Offset

Operation With HNIL or CMOS Logic

To obtain maximum noise immunity with a particular logic type, the threshold should be set approximately halfway between the upper and lower logic levels. For example, a 2 kΩ, 5% resistor connected between REF IN and +15V provides a threshold of +6V (a typical CMOS or HNIL threshold level). Adjusting the threshold voltage in this manner has no impact on the zero and full-scale trim techniques discussed earlier.

Operation With Signals Less Than +2V Peak

Connecting an 11 kΩ, 5% resistor between REF IN and –15V will set the threshold at 0V with hysteresis of approximately 340 mV. Now the input signal only needs to be larger than 340 mV. However, input signals less than 500 mV should be used with care. They may produce erroneous output voltage due to the uncertainty of the hysteresis level.

For input signals less than 500 mV, hysteresis should be reduced by connecting a 200Ω resistor between REF IN and COMMON. This will lower the hysteresis and noise immunity to approximately 60 mV (see Figure 5). A 100Ω resistor provides 30 mV of hysteresis, which is the minimum recommended value. When operating in this mode the 4736 is virtually a zero-crossing detector.

Operation With DC Common Mode

When the input signal is small and impressed on a DC voltage (i.e., +9V DC ±500 mV AC), it should be capacitively coupled to the 4736, as shown in Figure 5. If the DC voltage is large, greater than $\pm V_{CC}$, the input should be protected against transients with diodes, as shown in Figure 6.

Signals greater than $\pm V_{CC}$ peak-to-peak may also be attenuated with a simple resistive divider and the appropriate threshold level, as discussed earlier.

Scale Expansion and Bipolar Output

If an output voltage of –5V to +5V is required for 500 kHz to 1 MHz input, the same technique described in "Scale Expansion and Output Offset" is used. The scale is doubled and the output is offset a total of –15V (from +10V to –5V) by additional current into the SUMMING POINT (pin 9).

Output Ripple Filtering and Response Time

By definition, frequency-to-voltage conversion is converting an AC signal to a DC level. Therefore, there must be ripple on the output. This ripple is filtered by a frequency variable filter and by an internal RC network consisting of R_F and a capacitor (C2) (see block diagram). Additional filtering is obtained by adding an external capacitance between the summing point and output.

The response time of the F-to-V converter (how fast the output voltage changes for a step change in the input frequency) is the RC time constant of the ripple filter. If external capacitance is added, response time is increased. If faster response with reduced ripple voltage is required, a higher frequency-to-voltage should be used or a multipole (i.e., sharp cutoff) low-pass filter should follow the frequency-to-voltage.

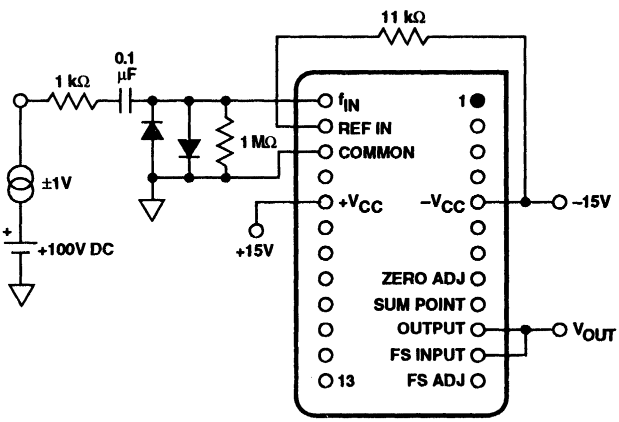


Figure 6. Input Conditioned for Small AC Signal Impressed on Large DC Voltage

NOTES

HIGH FREQUENCY, HYBRID VOLTAGE TO FREQUENCY CONVERTER

FEATURES

- Full Scale Output 10MHz
- Fully Differential Input
- Dynamic Range 100dB
- Linearity 11-Bit
- Supplies .... ±14V to ±18V
- Easily Modified for Different I/O Signals

APPLICATIONS

- Two-Wire Digital Data Transmission
- Ratiometric Data Conversion
- Long Term Integrators
- Fiber Optic Data Links
- FM Modulation

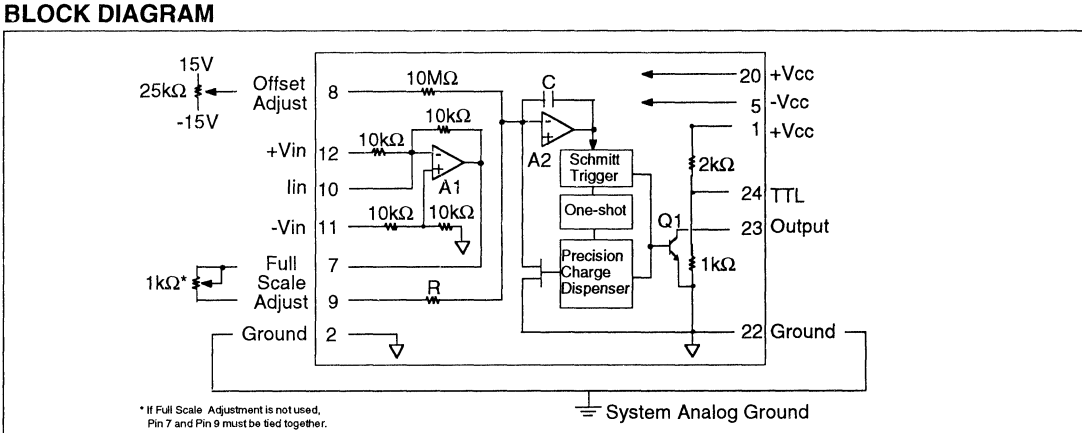
GENERAL DESCRIPTION

The 4743 hybrid voltage to frequency converter offers a full scale output of 10MHz, and can be externally trimmed to any value from its rated full scale output down to 2.5 MHz. The 4743 has full differential input and can be driven with positive voltage, negative voltage, or positive current. Common mode rejection ratio, with VCM = 10 volts, is 80 dB. With external resistors, the input is easily adapted to accept almost any input signal range. The output stage of the unit is a single uncommitted transistor that operates as a saturated switch. A pull-up resistor for TTL compatibility is internal to the 4743. An external resistor can be added to make the output CMOS compatible, and the output can drive 10 TTL loads.

The 4743 has quick response time, and settles to within ±0.01%FS of a new frequency in 15 µsec. Overload recovery time is approximately 10 output signal periods. Dynamic range is greater than 100 dB, and input/output linearity over a ±10 mV to ±10.5V input range is ±0.05%FS plus ±0.05% of signal. Initial zero offset error is ±8 mV (8 kHz). Zero Offset error is externally adjustable to zero. Initial full scale accuracy is ±50 kHz, and full scale error is also externally adjustable to zero. If full scale adjust is not employed, Pins 7 and 9 must be tied together.

The standard 4743 is specified for 0°C to +70°C operation. The -HR version is specified for -55°C to +125°C operation.

BLOCK DIAGRAM



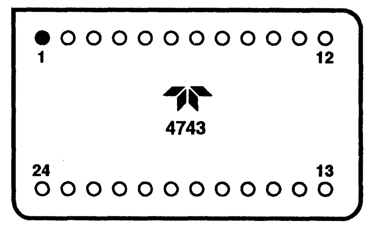
HIGH FREQUENCY, HYBRID VOLTAGE-TO-FREQUENCY CONVERTER

4743

PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	$+V_{CC}$	24	TTL
2	GROUND	23	f_{OUT}
3	NC	22	GROUND
4	NC	21	NC
5	$-V_{CC}$	20	$+V_{CC}$
6	NC	19	NC
7	FULL SCALE ADJUST	18	NC
8	OFFSET ADJUST	17	NC
9	FULL SCALE ADJUST	16	NC
10	$+I_{IN}$	15	NC
11	$-V_{IN}$	14	NC
12	$+V_{IN}$	13	NC

NC = No internal connection



ABSOLUTE MAXIMUM RATINGS

V_{CC}	Power Supplies	±22V
$\pm V_{IN}$	Input Voltage (Note 1)	±15V
V_{ID}	Differential Input Voltage	V_{CC}
I_{IN}	Current Input	2.1 mA
T_C	Specified Temperature Range, Case	
	4743	0°C to +70°C
	4743-HR	-55°C to +125°C
T_{STG}	Storage Temperature Range	–65°C to +150°C

ELECTRICAL CHARACTERISTICS: T_C = +25°C, $\pm V_{CC}$ = ±15V, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
$+V_{IN}$	Positive Input Range (Note 1)	For specified linearity	0.0001	—	10.5	V
$-V_{IN}$	Negative Input Range	For specified linearity	-0.0001	—	-10.5	V
V_{CM}	Common Mode Input Range		—	—	±10	V
CMRR	Common Mode Rejection Ratio		60	80	—	dB
V_{ID}	Differential Input Voltage	Referenced to $-V_{IN}$	10.5	12	—	V
I_{IN}	Current Input Range		0.0001	—	1.2	mA
	Input Dynamic Range		100	—	—	dB
V_{OS}	Input Offset Voltage	Adjustable to zero	—	±8	±20	mV
V_{OS} TC	Input Offset Drift		—	—	±100	µV/°C
$PSRR_1$	V_{OS} vs. Power Supplies	Constant voltage at Pin 8	—	—	±20	µV/%

ELECTRICAL CHARACTERISTICS: (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input (cont.)						
R_{+IN}	$+V_{IN}$ Input Impedance		—	10	—	kΩ
R_{-IN}	$-V_{IN}$ Input Impedance		—	20	—	kΩ
R_{IIN}	I_{IN} Input Impedance	Virtual Ground	—	<0.1	—	Ω
Output						
V_{OH}	Output High Voltage	$I_{OH} = 400\ \mu A$	**2.4**	—	**5**	V
V_{OL}	Output Low Voltage	$I_{OL} = -16$ mA	—	—	**0.4**	V
R_O	Output Impedance		632	666	700	Ω
Dynamic						
ts	Settling Time to ±0.01% 10V step		—	15	—	µs
	Overload Recovery	$\Delta V_{IN} = +20V$ to $+10V$	—	—	10	Cycles
Transfer						
f_O	Output Frequency	ΔV_{IN} equals $V_{IN} - (-V_{IN})$	$[\Delta V_{IN} \times f_A] \div 10V$ $[I_{IN} \times f_A] \div I_{FS}$			MHz MHz
f_A	Full Scale Frequency	@ V_{IN} = 10.0000V pins 7 & 9 shorted @ 25°C	**10**	**10.1**	**10.2**	MHz
I_{FS}	Full Scale Current		.75	1	1.25	mA
$f_A\ T_C$	f_A vs Temperature	$T_C = T_{MIN}$ to T_{MAX}	—	**±40**	**±100**	ppm/°C
$I_{FS}\ T_C$	I_{FS} vs Temperature		—	30	—	ppm/°C
±PSRR	f_A vs Power Supplies	@ 10 MHz, ±14 to ±18V	**-125**	—	**125**	ppm/%ΔV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10V$, $V_{dif} = .5V$	**60**	—	**120**	dB
$+V_{INLE}$	$+V_{IN}$ Linearity Error (Note 2)	V_{IN} = 10 mV to 10V	**-.100**	**<.05**	**.100**	%FS
$-V_{INLE}$	$-V_{IN}$ Linearity Error (Note 2)		-.100	<.05	.100	%FS
I_{INLE}	I_{IN} Linearity Error (Note 2)		-.100	<.05	.100	%FS
t_{PW}	Output Pulse Width	@ 10 MHz	**20**	—	**65**	ns
Power Supplies						
V_{CC}	Voltage Range		±14	±15	±18	V
	Voltage Asymmetry	$\lvert V_{CC}\rvert - \lvert -V_{CC}\rvert$	—	—	±4	V
$+I_{CC}$	Positive Supply Quiescent Current		—	**75**	**90**	mA
$-I_{CC}$	Negative Supply Quiescent Current		—	**-25**	**-35**	mA
P_D	Power Dissipation		—	1500	1875	mW

NOTES:
1. $+V_{IN}$ has a 10kΩ internal resistor and a 2 mA maximum input current limit. The Voltage input, if current limited by a series input resistor, is virtually unlimited.
2. Linearity specifications apply only after offset and gain have been trimmed to nominal.
3. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested. HR product tested at +125°C, +25°C and -55°C unless otherwise noted. Standard parts tested at room temperature only.

APPLICATION INFORMATION

To take maximum advantage of the 4743's versatility, a functional block diagram and theory of operation are provided. With this information, input and output circuitry are easily understood and adapted to handle virtually any signal or load.

The 4743 is a free-running (astable) voltage controlled multivibrator. A true differential input amplifier, (A_1), allows the device to be driven by positive input voltage applied to Pin 12 (with Pin 11 open or grounded), by negative voltage applied to Pin 11 (with Pin 12 open or grounded), by differential voltages applied between Pins 12 and 11 ($V_{IN} = +V_{IN} - (-V_{IN})$), or by positive current applied to Pin 10. CMRR with VCM = 10V is typically 80 dB.

No combination of input signals that will drive the output of amplifier A_1 positive is permitted. The trigger circuit has a positive threshold level and will not respond to the negative signals that would result from a positive A_1 output.

Operating with any of the input conditions described above results in a negative voltage at the output of A_1. Resistor R, amplifier A_2, and capacitor C(100 pF) form an integrator. C charges as a precise linear function of the V/F's input signal. When the voltage (charge) impressed on C reaches a fixed precise threshold, the trigger circuit triggers the one-shot (monostable) multivibrator, which in turn produces a constant-width output pulse. This pulse performs two functions. Amplified by Q_1, it becomes the output of the V/F and at the same time, it activates the precision charge dispenser (PCD).

The PCD discharges C to the same "zero" level every time an output pulse is produced. Thus, capacitor C is repeatedly charged between two precise voltages at a rate which is a linear function of the V/F input signal. That is, the rate of charging C, the repetition rate of reaching the trigger threshold, and the output frequency are all functions of the V/F voltage and/or current inputs.

Offset and Full Scale Trim Theory

Offset and full scale trim are performed at the input circuit. Offset is adjusted with a 25 kΩ potentiometer between $+V_{CC}$ and $-V_{CC}$, with its wiper tied to Pin 8. The subsequent voltage applied to Pin 8 falls across a 10 MΩ resistor to become a constant positive or negative current directly injected into the integrator capacitor.Full scale is adjusted by varying the integrator's input resistance with a series 1 kΩ potentiometer connected between Pins 7 and 9. This adjustment can only lower the V/F's full scale output frequency, so units are laser trimmed at the factory to have initial full scale output errors that are always positive. By placing a fixed resistor in series with the adjusting potentiometer, the full scale output frequency can be lowered to 2.5 MHz. If full scale adjustment is not employed, Pins 7 and 9 must be tied together with as short a jumper as possible.

4743 Output Circuit

The TTL logic pulse train from the V/F is designed to drive 10 TTL loads with ±15V supplies. The output circuit is a single transistor (Q_1) connected as a saturated switch with an uncommitted 2 kΩ pull-up resistor. With Pins 23 and 24 connected together, the output is approximately zero volts when Q_1 is on. With Q_1 off, the output voltage is $+V_{CC}/3$ or +5V when $+V_{CC} = +15V$. If Pin 23 is not connected to Pin 24, an external divider must be provided. The output circuit is easily adapted to drive CMOS logic by paralleling the 2 kΩ resistor with an external resistor large enough to bring the output up to the desired level. The additional pull-up resistor also decreases pulse rise time when driving larger capacitive loads.

The output (collector of Q_1) may be shorted to ground indefinitely without damage. However, since Q_1 is on most of the time, a short to $+V_{CC}$ will cause certain catastrophic failure in about 5 seconds.

TELEDYNE COMPONENTS

TC9400 TC9401 TC9402

VOLTAGE-TO-FREQUENCY/FREQUENCY-TO-VOLTAGE CONVERTERS

FEATURES

Voltage-to-Frequency

- Operation .... 1 Hz to 100 kHz
- Choice of Guaranteed Linearity:
  - TC9401 .... 0.01%
  - TC9400 .... 0.05%
  - TC9402 .... 0.25%
- Gain Temperature Stability .... ±25 ppm/°C Typ
- Open-Collector Output
- Output Can Interface With Any Form of Logic
- Pulse and Square-Wave Outputs
- Programmable Scale Factor
- Low Power Dissipation .... 27 mW Typ
- Single-Supply Operation .... +8V to +15V
- Dual-Supply Operation .... ±4V to ±7.5V
- Current or Voltage Input

Frequency-to-Voltage

- Operation .... DC to 100 kHz
- Choice of Guaranteed Linearity:
  - TC9401 .... 0.02%
  - TC9400 .... 0.05%
  - TC9402 .... 0.25%
- Op-Amp Output
- Programmable Scale Factor
- High Input Impedance .... >10 MΩ
- Accepts Any Voltage Waveshape

APPLICATIONS

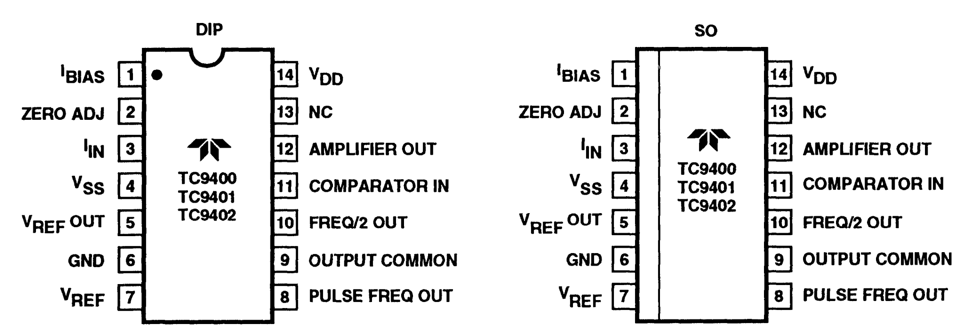
Voltage-to-Frequency

- Temperature Sensing and Control
- μP Data Acquisition
- Instrumentation
- 13-Bit Analog-to-Digital Converters
- Digital Panel Meters
- Analog Data Transmission and Recording
- Phase-Locked Loops
- Medical Isolation
- Transducer Encoding
- Alternate to 555 Astable Timer

Frequency-to-Voltage

- Frequency Meters/Tachometer
- Speedometers
- Analog Data Transmission and Recording
- Medical Isolation
- Motor Control
- RPM Indicator
- FM Demodulation
- Frequency Multiplier/Divider
- Flow Measurement and Control

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

TC9400
TC9401
TC9402

GENERAL DESCRIPTION

The TC9400/TC9401/TC9402 are low-cost voltage-to-frequency (V/F) converters combining bipolar and CMOS technology on the same substrate. The converters accept a variable analog input signal and generate an output pulse train whose frequency is linearly proportional to the input voltage.

The devices can also be used as highly-accurate frequency-to-voltage (F/V) converters, accepting virtually any input frequency waveform and providing a linearly-proportional voltage output.

A complete V/F or F/V system requires the addition of two capacitors, three resistors, and reference voltage.

ORDERING INFORMATION

Part No.	Linearity (V/F)	Package	Temperature Range
TC9400CPD	0.05%	14-Pin Plastic DIP	0°C to +70°C
TC9400EJD	0.05%	14-Pin CerDIP	–40°C to +85°C
TC9400COD	0.05%	14-Pin SO	0°C to +70°C
TC9401CPD	0.01%	14-Pin Plastic DIP	0°C to +70°C
TC9401EJD	0.01%	14-Pin CerDIP	–40°C to +85°C
TC9402CJD	0.25%	14-Pin Plastic DIP	0°C to +70°C
TC9402EJD	0.25%	14-Pin CerDIP	–40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

$V_{DD} - V_{SS}$ .... +18V
I_{IN} .... 10 mA
V_{OUT} Max $-V_{OUT}$ Common .... +25V
$V_{REF} - V_{SS}$ .... –1.5V
Storage Temperature Range .... –65°C to +150°C
Operating Temperature Range
  C Device .... 0°C to +70°C
  E Device .... –40°C to +85°C
Package Dissipation .... 500 mW
Lead Temperature (Soldering, 10 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

3

ELECTRICAL CHARACTERISTICS: V_{DD} = +5V, V_{SS} = –5V, V_{GND} = 0, V_{REF} = –5V, R_{BIAS} = 100 kΩ, Full Scale =10 kHz, unless otherwise specified. T_A = +25°C, unless temperature range is specified –40°C to +85°C for E device, 0°C to +70°C for C device.

VOLTAGE-TO-FREQUENCY		TC9401			TC9400			TC9402			
Parameter	**Definition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Accuracy											
Linearity 10 kHz	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	0.004	0.01	—	0.01	0.05	—	0.05	0.25	% Full Scale
Linearity 100 kHz	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	0.04	0.08	—	0.1	0.25	—	0.25	0.5	% Full Scale
Gain Temperature Drift (Note 1)	Variation in Gain A Due to Temperature Change	—	±25	±40	—	±25	±40	—	±50	±100	ppm/°C Full Scale
Gain Variance	Variation From Exact A Compensate by Trimming R_{IN}, V_{REF}, or C_{REF}	—	±10	—	—	±10	—	—	±10	—	% of Nominal
Zero Offset (Note 2)	Correction at Zero Adjust for Zero Output When Input is Zero	—	±10	±50	—	±10	±50	—	±20	±100	mV
Zero Temperature Drift (Note 1)	Variation in Zero Offset Due to Temperature Change	—	±25	±50	—	±25	±50	—	±50	±100	µV/°C
Analog Input											
I_{IN} Full Scale	Full-Scale Analog Input Current to Achieve Specified Accuracy	—	10	—	—	10	—	—	10	—	µA
I_{IN} Overrange	Overrange Current	—	—	50	—	—	50	—	—	50	µA
Response Time	Settling Time to 0.1% Full Scale	—	2	—	—	2	—	—	2	—	Cycle
Digital Output											
V_{SAT} @ I_{OL} = 10 µA (Note 3)	Logic "0" Output Voltage	—	—	0.4	—	—	0.4	—	—	0.4	V
V_{OUT} Max – V_{OUT} Common (Note 4)	Voltage Range Between Output and Common	—	—	18	—	—	18	—	—	18	V
Pulse Frequency Output Width		—	3	—	—	3	—	—	3	—	µs
Supply Current											
I_{DD} Quiescent	Current Required From Positive Supply During Operation										
E Device (Note 9)		—	2	4	—	2	4	—	—	—	mA
C Device		—	2	6	—	2	6	—	3	10	mA
I_{SS} Quiescent	Current Required From Negative Supply During Operation										
E Device (Note 10)		—	–1.5	–4	—	–1.5	–4	—	—	—	mA
C Device		—	–1.5	–6	—	–1.5	–6	—	–3	–10	mA
V_{DD} Supply	Operating Range of Positive Supply	4	—	7.5	4	—	7.5	4	—	7.5	V
V_{SS} Supply	Operating Range of Negative Supply	–4	—	–7.5	–4	—	–7.5	–4	—	–7.5	V
Reference Voltage											
V_{REF} –V_{SS}	Range of Voltage Reference Input	–1	—	—	–1	—	—	–1	—	—	V

NOTES:
1. Full temperature range.
2. I_{IN} = 0.
3. Full temperature range, I_{OUT} = 10 mA.
4. I_{OUT} = 10 µA.
5. 10 Hz to 100 kHz.
6. 5 µs minimum positive pulse width and 0.5 µs minimum negative pulse width.
7. $t_R = t_F$ = 20 ns.
8. $R_L \geq 2$ kΩ.
9. Full temperature range, V_{IN} = –0.1V.
10. V_{IN} = –0.1V.
11. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly, but must be buffered by external resistors.

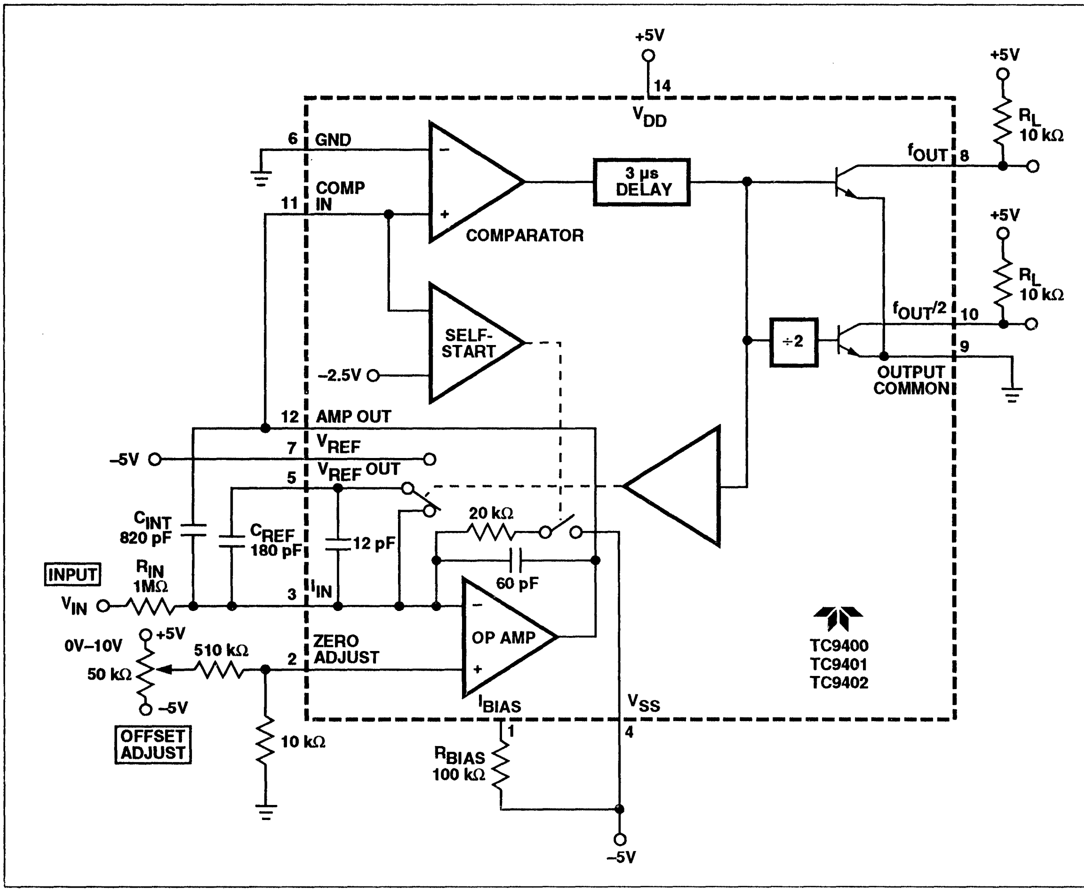
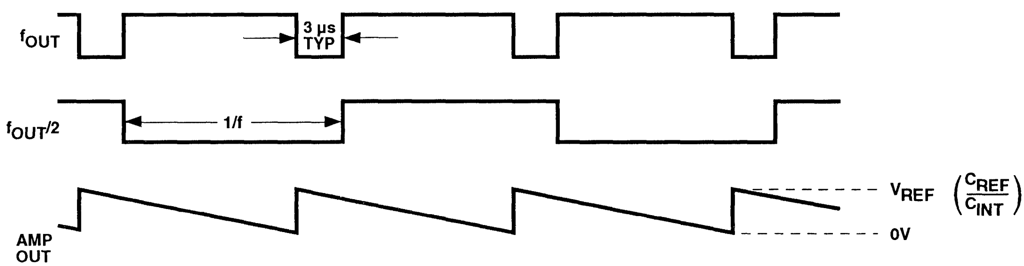


Figure 1 10 Hz to 10 kHz V/F Converter

VOLTAGE-TO-FREQUENCY (V/F) CIRCUIT DESCRIPTION

The TC9400 V/F converter operates on the principal of charge balancing. The input voltage (V_{IN}) is converted to a current (I_{IN}) by the input resistor. This current is then converted to a charge by the integrating capacitor and shows up as linearly decreasing voltage at the output of the op amp. The zero crossing of the output is sensed by the comparator causing the reference voltage to be applied to the reference capacitor for a time period long enough to virtually charge the capacitor to the reference voltage. This action reduces the charge on the integrating capacitor by a fixed amount ($q = C_{REF} \times V_{REF}$), causing the op-amp output to step up a finite amount.

At the end of the charging period, C_{REF} is shorted out, dissipating the stored reference charge, so when the output again crosses zero, the system is ready to recycle. In this manner, the continued discharging of the integrating capacitor by the input is balanced out by fixed charges from the reference voltage. As the input voltage is increased, the number of reference pulses required to maintain balance increases, causing the output frequency to also increase. Since each charge increment is fixed, the increase in frequency with voltage is near. In addition, the accuracy of the output pulses does not directly affect the linearity of the V/F. It must simply be long enough for full charge transfer to take place.



NOTES: 1. To adjust f_{MIN}, set V_{IN} = 10 mV and adjust the 50 kΩ offset for 10 Hz output.
2. To adjust f_{MAX}, set V_{IN} = 10V and adjust R_{IN} or V_{REF} for 10 kHz output.
3. To increase f_{OUT} MAX to 100 kHz, change C_{REF} to 27 pF and C_{INT} to 75 pF.
4. For high-performance applications, use high-stability components for R_{IN}, C_{REF}, V_{REF} (metal film resistors and glass capacitors). Also, separate output ground (pin 9) from input ground (pin 6).

Figure 2 Output Waveforms

The TC9400 contains a "self-start" circuit to ensure the V/F converter always operates properly when power is first applied. In the event during "power-on" the op-amp output is below comparator threshold, and C_{REF} is already charged, a positive voltage step will not occur. The op-amp output will continue to decrease until it crosses the –2.5V threshold of the "self-start" comparator. When this happens, a resistor is connected to the op-amp input, causing the output to quickly go positive until the TC9400 is once again in its normal operating mode.

The TC9400 utilizes both bipolar and MOS transistors on the same substrate, taking advantage of the best features of each. MOS transistors are used at the inputs to reduce offset and bias currents. Bipolar transistors are used in the op amp for high gain, and on all outputs for excellent current driving capabilities, CMOS logic is used throughout to minimize power consumption.

PIN FUNCTIONS

Comparator Input

In the V/F mode, this input is connected to the amplifier output (pin 12) and triggers the 3 µs pulse delay when the input voltage passes its threshold. In the F/V mode, the input frequency is applied to the comparator input.

Pulse Freq Out

This output is an open-collector bipolar transistor providing a pulse waveform whose frequency is proportional to the input voltage. This output requires a pull-up resistor and interfaces directly with MOS, CMOS and TTL logic.

Freq/2 Out

This output is an open-collector bipolar transistor providing a square wave one-half the frequency of the pulse frequency output. This output requires a pull-up resistor and interfaces directly with MOS, CMOS, and TTL logic.

Output Common

The emitters of both the freq/2 out and the pulse freq out are connected to this pin. An output level swing from the collector voltage to ground or to the V_{SS} supply may be obtained by connecting to the appropriate point.

R_{BIAS}

Specifications for the TC9400 are based on R_{BIAS} = 100 kΩ ±10%, unless otherwise noted. R_{BIAS} may be varied between the range of 82 kΩ ≤ R_{BIAS} ≤ 120 kΩ.

Amplifier Out

The output stage of the operational amplifier. A negative-going ramp signal is available at this pin in the V/F mode. In the F/V mode, a voltage proportional to the frequency input is generated.

Zero Adjust

The noninverting input of the operational amplifier. The low-frequency set point is determined by adjusting the voltage at this pin.

I_{IN}

The inverting input of the operational amplifier and the summing junction when connected in the V/F mode. An input current of 10 µA is specified for nominal full scale, but an overrange current up to 50 µA can be used without detrimental effect to the circuit operation.

V_{REF}

A reference voltage from either a precision source or the V_{SS} supply may be applied to this pin. Accuracy will be dependent on the voltage regulation and temperature characteristics of the circuitry.

V_{REF} Out

The charging current for C_{REF} is derived from the internal circuitry and switched by the break-before-make switch to this pin.

V/F CONVERTER DESIGN INFORMATION

Input/Output Relationships

The output frequency (f_{OUT}) is related to the analog input voltage (V_{IN}) by the transfer equation:

$$\text{Frequency out} = \frac{V_{IN}}{R_{IN}} \times \frac{1}{(V_{REF})\,(C_{REF})} = f_{OUT}.$$

External Component Selection

R_{IN}

The value of this component is chosen to give a full-scale input current of approximately 10 µA:

$$R_{IN} \cong \frac{V_{IN}\ \text{Full Scale}}{10\ \mu A}.$$

$$\text{Example:}\quad R_{IN} \cong \frac{10V}{10\ \mu A} = 1\ M\Omega.$$

Note that the value is an approximation and the exact relationship is defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed to obtain full-scale frequency at V_{IN} full scale (see "Adjustment Procedure"). Metal film resistors with 1% tolerance or better are recommended for high-accuracy applications because of their thermal stability and low-noise generation.

C_{INT}

The exact value is not critical but is related to C_{REF} by the relationship:

$$3C_{REF} \le C_{INT} \le 10\,C_{REF}.$$

Improved stability and linearity are obtained when $C_{INT} \le 4C_{REF}$. Low-leakage types are recommended, although mica and ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 12 and 13.

C_{REF}

The exact value is not critical and may be used to trim the full-scale frequency (see "Input/Output Relationships"). Glass film or air trimmer capacitors are recommended because of their stability and low leakage. Locate as close as possible to pins 5 and 3.

V_{DD}, V_{SS}

Power supplies of ±5V are recommended. For high-accuracy requirements, 0.05% line and load regulation and 0.1 µF disc decoupling capacitors located near the pins are recommended.

Adjustment Procedure

Figure 1 shows a circuit for trimming the zero location. Full scale may be trimmed by adjusting R_{IN}, V_{REF}, or C_{REF}. Recommended procedure for a 10 kHz full-scale frequency is as follows:

(1) Set V_{IN} to 10 mV and trim the zero adjust circuit to obtain a 10 Hz output frequency.

(2) Set V_{IN} to 10V and trim either R_{IN}, V_{REF}, or C_{REF} to obtain a 10 kHz output frequency.

If adjustments ar performed in this order, there should be no interaction and they should not have to be repeated.

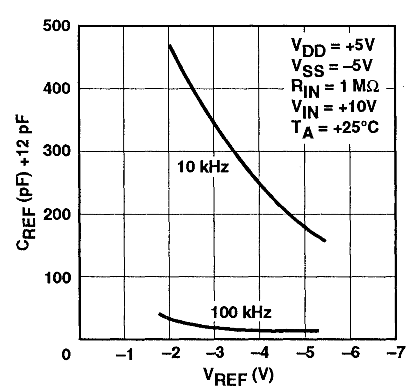
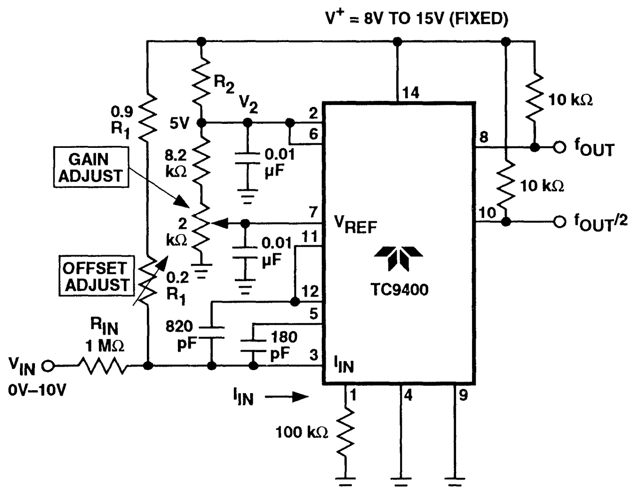


Figure 3 Recommended C_{REF} vs V_{REF}



V^+	R_1	R_2
10V	1 MΩ	10 kΩ
12V	14 MΩ	14 kΩ
15V	2 MΩ	20 kΩ

$$f_{OUT} = I_{IN} \times \frac{1}{(V_2-V_7)\,(C_{REF})}$$

$$I_{IN} = \frac{(V_{IN}-V_2)}{R_{IN}} + \frac{(V^+-V_2)}{(0.9\,R_1+0.2\,R_1)}$$

Figure 4 Fixed Voltage — Single Supply Operation

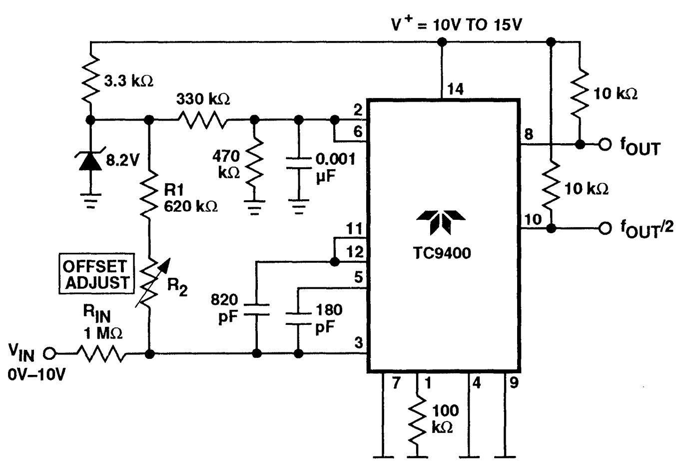


Figure 5 Variable Voltage — Single Supply Operation

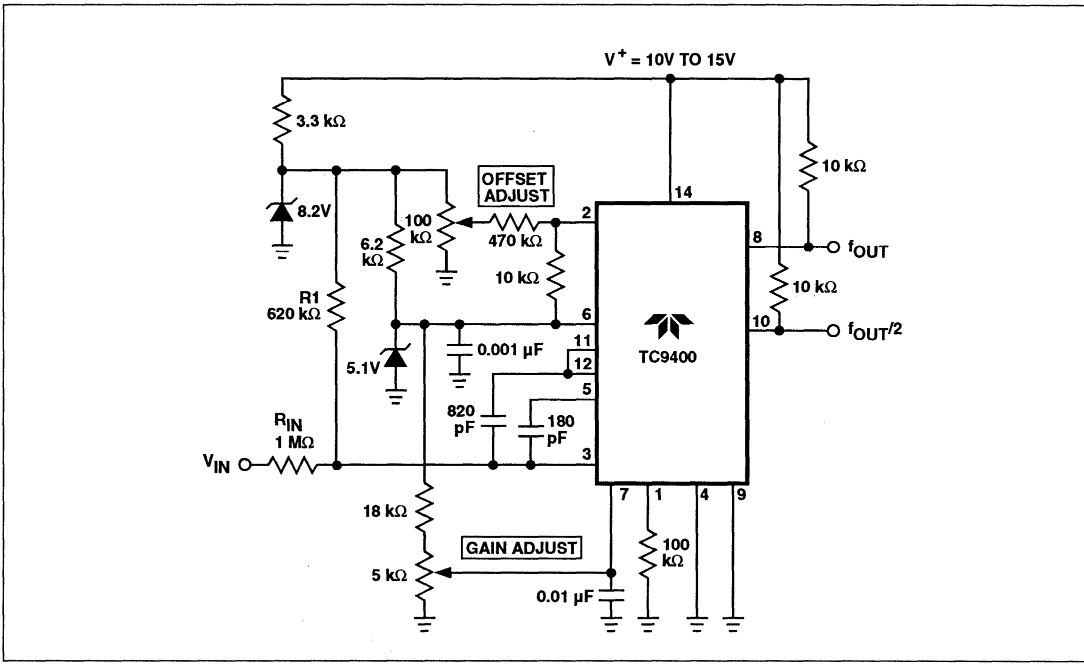


Figure 6 Single Variable Supply Voltage With Offset and Gain Adjust

ELECTRICAL CHARACTERISTICS:

V_{DD} = +5V, V_{SS} = –5V, V_{GND} = 0, V_{REF} = –5V, R_{BIAS} = 100 kΩ, Full Scale = 10 kHz, unless otherwise specified. T_A = +25°C, unless temperature range is specified –40°C to +85°C for E device, 0°C to +70°C for C device.

FREQUENCY-TO-VOLTAGE		TC9401			TC9400			TC9402			
Parameter	**Definition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Accuracy											
Nonlinearity (Note 5)	Deviation From Ideal Transfer Function as a Percentage Full-Scale Voltage		0.01	0.02		0.02	0.05		0.05	0.25	% Full Scale
Input Frequency Range (Note 6)	Frequency Range for Specified Nonlinearity	10		100k	10		100k	10		100k	Hz
Frequency Input											
Positive Excursion (Note 7)	Voltage Required to Turn Comparator On	0.4		V_{DD}	0.4		V_{DD}	0.4		V_{DD}	V
Negative Excursion (Note 7)	Voltage Required to Turn Comparator Off	–0.4		–2	–0.4		–2	–0.4		–2	V
Minimum Positive Pulse Width (Note 7)	Time Between Threshold Crossings		5			5			5		µs
Minimum Negative Pulse Width (Note 7)	Time Between Threshold Crossings		0.5			0.5			0.5		µs
Input Impedance		10			10			10			MW

ELECTRICAL CHARACTERISTICS (Cont.)

FREQUENCY-TO-VOLTAGE		TC9401			TC9400			TC9402			
Parameter	**Definition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Analog Outputs											
Output Voltage (Note 8)	Voltage Range of Op Amp Output for Specified Nonlinearity		$V_{DD}-1$			$V_{DD}-1$			$V_{DD}-1$		V
Output Loading	Resistive Loading at Output of Op Amp	2			2			2			kW
Supply Current											
I_{DD} Quiescent	Current Required From Positive Supply During Operation										
E Device (Note 9)			2	4		2	4				mA
C Device			2	6		2	6		3	10	mA
I_{SS} Quiescent	Current Required From Negative Supply During Operation										
E Device (Note 10)			–1.5	–4		–1.5	–4				mA
C Device			–1.5	–6		–1.5	–6		–3	–10	mA
V_{DD} Supply	Operating Range of Positive Supply	4		7.5	4		7.5	4		7.5	V
V_{SS} Supply	Operating Range of Negative Supply	–4		–7.5	–4		–7.5	–4		–7.5	V
Reference Voltage											
$V_{REF}-V_{SS}$	Range of Voltage Reference Input	–1			–1			–1			V

NOTES:
1. Full temperature range.
2. $I_{IN} = 0$.
3. Full temperature range, $I_{OUT} = 10$ mA.
4. $I_{OUT} = 10\ \mu A$.
5. 10 Hz to 100 kHz.
6. 5 µs minimum positive pulse width and 0.5 µs minimum negative pulse width.
7. $t_R = t_F = 20$ ns.
8. $R_L \geq 2\ k\Omega$.
9. Full temperature range, $V_{IN} = -0.1V$.
10. $V_{IN} = -0.1V$.
11. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly, but must be buffered by external resistors.

FREQUENCY-TO-VOLTAGE (F/V) CIRCUIT DESCRIPTION

When used as an F/V converter, the TC9400 generates an output voltage linearly proportional to the input frequency waveform.

Each zero crossing at the comparator's input causes a precise amount of charge ($q = C_{REF} \times V_{REF}$) to be dispensed into the op amp's summing junction. This charge in turn flows through the feedback resistor, generating voltage pulses at the output of the op amp. A capacitor (C_{INT}) across R_{INT} averages these pulses into a DC voltage which is linearly proportional to the input frequency.

F/V CONVERTER DESIGN INFORMATION

Input/Output Relationships

The output voltage is related to the input frequency (f_{IN}) by the transfer equation:

$$V_{OUT} = [V_{REF}\ C_{REF}\ R_{INT}]\ f_{IN}.$$

The response time to a change in f_{IN} is equal to (R_{INT} C_{INT}). The amount of ripple on V_{OUT} is inversely proportional to C_{INT} and the input frequency.

C_{INT} can be increased to lower the ripple. Values of 1 µF to 100 µF are perfectly acceptable for low frequencies.

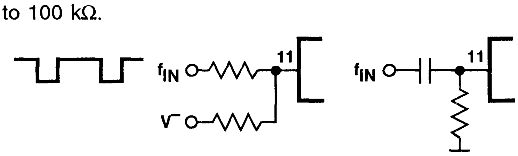
When the TC9400 is used in the single-supply mode, V_{REF} is defined as the voltage difference between pin 7 and pin 2.

Input Voltage Levels

The input signal must cross through zero in order to trip the comparator. To overcome the hysteresis, the amplitude must be greater than ±200 mV.

If only a unipolar input signal (f_{IN}) is available, it is recommended an offset circuit utilizing a resistor be used or the signal be coupled in via a capacitor.

For 100 kHz maximum input, R_{INT} should be decreased to 100 kΩ.



NOTE: C_{REF} should be increased for low f_{IN} max. Adjust C_{REF} so V_{OUT} is approximately 2.5V to 3V for maximum input frequency. When f_{IN} max is less than 1 kHz, the duty cycle should be greater than 20% to ensure C_{REF} is fully charged and discharged.

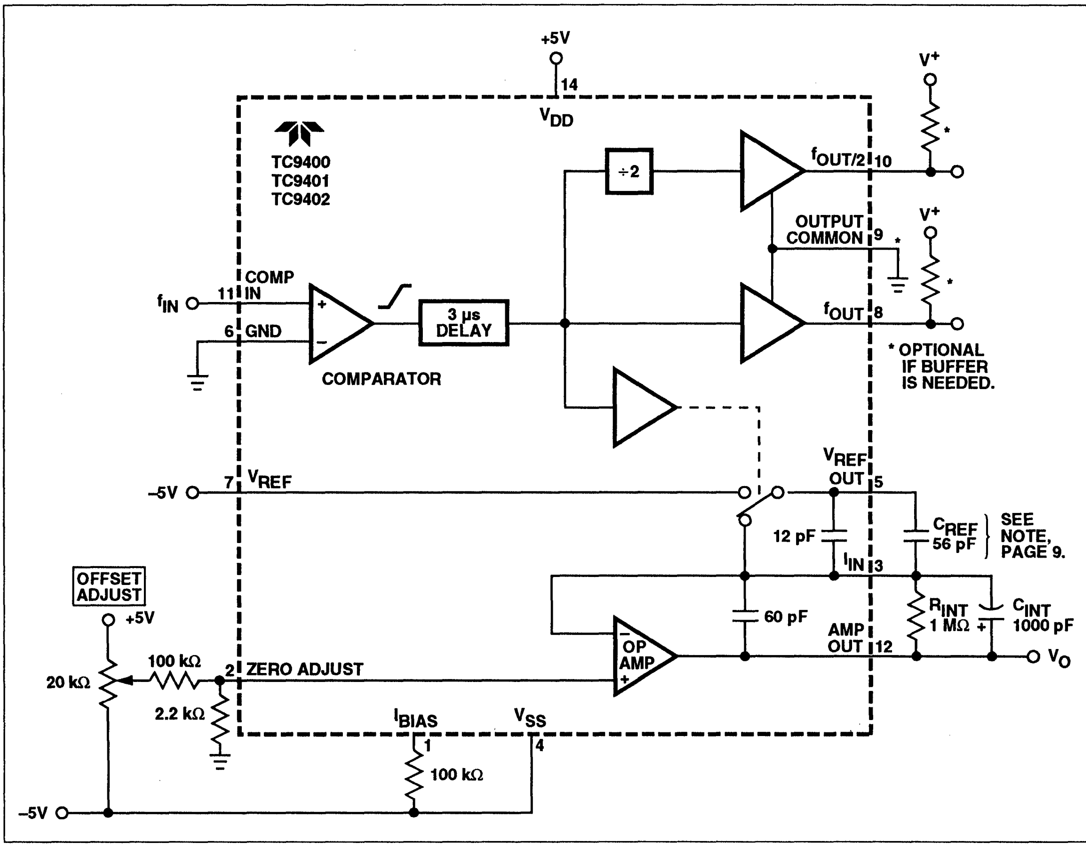


Figure 7 DC — 10 kHz F/V Converter

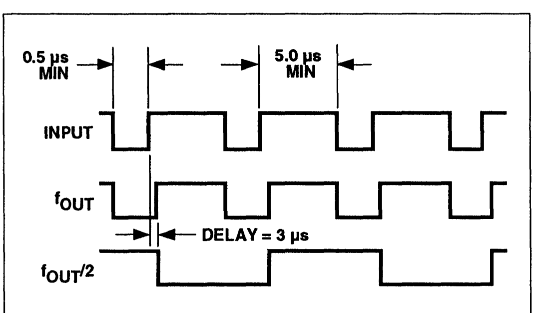
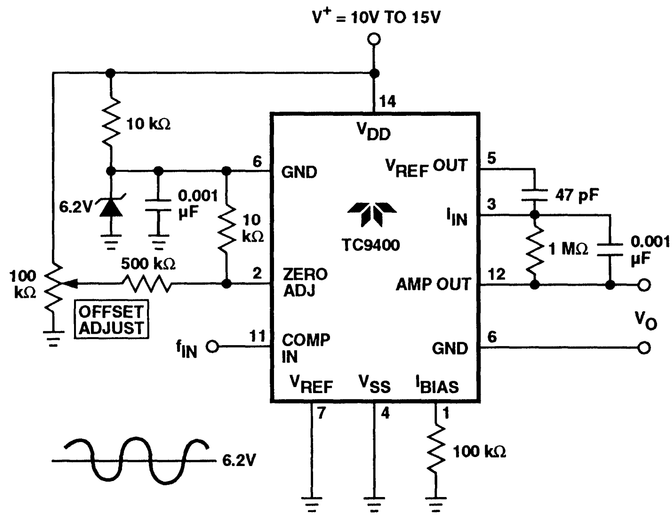


Figure 8 F/V Digital Outputs

Input Buffer

f_{OUT} and $f_{OUT}/2$ are not used in the F/V mode. However, these outputs may be useful for some applications, such as a buffer to feed additional circuitry. Then, f_{OUT} will follow the input frequency waveform, except that f_{OUT} will go high 3 µs after f_{IN} goes high; $f_{OUT}/2$ will be squarewave with a frequency of one-half f_{OUT}.

If these outputs are not used, pins 8, 9 and 10 may be left floating or connected to ground.



NOTES: 1. The input is now referenced to 6.2V (pin 6). The input signal must therefore be restricted to be greater than 4V (pin 6, 2V) and less than 10V to 15V (V_{DD}).

If the signal is AC coupled, a 100kΩ to 10 MΩ resistor must be placed between the input (pin 11) and ground (pin 6).

2. The output will now be referenced to pin 6 which is at 6.2V (V_Z). For frequency meter applications, a 1 mA meter with a series-scaling resistor can be placed across pins 6 and 12.

Figure 9 F/V Single Supply

The sawtooth ripple on the output of an F/V can be eliminated without affecting the F/V's response time by using the circuit in Figure 10. The circuit has a DC gain of +1. Any AC components (such as a ripple) are amplified positively via the lower path and negatively via the upper path. When both paths have the same gain, AC ripple is cancelled. The amount of cancellation is directly proportional to gain matching. If the two paths are matched within 10%, the ripple will be lowered by 1/10. For 1% matching, the ripple is lowered by 1/100. The 10 kΩ potentiometer is used to make the gain equal in both paths. This circuit is insensitive to frequency changes and signal waveshape.

F/V POWER-ON RESET

In F/V mode, the TC9400 output voltage will occasionally be at its maximum value when power is first applied. This condition remains until the first pulse is applied to f_{IN}. In most frequency-measurement applications this is not a problem, because proper operation begins as soon as the frequency input is applied.

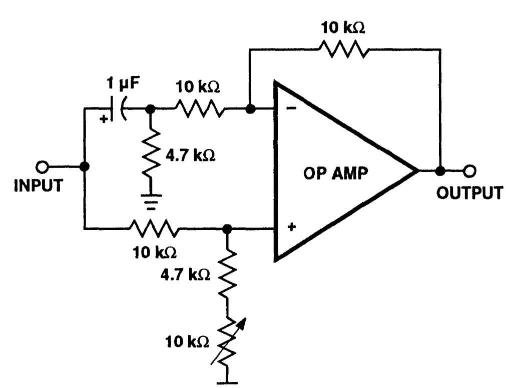


Figure 10 F/V Ripple Eliminator

In some cases, however, the TC9400 output must be zero at power-on without a frequency input. In such cases, a capacitor connected from pin 11 to V_{DD} will usually be sufficient to pulse the TC9400 and provide a power-on reset (see Figure 11A). Where predictable power-on operation is critical, a more complicated circuit, such as Figure 11B, may be required.

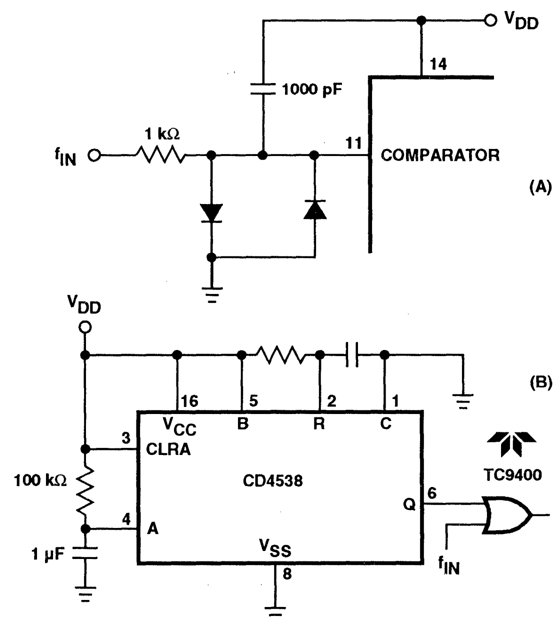


Figure 11 Power-On Operation/Reset

Section 4

Sensor Products

4

TELEDYNE COMPONENTS

TC620
TC621

SOLID STATE TEMPERATURE SENSOR

FEATURES

- ±3°C Absolute Temperature Accuracy
- 2 kV ESD Protection on All Pins
- Replaces Mechanical Thermostats and Switches
- On-Chip Temperature Sense (TC620)
- External Temperature Sense (TC621)
- 8-Pin DIP or SOIC for Direct PCB Mounting
- 2 User-Programmable Temperature Set Points
- 2 Independent Temperature Limit Outputs
- Heat/Cool Regulate Output

APPLICATIONS

- System Over-Temperature Shutdown
- Advanced Thermal Warning
- Fan Speed Control Circuits
- Vibration-Immune Temperature Sensing
- Accurate Appliance Temperature Sensing

GENERAL DESCRIPTION

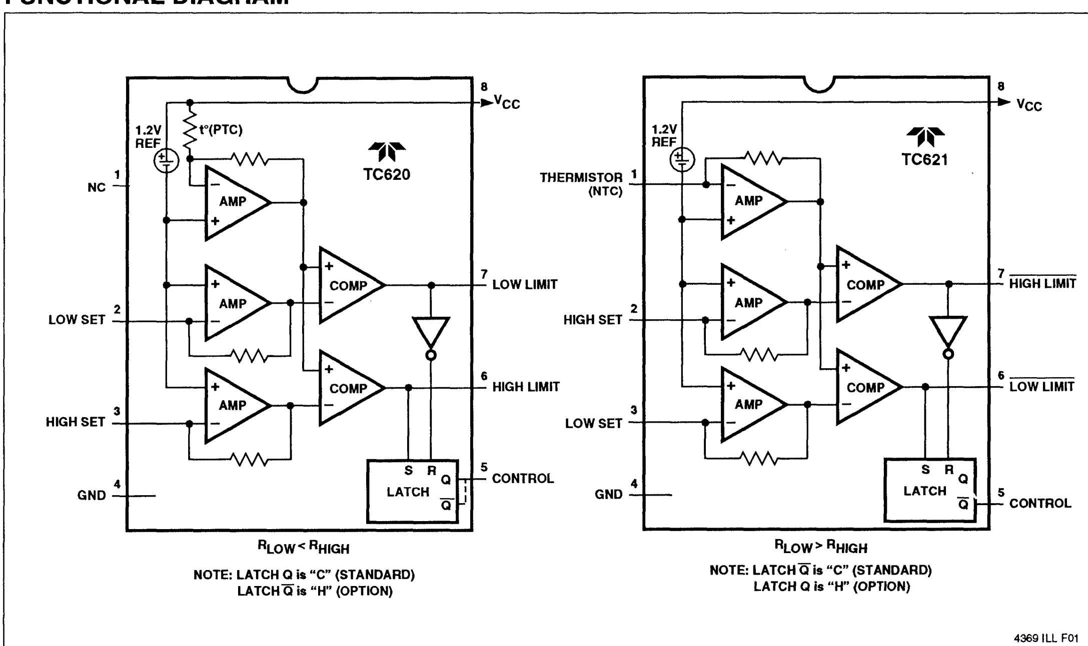
The TC620 and TC621 are solid-state temperature switches designed to replace mechanical switches in temperature sensing and control applications. Ambient temperature is sensed and compared to programmable temperature minimums and maximums.

Both devices provide a LOW LIMIT and HIGH LIMIT logical output as well as a CONTROL output. On the TC620, the LOW LIMIT is low when the measured temperature is below the low temperature set-point and the HIGH LIMIT is low when the measured temperature is below the high temperature set-point. The TC621 provides the same output functions except that the logical states are inverted. These outputs allow for easy 'over' and 'under' temperature detection.

The CONTROL output provides a programmable hysteresis in that it goes high when the measured temperature goes above the HIGH LIMIT set-point and returns to low when the measured temperature goes below the LOW LIMIT set-point. The CONTROL output of either device is easily applied to a temperature control system.

4

FUNCTIONAL DIAGRAM



Our proprietary technology provides excellent absolute temperature accuracy (±3°C). The low current requirement of these devices make them especially appealing in battery powered applications. The TC620 and TC621 have no moving parts so they are rugged and work well in equipment that needs to take a lot of abuse. Automotive, marine and industrial users will benefit from the ruggedness of these devices.

The LOW LIMIT and HIGH LIMIT temperatures are set by connecting the appropriate resistors to the LOW SET and HIGH SET inputs. The value of these SET resistors are a function of the temperature sensing element.

Internal Temperature Sensor (TC620)

The TC620 incorporates an on-board positive-temperature-coefficient (PTC) thermal sensor which reacts to the internal temperature of the die. The LOW SET resistor (pin 2) should always be lower than the HIGH SET resistor (pin 3) to insure proper operation.

External Temperature Sensor (TC621)

The TC621 performs the same function as the TC620 but employs a user supplied temperature sensing device. The most common type of temperature sensor is a negative-temperature-coefficient (NTC) thermistor. An NTC sensor requires that the input and output functions be reversed from that of the TC620. This means that the HIGH SET resistor (pin 2) should always be lower than the LOW SET resistor (pin 3) to insure proper operation. See the applications section of this data sheet for recommendations on selecting the thermistor.

DESIGN PARAMETERS

The designer must be sure that the LOW SET programming resistor is smaller than the HIGH SET programming resistor for the TC620 or that the LOW SET resistor is larger than the HIGH SET resistor when using the TC621 with an NTC external thermistor. No damage will be done to the part if this is not correct but the CONTROL output logic will be effected.

The LOW LIMIT and HIGH LIMIT outputs will go to a 'high' state ('low' state for TC621) whenever the temperature of the device (or external thermistor) exceeds the temperature programmed for the respective inputs.

The CONTROL output latch will go to a 'high' whenever the sensed temperature exceeds the HIGH SET temperature and will go to a 'low' if the sensed temperature drops below the LOW SET temperature. A bonding option may be used to invert the CONTROL output logic for heating applications. The part number for this option has an 'H' instead of a 'C' placed after the '620' or '621' digits.

If power is applied to the device while the sensed temperature is between the LOW SET temperature and the HIGH SET temperature, the LOW LIMIT output will go 'high' ('low' for the TC621) and the CONTROL output will go 'high'.

The resistance value for the TC620 can be determined by inserting the desired trip temperature (T) into the following formulas:

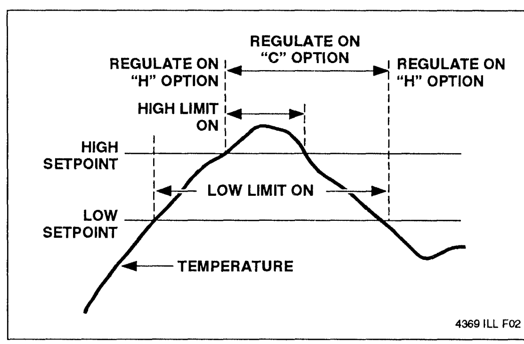
For Temperatures
below 70°C $R_{trip} = 0.783 \times T + 91$
above 70°C $R_{trip} = T + 77$

Where Rtrip = Programming resistor value in k ohms
T = Desired trip temperature in degrees C

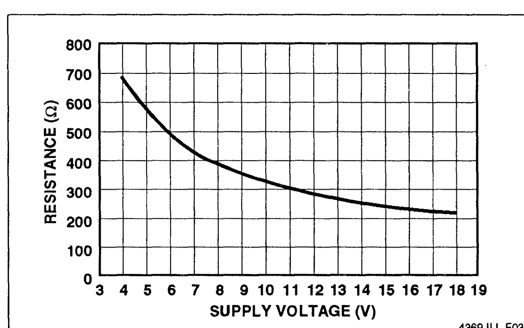
For example, to program the device to trip at 50°C, the programming resistor would be:

$R_{trip} = 0.783 \times 50 + 91 = 130.2\ k\Omega.$

The TC621 can source or sink 10 mA per output. The outputs of the TC620 can source or sink 1mA. If higher currents are utilized in the TC620, the device will generate internal heat, possibly causing erroneous temperature sensing.



TC620/621 Input vs. Output Logic



Output Resistance vs. Supply Voltage

SOLID STATE TEMPERATURE SENSOR

TC620
TC621

ABSOLUTE MAXIMUM RATINGS

Power Dissipation
- Plastic 1W
- CerDIP .... 800 mW

Derating Factors
- Plastic .... 8 mW/°C
- CerDIP .... 6.4 mW/°C

Supply Voltage 20V
Input Voltage Any Input .... (Gnd -0.3) to (VDD +0.3)
Operating Temperature
- M Version .... -55 to +125°C
- E Version .... -40 to +85°C
- C Version .... 0 to +70°C

Maximum Chip Temperature .... +150°C
Storage Temperature .... -65 to +150°C
Lead Temperature (10 sec) .... +300°C

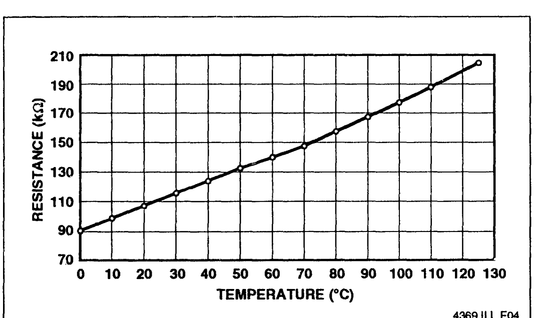
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part No.	Package	Ambient Temperature
TC620CCOA	8-Pin SOIC	0°C to +70°C
TC620CEOA	8-Pin SOIC	-40°C to +85°C
TC620CCPA	8-Pin Plastic DIP	0°C to +70°C
TC620CEPA	8-Pin Plastic DIP	-40°C to +85°C
TC620CMJA	8-Pin Ceramic DIP	-55°C to +125°C
TC621CCOA	8-Pin SOIC	0°C to+ 70°C
TC621CEOA	8-Pin SOIC	-40°C to +85°C
TC621CCPA	8-Pin Plastic DIP	0°C to +70°C
TC621CEPA	8-Pin Plastic DIP	-40°C to +85°C
TC621CMJA	8-Pin Ceramic DIP	-55°C to +125°C
TC620HCOA	8-Pin SOIC	0°C to +70°C
TC620HEOA	8-Pin SOIC	-40°C to +85°C
TC620HCPA	8-Pin Plastic DIP	0°C to +70°C
TC620HEPA	8-Pin Plastic DIP	-40°C to +85°C
TC620HMJA	8-Pin Ceramic DIP	-55°C to +125°C
TC621HCOA	8-Pin SOIC	0°C to +70°C
TC621HEOA	8-Pin SOIC	-40°C to +85°C
TC621HCPA	8-Pin Plastic DIP	0°C to +70°C
TC621HEPA	8-Pin Plastic DIP	-40°C to +85°C
TC621HMJA	8-Pin Ceramic DIP	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

Parameter		Conditions		Min	Typ	Max	Unit
Supply Voltage				4.5		18	V
Supply Current					140	200	μA
Output Resistance		Output High or Low			400	1000	Ω
Output Current	620	Temp Sensed	Source/Sink			1	mA
	621	Temp Sensed	Source/Sink			10	mA
Output Current	620	Cool/Heat	Source/Sink			1	mA
	621	Cool/Heat	Source/Sink			10	mA
Absolute Accuracy		T = Programmed Temperature		T -3	T	T +3	°C

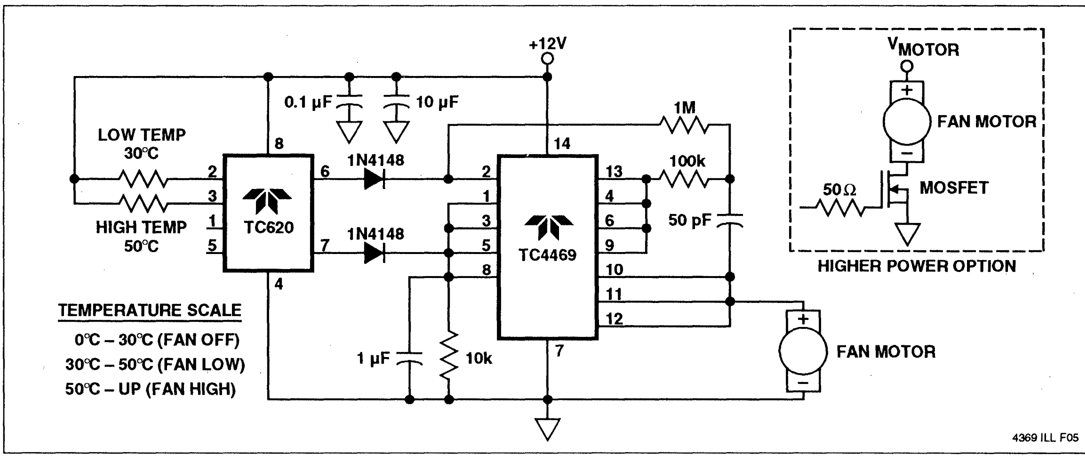


TC620 Sense Resistors vs. Trip Temperature

TYPICAL APPLICATIONS

Dual Speed Temperature Control

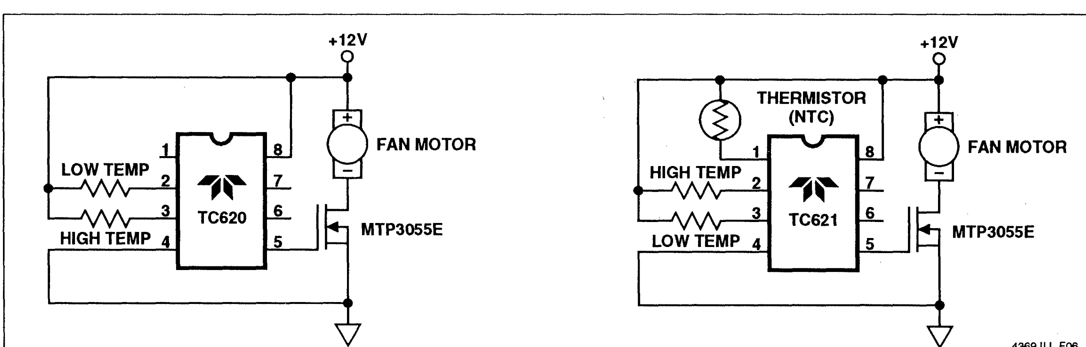
The Dual Speed Temperature Control adds features to the basic controller by using the TC4469 quad driver. Two of the drivers are configured in a simple oscillator. When the temperature is below the LOW TEMP set point, the output of the driver is off. When the temperature exceeds the LOW TEMP set point, the TC4469 gates the oscillator signal to the outputs of the driver. This square wave signal modulates the remaining outputs and drives the motor at a low speed. If this speed cannot keep the temperature below the HIGH TEMP set point, then the driver turns on continuously which increases the fan speed to high. The TC620 will monitor the temperature and only allow the fan to operate when needed, and at the required speed to maintain the desired temperature. A higher power option can be designed by adding a resistor and a power MOSFET.



Temperature Controlled Fan

In the Temperature Controlled Fan schematic, a high and a low temperature is selected by two 'set' resistors. The TC620 then monitors the ambient temperature and will turn on the FET switch when the temperature exceeds the HIGH TEMP set point. The fan remains on until the temperature decreases to the LOW TEMP set point. This provides the hysteresis. In this application, the fan will not turn on unless needed. This makes for a high-power fan control with only four parts.

The TC621 uses an external themistor to monitor the ambient temperature.



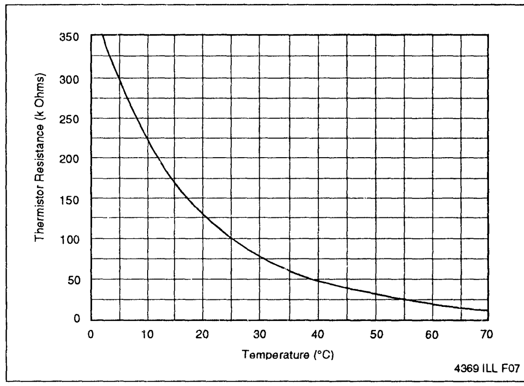
USING THE TC621

The TC621 uses an external thermistor to monitor the controlling temperature. A thermistor with a resistance value of approximately 100kΩ at 25°C is recommended.

Typical thermistors exhibit a negative temperature coefficient (NTC) which must be considered when selecting the set-point resistors. A temperature set-point is selected by picking a resistor whose value is equal to the resistance of the thermistor at the desired temperature.

A 30kΩ resistor between HIGH TEMP (pin 2)and V_{DD} (pin 8) will set the high temperature trip point at +50°C and a 49kΩ resistor on LOW TEMP (pin 3) will set the low temperature trip point to +40°C.

TYPICAL NTC THERMISTOR

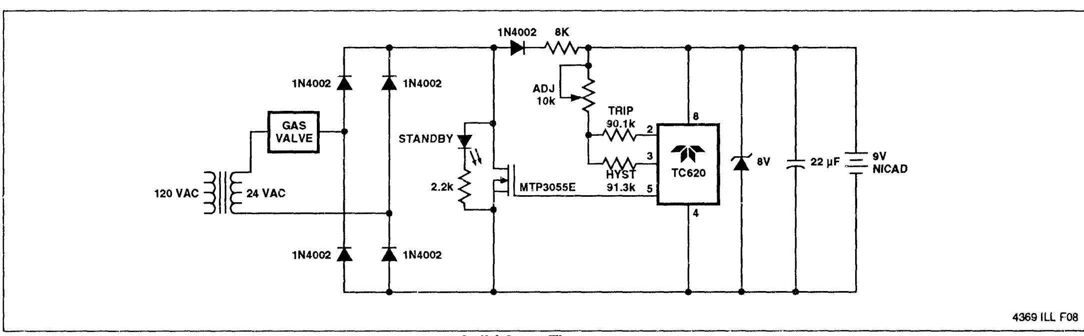


Typical Thermistor Resistance vs Temperature

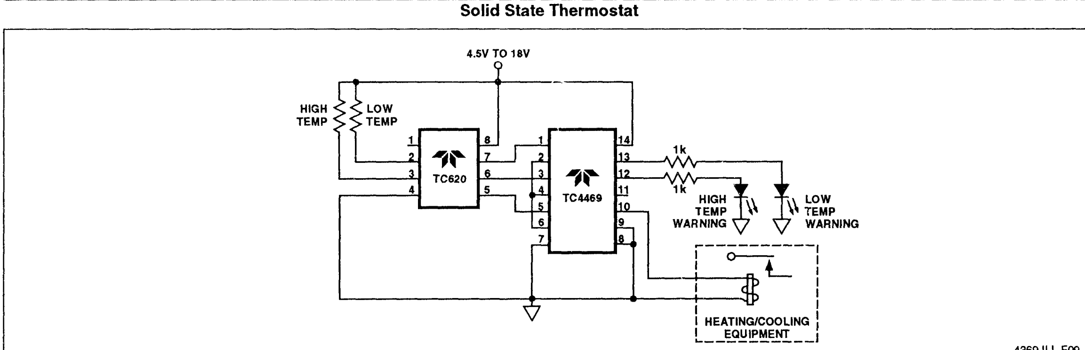
TYPICAL APPLICATIONS

Solid State Thermostat

The Solid State Thermostat diagram shows how the TC620 can be used to control home, industrial and commercial heating and cooling applications in a low cost, simple approach. The TC620 monitors the temperature and when heating is required, turns on the FET swich. This applies power to the gas valve and turns off the "standby" indicator. The Nicad battery provides power to the circuit when the FET is energized. D5 and R2 provide current limited power to the circuit when the FET is off. This also keeps the Nicad battery recharged. R3 and R4 set the desired hysteresis to prevent rapid cycling of the heating or cooling equipment.



Solid State Thermostat



TC620 Heating/Cooling Application

NOTES

SOLID-STATE TEMPERATURE SENSOR

FEATURES

- 2 kV ESD Protection on All Pins
- On-Chip Temperature Sensing
- Replaces Mechanical Thermostats and Switches
- TO-220 package for "Hot Spot" Mounting
- TO-92 Package for Direct Circuit Board Mounting
- ±3°C Absolute Temperature Accuracy
- 10 mA Output Signal TO-92 Package
- 50 mA Output Signal TO-220 Package

APPLICATIONS

- System Overtemperature Shutdown
- Advanced Thermal Warning
- Fan Speed Control Circuits
- Vibration-Immune Temperature Sensing
- Accurate Appliance Temperature Sensing

GENERAL DESCRIPTION

The TC626 is a solid-state temperature sensor designed to replace mechanical switches in temperature-sensing applications. The ambient temperature is sensed and compared to an internal programmed temperature. The preset internal temperatures can be ordered in 5°C increments, from 0°C to +125°C.

Our proprietary technology provides high, absolute temperature accuracy (±3°C). Since there are no moving parts, the TC626 is rugged and works well in harsh environments that could damage and reduce the life of mechanical temperature sensors. Automotive and industrial users will benefit from its immunity to vibration.

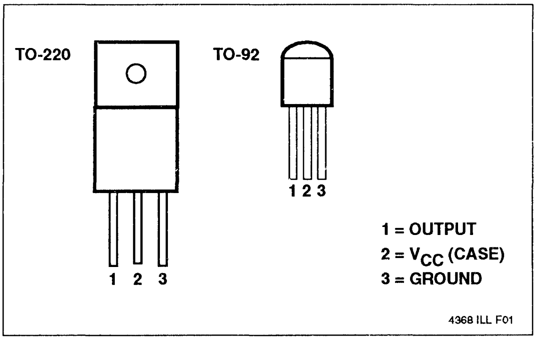
DESIGN PARAMETERS

The output will remain low until the internally programmed temperature is reached. The device then switches its output high. This output signal can source and sink up to 10 mA (TO-92 package) and 50 mA (TO-220 package).

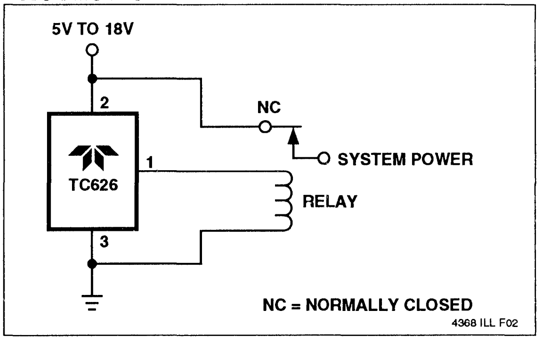
The heat-sinking ability of the surface to which the device is attached can permit higher power applications since the internal heating of the device will be negligible compared to the ambient temperature.

The hysteresis of the TC626 is 5 degrees at 20°C. At higher temperatures, it increases.

PIN CONFIGURATIONS



SYSTEM OVERTEMPERATURE PROTECTION



TC626

ORDERING INFORMATION

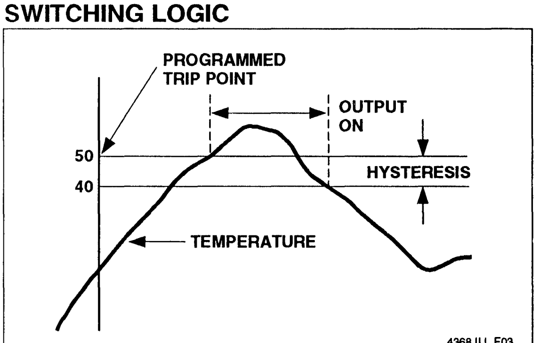
Part Number*	Package	Temperature Range
TC626XXXCAB	3-Pin TO-220	0°C to +70°C
TC626XXXEAB	3-Pin TO-220	–40°C to +85°C
TC626XXXVAB	3-Pin TO-220	–40°C to +125°C
TC626XXXCZB	3-Pin TO-92	0°C to +70°C
TC626XXXEZB	3-Pin TO-92	–40°C to +85°C
TC626XXXVZB	3-Pin TO-92	–40°C to +125°C

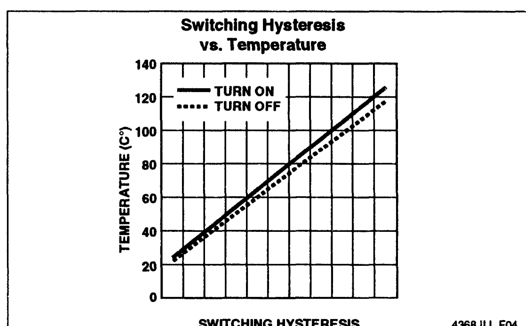
* XXX is temperature in 5°C increments, from 0 to +125°C (a 50°C part would be TC626050CAB).

ELECTRICAL CHARACTERISTICS: V_{DD} = +5V unless otherwise specified.

Parameter	Test Conditions	Min	Typ	Max	Units
Supply Voltage		4.5	—	18	V
Supply Current		—	300	600	µA
Output Resistance	Output High or Low	—	—	75	W
Output Current	Source/Sink, V_{CC} = 18V	—	—	25	mA
	Source/Sink, V_{CC} = 4.5V	—	—	10	mA
Absolute Accuracy		T–3	T	T+3	°C
Differential		3.5	5	6.5	°C

SWITCHING LOGIC





![TELEDYNE COMPONENTS]

TELEDYNE COMPONENTS

TC675
TC676

FAST NiCAD/Ni-HYDRIDE BATTERY CHARGER

FEATURES

- Fast Charge Cycle
- Automatic Overcharge Protection
- Fail Safe Fast Charge Shut-Off
- Programmable Min/Max Ambient Limits
- Selectable Charge Rate
- Automatic Trickle Charge
- Forced Trickle Charge (TC675)
- Timer Reset Pin (TC676)
- Safety Features
- Temperature Controlled Shut-Off
- Time Controlled Shut-Off
- Dual Mode Automatic Shut-Off
- Automatic Battery Insertion Detector

APPLICATIONS

- Battery Powered Applications
  - —Power Tools
  - —Laptop/Notebook Computers
  - —Medical
  - —Emergency Lighting Systems
  - —Communications
  - —Cellular Phones/Mobile Radio
  - —Portable Instruments

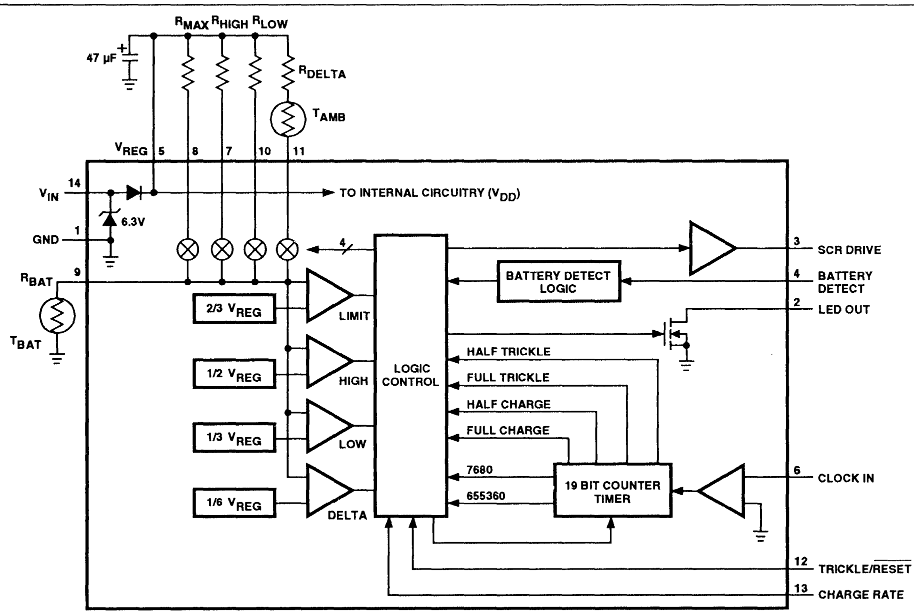
GENERAL DESCRIPTION

The TC675 and TC676 are designed for use with both NiCad and NiHydride batteries. These two devices meet the needs of the system designer whose battery charge applications require fast, reliable, and safe design.

The many automatic, programmable and selectable features of these devices provide capabilities found only in more expensive implementations. This, combined with inherent device capability of use in both AC or DC power sources, provide a flexible cost-effective solution to battery recharge maintenance.

4

FUNCTIONAL BLOCK DIAGRAM



NOTE: PIN NUMBERS REFER TO 14-PIN DIP

* TC675 'TRICKLE', '1' — TRICKLE-CHARGE
TC676 'RESET', '0' — FAST-CHARGE

4367 ILL F01

TC675
TC676

ORDERING INFORMATION

Part No.	Package	Operating Temp Range
TC675CPD	14-Pin Plastic DIP	0°C to +70°C
TC675EPD	14-Pin Plastic DIP	–40°C to +85°C
TC675MJD	14-Pin Ceramic DIP	–55°C to +125°C
TC675COE	16-Pin Plastic SOIC	0°C to +70°C
TC676CPD	14-Pin Plastic DIP	0°C to +70°C
TC676EPD	14-Pin Plastic DIP	–40°C to +85°C
TC676MJD	14-Pin Ceramic DIP	–55°C to +125°C
TC676COE	16-Pin Plastic SOIC	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Power Dissipation
- Plastic .... 1000 mW
- Ceramic .... 800 mW

Derating Factors
- Plastic .... 8 mW/°C
- Ceramic .... 6.4 mW/°C

Operating Temperature
- M Version .... –55°C to +125°C
- E Version .... –40°C to +85°C
- C Version .... 0°C to +70°C

Storage Temperature .... –65°C to +150°C
Lead Temperature (10 sec) .... +300°C
Max Zener Current (I_{IN}) .... 50 mA

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the Operational Specifications is not implied. Any exposure to Absolute Maximum Rating Conditions may affect device reliability.

OPERATIONAL SPECIFICATIONS: unless otherwise specified T_A = +25°C; I_S = 6 mA.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply						
I_S	Supply Current	(thru current limit resistor)	1	6	30	mA
V_Z	Zener Clamp Voltage	I_Z = 6 mA	6	6.3	7	V
R_Z	Zener Output Resistance	I_Z = 10 mA to 30 mA	—	10	20	Ω
V_{DD}	DC Input on V_{REG}	V_{IN} Open	4	5	6	V
I_{DD}	Internal Circuit Current	V_{DD} (V_{REG}) = 5V	—	0.3	1	mA
Regulator						
V_{REG}	Regulated Output	I_{REG} = 5 mA	5	—	6	V
R_{REG}	V_{REG} Output Resistance	I_{REG} = 0 mA to 5 mA	—	38	45	Ω
Switch Resistance (r_{DS} ON)						
RSW_{MAX}	MAX Switch		—	—	200	Ω
RSW_{HIGH}	HIGH Switch		—	—	450	Ω
RSW_{LOW}	LOW Switch		—	—	350	Ω
RSW_{DELTA}	DELTA Switch		—	—	300	Ω
RSW_{LED}	LED Drive		—	—	80	Ω
Threshold Voltage Tolerance						
δV_{MAX}	MAX	2/3 V_{REG}	—	±4	±10	%
δV_{HIGH}	HIGH	1/2 V_{REG}	—	±4	±10	%
δV_{LOW}	LOW	1/3 V_{REG}	—	±4	±10	%
δV_{DELTA}	DELTA	1/6 V_{REG}	—	±4	±10	%
$TC\delta V$	Threshold Voltage Temp Coefficient		—	±0.01	±0.1	%/°C

OPERATIONAL SPECIFICATIONS (Cont): unless otherwise specified $T_A = +25°C$; $I_S = 6$ mA.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Output						
$I_{OH}G$	SCR Gate Drive Source		—	5	—	mA
$I_{OL}G$	SCR Gate Drive Sink		—	3	—	mA
$V_{OL}L$	LED Low Output Voltage	$I_{OL}L = 10$ mA	—	—	0.8	V
Digital Input						
$I_{IL}CR$	CHARGE RATE Pull-up Current		—	—	10	μA
$I_{IH}TR$	TRICKLE/RESET Pull-down Current		—	—	25	μA
$I_{IL}BD$	BATTERY DETECT Pull-up Current		—	—	20	μA

ELECTRICAL CHARACTERISTICS: unless otherwise specified T_A = Operating Temperature Range; $I_S = 6$ mA.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply						
I_S	Supply Current	(thru current limit resistor)	1.2	6	30	mA
V_Z	Zener Clamp Voltage	$I_Z = 6$ mA	5.5	—	7.5	V
R_Z	Zener Output Resistance	$I_Z = 10$ mA to 30 mA	—	—	25	Ω
V_{DD}	DC Input on V_{REG}	V_{IN} Open	4	5	6	V
I_{DD}	Internal Circuit Current	V_{DD} (V_{REG}) = 5V	—	0.5	1.2	mA
Regulator						
V_{REG}	Regulated Output	$I_{REG} = 0$ mA to 5 mA	4.8	—	7	V
R_{REG}	V_{REG} Output Resistance	$I_{REG} = 5$ mA	—	45	60	Ω
Switch Resistance (r_{DS} ON)						
RSW_{MAX}	MAX Switch		—	—	260	Ω
RSW_{HIGH}	HIGH Switch		—	—	510	Ω
RSW_{LOW}	LOW Switch		—	—	410	Ω
RSW_{DELTA}	DELTA Switch		—	—	360	Ω
RSW_{LED}	LED Drive		—	—	100	Ω
Threshold Voltage Tolerance						
δV_{MAX}	MAX	2/3 V_{REG}	—	—	±10	%
δV_{HIGH}	HIGH	1/2 V_{REG}	—	—	±10	%
δV_{LOW}	LOW	1/3 V_{REG}	—	—	±10	%
δV_{DELTA}	DELTA	1/6 V_{REG}	—	—	±10	%
$TC\delta V$	Threshold Voltage Temp Coefficient		—	—	0.1	%/°C
Output						
$I_{OH}G$	SCR Gate Drive Source		—	5	—	mA
$I_{OL}G$	SCR Gate Drive Sink		—	3	—	mA
$V_{OL}L$	LED Low Output Voltage	$I_{OL}L = 10$ mA	—	—	1	V
Digital Input						
$I_{IL}CR$	CHARGE RATE Pull-up Current		—	—	15	μA
$I_{IH}TR$	TRICKLE/RESET Pull-down Current		—	—	35	μA
$I_{IL}BD$	BATTERY DETECT Pull-up Current		—	—	25	μA

TIMER-COUNTER

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Charge Time Counter	(1.517 Hr @ 120 Hz)	—	655360	—	Counts
	Delay Time Counter	(1.07 Min @ 120 Hz)	—	7680	—	Counts

DEVICE OPERATION

(All pin numbers refer to the 14-pin dip package)

Temperature Control

Safety is critical in charging NiCad/Ni-Hydride batteries because a fast-charge applied under the wrong conditions may cause severe damage to the battery and it's surroundings. The battery temperature is monitored by an external thermistor and the controller will not allow the battery to start a fast-charge cycle while the battery temperature is too hot or too cold. A NiCad/Ni-Hydride battery tends to warm up during a fast-charge cycle so a temperature that was too high to allow the charging to start may not be too high to allow the charging to continue. Another temperature threshold causes the charger to stop the fast-charge cycle as soon as the battery temperature gets too high.

A charger may also be required to work in cold ambient temperatures. The preprogrammed absolute maximum charging temperature may be too high for these conditions so a separate 'delta' temperature may be used. This will stop the fast-charge cycle if the battery temperature exceeds the ambient temperature by a predetermined amount. This option requires a second thermistor to monitor the ambient temperature.

Time Control

The TC675 and TC676 both use an on-board timer-counter which limits the maximum duration of the fast-charge cycle to 1.5 hours (1.8 hrs @ 50 Hz AC power). There is also a time delay of 60 seconds (77 sec @ 50 Hz AC power) before starting a fast-charge cycle. This delay gives the battery temperature sensor time to stabilize.

The counters are clocked by the full-wave rectified AC input. This clock rate is divided by 655,360 to time out the 1.517 hour (1.82 hrs @ 50 Hz AC power) maximum for the fast-charge cycle. A faster or slower clock may be used to modify the timing.

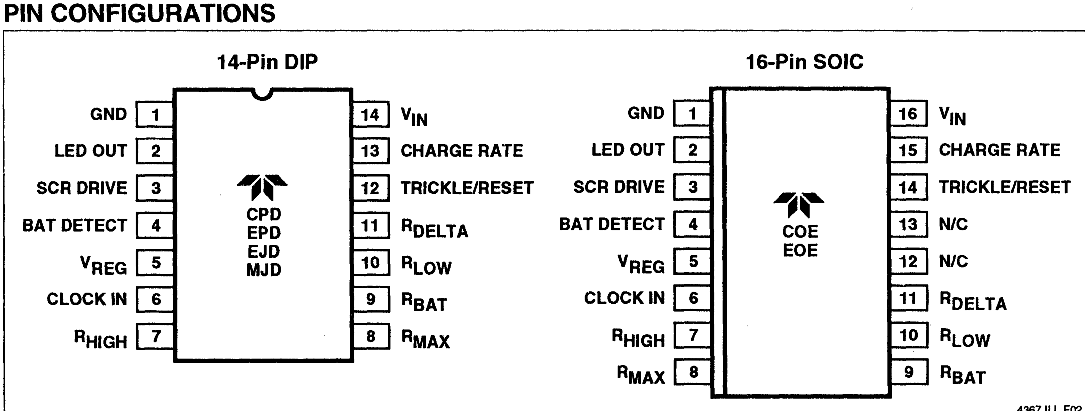
Full-Charge or Half-Charge Option

Both the TC675 and TC676 have a half-charge selection option. The CHARGE RATE input has an internal pull-up to select the full-charge mode (7/8 duty cycle). A low on this pin will select the half-charge mode (7/16 duty cycle). This input may be selected or toggled anytime during a fast-charge cycle without effecting the time-out sequence.

Trickle-Charge

The trickle-charge mode of the TC675 and the TC676 runs at ≈7% of the fast-charge mode (1/16 duty cycle for full-charge and 1/32 duty cycle for half-charge) and is the default mode whenever the fast-charge cycle is not running.

PIN CONFIGURATIONS



TRICKLE/RESET (PIN 12)

The only difference between the TC675 and the TC676 is the operation of the input on pin 12.

On the TC675 (pin 12 = 'TRICKLE'), a high (V_{DD}) on this pin will hold the charger in the trickle-charge mode. The internal timer will continue to count down. If the timer hasn't timed out, the charger will go back to the full-charge mode if this pin is returned to low (0V).

On the TC676 (pin 12 = 'RESET'), low transition (V_{DD} to 0V) on this pin will reset the timer and initialize a fast-charge cycle.

BATTERY SENSE (PIN 4)

This input is internally pulled up to about 1 volt. It is designed to be capacitively coupled to the cathode of the SCR (the positive terminal of the battery). Without a battery present, the pulses from the full-wave rectified AC signal are coupled by a bypass resistor around the SCR into the battery input through the capacitor. This produces a zero-crossing waveform at the battery pin which is interpreted as a 'no battery' condition. The presence of a battery will prevent these zero-crossings and the TC675/TC676 can begin a charge sequence.

Some battery packs contain a diode in series with the cells for safety purposes. This diode may prevent the battery from clamping the waveform to prevent zero-crossings. The auxiliary detect circuitry should be added to cause the diode, if present, to forward bias, which will then clamp the waveform to prevent zero-crossings and will indicate the presence of the battery.

CLOCK IN (PIN 6)

This input accepts the rectified AC signal and uses the pulses to establish timing. The waveform must reach zero volts during the pulse off time for accurate timing. Noise on this line could cause false clock triggering which can be prevented by placing a 0.01 µF capacitor from pin 6 to ground. This input is internally clamped to the V_{DD} (V_{DD}) potential (≈6V). A current limiting resistor must be used to connect the rectified AC signal.

SCR DRIVE (PIN 3)

A 1.5 kHz pulse is the output on this pin which turns on the SCR during each cycle of the rectified AC waveform. This signal should be capacitively coupled to the gate of the SCR. A 0.01 µF capacitor will effectively turn on the SCR and block any DC component.

CHARGE RATE (PIN 13)

This input has an internal pull-up which selects the normal-charge mode as default. A low on this pin will select 1/2 the current charge rate, i. e. if the charger is in full-charge then a low on pin 13 will select 1/2 full-charge, if the charger is in trickle-charge then 1/2 trickle-charge is selected.

LED OUTPUT (PIN 2)

This pin has a pull-down resistor to ground. With power applied and no battery installed, and during the 1 minute start delay, the transistor is on steady. The output will toggle at a 3 Hz rate during a fast-charge cycle. The output will stay on steady during the trickle-charge mode.

CONTROL TEMPERATURE

Each control temperature has a unique voltage threshold which is derived as a ratio of an internal, zener generated reference voltage (V_{REG}).

T_{MAX} ($\delta V_{MAX} = 2/3\ V_{REG}$)
the charger will stop the fast-charge mode if the battery temperature reaches this value.

T_{HIGH} ($\delta V_{HIGH} = 1/2\ V_{REG}$)
the charger will not start the fast-charge mode if the battery temperature is above this value.

T_{LOW} ($\delta V_{LOW} = 1/3\ V_{REG}$)
the charger will not start the fast-charge mode if the battery temperature is below this value.

T_{DELTA} ($\delta V_{DELTA} = 1/6\ V_{REG}$)
the charger will stop the fast-charge mode if the battery temperature exceeds the ambient temperature by this value.

THERMISTOR TEMPERATURE SENSOR

A common type of thermistor for this application is a negative-temperature-coefficient (NTC) with a relatively high resistance ratio. Some examples of this type are KC009-ND, KC020-ND or RL1006-53 from Keystone.

Thermistor Characteristics

The transfer function (Resistance vs. Temperature) of a normal NTC thermistor takes the form:

$$\ln R_T = A_0 + A_1/T + A_2/T^2 = \ldots + A_N/T^N \text{ (T in °Kelvin)}$$

The first three terms of this equation are sufficient to give a fit of better than ±0.01°C. The coefficients may be determined by setting up 3 simultaneous equations based on 3 known points.

The following calculations are based on a typical NTC thermistor (Keystone RL1006-53.4K-140-D1) with resistance values of 48.15 kΩ at 40°C (313.15°K), 100 kΩ at 25°C (298.15 K) and 221.8 kΩ at 10°C (282.15°K).

1st point:

$\ln(48150) = A_0 + A_1/313.15 + A_2/313.152$

2nd point:

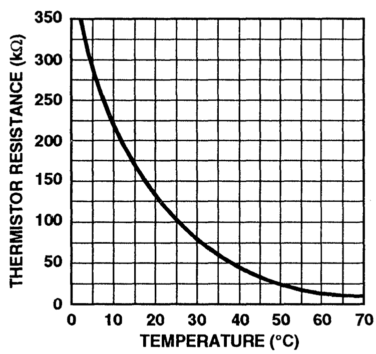
$\ln(100000) = A_0 + A_1/298.15 + A_2/298.152$

3rd point:

$\ln(221800) = A_0 + A_1/283.15 + A_2/283.152$

Solving these three equations for A_0, A_1 and A_2 yields:

$R_T = \ln^{-1}(-5.825 + 5821/T - 194235/T^2)$



SETTING UP THE CONTROL TEMPERATURES

Assume an application which requires that the battery charger not start while the battery temperature is below 20°C (T_{LOW}) or above 30°C (T_{HIGH}). Also assume that the battery should stop charging if it's temperature gets up to either 40°C (T_{MAX}) or 20°C (T_{DELTA}) above an ambient temperature of 15°C (T_{AMB}).

The control temperatures are programmed as a function of the resistance value of the battery temperature thermistor ($R_{BAT}T$) when it is at the temperature to be programmed (T) and the threshold voltage ratio (δV_X).

The form of the equation to determine the values of R_{LOW}, R_{HIGH} and R_{MAX} is as follows:

$$R_X = \frac{R_{BAT}T}{\delta V_X} - R_{BAT}T$$

where $R_{BAT}T$ is the resistance of the battery thermistor at temperature T connected to pin 9.

R_{MAX} (pin 8):

$T_{MAX} = 40°C$, $\delta V_{MAX} = 2/3$, $R_{BAT}40 = 48.1k$,

$$R_{MAX} = \frac{R_{BAT}40}{dV_{MAX}} - R_{BAT}40 = \frac{48.1k}{2/3} - 48.1k = 24k$$

R_{HIGH} (pin 7):

$T_{HIGH} = 30°C$, $\delta V_{HIGH} = 1/2$, $R_{BAT}30 = 77.8k$,

$$R_{HIGH} = \frac{R_{BAT}30}{\delta V_{HIGH}} - R_{BAT}30 = \frac{77.8k}{1/2} - 77.8k = 77.8k$$

R_{LOW} (pin 10):

$T_{LOW} = 20°C$, $\delta V_{LOW} = 1/3$, $R_{BAT}20 = 129.4k$,

$$R_{LOW} = \frac{R_{BAT}20}{\delta V_{LOW}} - R_{BAT}20 = \frac{129.4k}{1/3} - 129.4k = 268.8k$$

R_{DELTA} (PIN 11)

A second thermistor can be used to modify the battery temperature shutdown point as a function of the ambient temperature. A 'delta' temperature may be set up to limit the battery temperature to some value above ambient. This value is called T_{DELTA} and the ambient temperature that it works against is called T_{AMB}.

This control is very important for applications which are required to work over a wide range of ambient temperatures. Once a T_{DELTA} value has been set up to work at some T_{AMB} then the T_{DELTA} will change inversely proportional to T_{AMB}. This means that as the ambient temperature goes up, the trip point goes up at an ever decreasing rate because T_{DELTA} goes down.

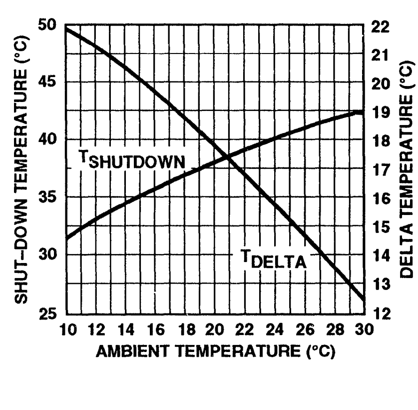
The form of the equation to determine the values of R_{DELTA} is different than the ones for the other temperature control resistors because two thermistors are used. If the same thermistor type is used for monitoring the ambient temperature as is used to monitor the battery temperature then the value of R_{DELTA}, based on the above example, is calculated thus:

$T_{DELTA} = 20°C$, $T_{AMB} = 15°C$,

$T_{BAT} = T_{AMB} + T_{DELTA} = 35°C$, $\delta V_{DELTA} = 1/6$,

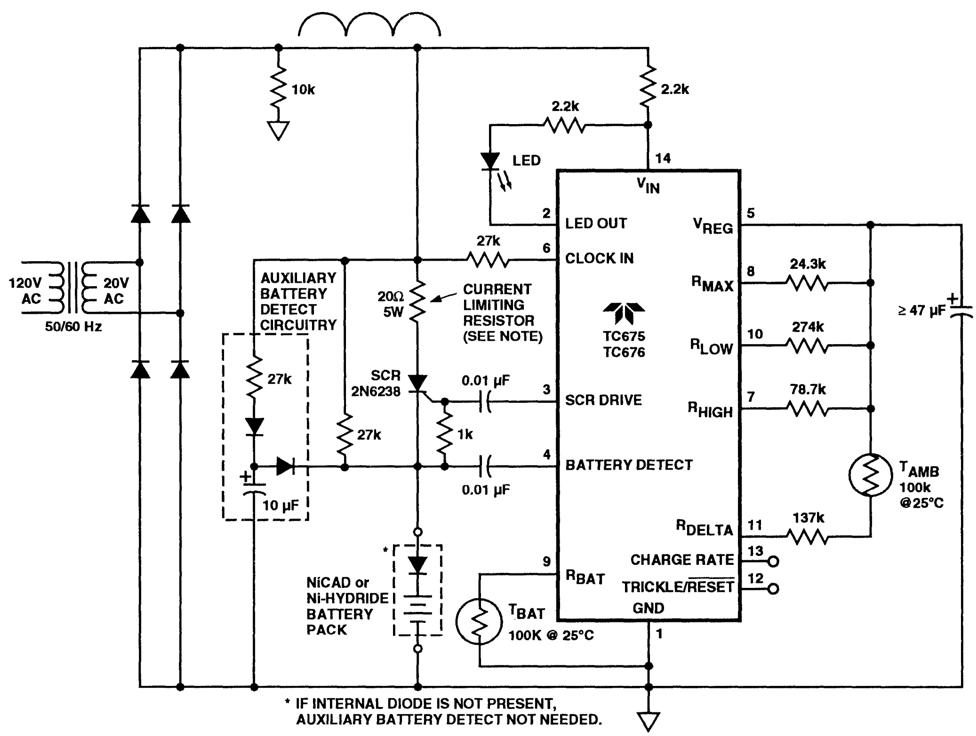
$$R_{DELTA} = \frac{R_{BAT}35}{dV_{DELTA}} - R_{BAT}35 - R_{AMB}15 =$$

$$\frac{61k}{1/6} - 61k - 168.7k = 197.3k$$



FAST NiCAD/Ni-HYDRIDE BATTERY CHARGER

TYPICAL APPLICATION



IMPORTANT NOTE: THE TC675 AND TC676 WILL MONITOR THE CHARGE TIME AND THE BATTERY TEMPERATURE BUT DOES NOT CONTROL THE CHARGING CURRENT. THE DESIGNER MUST LIMIT THE CHARGE CURRENT TO THE BATTERY BASED ON THE APPROPRIATE RATE FOR THE TYPE AND NUMBER OF CELLS IN THE NiCAD/Ni-HYDRIDE BATTERY TO BE CHARGED. EXCEEDING THE BATTERY MANUFACTURER'S MAXIMUM CHARGE CURRENT CAN RESULT IN DEGRADED PERFORMANCE OR EVEN CATASTROPHIC FAILURE.
CHARGING CURRENT CAN BE LIMITED WITH A RESISTOR, AS SHOWN, OR BY MATCHING THE MAXIMUM TRANSFORMER OUTPUT CURRENT TO THE BATTERY CHARGING RATE.

4367 ILL F03

CHARGING NiCAD BATTERIES FROM A DC SOURCE

The TC675 and TC676 are designed to control the charging of NiCad/Ni-Hydride batteries from a self-clocking, self-commutating power source (full-wave rectified, unfiltered 50/60 Hz AC power). Some applications may require that the NiCad be charged from a DC power source, i. e. battery-to-battery.

When a DC power source is used, the application must provide clock pulse to CLOCK IN (pin 6) to control the timing and a pulse train to BATTERY DETECT (pin 4) whenever a battery is NOT present. This pulse train should be modified by the presence of a battery such that it does not provide zero-crossings on pin 6.

A SET/RESET latch may be controlled by the SCR DRIVE output (pin 3) and the timing clock (pin 6) which can then mediate the charge current to the battery.

DC voltage may be supplied directly to the internal circuitry through pin 5. Under these conditions, V_{REG} becomes V_{DD} and must be at least 4 volts and no greater than 6 volts. The internal circuitry will take about 300 µA (1 mA max) and the V_{IN} input (pin 14) should be left open.

NOTES

Section 5

Power Supply Control ICs

5

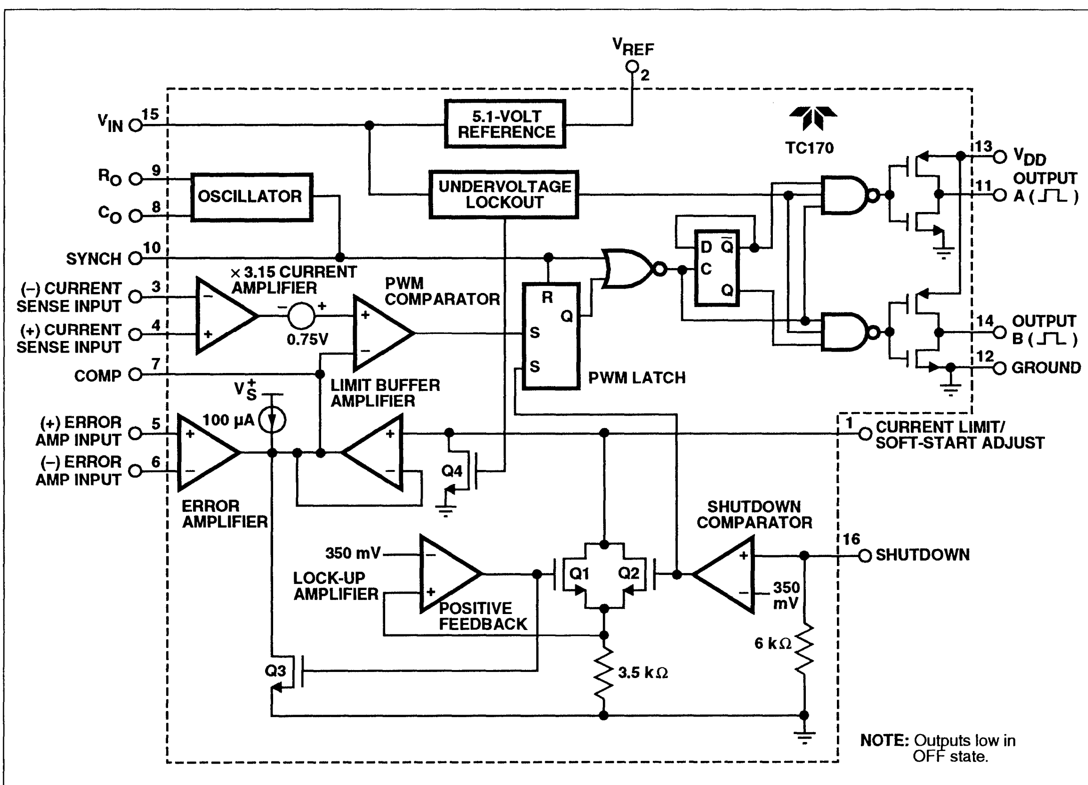
TELEDYNE
COMPONENTS

CMOS CURRENT-MODE PWM CONTROLLER

FEATURES

- Low Supply Current With CMOS Technology ....3.8 mA Max
- Current-Mode Control
- Internal Reference 5.1V
- Fast Rise/Fall Times (C_L = 1000 pF) ....50 ns
- Dual Push-Pull Outputs
- Direct-Power MOSFET Drive
- High Totem-Pole Output Drive ....300 mA
- Differential Current-Sense Amplifier
- Programmable Current Limit
- Soft-Start Operation
- Double-Pulse Suppression
- Undervoltage Lockout
- Wide Supply Voltage Operation ....8V to 16V
- High Frequency Operation..........................200 kHz
- Plastic and CerDIP Packages
- Available with Low OFF State Outputs
- Low Power, Pin-Compatible Replacement for UC3846

BLOCK DIAGRAM



TC170

GENERAL DESCRIPTION

The TC170 brings low-power CMOS technology to the current-mode-switching power supply controller market. Maximum supply current is 3.8 mA. Bipolar current-mode control integrated circuits require five times more operating current. Low power supply current eliminates auxiliary power transformers. In off-line powering schemes, where a simple zener diode circuit provides device supply voltage, power dissipation is greatly reduced. CMOS technology decreases system cost, increases power efficiency, reduces heat generation, and increases total system reliability.

The dual totem-pole CMOS outputs drive power MOSFETs or bipolar transistors. The 50-ns typical output rise and fall times, a 1000-pF capacitive loads, minimize MOSFET power dissipation. Output peak current is 300 mA.

The TC170 contains a full array of system-protection circuits. The undervoltage lockout circuit forces outputs OFF if the supply voltage drops below 7V. A soft-start feature is also available. The soft-start option forces the PWM outputs to initially operate at a minimum duty cycle and low peak output current. The TC170 can be directly turned off through a remote-shutdown control pin. The shutdown mode can be latched (power must be turned off to restart system) or nonlatched. The soft-start feature can also be used in system-shutdown applications. Double-output pulse suppression guarantees output drive pulses always alternate from one output driver to the other. Peak current is user-adjustable.

Current-mode control lets users parallel power supply modules. Two or more TC170 controllers can be slaved together for parallel operation. Circuits can operate from a master TC170 internal oscillator or an external system oscillator.

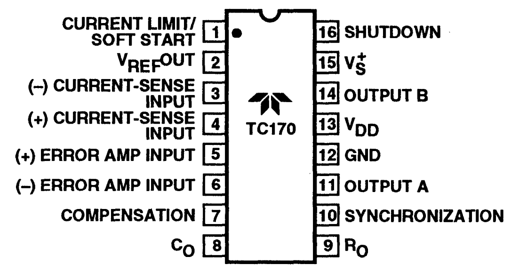
The TC170 operates from an 8V to 16V power supply. An internal 2%, 5.1V reference minimizes external component count. The TC170 is pin compatible with the Unitrode UC1846/2846/3846 bipolar controller.

Other advantages inherent in current-mode control include superior line and load regulation and automatic symmetry correction in push-pull converters.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
TC170CPE	16-Pin Plastic DIP	0°C to +70°C
TC170IJE	16-Pin CerDIP	–25°C to +85°C
TC170MJE	16-Pin CerDIP	–55°C to +125°C
TC170COE	16-Pin SO	0°C to +70°C
TC170EOE	16-Pin SO	–40°C to +85°C
TC170EPE	16-Pin Plastic DIP	0°C to +70°C

PIN CONFIGURATION



NOTE: Outputs low in "OFF" state.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Output Voltage .... V_{DD} or 18V
Analog Inputs .... –0.3V to V_S + 0.3V
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Maximum Chip Temperature .... 150°C
CerDIP Package Thermal Resistance:
- θ_{JA} (Junction to Ambient) .... 105°C/W
- θ_{JC} (Junction to Case) .... 60°C/W

Plastic Package Thermal Resistance:
- θ_{JA} (Junction to Ambient) .... 140°C/W
- θ_{JC} (Junction to Case) .... 70°C/W

Operating Temperature Range
- Commercial .... 0°C to +70°C
- Industrial .... –25°C to +85°C
- Military .... –55°C to +125°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{IN} = 16V, R_O = 24 kΩ, C_O = 1 nF, T_A = 25°C, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Reference Voltage						
V_{REF}	Output Voltage	I_{OUT} = 1 mA	5	5.1	5.3	V
	Line Regulation	V_{IN} = 8V to 16V		5	15	mV
	Load Regulation	I_{OUT} = 1 mA to 10 mA		13	20	mV
V_{RTC}	Temperature Coefficient	Over Operating Temperature Range		0.4	0.5	mV/°C
Oscillator						
	Oscillator Frequency		35	42	46	kHz
	Voltage Stability	V_{IN} = 8V to 16V		1.1	1.5	%/V
	Temperature Stability	Over Operating Temperature Range		5	10	%
Error Amplifier						
V_{OS}	Input Offset Voltage				30	mV
I_B	Input Bias Current				1	nA
V_{CMRR}	Common-Mode Input Voltage	V_{IN} = 8V to 16V	0		V_{DD}–2V	V
A_{VOL}	Open-Loop Voltage Gain	V_{OUT} =1V to 6V	70			dB
BW	Unity Gain Bandwidth			1.2		MHz
CMRR	Common-Mode Rejection Ratio	V_{CMV} 0V to 14V	60			dB
PSRR	Power Supply Rejection Ratio	V_{IN} = 8V to 16V	60			dB
Current Sense Amplifier						
	Amplifier Gain	Pin 3 = 0V to 1.1V	3	3.15	3.3	V/V
	Maximum Differential Input Signal	V_{PIN4} – V_{PIN3}			≤1.1	V
	Common-Mode Input Voltage		0		V_{DD}–3V	V
Current Limit Adjust						
	Current Limit Offset Voltage		0.5		1	V
I_B	Input Bias Current				1	nA
Shutdown Terminal						
V_{TB}	Threshold Voltage		0.3	0.35	0.4	V
V_{IN}	Input Voltage Range		0		V_{DD}	V
	Minimum Latching Current at Pin 1		125			µA
	Maximum Nonlatching Current at Pin 1				50	µA
Output Stage						
V_{DD}	Output Voltage	Pin 13			V_{DD}	V
V_{OL}	Output Low Level	I_{SINK} = 20 mA			0.4	V
V_{OL}	Output Low Level	I_{SINK} = 100 mA			2	V
V_{OH}	Output High Level	I_{SOURCE} = 20 mA	V_{DD}–1V			V
V_{OL}	Output High Level	I_{SOURCE} = 100 mA	V_{DD}–4V			V
t_R	Output Rise Time	C_L = 1000 pF		50	150	ns
t_F	Output Fall Time	C_L = 1000 pF		50	150	ns
Undervoltage Lockout						
	Start-Up	Threshold	7.25	7.7	8.25	V
	Threshold Hysteresis		0.5	0.75	1	V
Supply						
I_S	Standby Supply Current			2.7	3.8	mA

Peak Current Limit Setup

Resistors R1 and R2 at the current limit input (pin 1) set the TC170 peak current limit (Figure 1). The potential at pin 1 is easily calculated:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

R1 should be selected first. The shutdown circuit feature is not latched for $(V_{REF} - 0.35)/R1 < 50\ \mu A$ and is latched for currents greater than 125 μA.

The error amplifier output voltage is clamped from going above V1 through the limit buffer amplifier. Peak current is sensed by RS and amplified by the current amplifier which has a fixed gain of 3.15.

I_{PCL}, the peak current limit, is the current that causes the PWM comparator noninverting input to exceed V1; the potential at the inverting input. Once the comparator trip point is exceeded, both outputs are disabled.

I_{PCL} is easily calculated:

$$I_{PCL} = \frac{V1 - 0.75V}{3.15\ (RS)}$$

where:

$$V1 = V_{REF} \frac{R2}{R1 + R2}$$

V_{REF} = Internal voltage reference = 5.1V

3.15 = Gain of current-sense amplifier

0.75V = Current limit offset

Both driver outputs (pins 11 and 14) are OFF (low) when the peak current limit is exceeded. When the sensed current goes below I_{PCL}, the circuit operates normally.

Output Shutdown

The TC170 outputs can be turned off quickly through the shutdown input (pin 16). A signal greater than 350 mV at pin 16 forces the shutdown comparator output high. The PWM latch is held set, disabling the outputs.

Q2 is also turned on. If $V_{REF}/R1$ is greater than 125 μA, positive feedback through the lock-up amplifier and Q1 keeps the inverting PWM comparator inverting input below 0.75V. Q3 remains on even after the shutdown input signal is removed, because of the positive feedback. The state can be cleared only through a power-up cycle. Outputs will be disabled whenever the potential at pin 1 is below 0.75V.

The shutdown terminal gives a fast, direct way to disable the TC170 output transistors. System protection and remote shutdown applications are possible.

The input pulse to pin 16 should be at least 500 ns wide and have an amplitude of at least 1V in order to get the minimum propagation delay from input to output. If these parameters are met, the delay should be less than 600 ns at 25°C; however, the delay time will increase as the device temperature rises.

Soft Restart From Shutdown

A soft restart can be programmed if nonlatched shutdown operation is used.

A capacitor at pin 1 will cause a gradual increase in potential toward V1. When the voltage at pin 1 reaches 0.75V, the PWM latch set input is removed and the circuit establishes a regulated output voltage. The soft-start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak currents.

Even if a soft start is not required, it is necessary to insert a capacitor between pin 1 and ground if the current I_L is greater than 125 μA. This capacitor will prevent "noise triggering" of the latch, yet minimize the soft-start effect.

Soft-Start Power-Up

During power-up, a capacitor at R1, R2 initiates a soft-start cycle. As the input voltage (pin 15) exceeds the undervoltage lockout potential (7.7V), Q4 is turned off, ending undervoltage lockout. Whenever the PWM comparator inverting input is below 0.5V, both outputs are disabled.

When the undervoltage lockout level is passed, the capacitor begins to charge. The PWM duty cycle increases until the operating output voltage is reached. Soft-start operation forces the PWM output drivers to initially operate with minimum duty cycle and low peak current.

Current-Sense Amplifier

The current-sense amplifier operates at a fixed gain of 3.15. Maximum differential input voltage (V_{PIN4}–V_{PIN3}) is 1.1V. Common-mode input voltage range is 0V to $V_{IN} - 3V$.

Resistive-sensing methods are shown in Figure 2. In Figure 2(A), a simple RC filter limits transient voltage spikes at pin 4, caused by external output transistor-collector capacitance. Transformer coupling (Figure 3) offers isolation and better power efficiency, but cost and complexity increase.

In order to minimize the propagation delay from the input to the current amplifier to the output terminals, the current ramp should be in the order of 1 μs in width (min). Typical time delay values are in the 300 to 400 ns region at 25°C. The delay time increases with device temperature so that at 50°C, the delay times may be increased by as much as 100 ns.

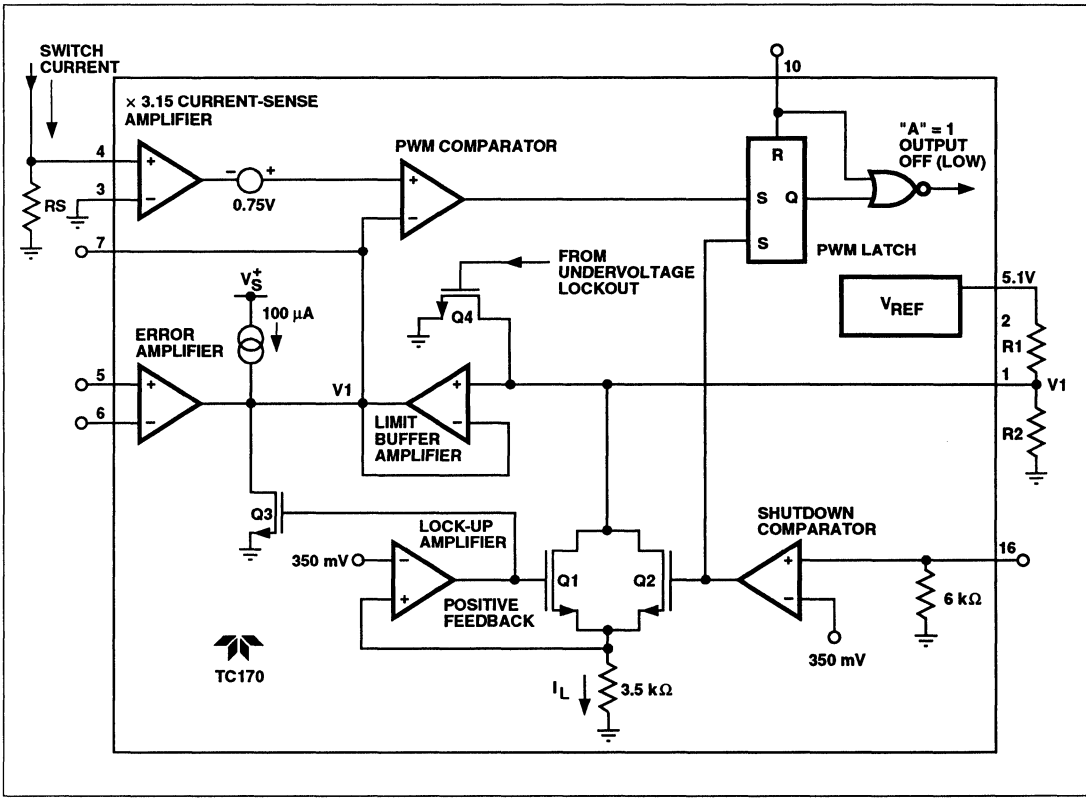


Figure 1 R1 and R2 Set Maximum Peak Output Current

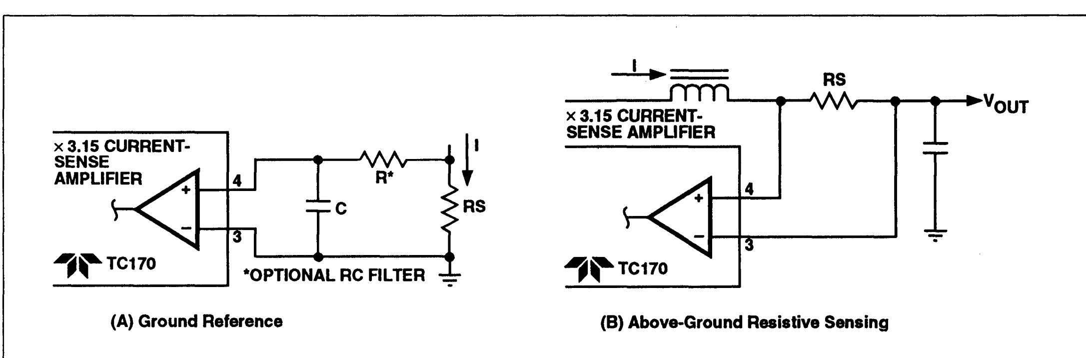


Figure 2 Resistive Sensing

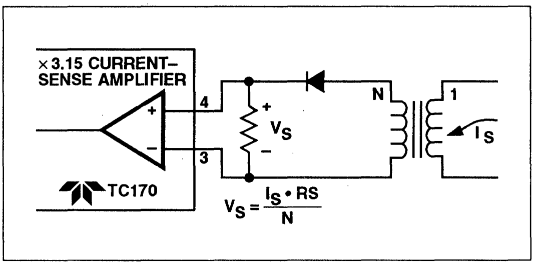


Figure 3 Transformer Isolated Current Sense

Undervoltage Lockout

The undervoltage lockout circuit forces the TC170 outputs OFF (low) if the supply voltage is below 7.7V. Threshold hysteresis is 0.75V and guarantees clean, jitter-free turn-on and turn-off points. The hysteresis also reduces capacitive filtering requirements at the PWM controller supply input (pin 15).

Circuit Synchronization

Current-mode-controlled power supplies can be operated in parallel with a common load. Paralleled converters will equally share the load current. Voltage-mode controllers unequally share the load current, decreasing system reliability.

Two or more TC170 controllers can be slaved together for parallel operation. Circuits can operate from a master TC170 internal oscillator with an external driver (Figure 4). Devices can also be slaved to an external oscillator (Figure 5). Disable internal slave device oscillators by grounding pin 8. Slave controllers derive an oscillator from the bidirectional synchronization output signal at pin 10.

Pin 10 is bidirectional in that it is intended to be both a sync output and input. This is accomplished by making the output driver "weak." This is advantageous in that it eliminates an additional pin from the package but does not enable the device to directly drive another device. In order to make it an effective driver, a buffer is required (Figure 4). In order to use pin 10 as a sync input, it is necessary to overcome the internal driver. This requires a pulse with an amplitude equal to V_{CC}. Since V_{CC} must be above 8.25V for the undervoltage lockout to be disabled, a CMOS or open-collector TTL driver should be used.

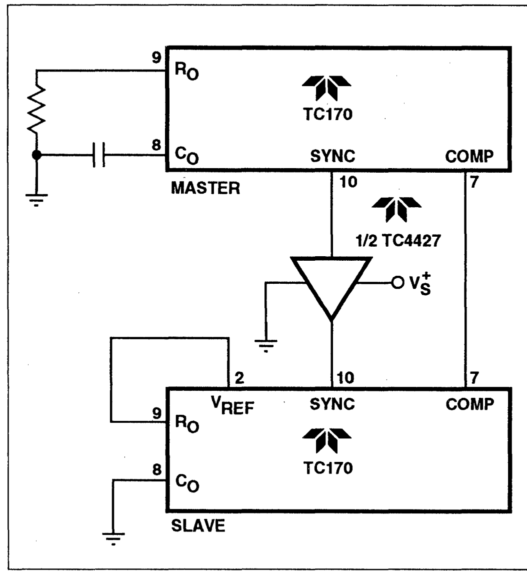


Figure 4 Master/Slave Parallel Operation

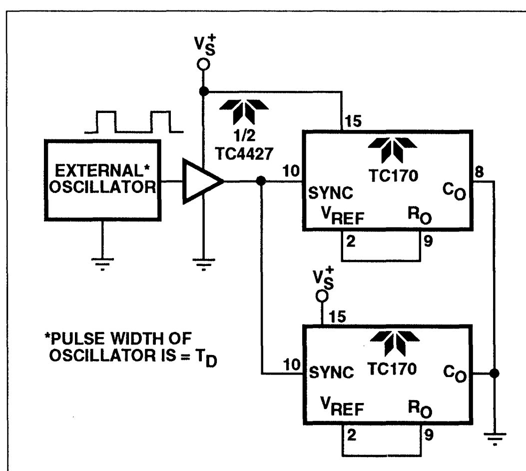


Figure 5 External Clock Synchronization

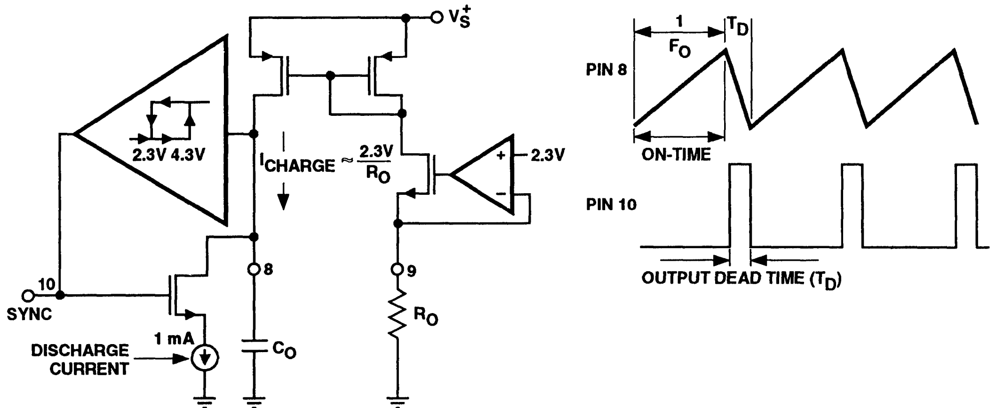


Figure 6 Oscillator Circuit

Oscillator Frequency and Output Dead Time

The oscillator frequency for R_O = 24 kΩ and C_O = 1000 pF is:

$$F_O = \left[\frac{1.27}{R_O C_O} - \frac{2800}{R_O^2 C_O}\right] \frac{C_O}{C_O + 150 \times 10^{-12}}$$

where: R_O = Oscillator Resistor (Ω)
C_O = Oscillator Capacitor (F)
F_O = Oscillator Frequency (Hz)

The oscillator resistor can range from 5 kΩ to 50 kΩ. Oscillator capacitor can range from 250 pF to 1000 pF. Figure 7 shows typical operation for various resistance and capacitance values.

During transitions between the two outputs, simultaneous conduction is prevented. Oscillator fall time controls the output off, or dead time (Figure 6).

Dead time is approximately:

$$T_D = \frac{2000\,[C_O]}{1 - \left(\frac{2.3}{R_O}\right)}$$

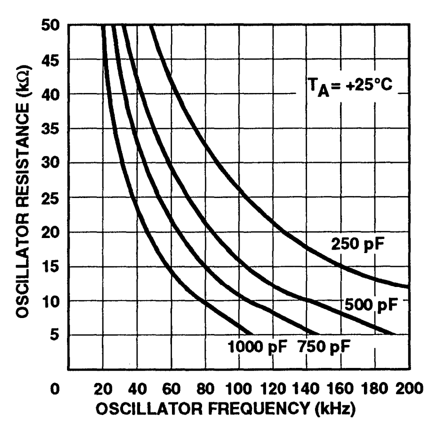
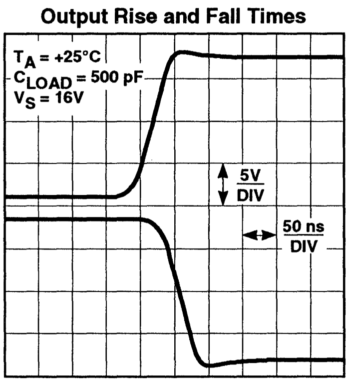


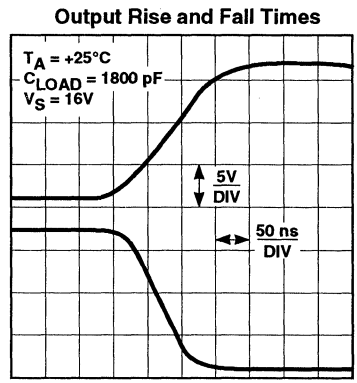
Figure 7 Oscillator Frequency vs Oscillator Resistance

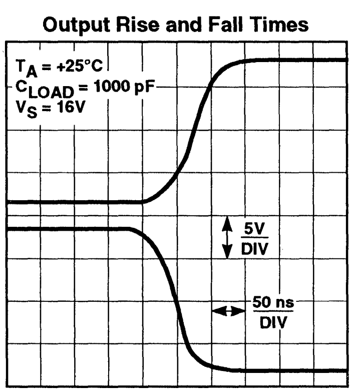
where: R_O = Oscillator Resistor (kΩ)
C_O = Oscillator Capacitor (pF)
T_D = Output Dead Time (sec)

Maximum possible duty cycle is set by the dead time.

TYPICAL CHARACTERISTIC CURVES

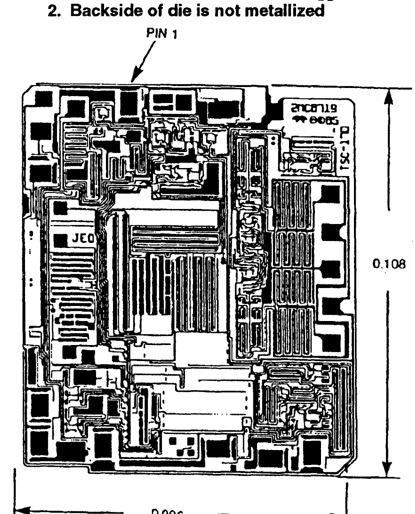






BONDING DIAGRAM

NOTES: 1. Backside of die is common to V_{DD}
2. Backside of die is not metallized



BiCMOS CURRENT-MODE PWM CONTROLLER

FEATURES

- Low Power BiCMOS Construction
- Low Supply Current .... 1.5 mA Typ
- Wide Supply Voltage Operation .... 8V to 18V
- Latch-Up Immunity .... 500 mA on Outputs
- Inputs Will Withstand Neg Inputs to –5V
- High Output Drive .... 1.2A Peak
- Current Mode Control
- Fast Rise/Fall Times .... 60 ns @ 1000 pF
- High Frequency Operation .... 1 MHz
- Clock Ramp Reset Current .... 2.5 mA ±10%
- Adjustable UV Lockout
- Adjustable UV Hysteresis
- Shutdown Pin Available
- UV Lockout Pin Available .... 30V Open Collector
- Duty Cycle Limited to 99%
- Soft-Start Duty Cycle Limit 49%
- Low Propagation Delay Current Amp to Output .... 140 ns Typ
- Low Propagation Delay Shutdown to Output .... 90 ns Typ
- 2kV ESD Protection

GENERAL DESCRIPTION

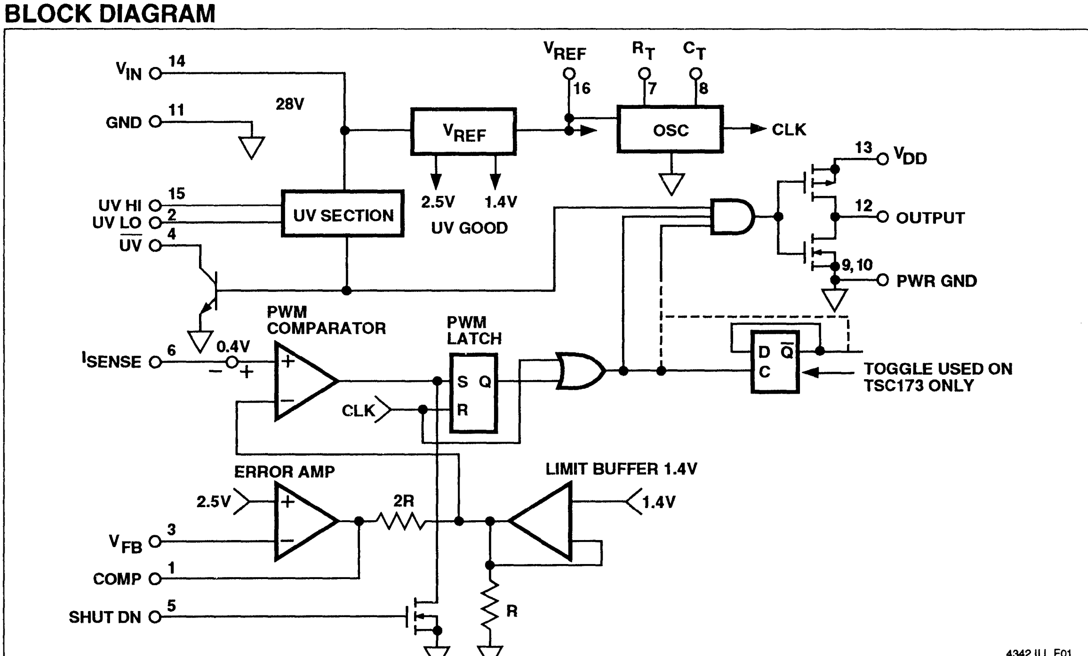
The TC172/173 are current-mode BiCMOS PWM control ICs. With a low 1.5 mA supply current along with the high drive currents (1.2A typical), they provide a low-cost solution for many PWM needs, since they can be driven without a 50–60 Hz transformer and can directly drive MOSFETs up to Hex 3 size.

The TC172/173 are based on the popular UC3842-type architecture, but are improved to bring out more control features to operate at higher frequency (1 MHz) and provide more output drive power.

The TC172/173 add additional features. They come in a 16-pin package. The additional pins allow more functions: a linear timing ramp for the clock (instead of exponential), user-adjustable undervoltage start and hysteresis level, as well as separate output drive and control grounds. In addition, the TC172/173 provides a separate shutdown pin for fast output shutdown, and an open-collector output pin that pulls low when the user-adjusted undervoltage lockout drops out.

5

BLOCK DIAGRAM



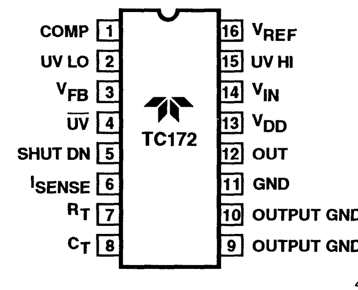
TC172
TC173

ORDERING INFORMATION

Part No.	Package	Temperature
TC17*MJE	16-Pin CerDIP	–55°C to +125°C
TC17*EOE	16-Pin SOIC Wide	–40°C to +85°C
TC17*EPE	16-Pin Plastic DIP	–40°C to +85°C
TC17*EJE	16-Pin CerDIP	–40°C to +85°C
TC17*COE	16-Pin SOIC Wide	0°C to +70°C
TC17*CPA	16-Pin Plastic DIP	0°C to +70°C

* The last digit defines the specific device:
172 — 99% duty cycle limit
173 — 49% duty cycle limit

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for:

–55°C ≤ T_A ≤ 125°C for TC172/173MXX
–40°C ≤ T_A ≤ 85°C for TC172/173EXX
0°C ≤ T_A ≤ 70°C for TC172/173CXX
V_{CC} = 15V (Note 4); R_T = 10 kΩ; C_T = 330 pF

		TC172/173MXX TC172/173EXX			TC172/173CXX			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Reference Section								
Output Voltage	T_J = 25°C, I_O = 1 mA	4.95	5	5.05	4.9	5	5.10	V
Line Regulation	12 ≤ V_{IN} ≤ 18V, I_O = 5 µA		±3	±10		±3	±10	mV
Load Regulation	1 mA ≤ I_O ≤ 11 mA		±5	±15		±5	±15	mV
Temperature Coefficient	(Note 1)		±0.25	±0.5		±0.25	±0.5	mV/°C
Total Output Variation	Line, Load, Temperature (Note 1)	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_A = 25°C (Note 1)		100			100		µV
Long-Term Stability	T_A = 125°C, 1000 Hrs. (Note 1)		±0.5			±0.5		%
Output Short Circuit		–20	–50	–100	–30	–50	–100	mA
Oscillator Section								
Initial Accuracy	T_J = 25°C (Note 5)	490	520	560	490	520	560	kHz
Voltage Coefficient	12 ≤ V_{CC} ≤ 18V		0.2	0.3		0.2	0.3	%/V
Temperature Coefficient	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 1)		2	3		2	3	%/°C
Amplitude	V_{PIN4} Peak-to-Peak	2.45	2.26	2.85	2.45	2.65	2.85	V
Maximum Frequency		1			1			MHz
Error Amp Section								
Input Offset Voltage	V_{PIN1} = 2.5V		±15	±50		±15	±50	mV
Input Bias Current			0.3	2		0.3	2	N/A
A_{VOL}	2 ≤ V_O ≤ 4V	70	90		70	90		dB
Unity Gain Bandwidth	(Note 1)	650	750		650	750		MHz
PSRR	12 ≤ V_{CC} ≤ 18V	80	100		80	100		dB

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Test Conditions	TC172/173MXX TC172/173EXX Min	Typ	Max	TC172/173CXX Min	Typ	Max	Units
Error Amp Section (Cont.)								
Output Sink Current	V_{PIN2} = 2.7V, V_{PIN1} = 1.1V	1.2	1.5		1.5	1.7		mA
Output Source Current	V_{PIN2} = 2.3V, V_{PIN1} = 5V	3	3.4		3.4	4.2		mA
V_{OUT} High	V_{PIN2} = 2.3V, R_L = 10K to Ground	5.8	6	6.5	5.8	6.0	6.5	V
V_{OUT} Low	V_{PIN2} = 2.7V, R_L = 10K to Pin 8	0.1	0.7	1.1	0.1	0.7	1.1	V
Rise/Fall Response Time	(Note 1)		5	7		5	7	μs
Current Sense Section								
Gain Ratio	(Notes 2 and 3)	2.8	2.9	3.1	2.8	2.9	3.1	V/V
Maximum Input Signal	V_{PIN1} = 5V (Note 2)	0.85	0.95	1.05	0.85	0.95	1.05	V
PSRR	$12 \leq V_{CC} \leq 18V$ (Note 2)	70	80		70	80		dB
Input Bias Current			±0.3	±2		±0.3	±2	N/A
Delay to Output			140	100		140	100	ns
Output Section								
RDSON	I_{SINK} = 20 mA		7	15		7	15	Ω
RDSON	I_{SOURCE} = 20 mA		11	20		11	15	Ω
Rise Time	C_L = 1 nF (Note 1)		40	60		35	60	ns
Fall Time	C_L = 1 nF (Note 1)		30	40		30	40	ns
Cross Conduction	C_L = 0 nF		6.5			6.5		nc
V_{DD} Maximum	Pin 12 (Note 1)			18			18	V
Peak Output Current	10,000 pF Load	1.1	1.2	1.5	1.1	1.2	1.5	A
Undervoltage Lockout Section								
Start Threshold	User Defined	8		18	8		18	V
Undervoltage Threshold	User Defined	8		18	8		18	V
Undervoltage Indicator								
Pulldown Voltage				100			100	mV
Shutdown Section								
Minimum Shutdown Pulse Width				100			100	ns
Shutdown Delay				100			100	ns
Shutdown Threshold			1.5			1.5		V
PWM Section								
Maximum Duty Cycle	172	95	97	100	95	97	100	%
	173	46	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current		50	170	300	50	170	300	μA
Operating Supply Current	$V_{PIN2} = V_{PIN3}$ = 0V		1	2		1	1.5	mA

NOTES:
1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with $V_{PIN2} = 0$
3. Gain defined as:

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}};\ 0 \leq V_{PIN3} \leq 0.8V$$

4. Adjust V_{CC} above the start threshold before setting at 15V.
5. Output frequency equals oscillator frequency for the TC172. Output frequency is one-half oscillator frequency for the TC173.

NOTES

TELEDYNE COMPONENTS

TC15C25 TC25C25 TC35C25 TC15C27 TC25C27 TC35C27

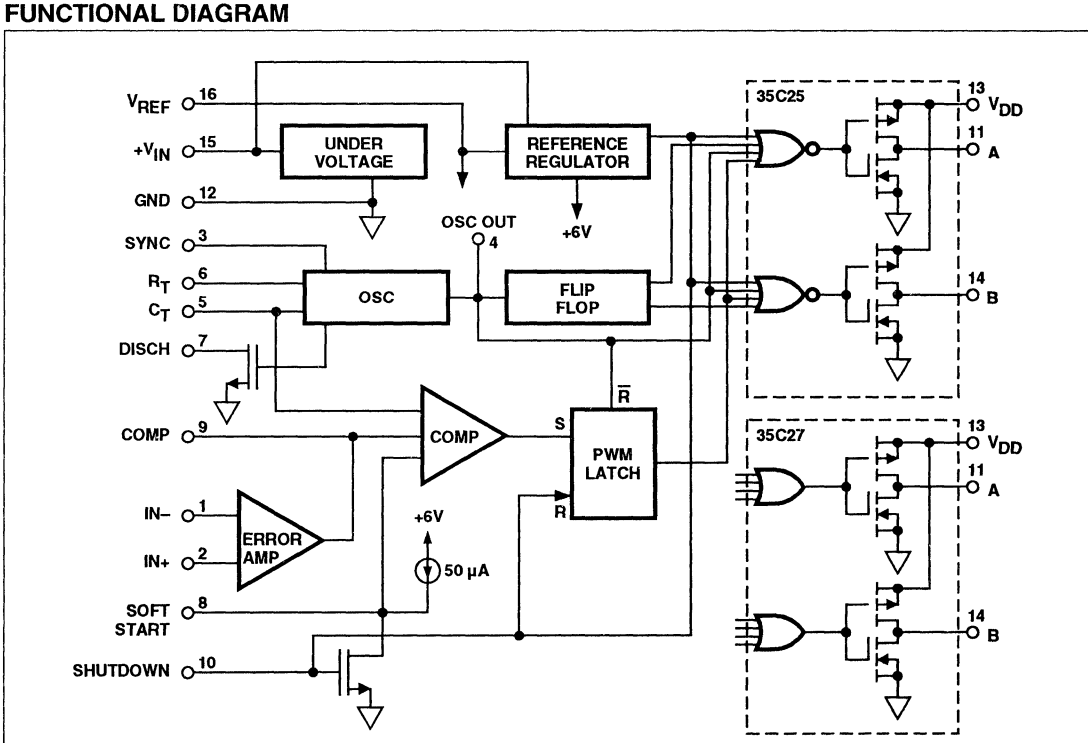
BiCMOS PWM CONTROLLERS

FEATURES

- Low Power BiCMOS Construction
- Low Supply Current .... 1.0 mA Typ
- Latch Up Immunity .... > 500 mA on Outputs
- Below Rail Input Protection .... –5V
- High Output Drive .... 500 mA Peak
- Fast Rise/Fall Time .... 50 ns @ 1000 pF
- High Frequency Operation .... Up To 1 MHz
- Tri-state Sync Pin For Easy Parallel Operation
- Undervoltage Hysterisis Guaranteed
- Shutdown Pin Available
- Double Ended
- Soft Start, With Small Cap
- Low Prop Delay Shutdown to Output .... 140 ns Typ

5

FUNCTIONAL DIAGRAM



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TC15C25 TC15C27
TC25C25 TC25C27
TC35C25 TC35C27

GENERAL DESCRIPTION

The TC35C25 and TC35C27 family of PWM controllers are CMOS implementations of the industry standard 3525 and 3527 voltage mode SMPS ICs.

These second generation CMOS devices employ Teledyne Components' Tough BiCMOS™ process for latch-up proof operation. They offer much lower power consumption than any of their previous CMOS or bipolar counterparts.

These controllers have separate supply pins for the control and output sections of the circuit. This allows 'bootstrap' operation. The CMOS output stage allows the output voltage to swing to within 25 mV of either rail.

Other improved features include tighter hysteresis and undervoltage start-up specifications over temperature, and very low input bias current on all inputs.

OUTPUT SECTION

The output stage of the TC35C25/27 is comprised of two pairs of complimentary CMOS drivers operating in a push-pull mode. Each output is capable of sinking or sourcing nearly 500 mA of peak current. They are also capable of absorbing just as much 'kick-back' current without latching.

SOFT START

A soft restart recovery rate may be selected by placing a capacitor from SOFT START (pin 8) to ground. The calculation for the recovery timing is approximately 60 ms/μF.

SOFT START will mediate the start-up from undervoltage recovery, power-on or SHUTDOWN.

SHUTDOWN

There is a minimum delay, non-latching shutdown feature on the TC35C25/27 PWM controller. Both outputs may be turned off by applying a positive voltage to SHUTDOWN (pin 10). Returning the pin back to ground will reinitialize the soft start cycle.

OSCILLATOR SECTION

A tri-state feature has been added to accommodate systems which require multiple controllers to be run in a 'master/slave' configuration. The timing resistor pin (R_T, pin 6) may be tied to V_{REF} to place the sync pin (SYNC, pin 3) in a high impedance state. This will allow the chip to be clocked from an external source.

The sync output (OSC OUT, pin 4) of the TC35C25 can drive several sync inputs configured in this manner.

REPLACING BIPOLAR VERSIONS WITH CMOS

Although the pin-out and functions are the same for both the Bipolar and CMOS versions, there are several differences that need to be taken into account. The reference voltage on the TC35C25/27 is 4V instead of 5V and the oscillator ramp is 3V, not 4V. The R_T and C_T values are different for any particular frequency and dead-time requirement.

The most important difference is that the absolute maximum rating of the V_{DD} and V_{IN} voltages for the TC35C25/27 is 18V, whereas the UC3525/27 is 40V.

ORDERING INFORMATION

Part No.	Configuration	Pkg./Temperature
TC15C25MJE	Non-Inverting	16-Pin CerDIP –55 to +125°C
TC15C27MJE	Inverting	16-Pin CerDIP –55 to +125°C
TC25C25EOE	Non-Inverting	16-Pin SOIC (wide) –40 to +85°C
TC25C25EPE	Non-Inverting	16-Pin Plastic DIP –40 to +85°C
TC25C27EOE	Non-Inverting	16-Pin SOIC (wide) –40 to +85°C
TC25C27EPE	Inverting	16-Pin Plastic DIP –40 to +85°C
TC35C25COE	Non-Inverting	16-Pin SOIC (wide) 0 to +70°C
TC35C25CPE	Non-Inverting	16-Pin Plastic DIP 0 to +70°C
TC35C27COE	Inverting	16-Pin SOIC (wide) 0 to +70°C
TC35C27CPE	Inverting	16-Pin Plastic DIP 0 to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Maximum Chip Temperature .... 150°C
Storage Temperature .... –65°C to +150°C
Lead Temperature (10 sec) .... 300°C
Package Thermal Resistance
- CerDip $R_{\theta J\text{-}A}$ .... 150°C/W
- CerDip $R_{\theta J\text{-}C}$ .... 55°C/W
- PDIP $R_{\theta J\text{-}A}$ .... 125°C/W
- PDIP $R_{\theta J\text{-}C}$ .... 45°C/W
- SOIC $R_{\theta J\text{-}A}$ .... 250°C/W
- SOIC $R_{\theta J\text{-}C}$ .... 75°C/W

Operating Temperature
- 15C2X .... –55C° ≤ T_A ≤ +125°C
- 25C2X .... –40C° ≤ T_A ≤ +85°C
- 35C2X .... 0C° ≤ T_A ≤ +70°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS: unless otherwise specified $V_{IN} = V_{DD} = 16V$, $T_A = 25°C$, $R_T = 3.7\ k\Omega$, $R_D = 760\Omega$, $C_T = 1000\ pF$; (See test circuit).

Parameter	Conditions	Min	Typ	Max	Units
Reference Section					
Output Voltage	$I_O = 1$ mA	3.95	4	4.05	V
Line Regulation	V_{IN} = 8 to 18V, (note 2)	—	±4	±10	mV
Load Regulation	I_I = 1 to 12 mA, (note 2)	—	±4	±15	mV
Temperature Coefficient	(notes 1, 2)	—	±0.01	±0.4	mV/°C
V_{REF}	Worst Case, (note 2)	3.85	4	4.15	V
Long Term Drift	(note 1)	—	±50	—	mV/1000 Hrs
Short Circuit Current	V_{REF} to GND (note 2)	20	40	70	mA
Output Noise	10 Hz ≤ f ≥ 10 kHz, (note 1)	—	21		μVRMS
Oscillator					
Initial Accuracy	@ 97 kHz	—	±2	±3	%
Voltage Coefficient	V_{IN} = 8 to 18V, (note 2)	—	±0.01	±0.1	%/V
Temperature Coefficient	(notes 1, 2)	—	±0.025	±0.06	%/°C
Osc Ramp Amplitude	(note 2)	2.9	3.2	3.4	V
Reset Switch $R_{DS\ (ON)}$		35	50	60	Ω
Clock Amplitude	f_{OSC} = 100 kHz, R_L = 1MΩ, (notes 1, 2)	4.9	5.5	6.7	V
Clock Min Width	R_D = 0Ω, (note 1) C_T = 100 pF, R_T = 1Ω	—	170	200	ns
Sync Threshold	R_T pin tied to V_{REF}, C_T pin at GND, (note 2)	1.8	2.2	2.8	V
Sync Input Current	Sync Voltage = 4V, V(R_T) = 4V (note 2	—	—	±1	μA
Min Sync Pulse Width	Sync Amplitude = 5V, (note 1)	—	130	175	ns
Max Osc Freq	R_T = 1 kΩ, C_T = 100 pF, R_D = 0Ω, (note 1)	1.0	—	—	MHz
Error Amplifier (V_{CM} = 2.5V)					
Input Offset Voltage	(note 2)	—	±5	±15	mV
Input Bias Current		—	±50	±200	pA
Input Offset Current		—	±25	±100	pA
DC Open Loop Gain	R_L = 100 kΩ, (note 2)	70	85	—	dB
Gain Bandwidth Product	(note 1, 2)	0.7	0.9	1.2	MHz
Output Low Level	R_L = 100 kΩ (N Channel), (note 2)	—	10	20	mV
Output High Level	R_L = 100 kΩ (NPN), (note 2)	4.9	5.4	5.9	V
CMRR	V_{CM} = 0.5 to 4.7V, (note 2)	60	75	—	dB

TC15C25 TC15C27
TC25C25 TC25C27
TC35C25 TC35C27

ELECTRICAL CHARACTERISTICS (Cont): unless otherwise specified $V_{IN} = V_{DD} = 16V$, $T_A = 25°C$, $R_T = 3.7\ k\Omega$, $R_D = 760\Omega$, $C_T = 1000\ pF$; (See test circuit).

Parameter	Conditions	Min	Typ	Max	Units
Error Amplifier (V_{CM} = 2.5V) (Cont.)					
Supply Voltage Rejection	V_{IN} = 8 to 18V, (note 2)	90	120	—	dB
Slew Rate	C_{LOAD} = 50 pF, A_{CL} = 1 V(EA+) = 1V to 3V Pulse, (notes 1,2)	—	1	—	V/µs
PWM Comparator					
Min Duty Cycle	(note 1)	—	—	0	%
Max Duty Cycle	f_{OSC} = 100 kHz, (note 1)	45	49	—	%
Input Threshold	$V(C_T)$ = 0.6V, (note 2)	0.5	0.6	0.7	V
Input Threshold	$V(C_T)$ = 3.6V, (note 2)	3.4	3.6	3.7	V
Input Bias Current	(note 1)	—	—	±1	µA
Soft Start Section					
Soft Start Current	$V_{SHUTDOWN}$ = 0V, (note 2)	30	46	75	µA
Soft Start Voltage	$V_{SHUTDOWN}$ = 3V, (note 2)	—	30	100	mV
Shutdown Input Current	$V_{SHUTDOWN}$ = 3V, (note 2)	—	±1	±100	nA
Min Shutdown Pulse Width	$V_{SHUTDOWN}$ = 5V Pulse, (notes 1, 2)	—	20	40	ns
Shutdown Delay	$V_{SHUTDOWN}$ = 5V Pulse, (notes 1, 2)	130	140	220	ns
Shutdown Threshold		1.5	2.4	3	V
Output Drivers (each output) (note 2)					
Output Low Level $R_{DS\,(ON)}$	I_{SINK} = 20 mA (note 2)	—	13	25	Ω
Output High Level $R_{DS\,(ON)}$	I_{SOURCE} = 20 mA (note 2)	—	20	35	Ω
Rise Time	C_L = 1 nF, (notes 1, 2)	—	55	80	ns
Fall Time	C_L = 1 nF, (notes 1, 2)	—	40	65	ns
Power Supply					
Supply Current	f_{OSC} = 100 kHz (See Test Circuit)	—	1	1.6	mA
UV Lockout Threshold	(note 2)	6.6	7	7.3	V
UV Lockout Hysteresis	(note 2)	1.7	2.2	2.5	V
Start-Up Current	(note 2)	—	75	200	µA

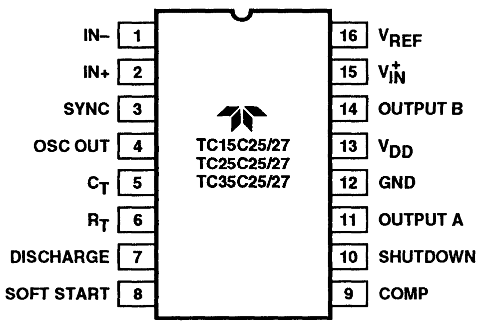
NOTES: 1. Not tested.
2. Guaranteed over operating temperature range.

BiCMOS PWM CONTROLLERS

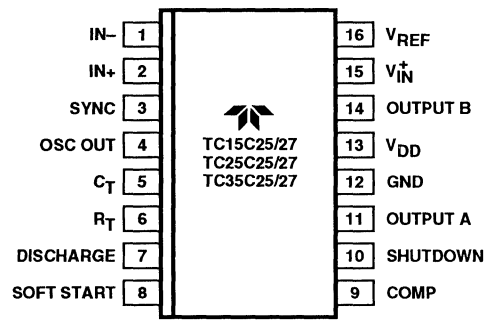
TC15C25 TC25C25 TC35C25 TC15C27 TC25C27 TC35C27

PIN CONFIGURATIONS

16-Pin DIP

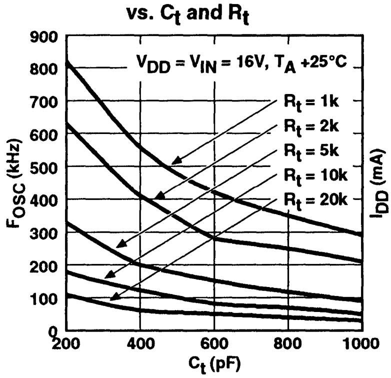


16-Pin SOIC

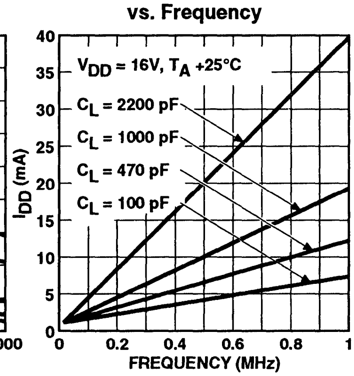


TYPICAL CHARACTERISTIC CURVES

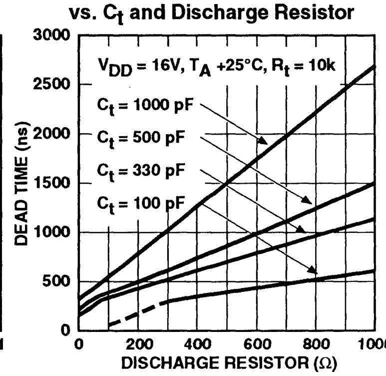
Oscillator Frequency vs. C_t and R_t



Supply Current vs. Frequency



Dead Time vs. C_t and Discharge Resistor



NOTES

TELEDYNE COMPONENTS

TC18C42/3/4/5
TC28C42/3/4/5
TC38C42/3/4/5

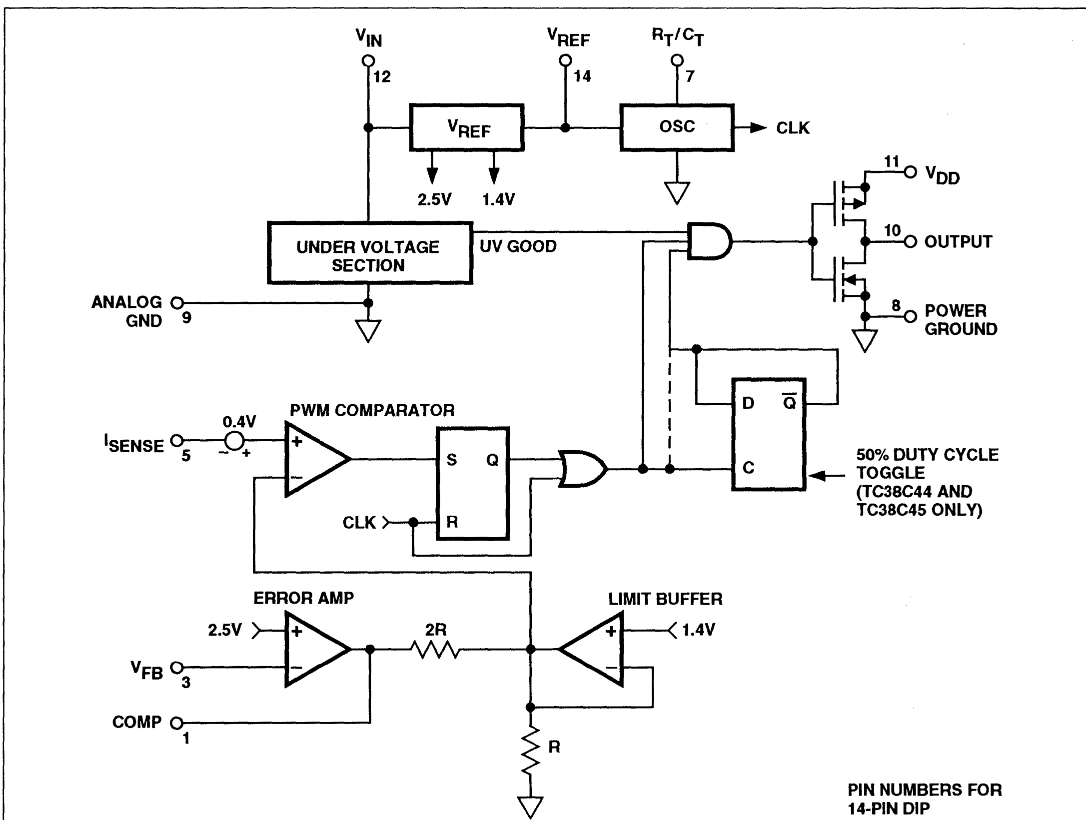
BiCMOS CURRENT MODE PWM CONTROLLER

FEATURES

- Low Power BiCMOS Design
- Tough CMOS™ Construction
- Low Supply Current .... 1.0 mA Typ @ 100 kHz
- Wide Supply Voltage Operation .... 8V to 18V
- Latch-Up Immunity .... 500 mA on Outputs
- Input Will Withstand Negative Inputs to –5 Volts
- High Output Drive .... 0.7A Peak (1.2A on 14 and 16-Pin Versions)
- 2 kV ESD Protection
- Current Mode Control
- Fast Rise/Fall Time (Max) .... 60 ns @ 1000 pf
- High Frequency Operation .... 300 kHz
- Clock Ramp Reset Current .... 2.5 mA ±10%
- Low Propagation Delay Current Amp to Output .... 140 ns Typ
- Pin Compatible with UC3842/3843/3844/3845

5

BLOCK DIAGRAM



BiCMOS CURRENT MODE PWM CONTROLLER

TC18C42/3/4/5
TC28C42/3/4/5
TC38C42/3/4/5

GENERAL DESCRIPTION

The TC38C42/3/4/5 are current mode BiCMOS PWM control ICs. With a low 1.0 mA supply current along with the high drive currents (0.7A peak) they provide a low cost solution for a PWM that operates to 300 kHz and directly drives MOSFETs up to HEX 3 size.

Performance of the oscillator and current sense amplifier have been greatly improved over previous bipolar versions. Voltage and temperature stability have been improved by a factor of 3. Noise immunity (PSRR) has also been improved. These improvements make for a more reliable power system.

Tough CMOS™ design and construction provide input and output latch protection, outstanding ESD tolerance, and high reliability manufacturing techniques and materials. Tough CMOS™ means high reliability.

The TC38C42/3/4/5 are pin compatible with earlier bipolar versions so that designers can easily update older designs. Improvements have been added though. For example, clock ramp reset current is specified at 2.5 mA (±10%) for accurate deadtime control. A few component values must be changed (R_T & C_T) to use TC38C42 family in existing bipolar designs.

The 14-pin DIP and 16-pin SO versions have separate and internally isolated grounds, and are rated for higher output current (1.2A). These separate grounds allow for 'bootstrap' operation of the PWM to further improve efficiency.

REFERENCE SECTION

The reference is a zener based design with a buffer amplifier to drive the output. It is unstable with capacitances between 0.01 µF and 3.3 µF. In a normal application a 4.7 µF is used. In some lower noise layouts the capacitor can be eliminated entirely.

The reference is active as soon as the 38C4X has power supplied. This is different than its bipolar counterparts, in that the bipolar reference comes on only after the IC has come out of its under voltage mode. Thus, on the 38C4X, the reference pin can not be used as a reset function such as on a soft start circuit.

OSCILLATOR SECTION

The oscillator frequency is set by the combination of a resistor from the reference to the R_T/C_T pin and by a capacitor from this pin to ground. The oscillator is designed to have ramp amplitude from 0.15 to 2.5 volts. This is approximate, as over shoot on the oscillator comparator causes the ramp amplitude to increase with frequency due to comparator delay. Minimum values for C_T and R_T are 33 pF and 1 kΩ respectively. Maximum values are dependent on leakage currents in the capacitor, not on the input currents to the R_T/C_T pin.

Frequency of Operation

The frequency of oscillation for the TC38C4X family is controlled by a resistor to V_{REF} (R_T) and a capacitor to ground (C_T). V_{REF} supplies current through the resistor and charges the capacitor until its voltage reaches the threshold of the upper comparator (≈2.5V). A 2.5 mA current is then applied to the capacitor to discharge it to near ground (≈0.15V). The discharge current is then shut off and the cycle repeats. An approximate equation for the frequency of operation is:

$$f_O \approx \frac{1}{R_T C_T} \quad (R_T \text{ in Ohms and } C_T \text{ in Farads})$$

The value of R_T affects the discharge current and the upper and lower comparators each have delay. As R_T gets smaller and as the frequency of operation gets higher, the above equation falls apart. Figure 5 illustrates this effect.

Dead Time

The value of R_T has a effect on the discharge rate but the primary consideration is the value of C_T. The time required to discharge the capacitor is approximately 1000 C_T.

ORDERING INFORMATION

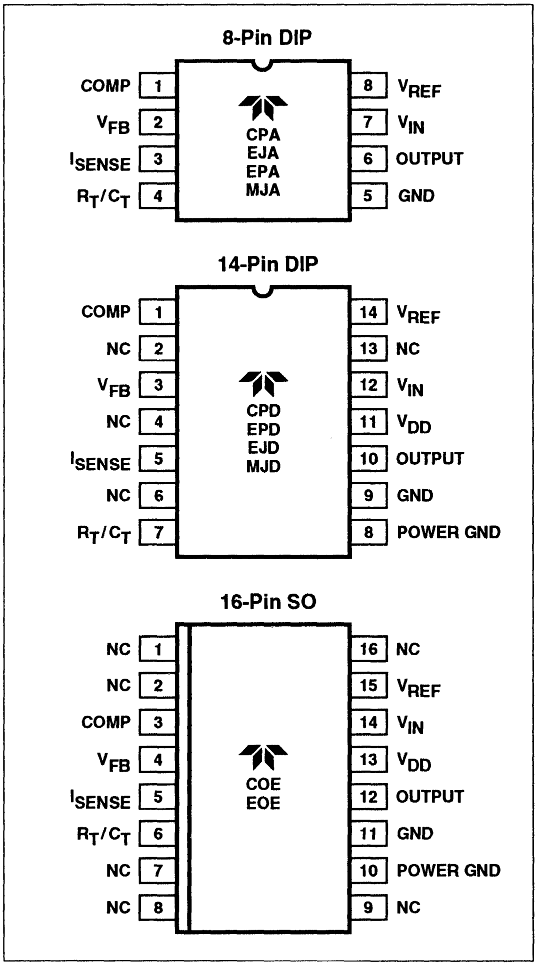
Part No.	Package	Temperature
TC18C**MJA	8-pin CerDIP	–55°C to +125°C
TC18C**MJD	14-pin CerDIP	–55°C to +125°C
TC28C**EJA	8-pin CerDIP	–40°C to +85°C
TC28C**EJD	14-pin CerDIP	–40°C to +85°C
TC28C**EOE	16-pin SOIC Wide	–40°C to +85°C
TC28C**EPA	8-pin Plastic DIP	–40°C to +85°C
TC28C**EPD	14-pin Plastic	–40°C to +85°C
TC38C**COE	16-pin SOIC Wide	0°C to +70°C
TC38C**CPA	8-pin Plastic DIP	0°C to +70°C
TC38C**CPD	14-pinPlastic	0°C to +70°C

	Duty Cycle Limitation	
Start-up Voltage	**99%**	**49%**
14.5 V	X8C42	X8C44
8.4 V	X8C43	X8C45

BiCMOS CURRENT MODE PWM CONTROLLER

TC18C42/3/4/5
TC28C42/3/4/5
TC38C42/3/4/5

PIN CONFIGURATIONS

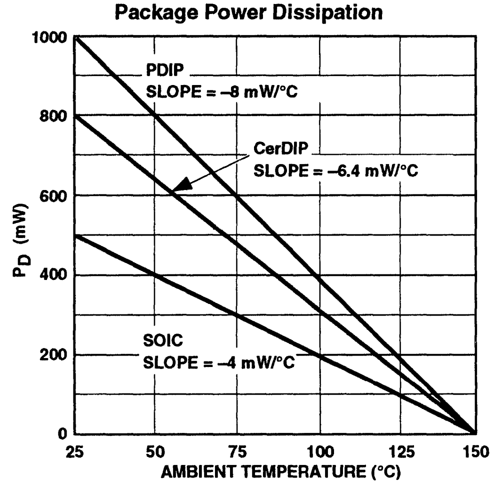


ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Maximum Chip Temperature	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (10 sec)	+300°C
Package Thermal Resistance	
CerDip $R_{\theta J\text{-}A}$	150°C/W
CerDip $R_{\theta J\text{-}C}$	55°C/W
PDIP $R_{\theta J\text{-}A}$	125°C/W
PDIP $R_{\theta J\text{-}C}$	45°C/W
SOIC $R_{\theta J\text{-}A}$	250°C/W
SOIC $R_{\theta J\text{-}C}$	75°C/W
Operating Temperature	
18C4X	–55C° ≤ T_A ≤ +125°C
28C4X	–40C° ≤ T_A ≤ +85°C
38C4X	0C° ≤ T_A ≤ +70°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Package Power Dissipation



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ELECTRICAL CHARACTERISTICS: unless otherwise stated, these specifications apply over specified temperature range. $V_{IN} = V_{DD} = 15V$; $R_T = 71\ k\Omega$; $C_T = 150\ pF$

		TC18C4X TC28C4X			TC38C4X			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Reference Section								
Output Voltage	$T_A = 25°C$, $I_O = 1$ mA	4.95	5	5.05	4.90	5	5.10	V
Line Regulation	$9.5V \le V_{IN} \le 15V$, $I_O = 1$ mA	—	±3	±10	—	±3	±10	mV
Load Regulation	$1mA \le I_O \le 11$ mA	—	±5	±15	—	±3	±10	mV
Temp Stability	(note 1)	—	±0.25	±0.5	—	±0.25	±0.5	mV/°C
Output Noise Voltage	$10\ Hz \le f \le 10\ kHz$, $T_A = 25°C$ (note 1)	—	100	—	—	100	—	µV(rms)
Long Term Stability	$T_A = 125°C$, 1000 Hrs. (note 1)	—	±0.5	—	—	±0.5	—	%
Output Short Circuit		-20	-50	-100	-30	-50	-100	mA
Oscillator Section								
Initial Accuracy	$T_A = 25°C$ (note 4)	95	100	105	95	100	105	kHz
Voltage Stability	$9.5V \le V_{IN} \le 15V$	—	±0.2	±0.3	—	±0.2	±0.3	%
Temp Stability	$T_{MIN} \le T_A \le T_{MAX}$ (note 1); Figure 2	—	±0.01	±0.05	—	±0.01	±0.03	%/°C
Clock Ramp Reset	R_T/C_T pin at 4V	2.25	2.5	2.75	2.25	2.5	2.75	mA
Amplitude	R_T/C_T pin peak to peak	2.45	2.65	2.85	2.45	2.65	2.85	V
Maximum Freq	(note 1)	300	—	—	300	—	—	kHz
Error Amp Section								
Input Offset Voltage	$V_{(COMP)} = 2.5V$	—	±15	±50	—	±15	±50	mV
Input Bias Current	(note 1)	—	±0.3	±2	—	±0.3	±2	nA
A_{VOL}	$2V \le V_O \le 4V$	70	90	—	70	90	—	dB
Gain Bandwidth Product	(note 1)	650	750	—	650	750	—	kHz
PSRR	$9.5V \le V_{IN} \le 15V$	80	100	—	80	100	—	dB
Output Sink Current	$V_{FB} = 2.7V$, $V_{(COMP)} = 1.1V$ (note 1)	1.2	1.5	—	1.5	1.7	—	mA
Output Source Current	$V_{FB} = 2.3V$, $V_{(COMP)} = 5V$ (note 1)	3	3.4	—	3.9	4.2	—	mA
V_{OUT} High	$V_{FB} = 2.3V$, $R_L = 10k$ to ground	5.8	6	6.5	5.8	6	6.5	V
V_{OUT} Low	$V_{FB} = 2.7V$, $R_L = 10k$ to V_{REF}	0.1	0.7	1.1	0.1	0.7	1.1	V
Rise Response	(note 1)	—	5	7	—	5	7	µs
Fall Response	(note 1)	—	3	5	—	3	5	µs
Current Sense Section								
Gain Ratio	(notes 2 & 3)	2.8	2.9	3.1	2.8	2.9	3.1	V/V
Maximum Input Signal	$V_{(COMP)} = 5V$ (note 2)	0.85	0.95	1.05	0.85	0.95	1.05	V
PSRR	$9.5V \le V_{IN} \le 15V$ (notes 1, 2 & 5)	70	80	—	70	80	—	dB
Input Bias Current	(note 1)	—	±0.3	±2	—	±0.3	±2	nA
Delay to Output	$V(I_{SENSE}) = 1V$ (note 1); Figure 3	—	140	160	—	140	150	ns
Output Section								
$r_{DS\ (ON)}$	$I_{SINK} = 20$ mA	—	7	15	—	7	15	Ω
$r_{DS\ (ON)}$	$I_{SOURCE} = 20$ mA	—	11	20	—	11	15	Ω
Rise Time	$C_L = 1$ nF (note 1)	—	40	60	—	35	60	ns
Fall Time	$C_L = 1$ nF (note 1)	—	30	40	—	30	40	ns
Cross Conduction	In coulombs (note 1)	—	6.5	—	—	6.5	—	nC
V_{DD} Max	(note 1)	—	—	18	—	—	18	V

ELECTRICAL CHARACTERISTICS (Cont): unless otherwise stated, these specifications apply over specified temperature range. $V_{IN} = V_{DD} = 15V$; $R_T = 71\ k\Omega$; $C_T = 150\ pF$.

		TC18C4X TC28C4X			TC38C4X			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Under Voltage Lockout Section								
Start Threshold	X8C42/4	14.1	14.5	14.9	14.1	14.5	14.9	V
	X8C43/5	8	8.4	8.8	8	8.4	8.8	V
Under Voltage Threshold	X8C42/4	8.6	9	9.4	8.6	9	9.4	V
	X8C43/5	7.3	7.6	7.9	7.3	7.6	7.9	V
PWM Section								
Maximum Duty Cycle	X8C42/3 (note 1)	95	97	100	95	97	100	%
	X8C44/5 (note 1)	46	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Supply Current								
Start Up	$T_A = 25°C$, $V_{IN} < V_{UV}$; Figure 1	50	170	300	50	170	300	µA
Operating	$V_{FB} = V(I_{SENSE}) = 0V$; Figure 4		1	2		1	1.5	mA

NOTES: 1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch.
3. Gain ratio is defined as:

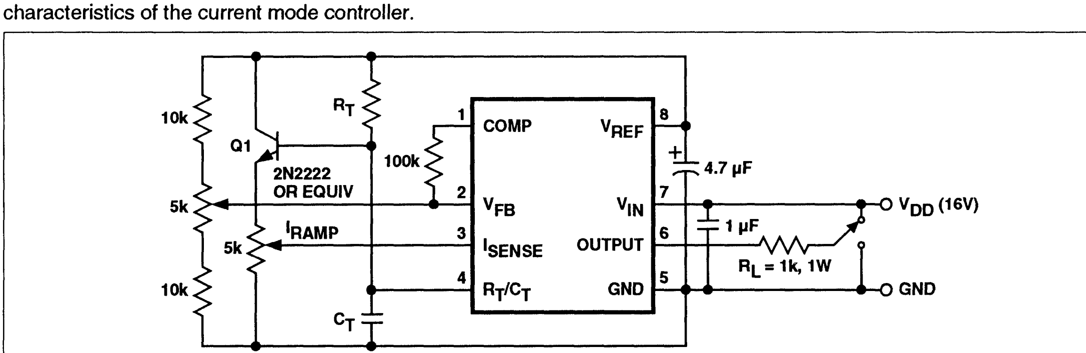
$$\frac{\Delta V_{COMP}}{\Delta V(I_{SENSE})}$$

where $0 \leq V(I_{SENSE}) \leq 0.8V$

4. Output frequency equals oscillator frequency for the X8C42 and X8C43. Output frequency is one half oscillator frequency for the X8C44 and X8C45.
5. PSRR of V_{REF}, Error Amp and PWM Comparator combination.

BENCH TEST OPERATIONAL SIMULATION

The timing ramp (R_T/C_T) is buffered by the emitter follower and fed back to the I_{SENSE} input. This ramp simulates the dI/dT current ramp which would flow through the primary of the transformer. The output voltage of the power supply is simulated by feeding some of the reference voltage into V_{FB}. The combination of the two input levels determines the operating characteristics of the current mode controller.



TYPICAL CHARACTERISTICS

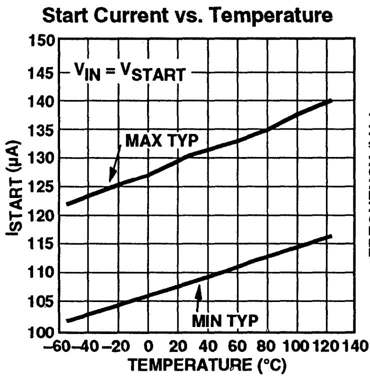


Figure 1

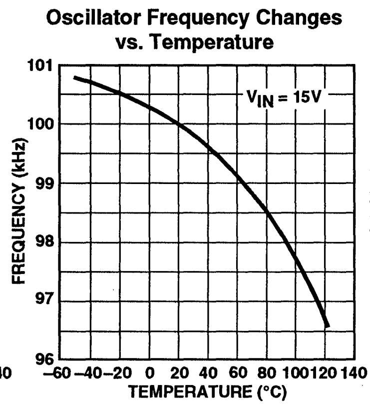


Figure 2

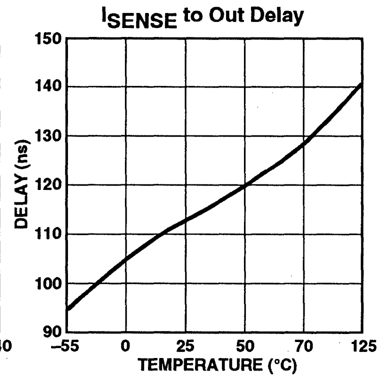


Figure 3

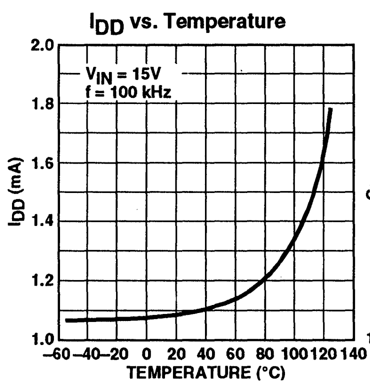


Figure 4

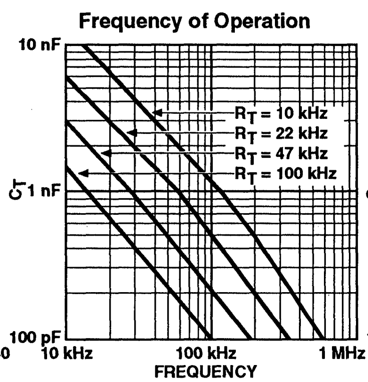


Figure 5

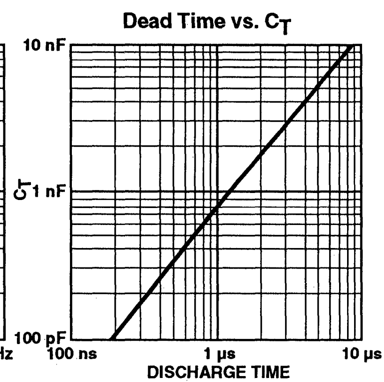


Figure 6

TELEDYNE COMPONENTS

TC18C46 TC18C47 TC28C46 TC28C47 TC38C46 TC38C47

CMOS CURRENT MODE PWM CONTROLLER

FEATURES

- Isolated Output Drive
- Low Power CMOS Construction
- Low Supply Current ....2 mA Typ
- Wide Supply Voltage Operation ....8V to 18V
- Latch-Up Immunity...................500 mA on Outputs
- Above and Below Rail Input Protection 6V
- High Output Drive ....500 mA Peak
- Current Mode Control
- Fast Rise/Fall Time ....50 ns @ 1000 pF
- High Frequency Operation..........................500 kHz
- UV Hysteresis Guaranteed
- Shutdown Pin Available
- Double Ended
- Soft Start
- Low Prop Delay Current Amp to Output ....< 350 ns Typ
- Low Prop Delay Shutdown to Output ....< 400 ns Typ
- TC38C46/47 Pin Compatible with Unitrode UC3846/3847
- ESD Protected ....±2 kV

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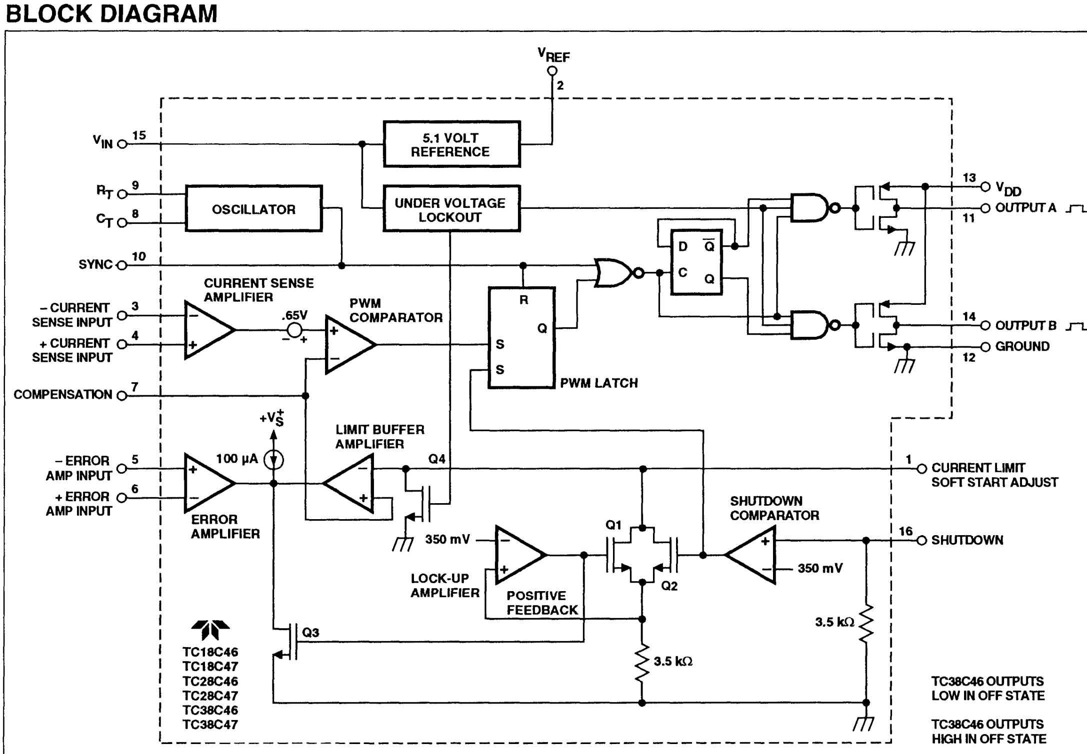
BLOCK DIAGRAM



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CMOS CURRENT MODE PWM CONTROLLER

TC18C46 TC18C47
TC28C46 TC28C47
TC38C46 TC38C47

GENERAL DESCRIPTION

The TC38C46/47 are current mode CMOS PWM control ICs. These only draw 2 mA supply current, so they can be driven without a costly 50-60 Hz transformer. The output drive stage is capable of high drive currents, 300 mA typical.

The TC38C46/47 are pin compatible with earlier bipolar products so that designers can easily update older designs. A number of improvements have been added.

This second generation part has been designed with an isolated drive stage. Unlike its cousin, the TC170, the output stage of the TC38C46/47 can be run from a separate power supply such as a secondary winding on an output transformer. This allows for bootstrap start-up of the power supply.

ORDERING INFORMATION

Part No.	Configuration	Pkg./Temperature
TC18C46MJE	Non-Inverting	16-Pin CerDIP –55 to +125°C
TC18C47MJE	Inverting	16-Pin CerDIP –55 to +125°C
TC28C46EOE	Non-Inverting	16-Pin SOIC (wide) –40 to +85°C
TC28C46EPE	Non-Inverting	16-Pin Plastic DIP –40 to +85°C
TC28C47EOE	Non-Inverting	16-Pin SOIC (wide) –40 to +85°C
TC28C47EPE	Non-Inverting	16-Pin Plastic DIP –40 to +85°C
TC38C46COE	Non-Inverting	16-Pin SOIC (wide) 0 to +70°C
TC38C46CPE	Non-Inverting	16-Pin Plastic DIP 0 to +70°C
TC38C47COE	Inverting	16-Pin SOIC (wide) 0 to +70°C
TC38C47CPE	Inverting	16-Pin Plastic DIP 0 to +70°C

ABSOLUTE MAXIMUM RATINGS

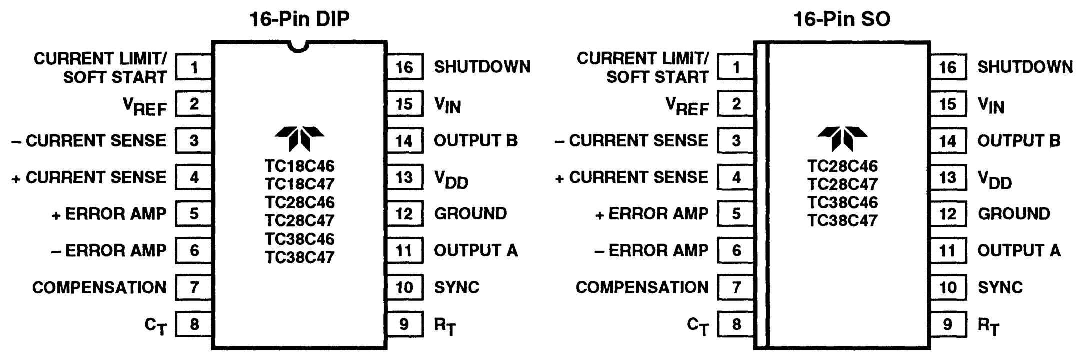
Output Current, Source or Sink (Pins 1, 14) ....500 mA
Analog Inputs (Pins 3, 4, 5, 6, 16)................–0.3V to $+V_{IN}$
Reference Output Current (Pin 2) ....–30 mA
Sync Output Current (Pin 10) ....–5 mA
Error Amplifier Output Current (Pin 7) ....–5 mA
Soft Start Sink Current (Pin 1) ....50 mA
Oscillator Charging Current (Pin 9) ....5 mA
Supply Voltage 18V
Maximum Chip Temperature ....150 °C
Storage Temperature ....–65°C to +150°C
Lead Temperature (10 sec) ....300 °C
Package Thermal Resistance
CerDIP $R_{\theta J\text{-}A}$ ....150°C/W
CerDIP $R_{\theta J\text{-}C}$ ....55°C/W
PDIP $R_{\theta J\text{-}A}$ ....125°C/W
PDIP $R_{\theta J\text{-}C}$ ....45°C/W
SOIC $R_{\theta J\text{-}A}$ ....250°C/W
SOIC $R_{\theta J\text{-}A}$ ....75°C/W

NOTES: 1. All voltages are with respect to Ground, Pin 13. Currents are positive into, negative out of the specified terminal.
2. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

CMOS CURRENT MODE PWM CONTROLLER

TC18C46 TC28C46 TC38C46 TC18C47 TC28C47 TC38C47

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS: unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for TC18C46/TC18C47; –40°C to +85°C for the TC28C46/TC28C47; and 0°C to +70°C for the TC38C46/TC38C47; V_{IN} = V_{DD} = 16V; R_T = 30.1k; C_T = 270 pF.

		TC18C46/47 TC28C46/47			TC38C46/47			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Reference Section								
Output Voltage	T_j = 25°C, I_O = 1 mA	5.05	5.1	5.15	5	5.1	5.20	V
Line Regulation	V_{IN} = 8V to 16V	—	±4	±20	—	±4	±20	mV
Load Regulation	I_O = 1mA to 10 mA	—	±4	±20	—	±4	±20	mV
Temp Coefficient	Over Operating Range, (note 1)	—	±0.2	±0.5	—	±0.2	±0.5	mV/°C
Total Output Range	Line, Load, and Temperature (note 1)	4.97	—	5.24	4.94	—	5.26	V
Long Term Drift	T_j = 125°C, 1000 Hrs (note 1)	—	±50	—	—	±50	—	mV
Short Circuit Output Current	V_{REF} = 0V	20	—	70	20	—	70	mA
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_j = 25°C (note 1)	—	22	—	—	22	—	µV(rms)
Oscillator Section								
Initial Accuracy	T_j = 25°C	96.5	102	106.5	96.5	101	106.5	kHz
Voltage Coefficient	V_{IN} = 8V to 16V	—	±.1	±1.5	—	±.1	±1.5	%/V
Temp Coefficient	Over Operating Range (note 1)	—	±.04	±0.06	—	±.04	±0.06	%/°C
Clock Ramp Reset Current		1.2	2	3	1.2	2	3	mA
Osc Ramp Amplitude		3.6	3.8	4	3.6	3.8	4	V
Sync Output High Level	(note 1)	V_{DD} –0.5	—	—	V_{DD} –0.5	—	—	V
Sync Output Low Level	(note 1)	—	—	0.5	—	—	0.5	V
Sync Input High Level	Pin 8 = 0V, (note 1)	12	8.5	—	12	8.5	—	V
Sync Input Low Level	Pin 8 = 0V, (note 1)	—	8.5	5	—	8.5	5	V
Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V	—	±5	±50	—	±5	±50	nA

ELECTRICAL CHARACTERISTICS (Cont): unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for TC18C46/TC18C47; –40°C to +85°C for the TC28C46/TC28C47; and 0°C to +70°C for the TC38C46/TC38C47; V_{IN} = V_{DD} = 16V; R_T = 30.1k; C_T = 270 pF.

		TC18C46/47 TC28C46/47			TC38C46/47			
Parameter	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Error Amp Section								
Input Offset Voltage		—	±5	±25	—	±5	±25	mV
Input Bias Current		—	±10	±100	—	±0.1	±0.5	nA
Input Offset Current		—	±10	±100	—	±0.1	±0.5	nA
Open Loop Voltage Gain	ΔV_O = 1V to 6V, R_L = 100k	70	90	—	70	90	—	dB
Gain Bandwidth Product	T_f = 25°C (note 1)	0.7	1	—	0.7	1	—	MHz
CMRR	V_{CM} = 0V to 11V	70	90	—	70	90	—	dB
PSRR	V_{IN} = 8V to 16V	70	90	—	70	90	—	dB
Output Sink Current	V(EA –) = 5V, V(EA+) = 4.9V, V(COMP) = 1.2V	2	4	—	2	4	—	mA
Output Source Current	V(EA –) = 5V, V(EA+) = 5.1V, V(COMP) = 2.5V	5	10	—	5	10	—	mA
High Level Output Volt	R_L = (COMP) 5 kΩ to GND, A_{CL} = 300	4.9	5	5.1	4.9	5	5.1	V
Low Level Output Volt	R_L = (COMP) 5 kΩ to GND, A_{CL} = 300	—	0.4	0.9	—	0.4	0.9	V
Slew Rate		1.3	2	—	1.3	2	—	V/µs
Current Sense Section								
Amplifier Gain	(notes 2, 3)	2.7	3	3.4	2.7	3	3.4	V
Max Differential Input Signal ($V_{Pin\ 4}$-$V_{Pin\ 3}$)	(note 2)	1.1	1.5	1.8	1.1	1.5	1.8	V
Input Offset Voltage	(note 2)	0.4	0.65	0.85	0.4	0.65	0.85	V
CMRR	V_{CM} = 1V to 12V, (note 2)	40	60	—	40	60	—	dB
PSRR	V_{IN} = 8V to 16V, (note 2)	40	60	—	40	60	—	dB
Input Bias Current	(note 1)	—	±1	±100	—	±1	±100	nA
Input Offset Current	(note 1)	—	±0.1	±2	—	±0.1	±2	nA
Input Common Mode Range	(note 1)	0	—	11	0	—	11	V
Delay to Outputs	T_f = 25°C, (note 1)	150	225	400	150	225	400	ns
Current Limit Adjust Section								
Current Limit Voltage Offset		—	±1	±25	—	±1	±25	mV
Input Impedance	(Shutdown Unlatched)	3	3.5	4	30	3.5	4	kΩ
Shutdown Terminal Section								
Threshold Voltage		320	360	400	320	360	400	mV
Input Voltage Range	(note 1)	0	—	V_{IN}	0	—	V_{IN}	V
Min Latching Current ($I_{Pin\ 1}$)	(note 4)	140	—	—	140	—	—	µA
Max Non-Latching Current (I_{Pin1})	(note 5)	—	—	65	—	—	65	µA
Min Pulse Width	(note 1)	100	50	—	100	50	—	ns
Delay to Outputs	(note 1)	125	250	400	125	250	400	ns

ELECTRICAL CHARACTERISTICS (Cont): unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for TC18C46/TC18C47; –40°C to +85°C for the TC28C46/TC28C47; and 0°C to +70°C for the TC38C46/TC38C47; $V_{IN} = V_{DD}$ = 16V; R_T = 30.1k; C_T = 270 pF.

Parameter	Test Conditions	TC18C46/47 TC28C46/47 Min	Typ	Max	TC38C46/47 Min	Typ	Max	Units
Output Section								
Output Low Level $r_{DS\,(ON)}$	I_{SINK} = 20 mA	—	10	20	—	10	20	Ω
Output High Level $r_{DS\,(ON)}$	I_{SOURCE} = 20 mA	—	20	35	—	20	35	Ω
Output Rise Time	C_L = 1 mF	—	55	90	—	55	90	ns
Output Fall Time	C_L = 1 mF	—	55	90	—	55	90	ns
Under Voltage Lockout Section								
Under Voltage Threshold		6.6	7	7.3	6.6	7	7.3	V
Start Threshold		7.5	7.8	8	7.5	7.8	8	V
Threshold Hysteresis		0.6	0.8	1	0.6	0.8	1	V
Total Standby Current								
Supply Current		—	1.2	2.5	—	1.2	2	mA
Start-Up Current		—	250	350	—	250	350	µA

NOTES: 1. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
2. Parameter measured at trip point of latch with $V_{Pin\,6} = V_{REF}$, $V_{Pin\,16}$ = 0V.
3. Amplifier gain is defined as: $G = \frac{\Delta V_{Pin\,7}}{\Delta V_{Pin\,4}}$; $\Delta V_{Pin\,4}$ = 0V to 1V
4. Current into Pin 1 guaranteed to latch circuit in shutdown state.
5. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

5

NOTES

TELEDYNE COMPONENTS

DC-TO-DC VOLTAGE CONVERTER

FEATURES

- **Converts +5V Logic Supply to ±5V System**
- **Wide Input Voltage Range .... 1.5V to 10V**
- **Efficient Voltage Conversion 99.9%**
- **Excellent Power Efficiency 98%**
- **Low Power Supply .... 500 μA Max**
- **Low Cost and Easy to Use**
  — Only Two External Capacitors Required
- **RS232 Negative Power Supply**
- **Available in Small Outline (SO) Package**

GENERAL DESCRIPTION

The TC7660 DC-to-DC voltage converter will generate a negative voltage from a positive source. With two external capacitors, the TC7660 will convert a 1.5V to 10V input signal to a –1.5V to –10V level. The TC7660 easily generates –5V in +5V digital systems.

Many analog-to-digital converters, digital-to-analog converters, operational amplifiers, and multiplexers require negative supply voltages. The TC7660 allows +5V digital logic systems to incorporate these analog components without adding an additional main power source. The TC7660 can lower total system cost, ease engineering development, and save space, power and weight.

The TC7660 charges a capacitor to the applied supply voltage. Internal analog gates connect the capacitor across the output. Charge is transferred to an output storage capacitor, completing the voltage conversion. Operation requires only two external capacitors for supply voltage <6.5V.

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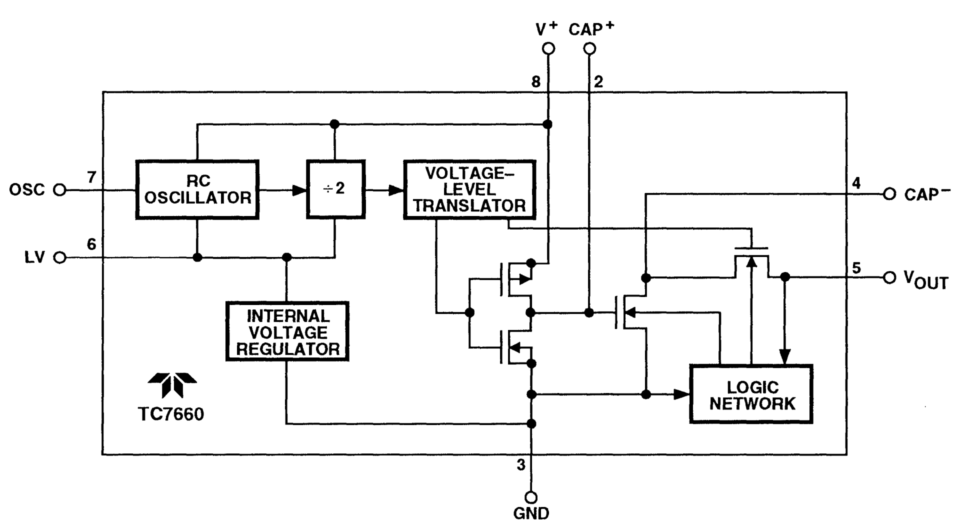
BLOCK DIAGRAM



Contained on-chip are a series DC power supply regulator, RC oscillator, voltage-level translator, four output power MOS switches, and a unique logic element which ensures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5V. This frequency can be lowered by the addition of an external capacitor to the OSC terminal (pin 7), or the oscillator may be overdriven by an external clock.

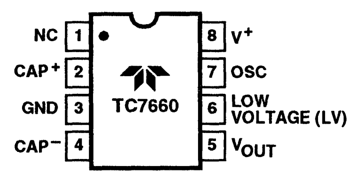
The low voltage (LV) terminal (pin 6) may be tied to GND (pin 3) to bypass the internal series regulator and improve LV operation. At medium-to-high voltages (+3.5V to +10V), the LV pin is left floating to prevent device latch-up.

The TC7660 open-circuit output voltage is equal to the input voltage to within 0.1%. The TC7660 has a 98% power conversion efficiency for 2 mA to 5 mA load currents.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7660CPA	8-Pin Plastic DIP	0°C to +70°C
TC7660IJA	8-Pin CerDIP	–40°C to +85°C
TC7660EOA	8-Pin Plastic DIP	–40°C to +85°C
TC7660EPA	8-Pin Plastic DIP	–40°C to +85°C
TC7660MJA	8-Pin CerDIP	–55°C to +125°C
TC7660COA	8-Pin SO	0°C to +70°C

PIN CONFIGURATION (DIP and SO)



NC = NO INTERNAL CONNECTION

DC-TO-DC VOLTAGE CONVERTER

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +10.5V
LV and OSC Inputs
  Voltage (Note 1) .... –0.3V to (V^++0.3V)
  for V^+ <5.5V
  (V^+–5.5V) to (V^++0.3V)
  for V^+ <5.5V
Current Into LV (Note 1) .... 20 µA for V^+ >3.5V
Output Short Duration ($V_{SUPPLY} \leq$ 5.5V) .... Continuous
Power Dissipation (Note 2)
  CerDIP .... 500 mW
  Plastic DIP .... 375 mW
Operating Temperature Range
  C Suffix .... 0°C to +70°C
  I Suffix .... –25°C to +85°C
  E Suffix .... –40°C to +85°C
  M Suffix .... –55°C to +125°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

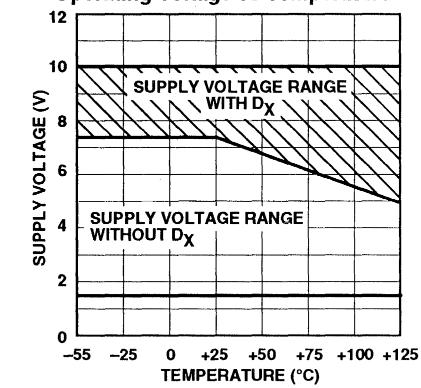
ELECTRICAL CHARACTERISTICS: V^+ = 5V, T_A = +25°C, C_{OSC} = 0, Test Circuit (Figure 1), unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I^+	Supply Current	$R_L = \infty$	—	170	500	µA
V^+_{H1}	Supply Voltage Range, High	0°C ≤ T_A ≤ +70°C, R_L = 10 kΩ, LV Open	3	—	6.5	V
	(D_X Out of Circuit) (Note 3)	–55°C ≤ T_A ≤ +125°C, 10 kΩ, LV Open	3	—	5	V
V^+_{L1}	Supply Voltage Range, Low (D_X Out of Circuit)	Min ≤ T_A ≤ Max, R_L = 10 kΩ, LV to GND	1.5	—	3.5	V
V^+_{H2}	Supply Voltage Range, High (D_X In Circuit)	Min ≤ T_A ≤ Max, R_L = 10 kΩ, LV Open	3	—	10	V
V^+_{L2}	Supply Voltage Range, Low (D_X In Circuit)	Min ≤ T_A ≤ Max, R_L = 10 kΩ, LV to GND	1.5	—	3.5	V
R_{OUT}	Output Source Resistance	I_{OUT} = 20 mA, T_A = 25°C	—	55	100	Ω
		I_{OUT} = 20 mA, 0°C ≤ T_A ≤ +70°C (C Device)	—	—	120	Ω
		I_{OUT} = 20 mA, –25°C ≤ T_A ≤ +85°C (I Device)	—	—	130	Ω
		I_{OUT} = 20 mA, –55°C ≤ T_A ≤ +125°C (M Device)	—	—	150	Ω
		V^+ = 2V, I_{OUT} = 3 mA, LV to GND 0°C ≤ T_A ≤ +70°C	—	—	300	Ω
		V^+ = 2V, I_{OUT} = 3 mA, LV to GND –55°C ≤ T_A ≤ +125°C (Note 3)	—	—	600	Ω
f_{OSC}	Oscillator Frequency		—	10	—	kHz
PEF	Power Efficiency	R_L = 5 kΩ	95	98	—	%
$V_{OUT\,EF}$	Voltage Conversion Efficiency	$R_L = \infty$	97	99.9	—	%
Z_{OSC}	Oscillator Impedance	V^+ = 2V	—	1	—	MΩ
		V^+ = 5V	—	100	—	kΩ

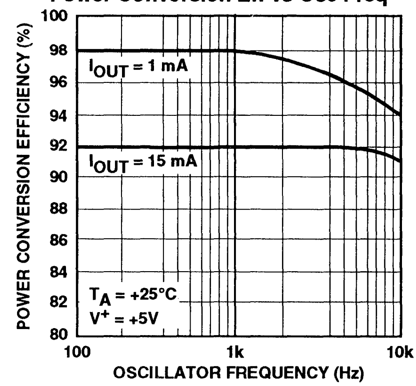
NOTES: 1. Connecting any input terminal to voltages greater than C+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TC7660.
2. Derate linearly above 50°C by 5.5 mW/°C.
3. TC7660M only.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 1)

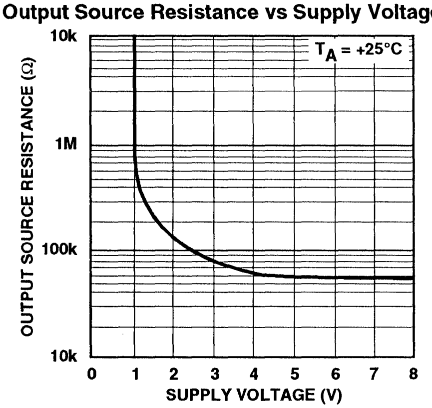
Operating Voltage vs Temperature



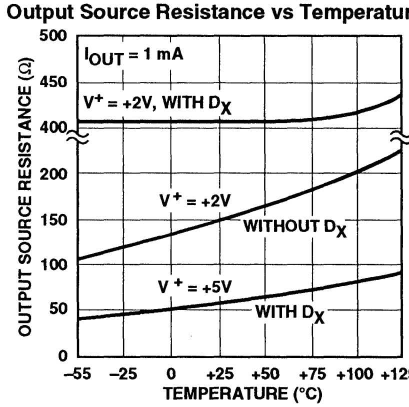
Power Conversion Eff vs Osc Freq



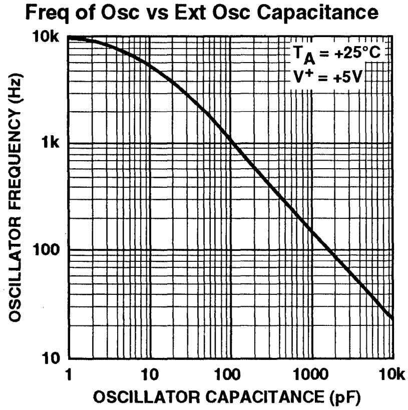
Output Source Resistance vs Supply Voltage



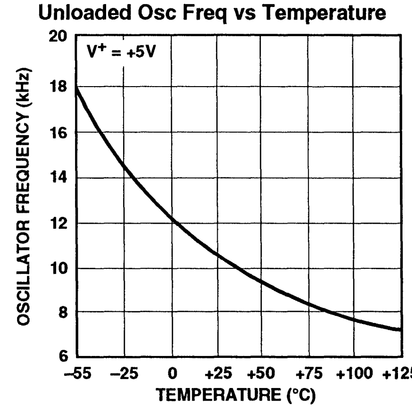
Output Source Resistance vs Temperature



Freq of Osc vs Ext Osc Capacitance

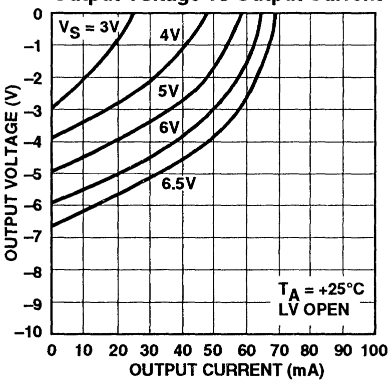


Unloaded Osc Freq vs Temperature

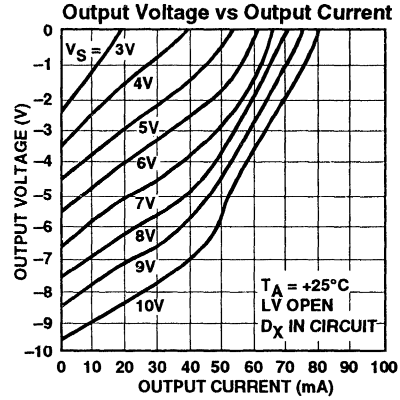


TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

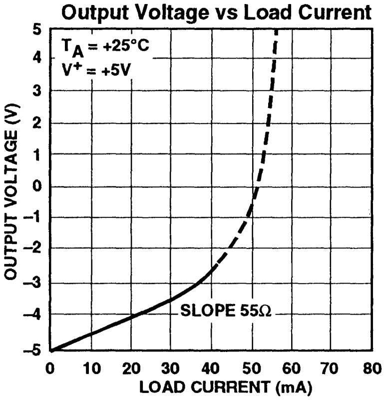
Output Voltage vs Output Current



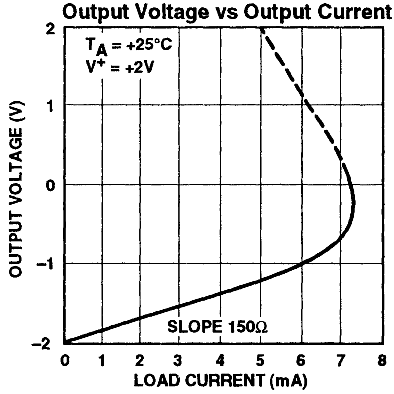
Output Voltage vs Output Current



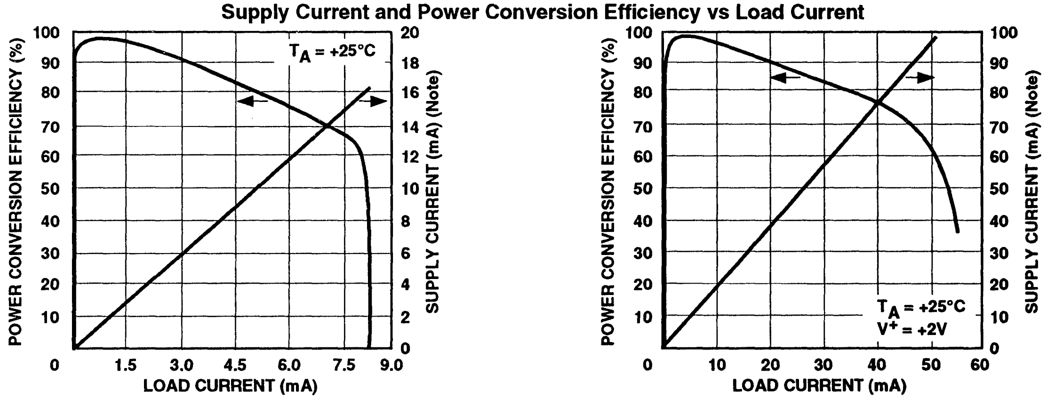
Output Voltage vs Load Current



Output Voltage vs Output Current

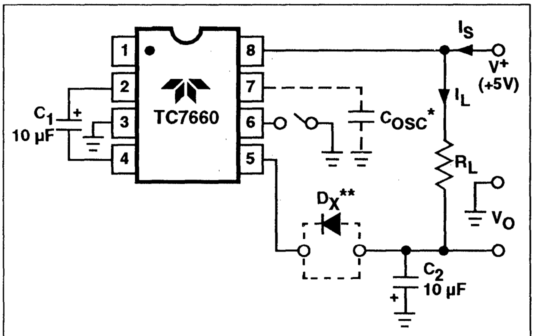


Supply Current and Power Conversion Efficiency vs Load Current



NOTE: The curves on the right include in the supply current that current fed directly into the load (R_L) from V^+ (see Figure 1). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half through the TC7660, to the negative side of the load. Ideally, $V_{OUT} = 2\ V_{IN}$, $I_S \cong 2\ I_L$, so $V_{IN} \bullet I_S \cong V_{OUT} \bullet I_L$.

TC7660



NOTES: * For large values of C_{OSC} (>1000 pF), the values of C_1 and C_2 should be increased to 100 µF.
** D_X is required for supply voltages greater than 6.5V at $-55° \leq T_A \leq +70°C$. Refer to performance curves for additional information.

Figure 1. TC7660 Test Circuit

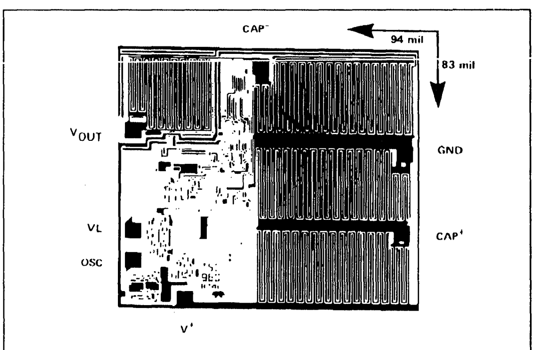


Figure 2. Chip Topography

Circuit Description

The TC7660 contains all the necessary circuitry to complete a voltage doubler, with the exception of two external capacitors, which may be inexpensive 10 µF polarized electrolytic capacitors. Operation is best understood by considering Figure 3, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (**Note:** Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2, such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

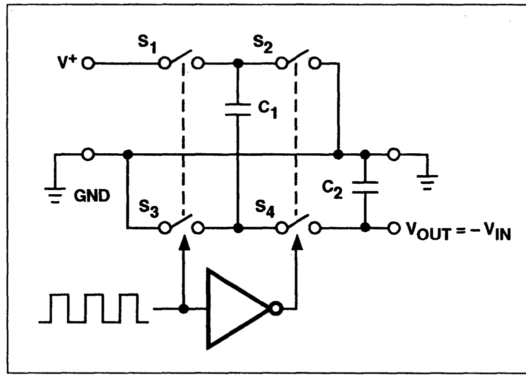


Figure 3. Idealized Switched Capacitor

The four switches in Figure 3 are MOS power switches; S_1 is a P-channel device, and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start-up, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up.

This problem is eliminated in the TC7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the TC7660 is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can, however, degrade operation at low voltages. To improve low-voltage operation, the LV pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation and prevent device damage.

Theoretical Power Efficiency Considerations

In theory, a voltage multiplier can approach 100% efficiency if certain conditions are met:

(1) The drive circuitry consumes minimal power.

(2) The output switches have extremely low ON resistance and virtually no offset.

(3) The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\, C_1\, (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 3), compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Dos and Don'ts

- Do not exceed maximum supply voltages.
- Do not connect LV terminal to GND for supply voltages greater than 3.5V.
- Do not short circuit the output to V^+ supply for voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the TC7660 and the + terminal of C_2 must be connected to GND.
- Add diode D_X (as shown in Figure 1) for high-voltage, elevated-temperature applications. A 1N914 diode is suitable.

Considerations for High Voltage and Elevated Temperature

The TC7660 will operate efficiently over its specified temperature range with only two external passive components (storage and pump capacitors), provided the operating supply voltage does not exceed 6.5V at +70°C and 5V at +125°C. Exceeding these maximums at the temperatures indicated may result in destructive latch-up of the TC7660.

Operation at supply voltages up to 10V over the full temperature range, without danger of latch-up, can be achieved by adding a general-purpose diode in series with the TC7660 output, as shown by D_X in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6V).

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

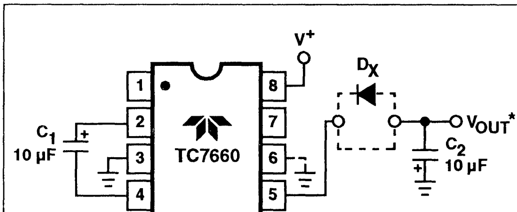
Figure 4 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +10V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V, and that diode D_X must be included for proper operation at higher voltage and/or elevated temperatures.

The output characteristics of the circuit in Figure 4 are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of –10 mA and a supply voltage of +5V, the output voltage would be –4.3V.

The dynamic output impedance of the TC7660 is due, primarily, to capacitive reactance of the charge transfer capacitor (C_1). Since this capacitor is connected to the output for only 1/2 of the cycle, the equation is:

$$X_C = \frac{2}{2\pi f\, C_1} = 3.18\Omega,$$

where f = 10 kHz and C_1 = 10 μF.



*NOTES: 1. $V_{OUT} = -n\, V^+$ for $1.5V \leq V^+ \leq 6.5V$.
2. $V_{OUT} = -n\, (V^+ - V_{FDX})$ for $6.5V \leq V^+ \leq 10V$.

Figure 4. Simple Negative Converter

Paralleling Devices

Any number of TC7660 voltage converters may be paralleled to reduce output resistance (Figure 5). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\text{ (of TC7660)}}{n\text{ (number of devices)}}$$

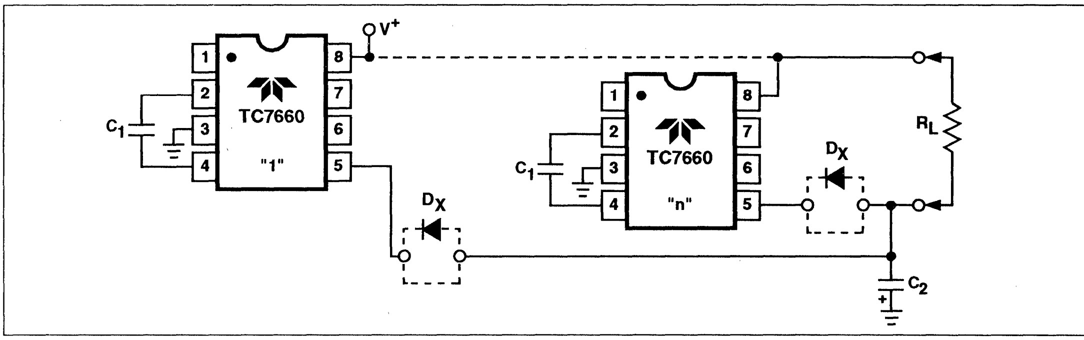


Figure 5. Paralleling Devices Lowers Output Impedance

Cascading Devices

The TC7660 may be cascaded as shown (Figure 6) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

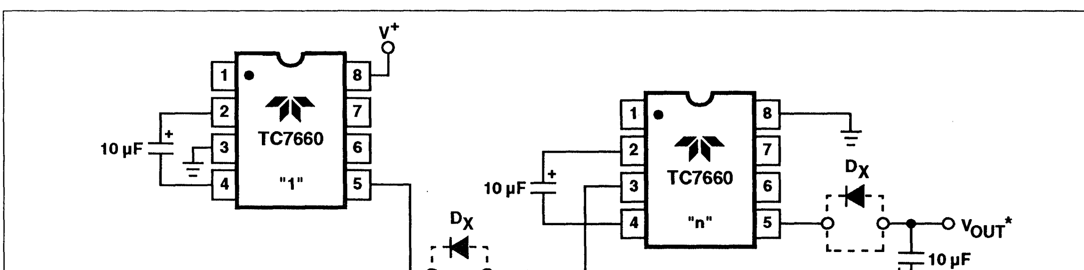
$$V_{OUT} = -n\ (V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC7660 R_{OUT} values.

Changing the TC7660 Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latch-up, a 1 kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the TC7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 8. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this, increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (OSC) and pin 8 (V^+) will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the values of C_1 and C_2 (from 10 µF to 100 µF).



*NOTES:
1. $V_{OUT} = -n\ V^+$ for $1.5V \leq V^+ \leq 6.5V$.
2. $V_{OUT} = -n\ (V^+ - V_{FDX})$ for $6.5V \leq V^+ \leq 10V$.

Figure 6. Increased Output Voltage by Cascading Devices

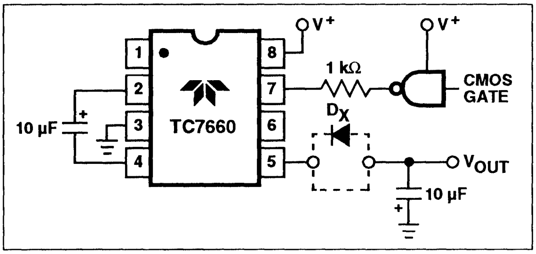


Figure 7. External Clocking

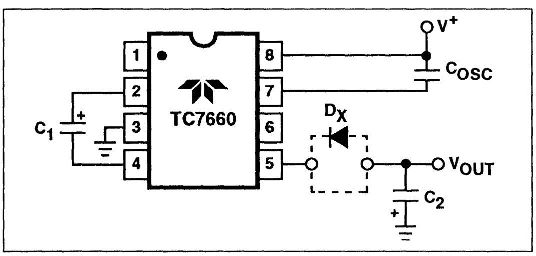


Figure 8. Lowering Oscillator Frequency

Positive Voltage Multiplication

The TC7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 9. In this application, the pump inverter switches of the TC7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2 V^+) - (2 V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5V$ and an output current of 10 mA, it will be approximately 60Ω.

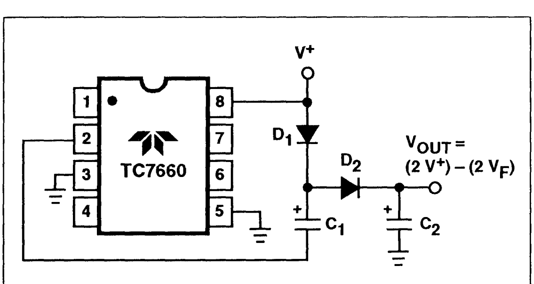


Figure 9. Positive Voltage Multiplier

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 4 and 9 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9V and –5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

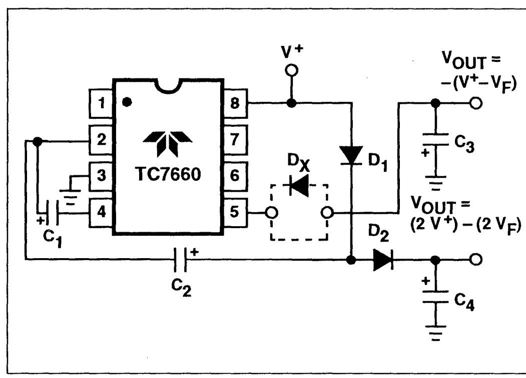


Figure 10. Combined Negative Converter and Positive Multiplier

Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backwards as easily as forwards. Figure 11 shows a TC7660 transforming –5V to +5V (or +5V to +10V, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 10, could be used to start this circuit up, after which it will bypass the other (D_1 and D_2 in Figure 10 would never turn on), or else the diode and resistor shown dotted in Figure 11 can be used to "force" the internal regulator on.

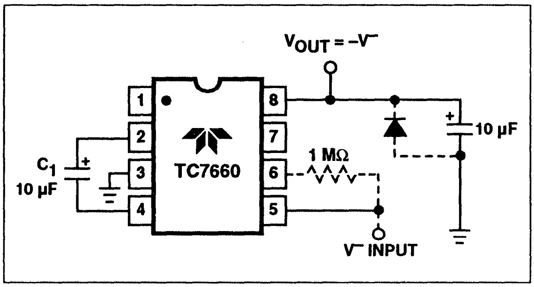


Figure 11. Positive Voltage Conversion

Voltage Splitting

The same bidirectional characteristics used in Figure 11 can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +15V can be converted (via +7.5V and –7.5V) to a nominal –15V, though with rather high series resistance (~250Ω).

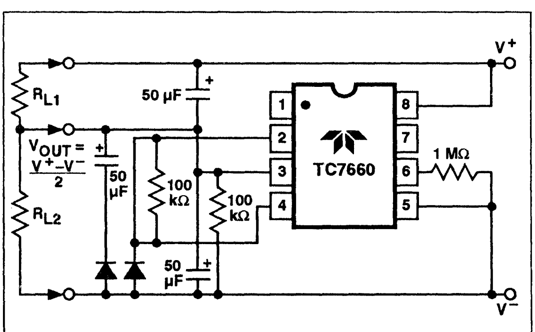


Figure 12. Splitting a Supply in Half

Negative Voltage Generation for Display ADCs

The TC7106 is designed to work from a 9V battery. With a fixed power supply system, the TC7106 will perform conversions with input signal referenced to power supply ground.

Negative Supply Generation for 4-1/2 Digit Data Acquisition System

The TC7135 is a 4-1/2 digit ADC operating from ±5V supplies. The TC7660 provides an inexpensive –5V source. (See AN16 and AN17 for TC7135 interface details and software routines.)

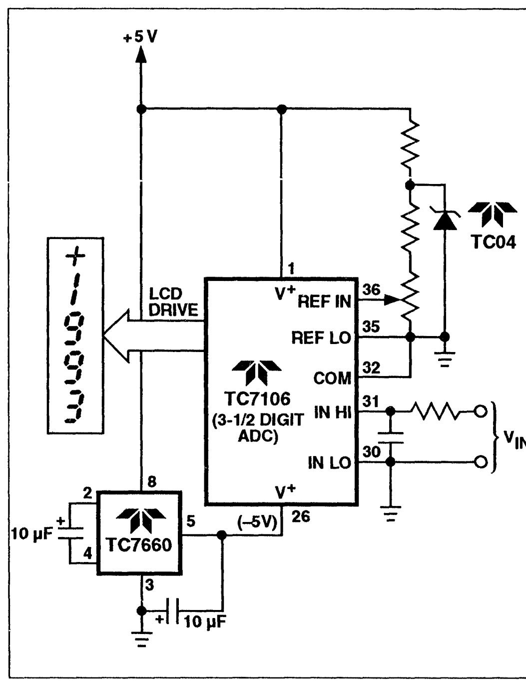


Figure 13a. Fixed Power Supply Operation of TC7106 ADC

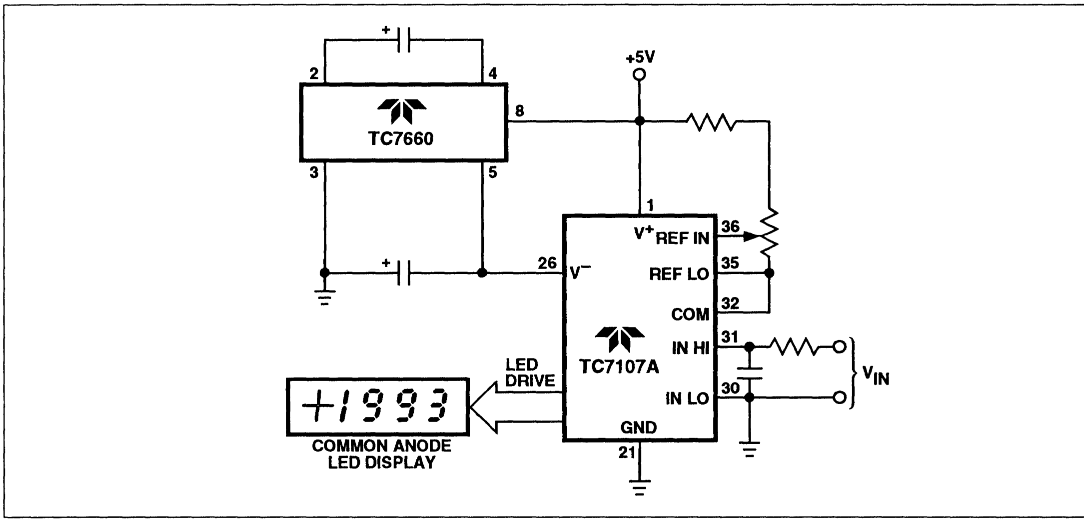


Figure 13b. Negative Power Supply Generation for TC7107A ADC

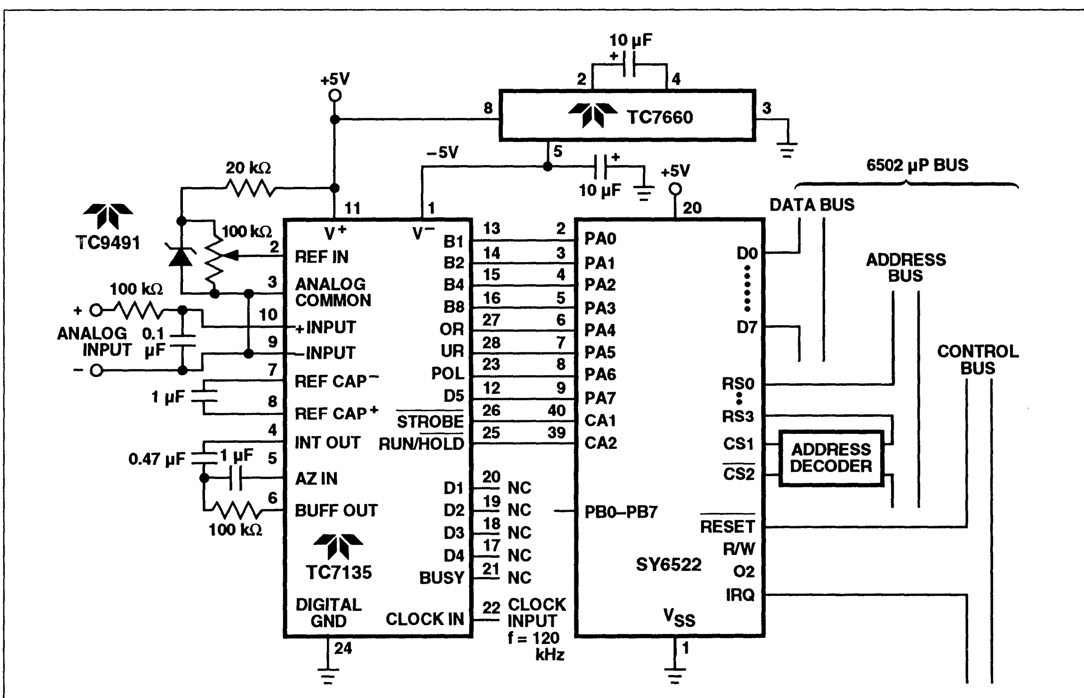


Figure 14. TC7660 Supplies –5V for Converters in Microprocessor-Controlled Data Acquisition Systems

NOTES

DC-TO-DC CONVERTER

FEATURES

- **Equivalent to ICL7662/SI7661/TC7660/LTC1044**
- **Increased Output Current .... 40 mA**
- **No External Diodes Required**
- **Wide Operating Range .... 3V to 18V**
- **Low Output Impedance @ I_L = 20 mA .... 40Ω Typ**
- **No Low-Voltage Terminal Required**
- **CMOS Construction**

GENERAL DESCRIPTION

The TC7662A is an improved version of the industry-standard TC7660/TC7662 switched capacitor DC-to-DC converters. CMOS construction and advanced design result in a device with twice the output power of the TC7662 and requires fewer parts in many applications.

The TC7662A can source 40 mA versus the TC7662's 20 mA capability. As an inverter, the TC7662A can output voltages as high as 18V and as low as 3V, without the need for external diodes. The output impedance of the device is a low 40Ω (typical), voltage conversion efficiency is 99.9%, and power conversion efficiency is 97%.

See TC962 if higher output current is required.

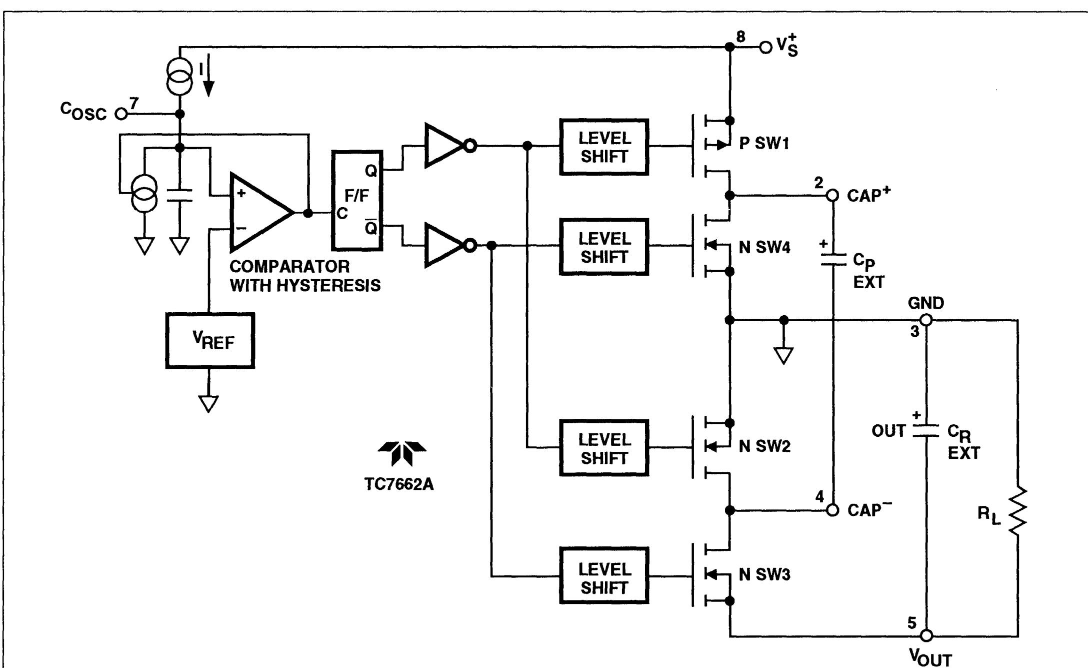
The low-voltage terminal (pin 6) required in some TC7662 applications has been eliminated. Only two external capacitors are required for inverter applications. If an external clock is needed to drive the TC7662A (such as when paralleling), driving pin 7 directly will cause the internal oscillator to sync to the external clock.

The TC7662A can be used in applications such as $V_{OUT} = -V_{IN}$, $V_{OUT} = 2\ V_{IN}$, $V_{OUT} = V_{IN}/2$, and $V_{OUT} = \pm nV_{IN}$. It may also be used as a DC-to-DC inverter, a doubler, a plus and minus supply splitter, and (when combined with other TC7662A's), as a voltage multiplier greater than two.

The TC7662A is compatible with the LTC1044, ICL7660, ICL7662, SI7661, and TC7660. It is recommended for designs requiring greater power and/or less input-to-output voltage drop.

5

FUNCTIONAL DIAGRAM

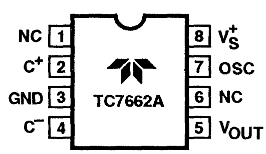


TC7662A

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7662ACPA	8-Pin Plastic DIP	0°C to +70°C
TC7662AIJA	8-Pin CerDIP	–25°C to +85°C
TC7662AEPA	8-Pin Plastic DIP	–40°C to +85°C
TC7662AMJA	8-Pin CerDIP	–55°C to +125°C

PIN CONFIGURATION



NC = NO INTERNAL CONNECTION

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_S^+ to GND .... +18V
Input Voltage (Any Pin) .... (V_S^+ + 0.3) to (V_S^- – 0.3)
Current Into Any Pin .... 10 mA
Operating Temperature Range
- CPA .... 0° to +70°C
- IJA .... –25°C to +85°C
- EPA .... –40°C to +85°C
- MJA .... –55°C to +125°C

Max Dissipation
- CPA, EPA .... 375 mW
- IJA, MJA .... 500 mW

Package Thermal Resistance
- CPA, EPA θ_{JA} .... 140°C/W
- IJA, MJA θ_{JA} .... 90°C/W

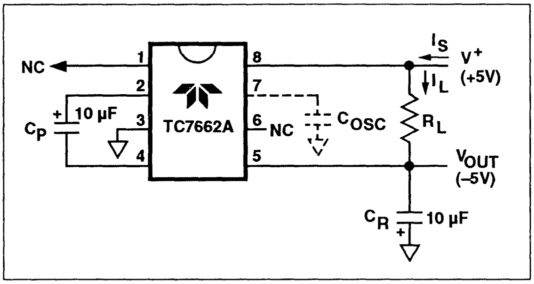
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
ESD Protection .... ±2000V
Output Short Circuit .... Continuous (at 5.5V Input)

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S^+ = 15V, T_A = +25°C (See Test Circuit)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_S^+	Supply Voltage		3	—	18	V
I_S	Supply Current	$R_L = \infty$				
	V_S^+ = +15V	T_A = +25°C	—	510	700	µA
		$0 \le T_A \le +70°C$	—	560	—	µA
		$-55 \le T_A \le +125°C$	—	650	—	µA
	V_S^+ = +5V	T_A = +25°C	—	190	—	µA
		$0 \le T_A \le +70°C$	—	210	—	µA
		$-55 \le T_A \le +125°C$	—	210	—	µA
R_O	Output Source Resistance	I_L = 20 mA, V_S^+ = +15V	—	40	50	Ω
		I_L = 40 mA, V_S^+ = +15V	—	50	60	Ω
		I_L = 3 mA, V_S^+ = +5V	—	100	125	Ω
C_{OSC}	Oscillator Frequency		—	12	—	kHz
P_{EFF}	Power Efficiency	V_S^+ = +15V, R_L = 2 kΩ	93	97	—	%
V_{EFF}	Voltage Efficiency	V^+_S = +15V, $R_L = \infty$	99	99.9	—	%
		Over Temperature Range	96	—	—	%

TEST CIRCUIT



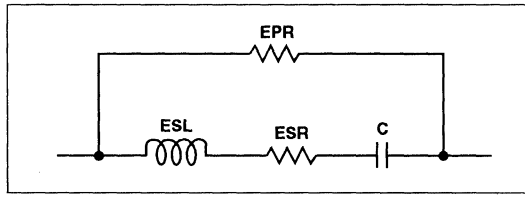


Figure 1 Capacitor Equivalent Circuit

APPLICATIONS INFORMATION

Theory of Operation

The TC7662A is a capacitive pump (sometimes called a switched capacitor circuit), where four MOSFET switches control the charge and discharge of a capacitor.

The functional diagram (page 1) shows how the switching action works. SW1 and SW2 are turned on simultaneously, charging C1 to the supply voltage, V_S^+. This assumes that the on resistance of the MOSFETs in series with the capacitor results in a charging time (3 time constants) less than the on time provided by the oscillator frequency, as shown:

$$3\ (R_{DS(ON)}\ C1) < C1/(0.5\ f_{OSC}).$$

In the next cycle, SW1 and SW2 are turned off and, after a very short interval of all switches being off (preventing large currents from occurring due to cross conduction), SW3 and SW4 are turned on. The charge in C1 is then transferred to C_{OUT}, BUT WITH THE POLARITY INVERTED. In this way, a negative voltage is now derived.

An oscillator supplies pulses to a flip-flop that is then fed to a set of level shifters. These level shifters then drive each set of switches at one-half the oscillator frequency.

The oscillator has a pin that controls the frequency of oscillation. Pin 7 can have a capacitor added that is run to ground. This will lower the frequency of the oscillator by adding capacitance to the timing capacitor internal to the TC7662A. (See Oscillator Frequency vs C_{EXT}, page 5.)

Capacitors

In early charge pump converters, capacitors were not considered critical due to the high $R_{DS(ON)}$ of the MOSFET switches. In order to understand this, let's look at a model of a typical electrolytic capacitor (Figure 1).

Note one of its characteristics is ESR (equivalent series resistance). This parasitic resistance winds up in series with the load. Thus, both voltage and power conversion efficiency are compromised if a low ESR capacitor is not used.

For example, in the "Test Circuit", changing C_P and C_R capacitors with typical ESR to low ESR types, the effective converter output impedance changed from 45Ω to 40Ω, an improvement of 12%.

This applies to all types of capacitors, including film types (polyester, polycarbonate etc.).

Some applications information suggest the capacitor is not critical and attribute the limiting factor of the capacitor to its reactive value. Let's examine this:

$$X_C = \frac{1}{2\pi f\ C} \quad \text{and} \quad Z_C = \frac{X_C}{DS},$$

where DS (duty cycle) = 50%.

Thus, $Z_C \approx 1.33\Omega$ at f = 12 kHz, where C = 10 µF.

For the TC7662A, f = 12,000 Hz, and a typical value of C would be 10 µF. This a reactive impedance of ≈1.33W. If the ESR is as great as 5W, the reactive value is not as critical as it would first appear, as the ESR would predominate. The 5W value is typical of a general-purpose electrolytic capacitor.

Synchronizing

The TC7662A may be synchronized by sourcing a 5 µs, 5 µA clock pulse to pin 7. Care should be taken not to drive pin 7 beyond +5V.

A TTL voltage level driving a diode and 100 kΩ resistor in series to pin 7 is the recommended procedure.

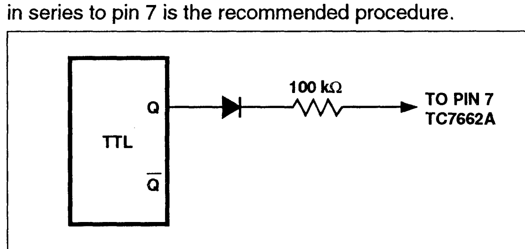
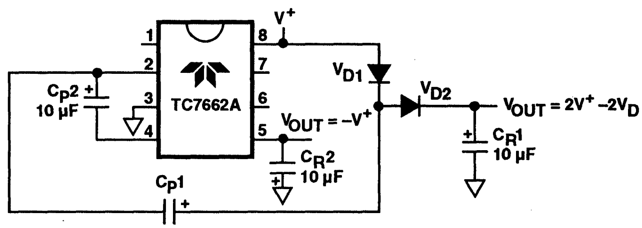


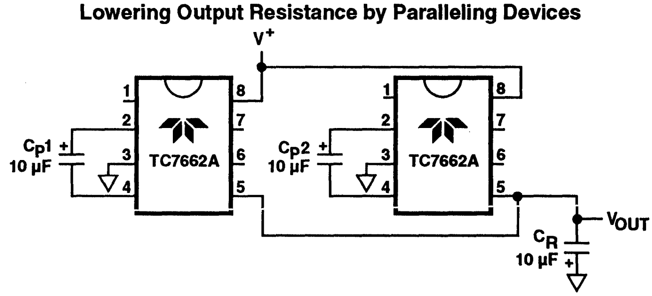
Figure 2 Synchronization

TYPICAL APPLICATIONS

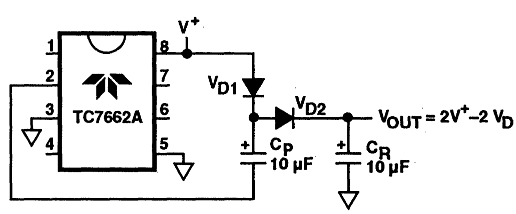
Combined Negative Converter and Positive Multiplier



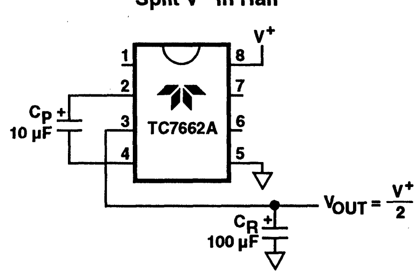
Lowering Output Resistance by Paralleling Devices



Positive Voltage Multiplier

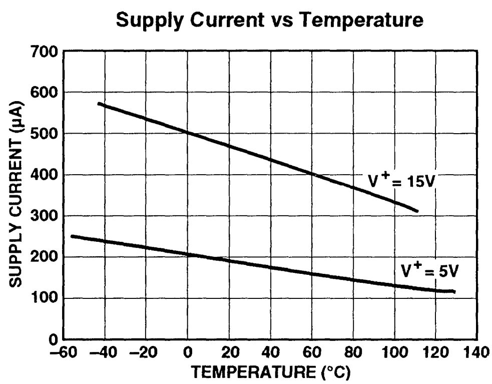


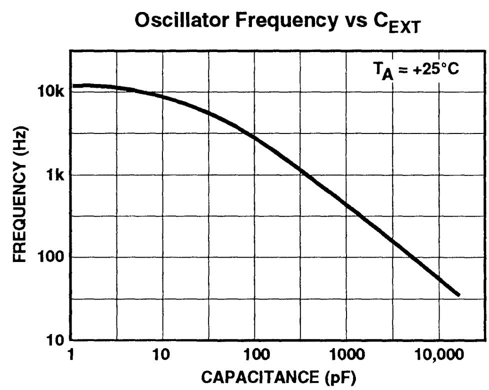
Split V+ In Half

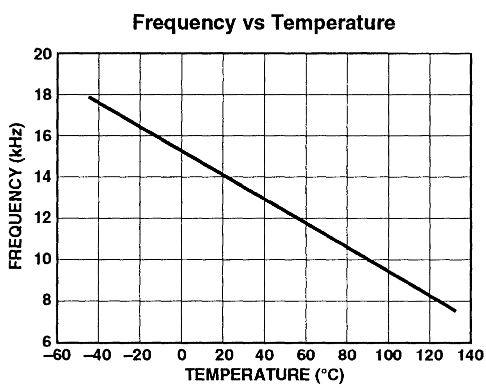


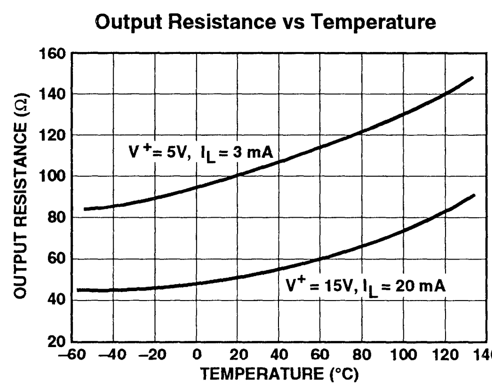
5

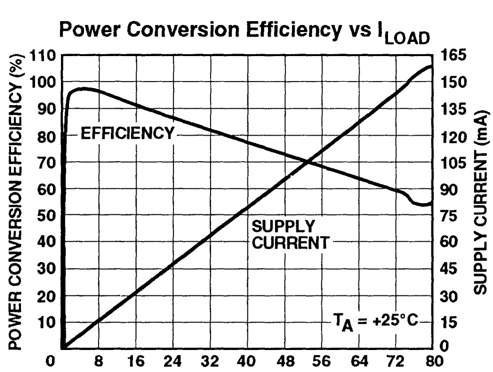
TYPICAL CHARACTERISTICS CURVES

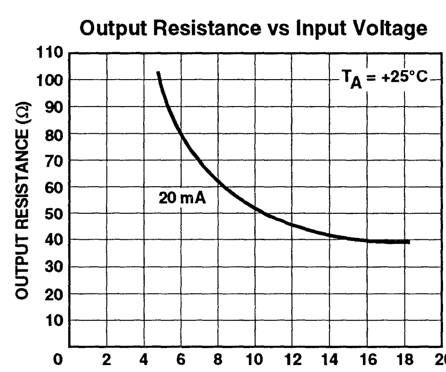












NOTES

HIGH CURRENT DC-TO-DC CONVERTER

FEATURES

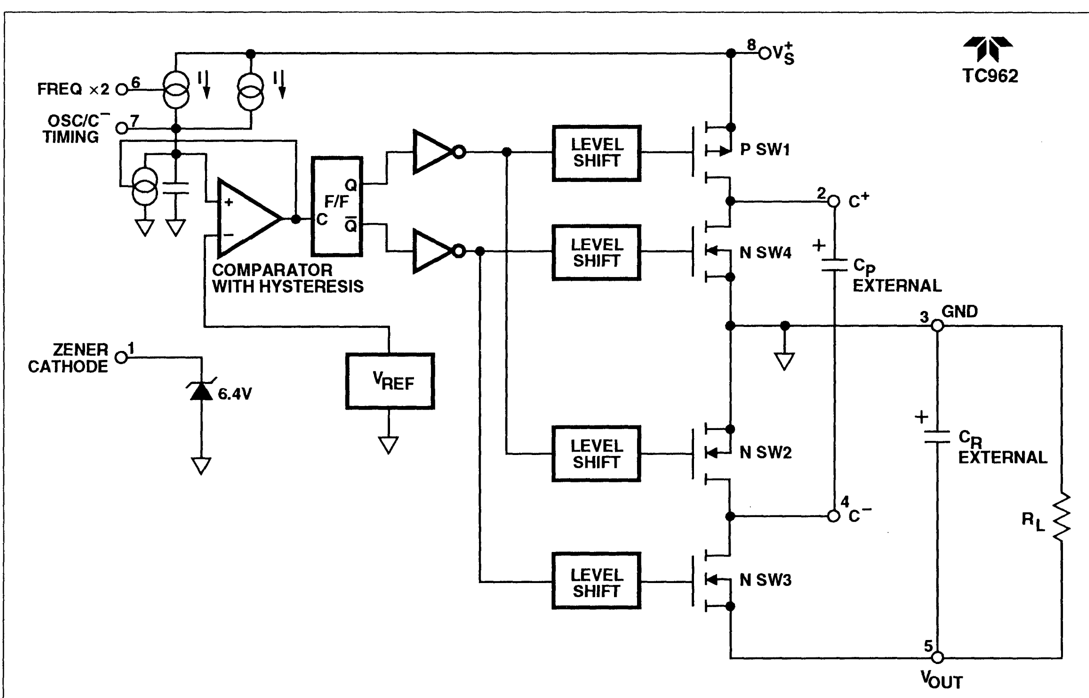
- Pin Compatible With TC7662/ICL7662/SI7661
- High Output Current .... 80 mA
- No External Diodes Required
- Wide Operating Range .... 3V to 18V
- Low Output Impedance .... 28Ω Typ
- No Low Voltage Terminal Required
- Application Zener On Chip
- Doubling Pin Option for Smaller Output Capacitors

GENERAL DESCRIPTION

The TC962 is an advanced version of the industry-standard 7662 high-voltage DC-to-DC converter. Using improved design techniques and CMOS construction, the TC962 can source as much as 80 mA versus the 7662's 20 mA capability.

As an inverter, the TC962 can put out voltages as high as 18V and as low as 3V without the need for external diodes. The output impedance of the device is a low 28Ω (with the proper capacitors), voltage conversion efficiency is 99.9%, and power conversion efficiency is 97%.

FUNCTIONAL DIAGRAM



TC962

The low voltage terminal (pin 6) required in some 7662 applications has been eliminated. Grounding this terminal will double the oscillator frequency from 12 kHz to 24 kHz. This will allow the use of smaller capacitors for the same output current and ripple, in most applications. Only two external capacitors are required for inverter applications. In the event an external clock is needed to drive the TC962 (such as paralleling), driving this pin directly will cause the internal oscillator to sync to the external clock.

Pin 1, which is used as a test pin on the 7662, is a voltage reference zener on the TC962. This zener (6.4V at 5 mA) has a dynamic impedance of 12W and is intended for use where the TC962 is supplying current to external regulator circuitry and a reference is needed for the regulator circuit. (See applications section.)

The TC962 is compatible with the LTC1044, SI7661, and ICL7662. It should be used in designs that require greater power and/or less input to output voltage drop. It offers superior performance over the ICL7660S.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_S^+ to GND) .... +18V
Input Voltage (Any Pin) .... (V_S^+ + 0.3) to (V_S^- – 0.3)
Current Into Any Pin .... 10 mA
ESD Protection .... ±2000V
Output Short Circuit .... Continuous (at 5.5V Input)
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Operating Temperature Range
CPA, COE .... 0°C to +70°C
IJA .... –25°C to +85°C
EOE, EPA .... –40°C to +85°C
MJA .... –55°C to +125°C
Max Dissipation
COE, CPA, EOE, EPA .... 375 mW
IJA, MJA .... 500 mW
Package Thermal Resistance
CerDIP, $R_{qJ\text{-}A}$ .... 90°C/W
PDIP, $R_{qJ\text{-}A}$ .... 140°C/W

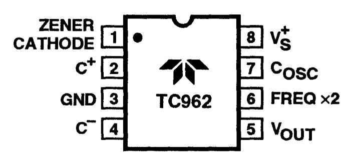
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ORDERING INFORMATION

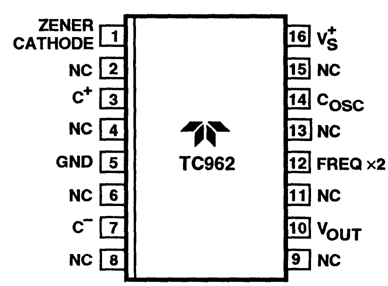
Part No.	Package	Temperature Range
TC962CPA	8-Pin Plastic DIP	0°C to +70°C
TC962IJA	8-Pin CerDIP	–25°C to +85°C
TC962EPA	8-Pin Plastic DIP	–40°C to +85°C
TC962MJA	8-Pin CerDIP	–55°C to +125°C
TC962COE	16-Pin SO	0 to +70°C
TC962EOE	16-Pin SO	–40°C to +85°C

PIN CONFIGURATIONS

8-Pin DIP



16-Pin SO



ELECTRICAL CHARACTERISTICS: $V_S^+ = 15V$, $T_A = +25°C$ (See Test Circuit)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_S^+	Supply Voltage		3		18	V
I_S	Supply Current	$R_L = \infty$				
	$V_S^+ = 15V$	$T_A = +25°C$		510	700	µA
		$0 \leq T_A \leq +70°C$		560		µA
		$-55 \leq T_A \leq +125°C$		650		µA
	$V_S^+ = 5V$	$T_A = +25°C$		190		µA
		$0 \leq T_A < +70°C$		210		µA
		$-55 \leq T_A \leq +125°C$		210		µA
R_O	Output Source Resistance	$I_L = 20$ mA, $V_S^+ = 15V$		28	32	Ω
		$I_L = 80$ mA, $V_S^+ = 15V$		30	35	Ω
		$I_L = 3$ mA, $V_S^+ = 5V$		—	46	Ω
C_{OSC}	Oscillator Frequency	Pin 6 Open		12		kHz
		Pin 6 GND		24		kHz
P_{EFF}	Power Efficiency	$V_S^+ = 15V$, $R_L = 2$ kΩ	93	97		%
V_{DEF}	Voltage Efficiency	$V_S^+ = 15V$, $R_L = \infty$	99	99.9		%
		Over Temperature Range	96	—		%
V_Z	Zener Voltage	$I_Z = 5$ mA	6.2	6.4	6.6	V
Z_{ZT}	Zener Impedance	$I_L = 2.5$ mA to 7.5 mA		12		Ω

APPLICATIONS INFORMATION

Theory of Operation

The TC962 is a capacitive pump (sometimes called a switched capacitor circuit), where four MOSFET switches control the charge and discharge of a capacitor.

The functional diagram (page 1) shows how the switching action works. SW1 and SW2 are turned on simultaneously, charging C_P to the supply voltage, V_{IN}. This assumes that the on resistance of the MOSFETs in series with the capacitor results in a charging time (3 time constants) that is less than the on time provided by the oscillator frequency as shown:

$$3\ (R_{DS(ON)}\ C_P) < C_P/(0.5\ f_{OSC})$$

In the next cycle, SW1 and SW2 are turned off and after a very short interval of all switches being off (this prevents large currents from occurring due to cross conduction), SW3 and SW4 are turned on. The charge in C_P is then transferred to C_R, BUT WITH THE POLARITY INVERTED. In this way, a negative voltage is now derived.

Page 1 shows a functional diagram of the TC962. An oscillator supplies pulses to a flip-flop that is then fed to a set of level shifters. These level shifters then drive each set of switches at one-half the oscillator frequency.

The oscillator has two pins that control the frequency of oscillation. Pin 7 can have a capacitor added that is run to ground. This will lower the frequency of the oscillator by adding capacitance to the timing capacitor internal to the TC962. Grounding pin 6 will turn on a current source and double the frequency. This will double the charge current going into the internal capacitor, as well as any capacitor added to pin 7.

A zener diode has been added to the TC962 for use as a reference in building external regulators. This zener runs from pin 1 to ground.

TC962

Capacitors

In early charge pump converters, the capacitors were not considered critical due to the high $R_{DS(ON)}$ of the MOSFET switches. In order to understand this, let's look at a model of a typical electrolytic capacitor (Figure 1).

Note that one of its characteristics is ESR (equivalent series resistance). This parasitic resistance winds up in series with the load. Thus, both voltage conversion efficiency and power conversion efficiency are compromised if a low ESR capacitor is not used.

In the test circuit, for example, just changing two capacitors, C_P and C_R, from capacitors with unspecified ESR to low ESR-type output, impedance changes from 36Ω to 28Ω, an improvement of 23%!

This applies to all types of capacitors, including film types (polyester, polycarbonate, etc.).

Some applications information suggest that the capacitor is not critical and attribute the limiting factor of the capacitor to its reactive value. Let's examine this:

$$X_C = \frac{1}{2\pi f\,C} \quad \text{and} \quad Z_C = \frac{X_C}{DS},$$

where DS (duty cycle) = 50%.

Thus, $Z_C \approx 2.6\Omega$ at f = 12 kHz, where C = 10 µF.

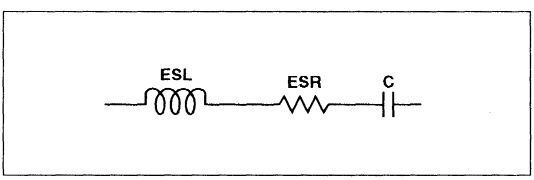


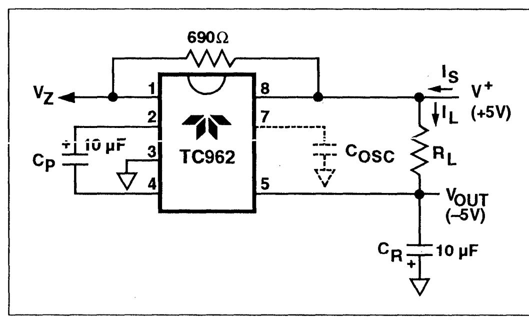
Figure 1 Typical Electrolytic Capacitor

For the TC962, f = 12,000 Hz, and a typical value of C would be 10 µF. This is a reactive impedance of ª 2.6W. If the ESR is as great as 5W, the reactive value is not as critical as it would first appear, as the ESR would predominate. The 5W value is typical of a general-purpose electrolytic capacitor.

Latch Up

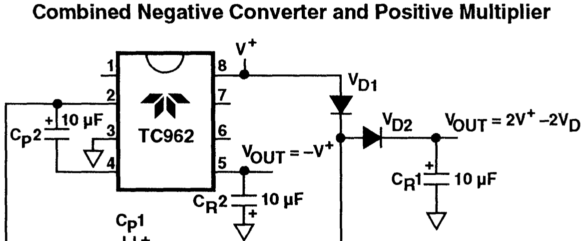
All CMOS structures contain a parasitic SCR. Care must be taken to prevent any input from going above or below the supply rail, or latch up will occur. The result of latch up is an effective short between V^+_S and V^-_S. Unless the power supply input has a current limit, this latch-up phenomena will result in damage to the device. (See Application Note 31 for additional information.)

TEST CIRCUIT

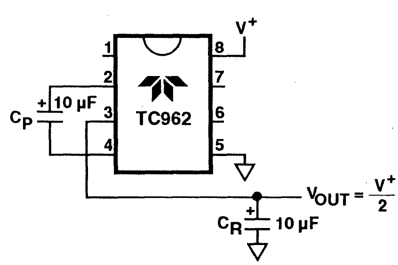


TYPICAL APPLICATIONS

Combined Negative Converter and Positive Multiplier

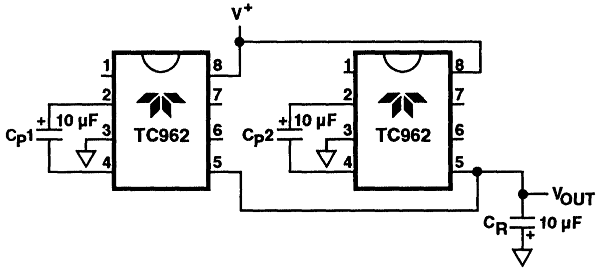


Split V+ In Half

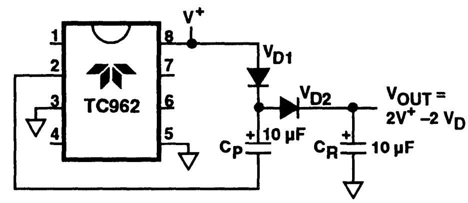


TYPICAL APPLICATIONS (Cont.)

Lowering Output Resistance by Paralleling Devices

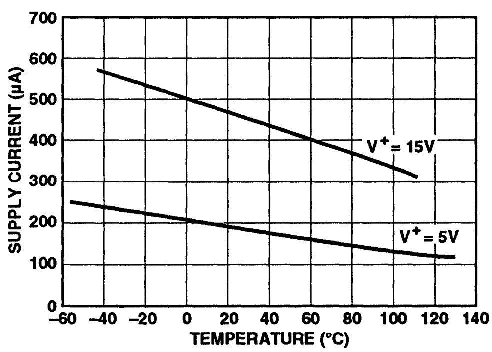


Positive Voltage Multiplier

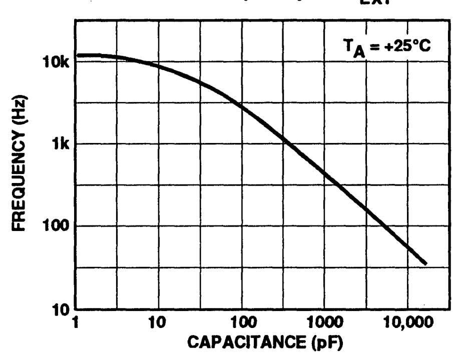


TYPICAL CHARACTERISTICS CURVES

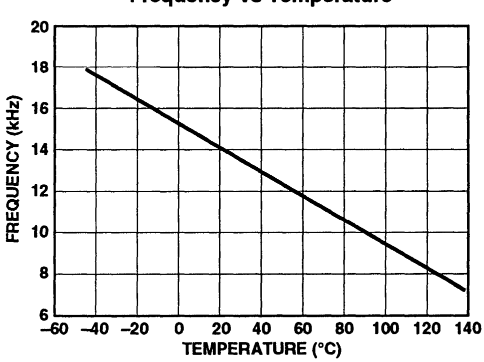
Supply Current vs Temperature



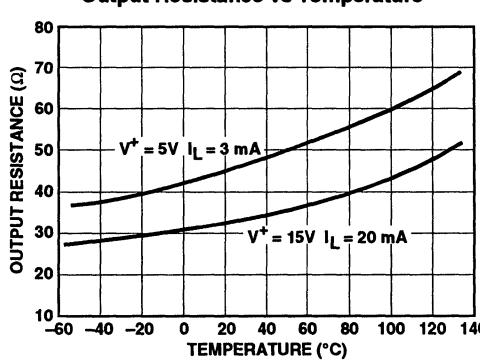
Oscillator Frequency vs C_{EXT}



Frequency vs Temperature

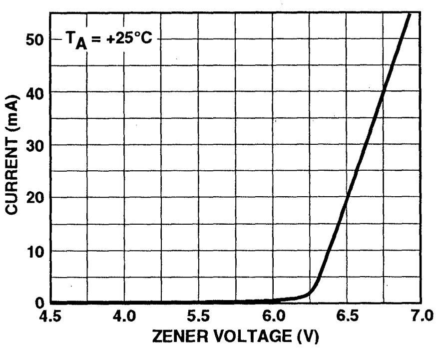


Output Resistance vs Temperature

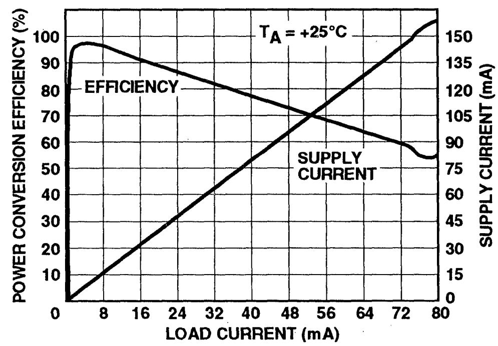


TYPICAL CHARACTERISTICS CURVES (Cont.)

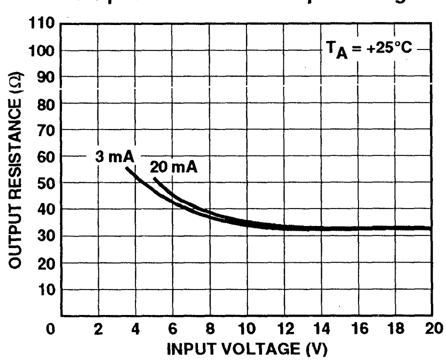
Current vs Zener Voltage



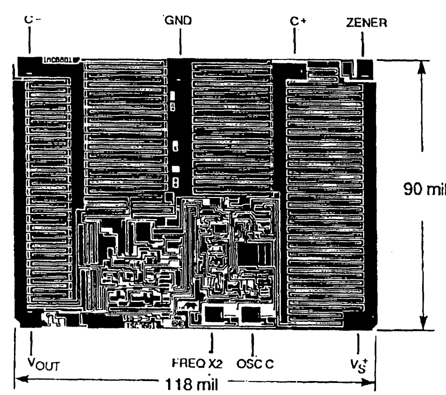
Power Conversion Efficiency vs I_{LOAD}



Output Resistance vs Input Voltage



BONDING DIAGRAM



Section 6

Power MOSFET, Motor and PIN Drivers

6

TELEDYNE COMPONENTS

HIGH SPEED PIN DRIVER

FEATURES

- **Tristateable output**
- **Dual inputs**
- **Wide input voltage range**
- **Short-circuit protected**

APPLICATIONS

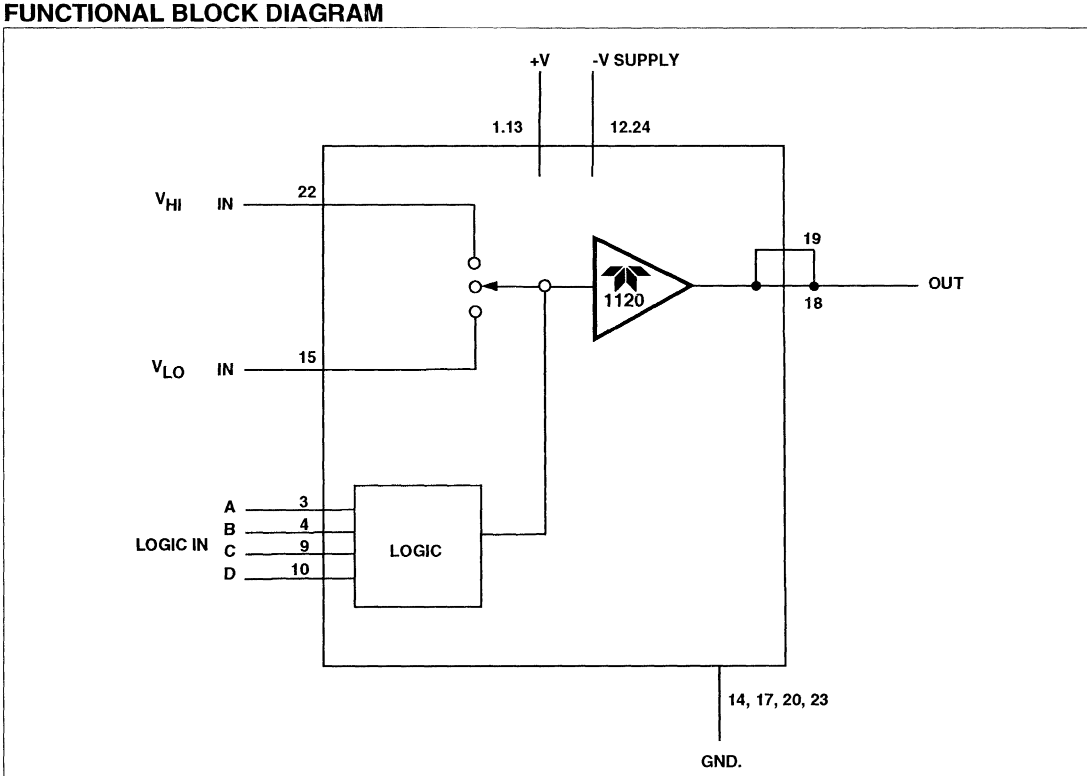
- **Mixed signal test systems**
- **Instrumentation**

GENERAL DESCRIPTION

The 1120 is a high speed pin driver for use in mixed signal test systems. Typical swing is 20ns rise/fall time for 10V step. This device features two logic-selectable inputs, both having unity gain. The output, with short-circuit current limiting, can also be configured for a tristate condition for testing I/O devices.

The 1120 pin driver is available in a 24-pin ceramic package and is specified for operation over the 0°C to +70°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

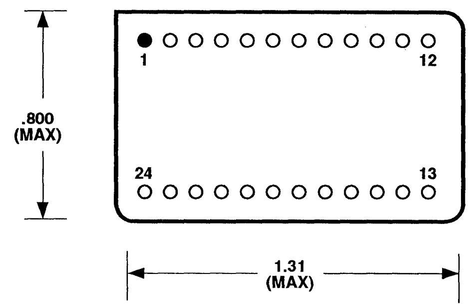


1120

PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	+24V Supply	24	-24V Supply
2	NC	23	GND
3	INPUT A	22	V_{HI} INPUT
4	INPUT B	21	NC
5	NC	20	GND
6	NC	19	OUT
7	NC	18	OUT
8	NC	17	GND
9	INPUT C	16	NC
10	INPUT D	15	V_{LO} INPUT
11	NC	14	GND
12	-24V Supply	13	+24V Supply

NC = No internal connection



ELECTRICAL CHARACTERISTICS: T_C = +25°C, $\pm V_{CC}$ = ±24V, unless otherwise indicated.

Parameter	Min	Max	Unit
VHI Offset 1,2,3	0.4	0.7	V
VLO Offset 1,2,3	0.4	0.7	V
VHI Clamp Current	—	20	mA
VLO Clamp Current	—	20	mA
VHI Output Current	30	—	mA
VLO Output Current	30	—	mA
Tristate Impedance	15	—	Mohms
+ICC	—	50	mA
-ICC	—	50	mA

LOGIC DIAGRAM:

Input A	Input B	Input C	Input D	Output
L	H	L	H	V HI IN
H	L	H	L	V LO IN
H	L	L	H	TRI STATE
L	H	H	L	NOT ALLOWED

H = ECL "1", L = ECL "0"

TELEDYNE COMPONENTS

TC1426
TC1427
TC1428

1.2A DUAL HIGH-SPEED MOSFET DRIVERS

FEATURES

- Low Cost
- Latch-Up Protected: Will Withstand 500 mA Reverse Output Current
- ESD Protected .... ±2 kV
- High Peak Output Current .... 1.2A Peak
- High Capacitive Load Drive Capability .... 1000 pF in 38 ns
- Wide Operating Range .... 4.5V to 16V
- Low Delay Time .... 75 ns Max
- Logic Input Threshold Independent of Supply Voltage
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}
- Low Output Impedance 8Ω

APPLICATIONS

- Power MOSFET Drivers
- Switched Mode Power Supplies
- Pulse Transformer Drive
- Small Motor Controls
- Print Head Drive

GENERAL DESCRIPTION

The TC1426/27/28 are a family of 1.2A dual high-speed drivers. They are ideal for high-volume OEM manufacturers, with latch-up protection, ESD protection, and a proprietary molding compound for high reliability. CMOS fabrication is used for low power consumption and high efficiency.

These devices are fabricated using an epitaxial layer to effectively short out the intrinsic parasitic transistor responsible for CMOS latch-up. They incorporate a number of other design and process refinements to increase their long-term reliability.

The TC1426 is compatible with the bipolar DS0026, but only draws 1/5 of the quiescent current. The TC1426/27/28 are also compatible with the TC426/27/28, but with 1.2A peak output current rather than the 1.5A of theTC426/27/28 devices.

The high-input impedance TC1426/27/28 drivers are CMOS/TTL input-compatible, do not require the speed-up needed by the bipolar devices, and can be directly driven by most PWM ICs.

This family of devices is available in inverting and non-inverting versions. Specifications have been optimized to achieve low-cost and high-performance devices, well-suited for the high-volume manufacturer.

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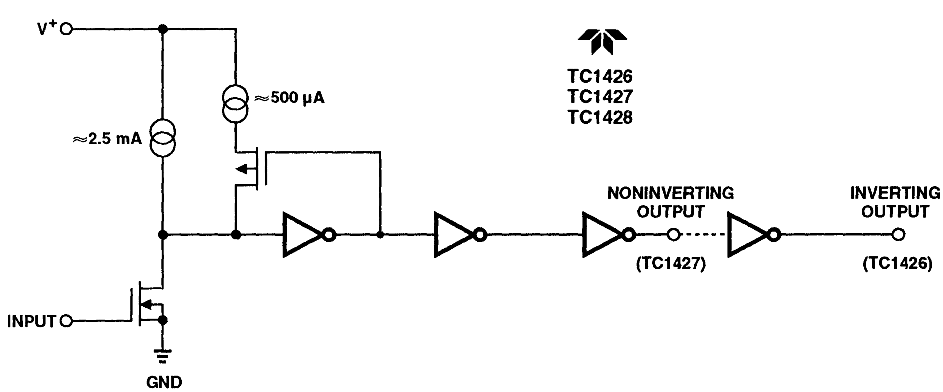
FUNCTIONAL DIAGRAM



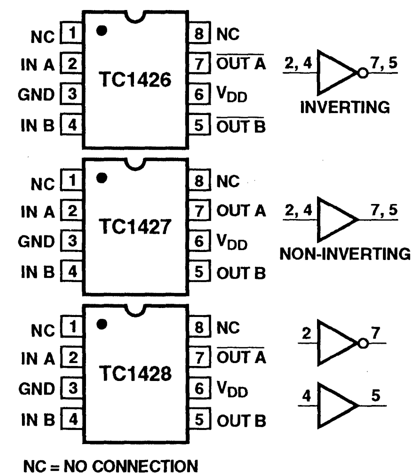
NOTE: TC1428 has one inverting and one noninverting driver. Ground any unused driver input.

TC1426
TC1427
TC1428

ORDERING INFORMATION

Part No.	Package	Configuration	Range
TC1426COA	8-Pin SO	Inverting	0°C to +70°C
TC1426CPA	8-Pin Plastic DIP	Inverting	0°C to +70°C
TC1426EPA	8-Pin Plastic DIP	Inverting	-40°C to +85°C
TC1426EOA	8-Pin SO	Inverting	-40°C to +85°C
TC1427COA	8-Pin SO	Non-Inverting	0°C to +70°C
TC1427CPA	8-Pin Plastic DIP	Non-Inverting	0°C to +70°C
TC1427EPA	8-Pin Plastic DIP	Non-Inverting	-40°C to +85°C
TC1427EOA	8-Pin SO	Non-Inverting	-40°C to +85°C
TC1428COA	8-Pin SO	Inverting and Non-Inverting	0°C to +70°C
TC1428CPA	8-Pin Plastic DIP	Inverting and Non-Inverting	0°C to +70°C
TC1428EPA	8-Pin Plastic DIP	Inverting and Non-Inverting	-40°C to +85°C
TC1428.EOA	8-Pin SO	Inverting and Non-Inverting	-40°C to +85°C

PIN CONFIGURATIONS



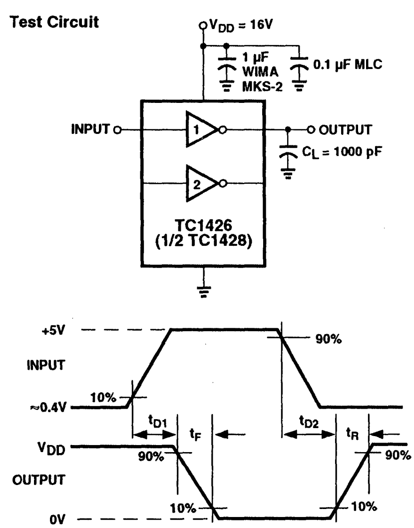


Figure 1. Inverting Driver Switching Time

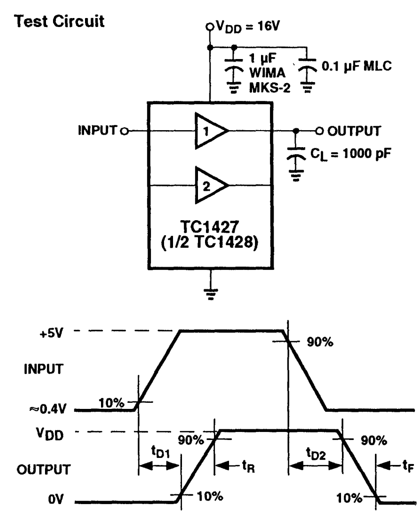


Figure 2. Non-Inverting Driver Switching Time

1.2A DUAL HIGH-SPEED MOSFET DRIVERS

TC1426
TC1427
TC1428

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Power Dissipation
- Plastic DIP 1W
- SOIC .... 500 mW

Derating Factor
- Plastic DIP .... 8 mW/°C
- SOIC .... 4 mW/°C

Supply Voltage 18V
Input Voltage, Any Terminal .... V_S + 0.3V to GND –0.3V
Operating Temperature: C Version .... 0°C to +70°C
: E Version .... -40°C to +85°C
Maximum Chip Temperature .... +150°C
Storage Temperature .... +65°C to +160°C
Lead Temperature (10 sec) .... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated inthe operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6

ELECTRICAL CHARACTERISTICS (T_A = 25°C with 4.5V ≤ $V_{DD}{}^+$ ≤ 16V unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, Input Voltage		3	—	—	V
V_{IL}	Logic 0, Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–1	—	1	µA
Output						
V_{OH}	High Output Voltage	Test Figures 1 and 2	V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage	Test Figures 1 and 2	—	—	0.025	V
R_O	Output Resistance	V_{IN} = 0.8V I_{OUT} = 10 mA, V_{DD} = 16V	—	12	18	Ω
		V_{IN} = 3V I_{OUT} = 10 mA, V_{DD} = 16V	—	8	12	Ω
I_{PK}	Peak Output Current		—	1.2	—	A
I	Latch-Up Current	Withstand Reverse Current	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Test Figures 1 and 2	—	—	35	ns
t_F	Fall Time	Test Figures 1 and 2	—	—	25	ns
t_{D1}	Delay Time	Test Figures 1 and 2	—	—	75	ns
t_{D2}	Delay Time	Test Figures 1 and 2	—	—	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	9	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.5	mA

Note: 1. Switching times guaranteed by design.

TC1426
TC1427
TC1428

ELECTRICAL CHARACTERISTICS

(Over operating temperature range with $4.5V \leq V_{DD}^{+} \leq 16V$ unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, Input Voltage		3	—	—	V
V_{IL}	Logic 0, Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–10	—	10	µA
Output						
V_{OH}	High Output Voltage	Test Figures 1 and 2	V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage	Test Figures 1 and 2	—	—	0.025	V
R_O	Output Resistance	$V_{IN} = 0.8V$ $I_{OUT} = 10$ mA, $V_{DD} = 16V$	—	15	23	Ω
		$V_{IN} = 3V$ $I_{OUT} = 10$ mA, $V_{DD} = 16V$	—	10	18	Ω
I	Latch-Up Current	Withstand Reverse Current	>500	—	—	mA
Switching Time						
t_R	Rise Time	Test Figures 1 and 2	—	—	60	ns
t_F	Fall Time	Test Figures 1 and 2	—	—	40	ns
t_{D1}	Delay Time	Test Figures 1 and 2	—	—	125	ns
t_{D2}	Delay Time	Test Figures 1 and 2	—	—	125	ns
Power Supply						
I_S	Power Supply Current	$V_{IN} = 3V$ (Both Inputs)	—	—	13	mA
		$V_{IN} = 0V$ (Both Inputs)	—	—	0.7	mA

SUPPLY BYPASSING

Large currents are required to charge and discharge large capacitive loads quickly. For example, charging a 1000-pF load 16V in 25 ns requires an 0.8A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (<0.5-in.) should be used. A 1.0-µF film capacitor in parallel with one or two 0.1-µF ceramic MLC capacitors normally provides adequate bypassing.

GROUNDING

The TC1426 and TC1428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

INPUT STAGE

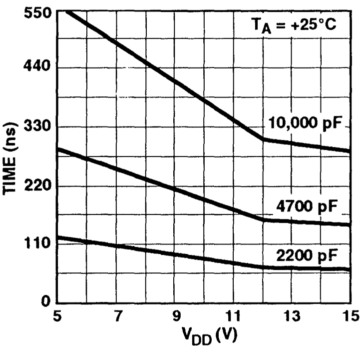
The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic "1" input, the maximum quiescent supply current is 9 mA. Logic "0" input level signals reduce quiescent current to 500 µA maximum. **Unused driver inputs must be connected to V_{DD} or GND**. Minimum power dissipation occurs for logic "0" inputs for the TC1426/27/28.

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making logic "1" input any voltage greater than 1.5V up to V_{DD}. Input current is less than 1 µA over this range.

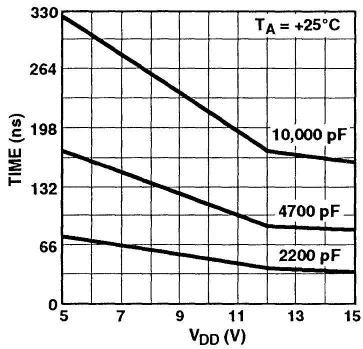
The TC1426/27/28 may be directly driven by the TL494, SG1526/27, TC38C42, TC170 and similar switch-mode power supply integrated circuits.

TYPICAL CHARACTERISTIC CURVES

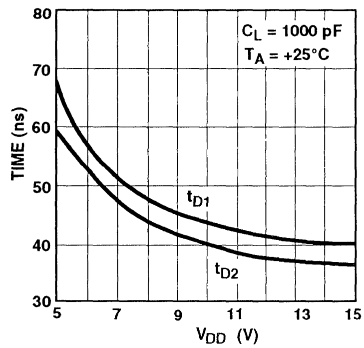
Rise Time vs Supply Voltage



Fall Time vs Supply Voltage



Delay Time vs Supply Voltage



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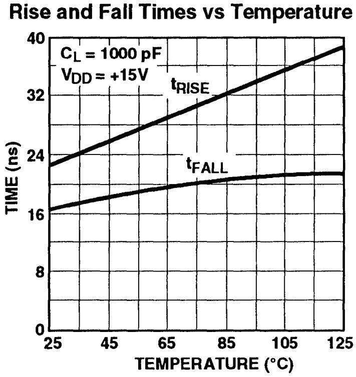
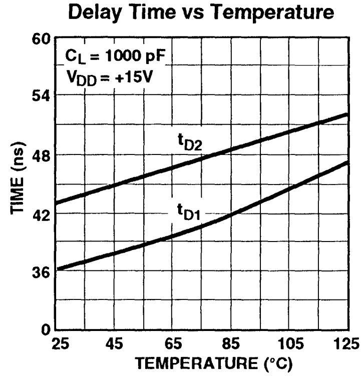
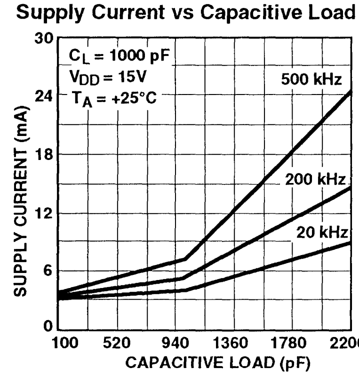
Rise and Fall Times vs Temperature



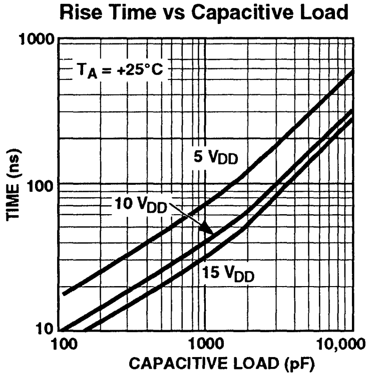
Delay Time vs Temperature



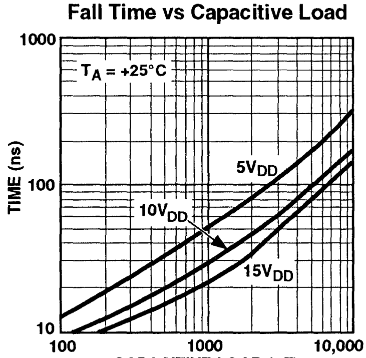
Supply Current vs Capacitive Load



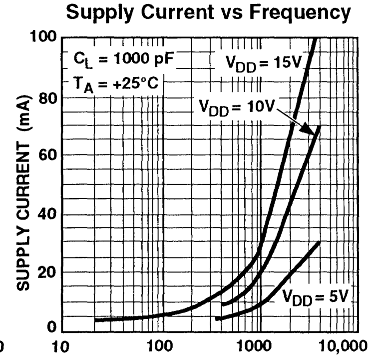
Rise Time vs Capacitive Load



Fall Time vs Capacitive Load



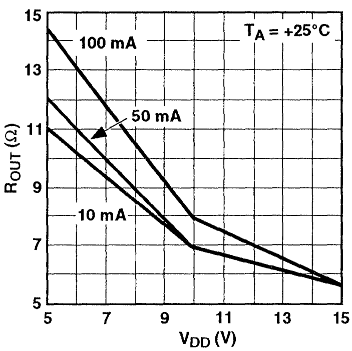
Supply Current vs Frequency



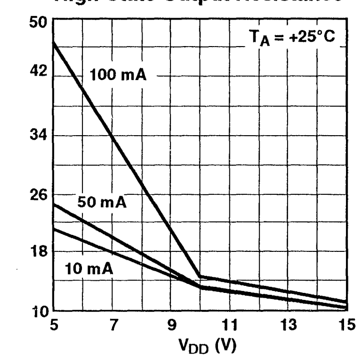
TC1426
TC1427
TC1428

TYPICAL CHARACTERISTIC CURVES (Cont.)

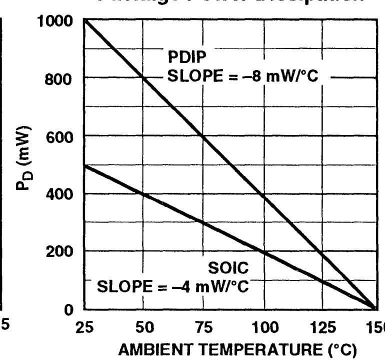
Low-State Output Resistance



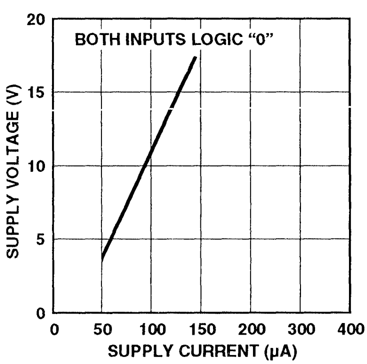
High-State Output Resistance



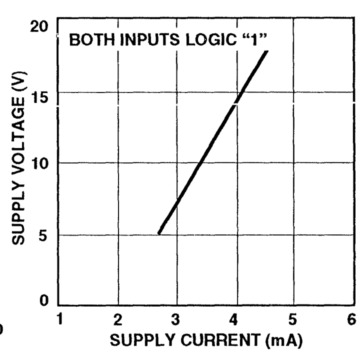
Package Power Dissipation



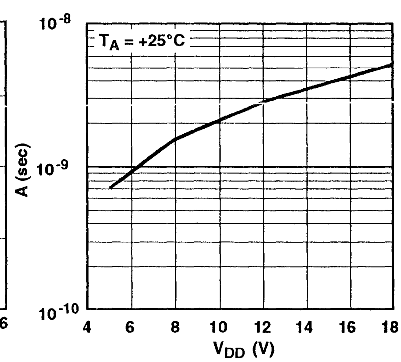
Quiescent Power Supply Current vs Supply Voltage



Quiescent Power Supply Current vs Supply Voltage



Crossover Energy Loss



TELEDYNE COMPONENTS

TC426
TC427
TC428

DUAL HIGH-SPEED POWER MOSFET DRIVERS

FEATURES

- **High-Speed Switching (C_L = 1000 pF) ....30 ns**
- **High Peak Output Current 1.5A**
- **High Output Voltage Swing ....V_{DD}–25 mV**
  GND+25 mV
- **Low Input Current (Logic "0" or "1") ....1 µA**
- **TTL/CMOS Input Compatible**
- **Available in Inverting and Noninverting Configurations**
- **Wide Operating Supply Voltage ....4.5V to 18V**
- **Current Consumption**
  — Inputs Low ....0.4 mA
  — Inputs High ....8 mA
- **Single Supply Operation**
- **Low Output Impedance..6Ω**
- **Pinout Equivalent of DS0026 and MMH0026**
- **Latch-Up Resistant: Withstands >500 mA Reverse Current**
- **ESD Protected ....2 kV**

GENERAL DESCRIPTION

The TC426/TC427/TC428 are dual CMOS high-speed drivers. A TTL/CMOS input voltage level is translated into an output voltage level swing equaling the supply. The CMOS output will be within 25 mV of ground or positive supply. Bipolar designs are capable of swinging only within 1V of the supply.

The low impedance, high-current driver outputs will swing a 1000 pF load 18V in 30 ns. The unique current and voltage drive qualities make the TC426/TC427/TC428 ideal power MOSFET drivers, line drivers, and DC-to-DC converter building blocks.

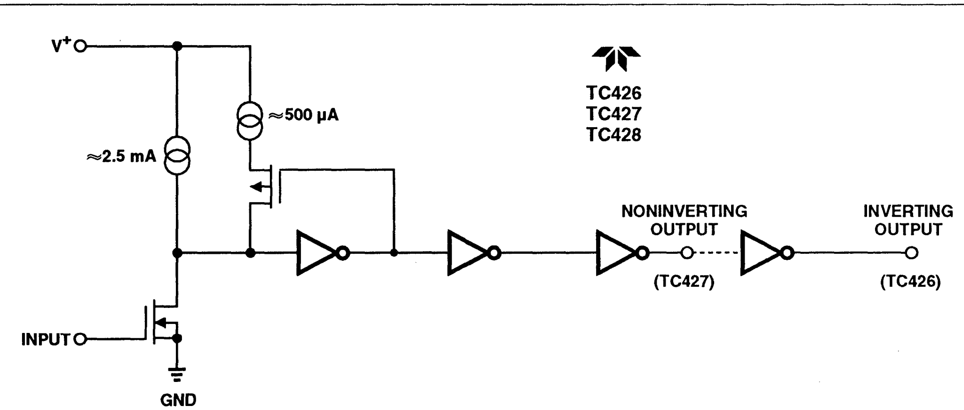
Input logic signals may equal the power supply voltage. Input current is a low 1 µA, making direct interface to CMOS/bipolar switch-mode power supply control ICs possible, as well as open-collector analog comparators.

Quiescent power supply current is 8 mA maximum. The TC426 requires 1/5 the current of the pin-compatible bipolar DS0026 device. This is important in DC-to-DC converter applications with power efficiency constraints and high-frequency switch-mode power supply applications. Quiescent current is typically 6 mA when driving a 1000 pF load 18V at 100 kHz.

The inverting TC426 driver is pin-compatible with the bipolar DS0026 and MMH0026 devices. The TC427 is noninverting; the TC428 contains an inverting and noninverting driver.

6

FUNCTIONAL DIAGRAM



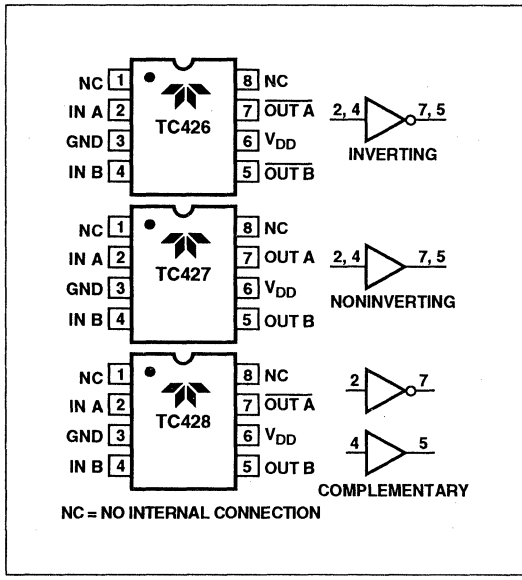
NOTE: TC428 has one inverting and one noninverting driver. Ground any unused driver input.

TC426
TC427
TC428

ORDERING INFORMATION

Part No.	Package	Configuration	Temperature Range
TC426CPA	8-Pin PDIP	Inverting	0°C to +70°C
TC427CPA	8-Pin PDIP	Noninverting	0°C to +70°C
TC428CPA	8-Pin PDIP	Complementary	0°C to +70°C
TC426COA	8-Pin SOIC	Inverting	0°C to +70°C
TC427COA	8-Pin SOIC	Noninverting	0°C to +70°C
TC428COA	8-Pin SOIC	Complementary	0°C to +70°C
TC426IJA	8-Pin CerDIP	Inverting	–25°C to +85°C
TC427IJA	8-Pin CerDIP	Noninverting	–25°C to +85°C
TC428IJA	8-Pin CerDIP	Complementary	–25°C to +85°C
TC426EOA	8-Pin SOIC	Inverting	–40°C to +85°C
TC427EOA	8-Pin SOIC	Noninverting	–40°C to +85°C
TC428EOA	8-Pin SOIC	Complementary	–40°C to +85°C
TC426MJA	8-Pin CerDIP	Inverting	–55°C to +125°C
TC427MJA	8-Pin CerDIP	Noninverting	–55°C to +125°C
TC428MJA	8-Pin CerDIP	Complementary	–55°C to +125°C

PIN CONFIGURATIONS (DIP and SO)



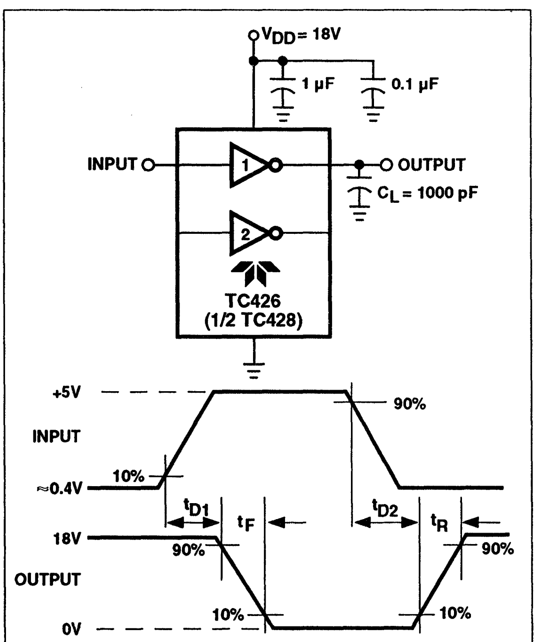


Figure 1. Inverting Driver Switching Time Test Circuit

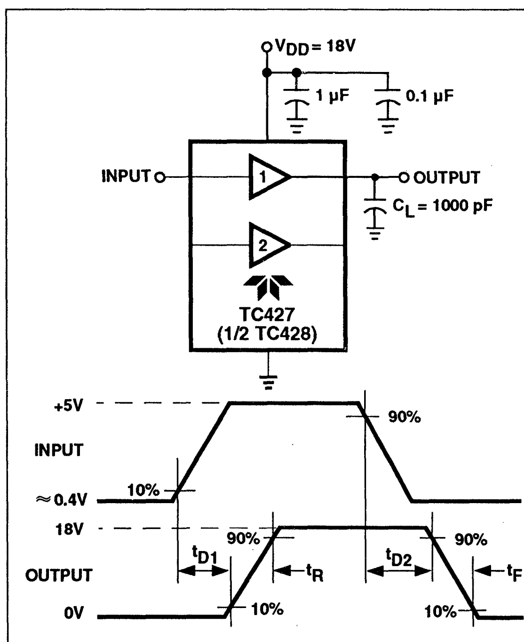


Figure 2. Noninverting Driver Switching Time Test Circuit

DUAL HIGH-SPEED POWER MOSFET DRIVERS

TC426 TC427 TC428

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +20V
Input Voltage, Any Terminal .... V_{DD}+0.3V to GND –0.3V
Power Dissipation
  Plastic .... 1000 mW
  CerDIP .... 800 mW
  SOIC .... 500 mW
Derating Factor
  Plastic .... 8 mW/°C
  CerDIP .... 6.4 mW/°C
  SOIC .... 4 mW/°C
Operating Temperature Range
  C Version .... 0°C to +70°C
  I Version .... –25°C to +85°C
  E Version .... –40°C to +85°C
  M Version .... –55°C to +125°C

Maximum Chip Temperature .... +150°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

6

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0, Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_{OH}	High Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V	—	10	15	Ω
R_{OL}	Low Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V	—	6	10	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
Switching Time (Note 1)						
t_R	Rise Time	Test Figure 1	—	—	30	ns
t_F	Fall Time	Test Figure 1	—	—	20	ns
t_{D1}	Delay Time	Test Figure 1	—	—	50	ns
t_{D2}	Delay Time	Test Figure 1	—	—	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	8	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.4	mA

ELECTRICAL CHARACTERISTICS:

Over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0, Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	—	10	μA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_{OH}	High Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V	—	13	20	Ω
R_{OL}	Low Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V	—	8	15	W
Switching Time (Note 1)						
t_R	Rise Time	Test Figure 1	—	—	60	ns
t_F	Fall Time	Test Figure 1	—	—	40	ns
t_{D1}	Delay Time	Test Figure 1	—	—	75	ns
t_{D2}	Delay Time	Test Figure 1	—	—	120	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	12	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.6	mA

NOTE: 1. Switching times guaranteed by design.

SUPPLY BYPASSING

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 1000-pF load 18V in 25 ns requires an 0.8A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (<0.5 in.) should be used. A 1 μF film capacitor in parallel with one or two 0.1 μF ceramic disk capacitors normally provides adequate bypassing.

GROUNDING

The TC426 and TC428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

INPUT STAGE

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic "1" input, the maximum quiescent supply current is 8 mA. Logic "0" input level signals reduce quiescent current to 0.4 mA maximum. Minimum power dissipation occurs for logic "0" inputs for the TC426/427/428. **Unused driver inputs must be connected to V_{DD} or GND.**

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making the device TTL compatible over the 4.5V to 18V supply operating range. Input current is less than 1 μA over this range.

The TC426/427/428 may be directly driven by the TL494, SG1526/1527, SG1524, SE5560, and similar switch-mode power supply integrated circuits.

POWER DISSIPATION

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations.

The TC426/427/428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8 mA compared to the DS0026 40 mA specification. For a 15V supply, power dissipation is typically 40 mW.

Two other power dissipation components are:

- Output stage AC and DC load power.
- Transition state power.

Output stage power is:

$P_o = P_{DC} + PAC$

$\quad = V_o\,(I_{DC}) + f\,C_L\,V_S^2$

Where:

V_o = DC output voltage
I_{DC} = DC output load current
f = Switching frequency
V_s = Supply voltage

In power MOSFET drive applications the P_{DC} term is negligible. MOSFET power transistors are high impedance, capacitive input devices. In applications where resistive loads or relays are driven, the P_{DC} component will normally dominate.

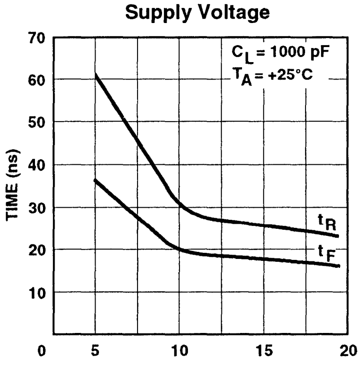
The magnitude of P_{AC} is readily estimated for several cases:

A.		B.	
1. f	= 20kHZ	1. f	= 200 kHz
2. C_L	=1000 pf	2. C_L	=1000 pf
3. Vs	= 18V	3. VS	=15V
4. P_{AC}	= 65 mW	4. P_{AC}	= 45 mW

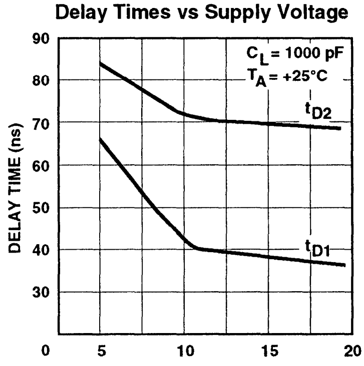
During output level state changes, a current surge will flow through the series connected N and P channel output MOSFETS as one device is turning "ON" while the other is turning "OFF". The current spike flows only during output transitions. The input levels should not be maintained between the logic "0" and logic "1" levels. **Unused driver inputs must be tied to ground and not be allowed to float.** Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

TYPICAL CHARACTERISTICS CURVES

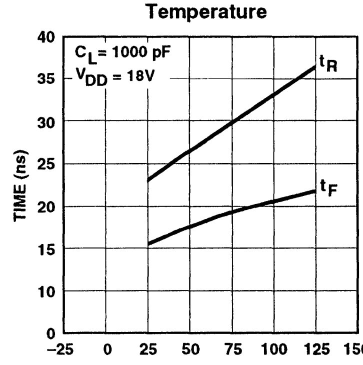
Rise and Fall Times vs Supply Voltage



Delay Times vs Supply Voltage

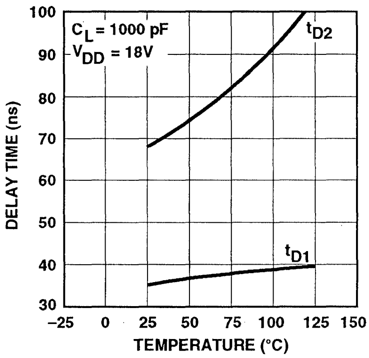


Rise and Fall Times vs Temperature

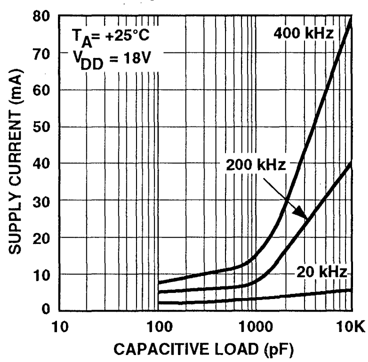


TYPICAL CHARACTERISTICS CURVES (Cont.)

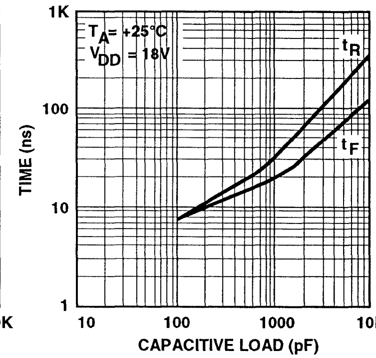
Delay Times vs Temperature



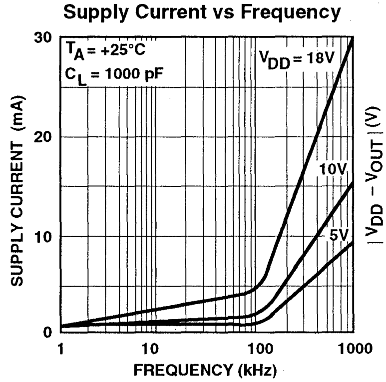
Supply Current vs Capacitive Load



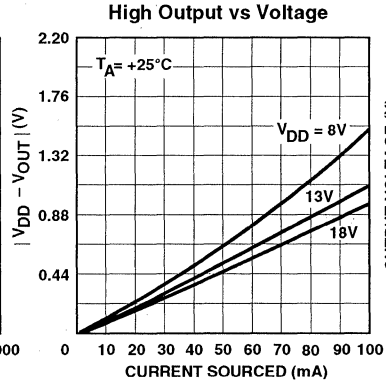
Rise and Fall Times vs Capacitive Load



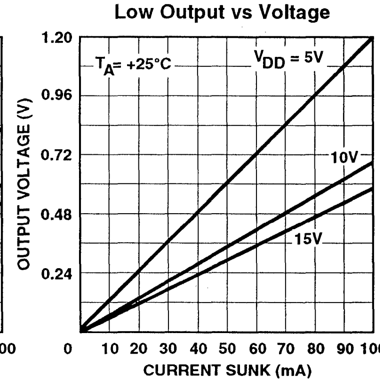
Supply Current vs Frequency



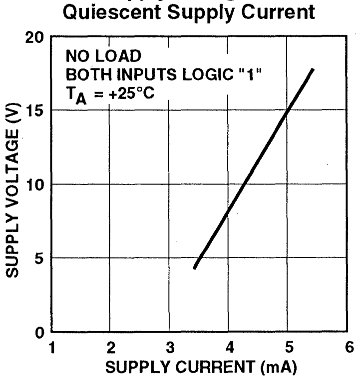
High Output vs Voltage



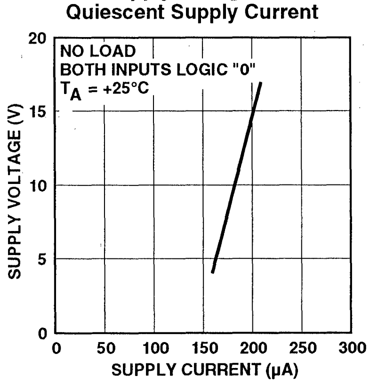
Low Output vs Voltage



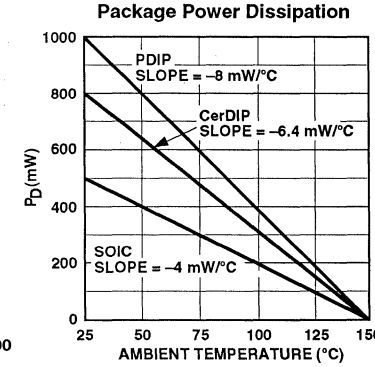
Supply Voltage vs Quiescent Supply Current



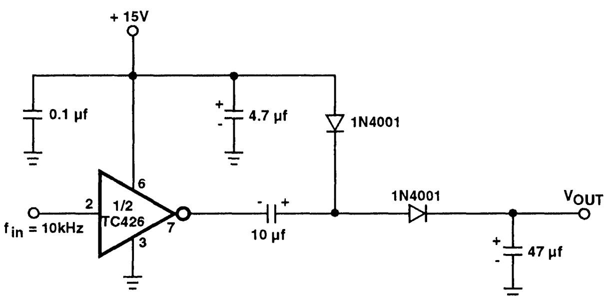
Supply Voltage vs Quiescent Supply Current



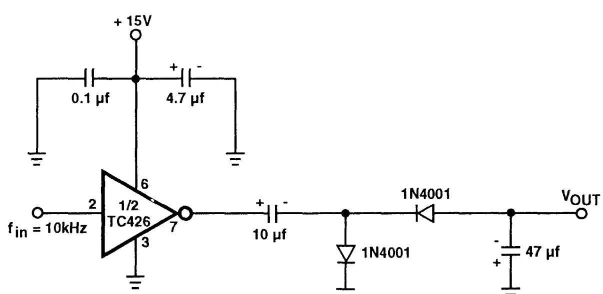
Package Power Dissipation

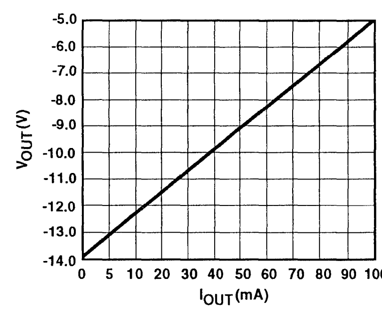


VOLTAGE DOUBLER



VOLTAGE INVERTER





6

NOTES

![TELEDYNE COMPONENTS]

TELEDYNE COMPONENTS

SINGLE HIGH-SPEED, CMOS POWER MOSFET DRIVER

FEATURES

- High Peak Output Current 6A
- Wide Operating Range .... 7V to 18V
- High-Impedance CMOS Logic Input
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - — With Logic 1 Input .... 5 mA Max
  - — With Logic 0 Input .... 0.5 mA Max
- Output Voltage Swing Within 25 mV of Ground or V_{DD}
- Low Delay Time .... 75 ns Max
- High Capacitive Load Drive Capability
  - — t_{RISE}, t_{FALL} = 35 ns Max With C_{LOAD} = 2500 pF

APPLICATIONS

- Switch-Mode Power Supplies
- CCD Drivers
- Pulse Transformer Drive
- Class D Switching Amplifiers

GENERAL DESCRIPTION

The TC429 is a high-speed, single CMOS-level translator and driver. Designed specifically to drive highly capacitive power MOSFET gates, the TC429 features 2.5Ω output impedance and 6A peak output current drive.

A 2500 pF capacitive load will be driven 18V in 25 ns. Delay time through the device is 60 ns. The rapid switching times with large capacitive loads minimize MOSFET transition power loss.

A TTL/CMOS input logic level is translated into an output voltage swing that equals the supply and will swing to within 25 mV of ground or V_{DD}. Input voltage swing may equal the supply. Logic input current is under 10 µA, making direct interface to CMOS/bipolar switch-mode power supply controllers easy. Input "speed-up" capacitors are not required.

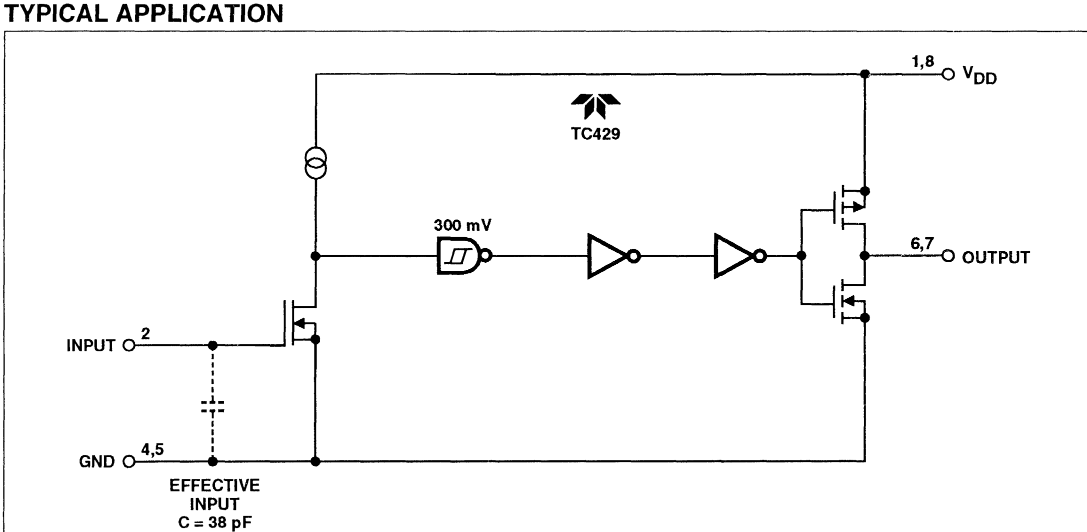
The CMOS design minimizes quiescent power supply current. With a logic 1 input, power supply current is 5 mA maximum and decreases to 0.5 mA for logic 0 inputs.

For dual devices, see the TC426/TC427/TC428 data sheet.

For noninverting applications, or applications requiring latch-up protection, see the TC4420/TC4429 data sheet.

6

TYPICAL APPLICATION



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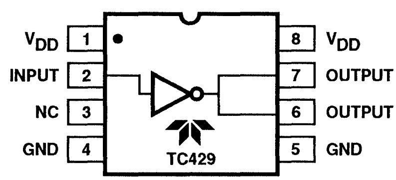
ORDERING INFORMATION

Part No.	Package	Temperature Range
TC429CPA	8-Pin Plastic DIP	0°C to +70°C
TC429IJA	8-Pin CerDIP	–25°C to +85°C
TC429EPA	8-Pin Plastic DIP	–40°C to +85°C
TC429MJA	8-Pin CerDIP	–55°C to +125°C
TC429Y	Chip	+25°C

PIN CONFIGURATION



NC = NO INTERNAL CONNECTION

NOTE: Duplicate pins must both be connected for proper operation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +20V
Input Voltage, Any Terminal ...... V_{DD} +0.3V to GND –0.3V
Power Dissipation
  Plastic .... 500 mW
  CerDIP .... 800 mW
Derating Factors
  Plastic .... 5.6 mW/°C Above 36°C
  CerDIP .... 6 mW/°C
Operating Temperature Range
  C Version .... 0°C to +70°C
  I Version .... –25°C to +85°C
  E Version .... –40°C to +85°C
  M Version .... –55°C to +125°C
Maximum Chip Temperature .... +150°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 7V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0, Low Input Voltage		—	1.3	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{IN} = 0.8V	—	1.8	2.5	Ω
		I_{OUT} = 10 mA, V_{DD} = 18V				
		V_{IN} = 2.4V	—	1.5	2.5	Ω
		I_{OUT} = 10 mA, V_{DD} = 18V				
I_{PK}	Peak Output Current	V_{DD} = 18V (See Figure 3)	—	6	—	A
Switching Time (note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	23	35	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1	—	53	75	ns
t_{D2}	Delay Time	Figure 1	—	60	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	3.5	5	mA
		V_{IN} = 0V	—	0.3	0.5	mA

NOTES: 1. Switching times guaranteed by design.

SINGLE HIGH-SPEED, CMOS POWER MOSFET DRIVER

ELECTRICAL CHARACTERISTICS: Over operating temperature with 7V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0, Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{IN} = 0.8V, I_{OUT} = 10 mA, V_{DD} = 18V	—	—	5	Ω
		V_{IN} = 2.4V, I_{OUT} = 10 mA, V_{DD} = 18V	—	—	5	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	—	70	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	—	70	ns
t_{D1}	Delay Time	Figure 1	—	—	100	ns
t_{D2}	Delay Time	Figure 1	—	—	120	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	—	12	mA
		V_{IN} = 0V	—	—	1	mA

NOTE: 1. Switching times guaranteed by design.

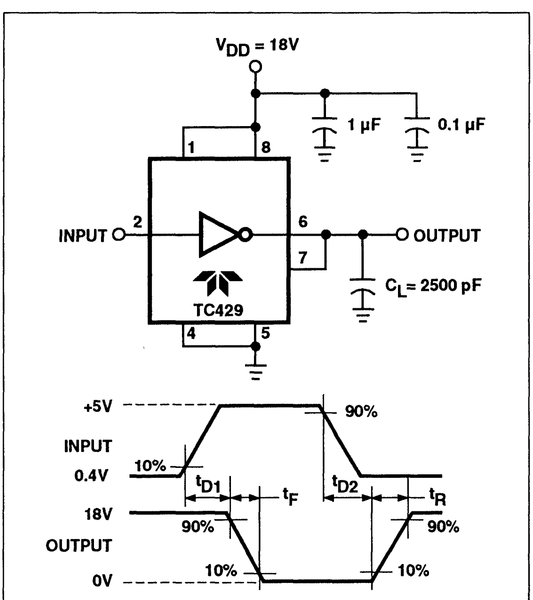
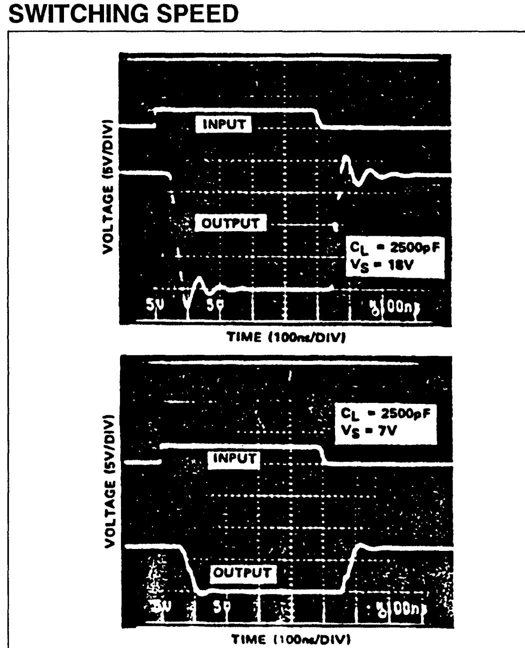


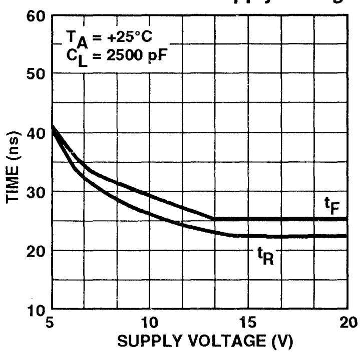
Figure 1 Inverting Driver Switching Time Test Circuit

SWITCHING SPEED

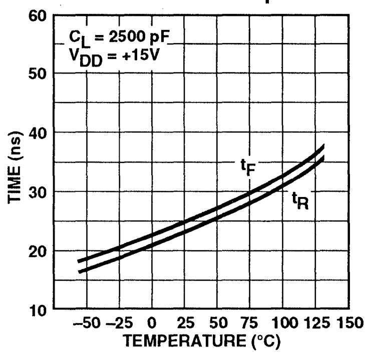


TYPICAL CHARACTERISTICS CURVES

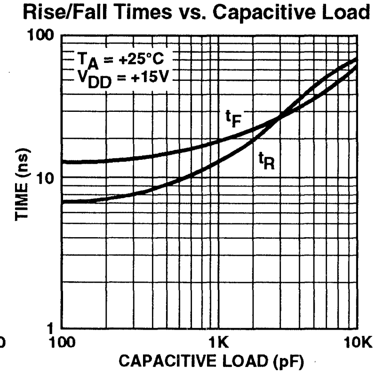
Rise/Fall Times vs. Supply Voltage



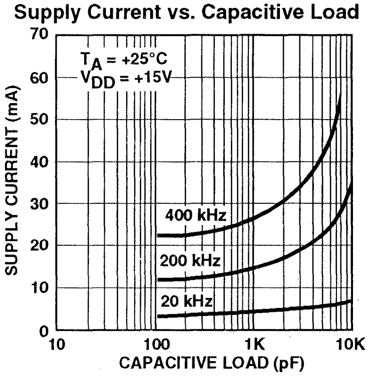
Rise/Fall Times vs. Temperature



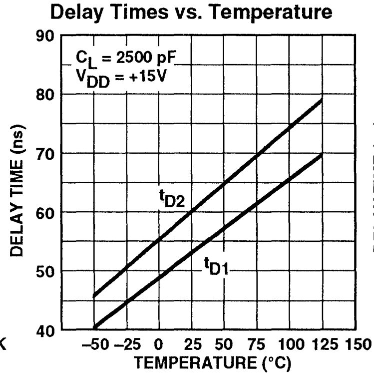
Rise/Fall Times vs. Capacitive Load



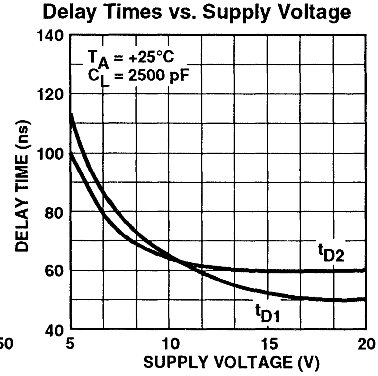
Supply Current vs. Capacitive Load



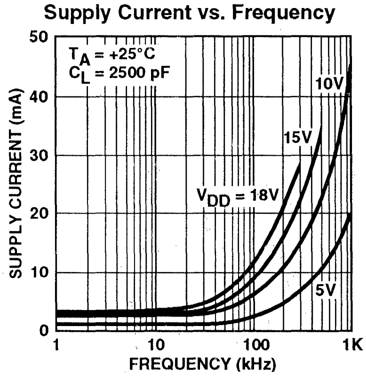
Delay Times vs. Temperature



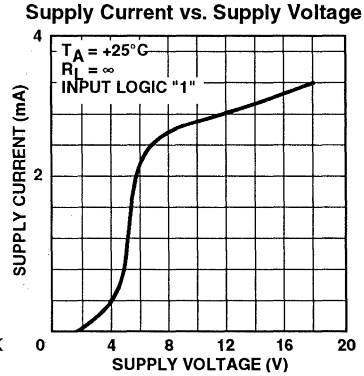
Delay Times vs. Supply Voltage



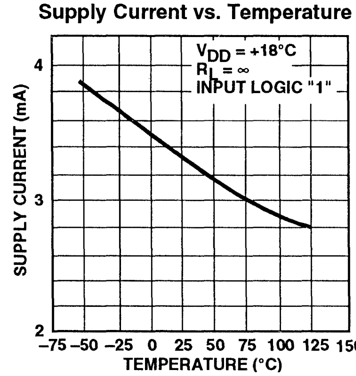
Supply Current vs. Frequency



Supply Current vs. Supply Voltage

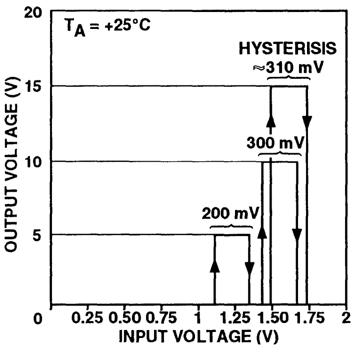


Supply Current vs. Temperature

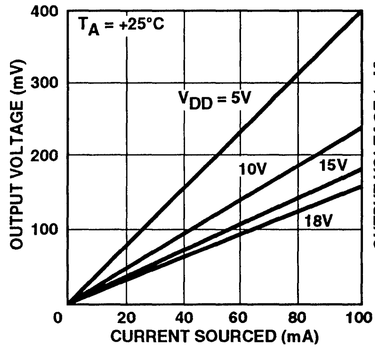


TYPICAL CHARACTERISTICS CURVES (Cont.)

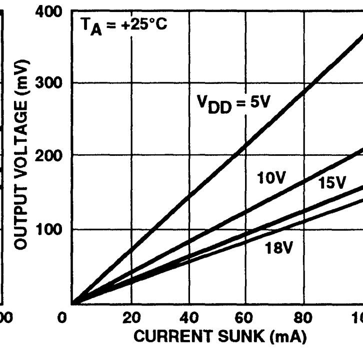
Voltage Transfer Characteristics



High Output Voltage vs. Current



Low Output Voltage vs. Current



SUPPLY BYPASSING

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500 pF load 18V in 25 ns requires a 1.8A current from the device's power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (<0.5 in.) should be used. A 1 µF film capacitor in parallel with one or two 0.1 µF ceramic disk capacitors normally provides adequate bypassing.

GROUNDING

The high-current capability of the TC429 demands careful PC board layout for best performance. Since the TC429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. The feedback is especially noticeable with slow rise-time inputs, such as those produced by an open-collector output with resistor pull-up. The TC429 input structure includes about 300 mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 2 shows the feedback effect in detail. As the TC429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the TC429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillations may result.

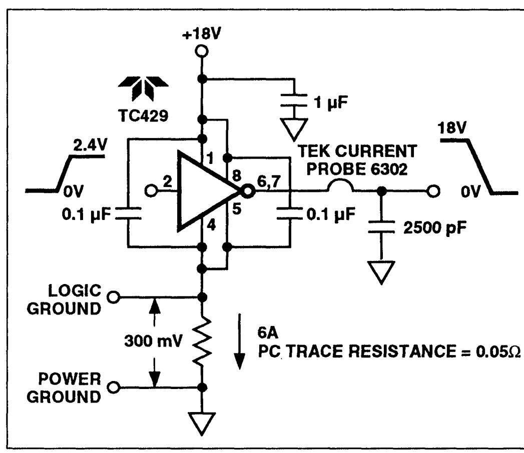


Figure 2 Switching Time Degradation Due to Negative Feedback

To ensure optimum device performance, separate ground traces should be provided for the logic and power connections. Connecting logic ground directly to the TC429 GND pins ensures full logic drive to the input and fast output switching. Both GND pins should be connected to power ground.

INPUT STAGE

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 3 mA current source load. With a logic "1" input, the maximum quiescent supply current is 5 mA. Logic "0" input level signals reduce quiescent current to 500 µA maximum.

The TC429 input is designed to provide 300 mV of hysteresis, providing clean transitions and minimizing output stage current spiking when changing states. Input voltage levels are approximately 1.5V, making the device TTL compatible over the 7V to 18V operating supply range. Input current is less than 10 μA over this range.

The TC429 can be directly driven by TL494, SG1526/1527, SG1524, SE5560 or similar switch-mode power supply integrated circuits. By off-loading the power-driving duties to the TC429, the power supply controller can operate at lower dissipation, improving performance and reliability.

POWER DISSIPATION

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as the 4000 and 74C have outputs that can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The TC429, however, can source or sink several amperes and drive large capacitive loads at high frequency. The packgae power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations. Table I lists the maximum operating frequency for several power supply voltages when driving a 2500 pF load. More accurate power dissipation figures can be obtained by summing the three power sources.

Input signal duty cycle, power supply voltage, and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operation temperature is easily calculated. The 8-pin cerDIP junction-to-ambient thermal resistance is 150°C/W. At +25°C, the package is rated at 800 mW maximum dissipation. Maximum allowable chip temperature is +150°C.

Three components make up total package power dissipation:

(1) Capacitive load dissipation (P_C)
(2) Quiescent power (P_Q)
(3) Transition power (P_T)

The capacitive load-caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation is:

$$P_C = f\,C\,V_S^2,$$

where: f = Switching frequency
C = Capacitive load
V_S = Supply voltage.

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low-power dissipation mode with only 0.5 mA total current drain. Logic high signals raise the current to 5 mA maximum. The queiscent power dissipation is:

$$P_Q = V_S\,(D\,(I_H) + (1-D)\,I_L),$$

where: I_H = Quiescent current with input high (5 mA max)
I_L = Quiescent current with input low (0.5 mA max)
D = Duty cycle.

Transition power dissipation arises because the output stage N- and P-channel MOS transistors are "on" simultaneously for a very short period when the output changes. The transition package power dissipation is approximately:

$$P_T = f\,V_S\,(3\ 3\ 10^{-9}).$$

An example shows the relative magnitude for each item.

Example 1:

C = 2500 pF
V_S = 15V
D = 50%
f = 200 kHz
P_D = Package power dissipation = $P_C + P_T + P_Q$
= 113 mW + 90 mW + 26 mW
= 229 mW.

Maximum operating temperature = $T_J - \theta_{JA}\,(P_D)$
= 115°C,

where: T_J = Maximum allowable junction temperature (+150°C)
θ_{JA} = Junction-to-ambient thermal resistance (50°C/W, CerDIP).

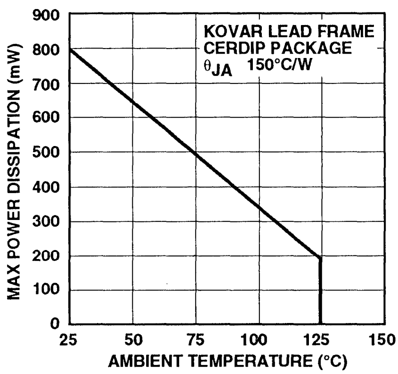
NOTE: Ambient operating temperature should not exceed +85°C for IJA devices or +125°C for MJA devices.

Table I. Maximum Operating Frequencies

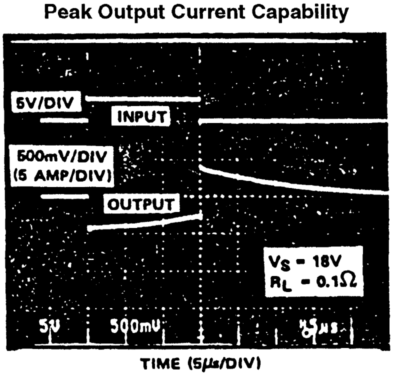
V_S	f_{Max}
18V	500 kHz
15V	700 kHz
10V	1.3 MHz
5V	>2 MHz

CONDITIONS: 1. CerDIP Package (θ_{JA} = 150°C/W)
2. T_A = +25°C
3. C_L = 2500 pF

Package Power Dissipation



Peak Output Current Capability



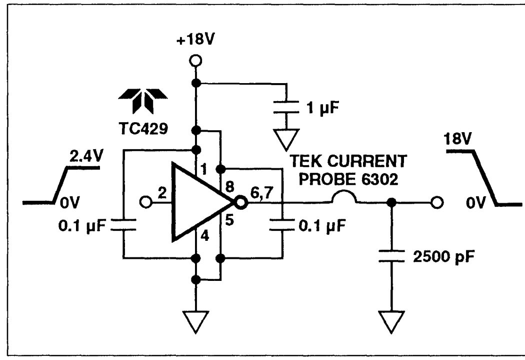
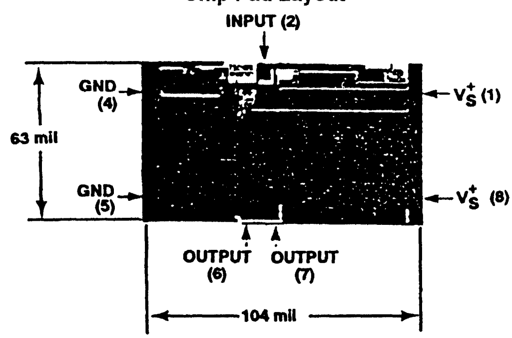


Figure 3 Peak Output Current Test Circuit

Chip Pad Layout



POWER-ON OSCILLATION

It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement. A 'quick fix' for most applications which exhibit POWER-ON OSCILLATION problems is to place approximately 10 kΩ in series with the input of the MOSFET driver.

NOTES

FAST CMOS CCD DRIVER

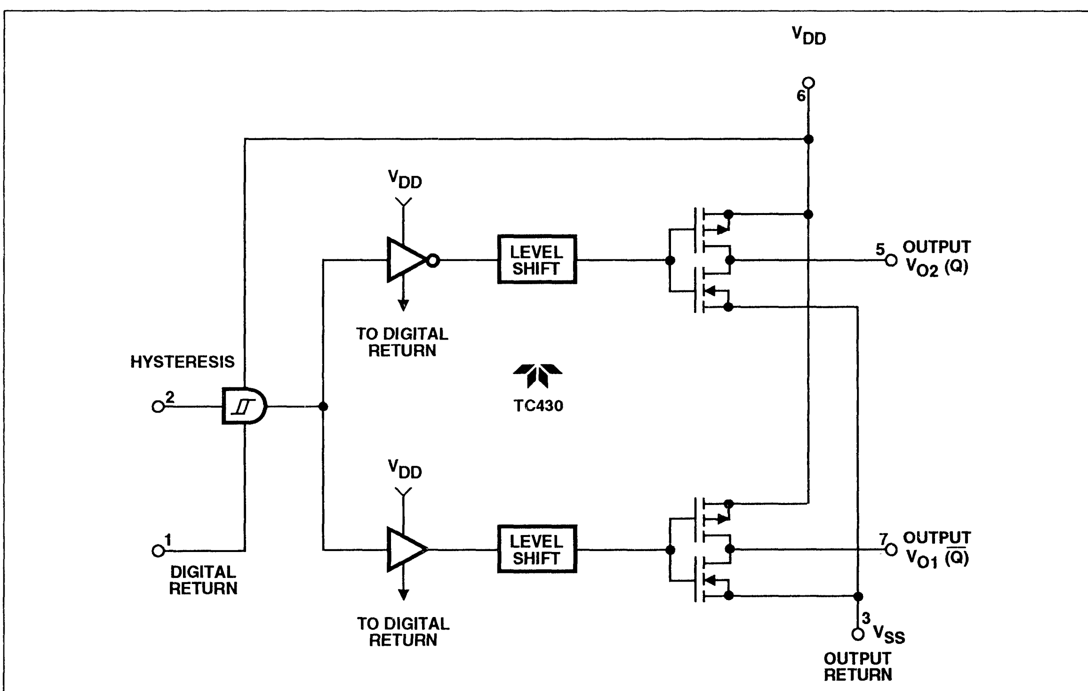
FEATURES

- Operating Range .... 4.5V ≤ ($V_{DD} - V_{SS}$) ≤ 12V
- TTL/CMOS-Compatible Inputs
- Low Delay Time .... 15 ns Typ
- Rise and Fall Times .... 2200 pF Load, 25 ns Typ
- Peak Output Current 3A
- Output Can Be Floated Below Digital Return
- Level Shifting for Split-Supply Operation
- Guaranteed Skew
- Complementary Outputs
- 10 MHz Operation With Adequate Heat Sink
- Drives 1000 pF at 4 MHz, in CerDIP With No External Heat Sink (10V $V_{DD} - V_{SS}$)
- Low Output Impedance .... 5Ω Max
- Low Quiescent Current .... 5 mA Max

APPLICATIONS

- CCD Driver
- MOSFET Driver
- Laser Diode Driver
- Differential Line Driver
- PIN Diode Driver
- Level Shifting Driver

FUNCTIONAL DIAGRAM



TC430

GENERAL DESCRIPTION

The TC430 is a super-fast CMOS power driver for driving CCDs and other loads. The TC430 operates at frequencies to 10 MHz and drives loads greater than 2200 pF. Peak current output is 3A.

The input is TTL/CMOS compatible. Digital return and output return can be at different voltages, allowing operation with output swings between positive and negative supplies without sacrificing AC performance when driven from TTL. The ability to swing negative is important when driving CCD devices.

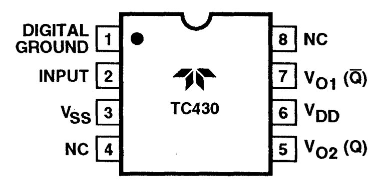
The output stages have been designed so the rising edge of one output crosses the 50% point of the transition within 5 ns of the other. This makes the TC430 ideal for driving CCDs and achieving high contrast images.

CMOS construction achieves low quiescent power (less than 5 mA at 15V and 25°C) and low input current requirements. This device requires fewer external components than bipolar devices like the DS0026 which need external speed-up capacitors.

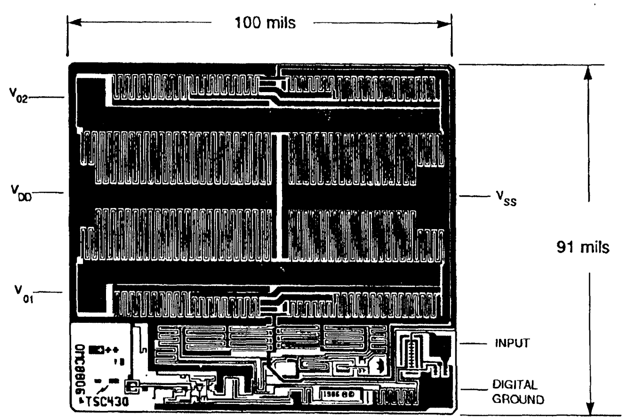
ORDERING INFORMATION

Part No.	Package	Temperature Range
TC430CPA	8-Pin Plastic	0°C to +70°C
TC430IJA	8-Pin CerDIP	–25°C to +85°C
TC430MJA	8-Pin CerDIP	–55°C to +125°C

PIN CONFIGURATION



BONDING DIAGRAM



NOTES:
1. Back of die is common to V_{DD}.
2. Bak if die is not metalized

ABSOLUTE MAXIMUM RATINGS

Power Dissipation at +25°C
Plastic .... 1000 mW
CerDIP .... 800 mW
Derating Factors
Plastic .... 8 mW/°C
CerDIP .... 6.4 mW/°C
Supply Voltage .... $V_{DD} - V_{SS} \leq 15V$
$V_{DD} - V_{DR} \leq 15V$
Input Voltage, Any Terminal .... V_{DD} +0.3V
Operating Temperature Range
M Version .... −55°C to +125°C
I Version .... −25°C to +85°C
C Version .... 0°C to +70°C
Maximum Chip Temperature .... 150°C

Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... 300°C
CerDIP $R_{\Theta\text{-}JA}$ .... 150°C/W
Plastic $R_{\Theta\text{-}JA}$ .... 125°C/W
ESD Protection 2000V

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V $\leq (V_{DD} - V_{DR}) \leq$ 12V, 4.5V $\leq (V_{DD} - V_{SS}) \leq$ 12V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Logic 1, High Input Voltage		2.4	1.6		V
V_{IL}	Logic 0, Low Input Voltage			1.3	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	−10		10	µA
V_{OH}	High Output Voltage		V_{DD}−0.025			V
V_{OL}	Low Output Voltage				V_{SS}+0.025	V
R_O	Output Resistance	V_{IN} = 0V, I_{OUT} = 10 mA, V_{SS} = 0V, V_{DD} = 12V		3	5	Ω
		V_{IN} = 3V, I_{OUT} = 10 mA, V_{SS} = 0V, V_{DD} = 12V		3	5	Ω
I_{PK}	Peak Output Current	V_{DD} = 12V		3		A
t_{SKEW1}	Output Pulse Skew	Figure 2		3	5	ns
t_{SKEW2}	Output Pulse Skew	Figure 2		3	5	ns
t_R	Rise Time	Figure 1 C_L = 2200 pF, V_{DD} = 12V		22	30	ns
t_F	Fall Time	Figure 1 C_L = 2200 pF, V_{DD} = 12V		22	30	ns
t_{D1}	Delay Time	Figure 1		18	25	ns
t_{D2}	Delay Time	Figure 1		18	25	ns
I_S	Quiescent Power Supply Current	V_{IN} = 3V, V_{DD} = 12V, V_{SS} = 0V V_{IN} = 0V, V_{DD} = 12V, V_{SS} = 0V		2.9	5 0.3	mA mA

NOTE: Switching times are guaranteed by design.

TC430

ELECTRICAL CHARACTERISTICS: $4.5V \leq (V_{DD} - V_{DR}) \leq 12V$; $4.5V \leq (V_{DD} - V_{SS}) \leq 12V$, $T_A = -55°C$ to $+125°C$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Logic 1, High Input Voltage		2.4			V
V_{IL}	Logic 0, Low Input Voltage				0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–10		10	µA
V_{OH}	High Output Voltage		V_{DD}–0.025			V
V_{OL}	Low Output Voltage				V_{SS}+0.025	V
R_O	Output Resistance	$V_{IN} = 0V$, $I_{OUT} = 10$ mA, $V_{SS} = 0V$, $V_{DD} = 12V$		4.5	7	Ω
		$V_{IN} = 3V$, $I_{OUT} = 10$ mA, $V_{SS} = 0V$, $V_{DD} = 12V$		4.5	7	Ω
I_{PK}	Peak Output Current	$V_{DD} = 12V$		3		A
t_{SKEW1}	Output Pulse Skew	Figure 2		5	10	ns
t_{SKEW2}	Output Pulse Skew	Figure 2		5	10	ns
t_R	Rise Time	Figure 1 $C_L = 2200$ pF, $V_{DD} = 12V$			40	ns
t_F	Fall Time	Figure 1 $C_L = 2200$ pF, $V_{DD} = 12V$			40	ns
t_{D1}	Delay Time	Figure 1			35	ns
t_{D2}	Delay Time	Figure 1			35	ns
I_S	Quiescent Power Supply Current	$V_{IN} = 3V$, $V_{DD} = 12V$, $V_{SS} = 0V$		5	8	mA
		$V_{IN} = 0V$, $V_{DD} = 12V$, $V_{SS} = 0V$			0.5	mA

NOTE: Switching times are guaranteed by design.

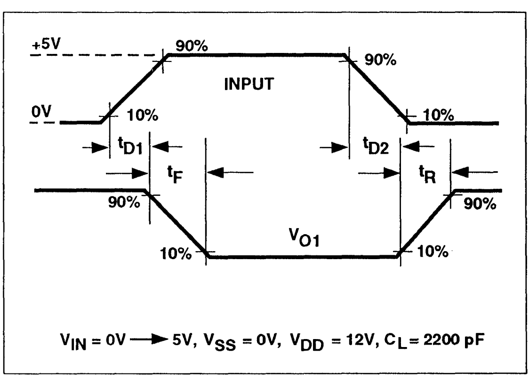


Figure 1 Driver Switching Time

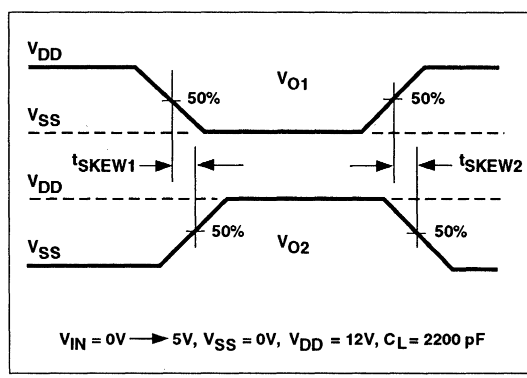
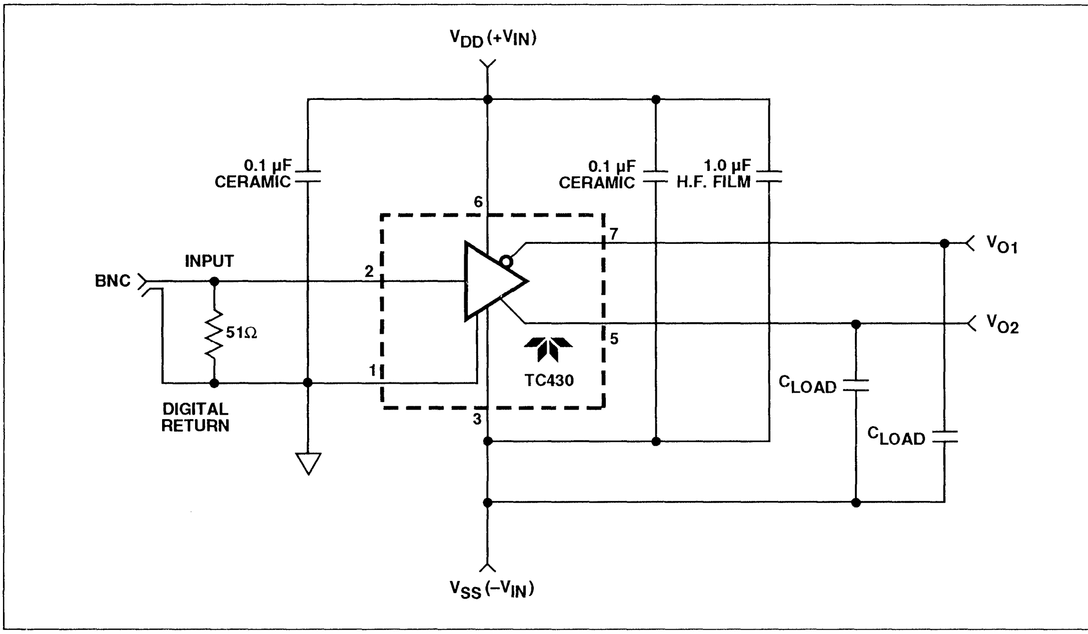


Figure 2 Output Drive Skew

TEST CIRCUIT



APPLICATIONS INFORMATION

Functional Description

The TC430 is fabricated with a super-fast silicon gate process. The input stage consists of a Schmitt trigger which drives a level shift circuit. The level shift circuit allows the input signal to be referenced to some point other than the output return, pin 3 (V_{SS}). This allows the output to swing positive and negative relative to the digital return (pin 1).

The output stage is a low-impedance MOSFET totem pole that can source or sink currents up to 3A peak. This type of output can swing to within millivolts of either rail when driving capacitive loads. Output rise times are on the order of 3 ns, while propagation delays are in the 15 ns region.

Application Tips

Due to its high speed and short transition times, proper layout of the PC board is critical. See Application Note 28 for further information on the effects of layout.

Additional precautions that must be made in addition to those in Application Note 28 are:

(1) Decoupling between the digital return and V_{DD} is critical.
(2) A minimum 4.5V must be maintained between digital return and V_{DD}.
(3) Decoupling between V_{DD} and V_{SS} is critical.
(4) Single-point (star) ground systems should be used.

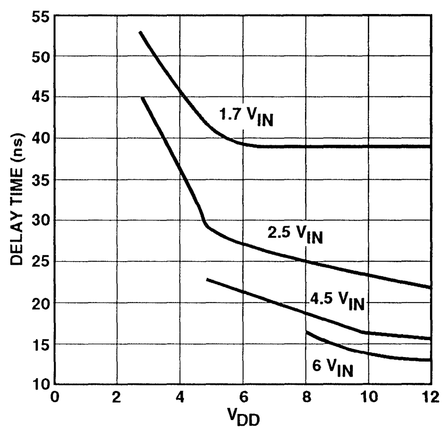
For decoupling between digital return and V_{DD} [item (1) above] a 1 µF 50V polyester film cap (such as a Wima MKS-2) in parallel with a multilayer ceramic 0.1 µF 50 X7R (such as an AVX dip guard) will work well. These capacitors have to be mounted as close as possible to the respective pins on the TC430 to minimize circuit inductance.

Circuits that are improperly decoupled will exhibit oscillations on the output.

A minimum 4.5V between digital return and V_{DD} [item (2) above] is necessary to ensure that the level shifting and hysteresis circuits have enough voltage to function properly. Put another way, the input circuit is referenced to the positive supply, not the negative supply.

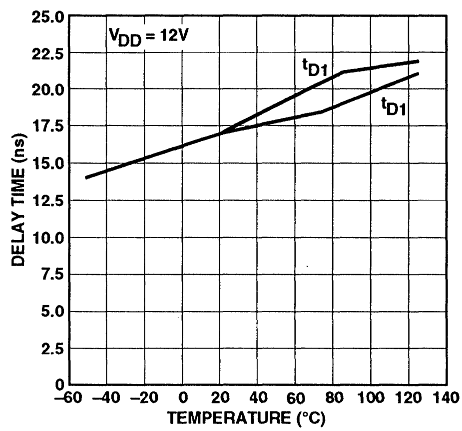
Decoupling of the V_{SS} to V_{DD} [item (3) above] is important because of the high peak current capability of the output of the TC430. The suggested decoupling is a low ESR polyester film capacitor (such as the 1 µF 50V MKS-2) and a ceramic capacitor (such as the AVX 0.1 µF 50V dip guard).

Delay Time vs V_{DD}



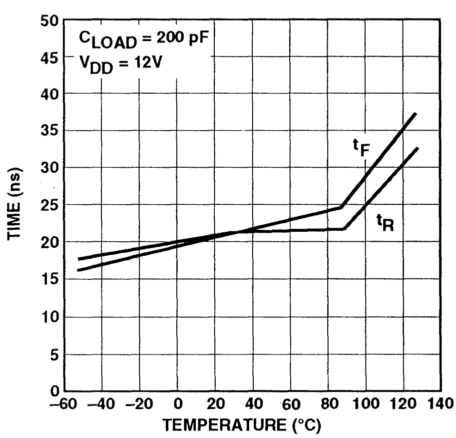
NOTE: Digital return tied to V_{SS}.

Delay Time vs Temperature



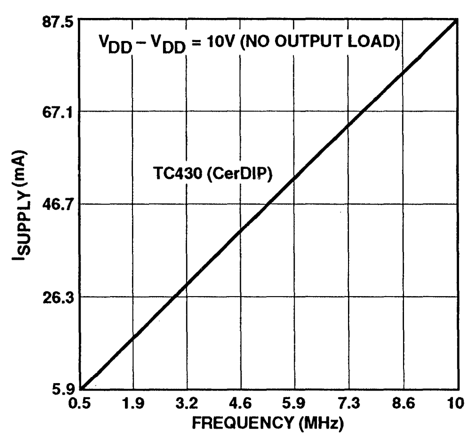
NOTE: Digital return tied to V_{SS}.

Rise/Fall Times vs Temperature



NOTE: Digital return tied to V_{SS}.

Supply Current vs Frequency



The parallel combination of the two capacitors forms a low-impedance source of power across a broad frequency range for the output stage. This will ensure that for any load and frequency of operation the output will be as "clean" as is practical.

The use of single-point grounds [item (4) above] is very critical. Due to the high peak currents that the TC430 is capable of generating, any additional trace or wire length can cause L di/dt drops that can effect the output and in the extreme cause the device to fail due to voltage breakdown.

Application Note 28 explains parasitic inductance problems further.

Operation From a Single Supply

If the TC430 is operated from a single supply voltage, the digital return pin must be tied to the V_{SS} pin. This eliminates the need for the decoupling capacitors from V_{DD} to digital return.

Load Return Path

It is very important to return the load currents directly to, and in the shortest possible distance to V_{SS}, pin 3. Again, this is due to the parasitic inductance of the PC board trace or wire. The test circuit shows how the load capacitors, C_{LOAD}, are returned to the same point as the decoupling capacitors which is directly on pin 3.

Input Signal Considerations

The amplitude of the input signal has a significant effect on the propagation delay through the IC.

While the device can be driven with a signal as small as 2V, propagation delays will be in the 40 ns region. If the input is increased to 5V, delays will be in the 15 ns region.

The input stage of the TC430 is a MOSFET gate. Thus, it is of high impedance and requires little drive current. This eliminates the need for speed-up capacitors as with older bipolar parts. The use of speed-up capacitors is not recommended, as they can cause voltage-doubling effects that can be detrimental to the life of the device.

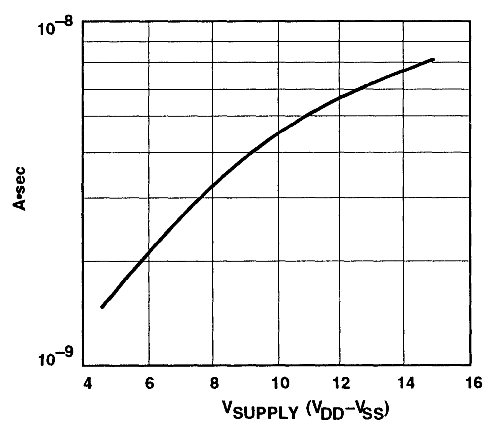
6

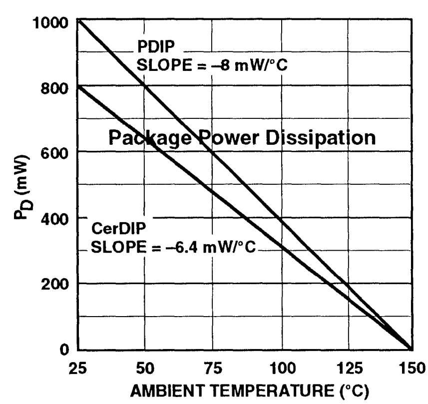
Table I Maximum Operating Frequency

V_S	Max Frequency
12V	4 MHz
10V	9.1 MHz
5V	20 MHz

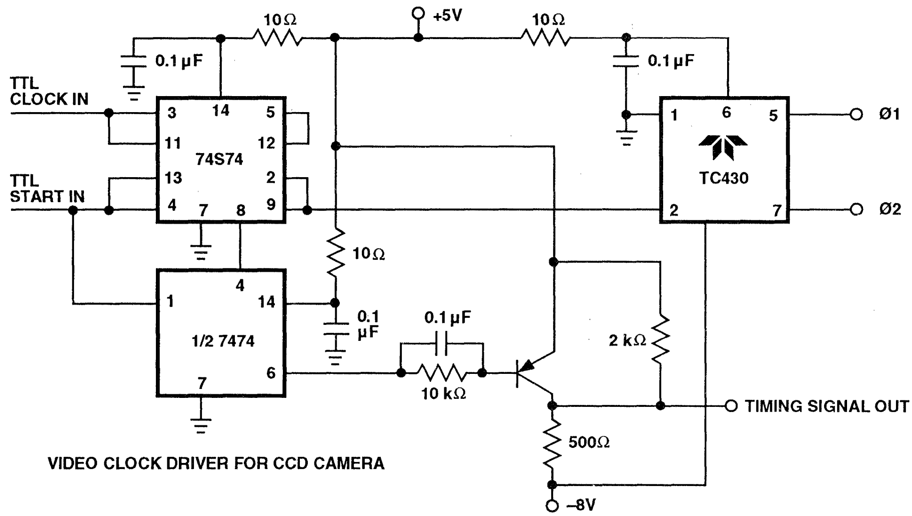
Conditions:
1. CerDIP Package (θ_{JA} = 150°C/W)
2. T_A = 25°C
3. No load

Crossover Energy Loss





APPLICATIONS



VIDEO CLOCK DRIVER FOR CCD CAMERA

![TELEDYNE COMPONENTS]

TELEDYNE COMPONENTS

6A OPEN-DRAIN MOSFET DRIVER

FEATURES

- Independently-Programmable Rise and Fall Times
- High Peak Output Current .... 6A Peak
- Low Output Impedance .... 2.5Ω Typ
- High Speed t_R, t_F .... <30 ns with 1800 pF Load
- Short Delay Times .... 55ns Typ
- Wide Operating Range .... 4.5V to 18V

APPLICATIONS

- Motor Controls
- Self-Commutating MOSFET Bridge Driver
- Driving Bipolar Transistors
- Driver for Nonoverlapping Totem Poles
- Reach-Up/Reach-Down Driver

RUGGED

- Tough CMOS Construction
- Latch-Up Protected: Will Withstand >1.5 mA Reverse Current (Either Polarity)
- Input Withstands Negative Swings Up to –5V
- ESD Protected 4kV

GENERAL DESCRIPTION

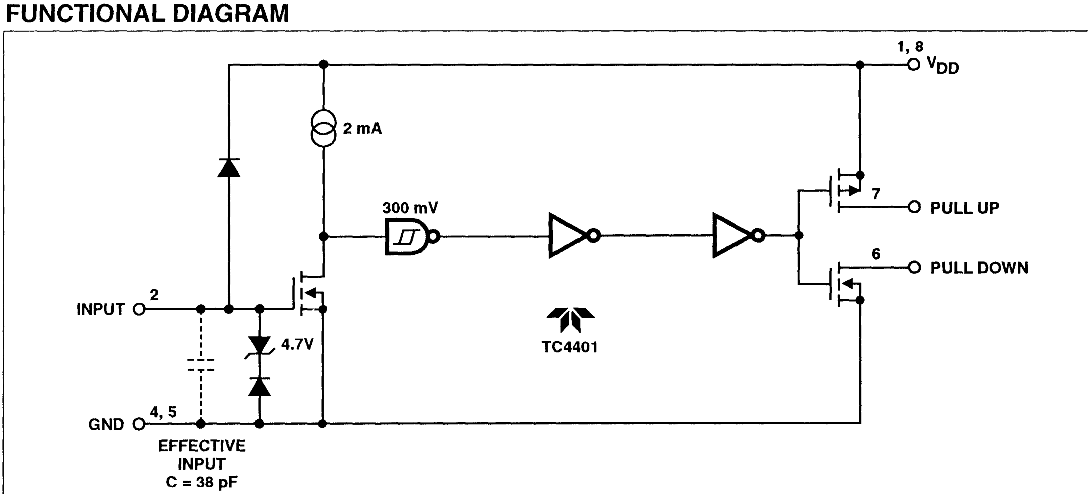
The TC4401 is a CMOS buffer-driver constructed with complementary MOS outputs, where the drains of the final output totem pole have been left disconnected so individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of individual drain current-limiting resistors in the pull-up and pull-down sections of the output, thus allowing the user to define the rates of rise and fall times desired for a capacitive load, or a reduced output swing if driving a resistive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 ns for a 2500-pF load. There is no upper limit.

For driving MOSFETs in motor-control applications, where slow-on/fast-off operation is desired, the TC4401 is superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because it allows accurate control of turn-on, while maintaining fast turn-off and maximum noise immunity for the device being driven.

When used to drive bipolar transistors, this driver maintains the high speeds common to other Teledyne drivers and allows insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-off. By proper positioning of the resistor, either npn or pnp transistors can be driven.

6

FUNCTIONAL DIAGRAM



TC4401

For driving many loads in low-power regimes, this driver, because it has very low quiescent current (<150 μA) and eliminates shoot-through currents in the output stage, requires significantly less power than similar drivers, and can be helpful in meeting low-power budgets.

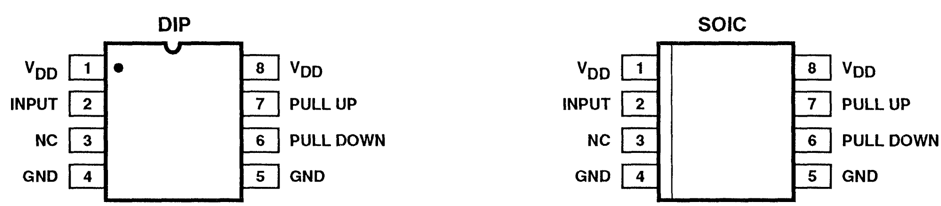
Because neither drain in an output is dependent on the other (though they do switch simultaneously), this device can also be used as an open-drain buffer/driver where both drains are available in one device, thus minimizing chip count. An unused open drain should be returned to the supply rail its device source are connected to (pull-down to ground, pull-up to V_{DD}), to prevent static damage. Alternatively, in situations where timing resistors, or other means of limiting crossover currents are used, multiple TC4401's may be paralleled for greater current-carrying capacity.

The TC4401 is built using Teledyne Components' new Tough CMOS process and is capable of giving reliable service in the most demanding electrical environments: it will not latch under any conditions within its power and voltage ratings; it is not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin; and it can accept, without damage or logic upset, up to 1.5 amp of reverse current (of either polarity) being forced back into the outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

ORDERING INFORMATION

Part No.	Logic	Package	Temperature Range
TC4401CPA	Inverting	8-Pin PDIP	0°C to +70°C
TC4401EPA	Inverting	8-Pin PDIP	–40°C to +85°C
TC4401COA	Inverting	8-Pin SOIC	0°C to +70°C
TC4401EOA	Inverting	8-Pin SOIC	–40°C to +85°C
TC4401IJA	Inverting	8-Pin CerDIP	–25°C to +85°C
TC4401MJA	Inverting	8-Pin CerDIP	–55°C to +125°C

PIN CONFIGURATIONS



NC = NO CONNECTION

NOTE: 1. Duplicate pins must both be connected for proper operation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +22V
Input Voltage .... V_{DD} + 0.3V to GND - 5.0V
Input Current ($V_{IN} > V_{DD}$) 50mA
Power Dissipation, $T_A \leq 25°C$
- PDIP 1W
- SOIC 500mW
- CerDIP 800mW

Derating Factors (To Ambient)
- PDIP .... 8 mW/°C
- SOIC .... 4 mW/°C
- CerDIP .... 6.4 mW/°C

Storage Temperature Range .... –65°C to +150°C
Maximum Chip Temperature .... +150°C
Operating Temperature Range
- C Version .... 0°C to +70°C
- I Version .... –25°C to +85°C
- E Version .... –40°C to +85°C
- M Version .... –55°C to +125°C

Lead Temperature (Soldering, 10 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

6

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0 Low Input Voltage		—	1.3	0.8	V
V_{IN} (Max)	Input Voltage Range		–5	—	V_{DD}+0.3	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.1	2.8	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	1.5	2.5	Ω
I_{PK}	Peak Output Current	V_{DD} = 18V	—	6	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1	—	55	75	ns
t_{D2}	Delay Time	Figure 1	—	55	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V	— —	0.45 55	1.5 150	mA µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.

TC4401

ELECTRICAL CHARACTERISTICS:

Measured over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
V_{IN} (Max)	Input Voltage Range		–5	—	V_{DD}+0.3	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	–10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	3	5	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.3	5	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	32	60	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	34	60	ns
t_{D1}	Delay Time	Figure 1	—	50	100	ns
t_{D2}	Delay Time	Figure 1	—	65	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V	— —	0.45 60	3 400	mA µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.

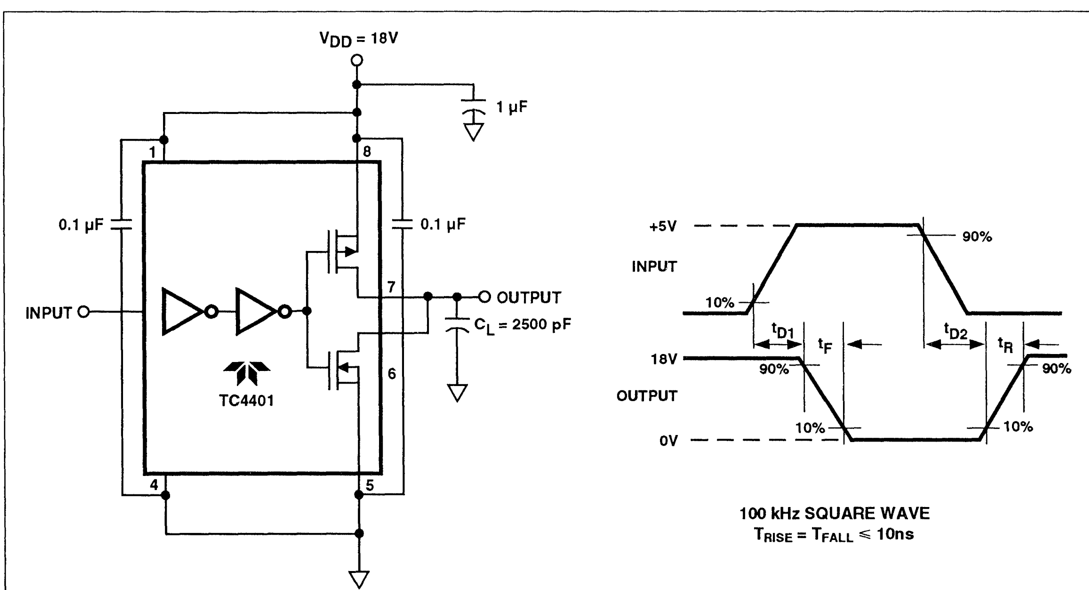
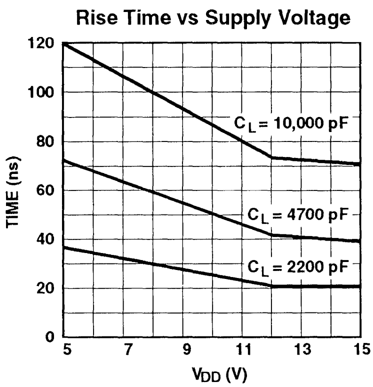
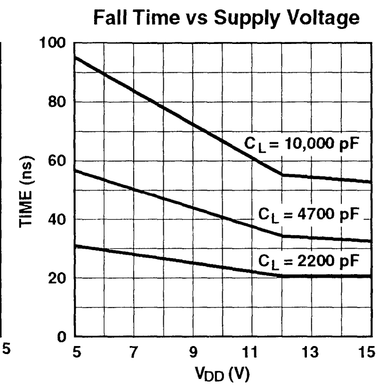
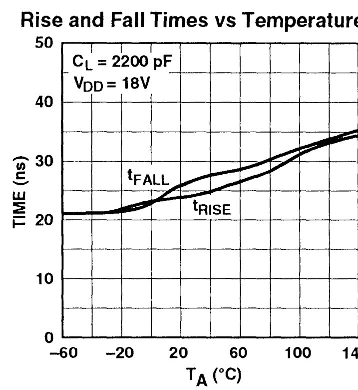


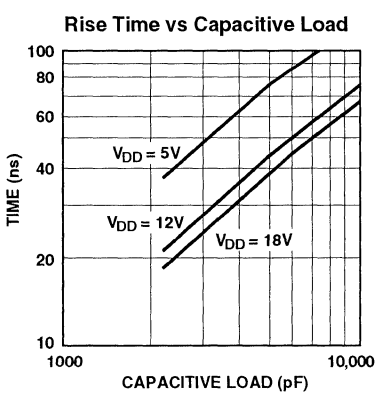
Figure 1. Switching Time Test Circuit

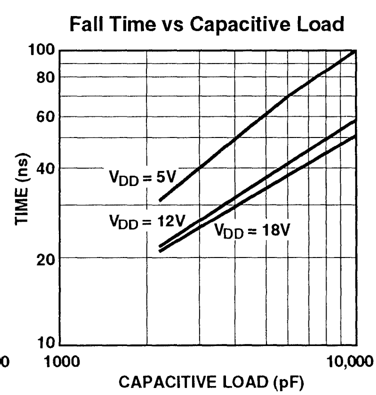
TYPICAL CHARACTERISTICS CURVES

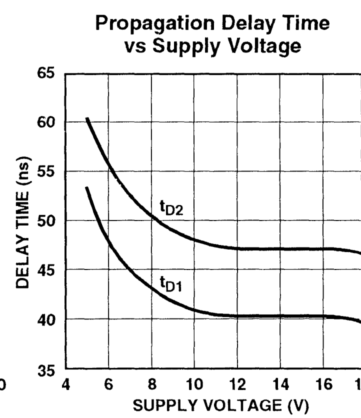


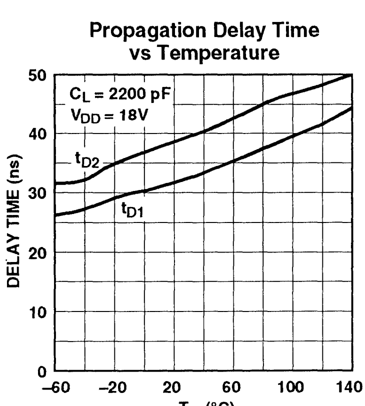


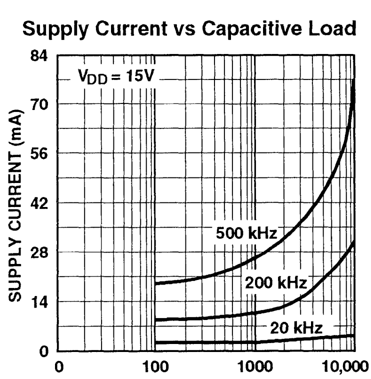


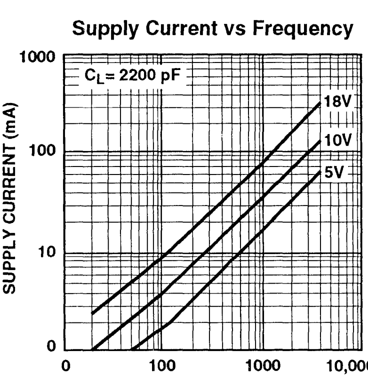








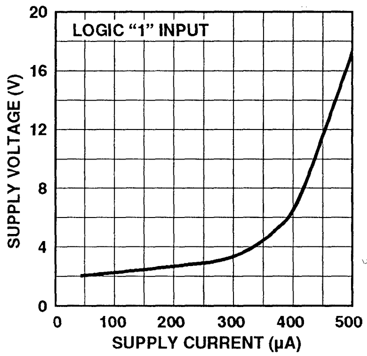




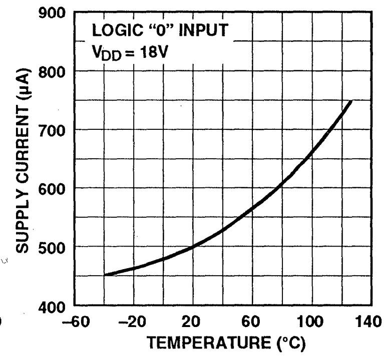
TC4401

TYPICAL CHARACTERISTICS CURVES (Cont.)

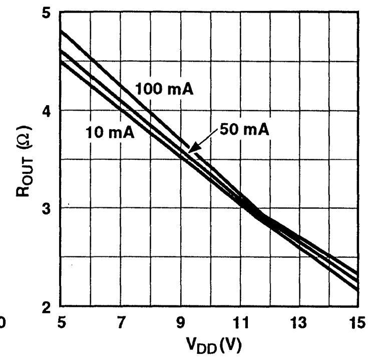
Quiescent Power Supply Current vs Supply Voltage



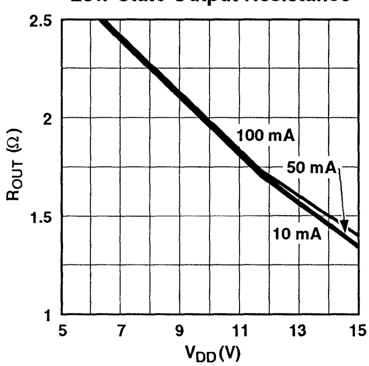
Quiescent Power Supply Current vs Temperature



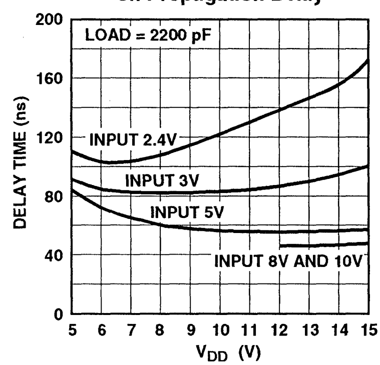
High-State Output Resistance



Low-State Output Resistance



Effect of Input Amplitude on Propagation Delay

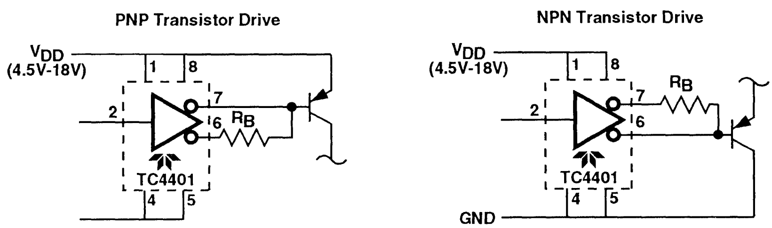


POWER-ON OSCILLATION

It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement. A 'quick fix' for most applications which exhibit POWER-ON OSCILLATION problems is to place approximately 10 kΩ in series with the input of the MOSFET driver.

TYPICAL APPLICATIONS



NOTES

1.5A HIGH-SPEED, FLOATING LOAD DRIVER

FEATURES

- Tough CMOS™ Construction
- Low Quiescent Current .... 300 μA Max
- Capacitive Inputs With 300 mV Hysteresis
- Both Inputs Must Be Driven to Drive Load
- Low Output Leakage
- High Peak Current Capability
- Fast Output Rise Time
- Outputs Individually Testable

APPLICATIONS

- Squib Drivers
- Isolated Load Drivers
- Pulsers
- Safety Interlocks

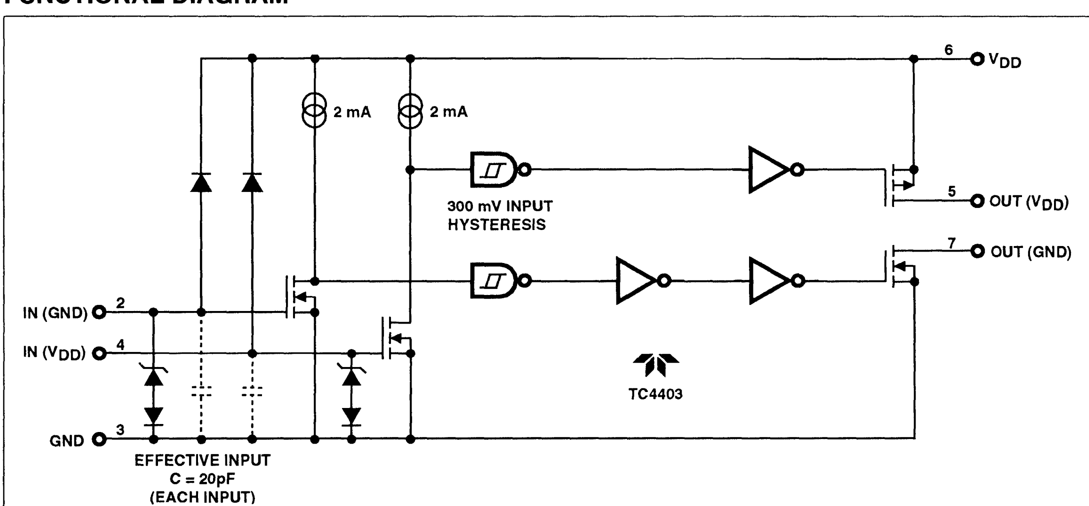
GENERAL DESCRIPTION

The TC4403 is a modified version of the TC4425 driver, intended to drive floating or isolated loads requiring high-current pulses. The load is intended to be connected between the outputs without other reference to supply or ground. Then, only when both logic inputs and the V_{DD} input are energized, is power supplied to the load. This construction allows the implementation of a wide variety of redundant input controllers.

The low off-state output leakage and independence of the two half-circuits permit a wide variety of testing schemes to be utilized to assure functionality. The high peak current capability, short internal delays, and fast output rise and fall times ensure sufficient power will be available to the load when it is needed. The TTL and CMOS compatible inputs allow operation from a wide variety of input devices. The ability to swing the inputs negative without affecting device performance allows negative biases to be placed on the inputs for greater safety. In addition, the capacitive nature of the inputs allows the use of series resistors on the inputs for extra noise suppression.

The TC4403 is built using Teledyne Components' new Tough CMOS process for outstanding ruggedness and reliability in harsh applications. Input voltage excursions above the supply voltage or below ground are clamped internally without damaging the device. The output stages are power MOSFETs with high-speed body diodes to prevent damage to the driver from inductive kickbacks.

FUNCTIONAL DIAGRAM

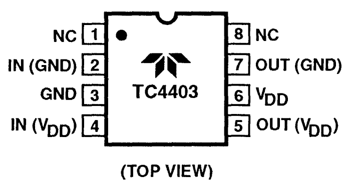


TC4403

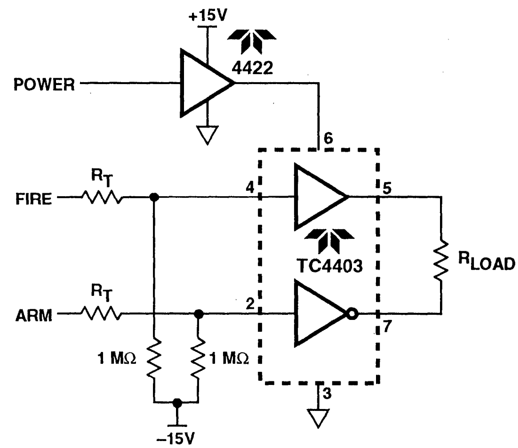
ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4403CPA	8-Pin PDIP	0°C to 70°C
TC4403EPA	8-Pin PDIP	–40°C to +85°C
TC4403MJA	8-Pin CerDIP	–55°C to +125°C

PIN CONFIGURATION



TYPICAL APPLICATION

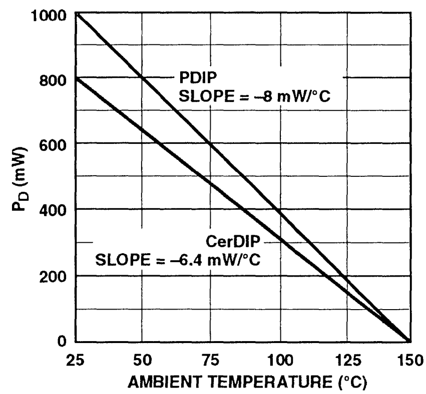


1.5A HIGH-SPEED, FLOATING LOAD DRIVER

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +22V
Maximum Chip Temperature .... +150°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Package Thermal Resistance
  CerDIP, $R_{\theta J\text{-}A}$ .... 150°C/W
  CerDIP, $R_{\theta J\text{-}C}$ .... 50°C/W
  PDIP, $R_{\theta J\text{-}A}$ .... 125°C/W
  PDIP, $R_{\theta J\text{-}C}$ .... 42°C/W
Operating Temperature Range
  C Version .... 0°C to +70°C
  E Version .... –40°C to +85°C
  M Version .... –55°C to +125°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.



ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_S ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ 5V	–1000	±10	+1000	nA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_{OS}	Sourcing Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V	—	2..8	5	Ω
R_{OG}	Grounding Output Resistance	I_{OUT} = –10 mA, V_{DD} = 18V	—	3.5	5	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	23	35	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	33	75	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	38	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	1.5	2.5	mA
		V_{IN} = 0V (Both Inputs)	—	0.15	0.25	mA

NOTE: 1. Switching times guaranteed by design.

TC4403

ELECTRICAL CHARACTERISTICS:

Measured over operating temperature range with 4.5V ≤ V_S ≤ 18V unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10,000	±10	+10,000	nA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_{OS}	Sourcing Output Resistance	V_{IN} = 2.4V I_{OUT} = 10 mA, V_{DD} = 18V	—	3.7	8	Ω
R_{OG}	Grounding Output Resistance	V_{IN} = 2.4V I_{OUT} = –10 mA, V_{DD} = 18V	—	4.3	8	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	28	60	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	32	60	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	32	100	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	38	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	2 0.2	3.5 0.3	mA mA

NOTE: 1. Switching times guaranteed by design.

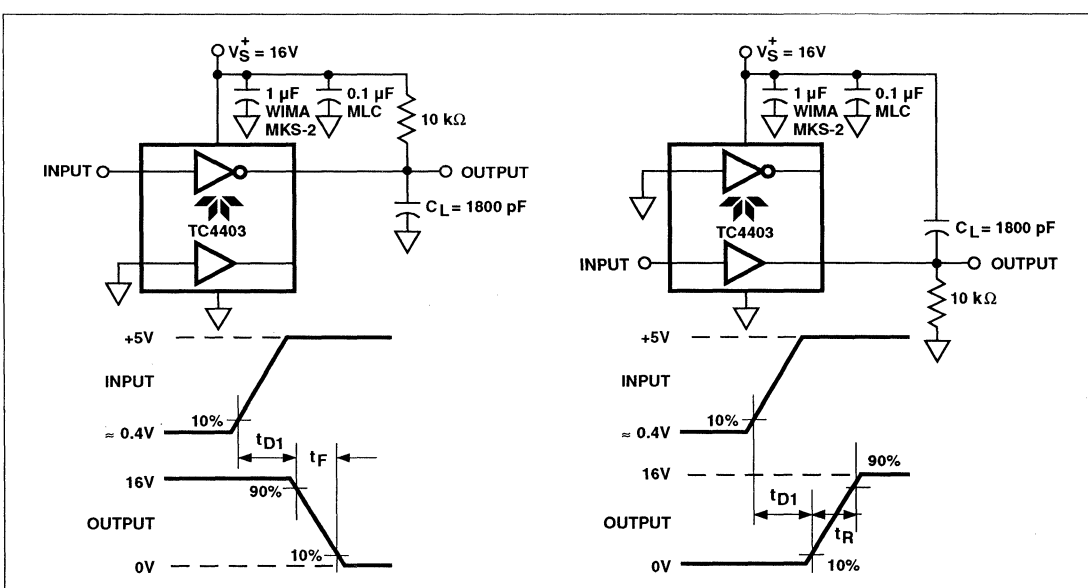
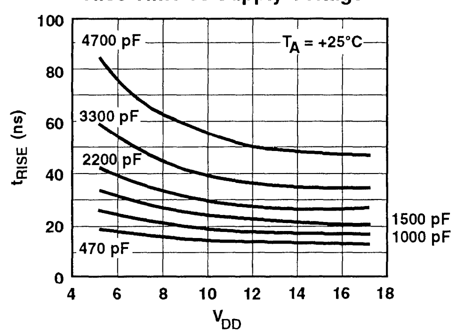


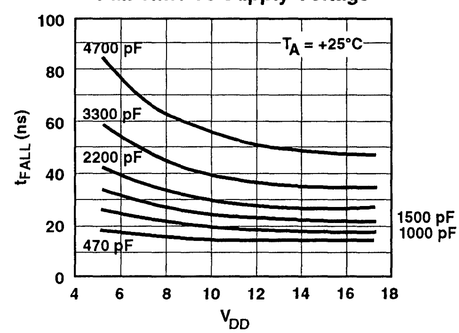
Figure 1 Switching Time Test Circuits

TYPICAL CHARACTERISTICS CURVES

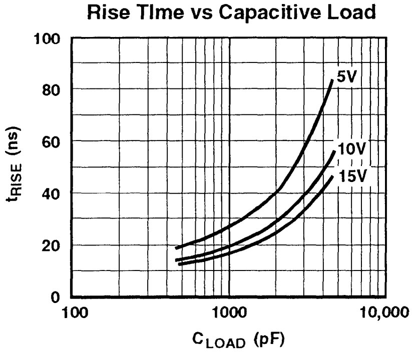
Rise Time vs Supply Voltage



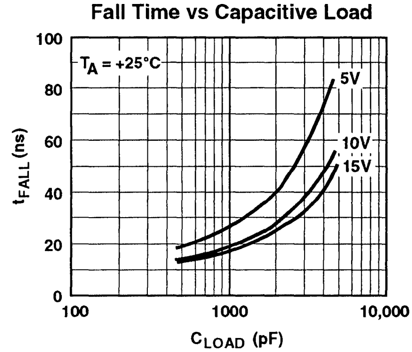
Fall Time vs Supply Voltage



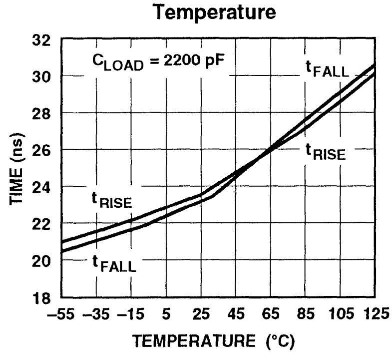
Rise Time vs Capacitive Load



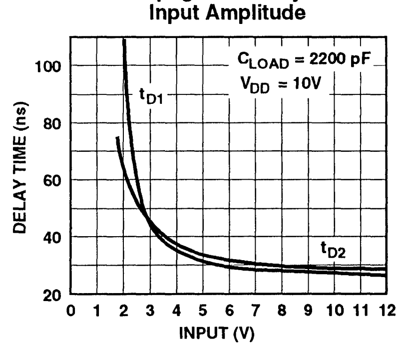
Fall Time vs Capacitive Load



Rise and Fall Times vs Temperature

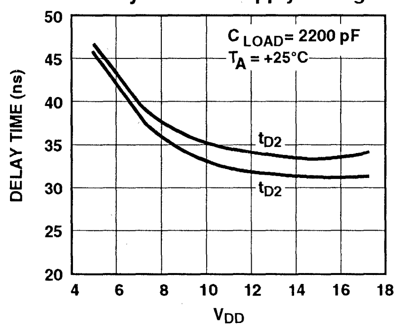


Propagation Delay vs Input Amplitude

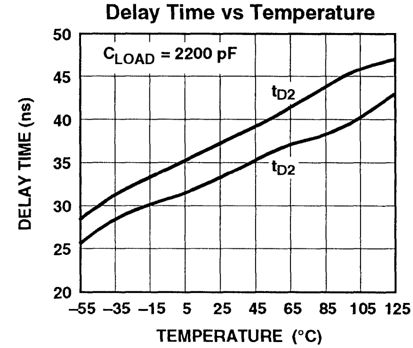


TYPICAL CHARACTERISTICS CURVES (Cont.)

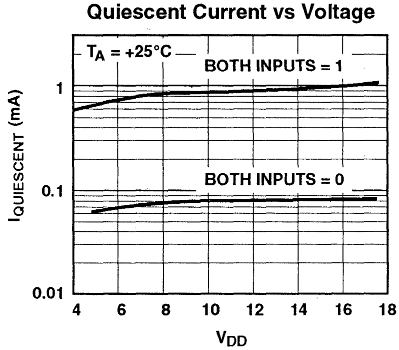
Delay Time vs Supply Voltage



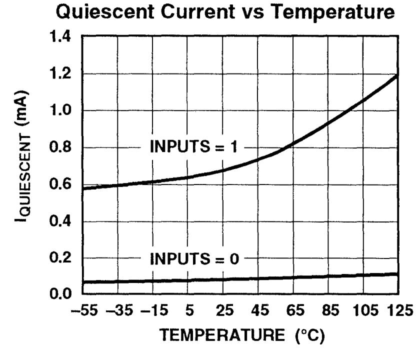
Delay Time vs Temperature



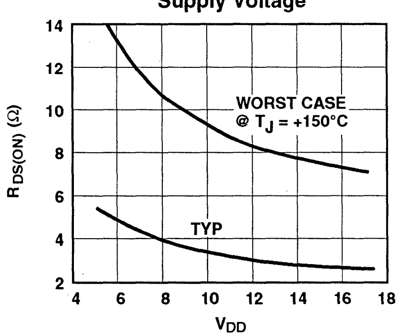
Quiescent Current vs Voltage



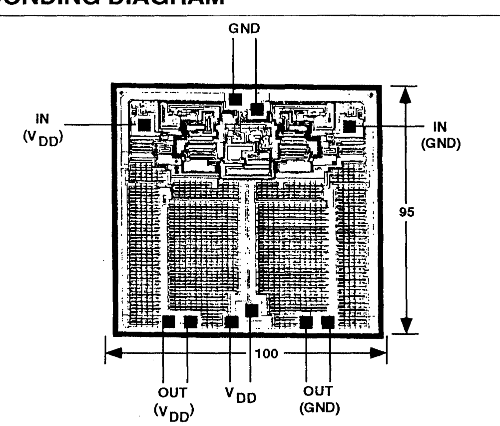
Quiescent Current vs Temperature



Output Resistance vs Supply Voltage



BONDING DIAGRAM



NOTES:
1. Back of die is not metallized.
2. Back of die is common to V_{DD}.
3. Dual bond pads must BOTH be connected.

TELEDYNE COMPONENTS

TC4404
TC4405

1.5A DUAL OPEN-DRAIN MOSFET DRIVERS

FEATURES

- Independently-Programmable Rise and Fall Times
- Low Output Impedance .... 7Ω Typ
- High Speed t_R, t_F .... <30 ns with 1000 pF Load
- Short Delay Times
- Wide Operating Range .... 4.5V to 18V

APPLICATIONS

- Motor Controls
- Self-Commutating MOSFET Bridge Driver
- Driving Bipolar Transistors
- Driver for Nonoverlapping Totem Poles
- Reach-Up/Reach-Down Driver

RUGGED

- Tough CMOS™ Construction
- Latch-Up Protected: Will Withstand >500 mA Reverse Current (Either Polarity)
- Input Withstands Negative Swings Up to –5V

GENERAL DESCRIPTION

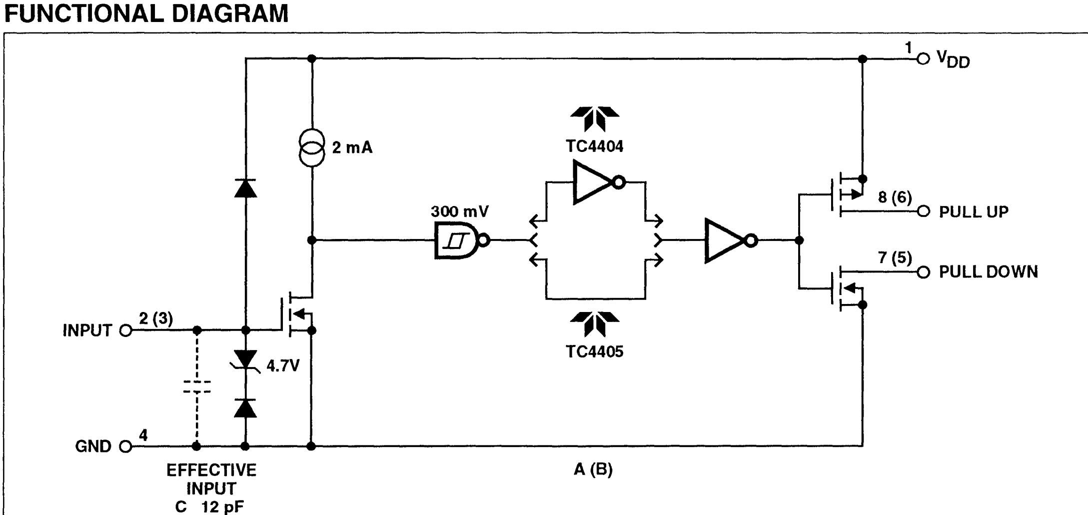
The TC4404 and TC4405 are CMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the final output totem pole have been left disconnected so individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of individual drain-current-limiting resistors in the pull-up and pull-down sections of the output, thus allowing the user to define the rates of rise and fall desired for a capacitive load, or a reduced output swing if driving a resistive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 ns for a 1000-pF load. There is no upper limit.

For driving MOSFETs in motor-control applications, where slow-on/fast-off operation is desired, these devices are superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because they allow accurate control of turn-on, while maintaining fast turn-off and maximum noise immunity for an OFF device.

When used to drive bipolar transistors, these drivers maintain the high speeds common to other Teledyne drivers and allow insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-off. By proper positioning of the resistor, either npn or pnp transistors can be driven.

6

FUNCTIONAL DIAGRAM



1023-1

1.5A DUAL OPEN-DRAIN MOSFET DRIVERS

TC4404
TC4405

For driving many loads in low-power regimes, these drivers, because they eliminate shoot-through currents in the output stage, require significantly less power at higher frequencies, and can be helpful in meeting low-power budgets.

Because neither drain in an output is dependent on the other, these devices can also be used as open-drain buffer/drivers where both drains are available in one device, thus minimizing chip count. Unused open drains should be returned to the supply rail their device sources are connected to (pull-downs to ground, pull-ups to V_{DD}), to prevent static damage. In addition, in situations where timing resistors, or other means of limiting crossover currents are used, like drains may be paralleled for greater current carrying capacity.

These devices are built using Teledyne Components' new Tough CMOS process and are capable of giving reliable service in the most demanding electrical environments: they will not latch under any conditions within their power and voltage ratings; they are not subject to damage when up to 5V of noise spiking of either polarity occurs on their ground pin; and they can accept, without damage or logic upset, up to 1/2 amp of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

ORDERING INFORMATION

Part No.	Logic	Package	Temperature Range
TC4404CPA	Inverting	8-Pin PDIP	0°C to +70°C
TC4404COA	Inverting	8-Pin SOIC	0°C to +70°C
TC4405CPA	Noninverting	8-Pin PDIP	0°C to +70°C
TC4405COA	Noninverting	8-Pin SOIC	0°C to +70°C
TC4404EPA	Inverting	8-Pin PDIP	–40°C to +85°C
TC4404EOA	Inverting	8-Pin SOIC	–40°C to +85°C
TC4405EPA	Noninverting	8-Pin PDIP	–40°C to +85°C
TC4405EOA	Noninverting	8-Pin SOIC	–40°C to +85°C
TC4404MJA	Inverting	8-Pin CerDIP	–55°C to +125°C
TC4405MJA	Noninverting	8-Pin CerDIP	–55°C to +125°C

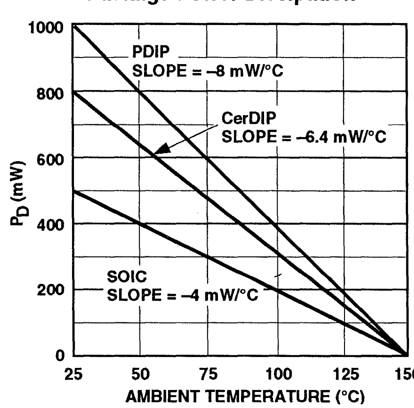
ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +22V
Maximum Chip Temperature .... +150°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J\text{-}A}$ .... 150°C/W
- CerDIP $R_{\theta J\text{-}C}$ .... 55°C/W
- PDIP $R_{\theta J\text{-}A}$ .... 125°C/W
- PDIP $R_{\theta J\text{-}C}$ .... 45°C/W
- SOIC $R_{\theta J\text{-}A}$ .... 250°C/W
- SOIC $R_{\theta J\text{-}C}$ .... 75°C/W

Operating Temperature Range
- C Version .... 0°C to +70°C
- E Version .... –40°C to +85°C
- M Version .... –55°C to +125°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Package Power Dissipation



1.5A DUAL OPEN-DRAIN MOSFET DRIVERS

POWER-ON OSCILLATION

It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement. A 'quick fix' for most applications which exhibit POWER-ON OSCILLATION problems is to place approximately 10 kΩ in series with the input of the MOSFET driver.

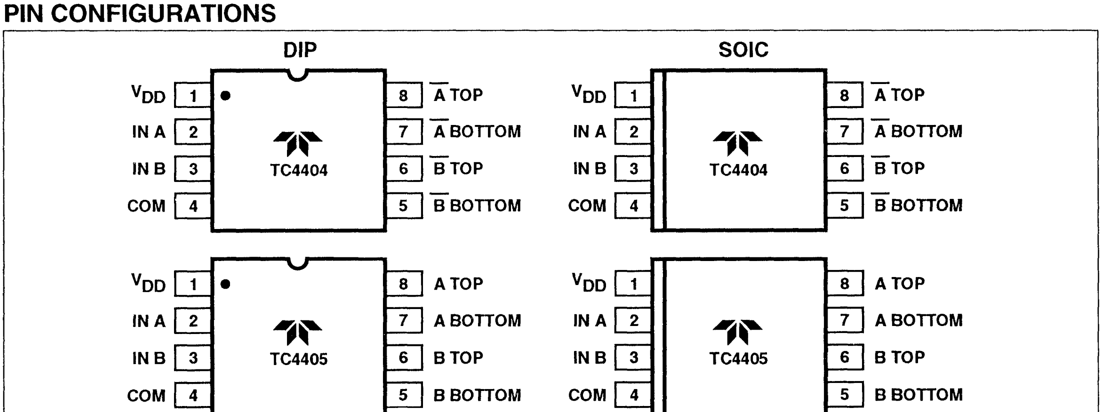
ELECTRICAL CHARACTERISTICS:

Specifications measured at T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	–5V ≤ V_{IN} ≤ V_{DD}	–1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V; Any Drain	—	7	10	Ω
I_{PK}	Peak Output Current	Any Drain	—	1.5	—	A
I_{DC}	Continuous Output Current	Any Drain	—	—	100	mA
I_R	Latch-Up Protection	Any Drain Withstand Reverse Current	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1000 pF	—	25	30	ns
t_F	Fall Time	Figure 1, C_L = 1000 pF	—	25	30	ns
t_{D1}	Delay Time	Figure 1, C_L = 1000 pF	—	—	30	ns
t_{D2}	Delay Time	Figure 1, C_L = 1000 pF	—	—	50	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	4.5	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.4	mA

NOTE: 1. Switching times guaranteed by design.

PIN CONFIGURATIONS



ELECTRICAL CHARACTERISTICS: Specifications measured over operating temperature range with $4.5V \le V_{DD} \le 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$-5V \le V_{IN} \le V_{DD}$	−10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD}−0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V; Any Drain	—	9	12	Ω
I_{PK}	Peak Output Current	Any Drain	—	1.5	—	A
I_{DC}	Continuous Output Current	Any Drain	—	—	100	mA
I_R	Latch-Up Protection	Any Drain Withstand Reverse Current	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1000 pF	—	—	40	ns
t_F	Fall Time	Figure 1, C_L = 1000 pF	—	—	40	ns
t_{D1}	Delay Time	Figure 1, C_L = 1000 pF	—	—	40	ns
t_{D2}	Delay Time	Figure 1, C_L = 1000 pF	—	—	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	8	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.6	mA

NOTE 1. Switching times guaranteed by design.

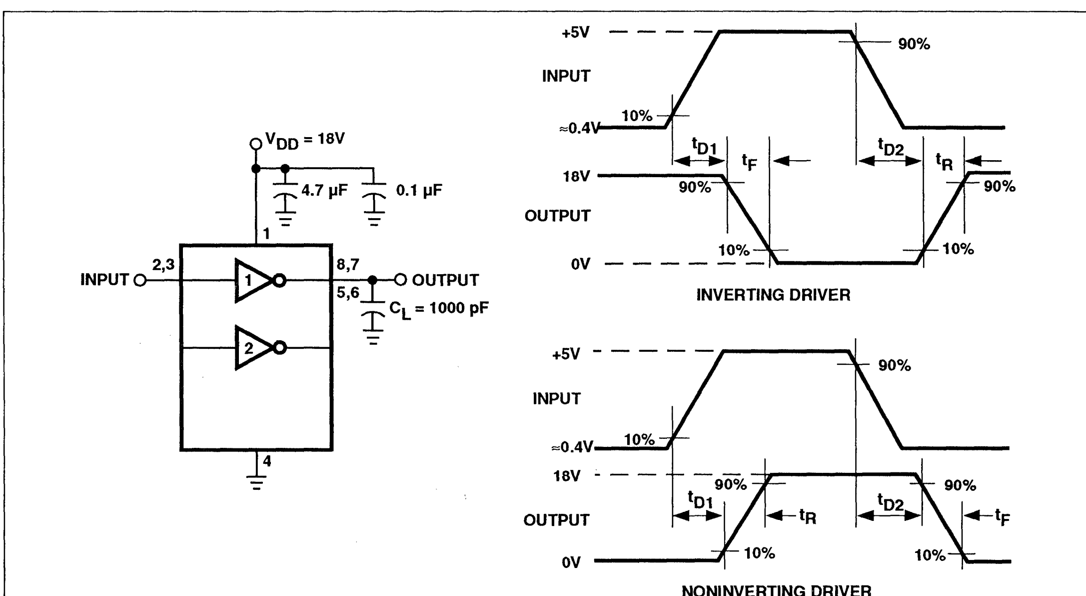
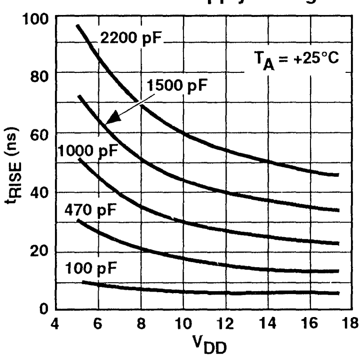


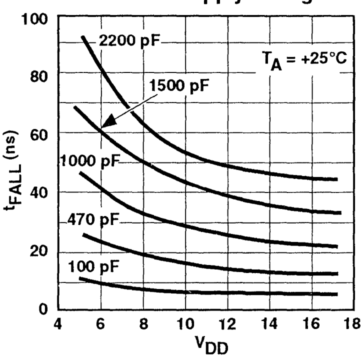
Figure 1 Switching Time Test Circuit

TYPICAL CHARACTERISTICS CURVES

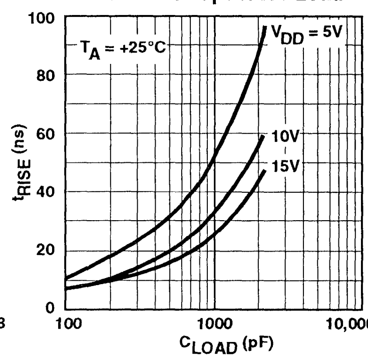
Rise Time vs. Supply Voltage



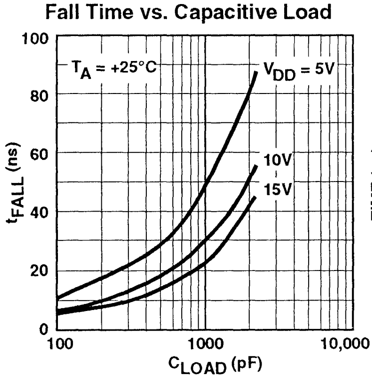
Fall Time vs. Supply Voltage



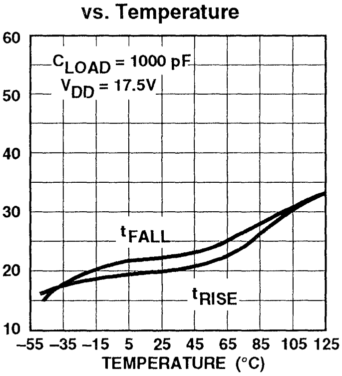
Rise TIme vs. Capacitive Load



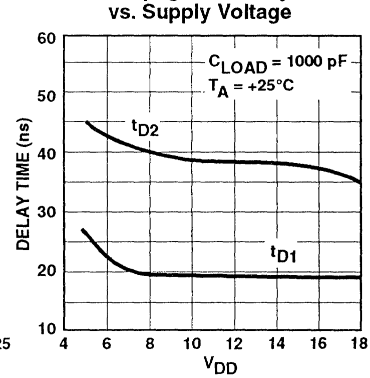
Fall Time vs. Capacitive Load



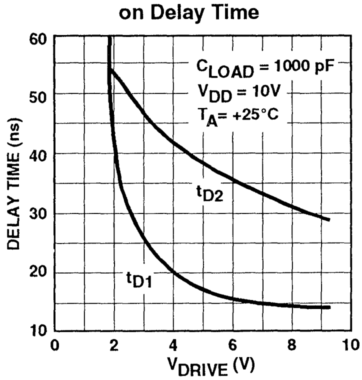
Rise and Fall Times
vs. Temperature



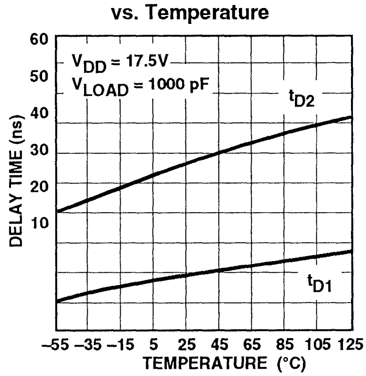
Propagation Delay
vs. Supply Voltage



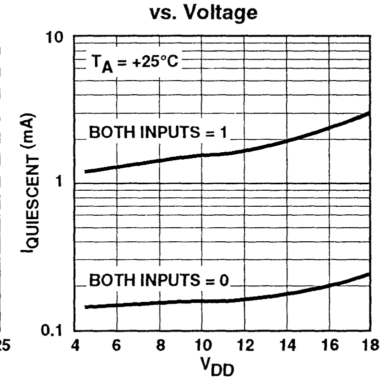
Effect of Input Amplitude
on Delay Time



Propagation Delay Time
vs. Temperature



Quiescent Supply Current
vs. Voltage



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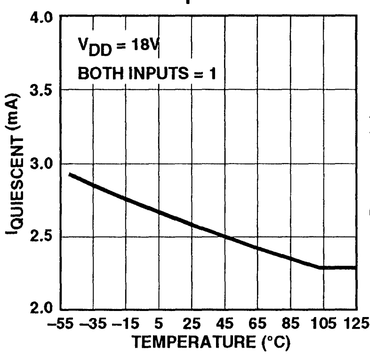
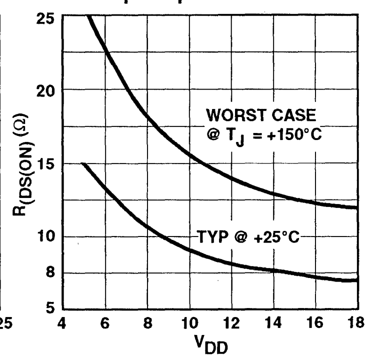
TYPICAL CHARACTERISTICS CURVES (Cont.)

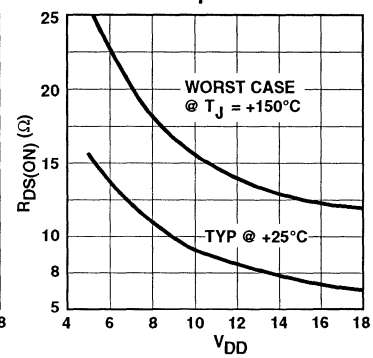
Quiescent Supply Current vs. Temperature



Pull-Up Output Resistance



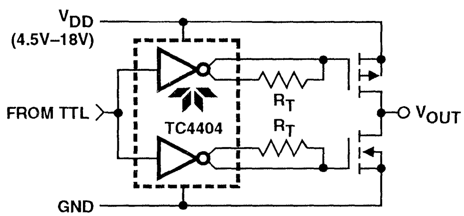
Pull-Down Output Resistance



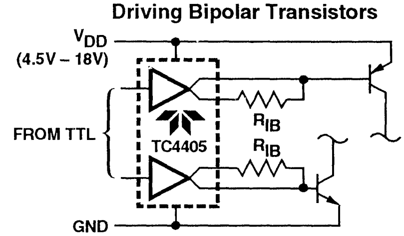
1.5A DUAL OPEN-DRAIN MOSFET DRIVERS

TYPICAL APPLICATIONS

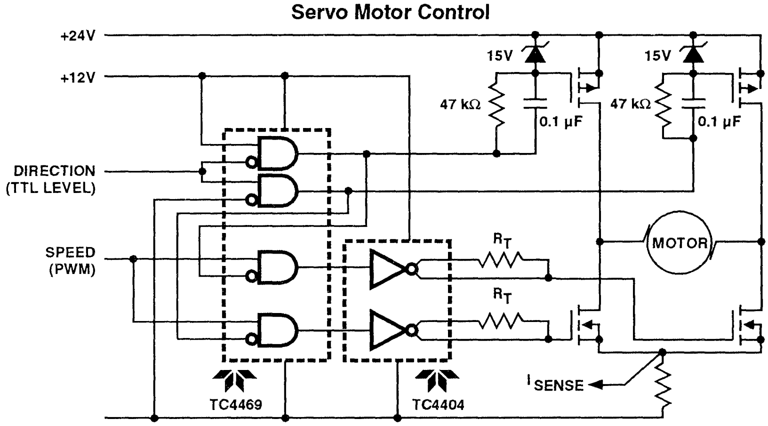
Zero Crossover Current Totem-Pole Switch



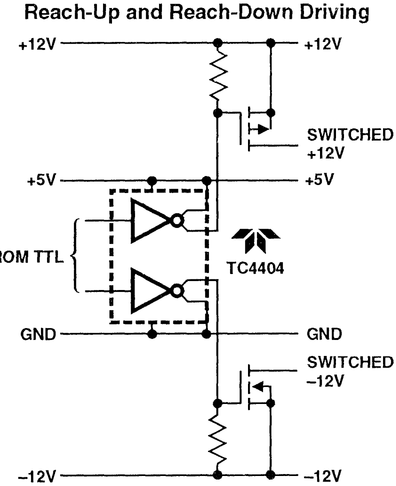
Driving Bipolar Transistors



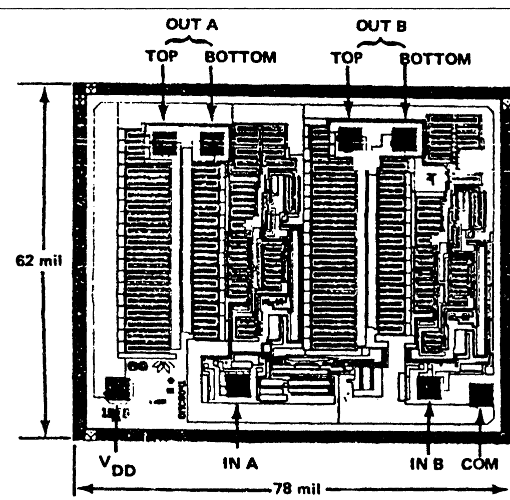
Servo Motor Control



Reach-Up and Reach-Down Driving



BONDING DIAGRAM



NOTES: 1. Back of die is not metallized.
2. Back of die is common to V_{DD}.

NOTES

TELEDYNE COMPONENTS

PRELIMINARY INFORMATION

TC4406
TC4407

3A DUAL OPEN-DRAIN MOSFET DRIVERS

FEATURES

- Independently-Programmable Rise and Fall Times
- Low Output Impedance .... 3.5Ω Typ
- High Speed t_R, t_F .... <30 ns with 1800 pF Load
- Short Delay Times
- Wide Operating Range .... 4.5V to 18V

APPLICATIONS

- Motor Controls
- Self-Commutating MOSFET Bridge Driver
- Driving Bipolar Transistors
- Driver for Nonoverlapping Totem Poles
- Reach-Up/Reach-Down Driver

RUGGED

- Tough CMOS™ Construction
- Latch-Up Protected: Will Withstand >500 mA Reverse Current (Either Polarity)
- Input Withstands Negative Swings Up to –5V

GENERAL DESCRIPTION

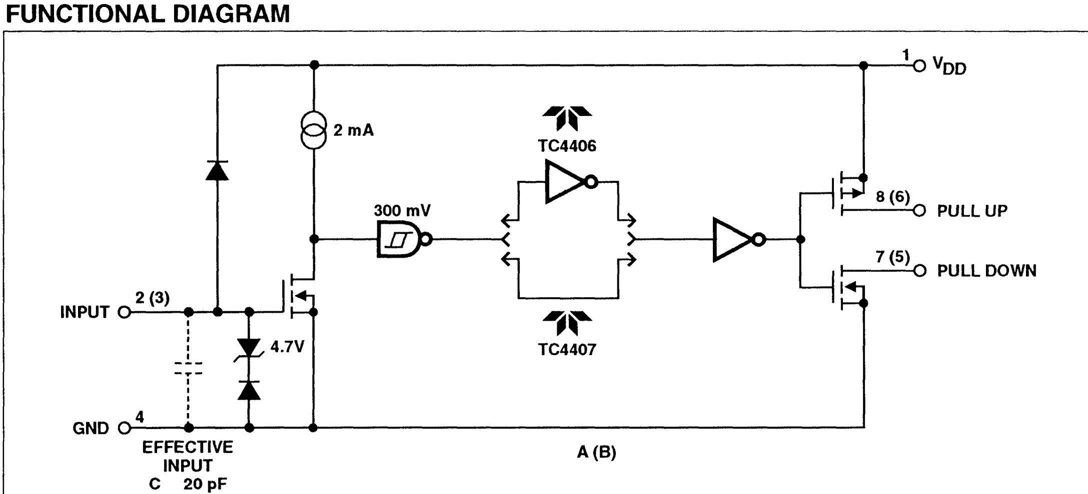
The TC4406 and TC4407 are CMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the final output totem pole have been left disconnected so individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of individual drain current-limiting resistors in the pull-up and pull-down sections of the outputs, thus allowing the user to define the rates of rise and fall desired for a capacitive load, or a reduced output swing if driving a resistive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 ns for a 1800-pF load. There is no upper limit.

For driving MOSFETs in motor-control applications, where slow-on/fast-off operation is desired, these devices are superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because they allow accurate control of turn-on, while maintaining fast turn-off and maximum noise immunity for the device being driven.

When used to drive bipolar transistors, these drivers maintain the high speeds common to other Teledyne drivers and allow insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-off. By proper positioning of the resistor, either npn or pnp transistors can be driven.

6

FUNCTIONAL DIAGRAM



1024-1

3A DUAL OPEN-DRAIN MOSFET DRIVERS

TC4406
TC4407

For driving many loads in low-power regimes, these drivers, because they have very low quiescent current (<250 μA) and eliminate shoot-through currents in the output stage, require significantly less power than similar drivers, and can be helpful in meeting low-power budgets.

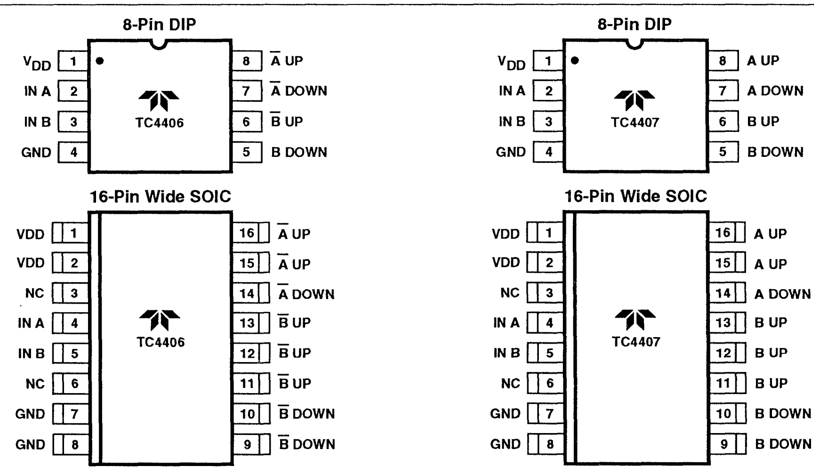
Because neither drain in an output is dependent on the other (though they do switch simultaneously), these devices can also be used as open-drain buffer/drivers where both drains are available in one device, thus minimizing chip count. Unused open drains should be returned to the supply rail their device sources are connected to (pull-downs to ground, pull-ups to V_{DD}), to prevent static damage. Alternatively, in situations where timing resistors, or other means of limiting crossover currents are used, like drains may be paralleled for greater current-carrying capacity.

The TC4406 and TC4407 are built using Teledyne Components' new Tough CMOS process and are capable of giving reliable service in the most demanding electrical environments: they will not latch under any conditions within their power and voltage ratings; they are not subject to damage when up to 5V of noise spiking of either polarity occurs on their ground pin; and they can accept, without damage or logic upset, up to 1/2 amp of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

ORDERING INFORMATION

Part No.	Logic	Package	Temperature Range
TC4406CPA	Inverting	8-Pin PDIP	0°C to +70°C
TC4406EPA	Inverting	8-Pin PDIP	–40°C to +85°C
TC4406EOE	Inverting	16-Pin SO Wide	–40°C to +85°C
TC4406MJA	Inverting	8-Pin CerDIP	–55°C to +125°C
TC4406COE	Inverting	16-Pin SO Wide	0°C to +70°C
TC4407CPA	Noninverting	8-Pin PDIP	0°C to +70°C
TC4407EPA	Noninverting	8-Pin PDIP	–40°C to +85°C
TC4407EOE	Noninverting	16-Pin SO Wide	–40°C to +85°C
TC4407MJA	Noninverting	8-Pin CerDIP	–55°C to +125°C
TC4407COE	Noninverting	16-Pin SO Wide	0°C to +70°C

PIN CONFIGURATIONS



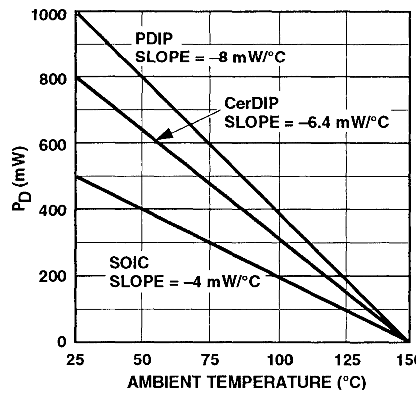
NOTE: 1. Duplicate pins must both be connected for proper operation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +22V
Maximum Chip Temperature .... +150°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Package Thermal Resistance
 CerDIP $R_{\theta J\text{-}A}$ .... 150°C/W
 CerDIP $R_{\theta J\text{-}C}$ .... 55°C/W
 PDIP $R_{\theta J\text{-}A}$ .... 125°C/W
 PDIP $R_{\theta J\text{-}C}$ .... 45°C/W
 SOIC $R_{\theta J\text{-}A}$ .... 250°C/W
 SOIC $R_{\theta J\text{-}C}$ .... 75°C/W
Operating Temperature Range
 C Version .... 0°C to +70°C
 E Version .... –40°C to +85°C
 M Version .... –55°C to +125°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Package Power Dissipation



ELECTRICAL CHARACTERISTICS:

unless otherwise specified, specifications measured at $T_A = +25°C$ with $4.5V \le V_{DD} \le 18V$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$-5V \le V_{IN} \le V_{DD}$	–1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, Pull Up	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.8	5	Ω
R_O	Output Resistance, Pull Down	I_{OUT} = 10 mA, V_{DD} = 18V	—	3.5	5	Ω
I_{PK}	Peak Output Current	Any Drain	—	3	—	A
I_{DC}	Continuous Output Current	Any Drain	—	—	150	mA
I_R	Latch-Up Protection Withstand Reverse Current	Any Drain	> 500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	23	35	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	33	75	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	38	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	1.5	2.5	mA
		V_{IN} = 0V (Both Inputs)	—	0.15	0.25	mA

ELECTRICAL CHARACTERISTICS:

Specifications measured over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	–5V ≤ V_{IN} ≤ V_{DD}	–10	—	10	μA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, Pull Up	I_{OUT} = 10 mA, V_{DD} = 18V	—	3.7	8	Ω
R_O	Output Resistance, Pull Down	I_{OUT} = 10 mA, V_{DD} = 18V	—	4.3	8	Ω
I_{PK}	Peak Output Current	Any Drain	—	3	—	A
I_{DC}	Continuous Output Current	Any Drain	—	—	150	mA
I_R	Latch-Up Protection	Any Drain Withstand Reverse Current	>500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	—	60	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	—	60	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	—	100	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	—	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	2	3.5	mA
		V_{IN} = 0V (Both Inputs)	—	0.2	0.3	mA

NOTE : 1. Switching times guaranteed by design.

Teledyne Components reserves the right to make changes in the circuitry or specifications detailed in this manual at any time without notice. Minimums and maximums are guaranteed. All other specifications are intended as guidelines only. Teledyne Components assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

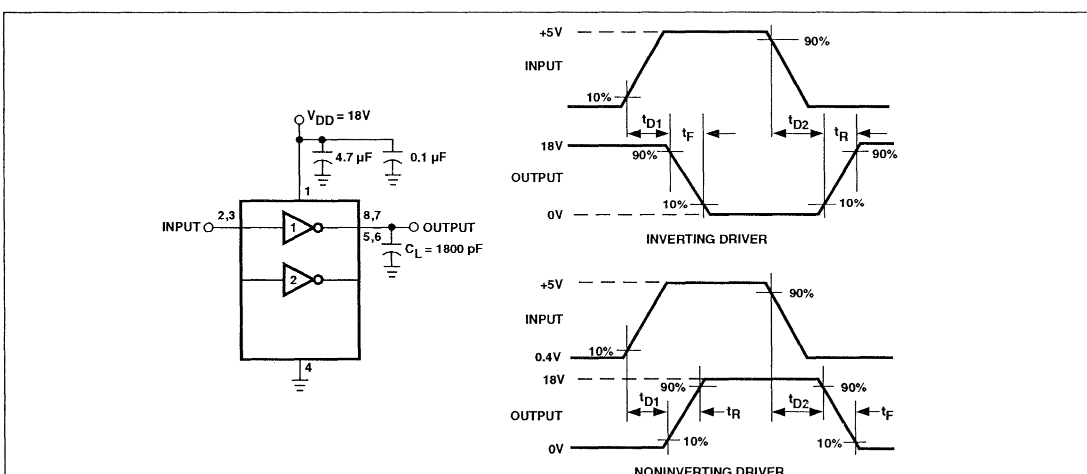
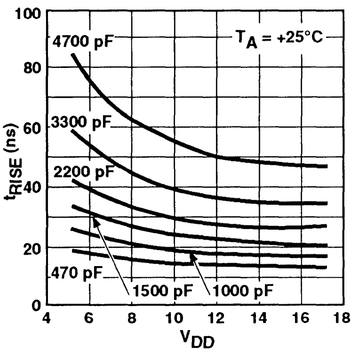


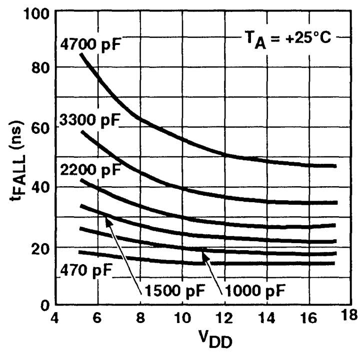
Figure 1 Switching Time Test Circuit

TYPICAL CHARACTERISTICS CURVES

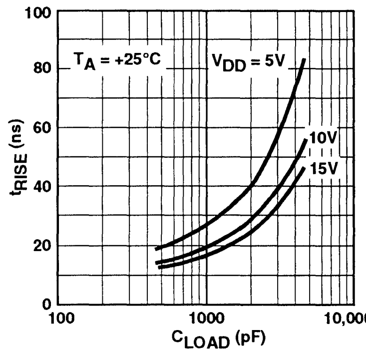
Rise Time vs. Supply Voltage



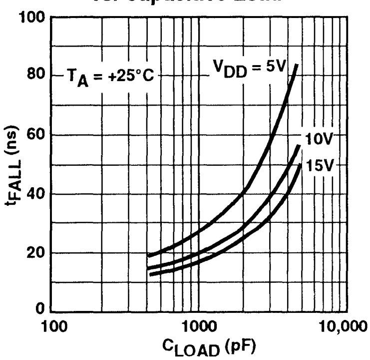
Fall Time vs. Supply Voltage



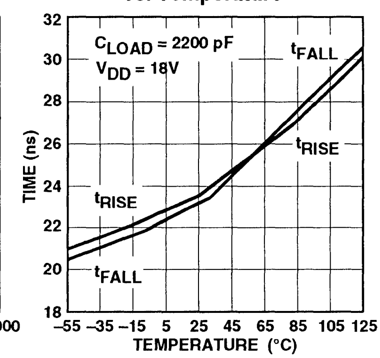
Rise Time vs. Capacitive Load



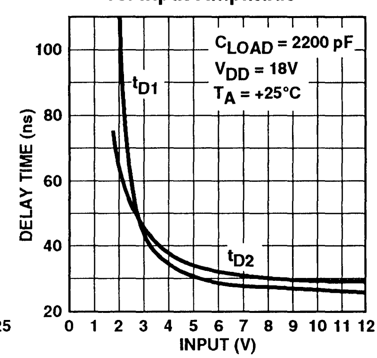
Fall Time vs. Capacitive Load



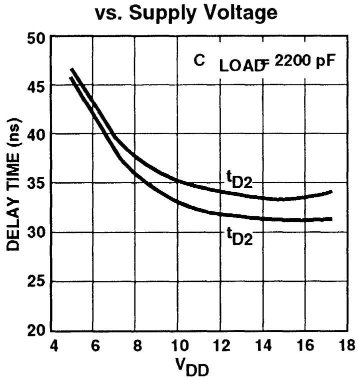
Rise and Fall Times vs. Temperature



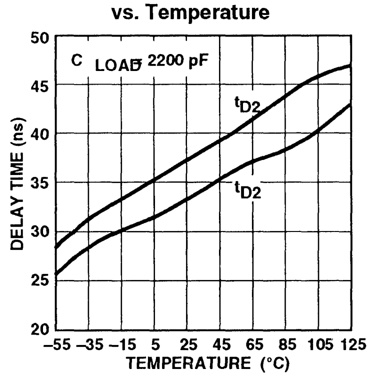
Propagation Delay vs. Input Amplitude



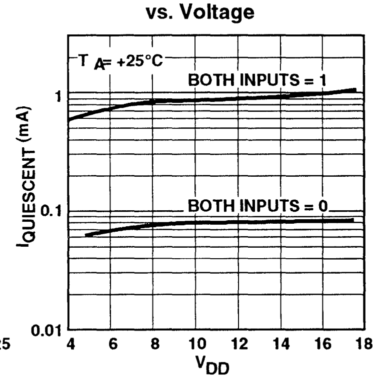
Propagation Delay Time vs. Supply Voltage



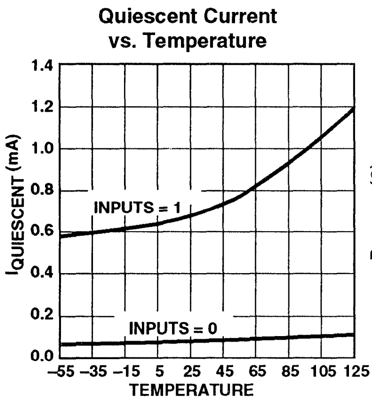
Delay Time vs. Temperature

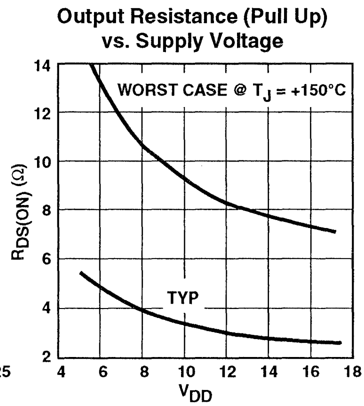


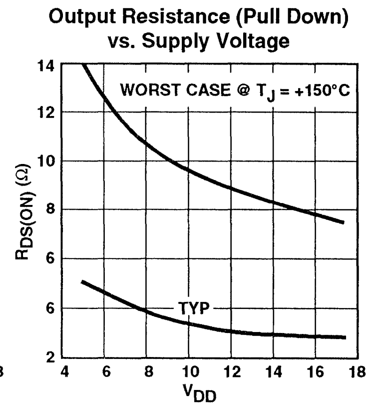
Quiescent Supply Current vs. Voltage



TYPICAL CHARACTERISTICS CURVES (Cont.)

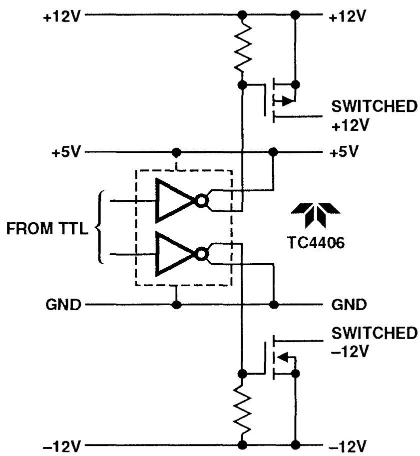




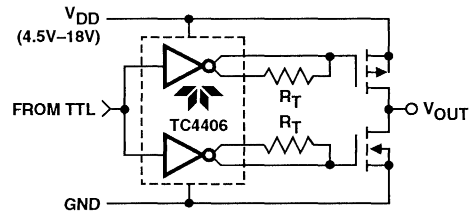


TYPICAL APPLICATIONS

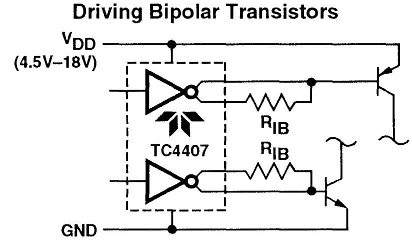
Reach-Up and Reach-Down Driving



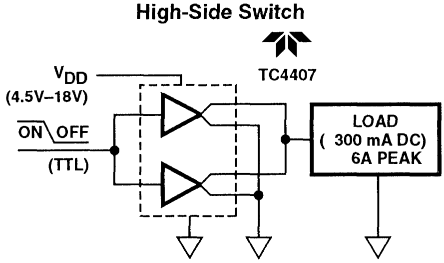
Zero Crossover-Current Totem-Pole Switch



Driving Bipolar Transistors



High-Side Switch



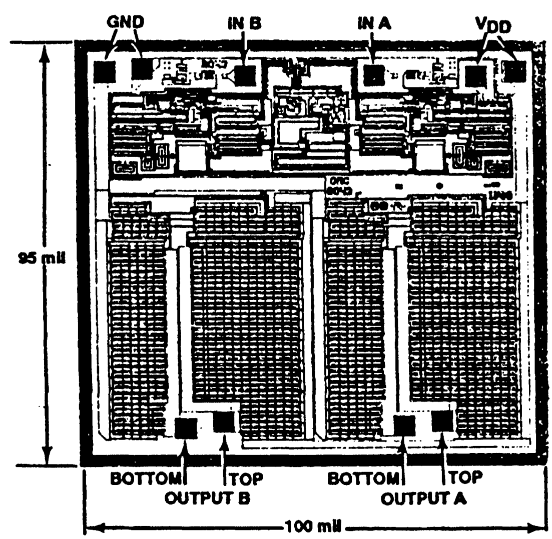
NOTE: Unused drains should be connected to their respective supplies.

POWER-ON OSCILLATION

It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement. A 'quick fix' for most applications which exhibit POWER-ON OSCILLATION problems is to place approximately 10 kΩ in series with the input of the MOSFET driver.

BONDING DIAGRAM



NOTES:
1. Back of die is common to V_{DD}.
2. Back of die is not metallized.
3. Dual bond pads must BOTH be connected (V_{DD} and GND).

NOTES

TELEDYNE
COMPONENTS

TC4420
TC4429

6A HIGH-SPEED MOSFET DRIVERS

FEATURES

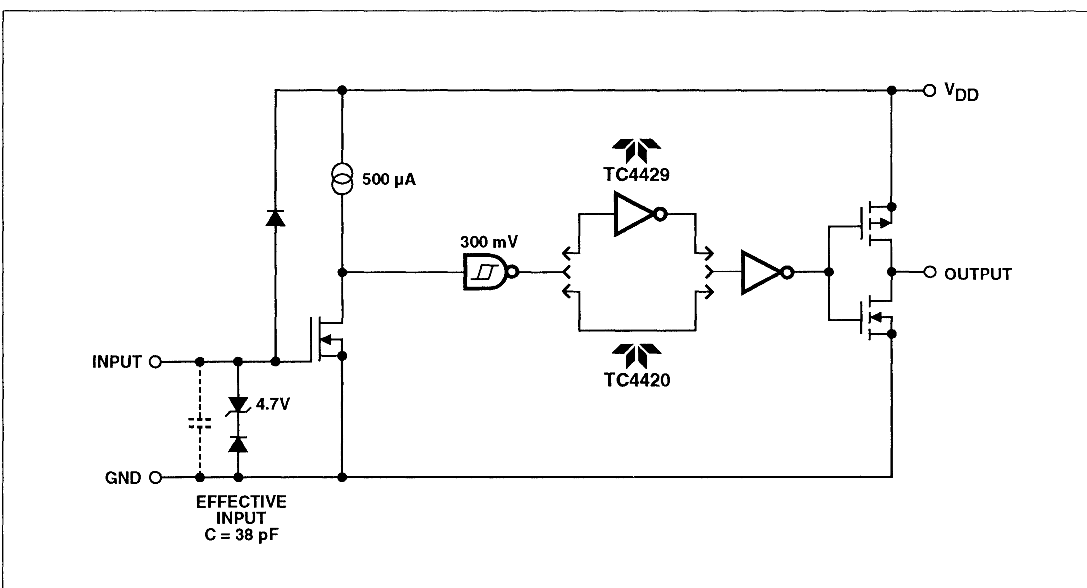
- Tough CMOS™ Construction
- Latch-Up Protected: Will Withstand >1.5A Reverse Output Current
- Logic Input Will Withstand Negative Swing Up to 5V
- ESD Protected .... 4 kV
- Matched Rise and Fall Times .... 25 ns
- High Peak Output Current .... 6A Peak
- Wide Operating Range .... 4.5V to 18V
- High Capacitive Load Drive .... 10,000 pF
- Low Delay Time .... 55 ns Typ
- Logic High Input, Any Voltage .... 2.4V to V_{DD}
- Low Supply Current With Logic "1" Input... 450 μA
- Low Output Impedance 2.5Ω
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}

APPLICATIONS

- Switch-Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class D Switching Amplifiers

6

FUNCTIONAL DIAGRAM



TC4420
TC4429

GENERAL DESCRIPTION

The TC4420/4429 Tough CMOS™ drivers are efficient and easy to use. These devices are 6A (peak) single output MOSFET drivers.

The TC4420/4429 will drive even the largest MOSFETs.

These devices are tough due to extra steps taken to protect them from failures. An epitaxial layer is used to prevent CMOS latch-up. Proprietary circuits allow the input to swing negative as much as 5V without damaging the part. Special circuits have been added to protect against damage from electrostatic discharge. A special molding compound is used for increased moisture resistance and ability to withstand high voltages. They are also tough because of Teledyne Components' world-class process controls and device quality.

Because these devices are fabricated in CMOS, they run cool, use less power and are easier to drive. The rail-to-rail swing capability of CMOS better insures adequate gate voltage to the MOSFET during power up/down sequencing.

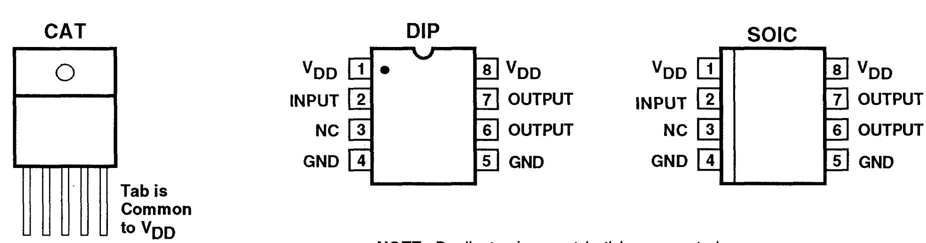
The Tough CMOS™ drivers are easy to use. Three or more discrete components can be replaced with a single device to save PCB area. Any logic input from 2.4V to V_{DD} can be used without external speed-up capacitors or resistor networks.

This family is available in inverting (TC4429) and noninverting (TC4420) configurations. The TC4429 is pin compatible with the popular TC429.

ORDERING INFORMATION

Part No.	Logic	Package	Temperature Range
TC4420CPA	Noninverting	8-Pin PDIP	0°C to +70°C
TC4420EPA	Noninverting	8-Pin PDIP	–40°C to +85°C
TC4420COA	Noninverting	8-Pin SOIC	0°C to +70°C
TC4420EOA	Noninverting	8-Pin SOIC	–40°C to +85°C
TC4420IJA	Noninverting	8-Pin CerDIP	–25°C to +85°C
TC4420MJA	Noninverting	8-Pin CerDIP	–55°C to +125°C
TC4420CAT	Noninverting	5-Pin TO-220	0°C to +70°C
TC4429CPA	Inverting	8-Pin PDIP	0°C to +70°C
TC4429EPA	Inverting	8-Pin PDIP	–40°C to +85°C
TC4429COA	Inverting	8-Pin SOIC	0°C to +70°C
TC4429EOA	Inverting	8-Pin SOIC	–40°C to +85°C
TC4429IJA	Inverting	8-Pin CerDIP	–25°C to +85°C
TC4429MJA	Inverting	8-Pin CerDIP	–55°C to +125°C
TC4429CAT	Inverting	5-Pin TO-220	0°C to +70°C

PIN CONFIGURATIONS



NOTE: Duplicate pins must *both* be connected for proper operation.

6A HIGH-SPEED MOSFET DRIVERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +20V
Input Voltage .... –5V to >V_{DD}
Input Current (V_{IN} > V_{DD}) .... 50 mA
Power Dissipation, $T_A \leq 25°C$
  PDIP 1W
  SOIC .... 500 mW
  CerDIP .... 800 mW
  5-Pin TO-220 .... 1.5W
Power Dissipation, $T_C \leq 25°C$
  5-Pin TO-220 .... 12.5W
Derating Factors (To Ambient)
  PDIP .... 8 mW/°C
  SOIC .... 4 mW/°C
  CerDIP .... 6.4 mW/°C
  5-Pin TO-220 .... 12 mW/°C
Thermal Impedances (To Case)
  5-Pin TO-220 $R_{\theta J\text{-}A}$ .... 10°C/W

Storage Temperature Range .... –55°C to +150°C
Operating Temperature (Chip) .... +150°C
Operating Temperature Range (Ambient)
  C Version .... 0°C to +70°C
  I Version .... –25°C to +85°C
  E Version .... –40°C to +85°C
  M Version .... –55°C to +125°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0 Low Input Voltage		—	1.3	0.8	V
V_{IN} (Max)	Input Voltage Range		–5	—	V_{DD}+0.3	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	—	10	μA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.1	2.8	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	1.5	2.5	Ω
I_{PK}	Peak Output Current	V_{DD} = 18V (See Figure 5)	—	6	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 μs	>1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1	—	55	75	ns
t_{D2}	Delay Time	Figure 1	—	55	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V	— —	0.45 55	1.5 150	mA μA
V_{DD}	Operating Input Voltage		4.5	—	18	V

TC4420
TC4429

ELECTRICAL CHARACTERISTICS:

Measured over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
V_{IN} (Max)	Input Voltage Range		–5	—	V_{DD}+0.3	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	–10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	3	5	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.3	5	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	32	60	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	34	60	ns
t_{D1}	Delay Time	Figure 1	—	50	100	ns
t_{D2}	Delay Time	Figure 1	—	65	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V	— —	0.45 60	3 400	mA µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.

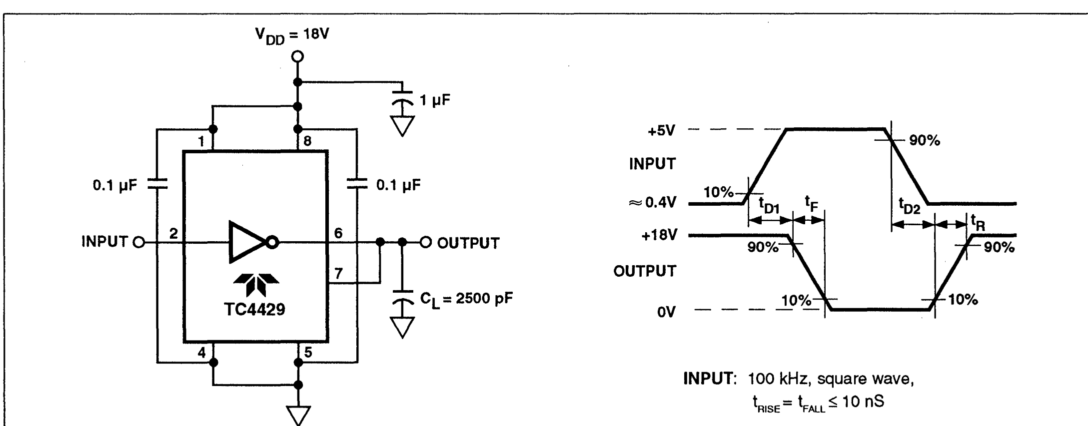
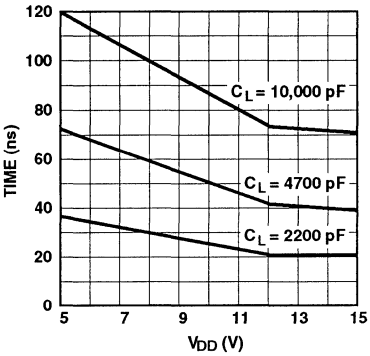


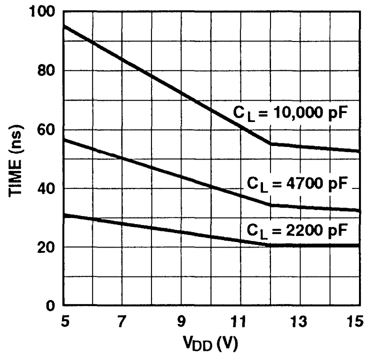
Figure 1. Switching Time Test Circuit

TYPICAL CHARACTERISTICS CURVES

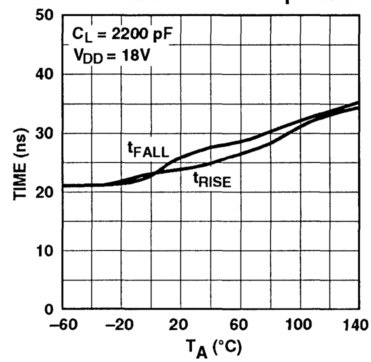
Rise Time vs Supply Voltage



Fall Time vs Supply Voltage



Rise and Fall Times vs Temperature



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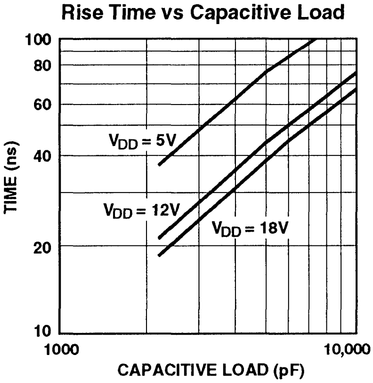
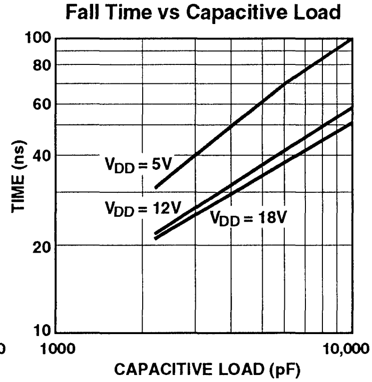
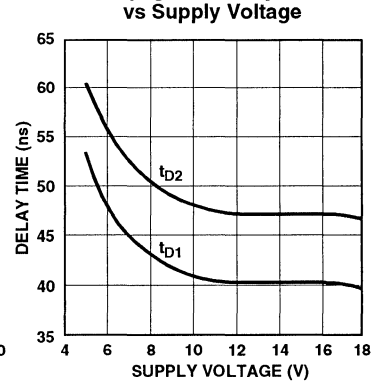
Rise Time vs Capacitive Load



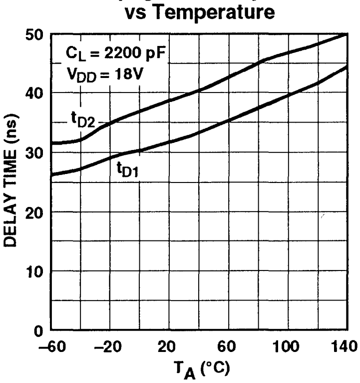
Fall Time vs Capacitive Load



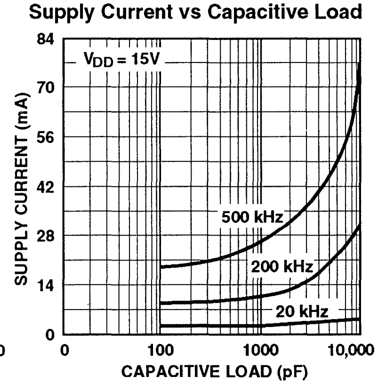
Propagation Delay Time vs Supply Voltage



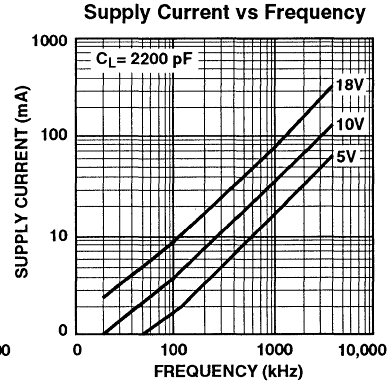
Propagation Delay Time vs Temperature



Supply Current vs Capacitive Load



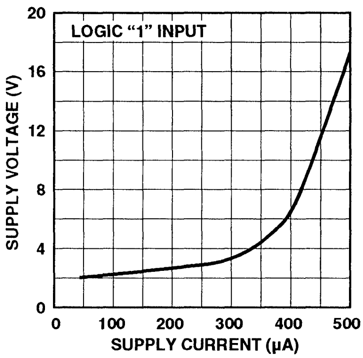
Supply Current vs Frequency



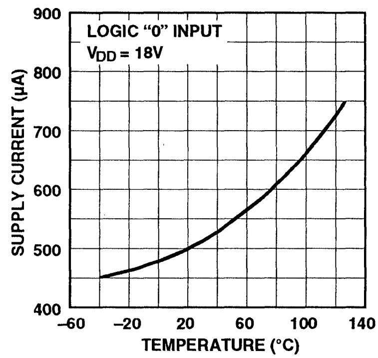
TC4420
TC4429

TYPICAL CHARACTERISTICS CURVES (Cont.)

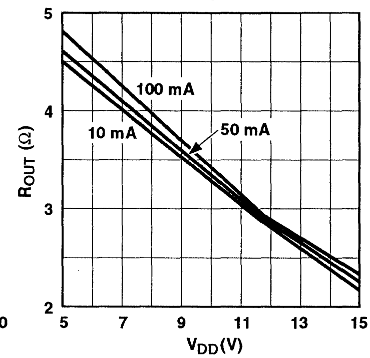
Quiescent Power Supply Current vs Supply Voltage



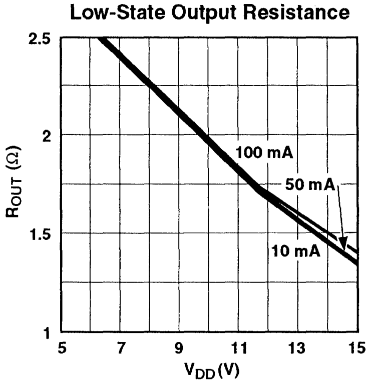
Quiescent Power Supply Current vs Temperature



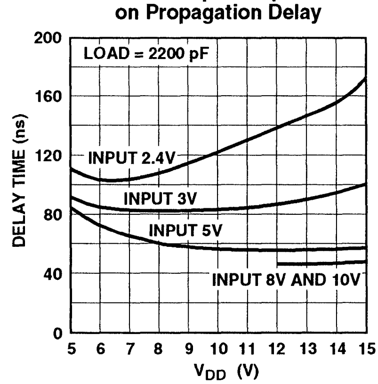
High-State Output Resistance



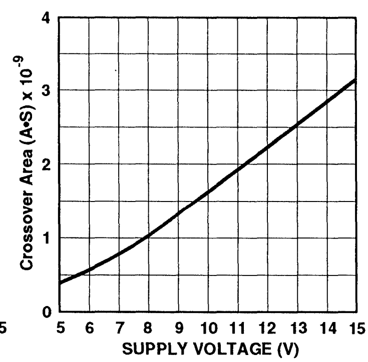
Low-State Output Resistance



Effect of Input Amplitude on Propagation Delay

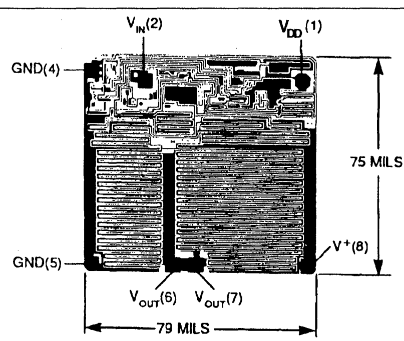


Total nA•S Crossover*



* The values on this graph represent the loss seen by the driver during one complete cycle. For a single transition, divide the value by 2.

BONDING DIAGRAM



NOTES: 1. Backside of die is common to V_{DD}.
2. Backside of die is not metallized.

TELEDYNE COMPONENTS

TC4421
TC4422

9A HIGH-SPEED FET DRIVER

FEATURES

- **Tough CMOS™ Construction**
- **High Peak Output Current 9A**
- **High Continuous Output Current .... 2A Max**
- **Fast Rise and Fall Times:**
  — 30 ns with 4,700 pF Load
  — 180 ns with 47,000 pF Load
- **Short Internal Delays .... 30 ns Typ**

APPLICATIONS

- **Line Drivers for Extra-Heavily-Loaded Lines**
- **Pulse Generators**
- **Driving Huge MOSFETs and IGBTs**
- **Local Power ON/OFF Switch**
- **Motor and Solenoid Driver**

GENERAL DESCRIPTION

The TC4421/4422 are large buffer/drivers built using Teledyne Components' proprietary Tough CMOS process. They can drive the largest MOSFETs and IGBTs now produced (including parallel-chip modules) at speeds up to the megahertz region while delivering the same fast rise and fall times and short delay intervals users expect from Teledyne's drivers.

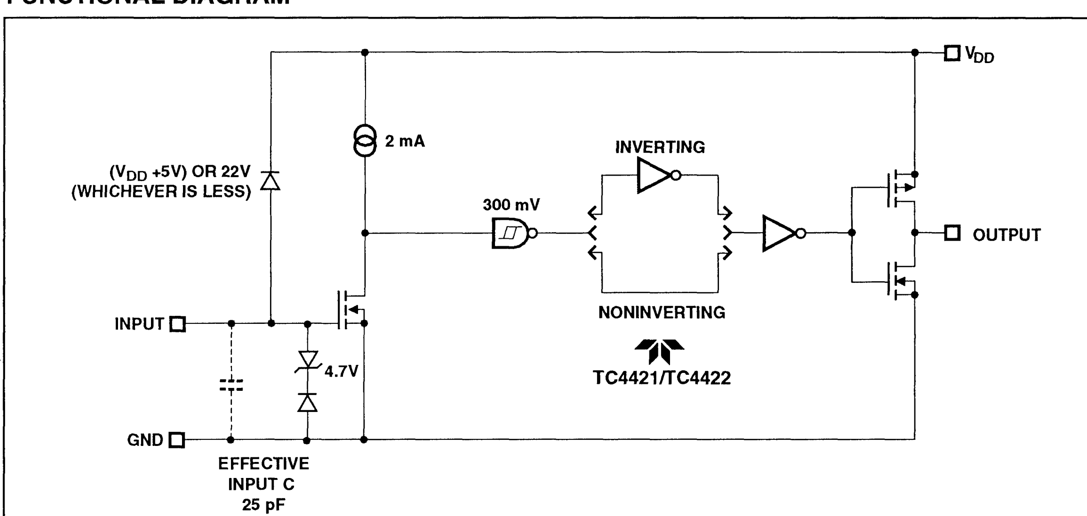
The drivers are essentially immune to any form of upset except direct overvoltage or over-dissipation — they cannot be latched under any conditions within their power and voltage ratings; they are not subject to damage or improper operation when up to 5V of ground bounce is present on their ground terminals; they can accept, without either damage or logic upset, more than 1A inductive current of either polarity being forced back into their outputs. In addition, all terminals are fully protected against up to 4 kV of electrostatic discharge.

As a result, the TC4421/4422 drivers are much easier to use, more flexible in operation, and much more forgiving than any other available driver — CMOS or bipolar. Because they are fabricated in CMOS, they dissipate minimum power and provide rail-to-rail output swings, assuring complete power to whatever they drive.

The maximum output swing, 18V, is sufficient to drive even insensitively-gated IGBTs, while the peak current capability allows capacitive loads up to 0.1 µF to be charged and discharged very rapidly.

6

FUNCTIONAL DIAGRAM



9A HIGH-SPEED FET DRIVER

TC4421
TC4422

As MOSFET drivers, the TC4421/4422 can drive the largest single-die MOSFET available and produce rise and fall times of less than 50 ns. Driving the largest parallel-chip MOSFET modules, they can produce rise and fall times of less than 150 ns. They also provide sufficiently low impedance in both the ON and OFF states to ensure that a MOSFET's or IGBT's intended state is not disturbed, even by large voltage transients.

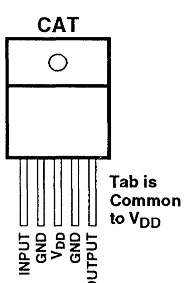
In addition, low output impedance (1.4Ω typ), high continuous current capacity (2A), and inherent general ruggedness make them useful in situations where a DC load must be switched on and off rapidly, such as in RF pulsers and laser drives. They are also suitable for driving a nearly endless variety of other loads, including long data lines, small motors, solenoids, piezo elements, or virtually any other load — capacitive, inductive, or resistive.

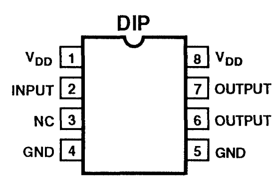
The TC4421/4422 inputs may be driven directly from either TTL or CMOS (3V to 18V). In addition, 300 mV of input hysteresis is built into the input, providing noise immunity and allowing the device to be driven from slowly rising or falling waveforms.

ORDERING INFORMATION

Part No.	Logic	Package	Temperature Range
TC4421CPA	Inverting	8-Pin PDIP	0°C to +70°C
TC4421EPA	Inverting	8-Pin PDIP	–40°C to +85°C
TC4421MJA	Inverting	8-Pin CerDIP	–55°C to +125°C
TC4421CAT	Inverting	5-Pin TO-220	0°C to +70°C
TC4422CPA	Non-Inverting	8-Pin PDIP	0°C to +70°
TC4422EPA	Non-Inverting	8-Pin PDIP	–40°C to +85°C
TC4422MJA	Non-Inverting	8-Pin CerDIP	–55°C to +125°C
TC4422CAT	Non-Inverting	5-Pin TO-220	0°C to +70°C

PIN CONFIGURATIONS





NOTE: Duplicate pins must *both* be connected for proper operation.
NC = No connection

ABSOLUTE MAXIMUM RATINGS

Power Dissipation, $T_A \leq 25°C$
- PDIP 1W
- CerDIP .... 800 mW
- 5-Pin TO-220 .... 1.5W

Power Dissipation, $T_C \leq 25°C$
- 5-Pin TO-220 .... 12.5W

Derating Factors (To Ambient)
- PDIP .... 8 mW/°C
- CerDIP .... 6.4 mW/°C
- 5-Pin TO-220 .... 12 mW/°C

Thermal Impedance (To Case)
- 5-Pin TO-220 $R_{\Theta J\text{-}A}$ .... 10°C/W

Storage Temperature .... –65°C to +150°C
Operating Temperature (Chip) .... 150°C
Operating Temperature (Ambient)
- C Version .... 0°C to +70°C
- E Version...................... –40°C to +85°C
- M Version .... –55°C to +125°C

Lead Temperature (10 sec) .... 300°C
Supply Voltage 20V
Input Voltage .... V_{DD} + 0.3V to GND - 5V
Input Current ($V_{IN} > V_{DD}$) .... 50 mA

6

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C with 4.5V ≤ V_{DD} ≤ 18V unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0 Input Voltage		—	1.3	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	V_{DD} = 18V, I_O = 10 mA	—	1.4	—	Ω
R_O	Output Resistance, Low	V_{DD} = 18V, I_O = 10 mA	—	0.9	1.7	Ω
I_{PK}	Peak Output Current	V_{DD} = 18V	—	9	—	A
I_{DC}	Continuous Output Current		2			A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>1500	—	—	mA
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 10,000 pF	—	60	75	ns
t_F	Fall Time	Figure 1, C_L = 10,000 pF	—	60	75	ns
t_{D1}	Delay Time	Figure 1	—	30	60	ns
t_{D2}	Delay Time	Figure 1	—	33	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	0.2	1.5	mA
		V_{IN} = 0V	—	55	150	µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

ELECTRICAL CHARACTERISTICS

(Measured over operating temperature range with 4.5V ≤ V_S ≤ 18V unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	V_{DD} = 18V, I_O = 10 mA	—	2.4	3.6	Ω
R_O	Output Resistance, Low	V_{DD} = 18V, I_O = 10 mA	—	1.8	2.7	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 10,000 pF	—	60	120	ns
t_F	Fall Time	Figure 1, C_L = 10,000 pF	—	60	120	ns
t_{D1}	Delay Time	Figure 1	—	50	80	ns
t_{D2}	Delay Time	Figure 1	—	65	80	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V	—	0.45	3	mA
		V_{IN} = 0V	—	0.06	0.2	mA
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.

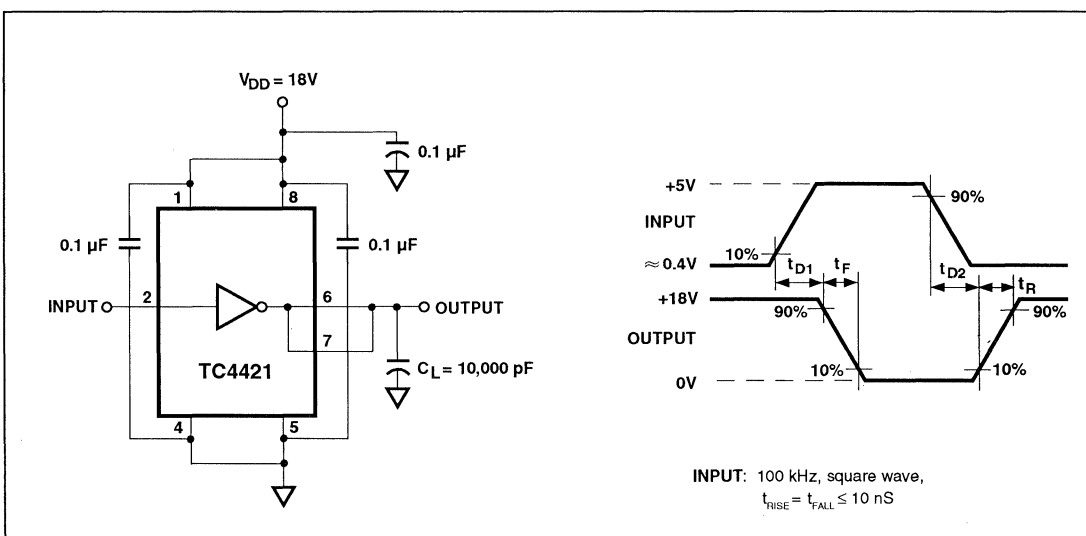
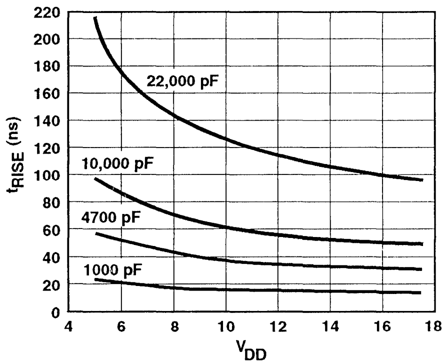


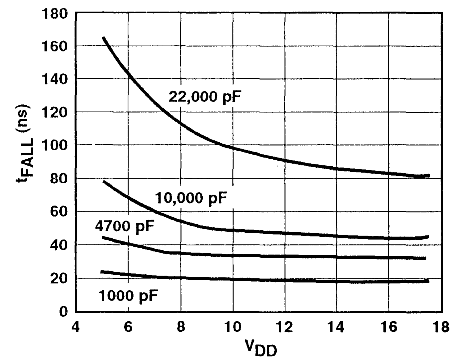
Figure 1. Switching Time Test Circuit

TYPICAL CHARACTERISTIC CURVES

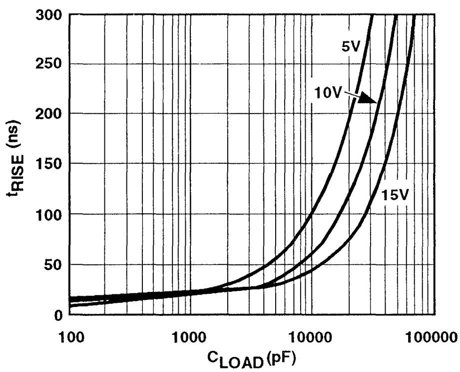
Rise Time vs Supply Voltage



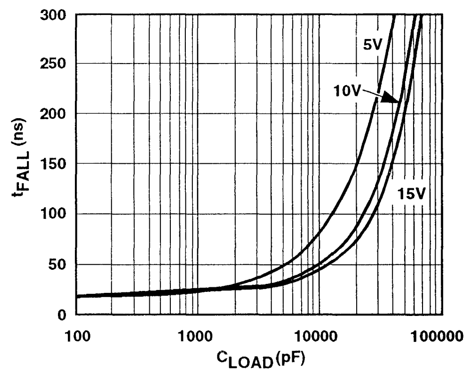
Fall Time vs Supply Voltage



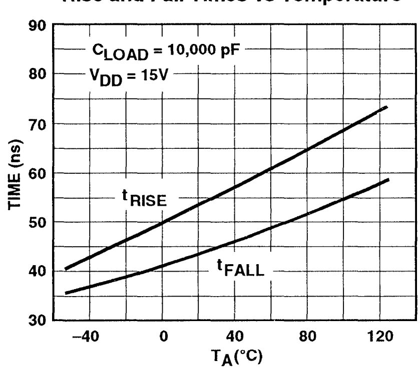
Rise TIme vs Capacitive Load



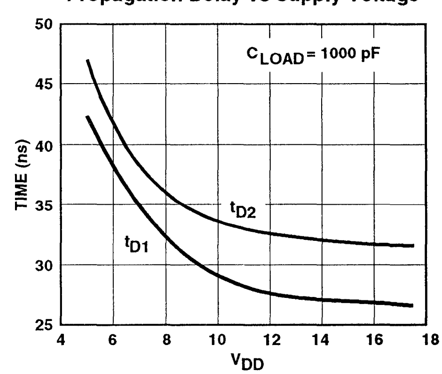
Fall TIme vs Capacitive Load



Rise and Fall Times vs Temperature

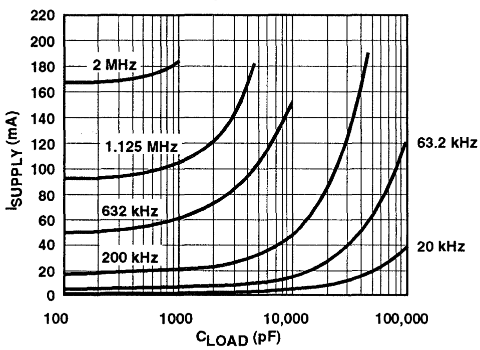


Propagation Delay vs Supply Voltage

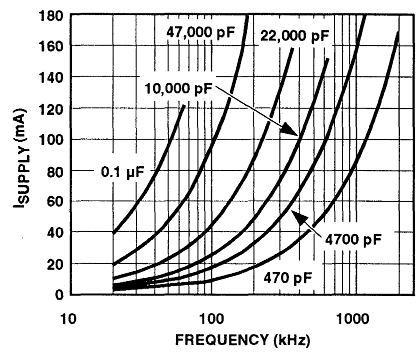


TYPICAL CHARACTERISTIC CURVES (Cont.)

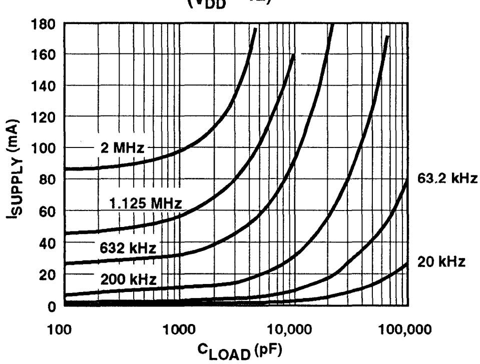
Supply Current vs Capacitive Load
(V_{DD} = 18V)



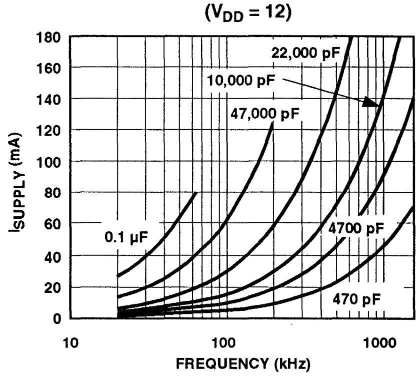
Supply Current vs Frequency
(V_{DD} = 18V)



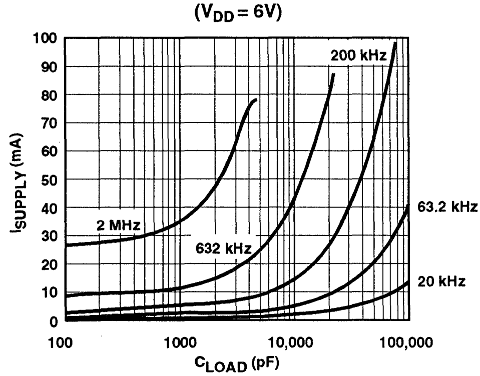
Supply Current vs Capacitive Load,
(V_{DD} = 12)



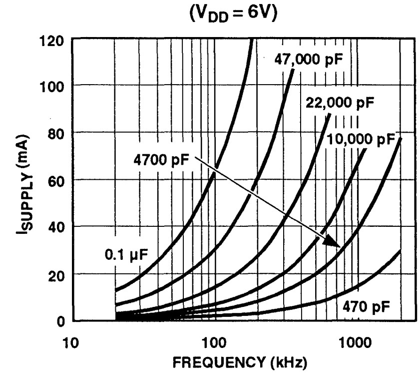
Supply Current vs Frequency
(V_{DD} = 12)



Supply Current vs Capacitive Load
(V_{DD} = 6V)

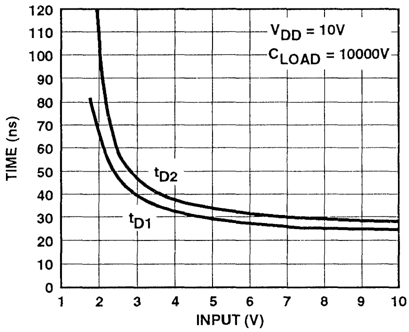


Supply Current vs Frequency
(V_{DD} = 6V)

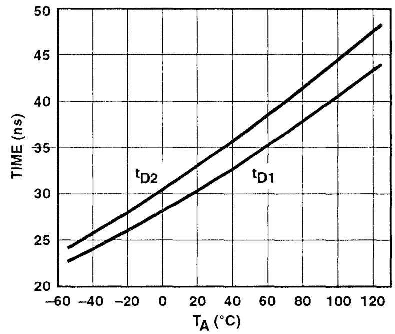


TYPICAL CHARACTERISTIC CURVES (Cont.)

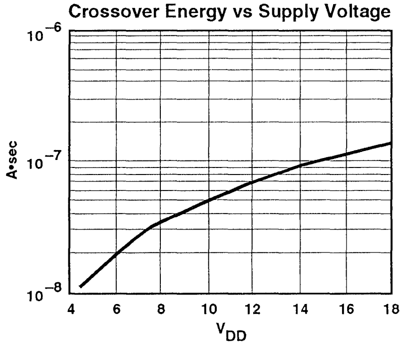
Propagation Delay vs Input Amplitude



Propagation Delay vs Temperature

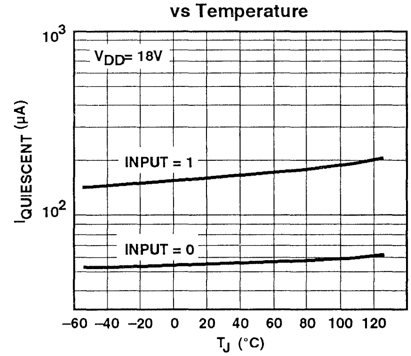


Crossover Energy vs Supply Voltage

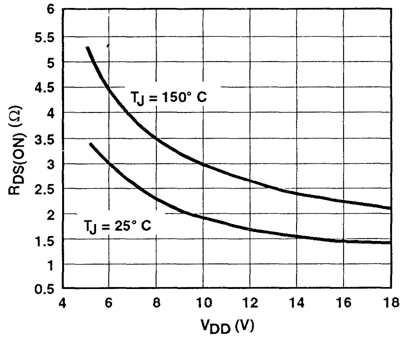


NOTE: The values on this graph represent the loss seen by the driver during a complete cycle. For the loss in a single transition, divide the stated value by 2.

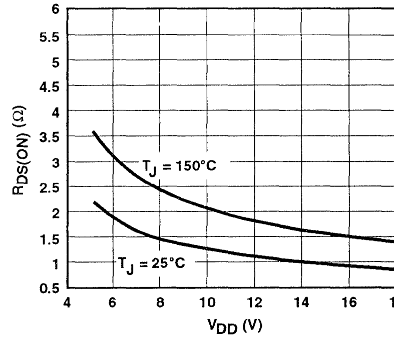
Quiescent Supply Current vs Temperature



High-State Output Resistance vs Supply Voltage



Low-State Output Resistance vs Supply Voltage



NOTES

TELEDYNE COMPONENTS

TC4423
TC4424
TC4425

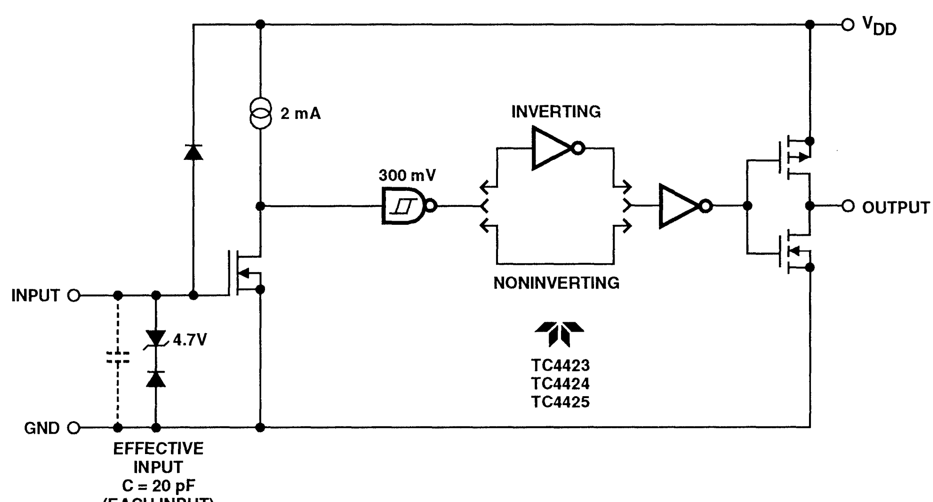
3A DUAL HIGH-SPEED MOSFET DRIVERS

FEATURES

- Tough CMOS™ Construction
- Latch-Up Protected: Will Withstand 1.5A Reverse Current
- Logic Input Will Withstand Negative Swing Up to 5V
- ESD Protected .... 4 kV
- High Peak Output Current 3A
- Wide Operating Range .... 4.5V to 18V
- High Capacitive Load Drive Capability .... 1800 pF in 25 ns
- Short Delay Times .... <40 ns Typ
- Consistent Delay Times With Changes in Supply Voltage
- Matched Rise/Fall Times
- Logic High Input, Any Voltage .... 2.4V to V_{DD}
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - — With Logic "1" Input .... 3.5 mA
  - — With Logic "0" Input .... 350 μA
- Low Input Impedance .... 3.5W Typ
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}
- Pinouts Same as TC1426/27/28; TC4426/27/28
- Available in Inverting, Noninverting, and Differential Configurations

6

FUNCTIONAL DIAGRAM



NOTES: 1. TC4425 has one inverting and one noninverting driver.
2. Ground any unused driver input.

3A DUAL HIGH-SPEED MOSFET DRIVERS

GENERAL DESCRIPTION

The TC4423/4424/4425 are CMOS buffer/drivers built using Teledyne Components' new Tough CMOS process. They are higher output current versions of the new TC4426/4427/4428 buffer/drivers, which, in turn, are improved versions of the earlier TC426/427/428 series. All three families are pin-compatible. The TC4423/4424/4425 drivers are capable of giving reliable service in far more demanding electrical environments than their antecedents. They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage, even when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without either damage or logic upset, up to 1.5A of reverse current (of either polarity) being forced back into their outputs. All terminals are also fully protected against up to 4 kV of electrostatic discharge.

As a result, the TC4423/4424/4425 drivers are much easier to use, more flexible in operation, and much more forgiving than any other drivers (CMOS or bipolar) currently available. Because they are fabricated in CMOS, they dissipate a minimum of power and provide rail-to-rail voltage swings to better ensure the logic state of any load they drive.

Although primarily intended for driving power MOSFETs, the TC4423/4424/4425 drivers are equally well-suited to driving any other load (capacitive, resistive, or inductive) which requires a low impedance driver capable of high peak currents and fast switching times. For example, heavily loaded clock lines, coaxial cables, or piezoelectric transducers can all be driven from the TC4423/4424/4425. The only known limitation on loading is the total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

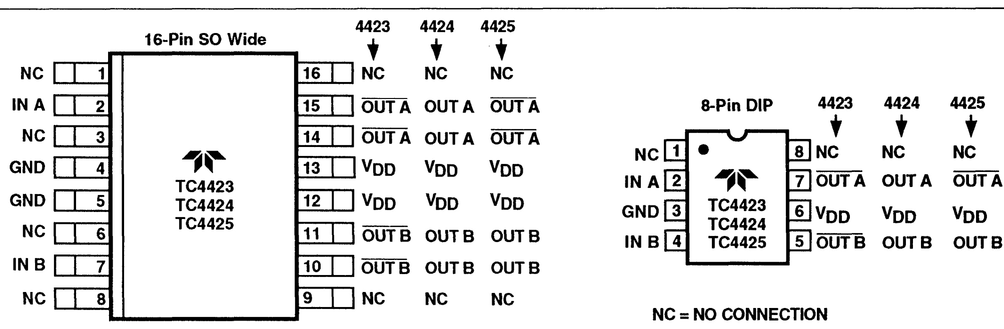
As MOSFET drivers, the TC4423/4424/4425 can easily switch 1800 pF gate capacitances in under 30 ns, and provide low enough impedances in both the ON and OFF states to ensure the MOSFET's intended state will not be affected, even by large transients.

The TC4423/4424/4425 design has taken into account five years of field use (and abuse) of our earlier parts, with the goal of making these drivers immune to all forms of improper operation known from that period, except exceeding the breakdown voltage and power dissipation ratings. We believe we have succeeded.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4423COE	16-Pin SO Wide	0°C to +70°C
TC4423CPA	8-Pin Plastic DIP	0°C to +70°C
TC4423IJA	8-Pin CerDIP	–25°C to +85°C
TC4423MJA	8-Pin CerDIP	–55°C to +125°C
TC4423EOE	16-Pin SO Wide	–40°C to +85°C
TC4423EPA	8-Pin Plastic DIP	–40°C to +85°C
TC4424COE	16-Pin SO Wide	0°C to +70°C
TC4424CPA	8-Pin Plastic DIP	0°C to +70°C
TC4424IJA	8-Pin CerDIP	–25°C to +85°C
TC4424MJA	8-Pin CerDIP	–55°C to +125°C
TC4424EOE	16-Pin SO Wide	–40°C to +85°C
TC4424EPA	8-Pin Plastic DIP	–40°C to +85°C
TC4425COE	16-Pin SO Wide	0°C to +70°C
TC4425CPA	8-Pin Plastic DIP	0°C to +70°C
TC4425IJA	8-Pin CerDIP	–25°C to +85°C
TC4425MJA	8-Pin CerDIP	–55°C to +125°C
TC4425EOE	16-Pin SO Wide	–40°C to +85°C
TC4425EPA	8-Pin Plastic DIP	–40°C to +85°C

PIN CONFIGURATIONS



NOTE: Duplicate pins must **both** be connected for proper operation.

3A DUAL HIGH-SPEED MOSFET DRIVERS

TC4423
TC4424
TC4425

ABSOLUTE MAXIMUM RATINGS

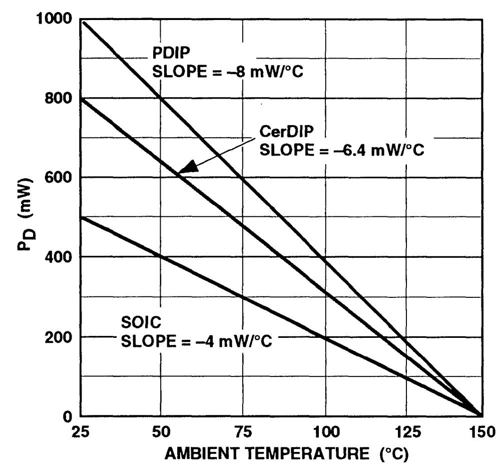
Supply Voltage ....+22V
Input Voltage, IN A or IN B .... V_{DD} + 0.3V to GND –5.0V
Maximum Chip Temperature .... +150°C
Storage Temperature Range.................. –65°C to +150°C
Lead Temperature (Soldering, 10 sec)................. +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J\text{-}A}$ .... 150°C/W
- CerDIP $R_{\theta J\text{-}C}$ .... 55°C/W
- PDIP $R_{\theta J\text{-}A}$ .... 125°C/W
- PDIP $R_{\theta J\text{-}C}$ .... 45°C/W
- SOIC $R_{\theta J\text{-}A}$ .... 250°C/W
- SOIC $R_{\theta J\text{-}C}$ .... 75°C/W

Operating Temperature Range
- C Version .... 0°C to +70°C
- I Version .... –25°C to +85°C
- E Version .... –40°C to +85°C
- M Version .... –55°C to +125°C

Power Dissipation
- Plastic DIP .... 1000 mW
- CerDIP .... 800 mW
- SOIC .... 500 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Package Power Dissipation



ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{OH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.8	5	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	3.5	5	Ω
I_{PK}	Peak Output Current		—	3	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	23	35	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	33	75	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	38	75	ns

ELECTRICAL CHARACTERISTICS:

Over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	3.7	8	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	4.3	8	Ω
I_{PK}	Peak Output Current		—	3	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 1800 pF	—	28	60	ns
t_F	Fall Time	Figure 1, C_L = 1800 pF	—	32	60	ns
t_{D1}	Delay Time	Figure 1, C_L = 1800 pF	—	32	100	ns
t_{D2}	Delay Time	Figure 1, C_L = 1800 pF	—	38	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	2	3.5	mA
		V_{IN} = 0V (Both Inputs)	—	0.2	0.3	mA

NOTE: 1. Switching times guaranteed by design.

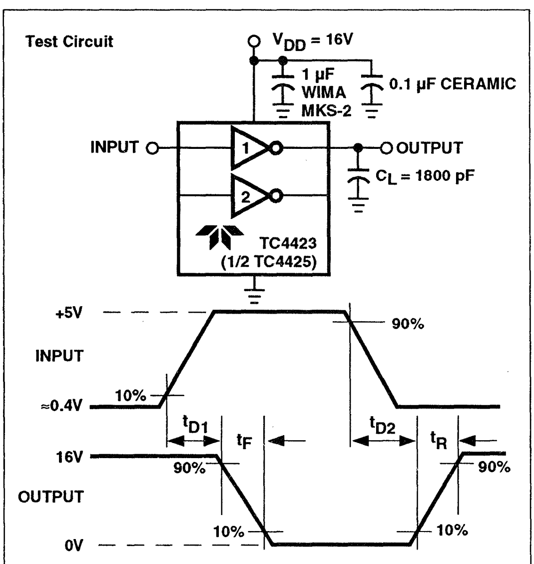


Figure 1 Inverting Driver Switching Time

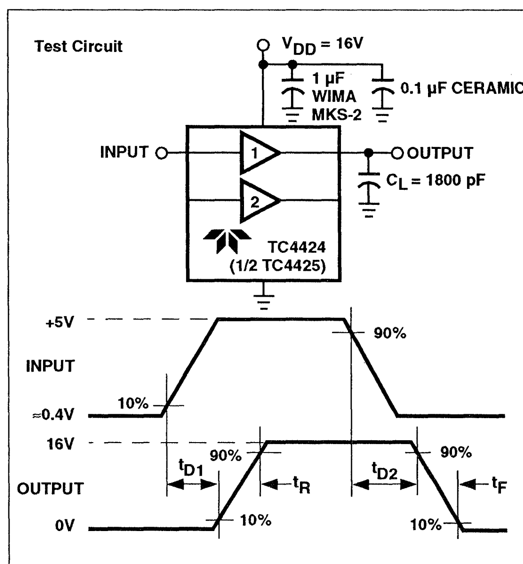
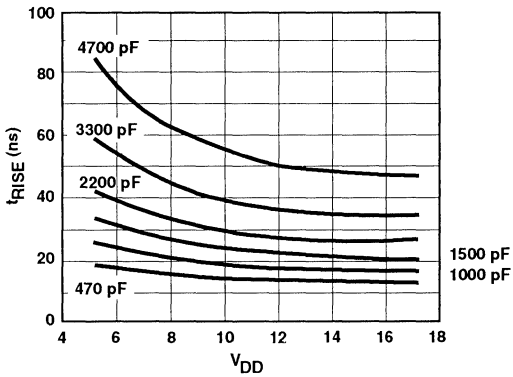


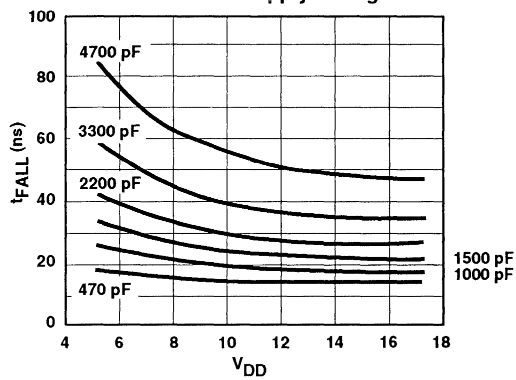
Figure 2 Noninverting Driver Switching Time

TYPICAL CHARACTERISTICS CURVES

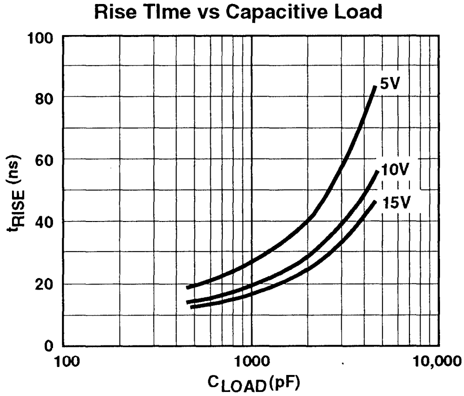
Rise Time vs Supply Voltage



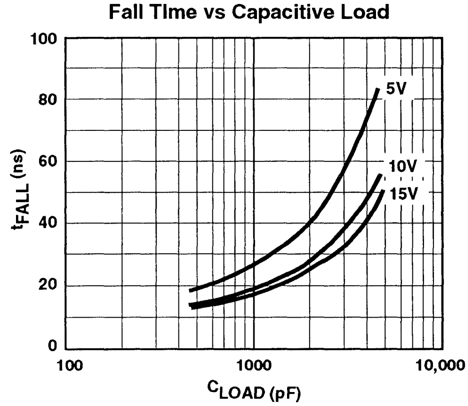
Fall Time vs Supply Voltage



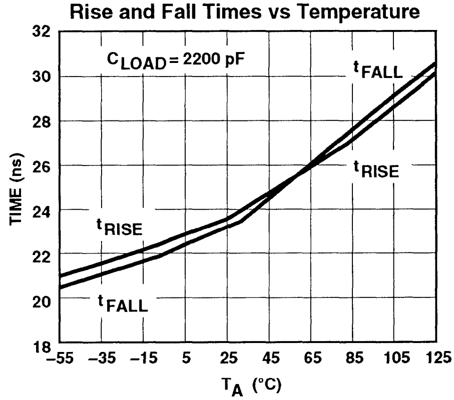
Rise Time vs Capacitive Load



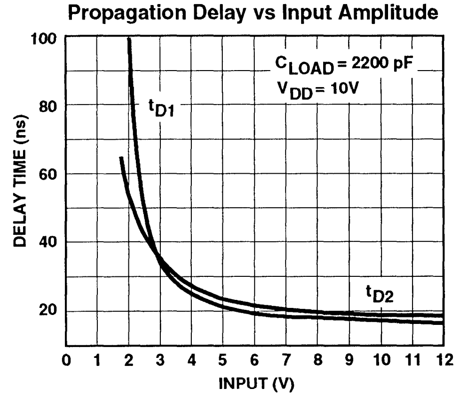
Fall Time vs Capacitive Load



Rise and Fall Times vs Temperature

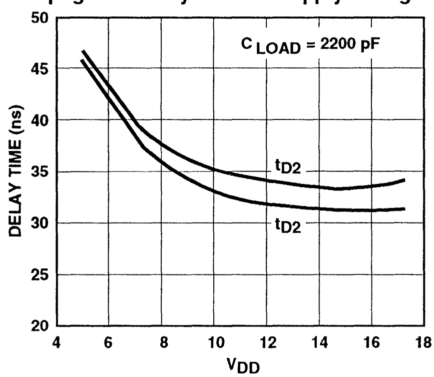


Propagation Delay vs Input Amplitude

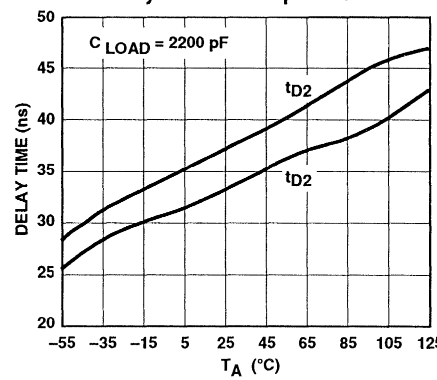


TYPICAL CHARACTERISTICS CURVES (Cont.)

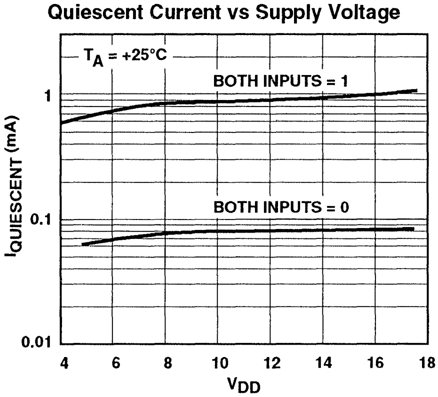
Propagation Delay Time vs Supply Voltage



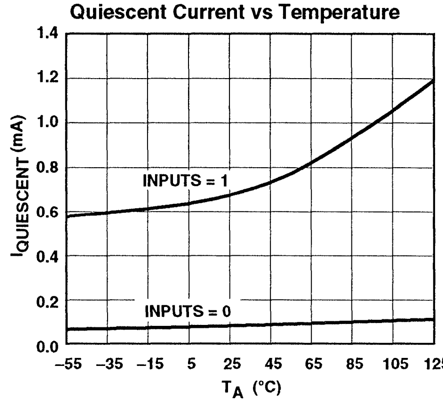
Delay Time vs Temperature



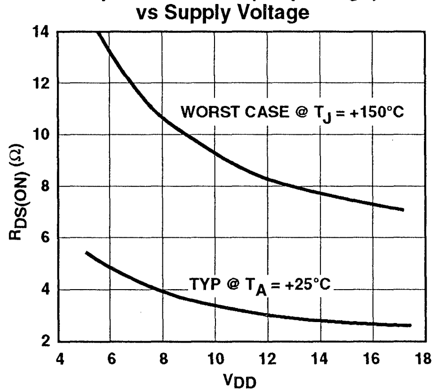
Quiescent Current vs Supply Voltage



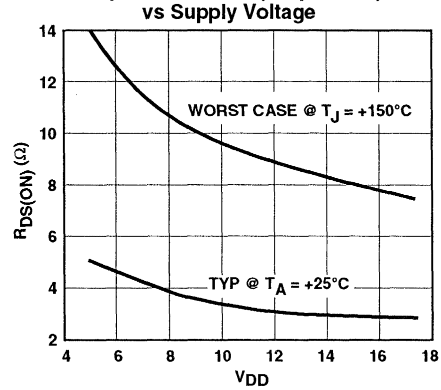
Quiescent Current vs Temperature



Output Resistance (Output High) vs Supply Voltage



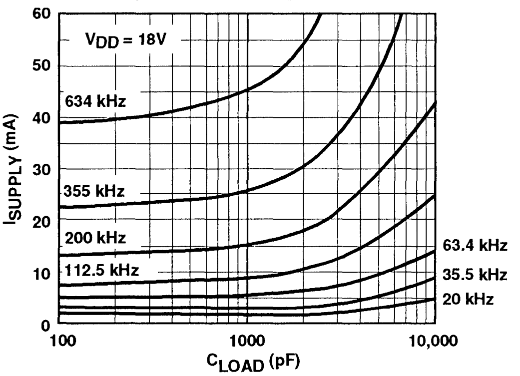
Output Resistance (Output Low) vs Supply Voltage



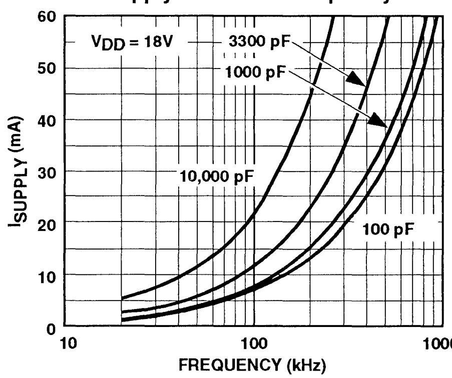
6

SUPPLY CURRENT CHARACTERISTICS (Load on Single Output Only)

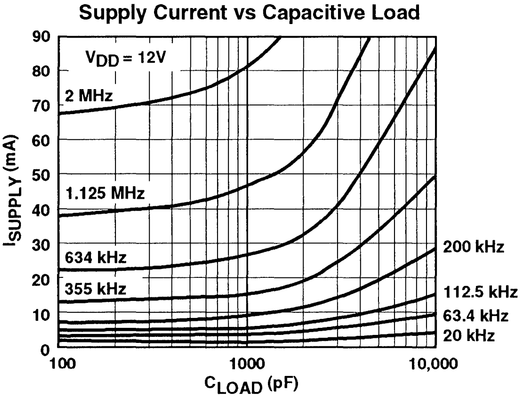
Supply Current vs Capacitive Load



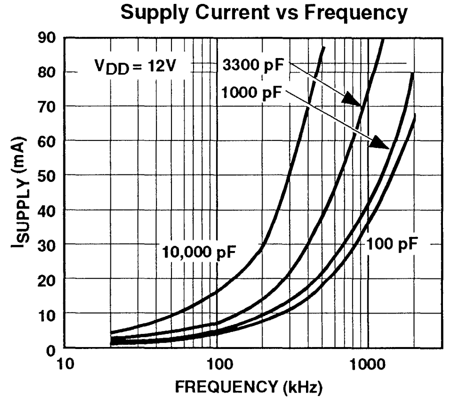
Supply Current vs Frequency



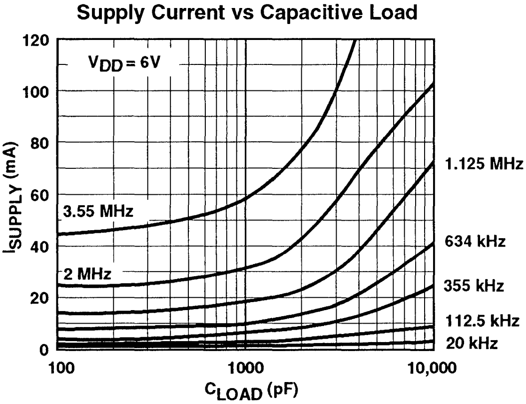
Supply Current vs Capacitive Load



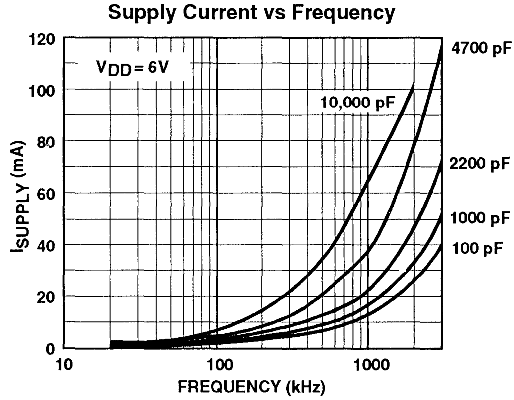
Supply Current vs Frequency



Supply Current vs Capacitive Load



Supply Current vs Frequency



NOTES

TELEDYNE COMPONENTS

TC4426
TC4427
TC4428

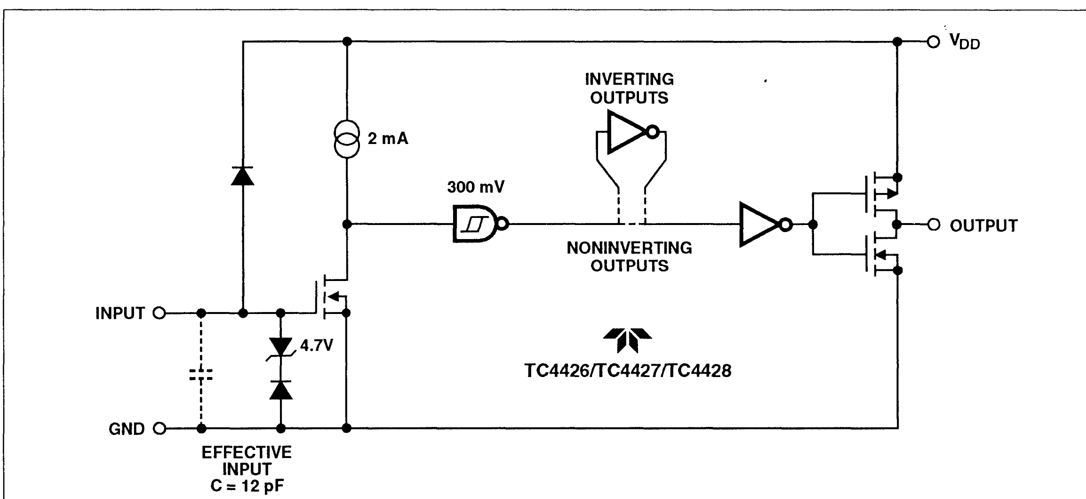
1.5A DUAL HIGH-SPEED FET DRIVERS

FEATURES

- Tough CMOS™ Construction
- Latch-Up Protected: Will Withstand >0.5A Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- ESD Protected .... 4 kV
- High Peak Output Current 1.5A
- Wide Operating Range .... 4.5V to 18V
- High Capacitive Load Drive Capability .... 1000 pF in 25 ns
- Short Delay Time .... <40 ns Typ
- Consistent Delay Times With Changes in Supply Voltage
- Matched Rise and Fall Times
- Logic High Input for Any Voltage From 2.4V to V_{DD}
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - — With Logic "1" Input .... 4 mA
  - — With Logic "0" Input .... 400 µA
- Low Output Impedance 7Ω
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}
- Pinout Same as TC426/TC427/TC428
- Available in Inverting, Noninverting, and Differential Configurations

6

FUNCTIONAL DIAGRAM



NOTES: 1. TC4428 has one inverting and one noninverting driver.
2. Ground any unused driver input.

TC4426
TC4427
TC4428

GENERAL DESCRIPTION

The TC4426/4427/4428 are CMOS buffer/drivers built using Teledyne Components' new Tough CMOS process. They are improved versions of the earlier TC426/427/428 family of buffer/drivers (with which they are pin compatible) and are capable of giving reliable service in far more demanding electrical environments. They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 4 kV of electrostatic discharge.

In addition, Teledyne now uses a custom-developed molding epoxy for plastic packages which, in tests, produced zero device failures after 10,000 hours in an 85°C–85% R.H. environment, and contains 50% less sodium and chlorine contamination than standard commercial molding compounds, increasing device lifetimes.

As a result, the TC4426/4427/4428 drivers are much easier to use, more flexible in operation, and much more forgiving than any other drivers (CMOS or bipolar) currently available. Because they are fabricated in CMOS, they dissipate a minimum of power and provide rail-to-rail voltage swings to ensure the logic state of any load they are driving.

Although primarily intended for driving power MOSFETs, the TC4426/4427/4428 drivers are equally well-suited to driving any other load (capacitive, resistive, or inductive) which requires a low-impedance driver capable of high peak currents and fast switching times. For example, heavily loaded clock lines, coaxial cables, or piezoelectric transducers all can be driven from the TC4426/4427/4428. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

As MOSFET drivers, the TC4426/4427/4428 can easily switch 1000 pF gate capacitances in under 30 ns, and provide low enough impedances in both the ON and OFF states to ensure the MOSFET's intended state will not be affected, even by large transients.

Generally, the design of the TC4426/4427/4428 has taken into account 5 years of field use (and abuse) of Teledyne's earlier parts, with the goal of making these parts immune to all forms of improper operation known from that period, except exceeding the breakdown voltage and power dissipation ratings.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4426COA	8-Pin SOIC	0°C to +70°C
TC4426EOA	8-Pin SOIC	–40°C to +85°C
TC4426CPA	8-Pin Plastic DIP	0°C to +70°C
TC4426EPA	8-Pin Plastic DIP	–40°C to +85°C
TC4426EJA	8-Pin CerDIP	–40°C to +85°C
TC4426MJA	8-Pin CerDIP	–55°C to +125°C
TC4427COA	8-Pin SOIC	0°C to +70°C
TC4427EOA	8-Pin SOIC	–40°C to +85°C
TC4427CPA	8-Pin Plastic DIP	0°C to +70°C
TC4427EPA	8-Pin Plastic DIP	–40°C to +85°C
TC4427EJA	8-Pin CerDIP	–40°C to +85°C
TC4427MJA	8-Pin CerDIP	–55°C to +125°C
TC4428COA	8-Pin SOIC	0°C to +70°C
TC4428EOA	8-Pin SOIC	–40°C to +85°C
TC4428CPA	8-Pin Plastic DIP	0°C to +70°C
TC4428EPA	8-Pin Plastic DIP	–40°C to +85°C
TC4428EJA	8-Pin CerDIP	–40°C to +85°C
TC4428MJA	8-Pin CerDIP	–55°C to +125°C

1.5A DUAL HIGH-SPEED FET DRIVERS

TC4426
TC4427
TC4428

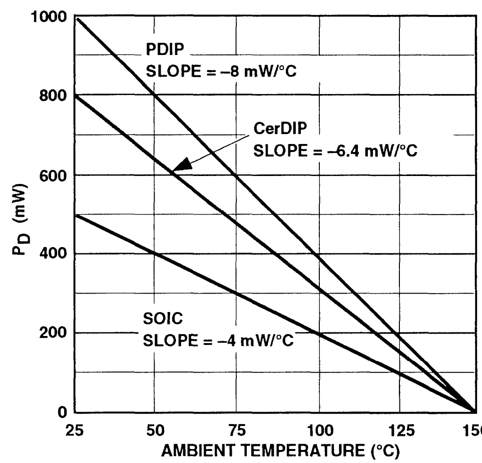
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ....+22V
Input Voltage, IN A or IN B .... V_{DD}+0.3V to GND–5.0V
Maximum Chip Temperature ....+150°C
Storage Temperature Range ....–65°C to +150°C
Lead Temperature (Soldering, 10 sec) ....+300°C
Package Thermal Resistance
- CerDIP $R_{\theta J\text{-}A}$ ....150°C/W
- CerDIP $R_{\theta J\text{-}C}$ ....50°C/W
- PDIP $R_{\theta J\text{-}A}$ ....125°C/W
- PDIP $R_{\theta J\text{-}C}$ ....42°C/W
- SOIC $R_{\theta J\text{-}A}$ ....250°C/W
- SOIC $R_{\theta J\text{-}C}$ ....75°C/W

Operating Temperature Range
- C Version ....0°C to +70°C
- E Version ....–40°C to +85°C
- M Version ....–55°C to +125°C

Power Dissipation
- Plastic ....1000 mW
- CerDIP ....800 mW
- SOIC ....500 mW

Package Power Dissipation



Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

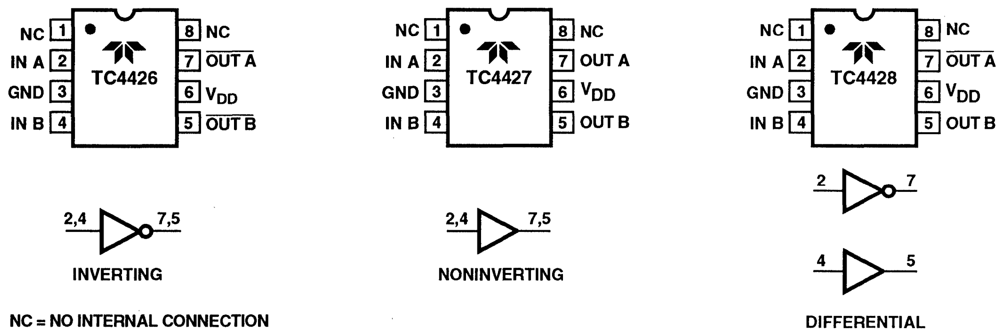
ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 18V, I_O = 10 mA	—	7	10	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>0.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1	—	25	30	ns
t_F	Fall Time	Figure 1	—	25	30	ns
t_{D1}	Delay Time	Figure 1	—	—	30	ns
t_{D2}	Delay Time	Figure 1	—	—	50	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	—	4.5	mA
		V_{IN} = 0V (Both Inputs)	—	—	0.4	mA

NOTE: 1. Switching times are guaranteed by design.

TC4426
TC4427
TC4428

PIN CONFIGURATIONS



NOTE: SOIC pinout is identical to DIP.

ELECTRICAL CHARACTERISTICS

Specifications measured over operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 18V, I_O = 10 mA	—	9	12	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>0.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1	—	—	40	ns
t_F	Fall Time	Figure 1	—	—	40	ns
t_{D1}	Delay Time	Figure 1	—	—	40	ns
t_{D2}	Delay Time	Figure 1	—	—	60	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	— —	8 0.6	mA mA

NOTE: 1. Switching times are guaranteed by design.

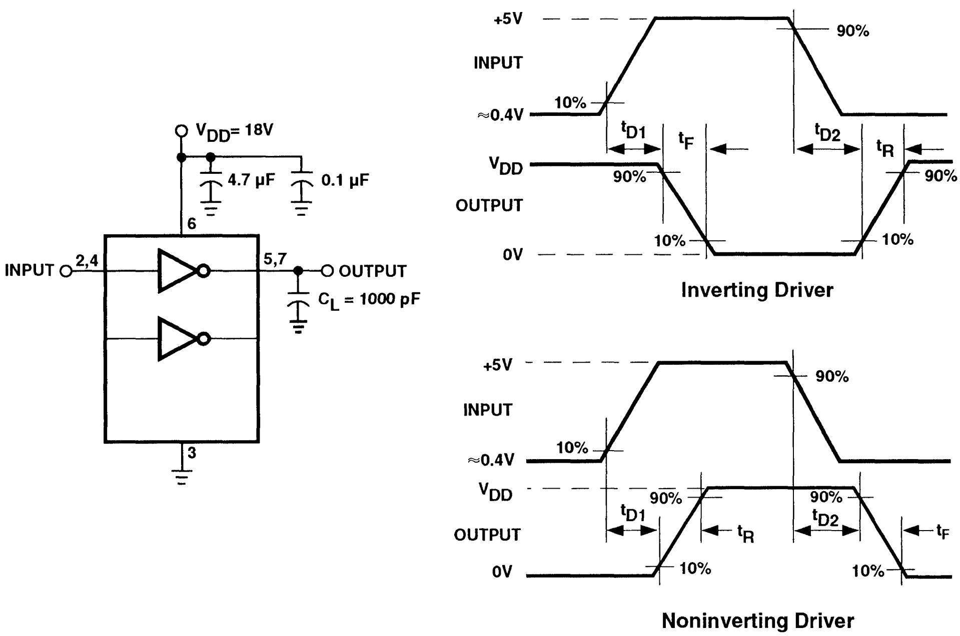
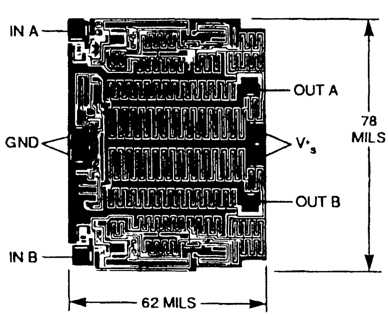
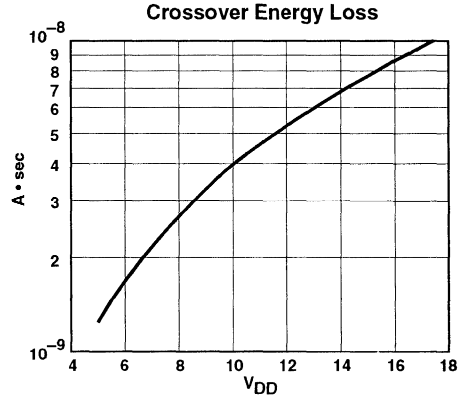


Figure 1. Switching Time Test Circuit

BONDING DIAGRAM



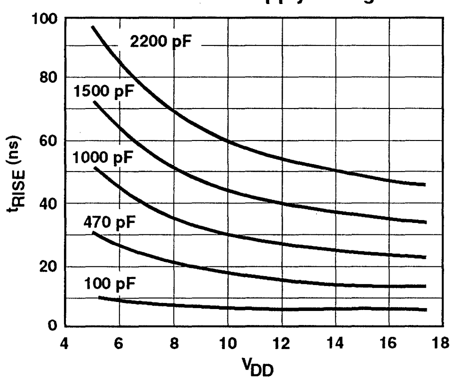
NOTES:
1. Back of die is common to V_{DD}.
2. Back of die is not metallized.



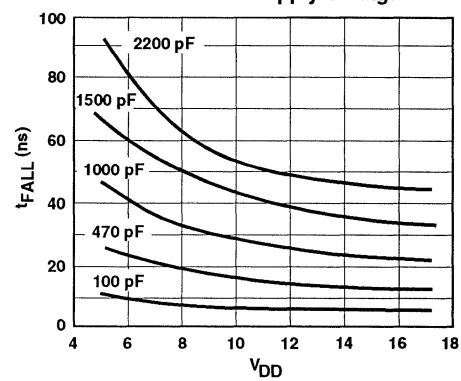
NOTE: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

TYPICAL CHARACTERISTICS CURVES

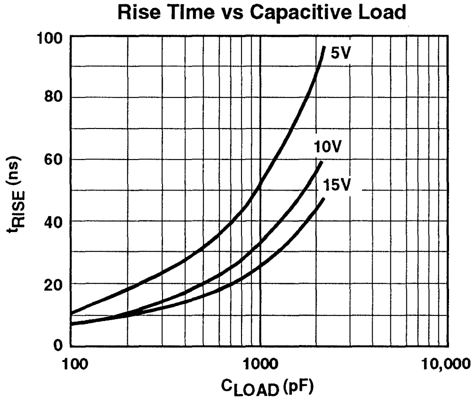
Rise Time vs Supply Voltage



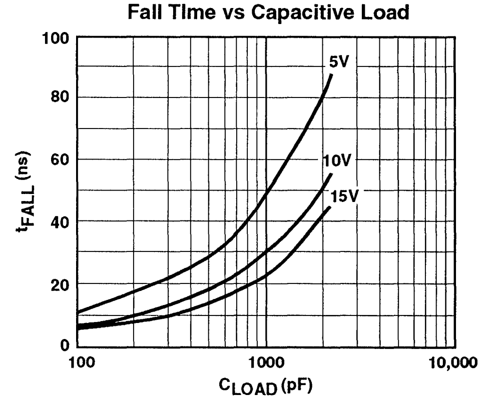
Fall Time vs Supply Voltage



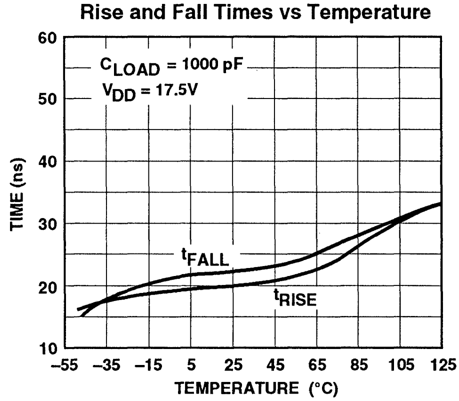
Rise Time vs Capacitive Load



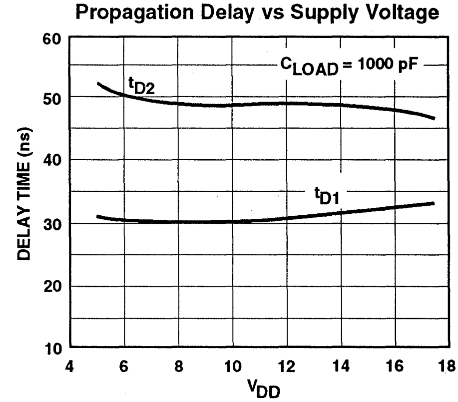
Fall Time vs Capacitive Load



Rise and Fall Times vs Temperature

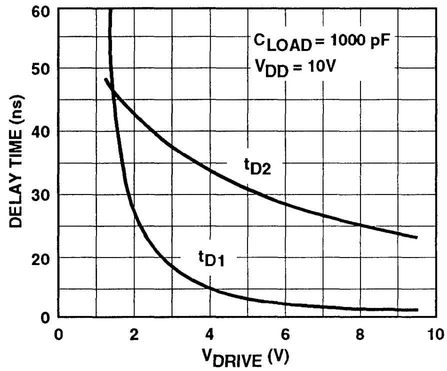


Propagation Delay vs Supply Voltage

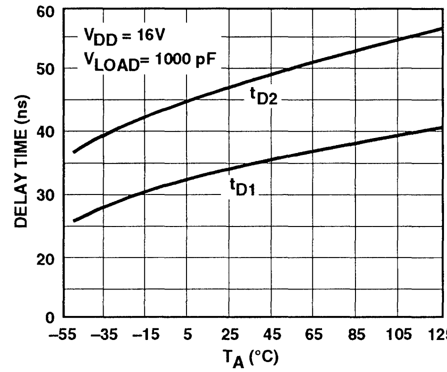


TYPICAL CHARACTERISTICS CURVES (Cont.)

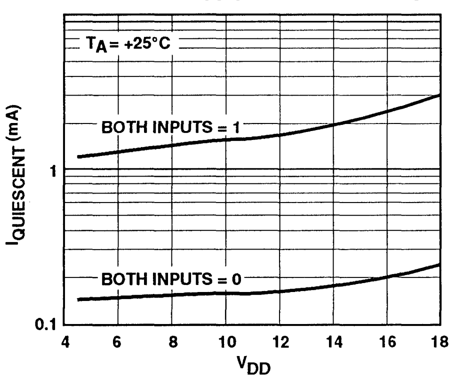
Effect of Input Amplitude on Delay Time



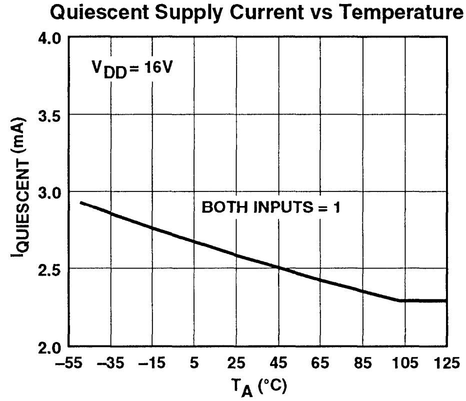
Propagation Delay Time vs Temperature



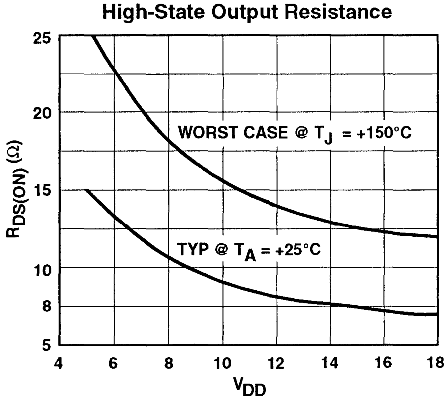
Quiescent Supply Current vs Voltage



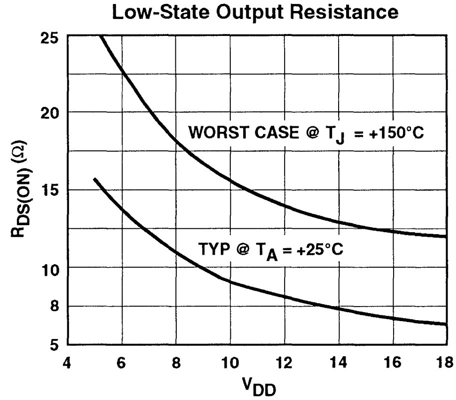
Quiescent Supply Current vs Temperature



High-State Output Resistance

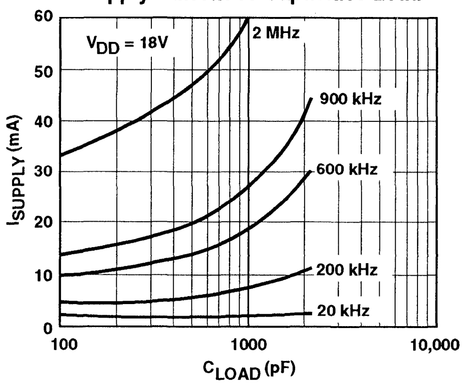


Low-State Output Resistance

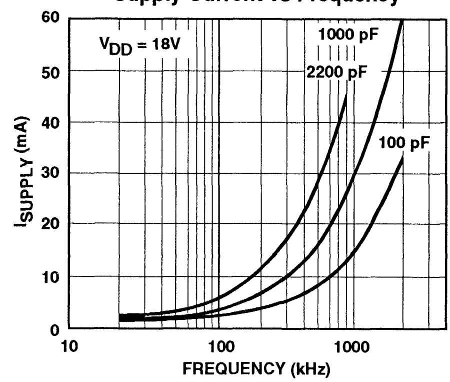


SUPPLY CURRENT CHARACTERISTICS CURVES (Load on Single Output Only)

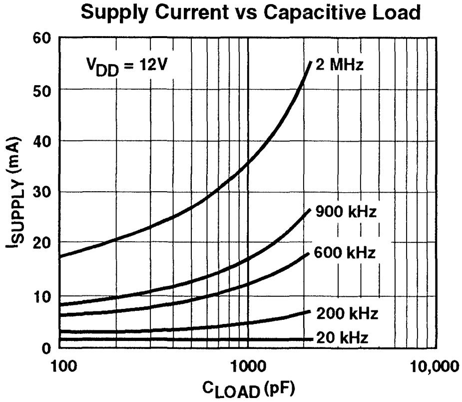
Supply Current vs Capacitive Load



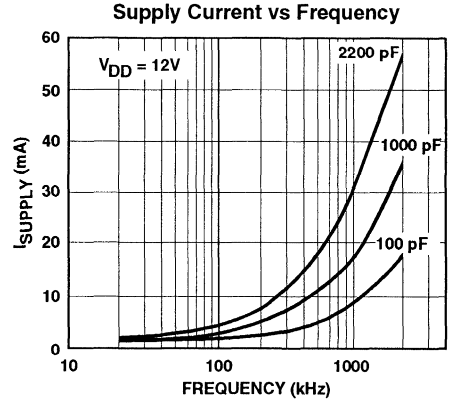
Supply Current vs Frequency



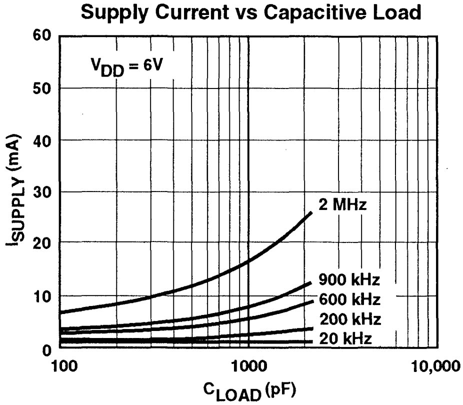
Supply Current vs Capacitive Load



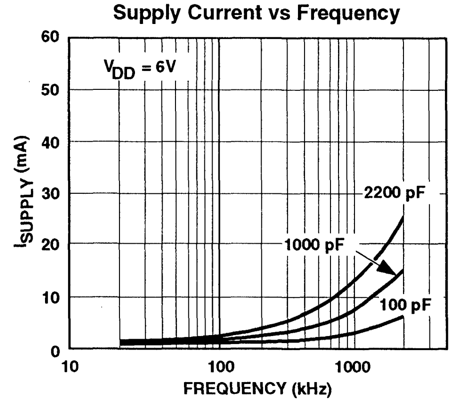
Supply Current vs Frequency



Supply Current vs Capacitive Load



Supply Current vs Frequency



TC4437/8/9 TC4467/8/9
TC4457/8/9 TC4487/8/9

POWER LOGIC CMOS QUAD DRIVERS

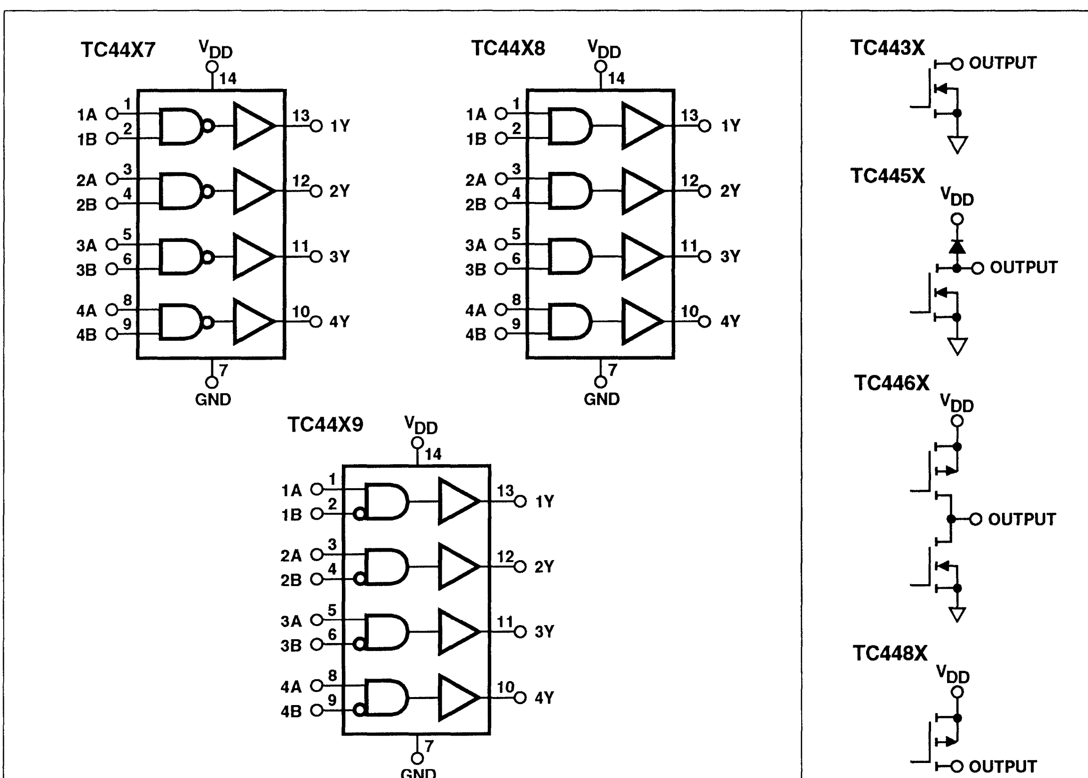
FEATURES

- Tough CMOS™ Construction
- Latchproof! Withstands 500 mA Inductive Kickback
- 3 Input Logic Choices
  — AND/NAND/AND+Inv
- 4 Output Structures
  — Pull-Up/Pull-Down/Totem Pole/
  Pull-Down with Clamp Diode
- Inverting or Non-Inverting Outputs
- Symmetrical Rise and Fall Times .... 25 ns
- Short, Equal Delay Times .... 75 ns
- High Peak Output Current 1.2A
- Wide Operating Range .... 4.5 to 18V
- Inputs = Logic 1 for Any Input From 2.4V to V_{DD}
- 2 kV ESD Protection on All Pins

APPLICATIONS

- General-Purpose CMOS Logic Buffer
- Driving All Four MOSFETs in an H-Bridge
- Direct Small Motor Driver
- Relay or Peripheral Drivers
- Dual Differential Output Power Drivers
- CCD Driver
- Pin-Switching Network Driver
- LED Driver
- High Side Switch

LOGIC DIAGRAMS



TC4437/8/9 TC4467/8/9
TC4457/8/9 TC4487/8/9

GENERAL DESCRIPTION

The TC44XX family of four-output CMOS buffer/drivers are an expansion from our earlier single- and dual-output drivers. Each driver has been equipped with a two-input logic gate for added flexibility. Four output configurations have also been provided, so high-efficiency CMOS drivers can be used whether the application requires a totem-pole output or pull-up/pull-down output, or pull-down with a clamp diode. These different input and output combinations make these Power Logic™ drivers well suited for a wide range of applications.

Although commonly used for driving power MOSFETs and similar highly capacitive loads, these drivers are equally well suited to driving any other load (capacitive, resistive, or inductive) which requires a high efficiency, low-impedance driver capable of high peak currents, rail-to-rail voltage swings, and fast switching times. For example, relays and solenoids can be driven with the 445X driver which contains an internal clamp diode which will shunt inductive flybacks back to the supply. The 443X driver provides a fast, low impedance path to ground for devices referenced to the upper supply rail like indicators, sounders or pin drivers. The 448X driver can source up to 250 mA into loads referenced to ground. Heavily loaded clock lines, coaxial cables, and piezoelectric transducers can all be driven easily with the 44XX series drivers. The only limitation on loading is that total power dissipation in the IC must be kept within the power dissipation limits of the package.

The TC44XX series drivers are built using Teledyne Component's new Tough CMOS process, which makes them easy and forgiving parts to use; capable of giving reliable service in very demanding operating environments. They will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (either polarity) occurs on the ground line. They can accept up to half an amp of inductive kickback current (either polarity) into their outputs without damage or logic upset. In addition, all terminals are protected against ESD to at least 2000V. Even the molding epoxy used on our plastic packages has been custom developed to contain less sodium and chlorine contamination than standard commercial molding compounds. In tests, it demonstrated zero device failures after 10,000 hours in an 85°C, 85% relative humidity environment.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC44**CPD	14-Pin Plastic DIP	0° to +70°C
TC44**COE	16-Pin Wide SOIC	0° to +70°C
TC44**EPD	14-Pin Plastic DIP	–40° to +85°C
TC44**EOE	16-Pin Wide SOIC	–40° to +85°C
TC44**EJD	14-Pin CerDIP	–40° to +85°C
TC44**MJD	14-Pin CerDIP	–55° to +125°C

**Two digits must be added in this position to define the device input and output configuration: TC44XX

3 Pull-Down	7 NAND
5 Pull-Down with Clamp Diode	8 AND
6 Pull-Up and Down	9 AND with INV
8 Pull-Up	

The first digit represents output structure. The second digit represents input logic. *Example:* TC4487 has a pull-up output and a NAND input.

TRUTH TABLE

	Inputs		Outputs			
Part No.	A	B	443X	445X	446X	448X
TC44*7	H	H	L	L	L	F
NAND	H	L	F	F	H	H
	L	H	F	F	H	H
	L	L	F	F	H	H
TC44*8	H	H	F	F	H	H
AND	H	L	L	L	L	F
	L	H	L	L	L	F
	L	L	L	L	L	F
TC44*9	H	H	L	L	L	F
AND/	H	L	F	F	H	H
INV	L	H	L	L	L	F
	L	L	L	L	L	F

H = High L = Low F = Floating

POWER LOGIC CMOS QUAD DRIVERS

TC4437/8/9 TC4467/8/9 TC4457/8/9 TC4487/8/9

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +20V
Input Voltage .... (GND – 5V) to (V_{DD} + 0.3V)
Maximum Chip Temperature
  Operating .... +150°C
  Storage .... –65° to +150°C
Maximum Lead Temperature
  (Soldering, 10 sec) .... +300°C
Operating Ambient Temperature Range
  C Device .... 0° to +70°C
  E Device .... –40° to +85°C
  M Device .... –55° to +125°C
Power Dissipation
  JD Package (14-Pin CerDIP) 1.25W
  PD Package (14-Pin Plastic DIP) 1.5W
  OE Package (16-Pin Wide SOIC) 1W

Package Thermal Resistance
JD Package (14-Pin CerDIP) $R_{\theta J\text{-}A}$ .... 10 mW/°C
$R_{\theta J\text{-}C}$ .... 45 mW/°C
PD Package (14-Pin Plastic DIP) $R_{\theta J\text{-}A}$ .... 12 mW/°C
$R_{\theta J\text{-}C}$ .... 20 mW/°C
OE Package (16-Pin Wide SOIC) $R_{\theta J\text{-}A}$ .... 8 mW/°C
$R_{\theta J\text{-}C}$ .... 31 mW/°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

6

ELECTRICAL CHARACTERISTICS: Measured at T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage	Note 3	2.4		V_{DD}	V
V_{IL}	Logic 0, Low Input Voltage	Note 3	0		0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–1		1	µA
Output						
V_{OH}	High Output Voltage	I_{LOAD} = 10 mA (Note 1)	V_{DD} –0.15			V
V_{OL}	Low Output Voltage	I_{LOAD} = 10 mA (Note 1)			0.15	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V		10	15	Ω
I_{PK}	Peak Output Current			1.2		A
I_{DC}	Continuous Output Current	Single Output Total Package			300 500	mA mA
I	Latch-Up Protection Withstand Reverse Current	4.5V ≤ V_{DD} ≤ 16V	500			mA
Switching Time						
t_R	Rise Time	Figure 1		15	25	ns
t_F	Fall Time	Figure 1		15	25	ns
t_{D1}	Delay Time	Figure 1		40	75	ns
t_{D2}	Delay Time	Figure 1		40	75	ns
Power Supply						
I_S	Power Supply Current			1.5	4	mA
V_{DD}	Power Supply Voltage	Note 2	4.5		18	V

POWER LOGIC CMOS QUAD DRIVERS

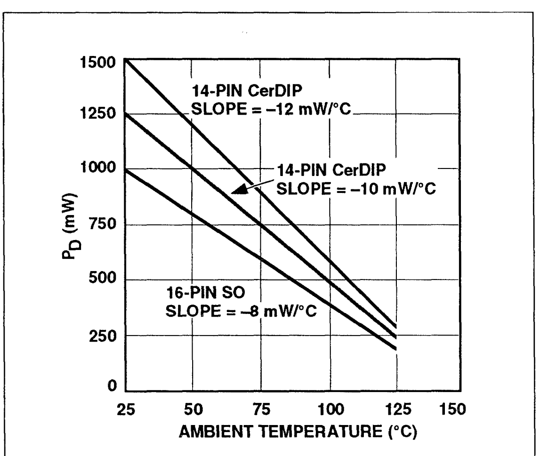
TC4437/8/9 TC4467/8/9 TC4457/8/9 TC4487/8/9

ELECTRICAL CHARACTERISTICS: Measured throughout operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V, unless otherwise specified.

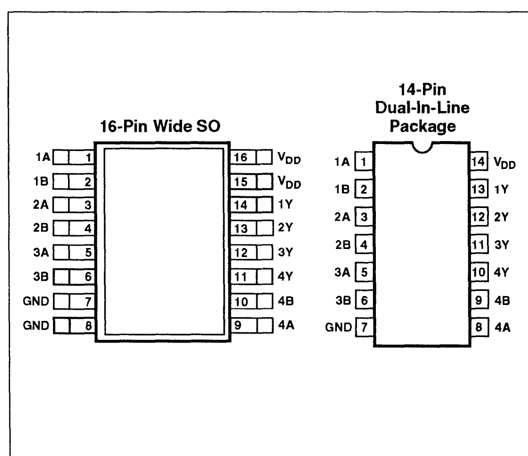
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1, High Input Voltage	(Note 3)	2.4			V
V_{IL}	Logic 0, Low Input Voltage	(Note 3)			0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DD}$	–1		1	µA
Output						
V_{OH}	High Output Voltage	I_{LOAD} = 10 mA (Note 1)	V_{DD} –0.30			V
V_{OL}	Low Output Voltage	I_{LOAD} = 10 mA (Note 1)			0.30	V
R_O	Output Resistance	I_{OUT} = 10 mA, V_{DD} = 18V		20	30	Ω
I_{PK}	Peak Output Current			1.2		A
I	Latch-Up Protection Withstand Reverse Current	$4.5V \leq V_{DD} \leq 16V$	500			mA
Switching Time						
t_R	Rise Time	Figure 1			50	ns
t_F	Fall Time	Figure 1			50	ns
t_{D1}	Delay Time	Figure 1			100	ns
t_{D2}	Delay Time	Figure 1			100	ns
Power Supply						
I_S	Power Supply Current				8	mA
I_S	Power Supply Voltage	Note 2	4.5		18	V

NOTES:
1. Totem-pole outputs should not be paralleled because the propagation delay differences from one to the other could cause one driver to drive high a few nanoseconds before another. The resulting current spike, although short, may decrease the life of the device.
2. When driving all four outputs simultaneously in the same direction, V_{DD} shall be limited to 16V. This reduces the chance that internal dv/dt will cause high-power dissipation in the device.
3. The input threshold has about 50 mV of hysteresis centered at approximately 1.5V. Slow moving inputs will force the device to dissipate high peak currents as the input transitions through this band. Input rise times should be kept below 5 µs to avoid high internal peak currents during input transitions. Static input levels should also be maintained above the maximum or below the minimum input levels specified in the "Electrical Characteristics" to avoid increased power dissipation in the device.

PACKAGE POWER DISSIPATION



PIN CONFIGURATIONS



Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, charging a 1000 pF load 18V in 25 ns requires a 0.8A current from the device's power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (<0.5 in.) should be used. A 1 μF film capacitor in parallel with one or two 0.1 μF ceramic disk capacitors normally provides adequate bypassing.

Grounding

The TC44X7 and TC44X9 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for input and output circuits or a ground plane should be used.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With logic "0" outputs, maximum quiescent supply current is 4 mA. Logic "1" output level signals reduce quiescent current to 1.4 mA maximum. Unused driver inputs must be connected to V_{DD} or V_{SS}. Minimum power dissipation occurs for logic "1" outputs.

The drivers are designed with 50 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5V, making Logic 1 input any voltage greater than 1.5V up to V_{DD}. Input current is less than 1 μA over this range.

Power Dissipation

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations.

Teledyne Components' CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 4 mA, compared to the D469's 20 mA specification.

Input signal duty cycle, power supply voltage, and load type influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operation temperature is easily calculated. The 14-pin plastic package junction-to-ambient thermal resistance is 83.3°C/W. At +25°C, the package is rated at 1500 mW maximum dissipation. Maximum allowable chip temperature is +150°C.

Three components make up total package power dissipation:

(1) Load caused dissipation (P_L)
(2) Quiescent power (P_Q)
(3) Transition power (P_T).

A capacitive-load-caused dissipation (driving MOSFET gates), is a direct function of frequency, capacitive load, and supply voltage. The power dissipation is:

$$P_L = f\,C\,V_S^2,$$

where: f = Switching frequency
C = Capacitive load
V_S = Supply voltage.

A resistive-load-caused dissipation for ground-referenced loads is a function of duty cycle, load current, and load voltage. The power dissipation is:

$$P_L = D\,(V_S - V_L)\,I_L,$$

where: D = Duty cycle
V_S = Supply voltage
V_L = Load voltage
I_L = Load current.

A resistive-load-caused dissipation for supply-referenced loads is a function of duty cycle, load current, and output voltage. The power dissipation is:

$$P_L = D\,V_O\,I_L,$$

where: f = Switching frequency
V_O = Device output voltage
I_L = Load current.

Quiescent power dissipation depends on input signal duty cycle. Logic high outputs result in a lower power dissipation mode with only 0.6 mA total current drain (all devices driven). Logic low outputs raise the current to 4 mA maximum. The quiescent power dissipation is:

$$P_Q = V_S\,(D(I_H) + (1-D)I_L),$$

where: I_H = Quiescent current with all outputs low (4 mA max)
I_L = Quiescent current with all outputs high (0.6 mA max)
D = Duty cycle
V_S = Supply voltage.

Transition power dissipation arises in the totem-pole configuration (TC446X) because the output stage N-channel and P-channel MOS transistors are ON simultaneously for a very short period when the output changes. The transition power dissipation is approximately:

$P_T = f\,V_S\,(10 \times 10^{-9})$.

Package power dissipation is the sum of load, quiescent and transition power dissipations. An example shows the relative magnitude for each term:

C = 1000 pF capacitive load
V_S = 15V
D = 50%
f = 200 kHz
P_D = Package Power Dissipation = $P_L + P_Q + P_T$
= 45 mW + 35 mW + 30 mW = 110 mW.

Maximum operating temperature:

$T_J - \theta_{JA}(P_D) = 141°C$,

where: T_J = Maximum allowable junction temperature (+150°C)
θ_{JA} = Junction-to-ambient thermal resistance (83.3°C/W) 14-pin plastic package.

NOTE: Ambient operating temperature should not exceed +85°C for "EJD" device or +125°C for "MJD" device.

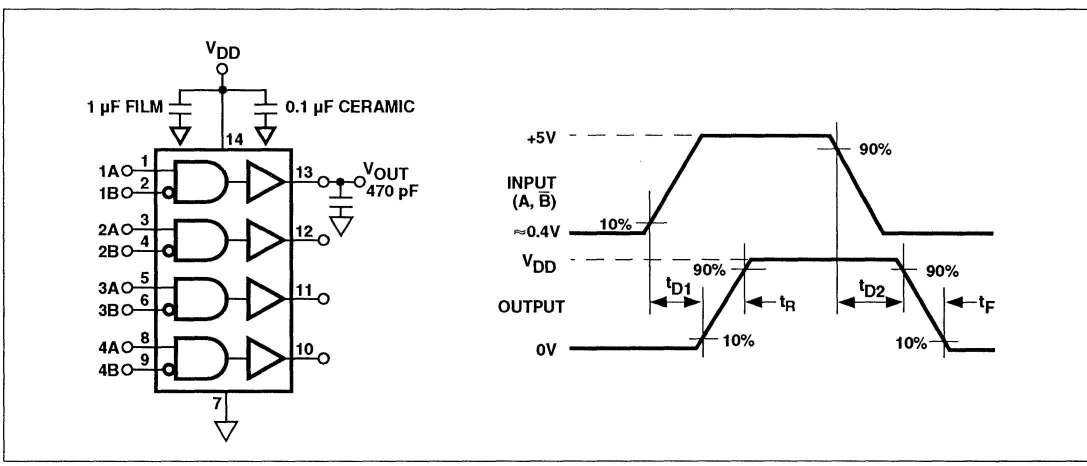
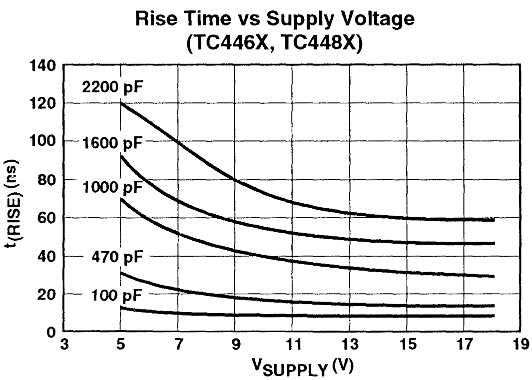
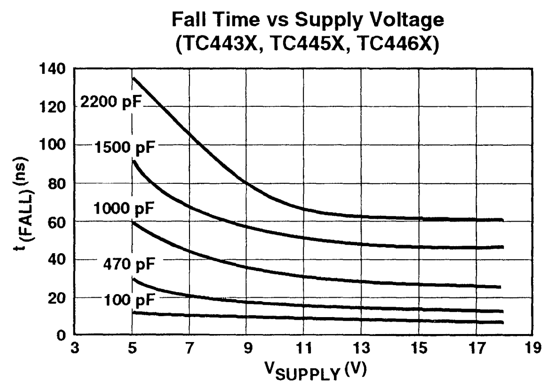
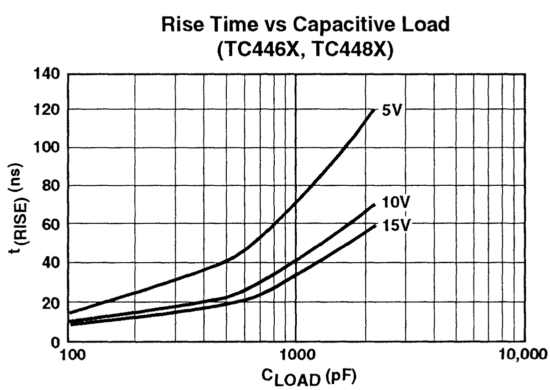


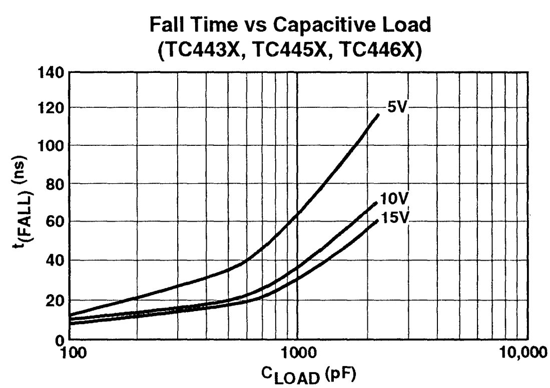
Figure 1 Switching Time Test Circuit

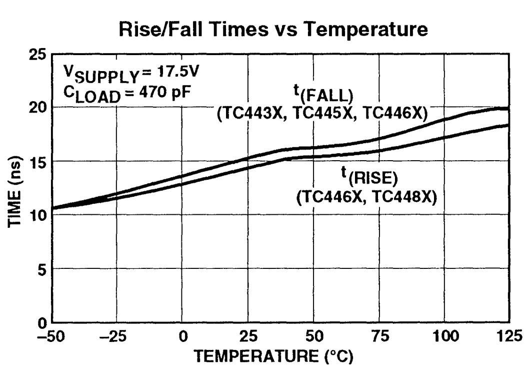
CHARACTERISTICS CURVES

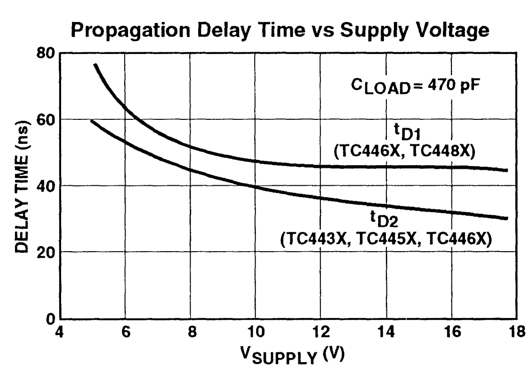






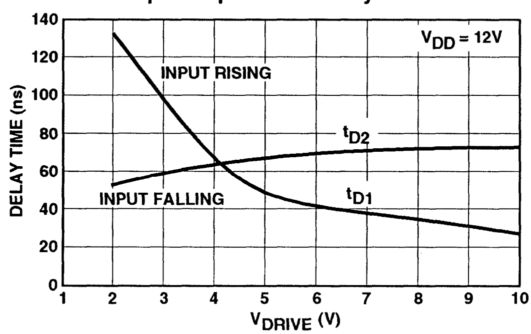




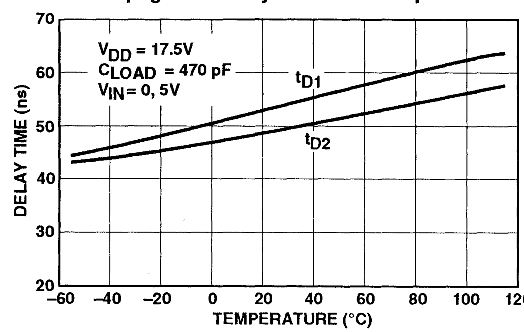


CHARACTERISTICS CURVES (Cont.)

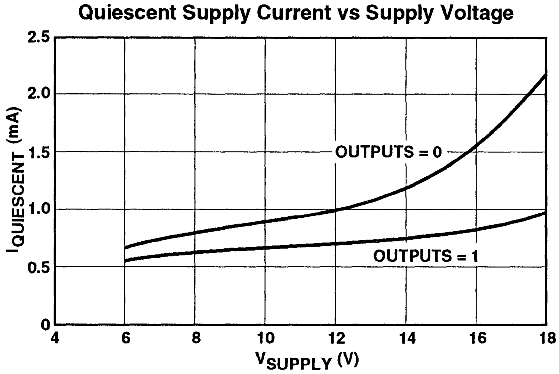
Input Amplitude vs Delay Times



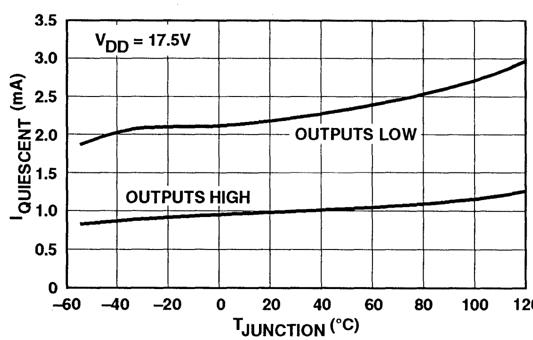
Propagation Delay Times vs Temperature



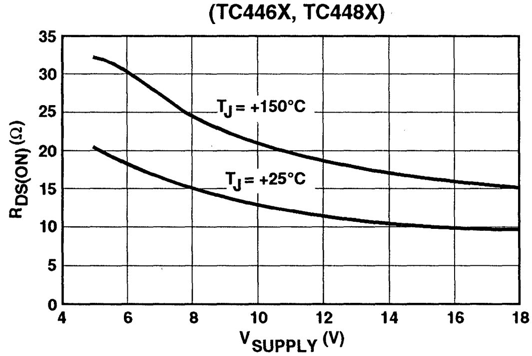
Quiescent Supply Current vs Supply Voltage



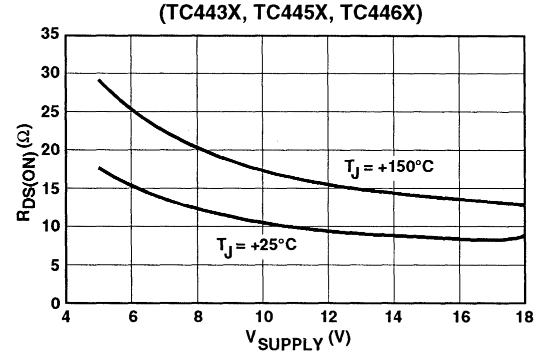
Quiescent Supply Current vs Temperature



High-State Output Resistance (TC446X, TC448X)

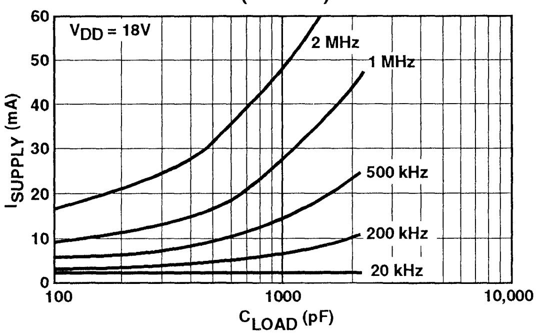


Low-State Output Resistance (TC443X, TC445X, TC446X)

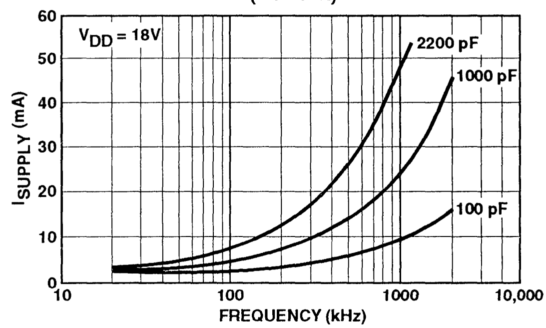


SUPPLY CURRENT CHARACTERISTICS (Load on Single Output Only)

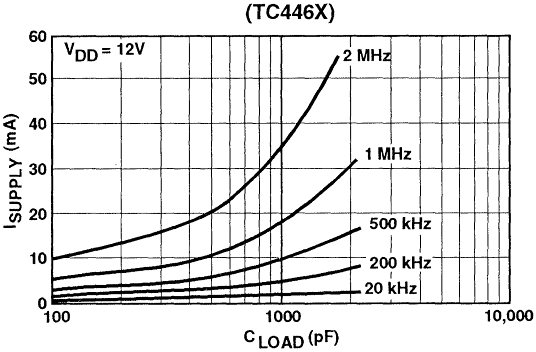
Supply Current vs Capacitive Load (TC446X)



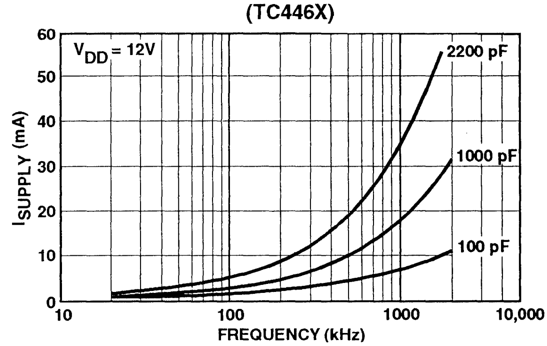
Supply Current vs Frequency (TC446X)



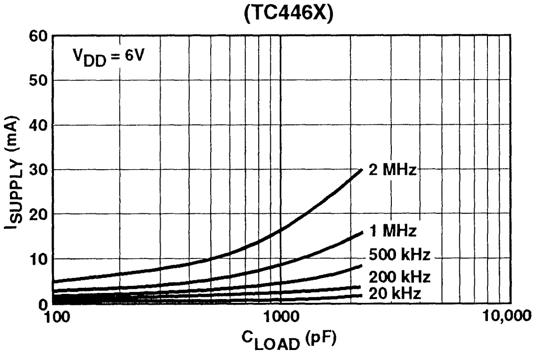
Supply Current vs Capacitive Load (TC446X)



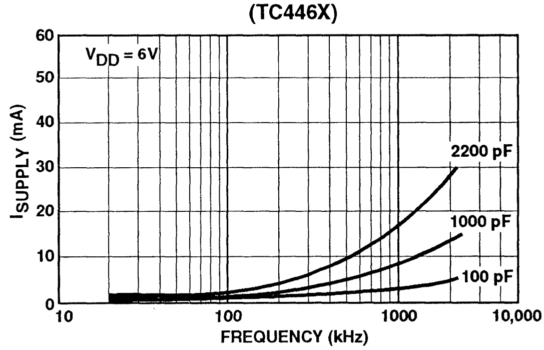
Supply Current vs Frequency (TC446X)



Supply Current vs Capacitive Load (TC446X)

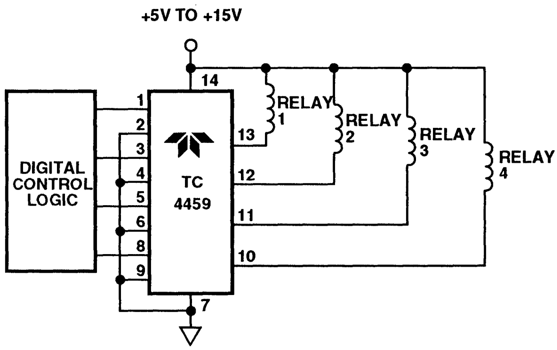


Supply Current vs Frequency (TC446X)

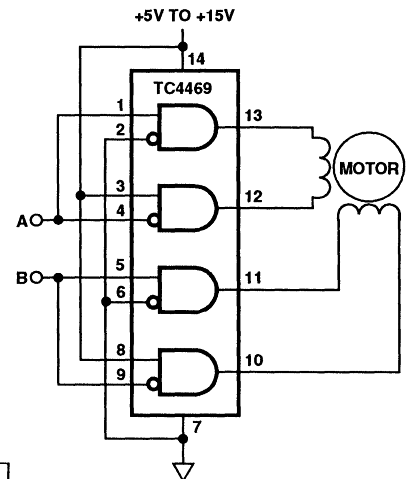


TYPICAL APPLICATIONS

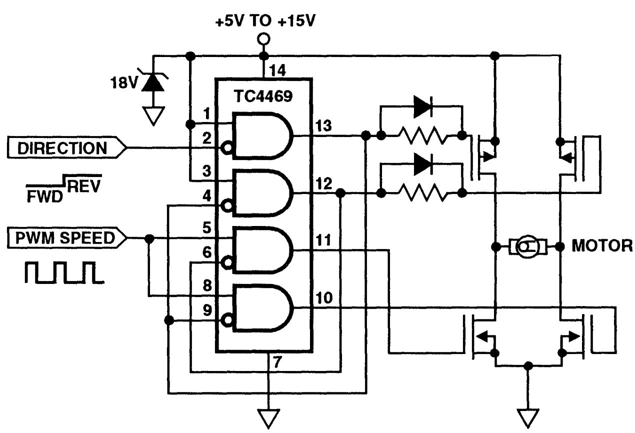
Quad Relay Driver Interface



Stepper Motor Drive

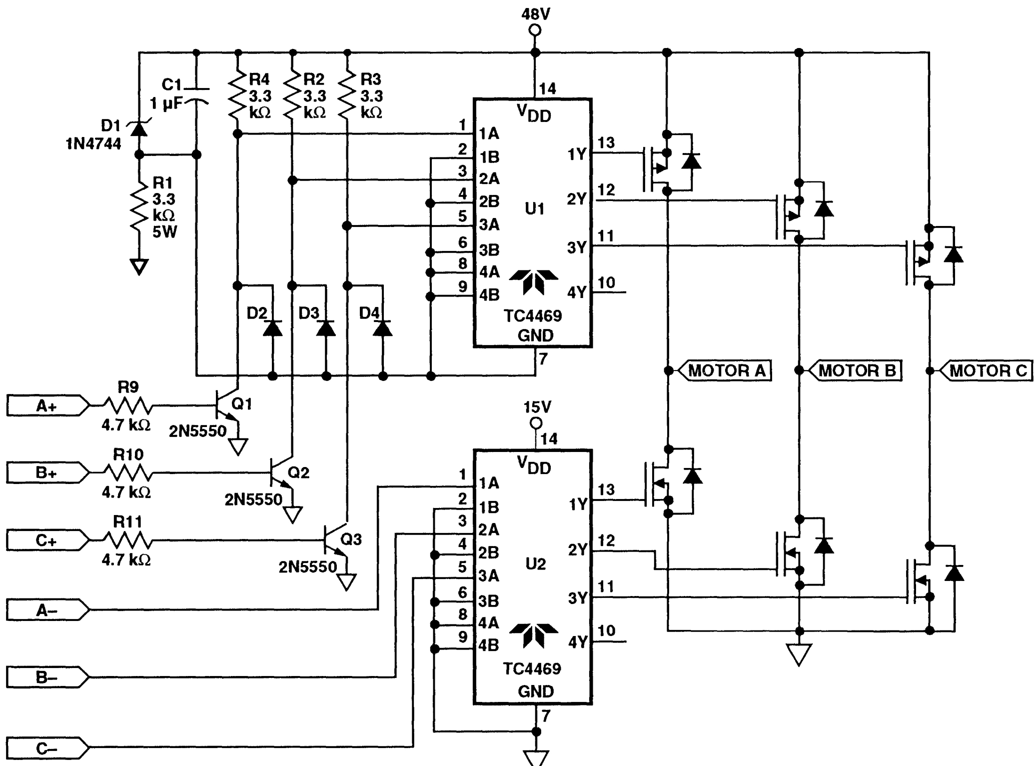


Quad Driver for H-Bridge Motor Control

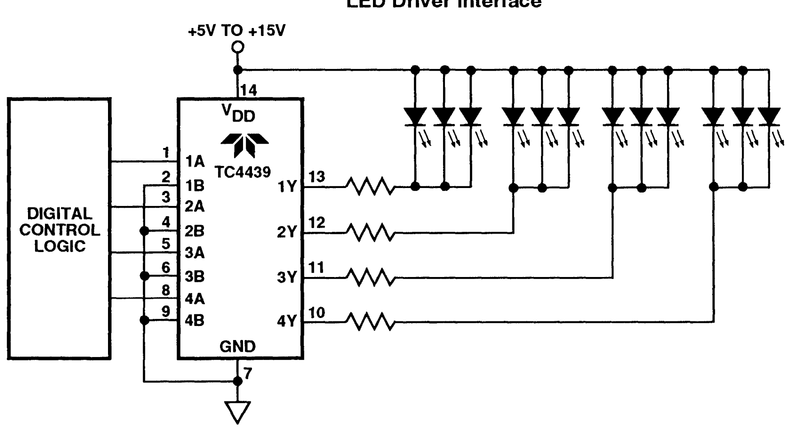


TYPICAL APPLICATIONS (Cont.)

48-Volt, 3-Phase Brushless Output Stage



LED Driver Interface



NOTES

TELEDYNE COMPONENTS

TC4460 TC4462
TC4461 TC4463

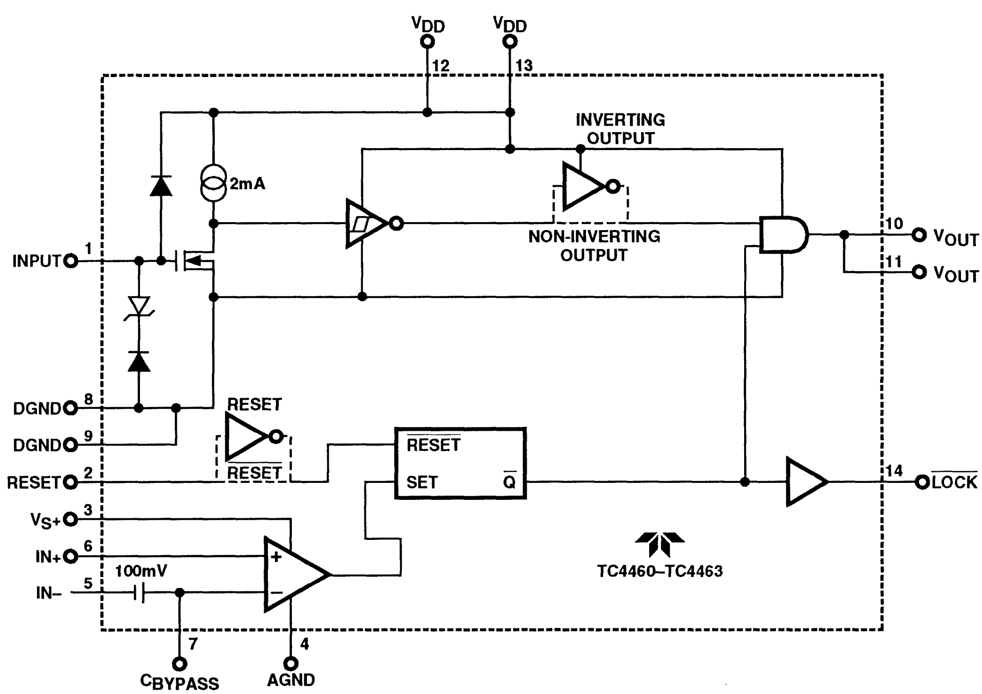
CURRENT-SENSING, 6 AMP POWER MOSFET DRIVER

FEATURES

- Complete Fault-Sensing Power Driver
  - — High Peak Output Current Driver
  - — Comparator
  - — Latch
- High Peak Output Current 6A
- Matched Rise and Fall Times
- High Capacitive Load Drive Capability .... 2500 pF in 25 ns
- Output Swing to within 25 mV of DGND or V_{DD}
- Low Output Impedance 2.5Ω
- Fast Comparator .... 170 ns typ
- Precision Comparator Threshold ... 100 mV ±10 mV
- Latch Status Output
- Tough CMOS™ Construction
- Logic Input Will Withstand Negative Swing Up to –5V
- Latch-up Protected: Will Withstand > 1.5A Reverse Output Current
- Logic High Input, Any Supply Voltage 2.4V to V_{DD}
- Low Supply Current
  - — With Logic '1' Input .... 6 mA
  - — With Logic '0' Input .... 3 mA

6

FUNCTIONAL DIAGRAM



NOTE: PIN NUMBERS SHOWN FOR 14-PIN DIP.

4351 ILL F01

CURRENT-SENSING, 6 AMP POWER MOSFET DRIVER

TC4460 TC4462 TC4461 TC4463

GENERAL DESCRIPTION

The TC4460/4461/4462/4463 are high speed CMOS drivers which incorporate a comparator input to terminate the output pulse. These devices are ideal for driving power MOSFETS, such as SENSEFETS®, which include a separate output which mirrors drain current.

The TC4460 devices consist of a power driver, comparator, and latch. In normal operation the device operates as a power driver with a 6 A peak current totem-pole output. When the comparator threshold is exceeded, the latch is set and the output turns off. The output will not turn on again until the latch is reset. A 'LOCK' output is provided to signal that the output is disabled.

The TC4460 is ideal for applications which require fast response to an overload condition, such as PWM motor drive circuits. The response time is enhanced because the overload indication does not have to propagate through the control loop circuitry. Instead, the comparator directly monitors the SENSEFET current and turns off the driver output. The comparator delay is typically only 170 ns.

The comparator threshold is set internally at 100 mV ±10 mV. In most applications the comparator threshold will be referenced to analog ground, but the comparator common mode range extends from 0 V to 3 V.

With a comparator threshold of only 100 mV, low value resistors can be used to monitor the SENSEFET's current. Low impedances maximize the SENSEFET linearity, as well as improving response time and reducing noise.

The totem-pole output will sink or source 6 A peak current, with an output impedance of 2.5Ω. Output swing is to within 25mV of either supply rail, which ensures that a power MOSFET will be turned fully ON or fully OFF. Rise and fall times are only 25 ns with a 2500 pF load. Maximum load capacitance is essentially limited by package power dissipation.

The TC4460/4461/4462/4463 are built with Teledyne Component's Tough CMOS™ process. Digital inputs are protected from noise spikes up to 5V below ground, while the output will accept up to 1.5A of reverse current (of either polarity) without damage.

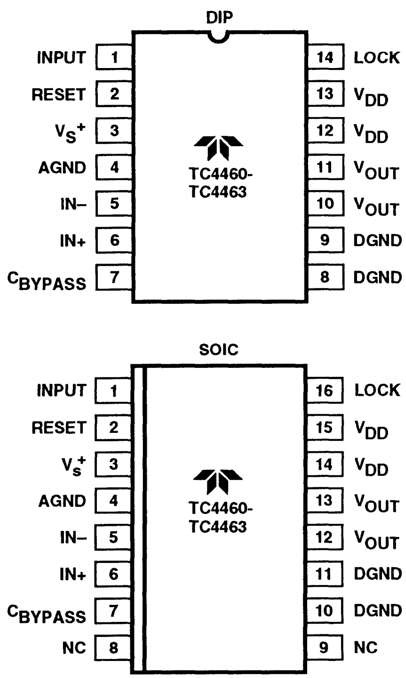
ORDERING INFORMATION

Part No.	Output Polarity	Reset Polarity	Package	Temp Range
TC4460CPD	Noninverting	Low	8-Pin PDIP	0°C to +70°C
TC4460COE	Noninverting	Low	8-Pin SOIC	0°C to +70°C
TC4460EPD	Noninverting	Low	8-Pin PDIP	−40°C to +85°C
TC4460EOE	Noninverting	Low	8-Pin SOIC	−40°C to +85°C
TC4460MJD	Noninverting	Low	8-Pin CerDIP	−55°C to +125°C
TC4461CPD	Inverting	Low	8-Pin PDIP	−55°C to +125°C
TC4461COE	Inverting	Low	8-Pin PDIP	−55°C to +125°C
TC4461EPD	Inverting	Low	8-Pin PDIP	−55°C to +125°C
TC4461EOE	Inverting	Low	8-Pin PDIP	−55°C to +125°C
TC4461MJD	Inverting	Low	8-Pin PDIP	−55°C to +125°C
TC4462CPD	Noninverting	Hi	8-Pin PDIP	−55°C to +125°C
TC4462COE	Noninverting	Hi	8-Pin PDIP	−55°C to +125°C
TC4462EPD	Noninverting	Hi	8-Pin PDIP	−55°C to +125°C
TC4462EOE	Noninverting	Hi	8-Pin PDIP	−55°C to +125°C
TC4462MJD	Noninverting	Hi	8-Pin PDIP	−55°C to +125°C
TC4463CPD	Inverting	Hi	8-Pin PDIP	−55°C to +125°C
TC4463COE	Inverting	Hi	8-Pin PDIP	−55°C to +125°C
TC4463EPD	Inverting	Hi	8-Pin PDIP	−55°C to +125°C
TC4463EOE	Inverting	Hi	8-Pin PDIP	−55°C to +125°C
TC4463MJD	Inverting	Hi	8-Pin PDIP	−55°C to +125°C

CURRENT-SENSING, 6 AMP POWER MOSFET DRIVER

TC4460 TC4462 TC4461 TC4463

PIN CONFIGURATIONS



NOTE: DUPLICATE PINS MUST BOTH BE CONNECTED FOR PROPER OPERATION.

NC = NO INTERNAL CONNECTION

4351 ILL 02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Digital and Analog .... +22V
Input Voltage, Pins 1 and 2 .... V_{DD}+0.3V to GND–5.0V
Input Voltage,
Pins 5 and 6 .... V_S^++0.3V to Analog GND–0.3V
Maximum Chip Temperature .... +150°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Package Thermal Resistance
CerDIP $R_{\theta J\text{–}A}$ .... 150°C/W
CerDIP $R_{\theta J\text{–}C}$ .... 55°C/E
PDIP $R_{\theta J\text{–}A}$ .... 125°C/W
PDIP $R_{\theta J\text{–}C}$ .... 45°C/W
SOIC $R_{\theta J\text{–}A}$ .... 250°C/W
SOIC $R_{\theta J\text{–}C}$ .... 75°C/W
Operating Temperature Range
C Device .... 0°C to +70°C
E Device .... –40°C to +85°C
M Device .... –55°C to +125°C
Power Disipation
Plastic DIP .... 1000 mW
CerDIP .... 800 mW
SOIC .... 500 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

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TC4460 TC4462
TC4461 TC4463

ELECTRICAL CHARACTERISTICS: $T_A = +25°C$ with $4.5V \le V_{DD} \le 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 1 Low Input Voltage		—	—	0.8	V
I_N	Input Current	$0V \le V_{IN} \le V_{DD}$	–10	—	10	μA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, High	I_{OUT}= 10mA, V_{DD} = 18V	—	2.2	2.8	Ω
R_O	Output Resistance, Low	I_{OUT}= 10mA, V_{DD} = 18V	—	1.9	2.5	Ω
I_{PK}	Peak Output Current		—	6	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% $t \le 300$ μs	1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	21	25	ns
t_F	FallTime	Figure 1, C_L = 2500 pF	—	21	25	ns
t_{D1}	Delay Time	Figure 1, C_L = 2500 pF	—	65	75	ns
t_{D2}	Delay Time	Figure 1, C_L = 2500 pF	—	65	75	ns
Comparator (Note 1)						
I_{IN+}	Comparator Input Bias Current (Plus)		—	—	1	μA
I_{IN-}	Comparator Input Bias Current (Minus)		—	—	150	μA
V_{OS}	Comparator Offset		90	—	110	mV
V_{CMR}	Comparator Common Mode Range		0	—	3	V
T_{CDO}	Comparator Delay to V_{OUT}	25 mV Overdrive	—	170	200	ns
T_{CDL}	Comparator Delay to $\overline{LOCK}$	25 mV Overdrive	—	170	200	ns
T_{RDL}	Reset Delay to $\overline{LOCK}$		—	70	100	ns
T_{RDO}	Reset Delay to Output		—	90	120	ns
V_{IHL}	Latch Input High	Pin 2, RESET	2.4	—		V
V_{ILL}	Latch Input Low	Pin 2, RESET	—	—	0.8	V
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	3.5 2.8	6 3	mA mA

NOTES: 1. Switching times guaranteed by design.

CURRENT-SENSING, 6 AMP POWER MOSFET DRIVER

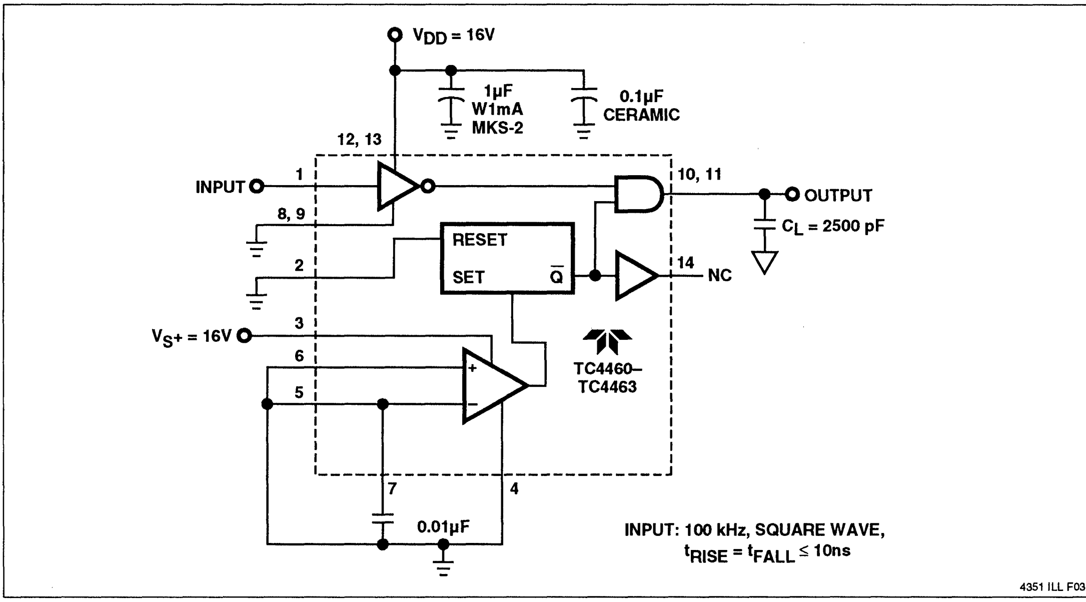
6

ELECTRICAL CHARACTERISTICS: Over operating temperature range with 4.5V≤ V_{DD} = 18V, unless otherwise specified.

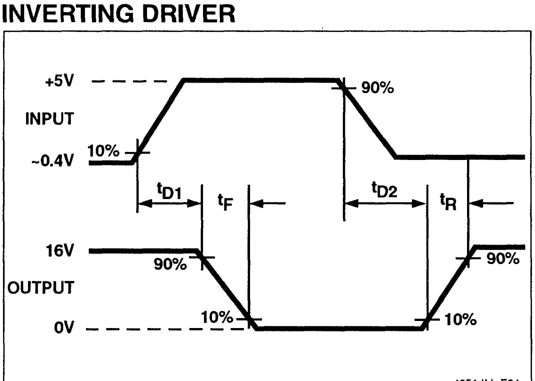
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 1 Low Input Voltage		—	—	0.8	V
I_N	Input Current	$0V \le V_{IN} \le V_{DD}$	–10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance, High	I_{OUT}= 10mA, V_{DD} = 18V	—	2.8	5	Ω
R_O	Output Resistance, Low	I_{OUT}= 10mA, V_{DD} = 18V	—	3.5	5	Ω
I_{PK}	Peak Output Current		—	6	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% $t \le 300$ µs	1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	30	35	ns
t_F	FallTime	Figure 1, C_L = 2500 pF	—	30	35	ns
t_{D1}	Delay Time	Figure 1, C_L = 2500 pF	—	80	90	ns
t_{D2}	Delay Time	Figure 1, C_L = 2500 pF	—	80	90	ns
Comparator (Note 1)						
I_{IN+}	Comparator Input Bias Current (Plus)		—	—	1	µA
I_{IN-}	Comparator Input Bias Current (Minus)		—	—	150	µA
V_{OS}	Comparator Offset		85	—	115	mV
V_{CMR}	Comparator Common Mode Range		0	—	3	V
T_{CDO}	Comparator Delay to V_{OUT}	25 mV Overdrive	—	150	280	ns
T_{CDL}	Comparator Delay to $\overline{LOCK}$	25 mV Overdrive	—	150	280	ns
T_{RDL}	Reset Delay to $\overline{LOCK}$		—	70	140	ns
T_{RDO}	Reset Delay to Output		—	90	160	ns
V_{IHL}	Latch Input High	Pin 2, RESET	2.4	—		V
V_{ILL}	Latch Input Low	Pin 2, RESET	—	—	0.8	V
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs)	—	3.5	6	mA
		V_{IN} = 0V (Both Inputs)	—	2.8	3.0	mA

NOTES: 1. Switching times guaranteed by design.

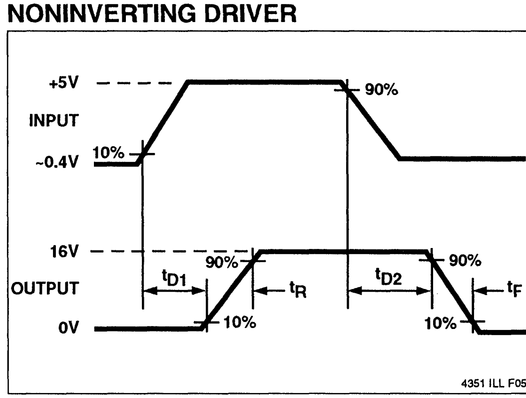
SWITCHING TIME TEST CIRCUIT



INVERTING DRIVER



NONINVERTING DRIVER



TELEDYNE COMPONENTS

TC4626
TC4627

POWER CMOS DRIVERS WITH V_{DD} TRIPLER

FEATURES

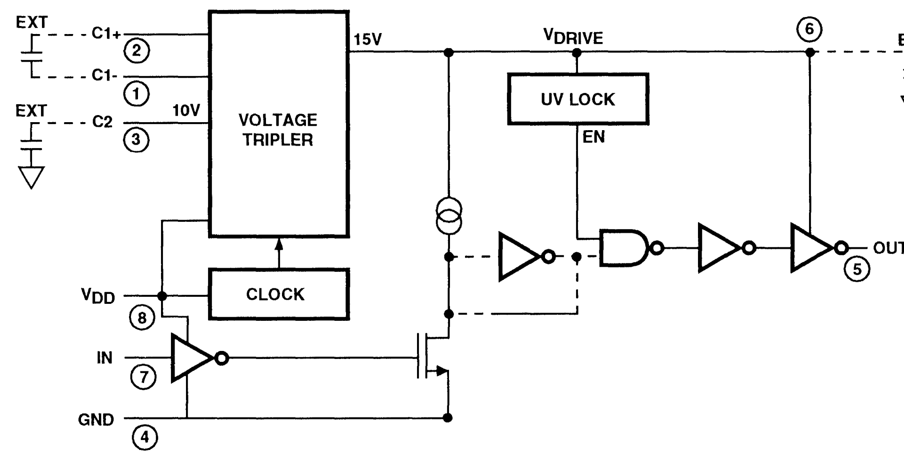
- Power driver with on Board Voltage Tripler
- Low IDD < 2.0 mA
- Small Package - 8 Pin PDIP
- Under voltage Circuitry
- Fast Rise-Fall Time < 50 ns @ 1000pF
- Below Rail Input Protection

GENERAL DESCRIPTION

The TC4626/4627 are single CMOS high speed drivers with an on board voltage tripler. Three external capacitors are required for the voltage tripler function. The part works with input supply voltages from 2.6 volts to 6 volts depending on the exact load requirements. An internal undervoltage lockout circuit keeps the driver section disenabled while the voltage at V_{DRIVE} remains below 9 volts.

6

FUNCTIONAL DIAGRAM



NOTE: Pin numbers correspond to 8-pin package

TC4626
TC4627

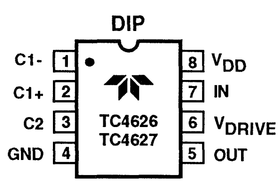
ORDERING INFORMATION

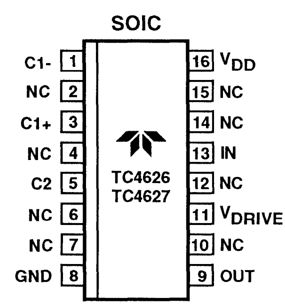
Part No.	Package
TC4626MJA	8-Pin CerDIP
TC4627MJA	8-Pin CerDIP
TC4626EPA	8-Pin PDIP
TC4627EPA	8-Pin PDIP
TC4626EOE	16-Pin SOIC
TC4627EOE	16-Pin SOIC
TC4626CPA	8-Pin PDIP
TC4627CPA	8-Pin PDIP
TC4626COE	16-Pin SOIC
TC4627COE	16-Pin SOIC

ABSOLUTE MAXIMUM RATINGS

Power Dissipation
PDIP .... 500 mW
CerDIP 800mW
Derating Factor
PDIP .... 5.6 mW/°C Above 36°C
CerDIP .... 6.0 mW/°C
Supply Voltage 18V
Input Voltage, Any Terminal .... V_S + 0.3V to GND –0.3V
Operating Temperature: M Version .... -55°C to +125°C
E Version .... -40°C to +85°C
C Version .... 0°C to +70°C
Maximum Chip Temperature .... +150°C
Storage Temperature .... -60°C to +150°C
Lead Temperature (10 sec) .... +300°C

PIN CONFIGURATIONS





ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ $V_{DD} = 5V$ $C_1 = C_2 = C_3$ 10µF unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Driver Input						
V_{IH}	Logic 1, Input Voltage		2.4	—	—	V
V_{IL}	Logic 0, Input Voltage		—	—	0.8	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_{DRIVE}$	–1	—	1	µA
Driver Output						
V_{OH}	High Output Voltage		V_{DRIVE}–0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	$V_{IN} = 0.8V$ $I_{OUT} = 10$ mA, $V_{DD} = 5V$	—	10	15	Ω
		$V_{IN} = 3V$ $I_{OUT} = 10$ mA, $V_{DD} = 5V$	—	6	10	Ω
I_{PK}	Peak Output Current		—	1.5	—	A
Switching Time						
t_R	Rise Time	Test Figure 1,2	—	—	40	ns
t_F	Fall Time	Test Figure 1,2	—	—	40	ns
t_{D1}	Delay Time	Test Figure 1,2	—	—	40	ns
t_{D2}	Delay Time	Test Figure 1,2	—	—	40	ns
F_{MAX}	Maximum Switching Frequency	Test Figure 1 $V_{DD} = 5V$, $V_{DRIVE} > 10V$	1.0	—	—	MHz
R_3	Voltage Tripler Output Source Resistance	$I_L = 10$ mA, $V_{DD} = 5V$	—	220	400	Ω
R_2	Voltage Doubler Output Source Resistance		—	120	200	Ω
F_{OSC}	Oscillator Frequency		12	—	28	KHz
V_{OSC}	Oscillator Amplitude Measured at C1-	$R_{LOAD} = 10K\Omega$	4.5	—	—	V
UV	Undervoltage Threshold	@ V_{DRIVE}	8.5	9	9.5	V
V_{START}	Start Up Voltage	@ V_{DRIVE}	10.5	11	11.5	V
V_{DRIVE}	@$V_{DD} = 5V$	No Load	14.7	—	—	V
Power Supply						
I_{DD}	Power Supply Current	V_{IN} = LOW or HIGH	—	—	2	mA
V_{DD}	Supply Voltage		3.8	—	6.2	V

6

TC4626
TC4627

SWITCHING TIME TEST CIRCUITS

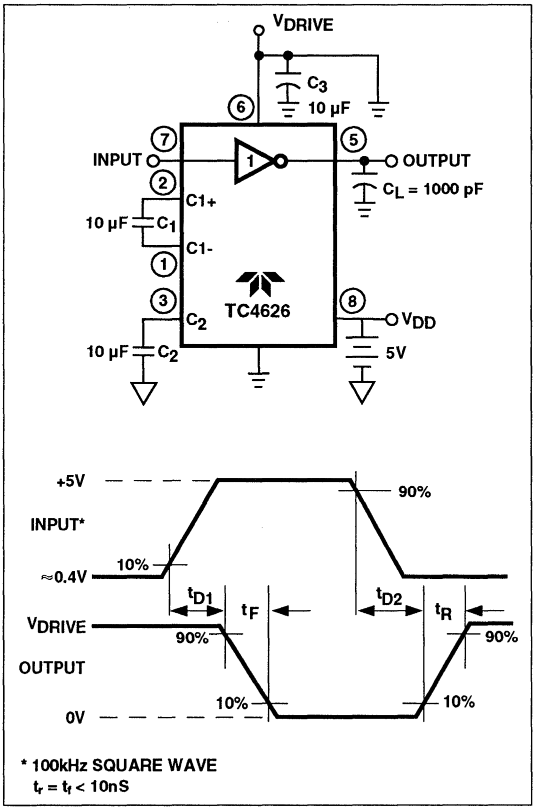


Figure 1. Inverting Driver Switching Time

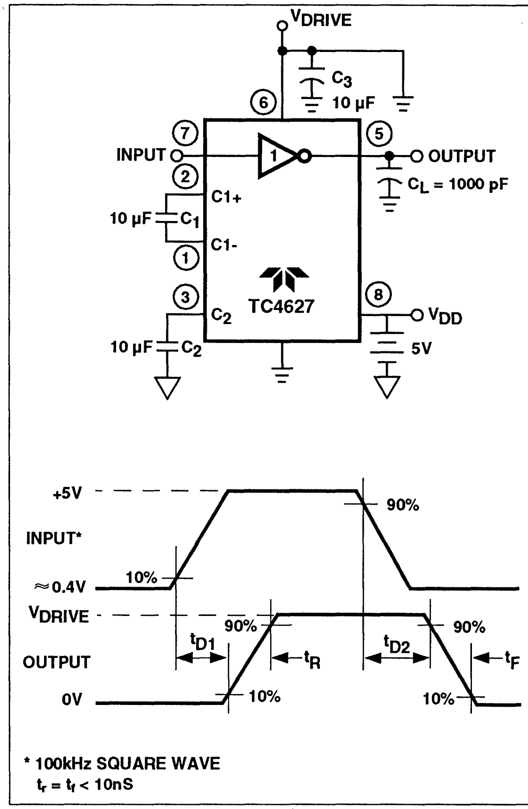


Figure 2. Non-Inverting Driver Switching Time

Section 7

References

7

LOW POWER, BAND-GAP VOLTAGE REFERENCES

FEATURES

- Temperature Coefficient .... 50 ppm/°C
- Wide Operating Current Range
  - TC04 .... 15 µA to 20 mA
  - TC05 .... 20 µA to 20 mA
- Dynamic Impedance 1Ω
- Output Tolerance 2%
- Output Voltage Option
  - TC04 .... 1.25V
  - TC05 .... 2.5V
- TO-92 Plastic or TO-52 Hermetic Packages
- 8-Pin Plastic Small Outline (SO) Package

APPLICATIONS

- ADC and DAC Reference
- Current Source Generation
- Threshold Detectors
- Power Supplies
- Multimeters

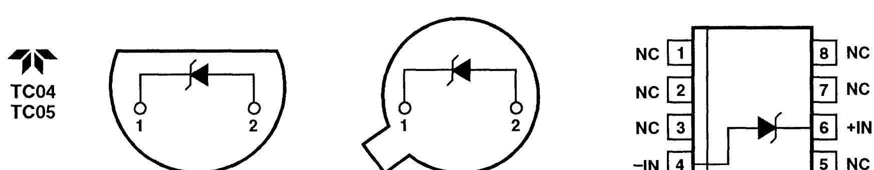
GENERAL DESCRIPTION

The TC04 (1.25V output) and TC05 (2.5V output) bipolar, two-terminal, band-gap voltage references offer precision performance without premium price. These devices do not require thin-film resistors, greatly lowering manufacturing complexity and cost.

A 50 ppm/°C output temperature coefficient and 15 µA to 20 mA operating current range make these devices attractive multimeter, data acquisition converter, and telecommunication voltage references.

7

PIN CONFIGURATIONS



TO-92
PLASTIC PACKAGE
(BOTTOM VIEW)

TO-52
HERMETIC PACKAGE
(BOTTOM VIEW)

SURFACE MOUNT
PLASTIC PACKAGE

NC = NO INTERNAL CONNECTION

LOW-POWER, BAND-GAP VOLTAGE REFERENCES

TC04 TC05

ORDERING INFORMATION

Voltage	Max Temperature Coefficient	Temperature Range: –55°C to +125°C TO-52 Package	Temperature Range: 0°C to +70°C TO-92 Package	Temperature Range: 0°C to +70°C Surface Mount Package
1.25V	50 ppm/°C	TC04AMRM	TC04ACZM	TC04ACOA
1.25V	100 ppm°C	TC04BMRM	TC04BCZM	TC04BCOA
2.5V	50 ppm/°C	TC05AMRM	TC05ACZM	TC04ACOA
2.5V	100 ppm/°C	TC05BMRM	TC05BCZM	TCO5BCOA

ABSOLUTE MAXIMUM RATINGS

Forward Current .... +10 mA
Reverse Current .... +30 mA
Storage Temperature Range .... –65°C to +150°C
Operating Temperature Range
TO-92 Package .... 0°C to +70°C
TO-52 Package .... –55°C to +125°C
COA Surface Mount Package .... 0°C to +70°C

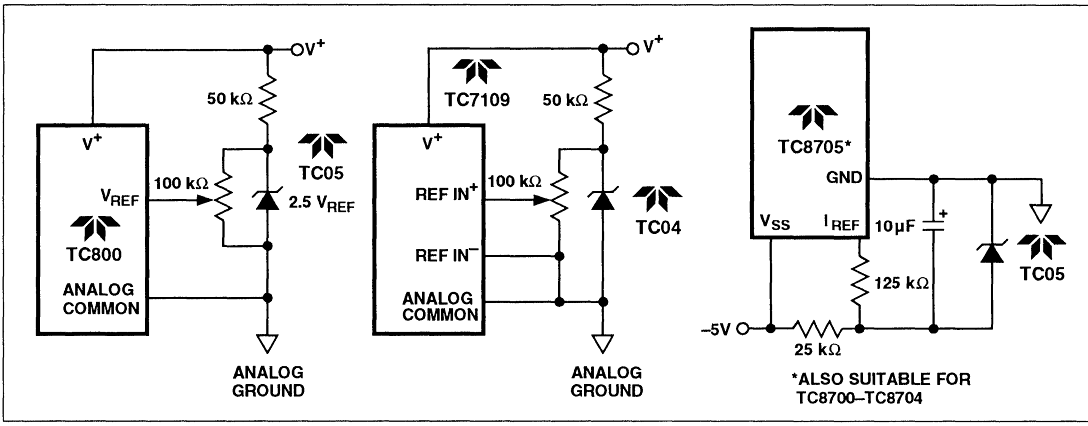
Lead Temperature (Soldering, 10 sec)
TO-92 Package .... +260°C
TO-52 Package .... +300°C
COA Surface Mount Package .... +260°C
Power Dissipation .... Limited by Forward/ Reverse Current

Functional operation above the absolute maximum stress ratings is not implied.

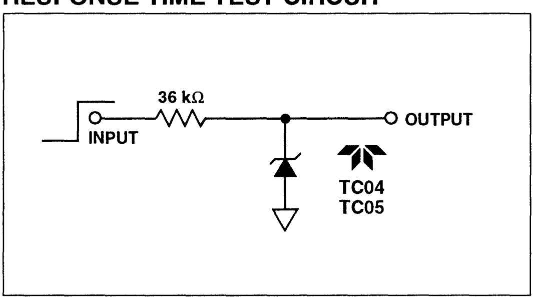
ELECTRICAL CHARACTERISTICS: $T_A = +25°C$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{BR}	Reverse Breakdown Voltage	$I_R = 100\ \mu A$				
	TC04		1.24	1.26	1.28	V
	TC05		2.45	2.50	2.60	V
DV_{BR}	Reverse Breakdown Voltage Change					
	TC04	$15\ \mu A < I_R < 20\ mA$	—	10	20	mV
		$20\ \mu A < I_R < 1\ mA$	—	0.25	1	mV
	TC05	$20\ \mu A < I_R < 20\ mA$	—	10	20	mV
		$25\ \mu A < I_R < 1\ mA$	—	0.25	1	mV
TC	Temperature Coefficient	$I_R = 100\ \mu A$				
	TC04A/TC05A		—	0.003	0.005	%/°C
	TC04B/TC05B		—	0.003	0.01	%/°C
I_R	Reverse Current					
	TC04		0.015	—	20	mA
	TC05		0.020	—	20	mA

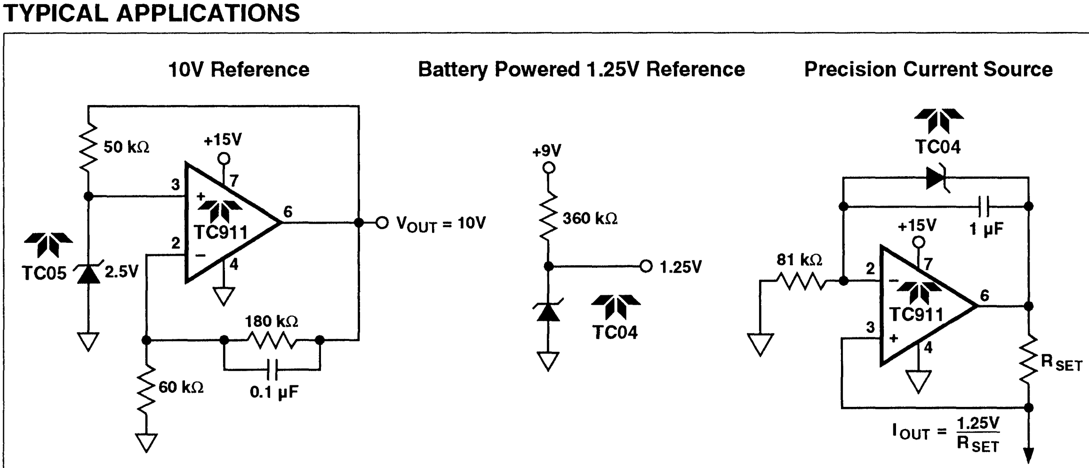
VOLTAGE REFERENCE CIRCUITS FOR SYSTEM DATA CONVERTERS



RESPONSE TIME TEST CIRCUIT

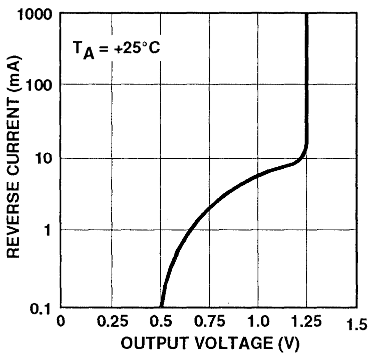


TYPICAL APPLICATIONS

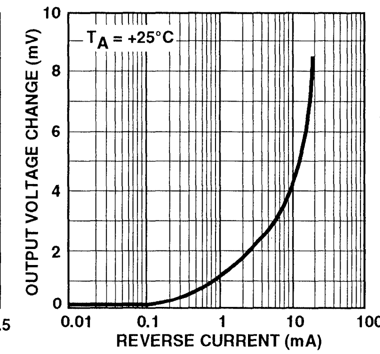


TYPICAL CHARACTERISTICS CURVES

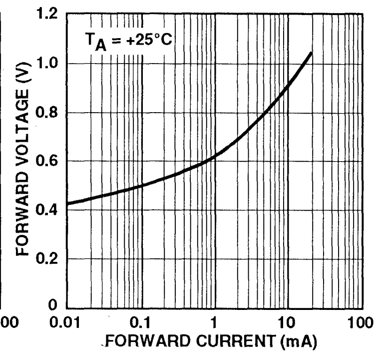
TC04: Output Voltage vs
Reverse Current



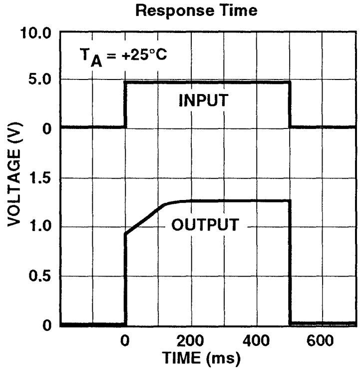
TC04: Output Voltage Change
vs Reverse Current



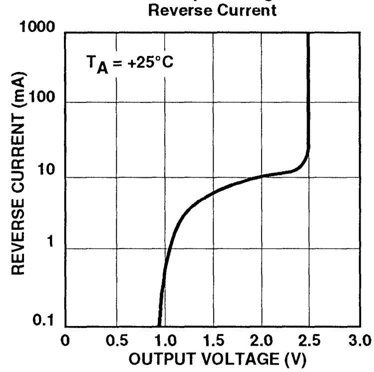
TC04: Forward Voltage vs
Forward Current



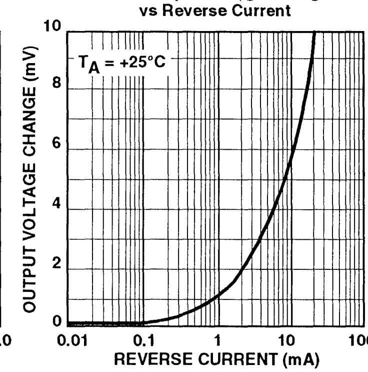
TC04
Response Time



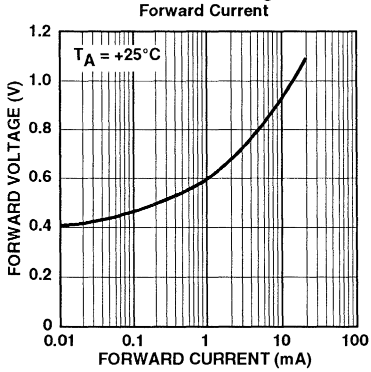
TC05: Output Voltage vs
Reverse Current



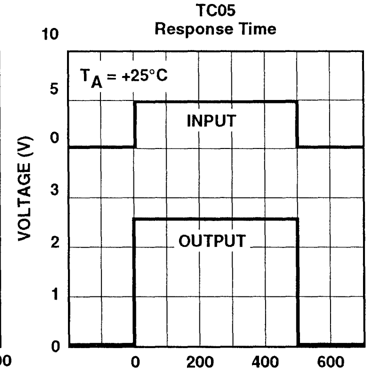
TC05: Output Voltage Change
vs Reverse Current



TC05: Forward Voltage vs
Forward Current



TC05
Response Time



Section 8

Chopper-Stabilized Operational Amplifiers

8

TELEDYNE COMPONENTS

TC900

LOW POWER, CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

FEATURES

- **Low Power Dissipation .... 2 mW**
- **Low Power Supply Current .... 140 μA**
- **Low-Input Offset Voltage .... 5 μV Max**
- **Low-Input Offset Voltage Drift .... 0.05 μV/°C Max**
- **High-Impedance Differential CMOS Inputs ... $10^{12}\Omega$**
- **High Open-Loop Voltage Gain .... 120 dB Min**
- **Low Input Noise Voltage .... 0.3 $\mu V_{P\text{-}P}$**
- **High Slew Rate .... 0.2 V/μs**
- **Unity-Gain Stable**
- **Available in 8-Pin DIP and SO**

GENERAL DESCRIPTION

The TC900 is a low power, precision operational amplifier. Its 200 μA maximum supply current reduces device power requirements over 15 times, compared to 7650 devices.

Offset voltage is a low 5 μV with drift at 0.05 μV/°C. Input offset voltage (V_{OS}) errors are removed and adjustment potentiometers are not necessary. The chopper-stabilized error-correction technique keeps offset voltage errors near zero throughout the device's operating temperature range.

The TC900 performance advantages are achieved without additional manufacturing complexity and costs incurred with laser or "zener zap" V_{OS} trim techniques. The TC900 is one of the lowest cost, low power, precision operational amplifiers available.

The TC900 nulling scheme corrects both DC V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} errors. Offset-nulling voltages are stored on two user-supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. The nulling scheme keeps V_{OS}

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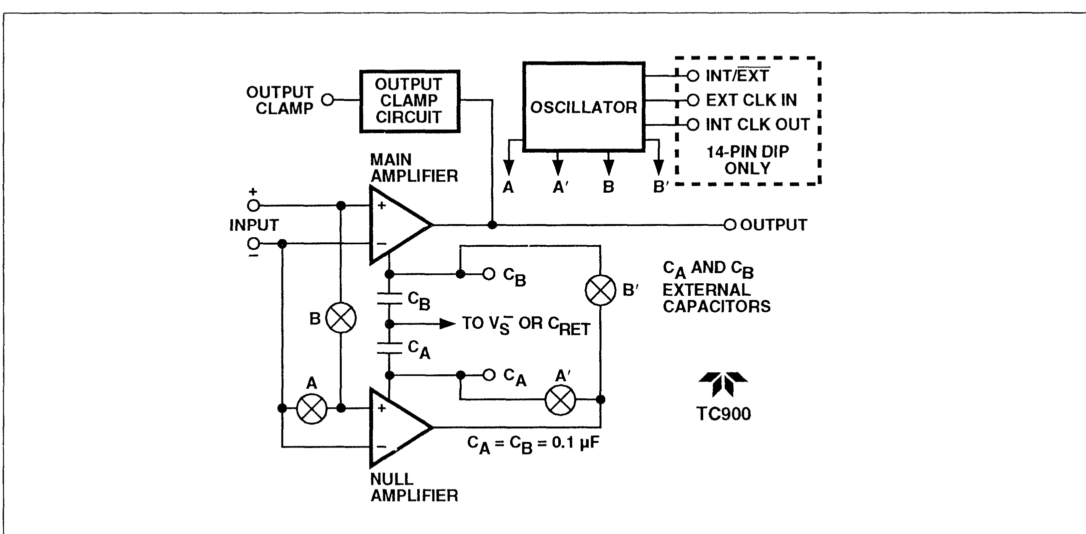
FUNCTIONAL DIAGRAM

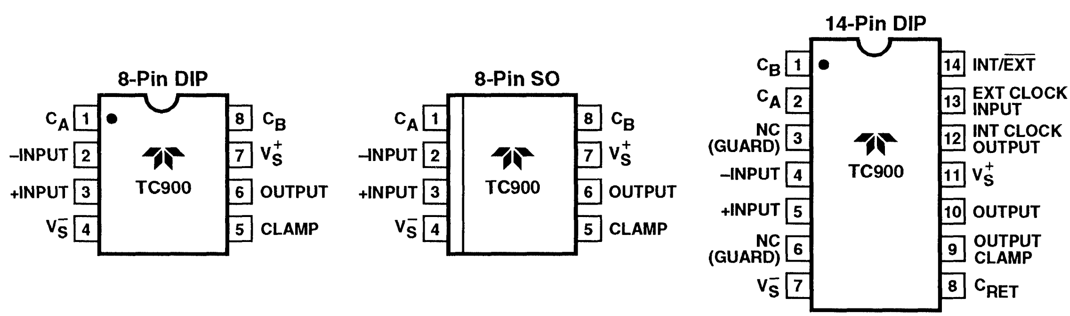


errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for V_{OS} at only one temperature.

The nulling-circuit oscillator and control circuits are integrated on-chip. Only two external V_{OS} error storage capacitors are required. The TC900 operates as a conventional operational amplifier with vastly improved input specifications. The low V_{OS} and V_{OS} drift errors make the TC900 ideal for thermocouple, thermistor, and strain gauge applications. Low DC errors and high open-loop gain make the TC900 an excellent preamplifier for precision analog-to-digital converters, such as the TC7135, TC850 and TC7109A.

The 14-pin package has an external oscillator input to drive the nulling circuitry. Both the 8-pin and 14-pin packages have an output voltage clamp circuit to minimize overload recovery time.

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

ORDERING INFORMATION

Part No.	Package	Temperature Range	Maximum V_{OS}	Maximum Supply Current
TC900ACPA	8-Pin Plastic DIP	0°C to +70°C	5 µV	200 µA
TC900ACOA	8-Pin SO	0°C to +70°C	5 µV	200 µA
TC900AIJA	8-Pin CerDIP	–25°C to +85°C	5 µV	200 µA
TC900ACPD	14-Pin Plastic DIP	0°C to +70°C	5 µV	200 µA
TC900AIJD	14-Pin CerDIP	–25°C to +85°C	5 µV	200 µA
TC900BCPA	8-Pin Plastic DIP	0°C to +70°C	15 µV	400 µA
TC900BCOA	8-Pin SO	0°C to +70°C	15 µV	400 µA
TC900BIJA	8-Pin CerDIP	–25°C to +85°C	15 µV	400 µA
TC900BCPD	14-Pin Plastic DIP	0°C to +70°C	15 µV	400 µA
TC900BIJD	14-Pin CerDIP	–25°C to +85°C	15 µV	400 µA

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) .... +18V
Input Voltage .... (V_S^+ +0.3V) to (V_S^- –0.3V)
Voltage on Oscillator Control Pins .... V_S^+ to V_S^-
Output Short-Circuit Duration .... Indefinite
Current Into Any Pin .... 10 mA
While Operating (Note 4) .... 100 µA
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Operating Temperature Range
C Device .... 0°C to +70°C
I Device .... –25°C to +85°C
Package Power Dissipation (T_A = 25°C) .... 500 mW

Static-sensitive device. Unused devices must be stored in conductive material to protect them from possible static damage. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S^+ = +5V, V_S^- = –5V, $C_A = C_B$ = 0.1 µF, T_A = +25°C

Symbol	Parameter	Test Conditions	TC900A Min	TC900A Typ	TC900A Max	TC900B Min	TC900B Typ	TC900B Max	Unit
Input									
V_{OS}	Input Offset Voltage		—	—	5	—	—	15	µV
TCV_{OS}	Input Offset Voltage vs Temperature Coefficient	Operating Temperature Range (Note 1)	—	0.02	0.05	—	0.1	0.3	µV/°C
I_{BIAS}	Average Input Bias Current (Note 5)	T_A = +25°C	—	—	50	—	—	80	pA
		0°C ≤ T_A ≤ +70°C	—	—	70	—	—	100	pA
		–25°C ≤ T_A ≤ +85°C	—	—	100	—	—	140	pA
I_{OS}	Input Offset Current	T_A = +25°C	—	0.5	—	—	0.5	—	pA
e_N	Input Noise Voltage	R_S = 100Ω, 0.1 Hz to 10 Hz	—	4	—	—	4	—	$µV_{P-P}$
		R_S = 100Ω, 0.1 to 1 Hz	—	0.3	—	—	0.3	—	$µV_{P-P}$
R_{IN}	Input Resistance		—	10^{12}	—	—	10^{12}	—	Ω
CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+–2	V_S^-	—	V_S^+–2	V
CMRR	Common-Mode Rejection Ratio	CMVR = –5V to +2V	110	130	—	100	—	—	dB
Output									
A_V	Large-Signal Voltage Gain	R_L = 10 kΩ	120	130	—	100	—	—	dB
V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10 kΩ	–4.7	—	+3.5	–4.7	—	+3.5	V
		R_L = 100 kΩ	–4.9	—	+3.9	–4.9	—	+3.9	V
	Clamp ON Current (Note 2)	R_L = 100 kΩ	20	90	200	20	90	200	µA
	Clamp OFF Current (Note 2)	–4V < V_{OUT} < 4V	—	1	—	—	1	—	pA
Dynamic									
BW	Unity-Gain Bandwidth	Unity Gain (+1)	—	0.7	—	—	0.7	—	MHz
SR	Slew Rate	C = 50 pF, R_L = 100 kΩ	—	0.2	—	—	0.2	—	V/µs
	Rise Time		—	0.5	—	—	0.5	—	µs
	Overshoot		—	18	—	—	18	—	%
f_{CH}	Internal Chopping Frequency	Pins 12–14 Open (14-Pin DIP)	—	150	—	—	150	—	Hz
Supply									
V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	4.5	—	16	V
I_S	Supply Current	No Load	—	140	200	—	—	400	µA
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±8V	120	—	—	100	—	—	dB

NOTES:
1. Operating temperature range is –25°C to +85°C for "I" grade and 0°C to +70°C for "C" grade.
2. See "Output Clamp" discussion.
3. Output clamp not connected.
4. Limiting input current to 100 µA is recommended to avoid latch-up problems.
5. Average current caused by switch charge transfer at input.

Chopper-Stabilized Operational Amplifiers

The TC900 is the first commercially-available, low-power, chopper-stabilized amplifer. Its maximum supply current is 15 times lower than the pin-compatible TC7650. Figure 1 shows how low supply current is achieved without sacrificing offset voltage or offset voltage drift performance.

Nulling-Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (pin 4) on the 8-pin device and to capacitor return (C_{RET}, pin 8) on the 14-pin device. The common connection should be made through a separate PC trace or wire to avoid voltage drops. Internally, V_S^- is connected to C_{RET}. (See Figure 2.)

Clock Operation

The internal oscillator is set for a 150 Hz nominal chopping frequency. With the 14-pin device, the 150 Hz internal chopping frequency is available at the INTERNAL CLOCK OUTPUT (pin 12). A 300 Hz nominal signal will be present at the EXTERNAL CLOCK INPUT pin (pin 13) with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before a divide-by-two operation.

The 14-pin device can be driven by an external clock. The INT/$\overline{\text{EXT}}$ input (pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/$\overline{\text{EXT}}$ must be tied to V_S^- (pin 7) to disable the internal clock. The external clock signal is applied to the external clock input.

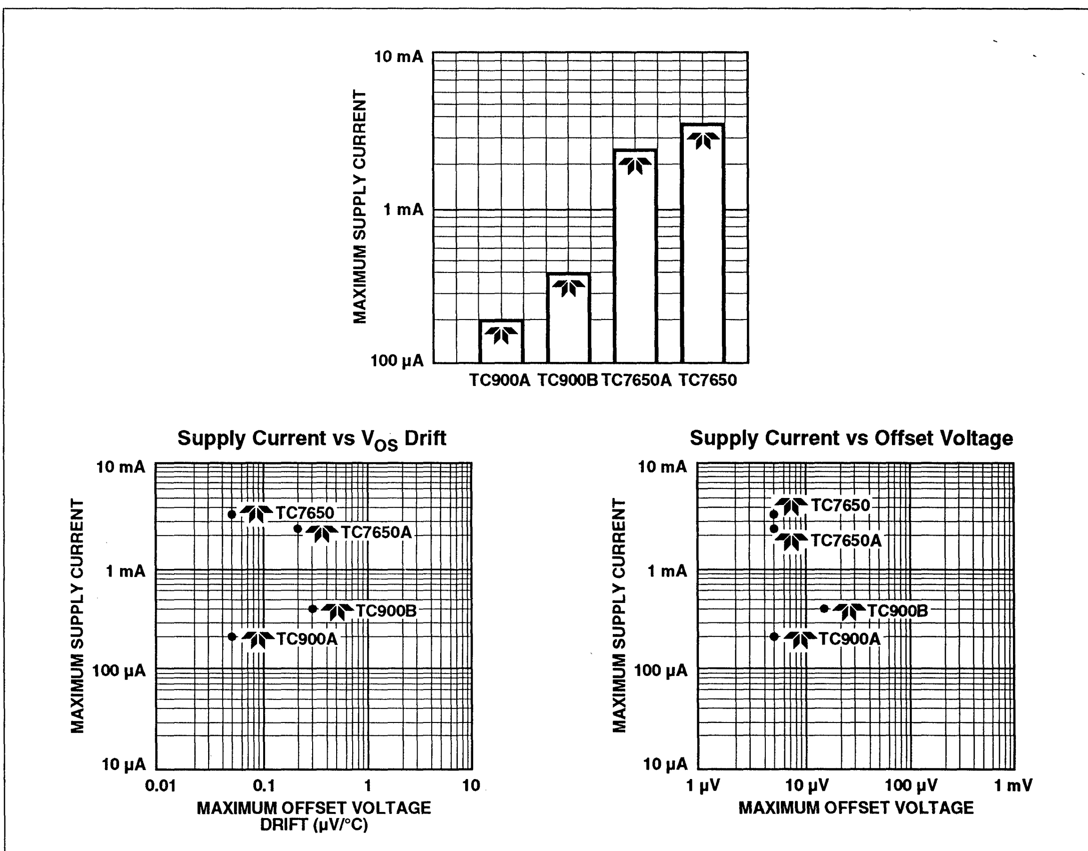


Figure 1

LOW POWER, CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

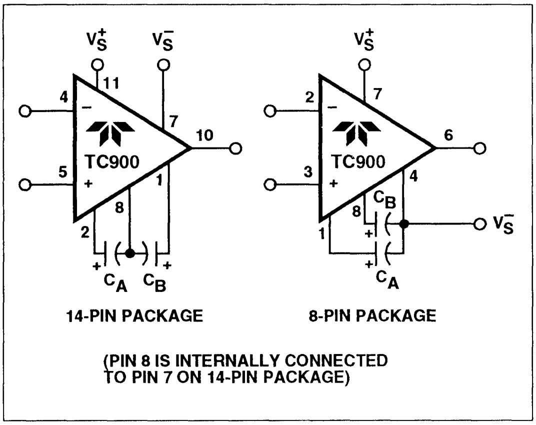


Figure 2. Nulling Capacitor Connection

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6V, and between V_S^+ and V_S^+ –6V for higher supply voltages.

At low frequencies, the external-clock duty cycle is not critical, since an internal divide-by-two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50% to 80% external-clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input, so that it is low during the time an overload signal is applied, neither capacitor will be charged. Leakage currents

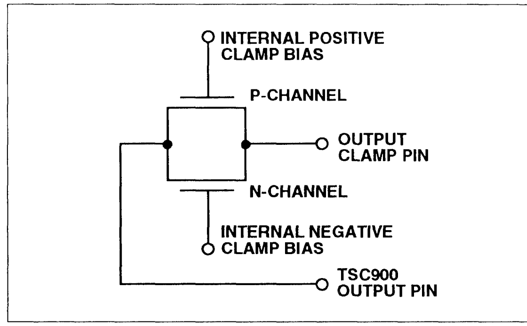


Figure 3. Internal Clamp Circuit

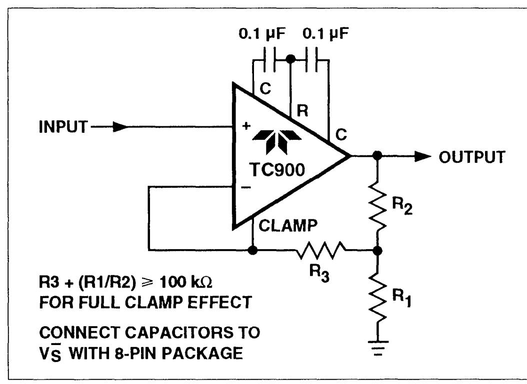


Figure 4. Noninverting Amplifier With Optional Clamp

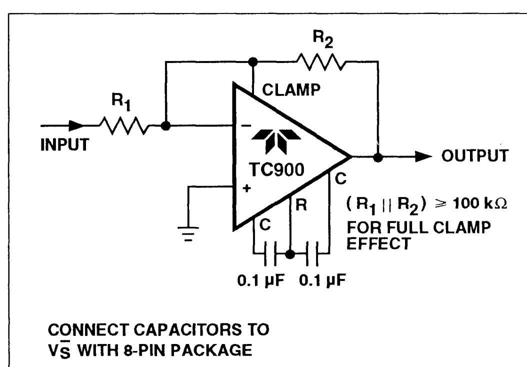


Figure 5. Inverting Amplifier With Optional Clamp

Output Clamp

Chopper-stabilized systems can show long overload recovery times. If the output is driven to either supply rail, output saturation occurs; the inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TC900 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3, with typical inverting and noninverting circuit connections shown in Figures 4 and 5. Output voltage versus clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be >100 kΩ.

Static Protection

All device pins are static-protected. However, strong static fields and discharges should be avoided, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational materials, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. Two such companies are:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072

- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520

Input Bias Current

The TC900 inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. However, the sampling causes charge transfer at the inputs. The charge transfer represents a peak impulse current of 200 nA to 290 nA at the inputs when the internal clock makes a transition.

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances, this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, voltages greater than 0.3V beyond the supply rails should not be applied to any pin. In general, the amplifier supplies must be established at the same time (or before) any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latch-up.

Thermoelectric Potentials

Precision DC measurements are ultimately limited by thermoelectric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages, typically around 0.1 μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the benefits extremely low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movements, especially those caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible, and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and separation from surrounding heat-dissipating elements is advised.

Pin Compatibility

On the 8-pin TC900, the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open, or are used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, the replacement of the offset null potentiometer between pins 1 and 8 by two capacitors from the pins to V_S^- will convert the OP05/07 pin configuration for TC900 operation. For LM108 devices, the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pinouts are modified similarly by removing any circuit connections to pin 5. On the TC900, pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

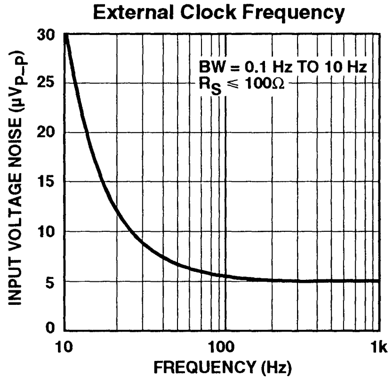
The minor modifications needed to retrofit a TC900 to existing sockets operating at reduced power supply voltages make prototyping and circuit verification straightforward.

Component Selection

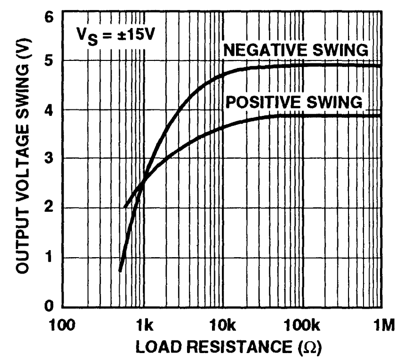
The two required capacitors, C_A and C_B, have optimum values, depending on the clock or chopping frequency. For the present internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock, if used. High-quality, film-type capacitors (such as Mylar) are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to microvolt levels.

TYPICAL CHARACTERISTICS CURVES

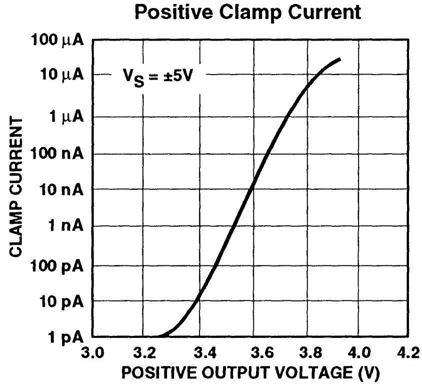
Input Voltage Noise vs External Clock Frequency



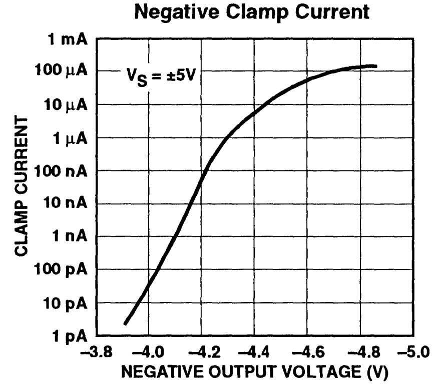
Output Voltage Swing vs Load Resistance



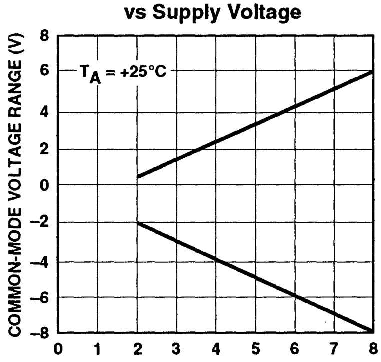
Positive Clamp Current



Negative Clamp Current

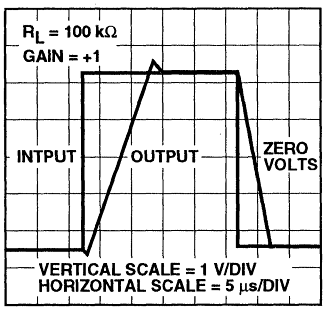


Input Common-Mode Voltage Range vs Supply Voltage

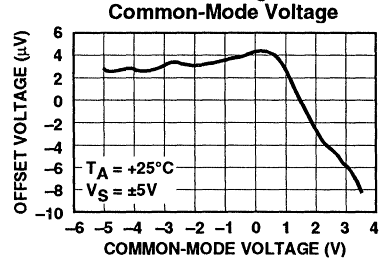


TYPICAL CHARACTERISTICS CURVES (Cont.)

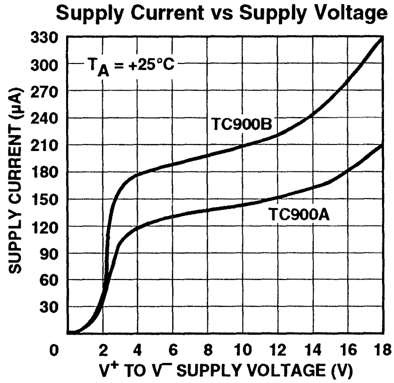
Slew Rate



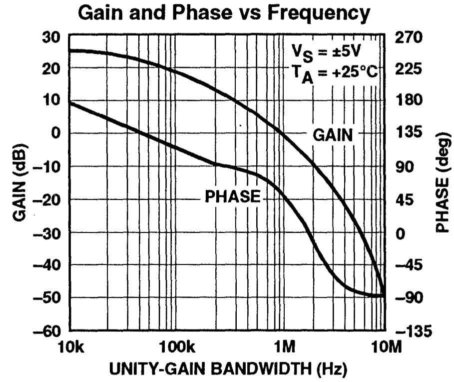
Offset Voltage vs Common-Mode Voltage



Supply Current vs Supply Voltage



Gain and Phase vs Frequency



MONOLITHIC, AUTO-ZEROED OPERATIONAL AMPLIFIER

FEATURES

- **Second-Generation Monolithic, Chopper-Stabilized Op-Amp**
- **No External Capacitors Required**
- **Single-Supply Operation ....±15V or 5V to 32V**
- **Supply Current .... 450 μA at 15V, Typ**
- **Input Offset Voltage ....7 μV, Typ**
- **Common-Mode Rejection Ratio ....140 dB, Typ**
- **Open-Loop Gain ....140 dB Into 10k Load, Typ**
- **Output Noise ....5 μV at 10 Hz Bandwidth**
- **Pinout Compatible With ICL7650**
- **Lowest Parts Count Chopper Op-Amp**

GENERAL DESCRIPTION

The TC901 is a monolithic, auto-zeroed operational amplifier. It is a second-generation design of the TC91X series, the world's first monolithic, CMOS chopper-stabilized op-amps with on-chip capacitors. This second-generation design allows use of higher supply voltages (±15V or single supply 30V), while decreasing noise.

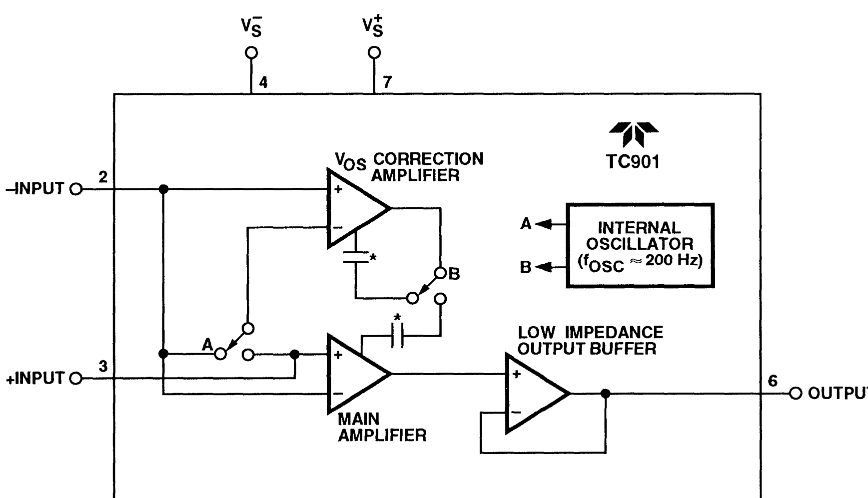
Elimination of the external capacitors allows the designer to increase reliability, lower cost, and simplify design by lowering parts count. Substantial space savings can be realized on PC board layouts. Other chopper-stabilized op-amps (such as the ICL7650/7652 and LTC1052) require external capacitors; therefore, these advantages are lost.

Since the TC901 is an auto-zeroing op-amp, input offset voltage is very low. More important, there is almost zero drift with time. This eliminates production line adjustments, as well as periodic calibration.

This device is supplied in 8-pin mini-dual-in-line and plastic SO (small outline) packages. It is pin compatible with bipolar, CMOS, JFET and chopper-stabilized op-amps using the industry-standard 741 pinout.

8

FUNCTIONAL DIAGRAM



NOTES: 1. *Internal capacitors; external capacitors not required.
2. Pin numbers are for 8-pin DIP.

TC901

Notable electrical characteristics are low supply current (450 µA, typical), single-supply operation (5V to 32V), low input offset voltage (7 µV, typical), low noise (<5 μV_{P-P}, typical, for a 10 Hz bandwidth), and fast recovery from saturation without the use of external clamp circuitry.

Pin Compatibility

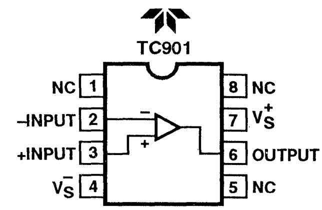
The CMOS TC901 is pin compatible with other chopper-stabilized amplifiers, such as the 7650, 7652 and 1052. Amplifiers such as the 7650 require 0.1 µF external capacitors connected to pins 1 and 8. The TC901 includes the chopper capacitors on-chip, so external capacitors are not required. Since pins 1, 5 and 8 of the TC901 are not connected, the TC901 can directly replace other chopper-stabilized amplifiers in existing circuits.

The TC901 pinout also matches many popular bipolar and JFET op-amps, such as the OP-07, OP20, LM101, LM108, 356 and 741. In many applications that operate from ±15V power supplies, the TC901 offers superior electrical performance and is a functional pin-compatible replacement. Offset voltage correction potentiometers, compensation capacitors, and chopper-stabilization capacitors can be removed when retrofitting existing equipment designs. System parts count, assembly time, and system cost are reduced, while reliability and performance are improved.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC901COA	8-Pin SO	0°C to +70°C
TC901CPA	8-Pin Plastic DIP	0°C to +70°C
TC901IJA	8-Pin CerDIP	–25°C to +85°C
TC901MJA	8-Pin CerDIP	–55°C to +125°C

PIN CONFIGURATION (DIP and SO)



NC = NO INTERNAL CONNECTION

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) .... +36V
Input Voltage .... (V_S^++0.3V) to (V_S^-–0.3V)
Current Into Any Pin .... 10 mA
While Operating .... 100 µA
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Operating Temperature Range
C Device .... 0°C to +70°C
I Device .... –25°C to +85°C
M Device .... –55°C to +125°C
Package Power Dissipation (T_A = +25°C)
CerDIP .... 500 mW
Plastic DIP .... 375 mW

Static-sensitive device. Appropriate precautions should be taken when handling, shipping, or storing these devices. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

ELECTRICAL CHARACTERISTICS: V_S ±15V, T_A = +25°C, unless otherwise indicated (each amplifier).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage (Figure 2)	T_A = +25°C	—	7	15	µV
V_{OS}/TC	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ +70°C	—	0.05	0.15	µV/°C
I_{BIAS}	Average Input Bias Current	T_A = +25°C 0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C	— — —	30 0.2 0.2	50 10 10	pA nA nA
I_{OS}	Average Input Offset Current	T_A = +25°C	—	50	100	pA
e_N	Input Voltage Noise (Figure 1B)	0.1 to 1 Hz, R_S ≤ 100Ω	—	1.2	—	μV_{P-P}
e_N	Input Voltage Noise (Figure 1A)	0.1 to 10 Hz, R_S ≤ 100Ω	—	5	—	μV_{P-P}
CMRR	Common-Mode Rejection Ratio	V_S^- ≤ V_{CM} ≤ V_S^+ –2V	120	140	—	dB
CMVR	Common-Mode Voltage Range	V_S = ±5V to ±15V	V_S^-	—	V_S^+ –2	V
A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_S = ±15V	120	140	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^-+1	—	V_S^+ –1.2	V
BW	Closed-Loop Bandwidth (Figure 7)	Closed-Loop Gain = +1	—	0.8	—	MHz
sr	Slew Rate	R_L = 10 kΩ, C_L = 50 pF	—	2	—	V/µs
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	120	140	—	dB
V_S	Operating Supply Voltage Range	Note 1	±3	—	±16	V
I_S	Quiescent Supply (Figure 2)	V_S = ±15V	—	0.45	0.6	mA

NOTE: 1. Single supply operation: V_S^+ = +5V to +32V.

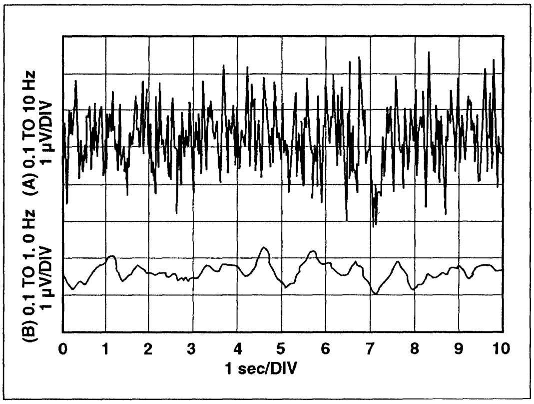


Figure 1 Input Voltage Noise

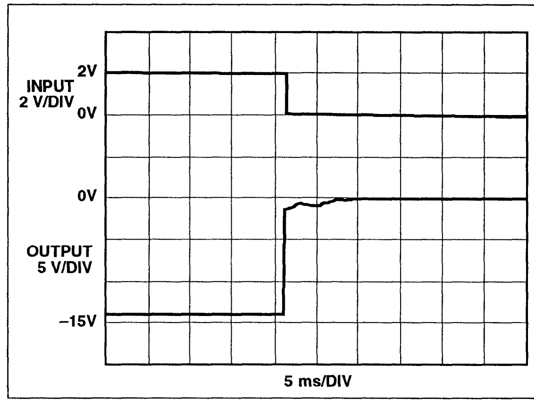


Figure 3 Recovery From Negative Saturation

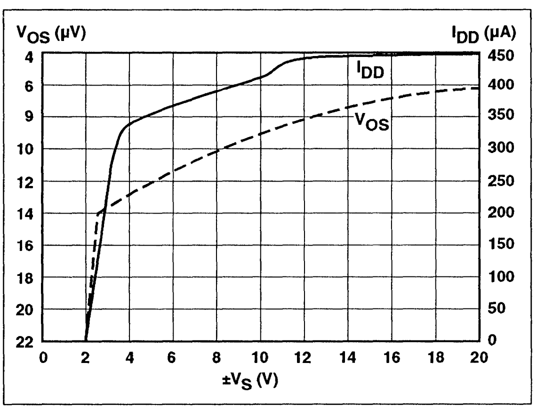


Figure 2 V_{OS} and I_{DD} vs Supply Voltage

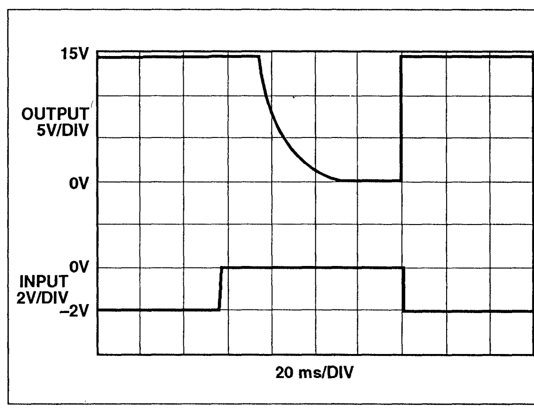


Figure 4 Recovery From Positive Saturation

Overload Recovery

The TC901 recovers quickly from output saturation. Typical recovery time from positive output saturation is 20 ms. Negative output saturation recovery time is typically 5 ms.

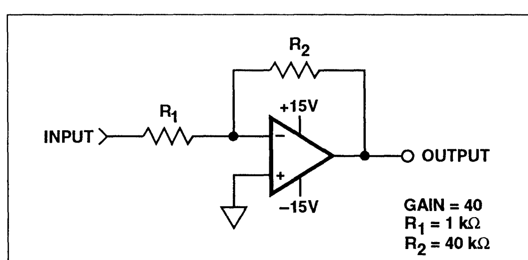


Figure 5 Saturation Test Circuit

Thermocouple Errors

Heating one joint of a loop made from two different metallic wires causes current flow. This is known as the Seebeck effect. By breaking the loop, an open-circuit voltage (Seebeck voltage) can be measured. Junction temperature and metal type determine the magnitude. Typical values are 0.1 μV/°C to 10 μV/°C. Thermal-induced voltages can be many times larger than the TC901's offset voltage drift. Unless unwanted thermocouple potentials can be controlled, system performance will be less than optimum.

Unwanted thermocouple junctions are created when leads are soldered or sockets/connectors are used. Low thermoelectric coefficient solder can reduce errors. A 60% Cd/40% Sn Pb solder has one-tenth the thermal voltage of common 64% Sn/36% Pb solder at a copper junction.

The number and type of dissimilar metallic junctions in the input circuit loop should be balanced. If the junctions are kept at the same temperature, their summation will add to zero-canceling errors (Figure 6).

Shielding precision analog circuits from air currents — especially those caused by power dissipating components and fans — will minimize temperature gradients and minimize thermocouple-induced errors.

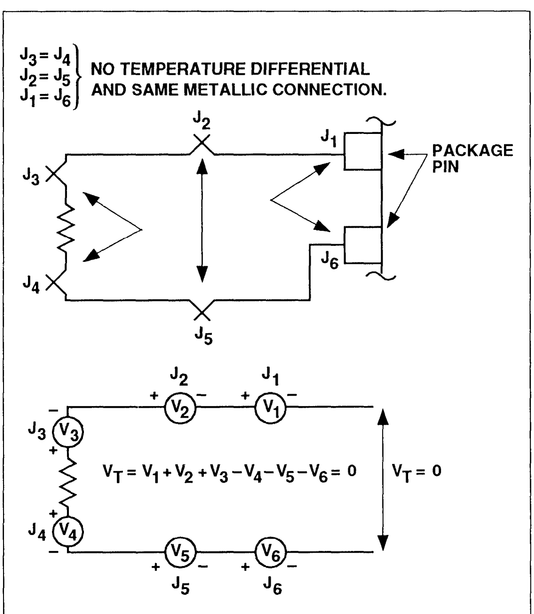


Figure 6 Unwanted Thermocouple Errors Eliminated by Reducing Thermal Gradients and Balancing Junctions

Avoiding Latch-Up

Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and excessive power dissipation. TC901's power supply should be established at the same time (or before) input signals are applied. If this is not possible, input current should be limited to 100 μA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers establish "static safe" CMOS component handling areas. Two such companies are:

- 3M
  Static Control Systems Division
  223-23W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

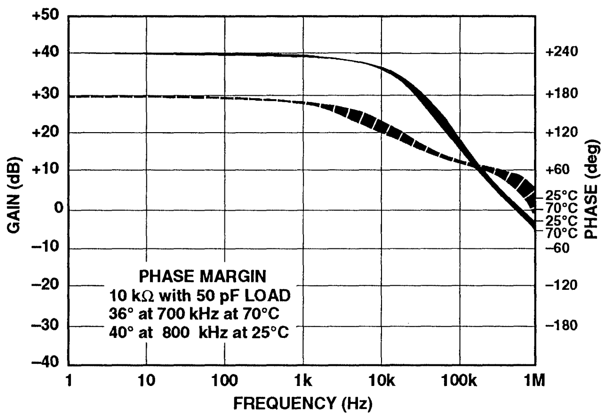
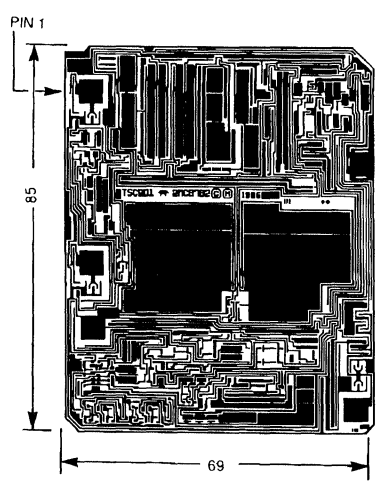


Figure 7 Phase-Gain

BONDING DIAGRAM



TELEDYNE COMPONENTS

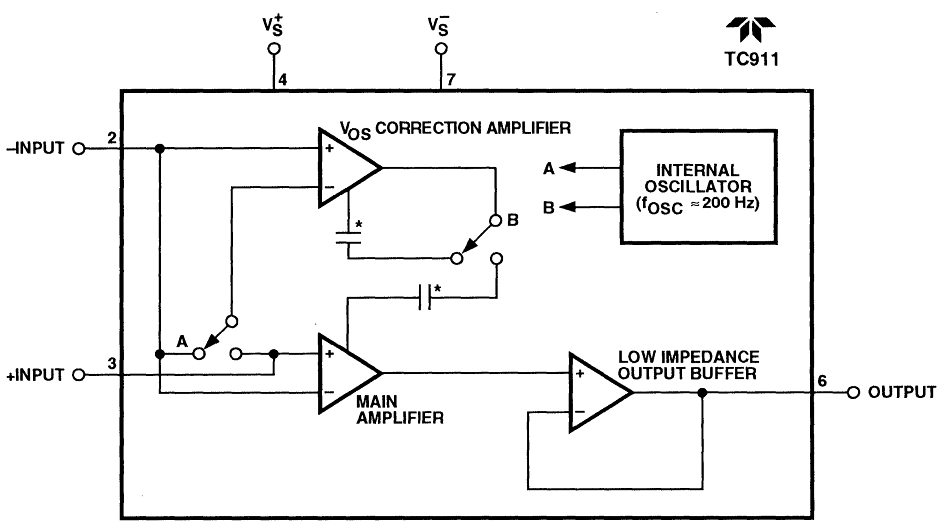
AUTO-ZEROED MONOLITHIC OPERATIONAL AMPLIFIER

FEATURES

- First Monolithic Chopper-Stabilized Amplifier With On-Chip Nulling Capacitors
- Offset Voltage .... 5 μV
- Offset Voltage Drift .... 0.05 μV/°C
- Low Supply Current .... 350 μA
- High Common-Mode Rejection .... 116 dB
- Single Supply Operation .... 4.5V to 16V
- High Slew Rate .... 2.5 V/μs
- Wide Bandwidth .... 1.5 MHz
- High Open-Loop Voltage Gain (R_L = 10 kΩ) .... 120 dB
- Low Input Voltage Noise (0.1 Hz to 1 Hz) .... 0.65 μV_{P-P}
- Pin Compatible With ICL7650
- Lower System Parts Count

8

FUNCTIONAL DIAGRAM



***NOTE:** Internal capacitors. No external capacitors required.

AUTO-ZEROED MONOLITHIC OPERATIONAL AMPLIFIER

TC911

GENERAL DESCRIPTION

The TC911 CMOS auto-zeroed operational amplifier is the first complete monolithic chopper-stabilized amplifier. Chopper operational amplifiers like the ICL7650/7652 and LTC1052 require user-supplied, external offset compensation storage capacitors. **External capacitors are not required with the TC911.** Just as easy to use as the conventional 741 type amplifier, the TC911 significantly reduces offset voltage errors. Pinout matches the OP07/741/7650 8-pin mini-DIP configuration.

Several system benefits arise by eliminating the external chopper capacitors: lower system parts count; reduced assembly time and cost; greater system reliability; reduced PC board layout effort and greater board area utilization. Also, space savings can be significant in multiple-amplifier designs.

Electrical specifications include 15 µV maximum offset voltage, 0.15 µV/°C maximum offset voltage temperature coefficient. Offset voltage error is five times lower than the premium OP07E bipolar device. The TC911 improves offset drift performance by eight times.

Low offset voltage errors eliminate trim procedures during manufacturing, periodic recalibrations, and reliability problems caused by damaged or misadjusted trim potentiometers.

The TC911 automatically corrects offset voltage drift with time. Operational amplifier long-term drift is less easily controlled and more expensive to maintain when low offset errors are obtained by trimming thin-film resistors. The TC911 internal circuits correct errors repetitively at a 200 Hz rate. Long-term drift is effectively eliminated.

The TC911 operates from dual or single power supplies. Supply current is typically 350 µA. Single 4.5V to 16V supply operation is possible, making single 9V battery operation possible. The TC7660 DC-to-DC converter can easily supply a negative potential in dual-supply applications where only a +5V system supply is available.

Open-loop voltage gain is 115 dB minimum with a 10 kΩ load. Unity gain bandwidth is 1.5 MHz. Slew rate is 2.5 V/µs. Common-mode rejection ratio is 116 dB. Input common-mode range extends from 2V below the positive supply to the negative supply.

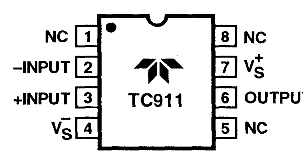
The TC911 is available in three package types: 8-pin plastic DIP, ceramic DIP and SO package. Die are available for hybrid applications.

For precision dual- and quad-monolithic chopper-stabilized amplifiers, see the TC913 (dual) and TC914 (quad) data sheets.

ORDERING INFORMATION

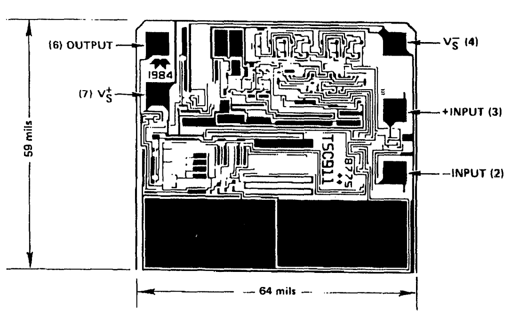
Part No.	Package	Temperature Range	Maximum Offset Voltage
TC911ACPA	8-Pin Plastic DIP	0°C to +70°C	15 µV
TC911ACOA	8-Pin SO	0°C to +70°C	15 µV
TC911BCPA	8-Pin Plastic DIP	0°C to +70°C	30 µV
TC911BCOA	8-Pin SO	0°C to +70°C	30 µV
TC911AIJA	8-Pin CerDIP	−25°C to +85°C	15 µV
TC911BIJA	8-Pin CerDIP	−25°C to +85°C	30 µV

PIN CONFIGURATION (SO and DIP)



NC = NO INTERNAL CONNECTION

BONDING DIAGRAM



NOTES: 1. Back of die is common to V_{CC}.
2. Back of die is not metalized.

AUTO-ZEROED MONOLITHIC OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) ....+18V
Input Voltage ....(V_S^++0.3V) to (V_S^-–0.3V)
Current into Any Pin ....10 mA
While Operating ....100 µA
Storage Temperature Range ....–65°C to +150°C
Lead Temperature (Soldering, 10 sec) ....+300°C
Operating Temperature Range
C Device ....0°C to +70°C
I Device ....–25°C to +85°C

Package Power Dissipation (T_A = +25°C)
CerDIP ....500 mW
Plastic DIP and SO ....375 mW

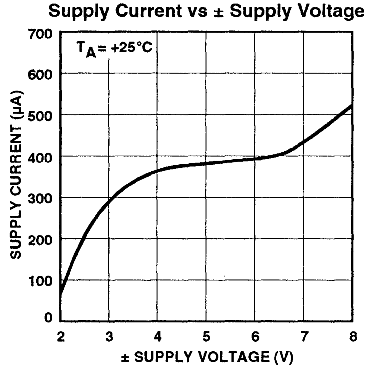
Static-sensitive device. Unused devices should be stored in conductive material. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

ELECTRICAL CHARACTERISTICS: V_S = ±5V, T_A = +25°C, unless otherwise indicated.

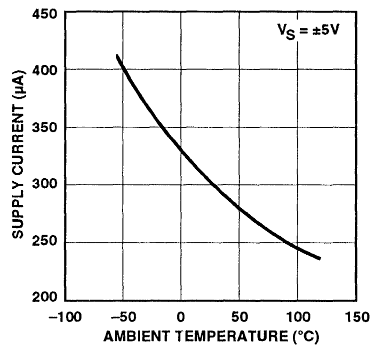
Symbol	Parameter	Test Conditions	TC911A Min	TC911A Typ	TC911A Max	TC911B Min	TC911B Typ	TC911B Max	Unit
V_{OS}	Input Offset Voltage	T_A = +25°C	—	5	15	—	15	30	µV
TCV_{OS}	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C	— —	0.05 0.05	0.15 0.15	— —	0.1 0.1	0.25 0.25	µV/°C µV/°C
I_B	Average Input Bias Current	T_A = +25°C 0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C	— — —	— — —	70 3 4	— — —	— — —	120 4 6	pA nA nA
I_{OS}	Average Input Offset Current		—	5	20	—	10	40	pA
e_N	Input Voltage Noise	0.1 to 1 Hz, R_S ≤ 100Ω 0.1 to 10 Hz, R_S ≤ 100Ω	— —	0.65 11	— —	— —	0.65 11	— —	μV_{P-P} μV_{P-P}
CMRR	Common-Mode Rejection Ratio	V_S^- ≤ V_{CM} ≤ V_S^+ – 2.2	110	116	—	105	110	—	dB
CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+–2	V_S^-	—	V_S^+–2	V
A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4V	115	120	—	110	120	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^-+0.3	—	V_S^+–0.9	V_S^-+0.3	—	V_S^+–0.9	V
BW	Closed Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pF	—	2.5	—	—	2.5	—	V/µs
PSRR	Power Supply Rejection Ratio	±3.3V to ±5.5V	112	—	—	105	—	—	dB
V_S	Operating Supply Voltage Range	Split Supply Single Supply	±3 4.5	— —	±8 16	±3 4.5	— —	±8 16	V V
I_S	Quiescent Supply Current	V_S = ±5V	—	350	600	—	—	800	µA

TYPICAL CHARACTERISTICS CURVES

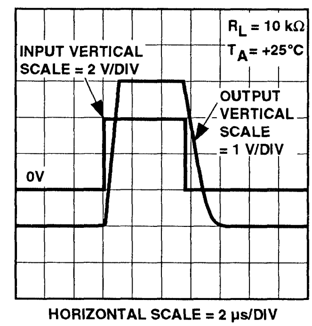
Supply Current vs ± Supply Voltage



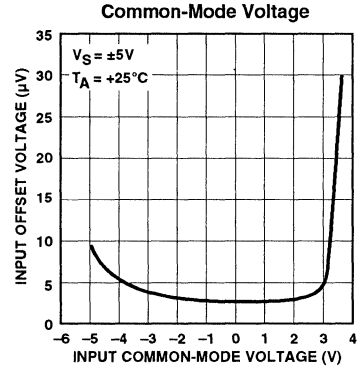
Supply Current vs Temperature



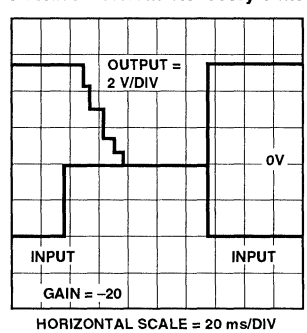
Large Signal Output Switching Waveform



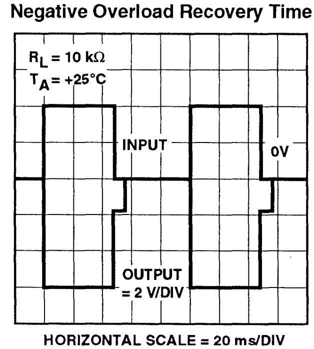
Input Offset Voltage vs Common-Mode Voltage



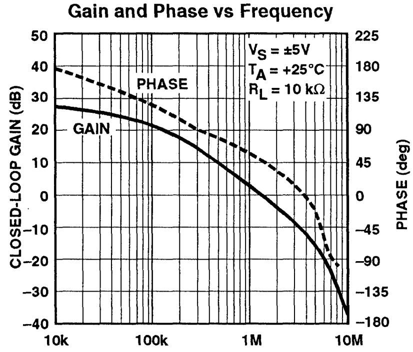
Positive Overload Recovery Time



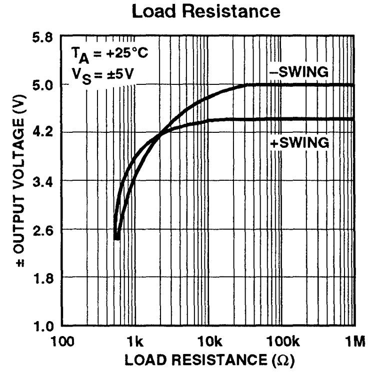
Negative Overload Recovery Time



Gain and Phase vs Frequency



Output Voltage Swing vs Load Resistance



AUTO-ZEROED MONOLITHIC OPERATIONAL AMPLIFIER

Pin Compatibility

The CMOS TC911 is pin compatible with the GE/Intersil ICL7650 chopper-stabilized amplifier. The ICL7650 must use external 0.1 μF capacitors connected at pins 1 and 8. **With the TC911, external offset voltage error canceling capacitors are not required.** On the TCS911 pins 1, 8 and 5 are not connected internally. The ICL7650 uses pin 5 as an optional output clamp connection. External chopper capacitors and clamp connections are not necessary with the TC911. External circuits connected to pins 1, 8 and 5 will have no effect. The TC911 can be quickly evaluated in existing ICL7650 designs. Since external capacitors are not required, system part count, assembly time, and total system cost are reduced. Reliability is increased and PC board layout eased by having the error storage capacitors integrated on the TC911 chip.

The TC911 pinout matches many existing op-amps: 741, LM101, LM108, OP05–OP08, OP20, OP21, ICL7650 and ICL7652. In many applications operating from +5V supplies the TC911 offers superior electrical performance and can be a functional pin-compatible replacement. Offset voltage correction potentiometers, compensation capacitors, and chopper-stabilization capacitors can be removed when retrofitting existing equipment designs.

Thermocouple Errors

Heating one joint of a loop made from two different metallic wires causes current flow. This is known as the Seebeck effect. By breaking the loop, an open circuit voltage (Seebeck voltage) can be measured. Junction temperature and metal type determine the magnitude. Typical values are 0.1 μV/°C to 10 μV/°C. Thermal-induced voltages can be many times larger than the TC911 offset voltage drift. Unless unwanted thermocouple potentials can be controlled, system performance will be less than optimum.

Unwanted thermocouple junctions are created when leads are soldered or sockets/connectors are used. Low thermo-electric coefficient solder can reduce errors. A 60% Sn/36% Pb solder has 1/10 the thermal voltage of common 64% Sn/36% Pb solder at a copper junction.

The number and type of dissimilar metallic junctions in the input circuit loop should be balanced. If the junctions are kept at the same temperature, their summation will add to zero-canceling errors (Figure 1).

Shielding precision analog circuits from air currents — especially those caused by power dissipating components and fans — will minimize temperature gradients and thermocouple-induced errors.

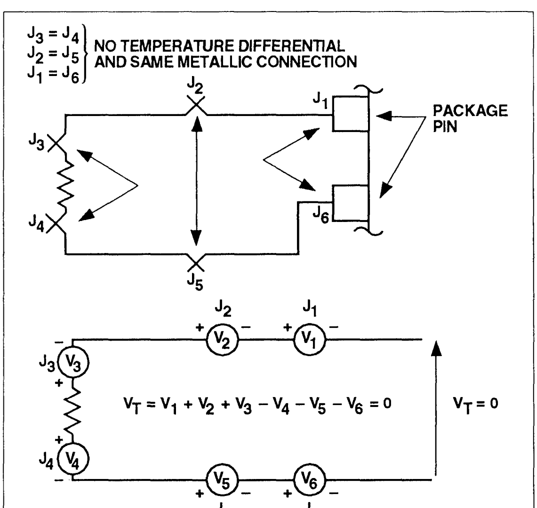


Figure 1. Unwanted Thermocouple Errors Eliminated by Reducing Thermal Gradients and Balancing Junctions

Avoiding Latch-Up

Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and excessive power dissipation. TC911 power supplies should be established at the same time or before input signals are applied. If this is not possible input current should be limited to 0.1 mA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers to establish "static safe" CMOS component handling areas. A partial company list is:

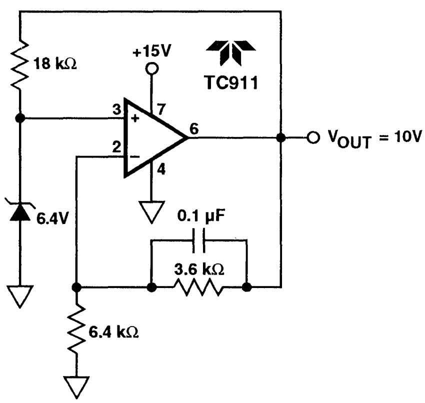
- 3M
  Static Control Systems Div
  223-23W EM Center
  St Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

Overload Recovery

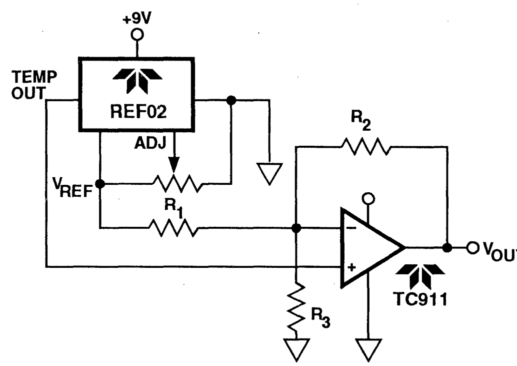
The TC911 recovers quickly from the output saturation. Typical recovery time from positive output saturation is 20 ms. Negative output saturation recovery time is typically 5 ms.

TYPICAL APPLICATIONS

10-Volt Precision Reference



Thermometer Circuit

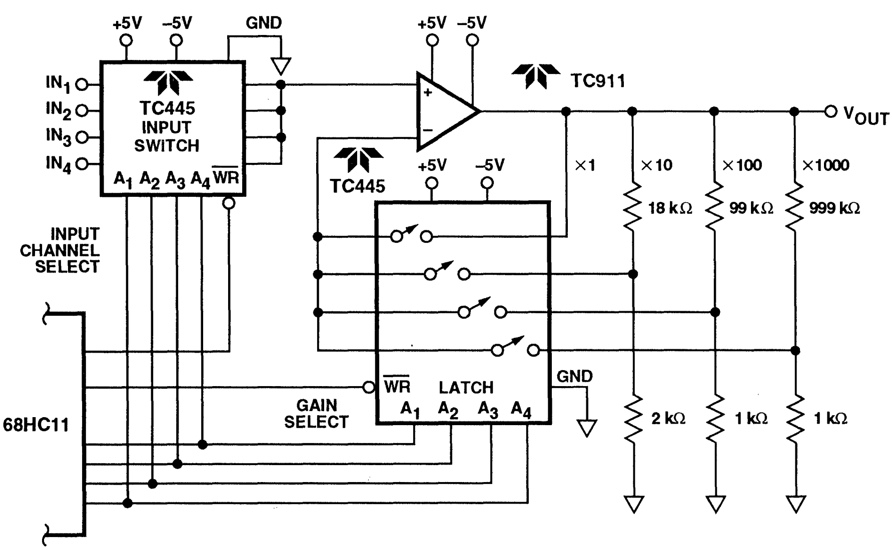


$$V_{OUT} = V_{TEMP}\left[1 + R_2\left(\frac{R_3 + R_1}{R_3 \parallel R_1}\right)\right] - \left[V_{REF}\,\frac{R_2}{R_1}\right]$$

$$\frac{d\,V_{OUT}}{dT} = \left[1 + R_2\left(\frac{R_3 + R_1}{R_3 \parallel R_1}\right)\right]\frac{d\,(V_{TEMP})}{dT} \approx K\ (2.1\ \mathrm{mV/^\circ C})$$

$$K = 1 + \frac{R_2}{R_3 \parallel R_1}$$

Programmable Gain Amplifier With Input Multiplexer



TELEDYNE COMPONENTS

TC913

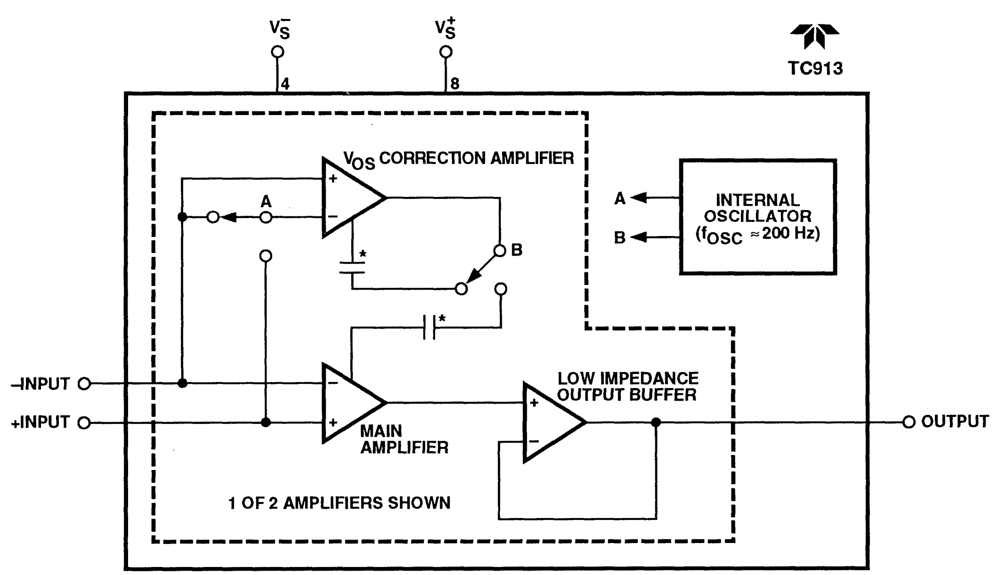
DUAL AUTO-ZEROED OPERATIONAL AMPLIFIER

FEATURES

- First Monolithic Dual Auto-Zeroed Operational Amplifier
- Chopper Amplifier Performance Without External Capacitors
  - — V_{OS} .... 15 µV Max
  - — V_{OS} Drift .... 0.15 µV/°C Max
  - — Saves Cost/Assembly of Four "Chopper" Capacitors
- SO Packages Available
- High DC Gain .... 120 dB
- Low Supply Current .... 650 µA
- Low Input Voltage Noise (0.1 Hz to 10 Hz) .... 0.65 μV_{P-P}
- Wide Common-Mode Voltage Range .... V_S^- to V_S^+ –2V
- High Common-Mode Rejection .... 116 dB
- Dual or Single Supply Operation .... ±3V to ±8V
  +4.5V to +16V
- Excellent AC Operating Characteristics
  - — Slew Rate .... 2.5 V/µs
  - — Unity-Gain Bandwidth .... 1.5 MHz
- Pin Compatible With LM358, OP14, MC1458, ICL7621, TL082, TLC322

8

FUNCTIONAL DIAGRAM



*NOTE: Internal capacitors. No external capacitors required.

DUAL AUTO-ZEROED OPERATIONAL AMPLIFIER

TC913

GENERAL DESCRIPTION

The TC913 is the world's first complete monolithic, dual auto-zeroed operational amplifier. The TC913 sets a new standard for low-power, precision dual-operational amplifiers. Chopper-stabilized or auto-zeroed amplifiers offer low offset voltage errors by periodically sampling offset error, and storing correction voltages on capacitors. Previous single amplifier designs required two user-supplied, external 0.1 μF error storage correction capacitors — much too large for on-chip integration. The unique TC913 architecture requires smaller capacitors, making on-chip integration possible. Microvolt offset levels are achieved and **external capacitors are not required.**

The TC913 system benefits are apparent when contrasted with a TC7650 chopper amplifier circuit implementation. A single TC913 replaces two TC7650's and four capacitors. Five components and assembly steps are eliminated.

The TC913 pinout matches many popular dual-operational amplifiers: OP04, TLC322, LM358, and ICL7621 are typical examples. In many applications, operating from dual 5V power supplies or single supplies, the TC913 offers superior electrical performance, and can be a functional drop-in replacement; printed circuit board rework is not necessary. The TC913's low offset voltage error eliminates offset voltage trim potentiometers often needed with bipolar and low-accuracy CMOS operational amplifiers.

The TC913 takes full advantage of Teledyne's proprietary CMOS technology. The TC913's 650 μA supply current (250 μA per amplifier) makes the TC913 the lowest power, precision dual-operational amplifier available. The 250 μA amplifier supply current does not compromise AC performance. Unity gain bandwidth is 1.5 MHz and slew rate is 2.5 V/μs.

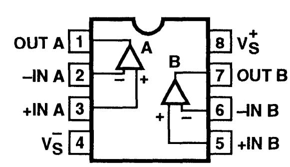
For single- and quad-operational amplifiers, see the TC911 and TC914 data sheets.

ORDERING INFORMATION

Part No.	Package	Temperature Range	Maximum Offset Voltage
TC913ACPA	8-Pin Plastic DIP	0°C to +70°C	15 μV
TC913ACOA	8-Pin SO	0°C to +70°C	15 μV
TC913BCPA	8-Pin Plastic DIP	0°C to +70°C	30 μV
TC913BCOA	8-Pin SO	0°C to +70°C	30 μV
TC913AIJA	8-Pin CerDIP	–25°C to +85°C	15 μV
TC913BIJA	8-Pin CerDIP	–25°C to +85°C	30 μV

PIN CONFIGURATION (SO and DIP)

TC913



DUAL AUTO-ZEROED OPERATIONAL AMPLIFIER

TC913

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) .... +18V
Input Voltage .... (V_S^++0.3V) to (V_S^-−0.3V)
Current into Any Pin .... 10 mA
While Operating .... 100 µA
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Operating Temperature Range
C Device .... 0°C to +70°C
I Device .... −25°C to +85°C

Package Power Dissipation (T_A = +25°C)
CerDIP .... 500 mW
Plastic DIP and SO .... 375 mW

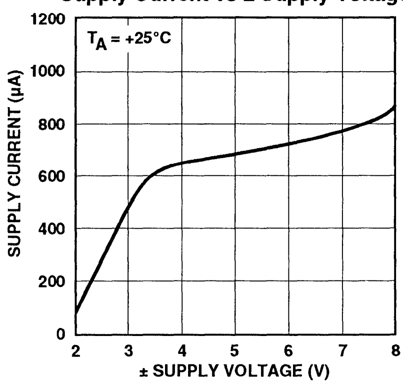
Static-sensitive device. Unused devices should be stored in conductive material. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

ELECTRICAL CHARACTERISTICS: V_S = ±5V, T_A = +25°C, unless otherwise indicated.

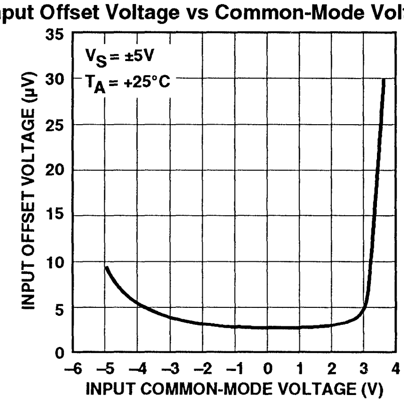
			TC913A			TC913B			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage	T_A = +25°C	—	5	15	—	15	30	µV
TCV_{OS}	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ +70°C	—	0.05	0.15	—	0.1	0.25	µV/°C
		−25°C ≤ T_A ≤ +85°C	—	0.05	0.15	—	0.1	0.25	µV/°C
I_B	Average Input Bias Current	T_A = +25°C	—	—	90	—	—	120	pA
		0°C ≤ T_A ≤ +70°C	—	—	3	—	—	4	nA
		−25°C ≤ T_A ≤ +85°C	—	—	4	—	—	6	nA
I_{OS}	Average Input Offset Current		—	5	20	—	10	40	pA
e_N	Input Voltage Noise	0.1 to 1 Hz, R_S ≤ 100Ω	—	0.6	—	—	0.6	—	$µV_{P-P}$
		0.1 to 10 Hz, R_S ≤ 100Ω	—	11	—	—	11	—	$µV_{P-P}$
CMRR	Common-Mode Rejection Ratio	V_S^- ≤ V_{CM} ≤ V_S^+ − 2.2V	110	116	—	100	110	—	dB
CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+ −2	V_S^-	—	V_S^+ −2	V
A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4V	115	120	—	110	120	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^- +0.3	—	V_S^+ −0.9	V_S^- +0.3	—	V_S^+ −0.9	V
BW	Closed-Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pF	—	2.5	—	—	2.5	—	V/µs
PSRR	Power Supply Rejection Ratio	±3.3V ≤ V_S ≤ ±5.5V	110	—	—	100	—	—	dB
V_S	Operating Supply Voltage Range	Split Supply	±3	—	±8	±3	—	±8	V
		Single Supply	4.5	—	16	4.5	—	16	V
I_S	Quiescent Supply Current	V_S = ±5V	—	0.65	0.85	—	—	1.1	mA

TYPICAL CHARACTERISTICS CURVES

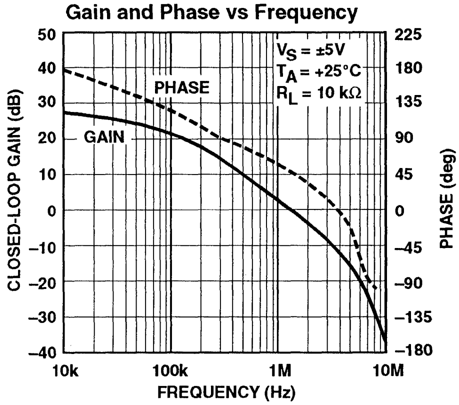
Supply Current vs ± Supply Voltage



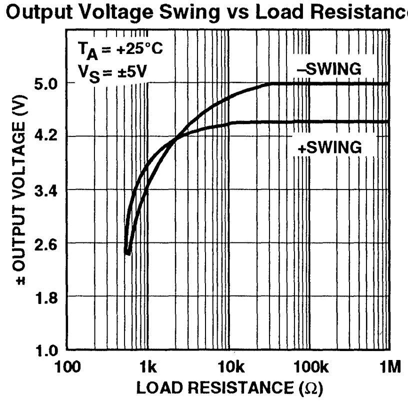
Input Offset Voltage vs Common-Mode Voltage



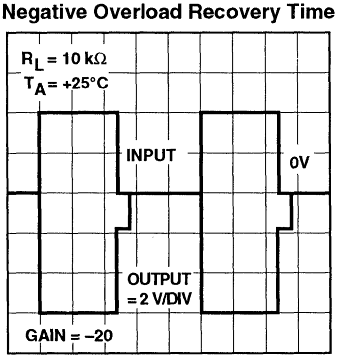
Gain and Phase vs Frequency



Output Voltage Swing vs Load Resistance

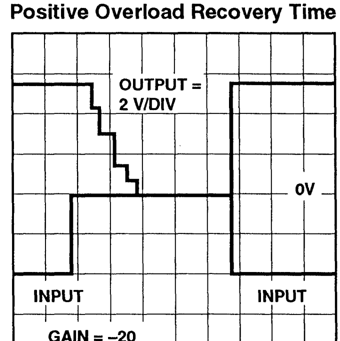


Negative Overload Recovery Time



HORIZONTAL SCALE = 20 ms/DIV

Positive Overload Recovery Time



HORIZONTAL SCALE = 20 ms/DIV

Theory of Operation

Each of the TC913's two op-amps actually consists of two amplifiers. A main amplifier is always connected from the input to the output. A separate nulling amplifier alternately nulls its own offset and then the offset of the amplifier. Since each amplifier is continuously being nulled, offset voltage drift with time, temperature, and power supply variations is greatly reduced.

All nulling circuitry is internal and the nulling operation is transparent to the user. Offset nulling voltages are stored on two internal capacitors. An internal oscillator and control logic, shared by the TC913's two amplifiers, control the nulling process.

Pin Compatibility

The TC913 pinout is compatible with OP14, LM358, MC1458, LT1013, TLC322, and similar dual op-amps. In many circuits operating from single or ±5V supplies, the TC913 is a drop-in replacement offering DC performance rivaling that of the best single op-amps.

The TC913's amplifiers include a low-impedance class AB output buffer. Some previous CMOS chopper amplifiers used a high-impedance output stage which made open-loop gain dependent on load resistance. The TC913's open-loop gain is not dependent on load resistance.

Overload Recovery

The TC913 recovers quickly from output saturation. Typical recovery time from positive output saturation is 20 ms. Negative output saturation recovery time is typically 5 ms.

Avoiding Latch-Up

Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and power dissipation. The TC913's power supplies should be established at the same time or before input signals are applied. If this is not possible, input current should be limited to 0.1 mA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers to establish "static safe" CMOS component handling areas. A partial company list is:

- 3M
  Static Control Systems Div
  223-23W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

NOTES

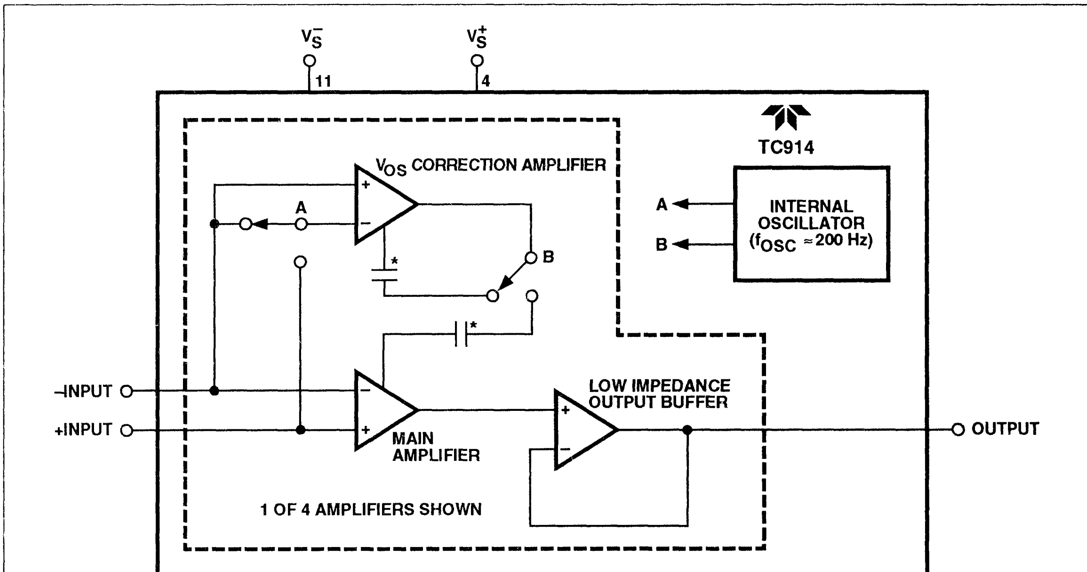
TELEDYNE COMPONENTS

QUAD AUTO-ZEROED OPERATIONAL AMPLIFIER

FEATURES

- First Monolithic Quad Auto-Zeroed Operational Amplifier
- Chopper Amplifier Performance Without External Capacitors
  - — V_{OS} .... 15 µV Max
  - — V_{OS} Drift .... 0.15 µV/°C Max
  - — Saves Cost/Assembly of Eight "Chopper" Capacitors
- High DC Gain .... 110 dB
- Low Supply Current .... 1.5 mA
- Wide Common-Mode Voltage Range .... V_S^- to V_S^+ –2V
- High Common-Mode Rejection .... 110 dB
- Dual or Single Supply Operation .... ±3V to ±8V; +4.5V to +16V
- Excellent AC Operating Characteristics
  - — Slew Rate .... 2.5 V/µs
  - — Unity-Gain Bandwidth .... 1.5 MHz
- Pin Compatible With LM358, TLC274, LM324, OP11, ICL7641/42

FUNCTIONAL DIAGRAM



*NOTE: Internal capacitors. No external capacitors required.

QUAD AUTO-ZEROED OPERATIONAL AMPLIFIER

TC914

GENERAL DESCRIPTION

The TC914 is the world's first complete monolithic quad auto-zeroed operational amplifier. The TC914 sets a new standard for low-power, precision quad operational amplifiers. Chopper-stabilized (or auto-zeroed) amplifiers offer low offset voltage errors by periodically sampling offset error, and storing correction voltages on capacitors. Previous single amplifier designs required two user-supplied, external 0.1 µF error storage correction capacitors — much too large for on-chip integration. The unique TC914 architecture requires smaller capacitors, making on-chip integration possible. Microvolt offset levels are achieved and **external capacitors are not required.**

The TC914 system benefits are apparent when contrasted with a TC7650 chopper amplifier circuit implementation. A single TC914 replaces four 7650's and eight capacitors. Eleven components and assembly steps are eliminated.

The TC914 pinout matches many popular quad operational amplifiers: OP11, TLC274, LTC1014, LM348, and ICL7642/41 are typical examples. In many applications, operating from dual 5V or single power supplies, the TC914 offers superior electrical performance, and can be a functional drop-in replacement; printed circuit board rework is not necessary. The TC914's low offset voltage error eliminates offset voltage trim potentiometers often needed with bipolar and low-accuracy CMOS operational amplifiers.

The TC914 takes full advantage of Teledyne's proprietary CMOS technology. Its 1.5 mA supply current (250 µA per amplifier) makes the TC914 the lowest power, precision quad operational amplifier available. The 250 µA amplifier supply current does not compromise AC performance. Unity-gain bandwidth is 1.5 MHz and slew rate is 2.5 V/µs.

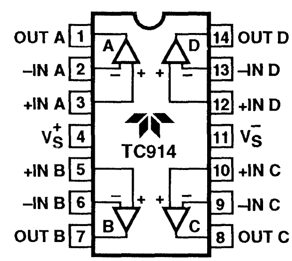
For single- and dual-operational amplifiers, see the TC911 and TC913 data sheets.

ORDERING INFORMATION

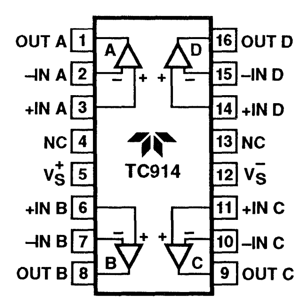
Part No.	Package	Temperature Range	Maximum Offset Voltage
TC914ACPD	14-Pin Plastic DIP	0°C to +70°C	15 µV
TC914BCPD	14-Pin Plastic DIP	0°C to +70°C	30 µV
TC914AIJD	14-Pin CerDIP	–25°C to +85°C	15 µV
TC914BIJD	14-Pin CerDIP	–25°C to +85°C	30 µV
TC914ACOE	16-Pin SO	0°C to +70°C	15 µV

PIN CONFIGURATIONS

14-Pin DIP



16-Pin SO



NC = NO INTERNAL CONNECTION

QUAD AUTO-ZEROED OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+_S to V^-_S) ....+18V
Input Voltage ....(V^+_S+0.3V) to (V^-_S –0.3V)
Current into Any Pin ....10 mA
While Operating ....100 µA
Storage Temperature Range..................–65°C to +150°C
Lead Temperature (Soldering, 10 sec) ....+300°C
Operating Temperature Range
C Device ....0°C to +70°C
I Device ....–25°C to +85°C

Package Power Dissipation (T_A = +25°C)
CerDIP ....500 mW
Plastic DIP and SO ....375 mW

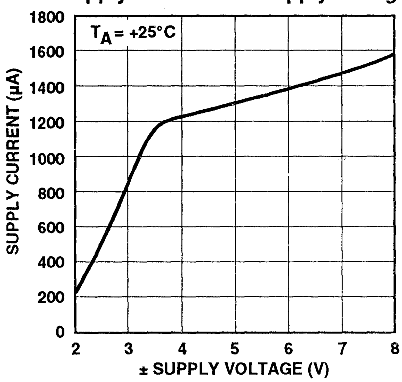
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = ±5V, T_A = +25°C, unless otherwise indicated.

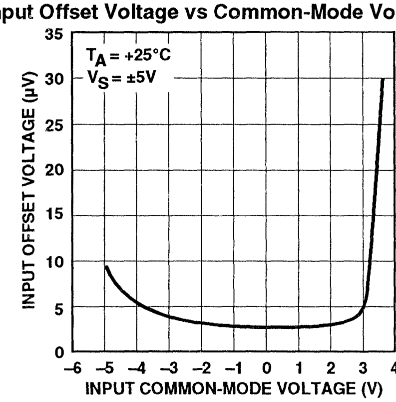
			TC913A			TC913B			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage	T_A = +25°C	—	5	15	—	15	30	µV
TCV_{OS}	Average Temperature Coefficient of Input Offset Voltage	0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C	— —	0.05 0.05	0.15 0.15	— —	— —	0.25 0.25	µV/°C µV/°C
I_B	Average Input Bias Current	T_A = +25°C 0°C ≤ T_A ≤ +70°C –25°C ≤ T_A ≤ +85°C	— — —	— — —	90 3 4	— — —	— — —	120 4 6	pA nA nA
I_{OS}	Average Input Offset Current	T_A = +25°C	—	5	20	—	10	40	pA
e_N	Input Voltage Noise	0.1 to 1 Hz, R_S ≤ 100Ω 0.1 to 10 Hz, R_S ≤ 100Ω	— —	0.6 11	— —	— —	0.6 11	— —	$µV_{P-P}$ $µV_{P-P}$
CMRR	Common-Mode Rejection Ratio	$V_S^- \le V_{CM} \le V_S^+ - 2.2V$	110	116	—	100	110	—	dB
CMVR	Common-Mode Voltage Range		V_S^-	—	$V_S^+ -2$	V_S^-	—	$V_S^+ -2$	V
A_{OL}	Open-Loop Voltage Gain	R_L = 10 kΩ, V_O = ±4V	115	120	—	110	120	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	$V_S^- +0.3$	—	$V_S^+ -0.9$	$V_S^- +0.3$	—	$V_S^+ -0.9$	V
BW	Closed-Loop Bandwidth	Closed Loop Gain = +1	—	1.5	—	—	1.5	—	MHz
SR	Slew Rate	R_L = 10 kΩ, C_L = 50 pF	—	2.5	—	—	2.5	—	V/µs
PSRR	Power Supply Rejection Ratio	±3.3V ≤ V_S ≤ ±5.5V	110	—	—	100	—	—	dB
V_S	Operating Supply Voltage Range	Split Supply Single Supply	±3 4.5	— —	±8 16	±3 4.5	— —	±8 16	V V
I_S	Quiescent Supply Current	V_S = ±5V	—	—	1.6	—	—	2.2	mA

TYPICAL CHARACTERISTICS CURVES

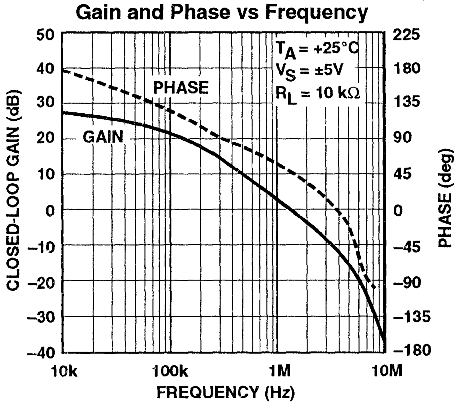
Supply Current vs ± Supply Voltage



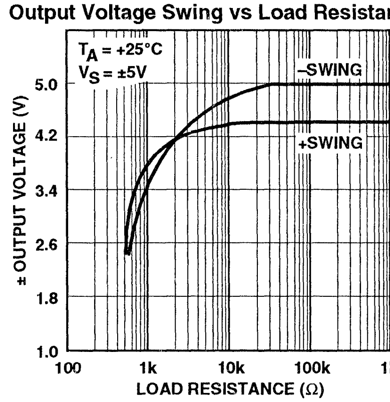
Input Offset Voltage vs Common-Mode Voltage



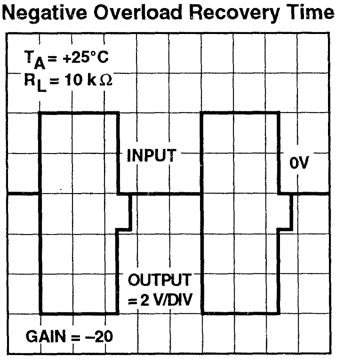
Gain and Phase vs Frequency



Output Voltage Swing vs Load Resistance

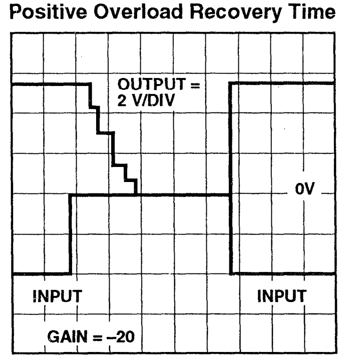


Negative Overload Recovery Time



HORIZONTAL SCALE = 20 ms/DIV

Positive Overload Recovery Time



HORIZONTAL SCALE = 20 ms/DIV

Theory of Operation

Each of the TC914's four op-amps actually consists of two amplifiers. A main amplifier is always connected from the input to the output. A separate nulling amplifier alternately nulls its own offset and then the offset of the main amplifier. Since each amplifier is continuously being nulled, offset voltage drift with time, temperature and power supply variations is greatly reduced.

All nulling circuitry is internal and the nulling operation is transparent to the user. Offset nulling voltages are stored on two internal capacitors. An internal oscillator and control logic, shared by the TC914's two amplifiers, control the nulling process.

Pin Compatibility

The TC914 pinout is compatible with OP11, LM324, LM348, LT1014, TLC274, and similar quad op-amps. In many circuits operating from single or ±5V supplies, the TC914 is a drop-in replacement, offering DC performance rivaling that of the best single op-amps.

The TC914's amplifiers include a low-impedance, class AB output buffer. Some previous CMOS chopper amplifiers used a high-impedance output stage which made open-loop gain dependent on load resistance. The TC914's open-loop gain is not dependent on load resistance.

Overload Recovery

The TC914 recovers quickly from output saturation. Typical recovery time from positive output saturation is 20 ms. Negative output saturation recovery time is typically 5 ms.

Avoiding Latch-Up

Junction-isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and power dissipation. The TC914's power supplies should be established at the same time or before input signals are applied. If this is not possible, input current should be limited to 0.1 mA to avoid triggering the p-n-p-n structure.

Static Protection

Input pins are protected against electrostatic fields. Static handling procedures should be used with all CMOS devices. Many companies provide services, educational material, and supplies to aid electronic equipment manufacturers to establish "static safe" CMOS component handling areas. A partial company list is:

- 3M
  Static Control Systems Div
  223-23W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (201) 561-9520

NOTES

TELEDYNE COMPONENTS

HIGH-VOLTAGE, AUTO-ZEROED OPERATIONAL AMPLIFIER

FEATURES

- High-Voltage Operation .... ±15V
- Low Offset Voltage .... 10 μV Max
- Low Offset Voltage Drift .... 0.2 μV/°C
- Low Input Bias Current .... 200 pA Max
- High Open-Loop Voltage Gain .... 140 dB
- Wide Common-Mode Voltage Range ....–15V to +13V
- Low Input Voltage Noise (0.1 Hz to 1 Hz) .... 0.2 μV_{P-P}
- Low Supply Current .... 1 mA
- Single Supply Operation .... 7V to 32V
- Pin Compatible With ICL7650
- Output Clamp Speeds Overload Recovery Time

GENERAL DESCRIPTION

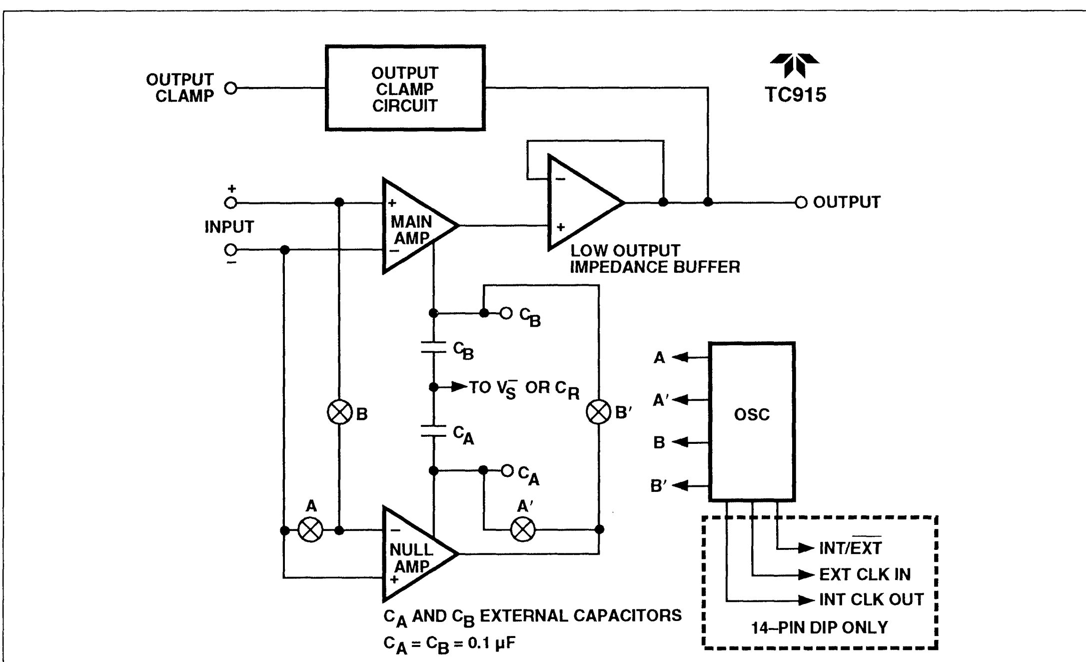
The TC915 is a high-voltage, high-performance CMOS, chopper-stabilized operational amplifier. It can operate from the same ±15V power supplies commonly used to power bipolar op amps, such as the OP07 and 741. Previous CMOS chopper-stabilized amplifiers, such as the TC7650, were limited to operating from ±7.5V power supplies.

The TC915's maximum V_{OS} specification is only 10 μV, almost a factor of 7 improvement over the industry-standard OP07E. The maximum V_{OS} drift of 0.1 μV/°C is 12 times less than the OP07E. Input bias and offset currents (both only 100 pA maximum) are factors of 20 improvements.

In addition to low initial offset errors, the nulling circuitry ensures excellent performance over time and temperature. Long-term drift, which results in periodic recalibration, is effectively eliminated. The nulling circuitry continues to operate over the full temperature range, whereas laser and "zener zap" trimming are only done at a single temperature. The result is a significant decrease in temperature-induced errors.

8

FUNCTIONAL DIAGRAM



HIGH-VOLTAGE, AUTO-ZEROED OPERATIONAL AMPLIFIER

TC915

The TC915 operates from dual- or single-power supplies. Supply current is typically 1 mA with ±15V supplies. Single supply operation extends from +7V to +32V, and the input common-mode range extends to V_S^-. For battery operation, see the low-power TC900 data sheet.

The TC915's open-loop gain is 120 dB minimum. Unlike the TC7650, the TC915's gain is independent of load resistance. The low-impedance output will drive a 10 kΩ load to ±14V. An output clamp circuit is provided to minimize overload recovery time.

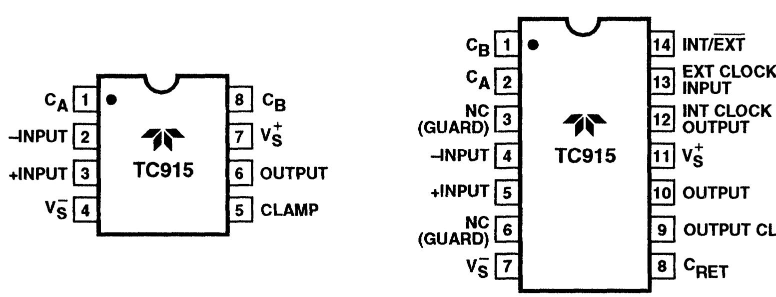
The TC915 uses two amplifiers to correct offset voltage errors. A main amplifier is always in the signal path, which prevents switching spikes at the output. A separate nulling amplifier alternately corrects its own V_{OS} error and then the main amplifier's V_{OS} error. Only two external capacitors are required to store the nulling error voltages. All active nulling circuitry, including switches and oscillators, are included on-chip.

TC915 does not require complicated processing and testing procedures associated with laser or "zener zap" V_{OS} trimming schemes. Simplified fabrication and high yields combine to make the TC915 one of the lowest-priced precision op amps available. It is available in 8-pin and 14-pin plastic or ceramic dual-in-line packages. Dice are available for hybrid applications.

ORDERING INFORMATION

Part No.	Package	Temperature Range	Max V_{OS}
TC915CPA	8-Pin Plastic DIP	0°C to +70°C	10 µV
TC915IJA	8-Pin CerDIP	–25°C to +85°C	10 µV
TC915MJA	8-Pin CerDIP	–55°C to +125°C	10 µV
TC915CPD	14-Pin Plastic DIP	0°C to +70°C	10 µV
TC915IJD	14-Pin CerDIP	–25°C to +85°C	10 µV
TC915MJD	14-Pin CerDIP	–55°C to +125°C	10 µV

PIN CONFIGURATION



NC = NO INTERNAL CONNECTION

HIGH-VOLTAGE, AUTO-ZEROED OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) .... +36V
Input Voltage .... (V_S^+ +0.3V) to (V_S^- −0.3V)
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Current Into Any Pin .... 10 mA
Operating Temperature Range
C Device .... 0°C to +70°C
I Device .... −25°C to +85°C
M Device .... −55°C to +125°C

Package Power Dissipation (T_A = +25°C)
CerDIP .... 500 mW
Plastic DIP .... 375 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = ±15V, T_A = +25°C, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{OS}	Input Offset Voltage		—	—	10	µV
TCV_{OS}	Input Offset Voltage vs Temperature Coefficient	0°C ≤ T_A ≤ +70°C	—	0.01	0.1	µV/°C
		−25°C ≤ T_A ≤ +85°C	—	—	0.3	µV/°C
I_B	Input Bias Current	T_A = +25°C	—	30	100	pA
		0°C ≤ T_A ≤ +70°C	—	—	—	pA
		−25°C ≤ T_A ≤ +85°C	—	—	10	pA
I_{OS}	Input Offset Current		—	50	100	pA
e_N	Input Voltage Noise	0.1 to 1 Hz, R_S ≤ 100Ω	—	0.2	—	$µV_{P-P}$
		0.1 to 10 Hz, R_S ≤ 100Ω	—	0.8	—	$µV_{P-P}$
CMRR	Common-Mode Rejection Ratio	V_S^- ≤ V_{CM} ≤ V_S^+−2	120	140	—	dB
CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+−2	V
A_{OL}	Open-Loop voltage Gain	R_L = 10 kΩ, V_O = ±10V	120	140	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^-+1	—	V_S^+−1.2	V
BW	Closed-Loop Bandwidth	Closed-Loop Gain = +1	—	0.5	—	MHz
	Slew Rate	R_L = 10 kΩ, C_L = 50 pF	—	0.5	—	V/µs
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	120	140	—	dB
V_S	Supply Voltage Operating Range	(Note 1)	±3.5	—	±16	V
I_S	Quiescent Supply	V_S = ±15V	—	1	1.5	mA

NOTE: 1. Single supply operation: V_S^+ = +7V to +32V.

Theory of Operation

Figure 1 shows the major elements of the TC915. There are two amplifiers: a main (signal) amplifier and a nulling amplifier. Both have offset-nulling capability. The main amplifier is always connected to the output. The nulling amplifier alternately samples and adjusts its own offset, then the offset of the main amplifier.

A two-phase operation nulls the main amplifier. During the first phase, the A pair of switches close, while the B switches open. The nulling amp's inputs are shorted and its output is fed back to the nulling input. Capacitor C_A charges to a voltage which will maintain the nulling amp in its nulled state.

During the second phase, the B switches close and the A switches open. The nulling amplifier's inputs now sample the offset voltage of the main amplifier. The nulling amplifier drives the main amplifier's nulling input to cancel the main amplifier's offset voltage. Capacitor C_B stores the nulling voltage of the main amplifier while the nulling amplifier is being nulled on the next cycle.

The TC915 design also incorporates an additional output buffer stage. The buffer provides a low-impedance output traditionally associated with bipolar op amps. Some CMOS chopper-stabilized amplifiers, such as the TC7650, have a high-output impedance which makes open-loop gain proportional to load resistance. The TC915's open-loop gain is not dependent on load resistance.

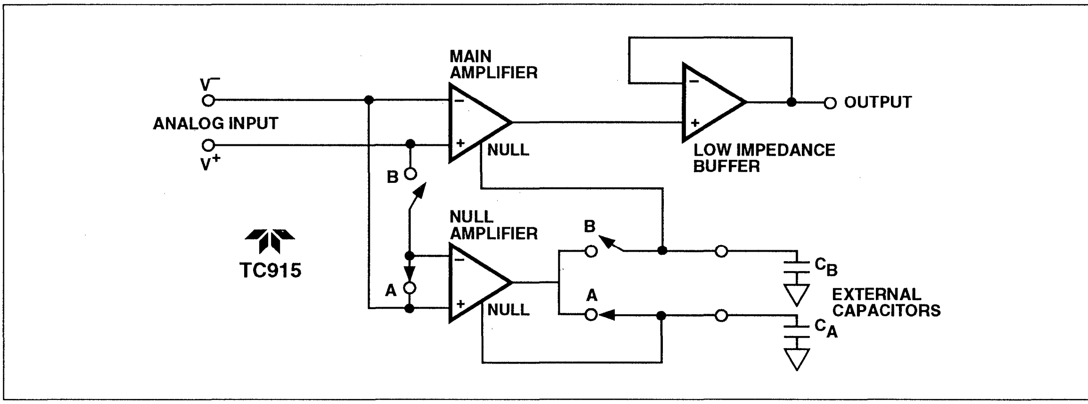


Figure 1 The TC915 Contains Nulling and Main Amplifiesr (Offset Correction Voltages Are Stored on Two External Capacitors)

Pin Compatibility

Since the TC915 operates from the same ±15V power supplies as bipolar op amps, upgrading existing circuits is simple. The bipolar op amp's nulling and compensation components are removed and the TC915's nulling capacitors are added.

On the 8-pin mini-DIP, the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, replacing the offset null potentiometer between pins 1 and 8 with two capacitors from the pins to V_S^- converts the OP05/07 pin configuration for TC915 operation. The 741 is easily upgraded by removing the nulling potentiometer between pin 4 and pins 1 and 5, then connecting capacitors from pin 4 to pins 1 and 8. For LM108 devices, the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pinouts are similarly modified by removing any circuit connections to pin 5. Pin 5 on the TC915 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

The minor modifications needed to retrofit a TC915 to existing sockets make prototyping and circuit verification straightforward.

Nulling Capacitors

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (pin 4) on the 8-pin packages and to capacitor return (C_{RET}, pin 8) on the 14-pin packages. The common connection should be made through a separate PC trace or wire, to avoid voltage drops. Internally, V_S^- is connected to C_{RET}.

C_A and C_B should be 0.1 µF film capacitors. Mylar capacitors are suitable.

Component Selection

The two required capacitors, C_A and C_B, have optimum values, depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 µF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock, if used. High-quality, film-type capacitors (such as Mylar) are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling at initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 µV.

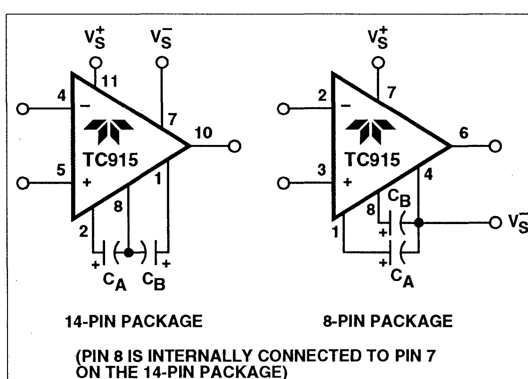


Figure 2 Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 1000 Hz nominal frequency on both the 8-pin and 14-pin DIPs. With the 14-pin device, the 250 Hz internal frequency is available at the INTERNAL CLOCK OUTPUT (pin 12). A 1000 Hz nominal signal will be present at the EXTERNAL CLOCK INPUT (pin 13) with INT/EXT high or open. This is the internal clock signal before a divide-by-four operation.

The 14-pin device can be driven by an external clock. The INT/EXT input (pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/EXT must be tied to V_S^- (pin 7) to disable the internal clock. The external clock signal is applied to the external clock input.

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6V, and between V_S^+ and V_S^+ –6V for higher supply voltages. When the external clock is generated by +5V logic, capacitive coupling to pin 13 (through a 0.1 µF capacitor) will provide adequate drive.

At low frequencies the external clock duty cycle is not critical, since an internal divide-by-four gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50% to 80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a stobe signal is connected at the external clock input, so that it is low during the time an overload signal is applied, neither capacitor will be charged. This function can be used to prevent input transients from overloading the nulling circuitry. Leakage currents at the capacitor pins are very low, minimizing offset voltage drift during strobe operation.

Output Clamp

Chopper-stabilized systems can show long overload recovery times. If the output is driven to either supply rail, output saturation occurs; the inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through the external-clamp connection, the TC915 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3, with typical inverting and noninverting circuit connections shown in Figures 4 and 5. For the clamp to be fully effective, the impedance across the clamp output should be >100 kΩ.

When the clamp is used, the clamp OFF leakage will add to input bias current. However, clamp leakage in the OFF state is typically only 1 pA.

Input Bias Current

The TC915 inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. However, the sampling causes charge transfer at the inputs.

The impulse current is not usually a problem, because the amount of charge transferred is very small. Care should be exercised, however, when replacing high-input bias current bipolar op amps. Conventional design practice is to cancel bias current by matching the input impedances (Figure 6a). The TC915 has an input bias current of only

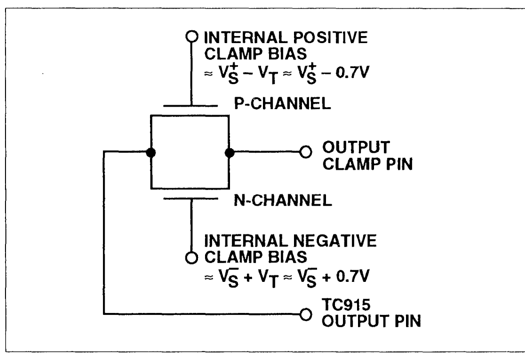


Figure 3 Internal Clamp Circuit

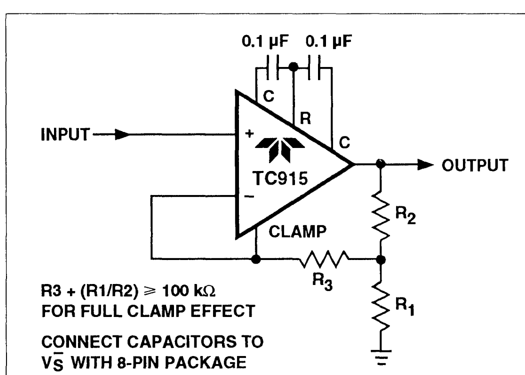


Figure 4 Noninverting Amplifier With Optional Clamp

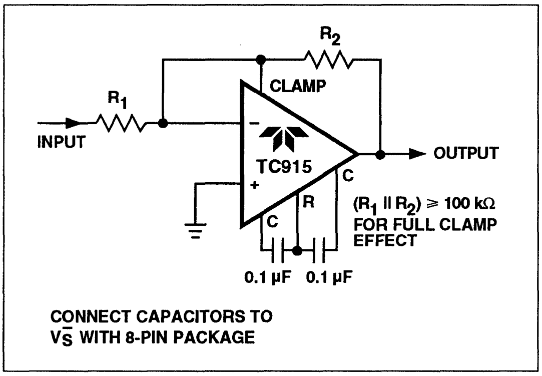


Figure 5 Inverting Amplifier With Optional Clamp

100 pA maximum, so the additional resistor is not necessary. In fact, including the resistor will make the charge injection current, passing through the impedance balancing resistor, appear as a noise source. When replacing an existing op amp with the TC915, either omit the resistor or bypass it to ground with a capacitor (Figure 6b).

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances, this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, voltages greater than 0.3V beyond the supply rails should not be applied to any pin. In general, the amplifier supplies must be established at the same time, or before, any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latch-up.

Static Protection

All device pins are static-protected. However, strong static fields and discharges should be avoided as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational materials, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. Two such companies are:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520

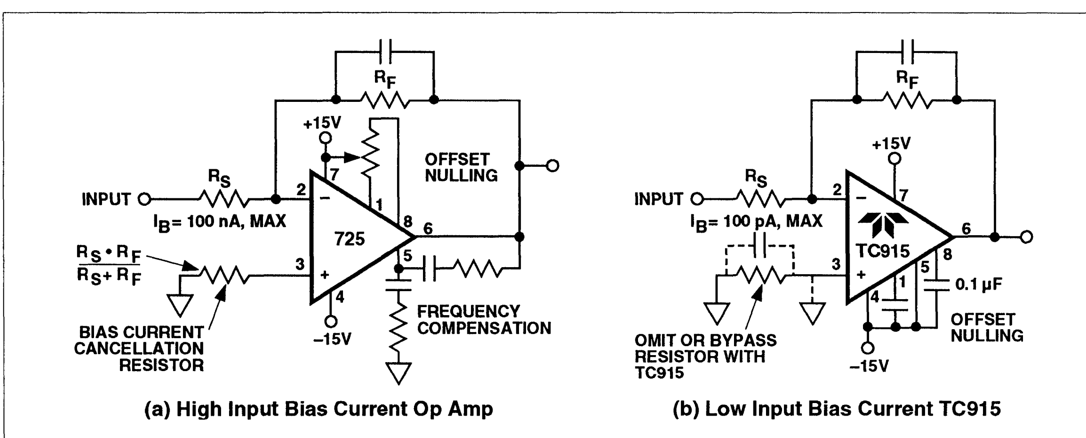
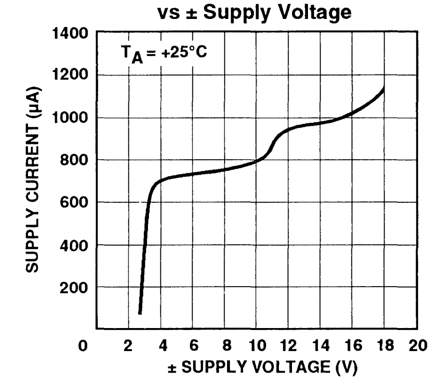


Figure 6 Input Bias Current Cancellation

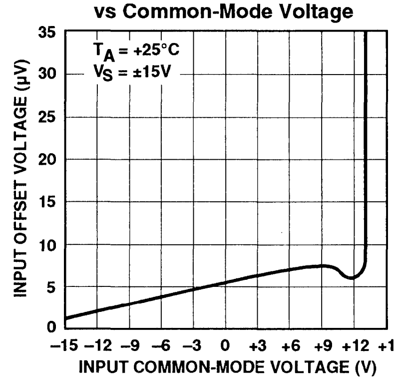
HIGH-VOLTAGE, AUTO-ZEROED OPERATIONAL AMPLIFIER

TYPICAL CHARACTERISTICS CURVES

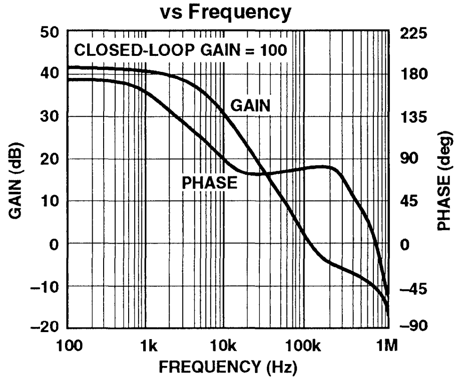
Supply Current vs ± Supply Voltage



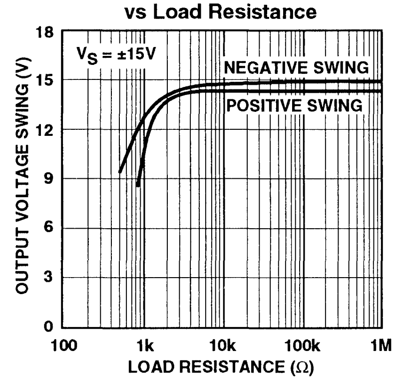
Input Offset Voltage vs Common-Mode Voltage



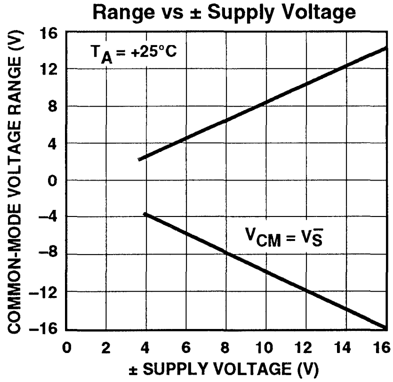
Gain and Phase vs Frequency



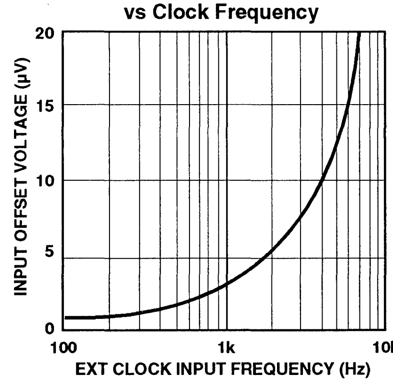
Output Voltage Swing vs Load Resistance



Input Common-Mode Voltage Range vs ± Supply Voltage



Input Offset Voltage vs Clock Frequency



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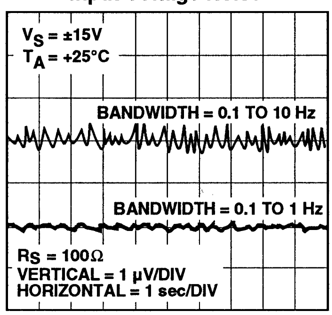
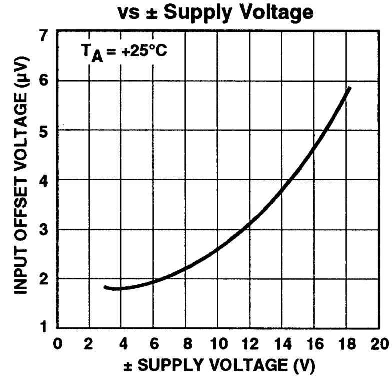
TYPICAL CHARACTERISTICS CURVES (Cont.)

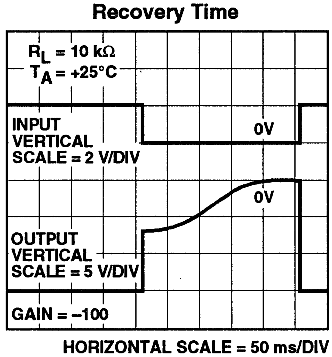
Input Voltage Noise



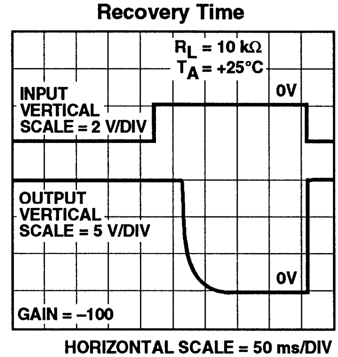
Input Offset Voltage vs ± Supply Voltage



Negative Overload Recovery Time



Positive Overload Recovery Time



TELEDYNE COMPONENTS

LOW-COST CMOS OPERATIONAL AMPLIFIER

FEATURES

- **Low Power Supply Current .... 800 µA Max**
- **Low Input Offset Voltage .... 50 µV Max**
- **Low Input Offset Voltage Drift .... 0.8 µV/°C Max**
- **High-Impedance Differential CMOS Inputs .... $10^{12}\Omega$**
- **High Open-Loop Voltage Gain .... 100 dB Min**
- **Low Input Noise Voltage .... 0.3 μV_{P-P}**
- **Compensated Internally for Stable Unity-Gain Operation**
- **High Common-Mode Rejection .... 98 dB Min**
- **Small Outline (SO) Packages Available**

GENERAL DESCRIPTION

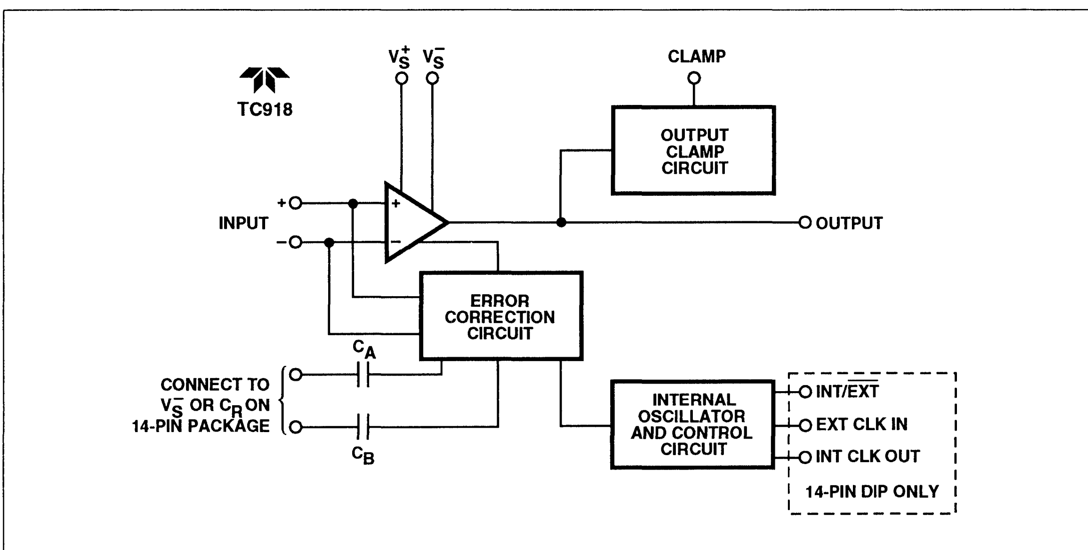
The TC918 is a general-purpose, low-cost CMOS operational amplifier. By periodically sampling input offset voltage and storing compensating voltages in external capacitors, low offset voltage errors are possible. The correction circuits compensate offset voltage drift with temperature and time. Offset voltage temperature coefficient is 0.8 µV/°C maximum; V_{OS} is 50 µV maximum.

The TC918 performance advantages are achieved without the manufacturing complexity and costs incurred with laser or "zener zap" V_{OS} trim techniques. The TC918 offers a 0.2 V/µs slew rate and a 700 kHz unity-gain bandwidth. Open-loop voltage gain is 100 dB.

Operating from ±5V supplies, the TC918's power dissipation is under 10 mW. In +5V-only systems, the TC7660 DC-to-DC converter can supply the TC918's negative supply potential. The TC918 will also operate from a single +5V supply.

For lower power dissipation and offset voltage errors, see the TC900 and TC7650/TC7650A specifications.

FUNCTIONAL DIAGRAM

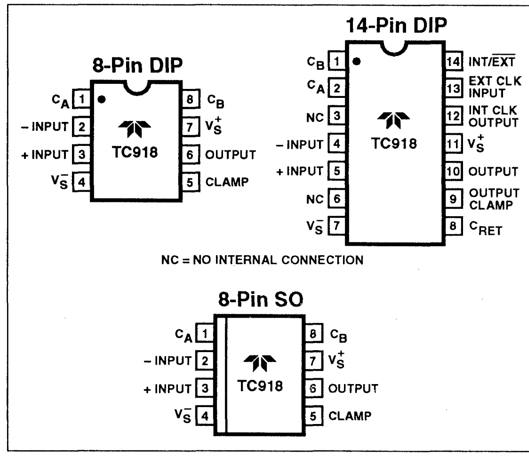


TC918

ORDERING INFORMATION

Part No.	Package	Temperature Range	Max V_{OS}
TC918CPA	8-Pin Plastic DIP	0°C to +70°C	50 µV
TC918COA	8-Pin SO	0°C to +70°C	50 µV
TC918IJA	8-Pin CerDIP	–25°C to +85°C	50 µV
TC918CPD	14-Pin Plastic DIP	0°C to +70°C	50 µV
TC918IJD	14-Pin CerDIP	–25°C to +85°C	50 µV

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) .... +18V
Input Voltage .... (V_S^+ +0.3V) to (V_S^- –0.3V)
Voltage on Oscillator Control Pins .... V_S^+ to V_S^-
Output Short Circuit Duration .... Indefinite
Current Into Any Pin .... 10 mA
While Operating (Note 4) .... 100 µA
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C
Operating Temperature Range
C Device .... 0°C to +70°C
I Device .... –25°C to +85°C

Package Power Dissipation (T_A = +25°C)
Plastic and CerDIP .... 500 mW

Static-sensitive device. Unused devices must be stored in conductive material to protect them from possible static damage. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_S^+ = +5V$, $V_S^- = –5V$, $C_A = C_B = 0.1$ µF, $T_A = +25°C$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{OS}	Input Offset Voltage	T_A = +25°C	—	—	50	µV
TCV_{OS}	Input Offset Voltage vs Average Temperature Coefficient	Operating Temperature Range (Note 1)	—	0.4	0.8	µV/°C
I_{BIAS}	Average Input Bias Current (Note 5)	T_A = +25°C	—	—	100	pA
I_{OS}	Input Offset Current	T_A = +25°C	—	0.5	—	pA
e_N	Input Noise Voltage	R_S = 100Ω, 0 to 10 Hz	—	4	—	$µV_{P-P}$
		R_S = 100Ω, 0 to 1 Hz	—	0.3	—	$µV_{P-P}$
R_{IN}	Input Resistance		—	10^{12}	—	Ω
CMVR	Common-Mode Voltage Range		V_S^-		V_S^+ –2	V
CMRR	Common-Mode Rejection Ratio	CMVR = –5V to +2V	98	115	—	dB

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Output						
A_V	Large-Signal Voltage Gain	$R_L = 10\ k\Omega$	100	130	—	dB
V_{OUT}	Output Voltage Swing (Note 3)	$R_L = 25\ k\Omega$ $R_L = 100\ k\Omega$	−4.7 −4.9	— —	+3.5 +3.9	V V
	Clamp ON Current (Note 2)	$R_L = 100\ k\Omega$	20	90	200	µA
	Clamp OFF Current (Note 2)	$-4V < V_{OUT} < +4V$	—	1	—	pA
Dynamic						
BW	Unity-Gain Bandwidth	Unity Gain (+1)	—	0.7	—	MHz
SR	Slew Rate	$C_L = 50\ pF$, $R_L = 10\ k\Omega$	—	0.2	—	V/µs
Supply						
V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	V
I_S	Supply Current	No Load	—	300	800	µA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 8V$	105	—	—	dB

NOTES: 1. Operating temperature range is −25°C to +85°C for "I" devices and 0°C to +70°C for "C" devices.
2. See "Output Clamp" discussion.
3. Output clamp not connected.
4. Limiting input current to 100 µA is recommended to avoid latch-up problems.
5. Average current caused by switch charge transfer at input.

Op-Amp Performance Comparison

The TC918 is a low-cost, low-power, precision amplifier. A comparison between the TC918 and other amplifiers is shown in Figure 1.

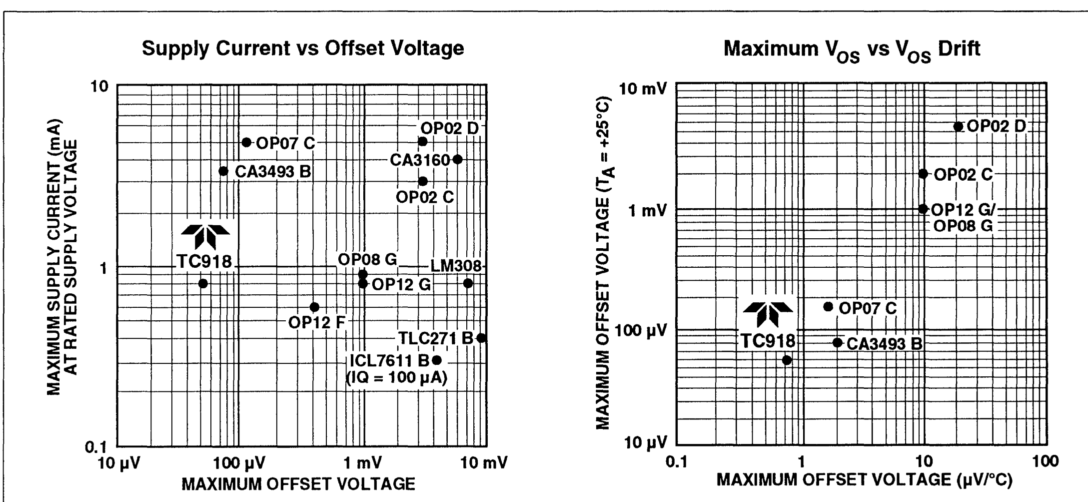


Figure 1. TC918 Comparison to Other Amplifiers

Nulling Capacitors

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (pin 4 on 8-pin devices) and to capacitor return C_{RET} (pin 8 on 14-pin devices). The common connection should be made through a separate PC trace or wire to avoid voltage drops.

Internally, V_S^- is connected to C_{RET}.

C_A and C_B should be 0.1 µF film capacitors. Mylar capacitors are suitable.

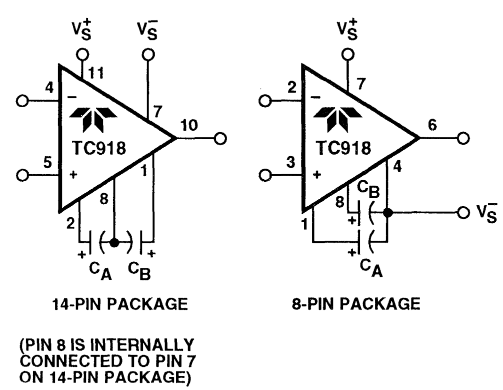


Figure 2. Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 150 Hz nominal frequency. With the 14-pin device, the 150 Hz internal frequency is available at the internal clock output (pin 12). A 300 Hz nominal signal will be present at the external clock input (pin 13), with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before a divide-by-two operation.

The 14-pin device can be driven by an external clock. The INT/$\overline{\text{EXT}}$ input (pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/$\overline{\text{EXT}}$ must be tied to V_S^- (pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6V and between V_S^+ and V_S^+ –6V for higher supply voltages.

At low frequencies, the external clock duty cycle is not critical, since an internal divide-by-two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50% to 80% external clock-positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input, so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low.

Output Clamp

If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the internal correction circuit and external capacitors.

Through an external clamp connection, the TC918 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

Normally, the clamp pin is not connected.

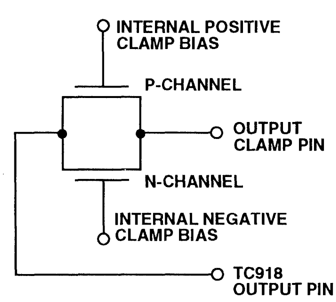


Figure 3. Internal Clamp Circuit

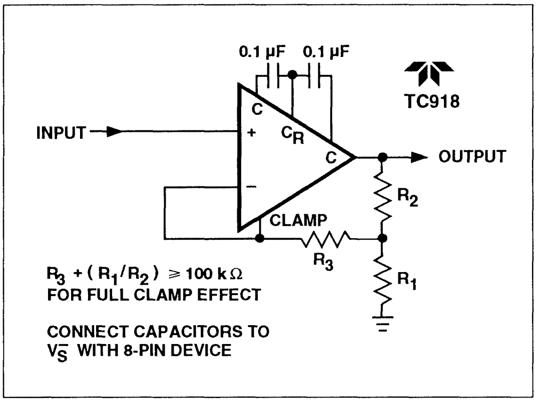


Figure 4. Noninverting Amplifier With Optional Clamp

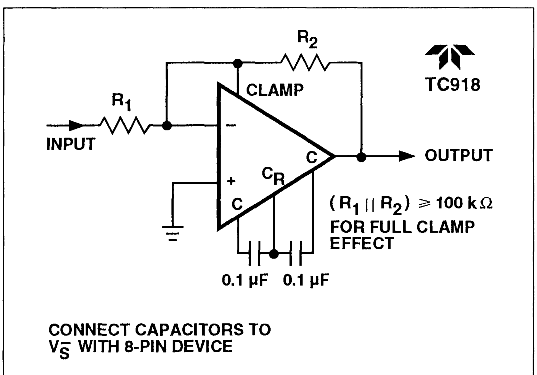


Figure 5. Inverting Amplifier With Optional Clamp

Input Bias Current

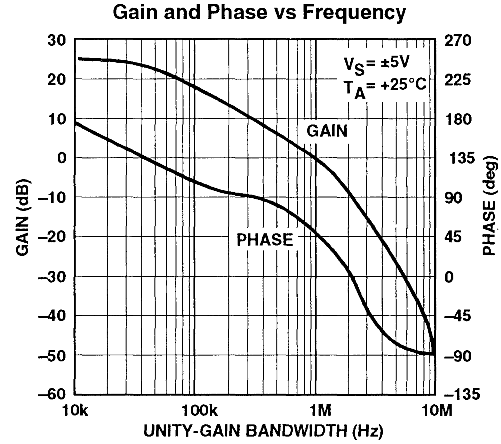
The TC918's inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling, however, causes charge transfer at the inputs. The charge transfer represents a peak impulse current of 200 nA to 290 nA at the inputs when the internal clock makes a transition.

Latch-Up Avoidance

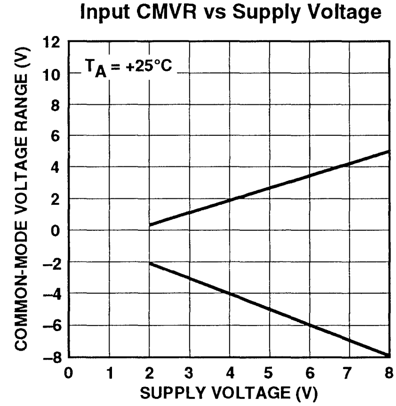
Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances, this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, voltages greater than 0.3V beyond the supply rails should not be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latch-up.

TYPICAL CHARACTERISTIC CURVES

Gain and Phase vs Frequency



Input CMVR vs Supply Voltage



NOTES

CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

FEATURES

- Low Input Offset Voltage .... 0.7 μV
- Low Input Offset Voltage Drift .... 0.05 μV/°C Max
- Low Input Bias Current .... 10 pA Max
- High Impedance Differential CMOS Inputs .... $10^{12}\Omega$
- High Open-Loop Voltage Gain .... 120 dB Min
- Low Input Noise Voltage .... 2.0 μ Vp-p
- High Slew Rate .... 2.5 V/μs
- Low-Power Operation .... 20 mW
- Output Clamp Speeds Recovery Time
- Compensated Internally for Stable Unity Gain Operation
- Direct Replacement for ICL7650
- Available in 8-Pin Dip

GENERAL DESCRIPTION

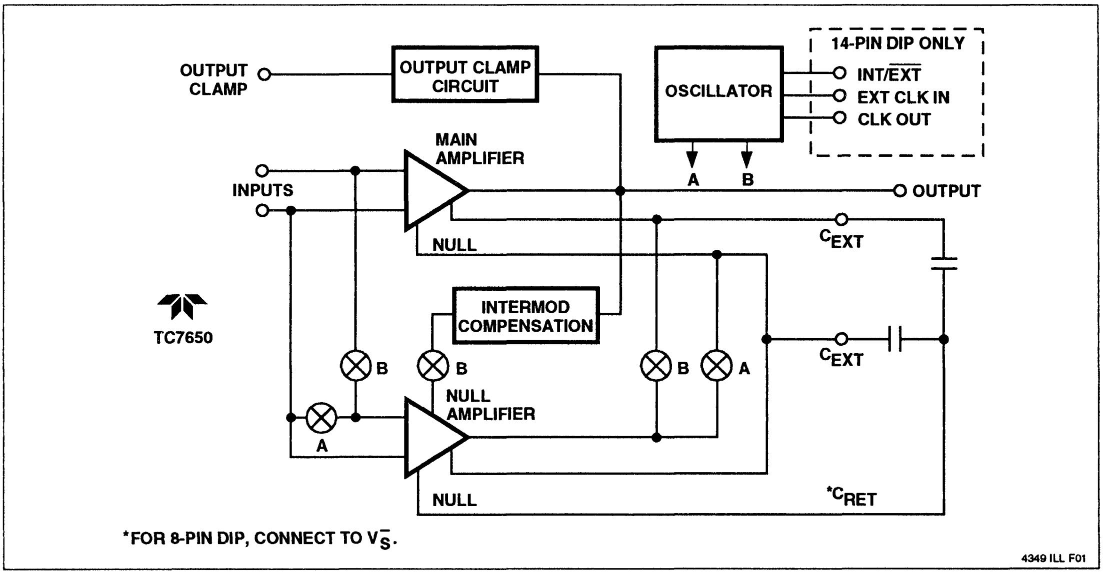
The TC7650 CMOS chopper-stabilized operational amplifier practically removes offset voltage error terms from system error calculations. The 5 μV maximum V_{OS} specification, for example, represents a 15 times improvement over the industry-standard OP07E. The 50 nV/°C offset drift specification is over 25 times lower than the OP07E. The increased performance eliminates V_{OS} trim procedures, periodic potentiometer adjustment and the reliability problems caused by damaged trimmers.

The TC7650 performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TC7650 is one of the lowest cost precision-operational amplifiers available.

The TC7650 nulling scheme corrects both DC V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user-supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the TC7650 output. The null scheme keeps V_{OS} errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for V_{OS} at only one temperature.

8

FUNCTIONAL DIAGRAM



TC7650

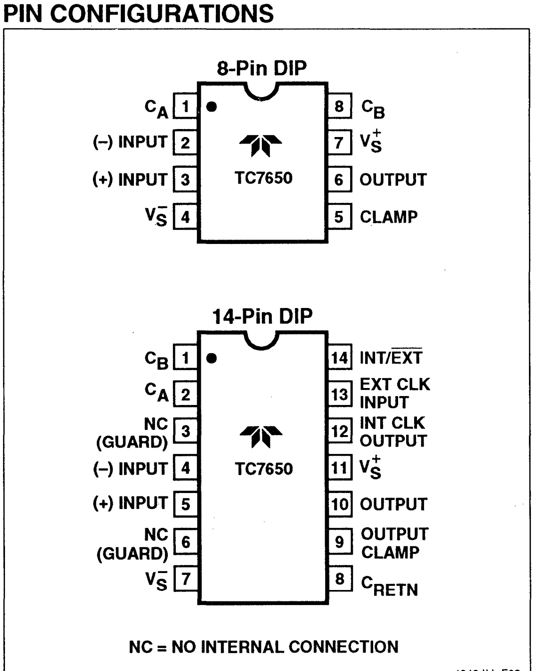
The nulling circuit oscillator and control circuits are integrated on-chip. Only two external V_{OS} error storage capacitors are required. The TC7650 operates as a conventional operational amplifier with improved input specifications. The low V_{OS} and V_{OS} drift errors make the TC7650 ideal for thermocouple, thermistor, and strain-gauge applications. Low DC errors and high open-loop gain make the TC7650 an excellent preamplifier for precision analog-to-digital converters, such as the TC7135 and TC800.

The 14-pin dual-in-line package (DIP) has an external oscillator input to drive the nulling circuitry for optimum noise performance. Both the 8- and 14-pin DIPs have an output voltage clamp circuit to minimize overload recovery time.

ORDERING INFORMATION

Part No.	Package	Temperature Range	Max V_{OS}
TC7650CPA	8-Pin Plastic DIP	0°C to +70°C	5 µV
TC7650IJA	8-Pin CerDIP	–25°C to +85°C	5 µV
TC7650CPD	14-Pin Plastic DIP	0°C to +70°C	5 µV
TC7650IJD	14-Pin CerDIP	–25°C to +85°C	5 µV

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) 18V
Input Voltage .... (V_S^++0.3V) to (V_S^-–0.3V)
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... 300°C
Voltage on Oscillator Control Pins .... V_S^+ to V_S^-
Output Short Circuit Duration .... Indefinite
Current Into Any Pin .... 10 mA
  While Operating (Note 4) .... 100 µA
Operating Temperature Range
  I Device .... –25°C to +85°C
  C Device .... 0°C to +70°C
Package Power Dissipation (T_A = 25°C)
  CerDIP .... 500 mW
  Plastic DIP .... 375 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_S^+ = +5V$, $V_S^- = -5V$, $C_A = C_B = 0.1\ \mu F$, $T_A = 25°C$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Input						
V_{OS}	Input Offset Voltage	$T_A = +25°C$ Over Operating Temp Range (Note 1)	— —	±0.7 ± 1.0	±5 —	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Temperature Coefficient	Operating Temperature Range (Note 1)	—	0.01	0.05	µV/°C
	Offset Voltage vs. Time		—	100	—	nV/ month
I_{BIAS}	Input Bias Current	$T_A = +25°C$ $0°C \le T_A \le +70°C$ $-25°C \le T_A \le +85°C$	— — —	1.5 35 100	10 150 400	pA pA pA
I_{OS}	Input Offset Current	$T_A = +25°C$	—	0.5	—	pA
e_{NP-P}	Input Noise Voltage	$R_S = 100\Omega$, 0 to 10 Hz	—	2	—	μV_{P-P}
I_N	Input Noise Current	f = 10 Hz	—	0.01	—	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance		—	10^{12}		Ω
CMVR	Common-Mode Voltage Range		–5	–5.2 to +2	+1.6	V
CMRR	Common-Mode Rejection Ratio	CMVR = –5V to +1.5V	120	130	—	dB
Output						
A	Large Signal Voltage Gain	$R_L = 10\ k\Omega$	120	130	—	dB
V_{OUT}	Output Voltage Swing (Note 3)	$R_L = 10\ k\Omega$ $R_L = 100\ k\Omega$	±4.7 —	±4.85 ±4.95	— —	V V
	Clamp ON Current (Note 2)	$R_L = 100\ k\Omega$	25	70	200	µA
	Clamp OFF Current (Note 2)	$-4V < V_{OUT} < +4V$	—	1	—	pA
Dynamic						
B_W	Unity-Gain Bandwidth	Unity Gain (+1)	—	2.0	—	MHz
S_R	Slew Rate	$C_L = 50\ pF$, $R_L = 10\ k\Omega$	—	2.5	—	V/µs
t_R	Rise Time		—	0.2	—	µs
	Overshoot		—	20	—	%
f_{CH}	Internal Chopping Frequency	Pins 12–14 Open (DIP)	120	200	375	Hz
Supply						
V_S^+, V_S^-	Operating Supply Range		4.5	—	16	V
I_S	Supply Current	No Load	—	2	3.5	mA
PSRR	Power Supply Rejection Ratio	$V_S = \pm3V$ to $\pm8V$	120	130		dB

NOTES: 1. Operating temperature range is –25°C to +85°C for "I" grade and 0°C to +70°C for "C" grade.
2. See "Output Clamp" discussion.
3. Output clamp not connected. See typical characteristics curves for output swing versus clamp current characteristics.
4. Limiting input current to 100 µA is recommended to avoid latch-up problems.

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Theory of Operation

Figure 1 shows the major elements of the TC7650. There are two amplifiers (the main amplifier and the nulling amplifier), and both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. Two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches minimizes chopper frequency charge injection at the input terminals, and the feed-forward-type injection into the compensation capacitor that can cause output spikes in this type circuit.

The circuit's offset voltage compensation is easily shown. With the nulling inputs shorted, a voltage almost identical to the nulling amplifier offset voltage is stored on C_A. The effective offset voltage at the null amplifier input is:

$$V_{OSE} = \frac{1}{A_N + 1} V_{OSN} \qquad (1)$$

After the nulling amplifier is zeroed, the main amplifier is zeroed; the A switches open and B switches close.

The output voltage equation is:

$$V_O = A_M [V_{OSM} + (V^+ - V^-) + A_N(V^+ - V^-) + A_N V_{OSE}] \qquad (2)$$

Substituting (1) $\rightarrow$ (2) and assuming $A_N >> 1$:

$$V_O = A_M A_N \left[(V^+ - V^-) + \frac{V_{OSM} + V_{OSN}}{A_N} \right] \qquad (3)$$

As desired, the device offset voltages are reduced by the high open-loop gain of the nulling amplifier.

Output Stage/Load Driving

The output circuit is a high-impedance stage (approximately 18 kΩ). With loads less than this, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for DC, the lower gain is of little consequence, since the DC gain is typically greater than 120 dB, even with a 1 kΩ load. In wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This results in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region, where the main amplifier takes over from the null amplifier. The clock frequency sets the transition region.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier results in a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies, and causing disturbances to the gain and phase versus frequency characteristics near the chopping frequency. These effects are substantially reduced in the TC7650 by feeding the nulling circuit with a dynamic current corresponding to the compensation capacitor current in such a way as to cancel that portion of the input signal due to a finite AC gain. The intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

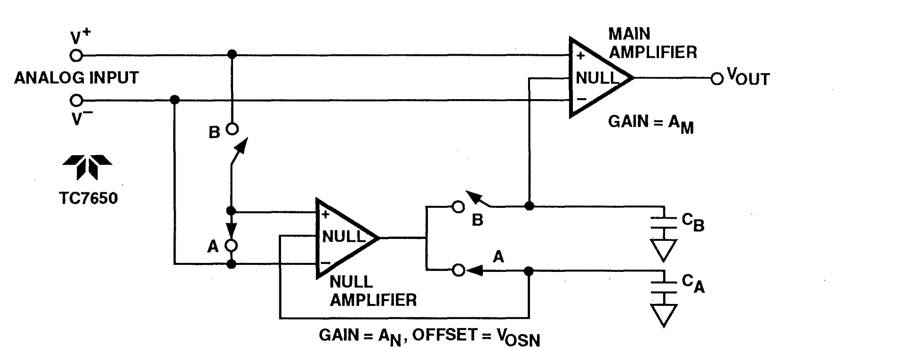

Figure 1 TC7650 Contains a Nulling and Main Amplifier. Offset Correction Voltages Are Stored on Two External Capacitors.

CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

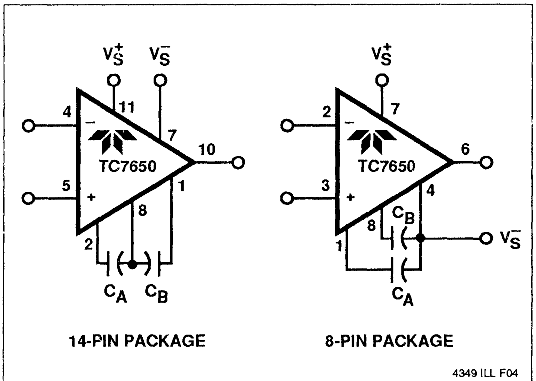

Figure 2 Nulling Capacitor Connection

Nulling Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (pin 4) on the 8-pin packages and to capacitor return (C_R, pin 8) on the 14-pin packages. The common connection should be made through either a separate PC trace or wire, to avoid voltage drops. The capacitors outside foil, if possible, should be connected to C_R or V_S^-.

Clock Operation

The internal oscillator is set for a 200 Hz nominal chopping frequency on both the 8- and 14-pin DIPs. With the 14-pin DIP TC7650, the 200 Hz internal chopping frequency is available at the internal clock output (pin 12). A 400 Hz nominal signal will be present at the external clock input pin (pin 13) with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before a divide-by-two operation.

The 14-pin DIP device can be driven by an external clock. The INT/$\overline{\text{EXT}}$ input (pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/$\overline{\text{EXT}}$ must be tied to V_S^- (pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6V and between V^+ and V^+ −6V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical, since an internal divide-by-two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50% to 80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitors pins are very low. At 25°C a typical TC7650 will drift less than 10 µV/sec.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TC7650 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

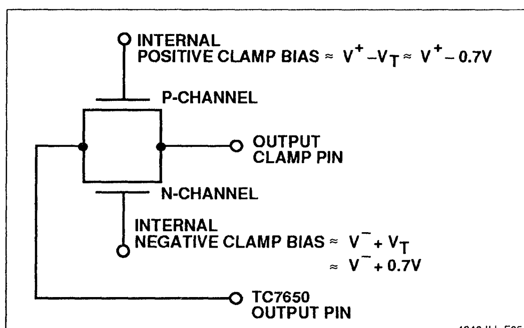

Figure 3 Internal Clamp Circuit

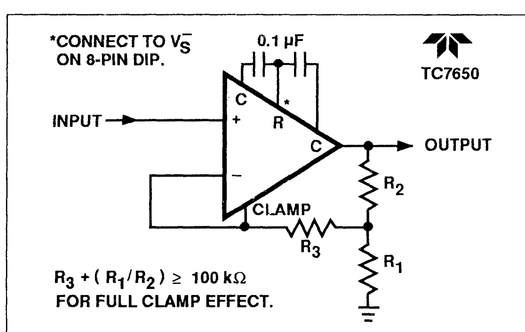

Figure 4 Noninverting Amplifier With Optional Clamp

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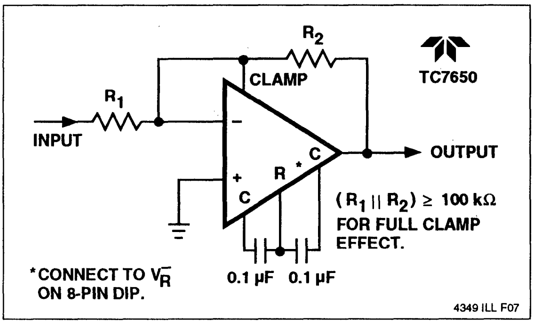


Figure 5 Inverting Amplifier With Optional Clamp

The output clamp circuit is shown in Figure 3, with typical inverting and noninverting circuit connections shown in Figures 4 and 5. Output voltage versus clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520
- American Converters
  1919 South Butlerfield Road
  Mundelein, IL 60060
  (312) 362-9000
- ACL
  1960 East Devon Avenue
  Elk Grove Village, IL 60007
  (312) 981-9212

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latch-up.

Thermoelectric Potentials

Precision DC measurements are ultimately limited by thermoelectric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages, typically around 0.1 μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the benefits extremely-low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially those caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and separation from surrounding heat-dissipating elements is advised.

Pin Compatibility

On the 8-pin mini-DIP TC7650, the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, the replacement of the offset null potentiometer between pins 1 and 8 by two capacitors from the pins to V_S^- will convert the OP05/07 pin configurations for TC7650 operation. For LM108 devices, the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pinouts are modified similarly by removing any circuit connections to pin 5. On the TC7650, pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offst or compensation point.

The minor modifications needed to retrofit a TC7650 into existing sockets operating at reduced power supply voltages make prototyping and circuit verification straightforward.

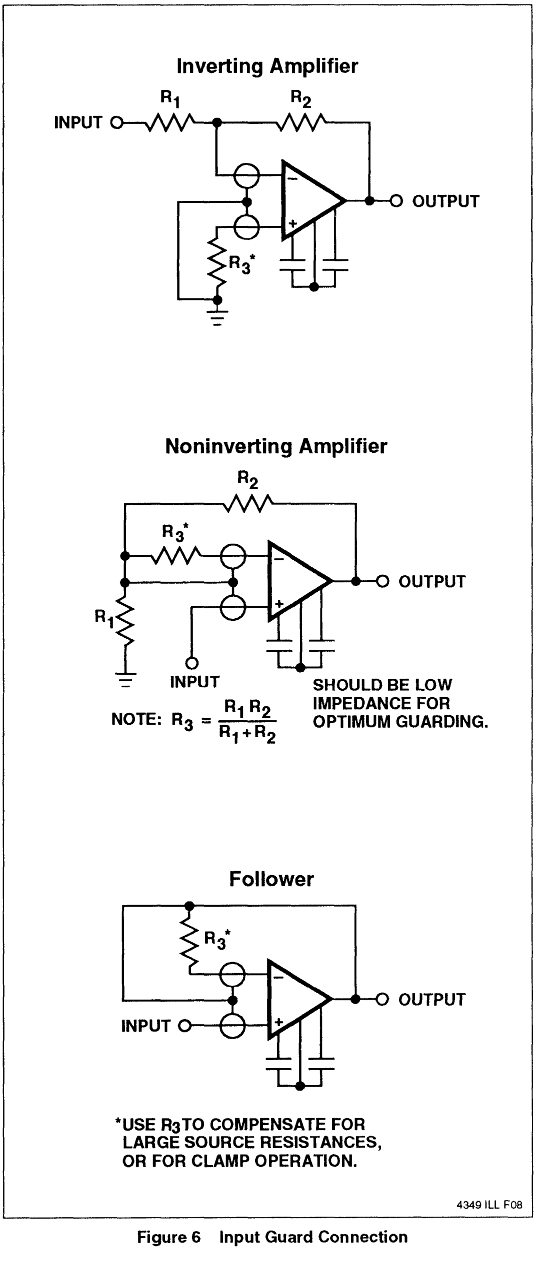


Figure 6 Input Guard Connection

Input Guarding

High impedance, low leakage CMOS inputs allow the TC7650 to make measurements of high-impedance sources. Stray leakage paths can increase input currents and decrease input resistance unless inputs are guarded. A guard is a conductive PC trace surrounding the input terminals. The ring connects to a low-impedance point at the same potential as the inputs. Stray leakages are absorbed by the low-impedance ring. The equal potential between ring and inputs prevents input leakage currents. Typical guard connections are shown in Figure 6.

The 14-pin DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are unused.

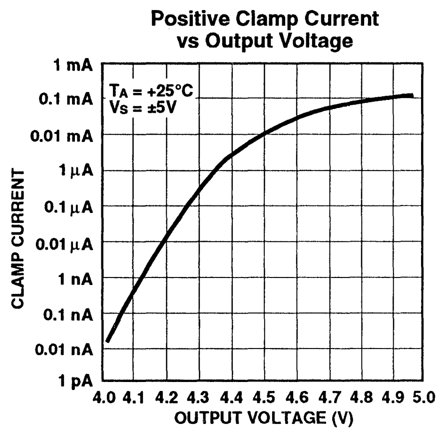
In applications requiring low leakage currents, boards should be cleaned thoroughly and blown dry after soldering. Protective coatings will prevent future board contamination.

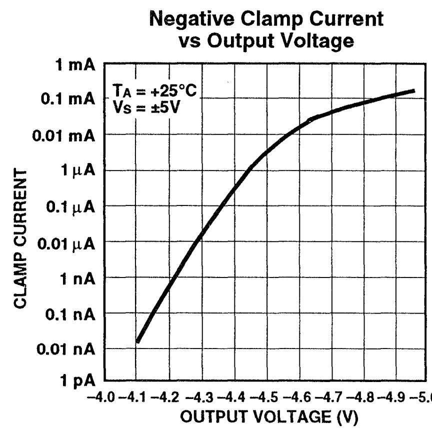
8

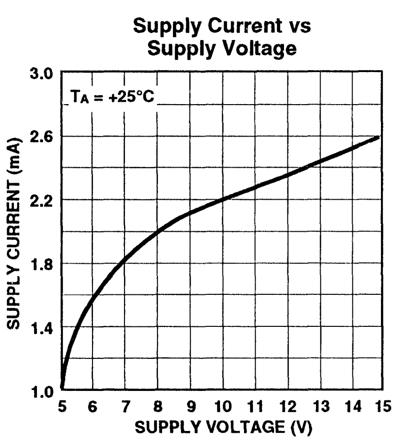
Component Selection

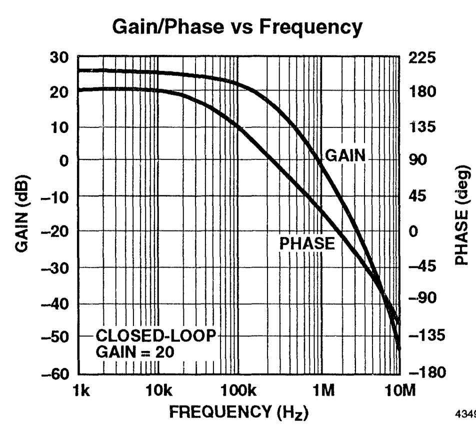
The two required capacitors, C_A and C_B, have optimum values, depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 µF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock, if used. High-quality film-type capacitors (such as Mylar) are preferred; ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 µV.

TYPICAL CHARACTERISTIC CURVES









4349 ILL F10

LOW NOISE, CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

FEATURES

- Low Offset Over Temperature Range .... 10 μV
- Ultra-Low Long-Term Drift .... 150 nV/Month
- Low Temperature Drift .... 100 nV/°C
- Low DC Input Bias Current .... 15 pA
- High Gain, CMRR and PSRR .... 110 dB Min
- Low Input Noise Voltage .... 0.2 μV_{P-P}; DC to 1 Hz
- Internally-Compensated for Utility-Gain Operation
- Clamp Circuit for Fast Overload Recovery

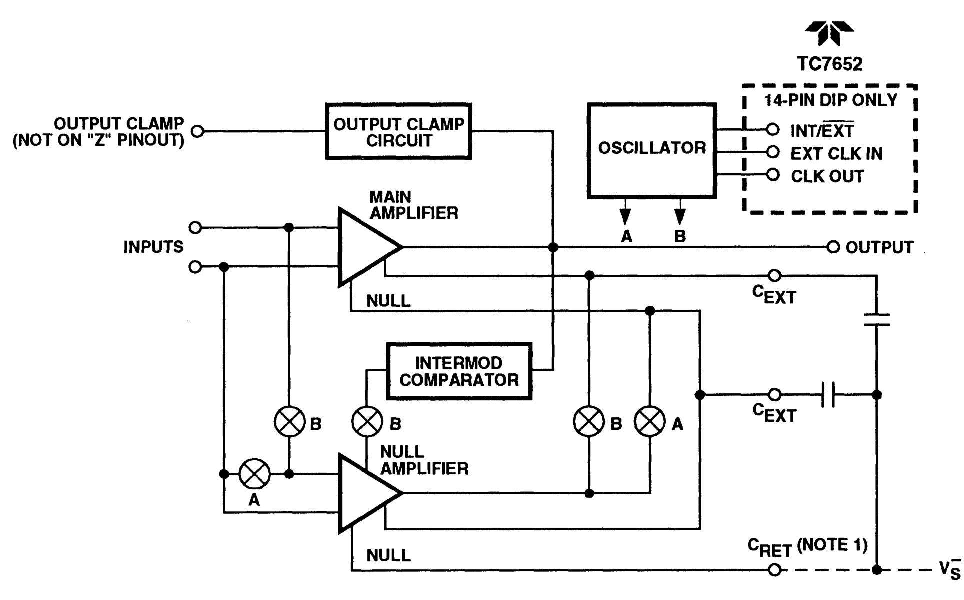
GENERAL DESCRIPTION

The TC7652 low noise, chopper-stabilized operational amplifier improves noise performance and provides a wider common-mode input voltage range. It offers low-input offset voltage and time/temperature stability, with reduced bandwidth and slew rate. CMOS circuitry eliminates most chopping spikes intermodulation effects and overrange lockup problems.

The TC7652 compares inverting and noninverting input voltages in an amplifier nulled by alternate clock phases. Two external capacitors store the correcting potentials on two amplifier-nulling inputs. All control circuitry, including the clock oscillator, is self-contained. The TC7652 is internally-compensated for unity-gain operation. If required, the 14-pin version can use an external clock.

The functional diagram shows the main components of the TC7652. The main and nulling amplifiers have offset-null capability. The main amp is continuously connected

FUNCTIONAL DIAGRAM



NOTE: 1. For 8-pin DIP connect to V_S^-, or to C_{RET} on "Z" pinout.

*Patented

from input to output. Controlled by the chopping-frequency oscillator and clock circuit, the nulling amp alternately nulls itself and the main amp. The nulling connections (MOSFET gates) are high impedance. Two external capacitors provide nulling potential storage and nulling loop-time constraints. Nulling operates over the full common-mode and power supply ranges. Independent of the output level, this arrangement gives exceptionally high CMRR, PSRR, and A_{VOL}.

The input switches are closely matched to reduce chopper frequency charge injection at the input terminals. The main cause of output spikes in this type circuit (feed-forward-type injection into the compensation capacitor) is minimized.

Other chopper-stabilized amplifiers experience intermodulation effects between chopper frequency and input signals. The finite AC gain of the amplifier requires a small AC signal at the input. The zeroing circuit sees this as an error signal, which it chops and feeds back. The circuit also injects sum-and-difference frequencies and causes gain and phase/frequency characteristics disturbances near the chopping frequency.

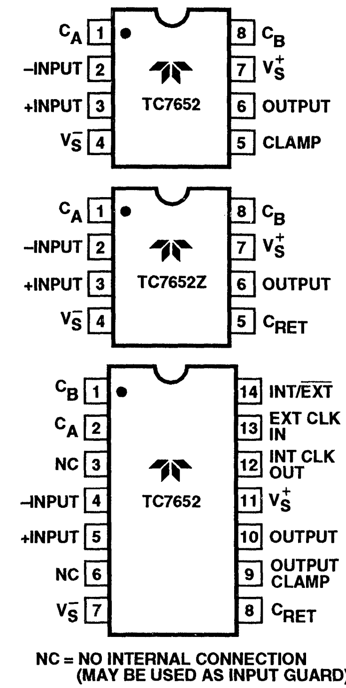
The TC7652 reduces these intermodulation effects by feeding the nulling circuit a dynamic current that corresponds to the compensation capacitor current and cancels the portion of the input signal from finite AC gain. In this way, the major cause of TC7652 error is minimized. The gain and phase disturbances are held to such low values that they can usually be ignored.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) .... +18V
Input Voltage .... (V_S^++0.3V) to (V_S^-–0.3V)
Voltage on Oscillator Control Pins .... V_S^+ to V_S^-
Duration of Output Short Circuit .... Indefinite
Current Into Any Pin .... 10 mA
While Operating (Note 4) .... 100 µA
Continuous Total Power Dissipation (T_A = 25°C)
CerDIP .... 500 mW
Plastic DIP .... 375 mW
Storage Temperature Range .... –65°C to +150°C
Operating Temperature Range
C Device .... 0°C to +70°C
I Device .... –25°C to +85°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



ORDERING INFORMATION

Part No.	Package	Temperature Range
TC7652CPA	8-Pin Plastic DIP	0°C to +70°C
TC7652ZCPA	8-Pin Plastic DIP	0°C to +70°C
TC7652IJA	8-Pin CerDIP	–25°C to +85°C
TC7652CPD	14-Pin Plastic DIP	0°C to +70°C
TC7652IJD	14-Pin CerDIP	–25°C to +85°C
TC7652MJA	8-Pin CerDIP	–55°C to +125°C
TC7652MJD	14-Pin CerDIP	–55°C to +125°C
TC7652ZMJA	8-Pin CerDIP	–55°C to +125°C
TC7652ZIJA	8-Pin CerDIP	–25°C to +85°C

LOW NOISE, CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

TC7652

ELECTRICAL CHARACTERISTICS: $V_S^+ = +5V$, $V_S^- = -5V$, $T_A = +25°C$, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OS}	Input Offset Voltage	$T_A = +25°C$ Over Operating Temperature Range (Note 1)		±2 ±10	±5	μV
TCV_{OS}	Average Temperature Coefficient of Input Offset Voltage	Operating Temperature Range (Note 1)		0.01	0.05	μV/°C
$V_{OS}/\Delta T$	Offset Voltage vs Time			150		nV/mo
I_{BIAS}	Input Bias Current (CLK On)	$T_A = +25°C$ $0°C < T_A < +70°C$ $-25°C < T_A < +85°C$		30 100 250	100 1000	pA pA pA
I_{BIAS}	Input Bias Current (CLK Off)	$T_A = +25°C$ $0°C < T_A < +70°C$ $-25°C < T_A < +85°C$		15 35 100	30	pA pA pA
I_{OS}	Input Offset Current	$T_A = +25°C$		25	150	pA
R_{IN}	Input Resistance			10^{12}		Ω
OL	Large Signal Voltage Gain	$R_L = 10\ k\Omega$ $V_{OUT} = \pm 4V$	120	150		dB
V_{OUT}	Output Voltage Swing (Note 3)	$R_L = 10\ k\Omega$ $R_L = 100\ k\Omega$	±4.7	±4.85 ±4.95		V V
CMVR	Common-Mode Voltage Range		–4.3		+3.5	V
MRR	Common-Mode Rejection Ratio	CMVR = –4.3V to +3.5V	120	140		dB
PSRR	Power Supply Rejection Ratio	±3V to ±8V	120	140		dB
e_N	Input Noise Voltage	$R_S = 100\Omega$, DC to 1 Hz DC to 10 Hz		0.2 0.7	1.5 5	μV_{P-P} μV_{P-P}
I_N	Input Noise Current	f = 10 Hz		0.01		pA/√Hz
GBW	Unity-Gain Bandwidth			0.4		MHz
SR	Slew Rate	$C_L = 50$ pF, $R_L = 10\ k\Omega$		1		V/μs
	Overshoot			15		%
V_S^+, V_S^-	Operating Supply Range		5		16	V
I_S	Supply Current	No Load		1	3	mA
f_{CH}	Internal Chopping Frequency	Pins 12–14 Open (DIP)	100	275		Hz
	Clamp ON Current (Note 2)	$R_L = 100\ k\Omega$	25	100		μA
	Clamp OFF Current (Note 2)	$-4V \leq V_{OUT} < +10V$		1		pA

NOTES:
1. –25°C to +85°C, or 0°C to +70°C.
2. See "Output Clamp" under detailed description.
3. Output clamp not connected. See typical characteristics curves for output swing versus clamp current characteristics.
4. Limiting input current to 100 μA is recommended to avoid latch-up problems. Typically, 1 mA is safe; however, this is not guaranteed.

Capacitor Connection

Connect the null-storage capacitors to the C_A and C_B pins with a common connection to the C_{RET} pin (14-pin TC7652 or 8-pin TC7652Z) or to V_S^- (8-pin TC7652). When connecting to V_S^-, avoid injecting load current IR drops into the capacitive circuitry by making this connection directly via a separate wire or PC trace.

Output Clamp

In chopper-stabilized amplifiers, the output clamp pin reduces overload recovery time. When a connection is made to the inverting input pin (summing junction), a current path is created between that point and the output pin, just before the device output saturates. This prevents uncontrolled differential input voltages and charge buildup on correction-storage capacitors. Output swing is reduced.

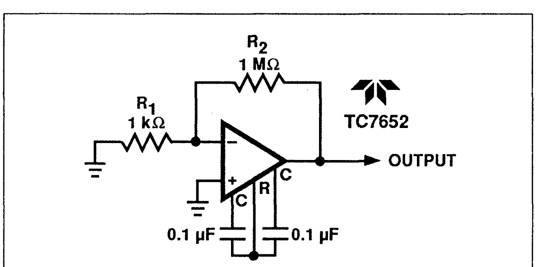
Clock

The TC7652 has a 550 kHz internal oscillator, which is divided by two before clocking the input chopper switches. The 275 Hz chopping frequency is available at INT CLK OUT (pin 12) on 14-pin devices. In normal operation, INT/$\overline{\text{EXT}}$ (pin 14), which has an internal pull-up, can be left open.

An external clock can also be used. To disable the internal clock and use an external one, the INT/$\overline{\text{EXT}}$ pin must be tied to V_S^-. The external clock signal is then applied to the EXT CLK IN input (pin 13). An internal divide-by-two provides a 50% switching duty cycle. The capacitors are only charged when EXT CLK IN is high, so a 50% to 80% positive duty cycle is recommended for higher clock frequencies. The external clock can swing between V_S^+ and V_S^-, with the logic threshold about 2.5V below V_S^+.

The output of the internal oscillator, before the divide-by-two circuit, is available at EXT CLK IN when INT/$\overline{\text{EXT}}$ is high or unconnected. This output can serve as the clock input for a second TC7652 (operating in a master/slave mode), so that both op amps will clock at the same frequency. This prevents clock intermodulation effects when two TC7652's are used in a differential amplifier configuration.

TEST CIRCUIT



If the TC7652's output saturates, error voltages on the external capacitors will slow overload recovery. This condition can be avoided if a strobe signal is available. The strobe signal is applied to EXT CLK IN and the overload signal is applied to the amplifier while the strobe is low. In this case, neither capacitor will be charged. The low leakage of the capacitor pins allow long measurements to be made with negligible errors (typical capacitor drift is 10 µV/sec).

APPLICATION NOTES

Component Selection

C_A and C_B (external capacitors) should be in the 0.1 µF to 1 µF range. For minimum clock ripple noise, use a 1 µF capacitor in broad bandwidth circuits. For limited bandwidth applications where clock ripple is filtered out, use a 0.1 µF capacitor for slightly lower offset voltage. High-quality film-type capacitors (polyester or polypropylene) are recommended, although a lower grade (ceramic) may work in some applications. For quickest settling after initial turn-on, use low dielectric absorption capacitors (e.g., polypropylene). With ceramic capacitors, settling to 1 µV takes several seconds.

Static Protection Although input diodes static protect all device pins, avoid strong static fields and discharges that can cause degraded diode junction characteristics and produce increased input-leakage currents.

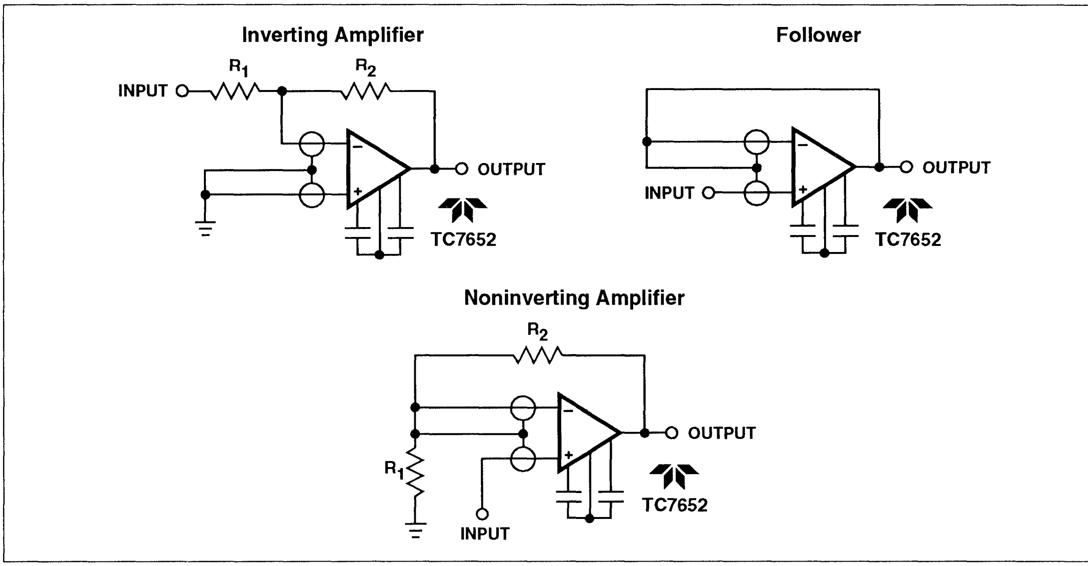
Latch-Up

Junction-isolated CMOS circuits have a 4-layer (p-n-p-n) structure similar to an SCR. Sometimes this junction can be triggered into a low-impedance state and produce excessive supply current. Therefore, avoid applying voltage greater than 0.3V beyond the supply rails to any pin. Establish the amplifier supplies at the same time or before any input signals are applied. If this is not possible, drive circuits must limit input current flow to under 1 mA to avoid latch-up, even under fault conditions.

Output Stage/Load Driving

The output circuit is high impedance (about 18 kW). With lesser loads, the chopper amplifier behaves somewhat like a transconductance amplifier with an open-loop gain proportional to load resistance. (For example, the open-loop gain is 17 dB lower with a 1 kW load than with a 10 kW load.) If the amp is used only for DC, the DC gain is typically greater than 120 dB (even with a 1 kW load), and this lower gain is inconsequential. For wideband, the best frequency response occurs with a load resistor of at least 10 kW. This produces a 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 2 degrees in the transition region, where the main amplifier takes over from the null amplifier.

CONNECTION OF INPUT GUARDS



Thermoelectric Effects

The thermoelectric (Peltier) effects in thermocouple junctions of dissimilar metals, alloys, silicon, etc. limit ultra-high-precision DC amplifiers. Unless all junctions are at the same temperature, thermoelectric voltages around 0.1 µV/°C (up to tens of µV/°C for some materials) are generated. To realize the low offset voltages of the chopper, avoid temperature gradients. Enclose components to eliminate air movement, especially from power-dissipating elements in the system. Where possible, use low thermoelectric-coefficient connections. Keep power supply voltages and power dissipation to a minimum. Use high-impedance loads and seek maximum separation from surrounding heat-dissipating elements.

Guarding

To benefit from TC7652 low-input currents, take care assembling printed circuit boards. Clean boards with alcohol or TCE, and blow dry with compressed air. To prevent contamination, coat boards with epoxy or silicone rubber.

Even if boards are cleaned and coated, leakage currents may occur because input pins are next to pins at supply potentials. To reduce this leakage, use guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard (a conductive ring surrounding inputs) is connected to a low-impedance point at about the same voltage as inputs. Then the guard absorbs leakage currents from high-voltage pins.

The 14-pin dual-in-line arrangement simplifies guarding. Like the LM108 pin configuration (but unlike the 101A and 741), pins next to inputs are not used.

Pin Compatibility

Where possible, the 8-pin device basic pinout conforms to such industry standards as the LM101 and LM741. Null-storing external capacitors connect to pins 1 and 8, which are usually for offset-null or compensation capacitors. Output clamp (pin 5) is similarly used. For OP05 and OP07 devices, replacement of the offset-null potentiometer (connected between pins 1 and 8 and V_S^+ by two capacitors from those pins to V_S^-) provides compatibility. Replacing the compensation capacitor between pins 1 and 8 by two capacitors to V_S^- is required. The same operation (with the removal of any connection to pin 5) works for LM101, µA748, and similar parts.

Because NC pins provide guarding between input and other pins, the 14-pin device pinout conforms closely to the LM108. Because this device does not use any extra pins and does not provide offset-nulling (but requires a compensation capacitor), some layout changes are necessary to convert to the TC7652.

Some Applications

Figures 1 and 2 show basic inverting and noninverting amplifier circuits using the output clamping circuit to enhance overload recovery performance. The only limitations on replacing other op amps with the TC7652 are supply voltage (±8V maximum) and output drive capability (10 kΩ load for full swing). Overcome these limitations with a booster circuit (Figure 3) to combine output capabilities of the LM741 (or other standard device) with input capabilities of the TC7652. These two form a composite device; therefore, when adding the feedback network, monitor loop gain stability.

Figure 4 shows the clamp circuit of a zero-offset comparator. Because the clamp circuit requires the inverting input to follow the input signal, problems with a chopper-stabilized op amp are avoided. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disrupting other parts of the system.

Figure 5 shows how the TC7652 can offset-null high slew rate and wideband amplifiers (such as Teledyne Components' 1437).

Mixing the TC7652 with circuits operating at ±15V requires a lower supply voltage divider with the TC7660 voltage converter circuit operated "backwards." Figure 6 shows an approximate connection.

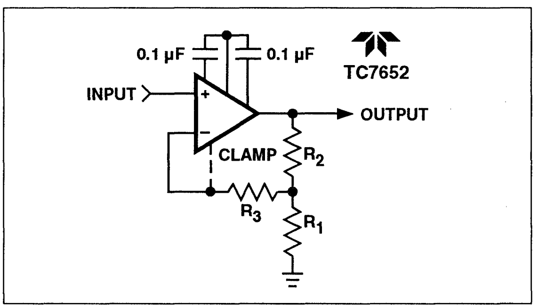


Figure 1 Noninverting Amplifier With Optional Clamp

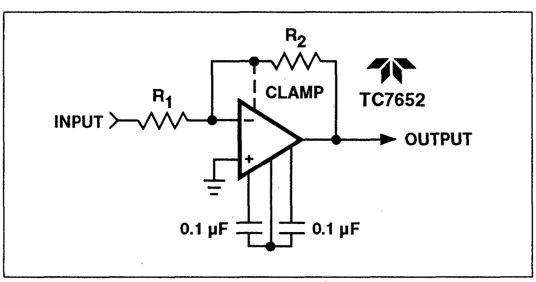


Figure 2 Inverting Amplifier With Optional Clamp

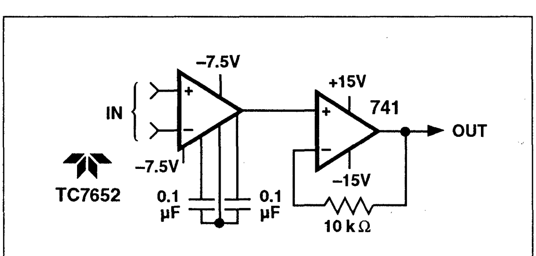


Figure 3 Using 741 to Boost Output Drive Capability

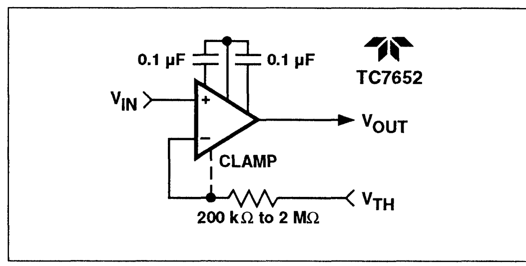


Figure 4 Low Offset Comparator

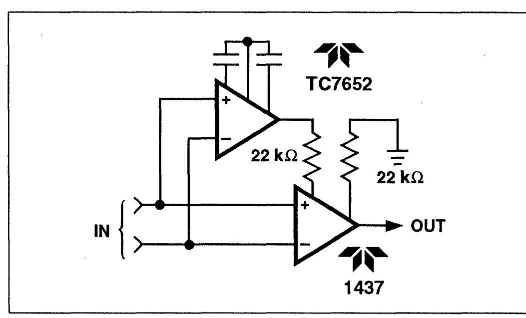


Figure 5 1437 Offset-Nulled by TC7652

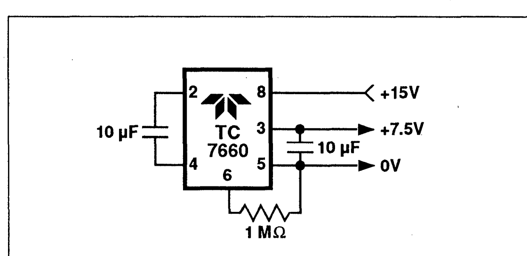
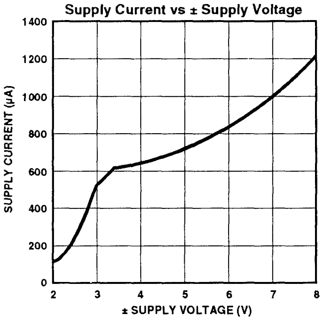


Figure 6 Splitting +15V With the 7660 at >95% Efficiency

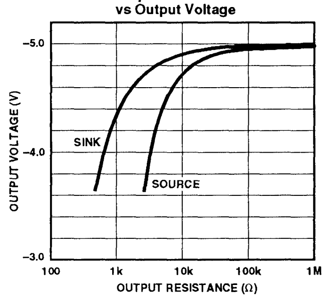
LOW NOISE, CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

TYPICAL CHARACTERISTICS CURVES

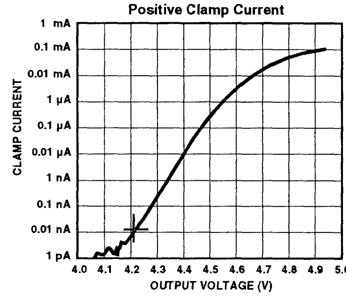
Supply Current vs ± Supply Voltage



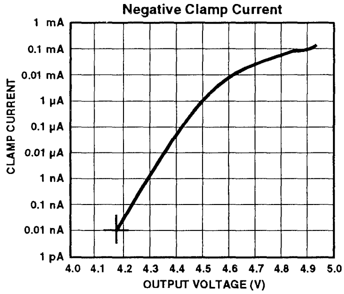
Output Resistance vs Output Voltage



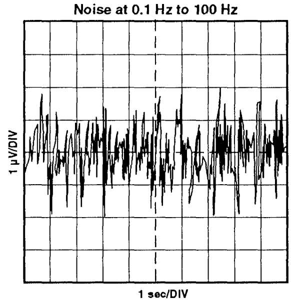
Positive Clamp Current



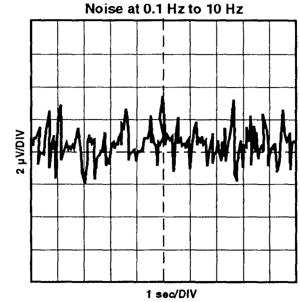
Negative Clamp Current



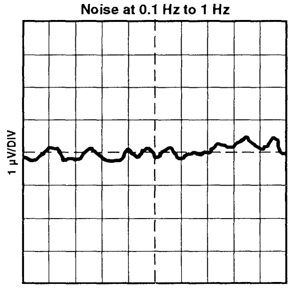
Noise at 0.1 Hz to 100 Hz



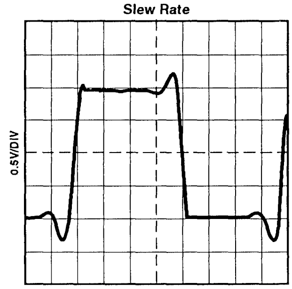
Noise at 0.1 Hz to 10 Hz



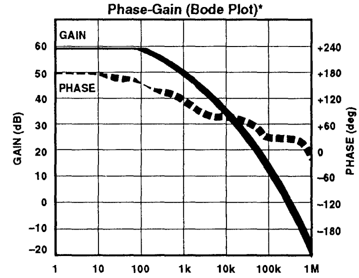
Noise at 0.1 Hz to 1 Hz



Slew Rate

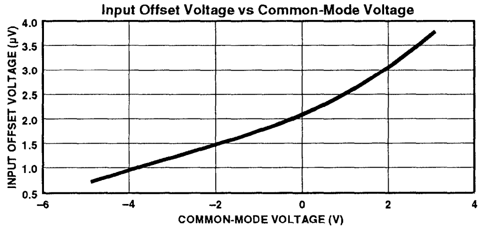


Phase-Gain (Bode Plot)*



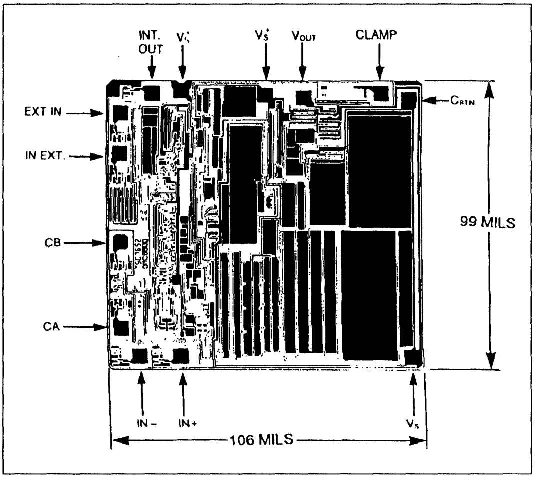
*NOTE: ±5V, ±2.5V supplies; no load to 10k load.

Input Offset Voltage vs Common-Mode Voltage



TC7652

BONDING DIAGRAM



TELEDYNE COMPONENTS

TC9420
TC9421

HIGH-VOLTAGE, AUTO-ZEROED OPERATIONAL AMPLIFIERS

FEATURES

- **High-Voltage Operation .... ±15V**
- **Low Offset Voltage .... 5 μV Max**
- **Low Offset Voltage Drift .... 0.1 μV/°C**
- **Low Input Bias Current .... 30 pA Max**
- **High Open-Loop Voltage Gain .... 140 dB**
- **Wide Common-Mode Voltage Range .... –15V to +13V**
- **Low Input Voltage Noise (0.1 Hz to 1 Hz) .... 0.2 μV$_{P-P}$**
- **Low Supply Current .... 1 mA**
- **Single Supply Operation .... 7V to 32V**
- **Output Clamp Speeds Overload Recovery Time**

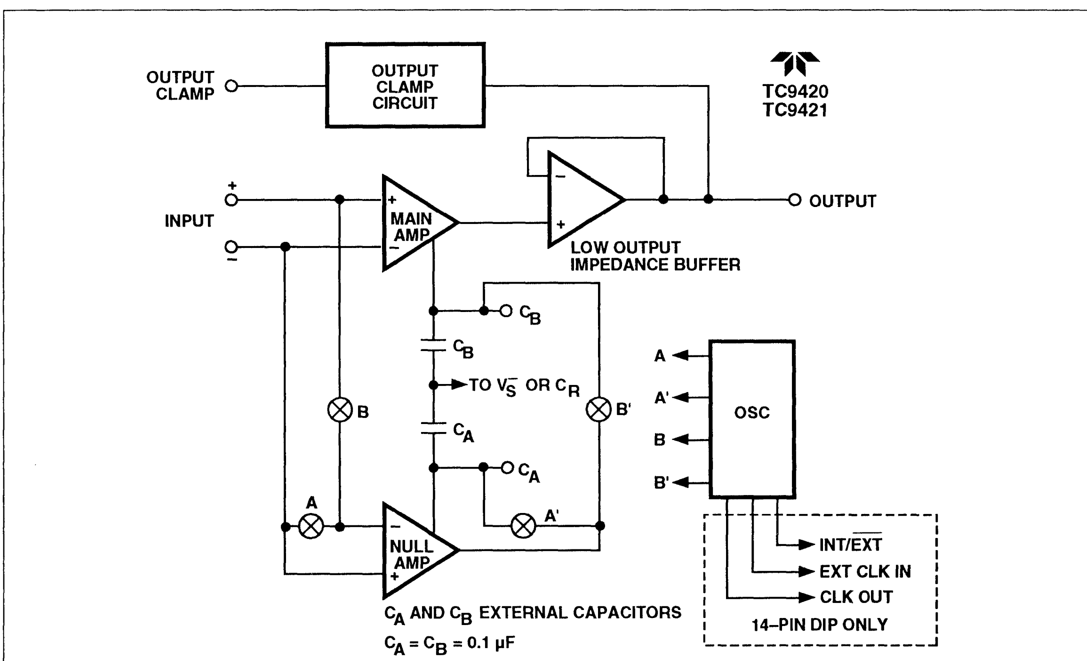
GENERAL DESCRIPTION

The TC9420 and TC9421 are high-voltage, high-performance, CMOS chopper-stabilized operational amplifiers. They can operate from the same ±15V power supplies as commonly used to power bipolar op-amps, such as the OP07 and OP741. Previous CMOS chopper amplifiers, such as the 7650, were limited to operating from ±7.5V supplies.

Maximum V_{OS} for the TC9420/TC9421 is only 5 μV, almost a factor of 14 improvement over the industry-standard OP07E. The maximum V_{OS} drift of 0.1 μV/°C is 12 times less than the OP07E. Input bias and offset currents, both only 30 pA maximum, are factors of 60 improvements.

8

FUNCTIONAL DIAGRAM



TC9420
TC9421

In addition to low initial offset errors, the nulling circuitry ensures excellent performance over time and temperature. Long-term drift, which results in periodic recalibration, is effectively eliminated. The nulling circuitry continues to operate over the full temperature range, whereas laser and "zener zap" trimming are only done at a single temperature. The result is a significant decrease in temperature-induced errors.

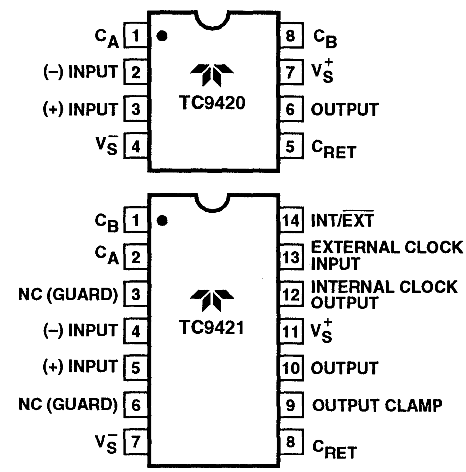
The TC9420/TC9421 operate from dual or single power supplies. Supply current is typically 1 mA with ±15V supplies. Single supply operation extends from +7V to +32V, and the input common-mode range extends to V_S^-. For battery operation, see the low-power TC900 data sheet.

The TC9420/TC9421 open-loop gain is 120 dB minimum. Unlike the 7650, the TC9420/TC9421 gain is independent of load resistance. The low impedance output will drive a 10 kΩ load to ±14V. An output clamp circuit is provided to minimize overload recovery time.

The TC9420/TC9421 use two amplifiers to correct offset voltage errors. A main amplifier is always in the signal path, which prevents switching spikes at the output. A separate nulling amplifier alternately corrects its own V_{OS} error. Only two external capacitors are required to store the nulling error voltages. All active nulling circuitry, including switches and oscillator, are included on the chip.

The TC9420/TC9421 are pin compatible with Maxim's MAX 420/421.

PIN CONFIGURATIONS



ORDERING INFORMATION

Part No.	Package	Temperature Range	Max V_{OS}
TC9420CPA	8-Pin Plastic DIP	0°C to +70°C	10 µV
TC9420EJA	8-Pin CerDIP	–40°C to +85°C	5 µV
TC9420EPA	8-Pin Plastic DIP	–40°C to +85°C	5 µV
TC9421CPD	14-Pin Plastic DIP	0°C to +70°C	10 µV
TC9421EJD	14-Pin CerDIP	–40°C to +85°C	5 µV
TC9421EPD	14-Pin Plastic DIP	–40°C to +85°C	5 µV

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) ....+36V
Input Voltage ....(V_S^+ + 0.3V) to (V_S^- – 0.3V)
Storage Temperature Range ....–65°C to +150°C
Lead Temperature (Soldering, 10 sec) ....+300°C
Current Into Any Pin ....10 mA
Operating Temperature Range
C Device ....0°C to +70°C
E Device..–40°C to +85°C
Package Power Dissipation (T_A = +25°C)
CerDIP Package ....500 mW
Plastic Package ....375 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S^+ = 15V, V_S^- = 15V, T_A = +25°C. Test circuit unless noted.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{OS}	Input Offset Voltage	T_A = +25°C	C		±1	±10	μV
			E		±1	±5	μV
		Over Temperature Range	C		±2	±20	μV
			E		±2	±10	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Average Temperature Coefficient of Input Offset Voltage	Over Temperature Range	E		0.02	0.1	μV/°C
I_B	Input Bias Current	T_A = +25°C	C		10	100	pA
			E		10	30	pA
		Over Temperature Range	C		30		pA
			E		35		pA
I_{OS}	Input Offset Current	T_A = +25°C	C		15	200	pA
			E		15	60	pA
		Over Temperature Range	C		30		pA
			E		50		pA
R_{IN}	Input Resistance				10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	R_L = 10 kΩ, V_{OUT} = ±10V, T_A = +25°C		120	150		dB
		Over Temperature Range		120	150		dB
V_{OUT}	Output Voltage Swing	CLAMP Not Connected	R_L = 10 kΩ	±12	±14.5		V
			R_L = 100 kΩ		±14.95		V
CMVR	Common-Mode Voltage Range			+12, −15	+13, −15.1		V
CMRR	Common-Mode Rejection Ratio	CMVR = +12V to −15V Over Temperature Range		120	140		dB
PSRR	Power Supply Rejection Ratio	±3V to ±16.5V Over Temperature Range		120	140		dB
e_N	Input Noise Voltage (Peak-to-Peak Value Not Exceeded 95% of Time)	R_S = 100Ω	DC to 1 Hz		0.3		μV_{P-P}
			DC to 10 Hz		1.1		μV_{P-P}
I_N	Input Noise Current	f = 10 Hz			0.01		$pA/\sqrt{Hz}$
UGBW	Unity-Gain Bandwidth				500		kHz
sr	Slew Rate	C_L = 50 pF, R_L = 10 kΩ			0.5		V/μs
t_R	Rise Time				0.7		μs
	Overshoot				20		%
V_S^+, V_S^-	Operating Supply Range (Note 1)			±2.5		±16.5	V
I_S	Supply Current	No Load, T_A = +25°C			1.3	2	mA
		Over Temperature Range				3.5	mA
f_{CH}	Internal Chopping Frequency	Pins 12–14 Open (TC9421)			250		Hz
	Clamp ON Current	R_L = 100 kΩ		25	100		μA
	Clamp OFF Current	$-10V \leq V_{OUT} \leq +10V$			1		pA
	Offset Voltage vs Time				100		$nV/\sqrt{Mo}$

NOTES: 1. Single supply operation: V_S^+ = +7V to +32V.

8

Theory of Operation

Figure 1 shows the major elements of the TC9420/TC9421. There are two amplifiers: the main (signal) amplifier and the nulling amplifier. Both have offset nulling capability. The main amplifier is always connected to the output. The nulling amplifier alternately samples and adjusts its own offset and then the offset of the main amplifier.

A two-phase operation nulls the main amplifier. During the first phase, the A pair of switches close, while the B switches open. Then nulling amp's inputs are shorted and its output is fed back to the nulling input. Capacitor C_A charges to a voltage which will maintain the nulling amp in its nulled state.

During the second phase, the B switches close and the A switches open. The nulling amp's inputs now sample the offset voltage of the main amp. The nulling amp drives the main amp's nulling input to cancel the main amplifier's offset voltage. Capacitor C_B stores the nulling voltage of the main amplifier while the nulling amp is being nulled on the next cycle.

The TC9420/TC9421 design also incorporates an additional output buffer stage. The buffer provides a low impedance output traditionally associated with bipolar op amps. Some CMOS chopper-stabilized amplifiers, such as the 7650, have a high output impedance which makes open-loop gain proportional to load resistance. The TC9420/TC9421 open-loop gain is not dependent on load resistance.

Pin Compatibility

Since the TC9420/9421 operate from the same ±15V power supplies as bipolar op amps, upgrading existing circuits is simple. The bipolar op amp's nulling and compensation components are removed, and the TC9420/TC9421 nulling capacitors are added.

On the 8-pin mini-DIP (TC9420), the external null storage capacitors are connected to pins 1 and 8. On most other op amps they are left open or used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, replacing the offset null pot between pins 1 and 8 with two capacitors from the pins to C_{RET} will convert the OP05/07 pin configuration for TC9420 operation. The 741 is easily upgraded by removing the nulling pot between pin 4 and pins 1 and 5, then connecting capacitors from pin 4 to pins 1 and 8. For LM108 devices, the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pinouts are modified similarly by also removing any circuit connections to pin 5.

The minor modifications needed to retrofit a TC9420 into existing sockets make prototyping and circuit verification straightforward.

Nulling Capacitors

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to C_{RET} (pin 5) on the 8-pin packages and to capacitor return (C_{RET}, pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops.

Internally, V_S^- is connected to C_{RET}.

C_A and C_B should be 0.1 µF film capacitors. Mylar capacitors are suitable.

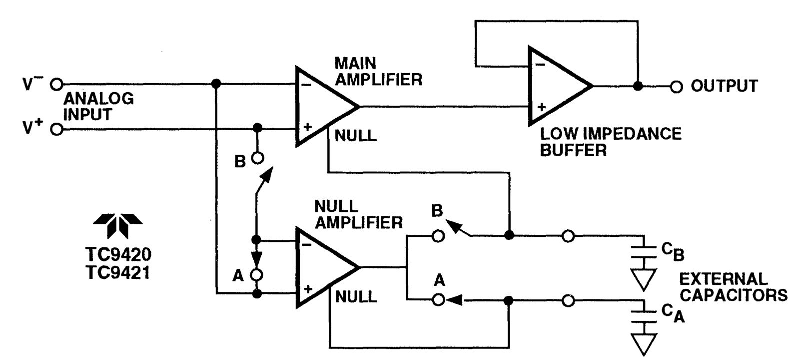


Figure 1. TC9420/TC9421 Contain a Nulling and Main Amplifier. Offset Correction Voltages Are Stored on Two External Capacitors.

HIGH-VOLTAGE, AUTO-ZEROED OPERATIONAL AMPLIFIERS

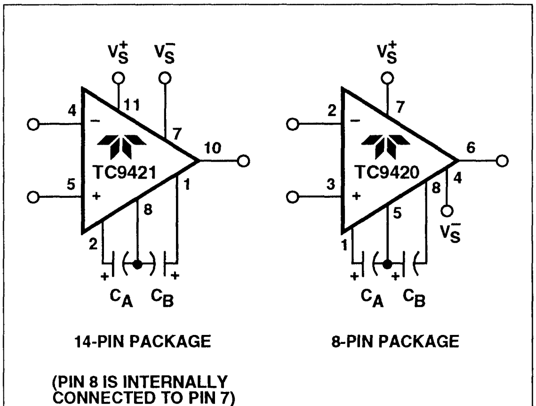


Figure 2. Nulling Capacitor Connection

Component Selection

The two required capacitors, C_A and C_B, have optimum values, depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and nulling time constant, the capacitor values should be scaled in proportion to the external clock, if used. High-quality film-type capacitors (such as Mylar) are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.

Clock Operation

The internal oscillator is set for a 1000 Hz nominal frequency on both the 8-pin and 14-pin DIPs. With the 14-pin DIP (TC9421), the 250-Hz internal frequency is available at the internal clock output (pin 12). A 1000 Hz nominal signal will be present at the external clock input (pin 13) with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before a ÷4 operation.

The 14-pin device can be driven by an external clock. The INT/$\overline{\text{EXT}}$ input (pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/$\overline{\text{EXT}}$ must be tied to V_S^- (pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6V, and between V_S^+ and V_S^+ –6V for higher supply voltages. When the external clock is generated by +5V logic, capacitive coupling to pin 13 (through a 0.1 μF capacitor) will provide adequate drive.

At low frequencies, the external clock duty cycle is not critical, since an internal ÷4 gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50% to 80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. This function can be used to prevent input transients from overloading the nulling circuitry. Leakage currents at the capacitor pins are very low, so offset voltage drift during strobe operation is minimized.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TC9421 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3, with typical inverting and noninverting circuit connections shown in Figures 4 and 5. For the clamp to be fully effective, the impedance across the clamp output should be >100 kΩ.

When the clamp is used, the clamp "OFF" leakage will add to input bias current. However, clamp leakage in the "OFF" state is typically only 1 pA.

Input Bias Current

The TC9420/TC9421 are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling, however, causes charge transfer at the inputs.

The impulse current is not usually a problem because the amount of charge transferred is very small. Care should be exercised, however, when replacing high-input bias current bipolar op amps. Conventional design practice is to cancel bias current by matching the input impedances (Figure 6a). The TC9420/TC9421 have input bias current of

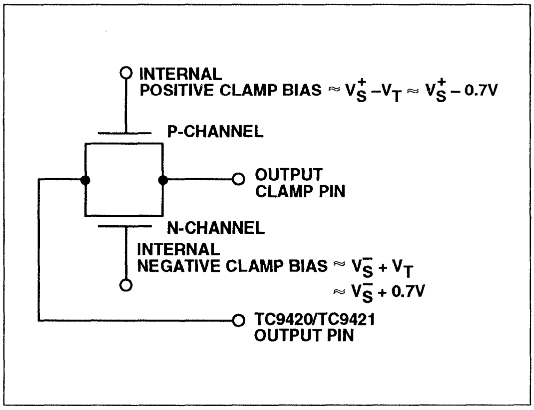


Figure 3. Internal Clamp Circuit

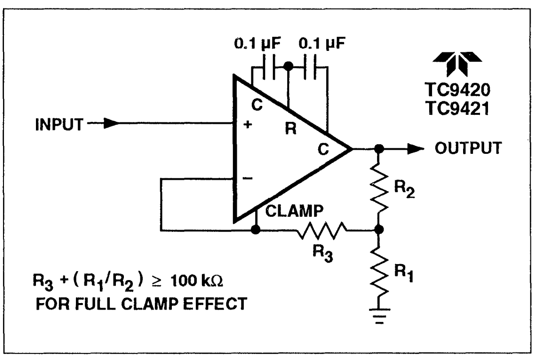


Figure 4. Noninverting Amplifier With Optional Clamp

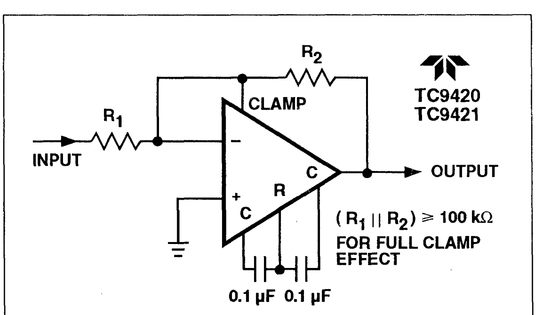


Figure 5. Inverting Amplifier With Optional Clamp

only 100 pA maximum, so the additional resistor is not necessary. In fact, including the resistor makes the charge injection current, passing through the impedance-balancing resistor, appear as a noise source. When replacing an existing op amp with the TC9420/TC9421, omit the resistor or bypass it to ground with a capacitor (Figure 6b).

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances, this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, voltages greater than 0.3V beyond the supply rails should not be applied to any pin. In general, the amplifier supplies must be established at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latch-up.

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, eductional materials, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072

- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520

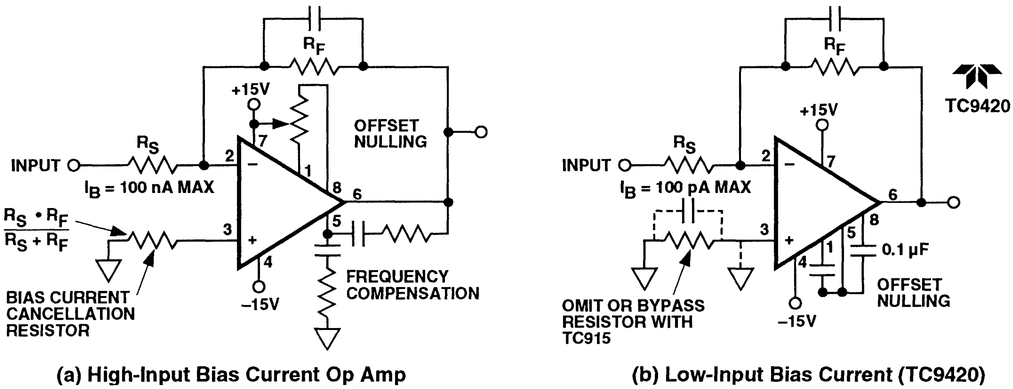
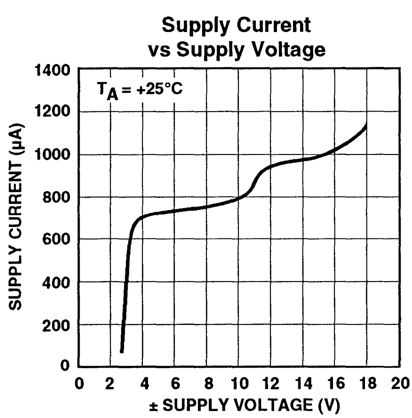
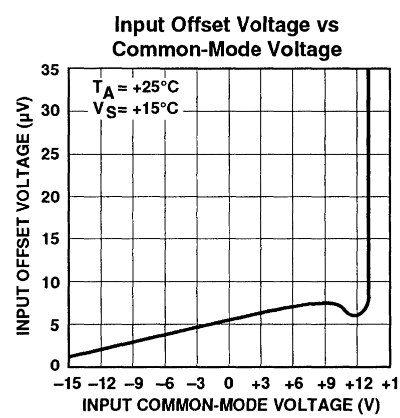


Figure 6. Input Bias Current Cancellation

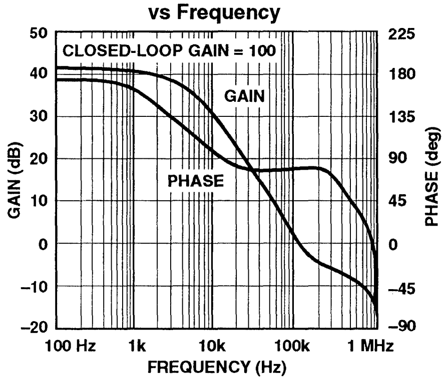
TYPICAL CHARACTERISTICS CURVES



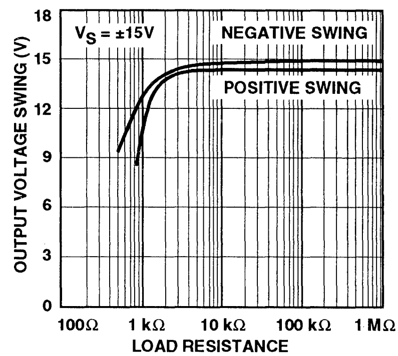


TYPICAL CHARACTERISTICS CURVES (Cont.)

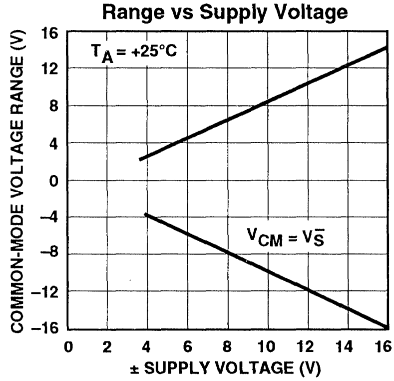
Gain and Phase vs Frequency



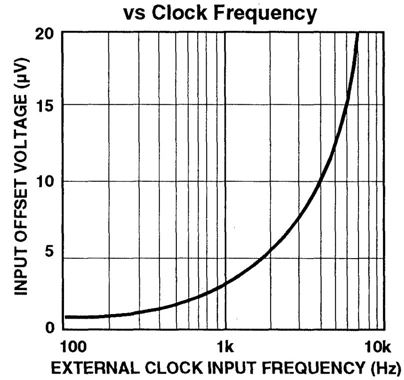
Output Voltage Swing vs Load Resistance



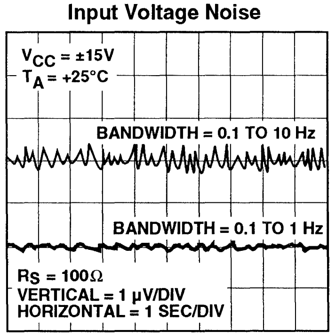
Input Common-Mode Voltage Range vs Supply Voltage



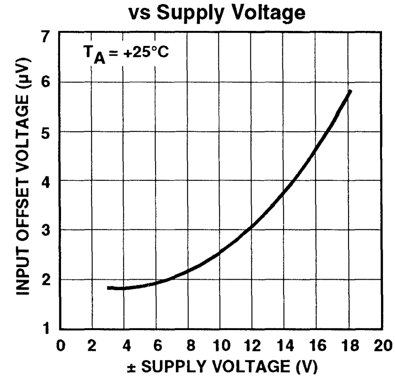
Input Offset Voltage vs Clock Frequency



Input Voltage Noise

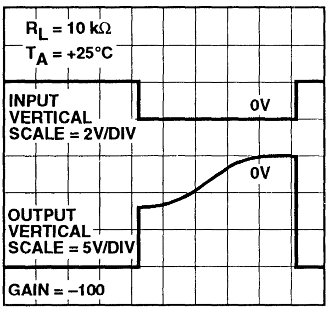


Input Offset Voltage vs Supply Voltage



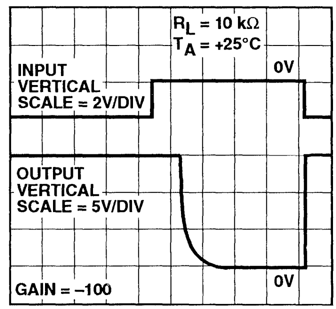
TYPICAL CHARACTERISTICS CURVES (Cont.)

Negative Overload Recovery Time



HORIZONTAL SCALE = 50 ms/DIV

Positive Overload Recovery Time



HORIZONTAL SCALE = 50 ms/DIV

NOTES

Section 9

High Performance Amplifiers/Buffers

TELEDYNE COMPONENTS

WIDEBAND, HIGH SLEW RATE OPERATIONAL AMPLIFIER

FEATURES

- Low Cost
- Fast Settling ....0.1% in 1 μsec
- Slew Rate 35V/μsec
- Full Power Bandwidth ....600 kHz
- Open Loop Gain ....100 dB
- Gain Bandwidth Product ....100 MHz

APPLICATIONS

- High-Frequency Amplifiers
- Current-to-Voltage Converters
- Video Amplifiers
- Differential Amplifiers
- Line Drivers
- Wideband Precision

GENERAL DESCRIPTION

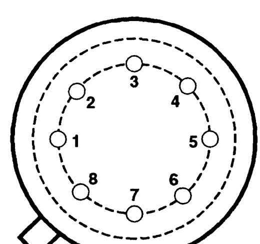
The 1321 is a bipolar input operational amplifier that combines high speed AC performance (35V/μs slew rate, 100 MHz GBWP) with superior DC characteristics (300 MΩ input impedance, ±5 nA input bias current, 100 dB gain). This combination of features makes it ideal for video and pulse amplifiers, fast integrators, high-Q active filters, and high-speed current-to-voltage converters.

This device is internally compensated for stable operation in circuits operating at closed loop gains of 5 or above. For operation at lower closed loop gains, an external compensation capacitor is required from Pin 8 to ground (or the alternate stabilizing scheme shown in Figure 1 may be used).

The standard 1321 is housed in a small outline, metal TO-99 case and is specified for 0°C to +75°C operation.

PIN CONFIGURATION

Pin No.	Designation
1	OFFSET ADJUST
2	-IN
3	+IN
4	$-V_{CC}$
5	OFFSET ADJUST
6	OUTPUT
7	$+V_{CC}$
8	BANDWIDTH CONTROL



BOTTOM VIEW

1321

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage .... ±22.5V
V_{IDF} Differential Input Voltage .... ±12V
T_C Operating Temperature Range (Case)
1321 .... 0°C to +75°C
T_{STG} Storage Temperature Range ...... –65°C to +150°C

ELECTRICAL CHARACTERISTICS: T_C = +25°C, ±V_{CC} = ±15V, R_L = 2 kΩ unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
I_b	Input Bias Current		—	±5	±25	nA
		T_{MIN} to T_{MAX}	—	—	±40	nA
IOS	Input Offset Current		—	±5	±25	nA
		T_{MIN} to T_{MAX}	—	—	±40	nA
VOS	Input Offset Voltage	Without external trim	—	±3	±5	mV
VOS TC	VOS vs Temperature		—	±5	—	μV/°C
PSRR	Input Offset vs Power Supply		—	90	—	dB
V_{ICM}	Common Mode	For DC linear operation	±11	±12	—	V
CMRR	Common Mode Rejection Ratio	@ DC	—	100	—	dB
Z_{ID}	Differential Input Impedance	@ DC	—	300	—	MΩ
Output						
VO	Voltage		±10	±12	—	V
IO	Current		±10	±18	—	mA
Voltage Gain						
AOL	Open Loop Voltage Gain	@ DC	98	104	—	dB
ACL	Closed Loop Gain	Stable operation w/o compensation	14	—	—	dB
Frequency Response						
GBWP	Gain Bandwidth Product	ACL = 10, C_C = 0 pF, f_t = 10 kHz	70	100	—	MHz
FPBW	Full Power Bandwidth	ACL ≥ 5, C_C = 0 pF	320	600	—	kHz
Time Response						
ts	Settling Time 10V step to 0.1%		—	1	—	μs
sr	Slew Rate	ACL ≥ 5, C_C = 0 pF	±20	±35	—	V/μs
Noise (Referenced to Input)						
en	Midband (fo = 10 Hz)		—	45	—	nV/√Hz
	Highband (fo = 100 Hz)		—	25	—	nV/√Hz
	Wideband (fo = 1 kHz to 100 kHz)		—	15	—	nV/√Hz
Power Supplies						
V_{CC}	Power Supply Voltage		—	±15	±22.5	V
I_{CC}	Quiescent Supply Current	V_{CC} = ±15V	—	±3	±4	mA

WIDEBAND, HIGH SLEW RATE OPERATIONAL AMPLIFIER

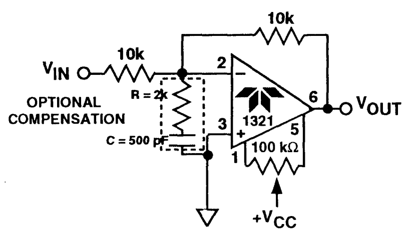


Figure 1. Optional Stabilizing Scheme (for unity gain stability at high speed)

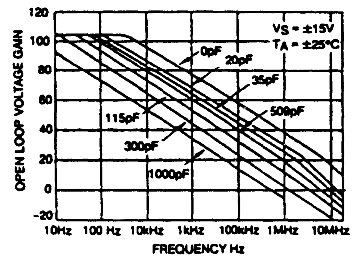


Figure 2. Bode Plot

NOTES

TELEDYNE COMPONENTS

WIDEBAND, HIGH SLEW RATE OPERATIONAL AMPLIFIER

FEATURES

- Low Cost
- Fast Settling .... 0.1% in 200 ns typ.
- Slew Rate 120V/µsec
- Full Power Bandwidth .... 1.6 MHz
- Open Loop Gain .... 84 dB
- Gain Bandwidth Product .... 20 MHz

APPLICATIONS

- High-Frequency Amplifiers
- Current-to-Voltage Converters
- Video Amplifiers
- Differential Amplifiers
- Line Drivers
- Wideband Precision

GENERAL DESCRIPTION

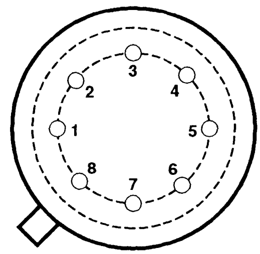
The 1322 is a high-speed, fast-settling operational amplifier designed for a wide variety of high-speed signal processing tasks. Its fast, accurate settling performance (200 ns to 0.1% accuracy for a 10V step) and good DC specifications (84 dB open loop gain, 10 mV offset voltage) make the 1322 eminently suitable for high speed 8- and 10-bit data conversion applications. In addition, its high slew rate (120V/µs) serves it well in high-speed pulse circuits, signal generators, or other circuits where full output swings at signal frequencies as high as 1.6 MHz are required.

This device is internally compensated for stable operation in circuits operating at closed loop gains of 3 or above. For operation at lower closed loop gains, an external compensation capacitor is required from Pin 8 to ground (or the alternate stabilizing scheme shown in Figure 1 may be used).

The standard 1322 is housed in a small outline, metal TO-99 case and is specified for 0°C to +75°C operation.

PIN CONFIGURATION

Pin No.	Designation
1	OFFSET ADJUST
2	-IN
3	+IN
4	$-V_{CC}$
5	OFFSET ADJUST
6	OUTPUT
7	$+V_{CC}$
8	BANDWIDTH CONTROL



BOTTOM VIEW

1322

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage .... ±20V
V_{IDF} Differential Input Voltage .... ±15V
T_C Operating Temperature Range (Case)
1322 .... 0°C to +75°C
T_{STG} Storage Temperature Range ...... −65°C to +150°C

ELECTRICAL CHARACTERISTICS: T_C = +25°C, $\pm V_{CC}$ = ±15V, R_L = 2 kΩ unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
I_b	Input Bias Current		—	±125	±250	nA
		T_{MIN} to T_{MAX}	—	—	±500	nA
IOS	Input Offset Current		—	±20	±50	nA
		T_{MIN} to T_{MAX}	—	—	±100	nA
VOS	Input Offset Voltage	Without external trim	—	±5	±10	mV
VOS TC	VOS vs Temperature		—	±30	—	µV/°C
PSRR	Input Offset vs Power Supply		—	90	—	dB
V_{ICM}	Common Mode	For DC linear operation	±10	—	—	V
CMRR	Common Mode Rejection Ratio	@ DC	—	90	—	dB
Z_{ID}	Differential Input Impedance	@ DC	40	100	—	MΩ
Output						
VO	Voltage		±10	±12	—	V
IO	Current		±10	±20	—	mA
Voltage Gain						
AOL	Open Loop Voltage Gain	@ DC	77	84	—	dB
ACL	Closed Loop Gain	Stable operation w/o compensation	10	—	—	dB
Frequency Response						
GBWP	Gain Bandwidth Product	ACL = 10, f = 10 kHz	10	20	—	MHz
FPBW	Full Power Bandwidth	ACL ≥ 3, C_C = 0	1.2	1.6	—	MHz
Time Response						
ts	Settling Time	10V step to 0.1%	—	200	—	ns
sr	Slew Rate	ACL = 3, C_C = 0	±80	±120	—	V/µs
Noise (Referenced to Input)						
en	Wideband (10 Hz to 1 kHz)		—	1	—	μV_{RMS}
Power Supplies						
V_{CC}	Power Supply Voltage		—	±15	±20	V
I_{CC}	Quiescent Supply Current	V_{CC} = ±15V	—	±4	±6	mA

WIDEBAND, HIGH SLEW RATE OPERATIONAL AMPLIFIER

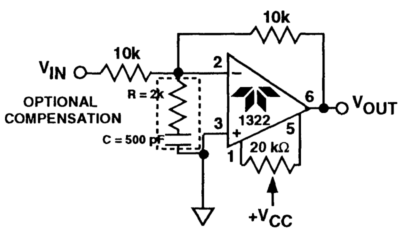


Figure 1. Optional Stabilizing Scheme
(for unity gain stability at high speed)

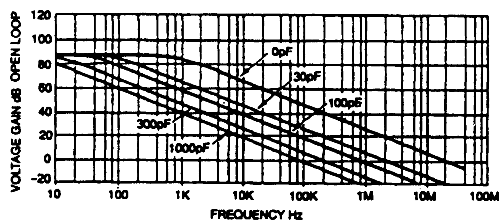


Figure 2. Bode Plot

NOTES

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FEATURES

- **Full Power Frequency .... 25 kHz**
- **$\pm V_{CC}$ Range .... ±40V**
- **Common Mode Range .... ±35V**
- **Slew Rate .... ±5V/µs**

APPLICATIONS

- **Precision High Voltage Source**
- **Avionics, 48V Operation**
- **Process Control**

GENERAL DESCRIPTION

The 1332 bipolar amplifier provides solutions to problems not solved with the typical 741. Specifications are optimized to provide such capabilities as low drift, high output voltage swing and high speed.

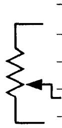
This true differential operational amplifier is matched pin-for-pin with the standard 741 (including 10 KΩ optional trim-pot connection).

The 1332's smooth 6 dB/octave roll off provides stable operation at all values of gain, even when connected as a unity gain follower.

The 1332 has a low initial offset voltage of 6 mV and is specified for 0°C to +75°C operation.

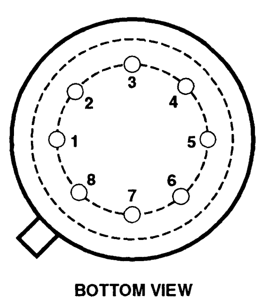
9

PIN CONFIGURATION



Optional E_{OS} Trim 10 kΩ

Pin No.	Designation
1	OFFSET ADJUST
2	-IN
3	+IN
4	$-V_{CC}$
5	OFFSET ADJUST
6	OUTPUT
7	$+V_{CC}$
8	NC (Bandwidth Control)



BOTTOM VIEW

1332

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply Voltage	±40V
V_{IDF}	Differential Input Voltage	$\pm V_{CC}$
V_{ICM}	Common Mode Input Voltage	$\pm V_{CC}$
T_C	Operating Temperature Range (Case)	
	1332	0°C to +75°C
T_{STG}	Storage Temperature Range	–65°C to +150°C

ELECTRICAL CHARACTERISTICS: T_C = +25°C, V_{CC} = ±40V, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
I_B	Initial Input Bias Current	Without External Trim	—	—	30	nA
I_B/TC	I_B vs Temperature		—	—	0.4	nA/°C
I_{OS}	Input Offset Current		—	—	30	nA
V_{OS}	Input Offset VoltageWithout External Trim		—	±2	±6	mV
V_{OS}/TC	V_{OS} vs Temperature		—	±15	±20	µV/°C
PSRR	Input Offset vs Power Supply	@ DC	74	90	—	dB
V_{ICM}	Common-Mode Input Voltage	DC Linear Operation	—	—	±35	V
CMRR	Common-Mode Rejection Ratio	@ DC	74	100	—	dB
Z_{IDF}	Differential-Mode Input Impedance		—	200	—	MΩ
Z_{ICM}	Common-Mode Input Impedance		—	1000	—	MΩ
Output						
V_O	Output Voltage		±35	—	—	V
I_O	Output Current		±10	±12	—	mA
Voltage Gain						
A_{OL}	Open-Loop Voltage Gain	R_L = Rated Load	100	106	—	dB
Frequency Response						
UGBW	Unity Gain Bandwidth	Open Loop	—	4	—	MHz
FPBW	Full Power Bandwidth	Sine Wave, 3 to 5% distortion	—	25	—	kHz
Time Response						
sr	Slew Rate		—	±5	—	V/µs
Power Supplies						
V_{CC}	Power Supply Voltage		±10	—	±40	V
I_{CC}	Quiescent Supply Current	Quiescent	—	±3.2	±4.5	mA

NOTE: The inputs are protected to $\pm V_{CC}$. The output is protected against short circuit to ground.

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

The 1332, operating with a ±40V power supply, can drive ±35V into 2.7 kΩ at 25 kHz (Figures 1 & 2). Under maximum load conditions, the output can be short circuited to common without danger, as the output is limited by a chip temperature sensing circuit.

To decrease bandwidth, capacitance may be added between Pin 8 and common. The effect of this capacitance is shown in Figure 3.

Single Supply Operation

Figure 4 shows a 1332 operating as an inverter from a single supply. This will allow a 1332 to operate from a 48V aircraft or vessel power.

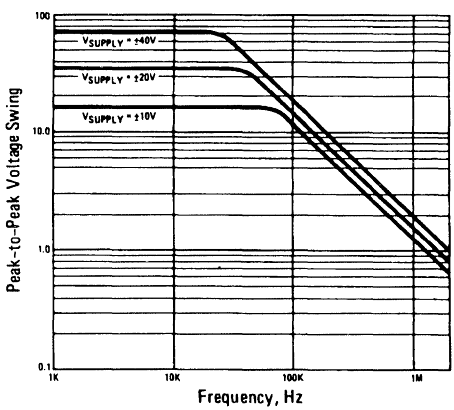


Figure 1. Output Voltage Swing vs Frequency at 25°C

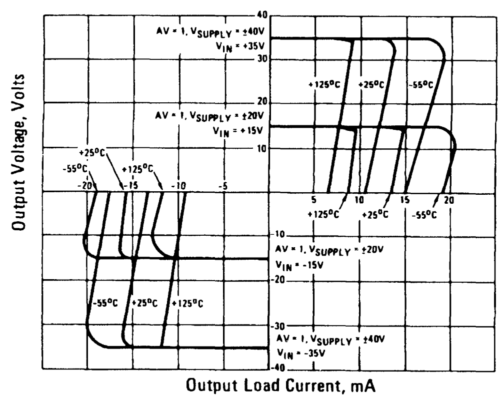


Figure 2. Output Current

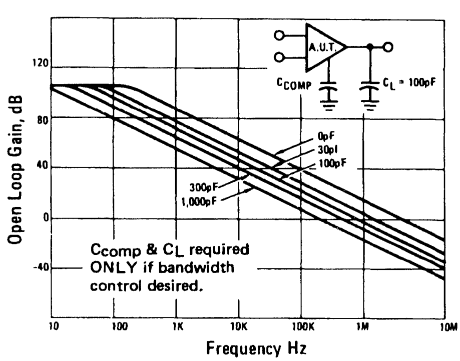


Figure 3. Gain vs Frequency vs Bandwidth Control Pin Capacity

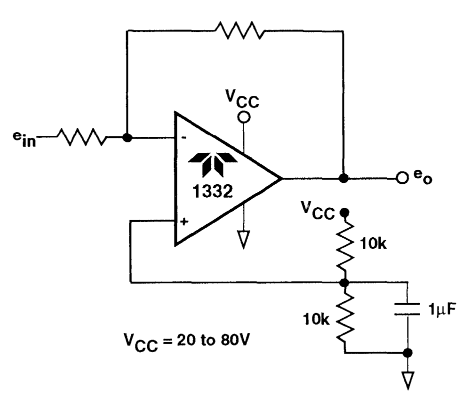


Figure 4. Single Supply Operation

NOTES

TELEDYNE COMPONENTS

MONOLITHIC WIDEBAND, JFET INPUT OPERATIONAL AMPLIFIER

FEATURES

- **Monolithic Construction**
- **Offset Voltage ....3mV Max**
- **Slew Rate 120V/µs**
- **Gain Bandwidth Product 100MHz**
- **Bias Current ....50pA Max**

APPLICATIONS

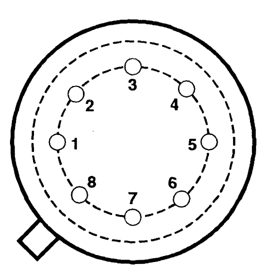
- **Pulse Amplifiers**
- **High Speed, Precision Integrators**
- **High Speed Track/Hold Amplifiers**
- **Video Amplifiers**

GENERAL DESCRIPTION

The 1344 Precision, High Speed Monolithic Operational Amplifier offers significant improvements in features vs other devices of its type. Stable with closed loop gains ≥ 10, the 1344 features 1 MHz full power bandwidth, 120V/µs slew rate and superior DC characteristics. It is ideal for high-speed data acquisition systems, precision pulse and video amplifiers and high speed buffers. Housed in an 8-pin TO-99 package, this device is specified for 0°C to +75°C temperature range.

PIN CONFIGURATION

Pin No.	Designation
1	NC
2	INVERTING INPUT
3	NON-INVERTING INPUT
4	$-V_{CC}$
5	NC
6	OUTPUT
7	$+V_{CC}$
8	COMPENSATION



BOTTOM VIEW

1344

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage .... ±20V
V_{IDF} Differential Input Voltage .... $\pm V_{CC}$
T_C Operating Temperature Range (Case) ....0°C to +75°C
T_{STG} Storage Temperature Range ......–65°C to +150°C
P_D Power Dissipation 675mW

ELECTRICAL CHARACTERISTICS: T_C = +25°C, V_{CC} = ±15V, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
I_B	Input Bias Current		—	±20	±50	pA
		T_{MIN} to T_{MAX}	—	±5	±10	nA
I_{OS}	Input Offset Current		—	±2	±10	pA
		T_{MIN} to T_{MAX}	—	±2	±5	nA
V_{OS}	Input Offset Voltage	Without External Trim	—	±1	±3	mV
		T_{MIN} to T_{MAX}	—	±3	±5	mV
$V_{OS}TC$	V_{OS} vs Temperature		—	±20	—	µV/°C
PSRR	Input Offset vs Power Supply	@ DC (Note 1)	74	86	—	dB
V_{ICM}	Common-Mode Input Voltage	DC Linear Operation	±10	±11	—	V
CMRR	Common-Mode Rejection Ratio	@ DC, V_{CM} = ±10V	74	80	—	dB
Z_{IDF}	Differential-Mode Input Impedance	@ DC	—	10^{12}	—	Ω
Output						
V_O	Output Voltage	R_L = 2 kΩ	±10	±11	—	V
I_O	Output Current		±10	±20	—	mA
Z_O	Output Impedance		—	50	—	Ω
Voltage Gain		R_L = 2 kΩ				
A_{OL}	Open-Loop Voltage Gain		97	104	—	dB
	Over Specified Temperature Range		95	100	—	dB
Frequency Response						
GBWP	Gain Bandwidth Product	A_V=10	—	100	—	MHz
UGBW	Unity-Gain Bandwidth		—	20	—	MHz
FPBW	Full-Power Bandwidth	R_L = 2kΩ	—	1.9	—	MHz
Time Response						
t_S	Settling Time	10V Step to 0.2%, A_{CL} = 10	—	280	—	ns
sr	Slew Rate		±100	±120	—	V/µs
t_R	Small Signal Rise Time		—	20	—	ns
Power Supplies						
V_{CC}	Power Supply Voltage		—	±15	—	V
I_{CC}	Quiescent Supply Current	V_{CC} = ±15V	—	±8	±10	mA

NOTES: 1. Specified over ±10V to ±20V supply range.

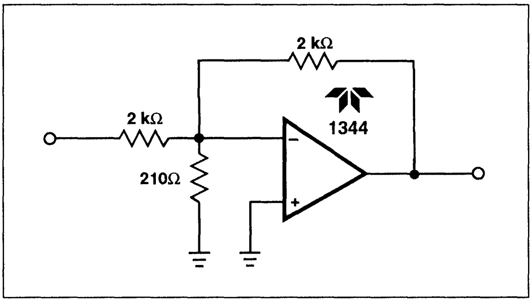


Figure 1. Fast-Settling Buffer

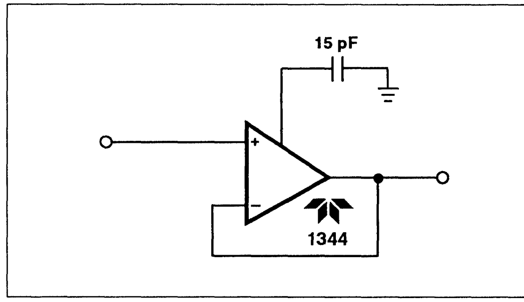


Figure 2. 20 MHz Voltage Follower

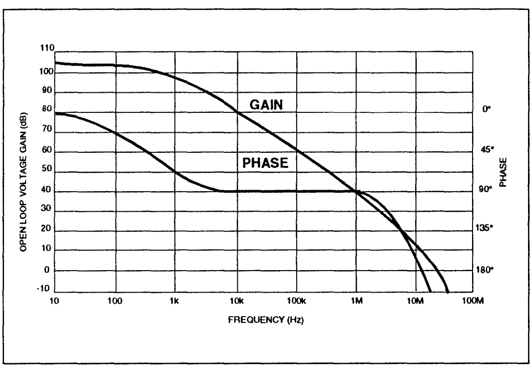


Figure 3. Open Loop Frequency Response

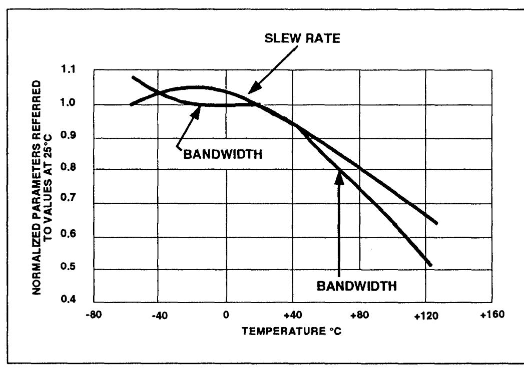


Figure 4. Normalized AC Parameters vs Temperature

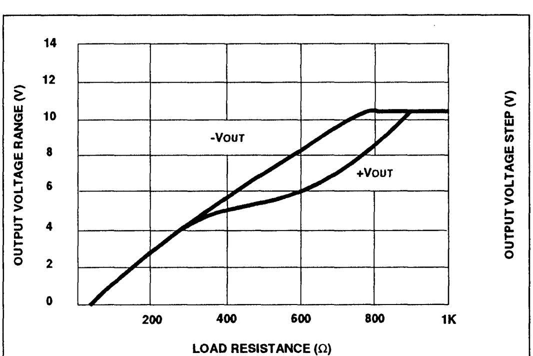


Figure 5. Output Voltage Swing vs Load Resistance

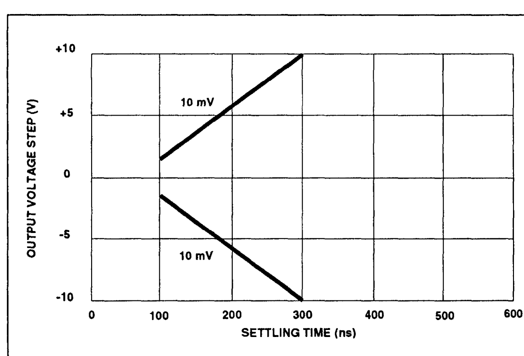


Figure 6. Settling Time for Various Output Step Voltages

9

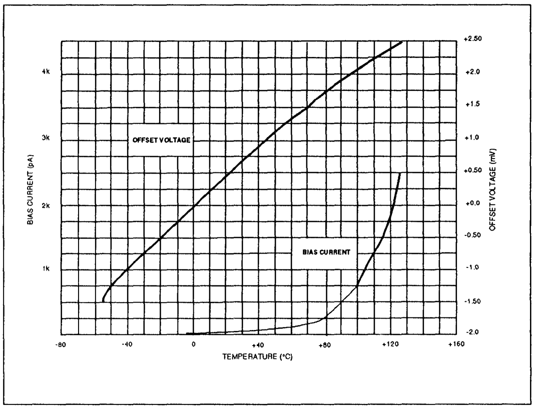


Figure 7. Input Offset Voltage and Bias Current vs Temperature

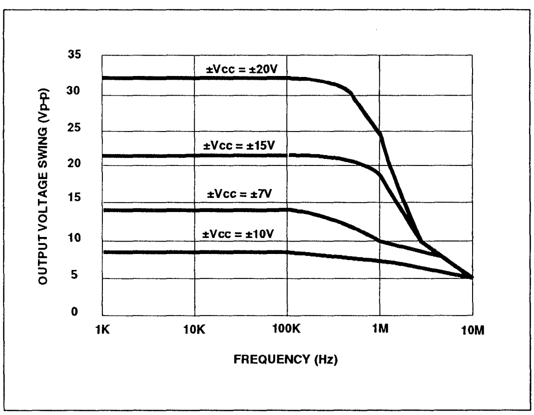


Figure 10. Output Voltage Swing vs Frequency

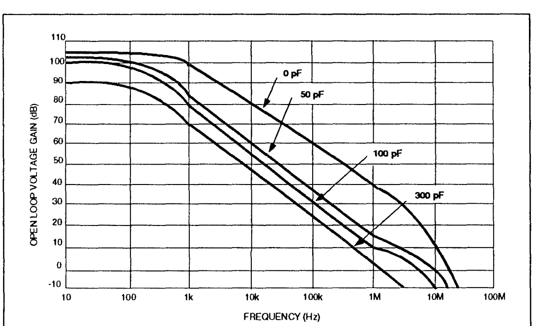


Figure 12. Open Loop Frequency Response For Various Bandwidth Control Capacitances

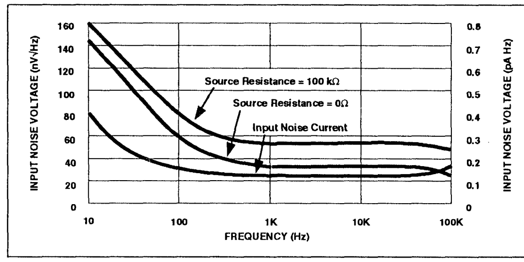


Figure 8. Input Noise Voltage and Noise Current vs Frequency

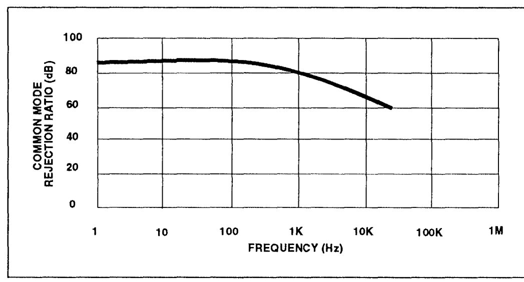


Figure 9. Common Mode Rejection Ratio vs Frequency

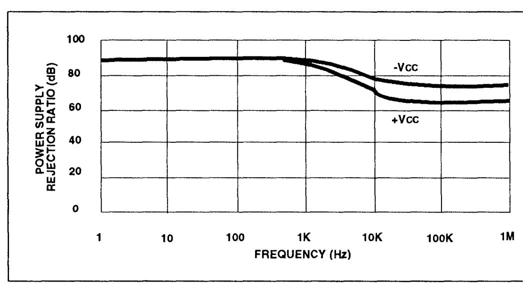


Figure 11. Power Supply Rejection Ratio vs Frequency

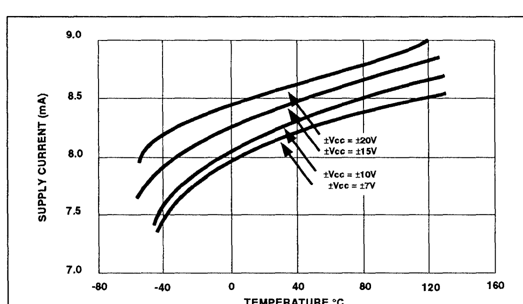


Figure 13. Power Supply Current vs Temperature

TELEDYNE COMPONENTS

MONOLITHIC LOW BIAS CURRENT OPERATIONAL AMPLIFIER

FEATURES

- **Unity Gain Bandwidth Product ....2 MHz**
- **Bias Current ....±250 fA**
- **Offset Voltage ....±3 mV Max**
- **Settling to ±0.1% ....2 µs**
- **Power Consumption ....30 mW Max**

APPLICATIONS

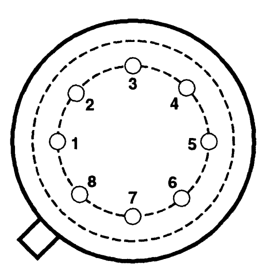
- **Track/Hold Amplifiers**
- **Electrometer Amplifiers**
- **Precision Amplifiers**

GENERAL DESCRIPTION

The 1346 High Performance, Monolithic Operational Amplifier combines JFET/Bipolar technology and dielectric isolation to provide the best AC and DC characteristics available in any monolithic device of its type. Specifications of 250 fA input bias current and 3 mV maximum offset voltage combined with 2 MHz unity gain bandwidth and 7V/µs slew rate make the 1346 ideal for such applications as high impedance, high performance buffers, precision track/hold amplifiers and long-term precision integrators. The 1346 is housed in an 8-pin TO-99 package.

PIN CONFIGURATION

Pin No.	Designation
1	TRIM
2	INVERTING INPUT
3	NON-INVERTING INPUT
4	$-V_{CC}$
5	TRIM
6	OUTPUT
7	$+V_{CC}$
8	CASE



BOTTOM VIEW

MONOLITHIC LOW BIAS CURRENT OPERATIONAL AMPLIFIER

1346

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply Voltage	±20V
V_{IDF}	Differential Input Voltage	$\pm V_{CC}$
T_C	Operating Temperature Range (Case) 1346	0°C to +75°C
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation	300mW

ELECTRICAL CHARACTERISTICS: T_C = +25°C, V_{CC} = ±15V, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
I_B	Input Bias Current		—	±0.25	±1	pA
		T_{MIN} to T_{MAX}	—	±6	±30	pA
I_{OS}	Input Offset Current		—	±0.03	±0.2	pA
		T_{MIN} to T_{MAX}	—	±1	±5	pA
V_{OS}	Input Offset Voltage	Without External Trim	—	±1	±3	mV
		T_{MIN} to T_{MAX}	—	—	±4	mV
PSRR	Input Offset vs Power Supply	@ DC, V_{CC} = ±10V to ±20V	85	105	—	dB
V_{ICM}	Common-Mode Input Voltage	DC Linear Operation	±10	±12	—	V
CMRR	Common-Mode Rejection Ratio	@ DC	90	110	—	dB
Z_{ID}	Differential Input Impedance	@ DC	—	1	—	GΩ
Output						
V_O	Output Voltage	R_L = 2 kΩ	±10	±12	—	V
I_O	Output Current		±10	±15	—	mA
I_{OSC}	Output Short Circuit Current		—	(Note 1)	—	—
Z_O	Output Impedance		—	25	—	Ω
Voltage Gain						
A_{OL}	Open-Loop Voltage Gain	R_L = 2kΩ	106	120	—	dB
		T_{MIN} to T_{MAX}	103	—	—	dB
Frequency Response						
UGBW	Unity-Gain Bandwidth		—	2	—	MHz
FPBW	Full-Power Bandwidth	R_L = 2kΩ	—	110	—	kHz
Time Response						
t_S	Settling Time	10V Step to 0.1%	—	2	—	µs
sr	Slew Rate		±4	±7	—	V/µs
t_R	Small Signal Rise Time		—	75	—	ns
Power Supplies						
V_{CC}	Power Supply Voltage		—	±15	±20	V
I_{CC}	Quiescent Supply Current	V_{CC} = ±15V	—	±0.8	±1	mA

Note 1: Output can withstand a short to ground for an indefinite length of time. Shorts to either supply will result in destruction.

MONOLITHIC
LOW BIAS CURRENT
OPERATIONAL AMPLIFIER

Applications Information

The 1346 is one of the lowest input bias current monolithic operational amplifiers available. When used in applications requiring maximum performance, precautions must be taken against unwanted noise and leakage current. To minimize leakage currents a teflon socket is recommended. Bypass capacitors should be as near as possible to the unit and the unit should be as near as possible to the signal source. The dielectric isolation process and JFET input design protect the 1346 against input signal transients beyond the level of the supplies as well as large differential signals equal to the differential supply voltage without degradation of performance.

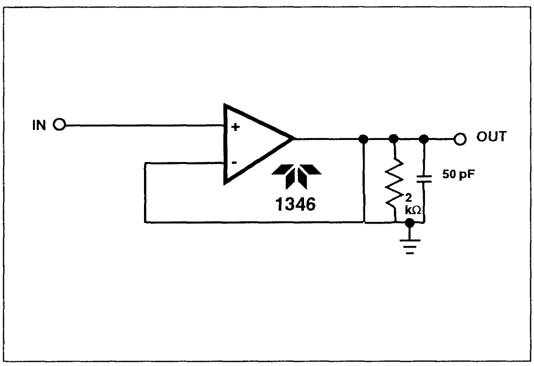


Figure 1. Slew Rate and Transient Response

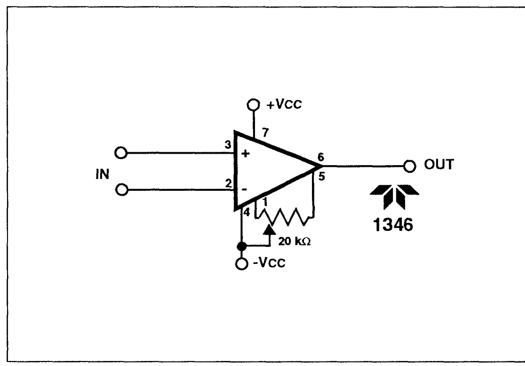


Figure 2. Suggested Offset Adjustment Circuit

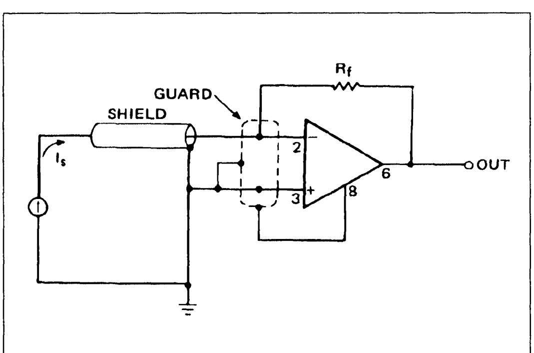


Figure 3. Current to Voltage Converter

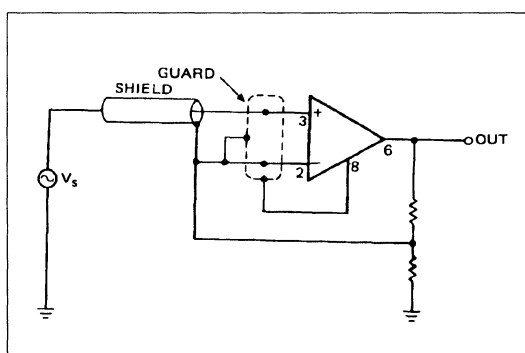


Figure 4. Very High Impedance Noninverting Amplifier

NOTES

TELEDYNE COMPONENTS

1430

FAST SETTLING, FET INPUT OPERATIONAL AMPLIFIER

FEATURES

- **Settling Time to ±0.01% (10V step)........200 ns Max**
- **Operating Temperature...................-55°C to +125°C**
- **Gain Bandwidth Product...........................100 MHz**
- **Slew Rate..750V/µs**
- **Output ....±11V, ±55 mA**

APPLICATIONS

- **Digital-to-Analog Converters**
- **Sample/Hold Circuits**
- **Pulse Amplifiers**
- **Wideband Amplifiers**

GENERAL DESCRIPTION

The 1430 is a high speed, precision, FET input hybrid op amp that features fast settling time, low bias current, high slew rate, wide bandwidth, and good phase margin. Guaranteed settling time of 200nsec (10V step to 0.01%) and a design that is tailored for inverting applications make the 1430 an ideal output amplifier for fast 12 bit D/A converters and other applications such as sample-hold amplifiers and radar pulse amplifiers.

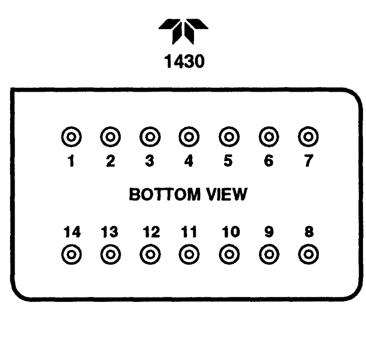
The 1430 was carefully designed so that output settling time would not vary appreciably with closed loop gain (Figure 1). This is particularly important for current to voltage converter applications as with high speed current-output DACs (see Figure 2). The 1430 requires only a feedback capacitor for stability at closed-loop gains of unity and above.

The 1430 is packaged in a 14-pin metal platform package. Both the standard 1430 and the High Reliability (HR) 1430 are specified to operate over the -55°C to +125°C temperature range.

9

PIN CONFIGURATION

Pin No.	Designation
1	NC
2	TRIM
3	TRIM
4	-IN
5	+IN
6	$-V_{CC}$
7	NC
8	COM
9	NC
10	OUTPUT
11	$+V_{CC}$
12	TRIM
13	NC
14	NC



1430

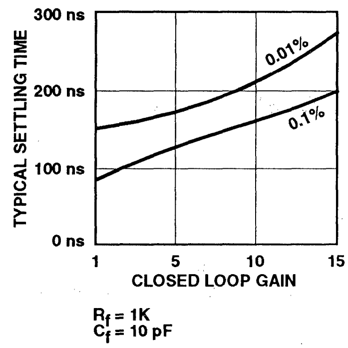


Figure 1. Settling Time vs Closed Loop Gain

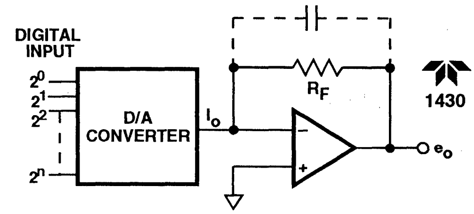


Figure 2. Output Amplifier for D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage ....±18V
V_{ID} Differential Input Voltage ....±V_{CC}
V_{ICM} Common Mode Input Voltage.......................±V_{CC}
T_C Operating Temperature Range (Case)
1430 ....-55°C to +125°C
1430-HR ....-55°C to +125°C (1)

T_{STG} Storage Temperature Range......–65°C to +150°C
(1) Operation above 85°C requires a 20°C/W heat sink.

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, inverting circuits only, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1430 Min	1430 Typ	1430 Max	1430-HR Min	1430-HR Typ	1430-HR Max	Unit
V_{OS}	Input Offset Voltage		—	±0.5	**±2**	—	±0.5	**±2**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±40	—	—	±40	**±100**	µV/°C
I_B	Input Bias Current		—	±10	**±100**	—	±10	**±100**	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±2	—	—	±2	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain	R_L = 200Ω	**106**	120	—	**106**	120	—	dB
PSRR	Power Supply Rejection Ratio		—	80	—	—	80	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±2V	—	65	—	—	65	—	dB
CMR	Common-Mode Range (DC Linear Operation)		—	+3/-10	—	—	+3/-10	—	V
Z_{ID}	Differential Input Impedance		—	$10^{11} \| 3$	—	—	$10^{11} \| 3$	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	$10^{11} \| 3$	—	—	$10^{11} \| 3$	—	Ω‖pF
V_O	Output Voltage Swing	R_L = 200Ω	**±10**	±11	—	**±10**	±11	—	V
I_O	Output Current	R_L = 200Ω	**±50**	±55	—	**±50**	±55	—	mA
I_{SC}	Output Short-Circuit Current		—	±110	—	—	±110	—	mA
R_O	Output Resistance (DC Open-Loop)		—	1000	—	—	1000	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±10	±15	±18	±10	±15	±18	V
I_{CC}	Quiescent Supply Current		—	±20	**±25**	—	±20	**±25**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

FAST SETTLING, FET INPUT OPERATIONAL AMPLIFIER

AC CHARACTERISTICS: (Note 1) $V_{CC} = \pm 15V$, $R_L = 1\ k\Omega$, inverting circuits only, $T_C = 25°C$, unless otherwise noted.

			1430			1430-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
S_R	Slew Rate		—	750	—	—	750	—	V/µs
GBWP	Gain-Bandwidth Product	f = 1 MHz	80	100	—	80	100	—	MHz
UGBW	Unity-Gain Bandwidth		—	60	—	—	60	—	MHz
t_s	Settling Time (A_{CL} = -1)	10V step/1%	—	70	—	—	70	—	ns
		10V step/0.1%	—	85	—	—	85	—	ns
		10V step/0.01%	—	175	200	—	175	200	ns
		5V step/1%	—	70	—	—	70	—	ns
		5V step/0.1%	—	100	—	—	100	—	ns
		5V step/0.01%	—	180	—	—	180	—	ns
		2V step/1%	—	80	—	—	80	—	ns
		2V step/0.1%	—	100	—	—	100	—	ns
		2V step/0.01%	—	240	—	—	240	—	ns
e_n	Input Voltage Noise Density	f = 1 kHz	—	16	—	—	16	—	nV/√Hz
i_n	Input Current Noise Density	f = 1 kHz	—	0.2	—	—	0.2	—	pA/√Hz
C_L	Capacitive Load (maximum w/o oscillation)		100	—	—	100	—	—	pF

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

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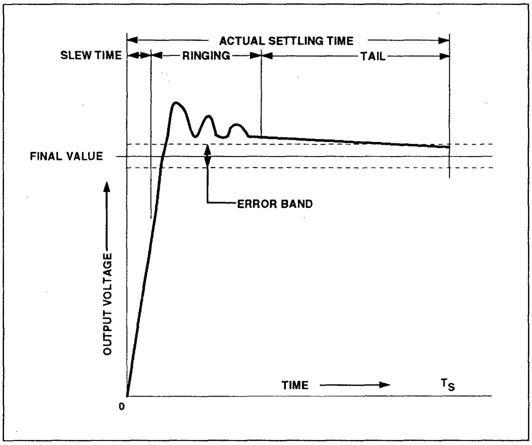


Figure 3. The Composition of Settling Time

Defining Settling Time

Settling time is the important specification when handling fast (sub-microsecond rise time), precision (0.1% or better amplitude accuracy) pulses. Settling time is the total time required, after the application of an input step (voltage or current), for a circuit's output to reach and stay within an error band specified in relation to the output's final value (see Figure 3).

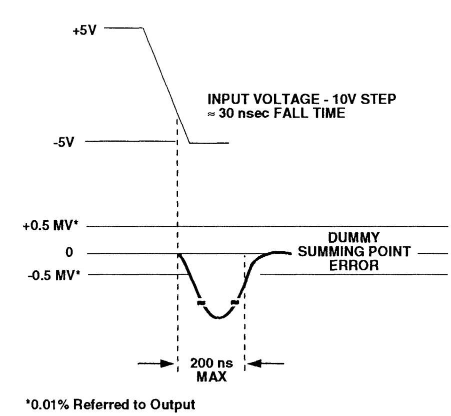
Settling time cannot be predicted from bandwidth or slew rate. A step input to the amplifier will cause the output to slew at its maximum rate toward the final value. When this value is reached the output will usually overshoot slightly and "ring" as it settles toward the final value. Settling time includes not only the slew rate but also that portion of the ringing time in which the peaks exceed the settling time error band.

The error band is generally expressed as a percentage of the op-amps full scale output (i.e. 0.01% or 1 mV for a 10V amplifier). When observing settling time on an oscilloscope the amplifier may appear to have settled because the ringing has ceased but the observed value is outside the error band for a few seconds until it drifts within the error band. This "long tail" phenomenon is often a source of error. The long tail makes it virtually impossible to calculate settling time by using slew rate, and ringing characteristics as the sole factors. Also, knowing the settling time to a given accuracy (i.e. 0.1%) is not helpful in extrapolating the settling time to a higher accuracy, such as 0.01% and vice versa.

If settling time cannot be extrapolated, calculated, guessed or ignored, it must be measured. This can be difficult and misleading if the proper procedures are not followed precisely. (Figure 4 illustrates the 1430's settling characteristics using the test circuit shown in Figure 5A).

Measuring Settling Time

It is not possible to obtain 0.1% or 0.01% accurate measurements directly from an oscilloscope looking at the output waveform. Measuring a 10V signal, at high sensitivity for proper resolution, will overdrive the scope's input amplifier such that it's own recovery time will be much longer than the settling time being measured. Measuring settling time to 0.01% requires a clipping amplifier to prevent overloading the oscilloscope's input (Figure 5B).



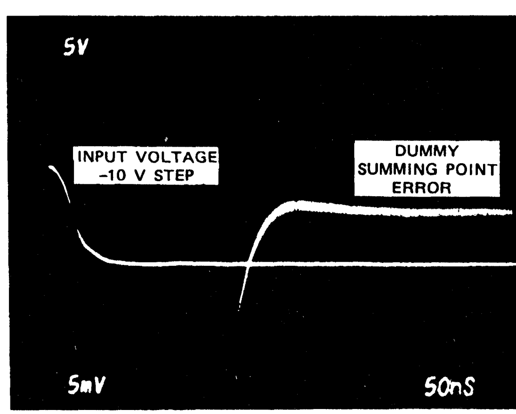


Figure 4. 1430/1430-HR Settling Time

Figure 5. Test Circuit and Clipping Amplifier

FAST SETTLING, FET INPUT OPERATIONAL AMPLIFIER

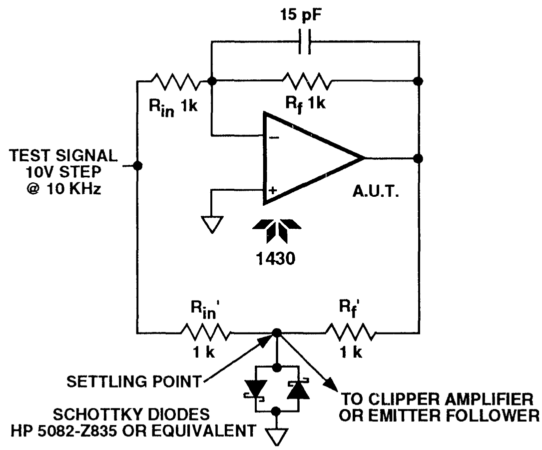


Figure 5A. Test Circuit

The test circuit (Figure 5A) is an excellent method for fast-settling time measurements. In this circuit R_{in} and R_f are matched to R_{in}' and R_f'. When the Amplifier Under Test (AUT) settles to ±0.01% of a 20V step (±2 mV) the settling point settles to ±1 mV. A FET follower with less than 1 pF input capacitance (3N128) is used in the clipper amp to buffer the settling point. The two schottky diodes acting as limiters on the settling point do not store a charge nor present much capacitive loading. Therefore, the lag due to capacitance, ≈3 pF, in combination with $R_f' = R_i' = 1\ k\Omega$ can be as low as 1.5 ns. Be sure to use an ideal square wave source for testing, since a square wave with significant ripple can unfairly cause an amplifier to look bad.

This method allows you to look directly at the true AUT output, yet avoids most drawbacks due to the output signal subtraction from the input signal.

Why not connect the 3N128 buffer directly to the summing point? Because of feedback capacitance, C_f, and the (A.U.T.) input capacitance, C_{in}. Many fast-settling amplifiers give best results when some finite amount of feedback capacitance is used. The effect of changing C_f can be seen at the settling point but not at the summing point. In addition, some good amplifiers have significant input capacitance due to "Miller capacitance" or feedforward capacitors. In this case, it is possible to see the true settling only at the settling point. You can test at the summing point if the result is the same as at the settling point; but if there is a difference measure at the settling point.

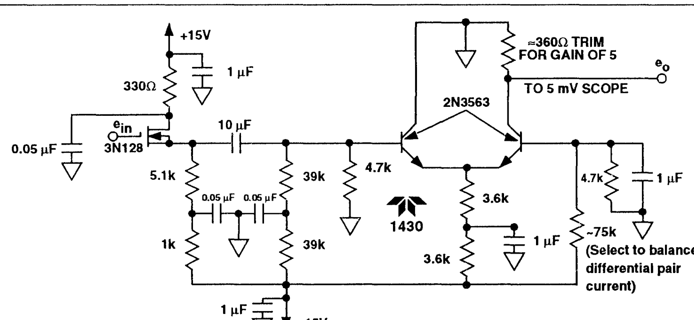


Figure 5B. Clipping Amplifier

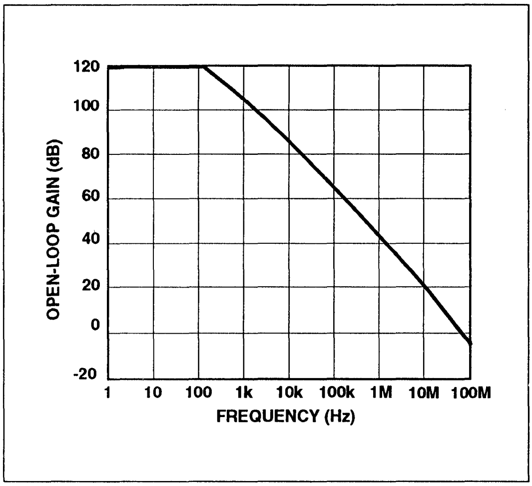


Figure 6. Open-Loop Gain vs Frequency

An amplifier is of little use in precision work if it's output for a 400ns pulse rises in 10ns, overshoots 20%, rings for 100ns, and, due to a tail does not arrive at and remain within 0.01% of the final value for another 600ns. A 1430 will be within 0.01% of final value within 200ns.

To operate the 1430 or 1430-HR from +85°C to +125°C, a 20°C per watt heat sink must be attached. A suggested device is the Thermalloy Model 6007A* modified by removing the two fins at each end and adding an aluminum "hold down bar" (Figure 7). Heat sink compound must be used between the 1430 and the heat sink.

*Thermalloy
2021 West Valley View Lane
Dallas, TX 75234

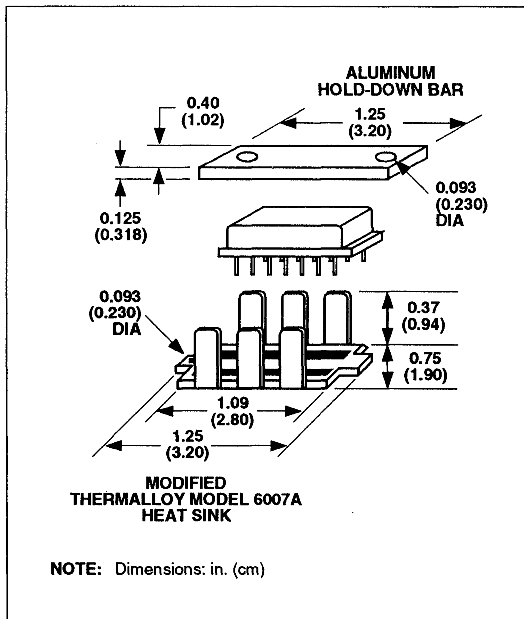


Figure 7. Heat Sink Assembly

OPERATIONAL AMPLIFIER — HIGH-FREQUENCY, FAST-SETTLING

FEATURES

- **Settling Time to 0.01% .... 70 ns**
- **Gain Bandwidth Product .... 1 GHz**
- **Common-Mode Rejection Ratio .... 100 dB**
- **Open-Loop Gain .... 95 dB**
- **Operating Temperature (-HR) .... –55°C to +125°C**

APPLICATIONS

- **Radar and Sonar Signal Processing**
- **Microwave Transmitter Modulators**
- **Graphic CRT Displays**
- **Linear Video Mixers**
- **Video ADCs, DACs, S/Hs**

GENERAL DESCRIPTION

The 1435 is an ultra-fast, differential-input operational amplifier designed for precision amplification of wideband, complex waveforms with frequency components from DC to 100 MHz. Such performance is made possible by a unique design featuring high open-loop gain, flat frequency response beyond 10 kHz, and smooth 6 dB/octave rolloff to greater than 100 MHz.

Applications of the 1435 are based on using the precision capabilities of a differential-input op amp at higher frequencies than previously possible. These applications include video mixers with 20 dB to 40 dB gain, fully-differential-input, and 0.1% gain stability; peak detectors (and sample/holds) that can capture 10V, 50 ns pulses to 1% accuracy and 70 ns pulses to 0.01% accuracy; video A/D and D/A converters; submicrosecond, precision analog comparators.

The standard 1435 is specified for 0°C to +70°C operation. For high-reliability military/aerospace applications, the 1435 High Reliability (HR) version is specified for –55°C to +125°C operation.

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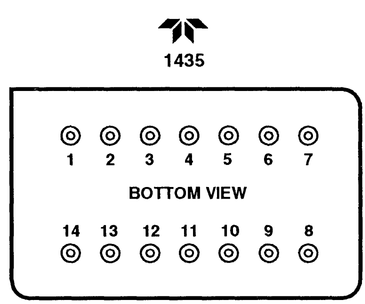
PIN CONFIGURATION

PIN NO.	DESIGNATION	PIN NO.	DESIGNATION
1	OPTIONAL BYPASS CAPACITOR	8	+INPUT
2	OUTPUT SOURCE	9	NC
3	COMPENSATION CAPACITOR	10	NC
4	$+V_{CC}$	11	NC
5	E_{OS} TRIM	12	$-V_{CC}$
6	E_{OS} TRIM	13	OUTPUT SINK
7	–INPUT	14	CASE COMMON

NC = NO INTERNAL CONNECTION



1435

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply Voltage	±18V
V_{ID}	Differential Input Voltage	±4V
V_{ICM}	Common-Mode Input Voltage	±10V
T_C	Operating Temperature Range (Case)	
	1435	0°C to +70°C
	1435-HR	–55°C to +125°C
T_{STG}	Storage Temperature Range	–65°C to +150°C

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 500Ω, T_C = 25°C, unless otherwise noted.

			1435			1435-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage		—	±2	**±5**	—	±2	**±5**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±5	—	—	±5	**±25**	μV/°C
I_B	Input Bias Current		—	±10	**±30**	—	±10	**±30**	μA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±50	—	—	±50	**±150**	nA/°C
I_{OS}	Input Offset Current		—	±0.3	—	—	±0.3	—	μA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±2	—	—	±2	—	nA/°C
A_{VOL}	Open-Loop Voltage Gain		**80**	95	—	**80**	95	—	dB
PSRR	Power Supply Rejection Ratio		—	86	—	—	86	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±5V	**80**	100	—	**80**	100	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 74 dB	**±7**	±8.5	—	**±7**	±8.5	—	V
Z_{ID}	Differential Input Impedance		—	2.5k‖2	—	—	2.5k‖2	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	1M‖2	—	—	1M‖2	—	Ω‖pF
V_O	Output Voltage Swing		**±5**	±7	—	**±5**	±7	—	V
I_O	Output Current		**±10**	±14	—	**±10**	±14	—	mA
I_{SC}	Output Short-Circuit Current		—	-16/+35	—	—	-16/+35	—	mA
R_O	Output Resistance (DC Open-Loop)		—	100	—	—	100	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±12	±15	±16	±12	±15	±16	V
I_{CC}	Quiescent Supply Current		—	±25	**±30**	—	±25	**±30**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, C_C = 2 pF, T_C = 25°C, unless otherwise noted.

			1435			1435-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
S_R	Slew Rate	C_C = 0	250	300	—	250	300	—	V/μs
GBWP	Gain-Bandwidth Product	f = 10 MHz, C_C = 0	700	1000	—	700	1000	—	MHz
UGBW	Unity-Gain Bandwidth	C_C = 0	—	150	—	—	150	—	MHz
t_s	Settling Time (A_{CL} = -1)	10V step/0.025%	—	60	85	—	60	75	ns
		10V step/0.01%	—	70	—	—	70	—	ns
		5V step/1%	—	25	—	—	25	—	ns
		5V step/0.1%	—	40	60	—	40	60	ns
		1V step/1%	—	10	—	—	10	—	ns
		1V step/0.1%	—	20	—	—	20	—	ns
e_n	Input Voltage Noise Density	f = 1 kHz	—	16	—	—	16	—	nV/√Hz
i_n	Input Current Noise Density	f = 1 kHz	—	25	—	—	25	—	pA/√Hz
C_L	Capacitive Load (Maximum w/o oscillation)	NG > 2, C_C = 3 pF	1000	—	—	1000	—	—	pF

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

HIGH-FREQUENCY, FAST-SETTLING OPERATIONAL AMPLIFIER

APPLICATION INFORMATION

Basic Connections and Wiring Techniques

A schematic and suggested physical layout of basic connections for the 1435 are shown in Figure 1. Illustrated are wiring techniques recommended to obtain specified high frequency/time response from the 1435. The circuit should be built on a ground plane with minimum length, point-to-point connections, wired directly to the pins of the 1435. If a socket is necessary, it should be made of Teflon (such as the Augat model 114-AG-2A). Remember, 1000Ω and 10 pF provide a time constant of 10 ns.

The 1435 has a Class A output stage. Pin 2 is a follower output, while pin 13 is a current sink used to provide quiescent bias for the follower, as well as sinking load current for negative output swings. For most applications, pins 2 and 13 (the output circuit) are connected together.

Stability and Compensation

The 1435 operates in any conventional op-amp circuits, including the noninverting amplifier, current-to-voltage converter, integrator, etc. However, it must be used at a noise gain of at least 2 (noise gain = $1 + R_F/R_{IN}$). For example, it can operate as a gain-of-one inverter (Figure 1), or differential amplifier, but as a non-inverting amplifier, it must have a gain of at least 2.

Capacitor C_1 (shown in Figure 1), is a 2 pF compensation capacitor which must be used to maintain stable operation when noise gain is less than 10.

Resistor R_3 connected to the (+) input compensates for the (–) input bias current. It should be equal to R_{IN} and R_F in parallel. The 1 kΩ, E_{OS} adjust potentiometer is optional. The 1 µF bypass capacitor (C_2) on pin 1 may be necessary to prevent oscillation of the output stage when driving capacitive loads.

When operating at the low impedances required by the 1435, care should be taken to include the load provided by the feedback resistor when calculating the total load on amplifier output.

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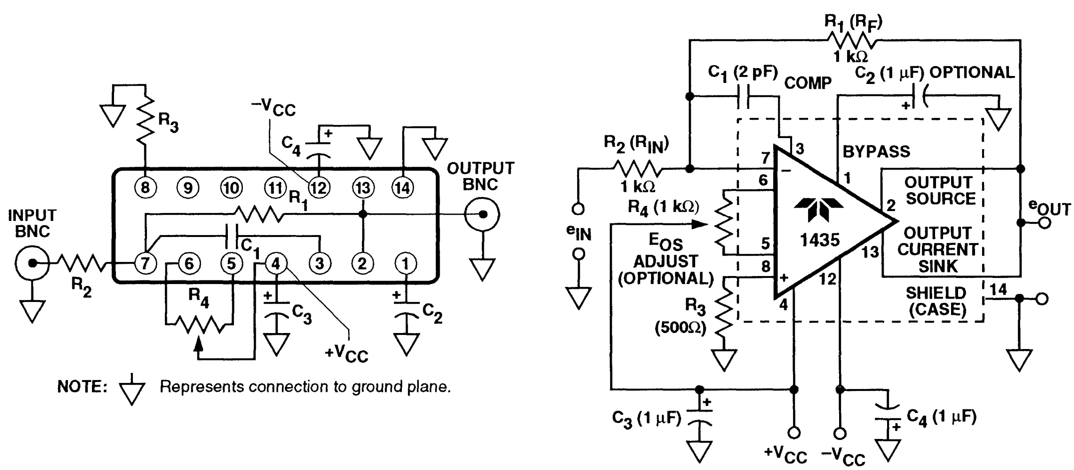


NOTES: 1. $R_3 = \frac{(R_F)(R_{IN})}{R_F + R_{IN}}$ bias current compensation.

2. 1 µF bypass capacitors should be solid tantalum.

3. Pins 9, 10, 11 = no connection

Figure 1. Suggested Layout and Schematic

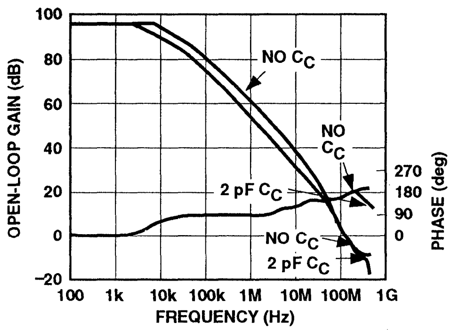
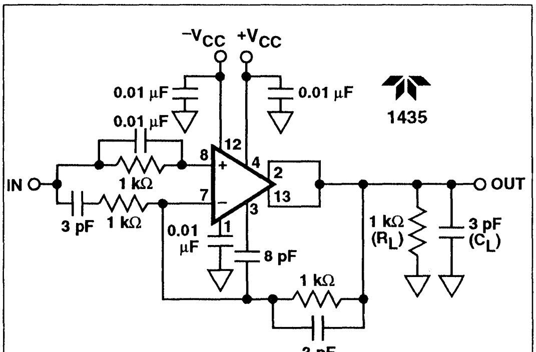


Figure 2. Open-Loop Gain and Phase vs Frequency

Operation as a Follower

When operated as a follower, the 1435 requires a noise gain of at least 2 for stability. Figure 3 shows one method of obtaining a noise gain of 2.



NOTE: ZI = 2.3 pF $f_I < 30$ MHz
1.5 pF, 30 MHz < f_I < 100 MHz
230Ω $f_I < 150$ MHz
f_{FP} (10 V_{P-P}) = 9 MHz (full-power bandwidth)

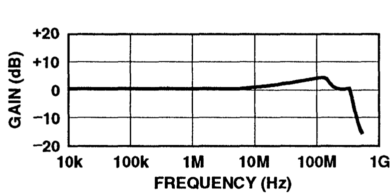
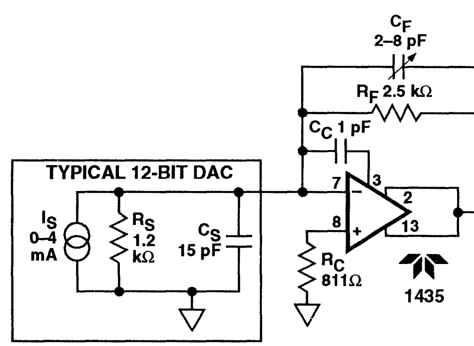


Figure 3. The 1435 as High Impedance Input Follower

Operation as a Current-to-Voltage Converter

The 1435 is an optimum choice for a current-to-voltage converter because of its excellent E_{OS} and I_{OS} temperature coefficients (TC). When used with a current output DAC the required noise gain of ≥2 is provided by using the output impedance of the DAC (see Figure 4). The initial input bias current of the 1435 is compensated by the addition of R_C, which is equal to the parallel combination of the feedback resistor and the input (DAC output) impedance. The typical I_{OS} TC of 2 nA/°C times the feedback resistor (2.5 kΩ) produces 5 µV/°C of output drift over temperature, and the typical E_{OS} TC of 5 µV/°C times a noise gain of 3.1 contributes only 15.5 µV/°C to the output drift.



$R_C = R_F \| R_S$
$NG = 1 + R_F/R_S$

NOTES: 1. TC = contributions: E_{OS} TC χ NG = 15.5 µV/°C
I_{OS} TC χ R_F = 5 µV/°C
2. Average overall output drift= 20.5 µV/°C

Figure 4. The 1435 as a Fast Current-to-Voltage Converter

Settling-Time Measurement

The measurement of amplifier settling time to 0.01% under 100 ns accuracy requires great care. The 1435's settling time may be measured using the circuit shown in Figure 5. The settling-time test point is connected to an emitter-follower buffer for 0.1% measurement and to a gain-of-5 amplifier for 0.01%. (For a detailed discussion of these measurement techniques, see Teledyne Components' Model 1430 data sheet.)

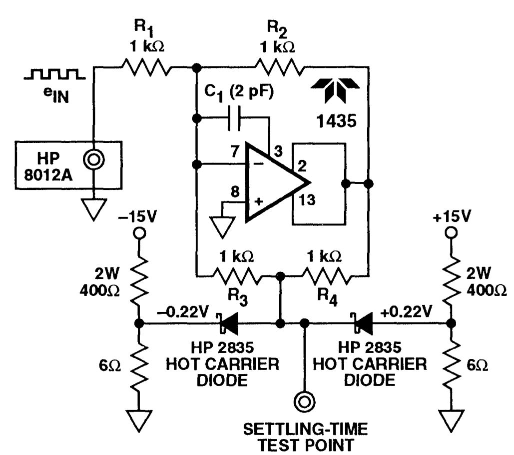


Figure 5. Settling-Time Test Circuit

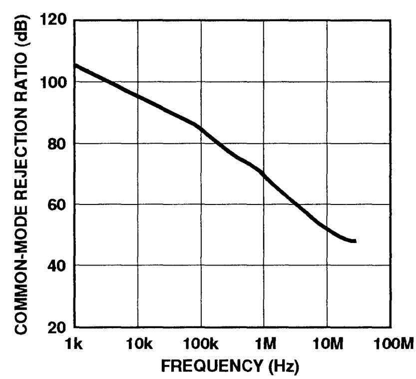


Figure 6. CMRR vs Frequency

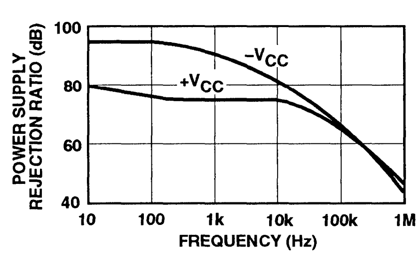


Figure 7. PSRR vs Frequency

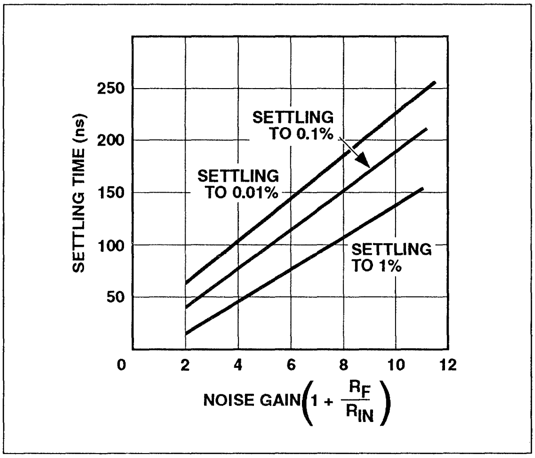


Figure 8. Typical Settling Time vs Noise Gain

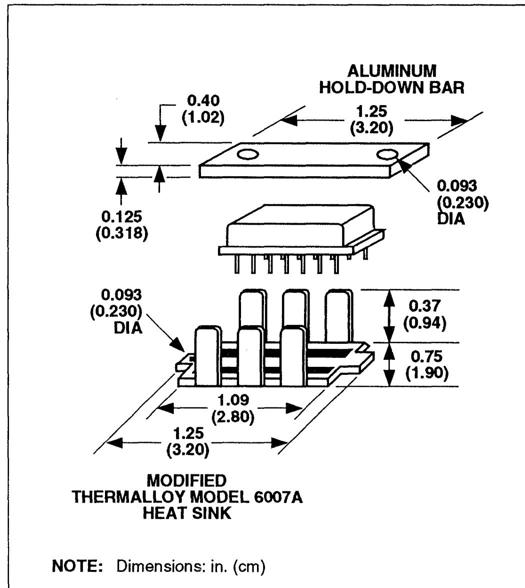


Figure 9. 1435-HR Heat Sink Assembly

CMRR/PSRR vs Frequency

Figure 6 plots CMRR versus frequency, illustrating that the 1435 is fully differential at video frequencies and is an excellent choice for differential and non-inverting applications.

Figure 7 plots PSRR versus frequency, and illustrates the need to bypass the power supplies at video frequencies (to prevent oscillation).

Settling Time vs Noise Gain

The dependency of the 1435's dynamic performance on circuit gain is shown in Figure 8. Because of the enormous gain bandwidth of the 1435, settling time remains good even with significant gain.

Operation Above +85°C

In order to operate the 1435-HR from +85°C to +125°C, it must be used with a 18°C/W heat sink. A suggested heat sink is the Thermalloy Model 6007A* (modified by removing the two fins at each end and adding the aluminum hold-down bar, as shown in Figure 10.) Heat-sink compound must be used between the 1435-HR and the heat sink.

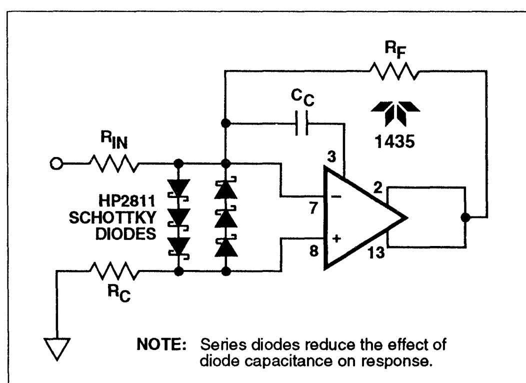


Figure 10. Input Protection

* To obtain the heat sinks mentioned here, please contact:

Thermalloy
2021 West Valley View Lane
Dallas, TX 75234

WARNING

If $-V_{CC}$ is open, the output will follow $+V_{CC}$. Depending on the feedback network, this may cause an input differential voltage greater than ±4V, which will degrade the input transistors. To maximize frequency response, the 1435 DOES NOT have input protection. Therefore, the following precautions MUST be taken:

1. Do not apply $+V_{CC}$ before $-V_{CC}$.
2. Do not apply voltage to either input (pins 7 and 8) prior to application of $\pm V_{CC}$.
3. Provide input protection per Figure 10.

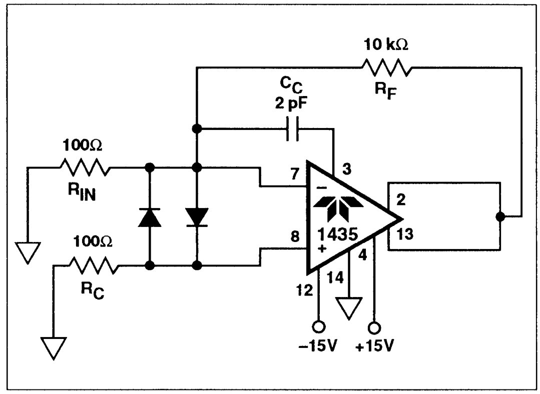


Figure 11. Burn-in Circuit

NOTES

OPERATIONAL AMPLIFIER — WIDEBAND, FAST-SETTLING

FEATURES

- **Gain Bandwidth Product .... 350 MHz**
- **Unity Gain Bandwidth .... 40 MHz**
- **Settling Time to 0.1% (10V step) .... 85 ns**
- **Output .... ±12V, ±24 mA**
- **Small, TO-99 Package**
- **Single External Compensation Capacitor**
- **FET Input**

APPLICATIONS

- **Current-to-Voltage DACs**
- **Pulse Amplifiers**
- **Radar and Sonar Signal Processing**
- **Graphics CRT Displays**
- **Video ADCs, DACs, and S/Hs**

GENERAL DESCRIPTION

The 1437 hybrid op amp offers versatility in wideband steady-state and fast-transient applications. It stands out for speed and predictability, as exemplified by its fast, smooth settling. The absence of large transients and oscillations in the settling waveform make the 1437 a dependable system element that can resolve settling problems associated with ADCs, DACs, and sampling circuits.

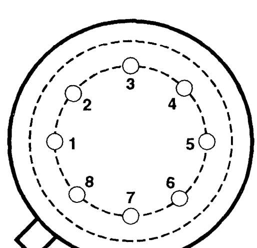
The 1437 has excellent DC characteristics: ±200 pA input bias current, 95 dB open-loop gain, and ±0.5 mV input offset voltage. The choice of a single external compensation capacitor ensures a 40 MHz bandwidth at a variety of gains. True differential inputs ensure superior performance in all circuit configurations: inverting, noninverting, or differential. With an attractive price/performance ratio, the 1437 is an industry-standard for high-speed, high-accuracy signal processing and data acquisition.

The 1437 is packaged in an 8-pin TO-99 can and is specified for 0°C to +70°C operation. The 1437 High Reliability (HR) version is specified for –55°C to +125°C operation.

9

PIN CONFIGURATION

PIN NO.	DESIGNATION
1	OFFSET TRIM
2	INVERTING INPUT
3	NONINVERTING INPUT
4	$-V_{CC}$
5	OFFSET TRIM
6	OUTPUT
7	$+V_{CC}$
8	COMPENSATION



BOTTOM VIEW

1437

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage .... ±20V
V_{ID} Differential Input Voltage .... ±25V
V_{ICM} Common-Mode Input Voltage .... $\pm V_{CC}$
T_C Operating Temperature Range (Case)
1437 .... 0°C to +70°C
1437-HR .... –55°C to +125°C
T_{STG} Storage Temperature Range ...... –65°C to +150°C
θ_{JC} Overall Junction-to-Case Thermal Resistance (Note 1) .... 32°C/W
θ_{JC} Output Transistor Junction-to-Case Thermal Resistance (Note 2) .... 65°C/W

NOTES: 1. Overall thermal resistance during normal operating conditions. Multiply this value by the power dissipation of the entire 1437 to determine maximum temperature rise case to junction in the hybrid.
2. Individual thermal resistance of the output stage. The 1437 is a Class AB amplifier. To calculate the output transistor temperature rise case to junction, multiply this figure by the power dissipation of the output transistor. At AC frequencies above 100 Hz, the effective thermal resistance of the output stage will drop 32.5°C/W for the 1437.

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 500Ω, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1437 Min	1437 Typ	1437 Max	1437-HR Min	1437-HR Typ	1437-HR Max	Unit
V_{OS}	Input Offset Voltage		—	±0.5	**±2**	—	±0.5	**±2**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±15	—	—	±15	**±50**	μV/°C
I_B	Input Bias Current		—	±200	—	—	±200	—	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±20	—	—	±20	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain		**88**	95	—	**88**	95	—	dB
PSRR	Power Supply Rejection Ratio		—	76	—	—	76	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±8V	**60**	78	—	**60**	78	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 54 dB	**±10**	±12	—	**±10**	±12	—	V
Z_{ID}	Differential Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
V_O	Output Voltage Swing		**±10**	±12	—	**±10**	±12	—	V
I_O	Output Current		**±20**	±24	—	**±20**	±24	—	mA
I_{SC}	Output Short-Circuit Current		—	±50	—	—	±50	—	mA
R_O	Output Resistance (DC Open-Loop)		—	90	—	—	90	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±12	±15	±20	±12	±15	±20	V
I_{CC}	Quiescent Supply Current		—	±12	**±15**	—	±12	**±15**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

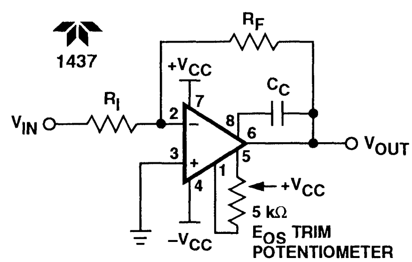
AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 500Ω, C_C = 0 pF, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1437 Min	1437 Typ	1437 Max	1437-HR Min	1437-HR Typ	1437-HR Max	Unit
S_R	Slew Rate		—	400	—	—	400	—	V/μs
		C_C =15 pF	—	225	—	—	225	—	V/μs
GBWP	Gain-Bandwidth Product	f = 10 MHz	—	350	—	—	350	—	MHz
UGBW	Unity-Gain Bandwidth	C_C = 27 pF	—	40	—	—	40	—	MHz
t_s	Settling Time (A_{CL} = -1, C_C = 15 pF)	10V step/1%	—	65	—	—	65	—	ns
		10V step/0.1%	—	85	120	—	85	120	ns
		10V step/0.025%	—	150	—	—	150	—	ns
		10V step/0.01%	—	180	—	—	180	—	ns
e_n	Input Voltage Noise Density	f = 1 kHz	—	10	—	—	10	—	nV√Hz

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

APPLICATIONS

The basic connections for the 1437 in the inverting mode are shown in Figure 1.



NOTES: An E_{OS} trim potentiometer is optional.

Power supplies should be bypassed with 1 µF tantalum and 0.01 µF ceramic capacitors.

Use of a finned heat sink is recommended.

Figure 1. Normal Inverting Operation

Data Conversion

Fast settling time, low bias and offset currents, and modest power consumption make the 1437 an excellent choice for use in data conversion applications. Figure 2 illustrates the 1437 as a fast-settling input buffer to a 12-bit A/D converter.

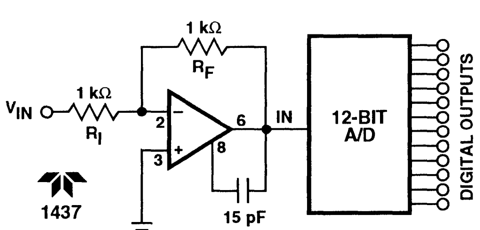


Figure 2. Fast-Settling Buffer

Figure 3 demonstrates the 1437 used as a current-to-voltage converter for a 12-bit DAC.

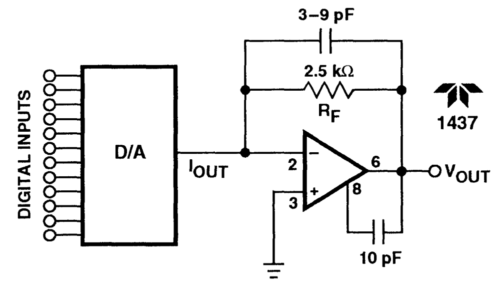


Figure 3. Current-to-Voltage Converter

Stability and Compensation

For wide bandwidth applications, the 1437 can achieve 30 MHz bandwidth at 20 dB gain with a 2 pF compensation capacitor, as shown in Figure 4. The 1437 can operate as a unity-gain buffer out to 40 MHz bandwidth with 27 pF compensation (Figure 5). The 1437 is stable without a compensation capacitor in applications with gains greater than 30 dB, such as a video amplifier (Figure 6), where the gain is 70 dB and a compensation capacitor is not needed. Refer to Figure 8 to determine the required compensation for other gain selections.

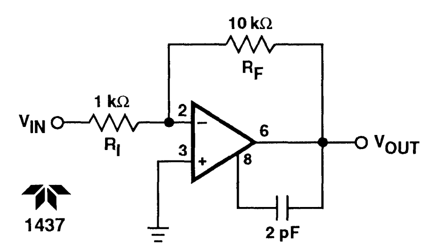


Figure 4. Inverting Gain of 10

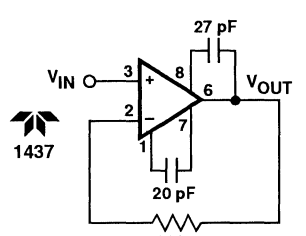


Figure 5. 40 MHz Unity-Gain Buffer

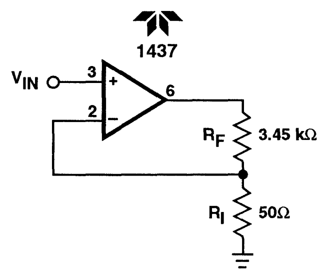


Figure 6. Video Amplifier

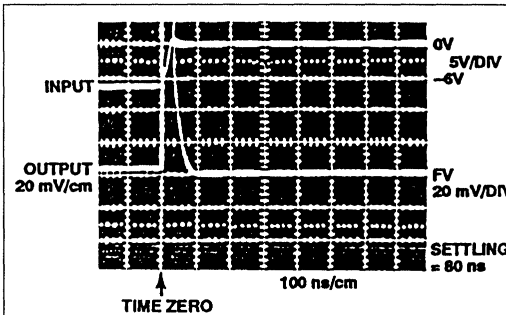
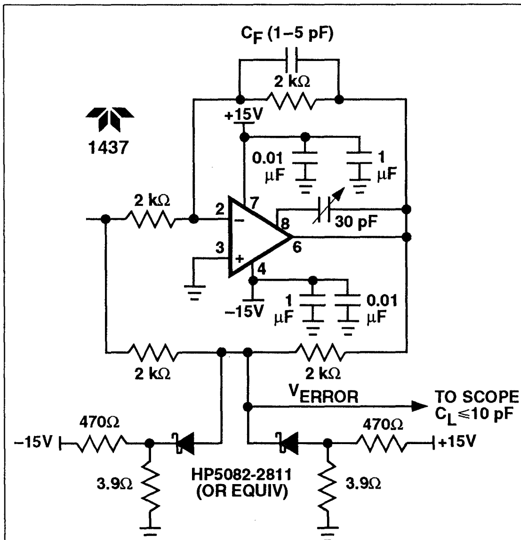


Figure 7b. Settling-Time Graph

Settling-Time Measurements

A typical settling-time measurement circuit for the 1437 is shown in Figure 7a; a photograph of a typical measurement is shown in Figure 7b. Figure 11 presents a graph of settling time to either 100 mV or 10 mV versus the output step size.



NOTES: All resistors 1%, all capacitors 10%. Refer to 1430 data sheet for discussion on settling-time measurement. All capacitors in µF unless otherwise indicated.

Figure 7a. Typical Settling-Time Test Circuit

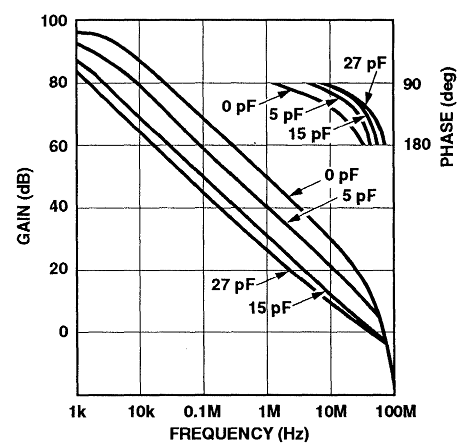


Figure 8. Open-Loop Gain and Phase vs Frequency

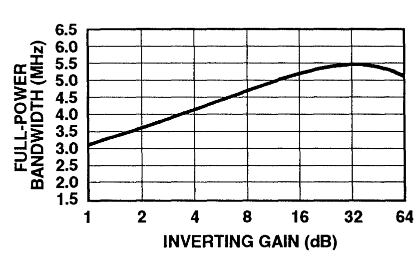


Figure 9. Full-Power Bandwidth vs Inverting Gain

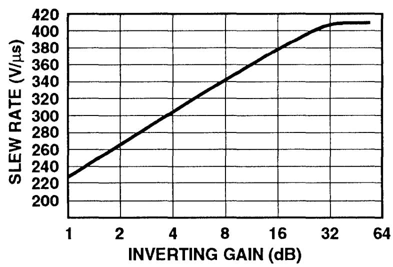


Figure 10. Slew Rate vs Inverting Gain

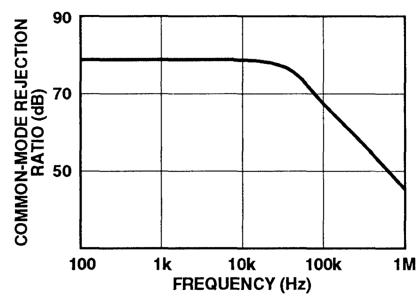


Figure 13. CMRR vs Frequency

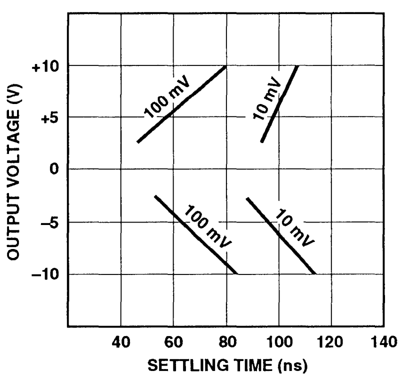


Figure 11. Settling Time vs Output Voltage Change

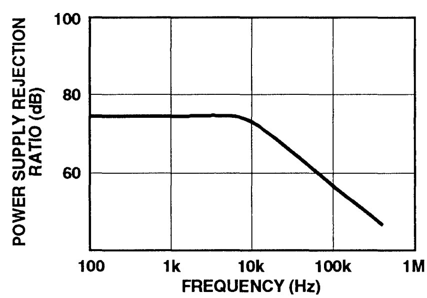


Figure 14. PSRR vs Frequency

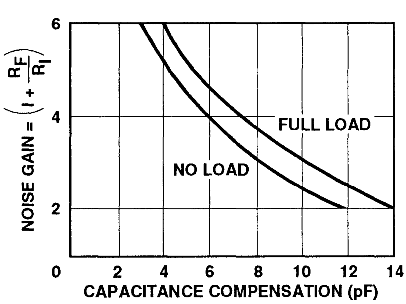


Figure 12. Noise Gain vs C_C for 16% Overshoot

9

NOTES

TELEDYNE COMPONENTS

OPERATIONAL AMPLIFIER — WIDEBAND, FAST-SETTLING

FEATURES

- Gain-Bandwidth Product .... 350 MHz
- Unity Gain Bandwidth .... 40 MHz
- Settling Time to 0.1% (10V step) .... 85 ns
- Output .... ±12V, ±60 mA
- Small, TO-8 Package
- Single External Compensation Capacitor
- FET Input

APPLICATIONS

- Current-to-Voltage DACs
- Pulse Amplifiers
- Radar and Sonar Signal Processing
- Graphics CRT Displays
- Video ADCs, DACs, and S/Hs

GENERAL DESCRIPTION

The 1438 hybrid operational amplifier offers versatility in wideband steady-state and fast-transient applications. The 1438 stands out for speed and predictability, as exemplified by its fast, smooth settling. The absence of large transients and oscillations in the settling waveform make it a dependable system element that can resolve settling problems associated with ADCs, DACs, and sampling circuits.

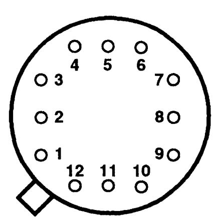
The 1438 has excellent DC characteristics: ±200 pA input bias current, 93 dB open-loop gain, and ±0.5 mV input offset voltage. The choice of a single external compensation capacitor is all that is needed to ensure a 40 MHz bandwidth at a variety of gains. True differential inputs ensure superior performance in all circuit configurations, whether inverting, noninverting, or differential. With an attractive price/performance ratio, the 1438 is an industry standard for high-speed, high-accuracy signal processing and data acquisition.

The 1438 is packaged in a 12-pin TO-8 can and is specified for 0°C to +70°C operation. The High Reliability (-HR) version is specified for –55°C to +125°C operation.

PIN CONFIGURATION

PIN NO.	DESIGNATION	PIN NO.	DESIGNATION
1	NC	12	NC
2	OFFSET TRIM	11	COMPENSATION
3	INVERTING INPUT	10	$+V_{CC}$
4	NONINVERTING INPUT	9	OUTPUT
5	$-V_{CC}$	8	OFFSET TRIM
6	NC	7	NC

NC = NO INTERNAL CONNECTION



BOTTOM VIEW

1438

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage ....±20V
V_{ID} Differential Input Voltage ....±25V
V_{ICM} Common-Mode Input Voltage ....$\pm V_{CC}$
T_C Operating Temperature Range (Case)
1438 ....0°C to +70°C
1438-HR ....–55°C to +125°C
T_{STG} Storage Temperature Range ......–65°C to +150°C
θ_{JC} Overall Junction-to-Case Thermal Resistance (Note 1) ....19°C/W
θ_{JC} Output Transistor Junction-to-Case Thermal Resistance (Note 2) ....35°C/W

NOTES: 1. Overall thermal resistance during normal operating conditions. Multiply this value by the power dissipation of the entire 1438 to determine maximum temperature rise case to junction in the hybrid.
2. Individual thermal resistance of the output stage. The 1438 is a Class AB amplifier. To calculate the output transistor temperature rise case to junction, multiply this figure by the power dissipation of the output transistor. At AC frequencies above 100 Hz, the effective thermal resistance of the output stage will drop 32.5°C/W for the 1438.

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 200Ω, T_C = 25°C, unless otherwise noted.

			1438			1438-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage		—	±0.5	**±2**	—	±0.5	**±2**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±15	—	—	±15	**±50**	µV/°C
I_B	Input Bias Current		—	±200	—	—	±200	—	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±20	—	—	±20	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain		**86**	93	—	**86**	93	—	dB
PSRR	Power Supply Rejection Ratio		—	76	—	—	76	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±8V	**60**	78	—	**60**	78	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 54 dB	**±10**	±12	—	**±10**	±12	—	V
Z_{ID}	Differential Input Impedance		—	$10^{11}\|3$	—	—	$10^{11}\|3$	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	$10^{11}\|3$	—	—	$10^{11}\|3$	—	Ω‖pF
V_O	Output Voltage Swing		**±10**	±12	—	**±10**	±12	—	V
I_O	Output Current		**±50**	±60	—	**±50**	±60	—	mA
I_{SC}	Output Short-Circuit Current		—	±125	—	—	±125	—	mA
R_O	Output Resistance (DC Open-Loop)		—	90	—	—	90	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±12	±15	±20	±12	±15	±20	V
I_{CC}	Quiescent Supply Current		—	±12	**±15**	—	±12	**±15**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

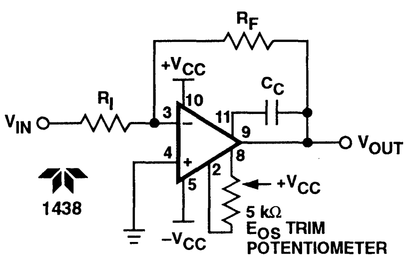
AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 200Ω, C_C = 0 pF, T_C = 25°C, unless otherwise noted.

			1438			1438-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
S_R	Slew Rate		—	400	—	—	400	—	V/µs
		C_C =15 pF	—	225	—	—	225	—	V/µs
GBWP	Gain-Bandwidth Product	f = 10 MHz	—	350	—	—	350	—	MHz
UGBW	Unity-Gain Bandwidth	C_C = 27 pF	—	40	—	—	40	—	MHz
t_s	Settling Time (A_{CL} = -1, C_C = 15 pF)	10V step/1%	—	65	—	—	65	—	ns
		10V step/0.1%	—	85	120	—	85	120	ns
		10V step/0.025%	—	150	—	—	150	—	ns
		10V step/0.01%	—	180	—	—	180	—	ns
e_n	Input Voltage Noise Density	f = 1 kHz	—	10	—	—	10	—	nV/√Hz

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

APPLICATIONS

Basic connections for the 1438 in the normal inverting mode are shown in Figure 1.



NOTES: An E_{OS} trim potentiometer is optional.

Power supplies should be bypassed with 1 µF tantalum and 0.01 µF ceramic capacitors.

Use of a finned heat sink is recommended.

Figure 1. Normal Inverting Operation

Data Conversion

Fast settling time, low bias and offset currents, and modest power consumption make the 1438 an excellent choice for use in data conversion applications. Figure 2 illustrates the 1438 as a fast-settling input buffer to a 12-bit A/D converter.

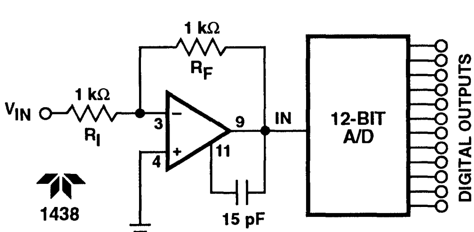


Figure 2. Fast-Settling Buffer

Figure 3 demonstrates the 1438 used as a current-to-voltage converter for a 12-bit DAC.

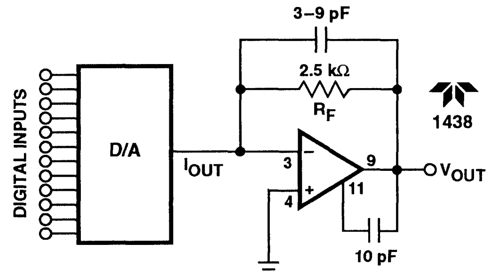


Figure 3. Current-to-Voltage Converter

Stability and Compensation

For wide bandwidth applications, the 1438 can achieve 30 MHz bandwidth at 20 dB gain with a 2 pF compensation capacitor, as shown in Figure 4. The 1438 can operate as a unity-gain buffer out to 40 MHz bandwidth with 27 pF compensation (Figure 5). The 1438 is stable without a compensation capacitor in applications with gains greater than 30 dB, such as a video amplifier (Figure 6), where the gain is 70 dB and a compensation capacitor is not needed. Refer to Figure 8 to determine the required compensation for other gain selections.

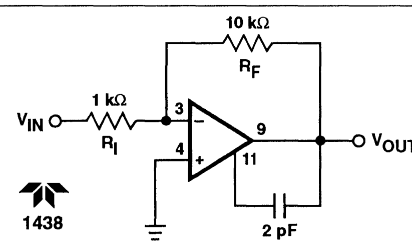


Figure 4. Inverting Gain of 10

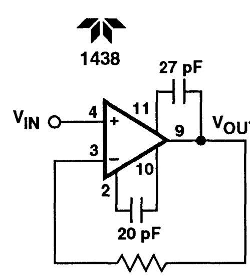


Figure 5. 40 MHz Unity-Gain Buffer

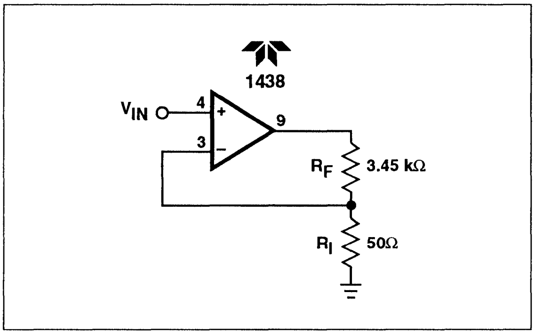


Figure 6. Video Amplifier

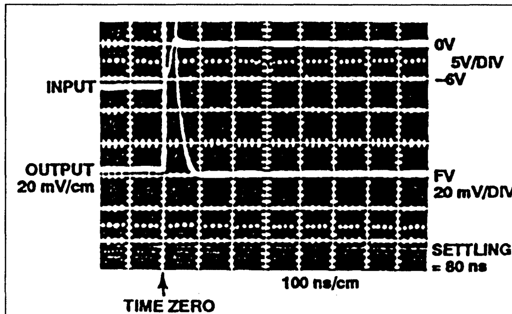
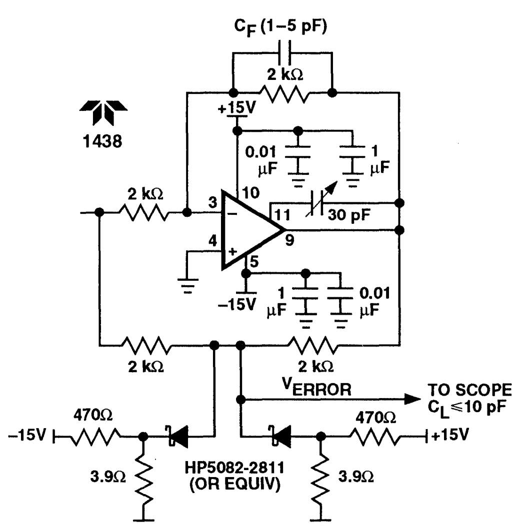


Figure 7b. Settling-Time Graph

Settling-Time Measurements

A typical settling-time measurement circuit for the 1438 is shown in Figure 7a; a photograph of a typical measurement is shown in Figure 7b. Figure 11 presents a graph of settling time to either 100 mV or 10 mV versus the output step size.



NOTES: All resistors 1%, all capacitors 10%. Refer to 1430 data sheet for discussion on settling-time measurement. All capacitors in µF unless otherwise indicated.

Figure 7a. Typical Settling-Time Test Circuit

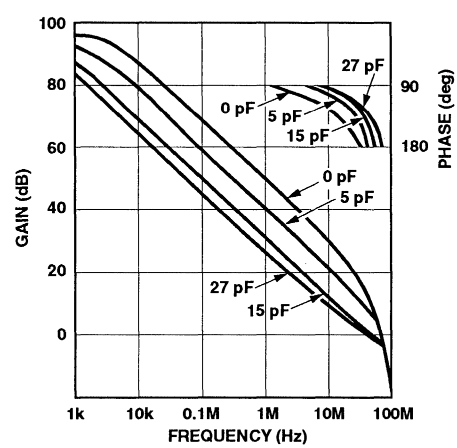


Figure 8. Open-Loop Gain and Phase vs Frequency

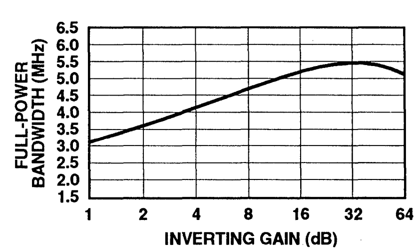


Figure 9. Full-Power Bandwidth vs Inverting Gain

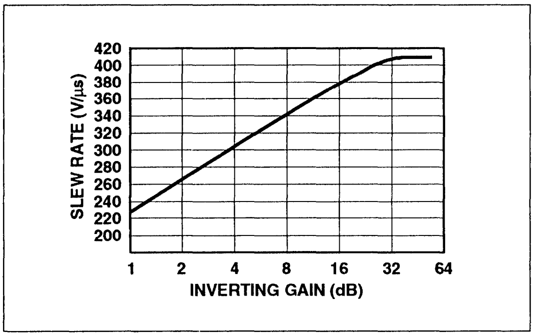


Figure 10. Slew Rate vs Inverting Gain

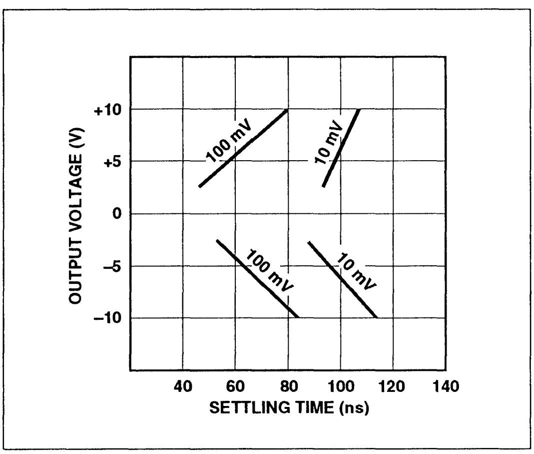


Figure 11. Settling Time vs Output Voltage Change

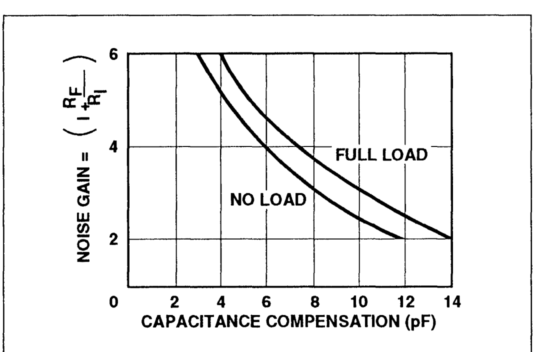


Figure 12. Noise Gain vs C_C for 16% Overshoot

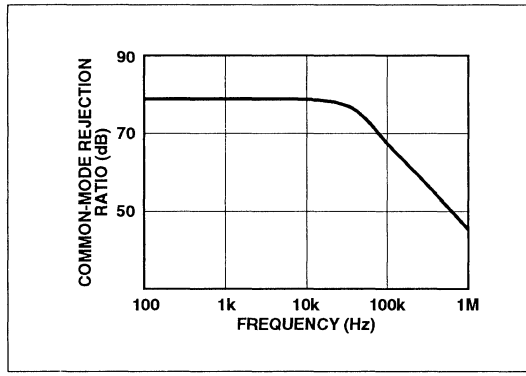


Figure 13. CMRR vs Frequency

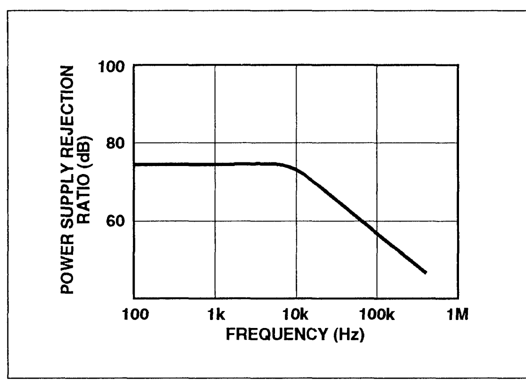


Figure 14. PSRR vs Frequency

NOTES

TELEDYNE COMPONENTS

OPERATIONAL AMPLIFIER — FAST-SETTLING, FULLY-DIFFERENTIAL, FET-INPUT

FEATURES

- Gain-Bandwidth Product .... 2000 MHz
- Unity-Gain Bandwidth .... 80 MHz
- Slew Rate @ $A_{CL} = -1$ .... 1200 V/µs
- Settling Time to 0.01% (10V step) .... 130 ns
- Open Loop Gain .... 110 dB
- Output .... ±13V, ±130 mA
- Excellent Low Gain Stability

APPLICATIONS

- Video Instrumentation
- High-Speed Follower
- Low Error Current Integrator
- Radar
- Video Frequency Filters
- Video Line Driver

GENERAL DESCRIPTION

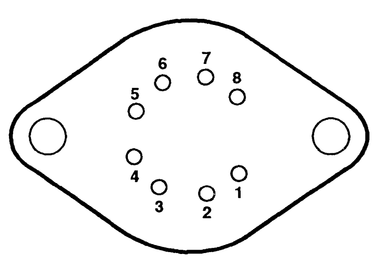
The 1443's combination of high speed, wide bandwidth, excellent DC characteristics, and low-gain stability places it at the forefront of high-performance operational amplifiers. Its 2 GHz gain-bandwidth product, 1200 V/µs slew rate (when compensated for unity gain), and 130 ns settling time clearly make it an outstanding high-speed device. It has been carefully engineered to eliminate the low-gain stability problems that have historically plagued high-speed op amps such as the BB3554. For example, as a unity-gain follower with a 54 pF capacitive load, the 1443 has a small signal (3 dB) bandwidth of 120 MHz, yet still has 35° of phase margin, without using exotic circuit techniques.

The 1443 has a fully-differential FET input followed by a bipolar gain stage that, together, produce excellent DC characteristics. Common-mode rejection ratio (CMRR) is 80 dB (minimum). Offset voltage and bias current are guaranteed less than ±3 mV and –50 pA, respectively. Open-loop gain is 100 dB (minimum). External compensation with a single capacitor allows users to tailor 1443 performance for different applications.

The 1443 is packaged in an 8-pin TO-3 can and is specified for 0°C to +70°C operation. The 1443 High Reliability (HR) version is specified for –55°C to +125°C operation.

PIN CONFIGURATION

PIN NO.	DESIGNATION
1	OUTPUT
2	$+V_{CC}$
3	COMPENSATION
4	E_{OS} TRIM
5	–INPUT
6	+INPUT
7	$-V_{CC}$
8	E_{OS} TRIM



BOTTOM VIEW

1443

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply Voltage	±18V
V_{ID}	Differential Input Voltage	±25V
V_{ICM}	Common-Mode Input Voltage	$\pm V_{CC}$
T_C	Operating Temperature Range (Case)	
	1443	0°C to +70°C
	1443-HR	–55°C to +125°C
T_{STG}	Storage Temperature Range	–65°C to +150°C

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, T_C = 25°C, unless otherwise noted.

			1443			1443-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage		—	±1	**±3**	—	±1	**±3**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±25	—	—	±25	**±75**	µV/°C
I_B	Input Bias Current		—	±10	**±50**	—	±10	**±50**	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±5	—	—	±5	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain	R_L = 100Ω	**100**	110	—	**100**	110	—	dB
PSRR	Power Supply Rejection Ratio		**70**	90	—	**70**	90	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±5V	**80**	100	—	**80**	100	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 74 dB	**±7**	±9	—	**±7**	±9	—	V
Z_{ID}	Differential Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
V_O	Output Voltage Swing	R_L = 100Ω	**±10.5**	±13	—	**±10.5**	±13	—	V
I_O	Output Current		**±100**	±130	—	**±100**	±130	—	mA
I_{SC}	Output Short-Circuit Current	(Note 2)	—	±160	—	—	±160	—	mA
R_O	Output Resistance (DC Open-Loop)		—	200	—	—	200	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±12	±15	±18	±12	±15	±18	V
I_{CC}	Quiescent Supply Current		—	±45	**±55**	—	±45	**±55**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.
2. The 1443 cannot withstand a continuous short-circuit to ground.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, C_C = short, T_C = 25°C, unless otherwise noted.

			1443			1443-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
S_R	Slew Rate	R_L = 100Ω, A_{CL} = -1	900	1200	—	900	1200	—	V/µs
GBWP	Gain-Bandwidth Product	f = 100 kHz, R_L = 200Ω,	—	2000	—	—	2000	—	MHz
		C_C = 0 pF, f = 1 MHz, R_L = 200Ω, C_C = 10 pF	90	130	—	90	130	—	MHz
UGBW	Unity-Gain Bandwidth		—	80	—	—	80	—	MHz
t_s	Settling Time (A_{CL} = -1)	10V step/1%	—	50	—	—	50	—	ns
		10V step/0.1%	—	80	—	—	80	—	ns
		10V step/0.01%	—	130	165	—	130	165	ns
e_n	Input Voltage Noise Density	f = 1 kHz	—	15	—	—	15	—	nV/√Hz
C_L	Capacitive Load (maximum w/o oscillation)	R_L = 100Ω, A_{CL} = -1	—	>300	—	—	>300	—	pF

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

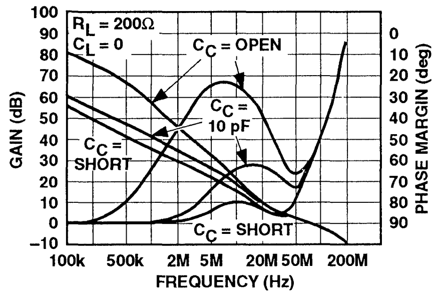


Figure 1. Gain and Phase vs Frequency for Variable Compensation

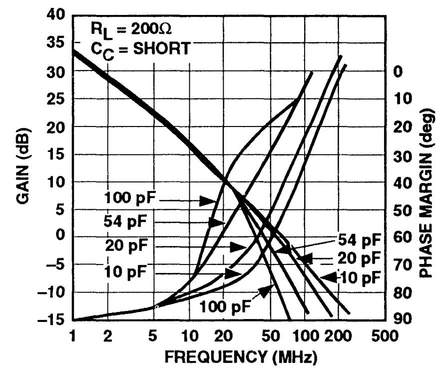


Figure 4. Gain and Phase vs Frequency for Variable C_L

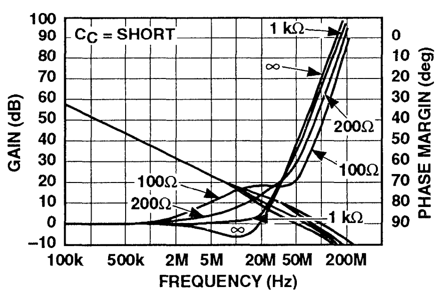
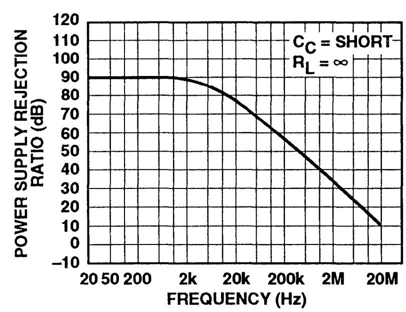


Figure 2. Gain and Phase vs Frequency for Variable R_L



NOTE: Good PSRR vs frequency means smaller supply bypasses can be used to suppress supply noise feedthrough.

Figure 5. PSRR vs Frequency

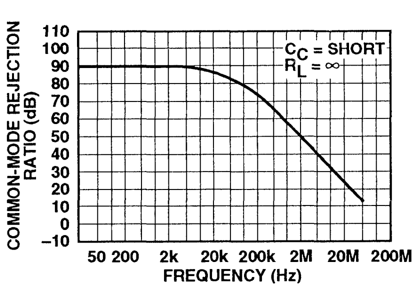


Figure 3. CMRR vs Frequency

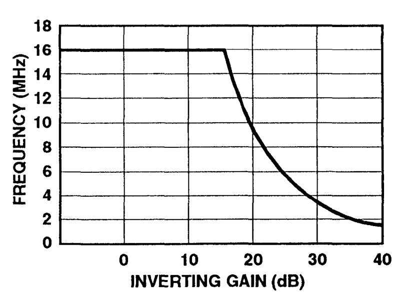


Figure 6. Utilizable Full-Power Bandwidth

APPLICATIONS INFORMATION

Compensation

The 1443's design allows users to tailor its compensation, and thereby its performance, to suit different applications. The total effective compensation is an internal 5 pF capacitor in series with whatever capacitor is placed between the compensation input (pin 3) and the output (pin 1).

To minimize low frequency (<1 MHz) slewing error and maximize bandwidth for higher gains (>30 dB), the external compensation capacitance should range from 0 pF (open) to 5 pF. For best transient response at lower gains, values greater than 5 pF are recommended. Above approximately 15 pF, a short is recommended in lieu of a larger capacitor. The exact value of compensation depends on how much ringing and overshoot an application allows. Most low-gain applications will achieve best overall results by shorting pin 1 to pin 3.

Following selection of a compensation capacitor (C_C), a feedback capacitor (C_{FB}) must be selected to properly compensate for input capacitance:

$$C_{FB} = 2\ \text{pF}/(NG-1),$$

where NG = noise gain.

Noise gain is defined as $1/\beta$, where β is equal to the fraction of the output signal that is fed back to the input. Note that noise gain is the multiple of amplifier input noise which appears at the amplifier output. In case of low C_C, C_{FB} may be increased to provide extra phase lead. The choice of C_{FB} is best made on the basis of permissible overshoot after C_C has been chosen on the basis of gain.

Bypassing

The traditional practice of decoupling power supply lines with bypass capacitors is necessary to prevent high-frequency oscillations resulting from power supply lead inductance and parasitic capacitance. Unfortunately, the bypass capacitor and lead inductance form a tank circuit that can ring when a step change in the op-amp output forces a current pulse from the supply. In many cases, adding a dissipative element (a resistor) will damp the ringing; its exact value is not critical, but its presence is.

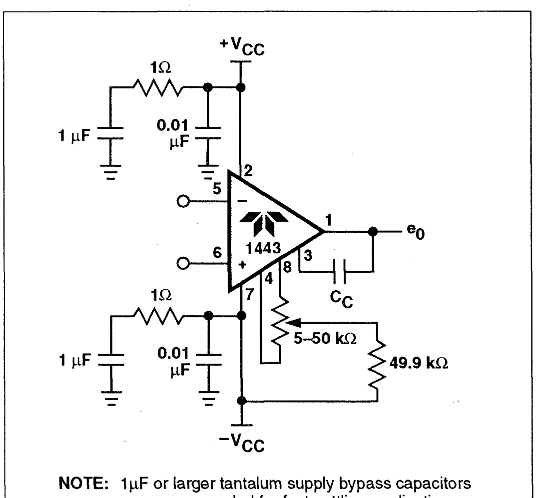


Figure 7. Typical Connection

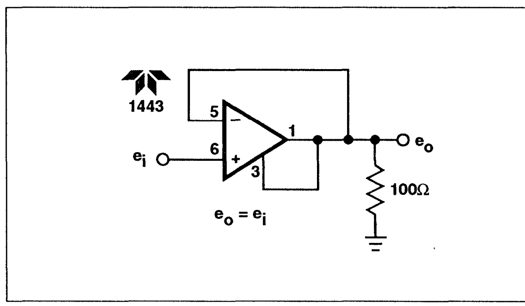


Figure 8. Follower Configuration

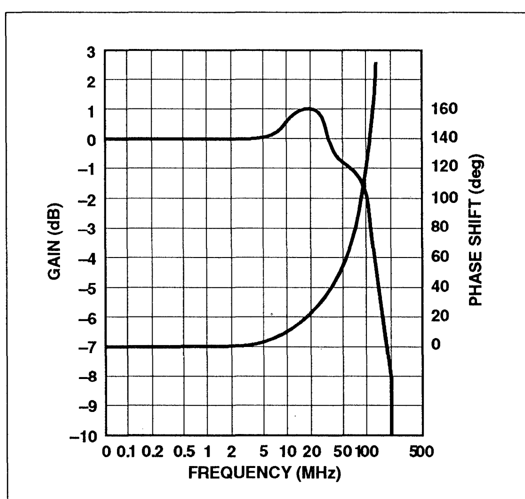


Figure 9. Frequency Response (As a Follower)

Follower

When used as a unity-gain follower (Figure 8), the 1443 has a 3 dB bandwidth of 120 MHz with only 1 dB of peaking, as shown in Figure 9. Pulse response in this configuration is shown in Figure 10.

Unity-Gain Inverter

As a unity-gain inverter (Figure 11), the 1443 has a typical 3 dB bandwidth of 60 MHz. It will settle quickly even with loads of C_L = 100 pF and R_L = 100Ω, yet will not oscillate if R_{IN} is open.

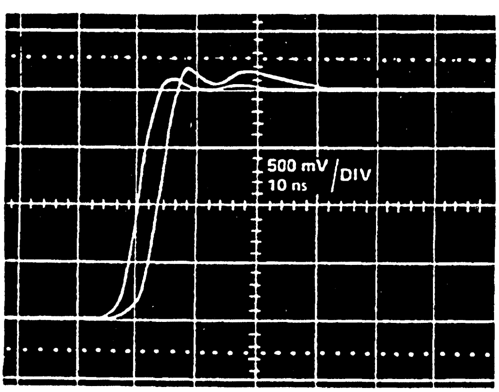


Figure 10. Follower Pulse Response

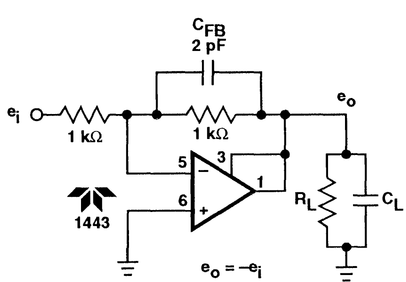


Figure 11. Unity-Gain Inverter

Differential Amplifier

With fully-differential capabilities, the 1443 lends itself to many system configurations. Figure 12 shows a typical configuration for the 1443 as a wideband (approximately 15 MHz) differential amplifier with 20 dB gain.

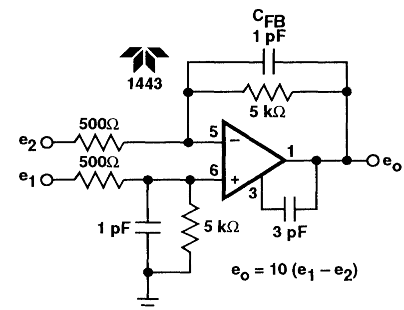


Figure 12. Wideband Differential Amplifier

High-Speed Coaxial Driver

Figure 13 shows the 1443 being used as a high-speed coaxial line driver. The 1443 can drive a 50Ω cable to ±5V with 50Ω terminating resistors at both ends to minimize reflections. Using 1% termination resistors and 50Ω line, ghosts are attenuated at least 77 dB. Without the series 50Ω resistor at the amplifier output, ghosts may only be attenuated by 38 dB.

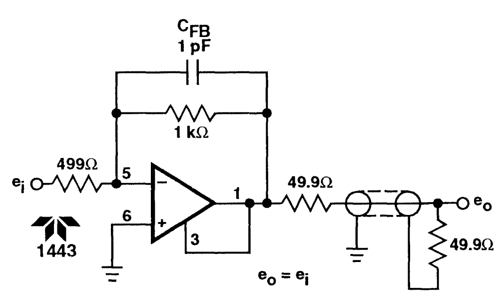


Figure 13. High-Speed Coaxial Driver

9

HIGH-FREQUENCY TROUBLESHOOTING TECHNIQUES

Parasitic Oscillations

With VHF operational amplifiers like the 1443, it is not enough to only be concerned with stability problems due to loop closure. Of equal concern (and often times more annoying) are oscillations due to parasitics. Parasitic oscillations are apt to arise in VHF op-amp circuits in which lead lengths are long (>1/2 inch), or loop areas are large (>1 cm^2) at the summing junction, feedback capacitor, power supply pins, or ground-return paths (from bypass capacitors or the amplifier case).

For the 1443, these oscillations may contain frequencies up to 0.5 GHz. Therefore, you cannot always count on seeing them with an oscilloscope. When parasitic oscillation occurs, it often appears as a DC offset because circuit conductance nonlinearities detect its RF envelope. If what appears to be a DC offset is noisy and erratic, or responsive to the placement of your finger or a test probe, parasitic oscillations may be the problem.

Parasitic oscillations are also likely if there is any significant lead length separating the amplifier output from its load capacitance. The lead inductance and load capacitance form a series LC circuit that looks like a larger and larger capacitor as it approaches resonant frequency from below.

Even lead lengths associated with attaching an oscilloscope probe can cause problems. For a typical scope probe, with the ground attached 10 cm from the measurement point, the ground lead and probe form a series LC circuit of approximately 100 nH and 12 pF. At 100 MHz band-edge for the 1443, the apparent probe capacitance will double. In parallel with already-existing circuit capacitances, this 24 pF may be enough to cause oscillation. A good practice is to wrap the ground lead around the probe tip. An even better practice is to use a probe socket (Tektronix 131-0258-00) installed in the circuit, with careful choice of the ground return route.

Semiconductor capacitances and bandwidths are nonlinearly-dependent on voltage and current. Devices that oscillate at one voltage level may not oscillate at another. Check for op-amp oscillations at zero volt output and at several additional output points in each polarity. You will often find that oscillations exist at one or two points in the circuits' output range. These might be observed only as unexplained perturbations on the output (they may not appear as bursts) due to envelope detection, as previously discussed.

The Finger as an Analog Development Tool

In 15V systems, the finger can be a useful investigative tool, if thoughtfully applied. It can couple signals in and out and can also be used as a load. A well-laid-out RF op-amp circuit will be only slightly affected by a light touch. Dramatic changes reveal a sensitive point! Check a circuit by touching the amplifier case, the supply rails (carefully), ground, control knobs, chassis parts, etc. If things change markedly when you touch these areas, parasitics may be the problem.

Other Considerations

Problems commonly associated with video amplifiers are naturally present in VHF circuits. Therefore, proper compensation of input capacitance by C_{FB} cannot be ignored. Nor can the impedance (inductance) of the ground return paths (though use of a ground-plane is helpful, it is no panacea).

Thermal Considerations

The 1443 has internal current limiting but can only withstand an output short to ground if, during the short, the output current is negative as often as positive during each 100 ms period. It is not short-circuit-proof under all conditions. Maximum continuous junction temperature should be kept below +150°C.

The case-to-ambient thermal resistance of the TO-3 package is θ_{CA} = 35°C/W. For the two output transistors, θ_{JC} is 95°C/W.With a 20 V_{P-P} output sinusoid, the effective θ_{JC} of these two transistors is 65°C/W. A heat sink is required above +75°C ambient (+85°C for sinusoidal output) if a 200Ω load is used. With a 100Ω load, a heat sink is required above +40°C ambient (+50°C for sinusoidal output).

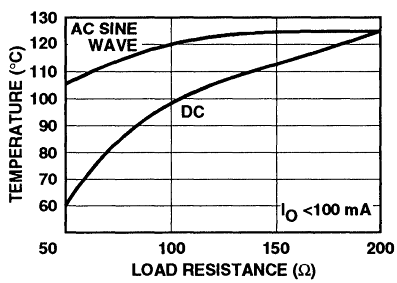


Figure 14. Maximum Allowable Case Temperature vs Load Resistance With Worst-Case Power Dissipation

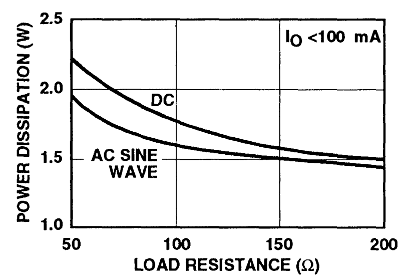


Figure 15. Worst-Case Power Dissipation vs Load Resistance

9

NOTES

TELEDYNE COMPONENTS

OPERATIONAL AMPLIFIER — HIGH SPEED, VMOS OUTPUT

FEATURES

- **Output** .... ±31V, ±200 mA
- **Gain-Bandwidth Product** .... 1 GHz
- **Slew Rate** 300V/µsec
- **VMOS Output Stage**
- **No SOA Restrictions**
- **Fully Differential Input**

APPLICATIONS

- **Video Amplifiers**
- **Video Yoke Drivers**
- **ATE Pin Drivers**
- **Driving Inductive and Capacitive Loads**

GENERAL DESCRIPTION

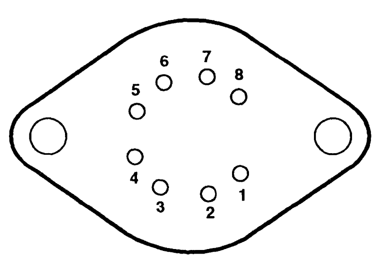
The 1460 heralds a new era in high power, wideband operational amplifiers. Designed for ATE signal amplification and pin driving, the 1460 surpasses the competition in speed (1 GHz gain bandwidth product, 300V/µsec slew rate) and in output capability (full ±31V, ±200 mA output). The 1460 is a fully differential input, single-ended output device with internal current limiting and external compensation. A single capacitor allows users to tailor 1460 performance to different applications.

The 1460 is ideal for high speed, high gain applications that require a ±30V, high current output. It is optimized for gains greater than five, making it a superb choice for either analog or digital signal amplification at video frequencies. Secondary breakdown problems associated with most power op amps are virtually eliminated in the 1460 through the use of a unique VMOS output stage. The output voltage and current are limited only by power dissipation and not by safe operating area curves. For any application in which the amplifier will be dissipating more than one watt of power, an external heat sink must be used. The thermal resistance of the 1460 is 20°C/watt (θ_{JC}) and 50°C/watt (θ_{JA}). Junction temperatures should not exceed 150°C for normal operation or 200°C for a short-circuit condition.

The 1460 is packaged in an 8-pin TO-3 can. The standard unit is specified for 0°C to +70°C operation. The 1460 High Reliability (HR) version is specified for –55°C to +125°C operation.

PIN CONFIGURATION

PIN NO.	DESIGNATION
1	OUTPUT
2	OFFSET ADJUST
3	$+V_{CC}$
4	+IN
5	–IN
6	$-V_{CC}$
7	COMPENSATION
8	COMPENSATION/OFFSET ADJUST



BOTTOM VIEW

1460

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage .... ±40V
V_{ID} Differential Input Voltage .... ±6V
V_{ICM} Common-Mode Input Voltage .... +V_{CC} to (+V_{CC} - 60V)

T_C Operating Temperature Range (Case)
1460 .... 0°C to +70°C
1460-HR .... –55°C to +125°C
T_{STG} Storage Temperature Range ...... –65°C to +150°C

DC CHARACTERISTICS: (Note 1) V_{CC} = ±36V, R_L = 10 kΩ, T_C = 25°C, unless otherwise noted.

			1460			1460-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage		—	±1	**±5**	—	±1	**±5**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±10	—	—	±10	**±50**	µV/°C
I_B	Input Bias Current		—	±5	**±15**	—	±5	**±15**	µA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±50	—	—	±50	**±150**	nA/°C
I_{OS}	Input Offset Current		—	±0.3	**±1.5**	—	±0.3	**±1.5**	µA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±3	—	—	±3	—	nA/°C
A_{VOL}	Open-Loop Voltage Gain	R_L = 200Ω	**80**	92	—	**80**	92	—	dB
PSRR	Power Supply Rejection Ratio		**75**	100	—	**75**	100	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = -18V/+30V	**70**	85	—	**70**	85	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 64 dB	**-20/+32**	-22/+34	—	**-20/+32**	-22/+34	—	V
Z_{ID}	Differential Input Impedance		—	7.5kII30	—	—	7.5kII30	—	ΩIIpF
Z_{ICM}	Common-Mode Input Impedance		—	1MII6	—	—	1MII6	—	ΩIIpF
V_O	Output Voltage Swing	R_L = 200Ω	**±30**	±31	—	**±30**	±31	—	V
I_O	Output Current		**±150**	±200	—	**±150**	±200	—	mA
I_{SC}	Output Short-Circuit Current		—	±250	**±300**	—	±250	**±300**	mA
R_O	Output Resistance (DC Open-Loop)		—	20	—	—	20	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±15	±36	±40	±15	±36	±40	V
I_{CC}	Quiescent Supply Current		—	±20	**±25**	—	±20	**±25**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

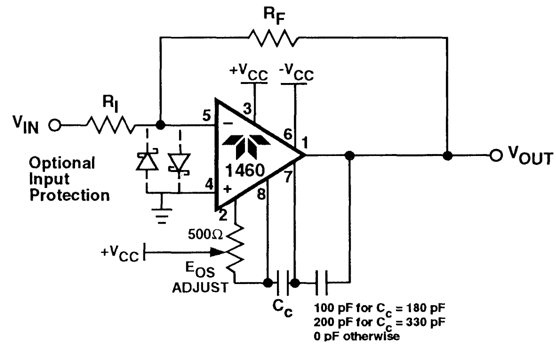
AC CHARACTERISTICS: (Note 1) V_{CC} = ±36V, R_L = 10 kΩ, C_C = 0 pF, T_C = 25°C, unless otherwise noted.

			1460			1460-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
S_R	Slew Rate		—	300	—	—	300	—	V/µs
		C_C = 40 pF	50	65	—	50	65	—	V/µs
GBWP	Gain-Bandwidth Product	f = 10 MHz	—	1000	—	—	1000	—	MHz
UGBW	Unity-Gain Bandwidth		—	74	—	—	74	—	MHz
t_s	Settling Time (A_{CL} = -6, C_C = 40 pF)	30V step/0.1%	—	1	—	—	1	—	µs
		10V step/0.1%	—	0.8	—	—	0.8	—	µs

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

HIGH SPEED, VMOS OUTPUT OPERATIONAL AMPLIFIER

STANDARD CONFIGURATION



APPLICATIONS INFORMATION

In the absence of a positive supply voltage, the output will follow the negative supply. Should such a condition occur, it is possible, depending on the feedback network used, that the maximum allowable differential input voltage may be exceeded. If there is a possibility that the differential input voltage may exceed ±6V, input overvoltage protection, shown in the Standard Configuration diagram, should be used.

Compensation

For optimum performance and noise rejection, power supplies should be bypassed with 1 µF tantalum capacitors. When driving heavy loads, more bypass capacitance may be needed.

Figures 1 and 2 illustrate low gain noninverting and inverting applications. The 1460's compensation capacitor for each of these applications was chosen for 10 MHz bandwidth operation.

The application in Figure 3 has a 10 MHz bandwidth and an inverting gain of 100 yielding 1 GHz gain bandwidth product. Notice that there is no compensation capacitor on the 1460. No compensation capacitor is needed for gains over 100. However, a feedback capacitor between 1 pF and 10 pF is recommended to compensate for the 1460's input capacitance.

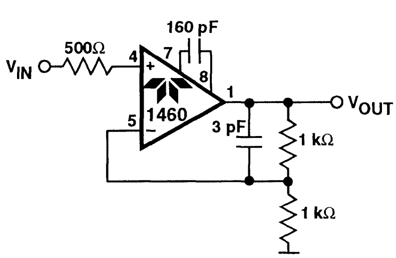


Figure 1. 10 MHz Noninverting Gain of Two Amplifier

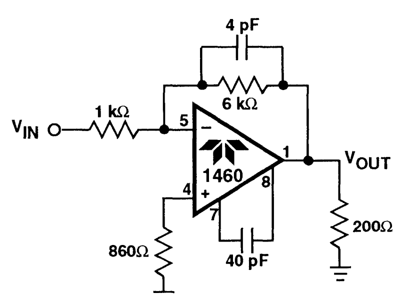


Figure 2. 10 MHz Inverting Gain of Six Amplifier

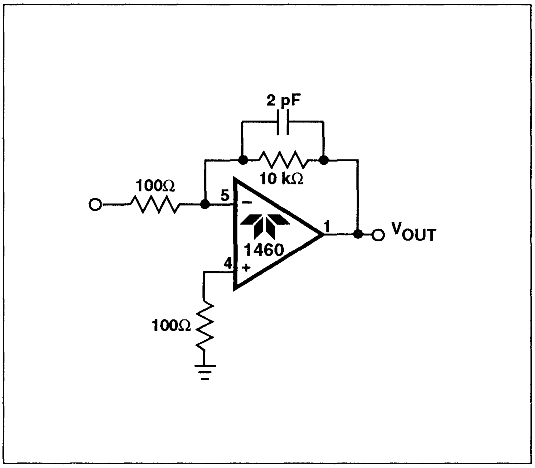


Figure 3. 10 MHz Inverting Gain of 100

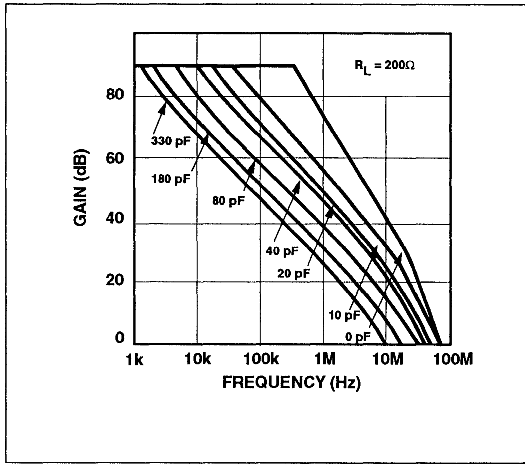


Figure 4. Bode Plot

Cc	Frequency at Unity Gain	Phase at Unity Gain	Frequency at 180°	Slew Rate
0 pF	74 MHz	275°	5 MHz	250V/µs
10 pF	74 MHz	267°	25 MHz	125V/µs
20 pF	55 MHz	277°	32 MHz	84V/µs
40 pF	50 MHz	216°	36 MHz	50V/µs
80 pF	32 MHz	165°	37 MHz	28V/µs
180 pF	17 MHz	132°	45 MHz	13V/µs
330 pF	10 MHz	118°	50 MHz	7V/µs

Figure 5. A.C. Characteristics vs C_C

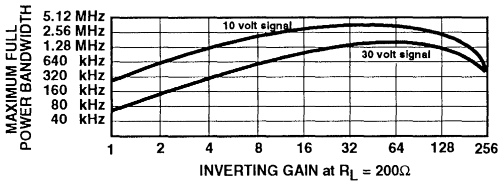


Figure 6. Full Power Bandwidth vs Inverting Gain

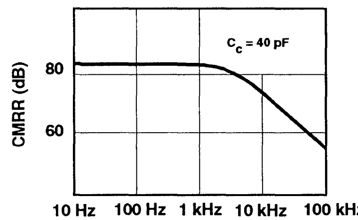


Figure 8. CMRR vs Frequency

9

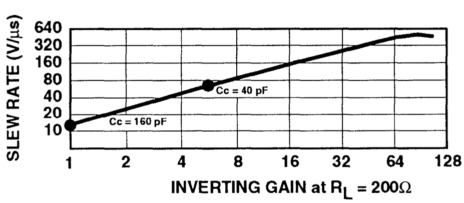


Figure 7. Slew Rate vs Inverting Gain

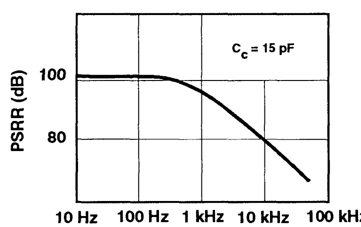


Figure 9. PSRR vs Frequency

NOTES

TELEDYNE COMPONENTS

OPERATIONAL AMPLIFIER — HIGH-SPEED, HIGH-POWER, VMOS-OUTPUT

FEATURES

- **Output .... ±34V, ±750 mA**
- **Gain-Bandwidth Product .... 1 GHz**
- **Slew Rate .... 1000 V/µs**
- **FET Input**
- **VMOS-Output Stage**
- **No SOA Restrictions**
- **Operation (-HR) .... –55°C to +125°C**

APPLICATIONS

- **Video Yoke Drivers**
- **Video Distribution Amplifiers**
- **High-Speed ATE Pin Drivers**
- **High-Accuracy Audio Amplification**
- **Driving Inductive and Capacitive Loads**

GENERAL DESCRIPTION

The 1461 is an extremely fast, FET-input, VMOS-output, power operational amplifier. It operates from ±15V to ±40V supplies, has output voltages up to ±34V, and output currents up to ±750 mA. Its unique VMOS-output stage eliminates the safe operating area (SOA) restrictions and secondary breakdown problems that plague virtually all other presently-available power op amps. The 1461's ability to handle high output currents at any voltage eliminates the intricate problems normally caused by driving capacitive or inductive loads.

The 1461's combination of speed and power characteristics is unmatched. Its 115 dB open-loop gain, 1 GHz gain-bandwidth product, and 1000 V/µs slew rate make it an outstanding high-speed op amp.

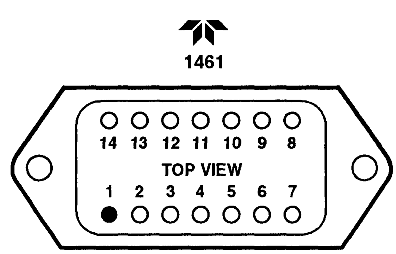
The 1461 is housed in a 14-pin dual-in-line package with "ears" for easy mounting to heat sinks. Compensation is accomplished with a single external capacitor. Two external current-limiting resistors are optional.

The standard 1461 is specified for 0°C to +70°C operation. For high-reliability military/aerospace applications, the High Reliability (HR)1461 version is specified for –55°C to +125°C operation.

PIN CONFIGURATION

PIN NO.	DESIGNATION	PIN NO.	DESIGNATION
1	–IN	8	OUTPUT
2	+IN	9	$+I_{LIMIT}$
3	NC	10	$+V_{CC}$
4	NC	11	COMPENSATION
5	$-V_{CC}$	12	COMPENSATION
6	$-I_{LIMIT}$	13	OFFSET ADJUST
7	NC	14	OFFSET ADJUST

NC = NO INTERNAL CONNECTION



1461

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage .... ±45V
V_{ID} Differential Input Voltage .... ±25V
V_{ICM} Common-Mode Input Voltage .... $\pm V_{CC}$
T_C Operating Temperature Range (Case)
1461 .... 0°C to +70°C
1461-HR .... –55°C to +125°C
T_{STG} Storage Temperature Range .... –65°C to +150°C
θ_{JC} Output Transistor Junction-to-Case Thermal Resistance .... 11°C/W

DC CHARACTERISTICS: (Note 1) V_{CC} = ±36V, R_L = 10 kΩ, T_C = 25°C, unless otherwise noted.

			1461			1461-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage		—	±0.5	**±5**	—	±0.5	**±5**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±25	—	—	±25	**±75**	µV/°C
I_B	Input Bias Current		—	±10	**±100**	—	±10	**±100**	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±5	—	—	±5	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain		**100**	115	—	**100**	115	—	dB
PSRR	Power Supply Rejection Ratio		—	100	—	—	100	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±22V	**90**	108	—	**90**	108	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 84 dB	**±24**	±28	—	**±24**	±28	—	V
Z_{ID}	Differential Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
V_O	Output Voltage Swing		**±30**	±34	—	**±30**	±34	—	V
		R_L =50Ω	**±27**	±29	—	**±27**	±29	—	V
I_O	Output Current		**±600**	±750	—	**±600**	±750	—	mA
I_{SC}	Output Short-Circuit Current	Note 2	—	±800	—	—	±800	—	mA
R_O	Output Resistance (DC Open-Loop)		—	10	—	—	10	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±15	±36	±40	±15	±36	±40	V
I_{CC}	Quiescent Supply Current		—	±20	**±25**	—	±20	**±25**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.
2. Internally current limited. May be limited to lower current using external resistors.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±36V, R_L = 10 kΩ, C_C = 0 pF, T_C = 25°C, unless otherwise noted.

			1461			1461-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
S_R	Slew Rate	R_L ≥ 1 kΩ	700	1000	—	700	1000	—	V/µs
		C_C = 30 pF, R_L ≥ 1 kΩ	—	150	—	—	150	—	V/µs
GBWP	Gain-Bandwidth Product	f = 100 kHz	800	1000	—	800	1000	—	MHz
UGBW	Unity-Gain Bandwidth	C_C = 20 pF	—	15	—	—	15	—	MHz
t_s	Settling Time (A_{CL} = -1, C_C = 30 pF)	25V step/1%	—	350	—	—	350	—	ns
		25V step/0.1%	—	0.5	1	—	0.5	1	µs
		10V step/1%	—	250	—	—	250	—	ns
		10V step/0.1%	—	400	—	—	400	—	ns
e_n	Input Voltage Noise Density	f = 1 kHz	—	15	—	—	15	—	nV/√Hz

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

HIGH-SPEED, HIGH-POWER, VMOS-OUTPUT OPERATIONAL AMPLIFIER

APPLICATIONS INFORMATION

Compensation

The 1461 is externally compensated with a single capacitor. The gain bandwidth and slew rate of this device are related to the value of the capacitor by the following approximations:

Slew Rate $\cong$ $(0.006/C_C)$ V/sec
Gain Bandwidth $\cong$ $(0.001/C_C)$ Hz

These formulas are accurate for C_C ranging down to a value of 5–10 pF, at which point circuit parasitics begin to take effect and limit the gain-bandwidth product to about 1 GHz and the slew rate to approximately 1000 V/µs.

In order to ensure stability when using the 1461, the value of the compensation capacitor must be such that the result of the gain-bandwidth product divided by the noise gain is less than 15 MHz. This amplifier can maintain a 15 MHz bandwidth up to noise gains of 10–20 dB by proper adjustment of the compensating capacitance.

Teledyne Components defines noise gain as $1/\beta$, where β is equal to the fraction of the output signal that is fed back to the inverting input. Note that noise gain is the multiple of the amplifier input noise that appears at the amplifier output.

Current Limiting

Internal to the 1461 are two 0.8Ω resistors that limit maximum output current to approximately 750 mA. Output current can be further limited by the use of two external, user-supplied resistors. One resistor ($+R_{SC}$) limits the positive current, the other resistor ($-R_{SC}$) limits the negative current. To determine the value of the limiting resistors, the following approximation can be used:

$$\pm R_{SC} \cong [(0.65/I_{LIMIT}) - 0.8]\Omega$$

During initial testing, it is recommended 10Ω resistors be used for $+R_{SC}$ and $-R_{SC}$, to minimize the possibility of damage to the amplifier during circuit verification.

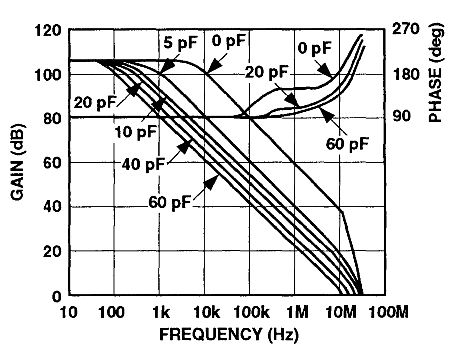


Figure 1. Bode Plot

Thermal Considerations

The physics of standard bipolar output devices lead to a problem known as thermal runaway. This phenomenon is due to the fact that as a transistor gets hot it conducts more current for any given V_{BE}, and the more current it conducts the hotter it gets. This cycle continues until the transistor eventually destroys itself. This phenomenon also occurs in small regions of the base of a transistor. If heat is not given time to dissipate from these hot spots, the transistor will destruct at power levels far below that which the device could normally withstand. This is called secondary breakdown and is the reason for safe operating curves on most power op-amp data sheets.

The 1461 has a VMOS-output stage. Since field effect transistors do not exhibit thermal runaway, they do not suffer from secondary breakdown problems. Output voltages and currents are limited only by power dissipation and not by safe operating curves. However, heat sinking may be required to ensure maximum allowable junction temperatures are not exceeded.

Example: On the 1461's thermal derating curves, the slope of the infinite heat sink line is 11°C/W. This is the thermal resistance (θ_{JC}) from each VMOS. Assuming each VMOS junction dissipates 4W, maximum ambient temperature (T_A) is +70°C, and maximum allowable junction temperature (T_J) is +150°C, the necessary thermal resistance of the heat sink can be determined as follows:

1. Assuming the device has a complementary output stage and the thermal rise (junction-case) of each VMOS-output transistor does not affect the other, calculate the maximum amount of power dissipated for each of the two output devices (5W and 4W for this example). Using the higher power dissipation number, determine the maximum allowable case temperature (T_C):

$$T_C = T_J - P_{VMOS1}\ (\theta_{JC})$$
$$T_C = +150°C - (5W)\ (11°C/W)$$
$$T_C = +95°C$$

2. Calculate maximum total power dissipation (P_T) for the 1461 (assuming ±36V supply and 20 mA quiescent current):

$$P_T = (72V)\ (20\ mA) + 5\ W_{VMOS1} + 4\ W_{VMOS2}$$
$$P_T = 10.44W$$

3. Calculate thermal resistance (θ_{CA}) of the heat sink needed to dissipate this power:

$$\theta_{CA} = (T_C - T_A)/P_T$$
$$\theta_{CA} = (95°C - 70°C)/10.44W$$
$$= 2.4°C/W$$

Lead Inductance

The high frequencies and high-current levels involved with the 1461 necessitate a closer look at the phenomenon of lead inductance. A single 22-gauge wire has a lead inductance of 0.636 µH/ft. This inductance can become significant when large rates of dI/dt are demanded at the output.

For example, if as much as 4 inches of wire is used to connect pin 9 to pin 10 (the + current-limiting terminals), this wire would have an inductance of 212 nH. At 10 MHz, this inductance would have an effective impedance of 13.3Ω. This resistance would limit the output current to only 42.5 mA. If the unit were driving a 50Ω load, the effective slew rate would be limited to:

$$dI/dt = 0.6/L = 2.82\ A/\mu s,$$

yielding a maximum slew rate of 141 V/µs, far less than the capability of this device.

Skin Effect

Skin effect, though not quite as important as lead inductance, can also cause problems in high-frequency, high-power designs. The current flowing in a conductor establishes a magnetic field around the conductor. This causes the distribution of current flow to vary as a function of frequency. At higher frequencies, current is forced to the surface of the conductor, effectively yielding a much smaller wire. The effective resistance of the wire increases with the frequency according to the following formula:

$$R_{AC} = K\ (\sqrt{f})\ R_{DC},$$

where f is frequency in MHz and K is a factor that varies with wire size and type.

Example: A 1-foot 22-gauge wire will have the following effective resistance at 10 MHz:

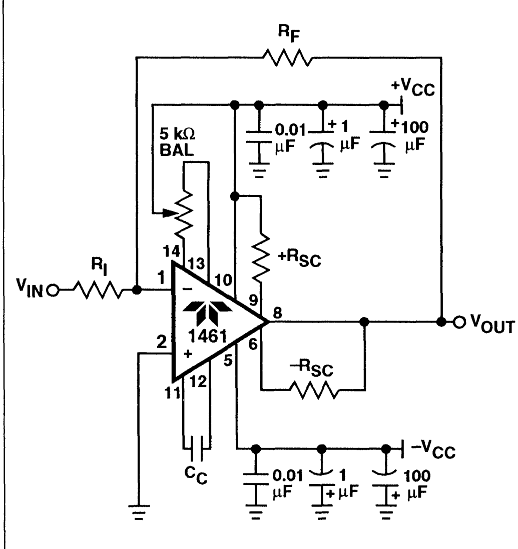
$$K = 6.86$$
$$R_{DC} = 0.016\ \Omega/ft$$
$$R_{AC} = (6.86)\ (\sqrt{10})\ (0.016) = 0.347\Omega$$

Even as little as 0.347Ω can decrease output current capabilities of the 1461 by as much as 30%.

It should be clear from this review of lead inductance and skin effect that short lead lengths are necessary in fast, high-power applications.

Standard Configuration

The 1461 in a standard inverting amplifier configuration (including compensation capacitor, current-limiting resistors, and offset adjusting potentiometer) is shown in Figure 2. To meet specified performance and avoid output oscillations, power supplies should be bypassed as shown. The 100 µF capacitors are needed when driving heavy loads at high frequencies.



$$\pm R_{SC} \cong \left(\frac{0.65}{I_{LIMIT}} - 0.8\right)\Omega$$

Figure 2. Standard Inverting Configuration

HIGH-SPEED, HIGH-POWER, VMOS-OUTPUT OPERATIONAL AMPLIFIER

Capacitive Loads

The 1461 can be used with a compensation network that can compensate for almost any value of capacitive load (Figure 3). First, choose C_C for operation without a capacitive load. Then choose a series compensation resistor, R_C, such that $R_C C_C = R_{INT} C_L$, where R_{INT} is approximately 10Ω.

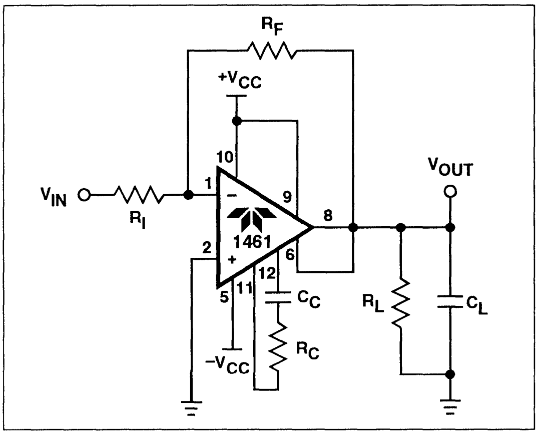


Figure 3. **Capacitive Load Driver**

Yoke Driver

The absence of secondary breakdown makes the 1461 an excellent choice for driving electron-beam-deflection yokes, with settling times as low as 2–3 μs for a 0.5A step. For inductive load compensation, choose $R_C C_C = L/R$. (See Figure 4.)

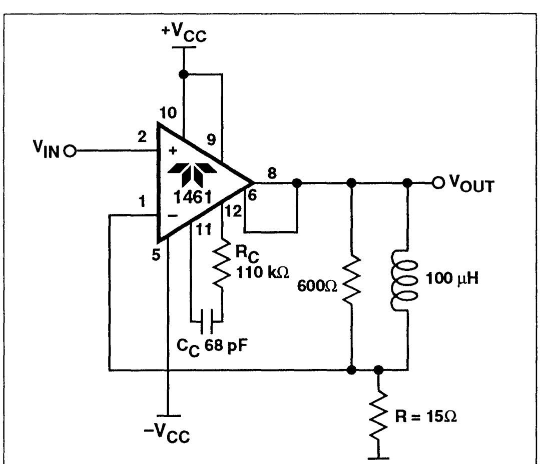


Figure 4. **Yoke Driver**

Video Amplifier

The 1461 as a video distribution amplifier (Figure 5) can directly drive 10 coax cables. At a gain of 16 or higher, a compensation capacitor is not needed.

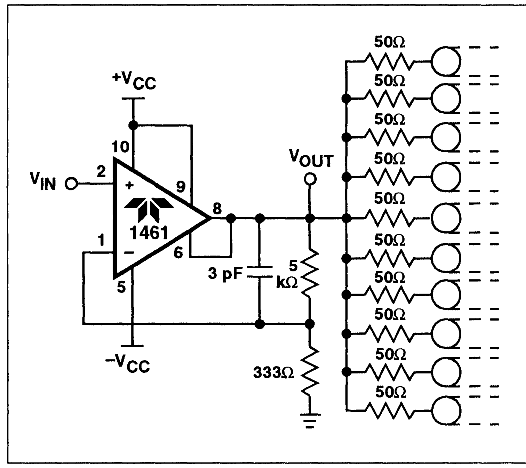


Figure 5. **Video Distribution Amplifier**

Audio Amplifier

The 1461 has plenty of output current to drive the large base current requirements of high-power transistors. (See Figure 6.)

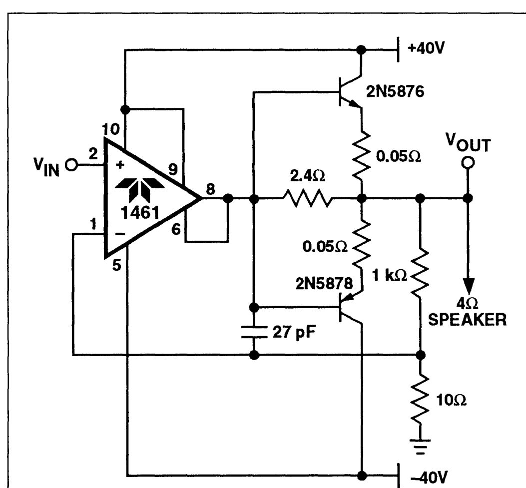


Figure 6. **High-Power Audio Amplifier**

Inverting Unity Gain

The 1461 can drive a 50Ω load in an inverting unity-gain configuration as shown in Figure 7. The recommended compensation for this application is 20 pF.

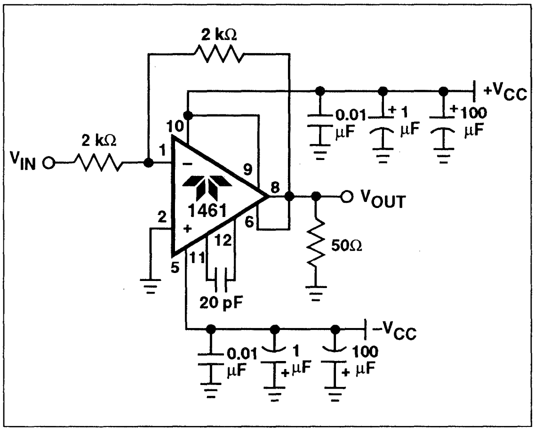


Figure 7. Inverting Unity Gain

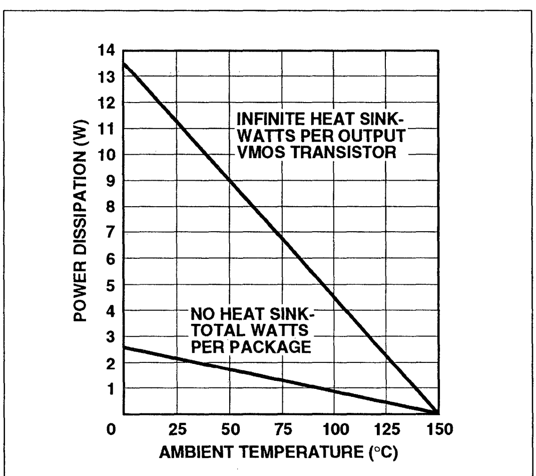


Figure 8. Allowable Power Dissipation vs Ambient Temperature

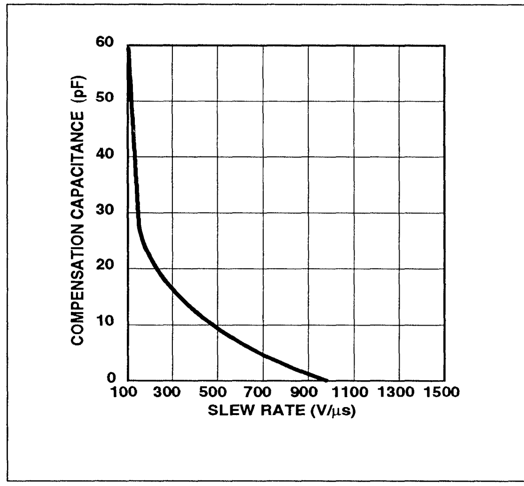


Figure 9. Slew Rate vs. C_C

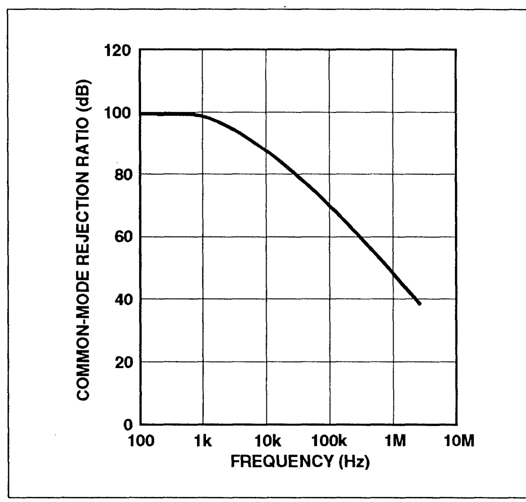


Figure 10. CMRR vs Frequency

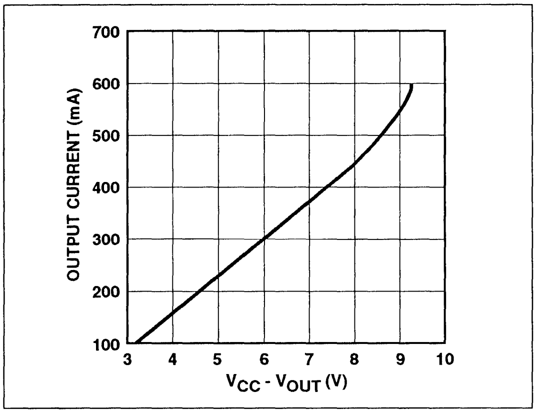


Figure 11. Output Voltage vs Output Current

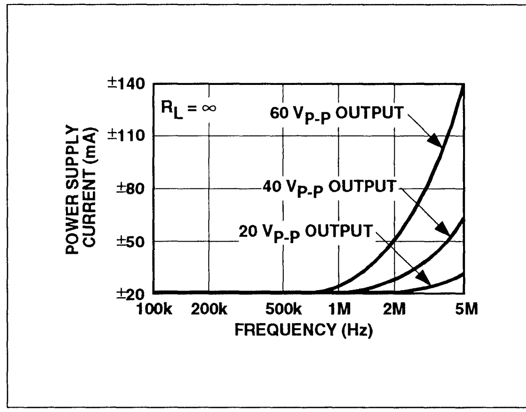


Figure 13. Quiescent Current vs Operating Frequency ($R_L = \infty$)

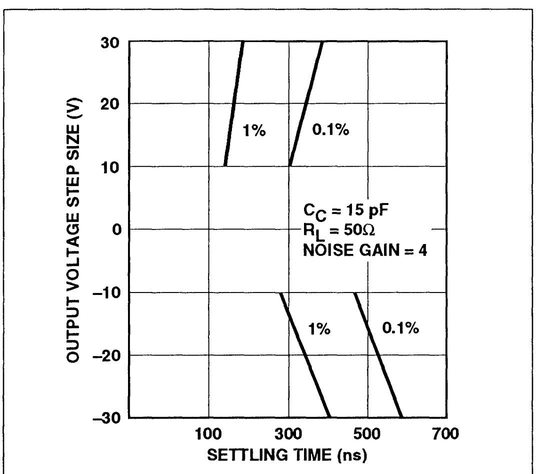


Figure 12. Settling Time vs Output Voltage Step Size

9

NOTES

TELEDYNE COMPONENTS

OPERATIONAL AMPLIFIER — HIGH-VOLTAGE, VERY-HIGH-POWER

FEATURES

- **High-Output Current Guaranteed........±10A (Peak)**
- **Unity-Gain Stable**
- **Gain-Bandwidth Product (Single-Pole Rolloff) ....4 MHz**
- **Slew Rate...5V/µs**
- **Voltage Supplies ....±10V to ±50V**
- **Pin/Performance Compatible with PA-12, OPA512**

APPLICATIONS

- **Motor Drives**
- **Magnetic Deflection Circuits**
- **Programmable Power Supplies**
- **High-Power Servo Amplifiers**
- **Audio Amplifiers (to 120W rms)**

GENERAL DESCRIPTION

The 1468 is a high-voltage, very-high-power operational amplifier. It can operate over a wide range of supply voltages (±10V to ±50V) and has a guaranteed minimum output current of ±10A (peak). The output stage is biased Class AB for low crossover distortion and optimum linearity. It is also protected against back-EMF which is encountered when driving inductive loads, such as motors or solenoids.

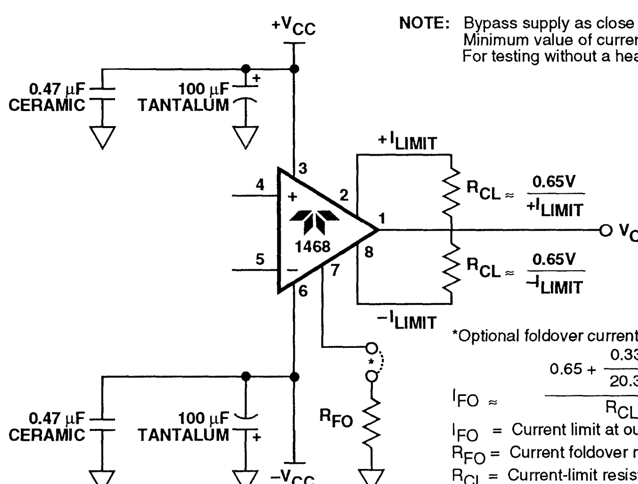
With an 8Ω load, the 1468's open-loop gain is 96 dB minimum, 108 dB typical. Input offset voltage is ±2 mV and input bias current is 12 nA. The 1468 is internally compensated for unity gain and delivers excellent dynamic performance for a device of this type. Slew rate is a fast 5V/µs and unity-gain bandwidth is an impressive 4 MHz.

The 1468 is housed in an 8-pin TO-3 can. The standard product is specified for –25°C to +85°C operation. The 1468 High Reliability (HR) version is specified for –55°C to +125°C operation.

9

STANDARD CONFIGURATION

NOTE: Bypass supply as close to power supply pins as possible. Minimum value of current-limit resistors is 0.043Ω (15A). For testing without a heat sink, use R_{CL} = 2.2Ω, 1/4W.



*Optional foldover current limiting.

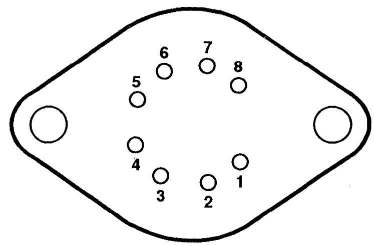
$$I_{FO} \approx \frac{0.65 + \dfrac{0.33 \times V_O}{20.33 + R_{FO}}}{R_{CL}}$$

I_{FO} = Current limit at output voltage V_O
R_{FO} = Current foldover resistor in kΩ
R_{CL} = Current-limit resistor in Ω
V_O = Instantaneous output voltage

1468 (TCPA12)

PIN CONFIGURATION

PIN NO.	DESIGNATION
1	OUTPUT
2	$+I_{LIMIT}$
3	$+V_{CC}$
4	+INPUT
5	–INPUT
6	$-V_{CC}$
7	FOLDOVER
8	$-I_{LIMIT}$



BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage ....±50V
V_{ID} Differential Input Voltage ....±(|V_{CC}|–3V)
V_{ICM} Common-Mode Input Voltage ....±V_{CC}
I_O Output Current ....±15A
P_D Internal Power Dissipation 125W
T_C Operating Temperature Range (Case)
1468 ....–25°C to +85°C
1468-HR ....–55°C to +125°C

T_{STG} Storage Temperature Range ....–65°C to +150°C
T_J Junction Temperature
(Output Transistor) (Note 1)......................+200°C
θ_{JC} Junction-to-Case Thermal Resistance
(Output Transistor) (Note 2)............0.9°C/W @ AC
1.4°C/W @ DC

NOTES: 1. Prolonged operation at maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF.
2. AC rating applies if the output current alternates between both output transistors at a rate greater than 60 Hz.

DC CHARACTERISTICS: (Note 1) V_{CC} = ±40V, R_L = 1 kΩ, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1468 Min	1468 Typ	1468 Max	1468-HR Min	1468-HR Typ	1468-HR Max	Unit
V_{OS}	Input Offset Voltage		—	±2	**±6**	—	±2	**±6**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±10	—	—	±10	**±65**	µV/°C
I_B	Input Bias Current		—	±12	**±30**	—	±12	**±30**	nA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±50	—	—	±50	**±400**	pA/°C
I_{OS}	Input Offset Current		—	±12	**±30**	—	±12	**±30**	nA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±50	—	—	±50	**±400**	pA/°C
A_{VOL}	Open-Loop Voltage Gain		—	110	—	—	110	—	dB
		R_L = 8Ω	**96**	108	—	**96**	108	—	dB
PSRR	Power Supply Rejection Ratio		**74**	90	—	**74**	90	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±33V	**74**	100	—	**74**	100	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 68 dB	**±35**	±37	—	**±35**	±37	—	V
Z_{ID}	Differential Input Impedance		—	200M‖3	—	—	200M‖3	—	Ω‖pF
V_O	Output Voltage Swing	I_{OUT} = 5A	**±35**	—	—	**±35**	—	—	V
		I_{OUT} = 10A	**±34**	—	—	**±34**	—	—	V
I_O	Output Current	Peak	**±10**	—	—	**±10**	—	—	A
I_{SC}	Output Short-Circuit Current	Note 2	—	—	—	—	—	—	A
R_O	Output Resistance (DC Open-Loop)		—	2	—	—	2	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±10	±40	±45	±10	±40	±45	V
I_{CC}	Quiescent Supply Current		—	±25	**±50**	—	±25	**±50**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.
2. Current limiting is set by user via external resistors.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±40V, R_L = 1 kΩ, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1468 Min	1468 Typ	1468 Max	1468-HR Min	1468-HR Typ	1468-HR Max	Unit
S_R	Slew Rate		2.5	5	—	2.5	5	—	V/µs
GBWP	Gain-Bandwidth Product	f = 1 MHz, R_L = 8Ω	—	4	—	—	4	—	MHz
UGBW	Unity-Gain Bandwidth		—	4	—	—	4	—	MHz
t_s	Settling Time (A_{CL} = -1)	2V step/0.1%	—	2	—	—	2	—	µs
e_n	Input Voltage Noise Density	f = 1 kHz	—	16	—	—	16	—	nV/√Hz
i_n	Input Current Noise Density	f = 1 kHz	—	0.18	—	—	0.18	—	pA/√Hz
C_L	Capacitive Load (Maximum w/o oscillation)	A_{CL} = +1	1500	—	SOA	1500	—	SOA	pF

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

Output Current Limiting

The 1468 output can be current limited using the $\pm I_{LIMIT}$ formulas shown in the standard configuration diagram. In some applications, foldover current limiting can be used to allow increased output current as the 1468 output approaches the power supply rail voltage. To calculate the foldover current limit, use the formula for I_{FO} shown in the diagram. The following procedures should be followed:

1. Calculate a value for R_{CL} that provides a safe current limit at V_O = 0V.
2. Calculate the maximum value of I_{FO}* by using a value of 0Ω for R_{FO}. This is the maximum current limit possible using the foldover current-limit option.
3. Calculate a value for R_{FO} using the value for R_{CL} calculated in step 1, and a desired I_{FO} limit which is lower than the maximum limit calculated in step 2.

*This calculation assumes the output voltage (V_O) is the same polarity as the current carrying supply voltage. If not, invert the polarity of V_O before making this calculation.

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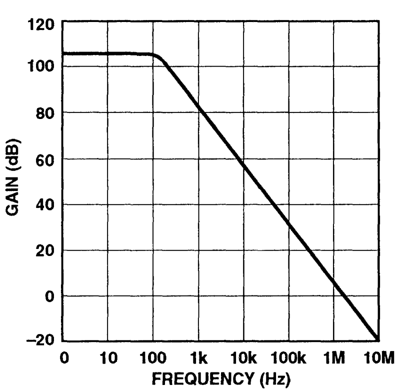


Figure 1. Bode Plot

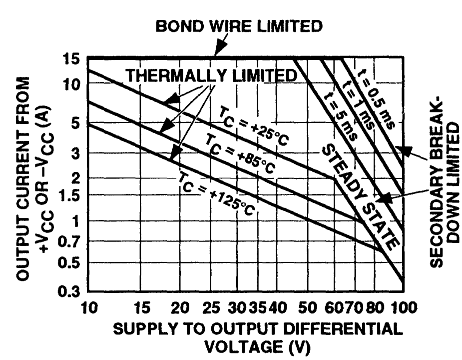


Figure 2. Safe Operating Area (SOA)

NOTES

TELEDYNE COMPONENTS

OPERATIONAL AMPLIFIER — FAST-SETTLING, HIGH-VOLTAGE

FEATURES

- **Output ....±143V, ±100 mA**
- **Settling Time (100V Step to ±0.01%) ......2.5 μs Max**
- **Common-Mode Voltage ....±140V**
- **Input Overvoltage and Output Short-Circuit Protected**
- **Standard TO-3 Can**
- **BB3583 Compatible with Improved AC Performance**
- **Operating Temperature (-HR) ....–55°C to +125°C**

APPLICATIONS

- **ATE Pin Drivers**
- **Electrostatic Deflection**
- **High-Voltage DACs**

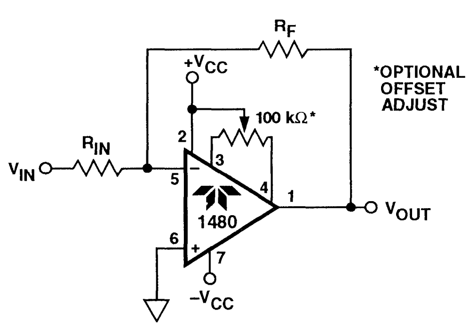
GENERAL DESCRIPTION

The 1480 is a fully-differential FET-input operational amplifier capable of operating over a voltage supply range of ±15V to ±150V with common-mode and output voltages ranging to within 10V of the supply voltages, and output currents of up to ±100 mA. The 1480 is pin compatible with the BB3583, but has superior time and frequency performance. Gain-bandwidth product is 18 MHz, slew rate is 100V/μs, and unity-gain bandwidth is 5 MHz.

The input of the 1480 is fully protected. It can withstand common-mode voltages to $\pm(|V_{CC}|+5)$V, differential voltages to 450V, and input voltage slew rates to 150 kV/μs. Output current is short-circuit limited at ±125 mA. The true differential FET-input (typical CMRR is 125 dB) limits input bias current to ±200 pA (maximum). The bias and offset current drifts are small enough to greatly reduce the large offset drifts normally associated with high-voltage circuits.

The 1480 is packaged in a TO-3 metal can and is specified for 0°C to +70°C operation. The 1480 High Reliability (HR) version is specified for –55°C to +125°C operation.

NORMAL INVERTING OPERATION



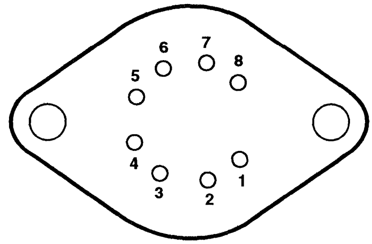
NOTE: The metal case is electrically isolated. It is recommended that it be grounded during use.

1480

PIN CONFIGURATION

PIN NO.	DESIGNATION
1	OUTPUT
2	$+V_{CC}$
3	OFFSET TRIM
4	OFFSET TRIM
5	–IN
6	+IN
7	$-V_{CC}$
8	NC

NC = NO INTERNAL CONNECTION



BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage .... ±160V
V_{ID} Differential Input Voltage (Note 1) .... ±450V
V_{ICM} Common-Mode Input Voltage .... $\pm(V_{CC}+5)$V
Input Slew Rate (Notes 1, 2) .... ±150 kV/µs
T_C Operating Temperature Range (Case)
1480 .... 0°C to +70°C
1480-HR .... –55°C to +125°C
T_{STG} Storage Temperature Range ...... –65°C to +150°C

NOTES: 1. Includes power-off conditions.
2. The high differential voltage and dv/dt ratings of the input prevent input stage blowout even if the input is directly shorted to either rail. Such shorts do stress the input, however, and we cannot guarantee protection for durations exceeding a few seconds.

DC CHARACTERISTICS: (Note 1) $V_{CC} = \pm150$V, $R_L = 10$ kΩ, $T_C = 25$°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1480 Min	1480 Typ	1480 Max	1480-HR Min	1480-HR Typ	1480-HR Max	Unit
V_{OS}	Input Offset Voltage		—	±1	**±3**	—	±1	**±3**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±15	—	—	±15	**±100**	µV/°C
I_B	Input Bias Current		—	±50	**±200**	—	±50	**±200**	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±40	—	—	±40	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain		—	120	—	—	120	—	dB
		$R_L = 1.8$ kΩ	**95**	115	—	**95**	115	—	dB
PSRR	Power Supply Rejection Ratio		**100**	120	—	**100**	120	—	dB
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm130$	**110**	125	—	**110**	125	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 104 dB	**±135**	±140	—	**±135**	±140	—	V
Z_{ID}	Differential Input Impedance		—	$10^{11}\|\|5$	—	—	$10^{11}\|\|5$	—	Ω||pF
Z_{ICM}	Common-Mode Input Impedance		—	$10^{11}\|\|3$	—	—	$10^{11}\|\|3$	—	Ω||pF
V_O	Output Voltage Swing	$R_L = 1.8$ kΩ	**±140**	±143	—	**±140**	±143	—	V
I_O	Output Current		**±75**	±100	—	**±75**	±100	—	mA
I_{SC}	Output Short-Circuit Current	$R_L = 500$Ω (Note 2)	—	±125	—	—	±125	—	mA
R_O	Output Resistance (DC Open-Loop)		—	200	—	—	200	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±15	—	±150	±15	—	±150	V
I_{CC}	Quiescent Supply Current		—	±10	**±12**	—	±10	**±12**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.
2. The 1480 is short-circuit protected to ground or either supply for supply voltages totalling <100V. It is short-circuit protected to ground only for supplies totalling up to 160V.

AC CHARACTERISTICS: (Note 1) $V_{CC} = \pm150V$, $R_L = 10\ k\Omega$, $T_C = 25°C$, unless otherwise noted.

			1480			1480-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
S_R	Slew Rate		—	100	—	—	100	—	V/µs
GBWP	Gain-Bandwidth Product	f = 100 kHz	—	18	—	—	18	—	MHz
UGBW	Unity-Gain Bandwidth		—	5	—	—	5	—	MHz
t_s	Settling Time (A_{CL} = -10)	100V step/0.1%	—	1	1.5	—	1	1.5	µs
		100V step/0.01%	—	1.5	2.5	—	1.5	2.5	µs
e_n	Input Voltage Noise Density	f = 1 kHz	—	20	—	—	20	—	nV/√Hz
C_L	Capacitive Load (Maximum w/o oscillation)		100	250	—	100	250	—	pF

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

NOTES

OPERATIONAL AMPLIFIER — HIGH-VOLTAGE

FEATURES

- **Output .... ±70V, ±100 mA**
- **Fully Differential FET Input**
- **Wide Supply Range .... ±15V to ±75V**
- **Input Overvoltage Protected**
- **Output Current Limited at ±125 mA**

APPLICATIONS

- **ATE Pin Drivers**
- **Electrostatic Deflection**

GENERAL DESCRIPTION

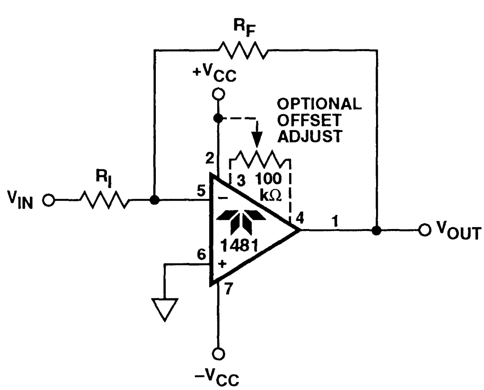
The 1481 is a high-voltage operational amplifier capable of operating with supply voltages as high as ±75V or as low as ±15V. It can provide output voltage swings as high as ±70V with output currents to ±100 mA (short circuit limited to ±125 mA). The cascoded FET input stage is fully overvoltage protected.

This operational amplifier features a 25V/µs slew rate and a 4.5 MHz unity-gain bandwidth. Maximum input offset voltage is ±3 mV, and minimum open-loop gain is 94 dB (full load). The Class AB output stage can drive up to 10,000 pF capacitive loads at closed-loop gains of 10 or more. Pin compatible with the BB3581, the 1481 features more than double the output current capability of its competitor's and faster settling time.

The 1481 is packaged in an 8-pin TO-3 can. The standard unit is specified for 0°C to +70°C operation. The 1481 High Reliability (HR) version is specified for –55°C to +125°C operation.

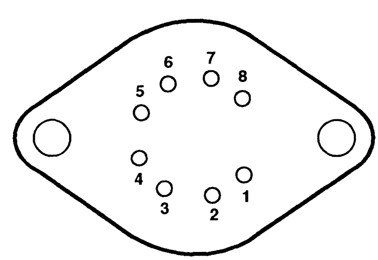
9

NORMAL INVERTING OPERATION



NOTE: The metal case is electrically isolated. It is recommended the case be grounded during use.

PIN CONFIGURATION



BOTTOM VIEW

PIN NO.	DESIGNATION
1	OUTPUT
2	$\pm V_{CC}$
3	OFFSET TRIM
4	OFFSET TRIM
5	–INPUT
6	+INPUT
7	$-V_{CC}$
8	NC

NC = NO INTERNAL CONNECTION

1481

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage ....±80V
V_{ID} Differential Input Voltage ....±V_{CC}
V_{ICM} Common-Mode Input Voltage ....±V_{CC}
T_C Operating Temperature Range (Case)
1481 .... 0°C to +70°C
1481-HR ....–55°C to +125°C
T_{STG} Storage Temperature Range ......–65°C to +150°C
θ_{JC} Output Transistor Junction-to-Case Thermal Resistance ....6°C/W

DC CHARACTERISTICS: (Note 1) V_{CC} = ±75V, R_L = 10 kΩ, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1481 Min	1481 Typ	1481 Max	1481-HR Min	1481-HR Typ	1481-HR Max	Unit
V_{OS}	Input Offset Voltage		—	±1	**±3**	—	±1	**±3**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±15	—	—	±15	**±50**	µV/°C
I_B	Input Bias Current		—	±10	**±100**	—	±10	**±100**	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±10	—	—	±10	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain		—	108	—	—	108	—	dB
		R_L = 850Ω	**94**	106	—	**94**	106	—	dB
PSRR	Power Supply Rejection Ratio		**70**	94	—	**70**	94	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±60	**70**	94	—	**70**	94	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 64 dB	**±65**	±70	—	**±65**	±70	—	V
Z_{ID}	Differential Input Impedance		—	10^{11}‖6	—	—	10^{11}‖6	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
V_O	Output Voltage Swing		—	±73	—	—	±73	—	V
		R_L = 850Ω	**±68**	±70	—	**±68**	±70	—	V
I_O	Output Current		**±80**	±100	—	**±80**	±100	—	mA
I_{SC}	Output Short-Circuit Current	R_L =330Ω	—	±125	**±150**	—	±125	**±150**	mA
R_O	Output Resistance (DC Open-Loop)		—	100	—	—	100	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±15	—	±75	±15	—	±75	V
I_{CC}	Quiescent Supply Current		—	±11	**±15**	—	±11	**±15**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±75V, R_L = 10 kΩ, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1481 Min	1481 Typ	1481 Max	1481-HR Min	1481-HR Typ	1481-HR Max	Unit
S_R	Slew Rate		—	25	—	—	25	—	V/µs
GBWP	Gain-Bandwidth Product	f = 100 kHz	—	7.5	—	—	7.5	—	MHz
UGBW	Unity-Gain Bandwidth		3	4.5	—	3	4.5	—	MHz
t_s	Settling Time (A_{CL} = -1)	100V step/0.1%	—	7.5	—	—	7.5	—	µs
e_n	Input Voltage Noise Density	f = 1 kHz	—	20	—	—	20	—	nV/√Hz
C_L	Capacitive Load (Maximum w/o oscillation)	A_{CL} ≥ 10	10,000	—	—	10,000	—	—	pF

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

OPERATIONAL AMPLIFIER — HIGH-VOLTAGE

FEATURES

- **Output .... ±70V, ±40 mA**
- **Fully Differential FET Input**
- **Wide Supply Range .... ±15V to ±75V**
- **Input Overvoltage Protected**
- **Output Current Limited at ±65 mA**
- **Low Supply Current .... ±6.5 mA**

APPLICATIONS

- **ATE Pin Drivers**
- **Electrostatic Deflection**

GENERAL DESCRIPTION

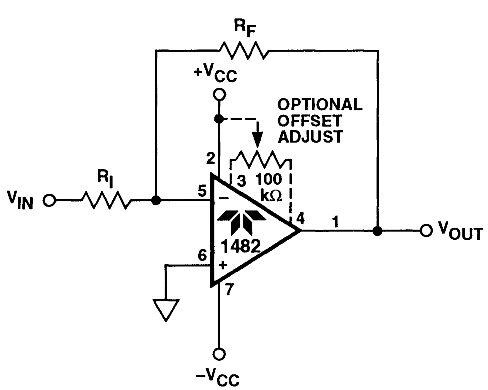
The 1482 is a high voltage operational amplifier capable of operating with supply voltages as high as ±75V, or as low as ±15V. It can provide output swings as high as ±70V with output currents to ±40 mA (short circuit limited to ±65 mA). The cascoded FET input stage is fully overvoltage protected.

This op amp features a 25V/µS slew rate and a 7.5 MHz unity gain-bandwidth. Maximum input offset voltage is ±3 mV, and minimum open loop gain is 94 dB (full load). The class AB output stage can drive up to 10,000 pF capacitive loads at closed loop gains of ten or more. The 1482 is pin and performance compatible with the BB3581, but with faster settling time.

The 1482 is packaged in an 8 pin, TO-3 package. The standard unit is specified for 0°C to +70°C operation. The 1482 High Reliability (HR) version is specified for -55°C to +125°C operation.

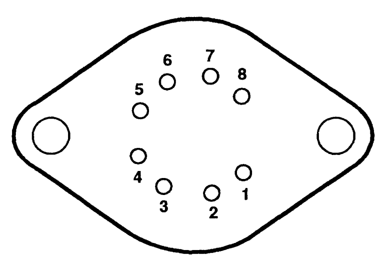
9

NORMAL INVERTING OPERATION



NOTE: The metal case is electrically isolated. It is recommended the case be grounded during use.

PIN CONFIGURATION



BOTTOM VIEW

PIN NO.	DESIGNATION
1	OUTPUT
2	$+V_{CC}$
3	OFFSET TRIM
4	OFFSET TRIM
5	–INPUT
6	+INPUT
7	$-V_{CC}$
8	NC

NC = NO INTERNAL CONNECTION

1482

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage ....±80V
V_{ID} Differential Input Voltage ....±V_{CC}
V_{ICM} Common-Mode Input Voltage ....±V_{CC}
T_C Operating Temperature Range (Case)
1482 ....0°C to +70°C
1482-HR ....–55°C to +125°C
T_{STG} Storage Temperature Range ......–65°C to +150°C
θ_{JC} Output Transistor Junction-to-Case Thermal Resistance ....12°C/W

DC CHARACTERISTICS: (Note 1) V_{CC} = ±75V, R_L = 10 kΩ, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1482 Min	1482 Typ	1482 Max	1482-HR Min	1482-HR Typ	1482-HR Max	Unit
V_{OS}	Input Offset Voltage		—	±1	**±3**	—	±1	**±3**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±15	—	—	±15	**±50**	μV/°C
I_B	Input Bias Current		—	±10	**±100**	—	±10	**±100**	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±10	—	—	±10	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain		—	108	—	—	108	—	dB
		R_L = 2 kΩ	**94**	106	—	**94**	106	—	dB
PSRR	Power Supply Rejection Ratio		**70**	94	—	**70**	94	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±60	**70**	94	—	**70**	94	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 64 dB	**±65**	±70	—	**±65**	±70	—	V
Z_{ID}	Differential Input Impedance		—	10^{11}‖6	—	—	10^{11}‖6	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
V_O	Output Voltage Swing		—	±73	—	—	±73	—	V
		R_L = 2 kΩ	**±68**	±70	—	**±68**	±70	—	V
I_O	Output Current		**±35**	±40	—	**±35**	±40	—	mA
I_{SC}	Output Short-Circuit Current	R_L =680Ω	—	±65	**±80**	—	±65	**±80**	mA
R_O	Output Resistance (DC Open-Loop)		—	100	—	—	100	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±15	—	±75	±15	—	±75	V
I_{CC}	Quiescent Supply Current		—	±6.5	**±8**	—	±6.5	**±8**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±75V, R_L = 10 kΩ, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	1482 Min	1482 Typ	1482 Max	1482-HR Min	1482-HR Typ	1482-HR Max	Unit
S_R	Slew Rate		—	25	—	—	25	—	V/μs
GBWP	Gain-Bandwidth Product	f = 100 kHz	—	9	—	—	9	—	MHz
UGBW	Unity-Gain Bandwidth		5	7.5	—	5	7.5	—	MHz
t_s	Settling Time (A_{CL} = -1)	100V step/0.1%	—	7.5	—	—	7.5	—	μs
e_n	Input Voltage Noise Density	f = 1 kHz	—	20	—	—	20	—	nV/√Hz
i_n	Input Current Noise Density	f = 1 kHz	—	—	—	—	—	—	pA/√Hz
C_L	Capacitive Load (Maximum w/o oscillation)	A_{CL} ≥ 10	10,000	—	—	10,000	—	—	pF

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TELEDYNE COMPONENTS

LOW COST MICROCIRCUIT SAMPLE/HOLD AMPLIFIER

FEATURES

- **Gain-Bandwidth Product .... 2.5 MHz**
- **Acquisition Time to 0.1% .... 2.3 µsec**
- **Slew Rate 5V/µsec**
- **Ultra-Versatile: Inverting, Non-inverting, With or Without Gain**
- **Wide Temperature Range Version Available**

APPLICATIONS

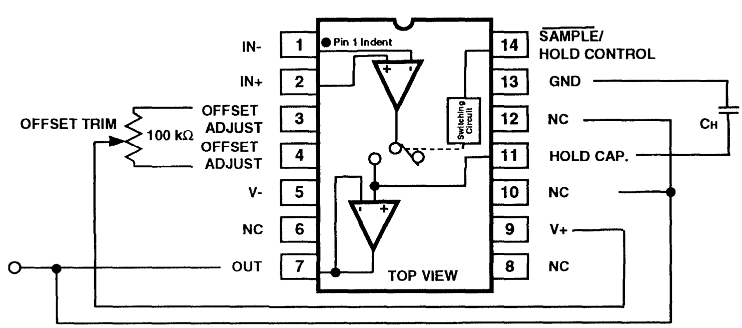
- **Data Acquisition Systems**
- **Analog Memories**
- **Data Distribution Systems**
- **Deglitch Circuits**

GENERAL DESCRIPTION

The 4856 is a high performance sample/hold amplifier for applications requiring high speed and small size. This unit has been designed for maximum versatility in circuit design and "tailoring" of specifications. With a minimum of external components, the 4856 can be used inverting or non-inverting, with or without gain. In the sample mode, the 4856 acts as an op amp and any of the standard op amp feedback circuits may be externally connected to control such parameters as gain and frequency response.

In addition, the externally connected hold capacitor enables the user to achieve the best compromise between acquisition time and droop rate for the particular application. A standard device is specified for 0°C to +75°C. The High Reliability (HR) version is specified for -55°C to +125°C temperature range.

BLOCK DIAGRAM

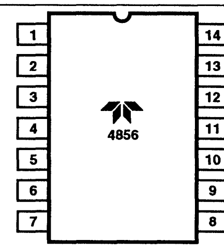


NOTES: 1. Use Cermet Potentiometer
2. C_H should be a polystyrene, mica, or teflon capacitor. The value of C_H to be determined from Figure 1.

4856

PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	-IN	8	NC
2	+IN	9	+V
3	OFFSET ADJUST	10	NC
4	OFFSET ADJUST	11	HOLD CAP.
5	-V	12	NC
6	NC	13	GND
7	OUT	14	$\overline{\text{SAMPLE}}$/HOLD CONTROL



DC CHARACTERISTICS: (Note 1) $V_{CC} = \pm15V$, Unity Gain Configuration, $C_H = 1000$ pF, $T_C = 25°C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	4856 Min	4856 Typ	4856 Max	4856-HR Min	4856-HR Typ	4856-HR Max	Unit
V_{IN}	Input Voltage Range		±10	—	—	±10	—	—	V
R_{IN}	Input Resistance		5	10	—	5	10	—	MΩ
I_B	Input Bias Current		—	±40	**±200**	—	±40	**±200**	nA
		T_{MIN} to T_{MAX}	—	—	—	—	—	**±400**	nA
I_{OS}	Input Offset Current		—	10	**50**	—	10	**50**	nA
		T_{MIN} to T_{MAX}	—	—	—	—	—	**100**	nA
V_{Os}	Input Offset Voltage		—	±2	**±4**	—	±2	**±4**	mV
		T_{MIN} to T_{MAX}	—	±3	—	—	±3	**±6**	mV
PSRR	Power Supply Rejection Ratio		**80**	90	—	**80**	90	—	dB
V_O	Output Voltage Swing	$R_L = 2$ kΩ	**±10**	—	—	**±10**	—	—	V
I_O	Output Current		**±15**	—	—	**±15**	—	—	mA
R_O	Output Resistance (DC)		—	0.15	—	—	0.15	—	Ω
A_{VOL}	Large Signal Voltage Gain	$R_L = 2$ kΩ	**88**	94	—	**88**	94	—	dB
V_P	Pedestal Voltage	V_{IN} =0V	—	10	**20**	—	10	**20**	mV
CMR	Common-Mode Range		**±10**	—	—	**±10**	—	—	V
V_{IH}	Logic "1" Input Voltage		2	—	—	2	—	—	V
V_{IL}	Logic "0" Input Voltage		—	—	**0.8**	—	—	**0.8**	V
I_{CC}	Quiescent Supply Current	Positive Supply	—	3.5	**5.5**	—	3.5	**5.5**	mA
		Negative Supply	—	2.5	**3.5**	—	2.5	**3.5**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

AC CHARACTERISTICS: (Note 1) $V_{CC} = \pm15V$, Unity Gain Configuration, $C_H = 1000$ pF, $T_C = 25°C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	4856 Min	4856 Typ	4856 Max	4856-HR Min	4856-HR Typ	4856-HR Max	Unit
t_{acq}	Acquisition Time	to 0.01% of 10V step	—	3.2	6	—	3.2	6	µs
		to 0.1% of 10V step	—	2.3	4	—	2.3	4	µs
t_{ad}	Aperture Delay Time		—	30	—	—	30	—	ns
t_{aj}	Aperture Jitter		—	5	—	—	5	—	ns
sr	Slew Rate	$V_O = 10\ V_{PP}$	3.5	5	—	3.5	5	—	V/µs
t_r	Rise Time	$R_L = 2k$	—	75	100	—	75	100	ns
GBW	Gain-Bandwidth Product		—	2.5	—	—	2.5	—	MHz

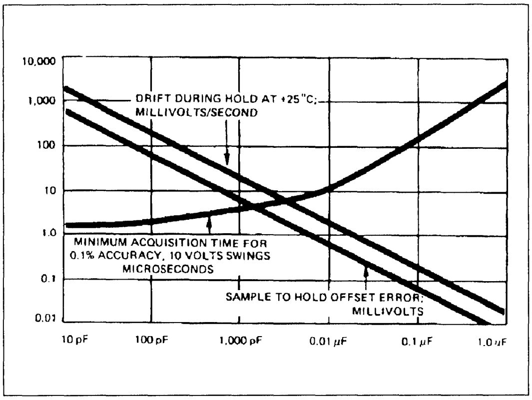


Figure 1. Typical Performance Curve

Offset Voltage Trim

The offset voltage, in either the "Sample" or "Hold" mode, may be trimmed to 0V while cycling between sample and hold with 0V input and adjusting the 100 kΩ potentiometer (Block Diagram) for 0V output. This does not, however, reduce the difference between the Sample and Hold offset voltages to zero.

Droop Rate Adjust

The Droop Rate for this unit is determined from the value of the external capacitance, (CH), shown in the Block Diagram. Figure 1 shows the curves that give the value of CH for the desired Droop Rate, as well as the effect on Acquisition Time.

To minimize errors caused by dielectric absorption, it is important to choose a polystyrene, mica, or teflon capacitor for the external hold capacitor. The external capacitor should be located close to the unit to reduce the effects of stray inductance.

Guard Ring

Leakage paths on the P.C. board and on the package surface must be minimized to reduce Droop Rate during hold. The output line forms a guard ring around the Hold Capacitance pin, which, because of the very nearly equal potentials between the output and the Hold Capacitance pin, will result in a very low leakage current. In addition, Pins 10 and 12, which are not internally connected, may be connected to the guard ring to reduce package surface leakage.

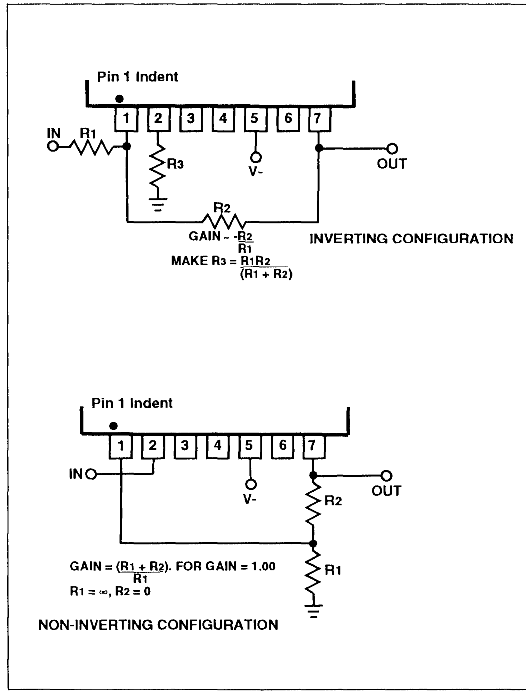


Figure 2. Pin Programming

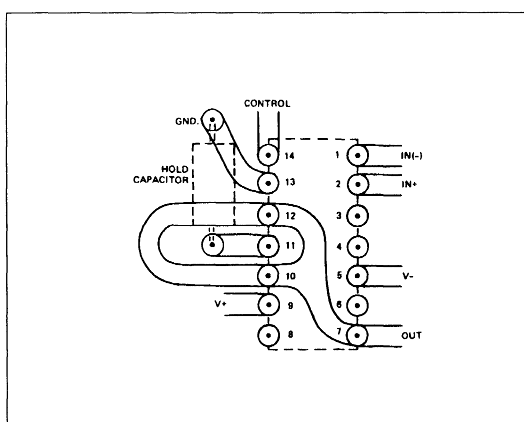


Figure 3. Guard Ring Layout (Bottom View)

9

NOTES

TELEDYNE COMPONENTS

FAST, 12-BIT SAMPLE/HOLD AMPLIFIER

FEATURES

- **Acquisition Time for a 10V Step to ±0.01%FS ......200 ns Max**
- **Sample-to-Hold Settling Time ......100 ns Max**
- **Aperture Jitter ......±50 psec**
- **Feedthrough Attenuation ......74 dB**
- **TTL Compatible**

APPLICATIONS

- **Transient Recorders**
- **Fast Fourier Analysis**
- **High Speed DASs**
- **High Speed DDSs**
- **Analog Delay and Storage**

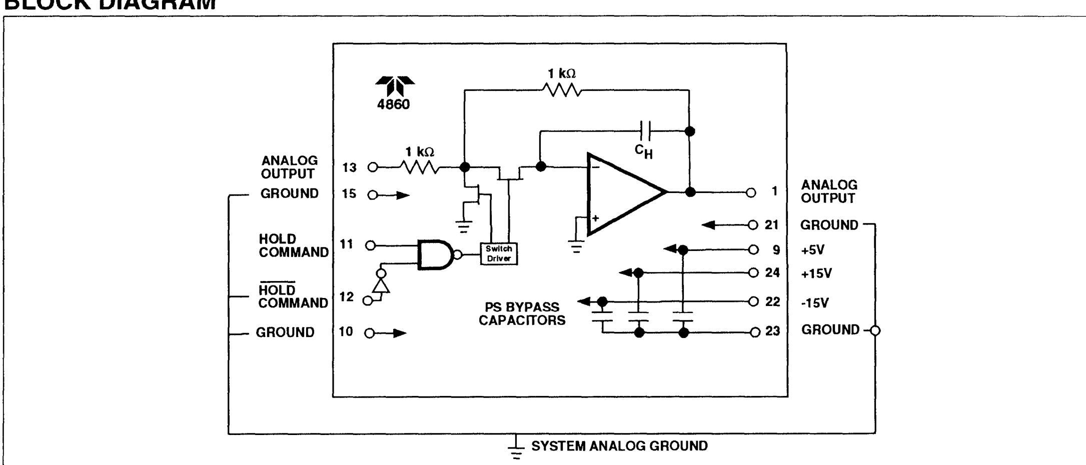
GENERAL DESCRIPTION

The 4860 is a very fast, high-resolution sample/hold (track/hold) amplifier. Its acquisition time and sample-to-hold settling time (a S/H's two throughput limiting specifications) are guaranteed to ±0.01%, unlike other S/H amplifiers that only achieve ±0.1% or ±1%. The 4860 acquires a 10V signal step to ±0.01% in 200 nsec maximum and then tracks signal components up to 16 MHz. In the track mode, offset error is typically ±0.5 mV, and gain error is typically ±0.05%. When commanded to Hold the 4860's output settles within ±0.01%FS of its final value in 100 nsec maximum. The aperture delay time is 6 nsec, aperture jitter is ±50 psec, and pedestal is a minimal ±2.5 mV. In the hold mode the output droop rate is a low 5 µV/µsec maximum and feedthrough attenuation, at 2.5 MHz, is an impressive 74 dB.

Its 24-pin, dual-in-line package, gain of -1, ±10V input/output range, and TTL compatible logic make the 4860's performance compatible with many industry standard devices. Being a second-generation design, however, the 4860 is superior to these units in almost every performance specification. Faster switching and better feedthrough attenuation are the results of our unique MOSFET switching scheme. Shorter acquisition and settling times and considerably lower droop are the result of our proprietary high speed, FET input op amp designs.

A standard device is specified for 0°C to +70°C. The High Reliability (HR) version is specified for -55°C to +125°C temperature range.

BLOCK DIAGRAM

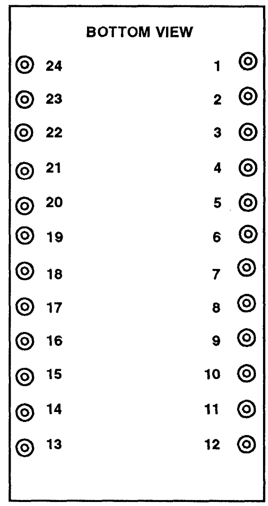


4860

PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	ANALOG OUTPUT	13	ANALOG INPUT
2	NC	14	NC
3	NC	15	GROUND
4	NC	16	NC
5	NC	17	NC
6	NC	18	NC
7	NC	19	NC
8	NC	20	NC
9	+5V SUPPLY	21	GROUND
10	GROUND	22	-15V SUPPLY
11	HOLD	23	GROUND
12	$\overline{\text{HOLD}}$	24	+15V SUPPLY

NC = No internal connection



ABSOLUTE MAXIMUM RATINGS

V_{CC} ±15V Supplies .... ±18V
V_{DD} +5V Supply .... -0.5V to +7V
V_{IN} Analog Input .... $\pm V_{CC}$
V_{ID} Digital Input .... -0.5V to +5.5V
T_C Operating Temperature Range (Case)
4860 .... 0°C to +70°C
4860-HR .... –55°C to +125°C
T_{STG} Storage Temperature Range ..... –65°C to +150°C

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, Unity Gain Configuration, C_H = 1000 pF, T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	4860 Min	4860 Typ	4860 Max	4860-HR Min	4860-HR Typ	4860-HR Max	Unit
V_{IN}	Input Voltage Range		**±10.25**	±11.50	—	**±10.25**	±11.50	—	V
Z_{IN}	Input Impedance		—	1	—	—	1	—	kΩ
V_{OS}	Input Offset Voltage	Track Mode	—	±0.5	**±5**	—	±0.5	**±5**	mV
V_{OS} TC	Input Offset Voltage vs Temperature	T_{MIN} to T_{MAX}	—	±60	**±300**	—	±60	**±300**	µV/°C
PSRR	Power Supply Rejection Ratio		—	66	—	—	66	—	dB
V_O	Output Voltage Swing	R_L = 2 kΩ	**±10.25**	±11.50	—	**±10.25**	±11.50	—	V
I_O	Output Current		**±40**	—	—	**±40**	—	—	mA
Z_O	Output Impedance		—	0.1	—	—	0.1	—	Ω
A_V	Voltage Gain		—	-1	—	—	-1	—	V/V
A_A	Gain Accuracy		—	±0.05	**±0.1**	—	±0.05	**±0.1**	%
		T_{MIN} to T_{MAX}	—	±0.05	**±0.15**	—	±0.05	**±0.15**	%
A_L	Gain Nonlinearity		—	±0.003	**±0.01**	—	±0.003	**±0.01**	%FS
A_V TC	Gain Drift		—	±0.5	**±5**	—	±0.5	**±5**	ppm/°C
V_P	Pedestal Voltage	V_{IN} = 0V	—	±2.5	**±20**	—	±2.5	**±20**	mV
V_P TC	Pedestal Drift		—	±80	—	—	±80	—	µV/°C

DC CHARACTERISTICS: (Continued)

Symbol	Parameter	Test Conditions	4860 Min	4860 Typ	4860 Max	4860-HR Min	4860-HR Typ	4860-HR Max	Unit
V_{IH}	Logic "1" Input Voltage		2	—	—	2	—	—	V
V_{IL}	Logic "0" Input Voltage		—	—	**0.8**	—	—	**0.8**	V
$\pm V_{CC}$	Voltage Range	±15V Supply	—	±3	—	—	±3	—	%
		±5V Supply	—	±5	—	—	±5	—	%
$\pm I_{CC}$	Quiescent Current	±15V Supply	—	±21	**±25**	—	±21	**±25**	mA
		±5V Supply	—	17	**25**	—	17	**25**	mA
P_D	Power Dissipation		—	730	**875**	—	730	**875**	mW

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, Unity Gain Configuration, C_H = 1000 pF, T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	4860 Min	4860 Typ	4860 Max	4860-HR Min	4860-HR Typ	4860-HR Max	Unit
t_{acq}	Acquisition Time	10V step to 0.01%FS (±1 mV)	—	160	200	—	160	200	ns
		10V step to 0.1%FS (±10 mV)	—	100	170	—	100	170	ns
		10V step to 1%FS (±100 mV)	—	90	—	—	90	—	ns
		1V step to 1%FS (±100 mV)	—	75	—	—	75	—	ns
t_s	Settling Time, Sample to Hold	to 0.01%FS (±1 mV)	—	60	100	—	60	100	ns
		to 0.1%FS (±10 mV)	—	40	—	—	40	—	ns
V_{TSH}	Sample tof Hold Transient		—	180	—	—	180	—	mVp-p
t_{ad}	Aperture Delay Time		—	30	—	—	30	—	ns
t_{aj}	Aperture Jitter		—	±50	—	—	±50	—	ps
sr	Slew Rate		—	±300	—	—	±300	—	V/µs
BW	Small Signal Bandwidth (-3 dB)		—	16	—	—	16	—	MHz
V_{HD}	Droop Rate		—	±0.5	±5	—	±0.5	±5	µV/µs
F_{RR}	Feedthrough Rejection Ratio	f = 2.5 MHz, V_{IN} = 20 Vp-p	—	74	—	—	74	—	dB

4860

APPLICATIONS INFORMATION

The 4860 is ideally suited for 12 to 14-bit high speed data acquisition/distribution systems. In a ±10V system, its ±0.01%FS (±0.005%FSR) linearity is equivalent to better than ±1/2LSB in 13 bits. Its low ±50ps aperture uncertainty enables it to accurately (±1/2LSB in 12 bits) sample signals with slew rates up to 24.4V/µsec. Its low, 5µV/µsec, output droop rate enables it to hold signals to ±1/2LSB in 14 bits for up to 125µsec. The 4860 is functionally laser trimmed at the factory to correct offset, pedestal and gain errors, and is designed to be used without external adjustments. If system requirements call for tighter accuracies, units can be selected at the factory or adjustments can be made to the A/D or D/A used with the 4860.

Grounding and Bypassing

With proper grounding and bypassing, the 4860 meets all its published performance specifications without any additional external components. The device has four ground pins (Pins 10, 15, 21 and 23), and all must be tied together and connected to system analog ground as close to the package as possible. It is preferable to have a large analog ground plane beneath the 4860 and have all four ground pins soldered directly to it. Pin 10 is particularly sensitive to ground noise because most of the digital elements that constitute the switch drive circuit are grounded to Pin 10. Noise in the switch drive circuit couples directly to the main op amp summing junction—the most noise-sensitive point in any S/H circuit. Most digital ground currents enter or leave the 4860 through Pin 10, therefore, in order to keep the output clean, care must be taken to ensure that no ground potentials exist between Pin 10 and the other ground pins. This is why Pin 10 must be tied to the analog and not the digital ground system. For the same reason, the +5V digital logic supply (Pin 9) should be kept as clean as possible. This supply (as well as the ±15V supplies, Pins 24 and 22) is bypassed to ground with a 0.01µF ceramic capacitor inside the 4860. In critical applications, additional external 0.1µF to 1µF tantalum bypass capacitors may be required.

Sample/Hold Command

A TTL logic "0" applied to Pin 11, or a logic "1" applied to Pin 12 puts the 4860 into the sample (track) mode. In this mode, the device acts as an inverting unity gain amplifier, and its output follows (tracks) its input. A logic "1" applied to Pin 11 and a logic "0" applied to Pin 12 puts the 4860 into the hold mode, and the output is held constant at the level present when the hold command was given. If Pin 11 is used to control the 4860, Pin 12 must be connected to digital ground. If Pin 12 is used to control the 4860, Pin 11 must be tied to +5V. Pins 11 and 12 each represent 1 TTL load to the digital drive circuit.

Capacitive and Resistive Loading

In order to avoid oscillations, current limiting or performance variations over temperature, the 4860's output loading has certain restrictions. To avoid oscillation the largest capacitive load is typically 250 pF. The largest recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50 pF. However, higher capacitive loads will affect both acquisition and settling time.

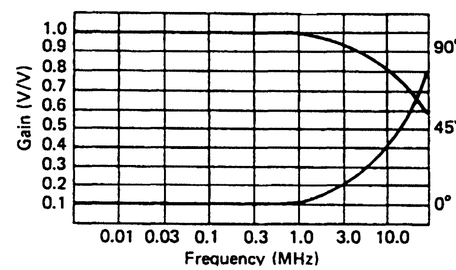


Figure 1. Track Mode Gain Amplitude and Phase Response

Aperature Jitter

The most common use of sample (track)/hold amplifiers is as an input for A/D converters to permit the accurate digitizing of signals with slew rates (frequencies) much higher than the A/D alone could handle. A rule of thumb for obtaining desired accuracy in successive approximation type A/D conversion is to ensure that the analog input signal being converted does not change by more than ±1/2LSB during the conversion. Applying this rule to any given A/D converter, one can calculate an input slew rate limit beyond which accurate digitizing is impossible. The slew rate can then be converted to a frequency limit if you choose to speak in those terms.

Example: For a 12-bit 500ns A/D converter with a ±2.5V input range, 1/2LSB is equivalent to .61 mV. If the input is not allowed to change more than .61 mV in 500 ns, the ADC's input slew rate limit is ±1.22 mV/µsec. If one were trying to accurately digitize a ±2.5V sine wave its frequency would have to be less than 77.7 Hz.

For example: dv/dt (max) = 2.5ωcosωt (Max)

1.22mV/μs = 2.5ω

1.22mV/μs = 5πf

77.7 (Hz) = f (Max)

A sample/hold in front of an A/D converter can "freeze" the converter's input signal whenever a conversion is made. Even though the S/H reduces system throughput, because the S/H acquisition time has to be added to the A/D conversion time, it makes it possible for the A/D to accurately digitize input signals with much higher slew rates (frequencies). How is this accomplished? Let's look at the timing for a conversion that uses a sample/hold input buffer.

Once a S/H (T/H) has acquired an input signal and is tracking it, the S/H can be commanded to hold at any instant. There is normally a small delay between the time the unit is commanded to hold and the time it actually holds. This delay is called aperture delay time or aperture time delay. It normally does not present a problem because the hold command signal can be advanced in time to make the amplifier hold at the correct time. Aperture delay time can vary as a given device takes sample after sample. The sample-to-sample variation in aperture delay time is called aperture jitter. Although aperture delay time is not normally a problem, aperture jitter is a problem. This is because it is impossible to control or compensate for aperture jitter. Since we have no control during the period of aperture jitter, w ould like our input signal to change as little as possible during this period. To return to our rule of thumb, we don't want the input to change by more than ±1/2LSB. Therefore, if we're using a S/H in front of an A/D converter, the slew rate limitation is no longer ±1/2LSB during the conversion time but ±1/2LSB during the aperture jitter time.

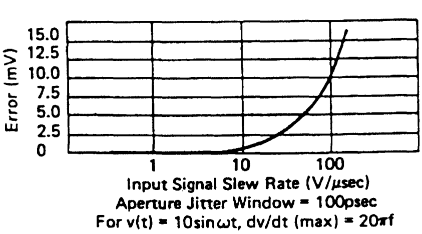


Figure 2. Accuracy Error Due to Aperture Uncertainty

The 4860 has a ±50 psec aperture jitter. This means there is a 100 psec period during which the input signal should not change more than ±1/2LSB. If, for example, you are using the 4860 S/H in front of a 12-bit A/D converter, then 1/2LSB = 0.61 mV. The input signal slew rate limitation for accurate digitizing is then 0.61 mV/100 psec or 6.1V/μsec. This is equivalent to the highest slew rate one would encounter in a ±2.5V sine wave with a frequency of 388 kHz. This is a considerable improvement over the 78 Hz sine wave that a 12-bit, 500 ns ADC could accurately digitize without a S/H. Notice that 388 kHz to 78 Hz is the same ratio as 500 nsec, the ADC's conversion time, to 100 psec, the 4860's aperture jitter.

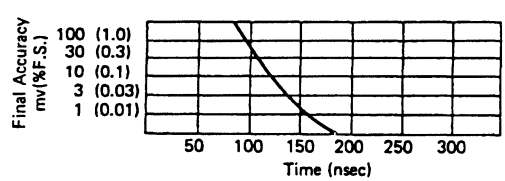


Figure 3. Acquisition Accuracy vs Acquisition Time for 10V Step

This procedure, which determines how fast a signal a given S/H permits one to digitize, assumes that the output droop rate of the chosen sample/hold is low enough to keep the A/D's input constant to within ±1/2LSB during a conversion time. It also assumes that at the input slew rate (frequency) of interest, the S/H's output is not slew rate (bandwidth) limited. Lastly, the fact that a given S/H and A/D combination can accurately digitize the fastest portions of a 388 kHz sine wave does not mean that the same combination can be used to digitize that signal for reproduction purposes. Nyquist criteria state that you have to sample a 388 kHz sine wave at twice its frequency, i.e. you have to take a sample every 1.25μsec. The 4860/ADC combination must sample at least this fast to reproduce the input.

9

Using the 4860 with A/D Converters

There are two important considerations when using S/Hs to drive successive approximation A/Ds. The first is a dual requirement—the S/H's output stage should exhibit a very low impedance compared to the A/D's input impedance, usually 1 to 10 kΩ, at frequencies up to five times the A/D's clock period; and the S/H should be able to recover from current transients in a time interval smaller than the A/D's clock period. These requirements are based on the fact that successive approximation A/D's internal D/A converter changes its output current just prior to the determination of each output bit, therefore, the S/H will be required to sink or source large, high frequency current transients and recover within one clock period. In the hold mode, the 4860's output impedance is typically 0.1Ω. Its output typically recovers (to ±0.01%) from a 2mA step in less than 100 nsec.

The second consideration involves the S/H's sample-to-hold transient settling time. If the same timing pulse that puts the S/H into the hold mode initiates the A/D conversion, the transient settling time has to be short enough to ensure that the A/D has a stable, accurate input when it makes the final decision on whether its MSB output should be a "1" or "0". This decision normally takes place one clock period after a conversion has begun.

In most applications by using the 4860 in front of a successive approximation A/D converter, the 4860's HOLD or HOLD can be driven directly from the converter's status output. The status output changes state when the converter receives a convert command, and this change can be used to drive the S/H from the track to the hold mode. The reverse change in state of the status output at the end of the conversion can also be used to set the S/H back into the track mode.

TELEDYNE COMPONENTS

OPERATIONAL AMPLIFIER — HIGH-SPEED, FET-INPUT

FEATURES

- **The Choice Device for All 0032 Applications**
- **Open-Loop Gain .... 85 dB**
- **Settling Time to ±1% .... 100 ns**
- **Slew Rate 650V/µs**

APPLICATIONS

- **High-Speed ADC Comparators**
- **ADC and SHA Integrators**
- **High-Speed Integrators**
- **Video Amplifiers**

GENERAL DESCRIPTION

The TP0032 is a high slew rate, FET-input, fully-differential operational amplifier. It features 85 dB open-loop gain, a wide bandwidth (25 MHz @ A_{CL} = +1), high-input impedance ($10^{11}\Omega$), and high-output drive capabilities.

The TP0032 can be used as a direct replacement for LH0032-type op amps and is far more capable. It features the following performance improvements:

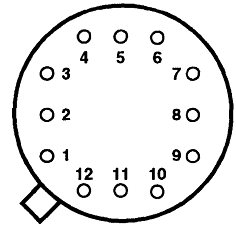
1. Increased open-loop gain; improves linearity and eliminates output voltage droop.
2. Superior second-stage biasing and decreased gain sensitivity to the transconductance of the JFET input yields faster, more consistent settling times.
3. The addition of supply current compensation over temperature improves dynamic response versus temperature.
4. Improved phase margin allows smaller compensation capacitance values to be used in low-gain applications, which means higher slew rates and faster settling times, and useful features for new designs.

The standard TP0032 is specified for –55°C to +125°C operation. The TP0032 High Reliability (HR) version is specified for –55°C to +125°C operation.

PIN CONFIGURATION

PIN NO.	DESIGNATION	PIN NO.	DESIGNATION
1	NC	7	NC
2	OUTPUT COMP	8	NC
3	BALANCE/COMP	9	NC
4	BALANCE/COMP	10	$-V_{CC}$
5	INVERTING INPUT	11	OUTPUT
6	NONINVERTING INPUT	12	$+V_{CC}$

NC = NO INTERNAL CONNECTION



BOTTOM VIEW

TP0032

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply Voltage	±18V
V_{ID}	Differential Input Voltage	±30V
V_{ICM}	Common-Mode Input Voltage	$\pm V_{CC}$
T_C	Operating Temperature Range (Case)	–55°C to +125°C
T_{STG}	Storage Temperature Range	–65°C to +150°C

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, T_C = 25°C, unless otherwise noted.

			TP0032			TP0032-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OS}	Input Offset Voltage		—	±2	**±5**	—	±2	**±5**	mV
		T_{MIN} to T_{MAX}	—	±4	—	—	±4	**±10**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±25	—	—	±25	—	μV/°C
I_B	Input Bias Current		—	±10	**±100**	—	±10	**±100**	pA
		T_{MIN} to T_{MAX}	—	±5	—	—	±5	**±50**	nA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±5	**±25**	—	±5	**±25**	pA
		T_{MIN} to T_{MAX}	—	±12	—	—	±12	**±25**	nA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain		**70**	85	—	**70**	85	—	dB
		T_{MIN} to T_{MAX}	—	83	—	**70**	83	—	dB
PSRR	Power Supply Rejection Ratio		**50**	70	—	**50**	70	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±8V	**50**	70	—	**50**	70	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 44 dB	**±10**	±12	—	**±10**	±12	—	V
Z_{ID}	Differential Input Impedance		—	10^{11}‖2	—	—	10^{11}‖2	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	10^{11}‖3	—	—	10^{11}‖3	—	Ω‖pF
V_O	Output Voltage Swing		**±10**	±13.5	—	**±10**	±13.5	—	V
I_O	Output Current		**±10**	±13.5	—	**±10**	±13.5	—	mA
I_{SC}	Output Short-Circuit Current	(Note 2)	—	N/A	—	—	N/A	—	mA
R_O	Output Resistance (DC Open-Loop)		—	90	—	—	90	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±10	±15	±18	±10	±15	±18	V
I_{CC}	Quiescent Supply Current		—	±17	**±20**	—	±17	**±20**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.
2. The TP0032 is not output short-circuit protected and neither are other vendors' 0032's.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, C_{C1} = 4 pF, C_{C2} = 100 pF, T_C = 25°C, unless otherwise noted.

			TP0032			TP0032-HR			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
S_R	Slew Rate	A_V = +1	350	650	—	350	650	—	V/μs
GBWP	Gain-Bandwidth Product	f = 100 kHz, C_{C1} = 0 pF, C_{C2} = 0 pF	—	600	—	—	600	—	MHz
UGBW	Unity-Gain Bandwidth	A_V = +1	—	25	—	—	25	—	MHz
t_s	Settling Time (A_{CL} = -1)	20V step/1%	—	100	—	—	100	—	ns
		20V step/0.1%	—	300	—	—	300	—	ns

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

APPLICATIONS INFORMATION

Wiring Recommendations

As with most high-speed op amps, the TP0032 is sensitive to circuit board layout; i.e., stray reactances. The power supplies should be bypassed as close to pins 10 and 12 as possible. Use low-inductance capacitors, such as 0.01 µF disc ceramics. Any other compensation capacitors, if used, should be located as close as possible to the appropriate pins to minimize stray capacitance. Good grounding techniques, as always, should be used.

Input Capacitance

The TP0032's input capacitance is typically 2-3 pF. To compensate for this, it is recommended that a small capacitor be placed across the feedback resistor. The value of this capacitor should be on the order of several picofarads. The exact value will vary with the effects of layout and closed-loop gain, and is therefore determined case by case.

When using the TP0032 in a noninverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This practice will divert leakage currents away from the noninverting input and reduce effective input capacitance.

Heat Sinking

When operating the TP0032 at T_A = +25°C, the case temperature will be approximately +65°C. Although the TP0032 is specified for operation without a heat sink, bias current performance may be improved with the use of a small heat sink, such as the Thermalloy 2240 or equivalent. The case is electrically isolated, so it may be connected to the heat sink. However, this will add capacitance to all pins and will probably necessitate compensation readjustment.

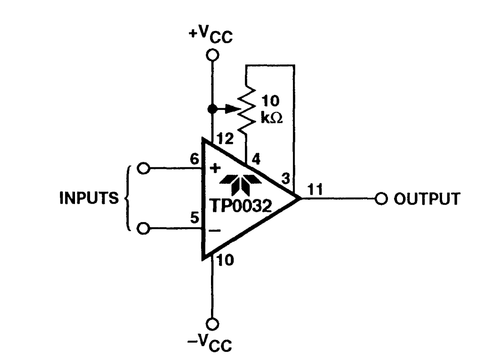


Figure 1. Offset Null

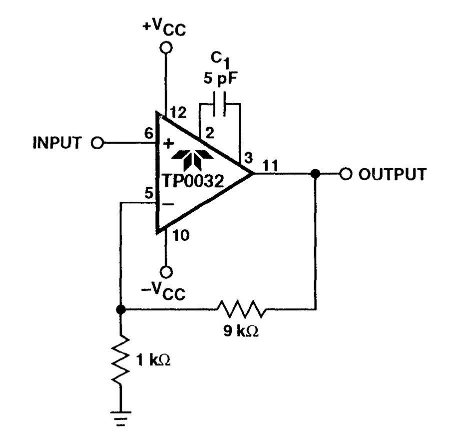


Figure 2. 10X Buffer Amplifier

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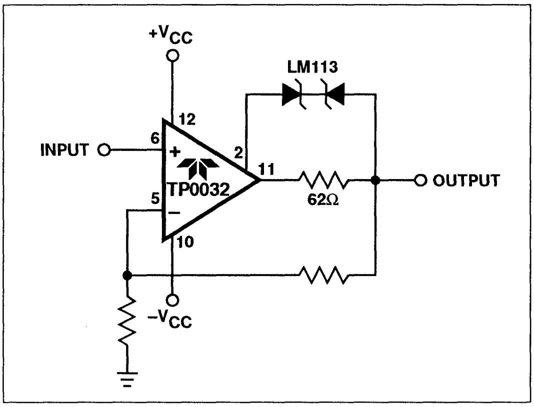


Figure 3. Output Short-Circuit Protection

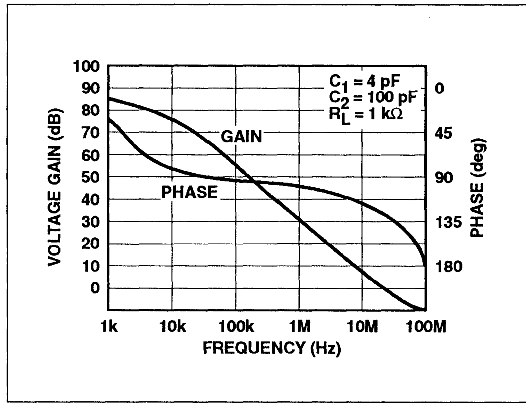


Figure 6. Bode Plot (Unity Gain Compensation)

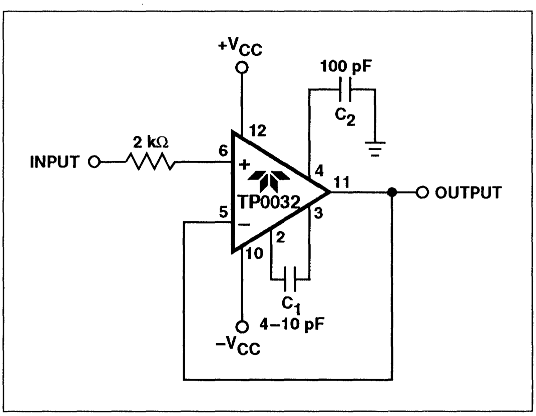


Figure 4. Unity-Gain Amplifier

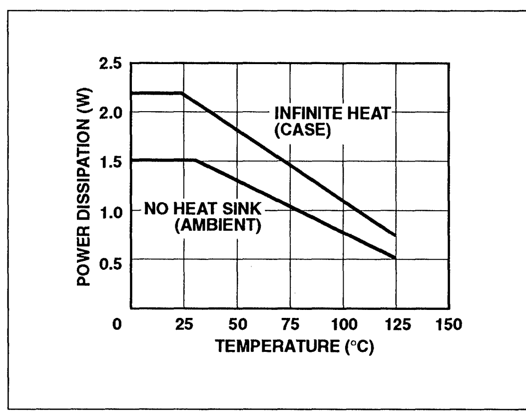


Figure 7. Maximum Power Dissipation

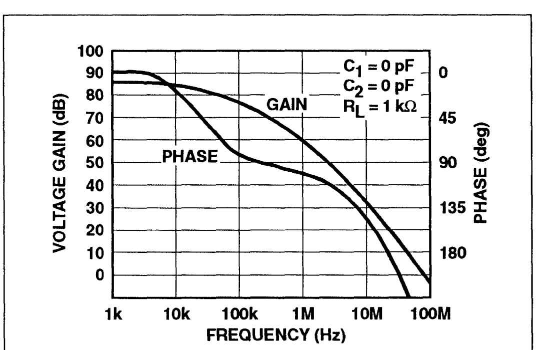


Figure 5. Bode Plot (Uncompensated)

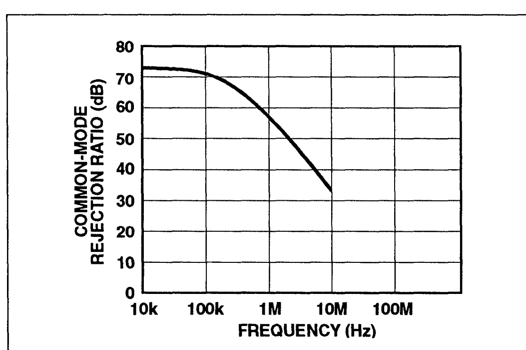


Figure 8. CMRR vs Frequency

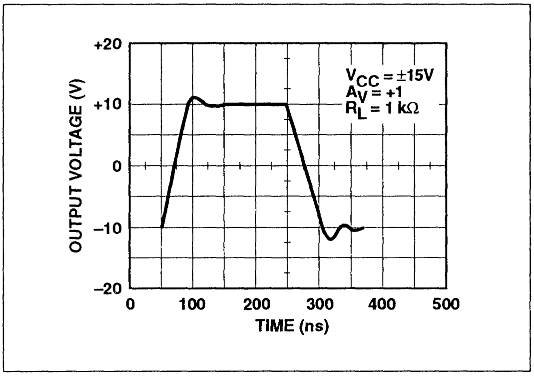


Figure 9. Large Signal Pulse Response

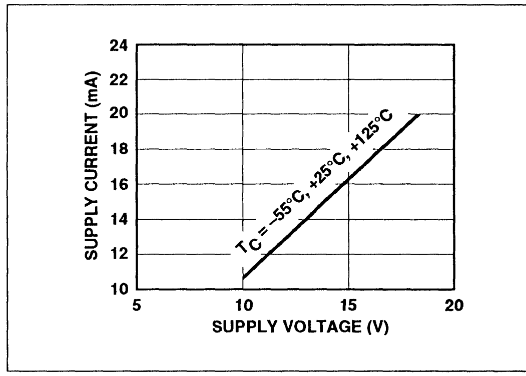


Figure 10. Supply Current vs Supply Voltage

9

NOTES

TELEDYNE COMPONENTS

HIGH-SPEED, UNITY-GAIN BUFFER/DRIVER AMPLIFIER

FEATURES

- Replaces All 0033's
- High Speed
  - Bandwidth .... DC to 100 MHz
  - Slew Rate .... 1500 V/µs
- Settling Time to ±1% (2V step) .... 25 ns
- Low Quiescent Current .... ±14 mA

APPLICATIONS

- Input-Buffering Flash ADCs
- CRT Deflection Yoke Drive
- Coaxial Line Driver
- Critical Military, Biomedical and Process Control Environments

GENERAL DESCRIPTION

The TP0033 is a high-speed, high-input impedance, unity-gain buffer amplifier that is pin, package and performance equivalent to the ubiquitous LH0033. This device matches or exceeds the performance of its counterpart in all applications, yet typically draws just ±14 mA quiescent current, versus ±20 mA typical for the LH0033.

The TP0033 has a FET input stage which provides high-input impedance ($10^{11}\Omega$), low-input bias current (0.5 nA), and low initial input offset voltage (±10 mV). The device operates with supply voltages from ±5V to ±20V (single supply operation is permissible). With nominal ±15V supplies, the TP0033 delivers a guaranteed output of ±12V into 1 kΩ. Other key large-signal specifications are 1500 V/µs slew rate and 25 ns settling time for the unit to settle a 2V step (typical "flash" ADC full-scale input) to within ±1% (±20 mV) of final value.

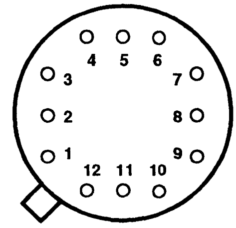
A 100 MHz bandwidth, 2.9 ns rise time and 1.2 ns propagation delay are key small-signal specifications that further demonstrate the TP0033's suitability for high-frequency, signal-buffering applications.

The TP0033 is housed in a 12-pin TO-8 can. The standard device is specified for –25°C to +85°C operation. The High Reliability (HR) version is specified for –55°C to +125°C operation.

PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	$+V_{CC}$	7	OFFSET TRIM
2	NC	8	NC
3	NC	9	$-V_{CC}$
4	NC	10	V^-
5	INPUT	11	OUTPUT
6	OFFSET PRESET	12	V^+

NC = No internal connection



BOTTOM VIEW

HIGH-SPEED, UNITY-GAIN BUFFER/DRIVER AMPLIFIER

TP0033

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}-(-V_{CC})$ Supply Voltage 40V

V_I Input Voltage .... $\pm V_{CC}$

P_D Power Dissipation (See Figure 9) 1.5W

T_C Operating Temperature Range (Case)
TP0033....................................–25°C to +85°C
TP0033-HR ....–55°C to +125°C

T_{STG} Storage Temperature Range.....–65°C to +150°C

DC CHARACTERISTICS: (Note 1) $V_{CC} = \pm15V$, $R_L = 1\ k\Omega$, $R_S = 100\Omega$, $T_C = 25°C$, unless otherwise noted.

Symbol	Parameter	Test Conditions	TP0033 Min	TP0033 Typ	TP0033 Max	TP0033-HR Min	TP0033-HR Typ	TP0033-HR Max	Unit
$A_{V/V}$	Voltage Gain		**0.96**	0.98	**1.00**	**0.96**	0.98	**1.00**	V/V
V_{OS}	Input Offset Voltage		—	±5	**±10**	—	±5	**±10**	mV
		T_{MIN} to T_{MAX}	—	—	—	—	—	**±15**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±50	—	—	±50	**±250**	µV/°C
I_B	Input Bias Current		—	±0.5	**±2.5**	—	±0.5	**±2.5**	nA
		T_{MIN} to T_{MAX}	—	—	—	—	—	**±50**	nA
PSRR	Power Supply Rejection Ratio		—	60	—	—	60	—	dB
Z_I	Input Impedance		10^{10}	10^{11}	—	10^{10}	10^{11}	—	Ω
V_O	Output Voltage Swing		**±12**	±13	—	**±12**	±13	—	V
		$R_L = 100$	**±9**	—	—	**±9**	—	—	V
		$V_{CC} = \pm5V$	—	6	—	—	6	—	VP-P
I_{SC}	Output Short-Circuit Current	(Note 2)	—	N/A	—	—	N/A	—	mA
R_O	Output Resistance (DC Open-Loop)		—	6	**10**	—	6	**10**	Ω
V_{CC}	Supply Voltage Range (Operating)		±5	±15	±20	±5	±15	±20	V
I_{CC}	Quiescent Supply Current		—	±14	**±22**	—	±14	**±22**	mA
		$V_{CC} = \pm5V$	—	±12	—	—	±12	—	mA
P_D	Quiescent Power Dissipation		—	420	**660**	—	420	**660**	mW
		$V_{CC} = \pm5V$	—	120	—	—	120	—	mW

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.
2. The TP0033 is not output short-circuit protected and neither are other vendors' 0033's.
Peak instantaneous output current must not exceed ±250 mA.
Continuous output current must not exceed ±100 mA.

AC CHARACTERISTICS: (Note 1) $V_{CC} = \pm15V$, $R_L = 1\ k\Omega$, $R_S = 50\Omega$, $T_C = 25°C$, unless otherwise noted.

Symbol	Parameter	Test Conditions	TP0033 Min	TP0033 Typ	TP0033 Max	TP0033-HR Min	TP0033-HR Typ	TP0033-HR Max	Unit
S_R	Slew Rate		1000	1500	—	1000	1500	—	V/µs
BW	Bandwidth (-3 dB)	V_{IN} = 1.0 VRMS	—	100	—	—	100	—	MHz
Φ_{NL}	Phase Non-Linearity	BW = 1 Hz to 20 MHz	—	2	—	—	2	—	°
t_s	Settling Time	2V step/1%	—	25	—	—	25	—	ns
t_r	Rise Time	$\Delta V_{IN} = 0.5V$	—	2.9	—	—	2.9	—	ns
t_{pd}	Propagation Delay	$\Delta V_{IN} = 0.5V$	—	1.2	—	—	1.2	—	ns
THD	Total Harmonic Distortion	f > 1 kHz	—	<0.1	—	—	<0.1	—	%

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

HIGH-SPEED, UNITY-GAIN BUFFER/DRIVER AMPLIFIER

APPLICATIONS INFORMATION

Offset Adjustment

The TP0033 is factory-trimmed for low initial offset voltage. This is achieved by laser trimming and is implemented by tying pin 6 (offset preset) to pin 7 (offset adjust input). If the offset needs adjusting for any reason (see "Single or Unbalanced Power Supplies"), it can be done by using the offset null scheme shown in Figure 1. If an adjustable offset is not needed, pin 7 must be tied to pin 6. (Pin 7 cannot be left open.)

Current Limiting

The output of the TP0033 is not short-circuit protected and should not exceed ±100 mA steady-state or ±250 mA peak instantaneous current. For overcurrent protection, the maximum output current of the TP0033 can be limited by the use of current-limiting resistors as shown in Figure 2, or by an active current-source circuit as shown in Figure 3. Whether or not the current is limited, pins 1 and 9 must be connected to $+V_{CC}$ and $-V_{CC}$, respectively.

Wiring Recommendations

The TP0033, like any high-speed device, is sensitive to layout inductances; therefore, ground planes are recommended. For best performance, each power supply should be individually decoupled; i.e., bypassed to ground. If pin 1 is tied directly to pin 12 and pin 9 is tied directly to pin 10 (Figure 1), connect low-inductance (0.1 µF) ceramic disc capacitors directly to pins 10 and 12 and ground them as closely as possible to the case. If pins 1 and 12 or pins 9 and 10 are not tied together, each pin should be decoupled by a low-inductance (0.1 µF) ceramic disc capacitor, grounded as close as possible to the case.

Reactive Loading

The TP0033 output can drive large (several thousand pF) capacitive loads and long, properly terminated coaxial lines without tendency to oscillate. Peak capacitive output current levels should not exceed 250 mA.

Single or Unbalanced Power Supplies

The TP0033 can operate from unbalanced power supplies, such as the +5V/–12V rails prevalent in MOS-based logic systems. An output offset voltage will result, but is correctable by the nulling method shown in Figure 1. It is predictable (with sufficient accuracy) as follows:

$$\text{Offset (V)} = (1-\text{Gain})\ (|+V_{CC}| - |-V_{CC}|)/2$$

gain is typically 0.985; therefore:

$$\text{Offset (V)} = 0.0075\ (|+V_{CC}| - |-V_{CC}|)$$

Heat Sinking

Idling in a +25°C ambient environment, the TP0033 has an approximate case temperature of +65°C. For best performance, a heat sink (Thermalloy 2240 or equivalent) is recommended, particularly for extended temperature operation.

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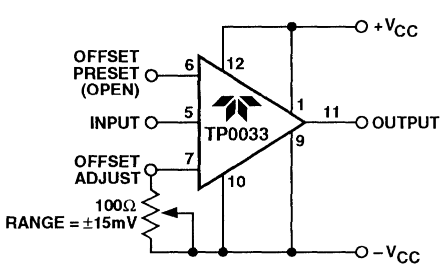
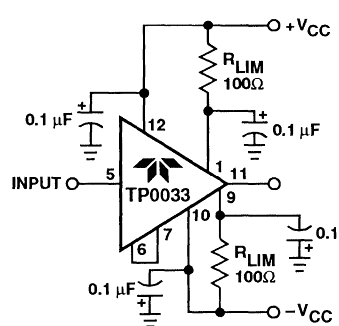


Figure 1. Basic Offset Null



$$R_{LIM} \approx \frac{+V_{CC}}{+I_{SC}} = \frac{-V_{CC}}{-I_{SC}}$$

$I_{SC} \leq 100$ mA

Figure 2. Resistive Output Current Limiting

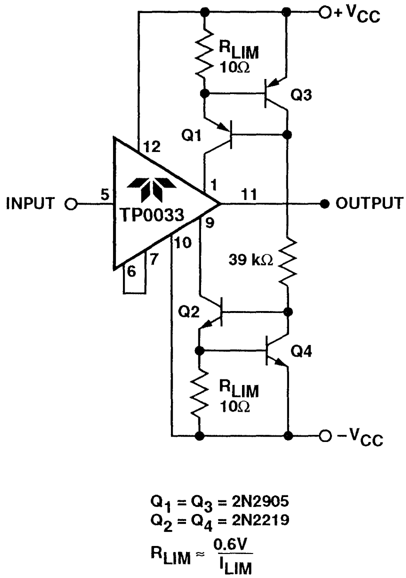


Figure 3. Active Current-Source Output Current Limiting

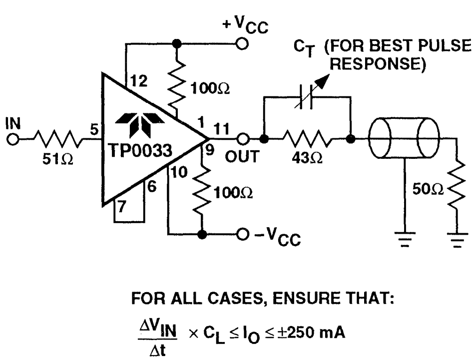


Figure 4. Coaxial Cable Driver

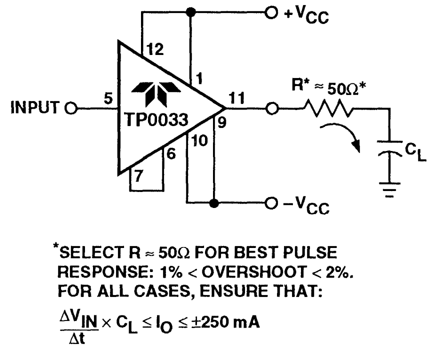


Figure 5. Capacitive Drive

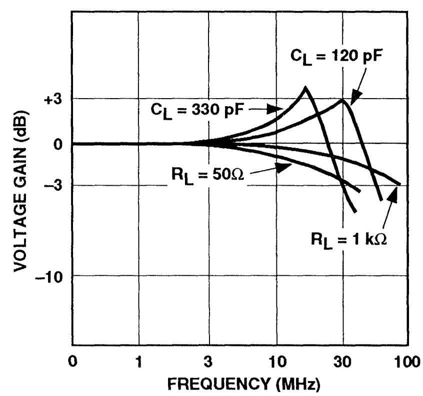


Figure 6. Frequency Response for Various Loads

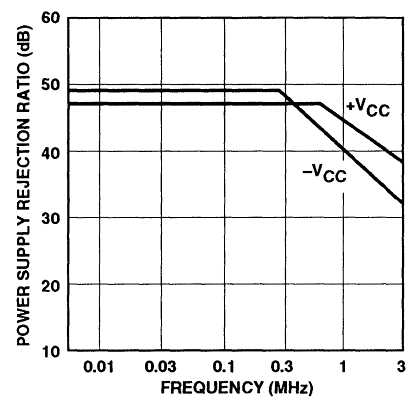


Figure 7. Power Supply Rejection Ratio

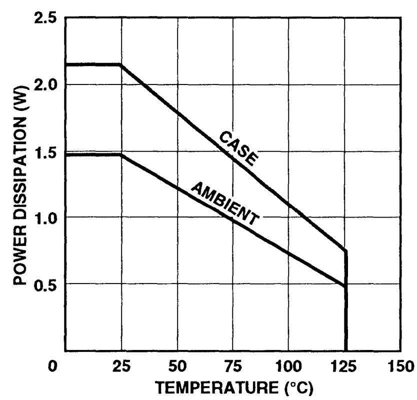


Figure 9. Maximum Power Dissipation

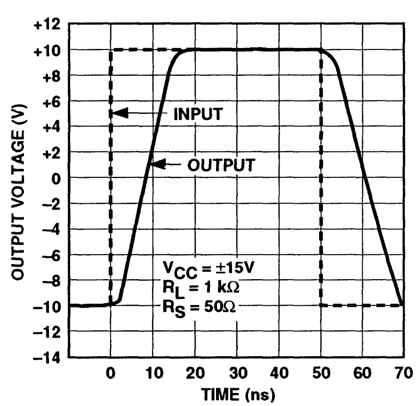


Figure 8. Large Signal Response

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NOTES

OPERATIONAL AMPLIFIER — HIGH-SPEED, WIDEBAND

FEATURES

- **Stable at Low Gain**
- **Gain Bandwidth Product .... 2 GHz**
- **Slew Rate .... 1200 V/µs**
- **Output .... ±12V, ±125 mA**
- **Low Quiescent Current .... ±14 mA**
- **Operating Temperature (-HR) .... –55°C to +125°C**

APPLICATIONS

- **Pulse Amplifiers**
- **Fast Buffer/Followers**
- **Fast D/A Converters**
- **Video Instrumentation**
- **Video Frequency Filters**

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply Voltage	±18V
V_{ID}	Differential Input Voltage	±25V
V_{ICM}	Common-Mode Input Voltage	$\pm V_{CC}$
T_C	Operating Temperature Range (Case)	
	TP3554	–25°C to +85°C
	TP3554-HR	–55°C to +125°C
T_{STG}	Storage Temperature Range	–65°C to +150°C

GENERAL DESCRIPTION

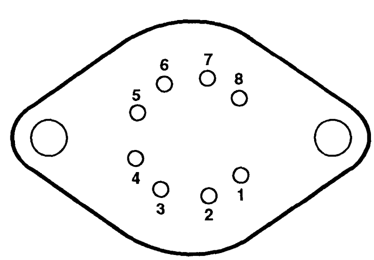
The TP3554 is a fully differential, wideband operational amplifier with 2 GHz gain bandwidth product, 1200 V/µs slew rate, and ±12V, ±125mA output. Settling time for a 10V step to 0.01% is guaranteed less than 250 ns, and external compensation allows users to optimize bandwidth, slew rate, or settling time in different applications.

The TP3554 is an improved second source to the Burr-Brown BB3554. In most applications, the TP3554 is a drop-in replacement for the BB3554, having similar bandwidth and slew rate characteristics with similar compensation. In other applications, the TP3554's superior design approach will solve many of the problems encountered with the BB3554. The TP3554's improved interior loop stability overcomes the BB3554's pronounced tendency to ring or oscillate at 120 MHz, especially at lower gains (higher compensations). The improved loop stability also results in an improved capacitive load capability. The TP3554 does not have input overload problems. Input slew rate does not affect settling time, and there are no input rise time restrictions. This eliminates many of the problems encountered in pulse-amplifier applications. The TP3554 has a much lower quiescent current drain, ±14 mA typical, (±20 mA maximum) and a lower short-circuit output current.

The standard TP3554 is housed in a TO-3 metal can and is specified for –25°C to +85°C operation. The TP3554 High Reliability (HR) version is specified for –55°C to +125°C operation.

PIN CONFIGURATION

PIN NO.	DESIGNATION
1	OUTPUT
2	$+V_{CC}$
3	COMPENSATION (PIN 3 TO 1)
4	OFFSET ADJUST
5	INVERTING INPUT
6	NONINVERTING INPUT
7	$-V_{CC}$
8	OFFSET ADJUST



BOTTOM VIEW

TP3554

DC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	TP3554 Min	TP3554 Typ	TP3554 Max	TP3554-HR Min	TP3554-HR Typ	TP3554-HR Max	Unit
V_{OS}	Input Offset Voltage		—	±0.5	**±2**	—	±0.5	**±2**	mV
V_{OS} TC	Input Offset Voltage Drift vs Temperature	Average, T_{MIN} to T_{MAX}	—	±20	—	—	±20	**±50**	μV/°C
I_B	Input Bias Current		—	±10	**±50**	—	±10	**±50**	pA
I_B TC	Input Bias Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
I_{OS}	Input Offset Current		—	±2	—	—	±2	—	pA
I_{OS} TC	Input Offset Current Drift vs Temperature	Average, T_{MIN} to T_{MAX}	Doubles every 11°C			Doubles every 11°C			—
A_{VOL}	Open-Loop Voltage Gain		**100**	106	—	**100**	106	—	dB
		R_L =100Ω	**90**	96	—	**90**	96	—	dB
PSRR	Power Supply Rejection Ratio		**80**	110	—	**80**	110	—	dB
CMRR	Common-Mode Rejection Ratio	V_{CM} = +5V/-10V	**70**	86	—	**70**	86	—	dB
CMR	Common-Mode Range (DC Linear Operation)	CMRR ≥ 64 dB	—	+8/-13	—	—	+8/-13	—	V
Z_{ID}	Differential Input Impedance		—	10^{11}‖2	—	—	10^{11}‖2	—	Ω‖pF
Z_{ICM}	Common-Mode Input Impedance		—	10^{11}‖2	—	—	10^{11}‖2	—	Ω‖pF
V_O	Output Voltage Swing	R_L = 100Ω	**±10.5**	±12	—	**±10.5**	±12	—	V
I_O	Output Current		**±100**	±125	—	**±100**	±125	—	mA
I_{SC}	Output Short-Circuit Current		—	±150	—	—	±150	—	mA
R_O	Output Resistance (DC Open-Loop)	(Note 2)	—	±100	—	—	±100	—	Ω
V_{CC}	Supply Voltage Range (Operating)		±8	±15	±18	±8	±15	±18	V
I_{CC}	Quiescent Supply Current		—	±14	**±20**	—	±14	**±20**	mA

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.
2. Typical output resistance is 20Ω at f = 10 MHz.

AC CHARACTERISTICS: (Note 1) V_{CC} = ±15V, R_L = 1 kΩ, C_C = 0 pF, T_C = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	TP3554 Min	TP3554 Typ	TP3554 Max	TP3554-HR Min	TP3554-HR Typ	TP3554-HR Max	Unit
S_R	Slew Rate	R_L = 100Ω	1000	1200	—	1000	1200	—	V/μs
GBWP	Gain-Bandwidth Product	@ A_{OL} = 10	150	225	—	150	225	—	MHz
		@ A_{OL} = 100	425	725	—	425	725	—	MHz
		@ A_{OL} = 1000	1000	2000	—	1000	2000	—	MHz
UGBW	Unity-Gain Bandwidth		—	90	—	—	90	—	MHz
t_s	Settling Time (A_{CL} = -1, C_C = 12 pF)	10V step/1%	—	40	—	—	40	—	ns
		10V step/0.1%	—	100	—	—	100	—	ns
		10V step/0.01%	—	150	250	—	150	250	ns
e_n	Input Voltage Noise Density	f = 1 kHz	—	10	—	—	10	—	nV/√Hz
C_L	Capacitive Load (maximum w/o oscillation)		—	75	—	—	75	—	pF

NOTES: 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

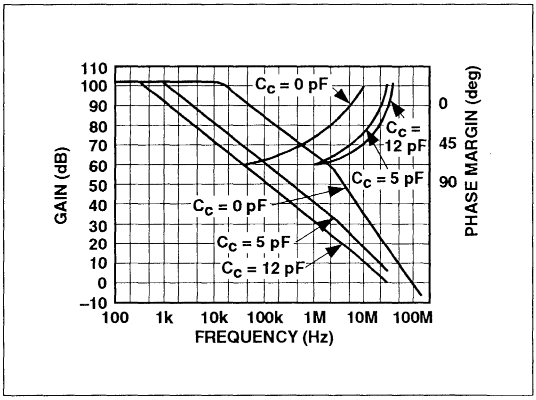


Figure 1. Bode Plot

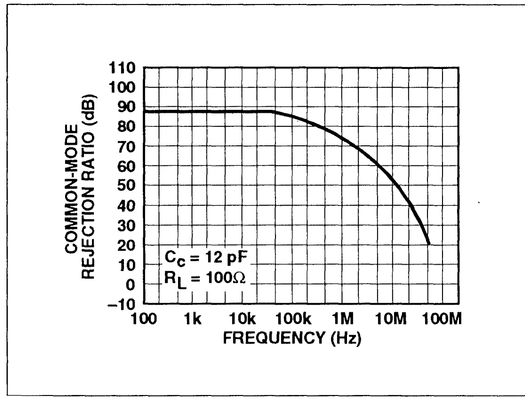


Figure 4. CMRR vs Frequency

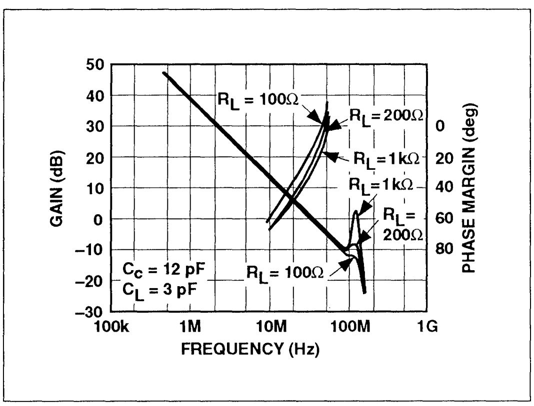


Figure 2. Gain and Phase vs Frequency for Variable R_L

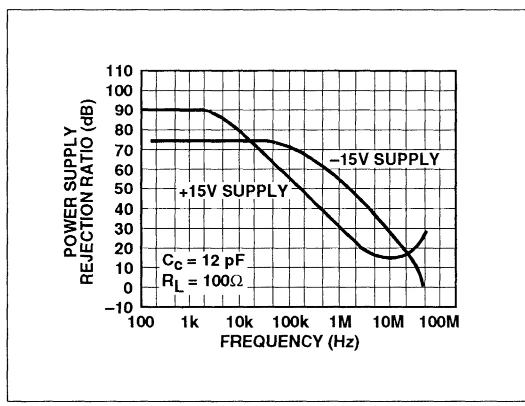


Figure 5. PSRR vs Frequency

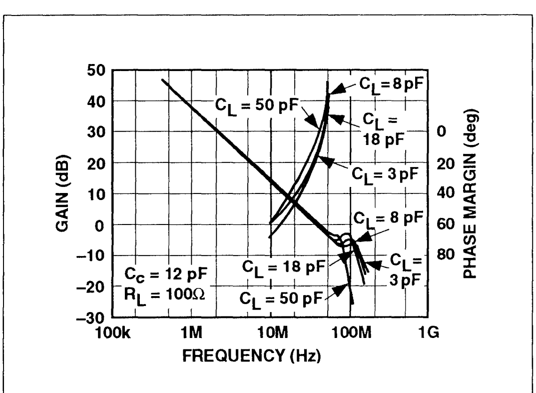


Figure 3. Gain and Phase vs Frequency for Variable C_L

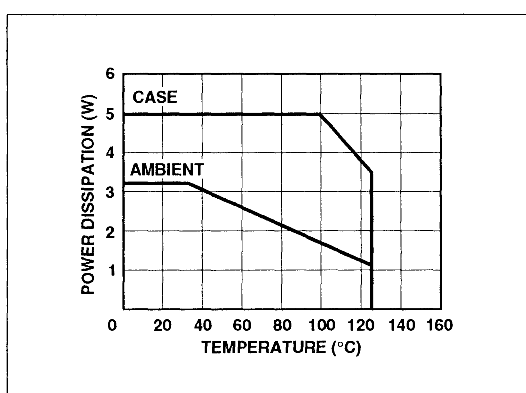


Figure 6. Maximum Power Dissipation

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APPLICATIONS INFORMATION

Layout, Grounding and Bypassing

To achieve fully-specified performance from the TP3554, careful grounding, bypassing, and wiring precautions are necessary. Grounding is the most important consideration; a ground plane is strongly recommended. The ground plane provides a low-resistance, low-inductance return path for all signals and power returns and reduces stray signal pickup. It should cover and connect all areas on the pattern side of the PC board not otherwise used.

The mechanical layout of the circuit is also very important. All circuit leads should be as short as possible. All PC board conductors should be wide to provide low-resistance, low-inductance connections, and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high-impedance nodes such as the input terminals of the amplifier. The inverting input (pin 5) is especially sensitive, and all associated connections must be short. Stray signal coupling from the output to the inputs or to pin 8 (see "Optional Offset Adjustment") should be minimized. Low resistor values should be used (values less than 5.6 kΩ are recommended). This practice will give the best circuit performance because the time constants formed with the circuit capacitances will be minimized and have little effect on amplifier performance.

Each power supply lead should be bypassed to ground as near to the amplifier pins as possible. The combination of a 1 µF tantalum capacitor in parallel with a 0.01 µF ceramic capacitor forms a suitable bypass. In inverting applications it is recommended that pin 6 (noninverting input) be grounded rather than connected to a bias-current-compensating resistor. This ensures a good signal ground at the noninverting input. A slight offset error will result; however, if the resistor values used are small, the offset error (due to bias current offset) will be minimal.

It is recommended the TP3554's case not be grounded during use (though it may be grounded, if desired). There is no internal connection to the case; however, a grounded case will add a slight capacitance to each pin. In an already functional circuit, grounding the case will probably require slight compensation adjustment and the compensation capacitor values may be slightly different from those indicated in the typical performance curves.

Optional Offset Adjustment

If the TP3554's guaranteed offset error is too large for a particular application, the initial offset may be adjusted to zero by connecting a 20 kΩ linear potentiometer between pins 4 and 8, with the wiper connected to the positive supply, as shown in Figure 7. A small, noninductive potentiometer is recommended. The leads connecting the potentiometer to pins 4 and 8 should be less than 6 inches long to avoid stray capacitance and stray signal pickup. Stray coupling from the output (pin 1) to offset adjust pin 4 has the effect of negative feedback; to pin 8 the effect is positive feedback and should be avoided.

Compensation

The TP3554 uses external frequency compensation to optimize bandwidth, slew rate, or settling time for particular applications. The bode plot (Figure 1) shows curves for several different compensation capacitors. In addition, several typical circuits are shown with recommended compensation for different applications. The primary compensation capacitor (C_C) is connected between pins 1 and 3. As the performance curves show, higher closed-loop gain configurations require less capacitance and improved gain bandwidth will be realized. Note that a compensation capacitor is not required for closed-loop gains above 35 dB.

The flat, high-frequency response of the TP3554 may be preserved and any high-frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop high-frequency transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2 pF), and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, thereby avoiding peaking, and preserving phase margin (resistor values less than 5.6 kΩ are recommended). The necessary feedback capacitance value is strongly dependent on circuit layout and closed-loop gain. It will be typically 2 pF for a clean layout using low value resistors (1 kΩ) and up to 10 pF for circuits using larger resistances.

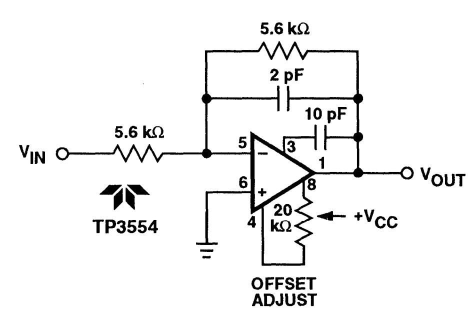

Figure 7. Unity Gain Inverter

Slew Rate

Slew rate is dependent upon compensation. Decreasing the compensation capacitor value will increase the available slew rate. Stray capacitances may have the same effect as the compensation capacitor. To avoid limiting the slew rate performance, stray capacitances should be minimized.

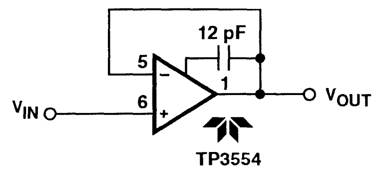

Figure 8. Follower

Heat Sinking

The TP3554 does not require a heat sink for operation in most environments. However, the use of a heat sink reduces the case temperature rise and results in lower junction operating temperatures. At extreme temperatures and under full load conditions, a heat sink will be necessary (as indicated in Figure 6). When heat sinking the TP3554, it is recommended the heat sink be connected directly to the amplifier case and the combination not be connected to the ground plane. The addition of a heat sink to an already-functional circuit will probably require slight compensation adjustment for optimum performance, due to the change in stray capacitances. The added stray capacitance to each pin from the heat sink will depend on the thickness and type of heat sink used.

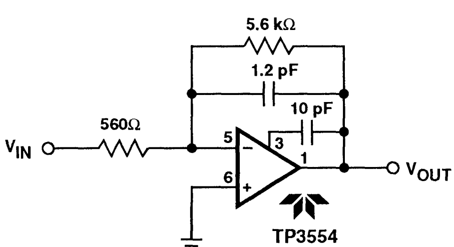

Figure 9. Inverting Gain of 10 Amplifier

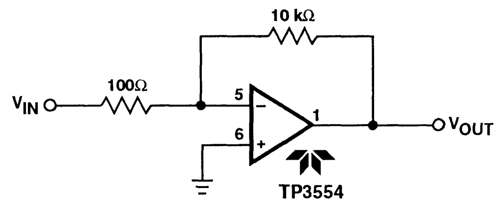

Figure 10. Inverting Gain of 100 Amplifier

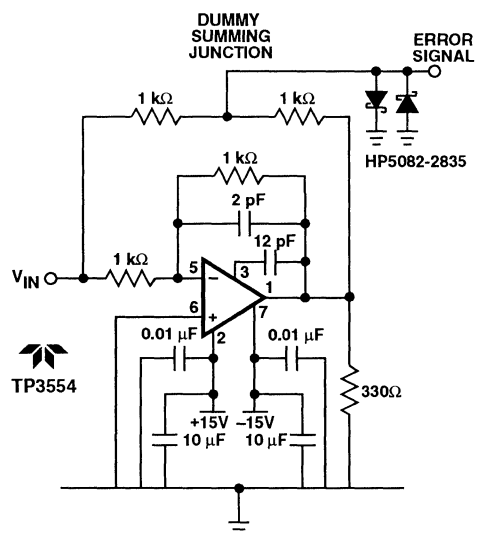

Figure 11. Typical Settling Time Test Circuit

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NOTES

Section 10

Video Display Drivers

TELEDYNE COMPONENTS

MONOLITHIC, HIGH VOLTAGE VIDEO DRIVER FOR CRT MONITORS

FEATURES

- Rise Time into a 6pF load 2.4ns
- Output Signal ....50V p-p
- Linear Variable Gain ....0 to 100
- 24-Pin Power-Tab Package

APPLICATIONS

- High Resolution Monochrome Displays
- High Resolution RGB Displays (Three Packages)

GENERAL DESCRIPTION

The 1900 is a high performance monolithic variable gain transconductance amplifier with a high voltage open collector output capable of driving a video display (CRT cathode) directly. Typical rise times of 2.4ns are achieved using a peaking inductor with a 200Ω load resistor and a 6pF total load (CRT and parasitic capacitance).

Differential inputs and a linear adjustable gain stage with an output offset adjustment make the 1900 versatile and well suited for many applications. The TTL BLANK input will set the output to a pre-determined black level independent of signal input.

The 1900 is available in a 24-pin DIP power-tab package. A suitable heat sink must be attached to maintain the junction temperature with the recommended operating range.

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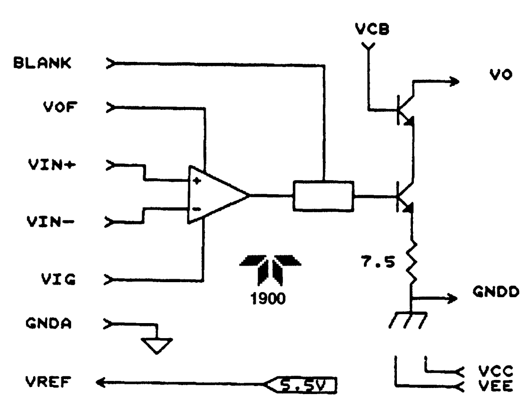
FUNCTIONAL DIAGRAM

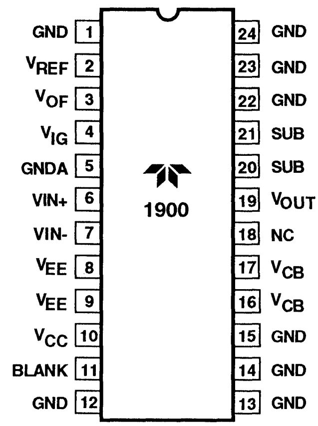


MONOLITHIC, HIGH VOLTAGE VIDEO DRIVER FOR CRT MONITORS

1900

PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	GND	24	GND
2	V_{REF}	23	GND
3	V_{OF}	22	GND
4	V_{IG}	21	SUB
5	GNDA	20	SUB
6	$V_{IN}+$	19	V_{OUT}
7	$V_{IN}-$	18	NC
8	V_{EE}	17	V_{CB}
9	V_{EE}	16	V_{CB}
10	V_{CC}	15	GND
11	BLANK	14	GND
12	GND	13	GND



NC = NO INTERNAL CONNECTION

ABSOLUTE MAXIMUM RATINGS* T_A = 25°C unless otherwise noted.

T_{JMAX}	Operating Temperature Range (Junction)	+150°C
T_{STG}	Storage Temperature	-55°C to +150°C
V_{VAA}	Output Signal Supply, wrt V_{VCB}	65V
V_{VCB}	Common Base Supply	20V
V_{VCC}	Positive IC Supply	12V
V_{VEE}	Negative IC Supply	-12V
V_{DIFF}	Differential Input Voltage, Signal	2V
V_{CM}	Common Mode Input Voltage, Signal	±2.0V
V_{VIG}	Gain Input Voltage	6V
V_{VOF}	Offset Input Voltage	6V
V_{BLANK}	Blank Input Voltage	6V
IV_{REF}	Reference Output Current	-5mA
T_S	Lead Temperature (solder <10 sec)	+260°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance (Junction to Case)	+6C/W

*An absolute maximum rating defines a bias, mechanical stress, or environmental condition beyond which the device may become unserviceable. The 1900 is static sensitive. Proper handling techniques for static-sensitive parts should be employed.

TYPICAL POWER CONSUMPTION T_A= 25°C Power Dissipation at V_{VAA} = 70V, R_L = 200Ω

V_O - V_{BLACK}	Duty Cycle %	IC P_D (Watts)	Load P_D (Watts)	Total P_D (Watts)
0	0	1.6	0	1.6
35	100	7.8	6.1	13.9
35	80	6.5	4.9	11.4
50	80	5.6	10	15.6

MONOLITHIC, HIGH VOLTAGE VIDEO DRIVER FOR CRT MONITORS

AC ELECTRICAL CHARACTERISTICS: V_{EE} = -10.5V, V_{CC} = +10V, V_{AA} = +70V, R_L = 200Ω, V_{BLANK} = 0.4V, $V_{IN} \leq$ 725mV, TA = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BW_{3dB}	Bandwidth, 3dB	V_{VOF} = 0V, R_L = 50Ω	200	—	—	MHz
t_r	Rise Time, Output	R_L = 0, $t_{r(VIN)}$ = 400ps	—	1.75	—	ns
		R_L = 200Ω, $t_{r(VIN)}$ = 1ns, C_L = 6pF (Note 1)	—	2.04	2.8	ns
t_s	Settling Time	90% point to 100% ±2%, no peaking network, C_L = 3.5pF	—	—	6	ns
gm	Transconductance	V_{VIG} = 5.0V	400	—	600	mS (Note 2)
		V_{VIG} = 1.0V	70	—	110	mS
		V_{VIG} = 0.0V	-25	—	25	mS
LE_A	Amplifier Linearity Error	V_{VIG} = 4.0V, V_{VOF} = 1.0V	—	—	±2	%GS (Note 3)
LE_{GA}	Gain Adjust Linearity Error	V_{VIN} = 0.20V, V_{VOF} = 1.0V	—	—	±2	%
TD	Thermal Distortion		—	—	±2	%
R_{VIN}	Signal Input Impedance	V_{VIN} = 0.0V	10k	20k	—	Ω
C_{VIN}	Signal Input Capacitance	V_{VIN} = 0.0V	—	2	—	pF

NOTES:
1. Total load capacitance on the output node of the IC including approximately 3pF load capacitor, 2pF parasitic board capacitance, and 1pF parasitic probe capacitance, with a peaking inductor as shown in the typical connection diagram.
2. "S" - Siemens (I/V).
3. "%GS" means percent of grey scale, referring to RS-343 standard video levels.

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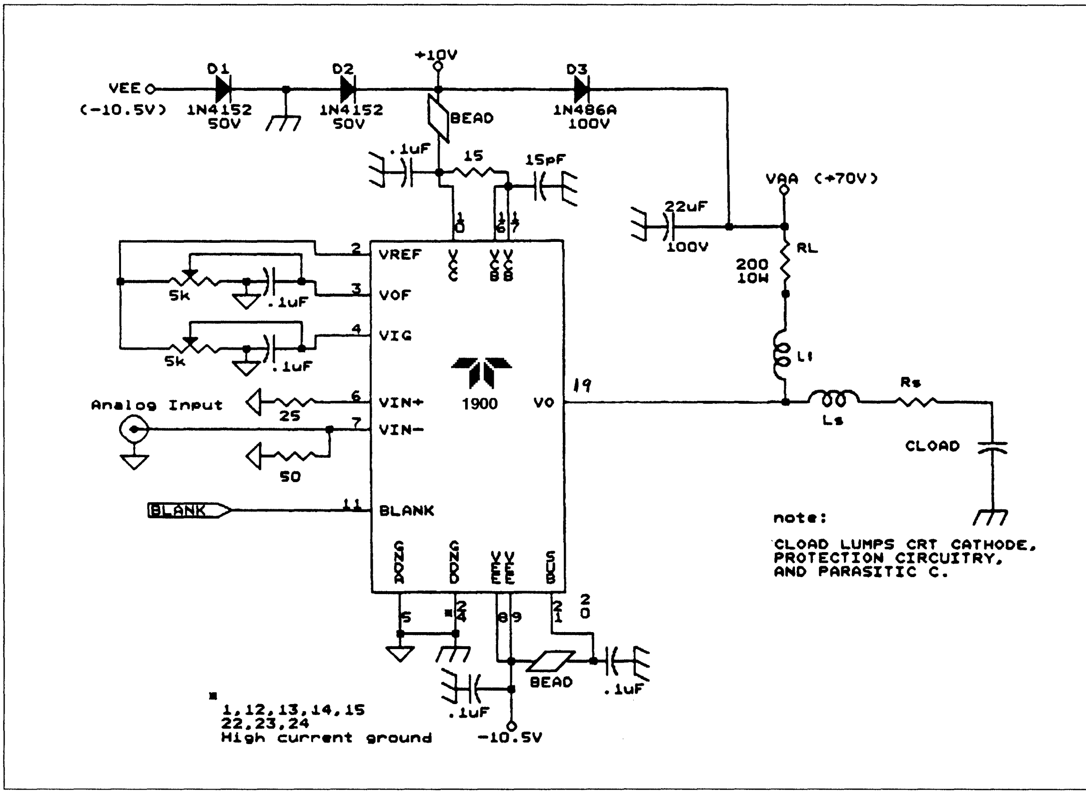
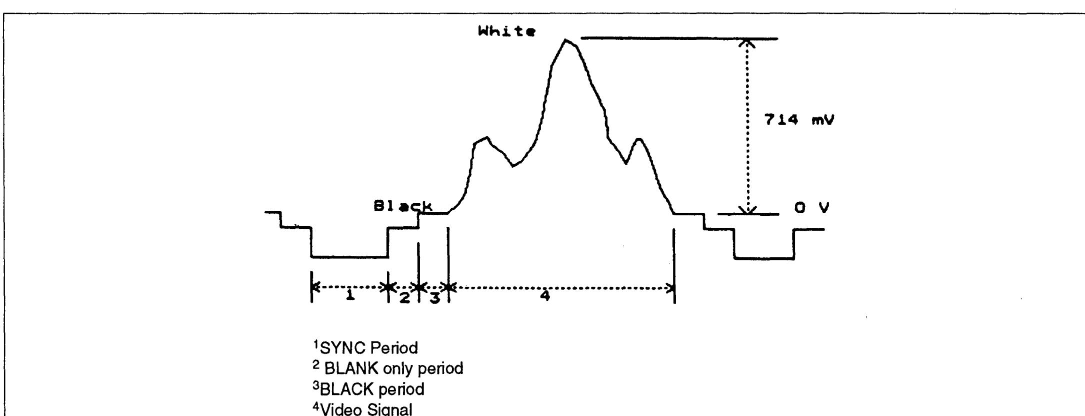
DC ELECTRICAL CHARACTERISTICS: V_{EE} = -10.5V, V_{CC} = +10V, V_{AA} = +70V, R_L = 200Ω, V_{BLANK} = 0.4V, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{REF}	Reference Output Voltage	I_O = 2mA	5.25	—	5.75	V
I_{VCC}	Positive Supply Current		40	—	70	mA
I_{VEE}	Negative Supply Current		-65	—	-100	mA
I_{VCB}	Common Base Supply Current		21	—	40	mA
I_{BLANK}	Blank Input Current	V_{BLANK} = 0.4V	-600	—	-400	µA
		V_{BLANK} = 2.4V	-400	—	-200	µA
I_{VOF}	Offset Adjust Input Current	V_{VOF} = 1V	0.5	—	10	µA
I_{VIG}	Gain Adjust Input Current	V_{VIG} = 5V	0.5	—	10	µA
I_{VIN}	Signal Input Current	V_{VIN} = 0V	-50	—	50	µA
I_O	Output Current	V_{BLANK} = 2.4V, V_{VOF} = 1.0V	-1	—	1	mA
		V_{BLANK} = 2.4V, V_{VOF} = 3.0V	-1	—	1	mA
		V_{VIN} = 0.0V, V_{VOF} = 0.0V, V_{VIG} = 4.0V	—	—	25	mA
		V_{VIN} = 0.0V, V_{VOF} = 5.0V, V_{VIG} = 0.0V	80	—	120	mA
$\Delta I_O/\Delta T$	Output Current vs Temperature	T_A = +25°C to +70°C	-2	—	2	mA
$\Delta I_O/\Delta VIG$	Output Current vs Gain Adjust	V_{VIN} = 0V, ΔV_{VIG} = 5.0V	-10	—	10	mA
$\Delta I_O/\Delta VIN$	Output Current vs Signal Adjust	V_{BLANK} = 2.4V, ΔV_{VIN} = 0.3V	-1	—	1	mA
CMRR	Common Mode Rejection Ratio	V_{CM} = ±0.5V	—	40	—	dB
PSRR	Power Supply Rejection Ratio	V_{VEE}, V_{VCC} = ±5%	25	30	—	dB

1900



Typical Connection Diagram



Typical Video Signal

MONOLITHIC, HIGH VOLTAGE VIDEO DRIVER FOR CRT MONITORS

APPLICATIONS INFORMATION

V_{IN}+, V_{IN}-

V_{IN}+ and V_{IN}- are the analog input pins. It is recommended that signals applied to these inputs be kept within ±1.3V with respect to ground. The input pins accept RS-343 signals of V_{VIN} = ±0.714mV p-p, and will operate properly with common mode range of ±0.5V with respect to ground (excluding signal). Although large offsets can be handled safely without damage to the device, output linearity suffers and therefore is not recommended.

V_{IG}

V_{IG} is the overall DC gain control that will vary the device gain from 0 to 80. An internal reference supply, V_{REF} (Pin 2), provides the 5V nominally needed to drive the gain and offset inputs (see typical connection diagram). Normally a 5kΩ potentiometer between V_{REF} and ground varies the gain, but an external source can be used, instead of V_{REF}, with some additional degradation of gain stability with temperature.

Gain control through V_{IG} is a linear relationship. Zero to 100% of the gain range of 0 to 100 is achieved by varying this input from 0 to 5 volts. This yields the following relationship for overall voltage gain of this device (for $I_O \le 250mA$):

$$V_{AA} - V_O = V_{IN} * g_m * R_L$$

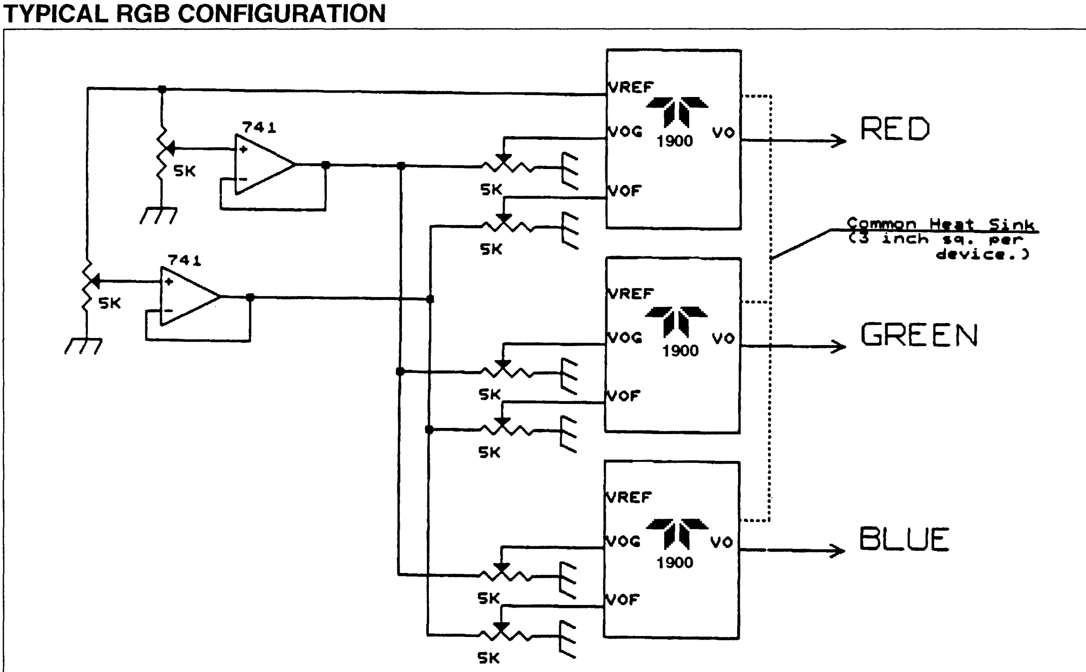
$$V_{AA} - V_O = V_{IN}(V)\ (V_{IG}(V) * 0.1 * R_L)$$

The overall gain of this device can vary by ±20% due to normal process variations of internal components (<150ppm/°C). If multiple devices are used in a system provisions should be made so that they all track thermally (i.e., a common heat sink), to offset any changes with varying ambient conditions.

V_{OF}

V_{OF} is an input control which sets the output quiescent current and therefore the output offset voltage (see Black level). Output quiescent current can be adjusted from 5mA to 55mA when V_{OF} is adjusted from 0 to 5.5V. Normally adjustment is done by using a 5kΩ potentiometer between V_{REF} and ground (see typical application diagram).

TYPICAL RGB CONFIGURATION



For color tracking the output reference voltage of one device should be buffered and used to drive all three devices. The monolithic construction of this device will allow tracking from chip to chip. To ensure uniform temperature in multi-chip circuits, a single heat sink should be used.

BLANK

When asserted (Blank = TTL High), this input disables the video signal and allows the output to rise to the predetermined blank level independent of the V_{OF} control when V_{OF} is between 0 to 3V. Above 3V there is some interaction between V_{OF} and the Blank level. Blank is independent of the input signal.

BLACK

Black level is the output voltage developed across the external resistor load that is achieved with 0V video input. This level can be modified by the quiescent operating point setup at the V_{OF} input (Pin 3). Adjustments for output current from 5mA to 55mA are easily made by varying the bias as V_{OF} from 0V to 5.5V.

V_{REF}

V_{REF} is a bias reference made available for ease in adjusting the offset, and gain inputs. This is a zener reference with a nominal output voltage of 5.5V ±5% which can source up to 4mA.

V_{CB}

The output stage consists of a common-base high-voltage stage and a high-speed low voltage current amplifier in a cascode arrangement. The V_{CB} input is the base connection to the common base device of this stage. Care should be taken to provide a stable DC voltage at this point of nominally +10V. High frequency compensation at this input is required to avoid output oscillations. A series 15Ω resistor with a 15pF capacitor to ground is recommended (see typical connection diagram). Smaller values of this RC combination will improve output rise/fall times, but can cause output oscillations near 330MHz.

SUB

SUB is the internal connection to the substrate and must be connected to V_{EE}, the most negative voltage applied to the device. Proper bypassing of the substrate supply, SUB (Pins 20,21) and the V_{EE} supply (Pins 8,9) is required to prevent output oscillations.

V_O

The output of the 1900 is an open collector of a cascode circuit. This output works with nominal output supplies of V_{AA} = +70V. The high voltage supply must be greater than any applied V_{CB} voltage for proper operation. The 1900 drives loads up to 250mA. Optimum performance can be achieved when a peaking network is used (see typical connection diagram).

Power Supply

A +10V and -10.5V supply are required for proper operation. These supplies can be set at ±12V for convenience but this will add additional heat through power dissipation internal to the package. The high voltage supply can be any voltage above the V_{CB} supply, but not greater than V_{CB} plus 65V. To achieve good performance from the 1900, close attention to high frequency grounding practices and printed circuit board layout is mandatory.

Supply Sequencing

Power supply sequencing is important to avoid internal device latch-up. To avoid sequencing problems external diodes should be placed from V_{EE} to ground, from ground to V_{CC} and from V_{CC} to the output supply V_{AA} (see typical connection diagram). With the external diodes in the circuit the most negative supply, V_{EE}, should be turned on first.

Power Dissipation

The 1900 dissipates a large amount of power due to different speed and load driving requirements. The Power-Tab package provides a low thermal resistance path from the chip to an external heat sink. Care should be taken in the board design to provide sufficient heat sinking capacity to allow operation over the intended operating range. When mounting to a chassis the device tab (heat sink) is attached to V_{EE} (-10.5V). It is recommended that a low thermal resistance insulator be used when attaching to a grounded chassis.

Initial Step

Initial setup of the device requires proper setup of the V_{OF} and V_{IG} inputs for balanced rise/fall times. If too little quiescent current is allowed it will slow the output rise time and limit eventual bandwidth.

TELEDYNE COMPONENTS

1902

HIGH-VOLTAGE VIDEO DRIVER FOR CRT MONITORS

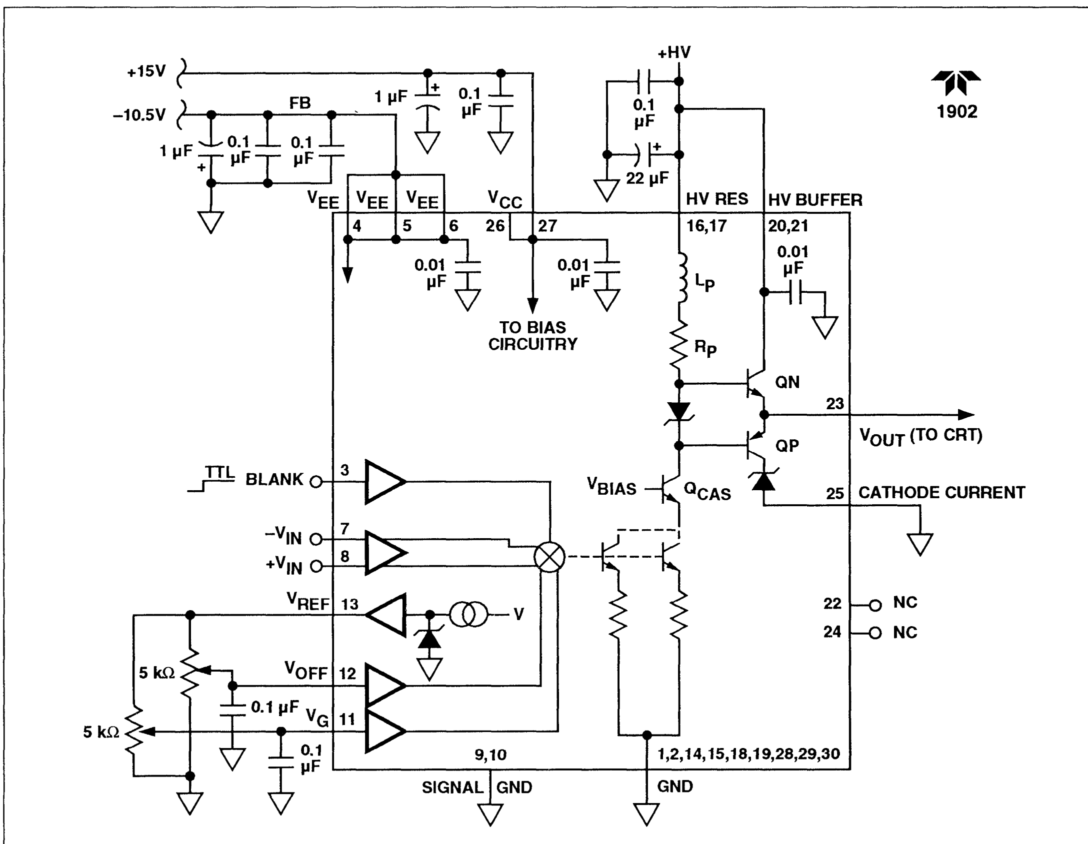
FEATURES

- Output Signals Into 10 pF .... 90 $V_{P\text{-}P}$
- Rise and Fall Times @ 50 $V_{P\text{-}P}$ .... 2.5 ns
- Linear Gain Adjustment for Matching
- Versions Available to Match Specific CRT Requirements

APPLICATIONS

- CRT Monitors
  - — Projection
  - — High-Resolution Monochrome
  - — High-Resolution RGB

STANDARD CONFIGURATION DIAGRAM



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1902

GENERAL DESCRIPTION

The 1902 is a high-performance, high-voltage amplifier designed to drive the cathode in high-resolution, high-brightness CRT monitors and projection displays.

The 1902 is replete with differential inputs, blanking control, linearly-adjustable gain stage, adjustable offset, and a differential emitter-follower output stage. The 1902 is capable of driving 10 pF to 20 pF loads, can be driven directly from a standard video DAC, and is RS170 and RS343 compatible.

The 1902 has three variants for different applications. The internal high-voltage resistor and output transistors are varied to strike the optimum balance between output voltage from 40V to 90V, and rise/fall times from 2.2 ns to 4.5 ns. The 1902-0 has no internal high-voltage resistor, thereby allowing the designer to select a high-voltage resistor to suit the specific application.

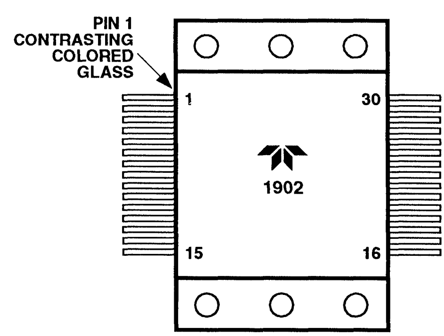
The 1902 is housed in a hermetically-sealed, 30-pin flat pack with 50-mil center pins on two sides. It has mounting flanges suitable for 4-40 screws. The 1902-X is specified for -25°C to +85°C operation. The 1902-X-HR is specified for –55°C to +125°C operation.

PIN CONFIGURATION

PIN NO.	DESIGNATION	PIN NO.	DESIGNATION
1	GND	30	GND
2	GND	29	GND
3	BLANK	28	GND
4	V_{EE}	27	V_{CC}
5	V_{EE}	26	V_{CC}
6	V_{EE}	25	GND
7	$-V_{IN}$	24	NC
8	$+V_{IN}$	23	V_{OUT}
9	GND	22	NC
10	GND	21	HV BUFFER
11	V_{GAIN}	20	HV BUFFER
12	V_{OFF}	19	GND
13	V_{REF}	18	GND
14	GND	17	HV RESISTOR
15	GND	16	HV RESISTOR

HV = HIGH VOLTAGE
NC = NO INTERNAL CONNECTION

30-Pin Flat Package



ABSOLUTE MAXIMUM RATINGS

V_{HV}	Pull-Up Resistor Supply	(V_{HV} Max +5V)
V_{CC}	Positive IC Supply	+17V
V_{EE}	Negative IC Supply	–12V
V_{IDF}	Differential Input Voltage	+2V
V_{ICM}	Common-Mode Input Voltage	±2V
V_{IG}	Gain Adjustment Input Voltage	+6V
V_{IOS}	Offset Adjust Input Voltage	+6V
V_{BLANK}	Blank Input Voltage	+6V
I_{RP}	Total Current Through R_P (Note 1)	290 mA
I_{REF}	Reference Output Current	–5 mA
T_C	Operating Case Temperature Range	
	1902-X	-25°C to +85°C
	1902-X-HR	–55°C to +125°C
T_J	Operating Junction Temperature Range	–55°C to +150°C
θ_{JC}	Junction-to-Case Thermal Resistance	10°C/W (for Q_{CAS} and Control IC)
		1.25°C/W (for R_p internal)
T_{STG}	Storage Temperature Range	–55°C to +150°C
T_S	Lead Temperature (Soldering, <10 sec)	+260°C

ELECTRICAL CHARACTERISTICS: T_C = +25°C, V_{EE} = −10.5V, V_{CC} = +15V, V_{HV} = Max, that is: 120V for 1902-0, 2 and 70V for 1902-4, V_{BLANK} = TTL Lo, V_{IG} = V_{OF} = ±V_{IN} = 0V, C_L = 10 pF(2), unless otherwise noted.

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
Input							
V_{IN}	Input Voltage Range		Referenced to Ground, Excluding V_{CM}	—	—	±0.714	V
I_B	Input Bias Current			–50	—	50	µA
V_{CM}	Input Common-Mode Range			–0.5	—	0.5	V
CMRR	Common-Mode Rejection Ratio		V_{CM} = ±0.5V	—	40	—	dB
R_{IN}	Signal Input Impedance			10	20	—	kΩ
C_{IN}	Signal Input Capacitance			—	2	—	pF
V_{OF}	Offset Adjust Input Voltage			0	—	5.5	V
I_{OF}	Offset Adjust Input Current		V_{OF} = 1V	0.5	—	10	µA
V_{IG}	Gain Adjust Input Voltage			0	—	5	V
I_{IG}	Gain Adjust Input Current		V_{IG} = 5V	0.5	—	10	µA
Digital Inputs							
I_{IL}	Input Logic "0" Current		V_{BLANK} = 0.4V	–600	—	–400	µA
I_{IH}	Input Logic "1" Current		V_{BLANK} = 2.4V	–400	—	–200	µA
Output							
V_O	Output Voltage	1902-0, -2	V_{HV} = Max (Note 3)	—	—	90	V_{P-P}
	Range, Peak-to-Peak	1902-4	V_{HV} = Max	—	—	50	V_{P-P}
R_P	Internal Pull-Up	1902-0	R_P is External, User-Selected	0	Note 3	0	Ω
	Resistor	1902-2		380	—	420	Ω
		1902-4		190	—	210	Ω
$V_{\Delta B}$	VΔ in BLANK Mode	(Note 4)	V_{BLANK} = 2.4V, V_{OF} = 1V, V_{IG} = 5V	**–R_P**	—	**2xR_P**	mV
	(VΔ = V_{HV} – V_O)	1902-0, -2	V_{BLANK} = 2.4V, V_{OF} = 1V, V_{IG} = 5V	**–0.4**	—	**0.8**	V
			V_{BLANK} = 2.4V, V_{OF} = 1V, V_{IG} = 5V	**–0.4**	—	**1**	V
		1902-4	V_{BLANK} = 2.4V, V_{OF} = 1V, V_{IG} = 5V	**–0.2**	—	**0.4**	V
			V_{BLANK} = 2.4V, V_{OF} = 1V, V_{IG} = 5V	**–0.4**	—	**1**	V
$V_{\Delta BIR}$	VΔ BLANK Mode	(Note 4)	V_{BLANK} = 2.4V, ΔV_{IN} = 0.3V, V_{IG} = 5V	—	—	±2xR_P	mV
	Input Rejection	1902-0, -2	V_{BLANK} = 2.4V, ΔV_{IN} = 0.3V, V_{IG} = 5V	—	—	±0.8	V
	(VΔ = V_{HV} – V_O)	1902-4	V_{BLANK} = 2.4V, ΔV_{IN} = 0.3V, V_{IG} = 5V	—	—	±0.4	V
VΔ/V_{OS}	VΔ vs Offset Adjust	1902-0, -2	V_{OF} = 0V, V_{IG} = 3V	**0.2**	—	**10**	V
	Min	1902-4	V_{OF} = 0V, V_{IG} = 3.5V	**0.1**	—	**6**	V
	Max	1902-0, -2	V_{OF} = 5V	**32**	—	**52**	V
		1902-4	V_{OF} = 5V	**16**	—	**26**	V
VΔ/V_{IG}	VΔ vs Gain Adjust	(Note 4)	ΔV_{IG} = 5V	—	—	**±10xR_P**	**mV**
	(Gain Adjust	1902-0, -2	ΔV_{IG} = 5V	—	—	**±4**	**V**
	Rejection)	1902-4	ΔV_{IG} = 5V	—	—	**±2**	**V**
VΔ T_C	VΔ Over	(Note 4)	T_C = +25°C to +75°C	—	—	±2xR_P	mV
	Temperature	1902-0, -2	T_C = +25°C to +75°C	—	—	±0.8	V
		1902-4	T_C = +25°C to +75°C	—	—	±0.4	V
V_{REF}	Reference Voltage		V_{CC} and V_{EE} = Nominal ±10%	**5.25**	—	**5.75**	**V**
I_{REF}	Reference Current			—	—	4	mA

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
Transfer							
A	Voltage Gain (Note 3)	1902-0, 2	V_{IG} = 3V, ΔV_{IN} = 0.6V	**71.5**	—	**133.8**	V/V
		1902-4	V_{IG} = 3.0V, ΔV_{IN} = 0.6V	**36**	—	**67**	V/V
LE_A	Linearity Error Amplifier		V_{IG} = 4V, V_{OF} = 1V, $V_{CM} \leq \pm 0.5V$	—	—	±2	%GS (Note 5)
LE_{GA}	Linearity Error Gain Adjust		V_{IN} = 0.2V, V_{OF} = 1V, $V_{CM} \leq \pm 0.5V$	—	—	±2	%
Dynamic							
t_R/t_F	Output Rise and Fall (10% to 90%)	1902-0 (25°C)	ΔV_{IN} = 0.6V, V_{OUT} from 20V to 110V	—	—	**5.0**	ns
		(-55,125°C)	ΔV_{IN} = 0.6V, V_{OUT} from 20V to 110V	—	—	**7.0**	ns
		1902-2 (25°C)	ΔV_{IN} = 0.6V, V_{OUT} from 20V to 110V	—	—	**4.0**	ns
		(-55,125°C)	ΔV_{IN} = 0.6V, V_{OUT} from 20V to 110V	—	—	**5.0**	ns
	C_L = 15 pF (Note 2)	1902-4 (25°C)	ΔV_{IN} = 0.6V, V_{OUT} from 15V to 65V	—	—	**2.5**	ns
		(-55,125°C)	ΔV_{IN} = 0.6V, V_{OUT} from 15V to 65V	—	—	**3.0**	ns
t_{BPW}	Blanking Input Pulse Width			—	—	30	ns
THD	Thermal Distortion			—	—	±2	%GS (Note 5)
Power Supplies							
V_{CC}	Positive IC Voltage		Acceptable Range	14.5	15	15.5	V
V_{EE}	Negative IC Voltage		Acceptable Range	−10	−10.5	−11	V
V_{HVMAX}	High-Voltage Supply	1902-0, -2		—	—	120	V
		1902-4		—	—	70	V
I_{CC}	Positive Supply Current			**80**	—	**100**	mA
I_{EE}	Negative Supply Current			**−70**	—	**−100**	mA
PSRR	Power Supply Rejection Ratio		V_{EE} and V_{CC} = Nominal ±5%	25	30	—	dB
PD	Power Dissipation			—	(Note 8)	—	W

Limits printed in **boldface** type are guaranteed and are 100% production tested. Limits in normal font are guaranteed but not 100% tested. Standard product tested at room temperature only. HR product tested at +125°C, 25°C, & -55°C.

NOTES:
1. This limit only applies when V_{HV} is greater than 90V.
2. Total load capacitance on the output mode of the IC includes load capacitance and parasitic.
3. All characterization measurements are made using a 400Ω resistor: internal (-2) or external (-0).
4. This specification applies to the 1902-0 when a custom pull-up resistor is selected by the user.
5. "%GS" means percent of grey scale, referring to RS343 standard video levels.
6. Rise and fall times depend on the value of R_P and L_P, peaking inductor (user-selected) and output load.
7. To meet the maximum speed, input rise times of less than 1 ns are needed. These limits are tested to guarantee device functionality.
8. See Table I, page 6, for power dissipation specifications.

HIGH-VOLTAGE VIDEO DRIVER FOR CRT MONITORS

ORDERING INFORMATION

Part Number	R_P (Ω)	High Voltage (V)	t_R At V_{PP} Max	Case Operating Temperature
1902-0	(Note 1)	120	(Note 2)	–25°C to +85°C
1902-0-HR	(Note 1)	120	(Note 2)	–55°C to +125°C
1902-2	400	120	90V/4.0 ns	–25°C to +85°C
1902-2-HR	400	120	90V/4.0 ns	–55°C to +125°C
1902-4	200	70	50V/2.5 ns	–25°C to +85°C
1902-4-HR	200	70	50V/2.5 ns	–55°C to +125°C

NOTES: 1. R_P is user-defined and supplied. The internal $R_P = 0\Omega$.
2. t_R is dependent upon user-defined R_P and V_{HV}.

EVALUATION BOARDS

Board Number	Driver Number	Description
6149-0	1902-0	These are demonstration boards which allow a user to quickly and easily evaluate the operating characteristics of the video display drivers in conjunction with the user's display. These cards contain the chosen driver, all necessary connectors (power supply, input/output, control signal) as well as gain and offset adjustment circuits. These boards are compact (4.5" x 4.5" max) and are supplied with an attached heat sink for thermal management. An application note is included with evaluation board to simplify the evaluation of driver performance.
6149-2	1902-2	
6149-4	1902-4	
6149-98		Heat sink kit used with the evaluation board.
6149-99		Fully assembled evaluation board with no hybrid inserted.

APPLICATIONS INFORMATION

Initial Setup

The initial setup of the 1902 requires proper setting of the V_{OF} and V_{IG} inputs to obtain balanced rise/fall times. If the quiescent current level (V_{OF}) is set too low, it slows the output rise time and limits the bandwidth of the 1902. If it is set too high, it will limit the fall time. Similar effects result if the gain control (V_{IG}) is set too high.

Signal Inputs

The analog inputs are $+V_{IN}$ and $-V_{IN}$. They are designed to accept RS343 signals, $\pm0.714\ V_{P\text{-}P}$. It is recommended that the input signal be limited to ±1.3V referenced to ground (0.714V signal +0.5V common mode). Offsets of ±2V (referenced to ground, signal included) can be tolerated without damage to the device, but are not recommended.

Output Voltage

The output voltage is controlled by the breakdown voltages of transistors Q_{CAS}, Q_N and Q_P (see standard configuration diagram), and the value of R_P. The maximum output voltage swing is determined by $V_{P\text{-}P} = 250\ mA \times R_P$. The dash-numbered versions of the 1902 differ in the values of R_P, L_P, and the breakdown voltages of the output transistors.

Rise and fall time specifications are based on very conservatively-peaked devices (<5% overshoot); i.e., L_P is low. The pull-up resistor (R_P) is connected directly to pins 16 and 17. External peaking can be added, use inductors with a high self-resonant frequency, and try to minimize capacitive coupling to ground. If no external resistors or inductors are added, use good, high-frequency bypassing on pins 16 and 17.

Care should be taken to limit the amount of the gain and offset adjustment so the total current through R_P does not cause excessive power dissipation. The gain adjust can set the AC current swing to greater than 250 mA (250 $mA_{P\text{-}P}$ = 100 $V_{P\text{-}P}$ on 400Ω). Higher currents and lower R_P values result in faster rise and fall times. For $V_{HV} > 90V$, do not exceed a total of 290 mA through R_P.

Access to the internal R_P also means the 1902 can be very easily configured for low power (but slower speed) applications by adding external resistance. Note that the device is characterized with a 400Ω resistor. Higher R_P values will degrade other specifications in addition to rise/fall times.

If large arc protection resistors are used (>50Ω), series inductance may improve the rise time of the output signal.

DC Gain (Contrast) Control

V_{IG} is the DC gain (contrast) control input. It can vary the device gain linearly from 0 to 80 by inputting a voltage from 0V to 5V. The internal reference (V_{REF}, pin 13) is designed to drive this input as well as the offset control input. Normally, a 5 kΩ potentiometer between V_{REF} and GND (see standard configuration diagram) is used to vary the gain; however, any external 0V to 5V DC source can be used, but some temperature performance degradation will result.

The gain equation for the 1902 is:

$$V_D = V_{HV} - V_O$$
$$= V_{IN} \times V_{IG} \times 0.1\ (\pm 20\%) \times R_P^*\ (\pm 5\%) \times 0.9$$

* R_P is inside the hybrid. Standard values are 200Ω ±5% and 400Ω ±5%. Other values can be added externally.

The overall gain of the 1902 may vary by ±20% due to process variations of internal components. Temperature variations also effect gain by as much as 150 ppm/°C. If more than one 1902 is used in a system, steps should be taken to make them track thermally (i.e., a common heat sink). This will reduce any mismatches due to varying ambient conditions.

Offset (Brightness) Control

V_{OF} is the output offset (brightness) control input. It sets the quiescent output current in R_P, thereby setting the output quiescent voltage level. Output quiescent voltage can be adjusted from (several µA x R_P) to (100 mA x R_P), nominal. From V_{HV} this is accomplished by inputting a DC voltage in the 0V to 5.5V range at V_{OF}. Normally, this input is from a 5 kΩ potentiometer between V_{REF} and GND (see standard configuration diagram).

Blank

The blank input, when asserted (i.e., TTL HIGH), disables the video input of the 1902 and sets the output to approximately V_{HV}. This input is independent of the input signal and operates with TTL levels.

Reference Voltage

V_{REF} is a zener reference with a nominal output voltage of 5.5V ±5%, and can source up to 4 mA. It is used to adjust offset and gain.

Power Supplies

Power supplies of 15V (±5%) and –10.5V (±5%) are required for proper operation. The negative supply can be set to –12V, but will increase the internal power dissipation and case temperature. V_{HV} is a function of the 1902 version selected. The maximum value is 120V, allowing up to 90 V_{P-P} output signals. Assume that the absolute maximum value is V_{HV} (listed in the specification table) plus 5V; i.e., the 1902-2 absolute maximum equals 125V. It is recommended the 1902 not be operated above V_{HV}. Because the output from this type of circuit is referenced to the V_{HV} rail, it is important that V_{HV} is very stable. In other words, there is no PSRR for V_{HV}. Your system supply will determine your DC stability.

To achieve maximum high-frequency performance, good high-frequency grounding practices and PC board layout are mandatory.

Supply Sequencing

It is essential that the V_{HV} supply be brought up before V_{EE} and V_{CC} when using the higher voltage versions of the 1902. Supply sequencing is of less importance when V_{HV} is less than 90V. The recommended sequence is V_{HV}, V_{CC}, then V_{EE}. If sequencing cannot be done, the supplies should be brought up within a few milliseconds of each other.

Power Dissipation

The 1902 power dissipation will vary in accordance to load requirements and pixel size. The 1902 flat pack is designed to provide a low thermal resistance path from the hybrid circuit to an external heat sink. Mounting flanges provide solid mechanical and thermal attachment of the package to the heat sink. In addition, the package is electrically isolated so no mounting insulators are needed and the heat sink can be at any convenient potential.

Table I. Typical Power Dissipations

					% of Time Signal is at			Average Power	Average Power
Device	V_{HV} (V)	Black Level (V)	White Level (V)	Max Signal (V_O-V_{BLACK}) (V)	Blank Level (%)	Black Level (%)	White Level (%)	Output Stage (Notes 1, 2) (W)	Total (Notes 1, 2) (W)
1902-2	120	110	20	0	100	0	0	0	2.5
1902-2	120	110	20	90	20	40	40	13.2	15.7
1902-4	70	65	15	0	100	0	0	0	2.5
1902-4	70	65	15	50	20	40	40	8.4	10.59

NOTES:
1. Input stage quiescent power is approximately 2.5W.
2. Power dissipations listed do not include power dissipation due to switching.

TELEDYNE COMPONENTS

HIGH NEGATIVE-VOLTAGE VIDEO DRIVER FOR CRT MONITORS

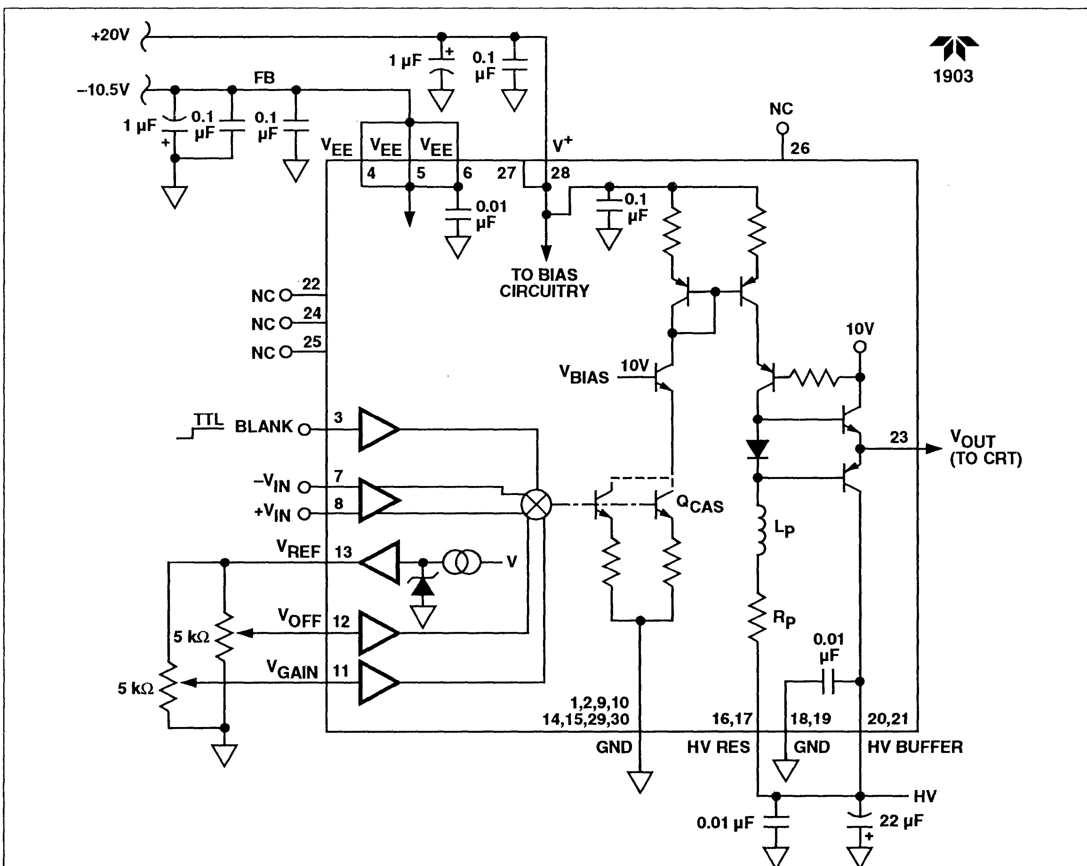
FEATURES

- Output Signals Into 10 pF Loads .... 80 V_{P-P}
- Rise and Fall Times @ 80 V_{P-P} .... <4 ns
- User-Defined Pull-Down Resistor
- Linear Gain Adjustment for Matching
- Versions Available to Match Specific CRT Requirements

APPLICATIONS

- CRT Monitors
  - — Projection
  - — High-Resolution
  - — Beam Index

STANDARD CONFIGURATION



1055-1

1903

GENERAL DESCRIPTION

The 1903 is a high-performance, high-voltage amplifier designed to drive the grid in high-resolution, high-brightness CRT monitors and projection displays.

The 1903 is replete with differential inputs, blanking control, linearly-adjustable gain stage, adjustable offset and a differential emitter-follower output stage. It is capable of driving 10 pF to 20 pF loads, can be driven directly from a standard video DAC, and is RS170 and RS343 compatible.

The 1903 has four variants to suit different applications. There are basically two types: Those with internal pull-down resistors and those that allow the user to choose and apply their own pull-down resistor. The parts within these two types differ in peak-to-peak output signal swing. The 1903-0 and 1903-2 are 90 V_{P-P} versions specified at less than 4 ns rise and fall times. The 1903-0 and 1903-2 operate from a –95V rail.

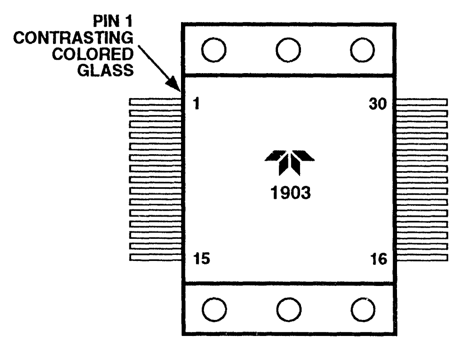
The 1903's are housed in hermetically-sealed, 30-pin flat packs with mounting flanges suitable for 4-40 screws. The standard 1903-X is specified for –25°C to +85°C operation. The 1903-X-HR is specified for –55°C to +125°C operation.

PIN CONFIGURATION

PIN NO.	DESIGNATION	PIN NO.	DESIGNATION
1	GND	30	GND
2	GND	29	GND
3	BLANK	28	V_{CC}
4	V_{EE}	27	V_{CC}
5	V_{EE}	26	NC
6	V_{EE}	25	NC
7	$-V_{IN}$	24	NC
8	$+V_{IN}$	23	V_{OUT}
9	GND	22	NC
10	GND	21	HV BUFFER
11	V_{GAIN}	20	HV BUFFER
12	V_{OFF}	19	GND
13	V_{REF}	18	GND
14	GND	17	HV RESISTOR
15	GND	16	HV RESISTOR

HV = HIGH VOLTAGE
NC = NO INTERNAL CONNECTION

30-Pin Flat Package



HIGH NEGATIVE-VOLTAGE VIDEO DRIVER FOR CRT MONITORS

ORDERING INFORMATION

Part Number	R_P	V_{HV}	Output Range	Rise Time	Fall Time	Case Operating Temperature
1903-0	0Ω*	–95V	-5V to -85V	**	**	–25°C to +85°C
1903-0-HR	0Ω*	–95V	-5V to -85V	**	**	–55°C to +125°C
1903-2	400Ω	–95V	-5V to -85V	3 ns	4.5 ns	–25°C to +85°C
1903-2-HR	400Ω	–95V	-5V to -85V	3 ns	4.5 ns	–55°C to +125°C

*User must provide an external R_P.

**Rise and fall times for devices with external R_P will approach the times specified here for corresponding values of external R_P versus internal R_P and output voltage swing.

EVALUATION BOARDS

Board Number	Driver Number	Description
6150-0	1903	These are demonstration boards which allow a user to quickly and easily evaluate the operating characteristics of the video display drivers in conjunction with the user's display. These cards contain the chosen driver, all necessary connectors (power supply, input/output, control signal) as well as gain and offset adjustment circuits. These boards are compact (4.5" x 4.5" max) and are supplied with an attached heat sink for thermal management. An application note is included with evaluation board to simplify the evaluation of driver performance.
6150-2	1903-2	
6150-98		Heat sink used with the evaluation board.
6150-99		Fully assembled evaluation board with no hybrid inserted.

ABSOLUTE MAXIMUM RATINGS

V_{HV} Load Resistor Supply .... (V_{HV} Max +5V)
V_{CC} Positive IC Supply .... +22V
V_{EE} Negative IC Supply .... –12V
V_{IDF} Differential Input Voltage .... +2V
V_{ICM} Common-Mode Input Voltage .... ±2V
V_{IG} Gain Adjustment Input Voltage .... +6V
V_{OF} Offset Adjustment Input Voltage .... +6V
V_{BLANK} Blank Input Voltage .... +6V
I_{RP} Total Current Through R_P (Note 1) .... 290 mA
I_{REF} Reference Output Current .... –5 mA

T_C Operating Case Temperature Range
1903 .... –25°C to +85°C
1903-X-HR .... –55°C to +125°C
T_J Operating Junction Temperature Range
.... –55°C to +150°C
θ_{JC} Junction-to-Case Thermal Resistance
.... 10°C/W (For Q_{CAS} and control IC)
.... 1.25°C/W (For R_p internal)
T_{STG} Storage Temperature Range ..... –55°C to +150°C
T_S Lead Temperature (Soldering, <10 sec) ... +260°C

ELECTRICAL CHARACTERISTICS: T_C = +25°C, V_{EE} = –10.5V, V_{CC} = 20V, V_{HV} = Max, that is, -95V, V_{BLANK} = TTL Low, $V_{IG} = V_{OF} = \pm V_{IN}$ = 0V, C_L = 10 pF[(2)], and external R_P = 400Ω (1903-0), unless otherwise noted.

Symbol	Parameter	Test Conditions	Sbgrp*	Min	Typ	Max	Unit
Input							
V_{IN}	Input Voltage Range	Referenced to Ground, Excluding V_{CM}	—	—	—	±0.714	V
I_B	Input Bias Current		—	–50	—	50	µA
V_{CM}	Input Common-Mode Range		—	–0.5	—	0.5	V

1903

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
Input (cont.)							
CMRR	Common-Mode Rejection Ratio		$V_{CM} = \pm 0.5V$	—	40	—	dB
R_{IN}	Signal Input Impedance			10	20	—	kΩ
C_{IN}	Signal Input Capacitance			—	2	—	pF
V_{OF}	Offset Adjust Input Voltage			0	—	5.5	V
I_{OF}	Offset Adjust Input Current		$V_{OF} = 1V$	0.5	—	10	μA
V_{IG}	Gain Adjust Input Voltage			0	—	5	V
I_{IG}	Gain Adjust Input Current		$V_{IG} = 5V$	0.5	—	10	μA
Digital Inputs							
I_{IL}	Input Logic "0" Current		$V_{BLANK} = 0.4V$	–600	—	–400	μA
I_{IH}	Input Logic "1" Current		$V_{BLANK} = 2.4V$	–400	—	–200	μA
Output							
V_O	Output Voltage Range	1903-0, -2	V_{HV} = Max	—	—	80	V_{P-P}
R_P	Internal Pull-Down Resistor	1903-0 1903-2	R_P is External and is User-Supplied	— 380	0 —	— 420	Ω Ω
$V_{\Delta B}$	V_Δ in BLANK Mode (Note 4) ($V_\Delta = V_{HV} - V_O$)	1903-0 1903-2	$V_{BLANK} = 2.4V$, $V_{OF} = 1V$, $V_{IG} = 5V$ $V_{BLANK} = 2.4V$, $V_{OF} = 1V$, $V_{IG} = 5V$	**$-2xR_P$** **$-2.5xR_P$** **–1**	— — —	**R_P** **0.4** **0.4**	mV V V
$V_{\Delta BIR}$	BLANK Mode Input Rejection (Note 4)	 1903-0, -3	$V_{BLANK} = 2.4V$, $\Delta V_{IN} = 0.3V$, $V_{IG} = 5V$ $V_{BLANK} = 2.4V$, $\Delta V_{IN} = 0.3V$, $V_{IG} = 5V$	**$-2xR_P$** **–0.8**	— —	**$2xR_P$** **0.8**	mV V
V_Δ/V_{OS}	V_Δ Offset Voltage (Note that 1903-0 uses 400Ω load resistor)						
	Min	1903-2	$V_{IG} = 4V$	**–0.2**	—	**–10**	V
	Max	1903-2	$V_{OF} = 5V$	**–52**	—	**–32**	V
V_O/V_{IG}	V_Δ vs Gain Adjust	1903-0 1903-2	$\Delta V_{IG} = 5V$ $\Delta V_{IG} = 5V$	— —	— —	**$\pm 10xR_P$** **±4**	mV V
$V_\Delta T_C$	V_Δ Over Temperature	1903-0 1903-2	T_C = +25°C to +75°C T_C = +25°C to +75°C	— —	— —	$\pm 2xR_P$ ±0.84	mV V
V_{REF}	Reference Voltage		V_{CC} and V_{EE} = Nominal ±10%	**5.25**	—	**5.75**	V
I_{REF}	Reference Current			—	—	4	mA
Transfer							
A	Voltage Gain (Note 4)	1903-0, -2	$V_{IG} = 3V$, $\Delta V_{IN} = 0.6V$	**71.5**	—	**133.8**	V/V
LE_A	Linearity Error Amplifier		$V_{IG} = 4V$, $V_{OF} = 1V$, $V_{CM} \leq \pm 0.5V$	—	—	±2	%GS (Note 3)
LE_{GA}	Linearity Error Gain Adjust		$V_{IN} = 0.2V$, $V_{OF} = 1V$, $V_{CM} \leq \pm 0.5V$	—	—	±2	%GS (Note 3)
Dynamic							
t_R	Output Rise Time From $\pm V_{IN}$ (Note 5)	1903-0, -2 25°C, -55°C	$\Delta V_{IN} = 0.6V$, t_R (V_{IN}) = 1 ns, C_L = 15 pF V_O = –5V to –85V (Note 2)	—	3	**4**	ns
t_F	Output Fall Time From $\pm V_{IN}$ (Note 5)	1903-0, -2 25°C, -55°C	$\Delta V_{IN} = 0.6V$, t_R (V_{IN}) = 1 ns, C_L = 15 pF V_O = –5V to –85V (Note 2)	—	4	**6**	ns
t_R, t_F	Output Rise and Fall Time From $\pm V_{IN}$ (Note 5)	1903-0, -2	HR only, 125°C	—	6	**9**	ns
t_{BPW}	Blanking Input Pulse Width			30	—	—	ns
THD	Thermal Distortion			—	—	±2	% GS (Note 3)

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supplies						
V_{CC}	Positive IC Voltage		19.5	20	20.5	V
V_{EE}	Negative IC Voltage		–10	–10.5	–11	V
V_{HV}	High Voltage Supply	1903-0, -2	0	—	–105	V
		1903-1, -3	0	—	–85	V
I_{CC}	Positive Supply Current		—	—	**100**	mA
I_{EE}	Negative Supply Current		—	—	**–90**	mA
PSRR	Power Supply Rejection Ratio	V_{EE} and V_{CC} = Nominal ±5%	25	—	—	dB
PD	Power Dissipation		—	(Note 6)	—	W

Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested. Standard part tested at room temperature. HR parts tested at +125°C, -55°C & +25°C.

NOTES:
1. This limit only applies when V_{HV} is greater than –60V.
2. Total load capacitance on the output mode of the IC includes load capacitance and parasitic.
3. "%GS" means percent of grey scale, referring to RS343 standard video levels.
4. All characterization measurements are made using a 400Ω resistor.
5. Rise and fall times for devices with external R_P will approach the times specified here for corresponding values of external R_P versus internal R_P and output voltage swing, depending on PC board layout parasitics.
6. Refer to Table I, page 6, for power dissipation specifications.

APPLICATIONS INFORMATION

Initial Setup

The initial setup of the 1903 requires proper setting of the V_{OF} and V_{IG} inputs to obtain balanced rise and fall times. If the black level (V_{OF}) is set too low, it will slow the output fall time and limit the bandwidth of the 1903. If it is set too high, it will limit the rise time. Similar effects will result if the gain control (V_{IG}) is set too high.

Signal Inputs

The analog inputs are $+V_{IN}$ and $-V_{IN}$. They are designed to accept RS343 signals, ±0.714 V_{P-P}. It is recommended that the input signal be limited to ±1.3V, referenced to ground (0.714V signal + 0.5V common mode). Offsets of ±2V (referenced to ground, signal included) can be tolerated without damage to the device, but are not recommended.

Output Voltage

The output voltage is controlled by the breakdown voltages of transistors Q_{CAS}, Q_N, and Q_P (see standard configuration diagram), and the value of R_P. The maximum output voltage swing is determined by V_{PP} = 250 mA x R_P.

The rise and fall time specifications are based on conservatively-peaked devices (<5% at the max V_{P-P}). The internal pull-down resistor (R_P) is connected directly to pins 16 and 17. External peaking can be added; use inductors with a high self-resonant frequency and try to minimize capacitive coupling to ground. If no external resistors or inductors are added, use good, high-frequency bypassing on pins 16 and 17.

If large arc-protection resistors are used; i.e., >50Ω, use of a series inductor may improve the rise time of the output signal.

DC Gain (Contrast) Control

V_{IG} is the DC gain (contrast) control input. It can vary the device gain linearly from 0 to 100 by inputting a voltage from 0V to 5V. The internal reference (V_{REF}, pin 13) is designed to drive this input as well as the offset control input. Normally, a 5 kΩ potentiometer between V_{REF} and GND (see standard configuration diagram) is used to vary the gain. However, any external 0V to 5V DC source can be used, but some temperature performance degradation will result.

The gain equation for the 1903 is:

$$[V_{HV} - V_O] = (V_{IN} \times V_{IG} \times 0.1\ (\pm 20\%) \times R_P\ (\pm 5\%) \times 0.9$$

*R_P can be the internal 400Ω resistor or an external user-defined/ supplied resistor.

The overall gain of the 1903 may vary by ±20% due to process variations of the internal components. Temperature variations also affect gain by as much as 150 ppm/°C. If more than one 1903 is used in a system, steps should be taken to have them track thermally; i.e., a common heat sink. This will reduce any mismatches due to varying ambient conditions.

Offset (Brightness) Control

V_{OF} is the output offset (brightness) control input. It sets the quiescent output current, in R_P, thereby setting the output quiescent voltage level. Output quiescent voltage can be adjusted from several µA x R_P to 100 mA x R_P, nominal, from the V_{HV} rail. This is accomplished by inputting a DC voltage in the 0V to 5.5V range at V_{OF}. Normally, this input is from a 5 kW potentiometer bertween V_{REF} and GND (see standard configuration diagram).

Blank

The blank input, when asserted (i.e., TTL HIGH), disables the video input of the 1903 and sets the output to approximately V_{HV}. This input is independent of the input signal and operates with TTL levels.

Reference Voltage

V_{REF} is a zener reference with a nominal output voltage of 5.5V ±5%, and can source up to 4 mA. It is used in adjusting offset and gain.

Power Supply

Power supplies of 20V (±5%) and –10.5V (±5%) are required for proper operation. The negative supply can be set to –12V, but will increase the internal power dissipation and case temperature. V_{HV} is a function of the 1903 version selected. The maximum voltage is –95V, allowing up to 80 $V_{P\text{-}P}$ output signals. The absolute maximum voltage, to preclude damage, is equal to the V_{HV} listed in the specification table, plus 5V. For example, the 1903-0 absolute maximum is –100V. It is recommended that the high voltage supply not exceed the listed V_{HV}.

Due to the fact the output from this type of circuit is referenced to the V_{HV} rail, there is no PSRR for V_{HV}. Therefore, it is important that the V_{HV} rail is very stable. Your system power supply will determine your DC stability.

To achieve maximum high-frequency performance, good high-frequency grounding practices and PC board layout are mandatory. For best performance, the case must be held at AC ground. That is, if the case cannot be grounded directly (such as through a grounded heat sink), it should be capacitively grounded.

Supply Sequencing

It is essential that the V_{HV} supply be brought up before V_{EE} and V_{CC} when using the higher voltage version of the 1903. Supply sequencing is less important when V_{HV} is less than –70V. The recommended sequence is V_{HV}, V_{CC} then V_{EE}. If sequencing is not possible, the supplies should be brought up within a few milliseconds of each other.

Power Dissipation

The 1903 power dissipation will vary in accordance to load requirements and pixel size. The 1903 flat pack is designed to provide a low thermal resistance path from the hybrid circuit to an external heat sink. Mounting flanges provide solid mechanical and thermal attachment of the package to the heat sink. In addition, the package is electrically isolated so no mounting insulators are needed and the heat sink can be at any convenient voltage potential. (See Table I.)

Table I. Typical Power Dissipations

Device	V_{HV} (V)	Black Level (V)	White Level (V)	Max. Signal (V_O-V_{BLACK}) (V)	% of Time Signal is at: Blank Level (%)	Black Level (%)	White Level (%)	Average Power Output Stage (Notes 1, 2) (W)	Average Power Total (Notes 1, 2) (W)
1903-2	–95	–85	–5	0	100	0	0	0	2.5
1903-2	–95	–85	–5	80	20	40	40	13.5	16

NOTES: 1. Input stage quiescent power is approximately 2.5W.
2. Power dissipations listed do not include power dissipation due to switching.

Section 11

Display Drivers

4-DIGIT CMOS DISPLAY DECODER/DRIVER

FEATURES

TC7211A (LCD DRIVER)

- **4-Digit Nonmultiplexed, 7-Segment LCD Outputs With Backplane Driver**
- **RC Oscillator On Chip Generates Backplane Drive Signal**
- **Eliminates DC Bias Which Degrades LCD Life**
- **Backplane Input/Output Pin Permits Synchronization of Cascaded Slave Device to a Master Backplane Signal**
- **Separate Digit Select Inputs to Accept Multiplexed BCD/Binary Inputs**
- **Binary and BCD Inputs Decoded to Code B (0 to 9, —, E, H, L, P, Blank)**
- **Pin Compatible and Functionally Equivalent to ICM7211A and DF411**
- **Connect to TC7135 in Flat Package for Compact 4-1/2 Digit Meter Systems**

TC7212A (LED DRIVER)

- **28 Current Limited Outputs Drive Common-Anode LEDs at Greater than 5 mA Per Segment**
- **Brightness Input Allows Potentiometer Control of LED Segment Current Pin Also Serves as Digital Display Enable**
- **Same Input Configuration and Output Decoding as the TC7211A**
- **Pin compatible and Functionally Equivalent to iCM7212A**

GENERAL DESCRIPTION

The TC7211A (LCD Decoder/Driver) and TC7212A (LED Decoder/Driver) is a direct drive, 4-digit, 7-segment display decoder and driver.

The TC7211A drives conventional LCDs. An RC oscillator, divider chain, backplane driver, and 28-segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane, but in-phase for an OFF segment and out-of-phase for an ON segment. The net DC voltage applied between driver segment and backplane is zero.

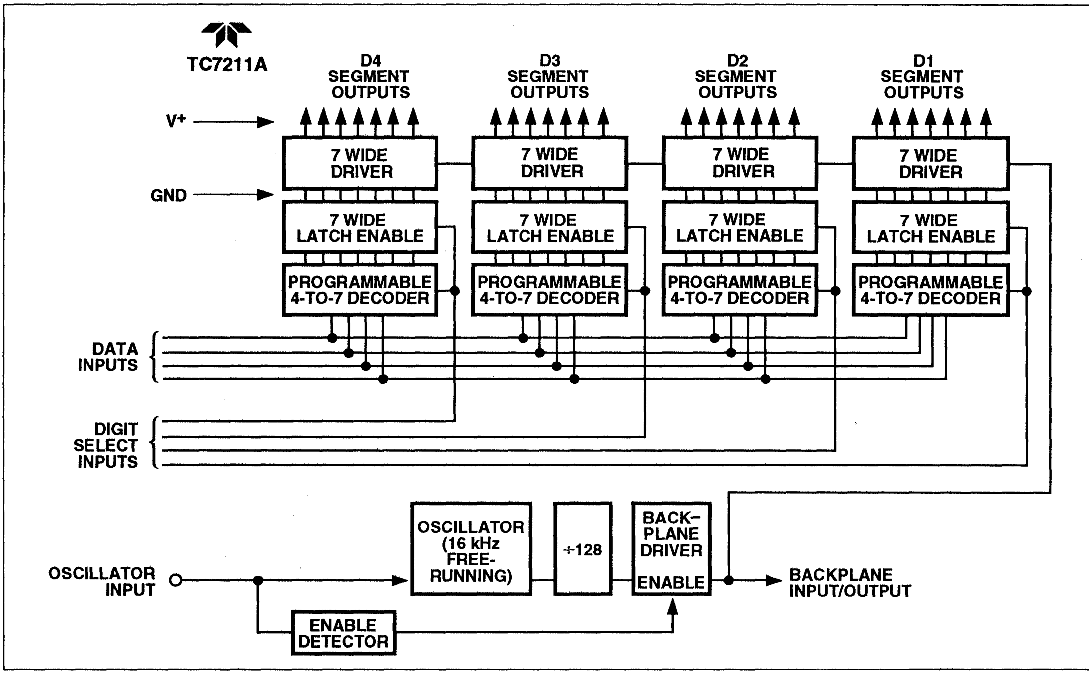
The TC7212A Drives common -anode LED displays with 28 current controlled, low leakage, open, N-Channel output transistors. The brightness control input can be used as a digital display enable. A varying voltage at the control input will allow continuous display brightness control.

The TC7211A (LCD) and TC7212A (LED) requires only 4 data bit inputs and 4 digit select signals to interface with multiplexed BCD or binary output devices (such as the ICM7217, ICM7226, ICL7103 and TC7135). The 4-bit binary input code is decoded into the 7-segment alphanumeric code known as “Code B.”

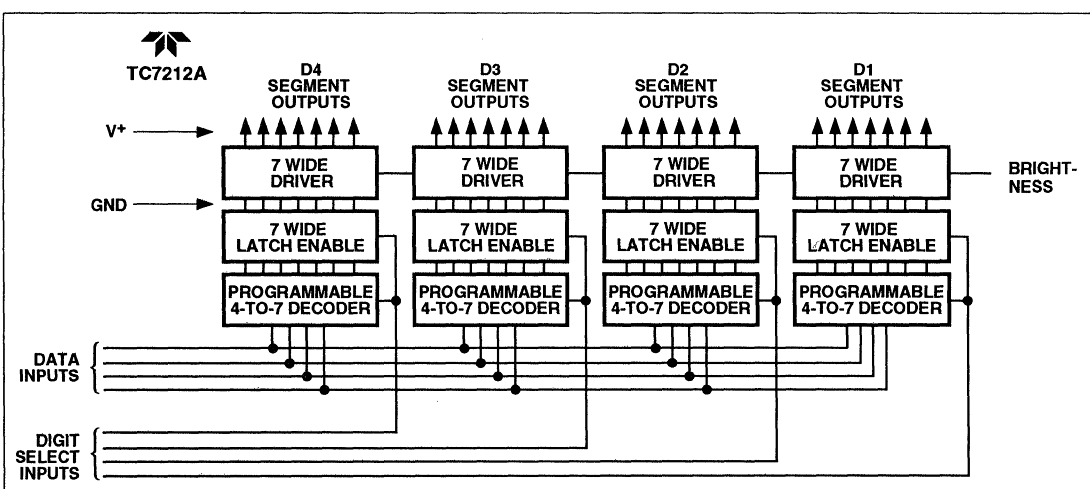
The "Code B" output format results in a 0 to 9, —, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the 7-segment display format.

The CMOS TC7211A and TC7212A are available in a 40-pin epoxy dual-in-line package and a compact 60-pin flat package. All inputs are protected against static discharge.

FUNCTIONAL BLOCK DIAGRAM



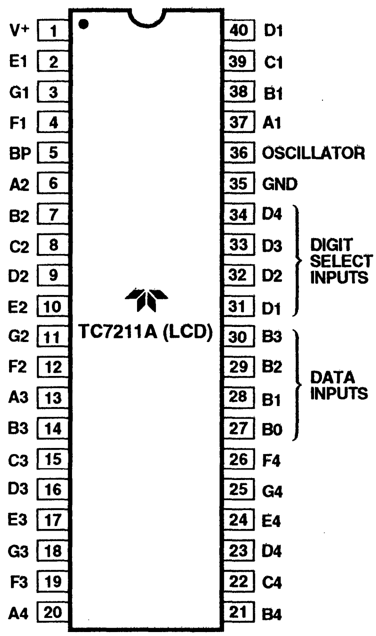
FUNCTIONAL BLOCK DIAGRAM

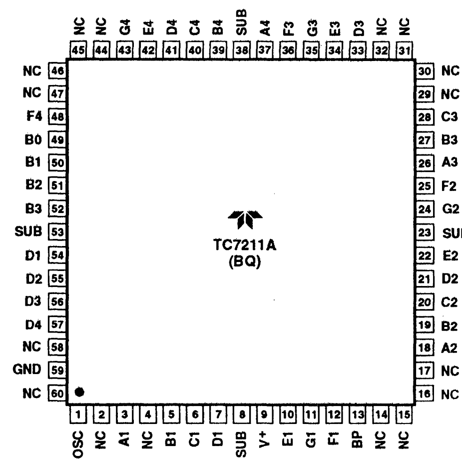


4-DIGIT CMOS DISPLAY DECODER/DRIVER

TC7211A
TC7212A

PIN CONFIGURATIONS





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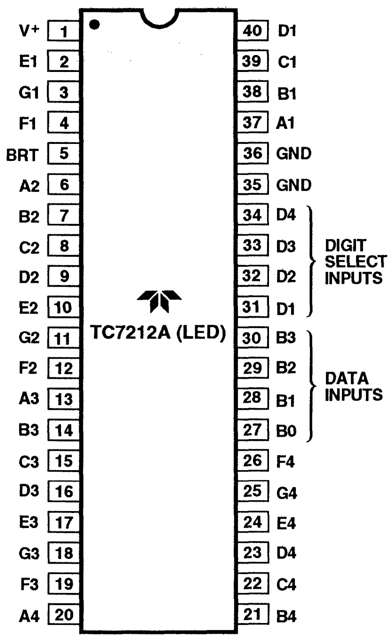
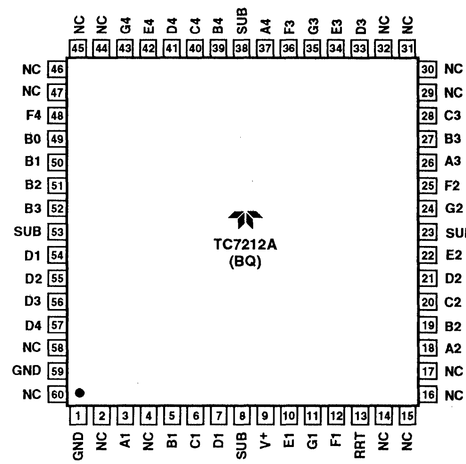
TC7211A
TC7212A

PIN CONFIGURATIONS



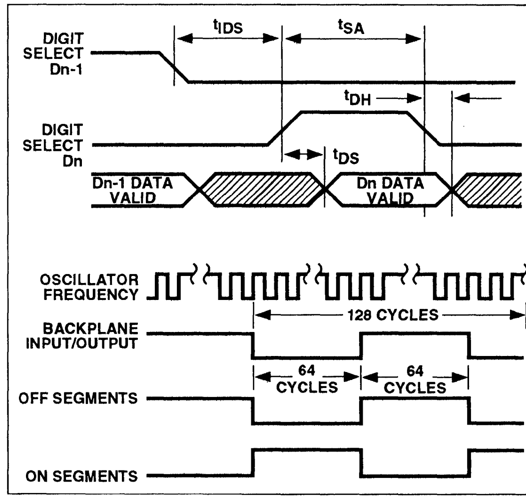


NOTES: 1. NC = No internal connection.
2. Pins 8, 23, 38 and 53 are connected to the die substrate. The potential at these pins is approximately V^+. No external connections should be made.

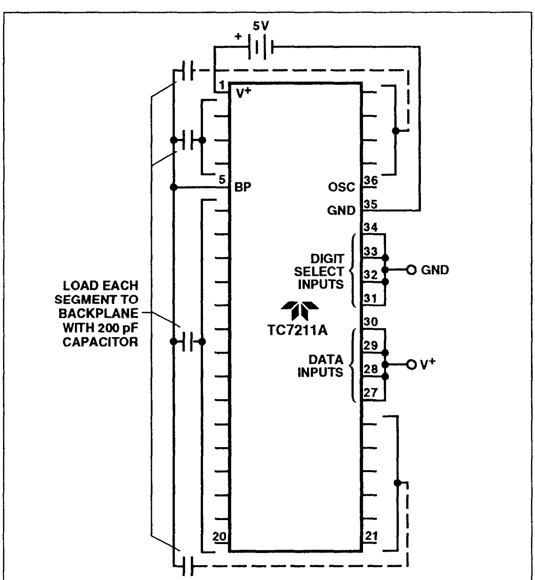
ORDERING INFORMATION

Part No.	Driver Type	Package	Output Code	Input Config.
TC7211AIPL	LCD	40-Pin Plastic DIP	Code B	Multiplexed 4-bit Binary or BCD
TC7212AIPL	LED	40-Pin Plastic DIP	Code B	Multiplexed 4-bit Binary or BCD
TC7211AIJL	LCD	40-Pin CerDIP	Code B	Multiplexed 4-bit Binary or BCD
TC7212AIJL	LED	40-Pin CerDIP	Code B	Multiplexed 4-bit Binary or BCD
TC7211AIBQ	LCD	60-Pin Flat Package Form Leads	Code B	Multiplexed 4-bit Binary or BCD
TC7212AIBQ	LED	60-Pin Flat Package Form Leads	Code B	Multiplexed 4-bit Binary or BCD

TIMING DIAGRAMS



TEST CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +6.5V
Input Voltage, Any Terminal
(Note 2) .... V+ +0.3V, GND –0.3V
Power Dissipation (Note 1) .... 0.8 W at +70°C
Operating Temperature Range .... –20°C to +85°C
Storage Temperature Range .... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES: 1. This limit refers to that of the package and will not be realized during normal operation.
2. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V+ or less that GND may cause destructive latch-up. For this reason it is recommended that inputs from external sources not operating on the same power supply not be applied to the device before its supply is established, and, in multiple supply systems, the supply to the TC7211A/TC7212A be turned on first.

TABLE I: OPERATING CHARACTERISTICS

Test Conditions: All parameters measured with V+ = 5V

TC7211A Characteristics (LCD Decoder/Driver)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SUP}	Operating Voltage Range		3	5	6	V
I_{OP}	Operating Current	Display Blank	—	10	50	µA
I_{OSCI}	Oscillator Input Current	Pin 36	—	±2	±10	µA
t_{RFS}	Segment Rise/Fall Time	C_L = 200 pF	—	0.5	—	µA
t_{RFB}	Backplane Rise/Fall Time	C_L = 5000 pF	—	1.5	—	µs
f_{OSC}	Oscillator Frequency	Pin 36 Floating	—	16	—	kHz
f_{BP}	Backplane Frequency	Pin 36 Floating	—	125	—	Hz

TC7212A Characteristics (Common-Anode LED Decoder/Driver)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SUP}	Operating Voltage Range		4	5	6	V
I_{OP}	Operating Current	Pin 5 (Brightness),	—	10	50	µA
	Display Off	Pins 27-34 = GROUND				
I_{OP}	Operating Current	Pin 5 at V+, Display all 8's	—	200	—	mA
I_{SLK}	Segment Leakage Current	Segment Off	—	±0.01	±1	µA
I_{SEG}	Segment On Current	Segment On, V_O = +3V	5	8	—	mA
V_{IH}	Logic "1" High Input Voltage		3	—	—	V
V_{IL}	Logic "0" Low Input Voltage		—	—	1	V
I_{ILK}	Input Leakage Current	Pins 27–34	—	±0.01	±1	µA
C_{IN}	Input Capacitance	Pins 27–34	—	5	—	pF
I_{BPLK}	BP/Brightness Input Current Leakage	Measured at Pin 5 With Pin 36 at GND	—	±0.01	±1	µA
C_{BPI}	BP/Brightness Input Capacitance	All Devices	—	200	—	pF

AC Characteristics (LCD and LED Decoder/Driver)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{SA}	Chip Select Active Pulse Width	Refer to Timing Diagrams	1	—	—	µs
t_{DS}	Data Valid Time	Refer to Timing Diagrams	—	—	—	ns
t_{DH}	Data Hold Time	Refer to Timing Diagrams	200	—	—	ns
t_{IDS}	Inter-Digit Select Time	Refer to Timing Diagrams	2	—	—	µs

4-DIGIT CMOS DISPLAY DECODER/DRIVER

TC7211A
TC7212A

INPUT DEFINITIONS

In this table, V^+ and GND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

Input	Pin No.	Condition	Function	
B0	27 (49)	V^+ = Logic "1" GND = Logic "0"	Ones (Least Significant)	Data Input Bits
B1	28 (50)	V^+ = Logic "1" GND = Logic "0"	Twos	Data Input Bits
B2	29 (51)	V^+ = Logic "1" GND = Logic "0"	Fours	Data Input Bits
B3	30 (52)	V^+ = Logic "1" GND = Logic "0"	Eights (Most Significant)	Data Input Bits
OSC	36 (1)	Floating or with external capacitor GND	Oscillator input. Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (pin 5)	
D1	31 (54)		D1 Digit Select (Least Significant)	
D2	32 (55)	V^+ = Active	D2 Digit Select	
D3	33 (56)	GND = Inactive	D3 Digit Select	
D4	34 (57)		D4 Digit Select (Most Significant)	

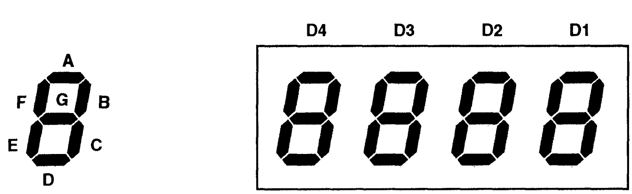
OUTPUT DEFINITIONS

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

Output	Pin No.		Function	Output	Pin No.		Function
A1	37 (3)	A	Segment Drive Digit 1 (LSD)	A3	13 (26)	A	Segment Drive Digit 3
B1	38 (5)	B		B3	14 (27)	B	
C1	39 (6)	C		C3	15 (28)	C	
D1	40 (7)	D		D3	16 (33)	D	
E1	2 (10)	E		E3	17 (34)	E	
F1	4 (12)	F		F3	19 (36)	F	
G1	3 (11)	G		G3	18 (35)	G	
A2	6 (18)	A	Segment Drive Digit 2	A4	20 (37)	A	Segment Drive Digit 4 (MSD)
B2	7 (19)	B		B4	21 (39)	B	
C2	8 (20)	C		C4	22 (40)	C	
D2	9 (21)	D		D4	23 (41)	D	
E2	10 (22)	E		E4	24 (42)	E	
F2	12 (25)	F		F4	26 (48)	F	
G2	11 (24)	G		G4	25 (43)	G	

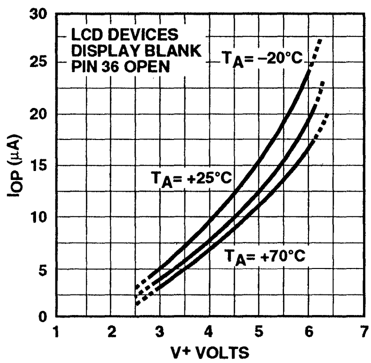
*Pin number in parentheses ( ) are for 60-pin flat pack.

DIGIT ASSIGNMENT

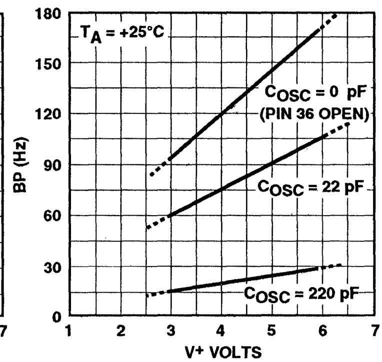


TYPICAL OPERATING CHARACTERISTICS CURVES

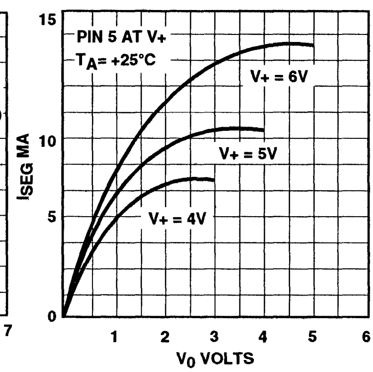
Operating Supply Current vs Supply Voltage



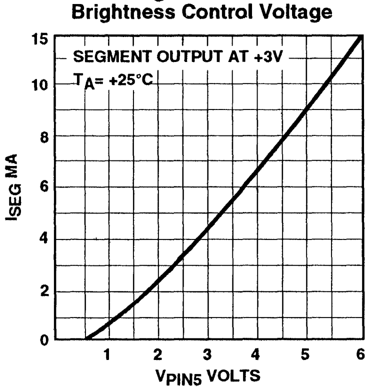
Backplane Frequency vs Supply Voltage



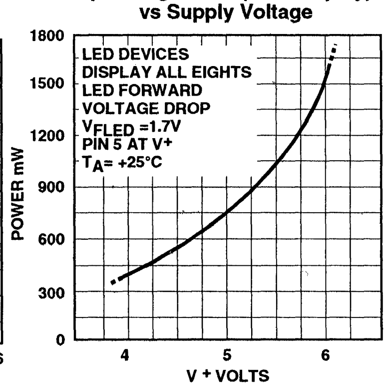
LED Segment Current vs Output Voltage



LED Segment Current vs Brightness Control Voltage



Operating Power (LED Display) vs Supply Voltage



BASIC OPERATION

The TC7211A drives 4-digit by 7-segment LCDs. The device contains 28 individual segment drivers, a backplane driver, an on-chip oscillator, and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N- and P-channel transistors for identical "ON" resistance. The equal resistances eliminate the DC output driver component resulting from unequal rise and fall times. This ensures maximum LCD life.

The backplane output driver can be disabled by grounding the OSCILLATOR input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane (BP) terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCDs with characters in multiples of four. (See Figure 1.)

Each slave's backplane input represents only a 200 pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices drivable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half-inch characters with rise and fall times under 5 µs. This represents a system with three slave devices and a fourth master device driving the backplane.

If more than four devices are slaved together, the backplane signal should be derived externally and all TC7211A devices slaved to it. The external drive signal must drive a high capacitive load with 1µs to 2 µs rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures, the frequency may be reduced to compensate for display response time.

The on-chip RC oscillator free-runs at approximately 16 kHz. A ÷128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal and V^+. (See typical operating characteristics curves.)

The free-running oscillator may be overridden (if desired) by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or low portion, as this will result in a DC drive component being applied to the LCD, limiting the LCD's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range. The oscillator input signal duty cycle is skewed so the low portion duration is less than 1 µs. The backplane disable sensing circuit will not respond to such a short signal.

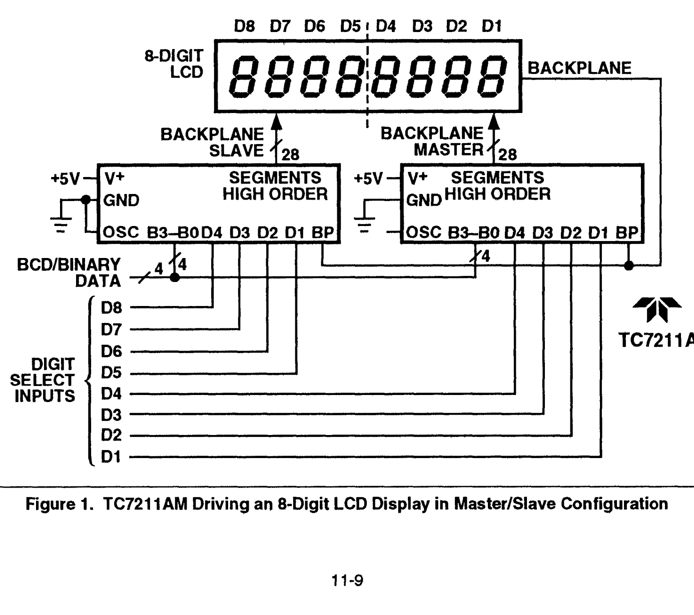


Figure 1. TC7211AM Driving an 8-Digit LCD Display in Master/Slave Configuration

TC7212A LED Decoder

The brightness input may also be operated digitally as a display enable. At a logic 1 the display is fully "ON" and at a logic signal of varying duty cycle also. When operating with LEDs at a higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperature rise. The maximum TC7212AM LED Decoder/Driver

The TC7212AM directly drives four digit, seven segment, common-anode LED displays. The 28 segment drivers are low leakage, current controlled, open drain N-channel MOS transistors.

A brightness input (pin 5) can be used in two ways to control output transistor drain current. The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment drivers "ON" resistance. A variable brightness control may be implemented with a single potentiometer (Figure 4). A high value potentiomenter (100 kΩ to 1MΩ) will minimize power consumption. The maximum power dissipation is 1 watt at 25° C. Derate linearly above 35° C to 500 mW at 70°C (-15 mW/° C above 35°C). Power dissipation for the device is given by:

$$P = (V+ - V_{FLED})\,(I_{SEG})\,(n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{seg} is the number of "ON" segments. If the device is operated at elevated temperatures, the segment current can be limited through the brightness input to keep power dissipation within the limits described above.

The display may be blanked (all segments OFF) by applying the input code 1111 or by driving the brightness pin witha logic). If brightness control is not needed, pin 5 should be tied to 5.0 V.

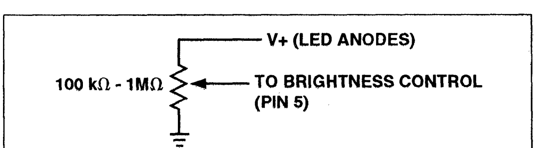


Figure 2. Brightness Control

Input Configuration and Output Codes

The TC7211AM accepts a 4-bit, true binary (positive level = logic "1") input at pin 27 (LSB) through pin 30 (MSB). The binary input is decoded to the 7-segment output known as Code B. The output display format is 0 to 9, —, E, H, L, P and blank display (see Table I). Segment assignments are shown in Figure 3. The TC7211AM will correctly decode binary and BCD true codes to a 7-segment output.

The TC7211A accepts multiplexed binary or BCD input data at pin 27 (LSB) through pin 30 (MSB). Pins 31 (LSD) through 34 (MSD) are the digit select lines. When the digit select line is taken to logic "1", input data is decoded and stored in the enabled output latch of the selected digit. More than one digit select line may be activated simultaneously. The same character will be written into all selected digits. (See Figure 5 for decoder segment assignments.)

Table I. Output Code

Binary Input				
B3	B2	B1	B0	Code B
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

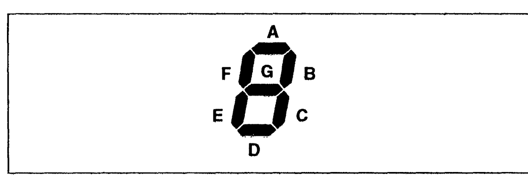


Figure 3. Segment Assignment

4-DIGIT CMOS DISPLAY DECODER/DRIVER

Special Order Decoder Option

The TC7211A is mask programmed to give the 16 combinations of 7-segment output codes. For large volume orders (50K pieces minimum), custom decoder options are available. Contact Teledyne Components for details.

Applications Information

The TC7212 A has two ground pins. Theses should be connected together.

TYPICAL APPLICATIONS

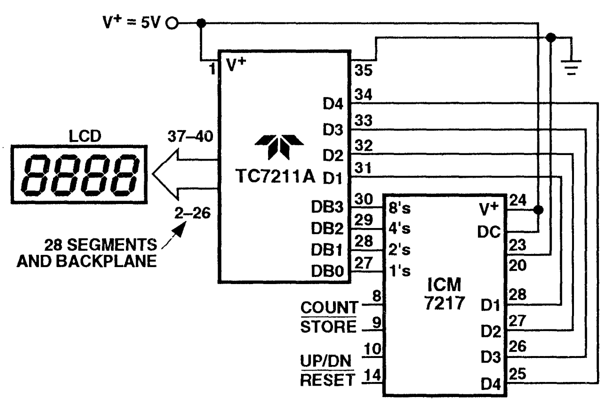


Figure 4. LCD Display Interface to 4-Digit Counter

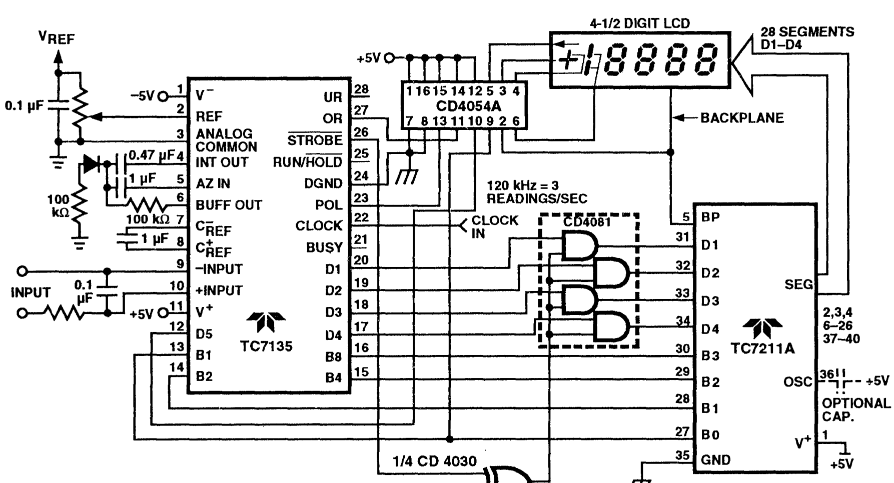


Figure 5: 4-1/2 Digit ADC Interfaced to LCD

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TYPICAL APPLICATIONS (Cont.)

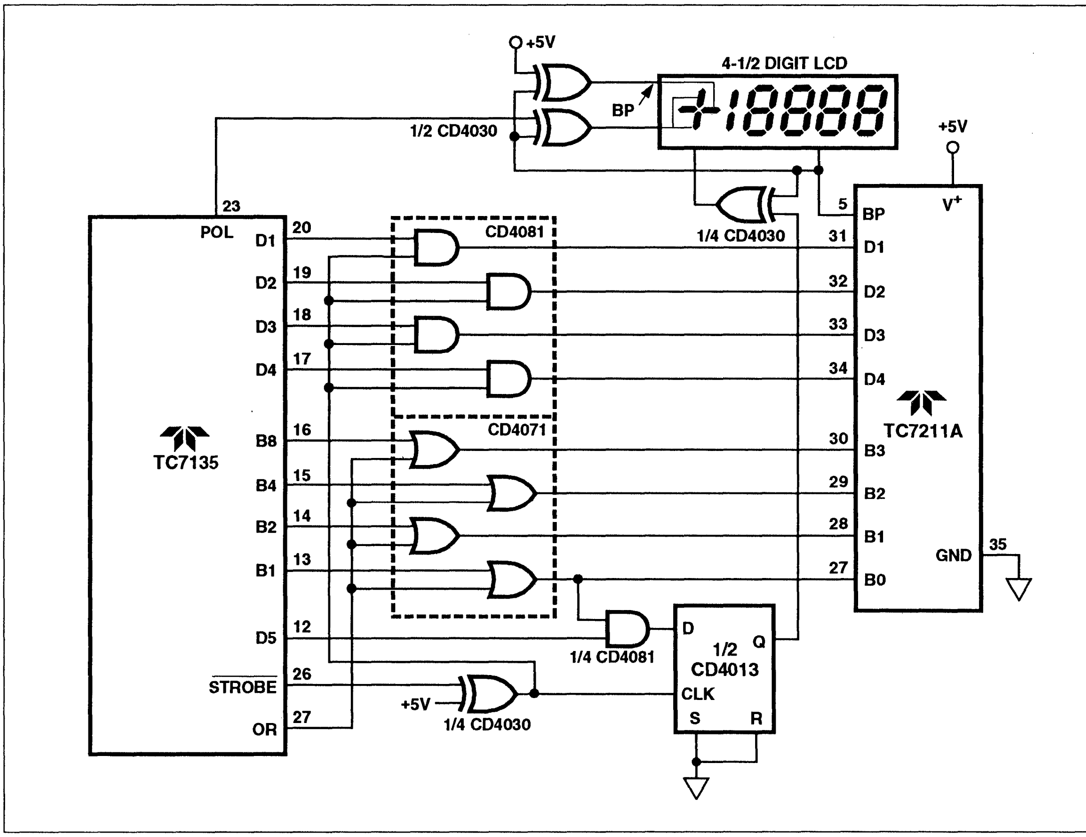


Figure 6. 4-1/2 Digit ADC Interfaced to LCD Display with Digit Blanking on Overrange

TYPICAL APPLICATIONS (Cont.)

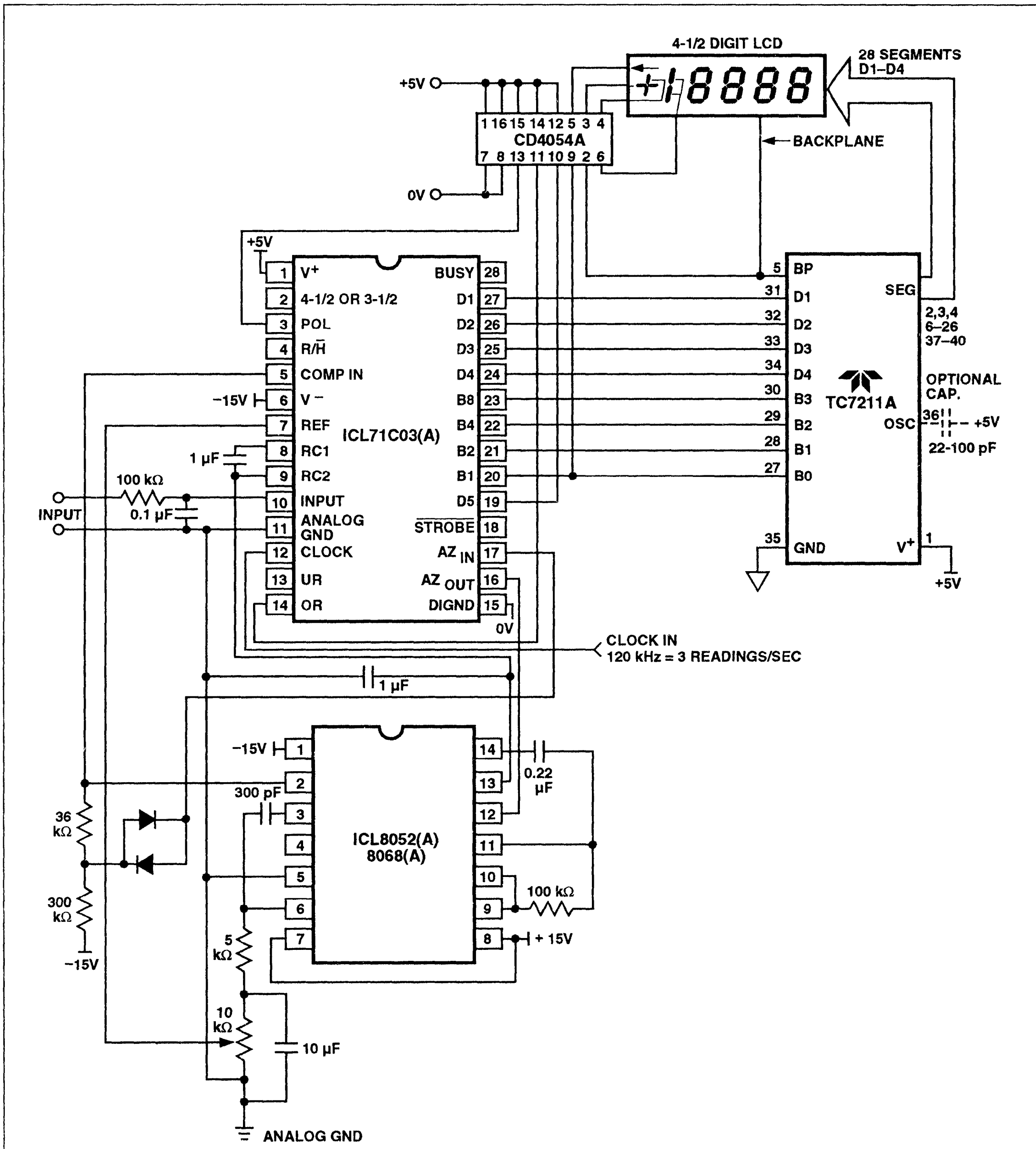


Figure 7. 4-1/2 Digit ADC Interfaced to LCD Display with Digit Blanking on Overrange

TYPICAL APPLICATIONS (Cont.)

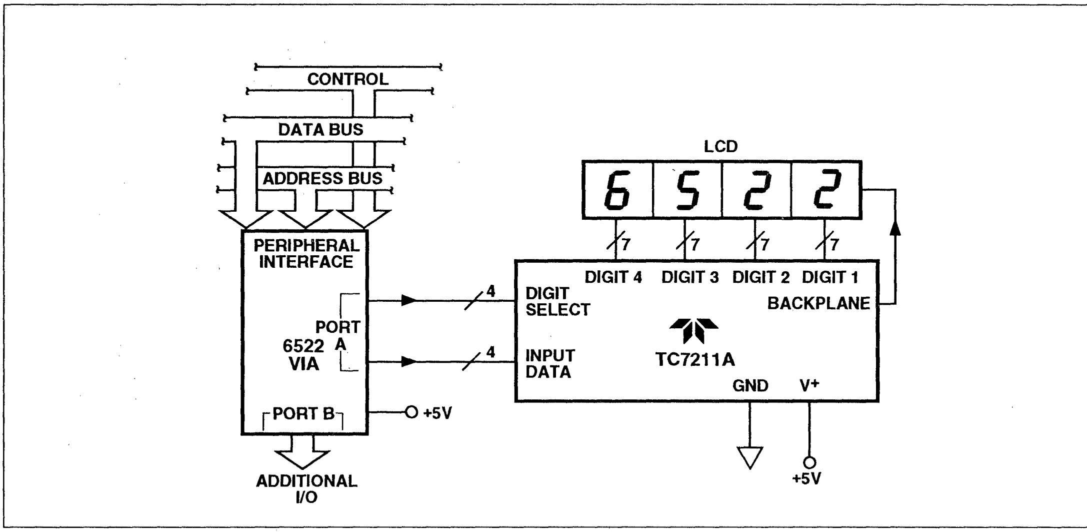


Figure 8: LCD Interface to SY6522 VIA

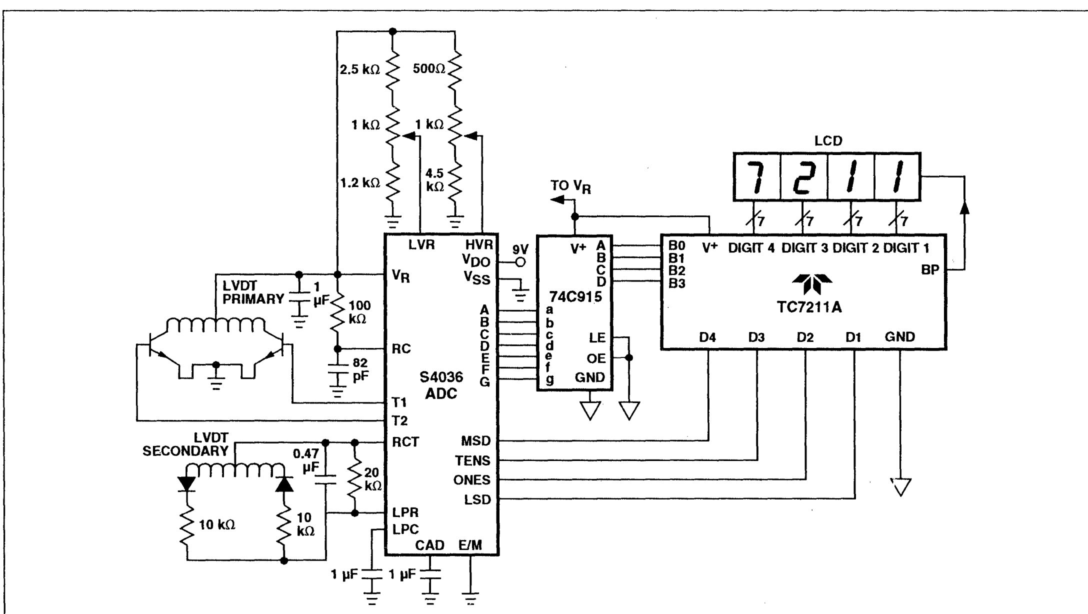


Figure 9: Digital Scale With LCD Readout

BUS COMPATIBLE 4-DIGIT CMOS DECODER/DRIVER

FEATURES

TC7211AM (LCD DRIVER)

- 4-Digit Non-Multiplexed 7-Segment LCD Outputs With Backplane Driver
- Input and Digit Select Data Latches
- RC Oscillator On-Chip Generates Backplane Drive Signal
- Eliminates DC Bias Which Degrades LCD Life
- Backplane Input/Output Pin Permits Synchronization of Cascaded Slave Device to a Master Backplane Signal
- Binary and BCD Inputs Decoded to Code B (0 to 9, —, E, H, L, P, Blank)
- Pin Compatible and Functionally Equivalent to ICM7211AM

TC7212AM (LED DRIVER)

- 28 Current Limited Outputs Drive Common-Anode LEDs at 8 mA Per Segment
- Input and Digit Select Data Latches
- Brightness Input Allows Potentiometer Control of LED Segment current. Pin Also Serves as Digital Display Enable
- Same Input Configuration and Output Decoding as the TCM7211AM
- Pin Compatible and Functionally Equivalent to ICM7212AM

GENERAL DESCRIPTION

The TC7211AM (LCD Decoder/driver) and TC7211AM are CMOS direct drive, 4-digit, 7-segment display decoder and driver. The devices are bus compatible making microprocessor controlled displays possible. Two chip select signals control data and digit select code latching prior to decoding and display. External data latches are unnecessary.

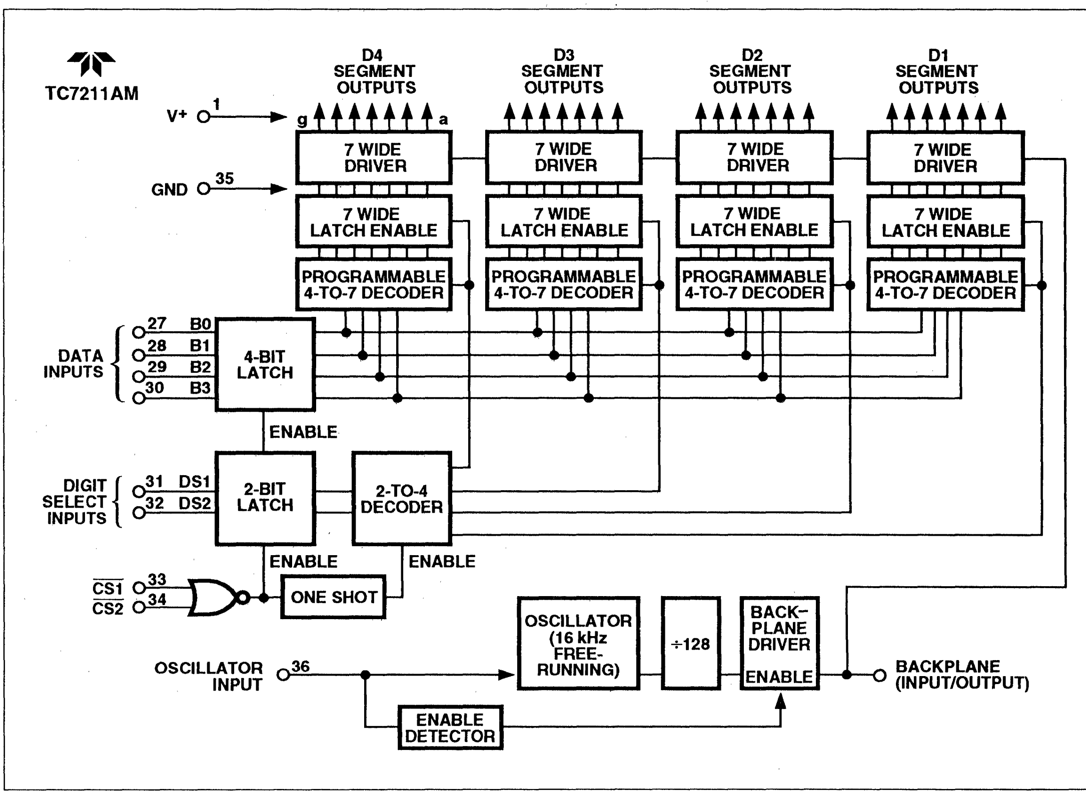
The TC7211AM drives conventional LCDs. An RC oscillator, divider chain, backplane driver, and 28-segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane, but in-phase for an OFF segment and out-of-phase for an ON segment. The net DC voltage applied between driver segment and backplane is near zero maximizing display lifetime.

The TC7212AM drives common-anode LED displays with 28 current controlled, low leakage, open drain, N-Channel output transistors. The brightness control input can be used as a digital display enable. A varying voltage at the control input will allow continous display brightness control.

The four bit binary input code is decoded into the seven segment alphanumeric code known as "Code B". The "Code B" output format results in a 0 to 9,—, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the seven segment display format.

TC7211AM
TC7212AM

FUNCTIONAL BLOCK DIAGRAM



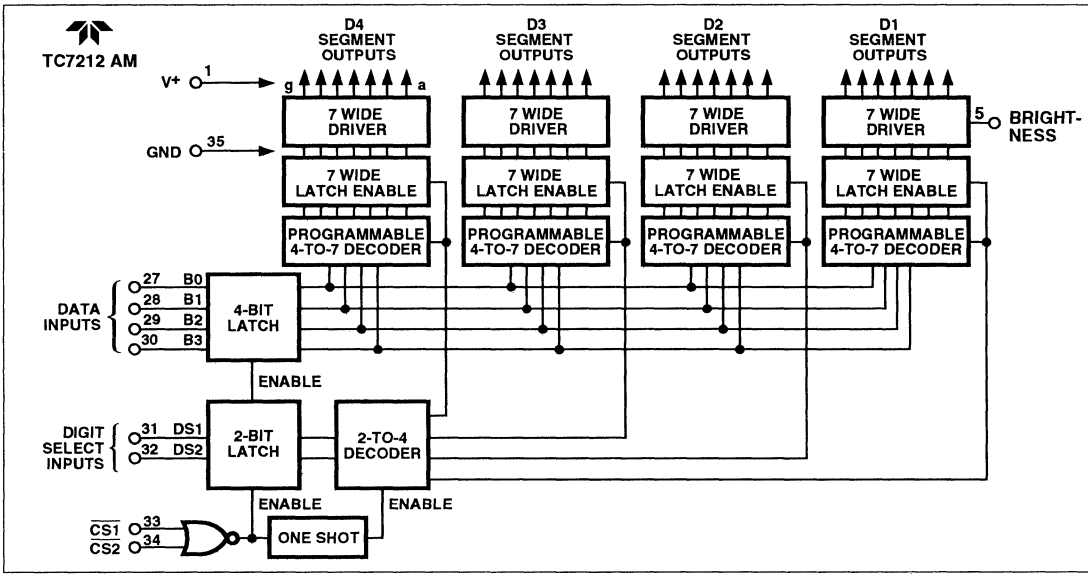
ORDERING INFORMATION

Part No.	Driver Type	Package	Input Code	Output Config.
TC7211AMIPL	LCD	40-Pin Plastic	Code B	Data and Digit Select Latches
TC7212AMIPL	LED	40-Pin Plastic	Code B	Data and Digit Select Latches

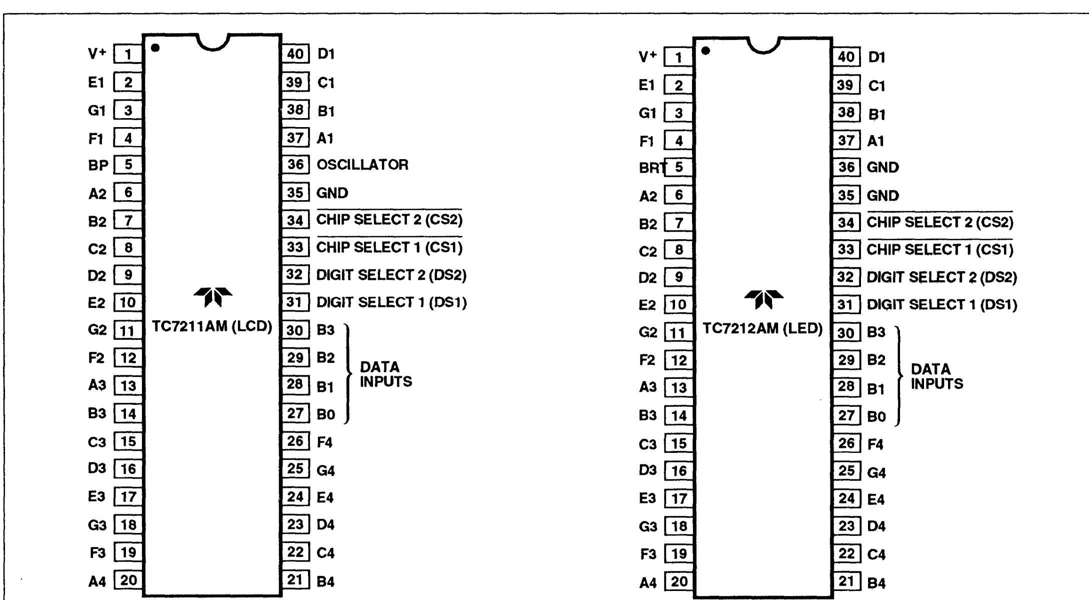
BUS COMPATIBLE, 4-DIGIT CMOS DECODER/DRIVER

TC7211AM
TC7212AM

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



TC7211AM
TC7212AM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... +6.5V
Input Voltage, Any Terminal
(Note 2) .... V^+ +0.3V, GND −0.3V
Power Dissipation (Note 1) .... 1W at +70°C
Operating Temperature Range .... −20°C to +85°C
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTES: 1. This limit refers to that of the package and will not be realized during normal operation.
2. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. For this reason, it is recommended that inputs from external sources not operating on the same power supply not be applied to the device before its supply is established, and, in multiple supply systems, the supply to the TC7211AM be turned on first.

TABLE I: OPERATING CHARACTERISTICS

Test Conditions: All parameters measured with V+ = 5V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
TC7211AM Characteristics (LCD Decoder/Driver)						
V_{SUP}	Operating Voltage Range		3	5	6	V
I_{OP}	Operating Current	Display Blank	—	10	50	μA
I_{OSCI}	Oscillator Input Current	Pin 36	—	±2	±10	μA
t_{RFS}	Segment Rise/Fall Time	C_L = 200 pF	—	0.5	—	μA
t_{RFB}	Backplane Rise/Fall Time	C_L = 5000 pF	—	1.5	—	μs
f_{OSC}	Oscillator Frequency	Pin 36 Floating	—	16	—	kHz
f_{BP}	Backplane Frequency	Pin 36 Floating	—	125	—	Hz
TC7212AM Characteristics (Common-Anode LED Decoder/Driver)						
V_{SUP}	Operating Voltage Range		4	5	6	V
I_{OP}	Operating Current	Pin 5 (Brightness),	—	10	50	μA
	Display Off	Pins 27-34 = GROUND				
I_{OP}	Operating Current	Pin 5 at V+, Display all 8's	—	200	—	mA
I_{SLK}	Segment Leakage Current	Segment Off	—	±0.01	±1	μA
I_{SEG}	Segment On Current	Segment On, V_{SO} = +3V	5	8	—	mA
Input Characteristics (LCD and LED Decoder/Driver)						
V_{IH}	Logic "1" High Input Voltage		3	—	—	V
V_{IL}	Logic "0" Low Input Voltage		—	—	1	V
I_{ILK}	Input Leakage Current	Pins 27–34	—	±0.01	±1	μA
C_{IN}	Input Capacitance	Pins 27–34	—	5	—	pF
I_{BPLK}	BP/Brightness Input Current Leakage	Measured at Pin 5 With Pin 36 at GND	—	±0.01	±1	μA
C_{BPI}	BP/Brightness Input Capacitance	All Devices	—	200	—	pF

TABLE I: OPERATING CHARACTERISTICS

Test Conditions: All parameters measured with V+ = 5V

AC Characteristics (LCD and LED Decoder/Driver)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{CSA}	Chip Select Active Pulse Width	(Note 3)	200	—	—	ns
t_{DS}	Data Setup Time		100	—	—	ns
t_{DH}	Data Hold Time		10	0	—	ns
t_{ICS}	Inter-Chip Select Time		2	—	—	µs

NOTE: 3. Other chip select (CS) is either held at logic zero or both CS1 and CS2 driven together.

TIMING DIAGRAMS

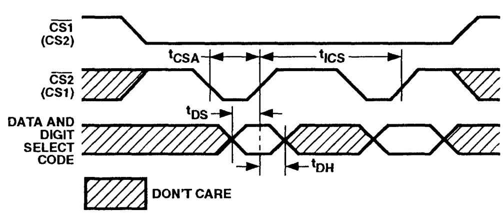


Figure 1: BUS Interface Timing Diagram (LED or LCD)

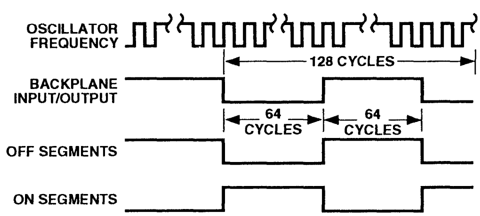


Figure 2: LCD Display Waveforms

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INPUT DEFINITIONS

In this table, V^+ and GND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

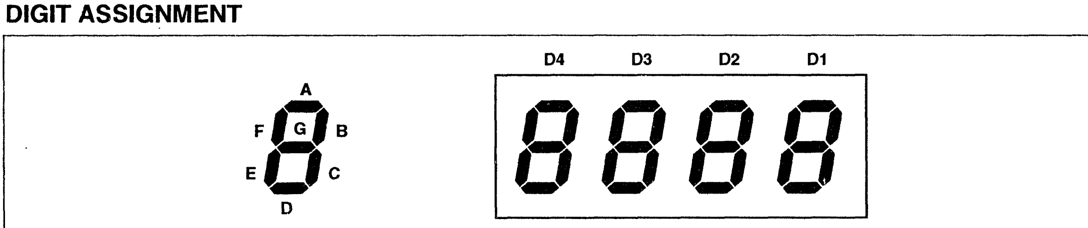
Input	Pin No.	Condition	Function	
B0	27	V^+ = Logic "1" GND = Logic "0"	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logic "1" GND = Logic "0"	Twos	Data Input Bits
B2	29	V^+ = Logic "1" GND = Logic "0"	Fours	Data Input Bits
B3	30	V^+ = Logic "1" GND = Logic "0"	Eights (Most Significant)	Data Input Bits
OSC	36	Floating or with external capacitor GND	Oscillator input. Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (pin 5)	
DS1	31	V^+ = Logical One	DS2, DS1 = 00 Selects D4 DS2, DS1 = 01 Selects D3 DS2, DS1 = 10 Selects D2 DS2, DS1 = 11 Selects D1	Digit Select Inputs
$\overline{DS2}$	32	GND = Logical Zero		
$\overline{CS1}$	33	V^+ = Inactive	When both $\overline{CS1}$ and $\overline{CS2}$ are low, the data and digit select input latches are open or enabled. On the rising of $\overline{CS1}$ or $\overline{CS2}$, data is latched, decoded and stored in the output drive latches.	
CS2	34	GND = Active		

OUTPUT DEFINITIONS

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

Output	Pin No.	Function				Output	Pin No.	Function			
A1	37	A	Segment Drive	Digit 1	(LSD)	A3	13	A	Segment Drive	Digit 3	
B1	38	B				B3	14	B			
C1	39	C				C3	15	C			
D1	40	D				D3	16	D			
E1	2	E				E3	17	E			
F1	4	F				F3	19	F			
G1	3	G				G3	18	G			
A2	6	A	Segment Drive	Digit 2		A4	20	A	Segment Drive	Digit 4	(MSD)
B2	7	B				B4	21	B			
C2	8	C				C4	22	C			
D2	9	D				D4	23	D			
E2	10	E				E4	24	E			
F2	12	F				F4	26	F			
G2	11	G				G4	25	G			

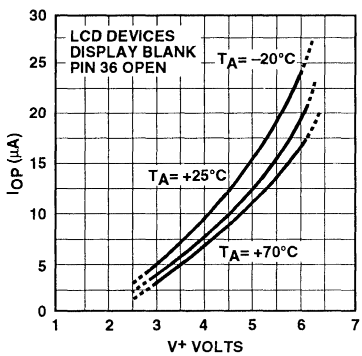
DIGIT ASSIGNMENT



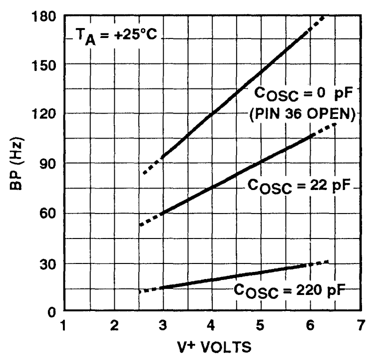
BUS COMPATIBLE, 4-DIGIT CMOS DECODER/DRIVER

TYPICAL OPERATING CHARACTERISTICS CURVES

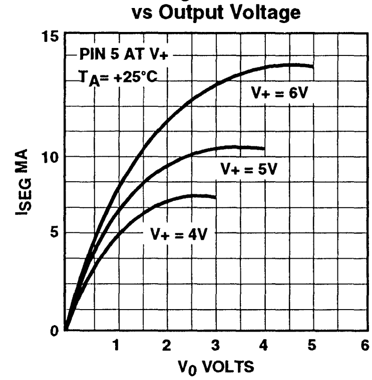
Operating Supply Current vs Supply Voltage



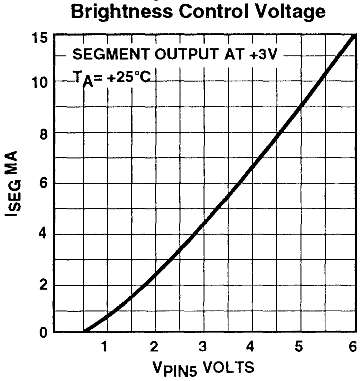
Backplane Frequency vs Supply Voltage



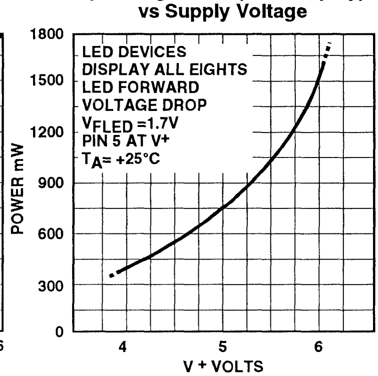
LED Segment Current vs Output Voltage



LED Segment Current vs Brightness Control Voltage



Operating Power (LED Display) vs Supply Voltage



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BASIC OPERATION

The TC7211AM drives 4-digit, 7-segment LCDs. This device contains 28 individual segment drivers, a backplane driver, a self-contained oscillator, and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N- and P-channel transistors for identical "ON" resistance. The equal resistances eliminate the DC output driver component resulting from unequal rise and fall times. This ensures maximum LCD life.

The backplane output driver can be disabled by grounding the OSCILLATOR input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane (BP) terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCDs with characters in multiples of four.

Each slave's backplane input represents only a 200 pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices drivable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half-inch characters with rise and fall times under 5 µs. This represents a system with three slave devices and a fourth master device driving the backplane. (See Figure 1.)

If more than four devices are slaved together, the backplane signal should be derived externally and all TC7211AM devices slaved to it. The external drive signal must drive a high capacitive load with 1µs to 2 µs rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures, the frequency may be reduced to compensate for display response time.

The on-chip RC oscillator free-runs at approximately 16 kHz. A ÷128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal and V^+. (See typical operating characteristics curves.)

The free-running oscillator may be overridden (if desired) by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or low portion, as this will result in a DC drive component being applied to the LCD, limiting the LCD's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range.

The oscillator input signal duty cycle is skewed so the low portion duration is less than 1 µs. The backplane disable sensing circuit will not respond to such a short signal.

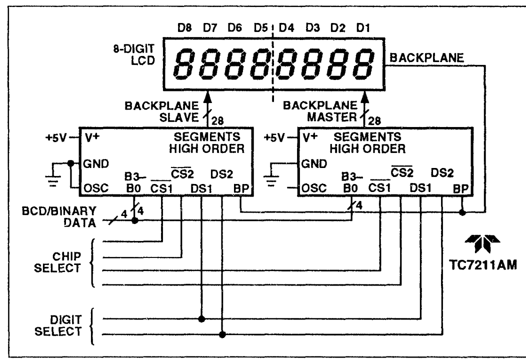


Figure 3. TC7211AM Driving an 8-Digit LCD Display in Master/Slave Configuration

TC7212AM LED Decoder/Driver

The TC7212AM directly drives 4-digit, 7-segment, common-anode LED displays. The 28 segment drivers are low leakage, current controlled, open drain N-channel MOS transistors.

A brightness input (pin 5) can be used in two ways to control output transistor drain current. The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment drivers "ON" resistance. A variable brightness control may be implemented with a single potentiometer (Figure 4). A high value potentiomenter (100 kΩ to 1MΩ) will minimize power consumption.

The brightness input may also be operated digitally as a display enable. At a logic 1 the display is fully "ON" and at a logic signal of varying duty cycle also. When operating with LEDs at a higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperature rise. The maximum power dissipation is 1 watt at 25° C. Derate linearly above 35°C to 500 mW at 70°C (-15 mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V+ - V_{FLED}) (I_{SEG}) (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{seg} is the number of "ON" segments. If the device is operated at elevated temperatures, the segment current can be limited through the brightness input to keep power dissipation within the limits described above.

The display may be blanked (all segments OFF) by applying the input code 1111 or by driving the brightness pin witha logic). If brightness control is not needed, pin 5 should be tied to 5.0 V.

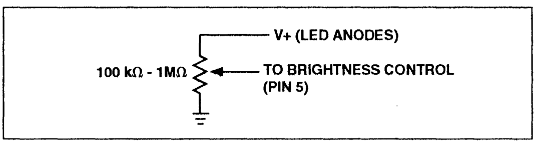


Figure 4. Brightness Control

Input Configuration and Output Codes

The TC7211AM accepts a 4-bit, true binary (positive level = logic "1") input at pin 27 (LSB) through pin 30 (MSB). The binary input is decoded to the 7-segment output known as Code B. The output display format is 0 to 9, —, E, H, L, P and blank display (see Table I). Segment assignments are shown in Figure 2. The TC7211AM will correctly decode binary and BCD true codes to a 7-segment output.

The TC7211AM is designed to interface with a data bus and display data under microprocessor control. Four data inputs (pins 27–30) and two digit select input bits (pins 31 and 32) are written into input buffer latches. The rising edge of either chip select causes data to be latched, decoded and stored in the selected digit ouptut data latch. The 2-bit digit code selects the appropriate output digit latch. The 4-bit display data word is decoded to the "Code B" 7-segment output format.

For applications where bus compatibility is not required, refer to the TC7211A (LCD) 4-digit decoder driver datasheet. This device is designed to accept multiplexed BCD/binary input data for display under the control of four separate digit select control signals.

Table 1: Output Code

Binary Input				
B3	**B2**	**B1**	**B0**	**Code B**
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	Blank

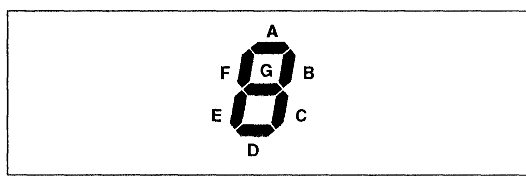


Figure 2. Segment Assignment

Special Order Decoder Option

The TC7211A is mask programmed to give the 16 combinations of 7-segment output codes. For large volume orders (50K pieces minimum), custom decoder options are available. Contact Teledyne Components for details.

Applications Information

The TC7212AM has two ground pins. These pins should be connected together.

NOTES

TELEDYNE COMPONENTS

SERIAL INPUT/16-BIT PARALLEL OUTPUT PERIPHERAL DRIVER

FEATURES

- **High Voltage Outputs 15V**
- **High Output Current Sink Capability .... 60 mA**
- **Low Standby Power .... 20 mW**
- **High-Speed Operation .... 3 MHz**
- **16 Parallel Outputs**
- **Cascading Possible for Longer Data Words**

APPLICATIONS

- **Incandescent Lamp Driver**
- **Thermal Printhead Driver**
- **LED Bar-Graph Driver**
- **High Current, Microprocessor Serial Port Extender**
- **Relay/Solenoid Driver**
- **Tungsten Lamp Driver**
- **SCR Gate Driver**

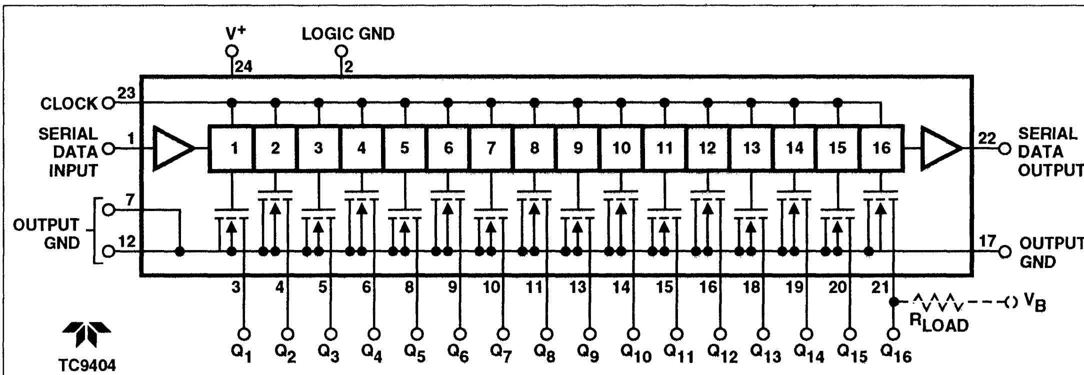
GENERAL DESCRIPTION

The TC9404 is a serial input/16-bit parallel output shift register. High output power MOS switching transistors make the TC9404 an ideal interface circuit between microprocessor I/O ports and high current/voltage peripherals. The CMOS construction limits quiescent power dissipation to 20 mW.

The TC9404 common-source, open-drain MOS outputs sustain 15V in the OFF state and maintain leakage currents under 100 μA. The 16 parallel outputs continuously sink 60 mA ($V_{SAT} \leq 0.5V$).

Successive connection of serial data outputs to serial data inputs makes longer length serial-to-parallel conversions possible. Device cascading makes the TC9404 an ideal thermal printhead or high-resolution LED bar-graph driver.

SIMPLIFIED SCHEMATIC



NOTE: Logic "1" serial data input bit turns output NMOS on.

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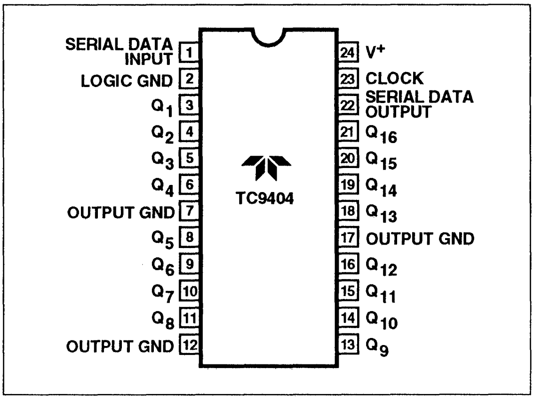
SERIAL INPUT/16-BIT PARALLEL OUTPUT PERIPHERAL DRIVER

TC9404

PIN CONFIGURATION



ORDERING INFORMATION

Part No.	Package	Temperature Range	Output Voltage
TC9404CPG	24-Pin Plastic DIP	0°C to +70°C	15V
TC9404IJG	24-Pin CerDIP	–25°C to +85°C	15V
TC9404MJG	24-Pin CerDIP	–55°C to +125°C	15V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to Logic Ground) 7V
Digital Logic Input Voltage 5.5V
Parallel Output Drain Voltage 22V
Parallel Output Drain Current .... 80 mA
Logic Ground to Output Ground
  Potential Difference .... 100 mV
Package Power Dissipation
  CerDIP .... 1W @ +85°C
  CerDIP .... 0.4W @ +125°C
  Plastic Package .... 1W @ +70°C
Operating Temperature
  CerDIP (IJ) .... $-25°C \le T_A \le +85°C$
  CerDIP (MJ) .... $-55°C \le T_A \le +125°C$
  Plastic Package(CP) .... $0°C \le T_A \le +70°C$
Storage Temperature .... $-65°C \le T_A \le +150°C$
Lead Temperature (Soldering, 60 sec) .... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = 5V, 0°C ≤ T_A ≤ +70°C for TC9404CPG and –25°C ≤ T_A ≤ +85°C for TC9404IJG, and –55°C to +125°C for TC9404MJG, unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Output						
V_{SAT}	Output ON Voltage	I_O = 60 mA V_S = 4.75V	—	0.35	0.5	V
V_B	Output OFF Voltage		—	—	15	V
I/O	Output Sink Current	V_{SAT} ≤0.5V (Note 1)	60	—	—	mA
I_{OX}	Output Leakage Current	V_S = 4.75V, V_B = 15V	—	—	100	µA
V_{OH}	Serial Output Logic "1" Voltage	I_{OH} = 400 µA I_{OH} = 10 µA	2.4 4.5	— —	— —	V V
V_{OL}	Serial Output Logic "0" Voltage	I_{OL} = 5 mA	—	—	0.4	V
Input						
V_{INH}	Logic "1" Input Voltage	V_S = 5.25V	3.3	—	—	V
V_{INL}	Logic "0" Input Voltage	V_S = 5.25V	—	—	0.8	V
I_{INH}	Logic "1" Input Current	V_S = 5.25V	—	—	20	V
I_{INL}	Logic "0" Input Current	V_{INL} = 0.4V V_S = 5.25V	—	—	400	µA
C_{IN}	Input Capacitance	V_{INL} = 0V	—	15	—	µA
Timing						
t_{DH}	Serial Input Data Hold Time		20	0	—	ns
t_{DS}	Serial Input Data Set-Up Time		100	70	—	ns
t_{CP}	Clock Frequency		3	5	—	MHz
t_{PW}	Clock Pulse Width		150	100	—	ns
t_{PLH}	Parallel Output Low-to-High Transition Time	V_B = 15V R_L = 330Ω C_L = 25 pF	—	—	150	ns
t_{PHL}	Parallel Output High-to-Low Transition Time	V_B = 15V R_L = 330Ω C_L = 25 pF	—	—	150	ns
t_{SLH}	Serial Output Low-to-High Transition Time	I_{OH} = 400 µA C_L = 25 pF	—	—	150	ns
t_{SHL}	Serial Output High-to-Low Transition Time	I_{OL} = 5 mA C_L = 25 pF	—	—	75	ns
Power						
V_S	Operating Supply Voltage		4.75	5	5.25	V
I_S	Quiescent Power Supply	V_S = 5.25V f_C = 0 Hz V_{IHL} = 0V I_O = 0 mA Pin 22 Open	—	1	4	mA

NOTE 1. Maintain chip temperature ≤150°C.

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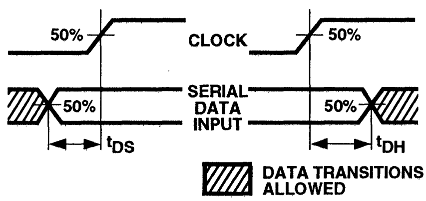
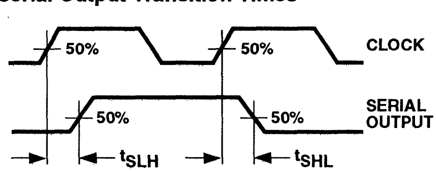
TC9404

TIMING DIAGRAMS

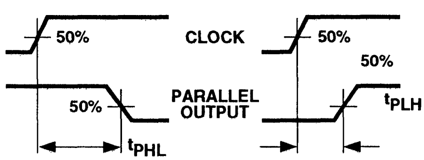
a) Serial Input Data Hold and Set-Up Times



b) Serial Output Transition Times



c) Parallel Output Transition Times



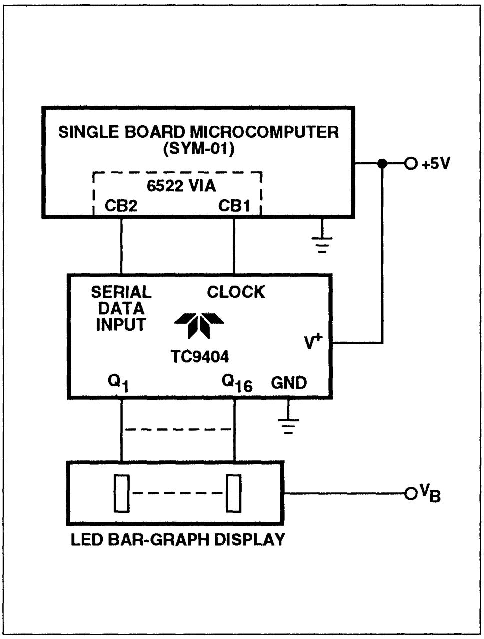
FUNCTION TABLE

Data Input D_N	Clock Input	Parallel Outputs Q_1	Q_2	Q_3	...Q_{16}
X	L	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_3}$	...$\overline{D_{16}}$
H	↗	L*	$\overline{D_1}$	$\overline{D_2}$	...$\overline{D_{15}}$
L	↗	H*	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_{15}}$

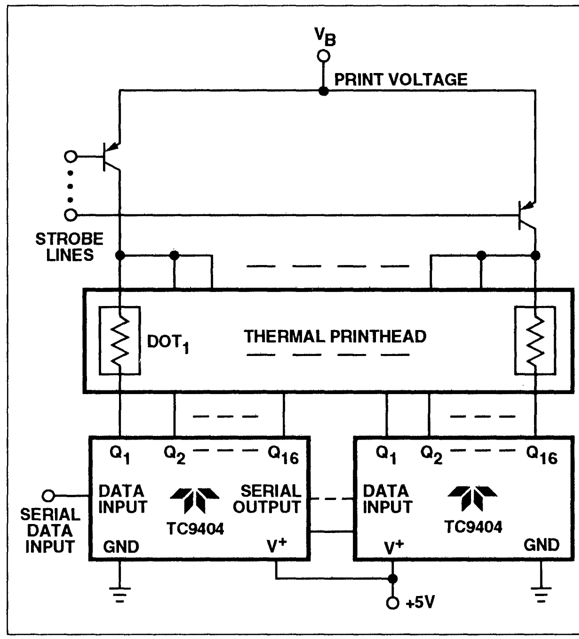
L = Logic 0
H = Logic 1
L* = Output NMOS ON
H* = Output NMOS OFF
X = Don't Care
↗ = Transition from Low-to-High
D_1, D_2, ...D_{16} = Data inputs at clock time T_{-N}.
Data is inverted at the parallel outputs.

APPLICATIONS

Microprocessor-Controlled LED Bar-Graph Display



Thermal Printhead Driver



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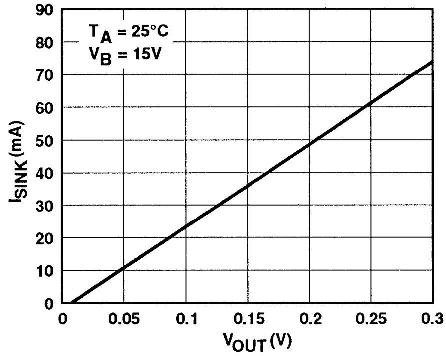
NOTES

TELEDYNE COMPONENTS

16-BIT PARALLEL-LATCHED OUTPUT PERIPHERAL DRIVER

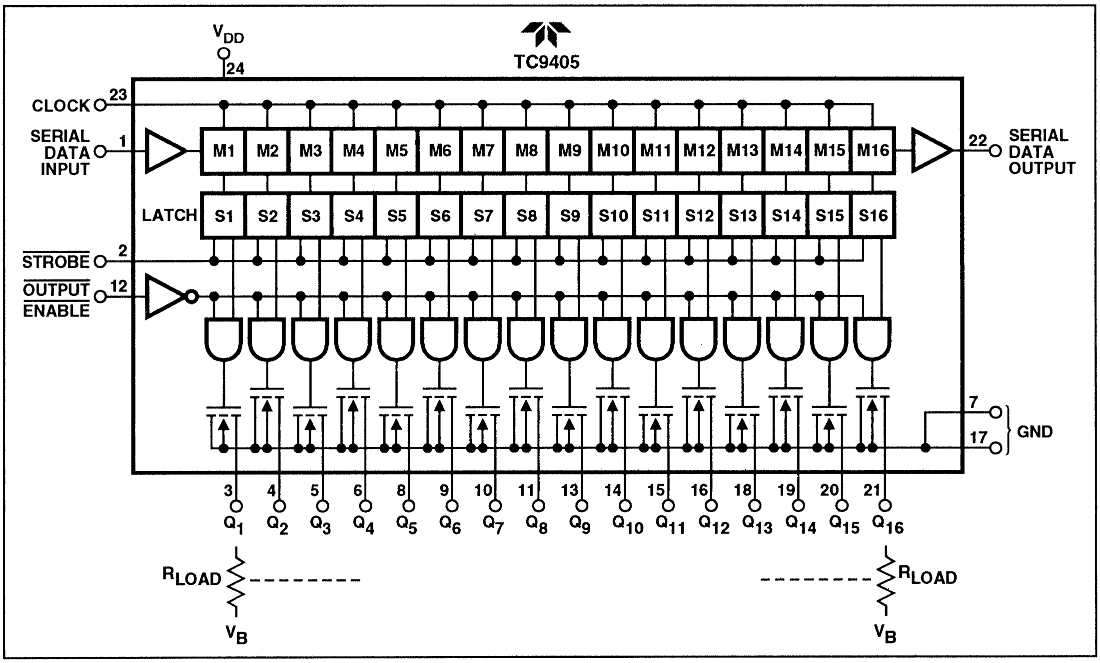
Saturation Voltage vs Sink Current



FEATURES

- High Voltage Outputs 15V
- High Output Current Sink Capability ...... 60 mA
- Low Standby Power .... 1 mW
- High-Speed Operation .... 3 MHz
- 16 Latched Parallel Outputs
- Cascading Possible for Longer Data Words
- Dual-Rank Latches and $\overline{\text{STROBE}}$ Input for Ripple-Free Data Update
- $\overline{\text{OUTPUT ENABLE}}$ Input Disables Outputs Without Corrupting Data

FUNCTIONAL DIAGRAM



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16-BIT PARALLEL-LATCHED OUTPUT PERIPHERAL DRIVER

TC9405

GENERAL DESCRIPTION

The TC9405 is a serial input, 16-bit parallel-latched output shift register. Master/slave data latches and high output power MOS switching transistors combine to make the TC9405 an ideal interface circuit between microprocessor I/O ports and high current/voltage peripherals. The CMOS construction limits quiescent power dissipation to 1 mW.

The TC9405 common-source, open-drain MOS outputs sustain 15V in the OFF state and maintain leakage currents under 100 µA. The low output ON resistance allows all 16 channels to simultaneously sink 60 mA with a saturation voltage of 0.5V maximum and power dissipation of 480 mW. Typical power dissipation of 16 channels sinking 60 mA is only 325 mW.

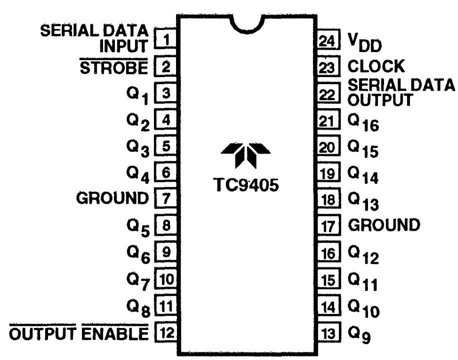
Dual rank latches and a $\overline{\text{STROBE}}$ input permit glitch-free data updating. With the $\overline{\text{STROBE}}$ input high, data is entered into master latches on each rising edge of the CLOCK input. When $\overline{\text{STROBE}}$ is brought low, data is transferred to the slave latches simultaneously. An $\overline{\text{OUTPUT ENABLE}}$ ($\overline{\text{OE}}$) input is also included, so that all outputs can be turned off. Both $\overline{\text{STROBE}}$ and $\overline{\text{OUTPUT ENABLE}}$ are asynchronous, level-sensitive inputs.

Successive connection of serial data outputs to serial data inputs make longer length serial-to-parallel conversions possible. Device cascading makes the TC9405 an ideal thermal printhead, high-resolution LED bar-graph, or incandescent lamp driver.

APPLICATIONS

- Incandescent Lamp Driver
- Thermal Printhead Driver
- LED Bar-Graph Driver
- High Current, Microprocessor Serial Port Expander
- Relay/Solenoid Driver
- Tungsten Lamp Driver
- SCR Gate Driver

PIN CONFIGURATIONS



ORDERING INFORMATION

Part	Package	Temperature Range	Output Voltage
TC9405CPG	24-Pin Plastic DIP	0°C to +70°C	15V
TC9405IJG	24-Pin CerDIP	–25°C to +85°C	15V
TC9405MJG	24-Pin CerDIP	–55°C to +125°C	15V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to Ground) 7V
Digital Logic Input voltage 5.5V
Parallel Output Drain Voltage 18V
Parallel Output Drain Current .... 80 mA
Package Power Dissipation
  CerDIP Package .... 1W @ 85°C
  CerDIP Package .... 0.4W @ 125°C
  Epoxy Package .... 1W @ 70°C

Operating Temperature
  CerDIP Package (IJG)........ $-25°C \leq T_A \leq +85°C$
  CerDIP Package (MJG)...... $-55°C \leq T_A \leq +125°C$
  Epoxy Package (CPG) .... $0°C \leq T_A \leq +70°C$
Storage Temperature.......... $-65°C \leq T_A \leq +150°C$
Lead Temperature (Soldering, 60 sec) .... +300°C

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V **T_A**
TC9405C .... 0°C to +70°C
TC9405I .... –25°C to +85°C
TC9405M .... –55°C to +125°C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{INH}	Logic 1 Input Voltage	V_{DD} = 5.25V	2.4	—	—	V
V_{INL}	Logic 0 Input Voltage	V_{DD} = 5.25V	—	—	0.8	V
I_{INH}	Logic 1 Input Current	V_{INH} = 2.4V V_{DD} = 5.25V	—	—	40	µA
I_{INL}	Logic 0 Input Current	V_{INL} = 0.8V V_{DD} = 5.25V	—	—	40	µA
C_{IN}	Input Capacitance	V_{IN} = 0V	—	15	—	pF
V_{OH}	Serial Output Logic 1 Voltage	I_{OH} = 400 µA I_{OH} = 10 µA	2.4 4.5	4.7 4.98	— —	V V
V_{OL}	Serial Output Logic 0 Voltage	I_{OL} = 3.6 mA	—	—	0.4	V
Output						
V_{SAT}	Output ON Voltage	I_O = 60 mA V_{DD} = 4.75V, T_A = 24°C (Note 2)	—	0.25	0.4	V
V_{SAT}	Output ON Voltage	I_O = 60 mA V_{DD} = 4.75V, T_A = FULL (Note 2)	—	—	0.6	V
V_B	Output OFF Voltage				15	V
I_O	Output Sink Current	$V_{SAT} \leq 0.6V$ (Note 1)	60	—	—	mA
I_{OX}	Output Leakage Current	V_{DD} = 4.75V V_B = 15V	—	—	100	µA

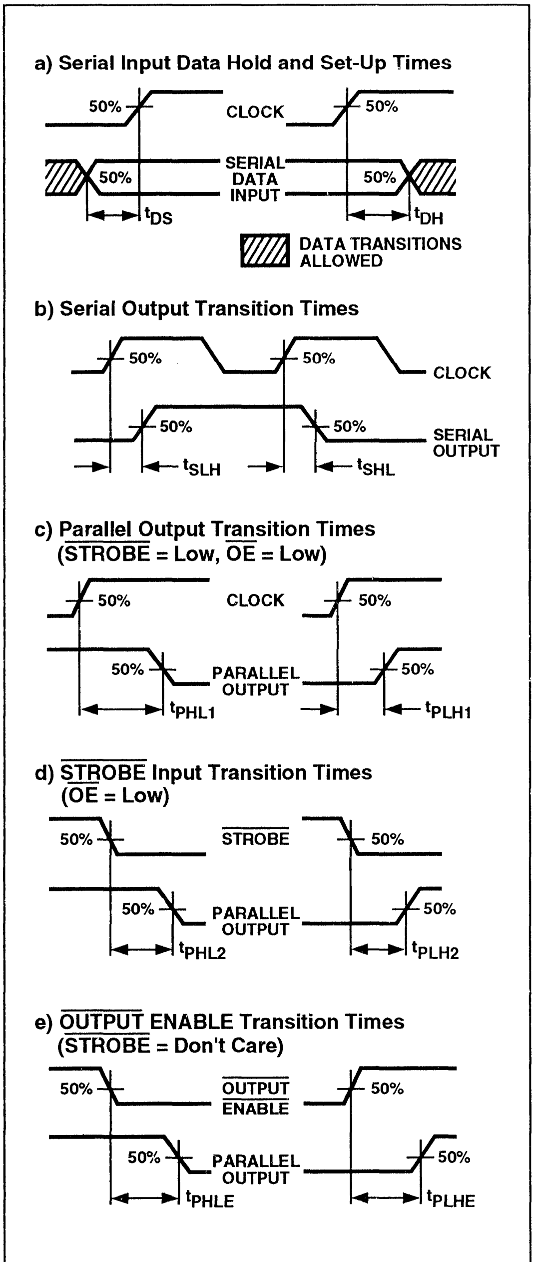
TC9405

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Timing						
t_{DH}	Serial Input Data Hold Time	$T_A = 25°C$	40	20	—	ns
t_{DS}	Serial Input Data Set-Up Time	$T_A = 25°C$	50	0	—	ns
f_C	Maximum Clock Frequency	$T_A = 25°C$	3	5	—	MHz
t_{PW}	Clock Pulse Width	$T_A = 25°C$	150	100	—	ns
t_{PLH1}	Parallel Output Low-to-High Transition Time	$\overline{STROBE}$ = LOW $\overline{OE}$ = LOW (Note 3 and Figure 1)	—	—	300	ns
t_{PHL1}	Parallel Output High-to-Low Transition Time	$\overline{STROBE}$ = LOW $\overline{OE}$ = LOW (Note 3 and Figure 1)	—	—	300	ns
t_{PLH2}	Parallel Output Low-to-High Transition Time	$\overline{STROBE}$ = $\overline{OE}$ = LOW (Note 3 and Figure 1)	—	—	300	ns
t_{PLHL2}	Parallel Output High-to-Low Transition Time	$\overline{STROBE}$ = $\overline{OE}$ = LOW (Note 3 and Figure 1)	—	—	300	ns
t_{PLHE}	Parallel Output Low-to-High Transition Time	$\overline{STROBE}$ = Don't Care $\overline{OE}$ = (Note 3 and Figure 1)	—	—	250	ns
t_{PHLE}	Parallel Output High-to-Low Transition Time	$\overline{STROBE}$ = Don't Care $\overline{OE}$ = (Note 3 and Figure 1)	—	—	250	ns
t_{SHL}	Serial Output High-to-Low Transition Time	$I_{OL} = 3.6$ mA $C_L = 25$ pF, $T_A = 25°C$	—	—	150	ns
t_{SLH}	Serial Output Low-to-High Transition Time	$I_{OH} = 400$ μA $C_L = 25$ pF, $T_A = 25°C$	—	—	150	ns
t_{SPW}	Strobe Pulse Width	$T_A = 25°C$	80	—	—	ns
Supply						
V_{DD}	Operating Supply Voltage		+4.75	+5	+5.25	V
I_S	Quiescent Power Supply	$V_{DD} = 5.25V$, $f_C = 0$ Hz $V_{INL} = 0V$, $I_O = 0$ mA Pin 22 Open	—	50	200	μA

NOTES:
1. Maintain die temperature ≤ 150°C.
2. V_{SAT} increases by 0.1V when all outputs are sinking 60 mA due to internal ground drop and self-heating.
3. $V_B = 15V$, $R_L = 330\Omega$, $C_L = 25$ pF, $T_A = 25°C$.

Figure 1. Timing Diagrams



FUNCTION TABLE

$\overline{OE}$	$\overline{STROBE}$	Data Input (D_N)	Clock Input	Parallel Outputs Q_1	Q_2	Q_3	...Q_{16}
L	L	X	L	D_1	D_2	D_3	...D_{16}
L	L	H	↑	L*	D_1	D_2	...D_{15}
L	L	L	↑	H*	D_1	D_2	...D_{15}
L	H	X	X	Maintains Last Valid State			
H	X	X	X	H*	H*	H*	H*

L = Logic 0
H = Logic 1
L* = Output NMOS ON
H* = Output NMOS OFF
X = Don't Care
↑ = Transition from low-to-high
D_1, D_2, ...D_{16} = Data outputs before the low-to-high transition of the clock

NOTE: $\overline{OE}$ and $\overline{STROBE}$ inputs are level-sensitive, not edge-triggered.

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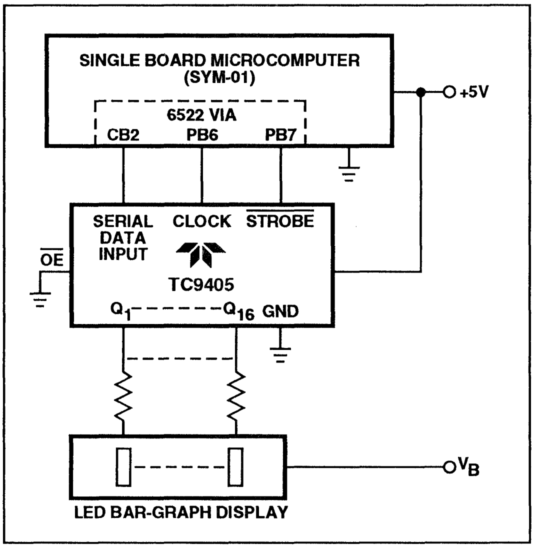
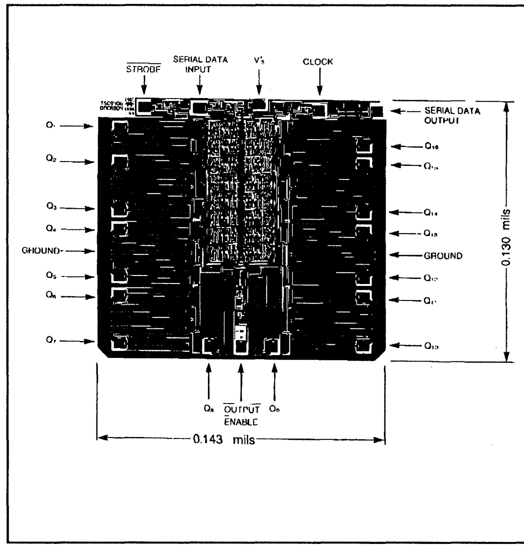
APPLICATIONS

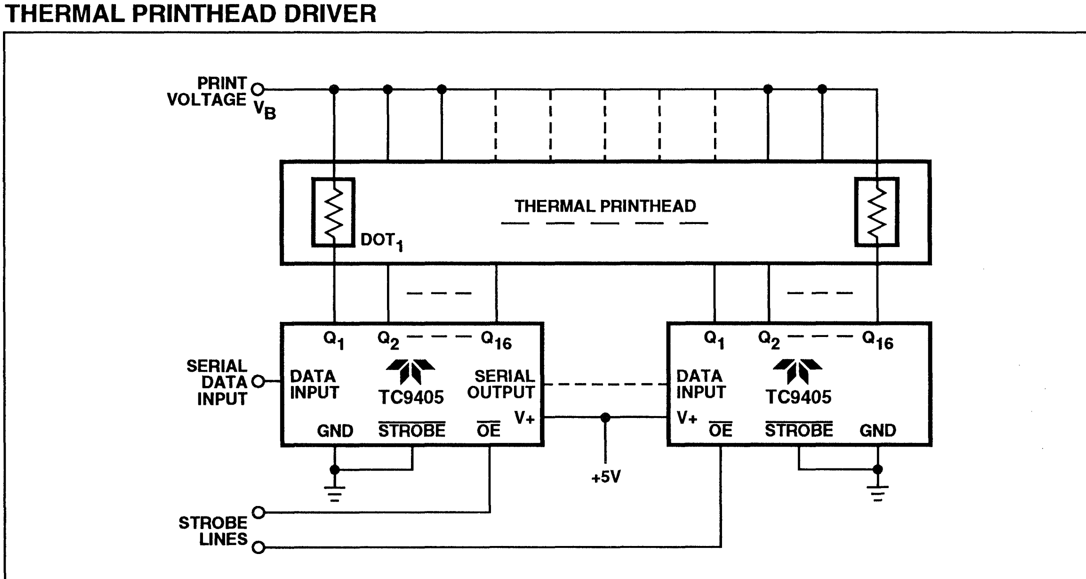
MICROPROCESSOR CONTROLLED LED BAR-GRAPH DISPLAY



BONDING DIAGRAM



THERMAL PRINTHEAD DRIVER



Section 12

Analog Switches and Multiplexers

MONOLITHIC CMOS/DMOS, QUAD SPST ANALOG SWITCH

FEATURES

- High OFF Isolation ....66 dB @ 10 MHz
- Wide Bandwidth Switches ....–1 dB @ 100 MHz
- Low Channel-to-Channel Cross Talk ....–80 dB @ 10 MHz
- TTL Compatible
- Industry-Standard Pinout

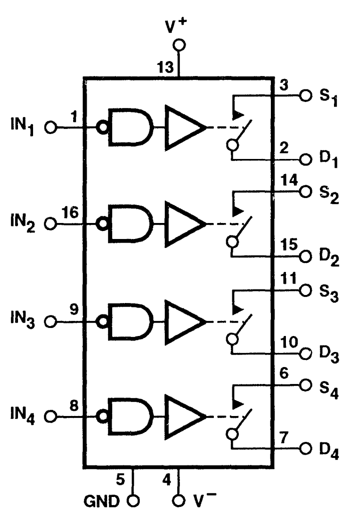
APPLICATIONS

- Glitch-Free Analog Switching
- RF and Video
- Track-and-Hold
- Sample-and-Hold

GENERAL DESCRIPTION

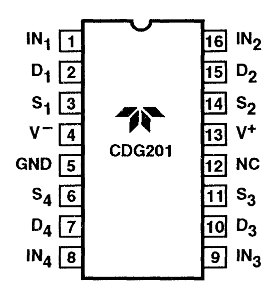
The CDG201 features TTL-compatible input logic and wideband lateral DMOS switches on a single chip. The on-chip reference used for TTL compatibility gives an added advantage of constant logic switching over a wide range of supply voltages and temperature without a separate power supply. Industry-standard pinout makes the CDG201 particularly suitable for replacing existing analog switches, while upgrading high-frequency performance.

FUNCTIONAL BLOCK DIAGRAM



NOTES: 1. Four SPST switches per package.
2. Switches shown in logic "1" (OFF) position.
3. ON = Logic "0" ≤ 0.8V.
OFF = Logic "1" ≤ 2.4V.

PIN CONFIGURATION



NC = NO INTERNAL CONNECTION

CDG201

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
CDG201COE	16-Pin Plastic SO	0°C to +70°C
CDG201CPE	16-Pin Plastic DIP	0°C to +70°C
CDG201EOE	16-Pin Plastic SO	–40°C to +85°C
CDG201EPE	16-Pin Plastic DIP	–40°C to +85°C
CDG201EJE	16-Pin CerDIP	–40°C to +85°C
CDG201MJE	16-Pin CerDIP	–55°C to +125°C

RECOMMENDED OPERATING CONDITIONS

Negative Supply Voltage ....–8V to –15V
Positive Supply Voltage ....+8V to +15V
Control Input Voltage Range ....0V to +5V
Operating Temperature Range
- C Suffix ....0°C to +70°C
- E Suffix ....–40°C to +85°C
- M Suffix ....–55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ....±20V
Control Input Voltage Range ....V^+ +0.3V, V^- –0.3V
Continuous Current, Any Pin Except S or D ....20 mA
Continuous Current, S or D ....30 mA
Peak Pulsed Current, S or D,
80 µs, 1%, Duty Cycle ....90 mA
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....–65°C to +150°C
Power Dissipation
(Derate at 5.5 mW/°C, Above +85°C) ....500 mW

NOTE: All devices contain diodes to protect inputs against damage due to high-static voltages or electric fields. However, it is advised precautions be taken not to exceed maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (V_{DD} or GND). Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, V^- = –15V, V^+ = +15V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static						
V_{ANALOG}	Analog Signal Range		–10	—	+10	V
$r_{DS(ON)}$	Switch ON Resistance	V_S = –10V, V_{IN} = 0V	—	40	80	Ω
	V_S = +2V, V_{IN} = 0V	—	45	80	Ω	
	V_S = +10V, V_{IN} = 0V	—	100	160	Ω	
V_{IH}	High Level Input Voltage, Logic "1" (OFF)		2.4	—	—	V
V_{IL}	Low Level Input Voltage, Logic "0" (ON)		—	—	0.8	V
I_{IN}	Logic Input Leakage Current	V_{IN} = +2.4V	—	0.01	0.1	µA
	V_{IN} = +15V	—	0.02	0.1	µA	
$I_{D(OFF)}$	Switch OFF Leakage Current	V_D = +10V, V_S = –10V, V_{IN} = +2.4V	—	0.2	5	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_S = +10V, V_D = –10V, V_{IN} = +2.4V	—	0.4	5	nA
I^-	Negative Supply Quiescent Current	V_{IN} = 0V to +2.4V	—	–0.3	–1	mA
I^+	Positive Supply Quiescent Current	V_{IN} = 0V to +2.4V	—	0.6	2	mA
Dynamic						
t_{ON}	Switch Turn-On Time	See Switching Times Test Circuit	—	400	600	ns
t_{OFF}	Switch Turn-Off Time	See Switching Times Test Circuit	—	70	300	ns
OIRR	Off Isolation Rejection Ratio	f = 10 MHz, R_L = 50Ω	60	66	—	dB
CCRR	Cross-Coupling Rejection Ratio	f = 10 MHz, R_L = 50Ω	—	80	—	dB
C_D	Drain-Node Capacitance	V_D = V_S = 0V, f = 1 MHz, V_{IN} = +2.4V	—	0.3	—	pF
C_S	Source-Node Capacitance	V_D = V_S = 0V, f = 1 MHz, V_{IN} = +2.4V	—	3	—	pF

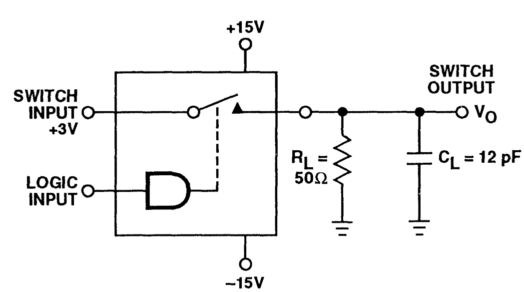
MONOLITHIC CMOS/DMOS, QUAD SPST ANALOG SWITCH

ELECTRICAL CHARACTERISTICS: $V^- = -15V$, $V^+ = +15V$

Limits at Temperature Extremes

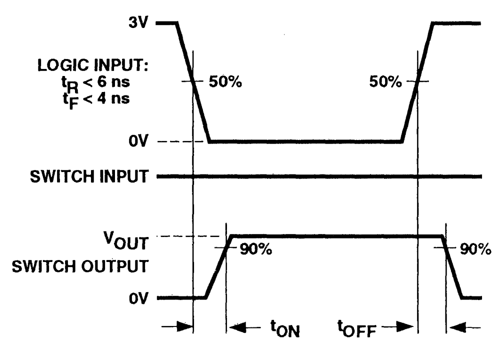
Symbol	Parameter	Test Conditions	Maximum @ T_A = −55°C	−40°C	+70°C	+85°C	+125°C	Unit
Static								
V_{ANALOG}	Analog Signal Range		±10	±10	±10	±10	±10	V
$r_{DS(ON)}$	Switch ON Resistance	$V_S = -10V$, $V_{IN} = 0V$	80	80	120	120	150	Ω
		$V_S = +2V$, $V_{IN} = 0V$	80	80	120	120	150	Ω
		$V_S = +10V$, $V_{IN} = 0V$	160	160	240	240	300	Ω
I_{IN}	Logic Input Leakage Current	$V_{IN} = +2.4V$	0.1	0.1	1	1	10	µA
		$V_{IN} = +15V$	0.1	0.1	2	2	20	µA
$I_{D(OFF)}$	Switch OFF Leakage Current	$V_D = +10V$, $V_S = -10V$, $V_{IN} = +2.4V$	5	5	100	100	1000	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	$V_S = +10V$, $V_D = -10V$, $V_{IN} = +2.4V$	5	5	100	100	1000	nA
I^-	Negative Supply Quiescent Current	V_{IN} = 0V to +2.4	−1	−1	−1	−1	−1	mA
I^+	Positive Supply Quiescent Current	V_{IN} = 0V to +2.4	2	2	2	2	2	mA

SWITCHING TIMES TEST CIRCUIT



NOTE: Switch shown in logic "1" (OFF) position.

TEST WAVEFORMS



$$V_{OUT} = \frac{R_L}{R_L + r_{DS(ON)}}$$

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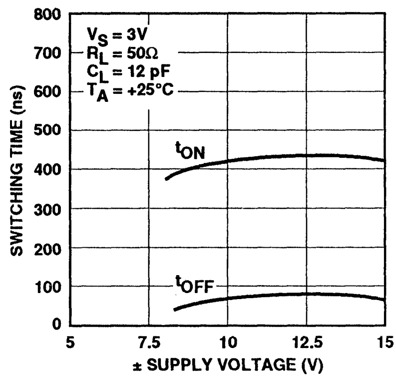
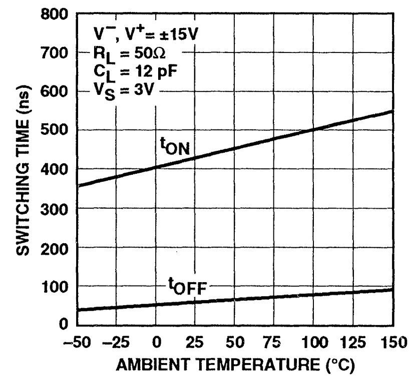
CDG201

TYPICAL CHARACTERISTICS CURVES

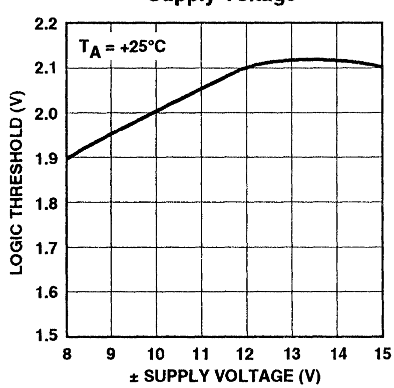
Switching Times vs Supply Voltage



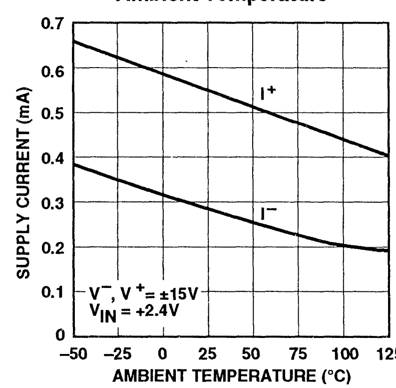
Switching Times vs Ambient Temperature



Logic Threshold vs Supply Voltage

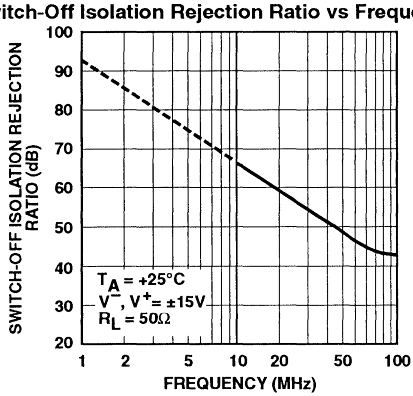


Supply Currents vs Ambient Temperature

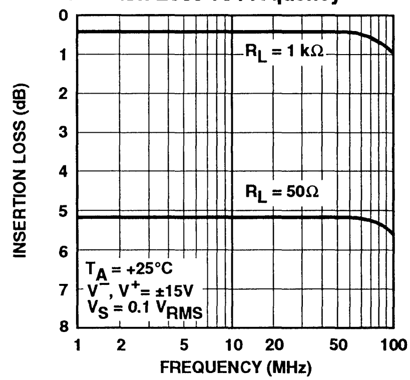


TYPICAL CHARACTERISTICS CURVES (Cont.)

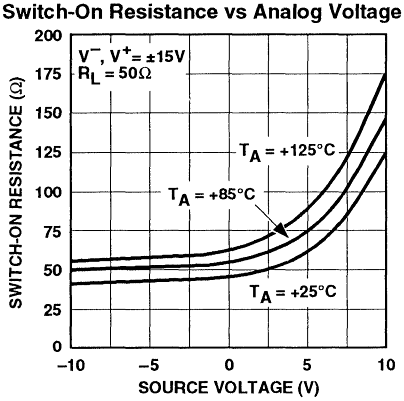
Switch-Off Isolation Rejection Ratio vs Frequency



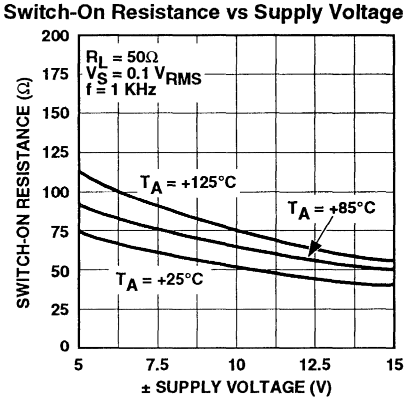
Insertion Loss vs Frequency



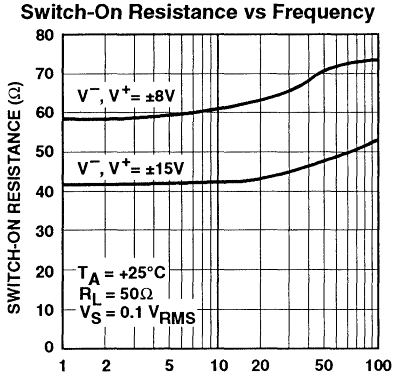
Switch-On Resistance vs Analog Voltage



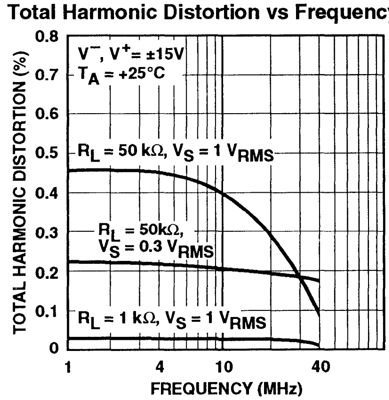
Switch-On Resistance vs Supply Voltage



Switch-On Resistance vs Frequency



Total Harmonic Distortion vs Frequency



NOTES

QUAD MONOLITHIC, SPST CMOS/DMOS ANALOG SWITCH

FEATURES

- **High OFF Isolation .... 66 dB @ 10 MHz**
- **Wide Bandwidth Switches .... 0.9 × DC @ 100 MHz**
- **Low Channel-to-Channel Cross Talk .... –80 dB @ 10 MHz**
- **TTL Compatible**
- **Low OFF Leakage**
- **Industry-Standard Pinouts**

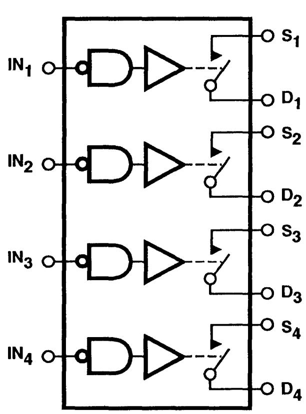
APPLICATIONS

- **Switches**
  - **— Glitch-Free Analog**
  - **— RF and Video**
  - **— Track-and-Hold**
  - **— Sample-and-Hold**

GENERAL DESCRIPTION

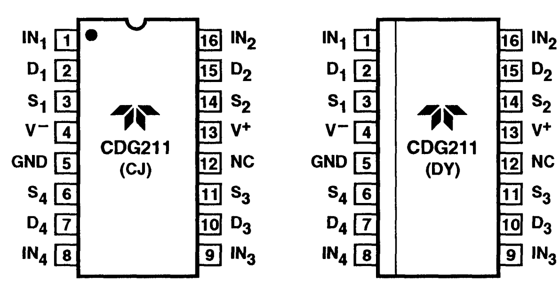
Teledyne Components' CDG211 low-cost analog switch features TTL-compatible input logic and wideband lateral DMOS switches on a single chip. The on-chip reference used for TTL compatibility gives the added advantage of constant logic switching over a wide range of supply voltages and temperature without a separate power supply. Industry-standard pinout makes the CDG211 particularly suitable for replacement of existing analog switches and upgrading high frequency performance at the same time.

FUNCTIONAL BLOCK DIAGRAM



NOTES: 1. Four SPST switches per package.
2. Switches shown in logic "1" (OFF) position.
3. ON = Logic "0" ≤ 0.8V
OFF = Logic "1" ≤ 2.4V

PIN CONFIGURATIONS



(TOP VIEW) (TOP VIEW)

NC = NO INTERNAL CONNECTION

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CDG211

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
CDG211CJ	16-Pin Plastic DIP	0°C to +70°C
CDG201DY	16-Pin SO	−40°C to +85°C

RECOMMENDED OPERATING CONDITIONS

V^- Negative Supply Voltage .... −8V to −15V
V^+ Positive Supply Voltage .... +8V to +15V
V_{IN} Control Input Voltage Range .... 0V to +5V
V_S Analog Switch Voltage Range .... ±10V
T_{OP} Operating Temperature Range
C Suffix .... 0°C to +70°C
D Suffix .... −40°C to +85°C

NOTE: All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (V_{DD} or GND).

ABSOLUTE MAXIMUM RATINGS

V^- Negative Supply Voltage .... −20V
V^+ Positive Supply Voltage .... +20V
V_{IN} Control Input Voltage
Range .... V^+ +0.3V, V^- −0.3V
I_L Continuous Current, Any Pin Except S or D ... 30 mA
I_S Continuous Current, S or D .... 30 mA
I_S Peak Pulsed Current, S or D,
80 µs, 1%, Duty Cycle .... 90 mA
T_{STG} Storage Temperature Range .... −55°C to +125°C
PD Power Dissipation .... 500 mW

ELECTRICAL CHARACTERISTICS: T_A = +25°C, V^- = −15V, V^+ = +15V per channel, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static						
V_{ANALOG}	Analog Signal Range		−10	—	+10	V
$r_{DS(ON)}$	Switch ON Resistance	V_S = −10V, V_{IN} = 0	—	40	80	Ω
		V_S = +2V, V_{IN} = 0	—	45	80	Ω
		V_S = +10V, V_{IN} = 0	—	100	160	Ω
V_{IH}	High Level Input Voltage		2.4	—	—	V
V_{IL}	Low Level Input Voltage		—	—	0.8	V
I_{IN}	Logic Input Leakage Current	V_{IN} = +2.4V	—	0.01	0.1	µA
		V_{IN} = +15V	—	0.02	0.1	µA
$I_{D(OFF)}$	Switch OFF Leakage Current	V_D = +10V, V_S = −10V, V_{IN} = +2.4V	—	0.2	5	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_S = +10V, V_D = −10V, V_{IN} = +2.4V	—	0.4	5	nA
I^-	Negative Supply Quiescent Current	V_{IN} = 0 or +2.4V	—	−0.3	−1	mA
I^+	Positive Supply Quiescent Current	V_{IN} = 0 or +2.4V	—	0.6	2	mA
Dynamic						
t_{ON}	Switch Turn-On Time	See Switching Times Test Circuit	—	400	600	ns
t_{OFF}	Switch Turn-Off Time	See Switching Times Test Circuit	—	70	300	ns
OIRR	OFF Isolation Rejection Ratio	f = 10 MHz, R_L = 50Ω	60	66	—	dB
CCRR	Cross-Coupling Rejection Ratio	f = 10 MHz, R_L = 50Ω	—	80	—	dB
C_D	Drain-Node Capacitance	V_D = V_S = 0, f = 1 MHz, V_{IN} = +2.4V	—	0.3	—	pF
C_S	Source-Node Capacitance	V_D = V_S = 0, f = 1 MHz, V_{IN} = +2.4V	—	3	—	pF

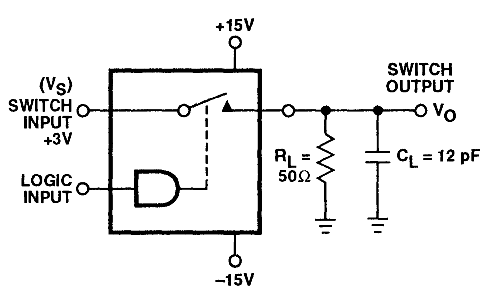
QUAD MONOLITHIC, SPST CMOS/DMOS ANALOG SWITCH

CDG211

ELECTRICAL CHARACTERISTICS: $V^- = -15V$, $V^+ = +15V$ per channel, unless otherwise noted.
Limits at Temperature Extremes

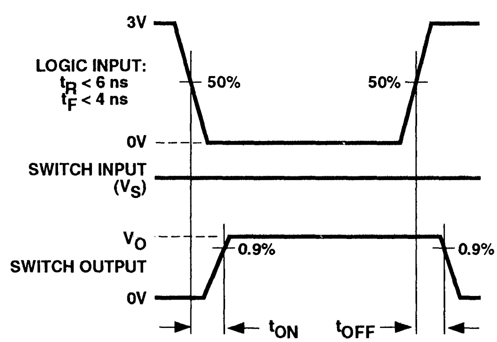
Symbol	Parameter	Test Conditions	Maximum @ T_A = –40°C	0°C	+70°C	+85°C	Unit
Static							
V_{ANALOG}	Analog Signal Range		±10	±10	±10	±10	V
$r_{DS(ON)}$	Switch ON Resistance	$V_S = -10V$, $V_{IN} = 0$, $V_S = +2V$	80	80	120	120	Ω
		$V_S = +10V$, $V_{IN} = 0$	160	160	240	240	Ω
I_{IN}	Logic Input Leakage Current	$V_{IN} = +2.4V$, $V_{IN} = +15V$	0.1	0.1	1	1	µA
$I_{D(OFF)}$	Switch OFF Leakage Current	$V_D = +10V$, $V_S = -10V$, $V_{IN} = +2.4V$	5	5	100	100	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	$V_S = +10V$, $V_D = -10V$, $V_{IN} = +2.4V$	5	5	100	100	nA
I^-	Negative Supply Quiescent Current	$V_{IN} = 0$ or $+2.4V$	–1	–1	–1	–1	mA
I^+	Positive Supply Quiescent Current	$V_{IN} = 0$ or $+2.4V$	2	2	2	2	mA

SWITCHING TIMES TEST CIRCUIT



NOTE: Switch shown in logic "1" (OFF) position.

TEST WAVEFORMS



$$V_{OUT} = \frac{R_L}{R_L + r_{DS(ON)}}$$

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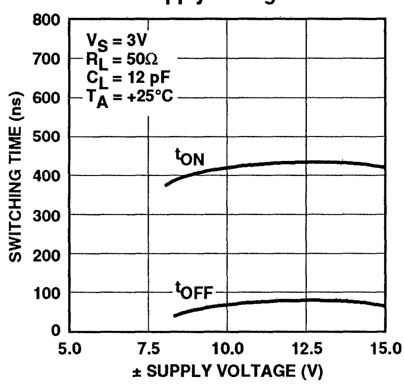
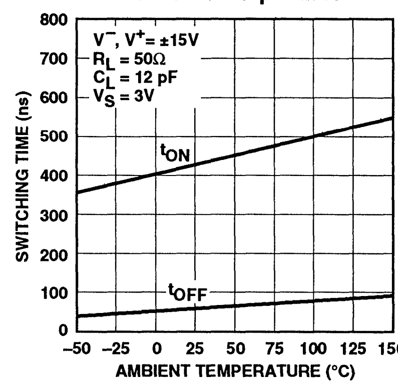
TYPICAL PERFORMANCE CHARACTERISTICS

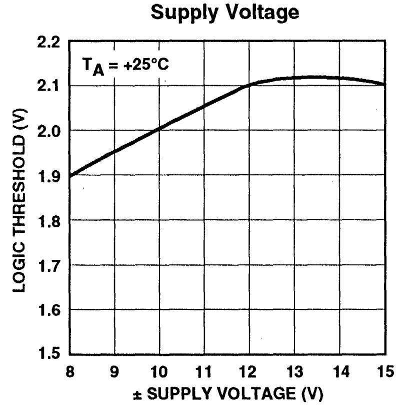
Switching Time vs Supply Voltage



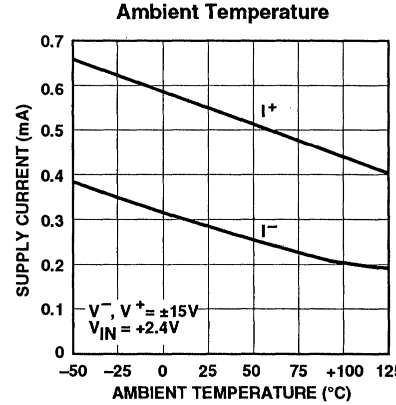
Switching Time vs Ambient Temperature



Logic Threshold vs Supply Voltage

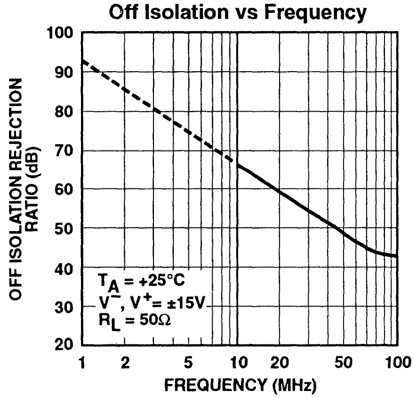


Supply Current vs Ambient Temperature

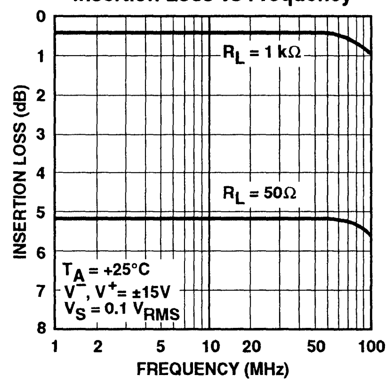


TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

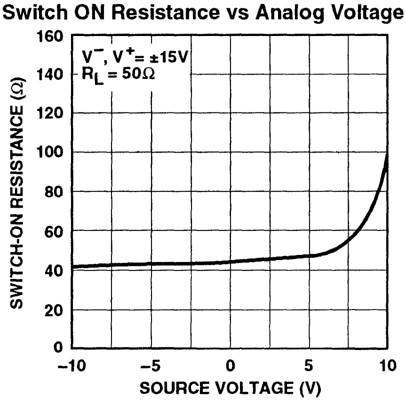
Off Isolation vs Frequency



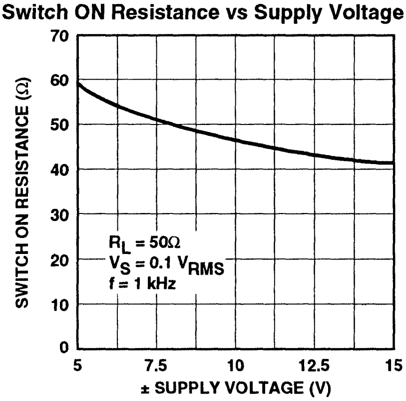
Insertion Loss vs Frequency



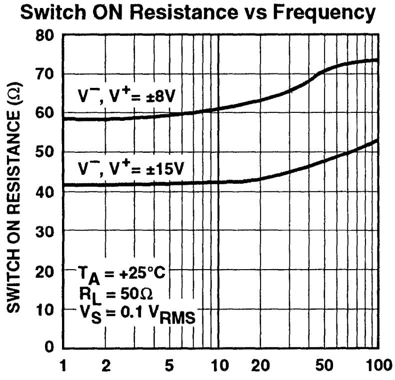
Switch ON Resistance vs Analog Voltage



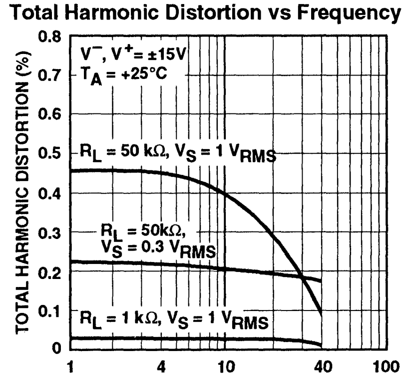
Switch ON Resistance vs Supply Voltage



Switch ON Resistance vs Frequency



Total Harmonic Distortion vs Frequency



NOTES

HIGH-SPEED ANALOG SWITCH

FEATURES

- **Ultra-High OFF Isolation .... >40 dB @ 100 MHz**
  >25 dB @ 200 MHz
- **High-Speed Switching**
  — t_{ON} .... 40 ns
  — t_{OFF} .... 20 ns
- **CMOS-Compatible Inputs**
- **Low ON Resistance .... <50Ω**
- **Wide Bandwidth .... –3 dB @ 250 MHz**

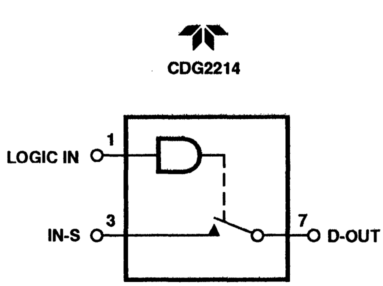
APPLICATIONS

- **RF and Video Switches**
- **High-Frequency Data Acquisition**
- **High-Frequency Multiplexers**

GENERAL DESCRIPTION

Teledyne Components' CMOS/DMOS analog switches feature high-speed, low-power CMOS input logic and level translation circuitry, and high-speed, low-capacitance, lateral DMOS switches. CMOS and lateral DMOS circuitry are fabricated together on a single silicon chip.

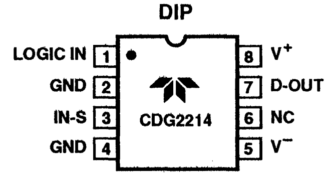
FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. One SPST switch per package.
2. Switch shown in logic "1" position.
3. Logic "0" ≤1V; Logic "1" ≥4.5V
4. Logic "0" = ON; Logic "1" = OFF

PIN CONFIGURATIONS

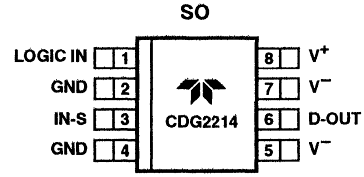
DIP



(TOP VIEW)

NC = NO INTERNAL CONNECTION

SO



(TOP VIEW)

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CDG2214

ABSOLUTE MAXIMUM RATINGS

Negative Supply Voltage .... −20V
Positive Supply Voltage .... +20V
Control Input Voltage Range .... V^+ +0.3V, V^- −0.3V
Continuous Current, Any Pin
Except S or D .... 20 mA
Continuous Current, S or D .... 40 mA
Peak Pulsed Current, S or D,
80 µs, 1%, Duty Cycle .... 100 mA
Junction Temperature Range .... −55°C to +125°C
Storage Temperature Range .... −65°C to +125°C
Power Dissipation .... 500 mW
(Derate at 12 mW/°C, Above +85°C)

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Negative Supply Voltage .... −5V to −15V
Positive Supply Voltage .... +5V to +15V
Control Input Voltage Range .... 0V to +5V
Operating Temperature Range
C Suffix .... 0°c to +70°C
E Suffix .... −40°C to +85°C
M Suffix .... −55°C to +125°C

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
CDG2214CPA	8-Pin Plastic DIP	0°C to +70°C
CDG2214EPA	8-Pin Plastic DIP	−40°C to +85°C
CDG2214MJA	8-Pin CerDIP	−55°C to +125°C
CDG2214COA	8-Pin Plastic SO	0°c to +70°C
CDG2214EOA	8-Pin Plastic SO	−40°C to +85°C

ELECTRICAL CHARACTERISTICS: T_A = +25°C, V^- = −15V, V^+ = +15V per channel, unless otherwise noted.

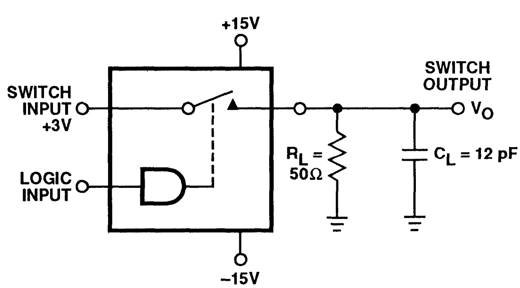
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static						
V_{ANALOG}	Analog Signal Range		−10	—	+10	V
$r_{DS(ON)}$	Switch ON Resistance	V_S = −10V	—	45	80	Ω
		V_S = +2V	—	50	80	Ω
		V_S = +10V	—	130	160	Ω
V_{IH}	High Level Input Voltage		4.5	3.4	—	V
V_{IL}	Low Level Input Voltage		—	—	1	V
I_{IN}	Logic Input Leakage Current	V_{IN} = +5V	—	0.01	0.1	µA
		V_{IN} = +15V	—	0.02	0.1	µA
$I_{D(OFF)}$	Switch OFF Leakage Current	V_D = +10V, V_S = −10V, V_{IN} = +5V	—	0.2	5	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_S = +10V, V_D = −10V, V_{IN} = +5V	—	0.2	5	nA
I^-	Negative Supply Quiescent Current	V_{IN} = 0 or V^+	—	—	−8	mA
I^+	Positive Supply Quiescent Current	V_{IN} = 0 or V^+	—	—	8	mA
Dynamic						
t_{ON}	Switch Turn-On Time	V_{IN} = 5V, R_L = 50Ω, C_L = 12 pF	—	40	60	ns
t_{OFF}	Switch Turn-Off Time	V_{IN} = 5V, R_L = 50Ω, C_L = 12 pF	—	20	40	ns
OIRR	Off Isolation Rejection Ratio	f = 100 MHz, R_L = 50Ω	37	40	—	dB
		f = 200 MHz, R_L = 50Ω	22	25	—	dB
I_L	Insertion Loss	f = 200 MHz, R_L = 50Ω	—	7.8	13	dB
C_D	Drain-Node Capacitance	V_D = 0, f = 1 MHz, V_{IN} = 0V	—	0.3	—	pF
C_S	Source-Node Capacitance	V_S = 0, f = 1 MHz, V_{IN} = 0V	—	3	—	pF

ELECTRICAL CHARACTERISTICS: $V^- = -15V$, $V^+ = +15V$ per channel, unless otherwise noted.

Limits at Temperature Extremes

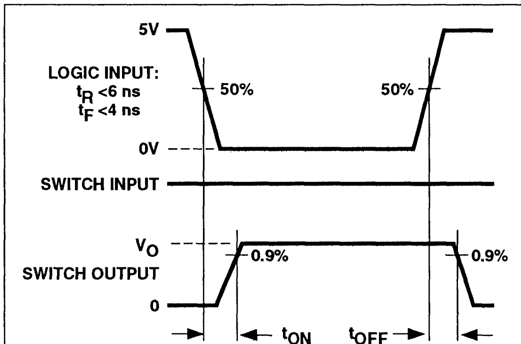
Symbol	Parameter	Test Conditions	Maximum @ T_A = −55°C	−40°C	+85°C	+125°C	Unit
Static							
V_{ANALOG}	Analog Signal Range		±10	±10	±10	±10	V
$r_{DS(ON)}$	Switch ON Resistance	$V_S = +2V$	80	80	120	150	Ω
		$V_S = -10V$	80	80	120	150	Ω
		$V_S = +10V$	160	160	240	300	Ω
I_{IN}	Logic Input Leakage Current	$V_{IN} = +5V$	0.1	0.1	1	10	μA
		$V_{IN} = +15V$	0.1	0.1	2	20	μA
$I_{D(OFF)}$	Switch OFF Leakage Current	$V_D = +10V$, $V_S = -10V$, $V_{IN} = +5V$	5	5	200	1000	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	$V_S = +10V$, $V_D = -10V$, $V_{IN} = +5V$	5	5	200	1000	nA
I^-	Negative Supply Quiescent Current	$V_{IN} = 0$ or V^+	−8	−8	−10	−10	mA
I^+	Positive Supply Quiescent Current	$V_{IN} = 0$ or V^+	8	8	10	10	mA

SWITCHING TIMES TEST CIRCUIT

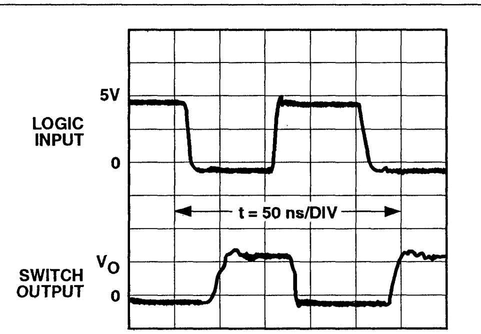


NOTE: Switch shown in logic "1" (OFF) position.

TEST WAVEFORMS



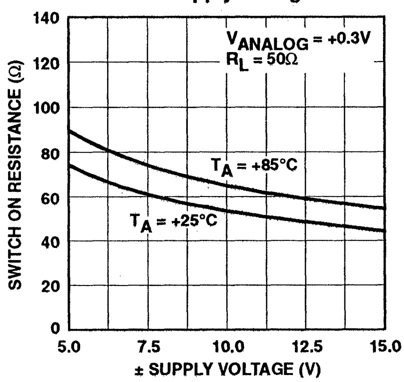
TEST RESULTS



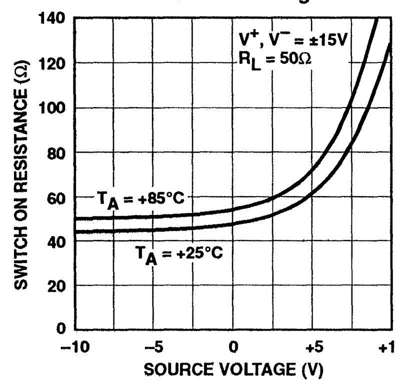
CDG2214

TYPICAL PERFORMANCE CHARACTERISTICS

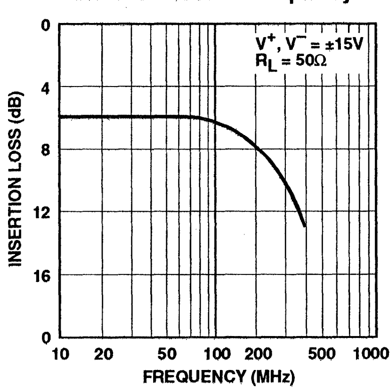
Switch ON Resistance vs Supply Voltage



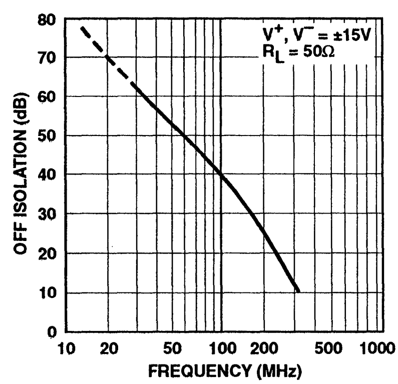
Switch ON Resistance vs Source Voltage



Insertion Loss vs Frequency



Off Isolation vs Frequency



TELEDYNE
COMPONENTS

DUAL SPDT CMOS/DMOS ANALOG SWITCH WITH DATA LATCH

FEATURES

- **High OFF Isolation**
- **Low Channel-to-Channel Cross Talk**
- **Wide Bandwidth**
- **Analog Signal Range .... +10V to –10V**
- **Low ON Resistance .... 20W Typ**

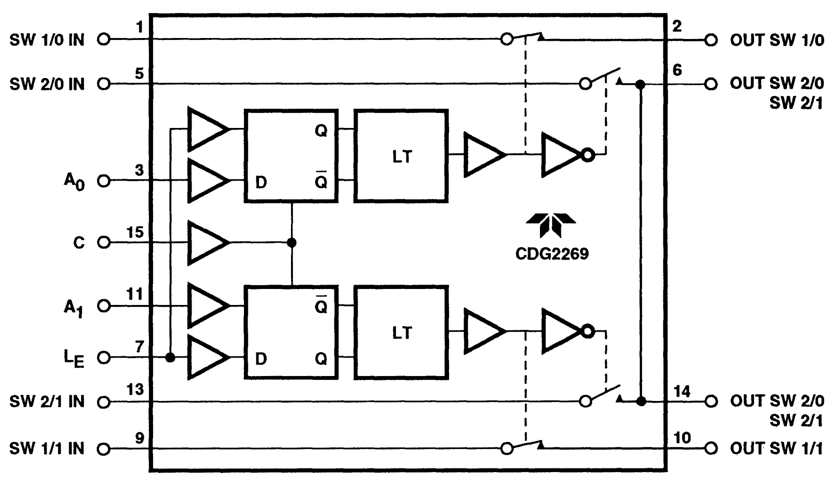
APPLICATIONS

- **RF and Video Switches**
- **High-Speed Precision Data Acquisition**
- **L-PAD Digital-Controlled Attenuators**

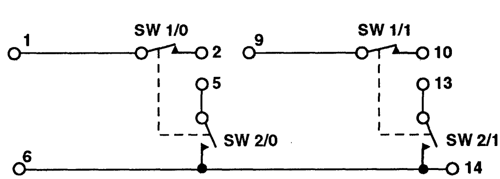
GENERAL DESCRIPTION

Teledyne Components' CMOS/DMOS analog switches feature high-speed, low-power CMOS input logic and level translation circuitry, and high-speed, low-capacitance, lateral DMOS switches. CMOS and lateral DMOS circuitry are fabricated together on a single silicon chip. This device is designed for applications where high OFF isolation at high frequencies is needed.

LOGIC DIAGRAM



NOTE: Switches shown in logic "0" position.



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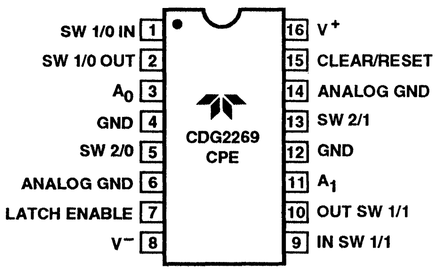
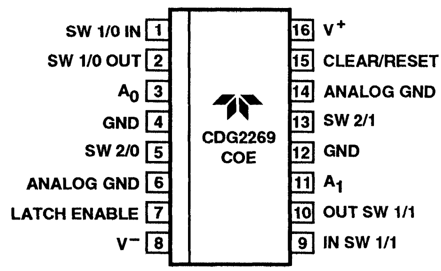
DUAL SPDT CMOS/DMOS ANALOG SWITCH WITH DATA LATCH

CDG2269

PIN CONFIGURATIONS



(TOP VIEW)



(TOP VIEW)

FUNCTION TABLE

Input			Switch	
A	L_E	C	SW_1	SW_2
L	H	L	ON	OFF
H	H	L	OFF	ON
X	X	H	OFF	ON
L	L	L	Note 1	Note 2

NOTES: 1. Hold input state one setup before L_E high-to-low transition. If input state is low, then switch ON. If input state is high, then switch OFF.
2. $SW_1 = \overline{SW_2}$.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
CDG2269CPE	16-Pin Plastic DIP	0°C to +70°C
CDG2269COE	16-Pin SO	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Negative Supply Voltage .... −20V
Positive Supply Voltage .... +20V
Control Input Voltage
Range .... V^+ +0.3V, V^- −0.3V
Continuous Current, Any Pin Except S or D .... 20 mA
Continuous Current, S or D .... 30 mA
Peak Pulsed Current, S or D,
80 µs, 1%, Duty Cycle .... 100 mA
Junction Temperature Range .... −55°C to +125°C
Storage Temperature Range .... −65°C to +150°C
Power Dissipation .... 500 mW

NOTE: All devices contain diodes to protect inputs against damage due to high-static voltages or electric fields. However, it is advised precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (V_{DD} or GND). Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

DUAL SPDT CMOS/DMOS ANALOG SWITCH WITH DATA LATCH

CDG2269

RECOMMENDED OPERATING CONDITIONS

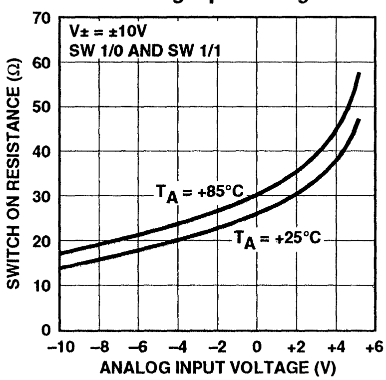
Negative Supply Voltage .... –8V to –15V
Positive Supply Voltage .... +8V to +15V
Control Input Voltage Range .... 0V to +5V
Operating Temperature Range .... 0°C to +70°C

ELECTRICAL CHARACTERISTICS: T_A = +25°C, V^- = –15V, V^+ = +15V per channel, unless otherwise noted.

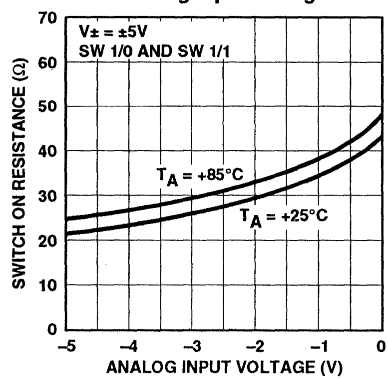
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static						
V_{ANALOG}	Analog Signal Range		–10	—	+10	V
$r_{DS(ON)}$	Switch ON Resistance	V_S = –10V, I_S = –1 mA	—	29	80	Ω
	(Switches 2/0 and 2/1)	V_S = +2V, I_S = 1 mA	—	40	80	Ω
		V_S = +10V, I_S = –1 mA	—	100	160	Ω
$r_{DS(ON)}$	Switch ON Resistance	V_S = –10V, I_S = –1 mA	—	13	40	Ω
	(Switches 1/0 and 1/1)	V_S = +2V, I_S = 1 mA	—	20	40	Ω
		V_S = +10V, I_S = –1 mA	—	50	80	Ω
V_{IH}	Logic "1" High Input Voltage		4.5	3.4	—	V
V_{IL}	Logic "0" Low Input Voltage		—	—	1	V
I_{IN}	Logic Input Leakage Current	V_{IN} = +5V	—	0.01	0.1	μA
		V_{IN} = +15V	—	0.02	0.1	μA
$I_{D(OFF)}$	Switch OFF Leakage Current (Switches 2/0 and 2/1)	V_D = +10V, V_S = –10V	—	0.4	5	nA
$I_{S(OFF)}$	Switch OFF Leakage Current (Switches 2/0 and 2/1)	V_S = +10V, V_D = –10V	—	4	20	nA
$I_{D(OFF)}$	Switch OFF Leakage Current (Switches 1/0 and 1/1)	V_D = +10V, V_S = –10V	—	0.4	5	nA
$I_{S(OFF)}$	Switch OFF Leakage Current (Switches 1/0 and 1/1)	V_S = +10V, V_D = –10V	—	4	20	nA
I^-	Negative Supply Quiescent Current	V_{IN} = 0V or V^+	—	–0.05	–0.5	μA
I^+	Positive Supply Quiescent Current	V_{IN} = 0V or V^+	—	0.03	0.5	μA
Dynamic						
t_D	Propagation Delay					
	Data to Switch ON		—	180	250	ns
	Data to Switch OFF		—	100	200	ns
	Latch Enable to Switch ON		—	180	250	ns
	Latch Enable to Switch OFF		—	140	200	ns
	Clear to Switch ON		—	180	250	ns
	Clear to Switch OFF		—	90	150	ns
t_S	Setup Time		150	120	—	ns
t_H	Hold Time		150	90	—	ns
t_W	Pulse Width		50	40	—	ns
OIRR	Off Isolation Rejection Ratio	f = 10 MHz, R_L = 50Ω	42	45	—	dB
	(Switches 1/0 and 1/1)	f = 200 MHz, R_L = 50Ω	12	15	—	dB
	Frequency Roll-Off (Bandwidth)	f = 200 MHz, R_L = 50Ω	—	1	3	dB
C_D	Drain-Node Capacitance	V_D = 0V, f = 1 MHz, V_{IN} = 0V	—	0.6	—	pF
C_S	Source-Node Capacitance	V_S = 0V, f = 1 MHz, V_{IN} = 0V	—	6	—	pF

TYPICAL PERFORMANCE CHARACTERISTICS CURVES

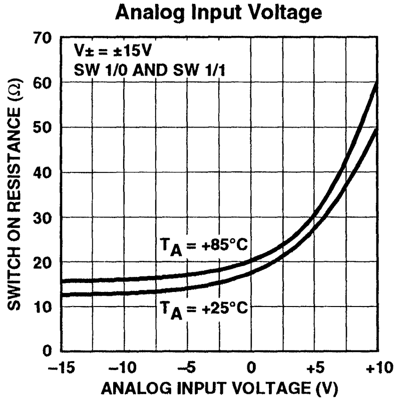
Switch ON Resistance vs Analog Input Voltage



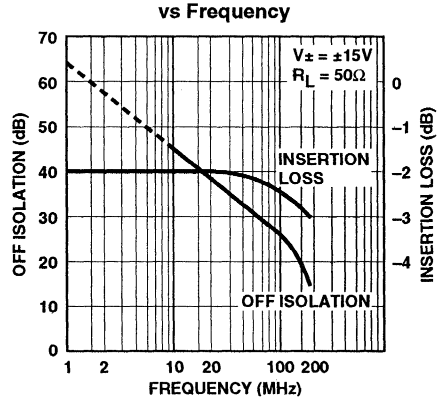
Switch ON Resistance vs Analog Input Voltage



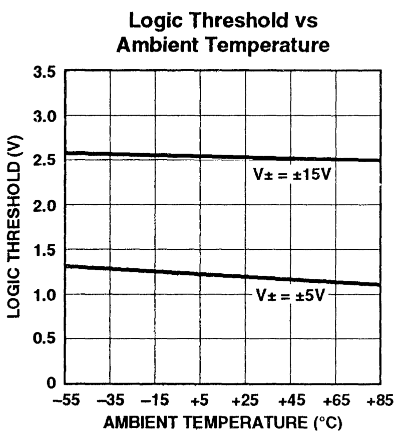
Switch ON Resistance vs Analog Input Voltage

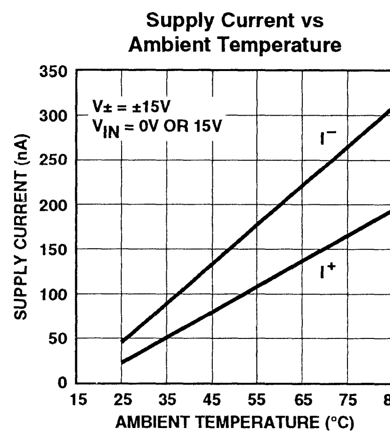


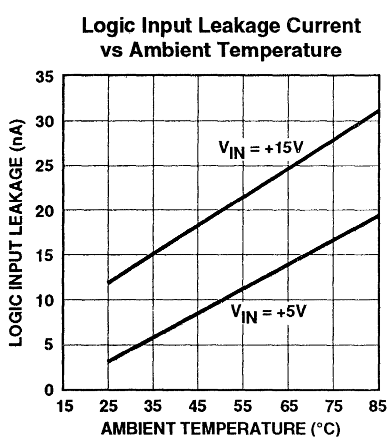
Off Isolation and Insertion Loss vs Frequency

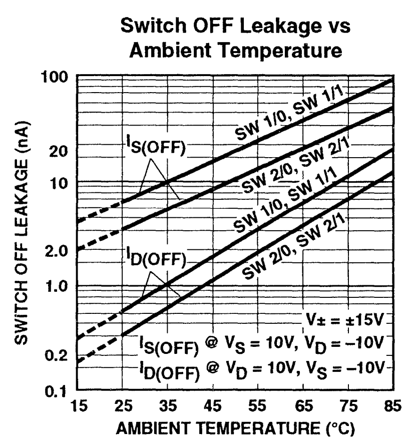


TYPICAL PERFORMANCE CHARACTERISTICS CURVES (Cont.)









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NOTES

TELEDYNE COMPONENTS

CDG308 CDG4308
CDG309 CDG4309

QUAD MONOLITHIC, SPST CMOS/DMOS ANALOG SWITCHES

FEATURES

- High OFF Isolation .... 68 dB @ 10 MHz
- Low Insertion Loss .... –1 dB @ 100 MHz
- Low Channel-to-Channel Cross Talk .... –80 dB @ 10 MHz
- CMOS-Compatible Inputs
- Low OFF Leakage
- Industry Standard Pinout (CDG308/CDG309)

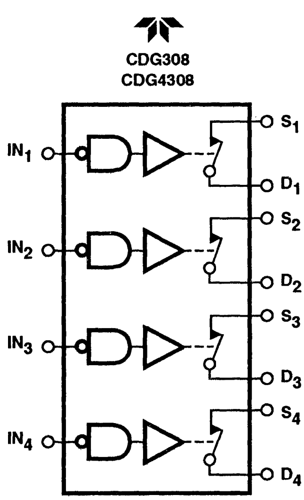
APPLICATIONS

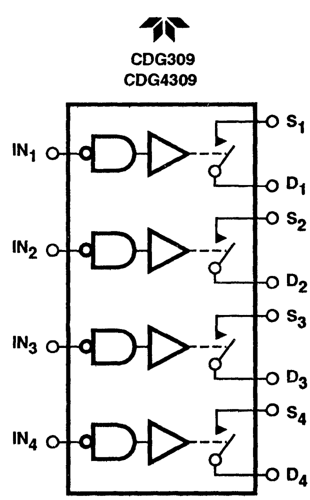
- Glitch-Free Analog Switching
- RF and Video
- Track-and-Hold
- Sample-and-Hold

GENERAL DESCRIPTION

Teledyne Components' CMOS/DMOS analog switches feature high-speed, low-power CMOS input logic and level translation circuitry, and high-speed, low-capacitance, lateral DMOS switches. CMOS and lateral DMOS circuitry are fabricated together on a single silicon chip. The CDG4308 and CDG4309 use the same die as CDG308 and CDG309; the extra isolating pin between switch input and output increases isolation by 6 dB.

FUNCTIONAL BLOCK DIAGRAMS





NOTES: 1. Four SPST switches per package.
2. Switches shown in logic "1" position.
3. CDG308/CDG4308: Logic "0" = OFF; Logic "1" = ON
CDG309/CDG4309: Logic "0" = ON; Logic "1" = OFF

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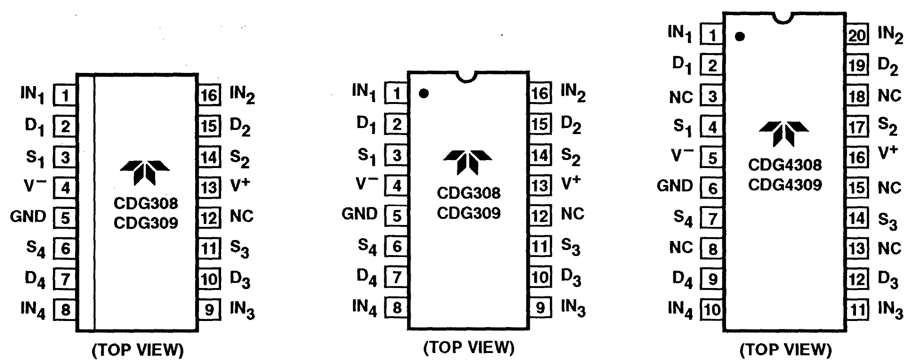
QUAD MONOLITHIC, SPST CMOS/DMOS ANALOG SWITCHES

CDG308 CDG4308 CDG309 CDG4309

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
CDG308COE	16-Pin SO	0°C to +70°C
CDG308CPE	16-Pin Plastic DIP	0°C to +70°C
CDG308EJE	16-Pin CerDIP	–40°C to +85°C
CDG308EOE	16-Pin SO	–40°C to +85°C
CDG308EPE	16-Pin Plastic DIP	–40°C to +85°C
CDG308MJE	16-Pin CerDIP	–55°C to +125°C
CDG309COE	16-Pin SO	0°C to +70°C
CDG309CPE	16-Pin Plastic DIP	0°C to +70°C
CDG309EJE	16-Pin CerDIP	–40°C to +85°C
CDG309EOE	16-Pin SO	–40°C to +85°C
CDG309EPE	16-Pin Plastic DIP	–40°C to +85°C
CDG309MJE	16-Pin CerDIP	–55°C to +125°C
CDG4308CPP	20-Pin Plastic DIP	0°C to +70°C
CDG4308EPP	20-Pin Plastic DIP	–40°C to +85°C
CDG4309CPP	20-Pin Plastic DIP	0°C to +70°C
CDG4309EPP	20-Pin Plastic DIP	–40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Negative Supply Voltage .... –20V
Positive Supply Voltage .... +20V
Control Input Voltage Range .... V^+ +0.3V, V^- –0.3V
Continuous Current, Any Pin Except S or D .... 20 mA
Continuous Current, S or D .... 30 mA
Peak Pulsed Current, S or D,
80 µs, 1%, Duty Cycle .... 180 mA
Junction Temperature Range ....–55°C to +125°C
Storage Temperature Range ....–65°C to +150°C
Power Dissipation .... 500 mW

NOTE: All devices contain diodes to protect inputs against damage due to high-static voltages or electric fields. However, it is advised precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (V_{DD} or GND). Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

QUAD MONOLITHIC, SPST CMOS/DMOS ANALOG SWITCHES

CDG308 CDG4308 CDG309 CDG4309

RECOMMENDED OPERATING CONDITIONS

Negative Supply Voltage .... –8V to –15V
Positive Supply Voltage .... +8V to +15V
Control Input Voltage Range .... 0V to +5V
Analog Switch Voltage Range .... ±10V
Operating Temperature Range
  C Suffix .... 0°C to +70°C
  E Suffix .... –40°C to +85°C
  M Suffix .... –55°C to +125°C

ELECTRICAL CHARACTERISTICS: T_A = +25°C, V^- = –15V, V^+ = +15V per channel, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static						
V_{ANALOG}	Analog Signal Range		–10	—	+10	V
$r_{DS(ON)}$	Switch ON Resistance	V_S = –10V	—	40	80	Ω
		V_S = +2V	—	45	80	Ω
		V_S = +10V	—	100	160	Ω
V_{IH}	High Level Input Voltage		4.5	3.4	—	V
V_{IL}	Low Level Input Voltage		—	—	1	V
I_{IN}	Logic Input Leakage Current	V_{IN} = +5V	—	0.01	0.1	µA
		V_{IN} = +15V	—	0.02	0.1	µA
$I_{D(OFF)}$	Switch OFF Leakage Current	V_D = +10V, V_S = –10V V_{IN} = +5V (CDG309/CDG4309) V_{IN} = +1V (CDG308/CDG4308)	—	0.2	5	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_S = +10V, V_D = –10V V_{IN} = +5V (CDG309/CDG4309) V_{IN} = +1V (CDG308/CDG4308)	—	0.4	5	nA
I^-	Negative Supply Quiescent Current	V_{IN} = +5V (CDG309/CDG4309) V_{IN} = +1V (CDG308/CDG4308)	—	–0.1	–0.5	µA
I^+	Positive Supply Quiescent Current	V_{IN} = +5V (CDG309/CDG4309) V_{IN} = +1V (CDG308/CDG4308)	—	0.1	0.5	µA
Dynamic						
t_{ON}	Switch Turn-On Time	V_{IN} = +1V (CDG308/CDG4308) V_{IN} = +5V (CDG309/CDG4309)	—	140	250	ns
t_{OFF}	Switch Turn-Off Time	V_{IN} = +1V (CDG308/CDG4308) V_{IN} = +5V (CDG309/CDG4309)	—	80	220	ns
OIRR	Off Isolation Rejection Ratio	f = 10 MHz, R_L = 50Ω (CDG308/CDG309)	60	62	—	dB
		f = 10 MHz, R_L = 50Ω (CDG4308/CDG4309)	66	68	—	dB
C_{CRR}	Cross-Coupling Rejection Ratio	f = 10 MHz, R_L = 50Ω	—	80	—	dB
C_D	Drain-Node Capacitance	V_D = V_S = 0, f = 1 MHz V_{IN} = +1V (CDG308/CDG4308) V_{IN} = +5V (CDG309/CDG4309)	—	0.3	—	pF
C_S	Source-Node Capacitance	V_D = V_S = 0, f = 1 MHz V_S = 0, f = 1 MHz, V_{IN} = 0V V_{IN} = +5V (CDG309/CDG4309)	—	3	—	pF

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ELECTRICAL CHARACTERISTICS: $V^- = -15V$, $V^+ = +15V$ per channel, unless otherwise noted.

Limits at Temperature Extremes

Symbol	Parameter	Test Conditions	Maximum @ T_A =					Unit
			–55°C	–40°C	+70°C	+85°C	+125°C	
Static								
V_{ANALOG}	Analog Signal Range		±10	±10	±10	±10	±10	V
$r_{DS(ON)}$	Switch ON Resistance	$V_S = +2V$, $V_S = -10V$	80	80	120	120	150	Ω
		$V_S = +10V$	160	160	240	240	300	Ω
I_{IN}	Logic Input Leakage Current	$V_{IN} = +5V$	0.1	0.1	1	1	10	µA
		$V_{IN} = +15V$	0.1	0.1	2	2	20	µA
$I_{D(OFF)}$	Switch OFF Leakage Current	$V_D = +10V$, $V_S = -10V$	5	5	100	100	1000	nA
$I_{(OFF)}$	Switch OFF Leakage Current	$V_S = +10V$, $V_D = -10V$	5	5	100	100	1000	nA
I^-	Negative Supply Quiescent Current		–0.5	–0.5	–20	–20	–100	µA
I^+	Positive Supply Quiescent Current		0.5	0.5	20	20	100	µA

SWITCH CONTACTS

Switches are bidirectional (analog input can be to source or drain). However, for optimum performance in video applications, connect input to source and output to drain. (See Figure 1.)

POWER SUPPLY DECOUPLING CIRCUIT

By inserting 1 kΩ resistors in series with V^+ and V^- power supply lines, and decoupling both pins at the device socket, it is possible to improve video switch power supply rejection ratios by 50 dB at frequencies of 20 MHz and higher. (See Figure 2.)

APPLICATIONS

Very Low Distortion Circuit for Low Frequency/Large Signal Applications

The circuit shown in Figure 3 provides very low distortion (<0.1%) and high off isolation (>90 dB) at signal levels equal to the supply voltage. The signal passes through a "T" switch configuration and at the same time modulates the power supply. This modulation maintains a constant ON resistance, $r_{DS(ON)}$, which in turn reduces distortion. R5 is for bypassing the power supply and has a typical value of 1 kΩ; R4 should be a value that can be accommodated by the signal source as load; R3 is only necessary at loads lower

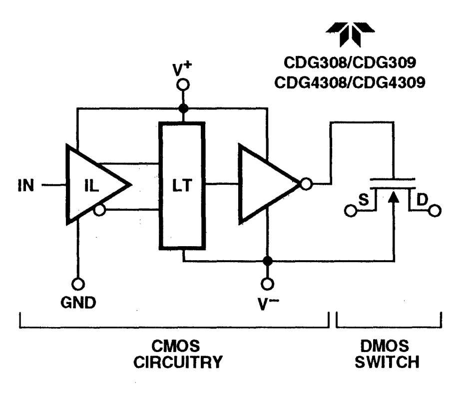

Figure 1 Functional Diagram (1 of 4 Channels)

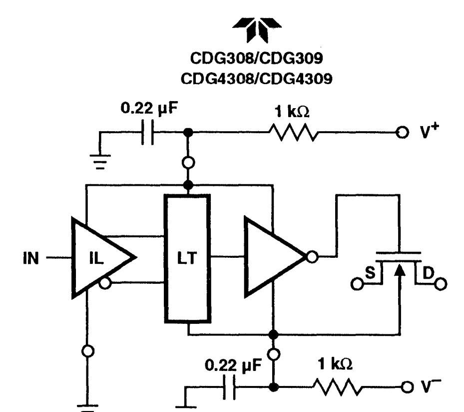

Figure 2 Power Supply Decoupling Circuit

than 100Ω and should be selected during initial circuit design; C1 has to be large enough for the lowest signal to pass and C2 will have to bypass all signals. R1 and R2 set up the logic "1" level for the control input and should be set to 5V.

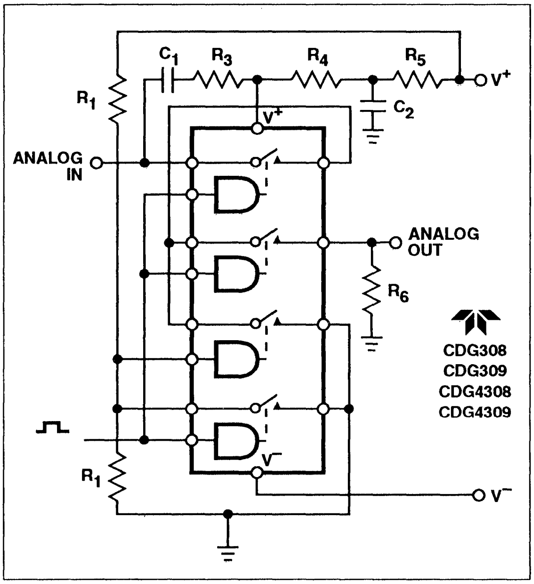

Figure 3 Low Distortion, Rail-to-Rail Analog Switch

Logic Inverter

The circuit shown in Figure 4 provides logic inversion with two resistors and one switch. It does not require additional logic parts. The resistors divide the supply voltage to a 5V level when high, and are switched to a low level via the switch. This configuration allows a single-pole, single-throw switch to be changed into a single-pole, double-throw switch.

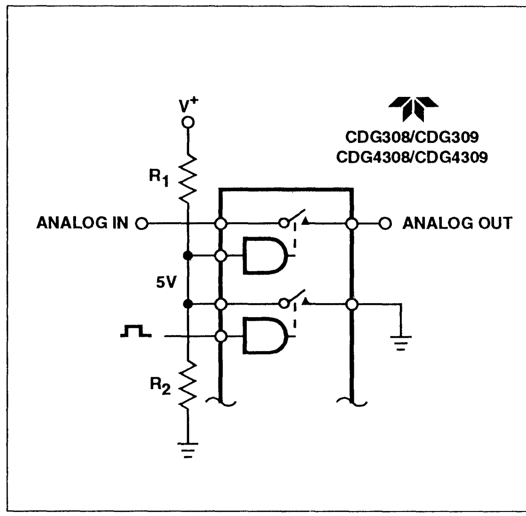

Figure 4 Logic Inverter

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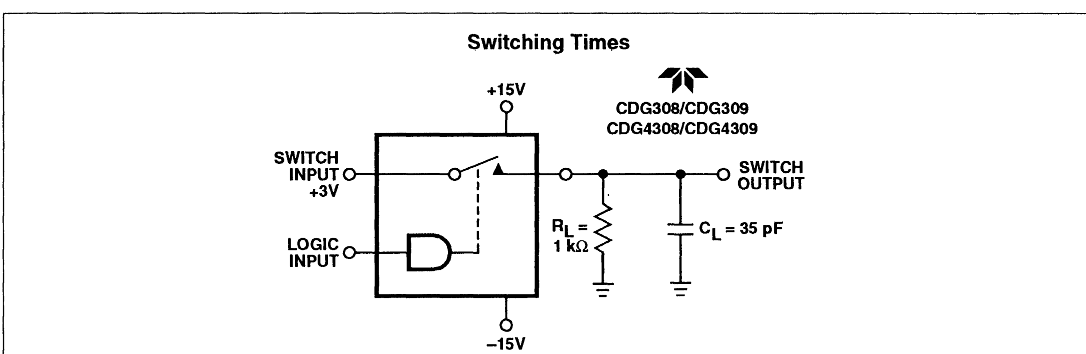
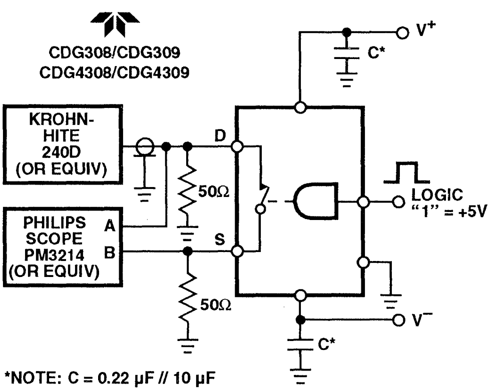
TEST CIRCUITS



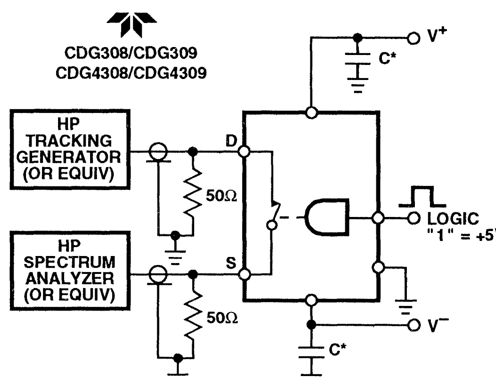
TEST CIRCUITS (Cont.)

Off Isolation



*NOTE: C = 0.22 µF // 10 µF

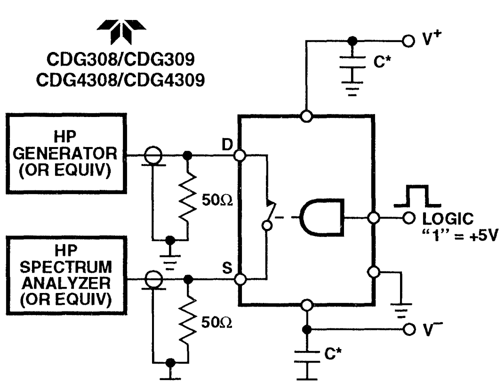
Switch ON Resistance vs Frequency



ON RESISTANCE
20 MHz TO 100 MHz

*NOTE: C = 0.22 µF // 10 µF

Distortion vs Frequency

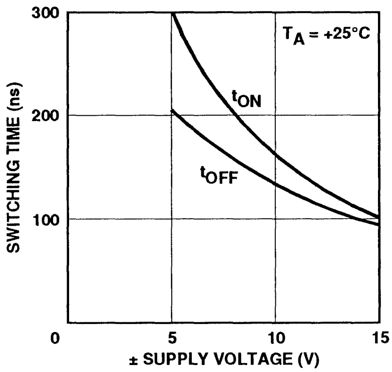


HARMONIC DISTORTION
10 MHz TO 40 MHz

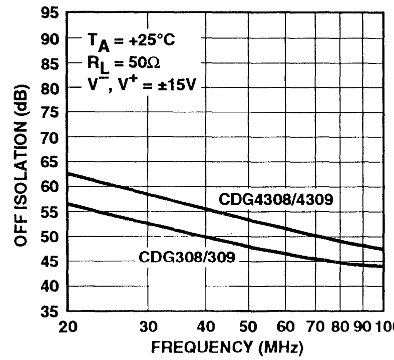
*NOTE: C = 0.22 µF // 10 µF

TYPICAL PERFORMANCE CHARACTERISTICS

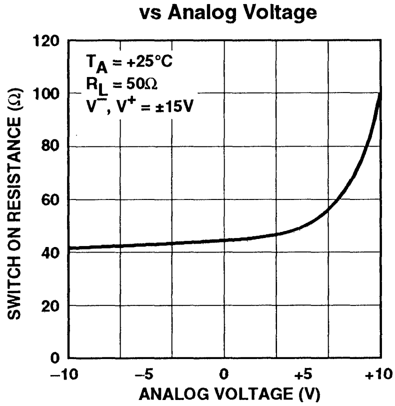
Switching Time vs Supply Voltage



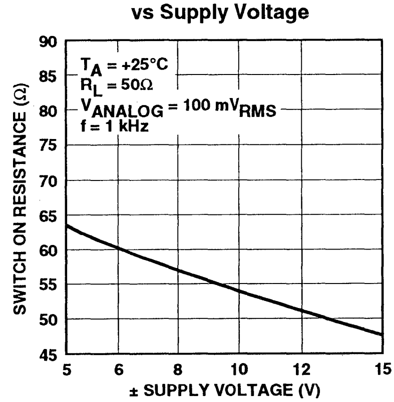
Off Isolation Rejection Ratio vs Frequency



Switch ON Resistance vs Analog Voltage



Switch ON Resistance vs Supply Voltage



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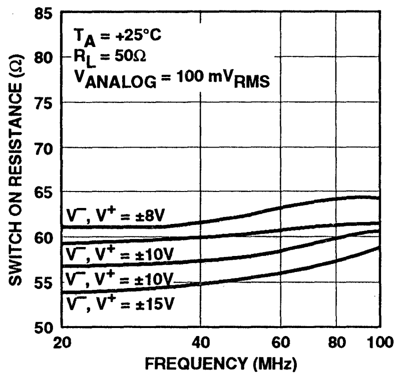
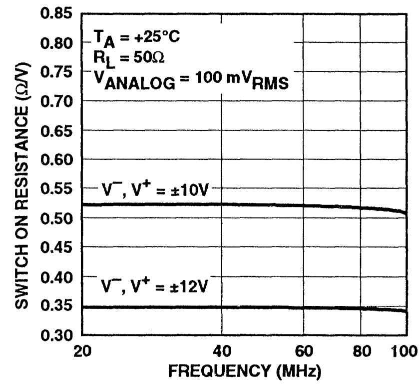
TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

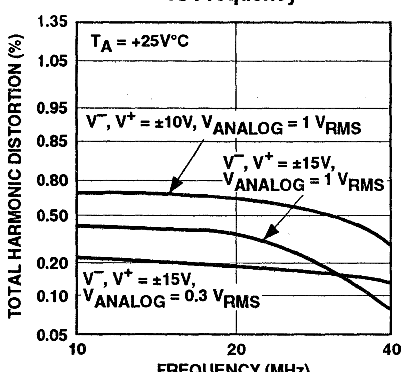
Switch ON Resistance vs Frequency



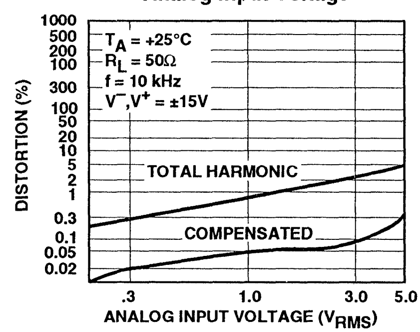
Switch ON Resistance vs Supply Voltage and Frequency



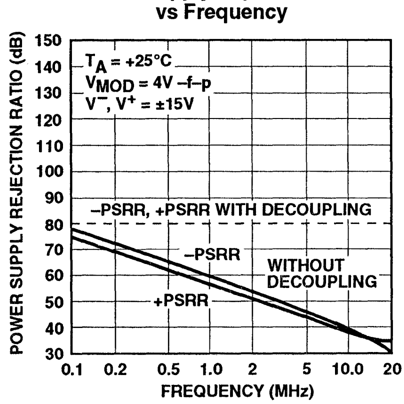
Total Harmonic Distortion vs Frequency



Distortion vs Analog Input Voltage



Power Supply Rejection Ratio vs Frequency



4-CHANNEL CMOS/DMOS HIGH-FREQUENCY MULTIPLEXER

FEATURES

- High OFF Isolation, >62dB @ 10 MHz
- Low Channel-to-Channel Crosstalk, >80dB @ 10 MHz
- 5 Volt CMOS Compatible Inputs
- Low ON Resistance, 40 Ω typ.
- Wide Bandwidth, –3.0dB @ 100 MHz
- Wide Analog Signal Range +10V to –10V
- High Speed Logic Control

APPLICATIONS

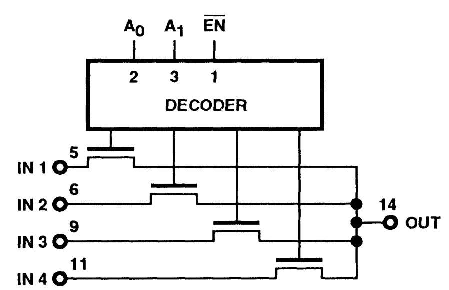
- RF & Video Switches
- High Speed Precision Data Acquisition

GENERAL DESCRIPTION

Teledyne CMOS/DMOS Analog Multiplexers feature high-speed, low-power 5 volt CMOS input logic and level translation circuitry and high speed, low capacitance Lateral DMOS switches. CMOS and Lateral DMOS circuitry are fabricated together on a single silicon chip. This part is designed for applications where high "off" isolation at high frequencies is needed. The 14 pin configuration gives a compact board layout without impacting "off" isolation and by use of the enable allows higher levels of multiplexing.

All devices contain diodes to protect inputs against damage due to high static voltages or electric fields; however, it is advised that precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic level (either V_{CC} or GND).

FUNCTION DIAGRAM



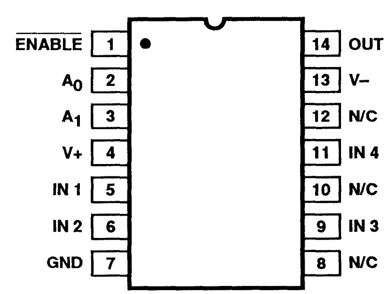
4346 ILL F01

FUNCTION TABLE

ENABLE	A_0	A_1	CHANNEL
H	X	X	OFF
L	L	L	S1
L	H	L	S2
L	L	H	S3
L	H	H	S4

X = Undefined

PIN CONFIGURATION



TOP VIEW

CDG4500AK
CDG4500BK
(See Package 14)

CDG4500BJ
CDG4500CJ
(See Package 9)

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CDG4500

ABSOLUTE MAXIMUM RATINGS

V–	Negative Supply Voltage	–20V
V+	Positive Supply Voltage	+20V
V_{IN}	Control Input Voltage Range	V+ +0.3V, V– –0.3V
I_L	Continuous Current, any Pin except S or D	20mA
I_S	Continuous Current, S or D	30mA
I_S	Peak Pulsed Current, S or D, 80µsec, 1% Duty Cycle	100mA
T_J	Junction Temperature Range	–55°C to +125°C
T_S	Storage Temperature Range	–55°C to +125°C
P_D	Power Dissipation (derate at 12mW/°C, above +85°C)	500mW

RECOMMENDED OPERATING CONDITIONS

V–	Negative Supply Voltage	–8.0 to –15V
V+	Positive Supply Voltage	+8.0 to +15V
V_{IN}	Control Input Voltage Range	0 to +5V
T_{OP}	Operating Temperature	
	(A Suffix)	–55 to +125°C
	(B Suffix)	–40 to +85°C
	(C Suffix)	0 to +70°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

4-Channel Multiplexer with Enable	14-Pin Plastic DIP	14-Pin Ceramic DIP
Commercial Temp. Range	CDG4500 CPD	—
Industrial Temp. Range	CDG4500 EPD	CDG4500 EJD
Military Temp. Range	—	CDG4500 MJD

4-CHANNEL CMOS/DMOS HIGH-FREQUENCY MULTIPLEXER

CDG4500

ELECTRICAL CHARACTERISTICS: (V- = –15V, V+ = +15V, per channel, unless otherwise noted, T_A = +25°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static						
V_{ANALOG}	Analog Signal Range		–10		+10	V
$r_{DS(on)}$	Channel On Resistance	V_S = –10V	—	40	80	Ω
		V_S = +2.0V	—	45	80	
		V_S = +10V	—	100	160	
V_{IH}	Logic High Level Input Voltage		4.5	3.4	—	V
V_{IL}	Logic Low Level Input Voltage		—	—	1.0	V
I_{IN}	Logic Input Leakage Current	V_{IN} = +5.0V	—	0.01	0.1	µA
		V_{IN} = +15V	—	0.02	0.1	
$I_{D(OFF)}$	Switch OFF Leakage Current	V_D = +10V, V_S = –10V	—	0.2	5.0	nA
$I_{S(OFF)}$		V_S = +10V, V_D = –10V	—	0.4	5.0	
I-	Negative Supply Queiescent Current	V_{IN} = 0 or V+	—	–1.4	–4.0	mA
I+	Positive Supply Quiescent Current	V_{IN} = 0 or V+	—	1.6	4.0	mA
Dynamic						
t_{ON}	Switch Turn-On Time (All inputs)	V_{IN} = 5.0V	—	150	250	nsec
t_{OFF}	Switch Turn-OFF Time (All inputs)	V_{IN} = 5.0V	—	120	220	nsec
C_{CRR}	All Crosstalk	f = 10 MHz, R_L = 50Ω	62	—	—	dB
	Single Channel Crosstalk	f = 10 MHz, R_L = 50Ω	80	—	—	
	Frequency Roll-Off (Bandwidth)	f = 100 MHz, R_L = 50Ω	—	1.0	3.0	
C_d	Output Node Capacitance	V_D = 0, f = 1 MHz, V_{IN} = 0	—	8.0	12.0	pF
C_s	Input Node Capacitance	V_S = 0, f = 1 MHz, V_{IN} = 0	—	2.5	4.0	pF

ELECTRICAL CHARACTERISTICS: (V– = –15V, V+ = +15V, per channel, unless otherwise noted)

LIMITS AT TEMPERATURE EXTREMES

Symbol	Parameter	Test Conditions	MAXIMUM @ T_A =					Units
			–55°C	–40°C	+70°C	+85°C	+125°C	
Static								
V_{ANALOG}	Analog Signal Range		±10	±10	±10	±10	±10	V
$r_{DS(on)}$	Channel On Resistance	V_S = –10V, I_S = –1.0 mA	80	80	120	120	150	Ω
		V_S = +2.0V, I_S = +1.0 mA	80	80	120	120	150	Ω
		V_S = +10V, I_S = –1.0 mA	160	160	240	240	300	Ω
I_{IN}	Logic Input	V_{IN} = +5.0V	0.1	0.1	1.0	1.0	10	µA
	Leakage Currents	V_{IN} = +15V	0.1	0.1	2.0	2.0	20	
$I_{D(OFF)}$	Switch OFF	V_D = +10V, V_S = –10V	5.0	5.0	100	100	1000	nA
$I_{S(OFF)}$	Leakage Currents	V_S = +10V, V_D = –10V	5.0	5.0	100	100	1000	
I–	Supply	V_{IN} = 0 or V+	–4.0	–4.0	–4.0	–4.0	–4.0	mA
I+	Quiescent Currents	V_{IN} = 0 or V+	4.0	4.0	4.0	4.0	4.0	mA

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NOTES

TELEDYNE COMPONENTS

DUAL MONOLITHIC, SPST CMOS/DMOS "T" CONFIGURATION ANALOG SWITCH

FEATURES

- Ultra-High OFF Isolation .... >80 dB @ 10 MHz
- Low Channel-to-Channel Cross Talk .... –80 dB @ 10 MHz
- CMOS-Compatible Inputs
- Low ON Resistance .... <110Ω
- Wide Bandwidth .... –1 dB @ 50 MHz

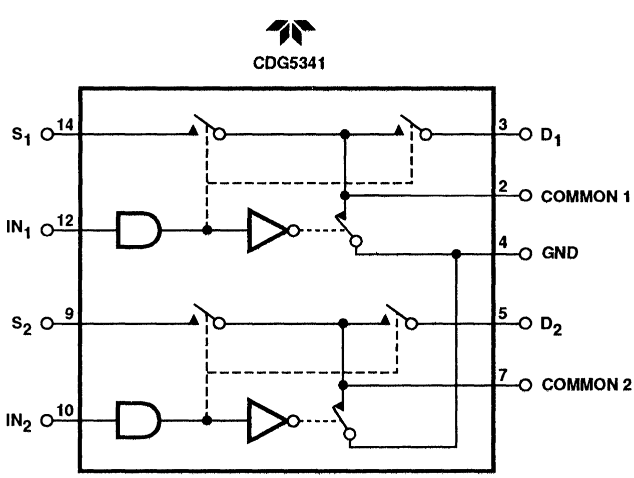
APPLICATIONS

- RF and Video Switches
- Data Acquisition

GENERAL DESCRIPTION

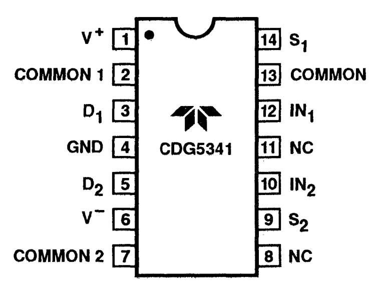
Teledyne Components' CMOS/DMOS analog switches feature high-speed, low-power 5V CMOS input logic and level translation circuitry, and high-speed, low-capacitance, lateral DMOS switches. CMOS and lateral DMOS circuitry are fabricated together on a single silicon chip.

FUNCTIONAL BLOCK DIAGRAM



NOTES: 1. Two SPST "T" switches per package.
2. Switchs shown in logic "0" position.
3. Compensation networks can be connected to COMMON 1 and COMMON 2.
4. Switches are "BREAK–before–MAKE"
5. Logic "0" = OFF; Logic "1" = ON

PIN CONFIGURATION



(TOP VIEW)

NC = NO INTERNAL CONNECTION

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DUAL MONOLITHIC, SPST CMOS/DMOS "T" CONFIGURATION ANALOG SWITCH

CDG5341

ORDERING INFORMATION

Part No.	Operating Package	Temperature Range
CDG5341EPE	14-Pin Plastic DIP	−40°C t0 +85°C
CDG5341CPE	14-Pin Plastic DIP	0°C t0 +70°C
CDG5341EJE	14-Pin CerDIP	−40°C to +85°C
CDG5341MJE	14-Pin CerDIP	−55°C to +125°C

RECOMMENDED OPERATING CONDITIONS

Negative Supply Voltage .... −8V to −15V
Positive Supply Voltage .... +8V to +15V
Control Input Voltage Range .... 0V to +5V
Analog Switch Voltage Range .... ±10V
Operating Temperature Range
M Suffix .... −55°C to +125°C
E Suffix .... −40°C to +85°C
C Suffix .... 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Negative Supply Voltage .... −20V
Positive Supply Voltage .... +20V
Control Input Voltage
Range .... V^+ +0.3V, V^- −0.3V
Continuous Current, Any Pin Except S or D .... 20 mA
Continuous Current, S or D .... 30 mA
Peak Pulsed Current, S or D,
80 μs, 1%, Duty Cycle .... 100 mA
Junction Temperature Range .... −55°C to +125°C
Storage Temperature Range .... −65°C to +150°C
Power Dissipation .... 500 mW
(Derate at 12 mW/°C Above +85°C)

NOTE: All devices contain diodes to protect inputs against damage due to high-static voltages or electric fields. However, it is advised precautions be taken not to exceed the maximum recommended input voltages. All unused inputs must be connected to an appropriate logic voltage level (V_{DD} or GND). Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, V^- = −15V, V^+ = +15V per channel, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static						
V_{ANALOG}	Analog Signal Range		−10	—	+10	V
$r_{DS(ON)}$	Switch ON Resistance	V_S = −10V, I_S = −1 mA	—	100	160	Ω
		V_S = +2V, I_S = 1 mA	—	110	160	Ω
		V_S = +10V, I_S = −1 mA	—	200	320	Ω
V_{IH}	High Level Input Voltage		4.5	3.4	—	V
V_{IL}	Low Level Input Voltage		—	—	1	V
I_{IN}	Logic Input Leakage Current	V_{IN} = +5V	—	0.01	0.1	μA
		V_{IN} = +15V	—	0.02	0.1	μA
$I_{D(OFF)}$	Switch OFF Leakage Current	V_D = +10V, V_S = −10V	—	0.2	5	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_S = +10V, V_D = −10V	—	0.2	5	nA
I^-	Negative Supply Quiescent Current	V_{IN} = 0 or V^+	—	−0.1	−0.5	μA
I^+	Positive Supply Quiescent Current	V_{IN} = 0 or V^+	—	0.1	0.5	μA
Dynamic						
t_{ON}	Switch Turn-On Time	V_{IN} = +5V	—	150	250	ns
t_{OFF}	Switch Turn-Off Time	V_{IN} = +5V	—	80	220	ns
OIRR	Off Isolation Rejection Ratio	f = 10 MHz, R_L = 50Ω	80	—	—	dB
CCRR	Cross-Coupling Rejection Ratio	f = 10 MHz, R_L = 50Ω	80	—	—	dB
	Frequency Roll-Off (Bandwidth)	f = 10 MHz, R_L = 50Ω	—	1	3	dB
C_D	Drain-Node Capacitance	V_D = 0, f = 1 MHz, V_{IN} = 0V	—	0.3	—	pF
C_S	Source-Node Capacitance	V_S = 0, f = 1 MHz, V_{IN} = 0V	—	3	—	pF

DUAL MONOLITHIC, SPST CMOS/DMOS "T" CONFIGURATION ANALOG SWITCH

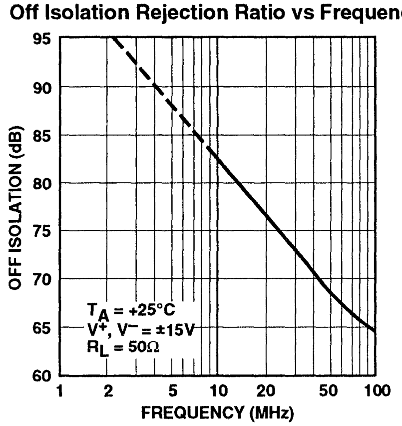
ELECTRICAL CHARACTERISTICS: $V^- = -15V$, $V^+ = +15V$ per channel, unless otherwise noted.

Limits at Temperature Extremes

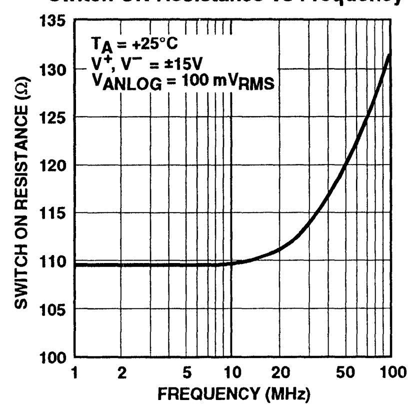
Symbol	Parameter	Test Conditions	Maximum @ T_A = −55°C	−40°C	+70°C	+85°C	+125°C	Unit
Static								
V_{ANALOG}	Analog Signal Range		±10	±10	±10	±10	±10	V
$r_{DS(ON)}$	Switch ON Resistance	$V_S = -10V$, $I_S = -1$ mA	160	160	240	240	300	Ω
		$V_S = +2V$, $I_S = +1$ mA	160	160	240	240	300	Ω
		$V_S = +10V$, $I_S = -1$ mA	320	320	480	480	600	Ω
I_{IN}	Logic Input Leakage Current	$V_{IN} = +5V$	0.1	0.1	1	1	10	µA
		$V_{IN} = +15V$	0.1	0.1	2	2	20	µA
$I_{D(OFF)}$	Switch OFF Leakage Current	$V_D = +10V$, $V_S = -10V$	5	5	100	100	1000	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	$V_S = +10V$, $V_D = -10V$	5	5	100	100	1000	nA
I^-	Negative Supply Quiescent Current	$V_{IN} = 0$ or V^+	−0.5	−0.5	−20	−20	−100	µA
I^+	Positive Supply Quiescent Current	$V_{IN} = 0$ or V^+	0.5	0.5	20	20	100	µA

TYPICAL PERFORMANCE CHARACTERISTICS CURVES

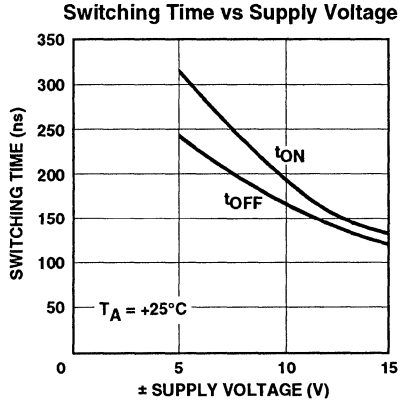
Off Isolation Rejection Ratio vs Frequency



Switch ON Resistance vs Frequency



Switching Time vs Supply Voltage



NOTES

TELEDYNE COMPONENTS

TC4201
TC4202
TC4203

QUAD SINGLE-POLE CMOS ANALOG SWITCHES

FEATURES

- **Low $r_{DS(ON)}$ (+25°C) .... <175Ω Max**
- **Analog Input Leakage Current .... 1 nA**
- **Analog Input Equal to Supply**
- **Supply Current .... 300 µA**
- **Low-Current Logic Input**
- **Pin Compatible With DG201 (TC4201)**

GENERAL DESCRIPTION

The TC4201, TC4202 and TC4203 are quad CMOS analog switches, specifically designed for low supply voltage applications. Special care was taken to reduce crosstalk and feedthrough, while maintaining uniform "on" resistance at supply voltages as low as ±1.5V. This also results in extremely low charge transfer during switching, typically 5 pC, compared to 30 pC with similar devices.

Charge transfer is an extremely important consideration in the design of sample-and-hold circuits, low-level analog signal switching, and interfacing to high-input impedances, such as those presented by analog-to-digital converters.

This switch family offers four independent single-pole, single-throw (SPST) circuits and features single- or dual-supply operation, with analog input voltage range equal to the supply voltage. The CMOS design requires very low supply current.

The TC4201 consists of four normally-open (Form A) contacts.

The TC4202 consists of four normally-open (Form B) contacts.

The TC4203 combines two Form A contacts with two Form B contacts, and may be configured as two Form C (SPDT) circuits.

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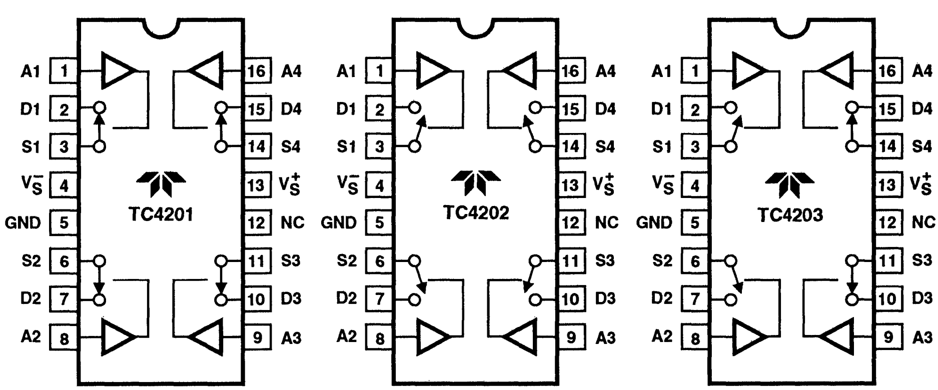
PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION

TC4201
TC4202
TC4203

QUAD SINGLE-POLE CMOS ANALOG SWITCHES

TRUTH TABLE

Logic	TC4201 SW1–4	TC4202 SW1–4	TC4203 SW1	SW2	SW3	SW4
0	Closed	Open	Open	Open	Closed	Closed
1	Open	Closed	Closed	Closed	Open	Open

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC420XCPE	16-Pin Plastic DIP	0°C to +70°C
TC420XCOE	16-Pin SO Wide	0°C to +70°C
TC420XIJE	16-Pin CerDIP	–25°C to +85°C
TC420XMJE	16-Pin CerDIP	–55°C to +125°C

NOTE: X = 1, 2 or 3.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_S^+ to V_S^- .... +18V
- V_S^+ to GND .... +18V
- V_S^- to GND .... –18V
- V_S or V_D to V_S^- .... 0V to +18V
- V_S or V_D to V_S^+ .... 0V to –18V
- $V_{DIGITAL}$ to GND .... V_S^-, V_S^+

Current*
- Any Pin .... 20 mA
- S or D, Peak (1 ms, 10% Duty Cycle) .... 70 mA

Storage Temperature Range .... +65°C to +150°C

Operating Temperature Range
- Plastic DIP (C) .... 0°C to +70°C
- CerDIP (I) .... –25°C to +85°C
- CerDIP (M) .... –55°C to +125°C

Package Power Dissipation (T_A = +25°C)
- Plastic DIP (C) .... 375 mW (Notes 1, 2)
- CerDIP (I and M) .... 500 mW (Notes 1, 3)

*Input voltages that exceed V_S^+ or V_S^- will be clamped by internal diodes. Limit current to maximum current ratings.

NOTES:
1. All pins soldered or welded to PC board.
2. Derate at 6.5 mW/°C above +75°C.
3. Derate at 13 mW/°C above +75°C.

Static-sensitive devices. Unused devices should be stored in conductive material. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied.

ELECTRICAL CHARACTERISTICS: V_S^+ = +5V, V_S^- = 0V, GND = 0V, unless otherwise indicated.

Symbol	Parameter	Test Conditions	+25°C Min	Typ	Max	0°C to +70°C Min	Max	–25°C to +85°C Min	Max	–55°C to +125°C Min	Max	Unit
Switches												
V_S, V_D	Analog Input Signal Range		0	—	5	0	5	0	5	0	5	V
$r_{DS(ON)}$	Drain Source On Resistance	I_S = 1 mA, Switch On	—	105	195	—	240	—	240	—	260	Ω
$I_{S(OFF)}$	Source Off Leakage Current	V_S = 0.5V to 4.5V, V_D = 4.5 to 0.5V, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(OFF)}$	Drain Off Leakage Current	V_S = 0.5V to 4.5V, V_D = 4.5 to 0.5V, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(ON)}$	Drain On Leakage Current	V_D = V_S = 0.5V to 4.5V, Switch Off	—	0.02	1	—	200	—	200	—	230	nA

QUAD SINGLE-POLE CMOS ANALOG SWITCHES

TC4201 TC4202 TC4203

ELECTRICAL CHARACTERISTICS: $V_S^+ = +5V$, $V_S^- = -5V$, GND = 0V, unless otherwise indicated.

Symbol	Parameter	Test Conditions	+25°C Min	+25°C Typ	+25°C Max	0°C to +70°C Min	0°C to +70°C Max	–25°C to +85°C Min	–25°C to +85°C Max	–55°C to +125°C Min	–55°C to +125°C Max	Unit
Switches												
V_S, V_D	Analog Input Signal Range		–5	—	+5	–5	+5	–5	+5	–5	+5	V
$r_{DS(ON)}$	Drain Source On Resistance	$V_D = \pm3.5V$, Switch On, $I_S = 1$ mA	—	95	175	—	230	—	230	—	250	Ω
$I_{S(OFF)}$	Source Off Leakage Current	$V_S = \pm4.5V$, $V_D = \mp4.5V$, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(OFF)}$	Drain Off Leakage Current	$V_S = \pm4.5V$, $V_D = \mp4.5V$, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(ON)}$	Drain On Leakage Current	$V_D = V_S = \pm4.5V$, Switch On	—	0.02	1	—	200	—	200	—	230	nA
Digital												
V_{INH}	Input High Voltage (Logic "1")		—	1.5	2.4	—	2.4	—	2.4	—	2.4	V
V_{INL}	Input Low Voltage (Logic "0")		0.8	1.5	—	0.8	—	0.8	—	0.8	—	V
I_{INH}	Input Current With Input High Voltage	$V_{IN} = 5V$	—	0.001	1	—	10	—	10	—	12	µA
I_{INL}	Input Current With Input Low Voltage	$V_{IN} = 0V$	—	0.001	1	—	10	—	10	—	12	µA
Dynamic												
t_{ON}	Turn-On Time	See Switch Time Test Circuit	—	250	500	—	650	—	650	—	750	ns
t_{OFF}	Turn-Off Time	See Switch Time Test Circuit	—	185	350	—	450	—	450	—	550	ns
Q_{INJ}	Charge Injection	$C_L = 1$ nF, $V_{GEN} = 0V$, $R_{GEN} = 0\Omega$	—	5	—	—	—	—	—	—	—	pC
$C_{S(OFF)}$	Source Off Capacitance	$V_D = V_S = 0V$, f = 100 kHz	—	8	—	—	—	—	—	—	—	pF
$C_{D(OFF)}$	Drain Off Capacitance	$V_D = V_S = 0V$, f = 100 kHz	—	8	—	—	—	—	—	—	—	pF
$C_{C(ON)}$	Channel-On Capacitance	$V_D = V_S = 0V$, f = 100 kHz	—	23	—	—	—	—	—	—	—	pF
OIRR	Off Isolation	f = 100 kHz, $R_L = 1000\Omega$	—	65	—	—	—	—	—	—	—	dB
CCRR	Cross-Talk Rejection	f = 100 kHz, $R_L = 1000\Omega$	—	85	—	—	—	—	—	—	—	dB
Power Supply												
I_S^+	Positive Supply Current	$V_{IN} = 5V$	—	275	500	—	700	—	700	—	750	µA
I_S^-	Negative Supply Current	$V_{IN} = 5V$	—	0.01	10	—	10	—	10	—	12	µA
Supply Operating Range												
	V_S^+ to V_S^- and V_S^+ to GND		3	—	16	3	16	3	16	3	16	V

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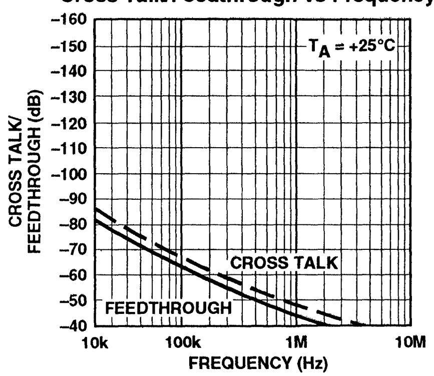
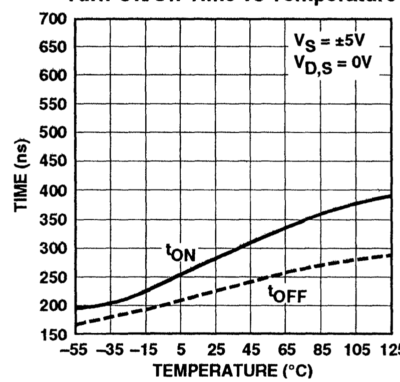
TYPICAL CHARACTERISTIC CURVES

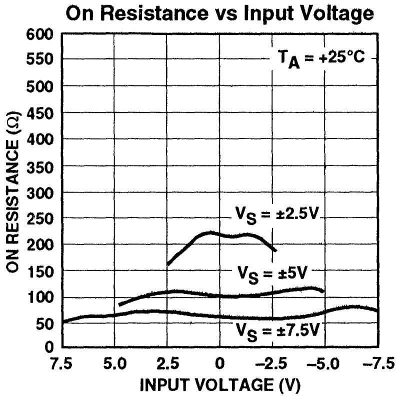
Cross Talk/Feedthrough vs Frequency



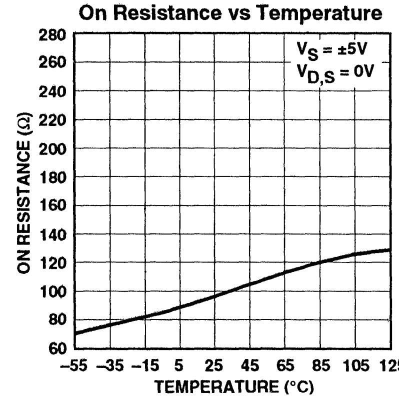
Turn-On/Off Time vs Temperature



On Resistance vs Input Voltage

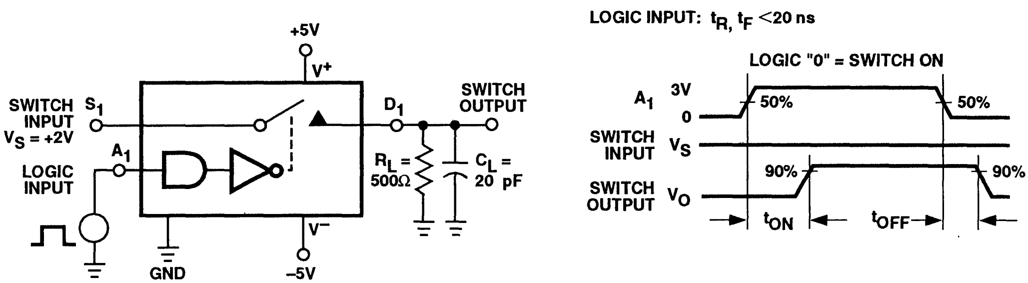


On Resistance vs Temperature



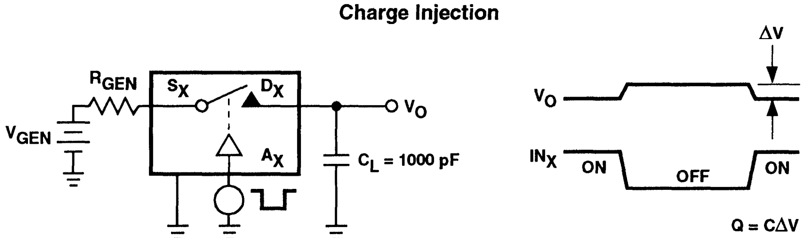
TEST CIRCUITS

Switching Time

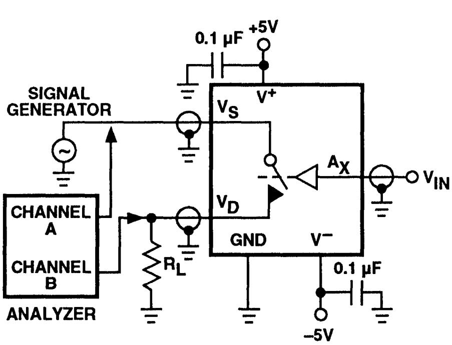


NOTE: Repeat test for A2, A3 and A4.

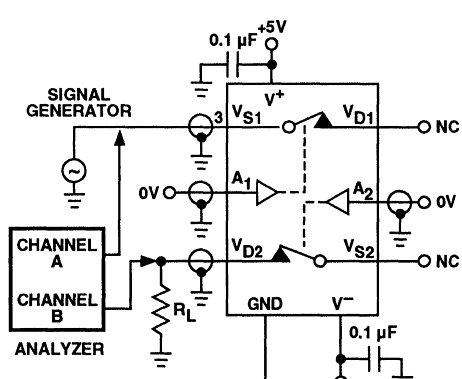
Charge Injection



Off Isolation



Channel-to-Channel Cross-Talk



$$CCRR = 20 \text{ Log } \frac{V_{S1}}{V_{D2}}$$

NOTES

TELEDYNE COMPONENTS

TC441
TC442
TC443

MICROPROCESSOR COMPATIBLE CMOS ANALOG SWITCHES

FEATURES

- **Data Address Latch On-Chip**
- **Transparent Latch With WR = 0**
- **Write Pulse Operation ....< 250 ns**
- **Dual- or Single-Supply Operation**
- **Low $r_{DS(ON)}$ (+25°C)................................< 175Ω Max**
- **Supply Current ....300 µA**
- **Analog Input Equal to Supply**
- **Analog Input Leakage Current ....1 nA**
- **TTL/CMOS Compatible**
- **Low-Current Logic Input**
- **Pin Compatible With DG201 and DG221 (TC441)**

GENERAL DESCRIPTION

The TC441, TC442 and TC443 are CMOS quad, SPST analog switches with data address latches. Their pinouts match the "201/221" analog switch configuration. The write input ($\overline{WR}$, pin 12) is not used on the 201/221. The address latch is transparent when $\overline{WR}$ is tied low.

This switch family features single- or dual-supply operation, with analog input voltage range equal to the supply voltage. The CMOS design requires very low supply current.

The TC441 has four normally-closed (Form B) contacts, the TC442 has four normally-open contacts (Form A), and the TC443 has two normally-open and two normally-closed contacts.

The TC443 can be configured as two DPST (Form C) switches.

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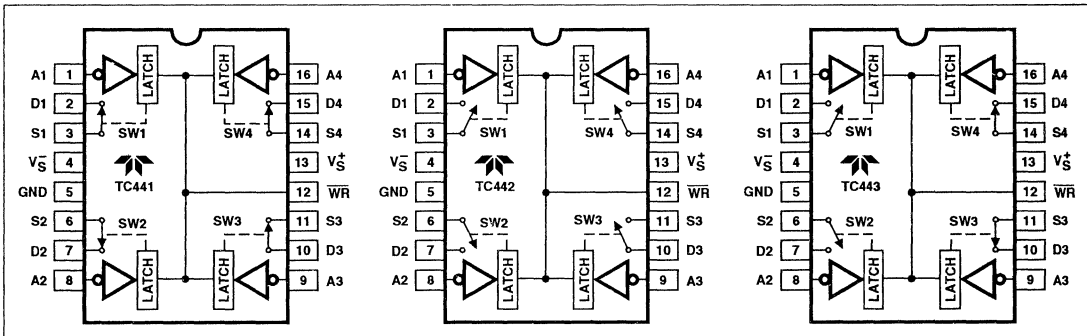
PIN CONFIGURATIONS



SWITCHES SHOWN WITH An = 0

1072-1

TC441
TC442
TC443

MICROPROCESSOR COMPATIBLE CMOS ANALOG SWITCHES

ORDERING INFORMATION

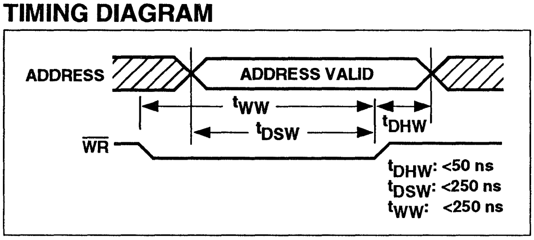
Part No.	Package	Temperature Range
TC44XCPE	16-Pin Plastic DIP	0°C to +70°C
TC44XCOE	16-Pin Plastic SO	0°C to +70°C
TC44XIJE	16-Pin CerDIP	–25°C to +85°C
TC44XMJE	16-Pin CerDIP	–55°C to +125°C

X = 1, 2 or 3.

TRUTH TABLE (Switch State)

A_N	$\overline{WR}$	TC441	TC442	TC443
0	0	Closed	Open	SW1, SW2 Open SW3, SW4 Closed
1	0	Open	Closed	SW1, SW2 Closed SW3, SW4 Open
X	1	Maintain Previous State		

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_S^+ to V_S^- .... +18V
- V_S^+ to GND .... +18V
- V_S^- to GND .... –18V
- V_S or V_D to V_S^+ .... 0V, –18V
- V_S or V_D to V_S^- .... 0V, +18V
- $V_{DIGITAL}$ to GND .... V_S^-, V_S^+

Current*
- Any Pin .... 20 mA
- S or D, Peak (1 ns, 10% Duty Cycle) .... 70 mA

Storage Temperature Range .... –65°C to +150°C

Operating Temperature Range
- Plastic DIP (C) .... 0°C to +70°C
- CerDIP (I) .... –25°C to +85°C
- CerDIP (M) .... –55°Cto +125°C

Package Power Dissipation (T_A = +25°C)
- Plastic DIP (C) .... 375 mW (Notes 1 and 2)
- CerDIP (I and M) .... 500 mW (Notes 1 and 3)

*Input voltages that exceed V_S^+ or V_S^- will be clamped by internal diodes. Limit current to maximum current ratings.

NOTES:
1. All pins soldered or welded to PC board.
2. Derate at 6.5 mW/°C.
3. Derate at 13 mW/°C above +75°C.
4. Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S^+ = +5V, V_S^- = 0V, GND = 0V, unless otherwise indicated.

			+25°C			0°C to +70°C		–25°C +85°C		–55°C to +125°C		
Symbol	Parameter	Test Conditions	Min	Typ	Max	Min	Max	Min	Max	Min	Max	Unit
Switches												
V_S, V_D	Analog Input Signal Range		0	—	5	0	5	0	5	0	5	V
$r_{DS(ON)}$	Drain Source On Resistance	I_S = 1 mA, Switch On	—	105	195	—	240	—	240	—	260	Ω
$I_{S(OFF)}$	Source Off Leakage Current	V_S = 0.5V–4.5V, V_D = 4.5V–0.5V, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(OFF)}$	Drain Off Leakage Current	V_S = 0.5V–4.5V, V_D = 4.5V–0.5V, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(ON)}$	Drain On Leakage Current	V_D = V_S = 0.5V–4.5V, Switch Off	—	0.02	1	—	200	—	200	—	230	nA

MICROPROCESSOR COMPATIBLE CMOS ANALOG SWITCHES

TC441 TC442 TC443

ELECTRICAL CHARACTERISTICS: V_S^+ = +5V, V_S^- = –5V, GND = 0V, unless otherwise indicated.

			+25°C			0°C to +70°C		–25°C +85°C		–55°C to +125°C		
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Switches												
V_S, V_D	Analog Input Signal Range		–5	—	+5	–5	+5	–5	+5	–5	+5	V
$r_{DS(ON)}$	Drain Source On Resistance	V_D = ±3.5V, Switch On, I_S = 1 mA	—	95	175	—	230	—	230	—	250	Ω
$I_{S(OFF)}$	Source Off Leakage Current	V_S = ±4.5V, V_D = ∓4.5V, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(OFF)}$	Drain Off Leakage Current	V_S = ±4.5V, V_D = ∓4.5V, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(ON)}$	Drain On Leakage Current	V_D = V_S = ±4.5V, Switch On	—	0.02	1	—	200	—	200	—	230	nA
Digital												
V_{INH}	Input High Voltage (Logic "1")		—	1.5	2.4	—	2.4	—	2.4	—	2.4	V
V_{INL}	Input Low Voltage (Logic "0")		0.8	1.5	—	0.8	—	0.8	—	0.8	—	V
I_{INH}	Input Current With Input High Voltage	$V_{DIGITAL}$ = 5V	—	0.001	1	—	10	—	10	—	12	µA
I_{INL}	Input Current With Input Low Voltage	$V_{DIGITAL}$ = 0V	—	0.001	1	—	10	—	10	—	12	µA
Dynamic												
t_{WW}	Write Pulse Width	See Timing Diagram	—	—	250	—	325	—	325	—	375	ns
t_{DSW}	Data Setup Time	See Timing Diagram	—	—	250	—	325	—	325	—	375	ns
t_{DHW}	Data Hold Time	See Timing Diagram	—	—	50	—	50	—	50	—	50	ns
t_{ON}	Turn-On Time	See Switch Time Test Circuit	—	250	500	—	650	—	650	—	750	ns
t_{OFF}	Turn-Off Time	See Switch Time Test Circuit	—	185	350	—	450	—	450	—	550	ns
Q_{INJ}	Charge Injection	C_L = 1 nF, V_{GEN} = 0V, R_{GEN} = 0Ω	—	5	—	—	—	—	—	—	—	pC
$C_{S(OFF)}$	Source-Off Capacitance	V_D = V_S = 0V, f = 100 kHz	—	8	—	—	—	—	—	—	—	pF
$C_{D(OFF)}$	Drain-Off Capacitance	V_D = V_S = 0V, f = 100 kHz	—	8	—	—	—	—	—	—	—	pF
$C_{C(ON)}$	Channel-On Capacitance (Except TC444	V_D = V_S = 0V, f = 100 kHz	—	23	—	—	—	—	—	—	—	pF
OIRR	Off Isolation	f = 100 kHz, R_L = 1000Ω	—	65	—	—	—	—	—	—	—	dB
CCRR	Cross-Talk Rejection	f = 100 kHz, R_L = 1000W	—	70	—	—	—	—	—	—	—	dB
Power Supply												
I_S^+	Positive Supply Current	$V_{DIGITAL}$ = 5V	—	275	500	—	700	—	700	—	750	µA
I_S^-	Negative Supply Current	$V_{DIGITAL}$ = 5V	—	0.01	10	—	10	—	10	—	12	µA
Supply Operating Range												
	V_S^+ to V_S^- and V_S^+ to GND		3	—	16	3	16	3	16	3	16	V

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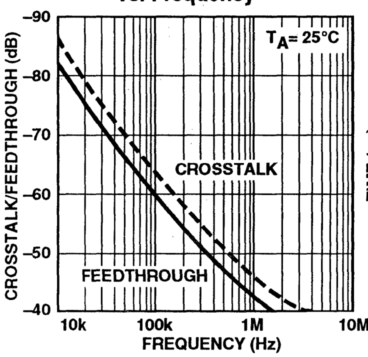
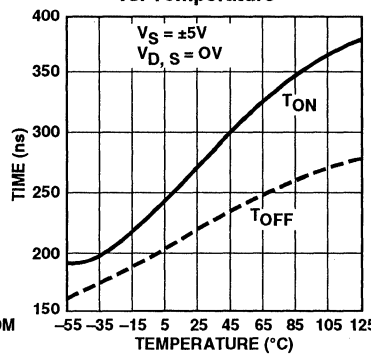
TYPICAL CHARACTERISTIC CURVES

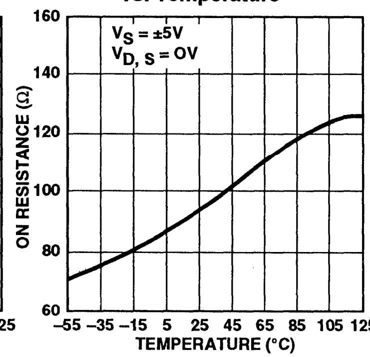
Crosstalk & Feedthrough vs. Frequency



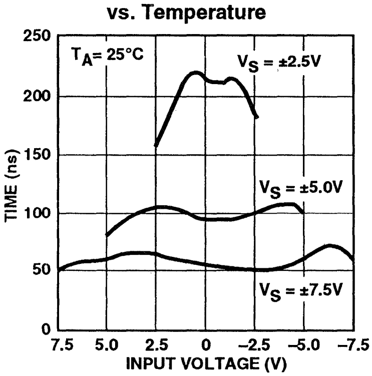
Turn-On/Turn-Off Time vs. Temperature



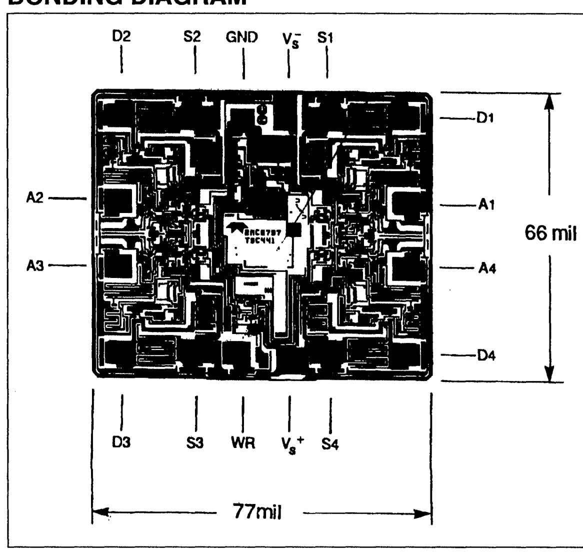
On Resistance vs. Temperature



On Resistance vs. Temperature

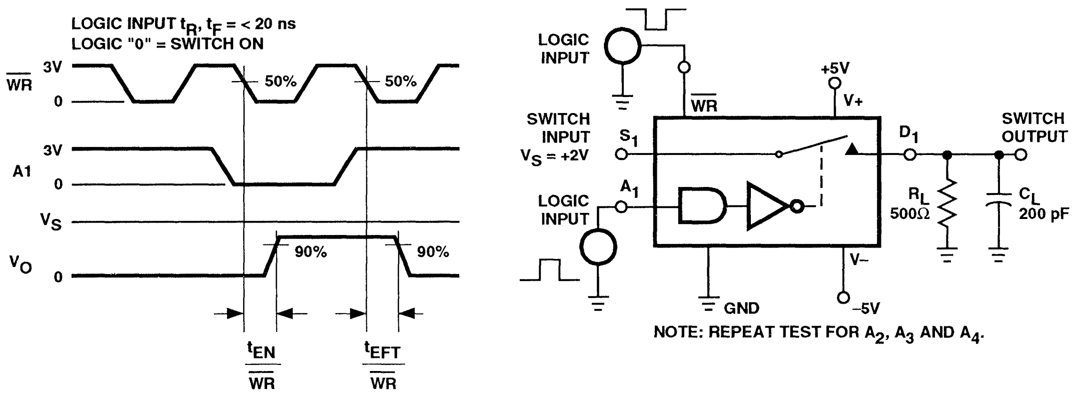


BONDING DIAGRAM

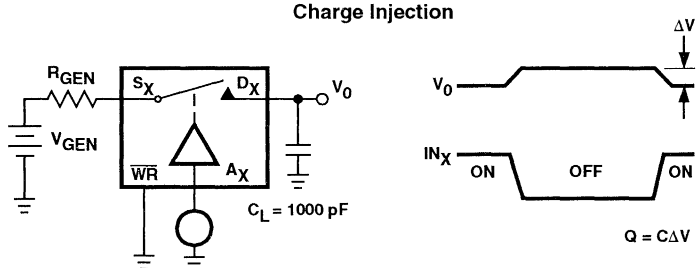


TEST CIRCUITS

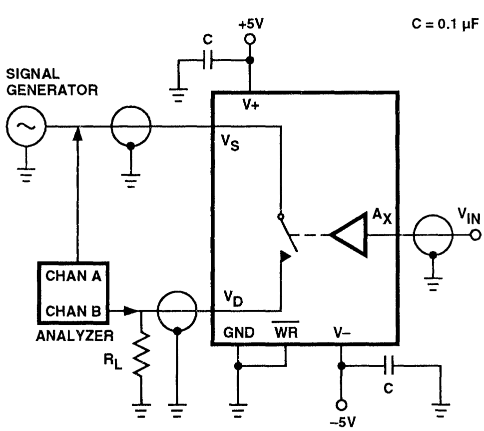
$\overline{WR}$ Switching Time



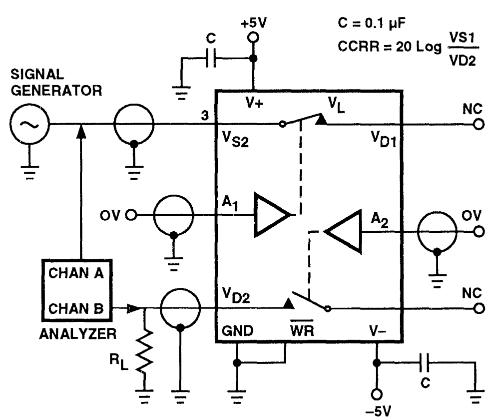
Charge Injection



Off Isolation



Channel-to-Channel Cross Talk



NOTES

MICROPROCESSOR COMPATIBLE CMOS ANALOG SWITCHES

FEATURES

- Data Address Latch On-Chip
- Low-Power CMOS
- Write .... 250 ns
- Transparent Latch With $\overline{WR}$ = 0
- Write Pulse Operation .... <250 ns
- Address Hold Time .... <50 ns
- Dual- or Single-Supply Operation
- $r_{DS(ON)}$ (+25°C) .... <175Ω Max
- Supply Current .... 300 μA
- Analog Input Equal to Supply
- Analog Input Leakage Current .... 1 nA
- TTL/CMOS Compatible
- Low-Current Logic Input
- Pin Compatible With AD7590 Series

GENERAL DESCRIPTION

The TC444, TC445, TC446 and TC447 are CMOS analog switches offering low on-resistance at low supply voltages. Each provides for transparent (nonlatched) or latched addresses, making them ideal for microprocessor interface applications.

This switch family features single- or dual-supply operation, with analog input range equal to supply voltages. The CMOS design requires very low supply current.

The TC444 is configured as two single-pole, three-position switches. Either switch can be independently selected (transparent or latched) for its own A or B position. (See TC444 Switch Circuit.)

Also, both switches are put in the C position (both open) by pulling the $\overline{DISABLE}$ input low. These various switch positions can be latched using the $\overline{WRITE}$ ($\overline{WR}$) input. This switch is especially useful in multi-path operations requiring complete isolation.

The TC445 is configured as four independent, normally-open switches. The $\overline{WR}$ input is used to latch the switches in any selected mode, or may be held low for transparent operation.

The TC446 has the same features as the TC445, except the switches are normally closed.

The TC447 provides two normally-open and two normally-closed switches. Its operation is the same as the TC445 and TC446.

The TC444 is pin compatible with the AD7592. The TC445/TC446 is pin compatible with the AD7590/AD7591.

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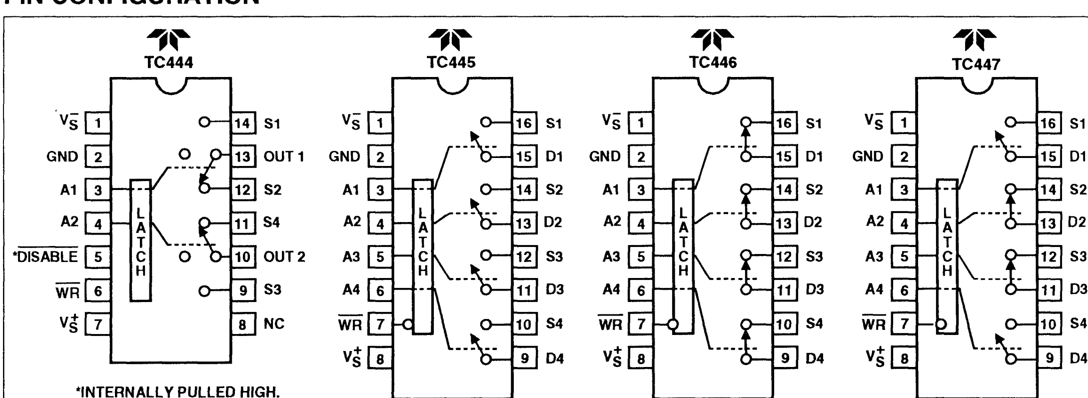
PIN CONFIGURATION



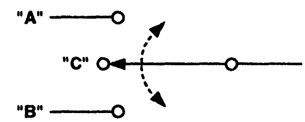
*INTERNALLY PULLED HIGH.

NOTE: All switches shown with A_n = 0.

TC444
TC445
TC446
TC447

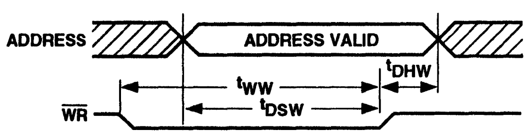
MICROPROCESSOR COMPATIBLE CMOS ANALOG SWITCHES

TC444 SWITCH CIRCUIT



NOTE; Both switches may be latched in the off state by pulling $\overline{\text{WR}}$ high when $\overline{\text{DISABLE}}$ is low.

TIMING DIAGRAM



ORDERING INFORMATION

Part No.	Package	Temperature Range
TC444		
TC444CPD	14-Pin Plastic DIP	0°C to +70°C
TC444COD	14-Pin Plastic SO	0°C to +70°C
TC444IJD	14-Pin CerDIP	–25°C to +85°C
TC444MJD	14-Pin CerDIP	–55°C to +125°C
TC445/446/447		
TC44XCPE	16-Pin Plastic DIP	0°C to +70°C
TC44XCOE	16-Pin Plastic SO	0°C to +70°C
TC44XIJE	16-Pin CerDIP	–25°C to +85°C
TC44XMJE	16-Pin CerDIP	–55°C to +125°C

X = 5, 6 or 7

TC444 TRUTH TABLE (Switch State)

$\overline{\text{DISABLE}}$	A_N	$\overline{\text{WR}}$	TC444
0	X	X	All switches open
1	0	0	S2 to OUT 1 closed S4 to OUT 2 closed
1	1	0	S1 to OUT 1 closed S3 to OUT 2 closed
1	X	1	Maintain previous state

TC445/446/447 TRUTH TABLE (Switch State)

A_N	$\overline{\text{WR}}$	TC445	TC446	TC447
0	0	Open	Closed	SW1, SW4 open SW2, SW3 closed
1	0	Closed	Open	SW1, SW4 closed SW2, SW3 open
X	1	Maintain previous state		

X = Don't Care

MICROPROCESSOR COMPATIBLE CMOS ANALOG SWITCHES

TC444 TC445 TC446 TC447

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_S^+ to V_S^- .... +18V
- V_S^+ to GND .... +18V
- V_S^- to GND .... –18V
- V_S or V_D to V_S^+ .... 0V, –18V
- V_S or V_D to V_S^- .... 0V, +18V
- $V_{DIGITAL}$ to GND .... V_S^-, V_S^+

Current*
- Any Pin .... 20 mA
- S or D, Peak (1 ns, 10% Duty Cycle) .... 70 mA

Storage Temperature .... –65°C to +150°C

Operating Temperature Range
- Plastic DIP (C) .... 0°C to +70°C
- CerDIP (I) .... –25°C to +85°C
- CerDIP (M) .... –55°Cto +125°C

Package Power Dissipation (T_A = +25°C)
- Plastic DIP (C) .... 375 mW (Notes 1, 2)
- CerDIP (I and M) .... 500 mW (Notes 1, 3)

* Input voltages that exceed V_S^+ or V_S^- will be clamped by internal diodes. Limit current to maximum current ratings.

NOTES: 1. All pins soldered or welded to PC board.
2. Derate at 6.5 mW/°C.
3. Derate at 13 mW/°C above +75°C.

ELECTRICAL CHARACTERISTICS: V_S^+ = +5V, V_S^- = 0V, GND = 0V, unless otherwise indicated.

Symbol	Parameter	Test Conditions	+25°C Min	+25°C Typ	+25°C Max	0°C to +70°C Min	0°C to +70°C Max	–25°C to +85°C Min	–25°C to +85°C Max	–55°C to +125°C Min	–55°C to +125°C Max	Unit
Switches												
V_S, V_D	Analog Input Signal Range		0	—	5	0	5	0	5	0	5	V
$r_{DS(ON)}$	Drain Source On Resistance	I_S = 1 mA, Switch On	—	105	195	—	240	—	240	—	260	Ω
$I_{S(OFF)}$	Source Off Leakage Current	V_S = 0.5V to 4.5V, V_D = 4.5 to 0.5V, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(OFF)}$	Drain Off Leakage Current	V_S = 0.5V to 4.5V, V_D = 4.5 to 0.5V, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(ON)}$	Drain On Leakage Current	V_D = V_S = 0.5V to 4.5V, Switch Off	—	0.02	1	—	200	—	200	—	230	nA

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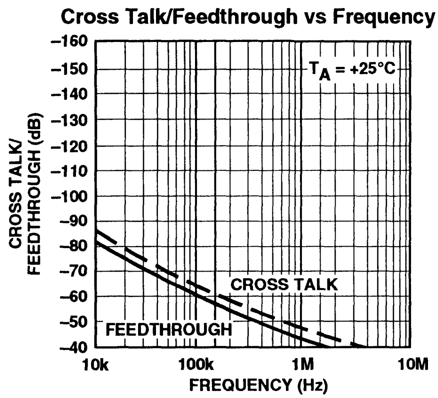
ELECTRICAL CHARACTERISTICS: V_S^+ = +5V, V_S^- = –5V, GND = 0V, unless otherwise indicated.

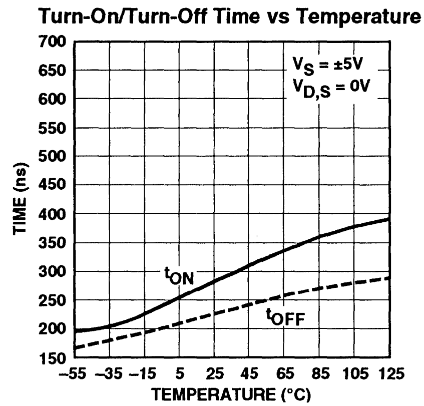
Symbol	Parameter	Test Conditions	+25°C Min	+25°C Typ	+25°C Max	0°C to +70°C Min	0°C to +70°C Max	–25°C to +85°C Min	–25°C to +85°C Max	–55°C to +125°C Min	–55°C to +125°C Max	Unit
Switches												
V_S, V_D	Analog Input Signal Range		–5	—	5	–5	5	–5	5	–5	5	V
$r_{DS(ON)}$	Drain Source On Resistance	V_D = ±3.5V, Switch On, I_S = 1 mA	—	95	175	—	230	—	230	—	250	Ω
$I_{S(OFF)}$	Source Off Leakage Current	V_S = ±4.5V, V_D = ∓4.5V, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(OFF)}$	Drain Off Leakage Current	V_S = ±4.5V, V_D = ∓4.5V, Switch Off	—	0.01	1	—	100	—	100	—	120	nA
$I_{D(ON)}$	Drain On Leakage Current	V_D = V_S = ±4.5V, Switch On	—	0.02	1	—	200	—	200	—	230	nA
Digital												
V_{INH}	Input High Voltage (Logic "1")		—	1.5	2.4	—	2.4	—	2.4	—	2.4	V
V_{INL}	Input Low Voltage (Logic "0")		0.8	1.5	—	0.8	—	0.8	—	0.8	—	V

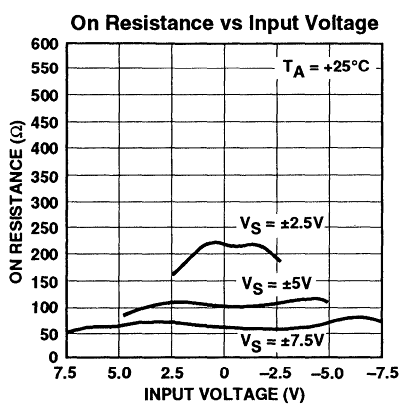
ELECTRICAL CHARACTERISTICS (Cont.)

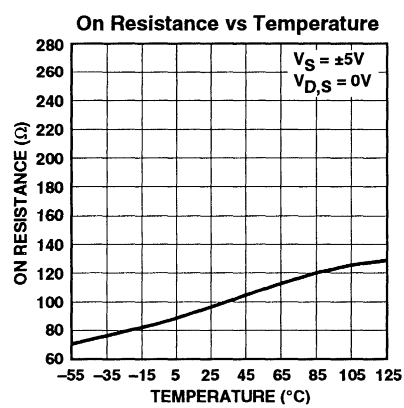
Symbol	Parameter	Test Conditions	+25°C Min	+25°C Typ	+25°C Max	0°C to +70°C Min	0°C to +70°C Max	−25°C to +85°C Min	−25°C to +85°C Max	−55°C to +125°C Min	−55°C to +125°C Max	Unit
Digital (Cont.)												
I_{INH}	Input Current With Input High Voltage	$V_{DIGITAL}$ = 5V	—	0.001	1	—	10	—	10	—	12	μA
I_{INL}	Input Current With Input Low Voltage	$V_{DIGITAL}$ = 0V	—	0.001	1	—	10	—	10	—	12	μA
V_{INH}	$\overline{\text{DISABLE}}$ Input (TC444)	$V_{DIGITAL}$ = 5V	—	0.1	10	—	15	—	15	—	17	μA
V_{INL}	$\overline{\text{DISABLE}}$ Input (TC444)	$V_{DIGITAL}$ = 0V	—	5	10	—	15	—	15	—	15	μA
Dynamic												
t_{WW}	Write Pulse Width	See Timing Diagram	—	—	250	—	325	—	325	—	375	ns
t_{DSW}	Data Setup Time	See Timing Diagram	—	—	250	—	325	—	325	—	375	ns
t_{DHW}	Data Hold Time	See Timing Diagram	—	—	50	—	50	—	50	—	50	ns
t_{ON}	Turn-On Time	See Switch Time Test Circuit	—	250	500	—	650	—	650	—	750	ns
t_{OFF}	Turn-Off Time	See Switch Time Test Circuit	—	185	350	—	450	—	450	—	550	ns
Q_{INJ}	Charge Injection	C_L = 1 nF, V_{GEN} = 0V, R_{GEN} = 0Ω	—	5	—	—	—	—	—	—	—	pC
$C_{S(OFF)}$	Source-Off Capacitance	$V_D = V_S$ = 0V, f = 100 kHz	—	8	—	—	—	—	—	—	—	pF
$C_{D(OFF)}$	Drain-Off Capacitance	$V_D = V_S$ = 0V, f = 100 kHz	—	8	—	—	—	—	—	—	—	pF
$C_{C(ON)}$	Channel-On Capacitance (Except TC444)	$V_D = V_S$ = 0V, f = 100 kHz	—	23	—	—	—	—	—	—	—	pF
$C_{C(ON)}$	Channel-On Capacitance (TC444 Only)	$V_D = V_S$ = 0V, f = 100 kHz	—	30	—	—	—	—	—	—	—	pF
DIRR	Off Isolation	f = 100 kHz, R_L = 1000Ω	—	65	—	—	—	—	—	—	—	dB
CCRR	Cross-Talk Rejection	f = 100 kHz, R_L = 1000Ω	—	70	—	—	—	—	—	—	—	dB
Power Supply												
I_S^+	Positive Supply Current	$V_{DIGITAL}$ = 5V	—	275	500	—	700	—	700	—	750	μA
I_S^-	Negative Supply Current	$V_{DIGITAL}$ = 5V	—	0.01	10	—	10	—	10	—	12	μA
Supply Operating Range												
	V_S^+ to V_S^- and V_S^+ to GND		3	—	16	3	16	3	16	3	16	V

TYPICAL CHARACTERISTIC CURVES



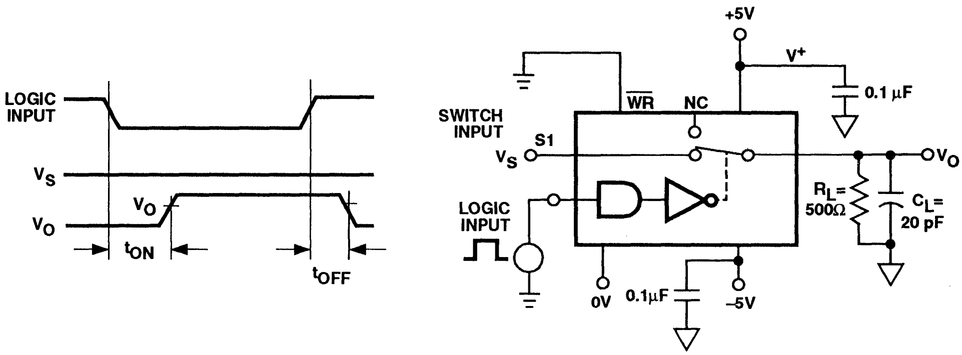




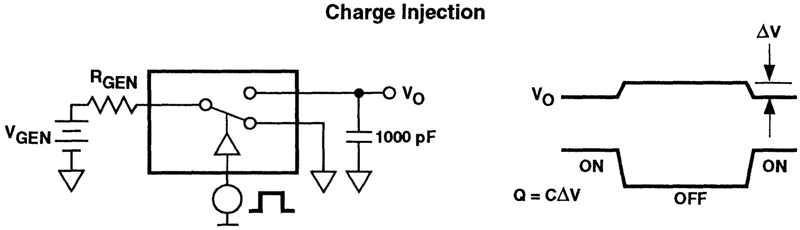


TEST CIRCUITS

Switching Time

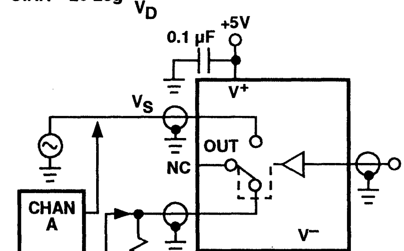


Charge Injection



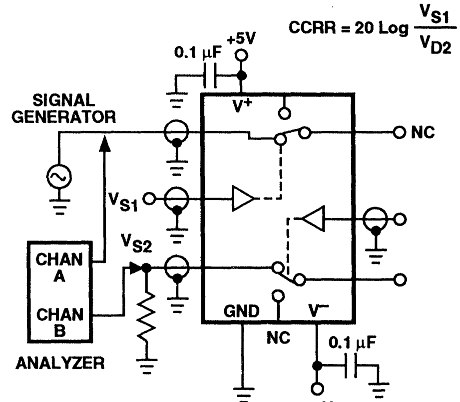
OIRR Off Isolation

$$\text{OIRR} = 20 \text{ Log } \frac{V_S}{V_D}$$



CCRR Channel-to-Channel Cross-Talk

$$\text{CCRR} = 20 \text{ Log } \frac{V_{S1}}{V_{D2}}$$



Section 13

Data Communications

DUAL RS-232 TRANSMITTER/RECEIVER AND POWER SUPPLY

FEATURES

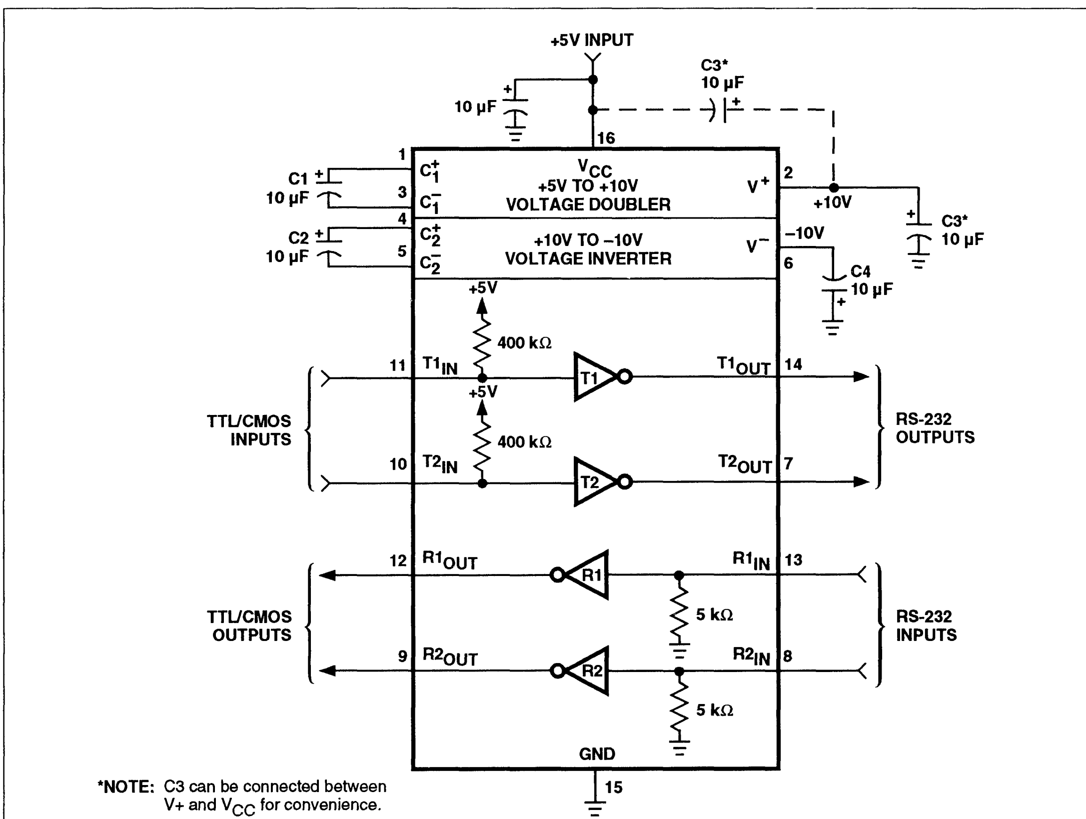
- **Meets All RS-232C Specifications**
- **Operates From Single 5V Power Supply**
- **2 Drivers and 2 Receivers**
- **On-Board Voltage Quadrupler**
- **Input Levels .... ±30V**
- **Output Swing With +5V Supply .... ±9V**
- **Low Power CMOS .... 5 mA**

GENERAL DESCRIPTION

The TC232 is a dual RS-232 transmitter/receiver that complies with EIA RS-232C guidelines and is ideal for all RS-232C communication links. This device has a 5V power supply and two charge pump voltage converters that produce ±10V power supplies.

The TC232 has four level translators. Two are RS-232 transmitters that convert TTL/CMOS input levels to 9V RS-232 outputs. The other two translators are RS-232 receivers that convert RS-232 inputs to 5V TTL/CMOS output levels. The receivers have a nominal threshold of 1.3V, a typical hysteresis of 0.5V, and can operate with up to ±30V inputs.

TYPICAL APPLICATION



***NOTE:** C3 can be connected between V+ and V_{CC} for convenience.

*Patented

TC232

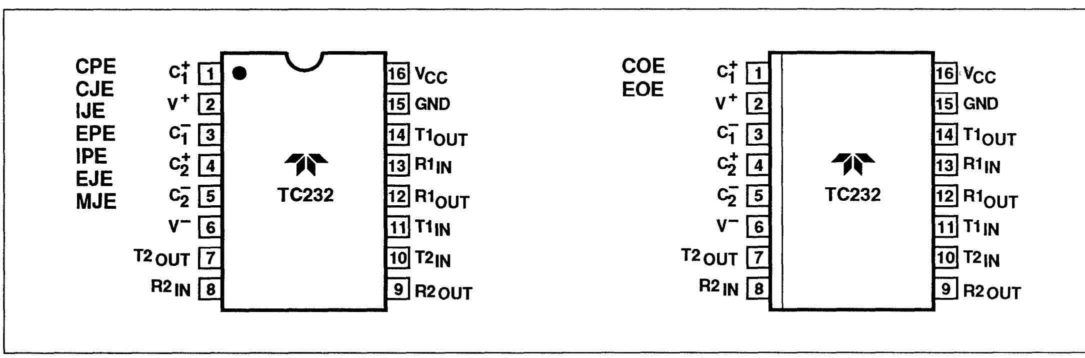
APPLICATIONS

The TC232 is ideal for all RS-232C communication links: Battery-powered systems, computers, instruments, modems, and peripherals. It can run without the 12V power supplies other RS-232 devices require.

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC232CPE	16-Pin Plastic	0°C to +70°C
TC232CJE	16-Pin CerDIP	0°C to +70°C
TC232IJE	16-Pin CerDIP	–25°C to +85°C
TC232EPE	16-Pin Plastic	–40°C to +85°C
TC232IPE	16-Pin Plastic	–25°C to +85°C
TC232EJE	16-Pin CerDIP	–40°C to +85°C
TC232COE	16-Pin SO	0°C to +70°C
TC232EOE	16-Pin SO	–40°C to +85°C
TC232MJE	16-Pin CerDIP	–55°C to +125°C

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

V_{CC} .... +6V
V^+ .... +12V
V^- .... +12V
Input Voltages
  $T1_{IN}$, $T2_{IN}$ .... –0.3 to (V_{CC} +0.3V)
  $R1_{IN}$, $R2_{IN}$ .... ±30V
Output Voltages
  $T1_{OUT}$, $T2_{OUT}$ .... (V^+ +0.3V) to (V^- –0.3V)
  $R1_{OUT}$, $R2_{OUT}$ .... –0.3 to (V_{CC} +0.3V)
Short Circuit Duration
  V^+ .... 30 sec
  V^- .... 30 sec
  $T1_{OUT}$, $T2_{OUT}$ .... Continuous

Power Dissipation
  CerDIP .... 675 mW
    Derate 9.5 mW/°C Above +70°C
  Plastic DIP .... 375 mW
    Derate 7 mW/°C Above +70°C
  Small Outline (SO) .... 375 mW
    Derate 7 mW/°C Above +70°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{CC} = 5V ±10%, T_A = operating temperature range, test circuit unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Output Voltage Swing	$T1_{OUT}$, $T2_{OUT}$ Loaded With 3 kΩ to Ground	±5	±9	±10	V
Power Supply Current			5	10	mA
Input Logic Threshold Low	$T1_{IN}$, $T2_{IN}$			0.8	V
Input Logic Threshold High	$T1_{IN}$, $T2_{IN}$	2			V
Logic Pull-Up Current	$T1_{IN}$, $T2_{IN}$ = 0V		15	200	µA
RS-232 Input Voltage Operating Range		–30		+30	V
RS-232 Input Threshold Low	V_{CC} = 5V	0.8	1.2		V
RS-232 Input Threshold High	V_{CC} = 5V		1.7	2.4	V
RS-232 Input Hysteresis		0.2	0.5	1	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V	3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2 mA			0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = –1 mA	3.5			V
Propagation Delay	RS-232 to TTL or TTL to RS-232		0.5		µs
Instantaneous Slew Rate	C_L = 10 pF, R_L = 3 kΩ to 7 kΩ, T_A = +25°C (Note 1)			30	V/µs
Transition Region Slew Rate	R_L = 3 kΩ, C_L = 2500 pF Measured From +3V to –3V or –3V to +3V		3		V/µs
Output Resistance	$V_{CC} = V^+ = V^-$ = 0V, V_{OUT} = ±2V	300			Ω
RS-232 Output Short-Circuit Current			±10		mA

NOTE 1. Sample tested.

DETAILED DESCRIPTION

The TC232 contains a +5V to ±10V dual charge pump voltage converter, a dual transmitter and a dual receiver.

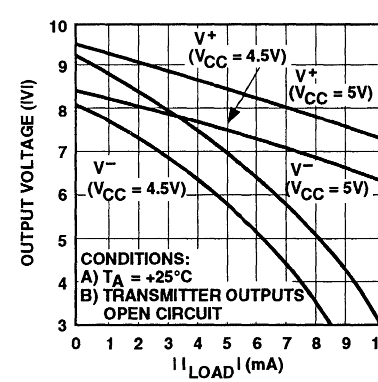
+5V to ±10V Dual Charge Pump Voltage Converter

The TC232 power supply consists of two charge pumps. One uses external capacitor C1 to double the +5V input to +10V, with output impedance of about 200Ω. The other uses C2 to invert +10V to –10V, with overall output impedance of 450Ω (including effects of +5V to +10V doubler impedance).

The clock in the doubler circuit will start at ≈4.2V in the typical part, but external loads may make this point rise to as high as 4.5V with a load of 2 kΩ on each of the two output voltages.

Because of this, use of the doubler and inverter to run external circuits should be limited. The maximum current should be no more than 2.5 mA from the +10V and –10V in order to guarantee start-up of the doubler clock.

V^+, V^- Output Voltages vs Load Current



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The test circuit employs 22 μF capacitors for C1 to C4, but the value is not critical. These capacitors usually are low-cost aluminum electrolytic capacitors, or polyester if size is critical.

Increasing C1 and C2 to 47 μF lowers the output impedance of the +10V doubler and the –10V inverter by the change in the ESR of the capacitors.

Increasing C3 and C4 lowers ripple on the ±10V voltage outputs and 16 kHz ripple on the RS-232 outputs. Where size is critical, the value of C1 to C4 can be lowered to 1 μF. The use of a low ESR-value capacitor will help lower the output ripple and keep the output impedance of the ±10V as low as possible.

Dual Transmitter

TC232 transmitters are CMOS inverters driven by ±10V internally-generated voltages. The input is TTL/CMOS compatible, with a logic threshold of about 26% of V_{CC} (1.3V for 5V V_{CC}). The input of an unused transmitter can be left unconnected. An internal 400 kΩ pull-up resistor connected between the transmitter input and V_{CC} pulls the input high and forces the unused transmitter output to the low state.

With V_{CC} at 5V, the outputs will go from (V^+–0.6V) to V^- with no load and will swing ±9V when loaded with 3 kΩ. The minimum output voltage swing, with V_{CC} at 4.5V and at maximum ambient temperature, is ±5V. This conforms to RS-232 specifications for "worst-case" conditions.

EIA RS-232C specs limit the slew rate at output to less than 30V/μs.

The powered-down output impedance (V_{CC} = 0V) is a minimum of 300Ω with ±2V applied to outputs.

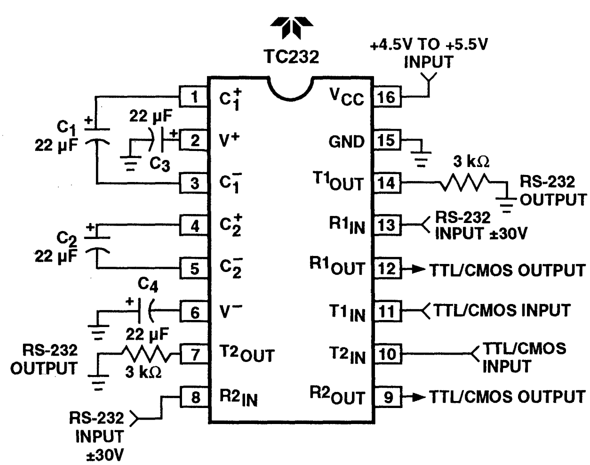
The outputs are short-circuit-protected and can be short-circuited to ground indefinitely.

Dual Receiver

TC232 receivers meet RS-232C input specifications. Input impedance is between 3 kΩ and 7 kΩ. Switching thresholds are within the ±3V limits, and the receivers withstand up to ±30V inputs. RS-232 and TTL/CMOS input compatible, the receivers have 0.8V V_{IL} and 2.4V V_{IH} with 0.5V hysteresis to reject noise.

The TTL/CMOS compatible receiver output is low when RS-232 input is greater than 2.4V. It is high when input is floating or between +0.8V and –30V.

TEST CIRCUIT



Section 14

Discrete DMOS Products

TELEDYNE COMPONENTS

2N7000
2N7002

N-CHANNEL ENHANCEMENT-MODE DMOS POWER FETS

FEATURES

- **High Gate Oxide Breakdown, ±40V min.**
- **Low Output and Transfer Capacitances**
- **Extended Safe Operating Area**

APPLICATIONS

- **High-Speed Pulse Amplifiers**
- **Logic Buffers**
- **Line Drivers**
- **Solid-State Relays**
- **Motor Controls**
- **Power Supplies**

ORDERING INFORMATION

Part No.	Package	Description
2N7000	TO-226AA (TO-92) Plastic Package	60V, 5Ω
2N7002	SOT-23 Package	60V, 5Ω

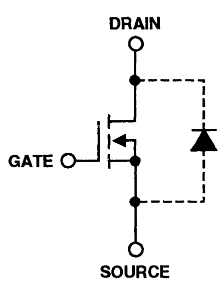
ABSOLUTE MAXIMUM RATINGS

(T_A - +25°C unless otherwise noted) (TO-92 Package)

Drain-Source Voltage .... +60V
Drain-Gate Voltage (V_{GS} = 0) .... +60V
Gate-Source Voltage .... ±40V
Continuous Drain Current
  T_A = 25°C 0.21A
  T_C = 25°C 0.32A
Peak Pulsed Drain Current 0.79A
Continuous Device Dissipation 530mW
  Linear Derating Factor .... 4.3mW/°C
Pulsed Device Dissipation 3.125W
  Linear Derating Factor .... 25mW/°C
Operating Junction
Temperature Range .... –55 to +150°C
Storage Temperature Range .... –55 to +150°C
Lead Temperature (1/16" from
mounting surface for 30 sec) .... +260°C

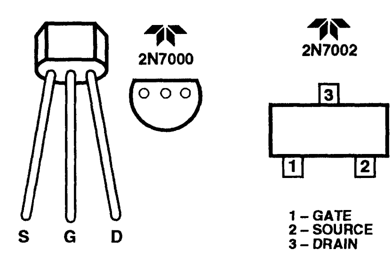
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



4353 ILL F01

PIN CONFIGURATIONS



4353 ILL F02

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2N7000
2N7002

ELECTRICAL CHARACTERISTICS: (T_C = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 10\mu A$, $V_{GS} = 0$	60	100	—	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	$I_D = 1.0mA$, $V_{DS} = V_{GS}$	0.8	1.9	3.0	V
I_{GBS}	Gate-Body Source Leakage Current	$V_{GS} = \pm 15V$, $V_{DS} = 0$	—	±1.0	±10	nA
I_{DSS}	Drain-Source OFF Leakage Current	$V_{DS} = 48V$, $V_{GS} = 0$		0.1	1.0	μA
		$V_{DS} = 48V$, $V_{GS} = 0$ $T_C = +125°C$	—	.01	1.0	mA
$I_{D(on)}$	ON Drain Current	$V_{DS} = 10V$, $V_{GS} = 4.5V^{(1)}$	75	—	—	mA
$V_{DS(on)}$	Drain-Source ON Voltage	$V_{GS} = 4.5V$, $I_D = 75mA^{(1)}$	—	—	0.4	V
		$V_{GS} = 10V$, $I_D = 0.5A^{(1)}$	—	1.5	2.5	
$r_{DS(on)}$	Drain-Source ON Resistance	$V_{GS} = 10V$, $I_D = 0.5A^{(1)}$	—	3.0	5.0	Ω
		$V_{GS} = 10V$, $I_D = 0.5A^{(1)}$ $T_C = +125°C$	—	4.7	9.0	Ω
Dynamic						
g_{fs}	Common-Source Forward Transcond	$V_{DS} = 10V$, $I_D = 0.2A$ $f = 1KHz^{(1)}$	100	360	—	mmhos
c_{iss}	Common-Source Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0$ $f = 1MHz$	—	47	60	pF
c_{rss}	Common-Source Reverse Transfer Capacitance	$V_{DS} = 25V$, $V_{GS} = 0$ $f = 1MHz$	—	3.0	5.0	pF
c_{oss}	Common-Source Output Capacitance	$V_{DS} = 25V$, $V_{GS} = 0$ $f = 1MHz$	—	15	25	pF
t_{on}	Turn-On Time	$R_G = 25\Omega$, $R_L = 25\Omega$ $V_{DD} = 15V$, $V_{G(on)} = 10V$	—	5.0	10	nSec
t_{off}	Turn-Off Time	$R_G = 25\Omega$, $R_L = 25\Omega$ $V_{DD} = 15V$, $V_{G(on)} = 10V$	—	6.0	10	nSec

Note: 1. Pulse Test 80μ Sec, 1% Duty Cycle

TELEDYNE
COMPONENTS

BS170

N-CHANNEL ENHANCEMENT-MODE DMOS POWER FET

FEATURES

- **Reliable, low cost, plastic package**
- **European TO-92 pin-out**
- **Low capacitance**

APPLICATIONS

- **High-Speed Pulse Amplifiers**
- **Logic Buffers**
- **Line Drivers**

ORDERING INFORMATION

Part No.	Package	Description
BS170	TO-92 Plastic	60V, 5Ω

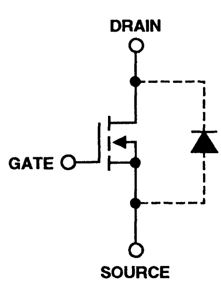
ABSOLUTE MAXIMUM RATINGS

(TC = +25°C unless otherwise specified)

Drain-Source Voltage 60V
Drain-Gate Voltage (R_{GS} 1MΩ) 60V
Gate-Source Voltage .... ±30V
Continuous Drain Current
T_C = +100°C 0.21A
T_C = +25°C 0.32A
Peak Pulsed Drain Current 1.0A
Maximum Power Dissipation
T_C = +100°C 0.9
T_C = +25°C 2.25
Linear Derating Factor
Junction to Ambient .... 4.3mW/°C
Junction to Case .... 18mW/°C
Operating Junction and
StorageTemperature Range .... –55°C to +150°C
Lead Temperature (1/6" from
mounting surface for 30 sec) .... +260°C

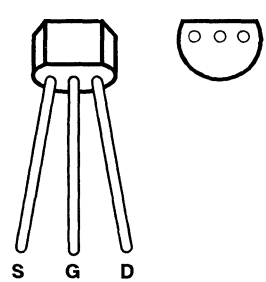
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



4354 FHD 01

PIN CONFIGURATIONS



4354 FHD 04

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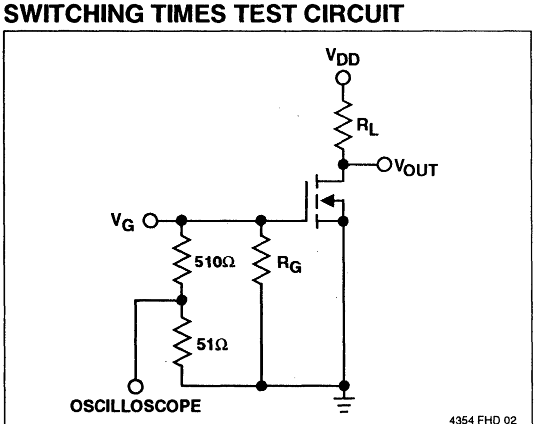
BS170

ELECTRICAL CHARACTERISTICS: (T_C = +25°C unless otherwise noted)

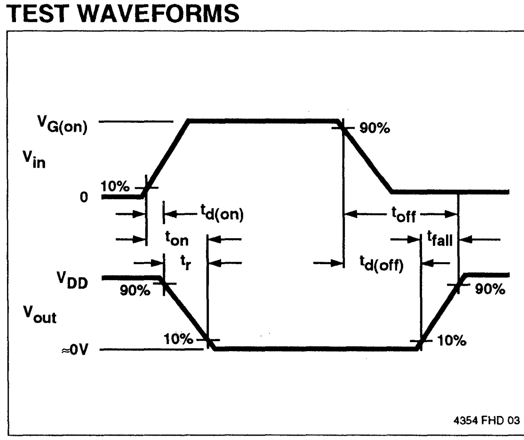
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 100µA, V_{GS} = 0	60	100	—	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 1mA	0.8	2.1	3.0	V
I_{GSSF}	Gate Body Forward Leakage Current	V_{GS} = 20V, V_{DS} = 0	—	.03	10	nA
I_{GSSR}	Gate Body Reverse Leakage Current	V_{GS} = –20V, V_{DS} = 0		–.06	–10	µA
I_{DSS}	Drain-Source OFF Leakage Current	V_{DS} = 25V, V_{GS} = 0	—	—	0.5	µA
		V_{DS} = 25V, V_{GS} = 0 T_C = +125°C	—	—	500	µA
$I_{D(ON)}$	ON Drain Current[(1)]	V_{DS} = 10V, V_{GS} = 10V	0.3	—	—	A
$r_{DS(ON)}$	Drain-Source ON Resistance[(1)]	V_{GS} = 10V, I_D = 200mA T_C = +125°C	— —	2.8 —	5.0 9.0	Ω
Dynamic						
g_{fs}	Common-Source Forward Transcond[(1)]	V_{DS} = 10V, I_D = 0.2A f = 1KHz	100	300	—	mmhos
c_{iss}	Common-Source Input Capacitance	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	—	47	60	pF
c_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	—	3.0	5.0	pF
c_{oss}	Common-Source Output Capacitance	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	—	15	25	pF
t_{on}	Turn-On Time	V_{DD} = 25V, $V_{G(ON)}$ = 10V R_L = 23Ω, R_G = 51Ω	—	—	10	nSec
t_{off}	Turn-Off Time	V_{DD} = 25V, $V_{G(ON)}$ = 10V R_L = 23Ω, R_G = 51Ω	—	—	10	nSec

NOTE: 1. Pulse test 80µ Sec, 1% duty cycle

SWITCHING TIMES TEST CIRCUIT



TEST WAVEFORMS



TELEDYNE COMPONENTS

SD1106

N-CHANNEL ENHANCEMENT-MODE DMOS POWER FETS

FEATURES

- Inherent Current Sharing Capability when Parralleled
- Simple Straight-Forward DC Biasing
- Extended Safe Operating Area
- Inherently Temperature Stable— Output Current Decreases as Temperature increases

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays

ORDERING INFORMATION

Part No.	Package	Description
SD1106DD	TO-206AA (TO-18) Package	60V min

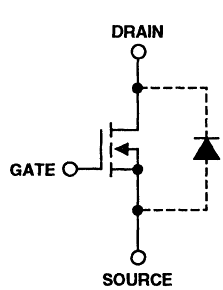
ABSOLUTE MAXIMUM RATINGS

(T_C = +25°C unless otherwise noted)

Drain-Source Voltage 60V
Drain-Gate Voltage (R_{GS} = 1MΩ) 60V
Gate-Source Voltage .... ±40V
Continuous Drain Current
T_C = +100°C 0.21A
T_C = +25°C 0.34A
Peak Pulsed Current 2.0A
Continuous Device Dissipation
T_C = +100°C 0.4W
T_C = +25°C 1.0W
Linear Derating Factor
T_C = +100°C .... 5.3mW/°C
T_C = +25°C .... 8.0mW/°C
Operating Junction and Storage Temperature Range .... –55°C to +150°C
Lead Temperature (1/16" from mounting surface for 10 sec) .... +260°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



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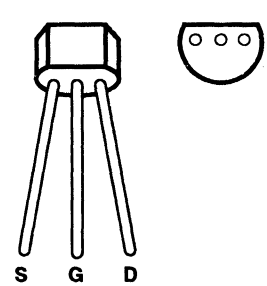
PIN CONFIGURATION



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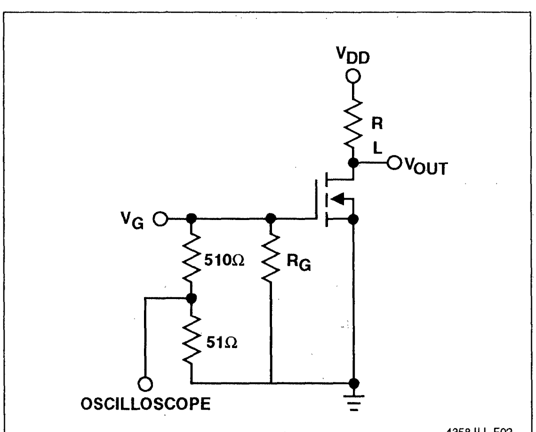
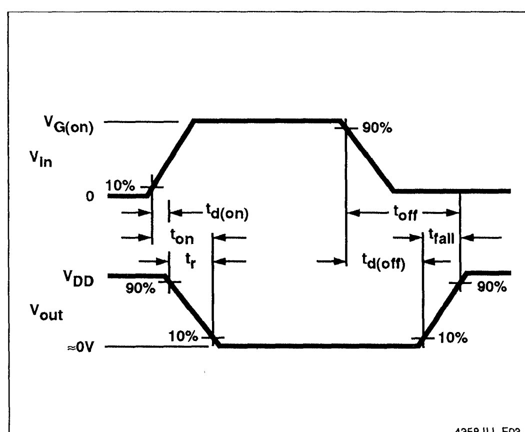
SD1106

ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 100μA, V_{GS} = 0	60	—	—	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 1mA	0.8	—	2.5	V
I_{GBS}	Gate-Body Source Leakage Current	V_{GS} = 20V, V_{DS} = 0	—	.03	10	nA
I_{DSS}	Drain-Source OFF Leakage Current	V_{DS} = 40V, V_{GS} = 0	—	.01	10	μA
$I_{D(on)}$	ON Drain Current	V_{DS} = 25V(1), V_{GS} = 5V V_{DS} = 25V(1), V_{GS} = 10V	0.25 0.50	— —	— —	A
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 10V, I_D = 0.5A(1)	—	1.8	2.5	V
Dynamic						
g_{fs}	Common-Source Forward Transcond.	V_{DS} = 15V, I_D = 0.5A f = 1KHz(1)	100	270	—	mmhos
c_{iss}	Common-Source Input Capacitance	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	—	115	150	pF
c_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	—	4	7	pF
c_{oss}	Common-Source Output Capacitance	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	—	20	35	pF
t_{on}	Turn-On Time	V_{DD} = 25V, R_L = 25Ω R_G = 51Ω, $V_{G(on)}$ = 10V	—	4.0	6.0	nSec
t_{off}	Turn-Off Time	V_{DD} = 25V, R_L = 25Ω R_G = 51Ω, $V_{G(on)}$ = 10V	—	4.0	6.0	nSec

NOTE: 1. Pulse Test 80μSec, 1% Duty Cycle





TELEDYNE COMPONENTS

SD210 SD211 SD212 SD213 SD214 SD215

N-CHANNEL ENHANCEMENT-MODE DMOS FET SWITCHES

FEATURES

- High Input to Output Isolation—120dB typical
- Low feedthrough and feedback transients
- Low Inter-electrode Capacitances

APPLICATIONS

- +30V Switch Drivers—SD210, SD211
- ±10V Analog Switches—SD214, SD215
- ±5V Analog Switches—SD212, SD213

ORDERING INFORMATION

Part No.	Package	Description
SD210DE	TO-206AF (TO-72)	10V, 70Ω
SD210DE/R	Shorting Rings	10V, 70Ω
SD211DE	TO-206AF (TO-72)	10V, 70Ω
SD211DE/R	Shorting Rings	10V, 70Ω
SD212DE	TO-206AF (TO-72)	10V, 70Ω
SD212DE/R	Shorting Rings	10V, 70Ω
SD213DE	TO-206AF (TO-72)	10V, 70Ω
SD213DE/R	Shorting Rings	10V, 70Ω
SD214DE	TO-206AF (TO-72)	20V, 70Ω
SD214DE/R	Shorting Rings	20V, 70Ω
SD215DE	TO-206AF (TO-72)	20V, 70Ω
SD215DE/R	Shorting Rings	20V, 70Ω

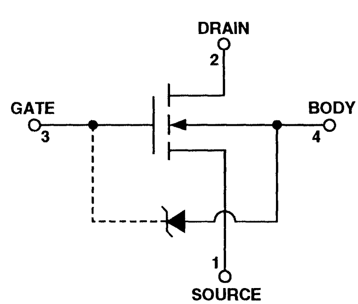
ABSOLUTE MAXIMUM RATINGS

	SD210	SD211	SD212	SD213	SD214	SD215	Unit
V_{DS}	+30	+30	+10	+10	+20	+20	Vdc
V_{SD}	+10	+10	+10	+10	+20	+20	Vdc
V_{DB}	+30	+30	+15	+15	+25	+25	Vdc
V_{SB}	+15	+15	+15	+15	+25	+25	Vdc
V_{GS}	±40	–15	±40	–15	±40	–25	Vdc
		+25		+25		+30	Vdc
V_{GB}	±40	–0.3	±40	–0.3	±40	–0.3	Vdc
		+25		+25		+30	Vdc
V_{GD}	±40	–30	±40	–15	±40	–25	Vdc
		+25		+25		+30	Vdc

I_D Continuous Drain Current 50mA
P_T Power Dissipation (at or below T_C = +25°C) 1.2W
Linear Derating Factor ....12mW/°C
P_D Power Dissipation (at or below T_A = +25°C)...300mW
Linear Derating Factor ....3.0mW/°C
T_j Operating Junction
Temperature Range ....–55 to +125°C
T_s Storage Temperature Range ....–65 to +175°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



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N-CHANNEL ENHANCEMENT-MODE DMOS FET SWITCHES

SD210 SD213
SD211 SD214
SD212 SD215

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.)

Symbol	Parameter	Test Conditions	SD210, SD211			SD212, SD213			SD214, SD215			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Static												
BV_{DS}	Drain-Source Breakdown Voltage	$I_D = 10\mu A$, $V_{GS} = V_{BS} = 0$	30	35	—	—	—	—	—	—	—	V
BV_{DS}	Drain-Source Breakdown Voltage	$I_D = 10nA$, $V_{GS} = V_{BS} = -5V$	10	25	—	10	25	—	20	25	—	V
BV_{SD}	Source-Drain Breakdown Voltage	$I_S = 10nA$ $V_{GD} = V_{BD} = -5V$	10	—	—	10	—	—	20	—	—	V
BV_{DB}	Drain-Substrate Breakdown Voltage	I_D - 10nA, V_{GB} =0 Source OPEN	15	—	—	15	—	—	25	—	—	V
BV_{SB}	Source-Substrate Breakdown Voltage	$I_S = 10\ \mu A$, $V_{GB} = 0$ Drain OPEN	15	—	—	15	—	—	25	—	—	V
$I_{D(OFF)}$	Drain-Source OFF Current	$V_{DS} = 10V$, $V_{GS} = V_{BS} = -5V$	—	—	10	—	—	10	—	—	—	nA
		$V_{DS} = 20V$, $V_{GS} = V_{BS} = -5V$	—	—	—	—	—	—	—	—	10	
$I_{S(OFF)}$	Source-Drain OFF Current	$V_{SD} = 10V$, $V_{GD} = V_{BD} = -5V$	—	—	10	—	—	10	—	—	—	nA
		$V_{SD} = 20V$, $V_{GD} = V_{BD} = -5V$	—	—	—	—	—	—	—	—	10	
I_{GBS}	Gate-Body Source Leakage Current SD210	$V_{GB} = \pm 40V$, $V_{DB} = V_{SB} = 0$	—	—	0.1	—	—	—	—	—	—	nA
	SD212	$V_{GB} = \pm 40V$, $V_{DB} = V_{SB} = 0$	—	—	—	—	—	0.1	—	—	—	nA
	SD214	$V_{GB} = \pm 40V$, $V_{DB} = V_{SB} = 0$	—	—	—	—	—	—	—	—	0.1	nA
	SD211	$V_{GB} = 25V$, $V_{DB} = V_{SB} = 0$	—	—	10	—	—	—	—	—	—	μA
	SD213	$V_{GB} = 25V$, $V_{DB} = V_{SB} = 0$	—	—	—	—	—	10	—	—	—	μA
	SD215	$V_{GB} = 30V$, $V_{DB} = V_{SB} = 0$	—	—	—	—	—	—	—	—	10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1\mu A$, $V_{SB} = 0V$	0.5	1.0	2.0	0.1	—	2.0	0.1	1.0	2.0	V
$r_{DS(on)}$	Drain-Source ON Resistance	$V_{GS} = 5V$, $I_D = 1mA$, $V_{SB} = 0V$	—	50	70	—	50	70	—	50	70	Ω
		$V_{GS} = 10V$, $I_D = 1mA$, $V_{SB} = 0V$	—	30	45	—	30	45	—	30	45	
Dynamic												
g_{fs}	Common-Source Forward Transcond.	$V_{DS} = 10V$, $I_D = 20mA$, f = 1KHz, $V_{SB} = 0$	10	12	—	10	12	—	10	12	—	mmhos
$C_{(gs+gd+gb)}$	Gate Node Capacitance	$V_{DS} = 10V$, $V_{GS} = V_{BS} = -15V$, f = 1 MHz	—	2.4	3.5	—	2.4	3.5	—	2.4	3.5	pF
$C_{(gd+db)}$	Drain Node Capacitance	$V_{DS} = 10V$, $V_{GS} = V_{BS} = -15V$, f = 1 MHz	—	1.3	1.5	—	1.3	1.5	—	1.3	1.5	pF
$C_{(gs+sb)}$	Source Node Capacitance	$V_{DS} = 10V$, $V_{GS} = V_{BS} = -15V$, f = 1 MHz	—	3.5	4.0	—	3.5	4.0	—	3.5	4.0	pF
$C_{(dg)}$	Reverse Transfer Capacitance	$V_{DS} = 10V$, $V_{GS} = V_{BS} = -15V$, f = 1 MHz	—	0.3	0.5	—	0.3	0.5	—	0.3	0.5	pF
$t_{D(on)}$	Turn ON Delay Time	$V_{DD} = 5V$, $V_{G(on)} = 10V$, $R_L = 680\Omega$, $R_G = 51\Omega$	—	0.7	1.0	—	0.7	1.0	—	0.7	1.0	nSec
t_R	Rise Time	$V_{DD} = 5V$, $V_{G(on)} = 10V$, $R_L = 680\Omega$, $R_G = 51\Omega$	—	0.8	1.0	—	0.8	1.0	—	0.8	1.0	nSec
t_{off}	Turn OFF Time	$V_{DD} = 5V$, $V_{G(on)} = 10V$, $R_L = 680\Omega$, $R_G = 51\Omega$	—	10	—	—	10	—	—	10	—	nSec

TELEDYNE COMPONENTS

SD211A
SD215A

N-CHANNEL ENHANCEMENT-MODE DMOS FET SWITCHES

FEATURES

- High Input to Output Isolation—120dB typical
- Low feedthrough and feedback transients
- Low inter-electrode Capacitances
- Low Gamma Process
- On Resistance Guaranteed in Analog Switch Configuration

APPLICATIONS

- +30V Switch Driver—SD211A
- ±10V Analog Switch—SD215A
- ±5V Analog Switch—SD211A

ORDERING INFORMATION

Part No.	Package	Description
SD211ADE	TO-206AF (TO-72) Package	BV_{SD} 10V (min.)
SD211ADE/R	Shorting Rings	BV_{SD} 10V (min.)
SD215ADE	TO-206AF (TO-72) Package	BV_{SD} 20V (min.)
SD215ADE/R	Shorting Rings	BV_{SD} 20V (min.)

ABSOLUTE MAXIMUM RATINGS

Parameter	SD211A	SD215A	Units
V_{DS}	+30	+20	V
V_{SD}	+10	+20	V
V_{DB}	+30	+25	V
V_{SB}	+15	+25	V
V_{GS}	–15	–25	V
	+25	+30	V
V_{GB}	–0.3	–0.3	V
	+25	+30	V
V_{GD}	–30	–25	V
	+25	+30	V

I_D Continuous Drain Current 50mA

P_T Power Dissipation @ or below
T_C = +25°C) 1.2W
Linear Derating Factor .... 12mW/°C

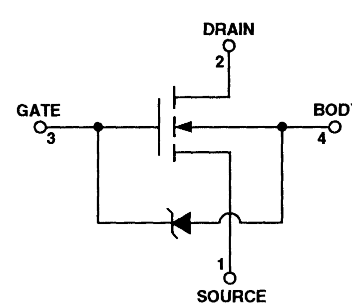
P_D Power Dissipation @ or below
T_A = +25°C 300mW
Linear Derating Factor .... 3.0mW/°C

T_j Operating Junction
Temperature Range .... –55°C to +125°C

T_s Storage Temperature
Range .... –65°C to +175°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



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SD211A
SD215A

ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	SD211A Min	SD211A Typ	SD211A Max	SD215A Min	SD215A Typ	SD215A Max	Units
Static									
BV_{DS}	Drain-Source Breakdown Voltage	$I_D = 10\mu A$, $V_{GS} = V_{BS} = 0$	30	35	—	—	—	—	V
		$I_D = 10nA$, $V_{GS} = V_{BS} = -5V$	10	25	—	20	25	—	
BV_{SD}	Source-Drain Breakdown Voltage	$I_S = 10nA$, $V_{GD} = V_{BD} = -5V$	10	—	—	20	—	—	V
BV_{DB}	Drain-Substrate Breakdown Voltage	$I_D = 10\mu A$, $V_{GB} = 0$ Source OPEN	15	—	—	25	—	—	V
BV_{SB}	Source-Substrate Breakdown Voltage	$I_S = 10\mu A$, $V_{GB} = 0$ Drain OPEN	15	—	—	25	—	—	V
$I_{D(off)}$	Drain-Source Off Current	$V_{DS} = 10V$, $V_{GS} = V_{BS} = -5V$	—	—	10	—	—	—	nA
		$V_{DS} = 20V$, $V_{GS} = V_{BS} = -5V$	—	—	—	—	—	10	
$I_{S(off)}$	Source-Drain Off Current	$V_{SD} = 10V$, $V_{GD} = V_{BD} = -5V$	—	—	10	—	—	—	nA
		$V_{SD} = 20V$, $V_{GD} = V_{BD} = -5V$	—	—	—	—	—	10	
I_{GBS}	Gate-Body Source Leakage Current	$V_{GB} = 25V$, $V_{DB} = V_{SB} = 0$	—	—	10	—	—	—	µA
		$V_{GB} = 30V$, $V_{DB} = V_{SB} = 0$	—	—	—	—	—	10	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1.0\mu A$, $V_{SB} = 0$	0.75	1.0	1.5	0.75	1.0	1.5	V
$r_{DS(on)}$	Drain-Source ON Resistance	$V_{GS} = 4.5V$, $I_D = 1mA$ $V_{SB} = 5V$	—	—	90	—	—	—	Ω
		$V_{GS} = 4.5V$, $I_D = 1mA$ $V_{SB} = 10V$	—	—	—	—	—	90	
		$V_{GS} = 10V$, $I_D = 1mA$ V_{SB} -=0	—	30	45	—	30	45	
Dynamic									
g_{fs}	Common-Source Forward Transcond.	$V_{DS} = 10V$, $I_D = 20mA$ f = 1KHz, $V_{SB} = 0$	10	13	—	10	13	—	mmhos
$C_{(gs+gd+gb)}$	Gate Node Capacitance	$V_{DS} = 10V$, f = 1MHz $V_{GS} = V_{BS} = -15V$	—	2.4	3.5	—	2.4	3.5	pF
$C_{(gd+db)}$	Drain Node Capacitance	$V_{DS} = 10V$, f = 1MHz $V_{GS} = V_{BS} = -15V$	—	1.3	1.5	—	1.3	1.5	pF
$C_{(gs+sb)}$	Source Node Capacitance	$V_{DS} = 10V$, f = 1MHz $V_{GS} = V_{BS} = -15V$	—	3.5	4.0	—	3.5	4.0	pF
C_{dg}	Reverse Transfer Capacitance	$V_{DS} = 10V$, f = 1MHz $V_{GS} = V_{BS} = -15V$	—	0.3	0.5	—	0.3	0.5	pF
$T_{D(on)}$	Turn ON Delay Time	$V_{DD} = 5V$, $V_{G(on)} = 10V$, $R_L = 680\Omega$, $R_G = 51\Omega$	—	0.7	1.0	—	0.7	1.0	nSec
t_r	Rise Time	$V_{DD} = 5V$, $V_{G(on)} = 10V$, $R_L = 680\Omega$, $R_G = 51\Omega$	—	0.8	1.0	—	0.8	1.0	nSec
t_{off}	Turn OFF Time	$V_{DD} = 5V$, $V_{G(on)} = 10V$, $R_L = 680\Omega$, $R_G = 51\Omega$	—	10	—	—	10	—	nSec

TELEDYNE COMPONENTS

SD304
SD306

N-CHANNEL ENHANCEMENT-MODE DUAL GATE DMOS FET

FEATURES

- **Normally Off-Enhancement-Mode Operation**
- **Dual Gate with Gate Protective Diodes**
- **Low Feedback Capacitance—c_{rss} .03pF (typ)**
- **Wide Dynamic Range-Remote AGC Capability**
- **High Power Gain—17dB min. @ 500MHz (SD306)**
- **Low Noise—6.0dB max. @ 500MHz (SD306)**
- **Low Cross-Modulation Distortion**

APPLICATIONS

- **Wide Band (Unneutralized) VHF/UHF Amplifiers**
- **VHF/UHF Linear Mixers**

ORDERING INFORMATION

Part No.	Package	Description
SD304DE	TO-206AF (TO-72) Package	25V, 130Ω
SD306DE	TO-206AF (TO-72) Package	20V, 100Ω

ABSOLUTE MAXIMUM RATINGS

V_{DS} Drain-Source Voltage
- SD304 .... +25V
- SD306 .... +20V

V_{G1B} Gate 1-Substrate Voltage
- SD304 .... –0.3 to +10V
- SD306 .... –0.3 to +20V

V_{G2B} Gate 2-Substrate Voltage
- SD304 .... –0.3 to +15V
- SD306 .... –0.3 to +20V

I_D Continuous Drain Current (Note 1) 50mA

P_D Continuous Power Dissipation (Note 1)
- T_A = +25°C (Free Air) 300mW
- T_C = +25°C (Infinite Heat Sink) 1.2W
- Power Derating Factors (Note 1)
- Free Air .... 3.0mW/°C
- Infinite Heat Sink .... 12mW/°C

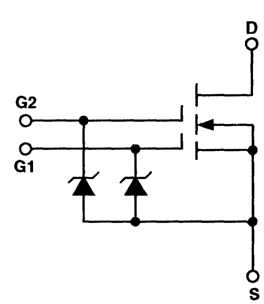
T_{op} Operating Junction Temperature Range .... –55 to +125°C

T_{stg} Storage Temperature Range .... –65 to +175°C

NOTE: 1. Not applicable to chips. Final value depends mounting substrate.

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



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SD304
SD306

ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	SD304 Min	SD304 Typ	SD304 Max	SD306 Min	SD306 Typ	SD306 Max	Units
Static									
BV_{DS}	Drain-Source Breakdown Voltage	$I_D = 5\mu A$, $V_{G1S} = V_{G2S} = 0$	25	30	—	20	25	—	V
I_{DSS}	Drain-Source OFF Leakage Current	$V_{DS} = 15V$ $V_{G1S} = V_{G2S} = 0$	—	.01	1.0	—	.01	1.0	µA
I_{G1SS}	Gate 1 Leakage Current	$V_{G1S} = 5V$ $V_{G2S} = V_{DS} = 0$	—	1.0	100	—	1.0	100	nA
I_{G2SS}	Gate 2 Leakage Current	$V_{G2S} = 10V$, $V_{G1S} = V_{DS} = 0$	—	1.0	100	—	1.0	100	nA
V_{T1}	Gate 1-Source Threshold Voltage	$V_{DS} = V_{G1S}$, $V_{G2S} = 10V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
V_{T2}	Gate 2-Source Threshold Voltage	$V_{G1S} = 4V$, $V_{DS} = V_{G2S}$ $I_D = 1\mu A$	0.1	1.0	2.0	—	—	—	V
		$V_{G1S} = 5V$, $V_{DS} = V_{G2S}$ $I_D = 1\mu A$	—	—	—	0.1	0.5	1.5	V
$r_{DS(on)}$	Drain-Source ON Resistance	$I_D = 1mA$, $V_{G1S} = 5V$ $V_{G2S} = 10V$	—	90	130	—	65	100	Ω
Dynamic									
g_{fs}	Common-Source Forward Transcond.	$V_{DS} = 15V$, $I_D = 18mA$ $V_{G2S} = 10V$, f = 1KHz	8.0	10	—	13	15	—	mmhos
c_{iss}	Common-Source Input Capacitance	$V_{DS} = 15V$, $I_D = 18mA$ $V_{G2S} = 10V$, f = 1MHz	—	2.5	3.0	—	3.3	3.6	pF
c_{oss}	Common-Source Output Capacitance	$V_{DS} = 15V$, $V_{G1S} = 0$ $V_{G2S} = 10V$, F = 1MHz	—	1.0	1.2	—	1.0	1.3	pF
c_{rss}	Common-Source Reverse Transfer Capacitance	$V_{DS} = 15V$, $V_{G1S} = 0$ $V_{G2S} = 10V$, F = 1MHz	—	.03	—	—	.03	—	pF
$Re_{(Y11)}$	Input Admittance	$V_{DS} = 15V$, ID = 18mA, $V_{G2S} = 10V$, f = 200MHz	—	—	—	—	1.11	—	mmhos
$Im_{(Y11)}$	Input Admittance	$V_{DS} = 15V$, ID = 18mA, $V_{G2S} = 10V$, f = 200MHz	—	—	—	—	4.76	—	mmhos

N-CHANNEL ENHANCEMENT-MODE DUAL GATE DMOS FET

SD304 SD306

ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	SD304 Min	SD304 Typ	SD304 Max	SD306 Min	SD306 Typ	SD306 Max	Units
Re(Y22)	Output Admittance	V_{DS} = 15V, I_D = 18mA V_{G2S} = 10V, f = 200MHz	—	—	—	—	1.05	—	mmhos
IM (Y22)	Output Admittance	V_{DS} = 15V, I_D = 18mA V_{G2S} = 10V, f = 200MHz	—	—	—	—	1.54	—	mmhos
Re (Y21)	Forward Transmittance	V_{DS} = 15V, I_D = 18mA V_{G2S} = 10V, f = 200MHz	—	—	—	—	13.23	—	mmhos
Im (Y21)	Forward Transmittance	V_{DS} = 15V, I_D = 18mA V_{G2S} = 10V, f = 200MHz	—	—	—	—	–5.62	—	mmhos
Re (Y12)	Reverse Transmittance	V_{DS} = 15V, I_D = 18mA V_{G2S} = 10V, f = 200MHz	—	—	—	—	0.01	—	mmhos
Im (Y12)	Reverse Transmittance	V_{DS} = 15V, I_D = 18mA V_{G2S} = 10V, f = 200MHz	—	—	—	—	–0.04	—	mmhos
G_{ps}	Power Gain	f = 500MHz, I_D = 18mA V_{DS} = 15V, V_{G2S} = 10V	13	16	—	—	—	—	dB
		f = 200MHz, I_D = 18mA V_{DS} = 15V, V_{G2S} = 10V	—	—	—	17	20	—	
NF	Noise Figure	f = 500MHz, I_D = 18mA V_{DS} = 15V, V_{G2S} = 10V	—	5.0	6.0	—	—	—	dB
		f = 200MHz, I_D = 18ma V_{DS} = 15V, V_{G2S} = 10V	—	—	—	—	1.5	2.5	
AGC(V_{G2S})	Range of Automatic Gain Control	$V_{G1S} \cong$ 3.5V, f = 500MHz V_{DS} = 15V, V_{G2S} = 10V to 0V	—	40	—	—	—	—	dB
		$V_{G1S} \cong$ 2.5V, f = 200MHz V_{DS} = 15V, V_{G2S} = 10V to 0V	—	—	—	—	50	—	
E_{INT}	Interfering Signal at Gate for 1% Cross-Modulation Distortion (Peak Voltage ref. to 50 ohm system)	fo = 500MHz, I_D = 18mA V_{DS} = 15V, V_{G2S} = 10V f = 501MHz	—	200	—	—	—	—	mV
		fo = 200MHz, I_D = 18mA V_{DS} = 15V, V_{G2S} = 10V f = 196MHz	—	—	—	—	480	—	
G_{psc}	Conversion Power Gain (I_D = 8mA)	V_{DS} = 15V, V_{G1S} = V_{G2S} f = 200MHz f = 245MHz	—	—	—	14	17	—	dB

NOTES

TELEDYNE COMPONENTS

SD5000
SD5001
SD5002

N-CHANNEL ENHANCEMENT-MODE QUAD DMOS FET ANALOG SWITCH ARRAYS

FEATURES

- **High Input to Output Isolation—120dB typical**
- **Low feedthrough and feedback transients**
- **Low Inter-electrode Capacitances**

APPLICATIONS

- **±10V Analog Switches—SD5000**
- **±5V Analog Switches—SD5001**
- **±7.5V Analog Switches—SD5002**
- **Sample and Hold**
- **Wide-Band, Dual Differential Amplifiers**

ORDERING INFORMATION

Part No.	Package	Description
SD5000J	16-Pin Ceramic Dual In-Line	20V, 70Ω
SDSD5001J	16-Pin Ceramic Dual In-Line	10V, 70Ω
SD5002J	16-Pin Ceramic Dual In-Line	15V, 70Ω
SD5000N	16-Pin Plastic Dual In-Line	20V, 70Ω
SD5001N	16-Pin Plastic Dual In-Line	10V, 70Ω
SD5002N	16-Pin Plastic Dual In-Line	15V, 70Ω

ABSOLUTE MAXIMUM RATINGS

	SD5000	SD5001	SD5002	Unit
V_{DS}	+20	+10	+15	Vdc
V_{SD}	+20	+10	+15	Vdc
V_{DB}	+25	+15	+22.5	Vdc
V_{SB}	+25	+15	+22.5	Vdc
V_{GS}	–25	–15	–22.5	Vdc
	+30	+25	+30	Vdc
V_{GB}	–0.3	–0.3	–0.3	Vdc
	+30	+25	+30	Vdc
V_{GD}	–25	–15	–22.5	Vdc
	+30	+25	+30	Vdc

I_D Continuous Drain Current 50mA

P_D Total Package Power Dissipation (at or below T_A = +25°C) 640mW
Linear Derating Factor ....10.67mW/°C

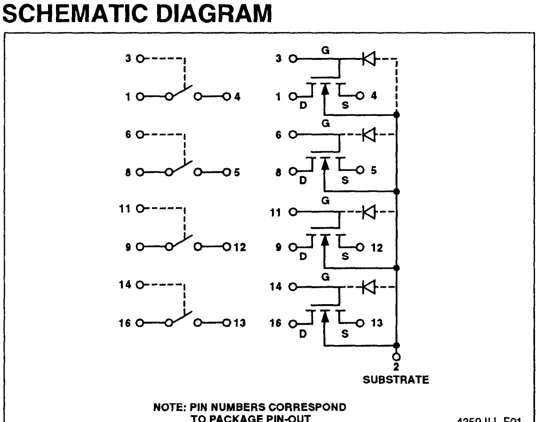
P_D Single Device Power Dissipation (at or below T_A = +25°C) 300mW

T_j Operating Junction Temperature Range ....–55 to +85°C

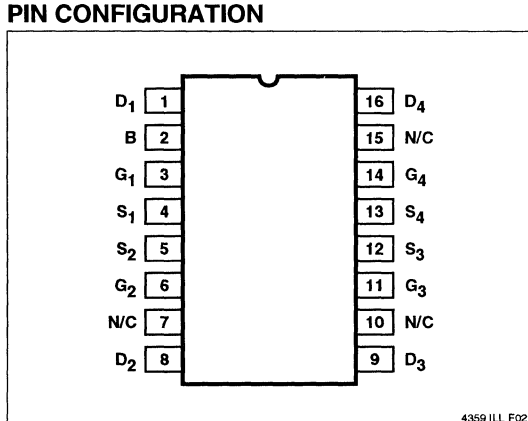
T_s Storage Temperature Range ....–55 to +150°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



PIN CONFIGURATION



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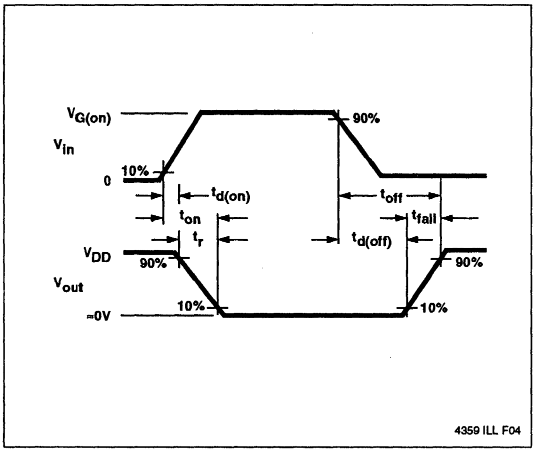
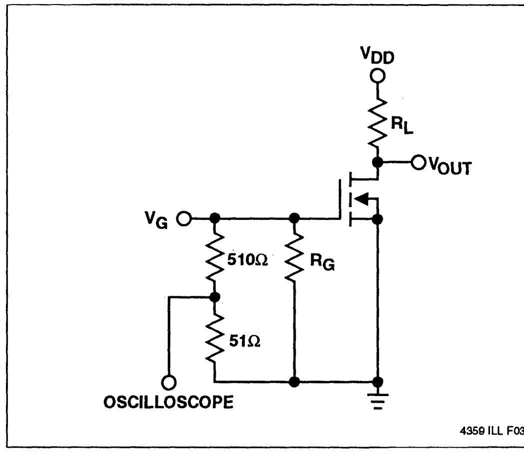
TEST WAVEFORMS



SWITCHING TIMES TEST CIRCUIT



N-CHANNEL ENHANCEMENT-MODE QUAD DMOS FET ANALOG SWITCH ARRAYS

SD5000
SD5001
SD5002

ELECTRICAL CHARACTERISTICS: (T_A = +25°C per channel, unless otherwise noted.)

			SD5000			SD5001			SD5002			
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Static												
BV_{DS}	Drain-Source Breakdown Voltage	I_D = 10 nA, $V_{GS} = V_{BS}$ = –5V	20	25	—	10	25	—	15	25	—	V
BV_{SD}	Source-Drain Breakdown Voltage	I_S = 10 nA $V_{GD} = V_{BD}$ = –5V	20	—	—	10	—	—	15	—	—	V
BV_{DB}	Drain-Substrate Breakdown Voltage	I_D = 10nA, V_{GB} =0 Source Open	25	—	—	15	—	—	22.5	—	—	V
BV_{SB}	Source-Substrate Breakdown Voltage	I_S = 10 µA, V_{GB} = 0 Drain Open	25	—	—	15	—	—	22.5	—	—	V
$I_{D(off)}$	Drain-Source Off Current	V_{DS} = 10V, $V_{GS} = V_{BS}$ = –5V	—	—	—	—	—	10	—	—	—	nA
		V_{DS} = 15V, $V_{GS} = V_{BS}$ = –5V	—	—	—	—	—	—	—	—	10	
		V_{DS} = 20V, $V_{GS} = V_{BS}$ = –5V	—	—	10	—	—	—	—	—	—	
$I_{S(off)}$	Source-Drain Off Current	V_{SD} = 10V, $V_{GD} = V_{BD}$ = –5V	—	—	—	—	—	10	—	—	—	nA
		V_{SD} = 15V, $V_{GD} = V_{BD}$ = –5V	—	—	—	—	—	—	—	—	10	
		V_{SD} = 20V, $V_{GD} = V_{BD}$ = –5V	—	—	10	—	—	—	—	—	—	
I_{GBS}	Gate-Body Source Leakage Current	V_{GB} = 25V, $V_{DB} = V_{SB}$ = 0	—	—	—	—	—	1.0	—	—	—	µA
		V_{GB} = 30V, $V_{DB} = V_{SB}$ = 0	—	—	1.0	—	—	—	—	—	1.0	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 1 µA, V_{SB} = 0	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
$r_{DS(on)}$	Drain-Source ON Resistance	V_{GS} = 5V, I_D = 1mA, V_{SB} = 0	—	50	70	—	50	70	—	50	70	Ω
		V_{GS} = 10V, I_D = 1mA, V_{SB} = 0	—	30	—	—	30	—	—	30	—	
		V_{GS} = 15V, I_D = 1mA, V_{SB} = 0	—	23	—	—	23	—	—	23	—	
		V_{GS} = 20V, I_D = 1mA, V_{SB} = 0	—	19	—	—	19	—	—	19	—	
r_{DSM}	ON Resistance Match	V_{GS} = 5V, I_D = 1mA, V_{SB} = 0	—	1.0	5.0	—	1.0	5.0	—	1.0	5.0	Ω
Dynamic												
g_{fs}	Common-Source Forward Transcond	V_{DS} = 10V, I_D = 20mA, f = 1KHz, V_{SB} = 0	10	12	—	10	12	—	10	12	—	mmhos
$C_{(gs+gd+gb)}$	Gate Node Capacitance	V_{DS} = 10V, $V_{GS} = V_{BS}$ = –15V, f = 1 MHz	—	2.4	3.5	—	2.4	3.5	—	2.4	3.5	pF
$C_{(gs+db)}$	Drain Node Capacitance	V_{DS} = 10V, $V_{GS} = V_{BS}$ = –15V, f = 1 MHz	—	1.3	1.5	—	1.3	1.5	—	1.3	1.5	pF
$C_{(gs+sb)}$	Source Node Capacitance	V_{DS} = 10V, $V_{GS} = V_{BS}$ = –15V, f = 1 MHz	—	3.5	4.0	—	3.5	4.0	—	3.5	4.0	pF
$C_{(dg)}$	Reverse Transfer Capacitance	V_{DS} = 10V, $V_{GS} = V_{BS}$ = –15V, f = 1 MHz	—	0.3	0.5	—	0.3	0.5	—	0.3	0.5	pF
C_T	Cross Talk	f = 3KHz, R_G = 600Ω	—	–107	—	—	–107	—	—	–107	—	dB
$t_{d(on)}$	Turn ON Delay Time	V_{DD} = 5V, $V_{G(on)}$ = 10V, R_L = 680Ω, R_G = 51Ω	—	0.7	1.0	—	0.7	1.0	—	0.7	1.0	nSec
t_r	Rise Time	V_{DD} = 5V, $V_{G(on)}$ = 10V, R_L = 680Ω, R_G = 51Ω	—	0.8	1.0	—	0.8	1.0	—	0.8	1.0	nSec
t_{off}	Turn OFF Time	V_{DD} = 5V, $V_{G(on)}$ = 10V, R_L = 680Ω, R_G = 51Ω	—	10	—	—	10	—	—	10	—	nSec

NOTES

TELEDYNE COMPONENTS

SD5100
SD5101

N-CHANNEL ENHANCEMENT-MODE QUAD DMOS FET ANALOG SWITCH ARRAYS

FEATURES

- Common source for 4 channels
- Low feedthrough and feedback transients
- Low Inter-electrode Capacitances

APPLICATIONS

- +30V Switch Drivers—SD5100
- +15V Switch Drivers—SD5101

ORDERING INFORMATION

Part No.	Package	Description
SD5100N	14-Pin Plastic Dual In-Line	30V, 70Ω
SD5101N	14-Pin Plastic Dual In-Line	15V, 70Ω
SD5100CY	SO-14 Package	30V, 70Ω
SD5101CY	SO-14 Package	15V, 70Ω

ABSOLUTE MAXIMUM RATINGS

Parameter	SD5100	SD5101	Unit
V_{DS}	+30	+15	Vdc
V_{SD}	+0.5	+0.5	Vdc
V_{DB}	+30	+15	Vdc
V_{SB}	+0.5	+0.5	Vdc
V_{GS}	+20	+20	Vdc
V_{GB}	+20	+20	Vdc
	–0.3	–0.3	Vdc
V_{GD}	+20	+20	Vdc
	–30	–15	Vdc

I_D Continuous Drain Current 50mA

P_D Total Package Power Dissipation (at or below T_A = +25°C) 640mW

Linear Derating Factor ....10.67mW/°C

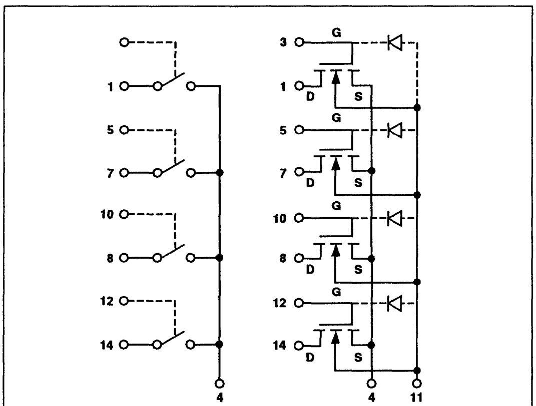
P_D Single Device Power Dissipation at or below TA = +25°C) 300mW

T_j Operating Junction Temperature Range ....–55 to +85°C

T_s Storage Temperature Range ....–55 to +150°C

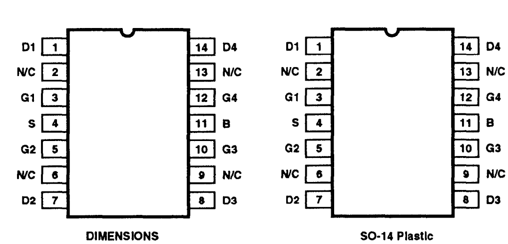
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pin-Out 4360 ILL F01

PIN CONFIGURATION



4360 ILL F02

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SD5100
SD5101

ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	SD5100			SD5101			Units
			Min	Typ	Max	Min	Typ	Max	
Static									
BV_{DS}	Drain-Source Breakdown Voltage	I_D = 1.0μA, $V_{GS} = V_{BS}$ = 0	30	35	—	15	30	—	V
BV_{SD}	Source-Drain Breakdown Voltage	I_S = 10nA, $V_{GD} = V_{BD}$ = 0	0.5	—	—	0.5	—	—	V
BV_{DB}	Drain-Substrate Breakdown Voltage	I_D - 1.0μA, V_{GB} = 0 Source Open	30	—	—	15	—	—	V
BV_{SB}	Source-Substrate Breakdown Voltage	I_S = 100nA, V_{GB} = 0 Drain Open	0.5	—	—	0.5	—	—	V
$I_{D(off)}$	Drain-Source OFF Current	V_{DS} = 10V, $V_{GS} = V_{BS}$ = 0	—	1.0	10	—	1.0	10	nA
I_{GBS}	Gate-Substrate Source Leakage Current	V_{GS} = 20V, $V_{DB} = V_{SB}$ = 0	—	—	10	—	—	10	μA
$V_{GS(th)}$	Gate-Source Threshold Voltage	I_D = 1.0μA, $V_{DS} = V_{GS}$ V_{SB} = 0	0.5	1.0	2.0	0.5	1.0	2.0	V
$r_{DS(on)}$	Drain-Source ON Resistance	V_{GS} = 5V, I_D = 1mA V_{SB} = 0	—	50	70	—	50	70	Ω
		V_{GS} = 10V, I_D = 1mA V_{SB} = 0	—	30	45	—	30	45	
		V_{GS} = 15V, I_D = 1mA V_{SB} = 0	—	23	—	—	23	—	
		V_{GS} = 20V, I_D = 1mA V_{SB} = 0	—	19	—	—	19	—	
r_{DSM}	ON Resistance Match	VGS = 5V, I_D = 1mA, V_{SB} = 0	—	1.0	5.0	—	1.0	5.0	Ω
Dynamic									
g_{fs}	Common-Source Forward Transcond	V_{DS} = 10V, I_D = 20mA f = 1KHz, V_{SB} = 0	10	15	—	10	15	—	mmhos
$c_{(gs+gd+gb)}$	Gate Node Capacitance	V_{DS} = 10V, f = 1MHz $V_{GS} = V_{BS}$ = –5V	—	2.4	3.5	—	2.4	3.5	pF
$c_{(gd+db)}$	Drain Node Capacitance	V_{DS} = 10V, f = 1MHz $V_{GS} = V_{BS}$ = –5V	—	1.3	1.5	—	1.3	1.5	pF
c_{dg}	Reverse Transfer Capacitance	V_{DS} = 10V, f = 1MHz $V_{GS} = V_{BS}$ = –5V	—	0.3	0.5	—	0.3	0.5	pF
C_T	Cross Talk	f = 3KHz, R_G = 600Ω	—	–107	—	—	–107	—	dB

NOTE: 1. Pulse Test 80μ Sec, 1% Duty Cycle

N-CHANNEL ENHANCEMENT-MODE QUAD DMOS FET DRIVER ARRAY

FEATURES

- **Normally OFF Configuration**
- **Low Interelectrode Capacitance**
- **High-speed Switching**

APPLICATIONS

- **+30V Analog Switch Drivers**
- **Wide-Band Dual Differential Amplifiers**

ORDERING INFORMATION

Part No.	Package	Description
SD5200N	16-Pin Plastic Dual In-Line	30V, 80Ω

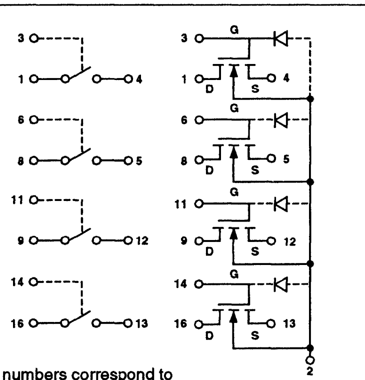
ABSOLUTE MAXIMUM RATINGS

(per channel, T_A = +25°C unless otherwise noted)

V_{DS}	Drain-Source Voltage	+30Vdc
V_{SD}	Source-Drain Voltage	+0.5Vdc
V_{DB}	Drain-Body Voltage	+30Vdc
V_{SB}	Source-Body Voltage	+15Vdc
V_{GS}	Gate-Source Voltage	+25Vdc
V_{GB}	Gate-Body Voltage	+25Vdc
	Gate-Body Voltage	–0.3Vdc
V_{GD}	Gate-Drain Voltage	+25Vdc, –30Vdc
I_D	Continuous Drain Current	50mA
P_D	Total Package Power Dissipation (at or below T_A = +25°C)	640mW
	Linear Derating Factor	10.7mW/°C
P_D	Single Device Power Dissipation (at or below T_A = +25°C)	300mW
	Linear Derating Factor	5.0mW/°C
Tj	Operating Junction Temperature Range	–55 to +85°C
T_S	Storage Temperature Range	–55 to +150°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

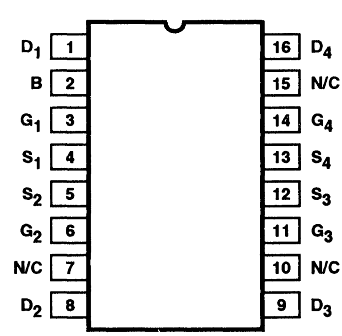
SCHEMATIC DIAGRAM



Note: Pin numbers correspond to Package Pinout

4370 ILL F01

PIN CONFIGURATION



4370 ILL F02

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SD5200

ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Static						
BV_{DS}	Drain-Source Breakdown Voltage	$I_D = 10\mu A$, $V_{GS} = V_{BS} = 0$	30	35	—	V
BV_{SB}	Source-Substrate Breakdown Voltage	$I_S = 10\mu A$, $V_{GB} = 0$ Drain Open	15	—	—	V
I_{GBS}	Gate-Body Leakage Current	$V_{GB} = 25V$, $V_{DB} = V_{SB} = 0$	—	—	1.0	µA
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1.0\mu A$ $V_{SB} = 0$	0.5	1.0	2.0	V
$r_{DS(on)}$	Drain-Source ON Resistance	$V_{GS} = 5V$, $I_D = 1mA$, $V_{SB} = 0$	—	50	80	Ω
		$V_{GS} = 10V$, $I_D = 1mA$, $V_{SB} = 0$	—	30	—	
		$V_{GS} = 15V$, $I_D = 1mA$, $V_{SB} = 0$	—	23	—	
		$V_{GS} = 20V$, $I_D = 1mA$, $V_{SB} = 0$	—	19	—	
DYNAMIC						
g_{fs}	Common-Source Forward Transcond.	$V_{DS} = 10V$, $I_D = 20mA$ $f = 1KHz$, $V_{SB} = 0$	10	12	—	mmhos
$c_{(gs+gd+gb)}$	Gate Node Capacitance	$f = 1MHz$, $V_{DS} = 10V$ $V_{GS} = V_{BS} = -15V$	—	2.4	3.5	pF
$c_{(gd+db)}$	Drain Node Capicitance	$f = 1MHz$, $V_{DS} = 10V$ $V_{GS} = V_{BS} = -15V$	—	1.3	1.5	pF
$c_{(gs+sb)}$	Source Node Capacitance	$f = 1MHz$, $V_{DS} = 10V$ $V_{GS} = V_{BS} = -15V$	—	3.5	4.0	pF
$c_{(dg)}$	Reverse Transfer Capacitance	$f = 1MHz$, $V_{DS} = 10V$ $V_{GS} = V_{BS} = -15V$	—	0.3	0.5	pF
C_T	Cross Talk		—	−107	—	dB

TELEDYNE COMPONENTS

SD5400
SD5401
SD5402

QUAD DMOS FET ANALOG SWITCH ARRAYS

FEATURES

- Low Interelectrode Capacitances
  - — Analog Input .... 3.5 pF Typ
  - — Input (Gate) .... 2.4 pF Typ
  - — Output .... 1.3 pF Typ
  - — Feedback .... 0.3 pF Typ
- Low Insertion Loss .... r_{DS} <30Ω
- Low Cross Talk .... 107 dB @ 3 kHz
- Bidirectional Switches
- Small-Outline, Surface-Mount Package

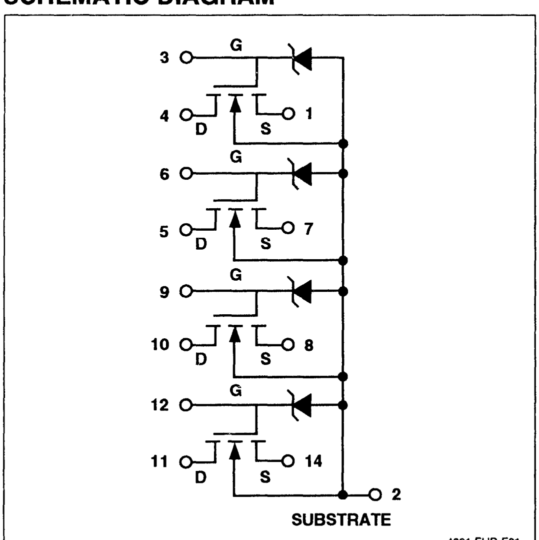
ORDERING INFORMATION

Part No.	Package	Description	Temperature Range
SD5400CY	14-Pin Plastic Small-Outline	20V, 30Ω	Commercial
SD5401CY	14-Pin Plastic Small-Outline	10V, 30Ω	Commercial
SD5402CY	14-Pin Plastic Small-Outline	15V, 30Ω	Commercial

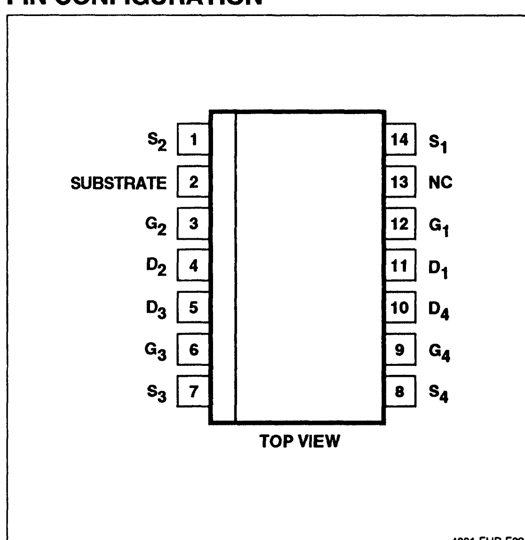
APPLICATIONS

- High-Speed Analog Switches
  - SD5400 .... ±10V
  - SD5401 .... ±5V
  - SD5402 .... ±7.5V
- High-Speed Switch Drivers
  - SD5400 .... 20V
  - SD5401 .... 10V
  - SD5402 .... 15V
- Sample-and-Hold

SCHEMATIC DIAGRAM



PIN CONFIGURATION



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QUAD DMOS FET ANALOG SWITCH ARRAYS

SD5400
SD5401
SD5402

ABSOLUTE MAXIMUM RATINGS:

T_C = +25°C, unless otherwise noted.

V_{DB} Drain-Body Voltage
- SD5400 .... +25V
- SD5401 .... +15V
- SD5402 .... +22.5V

V_{DS} Drain-Source Voltage
- SD5400 .... +20V
- SD5401 .... +10V
- SD5402 .... +15V

V_{SB} Source-Body Voltage
- SD5400 .... +25V
- SD5401 .... +15V
- SD5402 .... +22.5V

V_{SD} Source-Drain Voltage
- SD5400 .... +20V
- SD5401 .... +10V
- SD5402 .... +15V

V_{GB} Gate-Body Voltage
- SD5400 .... −0.3V, +30V
- SD5401 .... −0.3V, +25V
- SD5402 .... −0.3V, +30V

V_{GD} Gate-Drain Voltage
- SD5400 .... −25V, +30V
- SD5401 .... −15V, +25V
- SD5402 .... −22.5V, +30V

V_{GS} Gate-Source Voltage
- SD5400 .... −25V, +30V
- SD5401 .... −15V, +25V
- SD5402 .... −22.5V, +30V

I_D Continuous Drain Current .... 50 mA

P_D Total Package Power Dissipation
- @ or Below T_A = +25°C .... 640 mW
- Linear Derating Factor .... 5.33 mW/°C

P_D Single Device Power Dissipation
- @ or Below T_A = +25°C .... 300 mW

T_J Operating Junction
- Temperature Range .... 0°C to +70°C

T_{STG} Storage Temperature Range .... −55°C to +125°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

QUAD DMOS FET ANALOG SWITCH ARRAYS

SD5400 SD5401 SD5402

ELECTRICAL CHARACTERISTICS (T_A = +25°C per channel, unless otherwise noted.)

Symbol	Parameter	Test Conditions	SD5400			SD5401			SD5402			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Static												
BV_{DS}	Drain-Source Breakdown Voltage	I_D = 10 nA, $V_{GS} = V_{BS}$ = –5V	20	25	—	10	25	—	15	25	—	V
BV_{SD}	Source-Drain Breakdown Voltage	I_S = 10 nA, $V_{GD} = V_{BD}$ = –5V	20	—	—	10	—	—	15	—	—	V
BV_{DB}	Drain-Substrate Breakdown Voltage	I_D = 10 nA, V_{GB} = 0V, Source OPEN	25	—	—	15	—	—	22.5	—	—	V
BV_{SB}	Source-Substrate Breakdown Voltage	I_S = 10 µA, V_{GB} = 0V, Drain OPEN	25	—	—	15	—	—	22.5	—	—	V
$I_{D(OFF)}$	Drain-Source OFF Current	$V_{GS} = V_{BS}$ = –5V, V_{DS} = 10V $V_{GS} = V_{BS}$ = –5V, V_{DS} = 15V $V_{GS} = V_{BS}$ = –5V, V_{DS} = 20V	— — —	— — —	— — 10	— — —	— — —	10 — —	— — —	— — —	— 10 —	nA
$I_{S(OFF)}$	Source-Drain OFF Current	$V_{GD} = V_{BD}$ = –5V, V_{SD} = 10V $V_{GD} = V_{BD}$ = –5V, V_{SD} = 15V $V_{GD} = V_{BD}$ = –5V, V_{SD} = 20V	— — —	— — —	— — 10	— — —	— — —	10 — —	— — —	— — —	— 10 —	nA
I_{GBS}	Gate-Body Source Leakage Current	$V_{DB} = V_{SB}$ = 0V, V_{GB} = 25V $V_{DB} = V_{SB}$ = 0V, V_{GB} = 30V	— —	— —	— 1	— —	— —	1 —	— —	— —	— 1	µA
$V_{GS(TH)}$	Gate Source Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 1 µA, V_{SB} = 0V	0.1	1	2	0.1	1	2	0.1	1	2	V
$r_{DS(ON)}$	Drain-Source ON Resistance	V_{GS} = 5V, I_D = 1 mA, V_{SB} = 0V	—	50	70	—	50	70	—	50	70	Ω
		V_{GS} = 10V, I_D = 1 mA, V_{SB} = 0V	—	30	—	—	30	—	—	30	—	Ω
		V_{GS} = 15V, I_D = 1 mA, V_{SB} = 0V	—	23	—	—	23	—	—	23	—	Ω
		V_{GS} = 20V, I_D = 1 mA, V_{SB} = 0V	—	19	—	—	19	—	—	19	—	Ω
$r_{DSM(ON)}$	Drain-Source Match ON Resistance	V_{GS} = 5V, I_D = 1 mA, V_{SB} = 0V	—	1	5	—	1	5	—	1	5	Ω
Dynamic												
$g_{m\,(FS)}$	Common-Source Forward Transconductance	V_{DS} = 10V, I_D = 20 mA, V_{SB} = 0 f = 1 kHz	10	12	—	10	12	—	10	12	—	mmhos
$C_{(GS+GD+GB)}$	Gate Node Capacitance	V_{DS} = 10V, $V_{GS} = V_{BS}$ = –15V, f = 1 MHz	—	2.4	3.5	—	2.4	3.5	—	2.4	3.5	pF
$C_{(GS+DB)}$	Drain Node Capacitance	V_{DS} = 10V, $V_{GS} = V_{BS}$ = –15V, f = 1 MHz	—	1.3	1.5	—	1.3	1.5	—	1.3	1.5	pF
$C_{(GS+SB)}$	Source Node Capacitance	V_{DS} = 10V, $V_{GS} = V_{BS}$ = –15V, f = 1 MHz	—	3.5	4	—	3.5	4	—	3.5	4	pF
$C_{(DG)}$	Reverse Transfer Capacitance	V_{DS} = 10V, $V_{GS} = V_{BS}$ = –15V, f = 1 MHz	—	0.3	0.5	—	0.3	0.5	—	0.3	0.5	pF
CT	Cross-Talk	f = 3 kHz, R_G = 600Ω	—	–107	—	—	–107	—	—	–107	—	dB
$t_{D(ON)}$	Turn ON Delay Time	V_{DD} = 5V, $V_{G(ON)}$ = 10V, R_L = 680Ω, R_G = 51Ω	—	0.7	1	—	0.7	1	—	0.7	1	ns
t_R	Rise Time	V_{DD} = 5V, $V_{G(ON)}$ = 10V, R_L = 680Ω, R_G = 51Ω	—	0.8	1	—	0.8	1	—	0.8	1	ns
t_{OFF}	Turn OFF Time	V_{DD} = 5V, $V_{G(ON)}$ = 10V, R_L = 680Ω, R_G = 51Ω	—	10	—	—	10	—	—	10	—	ns

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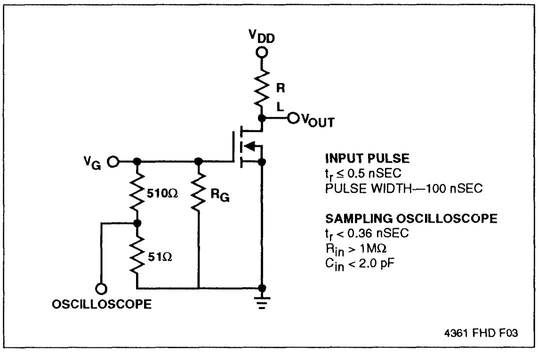
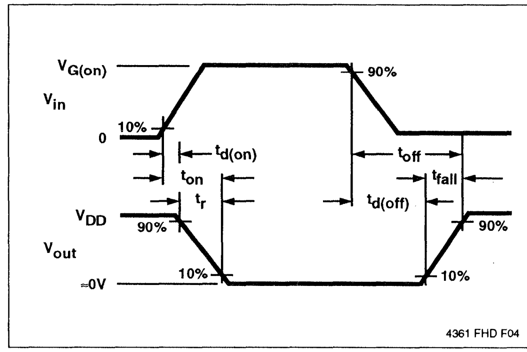
SWITCHING TIMES TEST CIRCUIT

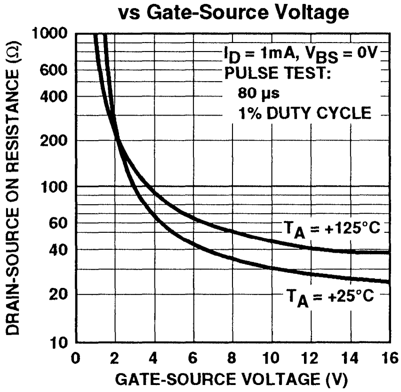


TEST WAVEFORMS

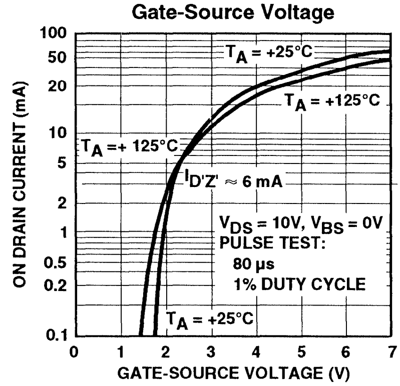


TYPICAL PERFORMANCE CHARACTERISTICS: T_A = +25°C per channel, unless otherwise noted.

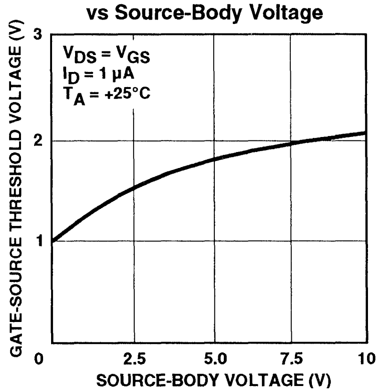
Drain-Source On Resistance vs Gate-Source Voltage



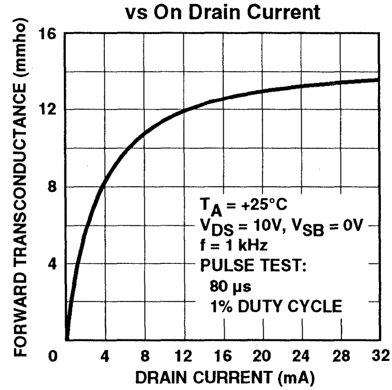
On Drain Current vs Gate-Source Voltage



Gate-Source Threshold Voltage vs Source-Body Voltage



Forward Transconductance vs On Drain Current



TELEDYNE COMPONENTS

VN0610LL
VN2222LL

N-CHANNEL ENHANCEMENT-MODE DMOS POWER FETs

FEATURES

- **High Gate Oxide Breakdown, ±40V min.**
- **Low Output and Transfer Capacitances**
- **Extended Safe Operating Area**

APPLICATIONS

- **High-Speed Pulse Amplifiers**
- **Logic Buffers**
- **Line Drivers**
- **Solid-State Relays**
- **Motor Controls**
- **Power Supplies**

ORDERING INFORMATION

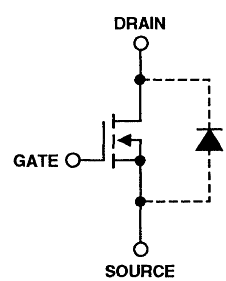
Part No.	Package	Description
VN0610LL	TO-92 Plastic Package	60V, 5Ω
VN2222LL	TO-92 Plastic Package	60V, 7.5Ω

ABSOLUTE MAXIMUM RATINGS

Drain-Source Voltage .... +60V
Drain-Gate Voltage (V_{GS} = 0) .... +60V
Gate-Source Voltage .... ±40V
Continuous Drain Current
VN0610LL
T_A = +25°C 0.18A
T_C = +25°C 0.32A
VN2222LL
T_A = +25°C 0.15A
T_C = +25°C 0.26A
Peak Pulsed Drain Current 1.0A
Continuous Device Dissipation
T_A = +25°C 0.3W
T_C = +25°C 1.0W
Linear Derating Factor
T_A = +25°C .... 2.4mW/°C
T_C = +25°C .... 8.0mW/°C
Operating Junction
Temperature Range .... –55 to +150°C
Storage Temperature Range .... –55 to +150°C
Lead Temperature (1/16" from mounting
surface for 30 sec) .... +260°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



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VN0610LL
VN2222LL

ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	VN0610LL Min	VN0610LL Typ	VN0610LL Max	VN2222LL Min	VN2222LL Typ	VN2222LL Max	Units
Static									
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 100μA, V_{GS} = 0	60	100	—	60	100	—	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	I_D = 1.0mA, V_{DS} = V_{GS}	0.8	1.9	2.5	0.6	1.9	2.5	V
I_{GBS}	Gate-Body Source Leakage Current	V_{GS} = ±30V, V_{DS} = 0	—	±1.0	±100	—	±1.0	±100	nA
I_{DSS}	Drain-Source OFF Leakage Current	V_{DS} = 48V, V_{GS} = 0	—	0.1	10	—	0.1	10	μA
		V_{DS} = 48V, V_{GS} = 0 T_A = 125°C	—	5.0	500	—	5.0	500	μA
$I_{D(on)}$	ON Drain Current	V_{DS} = 10V, V_{GS} = 10V(1)	1.0	2.2	—	1.0	2.2	—	A
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 5V, I_D = 0.2A(1) V_{GS} = 10V, I_D = 0.5A(1)	— —	0.9 1.5	1.5 2.5	— —	0.9 1.5	1.5 3.75	V
$r_{DS(on)}$	Drain-Source ON Resistance	V_{GS} = 5V, I_D = 0.2A(1) V_{GS} = 10V, I_D = 0.5A(1) V_{GS} = 10V, I_D = 0.5A(1) T_A = +125°C	— — —	4.5 3.0 4.7	7.5 5.0 9.0	— — —	4.5 3.0 4.7	7.5 7.5 13.5	Ω
Dynamic									
g_{fs}	Common-Source Forward Transcond	V_{DS} = 10V, I_D = 0.5A f = 1KHz(1)	100	400	—	100	400	—	mmhos
c_{iss}	Common-Source Input Capacitance	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	—	80	100	—	80	100	pF
c_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	—	1.3	5.0	—	1.3	5.0	pF
c_{oss}	Common-Source Output Capacitance	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	—	10.5	25	—	10.5	25	pF
t_{on}	Turn-On Time	V_{DD} = 15V, $V_{G(on)}$ = 10V R_G = 25Ω, R_L = 25Ω	—	5.0	10	—	5.0	10	nSec
t_{off}	Turn-Off Time	V_{DD} = 15V, $V_{G(on)}$ = 10V R_G = 25Ω, R_L = 25Ω	—	6.0	10	—	6.0	10	nSec

NOTE: 1. Pulse Test 80μ Sec, 1% Duty Cycle

TELEDYNE COMPONENTS

N-CHANNEL ENHANCEMENT-MODE DMOS POWER FETS

FEATURES

- High Gate Oxide Breakdown, ±40V min.
- Low Output and Transfer Capacitances
- Extended Safe Operating Area

APPLICATIONS

- High-Speed Pulse Amplifiers
- Logic Buffers
- Line Drivers
- Solid-State Relays
- Motor Controls
- Power Supplies

ORDERING INFORMATION

Part No.	Package	Description
VN10KN3	TO-92 Plastic	60V, 5Ω

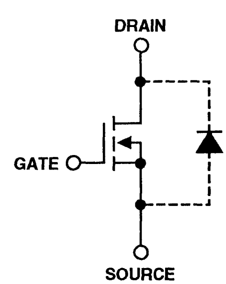
ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

Drain-Source Voltage .... +60V
Drain-Gate Voltage (V_{GS} = 0) .... +60V
Gate-Source Voltage .... ±30V
Continuous Drain Current
T_A = +25°C 0.24A
T_C = +25°C 0.32A
Peak Pulsed Drain Current 1.0A
Continuous Device Dissipation
T_A = +25°C 0.30W
T_C = +25°C 1.0W
Linear Derating Factor
T_A = +25°C .... 2.4mW/°C
T_C = +25°C .... 8.0mW/°C
Operating Junction Temperature
Range .... –55 to +150°C
Storage Temperature Range .... –55 to +150°C
Lead Temperature (1/16" from mounting
surface for 30 sec) .... +260°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



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VN10KN

ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 100μA, V_{GS} = 0	60	100	—	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	I_D = 1.0mA, V_{DS} = V_{GS}	0.8	1.9	2.5	V
I_{GBS}	Gate-Body Source Leakage Current	V_{GS} = ±15V, V_{DS} = 0	—	±10	±100	nA
I_{DSS}	Drain-Source OFF Leakage Current	V_{DS} = 40V, V_{GS} = 0	—	0.1	10	μA
		V_{DS} = 40V, V_{GS} = 0 T_A = 125°C	—	5.0	500	μA
$I_{D(on)}$	ON Drain Current	V_{GS} = 5V, V_{DS} = 10V(1) V_{GS} = 10V, V_{DS} = 10V(1)	0.25 0.75	— —	— —	A
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 10V, I_D = 0.5A(1)	—	1.5	2.5	V
$r_{DS(on)}$	Drain-Source ON Resistance	V_{GS} = 10V, I_D = 0.5A(1) V_{GS} = 10V, I_D = 0.5A(1) T_A = +125°C	— —	3.0 4.7	5.0 9.0	Ω
Dynamic						
g_{fs}	Common-Source Forward Transcond	V_{DS} = 10V, I_D = 0.5A f = 1KHz(1)	100	400	—	mmhos
c_{iss}	Common-Source Input Capacitance	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	—	80	100	pF
c_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	—	1.3	5.0	pF
c_{oss}	Common-Source Output Capacitance	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	—	10.5	25	pF
t_{on}	Turn-On Time	V_{DD} = $V_{G(on)}$ = 10V R_G = 25Ω, R_L = 25Ω	—	5.0	10	nSec
t_{off}	Turn-Off Time	V_{DD} = $V_{G(on)}$ = 10V R_G = 25Ω, R_L = 25Ω	—	6.0	10	nSec

NOTE: 1. Pulse Test 80μ Sec, 1% Duty Cycle

TELEDYNE COMPONENTS

VN10LM
VN2222LM

N-CHANNEL ENHANCEMENT-MODE DMOS POWER FETs

FEATURES

- **High Gate Oxide Breakdown, ±40V min.**
- **Low Output and Transfer Capacitances**
- **Extended Safe Operating Area**

APPLICATIONS

- **High-Speed Pulse Amplifiers**
- **Logic Buffers**
- **Line Drivers**
- **Solid-State Relays**
- **Motor Controls**
- **Power Supplies**

ORDERING INFORMATION

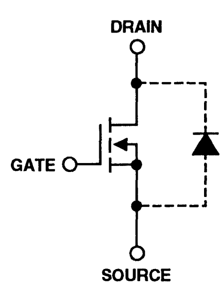
Part No.	Package	Description
VN10LM	TO-237 Plastic	60V, 5Ω
VN2222LM	TO-237 Plastic	60V, 7.5Ω

ABSOLUTE MAXIMUM RATINGS

Drain-Source Voltage .... +60V
Drain-Gate Voltage (V_{GS} = 0) .... +60V
Gate Source Voltage .... ±40
Continuous Drain Current
  VN10LM
  T_A = +25°C 0.19A
  T_C = +25°C 0.44A
  VN2222LM
  T_A = +25°C 0.16A
  T_C = +25°C 0.36A
Peak Pulsed Drain Current 1.0A
Continuous Device Dissipation
  T_A = +25°C 0.36W
  T_C = +25°C 1.8W
Linear Derating Factor
  T_A = 25°C .... 2.9mW/°C
  T_C = 25°C .... 14.4mW/°C
Operating Junction Temperature
Range .... –55 to +150°C
Storage Temperature Range .... –55 to +150°C
Lead Temperature (1/16" from mounting
surface for 30 sec) .... +260°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM



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VN10LM
VN2222LM

ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	VN10LM Min	VN10LM Typ	VN10LM Max	VN2222LM Min	VN2222LM Typ	VN2222LM Max	Units
Static									
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 100µA, V_{GS} = 0	60	100	—	60	100	—	V
$V_{GS(th)}$	Gate-Source	I_D = 1.0mA, V_{DS} = V_{GS}	0.8	1.9	2.5	0.6	1.9	2.5	V
I_{GBS}	Gate-Body Source Leakage Current	V_{GS} = ±30V, V_{DS} = 0	—	±1.0	±100	—	±1.0	±100	nA
I_{DSS}	Drain-Source OFF Leakage Current	V_{DS} = 48V, V_{GS} = 0	—	0.1	10	—	0.1	10	µA
		V_{DS} = 48V, V_{GS} = 0 T_A = 125°C	—	5.0	500	—	5.0	500	µA
$I_{D(on)}$	ON Drain Current	V_{DS} = 10V, V_{GS} = 10V(1)	1.0	2.2	—	1.0	2.2	—	A
$V_{DS(on)}$	Drain-Source ON Voltage	V_{GS} = 5V, I_D = 0.2A(1) V_{GS} = 10V, I_D = 0.5A(1)	— —	0.9 1.5	1.5 2.5	— —	0.9 1.5	1.5 3.75	V
$r_{DS(on)}$	Drain-Source ON Resistance	V_{GS} = 5V, I_D = 0.2A(1) V_{GS} = 10V, I_D = 0.5A(1) V_{GS} = 10V, I_D = 0.5A(1) T_A = +125°C	— — —	4.5 3.0 4.7	7.5 5.0 9.0	— — —	4.5 3.0 4.7	7.5 7.5 13.5	Ω
Dynamic									
g_{fs}	Common-Source Forward Transcond	V_{DS} = 10V, I_D = 0.5A f = 1KHz(1)	100	400	—	100	400	—	mmhos
c_{iss}	Common-Source Input Capacitance	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	—	80	100	—	80	100	pF
c_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	—	1.3	5.0	—	1.3	5.0	pF
c_{oss}	Common-Source Output Capacitance	V_{DS} = 15V, V_{GS} = 0 f = 1MHz	—	10.5	25	—	10.5	25	pF
t_{on}	Turn-On Time	V_{DD} = 15V, $V_{G(on)}$ = 10V R_G = 25Ω, R_L = 25Ω	—	5.0	10	—	5.0	10	nSec
t_{off}	Turn-Off Time	V_{DD} = 15V, $V_{G(on)}$ = 10V R_G = 25Ω, R_L = 25Ω	—	6.0	10	—	6.0	10	nSec

NOTES: 1. Pulse Test 80µ Sec, 1% Duty Cycle

TELEDYNE COMPONENTS

VQ1000

N-CHANNEL ENHANCEMENT-MODE QUAD DMOS POWER FET ARRAY

FEATURES

- **Inherent Current Sharing Capability when Paralleled**
- **Simple Straightforward DC Biasing**
- **Extended Safe Operating Area**
- **CMOS and TTL Compatible**

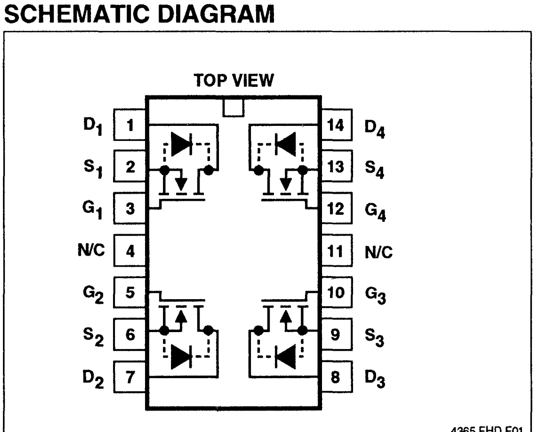
APPLICATIONS

- **High-Speed Pulse Amplifiers**
- **CMOS Logic to High-Current Interfaces**
- **High-Speed Switching**
- **Line Drivers**
- **Stepper Motor Drivers**

ORDERING INFORMATION

Part No.	Package	Description
VQ1000J	14 Pin Plastic DIP	60V, 5.5Ω

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C, unless otherwise noted.)

Drain-Source Voltage 60V
Drain-Gate Voltage (V_{GS} = 0) 60V
Gate-Source Voltage .... ±40V
Continuous Drain Current
  Total Package
  T_A = +25°C 0.29A
  T_C = +25°C 0.51A
  Single Device
  T_A = +25°C 0.20A
  T_C = +25°C 0.36A
Peak Pulsed Drain Current 1.0A
Continuous Device Dissipation
  Total Package
  T_A = +25°C 0.64W
  T_C = +25°C 2.0W
  Single Device
  T_A = +25°C 0.30W
  T_C = +25°C 1.0W
Linear Derating Factor
  Total Package
  T_A = +25°C .... 5.1mW/°C
  T_C = +25°C .... 16mW/°C
  Single Device
  T_A = +25°C .... 2.4mW/°C
  T_C = +25°C .... 8.0mW/°C
Operating Junction
Temperature Range .... –55 to +150°C
Storage Temperature Range .... –55 to +150°C
Lead Temperature (1/16" from mounting surface for 30 Sec) .... +260°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

VQ1000

ELECTRICAL CHARACTERISTICS: (T_A = +25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 100μA, V_{GS} = 0	60	105	—	V
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 1.0mA	0.8	1.9	2.5	V
I_{GBS}	Gate-Body Source Leakage Current	V_{GS} = 10V, V_{DS} = 0	—	.10	100	nA
		V_{GS} = 10V, V_{DS} = 0 T_A = +125°C	—	10	500	nA
		V_{GS} = −10V, V_{DS} = 0	—	−.10	−100	
I_{DSS}	Drain-Source OFF Leakage Current	V_{DS} = 60V, V_{GS} = 0	—	.10	10	μA
		V_{DS} = 60V, V_{GS} = 0 T_A = +125°C	—	10	500	μA
$I_{D(on)}$	Drain-Source ON Current(1)	V_{DS} = 10V, V_{GS} = 5V V_{DS} = 10V, V_{GS} = 10V	0.2 0.5	1.3 2.5	— —	A
$V_{DS(on)}$	Drain-Source ON Voltage(1)	V_{GS} = 5V, I_D = 0.2A V_{GS} = 10V, I_D = 0.3A	— —	— —	1.50 1.65	V
$r_{DS(on)}$	Drain-Source ON Resistance(1)	V_{GS} = 5V, I_D = 0.2A	—	—	7.5	Ω
		V_{GS} = 10V, I_D = 0.3A	—	—	5.5	
		V_{GS} = 10V, I_D = 0.3A T_A = + 125°C	—	—	7.6	Ω
Dynamic						
g_{fs}	Common-Source Forward Transcond(1)	V_{DS} = 10V, I_D = 0.5A f = 1KHz	100	400	—	mmhos
c_{iss}	Common-Source Input Capacitance	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	—	—	60	pF
c_{rss}	Common-Source Reverse Transfer Capacitance	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	—	—	5.0	pF
c_{oss}	Common-Source Output Capacitance	V_{DS} = 25V, V_{GS} = 0 f = 1MHz	—	—	25	pF
t_{on}	Turn-On Time	V_{DD} = 15V, $V_{G(on)}$ 10V R_G = 25Ω, R_L = 25Ω	—	—	10	nSec
t_{off}	Turn-Off Time	V_{DD} = 15V, $V_{G(on)}$ 10V R_G = 25Ω, R_L = 25Ω	—	—	10	nSec

NOTES: 1. Pulse Test 80μ Sec, 1% Duty Cycle

Section 15

Reliability and Quality Assurance

RELIABILITY AND QUALITY ASSURANCE

Teledyne Components continually strives to improve the quality and reliability of our products. This on-going process encompasses all areas of our operation, from design and development through delivery of finished product and customer service. As a result, we are proud of our many years of proven success supplying reliable high performance components to our customers.

New Product Qualification Tests

All products in development must pass a minimum set of die and package related qualification tests as a requirement for their release to manufacturing. As an example, Table 1 summarizes the reliability tests that are performed on new plastic packaged IC's. Samples from three separate fabrication lots must pass each test before production is allowed to begin.

Manufacturing Quality Assurance

The quality and reliability tests and controls in the manufacturing process (see Figure 1) are described below.

Incoming Inspection

Raw materials (silicon wafers, photomasks, leadframes, molding compound, etc.) are inspected by Quality Control on a sample basis. In some cases, where the vendor has an approved SPC program in place, vendor data may be substituted for incoming inspection at Teledyne Components. All raw material vendors are subject to periodic audits by Teledyne Components Quality personnel.

Wafer Fab

In addition to production controls, critical dimension measurements, and electrical measurements of wafers in process, Quality Assurance personnel conduct audits and monitors to assure adherence to specifications.

Wafer Sort

Each die on every wafer is tested on automatic test equipment to the electrical limits in the data sheet. Quality Assurance conducts periodic audits to assure that proper test programs and procedures are being used and that all test equipment is properly calibrated.

Assembly

Sample inspections are performed by Quality Control personnel after die attach, lead bond, and tin plate (for devices with plated leads).

Assembly Environmental

Periodic samples are tested by Quality Assurance for marking permanency, solderability, resistance to solder heat, temperature cycle and thermal shock. Also tested, for hermetic devices, are hermeticity and constant acceleration, and for plastic devices, are resistance to steam (pressure cooker) and high temperature biased humidity life (85°C/85%RH).

Electrical Test

After assembly, devices are 100% tested to the room temperature DC specifications in the data sheet. Following 100% test, lots are submitted to Quality Assurance for sample testing to all data sheet specifications (DC & AC) over the operating temperature range.

Final Visual and Clearance

Prior to shipping, the devices are inspected by Quality Assurance to Teledyne Components' visual criteria and all paperwork is checked to assure that all manufacturing steps were properly completed and that devices meet the customer's requirements.

Hi-Rel Screening

Teledyne Components offers a number of Monolithic IC and Hybrid products with extra screening for applications that require higher assurance levels of quality and reliability, similar to those demanded for military grade devices*. This "/HR" screening flow, created in 1991, is outlined in Figure 2.

* The similarity between our internal specification numbers and MIL-STD-883 test method numbers (e.g. TC2010 for internal visual) is intentional and was meant as an aid to understanding our new flow. The procedures, despite the similarity in numbers, are not intended to be identical to or in conformance with the test methods contained in MIL-STD-883.

RELIABILITY AND QUALITY ASSURANCE

RELIABILITY QUALIFICATION TESTS

Test	Conditions
Steady State Life	Ta = 125°C t = 1000Hrs.
High Temperature Storage	Ta = 150°C t = 1000Hrs.
Temperature, Humidity, Bias	Ta = 85°C, RH = 85% t = 1000Hrs.
Temperature Cycle	T-high = 150°C T-low = –65°C # of cycles =1000
Thermal Shock	T-high = 150°C T-low = –55°C # of cycles =15
Resistance to Solder Heat	Per JEDEC Std 22
Autoclave	Ta = 121°C t = 168 Hrs.
ESD Sensitivity	Per Mil-Std 883 Method 3015

Table 1

PRODUCT ASSURANCE FLOW

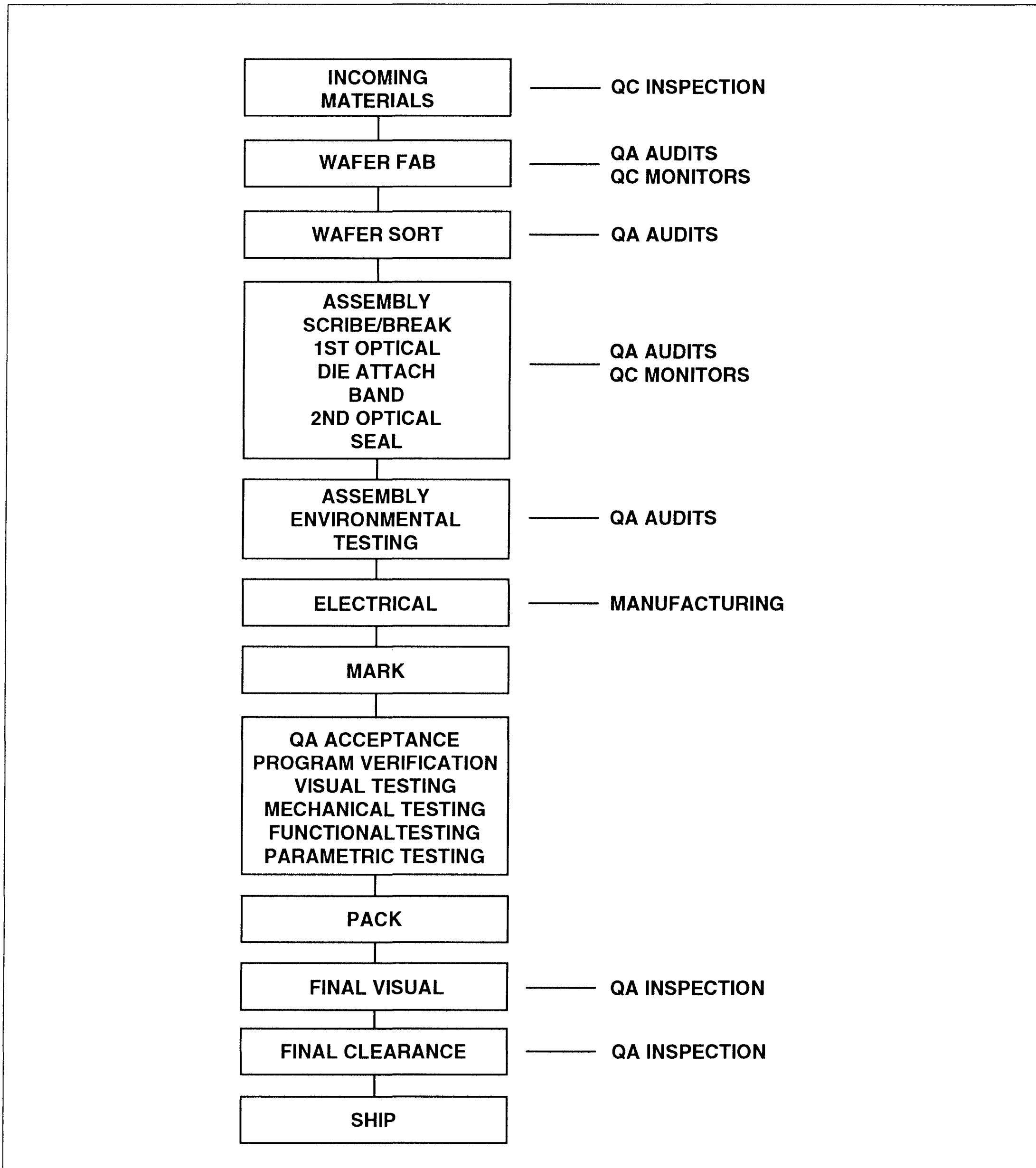


Figure 1

MONOLITHIC I.C. PRODUCTS/HR SCREENING FLOW

Traceability to Wafer Fab

Internal Visual
TC 2010*, Condition B

Temperature Cycle
TC1010*, Condition C

Constant Acceleration
TC 2001*, Condition E

Initial (Pre-Burn-In) **Electrical**
per Applicable Device Specification

Burn-In Test
TC 1015*, Condition A, B, or C

Interim (Post Burn-In) **Electrical**
per Applicable Device Specification
DC @ 25°C
Percent Defective (PDA) 5%

Final Electrical
per Applicable Device Specification
DC @ -55°C and +125°C
AC @ 25°C

Solder Dip (100%)**

Hermeticity
Fine Leak, Condition A1
Gross Leak, Condition C
TC 1014*

Device Marking
Teledyne Logo, Part Number,
ESD Designator, Date Code,
Country of Origin

External Visual
TC 2009*

Quality Conformance Inspection
TC 5005*
Group A and B, Each Lot
per Applicable Device Specification
Group C and D every 12 months

*** Teledyne Components Internal Procedure**
**** Except Gold Plated Leads**

Figure 2A

HYBRID PRODUCTS/HR SCREENING FLOW

Traceability to Elements
IC's, Capacitors, Resistors, Cover,Package
Substrate, Wire, Epoxy

Internal Visual, Hybrid Construction
TC 2017*, Class B
Internal Visual, Elements
TC 2032*, Class B
Internal Visual, Integrated Circuits
TC 2010*, Condition B

Temperature Cycle
TC1010*, Condition C

Constant Acceleration
TC 2001*, Condition A

Hermeticity
Fine Leak, Condition A1
Gross Leak, Condition C, TC 1014*

Initial (Pre-Burn-In) **Electrical**
per Applicable Device Specification

Burn-In Test
TC1015*, Condition A, B, or C

Interim (Post Burn-In) **Electrical**
per Applicable Device Specification
DC @ 25°C, Percent Defective (PDA) 10%
/Pattern Failure

Final Electrical
per Applicable Device Specification
DC @ –55°C and +125°C, AC @ 25°C

Device Marking
Teledyne Logo, Part Number,
ESD Designator, Date Code,
Country of Origin, BeO

External Visual
TC 2009*

Quality Conformance Inspection
TC 5008*
Group A and B, Each Lot
per Applicable Device Specification
Group C once per design or major
change, Group D per package
type every 6 months

*** Teledyne Components Internal Procedure**

Figure 2B

NOTES

Section 16

Ordering Information

ORDERING INFORMATION

TELEDYNE COMPONENTS INTEGRATED CIRCUIT PRODUCT NUMBERING SYSTEM (except High Noise Immunity Products)

Teledyne Components Device

Device Number

Electrical Performance Grade Option (if applicable)
R — Reversed Pin Layout

Operating Temperature Range

Package Type

Number of Package Pins

Processing Option
HRX — HR Flow, Class B Processing
BI — 100% Burn-In at TC = 125°C ±5°C for 160 Hours

TC 7106 A C P L /HRX

Number of Package Pins (see listing)

Package Type (see listing)

Operating Temperature Range
M — Military Temperature Range (–55°C to +125°C)
I* — Industrial Temperature Range (–25°C to +85°C)
C — Commercial Temperature Range (0°C to +70°C)
E — Extended Industrial Temperature Range (–40°C to +85°C)
* — May be –40°C to +85°C.
Refer to specific device specification.

See data sheet for electrical grade options.

Note that all proprietary part number prefixes have been changed to 'TC'.

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ORDERING INFORMATION

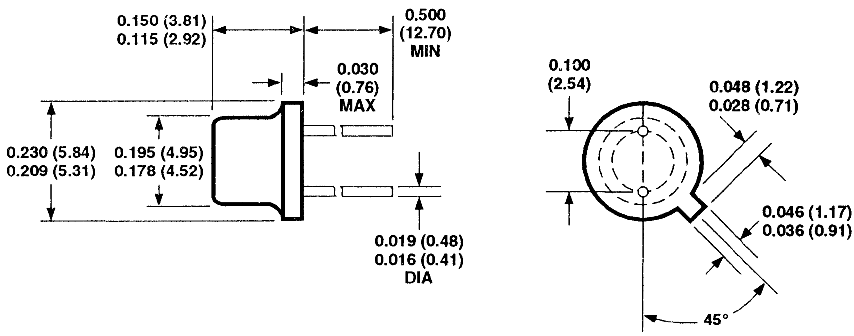
Package Type		Number of Package Pins	
A	TO-220	**A**	8
B	Plastic Flat Pack	**B**	3
C	SOT-23	**C**	3 (Pin 2 connected to case)
D	MO-078AA	**D**	14
H	Side-Brazed CerDIP	**E**	16
I	TO-220 (Isolated)	**G**	24
J	CerDIP	**I**	28
K	Plastic Gullwing Quad Flat Package	**L**	40
L	Plastic Leaded Chip Carrier (PLCC)	**M**	2
M	SOT-89	**N**	18
N	Ceramic Leadless Chip Carrier (LCC)	**P**	20
O	Plastic 'SO' Surface Mount	**Q**	60
P	Plastic DIP	**R**	5 (Pin 3 connected to case)
R	TO-52	**S**	68
T	TO-99	**T**	5
V	8-Pin Metal Can	**V**	8 (Pin 8 connected to case)
Y	Dice	**W**	44
Z	TO-92	**Y**	8 (Pin 4 connected to case)

Section 17

Package Information

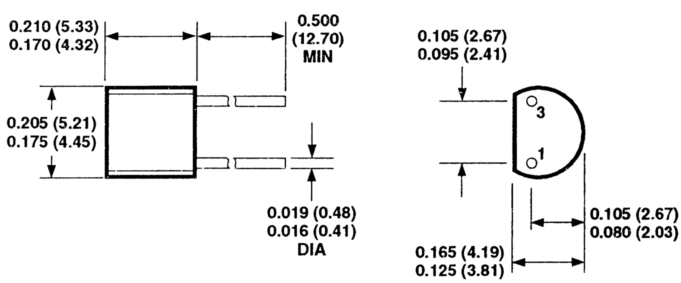
PACKAGE 1

TO-52 (2-PIN)



PACKAGE 2

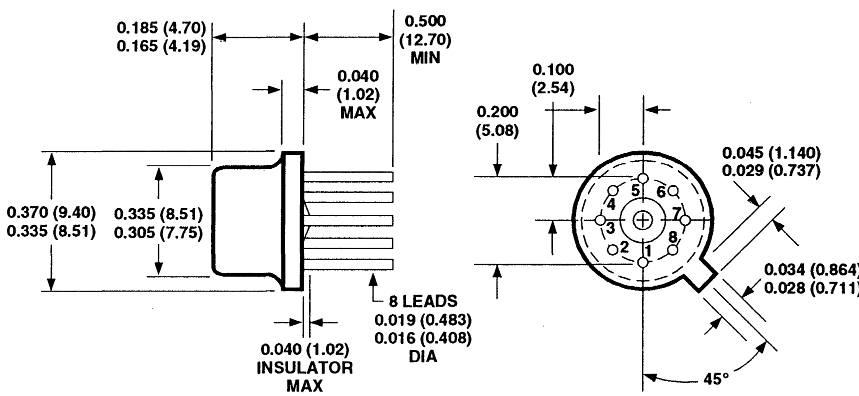
TO-92 (2-PIN)



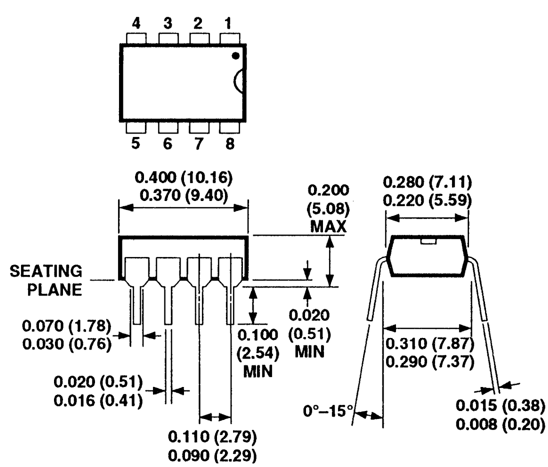
17

PACKAGE INFORMATION

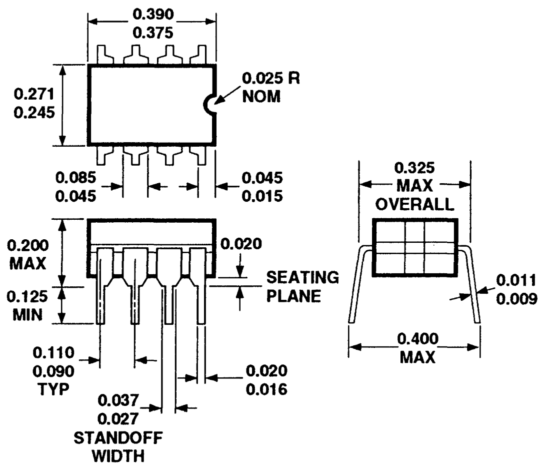
PACKAGE 3
TO-99 (8-PIN)



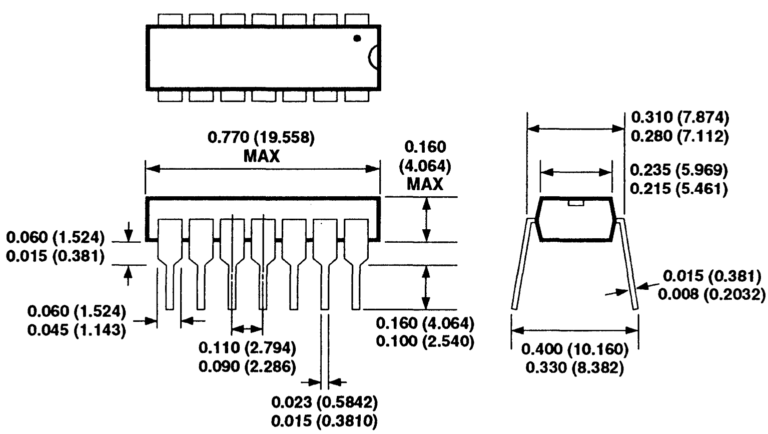
PACKAGE 4
8-PIN PLASTIC DIP



PACKAGE 5
8-PIN CERDIP



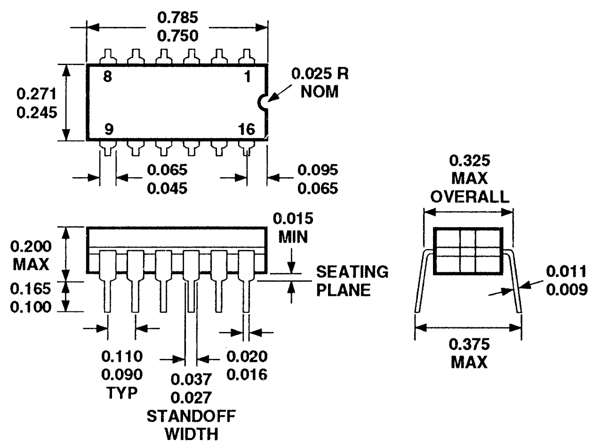
PACKAGE 6
14-PIN PLASTIC DIP



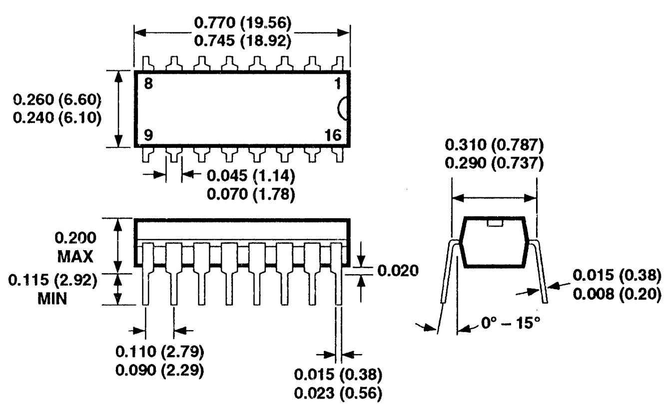
17

PACKAGE INFORMATION

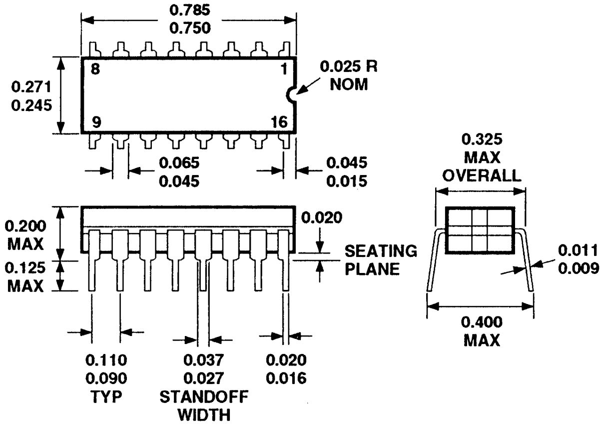
PACKAGE 7
14-PIN CERDIP



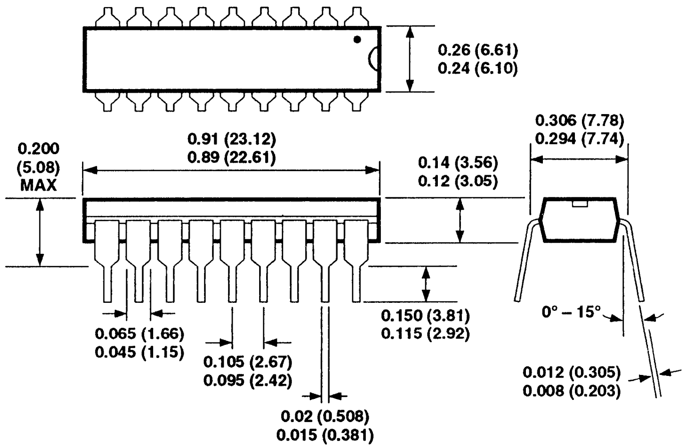
PACKAGE 8
16-PIN PLASTIC DIP



PACKAGE 9
16-PIN CERDIP



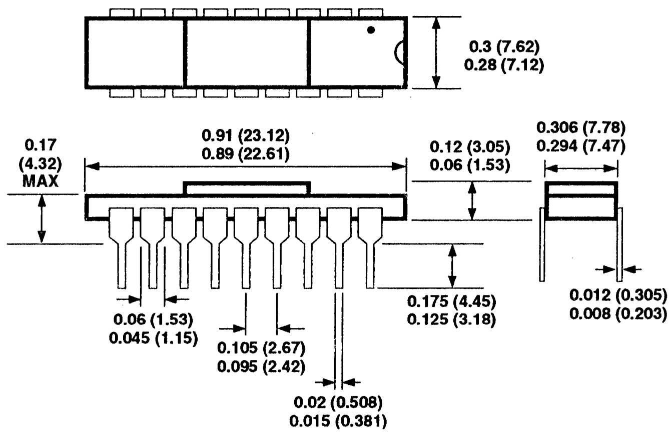
PACKAGE 10
18-PIN PLASTIC DIP



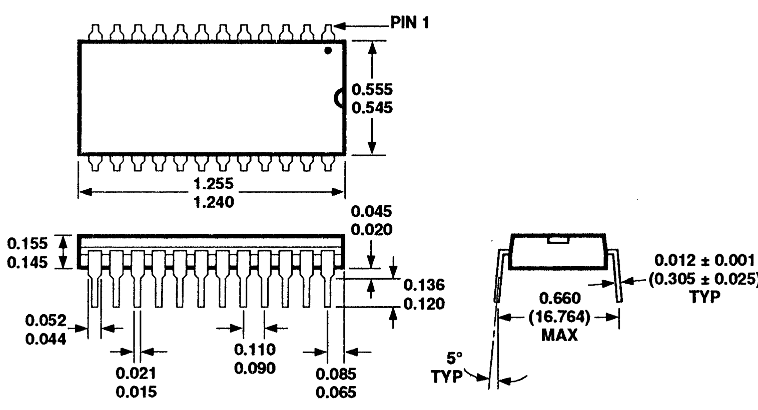
17

PACKAGE INFORMATION

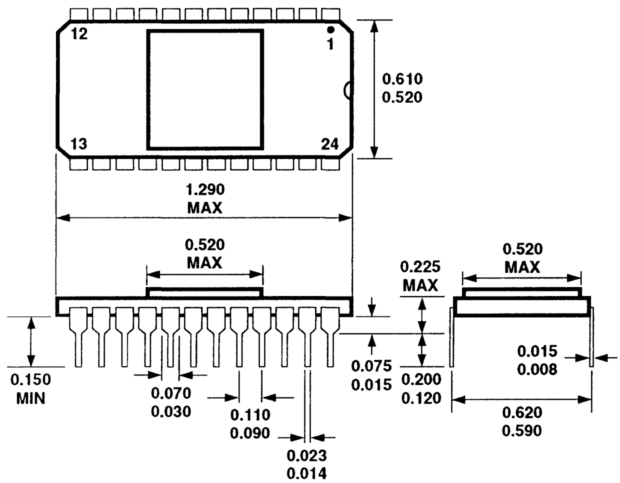
PACKAGE 11
18-PIN CERAMIC DIP



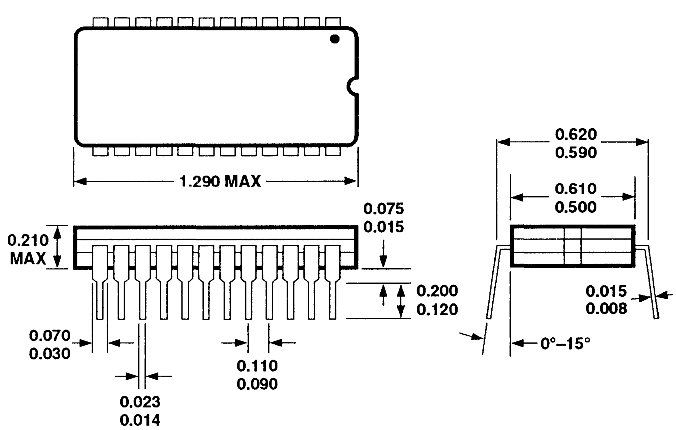
PACKAGE 12
24-PIN PLASTIC DIP



PACKAGE 13
24-PIN CERAMIC DIP

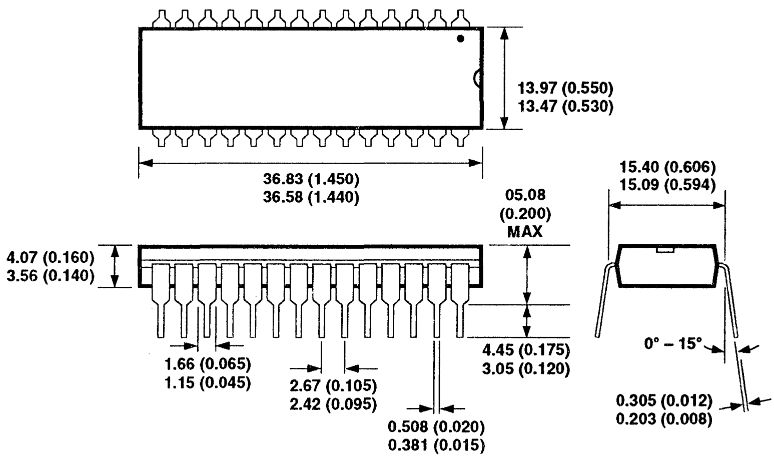


PACKAGE 14
24-PIN CERDIP

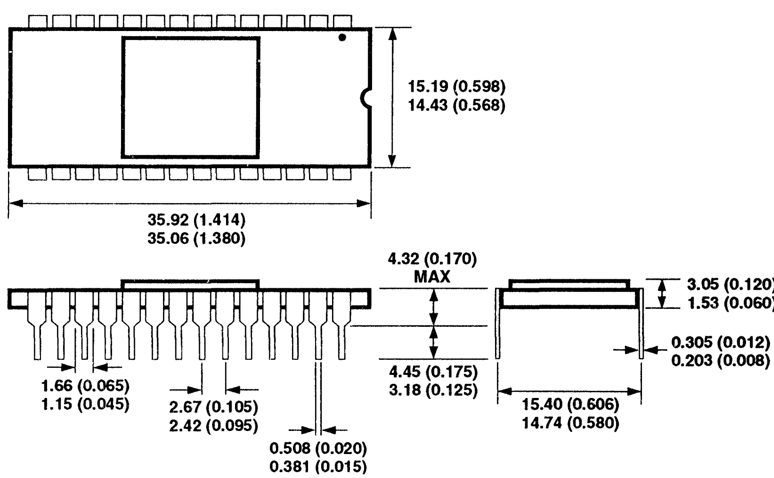


PACKAGE INFORMATION

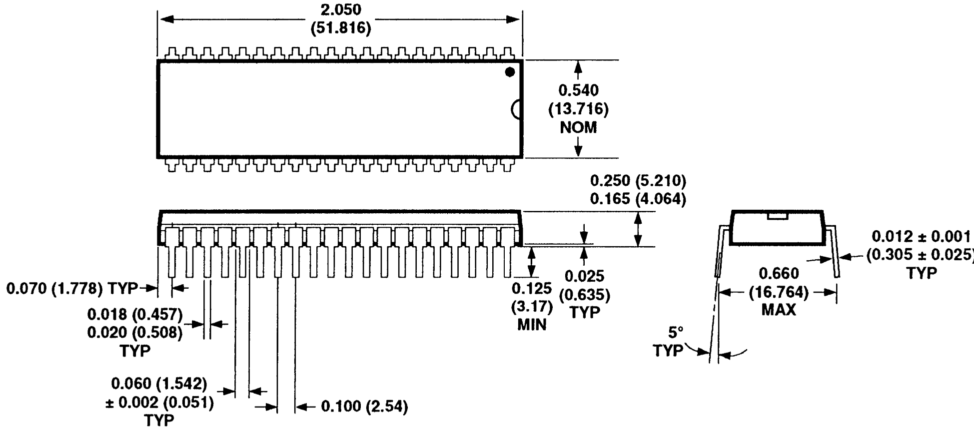
PACKAGE 15
28-PIN PLASTIC DIP



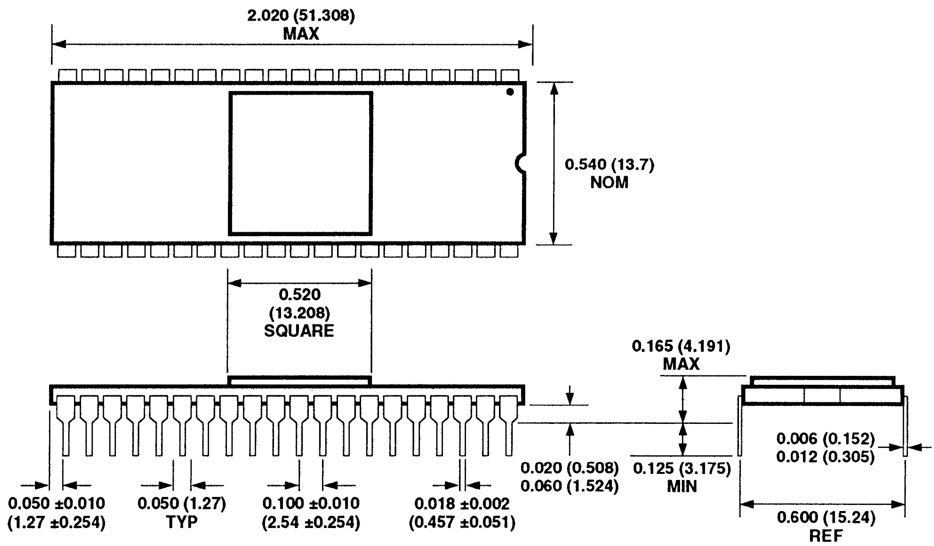
PACKAGE 16
28-PIN CERAMIC DIP



PACKAGE 17
40-PIN PLASTIC DIP



PACKAGE 18
40-PIN CERAMIC DIP



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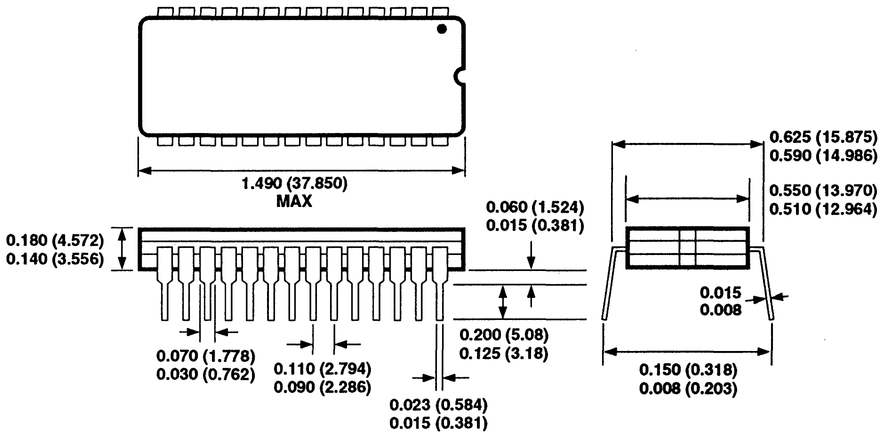
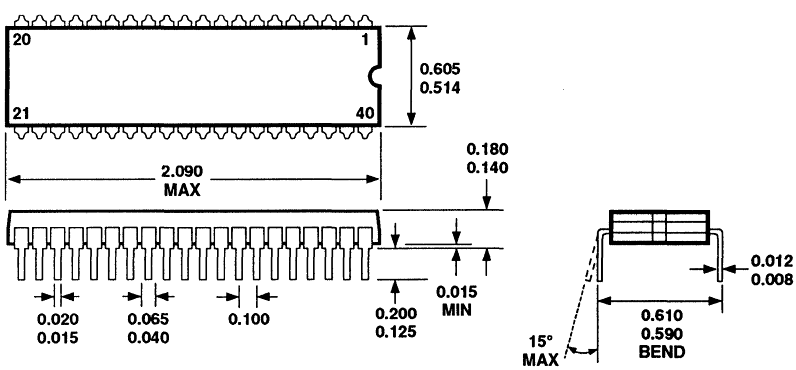
PACKAGE INFORMATION

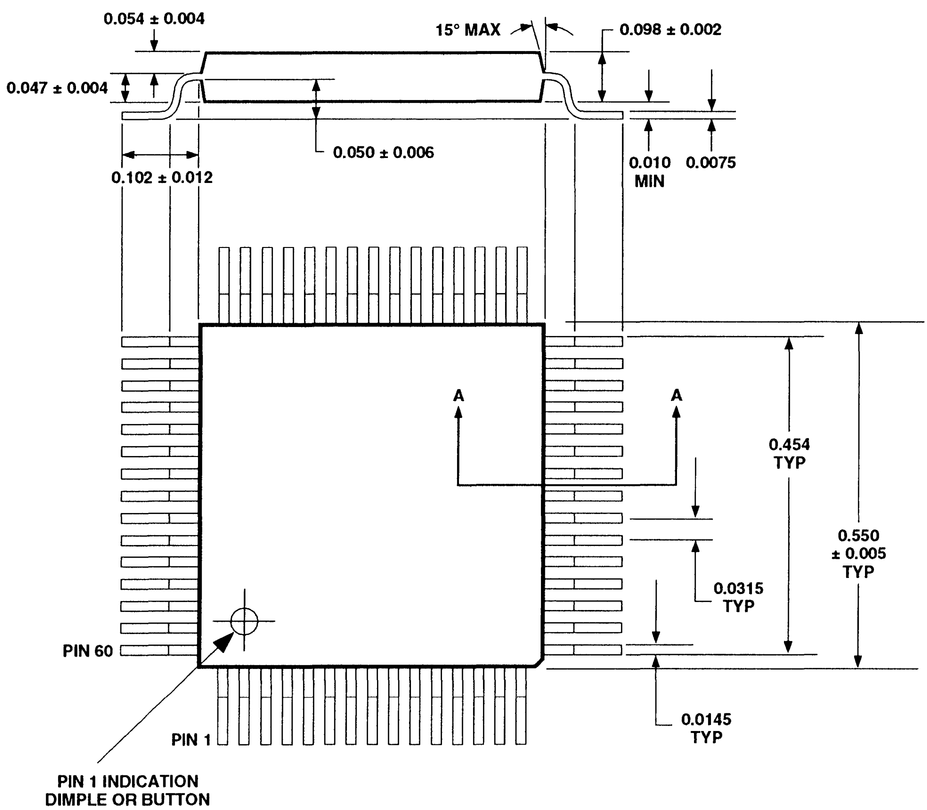
PACKAGE 19
28-PIN CERDIP



PACKAGE 20
40-PIN CERDIP

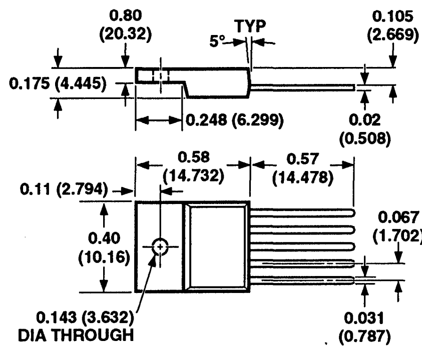


PACKAGE 21
60-PIN FLATPACK FORMED LEADS

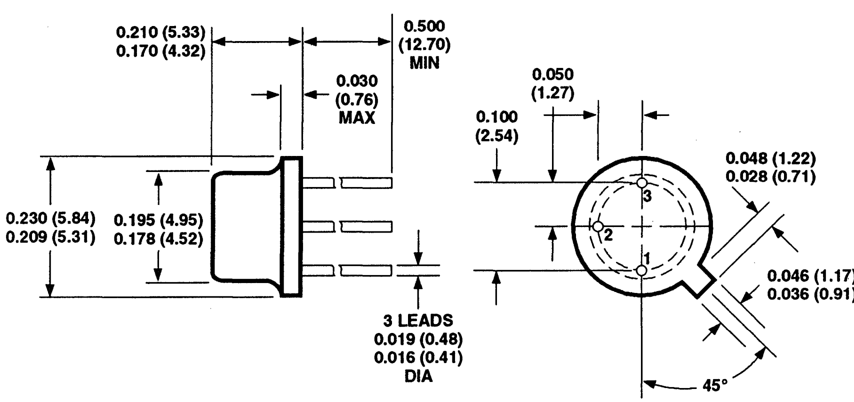


PACKAGE INFORMATION

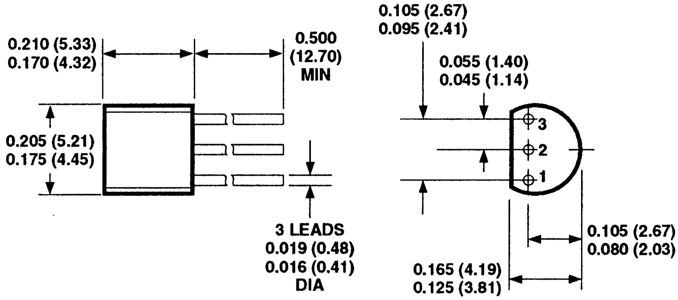
PACKAGE 22
5-PIN TO-220 (PACKAGE AT)



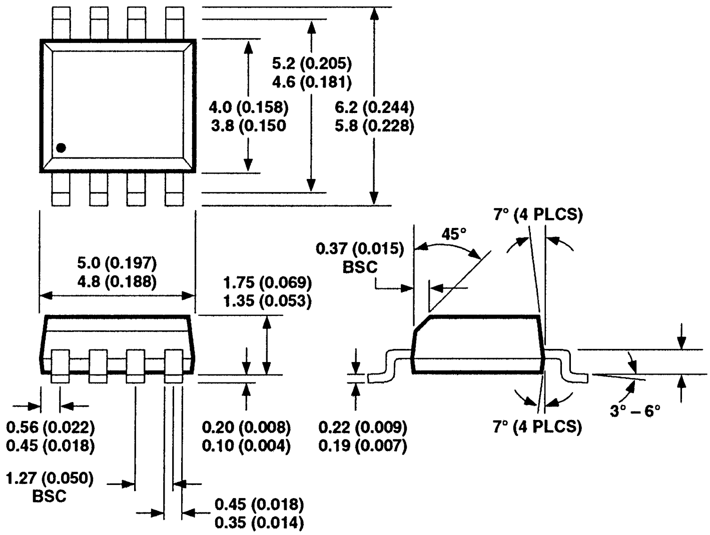
PACKAGE 23
TO-18 (3-PIN)



PACKAGE 24
TO-92 (3-PIN)



PACKAGE 25
8-PIN PLASTIC "SO"



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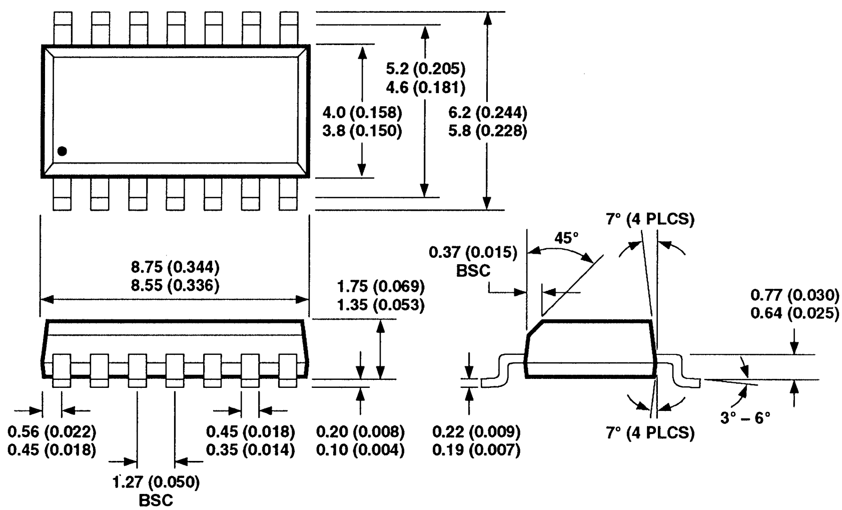
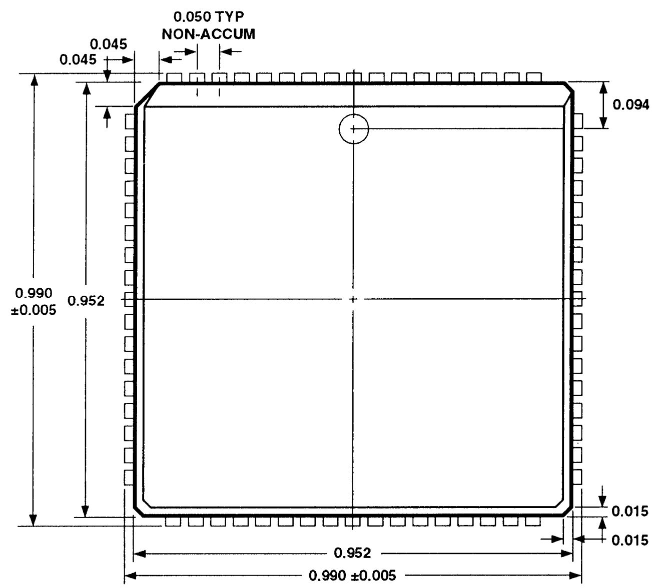
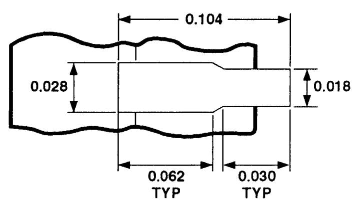
PACKAGE INFORMATION

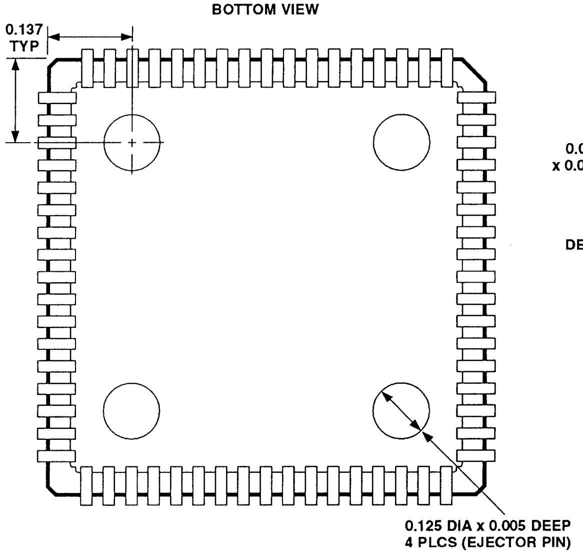
PACKAGE 26
14-PIN PLASTIC "SO"

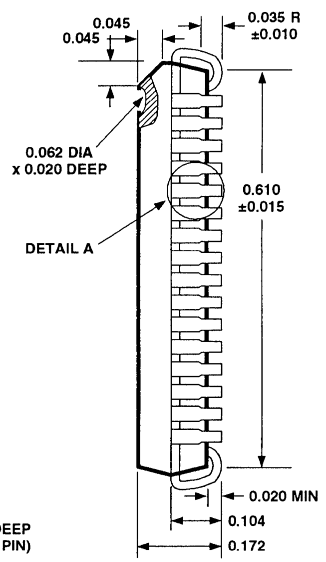


PACKAGE 27
68-PIN PLCC





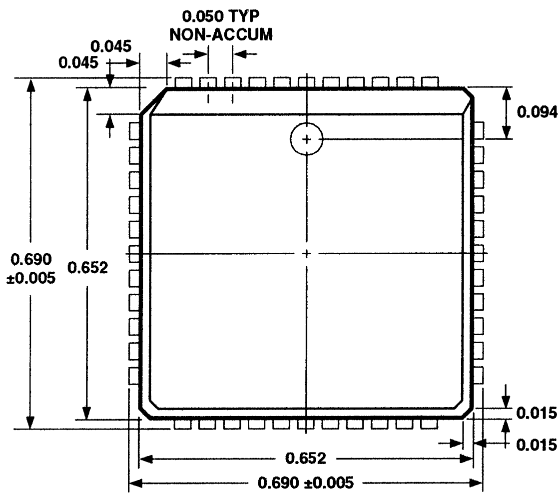




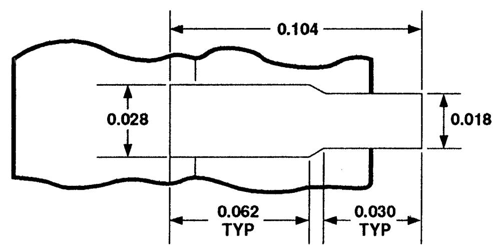
PACKAGE INFORMATION

PACKAGE 28
44-PIN PLCC

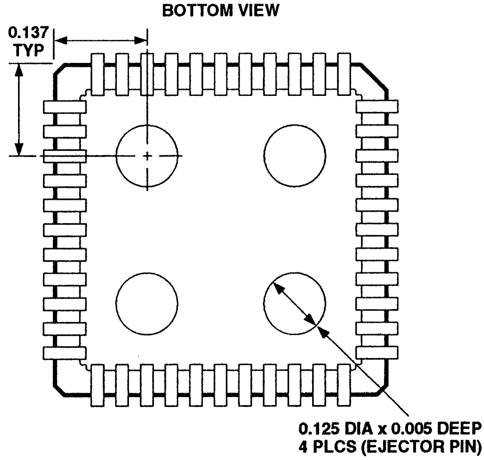
TOP VIEW



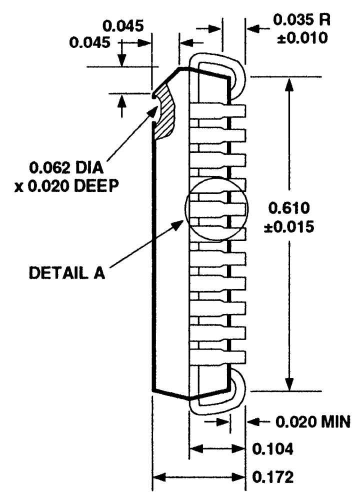
DETAIL VIEW A



BOTTOM VIEW

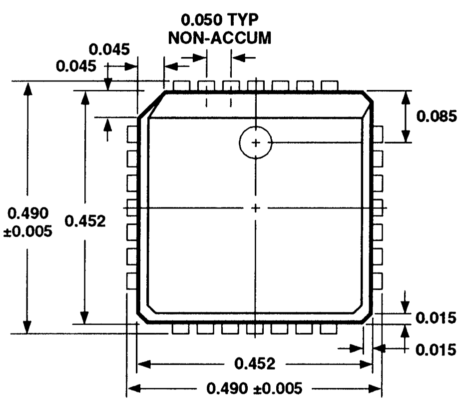


SIDE VIEW

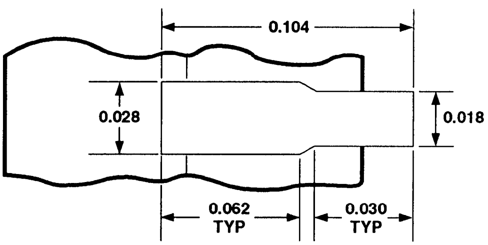


PACKAGE 29
28-PIN PLCC

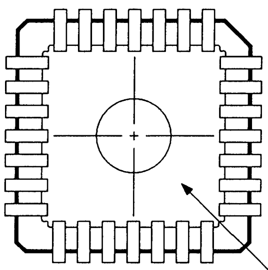
TOP VIEW



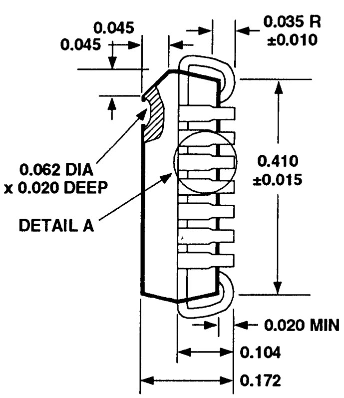
DETAIL VIEW A



BOTTOM VIEW

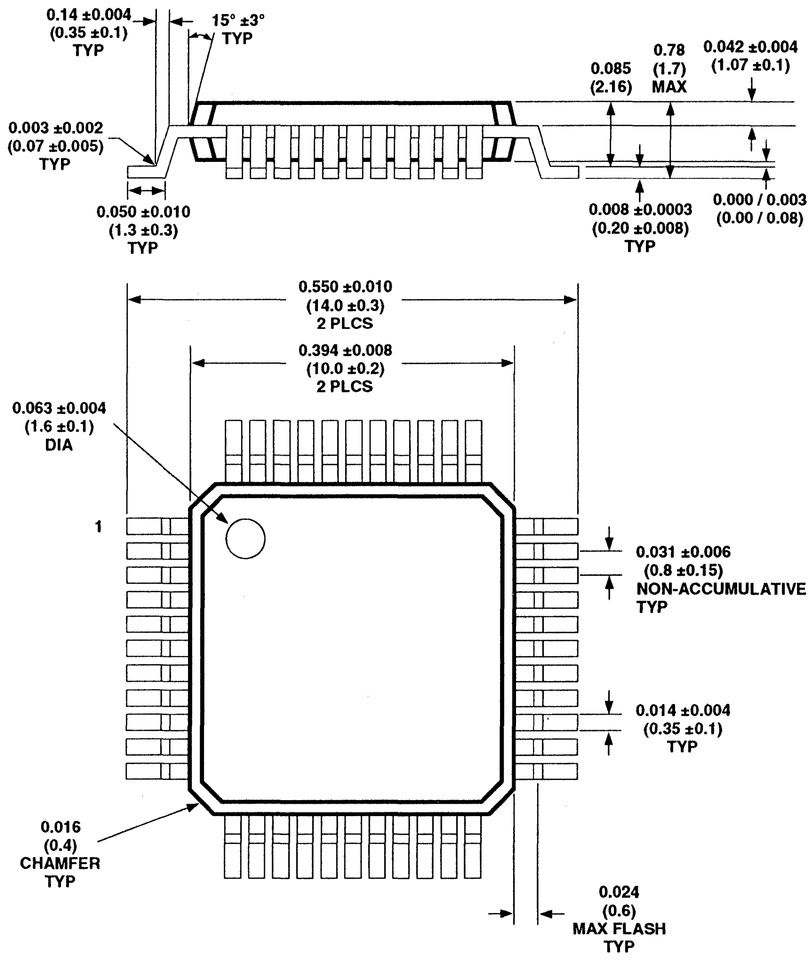


SIDE VIEW

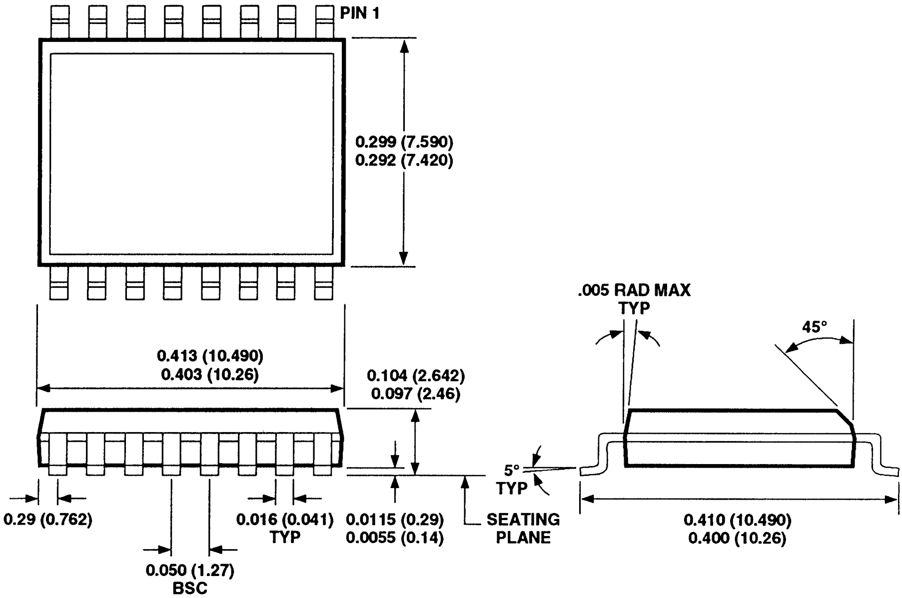


PACKAGE INFORMATION

PACKAGE 30
44-PIN FLAT PACK



PACKAGE 31
16-PIN "SO" WIDE



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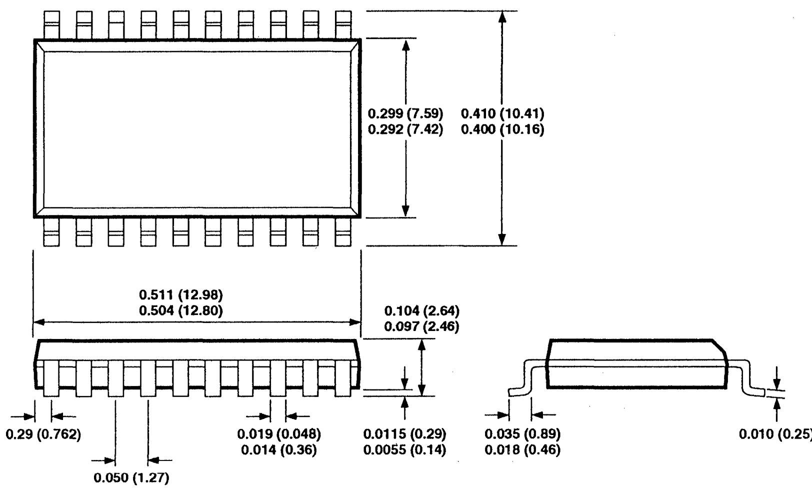
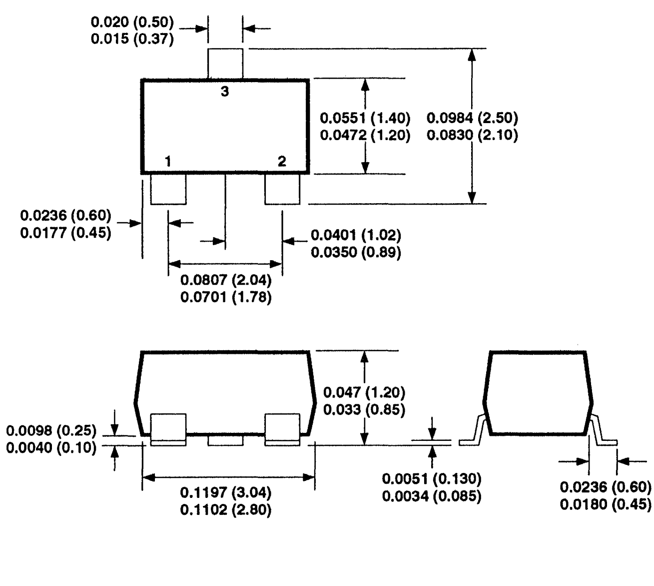
PACKAGE INFORMATION

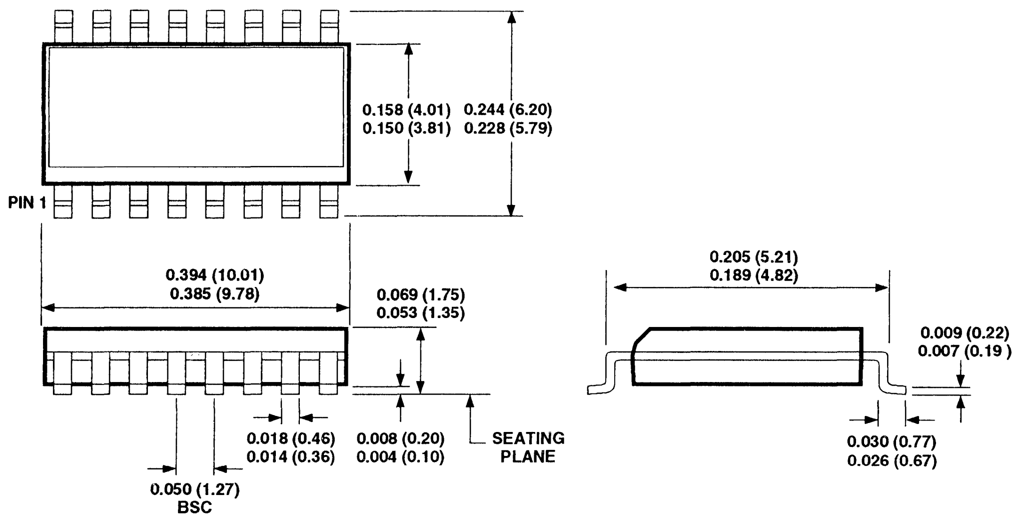
PACKAGE 32
20-PIN "SO" WIDE



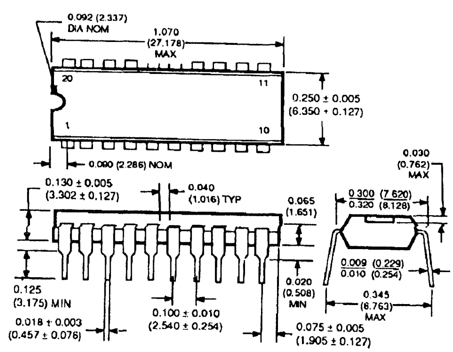
PACKAGE 33
SOT



PACKAGE 34
16-PIN SO



PACKAGE 35
20-PIN PLASTIC DIP



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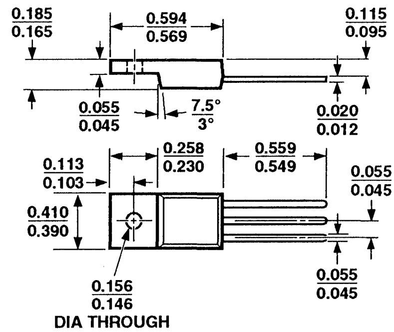
PACKAGE INFORMATION

PACKAGE 36

TO-220 (3-PIN)



Section 18

Sales Offices

Main Sales Offices

Domestic Sales Offices

Teledyne Components
1300 Terra Bella Avenue
P.O. Box 7267
Mountain View, CA 94039-7267
TEL: 415-968-9241
TWX: 910-379-6494
FAX: 415-967-1590

Teledyne Components
10 Oceana Way
Norwood, MA 02062-2601
TEL: 617-255-0300
FAX: 617-255-9576

Foreign Sales Offices

Teledyne Components
Abraham Lincoln Strabe 38-42
6200 Wiesbaden
Germany
TEL: 49-611-768 0
FAX: 49-611-701 239

Teledyne Components
The Harlequin Centre
Southhall Lane
Southhall
Middlesex, UB2 5NH
England
TEL: 44-1-571-9596
FAX: 44-1-571-9439
FAX: 44-1-571-8177

Teledyne Components
11 Dhoby Ghaut #09-06
Cathay Building
Singapore 0922
TEL: 3388077/3387313
FAX: 3393316

United States Manufacturers Representatives

Alabama

Group 2000 Sales, Inc.
109C Jefferson Street
Huntsville, AL 35801
(205) 536-2000
FAX: (205) 533-5525

Alaska

Teledyne Components
1300 Terra Bella Avenue
P.O. Box 7267
Mountain View, CA 94039-7267
(415) 968-9241
TWX: 910/379-6494
FAX: 415/967-1590

Arizona

SMS Associates
7819 E. Greenway Rd., Ste. 5
Scottsdale, AZ 85260
(602) 998-0831
FAX: (602) 998-2045

Arkansas

Southern States Mkting., Inc.
1143 Rockingham, Ste. 106
Richardson, TX 75080
(214) 238-7500
FAX: (214) 231-7662

California

Bestronics of San Diego
9683 Tierra Grande St.
Ste. 102
San Diego, CA 92126
(619) 693-1111
FAX: (619) 693-1963

H-Technical Sales II, Inc.
4 Ventura, Ste. 220
Irvine, CA 92640
(714) 753-7810
FAX: (714) 753-7818

ProMerge Sales, Inc.
1737 N. First Street #510
San Jose, CA 95112
(408) 543-5544
FAX: (408) 453-9536

Colorado

Wescom Marketing
4891 Independence St.
Ste. 235
Wheat Ridge, CO 80033
(303) 422-8957
FAX: (303) 422-9892

Connecticut

Alpha-Omega Sales Corp
325 Main Street
North Reading, MA 01864
(508) 664-1118
FAX: (508) 664-3212

Delaware

S-J Associates, Inc.
204 Plaza Office Center
Mt. Laurel, NJ 08054
(609) 866-1234
FAX: (609) 866-8627

Florida

Component Design Marketing
7616 Southland Blvd. Ste. 103
Orlando, FL 32809
(407) 240-3903
FAX: (407) 240-4305

1900 S.W. 85th Avenue
North Lauderdate, FL 33068
(407) 726-5444
FAX: (305) 480-7674

4502 W. Elm Street
Tampa, FL 33614
(813) 886-9721
FAX: (813) 888-7816

Georgia

Group 2000 Sales, Inc.
5390 Peachtree Industrial Blvd.
Ste. 210B
Norcross, Georgia 30071
(404) 729-1889
FAX: (404) 729-1896

Hawaii

Teledyne Components
1300 Terra Bella Avenue
P.O. Box 7267
Mountain View, CA 94039-7267
(415) 968-9241
TWX: 910/379-6494
FAX: 415/967-1590

Idaho

Wescom Marketing
4891 Independence St.
Ste. 235
Wheat Ridge, CO 80033
(303) 422-8957
FAX: (303) 422-9892

Illinois

CenTech, Inc.
10312 East 63rd Terrace
Raytown, MO 64133
(816) 358-8100
FAX: (816) 358-8107

Dolin Sales Co.
609 Academy Dr.
Northbrook, IL 60062
(708) 498-6770
FAX: (708) 498-4885

Indiana

Luebbe Sales Company
6515 E. 82nd Street, Ste. 202
Indianapolis, IN 46250
(317) 845-7389
FAX: (317) 845-5875

Iowa

Rep Associates Corp.
4905 Lakeside Drive N.E.
Cedar Rapids, IA 52402
(319) 373-0152
FAX: (319) 373-0217

Kansas

Centech, Inc.
10312 East 63rd Terrace
Raytown, MO 64133
(816) 358-8100
FAX: (816) 358-8107

United States Manufacturers Representatives (Cont.)

Kentucky

Luebbe Sales Company
7260 Edington Drive
Cincinnati, OH 45249
(513) 530-0600
FAX: (513) 530-0623

24610 Detroit Road
Westlake, OH 44145
(216) 899-0071
FAX: (216) 899-1072

Mad River Station, Ste. 205-B
2717 Miamisburg-Centerville Road
Dayton, OH 45459-3704
(513) 438-0490
FAX: (513) 438-8760

Louisiana

Southern States Mkting., Inc.
1143 Rockingham, Ste. 106
Richardson, TX 75080
(214) 238-7500
FAX: (214) 231-7662

400 East Anderson Lane
Ste. 610
Austin, TX 78752
(512) 835-5822
FAX: (512) 835-1404

10700 Richmond, Ste. 243
Houston, TX 77042
(713) 789-2426
FAX: (713) 789-3202

Maine

Alpha-Omega Sales Corp
325 Main Street
North Reading, MA 01864
(508) 664-1118
FAX: (508) 664-3212

Maryland

Arbotek Associates
1404 E. Joppa Road
Towson, MD 21204
(301) 825-0775
FAX: (301) 337-2781

Massachusetts

Alpha-Omega Sales Corp
325 Main Street
North Reading, MA 01864
(508) 664-1118
FAX: (508) 664-3212

Michigan

Luebbe Sales Company
27280 Haggerty Road C-11
Farmington Hills, MI 48331
(313) 489-8828
FAX: (313) 489-8829

Minnesota

Comprehensive Technical Sales
6525 City West Pkwy.
Eden Prairie, MN 55344
(612) 941-7181
FAX: (612) 941-4322

Mississippi

Group 2000 Sales, Inc.
5390 Peachtree Industrial Blvd.
Ste. 210B
Norcross, Georgia 30071
(404) 729-1889
FAX: (404) 729-1896

Missouri

CenTech, Inc.
10312 East 63rd Terrace
Raytown, MO 64133
(816) 358-8100
FAX: (816) 358-8107

Montana

Wescom Marketing
4891 Independence St.
Ste. 235
Wheat Ridge, CO 80033
(303) 422-8957
FAX: (303) 422-9892

Nebraska

CenTech, Inc.
10312 East 63rd Terrace
Raytown, MO 64133
(816) 358-8100
FAX: (816) 358-8107

Nevada

ProMerge Sales, Inc.
1737 N. First Street #510
San Jose, CA 95112
(408) 543-5544
FAX: (408) 543-5020

New Hampshire

Alpha-Omega Sales Corp
325 Main Street
North Reading, MA 01864
(508) 664-1118
FAX: (508) 664-3212

New Jersey

Metro Logic Corp.
271 Route 46 West
Ste. D 202
Fairfield, NJ 07006
(201) 575-5585
FAX: (201) 575-8023

S-J Associates, Inc.
204 Plaza Office Center
Mt. Laurel, NJ 08054
(609) 866-1234
FAX: (609) 866-8627

New Mexico

SMS Associates
7819 E. Greenway Rd., Ste. 5
Scottsdale, AZ 85260
(602) 998-0831
FAX: (602) 998-2045

New York

Gen-Tech Electronics
4855 Executive Drive
Liverpool, NY 13088
(317) 451-3480
FAX: (317) 451-0988

United States Manufacturers Representatives (Cont.)

New York (Cont.)

Metro Logic Corp.
271 Route 46 West
Ste. D 202
Fairfield, NJ 07006
(201) 575-5585
FAX: (201) 575-8023

North Carolina

Group 2000 Sales, Inc.
109C Jefferson Street
Huntsville, Alabama 35801
(205) 536-2000
FAX: (205) 533-5525

5390 Peachtree Industrial Blvd.
Ste. 210B
Norcross, Georgia 30071
(404) 729-1889
FAX: (404) 729-1896

North Dakota

Comprehensive Technical Sales
6525 City West Pkwy.
Eden Prairie, MN 55344
(612) 941-7181
FAX: (612) 941-4322

Ohio

Luebbe Sales Company
7260 Edington Drive
Cincinnati, Oh 45249
(513) 530-0600
FAX: (513) 530-0623

Mad River Sta., Ste. 205-B
2717 Miamisburg-Centerville Road
Dayton, OH 45459-3704
(513) 438-0490

24610 Detroit Road
Westlake, OH 44145
(216) 899-0071
FAX: (216) 899-1072

Oklahoma

Southern States Mkting., Inc.
1143 Rockingham, Ste. 106
Richardson, TX 75080
(214) 238-7500
FAX: (214) 231-7662

Oklahoma (Cont.)

400 East Anderson Lane
Ste. 610
Austin, TX 78752
(512) 835-5822
FAX: (512) 835-1404

10700 Richmond, Ste. 243
Houston, TX 77042
(713) 789-2426
FAX: (713) 789-3202

Oregon

Advanced Technical Marketing
4900 S.W. Griffith Drive, #105
Beaverton, OR 97005
(503) 643-8307
FAX: (503) 643-4364

Pennsylvania

Luebbe Sales Company
9800 McKnight Rd., Ste. 200-B
Pittsburgh, PA 15237
(412) 364-0490
FAX: (412) 364-4290

S-J Associates, Inc.
204 Plaza Office Center
Mt. Laurel, NJ 08054
(609) 866-1234
FAX: (609) 866-8627

Rhode Island

Alpha-Omega Sales Corp.
325 Main Street
North Reading, MA 01864
(508) 664-1118
FAX: (508) 664-3212

South Carolina

Group 2000 Sales, Inc.
109C Jefferson Street
Huntsville, AL 35801
(205) 536-2000
FAX: (205) 533-5525

South Dakota

Comprehensive Technical Sales
6525 City West Parkway
Eden Prairie, MN 55344
(612) 941-7181
FAX: (612) 941-4322

Tennessee

Group 2000 Sales, Inc.
109C Jefferson Street
Huntsville, AL 35801
(205) 536-2000
FAX: (205) 533-5525

Texas

Southern States Mkting., Inc.
1143 Rockingham, Ste. 106
Richardson, TX 75080
(214) 238-7500
FAX: (214) 231-7662

400 East Anderson Lane
Ste. 610
Austin, TX 78752
(512) 835-5822
FAX: (512) 835-1404

10700 Richmond, Ste. 243
Houston, TX 77042
(713) 789-2426
FAX: (713) 789-3202

Utah

Wescom Marketing
3500 S. Main Street
Salt Lake City, UT 94115
(801) 269-0419
FAX: (303) 422-9892

Vermont

Alpha-Omega Sales Corp.
325 Main Street
North Reading, MA 01864
(508) 664-1118
FAX: (508) 664-3212

United States Manufacturers Representatives (Cont.)

Virginia

Arbotek Associates, Inc.
1404 E. Joppa Road
Towson, MD 21204
(301) 825-0775
FAX: (301) 337-2781

Washington

Advanced Technical Marketing
8521 154th Avenue N.E.
Redmond, WA 98052
(206) 869-7636
FAX: (206) 869-9841

Washington, DC

Arbotek Associates
1404 E. Joppa Road
Towson, MD 21204
(301) 825-0775
FAX: (301) 337-2781

West Virginia

Luebbe Sales Company
9800 McKnight Road
Ste. 200-B
Pittsburgh, PA 15237
(412) 364-0490
FAX: (412) 364-4290

Wisconsin

Comprehensive Technical Sales
6525 City West Parkway
Eden Prairie, MN 55344
(612) 941-7181
FAX: (612) 941-4322

Dolin Sales Co.
250 W. Coventry Ct.
Glendale, WI 53217
(414) 482-1111
FAX: (414) 351-4142

Wyoming

Wescom Marketing
4891 Independence Street
Ste. 235
Wheat Ridge, CO 80033
(303) 422-8957
FAX: (303) 422-9892

Canadian Manufacturers Representatives

British Columbia

Weiss Company
4381 Fraser Street, #202
Vancouver, British Columbia,
CN V5V 4G4
(604) 873-1112
FAX: (604) 873-1120

Manitoba

Weiss Company
P.O. Box 225, Station "L"
Winnepeg, Manitoba
CN R3H 0Z5
(204) 772-3665
FAX: (204) 774-1814

Ontario

Weiss Company
7270 Torbram Road, #5
Mississauga, Ontario
CN L4T 3Y7
(416) 673-0011
FAX: (416) 673-1270

Weiss Company
P.O. Box 1235, Station "H"
Nepean, Ontario
CN K2J 1Z9
(613) 692-0617
FAX: (613) 692-4081

Quebec

Weiss Company
2044 St. Regis Blvd.
Dorval, Quebec
CN H9P 1H6
(514) 685-6644
FAX: (514) 685-6950

Canadian Distributors

Alberta

Future Electronics, Inc.
3833-29th Street NE
Calgary, Alberta
CN T1Y 6B5
(403) 250-5550
FAX: (403) 291-7054

4606-97th Street
Edmonton, Alberta
CN T6E 5N9
(403) 438-2858
FAX: (403) 434-0812

British Columbia

Future Electronics, Inc.
1695 Boundary Road
Vancouver, BC
CN V5K 4X7
(604) 294-1166
FAX: (604) 294-1206

Manitoba

Future Electronics, Inc.
106 King Edward
Winnipeg, Manitoba
CN R3H 0N8
(204) 786-7711
FAX: (204) 783-8133

Ontario

Future Electronics, Inc.
1050 Baxter Road
Ottawa, Ontario
CN K2C 3P2
(613) 820-8313
FAX: (613) 820-3271

5935 Airport Road, Suite 200
Mississuaga, Ontario
CN L4V 1W5
(416) 612-9200
FAX: (416) 612-9185

Marshall Industries, Inc.
4 Paget Road, Units 10 & 11
Building 1112
Brampton, Ontario
CN L6T 5G3
(416) 458-8046
FAX: (416) 458-1613

Quebec

Future Electronics, Inc.
1000 Ave St. Jean Baptist,
Suite 100
Quebec
CN G2E 5G5
(418) 877-6666
FAX: (418) 877-6671

237 Hymus Blvd.
Polnte Claire, Quebec
CN H9R 5P9
(514) 694-7710
FAX: (514) 694-3707

Marshall Industries, Inc.
148 Brunswick Blvd.
Polnte Claire, Quebec
CN H9R 5P9
(514) 694-8142
FAX: (514) 694-6989

United States Distributors

Alabama

Future Electronics, Inc.
237 Hymus Blvd.
Huntsville, AL 35805
(205)830-2322
Fax: (205)830-6664

Marshall Industries, Inc.
3313 Memorial Pkwy South
Huntsville, AL 35801
(205)881-9235
Fax: (205)881-1490

Arizona

Future Electronics, Inc.
4636 E. University Dr.
Suite 245
Phoenix, AZ 85034
(602)968-7140
Fax: (602)968-0334

Marshall Industries, Inc.
9830 S. 51st St.
Phoenix, AZ 85044
(602)496-0290
Fax: (602)893-9029

California

All American Semiconductor
2360 Qume Dr., Suite C
San Jose, CA 95131
(408)943-1200
(800)222-6001
Fax: (408)943-1393

All American Semiconductor
369 Van Ness Way
Suite 701
Torrance, CA 90501
(310)320-0240
(800)669-8300
Fax: (310)320-7207

All American Semiconductor
5060 Shoreham Place
Suite 200
San Diego, CA 92122
(619)458-5850
Fax: (619)458-5866

California (Cont.)

All American Semiconductor
17220 New Hope St.
Suite 211
Fountain Valley, CA 92708
(714)435-0115

Elmo Semiconductor Corp.
7590 N. Glen Oaks Blvd.
Burbank, CA 91504
(818)768-7400
Fax: (818)767-7038

Future Electronics, Inc.
2220 O'Toole Ave.
San Jose, CA 95131
(408)434-1122
Fax: (408)344-0822

Future Electronics, Inc.
9301 Oakdale Ave.
Suite 210
Chatsworth, CA 91311
(818)772-6240
Fax: (818)772-6247

Future Electronics, Inc.
16925 Browning Ave.
Irvine, CA 92714
(714)250-4141
Fax: (714)250-4185

Future Electronics, Inc.
3940 Ruffin Rd., Unit E
San Diego, CA 92123
(619)278-5020
Fax: (619)756-8546

Marshall Industries, Inc.
9320 Telstar Ave.
El Monte, CA 91731-3004
(1-800)522-0084
Fax: (818)307-6297

Marshall Industries, Inc.
26637 Agoura Rd.
Calabasas, CA 91302-1959
(818)880-7000
Fax: (818)880-6846

Marshall Industries, Inc.
One Morgan
Irvine, CA 92718
(714)458-5301
Fax: (714)581-5255

California (Cont.)

Marshall Industries, Inc.
10105 Carroll Canyon Rd.
San Diego, CA 92131
(619)578-9600
Fax: (619)586-0469

Marshall Industries, Inc.
3039 Kilgore Ave., #140
Rancho Cordova, CA 95670
(916)635-9700
Fax: (916)635-6044

Marshall Industries, Inc.
336 Los Coches St.
Milpitas, CA 95035
(408)942-4600
Fax: (408)262-1224

Zeus Components, Inc.
5236 Colodny Dr.
Agoura Hills, CA 91301
(818)889-3838
Fax: (818)889-2464

Zeus Components, Inc.
6276 San Ignacio Ave., Suite E
San Jose , CA 95119
(408)629-4789
Fax: (408)629-4792

Zeus Components, Inc.
22700 Savi Ranch Pkwy
Yorba Linda, CA 92686
(714)921-9000
Fax: (714)921-2715

Colorado

Future Electronics, Inc.
9030 Yukon St., Suite 2700
Broomfield, CO 80021
(303)421-0123
Fax: (303)421-7696

Integrated Electronics Corp.
5750 N. Logan St.
Denver, CO 80216
(303)292-6121
Fax: (303)297-2053

Marshall Industries, Inc.
12351 N. Grant
Thornton, CO 80241
(303)451-8383
Fax: (303)457-2899

United States Distributors

Connecticut

Future Electronics, Inc.
24 Stony Hill Rd.
Bethel, CT 06801
(203)743-9594
Fax: (203)798-9745

Marshall Industries, Inc.
20 Sterling Dr.
Barnes Indl. Park North
P.O. Box 200
Wallingford, CT 06492-0200
(203)265-3822
Fax (203)284-9285

Florida

All American Semiconductor
16251 NW 54th Ave.
Miami, FL 33014
(305)621-8282
(800)829-8282
Fax: (305)620-7831

All American Semiconductor
5009 Hiatus Rd.
Sunrise, FL 33351
(305)572-7999
(800)222-6001
Fax: (305)749-9229

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810
(407)298-7100
Fax: (407)290-0164

Future Electronics, Inc.
650 Northlake Blvd.
Suite 520
Altamonte Springs, FL 32701
(407)767-8414
Fax: (407)767-0645

Future Electronics, Inc.
2200 Tall Pines Dr., Suite 108
Largo, FL 34641
(813)530-1222
Fax: (813)538-9598

Marshall Industries, Inc.
380 S. Northlake Blvd.
Suite 1024
Altamonte Springs, FL 32701
(407)767-8585
Fax: (305)767-8585

Florida (Cont.)

Marshall Industries, Inc.
2700 W. Cypress Creek Rd.
Suite D114
Ft. Lauderdale, FL 33309
(305)977-4880
Fax: (305)977-4887

Marshall Industries, Inc.
2840 Scherer Dr., Suite 410
St. Petersburg, FL 33716
(813)573-1399
Fax: (305)767-8676

Nu-Horizons
3421 NW 55th St.
Fort Lauderdale, FL 33309
(305)735-2555
Fax: (305)735-2880

Zeus Components, Inc.
285 Central Pkwy
Suite 1730
Altamonte Springs, FL 32714
(407)365-3000
Fax: (407)365-2356

Georgia

Future Electronics, Inc.
3000 Northwoods Pkwy
Suite 295
Norcross, GA 30071
(404)441-7676
Fax: (404)441-7580

Nu-Horizons
555 Oakbrook Pkwy
Suite 340
Norcross, GA 30093
(404)416-8666
Fax: (404)416-9060

Illinois

Advent Electronics Inc.
7110-16 N. Lyndon St.
Rosemont, IL 60018
(708)298-4210
Fax: (708)297-6650

Future Electronics, Inc.
1000 E. State Pkwy Unit B
Schaumburg, IL 60173
(708)882-1255
Fax: (708)490-9290

Illinois (Cont.)

Marshall Industries, Inc.
50 E. Commerce Dr., Unit 1
Schaumburg, IL 60173
(708)490-0155
Fax: (312)490-0569

Indiana

Advent Electronics Inc.
8446 Moller Rd.
Indianapolis, IN 46268
(317)872-4910
Fax: (317)872-9987

Marshall Industries, Inc.
6990 Corporate Dr.
Indianapolis, IN 46278
(317)297-0483
Fax: (317)297-2787

Iowa

Advent Electronics Inc.
682-58th Ave. Court SW
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(319)363-0221
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Lenexa, KS 66214
(913)492-3121
Fax: (913)492-6205

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(301)997-1118
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Wakefield, MA 01880
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(800)274-2834
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Wakefield, MA 01880
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24713 Crestview Court
Farmington, MI 48331
(313)477-1650
Fax: (313)477-2630

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Suite 106
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31067 Schoolcraft
Livonia, MI 48150
(313)525-5850
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Eden Prairie, MN 55344
(612)944-2151
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Suite 196
Eden Prairie, MN 55344
(612)944-2200
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3955 Annapolis Ln.
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(612)559-2211
Fax: (612)559-8321

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St. Louis, MO 63141
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P.O. Box 600
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(704)455-9030
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1 N. Comm. Ctr.
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(513)989-4480
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30700 Bainbridge Rd., Unit A
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(216)248-1178
Fax: (216)248-2312

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Zeus Components, Inc.
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Suite 106
Dayton, OH 45439
(513)293-6162
Fax: (513)293-1781

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Future Electronics, Inc.
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Beaverton, OR 97006
(503)645-9454
Fax: (503)645-1559

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Beaverton, OR 97005
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Fax: (503)644-5050

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Marshall Industries, Inc.
401 Parkway View Dr.
Pittsburgh, PA 15205
(412)788-0441
Fax: (412)963-7982

Texas

All American Semiconductor
1819 Firman Dr.
Suite 127
Richardson, TX 75081
(214)231-5300
(800)541-1435
Fax: (214)437-0353

Future Electronics, Inc.
1850 N. Greenville
Suite 146
Richardson, TX 75081
(214)437-2437
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2117 South 3600 West
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(801)977-9750
Fax: (801)975-1207

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2355 S. 1070 W. Suite D
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(801)973-2288
Fax: (801)973-2296

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Future Electronics, Inc.
4038-148th Ave., NE
Redmond, WA 98052
(206)881-8199
Fax: (206)881-5232

Washington (Cont.)

Marshall Industries, Inc.
11715 N. Creek Pkwy. South
Suite 112
Bothell, WA 98011
(206)486-5747
Fax: (206)486-6964

Wisconsin

Future Electronics, Inc.
20875 Crossroads Circle
Suite 200
Waukesha, WI 53186
(414)786-1884
Fax: (414)786-0744

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Crossroads Corporate Center 1
20900 Swenson Dr.
Suite 150
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Fax: (414)797-8270

International Representatives and Distributors

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Fax: (011)49 6501/6726

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Fax: (011)43 222 8285617

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Fax: (011)45 44 532044

Finland

OY Fintronic AB
Heikkillantie 2A
SF-02100 Helsinki
(011)0 358 692 6022
Fax: (011)0 358 682 1251

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SF-00700 Helsinki
(011)0 358 351 1800
Fax: (011)0 358 345 3384

France

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F-92310 Sevres
(011)145 347535
Fax: (011)145 072191

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F-92320 Chatillon-Sous-Bagneux
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Fax: (011)149 652769

Hong Kong

Component Agent Ltd.
36/F Metroplaza, Tower 1
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Kwai Chung
(011)852-487 8826
Fax: (011)852 487 1268

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G.K. Marg, Lower Parcel
Bombay 400013, India
(011)91-22-494-7457

Italy

Velco SRL
Contra S. Francesco 75
1-361000 Vicenza
(011)39 444 922922
Fax: (011)39 444 922338

Japan

Tomen Electonics Corp.
1-1, Uchisaiwai-Cho 2-Chome
Chiyoda-Ku, Tokyo 100 Japan
(011)81 3 506-3477
Fax: (011)81 3 506-3497

U.S.A. Branch
1333 Lawrence Expressway
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Fax: (408)248-2960

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(011)81 6 208-3636
Fax: (011)81 6 208-3640

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K S Bldg 2 F
2-4-1 Sadohara-cho, Ichigaya
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(011)3 260 8401
Fax: (011)3 260-8412

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Seoul
Korea
(011)82 2 266 1663
Fax: (011)82 2 272 7807

International Representatives and Distributors

Malaysia

NIE Electronics (M) Sdn Bhd
1004/1005, Resource
Complex 33
Jalan Segambut Atas
51200 Kuala Lumpur
Malaysia
(011)60-3-621-2122
Fax: (011)60-3-621-1789

New Zealand

R&D Electronics
4 Florence Street
P.O. Box 206
Burwood, Victoria
Australia 3125
(011)61-3-808-8911
Fax: (011)61-3-808-9168

North Germany

Adelco Elektronik GmbH
Boxholmstrasse 5
2085 Quickborn bei Hamburg
Germany
(011)49 4106 2024
Fax: (01149 4106 3852

Weisbauer Elektronik GmbH
Heiliger Weg 1
4600 Dortmund 1
(011)49 231 579547
Fax: (011)49 231 577514

Norway

Hefro Elektronikk a.s.
Haavard Martinsens vei 19
N-0915 Oslo 9
(011)2 10 73 00
(011)2 10 65 46

Portugal

Componenta
Components Electronicos, Lda
Rua Luis Camoes, 128
P-1399 Lisboa
(011)351 1362 12 83/84

Singapore

NIE Electronics (S) PTE Ltd.
Block 5022 #03-41
Ang Mo Kio
Industrial Park 2
Singapore 2056
(011)483-3133
Fax: (011)483-4288

South Africa

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RSA 2125 Randburg
(011)27 789 1065/75
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(011)12-3227613/21
Fax: (011)12-3223721

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Semitron W. Rock GmbH
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7897 Kussaberg 6
(011)49 7742 80010
Fax: (011)49 7742 6901

Neumuller GmbH
Eschenstrassee 2
8028 Taufkirchen/Munchen
(011)49 89 612080
Fax: (011)49 89 61208248

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Julius-Holder-Strasse 42
7000 Stuttgart 70
(011)49 711 720010
Fax: (011)49 711 7289780

Spain

Amitron SA
Avda. de Valladolid, 47D
E-28008 Madrid
(011)34 1 542 0906
Fax: (01134 1 248 7958

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Bexab Technology AB
Kemistvagen 10
S-18325 Taby
(011)46 8 732 8980
Fax: (011)46 8 732 7058

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Fax: (011)41 57 341443

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Fax: (011)41 1 8335081

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Taiwan
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Fax: (011)886-2-706 0465

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Pazarlama A.S.
Florya Is Merkezi
Londra Asfalti, 5 Yol
TR-34630 Sefakoy-Istanbul
(011)90 15806767
Fax: (011)90 1598 5353

International Representatives and Distributors

United Kingdom

Future Electronics Ltd.
Petersfeld Avenue
Slough, Berks SL2 5EA
(011)44 75321193
Fax: (011)44 75377661

Hunter Electronic Components
Unit 3 Central Estate
Denmark St.
Maidenhead, Berks, SL67BN
(011)44 628 75911
Fax: (011)44 628 75611

Phoenix Electronics
Phoenix House
Bothwell Road
Castlehill
Carluke
Strathclyde ML8 5UF
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Fax: (011)44 55551562

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Fax: (011)52 14 11-27-67

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Sector Juarex
44100 Guadalajara, Jal
(011)52 36 26-12-32
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Alejandro Humbolt 17502-105
Fraco, Garita De Otay
22300 Tijuana, B.C.
(011)52 66 23-78-93
Fax: (011)52 66 23-78-94