

TLC32046

Wide-Band Analog Interface Circuit

Data Manual

TLC32046
Wide-Band Analog Interface Circuit
Data Manual



IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to or to discontinue any semiconductor product or service identified in this publication without notice. TI advises its customers to obtain the latest version of the relevant information to verify, before placing orders, that the information being relied upon is current.

TI warrants performance of its semiconductor products to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Unless mandated by government requirements, specific testing of all parameters of each device is not necessarily performed.

TI assumes no liability for TI applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Texas Instruments products are not intended for use in life-support appliances, devices, or systems. Use of a TI product in such applications without the written consent of the appropriate TI officer is prohibited.

Copyright © 1991, Texas Instruments Incorporated

Printed in the U.S.A.

Contents

| | <i>Page</i> |
|---|-------------|
| Introduction | 1-1 |
| Features | 1-2 |
| Functional Block Diagrams | 1-3 |
| Terminal Assignments | 1-6 |
| Terminal Functions | 1-7 |
| Detailed Description | 2-1 |
| Internal Timing Configuration | 2-2 |
| Analog Input | 2-4 |
| A/D Band-Pass Filter, Clocking, and Conversion Timing | 2-4 |
| A/D Converter | 2-4 |
| Analog Output | 2-4 |
| D/A Low-Pass Filter, Clocking, and Conversion Timing | 2-4 |
| D/A Converter | 2-5 |
| Serial Port | 2-5 |
| Synchronous Operation | 2-5 |
| One 16-Bit Word | 2-5 |
| Two 8-Bit Bytes | 2-5 |
| Synchronous Operating Frequencies | 2-6 |
| Asynchronous Operation | 2-6 |
| One 16-Bit Word | 2-6 |
| Two 8-Bit Bytes | 2-6 |
| Asynchronous Operating Frequencies | 2-7 |
| Operation of TLC32046 With Internal Voltage Reference | 2-7 |
| Operation of TLC32046 With External Voltage Reference | 2-7 |
| Reset | 2-7 |
| Loopback | 2-7 |
| Communications Word Sequence | 2-8 |
| DR Serial Data Word Format | 2-8 |
| DR Word Bit Pattern | 2-8 |
| DX Serial Data Word Format | 2-9 |
| Primary DX Word Bit Pattern | 2-9 |

| | <i>Page</i> |
|--|-------------|
| Secondary DX Word Blt Pattern | 2-10 |
| Reset Function | 2-10 |
| Power-Up Sequence | 2-11 |
| AIC Register Constraints | 2-11 |
| AIC Responses to Improper Conditions | 2-11 |
| Operation With Conversion Times Too Close Together | 2-12 |
| More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation | 2-12 |
| More than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation | 2-13 |
| More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs – Asynchronous Operation | 2-13 |
| System Frequency Response Correction | 2-14 |
| (sin x)/x Correction | 2-14 |
| (sin x)/x Roll-Off for a Zero-Order Hold Function | 2-14 |
| Correction Filter | 2-15 |
| Correction Results | 2-15 |
| TMS320 Software Requirements | 2-16 |
| Specifications | 3-1 |
| Absolute Maximum Ratings | 3-1 |
| Recommended Operating Conditions | 3-1 |
| Electrical Characteristics | 3-2 |
| total device | 3-2 |
| power supply rejection and crosstalk attenuation | 3-2 |
| serial port | 3-2 |
| receive amplifier input | 3-2 |
| transmit filter output | 3-3 |
| receive and transmit system distortion specifications | 3-3 |
| receive channel signal-to-distortion ratio | 3-3 |
| transmit channel signal-to-distortion ratio | 3-4 |
| receive and transmit gain and dynamic range | 3-4 |
| receive channel band-pass filter transfer function | 3-4 |
| receive and transmit channel low-pass filter transfer function | 3-5 |
| Operating Characteristics (Noise) | 3-5 |
| Timing Requirements | 3-6 |
| Parameter Measurement Information – Timing Diagrams | 4-1 |
| TMS32046 – Processor Interface | 4-4 |
| Typical Characteristics | 5-1 |
| Applications Information | 6-1 |

List of Illustrations

| <i>Figure</i> | | <i>Page</i> |
|---------------|--|-------------|
| 1-1 | Dual-Word (Telephone Interface) Mode | 1-4 |
| 1-2 | Word Mode | 1-5 |
| 1-3 | Byte Mode | 1-5 |
| 2-1 | Asynchronous Internal Timing Configuration | 2-3 |
| 2-2 | Primary and Secondary Communications Word Sequence | 2-8 |
| 2-3 | Reset on Power-Up Circuit | 2-11 |
| 2-4 | Conversion Times Too Close Together | 2-12 |
| 2-5 | More Than One Receive Frame Sync Between Two Transmit Frame Syncs . | 2-13 |
| 2-6 | More Than One Transmit Frame Sync Between Two Receive Frame Syncs . | 2-13 |
| 2-7 | More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs | 2-14 |
| 2-8 | First-Order Correction Filter | 2-15 |
| 4-1 | IN+ and IN- Gain Control Circuitry | 4-1 |
| 4-2 | Dual-Word (Telephone Interface) Mode Timing | 4-2 |
| 4-3 | Word Timing | 4-2 |
| 4-4 | Byte-Mode Timing | 4-3 |
| 4-5 | Shift-Clock Timing | 4-4 |
| 4-6 | TMS32010/TMS320C15-TLC32046 Interface Circuit | 4-4 |
| 4-7 | TMS32010/TMS320C15-TLC32046 Interface Timing | 4-5 |
| 5-1 | D/A and A/D Low-Pass Filter Response Simulation | 5-1 |
| 5-2 | D/A and A/D Low-Pass Filter Response | 5-1 |
| 5-3 | D/A and A/D Low-Pass Group Delay | 5-2 |
| 5-4 | A/D Band-Pass Response | 5-2 |
| 5-5 | A/D Band-Pass Filter Response Simulation | 5-3 |
| 5-6 | A/D Band-Pass Filter Group Delay | 5-3 |
| 5-7 | A/D Channel High-Pass Filter | 5-4 |
| 5-8 | D/A (sin x)/x Correction Filter Response | 5-4 |
| 5-9 | D/A (sin x)/x Correction Filter Response | 5-5 |
| 5-10 | D/A (sin x)/x Correction Error | 5-5 |
| 5-11 | A/D Band-Pass Group Delay | 5-6 |
| 5-12 | D/A Low-Pass Group Delay | 5-6 |
| 5-13 | A/D Signal-to-Distortion Ratio vs Input Signal | 5-7 |
| 5-14 | A/D Gain Tracking | 5-7 |
| 5-15 | D/A Converter Signal-to-Distortion Ratio vs Input Signal | 5-8 |
| 5-16 | D/A Gain Tracking | 5-8 |

List of Illustrations (continued)

| <i>Figure</i> | | <i>Page</i> |
|---------------|---|-------------|
| 5-17 | A/D Second Harmonic Distortion vs Input Signal | 5-9 |
| 5-18 | D/A Second Harmonic Distortion vs Input Signal | 5-9 |
| 5-19 | A/D Third Harmonic Distortion vs Input Signal | 5-10 |
| 5-20 | D/A Third Harmonic Distortion vs Input Signal | 5-10 |
| 6-1 | AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode | 6-1 |
| 6-2 | External Reference Circuit for TLC32046 | 6-1 |

List of Tables

| <i>Table</i> | | <i>Page</i> |
|--------------|--|-------------|
| 2-1 | Mode-Selection Function Table | 2-1 |
| 2-2 | Primary DX Serial Communication Protocol | 2-9 |
| 2-3 | Secondary DX Serial Communication Protocol | 2-10 |
| 2-4 | AIC Responses to Improper Conditions | 2-12 |
| 2-5 | (sin x)/x Roll-Off Error | 2-15 |
| 2-6 | (sin x)/x Correction Table for $f_s = 8000$ Hz and $f_s = 9600$ Hz | 2-16 |
| 4-1 | Gain Control Table | 4-1 |

Introduction

The TLC32046 wide-band analog interface circuit (AIC) is a complete analog-to-digital and digital-to-analog interface system for advanced digital signal processors (DSPs) similar to the TMS32020, TMS320C25, and TMS320C30. The TLC32046 offers a powerful combination of options under DSP control: three operating modes (dual-word [telephone interface], word, and byte) combined with two word formats (8 bits and 16 bits) and synchronous or asynchronous operation. It provides a high level of flexibility in that conversion and sampling rates, filter bandwidths, input circuitry, receive and transmit gains, and multiplexed analog inputs are under processor control.

This AIC features a

- band-pass switched-capacitor antialiasing input filter
- 14-bit-resolution A/D converter
- 14-bit-resolution D/A converter
- low-pass switched-capacitor output-reconstruction filter.

The antialiasing input filter comprises eighth-order and fourth-order CC-type (Chebyshev/elliptic transitional) low-pass and high-pass filters, respectively. The input filter is implemented in switched-capacitor technology and is preceded by a continuous time filter to eliminate any possibility of aliasing caused by sampled data filtering. When low-pass filtering is desired, the high-pass filter can be switched out of the signal path. A selectable auxiliary differential analog input is provided for applications where more than one analog input is required.

The output-reconstruction filter is an eighth-order CC-type (Chebyshev/elliptic transitional low-pass filter) followed by a second-order $(\sin x)/x$ correction filter and is implemented in switched-capacitor technology. This filter is followed by a continuous-time filter to eliminate images of the sample data signal. The on-board $(\sin x)/x$ correction filter can be switched out of the signal path using digital signal processor control.

The A/D and D/A architectures ensure no missing codes and monotonic operation. An internal voltage reference is provided to ease the design task and to provide complete control over the performance of the IC. The internal voltage reference is brought out to pin 8. Separate analog and digital voltage supplies and ground are provided to minimize noise and ensure a wide dynamic range. The analog circuit path contains only differential circuitry to keep noise to a minimum. The exception is the DAC sample-and-hold, which utilizes pseudo-differential circuitry.

The TLC32046C is characterized for operation from 0°C to 70°C, and the TLC32046I is characterized for operation from –40°C to 85°C.

Features

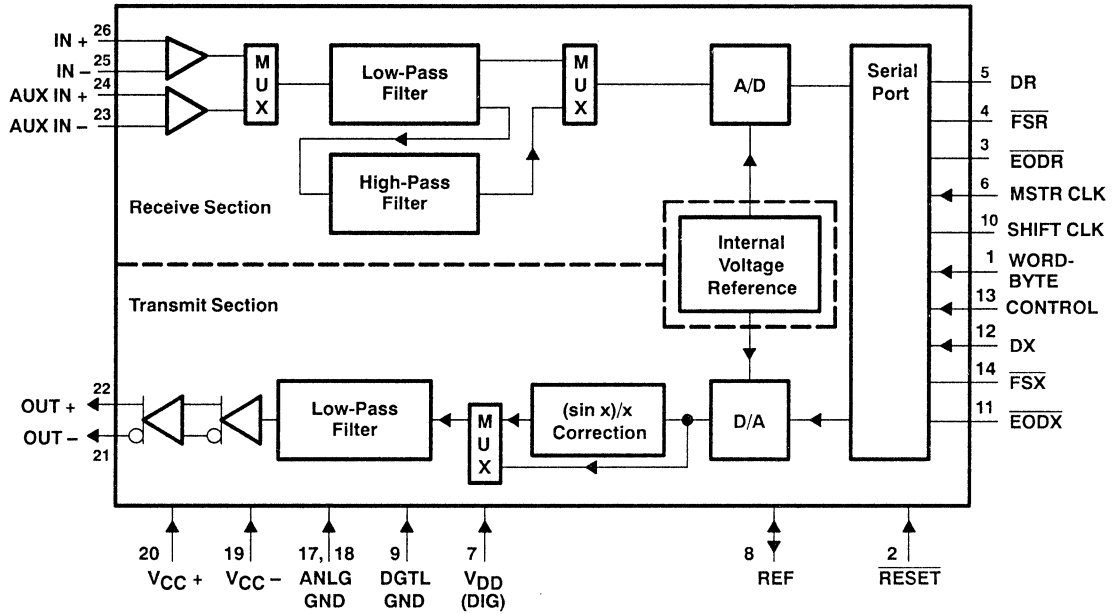
- **Advanced LinCMOS™ Silicon-Gate Process Technology**
- **14-Bit Dynamic Range ADC and DAC**
- **16-Bit Dynamic Range Input With Programmable Gain**
- **Synchronous or Asynchronous ADC and DAC Sampling Rates Up to 25,000 Samples Per Second**
- **Programmable Incremental ADC and DAC Conversion Timing Adjustments**
- **Typical Applications**
 - **Speech Encryption for Digital Transmission**
 - **Speech Recognition and Storage Systems**
 - **Speech Synthesis**
 - **Modems at 8-kHz, 9.6-kHz, and 16-kHz Sampling Rates**
 - **Industrial Process Control**
 - **Biomedical Instrumentation**
 - **Acoustical Signal Processing**
 - **Spectral Analysis**
 - **Instrumentation Recorders**
 - **Data Acquisition**
- **Switched-Capacitor Antialiasing Input Filter and Output-Reconstruction Filter**
- **Three Fundamental Modes of Operation: Dual-Word (Telephone Interface), Word, and Byte**
- **600-mil Wide N Package**
- **Digital Output in Twos Complement Format**

FUNCTION TABLE

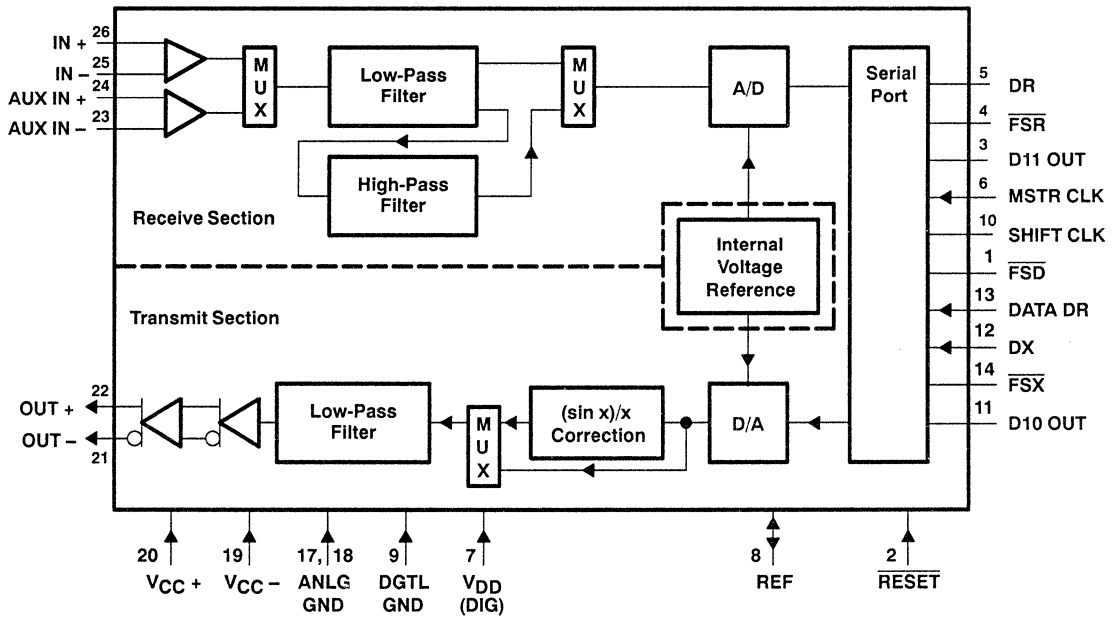
| DATA COMMUNICATIONS FORMAT | SYNCHRONOUS (CONTROL REGISTER BIT D5 = 1) | ASYNCHRONOUS (CONTROL REGISTER BIT D5 = 0) | FORCING CONDITION | DIRECT INTERFACE |
|------------------------------------|---|--|---|--|
| 16-bit format | Dual-word (telephone interface) mode | Dual-word (telephone interface) mode | Pin 13 = 0 to 5 V Pin 1 = 0 to 5 V | TMS32020, TMS320C25, TMS320C30 |
| 16-bit format | Word mode | Word mode | Pin 13 = V_{CC-} (-5 V nom) Pin 1 = V_{CC+} (+5 V nom) | TMS32020, TMS320C25, TMS320C30, indirect interface to TMS320C10. (see Figure 7). |
| 8-bit format (2 bytes required) | Byte mode | Byte mode | Pin 13 = V_{CC-} (-5 V nom) Pin 1 = V_{CC-} (-5 V nom) | TMS320C17 |

Functional Block Diagrams

WORD OR BYTE MODE



DUAL-WORD (TELEPHONE INTERFACE) MODE



FRAME SYNCHRONIZATION FUNCTIONS

| TLC32046 Function | Frame Sync Output |
|--|-------------------------------------|
| Receiving serial data on DX from processor to internal DAC | $\overline{\text{FSX}}$ low |
| Transmitting serial data on DR from internal ADC to processor, primary communications | $\overline{\text{FSR}}$ low |
| Transmitting serial data on DR from Data DR (pin 13) to processor, secondary communications in dual-word (telephone interface) mode only | $\overline{\text{FSD}}$ (pin 1) low |

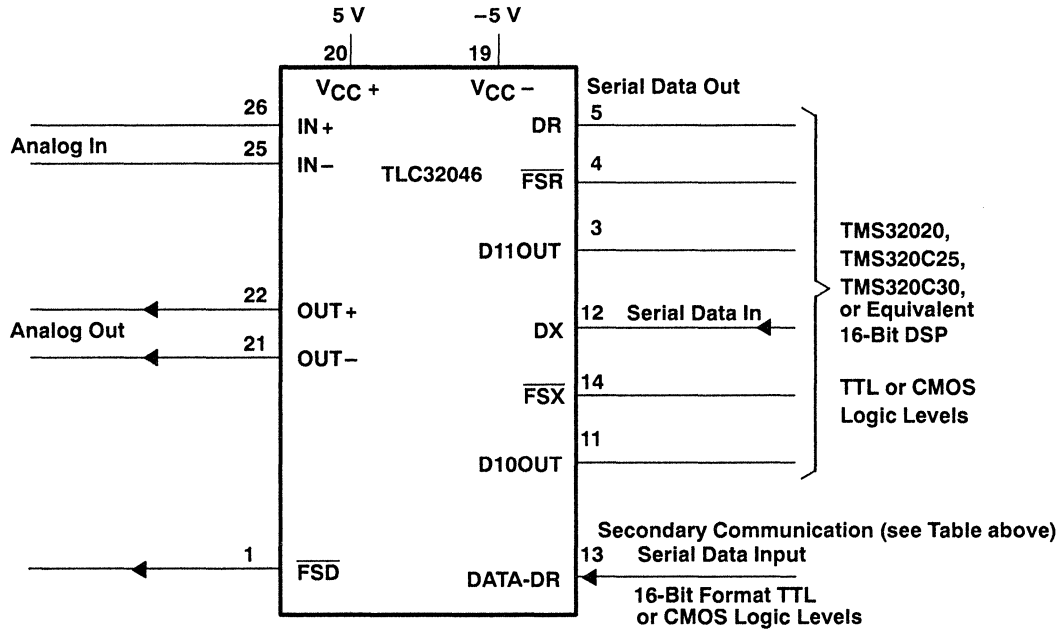


Figure 1-1. Dual-Word (Telephone Interface) Mode

When the DATA-DR/CONTROL input (pin 13) is tied to a logic signal source varying between 0 and 5 V, the TLC32046 is in the dual-word (telephone interface) mode. This logic signal is routed to the DR line for input to the DSP only when pin 1, data frame synchronization ($\overline{\text{FSD}}$), outputs a low level. The $\overline{\text{FSD}}$ pulse duration is 16 shift clock pulses. Also, in this mode, the control register data bits D10 and D11 appear on pins 11 and 3, respectively, as outputs.

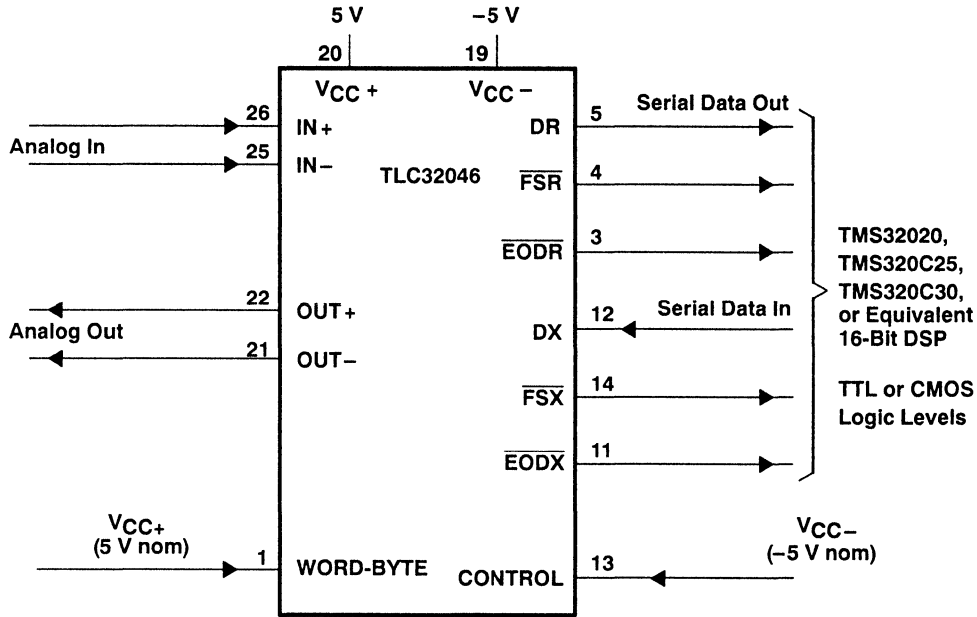


Figure 1-2. Word Mode

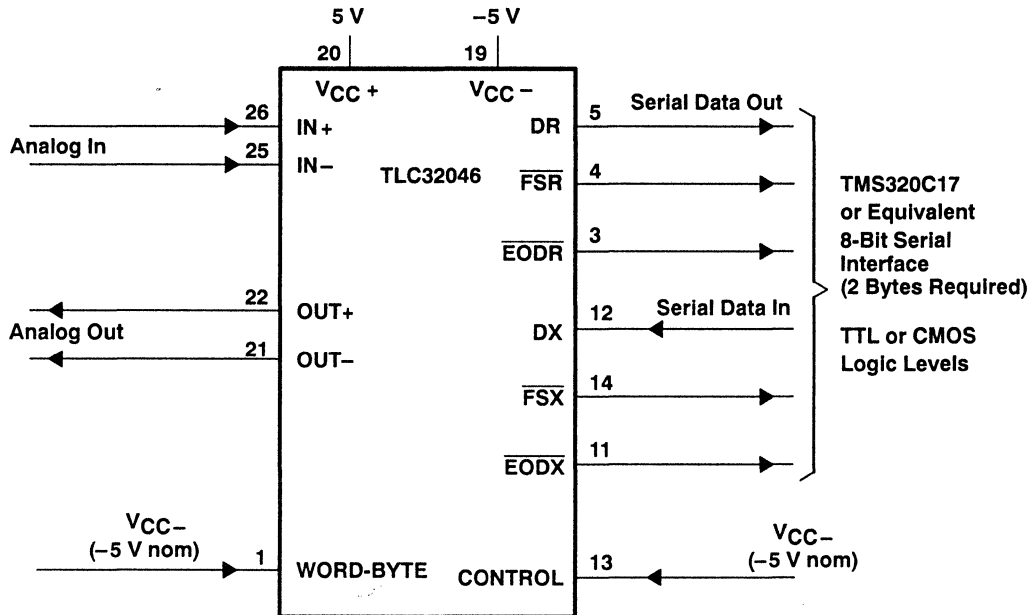
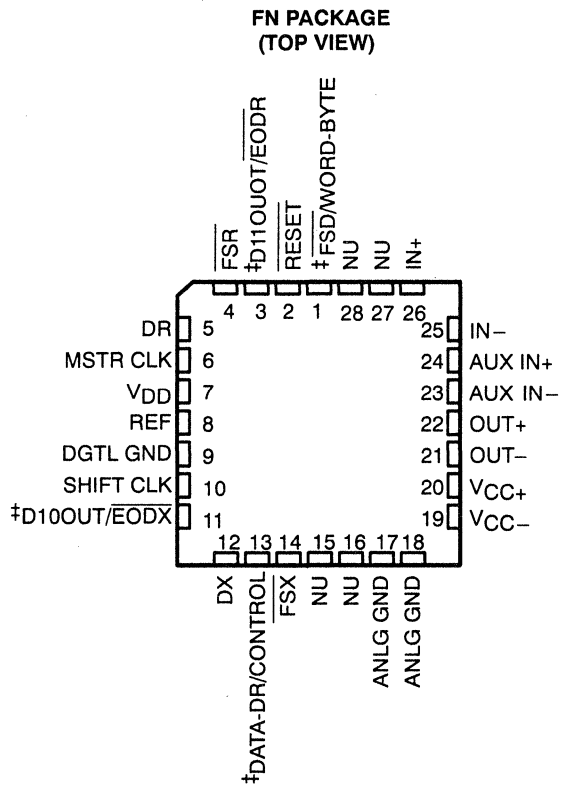
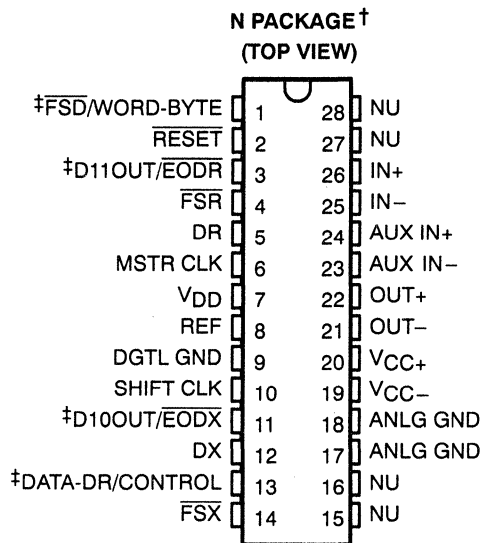


Figure 1-3. Byte Mode

The word or byte mode is selected by first connecting the DATA-DR/CONTROL input (pin 13) to V_{CC-} . $\overline{\text{FSR}}$ /WORD-BYTE (pin 1) becomes an input and can then be used to select either word or byte transmission formats. The end-of-data transmit (EODX) and the end-of-data receive (EODR) signals on pins 11 and 3, respectively, are used to signal the end of word or byte communication (see the Terminal Functions section).

Terminal Assignments



NU - Nonusable; no external connection should be made to these pins.

† 600-mil wide

‡ The portion of the pin name to the left of the slash is used for the Dual-Word (Telephone Interface) mode. The portion of the pin name to the right of the slash is used for Word-Byte mode.

Terminal Functions

| PIN NAME | NO. | I/O | DESCRIPTION |
|--------------------------|-------|-----|--|
| ANLG GND | 17,18 | | Analog ground return for all internal analog circuits. Not internally connected to DGTL GND. |
| AUX IN+ | 24 | I | Noninverting auxiliary analog input stage. This input can be switched into the band-pass filter and ADC path via software control. If the appropriate bit in the control register is a 1, the auxiliary inputs replace the IN+ and IN- inputs. If the bit is a 0, the IN+ and IN- inputs are used (see the DX Serial Data Word Format). |
| AUX IN- | 23 | I | Inverting auxiliary analog input (see the above AUX IN+ pin description). |
| DATA-DR | 13 | I | The dual-word (telephone interface) mode, selected by applying an input logic level between 0 and 5 V to this input, allows this pin to function as a data input. The data is then framed by the $\overline{\text{FSD}}$ signal and transmitted as an output to the DR line during secondary communication. The functions $\overline{\text{FSD}}$ (pin 1), D11OUT (pin 3), and D10OUT (pin 11) are valid with this mode selection (see Table 2-1). |
| CONTROL | | | When this input is tied to V_{CC-} , the device is in the word or byte mode. The functions WORD-BYTE (pin 1), $\overline{\text{EODR}}$ (pin 3), and $\overline{\text{EODX}}$ (pin 11) are valid in this mode. Pin 1 is then used to select either the word or byte mode (see Function Table). |
| DR | 5 | O | This pin is used to transmit the ADC output bits from the AIC to the TMS320 serial port. This transmission of bits from the AIC to the TMS320 serial port is synchronized with the SHIFT CLK (pin 10) signal. |
| DX | 12 | I | This pin is used to receive the DAC input bits and timing and control information from the TMS320. This serial transmission from the TMS320 serial port is synchronized with the SHIFT CLK (pin 10) signal. |
| D10OUT | 11 | O | In the dual-word (telephone interface) mode, bit D10 of the Control Register is output to this pin. When the device is reset, bit D10 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D10. |
| $\overline{\text{EODX}}$ | | | End of Data Transmit. During the word-mode timing, a low-going pulse occurs on this output immediately after the 16 bits of DAC and control or register information have been transmitted from the TMS320 serial port to the AIC. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the TMS320 serial port to the AIC and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate first and second bytes. |
| D11OUT | 3 | O | In the dual-word (telephone interface) mode, bit D11 of the control register is output to this pin. When the device is reset, bit D11 is initialized to 0 (see DX Serial Data Word Format). The output update is immediate upon changing bit D11. |
| $\overline{\text{EODR}}$ | | | End of Data Receive. During the word-mode timing, a low-going pulse occurs on this output immediately after the 16 bits of A/D information have been transmitted from the AIC to the TMS320 serial port. This signal can be used to interrupt a microprocessor upon completion of serial communications. Also, this signal can be used to strobe and enable external serial-to-parallel shift registers, latches, or external FIFO RAM, and to facilitate parallel data bus communications between the DSP and the serial-to-parallel shift registers. During the byte-mode timing, this signal goes low after the first byte has been transmitted from the AIC to the TMS320 serial port and is kept low until the second byte has been transmitted. The TMS320C17 can use this low-going signal to differentiate between first and second bytes. |

Terminal Functions (continued)

| PIN NAME | NO. | I/O | DESCRIPTION |
|-------------------------|-----|-----|---|
| DGTL | 9 | | Digital ground for all internal logic circuits. Not internally connected to ANLG GND. |
| FSD | 1 | O | Frame Sync Data. The $\overline{\text{FSD}}$ output remains high during primary communication. In the dual-word (telephone interface) mode, the $\overline{\text{FSD}}$ output is identical to the FSX output during secondary communication. |
| WORD-BYTE | | I | The WORD-BYTE pin allows differentiation between the word and byte data format (see DATA-DR/CONTROL (pin 13) and Table 2-1 for details). |
| FSR | 4 | O | Frame Sync Receive. The $\overline{\text{FSR}}$ pin is held low during bit transmission. When the $\overline{\text{FSR}}$ pin goes low, the TMS320 serial port begins receiving bits from the AIC via the DR pin of the AIC. The most significant DR bit is present on the DR pin before $\overline{\text{FSR}}$ goes low. See Serial Port Sections and Internal Timing Configuration Diagrams. |
| $\overline{\text{FSX}}$ | 14 | O | Frame Sync Transmit. When this pin goes low, the TMS320 serial port begins transmitting bits to the AIC via the DX pin of the AIC. The $\overline{\text{FSX}}$ pin is held low during bit transmission (see Serial Port Sections and Internal Timing Configuration Diagrams). |
| IN+ | 26 | I | Noninverting input to analog input amplifier stage |
| IN- | 25 | I | Inverting input to analog input amplifier stage |
| MSTR CLK | 6 | I | The master clock signal is used to derive all the key logic signals of the AIC, such as the shift clock, the switched-capacitor filter clocks, and the A/D and D/A timing signals. The Internal Timing Configuration diagram shows how these key signals are derived. The frequencies of these signals are synchronous submultiples of the master clock frequency to eliminate unwanted aliasing when the sampled analog signals are transferred between the switched-capacitor filters and the ADC and DAC converters (see the Internal Timing Configuration). |
| OUT+ | 22 | O | Noninverting output of analog output power amplifier. Drives transformer hybrids or high-impedance loads directly in a differential or a single-ended configuration. |
| OUT- | 21 | O | Inverting output of analog output power amplifier. Functionally identical with and complementary to OUT+. |
| REF | 8 | I/O | The internal voltage reference is brought out on this pin. An external voltage reference can be applied to this pin to override the internal voltage reference. |
| RESET | 2 | I | A reset function is provided to initialize TA, TA', TB, RA, RA', RB (see Figure 2-1), and the control registers. This reset function initiates serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on the $\overline{\text{RESET}}$ pin, the AIC registers are initialized to provide a 16-kHz data conversion rate for a 10.368-MHz master clock input signal. The conversion rate adjust registers, TA' and RA', are reset to 1. The CONTROL register bits are reset as follows (see AIC DX Data Word Format section): D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1 The shift clock (SCLK) is held high during $\overline{\text{RESET}}$. This initialization allows normal serial-port communication to occur between the AIC and the DSP. |
| SHIFT CLK | 10 | O | The shift clock signal is obtained by dividing the master clock signal frequency by four. This signal is used to clock the serial data transfers of the AIC. |
| VDD | 7 | | Digital supply voltage, 5 V \pm 5% |
| VCC+ | 20 | | Positive analog supply voltage, 5 V \pm 5% |
| VCC- | 19 | | Negative analog supply voltage, -5 V \pm 5% |

Detailed Description

Table 2–1. Mode-Selection Function Table

| DATA-DR/ CONTROL (Pin 13) | FSD/ WORD-BYTE (Pin 1) | CONTROL REGISTER BIT (D5) | OPERATING MODE | SERIAL CONFIGURATION | DESCRIPTION |
|---------------------------------|---|---------------------------------|---------------------------------------|----------------------------------|--|
| Data in (0 to 5 V) | $\overline{\text{FSD}}$ out (0 to 5 V) | 1 | Dual-Word (Telephone Interface) | Synchronous, One 16-Bit Word | Pin functions DATA-DR (pin 13 [†]), $\overline{\text{FSD}}$ (pin 1 [†]), D11OUT (pin 3), and D10OUT (pin 11) are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but the $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication. |
| Data in (0 to 5 V) | $\overline{\text{FSD}}$ out (0 to 5 V) | 0 | Dual-Word (Telephone Interface) | Asynchronous, One 16-Bit Word | Pin functions DATA-DR (pin 13 [†]), $\overline{\text{FSD}}$ (pin 1 [†]), D11OUT (pin 3), and D10OUT (pin 11) are applicable in this configuration. $\overline{\text{FSD}}$ is asserted during secondary communication, but the $\overline{\text{FSR}}$ is not asserted. However, $\overline{\text{FSD}}$ remains high during primary communication. If secondary communications occur while the A/D conversion is being transmitted from the DR (pin 5), $\overline{\text{FSD}}$ cannot go low, and data from the DATA-DR pin cannot go onto the DR pin (pin 5). |
| V_{CC-} | V_{CC+} | 1 | WORD | Synchronous, One 16-Bit Word | Pin functions CONTROL (pin 13 [†]), WORD-BYTE (pin 1 [†]), $\overline{\text{EODR}}$ (pin 3), and $\overline{\text{EODX}}$ (pin 11) are applicable in this configuration. |
| | | 0 | | Asynchronous, One 16-bit Word | Pin functions CONTROL (pin 13 [†]), WORD-BYTE (pin 1 [†]), $\overline{\text{EODR}}$ (pin 3), and $\overline{\text{EODX}}$ (pin 11) are applicable in this configuration. |
| | V_{CC-} | 1 | BYTE | Synchronous, Two 8-Bit Bytes | Pin functions CONTROL (pin 13 [†]), WORD-BYTE (pin 1 [†]), $\overline{\text{EODR}}$ (pin 3), and $\overline{\text{EODX}}$ (pin 11) are applicable in this configuration. |
| | | 0 | | Asynchronous, Two 8-Bit Bytes | Pin functions CONTROL (pin 13 [†]), WORD-BYTE (pin 1 [†]), $\overline{\text{EODR}}$ (pin 3), and $\overline{\text{EODX}}$ (pin 11) are applicable in this configuration. |

[†] Pin 13 has an internal pulldown resistor to -5 V, and pin 1 has an internal pullup resistor to 5 V.

Internal Timing Configuration (see Figure 2–1)

All the internal timing of the AIC is derived from the high-frequency clock signal that drives the master clock input pin. The shift clock signal, which strobes the serial port data between the AIC and DSP, is derived by dividing the master clock input signal frequency by four.

The TX(A) counter and the TX(B) counter, which are driven by the master clock signal, determine the D/A conversion timing. Similarly, the RX(A) counter and the RX(B) counter determine the A/D conversion timing. In order for the low-pass switched-capacitor filter in the D/A path (see Functional Block Diagram) to meet its transfer function specifications, the frequency of its clock input must be 288 kHz. If the clock frequency is not 288 kHz, the filter transfer function frequencies are frequency-scaled by the ratios of the clock frequency to 288 kHz:

$$\text{Absolute Frequency (kHz)} = \frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288} \quad (1)$$

For Low-Pass SCF $f_{\text{clock}} > 288$ kHz, please call the factory.

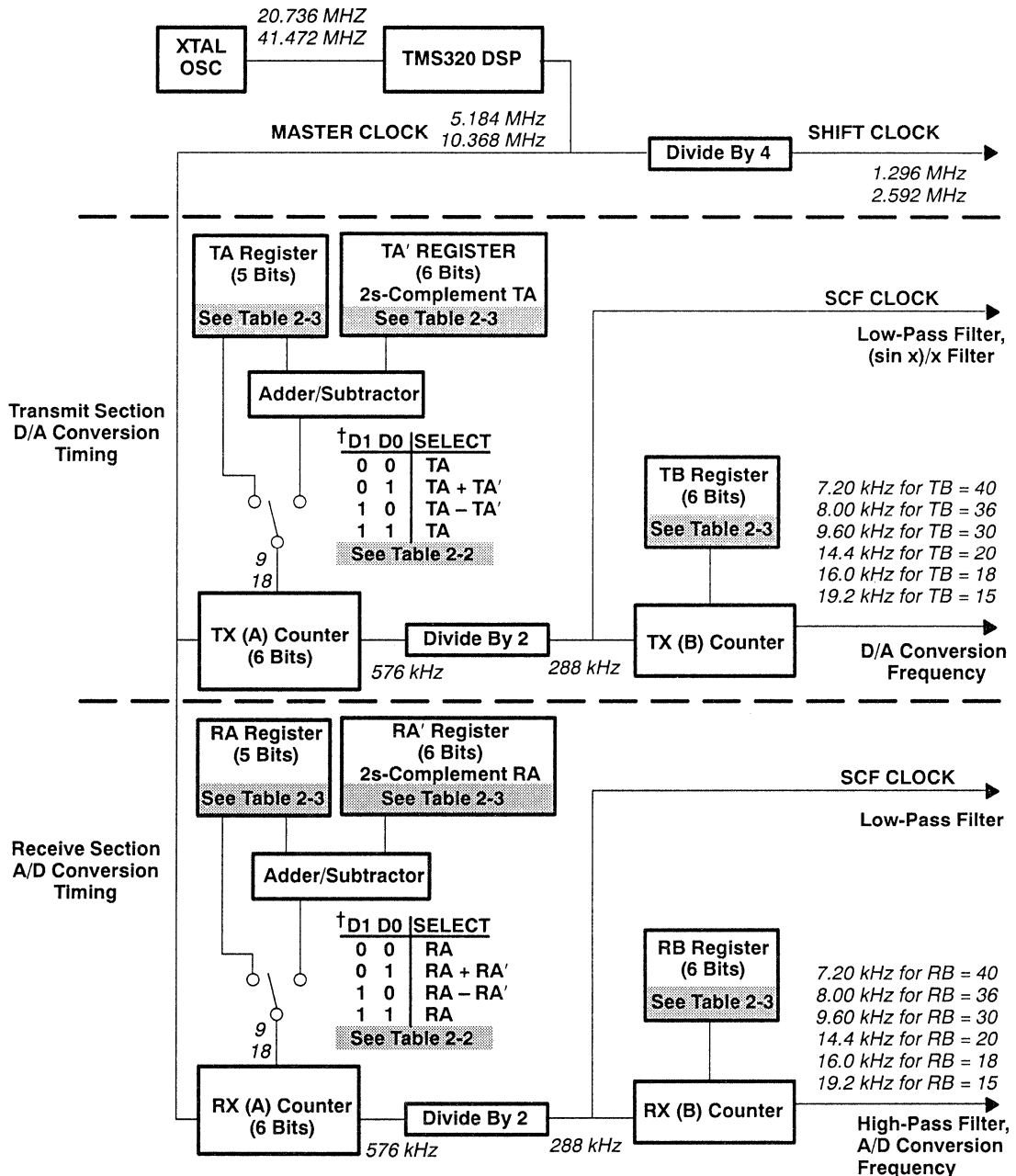
To obtain the specified filter response, the combination of master clock frequency and the TX(A) counter and the RX(A) counter values must yield a 288-kHz switched-capacitor clock signal. This 288-kHz clock signal can then be divided by the TX(B) counter to establish the D/A conversion timing.

The transfer function of the band-pass switched-capacitor filter in the A/D path (see Functional Block Diagram) is a composite of its high-pass and low-pass transfer functions. When the Shift Clock Frequency (SCF) is 288 kHz, the high-frequency roll-off of the low-pass section will meet the band-pass filter transfer function specification. Otherwise, the high-frequency roll-off will be frequency-scaled by the ratio of the high-pass section's SCF clock to 288 kHz (see Figure 5–5). The low-frequency roll-off of the high-pass section meets the band-pass filter transfer function specification when the A/D conversion rate is 16 kHz. If not, the low-frequency roll-off of the high-pass section is frequency-scaled by the ratio of the A/D conversion rate to 16 kHz.

The TX(A) counter and the TX(B) counter are reloaded each D/A conversion period, while the RX(A) counter and the RX(B) counter are reloaded every A/D conversion period. The TX(B) counter and the RX(B) counter are loaded with the values in the TB and RB registers, respectively. Via software control, the TX(A) counter can be loaded with the TA register, the TA register less the TA' register, or the TA register plus the TA' register. By selecting the TA register less the TA' register option, the upcoming conversion timing occurs earlier by an amount of time that equals TA' times the signal period of the master clock. If the TA register plus the TA' register option is executed, the upcoming conversion timing occurs later by an amount of time that equals TA' times the signal period of the master clock. Thus, the D/A conversion timing can be advanced or retarded. An identical ability to alter the A/D conversion timing is provided. However, the RX(A) counter can be programmed via software control with the RA register, the RA register less the RA' register, or the RA register plus the RA' register.

The ability to advance or retard conversion timing is particularly useful for modem applications. This feature allows controlled changes in the A/D and D/A conversion timing and can be used to enhance signal-to-noise performance, to perform frequency-tracking functions, and to generate nonstandard modem frequencies.

If the transmit and receive sections are configured to be synchronous, then the low-pass and band-pass switched-capacitor filter clocks are derived from the TX(A) counter. Also, both the D/A and A/D conversion timings are derived from the TX(A) counter and the TX(B) counter. When the transmit and receive sections are configured to be asynchronous, the RX(A) counter, RX(B) counter, RA register, RA' register, and RB registers are not used.



† These control bits are described in the DX Serial Data Word Format section.

- NOTES: A. Tables 2-2 and 2-3 (pages 2-9 and 2-10) are primary and secondary communication protocols, respectively.
 B. In synchronous operation, RA, RA', RB, RX(A), and RX(B) are not used. TA, TA', TB, TX(A), and TX(B) are used instead.
 C. Items in italics refer only to frequencies and register contents, which are variable. A crystal oscillator driving 20.736 MHz into the TMS320-series DSP will provide a master clock frequency of 5.184 MHz. The TLC32046 will produce a shift clock frequency of 1.296 MHz. If the TX(A) register contents equal 9, the SCF clock frequency will then be 288 kHz, and the D/A conversion frequency will be 288 kHz + T(B).

Figure 2-1. Asynchronous Internal Timing Configuration

Analog Input

Two pairs of analog inputs are provided. Normally, the IN+ and IN– input pair is used; however, the auxiliary input pair, AUX IN+ and AUX IN–, can be used if a second input is required. Since sufficient common-mode range and rejection are provided, each input set can be operated in differential or single-ended modes. The gain for the IN+, IN–, AUX IN+, and AUX IN– inputs can be programmed to 1, 2, or 4 (see Table 4–1). Either input circuit can be selected via software control. Multiplexing is controlled with the D4 bit (enable/disable AUX IN+ and AUX IN–) of the secondary DX word (see Table 2–3). The multiplexing requires a 2-ms wait at $SCF = 288$ kHz (see Figure 5–3) for a valid output signal. Note that a wide dynamic range is assured by the differential internal analog architecture and the separate analog and digital voltage supplies and grounds.

A/D Band-Pass Filter, A/D Band-Pass Filter Clocking, and A/D Conversion Timing

The receive-channel A/D high-pass filter can be selected or bypassed via software control (see Functional Block Diagram). The frequency response of this filter is on page 3-5. This response results when the switched-capacitor filter clock frequency is 288 kHz and the A/D sample rate is 16 kHz. Several possible options can be used to attain a 288-kHz switched-capacitor filter clock. When the filter clock frequency is not 288 kHz, the low-pass filter transfer function is frequency-scaled by the ratio of the actual clock frequency to 288 kHz (see Typical Characteristics section). The ripple bandwidth and 3-dB low-frequency roll-off points of the high-pass section are 300 Hz and 200 Hz, respectively. However, the high-pass section low-frequency roll-off is frequency-scaled by the ratio of the A/D sample rate to 16 kHz.

Figure 2–1 and the DX Serial Data Word Format sections of this data manual indicate the many options for attaining a 288-kHz band-pass switched-capacitor filter clock. These sections indicate that the RX(A) counter can be programmed to give a 288-kHz band-pass switched-capacitor filter clock for several master clock input frequencies.

The A/D conversion rate is attained by frequency-dividing the band-pass switched-capacitor filter clock with the RX(B) counter. Unwanted aliasing is prevented because the A/D conversion rate is an integer submultiple of the band-pass switched-capacitor filter sampling rate, and the two rates are synchronously locked.

A/D Converter

Fundamental performance specifications for the receive channel ADC circuitry are on pages 3-2 and 3-3 of this data manual. The ADC circuitry, using switched-capacitor techniques, provides an inherent sample-and-hold function.

Analog Output

The analog output circuitry is an analog output power amplifier. Both noninverting and inverting amplifier outputs are brought out of the IC. This amplifier can drive transformer hybrids or low-impedance loads directly in either a differential or single-ended configuration.

D/A Low-Pass Filter, D/A Low-Pass Filter Clocking, and D/A Conversion Timing

The frequency response of these filters is on page 3-5. This response results when the low-pass switched-capacitor filter clock frequency is 288 kHz (see Equation 1). Like the A/D filter, the transfer function of this filter is frequency-scaled when the clock frequency is not 288 kHz (see Typical Characteristics section). A continuous-time filter is provided on the output of the low-pass filter to eliminate the periodic sample data signal information, which occurs at multiples of the 288-kHz switched-capacitor clock feedthrough.

The D/A conversion rate is attained by frequency-dividing the 288-kHz switched-capacitor filter clock with the T(B) counter. Unwanted aliasing is prevented because the D/A conversion rate is an integer submultiple of the switched-capacitor low-pass filter sampling rate, and the two rates are synchronously locked.

D/A Converter

Fundamental performance specifications for the transmit channel DAC circuitry are on pages 3-3 and 3-4. The DAC has a sample-and-hold function that is realized with a switched-capacitor ladder.

Serial Port

The serial port has four possible configurations summarized in the Function Table on page 1-2. These configurations are briefly described below.

1. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
2. The transmit and receive sections are operated asynchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, and TMS320C30. The communications protocol is one 16-bit word.
3. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS320C17. The communications protocol is two 8-bit bytes.
4. The transmit and receive sections are operated synchronously, and the serial port interfaces directly with the TMS32020, TMS320C25, TMS320C30, or two SN74299 serial-to-parallel shift registers, which can interface in parallel to the TMS32010, TMS320C15, to any other digital signal processor, or to external FIFO circuitry. The communications protocol is one 16-bit word.

Synchronous Operation

When the transmit and receive sections are operated synchronously, the low-pass filter clock drives both low-pass and band-pass filters (see Functional Block Diagram). The A/D conversion timing is derived from and equal to the D/A conversion timing. When data bit D5 in the control register is a logic 1, transmit and receive sections are synchronous. The band-pass switched-capacitor filter and the A/D converter timing are derived from the TX(A) counter, the TX(B) counter, and the TA and TA' registers. In synchronous operation, both the A/D and the D/A channels operate from the same frequencies. The \overline{FSX} and the \overline{FSR} timing is identical during primary communication, but \overline{FSR} is not asserted during secondary communication because there is no new A/D conversion result.

One 16-Bit Word (Dual-Word [Telephone Interface] or Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and the TMS320C30, and communicates in one 16-bit word. The operation sequence is as follows:

1. The \overline{FSX} and \overline{FSR} pins are brought low by the TLC32046 AIC.
2. One 16-bit word is transmitted and one 16-bit word is received.
3. The \overline{FSX} and \overline{FSR} pins are brought high.
4. The \overline{EODX} and \overline{EODR} pins emit low-going pulses one shift clock wide. \overline{EODX} and \overline{EODR} are valid in the word or byte mode only.

If the device is in the dual-word (telephone interface) mode, \overline{FSD} goes low during the secondary communication period and enables the data word received at the DATA-DR/CONTROL input pin to be routed to the DR line. The secondary communication period occurs four shift clocks after completion of primary communications.

Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operation sequence is as follows:

1. The \overline{FSX} and \overline{FSR} pins are brought low.
2. One 8-bit word is transmitted and one 8-bit word is received.
3. The \overline{EODX} and \overline{EODR} pins are brought low.
4. The \overline{FSX} and \overline{FSR} pins emit positive frame-sync pulses that are four shift clock cycles wide.

5. One 8-bit byte is transmitted and one 8-bit byte is received.
6. The $\overline{\text{FSX}}$ and $\overline{\text{FSR}}$ pins are brought high.
7. The $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ pins are brought high.

Synchronous Operating Frequencies

The synchronous operating frequencies are determined by the following equations.

Switched capacitor filter (SCF) frequencies (see Figure 2–1):

$$\text{Low-pass SCF clock frequency (D/A and A/D channels)} = \frac{\text{master clock frequency}}{T(A) \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency}$$

$$\begin{aligned} \text{Conversion frequency (A/D and D/A channels)} &= \frac{\text{Low pass SCF clock frequency}}{T(B)} \\ &= \frac{\text{master clock frequency}}{T(A) \times 2 \times T(B)} \end{aligned}$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

Asynchronous Operation

When the transmit and the receive sections are operated asynchronously, the low-pass and band-pass filter clocks are independently generated from the master clock. The D/A and the A/D conversion timing is also determined independently.

D/A timing is set by the counters and registers described in synchronous operation, but the RA and RB registers are substituted for the TA and TB registers to determine the A/D channel sample rate and the A/D path switched-capacitor filter frequencies. Asynchronous operation is selected by control register bit D5 being zero.

One 16-Bit Word (Word Mode)

The serial port interfaces directly with the serial ports of the TMS32020, TMS320C25, and TMS320C30 and communicates with 16-bit word formats. The operation sequence is as follows:

1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pins are brought low by the TLC32046 AIC.
2. One 16-bit word is transmitted or one 16-bit word is received.
3. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pins are brought high.
4. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins emit low-going pulses one shift clock wide. $\overline{\text{EODX}}$ and $\overline{\text{EODR}}$ are valid in either the word or byte mode only.

Two 8-Bit Bytes (Byte Mode)

The serial port interfaces directly with the serial port of the TMS320C17 and communicates in two 8-bit bytes. The operating sequence is as follows:

1. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pins are brought low by the TLC32046 AIC.
2. One byte is transmitted or received.
3. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins are brought low.
4. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pins are brought high for four shift clock periods and then brought low.
5. The second byte is transmitted or received.
6. The $\overline{\text{FSX}}$ or $\overline{\text{FSR}}$ pins are brought high.
7. The $\overline{\text{EODX}}$ or $\overline{\text{EODR}}$ pins are brought high.

Asynchronous Operating Frequencies

The asynchronous operating frequencies are determined by the following equations.

Switched-capacitor filter frequencies (see Figure 2–1):

$$\text{Low-pass D/A SCF clock frequency} = \frac{\text{master clock frequency}}{T(A) \times 2}$$

$$\text{Low-pass A/D SCF clock frequency} = \frac{\text{master clock frequency}}{R(A) \times 2}$$

$$\text{High-pass SCF clock frequency (A/D channel)} = \text{A/D conversion frequency} \quad (2)$$

Conversion frequency:

$$\text{D/A conversion frequency} = \frac{\text{Low-pass D/A SCF clock frequency}}{T(B)}$$

$$\text{A/D conversion frequency} = \frac{\text{Low-pass A/D SCF clock frequency (for low pass receive filter)}}{R(B)} \quad (3)$$

NOTE: T(A), T(B), R(A), and R(B) are the contents of the TA, TB, RA, and RB registers, respectively.

Operation of TLC32046 With Internal Voltage Reference

The internal reference of the TLC32046 eliminates the need for an external voltage reference and provides overall circuit cost reduction. The internal reference eases the design task and provides complete control of the IC performance. The internal reference is brought out to pin 8. To keep the amount of noise on the reference signal to a minimum, an external capacitor can be connected between REF and ANLG GND.

Operation of TLC32046 With External Voltage Reference

The REF pin can be driven from an external reference circuit. This external circuit must be capable of supplying 250 μA and must be protected adequately from noise and crosstalk from the analog input.

Reset

A reset function is provided to initiate serial communications between the AIC and DSP and to allow fast, cost-effective testing during manufacturing. The reset function initializes all AIC registers, including the control register. After a negative-going pulse on the RESET pin, the AIC is initialized. This initialization allows normal serial port communications activity to occur between AIC and DSP (see AIC DX Data Word Format section). After RESET, TA=TB=RA=RB=18 (or 12 hexadecimal), TA'=RA'=01 (hexadecimal), the A/D high-pass filter is inserted, the loop-back function is deleted, AUX IN+ and AUX IN– pins are disabled, transmit and receive sections are in synchronous operation, programmable gain is set to 1, the on-board (sin x)/x correction filter is not selected, D10 OUT is set to 0, and D11 OUT is set to 0.

Loopback

This feature allows the circuit to be tested remotely. In loopback, the OUT+ and OUT– pins are internally connected to the IN+ and IN– pins. The DAC bits (D15 to D2), which are transmitted to the DX pin, can be compared with the ADC bits (D15 to D2), received from the DR pin. The bits on the DR pin equal the bits on the DX pin. However, there is some difference in these bits due to the ADC and DAC output offsets.

The loopback feature is implemented with digital signal processor control by transmitting a logic '1' for data bit D3 in the DX secondary communication to the control register (see Table 2–3).

Communications Word Sequence

In the Dual-Word (Telephone Interface) mode, there are two data words that are presented to the DSP or μ P from the DR terminal. The first data word is the ADC conversion result occurring during the FSR time, and the second is the serial data applied to the DATA-DR pin during the FSD time. FSR is not asserted during secondary communications and FSD is not asserted during primary communications.

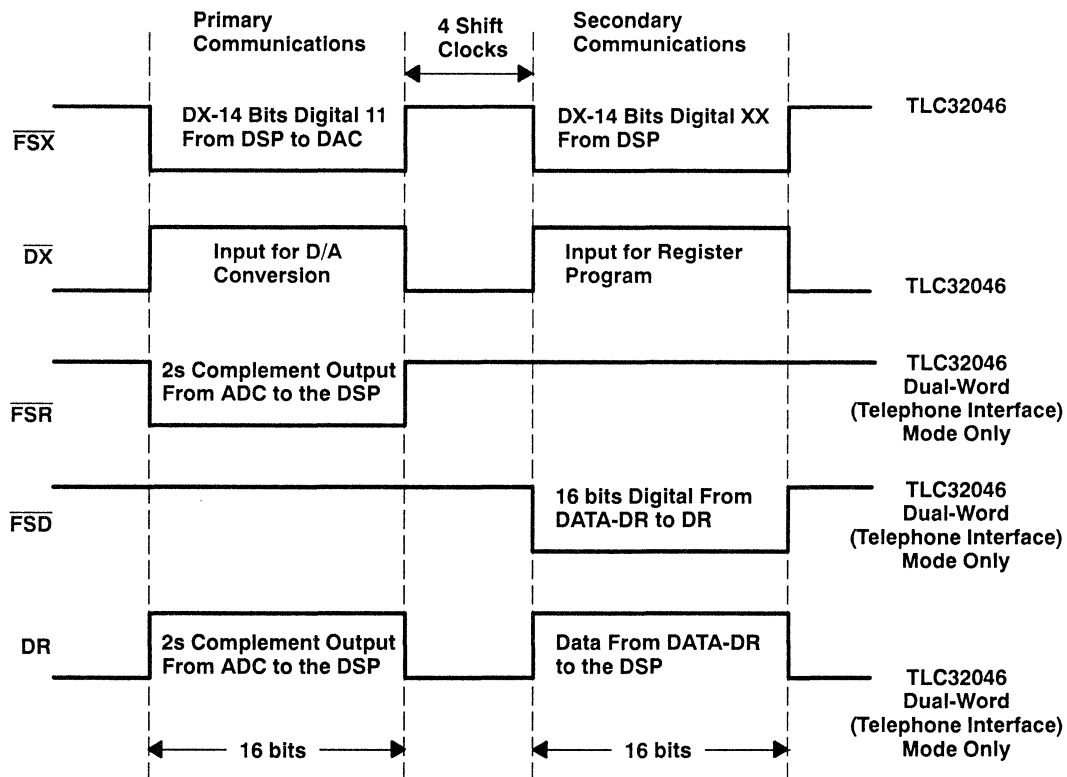
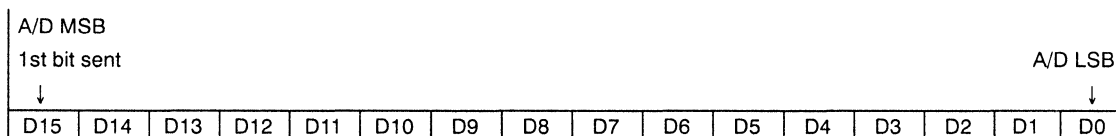


Figure 2-2. Primary and Secondary Communications Word Sequence

DR SERIAL DATA WORD FORMAT

DR Word Bit Pattern



The data word is the 14-bit conversion result of the receive channel to the processor in 2s complement format. With 16-bit processors, the data is 16 bits long with the two LSBs at zero. Using 8-bit processors, the data word is transmitted in the same order as one 16-bit word, but as two bytes with the two LSBs of the second byte set to zero.

DX SERIAL DATA WORD FORMAT

Primary DX Word Bit Pattern

| | | | | | | | | | | | | | | | |
|----------------|-----|-----|-----|-----|--------------------------|----|----|----|----|----------------|----|----|----|----|----|
| A/D OR D/A MSB | | | | | | | | | | | | | | | |
| 1st bit sent | | | | | 1st bit sent of 2nd byte | | | | | A/D or D/A LSB | | | | | |
| ↓ | | | | | | | | ↓ | | | | | ↓ | | |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Table 2-2. Primary DX Serial Communication Protocol

| FUNCTIONS | D1 | D0 |
|--|----|----|
| D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A). See Figure 2-1. TB → TX(B), RB → RX(B). See Figure 2-1. | 0 | 0 |
| D15 (MSB)-D2 → DAC Register. TA+TA' → TX(A), RA+RA' → RX(A). See Figure 2-1. TB → TX(B), RB → RX(B). See Figure 2-1. The next D/A and A/D conversion period will be changed by the addition of TA' and RA' master clock cycles, in which TA' and RA' can be positive, negative, or zero. Refer to Table 2-4, AIC Responses to Improper Conditions. | 0 | 1 |
| D15 (MSB)-D2 → DAC Register. TA-TA' → TX(A), RA-RA' → RX(A). See Figure 2-1. TB → TX(B), RB → RX(B). See Figure 2-1. The next D/A and A/D conversion period will be changed by the subtraction of TA' and RA' master clock cycles, in which TA' and RA' can be positive, negative, or zero. Refer to Table 2-4, AIC Responses to Improper Conditions. | 1 | 0 |
| D15 (MSB)-D2 → DAC Register. TA → TX(A), RA → RX(A). See Figure 2-1. TB → TX(B), RB → RX(B). See Figure 2-1. After a delay of four shift cycles, a secondary transmission follows to program the AIC to operate in the desired configuration. In the telephone interface mode, data on DATA DR (pin 13) is routed to DR (Serial Data Output) during secondary transmission. | 1 | 1 |

NOTE: Setting the two least significant bits to 1 in the normal transmission of DAC information (primary communications) to the AIC initiates secondary communications upon completion of the primary communications. When the primary communication is complete, \overline{FSX} remains high for four SHIFT CLOCK cycles and then goes low and initiates the secondary communication. The timing specifications for the primary and secondary communications are identical. In this manner, the secondary communication, if initiated, is interleaved between successive primary communications. This interleaving prevents the secondary communication from interfering with the primary communications and DAC timing. This prevents the AIC from skipping a DAC output. It is important to note that \overline{FSR} is not asserted during secondary communications activity. However, in the dual-word (telephone interface) mode, \overline{FSD} is asserted during secondary communications but not during primary communications.

Secondary DX Word Bit Pattern

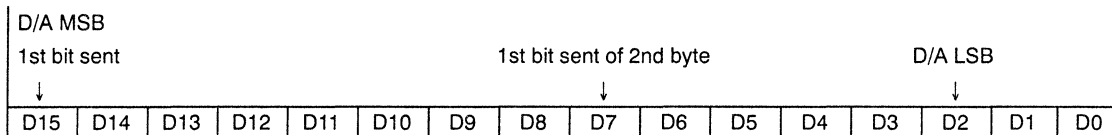


Table 2-3. Secondary DX Serial Communication Protocol

| FUNCTIONS | D1 | D0 |
|--|----|----|
| D13 (MSB)-D9 → TA, 5 bits unsigned binary. See Figure 2-1. D6 (MSB)-D2 → RA, 5 bits unsigned binary. See Figure 2-1. D15, D14, D8, and D7 are unassigned. | 0 | 0 |
| D14 (sign bit)-D9 → TA', 6 bits 2s complement. See Figure 2-1. D7 (sign bit)-D2 → RA', 6 bits 2s complement. See Figure 2-1. D15 and D8 are unassigned. | 0 | 1 |
| D14 (MSB)-D9 → TB, 6 bits unsigned binary. See Figure 2-1. D7 (MSB)-D2 → RB, 6 bits unsigned binary. See Figure 2-1. D15 and D8 are unassigned. | 1 | 0 |
| D2 = 0/1 deletes/inserts the A/D high-pass filter. D3 = 0/1 deletes/inserts the loopback function. D4 = 0/1 disables/enables the AUX IN+ and AUX IN- pins. D5 = 0/1 asynchronous/synchronous transmit and receive sections. D6 = 0/1 gain control bits (see Table 4-1). D7 = 0/1 gain control bits (see Table 4-1). D9 = 0/1 delete/insert on-board second-order (sinx)/x correction filter D10 = 0/1 output to D10OUT (dual-word (telephone interface) mode) D11 = 0/1 output to D11OUT (dual-word (telephone interface) mode) D8, D12-D15 are unassigned. | 1 | 1 |

Reset Function

A reset function is provided to initiate serial communications between the AIC and DSP. The reset function initializes all AIC registers, including the control register. After power has been applied to the AIC, a negative-going pulse on the **RESET** pin initializes the AIC registers to provide a 16-kHz A/D and D/A conversion rate for a 10.368-MHz master clock input signal. Also, the pass-bands of the A/D and D/A filters are 300 Hz to 7200 Hz and 0 Hz to 7200 Hz, respectively. Therefore, the filter bandwidths are half those shown in the filter transfer function specification section. The AIC, excepting the CONTROL register, is initialized as follows (see AIC DX Data Word Format section):

| | | | | | | |
|--------------------------------|-----------|------------|-----------|-----------|------------|-----------|
| REGISTER | TA | TA' | TB | RA | RA' | RB |
| INITIALIZED VALUE (HEX) | 12 | 01 | 12 | 12 | 01 | 12 |

The CONTROL register bits are reset as follows (see Table 2-3):

D11 = 0, D10 = 0, D9 = 1, D7 = 1, D6 = 1, D5 = 1, D4 = 0, D3 = 0, D2 = 1

This initialization allows normal serial port communications to occur between the AIC and the DSP. If the transmit and receive sections are configured to operate synchronously and the user wishes to program different conversion rates, only the TA, TA', and TB register need to be programmed. Both transmit and receive timing are synchronously derived from these registers (see the Terminal Functions and DX Serial Data Word Format sections).

Figure 2-3 shows a circuit that provides a reset on power-up when power is applied in the sequence given in the Power-Up Sequence section. The circuit depends on the power supplies reaching their recommended values a minimum of 800 ns before the capacitor charges to 0.8 V above DGTL GND.

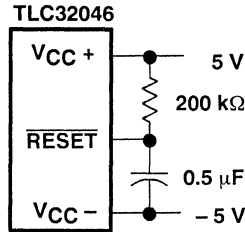


Figure 2–3. Reset on Power-Up Circuit

Power-Up Sequence

To ensure proper operation of the AIC and as a safeguard against latch-up, it is recommended that Schottky diodes with forward voltages less than or equal to 0.4 V be connected from V_{CC-} to ANLG GND and from V_{CC-} to DGTL GND. In the absence of such diodes, power is applied in the following sequence: ANLG GND and DGTL GND, V_{CC-} , then V_{CC+} and V_{DD} . Also, no input signal is applied until after power-up.

AIC Register Constraints

The following constraints are placed on the contents of the AIC registers:

1. TA register must be ≥ 4 in word mode (WORD/BYTE= High).
2. TA register must be ≥ 5 in byte mode (WORD/BYTE= Low).
3. TA' register can be either positive, negative, or zero.
4. RA register must be ≥ 4 in word mode (WORD/BYTE = High).
5. RA register must be ≥ 5 in byte mode (WORD/BYTE = Low).
6. RA' register can be either positive, negative, or zero.
7. (TA register \pm TA' register) must be > 1 .
8. (RA register \pm RA' register) must be > 1 .
9. TB register must be ≥ 15 .
10. RB register must be ≥ 15 .

AIC Responses to Improper Conditions

The AIC has provisions for responding to improper conditions. These improper conditions and the response of the AIC to these conditions are presented in Table 2–4.

Table 2–4. AIC Responses to Improper Conditions

| IMPROPER CONDITION | AIC RESPONSE |
|--|--|
| TA register + TA' register = 0 or 1 TA register – TA' register = 0 or 1 | Reprogram TX(A) counter with TA register value |
| TA register + TA' register < 0 | MODULO 64 arithmetic is used to ensure that a positive value is loaded into TX(A) counter, i.e., TA register + TA' register + 40 HEX is loaded into TX(A) counter. |
| RA register + RA' register = 0 or 1 RA register – RA' register = 0 or 1 | Reprogram RX(A) counter with RA register value |
| RA register + RA' register = 0 or 1 | MODULO 64 arithmetic is used to ensure that a positive value is loaded into RX(A) counter, i.e., RA register + RA' register + 40 HEX is loaded into RX(A) counter. |
| TA register = 0 or 1 RA register = 0 or 1 | AIC is shut down. Reprogram TA or RA registers after a reset. |
| TA register < 4 in word mode TA register < 5 in byte mode RA register < 4 in word mode RA register < 5 in byte mode | The AIC serial port no longer operates. Reprogram TA or RA registers after a reset. |
| TB register < 15 | Reprogram TB register with 12 HEX |
| RB register < 15 | Reprogram RB register with 12 HEX |
| AIC and DSP cannot communicate | Hold last DAC output |

Operation With Conversion Times Too Close Together

If the difference between two successive D/A conversion frame syncs is less than 1/25 kHz, the AIC operates improperly. In this situation, the second D/A conversion frame sync occurs too quickly, and there is not enough time for the ongoing conversion to be completed. This situation can occur if the A and B registers are improperly programmed or if the A + A' register result is too small. When incrementally adjusting the conversion period via the A + A' register options, the designer should not violate this requirement. See Figure 2–4.

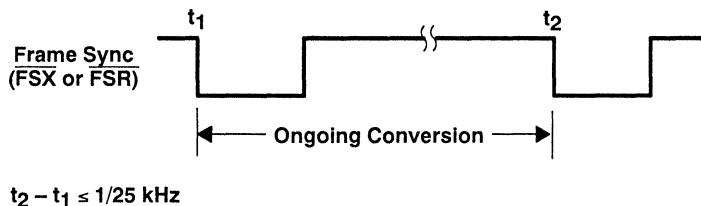


Figure 2–4. Conversion Times Too Close Together

More Than One Receive Frame Sync Occurring Between Two Transmit Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the A + A' or A – A' register options, a specific protocol is followed. The command to use the incremental conversion period adjust option is sent to the AIC during an $\overline{\text{FSX}}$ frame sync. The ongoing conversion period is then adjusted; however, either receive conversion period A or conversion period B may be adjusted. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. If there is sufficient time between t_1 and t_2 , the receive conversion period adjustment is performed during receive conversion period A. Otherwise, the adjustment is performed during receive conversion period B.

The adjustment command only adjusts one transmit conversion period and one receive conversion period. To adjust another pair of transmit and receive conversion periods, another command must be issued during a subsequent FSX frame (see Figure 2–5).

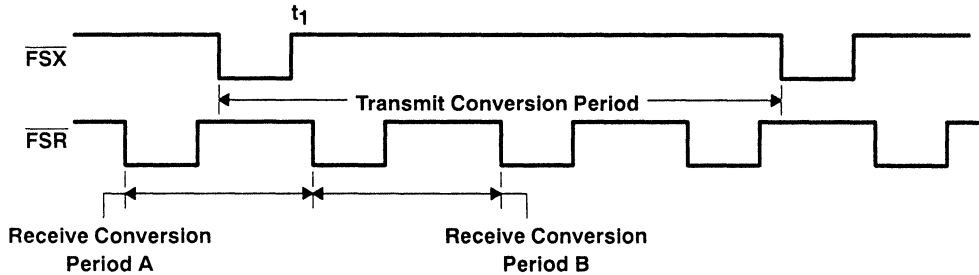


Figure 2–5. More Than One Receive Frame Sync Between Two Transmit Frame Syncs

More Than One Transmit Frame Sync Occurring Between Two Receive Frame Syncs – Asynchronous Operation

When incrementally adjusting the conversion period via the $A + A'$ or $A - A'$ register options, a specific protocol must be followed. For both transmit and receive conversion periods, the incremental conversion period adjustment is performed near the end of the conversion period. The command to use the incremental conversion period adjust options is sent to the AIC during an $\overline{\text{FSX}}$ frame sync. The ongoing transmit conversion period is then adjusted. However, three possibilities exist for the receive conversion period adjustment as shown in Figure 2–6. When the adjustment command is issued during transmit conversion period A, receive conversion period A is adjusted if there is sufficient time between t_1 and t_2 . If there is not sufficient time between t_1 and t_2 , receive conversion period B is adjusted. The third option is that the receive portion of an adjustment command can be ignored if the adjustment command is sent during a receive conversion period, which is adjusted due to a prior adjustment command. For example, if adjustment commands are issued during transmit conversion periods A, B, and C, the first two commands may cause receive conversion periods A and B to be adjusted, while the third receive adjustment command is ignored. The third adjustment command is ignored since it was issued during receive conversion period B, which already is adjusted via the transmit conversion period B adjustment command.

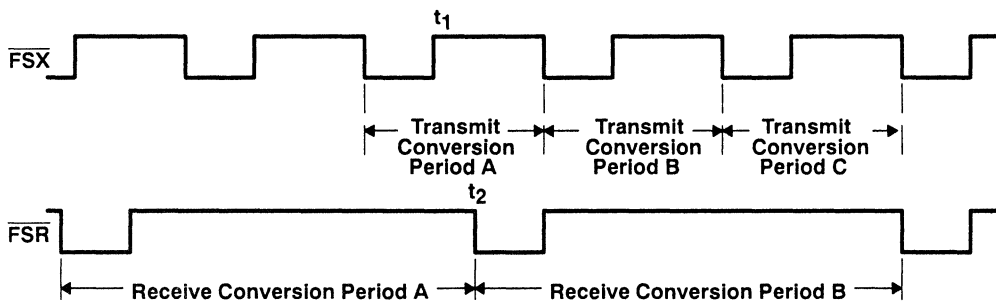


Figure 2–6. More Than One Transmit Frame Sync Between Two Receive Frame Syncs

More than One Set of Primary and Secondary DX Serial Communications Occurring Between Two Receive Frame Syncs (See DX Serial Data Word Format section) – Asynchronous Operation

The TA, TA', TB, and control register information that is transmitted in the secondary communication is accepted and applied during the ongoing transmit conversion period. If there is sufficient time between t_1

and t_2 , the TA, RA', and RB register information, sent during transmit conversion period A, is applied to receive conversion period A. Otherwise, this information is applied during receive conversion period B. If RA, RA', and RB register information has been received and is being applied during an ongoing conversion period, any subsequent RA, RA', or RB information received during this receive conversion period is disregarded. See Figure 2-7.

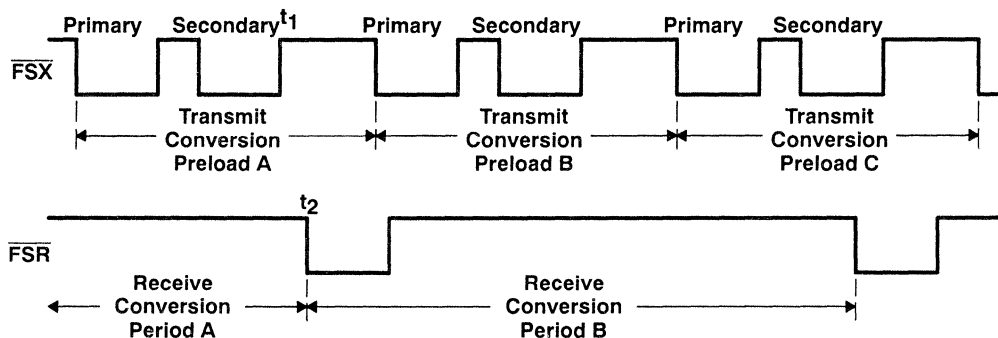


Figure 2-7. More Than One Set of Primary and Secondary DX Serial Communications Between Two Receive Frame Syncs

System Frequency Response Correction

The $(\sin x)/x$ correction for the DAC zero-order sample-and-hold output can be provided by an on-board second-order $(\sin x)/x$ correction filter (see Functional Block Diagram). This $(\sin x)/x$ correction filter can be inserted into or omitted from the signal path by digital-signal-processor control (data bit D9 in the DX secondary communications). When inserted, the $(\sin x)/x$ correction filter precedes the switched-capacitor low-pass filter. When the TB register (see Figure 2-1) equals 15, the correction results of Figures 5-8, 5-9, and 5-10 can be obtained.

The $(\sin x)/x$ correction [see section $(\sin x)/x$] can also be accomplished by disabling the on-board second-order correction filter and performing the $(\sin x)/x$ correction in digital signal processor software. The system frequency response can be corrected via DSP software to ± 0.1 dB accuracy to a band edge of 3000 Hz for all sampling rates. This correction is accomplished with a first-order digital correction filter, that requires seven TMS320 instruction cycles. With a 200-ns instruction cycle, seven instructions represent an overhead factor of 1.1% and 1.3% for sampling rates of 8 and 9.6 kHz, respectively (see the $(\sin x)/x$ Correction Section for more details).

$(\sin x)/x$ Correction

If the designer does not wish to use the on-board second-order $(\sin x)/x$ correction filter, correction can be accomplished in digital signal processor (DSP) software. $(\sin x)/x$ correction can be accomplished easily and efficiently in digital signal processor software. Excellent correction accuracy can be achieved to a band edge of 3000 Hz by using a first-order digital correction filter. The results shown below are typical of the numerical correction accuracy that can be achieved for sample rates of interest. The filter requires seven instruction cycles per sample on the TMS320 DS. With a 200-ns instruction cycle, nine instructions per sample represents an overhead factor of 1.4% and 1.7% for sampling rates of 8000 Hz and 9600 Hz, respectively. This correction adds a slight amount of group delay at the upper edge of the 300-Hz to 3000-Hz band.

$(\sin x)/x$ Roll-Off for a Zero-Order Hold Function

The $(\sin x)/x$ roll-off error for the AIC DAC zero-order hold function at a band-edge frequency of 3000 Hz for the various sampling rates is shown in Table 2-5 (see Figure 5-10).

Table 2-5. (sin x)/x Roll-Off Error

| f_s (Hz) | Error = $20 \log \frac{\sin \pi f/f_s}{\pi f/f_s}$ $f = 3000$ Hz (dB) |
|------------|---|
| 7200 | -2.64 |
| 8000 | -2.11 |
| 9600 | -1.44 |
| 14400 | -0.63 |
| 16000 | -0.50 |
| 19200 | -0.35 |
| 25000 | -0.21 |

The actual AIC (sin x)/x roll-off is slightly less than the figures above because the AIC has less than 100% duty cycle hold interval.

Correction Filter

To externally compensate for the (sin x)/x roll-off of the AIC, a first-order correction filter can be implemented as shown in Figure 2-8.

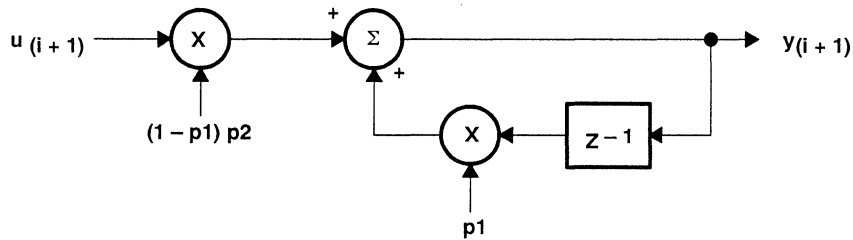


Figure 2-8. First-Order Correction Filter

The difference equation for this correction filter is:

$$y(i+1) = p2 \cdot (1-p1) \cdot u(i+1) + p1 \cdot y(i) \quad (4)$$

where the constant p1 determines the pole locations.

The resulting squared magnitude transfer function is:

$$|H(f)|^2 = \frac{(p2)^2 \cdot (1-p1)^2}{1 - 2 \cdot p1 \cdot \cos(2\pi f/f_s) + (p1)^2} \quad (5)$$

Correction Results

Table 2-6 shows the optimum p values and the corresponding correction results for 8000-Hz and 9600-Hz sampling rates (see Figures 5-8, 5-9, and 5-10).

Table 2-6. (sin x)/x Correction Table for $f_s = 8000$ Hz and $f_s = 9600$ Hz

| f (Hz) | ROLL-OFF ERROR (dB) | |
|--------|---|--|
| | $f_s = 8000$ Hz p1 = -0.14813 p2 = 0.9888 | $f_s = 9600$ Hz p1 = -0.1307 p2 = 0.9951 |
| 300 | -0.099 | -0.043 |
| 600 | -0.089 | -0.043 |
| 900 | -0.054 | 0 |
| 1200 | -0.002 | 0 |
| 1500 | 0.041 | 0 |
| 1800 | 0.079 | 0.043 |
| 2100 | 0.100 | 0.043 |
| 2400 | 0.091 | 0.043 |
| 2700 | -0.043 | 0 |
| 3000 | -0.102 | -0.043 |

TMS320 Software Requirements

The digital correction filter equation can be written in state variable form as follows:

$$Y_{(i+1)} = Y_{(i)} \cdot k1 + u_{(i+1)} \cdot k2$$

where $k1 = p1$, $k2 = (1 - p1)p2$, $y(i)$ is the filter state, and $u(i+1)$ is the next I/O sample. The coefficients $k1$ and $k2$ must be represented as 16-bit integers. The SACH instruction (with the proper shift) yields the correct result. With the assumption that the TMS320 processor page pointer and memory configuration are properly initialized, the equation can be executed in seven instructions or seven cycles with the following program:

```
ZAC
LT K2
MPY U
LTA K1
MPY Y
APAC
SACH (dma), (shift)
```

Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)

| | |
|---|----------------|
| Supply voltage range, V_{CC+} (see Note 1) | -0.3 V to 15 V |
| Supply voltage range, V_{DD} | -0.3 V to 15 V |
| Output voltage range, V_O | -0.3 V to 15 V |
| Input voltage range, V_I | -0.3 V to 15 V |
| Digital ground voltage range | -0.3 V to 15 V |
| Operating free-air temperature range: TLC32046C | 0°C to 70°C |
| TLC32046I | -40°C to 85°C |
| Storage temperature range | -40°C to 125°C |
| Case temperature for 10 seconds: FN package | 260°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package | 260°C |

NOTE 1: Voltage values for maximum ratings are with respect to V_{CC-} .

Recommended Operating Conditions

| | MIN | NOM | MAX | UNIT |
|---|-----------|-----|--------------|----------|
| Supply voltage, V_{CC+} (see Note 2) | 4.75 | 5 | 5.25 | V |
| Supply voltage, V_{CC-} (see Note 2) | -4.75 | -5 | -5.25 | V |
| Digital supply voltage, V_{DD} (see Note 2) | 4.75 | 5 | 5.25 | V |
| Digital ground voltage with respect to ANLG GND, DGTL GND | | 0 | | V |
| Reference input voltage, $V_{ref(ext)}$ (see Note 2) | 2 | | 4 | V |
| High-level input voltage, V_{IH} | 2 | | $V_{DD}+0.3$ | V |
| Low-level input voltage, V_{IL} (see Note 3) | -0.3 | | 0.8 | V |
| Load resistance at OUT+ and/or OUT-, R_L | 300 | | | Ω |
| Load capacitance at OUT+ and/or OUT-, C_L | | | 100 | pF |
| MSTR CLK frequency (see Note 4) | | 5 | 10.368 | MHz |
| Analog input amplifier common mode input voltage (see Note 5) | | | ± 1.5 | V |
| A/D or D/A conversion rate | | | 25 | kHz |
| Operating free-air temperature range, T_A | TLC32046C | 0 | 70 | °C |
| | TLC32046I | -40 | 85 | |

NOTES: 2. Voltages at analog inputs and outputs, REF, V_{CC+} , and V_{CC-} are with respect to the ANLG GND terminal. Voltages at digital inputs and outputs and V_{DD} are with respect to the DGTL GND terminal.

- The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data manual for logic voltage levels only.
- The band-pass switched-capacitor filter (SCF) specifications apply only when the low-pass section SCF clock is 288 kHz and the high-pass section SCF clock is 16 kHz. If the low-pass SCF clock is shifted from 288 kHz, the low-pass roll-off frequency shifts by the ratio of the low-pass SCF clock to 288 kHz. If the high-pass SCF clock is shifted from 16 kHz, the high-pass roll-off frequency shifts by the ratio of the high-pass SCF clock to 16 kHz. Similarly, the low-pass switched-capacitor filter (SCF) specifications apply only when the SCF clock is 288 kHz. If the SCF clock is shifted from 288 kHz, the low-pass roll-off frequency shifts by the ratio of the SCF clock to 288 kHz.
- This range applies when $(IN+ - IN-)$ or $(AUX IN+ - AUX IN-)$ equals ± 6 V.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted)

total device, MSTR CLK frequency = 5.184 MHz, outputs not loaded

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-----------------|---|---|-----|------|-----|------------|
| V_{OH} | High-level output voltage | $V_{DD} = 4.75\text{ V}$, $I_{OH} = -300\text{ }\mu\text{A}$ | 2.4 | | | V |
| V_{OL} | Low-level output voltage | $V_{DD} = 4.75\text{ V}$, $I_{OL} = 2\text{ mA}$ | | | 0.4 | V |
| I_{CC+} | Supply current from V_{CC+} | TLC32046C | | | 35 | mA |
| | | TLC32046I | | | 40 | |
| I_{CC-} | Supply current from V_{CC-} | TLC32046C | | | -35 | mA |
| | | TLC32046I | | | -40 | |
| I_{DD} | Supply current from V_{DD} | | | | 7 | mA |
| V_{ref} | Internal reference output voltage | | 3 | | 3.3 | V |
| α_{Vref} | Temperature coefficient of internal reference voltage | | | 250 | | ppm/°C |
| r_o | Output resistance at REF | | | 100 | | k Ω |

power supply rejection and crosstalk attenuation

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|--|------------------------|---|-----|------|-----|------|
| V_{CC+} or V_{CC-} supply voltage rejection ratio, receive channel | $f = 0$ to 30 kHz | Idle channel, supply signal at 200 mV p-p measured at DR (ADC output) | | 30 | | dB |
| | $f = 30$ kHz to 50 kHz | | | 45 | | |
| V_{CC+} or V_{CC-} supply voltage rejection ratio, transmit channel (single-ended) | $f = 0$ to 30 kHz | Idle channel, supply signal at 200 mV p-p measured at OUT+ | | 30 | | dB |
| | $f = 30$ kHz to 50 kHz | | | 45 | | |
| Crosstalk attenuation, transmit-to-receive (single-ended) | | | | 80 | | dB |

serial port

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-----------|--------------------------------|------------------------------------|-----|------|-----------|---------------|
| V_{OH} | High-level output voltage | $I_{OH} = -300\text{ }\mu\text{A}$ | 2.4 | | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 2\text{ mA}$ | | | 0.4 | V |
| I_I | Input current | | | | ± 10 | μA |
| I_I | Input current, DATA-DR/CONTROL | | | | ± 100 | μA |
| C_i | Input capacitance | | | 15 | | pF |
| C_o | Output capacitance | | | 15 | | pF |

† All typical values are at $T_A = 25^\circ\text{C}$.

receive amplifier input

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|--|-----------------|-----|------|-----|------------|
| A/D converter offset error (filters in) | | | | 10 | 70 | mV |
| CMRR | Common-mode rejection ratio at IN+, IN-, or AUX IN+, AUX IN- | See Note 6 | | 55 | | dB |
| r_i | Input resistance at IN+, IN-, or AUX IN+, AUX IN-, REF | | | 100 | | k Ω |

NOTE 6: The test condition is a 0-dBm, 1-kHz input signal with a 16-kHz conversion rate.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (Continued)

transmit filter output

| PARAMETER | | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|-----------|---|--|---------|------------------|-----|------|
| V_{OO} | Output offset voltage at OUT+ or OUT– (single-ended relative to ANLG GND) | | | 15 | 80 | mV |
| V_{OM} | Maximum peak output voltage swing across R_L at OUT+ or OUT– (single-ended) | $R_L \geq 300\ \Omega$, Offset voltage = 0 | ± 3 | | | V |
| V_{OM} | Maximum peak output voltage swing between OUT+ and OUT– (differential output) | $R_L \geq 600\ \Omega$ | ± 6 | | | V |

[†] All typical values are at $T_A = 25^\circ\text{C}$.

receive and transmit channel system distortion, SCF clock frequency = 288 kHz (see Note 7)

| PARAMETER | | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT | |
|---|--------------|---|---|------------------|-----|------|----|
| Attenuation of second harmonic of A/D input signal | single-ended | $V_{in} = -0.1\text{ dB to } -24\text{ dB}$ | | 70 | | dB | |
| | differential | | 62 | 70 | | | |
| Attenuation of third and higher harmonics of A/D input signal | single-ended | | | 65 | | dB | |
| | differential | | 57 | 65 | | | |
| Attenuation of second harmonic of D/A input signal | single-ended | | $V_{in} = -0\text{ dB to } -24\text{ dB}$ | | 70 | | dB |
| | differential | | | 62 | 70 | | |
| Attenuation of third and higher harmonics of D/A input signal | single-ended | | | 65 | | dB | |
| | differential | 57 | | 65 | | | |

[†] All typical values are at $T_A = 25^\circ\text{C}$.

receive channel signal-to-distortion ratio (see Note 7)

| PARAMETER | TEST CONDITIONS | $A_V = 1^\ddagger$ | | $A_V = 2^\ddagger$ | | $A_V = 4^\ddagger$ | | UNIT |
|--|--|--------------------|-----|--------------------|-----|--------------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| A/D channel signal-to-distortion ratio | $V_{in} = -6\text{ dB to } -0.1\text{ dB}$ | 58 | | § | | § | | dB |
| | $V_{in} = -12\text{ dB to } -6\text{ dB}$ | 58 | | 58 | | § | | |
| | $V_{in} = -18\text{ dB to } -12\text{ dB}$ | 56 | | 58 | | 58 | | |
| | $V_{in} = -24\text{ dB to } -18\text{ dB}$ | 50 | | 56 | | 58 | | |
| | $V_{in} = -30\text{ dB to } -24\text{ dB}$ | 44 | | 50 | | 56 | | |
| | $V_{in} = -36\text{ dB to } -30\text{ dB}$ | 38 | | 44 | | 50 | | |
| | $V_{in} = -42\text{ dB to } -36\text{ dB}$ | 32 | | 38 | | 44 | | |
| | $V_{in} = -48\text{ dB to } -42\text{ dB}$ | 26 | | 32 | | 38 | | |
| $V_{in} = -54\text{ dB to } -48\text{ dB}$ | 20 | | 26 | | 32 | | | |

[‡] A_V is the programmable gain of the input amplifier.

§ Measurements under these conditions are unreliable due to overrange and signal clipping.

NOTE 7: The test condition is a 1-kHz input signal with a 16-kHz conversion rate. The load impedance for the DAC is 600 Ω . Input and output voltages are referred to V_{ref} .

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (Continued)

transmit channel signal-to-distortion ratio (see Note 7)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--|--|-----|-----|------|
| D/A channel signal-to-distortion ratio | $V_{in} = -6\text{ dB to } -0.1\text{ dB}$ | 58 | | dB |
| | $V_{in} = -12\text{ dB to } -6\text{ dB}$ | 58 | | |
| | $V_{in} = -18\text{ dB to } -12\text{ dB}$ | 56 | | |
| | $V_{in} = -24\text{ dB to } -18\text{ dB}$ | 50 | | |
| | $V_{in} = -30\text{ dB to } -24\text{ dB}$ | 44 | | |
| | $V_{in} = -36\text{ dB to } -30\text{ dB}$ | 38 | | |
| | $V_{in} = -42\text{ dB to } -36\text{ dB}$ | 32 | | |
| | $V_{in} = -48\text{ dB to } -42\text{ dB}$ | 26 | | |
| | $V_{in} = -54\text{ dB to } -48\text{ dB}$ | 20 | | |

NOTE 7: The test condition is a 1-kHz input signal with a 16-kHz conversion rate. The load impedance for the DAC is 600 Ω . Input and output voltages are referred to V_{ref} .

receive and transmit gain and dynamic range (see Note 8)

| PARAMETER | TEST CONDITIONS | MIN | TYP [†] | MAX | UNIT |
|------------------------------|--|------------|------------------|-----|------|
| Transmit gain tracking error | $V_{out} = -48\text{ dB to } 0\text{ dB}$ signal range | ± 0.05 | ± 0.15 | | dB |
| Receive gain tracking error | $V_{in} = -48\text{ dB to } 0\text{ dB}$ signal range | ± 0.05 | ± 0.15 | | dB |

NOTE 8: Gain tracking is relative to the absolute gain at 1 kHz and 0 dB (0 dB relative to V_{ref}).

receive channel band-pass filter transfer function, SCF $f_{clock} = 288\text{ kHz}$, input (IN+ – IN–) is a $\pm 3\text{-V}$ sine wave[‡] (see Note 9)

| PARAMETER | TEST CONDITION | FREQUENCY | ADJUSTMENT | MIN | TYP [†] | MAX | UNIT |
|-------------|--------------------------------|---|-----------------------------|-------|------------------|------|------|
| Filter gain | Input signal reference is 0 dB | $f \leq 100\text{ Hz}$ | $K1 \times 0\text{ dB}$ | -33 | -29 | -25 | dB |
| | | $f = 200\text{ Hz}$ | $K1 \times -0.26\text{ dB}$ | -4 | -2 | -1 | |
| | | $f = 300\text{ Hz to } 6200\text{ Hz}$ | $K1 \times 0\text{ dB}$ | -0.25 | 0 | 0.25 | |
| | | $f = 6200\text{ Hz to } 6600\text{ Hz}$ | $K1 \times 0\text{ dB}$ | -0.3 | 0 | 0.3 | |
| | | $f = 6600\text{ Hz to } 7300\text{ Hz}$ | $K1 \times 0\text{ dB}$ | -0.5 | 0 | 0.5 | |
| | | $f = 7600\text{ Hz}$ | $K1 \times 2.3\text{ dB}$ | -5 | -2 | -0.5 | |
| | | $f = 8000\text{ Hz}$ | $K1 \times 2.7\text{ dB}$ | | -16 | -14 | |
| | | $f \geq 8800\text{ Hz}$ | $K1 \times 3.2\text{ dB}$ | | | -40 | |
| | | $f \geq 10000\text{ Hz}$ | $K1 \times 0\text{ dB}$ | | | -65 | |

[†] All typical values are at $T_A = 25^\circ\text{C}$.

[‡] The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where $K1 = 100 \cdot [(SCF\text{ frequency} - 288\text{ kHz})/288\text{ kHz}]$. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 300 Hz to 7200 Hz and 0 to 7200 Hz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$ (Unless Otherwise Noted) (Continued)

receive and transmit channel low-pass filter transfer function, SCF $f_{\text{clock}} = 288\text{ kHz}$ (see Note 9)

| PARAMETER | TEST CONDITION | FREQUENCY RANGE | ADJUSTMENT ADDEND [‡] | MIN | TYP [†] | MAX | UNIT |
|-------------|--------------------------------|------------------------|--------------------------------|-------|------------------|------|------|
| Filter gain | Input signal reference is 0 dB | f = 0 Hz to 6200 Hz | $K1 \times 0\text{ dB}$ | -0.25 | 0 | 0.25 | dB |
| | | f = 6200 Hz to 6600 Hz | $K1 \times 0\text{ dB}$ | -0.3 | 0 | 0.3 | |
| | | f = 6600 Hz to 7300 Hz | $K1 \times 0\text{ dB}$ | -0.5 | 0 | 0.5 | |
| | | f = 7600 Hz | $K1 \times 2.3\text{ dB}$ | -5 | -2 | -0.5 | |
| | | f = 8000 Hz | $K1 \times 2.7\text{ dB}$ | | -16 | -14 | |
| | | f \geq 8800 Hz | $K1 \times 3.2\text{ dB}$ | | | -40 | |
| | | f \geq 10000 Hz | $K1 \times 0\text{ dB}$ | | | -65 | |

[†] All typical values are at $T_A = 25^\circ\text{C}$.

[‡] The MIN, TYP, and MAX specifications are given for a 288-kHz SCF clock frequency. A slight error in the 288-kHz SCF may result from inaccuracies in the MSTR CLK frequency, resulting from crystal frequency tolerances. If this frequency error is less than 0.25%, the ADJUSTMENT ADDEND should be added to the MIN, TYP, and MAX specifications, where $K1 = 100 \cdot [(SCF\text{ frequency} - 288\text{ kHz})/288\text{ kHz}]$. For errors greater than 0.25%, see Note 9.

NOTE 9: The filter gain outside of the pass band is measured with respect to the gain at 1 kHz. The filter gain within the pass band is measured with respect to the average gain within the pass band. The pass bands are 300 Hz to 7200 Hz and 0 to 7200 Hz for the band-pass and low-pass filters, respectively. For switched-capacitor filter clocks at frequencies other than 288 kHz, the filter response is shifted by the ratio of switched-capacitor filter clock frequency to 288 kHz.

Operating Characteristics Over Recommended Operating Free-Air Temperature Range, $V_{CC+} = 5\text{ V}$, $V_{CC-} = -5\text{ V}$, $V_{DD} = 5\text{ V}$

receive and transmit noise (measurement includes low-pass and band-pass switched-capacitor filters)

| PARAMETER | | TEST CONDITIONS | TYP [†] | MAX | UNIT |
|-----------------------------|--|--|------------------|-----|-------------------|
| Transmit noise | broadband with (sin x)/x | DX input = 00000000000000, constant input code | 250 | 500 | $\mu\text{V rms}$ |
| | broadband without (sin x)/x | | 200 | 450 | |
| | 0 to 30 kHz with (sin x)/x | | 200 | 400 | |
| | 0 to 30 kHz without (sin x)/x | | 200 | 400 | |
| | 0 to 3.4 kHz with (sin x)/x | | 180 | 300 | |
| | 0 to 3.4 kHz without (sin x)/x | | 160 | 300 | |
| | 0 to 6.8 kHz with (sin x)/x [wide-band operation with 7.2 kHz roll-off] | | 180 | 350 | |
| | 0 to 6.8 kHz without (sin x)/x [wide-band operation with 7.2 kHz roll-off] | | 160 | 350 | |
| Receive noise (see Note 10) | | Inputs grounded, gain = 1 | 300 | 500 | $\mu\text{V rms}$ |
| | | | 18 | | dBrnc0 |

[†] All typical values are at $T_A = 25^\circ\text{C}$.

NOTE 10: The noise is computed by statistically evaluating the digital output of the A/D converter.

Timing Requirements

serial port recommended input signals

| PARAMETER | | MIN | MAX | UNIT |
|---------------------|--|----------------------|-----|------|
| $t_c(\text{MCLK})$ | Master clock cycle time | 95 | | ns |
| $t_r(\text{MCLK})$ | Master clock rise time | | 10 | ns |
| $t_f(\text{MCLK})$ | Master clock fall time | | 10 | ns |
| | Master clock duty cycle | 25% | 75% | |
| | $\overline{\text{RESET}}$ pulse duration (see Note 11) | 800 | | ns |
| $t_{su}(\text{DX})$ | DX setup time before SCLK \downarrow | 20 | | ns |
| $t_h(\text{DX})$ | DX hold time after SCLK \downarrow | $t_c(\text{SCLK})/4$ | | ns |

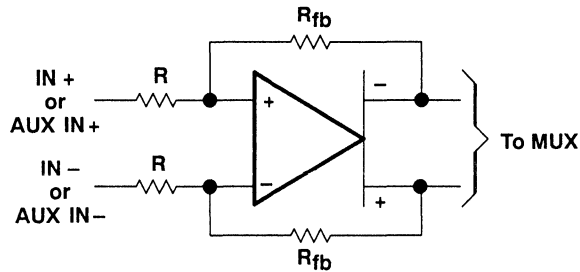
NOTE 11: $\overline{\text{RESET}}$ pulse duration is the amount of time that the reset pin is held below 0.8 V after the power supplies have reached their recommended values.

serial port – AIC output signals, $C_L = 30$ pF for SHIFT CLK output, $C_L = 15$ pF for all other outputs

| PARAMETER | | MIN | TYP [†] | MAX | UNIT |
|---------------------|---|-----|------------------|-----|------|
| $t_c(\text{SCLK})$ | Shift clock (SCLK) cycle time | 380 | | | ns |
| $t_f(\text{SCLK})$ | Shift clock (SCLK) fall time | | 3 | 8 | ns |
| $t_r(\text{SCLK})$ | Shift clock (SCLK) rise time | | 3 | 8 | ns |
| | Shift clock (SCLK) duty cycle | 45 | | 55 | % |
| $t_d(\text{CH-FL})$ | Delay from SCLK \uparrow to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}\downarrow$ | | 30 | | ns |
| $t_d(\text{CH-FH})$ | Delay from SCLK \uparrow to $\overline{\text{FSR}}/\overline{\text{FSX}}/\overline{\text{FSD}}\uparrow$ | | 35 | 90 | ns |
| $t_d(\text{CH-DR})$ | DR valid after SCLK \uparrow | | | 90 | ns |
| $t_d(\text{CH-EL})$ | Delay from SCLK \uparrow to $\overline{\text{EODX}}/\overline{\text{EODR}}\downarrow$ in word mode | | | 90 | ns |
| $t_d(\text{CH-EH})$ | Delay from SCLK \uparrow to $\overline{\text{EODX}}/\overline{\text{EODR}}\uparrow$ in word mode | | | 90 | ns |
| $t_f(\text{EODX})$ | $\overline{\text{EODX}}$ fall time | | 2 | 8 | ns |
| $t_f(\text{EODR})$ | $\overline{\text{EODR}}$ fall time | | 2 | 8 | ns |
| $t_d(\text{CH-EL})$ | Delay from SCLK \uparrow to $\overline{\text{EODX}}/\overline{\text{EODR}}\downarrow$ in byte mode | | | 90 | ns |
| $t_d(\text{CH-EH})$ | Delay from SCLK \uparrow to $\overline{\text{EODX}}/\overline{\text{EODR}}\uparrow$ in byte mode | | | 90 | ns |
| $t_d(\text{MH-SL})$ | Delay from MSTR CLK \uparrow to SCLK \downarrow | | 65 | 170 | ns |
| $t_d(\text{MH-SH})$ | Delay from MSTR CLK \uparrow to SCLK \uparrow | | 65 | 170 | ns |

[†] Typical values are at $T_A = 25^\circ\text{C}$.

Parameter Measurement Information



$$R_{fb} = R \text{ for } D6 = 1 \text{ and } D7 = 1$$

$$D6 = 0 \text{ and } D7 = 0$$

$$R_{fb} = 2R \text{ for } D6 = 1 \text{ and } D7 = 0$$

$$R_{fb} = 4R \text{ for } D6 = 0, \text{ and } D7 = 1$$

Figure 4-1. IN+ and IN- Gain Control Circuitry

Table 4-1. Gain Control Table (Analog Input Signal Required for Full-Scale Bipolar A/D Conversion Twos Complement)[†]

| INPUT CONFIGURATIONS | CONTROL REGISTER BITS | | ANALOG INPUT [‡] § | A/D CONVERSION RESULT |
|---|-----------------------|----|------------------------------|-----------------------|
| | D6 | D7 | | |
| Differential configuration Analog input = IN+ - IN- = AUX IN+ - AUX IN- | 1 | 1 | $V_{ID} = \pm 6 \text{ V}$ | \pm full scale |
| | 0 | 0 | $V_{ID} = \pm 3 \text{ V}$ | \pm full scale |
| | 1 | 0 | $V_{ID} = \pm 1.5 \text{ V}$ | \pm full scale |
| Single-ended configuration Analog input = IN+ - ANLG GND = AUX IN+ - ANLG GND | 0 | 1 | $V_I = \pm 1.5 \text{ V}$ | \pm full scale |
| | 1 | 1 | $V_I = \pm 3 \text{ V}$ | \pm half scale |
| | 0 | 0 | $V_I = \pm 3 \text{ V}$ | \pm full scale |

[†] $V_{CC+} = 5 \text{ V}$, $V_{CC-} = -5 \text{ V}$, $V_{DD} = 5 \text{ V}$

[‡] V_{ID} = Differential Input Voltage, V_I = Input voltage referenced to ground with IN- or AUX IN- connected to ground.

[§] In this example, V_{ref} is assumed to be 3 V. In order to minimize distortion, it is recommended that the analog input not exceed 0.1 dB below full scale.

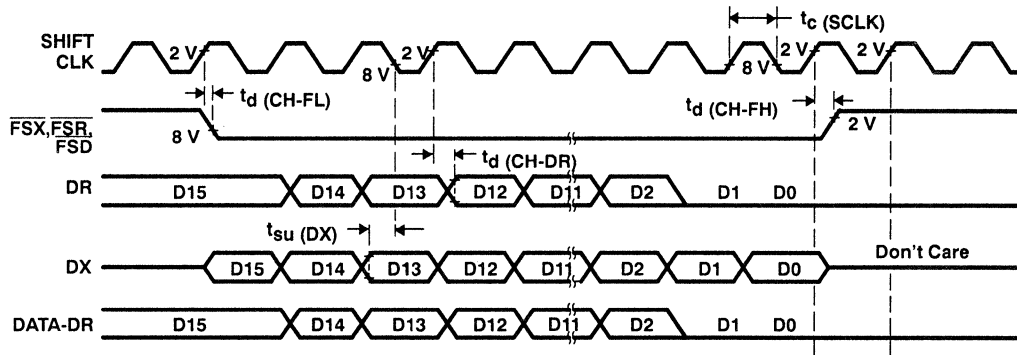


Figure 4-2. Dual-Word (Telephone Interface) Mode Timing

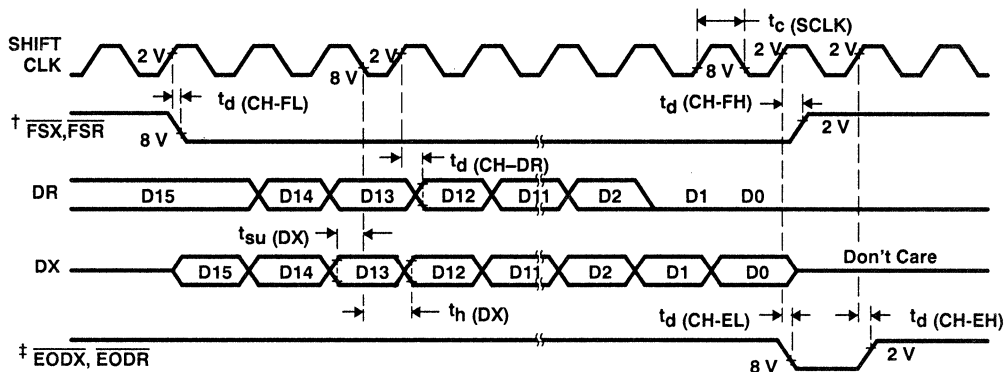


Figure 4-3. Word Timing

† The time between falling edges of \overline{FSR} is the A/D conversion period and the time between falling edges of \overline{FSX} is the D/A conversion period.

‡ In the word format, \overline{EODX} and \overline{EODR} go low to signal the end of a 16-bit data word to the processor. The word-cycle is 20 shift-clacks wide, giving a four-clock period setup time between data words.

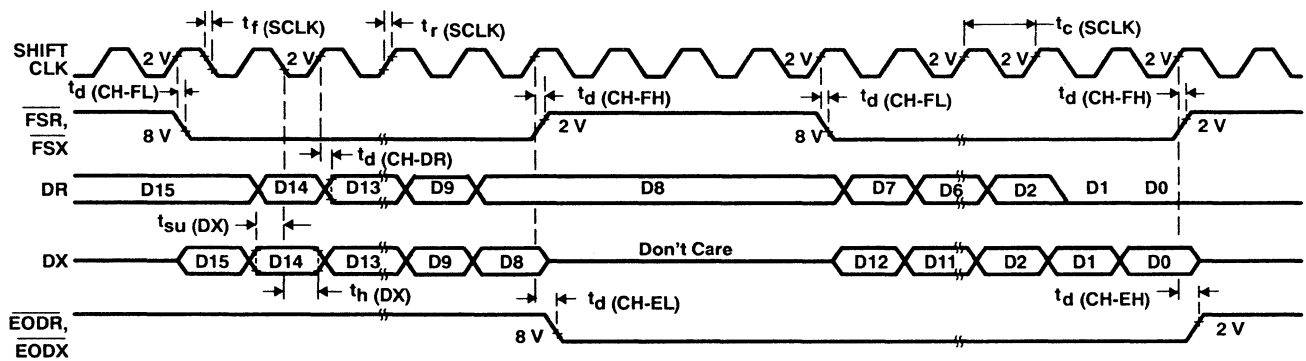


Figure 4-4. Byte-Mode Timing

† The time between falling edges of FSR is the A/D conversion period, and the time between falling edges of FSX is the D/A conversion period.

‡ In the byte mode, when EODX or EODR is high, the first byte is transmitted or received, and when these signals are low, the second byte is transmitted or received. Each byte-cycle is 12 shift-clacks long, allowing for a four-shift-clock setup time between byte transmissions.

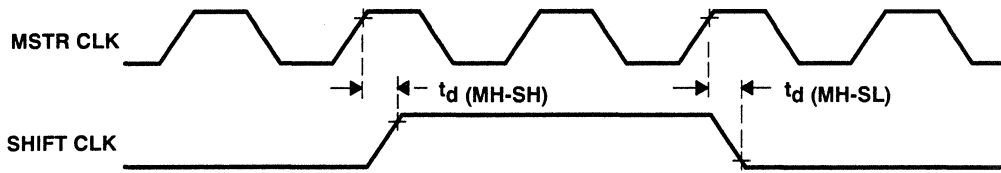


Figure 4-5. Shift-Clock Timing

TMS32046 – Processor Interface

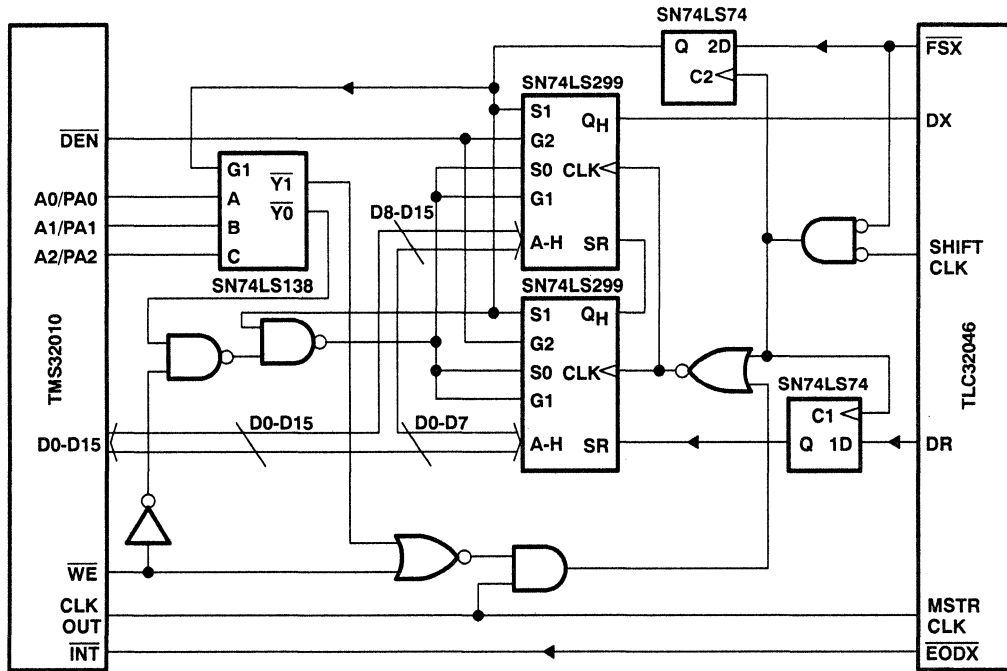
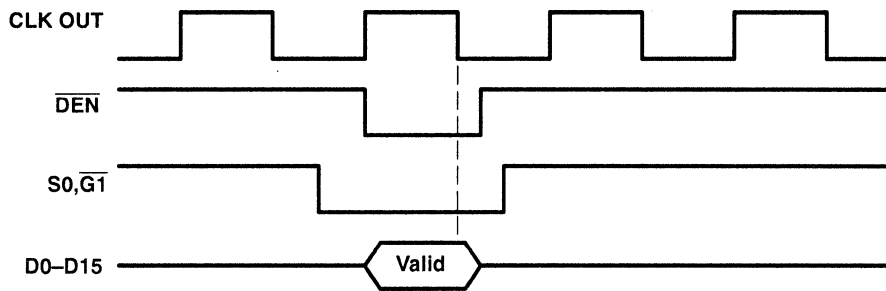


Figure 4-6. TMS32010/TMS320C15-TLC32046 Interface Circuit

IN instruction timing



OUT instruction timing

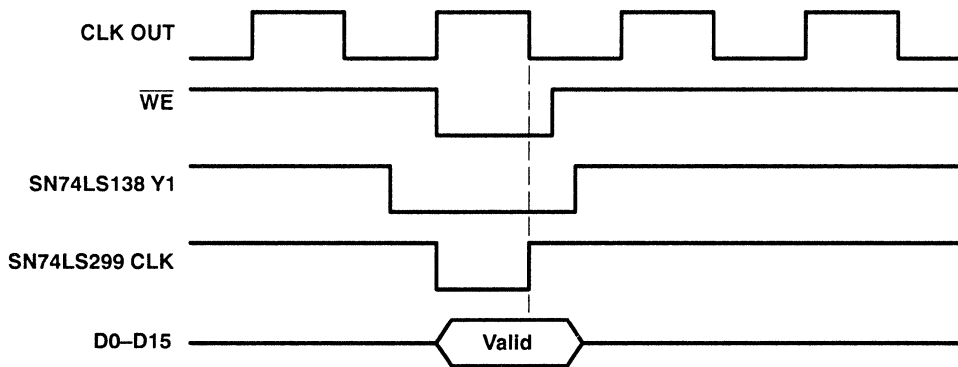


Figure 4-7. TMS32010/TMS320C15-TLC32046 Interface Timing

Typical Characteristics

D/A AND A/D LOW-PASS FILTER RESPONSE SIMULATION

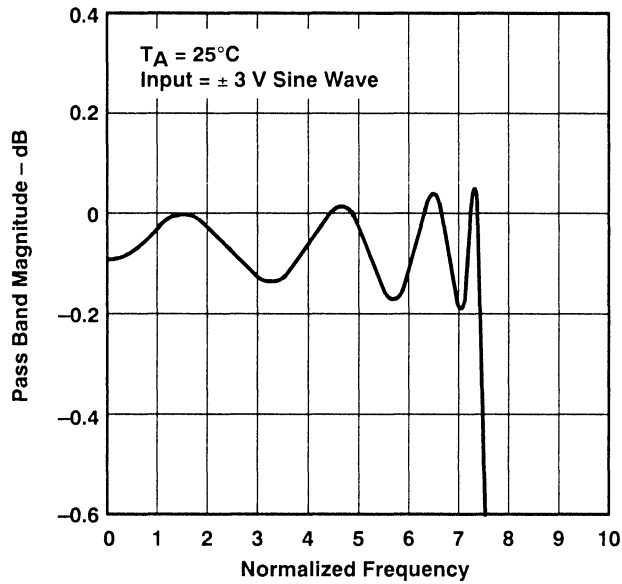


Figure 5-1

D/A AND A/D LOW-PASS FILTER RESPONSE

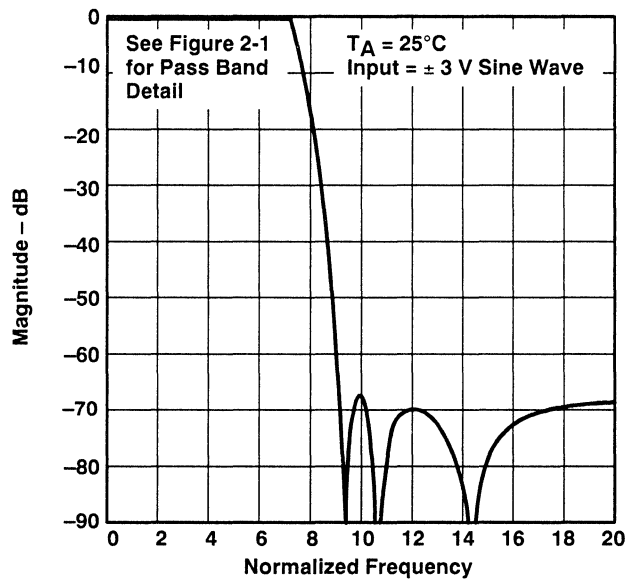


Figure 5-2

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288}$

For Low-Pass SCF $f_{\text{clock}} > 288$ kHz, please call the factory.

D/A AND A/D LOW-PASS GROUP DELAY

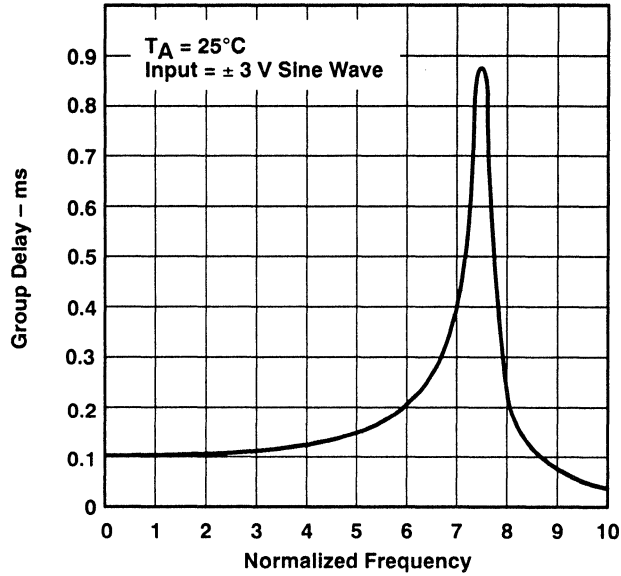


Figure 5-3

A/D BAND-PASS RESPONSE

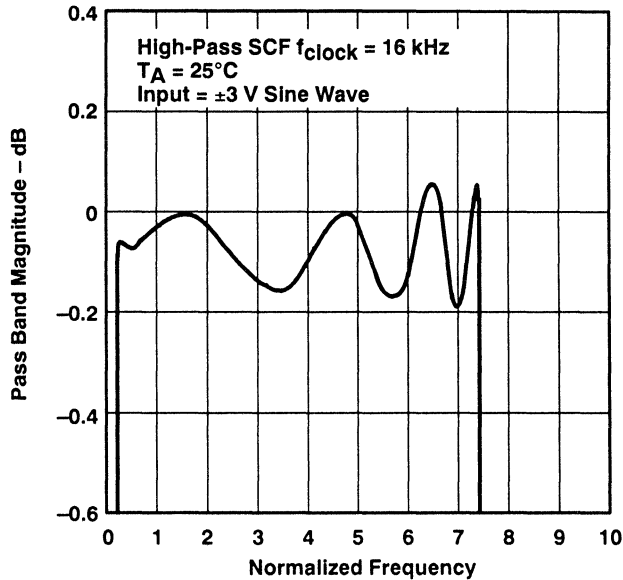


Figure 5-4

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288}$

For Low-Pass SCF $f_{\text{clock}} > 288$ kHz, please call the factory.

A/D BAND-PASS FILTER RESPONSE SIMULATION

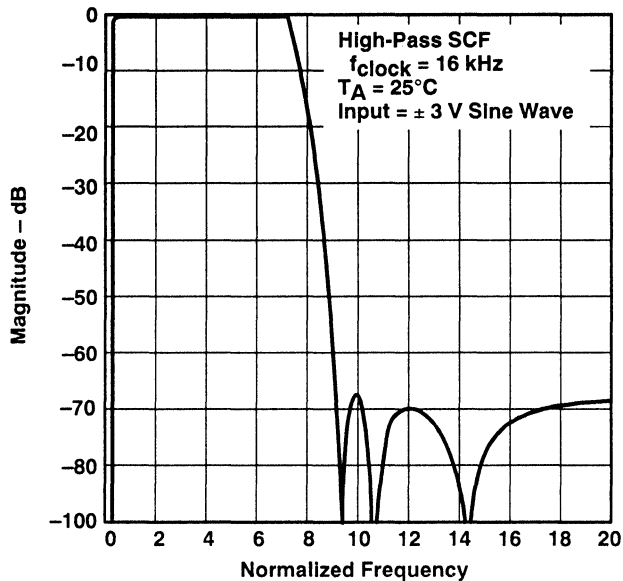


Figure 5-5

A/D BAND-PASS FILTER GROUP DELAY

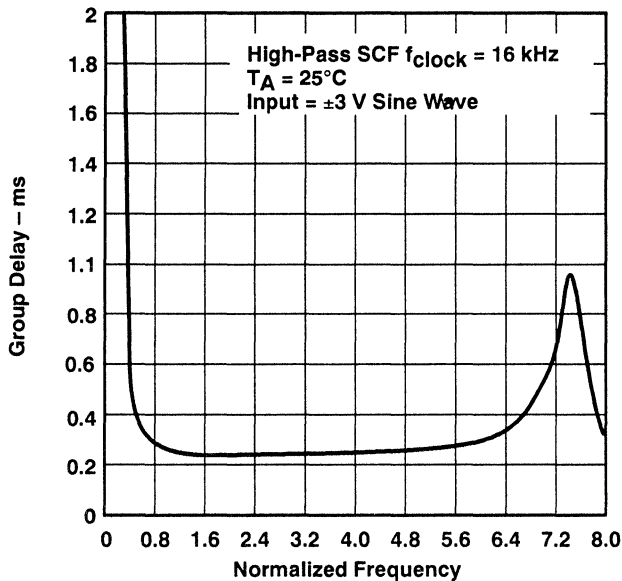


Figure 5-6

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288}$

For Low-Pass SCF $f_{\text{clock}} > 288 \text{ kHz}$, please call the factory.

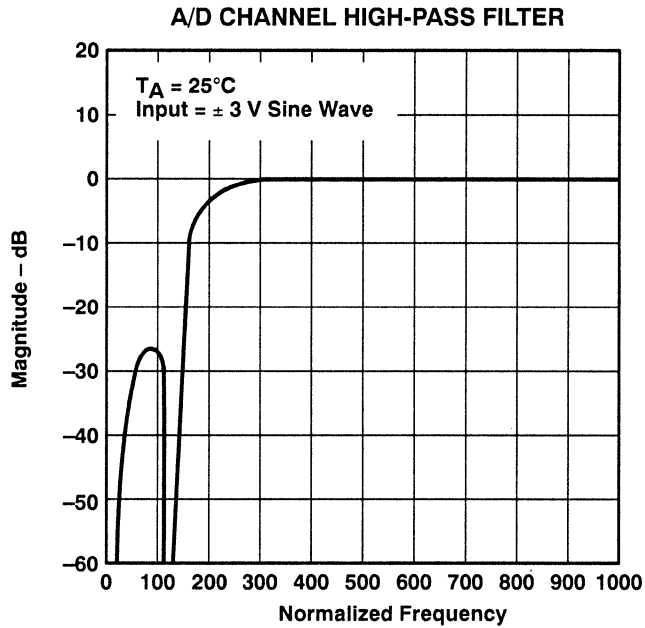


Figure 5-7

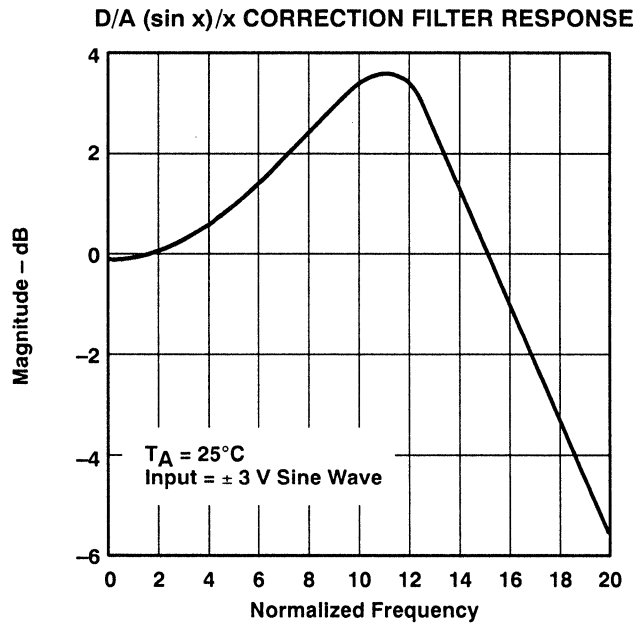


Figure 5-8

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288}$

For Low-Pass SCF $f_{\text{clock}} > 288\text{ kHz}$, please call the factory.

D/A (sin x)/x CORRECTION FILTER RESPONSE

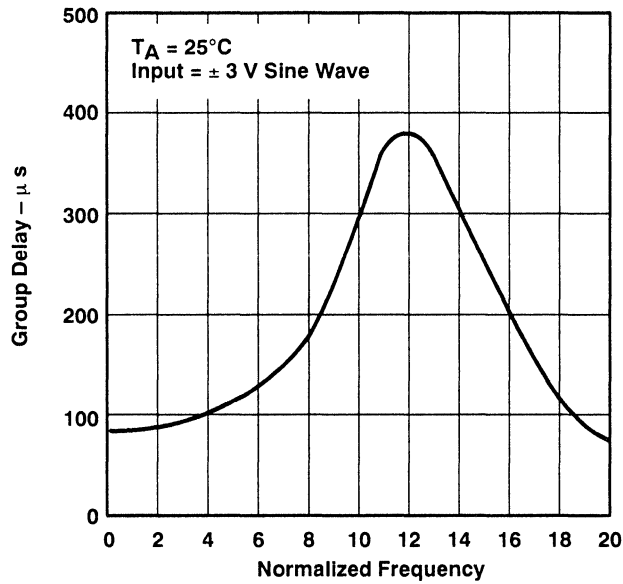


Figure 5-9

D/A (sin x)/x CORRECTION ERROR

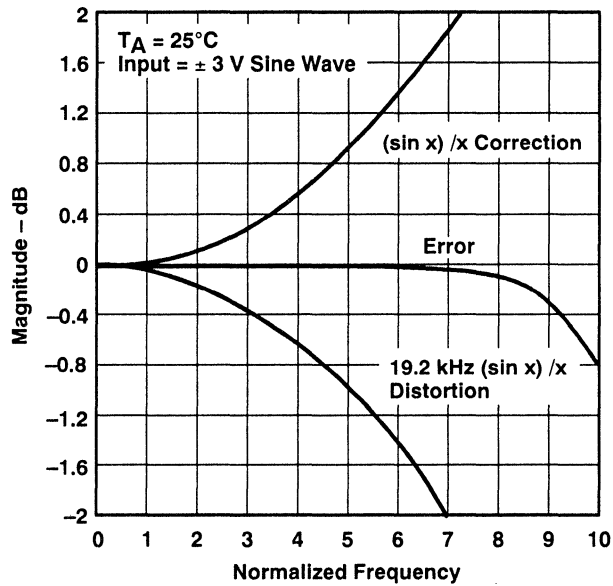


Figure 5-10

NOTE : Absolute Frequency (kHz) = $\frac{\text{Normalized Frequency} \times \text{SCF } f_{\text{clock}} \text{ (kHz)}}{288}$

For Low-Pass SCF $f_{\text{clock}} > 288$ kHz, please call the factory.

A/D BAND-PASS GROUP DELAY

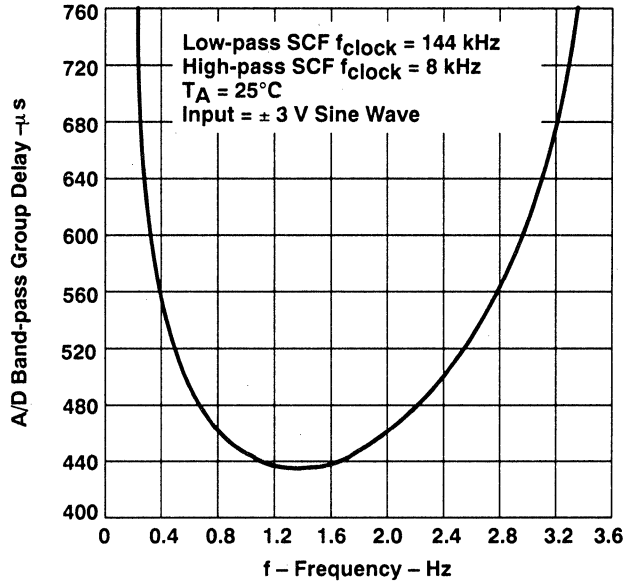


Figure 5-11

D/A LOW-PASS GROUP DELAY

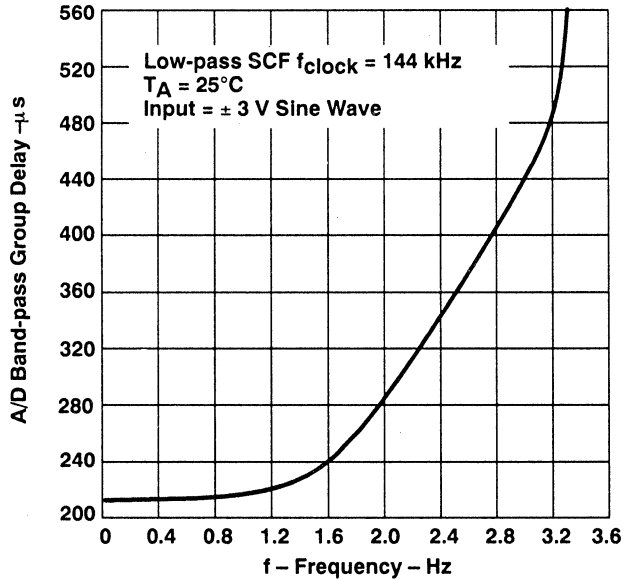


Figure 5-12

**A/D SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL**

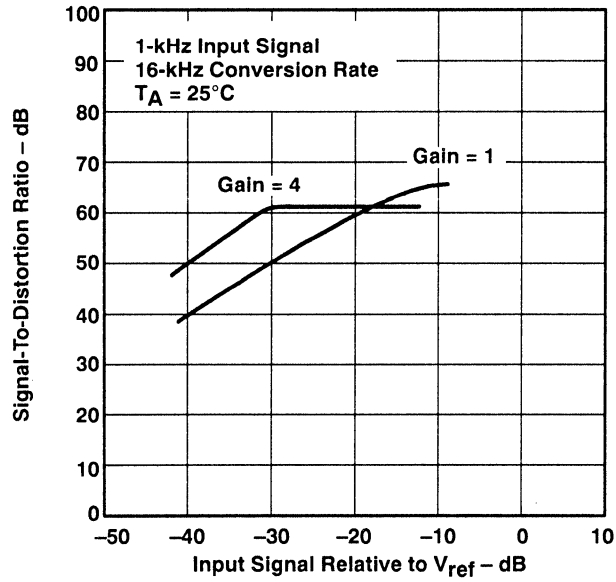


Figure 5-13

**A/D GAIN TRACKING
(GAIN RELATIVE TO GAIN AT 0-dB INPUT SIGNAL)**

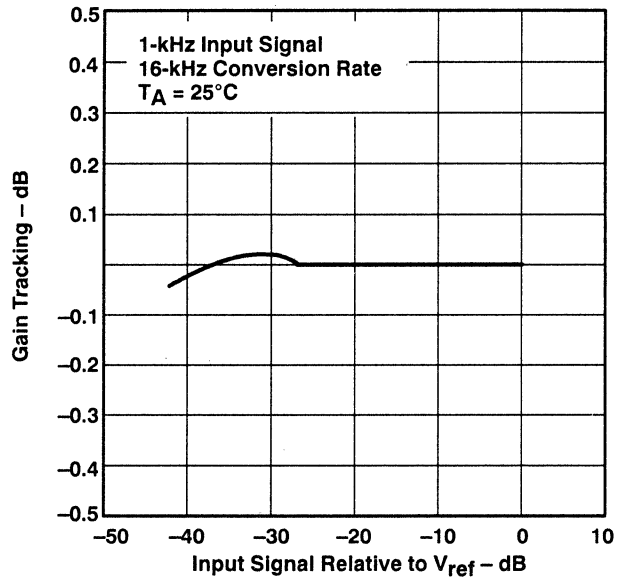


Figure 5-14

**D/A CONVERTER SIGNAL-TO-DISTORTION RATIO
vs
INPUT SIGNAL**

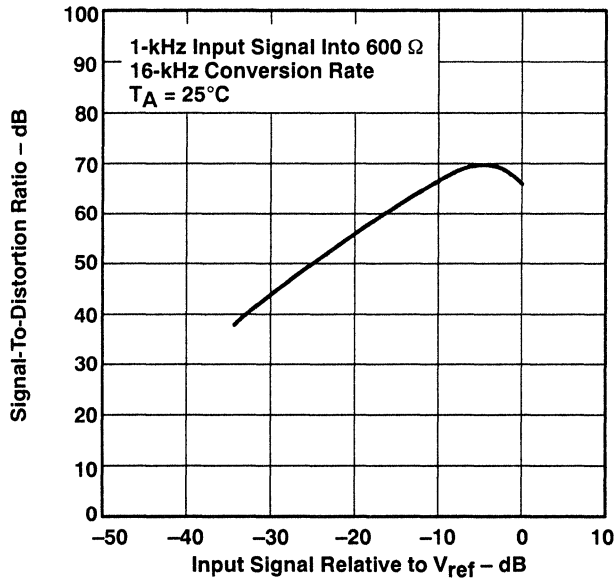


Figure 5-15

**D/A GAIN TRACKING (GAIN RELATIVE TO GAIN
AT 0-dB INPUT SIGNAL)**

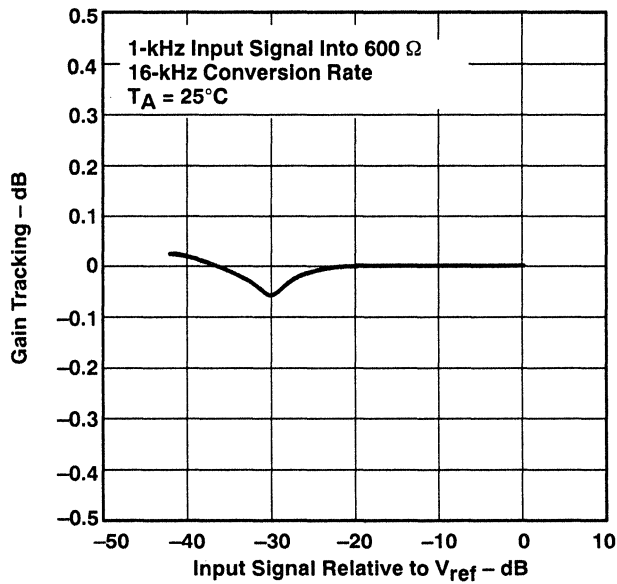


Figure 5-16

**A/D SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL**

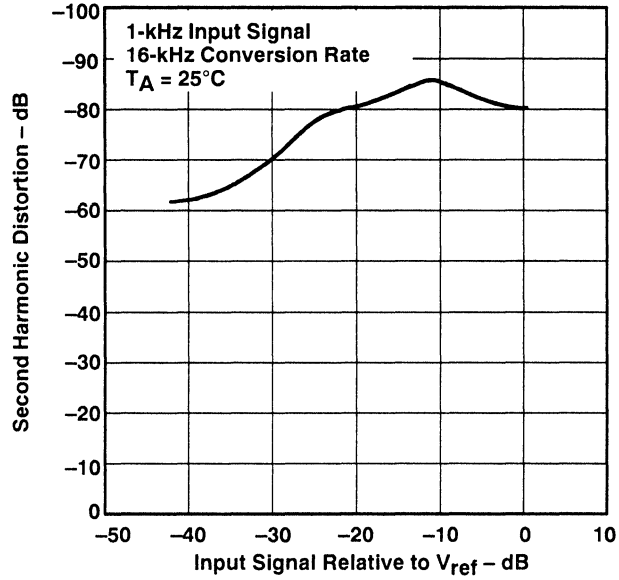


Figure 5-17

**D/A SECOND HARMONIC DISTORTION
vs
INPUT SIGNAL**

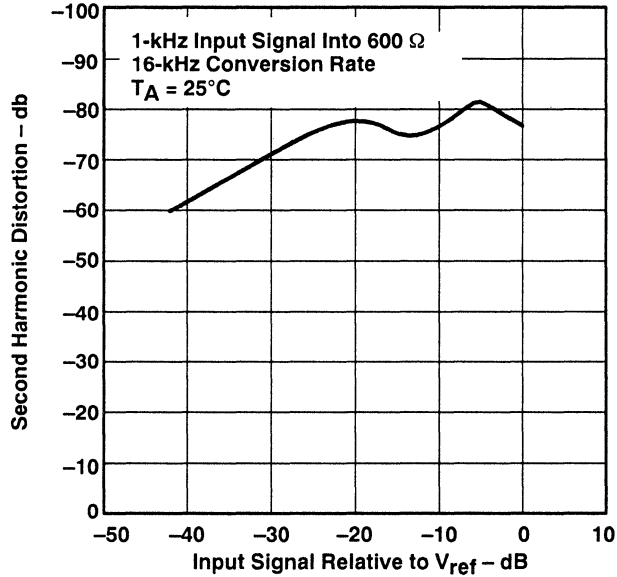


Figure 5-18

**A/D THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL**

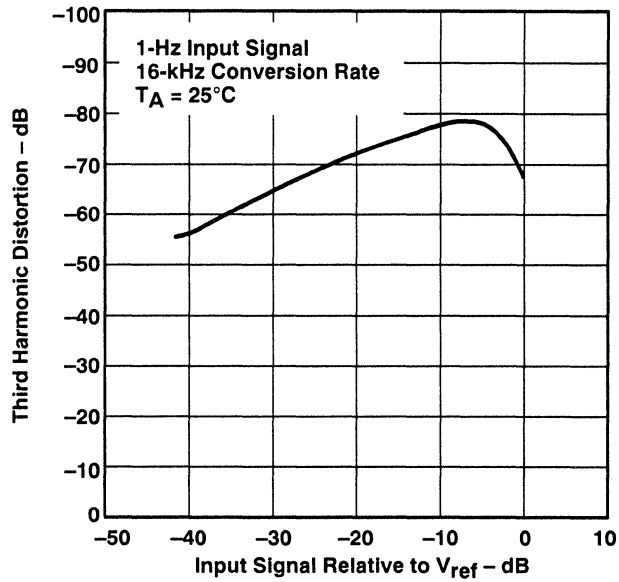


Figure 5-19

**D/A THIRD HARMONIC DISTORTION
vs
INPUT SIGNAL**

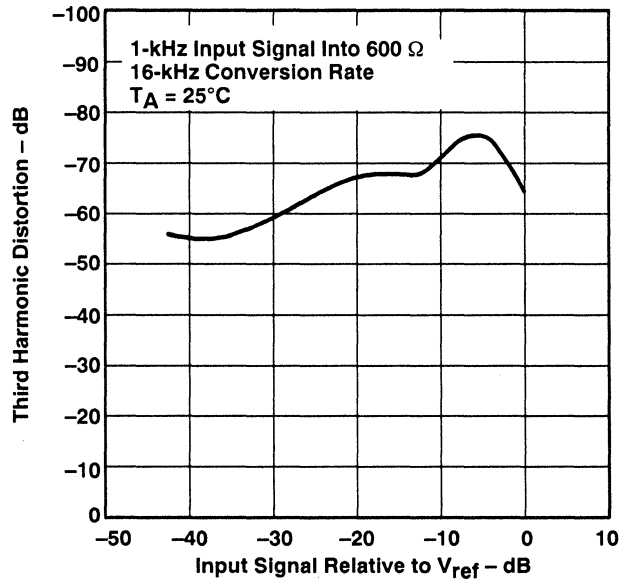


Figure 5-20

Application Information

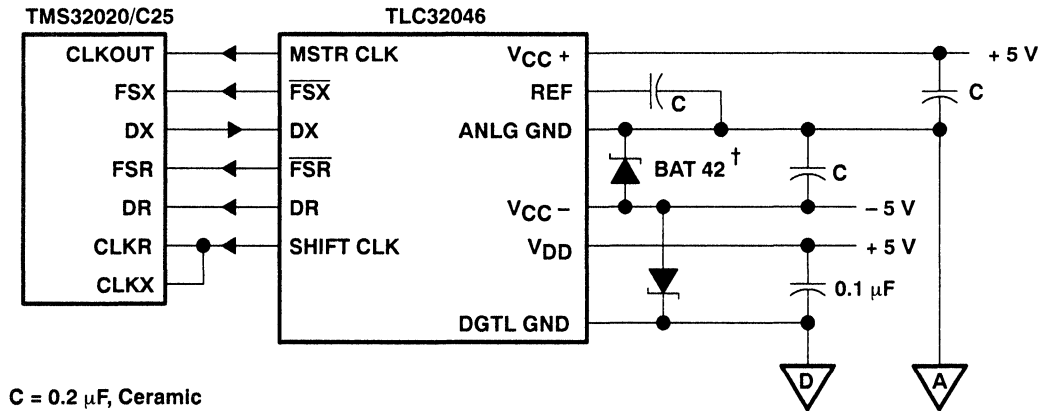
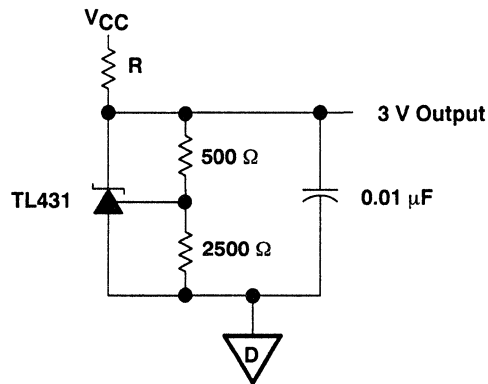


Figure 6-1. AIC Interface to the TMS32020/C25 Showing Decoupling Capacitors and Schottky Diode†

† Thomson Semiconductors



FOR: $V_{CC} = 12 \text{ V}, R = 7200 \Omega$
 $V_{CC} = 10 \text{ V}, R = 5600 \Omega$
 $V_{CC} = 5 \text{ V}, R = 1600 \Omega$

Figure 6-2. External Reference Circuit for TLC32046

