TMS7000 Programmer's Pocket Reference

8-Bit Microcomputer Family

TEXAS INSTRUMENTS

RTC HOTLINE NUMBERS

For assistance in using the TMS7000, call the TI Regional Technology Center nearest you. The centers are staffed with Applications Engineers ready to answer all your questions.

ATLANTA	(404) 452-4686
BOSTON	(617) 890-4271
CHICAGO	(312) 228-6008
DALLAS	(214) 680-5096
NORTHERN CALIFORNIA	(408) 980-0305
SOUTHERN CALIFORNIA	(714) 660-8164

TMS7000-ASSOCIATED DOCUMENTS

TMS7000 8-Bit Microcomputer Data Manual
Part No. MP008A

TMS7000 Assembly Language Programmer's Guide,
Part No. MP916A

TMS7000 Family Data Manual
Part No. SPND001

TMS7000 Family Microassembler,
Part No. MP457

TMS7000 Microprogrammer's Reference Card,
Part No. MP 459

TMS7000/TMS7001/TMS7020/TMS7040, TMS7041,TMS70120,SE70P161

TABLE OF CONTENTS

TMS7000 INSTRUCTION SET

Single Operand Instructions

MNEMONIC	DEFINITION	STATUS BITS AFFECTED	ACTION
CLR	Clear Operand	C/Z/N	0 → Destination
DEC	Decrement	C/Z/N	Destination − 1 → Destination
DECD	Decrement Double	C/Z/N	Register Pair − 1 → Register Pair
INC	Increment	C/Z/N	Destination + 1 → Destination
INV	Invert	C/Z/N	Destination → Destination
POP	Pop From Stack	C/Z/N	Top of Stack → Destination, SP − 1 → SP
PUSH	Push On Stack	C/Z/N	SP + 1 → SP, Destination → Top of Stack
RL	Rotate Left	C/Z/N	bn → bn + 1, b7 → b0, b7 → C
RLC	Rotate Left Through Carry	C/Z/N	bn → bn + 1, C → b0, b7 → C
RR	Rotate Right	C/Z/N	bn + 1 → bn, b0 → b7, b0 → C
RRC	Rotate Right Through Carry	C/Z/N	bn + 1 → bn, C → b7, b0 → C
XCHB	Exchange With Register B	C/Z/N	B → Destination, Destination → B; Z, N set on Final Destination contents

Extended Instructions

BR	Unconditional Branch	none	Destination → PC
CMPA	Compare To A Register	C/Z/N	A-source computed but not stored bits set on result.
LDA	Load A Register	C/Z/N	Source → A
STA	Store A Register	C/Z/N	A → Destination

TMS7000 INSTRUCTION SET (Continued)

Dual Operand Instructions

MNEMONIC	DEFINITION	STATUS BITS AFFECTED	ACTION
ADC	Add With Carry	C/Z/N	Source + Destination + C → Destination
ADD	Add Bytes	C/Z/N	Source + Destination → Destination
AND	AND Bytes	C/Z/N	Source ANDed with Destination → Destination
ANDP	AND Peripheral File	C/Z/N	Source ANDed with PF → PF
CMP	Compare	C/Z/N	Destination − Source computed but not stored, ST bits set on result
DAC	Decimal Add With Carry	C/Z/N	Source + Destination + C → Destination (Decical)
DSB	Decimal Subtract With Borrow	C/Z/N	Destination − Source − 1 + C → Destination (Decimal)
MOV	Move	C/Z/N	Source → Destination
MOVD	Move Double	C/Z/N	Register Pair → Register Pair
MOVP	Move Peripheral File	C/Z/N	Read/Write data to PF
MPY	Multiply	C/Z/N	Source x Destination → A & B Register Pair
OR	OR Bytes	C/Z/N	Source ORed with Destination → Destination
ORP	OR Peripheral File	C/Z/N	Source ORed with PF → PF
SBB	Subtract With Borrow	C/Z/N	Destination − Source −1 + C → Destination
SUB	Subtract Bytes	C/Z/N	Destination − Source → Destination
XOR	Exclusive OR Bytes	C/Z/N	Source exclusive ORed with Destination → Destination
XORP	Exclusive OR Peripheral File	C/Z/N	Source exclusive ORed with PF → PF

TMS7000 INSTRUCTION SET (Continued)

JUMP Instructions

MNEMONIC	DEFINITION	STATUS BITS AFFECTED	ACTION
BTJO	Bit Test JUMP If One	C/Z/N	If source ANDed with Destination $<>$ 0, JUMP
BTJOP	Bit Test JUMP If One, Peripheral File	C/Z/N	If source ANDed with PF $<>$ 0, JUMP
BTJZ	Bit Test JUMP If Zero	C/Z/N	If source ANDed with $\overline{\text{Destination}}$ $<>$ 0, JUMP
BTJZP	Bit Test JUMP If Zero, Peripheral File	C/Z/N	If source ANDed with $\overline{\text{PF}}$ $<>$ 0, JUMP
DJNZ	Decrement Register JUMP If Non-zero	none	Destination $-1 \rightarrow$ Destination, if Destination 0, JUMP
JMP	Unconditional JUMP	none	PC + offset $\rightarrow$ PC
JC/JHS	JUMP If Carry Set/JUMP If Higher Or Same	none	If C = 1, PC + offset $\rightarrow$ PC
JN	JUMP If Negative	none	If N = 1, PC + offset $\rightarrow$ PC
JNC/JL	JUMP If No Carry/JUMP If Lower	none	If C = 0, PC + offset $\rightarrow$ PC
JNZ/JNE	JUMP If Not Zero/JUMP If Not Equal	none	If Z = 0, PC + offset $\rightarrow$ PC
JP	JUMP If Positive	none	If N = 0, + Z = 0, PC + offset $\rightarrow$ PC
JPZ	JUMP If Positive Or Zero	none	If N = 0, PC + offset $\rightarrow$ PC
JZ/JEQ	JUMP If Zero/JUMP If Equal To	none	If Z = 1, PC + offset $\rightarrow$ PC

TMS7000 INSTRUCTION SET (Continued)

Control Instructions

MNEMONIC	DEFINITION	STATUS BITS AFFECTED	ACTION
CLRC	Clear Carry Bit	C/Z/N	0 → C,N,Z set from A register
DINT	Disable Interrupts	I/C/Z/N	0 → I, 0 → C, 0 → N, 0 → Z
EINT	Enable Interrupts	I/C/Z/N	1 → I, 1 → C, 1 → N, 1 → Z
IDLE	Idle Until Interrupt	none	Suspend until Interrupt
LDSP	Load Stack Pointer	none	B register → SP
NOP	No Operation	none	PC + 1 → PC
SETC	Set Carry	C/Z/N	1 → C, 0 → N, 1 → Z
STSP	Store Stack Pointer	none	SP → B register
SWAP	Swap Nibbles	C/Z/N	B7-B4 <-> B3-B0
TSTA	Test A Register	C/Z/N	0 → C,N,Z set from A register
TSTB	Test B Register	C/Z/N	0 → C,N,Z set from B register

TMS7000 INSTRUCTION SET (Concluded)

Subroutine Instructions

MNEMONIC	DEFINITION	STATUS BITS AFFECTED	ACTION
CALL	Call Subroutine	none	SP + 1 → SP, PC Hi byte → stack, SP + 1 → SP, PC Lo byte → stack Operand (address) → PC
RETI	Return From Interrupt	loaded from stack	Stack → PC Lo byte, SP – 1 → SP, Stack → PC Hi byte, SP – 1 → SP, Stack → ST, SP – 1 → SP
RETS	Return From Subroutine	none	Stack → PC Lo byte, SP – 1 → SP, Stack → PC Hi byte, SP – 1 → SP,
TRAP0 • • TRAP23	Trap To Subroutine	none	SP + 1 → SP, PC Hi byte → stack, SP + 1 → SP, PC Lo byte → stack Entry vector → PC

RESET, INTERRUPT, AND TRAP VECTOR LOCATIONS

ADDRESS LOCATIONS MSB	LSB	TRAP LEVEL		INTERRUPT LEVEL	INTERRUPT SOURCE
FFFE	FFFF	TRAP 0		RESET Highest Priority	External
FFFC	FFFD	TRAP 1		INT1	External
FFFA	FFFB	TRAP 2		INT2	Timer 1
FFF8	FFF9	TRAP 3		INT3	External
FFF6	FFF7	TRAP 4	*	INT4	RXBUF, TXBUF, Timer 3
FFF4	FFF5	TRAP 5	*	INT5 Lowest Priority	Timer 2
FFF2	FFF3	TRAP 6			
FFF0	FFF1	TRAP 7			
FFEE	FFEF	TRAP 8			
FFEC	FFED	TRAP 9			
FFEA	FFEB	TRAP 10			
FFE8	FFE9	TRAP 11			
FFE6	FFE7	TRAP 12			
FFE4	FFE5	TRAP 13			
FFE2	FFE3	TRAP 14			
FFE0	FFE1	TRAP 15			
FFDE	FFDF	TRAP 16			
FFDC	FFDD	TRAP 17			
FFDA	FFDB	TRAP 18			
FFD8	FFD9	TRAP 19			
FFD6	FFD7	TRAP 20			
FFD4	FFD5	TRAP 21			
FFD2	FFD3	TRAP 22			
FFD0	FFD1	TRAP 23			

*Available on 7001/7041/70P161 only.

PERIPHERAL FILE MEMORY MAPS
ALL TMS7000 DEVICES

I/O PORT	MEMORY ADDRESS	I/O REGISTER	IN MODES:
P0	>0100	I/O Control 0 (IOCNTLO)	All
P1	>0101	Reserved	
P2	>0102	Timer 1 Data (TIDATA)	All
P3	>0103	Timer 1 Control (TICTRL)	All
P4	>0104	Port A Data (APORT)	All
P5	>0105	*Port A Data Direction (ADDR)	
P6	>0106 B(0) – B(3)	Port B Data (BPORT	All
P6	>0106 B(4) – B(7)	Port B Data (BPORT)	SC
		Peripheral File Expansion	PE, FE, MP
P7	>0107	Reserved	
P8	>0108	Port C Data (CPORT)	SC
		Peripheral File Expansion	PE, FE, MP
P9	>0109	Port C Data Dir (CDDR)	SC
		Peripheral File Expansion	PE, FE, MP
P10	>010A	Port D Data (DPORT)	SC, PE
		Peripheral File Expansion	FE, MP

P11	>010B		Port D Data Direc (DDDR)	SC, PE
			Peripheral File Expansion	FE, MP
P12-P15	>010C – >10F		Not Used	SC
			Peripheral File Expansion	PE, FE, MP
P16	>0110	**	I/O Control 1 (IOCNTL1)	All
P17	>0111		Serial Mode (SMODE)	
			Serial Control 0 (SCTL0)	
			Status Register (SSTAT)	
P18	>0112		Timer 2 Data (T2DATA)	
P19	>0113		Timer 2 Control (T2CTRL)	
P20	>0114		Timer 3 Data (T3DATA)	
P21	>0115		Serial Control 1 (SCTL1)	
P22	>0116		Receiver Buffer (RXBUF)	
P23	>0117		Transmitter Buffer (TXBUF)	
P24-P255	>0118 – >01FF		Not Used	SC
			Perpheral File Expansion	PE, FE, MP

NOTES:

*Available on 7041/7001/70P161 only.

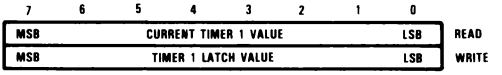
**Available only on 7041/7001/70P161. For other devices, this is Peripheral file expansion in PE, FE, and MP modes. Not available in SC mode.

SC = Single Chip Mode
PE = Peripheral Expansion Mode
FE = Full Expansion Mode
MP = Microprocessor Mode

PERIPHERAL FILE REGISTERS

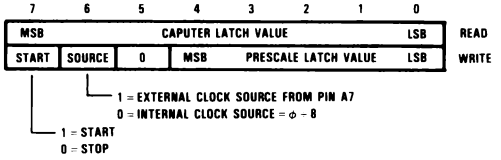
T1DATA: Timer 1 Data Register

PF NUMBER: P2
ADDRESS: >0102



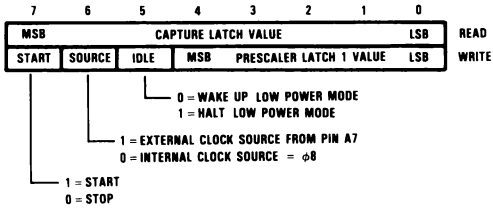
T1CTRL: Timer 1 Control Register (All Except CMOS Devices)

PF NUMBER: P3
ADDRESS: >0103



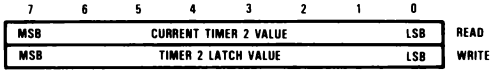
T1CTRL: Timer 1 Control Register (70C00, 70C20, 70C40 Only)

PF NUMBER: P3
ADDRESS: 0103



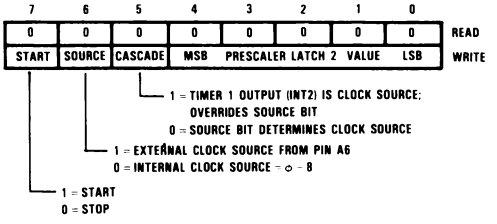
T2DATA: Timer 2 Data Register *

PF NUMBER: P18
ADDRESS: >0112



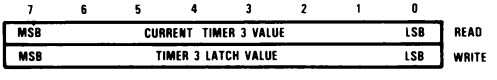
T2CTRL: Timer 2 Control Register *

PF NUMBER: P19
ADDRESS: >0113



T3DATA: Timer 3 Data Register *

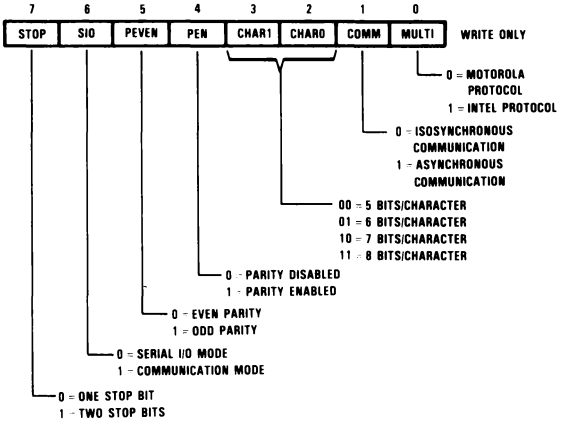
PF NUMBER: P20
ADDRESS: >0114



*Available on 7001/7041/70P161 only.

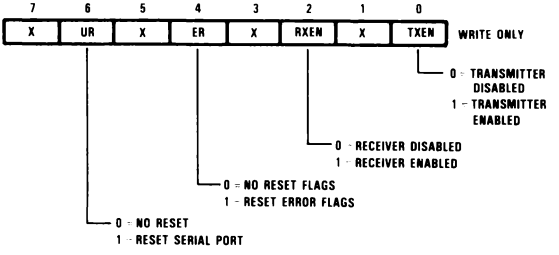
SMODE: Serial Mode Register (First Write After RESET) *

PF NUMBER: P17
ADDRESS: >0111



SCTL0: Serial Control 0 Register *

PF NUMBER: P17
ADDRESS: >0111

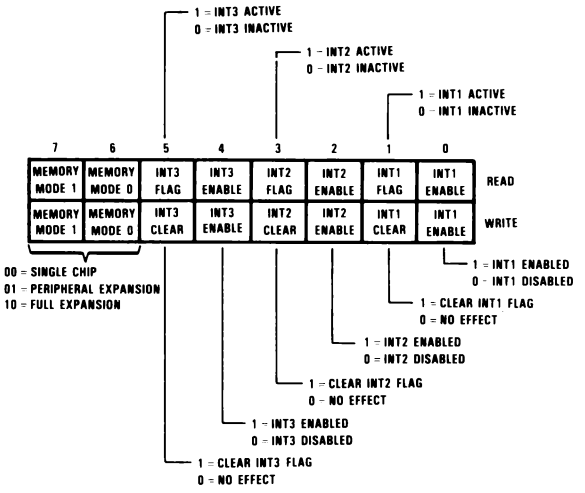


*Available on 7001/7041/70P161 only.

PERIPHERAL FILE REGISTERS (Cont.)

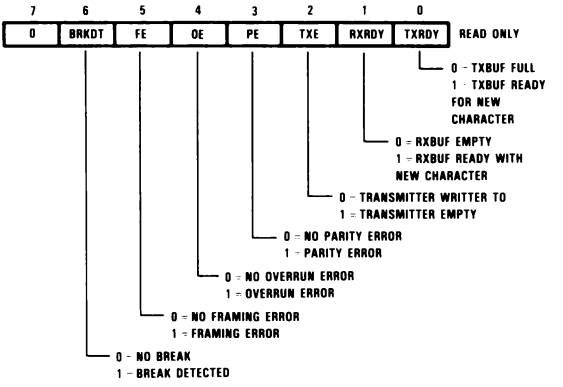
IOCNT0: I/O Control 0 Register (Cleared By RESET)

PF NUMBER: P0
ADDRESS: >0100



SSTAT: Serial Port Status Register *

PF NUMBER: P17
ADDRESS: >0111

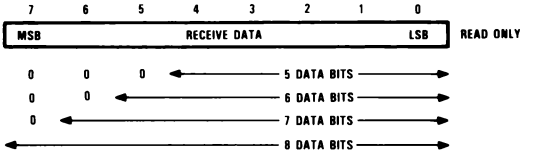


*AVAILABLE ON 7001/7041/70P161 only.

PERIPHERAL FILE REGISTERS (Cont.)

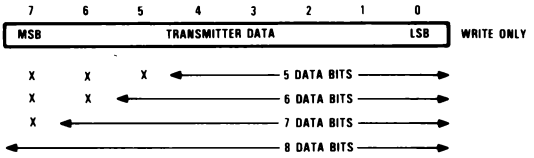
RXBUF: Receiver Buffer *

PF NUMBER: P22
ADDRESS: >0116



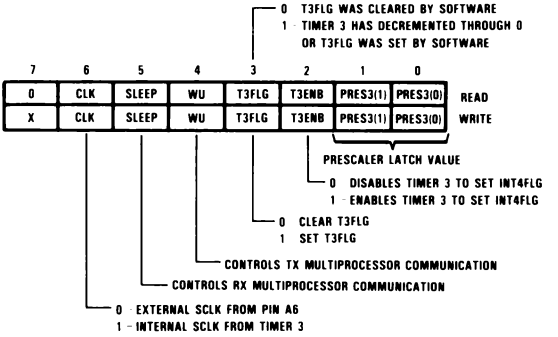
TXBUF: Transmitter Buffer *

PF NUMBER: P23
ADDRESS: >0117



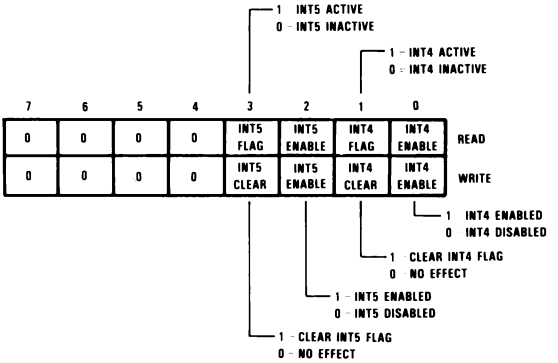
SCTL1: Serial Control 1 Register *

PF NUMBER: P21
ADDRESS: >0115



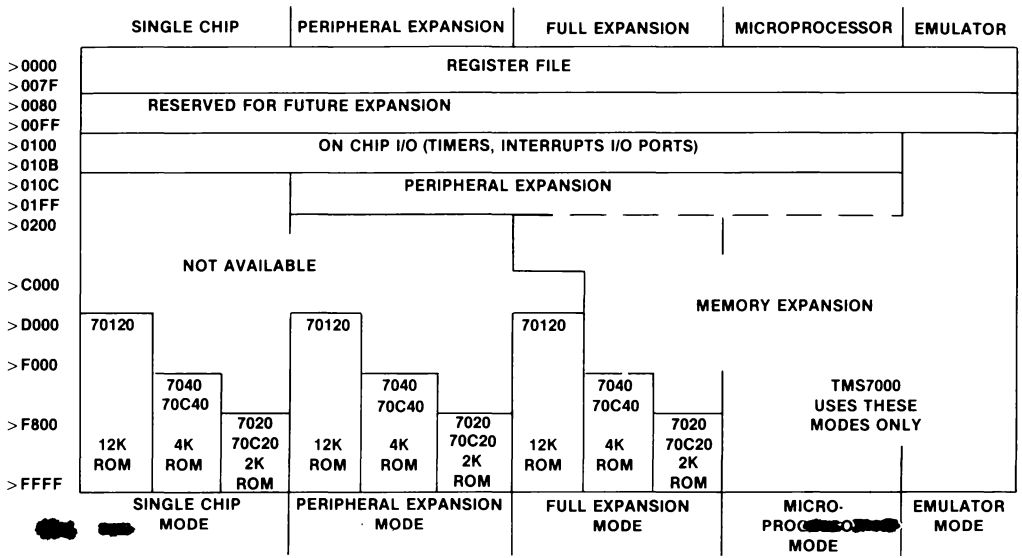
IOCNT1: I/O Control Register (Not Cleared By RESET)*

PF NUMBER: P16
ADDRESS: >0110

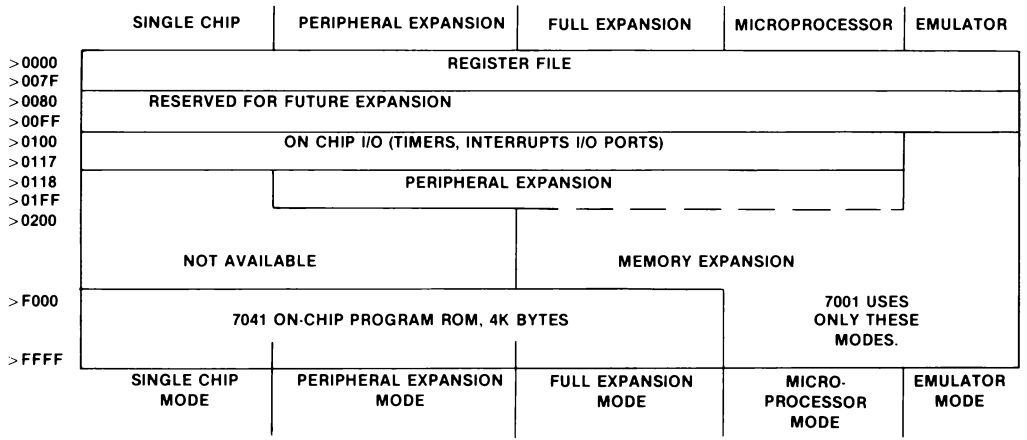


*Available on 7001/7041/70P161 only.

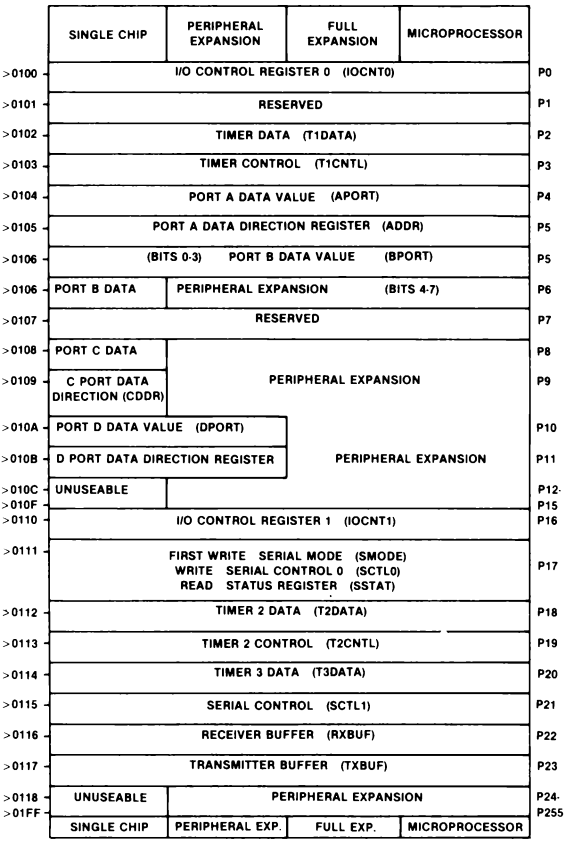
MEMORY MAPS
70X0 MEMORY MAP



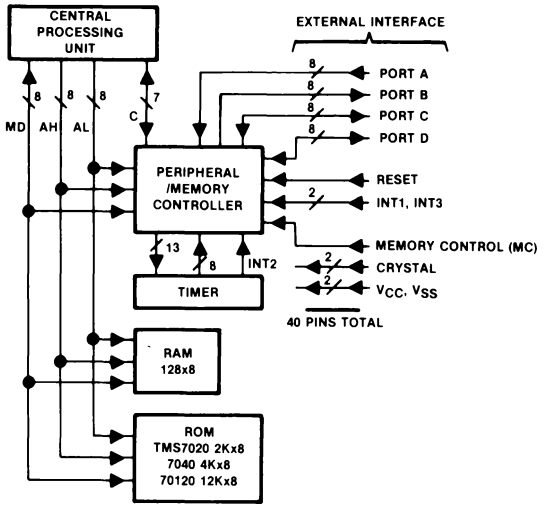
70X1 MEMORY MAP



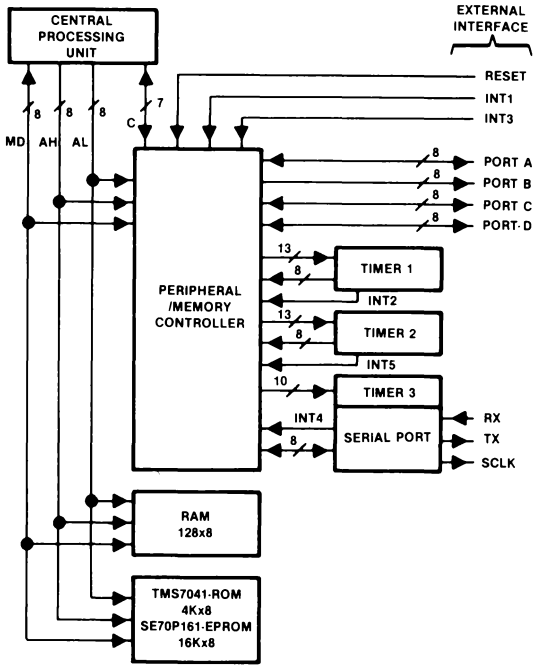
TMS70X1 PERIPHERAL MEMORY MAP



TMS7000 BLOCK DIAGRAM



TMS7001, TMS7041, SE70P161 BLOCK DIAGRAM



PIN ASSIGNMENTS ALL TMS7000 DEVICES

Signature	Pin	I/O	Description
A0 (LSB)	6	I/O	7001/7041/70P161 ONLY: A0-A4 and A7 can be individually selected in software as general-purpose input or output pins. A5 is a general-purpose input only pin, or also may function as a serial port input-only pin. A6 is a general-purpose input-only pin, or may also function as a serial port clock I/O or as clock input for Timer 2. A7 can also serve as a clock input for Timer 1.
A1	7	I/O	
A2	8	I/O	
A3	9	I/O	
A4	10	I/O	
A5 (RX)*	16	IN	
A6 (SCLK)*	15	I/O	All 70X0 DEVICES: A0-A7 are general-purpose input-only pins. A7 can also serve as clock input for the Timer.
A7	11	I/O	
B0 (LSB)	3	OUT	All 7000 DEVICES: B0-B7 are general-purpose output-only pins. B4-B7 become memory expansion control signals in Peripheral Expansion, Full Expansion, and Microprocessor modes. 7001/7041/70P161 ONLY: B3 also functions as a serial port output pin.
B1	4	OUT	
B2	5	OUT	
B3 (TX)*	37	OUT	
B4 (ALATCH)	38	OUT	
B5 (R/W)	1	OUT	
B6 (ENABLE)	39	OUT	
B7 (CLKOUT)	2	OUT	
C0 (LSB)	28	I/O	All 7000 DEVICES: C0-C7 can be individually selected in software as general-purpose input or output in Single Chip mode. C0-C7 beocme the LSB address Data Bus in Peripheral Expansion, Full expansion, and Microprocessor modes.
C1	29	I/O	
C2	30	I/O	
C3	31	I/O	
C4	32	I/O	

C5	33	I/O	
C6	34	I/O	
C7 (MSB)	35	I/O	
D0 (LSB)	27	I/O	All 7000 DEVICES: D0-D7 can be individually selected in software as general-purpose
D1	26	I/O	input or output pins in Single Chip or Peripheral Expansion modes. D0-D7 become
D2	24	I/O	the MSB Address Bus in Full Expansion and Microprocessor modes.
D3	23	I/O	
D4	22	I/O	
D5	21	I/O	
D6	20	I/O	
D7 (MSB)	19	I/O	
INT1	13	IN	Maskable interrupt, priority level 1. 7000 NMOS devices are latch- and level-triggered. CMOS devices are latched only.
INT3	12	IN	Maskable interrupt, priority level 3. All devices are latch- and level-triggered.
RESET	14	IN	Non-maskable system reset, priority level 0.
MC	36	IN	Mode control pin.
XTAL2/CLKIN	17	IN	External clock input. Crystal connect 2
XTAL1	18	IN	No-connect for external clock. Crystal connect 1.
V_{CC}	25	IN	Supply voltage (+5V)
V_{SS}	40	IN	Ground reference

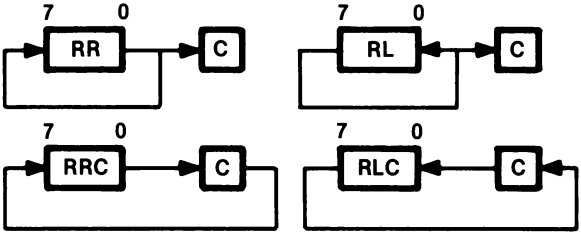
*Pins 15, 16, and 37 are SCLK, RX, and TX on 7001/7041/70P161 only.

MODE SELECT CONDITIONS

MODE	MODE SELECT CONDITIONS	
	MODE CNTL PIN	I/O CONTROL REG. BIT 7, 6
Single-Chip	0 V	0 0
Peripheral Expansion	0 V	0 1
Full Expansion	0 V	1 0
Microprocessor	V_{CC}	X X
System Emulator	+14 V	X X

X = Don't Care

BIT FLOW FOR ROTATE INSTRUCTIONS



ASCII CHARACTER SET

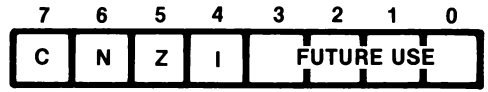
HEX (Low Byte)	0	1	2	3	4	5	6	7 (High Byte)
0	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	` 96	p 112
1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
2	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
3	ETX 3	DC3 19	- 35	3 51	C 67	S 83	c 99	s 115
4	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
5	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
6	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
7	BEL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
8	BS 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
9	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
A	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
B	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
C	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	: 124
D	CR 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
E	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
F	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	DEL 127

STATUS BIT VALUES FOR CONDITIONAL JUMP INSTRUCTIONS

MNEMONIC	INSTRUCTION	CONDITION ON WHICH JUMP IS TAKEN	STATUS BIT VALUES FOR JUMP: C	N	Z	SIGNED	UN-SIGNED
JC/JHS	Jump If Carry/Jump If Higher Or same	(d)unsigned > = (s)	1	X	X	Y	Y
JNC/JL	Jump If No Carry/ Jump If Lower	(d)unsigned < (s)	0	X	X	Y	Y
JZ/JEQ	Jump If Zero/Jump If Equal	(d) = (s)	X	X	1	Y	Y
JNZ/JNE	Jump If Non-zero/ Jump If Not Equal	(d) < > (s)	X	X	0	Y	Y
JP	Jump If Positive	(d)-(s) = pos #	X	0	0	Y	N
JN	Jump If Negative	(d)-(s) = neg #	X	1	X	Y	N
JPZ	Jump If Positive or Zero	(d)-(s) = pos # or 0	X	0	X	Y	N

X = Don't care

STATUS REGISTER

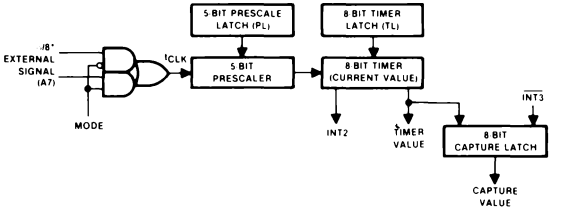


- C – CARRY OUT (NO BORROW)
- N – SIGN BIT
- Z – ZERO
- I – INTERRUPT ENABLE

(This register is CPU internal)

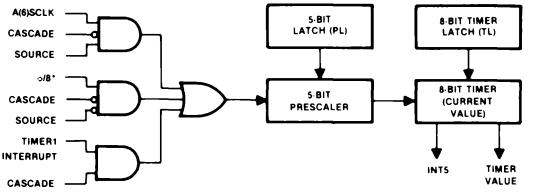
PROGRAMMABLE TIMER/EVENT COUNTERS

TIMER 1

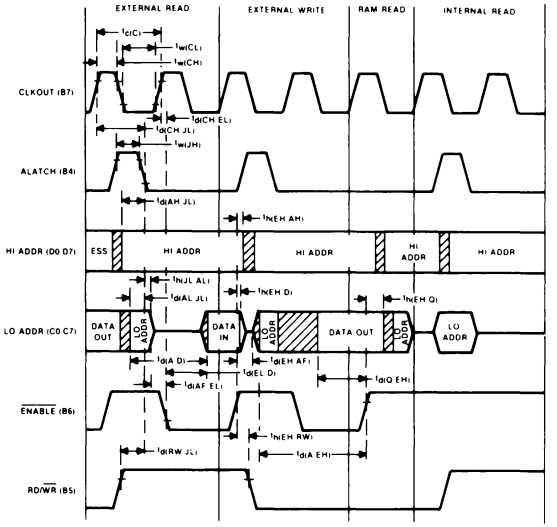


*NOTE: $\phi = f_{osc}/2$ for /2 clock option
$\phi = f_{osc}/4$ for /4 clock option

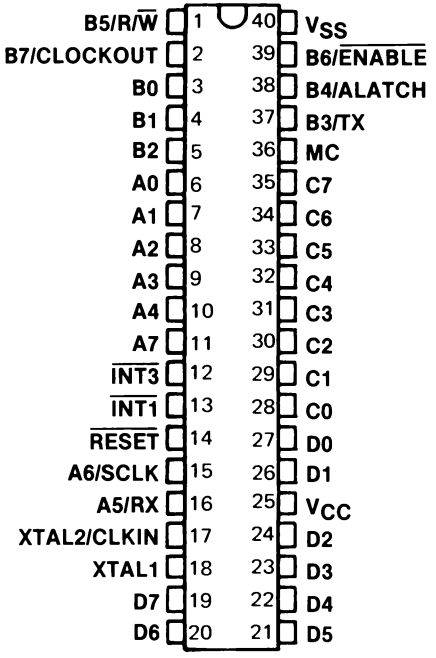
TIMER 2



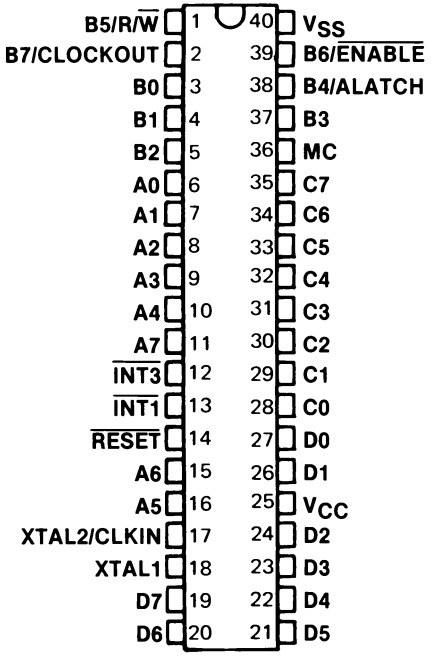
READ/WRITE CYCLE TIMING



PIN ASSIGNMENTS
TMS7001 AND TMS7041



PIN ASSIGNMENTS
TMS70X0 AND TMS70CX0



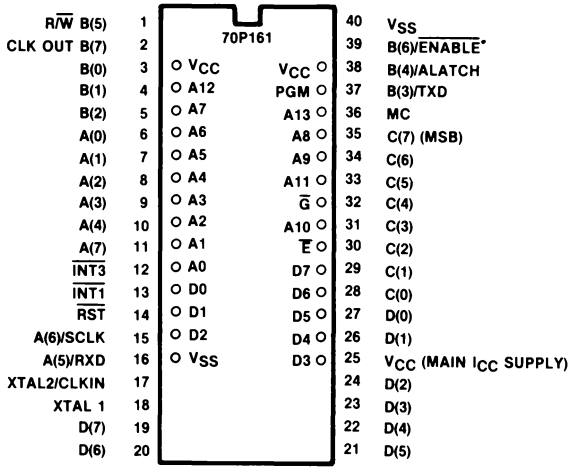
THE SE70P161 SYSTEM EMULATOR

EPROM Use (SE70P161 Only)

EPROM TYPE	70XX ROM SPACE	70XX * START ADDRESS	27XX START ADDRESS
27128	16K Bytes	>C006	>0006
27128	12K Bytes	>D006	>1006
2764	8K Bytes	>E006	>0006
2764	4K Bytes	>F006	>1006
2764	1K Bytes	>F806	>1806

* (1) Texas Instruments reserves the first 6 bytes of ROM.
(2) All EPROM access times are not more than 250 ns.

PIN ASSIGNMENTS (SE70P161 Only)



*** Pins low, EPROM always enabled.**

INSTRUCTION – OPCODE SET

	SINGLE OPERAND			DUAL OPERAND								
	A	B	Rn	A,B	B,A	Rn,A	%n,A	Rn,B		%nRn	A,Rn	B,Rn
ADC					69	19	29	39	59	49	79		
ADD					68	18	28	38	58	48	78		
AND					63	13	23	33	53	43	73		
ANDP													
BTJO					66	16	26	36	56	46	76		
BTJOP													
BTJZ					67	17	27	37	57	47	77		
BTJZP													
BR													
CALL													
CLR	B5	C5	D5										
CLRC													
CMP					6D	1D	2D	3D	5D	4D	7D		
CMPA													
DAC					6E	1E	2E	3E	5E	4E	7E		
DEC	B2	C2	D2										
DECD	BB	CB	DB										
DINT													
DJNZ	BA	CA	DA										
DSB					6F	1F	2F	3F	5F	4F	7F		
EINT													
IDLE													
INC	B3	C3	D3										
INV	B4	C4	D4										
JMP													
JC/JHS													
JN/JLT													
JNC/JL													
JNZ/JNE													
JP/JGT													
JPZ/JGE													
JZ/JEQ													
LDA													
LDSP													
MOV				C0	62	12	22	32	52	42	72	D0	D1
MOVD													
MOVP													
MPY					6C	1C	2C	3C	5C	4C	7C		
NOP													
OR					64	14	24	34	54	44	74		
ORP													
POP	B9	C9	D9										
PUSH	B8	C8	D8										
RETI													
RETS													
RL	BE	CE	DE										
RLC	BF	CF	DF										
RR	BC	CC	DC										
RRC	BD	CD	DD										
SBB					6B	1B	2B	3B	5B	4B	7B		
SETC													
STA													
STSP													
SUB					6A	1A	2A	3A	5A	4A	7A		
SWAP	B7	C7	D7										
TSTA													
TSTB													
TRAP													
XCHB	B6		D6										
XOR					65	15	25	35	55	45	75		
XORP													

INSTRUCTION – OPCODE SET

PERIPHERAL					EXTENDED			OTH-ER	STATUS WORD		
A,Pn	Pn,A	B,Pn	Pn,B	%n,Pn	DIRECT	INDIRECT	INDEXED	OTHER	COND. BITS	INT. EN. BIT	
									X		ADC
									X		ADD
									X		AND
83		93		A3					X		ANDP
									X		BTJO
86		96		A6					X		BTJOP
									X		BTJZ
87		97		A7					X		BTJZP
					8C	9C	AC				BR
					8E	9E	AE				CALL
									X		CLR
								B0	X		CLRC
									X		CMP
					8D	9D	AD		X		CMPA
									X		DAC
									X		DEC
									X		DECD
								06	X	X	DINT
											DJNZ
									X		DSB
								05	X	X	EINT
								01			IDLE
									X		INC
									X		INV
								E0			JMP
								E3			JC/JHS
								E1			JN/JLT
								E7			JNC/JL
								E6			JNZ/JNE
								E4			JP/JGT
								E5			JPZ/JGE
								E2			JZ/JEQ
					8A	9A	AA		X		LDA
								0D			LDSP
									X		MOV
					88	98	A8		X		MOVD
82	80	92	91	A2					X		MOVP
									X		MPY
								00			NOP
									X		OR
84		94		A4					X		ORP
								08	X		POP
								0E	X		PUSH
								0B			RETI
								0A			RETS
									X		RL
									X		RLC
									X		RR
									X		RRC
									X		SBB
								07	X		SETC
					8B	9B	AB		X		STA
								09			STSP
									X		SUB
									X		SWAP
								B0	X		TSTA
								C1	X		TSTB
								E8-FF			TRAP
									X		XCHB
									X		XOR
85		95		A5					X		XORP

INSTRUCTION EXECUTION TIMES

OPERATION		ADDRESSING MODES							
		A	B	RF	PF	@ lab	* RF	@ lab (B)	OTHER
ADC	B, – –	1/5							
	RF, – –	2/8	2/8	3/10					
	%lop, – –	2/7	2/7	3/9					
ADD	B, – –	1/5							
	RF, – –	2/8	2/8	3/10					
	%lop, – –	2/7	2/7	3/9					
AND	B, – –	1/5							
	RF, – –	2/8	2/8	3/10					
	%lop, – –	2/7	2/7	3/9					
ANDP	A, – –				2/10				
	B, – –				2/9				
	%lop, – –				3/11				
BTJO[1]	B, – –	2/7							
	RF, – –	3/10	3/10	4/12					
	%lop, – –	3/9	3/9	4/11					
BTJOP[1]	A, – –				3/11				
	B, – –				3/10				
	%lop, – –				4/12				
BTJZ[1]	B, – –	2/7							
	RF, – –	3/10	3/10	4/12					
	%lop, – –	3/9	3/9	4/11					
BTJZP[1]	A, – –				3/11				
	B. – –				3/10				
	%lop, – –				4/12				
BR	– –					3/10	2/9	3/12	
CALL	– –					3/14	2/13	3/16	
CLR	– –	1/5	1/5	2/7					
CLRC	– –								1/6
CMP	B, – –	1/5							
	RF, – –	2/8	2/8	3/10					
	%lop, – –	2/7	2/7	3/9					
CMPA	– –					3/12	2/11	3/14	
DAC	B, – –	1/7							
	RF, – –	2/10	2/10	3/12					
	%lop, – –	2/9	2/9	3/11					
DEC	– –	1/5	1/5	2/7					
DECD	– –	1/9	1/9	2/11					
DINT	– –								1/5
DJNZ[1]	– –	2/7	2/7	3/9					
DSB	B, – –	1/7							
	RF, – –	2/10	2/10	3/12					
	%lop, – –	2/9	2/9	3/11					
EINT	– –								1/5
IDLE	– –								1/6 +
INC	– –	1/5	1/5	2/7					
INV	– –	1/5	1/5	2/7					
JMP	– –								2/7
Jcnd[1,2]	lab								2/5
LDA	– –					3/11	2/10	3/13	
LDSP	– –								1/5
MOV	A, – –		1/6	2/8					
	B, – –	1/5		2/7					
	RF, – –	2/8	2/8	3/10					
	%lop, – –	2/7	2/7	3/9					
MOVD	%lop, – –			4/15					
	%lop (B), – –			4/17					
	RF, – –			3/14					

[1]Add 2 to cycle count if branch is taken.

[2]Conditional Jump Instructions (see Table 3-21 of TMS7000 Family Data Manual.)

NOTATION:

Data Form – number of bytes/number of internal clock cycles.

A A register
B B register
RF Register File number
PF Peripheral File number
lab Label
lop Immediate operand

INSTRUCTION EXECUTION TIMES

OPERATION		ADDRESSING MODES							
		A	B	RF	PF	@ lab	* RF	@ lab (B)	OTHER
MOVP	A, - -				2/10				
	B, - -				2/9				
	%lop, - -				3/11				
	PF, - -	2/9	2/8						
MPY	B, - -	1/44							
	RF, - - - -	2/47	2/47	3/49					
	%lop, - -	2/46	2/46	3/48					
NOP	- -								1/4
OR	B, - -	1/5							
	RF, - -	2/8	2/8	3/10					
	%lop, - -	2/7	2/7	3/9					
ORP	A, - -				2/10				
	B, - -				2/9				
	%lop, - -				3/11				
POP	- -	1/6	1/6	2/8					
POP ST	- -								1/6
PUSH	- -	1/6	1/6	2/8					
PUSH ST	- -								1/6
RETI	- -								1/9
RETS	- -								1/7
RL	- -	1/5	1/5	2/7					
RLC	- -	1/5	1/5	2/7					
RR	- -	1/5	1/5	2/7					
RRC	- -	1/5	1/5	2/7					
SBB	B, - -	1/5							
	RF, - -	2/8	2/8	3/10					
	%lop, - -	2/7	2/7	3/9					
SETC	- -								1/5
STA	- -					3/11	2/10	3/13	
STSP	- -								1/6
SUB	B, - -	1/5							
	RF, - -	2/8	2/8	3/10					
	%lop, - -	2/7	2/7	3/9					
SWAP	- -	1/8	1/8	2/10					
TSTA	- -								1/6
TSTB	- -								1/5
TRAP n	- -								1/14
XCHB	- -	1/6	1/6	2/8					
XOR	B, - -	1/5							
	RF, - -	2/8	2/8	3/10					
	%lop, - -	2/7	2/7	3/9					
XORP	A, - -				2/10				
	B, - -				2/9				
	%lop, - -				3/11				

NOTATION:

Data Form – number of bytes/number of internal clock cycles.

A A register
B B register
RF Register File number
PF Peripheral File number
lab Label
lop Immediate operand

TEXAS INSTRUMENTS

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