FEBRUARY 1961

APPLICATION NOTES

DESIGN OF A *NOR* CIRCUIT FOR USE AS A BINARY ADDER

ABSTRACT

The transistor NOR circuit is discussed and its operating speed as a binary full-adder is evaluated with regard to turn-on and storage delays. A design procedure is presented for a NOR circuit which is to meet specified propagation delays and a design example is given.

DESIGN OF A NOR CIRCUIT FOR USE AS A BINARY ADDER

INTRODUCTION

The use of a transistor-resistor logic (TRL) circuit as the basic element in a binary half-adder has been presented at past electrical conventions.[1] Because of the logical operation performed by this circuit, it is usually referred to as a NOR circuit. There are several reports concerning the d-c design of a NOR logic element which insure that under worst case variations of supply voltages, resistors, and transistor parameters, the circuit will function properly. However, no attempt is made to design the NOR element for even moderate switching speeds and as a result, the circuit is potentially capable of faster operating speed than is usually realized.

This report will discuss the design of a NOR logic circuit to be incorporated into a binary full adder. A brief analysis of the operation of a NOR circuit will first be presented. The NOR elements will then be combined into a half-adder and also into a full-adder. Next, the importance of turn-on delay and turn-off delay (storage time) of the individual NOR circuits will be discussed. Following this, a design procedure for a NOR element will be outlined and an example will be given. Although the design emphasis is on a NOR circuit for use in a full-adder, the method of design is general and is applicable to any type of NOR logic block.

1. W. D. Rowe, "The Transistor NOR Circuit," *IRE Wescon Convention Record,* 1957, pt. 4, p. 231-45.

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NOR CIRCUIT OPERATION

Figure 1 is a diagram of a NOR circuit. The total number of input resistors is referred to as the fan-in factor (M) and the total number of output resistors is designated as the fan-out factor (N). Input and output resistors have equal values in this circuit; the output resistors serve as input resistors to succeeding NOR circuits as indicated in Figure 2.

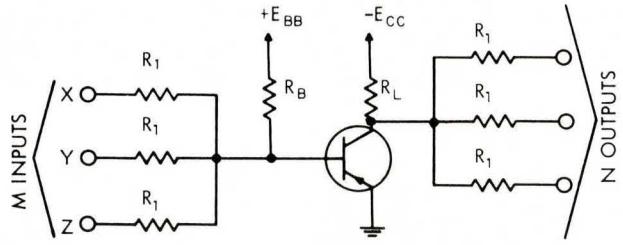

FIGURE 1 - NOR CIRCUIT

A negative signal to any of the input resistors of Figure 1 will cause the transistor to be in saturation and the collector voltage will be at ground potential. The collector voltage will be negative only when neither input X nor Y nor Z is negative. If binary 1 is regarded as the most negative level of a signal, the output of the circuit can be written:

$$\text{Output} = \overline{X + Y + Z}$$

where the right side of the equation is read "not X or Y or Z."

BINARY ADDITION WITH THE NOR CIRCUIT

Five NOR circuits can be combined into a binary half-adder as shown in Figure 3. The output of each NOR block is shown in terms of input signals to that block. Table 1 is a truth table for the outputs of blocks 4 and 5 for all combinations of X and Y. According to the rules for binary addition, a sum of 1 is obtained only when one input or the other, but not both, is at binary 1 and a carry of 1 occurs only when both inputs are at binary 1. NOR logic blocks 5 and 4 of Figure 3 thus give the correct sum and carry, respectively.

TABLE I

X	Y	Output of Block 5	Output of Block 4
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

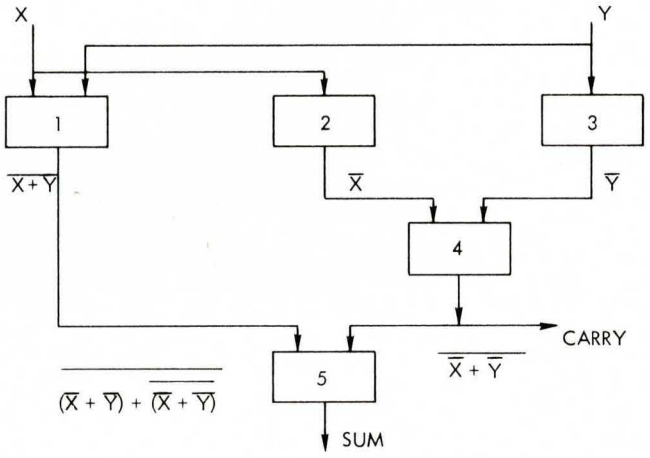

FIGURE 3 - BINARY HALF-ADDER

The binary half-adder has no provision for adding in a carry from a previous order and for this reason is called a half-adder. If two half-adders are combined as in Figure 4, a binary full-adder is obtained which can add in a carry from the next lower order bit position. Figure 5 shows four full-adders combined to add two four-bit numbers.

DELAYS IN THE FULL ADDER

It is important to consider delays encountered in the adder of Figure 5. The four inputs X_1, Y_1 through X_4, Y_4 are applied simultaneously to all adders. Correct carry-out and sum signals at any full adder cannot appear until a short time after all input signals, including the carry-out from the previous adder, have reached constant values. For example, assume that the output of any full adder appears 2 μsec after all input signals have reached a constant value. If C_{i4} is applied simultaneously with X_4 and Y_4, the output C_{04} will appear 2 μsec later. An additional lapse of 2 μsec is required for C_{03} to appear. The same delay is present for FA_2 and

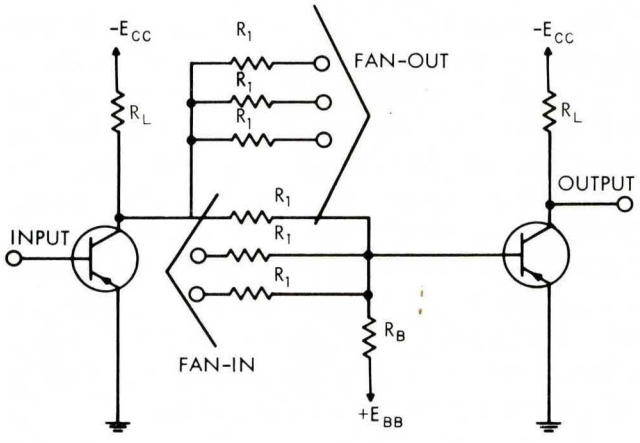

FIGURE 2 - CONNECTION OF NOR CIRCUITS

FA_1 to give a total delay of 8 μsec from application of input signals to the time correct output signals are realized.

The time delay associated with propagation of signals through a full adder is caused primarily by turn-on and storage delay of the NOR circuit. As the full adder is composed of two half-adders, an analysis of the delay occurring in a half-adder will be presented. Figure 6 shows the collector waveform for each NOR circuit in a half-adder under two separate operating conditions. Transistors used in the five NOR logic blocks are PNP transistors and a negative level is considered to be binary 1. Initially, inputs X and Y are at binary 0. The left hand column of Figure 6 shows that blocks 1, 2 and 3 are off while blocks 4 and 5 are turned on. Output waveforms at each collector are also shown in this column.

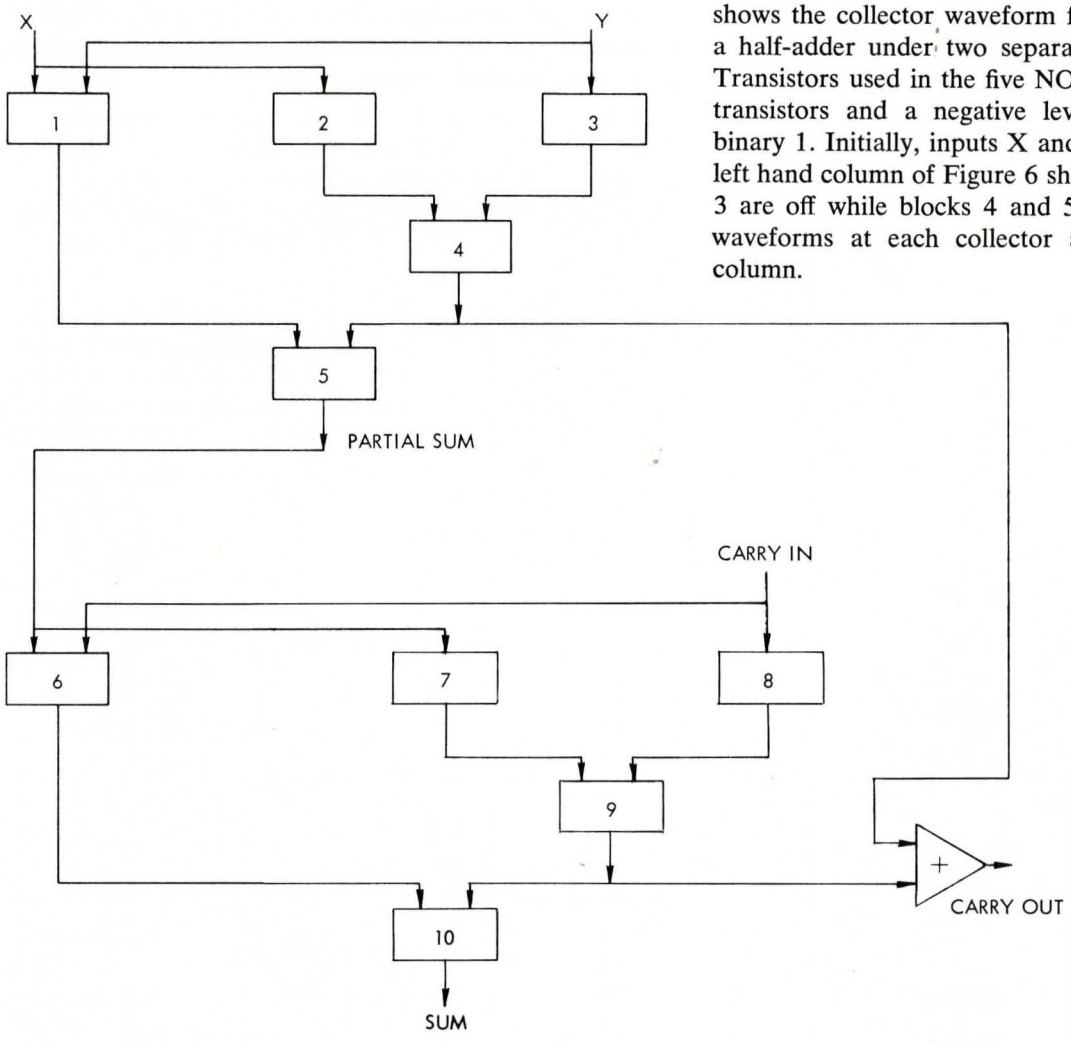

FIGURE 4 - BINARY FULL-ADDER

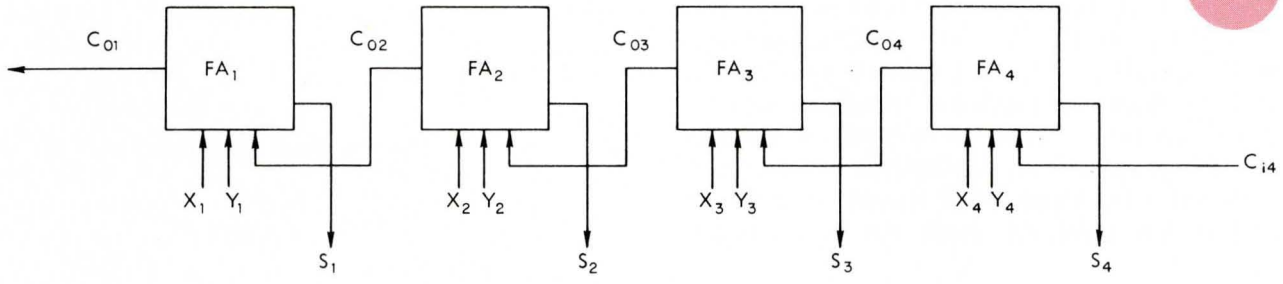

FIGURE 5

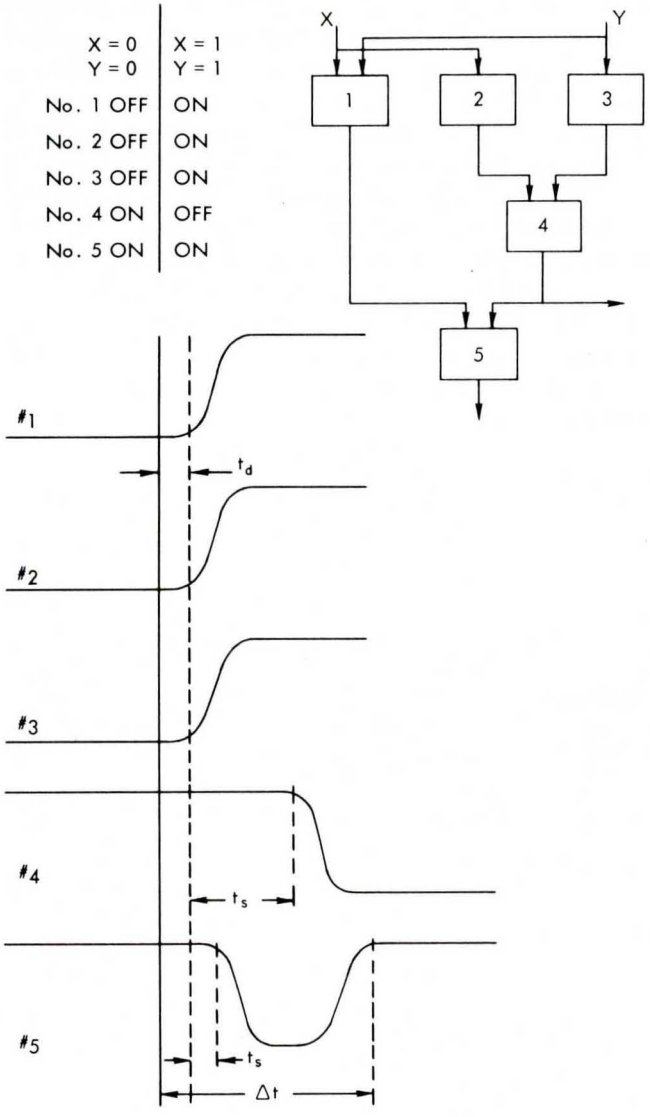

FIGURE 6

The second operating condition depicted in Figure 6 is for X and Y equal to binary 1. The collector voltage of blocks 1, 2 and 3 drops to zero volts. The input voltage to block 4 will not decrease until the transistors in blocks 2 and 3 have begun to turn on. Block 4 previously had two active inputs as compared to only one active input for block 5 and for this reason, the transistor associated with block 4 will remain in saturation longer than that of block 5. There may be an interval of time when all inputs to block 5 are at binary 0. Under this condition, the output voltage of block 5 will rise to a negative level and then fall to zero volts as block 4 comes out of saturation. Figure 6 shows that the correct output levels have not been established until a time ΔT has elapsed from application of the input signals. Consequently, the time required for performing addition is dependent upon t_d and t_s.

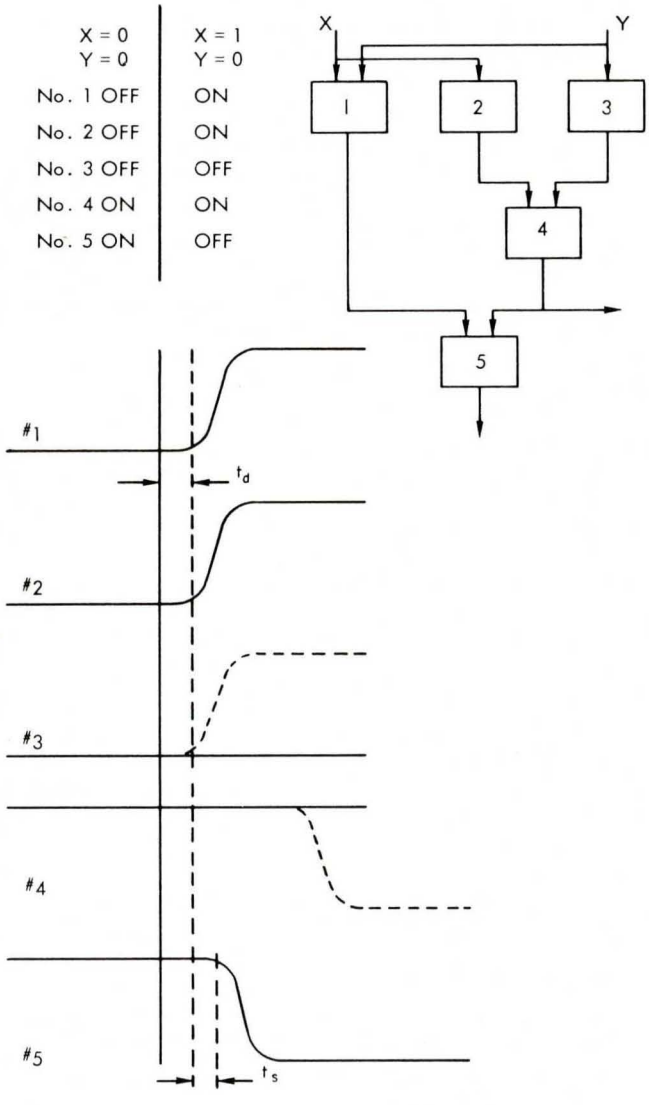

FIGURE 7

Figure 7 shows the condition where input X changes to binary 1 and input Y remains at binary 0. This figure reveals that less time is required for the outputs to reach final values than when both X and Y changed to binary 1.

NOR CIRCUIT DESIGN

The design method to be presented here employs a semi-graphical technique to determine values for R_1, R_B, and E_{BB} in the NOR circuit of Figure 2. These parameters are to be chosen so that the circuit will meet specified values of t_d and t_s.

A value of collector current (I_C) must be selected for the transistor to be used. This choice will depend upon the current rating of the transistor, the h_{FE} of the transistor at that current, and also upon loading at the collector (the collector current must be at least equal to the sum of all load currents).

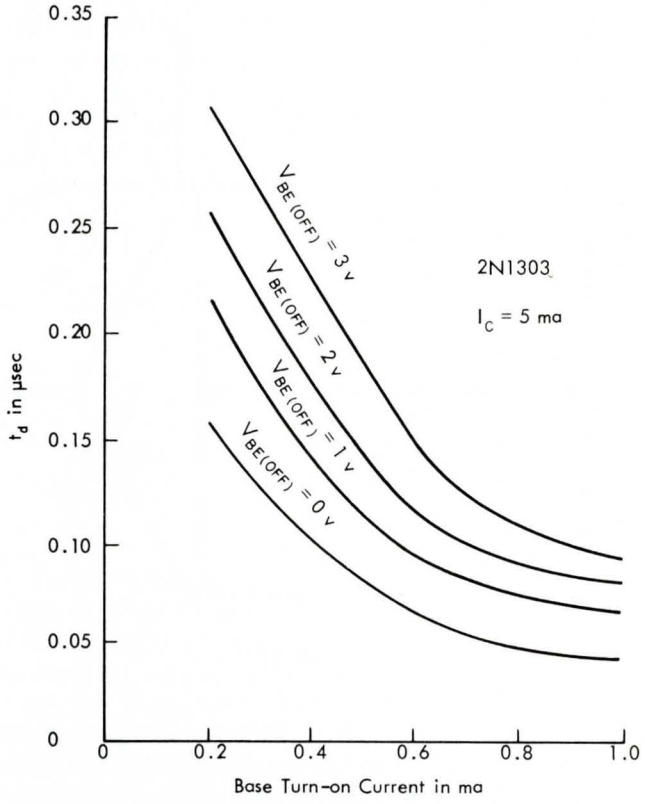

FIGURE 8

After a value of I_C has been chosen, it is necessary to obtain curves similar to those of Figures 8 and 9. Figure 8 is a plot of t_d versus base turn-on current for various values of $V_{BE(OFF)}$. For a given value of turn-on current, delay time is seen to increase as the value of base-emitter reverse voltage increases. Storage time is plotted versus base turn-on current in Figure 9 for various values of I_{B2} (base turn-off current). As I_{B2} increases, t_s decreases for constant values of turn-on current.

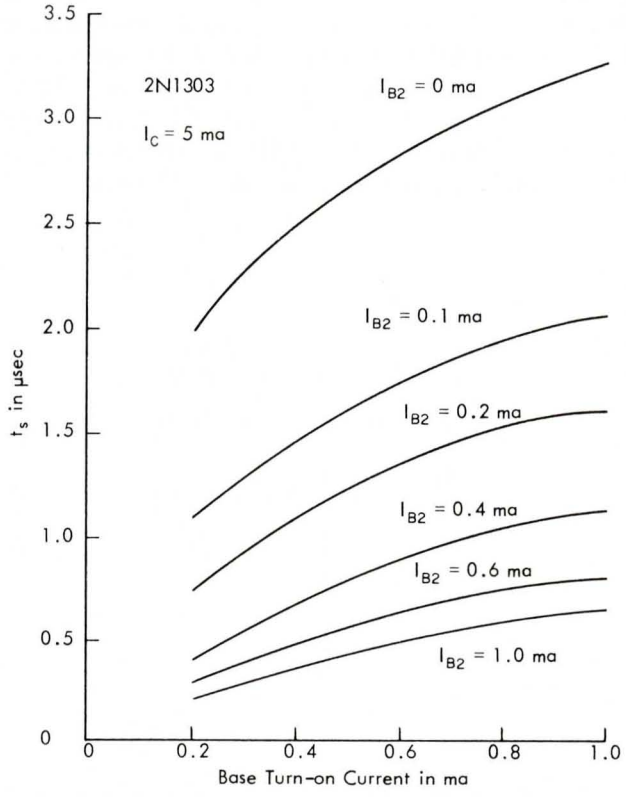

FIGURE 9

The effects of transistor rise and fall times are neglected in this design. Delay and storage times of a transistor stage are affected by the fall and rise times, respectively, of the driver transistor stages. The curves of Figures 8 and 9 are obtained with input pulses having rise and fall times which may be considerably different than the rise and fall times obtained at a transistor output. For this reason, measured delay and storage times are not expected to be the same as the design predicts.

Arbitrary values must be chosen for M, N, t_d max, t_s max, and $V_{BE(OFF)}$. Values for M and N are determined by the maximum number of inputs and outputs which the circuit must have. Delay and storage times must be small enough that the speed of the NOR circuit is compatible with other circuits in the over-all system, and $V_{BE(OFF)}$ must be sufficiently large to assure that off-transistor leakage currents will be negligible even at elevated temperatures.

Figure 8 is used, together with the values of t_d max and $V_{BE(OFF)}$, to determine the minimum value for base turn-on current. This is the minimum current which must be supplied to a NOR stage and occurs when all except one of the input transistors are in saturation and that input transistor alone must supply turn-on current to all other fan-out transistors. The minimum value of base turn-on current will be referred to as I_{B1}. An equivalent network for this condition is shown in Figure 10. Appendix A shows a derivation of this circuit.

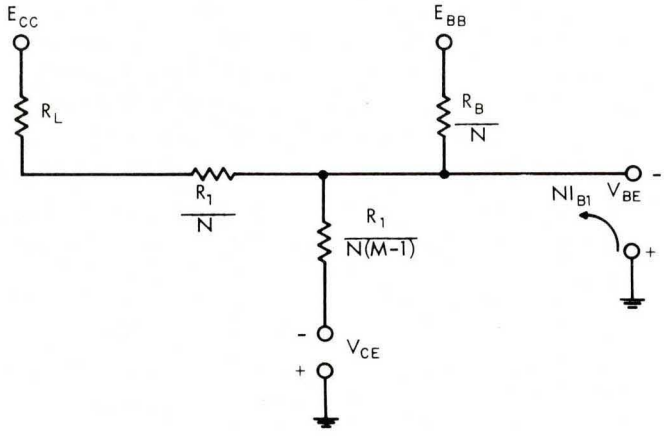

FIGURE 10

The maximum value of t_s occurs when all fan-in transistors connected to a stage are at cut-off. The base current supplied by each of these fan-in transistors is dependent upon loading of each transistor. If there is only one fan-out from each of these fan-in stages, the maximum amount of current will be supplied to the base of the on stage.

An approximate circuit with which to evaluate the maximum turn-on current to a transistor is shown in Figure 11. It is assumed that a negligible amount of current is required to turn on other transistors to which the fan-in transistors may be connected. A base turn-on current which is larger than the required value of I_{B1} is referred to as I_{B1}' and is given in equation (1) in terms of M, I_{B1}, and I_{B2}.

$$I_{B1}' = MI_{B1} + (M-1)I_{B2} \quad \ldots\ldots\ldots\ldots \quad (1)$$

The next step in the design is to determine a value of I_{B2} to give the required maximum value for t_s. The curves of Figure 9 cannot be used directly as values for I_{B1}' and I_{B2} are not known. An approximate expression for the curves in Figure 11 is given in equation (2).

$$t_s = \frac{0.3}{I_{B2}} + 0.3\, I_{B1}' \quad \ldots\ldots\ldots\ldots \quad (2)$$

Substitution of equation (1) into equation (2) gives

$$t_s = \frac{0.3}{I_{B2}} + 0.3\, MI_{B1} + 0.3(M-1)I_{B2} \quad \ldots\ldots\ldots \quad (3)$$

Equation (3) can be solved for I_{B2} in terms of t_s and I_{B1}.

Three simultaneous equations must now be solved for R_1, R_B, and E_{BB}. These equations are listed below:

$$I_{B1} = \frac{E_{CC} - V_{BE}}{NR_L + R_1} - \frac{(E_{BB} + V_{BE})}{R_B} - \frac{(M-1)(V_{BE} - V_{CE})}{R_1} \quad \ldots \quad (4)$$

$$I_{B2} = \frac{E_{BB} + V_{BE}}{R_B} + \frac{M(V_{BE} - V_{CE})}{R_1} \quad \ldots\ldots\ldots \quad (5)$$

$$V_{BE(OFF)} = \frac{R_1(E_{BB} + V_{CE})}{MR_B + R_1} - V_{CE} \quad \ldots\ldots\ldots \quad (6)$$

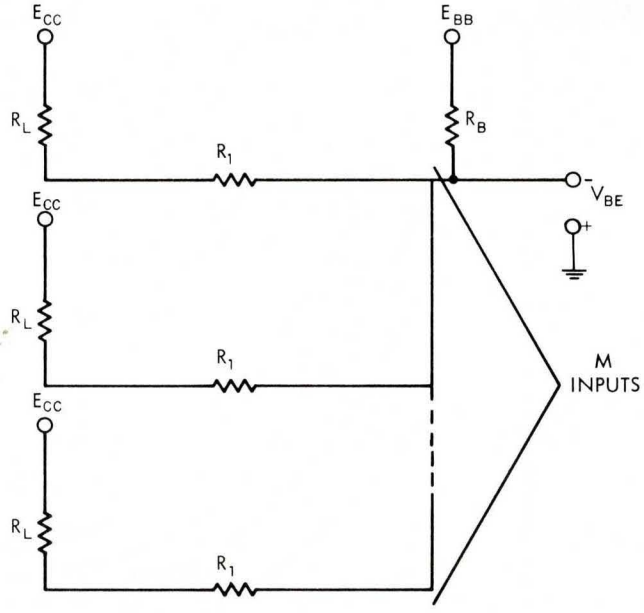

FIGURE 11

Equation (4) is obtained from the circuit of Figure 10. Equations (5) and (6) are derived from the circuit shown in Figure 12. This figure shows an equivalent input circuit to the base of an off transistor when all input transistors are in saturation. The value of I_{B2} is determined for the brief interval of time when the fan-in collector voltages have decreased to saturation values,

but the base emitter voltage of the fan-out transistor has not yet changed. Equation (6) is a steady-state expression for the value of $V_{BE(OFF)}$.

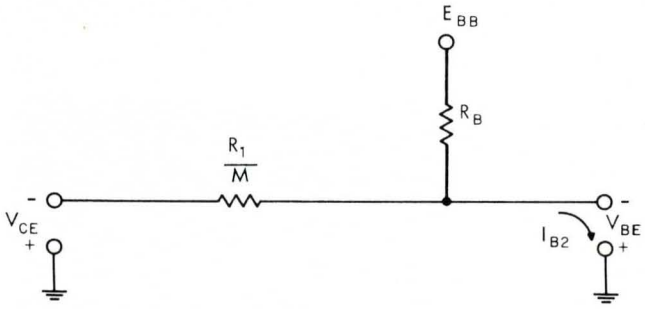

FIGURE 12

DESIGN EXAMPLE

A design example will now be presented for a NOR circuit having both M and N equal to two. This will allow it to be used as any of the logic blocks in Figure 4. The following values are arbitrarily chosen: $E_{CC} = 20V$, $R_L = 4$ K, t_d max $= 0.15$ μsec, $V_{BE(OFF)} = 1.0$ V, and t_s max $= 1.0$ μsec. The 2N1303 transistor is to be used.

Figures 8 and 9 have been plotted for the 2N1303 transistor with $I_C = 5$ ma. The input pulse source had rise and fall times of 20 mμsec. From Figure 8, I_{B1} is determined to be 0.37 ma. Substitution of this value into equation (3) gives a value of 0.47 ma for I_{B2}. Values for saturated collector-emitter voltage and base-emitter on voltage are chosen as 0.1 and 0.35 volts respectively. A simultaneous solution of equations (4), (5) and (6) gives the following:

$R_1 = 15.7K$

$R_B = 4.5K$

$E_{BB} = 1.6V$

DESIGN RESULTS

Ten NOR circuits were built and incorporated into the full adder of Figure 4. Values for R_1, R_B, and E_{BB} were as determined in the design example. Unused input and output resistors were grounded. A delay time of 0.5 μsec was measured for block 4 for the condition where the output of block 3 went from saturation to cutoff and the output of block 2 remained in saturation. The maximum storage time of block 4 was measured to be 1.8 μsec and occurred when the outputs of blocks 2 and 3 changed from a negative value to saturation.

The output rise and fall times of either block 2 or block 3 were measured to be 0.8 μsec and 0.4 μsec, respectively. These values are much larger than the 20 mμsec rise and fall times of the pulse generator used to obtain the curves of Figures 8 and 9. This explains the discrepancy between design and measured delay and storage times.

The over-all delay of the full adder was measured to be 2.6 μsec for the sum output and 2.5 μsec for the carry out output.

APPENDIX

An equivalent circuit is to be derived for the case where one NOR circuit must supply base turn-on current to several other NOR circuits. The fan-out and fan-in of a circuit are N and M, respectively. Figure A1 shows that transistor T_1 is off and transistors T_2, T_3, ... T_N are turned on. Each of the fan-out transistors has all inputs, except one, connected to the collector of saturated transistors. Thus, there are M-1 input resistors which are connected to each base and also to V_{CE}. These resistors are shown as the equivalent resistance, $\frac{R_1}{M-1}$, to each base.

From Figure A1,

$$I_4 = \frac{E_{BB} + V_{BE}}{R_B} + I_{B1} + \frac{V_{BE} - V_{CE}}{\frac{R_1}{M-1}} \quad \text{(A1)}$$

where the positive value of each voltage is to be used. Current through R_L is the sum of all currents entering the junction at point A. Hence,

$$I_C' = NI_4 = \frac{E_{BB} + V_{BE}}{R_B/N} + NI_{B1} + \frac{V_{BE} - V_{CE}}{R_1/N(M-1)} \quad \text{(A2)}$$

The current I_C' in the circuit of Figure A2 is given by equation (A2). Thus, this circuit is equivalent to the circuit of Figure A1.

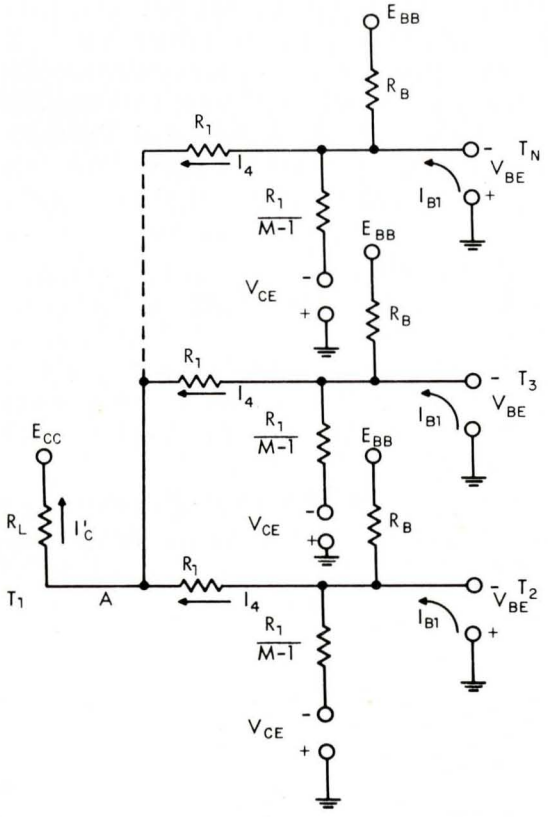

FIGURE A1

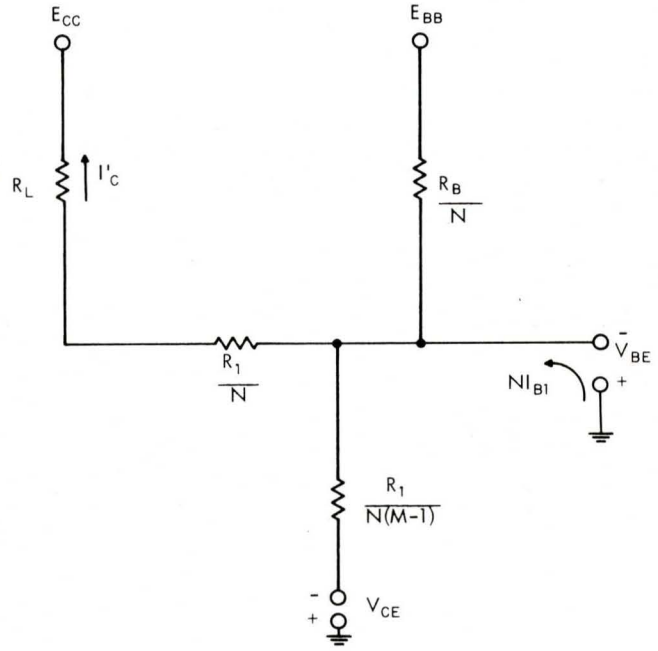

FIGURE A2

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