TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T C 9 4 A 0 9 F

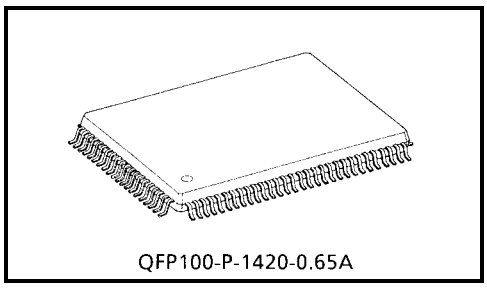
Single-Chip CD Processor with Built-in Controller

The TC94A09F is a single-chip CD processor for digital servo. The IC has a built-in 4-bit microcontroller.

The controller features an LCD/LED driver, 4-channel 6-bit AD converter, 2/3-line serial interface, buzzer, interrupt function, and 8-bit timer/counter. The CPU can select one of three crystal oscillator operating clocks (16.9344 MHz, 4.5 MHz, and 75 kHz), facilitating interface with the CD processor.

The CD processor incorporates sync separation protection and interpolation, EFM decoder, error correction, digital equalizer for servo, and servo controller. The CD processor also incorporates a 1-bit DA converter. In combination with a RF amp TA2153FN and TA2109F, the TC94A09F can very simply configure an adjustment-free CD player.

Thus, the IC is suitable for CD systems for automobiles and radio-cassette players.



Weight: 1.6 g (typ.)

Features

- Single-chip CD processor with built-in CMOS LCD/LED driver and 4-bit microcontroller
- Operating voltage: At CD on: V_{DD} = 4.5 to 5.5 V (typ. 5.0 V)
  At CD off: V_{DD} = 3.0 to 5.5 V (only CPU on)
- Current dissipation: At CD on: I_{DD} = 50 mA (typ.)
  At CD off: I_{DD} = 2 mA (with 4.5 MHz crystal oscillator, only CPU on)
  At CD off: I_{DD} = 0.3 mA (with 75 kHz crystal oscillator, only CPU on)
- Operating temperature range: Ta = −40 to 85°C
- Package: QFP100-P-1420-0.65A (0.65 mm pitch, 2.7 mm thick)
- One-time PROM version: TC94AP09F

4-bit Microcontroller

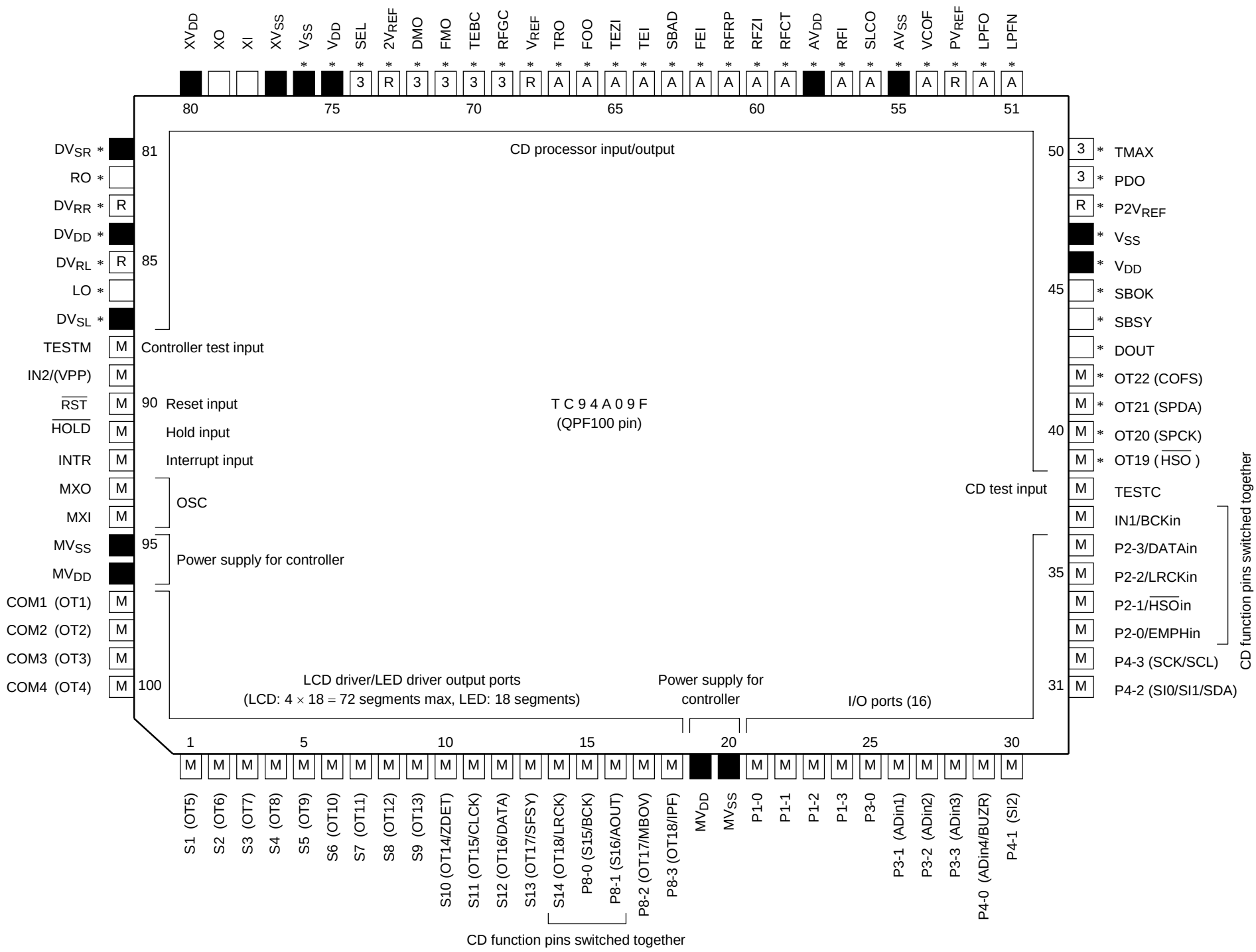
- Program memory (ROM): 16-bit × 12-k step
- Data memory (RAM): 4-bit × 512-word
- Instruction execution time: 1.89/1.78/40 μs (all one-word instructions)
- Crystal oscillator frequency: 16.9344 MHz/4.5 MHz/75 kHz
- Stack level: 8
- AD converter: 6-bit × 4-channel
- LCD driver: 1/4 duty, 1/2 or 1/3 bias method, 72 segments max
- LED driver: 4-digit × 14-segment (max), also used as LCD driver switched by software
- I/O port: CMOS I/O port: 16
  N-channel open drain I/O port: 4 (max)
  Output-only port: 4 (max), also used as CD processor pins
  Input-only port: 4
- Timer/counter: 8 bit (INTR, instruction cycle, 100/1 kHz selectable as timer clock)
  10, 100, or 500 Hz: internal port
  2 Hz: Flip-flop port
- Serial interface: Supports 2/3-line method (data length: 4 or 8 bits)
- Buzzer: Four types: 0.75, 1, 1.5, and 3 kHz
  Four modes: Continuous, Single-Shot, 10 Hz Intermittent, and 10 Hz Intermittent at 1 Hz Interval
- Interrupts: 1 external, 3 internal (CD sub-sync, serial interface, 8-bit timer)
- Back-up mode: three types
  Clock stop mode: X'tal operation stop
  Hardware wait mode: X'tal oscillation operation, no operation in CPU
  Software wait mode: Intermittent operation
- Reset function: Power-on reset, Built-in supply voltage detection circuit (Detection voltage = 2.5 V typ.)

CD Processor

- Reliable sync pattern detection, sync signal protection and interpolation
- Built-in EFM decoder and sub code decoder
- High-correction capability using cross interleave read Solomon code (CIRC) logical equation
  C1 correction: dual
  C2 correction: quadruple
- Supports variable speeds
- Jitter absorption capability of ±6 frames
- Built-in 16 KB RAM
- Built-in digital output circuit
- Built-in L/R independent digital attenuators
- Bilingual audio output (Note)
- Sub code Q data are read-timing free and can be output in sync with audio data. (Note)
- Built-in data slice and analog PLL (adjustment-free VCO used) circuit
- Auto adjustment of loop gain, offset, and balance at focus servo and tracking servo
- RF gain auto adjustment circuit
- Built-in digital equalizer for phase compensation
- Supports different pickups using digital equalizer coefficient RAM.
- Built-in focus and tracking servo control circuit
- Search control supports all modes and realizes high-speed, stable search.
- Lens kick and feed kick use speed control method.
- Built-in AFC circuit and APC circuit for disc motor CLV servo
- Built-in defect/shock detector
- Built in 8 times oversampling digital filter and 1-bit DA converter

(Note) Output pins for sub code Q data and audio data are also used as LCD driver pins. The function of the pins can be switched by program.

Pin Connections



(Note) Symbols for the pins used above indicate the following pin functions:

* : CD processor-dedicated pin

■ : Power supply pin

3 : CD processor tri-state output pin

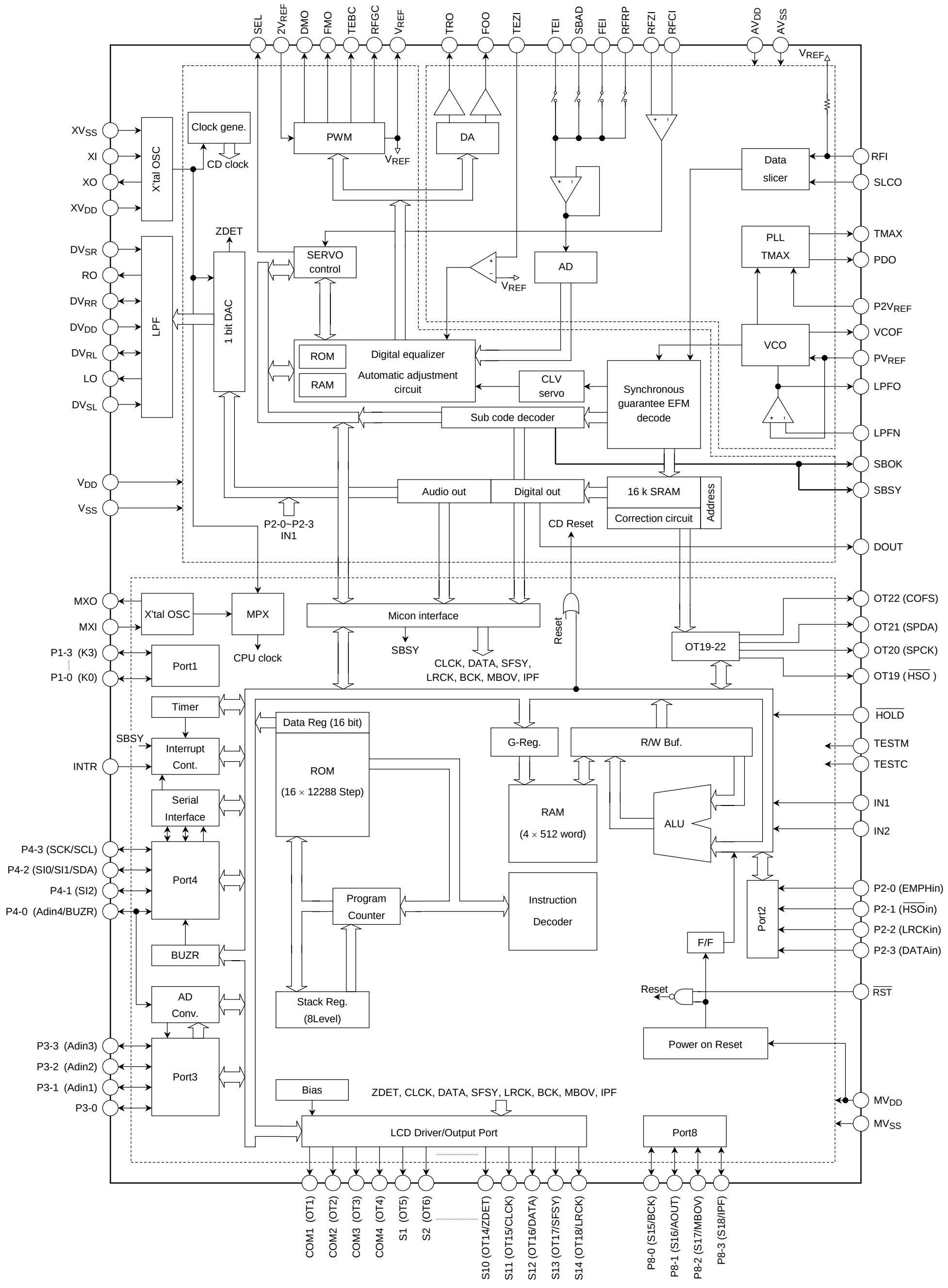
A : CD processor analog input/output pin

R : Reference input pin

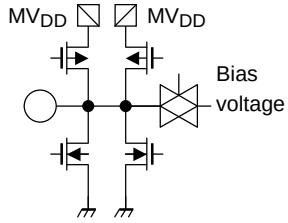
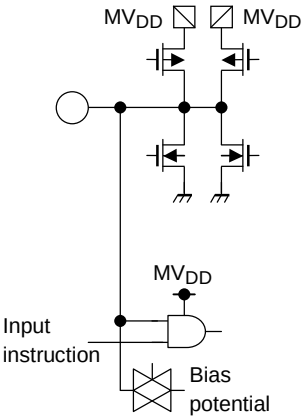
M : Controller-dedicated pin

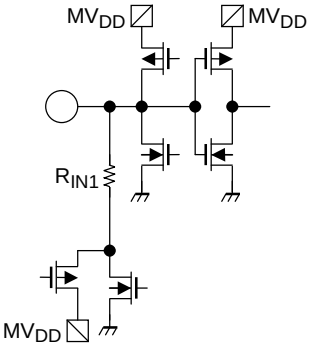
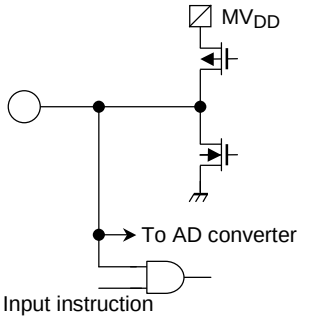
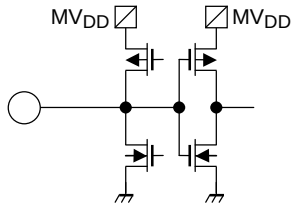
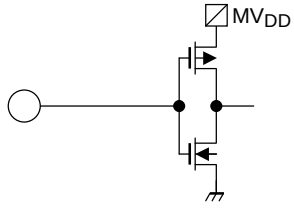
(Note) When the CD is off, the power supply pins for the controller (MV_{DD}) and the power pins supply for the CD oscillator (XV_{DD}) are on and the CD processor-dedicated power supply (indicated by an asterisk *) pins are off.

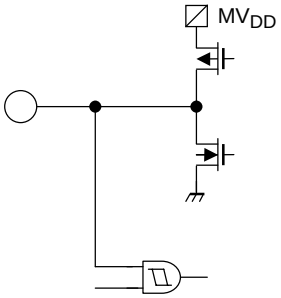
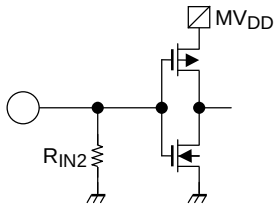
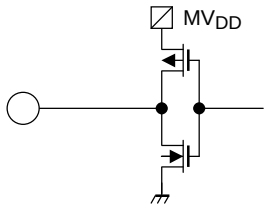
Block Diagram

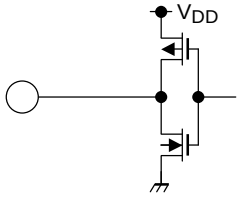
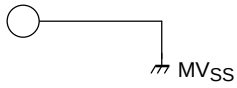
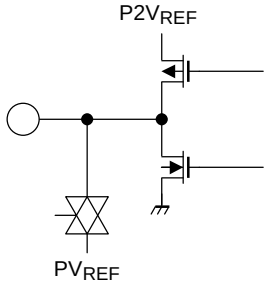
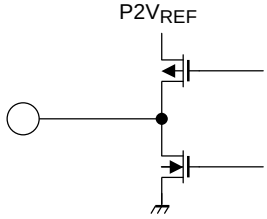
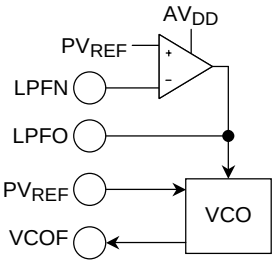
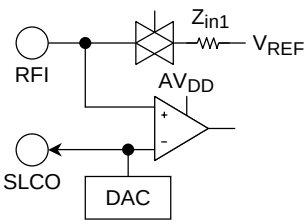


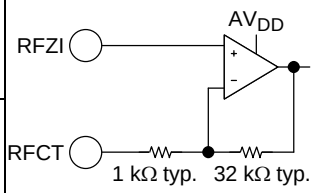
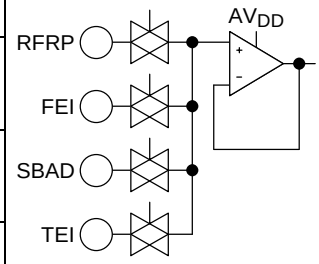
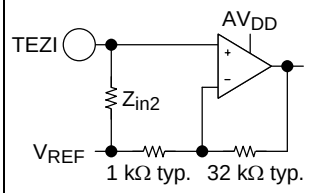
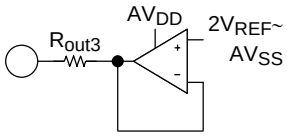
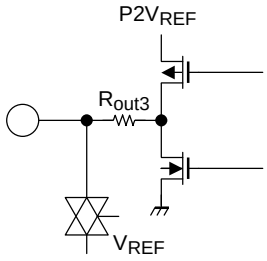
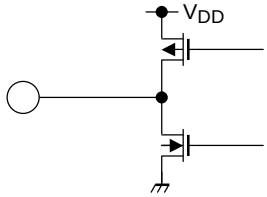
Pin Descriptions

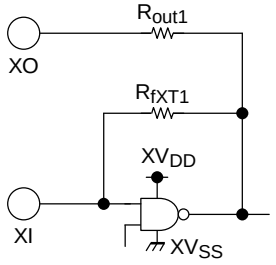
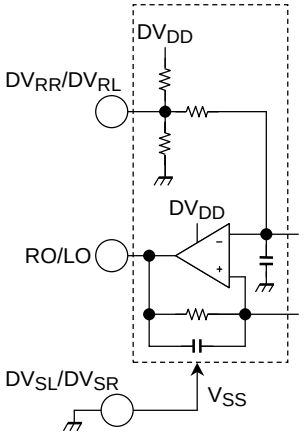
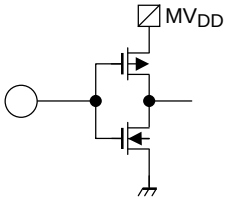
Pin Number	Symbol	Pin Name	Function and Operation	Remarks
97	COM1/OT1	LCD common output /output port	Common signal output pins for the LCD panel. Those pins configure matrix with S1 to S18 and display up to 72 segments. The LCD can be driven by the 1/2 or 1/3 bias method. When the 1/2 bias method is set three levels, MV_{DD}, 1/2MV_{DD}, and GND, are output at 2-ms intervals. When the 1/3 bias method is set four levels, MV_{DD}, 1/3MV_{DD}, 2/3MV_{DD}, and GND, are output at a 62.5 Hz cycle (when either the 4.5 MHz or 75 kHz crystal oscillator is used). After system reset or clock stop execution is released, the non-selected waveform (bias voltage) is output. The DISP OFF bit is set to 0 and the common signal is output. These pins can be switched to an output port (Note1) or LED driver pins by program. They are usually used for digit output to drive the LEDs.	
98	COM2/OT2			
99	COM3/OT3			
100	COM4/OT4			
1~9	S1/OT4 ~ S9/OT13	LCD segment output /output port	Segment signal output pins for the LCD panel. Those pins configure a matrix with COM1 to COM4 and display up to 72 segments. When the 1/2 bias method is set two levels, MV_{DD} and GND, are output. When the 1/3 bias method is set four levels, MV_{DD}, 1/3MV_{DD}, 2/3MV_{DD}, and GND, are output. The S1 to S14 pins can be switched to an output port (Note1) by program. Port 8 and S15 to S18 pins can be switched pin by pin to an I/O port and segment output pins. When the pins are set to an I/O port, output is N-channel open drain. The S10 to S14 and P8-0 to P8-3 pins can be switched to CD signal input/output pins by program. Setting the CD10 bit to 1 switches the pins to the LRCK, BCK, and AOUT pins as the CD pins in batches. The other pins can be individually switched according to the S14/S15/S16 segment data. ・CLCK Inputs/outputs sub code P to W data reading clock. ・DATA Outputs sub code P to W data. ・SFSY Outputs frame sync signal for playback. ・LRCK Outputs channel clock (44.1 kHz). When L channel, outputs Low. When R channel, outputs High. The polarity can be inverted by command. ・BCK Outputs bit clock (1.4112 MHz). ・AOUT Outputs audio data. ・MBOV Outputs buffer-memory-overflow signal. When buffer memory overflows, outputs H. ・IPF Outputs interpolation pointing flag. If AOUT output is C2 error detection/correction, outputs High to indicate correction is impossible. ・ZDET Outputs 1-bit DAC zero detection flag. Pins set as an output port are used for segment output for the LED driver. The output port can increment OT1 to OT18 by instruction, facilitating access to data in external RAM and ROM. (Note1) After a system reset, pins also used as output ports are set to LCD output; pins also used as I/O ports are set to I/O port input.	
10	S10/OT14 /ZDET	LCD segment output /output port /CD signal		
11	S11/OT15 /CLCK			
12	S12/OT16 /DATA			
13	S13/OT17 /SFSY			
14	S14/OT18 /LRCK			
15	P8-0/S15 /BCK	I/O port /LCD segment output /CD signal		
16	P8-1/S16 /AOUT			
17	P8-2/S17 /MBOV			
18	P8-3/S18 /IPF			

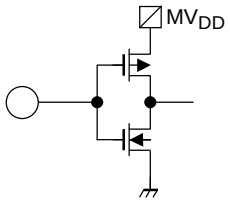
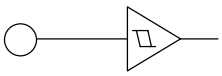
Pin Number	Symbol	Pin Name	Function and Operation	Remarks
21~24	P1-0~P1-3	I/O port 1	4-bit CMOS I/O port. Input/output can be set for each bit by program. The pins can be set to be pulled-up or pulled-down by program. Thus, they can be used as key input pins. When the pins are set to I/O port input, Clock Stop mode and Wait mode can be released, according to the change in input to the pins.	
25	P3-0	I/O port 3	5-bit CMOS I/O port. Input/output can be set for each bit by program. P3-1 and P4-0 pins are also used as built-in 6-bit 4-channel AD converter analog input pins. The built-in AD converter uses successive approximation. The conversion time is 6 instruction cycles (280 μs) when the 75 kHz crystal oscillator is used; 198 μs when the 4.5 MHz crystal oscillator is used; 180 μs when the 16.9344 MHz crystal oscillator is used. AD analog input can be set for each pin by program. The internal power supply (MV_{DD}) is used as the reference voltage. The P4-0 pin is also used as the buzzer output pin. One of four frequencies: 0.75, 1, 1.5, and 3 kHz, can be selected for buzzer output. The buzzer is output at the selected frequency at 1 Hz intervals in one of four modes: Continuous, single-shot, 10 Hz intermittent, and 10 Hz intermittent at 1 Hz interval. Settings for the AD converter and buzzer, and their control can be performed by program.	
26~28	P3-1/ADin1 ~ P3-3/ADin3	I/O port 3 /AD analog voltage input		
29	P4-0 /ADin4 /BUZR	I/O port 4 /AD analog voltage input /buzzer output		
33 34 35 36	P2-0 /EMPHin P2-1/HSOin P2-2 /LRCKin P2-3 /DATAin	I/O port 2 /1-bit DAC input	I/O port 2 is a 4-bit CMOS I/O port. IN1 and IN2 are a 2-bit general-purpose input port. Input/output can be set for each bit of I/O port 2 by program. I/O port 2 and the IN1 pin can be switched to 1-bit DAC input pins by the CD command to support shock-proofing functions. In this case, the I/O port must be set to input. With the OTP version, the IN2 pin is also used as the program power supply pin.	
37 89	IN1/BCKin IN2/ (VPP)	General-purpose input port /1-bit DAC input (VPP input)		

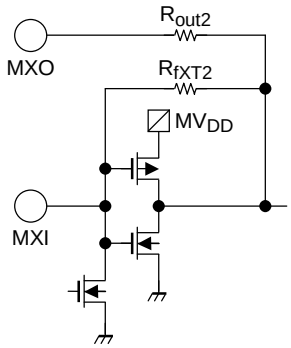
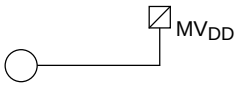
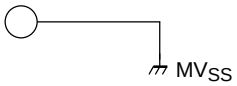
Pin Number	Symbol	Pin Name	Function and Operation	Remarks
30 31 32	P4-1/S12 P4-2 /SI0/SI1/ SDA P4-3 /SCK/SCL	I/O port 4 /Serial data input /Serial data input/output /Serial clock input/output	3-bit CMOS I/O port. Input/output can be set for each bit by program. These pins are also used as serial interface (SIO) circuit input/output pins. SIO is a serial interface supporting 2-line and 3-line methods. Starting from the MSB or LSB, 4 or 8-bit serial data are output to the SO/SDA pin, or data on the S11 and S12 pins are input to the device at the clock edge on the SCK/SCL pin. As the serial operating clock (SCK/SCL), an internal (450/225/150/75 kHz) or external clock can be selected. Rising or falling shift can also be selected. The clock and data output can be N-channel open drain. These selections facilitate controlling the LSI and communications between the controllers. When SIO interrupts are enabled, an interrupt is generated as soon as execution of the SIO completes, and the program jumps to address 4. This is effective for performing serial communications at high speed. All SIO inputs incorporate a Schmidt circuit. SIO and its control can be set by program.	 Input instruction + $SI0_{ON}$
38 88	TESTC TESTM	Test mode control input	Input pins for controlling Test mode. When the pins are at High level, the device is in Test mode; at Low level, in normal operation. Normally, set the pins to Low level or NC (pull-down resistors are incorporated).	
39~42	OT19/ $\overline{HSO}$ OT20/SPCK OT21/SPDA OT22/COFS	Output port /CD control signal output	4-bit general-purpose output port. After system reset, the pins are set to a Low-level output port. The pins can be switched to CD control output pins by program. Setting OT19 to OT22 to 0 switches all four pins to CD control output pins. Setting the CDIO bit to 1 enables the pins to be switched as follows according to the segment data contents of the S15 and S16 pins: ・$\overline{HSO}$ Outputs playback speed mode. Normal speed: High Double speed: Low ・SPCK Outputs clock for reading processor status signal (176.4 kHz). ・SPDA Outputs processor status signal. ・COFS Outputs frame clock for correction (7.35 kHz).	

Pin Number	Symbol	Pin Name	Function and Operation	Remarks
43	DOUT	CD processor control input/output	Digital out output pin.	
44	SBSY		Sub code block sync output pin. When sub code sync is detected, outputs High at the S1 position.	
45	SBOK		Sub code Q data CRCC result output pin. When the result is OK, outputs High.	
46, 75	V_{DD}		Power supply pins for CD digital block. Normally, 5 V is applied. When CD is not used (CD off), the power supply can be set to off, but only the controller power supply can be set to on, enabling the controller to operate. At this time, 1 must be set in the CDoff bit. If pins from 11 to 18 and 39 to 42 are set as CD control signal input/output pins, setting the CDoff bit to 1 switches all the pins to an output port.	
47, 76	V_{SS}			
48	$P2V_{REF}$		$2V_{REF}$ pin for PLL block	—
49	PDO		Outputs phase error signal between the EFM and PLCK signals.	
50	TMAX		TMAX detection result output pin. Selected by command bit TMPS. Longer than the specified cycle: Outputs $P2V_{REF}$. Shorter than the specified cycle: Outputs Low level (V_{SS}). Within the specified cycle: at high impedance	
51	LPFN		Inverted input pin for low-pass filter amp.	
52	LPFO		Output pin for low-pass filter amp.	
53	PV_{REF}		V_{REF} pin for PLL block	
54	VCOF		VCO filter pin	
55	AV_{SS}		Ground pin for analog block	—
56	SLCO		DAC output pin for generating data slice level	
57	RFI		RF signal input pin	
58	AV_{DD}		Power supply pin for analog block	—

Pin Number	Symbol	Pin Name	Function and Operation	Remarks
59	RFCT	CD processor control input/output	RFRP signal center level input pin	
60	RFZI		RFRP zero-cross signal input pin	
61	RFRP		RF ripple signal input pin	
62	FEI		Focus error signal input pin	
63	SBAD		Sub beam addition signal input pin	
64	TEI		Tracking error input pin. The pin is read at tracking servo on.	
65	TEZI		Tracking error/zero-cross signal input pin	
66	FOO		Focus equalizer output pin	
67	TRO		Tracking equalizer output pin	
68	V_{REF}		Analog reference voltage power supply pin	—
69	RFGC		Control signal output pin for adjusting RF amplitude. Outputs tri-state PWM signal (PWM carrier = 88.2 kHz).	
70	TEBC		Tracking balance control signal output pin. Outputs tri-state PWM signal (PWM carrier = 88.2 kHz).	
71	FMO		Focus equalizer output pin. Outputs tri-state PWM signal (PWM carrier = 88.2 kHz).	
72	DMO		Disc equalizer output pin. Outputs tri-state PWM signal (PWM carrier = 88.2 kHz for DSP block, in sync with PXO).	
73	$2V_{REF}$		Analog reference voltage power supply pin ($2 \times V_{REF}$)	—
74	SEL		APC circuit on/off signal output pin. At laser on, high impedance at UHS = High; H level output at UHS = High.	

Pin Number	Symbol	Pin Name	Function and Operation	Remarks
77	XV_{SS}	CD processor crystal oscillator pins	Power supply pins for CD crystal oscillator. To control the CD processor power supply and the controller power supply individually, connect the MV_{DD} and MV_{SS} pins to the power supply lines used in common for the V_{DD} and V_{SS} pins.	—
80	XV_{DD}			
78	XI		CD crystal oscillator input/output pins. Connect a 16.9344 MHz crystal oscillator. The clock is used as the CD system clock and controller system clock. After system reset, this clock is supplied as the controller system clock and starts the CPU. The crystal oscillator can be halted by program. If the 4.5 MHz or 75 kHz oscillator is selected as the controller system clock, the oscillator is halted by program when the CD processor is off. (Note) When switching the controller system clock from the controller oscillator to the CD crystal oscillator, make sure that the CD crystal oscillator is in stable state.	
79	XO			
81	DV_{SR}	CD processor control input/output	R-channel DA converter block ground pin	
82	RO		R-channel data forward rotation output pin	
83	DV_{RR}		R-channel reference voltage pin	
84	DV_{DD}		DA converter block power supply pin	
85	DV_{RL}		L-channel reference voltage pin	
86	LO		L-channel data forward rotation output pin	
87	DV_{SL}		L-channel DA converter block ground pin	
90	$\overline{RST}$	Reset input	Device system reset signal input pin While the $\overline{RST}$ is at Low level, reset is applied. When the $\overline{RST}$ is at High level, the CD block is in operation, and the controller program starts from address 0. Normally, when 2.7 V or higher voltage is supplied to the MV_{DD} when at 0 V, system reset is applied (power-on reset). Fix the pin to High level.	

Pin Number	Symbol	Pin Name	Function and Operation	Remarks
91	$\overline{HOLD}$	Hold mode control input	Input pin used to request or release hold state. Normally, the pin is used for inputting the CD mode selection signal or battery detection signal. Halt states are Clock Stop mode (crystal oscillator stops oscillation) and Wait mode (CPU stops). The modes are entered using the CKSTP and WAIT instructions. By program, Clock Stop mode can be entered by detection of Low level on the $\overline{HOLD}$ pin or by forced execution. Clock Stop mode can be released by detection of High level on the $\overline{HOLD}$ pin or change in the $\overline{HOLD}$ pin input. Executing the CKSTP instruction stops the clock generator and the CPU, entering memory backup state. During memory backup state, current dissipation becomes low (1 μA or below). The display output and CMOS output port automatically become Low level. The N-channel open drain output becomes off. Regardless of the $\overline{HOLD}$ pin input state, Wait mode is executed and current dissipation becomes low. Crystal oscillator only on or CPU operation suspended can be programmed. When the crystal oscillator only is on, all displays are at Low level. The other pins are in hold state. When CPU operation is suspended, all states are held except that the CPU is suspended. Wait mode is released by a change of the $\overline{HOLD}$ pin input. (Note) For Backup mode, use the oscillator connected to the MXO and MXI pins. Turn off the V_{DD} pin (power supply for CD), and enter Backup mode.	
92	INTR	External interrupt input	External interrupt input pin. When interrupts are enabled and a pulse of 1.11 to 3.33 μs or more (13.3 to 40 μs when the 75 kHz clock is used) is input to this pin, an interrupt is generated and the program jumps to address 1. Input logic and rising/falling edge can be individually selected for interrupt inputs. The internal 8-bit timer clock can be selected for interrupt inputs. Interrupts can be generated (address 3) by pulse count or the count value. Interrupt inputs are Schmidt inputs. The pin can be used as an input port for inputs such as remote control signals.	

Pin Number	Symbol	Pin Name	Function and Operation	Remarks
93	MXO	Crystal oscillator for controller	Crystal oscillator pins for the controller. The oscillator clock is used as a time base for the clock function as well as the system clock for the controller. After system reset, the CPU starts operation using the 16.9344 MHz CD oscillator (connected to the XI and XO pins). The oscillator is switched to the controller oscillator by program. Either a 4.5 MHz reference oscillator or a 75 kHz oscillator is connected to the MXO and MXI pins. The oscillators are switched by a bit used to select a frequency of 4.5 MHz or 75 kHz. The oscillators incorporate a feedback resistor. Switching frequencies automatically switches the feedback resistor of the crystal oscillator. 75 kHz: R_{out2} = 2 kΩ, R_{fXT2} = 10 MΩ typ. 4.5 MHz: R_{out2} = 2 kΩ, R_{fXT2} = 1 MΩ typ. If the operating clock is the CD crystal oscillator, fix the MXI pin to GND. During execution of the CKSTP instruction, oscillation halts. Selection and control of crystal oscillators are done by program. (Note) When the 75 kHz crystal oscillator is used, externally add/connect a 100 kΩ output resistor.	
94	MXI			
19, 96	MV_{DD}	Power supply pins for controller block	Power supply pins for the controller block. Normally, V_{DD} = 4.5 to 5.5 V. In backup state (when executing the CKSTP instruction), current dissipation becomes low (1 μA or below), dropping the power supply voltage to 2.0 V. If 2.7 V or more is applied to these pins when at 0 V, a system reset is applied to the device and the program starts from address 0 (power-on reset). (Note) At power-on reset operation, allow 10 to 100 ms while the device power supply voltage rises.	
20, 95	MV_{SS}			

Maximum Ratings (Ta = 25°C, $V_{DD} = DV_{DD} = AV_{DD}$, $MV_{DD} = XV_{DD}$)

Characteristics		Symbol	Test Condition	Unit
Power supply voltage		V_{DD}	−0.3~6.0 ($MV_{DD} \geqq V_{DD}$)	V
		MV_{DD}		
Input voltage	V_{DD} power supply pin	V_{IN1}	−0.3~V_{DD} + 0.3	V
	MV_{DD} power supply pin	V_{IN2}	−0.3~MV_{DD} + 0.3	
Power dissipation		P_D	1400	mW
Operating temperature		T_{opr}	−40~85	°C
Storage temperature		T_{stg}	−65~150	°C

Electrical Characteristics

(unless otherwise specified, Ta = 25°C, V_{DD} = MV_{DD} = XV_{DD} = DV_{DD} = AV_{DD} = 5 V, $2V_{REF}$ = $P2V_{REF}$ = 4.2 V, V_{REF} = PV_{REF} = 2.1 V)

V_{DD} (power supply pins for CD processor block: V_{DD}, XV_{DD}, DV_{DD}, and AV_{DD})

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage range	V_{DD}	—	MV_{DD} = XV_{DD} ≧ V_{DD} = DV_{DD} = AV_{DD} *	4.5	~	5.5	V
Operating power supply current	I_{DD}	—	(V_{DD}, DV_{DD}, AV_{DD}) operating at 16.9344 MHz	—	50	60	mA
	XI_{DD}	—	(XV_{DD}) 16.9344 MHz crystal oscillator connected	—	2.0	—	
Crystal oscillator standby current	X_{STBY}	—	(XV_{DD}) 16.9344 MHz crystal oscillator off	—	0.01	—	μA
Crystal oscillator frequency	f_{XT}	—	C_i = C_o = 15 pF (Note 1)*	—	16.9344	—	MHz

MV_{DD} (power supply pins for CPU block: MV_{DD}, XV_{DD}) (Note 2)

Characteristics	Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Operating power supply voltage range	MV_{DD1}	—	CPU and CD in operation MV_{DD} = XV_{DD} ≧ V_{DD} = DV_{DD} = AV_{DD} *		4.5	~	5.5	V
	MV_{DD2}		CPU in operation (CD off, 4.5 MHz/16.9344 MHz crystal oscillator used) *		4.5	~	5.5	
	MV_{DD3}		CPU in operation (CD off, 75 kHz crystal oscillator used) *		3.0	~	5.5	
Memory hold voltage range	MV_{HD}	—	Crystal oscillator stopped (executing CKSTP instruction) *		2.0	~	5.5	
Operating power supply current (Note 3)	MI_{DD1}	—	CPU in operation	XI = 16.9344 MHz crystal oscillator connected	—	3.0	5.0	mA
	MI_{DD2}	—		MXI = 4.5 MHz crystal oscillator connected	—	1.4	2.5	
	MI_{DD3}	—		MXI = 75 kHz crystal oscillator connected	—	0.3	1.0	
	MI_{DD4}	—	Standby mode (crystal oscillator only in operation)	XI = 16.9344 MHz crystal oscillator connected	—	1.5	—	
	MI_{DD5}	—		MXI = 4.5 MHz crystal oscillator connected	—	0.25	—	
	MI_{DD6}	—		MXI = 75 kHz crystal oscillator connected	—	0.1	—	
Memory hold current	MI_{HD}	—	Crystal oscillator stopped (executing CKSTP instruction)		—	0.1	1.0	μA
Crystal oscillator frequency	f_{MXT1}	—	4.5 MHz crystal oscillator set (Note 1)*		—	4.5	—	MHz
	f_{MXT2}	—	75 kHz crystal oscillator set, MV_{DD} = 2.7~5.5 V (Note 1)*		—	75	—	kHz
Crystal oscillator start time	t_{st}	—	Crystal oscillator f_{mxt} = 75 kHz		—	—	1.0	s

Note 1: Design and set constants according to the crystal oscillator to be connected.

Note 2: The power supply/memory hold current is the value obtained by summing the XV_{DD} and MV_{DD} pin currents.

Note 3: The values are those when the power supply detector function is operating. Setting the function reduces current dissipation by 150 μA (typ.). (Except in Standby mode)

An asterisk (*) indicates the values are guaranteed when V_{DD} = MV_{DD} = XV_{DD} = DV_{DD} = AV_{DD} and Ta = –40 to 85°C.
When CD is off, V_{DD} = DV_{DD} = AV_{DD} = 0 V

LCD common output/output port (COM1/OT1~COM4/OT4)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 4.5 V (LCD output)	−200	−600	—	μA
		I_{OH2}	—	V_{OH} = 4.5 V (OT output)	−15	−30	—	mA
	"L" level	I_{OL1}	—	V_{OL} = 0.5 V (LCD output)	200	600	—	μA
		I_{OL5}	—	V_{OL} = 0.5 V (OT output)	4.0	10	—	mA
Bias voltage	1/2 level	V_{BS2}	—	No load (LCD output, 1/2 bias method set)	2.3	2.5	2.7	V
	1/3 level	V_{BS1}	—	No load (LCD output, 1/3 bias method set)	1.47	1.67	1.87	
	2/3 level	V_{BS3}	—		3.13	3.33	3.53	

Segment output, output ports, I/O ports, and CD function output (S1/OT4~S9/OT13, S10/OT14/ZDET~S14/OT18/LRCK, P8-0/S14/BCK~P8-3/S18/IPF, OT19)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH1}	—	V_{OH} = 4.5 V (LCD output)	−200	−600	—	μA
		I_{OH4}	—	V_{OH} = 4.5 V (OT output, CD output, excluding P8-0~P8-3 pins)	−1.5	−4.0	—	mA
	"L" level	I_{OL1}	—	V_{OL} = 0.5 V (LCD output)	200	600	—	μA
		I_{OL5}	—	V_{OL} = 0.5 V (OT output, CD output)	4.0	10	—	mA
Input leakage current		I_{LI}	—	V_{IH} = 5.0 V, V_{IL} = 0 V (P8-0~P8-3)	—	—	±1.0	μA
Input voltage	"H" level	V_{IH}	—	(P8-0~P8-3, CLCK)	MV_{DD} × 0.8	~	MV_{DD}	V
	"L" level	V_{IL}	—	(P8-0~P8-3, CLCK)	0	~	MV_{DD} × 0.2	
Bias voltage	1/3 level	V_{BS1}	—	No load (LCD output, 1/3 bias method set)	1.47	1.67	1.87	V
	2/3 level	V_{BS3}	—		3.13	3.33	3.53	

I/O port (P1-0~P4-3)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH3}	—	V_{OH} = 4.5 V	−0.8	−2.0	—	mA
	"L" level	I_{OL3}	—	V_{OL} = 0.5 V (excluding P4-1, P4-2, P4-3 pins)	1.0	3.0	—	
		I_{OL5}	—	V_{OL} = 0.5 V (P4-1, P4-2, P4-3 pins)	4.0	10	—	
Input leakage current		I_{LI}	—	V_{IH} = 5.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH}	—	—	MV_{DD} × 0.8	~	MV_{DD}	V
	"L" level	V_{IL}	—	—	0	~	MV_{DD} × 0.2	
Input pull-up/down resistance		R_{IN1}	—	(P1-0~P1-3 pins) pull-down/up set	25	50	120	kΩ

$\overline{\text{HOLD}}$, INTR input port, $\overline{\text{RST}}$ input, 1-bit DAC data input (EMPHin/HSOin/LRCKin/DATAin/BCKin) Input port (IN1/IN2)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input leakage current		I_{LI}	—	V_{IH} = 5.0 V, V_{IL} = 0 V	—	—	±1.0	μA
Input voltage	"H" level	V_{IH}	—	—	MV_{DD} × 0.8	~	MV_{DD}	V
	"L" level	V_{IL}	—	—	0	~	MV_{DD} × 0.2	

AD converter (ADin1~ADin4)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog input voltage range	V_{AD}	—	ADin1~ADin4	0	~	MV_{DD}	V
Resolution	VRES	—	—	—	6	—	bit
Total conversion error	—	—	—	—	±0.5	±1.0	LSB
Analog input leakage	I_{LI}	—	V_{IH} = 5.0 V, V_{IL} = 0 V (ADin1~ADin4)	—	—	±1.0	μA

DOUT, SBSY, SBOK, SEL, OT19/$\overline{HSO}$, OT20/SPCK, OT21/SPDA, OT22/COFS output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH4}	—	V_{OH} = 4.5 V	−1.5	−4.0	—	mA
	"L" level	I_{OL4}	—	V_{OL} = 0.5 V	1.5	4.0	—	

PDO, TMAX, RFGC, TEBC, FMO, DMO, TRO, FOO output

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	"H" level	I_{OH6}	—	V_{OH} = 3.8 V, $P2V_{REF}$ = 4.2 V (PDO, TMAX)	—	−2.0	—	mA
	"L" level	I_{OL4}	—	V_{OL} = 0.5 V, $P2V_{REF}$ = 4.2 V (PDO, TMAX)	—	6.0	—	
Output resistance		R_{out3}	—	(RFGC, TEBC, FMO, DMO, TRO, FOO)	—	3.3	—	kΩ
V_{REF} output resistance		V_{oref}	—	(RFGC, TEBC, FMO, DMO, PDD) V_{REF} = PV_{REF} = 2.1 V	—	2.1	—	V

Transfer delay time (AOUT, SPDA, DATA, SBSY, SBOK)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Transfer delay time	"H" level	t_{pLH}	—	—	—	10	—	ns
	"L" level	t_{pHL}	—	—	—	10	—	

1-bit DA converter

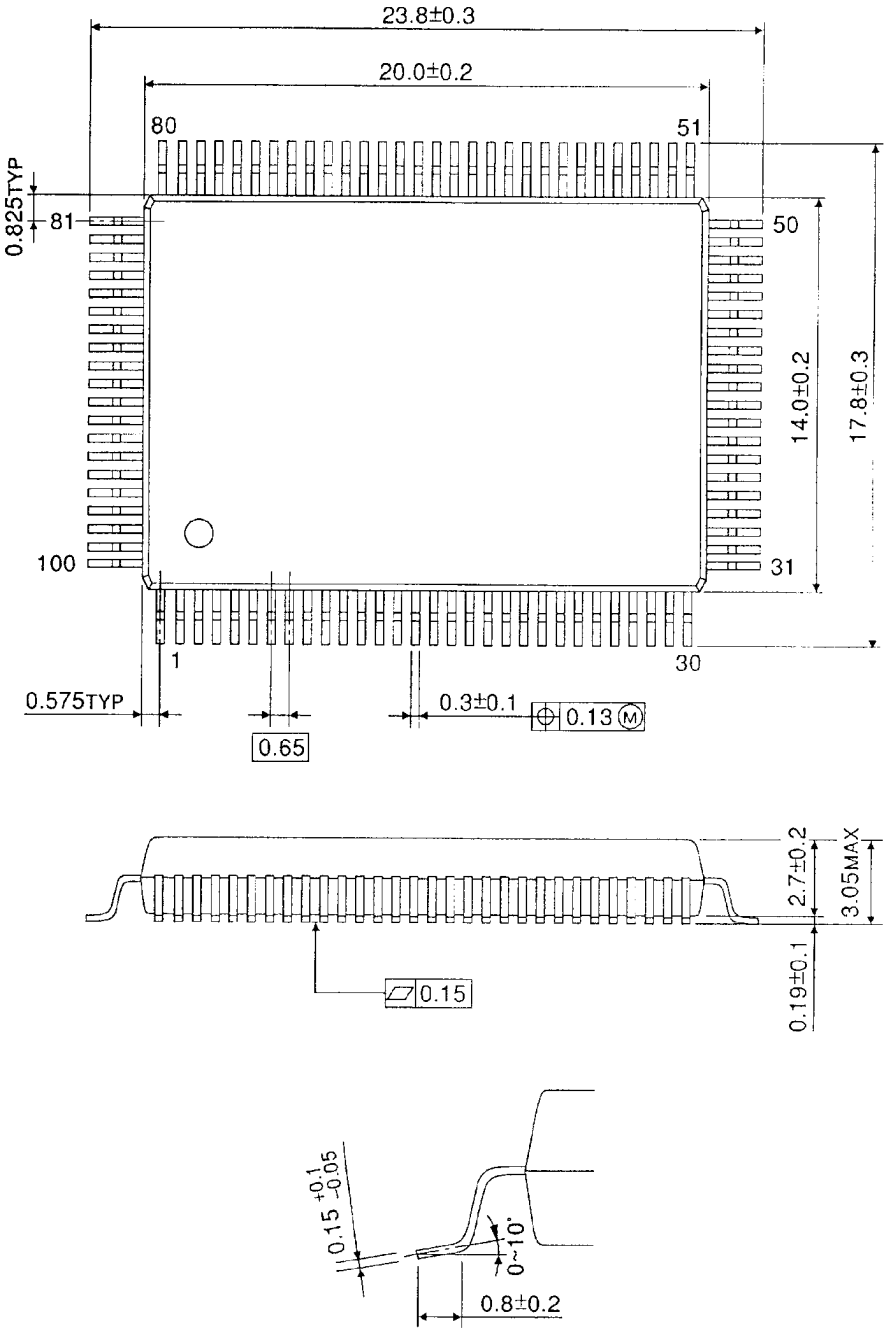
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Total harmony distortion	THD + N	—	1 kHz sine wave, full-scale input	—	−85	−78	dB
S/N ratio	S/N	—	—	90	98	—	
Dynamic range	DR	—	1 kHz sine wave, −60dB input conversion	85	90	—	
Crosstalk	CT	—	1 kHz sine wave, full-scale input	—	−90	−85	
Analog output level	DAC_{out}	—	1 kHz sine wave, full-scale input	1200	1250	1300	mVrms

Others

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input pull-down resistance	R_{IN2}	—	(TESTC, TESTM)	—	10	—	kΩ
XI amp feedback resistance	R_{fXT1}	—	(XI-XO)	1.0	2.0	4.0	MΩ
XO output resistance	R_{out1}	—	(XO)	—	0.5	—	kΩ
MXI amp feedback resistance	R_{fXT2}	—	When 4.5 MHz crystal set, (MXI-MXO)	0.5	1.0	2.5	MΩ
		—	When 75 kHz crystal set, (MXI-MXO)	—	10	—	
MXO output resistance	R_{out2}	—	(MXO)	—	2.0	—	kΩ
Input resistance	Z_{in1}	—	Set resistance by (RFI) CD command	—	10	—	kΩ
				—	5	—	
				—	2.5	—	
				—	1.25	—	
	Z_{in2}	—	(TEZI)	—	10	—	

Package Dimensions

QFP100-P-1420-0.65A Unit : mm



Weight: 1.6 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer’s own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.