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Continuity

There is no change to this datasheet as a result of offering the device as a Winbond product.

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APC.Support@winbond.com

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July 2003
Revision 1.2

National Semiconductor

PC87413, PC87414, PC87416, PC87417 LPC ServerI/O for Servers and Workstations

General Description

The National Semiconductor® PC8741x family of LPC ServerI/O devices ("**PC8741x**") comprises highly integrated Advanced I/O products. The PC8741x is targeted for a wide range of servers and workstations that use the Low Pin Count (LPC) bus for the host interface and the serial ACCESS.bus or SMBus® for the embedded controller interface.

The PC8741x features an X-Bus extension for read and write operations over the X-Bus for both LPC and ACCESS.bus cycles. Boot Flash and I/O devices can be accessed over this X-Bus.

Embedded controllers can access the PC8741x and its X-Bus via the ACCESS.bus or SMBus serial interface when V_{SB} exists, regardless of the LPC bus state. Some of the PC8741x logical devices can be disabled, or their pins can be floated, under control of the V_{SB}-powered serial bus.

The PC8741x provides a V_{SB}-powered high-frequency clock for on-chip peripherals and for other V_{SB}-powered platform components.

The PC8741x's extended wake-up support complements the chipset's ACPI controller and the platform embedded controllers. The PC8741x can monitor the Power and Sleep buttons and control the power supply of simple platforms that lack an embedded controller. The System Wake-Up Control (SWC) module is powered by V_{SB} and V_{BAT} power supplies. It supports flexible wake-up and power-off request mechanisms in any sleep state. It features Main and Standby power-on elapsed-time counters.

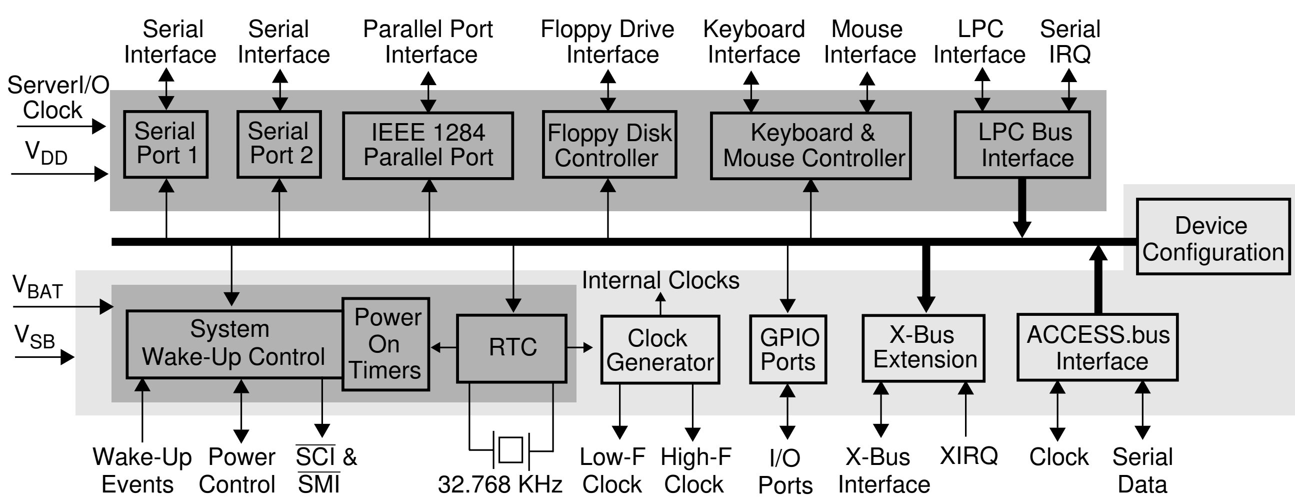
The PC8741x also incorporates a Floppy Disk Controller (FDC), two serial ports (UARTs), a Keyboard and Mouse Controller (KBC), a Real-Time Clock (RTC), a fully compliant IEEE 1284 Parallel Port, General-Purpose Input/Output (GPIO) for a total of 51 ports and an Interrupt Serializer for Parallel IRQs.

Outstanding Features

- LPC Interface, based on Intel's *LPC Interface Specification, Revision 1.0, September 29th, 1997*
- V_{SB}-powered access to modules through ACCESS.bus or SMBus (**PC87413 and PC87417**)
- X-Bus Extension for memory and I/O (**PC87416 and PC87417**)
- PC01 Revision 0.5 and ACPI Revision 1.0b compliant
- ServerI/O modules: Parallel Port, FDC, two Serial Ports (UARTs) and a Keyboard and Mouse Controller (KBC)
- Y2K-compliant RTC with 242 bytes of RAM
- 51 GPIO ports with a variety of wake-up events
- Extremely low current consumption in Battery Backup mode
- 128-pin PQFP package

Block Diagram

PC87417 (See page 5 for other PC8741x diagrams.)



Features

Bus Interfaces

- LPC Bus Interface
  - Based on Intel's *LPC Interface Specification Revision 1.0, September 29, 1997*
  - Synchronous cycles using up to 33 MHz bus clock
  - 8-bit I/O and Memory read and write cycles
  - Up to four 8-bit DMA channels
  - Serial IRQ
  - Supports bootable memory
  - Reset input
  - $\overline{\text{CLKRUN}}$ support
  - FWH Transaction support
- ACCESS.bus (ACB) Interface (**PC87413 and PC87417**)
  - Enables a system controller to access the internal functions and the X-Bus extension
  - Supports slave operation compatible with:
    - Intel SMBus
    - ACCESS.bus
  - Proprietary commands for read/write byte from/to:
    - Internal register
    - X-Bus I/O device
    - X-Bus memory device
  - Slave address:
    - Two values selected by strap
    - Programmable through the LPC bus
    - V_{BAT} backed-up
  - Concurrent access with the LPC bus
  - V_{SB} powered
  - Optional internal pull-up on the ACBDAT and ACBCLK pins
- X-Bus Extension (**PC87416 and PC87417**)
  - Supports I/O and Memory read/write operations
  - 8-bit data bus, 28-bit address
  - Multiplexed address-data lines:
    - Four direct address lines
    - Partial non-multiplexed option
  - Boot configuration selected by straps
  - Four chip-select outputs, each supporting multiple zones:
    - Up to 32 MByte BIOS memory zones
    - Up to 32 MByte user-defined memory zones
    - Four user-defined I/O zones
    - Test port and other I/O ports
  - Optional indirect addressing of memory
  - $\overline{\text{XRD}}$-XEN or $\overline{\text{XWR}}$-XR/$\overline{\text{W}}$ mode support
  - Supports both slow and fast devices
  - Accessible from both LPC and ACB buses
  - Programmable protection control over access from the LPC bus
  - V_{SB} powered
  - External Interrupt support via XIRQ pin
- Configuration Control (via LPC bus)
  - Compliant with *PC01 Specification Revision 0.5, November 2, 1999*
  - Plug and Play (PnP) Configuration register structure
  - Base Address strap to setup the address of the Index-Data register pair
  - Flexible resource allocation for all logical devices:
    - Relocatable base address
    - 15 IRQ routing options to serial IRQ
    - Up to four optional 8-bit DMA channels
  - ACCESS.bus control over pin multiplexing, module disable and output TRI-STATE for all Legacy modules (**PC87413 and PC87417**)

Legacy Modules

- Serial Ports 1 and 2
  - Software compatible with the 16550A and the 16450
  - Supports shadow register for write-only bit monitoring
  - UART data rates up to 1.5 Mbaud
- IEEE 1284-compliant Parallel Port
  - ECP, with Level 2 (14 mA sink and source output buffers)
  - Software or hardware control
  - Enhanced Parallel Port (EPP) compatible with EPP 1.7 and EPP 1.9
  - Supports EPP as mode 4 of the Extended Control Register (ECR)
  - Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - Supports a demand DMA mode mechanism and a DMA fairness mechanism for improved bus utilization
  - Protection circuit that prevents damage to the parallel port when a printer connected to it powers up or is operated at high voltages, even if the device is in power-down state
  - Optional outputs TRI-STATE by external pin
- Floppy Disk Controller (FDC)
  - Programmable write protect
  - Supports FM and MFM modes
  - Supports Enhanced mode command for three-mode Floppy Disk Drive (FDD)
  - Perpendicular recording drive support for 2.88 MB
  - Burst and Non-Burst modes
  - Full support for IBM Tape Drive Register (TDR) implementation of AT and PS/2 drive types
  - 16-byte FIFO
  - Error-free handling of data overrun and underrun conditions during DMA transactions (i.e., does not lose data or status bytes and is free of the NEC765A bug)
  - Software compatible with the PC8477, which contains a superset of the FDC functions in the µDP8473, NEC µPD765A/B and N82077
  - High-performance digital separator
  - Supports standard 5.25" and 3.5" FDDs
  - Supports up to four FDDs

Features (Continued)

- — Supports fast tape drives (2 Mbps) and standard tape drives (1 Mbps, 500 Kbps and 250 Kbps)
- ■ Keyboard and Mouse Controller (KBC)
  - — 8-bit microcontroller, software compatible with 8042AH and PC87911
  - — Standard interface (60h, 64h, IRQ1 and IRQ12)
  - — Supports two external swapable PS/2 interfaces for keyboard and mouse
  - — Five programmable, dedicated, open-drain I/O lines (Fast GA20/P21, $\overline{\text{KBRST}}$/P20, P12, P16, P17)

General-Purpose Modules

- ■ General-Purpose I/O (GPIO) Ports
  - — 51 GPIO Ports:
    - ❏ Individually assigned to either LPC or ACB control (**PC87413 and PC87417**)
    - ❏ 46 individually configured as input or output
    - ❏ Five output-only
  - — Programmable features for each output pin:
    - ❏ Drive type (open-drain, push-pull or TRI-STATE)
    - ❏ TRI-STATE on V_{DD}-fall detection for pins driving V_{DD}-supplied devices
  - — Programmable option for internal pull-up resistor on each input pin
  - — Lock option for the configuration and data of each output pin
  - — 16 GPIO ports generate IRQ/$\overline{\text{SIOSMI}}$/$\overline{\text{SIOSCI}}$ for wake-up events, with individual:
    - ❏ Enable control
    - ❏ Polarity and edge/level selection
    - ❏ Debounce mechanism
  - — V_{SB} powered
  - — Low-cost external GPIO port expansion via X-Bus (**PC87416 and PC87417**)
- ■ Real-Time Clock (RTC)
  - — DS1287, MC146818 and PC87911 compatible
  - — 242-byte battery backed-up CMOS RAM in two banks (accessed through 70-71h and 72-73h)
  - — Selective lock mechanisms for the RTC RAM
  - — Y2K-compliant calendar, including century and automatic leap-year adjustment
  - — Time of day in seconds, minutes and hours that allows a 12-hour or 24-hour format with optional adjustment for daylight saving time
  - — BCD or binary format for timekeeping
  - — Four individually maskable interrupt event flags:
    - ❏ Periodic rates from 122 µs to 500 ms
    - ❏ Day-of-month alarm
    - ❏ Time-of-day alarm
    - ❏ Once-per-second to once-per-day
  - — Double-buffer time registers

Power Management

- ■ Supports *ACPI Specification Revision 1.0b, Feb. 2, 1999*
- ■ System Wake-Up Control (SWC)
  - — Wake-up request on detection of:
    - ❏ Preprogrammed Keyboard or Mouse sequence
    - ❏ External modem ring from $\overline{\text{RI1}}$ or $\overline{\text{RI2}}$ on serial ports
    - ❏ Predetermined RTC date and time alarm
    - ❏ General-Purpose Input Events from up to 16 GPIO pins
    - ❏ IRQs of internal logical devices
  - — Optional routing of power-up request to SERIRQ, $\overline{\text{SIOSMI}}$, $\overline{\text{SIOSCI}}$, $\overline{\text{PWBTOUT}}$ and $\overline{\text{ONCTL}}$
  - — Routing control per input/output event combination
  - — Outputs enable/disable per event and system state combination (ACPI Sx states)
  - — Implements bank “b” of the ACPI registers
  - — Suspend modes via software emulation (control)
  - — Battery-backed event-logic configuration
  - — Power button support, featuring:
    - ❏ On/Off control
    - ❏ Power-off, 4-second override
    - ❏ Power button output
  - — Sleep Button support
- ■ Power Supply On/Off control
  - — Supports Legacy- and ACPI-compatible Power button
  - — Direct power supply control in response to wake-up events
  - — Programmable Crowbar time-out for On request
  - — On/Off control via software emulation
  - — Power-fail recovery
- ■ Enhanced Power Management (PM), including:
  - — Special configuration registers for power down
  - — Reduced current leakage from pins
  - — Low-power CMOS technology
  - — Ability to disable all modules
- ■ Keyboard Events
  - — Wake-up on any key
  - — Supports programmable 8-byte sequence “password” for Power Management
  - — Simultaneous recognition of three programmable keys (sequences): “Power”, “Sleep” and “Resume”
- ■ Power Active Timers
  - — Two power-on, elapsed-time counters for the main (V_{DD}) and standby (V_{SB}) power supplies
  - — 32-bit counters with 1 second LSB
  - — V_{BAT} backed-up counters

Features (Continued)

- Watchdog
  - — Watchdog counter reset by:
    - ❑ Serial Ports Interrupts
    - ❑ Keyboard and Mouse Interrupts
    - ❑ Software control
  - — 8-bit counter with 1 minute LSB
  - — Generates a 250 ms pulse at $\overline{\text{WDO}}$ pin
  - — Programmable $\overline{\text{SIOSMI}}$ or $\overline{\text{SIOSCI}}$ events

Clocking, Supply and Package Information

- Strap Input Controlled Operating Modes
  - — Base Address (BADDR) for the PnP Index-Data register pair
  - — Input clock presence (CKIN48) select
  - — X-Bus configuration (XCNF2-0) select (**PC87413 and PC87417**)
  - — ACCESS.bus slave address (ACBSA) select (**PC87416 and PC87417**)
  - — TRI-STATE device pins (TRIS)
- Clocks
  - — LPC clock input (up to 33 MHz)
  - — ServerI/O modules clock input: 48 MHz or no clock
  - — Single 32.768 KHz crystal
  - — On-chip low-frequency clock generator:
    - ❑ 32.768 KHz for RTC, System Wake-Up Control (SWC), Power Active timers and the high-frequency clock generator
    - ❑ Very low power consumption
    - ❑ V_{BAT} powered
  - — On-chip high-frequency clock generator:
    - ❑ Based on the 32.768 KHz clock
    - ❑ V_{SB} powered
  - — Clock outputs:
    - ❑ LFCKOUT: 32.768 KHz or 1 Hz
    - ❑ HFCKOUT: 48 MHz or 40 MHz (or divided)
- Protection
  - — All pins are 5V tolerant and back-drive protected (except the LPC bus pins)
  - — Separate battery pin that includes an internal UL protection resistor
  - — GPIO multiplexing configuration lock
- Power Supply
  - — 3.3V supply operation
  - — Separate pins for main (V_{DD}) and standby (V_{SB}) power supplies
  - — Backup battery input for RTC, SWC and Power Active timers
  - — Reduced standby power consumption
  - — Very low power consumption for RTC and timers (0.9 µA typical) from backup battery
- Package
  - — 128-pin PQFP

Device-Specific Information

The following table shows the main features for each device in the PC8741x family.

Function[1,2]	PC87413	PC87414	PC87416	PC87417
LPC Bus Interface	YES	YES	YES	YES
X-Bus Extension	NO	NO	YES	YES
ACCESS.bus Interface	YES	NO	NO	YES
General-Purpose Input/Output Ports (GPIO)	YES	YES	YES	YES
Real Time Clock (RTC)	YES	YES	YES	YES
System Wake-Up Control (SWC)	YES	YES	YES	YES
Legacy Functional Blocks	YES	YES	YES	YES

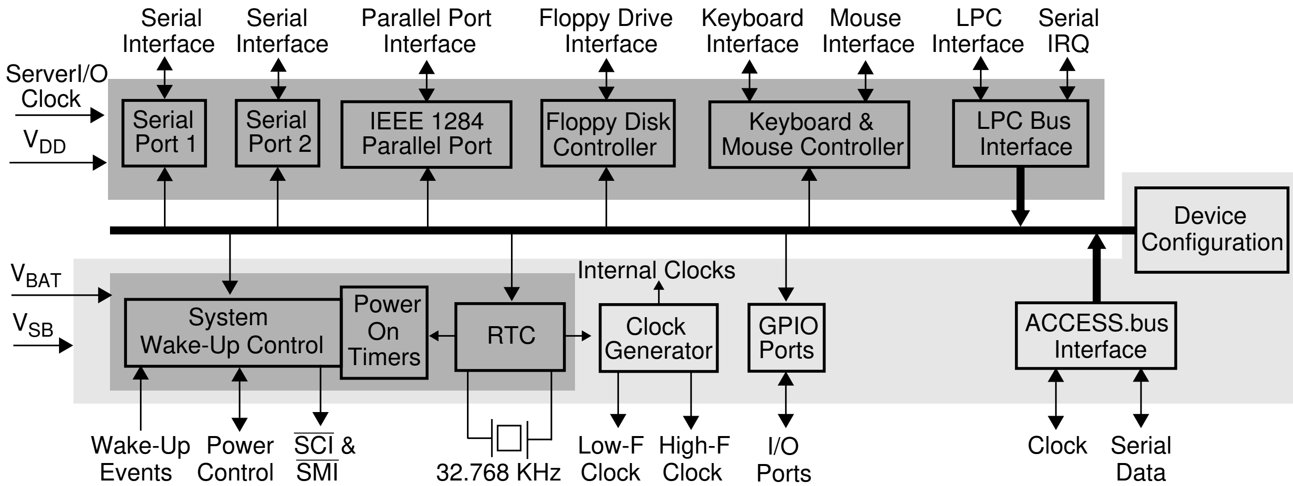
1. This Datasheet contains notes that are device specific.
2. The “not implemented” functions must not be accessed by the host/controller, because correct operation is not guaranteed.

Features (Continued)

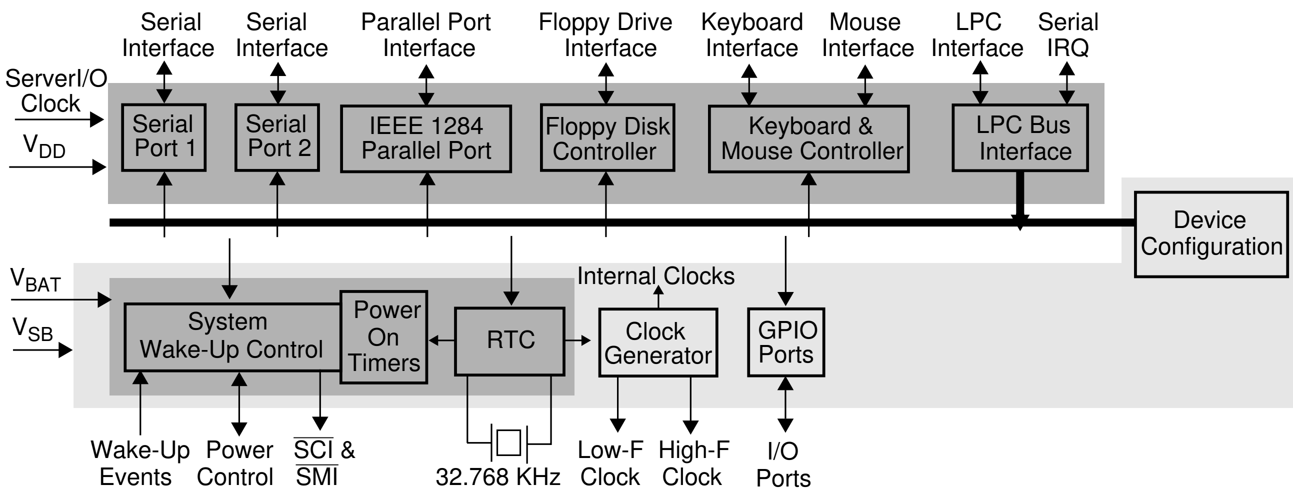
Block Diagrams

These are the block diagrams for the remaining PC8741x devices (see page 1 for the PC87417):

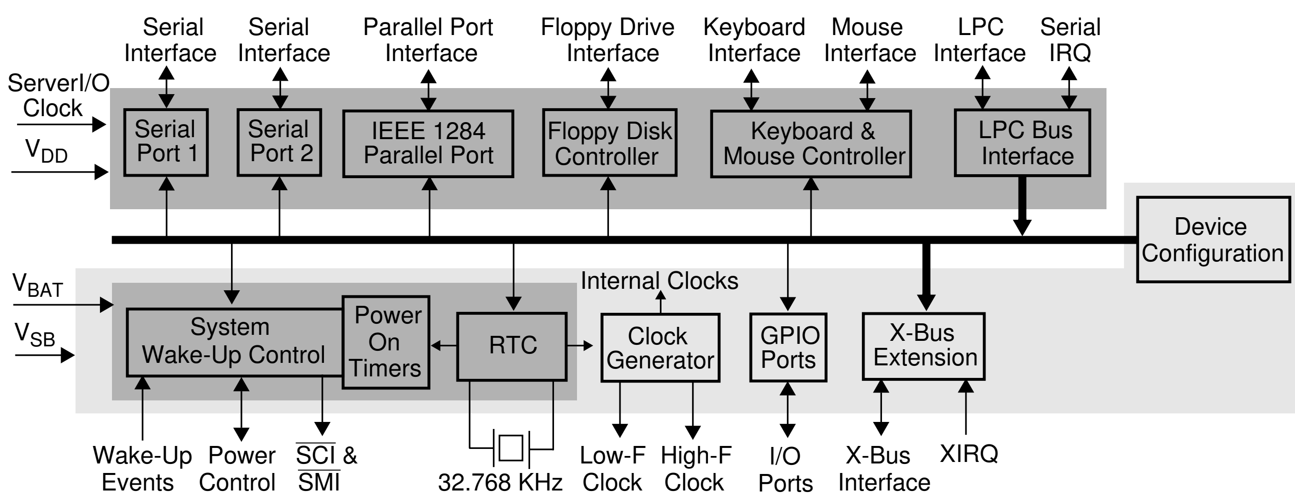
PC87413



PC87414



PC87416



Datasheet Revision Record

Revision Date	Status	Comments
July 2000	Preliminary Datasheet	First issue - Rev 0.12
October 2000	Preliminary Datasheet	Second issue - Rev 0.13
March 2001	Preliminary Datasheet	Third issue - Rev 1.0
November 2001	Preliminary Datasheet	Fourth issue - Rev 1.1
July 2003	Datasheet	Non-preliminary revision, Rev 1.2

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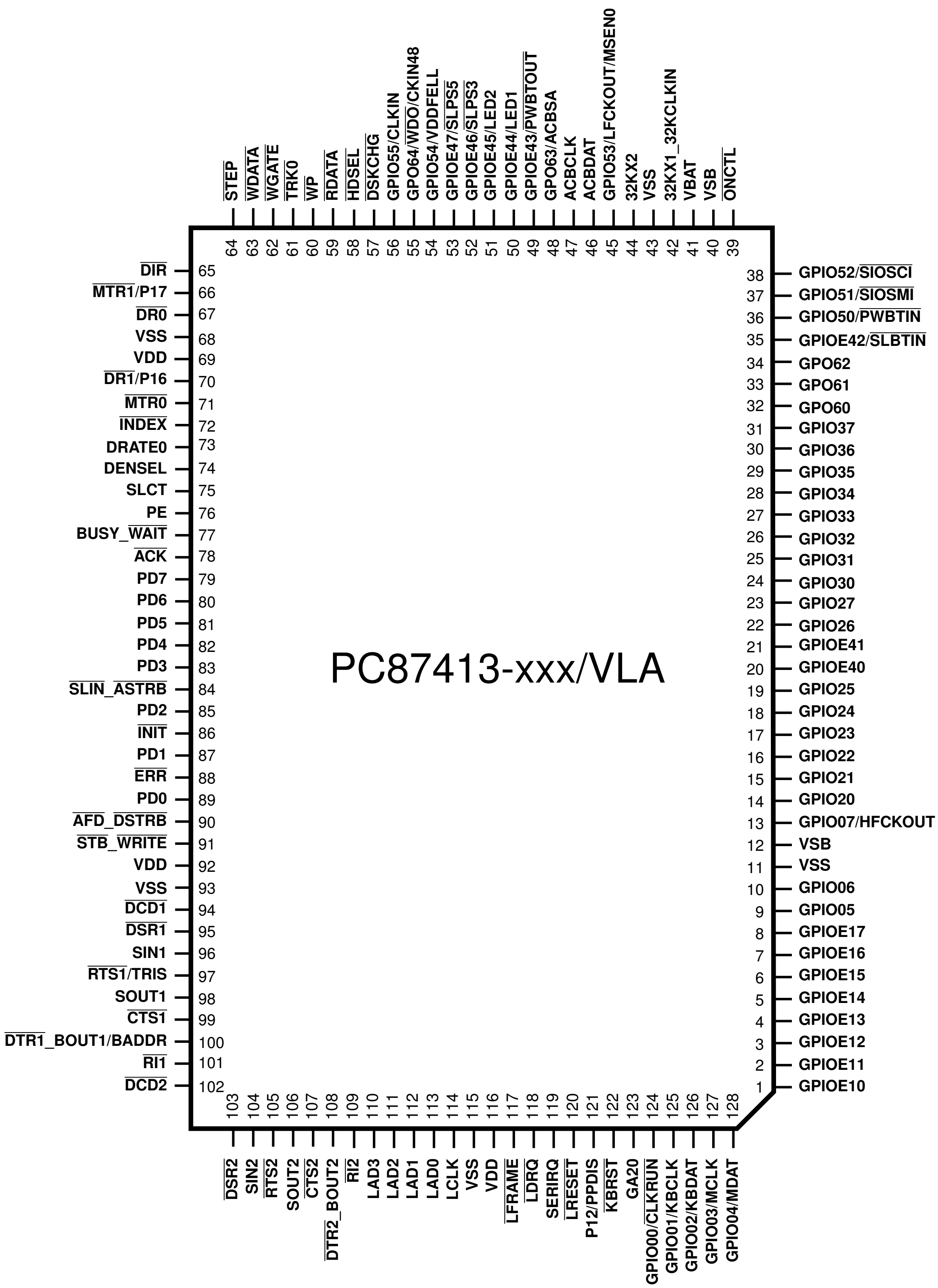
1.0 Signal/Pin Connection and Description

1.1 CONNECTION DIAGRAMS



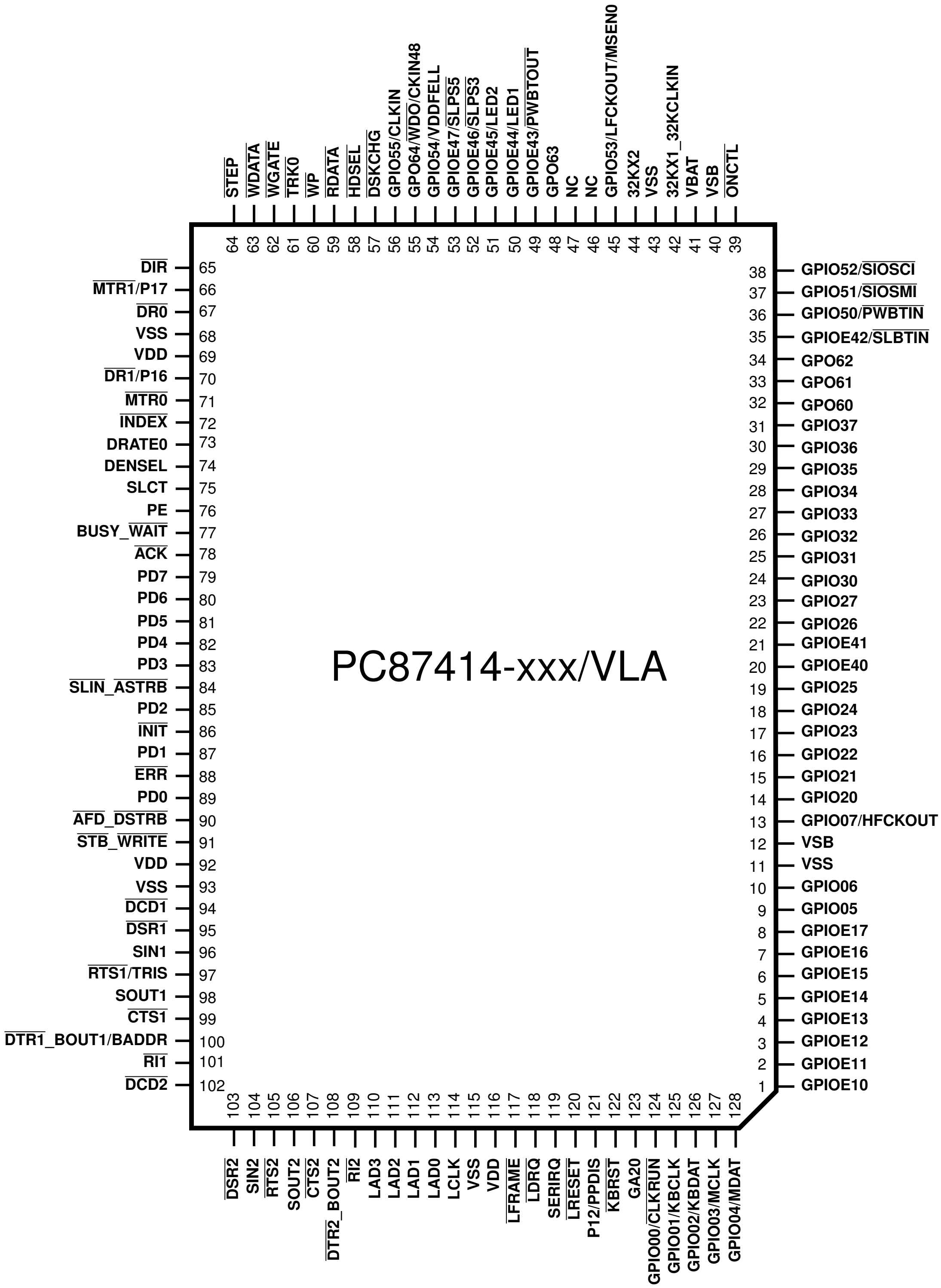
Plastic Quad Flatpack (PQFP), JEDEC

Order Number PC87413-xxx/VLA

See NS Package Number VLA128A

xxx = Three-character identifier for National data, keyboard ROM and/or customer identification code.

1.0 Signal/Pin Connection and Description (Continued)

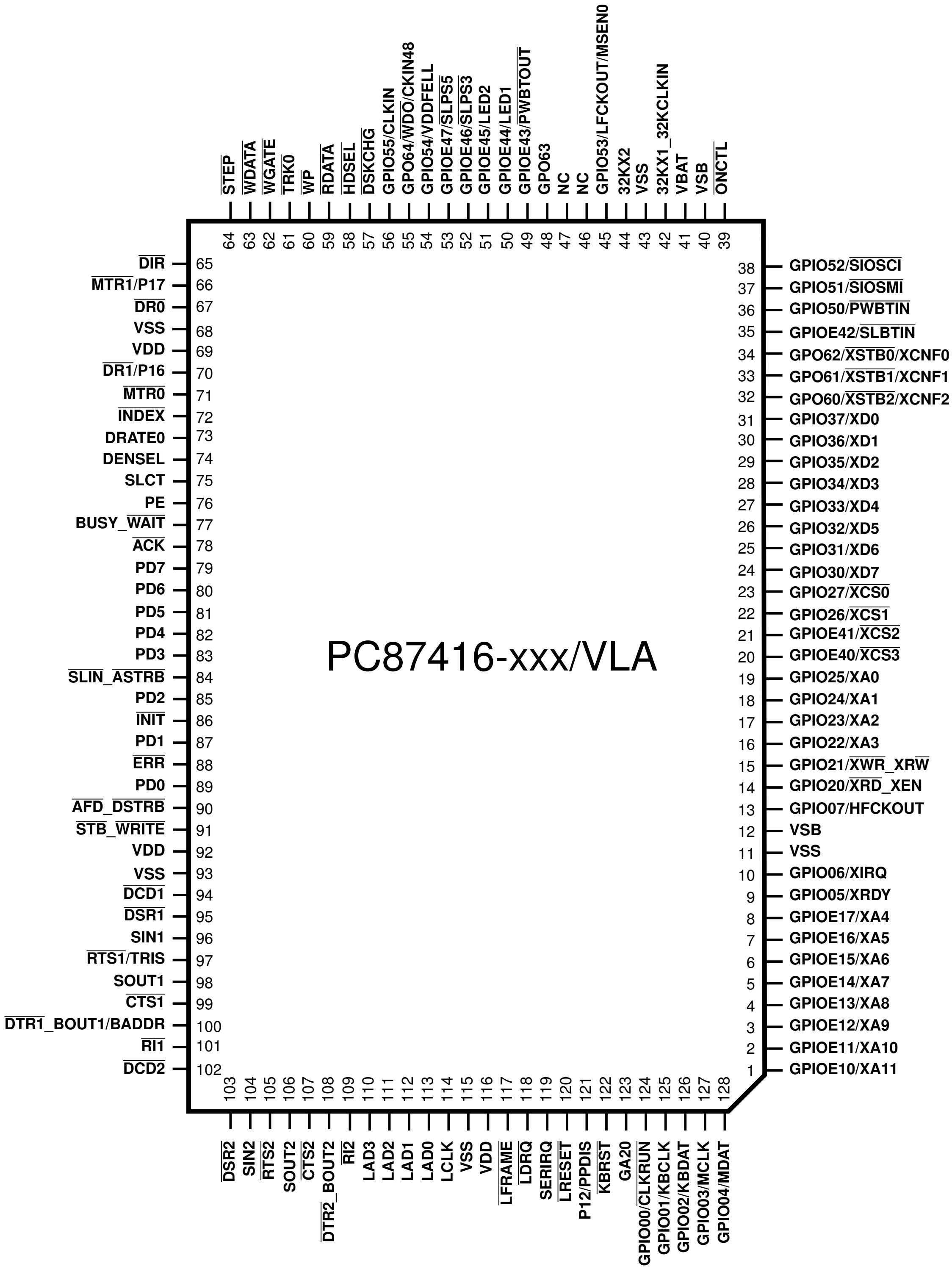


NC - Not Connected (these pins should be left unconnected)

Plastic Quad Flatpack (PQFP), JEDEC
Order Number PC87414-xxx/VLA
See NS Package Number VLA128A

xxx = Three-character identifier for National data, keyboard ROM and/or customer identification code.

1.0 Signal/Pin Connection and Description (Continued)

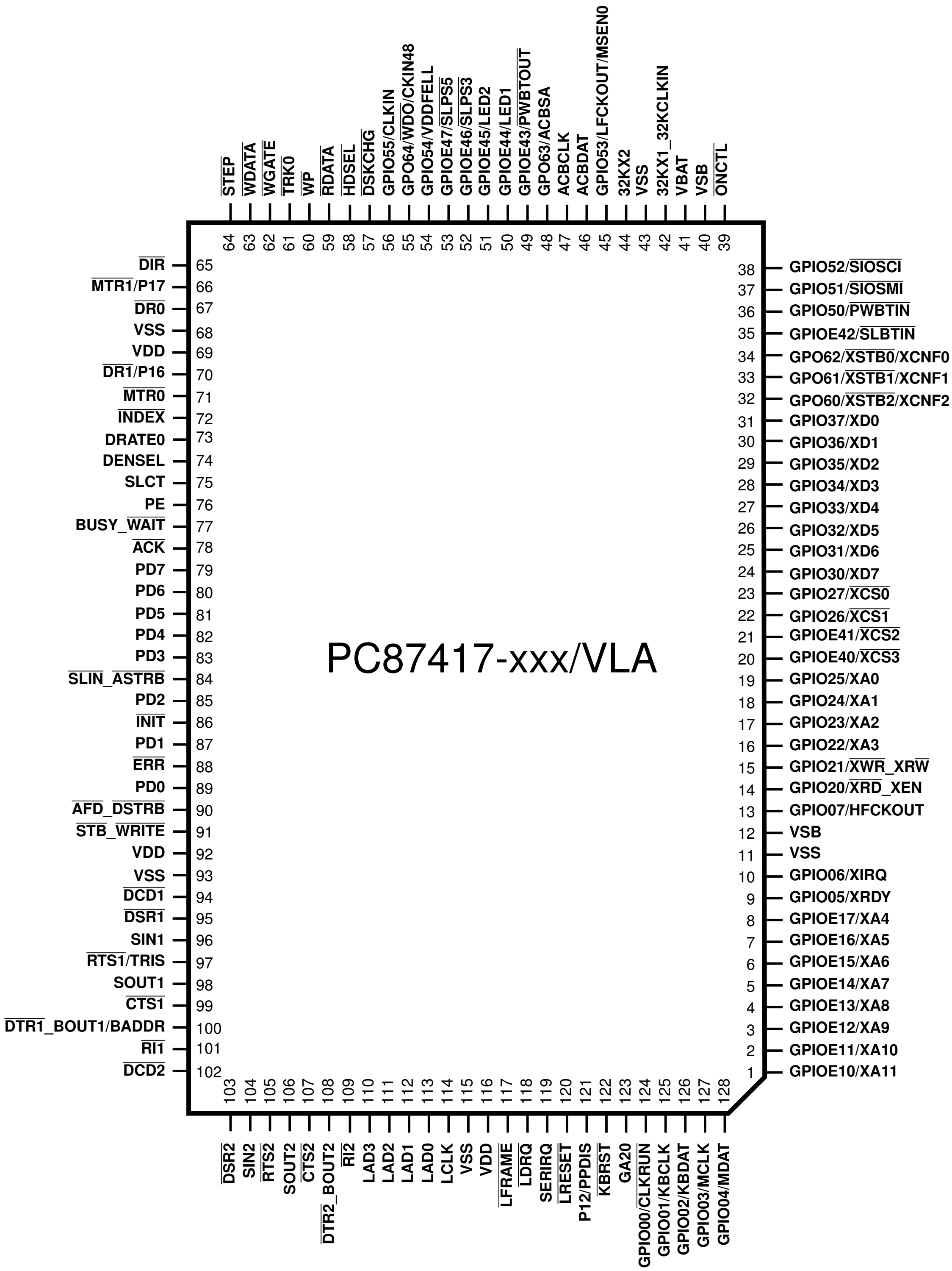


NC - Not Connected (these pins should be left unconnected)

Plastic Quad Flatpack (PQFP), JEDEC
Order Number PC87416-xxx/VLA
See NS Package Number VLA128A

xxx = Three-character identifier for National data, keyboard ROM and/or customer identification code.

1.0 Signal/Pin Connection and Description (Continued)



Plastic Quad Flatpack (PQFP), JEDEC
Order Number PC87417-xxx/VLA
See NS Package Number VLA128A

xxx = Three-character identifier for National data, keyboard ROM and/or customer identification code.

1.0 Signal/Pin Connection and Description (Continued)

1.2 BUFFER TYPES AND SIGNAL/PIN DIRECTORY

The signal DC characteristics of the pins described in Section 1.4 are denoted by buffer type symbols, which are defined in Table 1 and described in further detail in Section 11.2. The pin multiplexing information refers to two different types of multiplexing:

- Multiplexed, denoted by a slash (/) between pins in the diagrams in Section 1.1. Pins are shared between two different functions. Each function is associated with different board connectivity. Normally, the function selection is determined by the board design and cannot be changed dynamically. The multiplexing options must be configured by the BIOS upon power-up in order to comply with the board implementation.
- Multiple Mode, denoted by an underscore (_) between pins in the diagrams in Section 1.1. Pins have two or more modes of operation within the same function. These modes are associated with the same external (board) connectivity. Mode selection may be controlled by the device driver through the registers of the functional block and do not require a special BIOS setup upon power-up. These pins are not considered multiplexed pins from the ServerI/O configuration perspective. The mode selection method (registers and bits), as well as the signal specification in each mode, are described within the functional description of the relevant functional block.

Table 1. Buffer Types

Symbol	Description
IN_{CS}	Input, CMOS compatible, with Schmitt Trigger
IN_{OSC}	Input, from crystal oscillator (not characterized)
IN_{PCI}	Input, PCI 3.3V
IN_{SM}	Input, ACCESS.bus and SMBus compatible
IN_T	Input, TTL compatible
IN_{TS}	Input, TTL compatible, with Schmitt Trigger
IN_{ULR}	Input, power, resistor protected (not characterized)
$O_{p/n}$	Output, push-pull output buffer capable of sourcing *p* mA and sinking *n* mA
OD_n	Output, open-drain output buffer capable of sinking *n* mA
O_{OSC}	Output, to crystal oscillator (not characterized)
O_{PCI}	Output, PCI 3.3V
PWR	Power pin
GND	Ground pin

1.3 PIN MULTIPLEXING

The table below shows only multiplexed pins, their associated functional blocks and the configuration bits for the selection of the multiplexed options used in the PC8741x. **Some PC8741x devices implement a subset of these signals.** Refer to *Device-Specific Information* on page 4 to identify the functions relevant to a specific device.

1.0 Signal/Pin Connection and Description (Continued)

Table 2. Pin Multiplexing Configuration

Pin	Functional Block	Signal	Functional Block	Signal	Functional Block	Strap/Wake-up	Configuration Select
1	GPIO	GPIOE10	X-Bus	XA11	SWC	GPIOE10	SIOCF4.NOADDIR
2		GPIOE11		XA10		GPIOE11	
3		GPIOE12		XA9		GPIOE12	
4		GPIOE13		XA8		GPIOE13	
5		GPIOE14		XA7		GPIOE14	
6		GPIOE15		XA6		GPIOE15	
7		GPIOE16		XA5		GPIOE16	
8		GPIOE17		XA4		GPIOE17	
9		GPIO05		XRDY			SIOCF4.XRDYMUX
10		GPIO06		XIRQ			SIOCF5.XIRQMUX
13		GPIO07	CLKGEN	HFCKOUT			SIOCF4.HFCKMUX
14		GPIO20	X-Bus	$\overline{\text{XRD}}$_XEN			SIOCF4.NOXBUS
15		GPIO21		$\overline{\text{XWR}}$_XR$\overline{\text{W}}$			
16		GPIO22		XA3			
17		GPIO23		XA2			
18		GPIO24		XA1			
19		GPIO25		XA0			
22		GPIO26		$\overline{\text{XCS1}}$			SIOCF5.XCS1MUX
23		GPIO27		$\overline{\text{XCS0}}$			SIOCF5.XCS0MUX
20		GPIOE40		$\overline{\text{XCS3}}$	SWC	GPIOE40	SIOCF5.XCS3MUX
21		GPIOE41		$\overline{\text{XCS2}}$		GPIOE41	SIOCF5.XCS2MUX
24		GPIO30		XD7			SIOCF4.NOXBUS
25		GPIO31		XD6			
26		GPIO32		XD5			
27		GPIO33		XD4			
28		GPIO34		XD3			
29		GPIO35		XD2			
30		GPIO36		XD1			
31		GPIO37		XD0			
32		GPO60		$\overline{\text{XSTB2}}$	Straps	XCNF2	SIOCF5.XSTB2MUX
33		GPO61		$\overline{\text{XSTB1}}$		XCNF1	SIOCF5.XSTB1MUX
34		GPO62		$\overline{\text{XSTB0}}$		XCNF0	SIOCF5.XSTB0MUX

1.0 Signal/Pin Connection and Description (Continued)

Table 2. Pin Multiplexing Configuration (Continued)

Pin	Functional Block	Signal	Functional Block	Signal	Functional Block	Strap/Wake-up	Configuration Select
35	GPIO	GPIOE42	SWC	$\overline{\text{SLBTIN}}$	SWC	GPIOE42	SIOCF3.SLBTIMUX
36		GPIO50		$\overline{\text{PWBTIN}}$			SIOCF3.PWBTIMUX
37		GPIO51		$\overline{\text{SIOSMI}}$			SIOCF3.SMIMUX
38		GPIO52		$\overline{\text{SIOSCI}}$			SIOCF3.SCIMUX
45		GPIO53	CLKGEN	LFCKOUT			SIOCF4.LFCKMUX
			FDC	MSEN0			
48		GPO63			Straps	ACBSA	
49		GPIOE43	SWC	$\overline{\text{PWBTOUT}}$	SWC	GPIOE43	SIOCF3.PWBTOMUX
50		GPIOE44		LED1		GPIOE44	SIOCF3.LED1MUX
51		GPIOE45		LED2		GPIOE45	SIOCF3.LED2MUX
52		GPIOE46		$\overline{\text{SLPS3}}$		GPIOE46	SIOCF3.EXTSTMUX
53		GPIOE47		$\overline{\text{SLPS5}}$		GPIOE47	SIOCF3.EXTSTMUX
54		GPIO54		VDDFELL			SIOCF2.VDDFLMUX
55		GPO64		$\overline{\text{WDO}}$	Straps	CKIN48	SIOCF2.WDOMUX
56		GPIO55	CLKGEN	CLKIN			CLOCKCF.CKIN48
66	FDC	$\overline{\text{MTR1}}$	KBC	P17			SIOCF2.P17MUX
70		$\overline{\text{DR1}}$		P16			SIOCF2.P16MUX
97	Serial Port 1	$\overline{\text{RTS1}}$			Straps	TRIS	
100		$\overline{\text{DTR1}}$_BOUT1				BADDR	
101		$\overline{\text{RI1}}$			SWC	$\overline{\text{RI1}}$	
109	Serial Port 2	$\overline{\text{RI2}}$				$\overline{\text{RI2}}$	
121	Parallel Port	PPDIS	KBC	P12			SIOCF2.P12MUX
124	GPIO	GPIO00	LPC I/F	$\overline{\text{CLKRUN}}$			SIOCF2.CLKRNMUX
125		GPIO01	KBC	KBCLK	SWC	KBCLK	SIOCF2.NOKBC
126		GPIO02		KBDAT		KBDAT	
127		GPIO03		MCLK		MCLK	
128		GPIO04		MDAT		MDAT	

1.4 DETAILED SIGNAL/PIN DESCRIPTIONS

This section describes all the signals of the PC8741x devices. **Some PC8741x devices implement a subset of these signals.** Refer to *Device-Specific Information* on page 4 to identify the functions relevant to a specific device. Device signals are organized by functional group.

1.0 Signal/Pin Connection and Description (Continued)

1.4.1 LPC Interface

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
LAD3-0[1]	110-113	I/O	IN_{PCI}/O_{PCI}	V_{DD}	**LPC Address-Data.** Multiplexed command, address bidirectional data and cycle status.
LCLK[1]	114	I	IN_{PCI}	V_{DD}	**LPC Clock.** Derived from the PCI clock (up to 33 MHz).
$\overline{\text{LFRAME}}$[1]	117	I	IN_{PCI}	V_{DD}	**LPC Frame.** Low pulse indicates the beginning of a new LPC cycle or termination of a broken cycle.
$\overline{\text{LDRQ}}$[1]	118	O	O_{PCI}	V_{DD}	**LPC DMA Request.** Encoded DMA request for LPC Interface.
$\overline{\text{LRESET}}$[1]	120	I	IN_{PCI}	V_{DD}	**LPC Reset.** Derived from the PCI system reset.
SERIRQ[1]	119	I/O	IN_{PCI}/O_{PCI}	V_{DD}	**Serial IRQ.** The interrupt requests are serialized over a single pin, where each IRQ level is delivered during a designated time slot.
$\overline{\text{CLKRUN}}$[1]	124	I/OD	IN_{PCI}/OD_6	V_{DD}	**Clock Run.** Indicates that LCLK is going to be stopped and requests full-speed LCLK (same behavior as PCI $\overline{\text{CLKRUN}}$).

1. This pin is neither 5-Volt tolerant, nor back-drive protected.

1.4.2 ACCESS.bus (ACB) Interface (PC87413 and PC87417)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
ACBCLK	47	I/O	IN_{SM}/OD_6	V_{SB}	**ACCESS.bus Clock.** An internal pull-up for this pin is optional.
ACBDAT	46	I/O	IN_{SM}/OD_6	V_{SB}	**ACCESS.bus Serial Data.** An internal pull-up for this pin is optional.

1.4.3 X-Bus Extension (PC87416 and PC87417)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{\text{XRD}}$_XEN	14	O	$O_{3/6}$	V_{SB}	**Read.** Active (low) level indicates read cycle on the X-Bus. **Enable.** Active (high) level indicates valid data on the X-Bus.
XWR_XR$\overline{\text{W}}$	15	O	$O_{3/6}$	V_{SB}	**Write.** Active (low) level indicates a write cycle on the X-Bus. **Read/Write.** A high level indicates a read cycle on the X-Bus; a low level indicates a write cycle on the X-Bus.
XD7-0	24-31	I/O	$IN_{TS}/O_{3/6}$	V_{SB}	**Data Bus.** 8-bit data multiplexed with the address lines XA27-4.
XA11-4, XA3-0	1-8 16-19	O	$O_{3/6}$	V_{SB}	**Address Bus.** The XA27-12 address lines are always multiplexed with the data lines.
$\overline{\text{XSTB}}$2-0	32-34	O	$O_{3/6}$	V_{SB}	**Address Strobes.** Control the strobe of up to three external latches for the multiplexed address lines.
$\overline{\text{XCS}}$3-0	20-23	O	$O_{3/6}$	V_{SB}	**Chip Selects.** Control the selection of up to four devices residing on the X-Bus.
XRDY	9	I	IN_{TS}	V_{SB}	**I/O Ready.** Instructs the PC8741x to extend the access cycle.
XIRQ	10	I	IN_{TS}	V_{SB}	**X-Bus Interrupt.** Converted into serial interrupt by the Interrupt Serializer. The system configuration includes the interrupt number associated with this signal.

1.0 Signal/Pin Connection and Description (Continued)

1.4.4 Serial Port 1 and Serial Port 2 (UART1 and UART2)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{CTS1}$ $\overline{CTS2}$	99 107	I	IN_{TS}	V_{DD}	**Clear to Send.** When low, indicates that the modem or other data transfer device is ready to exchange data.
$\overline{DCD1}$ $\overline{DCD2}$	94 102	I	IN_{TS}	V_{DD}	**Data Carrier Detected.** When low, indicates that the modem or other data transfer device has detected the data carrier.
$\overline{DSR1}$ $\overline{DSR2}$	95 103	I	IN_{TS}	V_{DD}	**Data Set Ready.** When low, indicates that the data transfer device, e.g., modem, is ready to establish a communications link.
$\overline{DTR1}$_BOUT1 $\overline{DTR2}$_BOUT2	100 108	O	$O_{3/6}$	V_{DD}	**Data Terminal Ready.** When low, indicates to the modem or other data transfer device that the UART is ready to establish a communications link. After a system reset, these pins provide the $\overline{DTR}$ function and set these signals to inactive high. Loopback operation holds them inactive. **Baud Output.** Provides the associated serial channel baud rate generator output signal if Test mode is selected, i.e., bit 7 of the EXCR1 register is set.
$\overline{RI1}$ $\overline{RI2}$	101 109	I	IN_{TS}	V_{DD}	**Ring Indicator.** When low, indicates that a telephone ring signal has been received by the modem. These pins are monitored during V_{DD} power-off for wake-up event detection.
$\overline{RTS1}$ $\overline{RTS2}$	97 105	O	$O_{3/6}$	V_{DD}	**Request to Send.** When low, indicates to the modem or other data transfer device that the corresponding UART is ready to exchange data. A system reset sets these signals to inactive high, and loopback operation holds them inactive.
SIN1 SIN2	96 104	I	IN_{TS}	V_{DD}	**Serial Input.** Receives composite serial data from the communications link (peripheral device, modem or other data transfer device).
SOUT1 SOUT2	98 106	O	$O_{3/6}$	V_{DD}	**Serial Output.** Sends composite serial data to the communications link (peripheral device, modem or other data transfer device). These signals are set active high after a system reset.

1.0 Signal/Pin Connection and Description (Continued)

1.4.5 Parallel Port

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
ACK	78	I	IN_T	V_{DD}	**Acknowledge.** Pulsed low by the printer to indicate that it has received data from the parallel port.
AFD_DSTRB	90	O	OD_{14}, $O_{14/14}$	V_{DD}	**AFD - Automatic Feed.** When low, instructs the printer to automatically feed a line after printing each line. This pin is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **DSTRB - Data Strobe (EPP).** Active low, used in EPP mode to denote a data cycle. When the cycle is aborted, DSTRB becomes inactive (high).
BUSY_WAIT	77	I	IN_T	V_{DD}	**Busy.** Set high by the printer when it cannot accept another character. **Wait.** In EPP mode, the parallel port device uses this active low signal to extend its access cycle.
ERR	88	I	IN_T	V_{DD}	**Error.** Set active low by the printer when it detects an error.
INIT	86	O	OD_{14}, $O_{14/14}$	V_{DD}	**Initialize.** When low, initializes the printer. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin.
PD7-3 PD2 PD1 PD0	79-83 85 87 89	I/O	$IN_T/O_{14/14}$	V_{DD}	**Parallel Port Data.** Transfers data to and from the peripheral data bus and the appropriate parallel port data register. These signals have a high current drive capability.
PE	76	I	IN_T	V_{DD}	**Paper End.** Set high by the printer when it is out of paper. This pin has an internal weak pull-up or pull-down resistor.
SLCT	75	I	IN_T	V_{DD}	**Select.** Set active high by the printer when the printer is selected.
SLIN_ASTRB	84	O	OD_{14}, $O_{14/14}$	V_{DD}	**SLIN - Select Input.** When low, selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **ASTRB - Address Strobe (EPP).** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, ASTRB becomes inactive (high).
STB_WRITE	91	O	OD_{14}, $O_{14/14}$	V_{DD}	**STB - Data Strobe.** When low, Indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor must be connected to this pin. **WRITE - Write Strobe.** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, WRITE becomes inactive (high).
PPDIS	121	I	IN_T	V_{DD}	**Parallel Port Disable.** When high, this input disables (TRI-STATEs) all the output signals of the parallel port.[1]

1. If this feature is not used, either select the alternate function (P12 port) at the pin multiplexer (see Section 3.7.3 on page 50) or connect an external 3.3 KΩ pull-down resistor to this pin. If the function connected to the pin is PPDIS and the pin is left unconnected, the output signals of the parallel port will float.

1.0 Signal/Pin Connection and Description (Continued)

1.4.6 Floppy Disk Controller (FDC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
DENSEL	74	O	$O_{2/12}$	V_{DD}	**Density Select.** Indicates that a high FDC density data rate (500 Kbps, 1 Mbps or 2 Mbps) or a low density data rate (250 or 300 Kbps) is selected.
$\overline{\text{DIR}}$	65	O	OD_{12}, $O_{2/12}$	V_{DD}	**Direction.** Determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in; inactive = step out) during a seek operation.
$\overline{\text{DR1}}$ $\overline{\text{DR0}}$	70 67	O	OD_{12}, $O_{2/12}$	V_{DD}	**Drive Select.** Decoded output signals in Two-Drive mode or encoded signals in Four-Drive mode. Controlled by bits 1 and 0 of the Digital Output Register (DOR).
DRATE0	73	O	$O_{3/6}$	V_{DD}	**Data Rate.** Reflects the value of bit 0 of the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last.
$\overline{\text{DSKCHG}}$	57	I	IN_T	V_{DD}	**Disk Change.** Indicates if the drive door has been opened.
$\overline{\text{HDSEL}}$	58	O	OD_{12}, $O_{2/12}$	V_{DD}	**Head Select.** Determines which side of the FDD is accessed. Active low selects side 1; inactive selects side 0.
$\overline{\text{INDEX}}$	72	I	IN_T	V_{DD}	**Index.** Indicates the beginning of an FDD track.
MSEN0	45	I	IN_T	V_{DD}	**Automatic Media Sense.** Identifies the media type of the floppy disk in drives 1 and 0 (if the drives support this protocol).
$\overline{\text{MTR1}}$ $\overline{\text{MTR0}}$	66 71	O	OD_{12}, $O_{2/12}$	V_{DD}	**Motor Select.** Active low, motor enable lines for drives 1 and 0, controlled by bits D7-4 of the Digital Output Register (DOR). MTR0 is used to decode DR1 and DR0 in Four-Drive mode.
$\overline{\text{RDATA}}$	59	I	IN_T	V_{DD}	**Read Data.** Raw serial input data stream read from the FDD.
$\overline{\text{STEP}}$	64	O	OD_{12}, $O_{2/12}$	V_{DD}	**Step.** Issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
$\overline{\text{TRK0}}$	61	I	IN_T	V_{DD}	**Track 0.** Indicates to the controller that the head of the selected floppy disk drive is at track 0.
$\overline{\text{WDATA}}$	63	O	OD_{12}, $O_{2/12}$	V_{DD}	**Write Data**. Carries out the pre-compensated serial data that is written to the FDD. Pre-compensation is software selectable.
$\overline{\text{WGATE}}$	62	O	OD_{12}, $O_{2/12}$	V_{DD}	**Write Gate.** Enables the write circuitry of the selected FDD. WGATE is designed to prevent glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
$\overline{\text{WP}}$	60	I	IN_T	V_{DD}	**Write Protected.** Indicates that the disk in the selected drive is write protected.

1.0 Signal/Pin Connection and Description (Continued)

1.4.7 Keyboard and Mouse Controller (KBC)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
KBCLK	125	I/O	IN_{TS}/OD_{14}	V_{DD}	**Keyboard Clock.** Keyboard clock signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD} power-off for wake-up event detection.
KBDAT	126	I/O	IN_{TS}/OD_{14}	V_{DD}	**Keyboard Data.** Keyboard data signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD} power-off for wake-up event detection.
MCLK	127	I/O	IN_{TS}/OD_{14}	V_{DD}	**Mouse Clock.** Mouse clock signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD} power-off for wake-up event detection.
MDAT	128	I/O	IN_{TS}/OD_{14}	V_{DD}	**Mouse Data.** Mouse data signal. External pull-up resistor is required for PS/2 compliance. This pin is monitored during V_{DD} power-off for wake-up event detection.
KBRST	122	I/O	IN_T/OD_2	V_{DD}	**KBD Reset.** Keyboard reset (P20) open-drain output.
GA20	123	I/O	IN_T/OD_2	V_{DD}	**Gate A20.** KBC gate A20 (P21) open-drain output.
P12, P16, P17	121, 70, 66	I/O	IN_T/OD_2, $O_{2/2}$	V_{DD}	**I/O Port.** KBC quasi-bidirectional signal for general-purpose input and output (controlled by KBC firmware).

1.4.8 General-Purpose I/O (GPIO)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
GPIO01-04	125-128	I/O	IN_{TS}/ OD_{14}, $O_{3/14}$	V_{SB}	**General-Purpose I/O Ports.** Each pin is configured independently as input or I/O with or without static pull-up and with either open-drain or push-pull output type. The GPIOE*nn* pins have event detection capability.
GPIOE44, 45	50, 51	I/O	IN_{TS}/ OD_{12}, $O_{12/12}$	V_{SB}	
GPIO07	13	I/O	IN_{TS}/ OD_4, $O_{2/4}$	V_{SB}	
GPIO53	45	I/O	IN_{TS}/ OD_2, $O_{1/2}$	V_{SB}	
GPIO00, GPIO05-06, GPIOE10-17, GPIO20-25, GPIO26-27, GPIO30-37, GPIOE40-41, GPIOE42, 43, GPIOE46, 47, GPIO50-52, GPIO54, 55	124 9-10 1-8 14-19 22-23 24-31 2-21 35, 49 52, 53 36-38 54, 56	I/O	IN_{TS}/ OD_6, $O_{3/6}$	V_{SB}	
GPO60-62, 63, 64	32-34, 48, 55	O	OD_6, $O_{3/6}$	V_{SB}	**General-Purpose Output Ports.** Each pin is configured independently for either open-drain or push-pull output type.

1.0 Signal/Pin Connection and Description (Continued)

1.4.9 System Wake-Up Control (SWC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
GPIOE10-17, GPIOE40-41, GPIOE42, GPIOE43-47,	1-8 2-21 35 49-53	I	IN_{TS}	V_{SB}	**Wake-up Inputs.** Generate a wake-up event or an interrupt. These pins have programmable debounce protection.
$\overline{\text{RI1}}$ $\overline{\text{RI2}}$	101 109	I	IN_{TS}	V_{SB}	**Ring Indicator Wake-up.** When low, generates a wake-up event or an interrupt, indicating that a telephone ring signal was received by the modem.
KBCLK	125	I/O	IN_{TS}/OD_{14}	V_{SB}	**Keyboard Clock Wake-up.** Generates a wake-up event or an interrupt, indicating a change in the keyboard clock signal.
KBDAT	126	I/O	IN_{TS}/OD_{14}	V_{SB}	**Keyboard Data Wake-up.** Generates a wake-up event or an interrupt, indicating a change in the keyboard data signal.
MCLK	127	I/O	IN_{TS}/OD_{14}	V_{SB}	**Mouse Clock Wake-up.** Generates a wake-up event or an interrupt, indicating a change in the mouse clock signal.
MDAT	128	I/O	IN_{TS}/OD_{14}	V_{SB}	**Mouse Data Wake-up.** Generates a wake-up event or an interrupt, indicating a change in the mouse data signal.
PWBTIN	36	I	IN_{TS}	V_{SB}	**Power Button In.** Active (low) level indicates a user request to turn the power on or off. This pin has debounce protection.
PWBTOUT	49	O	OD_6	V_{SB}	**Power Button Out.** Output for the chip-set Power button input.
SLBTIN	35	I	IN_{TS}	V_{SB}	**Sleep Button In.** Active (low) level indicates a user request to enter or exit Sleep mode. This pin has debounce protection.
SLPS3, SLPS5	52, 53	I	IN_{TS}	V_{SB}	**Sleep State 3 to 5.** Active (low) level indicates the system is in one of the sleep states S3, S4 or S5. These signals are generated by an external ACPI controller. **Pins** **$\overline{\text{SLPS3}}$ $\overline{\text{SLPS5}}$ Functionality** 1 1 Working state (S0) or sleep states S1 or S2 0 1 Sleep state S3 0 0 Sleep states S4 or S5 1 0 Illegal combination
SIOSCI	38	O	OD_6	V_{SB}	**System Control Interrupt.** Active (low) level indicates that a wake-up event occurred, causing the system to exit its current sleep state. External pull-up resistor to V_{SB} is required.
$\overline{\text{SIOSMI}}$	37	O	OD_6	V_{SB}	**System Management Interrupt.** Active (low) level indicates that an SMI occurred. External pull-up resistor to V_{SB} is required.
ONCTL	39	O	OD_6	V_{SB}	**Power Supply On/Off Control.** Active level (low) indicates that the power should be turned on. External pull-up resistor is required
LED1, LED2	50, 51	O	$O_{12/12}$	V_{SB}	**LED Drive.** These outputs can be connected directly to LED devices. They can be configured as one dual-colored LED or two single-colored LEDs with programmable blink rate for all LEDs.
VDDFELL	54	O	$O_{3/6}$	V_{SB}	**V_{DD} Power Fell.** Active pulse (high) indicates that the V_{DD} power supply has been turned off. Optionally, this pin can be used to drive an external circuit that pulses the V_{SB} power to the Keyboard and Mouse, thus resetting them.
WDO	55	O	$O_{3/6}$	V_{SB}	**Watchdog Out.** An active pulse (low) of a fixed width; it is generated when a watchdog time-out occurs.

1.0 Signal/Pin Connection and Description (Continued)

1.4.10 Clocks

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
32KX1_32KCLKIN[1]	42	I	IN_{OSC}	V_{PP}	**32.768 KHz Crystal Input.** Input from external crystal oscillator circuitry. **32.768 KHz Clock Oscillator Input.** Input from external clock oscillator device.
32KX2[2]	44	O	O_{OSC}	V_{PP}	**32.768 KHz Crystal Oscillator Output.** Output to external crystal oscillator circuitry.
LFCKOUT	45	O	$O_{1/2}$	V_{SB}	**Low Frequency Clock Output.** The Real-Time Clock frequency (32.768 KHz) or a 1 Hz clock output.
CLKIN	56	I	IN_{TS}	V_{SB}[3]	**Clock Input.** 48 MHz for the Legacy functions or no input clock.
HFCKOUT	13	O	$O_{2/4}$	V_{SB}	**High Frequency Clock Output.** Clock output for system use.

1. This pin is not 5-volt tolerant.
2. This pin is neither 5-volt tolerant nor back-drive protected.
3. The CLKIN signal source can be V_{DD} powered.

1.4.11 Configuration Straps

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
BADDR	100	I	IN_{CS}	V_{DD}	**Base Address.** Sampled at V_{DD} Power-Up reset to determine the base address of the configuration Index-Data register pair, as follows: No pull-up resistor: 2Eh-2Fh 10 KΩ external pull-up resistor: 4Eh-4Fh
TRIS	97	I	IN_{CS}	V_{DD}	**TRI-STATE Device.** Sampled at V_{DD} Power-Up reset to force the device to float all its output and I/O pins, as follows: No pull-up resistor: pins active 4.7 KΩ external pull-up resistor:pins floating
CKIN48	55	I	IN_{CS}	V_{SB}	**CLKIN 48 MHz.** Sampled at V_{SB} Power-Up reset to determine the presence of the 48 MHz input clock at the CLKIN pin, as follows: No pull-up resistor: no clock 10 KΩ external pull-up resistor: 48 MHz clock
XCNF2-0 (**PC87416, PC87417**)	32-34	I	IN_{CS}	V_{SB}	**X-Bus Default Configuration.** Sampled at V_{SB} Power-Up reset to set the configuration of the X-Bus transactions. **Pins** **2 1 0 Functionality** 0 x x No BIOS 1 0 0 With BIOS, XA11-4 multiplexed, XRDY disabled 1 0 1 With BIOS, XA11-4 multiplexed, XRDY enabled 1 1 0 With BIOS, XA11-4 direct, XRDY disabled 1 1 1 With BIOS, XA11-4 direct, XRDY enabled Pulled to 0 by internal resistor or set to 1 by external 10 KΩ pull-up resistor.
ACBSA (**PC87413, PC87417**)	48	I	IN_{CS}	V_{SB}	**ACCESS.bus Slave Address.** Sampled at V_{SB} Power-Up reset to determine the slave address of the device on the ACCESS.bus, as follows No pull-up resistor: D8h, D9h 10 KΩ external pull-up resistor: 60h, 61h

1.0 Signal/Pin Connection and Description (Continued)

1.4.12 Power and Ground

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
V_{SS}	11, 43, 68, 93, 115	I	GND		**Ground.** Serves for both on-chip logic, output drivers and back-up battery circuit.
V_{DD}	69, 92, 116	I	PWR		**Digital 3.3V Power Supply.** Serves as power supply for the legacy peripherals and the LPC Interface.
V_{SB}	12, 40	I	PWR		**Standby Digital 3.3V Power Supply.** Used for the ACB and X-Bus Interfaces, the GPIO ports and the clock generator. When active, it also powers the RTC and the SWC.
V_{BAT}	41	I	IN_{ULR}		**Battery Power Supply.** When V_{SB} is off, this supply provides battery back-up to the SWC registers, to the RTC and to the 32 KHz crystal oscillator. The pin is connected to the internal logic through a series resistor for UL-compliant protection.

1.5 INTERNAL PULL-UP AND PULL-DOWN RESISTORS

The signals listed in Table 3 have internal pull-up (PU) and/or pull-down (PD) resistors. The internal resistors are optional for those signals indicated as “Programmable”. See Section 11.3 on page 236 for the values of each resistor type.

Table 3. Internal Pull-Up and Pull-Down Resistors

Signal	Pin/s	Type	Comments
Parallel Port			
$\overline{\text{ACK}}$	78	PU_{220}	
$\overline{\text{AFD}}$_$\overline{\text{DSTRB}}$	90	PU_{440}	
BUSY_$\overline{\text{WAIT}}$	77	PD_{120}	
$\overline{\text{ERR}}$	88	PU_{220}	
$\overline{\text{INIT}}$	86	PU_{440}	
PE	76	PU_{220}/ PD_{110}	Programmable
SLCT	75	PD_{110}	
$\overline{\text{SLIN}}$_$\overline{\text{ASTRB}}$	84	PU_{440}	
$\overline{\text{STB}}$_$\overline{\text{WRITE}}$	91	PU_{440}	
PPDIS	121	PU_{25}	
Keyboard and Mouse Controller (KBC)			
P12, P16, P17	121, 70, 66	PU_{25}	
ACCESS.bus (ACB) Interface (PC87413 and PC87417)			
ACBCLK	47	PU_{25}	Programmable[1]
ACBDAT	46	PU_{25}	Programmable[1]

1.0 Signal/Pin Connection and Description (Continued)

Table 3. Internal Pull-Up and Pull-Down Resistors (Continued)

Signal	Pin/s	Type	Comments
System Wake-Up Control (SWC)			
$\overline{\text{PWBTIN}}$	36	PU_{25}	
$\overline{\text{SLBTIN}}$	35	PU_{25}	
$\overline{\text{PWBTOUT}}$	49	PU_{25}	Note [2]
General-Purpose Input/Output (GPIO) Ports			
GPIO00-04, 05-06, 07	124-128, 9-10, 13	PU_{25}	Programmable[3]
GPIOE10-17	1-8	PU_{25}	Programmable[3]
GPIO20-25, 26-27	14-19, 22-23	PU_{25}	Programmable[3]
GPIO30-37	24-31	PU_{25}	Programmable[3]
GPIOE40-41, 42, 43-47	20-21, 35, 49-53	PU_{25}	Programmable[3]
GPIO50-52, 53, 54, 55	36-38, 45, 54, 56	PU_{25}	Programmable[3]
GPO60-62, 63, 64	32-34, 48, 55	PU_{50}	Programmable[3,4]
Strap Configuration			
BADDR	100	PD_{110}	Strap[5]
TRIS	97	PD_{60}	Strap[5]
CKIN48	55	PD_{110}	Strap[6]
XCNF2-0 (**PC87416, PC87417**)	32-34	PD_{110}	Strap[6]
ACBSA (**PC87413, PC87417**)	48	PD_{110}	Strap[6]

1. Default at reset: disabled.
2. Disabled when V_{DD} is off.
3. See Table 26 on page 73 for default value at reset (0 = PU disabled, 1 = PU enabled).
4. Disabled during V_{SB} Power-Up reset.
5. Active only during V_{DD} Power-Up reset.
6. Active only during V_{SB} Power-Up reset.

2.0 Power, Reset and Clocks

2.1 POWER

2.1.1 Power Planes

The PC8741x devices have three power planes (wells), as shown in the table below:

Table 4. Power Planes

Power Plane	Description	Power Pins	Ground Pins
Main	Powers the Legacy modules (Serial Ports, Parallel Port, FDC, KBC), the LPC Interface, part of the Configuration Control and some external signals[1]	V_{DD}	V_{SS}
Standby	Powers the ACCESS.bus and X-Bus Interfaces, the GPIO ports, the Clock Generator, part of the SWC, part of the Configuration Control and some external related signals[1]	V_{SB}	V_{SS}
Backup	Powers the RTC, the 32.768 KHz clock/crystal oscillator, part of the SWC and some functions that must be preserved at all times[1]	V_{PP}[2]	V_{SS}

1. See the tables in Section 1.4 (pages 23-30), specifically the *Power Well* column.
2. V_{PP} is an internal power signal derived from V_{SB} or V_{BAT}. V_{PP} is taken from V_{SB} if it is greater than the minimum value defined in Section 11.1.5; otherwise it is taken from V_{BAT}. For more details on switching between them, refer to Section 8.2.9.

For correct operation, either V_{SB} or V_{BAT} must be applied whenever V_{DD} is applied.

2.1.2 Power States

The PC8741x devices have four power states:

- **Battery Fail** - the Main, Standby and Backup power planes are all powered off (V_{DD}, V_{SB} and V_{BAT} are inactive).
- **Power Fail** - the Main and Standby power planes are powered off; the Backup power plane is on (V_{DD} and V_{SB} are inactive; V_{BAT} is active).
- **Power Off** - the Main power plane is powered off; the Standby power plane is on; the Backup power plane is on (V_{DD} is inactive; V_{SB} is active; V_{BAT} is irrelevant).
- **Power On** - the Main and Standby power planes are powered on; the Backup power plane may is on (V_{DD} and V_{SB} are active; V_{BAT} is irrelevant).

The following power state is illegal:

- The Main power plane is powered on, the Standby power plane is off and the Backup power plane is on or off (i.e., V_{DD} is active, V_{SB} is inactive and V_{BAT} is irrelevant).

The following table summarizes the power states described above.

Table 5. Power States and Related Power Planes

Power State	Main (V_{DD})	Standby (V_{SB})	Backup (V_{PP})	V_{BAT}
Battery Fail	Off	Off	Off	Off
Power Fail	Off	Off	On	On
Power Off	Off	On	On	On or Off
Power On	On	On	On	On or Off
Illegal[1]	On	Off	On or Off	On or Off

1. Operation is not guaranteed and register data may be corrupted.

2.0 Power, Reset and Clocks (Continued)

Figure 1 shows the power state transitions:

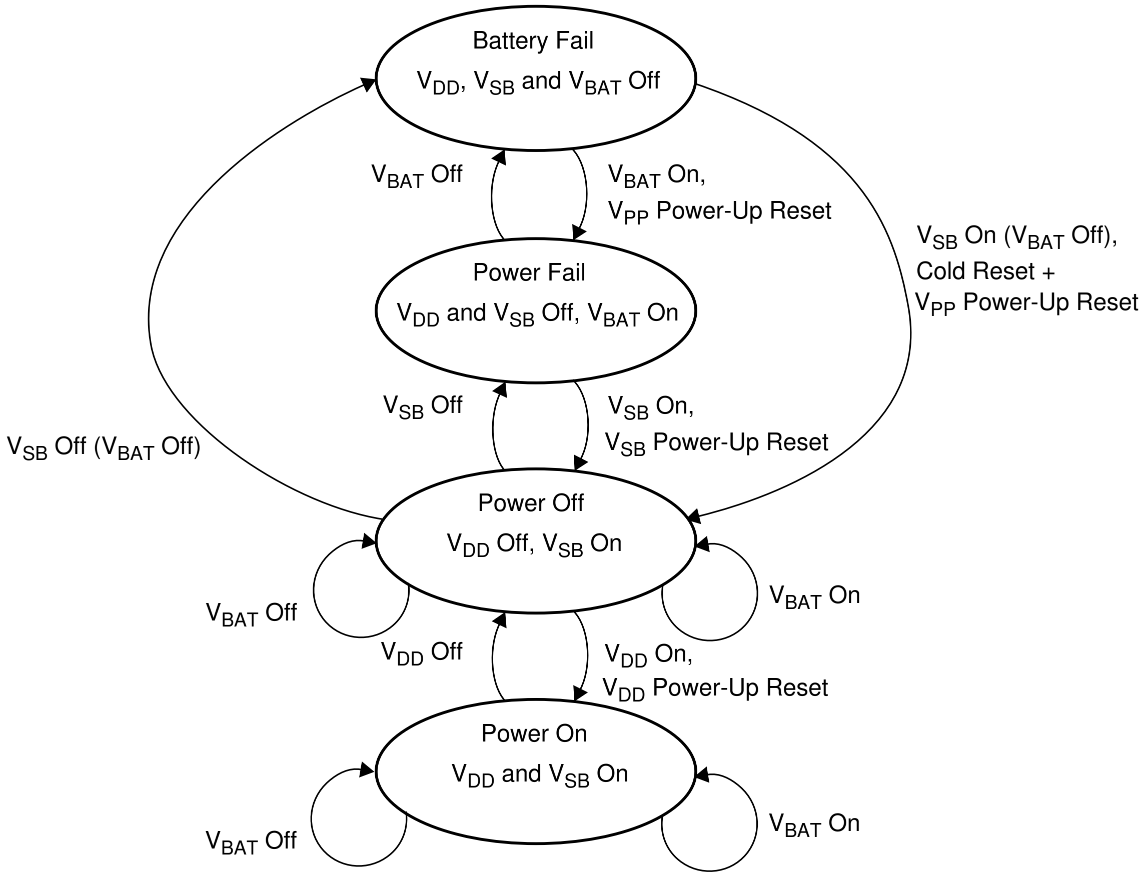


Figure 1. Power State Transitions

2.1.3 Power Connection and Layout Guidelines

The PC8741x requires a power supply voltage of 3.3V ± 10% for both the V_{DD} and the V_{SB} supplies. The device is designed to operate with a Lithium backup battery supplying up to 3.6V. Therefore, it includes an internal current-limiting resistor on the V_{BAT} input to prevent the battery from shorting, as required by the UL regulations.

V_{DD}, V_{SB} and V_{BAT} use a common ground return marked V_{SS}.

To obtain the best performance, bear in mind the following recommendations.

Ground Connection. The following items must be connected to the ground layer (V_{SS}) as close to the device as possible:

- The five ground return (V_{SS}) pins.
- The decoupling capacitors of the Main power supply (V_{DD}) pins.
- The decoupling capacitors of the Standby power supply (V_{SB}) pins.
- The decoupling capacitor of the Backup battery (V_{BAT}) pin.

Note that a low-impedance ground layer also improves noise isolation.

Decoupling Capacitors. The following decoupling capacitors must be used in order to reduce EMI and ground bounce:

- Main power supply (V_{DD}): Place one capacitor of 0.1 µF on *each* V_{DD}-V_{SS} pin pair as close to the pin as possible. In addition, place one 10–47 µF tantalum capacitor on the common net as close to the chip as possible.
- Standby power supply (V_{SB}): Place one capacitor of 0.1 µF on *each* V_{SB}-V_{SS} pin pair as close to the pin as possible. In addition, place one 10–47 µF tantalum capacitor on the common net as close to the chip as possible.
- Backup battery (V_{BAT}): Place one capacitor of 0.1 µF on the V_{BAT} pin as close to the pin as possible. In addition, place one 4.7–10 µF ceramic capacitor on the common net as close to the chip as possible.

2.0 Power, Reset and Clocks (Continued)

2.2 RESET SOURCES AND TYPES

The PC8741x devices have up to six reset sources:

- **V_{PP} Power-Up Reset** - activated when either V_{SB} or V_{BAT} is powered up after both have been off.
- **V_{SB} Power-Up Reset** - activated when V_{SB} is powered up.
- **V_{DD} Power-Up Reset** - activated when V_{DD} is powered up.
- **Hardware Reset** - activated when the $\overline{\text{LRESET}}$ input is asserted (low).
- **Host Software Reset** - triggered by the HSWRST bit of the SIOCF1 register (see Section 3.7.2 on page 49); the HSWRST bit is set by the host through the LPC Interface.
- **Controller Software Reset (PC87413 and PC87417)** - triggered by the CSWRST bit of the ACBCFG register (see Section 6.3.3 on page 128); the CSWRST bit is set by the system controller through the ACCESS.bus Interface.

Unless otherwise noted, reset references throughout the modules of the PC8741x devices default to the following resets:

- For V_{PP}-retained functions (RTC, part of SWC and some other functions): V_{PP} Power-Up reset.
- For V_{SB}-powered functions (ACCESS.bus, X-Bus, GPIO ports, Clock Generator, part of SWC and part of Configuration Control): V_{SB} Power-Up reset or Controller Software Reset (within the limitations described in Section 2.2.3).
- For V_{DD}-powered functions (Legacy modules, LPC and part of Configuration Control): V_{DD} Power-Up reset, Hardware Reset or Host Software Reset (within the limitations described in Section 2.2.6).

The following sections detail the sources and effects of the various resets on the PC8741x devices per reset source.

2.2.1 V_{PP} Power-Up Reset

V_{PP} is an internal power signal derived from V_{SB} and V_{BAT}. V_{PP} Power-Up reset is generated by an internal circuit that detects the status of the V_{PP} power. An active V_{PP} Power-Up reset signal is generated following a rise in the V_{PP} until the V_{PP} power within the accepted range is detected (see Section 11.1.5 on page 232). When V_{PP} Power-Up reset is active, it resets the modules and registers whose values are retained by V_{PP} (RTC, part of SWC and some other functions). The V_{PP} Power-Up reset also activates the 32 KHz internal crystal oscillator.

2.2.2 V_{SB} Power-Up Reset

V_{SB} Power-Up reset is generated by an internal circuit when V_{SB} power is applied. This reset is completed after 8,192 cycles of the 32 KHz clock (t_{32KOSC}). However, if the 32 KHz on-chip crystal oscillator was disabled before V_{SB} power-up, a delay of t_{32KW} (see *Low Frequency Clock Timing* on page 242) is added to t_{IRST} (see *VSB Power-Up Reset* on page 239) to account for the time required by the 32 KHz oscillator to stabilize. In addition, if the Hardware reset ($\overline{\text{LRESET}}$) is de-asserted in an early stage, only 1,280 clock cycles are required to complete the V_{SB} Power-Up reset.

External devices should wait at least t_{IRST} before accessing the PC8741x device. However, if the system controller accesses the PC8741x device (through the ACCESS.bus) before t_{IRST} ends, both the ACBDAT and the ACBCLK signals will float until the end of V_{SB} Power-Up reset, which is when the ACCESS.bus Interface becomes operational. Since these signals are pulled-up by external resistors, this situation is equivalent to generating a NACK condition in response to the system controller access (see Section 6.2.4 on page 118).

V_{SB} Power-Up reset performs the following actions and all the actions performed by V_{DD} Power-Up reset (if the V_{DD} power is already active):

- Activates the Clock Generator and sets its output to the default frequency.
- Puts pins with V_{SB} strap options into TRI-STATE and enables their internal pull-down resistors.
- Samples the logic levels of the V_{SB} strap pins.
- Sets up the PC8741x device slave address on the ACCESS.bus (**PC87413 and PC87417**).
- Resets the V_{SB}-powered lock bits in the Configuration Control and X-Bus (**PC87416 and PC87417**).
- Loads default values to the GPIO Configuration bits: VDDLOAD and BUSCTL.
- Loads default values to the V_{SB}-powered bits in SWC.
- Loads default values to the bits in ACCESS.bus Interface (**PC87413 and PC87417**).
- Sets up the pull-up option and the default source for the V_{SB}-powered multiplexed output pins.
- Executes all the actions performed by the Controller Software reset (see Section 2.2.3 on page 35) in **all PC8741x devices**.

2.0 Power, Reset and Clocks (Continued)

2.2.3 Controller Software Reset (PC87413 and PC87417)

The Controller Software reset is initiated by the system controller through the ACCESS.bus Interface. The system controller can trigger this reset by setting the CSWRST bit of the ACBCFG register (see Section 6.3.3 on page 128).

The Controller Software reset performs the following actions:

- Updates the V_{SB}-powered strap configuration bits with the strap levels sampled during the V_{SB} Power-Up reset.
- Loads default values to the V_{SB}-powered unlocked bits in the Configuration Control and X-Bus (**PC87416 and PC87417**).
- Loads default values to the unlocked GPIO Configuration and Data bits for those GPIO ports with VDDLOAD = 0. The VDDLOAD and BUSCTL bits are not affected.
- Loads default values to the bits in the ACBCST, ACBDIS and ACBTRIS registers of the ACCESS.bus Interface (**PC87413 and PC87417**).
- Terminates any transaction involving the internal modules of the PC8741x device that were initiated by the ACCESS.bus Interface.

2.2.4 V_{DD} Power-Up Reset

V_{DD} Power-Up reset is generated by an internal circuit when V_{DD} power is turned on. This reset is completed after 8,192 cycles of the 32 KHz clock (t_{32KOSC}; see *Low Frequency Clock Timing* on page 242). However, if the Hardware reset ($\overline{\text{LRESET}}$) is de-asserted in an early stage, t_{IRST} (see *VSB Power-Up Reset* on page 239) is shortened to only 1,280 clock cycles. In any condition, the V_{DD} Power-Up reset ends after the V_{SB} Power-Up reset.

External devices must wait at least t_{IRST} before accessing the PC8741x device. If the host processor accesses the device during this time, the PC8741x device ignores the transaction (that is, it does not return SYNC response).

V_{DD} Power-Up reset performs the following actions:

- Puts pins with V_{DD} strap options into TRI-STATE and enables their internal pull-down resistors.
- Samples the logic levels of the V_{DD} strap pins.
- Executes all the actions performed by the Hardware reset (see Section 2.2.5 on page 35).

2.2.5 Hardware Reset

Hardware reset is activated by the assertion (low) of the $\overline{\text{LRESET}}$ input while V_{DD} is “good”. When the V_{DD} power is Off, the PC8741x device ignores the level of the $\overline{\text{LRESET}}$ input. Hardware reset performs the following actions:

- Resets the V_{SB}-powered lock bits in the Configuration Control and X-Bus (**PC87416 and PC87417**), if VSBLOCK = 0 in the ACBLKCTL register (in PC87414 and PC87416, VSBLOCK is always ‘0’).
- Sets up the pull-up option and the default source for the V_{DD}-powered multiplexed output pins.
- Executes all the actions performed by the Host Software reset (see Section 2.2.6 on page 35).

2.2.6 Host Software Reset

The Host Software reset is triggered by the host setting the HSWRST bit of the SIOCF1 register (see Section 3.7.2 on page 49) through the LPC Interface. The Host Software reset performs the following actions:

- Updates the V_{DD}-powered strap configuration bits with the strap levels sampled during the V_{DD} Power-Up reset.
- Loads default values to the V_{DD}-powered unlocked bits in the Configuration Control.
- Loads default values to the V_{SB}-powered unlocked GPIO Configuration and Data bits for those GPIO ports with VDDLOAD = 1. The VDDLOAD and BUSCTL bits are not affected.
- Resets all the V_{DD}-powered Legacy logical devices.
- Loads default values to all the V_{DD}-powered Legacy module registers.
- Terminates any transaction involving the internal modules of the PC8741x device that were initiated by the LPC bus Interface.

2.0 Power, Reset and Clocks (Continued)

2.3 CLOCK GENERATION

2.3.1 Clock Domains

The PC8741x devices have five clock domains, as shown in Table 6.

Table 6. Clock Domains of the PC8741x

Clock Domain	Frequency	Source	Usage
LPC	Up to 33 MHz	LPC clock input (LCLK)	LPC bus Interface
Legacy	48 MHz	Clock input (CLKIN) or Clock Generator	Legacy functions (Serial Ports, Parallel Port, FDC, KBC)
Output Clock	Up to 40 or 48 MHz	Clock Generator	External Devices
Standby	20 or 24 MHz	Clock Generator	V_{SB}-powered functions (ACCESS.bus and X-Bus Interfaces)
RTC	32.768 KHz	Clock input or on-chip oscillator (32KX1, 32KX2)[1]	RTC, Clock Generator, SWC, GPIO

1. See Section 8.2 on page 142.

The LPC and Legacy clock domains, and the modules using them, are powered by the Main power plane. Therefore, these two clock domains are only active when the V_{DD} power supply is on; however, if the Legacy clock domain is sourced by the Clock Generator, it is active also during the time V_{DD} power supply is off.

The Standby and Output clock domains are sourced by the Clock Generator, which is supplied by the Standby power plane. These two clock domains are active while the V_{SB} power supply is on. Both clock domains require a certain amount of time to stabilize after V_{SB} becomes active. Moreover, if the 32 KHz on-chip crystal oscillator was disabled before V_{SB} power-up, the time required for the clocks to stabilize is t_{32KOSC} (see Section 11.5.3 on page 241). The selection of 40 MHz (or its divisions) or 48 MHz (or its divisions) is set by the CKIN48 strap.

The RTC clock domain is sourced either by a clock input or by the on-chip crystal oscillator, which are supplied by the Backup power plane. This clock domain is active while either the V_{BAT} or V_{SB} power supply is on. At V_{BAT} or V_{SB} power-up, the clock requires t_{32KOSC} to stabilize.

2.3.2 Clock Generator

The Clock Generator is the source of the Standby and Output clock domains; it is also the source of the Legacy clock domain if the 48 MHz clock input is not available. The Clock Generator is fed by the 32.768 KHz from the on-chip crystal oscillator and supplied by the Standby power plane. It starts generating clock output either after the V_{SB} power supply is turned on (if the 32.768 KHz clock is already stable) or after the 32.768 KHz clock stabilizes (if V_{BAT} was inactive previous to V_{SB} power-on), whichever occurs last.

Operation

Figure 2 shows a simplified diagram of the Clock Generator.

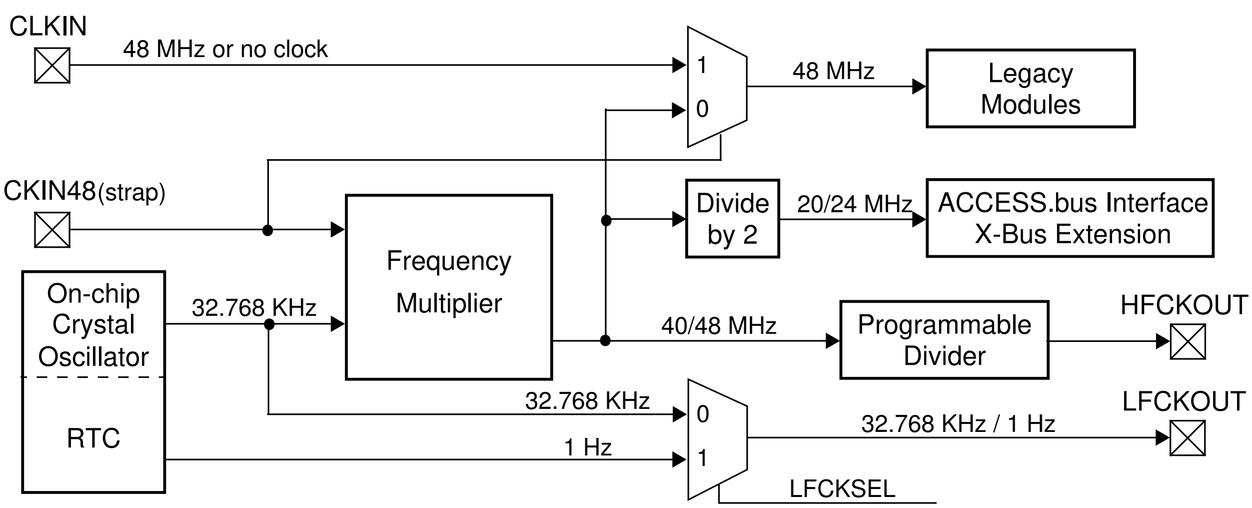


Figure 2. Clock Generator - Simplified Diagram

2.0 Power, Reset and Clocks (Continued)

The Frequency Multiplier generates either a 40 MHz or a 48 MHz clock out of the 32.768 KHz clock from the on-chip crystal oscillator (which is a part of the RTC module; see Section 8.2.2 on page 142). The frequency is selected by the value read at V_{SB} Power-Up reset from the CKIN48 strap input pin (available for read in the CKIN48 bit of the CLOCKCF register; see Section 3.7.10 on page 56):

- A strap value of ‘0’ configures the PC8741x device to work without a clock signal that is connected to the CLKIN pin and to generate a 48 MHz internal clock. This clock is used for the Standby and Output clock domains and is also selected for the Legacy modules.
- A strap value of ‘1’ configures the PC8741x device to work with a 48 MHz clock signal connected to the CLKIN pin and to generate a 40 MHz internal clock. This clock is used only for the Standby and Output clock domains. The 48 MHz input clock is selected for the Legacy modules.

The internal clock generated by the Frequency Multiplier is divided by two and used as the basic clock for the ACCESS.bus Interface and X-Bus Extension modules. In addition, it is scaled-down by a programmable divider and generates the HFCKOUT signal.

On power-up, when V_{SB} is applied, the Frequency Multiplier waits for the 32.768 KHz clock to stabilize before it starts generating the internal clock. The multiplier output clock is frozen to a low level until the multiplier provides a stable clock signal that meets all requirements. Then the multiplier output clock starts toggling.

The status of the internal clock is indicated by the CKVALID bit of the CLOCKCF register. While either the on-chip crystal oscillator or the Frequency Multiplier is stabilizing, this bit is 0, indicating an internal clock frozen at low level. When the internal clock starts toggling, this bit is set to 1. The software must activate (enable) the Legacy modules (Serial Ports, Parallel Port, FDC, KBC) only after the CKVALID bit is set.

The programmable divider scales down the frequency of the internal clock according to the CKIN48 strap and the HFCKDV field of the CLOCKCF register (see Section 3.7.10 on page 56), as shown in Table 7.

.

Table 7. HFCKOUT Frequency Selection

HFCKOUT Frequency		HFCKDIV Field			Divisor	Default
CKIN48 = 0	**CKIN48 = 1**	**Bit 2**	**Bit 1**	**Bit 0**		
48 MHz	40 MHz[1]	0	0	0	1	40 MHz at CKIN48=1
24 MHz	20 MHz	0	0	1	2[2]	24 MHz at CKIN48=0
16 MHz	13.333 MHz	0	1	0	3	
12 MHz	10 MHz	0	1	1	4	
8 MHz	6.667 MHz	1	0	0	6	
6 MHz	5 MHz	1	0	1	8	
4 MHz	3.333 MHz	1	1	0	12	
3 MHz	2.5 MHz	1	1	1	16	

1. The actual value is 40.004 MHz.
2. The output signal, generated using all the division ratios (divisors), has an accurate 50% duty cycle.

During frequency transitions caused by software changing the HFCKDIV field value, the output clock is guaranteed to be glitch free. The high or low level of the clock signal is stable for at least half of the shortest cycle between the previous and the new frequency.

When the alternate function (GPIO07) is selected for the device pin (see Section 3.7.3 on page 50) or if the HFCKDIS bit in the CLOCKCF register is set, the programmable divider is disabled to save power. When the programmable divider is disabled by setting the HFCKDIS bit, HFCKOUT is stopped at low level.

Specifications

Frequency Multiplier wake-up time is 33 msec (maximum). This is measured from a valid V_{SB} or a valid 32.768 KHz clock until the internal clock is stable. Tolerance (long term deviation) of the multiplier output clock, relative to the 32.768 KHz clock, is ±110 ppm. Total tolerance is therefore ± (input clock tolerance + 110 ppm). Cycle-by-cycle variance is 0.4 nsec (maximum).

2.3.3 Low Frequency Clock

This clock output is obtained by selecting to the LFCKOUT pin either the 32.768 KHz clock or a 1 Hz signal (generated by the RTC). The LFCKSEL bit in the CLOCKCF register (see Section 3.7.10 on page 56) is responsible for the selection. The transition from one clock source to the other is not guaranteed to be glitch free.

3.0 Device Architecture and Configuration

The PC8741x devices comprise a collection of legacy and proprietary functional blocks. Each functional block is described in a separate chapter in this document. However, some parameters in the implementation of each functional block may vary per ServerI/O device. This chapter describes the structure of the PC8741x devices and provides all logical device specific information, including special implementation of generic blocks, system interface and device configuration.

3.1 OVERVIEW

The PC8741x consists of the following: up to 10 logical devices, the host interface, the system controller interface and a central set of configuration registers. All these components are built around a central, internal bus. The internal bus is similar to an 8-bit ISA bus protocol. See the Block Diagram on page 1, which illustrates the blocks and the internal bus.

The host, via the LPC Interface, can access the modules connected to the Internal bus. This interface supports 8-bit I/O Read/Write, 8-bit Memory Read/Write and 8-bit DMA transactions of the LPC bus (see Section 4.2 on page 90).

The system controller can access these modules via the ACB Interface (**PC87413 and PC87417**). This interface supports slave operation for 8-bit I/O Read/Write and 8-bit Memory Read/Write transactions of the ACCESS.bus (see Section 6.2 on page 117).

Both the host and system controller accesses occur concurrently via the Internal bus.

The central configuration register set is ACPI compliant and supports PnP configuration. The configuration registers are structured as a subset of the Plug and Play Standard registers, defined in Appendix A of the *Plug and Play ISA Specification, Revision 1.0a* by Intel and Microsoft®. All system resources assigned to the functional blocks (I/O address space, IRQ numbers and DMA channels) are configured in and managed by the central configuration register set. In addition, some function-specific parameters are configurable through the configuration registers and distributed to the functional blocks through special control signals. Access through the ACB Interface (**PC87413 and PC87417**) ignores the PnP configuration registers and thus the system resources assigned through them.

3.2 CONFIGURATION STRUCTURE AND ACCESS

The configuration structure is comprised of a set of banked registers that are accessed via a pair of specialized registers.

3.2.1 The Index-Data Register Pair

Access to the ServerI/O configuration registers is via an Index-Data register pair, using only two system I/O byte locations. The base address of this register pair is determined during reset, according to the state of the hardware strapping option on the BADDR pin. Table 8 shows the selected base addresses as a function of BADDR. The I/O location of the Index-Data register pair is irrelevant when the configuration is accessed through the ACB Interface.

Table 8. BADDR Strapping Options

BADDR	I/O Address	
	Index Register	**Data Register**
0	2Eh	2Fh
1	4Eh	4Fh

The Index register is an 8-bit read/write register located at the selected base address (Base+0). It is used as a pointer to the configuration register file and holds the index of the configuration register that is currently accessible via the Data register. Reading the Index register returns the last value written to it (or the default of 00h after reset).

The Data register is an 8-bit register (Base+1) used as a data path to any configuration register. Accessing the Data register actually accesses the configuration register that is currently pointed to by the Index register.

The Index, Data and Logical Device Number registers are duplicated to enable concurrent access to the configuration registers from the LPC bus and ACCESS.bus, without contention (**PC87413 and PC87417**). Each bus has its own set of registers (Index/Data/LDN) powered from the V_{SB} well (ACCESS.bus set) or the V_{DD} well (LPC bus set). This power scheme allows access to the configuration registers of the V_{SB}-powered modules while in Power Off state (V_{DD} off). In this case, access is possible only through the ACCESS.bus.

3.0 Device Architecture and Configuration (Continued)

3.2.2 Banked Logical Device Registers Structure

Each functional block is associated with a Logical Device Number (LDN). The configuration registers are grouped into banks, where each bank holds the standard configuration registers of the corresponding logical device. Table 9 shows the LDN values of the PC8741x functional blocks. Any value not listed is reserved.

Figure 3 shows the structure of the standard configuration register file. The LDN and ServerI/O Configuration registers are not banked and are accessed by the Index-Data register pair only, as described above. However, the device control and device configuration registers are duplicated over 10 banks for the 10 logical devices. Therefore, accessing a specific register in a specific bank is performed by two-dimensional indexing, where the LDN register selects the bank (or logical device) and the Index register selects the register within the bank. Accessing the Data register while the Index register holds a value of 30h or higher actually accesses the configuration registers of the logical device selected by the LDN register and pointed to by the Index register.

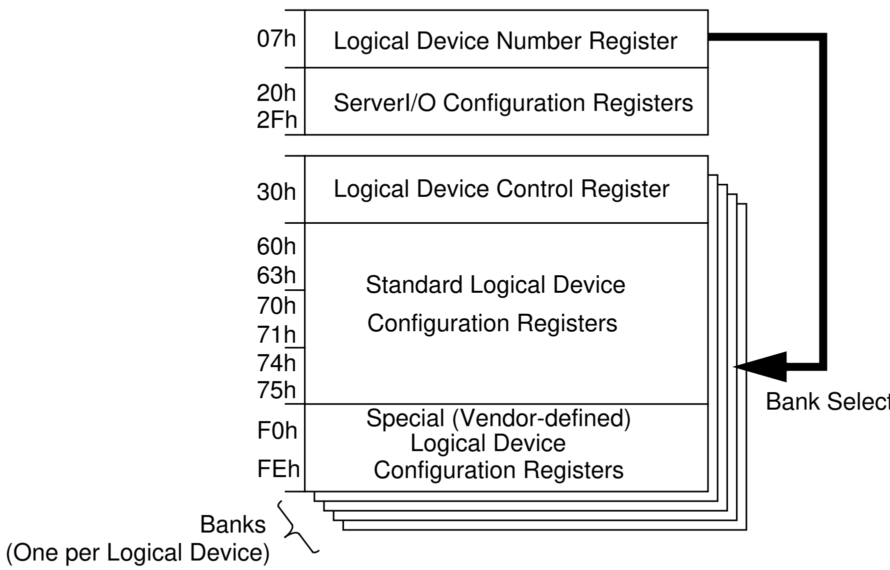


Figure 3. Structure of Standard Configuration Register File

Table 9. Logical Device Number (LDN) Assignments

LDN	Functional Block
00h	Floppy Disk Controller (FDC)
01h	Parallel Port (PP)
02h	Serial Port 2 (SP2)
03h	Serial Port 1 (SP1)
04h	System Wake-Up Control (SWC)
05h	Keyboard and Mouse Controller (KBC) - Mouse Interface
06h	Keyboard and Mouse Controller (KBC) - Keyboard Interface
07h	General-Purpose I/O (GPIO) Ports
0Fh	X-Bus Extension (**PC87416 and PC87417**)
10h	Real Time Clock (RTC)

Write accesses to unimplemented registers (i.e., accessing the Data register while the Index register points to a non-existing register) are ignored. Read accesses return 00h on all addresses, except for 74h and 75h (DMA configuration registers), which returns 04h (indicating no DMA channel). The configuration registers are accessible immediately after reset.

3.0 Device Architecture and Configuration (Continued)

3.2.3 Standard Configuration Register Definitions

In the registers below, any undefined bit is reserved. Unless otherwise noted, the following definitions also hold true:

- All registers are read/write.
- All reserved bits return 0 on reads, except where noted otherwise. To prevent unpredictable results, do not modify these bits. Use read-modify-write to prevent the values of reserved bits from being changed during write.
- Write-only registers must not use read-modify-write during updates.

Table 10. Standard General Configuration Registers

Index	Register Name	Description
07h	Logical Device Number	This register selects the current logical device. See Table 9 for valid numbers. All other values are reserved.
20h - 2Fh	ServerI/O Configuration	ServerI/O configuration registers and ID registers.

Table 11. Logical Device Activate Register

Index	Register Name	Description
30h	Activate	Bit 0 - Logical device activation control (see Section 3.3 on page 43) 0: Disabled 1: Enabled Bits 7-1 - Reserved

Table 12. I/O Space Configuration Registers

Index	Register Name	Description
60h	I/O Port Base Address Bits (15-8) Descriptor 0	Indicates selected I/O lower limit address bits 15-8 for I/O Descriptor 0.
61h	I/O Port Base Address Bits (7-0) Descriptor 0	Indicates selected I/O lower limit address bits 7-0 for I/O Descriptor 0.
62h	I/O Port Base Address Bits (15-8) Descriptor 1	Indicates selected I/O lower limit address bits 15-8 for I/O Descriptor 1.
63h	I/O Port Base Address Bits (7-0) Descriptor 1	Indicates selected I/O lower limit address bits 7-0 for I/O Descriptor 1.

3.0 Device Architecture and Configuration (Continued)

Table 13. Interrupt Configuration Registers

Index	Register Name	Description
70h	Interrupt Number and Wake-Up on IRQ Enable	Indicates selected interrupt number. Bits 7-5 - Reserved. Bit 4 - Enables a Power Management event (SCI or wake-up) from the IRQ of the logical device. When enabled, IRQ assertion sets the respective *XXX*_IRQ_STS bit (*XXX* is MOD, MS or KBD) in the GPE1_STS_3 register (see Section 9.4.11 on page 211). 0: Disabled (default) 1: Enabled **Note:** If the BIOS routine that sets IRQ does not use a Read-Modify-Write sequence, it might reset bit 4. To ensure that the system wakes up, the BIOS must set bit 4 before the system goes to sleep. Bits 3-0 select the interrupt number. A value of 1 selects IRQ1. A value of 15 selects IRQ15. IRQ0 is not a valid interrupt selection and represents no interrupt selection. **Note:** Avoid selecting the same interrupt number (except 0) for different Logical Devices, as it causes the PC8741x device to behave unpredictably.
71h	Interrupt Request Type Select	Indicates the type and polarity of the interrupt request number selected in the previous register. If a logical device supports only one type of interrupt, the corresponding bit is read-only. Bits 7-2 - Reserved. Bit 0 - Type of interrupt request selected in previous register 0: Edge 1: Level Bit 1 - Polarity of interrupt request selected in previous register 0: Low polarity 1: High polarity

Table 14. DMA Configuration Registers

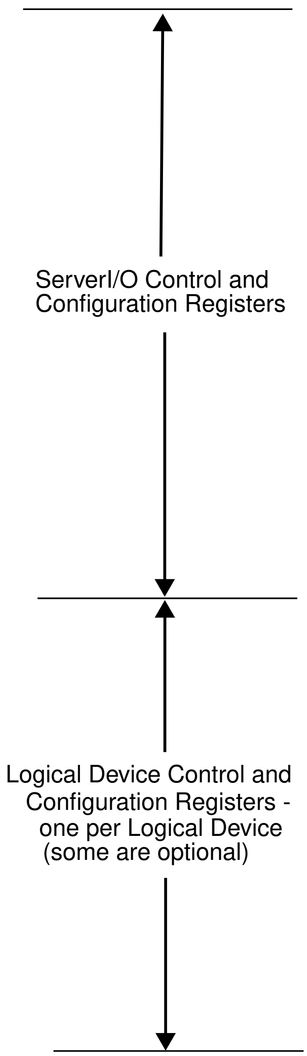
Index	Register Name	Description
74h	DMA Channel Select 0	Indicates selected DMA channel for DMA 0 of the logical device (0 - The first DMA channel in case of using more than one DMA channel). Bits 7-3 - Reserved. Bits 2-0 select the DMA channel for DMA 0. The valid choices are 0-3, where: - A value of 0 selects DMA channel 0, 1 selects channel 1, etc. - A value of 4 indicates that no DMA channel is active. - The values 5-7 are reserved. **Note:** Avoid selecting the same DMA channel (except 4) for different Logical Devices, as it causes the PC8741x device to behave unpredictably.
75h	DMA Channel Select 1	Indicates selected DMA channel for DMA 1 of the logical device (1 - The second DMA channel in case of using more than one DMA channel). Bits 7-3 - Reserved. Bits 2-0 select the DMA channel for DMA 1. The valid choices are 0-3, where: - A value of 0 selects DMA channel 0, 1 selects channel 1, etc. - A value of 4 indicates that no DMA channel is active. - The values 5-7 are reserved. **Note:** Avoid selecting the same DMA channel (except 4) for different Logical Devices, as it causes the PC8741x device to behave unpredictably.

3.0 Device Architecture and Configuration (Continued)

Table 15. Special Logical Device Configuration Registers

Index	Register Name	Description
F0h-FEh	Logical Device Configuration	Special (vendor-defined) configuration options.

3.2.4 Standard Configuration Registers



Index	Register Name
07h	Logical Device Number
20h	ServerI/O ID
21h	ServerI/O Configuration 1
22h	ServerI/O Configuration 2
23h	ServerI/O Configuration 3
24h	ServerI/O Configuration 4
25h	ServerI/O Configuration 5
26h	ServerI/O Configuration 6
27h	ServerI/O Revision ID
28h	ServerI/O Configuration 8
29h	Clock Generator Configuration
2Ah	ACCESS.bus Configuration
2Bh - 2Fh	Reserved for National use
30h	Logical Device Control (Activate)
60h	I/O Base Address Descriptor 0 Bits 15-8
61h	I/O Base Address Descriptor 0 Bits 7-0
62h	I/O Base Address Descriptor 1 Bits 15-8
63h	I/O Base Address Descriptor 1 Bits 7-0
70h	Interrupt Number and Wake-Up on IRQ Enable
71h	IRQ Type Select
74h	DMA Channel Select 0
75h	DMA Channel Select 1
F0h - FFh	Device Specific Logical Device Configuration

Figure 4. Configuration Register Map

ServerI/O Control and Configuration Registers

The ServerI/O configuration registers at indexes 20h (ServerI/O ID) and 27h (ServerI/O Revision ID) are used for part identification. The other configuration registers are used for global power management and selecting pin multiplexing options. For details, see Section 3.7 on page 48.

Logical Device Control and Configuration Registers

A subset of these registers is implemented for each logical device. See functional block descriptions in the following sections.

3.0 Device Architecture and Configuration (Continued)

Control

The only implemented control register for each logical device is the Activate register at index 30h. Bit 0 of the Activate register controls the activation of the associated functional block. Activation enables access to the functional block's runtime registers and attaches its system resources, which are unassigned as long as it is not activated. Other effects may apply on a function-specific basis (such as clock enable and active pinout signaling). Access to the configuration register of the logical device is enabled even when the logical device is not activated.

Standard Configuration

The standard configuration registers manage the PnP resource allocation to the functional blocks. The I/O port base address descriptor 0 is a pair of registers at Index 60-61h that hold the first 16-bit base address for the register set of the functional block. An optional 16-bit second base-address (descriptor 1) at index 62-63h is used for logical devices with more than one continuous register set. Interrupt Number and Wake-Up on IRQ Enable (index 70h) and IRQ Type Select (index 71h) allocate an IRQ line to the block and control its type. DMA Channel Select 0 (index 74h) allocates a DMA channel to the block, where applicable. DMA Channel Select 1 (index 75h) allocates a second DMA channel, where applicable.

Special Configuration

The vendor-defined registers, starting at index F0h, control function-specific parameters such as operation modes, power saving modes, pin TRI-STATE, clock rate selection and non-standard extensions to generic functions.

3.2.5 Default Configuration Setup

The default configuration setup of the PC8741x device is determined by the six reset types described in Section 2.2 on page 34. See the specific register descriptions for the bits affected by each reset source.

In the event of a V_{DD} Power-Up (also induced by V_{SB} Power-Up reset) or Hardware reset, the PC8741x device wakes up with the following default configuration setup:

- The configuration base address is 2Eh or 4Eh, according to the BADDR strap pin value, as shown in Table 8 on page 38.
- If the VSBLOCK bit in the ACBLKCTL register is ‘0’ (see Section 6.3.4 on page 128; in **PC87414 and PC87416**, VSBLOCK is always ‘0’), all lock bits in the Configuration Control registers are reset (the protected bits are unlocked).
- All the actions performed by the Host Software reset are executed.

If a Host software reset occurs, the PC8741x device wakes up with the following default configuration setup:

- All logical devices are disabled (the Activation bit is reset) and the V_{SB}-powered logical devices (X-Bus, GPIO, RTC and SWC) remain functional but their registers cannot be accessed by the Host.
- Standard configuration registers of all logical devices are set to their default values.
- National proprietary functions are not assigned with any default resources and the default values of their base addresses are all 00h.
- All Legacy devices are reset. Default values are loaded into the Legacy module runtime registers.

3.3 MODULE CONTROL

Module control is performed primarily through the Activation bit (bit 0 of index 30h) of each logical device. The operation of each module can be controlled either by the host through the LPC bus or by the Embedded Controller through the ACCESS.bus (**PC87413 and PC87417**). This dual control is supported by two interacting mechanisms: a dual enable/disable and an access lock (the access lock is available only through the ACCESS.bus).

3.3.1 Module Enable/Disable

LPC Control. Module enable/disable by the host through the LPC bus is controlled by the following bits (see Figure 5 on page 45):

- Activation bit (bit 0) in index 30h of the Standard configuration registers (see Section 3.2.3 on page 40).
- Fast Disable bit in the SIOCF6 register (see Section 3.7.7 on page 54) - only for the FDC, Parallel Port and Serial Port 1 and 2 modules.
- Fast Disable bit in the SWCFDIS register (see Section 9.3.8 on page 185) - only for the KBC, FDC, Parallel Port and Serial Port 1 and 2 modules.
- Global Enable bit (GLOBEN) in the SIOCF1 register (see Section 3.7.2 on page 49).

A module is enabled only if all these bits are set to their “enable” value and the module's enable/disable is not controlled by the Embedded Controller as described in the next paragraph. Although possible, changing the above bits by the Embedded Controller through the ACCESS.bus (**PC87413 and PC87417**) is not recommended.

3.0 Device Architecture and Configuration (Continued)

ACCESS.bus Control. Module enable/disable by the Embedded Controller through the ACCESS.bus (**PC87413 and PC87417**) is controlled by the following bits:

- Access lock bit (*xxx*ALOK) in the ACCLCF1 and ACCLCF2 registers (see Sections 6.3.7 and 6.3.8 on pages 132ff.) - for the FDC, Parallel Port, Serial Port 1 and 2, KBC, X-Bus, RTC and SWC modules.
- Fast Disable bit in the ACBFDIS register (see Section 6.3.5 on page 130) - only for the KBC, FDC, Parallel Port and Serial Port 1 and 2 modules.

A module is enabled if both the Access lock bit is set to “lock” and the Fast Disable bit is set to “enable”. When the module enable/disable is controlled by the Embedded Controller, the setting of the Activation, Fast Disable (in both SIOCF6 and SWCFDIS) or Global Enable bits is ignored (see Figure 5 on page 45).

When a V_{DD}-powered module (FDC, Parallel Port and Serial Port 1 and 2 and KBC) is disabled, the following takes place:

- The host system resources of the logical device (IRQ, DMA and runtime address range) are unassigned.
- Access to the standard- and device-specific Logical Device configuration registers, through LPC bus or ACCESS.bus, remains enabled.
- Access to the module’s runtime registers through the LPC bus is disabled (transactions are ignored; SYNC cycle is not generated).
- Access to the module’s runtime registers through the ACCESS.bus causes unpredictable results, and therefore is not allowed.
- The module’s internal clock is disabled (the module is not functional) to lower power consumption.

When a V_{SB}-powered module (X-Bus, GPIO, RTC and SWC) is disabled, the following takes place:

- The host system resources of the logical device (IRQ, DMA and runtime address range)) are unassigned, with the exception of the XIRQ interrupt, which is not a resource of the X-Bus Extension and therefore remains operational.
- Access to the standard and device specific Logical Device configuration registers, through the LPC bus or ACCESS.bus, remains enabled.
- Access to the module’s runtime registers through the LPC bus is disabled (transactions are ignored; SYNC cycle is not generated).
- Access to the module’s runtime registers through the ACCESS.bus causes unpredictable results, and therefore is not allowed.
- The module is functional.

3.3.2 Module Lock by ACCESS.bus (PC87413 and PC87417)

A module can be locked to allow only ACCESS.bus control over its registers. In this case, only the setting of the Fast Disable bit in the ACBFDIS register controls the enable/disable of the module (see Figure 5 on page 45). The setting of the Activation, Fast Disable (in both SIOCF6 and SWCFDIS) or Global Enable bits is ignored. Module locking is controlled by the bits of the ACCLCF1 and ACCLCF2 registers (see Sections 6.3.7 and 6.3.8 on pages 132ff.).

When a module is locked for sole use by ACCESS.bus, the following takes place:

- The system resources of the logical device (IRQ, DMA) are forced to their inactive level, with the exception of the XIRQ interrupt, which is not a resource of the X-Bus Extension and therefore remains operational.
- Host read access to the Logical Device Standard and Device Specific configuration registers (through the LPC bus) remains enabled. Host write access to these registers is ignored.
- Host access to the module’s runtime registers (through the LPC bus) is disabled and the transaction is performed according to the setting of the ACCLMD field, as described in the next paragraph.
- The module is functional.

If, the host tries to access the runtime registers of a locked module, the LPC transaction is performed according to the value of the ACCLMD field in the ACBCFG register (see Section 6.3.3 on page 128). In addition, the ACCLVIOL bit in the ACBCST register (see Section 6.3.2 on page 127) is set, indicating a lock violation attempt.

Since a locked module and a disabled module behave similarly, the ACTSTAT bit in the ACBCFG register (see Section 6.3.3 on page 128) allows the software to control the behavior of the Activation bit when read through the LPC bus. When a module is locked or disabled by the Fast Disable bit in the ACBFDIS register, the ACTSTAT bit selects the value the host reads from the Activation bit. This value is either the actual value of the Activation bit or ‘0’ (module disabled).

3.0 Device Architecture and Configuration (Continued)

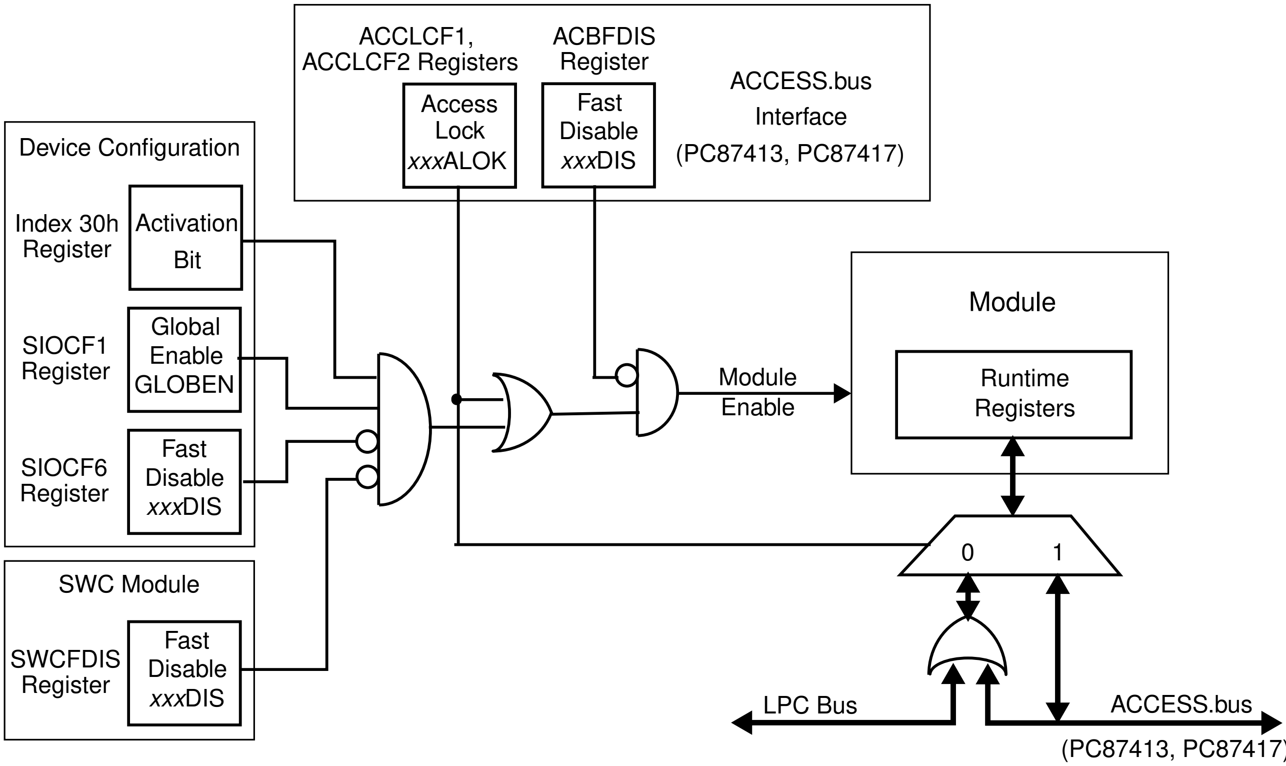


Figure 5. Module Enable and Access Control

3.4 INTERNAL ADDRESS DECODING

A full 16-bit address decoding is applied when accessing the configuration I/O space as well as the registers of the functional blocks. However, the number of configurable bits in the base address registers varies for each logical device.

The lower 1, 2, 3, 4 or 5 address bits are decoded in the functional block to determine the offset of the accessed register within the logical device's I/O range of 2, 4, 8, 16 or 32 bytes, respectively. The rest of the bits are matched with the base address register to decode the entire I/O range allocated to the logical device. Therefore, the lower bits of the base address register are forced to 0 (read only), and the base address is forced to be 2, 4, 8, 16 or 32 byte-aligned, according to the size of the I/O range.

The base address of the FDC, Serial Port 1, Serial Port 2, KBC and RTC are limited to the I/O address range of 00h to 7FXh only (bits 11-15 are forced to 0). The Parallel Port base address is limited to the I/O address range of 00h to 3F8h. The addresses of the non-legacy logical devices, including the SWC, GPIO and X-Bus, are configurable within the full 16-bit address range (up to FFFXh).

In some special cases, other address bits are used for internal decoding (such as bit 2 in the KBC and bit 10 in the Parallel Port). The KBC has two I/O base addresses with some implied dependency between them. For more details, see the description of the base address register for each logical device.

The X-Bus extension (**PC87416 and PC87417**) serves as a bridge from the LPC to the X-Bus. For module control and security function registers, the 16-bit base address is applied through the configuration address space. The lower five address bits are decoded in the X-Bus to access each register. The address ranges in the LPC I/O space and the LPC or FWH memory space that are bridged to the X-Bus are defined in the configuration section of the X-Bus bridge. The number of address bits used for this bridge decoding varies according to the specified zones and their sizes. See Sections 3.15.2 and 3.15.3 on pages 75ff. for details of the address range specifications.

3.0 Device Architecture and Configuration (Continued)

3.5 PROTECTION

The PC8741x devices provide features to protect the hardware configuration from changes made by application software running on the host.

The protection is activated by the software setting a “sticky” lock bit. Each lock bit protects a group of configuration bits located either in the same register or in different registers. When the lock bit is set, the lock bit and all the protected bits become read only and cannot be further modified by the host through the LPC bus. However, for each lock bit there is an unlock bit in the ACCESS.bus Interface (ACBLKCTL register; see Section 6.3.4 on page 128). Setting an unlock bit through the ACCESS.bus resets the corresponding lock bit, thus releasing the locked configuration bits, which again become read/write bits (**PC87413 and PC87417**).

In addition, all the lock bits are reset by power-up reset, thus unlocking the protected configuration bits. The VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128; in **PC87414 and PC87416**, VSBLOCK is always ‘0’) selects which power-up reset clears the lock bits: V_{DD} Power-Up reset (or Hardware reset) or V_{SB} Power-Up reset. Note that the locked configuration bits are not reset by the selected power-up reset, unless the selected power-up reset corresponds with the default reset defined for the power well of the locked configuration bits (see Section 2.2 on page 34).

The bit locking protection mechanism can be used optionally.

The protected groups of configuration bits are described below.

3.5.1 Multiplexed Pins Configuration Lock

Protects the configuration of all the multiplexed device pins.

Lock bit: LOCKMCF in SIOCF1 register (Device Configuration).

Unlock bit: UNLOCKM in ACBLKCTL register (ACCESS.bus Interface - **PC87413 and PC87417**).

Protected bits: DMAWAIT, IOWAIT in SIOCF1 register and all bits of the SIOCF2, SIOCF3, SIOCF4 and SIOCF5 registers (Device Configuration).

3.5.2 GPIO Ports Configuration Lock

Protects the configuration (but not the data) of all the GPIO Ports.

Lock bit: LOCKGCF in SIOCF1 register (Device Configuration).

Unlock bit: UNLOCKG in ACBLKCTL register (ACCESS.bus Interface - **PC87413 and PC87417**).

Protected bits for each GPIO Port: All bits of the GPCFG1, GPEVR and GPCFG2 registers except the LOCKCFP bit (Device Configuration).

3.5.3 Fast Disable Configuration Lock

Protects the Fast Disable bits for all the Legacy modules.

Lock bit: LOCKFDS in SIOCF6 register (Device Configuration).

Unlock bit: UNLOCKF in ACBLKCTL register (ACCESS.bus Interface - **PC87413 and PC87417**).

Protected bits: All bits of the SIOCF6 register, except the General-Purpose Scratch bits (Device Configuration).

3.5.4 Clock Generator Configuration Lock

Protects the Clock Generator configuration bits.

Lock bit: LOCKCCF in CLOCKCF register (Device Configuration).

Unlock bit: UNLOCKC in ACBLKCTL register (ACCESS.bus Interface).

Protected bits: All bits of the CLOCKCF register (Device Configuration).

3.5.5 GPIO Ports Lock

Protects the configuration and data of all the GPIO Ports.

Lock bit: LOCKCFP in GPCFG1 register, for each GPIO Port (Device Configuration).

Unlock bit: UNLOCKG in ACBLKCTL register (ACCESS.bus Interface - **PC87413 and PC87417**).

Protected bits for each GPIO Port: PUPCTL, OUTTYPE and OUTENA in GPCFG1 register; all bits of the GPCFG2 register (Device Configuration); the corresponding bit (to the port pin) in the GPDO register (GPIO Ports).

3.0 Device Architecture and Configuration (Continued)

3.5.6 X-Bus I/O Map Lock (PC87416 and PC87417)

Protects the configuration of the X-Bus I/O address mapping.

Lock bit: LOCKIOMP in XIOCNF register (Device Configuration).

Unlock bit: UNLOCKX in ACBLKCTL register (ACCESS.bus Interface - **PC87417**).

Protected bits: All bits of the XIOCNF, XIOBA1H, XIOBA1L, XIOSIZE1, XIOBA2H, XIOBA2L and XIOSIZE2 registers (Device Configuration).

3.5.7 X-Bus Memory Map Lock (PC87416 and PC87417)

Protects the configuration of the X-Bus memory address mapping.

Lock bit: LOCKMMP in XMEMCNF2 register (Device Configuration).

Unlock bit: UNLOCKX in ACBLKCTL register (ACCESS.bus Interface - **PC87417**).

Protected bits: All bits of the XMEMCNF1, XMEMCNF2, XMEMBAH, XMEMBAL and XMEMSIZE registers (Device Configuration).

3.5.8 X-Bus Chip Select Configuration Lock (PC87416 and PC87417)

Protects the configuration of the four X-Bus chip selects.

Lock bit: LOCKXSCF in XZM0 to XZM3 register (X-Bus Extension).

Unlock bit: UNLOCKX in ACBLKCTL register (ACCESS.bus Interface - **PC87417**).

Protected bits: All bits of the XBCNF, XZCNF0 to XZCNF3 and XZM0 to XZM3 registers, except the WRSTAT bit of the XZM0-XZM3 registers (X-Bus Extension).

3.5.9 X-Bus Host Protection Lock (PC87416 and PC87417)

Protects the Host Protection configuration bits for each memory block of $\overline{\text{XCS0}}$ and $\overline{\text{XCS1}}$ chip selects.

Lock bit: LOCKXHP in all 16 indexes of the HAP0 and HAP1 registers (X-Bus Extension).

Unlock bit: UNLOCKX in ACBLKCTL register (ACCESS.bus Interface - **PC87417**).

Protected bits: HWRP and HRDP bits of all 16 indexes of the HAP0 and HAP1 registers (X-Bus Extension).

3.5.10 SWC Timers Protection Lock

Protects the access to the reset of the Power Active timers in the SWC module.

Lock bit: LOCK_TMRRST in PWTMRCTL register (System Wake-Up Control).

Unlock bit: UNLOCKS in ACBLKCTL register (ACCESS.bus Interface - **PC87413 and PC87417**).

Protected bits: All bits of the PWTMRCTL register (System Wake-Up Control).

3.5.11 SWC Sleep State Configuration Lock

Protects the Sleep Type encoding configuration in the SWC module.

Lock bit: LOCK_SLP_ENC in SLP_ST_CFG register (System Wake-Up Control).

Unlock bit: UNLOCKS in ACBLKCTL register (ACCESS.bus Interface - **PC87413 and PC87417**).

Protected bits: All bits of the SLP_ST_CFG and S0_SLP_TYP to S5_SLP_TYP registers (System Wake-Up Control).

3.5.12 CMOS RAM Access Lock

Protects access lock configuration bits of the CMOS Standard and Extended RAM.

Lock bits: BLSTR, BLRWR, BLEXRWR, BLEXRRD and BLEXR in RLR register (Real-Time Clock).

Unlock bit: UNLOCKR in ACBLKCTL register (ACCESS.bus Interface - **PC87413 and PC87417**).

Protected bits: Standard and Extended CMOS RAM bits for read and/or write access by the host (Real-Time Clock; see Section 3.16.3 on page 88).

3.0 Device Architecture and Configuration (Continued)

3.6 REGISTER TYPE ABBREVIATIONS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from a specific register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

In the registers below, use one of the following methods to handle the **Reserved** bits:

- Write 0 to reserved bits, unless another “required value” is specified. This method can be used for registers containing bits of all types.
- Use read-modify-write to preserve the values of the reserved bits. This method can be used only for registers containing bits of R/W, RO, R/W1C and R/W1S types.

3.7 SERVERI/O CONFIGURATION REGISTERS

This section describes the ServerI/O configuration and ID registers (those registers with first level indexes in the range of 20h - 2Eh). See Table 16 for a summary and directory of these registers.

Table 16. ServerI/O Configuration Registers

Index	Mnemonic	Register Name	Power Well	Type	Section
20h	SID	ServerI/O ID	V_{SB}	RO	3.7.1
21h	SIOCF1	ServerI/O Configuration 1	V_{SB}	Varies per bit	3.7.2
22h	SIOCF2	ServerI/O Configuration 2	V_{SB}	R/W or RO	3.7.3
23h	SIOCF3	ServerI/O Configuration 3	V_{SB}	R/W or RO	3.7.4
24h	SIOCF4	ServerI/O Configuration 4	V_{SB}	R/W or RO	3.7.5
25h	SIOCF5	ServerI/O Configuration 5	V_{SB}	R/W or RO	3.7.6
26h	SIOCF6	ServerI/O Configuration 6	V_{SB}	Varies per bit	3.7.7
27h	SRID	ServerI/O Revision ID	V_{SB}	RO	3.7.8
28h	SIOCF8	ServerI/O Configuration 8	V_{SB}	R/W	3.7.9
29h	CLOCKCF	Clock Generator Configuration	V_{SB}	Varies per bit	3.7.10
2Ah	ACBCF	ACCESS.bus Configuration	V_{PP}	R/W or RO	3.7.11
2Bh - 2Fh	Reserved for National use				

3.0 Device Architecture and Configuration (Continued)

3.7.1 ServerI/O ID Register (SID)

This register contains the identity number of the device family. The PC8741x family is identified by the value EEh.

Power Well: V_{SB}

Location: Index 20h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Family ID**							
Reset	EEh							

Bit	Description
7-0	**Family ID.** These bits identify a family of devices with similar functionality but with different implemented options.

3.7.2 ServerI/O Configuration 1 Register (SIOCF1)

Power Well: V_{SB}

Location: Index 21h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKMCF**	**LOCKGCF**	**Reserved**		**IOWAIT**		**HSWRST**	**GLOBEN**
Reset	0	0	0	1	0	0	0	1

Bit	Type	Description
7	R/W1S	**LOCKMCF (Lock Multiplexing Configuration).** When set to 1, this bit locks the configuration of registers SIOCF1, SIOCF2, SIOCF3, SIOCF4 and SIOCF5 by disabling writing to all bits in these registers (including the LOCKMCF bit itself), except for the LOCKGCF, HSWRST and GLOBEN bits of SIOCF1. Once set, this bit can be cleared either by V_{DD} Power-Up reset (or Hardware reset) or by V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKM bit in the ACBLKCTL register (**PC87413 and PC787417**). 0: R/W bits are enabled for write (default) 1: All bits are RO
6	R/W1S	**LOCKGCF (Lock GPIO Pins Configuration).** When set to 1, this bit locks the configuration registers of all the GPIO pins (see Section 3.14.2 on page 71) by disabling writing to all their bits (including the LOCKGCF bit itself). Once set, this bit can be cleared either by V_{DD} Power-Up reset (or Hardware reset) or by V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKG bit in the ACBLKCTL register (**PC87413 and PC787417**). 0: R/W bits are enabled for write (default) 1: All bits are RO
5-4		**Reserved** (must be ‘01’).
3-2	R/W or RO	**IOWAIT (Number of I/O Wait States).** These bits set the number of wait states for I/O transactions through the LPC bus. **Bits** **3 2 Number of wait states** 0 0: 0 (Zero - default) 0 1: 2 1 0: 6 1 1: 12

3.0 Device Architecture and Configuration (Continued)

Bit	Type	Description
1	R/W	**HSWRST (Host Software Reset).** When set to 1, this bit triggers the Host Software reset sequence (see Section 2.2.6 on page 35), after which it returns to 0. Read always returns 0. This bit is not influenced by the value of LOCKMCF. 0: Inactive (default) 1: Trigger the Host Software reset sequence
0	R/W or RO	**GLOBEN (Global Device Enable).** When set to 1, this bit allows the operation of all the logical devices of the PC8741x device (see Table 9 on page 39). The behavior of the different devices is explained in Section 3.3. When cleared, this bit forces all logical devices to be disabled simultaneously by writing to a single bit. 0: All logical devices in the PC8741x device are forced to be disabled and their resources are released 1: Each logical device may be enabled; see Section 3.3.1 on page 43 (default)

3.7.3 ServerI/O Configuration 2 Register (SIOCF2)

Power Well:V_{SB}

Location:Index 22h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**WDOMUX**	**Reserved**	**NOKBC**	**VDDFLMUX**	**P17MUX**	**P16MUX**	**P12MUX**	**CLKRNMUX**
Reset	0	0	1	0	0	0	0	0

Bit	Description
7	**WDOMUX (Watchdog Out Multiplex Control).** Selects the function connected to pin 55. 0: GPO64 port - GPIO (default) 1: $\overline{\text{WDO}}$ - SWC
6	**Reserved.**
5	**NOKBC (Keyboard and Mouse Multiplex Control).** Selects the function connected to pins 125-128. 0: GPIO01-GPIO04 ports - GPIO 1: KBCLK, KBDAT, MCLK, MDAT - KBC (default)
4	**VDDFLMUX (VDDFELL Multiplex Control).** Selects the function connected to pin 54. 0: GPIO54 - GPIO (default) 1: VDDFELL - SWC
3	**P17MUX (P17 Multiplex Control).** Selects the function connected to pin 66. 0: $\overline{\text{MTR1}}$ - FDC (default) 1: P17 port - KBC
2	**P16MUX (P16 Multiplex Control).** Selects the function connected to pin 70. 0: $\overline{\text{DR1}}$ - FDC (default) 1: P16 port - KBC
1	**P12MUX (P12 Multiplex Control).** Selects the function connected to pin 121. 0: PPDIS - Parallel Port (default)[1] 1: P12 port - KBC (internally, PPDIS is set to 0; Parallel Port enabled)
0	**CLKRNMUX ($\overline{\text{CLKRUN}}$ Multiplex Control).** Selects the function connected to pin 124. 0: GPIO00 port - GPIO (default) 1: $\overline{\text{CLKRUN}}$ - LPC Interface

1. If this feature is not used, either select the P12 port or connect an external 3.3 KΩ pull-down resistor to pin 121. If the function connected to the pin is PPDIS and the pin is left unconnected, the output signals of the parallel port will float.

3.0 Device Architecture and Configuration (Continued)

3.7.4 ServerI/O Configuration 3 Register (SIOCF3)

Power Well:V_{SB}

Location:Index 23h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**EXTSTMUX**	**SCIMUX**	**SMIMUX**	**PWBTOMUX**	**PWBTIMUX**	**SLBTIMUX**	**LED2MUX**	**LED1MUX**
Reset	EXT_ST _SELECT[1]	0	0	0	0	0	0	0

1. The reset value is the same as the value set to the EXT_ST_SELECT bit in the SLP_ST_CFG register (see Section 9.3.31 on page 200).

Bit	Description
7	**EXTSTMUX (External PM State Multiplex Control).** Selects the function connected to pins 52 and 53. 0: GPIOE46, GPIOE47 ports - GPIO (internally, $\overline{\text{SLPS3}}$ and $\overline{\text{SLPS5}}$ are both set to 1; not in S3-S5 states) 1: $\overline{\text{SLPS3}}$, $\overline{\text{SLPS5}}$ - SWC
6	**SCIMUX ($\overline{\text{SIOSCI}}$ Multiplex Control).** Selects the function connected to pin 38. 0: GPIO52 port - GPIO (default) 1: $\overline{\text{SIOSCI}}$ - SWC
5	**SMIMUX ($\overline{\text{SIOSMI}}$ Multiplex Control).** Selects the function connected to pin 37. 0: GPIO51 port - GPIO (default) 1: $\overline{\text{SIOSMI}}$ - SWC
4	**PWBTOMUX ($\overline{\text{PWBTOUT}}$ Multiplex Control).** Selects the function connected to pin 49. 0: $\overline{\text{PWBTOUT}}$ - SWC (default) 1: GPIOE43 port - GPIO
3	**PWBTIMUX ($\overline{\text{PWBTIN}}$ Multiplex Control).** Selects the function connected to pin 36. 0: $\overline{\text{PWBTIN}}$ - SWC (default) 1: GPIO50 port - GPIO (internally, $\overline{\text{PWBTIN}}$ is set to 1; Power button not active)
2	**SLBTIMUX ($\overline{\text{SLBTIN}}$ Multiplex Control).** Selects the function connected to pin 35. 0: GPIOE42 port - GPIO (default; internally, $\overline{\text{SLBTIN}}$ is set to 1; Sleep button not active) 1: $\overline{\text{SLBTIN}}$ - SWC
1	**LED2MUX (LED2 Multiplex Control).** Selects the function connected to pin 51. 0: GPIOE45 port - GPIO (default) 1: LED2 - SWC
0	**LED1MUX (LED1 Multiplex Control).** Selects the function connected to pin 50. 0: GPIOE44 port - GPIO (default) 1: LED1 - SWC

3.0 Device Architecture and Configuration (Continued)

3.7.5 ServerI/O Configuration 4 Register (SIOCF4)

Power Well:V_{SB}

Location:Index 24h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**HFCKMUX**	**LFCKMUX**		**Reserved**	**SMI2IRQ2**	**NOXBUS**	**NOADDIR**	**XRDYMUX**
Reset	0	0	0	0	0	Strap	Strap	Strap

Bit	Description
7	**HFCKMUX (HFCKOUT Multiplex Control).** Selects the function connected to pin 13. 0: HFCKOUT - Clock Generator (default) 1: GPIO07 port - GPIO
6-5	**LFCKMUX (LFCKOUT Multiplex Control).** Selects the function connected to pin 45. **Bits** **6 5 Function** 0 0: GPIO53 port - GPIO (default; internally, MSEN0 is set to 1) 0 1: LFCKOUT - Clock Generator (internally, MSEN0 is set to 1) 1 0: MSEN0 - FDC 1 1: Reserved
4	**Reserved.**
3	**SMI2IRQ2 (SMI to IRQ2 Enable).** This bit enables the SMI interrupt to the IRQ2 slot of the SERIRQ. 0: Disabled (default) 1: Enabled (the SMI interrupt is shared with the interrupt source selected to IRQ2; see Table 13 on page 41)
2	**NOXBUS (Basic X-Bus Multiplex Control).** Selects the function connected to pins 14-19 and 24-31. The default value is set according to the XCNF2 strap, sampled at V_{SB} Power-Up reset. 0: GPIO20-GPIO25, GPIO30-GPIO37 ports - GPIO 1: $\overline{\text{XRD}}$_XEN, $\overline{\text{XWR}}$_XR$\overline{\text{W}}$, XA3-XA0, XD7-XD0 - X-Bus (**PC87416 and PC87417**)
1	**NOADDIR (XA11-4 Multiplex Control).** Selects the function connected to pins 1-8. The default value is set by the XCNF1 strap if XCNF2 = 1 or to 0 if XCNF2 = 0. The XCNF2 and XCNF1 straps are sampled at V_{SB} Power-Up reset. 0: GPIOE10-GPIOE17 ports - GPIO 1: XA11-XA4 - X-Bus (**PC87416 and PC87417**)
0	**XRDYMUX (XRDY Multiplex Control).** Selects the function connected to pin 9. The default value is set by the XCNF0 strap if XCNF2 = 1 or to 0 if XCNF2 = 0. The XCNF2 and XCNF0 straps are sampled at V_{SB} Power-Up reset. 0: GPIO05 port - GPIO (internally, XRDY is set to 1; device ready) 1: XRDY - X-Bus (**PC87416 and PC87417**)

3.0 Device Architecture and Configuration (Continued)

3.7.6 ServerI/O Configuration 5 Register (SIOCF5)

Power Well: V_{SB}

Location: Index 25h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**XIRQMUX**	**XSTB2MUX**	**XSTB1MUX**	**XSTB0MUX**	**XCS3MUX**	**XCS2MUX**	**XCS1MUX**	**XCS0MUX**
Reset	0	Strap	Strap	Strap	0	0	0	Strap

Bit	Description
7	**XIRQMUX (XIRQ Multiplex Control).** Selects the function connected to pin 10. 0: GPIO06 port - GPIO (default; internally, XIRQ is set to 0; Interrupt not active) 1: XIRQ - X-Bus (**PC87416 and PC87417**)
6	**XSTB2MUX ($\overline{\text{XSTB2}}$ Multiplex Control).** Selects the function connected to pin 32. The default value is set to 0 if XCNF2 = 1 or to 1 if XCNF2 = 0. The XCNF2 strap is sampled at V_{SB} Power-Up reset. 0: $\overline{\text{XSTB2}}$ - X-Bus (**PC87416 and PC87417**) 1: GPO60 port - GPIO
5	**XSTB1MUX ($\overline{\text{XSTB1}}$ Multiplex Control).** Selects the function connected to pin 33. The default value is set to 0 if XCNF2 = 1 or to 1 if XCNF2 = 0. The XCNF2 strap is sampled at V_{SB} Power-Up reset. 0: $\overline{\text{XSTB1}}$ - X-Bus (**PC87416 and PC87417**) 1: GPO61 port - GPIO
4	**XSTB0MUX ($\overline{\text{XSTB0}}$ Multiplex Control).** Selects the function connected to pin 34. The default value is set to 0 if XCNF2 = 1 or to 1 if XCNF2 = 0. The XCNF2 strap is sampled at V_{SB} Power-Up reset. 0: $\overline{\text{XSTB0}}$ - X-Bus (**PC87416 and PC87417**) 1: GPO62 port - GPIO
3	**XCS3MUX ($\overline{\text{XCS3}}$ Multiplex Control).** Selects the function connected to pin 20. 0: GPIOE40 port - GPIO (default) 1: $\overline{\text{XCS3}}$ - X-Bus (**PC87416 and PC87417**)
2	**XCS2MUX ($\overline{\text{XCS2}}$ Multiplex Control).** Selects the function connected to pin 21. 0: GPIOE41 port - GPIO (default) 1: $\overline{\text{XCS2}}$ - X-Bus (**PC87416 and PC87417**)
1	**XCS1MUX ($\overline{\text{XCS1}}$ Multiplex Control).** Selects the function connected to pin 22. 0: GPIO26 port - GPIO (default) 1: $\overline{\text{XCS1}}$ - X-Bus (**PC87416 and PC87417**)
0	**XCS0MUX ($\overline{\text{XCS0}}$ Multiplex Control).** Selects the function connected to pin 23. The default value is set to 0 if XCNF2 = 1 or to 1 if XCNF2 = 0. The XCNF2 strap is sampled at V_{SB} Power-Up reset. 0: $\overline{\text{XCS0}}$ - X-Bus (**PC87416 and PC87417**) 1: GPIO27 port - GPIO

3.0 Device Architecture and Configuration (Continued)

3.7.7 ServerI/O Configuration 6 Register (SIOCF6)

This register provides a fast way to disable one or more modules, without having to access the Activate register of each (see Section 3.3.1 on page 43).

Power Well: V_{SB}

Location: Index 26h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKFDS**	**General-Purpose Scratch**		**Reserved**	**SER1DIS**	**SER2DIS**	**PARPDIS**	**FDCDIS**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W1S	**LOCKFDS (Lock Fast Disable Configuration).** When set to 1, this bit locks itself, the SER1DIS, SER2DIS, PARPDIS and FDCDIS bits in this register and the GLOBEN bit in the SIOCF1 register by disabling writing to all these bits. Once set, this bit can be cleared either by V_{DD} Power-Up reset (or Hardware reset) or by V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKF bit in the ACBLKCTL register (**PC87413 and PC87417**). 0: R/W bits are enabled for write (default) 1: All bits are RO
6-5	R/W	**General-Purpose Scratch.**
4	-	**Reserved.**
3	R/W or RO	**SER1DIS (Serial Port 1 Disable).** When set to 1, this bit forces the Serial Port 1 module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
2	R/W or RO	**SER2DIS (Serial Port 2 Disable).** When set to 1, this bit forces the Serial Port 2 module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
1	R/W or RO	**PARPDIS (Parallel Port Disable).** When set to 1, this bit forces the Parallel Port module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
0	R/W or RO	**FDCDIS (Floppy Disk Controller Disable).** When set to 1, this bit forces the Floppy Disk Controller module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled

3.0 Device Architecture and Configuration (Continued)

3.7.8 ServerI/O Revision ID Register (SRID)

This register contains the ID number of the specific family member (Chip ID) and the chip revision number (Chip Rev).

Power Well:V_{SB}

Location:Index 27h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name		**Chip ID (N/A)**				**Chip Rev**		
Reset	X	X	X	X	X	X	X	X

Bit	Description
7-5	**Chip ID (N/A).** These bits identify a specific device of a family. Note: Not applicable for the PC8741x family
4-0	**Chip Rev.** These bits identify the device revision. The value is incremented on each revision.

3.7.9 ServerI/O Configuration 8 Register (SIOCF8)

Power Well:V_{SB}

Location:Index 28h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name		**Reserved**		**MIRQ2SMI**	**KIRQ2SMI**	**KBCP12SMI**	**GPIO2SMI**	**Reserved**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4	**MIRQ2SMI (Mouse IRQ to SMI Enable).** Controls the routing of the Mouse interrupt to the $\overline{\text{SIOSMI}}$ pin. 0: Disabled (default) 1: Enabled
3	**KIRQ2SMI (Keyboard IRQ to SMI Enable).** Controls the routing of the Keyboard interrupt to the $\overline{\text{SIOSMI}}$ pin. 0: Disabled (default) 1: Enabled
2	**KBCP12SMI (KBC P12 to SMI Enable).** Controls the routing of the P12 port of the KBC to the $\overline{\text{SIOSMI}}$ pin. 0: Disabled (default) 1: Enabled
1	**GPIO2SMI (GPIO IRQ to SMI Enable).** Controls the routing of the GPIO event (see Section 7.3.2 on page 138) to the $\overline{\text{SIOSMI}}$ pin. 0: Disabled (default) 1: Enabled
0	**Reserved.**

3.0 Device Architecture and Configuration (Continued)

3.7.10 Clock Generator Configuration Register (CLOCKCF)

Power Well:V_{SB}

Location:Index 29h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKCCF**	**LFCKSEL**	**HFCKDIS**	**CKVALID**	**CKIN48**	**HFCKDIV**		
Reset	0	0	0	0	Strap	0	0	See Table

Bit	Type	Description
7	R/W1S	**LOCKCCF (Lock Clock Configuration).** When set to 1, this bit locks the configuration register CLOCKCF by disabling writing to all its bits (including to the LOCKCCF bit itself). Once set, this bit can be cleared either by V_{DD} Power-Up reset (or Hardware reset) or by V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKC bit in the ACBLKCTL register (**PC87413 and PC87417**). 0: R/W bits are enabled for write (default) 1: All bits are RO
6	R/W or RO	**LFCKSEL (Low Frequency Clock Select).** Selects the frequency generated at the LFCKOUT pin. 0: 32.768 KHz (default) 1: 1 Hz
5	R/W or RO	**HFCKDIS (High Frequency Clock Disable).** Disables both the HFCKOUT output and the programmable divider to save power. 0: Enabled (default) 1: Disabled (set low)
4	RO	**CKVALID (Valid Multiplier Clock Status).** This bit indicates the status of output from the Frequency Multiplier (the internal clock signal). 0: Internal clock frozen (default) 1: Internal clock active (stable and toggling)
3	RO	**CKIN48 (Clock Input Available).** This bit indicates the value of the CKIN48 strap input, sampled at V_{SB} Power-Up reset. 0: No clock is available at the CLKIN pin (pin 56 connected to GPIO55) 1: A 48 MHz clock is available at the CLKIN pin (pin 56 connected to CLKIN)
2-0	R/W or RO	**HFCKDIV (High Frequency Clock Divisor).** These bits define the value by which the 48 MHz or 40 MHz internal clock frequency is divided to generate the HFCKOUT signal. The resulting frequency depends on the value of the CKIN48 bit (see Table 7 on page 37). **Bits** **2 1 0 Function** 0 0 0: Divide by 1 (default for CKIN48 = 1) 0 0 1: Divide by 2 (default for CKIN48 = 0) 0 1 0: Divide by 3 0 1 1: Divide by 4 1 0 0: Divide by 6 1 0 1: Divide by 8 1 1 0: Divide by 12 1 1 1: Divide by 16

3.0 Device Architecture and Configuration (Continued)

3.7.11 ACCESS.bus Configuration (ACBCF) Register

This register is relevant only for the PC87413 and PC87417. In the PC87414 and PC87416, all bits are held at their default value.

This register may be written only once. All eight bits must be updated in a single write operation, after which the data in the register becomes read only. The register is cleared and the write-lock released only by V_{PP} Power-Up reset.

Power Well:V_{PP}

Location:Index 2Ah

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**ACBPUEN**	**ACBSADD**						
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**ACBPUEN (ACCESS.bus Signals Pull-Up Enable).** This bit controls the internal pull-up resistors connected to the ACBCLK and ACBDAT signals (see Section 1.5 on page 30). 0: Disconnected (default) 1: Connected
6-0	**ACBSADD (ACCESS.bus Slave Address).** This field defines the slave address on the ACCESS.bus for the PC8741x devices. This address, once programmed by the host, is preserved as long as the V_{PP} power is active (V_{SB} or V_{BAT}). The 7-bit slave address is used to access the PC8741x devices (see Section 6.2.6 on page 119). A non-zero value read from this field indicates that ACBSADD contains a valid slave address.

3.0 Device Architecture and Configuration (Continued)

3.8 FLOPPY DISK CONTROLLER (FDC) CONFIGURATION

3.8.1 General Description

The generic FDC is a standard FDC with a digital data separator and is DP8473 and N82077 software compatible. The PC8741x FDC supports 14 of the 17 standard FDC signals described in the generic Floppy Disk Controller (FDC) chapter, including (see Section 10.1 on page 220):

- FM and MFM modes are supported. To select either mode, set bit 6 of the first command byte when writing to/reading from a diskette, where:
  0 = FM mode
  1 = MFM mode
- A logic 1 is returned during LPC I/O read cycles by all register bits reflecting the state of floating (TRI-STATE) FDC pins.

Exceptions to standard FDC are:

- Automatic media sense using the MSEN1 signal is not supported
- DRATE1 is not supported.

The FDC functional block registers are shown in Section 10.1 on page 220. All these registers are V_{DD} powered.

3.8.2 Logical Device 0 (FDC) Configuration

Table 17 lists the configuration registers that affect the FDC. Only the last two registers (F0h and F1h) are described here. See Section 3.2.3 on page 40 for descriptions of the other configuration registers. All these registers are V_{DD} powered.

Table 17. FDC Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 43).	R/W	V_{DD}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	V_{DD}	03h
61h	Base Address LSB register. Bits 2 and 0 (for A2 and A0) are read only, 00b.	R/W	V_{DD}	F2h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD}	06h
71h	Interrupt Type. Bit 1 is read/write; other bits are read only.	R/W	V_{DD}	03h
74h	DMA Channel Select.	R/W	V_{DD}	02h
75h	Report no second DMA assignment.	RO	V_{DD}	04h
F0h	FDC Configuration register.	R/W	V_{DD}	24h
F1h	Drive ID register.	R/W	V_{DD}	00h

3.0 Device Architecture and Configuration (Continued)

3.8.3 FDC Configuration Register

This register is reset by hardware to 24h.

Power Well:V_{DD}

Location:Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Four-Drive Encode Enable**	**TDR Register Mode**	**DENSEL Polarity Control**	**FDC 2Mbps Enable**	**Write Protect**	**PC-AT or PS/2 Drive Mode Select**	**Reserved**	**TRI-STATE Control**
Reset	0	0	1	0	0	1	0	0

Bit	Description
7	**Four-Drive Encode Enable.** 0: Two floppy drives are directly controlled by $\overline{\text{DR1-0}}$, $\overline{\text{MTR1-0}}$ (default) 1: Four floppy drives are controlled with the aid of an external decoder
6	**TDR Register Mode.** 0: PC-AT-Compatible Drive mode; i.e., bits 7-2 of the TDR are 111111b (default) 1: Enhanced Drive mode
5	**DENSEL Polarity Control.** 0: Active low for 500 Kbps or 1 or 2 Mbps data rates 1: Active high for 500 Kbps or 1 or 2 Mbps data rates (default)
4	**FDC 2Mbps Enable.** This bit is set only when a 2 Mbps drive is used. 0: 2 Mbps disabled and the FDC clock is 24 MHz (default) 1: 2 Mbps enabled and the FDC clock is 48 MHz
3	**Write Protect.** This bit enables forcing of write protect functionality by software. When set, writes to the floppy disk drive are disabled. This effect is identical to an active $\overline{\text{WP}}$ signal. 0: Write protected according to $\overline{\text{WP}}$ signal (default) 1: Write protected regardless of value of $\overline{\text{WP}}$ signal
2	**PC-AT or PS/2 Drive Mode Select.** 0: PS/2 Drive mode 1: PC-AT Drive mode (default)
1	**Reserved.**
0	**TRI-STATE Control.** When enabled and the device is inactive (see Section 3.3.1 on page 43), the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

3.0 Device Architecture and Configuration (Continued)

3.8.4 Drive ID Register

This register is reset by hardware to 00h. This register controls bits 5 and 4 of the TDR register in Enhanced mode.

Power Well:V_{DD}
Location:Index F1h
Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**Drive 1 ID**		**Drive 0 ID**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3-2	**Drive 1 ID.** When drive 1 is accessed, these bits are reflected on bits 5-4 of the TDR register, respectively.
1-0	**Drive 0 ID.** When drive 0 is accessed, these bits are reflected on bits 5-4 of the TDR register, respectively.

Usage Hints: Some BIOS implementations support automatic media sense FDDs, in which case bit 5 of the TDR register in the Enhanced mode is interpreted as valid media sense when it is cleared to 0. If drive 0 and/or drive 1 do not support automatic media sense, bits 1 and/or 3 of the Drive ID register must be set to 1 (to indicate non-valid media sense). When Drive 0 or Drive 1 is selected, the Drive ID bit is reflected on bit 5 of the TDR register in Enhanced mode.

3.0 Device Architecture and Configuration (Continued)

3.9 PARALLEL PORT (PP) CONFIGURATION

3.9.1 General Description

The PC8741x Parallel Port supports all IEEE1284 standard communication modes: Compatibility (also known as Standard or SPP), Bidirectional (known also as PS/2), FIFO, EPP (also known as mode 4) and ECP (with an optional Extended ECP mode).

The Parallel Port includes two groups of runtime registers, as follows (see Section 10.2 on page 222):

- A group of 21 registers at first level offset, sharing 14 entries. Three of this registers (at offsets 403h, 404h and 405h) are used only in the Extended ECP mode.
- A group of four registers, used only in the Extended ECP mode, accessed by a second level offset.

The desired mode is selected by the ECR runtime register (offset 402h). The selected mode determines which runtime registers are used and which address bits are used for the base address. The FDC functional block registers are shown in Section 10.2 on page 222. All these registers are V_{DD} powered.

3.9.2 Logical Device 1 (PP) Configuration

Table 18 lists the configuration registers that affect the Parallel Port. Only the last register (F0h) is described here. See Section 3.2.3 on page 40 for descriptions of the other configuration registers. All these registers are V_{DD} powered.

Table 18. Parallel Port Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 43).	R/W	V_{DD}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b. Bit 2 (for A10) must be 0b.	R/W	V_{DD}	02h
61h	Base Address LSB register. Bits 1 and 0 (A1 and A0) are read only, 00b. For ECP mode 4 (EPP) or when using the Extended registers, bit 2 (A2) must also be 0b.	R/W	V_{DD}	78h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD}	07h
71h	Interrupt Type: Bits 7-2 are read only. Bit 1 is a read/write bit. Bit 0 is read only. It reflects the interrupt type dictated by the Parallel Port operation mode. This bit is set to 1 (level interrupt) in Extended mode and cleared (edge interrupt) in all other modes.	R/W	V_{DD}	02h
74h	DMA Channel Select.	R/W	V_{DD}	04h
75h	Report no second DMA assignment.	RO	V_{DD}	04h
F0h	Parallel Port Configuration register.	R/W	V_{DD}	F2h

3.0 Device Architecture and Configuration (Continued)

3.9.3 Parallel Port Configuration Register

This register is reset by hardware to F2h.

Power Well:V_{DD}

Location:Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Parallel Port Mode Select**			**Extended Register Access**	**Reserved**		**Power Mode Control**	**TRI-STATE Control**
Reset	1	1	1	1	0	0	1	0

Bit	Description
7-5	**Parallel Port Mode Select.** 000: SPP-Compatible mode. PD7-0 are always output signals 001: SPP Extended mode. PD7-0 direction is controlled by software 010: EPP 1.7 mode 011: EPP 1.9 mode 100: ECP mode (IEEE1284 register set), with no support for EPP mode 101: Reserved 110: Reserved 111: ECP mode (IEEE1284 register set), with EPP mode selectable as mode 4 (default) Selection of EPP 1.7 or 1.9 in ECP mode 4 is controlled by bit 4 of the Control2 configuration register of the parallel port at offset 02h. **Note**: Before setting bits 7-5, enable the parallel port and set CTR/DCR (at base address + 2) to C4h.
4	**Extended Register Access.** 0: Registers at base (address) + 403h, base + 404h and base + 405h are not accessible (reads and writes are ignored) 1: Registers at base (address) + 403h, base + 404h and base + 405h are accessible. This option supports run-time configuration within the Parallel Port address space (default).
3-2	**Reserved.**
1	**Power Mode Control.** When the logical device is active: 0: Parallel port clock disabled. ECP modes and EPP time-out are not functional when the logical device is active. Registers are maintained. 1: Parallel port clock enabled. All operation modes are functional when the logical device is active (default).
0	**TRI-STATE Control.** When enabled and the device is inactive (see Section 3.3.1 on page 43), the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

3.0 Device Architecture and Configuration (Continued)

3.10 SERIAL PORT 2 CONFIGURATION

3.10.1 General Description

Serial Port 2 provides UART functionality by supporting serial data communication with remote peripheral device or modem. The functional blocks can function as a standard 16450 or 16550 or as an Extended UART.

Serial Port 2 includes four register banks, each containing eight runtime registers, as shown in Section 10.3 on page 225. All these registers are V_{DD} powered.

3.10.2 Logical Device 2 (SP2) Configuration

Table 19 lists the configuration registers that affect Serial Port 2. Only the last register (F0h) is described here. See Section 3.2.3 on page 40 for descriptions of the other configuration registers. All these registers are V_{DD} powered.

Table 19. Serial Port 2 Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 43).	R/W	V_{DD}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	V_{DD}	02h
61h	Base Address LSB register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	V_{DD}	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD}	03h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	V_{DD}	03h
74h	Report no DMA Assignment.	RO	V_{DD}	04h
75h	Report no DMA Assignment.	RO	V_{DD}	04h
F0h	Serial Port 2 Configuration register.	R/W	V_{DD}	02h

3.0 Device Architecture and Configuration (Continued)

3.10.3 Serial Port 2 Configuration Register

This register is reset by hardware to 02h.

Power Well:V_{DD}

Location:Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Fast TRI-STATE**	**Reserved**			**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable.** Enables bank switching for Serial Port 2. 0: All attempts to access the extended registers in Serial Port 2 are ignored (default) 1: Enables bank switching for Serial Port 2
6	**Fast TRI-STATE.** When set, the logical device output pins are in TRI-STATE and the input pins are internally held at inactive level (high), regardless of the device activation (Activation bit - Section 3.3.1 on page 43; SER2DIS - Section 3.7.7 on page 54; GLOBEN - Section 3.7.2 on page 49; SER2DIS - Section 9.3.8 on page 185; SER2ALOK - Section 6.3.7 on page 132; SER2DIS - Section 6.3.5 on page 130). 0: Device pins active (default) 1: Device pins disabled
5-3	**Reserved.**
2	**Busy Indicator.** This read only bit can be used by power management software to decide when to power-down the Serial Port 2 logical device. 0: No transfer in progress (default) 1: Transfer in progress
1	**Power Mode Control.** When the logical device is active in: 0: Low-Power mode Serial Port 2 clock disabled. The output signals are set to their default states. The $\overline{RI}$ input signal can be programmed to generate an interrupt. Registers are maintained (unlike Active bit in index 30 that also prevents access to Serial Port 2 registers). 1: Normal Power mode Serial Port 2 clock enabled. Serial Port 2 is functional when the logical device is active (default).
0	**TRI-STATE Control.** When enabled and the device is inactive (see Section 3.3.1 on page 43), the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

3.0 Device Architecture and Configuration (Continued)

3.11 SERIAL PORT 1 CONFIGURATION

3.11.1 General Description

Serial Port 1 provides UART functionality by supporting serial data communication with remote peripheral device or modem. The functional blocks can function as a standard 16450 or 16550 or as an Extended UART.

Serial Port 1 includes the same register banks and runtime registers as Serial Port 2 (see Section 10.3 on page 225). All the registers are V_{DD} powered.

3.11.2 Logical Device 3 (SP1) Configuration

Table 20 lists the configuration registers that affect Serial Port 1. Only the last register (F0h) is described here. See Section 3.2.3 on page 40 for descriptions of the other configuration registers. All these registers are V_{DD} powered.

Table 20. Serial Port 1 Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 43).	R/W	V_{DD}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	V_{DD}	03h
61h	Base Address LSB register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	V_{DD}	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD}	04h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	V_{DD}	03h
74h	Report no DMA Assignment.	RO	V_{DD}	04h
75h	Report no DMA Assignment.	RO	V_{DD}	04h
F0h	Serial Port 1 Configuration register.	R/W	V_{DD}	02h

3.0 Device Architecture and Configuration (Continued)

3.11.3 Serial Port 1 Configuration Register

This register is reset by hardware to 02h.

Power Well:V_{DD}

Location:Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Fast TRI-STATE**	**Reserved**			**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable.** Enables bank switching for Serial Port 1. 0: All attempts to access the extended registers in Serial Port 1 are ignored (default) 1: Enables bank switching for Serial Port 1
6	**Fast TRI-STATE.** When set, the logical device output pins are in TRI-STATE and the input pins are internally held at inactive level (high), regardless of the device activation (Activation bit - Section 3.3.1 on page 43; SER1DIS - Section 3.7.7 on page 54; GLOBEN - Section 3.7.2 on page 49; SER1DIS - Section 9.3.8 on page 185; SER1ALOK - Section 6.3.7 on page 132; SER1DIS - Section 6.3.5 on page 130). 0: Device pins active (default) 1: Device pins disabled
5-3	**Reserved.**
2	**Busy Indicator.** This read only bit can be used by power management software to decide when to power-down the Serial Port 1 logical device. 0: No transfer in progress (default) 1: Transfer in progress
1	**Power Mode Control.** When the logical device is active in: 0: Low-Power mode Serial Port 1 clock disabled. The output signals are set to their default states. The $\overline{RI}$ input signal can be programmed to generate an interrupt. Registers are maintained (unlike Active bit in Index 30;s which also prevents access to Serial Port 1 registers). 1: Normal Power mode Serial Port 1 clock enabled. Serial Port 1 is functional when the logical device is active (default).
0	**TRI-STATE Control.** When enabled and the device is inactive (see Section 3.3.1 on page 43), the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

3.0 Device Architecture and Configuration (Continued)

3.12 SYSTEM WAKE-UP CONTROL (SWC) CONFIGURATION

3.12.1 General Description

System Wake-up Control provides wake-up and power management functionality according to ACPI specification (see Section 9.1 on page 161). Its registers are V_{PP} or V_{SB} powered.

3.12.2 Logical Device 4 (SWC) Configuration

Table 21 lists the configuration registers that affect the SWC. See Section 3.2.3 on page 40 for a detailed description of these registers. All these registers are V_{DD} powered.

Table 21. System Wake-Up Control (SWC) Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate. When bit 0 is cleared, the runtime registers of this logical device are not accessible (see Section 3.3.1 on page 43).[1]	R/W	V_{DD}	00h
60h	SWC Base Address MSB register.	R/W	V_{DD}	00h
61h	SWC Base Address LSB register. Bits 4-0 (for A4-0) are read only, 00000b.	R/W	V_{DD}	00h
62h	PM1b_EVT_BLK Base Address MSB register.	R/W	V_{DD}	00h
63h	PM1b_EVT_BLK Base Address LSB register. Bits 1-0 (for A1-0) are read only, 00b.	R/W	V_{DD}	00h
64h	PM1b_CNT_BLK Base Address MSB register.	R/W	V_{DD}	00h
65h	PM1b_CNT_BLK Base Address LSB register. Bits 1-0 (for A1-0) are read only, 00b.	R/W	V_{DD}	00h
66h	GPE1_BLK Base Address MSB register.	R/W	V_{DD}	00h
67h	GPE1_BLK Base Address LSB register. Bits 2-0 (for A2-0) are read only, 000b.	R/W	V_{DD}	00h
70h	Interrupt Number.	R/W	V_{DD}	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	V_{DD}	03h
74h	Report no DMA assignment.	RO	V_{DD}	04h
75h	Report no DMA assignment.	RO	V_{DD}	04h

1. The logical device runtime registers are maintained and all wake-up detection mechanisms are functional.

3.0 Device Architecture and Configuration (Continued)

3.13 KEYBOARD AND MOUSE CONTROLLER (KBC) CONFIGURATION

3.13.1 General Description

The KBC is implemented physically as a single hardware module and houses two separate logical devices: a Mouse controller (Logical Device 5) and a Keyboard controller (Logical Device 6). The KBC is functionally equivalent to the industry standard 8042A Keyboard controller. Technical references for the standard 8042A Keyboard Controller may serve as detailed technical references for the KBC.

The Keyboard and Mouse Controller runtime registers are described in Section 10.4 on page 229. All the registers are V_{DD} powered.

3.13.2 Logical Devices 5 and 6 (Mouse and Keyboard) Configuration

Tables 22 and 23 list the configuration registers that affect the Mouse and the Keyboard logical devices, respectively. Only the last register (F0h) is described here. See Section 3.2.3 on page 40 for descriptions of the other configuration registers. All these registers are V_{DD} powered.

Table 22. Mouse Configuration Registers

Index	Mouse Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.2.3 on page 40). When the Mouse of the KBC is inactive, the IRQ selected by the Mouse Interrupt Number and Wake-Up on IRQ Enable register (index 70h) are not asserted. This register has no effect on host KBC commands handling the PS/2 Mouse.	R/W	V_{DD}	00h
70h	Mouse Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD}	0Ch
71h	Mouse Interrupt Type. Bits 1,0 are read/write; other bits are read only.	R/W	V_{DD}	02h
74h	Report no DMA assignment.	RO	V_{DD}	04h
75h	Report no DMA assignment.	RO	V_{DD}	04h

Table 23. Keyboard Configuration Registers

Index	Keyboard Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.2.3 on page 40). When the Keyboard of the KBC is inactive, the IRQ selected by the Keyboard Interrupt Number and Wake-Up on IRQ Enable register (index 70h) are not asserted.	R/W	V_{DD}	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	V_{DD}	00h
61h	Base Address LSB register. Bits 2-0 (for A2-0) are read-only 000b.	R/W	V_{DD}	60h
62h	Command Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	V_{DD}	00h
63h	Command Base Address LSB. Bits 2-0 (for A2-0) are read-only 100b.	R/W	V_{DD}	64h
70h	KBD Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD}	01h
71h	KBD Interrupt Type. Bits 1,0 are read/write; others are read only.	R/W	V_{DD}	02h
74h	Report no DMA assignment.	RO	V_{DD}	04h
75h	Report no DMA assignment.	RO	V_{DD}	04h
F0h	KBC Configuration register.	R/W	V_{DD}	40h

3.0 Device Architecture and Configuration (Continued)

3.13.3 KBC Configuration Register

This register is reset by hardware to 40h.

Power Well:V_{DD}

Location:Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**KBC Clock Source**		**Reserved**		**Swap**	**Reserved**		**TRI-STATE Control**
Reset	0	1	0	0	0	0	0	0
Required						0		

Bit	Description
7-6	**KBC Clock Source.** The clock source can be changed only when the KBC is inactive (disabled). **Bits** **7 6 Source** 0 0: 8 MHz 0 1: 12 MHz (default) 1 0: 16 MHz 1 1: Reserved
5-4	**Reserved.**
3	**Swap.** This bit swaps between the Keyboard and Mouse Interface pins. 0: KBCLK and KBDAT are Keyboard Interface; MCLK and MDAT are Mouse Interface (default) 1: KBCLK and KBDAT are Mouse Interface; MCLK and MDAT are Keyboard Interface
2-1	**Reserved.**
0	**TRI-STATE Control.** If the keyboard is inactive (see Section 3.3.1 on page 43) when this bit is set, the KBD pins (KBCLK and KBDAT) are in TRI-STATE. If the mouse is inactive (see Section 3.3.1 on page 43) when this bit is set, the mouse pins (MCLK and MDAT) are in TRI-STATE. 0: Disabled (default) 1: Enabled

Usage Hints:

1. To change the clock frequency of the KBC:
   a. Disable the KBC logical devices.
   b. Change the frequency setting.
   c. Enable the KBC logical devices.
2. Before swapping between the Keyboard and Mouse Interface pins, disable the KBC logical devices and both pin sets. After swapping, the software must issue a synchronization command to the Keyboard and Mouse through the KBC to regain synchronization with these devices.

3.0 Device Architecture and Configuration (Continued)

3.14 GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORTS CONFIGURATION

3.14.1 General Description

The GPIO functional block includes 51 pins arranged in seven ports:

- Ports 1 and 4 contain eight GPIOE pins each.
- Ports 0, 2 and 3 contain eight GPIO pins each.
- Port 5 contains six GPIO pins.
- Port 6 contains five GPO pins (see Section 1.4.8 on page 27).

All the pins of Ports 1 and 4 and have full event detection capability (see Section 1.3 on page 20), enabling them to trigger the assertion of IRQ or $\overline{\text{SIOSMI}}$ signals. In addition, through the SWC functional block, the pins of Ports 1 and 4 can trigger the $\overline{\text{SIOSCI}}$, control the $\overline{\text{ONCTL}}$ signal or enable the generation of a pulse in the $\overline{\text{PWBTOUT}}$ signal. The pins of Ports 0-5 are I/O, however the five pins of Port 6 are output only.

All 51 GPIO pins are powered from the V_{SB} well. The 17 runtime registers associated with the seven ports are arranged in the GPIO address space as shown in Table 24. The GPIO ports with wake-up event detection capability (such as Ports 1 and 4) have four runtime registers; the other ports have only 2. Port 6 contains only GPO pins and therefore has only one runtime register. The GPIO base address is 32-byte aligned. Address bits 4-0 are used to indicate the register offset.

The specific runtime registers implemented in the PC8741x devices are shown in Table 24. All these registers are V_{SB} powered.

Table 24. Runtime Registers in GPIO Address Space

Offset	Mnemonic	Register Name	Port	Power Well	Type
00h	GPDO0	GPIO Data Out 0	0	V_{SB}	R/W
01h	GPDI0	GPIO Data In 0		V_{SB}	RO
02h	GPDO1	GPIO Data Out 1	1	V_{SB}	R/W
03h	GPDI1	GPIO Data In 1		V_{SB}	RO
04h	GPEVEN1	GPIO Event Enable 1		V_{SB}	R/W
05h	GPEVST1	GPIO Event Status 1		V_{SB}	R/W1C
06h	GPDO2	GPIO Data Out 2	2	V_{SB}	R/W
07h	GPDI2	GPIO Data In 2		V_{SB}	RO
08h	GPDO3	GPIO Data Out 3	3	V_{SB}	R/W
09h	GPDI3	GPIO Data In 3		V_{SB}	RO
0Ah	GPDO4	GPIO Data Out 4	4	V_{SB}	R/W
0Bh	GPDI4	GPIO Data In 4		V_{SB}	RO
0Ch	GPEVEN4	GPIO Event Enable 4		V_{SB}	R/W
0Dh	GPEVST4	GPIO Event Status 4		V_{SB}	R/W1C
0Eh	GPDO5	GPIO Data Out 5	5	V_{SB}	R/W
0Fh	GPDI5	GPIO Data In 5		V_{SB}	RO
10h	GPDO6	GPIO Data Out 6	6	V_{SB}	R/W

3.0 Device Architecture and Configuration (Continued)

3.14.2 Logical Device 7 (GPIO) Configuration

Table 25 lists the configuration registers that affect the GPIO. Only the last three registers (F0h - F2h) are described here. See Section 3.2.3 on page 40 for a detailed description of the other configuration registers. The standard configuration registers are powered by V_{DD}, however the specific configuration registers are powered by V_{SB}.

Table 25. GPIO Configuration Register

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.2.3 on page 40).	R/W	V_{DD}	00h
60h	Base Address MSB register.	R/W	V_{DD}	00h
61h	Base Address LSB register. Bits 4-0 (for A4-0) are read-only 00000b.	R/W	V_{DD}	00h
70h	Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD}	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	V_{DD}	03h
74h	Report no DMA assignment.	RO	V_{DD}	04h
75h	Report no DMA assignment.	RO	V_{DD}	04h
F0h	GPIO Pin Select register (GPSEL).	R/W	V_{SB}	00h
F1h	GPIO Pin Configuration register 1 (GPCFG1).	R/W	V_{SB}	See text
F2h	GPIO Pin Event Routing register (GPEVR).	R/W	V_{SB}	01h
F3h	GPIO Pin Configuration register 2 (GPCFG2).	R/W	V_{SB}	00h

Figure 6 shows the organization of these registers:

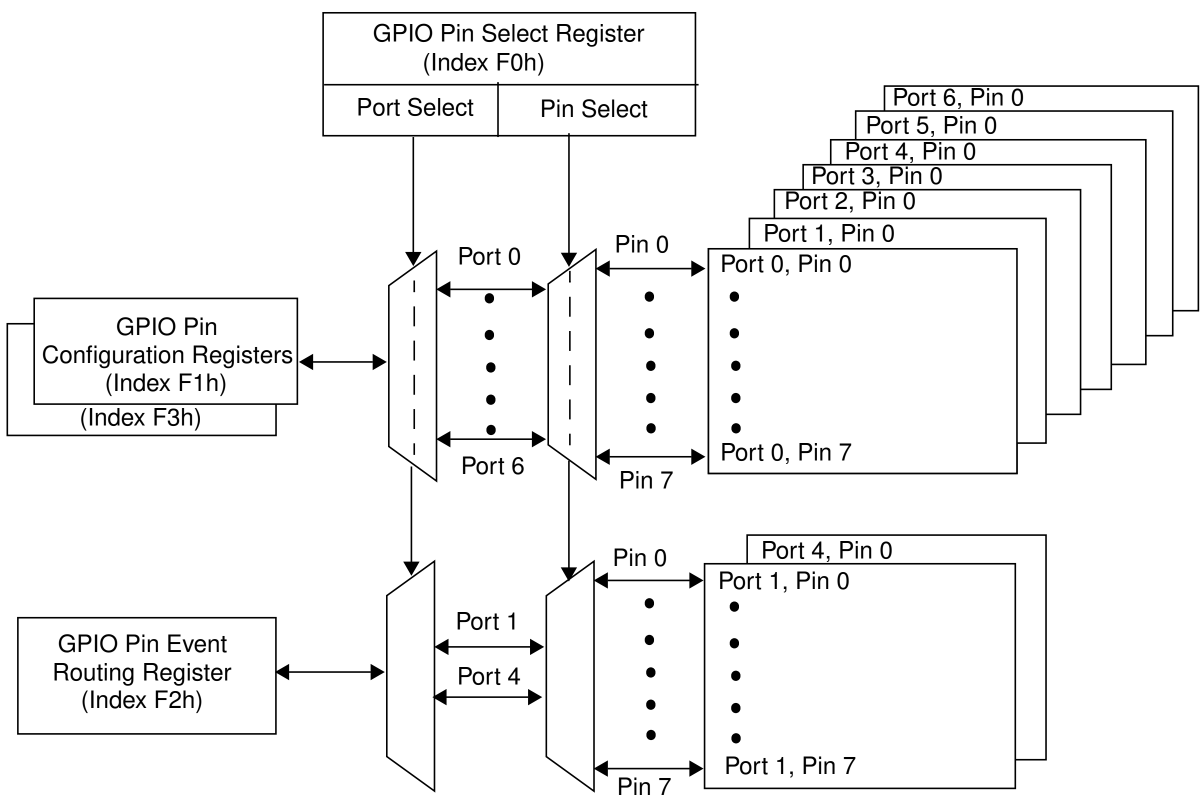


Figure 6. Organization of GPIO Pin Registers

3.0 Device Architecture and Configuration (Continued)

3.14.3 GPIO Pin Select Register (GPSEL)

This register selects the GPIO pin (port number and bit number) to be configured (i.e., which register is accessed via the GPIO configuration registers). Since access to the pin configuration requires two transactions (first to GPSEL, then to the configuration register) and since the LPC bus and ACCESS.bus concurrently access the module (**PC87413 and PC87417**), the GPSEL register is duplicated (one GPSEL register is accessed by the host and one by the ACCESS.bus). This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**PORTSEL**			**Reserved**	**PINSEL**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
5-4	**PORTSEL (Port Select).** These bits select the GPIO port to be configured: 000: Port 0 (default) 001 to 110: Binary value of port numbers 1-6, respectively (all other values are reserved)
3	**Reserved.**
2-0	**PINSEL (Pin Select).** These bits select the GPIO pin of the selected port, to be configured: 000: Pin 0 (default) 001 to 111: Binary value of pin number 1-7, respectively

3.14.4 GPIO Pin Configuration Register 1 (GPCFG1)

This register reflects, for both read and write, the register currently selected by the GPIO Pin Select register. All the GPIO Pin Configuration registers have a common bit structure, as shown below. Ports 1 and 4 are reset by hardware to 01000X00b. Ports 0, 2, 3, 5 and 6 are reset to 00000X00b (see Table 26 on page 73 for the value of ‘X’).

Power Well:V_{SB}

Location:Index F1h

Type: Varies per bit

Ports 1 and 4 (With Wake-Up Event Detection Capability)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**EVDBNC**	**EVPOL**	**EVTYPE**	**LOCKCFP**	**PUPCTL**	**OUTTYPE**	**OUTENA**
Reset	0	1	0	0	0	see Table 26	0	0

Ports 0, 2, 3, 5 and 6 (Without Wake-Up Event Detection Capability)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**LOCKCFP**	**PUPCTL**	**OUTTYPE**	**OUTENA**
Reset	0	0	0	0	0	see Table 26	0	0

3.0 Device Architecture and Configuration (Continued)

Bit	Type	Description
7	-	**Reserved (note that for Ports 0, 2, 3, 5, and 6, bits 7-4 are reserved).**
6	- R/W	**Reserved for Ports 0, 2, 3, 5, and 6.** **For Ports 1 and 4: EVDBNC (Event Debounce Enable).** This bit enables the debounce circuit in the event input path of the selected GPIO pin. The event is detected after a predetermined debouncing period of time (see Section 7.3 on page 137). 0: Disabled 1: Enabled (default)
5	- R/W	**Reserved for Ports 0, 2, 3, 5, and 6.** **For Ports 1 and 4: EVPOL (Event Polarity).** This bit defines the polarity of the wake-up signal that issues an event from the selected GPIO pin (see Section 7.3 on page 137). 0: Falling edge or low level input (default) 1: Rising edge or high level input
4	- R/W	**Reserved for Ports 0, 2, 3, 5, and 6.** **For Ports 1 and 4: EVTYPE (Event Type).** This bit defines the type of the wake-up signal that issues an event from the selected GPIO pin (see Section 7.3 on page 137). 0: Edge input (default) 1: Level input
3	R/W1S	**LOCKCFP (Lock Configuration of Pin).** When set to 1, this bit locks the GPIO pin configuration and data (see also Section 7.4 on page 139) by disabling writing to itself, to GPCFG1 register bits PUPCTL, OUTTYPE and OUTENA, to all the bits of the GPCFG2 register and to the corresponding bit in the GPDO register. Once set, this bit can be cleared by V_{DD} Power-Up reset (or Hardware reset) or by V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKG bit in the ACBLKCTL register (**PC87413 and PC87417**). 0: R/W bits are enabled for write (default) 1: All bits are RO
2	R/W or RO	**PUPCTL (Pull-Up Control).** This bit controls the internal pull-up resistor of the selected GPIO pin (see Section 7.2 on page 136). 0: Disabled (for default value, see Table 26) 1: Enabled (for default value, see Table 26)
1	R/W or RO	**OUTTYPE (Output Type).** This bit controls the output buffer type of the selected GPIO pin (see Section 7.2 on page 136). 0: Open-drain (default) 1: Push-pull
0	R/W or RO	**OUTENA (Output Enable).** This bit controls the output buffer of the selected GPIO pin (see Section 7.2 on page 136). 0: TRI-STATE (default) 1: Output buffer enabled

Table 26. Reset Values for PUPCTL Bit

GP(I)O(E)*nn*	00-07,10-17	20,21	22-25	26,27,30-37,40-42	43-47,50	51-53	54,55,60-63	64[1]
PUPCTL	0	1	0	1	0	1	0	1

1. The pull-up resistor is disabled during V_{SB} Power-Up reset.

3.0 Device Architecture and Configuration (Continued)

3.14.5 GPIO Event Routing Register (GPEVR)

This register enables the routing of the GPIO event (see Section 7.3.2 on page 138) to IRQ and/or $\overline{\text{SIOSMI}}$ signals. It is implemented only for Ports 1 and 4, which have wake-up event detection capability. This register is reset by hardware to 01h.

Power Well:V_{SB}

Location:Index F2h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**EV2SMI**	**EV2IRQ**
Reset	0	0	0	0	0	0	0	1

Bit	Description
7-2	**Reserved.**
1	**EV2SMI (Event to SMI Routing).** Controls the routing of the event from the selected GPIO pin to $\overline{\text{SIOSMI}}$ (see Section 7.3 on page 137). 0: Disabled (default) 1: Enabled
0	**EV2IRQ (Event to IRQ Routing).** Controls the routing of the event from the selected GPIO pin to IRQ (see Section 7.3 on page 137). 0: Disabled 1: Enabled (default)

3.14.6 GPIO Pin Configuration Register 2 (GPCFG2)

This register controls the access to the GPIO pin from one of the two buses. This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F3h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**BUSCTL**		**VDDLOAD**	**Reserved**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
6-5	**BUSCTL (Bus Control).** These bits select the bus (ACCESS.bus or LPC bus) that controls the configuration and data of the selected GPIO pin. The bus not selected has read-only access to the GPCFG1, GPCFG2 and GPEVR registers and to the corresponding bit in the GPDO, GPEVEN and GPEVST registers (see Section 7.4.2 on page 140). In the **PC87414 and PC87416**, these bits are irrelevant because only the LPC bus is available. **Bits** **6 5 Function** 0 0: Access from ACCESS.bus and LPC bus (default) 0 1: Access from ACCESS.bus only 1 0: Access from LPC bus only 1 1: Reserved
4	**VDDLOAD (V_{DD}-Powered Load).** This bit indicates that the selected GPIO pin is connected to a device powered by V_{DD}. The input and output (including the internal pull-up) of such a GPIO pin are disabled whenever V_{DD} power to the PC8741x device falls below a certain value (see Section 11.1.5 on page 232). 0: GPIO pin connected to a V_{SB}-powered load (default) 1: GPIO pin connected to a V_{DD}-powered load
3-0	**Reserved.**

3.0 Device Architecture and Configuration (Continued)

3.15 X-BUS CONFIGURATION

This section is relevant only for the PC87416 and PC87417.

3.15.1 Logical Device F (X-Bus) Configuration

Table 27 lists the configuration registers that affect the X-Bus functional block. The X-Bus base address registers point to the X-Bus runtime registers described in Section 5.4 on page 107. The memory space to which the X-Bus responds is defined by the configuration registers described in the sections below. See Section 3.2.3 on page 40 for a detailed description of the other configuration registers. The standard configuration registers are powered by V_{DD}, however the specific configuration registers are powered by V_{SB}.

Table 27. X-Bus Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 43). When bit 0 is cleared, the registers of this logical device are not accessible.	R/W	V_{DD}	00h
60h	Base Address MSB register.	R/W	V_{DD}	00h
61h	Base Address LSB register. Bits 4-0 (for A4-A0) are read only, 00000b.	Varies per bit	V_{DD}	00h
70h	Interrupt Number and wake-up on IRQ enable.	RO	V_{DD}	00h
71h	Interrupt Type.	RO	V_{DD}	00h
74h	Report no DMA assignment.	RO	V_{DD}	04h
75h	Report no DMA assignment.	RO	V_{DD}	04h
F0h	X-Bus I/O Configuration register (XIOCNF).	Varies per bit	V_{SB}	00h
F1h	X-Bus I/O Base Address 1 High Byte register (XIOBA1H).	R/W or RO	V_{SB}	00h
F2h	X-Bus I/O Base Address 1 Low Byte register (XIOBA1L).	R/W or RO	V_{SB}	00h
F3h	X-Bus I/O Size 1 Configuration register (XIOSIZE1).	R/W or RO	V_{SB}	00h
F4h	X-Bus I/O Base Address 2 High Byte register (XIOBA2H).	R/W or RO	V_{SB}	00h
F5h	X-Bus I/O Base Address 2 Low Byte register (XIOBA2L).	R/W or RO	V_{SB}	00h
F6h	X-Bus I/O Size 2 Configuration register (XIOSIZE2).	R/W or RO	V_{SB}	00h
F7h	X-Bus Memory Configuration register 1 (XMEMCNF1).	R/W or RO	V_{SB}	00h
F8h	X-Bus Memory Configuration register 2 (XMEMCNF2).	Varies per bit	V_{SB}	00h
F9h	X-Bus Memory Base Address High Byte register (XMEMBAH).	R/W or RO	V_{SB}	00h
FAh	X-Bus Memory Base Address Low Byte register (XMEMBAL).	R/W or RO	V_{SB}	00h
FBh	X-Bus Memory Size Configuration register (XMEMSIZE).	R/W or RO	V_{SB}	00h
FCh	X-Bus IRQ Mapping register (XIRQMAP).	R/W	V_{SB}	00h

3.15.2 X-Bus I/O Range Programming

LPC I/O transactions can be forwarded to the X-Bus of the PC8741x device. The X-Bus I/O configuration registers define the map of I/O addresses to be forwarded. The PC8741x provides five individually enabled I/O zones. Each zone generates an internal select signal that is sent to the X-Bus functional block. The mapping of the internal select signals to the $\overline{XCS0-3}$ signals of the PC8741x device is controlled by the X-Bus functional block. See Section 5.2 on page 92 for further details.

The supported I/O zones are:

- User-Defined I/O Zone 0 through 3 (UDIZ0-3) - specified using the zone size (2^n where n is 0 through 8) and start address (must be aligned with the zone size).
- Debug Port Address (TST) - This zone is for debug use only.

3.0 Device Architecture and Configuration (Continued)

These decoded I/O zones are determined by the following seven registers: X-Bus I/O Configuration, X-Bus I/O Zone Base Address 1/2 High and Low Byte and X-Bus I/O Size 1/2 Configuration. When a zone is enabled but is not associated with any $\overline{XCS0\text{-}3}$ select signal in the X-Bus Interface, the X-Bus does not respond to LPC transactions accessing that zone.

The I/O Address Map Lock bit (LOCKIOMP) in XIOCNF register enables protecting the contents of the I/O mapping by preventing modifications to them that would cause access rights violation through aliasing.

Figure 7 illustrates the mapping of the User-Defined I/O zones to the host I/O space. The order between Base Address 1 and 2 is an example only and may be reversed.

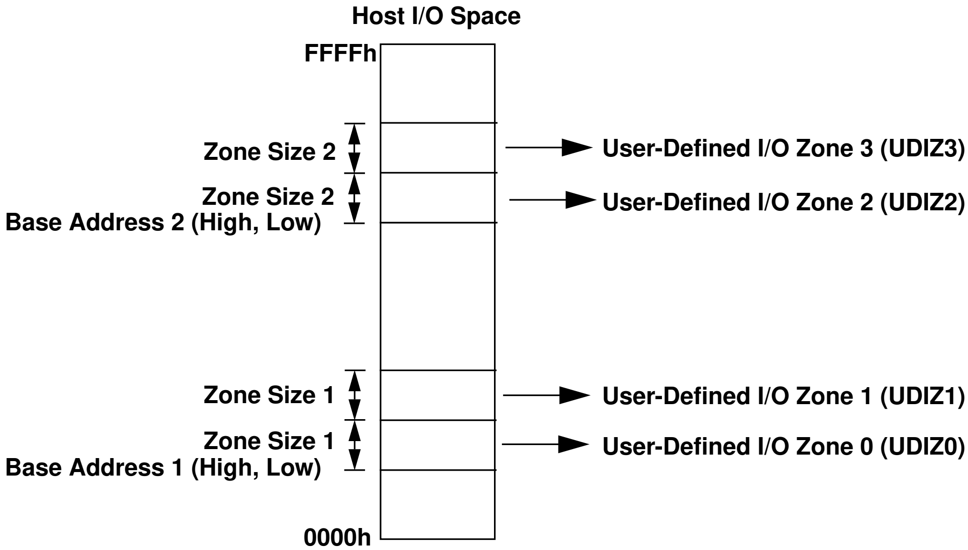


Figure 7. User-Defined I/O Block Mapping

3.15.3 X-Bus Memory Range Programming

LPC memory transactions or LPC-FWH transactions can be forwarded to the X-Bus Extension of the PC8741x device. X-Bus Memory Configuration Register 1 defines the address space to which the device responds. The XCNF2 strap input controls the default setting of the XMEMCNF1 register to enable booting from memories connected on the X-Bus. Two memory areas may be individually enabled: a user-defined zone and a BIOS memory zone (either BIOS-LPC, or BIOS-FWH spaces).

To enable BIOS support, set the XCNF2 strap input to select the BIOS mode (see Section 1.4.11 on page 29 for details). The PC8741x devices respond to LPC memory read and write transactions to/from the BIOS address spaces (see Table 28) as long as the BIOLPCEN bit of XMEMCNF1 register is set (see Section 3.15.11 on page 83).

Table 28. BIOS-LPC Memory Space Definition

Memory Address Range	Description
000E 0000h - 000E FFFFh	Extended BIOS Range (Legacy) Only when BIOEXTEN = 1 in XMEMCNF1 register
000F 0000h - 000F FFFFh	BIOS Range (Legacy)
FFFC 0000h - FFFF FFFFh FFF8 0000h - FFFF FFFFh FFF0 0000h - FFFF FFFFh FFE0 0000h - FFFF FFFFh FFC0 0000h - FFFF FFFFh FF80 0000h - FFFF FFFFh FF00 0000h - FFFF FFFFh FE00 0000h - FFFF FFFFh	386 mode BIOS Range. This is the upper 256 Kbytes to 32 Mbytes of the memory space, depending on the setting of BIOSIZE and SEL2BIOS in XMEMCNF2 (see Section 3.15.12 on page 84).

The PC8741x devices respond to LPC-FWH read transactions from the high memory address range ('386' mode BIOS range), shown in Table 28, as long as BIOFWHEN = 1 in the XMEMCNF1 register.

3.0 Device Architecture and Configuration (Continued)

Table 29. BIOS-FWH Memory Space Definition

Memory Address Range	Description
FFFC 0000h - FFFF FFFFh FFF8 0000h - FFFF FFFFh FFF0 0000h - FFFF FFFFh FFE0 0000h - FFFF FFFFh FFC0 0000h - FFFF FFFFh FF80 0000h - FFFF FFFFh FF00 0000h - FFFF FFFFh FE00 0000h - FFFF FFFFh	386 mode BIOS Range. This is the upper 256 Kbytes to 32 Mbytes of the memory space, depending on the setting of BIOSIZE and SEL2BIOS in XMEMCNF2 (see Section 3.15.12 on page 84). The PC8741x devices use the ID field and address bits A18-A27 to A25-A27, respectively, to identify FWH access to the BIOS memory.

Upon reset in BIOS mode, both the BIOLPCEN and the BIOFWHEN bits in the XMEMCNF1 register are set. The PC8741x device automatically detects the type of host boot protocol in use via the first completed BIOS read transaction after reset. If the first read is an LPC memory read, the BIOFWHEN bit is cleared. If the first read is an LPC-FWH read, the BIOLPCEN bit is cleared. The succeeding LPC or LPC-FWH transactions do not influence the BIOLPCEN and BIOFWHEN bits. The software can later enable the response to both address spaces by setting the cleared bit. Figure 8 illustrates this behavior.

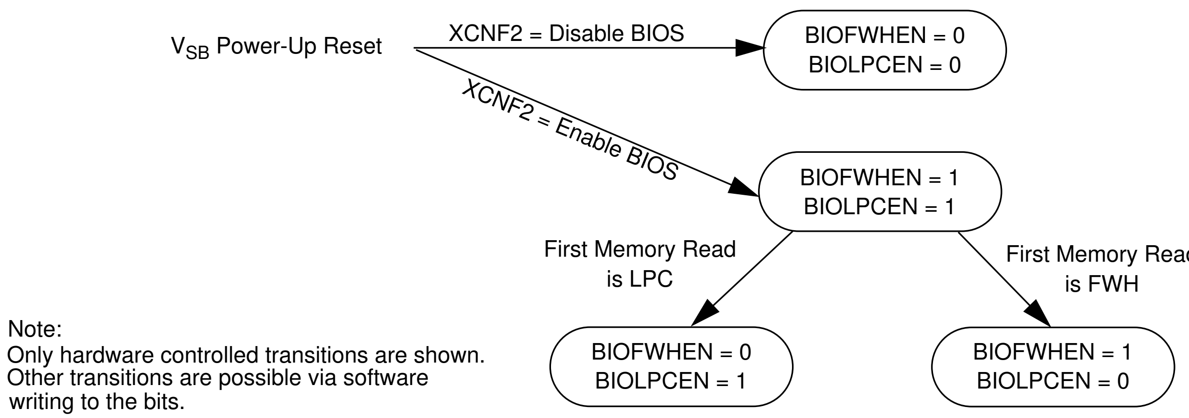


Figure 8. BIOS Mapping Enable Scheme

The two User-Defined Memory Zones (MEM0 and MEM1) are specified via a 32-bit base address. This address is formed by eight bits of the XMEMBAL register, eight bits of the XMEMBAH register and 16 least significant bits of 0. The size of each zone is specified through the XMEMSIZE register. The base address must be aligned to the block size. Figure 9 and Figure 10 illustrate the mapping of the LPC and FWH spaces to the different memory zones.

The Memory Address Map Lock bit in X-Bus Memory Configuration Register 2 enables protection of the contents of the memory mapping, thus preventing modifications to them that may cause access rights violation through aliasing.

The address used for the X-Bus transaction is the 28 least significant bits of the address bus. In read transactions, the data read from the X-Bus is passed to the LPC bus. In write transactions, the data from the LPC is passed to the X-Bus.

3.0 Device Architecture and Configuration (Continued)

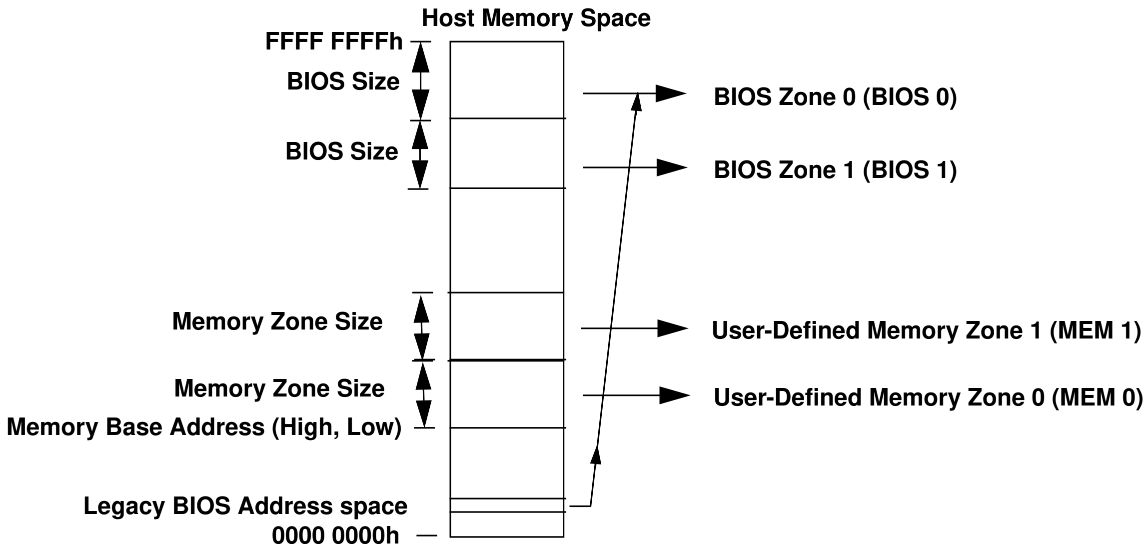


Figure 9. Memory Block Mapping

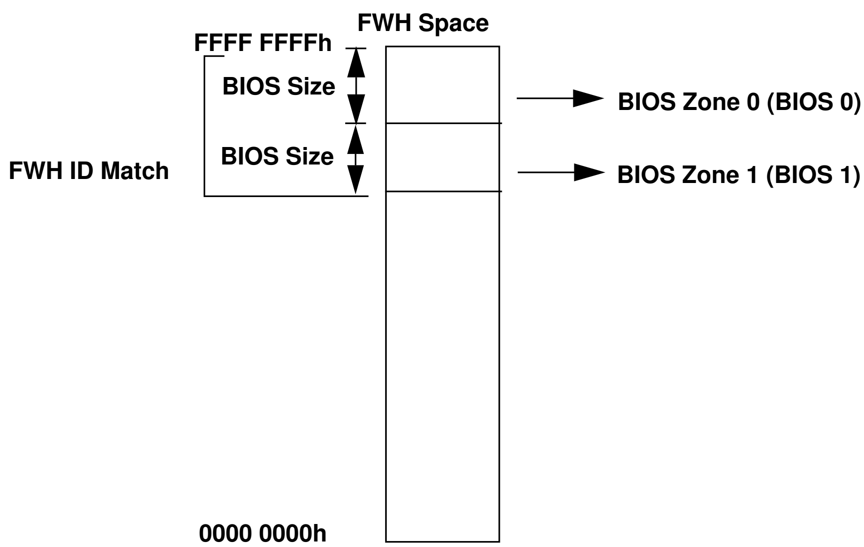


Figure 10. FWH Memory Mapping

3.15.4 X-Bus I/O Configuration Register (XIOCNF)

This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F0h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKIOMP**	**Reserved**		**TSTADEN**	**UDIOZEN3**	**UDIOZEN2**	**UDIOZEN1**	**UDIOZEN0**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	RW1L	**LOCKIOMP (Lock I/O Address Map).** When set to 1, this bit locks the configuration of registers XIOCNF, XIOBA1H, XIOBA1L, XIOSIZE1, XIOBA2H, XIOBA2L and XIOSIZE2 by disabling writing to all their bits (including to the LOCKIOMP bit itself). Once set, this bit can be cleared either by V_{DD} Power-Up reset (or Hardware reset) or by V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKX bit in the ACBLKCTL register (**PC87417**). 0: R/W bits are enabled for write (default) 1: All bits are RO
6-5	-	**Reserved.**
4	R/W or RO	**TSTADEN (TST Debug Port Address Enable).** When set, enables the mapping of I/O address 80h to the X-Bus space. 0: Disabled (default) 1: Enabled
3	R/W or RO	**UDIOZEN3 (User-Defined I/O Zone Enable 3).** This bit enables the mapping of the User-Defined I/O zone 3 to the X-Bus space. The zone base address and size are defined by the XIOBA2H/XIOBA2L and XIOSIZE2 registers, respectively. The base address for this Zone is: (Base Address 2) + (Size 2) 0: Disabled (default) 1: Enabled
2	R/W or RO	**UDIOZEN2 (User-Defined I/O Zone Enable 2).** This bit enables the mapping of the User-Defined I/O zone 2 to the X-Bus space. The zone base address and size are defined by the XIOBA2H/XIOBA2L and XIOSIZE2 registers, respectively. The base address for this Zone is: (Base Address 2) 0: Disabled (default) 1: Enabled
1	R/W or RO	**UDIOZEN1 (User-Defined I/O Zone Enable 1).** This bit enables the mapping of the User-Defined I/O zone 1 to the X-Bus space. The zone base address and size are defined by the XIOBA1H/XIOBA1L and XIOSIZE1 registers, respectively. The base address for this Zone is: (Base Address 1) + (Size 1) 0: Disabled (default) 1: Enabled
0	R/W or RO	**UDIOZEN0 (User-Defined I/O Zone Enable 0).** This bit enables the mapping of the User-Defined I/O zone 0 to the X-Bus space. The zone base address and size are defined by the XIOBA1H/XIOBA1L and XIOSIZE1 registers, respectively. The base address for this Zone is: (Base Address 1) 0: Disabled (default) 1: Enabled

3.15.5 X-Bus I/O Base Address 1 High Byte Register (XIOBA1H)

This register describes the high byte of the Base Address for user-defined I/O zone blocks 0 and 1, which are mapped to the X-Bus. This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F1

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	IOBA1H							
Reset	0	0	0	0	0	0	0	0

3.0 Device Architecture and Configuration (Continued)

Bit	Description
7-0	**IOBA1H (I/O User-Defined Zone Base Address 1 High).** Defines the upper eight bits of the user-defined I/O blocks 0 and 1 base address. The base address must be aligned on the selected block size.

3.15.6 X-Bus I/O Base Address 1 Low Byte Register (XIOBA1L)

This register describes the low byte of the Base Address for User-Defined I/O zone blocks 0 and 1, which are mapped to the X-Bus. This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F2h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**IOBA1L**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**IOBA1L (I/O User-Defined Zone Base Address 1 Low).** Defines the lower eight bits of the user-defined I/O blocks 0 and 1 base address. The base address must be aligned on the selected block size.

3.15.7 X-Bus I/O Size 1 Configuration Register (XIOSIZE1)

This register defines the size of User-Defined I/O zone blocks 0 and 1, which are mapped to the X-Bus. The two blocks are contiguous and both have the same size. The User-Defined I/O Zone 1 address does not depend on Zone 0 being enabled. This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F3h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**IOSIZE1**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3-0	**IOSIZE1 (User-Defined I/O Zone Size 1).** Defines the size in bytes of the zone window. The size is defined as a power of two using the equation: NumOfBytes = 2^n (where n = the value of the IOSIZE1 field). The zone must always be aligned to the window size (i.e., for a 128-byte window, the seven LSBs of the base address are zero). **Bits** **3 2 1 0 Size (Bytes)** 0 0 0 0: 1 (2^0 - default) . . . 1 0 0 0: 256 (2^8) Other: Reserved

3.0 Device Architecture and Configuration (Continued)

3.15.8 X-Bus I/O Base Address 2 High Byte Register (XIOBA2H)

This register describes the high byte of the Base Address for User-Defined I/O zone blocks 2 and 3, which are mapped to the X-Bus. This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F4

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**IOBA2H**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**IOBA2H (I/O User-Defined Zone Base Address 2 High).** Defines the upper eight bits of the User-Defined I/O blocks 2 and 3 base address. The base address must be aligned on the selected block size.

3.15.9 X-Bus I/O Base Address 2 Low Byte Register (XIOBA2L)

This register describes the low byte of the Base Address for User-Defined I/O zone blocks 2 and 3, which are mapped to the X-Bus. This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F5h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**IOBA2L**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**IOBA2L (I/O User-Defined Zone Base Address 2 Low).** Defines the lower eight bits of the user-defined I/O blocks 2 and 3 base address. The base address must be aligned on the selected block size.

3.0 Device Architecture and Configuration (Continued)

3.15.10 X-Bus I/O Size 2 Configuration Register (XIOSIZE2)

This register defines the size of User-Defined I/O zone blocks 2 and 3, which are mapped to the X-Bus. The two blocks are contiguous and have the same size. The User-Defined I/O Zone 3 address does not depend on Zone 2 being enabled. This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F6h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**IOSIZE2**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3-0	**IOSIZE2 (User-Defined I/O Zone Size 2).** Defines the size in bytes of the zone window. The size is defined as a power of two using the equation: NumOfBytes = 2^n (where n = the value of bits 3-0). The zone must always be aligned to the window size (i.e., for a 128-byte window, the seven LSBs of the base address are zero). **Bits** **3 2 1 0 Size (Bytes)** 0 0 0 0: 1 (2^0 - default) ▪ ▪ ▪ 1 0 0 0: 256 (2^8) Other: Reserved

3.0 Device Architecture and Configuration (Continued)

3.15.11 X-Bus Memory Configuration Register 1 (XMEMCNF1)

This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F7h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**FWHID**				**BIOFWHEN**	**UDMEMEN**	**BIOEXTEN**	**BIOLPCEN**
Reset	0	0	0	0	Strap	0	0	Strap

Bit	Description
7-4	**FWHID (BIOS FWH ID).** These four bits correspond to the Device Select nibble that is part of a FWH transaction (see Section 4.2 on page 90 for details).
3	**BIOFWHEN (BIOS FWH Enable).** When set, this bit enables the PC8741x device to respond to LPC-FWH transactions to the BIOS-FWH space. The default value is set according to the XCNF2 strap, sampled at V_{SB} Power-Up reset. The value of this bit is later updated based on the detected host BIOS scheme (see Section 3.15.3 on page 76 for details). 0: Disabled (default when XCNF2 = 0 - disables BIOS configuration) 1: Enabled (default when XCNF2 = 1 - enables BIOS configuration)
2	**UDMEMEN (User-Defined Memory Space Enable).** When set, this bit enables the PC8741x device to respond to LPC memory read and write transactions in the user-defined memory range. The base address and size of the user-defined range is specified by the XMEMBAH/XMEMBAL and XMEMSIZE registers, respectively. 0: Disabled (default) 1: Enabled
1	**BIOEXTEN (BIOS Extended Space Enable).** Expands the BIOS address space to which the PC8741x device responds, to include the Extended BIOS address range. 0: Disabled (default) 1: Enabled
0	**BIOLPCEN (BIOS LPC Enable).** Enables the PC8741x device to respond to LPC memory transactions to the BIOS-LPC space. The default value is set according to the XCNF2 strap, sampled at V_{SB} Power-Up reset. The value of this bit is later updated, based on the detected host BIOS scheme (see Section 3.15.3 on page 76 for details). 0: Disabled (default when XCNF2 = 0 - disables BIOS configuration) 1: Enabled (default when XCNF2 = 1 - enables BIOS configuration)

3.0 Device Architecture and Configuration (Continued)

3.15.12 X-Bus Memory Configuration Register 2 (XMEMCNF2)

This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F8h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKMMP**	**Reserved**		**SEL2UDM**	**SEL2BIOS**	**BIOSIZE**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**LOCKMMP (Lock Memory Address Map).** When set to 1, this bit locks the configuration of registers XMEMCNF1, XMEMCNF2, XMEMBAH, XMEMBAL and XMEMSIZE by disabling writing to all their bits (including to the LOCKMAP bit itself). Once set, this bit can be cleared either by V_{DD} Power-Up reset (or Hardware reset) or by V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKX bit in the ACBLKCTL register (**PC87417**). 0: R/W bits are enabled for write (default) 1: All bits are RO
6-5	**Reserved.**
4	**SEL2UDM (Dual User-Defined Memory Select Enable).** Enables the PC8741x device to control two memory devices for data storage. The second zone (MEM Zone 1) is mapped on top of the first zone (MEM Zone 0). Both zones are the same size. The base address of MEM Zone 0 is specified by the XMEMBAH and XMEMBAL registers. The size of both memory zones is specified by the XMEMSIZE register. The base address of MEM Zone 1 is: (Base Address Memory Zone) + (Size Memory Zone). 0: Disabled - Use only MEM Zone 0, if enabled (default) 1: Enabled - If the user-defined memory is enabled, use both MEM Zone 0 and MEM Zone 1
3	**SEL2BIOS (Dual BIOS Select Enable).** Enables the PC8741x device to control two flash devices for BIOS storage. The first device (BIOS Zone 0) is used for legacy and the upper 386 zone. BIOS zone 1 is on the next “BIOS Size” block in the 386 address range (addresses lower than these of Block 1). When FWH is enabled, BIOS Zone 0 responds to the upper addresses and BIOS Zone 1, if enabled, responds to the group below Zone 0, as defined by BIOS Size. Both zones use the same FWHID value. 0: Disabled - Use BIOS Zone 0 only, if enabled (default) 1: Enabled - If either the LPC BIOS or the FWH BIOS is enabled, use both BIOS Zone 0 and BIOS Zone 1
2-0	**BIOSIZE (BIOS Size).** Define the Size of one BIOS Zone in the 386 range. Note that by setting the Dual BIOS Select Enable, two equal-sized BIOS Zones are available. **Bits** **2 1 0 Size (Bytes)** 0 0 0: 256 Kbytes (default) 0 0 1: 512 Kbytes 0 1 0: 1 Mbyte 0 1 1: 2 Mbytes 1 0 0: 4 Mbytes 1 0 1: 8 Mbytes 1 1 0: 16 Mbytes 1 1 1: Reserved

3.0 Device Architecture and Configuration (Continued)

3.15.13 X-Bus Memory Base Address High Byte Register (XMEMBAH)

This register describes the high byte for the user-defined memory zones mapped to the X-Bus (decoded as bits 31 to 24 of the 32-bit address range; bits 15-0 are 0). This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index F9h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**MEMBAH**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**MEMBAH (User-Defined Memory Zone Address High).** Defines the upper eight bits of the user-defined memory block base address. The base address must be aligned on the selected block size.

3.15.14 X-Bus Memory Base Address Low Byte Register (XMEMBAL)

This register describes the low byte for the user-defined memory zones mapped to the X-Bus (decoded as bits 23 to 16 of the 32-bit address range; bits 15 to 0 are 0). This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index FAh

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**MEMBAL**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**MEMBAL (User-Defined Memory Zone Address Low).** Defines the lower eight bits of the user-defined memory block base address. The base address must be aligned on the selected block size.

3.0 Device Architecture and Configuration (Continued)

3.15.15 X-Bus Memory Size Configuration Register (XMEMSIZE)

This register defines the size of each user-defined memory zone mapped to the X-Bus. This register is reset by hardware to 00h.

Power Well:V_{SB}

Location:Index FBh

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**MEMSIZE**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3-0	**MEMSIZE (User-Defined Memory Zone Size).** Defines the size of one zone window (in bytes). The size is defined as a power of two using the equation: NumOfBytes = 2^n (where n = the value of the MEMSIZE field +16). The zone must always be aligned to the window size (i.e., for a 128 Kbyte window, the 17 LSBs of the address must be zero). **Bits** **3 2 1 0 Size (Bytes)** 0 0 0 0: 64K (2^{16} - default) . . . 1 0 0 0: 16M (2^{24}) Other: Reserved

3.15.16 X-Bus IRQ Mapping Register (XIRQMAP)

This register defines the mapping of the XIRQ signal.

Power Well:V_{SB}

Location:Index FCh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**IRQMAP**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3-0	**IRQMAP (XIRQ Mapping).** Defines to which host IRQ the XIRQ input is routed. **Bits** **3 2 1 0 Function** 0 0 0 0: IRQ Disabled (default) 0 0 0 1: IRQ1 . . . 1 1 1 1: IRQ 15

3.0 Device Architecture and Configuration (Continued)

3.16 REAL TIME CLOCK (RTC) CONFIGURATION

3.16.1 General Description

The RTC provides timekeeping and calendar management capabilities. It uses a 32.768 KHz signal as the basic clock for timekeeping. The RTC also includes 242 bytes of battery-backed RAM for general-purpose use.

The RTC runtime registers are shown in Section 8.3.2 on page 150. These registers are V_{PP} powered.

3.16.2 Logical Device 10 (RTC) Configuration

Table 30 lists the configuration registers that affect the Real Time Clock. The standard configuration registers (see Section 3.2.3 on page 40) are powered by V_{DD}. The specific configuration registers are powered by V_{SB}.

Table 30. RTC Configuration Registers

Index	RTC Configuration Register or Action	Type	Power Well	Reset
30h	Activate (see Section 3.3.1 on page 43). When bit 0 is cleared, the runtime registers of this logical device are not accessible.	R/W	V_{DD}	00h
60h	Standard Base Address MSB register.	R/W	V_{DD}	00h
61h	Standard Base Address LSB register. Bit 0 (for A0) is read only 0b.	R/W	V_{DD}	70h
62h	Extended RAM Base Address MSB register.	R/W	V_{DD}	00h
63h	Extended RAM Base Address LSB register. Bit 0 (for A0) is read only 0b.	R/W	V_{DD}	72h
70h	RTC Interrupt Number and Wake-Up on IRQ Enable register.	R/W	V_{DD}	08h
71h	RTC Interrupt Type. Bit 1 is read/write; other bits are read only.	R/W	V_{DD}	00h
74h	Report no DMA assignment.	RO	V_{DD}	04h
75h	Report no DMA assignment.	RO	V_{DD}	04h
F0h	RAM Lock Register (RLR).	R/W1S	V_{SB}	00h
F1h	Date-of-Month Alarm Register Offset (DOMAO).	R/W	V_{SB}	00h
F2h	Month Alarm Register Offset (MONAO).	R/W	V_{SB}	00h
F3h	Century Register Offset (CENO).	R/W	V_{SB}	00h

3.0 Device Architecture and Configuration (Continued)

3.16.3 RAM Lock Register (RLR)

Once a non-reserved bit is set to 1, it can be cleared either by V_{DD} Power-Up reset (or Hardware reset) or by V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, all the bits are cleared by setting the UNLOCKR bit in the ACBLKCTL register (see Section 6.3.4 on page 128 - **PC87413 and PC87417**).

Power Well:V_{SB}

Location:Index F0h

Type: R/W1S

Bit	7	6	5	4	3	2	1	0
Name	**BLSTR**	**BLRWR**	**BLEXRWR**	**BLEXRRD**	**BLEXR**	**Reserved**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**BLSTR (Block Standard RAM).** Disables both read and write access to locations 38h-3Fh of the Standard RAM (writes are ignored; reads return FFh). 0: Normal access (default) 1: Read and write to locations 38h-3Fh of the Standard RAM are blocked
6	**BLRWR (Block RAM Write).** Disables write access to both the Standard and Extended RAM (writes are ignored). 0: Normal access (default) 1: Writes to RAM (Standard and Extended) are blocked
5	**BLEXRWR (Block Extended RAM Write).** Disables write access to bytes 00h-1Fh of the Extended RAM (writes are ignored). 0: Normal access (default) 1: Writes to bytes 00h-1Fh of the Extended RAM are blocked
4	**BLEXRRD (Block Extended RAM Read).** Disables read access from bytes 00h-1Fh of the Extended RAM (reads return FFh). 0: Normal access (default) 1: Reads from bytes 00h-1Fh of the Extended RAM are blocked
3	**BLEXR (Block Extended RAM).** Disables both read and write access to the Extended RAM (writes are ignored; reads return FFh). 0: Normal access (default) 1: Read and write to the Extended RAM are blocked
2-0	**Reserved.**

3.0 Device Architecture and Configuration (Continued)

3.16.4 Date-of-Month Alarm Register Offset (DOMAO)

Power Well: V_{SB}
Location: Index F1h
Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**DOMAO**						
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
6-0	**DOMAO (Date of Month Alarm Register Offset Value).** Sets the offset value of the Date-of-Month Alarm (DOMA) runtime register.

3.16.5 Month Alarm Register Offset (MONAO)

Power Well: V_{SB}
Location: Index F2h
Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**MONAO**						
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
6-0	**MONAO (Month Alarm Register Offset Value).** Sets the offset value of the Month Alarm (MONA) runtime register.

3.16.6 Century Register Offset (CENO)

Power Well: V_{SB}
Location: Index F3h
Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**CENO**						
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved.**
6-0	**CENO (Century Register Offset Value).** Sets the offset value of the Century (CEN) runtime register.

4.0 LPC Bus Interface

With the exception of the ACCESS.bus Interface, the host can access all the functional blocks of the PC8741x device through the LPC bus.

4.1 OVERVIEW

The LPC host Interface supports 8-bit I/O Read, 8-bit I/O Write and 8-bit DMA transactions, as defined in Intel's *LPC Interface Specification, Revision 1.0*.

4.2 LPC TRANSACTIONS

The LPC Interface of the PC8741x devices can respond to the following LPC transactions as part of the standard ServerI/O implementation:

- 8-bit I/O read and write cycles.
- 8-bit DMA read and write cycles.
- DMA request cycles.

In addition, the X-Bus bridge uses the following transactions (**PC87416 and PC87417**):

- 8-bit I/O read and write cycles.
- 8-bit memory read and write.
- 8-bit FWH read

LPC-FWH Cycles: The LPC bus and the ACCESS.bus (**PC87413 and PC87417**) use the internal bus of the PC8741x device to access the internal modules or to bridge transactions to the X-Bus (see the Block Diagrams on pages 1 and 5). In case both the LPC and the ACCESS.bus try to access targets (same or different) through the internal bus simultaneously, the LPC transaction is deferred until the end of the ACCESS.bus transaction. This is achieved by generating Long Wait SYNC cycles on the LPC bus. The amount of time the LPC bus waits depends on the duration of the ACCESS.bus transaction (see Section 6.2.10 on page 125). An LPC transaction that starts before an ACCESS.bus transaction is performed normally (i.e., without interference).

The LPC-FWH read cycle is similar to the LPC memory read cycle, as shown below. The DATA, TAR and SYNC fields are as specified for LPC memory read cycle. The START field is similar to the equivalent field in the LPC memory read cycle but differs in the data placed on the LAD signals (see details in the cycle description). The Address field contains only seven nibbles (A27-A0), starting with the most significant. The IDSEL and MSIZE fields are specific to LPC-FWH transactions.

FWH Read Cycle

1. START FWH Memory Read cycle type = 1101 (0Dh).
2. IDSEL FWH Device Select ID nibble (compared with the FWHID field in the XMEMCNF1 register, Section 3.15.11 on page 83).
3. MADDR Memory Address: seven address nibbles, MS nibble first (see *LPC-FWH Address Translation:*, below).
4. MSIZE Memory Size, single byte = 0000 (00h).
5. TAR (two cycles).
6. SYNC.
7. DATA Data: two nibbles, LS nibble first (D3-D0, D7-D4).
8. TAR (two cycles).

The IDSEL field is compared with the FWHID field in the XMEMCNF1 register, as described in Section 3.15.11 on page 83. If the two match, the PC8741x device continues handling the transaction; if not, the current LPC-FWH transaction is ignored.

The MSIZE field is ignored by the PC8741x devices.

LPC-FWH Address Translation: The address field in the LPC-FWH transaction is constructed of seven nibbles, containing the 28 LS address bits (A27-A0), as follows: the first incoming nibble corresponds to addresses A27-A24, the second to A23-A20, and so forth, until the seventh nibble, which corresponds to A3-A0. The MS bits of the 32-bit addresses (A31-A28) are assumed to be ‘1111’.

4.0 LPC Bus Interface (Continued)

4.3 CLKRUN FUNCTIONALITY

The PC8741x devices support the CLKRUN I/O signal, which is implemented according to the specification in *PCI Mobile Design Guide*, *Revision 1.1,* December 18, 1998. The PC8741x devices support operation with both a slow and stopped clock in ACPI state S0 (the system is active but is not being accessed). In the following cases, the PC8741x device drives the CLKRUN signal low to force the LPC bus clock into full speed operation:

- An IRQ is pending internally, waiting to be sent through the serial IRQ.
- A DMA request is pending internally, waiting to be sent through the serial DMA.

Note: When the CLKRUN signal is not in use, the PC8741x devices assume a valid clock on the LCLK pin.

4.4 INTERRUPT SERIALIZER

The Interrupt Serializer translates parallel interrupt request (PIRQ) signals received from external devices, via the XIRQ pin (**PC87416 and PC87417**) and from internal IRQ sources, into serial interrupt request data transmitted over the SERIRQ bus. This enables devices that support only parallel IRQs to be integrated into a system that supports only serial IRQs.

The external XIRQ signal and the internal IRQs are fed into a Mapping, Enable and Polarity Control block, which maps them to their associated IRQ slots. The IRQs are then fed into the Interrupt Serializer, where they are translated into serial data and transmitted over the SERIRQ bus.

The XIRQ input value is routed to the Interrupt Serializer as the IRQn value to be driven onto IRQ slot n.

The same slot cannot be shared among different interrupt sources in the device.

When a transition is sensed on an IRQ source, the new value of the IRQ source is transmitted over the SERIRQ bus during the corresponding IRQ slot. For example, when a transition on XIRQ is sensed, the new value of XIRQ is transmitted during slot n of the SERIRQ bus.

Figure 11 shows the mechanism for both interrupt serialization and wake-up.

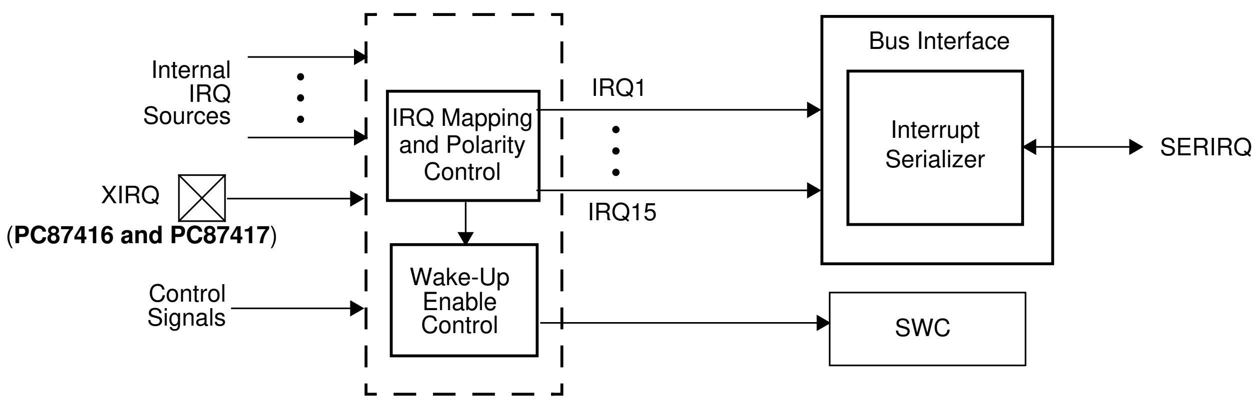


Figure 11. Interrupt Serialization and Wake-Up Mechanism

5.0 X-Bus Extension

This section is relevant only for the PC87416 and PC87417. In the PC87413 and PC87414, all X-Bus Extension bits and signals that influence other modules are at their default value.

5.1 OVERVIEW

The PC8741x provides an X-Bus extension to the LPC bus or ACCESS.bus to enable the connection of external 8-bit memories or peripherals through the X-Bus's ISA-like interface. A single read/write line and an enable pin replace the ISA-like protocol. The decode logic, described in Section 3.15 on page 75, defines the addresses for which the X-Bus generates transactions that occur in the I/O address space and memory address space or in the FWH memory address space. Using the X-Bus Interface, the PC8741x serves as a bridge for such transactions over the X-Bus. Figure 12 is a block diagram of the X-Bus bridging function. For details on the decoder functions, see Section 3.15 on page 75. All other functions are described in detail in this section.

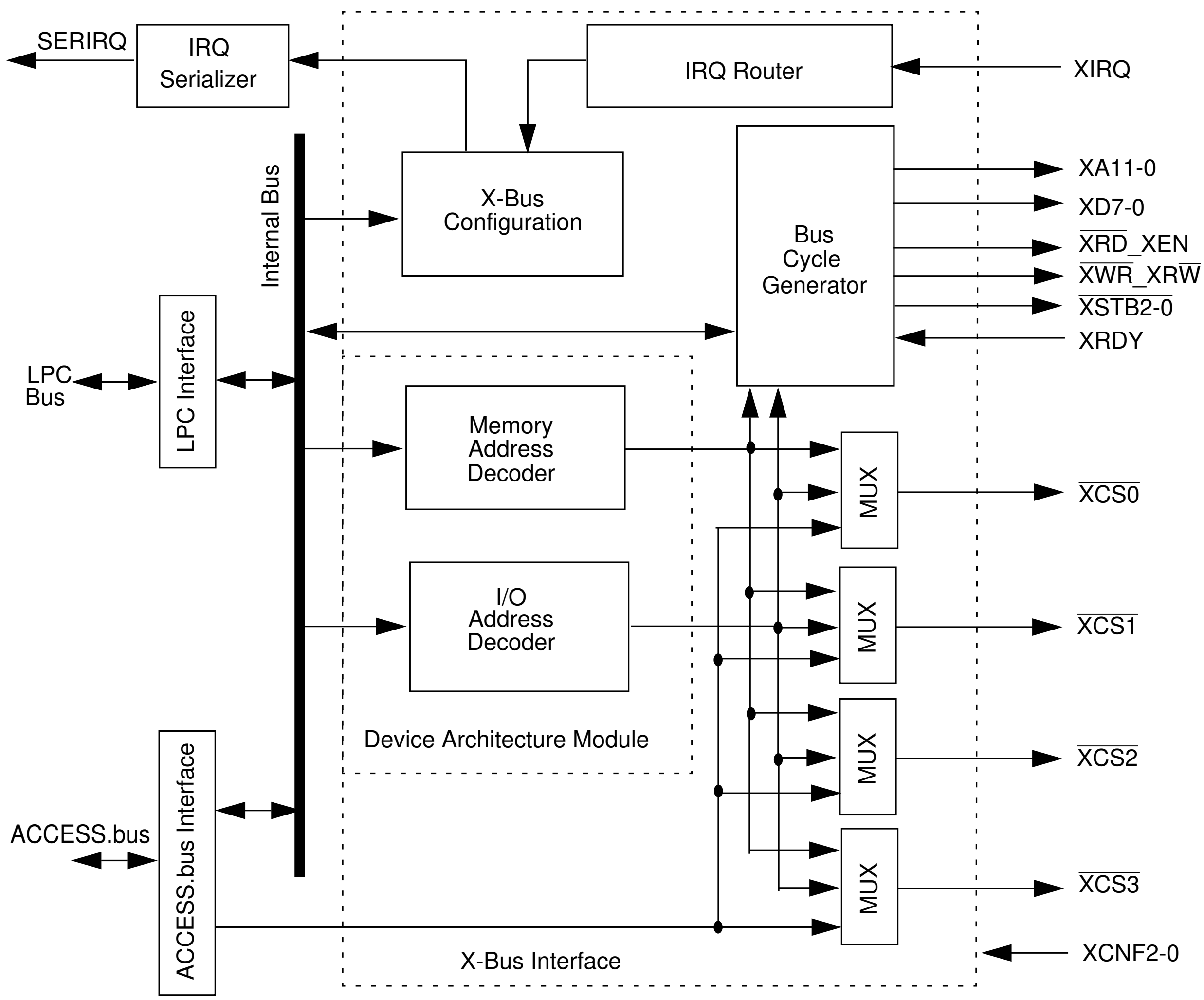


Figure 12. X-Bus Extension Block Diagram

The PC8741x supports one IRQ input: XIRQ. This pin may be used to support external legacy devices that are connected on the X-Bus. The interrupt from this pin can be routed to any one of 15 host IRQs. The IRQ input is mapped by the X-Bus XIRQ Mapping register at FCh. The XIRQC register enables the user to define the interrupt as active high or low and to route it to a wake-up event.

5.2 X-BUS TRANSACTIONS

The X-Bus extension supports 8-bit I/O or Memory read/write cycles.

The zone mapping of the chip-select signals determines how X-Bus read and write cycles correspond to memory and I/O LPC bus cycles. The zone mapping to a select signal (XCS3-0) must be enabled in order for the zone to respond to LPC transactions. However, when the chip-select signal is not required by an off-chip device, multiplexing the chip select to a pin is not necessary.

5.0 X-Bus Extension (Continued)

There are two X-Bus address modes:

- Normal Address mode - A signal is assigned for each address line (only XA11-XA0 are available at the device pins) and a non-multiplexed address data bus is used. In this mode, only address signals 0 through 11 are generated.
- Latched Address mode - The number of pins used for outputting the address is reduced. The address lines are multiplexed with the data bus. External latches may be used to generate address signals from the multiplexed bus. These address signals are required to access memory and I/O devices. In this mode address, signals 0 through 27 are generated, allowing access to memory in excess of 1 Mbyte.

There are two X-Bus transaction modes:

- Mode 0 - The X-Bus transactions are ISA-like, using separate read and write signals. $\overline{\text{XWR}}$_XR$\overline{\text{W}}$ functions as the write signal ($\overline{\text{XWR}}$); $\overline{\text{XRD}}$_XEN functions as the read signal ($\overline{\text{XRD}}$). The following speed levels are available for Mode 0, X-Bus transactions:
  - — Normal
  - — Fast
  - — Turbo
- Mode 1 - The X-Bus transactions are read/write and enable controlled transactions, using $\overline{\text{XWR}}$_XR$\overline{\text{W}}$ as the read and write signal (XR$\overline{\text{W}}$) and $\overline{\text{XRD}}$_XEN as the enable signal (XEN). When $\overline{\text{XWR}}$_XR$\overline{\text{W}}$ is high, it identifies a read transaction; when low, it identifies a write transaction.

5.2.1 Transaction Clock

X-Bus access timing is referenced to an internal clock referred to as CLK or “the clock”. Transactions are described in terms of this clock and the AC specifications are also defined relative to it. This provides an easy way for calculating the timing during system design. Note that the system interface is optimized for an asynchronous interface. For hints on how to use the asynchronous interface, refer to the usage hints in Section 5.5 on page 115.

X-Bus Clock:

- For transactions triggered by the LPC bus, the clock is an internal version of the LPC clock (i.e., it has the same frequency but may have some phase delay).
- For transactions driven by the ACCESS.bus (**PC87417**), the clock is the Standby clock as defined in Section 2.3.1 on page 36.

5.2.2 Programmable Range Chip Select

The PC8741x has four chip-select signals ($\overline{\text{XCS3-0}}$) to control the X-Bus accesses to off-chip devices. The PC8741x X-Bus functional block enables flexible association of these chip selects with I/O and memory address ranges in the LPC address space. The Zone Mapping field of the X-Bus Select Configuration registers defines the decoded address range(s) to which the specific $\overline{\text{XCSn}}$ signal responds. In addition, the X-Bus Configuration register enables specifying the access time for each select signal via bits that control the fixed wait and variable wait cycles (using the XRDY input).

If the chip-select signal setting results in a conflict in which one or more selects are configured for the same zone, $\overline{\text{XCS0}}$ has the highest priority and $\overline{\text{XCS3}}$ has the lowest. The $\overline{\text{XCSn}}$ signal with the lower priority remain inactive and their Select Configuration register setting is ignored. For zones that are not associated with one of the chip-select signals, the X-Bus does not respond to LPC transactions.

In addition, X-Bus transactions may be generated in response to a request from the ACCESS.bus (**PC87417**). In such a case, the target select signal ($\overline{\text{XCS3}}$) and the offset address are specified in the ACCESS.bus protocol. See Section 6.2.9 on page 121 for the specification of ACCESS.bus operation.

5.2.3 LPC and FWH Address-to-X-Bus Address Translation

The BIOS memory on the LPC bus can occupy one of three regions in the memory space (see Table 28 on page 76). Address translation between the LPC bus address and the X-Bus is performed as follows:

I/O Transactions. The 16-bit address received from the LPC bus is used to decode the different I/O zones described in Section 3.15.2 on page 75. The address is then left-padded with zeroes (address lines 16 through 27) to create the 28-line input address to the X-Bus Extension functional block.

5.0 X-Bus Extension (Continued)

Memory Transactions. The 32-bit address received from the LPC bus is used to decode the different memory zones described in Section 3.15.3 on page 76. The address is then translated to the X-Bus address, using the following rules:

- User-Defined Memory Zones (MEM 0 and MEM 1) and 386 Mode-Compatible BIOS Range: The 28 least significant address lines of the LPC address are used as the X-Bus input address. Figure 13 illustrates the mapping for this zone.
- Legacy and Extended Legacy BIOS Range: The 17 least significant address lines (A16-0) of the LPC address are routed as the 17 least significant address signals of the X-Bus (XA16-0). The upper 11 X-Bus address lines are driven to '1'. This shifts the addresses to the top of the X-Bus memory space (see Figure 14).

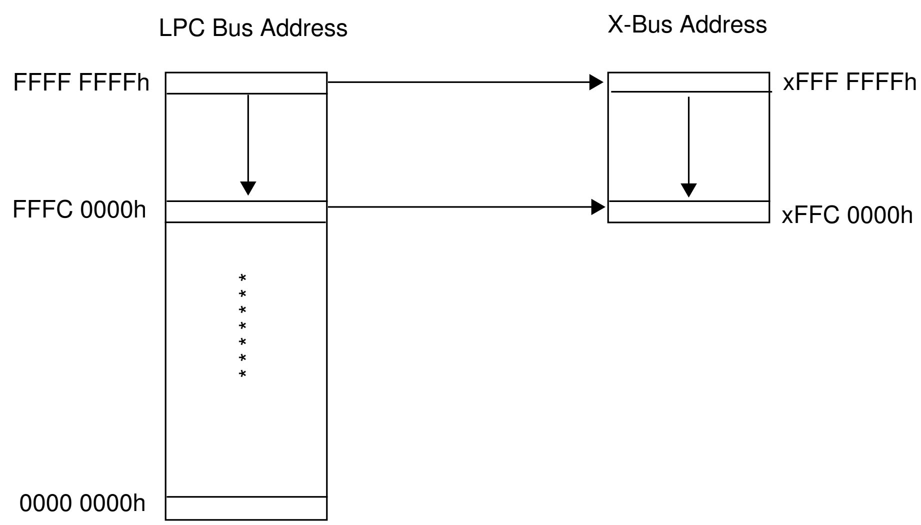


Figure 13. LPC-to-X-Bus Address Translation: 386 Mode-Compatible BIOS Range

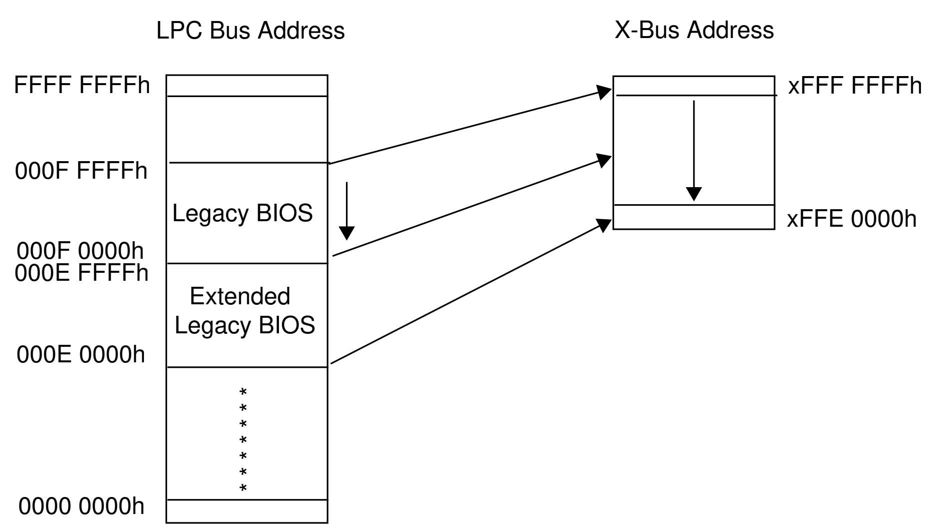


Figure 14. LPC-to-X-Bus Address Translation: Legacy and Extended Legacy BIOS Ranges

5.0 X-Bus Extension (Continued)

5.2.4 Indirect Memory Read and Write Transactions

I/O mapped registers accessed through an LPC I/O transaction may be used to perform an X-Bus memory transaction. This mechanism uses the following X-Bus Extension module registers:

- Four Indirect Memory Address registers (XIMA3-0), representing address bits 31 to 0.
- One Indirect Memory Data register (XIMD), representing data bits 7 to 0.
- Four enable bits, one for each Select Configuration register, XZCNF0, XZCNF1, XZCNF2 and XZCNF3.

Following an LPC I/O write to the XIMD register, a Memory write cycle is initiated on the X-Bus using the addresses from the previously written XIMA3-0 registers and data from the XIMD register. Following an LPC I/O read from the XIMD register, a Memory read cycle is initiated on the X-Bus using the address from the XIMA3-0 registers. The returned data from the X-Bus cycle is used to finish the read cycle from the XIMD register.

Indirect memory transactions may be enabled for one chip-select signal only. If more than one enable bit in the Select Configuration registers is set, the indirect memory access will be available only for the $\overline{\text{XCSn}}$ with the highest priority. The setting of the enable bit for the chip selects with lower priority will be ignored. $\overline{\text{XCS0}}$ has the highest priority and $\overline{\text{XCS3}}$ has the lowest priority.

5.2.5 Mode 0, Normal Address X-Bus Transactions

The read and write transactions in Normal Address mode are similar to those used in the X-Bus or ISA bus. At least two idle cycles are inserted at the end of each X-Bus transaction cycle before the next transaction starts (there may be more idle cycles due to the LPC transactions). This mode is selected for transactions accessing $\overline{\text{XCSn}}$ by setting TRANSMD = 0 in the corresponding XZMn register.

Read Transactions. When a read cycle on the LPC falls within an enabled decoded address range of the X-Bus functional block (or an indirect read is started or an X-Bus read through the ACCESS.bus is started) and the relevant $\overline{\text{XCSn}}$ is set to mode 0, a Mode 0 read cycle begins. A read cycle (see Figure 15) starts by outputting the address on address signals XA11-0 on the rising edge of the clock. During this time, the PC8741x device does not drive the data bus signals XD7-0. One CLK cycle later, a chip-select signal $\overline{\text{XCSn}}$ is asserted, where n is a chip-select number from 0 to 3, based on the address accessed and the select signal mapping. Three CLK cycles later, on the rising edge of the clock, the $\overline{\text{XRD}}$ signal is asserted (set low), indicating a read cycle and enabling the accessed device to drive the data bus. After 16 CLK cycles plus the internally programmed wait state period, if XRDY use is enabled for this zone, its value is then sampled on the rising edge of the clock. The transaction is extended until XRDY is detected to be high. Four CLK cycles later, the input data XD7-0 is sampled on the rising edge of the clock. One CLK cycle later, $\overline{\text{XRD}}$ is de-asserted (set high) and one CLK cycle after that, the transaction is completed by de-asserting $\overline{\text{XCSn}}$. The address is retained for two more CLK cycles after which the address lines are driven to 0.

5.0 X-Bus Extension (Continued)

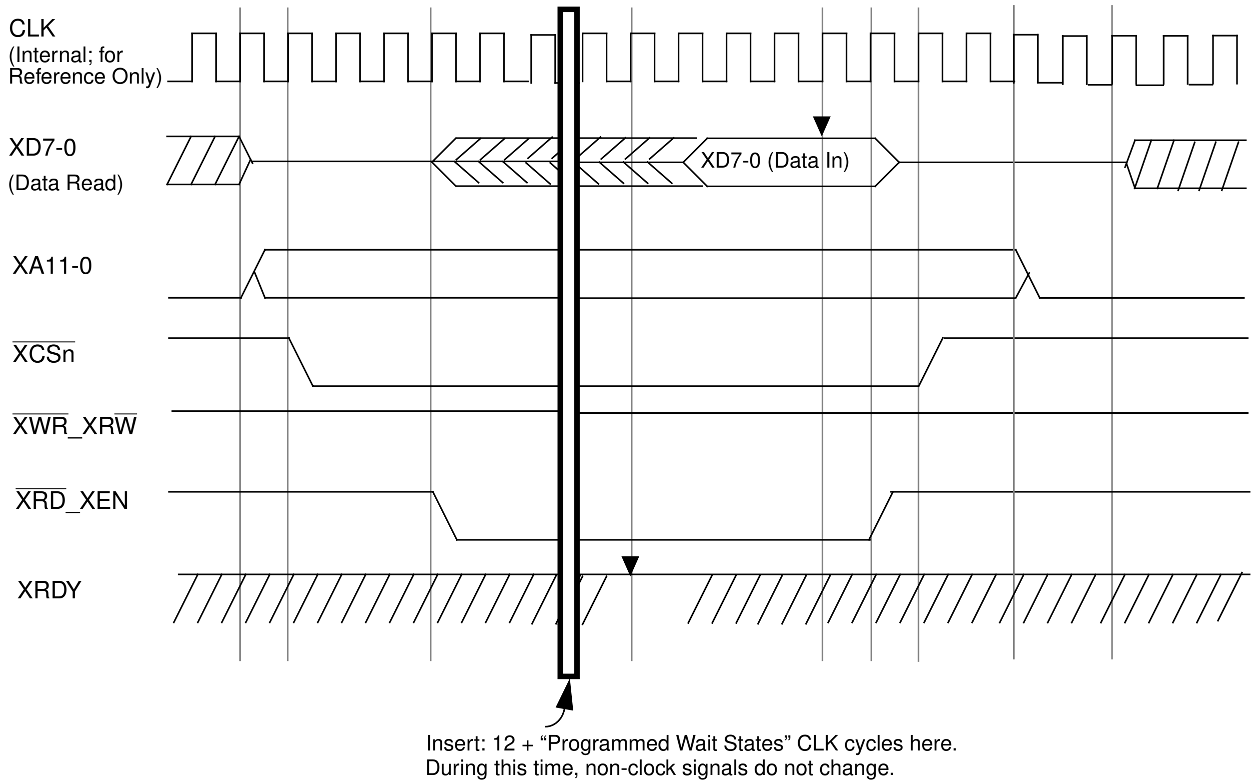


Figure 15. Mode 0, Normal Address X-Bus Transaction - Read Access Cycle

Write Transactions. When a write cycle on the LPC falls within any of the enabled decoded address ranges of the X-Bus functional block (or an indirect write is started or an X-Bus write through the ACCESS.bus is started) and the relevant $\overline{XCSn}$ is set to mode 0, a Mode 0 write cycle begins. A write cycle (see Figure 16) starts by outputting the address on address signals XA11-0 and the data signals on data pins XD7-0 on the rising edge of the clock. One CLK cycle later, a chip-select signal $\overline{XCSn}$ is asserted, where n is a chip-select number from 0 to 3, based on the address accessed and the select signal mapping. Three CLK cycles later, on the rising edge of the clock, the $\overline{XWR}$ signal is asserted (set low), indicating a write cycle and enabling the accessed device to be written. After 16 CLK cycles plus the internally programmed wait state period, if XRDY use is enabled for this zone, its value is then sampled on the rising edge of the clock. The transaction is extended until XRDY is detected to be high. Five CLK cycles later, $\overline{XWR}$ is de-asserted (set high) and one CLK cycle later, the transaction is completed by de-asserting $\overline{XCSn}$ and floating the data bus signals XD7-0. Two CLK cycles later, the address lines are driven to 0.

5.0 X-Bus Extension (Continued)

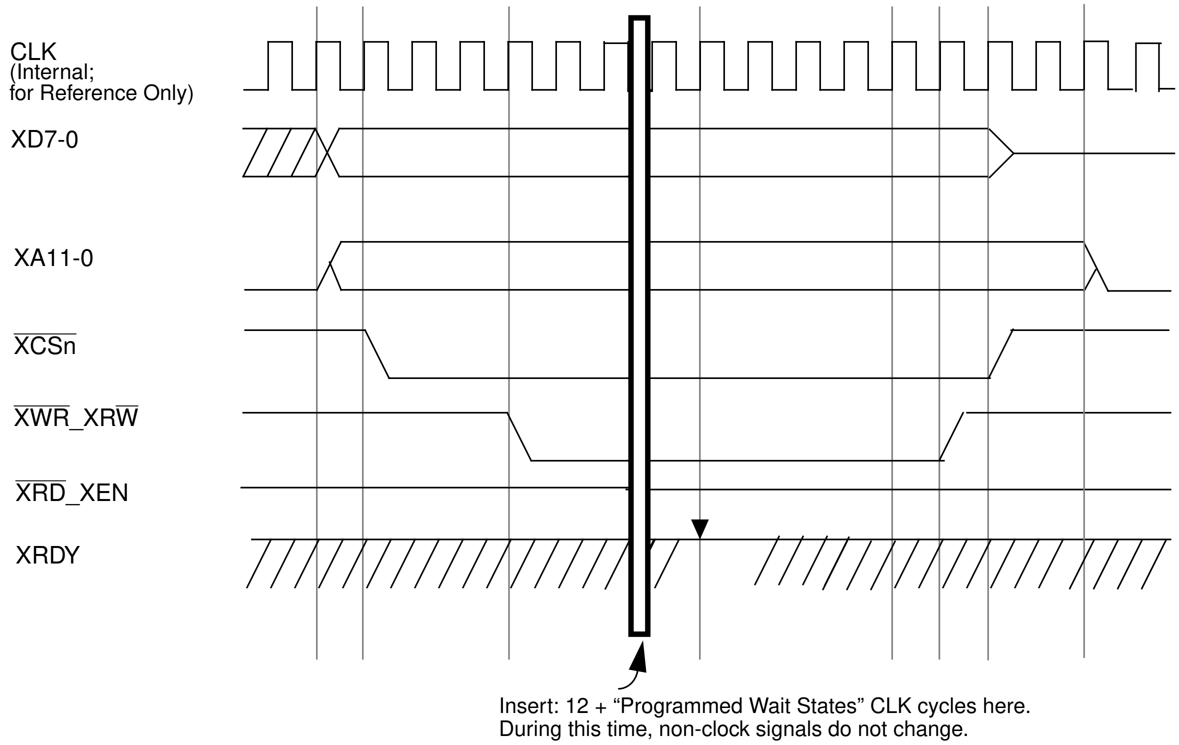


Figure 16. Mode 0, Normal Address X-Bus Transaction - Write Access Cycle

5.2.6 Mode 0, Normal Address, Fast X-Bus Transactions

The read and write transactions in Normal Address, Fast X-Bus transactions are similar to those in *Mode 0, Normal Address X-Bus Transactions* on page 95, differing only in the delay for valid data. Because Normal Address, Fast X-Bus transactions have 14 to 20 fewer cycles than Normal Address transactions, they can be used to speed up access to fast devices. The gray areas in Figures Figure 15 and Figure 16 (+ 2 CLK cycles) represent the additional cycles that Fast transactions (Figures Figure 17 and Figure 18) do not perform. This mode is selected for transactions accessing $\overline{\text{XCSn}}$ by setting TRANSMD = 0 and TRANSPD = 1 in the corresponding XZMn register.

5.0 X-Bus Extension (Continued)

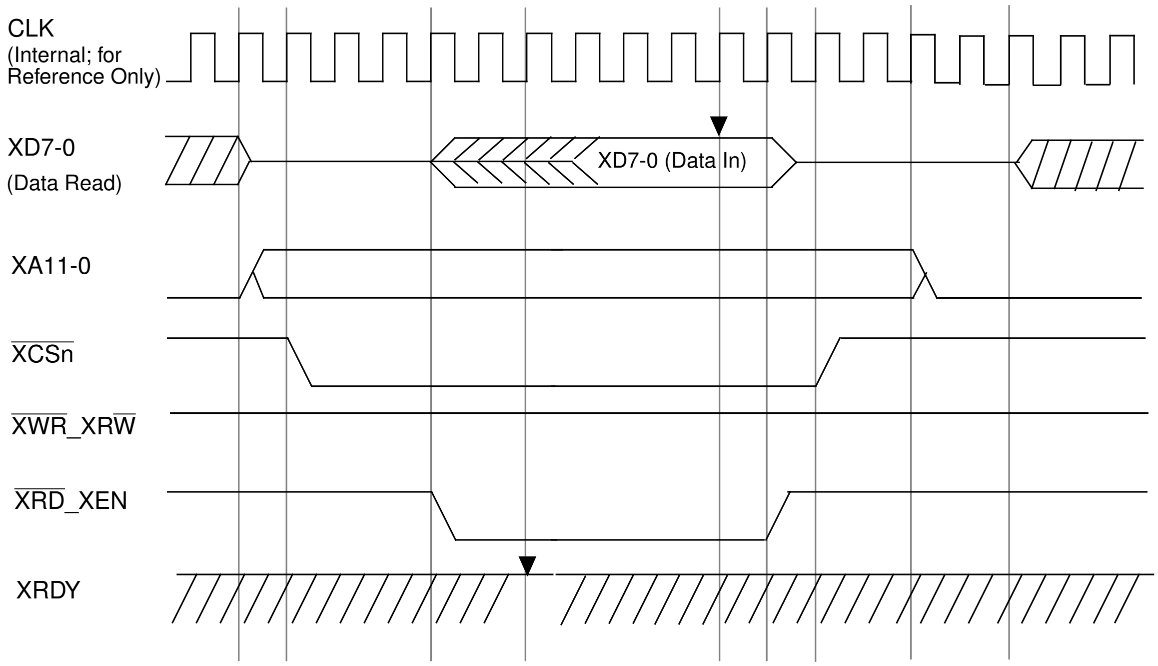


Figure 17. Mode 0, Normal Address, Fast X-Bus Transaction - Read Access Cycle

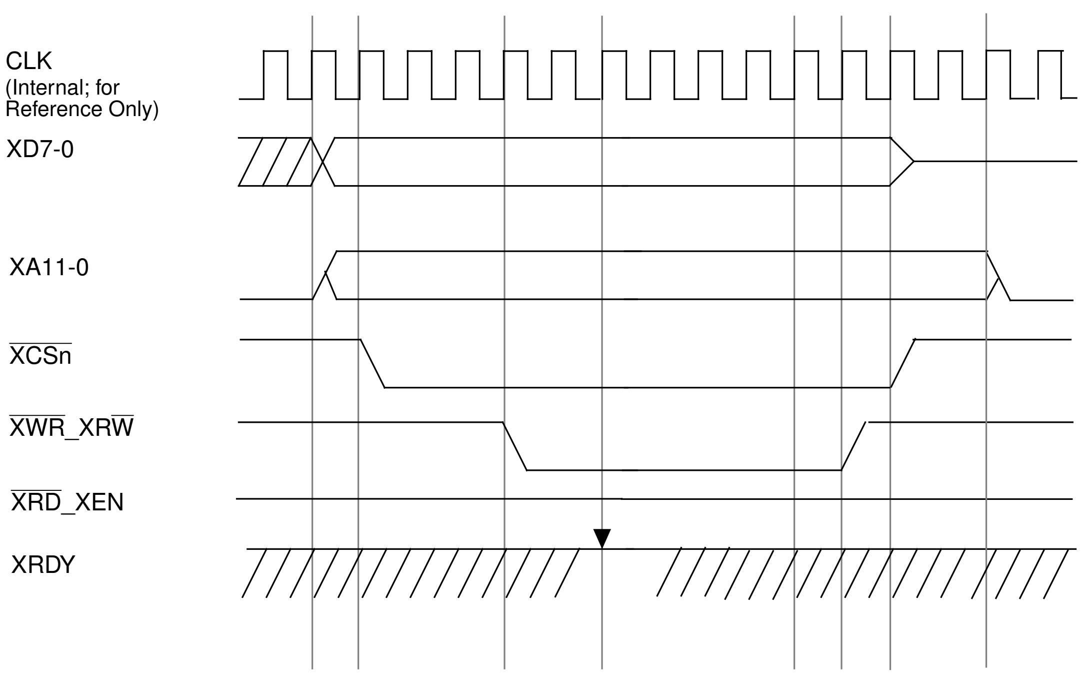


Figure 18. Mode 0, Normal Address, Fast X-Bus Transaction - Write Access Cycle

5.0 X-Bus Extension (Continued)

5.2.7 Mode 0, Normal Address, Turbo X-Bus Transactions

The read and write transactions in Normal Address, Turbo X-Bus transactions provide a lower access time than those in Mode 0, Normal Address, Fast X-Bus transactions. Because Normal Address, Turbo X-Bus transactions have seven fewer cycles than Normal Address, Fast X-Bus transactions, they efficiently access very fast devices. This mode is selected for transactions accessing $\overline{\text{XCSn}}$ by setting TRANSMD = 0 in the corresponding XZMn register and TBXCSn = 1 in the XBCNF register.

Read Transactions. When a read cycle on the LPC starts and the relevant $\overline{\text{XCSn}}$ is set to Turbo mode, a Mode 0, Normal Address, Turbo X-Bus Transaction read cycle begins. A read cycle (Figure 21, below) starts by outputting the address on address signals XA11-0 on the rising edge of the clock. During this time, the PC8741x device does not drive the data bus signals XD7-0. One CLK cycle later, a chip-select signal $\overline{\text{XCSn}}$ is asserted. One CLK cycle after that, the $\overline{\text{XRD}}$ signal is asserted (set low), indicating a read cycle and enabling the accessed device to drive the data bus. In Turbo X-Bus transactions, $\overline{\text{XRDY}}$ is ignored. Two CLK cycles later, the input data XD7-0 is sampled on the rising edge of the clock. One CLK cycle after that, $\overline{\text{XRD}}$ is de-asserted (set high) and one CLK cycle later, the transaction is completed by de-asserting $\overline{\text{XCSn}}$. The address is retained for one more CLK cycle, after which the address lines are driven to 0.

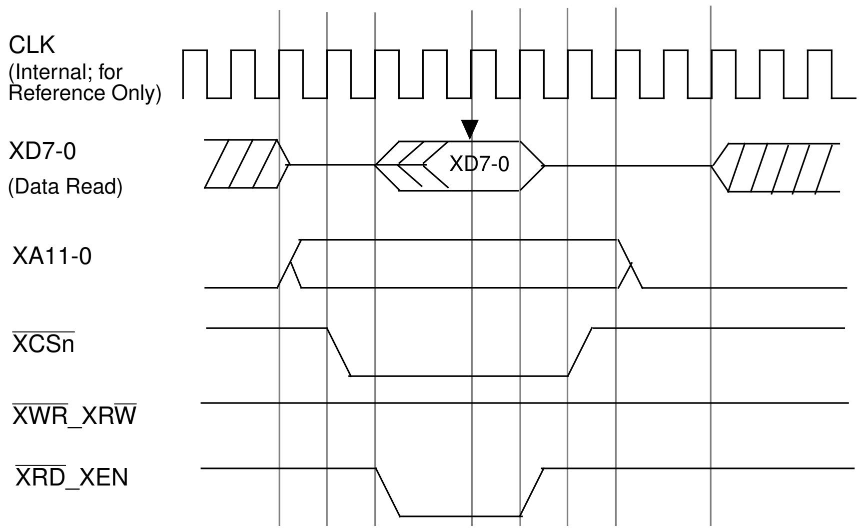


Figure 19. Mode 0, Normal Address, Turbo X-Bus Transaction - Read Access Cycle

Write Transactions. When a write cycle on the LPC starts and the relevant $\overline{\text{XCSn}}$ is set to Turbo mode, a Mode 0, Normal Address, Turbo X-Bus Transaction write cycle begins. A write cycle (Figure 22, below) starts by outputting the address on address signals XA11-0 and the data signals on data pins XD7-0 on the rising edge of the clock. One CLK cycle later, a chip-select signal $\overline{\text{XCSn}}$ is asserted. One CLK cycle after that, the $\overline{\text{XWR}}$ signal is asserted (set low), indicating a write cycle and enabling the accessed device to be written. In Turbo X-Bus transactions, $\overline{\text{XRDY}}$ is ignored. Three CLK cycles later, $\overline{\text{XWR}}$ is de-asserted (set high) and one CLK cycle after that, the transaction is completed by de-asserting $\overline{\text{XCSn}}$ and floating the data bus signals XD7-0. One CLK cycle later, the address lines are driven to 0.

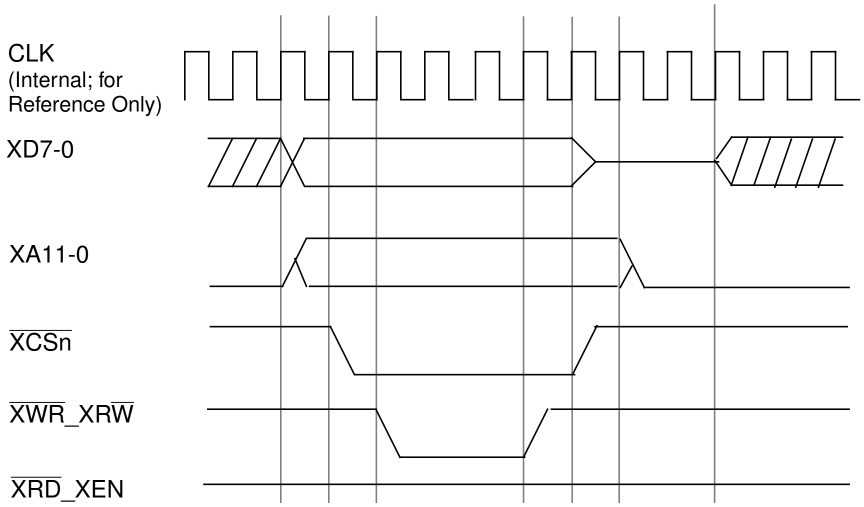


Figure 20. Mode 0, Normal Address, Turbo X-Bus Transaction - Write Access Cycle

5.0 X-Bus Extension (Continued)

5.2.8 Mode 1, Normal Address Transactions

Read and write transactions in mode 1 use an Enable signal and a R/W signal controlled protocol. At least two idle cycles are inserted at the end of each X-Bus transaction cycle (though there may be more idle cycles due to the LPC transactions). This mode is selected for transactions accessing XCSn by setting TRANSMD = 1 in the corresponding XZMn register.

Read Transactions. When a read cycle on the LPC falls within any of the enabled decoded address ranges of the X-Bus functional block (or an indirect read is started or an X-Bus read through the ACCESS.bus is started) and the relevant XCSn is set to mode 1, a Mode 1 read cycle begins. A Mode 1 read cycle (see Figure 21) begins with the de-assertion of XRD_XEN (set low). At the same time, the address is driven on the XA11-0. Ten CLK cycles later, XCSn is asserted (set low). After five CLK cycles, XRD_XEN is asserted (set high) and remains asserted for 18 cycles plus the internally programmed wait state period. During the period that XRD_XEN is asserted, the data must be driven on XD7-0 by the target device. XRD_XEN is then de-asserted for two CLK cycles. The data from XD7-0 is sampled at the rising edge of the clock one CLK cycle before XRD_XEN is de-asserted. At the end of these two CLK cycles, XCSn is set high, and after one CLK cycle, XRD_XEN is also set high. One CLK cycle later, the address lines XA11-0 are driven low.

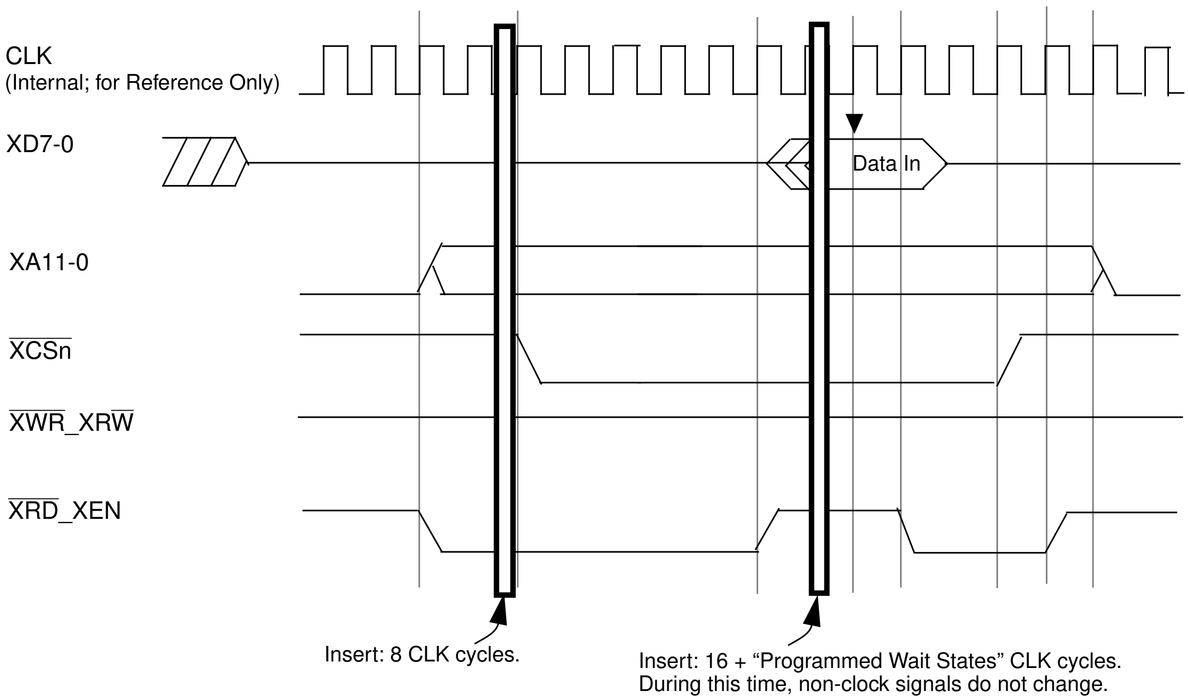


Figure 21. Mode 1, Normal Address X-Bus Transaction - Read Access Cycle

Write Transactions. When a write cycle on the LPC falls within any of the enabled decoded address ranges of the X-Bus functional block (or an indirect write is started or an X-Bus write through the ACCESS.bus is started) and the relevant XCSn is set to mode 1, a Mode 1 write cycle begins. A mode 1 write cycle (see Figure 22) begins with a de-assertion of XRD_XEN (set low). At the same time, the address is driven on the XA11-0 and the data is driven on XD7-0. After ten CLK cycles, XCSn and XWR_XRW are asserted (set low). After five CLK cycles, XRD_XEN is asserted (set high) and remains asserted for 18 cycles plus the internally programmed wait state period. XRD_XEN is then de-asserted for two CLK cycles. At the end of these two CLK cycles, XCSn is set high. After another CLK cycle, XWR_XRW and XRD_XEN are set high. Address lines XA11-0 are driven low one CLK cycle later (at the end of the transaction).

5.0 X-Bus Extension (Continued)

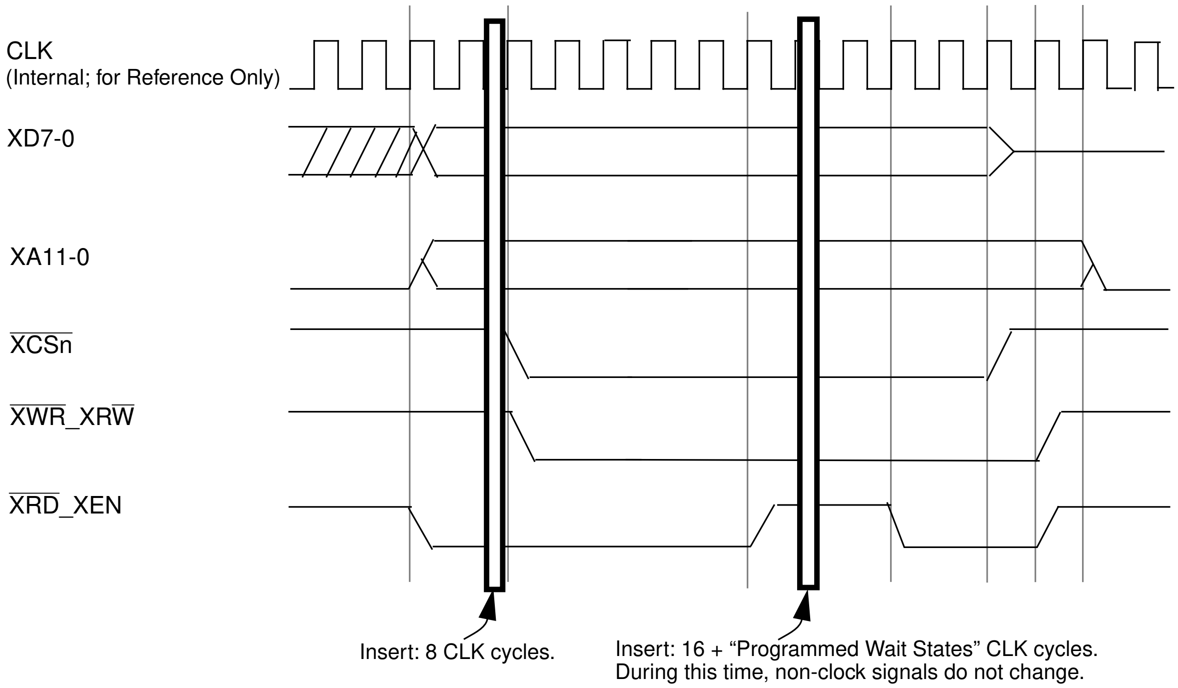


Figure 22. Mode 1, Normal Address X-Bus Transaction - Write Access Cycle

5.2.9 Latched Address Mode X-Bus Transactions

The read and write transactions in Latched Address mode are similar to those used in Normal Address mode except for the way the addresses are placed on the X-Bus. In Latched Address mode, address signals 27-0 are output using the XA signals via multiplexing over the data bus (XD7-0). The purpose of Latch control signals $\overline{\text{XSTB2-0}}$ is to separate the XA signals from the XD7-0 data bus. The $\overline{\text{XSTB2-0}}$ signals are active from the time the address signals are valid (and until the end of a transaction).

Latched address X-Bus transactions are available at two levels:

- Standard - standard access time transactions available in mode 0, mode 0 fast, and mode 1.
- Turbo - low access time transactions available in mode 0 turbo.

Standard Read Transactions. When a read cycle on the LPC falls within any of the enabled X-Bus decoded address ranges (or an indirect read is started or an X-Bus read through the ACCESS.bus is started), a read cycle begins. A read cycle starts by outputting the lower 12 address signals on address signals XA11-0 and by outputting address lines 27-20 on data signals XD7-0 on the rising edge of the clock. Two CLK cycles later, a strobe signal ($\overline{\text{XSTB2}}$) is asserted to latch the address in an external latch. Two CLK cycles later, a second set of address lines (19-12) is placed on data pins XD7-0. These can be latched by the strobe signal $\overline{\text{XSTB1}}$ asserted two cycles later on the rising edge of the clock. Two CLK cycles later, the last group of address lines (11-4) is placed on data signals XD7-0. The $\overline{\text{XSTB0}}$, asserted two cycles later on the rising edge of the clock, can be used to latch this part of the address. Two CLK cycles later on the rising edge of the clock, the PC8741x stops driving the data bus. At this point, all addresses are available either at the address outputs of the PC8741x (XA11-0) or in the three latches. The system may require only part of these addresses, depending on the size of the memory or peripheral address space. One CLK cycle later, either a chip-select signal $\overline{\text{XCSn}}$ or the enable signal $\overline{\text{XRD}}$_XEN is asserted, based on the $\overline{\text{XCSn}}$ mode setting (where n is a chip-select number from 0 to 3, based on the address accessed and the select signal mapping). From this point, the read continues as described for the Normal Address mode. $\overline{\text{XSTB2-0}}$ are de-asserted one CLK cycle after the de-assertion of $\overline{\text{XCSn}}$. At this time, the latched address becomes invalid.

5.0 X-Bus Extension (Continued)

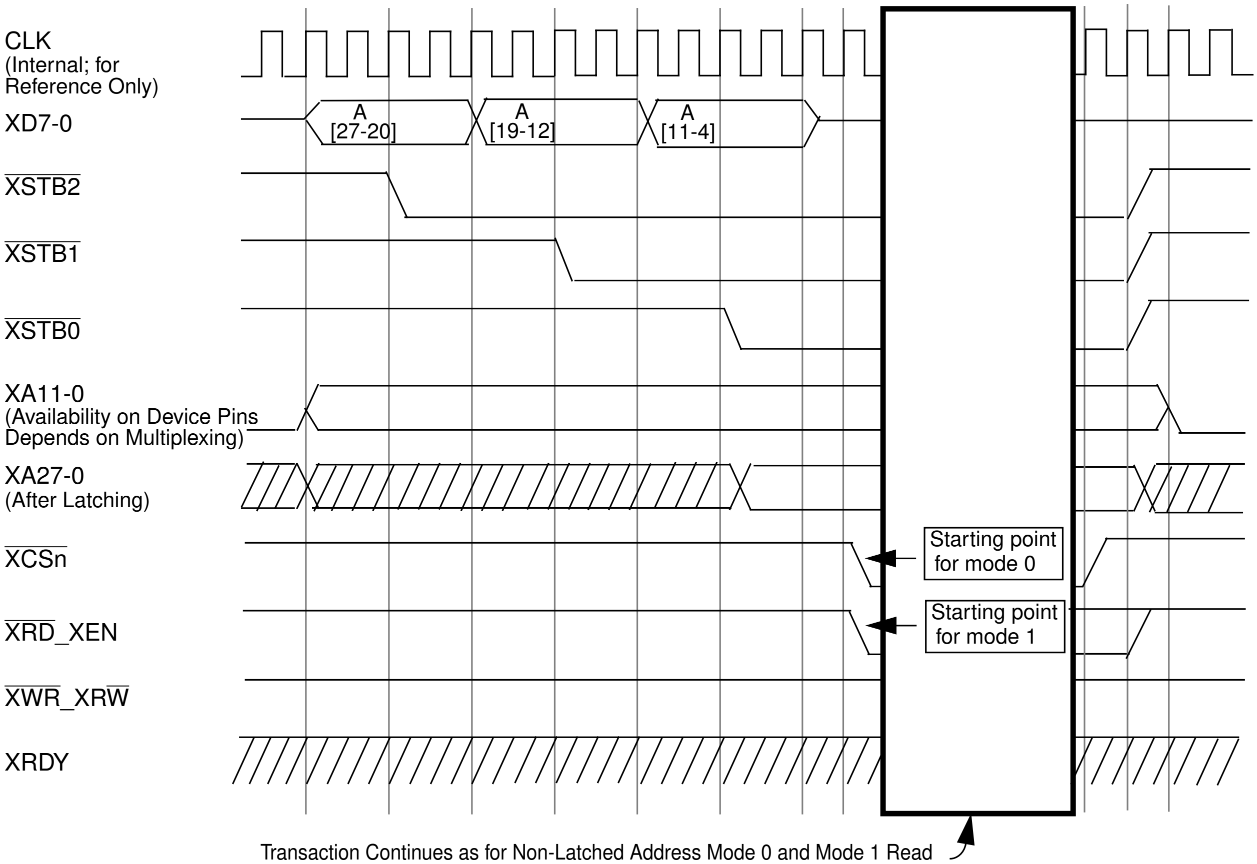


Figure 23. Standard Latched Address Mode - X-Bus Read Access Cycle

Standard Write Transactions. When a write cycle on the LPC falls within any of the enabled decoded address ranges of the X-Bus functional block (or an indirect write is started or an X-Bus write through the ACCESS.bus is started), a write cycle begins. A write cycle starts by outputting the lower 12 address signals on address signals XA11-0 and address lines 27-20 on data signals XD7-0 on the rising edge of the clock. Two CLK cycles later, a strobe signal ($\overline{\text{XSTB2}}$) is asserted to latch the address in an external latch. Two CLK cycles after that, a second set of address lines (19-12) is placed on data pins XD7-0. These can be latched by the strobe signal $\overline{\text{XSTB1}}$ asserted two cycles later on the rising edge of the clock. Two CLK cycles later, the last group of address lines (11-4) is output on the data signals XD7-0. The $\overline{\text{XSTB0}}$, asserted two CLK cycles later on the rising edge of the clock, can be used to latch this part of the address. Two CLK cycles later on the rising edge of the clock, the PC8741x outputs the data signals on data pins XD7-0. At this point, all the addresses are available either at the address outputs of the PC8741x (XA11-0) or at the outputs of the three latches. The system may require only part of these addresses, depending on the size of the memory or peripheral address space. One CLK cycle later, either a chip-select signal $\overline{\text{XCSn}}$ or the enable signal $\overline{\text{XRD}}$_XEN is asserted, based on the $\overline{\text{XCSn}}$ mode setting (where n is a chip-select number from 0 to 3, based on the address accessed and the select signal mapping). From this point, the write continues as described for the Normal Address mode. $\overline{\text{XSTB2-0}}$ are de-asserted one CLK cycle after the de-assertion of $\overline{\text{XCSn}}$. At this time, the latched address becomes invalid.

5.0 X-Bus Extension (Continued)

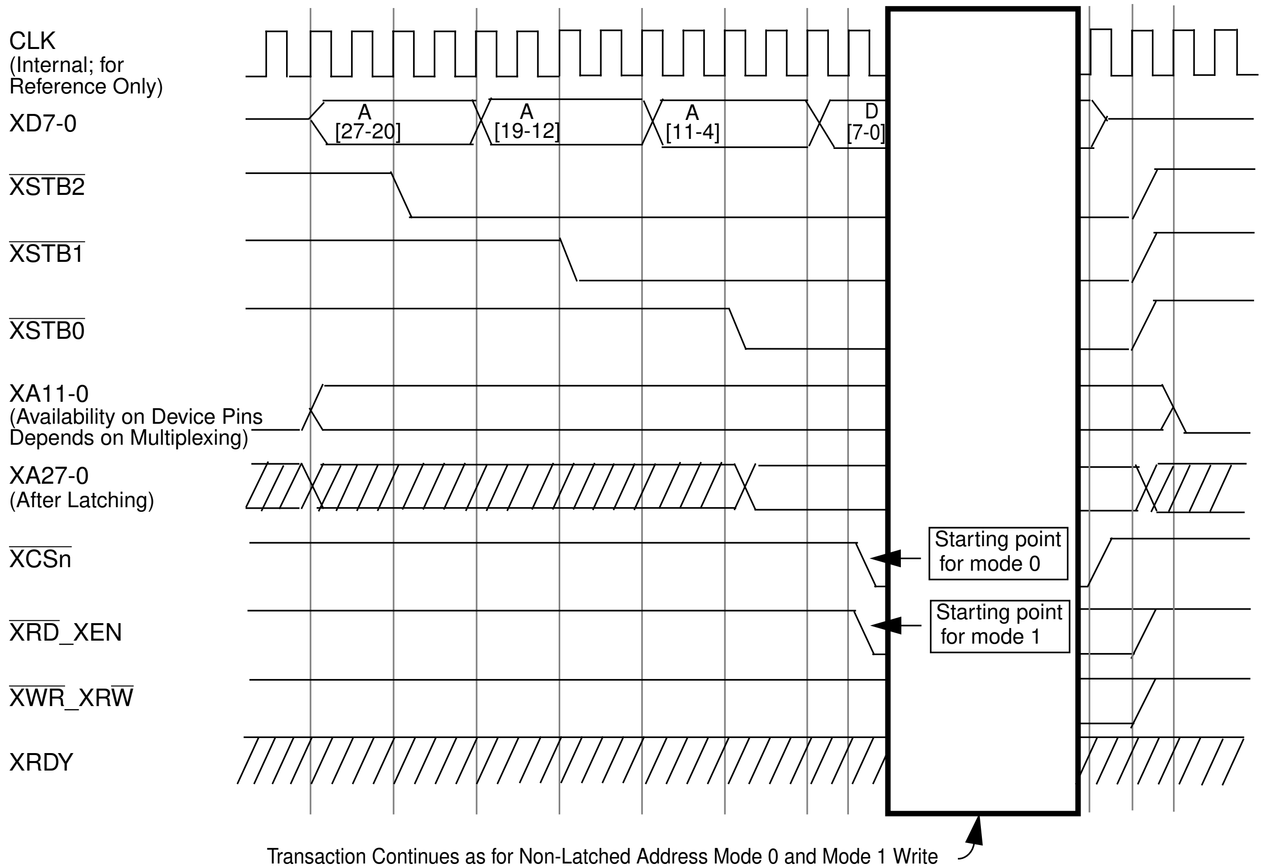


Figure 24. Standard Latched Address Mode - X-Bus Write Access Cycle

Turbo Read Transactions. A Turbo read cycle starts by outputting the lower 12 address signals on address signals XA11-0 and by outputting address lines 27-20 on data signals XD7-0 on the rising edge of the clock. One CLK cycle later, a strobe signal (XSTB2) is asserted to latch the address in an external latch. One CLK cycle after that, a second set of address lines (19-12) is placed on data pins XD7-0. These can be latched by the strobe signal XSTB1, asserted one cycle later on the rising edge of the clock. One CLK cycle later, the last group of address lines (11-4) is placed on data signals XD7-0. The XSTB0, asserted one cycle later on the rising edge of the clock, can be used to latch this part of the address. One CLK cycle later on the rising edge of the clock, the PC8741x stops driving the data bus. At this point, all addresses are available either at the address outputs of the PC8741x (XA11-0) or in the three latches. The system may require only part of these addresses, depending on the size of the memory or peripheral address space. One CLK cycle later, the chip-select signal XCSn is asserted, based on the XCSn Turbo mode setting. From this point, the read continues as described for the Normal Address Turbo transaction, Mode 0. XSTB2-0 are de-asserted one CLK cycle after the de-assertion of XCSn. At this time, the latched address becomes invalid. At the same time, the address signals XA11-0 are driven to low level.

5.0 X-Bus Extension (Continued)

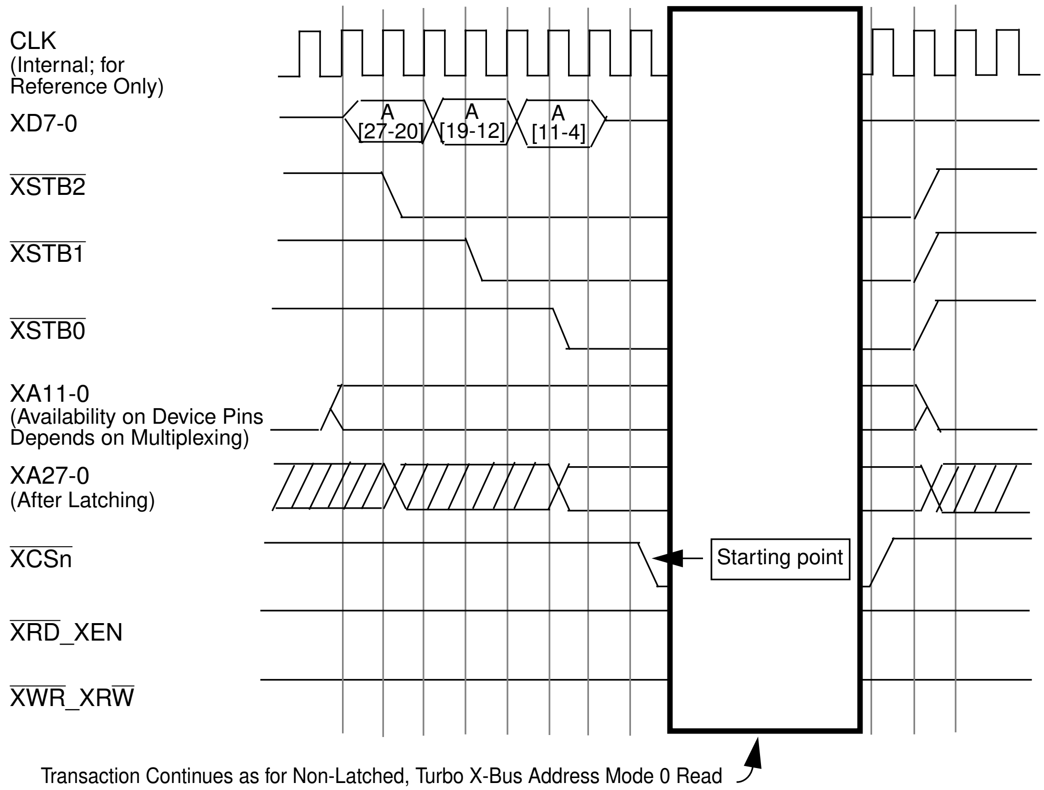


Figure 25. Turbo Latched Address Mode - X-Bus Read Access Cycle

Turbo Write Transactions. A Turbo write cycle starts by outputting the lower 12 address signals on address signals XA11-0 and by outputting address lines 27-20 on data signals XD7-0 on the rising edge of the clock. One CLK cycle later, a strobe signal (XSTB2) is asserted to latch the address in an external latch. One CLK cycle after that, a second set of address lines (19-12) is placed on data pins XD7-0. These can be latched by the strobe signal XSTB1, asserted one cycle later on the rising edge of the clock. One CLK cycle later, the last group of address lines (11-4) is output on the data signals XD7-0. The XSTB0, asserted one CLK cycle later on the rising edge of the clock, can be used to latch this part of the address. One CLK cycle later on the rising edge of the clock, the PC8741x outputs the data signals on data pins XD7-0. At this point, all the addresses are available either at the address outputs of the PC8741x (XA11-0) or at the outputs of the three latches. The system may require only part of these addresses, depending on the size of the memory or peripheral address space. One CLK cycle later, the chip-select signal XCSn is asserted, based on the XCSn Turbo mode setting. From this point, the write continues as described for the Normal Address Turbo transaction, Mode 0. XSTB2-0 are de-asserted one CLK cycle after the de-assertion of XCSn. At this time, the latched address becomes invalid. At the same time, the address signals XA11-0 are driven to low level.

5.0 X-Bus Extension (Continued)

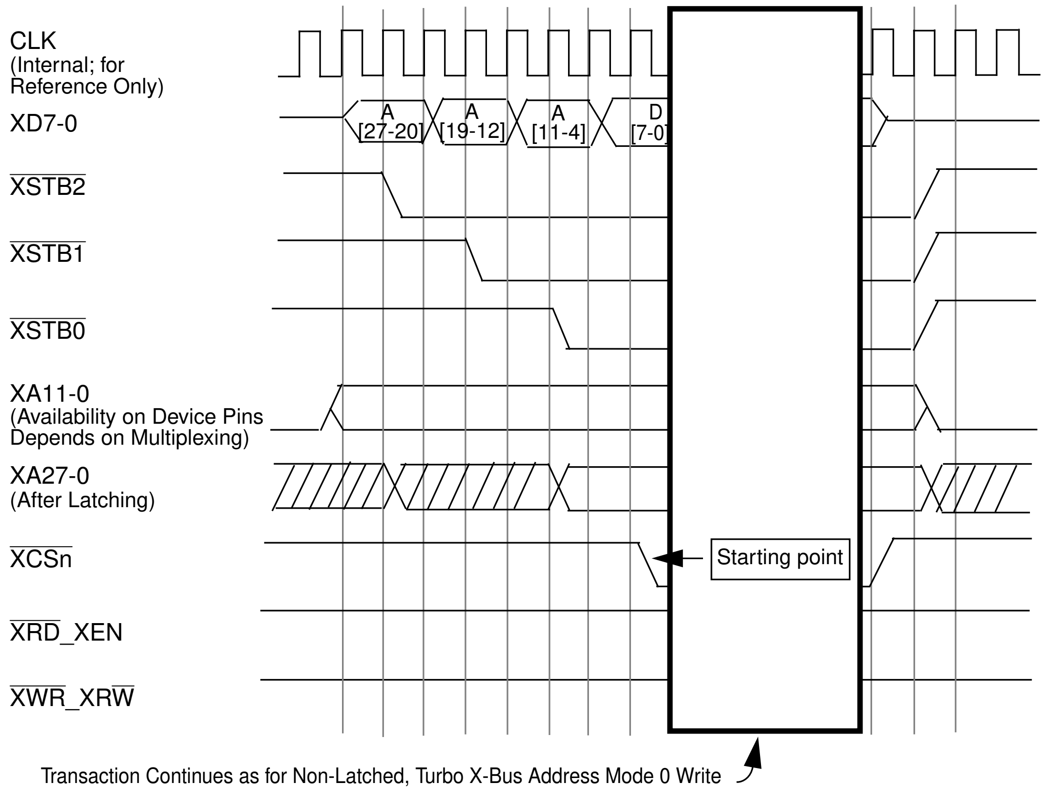


Figure 26. Turbo Latched Address Mode - X-Bus Write Access Cycle

5.3 X-BUS PROTECTION

The PC8741x devices include a mechanism to protect the settings of the X-Bus mapping functions and the contents of the memories mapped to it. This mechanism consists of three separate lock mechanisms, which must all be in use to obtain the most comprehensive protection:

- Lock the memory mapping by the host, using the lock bit in the X-Bus Memory Configuration register and X-Bus I/O Configuration register.
- Lock the bits of the X-Bus Select n Configuration register and X-Bus Mode n register, using the lock bit in the respective X-Bus Mode register.
- A Memory protection mechanism is available for $\overline{\text{XCS0}}$ and $\overline{\text{XCS1}}$. This protects the contents of up to two memory devices (one for each chip-select) for read and/or write with a granularity of 16 blocks each. This is done using the Host Access Protect registers 0 and 1 for $\overline{\text{XCS0}}$ and $\overline{\text{XCS1}}$, respectively.

Note that access protection is provided only for $\overline{\text{XCS0}}$ and $\overline{\text{XCS1}}$. Absolute access protection is only enabled by using all three lock levels.

The Memory protection mechanism pertains to the X-Bus address and the chip-select ($\overline{\text{XCS0}}$ or $\overline{\text{XCS1}}$) involved in the transaction. The size of a protected block is determined by dividing the size of each BIOS Zone by 16 (see Section 3.15.12 on page 84). Table 31 on page 106 shows the protected block size for different BIOS Zone sizes.

5.0 X-Bus Extension (Continued)

Table 31. Protected Block Size

BIOS Zone Size	BIOSIZE2-BIOSIZE0	Protected Block Size	Address Lines Used for Block Selection[1,2]
256 Kbyte	000	16 Kbyte	XA17-XA14
512 Kbyte	001	32 Kbyte	XA18-XA15
1 Mbyte	010	64 Kbyte	XA19-XA16
2 Mbyte	011	128 Kbyte	XA20-XA17
4 Mbyte	100	256 Kbyte	XA21-XA18
8 Mbyte	101	512 Kbyte	XA22-XA19
16 Mbyte	110	1 Mbyte	XA23-XA20

1. Selects the block according to the HAPINDX3-HAPINDX0 setting in the HAP0-HAP1 registers.
2. All the other address lines are ignored.

A read/write transaction to/from a protected block is not allowed to take place if, for the respective block number, the HWRP/HRDP bit is set in the HAP0 or HAP1 register (see Section 5.4.11 on page 114). This includes both memory and I/O transactions.

To prevent bypassing the protection by selecting additional non-BIOS zones to $\overline{XCS0}$ or $\overline{XCS1}$, the upper lines of the address are not used for block selection. This results in the aliasing of a protected block in each area of X-Bus memory space that has the same size as the BIOS Zone (see Figure 27).

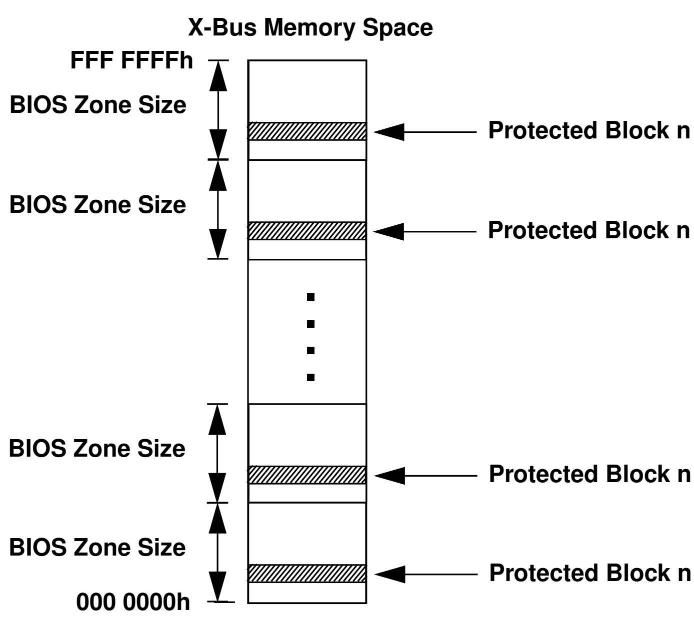


Figure 27. Protected Block Aliasing

The SMI interrupt generated on access to $\overline{XCS0}$ and $\overline{XCS1}$ may be used to allow flash updates under System Management protection.

5.0 X-Bus Extension (Continued)

5.4 X-BUS REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from a specific register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

5.4.1 X-Bus Register Map

The following table lists the X-Bus registers. All these registers are V_{SB} powered.

Offset	Mnemonic	Register Name	Type	Power Well	Section
00h	XBCNF	X-Bus Configuration Register.	R/W or RO	V_{SB}	5.4.2
01h	XZCNF0	X-Bus Select 0 Configuration Register.	R/W or RO	V_{SB}	5.4.3
02h	XZCNF1	X-Bus Select 1 Configuration Register.	R/W or RO	V_{SB}	5.4.3
04h	XIRQC	X-Bus IRQ Configuration Register.	R/W	V_{SB}	5.4.4
08h	XIMA0	X-Bus Indirect Memory Address Register 0.	R/W	V_{SB}	5.4.5
09h	XIMA1	X-Bus Indirect Memory Address Register 1.	R/W	V_{SB}	5.4.6
0Ah	XIMA2	X-Bus Indirect Memory Address Register 2.	R/W	V_{SB}	5.4.7
0Bh	XIMA3	X-Bus Indirect Memory Address Register 3.	R/W	V_{SB}	5.4.8
0Ch	XIMD	X-Bus Indirect Memory Data Register.	R/W	V_{SB}	5.4.9
0Dh	XZCNF2	X-Bus Select 2 Configuration Register.	R/W or RO	V_{SB}	5.4.3
0Eh	XZCNF3	X-Bus Select 3 Configuration Register.	R/W or RO	V_{SB}	5.4.3
0Fh	XZM0	X-Bus Select 0 Mode Register.	Varies per bit	V_{SB}	5.4.10
10h	XZM1	X-Bus Select 1 Mode Register.	Varies per bit	V_{SB}	5.4.10
11h	XZM2	X-Bus Select 2 Mode Register.	Varies per bit	V_{SB}	5.4.10
12h	XZM3	X-Bus Select 3 Mode Register.	Varies per bit	V_{SB}	5.4.10
13h	HAP0	Host Access Protect Register 0.	Varies per bit	V_{SB}	5.4.11
14h	HAP1	Host Access Protect Register 1.	Varies per bit	V_{SB}	5.4.11
Other	Reserved for National use.				

5.0 X-Bus Extension (Continued)

5.4.2 X-Bus Configuration Register (XBCNF)

This register affects the functionality mode of the X-Bus.

Power Well:V_{SB}

Location:Offset 00h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**TBXCS3**	**TBXCS2**	**TBXCS1**	**TBXCS0**	**Reserved**			**LADEN**
Reset	0	0	0	0	0	0	0	Strap

Bit	Description
7	**TBXCS3 (Turbo Transactions on $\overline{\text{XCS3}}$).** When set to 1 and mode 0 is selected (TRANSMD = 0 in the XZM3 register), enables Turbo X-Bus transactions (see Section 5.2.7 on page 99) when $\overline{\text{XCS3}}$ is accessed. The Turbo transactions are Normal Address or Latched Address (see Section 5.2.9 on page 101), according to the setting of the LADEN bit. This bit is locked by setting at least one of the LOCKXSCF bits in the XZM0-XZM3 registers. 0: Disabled (default) 1: Enabled
6	**TBXCS2 (Turbo Transactions on $\overline{\text{XCS2}}$).** When set to 1 and mode 0 is selected (TRANSMD = 0 in the XZM2 register), enables Turbo X-Bus transactions (see Section 5.2.7 on page 99) when $\overline{\text{XCS2}}$ is accessed. The Turbo transactions are Normal Address or Latched Address (see Section 5.2.9 on page 101), according to the setting of the LADEN bit. This bit is locked by setting at least one of the LOCKXSCF bits in the XZM0-XZM3 registers. 0: Disabled (default) 1: Enabled
5	**TBXCS1 (Turbo Transactions on $\overline{\text{XCS1}}$).** When set to 1 and mode 0 is selected (TRANSMD = 0 in the XZM1 register), enables Turbo X-Bus transactions (see Section 5.2.7 on page 99) when $\overline{\text{XCS1}}$ is accessed. The Turbo transactions are Normal Address or Latched Address (see Section 5.2.9 on page 101), according to the setting of the LADEN bit. This bit is locked by setting at least one of the LOCKXSCF bits in the XZM0-XZM3 registers. 0: Disabled (default) 1: Enabled
4	**TBXCS0 (Turbo Transactions on $\overline{\text{XCS0}}$).** When set to 1 and mode 0 is selected (TRANSMD = 0 in the XZM0 register), enables Turbo X-Bus transactions (see Section 5.2.7 on page 99) when $\overline{\text{XCS0}}$ is accessed. The Turbo transactions are Normal Address or Latched Address (see Section 5.2.9 on page 101), according to the setting of the LADEN bit. This bit is locked by setting at least one of the LOCKXSCF bits in the XZM0-XZM3 registers. 0: Disabled (default) 1: Enabled
3-1	**Reserved.**
0	**LADEN (Latch Address Mode Enabled).** When set to 1, enables addresses XA27-XA4 to be multiplexed with the data pins in three phases. Reset value of this bit is set according to the XCNF2 strap, sampled at V_{SB} Power-Up reset. See Section 1.4.11 on page 29 for the definition of strap setting. This bit is locked by setting at least one of the LOCKXSCF bits in the XZM0-XZM3 registers. 0: Disabled (default if XCNF2 = 0 - No BIOS) 1: Enabled (default if XCNF2 = 1 - With BIOS)

5.4.3 X-Bus Select Configuration Registers (XZCNF0 to XZCNF3)

These registers control the mapping of I/O and Memory Zones to XCSn, where n is from 0 to 3.

Power Well:V_{SB}

Location:Offset 01h (XZCNF0)

Location:Offset 02h (XZCNF1)

Location:Offset 0Dh (XZCNF2)

Location:Offset 0Eh (XZCNF3)

Type: R/W or RO

5.0 X-Bus Extension (Continued)

Bit	7	6	5	4	3	2	1	0
Name	**XRDYEN**	**WAITSEN**	**INDIRMEN**	**ZSELMAP**				
Reset	Strap	1	0	Strap				

Bit	Description
7	**XRDYEN (XRDY Enable).** Enables the use of XRDY input for the zones mapped to $\overline{XCSn}$. The reset value of this bit depends on the setting of XCNF2 and XCNF0 straps, sampled at V_{SB} Power-Up reset. 0: Disabled (default for XZCNF1-3; default for XZCNF0 if XCNF0 = 0 or XCNF2 = 0) 1: Enabled (default for XZCNF0 if XCNF0 = 1 and XCNF2 = 1)
6	**WAITSEN (Wait States Enable).** This bit controls the number of wait states added to an X-Bus transaction. If the TRANSPD bit in the XZM0 to XZM3 registers is set, the setting of WAITSEN is ignored (wait states are disabled). 0: Wait states disabled 1: Eight wait states (CLK cycles) enabled (default)
5	**INDIRMEN (Indirect Memory Access Enable).** Enables indirect memory access mechanism to generate memory transactions through $\overline{XCSn}$. 0: Disabled (default) 1: Enabled
4-0	**ZSELMAP (Zone Select Mapping).** UDIZ = User-Defined I/O Zone. MEM = User-Defined Memory Zone. - = $\overline{XCSn}$ does not respond to this zone decode. + = $\overline{XCSn}$ responds to this zone decode and is influenced by its setting.

Bits 4 3 2 1 0	UDIZ0	UDIZ1	UDIZ2	UDIZ3	TST	BIOS0	BIOS1	MEM0	MEM1	
0 0 0 0 0:	-	-	-	-	-	-	-	-	-	(default for XZCNF1-3; default for XZCNF0 if XCNF2 = 0)
0 0 0 0 1:	-	-	-	-	-	+	-	-	-	(default for XZCNF0 if XCNF2 = 1)
0 0 0 1 0:	+	-	-	-	-	+	-	-	-	
0 0 0 1 1:	+	+	-	-	-	+	-	-	-	
0 0 1 0 0:	+	+	+	-	-	+	-	-	-	
0 0 1 0 1:	+	+	+	+	-	+	-	-	-	
0 0 1 1 0:	-	-	-	-	+	+	-	-	-	
0 0 1 1 1:	+	+	+	-	+	+	-	-	-	
0 1 0 0 0:	+	+	+	+	+	+	-	-	-	
0 1 0 0 1:	+	-	-	-	-	-	-	-	-	
0 1 0 1 0:	+	-	-	-	+	-	-	-	-	
0 1 0 1 1:	+	+	-	-	-	-	-	-	-	
0 1 1 0 0:	+	+	+	-	-	-	-	-	-	
0 1 1 0 1:	+	+	+	+	-	-	-	-	-	
0 1 1 1 0:	-	-	-	-	+	-	-	-	-	
0 1 1 1 1:	+	+	+	+	+	-	-	-	-	
1 0 0 0 0:	+	+	+	+	+	-	-	+	-	
1 0 0 0 1:	+	-	-	-	-	-	-	+	+	
1 0 0 1 0:	-	-	-	-	-	-	-	+	-	
1 0 0 1 1:	+	+	-	-	-	-	-	+	-	
1 0 1 0 0:	+	+	+	-	-	-	-	+	+	
1 0 1 0 1:	+	+	+	+	-	-	+	+	-	
1 0 1 1 0:	-	-	-	-	+	-	+	+	+	
1 0 1 1 1:	+	+	+	+	+	+	+	+	+	
1 1 0 0 0:	-	-	-	-	-	-	-	+	+	
Others:	Reserved									

5.0 X-Bus Extension (Continued)

5.4.4 X-Bus IRQ Configuration Register (XIRQC)

This register defines the functionality of the XIRQ signal.

Power Well: V_{SB}

Location: Offset 04h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**IRQPOLINV**	**IRQEN**	**IRQPOL**	**PWUREN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3	**IRQPOLINV (IRQ Polarity Inversion).** This bit controls the polarity of the IRQ signal sent through the IRQ Serializer (see Table 32). This bit is reset to ‘0’.
2	**IRQEN (IRQ Enable).** When this bit is set, it enables the interrupt. The bit is ignored when the IRQ is mapped to zero (see Section 3.2.3 on page 40). 0: Disabled (default) 1: Enabled
1	**IRQPOL (IRQ Polarity).** This bit specifies the active level of the incoming IRQ signal. 0: Active low (default) 1: Active high
0	**PWUREN (Power-Up Request Enable).** When this bit is set, an XIRQ event is routed to the Modules IRQ Wake-Up Event (bit MOD_IRQ_STS in the GPE1_STS_3 register; see Section 9.4.11 on page 211). 0: Disabled (default) 1: Enabled

Table 32. Serial IRQ vs. XIRQ Polarity

IRQPOLINV	IRQPOL	Serial IRQ
0	0	XIRQ
0	1	$\overline{\text{XIRQ}}$
1	0	$\overline{\text{XIRQ}}$
1	1	XIRQ

5.0 X-Bus Extension (Continued)

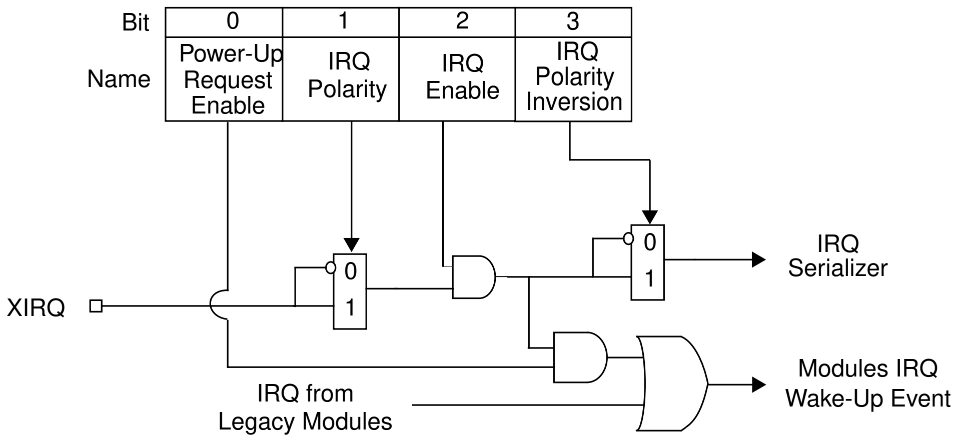


Figure 28. Functional Illustration of X-Bus IRQ Configuration Register

5.4.5 X-Bus Indirect Memory Address Register 0 (XIMA0)

This register holds addresses 7-0 for indirect read or write transactions to memory or I/O.

Power Well:V_{SB}

Location:Offset 08h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**X-Bus Indirect Memory or I/O Address 7-0**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**X-Bus Indirect Memory or I/O Address 7-0.**

5.4.6 X-Bus Indirect Memory Address Register 1 (XIMA1)

This register holds addresses 15-8 for indirect read or write transactions to memory or I/O.

Power Well:V_{SB}

Location:Offset 09h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**X-Bus Indirect Memory or I/O Address 15-8**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**X-Bus Indirect Memory or I/O Address 15-8.**

5.0 X-Bus Extension (Continued)

5.4.7 X-Bus Indirect Memory Address Register 2 (XIMA2)

This register holds addresses 23-16 for indirect read or write transactions to the memory.

Power Well:V_{SB}

Location:Offset 0Ah

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**X-Bus Indirect Memory Address 23-16**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**X-Bus Indirect Memory Address 23-16.**

5.4.8 X-Bus Indirect Memory Address Register 3 (XIMA3)

This register holds addresses 31-24 for indirect read or write transactions to the memory.

Power Well:V_{SB}

Location:Offset 0Bh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**X-Bus Indirect Memory Address 31-24**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**X-Bus Indirect Memory Address 31-24.**

5.4.9 X-Bus Indirect Memory Data Register (XIMD)

This register holds data bits 7-0 for indirect read or write transactions to memory or I/O.

Power Well:V_{SB}

Location:Offset 0Ch

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**X-Bus Indirect Memory or I/O Data 7-0**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**X-Bus Indirect Memory or I/O Data 7-0.**

5.0 X-Bus Extension (Continued)

5.4.10 X-Bus Select Mode Register (XZM0 to XZM3)

These registers control the operation mode of chip select $\overline{XCSn}$, where n is from 0 to 3.

Power Well:V_{SB}

Location:Offset 0Fh (XZM0)

Location:Offset 10h (XZM1)

Location:Offset 11h (XZM2)

Location:Offset 12h (XZM3)

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCKXSCF**	**WRSTAT**	**SMIWREN**	**XCSPOL**	**XCSTIM**		**TRANSMD**	**TRANSPD**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W1S	**LOCKXSCF (X-Bus Select Configuration Lock).** Locks the configuration registers of the respective $\overline{XCSn}$ signal (both XZCNFn register and XZMn register) by disabling writing to all their bits (including to itself). An exception to this is the WRSTAT bit of the XZMn register. In addition, it locks the bits in the XBCNF register. Once set, this bit can be cleared either by the V_{DD} Power-Up reset (or Hardware reset) or by the V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKX bit in the ACBLKCTL register (**PC87417**). 0: Lock Disabled (default) 1: Lock Enabled, protecting the configuration for this chip select
6	R/W1C	**WRSTAT (Write Status).** This bit is set if a write to the chip select occurred. Writing 1 to this bit clears it to 0. WRSTAT is not locked by the LOCKXSCK bit. 0: No write detected (default) 1: Write to the chip select detected
5	R/W or RO	**SMIWREN (SMI-on-Write Enable).** Enables the generation of an SMI, if the WRSTAT bit is set by the occurrence of a write to the chip select. 0: SMI Disabled (default) 1: SMI Enabled
4	R/W or RO	**XCSPOL (XCS Polarity Control).** Selects the polarity of the $\overline{XCSn}$ signal. 0: Active low - idle = 1, select = 0 (default) 1: Active high - idle = 0, select = 1
3-2	R/W or RO	**XCSTIM (XCS Timing Control).** Selects the timing of the $\overline{XCSn}$ signal during read and write transactions in mode 0. If TRANSMD bit is set to mode 1, the value of these bits is ignored and they are treated as ‘00’. **Bits** **3 2 Function** 0 0: Normal $\overline{XCSn}$ timing for both read and write cycles (default) 0 1: Normal $\overline{XCSn}$ timing during write cycles; $\overline{XRD}$_XEN timing for $\overline{XCSn}$ during read cycles 1 0: Normal $\overline{XCSn}$ timing during read cycles; $\overline{XWR}$_XR$\overline{W}$ timing for $\overline{XCSn}$ during write cycles 1 1: $\overline{XRD}$_XEN timing for $\overline{XCSn}$ during read cycles; $\overline{XWR}$_XR$\overline{W}$ timing for $\overline{XCSn}$ during write cycles
1	R/W or RO	**TRANSMD (X-Bus Transaction Mode).** Selects the X-Bus transaction mode pertaining to the behavior of the $\overline{XWR}$_XR$\overline{W}$ and $\overline{XRD}$_XEN signals during a transaction. 0: Mode 0 - This is an ISA-like mode. When accessing the $\overline{XCSn}$, $\overline{XWR}$_XR$\overline{W}$ functions as an active low write signal and $\overline{XRD}$_XEN functions as an active low read signal (default) 1: Mode 1 - In this mode, when accessing the $\overline{XCSn}$, $\overline{XWR}$_XR$\overline{W}$ functions as a read/write signal (high for a read transaction and low for a write transaction) and $\overline{XRD}$_XEN functions as an active high enable signal

5.0 X-Bus Extension (Continued)

Bit	Type	Description
0	R/W or RO	**TRANSPD (X-Bus Transaction Speed).** When set to 1, removes the additional cycles from mode 0 read and write transactions. In this situation, the setting of WAITSEN bit in the XZCNF0 to XZCNF3 registers is ignored (wait states are disabled). 0: Sixteen additional CLK cycles (apart from the programmed number of wait states) are inserted into mode 0 read and write transactions when accessing the $\overline{XCSn}$ (default) 1: No CLK cycles are inserted

5.4.11 Host Access Protect Register (HAP0 to HAP1)

HAP0 and HAP1 registers hold the read/write protection and lock control bits for access control to $\overline{XCS0}$ and $\overline{XCS1}$, respectively. Each register defines the access rights for a group of 16 blocks of the related chip select (see Section 5.3 on page 105 for more information on how to define these blocks). Each block is protected by three bits, which are accessed through the block number written into the Host Access Protection Index field.

The lock bit for each block is cleared either by reset or by writing a ‘0’ through the ACCESS.bus (**PC87417**). When a lock bit is cleared, the related write-protect flag is set and the read-protect flag is cleared.

Power Well:V_{SB}

Location:Offset 13h and 14h

Type: Varies per bit

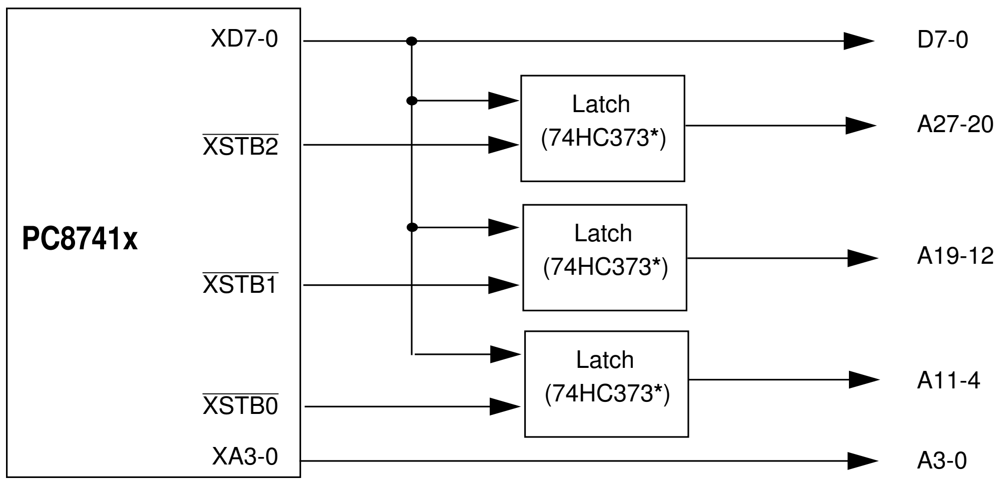
Bit	7	6	5	4	3	2	1	0
Name	**HAPINDX**				**INDXWR**	**LOCKXHP**	**HWRP**	**HRDP**
Reset	0	0	0	0	0	0	1	0

Bit	Type	Description
7-4	R/W	**HAPINDX (Host Access Protection Index).** Holds the index for the block number to be accessed by the other fields in this register. All blocks are 16 KByte up to 1 MByte in size (see Section 5.3 on page 105). 0000b - 1111b - index for block numbers of 0-15, respectively (0000b = default).
3	WO	**INDXWR (Index Write).** Indicates an index write transaction for which the value of bits 2-0 are ignored (not written). This bit always returns ‘0’ when read. 0: Index and Data write transaction (writes bits 2-0 according to the newly written index); (default) 1: Index update write transaction (bits 2-0 are not updated by this write)
2	R/W1S	**LOCKXHP (Lock Host Protection).** When set to ‘1’ through the LPC bus, this bit locks itself and the two HWRP and HRDP protection bits by disabling writing to them. The block number these three bits relate to is pointed to by the Index field. Once set, this bit can be cleared either by the V_{DD} Power-Up reset (or Hardware reset) or by the V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKX bit in the ACBLKCTL register (**PC87417**). This bit may be set or reset through the ACCESS.bus (**PC87417**), regardless of its value (it is not self-locking). 0: Changes to protection bits (2-0) for this block are enabled (default) 1: Protection bits (2-0) for this block are locked and their values cannot be changed
1	R/W or RO	**HWRP (Host Write Protection).** This bit prevents writes to a block, thus preventing programming or erasing of the flash memory connected to the $\overline{XCSn}$. The block number affected by this field is the one pointed to by the Index field. 0: Host writes to this block are allowed 1: Host writes to this block are inhibited (default)
0	R/W or RO	**HRDP (Host Read Protection).** This bit prevents reads from a block, thus protecting the contents of the flash memory connected to the $\overline{XCSn}$. The block number affected by this field is the one pointed to by the Index field. 0: Host reads from this block are allowed (default) 1: Host reads from this block are inhibited

5.0 X-Bus Extension (Continued)

5.5 USAGE HINTS

1. Bear in mind the following system design hints for asynchronous X-Bus use:
   - The chip-select signal must be used as a qualifier with the address when partial address decoding is in use for multiple device access control.
   - In read cycles, the system may drive the data until the read signal $\overline{\text{XRD}}$_XEN is de-asserted to guarantee the proper PC8741x sampling.
   - In write cycles, use either the falling or rising edge of the write control signal ($\overline{\text{XWR}}$_XR$\overline{\text{W}}$) to latch the data in the device.
2. Address multiplexing on XD7-0 and strobe signals $\overline{\text{XSTB2-0}}$ are designed for glueless interface with off-chip latch components (see the example in Figure 29).



* - For mode 0, mode 0 fast, and mode 1, use 74HC373
- For mode 0 turbo, use 74VHC373
- For 5V-powered X-Bus devices, use 74HCT/VHCT373, which is also powered by the 5V supply.

Figure 29. Latched Mode X-Bus Transaction External Logic

5.0 X-Bus Extension (Continued)

5.6 X-BUS EXTENSION REGISTER BITMAP

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	XBCNF	TBXCS3	TBXCS2	TBXCS1	TBXCS0	Reserved			LADEN
01h	XZCNF0	XRDYEN	WAITSEN	INDIRMEN	ZSELMAP				
02h	XZCNF1	XRDYEN	WAITSEN	INDIRMEN	ZSELMAP				
04h	XIRQC	Reserved				IRQPOLINV	IRQEN	IRQPOL	PWUREN
08h	XIMA0	X-Bus Indirect Memory Address 7-0							
09h	XIMA1	X-Bus Indirect Memory Address 15-8							
0Ah	XIMA2	X-Bus Indirect Memory Address 23-16							
0Bh	XIMA3	X-Bus Indirect Memory Address 31-24							
0Ch	XIMD	X-Bus Indirect Memory or I/O Data 7-0							
0Dh	XZCNF2	XRDYEN	WAITSEN	INDIRMEN	ZSELMAP				
0Eh	XZCNF3	XRDYEN	WAITSEN	INDIRMEN	ZSELMAP				
0Fh	XZM0	LOCKXSCF	WRSTAT	SMIWREN	XCSPOL	XCSTIM		TRANSMD	TRANSPD
10h	XZM1	LOCKXSCF	WRSTAT	SMIWREN	XCSPOL	XCSTIM		TRANSMD	TRANSPD
11h	XZM2	LOCKXSCF	WRSTAT	SMIWREN	XCSPOL	XCSTIM		TRANSMD	TRANSPD
12h	XZM3	LOCKXSCF	WRSTAT	SMIWREN	XCSPOL	XCSTIM		TRANSMD	TRANSPD
13h	HAP0	HAPINDX				INDXWR	LOCKXHP	HWRP	HRDP
14h	HAP1	HAPINDX				INDXWR	LOCKXHP	HWRP	HRDP
Other	Reserved for National use								

6.0 ACCESS.bus Interface

This section is relevant only for the PC87413 and PC87417. In the PC87414 and PC87416, all ACCESS.bus Interface bits and signals that influence other modules are at their default value.

The ACCESS.bus Interface is a two-wire synchronous serial interface compatible with the ACCESS.bus (*Specification Rev. 3.0 Sep. 1995*) and with Intel's SMBus (*Specification Rev 1.1 Dec. 11, 1998*). The ACCESS.bus Interface acts as a slave device controlled by a bus master. The ACCESS.bus Interface uses proprietary commands for AdvancedI/O access, compatible with the Physical, Data Link and Transport layers defined by the above specifications.

This chapter describes the ACCESS.bus Interface functional block.

6.1 OVERVIEW

The ACCESS.bus protocol uses a two-wire interface for bidirectional communication between the devices connected to the bus. The two interface lines are the Serial Data Line (ACBDAT) and the Serial Clock Line (ACBCLK). These open-drain lines must be connected to a positive supply via an internal or an external pull-up resistor and remain high when the bus is idle.

Each device connected to the bus has a unique address and can operate as a transmitter or a receiver (though some peripherals are only receivers).

During data transactions, the master device initiates the transaction with an attached peripheral, generates the clock signal and terminates the transaction. When the master sends a slave address or data, the peripheral behaves as a receiver. When the slave responds and sends data to the master, the peripheral behaves as a transmitter.

6.2 FUNCTIONAL DESCRIPTION

6.2.1 Bus Signals

ACBDAT and ACBCLK Signals

The ACBDAT and ACBCLK are open-drain signals. The device permits the user to define whether to enable or disable the internal pull-up of these two signals (at reset, the internal pull-up is disabled).

Clock Frequency

The PC8741x device is a slave device that synchronizes to the clock frequency of the ACCESS.bus clock. The maximum clock frequency is 100 kHz and the minimum is 10 kHz (limited by the 50 μsec maximum high time required by the standards to detect a Bus Idle condition). However, since the PC8741x device is a slave device, the minimum clock frequency limitation is ignored. The clock low period may be extended by stall periods initiated by the ACCESS.bus Interface (see Section 11.5.6 on page 246).

6.2.2 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (ACBCLK). Consequently, throughout the high period of the clock, the data must remain stable (see Figure 30). Any change in mid-transaction on the ACBDAT line during the high period of the ACBCLK aborts the transaction and releases the ACBDAT signal (to high level), thus generating Negative Acknowledge (NACK) cycles (see Section 6.2.4 on page 118). In addition, the PC8741x device sets the BUSERR bit in the ACBCST register (see Section 6.3.2 on page 127). Data must be driven onto the bus only during the low ACBCLK period. This protocol permits a single data line to transfer both command/control information and data, using the synchronous serial clock.

During each clock cycle, while the slave handles the received data or prepares the data to be sent, it can stall the master. The slave can do this for each bit transferred or on a byte boundary by holding ACBCLK low to extend the clock-low period. Typically, slaves extend the first clock cycle of a transfer if a byte written has not yet been stored or if the byte to be read is not yet ready. Some microcontroller-based masters with limited hardware support for ACCESS.bus extend the access after each bit, thus allowing the software to handle the bit.

Each data transaction is composed of a Start Condition, a number of byte transfers (defined by the protocol) and a Stop Condition to terminate the transaction. Each byte (eight bits) is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

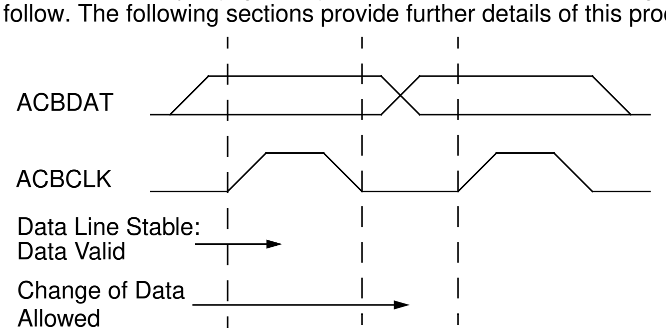


Figure 30. Data Bit Transfer

6.0 ACCESS.bus Interface (Continued)

6.2.3 Start and Stop Conditions

The ACCESS.bus master generates Start and Stop Conditions (control codes). After a Start Condition is generated, the bus remains busy until after a Stop Condition is generated. A high-to-low transition of the data line (ACBDAT) while the clock (ACBCLK) is high indicates a Start Condition. A low-to-high transition of the ACBDAT line while the ACBCLK is high indicates a Stop Condition (Figure 31).

A transaction begins with a Start Condition and ends with a Stop Condition. However, a Restart Condition can be generated in the middle of a transaction (without the need for a Stop Condition) in order to change the direction of data transfer (from address/data write to data read).

Before a Start condition, any changes of the ACBDAT line outside the high period of the ACBCLK are ignored. A Stop condition encountered in mid-transaction on the ACBDAT line aborts the transaction. The PC8741x device releases the ACBDAT signal (to high level), thus generating Negative Acknowledge (NACK) cycles (see Section 6.2.4). In addition, the PC8741x device sets the BUSERR bit in the ACBCST register (see Section 6.3.2 on page 127).

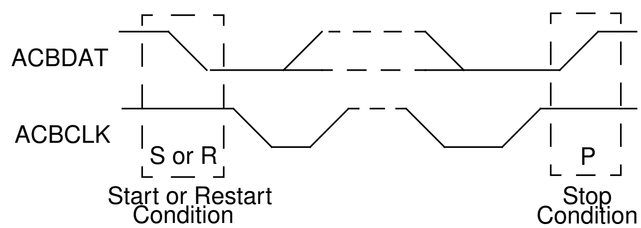


Figure 31. Start, Restart and Stop Conditions

6.2.4 Acknowledge (ACK) Cycle

The ACK cycle involves two signals: the ACK clock pulse, sent by the master after each byte transferred, and the ACK data signal, sent by the receiving device (see Figure 32).

The master generates the ACK clock pulse on the ninth clock pulse of the byte transfer. The transmitter (master or slave) releases the ACBDAT line (allows it to go high) to allow the receiver to send the ACK signal. The receiver must pull down the ACBDAT line during the ACK clock pulse, signalling that it correctly received the previous data byte and is ready to receive the next byte. If the receiver does not pull the ACBDAT line (leaves it high), the transmitter identifies it as a NACK condition (see Section 6.2.5). Figure 33 illustrates the ACK cycle.

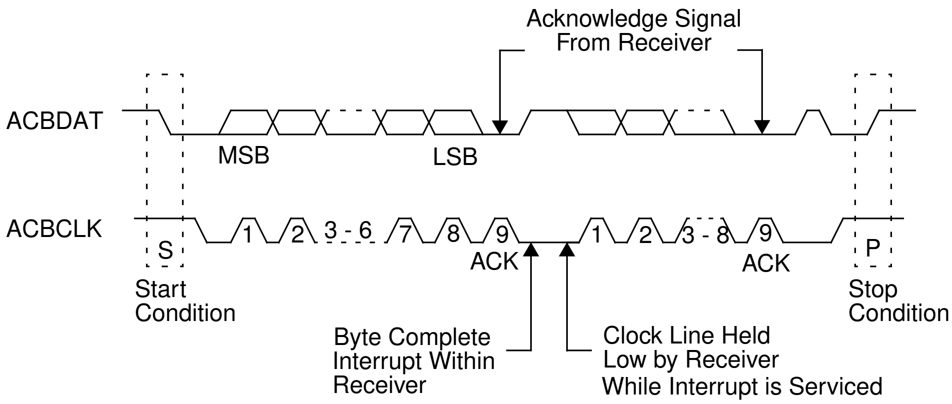


Figure 32. ACCESS.bus Data Transaction with Acknowledge

6.0 ACCESS.bus Interface (Continued)

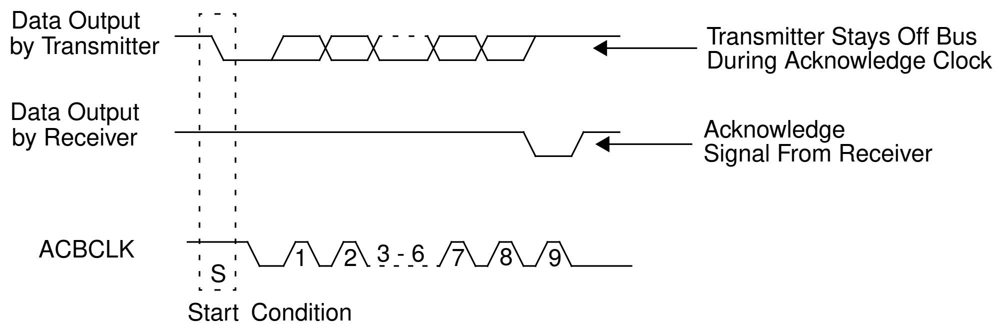


Figure 33. ACCESS.bus Acknowledge Cycle

6.2.5 Acknowledge after Every Byte Rule

According to this rule, the master generates an acknowledge clock pulse after each byte transfer and the receiver (master or slave) sends an acknowledge signal after every byte received. There are two exceptions to this rule:

- When the master is the receiver, it must indicate to the slave transmitter the end of the expected data by not acknowledging (NACK) the last byte clocked out of the slave. This negative acknowledge still includes the acknowledge clock pulse (generated by the master), but the ACBDAT line is not pulled down.
- When a problem has occurred in the slave receiver, it sends a NACK to indicate that it did not accept the previous data byte or cannot accept additional data bytes.

The NACK indicates an error in data reception (by slave or master) and a request to repeat the ACCESS.bus transaction.

6.2.6 Addressing Transfer Formats

Each device on the bus has a unique address. The PC8741x device starts a slave address set-up process if one of the following occurs:

- A V_{SB} Power-Up reset is activated by V_{SB} going up: in this case, the ACBSA strap value is also sampled (see Section 2.2.2 on page 34).
- A broadcast transaction to the General Call address with a “Reset and write programmable part of slave address by hardware” command is received over the ACCESS.bus (see below).

During the slave address set-up process, the PC8741x device performs the following actions in the order listed:

1. Checks the value of the ACBSADD field in the ACBCF register (see Section 3.7.11 on page 57); if the value of the bits is valid (not zero), the value is adopted and the other two actions are ignored.
2. Checks the value of the ACBSA strap sampled at the V_{SB} Power-Up reset.
3. Adopts one of the two fixed values (see Section 1.4.11 on page 29) for its slave address, according to the ACBSA value.

Before any data is transmitted, the master transmits the address of the target slave. The slave must send an acknowledge signal on the ACBDAT line once it recognizes its address.

The address consists of the first seven bits after a Start Condition. The direction of the data transfer (R/$\overline{W}$) depends on the eighth bit (which is sent after the address).

When the address is sent, each device in the system compares this address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending on the state of the R/$\overline{W}$ bit (1=read, 0=write), the device acts either as a transmitter or a receiver. The combination of the 7-bit address and the R/$\overline{W}$ bit is used in this document to define the slave address as a write address (even) and a read address (odd) pair.

A low-to-high transition during a ACBCLK high period indicates the Stop Condition and ends the transaction of ACBDAT (see Figure 34).

6.0 ACCESS.bus Interface (Continued)

The ACCESS.bus protocol allows a General Call address to be sent to all slaves connected to the bus. The first byte sent specifies the General Call address (00h) and the second byte specifies the meaning of the general call ("Reset and write programmable part of slave address by hardware"—06h). When a 00h-followed-by-a-06h transaction is detected, the PC8741x device resets the ACCESS.bus Interface logic and the data registers (except for the configuration registers) and reloads the default slave address.

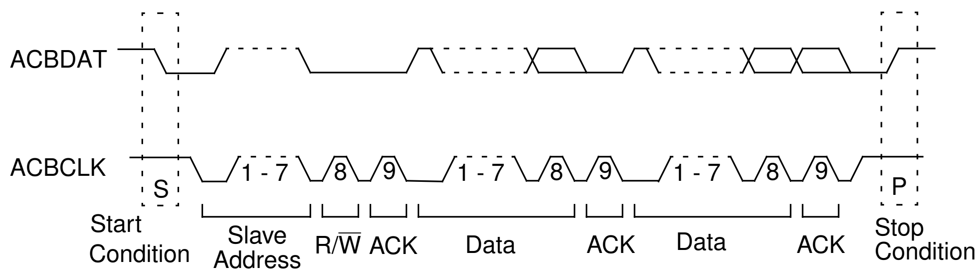


Figure 34. A Complete ACCESS.bus Data Transaction

6.2.7 Arbitration on the Bus

Multiple master devices on the bus require arbitration between their conflicting bus access demands. Control of the bus is initially determined according to address bits and clock cycle. If more than one master try to address the same slave, data comparisons determine the outcome of this arbitration. A master device immediately aborts a transaction if the value sampled on the ACBDAT line differs from the value internally driven by the device. (An exception to this rule is ACBDAT while the master is receiving data. The lines may be held low by the slave without causing an abort.)

The ACBCLK signal is monitored by the master for clock synchronization and to allow the slave to stall the bus. The actual clock period is set either by the master with the longest clock period or by the slave stall period. The maximum allowed "cumulative clock low extend time" of a slave device (per transaction) is defined in Section 11.5.6 on page 246. The clock high period is determined by the master with the shortest clock high period; however, it must not be longer than the value defined in Section 11.5.6.

When an abort occurs during the address transmission, the master that identifies the conflict must release the bus, switch to Slave mode and continue to sample ACBDAT to check if it is being addressed by the winning master on the bus.

If the PC8741x device detects that ACBCLK is held low longer than the maximum allowed time, it aborts the current transaction and sets the LOWCKTO bit in the ACBCST register (see Section 6.3.2 on page 127).

6.2.8 Packet Error Check (PEC)

The Packet Error Checking mechanism complies with Revision 1.1 of the SMBus Specification. It consists of appending an error check byte to the end of each transaction (before the Stop condition).

The PC8741x devices are capable of communicating with all masters, whether or not they implement the PEC.

Master PEC Assessment

After reset, a master supporting the PEC feature performs the following sequence:

1. Read (**without** PEC) the ACBCST register of the PC8741x slave device.
2. Check the PECAVAIL bit (bit 0 of the register), which indicates the PEC slave support (for the PC8741x devices, this bit is always '1').
3. Read (**with** PEC) the ACBCST register and check for its correctness.
4. Register the PC8741x slave device as PEC compliant.

All subsequent transactions between the master and the PEC-compliant slave include the PEC byte. During write transactions, the master provides the PEC of the transmitted data. During read transactions, the master checks the received data using the PEC supplied by the slave. In both cases, the master supplies the number of ACBCLK cycles required for PEC support. If the master does not supply these clock cycles, the PC8741x device considers that PEC is not supported during the current transaction (i.e., there is no error condition).

Slave PEC Support

The PC8741x device provides PEC support when the master also requires it. However, the PC8741x device always calculates the PEC value of the incoming or outgoing data.

6.0 ACCESS.bus Interface (Continued)

After the last bytes of a write transaction, if the master supplies additional ACBCLK cycles, the PC8741x device receives the PEC byte and compare it with the calculated PEC value. Otherwise, it just ignores the calculated PEC. If the comparison fails, the PC8741x device generates a NACK bit at the end of the PEC byte and sets the PECERR bit in the ACBCST register (see Section 6.3.2 on page 127) but does not execute the write transaction.

At the end of the last byte of a read transaction, if the master generates an ACK for the last byte (instead of a NACK), the PC8741x device sends the calculated PEC value during the following byte. Otherwise, it discards the calculated PEC.

PEC Implementation

The PEC is an 8-bit cyclic redundancy check (CRC-8) value attached at the end of an ACCESS.bus transaction as the last byte transmitted before the Stop condition.

The PC8741x device calculates the PEC value by hardware (bit-by-bit), using all the bytes in the transaction (except the PEC byte itself). PEC calculation does not include Start, Restart, Stop, ACK or NACK, which are bus control bits and not data bits. The PEC value is generated using the polynomial $C(x) = x^8 + x^2 + x^1 + 1$, which is specified in Intel's SMBus Specification (*Rev 1.1 Dec. 11, 1998*). During a read transaction, the PEC value is generated by the PC8741x device and checked by the master; during a write transaction, it is generated by the master and checked by the slave.

6.2.9 ACCESS.bus Protocol

The protocol is based on five basic byte types: Save Address, Command, Offset Address, Data and PEC; these are described below. An error is flagged in the following cases:

- If the number of bytes in the transaction differs from the number of bytes required by the Command byte.
- For Command byte type, if the reserved bit is not zero.

When an error is flagged, a NACK is generated at the end of the current byte (the current transaction is aborted) and the ILGCOM bit in the ACBCST register is set (see Section 6.3.2 on page 127).

Slave Address Byte Type

Bit	7	6	5	4	3	2	1	0
Name	**SLAVEAD**							**ACBRW**

Bit	Description
7-1	**SLAVEAD (Slave Address).** This seven-bit field indicates the slave address of the accessed device. If its value is the same as the one selected during the set-up process (see Section 6.2.6), the PC8741x device responds to the present transaction.
0	**ACBRW (ACCESS.bus Read/Write Mode).** Selects the transfer direction for the current transaction. 0: Write ACCESS.bus transaction (from master to slave) - equivalent to an even 8-bit slave address 1: Read ACCESS.bus transaction (from slave to master) - equivalent to an odd 8-bit slave address

6.0 ACCESS.bus Interface (Continued)

Command Byte Type

This type has two variations, according to the value of the INEX bit.

Bit	7	6	5	4	3	2	1	0
Name	**INEX=0**	**RDWR**	**LOGDEV**					

Bit	7	6	5	4	3	2	1	0
Name	**INEX=1**	**RDWR**	**Reserved**	**XBCSN**		**XA26-XA24**		

Bit	Description
7	**INEX (Internal/External Access).** Selects the access type for the current transaction. 0: Internal access - to modules within the PC8741x device 1: External access - to devices connected to the X-Bus (**PC87417**)
6	**RDWR (Read/Write Access).** Selects the access direction for the current transaction. 0: Write access - data sent by the master is written into the selected address 1: Read access - data read from the selected address is stored in the Read Buffer
5-0	**LOGDEV (Logical Device Number).** This field indicates the Logical Device Number (LDN) of the accessed internal functional block. Table 33 defines the LDN assignment for each functional block of the PC8741x device; other table values are not allowed. These LDNs are equivalent but not identical to those assigned by the plug-and-play configuration. Only those Logical Devices that can be accessed both through the ACCESS.bus and the LPC bus are assigned the same LDN.
5	**Reserved.**
4-3	**XBCSN (X-Bus Chip-Select Number).** These two bits select one of the four X-Bus chip-selects to be accessed during the current transaction (**PC87417**). **Bits** **4 3 Chip-Select** 0 0: $\overline{XCS0}$ 0 1: $\overline{XCS1}$ 1 0: $\overline{XCS2}$ 1 1: $\overline{XCS3}$
2-0	**XA26-XA24 (X-Bus Offset Address).** These bits set the value of the X-Bus address lines XA26-XA24, which are used as offset for the X-Bus access during the current transaction (**PC87417**). The XA27 address line is set to ‘0’.

6.0 ACCESS.bus Interface (Continued)

Table 33. Logical Device Number (LDN) Assignment for ACCESS.bus

LDN	Functional Block
00h	Floppy Disk Controller (FDC)
01h	Parallel Port (PP)
02h	Serial Port 2 (SP2)
03h	Serial Port 1 (SP1)
04h	System Wake-Up Control (SWC)
06h	Keyboard and Mouse Controller (KBC)[1]
07h	General-Purpose I/O (GPIO) Ports
0Fh	X-Bus Extension (**PC87417**)
10h	Real Time Clock (RTC)[2]
30h	PM1b_EVT_BLK (SWC-ACPI)
31h	PM1b_CNT_BLK (SWC-ACPI)
32h	GPE1_BLK (SWC-ACPI)
3Eh	Device Configuration (CONFIG)[3,4]
3Fh	ACCESS.bus Interface (ACB)[3]

1. This Logical Device has two chip selects for the Index/Data registers, each pointed to by a different Base Address in the configuration. The A2 bit of the Offset Address Byte differentiates between the two chip selects:
   A2 = 0: the Index/Data registers pointed to by the Base Address at 60h and 61h
   A2 = 1: the Index/Data registers pointed to by the Base Address at 62h and 63h.
2. This Logical Device has two chip selects for the Index/Data registers, each pointed to by a different Base Address in the configuration. The A1 bit of the Offset Address Byte differentiates between the two chip selects (see Note 1 above).
3. This Logical Device is accessible only through the ACCESS.bus.
4. Access to this Logical Device is through the Index register located at offset 00h and data register located at offset 01h.

Offset Address Byte Type

This is an 8-bit value representing either of the following:

- Internal access - the offset address from the base of the functional block.
- External access - eight bits of the offset address from the base of the X-Bus chip-select (**PC87417**).

The offset address value must be within the defined range for the selected Logical Device or X-Bus chip-select. Offset values outside this range are reserved.

Data Byte Type

This is an 8-bit value representing either the written or read data.

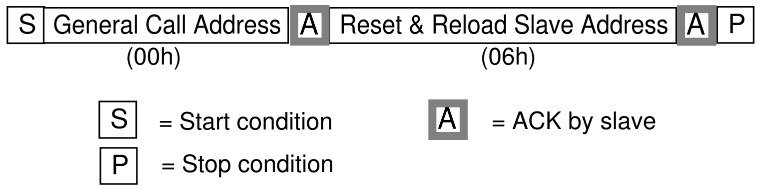
PEC Byte Type

This is an 8-bit value representing the 8-bit cyclic redundancy check of all the transferred bytes (see Section 6.2.8 on page 120).

6.0 ACCESS.bus Interface (Continued)

Reset Slave Transaction

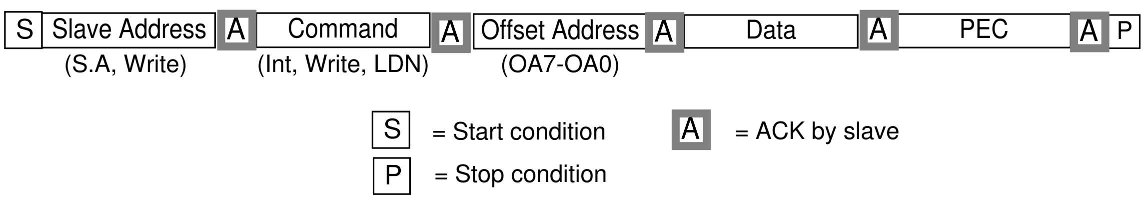
This is a broadcast transaction to the General Call address (00h) that resets the ACCESS.bus Interface logic and the data registers (the configuration registers are not affected) and reloads the current slave address by starting a slave address set-up process (see Section 6.2.6 on page 119). PEC is not supported for this transaction. Since this is a broadcast transaction, all slave devices connected to the ACCESS.bus respond to it.



Write Internal Transaction

This transaction writes a byte of data to a register of a functional block of the PC8741x device. The functional block is selected by the Logical Device Number for the ACCESS.bus (see Table 33 on page 123). The specific register is accessed using the 8-bit offset address (from the base of the functional block). If PEC is supported, the master sends a PEC byte at the end of the transaction.

If the selected Logical Device is not powered (the V_{DD} supply is off), the PC8741x device generates a NACK bit at the end of the Command byte, sets the OFFLDN bit in the ACBCST register (see Section 6.3.2 on page 127) and aborts the transaction.

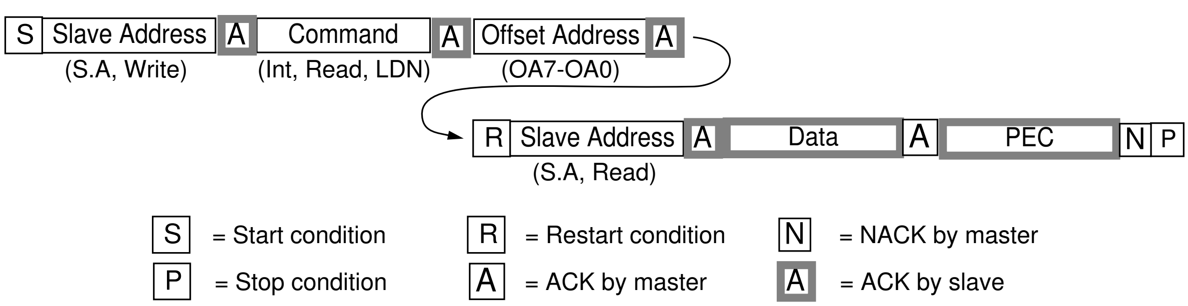


Read Internal Transaction

This transaction reads a byte of data from a register of a functional block of the PC8741x device. The functional block is selected by the Logical Device Number for the ACCESS.bus (see Table 33 on page 123). The specific register is accessed using the 8-bit offset address (from the base of the functional block). This transaction is executed in two phases:

- The master executes an ACCESS.bus write transaction, which conveys the Command (Read) and Offset Address information to the PC8741x device. During this phase, the data is read from the specific register into the Read Buffer. This phase has no Stop Condition.
- Following a Restart condition, the master executes an ACCESS.bus read transaction. During this phase the data is transferred from the Read Buffer to the master. At the end of this phase, the PC8741x device returns a PEC byte if required by the master. The calculated PEC value is based on the bytes transferred during both phases.

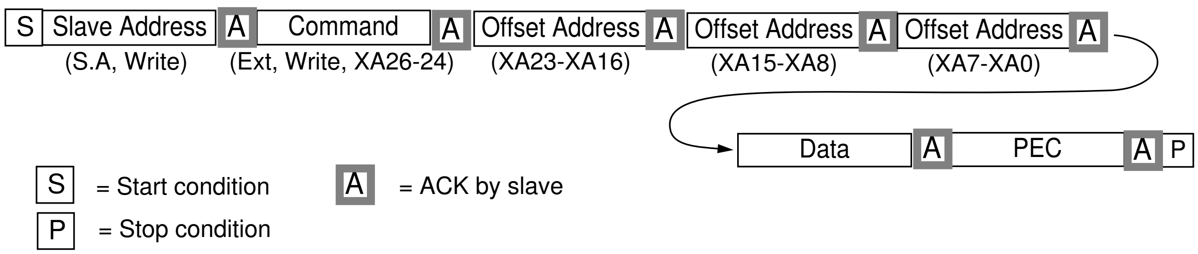
If the selected Logical Device is not powered (the V_{DD} supply is off), the PC8741x device generates a NACK bit at the end of the Command byte, sets the OFFLDN bit in the ACBCST register (see Section 6.3.2 on page 127) and aborts the transaction.



6.0 ACCESS.bus Interface (Continued)

Write External Transaction (PC87417)

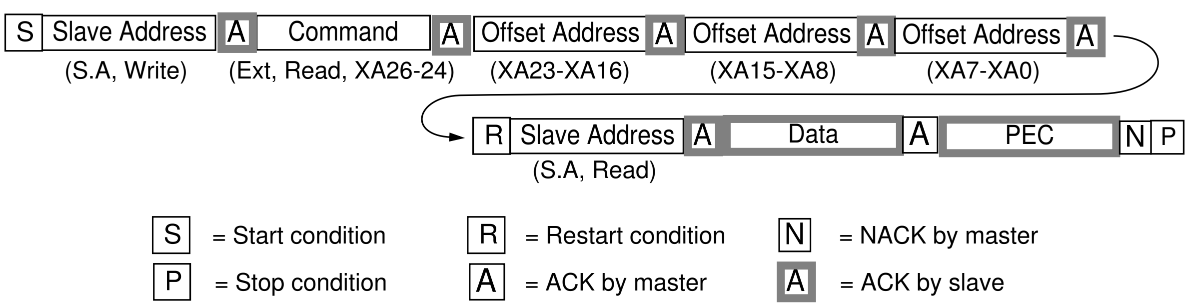
This transaction writes a byte of data to a memory device or to an I/O port connected to the X-Bus. The chip-select for the device is selected by the XBCSN field in the command byte. The specific memory location or I/O port register is accessed using a 27-bit offset address (from the base of the chip-select). The 27-bit offset address is broken into four bytes: XA26-XA24 in the Command byte and XA23-XA16, XA15-XA8 and XA7-XA0 in three successive Offset Address bytes. If PEC is supported, the master sends a PEC byte at the end of the transaction.



Read External Transaction (PC87417)

This transaction reads a byte of data from a memory device or from an I/O port connected to the X-Bus. The chip-select for the device is selected by the XBCSN field in the command byte. The specific memory location or I/O port register is accessed using a 27-bit offset address (from the base of the chip-select). The 27-bit offset address is broken in four bytes: XA26-XA24 in the Command byte and XA23-XA16, XA15-XA8 and XA7-XA0 in three successive Offset Address bytes. This transaction is executed in two phases:

- The master executes an ACCESS.bus write transaction, which conveys the Command (Read), chip-select and Offset Address information to the PC8741x device. During this phase, the data is read from the specific memory location or I/O port register into the Read Buffer. This phase has no Stop Condition.
- Following a Restart condition, the master executes an ACCESS.bus read transaction. During this phase the data is transferred from the Read Buffer to the master. At the end of this phase, the PC8741x device returns a PEC byte if required by the master. The calculated PEC value is based on the bytes transferred during both phases.



6.2.10 Transaction Execution

The ACCESS.bus uses the internal bus of the PC8741x device to access the internal modules (except its own registers) or to bridge transactions to the X-Bus (see “Block Diagram” on page 1). Since the same internal bus is also used independently by the LPC bus, the duration of the ACCESS.bus use of the internal bus is held to a minimum.

At the highest ACBCLK frequency (100 KHz), the longest ACCESS.bus transaction (Read External) takes at least 750 µs to complete. In order not to stall the internal bus for such a long time, the ACCESS.bus transactions are executed as follows:

- Write - data is written through the internal bus at the end of the transaction after the Stop condition is detected; the next ACCESS.bus transaction can start immediately while the present data is written through the internal bus.
- Read - data is read through the internal bus during the second part of the transaction (beginning with Restart), after the Slave Address is received and before it is acknowledged (ACK); while the data is read through the internal bus, the ACBCLK signal is held low, indicating to the ACCESS.bus master that PC8741x device is not ready (see Section 6.2.7 on page 120).

The duration of the ACCESS.bus transaction through the internal bus is longer for external access (X-Bus devices - **PC87417**) than for internal access (internal modules of the PC8741x device). If wait states are configured for the module or X-Bus access, their duration must be added to the internal bus transaction time. When the XRDY signal is in use, its delay must also be accounted for.

If an LPC transaction started before an ACCESS.bus transaction, the execution of the ACCESS.bus transaction through the internal bus is withheld until the end of the LPC transaction.

6.0 ACCESS.bus Interface (Continued)

6.3 ACB REGISTERS (ON ACCESS.BUS ONLY)

All these registers are accessible only through the ACCESS.bus.

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from a specific register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

6.3.1 ACB Register Map (on ACCESS.bus Only)

Offset	Mnemonic	Register Name	Type	Power Well	Section
00h	ACBCST	ACCESS.bus Control/Status	Varies per bit	V_{SB}	6.3.2
01h	ACBCFG	ACCESS.bus Configuration	Varies per bit	V_{SB}	6.3.3
02h	ACBLKCTL	ACCESS.bus Lock Control	Varies per bit	V_{SB}	6.3.4
03h	ACBFDIS	ACCESS.bus Fast Disable	R/W	V_{SB}	6.3.5
04h	ACBTRIS	ACCESS.bus TRI-State	R/W	V_{SB}	6.3.6
05h	ACCLCF1	Access Lock Configuration 1	R/W	V_{SB}	6.3.7
06h	ACCLCF2	Access Lock Configuration 2	R/W	V_{SB}	6.3.8

6.0 ACCESS.bus Interface (Continued)

6.3.2 ACCESS.bus Control/Status Register (ACBCST)

This register controls the ACCESS.bus interface and holds the status of the last transactions. On reset, it is cleared (01h).

Power Well: V_{SB}

Location: Offset 00h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**OFFLDN**	**ILGCOM**	**PECERR**	**BUSERR**	**LOWCKTO**	**ACCLVIOL**	**VDDSTAT**	**PECAVAIL**
Reset	0	0	0	0	0	0	0	1

Bit	Type	Description
7	R/W1C	**OFFLDN (Accessed LDN Powered-off Flag).** Indicates that the Logical Device accessed through the command byte (only for Internal Access mode, i.e., when INEX = 0) is powered-off (relevant for the Legacy functional blocks powered from the V_{DD} plane). Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Powered Logical Device accessed (default) 1: Unpowered Logical Device accessed
6	R/W1C	**ILGCOM (Illegal Command Flag).** Indicates that an illegal command code or an incorrect number of address/data bytes was received or requested for transmission (by last byte NACK or Stop control). Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Correct protocol (default) 1: Illegal command or number of bytes
5	R/W1C	**PECERR (PEC Error Flag).** Indicates that a PEC error was detected in the write transaction bytes that were received from the master. This bit is not updated if the master does not send a PEC byte. Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Correct PEC (default) 1: CRC of the received bytes differs from the received PEC
4	R/W1C	**BUSERR (Bus Error Flag).** Indicates that an unexpected Start, Restart or Stop Condition was detected during a read or write transaction. Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Correct transaction (default) 1: Illegal Start, Restart or Stop Condition
3	R/W1C	**LOWCKTO (Low Clock Timeout Flag).** Indicates that the ACBCLK signal was detected low for longer than the maximum allowed “cumulative clock low extend time” during a transaction, as defined in Section 11.5.6 on page 246. Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Correct clock low timing (default) 1: Clock low timeout
2	R/W1C	**ACCLVIOL (Access Lock Violation Flag).** Indicates that an LPC access to a functional module locked for sole use by ACCESS.bus was detected. Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Correct LPC access (default) 1: LPC access to a locked functional module
1	RO	**VDDSTAT (V_{DD} Power Status).** Indicates the actual status of the V_{DD} power supply to the PC8741x device. 0: V_{DD} power Off 1: V_{DD} power On
0	RO	**PECAVAIL (PEC Feature Available).** Enables the master to detect the availability of the PEC implementation in the slave. 0: Peripheral does not support PEC 1: Peripheral supports PEC (default and fixed value for PC8741x devices)

6.0 ACCESS.bus Interface (Continued)

6.3.3 ACCESS.bus Configuration Register (ACBCFG)

This register controls the configuration of the ACCESS.bus Interface. On reset, it is cleared (00h).

Power Well: V_{SB}

Location: Offset 01h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**CSWRST**	**Reserved**	**ACCLMD**		**Reserved**			**ACTSTAT**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W	**CSWRST (Controller Software Reset).** When set to '1', this bit triggers a Controller Software reset sequence (see Section 2.2.3 on page 35) and then returns to '0'. It always returns '0' when read. 0: Normal operation (default) 1: Enable the Controller Software Reset
6		**Reserved.**
5-4	R/W	**ACCLMD (Locked Module Access Mode).** These bits control the behavior of the LPC Interface whenever a locked module is accessed. **Bits 5 4 Function** 0 0: Complete cycle and generate Error SYNC; read 00h; ignore write (default). 0 1: Complete cycle; read 00h; ignore write. 1 0: Ignore cycle (do not generate SYNC). 1 1: – Locked X-Bus chip-select ($\overline{XCS3}$-$\overline{XCS0}$): Generate Long Wait SYNC for read and write until access lock is removed; then complete transaction normally. – Any other locked module: Complete cycle; read 00h; ignore write.
3-1		**Reserved.**
0	R/W	**ACTSTAT (Module Activation Status Configuration).** This bit configures the behavior of the Activation bit (for the Legacy modules) when read through the LPC bus (index 30; see Section 3.2.3 on page 40). When this bit is set to '1' and a specific module is disabled by the bits in the ACBFDIS register (see Section 6.3.5 on page 130), or when the module is locked by the bits in the ACCLCF1 register (see Section 6.3.7 on page 132), the module Activation status that is read through the LPC returns a '0' value, ignoring the actual setting of the Activation bit. 0: Activation status reflects the value of the Activation bit (default) 1: Activation status reflects the value of the Activation bit, or returns '0' if either the module is locked, or disabled by the bits in the ACBFDIS register

6.3.4 ACCESS.bus Lock Control Register (ACBLKCTL)

This register controls the configuration lock of the PC8741x device. On reset, it is cleared (00h).

Power Well: V_{SB}

Location: Offset 02h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**VSBLOCK**	**UNLOCKM**	**UNLOCKG**	**UNLOCKF**	**UNLOCKC**	**UNLOCKX**	**UNLOCKR**	**UNLOCKS**
Reset	0	0	0	0	0	0	0	0

6.0 ACCESS.bus Interface (Continued)

Bit	Type	Description
7	R/W1S	**VSBLOCK (Configuration Lock Until V_{SB} Reset).** Controls the reset source of the following lock bits: LOCKMCF and LOCKGCF in the SIOCF1 register, LOCKFDS in the SIOCF6 register, LOCKCCF in the CLOCKCF register, LOCKCFP in all GPCFG1 registers (for each GPIO pin), LOCKIOMP in the XIOCNF register (**PC87417**), LOCKMMP in the XMEMCNF2 register(**PC87417**), all bits of the RLR register, LOCKXSCF in the XZM0-XZM3 registers (**PC87417**), LOCKXHP in the HAP0 and HAP1 registers (**PC87417**), LOCK_TMRRST in the PWTMRCTL register and LOCK_SLP_ENC in the SLP_ST_CFG register. When set to ‘1’, this bit is cleared only by the V_{SB} Power-Up reset. 0: Lock bits cleared by V_{DD} Power-Up reset, by Hardware reset or by V_{SB} Power-Up reset (default) 1: Lock bits cleared only by V_{SB} Power-Up reset
6	R/W	**UNLOCKM (Unlock Multiplexing Configuration).** When set to ‘1’, this bit resets the LOCKMCF bit in the SIOCF1 register, ignoring the setting of the VSBLOCK bit. It always returns ‘0’ when read. 0: Normal operation (default) 1: Reset the LOCKMCF bit
5	R/W	**UNLOCKG (Unlock GPIO Configuration).** When set to ‘1’, this bit resets the LOCKGCF bit in the SIOCF1 register and the LOCKCFP bit in all the GPCFG1 registers (for each GPIO pin), ignoring the setting of the VSBLOCK bit. It always returns ‘0’ when read. 0: Normal operation (default) 1: Reset the LOCKGCF and all the LOCKCFP bits
4	R/W	**UNLOCKF (Unlock Fast Disable Configuration).** When set to ‘1’, this bit resets the LOCKFDS bit in the SIOCF6 register, ignoring the setting of the VSBLOCK bit. It always returns ‘0’ when read. 0: Normal operation (default) 1: Reset the LOCKFDS bit
3	R/W	**UNLOCKC (Unlock Clock Configuration).** When set to ‘1’, this bit resets the LOCKCCF bit in the CLOCKCF register, ignoring the setting of the VSBLOCK bit. It always returns ‘0’ when read. 0: Normal operation (default) 1: Reset the LOCKCCF bit
2	R/W	**UNLOCKX (Unlock X-Bus Configuration).** When set to ‘1’, this bit resets the LOCKIOMP bit in the XIOCNF register, the LOCKMMP bit in the XMEMCNF2 register, the LOCKXSCF bit in the XZM0-XZM3 registers and the LOCKXHP bit in the HAP0 and HAP1 registers, ignoring the setting of the VSBLOCK bit (**PC87417**). It always returns ‘0’ when read. 0: Normal operation (default) 1: Reset the LOCKIOMP, LOCKMMP, LOCKXSCF and LOCKXHP bits
1	R/W	**UNLOCKR (Unlock RAM Lock Configuration).** When set to ‘1’, this bit resets all the bits of the RLR register (see Section 3.16.3 on page 88), ignoring the setting of the VSBLOCK bit. It always returns ‘0’ when read. 0: Normal operation (default) 1: Reset all the bits of the RLR register
0	R/W	**UNLOCKS (Unlock SWC Configuration).** When set to ‘1’, this bit resets the LOCK_TMRRST bit in the PWTMRCTL register and the LOCK_SLP_ENC bit in the SLP_ST_CFG register, ignoring the setting of the VSBLOCK bit. It always returns ‘0’ when read. 0: Normal operation (default) 1: Reset the LOCK_TMRRST and LOCK_SLP_ENC bits

6.0 ACCESS.bus Interface (Continued)

6.3.5 ACCESS.bus Fast Disable Register (ACBFDIS)

This register provides a fast way to disable one or more modules through the ACCESS.bus without having to access the Activate register of each module (see Section 3.2.3 on page 40). It is reset by hardware to 00h.

Power Well: V_{SB}

Location: Offset 03h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**KBDDIS**	**MSDIS**	**SER1DIS**	**SER2DIS**	**PARPDIS**	**FDCDIS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**KBDDIS (Keyboard Controller Disable).** When set to 1, this bit forces the Keyboard Controller module (Logical Device 6) to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
4	**MSDIS (Mouse Controller Disable).** When set to 1, this bit forces the Mouse Controller module (Logical Device 5) to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
3	**SER1DIS (Serial Port 1 Disable).** When set to 1, this bit forces the Serial Port 1 module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
2	**SER2DIS (Serial Port 2 Disable).** When set to 1, this bit forces the Serial Port 2 module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
1	**PARPDIS (Parallel Port Disable).** When set to 1, this bit forces the Parallel Port module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
0	**FDCDIS (Floppy Disk Controller Disable).** When set to 1, this bit forces the Floppy Disk Controller module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled

6.0 ACCESS.bus Interface (Continued)

6.3.6 ACCESS.bus TRI-STATE Register (ACBTRIS)

This register provides a fast way to float the outputs of one or more modules through the ACCESS.bus without having to access their TRI-STATE Control bit in the Special Configuration register at index F0h. The module outputs enter TRI-STATE only when the module is disabled (see Section 6.3.5 on page 130). The register is reset by hardware to 00h.

Power Well: V_{SB}

Location: Offset 04h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**KBMSTRIS**	**SER1TRIS**	**SER2TRIS**	**PARPTRIS**	**FDCTRIS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4	**KBMSTRIS (Keyboard and Mouse Outputs TRI-STATE).** When set to 1 and the module is disabled, this bit forces the outputs of the Keyboard and Mouse Controller to be in TRI-STATE regardless of bit 0 in the Keyboard Configuration register (see Section 3.13.3 on page 69). 0: Enabled or Disabled, according to bit 0 in the Keyboard Configuration register (default) 1: Outputs in TRI-STATE
3	**SER1TRIS (Serial Port 1 Outputs TRI-STATE).** When set to 1 and the module is disabled, this bit forces the outputs of the Serial Port 1 module to be in TRI-STATE regardless of bits 6 and 0 in the Serial Port 1 Configuration register (see Section 3.11.3 on page 66). 0: Enabled or Disabled, according to bits 6 and 0 in the Serial Port 1 Configuration register (default) 1: Outputs in TRI-STATE
2	**SER2TRIS (Serial Port 2 Outputs TRI-STATE).** When set to 1 and the module is disabled, this bit forces the outputs of the Serial Port 2 module to be in TRI-STATE regardless of bits 6 and 0 in the Serial Port 2 Configuration register (see Section 3.10.3 on page 64). 0: Enabled or Disabled, according to bits 6 and 0 in the Serial Port 2 Configuration register (default) 1: Outputs in TRI-STATE
1	**PARPTRIS (Parallel Port Outputs TRI-STATE).** When set to 1 and the module is disabled, this bit forces the outputs of the Parallel Port module to be in TRI-STATE regardless of bit 0 in the Parallel Port Configuration register (see Section 3.9.3 on page 62). 0: Enabled or Disabled, according to bit 0 in the Parallel Port Configuration register (default) 1: Outputs in TRI-STATE
0	**FDCTRIS (Floppy Disk Controller Outputs TRI-STATE).** When set to 1 and the module is disabled, this bit forces the outputs of the Floppy Disk Controller module to be in TRI-STATE regardless of bit 0 in the FDC Configuration register (see Section 3.8.3 on page 59). 0: Enabled or Disabled, according to bit 0 in the FDC Configuration register (default) 1: Outputs in TRI-STATE

6.0 ACCESS.bus Interface (Continued)

6.3.7 Access Lock Configuration 1 Register (ACCLCF1)

This register controls the locking of the device functional blocks to LPC bus access. On reset, it is cleared (00h).

Power Well: V_{SB}

Location: Offset 05h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**CONFALOK**	**Reserved**		**KBCALOK**	**SER1ALOK**	**SER2ALOK**	**PARPALOK**	**FDCALOK**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**CONFALOK (Configuration Access Lock).** When set to 1, this bit disables LPC bus access to the Device Configuration module and locks the module for use by ACCESS.bus only. If the module is accessed through the LPC bus, it responds according to the setting of the ACCLMD field in the ACBCFG register (see Section 6.3.3 on page 128); in addition, the ACCLVIOL bit in ACBCST is set (see Section 6.3.2 on page 127). 0: Module opened for LPC access (default) 1: Module locked for LPC access and opened for use by ACCESS.bus only
6-5	**Reserved.**
4	**KBCALOK (Keyboard/Mouse Controller Access Lock).** When set to 1, this bit disables LPC bus access to the Keyboard/Mouse Controller module and locks the module for use by ACCESS.bus only. If the module is accessed through the LPC bus, it responds according to the setting of the ACCLMD field and the ACCLVIOL bit (see CONFALOK bit). The setting of this bit also forces module activation regardless of the actual setting of its Activation bit (index 30; see Section 3.2.3 on page 40) and of the setting of the global enable bit (GLOBEN bit in the SIOCF1 register). 0: Module opened for LPC access (default) 1: Module locked for LPC access and opened for use by ACCESS.bus only (see Section 3.3.2 on page 44)
3	**SER1ALOK (Serial Port 1 Access Lock).** When set to 1, this bit disables LPC bus access to the Serial Port 1 module and locks the module for use by ACCESS.bus only. If the module is accessed through the LPC bus, it responds according to the setting of the ACCLMD field and the ACCLVIOL bit (see CONFALOK bit). The setting of this bit also forces module activation regardless of the actual setting of its Activation bit (index 30; see Section 3.2.3 on page 40), of its fast-enable bit (SER1DIS bit in the SIOCF6 register) and of the setting of the global enable bit (GLOBEN bit in the SIOCF1 register). 0: Module opened for LPC access (default) 1: Module locked for LPC access and opened for use by ACCESS.bus only (see Section 3.3.2 on page 44)
2	**SER2ALOK (Serial Port 2 Access Lock).** When set to 1, this bit disables LPC bus access to the Serial Port 2 module and locks the module for use by ACCESS.bus only. This bit behaves like the SER1ALOK bit. 0: Module opened for LPC access (default) 1: Module locked for LPC access and opened for use by ACCESS.bus only (see Section 3.3.2 on page 44)
1	**PARPALOK (Parallel Port Access Lock).** When set to 1, this bit disables LPC bus access to the Parallel Port module and locks the module for use by ACCESS.bus only. This bit behaves like the SER1ALOK bit. 0: Module opened for LPC access (default) 1: Module locked for LPC access and opened for use by ACCESS.bus only (see Section 3.3.2 on page 44)
0	**FDCALOK (Floppy Disk Controller Access Lock).** When set to 1, this bit disables LPC bus access to the Floppy Disk Controller module and locks the module for use by ACCESS.bus only. This bit behaves like the SER1ALOK bit. 0: Module opened for LPC access (default) 1: Module locked for LPC access and opened for use by ACCESS.bus only (see Section 3.3.2 on page 44)

6.0 ACCESS.bus Interface (Continued)

6.3.8 Access Lock Configuration 2 Register (ACCLCF2)

This register controls the locking to LPC bus access of the device functional blocks. On reset, it is cleared (00h).

Power Well: V_{SB}

Location: Offset 06h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SWCALOK**	**RTCALOK**	**XBSALOK**	**Reserved**	**XCS3ALOK**	**XCS2ALOK**	**XCS1ALOK**	**XCS0ALOK**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**SWCALOK (System Wake-up Controller Access Lock).** When set to 1, this bit disables the LPC bus access to the System Wake-up Controller module and locks the module for use by ACCESS.bus only. If the module is accessed through the LPC bus (the SWC registers), it responds according to the setting of the ACCLMD field in the ACBCFG register (see Section 6.3.3 on page 128), and the ACCLVIOL bit in ACBCST is set (see Section 6.3.2 on page 127). This bit does not affect LPC access to the ACPI registers. The setting of this bit also forces module activation regardless of the actual setting of its Activation bit (index 30; see Section 3.2.3 on page 40) and of the setting of the global enable bit (GLOBEN bit in the SIOCF1 register). 0: Module opened for LPC access (default) 1: Module locked for LPC access and opened for use by ACCESS.bus only (see Section 3.3.2 on page 44)
6	**RTCALOK (Real-Time Clock Access Lock).** When set to 1, this bit disables the LPC bus access to the Real-Time Clock module and locks the module for use by ACCESS.bus only. This bit behaves like the SWCALOK bit. 0: Module opened for LPC access (default) 1: Module locked for LPC access and opened for use by ACCESS.bus only (see Section 3.3.2 on page 44)
5	**XBSALOK (X-Bus Module Access Lock).** When set to 1, this bit disables the LPC bus access to the X-Bus module and locks the module for use by ACCESS.bus only (**PC87417**). This bit behaves like the SWCALOK bit. 0: Module opened for LPC access (default) 1: Module locked for LPC access and opened for use by ACCESS.bus only (see Section 3.3.2 on page 44)
4	**Reserved.**
3	**XCS3ALOK (X-Bus XCS3 Access Lock).** When set to 1, this bit disables the LPC bus access to the X-Bus devices connected to $\overline{\text{XCS3}}$ and locks them for use by ACCESS.bus only (**PC87417**). This bit behaves like the SWCALOK bit. 0: $\overline{\text{XCS3}}$-connected devices opened for LPC access (default) 1: $\overline{\text{XCS3}}$-connected devices locked for LPC access and opened for use by ACCESS.bus only (see Section 3.3.2 on page 44)
2	**XCS2ALOK (X-Bus XCS2 Access Lock).** Same as XCS3ALOK bit for X-Bus devices connected to $\overline{\text{XCS2}}$ (**PC87417**)
1	**XCS1ALOK (X-Bus XCS1 Access Lock).** Same as XCS3ALOK bit for X-Bus devices connected to $\overline{\text{XCS1}}$ (**PC87417**)
0	**XCS0ALOK (X-Bus XCS0 Access Lock).** Same as XCS3ALOK bit for X-Bus devices connected to $\overline{\text{XCS0}}$ (**PC87417**)

6.0 ACCESS.bus Interface (Continued)

6.4 ACB REGISTER BITMAP

<table>
<tr><th colspan="2">Register</th><th colspan="8">Bits</th></tr>
<tr><th>Offset</th><th>Mnemonic</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>00h</td><td>ACBCST</td><td>OFFLDN</td><td>ILGCOM</td><td>PECERR</td><td>BUSERR</td><td>LOWCKTO</td><td>ACCLVIOL</td><td>VDDSTAT</td><td>PECAVAIL</td></tr>
<tr><td>01h</td><td>ACBCFG</td><td>CSWRST</td><td>Reserved</td><td colspan="2">ACCLMD</td><td colspan="3">Reserved</td><td>ACTSTAT</td></tr>
<tr><td>02h</td><td>ACBLKCTL</td><td>VSBLOCK</td><td>UNLOCKM</td><td>UNLOCKG</td><td>UNLOCKF</td><td>UNLOCKC</td><td>UNLOCKX</td><td>UNLOCKR</td><td>UNLOCKS</td></tr>
<tr><td>03h</td><td>ACBFDIS</td><td colspan="2">Reserved</td><td>KBDDIS</td><td>MSDIS</td><td>SER1DIS</td><td>SER2DIS</td><td>PARPDIS</td><td>FDCDIS</td></tr>
<tr><td>04h</td><td>ACBTRIS</td><td colspan="3">Reserved</td><td>KBMSTRIS</td><td>SER1TRIS</td><td>SER2TRIS</td><td>PARPTRIS</td><td>FDCTRIS</td></tr>
<tr><td>05h</td><td>ACCLCF1</td><td>CONFALOK</td><td colspan="2">Reserved</td><td>KBCALOK</td><td>SER1ALOK</td><td>SER2ALOK</td><td>PARPALOK</td><td>FDCALOK</td></tr>
<tr><td>06h</td><td>ACCLCF2</td><td>SWCALOK</td><td>RTCALOK</td><td colspan="2">Reserved</td><td>XCS3ALOK</td><td>XCS2ALOK</td><td>XCS1ALOK</td><td>XCS0ALOK</td></tr>
</table>

7.0 General-Purpose Input/Output (GPIO) Ports

This chapter describes one 8-bit port. A device may include a combination of several ports with different implementations. For device specific implementation, see Section 3.14 on page 70.

7.1 OVERVIEW

The GPIO port is an 8-bit port, connected to eight pins. It features:

- Software capability to control and read pin levels.
- Flexible system notification by several means, based on the pin level or level transition.
- Ability to capture and route events and their associated status.
- Back-drive protected pins.

GPIO port operation is associated with two sets of registers:

- Pin Configuration registers mapped in the Device Configuration space. These registers are used to set up the logical behavior of each pin. There are three registers for each GPIO pin: GPIO Pin Configuration registers 1 and 2 (GPCFG1, GPCFG2) and the GPIO Pin Event Routing register (GPEVR).
- Four 8-bit runtime registers: GPIO Data Out (GPDO), GPIO Data In (GPDI), GPIO Event Enable (GPEVEN) and GPIO Event Status (GPEVST). These registers are mapped in the GPIO device IO space (which is determined by the base address registers in the GPIO Device Configuration). They are used to control and/or read the pin values and to handle system notification. Each runtime register corresponds to the 8-pin port, such that bit ‘n’ in each one of the four registers is associated with GPIOXn pin, where ‘X’ is the port number.

Each GPIO pin is associated with configuration bits and the corresponding bit slice of the four runtime registers, as shown in Figure 35.

The functionality of the GPIO port is divided into basic functionality, which includes the control and reading of the GPIO pins and enhanced functionality, which includes wake-up event detection and system notification. Basic functionality is described in Section 7.2; enhanced functionality is described in Section 7.3.

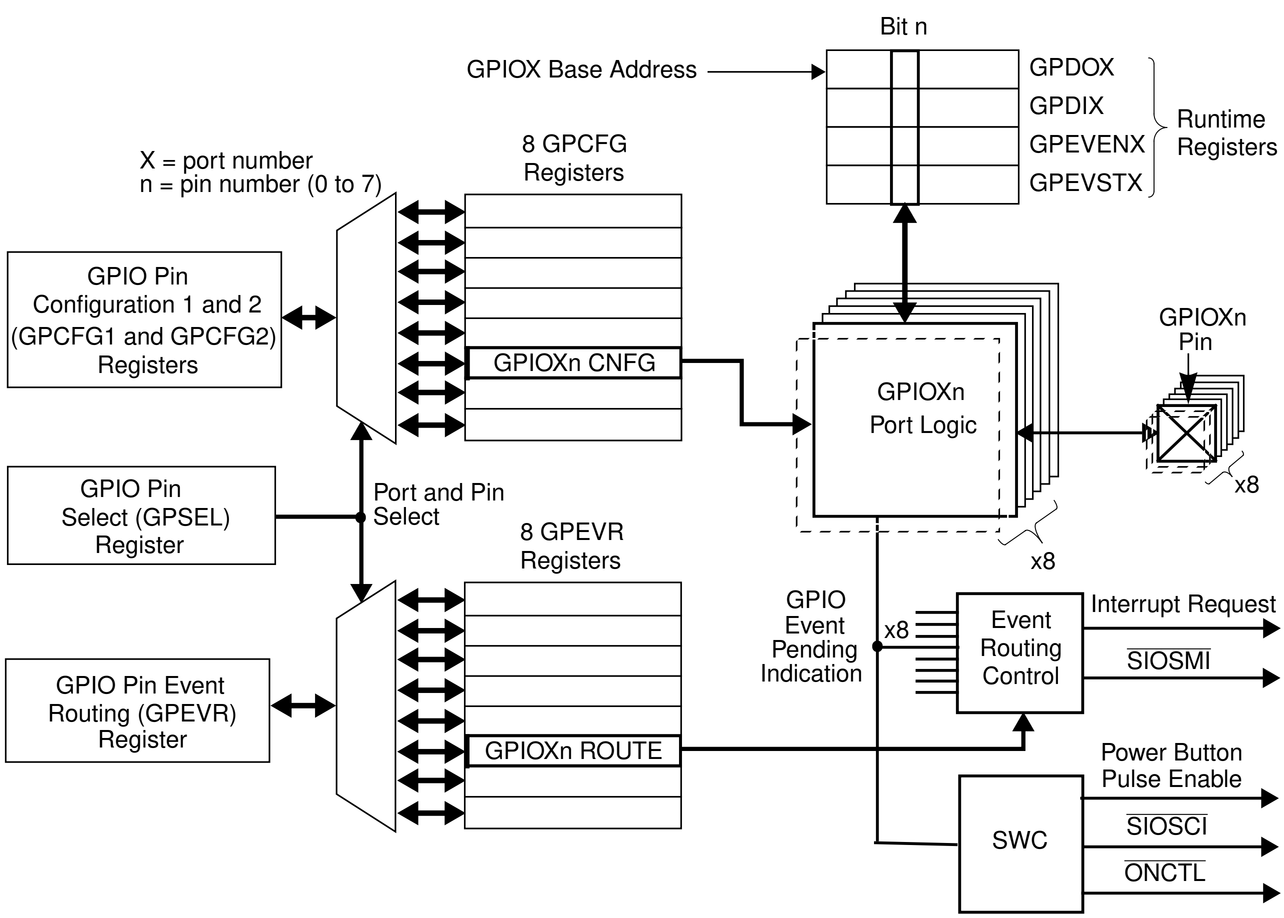


Figure 35. GPIO Port Architecture

7.0 General-Purpose Input/Output (GPIO) Ports (Continued)

7.2 BASIC FUNCTIONALITY

The basic functionality of each GPIO pin is based on four configuration bits and a bit slice of runtime registers GPDO and GPDI. The configuration and operation of a single pin GPIOXn (pin 'n' in port 'X') is shown in Figure 36.

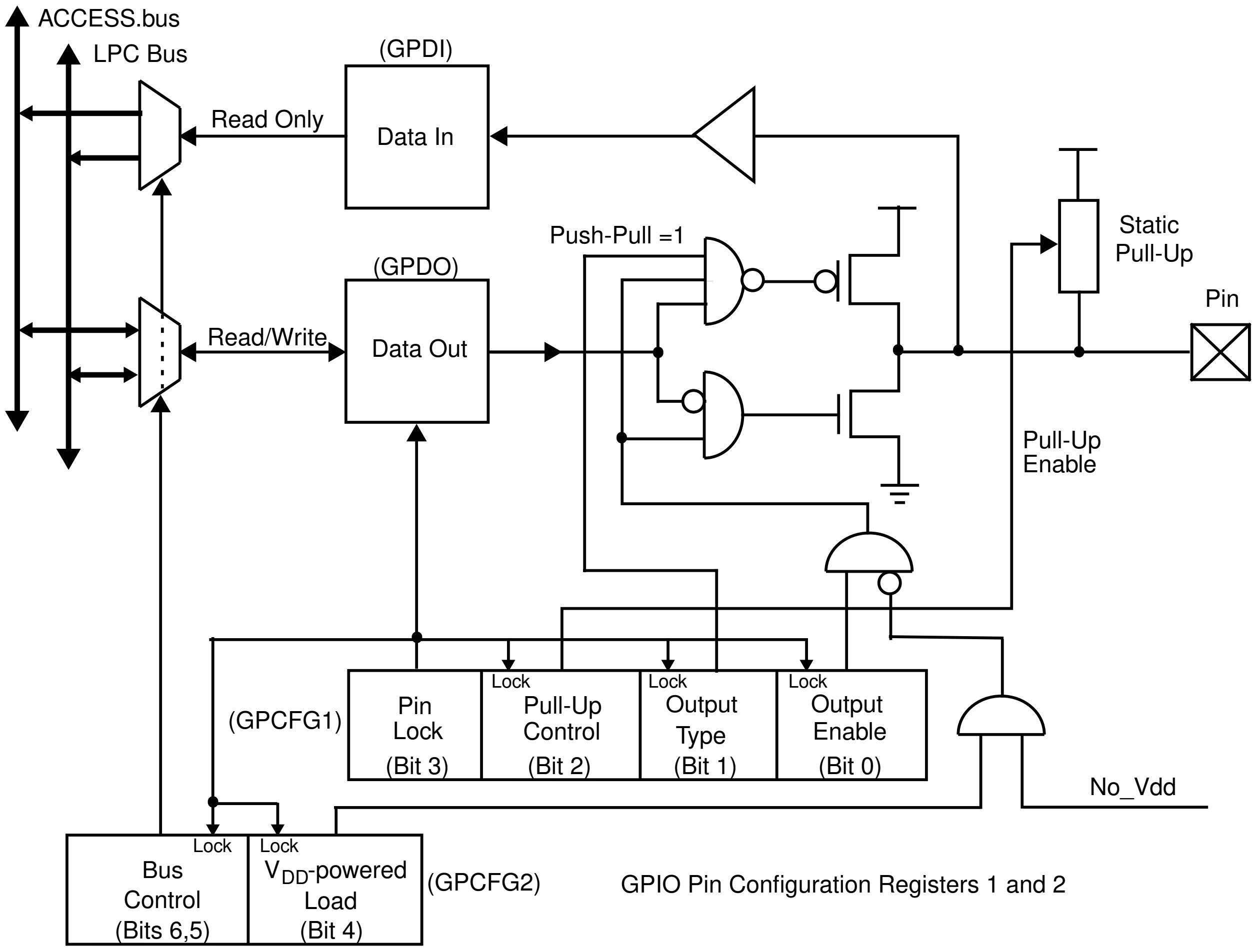


Figure 36. GPIO Basic Functionality

7.2.1 Configuration Options

The GPCFG1 register controls the following basic configuration options:

- Port Direction - Controlled by the Output Enable bit (bit 0).
- Output Type - Push-pull vs. open-drain. It is controlled by Output Buffer Type (bit 1) by enabling/disabling the upper transistor of the output buffer.
- Static Pull-Up - May be added to any type of port (input, open-drain or push-pull). It is controlled by Pull-Up Control (bit 2).
- Pin Lock - GPIO pin may be locked to prevent any changes in the output value and/or the output configuration. The lock is controlled by bit 3. It disables writes to the GPDO register bits, to bits 0-3 of the GPCFG1 register (including the Lock bit itself) and to bits 4-6 of the GPCFG2 register. Once locked, it can be released by reset or by the UNLOCKG bit in the ACBLKCTL register (see Section 6.3.4 on page 128 - **PC87413 and PC87417**).

The GPCFG2 register controls the following basic configuration options:

- Load Protection - Disables the Output Buffer (if enabled), the Static Pull-Up (if enabled) and the Input Buffer (if the Port is not a GPO type) if the specific GPIO pin is connected to a V_{DD}-powered device and the V_{DD} power is not present (No_Vdd). This function is controlled by the V_{DD}-powered Load bit (bit 4).

7.0 General-Purpose Input/Output (GPIO) Ports (Continued)

- Access Control - Limits access to the specific pin from only one of the buses (ACCESS.bus or LPC bus). When access from a bus is disabled, attempted writes to the Basic Functionality configuration registers (GPCFG1 bits 3-0 and GPCFG2 bits 6-4, none of which are shown in Figure 36) and to the corresponding bit in the GPDO register are ignored. Reads from the bits above and from the corresponding bit in the GPDI register are allowed and return the actual bit value. Bus access is controlled by Bus Control bits (bits 6 and 5). After reset, both bits are ‘0’ and access is allowed from both ACCESS.bus and LPC bus. **In the PC87414 and PC87416, this feature is irrelevant because only the LPC bus is available**.

7.2.2 Operation

If the output is enabled, the value that is written to the GPDO register is driven to the pin. Reading from the GPDO register returns its contents regardless of the actual pin value or the port configuration.

The GPDI register is a read-only register. Reading from the GPDI register returns the actual pin value regardless of its source (the port itself or an external device). Writing to this register is ignored.

Activation of the GPIO module is controlled by device-specific configuration bits. When this module is inactive, access through the LPC bus to the runtime registers (GPDI and GPDO) is disabled; however, there is no change in the GPDO value and therefore there is no effect on the outputs of the pins.

7.3 EVENT HANDLING AND SYSTEM NOTIFICATION

The enhanced GPIO port (GPIOE) supports system notification based on event detection. This functionality is based on configuration bits and a bit slice of runtime registers GPEVEN and GPEVST. The configuration and operation of the event detection capability is shown in Figure 37. System notification is described in Section 7.3.2.

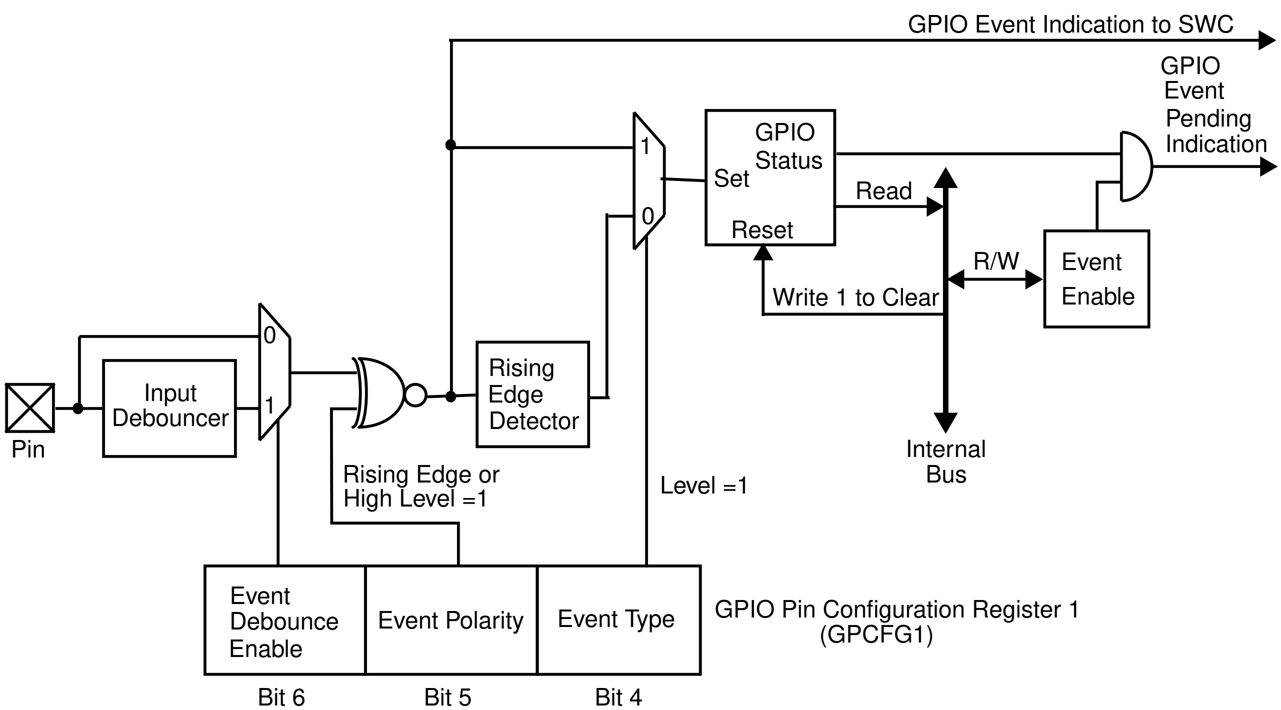


Figure 37. Event Detection

7.3.1 Event Configuration

Each pin in the GPIO port is a potential input event source. The event detection can trigger a system notification upon pre-determined behavior of the source pin. The GPCFG1 register determines the event detection trigger type for the system notification.

7.0 General-Purpose Input/Output (GPIO) Ports (Continued)

Event Debounce Enable

The input signal can be debounced for about 15 msec before entering the detector. To ensure that the signal is stable, the signal state is transferred to the event detector only after a debouncing period during which the signal has no transitions. The debouncer adds a 16 msec delay to both assertion and de-assertion of the event pending indicator (IRQ, SMI, SCI). The debounce is controlled by Event Debounce Enable (bit 6 of the GPCFG1 register).

Event Type and Polarity

Two trigger types of event detection are supported: edge and level. An edge event may be detected upon a source pin transition either from high to low or low to high. A level event may be detected when the source pin is either at high or low level. The trigger type is determined by Event Type (bit 4 of the GPCFG1 register). The direction of the transition (for edge) or the polarity of the active level (for level) is determined by Event Polarity (bit 5 of the GPCFG1 register).

The term *active edge* refers to a change in a GPIO pin level that matches the Event Polarity bit (1 for rising edge and 0 for falling edge). *Active level* refers to the GPIO pin level that matches the Event Polarity bit (1 for high level and 0 for low level). The corresponding bit of the GPEVST register is set by hardware whenever an active edge or an active level is detected regardless of the GPEVEN register setting. Writing 1 to the Status bit clears it to 0. Writing 0 is ignored.

A GPIO pin is in event pending state if an active event occurred (the corresponding bit of the GPEVST register is set) and the corresponding bit of the GPEVEN register is set.

7.3.2 System Notification

System notification on GPIO-triggered events is achieved by asserting at least one of the following output pins:

- Interrupt Request (via the Interrupt Serializer in the LPC Bus Interface).
- System Management Interrupt ($\overline{\text{SIOSMI}}$, via the System Wake-Up Control).

The system notification for each GPIO pin is controlled by the corresponding bit in the GPEVEN register and the bits of the GPEVR register. System notification by a GPIO pin is enabled if the corresponding bit of the GPEVEN register is set to 1. The bits of the GPEVR register select the means of system notification (IRQ or SMI) that the detected GPIO event is routed to. The event routing mechanism is described in Figure 38.

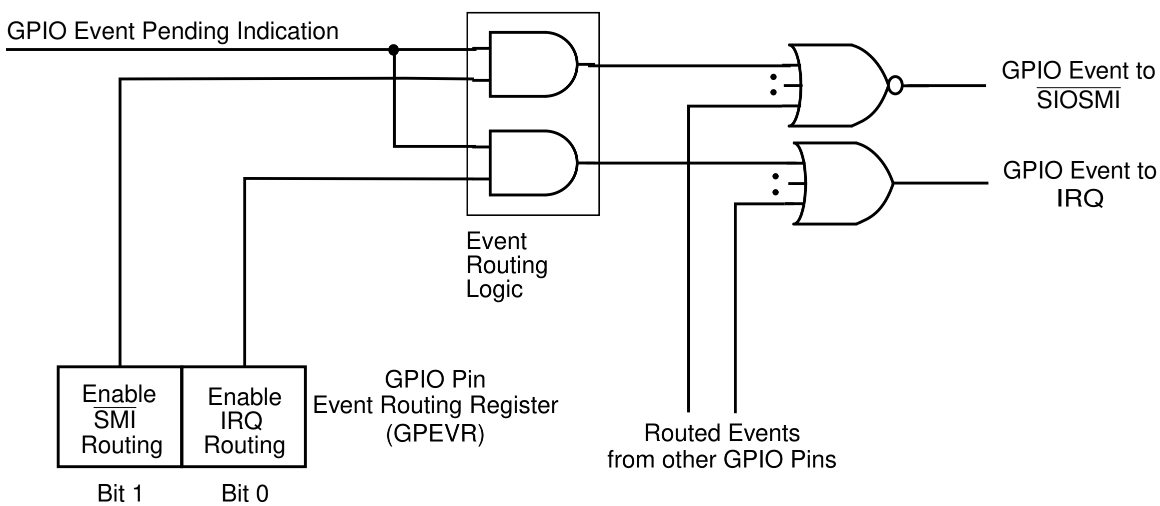


Figure 38. GPIO Event Routing Mechanism for System Notification

The system notification to the target is asserted if at least one GPIO pin is in event pending state.

The selection of the target (the means of system notification) is determined by the GPEVR register. If IRQ is selected as one of the means for the system notification, the specific IRQ number is determined by the IRQ selection procedure of the device configuration. The assertion of IRQ (as a means of system notification) is disabled either when the GPIO functional block is deactivated or when the V_{DD} power is Off.

The assertion of SMI is independent of the activation of the GPIO functional block. SMI from GPIO pins connected to a device powered by V_{DD} (VDDLOAD = 1 in the GPCFG2 register) is disabled when the V_{DD} power is Off. However, SMI from GPIO pins connected to a device powered by V_{SB} (VDDLOAD = 0) is not affected by the status of the V_{DD} power.

7.0 General-Purpose Input/Output (GPIO) Ports (Continued)

System notification through IRQ, SMI or SCI (see Section 9.2.1 on page 162) can be initiated by software by writing to the Data Out bit (in the GPDO register) of a GPIO pin. This is possible only if the output of the corresponding GPIO pin is enabled, pin multiplexing is selected for the GPIO function (see Section 1.3 on page 20) and the GPIO event is routed to IRQ, SMI or SCI. System notification is asserted according to the actual level at the GPIO pin driven by the GPIO output and/or by external circuitry. The level driven by the GPIO output should not cause a contention with the level driven by the external circuitry.

A pending edge event may be cleared by clearing the corresponding GPEVST bit. However, a level event source may not be released by software (except for disabling the source) as long as the pin is at active level. When level event is used, it is also recommended to disable the input debouncer.

Upon deactivation of the GPIO functional block and while the V_{DD} power is Off, access through the LPC bus to the runtime registers (GPEVST and GPEVEN) is disabled. All means of system notification that include the target IRQ number are detached from the GPIO and de-asserted.

When the V_{DD} power is Off, the status bits of the GPIO pins connected to a V_{DD}-powered device (VDDLOAD = 1) are cleared, however the status bits of the GPIO pins connected to a V_{SB}-powered device (VDDLOAD = 0) is not affected.

Before enabling any system notification, it is recommended to set the desired event configuration and then verify that the status registers are cleared.

7.4 GPIO PORT REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from a specific register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

7.4.1 GPIO Pin Configuration Registers Structure

For each Port, there is a group of eight identical sets of configuration registers. Each set is associated with one GPIO pin. The entire group is mapped to the PnP configuration space. The mapping scheme is based on the GPSEL register (see Section 3.14.3 on page 72), which functions as an index register, and the specific GPCFG1, GPEVR and GPCFG2 registers that reflect the configuration of the currently selected pin (see Table 34). All these registers are V_{SB} powered.

Table 34. GPIO Configuration Registers

Index	Configuration Register or Action	Type	Power Well	Reset
F0h	GPIO Pin Select register (GPSEL).	R/W	V_{SB}	00h
F1h	GPIO Pin Configuration register 1 (GPCFG1).	R/W	V_{SB}	Note[1]
F2h	GPIO Pin Event Routing register (GPEVR).	R/W	V_{SB}	01h
F3h	GPIO Pin Configuration register 2 (GPCFG2).	R/W	V_{SB}	00h

1. See Section 3.14.3 on page 72.

7.0 General-Purpose Input/Output (GPIO) Ports (Continued)

7.4.2 GPIO Port Runtime Register Map

All these registers are V_{SB} powered.

Offset	Mnemonic	Register Name	Type	Power Well	Reset	Section
Device specific[1]	GPDO	GPIO Data Out	R/W	V_{SB}	FFh	7.4.3
Device specific[1]	GPDI	GPIO Data In	RO	V_{SB}	-	7.4.4
Device specific[1]	GPEVEN	GPIO Event Enable	R/W	V_{SB}	00h	7.4.5
Device specific[1]	GPEVST	GPIO Event Status	R/W1C	V_{SB}	00h	7.4.6

1. The location of this register is defined in Section 3.14.1 on page 70.

7.4.3 GPIO Data Out Register (GPDO)

Power Well:V_{SB}

Location:Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	DATAOUT							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**DATAOUT (Data Out).** Bits 7-0 correspond to pins 7-0 of the specific Port. The value of each bit determines the value driven on the corresponding GPIO pin when its output buffer is enabled. Writing to the bit latches the written data unless the bit is locked by the GPCFG register Lock bit. Reading the bit returns its value regardless of the pin value and configuration. 0: Corresponding pin driven to low 1: Corresponding pin driven or released (according to buffer type selection) to high (default)

7.4.4 GPIO Data In Register (GPDI)

Power Well:V_{SB}

Location:Device specific

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	DATAIN							
Reset	X	X	X	X	X	X	X	X

Bit	Description
7-0	**DATAIN (Data In).** Bits 7-0 correspond to pins 7-0 of the specific Port. Reading each bit returns the value of the corresponding GPIO pin. Pin configuration and the GPDO register value may influence the pin value. Write is ignored. 0: Corresponding pin level low 1: Corresponding pin level high

7.0 General-Purpose Input/Output (GPIO) Ports (Continued)

7.4.5 GPIO Event Enable Register (GPEVEN)

Power Well:V_{SB}

Location:Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**EVTENA**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**EVTENA (Event Enable).** Bits 7-0 correspond to pins 7-0 of the specific Port. Each bit enables system notification by the corresponding GPIO pin. The bit has no effect on the corresponding Status bit in the GPEVST register. 0: Event Pending by corresponding GPIO pin masked 1: Event Pending by corresponding GPIO pin enabled

7.4.6 GPIO Event Status Register (GPEVST)

Power Well:V_{SB}

Location:Device specific

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**EVTSTAT**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**EVTSTAT (Event Status).** Bits 7-0 correspond to pins 7-0 of the specific Port. The setting of each bit is independent of the Event Enable bit in the GPEVEN register. An active event sets the Status bit, which may be cleared only by software writing 1 to the bit. 0: No active edge or level detected since last cleared 1: Active edge or level detected

8.0 Real-Time Clock (RTC)

8.1 OVERVIEW

The RTC provides timekeeping and calendar management capabilities. It uses a 32.768 KHz signal as the basic clock for timekeeping. The RTC also includes 242 bytes of battery-backed RAM for general-purpose use.

The RTC provides the following functions:

- Accurate timekeeping and calendar management.
- Alarm at a predetermined time and/or date.
- Three programmable interrupt sources.
- Valid timekeeping during power-down by utilizing external battery backup.
- 242 bytes of battery-backed RAM.
- RAM lock schemes to protect its content.
- Internal oscillator circuit (the crystal itself is off-chip) or external clock supply for the 32.768 KHz clock.
- A century counter.
- PnP support:
  - — Relocatable index and data registers
  - — Module access enable/disable option
  - — Host interrupt enable/disable option
- Additional low-power features such as:
  - — Automatic switching from V_{BAT} to V_{SB}
  - — Internal power monitoring on the VRT bit
  - — Oscillator disabling to conserve battery power during storage
- Software compatible with the DS1287 and MC146818.

8.2 FUNCTIONAL DESCRIPTION

8.2.1 Bus Interface

The RTC function is initially mapped to the default ServerI/O locations at indexes 70h to 73h (two Index/Data pairs). These locations may be reassigned in compliance with Plug and Play requirements.

8.2.2 RTC Clock Generation

The RTC uses a 32.768 KHz clock signal as the basic clock for timekeeping. The 32.768 KHz clock is supplied by either the internal oscillator circuit or by an external oscillator (see Sections 8.2.3 and 8.2.4).

8.2.3 Internal Oscillator

The internal oscillator employs an external crystal connected to the on-chip amplifier. The on-chip amplifier is accessible on the 32KX1 input pin and 32KX2 output pin. See Figure 39 for the recommended external circuit; see Table 35 on page 143 for a listing of the circuit components. The oscillator may be disabled in certain conditions. See Section 8.2.12 on page 147 for more details.

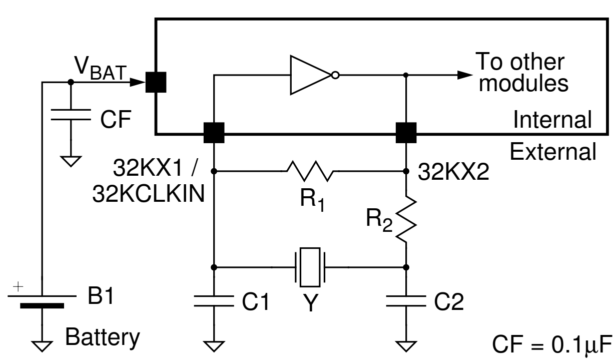


Figure 39. Recommended Oscillator External Circuitry

8.0 Real-Time Clock (RTC) (Continued)

Table 35. Crystal Oscillator Circuit Components

Component	Parameters	Values	Tolerance
Crystal	Resonance Frequency	32.768 KHz Parallel mode	User defined
	Type	N-Cut or XY-bar	
	Serial Resistance	40 KΩ	Max
	Quality Factor, Q	35000	Min
	Shunt Capacitance	2 pF	Max
	Load Capacitance, C_L	9-13 pF	
	Temperature Coefficient	User-defined	
Resistor R_1	Resistance	20 MΩ	5%
Resistor R_2	Resistance	510 KΩ	5%
Capacitor C_1	Capacitance	10 pF	5%
Capacitor C_2	Capacitance	10 pF	5%

External Elements

Choose C1 and C2 capacitors (see Figure 39) to match the crystal's load capacitance. The load capacitance C_L "seen" by crystal Y is comprised of C_1 in series with C_2 and in parallel with the parasitic capacitance of the circuit. The parasitic capacitance is caused by the chip package, board layout and socket (if any) and can vary from 0 to 8 pF. The rule of thumb in choosing these capacitors is:

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_{PARASITIC}$$

Oscillator Start-Up

The oscillator starts to generate 32.768 KHz pulses to the RTC after about t_{32KW} from when V_{BAT} is higher than V_{BATMIN} (2.4V) or V_{SB} is higher than V_{SBON} (2.5V). The oscillation amplitude on the X2C pin stabilizes to its final value (approximately 0.4V peak-to-peak around 0.7V DC) in about 1 sec.

C_1 can be trimmed to achieve precisely 32.768 KHz. For highly accurate timekeeping, use crystal and capacitors with low tolerance and temperature coefficients.

8.2.4 External Oscillator

32.768 KHz can be applied from an external clock source, as shown in Figure 40.

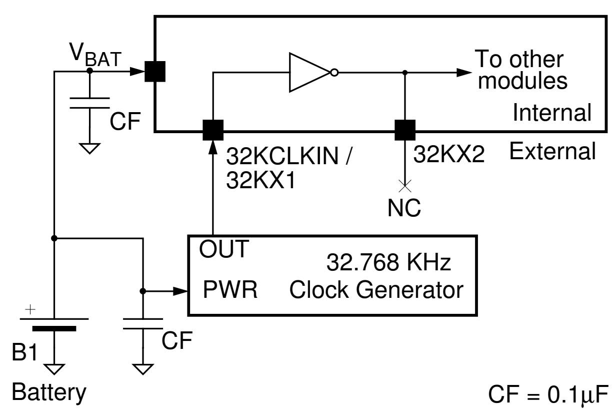


Figure 40. External Oscillator Connections

Connections

Connect the clock to the 32KCLKIN pin, leaving the oscillator output, 32KX2, unconnected.

8.0 Real-Time Clock (RTC) (Continued)

Signal Parameters

The signal levels must conform to the voltage level requirements for 32KCLKIN/32KX1 stated in Section 11.2 on page 233. The signal must have a duty cycle of approximately 50%. To oscillate during power-down, the signal must be sourced from a battery-backed source. This assures that the RTC delivers updated time/calendar information.

8.2.5 Timing Generation

The timing generation function divides the 32.768 KHz clock by 2^{15} to derive a 1 Hz signal, which serves as the input for the seconds counter. This is performed by a divider chain composed of 15 divide-by-two latches, as shown in Figure 41.

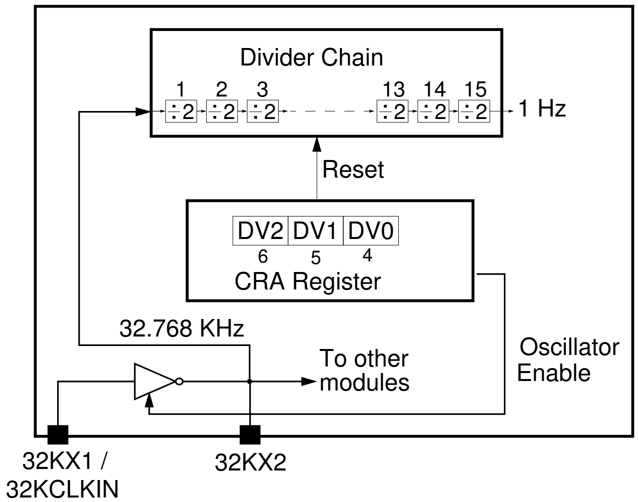


Figure 41. Divider Chain Control

Bits 6-4 (DV2-0) of the CRA register control the following functions:

- Normal operation of the divider chain (counting).
- Divider chain reset to 0.
- Oscillator activity when only V_{BAT} power is present (backup state).

The divider chain can be activated by setting Normal Operation mode (bits 6-4 of CRA = 010b). The first update occurs 500 ms after divider chain activation.

Bits 3-0 of the CRA register select one the of 15 taps from the divider chain to be used as a periodic interrupt. The periodic flag becomes active after half of the programmed period has elapsed, following divider chain activation.

See Section 8.3.13 on page 154 for more details.

8.2.6 Timekeeping

Data Format

Time is kept in BCD or binary format, as determined by bit 2 (DM) of Control Register B (CRB), and in either 12 or 24-hour format, as determined by bit 1 of this register.

Note: When changing the above formats, re-initialize all the time registers.

Daylight Saving

Daylight saving time exceptions are handled automatically, as described in the RTC Control Register B (CRB) in Section 8.3.2 on page 150.

Leap Years

Leap year exceptions are handled automatically by the internal calendar function (every four years, February is extended to 29 days).

8.0 Real-Time Clock (RTC) (Continued)

8.2.7 Updating

The time and calendar registers are updated once per second regardless of bit 7 (SET) of the CRB register. Since the time and calendar registers are updated serially, unpredictable results may occur if they are accessed during the update. Therefore, it is essential to ensure that reading or writing to the time storage locations does not coincide with a system update of these locations. There are four methods to avoid this contention.

Method 1

1. Set bit 7 of the CRB register to 1. This takes a “snapshot” of the internal time registers and loads them into the user copy registers. The user copy registers are seen when accessing the RTC from outside and are part of the double buffering mechanism. This bit may be kept set for up to 1 second, since the time/calendar chain continues to be updated once per second.
2. Read or write the required registers (since bit 7 is set, the access is to the user copy registers). If a read operation is performed, the information read is correct from the time bit 7 was set. If a write operation is performed, the write is only to the user copy registers.
3. Reset bit 7 to 0. During the transition, the user copy registers update the internal registers, using the double buffering mechanism to ensure that the update is performed between two time updates. This mechanism enables new time parameters to be loaded in the RTC.

Method 2

1. Access the RTC registers after detection of an Update Ended interrupt. The detection interrupt implies that an update has just been completed and 999 ms remain until the next update.
2. To detect an Update Ended interrupt, either:
   — Poll bit 4 of the CRC register.
   — Use the following interrupt routine:
      a) Set bit 4 of the CRB register.
      b) Wait for an interrupt from interrupt pin.
      c) Clear the IRQF flag of the CRC register before exiting the interrupt routine.

Method 3

Poll bit 7 of the CRA register. The update occurs 244 µs after this bit goes high. Therefore, if a 0 is read, the time registers remain stable for at least 244 µs.

Method 4

Use a periodic interrupt routine to determine if an update cycle is in progress, as follows:

1. Set the periodic interrupt to the desired period.
2. Set bit 6 of the CRB register to enable the interrupt from periodic interrupt.
3. Wait for the appearance of a periodic interrupt, which indicates that the period represented by the following expression remains until another update occurs:

   [(Period of periodic interrupt / 2) + 244 µs]

8.2.8 Alarms

The timekeeping function can be set to generate an alarm when the current time reaches a stored alarm time. After each RTC time update (every 1 second), the seconds, minutes, hours, date-of-month and month counters are compared with their corresponding registers in the alarm settings. If they are equal, bit 5 of the CRC register is set to 1 and sent to the SWC as an alarm signal. If the Alarm Interrupt Enable bit was previously set (bit 5 of the CRB register), the interrupt request pin is also active.

Any alarm register may be set to Unconditional Match by setting bits 7 and 6 to binary ‘11’. This combination, not used by any BCD or binary time codes, results in a periodic alarm. The rate of this periodic alarm is determined by the registers that were set to Unconditional Match.

For example, if all but the seconds and minutes alarm registers are set to Unconditional Match, an interrupt is generated every hour at the specified minute and second. If all but the seconds, minutes and hours alarm registers are set to Unconditional Match, an interrupt is generated every day at the specified hour, minute and second.

8.0 Real-Time Clock (RTC) (Continued)

8.2.9 Power Supply

The device is supplied from three supply voltages, as shown in Figure 42:

- System power supply voltage, V_{DD}.
- System standby power supply voltage, V_{SB}.
- Backup voltage, from low-capacity Lithium battery V_{BAT}.

A standby voltage (V_{SB}) from the external AC/DC power supply powers the RTC under normal conditions.

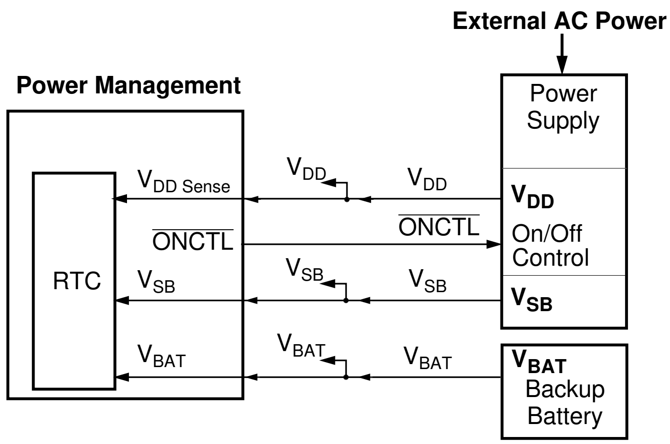
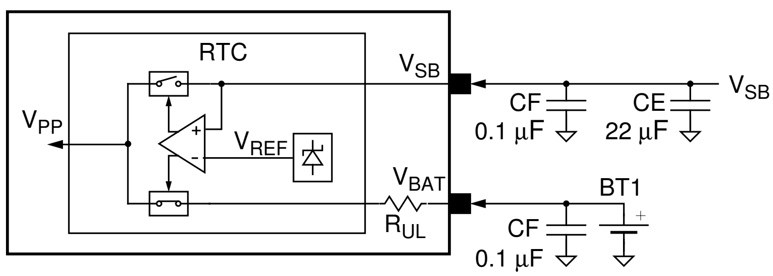


Figure 42. Power Supply Connections

Figure 43 shows a typical battery configuration. No external diode is required to meet the UL standard due to the internal switch and internal serial resistor R_{UL}(see the MCRS parameter in Section 11.1.2 on page 231).



1. Place a 0.1 µF capacitor on each V_{SB} power supply pin and on V_{BAT} as close to the pin as possible.
2. Place a 10-47 µF capacitor on the common V_{SB} power supply net as close to the device as possible.

Figure 43. Typical Battery Configuration

The RTC is supplied from one of two power supplies, V_{SB} or V_{BAT}, depending on their voltage levels. An internal voltage comparator delivers the control signals to a pair of switches. Battery backup voltage V_{BAT} maintains the correct time and saves the CMOS memory when the V_{SB} voltage is absent due to power failure or disconnection of the external AC/DC input power supply or V_{SB} main battery.

To ensure that the module uses power from V_{SB} and not from V_{BAT}, the V_{SB} voltage must be maintained above its minimum, as detailed in Section 11.1.5 on page 232.

The actual voltage point where the module switches from V_{BAT} to V_{SB} is lower than the minimum workable battery voltage but high enough to guarantee the correct functionality of the oscillator and the CMOS RAM.

Figure 44 shows typical battery current consumption during battery-backed operation; Figure 45 shows the same during normal operation.

8.0 Real-Time Clock (RTC) (Continued)

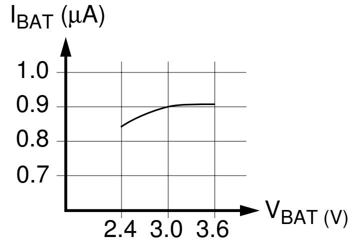
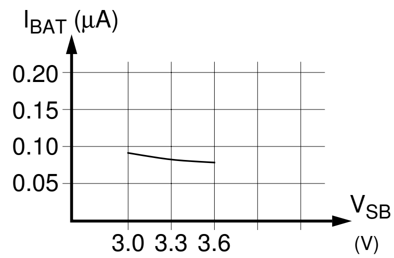


Figure 44. Typical Battery Current During Battery-Backed Power Mode



Note: Battery voltage in this test is 3.0V.

Figure 45. Typical Battery Current During Normal Operation Mode

8.2.10 System Bus Lockout

During power On or power Off, spurious bus transactions from the host may occur. To protect the data in the RTC internal registers from being corrupted, all inputs are automatically locked out. The lockout condition is asserted when V_{SB} is lower than V_{SBON} at V_{SB} power-on or V_{SBOFF} at V_{SB} power-off.

8.2.11 Power-Up Detection

When system power is restored after a power failure or power off state (V_{SB}=0), the lockout condition continues for a delay of 62 ms (minimum) to 125 ms (maximum) after the RTC switches from battery to system power.

The lockout condition is switched off immediately in the following situations:

- If the Divider Chain Control bits, DV0-2 (bits 6-4 in the CRA register), specify a normal operation mode (010), all input signals are enabled immediately on detection of system voltage above V_{SBON}.
- When battery voltage is below V_{BATDCT} and $\overline{\text{LRESET}}$ is 0, all input signals are enabled immediately on detection of system voltage above V_{SBON}. This also initializes registers at offsets 00h through 0Dh.
- If bit 7 (VRT) of the CRD register is 0, all input signals are enabled immediately on detection of system voltage above V_{SBON}.

8.2.12 Oscillator Activity

The RTC oscillator is active if:

- V_{SB} power supply is higher than V_{SBON} regardless of the battery voltage, V_{BAT}.
- V_{BAT} power supply is higher than V_{BATMIN} whether or not V_{SB} is present.

The RTC oscillator is disabled if:

- During power-down (V_{BAT} only), if the battery voltage drops below V_{BATMIN}, Battery Fail state may be entered. In this case, the oscillator may stop oscillating and memory contents may be corrupted or lost.
- Software writes 00h to DV2-0 bits of the CRA register and V_{SB} is removed. This disables the oscillator and decreases the power consumption from the battery connected to the V_{BAT} pin. When disabling the oscillator, the CMOS RAM is not affected as long as the battery is present at a correct voltage level.

8.0 Real-Time Clock (RTC) (Continued)

If the RTC oscillator becomes inactive, the following features are dysfunctional/disabled:

- Timekeeping.
- Periodic interrupt.
- Alarm.

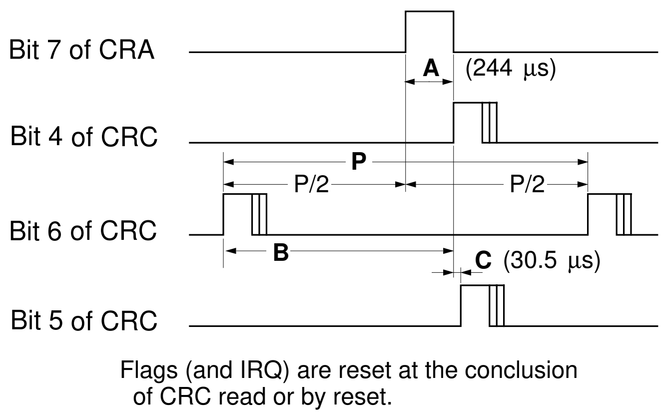
8.2.13 Interrupt Handling

The RTC has a single Interrupt Request line which handles the following three interrupt conditions:

- Periodic interrupt.
- Alarm interrupt.
- Update end interrupt.

The interrupts are generated if the respective enable bits in the CRB register are set prior to an interrupt event occurrence. Reading the CRC register clears all interrupt flags. Thus, when multiple interrupts are enabled, the interrupt service routine must first read and store the CRC register and then deal with all pending interrupts by referring to this stored status.

If an interrupt is not serviced before a second occurrence of the same interrupt condition, the second interrupt event is lost. Figure 46 illustrates the interrupt and status timing in the RTC.



A: Update In Progress bit high before update occurs = 244 µs
B: Periodic interrupt to update = (P/2 + A)
C: Update to Alarm Interrupt = 30.5 µs
P: Periodic interrupt cycle (programmed by RS3-0 of CRA)

Figure 46. Interrupt/Status Timing

8.2.14 Battery-Backed RAMs and Registers

The RTC has two battery-backed RAMs and 17 registers used by the logical units themselves. Battery-backup power enables information retention during system power down.

The RAMs are:

- Standard RAM.
- Extended RAM.

The memory maps and register content of the RAMs are illustrated in Section 8.6 on page 160.

The first 14 bytes and three programmable bytes of the Standard RAM are overlaid by time, alarm data and control registers. The remaining 111 bytes are general-purpose memory.

Registers with reserved bits must be written using the “Read-Modify-Write” method.

All register locations within the device are accessed by the RTC Index and Data registers (at base address and base address+1). The Index register points to the register location being accessed. The Data register contains the data to be transferred to or from the location. An additional 128 bytes of battery-backed RAM (also called Extended RAM) may be accessed via a second pair of Index and Data registers pointed at by the secondary base address and base address+1.

Access to the two RAMs may be locked. For details see the RAM Lock Register (RLR) in Section 3.16.3 on page 88.

8.0 Real-Time Clock (RTC) (Continued)

8.3 RTC REGISTERS

The RTC configuration registers can be accessed at any time during normal or standby operation; i.e., when V_{SB} and/or V_{DD} are within the recommended operation range. Access to the RTC configuration registers is disabled during battery-backed operation.

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write.
- R = Read from a specific register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

8.3.1 RTC Configuration Registers Structure

The RTC configuration registers can be accessed at any time during normal or standby operation; i.e., when V_{SB} and/or V_{DD} are within the recommended operation range. Access to the RTC configuration registers is disabled during battery-backed operation. See Section 3.16 on page 87 for a description of the Configuration registers.

Table 36. RTC Configuration Register Map

Index	RTC Configuration Register or Action	Type	Power Well	Reset
F0h	RAM Lock Register (RLR).	R/W1S	V_{SB}	00h
F1h	Date-of-Month Alarm Register Offset (DOMAO).	R/W	V_{SB}	00h
F2h	Month Alarm Register Offset (MONAO).	R/W	V_{SB}	00h
F3h	Century Register Offset (CENO).	R/W	V_{SB}	00h

8.0 Real-Time Clock (RTC) (Continued)

8.3.2 RTC Runtime Register Map

The RTC runtime registers can be accessed at any time during normal or standby operation; i.e., when V_{SB} and/or V_{DD} are within the recommended operation range. The access is disabled during battery-backed operation. Write operation to these registers is also disabled if bit 7 of the CRD register is 0 (see Section 8.3.16 on page 157).

Note: Before attempting to perform any start-up procedures, read the explanation of bit 7 (VRT) of the CRD register (see Section 8.3.16 on page 157).

See Section 8.6 on page 160 for a detailed description of the memory map for the RTC registers.

This section describes the RTC Timing and Control registers that control basic RTC functionality. All registers are V_{PP} powered.

Index	Mnemonic	Name	Type	Power Well	Reset	Section
00h	SEC	Seconds Register	R/W	V_{PP}	V_{PP} PUR	8.3.3
01h	SECA	Seconds Alarm Register	R/W	V_{PP}	V_{PP} PUR	8.3.4
02h	MIN	Minutes Register	R/W	V_{PP}	V_{PP} PUR	8.3.5
03h	MINA	Minutes Alarm Register	R/W	V_{PP}	V_{PP} PUR	8.3.6
04h	HOR	Hours Register	R/W	V_{PP}	V_{PP} PUR	8.3.7
05h	HORA	Hours Alarm Register	R/W	V_{PP}	V_{PP} PUR	8.3.8
06h	DOW	Day-of-Week Register	R/W	V_{PP}	V_{PP} PUR	8.3.9
07h	DOM	Date-of-Month Register	R/W	V_{PP}	V_{PP} PUR	8.3.10
08h	MON	Month Register	R/W	V_{PP}	V_{PP} PUR	8.3.11
09h	YER	Year Register	R/W	V_{PP}	V_{PP} PUR	8.3.12
0Ah	CRA	RTC Control Register A	Varies per bit	V_{PP}	Bit specific	8.3.13
0Bh	CRB	RTC Control Register B	R/W	V_{PP}	Bit specific	8.3.14
0Ch	CRC	RTC Control Register C	R/O	V_{PP}	Bit specific	8.3.15
0Dh	CRD	RTC Control Register D	R/O	V_{PP}	V_{PP} PUR	8.3.16
Programmable[1] by DOMAO	DOMA	Date-of-Month Alarm Register	R/W	V_{PP}	V_{PP} PUR	8.3.17
Programmable[1] by MONAO	MONA	Month Alarm Register	R/W	V_{PP}	V_{PP} PUR	8.3.18
Programmable[1] by CENO	CEN	Century Register	R/W	V_{PP}	V_{PP} PUR	8.3.19

1. Overlaid on RAM bytes in range 0Eh-7Fh.

8.3.3 Seconds Register (SEC)

Power Well: V_{PP}

Location: Index 00h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Seconds Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Seconds Data.** Values may be 00 to 59 in BCD format or 00 to 3B in Binary format.

8.0 Real-Time Clock (RTC) (Continued)

8.3.4 Seconds Alarm Register (SECA)

Power Well: V_{PP}

Location: Index 01h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Seconds Alarm Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Seconds Alarm Data.** Values may be 00 to 59 in BCD format or 00 to 3B in Binary format. When bits 7 and 6 are both set to one (‘11’), unconditional match is selected.

8.3.5 Minutes Register (MIN)

Power Well:V_{PP}

Location: Index 02h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Minutes Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Minutes Data.** Values may be 00 to 59 in BCD format or 00 to 3B in Binary format.

8.3.6 Minutes Alarm Register (MINA)

Power Well:V_{PP}

Location: Index 03h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Minutes Alarm Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Minutes Alarm Data.** Values may be 00 to 59 in BCD format or 00 to 3B in Binary format. When bits 7 and 6 are both set to one (‘11’), unconditional match is selected.

8.0 Real-Time Clock (RTC) (Continued)

8.3.7 Hours Register (HOR)

Power Well:V_{PP}

Location: Index 04h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Hours Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Hours Data.** For 12-Hour mode, values may be 01 to 12 (AM) and 81 to 92 (PM) in BCD format or 01 to 0C (AM) and 81 to 8C (PM) in Binary format. For 24-Hour mode, values may be 0 to 23 in BCD format or 00 to 17 in Binary format.

8.3.8 Hours Alarm Register (HORA)

Power Well:V_{PP}

Location: 05h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Hours Alarm Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Hours Alarm Data.** For 12-Hour mode, values may be 01 to 12 (AM) and 81 to 92 (PM) in BCD format or 01 to 0C (AM) and 81 to 8C (PM) in Binary format. For 24-Hour mode, values may be 0 to 23 in BCD format or 00 to 17 in Binary format. When bits 7 and 6 are both set to one (‘11’), unconditional match is selected.

8.3.9 Day-of-Week Register (DOW)

Power Well:V_{PP}

Location: Index 06h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Day-of-Week Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Day-of-Week Data.** Values may be 01 to 07 in BCD format or 01 to 07 in Binary format.

8.0 Real-Time Clock (RTC) (Continued)

8.3.10 Date-of-Month Register (DOM)

Power Well:V_{PP}

Location: Index 07h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Date-of-Month Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Date-of-Month Data.** Values may be 01 to 31 in BCD format or 01 to 1F in Binary format.

8.3.11 Month Register (MON)

Power Well:V_{PP}

Location: Index 08h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Month Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Month Data.** Values may be 01 to 12 in BCD format or 01 to 0C in Binary format.

8.3.12 Year Register (YER)

Power Well:V_{PP}

Location: Index 09h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Year Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Year Data.** Values may be 00 to 99 in BCD format or 00 to 63 in Binary format.

8.0 Real-Time Clock (RTC) (Continued)

8.3.13 RTC Control Register A (CRA)

This register controls test selection in addition to other functions. This register cannot be written before reading bit 7 of the CRD register.

Power Well:V_{PP}

Location: Index 0Ah

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Update in Progress**	**Divider Chain Control**			**Periodic Interrupt Rate Select**			
Reset	0	0	1	0	0	0	0	0

Bit	Type	Description
7	RO	**Update in Progress.** This bit is not affected by reset. It reads 0 when bit 7 of the CRB register is 1. 0: Timing registers not updated within 244 µs 1: Timing registers updated within 244 µs
6-4	R/W	**Divider Chain Control.** These bits control the configuration of the divider chain for timing generation (see Table 37). They are cleared to 000 as long as bit 7 of the CRD register reads 0.
3-0	R/W	**Periodic Interrupt Rate Select.** These bits select one of 15 output taps from the clock divider chain to control the rate of the periodic interrupt (see Table 38 and Figure 41 on page 144). They are cleared to 000 as long as bit 7 of the CRD register reads 0.

Table 37. Divider Chain Control and Test Selection

DV2 (CRA6)	DV1 (CRA5)	DV0 (CRA4)	Configuration
0	0	X	Oscillator Disabled
0	1	0	Normal Operation
0	1	1	Reserved
1	0	X	
1	1	X	Divider Chain Reset

8.0 Real-Time Clock (RTC) (Continued)

Table 38. Periodic Interrupt Rate Encoding

Rate Select 3 2 1 0	Periodic Interrupt Rate (ms)	Divider Chain Output
0 0 0 0	No interrupts	
0 0 0 1	3.906250	7
0 0 1 0	7.812500	8
0 0 1 1	0.122070	2
0 1 0 0	0.244141	3
0 1 0 1	0.488281	4
0 1 1 0	0.976562	5
0 1 1 1	1.953125	6
1 0 0 0	3.906250	7
1 0 0 1	7.812500	8
1 0 1 0	15.625000	9
1 0 1 1	31.250000	10
1 1 0 0	62.500000	11
1 1 0 1	125.000000	12
1 1 1 0	250.000000	13
1 1 1 1	500.000000	14

8.0 Real-Time Clock (RTC) (Continued)

8.3.14 RTC Control Register B (CRB)

Power Well: V_{PP}

Location: Index 0Bh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SETMODE**	**PIE**	**AIE**	**UIE**	**Reserved**	**DATMODE**	**HRMODE**	**DSVMODE**
Reset	0	0	0	0	0	0	0	0

.

Bit	Description
7	**SETMODE (Set Mode).** This bit is reset at V_{PP} power-up reset only. 0: Timing updates occur normally 1: User copy of time is frozen, allowing the time registers to be accessed whether or not an update occurs
6	**PIE (Periodic Interrupt Enable).** Bits 3-0 of the CRA register determine the rate at which this interrupt is generated. It is cleared to 0 on RTC reset (i.e., V_{SB} Power-Up reset) or when RTC is disabled. 0: Disabled 1: Enabled
5	**AIE (Alarm Interrupt Enable).** This interrupt is generated immediately after a time update in which the seconds, minutes, hours, date and month time equal their respective alarm counterparts. It is cleared to 0 as long as bit 7 of the CRD register reads 0. 0: Disabled 1: Enabled
4	**UIE (Update Ended Interrupt Enable).** This interrupt is generated when an update occurs. It is cleared to 0 on RTC reset (i.e., V_{SB} Power-Up reset) or when the RTC is disabled. 0: Disabled 1: Enabled
3	**Reserved.** This bit is defined as “Square Wave Enable” by MC146818 and is not supported by the RTC. It is always read as 0.
2	**DATMODE (Data Mode).** This bit is reset at V_{PP} power-up reset only. 0: BCD format enabled 1: Binary format enabled
1	**HRMODE (Hour Mode).** This bit is reset at V_{PP} power-up reset only. 0: 12-hour format enabled 1: 24-hour format enabled
0	**DSVMODE (Daylight Saving).** This bit is reset at V_{PP} power-up reset only. 0: Disabled 1: Enabled: In the spring, time advances from 1:59:59 AM to 3:00:00 AM on the first Sunday in April. In the fall, time returns from 1:59:59 AM to 1:00:00 AM on the last Sunday in October.

8.0 Real-Time Clock (RTC) (Continued)

8.3.15 RTC Control Register C (CRC)

Power Well: V_{PP}

Location: Index 0Ch

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**IRQF**	**PIF**	**AF**	**UF**	**Reserved**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**IRQF (IRQ Flag).** This bit mirrors the value on the interrupt output signal. When interrupt is active, this bit is 1. To clear this bit (and deactivate the interrupt pin), perform a read on the CRC register. This read also clears flag bits UF, AF and PF. 0: IRQ inactive 1: IRQ active, according to the equation: ((UIE and UF) or (AIE and AF) or (PIE and PF)); see Section 8.3.14 on page 156
6	**PIF (Periodic Interrupt Flag).** This bit is cleared to 0 on RTC reset (i.e., hardware or software reset) or when the RTC is disabled. In addition, this bit is cleared to 0 when this register is read. 0: No transition occurred on the selected tap since the last read 1: Transition occurred on the selected tap of the divider chain
5	**AIF (Alarm Interrupt Flag).** This bit is cleared to 0 as long as bit 7 of the CRD register is reads 0. In addition, this bit is cleared to 0 when this register is read. 0: No alarm detected since the last read 1: Alarm condition detected
4	**UIF (Update Ended Interrupt Flag).** This bit is cleared to 0 on RTC reset (i.e., hardware or software reset) or the RTC disabled. In addition, this bit is cleared to 0 when this register is read. 0: No update occurred since the last read 1: Time registers updated
3-0	**Reserved.**

8.3.16 RTC Control Register D (CRD)

Power Well: V_{PP}

Location: Index 0Dh

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Valid RAM and Time**	**Reserved**						
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Valid RAM and Time.** This bit senses the voltage that feeds the RTC (V_{SB} or V_{BAT}) and indicates if the voltage dropped below the specified minimum value V_{BATMIN}. If the voltage is too low, the RTC contents (time/calendar registers and CMOS RAM) are not valid. Reading this bit enables its updating by the status of the RTC supply voltage. 0: RTC contents not valid 1: RTC contents (time/calendar registers and CMOS RAM) are valid
6-0	**Reserved.**

8.0 Real-Time Clock (RTC) (Continued)

8.3.17 Date-of-Month Alarm Register (DOMA)

Power Well:V_{PP}

Location: Programmable Index through DOMAO register

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Date-of-Month Alarm Data**							
Reset	1	1	0	0	0	0	0	0

Bit	Description
7-0	**Date-of-Month Alarm Data.** Values may be 01 to 31 in BCD format or 01 to 1F in Binary format. When bits 7 and 6 are both set to one (‘11’), unconditional match is selected (default).

8.3.18 Month Alarm Register (MONA)

Power Well: V_{PP}

Location: Programmable Index through MONAO register

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Month Alarm Data**							
Reset	1	1	0	0	0	0	0	0

Bit	Description
7-0	**Month Alarm Data.** Values may be 01 to 12 in BCD format or 01 to 0C in Binary format. When bits 7 and 6 are both set to one (‘11’), unconditional match is selected (default).

8.3.19 Century Register (CEN)

Power Well:V_{PP}

Location: Programmable Index through CENO register

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Century Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Century Data.** Values may be 00 to 99 in BCD format or 00 to 63 in Binary format.

8.0 Real-Time Clock (RTC) (Continued)

8.3.20 BCD and Binary Formats

Parameter	BCD Format	Binary Format
Seconds	00 to 59	00 to 3B
Minutes	00 to 59	00 to 3B
Hours	12-Hour mode: 01 to 12 (AM) 81 to 92 (PM) 24-Hour mode: 00 to 23	12-Hour mode: 01 to 0C (AM) 81 to 8C (PM) 24-Hour mode: 00 to 17
Day	01 to 07 (Sunday = 01)	01 to 07
Date	01 to 31	01 to 1F
Month	01 to 12 (January = 01)	01 to 0C
Year	00 to 99	00 to 63
Century	00 to 99	00 to 63

8.4 USAGE HINTS

1. Read bit 7 of the CRD register at each system power-up to validate the contents of the RTC registers and the CMOS RAM. When this bit is 0, the contents of these registers and the CMOS RAM are questionable. This bit is reset when the backup battery voltage is below the minimum specified battery voltage, V_{BATMIN}. Although the RTC oscillator may function properly and the register contents may be correct at lower voltages than V_{BATMIN}, this bit is reset because correct functionality cannot be guaranteed. System BIOS may use a checksum method to revalidate the contents of the CMOS-RAM. The checksum byte must be stored in the CMOS RAM.
2. To maintain valid time and register information, change the backup battery while normal operating power is on and not while in Backup mode; however, if a low leakage capacitor is connected to V_{BAT}, the battery can also be changed in Backup mode.
3. A rechargeable NiCd battery may be used instead of a non-rechargeable Lithium battery. This is the preferred solution for portable systems, where small size components is essential.
4. A supercap capacitor may be used instead of the normal Lithium battery. In a portable system, the V_{SB} voltage is usually present because the power management stops the system before its voltage falls. The supercap capacitor in the range of 0.047-0.47F will supply the power during the battery replacement.

8.0 Real-Time Clock (RTC) (Continued)

8.5 RTC REGISTER BITMAP

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	SEC	Seconds Data							
01h	SECA	Seconds Alarm Data							
02h	MIN	Minutes Data							
03h	MINA	Minutes Alarm Data							
04h	HOR	Hours Data							
05h	HORA	Hours Alarm Data							
06h	DOW	Day-of-Week Data							
07h	DOM	Date-of-Month Data							
08h	MON	Month Data							
09h	YER	Year Data							
0Ah	CRA	Update in Progress	Divider Chain Control			Periodic Interrupt Rate Select			
0Bh	CRB	SETMODE	PIE	AIE	UIE	Reserved	DATMODE	HRMODE	DSVMODE
0Ch	CRC	IRQF	PIF	AIF	UIF	Reserved			
0Dh	CRD	Valid RAM and Time	Reserved						
Prog.	DOMA	Date-of-Month Alarm Data							
Prog.	MONA	Month Alarm Data							
Prog.	CEN	Century Data							

8.6 RTC GENERAL-PURPOSE RAM MAP

Table 39. Standard RAM Map

Index	Description
0Eh - 7Fh[1]	Battery-backed General-purpose 111-byte RAM.

1. Battery-backed 111-byte RAM (114–3 overlaid registers).

Table 40. Extended RAM Map

Index	Description
00h - 7Fh	Battery-backed General-purpose 128-byte RAM.

9.0 System Wake-Up Control (SWC)

9.1 OVERVIEW

The System Wake-Up Control supports the *ACPI Specification, Revision 1.0b, Feb. 2, 1999.*

The SWC functional block receives external events from the system and internal events from the functional blocks of the PC8741x device. Using these events together with the ACPI sleep state information supplied by the software or by external signals, the SWC generates system interrupts (IRQ, $\overline{\text{SIOSMI}}$) and Power Management signals ($\overline{\text{SIOSCI}}$, $\overline{\text{ONCTL}}$, $\overline{\text{PWBTOUT}}$). In addition, it controls two LED indicators and contains two Power Active timers and a watchdog timer.

The SWC receives the following external events:

- Sixteen V_{SB}-powered General-Purpose Input/Output events (GPIOE10-17 and GPIOE40-47).
- Two Modem Ring events ($\overline{\text{RI1}}$ and $\overline{\text{RI2}}$).
- Mouse movement and button pressing events (via MCLK and MDAT).
- Advanced key pressing events from the Keyboard (via KBCLK and KBDAT).
- Power and Sleep buttons pressing events ($\overline{\text{PWBTIN}}$ and $\overline{\text{SLBTIN}}$).

The SWC receives the following internal events:

- RTC alarm event.
- Keyboard and Mouse interrupt event (IRQ).
- Module interrupt (IRQ) event from the Legacy functional blocks (FDC, Parallel Port and Serial Ports 1 and 2) and from the XIRQ pin (mapped to IRQ).
- Watchdog time-out event.
- Software V_{DD} On and V_{DD} Off requests.

The SWC receives sleep state information either by software (writing the ACPI, SLP_TYPx and SLP_EN bits) or via the $\overline{\text{SLPS3}}$ and $\overline{\text{SLPS5}}$ pins from an external ACPI controller. In Legacy Power Button mode, the Power button can generate an S5 sleep state.

The SWC implements three ACPI fixed register groups: PM1 Event Group (block b), PM1 Control Group (block b) and General-Purpose Event 1 Group. The unimplemented functions in the first two groups (block b) are supported by returning zero.

The SWC generates the system interrupts, IRQ (via SERIRQ) and SMI (via $\overline{\text{SIOSMI}}$), based on the external and internal events (except GPIOE events) and on the routing information written into its registers. GPIOE events, the exception, are routed to the IRQ and SMI by the GPIO functional block. The IRQ and SMI interrupts are independent of the sleep state.

The SWC generates the Power Management signals (the ACPI interrupt—$\overline{\text{SIOSCI}}$, the $\overline{\text{ONCTL}}$ signal for the V_{DD} power supply control and the $\overline{\text{PWBTOUT}}$ signal, which is used by an external ACPI controller) based on the same external and internal events, on routing information and on the current sleep state. The $\overline{\text{ONCTL}}$ and $\overline{\text{PWBTOUT}}$ signals are enabled according to the current sleep state, based on information written into the SWC registers. In Legacy Power Button mode, $\overline{\text{ONCTL}}$ is controlled by the Power button external event. The ACPI-compatible SCI interrupt is independent of the current sleep state.

Two functions bypass event routing by the sleep state mechanism and directly affect the $\overline{\text{ONCTL}}$ and $\overline{\text{PWBTOUT}}$ signals. These are:

- Power Button Override, which forces the V_{DD} power supply off if the Power button is continuously pressed for more than four seconds.
- Crowbar, which releases the V_{DD} Power On request if the V_{DD} power supply refuses to turn on.

In addition, the SWC controls two LED indicators. Control is based on the current sleep state information or on the status of the V_{SB} and V_{DD} power. The SWC also includes two Power Active timers that measure the time the V_{SB} and V_{DD} power supplies are active (On).

Another function included in the SWC is the watchdog timer. If the watchdog is not retriggered by one of its event sources and reaches time-out, it generates an SMI (via $\overline{\text{SIOSMI}}$) or an SCI (via $\overline{\text{SIOSCI}}$) interrupt. In addition, the watchdog generates a pulse at the $\overline{\text{WDO}}$ pin.

The SWC contains two Power Management registers that allow the software to disable each Legacy module and to TRI-STATE its outputs in a centralized manner.

The SWC module is powered by the V_{PP} plane (see Section 2.1 on page 32). However, during Power Fail state (i.e., when only V_{BAT} is present), the module functions (event detection, output generation and time counting) are disabled and only the V_{PP}-powered registers retain their data.

Figure 47 shows the simplified block diagram of the SWC functional block.

9.0 System Wake-Up Control (SWC) (Continued)

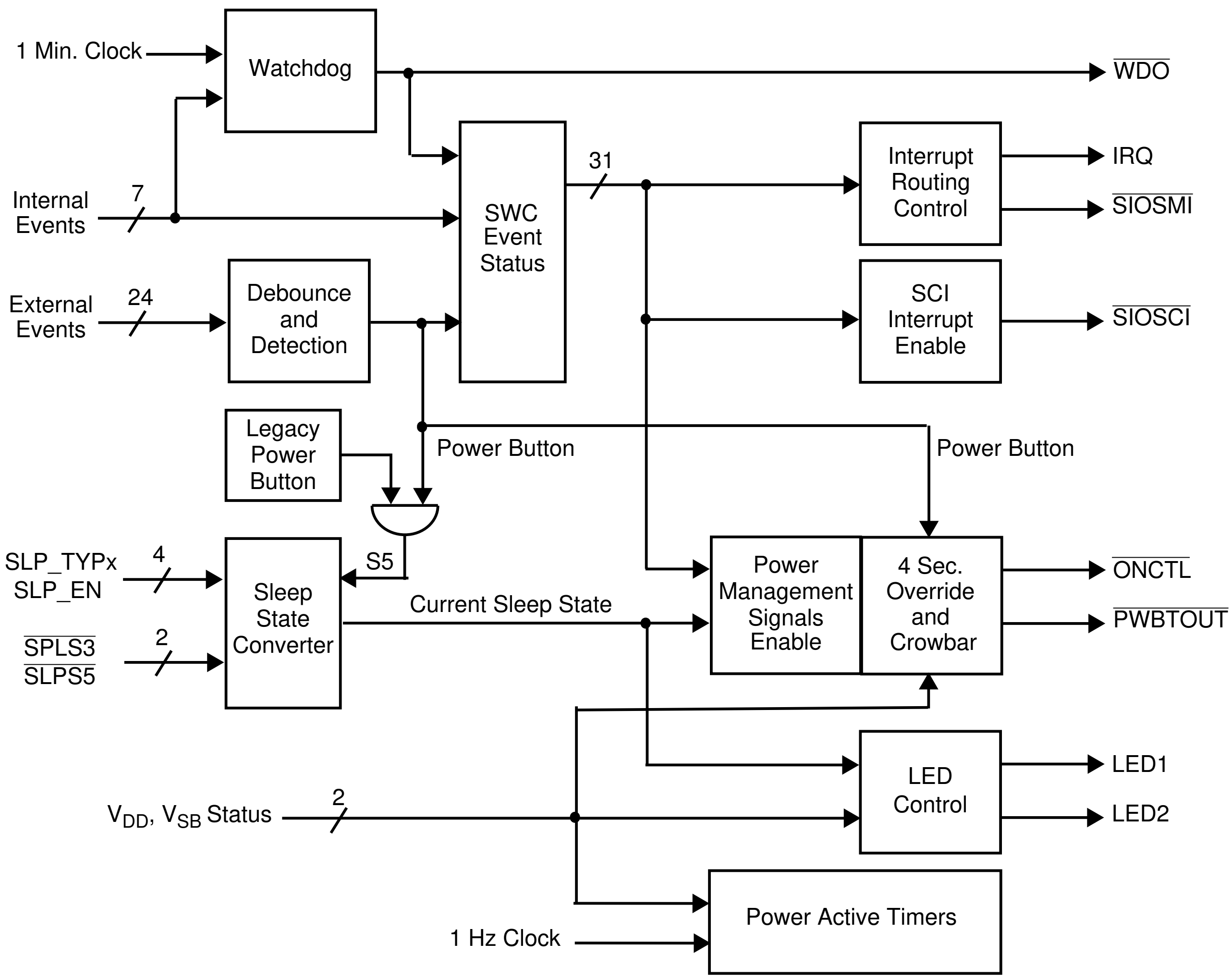


Figure 47. SWC Block Diagram

9.2 FUNCTIONAL DESCRIPTION

9.2.1 External Events

General-Purpose Input/Output Events

The PC8741x devices support 16 V_{SB}-powered General-Purpose Input/Output events through ports GPIOE10-17 and GPIOE40-47. V_{DD}- and V_{SB}-powered signals can be connected to the GPIO pins to become sources of external events. A V_{DD}-powered signal used to generate an event is internally disabled (for event generation) while V_{DD} power is off and also for 1 second after V_{DD} power is restored. This prevents the detection of false events during power transitions and while the signal driver is unpowered. For the same reasons, a V_{SB}-powered signal used to generate an event is enabled only 1 second after the V_{SB} power is on. (When V_{SB} is off, the whole SWC module is disabled.)

Each GPIOE pin has programmable polarity and an optional 16 ms debouncer (see Figure 48). The debouncer is enabled after the reset but can be disabled by software.

A GPIO event can generate the system interrupts (IRQ and SMI) if the event is enabled and routed to the specific interrupt. The status, event enable and pending event routing bits to IRQ and SMI are implemented in the GPIO Ports module (see Section 7.3 on page 137). The status bit is set when an event of the programmed type (edge or level) is detected.

A GPIO event can also generate the Power Management signals (the SCI interrupt, the $\overline{ONCTL}$ power supply control and the $\overline{PWBTOUT}$ signal). The status, event enable and wake-up state enable bits are implemented in the SWC module (see Figures 48 and 50).

9.0 System Wake-Up Control (SWC) (Continued)

An active level-type event sets the status bit in registers GPE1_STS_0 for ports GPIOE10-17 and GPE1_STS_1 for ports GPIOE40-47 (see Sections 9.4.8 and 9.4.9 on pages 209ff.). The status bit remains set even when the event becomes inactive. The status bit is cleared only when the software writes ‘1’ to the bit. If the event is still active when software writes ‘1’, the status bit remains set.

After changing the GPIOExx pin multiplexing, clear the relevant bits in the GPE1_STS_0 and GPE1_STS_1 registers, to prevent false events (caused by the pin multiplexing switch) from generating a wake-up event.

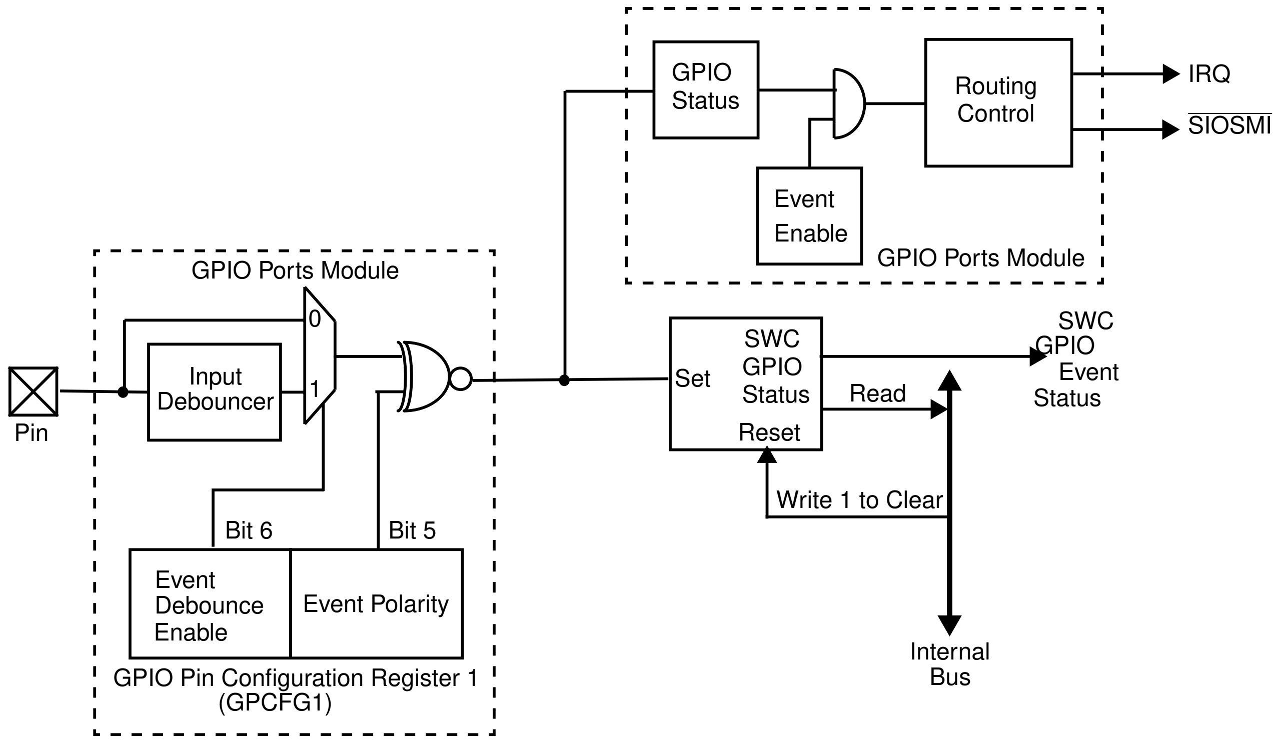


Figure 48. GPIO Events

Modem Ring Events

High-to-low transitions on $\overline{RI1}$ or $\overline{RI2}$ indicate the detection of a ring signal by an external modem connected to Serial Port 1 or Serial Port 2, respectively. The transitions on $\overline{RI1}$ and $\overline{RI2}$ are detected by the RI Wake-up Detector powered by V_{SB}, which works independently of the Serial Port 1 or Serial Port 2 modules (powered by V_{DD}).

A detected $\overline{RI1}$ or $\overline{RI2}$ transition sets the RI1_EVT_STS or RI2_EVT_STS status bits in the GPE1_STS_2 register (see Section 9.4.10 on page 210). A status bit is cleared only when the software writes ‘1’ to it.

The transition detection from $\overline{RI1}$ and $\overline{RI2}$ is enabled (for event generation) 1 second after the V_{SB} power is on. This prevents the detection of false events during V_{SB} power-On transitions.

Mouse Wake-Up Event

The mouse wake-up event is detected by the Keyboard/Mouse Wake-up Detector, which monitors the MCLK and MDAT signals. Since the detection mechanisms for keyboard and mouse events are independent, they can be operated simultaneously. Moreover, the Keyboard signals may be swapped with the Mouse signals by setting the SWAP_KBMS bit in the SWC_CTL register (see Section 9.3.10 on page 187). This bit must be set to the same value as the Swap bit in the KBC Configuration register (see Section 3.13.3 on page 69). The Keyboard/Mouse Wake-up Detector is powered by V_{SB} and works independently of the Keyboard Controller module (powered by V_{DD}).

The mouse event detection mechanism can be programmed to detect either a mouse click or movement, a specific mouse click (left or right) or a double-click. To program which mouse action causes an event detection, set the MSEVCFG field in the PS2CTL register (see Section 9.3.17 on page 194) to the required value.

A detected mouse event sets the MS_EVT_STS status bit in the GPE1_STS_2 register (see Section 9.4.10 on page 210). The status bit is cleared only when the software writes ‘1’ to it.

9.0 System Wake-Up Control (SWC) (Continued)

The mouse event detection from MCLK and MDAT is enabled (for event generation) 1 second after the V_{SB} power is on. This prevents the detection of false events during Mouse V_{SB} power-On transitions. In addition, if the Keyboard/Mouse Power Control feature (see Section 9.2.10 on page 175) is enabled by setting the VDDFLMUX bit to ‘1’ (in the SIOCF2 register; see Section 3.7.3 on page 50), mouse event detection is disabled for 2 seconds from the moment the V_{DD} power is turned off. If this feature is disabled (VDDFLMUX = ‘0’ in SIOCF2) mouse event detection is enabled regardless of the V_{DD} power status; however, the wake-up becomes effective (V_{DD} power is turned on) only 1 second after the V_{DD} power was turned off.

Keyboard Wake-Up Events

Keyboard wake-up events are also detected by the Keyboard/Mouse Wake-up Detector, which monitors the KBCLK and KBDAT signals. Since the detection mechanisms for keyboard and mouse events are independent, they can be operated simultaneously. Moreover, the Keyboard signals may be swapped with the Mouse signals, as explained in the *Mouse Wake-Up Event* section (page 163). The Keyboard/Mouse Wake-up Detector is powered by V_{SB} and works independently of the Keyboard Controller module (powered by V_{DD}).

The keyboard event detection mechanism can be programmed to detect:

- Any keystroke (Special Key Sequence mode).
- A specific programmable sequence of up to eight alphanumeric keystrokes (Password mode).
- Any programmable sequence of up to eight bytes of data received from the keyboard (Special Key Sequence mode).
- Up to three programmable, Power Management keys concurrently available, each including a sequence of up to three bytes of data received from the keyboard (Power Management Key mode).

The Keyboard/Mouse Wake-up Detector has three operation modes:

- Password mode.
- Special Key Sequence mode.
- Power Management Key mode.

Up to eight Keyboard Data registers (PS2KEY0 to PS2KEY7) are used to define which keyboard data string generates an event. Since the same set of registers is used by each operation mode, only one mode can be selected at a time.

In the modes involving more than one keystroke, the maximum delay allowed between pressing two consecutive keys is 4 seconds. A longer delay is interpreted by the Wake-up Detector as the beginning of a new sequence of keystrokes, which causes the present sequence to be discarded. In all operation modes, pressing a wrong key requires a recovery time of 4 seconds, before a new (correct) sequence may be recognized.

Password Mode. In Password mode, the Make and Break bytes transmitted by the keyboard are discarded, and only the keystroke data bytes are compared with those programmed in the PS2KEY0 to PS2KEY7 registers. If the two sets are equal, a keyboard event that sets the KBD_EVT1_STS bit in the GPE1_STS_2 register is detected (see Section 9.4.10 on page 210). The status bit is cleared only when the software writes ‘1’ to it. To simplify the detection mechanism, only keys with a keystroke data of one byte can be included in the sequence to be detected. To program the Keyboard/Mouse Wake-up Detector to operate in Password mode, proceed as follows:

1. Set KBDMODE bit in the KBDWKCTL register to ‘0’ (see Section 9.3.16 on page 193).
2. Set KBEVCFG field in the PS2CTL register to a value that indicates the desired number of alphanumeric keystrokes in the sequence. The programmed value = the number of keystrokes + 7. For example, to detect a sequence of two keys, set KBEVCFG to 9h.
3. Program the appropriate subset of the PS2KEY0-PS2KEY7 registers in sequential order with the data bytes of the keys in the sequence. For example, if there are three keys in the sequence and the keystroke data of these keys are 05h (first), 50h (second) and 44h (third), program PS2KEY0 to 05h, PS2KEY1 to 50h and PS2KEY2 to 44h (the scan codes are only examples).

Special Key Sequence Mode. In Special Key Sequence mode, all the bytes transmitted by the keyboard are compared with those programmed in the PS2KEY0 to PS2KEY7 registers. These include also the Make and Break bytes. If the two sets are equal, a keyboard event is detected, as explained in *Password Mode*, above. This mode enables the detection of any sequence of keystrokes, including keys as “Shift” and “Alt”. To program the Keyboard/Mouse Wake-up Detector to operate in Special Key Sequence mode, proceed as follows:

1. Set KBDMODE bit in the KBDWKCTL register to ‘0’ (see Section 9.3.16 on page 193).
2. Set KBEVCFG field in the PS2CTL register to a value that indicates the desired number of keystrokes in the sequence. The programmed value = the number of keystrokes + 1. For example, to detect a sequence of three received bytes (i.e., one keystroke), set KBEVCFG to 2h.
3. Program the appropriate subset of the PS2KEY0-PS2KEY7 registers in sequential order with the data bytes that comprise the sequence. For example, if the number of bytes in the sequence is four, and the values of these bytes are E0h (first), 5Bh (second), E0h (third) and DBh (fourth), program PS2KEY0 to E0h, PS2KEY1 to 5Bh, PS2KEY2 to E0h and PS2KEY3 to DBh (the byte values are only examples).

9.0 System Wake-Up Control (SWC) (Continued)

Special Key Sequence mode also enables detection of a specific single keystroke. To program the Keyboard/Mouse Wake-up Detector to wake-up on a single keystroke, perform the following sequence:

1. Set KBDMODE bit in the KBDWKCTL register to '0' (see Section 9.3.16 on page 193).
2. Set KBEVCFG field in the PS2CTL register to 0001b.
3. Program the PS2KEY0 and PS2KEY1 registers to 00h. This forces the detector to ignore the values of incoming data, thus causing it to detect a keyboard event on the single keystroke.

Power Management Mode. In Power Management Key mode, the PS2KEY0 to PS2KEY7 register bank is divided into three groups of registers: PS2KEY0 to PS2KEY2, PS2KEY3 to PS2KEY5 and PS2KEY6 to PS2KEY7. Each group can be programmed with different data bytes, allowing the bytes transmitted by the keyboard to be compared simultaneously with three keystroke sequences. If the bytes transmitted by the keyboard (including Make and Break) are equal to the data bytes in one register group, the related keyboard event is detected. The detection of Keyboard Event 1 (data in PS2KEY0-PS2KEY2) sets the KBD_EVT1_STS bit, the detection of Keyboard Event 2 (data in PS2KEY3-PS2KEY5) sets the KBD_EVT2_STS bit and the detection of Keyboard Event 3 (data in PS2KEY6-PS2KEY7) sets the KBD_EVT3_STS bit. All three status bits are in the GPE1_STS_2 register (see Section 9.4.10 on page 210). Each status bit is cleared only when the software writes '1' to the bit. This mode enables the detection of any sequence of keys.

Note: Do not use a byte sequence that is a "subset" of the byte sequence of another ("superset") Power Management key event. The subset sequence has fewer bytes (set by the EVTxCFG fields in the KBDWKCTL register) than the superset sequence; the bytes contained in the subset sequence (as programed in the PS2KEY0 to PS2KEY7 registers) are identical to the respective bytes of the superset sequence.

To program the Keyboard/Mouse Wake-up Detector to operate in Power Management Key mode, proceed as follows:

1. Set KBDMODE bit in the KBDWKCTL register to '1' (see Section 9.3.16 on page 193).
2. Set each event configuration field (EVT1CFG, EVT2CFG and EVT3CFG) in the KBDWKCTL register to a value that indicates the desired number of keystroke data bytes in the sequence, for each event. For example, to detect a sequence of two received bytes, set EVTxCFG to 2h.
3. Program each group of the PS2KEY0-PS2KEY7 registers in sequential order with the data bytes of the keys in the sequence for each event.

Event Generation. Keyboard event detection from KBCLK and KBDAT is enabled (for event generation) 1 second after the V_{SB} power is on. This prevents the detection of false events during Keyboard V_{SB} power-On transitions. In addition, if the Keyboard/Mouse Power Control feature (see Section 9.2.10 on page 175) is enabled by setting the VDDFLMUX bit to '1' (in the SIOCF2 register; see Section 3.7.3 on page 50), keyboard event detection is disabled for 2 seconds from the moment the V_{DD} power is turned off. If this feature is disabled (VDDFLMUX = '0' in SIOCF2) keyboard event detection is enabled regardless of the V_{DD} power status; however, the wake-up becomes effective (V_{DD} power is turned on) only 1 second after the V_{DD} power was turned off.

Power Button Event

A low level signal at $\overline{\text{PWBTIN}}$ indicates that the Power button was pressed. This input, filtered by a 16 ms debouncer, is bridged to the $\overline{\text{PWBTOUT}}$ output to synchronize an external ACPI controller (which is optional).

A detected low level signal sets the PWRBTN_STS status bit in the PM1b_STS_HIGH register (see Section 9.4.3 on page 205) and the PWBT_EVT_STS status bit in the GPE1_STS_2 register (see Section 9.4.10 on page 210). Note, however, that the PWRBTN_STS status bit is not set if the PWRBTN_EV_DIS bit in the ACPI_CFG register is reset (see Section 9.3.32 on page 201). This functionality is required for ACPI compatibility in case the Power button event is implemented in an (optional) external ACPI controller. Both status bits are cleared when the software writes '1' to any of them. If a low level is present at the input when software writes '1' to the status bit, the status bit remains set. The low level detection from $\overline{\text{PWBTIN}}$ is enabled (for event generation) 1 second after the V_{SB} power is on. This prevents the detection of false events during V_{SB} power-On transitions.

The Power button event is always enabled for wake-up in any sleep state. In addition, the Power button event is the only wake-up event available after a Power Button Override or a Crowbar condition (see Section 9.2.6 on page 172).

In Legacy Power Button mode (LEGACY_PWBT = 1 in the PWONCTL register; see Section 9.3.11 on page 188), a low-level signal at $\overline{\text{PWBTIN}}$, when the V_{DD} power is on, generates an S45 current sleep state (see Section 9.2.3 on page 167), which sets $\overline{\text{ONCTL}}$ to Off. In addition, the PWRBTN_STS and the PWBT_EVT_STS status bits are reset in this situation. In this mode, the Power button event is the only wake-up event available after $\overline{\text{ONCTL}}$ is turned off.

Sleep Button Event

A low level on $\overline{\text{SLBTIN}}$ indicates the Sleep button was pressed. This input is also filtered by a 16 ms debouncer.

A detected low level sets the SLPBTN_STS status bit in the PM1b_STS_HIGH register (see Section 9.4.3 on page 205) and the SLBT_EVT_STS status bit in the GPE1_STS_2 register (see Section 9.4.10 on page 210). Note, however, that the SLPBTN_STS status bit is not set if the SLPBTN_EV_DIS bit in the ACPI_CFG register is reset (see Section 9.3.32 on

9.0 System Wake-Up Control (SWC) (Continued)

page 201). This functionality is required for ACPI compatibility in case the Sleep Button event is implemented in an (optional) external ACPI controller. Both status bits are cleared when the software writes ‘1’ to either of them. If a low level is present at the input when software writes ‘1’ to the status bit, the status bit remains set.

The low level detection from $\overline{\text{SLBTIN}}$ is enabled (for event generation) 1 second after the V_{SB} power is on. This prevents the detection of false events during V_{SB} power-On transitions.

9.2.2 Internal Events

RTC Alarm Event

An RTC Alarm event is generated by the RTC functional block. An asserted RTC Alarm sets the RTC_STS status bit in the PM1b_STS_HIGH register (see Section 9.4.3 on page 205) and the RTC_EVT_STS status bit in the GPE1_STS_3 register (see Section 9.4.11 on page 211). Note, however, that the RTC_STS status bit is not set if the RTC_EV_DIS bit in the ACPI_CFG register (see Section 9.3.32 on page 201) is reset. This functionality is required for ACPI compatibility in case the RTC Alarm event is implemented in an (optional) external ACPI controller. Both status bits are cleared when the software writes ‘1’ to any of them. If the RTC Alarm is asserted when software writes ‘1’ to the status bit, the status bit remains set.

KBC P12 Event

A KBC P12 event is detected when the P12 port of the Keyboard Controller (KBC) functional block is set to ‘1’. For this to happen, the KBC module must be enabled (see Section 3.3.1 on page 43). Since the Keyboard Controller functional block is powered by V_{DD}, a P12 event can occur only when V_{DD} is present.

A high level at the P12 port of the KBC sets the P12_EVT_STS status bit in the GPE1_STS_3 register (see Section 9.4.11 on page 211). The status bit is cleared only when the software writes ‘1’ to it. If the P12 port is at high level when software writes ‘1’ to the status bit, the status bit remains set.

Keyboard and Mouse IRQ Events

Keyboard and Mouse IRQ events are detected when either the Keyboard IRQ or Mouse IRQ is asserted.

To enable the IRQ of a logical device to generate an IRQ event, the associated Enable bit (bit 4 of the configuration register at index 70h; see Section 3.2.3 on page 40) must be set to ‘1’. Since the Keyboard Controller (KBC) functional block is powered by V_{DD}, a Keyboard or Mouse IRQ event can occur only when V_{DD} is present.

An active (level-type) Keyboard IRQ event sets the KBD_IRQ_STS status bit and an active Mouse IRQ event sets the MS_IRQ_STS status bit. Both status bits are in the GPE1_STS_3 register (see Section 9.4.11 on page 211). A status bit is cleared only when the software writes ‘1’ to it. If the IRQ event is active when software writes ‘1’ to the status bit, the status bit remains set.

The ROM code used for the Keyboard Controller generates active high Keyboard and Mouse interrupts, used by the SWC module.

Module IRQ Event

A Module IRQ event is detected when one of the Legacy modules (FDC, Parallel Port, Serial Port 1 or 2) asserts its IRQ or when an active level is detected at the XIRQ pin (**PC87416 and PC87417**).

To enable the IRQ of a logical device to generate an IRQ event, the associated Enable bit (bit 4 of the configuration register at index 70h; see Section 3.2.3 on page 40) must be set to ‘1’. Since the Legacy modules are powered by V_{DD}, they can assert IRQ only when V_{DD} is present.

To enable an active level at the XIRQ pin (**PC87416 and PC87417)** to generate an event, both the IRQEN and the PWUREN bits in the XIRQC register (see Section 5.4.4 on page 110) must be set to ‘1’. Since the XIRQ interrupt belongs to the X-Bus Extension functional block powered by V_{SB}, an active level at the XIRQ pin can also generate a Module IRQ event when V_{DD} is off. The XIRQ detection enabled (for event generation) 1 second after the V_{SB} power is on. This prevents the detection of false events during V_{SB} power-On transitions.

The MOD_IRQ_STS status bit in the GPE1_STS_3 register is set by an IRQ that is asserted by one of the Legacy modules or by an active level at the XIRQ pin (see Section 9.4.11 on page 211). The status bit is cleared only when the software writes ‘1’ to it. If the Module IRQ event is active when software writes ‘1’ to the status bit, the status bit remains set.

Watchdog Time-Out Event

A watchdog time-out event is generated by the watchdog function in the SWC module (see Section 9.2.9 on page 174). An asserted watchdog event sets the WDO_EVT_STS status bit in the GPE1_STS_3 register (see Section 9.4.11 on page 211). A status bit is cleared only when the software writes ‘1’ to it. If the watchdog event is asserted when software writes ‘1’ to the status bit, the status bit remains set.

9.0 System Wake-Up Control (SWC) (Continued)

Software Power On/Off Events

A Software Power event is triggered when software writes ‘1’ to the SW_ON_CTL bit (for Power On) or to the SW_OFF_CTL bit (for Power Off). After being written ‘1’, these bits automatically return to their default value of ‘0’. Both bits are located in the SWC_CTL register (see Section 9.3.10 on page 187). If the V_{DD} power is not preset, these two bits can be written ‘1’ through the ACCESS.bus (**PC87413 and PC87417**), which is powered by V_{SB}.

A Software Power On event sets the SW_ON_STS status bit and a Software Power Off event sets the SW_OFF_STS status bit. Both bits are in the GPE1_STS_3 register (see Section 9.4.11 on page 211). A status bit is cleared only when the software writes ‘1’ to it.

9.2.3 Sleep States

Compliance with *ACPI Specification, Revision 1.0b, Feb. 2, 1999* requires the PC8741x devices to recognize the six system states: Working (G0/S0), Sleeping (G1-S1 to G1-S4) and Soft-off (G2/S5). The system state is written by the host into the SLP_TYPx field of the PM1b_CNT_HIGH register (see Section 9.4.7 on page 208) and updated by writing a ‘1’ to the SLP_EN bit in the same register.

The value written in the SLP_TYPx field is translated to one of the internal states (S0 to S5), using the data programmed in the Sleep Type Encoding registers. This translation mechanism allows the software to use any SLP_TYPx encoding scheme. Each of the six Sleep Type Encoding registers (S0_SLP_TYP to S5_SLP_TYP; see Section 9.3.30 on page 199) contains a 3-bit SLP_ENC_TYP field. The software must program this field with the SLP_TYPx code used for the internal state represented by the register. The software must program all six registers even if not all the system states are supported.

The SWC uses three current sleep states to control its operation. The six decoded internal states are converted to the current sleep states as follows (see Section 9.2.5 for the usage of the current sleep states):

- S0, S1 and S2 are converted to the S12 current state; this is the active state for the PC8741x device, with V_{DD} and V_{SB} power supplies being On.
- S3 is converted to the S3I current state; in this sleep state, the V_{SB} power is On but the V_{DD} power supply can be On or Off, according to the setting of the S3I_VDD_ON bit in the SLP_ST_CFG register (see Section 9.3.31 on page 200).
- S4 is converted to either S3I or S45 current states, according to the setting of the S4_SELECT bit in the SLP_ST_CFG register (see Section 9.3.31 on page 200).
- S5 is converted to the S45 current state; in this sleep state, the V_{SB} power is On but the V_{DD} power supply is Off.

If an active (optional) ACPI controller is located in an external device, the $\overline{\text{SLPS3}}$ and $\overline{\text{SLPS5}}$ signals are used to determine the system sleep state. This option is selected by setting both the EXTSTMUX bit in the SIOCF3 register (see Section 3.7.4 on page 51) and the EXT_ST_SELECT bit in the SLP_ST_CFG register (see Section 9.3.31 on page 200) to ‘1’. Table 41 shows how the levels of the $\overline{\text{SLPS3}}$ and $\overline{\text{SLPS5}}$ signals are converted to current sleep states.

Table 41. $\overline{\text{SLPS3}}$, $\overline{\text{SLPS5}}$ Conversion to Current Sleep States

$\overline{\text{SLPS3}}$	$\overline{\text{SLPS5}}$	Current Sleep State
1	1	S12
0	1	S3I
0	0	S45
1	0	Reserved

Note: The internal and external sleep state modes are mutually exclusive. The internal sleep state register (PM1b_CNT_HIGH) should not be used when External Sleep State mode is selected. Similarly, pins $\overline{\text{SLPS3}}$ and $\overline{\text{SLPS5}}$ should not be used when Internal Sleep State mode is selected.

The use of the external $\overline{\text{SLPS3}}$ and $\overline{\text{SLPS5}}$ signals to determine the current sleep state is enabled 1 second after the V_{SB} power is on. This prevents the selection of an erroneous current sleep state during V_{SB} power-On transitions.

In Legacy Power Button mode, when the V_{DD} power is on, an S45 current state is generated by a low-level signal at $\overline{\text{PWBTIN}}$.

9.0 System Wake-Up Control (SWC) (Continued)

9.2.4 Interrupt Signals

The SWC generates three system interrupts: IRQ (via SERIRQ), SMI (via $\overline{\text{SIOSMI}}$) and SCI (via $\overline{\text{SIOSCI}}$). The IRQ and SMI interrupts are not related to the ACPI-compatible system control but are based on the external and internal events, each with its status and enable bit in the SWC module. However, the status and enable bits for the GPIOE events (GPIOE10-17 and GPIOE40-47) related to IRQ and SMI generation are located in the GPIO functional block (see Section 7.3 on page 137). SCI is the Power Management interrupt defined by ACPI. Its status and enable bits are all located in the SWC module.

IRQ Interrupt

The external and internal events processed by the SWC for IRQ generation set a status bit in the GPE1_STS_2 and GPE1_STS_3 registers. Only those events that are allowed to be routed to the IRQ interrupt by the SWC have an associated enable bit in the GPE1_2IRQ_LOW and GPE1_2IRQ_HIGH registers (see Sections 9.3.4 and 9.3.5 on pages181ff.). When an enable bit is set, and if the corresponding status bit is set, an active IRQ is generated. The IRQ interrupt is independent of the system sleep state.

SMI Interrupt

The external and internal events processed by the SWC for SMI generation set a status bit in the GPE1_STS_2 and GPE1_STS_3 registers. Only those events that are allowed to be routed to the SMI interrupt by the SWC have an associated enable bit in the GPE1_2SMI_LOW and GPE1_2SMI_HIGH registers (see Sections 9.3.6 and 9.3.7 on pages 183ff.). When an enable bit is set, and if the corresponding status bit is set, an active SMI is generated. The SMI interrupt is independent of the system sleep state.

SCI Interrupt

All external and internal events (including GPIOE) are exclusively processed by the SWC to generate the Power Management interrupt, SCI. Each active event sets a status bit in the GPE1_STS_0 to GPE1_STS_3 registers. Three events, the Power button event, the Sleep button event and the RTC event each have an additional status bit in the PM1b_STS_HIGH register (PWRBTN_STS, SLPBTN_STS and RTC_STS bits, respectively). Each of the additional status bits is set only if the PC8741x device is assigned the specific function by the ACPI software (see Sections 9.2.1 and 9.2.2 on pages 162ff.).

For each status bit, the SWC holds an enable bit in the GPE1_EN_0 to GPE1_EN_3 registers (see Sections 9.4.12 to 9.4.15 on pages 213ff.). A set status bit can cause the assertion of the SCI interrupt only when an enable bit is set. Each of the three events mentioned in the previous paragraph also has additional enable bits in the PM1b_EN_HIGH register (see Section 9.4.5 on page 207). Each additional enable and status bit is reset if the respective bit (PWRBTN_EV_DIS, SLPBTN_EV_DIS or RTC_EV_DIS) in the ACPI_CFG register is reset (see Section 9.3.32 on page 201). This "dual control" behavior is required for ACPI compatibility in case one of these events is implemented in an (optional) external ACPI controller. An SCI from one of these dual control functions is generated if at least one enabled status bit (of the pair) is set.

The SCI interrupt is independent of the system sleep state with one exception, the Power button event. When the system is in a sleep state (S1-S5), a set PWRBTN_STS bit generates an active SCI regardless of the value of the PWRBTN_EN bit. S0 can be separated from the sleep states (S1-S5) only when the PC8741x device serves as an ACPI controller and the software writes the system state (SLP_TYPx) in the PM1b_CNT_HIGH register. The bypass of the PWRBTN_EN bit during sleep states (i.e., a set PWRBTN_STS bit generates SCI regardless of the PWRBTN_EN bit) is therefore available only if the EXT_ST_SELECT bit in the SLP_ST_CFG register is reset (see Section 9.3.31 on page 200).

When the SCI interrupt is asserted and the system is in a sleep state (S1-S5), the WAK_STS bit of the PM1b_STS_HIGH register is set. This feature, too, is available only if the EXT_ST_SELECT bit in the SLP_ST_CFG register is reset (the ACPI controller is implemented by the PC8741x device).

Figure 49 shows the SCI generation by the dual control functions and the behavior of the Power button event as a function of the sleep state.

9.0 System Wake-Up Control (SWC) (Continued)

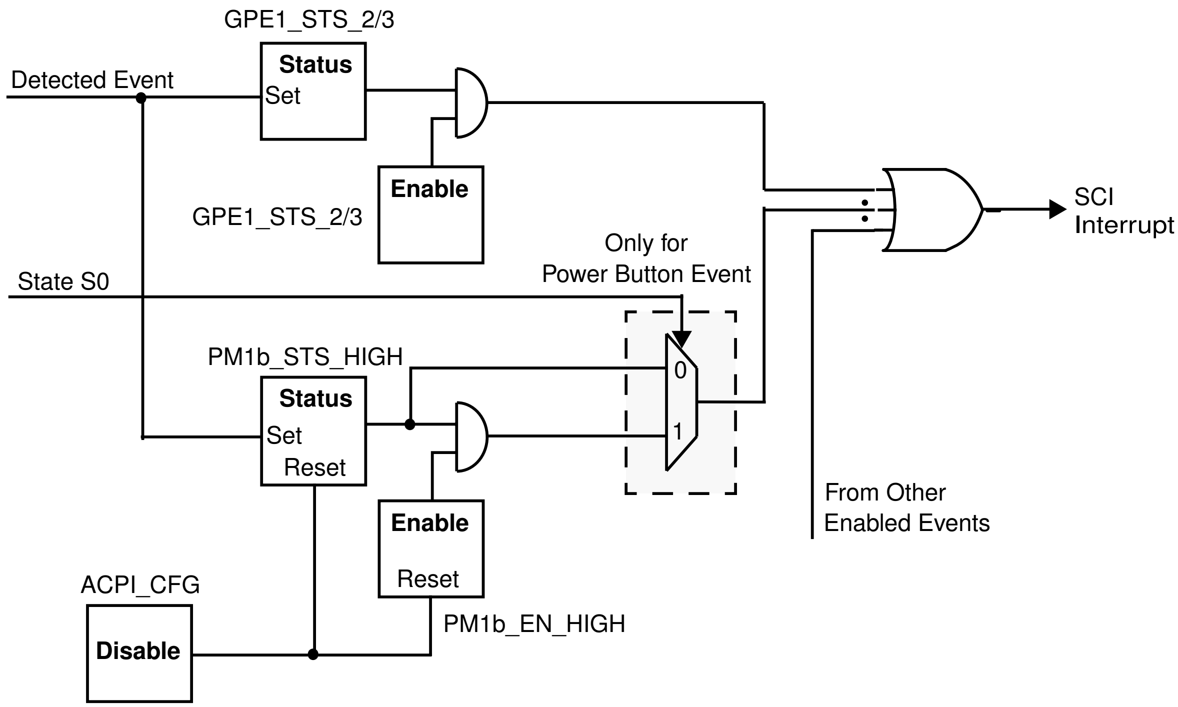


Figure 49. Dual Control Functions

9.2.5 Power Management Signals

The SWC generates two Power Management signals: $\overline{\text{ONCTL}}$, for the V_{DD} power supply control, and $\overline{\text{PWBTOUT}}$, which is used by an external ACPI controller. These signals are based on the external and internal events, each with its status and enable bits in the SWC module (including GPIOE). $\overline{\text{ONCTL}}$ and the $\overline{\text{PWBTOUT}}$ are generated according to the current sleep state.

Special Power Management functions, either required by the ACPI Specification or inherited from the Legacy Power Management, also affect the $\overline{\text{ONCTL}}$ and $\overline{\text{PWBTOUT}}$ outputs. These functions are described in Section 9.2.6.

Power Supply Control ($\overline{\text{ONCTL}}$)

Each active external or internal event (including GPIOE) sets a status bit in the GPE1_STS_0 to GPE1_STS_3 registers. Three events (Power button, Sleep button and RTC alarm) each have an additional status bit in the PM1b_STS_HIGH register. Their behavior is described in the *SCI Interrupt* section (page 168).

$\overline{\text{ONCTL}}$ generation is independent of the enable bits in the GPE1_EN_0 to GPE1_EN_3 registers. It is also independent of the three additional enable bits in the PM1b_EN_HIGH register (for Power button, Sleep button and RTC alarm events). $\overline{\text{ONCTL}}$ is not affected by the Watchdog Status bit (WDO_EVT_STS).

$\overline{\text{ONCTL}}$ is turned off (inactive: $\overline{\text{ONCTL}}$ = high level) according to the current sleep states, S3I and S45 (S12 is the active state for the PC8741x device and does not influence $\overline{\text{ONCTL}}$; see Section 9.2.3 on page 167). These current sleep states are decoded from the value of the SLP_TYPx field of the PM1b_CNT_HIGH register (for EXT_ST_SELECT = 0 in the SLP_ST_CFG register) or from the levels of the $\overline{\text{SLPS3}}$ and $\overline{\text{SLPS5}}$ signals (for EXT_ST_SELECT = 1 in the SLP_ST_CFG register and EXTSTMUX = 1 in the SIOCF3 register). In Legacy Power button mode, when the V_{DD} power is on, an S45 current state is generated by a low-level signal at $\overline{\text{PWBTIN}}$, overriding the decoded sleep states.

When the PC8741x device enters the S45 state, it turns the V_{DD} power supply Off by setting $\overline{\text{ONCTL}}$ = 1. The state of the V_{DD} power supply (On or Off) in S3I state depends on the setting of the S3I_VDD_ON bit in the SLP_ST_CFG register (see Section 9.3.31 on page 200).

If the PC8741x device is the ACPI controller of the system (EXT_ST_SELECT = 0 in the SLP_ST_CFG register), $\overline{\text{ONCTL}}$ is turned On by an active wake-up event. This is possible only if the event is enabled for wake-up (in the WK_ST_EN register) in the current sleep state.

Each external or internal event has its own Wake-Up State Enable register (WK_ST_EN), which is accessed by the software writing its index value (see Table 48 on page 179) into the WKUPSEL field of the Wake-Up Event Select register (WK_EVT_SEL; see Section 9.3.2). The currently accessed WK_ST_EN register selects the current sleep states for which

9.0 System Wake-Up Control (SWC) (Continued)

the related event generates a wake-up (i.e., it turns the V_{DD} power supply On by setting $\overline{ONCTL}$ = 0). The ONCTL_EN_S3I and ONCTL_EN_S45 bits enable or disable wake-up by the event when the PC8741x device is in S3I or in S45 current state, respectively. Only two events lack a Wake-Up State Enable register (WK_ST_EN). These are:

- — The watchdog event (flagged by the WDO_EVT_STS bit): this event does not affect $\overline{ONCTL}$ generation.
- — The Power button event (flagged by either the PWBT_EVT_STS bit or the PWRBTN_STS bit): this event unconditionally generates a wake-up (sets $\overline{ONCTL}$ = 0) when the PC8741x device is in S3I or S45 current states.

In addition, in Legacy Power Button mode (LEGACY_PWBT = 1 in the PWONCTL register), all wake-up events are ignored (regardless of the bit value in their WK_ST_EN register) after the power supply has been turned off (by setting $\overline{ONCTL}$ = 1) in response to a Power button event. In this case, the next Power button event unconditionally generates a wake-up (sets $\overline{ONCTL}$ = 0).

Optionally, the system ACPI controller can be located in an external device. To select this option, both the EXT_ST_SELECT bit in the SLP_ST_CFG register (see Section 9.3.31 on page 200) and the EXTSTMUX bit in the SIOCF3 register (see Section 3.7.4 on page 51) must be set to ‘1’. In this case, $\overline{ONCTL}$ is turned On when the $\overline{SLPS3}$ signal goes high (the system is in S0 - S2 states). In this mode, $\overline{ONCTL}$ is independent of any wake-up event, including the Power button event (flagged by either the PWBT_EVT_STS bit or the PWRBTN_STS bit).

Any valid wake-up event is disabled from reactivating the V_{DD} power supply (by setting $\overline{ONCTL}$ = 0) for 1 second after the power supply has been turned off (by setting $\overline{ONCTL}$ = 1). This feature protects the power supply from repeated on/off switching if an event (such as Power button) is active for an extended period of time. If the Keyboard/Mouse Power Control feature (VDDFELL; see Section 9.2.10 on page 175) is enabled by setting the VDDFLMUX bit to ‘1’ (in the SIOCF2 register; see Section 3.7.3 on page 50), the Keyboard and Mouse wake-up events are disabled from reactivating the V_{DD} for 2 seconds after the power supply has been turned off (by setting $\overline{ONCTL}$ = 1).

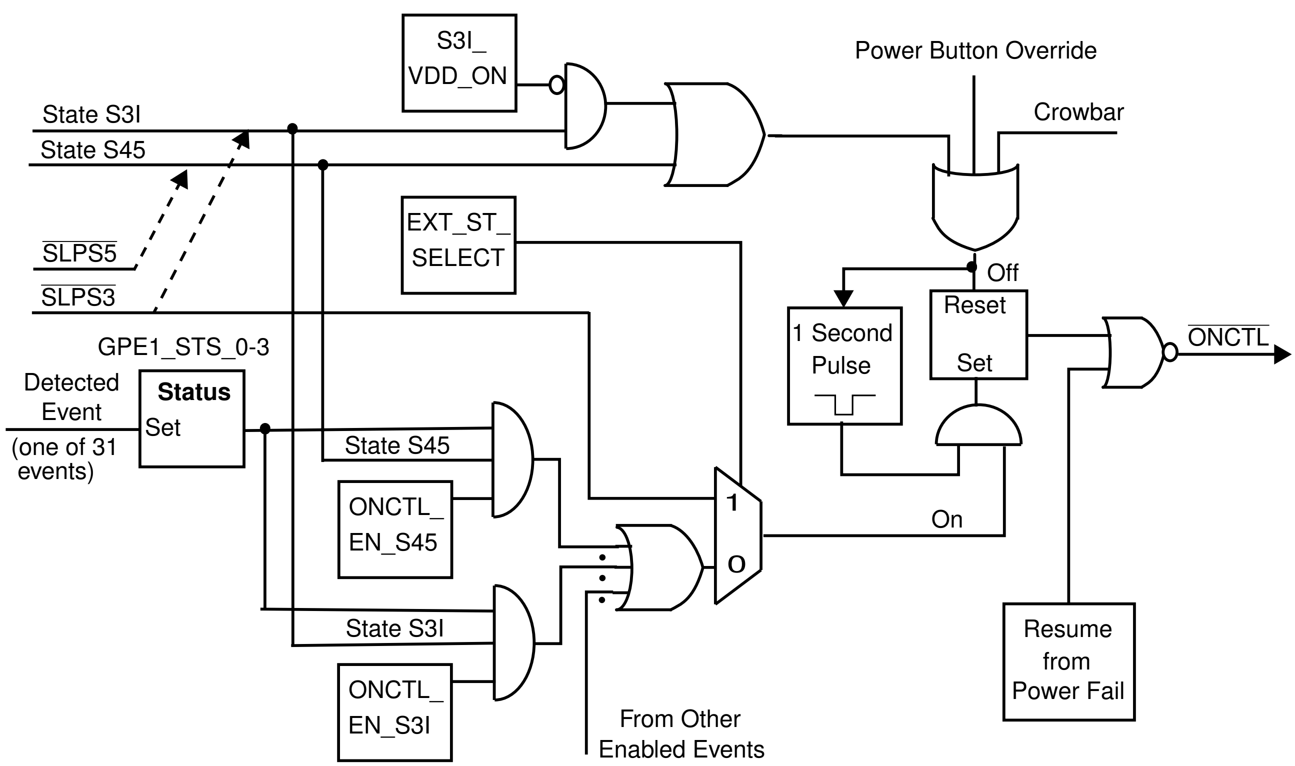


Figure 50. $\overline{ONCTL}$ Control

Power Button Output ($\overline{PWBTOUT}$)

The $\overline{PWBTOUT}$ function of the PC8741x device enables the (optional) external ACPI controller to synchronize its operation to the wake-up events detected by the PC8741x device and to control the V_{DD} power supply.

The Power button input ($\overline{PWBTIN}$) is bridged to $\overline{PWBTOUT}$ regardless of any PC8741x device configuration bits, internal state or wake-up event. This bridging is also independent of the status of the V_{DD} power supply.

9.0 System Wake-Up Control (SWC) (Continued)

In addition, a wake-up mechanism can be enabled to trigger a 100 ms pulse at the $\overline{\text{PWBTOUT}}$ output on each valid wake-up event. This wake-up mechanism is routed to the $\overline{\text{PWBTOUT}}$ pulse generator only if the PWBTOUT_MODE bit in the ACPI_CFG register (see Section 9.3.32 on page 201) is reset.

The $\overline{\text{PWBTOUT}}$ wake-up mechanism is similar to the one described for the $\overline{\text{ONCTL}}$ signal, as follows:

- It is based on status bits in the GPE1_STS_0 to GPE1_STS_3 registers and in the PM1b_STS_HIGH register (except the PWBT_EVT_STS and the PWRBTN_STS bits).
- It is not affected by the Watchdog Status bit (WDO_EVT_STS).
- It is independent of the enable bits in the GPE1_EN_0 to GPE1_EN_3 registers and in the PM1b_EN_HIGH register.
- It is dependent only on the S3I and S45 current sleep states.
- Its configuration bits are also located in the WK_ST_EN register, which is accessed by writing the event index value into the WKUPSEL field of the WK_EVT_SEL register.

The PWBT_EN_S3I and PWBT_EN_S45 bits control the generation of a wake-up pulse on $\overline{\text{PWBTOUT}}$ by an active event (currently accessed through the WK_EVT_SEL register) when the PC8741x device is in S3I or in S45 current state, respectively.

Any valid wake-up event is disabled from generating a wake-up pulse on $\overline{\text{PWBTOUT}}$ for 1 second after the power supply has been turned off (by setting $\overline{\text{ONCTL}}$ = 1). If the Keyboard/Mouse Power Control feature (VDDFELL) is enabled by setting the VDDFLMUX bit to ‘1’ (in the SIOCF2 register; see Section 3.7.3 on page 50), the Keyboard and Mouse wake-up events are disabled from generating a wake-up pulse for 2 seconds after the power supply has been turned off (by setting $\overline{\text{ONCTL}}$ = 1).

A $\overline{\text{PWBTOUT}}$ pulse is generated only when the V_{DD} power is not present or when a $\overline{\text{PWBTIN}}$ pulse occurred.

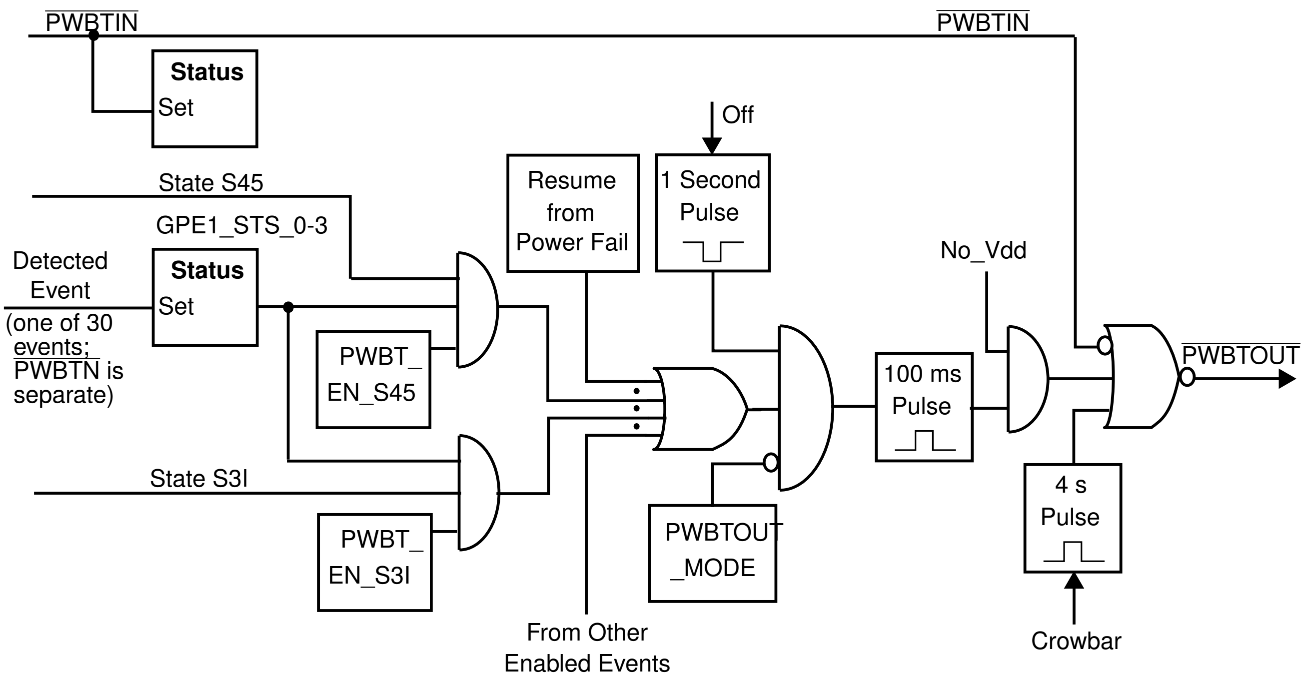


Figure 51. $\overline{\text{PWBTOUT}}$ Control

9.0 System Wake-Up Control (SWC) (Continued)

9.2.6 Special Power Management Functions

Three special Power Management functions are provided by the PC8741x device to respond to abnormal system behavior. These are:

- Power Button Override, which forces the V_{DD} power supply to be turned off when the software does not respond to the SCI interrupt.
- Crowbar, which forces the $\overline{ONCTL}$ to release the On request, thus protecting an overloaded V_{DD} power supply that refuses to turn on.
- Resume from Power Fail, which enables a system to return to a predetermined state when returning from Power Fail (caused by the mechanical switch or by AC power failure).

These functions bypass the mechanisms described in Section 9.2.5 and thus directly control the $\overline{ONCTL}$ and $\overline{PWBTOUT}$ outputs.

Power Button Override

Whenever the Power button ($\overline{PWBTIN}$) is pressed continuously for more than 3.9 seconds, the PC8741x device detects a Power Button Override condition. The Power button pressing at $\overline{PWBTIN}$ is replicated at $\overline{PWBTOUT}$ during these 3.9 seconds. $\overline{PWBTOUT}$ is then forced active for 0.2 seconds regardless of the actual level at $\overline{PWBTIN}$. Thus, the pulse generated at $\overline{PWBTOUT}$ has a width of minimum 4.1 seconds, allowing an (optional) external ACPI controller to detect this Power Button Override condition. In addition, at the end of the 4.1 seconds, $\overline{ONCTL}$ is forced to inactive level (V_{DD} power supply Off).

A Power Button Override condition also resets the PWRBTN_STS bit in the PM1b_STS_HIGH register (set by the Power button event) and updates the current sleep state of the PC8741x device to S45 (since the software is not capable of doing it). In addition, it sets the PWR_OVR_STS bit in the SWC_CTL register.

This function bypasses the regular control on the $\overline{ONCTL}$ and $\overline{PWBTOUT}$ signals (see Figures 50 and 51).

After a Power Button Override condition, only an active Power button event is allowed to wake-up the system (by setting $\overline{ONCTL}$ = 0 and generating a $\overline{PWBTOUT}$ pulse). However, in order to protect the power supply, $\overline{ONCTL}$ can go active ($\overline{ONCTL}$ = 0) only 1 second after the power supply has been turned off (by setting $\overline{ONCTL}$ = 1).

In Legacy Power Button mode, when the V_{DD} power is on, pressing the Power button ($\overline{PWBTIN}$) forces $\overline{ONCTL}$ to inactive level (V_{DD} power supply Off) before a Power Button Override condition is detected. In this case, the PWR_OVR_STS bit is not set.

Crowbar

When a valid wake-up event or a high $\overline{SLPS3}$ signal activates the V_{DD} power supply (by setting $\overline{ONCTL}$ = 0), the PC8741x device starts checking the presence of the V_{DD} power. If the V_{DD} power fails to resume for a time period longer than the Crowbar timeout, the power-on request is aborted (by setting $\overline{ONCTL}$ = 1). Crowbar timeout is also started if the V_{DD} power falls while the V_{DD} power supply is On ($\overline{ONCTL}$ = 0). If the V_{DD} power fails to resume before the timeout period expired, the V_{DD} power supply is turned off (by setting $\overline{ONCTL}$ = 1).

After turning the V_{DD} power supply Off (by setting $\overline{ONCTL}$ = 1), a 4 sec pulse is generated at the $\overline{PWBTOUT}$ output. This pulse informs an (optional) external ACPI controller of the occurrence of the Crowbar timeout by simulating a Power Button Override condition.

This function bypasses the regular control of the $\overline{ONCTL}$ and $\overline{PWBTOUT}$ signals (see Figures 50 and 51).

The Crowbar timeout value is selected by the CRBAR_TOUT field in the PWONCTL register (see Section 9.3.11 on page 188). The equivalent timeout is in the range of 0.5 to 20 seconds (the default value is 20 seconds).

When a Crowbar event is detected, the CROWBAR_STS bit in the SWC_CTL register (see Section 9.3.10 on page 187) is set.

Only an active Power button event is allowed to retry the activation of the V_{DD} power supply (by setting $\overline{ONCTL}$ = 0). However, no retry can take place for 5 seconds after the V_{DD} power supply was turned off (by setting $\overline{ONCTL}$ = 1) because all wake-up events (including Power button) are disabled for 1 second after the end of the $\overline{PWBTOUT}$ pulse.

Resume from Power Fail

Whenever a Power Fail condition is detected (i.e., when V_{DD} and V_{SB} power supplies are off), the value of the $\overline{ONCTL}$ signal is saved in the LAST_ONCTL bit of the PWONCTL register (see Section 9.3.11 on page 188). When the system exits Power Fail (i.e., when V_{SB} power is back on), this read-only bit serves as a snapshot of the V_{DD} power supply status before the power was turned off (by an external agent, such as a mechanical switch).

The WAS_PFAIL bit in the PWONCTL register is set by V_{SB} Power-Up reset (the system exits Power Fail), thus indicating that a Resume from Power Fail condition occurred. This indication is used by the software to decide if the system woke up from Power Fail or from a sleep state.

The Resume from Power Fail process starts 1 second after the V_{SB} power is on. This prevents the selection of an erroneous current sleep state during V_{SB} power-On transitions.

9.0 System Wake-Up Control (SWC) (Continued)

The RESUME_MD field in the PWONCTL register controls the behavior of the $\overline{\text{ONCTL}}$ and $\overline{\text{PWBTOUT}}$ signals during a Resume from Power Fail condition (see Table 49 on page 189):

- 00b – The state of the $\overline{\text{ONCTL}}$ and $\overline{\text{PWBTOUT}}$ signals is controlled solely by the $\overline{\text{SLPS3}}$ input generated by an (optional) external ACPI controller.
  If the sleep state control by $\overline{\text{SLPS3}}$, $\overline{\text{SLPS5}}$ option is selected by setting both the EXT_ST_SELECT bit in the SLP_ST_CFG register and the EXTSTMUX bit in the SIOCF3 register to '1', and if $\overline{\text{SLPS3}}$ = 1 (no sleep), the V_{DD} power supply is turned on ($\overline{\text{ONCTL}}$ = 0). Otherwise, the V_{DD} power supply remains off. Whenever $\overline{\text{ONCTL}}$ is asserted, a 100 ms pulse is also generated at the $\overline{\text{PWBTOUT}}$ output to inform an (optional) external ACPI controller of the new status of the V_{DD} power supply.
  If the $\overline{\text{SLPS3}}$, $\overline{\text{SLPS5}}$ option is not selected (EXT_ST_SELECT bit in the SLP_ST_CFG register and EXTSTMUX bit in the SIOCF3 register are both '0'), the V_{DD} power supply remains off ("Silent mode").
- 01b – The PC8741x device behaves the same as in the 00b combination.
  In addition, if an RTC Alarm event was active during the Power Fail, the V_{DD} power supply is turned on ($\overline{\text{ONCTL}}$ = 0) and a 100 ms pulse is generated at the $\overline{\text{PWBTOUT}}$ output. This happens regardless of the setting of the EXT_ST_SELECT and EXTSTMUX bits or of the value of the $\overline{\text{SLPS3}}$ input.
- 10b – The state of the $\overline{\text{ONCTL}}$ and $\overline{\text{PWBTOUT}}$ signals is controlled solely by the LAST_ONCTL bit of the PWONCTL register regardless of the setting of the EXT_ST_SELECT and EXTSTMUX bits.
  If LAST_ONCTL = 1 (V_{DD} power was on before Power Fail), the V_{DD} power supply is turned on ($\overline{\text{ONCTL}}$ = 0) and a 100 ms pulse is generated at the $\overline{\text{PWBTOUT}}$ output. Otherwise, the V_{DD} power supply remains off.
- 11b – The PC8741x device behaves the same as in the 10b combination.
  In addition, if an RTC Alarm event was active during the Power Fail, the V_{DD} power supply is turned on ($\overline{\text{ONCTL}}$ = 0) and a 100 ms pulse is generated at the $\overline{\text{PWBTOUT}}$ output. This happens regardless of the value of the LAST_ONCTL bit of the PWONCTL register.

The Resume from Power Fail function bypasses the regular control on the $\overline{\text{ONCTL}}$ and $\overline{\text{PWBTOUT}}$ signals.

After the Resume from Power Fail process ends, the $\overline{\text{ONCTL}}$ and $\overline{\text{PWBTOUT}}$ signals behave as described in Section 9.2.5 and in the *Power Button Override* and *Crowbar* sections (page 172).

9.2.7 LED Control

The PC8741x devices support LED indicators for two purposes:

- Visual indication of the system power state or sleep state.
- General-purpose visual indication of the software status.

The LEDCFG bit selects the configuration of the LED connection. There are two possible configurations: two regular LEDs are connected between each pin and ground or V_{SB} (one at LED1 and the other at LED2 pins) or one dual-color LED is connected between the LED1 and LED2 pins. The LEDPOL bit selects the polarity of the On state at both pins (LED1 and LED2). The LEDCFG and LEDPOL bits are located in the LEDCTL register (see Section 9.3.12 on page 190). The polarity of the On state at LED1 and LED2 pins depends on the setting of the LEDCFG and LEDPOL bits (see Table).

Table 42. LED On Polarity as a Function of LEDCFG and LEDPOL

LEDCFG	LEDPOL	LED1	LED2	Connection
0	0	High	Low	LED1 to LED2
0	1	Low	High	LED2 to LED1
1	0	High	High	LED1 and LED2 to GND
1	1	Low	Low	LED1 and LED2 to V_{SB}

The LED1BLNK and LED2BLNK fields in the LEDBLNK register control the On/Off state or the blinking rate of the LED1 and LED2 pins, respectively. For each LED pin, a different blink rate can be selected. Different blink rates can also be selected for the dual-color LED mode (LEDCFG = 0).

The LEDMOD field in the LEDCTL register controls the behavior of the LED1 and LED2 pins in each power state or sleep state (see Table 50 on page 190):

9.0 System Wake-Up Control (SWC) (Continued)

- 00b – The behavior of the LED1 and LED2 pins is controlled by software only (through the setting of the LED1BLNK and LED2BLNK fields), except for the Power Fail state (V_{SB} and V_{DD} off) when both LEDs are Off.
- 01b – The behavior of the LED1 and LED2 pins is controlled by the power states and by software.
  In the Power Fail state (V_{SB} and V_{DD} off), both LEDs are Off;
  In the Power Off state (V_{SB} on and V_{DD} off), both LEDs blink at a 1 Hz rate, with a 50% duty cycle;
  In the Power On state (V_{SB} and V_{DD} on), each LED behaves according to the setting of its LEDxBLNK field.
- 10b – The behavior of the LED1 and LED2 pins is controlled by the S3I sleep state and by software.
  In the Power Fail state (V_{SB} and V_{DD} off) and in the S45 sleep state, both LEDs are Off;
  In the Power On state (V_{SB} and V_{DD} on) and in the S3I sleep state, each LED behaves according to the setting of its LEDxBLNK field.
- 11b – The behavior of the LED1 and LED2 pins is controlled by the sleep states and by software.
  In the Power Fail state (V_{SB} and V_{DD} off), both LEDs are Off;
  In the Power On state (V_{SB} and V_{DD} on) and in the S45 and S3I sleep states, each LED behaves according to the setting of its LEDxBLNK field.

9.2.8 Power Active Timers

The SWC includes two 32-bit Power Active timers: a V_{DD} Active Timer, and a V_{SB} Active Timer. Each timer is clocked by a 1 Hz internal clock derived from the battery-backed 32.768 kHz crystal clock generator.

These timers measure the cumulative amount of time (in seconds) that the V_{SB} and the V_{DD} power supplies are active (On). Each of them is enabled for counting when its related power supply is turned on and stops counting when the power supply goes off.

Due to their 32-bit length, the timers do not need to be reset; however, a reset bit is available for each timer (VSB_TMR_RST and VDD_TMR_RST) in the PWTMRCTL register (see Section 9.3.29 on page 199).

The timer count data of the V_{DD} Active Timer is available to the software in the VDD_ON_TMR_0 to VDD_ON_TMR_3 read-only registers (see Sections 9.3.21 to 9.3.24 on pages 196ff.), which are updated each second with the actual count value of the timer. When VDD_ON_TMR_0 (the LSByte of the count data) is read, the updating of all four registers (VDD_ON_TMR_0 to VDD_ON_TMR_3) is stopped, freezing the count value. The VDD_ON_TMR_1 and VDD_ON_TMR_2 registers can then be read in any order. Finally, reading from the VDD_ON_TMR_3 register resumes the registers updating with the actual count value of the timer. Therefore, the VDD_ON_TMR_0 register must be read first and the VDD_ON_TMR_3 register last.

The same applies for the V_{SB} Active Timer, whose timer count data is available to the software in the VSB_ON_TMR_0 to VSB_ON_TMR_3 read-only registers (see Sections 9.3.25 to 9.3.28 on pages 197ff.).

9.2.9 Watchdog Function

The watchdog includes an 8-bit timer clocked by a 1-minute internal clock that is derived from the battery-backed 32.768 KHz crystal clock generator. The timer is loaded with the Watchdog Time-Out Data value written in the WDTO register (see Section 9.3.34 on page 202) and counts down to zero. This 8-bit data enables time-out values between 1 to 255 minutes to be programmed (00h is an invalid data value).

Five events can trigger the watchdog by reloading the timer:

- Keyboard interrupt.
- Mouse interrupt.
- Serial Port 1 interrupt.
- Serial Port 2 interrupt.
- Software writing a ‘1’ to the SW_WD_TRG bit of the WDCTL register (see Section 9.3.33 on page 202).

Each event can be masked by an enable bit in the WDCFG register (see Section 9.3.35 on page 203). Whenever an active edge of any enabled event is detected, the timer is restarted from the Watchdog Time-Out Data value. If no event occurs before the timer reaches 00h, the WDO_EVT_STS status bit in the GPE1_STS_3 register (see Section 9.4.11 on page 211) is set to ‘1’ and a 250 ms active low pulse is generated at the $\overline{\text{WDO}}$ pin. After a watchdog time-out or when the Hardware reset is active ($\overline{\text{LRESET}}$), the timer is reloaded.

The WDO_EVT_STS status bit can be routed either to the $\overline{\text{SIOSMI}}$ pin by the WDO_EVT_2SMI bit in the GPE1_2SMI_HIGH register (see Section 9.3.7 on page 184) or to the $\overline{\text{SIOSCI}}$ pin by the WDO_EVT_EN bit in the GPE1_EN_3 register (see Section 9.4.15 on page 215).

After either V_{SB} Power-up reset or V_{DD} Power-up reset, the watchdog is disabled. Its operation is enabled by setting the WDEN bit in the WDCTL register (see Section 9.3.33 on page 202) to ‘1’. Once set, this bit cannot be cleared by software.

9.0 System Wake-Up Control (SWC) (Continued)

The V_{SB} Power-up and V_{DD} Power-up resets both de-assert the $\overline{WDO}$ signal before the 250 ms have passed. The WDO_EVT_STS status bit is cleared by the V_{SB} Power-up reset.

Usage Hints Before changing the Watchdog Time-Out Data value in the WDTO register, set all the enable bits of the watchdog trigger events to ‘0’ - disable (in the WDCFG register; see Section 9.3.35 on page 203). Re-enable the watchdog trigger events (set to ‘1’) after writing the new Watchdog Time-Out Data.

9.2.10 Miscellaneous Functions

Power Management Control

The SWC contains two Power Management registers, which allows the software to disable each Legacy module and to TRI-STATE its outputs in a centralized manner.

The SWC Fast Disable register (SWCFDIS) provides a fast way for the Power Management software to disable one or more Legacy modules without having to access the Activate register of each module (at index 30h) through the Index/Data registers. The FDC, Parallel Port, Serial Port 1, Serial Port 2, Mouse Control and Keyboard Control logical devices can be disabled through the SWCFDIS register (see Section 9.3.8 on page 185).

The SWC TRI-STATE register (SWCTRIS) also provides a fast way for the Power Management software to float the outputs of one or more Legacy modules without having to access their TRI-STATE Control bit in the Special Configuration register at index F0h. The module outputs enter TRI-STATE only when the module is disabled. The FDC, Parallel Port, Serial Port 1, Serial Port 2, Mouse and Keyboard Control module outputs can be TRI-STATED through the SWCTRIS register (see Section 9.3.9 on page 186).

Keyboard/Mouse Power Control (VDDFELL)

If the VDDFLMUX bit in the SIOCF2 register (see Section 3.7.3 on page 50) is set to ‘1’, the SWC generates a 1 second, active high pulse at the VDDFELL pin each time the V_{DD} power supply is turned off (by setting the ONCTL signal to high level). This signal can be used by the system to turn off V_{SB} power to the Keyboard and Mouse devices, thus causing them to reset their internal circuits.

9.0 System Wake-Up Control (SWC) (Continued)

9.3 SWC REGISTERS

The SWC registers are organized in four banks. The offsets are related to the base address determined by the SWC Base Address register at indexes 60h - 61h in the SWC device configuration. The lower 16 offsets (00h-0Fh) are common to the four banks; the upper offsets (10h-1Fh) are divided as follows:

- Bank 0 holds registers related to the Keyboard/Mouse Wake-up Detector.
- Bank 1 holds registers related to the Power Active timers.
- Bank 2 holds registers related to sleep states and ACPI configuration.
- Bank 3 holds registers related to the watchdog.

The active bank is selected through the BNK_SEL1-BNK_SEL0 bits in the Bank Select register (BANKSEL). For details, see Section 9.3.15 on page 192.

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from a specific register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

9.3.1 SWC Register Map

The following tables list the SWC registers. For the SWC register bitmap, see Section 9.5 on page 216. Most of the registers are battery backed, however some are V_{SB} powered.

Table 43. Banks 0, 1, 2 and 3 - Common Register Map

Offset	Mnemonic	Register Name	Type	Power Well	Section
00h	WK_EVT_SEL	Wake-Up Event Select	R/W	V_{PP}	9.3.2
01h	WK_ST_EN	Wake-Up State Enable	R/W	V_{PP}	9.3.3
02h	GPE1_2IRQ_LOW	GPE1_STS Events to IRQ Enable Low	R/W	V_{PP}	9.3.4
03h	GPE1_2IRQ_HIGH	GPE1_STS Events to IRQ Enable High	R/W	V_{PP}	9.3.5
04h	GPE1_2SMI_LOW	GPE1_STS Events to SMI Enable Low	R/W	V_{PP}	9.3.6
05h	GPE1_2SMI_HIGH	GPE1_STS Events to SMI Enable High	R/W	V_{PP}	9.3.7
06h	SWCFDIS	SWC Fast Disable	R/W	V_{SB}	9.3.8
07h	SWCTRIS	SWC TRI-STATE	R/W	V_{SB}	9.3.9
08h	SWC_CTL	SWC Miscellaneous Control	Varies per bit	V_{PP}	9.3.10
09h	PWONCTL	Power On Control	Varies per bit	V_{PP}	9.3.11
0Ah	LEDCTL	LED Control	R/W	V_{PP}	9.3.12
0Bh	LEDBLNK	LED Blinking Control	R/W	V_{PP}	9.3.13
0Ch-0Dh	Reserved				
0Eh	BIOSGPR	BIOS General-Purpose Scratch	R/W	V_{PP}	9.3.14
0Fh	BANKSEL	Bank Select	R/W	V_{PP}	9.3.15

9.0 System Wake-Up Control (SWC) (Continued)

Table 44. Bank 0 - Keyboard/Mouse Wake-Up Detector Register Map

Offset	Mnemonic	Register Name	Type	Power Well	Section
10h-11h	Reserved				
12h	KBDWKCTL	Keyboard Wake-Up Control	R/W	V_{PP}	9.3.16
13h	PS2CTL	PS2 Protocol Control	R/W	V_{PP}	9.3.17
14h-15h	Reserved				
16h	KDSR	Keyboard Data Shift-Register	RO	V_{PP}	9.3.18
17h	MDSR	Mouse Data Shift-Register	RO	V_{PP}	9.3.19
18h	PS2KEY0	PS2 Keyboard Key Data 0	R/W	V_{PP}	9.3.20
19h	PS2KEY1	PS2 Keyboard Key Data 1	R/W	V_{PP}	9.3.20
1Ah	PS2KEY2	PS2 Keyboard Key Data 2	R/W	V_{PP}	9.3.20
1Bh	PS2KEY3	PS2 Keyboard Key Data 3	R/W	V_{PP}	9.3.20
1Ch	PS2KEY4	PS2 Keyboard Key Data 4	R/W	V_{PP}	9.3.20
1Dh	PS2KEY5	PS2 Keyboard Key Data 5	R/W	V_{PP}	9.3.20
1Eh	PS2KEY6	PS2 Keyboard Key Data 6	R/W	V_{PP}	9.3.20
1Fh	PS2KEY7	PS2 Keyboard Key Data 7	R/W	V_{PP}	9.3.20

Table 45. Bank 1 - Power Active Timers Register Map

Offset	Mnemonic	Register Name	Type	Power Well	Section
10h	VDD_ON_TMR_0	V_{DD} Active Timer 0	RO	V_{PP}	9.3.21
11h	VDD_ON_TMR_1	V_{DD} Active Timer 1	RO	V_{PP}	9.3.22
12h	VDD_ON_TMR_2	V_{DD} Active Timer 2	RO	V_{PP}	9.3.23
13h	VDD_ON_TMR_3	V_{DD} Active Timer 3	RO	V_{PP}	9.3.24
14h	VSB_ON_TMR_0	V_{SB} Active Timer 0	RO	V_{PP}	9.3.25
15h	VSB_ON_TMR_1	V_{SB} Active Timer 1	RO	V_{PP}	9.3.26
16h	VSB_ON_TMR_2	V_{SB} Active Timer 2	RO	V_{PP}	9.3.27
17h	VSB_ON_TMR_3	V_{SB} Active Timer 3	RO	V_{PP}	9.3.28
18h	PWTMRCTL	Power Active Timers Control	Varies per bit	V_{PP}	9.3.29
19h-1Fh	Reserved				

9.0 System Wake-Up Control (SWC) (Continued)

Table 46. Bank 2 - Sleep States and ACPI Configuration Register Map

Offset	Mnemonic	Register Name	Type	Power Well	Section
10h	S0_SLP_TYP	S0 Sleep Type Encoding	R/W or RO	V_{PP}	9.3.30
11h	S1_SLP_TYP	S1 Sleep Type Encoding	R/W or RO	V_{PP}	9.3.30
12h	S2_SLP_TYP	S2 Sleep Type Encoding	R/W or RO	V_{PP}	9.3.30
13h	S3_SLP_TYP	S3 Sleep Type Encoding	R/W or RO	V_{PP}	9.3.30
14h	S4_SLP_TYP	S4 Sleep Type Encoding	R/W or RO	V_{PP}	9.3.30
15h	S5_SLP_TYP	S5 Sleep Type Encoding	R/W or RO	V_{PP}	9.3.30
16h	SLP_ST_CFG	Sleep State Configuration	Varies per bit	V_{PP}	9.3.31
17h	ACPI_CFG	ACPI Configuration	R/W	V_{PP}	9.3.32
18h-1Fh	Reserved				

Table 47. Bank 3 - Watchdog Register Map

Offset	Mnemonic	Register Name	Type	Power Well	Section
10h	WDCTL	Watchdog Control	Varies per bit	V_{SB}	9.3.33
11h	WDTO	Watchdog Time-Out	R/W	V_{SB}	9.3.34
12h	WDCFG	Watchdog Configuration	R/W	V_{SB}	9.3.17
13h-1Fh	Reserved				

9.3.2 Wake-Up Event Select Register (WK_EVT_SEL)

This register selects the wake-up event to be configured (i.e., which register is accessed via the Wake-Up State Enable register). Since access to the Wake-Up State Enable register requires two transactions (first to WK_EVT_SEL and then to WK_ST_EN) and since the LPC bus and ACCESS.bus access the module concurrently (**PC87413 and PC87417**), the WK_EVT_SEL register is duplicated (one accessed by the host and one by the ACCESS.bus).This register is reset by hardware to 00h.

The wake-up events selected through this register are active when either the bits of the GPE1_STS_0 to GPE1_STS_3 registers or the PM1b_STS_HIGH register are set. Table 48 shows the mapping of the WKUPSEL field value to each wake-up event and the related status bit.

Power Well:V_{PP}

Location: **All Banks**, Offset 00h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**WKUPSEL**				
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4-0	**WKUPSEL (Wake-Up Event Select).** These bits select a wake-up event to be configured through the WK_ST_EN register (see Table 48). 00000: GPIOE10 Event Status (default) 00001 to 11111: Wake-up events (see Table 48)

9.0 System Wake-Up Control (SWC) (Continued)

Table 48. Wake-Up Event Select Field Map

WKUPSEL	Wake-Up Event Name	WK_ST_EN Class	GPE1_STS_n Bit	PM1b_STS_HIGH Bit	Notes
00h	GPIOE10 Event Status	A	GPIOE10_STS		
01h	GPIOE11 Event Status	A	GPIOE11_STS		
02h	GPIOE12 Event Status	A	GPIOE12_STS		
03h	GPIOE13 Event Status	A	GPIOE13_STS		
04h	GPIOE14 Event Status	A	GPIOE14_STS		
05h	GPIOE15 Event Status	A	GPIOE15_STS		
06h	GPIOE16 Event Status	A	GPIOE16_STS		
07h	GPIOE17 Event Status	A	GPIOE17_STS		
08h	GPIOE40 Event Status	A	GPIOE40_STS		
09h	GPIOE41 Event Status	A	GPIOE41_STS		
0Ah	GPIOE42 Event Status	A	GPIOE42_STS		
0Bh	GPIOE43 Event Status	A	GPIOE43_STS		
0Ch	GPIOE44 Event Status	A	GPIOE44_STS		
0Dh	GPIOE45 Event Status	A	GPIOE45_STS		
0Eh	GPIOE46 Event Status	A	GPIOE46_STS		
0Fh	GPIOE47 Event Status	A	GPIOE47_STS		
10h	$\overline{\text{RI1}}$ Event Status	A	RI1_EVT_STS		
11h	$\overline{\text{RI2}}$ Event Status	A	RI2_EVT_STS		
12h	Mouse Event Status	A	MS_EVT_STS		
13h	Keyboard Event 1 Status	A	KBD_EVT1_STS		
14h	Keyboard Event 2 Status	A	KBD_EVT2_STS		
15h	Keyboard Event 3 Status	A	KBD_EVT3_STS		
16h	Sleep Button Event Status	A	SLBT_EVT_STS	SLPBTN_STS	ORed bits
17h	Reserved				
18h	RTC Alarm Event Status	A	RTC_EVT_STS	RTC_STS	ORed bits
19h	Port P12 Event Status	B	P12_EVT_STS		
1Ah	Keyboard IRQ Event Status	B	KBD_IRQ_STS		
1Bh	Mouse IRQ Event Status	B	MS_IRQ_STS		
1Ch	Modules IRQ Event Status	A	MOD_IRQ_STS		
1Dh	Reserved				
1Eh	Software On Event Status	A	SW_ON_STS		
1Fh	Software Off Event Status	A	SW_OFF_STS		

9.0 System Wake-Up Control (SWC) (Continued)

9.3.3 Wake-Up State Enable Register (WK_ST_EN)

This register configures the wake-up event selected by the Wake-Up Event Select register. Two different classes (A and B) are defined for this register (see Table 48 on page 179). Both classes are reset by hardware to 00h.

The sleep states for which the outputs are enabled when the event is active are PC8741x device current states (see Section 9.2.3 on page 167).

Power Well:V_{PP}

Location: **All Banks**, Offset 01h

Type: R/W

Class: A

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**PWBT_EN_S3I**	**PWBT_EN_S45**	**ONCTL_EN_S3I**	**ONCTL_EN_S45**
Reset	0	0	0	0	0	0	0	0

Class: B

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**ONCTL_EN_S3I**	**ONCTL_EN_S45**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved.**
3 Class A	**PWBT_EN_S3I ($\overline{\text{PWBTOUT}}$ Pulse Enable in S3I).** Enables generating a $\overline{\text{PWBTOUT}}$ pulse when the selected event becomes active and the device is in S3I sleep state. The selected event affects the output regardless of the setting of the related enable bit in the GPE1_EN_n register. However, for a $\overline{\text{PWBTOUT}}$ pulse to be generated, the PWBTOUT_MODE bit in the ACPI_CFG register (see Section 9.3.32 on page 201) must be ‘0’. 0: Disable pulse (default) 1: Enable pulse in S3I state
2 Class A	**PWBT_EN_S45 ($\overline{\text{PWBTOUT}}$ Pulse Enable in S45).** Enables generating a $\overline{\text{PWBTOUT}}$ pulse when the selected event becomes active and the device is in S45 sleep state. The selected event affects the output regardless of the setting of the related enable bit in the GPE1_EN_n register. However, for a $\overline{\text{PWBTOUT}}$ pulse to be generated, the PWBTOUT_MODE bit in the ACPI_CFG register (see Section 9.3.32 on page 201) must be ‘0’. 0: Disable pulse (default) 1: Enable pulse in S45 state
3-2 Class B	**Reserved.**
1	**ONCTL_EN_S3I ($\overline{\text{ONCTL}}$ Active Enable in S3I).** Enables activation (turning the V_{DD} power On) Of the $\overline{\text{ONCTL}}$ output when the selected event becomes active and the device is in the S3I sleep state. The selected event affects the output regardless of the setting of the related enable bit in the GPE1_EN_n register. This bit is relevant only if the PC8741x device is the ACPI controller of the system (EXT_ST_SELECT = 0 in the SLP_ST_CFG register). 0: Disable activation (default) 1: Enable activation in S3I state
0	**ONCTL_EN_S45 ($\overline{\text{ONCTL}}$ Active Enable in S45).** Enables activation (turning the V_{DD} power On) of the $\overline{\text{ONCTL}}$ output when the selected event becomes active and the device is in the S45 sleep state. The selected event affects the output regardless of the setting of the related enable bit in the GPE1_EN_n register. This bit is relevant only if the PC8741x device is the ACPI controller of the system (EXT_ST_SELECT = 0 in the SLP_ST_CFG register). 0: Disable activation (default) 1: Enable activation in S45 state

9.0 System Wake-Up Control (SWC) (Continued)

9.3.4 GPE1_STS Events to IRQ Enable Low Register (GPE1_2IRQ_LOW)

This register enables the wake-up events contained in bits 16-23 of the GPE1_STS register to generate an IRQ. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **All Banks**, Offset 02h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PWBT_EVT _2IRQ**	**SLBT_EVT _2IRQ**	**KBD_EVT3 _2IRQ**	**KBD_EVT2 _2IRQ**	**KBD_EVT1 _2IRQ**	**MS_EVT _2IRQ**	**RI2_EVT _2IRQ**	**RI1_EVT _2IRQ**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**PWBT_EVT_2IRQ (Power Button Event to IRQ Enable).** Enables the Power button pressing event to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from Power button pressing event
6	**SLBT_EVT_2IRQ (Sleep Button Event to IRQ Enable).** Enables the Sleep button pressing event to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from Sleep button pressing event
5	**KBD_EVT3_2IRQ (Keyboard Event 3 to IRQ Enable).** Enables the “PM Key 3” (keyboard) pressing event to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from pressing “PM Key 3” on the keyboard
4	**KBD_EVT2_2IRQ (Keyboard Event 2 to IRQ Enable).** Enables the “PM Key 2” (keyboard) pressing event to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from pressing “PM Key 2” on the keyboard
3	**KBD_EVT1_2IRQ (Keyboard Event 1 to IRQ Enable).** Enables the event of pressing any keyboard key, key sequence or “PM Key 1” to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from pressing any key, key sequence or “PM Key 1” on the keyboard
2	**MS_EVT_2IRQ (Mouse Event to IRQ Enable).** Enables a mouse event identified by the Keyboard/Mouse Wake-up Detector to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from a mouse event identified by the Keyboard/Mouse Wake-up Detector
1	**RI2_EVT_2IRQ ($\overline{\text{RI2}}$ Event to IRQ Enable).** Enables a telephone ring event received at the Serial Port 2, identified by the RI Wake-up Detector, to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from the telephone ring event received at the Serial Port 2
0	**RI1_EVT_2IRQ ($\overline{\text{RI1}}$ Event to IRQ Enable).** Enables a telephone ring event received at the Serial Port 1, identified by the RI Wake-up Detector, to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from the telephone ring event received at the Serial Port 1

9.0 System Wake-Up Control (SWC) (Continued)

9.3.5 GPE1_STS Events to IRQ Enable High Register (GPE1_2IRQ_HIGH)

This register enables the wake-up events contained in 24-31 of the GPE1_STS register to generate an IRQ. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **All Banks**, Offset 03h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SW_OFF _2IRQ**	**SW_ON _2IRQ**	**Reserved**				**P12_EVT _2IRQ**	**Reserved**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**SW_OFF_2IRQ (Software Off Event to IRQ Enable).** Enables the event of the software writing a ‘1’ to the SW_OFF_CTL bit in the SWC_CTL register to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from the software writing a ‘1’ to the SW_OFF_CTL bit in the SWC_CTL register
6	**SW_ON_2IRQ (Software On Event to IRQ Enable).** Enables the event of the software writing a ‘1’ to the SW_ON_CTL bit in the SWC_CTL register to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from the software writing a ‘1’ to the SW_ON_CTL bit in the SWC_CTL register
5-2	**Reserved.**
1	**P12_EVT_2IRQ (Port P12 Event to IRQ Enable).** Enables an active high signal generated at the P12 pin to generate an IRQ. 0: Disable IRQ (default) 1: Enable IRQ from an active high signal generated at the P12 pin
0	**Reserved.**

9.0 System Wake-Up Control (SWC) (Continued)

9.3.6 GPE1_STS Events to SMI Enable Low Register (GPE1_2SMI_LOW)

This register enables the wake-up events contained in bits 16-23 of the GPE1_STS register to generate an SMI interrupt. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **All Banks**, Offset 04h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PWBT_EVT _2SMI**	**SLBT_EVT _2SMI**	**KBD_EVT3 _2SMI**	**KBD_EVT2 _2SMI**	**KBD_EVT1 _2SMI**	**MS_EVT _2SMI**	**RI2_EVT _2SMI**	**RI1_EVT _2SMI**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**PWBT_EVT_2SMI (Power Button Event to SMI Enable).** Enables the Power button pressing event to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from Power button pressing event
6	**SLBT_EVT_2SMI (Sleep Button Event to SMI Enable).** Enables the Sleep button pressing event to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from Sleep button pressing event
5	**KBD_EVT3_2SMI (Keyboard Event 3 to SMI Enable).** Enables the “PM Key 3” (keyboard) key pressing event to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from pressing “PM Key 3” on the keyboard
4	**KBD_EVT2_2SMI (Keyboard Event 2 to SMI Enable).** Enables the “PM Key 2” (keyboard) key pressing event to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from pressing “PM Key 2” on the keyboard
3	**KBD_EVT1_2SMI (Keyboard Event 1 to SMI Enable).** Enables the event of pressing any keyboard key, key sequence or “PM Key 1” to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from pressing any key, key sequence or “PM Key 1” on the keyboard
2	**MS_EVT_2SMI (Mouse Event to SMI Enable).** Enables a mouse event, identified by the Keyboard/Mouse Wake-up Detector, to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from the mouse event identified by the Keyboard/Mouse Wake-up Detector
1	**RI2_EVT_2SMI ($\overline{\text{RI2}}$ Event to SMI Enable).** Enables a telephone ring event received at the Serial Port 2, identified by the RI Wake-up Detector, to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from the telephone ring event received at the Serial Port 2
0	**RI1_EVT_2SMI ($\overline{\text{RI1}}$ Event to SMI Enable).** Enables a telephone ring event received at the Serial Port 1, identified by the RI Wake-up Detector, to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from the telephone ring event received at the Serial Port 1

9.0 System Wake-Up Control (SWC) (Continued)

9.3.7 GPE1_STS Events to SMI Enable High Register (GPE1_2SMI_HIGH)

This register enables the wake-up events contained in bits 24-31 of the GPE1_STS register to generate an SMI interrupt. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **All Banks**, Offset 05h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SW_OFF _2SMI**	**SW_ON _2SMI**	**WDO_EVT _2SMI**	**Reserved**				**RTC_EVT _2SMI**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**SW_OFF_2SMI (Software Off Event to SMI Enable).** Enables the event of the software writing a ‘1’ to the SW_OFF_CTL bit in the SWC_CTL register to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from the software writing a ‘1’ to the SW_OFF_CTL bit in the SWC_CTL register
6	**SW_ON_2SMI (Software On Event to SMI Enable).** Enables the event of the software writing a ‘1’ to the SW_ON_CTL bit in the SWC_CTL register to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from the software writing a ‘1’ to the SW_ON_CTL bit in the SWC_CTL register
5	**WDO_EVT_2SMI (Watchdog Event to SMI Enable).** Enables a watchdog time-out to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from watchdog time-out
4-1	**Reserved.**
0	**RTC_EVT_2SMI (RTC Alarm Event to SMI Enable).** Enables an RTC alarm to generate an SMI interrupt. 0: Disable SMI (default) 1: Enable SMI from RTC alarm

9.0 System Wake-Up Control (SWC) (Continued)

9.3.8 SWC Fast Disable Register (SWCFDIS)

This register provides a fast way for the Power Management software to disable one or more modules without having to access the Activate register of each module (see Section 3.3.1 on page 43). It is reset by hardware to 00h.

Power Well:V_{SB}

Location: **All Banks**, Offset 06h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**KBDDIS**	**MSDIS**	**SER1DIS**	**SER2DIS**	**PARPDIS**	**FDCDIS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**KBDDIS (Keyboard Controller Disable).** When set to 1, this bit forces the Keyboard Controller module (Logical Device 6) to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
4	**MSDIS (Mouse Controller Disable).** When set to 1, this bit forces the Mouse Controller module (Logical Device 5) to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
3	**SER1DIS (Serial Port 1 Disable).** When set to 1, this bit forces the Serial Port 1 module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
2	**SER2DIS (Serial Port 2 Disable).** When set to 1, this bit forces the Serial Port 2 module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
1	**PARPDIS (Parallel Port Disable).** When set to 1, this bit forces the Parallel Port module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled
0	**FDCDIS (Floppy Disk Controller Disable).** When set to 1, this bit forces the Floppy Disk Controller module to be disabled (and its resources released) regardless of the actual setting of its Activation bit (index 30). 0: Enabled or Disabled, according to Activation bit (default) 1: Disabled

9.0 System Wake-Up Control (SWC) (Continued)

9.3.9 SWC TRI-STATE Register (SWCTRIS)

This register provides a fast way for the Power Management software to float the outputs of one or more modules without having to access their TRI-STATE Control bit in the Special Configuration register at index F0h. The module outputs enter TRI-STATE only when the module is disabled (see Section 9.3.8). The register is reset by hardware to 00h.

Power Well:V_{SB}

Location: **All Banks**, Offset 07h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**KBMSTRIS**	**SER1TRIS**	**SER2TRIS**	**PARPTRIS**	**FDCTRIS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved.**
4	**KBMSTRIS (Keyboard and Mouse Outputs TRI-STATE).** When set to 1 and the module is disabled, this bit forces the outputs of the Keyboard and Mouse Controller to be in TRI-STATE regardless of bit 0 in the Keyboard Configuration register (see Section 3.13.3 on page 69). 0: Enabled or Disabled, according to bit 0 in the Keyboard Configuration register (default) 1: Outputs in TRI-STATE
3	**SER1TRIS (Serial Port 1 Outputs TRI-STATE).** When set to 1 and the module is disabled, this bit forces the outputs of the Serial Port 1 module to be in TRI-STATE regardless of bit 0 in the Serial Port 1 Configuration register (see Section 3.11.3 on page 66). 0: Enabled or Disabled, according to bit 0 in the Serial Port 1 Configuration register (default) 1: Outputs in TRI-STATE
2	**SER2TRIS (Serial Port 2 Outputs TRI-STATE).** When set to 1 and the module is disabled, this bit forces the outputs of the Serial Port 2 module to be in TRI-STATE regardless of bit 0 in the Serial Port 2 Configuration register (see Section 3.10.3 on page 64). 0: Enabled or Disabled, according to bit 0 in the Serial Port 2 Configuration register (default) 1: Outputs in TRI-STATE
1	**PARPTRIS (Parallel Port Outputs TRI-STATE).** When set to 1 and the module is disabled, this bit forces the outputs of the Parallel Port module to be in TRI-STATE regardless of bit 0 in the Parallel Port Configuration register (see Section 3.9.3 on page 62). 0: Enabled or Disabled, according to bit 0 in the Parallel Port Configuration register (default) 1: Outputs in TRI-STATE
0	**FDCTRIS (Floppy Disk Controller Outputs TRI-STATE).** When set to 1 and the module is disabled, this bit forces the outputs of the Floppy Disk Controller module to be in TRI-STATE regardless of bit 0 in the FDC Configuration register (see Section 3.8.3 on page 59). 0: Enabled or Disabled, according to bit 0 in the FDC Configuration register (default) 1: Outputs in TRI-STATE

9.0 System Wake-Up Control (SWC) (Continued)

9.3.10 SWC Miscellaneous Control Register (SWC_CTL)

This register contains control and status bits for the SWC module. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **All Banks**, Offset 08h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**SW_OFF _CTL**	**SW_ON _CTL**	**PWB_OVR _STS**	**CROWBAR _STS**	**Reserved**			**SWAP _KBMS**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W	**SW_OFF_CTL (Software Off Control).** Writing ‘1’ to this bit sets the SW_OFF_STS bit in the GPE1_STS_3 register (see Section 9.4.11 on page 211), which requests a V_{DD} power off sequence. This bit then returns to ‘0’ (read always returns ‘0’). 0: Inactive (default) 1: Requests a V_{DD} power off sequence
6	R/W	**SW_ON_CTL (Software On Control).** Writing ‘1’ to this bit sets the SW_ON_STS bit in the GPE1_STS_3 register (see Section 9.4.11 on page 211), which requests a V_{DD} Power On sequence. This bit then returns to ‘0’ (read always returns ‘0’). When the V_{DD} power is off, this bit can be written only through the ACCESS.bus (**PC87413 and PC87417**). 0: Inactive (default) 1: Requests a V_{DD} Power On sequence
5	R/W1C	**PWB_OVR_STS (Power Button Override Status).** Indicates that the Power Button Override event has occurred (Power button pressed for more than 4 seconds). In this condition the V_{DD} power is unconditionally turned off. Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Inactive (default) 1: Power Button Override event has occurred
4	R/W1C	**CROWBAR_STS (Crowbar Status).** Indicates that the Crowbar event has been detected (V_{DD} remained Off for longer than the Crowbar Timeout). In this condition the V_{DD} power is turned off. Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Inactive (default) 1: Crowbar event has been detected
3-1		**Reserved.**
0	R/W	**SWAP_KBMS (Swap Keyboard and Mouse Inputs).** When this bit is set, the keyboard signals (KBCLK and KBDAT) are swapped with the mouse signals (MCLK and MDAT). This bit must be set to the same value as the Swap bit in the KBC Configuration register (see Section 3.13.3 on page 69). 0: No swapping (default) 1: Swaps the keyboard and mouse signals

9.0 System Wake-Up Control (SWC) (Continued)

9.3.11 Power On Control Register (PWONCTL)

This register controls the power-On process and the way the PC8741x device resumes operation after Power Fail. It is reset by hardware to 87h.

Power Well: V_{PP}

Location: **All Banks**, Offset 09h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**WAS _PFAIL**	**LAST _ONCTL**	**RESUME_MD**		**LEGACY _PWBT**[1]	**CRBAR_TOUT**		
Reset	1	0	0	0	0	1	1	1

1. This bit is powered from the V_{DD} well and is reset either by V_{DD} power-up reset or by hardware reset.

Bit	Type	Description
7	R/W1C	**WAS_PFAIL (Was Power Fail Status).** Indicates that the device has woken up from a Power Fail condition (V_{DD} and V_{SB} off). This bit is set by V_{SB} Power-Up reset. Writing '1' clears this bit; writing '0' is ignored. 0: Inactive 1: Wake-up from Power Fail (default)
6	RO	**LAST_ONCTL (Last Value of $\overline{\text{ONCTL}}$).** This bit reflects the last value of the $\overline{\text{ONCTL}}$ signal when the previous Power Fail condition (V_{DD} and V_{SB} off) occurred. Writing to this bit is ignored. 0: $\overline{\text{ONCTL}}$ inactive - V_{DD} power Off (default) 1: $\overline{\text{ONCTL}}$ active - V_{DD} power On
5-4	R/W	**RESUME_MD (Resume Mode Control).** These bits control the power state to which the PC8741x device resumes after waking-up from a Power Fail condition (i.e., when V_{DD} and V_{SB} are off). Table 49 shows the behavior of the $\overline{\text{ONCTL}}$ and $\overline{\text{PWBTOUT}}$ signals in all four Resume modes.
3	R/W	**LEGACY_PWBT (Legacy Power Button).** This bit allows the Power button to set $\overline{\text{ONCTL}}$ to inactive level (V_{DD} power supply Off). 0: ACPI-compliant Power button - V_{DD} power turned off by sleep state (written into SLP_TYPx field or decoded from $\overline{\text{SLPS3}}$ and $\overline{\text{SLPS5}}$) or by a Power Button Override condition (default) 1: Legacy Power button - V_{DD} power turned off by pressing the Power button ($\overline{\text{PWBTIN}}$) when the V_{DD} power is on
2-0	R/W	**CRBAR_TOUT (Crowbar Timeout Configuration).** This field controls the timeout value for the Crowbar function (the time between the activation of $\overline{\text{ONCTL}}$ and its deactivation as a result of V_{DD} remaining off). After the Crowbar timeout, the PC8741x device waits another second before it accepts a new Power button event. **Bits** **2 1 0 Timeout (Seconds)** 0 0 0: 0.5 0 0 1: 1 0 1 0: 2 0 1 1: 3 1 0 0: 6 1 0 1: 10 1 1 0: 15 1 1 1: 20 (default)

9.0 System Wake-Up Control (SWC) (Continued)

Table 49. $\overline{\text{ONCTL}}$ and $\overline{\text{PWBTOUT}}$ as a Function of the Power Fail Resume Mode

RESUME_MD	EXT_ST_SELECT[1]	$\overline{\text{SLPS3}}$ Pin	LAST_ONCTL	RTC Alarm in Power Fail[2]	$\overline{\text{ONCTL}}$ Pin	$\overline{\text{PWBTOUT}}$ Pin
00 (Default)	0	X	X	X	1	-
	1	0	X	X	1	-
		1	X	X	0 (On)	Pulse[3]
01	0	X	X	0	1	-
	1	0	X	0	1	-
		1	X	X	0 (On)	Pulse[3]
	X	X	X	1	0 (On)	Pulse[3]
10	X	X	0	X	1	-
	X	X	1	X	0 (On)	Pulse[3]
11	X	X	0	0	1	-
	X	X	1	X	0 (On)	Pulse[3]
	X	X	X	1	0 (On)	Pulse[3]

1. EXT_ST_SELECT bit in the SLP_ST_CFG register (see Section 9.3.31 on page 200). The EXTSTMUX bit in the SIOCF3 register (see Section 3.7.4 on page 51) has to be set to the same value as EXT_ST_SELECT.
2. RTC Alarm event active during Power Fail.
3. A pulse is generated only if the PWBTOUT_MODE bit in the ACPI_CFG register is ‘0’ (see Section 9.3.32 on page 201).

9.0 System Wake-Up Control (SWC) (Continued)

9.3.12 LED Control Register (LEDCTL)

This register controls the operation mode of the two LEDs driven by the PC8741x device. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **All Banks**, Offset 0Ah

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**LEDCFG**	**LEDPOL**	**Reserved**		**LEDMOD**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**LEDCFG (LED Configuration).** This bit enables the use of either two regular LEDs, connected between each pin (LED1, LED2) and ground or V_{SB}, or one dual-colored LED, connected between the LED1 and LED2 pins. 0: One dual-colored LED (default) 1: Two regular LEDs
4	**LEDPOL (LED Polarity).** This bit determines the polarity of LED1 and LED2 outputs. An active output, according to this bit setting, turns the LED On. For the dual-colored LED configuration, changing the polarity reverses the LED colors. 0: Active high - LED cathode connected to ground (default) 1: Active low - LED anode connected to V_{SB}
3-2	**Reserved.**
1-0	**LEDMOD (LED Operation Mode).** These bits control the operation mode of LED1 and LED2 in each power state. Table 50 shows the behavior of the LED1 and LED2 outputs as a function of the system power state.

Table 50. LED1 and LED2 as a Function of the Power State

LEDMOD	Power Fail[1]	Power Off[1]	State S45[2]	State S3I[2]	Power On[1]	LED1	LED2
00 (default)	Yes					Off	Off
	No	X	X	X	X	S/W1[3]	S/W2[4]
01	Yes					Off	Off
		Yes	X	X		Blink[5]	Blink[5]
					Yes	S/W1	S/W2
10	Yes					Off	Off
		X	Yes			Off	Off
		X		Yes		S/W1	S/W2
					Yes	S/W1	S/W2
11	Yes					Off	Off
		X	Yes			S/W1	S/W2
		X		Yes		S/W1	S/W2
					Yes	S/W1	S/W2

1. Power Fail: V_{SB} and V_{DD} Off. Power Off: V_{SB} On, V_{DD} Off. Power On: V_{SB} and V_{DD} On;
2. Sleep states S3I and S45 are PC8741x device current states (see Section 9.3.31 on page 200).
3. Controlled by the value of LED1BLNK in the LEDBLNK register.
4. Controlled by the value of LED2BLNK in the LEDBLNK register.
5. 1 Hz blink with 50% duty cycle.

9.0 System Wake-Up Control (SWC) (Continued)

9.3.13 LED Blink Control Register (LEDBLNK)

This register controls the blinking rate of the two LEDs driven by the PC8741x device. It is reset by hardware to 70h.

Power Well:V_{PP}

Location: **All Banks**, Offset 0Bh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**LED2BLNK**			**Reserved**	**LED1BLNK**		
Reset	0	1	1	1	0	0	0	0

Bit	Description
7	**Reserved.**
6-4	**LED2BLNK (LED2 Blink Rate).** These bits control the blinking rate of LED2 output. **Bits** **6 5 4 Rate (Hz) Duty Cycle** 0 0 0: Off Always inactive 0 0 1: 0.25 12.5% 0 1 0: 0.5 25% 0 1 1: 1 50% 1 0 0: 2 50% 1 0 1: 3 50% 1 1 0: 4 50% 1 1 1: On Always active (default)
3	**Reserved.**
2-0	**LED1BLNK (LED1 Blink Rate).** These bits control the blinking rate of LED1 output. **Bits** **2 1 0 Rate (Hz) Duty Cycle** 0 0 0: Off Always inactive (default) 0 0 1: 0.25 12.5% 0 1 0: 0.5 25% 0 1 1: 1 50% 1 0 0: 2 50% 1 0 1: 3 50% 1 1 0: 4 50% 1 1 1: On Always active

9.3.14 BIOS General-Purpose Scratch Register (BIOSGPR)

This register may be used by the BIOS for general-purpose battery-backed data storage. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **All Banks**, Offset 0Eh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**General-Purpose Scratch**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**General-Purpose Scratch**

9.0 System Wake-Up Control (SWC) (Continued)

9.3.15 Bank Select Register (BANKSEL)

This register selects the active bank for the upper offsets (10h-1Fh). Since the access to registers at offsets 10h-1Fh requires two transactions (first to BANKSEL and then to the specific register) and since the LPC bus and ACCESS.bus access the module concurrently (**PC87413 and PC87417**), the BANKSEL register is duplicated (one is accessed by the host and one by the ACCESS.bus).This register is reset by hardware to 00h.

Power Well:V_{PP}

Location:**All Banks**, Offset 0Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**						**BNK_SEL**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-2	**Reserved.**
1-0	**BNK_SEL (Bank Select).** This field selects the active bank for the upper offsets (10h-1Fh). **Bits** **1 0 Active Bank** 0 0: Bank 0: holds registers related to the Keyboard/Mouse Wake-up Detector (default) 0 1: Bank 1: holds registers related to the Power Active timers 1 0: Bank 2: holds registers related to sleep states and ACPI configuration 1 1: Bank 3: holds registers related to watchdog configuration and control

9.0 System Wake-Up Control (SWC) (Continued)

9.3.16 Keyboard Wake-Up Control Register (KBDWKCTL)

This register configures the keyboard events detected by the Keyboard/Mouse Wake-up Detector. It is reset by hardware to 00h.

Power Well:V_{PP}

Location:**Bank 0**, Offset 12h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**KBDMODE**	**Reserved**	**EVT3CFG**		**EVT2CFG**		**EVT1CFG**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**KBDMODE (Keyboard Mode Select).** This bit selects one of the keyboard wake-up modes for the Keyboard/Mouse Wake-up Detector. 0: Special Key Sequence or Password modes - configured by bits 3-0 of the PS2CTL register (default) 1: Power Management Key mode - configured by bits 5-0 of the KBDWKCTL register
6	**Reserved.**
5-4	**EVT3CFG (Keyboard Event 3 Configuration).** These bits configure the keyboard data sequence for Keyboard Event 3, which indicates that “PM Key 3” was pressed on the keyboard. The setting of the EVT3CFG field is relevant only if the Keyboard/Mouse Wake-up Detector is in Power Management Key mode (KBDMODE = 1). The keyboard data sequence used to detect Keyboard Event 3 is stored in registers PS2KEY6 and PS2KEY7, starting with PS2KEY6. **Bits** **5 4** **Sequence Length** 0 0: 0 bytes - Keyboard Event 3 disabled (default) 0 1: 1 byte (PS2KEY6) 1 0: 2 bytes (PS2KEY6, PS2KEY7) 1 1: Reserved
3-2	**EVT2CFG (Keyboard Event 2 Configuration).** These bits configure the keyboard data sequence for Keyboard Event 2, which indicates that “PM Key 2” was pressed on the keyboard. The setting of the EVT2CFG field is relevant only if the Keyboard/Mouse Wake-up Detector is in Power Management Key mode (KBDMODE = 1). The keyboard data sequence used to detect Keyboard Event 2 is stored in registers PS2KEY3 to PS2KEY5, starting with PS2KEY3. **Bits** **3 2** **Sequence Length** 0 0: 0 bytes - Keyboard Event 2 disabled (default) 0 1: 1 byte (PS2KEY3) 1 0: 2 bytes (PS2KEY3, PS2KEY4) 1 1: 3 bytes (PS2KEY3, PS2KEY4, PS2KEY5)
1-0	**EVT1CFG (Keyboard Event 1 Configuration).** These bits configure the keyboard data sequence for Keyboard Event 1, which indicates that “PM Key 1” was pressed on the keyboard. The setting of the EVT1CFG field is relevant only if the Keyboard/Mouse Wake-up Detector is in Power Management Key mode (KBDMODE = 1). The keyboard data sequence used to detect Keyboard Event 1 is stored in registers PS2KEY0 to PS2KEY2, starting with PS2KEY0. **Bits** **1 0** **Sequence Length** 0 0: 0 bytes - Keyboard Event 1 disabled (default) 0 1: 1 byte (PS2KEY0) 1 0: 2 bytes (PS2KEY0, PS2KEY1) 1 1: 3 bytes (PS2KEY0, PS2KEY1, PS2KEY2)

9.0 System Wake-Up Control (SWC) (Continued)

9.3.17 PS2 Protocol Control Register (PS2CTL)

This register configures the keyboard and mouse events detected by the Keyboard/Mouse Wake-up Detector. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **Bank 0**, Offset 13h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**DISPAR**	**MSEVCFG**			**KBEVCFG**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**DISPAR (Disable Parity Check).** This controls the parity checking of the keyboard and mouse data by the Keyboard/Mouse Wake-up Detector. 0: Enable parity check (default) 1: Disable parity check
6-4	**MSEVCFG (Mouse Event Configuration).** These bits configure the mouse data sequence for the Mouse event. Before setting them to a new value, these bits must be cleared by writing a value of 000b. **Bits** **6 5 4 Event Configuration** 0 0 0: Disable mouse wake-up detection (default) 0 0 1: Wake-up on any mouse movement or button click 0 1 0: Wake-up on left button click 0 1 1: Wake-up on left button double-click 1 0 0: Wake-up on right button click 1 0 1: Wake-up on right button double-click 1 1 0: Wake-up on any button single-click (left, right or middle) 1 1 1: Wake-up on any button double-click (left, right or middle)
3-0	**KBEVCFG (Keyboard Event Configuration).** These bits configure the keyboard data sequence for the Keyboard event, which indicates that any key or key sequence was pressed on the keyboard. The setting of the KBEVCFG field is relevant only if the Keyboard/Mouse Wake-up Detector is in either Special Key Sequence or Password mode (KBDMODE = 0). The keyboard data sequence used to detect a Keyboard Event is stored in registers PS2KEY0 to PS2KEY7, starting with PS2KEY0. Before setting them to a new value, the KBEVCFG field must be cleared by writing a value of 0000b. **Bits** **3 2 1 0 Event Configuration** 0 0 0 0: Disable keyboard wake-up detection (default) 0 0 0 1 to 0 1 1 1 } Special Key Sequence mode 2-8 PS/2 data bytes, “Make” and “Break” (including Shift and Alt keys) 1 0 0 0 to 1 1 1 1 } Password Enabled mode with 1-8 keys “Make” code (excluding Shift and Alt keys)

9.0 System Wake-Up Control (SWC) (Continued)

9.3.18 Keyboard Data Shift Register (KDSR)

When keyboard wake-up detection is enabled, this register stores the keyboard data shifted in from the keyboard during transmission. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **Bank 0**, Offset 16h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Keyboard Data**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Keyboard Data.**

9.3.19 Mouse Data Shift Register (MDSR)

When mouse wake-up detection is enabled, this register stores the mouse data shifted in from the mouse during transmission. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **Bank 0**, Offset 17h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**Mouse Data**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2-0	**Mouse Data.**

9.3.20 PS2 Keyboard Key Data 0 to 7 Registers (PS2KEY0 to PS2KEY7)

These eight registers (PS2KEY0-PS2KEY7) store the data bytes for Special Key Sequence or Password mode (KBDMODE = 0) or for Power Management Key mode (KBDMODE = 1) of the Keyboard/Mouse Wake-up Detector.

In Special Key Sequence or in Password modes, the keyboard data is stored as follows:

- PS2KEY0 register stores the data byte for the first key in the sequence.
- PS2KEY1 register stores the data byte for the second key in the sequence.
- PS2KEY2 - PS2KEY7 registers store data bytes for the third to eighth key in the sequence.

For keyboard data storage in Power Management Key mode, see Section 9.3.16 on page 193.

When one of these registers is set to 00h, it indicates that the value of the corresponding data byte is ignored (not compared). These registers are reset by hardware to 00h.

Power Well: V_{PP}

Location: **Bank 0**, Offset 18h to 1Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Data Byte of Key**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Data Byte of Key.**

9.0 System Wake-Up Control (SWC) (Continued)

9.3.21 V_{DD} Active Timer 0 Register (VDD_ON_TMR_0)

This register holds a copy of bits 0-7 of the V_{DD} Active Timer. Whenever the VDD_ON_TMR_0 register is read, the updating of all four VDD_ON_TMR_0 to VDD_ON_TMR_3 registers is stopped, freezing the count value. Therefore, this register must be read first. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **Bank 1**, Offset 10h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**V_{DD} Timer Data Bits 0-7**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**V_{DD} Timer Data, bits 0-7.** An LSBit is equivalent to 1 second of the V_{DD} power being active (On).

9.3.22 V_{DD} Active Timer 1 Register (VDD_ON_TMR_1)

This register holds a copy of bits 8-15 of the V_{DD} Active Timer. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **Bank 1**, Offset 11h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**V_{DD} Timer Data Bits 8-15**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**V_{DD} Timer Data, bits 8-15.**

9.3.23 V_{DD} Active Timer 2 Register (VDD_ON_TMR_2)

This register holds a copy of bits 16-23 of the V_{DD} Active Timer. It is reset by hardware to 00h.

Power Well:V_{PP}

Location:**Bank 1**, Offset 12h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**V_{DD} Timer Data Bits 16-23**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**V_{DD} Timer Data, bits 16-23.**

9.0 System Wake-Up Control (SWC) (Continued)

9.3.24 V_{DD} Active Timer 3 Register (VDD_ON_TMR_3)

This register holds a copy of bits 24-31 of the V_{DD} Active Timer. Whenever the VDD_ON_TMR_3 register is read, the updating of all four VDD_ON_TMR_0 to VDD_ON_TMR_3 registers is resumed. Therefore, this register must be read last. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **Bank 1**, Offset 13h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**V_{DD} Timer Data Bits 24-31**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**V_{DD} Timer Data, bits 24-31.**

9.3.25 V_{SB} Active Timer 0 Register (VSB_ON_TMR_0)

This register holds a copy of bits 0-7 of the V_{SB} Active Timer. Whenever the VSB_ON_TMR_0 register is read, the updating of all four VSB_ON_TMR_0 to VSB_ON_TMR_3 registers is stopped, freezing the count value. Therefore, this register must be read first. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **Bank 1**, Offset 14h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**V_{SB} Timer Data Bits 0-7**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**V_{SB} Timer Data, bits 0-7.** An LSBit is equivalent to 1 second of the V_{DD} power being active (On).

9.3.26 V_{SB} Active Timer 1 Register (VSB_ON_TMR_1)

This register holds a copy of bits 8-15 of the V_{SB} Active Timer. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **Bank 1**, Offset 15h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**V_{SB} Timer Data Bits 8-15**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**V_{SB} Timer Data, bits 8-15.**

9.0 System Wake-Up Control (SWC) (Continued)

9.3.27 V_{SB} Active Timer 2 Register (VSB_ON_TMR_2)

This register holds a copy of bits 16-23 of the V_{SB} Active Timer. It is reset by hardware to 00h.

Power Well:V_{PP}

Location:**Bank 1**, Offset 16h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**V_{SB} Timer Data Bits 16-23**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**V_{SB} Timer Data, bits 16-23.**

9.3.28 V_{SB} Active Timer 3 Register (VSB_ON_TMR_3)

This register holds a copy of bits 24-31 of the V_{SB} Active Timer. Whenever the VSB_ON_TMR_3 register is read, the updating of all four VSB_ON_TMR_0 to VSB_ON_TMR_3 registers is resumed. Therefore, this register must be read last. It is reset by hardware to 00h.

Power Well: V_{PP}

Location: **Bank 1**, Offset 17h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**V_{SB} Timer Data Bits 24-31**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**V_{SB} Timer Data, bits 24-31.**

9.0 System Wake-Up Control (SWC) (Continued)

9.3.29 Power Active Timers Control Register (PWTMRCTL)

This register controls the reset by software of the V_{DD} and V_{SB} Active Timers. It is reset by hardware to 00h.

Power Well: V_{PP}

Location: **Bank 1**, Offset 18h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCK_TMRRST**	**Reserved**				**VSB_TMR_RST**	**Reserved**	**VDD_TMR_RST**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W1S	**LOCK_TMRRST (Lock Timers Reset).** When set to 1, this bit locks the VSB_TMR_RST and VDD_TMR_RST bits by disabling the writing to them (including to the LOCK_TMRRST bit itself). Once set, this bit can be cleared either by V_{DD} Power-Up reset (or Hardware reset) or by V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKS bit in the ACBLKCTL register (**PC87413 and PC87417**). 0: R/W bits are enabled for write (default) 1: All bits are RO
6-3		**Reserved.**
2	R/W or RO	**VSB_TMR_RST (V_{SB} Active Timer Reset).** Writing ‘1’ to this bit resets the V_{SB} Active Timer (the timer is reset within 1 second following the write). This bit then returns to ‘0’ (read always returns ‘0’). 0: Inactive (default) 1: Reset the V_{SB} Active Timer
1		**Reserved.**
0	R/W or RO	**VDD_TMR_RST (V_{DD} Active Timer Reset).** Writing ‘1’ to this bit resets the V_{DD} Active Timer (the timer is reset within 1 second following the write). This bit then returns to ‘0’ (read always returns ‘0’). 0: Inactive (default) 1: Reset the V_{DD} Active Timer

9.3.30 S0 to S5 Sleep Type Encoding Registers (S0_SLP_TYP to S5_SLP_TYP)

These registers hold the system Sleep Type encoding for each sleep state: Working (G0/S0), Sleeping (G1/S1-S4) and Soft-off (G2/S5). The Sleep Type is defined by the SLP_TYPx field of the PM1b_CNT_HIGH register (see Section 9.4.7 on page 208). These registers are reset by hardware to 00h.

Power Well: V_{PP}

Location: **Bank 2**, Offset 10h to 15h

Type: R/W or RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**SLP_TYP_ENC**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2-0	**SLP_TYP_ENC (Sleep Type Encoding).** The value used by the system for the sleep state defined by the specific register. This value must always be set after V_{PP} reset (default = 000b). For sleep states not supported by the system, select an unused value.

9.0 System Wake-Up Control (SWC) (Continued)

9.3.31 Sleep State Configuration Register (SLP_ST_CFG)

This register controls the operation of the Sleep Type encoding. It is reset by hardware to 00h.

Power Well:V_{PP}

Location:**Bank 2**, Offset 16h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LOCK _SLP_ENC**	**Reserved**				**EXT_ST _SELECT**	**S3I _VDD_ON**	**S4 _SELECT**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W1S	**LOCK_SLP_ENC (Lock Sleep Type Encoding).** When set to 1, this bit locks the S0_SLP_TYP to S5_SLP_TYP and the SLP_ST_CFG registers by disabling the writing to them (including to the LOCK_SLP_ENC bit itself). Once set, this bit can be cleared either by V_{DD} Power-Up reset (or Hardware reset) or by V_{SB} Power-Up reset, according to the VSBLOCK bit in the ACBLKCTL register (see Section 6.3.4 on page 128). In addition, this bit is cleared by setting the UNLOCKS bit in the ACBLKCTL register (**PC87413 and PC87417**). 0: R/W bits are enabled for write (default) 1: All bits are RO
6-3		**Reserved.**
2	R/W or RO	**EXT_ST_SELECT (External Sleep State Select).** Selects the source of the current sleep states. 0: SLP_TYPx field in the PM1b_CNT_HIGH register (see Section 9.4.7 on page 208); (default) 1: $\overline{\text{SLPS3}}$ and $\overline{\text{SLPS5}}$ signals from an external ACPI controller (see also the EXTSTMUX bit in the SIOCF3 register, Section 3.7.4 on page 51)
1	R/W or RO	**S3I_VDD_ON (V_{DD}-On in S3I Select).** Selects the state of the V_{DD} power supply in the S3I current sleep state. 0: V_{DD} power supply Off (default) 1: V_{DD} power supply On
0	R/W or RO	**S4_SELECT (S4 Select).** Selects whether the sleep state S4 (if supported) is included in either S3I or S45 current sleep states. 0: S45 = S5 or S4 (default) 1: S3I = S3 or S4

9.0 System Wake-Up Control (SWC) (Continued)

9.3.32 ACPI Configuration Register (ACPI_CFG)

This register configures some of the ACPI wake-up events and the $\overline{\text{PWBTOUT}}$ operation mode. It is reset by hardware to 00h.

Power Well:V_{PP}

Location: **Bank 2**, Offset 17h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PWBTOUT _MODE**	**Reserved**				**RTC_EV _DIS**	**SLPBTN _EV_DIS**	**PWRBTN _EV_DIS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**PWBTOUT_MODE ($\overline{\text{PWBTOUT}}$ Mode).** When reset, this bit enables the pulsing of the $\overline{\text{PWBTOUT}}$ pin whenever an enabled wake-up event occurs. 0: $\overline{\text{PWBTOUT}}$ pulsed by (default): — $\overline{\text{PWBTIN}}$ activation — Crowbar condition — Wake-Up events 1: $\overline{\text{PWBTOUT}}$ pulsed by: — $\overline{\text{PWBTIN}}$ activation — Crowbar condition
6-3	**Reserved.**
2	**RTC_EV_DIS (RTC Event Disable).** Disables the RTC alarm event to the PM1b_STS_HIGH and PM1b_EN_HIGH, ACPI registers (RTC_STS = 0, RTC_EN = 0). However, the RTC_EVT_STS bit in the GPE1_STS_3 register and the RTC_EVT_EN bit in the GPE1_EN_3 register are not affected. 0: Disable event (default) 1: Enable the RTC alarm event
1	**SLPBTN_EV_DIS (Sleep Button Event Disable).** Enables the Sleep button pressing event to the PM1b_STS_HIGH and PM1b_EN_HIGH ACPI registers (SLPBTN_STS = 0, SLPBTN_EN = 0). The SLBT_EVT_STS bit in the GPE1_STS_2 register and the SLBT_EVT_EN bit in the GPE1_EN_2 register are not affected. 0: Disable event (default) 1: Enable Sleep button pressing event
0	**PWRBTN_EV_DIS (Power Button Event Disable).** Enables the Power button pressing event to the PM1b_STS_HIGH and PM1b_EN_HIGH ACPI registers (PWRBTN_STS = 0, PWRBTN_EN = 0). The PWBT_EVT_STS bit in the GPE1_STS_2 register and the PWBT_EVT_EN bit in the GPE1_EN_2 register are not affected. 0: Disable event (default) 1: Enable Power button pressing event

9.0 System Wake-Up Control (SWC) (Continued)

9.3.33 Watchdog Control Register (WDCTL)

This register contains the control bits for the watchdog. It is reset by hardware to 00h.

Power Well:V_{SB}

Location: **Bank 3**, Offset 10h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**SW_WD _TRG**	**Reserved**						**WDEN**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W	**SW_WD_TRG (Software Watchdog Trigger).** Writing ‘1’ to this bit triggers the watchdog to start a new count. This bit then returns to ‘0’ (read always returns ‘0’). 0: Inactive (default) 1: Triggers a new watchdog count
6-1		**Reserved.**
0	R/W1S	**WDEN (Watchdog Enable).** When set to 1, this bit enables the watchdog function. Once set, this bit can be cleared either by V_{DD} Power-Up reset, or by V_{SB} Power-Up reset. 0: Watchdog disabled (default) 1: Watchdog enabled

9.3.34 Watchdog Time-Out Register (WDTO)

This register contains the watchdog time-out period. It is reset by hardware to 01h.

Power Well:V_{SB}

Location: **Bank 3**, Offset 11h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Watchdog Time-Out Data**							
Reset	0	0	0	0	0	0	0	1

Bit	Description
7-0	**Watchdog Time-Out Data.** The load value for the watchdog down counter. The value defines the time-out in minutes for a span of: 1 to 255 minutes. The 00h value is reserved.

9.0 System Wake-Up Control (SWC) (Continued)

9.3.35 Watchdog Configuration Register (WDCFG)

This register contains the enable bits for the watchdog trigger sources. Reset all the bits before writing a new value to the WDTO register. It is reset by hardware to 00h.

Power Well:V_{SB}

Location:**Bank 3**, Offset 12h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SW_WD _TREN**	**Reserved**			**SER2_IRQ _TREN**	**SER1_IRQ _TREN**	**MS_IRQ _TREN**	**KBD_IRQ _TREN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**SW_WD_TREN (Software Watchdog Trigger Enable).** Enables the event of the software writing a ‘1’ to the SW_WD_TRG bit in the WDCTL register (see Section 9.3.33) to trigger the watchdog to start a new count. 0: Disable trigger (default) 1: Enable trigger by the SW_WD_TRG bit in the WDCTL register
6-4	**Reserved.**
3	**SER2_IRQ_TREN (Serial Port 2 IRQ, Watchdog Trigger Enable).** Enables an active IRQ from the Serial Port 2 to trigger the watchdog to start a new count. 0: Disable trigger (default) 1: Enable trigger by an active IRQ from the Serial Port 2
2	**SER1_IRQ_TREN (Serial Port 1 IRQ, Watchdog Trigger Enable).** Enables an active IRQ from the Serial Port 1 to trigger the watchdog to start a new count. 0: Disable trigger (default) 1: Enable trigger by an active IRQ from the Serial Port 1
1	**MS_IRQ_TREN (Mouse IRQ, Watchdog Trigger Enable).** Enables an active IRQ from the mouse interface section of the KBC module to trigger the watchdog to start a new count. 0: Disable trigger (default) 1: Enable trigger by an active IRQ from the mouse interface section of the KBC module
0	**KBD_IRQ_TREN (Keyboard IRQ, Watchdog Trigger Enable).** Enables an active IRQ from the keyboard interface section of the KBC module to trigger the watchdog to start a new count. 0: Disable trigger (default) 1: Enable trigger by an active IRQ from the keyboard interface section of the KBC module

9.0 System Wake-Up Control (SWC) (Continued)

9.4 ACPI REGISTERS

The ACPI registers are organized in three groups, all of which are V_{SB} powered. The offsets are related to the base address determined by the Base Address registers at indexes 62h - 67h in the SWC device configuration.

The PC8741x devices support the following ACPI fixed register groups:

- PM1 Event Group (block b), containing the PM1b_STS and PM1b_EN registers, each with a length of two bytes.
- PM1 Control Group (block b), containing the PM1b_CNT register with a length of 2 bytes.
- General-Purpose Event 1 Group, containing the GPE1_STS and GPE1_EN registers, each with a length of four bytes.

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from a specific register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

9.4.1 ACPI Register Map

The following table lists the ACPI registers. All these registers are V_{SB} powered.

Base Registers	Offset	Mnemonic	Register Name	Type	Power Well	Section
At index 62h, 63h	00h	PM1b_STS_LOW	PM1 Status Low Register	RO	V_{SB}	9.4.2
	01h	PM1b_STS_HIGH	PM1 Status High Register	R/W1C	V_{SB}	9.4.3
	02h	PM1b_EN_LOW	PM1 Enable Low Register	RO	V_{SB}	9.4.4
	03h	PM1b_EN_HIGH	PM1 Enable High Register	R/W	V_{SB}	9.4.5
At index 64h, 65h	00h	PM1b_CNT_LOW	PM1 Control Low Register	RO	V_{SB}	9.4.6
	01h	PM1b_CNT_HIGH	PM1 Control High Register	Varies per bit	V_{SB}	9.4.7
At index 66h, 67h	00h	GPE1_STS_0	General-Purpose Status 1 Register 0	R/W1C	V_{SB}	9.4.8
	01h	GPE1_STS_1	General-Purpose Status 1 Register 1	R/W1C	V_{SB}	9.4.9
	02h	GPE1_STS_2	General-Purpose Status 1 Register 2	R/W1C	V_{SB}	9.4.10
	03h	GPE1_STS_3	General-Purpose Status 1 Register 3	R/W1C	V_{SB}	9.4.11
	04h	GPE1_EN_0	General-Purpose Enable 1 Register 0	R/W	V_{SB}	9.4.12
	05h	GPE1_EN_1	General-Purpose Enable 1 Register 1	R/W	V_{SB}	9.4.13
	06h	GPE1_EN_2	General-Purpose Enable 1 Register 2	R/W	V_{SB}	9.4.14
	07h	GPE1_EN_3	General-Purpose Enable 1 Register 3	R/W	V_{SB}	9.4.15

9.0 System Wake-Up Control (SWC) (Continued)

9.4.2 PM1 Status Low Register (PM1b_STS_LOW)

This register contains the eight low bits of the PM1_STS register. The PC8741x devices contain the block 'b' instance of the PM1_STS register. This register belongs to the PM1 Event Group of the ACPI fixed-feature space registers.

PM1_STS register bits that are specified by the ACPI but not implemented in the PC8741x devices have a '0' value.

Power Well:V_{SB}

Location: Offset 00h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**GBL_STS**	**BM_STS**	**Reserved**			**TMR_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**GBL_STS (Global Lock Status).** Not implemented. Always at '0'.
4	**BM_STS (Bus Master Status).** Not implemented. Always at '0'.
3-1	**Reserved.**
0	**TMR_STS (PM Timer Status).** Not implemented. Always at '0'.

9.4.3 PM1 Status High Register (PM1b_STS_HIGH)

This register contains the eight high bits of the PM1_STS register. The PC8741x devices contain the block 'b' instance of the PM1_STS register. This register belongs to the PM1 Event Group of the ACPI fixed-feature space registers.

PM1_STS register bits that are specified by the ACPI but not implemented in the PC8741x devices have a '0' value. All the implemented status bits behave according to the Sticky Status Bit definition (the bit is set by the HIGH level of the hardware signal and is only cleared by the software writing '1' to it) in the ACPI Specification.

Power Well:V_{SB}

Location: Offset 01h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**WAK_STS**	**Reserved**			**Ignored**	**RTC_STS**	**SLPBTN_STS**	**PWRBTN_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**WAK_STS (Wake-up Event Status).** Indicates that a power management event, enabled to generate SCI, has occurred. This bit is set only if the system is in a sleep state (S1-S5). Writing '1' while the system is in the working state (S0), clears this bit; writing '0' is ignored. When the system is in a sleep state (S1-S5) and an enabled event is active, writing '1' does not clear the WAK_STS bit. 0: Inactive (default) 1: At least one event enabled to SCI was active while the system was in a sleep state (S1-S5), since this bit was last cleared
6-4	**Reserved.**
3	**Ignored.** The data written is ignored; the data read is undefined.

9.0 System Wake-Up Control (SWC) (Continued)

Bit	Description
2	**RTC_STS (RTC Event Status).** Indicates that an enabled RTC alarm has occurred. This bit is set by the RTC alarm becoming active. Writing '1' clears this bit and the RTC_EVT_STS bit in the GPE1_STS_3 register; writing '0' is ignored. This bit is forced to '0' when the RTC_EV_DIS bit in the ACPI_CFG register is reset to '0', ignoring any RTC alarm. 0: Inactive (default) 1: An RTC alarm has occurred
1	**SLPBTN_STS (Sleep Button Event Status).** Indicates that the Sleep button was pressed. This feature is compatible with the ACPI model for a two-button system. The $\overline{\text{SLBTIN}}$ signal is internally debounced. Writing '1' clears this bit and the SLBT_EVT_STS bit in the GPE1_STS_2 register; writing '0' is ignored. This bit is forced to '0' when the SLPBTN_EV_DIS bit in the ACPI_CFG register is reset to '0', ignoring any Sleep button event. 0: Inactive (default) 1: The Sleep button was pressed
0	**PWRBTN_STS (Power Button Event Status).** Indicates that the Power button was pressed. This feature is compatible with the ACPI model for both a single-button and a two-button system. The $\overline{\text{PWBTIN}}$ signal is internally debounced. Writing '1' clears this bit and the PWBT_EVT_STS bit in the GPE1_STS_2 register; writing '0' is ignored. This bit is forced to '0' when the PWRBTN_EV_DIS bit in the ACPI_CFG register is reset to '0', ignoring any Power button event. This bit is also cleared in Legacy Power Button mode (LEGACY_PWBT = 1 in PWONCTL) when V_{DD} is turned off by pressing the Power button. 0: Inactive (default) 1: The Power button was pressed

9.4.4 PM1 Enable Low Register (PM1b_EN_LOW)

This register contains the eight low bits of the PM1_EN register. The PC8741x devices contain the block 'b' instance of the PM1_EN register. This register belongs to the PM1 Event Group of the ACPI fixed-feature space registers.

PM1_EN register bits that are specified by the ACPI but not implemented in the PC8741x devices have a '0' value.

Power Well:V_{SB}

Location: Offset 02h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**GBL_EN**	**Reserved**				**TMR_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved.**
5	**GBL_EN (Global Lock Enable).** Not implemented. Always at '0'.
4-1	**Reserved.**
0	**TMR_EN (PM Timer Enable).** Not implemented. Always at '0'.

9.0 System Wake-Up Control (SWC) (Continued)

9.4.5 PM1 Enable High Register (PM1b_EN_HIGH)

This register contains the eight high bits of the PM1_EN register. The PC8741x devices contain the block 'b' instance of the PM1_EN register. This register belongs to the PM1 Event Group of the ACPI fixed-feature space registers.

PM1_EN register bits that are specified by the ACPI but not implemented in the PC8741x devices have a '0' value. All the implemented enable bits behave according to the Enable Bit definition (the bit is read/write by software) in the ACPI Specification.

Power Well:V_{SB}

Location: Offset 03h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**RTC_EN**	**SLPBTN_EN**	**PWRBTN_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2	**RTC_EN (RTC Event Enable).** Enables the RTC alarm to generate a power management interrupt ($\overline{\text{SIOSCI}}$). This bit is forced to '0' when the RTC_EV_DIS bit in the ACPI_CFG register is reset to '0', disabling any RTC alarm event. 0: Disable SCI (default) 1: Enable SCI from RTC alarm
1	**SLPBTN_EN (Sleep Button Event Enable).** Enables Sleep button pressing to generate a power management interrupt ($\overline{\text{SIOSCI}}$). This bit is forced to '0' when the SLPBTN_EV_DIS bit in the ACPI_CFG register is reset to '0', disabling any Sleep button event. 0: Disable SCI (default) 1: Enable SCI from Sleep button pressing
0	**PWRBTN_EN (Power Button Event Enable).** Enables Power button pressing to generate a power management interrupt ($\overline{\text{SIOSCI}}$) when the system is in the active state (S0). This bit does not influence SCI generation when the system is in a sleep state (S1-S5). This bit is forced to '0' when the PWRBTN_EV_DIS bit in the ACPI_CFG register is reset to '0', disabling any Power button event. 0: Disable SCI (default) 1: Enable SCI from Power button pressing

9.0 System Wake-Up Control (SWC) (Continued)

9.4.6 PM1 Control Low Register (PM1b_CNT_LOW)

This register contains the eight low bits of the PM1_CNT register. The PC8741x devices contain the block ‘b’ instance of the PM1_CNT register. This register belongs to the PM1 Control Group of the ACPI fixed-feature space registers.

PM1_CNT register bits that are specified by the ACPI but not implemented in the PC8741x devices have a ‘0’ value.

Power Well:V_{SB}

Location:Offset 00h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**GBL_RLS**	**BM_RLD**	**SCI_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved.**
2	**GBL_RLS (Global Lock Release).** Not implemented. Always at ‘0’.
1	**BM_RLD (Bus Master Request Control).** Not implemented. Always at ‘0’.
0	**SCI_EN (SCI Enable).** Not implemented. Always at ‘0’.

9.4.7 PM1 Control High Register (PM1b_CNT_HIGH)

This register contains the eight high bits of the PM1_CNT register. The PC8741x devices contain the block ‘b’ instance of the PM1_CNT register. This register belongs to the PM1 Control Group of the ACPI fixed-feature space registers.

PM1_CNT register bits that are specified by the ACPI but not implemented in the PC8741x devices have a ‘0’ value. All the implemented control bits behave according to the Control bit definition (the bit is read/write by software) and Write-Only Control Bit definition (the bit is written by software; when read, it returns 0) in the ACPI Specification.

Power Well:V_{SB}

Location: Offset 01h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**SLP_EN**	**SLP_TYPx**			**Ignored**	**Reserved**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7-6	-	**Reserved.**
5	WO	**SLP_EN (Sleep Enable).** Setting this bit causes the PC8741x device to accept the value of SLP_TYPx as the system state code. This bit may be set in the same write cycle with a new SLP_TYPx value. 0: Inactive (default) 1: Update the system state code from the SLP_TYPx value

9.0 System Wake-Up Control (SWC) (Continued)

Bit	Type	Description
4-2	R/W	**SLP_TYPx (Sleep Type).** This field defines the system sleep state type (encoded). The states supported by the PC8741x devices are: Working (G0/S0), Sleeping (G1/S1-S4) and Soft-off (G2/S5). The encoding of the sleep state is programmed through the V_{PP}-powered registers S0_SLP_TYP to S5_SLP_TYP. **Bits** **2 1 0 Function** 0 0 0: Encoded 3-bit value for state S*n* (*n* = 0-5); (default) x x x: Encoded 3-bit value (except 000b) for the remaining 5 sleep states: S*n* (*n* = 0-5)
1	-	**Ignored.** The data written is ignored; the data read is undefined.
0	-	**Reserved.**

9.4.8 General-Purpose Status 1 Register 0 (GPE1_STS_0)

This register contains bits 0-7 of the GPE1_STS register. This register belongs to the General-Purpose Event 1 Group of the ACPI fixed-feature space registers.

The status bits behave according to the Sticky Status Bit definition (the bit is set by the HIGH level of the hardware signal and is only cleared by the software writing ‘1’ to it) in the ACPI Specification.

Power Well:V_{SB}

Location: Offset 00h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**GPIOE17 _STS**	**GPIOE16 _STS**	**GPIOE15 _STS**	**GPIOE14 _STS**	**GPIOE13 _STS**	**GPIOE12 _STS**	**GPIOE11 _STS**	**GPIOE10 _STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIOE17_STS (GPIOE17 Event Status).** Indicates that an active event has been detected at pin 7 of the GPIOE Port 1. The event has programmable polarity and the debounce option (see Section 7.3.1 on page 137). The bit is set by an active level at the GPIOE17 pin. Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Inactive since last cleared (default) 1: An active event has occurred
6-0	**GPIOE16_STS to GPIOE10_STS (GPIOE16 to GPIOE10 Event Status).** Same as above for pins 6-0 of the GPIOE Port 1.

9.4.9 General-Purpose Status 1 Register 1 (GPE1_STS_1)

This register contains bits 8-15 of the GPE1_STS register. This register belongs to the General-Purpose Event 1 Group of the ACPI fixed-feature space registers.

The status bits behave according to the Sticky Status Bit definition (the bit is set by the HIGH level of the hardware signal and is only cleared by the software writing ‘1’ to it) in the ACPI Specification.

Power Well:V_{SB}

Location: Offset 01h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**GPIOE47 _STS**	**GPIOE46 _STS**	**GPIOE45 _STS**	**GPIOE44 _STS**	**GPIOE43 _STS**	**GPIOE42 _STS**	**GPIOE41 _STS**	**GPIOE40 _STS**
Reset	0	0	0	0	0	0	0	0

9.0 System Wake-Up Control (SWC) (Continued)

Bit	Description
7	**GPIOE47_STS (GPIOE47 Event Status).** Indicates that an active event has been detected at pin 7 of the GPIOE Port 4. The event has programmable polarity and the debounce option (see Section 7.3.1 on page 137). The bit is set by an active level at the GPIOE47 pin. Writing '1' clears this bit; writing '0' is ignored. 0: Inactive since last cleared (default) 1: An active event has occurred
6-0	**GPIOE46_STS to GPIOE40_STS (GPIOE46 to GPIOE40 Event Status).** Same as above for pins 6-0 of the GPIOE Port 4.

9.4.10 General-Purpose Status 1 Register 2 (GPE1_STS_2)

This register contains bits 16-23 of the GPE1_STS register. This register belongs to the General-Purpose Event 1 Group of the ACPI fixed-feature space registers.

The status bits behave according to the Sticky status bit definition (the bit is set by the HIGH level of the hardware signal and is only cleared by the software writing '1' to it) in the ACPI Specification.

Power Well:V_{SB}

Location: Offset 02h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**PWBT_EVT_STS**	**SLBT_EVT_STS**	**KBD_EVT3_STS**	**KBD_EVT2_STS**	**KBD_EVT1_STS**	**MS_EVT_STS**	**RI2_EVT_STS**	**RI1_EVT_STS**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**PWBT_EVT_STS (Power Button Event Status).** Indicates that the Power button was pressed. This bit is similar to the PWRBTN_STS bit in the PM1b_STS_HIGH register. The $\overline{\text{PWBTIN}}$ signal is internally debounced. Writing '1' clears this bit and the PWRBTN_STS bit in the PM1b_STS_HIGH register; writing '0' is ignored. This bit is also cleared in Legacy Power Button mode (LEGACY_PWBT = 1 in PWONCTL) when V_{DD} is turned off by pressing the Power button. 0: Inactive (default) 1: The Power button was pressed
6	**SLBT_EVT_STS (Sleep Button Event Status).** Indicates that the Sleep button was pressed. This bit is similar to the SLPBTN_STS bit in the PM1b_STS_HIGH register. The $\overline{\text{SLBTIN}}$ signal is internally debounced. Writing '1' clears this bit and the SLPBTN_STS bit in the PM1b_STS_HIGH register; writing '0' is ignored. 0: Inactive (default) 1: The Sleep button was pressed
5	**KBD_EVT3_STS (Keyboard Event 3 Status).** Indicates that "PM Key 3" was pressed and that the event was identified by the Keyboard/Mouse Wake-up Detector. This bit is set only if the Keyboard/Mouse Wake-up Detector is in the Power Management Key mode (see Section 9.3.16 on page 193). Writing '1' clears this bit; writing '0' is ignored. 0: Inactive since last cleared (default) 1: The "PM Key 3" key was pressed on the keyboard
4	**KBD_EVT2_STS (Keyboard Event 2 Status).** Indicates that "PM Key 2" was pressed and that the event was identified by the Keyboard/Mouse Wake-up Detector. This bit is set only if the Keyboard/Mouse Wake-up Detector is in the Power Management Key mode (see Section 9.3.16 on page 193). Writing '1' clears this bit; writing '0' is ignored. 0: Inactive since last cleared (default) 1: The "PM Key 2" key was pressed on the keyboard

9.0 System Wake-Up Control (SWC) (Continued)

Bit	Description
3	**KBD_EVT1_STS (Keyboard Event 1 Status).** This bit indicates that a keyboard event occurred and was identified by the Keyboard/Mouse Wake-up Detector. The event type depends on the selected operation mode for the Keyboard/Mouse Wake-up Detector (see Sections 9.3.16 and 9.3.17 on pages 193ff.): • Pressing any key or a sequence of special keys in Special Key Sequence mode. • Pressing a sequence of keys in Password mode. • Pressing the “PM Key 1” in Power Management Key mode. Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Inactive since last cleared (default) 1: A keyboard event occurred
2	**MS_EVT_STS (Mouse Event Status).** Indicates that a mouse event occurred and was identified by the Keyboard/Mouse Wake-up Detector (see Section 9.3.17 on page 194). Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Inactive since last cleared (default) 1: A mouse event occurred
1	**RI2_EVT_STS ($\overline{\text{RI2}}$ Event Status).** Indicates that a telephone ring signal was received at Serial Port 2 and the event was identified by the RI Wake-up Detector. This bit is set by a high-to-low transition at the $\overline{\text{RI2}}$ pin (see Section 9.2.1 on page 162). Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Inactive since last cleared (default) 1: A telephone ring signal was received at the Serial Port 2
0	**RI1_EVT_STS ($\overline{\text{RI1}}$ Event Status).** Indicates that a telephone ring signal was received at Serial Port 1 and the event was identified by the RI Wake-up Detector. This bit is set by a high-to low transition at the $\overline{\text{RI1}}$ pin (see Section 9.2.1 on page 162). Writing ‘1’ clears this bit; writing ‘0’ is ignored. 0: Inactive since last cleared (default) 1: A telephone ring signal was received at the Serial Port 1

9.4.11 General-Purpose Status 1 Register 3 (GPE1_STS_3)

This register contains bits 24-31 of the GPE1_STS register. This register belongs to the General-Purpose Event 1 Group of the ACPI fixed-feature space registers.

The status bits behave according to the Sticky Status Bit definition (the bit is set by the HIGH level of the hardware signal and is only cleared by the software writing ‘1’ to it) in the ACPI Specification.

Power Well:V_{SB}

Location: Offset 03h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**SW_OFF_STS**	**SW_ON_STS**	**WDO_EVT_STS**	**MOD_IRQ_STS**	**MS_IRQ_STS**	**KBD_IRQ_STS**	**P12_EVT_STS**	**RTC_EVT_STS**
Reset	0	0	0	0	0	0	0	0

9.0 System Wake-Up Control (SWC) (Continued)

Bit	Description
7	**SW_OFF_STS (Software Off Event Status).** Indicates that the software wrote a '1' to the SW_OFF_CTL bit in the SWC_CTL register to request a V_{DD} power off sequence. Writing '1' clears this bit; writing '0' is ignored. 0: Inactive since last cleared (default) 1: '1' was written to the SW_OFF_CTL bit in the SWC_CTL register
6	**SW_ON_STS (Software On Event Status).** Indicates that the software wrote a '1' to the SW_ON_CTL bit in the SWC_CTL register to request a V_{DD} Power On sequence. When the V_{DD} power is off, the SW_ON_CTL bit can be written only through the ACCESS.bus (**PC87413 and PC87417**). Writing '1' clears this bit; writing '0' is ignored. 0: Inactive since last cleared (default) 1: '1' was written to the SW_ON_CTL bit in the SWC_CTL register
5	**WDO_EVT_STS (Watchdog Event Status).** Indicates that watchdog time-out has occurred. Writing '1' clears this bit; writing '0' is ignored. 0: Inactive (default) 1: A watchdog time-out has occurred
4	**MOD_IRQ_STS (Modules IRQ Event Status).** Indicates that an IRQ was generated by one of the Legacy modules (FDC, Parallel Port, Serial Port 1 and 2) or by the XIRQ pin (**PC87416 and PC87417**). For Legacy modules IRQ, this bit is set only if the IRQ is enabled for wake-up (bit 4 of the Standard configuration register at index 70h) and the related module is active (see Section 3.2.3 on page 40). For the XIRQ pin, this bit is set only if XIRQ is enabled for wake-up by setting both the IRQEN and the PWUREN bits in the XIRQC register (see Section 5.4.4 on page 110) to '1'. Writing '1' clears this bit; writing '0' is ignored. 0: Inactive since last cleared (default) 1: An enabled IRQ, from one of the Legacy modules or from the XIRQ pin, is active
3	**MS_IRQ_STS (Mouse IRQ Event Status).** Indicates that an IRQ was generated by the mouse interface section of the KBC module. This bit is set only if the IRQ is enabled for wake-up (bit 4 of the Mouse Logical Device configuration register at index 70h) and the KBC module is active (see Section 3.2.3 on page 40). Writing '1' clears this bit; writing '0' is ignored. 0: Inactive since last cleared (default) 1: An enabled IRQ, from the mouse interface section of the KBC module, is active
2	**KBD_IRQ_STS (Keyboard IRQ Event Status).** Indicates that an IRQ was generated by the keyboard interface section of the KBC module. This bit is set only if the IRQ is enabled for wake-up (bit 4 of the Keyboard Logical Device configuration register at index 70h) and the KBC module is active (see Section 3.2.3 on page 40). Writing '1' clears this bit; writing '0' is ignored. 0: Inactive since last cleared (default) 1: An enabled IRQ, from the keyboard interface section of the KBC module, is active
1	**P12_EVT_STS (Port P12 Event Status).** Indicates that an active high signal was generated by the KBC module, at the P12 pin. This bit is set only if the KBC module is active (see Section 3.2.3 on page 40). Writing '1' clears this bit; writing '0' is ignored. 0: Inactive since last cleared (default) 1: An active high signal at the P12 pin was generated by the KBC module
0	**RTC_EVT_STS (RTC Alarm Event Status).** Indicates that an enabled RTC alarm has occurred. This bit is similar to the RTC_STS bit in the PM1b_STS_HIGH register. Writing '1' clears this bit and the RTC_STS bit in the PM1b_STS_HIGH register; writing '0' is ignored. 0: Inactive (default) 1: An RTC alarm has occurred

9.0 System Wake-Up Control (SWC) (Continued)

9.4.12 General-Purpose Enable 1 Register 0 (GPE1_EN_0)

This register contains bits 0-7 of the GPE1_EN register. This register belongs to the General-Purpose Event 1 Group of the ACPI fixed-feature space registers.

The enable bits behave according to the Enable Bit definition (the bit is read/write by software) in the ACPI Specification.

Power Well: V_{SB}

Location: Offset 04h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**GPIOE17 _EN**	**GPIOE16 _EN**	**GPIOE15 _EN**	**GPIOE14 _EN**	**GPIOE13 _EN**	**GPIOE12 _EN**	**GPIOE11 _EN**	**GPIOE10 _EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIOE17_EN (GPIOE17 Event Enable).** Enables an active event at pin 7 of the GPIOE Port 1 to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI
6-0	**GPIOE16_EN to GPIOE10_EN (GPIOE16 to GPIOE10 Event Enable).** Same as above for pins 6-0 of GPIOE Port 1.

9.4.13 General-Purpose Enable 1 Register 1 (GPE1_EN_1)

This register contains bits 8-15 of the GPE1_EN register. This register belongs to the General-Purpose Event 1 Group of the ACPI fixed-feature space registers.

The enable bits behave according to the Enable Bit definition (the bit is read/write by software) in the ACPI Specification.

Power Well: V_{SB}

Location: Offset 05h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**GPIOE47 _EN**	**GPIOE46 _EN**	**GPIOE45 _EN**	**GPIOE44 _EN**	**GPIOE43 _EN**	**GPIOE42 _EN**	**GPIOE41 _EN**	**GPIOE40 _EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIOE47_EN (GPIOE47 Event Enable).** Enables an active event at pin 7 of the GPIOE Port 4 to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI
6-0	**GPIOE46_EN to GPIOE40_EN (GPIOE46 to GPIOE40 Event Enable).** Same as above for pins 6-0 of the GPIOE Port 4.

9.0 System Wake-Up Control (SWC) (Continued)

9.4.14 General-Purpose Enable 1 Register 2 (GPE1_EN_2)

This register contains bits 16-23 of the GPE1_EN register. This register belongs to the General-Purpose Event 1 Group of the ACPI fixed-feature space registers.

The enable bits behave according to the Enable Bit definition (the bit is read/write by software) in the ACPI Specification.

Power Well: V_{SB}

Location: Offset 06h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**PWBT_EVT_EN**	**SLBT_EVT_EN**	**KBD_EVT3_EN**	**KBD_EVT2_EN**	**KBD_EVT1_EN**	**MS_EVT_EN**	**RI2_EVT_EN**	**RI1_EVT_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**PWBT_EVT_EN (Power Button Event Enable).** Enables Power button pressing to generate a power management interrupt ($\overline{\text{SIOSCI}}$). This bit is similar to the PWRBTN_EN bit in the PM1b_EN_HIGH register. It should be enabled only if the system does not support the PM1b_EVT register block. 0: Disable SCI (default) 1: Enable SCI from Power button pressing
6	**SLBT_EVT_EN (Sleep Button Event Enable).** Enables Sleep button pressing to generate a power management interrupt ($\overline{\text{SIOSCI}}$). This bit is similar to the SLPBTN_EN bit in the PM1b_EN_HIGH register. It should be enabled only if the system does not support the PM1b_EVT register block. 0: Disable SCI (default) 1: Enable SCI from Sleep button pressing
5	**KBD_EVT3_EN (Keyboard Event 3 Enable).** Enables the event of pressing “PM Key 3” (on the keyboard) to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from pressing the “PM Key 3” on the keyboard
4	**KBD_EVT2_EN (Keyboard Event 2 Enable).** Enables the event of pressing “PM Key 2” (on the keyboard) to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from pressing the “PM Key 2” on the keyboard
3	**KBD_EVT1_EN (Keyboard Event 1 Enable).** Enables the event of pressing any key, key sequence or “PM Key 1” (on the keyboard) to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from pressing a sequence of keys or the “PM Key 1” on the keyboard
2	**MS_EVT_EN (Mouse Event Enable).** Enables a mouse event identified by the Keyboard/Mouse Wake-up Detector to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from mouse event identified by the Keyboard/Mouse Wake-up Detector
1	**RI2_EVT_EN ($\overline{\text{RI2}}$ Event Enable).** Enables a telephone ring received at the Serial Port 2 event, and identified by the RI Wake-up Detector, to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from telephone ring event received at the Serial Port 2
0	**RI1_EVT_EN ($\overline{\text{RI1}}$ Event Enable).** Enables a telephone ring received at the Serial Port 1 event, and identified by the RI Wake-up Detector, to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable event (default) 1: Enable SCI from telephone ring event received at the Serial Port 1

9.0 System Wake-Up Control (SWC) (Continued)

9.4.15 General-Purpose Enable 1 Register 3 (GPE1_EN_3)

This register contains bits 24-31 of the GPE1_EN register. This register belongs to the General-Purpose Event 1 Group of the ACPI fixed-feature space registers.

The enable bits behave according to the Enable Bit definition (the bit is read/write by software) in the ACPI Specification.

Power Well:V_{SB}

Location:Offset 07h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SW_OFF_EN**	**SW_ON_EN**	**WDO_EVT_EN**	**MOD_IRQ_EN**	**MS_IRQ_EN**	**KBD_IRQ_EN**	**P12_EVT_EN**	**RTC_EVT_EN**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**SW_OFF_EN (Software Off Event Enable).** Enables the event of the software writing a ‘1’ to the SW_OFF_CTL bit in the SWC_CTL register to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from the software writing a ‘1’ to the SW_OFF_CTL bit in the SWC_CTL register
6	**SW_ON_EN (Software On Event Enable).** Enables the event of the software writing a ‘1’ to the SW_ON_CTL bit in the SWC_CTL register to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from the software writing a ‘1’ to the SW_ON_CTL bit in the SWC_CTL register
5	**WDO_EVT_EN (Watchdog Event Enable).** Enables an watchdog time-out event to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from watchdog time-out
4	**MOD_IRQ_EN (Modules IRQ Event Enable).** Enables an active IRQ from one of the Legacy modules or from the XIRQ pin (**PC87413 and PC87417**) to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI by an active IRQ from one of the Legacy modules or from the XIRQ pin
3	**MS_IRQ_EN (Mouse IRQ Event Enable).** Enables an IRQ generated by the mouse interface section of the KBC module to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from an IRQ generated by the mouse interface section of the KBC module
2	**KBD_IRQ_EN (Keyboard IRQ Event Enable).** Enables an IRQ generated by the keyboard interface section of the KBC module to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from an IRQ generated by the keyboard interface section of the KBC module
1	**P12_EVT_EN (Port P12 Event Enable).** Enables an IRQ by an active high signal generated at the P12 pin to generate a power management interrupt ($\overline{\text{SIOSCI}}$). 0: Disable SCI (default) 1: Enable SCI from an active high signal generated at the P12 pin
0	**RTC_EVT_EN (RTC Alarm Event Enable).** Enables an RTC alarm to generate a power management interrupt ($\overline{\text{SIOSCI}}$). This bit is similar to the RTC_EN bit in the PM1b_EN_HIGH register. It should be enabled only if the system does not support the PM1b_EVT register block. 0: Disable SCI (default) 1: Enable SCI from RTC alarm

9.0 System Wake-Up Control (SWC) (Continued)

9.5 SYSTEM WAKE-UP CONTROL REGISTERS BITMAP

Table 51. Banks 0, 1, 2 and 3 - Common Register Map

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	WK_EVT_SEL	Reserved			WKUPSEL				
01h	WK_ST_EN	Reserved				PWBT_EN _S3I	PWBT_EN _S45	ONCTL _EN_S3I	ONCTL _EN_S45
02h	GPE1_2IRQ _LOW	PWBT_ EVT_2IRQ	SLBT_ EVT_2IRQ	KBD_EVT3 _2IRQ	KBD_EVT2 _2IRQ	KBD_EVT1 _2IRQ	MS_EVT _2IRQ	RI2_EVT _2IRQ	RI1_EVT _2IRQ
03h	GPE1_2IRQ _HIGH	SW_OFF _2IRQ	SW_ON _2IRQ	Reserved				P12_EVT _2IRQ	Reserved
04h	GPE1_2SMI _LOW	PWBT_ EVT_2SMI	SLBT_ EVT_2SMI	KBD_EVT3 _2SMI	KBD_EVT2 _2SMI	KBD_EVT1 _2SMI	MS_EVT _2SMI	RI2_EVT _2SMI	RI1_EVT _2SMI
05h	GPE1_2SMI _HIGH	SW_OFF _2SMI	SW_ON _2SMI	WDO_EVT _2SMI	Reserved				RTC_EVT _2SMI
06h	SWCFDIS	Reserved		KBDDIS	MSDIS	SER1DIS	SER2DIS	PARPDIS	FDCDIS
07h	SWCTRIS	Reserved			KBMSTRIS	SER1TRIS	SER2TRIS	PARPTRIS	FDCTRIS
08h	SWC_CTL	SW_OFF _CTL	SW_ON _CTL	PWB_OVR _STS	CROWBAR _STS	Reserved			SWAP _KBMS
09h	PWONCTL	WAS _PFAIL	LAST _ONCTL	RESUME_MD		LEGACY _PWBT	CRBAR_TOUT		
0Ah	LEDCTL	Reserved		LEDCFG	LEDPOL	Reserved		LEDMOD	
0Bh	LEDBLNK	Reserved	LED2BLNK			Reserved	LED1BLNK		
0Ch-0Dh	Reserved								
0Eh	BIOSGPR	General-Purpose Scratch							
0Fh	BANKSEL	Reserved						BNK_SEL	

9.0 System Wake-Up Control (SWC) (Continued)

Table 52. Bank 0 - Keyboard/Mouse Wake-Up Detector Register Map

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
10h-11h	Reserved								
12h	KBDWKCTL	KBDMODE	Reserved	EVT3CFG		EVT2CFG		EVT1CFG	
13h	PS2CTL	DISPAR	MSEVCFG			KBEVCFG			
14h-15h	Reserved								
16h	KDSR	Keyboard Data							
17h	MDSR	Reserved					Mouse Data		
18h	PS2KEY0	Data Byte of Key							
19h	PS2KEY1	Data Byte of Key							
1Ah	PS2KEY2	Data Byte of Key							
1Bh	PS2KEY3	Data Byte of Key							
1Ch	PS2KEY4	Data Byte of Key							
1Dh	PS2KEY5	Data Byte of Key							
1Eh	PS2KEY6	Data Byte of Key							
1Fh	PS2KEY7	Data Byte of Key							

Table 53. Bank 1 - Power Active Timers Register Map

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
10h	VDD_ON_TMR_0	V_{DD} Timer Data Bits 0-7							
11h	VDD_ON_TMR_1	V_{DD} Timer Data Bits 8-15							
12h	VDD_ON_TMR_2	V_{DD} Timer Data Bits 16-23							
13h	VDD_ON_TMR_3	V_{DD} Timer Data Bits 24-31							
14h	VSB_ON_TMR_0	V_{SB} Timer Data Bits 0-7							
15h	VSB_ON_TMR_1	V_{SB} Timer Data Bits 8-15							
16h	VSB_ON_TMR_2	V_{SB} Timer Data Bits 16-23							
17h	VSB_ON_TMR_3	V_{SB} Timer Data Bits 24-31							
18h	PWTMRCTL	LOCK_TMRRST	Reserved				VSB_TMR_RST	Reserved	VDD_TMR_RST
19h-1Fh	Reserved								

9.0 System Wake-Up Control (SWC) (Continued)

Table 54. Bank 2 - Sleep States and ACPI Configuration Register Map

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
10h	S0_SLP_TYP	Reserved					SLP_TYP_ENC		
11h	S1_SLP_TYP	Reserved					SLP_TYP_ENC		
12h	S2_SLP_TYP	Reserved					SLP_TYP_ENC		
13h	S3_SLP_TYP	Reserved					SLP_TYP_ENC		
14h	S4_SLP_TYP	Reserved					SLP_TYP_ENC		
15h	S5_SLP_TYP	Reserved					SLP_TYP_ENC		
16h	SLP_ST_CFG	LOCK_ SLP_ENC	Reserved				EXT_ST _SELECT	S3I _VDD_ON	S4 _SELECT
17h	ACPI_CFG	PWBTOUT _MODE	Reserved				RTC_EV _DIS	SLPBTN _EV_DIS	PWRBTN _EV_DIS
18h-1Fh	Reserved								

Table 55. Bank 3 - Watchdog Register Map

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
10h	WDCTL	SW_WD _TRG	Reserved						WDEN
11h	WDTO	Watchdog Time-Out Data							
12h	WDCFG	SW_WD _TREN	Reserved			SER2_IRQ _TREN	SER1_IRQ _TREN	MS_IRQ _TREN	KBD_IRQ _TREN
13h-1Fh	Reserved								

Table 56. ACPI Register Map with Base Address at Index 62h, 63h

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	PM1b_STS _LOW	Reserved		GBL_STS	BM_STS	Reserved			TMR_STS
01h	PM1b_STS _HIGH	WAK_STS	Reserved			Ignored	RTC_STS	SLPBTN _STS	PWRBTN _STS
02h	PM1b_EN_ LOW	Reserved		GBL_EN	Reserved				TMR_EN
03h	PM1b_EN_ HIGH	Reserved					RTC_EN	SLPBTN _EN	PWRBTN _EN

9.0 System Wake-Up Control (SWC) (Continued)

Table 57. ACPI Register Map with Base Address at Index 64h, 65h

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	PM1b_CNT_LOW	Reserved					GBL_RLS	BM_RLD	SCI_EN
01h	PM1b_CNT_HIGH	Reserved		SLP_EN	SLP_TYPx			Ignored	Reserved

Table 58. ACPI Register Map with Base Address at Index 66h, 67h

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	GPE1_STS_0	GPIOE17_STS	GPIOE16_STS	GPIOE15_STS	GPIOE14_STS	GPIOE13_STS	GPIOE12_STS	GPIOE11_STS	GPIOE10_STS
01h	GPE1_STS_1	GPIOE47_STS	GPIOE46_STS	GPIOE45_STS	GPIOE44_STS	GPIOE43_STS	GPIOE42_STS	GPIOE41_STS	GPIOE40_STS
02h	GPE1_STS_2	PWBT_EVT_STS	SLBT_EVT_STS	KBD_EVT3_STS	KBD_EVT2_STS	KBD_EVT1_STS	MS_EVT_STS	RI2_EVT_STS	RI1_EVT_STS
03h	GPE1_STS_3	SW_OFF_STS	SW_ON_STS	WDO_EVT_STS	MOD_IRQ_STS	MS_IRQ_STS	KBD_IRQ_STS	P12_EVT_STS	RTC_EVT_STS
04h	GPE1_EN_0	GPIOE17_EN	GPIOE16_EN	GPIOE15_EN	GPIOE14_EN	GPIOE13_EN	GPIOE12_EN	GPIOE11_EN	GPIOE10_EN
05h	GPE1_EN_1	GPIOE47_EN	GPIOE46_EN	GPIOE45_EN	GPIOE44_EN	GPIOE43_EN	GPIOE42_EN	GPIOE41_EN	GPIOE40_EN
06h	GPE1_EN_2	PWBT_EVT_EN	SLBT_EVT_EN	KBD_EVT3_EN	KBD_EVT2_EN	KBD_EVT1_EN	MS_EVT_EN	RI2_EVT_EN	RI1_EVT_EN
07h	GPE1_EN_3	SW_OFF_EN	SW_ON_EN	WDO_EVT_EN	MOD_IRQ_EN	MS_IRQ_EN	KBD_IRQ_EN	P12_EVT_EN	RTC_EVT_EN

10.0 Legacy Functional Blocks

This chapter briefly describes the following blocks, which provide legacy device functions:

- Floppy Disk Controller (FDC).
- Parallel Port (PP).
- Serial Ports 1 and 2 (SP1 and SP2).
- Keyboard and Mouse Controller (KBC).

The description of each Legacy block includes the sections listed below. For details on the general implementation of each legacy block, see the *SuperI/O Legacy Functional Blocks* datasheet.

- General Description.
- Register Map table(s).
- Bitmap table(s).

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write.
- R = Read from a specific register (write to the same address is to a different register).
- W = Write (see above).
- RO = Read Only.
- WO = Write Only. Reading from the bit returns 0.
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.
- R/W1S = Read/Write 1 to Set. Writing 1 to a bit sets its value to 1. Writing 0 has no effect.

10.1 FLOPPY DISK CONTROLLER (FDC)

10.1.1 General Description

The generic FDC is a standard FDC with a digital data separator and is DP8473 and N82077 software compatible. The PC8741x FDC supports 14 of the 17 standard FDC signals described in the generic Floppy Disk Controller (FDC) chapter, including:

- FM and MFM modes are supported. To select either mode, set bit 6 of the first command byte when writing to/reading from a diskette, where:
  - 0 = FM mode
  - 1 = MFM mode
- A logic 1 is returned during LPC I/O read cycles by all register bits, reflecting the state of floating (TRI-STATE) FDC pins.

Exceptions to standard FDC are:

- Automatic media sense using the MSEN1 signal is not supported.
- DRATE1 is not supported.

Table 59 lists the FDC functional block registers. All registers are V_{DD} powered.

Table 59. FDC Registers

Offset[1]	Mnemonic	Register Name	Type
00h	SRA	Status A	RO
01h	SRB	Status B	RO
02h	DOR	Digital Output	R/W
03h	TDR	Tape Drive	R/W
04h	MSR	Main Status	R
	DSR	Data Rate Select	W
05h	FIFO	Data (FIFO)	R/W

10.0 Legacy Functional Blocks (Continued)

Table 59. FDC Registers (Continued)

Offset[1]	Mnemonic	Register Name	Type
06h		N/A	X
07h	DIR	Digital Input	R
	CCR	Configuration Control	W

1. From the 8-byte aligned FDC base address.

10.1.2 FDC Bitmap Summary

The FDC supports two system operation modes: PC-AT mode and PS/2 mode. Unless specifically indicated otherwise, all fields in all registers are valid in both drive modes.

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	SRA[1]	IRQ Pending	Reserved	Step	$\overline{\text{TRK0}}$	Head Select	$\overline{\text{INDEX}}$	$\overline{\text{WP}}$	Head Direction
01h	SRB[1]	Reserved		Drive Select 0 Status	$\overline{\text{WDATA}}$	$\overline{\text{RDATA}}$	$\overline{\text{WGATE}}$	$\overline{\text{MTR1}}$	$\overline{\text{MTR0}}$
02h	DOR	Motor Enable 3	Motor Enable 2	Motor Enable 1	Motor Enable 0	DMAEN	Reset Controller	Drive Select	
03h	TDR	Reserved						Tape Drive Select 1,0	
	TDR[2]	Reserved (must be 1)	MSEN0	Drive ID Information		Logical Drive Exchange		Tape Drive Select 1,0	
04h	MSR	RQM	Data I/O Direction	Non-DMA Execution	Command in Progress	Drive 3 Busy	Drive 2 Busy	Drive 1 Busy	Drive 0 Busy
	DSR	Software Reset	Low Power	Reserved	Precompensation Delay Select			Data Transfer Rate Select	
05h	FIFO	Data Bits							
07h	DIR[3]	$\overline{\text{DSKCHG}}$	Reserved						
	DIR[1]	$\overline{\text{DSKCHG}}$	Reserved				DRATE 1,0 Status		High Density
07h	CCR	Reserved						DRATE1,0	

1. Applicable only in PS/2 Mode.
2. Applicable only in Enhanced TDR Mode.
3. Applicable only in PC-AT Compatible Mode.

10.0 Legacy Functional Blocks (Continued)

10.2 PARALLEL PORT

10.2.1 General Description

The Parallel Port supports all IEEE1284 standard communication modes:

- Compatibility (known also as Standard or SPP).
- Bidirectional (known also as PS/2).
- FIFO.
- EPP (known also as Mode 4).
- ECP (with an optional Extended ECP mode).

10.2.2 Parallel Port Register Map

The Parallel Port includes two groups of runtime registers, as follows:

- A group of 21 registers at first level offset, sharing 14 entries. Three of these registers (at offsets 403h, 404h and 405h) are used only in the Extended ECP mode.
- A group of four registers, used only in the Extended ECP mode, accessed by a second level offset.

EPP and second level offset registers are available only when the base address is 8-byte aligned.

The desired mode is selected by the ECR runtime register (offset 402h). The selected mode determines which runtime registers are used and which address bits are used for the base address. See Tables 60 and 61 for a listing of all registers, their offset addresses and the associated modes. All registers are V_{DD} powered.

Table 60. Parallel Port Registers at First Level Offset

Offset	Mnemonic	Mode(s)	Register Name	Type
00h	DATAR	0,1	Data	R/W
	AFIFO	3	ECP FIFO (Address)	W
	DTR	4	Data (for EPP)	R/W
01h	DSR	0,1,2,3	Status	RO
	STR	4	Status (for EPP)	RO
02h	DCR	0,1,2,3	Control	R/W
	CTR	4	Control (for EPP)	R/W
03h	ADDR	4	EPP Address	R/W
04h	DATA0	4	EPP Data Port 0	R/W
05h	DATA1	4	EPP Data Port 1	R/W
06h	DATA2	4	EPP Data Port 2	R/W
07h	DATA3	4	EPP Data Port 3	R/W
400h	CFIFO DFIFO TFIFO CNFGA	2 3 6 7	PP Data FIFO ECP Data FIFO Test FIFO Configuration A	W R/W R/W RO
401h	CNFGB	7	Configuration B	RO
402h	ECR	0,1,2,3	Extended Control	R/W
403h	EIR[1]	0,1,2,3	Extended Index	R/W
404h	EDR[1]	0,1,2,3	Extended Data	R/W
405h	EAR[1]	0,1,2,3	Extended Auxiliary Status	R/W

1. These registers are extended to the standard IEEE1284 registers. They are only accessible when enabled by bit 4 of the Parallel Port Configuration register (see Section 3.9.3 on page 62).

10.0 Legacy Functional Blocks (Continued)

Table 61. Parallel Port Registers at Second Level Offset

Offset	Mnemonic	Register Name	Type
00h	Control0	Extended Control 0	R/W
02h	Control2	Extended Control 1	R/W
04h	Control4	Extended Control 4	R/W
05h	PP Confg0	Configuration 0	R/W

10.2.3 Parallel Port Bitmap Summary

The Parallel Port functional block bitmaps are grouped according to first and second level offsets.

Table 62. Parallel Port Bitmap Summary for First Level Offset

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
000h	DATAR	Data Bits							
	AFIFO	Address Bits							
001h	DSR	Printer Status	$\overline{\text{ACK}}$ Status	PE Status	SLCT Status	$\overline{\text{ERR}}$ Status	Reserved		EPP Time-out Status
002h	DCR	Reserved		Direction Control	Interrupt Enable	PP Input Control	Printer Initialization Control	Automatic Line Feed Control	Data Strobe Control
003h	ADDR	EPP Device or Register Selection Address Bits							
004h	DATA0	EPP Device or R/W Data							
005h	DATA1	EPP Device or R/W Data							
006h	DATA2	EPP Device or R/W Data							
007h	DATA3	EPP Device or R/W Data							
400h	CFIFO	Data Bits							
400h	DFIFO	Data Bits							
400h	TFIFO	Data Bits							
400h	CNFGA	Reserved				Bit 7 of PP Confg0	Reserved		
401h	CNFGB	Reserved	Interrupt Request Value	Interrupt Select			Reserved	DMA Channel Select	
402h	ECR	ECP Mode Control			ECP Interrupt Mask	ECP DMA Enable	ECP Interrupt Service	FIFO Full	FIFO Empty
403h	EIR	Reserved					Second Level Offset		
404h	EDR	Data Bits							
405h	EAR	FIFO Tag	Reserved						

10.0 Legacy Functional Blocks (Continued)

Table 63. Parallel Port Bitmap Summary for Second Level Offset

Register		Bits							
Second Level Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	Control0	Reserved		DCR Register Live	Freeze Bit	Reserved			EPP Time-out Interrupt Mask
02h	Control2	SPP Compatibility	Channel Address Enable	Reserved	Revision 1.7 or 1.9 Select	Reserved			
04h	Control4	Reserved	PP DMA Request Inactive Time			Reserved	PP DMA Request Active Time		
05h	PP Confg0	Bit 3 of CNFGA	Demand DMA Enable	ECP IRQ Channel Number			PE Internal Pull-up or Pull-down	ECP DMA Channel Number	

10.0 Legacy Functional Blocks (Continued)

10.3 SERIAL PORTS (SP1 AND SP2)

10.3.1 General Description

The identical Serial Port functional blocks SP1 and SP2 both support serial data communication with a remote peripheral device or modem using a wired interface. The Serial Ports can function in one of three modes:

- 16450-Compatible mode (Standard 16450)
- 16550-Compatible mode (Standard 16550)
- Extended mode

Extended mode provides advanced functionality for the UART.

The Serial Ports provide receive and transmit channels that can operate concurrently in full-duplex mode. They perform all functions required to conduct parallel data interchange with the system and composite serial data exchange with the external data channel, including:

- Format conversion between the internal parallel data format and the external programmable composite serial format
- Serial data timing generation and recognition
- Parallel data interchange with the system using a choice of bidirectional data transfer mechanisms
- Status monitoring for all phases of communication activity
- Complete MODEM-control capability.

Existing 16550-based legacy software is completely and transparently supported. Module organization and specific fallback mechanisms switch the module to 16550-Compatible mode on reset or when initialized by 16550 software.

10.3.2 Register Bank Overview

Four register banks, each containing eight registers, control Serial Port operation. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The active bank must be selected by the software.

The register bank organization enables access to the banks as required for activation of all module modes, while maintaining transparent compatibility with 16450 or 16550 software.

The Bank Selection register (BSR) selects the active bank and is common to all banks as shown in Figure 52. Therefore, each bank defines seven new registers.

The default bank selection after system reset is 0.

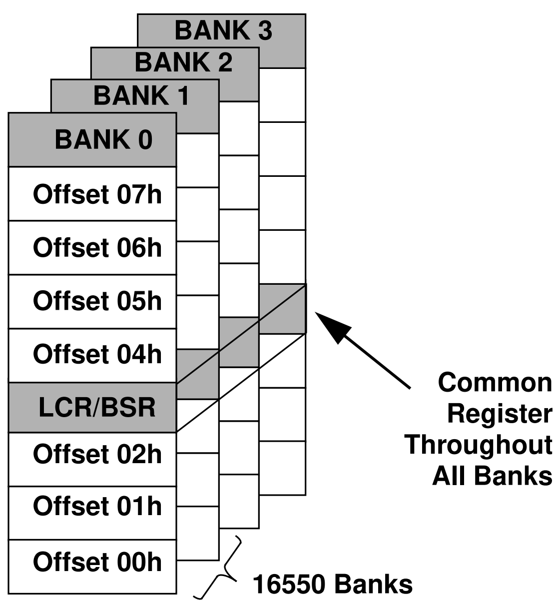


Figure 52. Register Bank Architecture

10.0 Legacy Functional Blocks (Continued)

10.3.3 SP1/SP2 Register Maps

Table 64. Bank 0 Register Map

Offset	Mnemonic	Register Name	Type
00h	RXD	Receiver Data	RO
	TXD	Transmitter Data	W
01h	IER	Interrupt Enable	R/W
02h	EIR	Event Identification	R
	FCR	FIFO Control	W
03h	LCR	Link Control	W
	BSR	Bank Select	R/W
04h	MCR	Modem/Mode Control	R/W
05h	LSR	Link Status	R/W
06h	MSR	Modem Status	R
07h	SPR	Scratch Pad	R/W
	ASCR	Auxiliary Status and Control	RO

Table 65. Bank 1 Register Map

Offset	Mnemonic	Register Name	Type
00h	LBGD(L)	Legacy Baud Generator Divisor (Low Byte)	R/W
01h	LBGD(H)	Legacy Baud Generator Divisor (High Byte)	R/W
02h		Reserved	
03h	LCR/BSR	Link Control/ Bank Select	R/W
04h-07h		Reserved	

Table 66. Bank 2 Register Map

Offset	Mnemonic	Register Name	Type
00h	BGD(L)	Baud Generator Divisor (Low Byte)	R/W
01h	BGD(H)	Baud Generator Divisor (High Byte)	R/W
02h	EXCR1	Extended Control 1	R/W
03h	BSR	Bank Select	R/W
04h	EXCR2	Extended Control 2	R/W
05h		Reserved	
06h	TXFLV	TX_FIFO Level	RO
07h	RXFLV	RX_FIFO Level	RO

10.0 Legacy Functional Blocks (Continued)

Table 67. Bank 3 Register Map

Offset	Mnemonic	Register Name	Type
00h	MRID	Module Identification and Revision ID	RO
01h	SH_LCR	Shadow of LCR	RO
02h	SH_FCR	Shadow of FIFO Control	RO
03h	BSR	Bank Select	R/W
04h-07h		Reserved	

10.3.4 SP1 Bitmap Summary

Table 68. Bank 0 Bitmap

<table>
<tr><th colspan="2">Register</th><th colspan="8">Bits</th></tr>
<tr><th>Offset</th><th>Mnemonic</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>00h</td><td>RXD</td><td colspan="8">RXD7-0</td></tr>
<tr><td>00h</td><td>TXD</td><td colspan="8">TXD7-0</td></tr>
<tr><td rowspan="2">01h</td><td>IER[1]</td><td colspan="4">Reserved</td><td>MS_IE</td><td>LS_IE</td><td>TXLDL_IE</td><td>RXHDL_IE</td></tr>
<tr><td>IER[2]</td><td colspan="2">Reserved</td><td>TXEMP_IE</td><td>Reserved</td><td>MS_IE</td><td>LS_IE</td><td>TXLDL_IE</td><td>RXHDL_IE</td></tr>
<tr><td rowspan="4">02h</td><td>EIR[1]</td><td colspan="2">FEN1-0</td><td colspan="2">Reserved</td><td>RXFT</td><td colspan="2">IPR1-0</td><td>IPF</td></tr>
<tr><td>EIR[2]</td><td colspan="2">Reserved</td><td>TXEMP_EV</td><td>Reserved</td><td>MS_EV</td><td>LS_EV</td><td>TXLDL_EV</td><td>RXHDL_EV</td></tr>
<tr><td>FCR[1]</td><td colspan="2">RXFTH1-0</td><td colspan="3">Reserved</td><td>TXSR</td><td>RXSR</td><td>FIFO_EN</td></tr>
<tr><td>FCR[2]</td><td colspan="2">RXFTH1-0</td><td colspan="2">TXFTH1-0</td><td>Reserved</td><td>TXSR</td><td>RXSR</td><td>FIFO_EN</td></tr>
<tr><td rowspan="2">03h</td><td>LCR</td><td>BKSE</td><td>SBRK</td><td>STKP</td><td>EPS</td><td>PEN</td><td>STB</td><td colspan="2">WLS1-0</td></tr>
<tr><td>BSR</td><td>BKSE</td><td colspan="7">BSR6-0</td></tr>
<tr><td rowspan="2">04h</td><td>MCR[1]</td><td colspan="3">Reserved</td><td>LOOP</td><td>ISEN/
DCDLP</td><td>RILP</td><td>RTS</td><td>DTR</td></tr>
<tr><td>MCR[2]</td><td colspan="4">Reserved</td><td>TX_DFR</td><td>Reserved</td><td>RTS</td><td>DTR</td></tr>
<tr><td>05h</td><td>LSR</td><td>ER_INF</td><td>TXEMP</td><td>TXRDY</td><td>BRK</td><td>FE</td><td>PE</td><td>OE</td><td>RXDA</td></tr>
<tr><td>06h</td><td>MSR</td><td>DCD</td><td>RI</td><td>DSR</td><td>CTS</td><td>DDCD</td><td>TERI</td><td>DDSR</td><td>DCTS</td></tr>
<tr><td rowspan="2">07h</td><td>SPR[1]</td><td colspan="8">Scratch Data</td></tr>
<tr><td>ASCR[2]</td><td colspan="7">Reserved</td><td>RXF_TOUT</td></tr>
</table>

1. Non-Extended mode
2. Extended mode

10.0 Legacy Functional Blocks (Continued)

Table 69. Bank 1 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	LBGD(L)	LBGD7-0							
01h	LBGD(H)	LBGD15-8							
02h		Reserved							
03h	LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
	BSR	BKSE	BSR6-0						
04h-07h		Reserved							

Table 70. Bank 2 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	BGD(L)	BGD7-0							
01h	BGD(H)	BGD15-8							
02h	EXCR1	BTEST	Reserved	ETDLBK	LOOP	Reserved			EXT_SL
03h	BSR	BKSE	BSR6-0						
04h	EXCR2	LOCK	Reserved	PRESL1-0		Reserved			
05h		Reserved							
06h	TXFLV	Reserved			TFL4-0				
07h	RXFLV	Reserved			RFL4-0				

Table 71. Bank 3 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	MRID	MID3-0				RID3-0			
01h	SH_LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1-0	
02h	SH_FCR	RXFTH1-0		TXFTH1-0		Reserved	TXSR	RXSR	FIFO_EN
03h	BSR	BKSE	BSR6-0						
04-07h		Reserved							

10.0 Legacy Functional Blocks (Continued)

10.4 KEYBOARD AND MOUSE CONTROLLER (KBC)

10.4.1 General Description

The KBC is implemented physically as a single hardware module and houses two separate logical devices: a mouse controller (Logical Device 5) and a keyboard controller (Logical Device 6). The KBC is functionally equivalent to the industry standard 8042A keyboard controller. The 8042A datasheet can be used as a detailed technical reference for the KBC.

The hardware KBC module is integrated to provide the following pin functions: P12, P16, P17, KBRST (P20), GA20 (P21), KBDAT, KBCLK, MDAT and MCLK. KBRST and GA20 are implemented as bidirectional open-drain pins. The keyboard and mouse interfaces are implemented as bidirectional open-drain pins. P12, P16 and P17 are implemented as quasi-bidirectional pins. Their internal connections are shown in Figure 53.

P10, P11, P13-P15 and P22-P27 of the KBC core are not available on dedicated pins; neither are T0 and T1. P10, P11, P22, P23, P26, P27, T0 and T1 are used to implement the keyboard and mouse interface.

Internal pull-ups are implemented only on P12, P16 and P17.

The KBC executes a program fetched from an on-chip 2Kbyte ROM. The code programmed in this ROM is user-customizable. The KBC has two interrupt request signals: one for the keyboard and one for the mouse. The interrupt requests are implemented using ports P24 and P25 of the KBC core. The interrupt requests are controlled exclusively by the KBC firmware, except for the type and number, which are affected by configuration registers (see Section 3.2.3 on page 40).

The interrupt requests are implemented as bidirectional signals. When an I/O port is read, all unused bits return the value latched in the output registers of the ports.

For KBC firmware that implements interrupt-on-OBF schemes, the following is the recommended implementation:

1. Put the data in DBBOUT.
2. Set the appropriate port bit to issue an interrupt request.

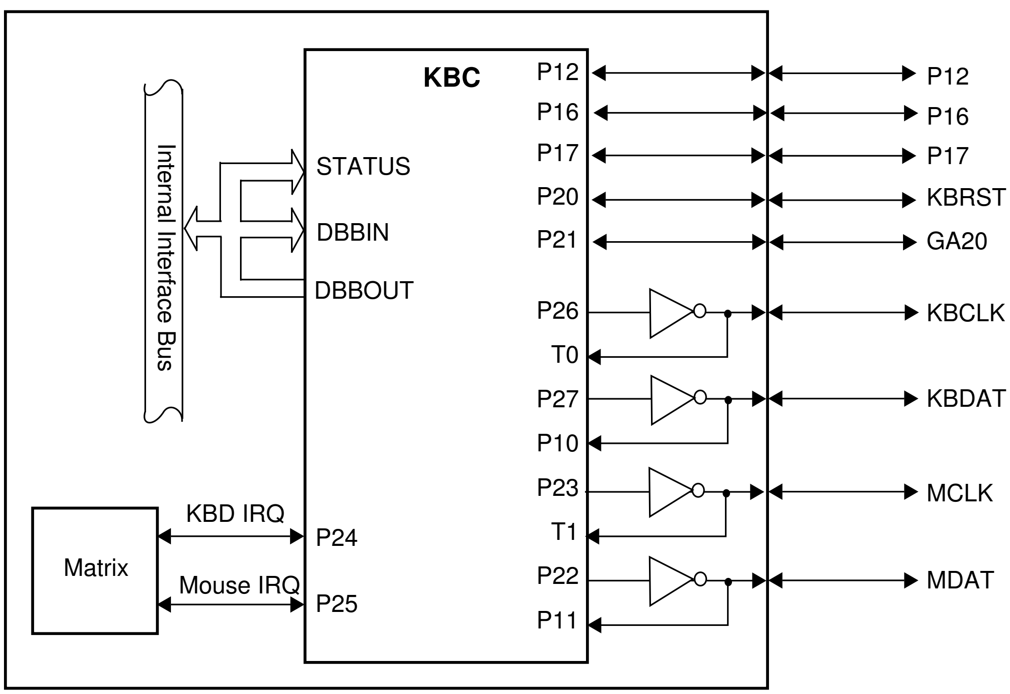


Figure 53. Keyboard and Mouse Interfaces

10.0 Legacy Functional Blocks (Continued)

10.4.2 KBC Register Map

All registers are V_{DD} powered.

Offset	Mnemonic	Register Name	Type
00h	DBBOUT	Read KBC Data	R
	DBBIN	Write KBC Data	W
04h	STATUS	Read Status	R
	DBBIN	Write KBC Command	W

10.4.3 KBC Bitmap Summary

Register		Bits							
Offset	**Mnemonic**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00h	DBBOUT	KBC Data Bits (For Read cycles)							
	DBBIN	KBC Data Bits (For Write cycles)							
04h	STATUS	General-Purpose Flags				F1	F0	IBF	OBF
	DBBIN	KBC Command Bits (For Write cycles)							

11.0 Device Characteristics

11.1 GENERAL DC ELECTRICAL CHARACTERISTICS

11.1.1 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{SB}	Standby Voltage	3.0	3.3	3.6	V
V_{BAT}	Battery Backup Supply Voltage	2.4	3.0	3.6	V
T_A	Operating Temperature	0		+70	°C

11.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUP}	Supply Voltage[1]		–0.5	+6.5	V
V_I	Input Voltage	All other pins	–0.5	5.5	V
		LCLK, LAD3-0, $\overline{\text{LFRAME}}$, $\overline{\text{LRESET}}$, SERIRQ, $\overline{\text{CLKRUN}}$, 32KX1_32KCLKIN	–0.5	V_{DD} + 0.5	V
V_O	Output Voltage	All other pins	–0.5	5.5	V
		LAD3-0, $\overline{\text{LDRQ}}$, SERIRQ, $\overline{\text{CLKRUN}}$, 32KX2	–0.5	V_{DD} + 0.5	V
T_{STG}	Storage Temperature		–65	+165	°C
P_D	Power Dissipation			1	W
T_L	Lead Temperature Soldering (10 s)			+260	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 KΩ[2]	2000		V
MCRS	Battery Maximum Safe Reverse Current	V_{SB} = 3.63V R_{UL}[3]=0.8KΩ	4.53		mA

1. V_{SUP} is V_{DD}, V_{SB} or V_{BAT}.
2. Value based on test complying with RAI-5-048-RA human body model ESD testing.
3. Minimum value of internal protection resistor (see Figure 45 on page 147).

11.0 Device Characteristics (Continued)

11.1.3 Capacitance

Symbol	Parameter	Min[2]	Typ[1]	Max[2]	Unit
C_{IN}	Input Pin Capacitance		4	5	pF
C_{IN1}	Clock Input Capacitance[3]	5	8	12	pF
C_{IO}	I/O Pin Capacitance		8	10	pF
C_O	Output Pin Capacitance		6	8	pF

1. T_A = 25°C, f = 1 MHz.
2. Not tested. Guaranteed by characterization.
3. LCLK, CLKIN.

11.1.4 Power Consumption under Recommended Operating Conditions

Symbol	Parameter	Conditions[1]	Typ	Max	Unit
I_{DD}	V_{DD} Average Main Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V No Load	21	30	mA
I_{DDLP}	V_{DD} Quiescent Main Supply Current in Low Power Mode[2]	V_{IL} = V_{SS}, V_{IH} = V_{DD} No Load	0.5	0.8	mA
I_{SB}	V_{SB} Average Main Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V No Load	14	20	mA
I_{SBLP}	V_{SB} Quiescent Main Supply Current in Low Power Mode[2]	V_{IL} = V_{SS}, V_{IH} = V_{SB} No Load	5	8	mA
I_{BAT}	V_{BAT} Battery Supply Current	V_{DD}, V_{SB} = 0V, V_{BAT} = 3V	0.9	1.5	µA

1. All parameters specified for 0° C ≤ T_A ≤ 70° C; V_{DD} and V_{SB} = 3.3V ±10%, unless otherwise specified.
2. All the modules disabled; clock outputs disabled; no LPC or ACCESS.bus activity.

11.1.5 Voltage Thresholds

Symbol	Parameter[1]	Min[2]	Typ	Max[2]	Unit
V_{DDON}	V_{DD} Detected as Power-on	2.3	2.6	2.9	V
V_{DDOFF}	V_{DD} Detected as Power-off	2.2	2.5	2.8	V
V_{DDHY}	V_{DD} Hysteresis (V_{DDON} – V_{DDOFF})	0.1			V
V_{SBON}	V_{SB} Detected as Power-on	2.3	2.6	2.9	V
V_{SBOFF}	V_{SB} Detected as Power-off	2.2	2.5	2.8	V
V_{SBHY}	V_{SB} Hysteresis (V_{SBON} – V_{SBOFF})	0.1			V
V_{BATDTC}	Battery Detected	1.0		1.2	V
V_{LOWBAT}	Low Battery Voltage	1.3		1.9	V

1. All parameters specified for 0° C ≤ T_A ≤ 70° C.
2. Not tested. Guaranteed by characterization.

11.0 Device Characteristics (Continued)

11.2 DC CHARACTERISTICS OF PINS, BY I/O BUFFER TYPES

The following tables summarize the DC characteristics of all device pins described in Section 1.2 on page 20. The characteristics describe the general I/O buffer types defined in Table 1 on page 20. For exceptions, refer to Section 11.2.9 on page 235. The DC characteristics of the LPC Interface meet the PCI Local Bus Specification *(Rev 2.2 December 18, 1998)* for 3.3V DC signaling. The DC characteristics of the ACCESS.bus Interface meet the SMBus (*Rev 1.1 Dec. 11, 1998*) and ACCESS.bus *(Rev. 3.0 Sep. 1995*) specifications for on-board devices.

11.2.1 Input, CMOS Compatible with Schmitt Trigger

Symbol: IN_{CS}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		0.75 V_{SUP}[1]	5.5[2]	V
V_{IL}	Input Low Voltage		–0.5[1]	1.1	V
V_{HY}	Input Hysteresis		200[3]		mV
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{SUP}$		±1[4]	µA

1. V_{SUP} is V_{DD}, V_{SB} or V_{PP} according to the input power well.
2. Not tested. Guaranteed by design.
3. Not tested. Guaranteed by characterization.
4. Maximum 10 µA for all pins together. Not tested. Guaranteed by characterization.

11.2.2 Input, PCI 3.3V

Symbol: IN_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		0.5 V_{DD}	V_{DD} + 0.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.3 V_{DD}	V
I_{IL}[2]	Input Leakage Current	$0 < V_{IN} < V_{DD}$		±1[3]	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs.
3. Maximum 10 µA for all pins together. Not tested. Guaranteed by characterization.

11.2.3 Input, SMBus Compatible

Symbol: IN_{SM}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		1.4	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
I_{IL}[2]	Input Leakage Current	$0 < V_{IN} < V_{SB}$		±1[3]	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs.
3. Maximum 10 µA for all pins together. Not tested. Guaranteed by characterization.

11.0 Device Characteristics (Continued)

11.2.4 Input, TTL Compatible

Symbol: IN_T

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
I_{IL}[2]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[3]		±1[4]	µA

1. Not tested. Guaranteed by design.
2. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs.
3. V_{SUP} is V_{DD}, V_{SB} or V_{PP} according to the input power well.
4. Maximum 10 µA for all pins together. Not tested. Guaranteed by characterization.

11.2.5 Input, TTL Compatible with Schmitt Trigger

Symbol: IN_{TS}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5[1]	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V
V_{HY}	Input Hysteresis		200[2]		mV
I_{IL}[3]	Input Leakage Current	$0 < V_{IN} < V_{SUP}$[4]		±1[5]	µA

1. Not tested. Guaranteed by design.
2. Not tested. Guaranteed by characterization.
3. Input leakage current includes the output leakage of the bidirectional buffers with TRI-STATE outputs.
4. V_{SUP} is V_{DD}, V_{SB} or V_{PP} according to the input power well.
5. Maximum 10 µA for all pins together. Not tested. Guaranteed by characterization.

11.2.6 Output, TTL Compatible Push-Pull Buffer

Symbol: $O_{p/n}$

Output, TTL Compatible, rail-to-rail Push-Pull buffer that is capable of sourcing *p* mA and sinking *n* mA

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	$I_{OH} = -p$ mA	2.4		V
		$I_{OH} = -50$ µA	$V_{SUP} - 0.2$[1]		V
V_{OL}	Output Low Voltage	$I_{OL} = n$ mA		0.4	V
		$I_{OL} = 50$ µA		0.2	V

1. V_{SUP} is V_{DD}, V_{SB} or V_{PP} according to the output power well.

11.0 Device Characteristics (Continued)

11.2.7 Output, Open-Drain Buffer

Symbol: OD_n

Output, TTL Compatible Open-Drain output buffer capable of sinking *n* mA. Output from these signals is open-drain and is never forced high.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = *n* mA		0.4	V
		I_{OL} = 50 µA		0.2	V

11.2.8 Output, PCI 3.3V

Symbol: O_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{out} = –500 µA	0.9 V_{DD}		V
V_{OL}	Output Low Voltage	I_{out} =1500 µA		0.1 V_{DD}	V

11.2.9 Exceptions

1. All pins are 5V tolerant except for the pins with PCI (IN_{PCI}, O_{PCI}) buffer types.
2. All pins are back-drive protected except for the pins with PCI (IN_{PCI}, O_{PCI}) and oscillator (O_{OSC}) buffer types.
3. The following pins have an internal static pull-up resistor (when enabled) and therefore may have leakage current to V_{SUP} (when V_{IN} = 0): $\overline{ACK}$, $\overline{AFD\_DSTRB}$, $\overline{ERR}$, $\overline{INIT}$, PE, $\overline{SLIN\_ASTRB}$, $\overline{STB\_WRITE}$, PPDIS, P12, P16, P17, ACBCLK, ACBDAT, $\overline{PWBTIN}$, SLBTIN, $\overline{PWBTOUT}$, GPIO00-07, GPIOE10-17, GPIO20-27, GPIO30-37, GPIOE40-47, GPIO50-55 and GPIO60-64.
4. The following pins have an internal static pull-down resistor (when enabled) and therefore may have leakage current to V_{SS} (when V_{IN} = V_{SUP}): BUSY_$\overline{WAIT}$, PE and SLCT.
5. The following strap pins have an internal static pull-down resistor enabled during power-up reset and therefore may have leakage current to V_{SS} (when V_{IN} = V_{SUP}): BADDR, TRIS, CKIN48, XCNF2-0 and ACBSA.
6. When V_{DD} = 0V, the following pins present a DC load to V_{SS} of 30 KΩ minimum (not tested, guaranteed by design) for a pin voltage of 0V to 3.6V: $\overline{CTS1}$, $\overline{CTS2}$, $\overline{DCD1}$, $\overline{DCD2}$, $\overline{DSR1}$, $\overline{DSR2}$, $\overline{DTR1\_BOUT1}$, $\overline{DTR2\_BOUT2}$, $\overline{RI1}$, $\overline{RI2}$, $\overline{RTS1}$, $\overline{RTS2}$, SIN1, SIN2, SOUT1, SOUT2.
7. Output from SLCT, BUSY_$\overline{WAIT}$ (and PE if bit 2 of PP Confg0 register is 0) is open-drain in all SPP modes except in SPP-Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
8. Output from $\overline{ACK}$, $\overline{ERR}$ (and PE if bit 2 of PP Confg0 register is set to 1) is open-drain in all SPP modes except in SPP-Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is set to 1. Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
9. Output from $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$ and $\overline{SLIN}$ is open-drain in all SPP modes, except in SPP-Compatible mode when the setup mode is ECP-based (FIFO). Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
10. I_{OH} is valid for a GPIO pin only when it is not configured as open-drain.

11.2.10 Terminology

Back-Drive Protection. A pin that is back-drive protected does not sink current into the supply when an input voltage higher than the supply, but below the pin's maximum input voltage, is applied to the pin. This is true even when the supply is inactive. Note that active pull-up resistors and active output buffers are typically not back-drive protected.

5-Volt Tolerance. An input signal that is 5V tolerant can operate with input voltage of up to 5V even though the supply to the device is only 3.3V. The actual maximum input voltage allowed to be supplied to the pin is indicated by the maximum high voltage allowed for the input buffer. Note that some pins have multiple buffers, not all of which are 5V tolerant. In such cases, there is a note that indicates at what conditions a 5V input may be applied to the pin; if there is no note, the low maximum voltage among the buffers is the maximum voltage allowed for the pin.

11.0 Device Characteristics (Continued)

11.3 INTERNAL RESISTORS

DC Test Conditions

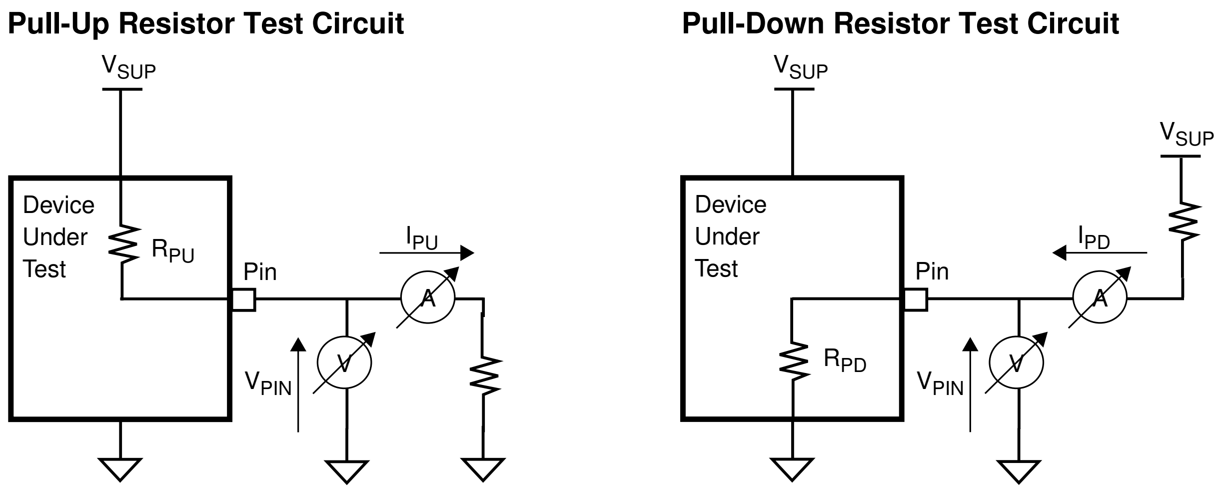


Figure 54. Internal Resistor Test Conditions, T_A = 0 °C to 70 °C, V_{SUP} = 3.3V

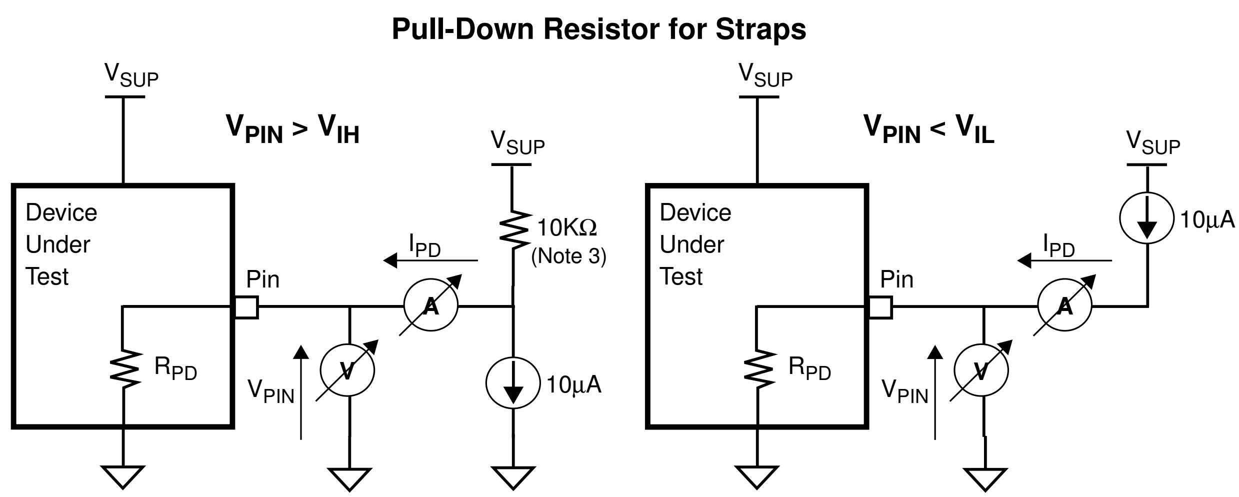


Figure 55. Internal Pull-Down Resistor for Straps, T_A = 0 °C to 70 °C, V_{SUP} = 3.3V

Notes for Figures 54 and 55:

1. V_{SUP} is V_{DD} or V_{SB} according to the pin power well.
1. The equivalent resistance of the pull-up resistor is calculated by $R_{PU} = (V_{SUP} - V_{PIN}) / I_{PU}$.
2. The equivalent resistance of the pull-down resistor is calculated by $R_{PD} = V_{PIN} / I_{PD}$.
3. The external pull-up resistor is 4.7KΩ for the TRIS strap.

11.0 Device Characteristics (Continued)

11.3.1 Pull-Up Resistor

Symbol: PU_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PU}	Pull-up equivalent resistance	$V_{PIN} = 0V$	*nn*–30%	*nn*	*nn*+30%	KΩ

1. TA = 0 °C to 70 °C, V_{SUP} = 3.3V.
2. Not tested. Guaranteed by characterization.

11.3.2 Pull-Down Resistor

Symbol: PD_{nn}

Symbol	Parameter	Conditions[1]	Min[2]	Typical	Max[2]	Unit
R_{PD}	Pull-down equivalent resistance	$V_{PIN} = V_{SUP}$	*nn*–30%	*nn*	*nn*+30%	KΩ
		$V_{PIN} = 0.17\ V_{SUP}$[3]			*nn*–50%	KΩ
		$V_{PIN} = 0.8\ V_{SUP}$[3]	*nn*–48%			KΩ

1. TA = 0 °C to 70 °C, V_{SUP} = 3.3V.
2. Not tested. Guaranteed by characterization.
3. For strap pins only.

11.4 PACKAGE THERMAL INFORMATION

Thermal resistance (degrees C/W) $Theta_{JC}$ and $Theta_{JA}$ values for the PC8741x package are as follows:

Table 3. Theta (Θ) J Values

Package Type	$Theta_{JA}$@0 lfpm	$Theta_{JA}$@225 lfpm	$Theta_{JA}$@500 lfpm	$Theta_{JC}$
128 PQFP	47	35.8	31.1	14.9

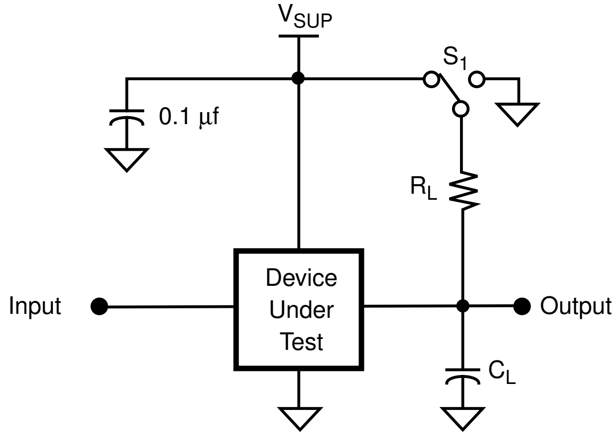
Note: Airflow for $Theta_{JA}$ values is measured in linear feet per minute (lfpm).

11.0 Device Characteristics (Continued)

11.5 AC ELECTRICAL CHARACTERISTICS

11.5.1 AC Test Conditions

Load Circuit



AC Testing Input, Output Waveform

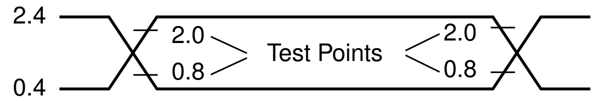


Figure 56. AC Test Conditions, T_A = 0 °C to 70 °C, V_{SUP} = 3.3V ±10%

Notes:

1. V_{SUP} is V_{DD}, V_{SB} or V_{PP} according to the pin power well.
2. C_L = 50 pF for all output pins except the following pin groups:
   C_L = 100 pF for Serial Port 1 and 2 (see Section 1.4.4 on page 24), Parallel Port (see Section 1.4.5) and Floppy Disk Controller (see Section 1.4.6) pins;
   C_L = 40 pF for HFCKOUT pin;
   C_L = 400 pF for ACCESS.bus pins (see Section 1.4.2 on page 23);
   These values include both jig and oscilloscope capacitance.
3. S_1 = Open for push-pull output pins.
   S_1 = V_{SUP} for high impedance to active low and active low to high impedance transition measurements.
   S_1 = GND for high impedance to active high and active high to high impedance transition measurements.
   R_L = 1.0 KΩ for all the pins.
4. For the FDC open-drain interface pins, S_1 = V_{DD} and R_L = 150 Ω.

11.0 Device Characteristics (Continued)

11.5.2 Reset Timing

V_{SB} Power-Up Reset

Symbol	Figure	Description	Reference Conditions	Min[1]	Max[1]
t_{LRST}	57	Minimum $\overline{\text{LRESET}}$ active time	Power stable to end of $\overline{\text{LRESET}}$	$2048 * t_{32KOSC}$	
t_{IRST}	57	Internal power-on reset time	Power stable to end of internal reset	$8192 * t_{32KOSC}$[2]	t_{32KW}[3] + $8192 * t_{32KOSC}$
t_{IPLV}	57	Internal strap pull-down resistors, valid time[4]	Before end of internal reset	$512 * t_{32KOSC}$	t_{IRST}
t_{EPLV}	57	External strap pull-up resistors, valid time	Before end of internal reset	$512 * t_{32KOSC}$	t_{IRST}

1. Not tested. Guaranteed by design.
2. Valid V_{BAT}; the 32 KHz internal clock is running while V_{SB} is Off (see *Low Frequency Clock Timing* on page 242).
3. No V_{BAT}; the 32 KHz internal clock is stopped while V_{SB} is Off (see *Low Frequency Clock Timing* on page 242).
4. Active on V_{SB} Power-Up reset only.

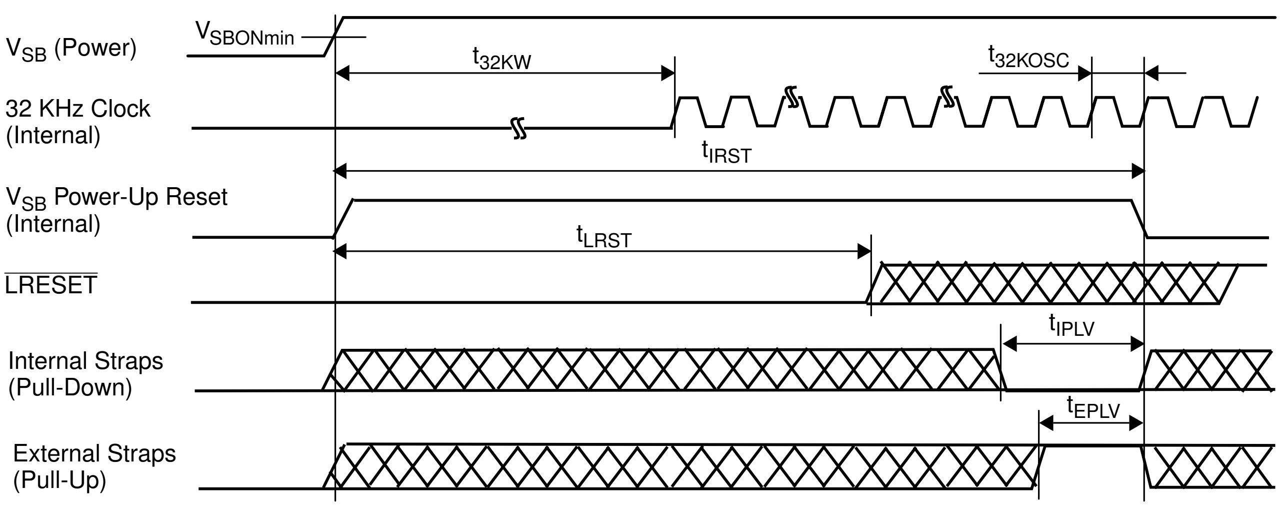


Figure 57. Internal V_{SB} Power-Up Reset (No V_{BAT})

11.0 Device Characteristics (Continued)

V_{DD} Power-Up Reset

Symbol	Figure	Description	Reference Conditions	Min[1]	Max[1]
t_{LRST}	58	Minimum $\overline{\text{LRESET}}$ active time	Power stable to end of $\overline{\text{LRESET}}$	$2048 * t_{32KOSC}$	
t_{IRST}	58	Internal Power-Up reset time	Power stable to end of internal reset	$8192 * t_{32KOSC}$	$8704 * t_{32KOSC}$
t_{IPLV}	58	Internal strap pull-down resistors, valid time[2]	Before end of internal reset	$512 * t_{32KOSC}$	t_{IRST}
t_{EPLV}	58	External strap pull-up resistors, valid time	Before end of internal reset	$512 * t_{32KOSC}$	t_{IRST}

1. Not tested. Guaranteed by design.
2. Active on V_{DD} Power-Up reset only.

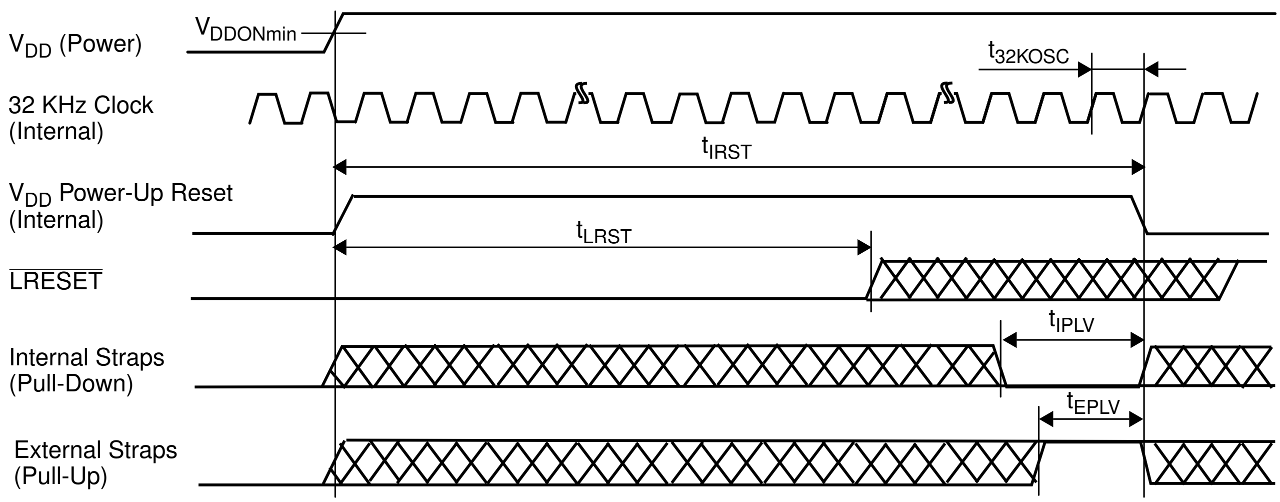


Figure 58. Internal V_{DD} Power-Up Reset

Hardware Reset

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{WRST}	59	$\overline{\text{LRESET}}$ pulse width		100 ns	

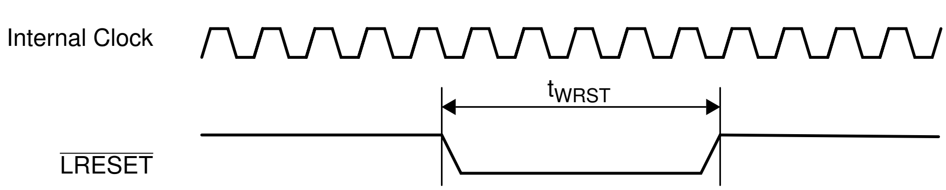


Figure 59. Hardware Reset

11.0 Device Characteristics (Continued)

11.5.3 Clock Timing

High Frequency Clock Timing

Symbol	Clock Input Parameter	CLKIN (48 MHz)			
		Min	Typ	Max	Unit
t_{CH}	Clock High Pulse Width[2]	8.2			ns
t_{CL}	Clock Low Pulse Width[2]	8.2			ns
t_{CP}	Clock Period[2] (50%-50%)	20	20.83	21.5	ns
t_{CR}	Clock Rise Time[2] (20%-80%)			2.5	ns
t_{CF}	Clock Fall Time[2] (80%-20%)			2.5	ns

Symbol	Clock Output Parameter		HFCKOUT (48 MHz)			HFCKOUT (40 MHz)			
			Min	Typ	Max	Min	Typ	Max	Unit
t_{CH}	Clock High Pulse Width[1,4]		8.2			10.3			ns
t_{CL}	Clock Low Pulse Width[1,4]		8.2			10.3			ns
t_{CP}	Clock Period[2] (50%-50%)		t_{48TYP} – $32K_{TOL}$[3] – 50ppm	20.83	t_{48TYP} + $32K_{TOL}$[3] + 50ppm	t_{40TYP} – $32K_{TOL}$[3] – 150ppm	25	t_{40TYP} + $32K_{TOL}$[3] + 150ppm	ns
t_{CR}	Clock Rise Time[4] (20%-80%)	C_L = 15 pF			2.5			2.5	ns
		C_L = 40 pF			5			5	ns
t_{CF}	Clock Fall Time[4] (80%-20%)	C_L = 15 pF			2.5			2.5	ns
		C_L = 40 pF			5			5	ns

1. C_L = 15 pF.
2. Not tested. Guaranteed by design.
3. $t_{32KCLKIN}$ tolerance.
4. Not tested. Guaranteed by characterization.

.

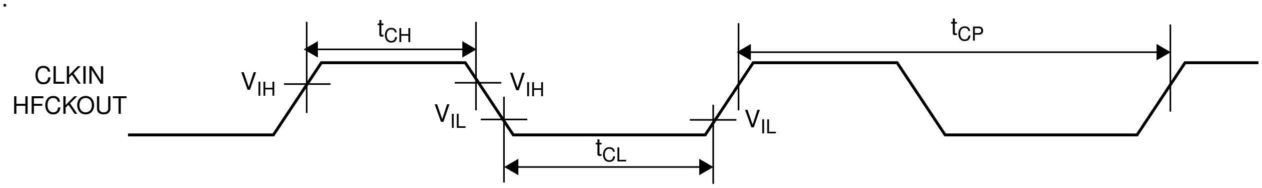


Figure 60. External High Frequency Clock Timing

11.0 Device Characteristics (Continued)

Low Frequency Clock Timing

Symbol	Figure	Description	Reference Conditions	Min	Typ	Max	Units
Clock Input Timing							
$t_{32KCLKIN}$	–	Required clock period for 32KCLKIN[1]	From RE to RE of 32KCLKIN.	30.5145 (t_{32TYP} – 100ppm)	30.517578 (t_{32TYP})	30.5206 (t_{32TYP} + 100ppm)	µs
Clock Output Timing							
t_{32KOSC}	61	Clock period of the internal oscillator[2]	From RE to RE of LFCKOUT.		30.517578 (t_{32TYP})		µs
t_{32KW}	61	32K oscillator wake-up time[3]	After $V_{SB} > V_{SBON}$			1	sec
t_{32KD}	62	Internally generated 40/48 MHz clock delay time[3]	After $V_{SB} > V_{SBON}$			33	ms

1. Recommended for RTC timekeeping accuracy and for HFCKOUT, LFCKOUT frequency accuracy.
2. Determined by the values of the external crystal circuit components.
3. Not tested. Guaranteed by characterization.

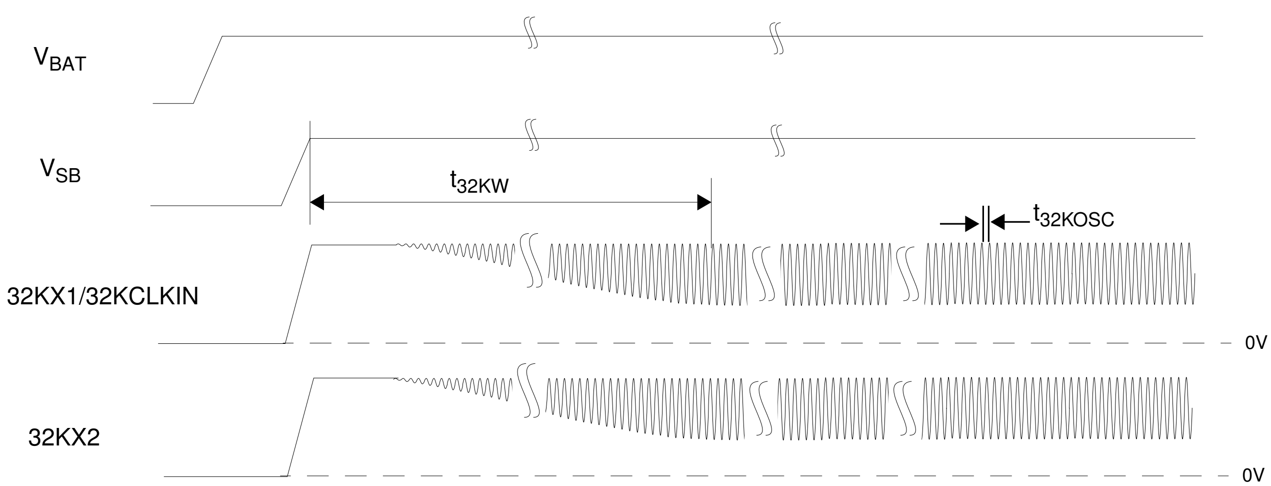


Figure 61. Low Frequency Clock Waveforms

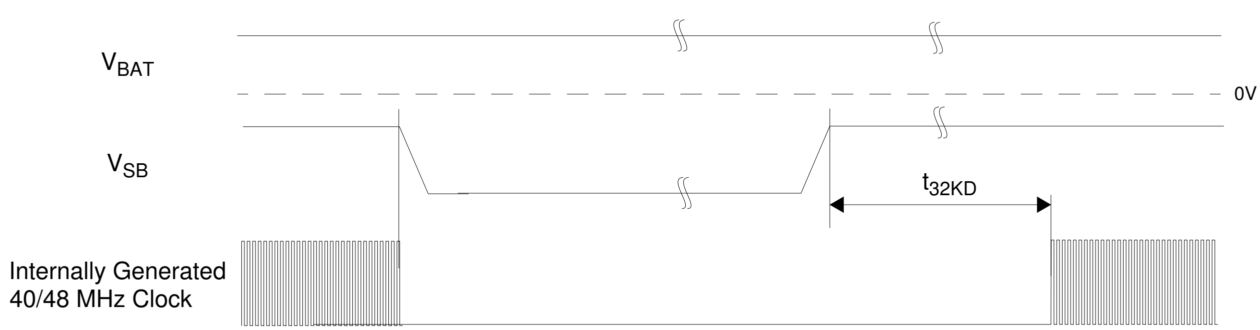


Figure 62. Internal Clock Waveforms

11.0 Device Characteristics (Continued)

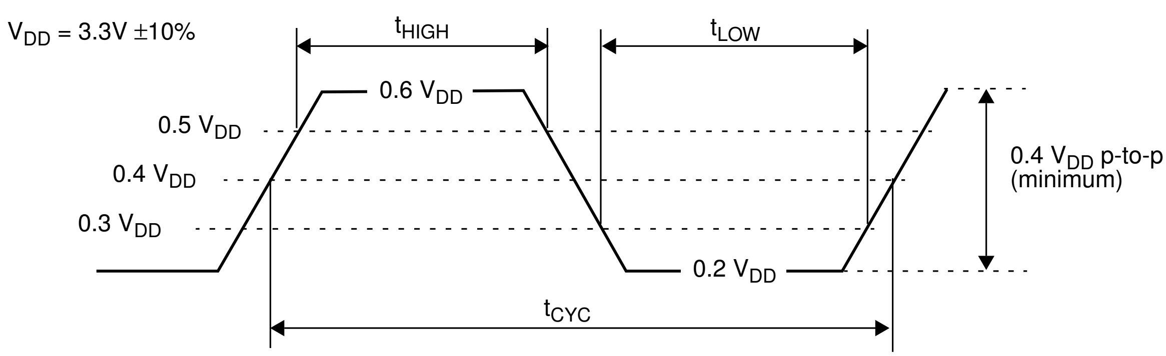
11.5.4 LPC Interface Timing

The AC characteristics of the LPC Interface meet the PCI Local Bus Specification *(Rev 2.2 December 18, 1998)* for 3.3V DC signaling.

LCLK and $\overline{\text{LRESET}}$

Symbol	Parameter	Min	Max	Units
t_{CYC}[1]	LCLK Cycle Time	30		ns
t_{HIGH}	LCLK High Time[2]	11		ns
t_{LOW}	LCLK Low Time[2]	11		ns
-	LCLK Slew Rate[2,3]	1	4	V/ns
-	$\overline{\text{LRESET}}$ Slew Rate[2,4]	50		mV/ns

1. The PCI may have any clock frequency between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz are guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system as long as the clock edges remain “clean” (monotonic) and the minimum cycle high and low times are not violated. The clock may only be stopped in a low state.
2. Not tested. Guaranteed by characterization.
3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock wavering (0.2 V_{DD} to 0.6 V_{DD}) as shown below.
4. The minimum $\overline{\text{LRESET}}$ slew rate applies only to the rising (de-assertion) edge of the reset signal and ensures that system noise cannot make an otherwise monotonic signal appear to bounce in the switching range.

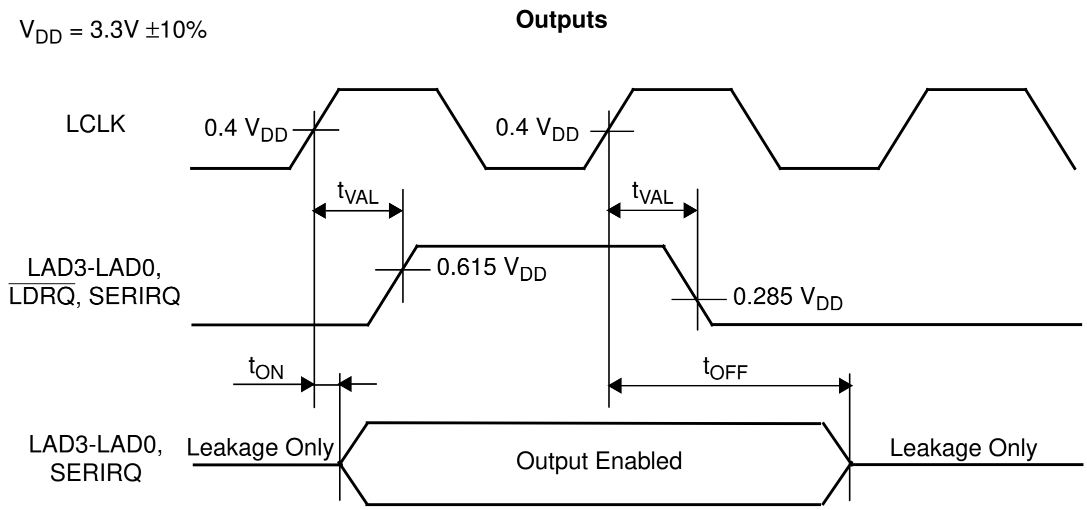


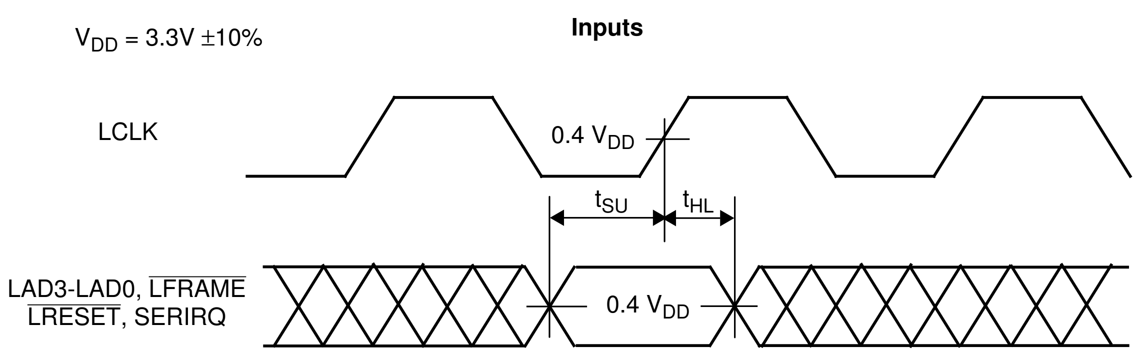
11.0 Device Characteristics (Continued)

SERIRQ and LPC Signals

Symbol	Figure	Description	Reference Conditions	Min	Max	Unit
t_{VAL}	Output	Output Valid Delay	After RE CLK		11	ns
t_{ON}	Output	Float to Active Delay	After RE CLK	2[1]		ns
t_{OFF}	Output	Active to Float Delay	After RE CLK		28[1]	ns
t_{SU}	Input	Input Setup Time	Before RE CLK	7		ns
t_{HL}	Input	Input Hold Time	After RE CLK	0		ns

1. Not tested. Guaranteed by characterization.





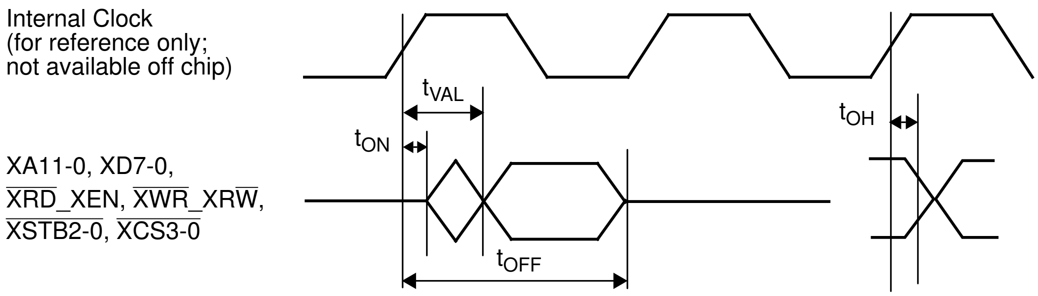
11.0 Device Characteristics (Continued)

11.5.5 X-Bus Extension Timing (PC87416 and PC87417)

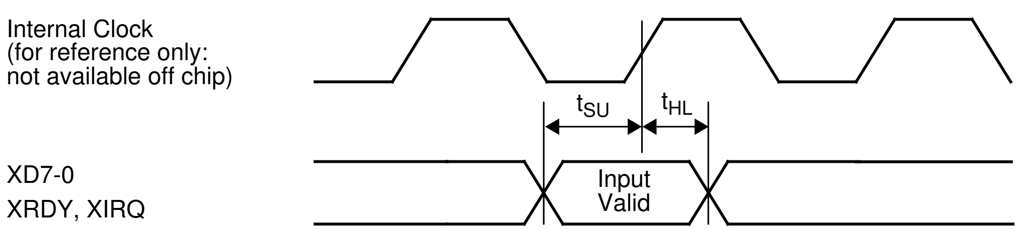
Symbol	Figure	Description	Reference Conditions	Min	Max	Unit
t_{VAL}	Outputs	Output Valid Delay	After RE Internal Clock		20[1]	ns
t_{ON}	Outputs	Float to Active Delay	After RE Internal Clock	0[2]		ns
t_{OH}	Outputs	Output Hold time	After RE Internal Clock	0[2]		ns
t_{OFF}	Outputs	Active to Float Delay	After RE Internal Clock		30[1]	ns
t_{SU}	Inputs	Input Setup Time	Before RE Internal Clock	15[1]		ns
t_{HL}	Inputs	Input Hold Time	After RE Internal Clock	0[1]		ns
t_{CSDV}	Mode 0 Turbo Read Transaction	Chip Select active to Data Valid	Read from External Device		75	ns

1. Not tested. Guaranteed by characterization.
2. Not tested. Guaranteed by design.

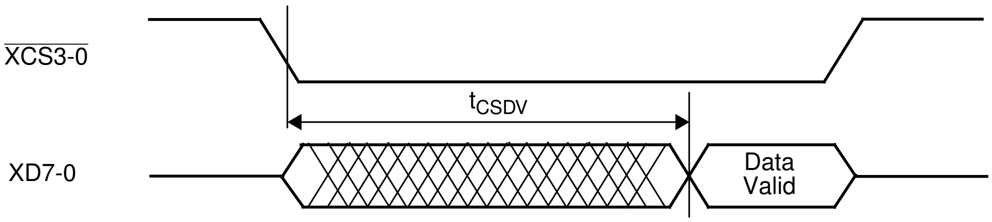
Outputs



Inputs



Mode 0 Turbo Read Transaction



11.0 Device Characteristics (Continued)

11.5.6 ACCESS.bus Timing (PC87413 and PC87417)

Symbol	Figure	Description	Type of Requirement[1]	Min	Max	Unit
t_{ACBR}	63	Rise time (ACBCLK and ACBDAT)	Input[2]		1000[3]	ns
t_{ACBF}	63	Fall time (ACBCLK and ACBDAT)	Input		300[3]	ns
			Output[2]		250[4]	ns
t_{ACBCKL}	63	Clock low period (ACBCLK)	Input	4.7		µs
t_{ACBCKH}	63	Clock high period (ACBCLK)	Input	4		µs
t_{ACBCY}	64	Clock cycle (ACBCLK)	Input	10		µs
t_{ACBDS}	64	Data setup time (before clock rising edge)	Input	250		ns
			Output[2]	250		ns
t_{ACBDH}	64	Data hold time (after clock falling edge)	Input	0		ns
			Output[2]	300		ns
t_{ACBPS}	65	Stop condition setup time (clock before data)	Input	4		µs
t_{ACBSH}	65	Start condition hold time (clock after data)	Input	4		µs
t_{ACBBUF}	65	Bus free time between Stop and Start conditions (ACBDAT)	Input	4.7		µs
t_{ACBRS}	66	Restart condition setup time (clock before data)	Input	4.7		µs
t_{ACBRH}	66	Restart condition hold time (clock after data)	Input	4		µs
t_{ACBLEX}	-	Cumulative clock low extend time from Start to Stop (ACBCLK)	Output		25[3]	ms
t_{ACBTO}	-	Clock low time-out (ACBCLK)	Input	25[3,5]		ms
			Output		35[3,6]	ms

1. An “Input” type is a value the PC8741x device expects from the system; an “Output” type is a value the PC8741x device provides to the system.
2. Test conditions: R_L = 1 KΩ to V_{SB} = 3.3V, C_L = 400 pF to GND.
3. Not tested. Guaranteed by design.
4. Not tested. Guaranteed by characterization.
5. The PC8741x device detects a time-out condition if ACBCLK is held low for more than t_{ACBTO}.
6. On detection of a time-out condition, the PC8741x device resets the ACCESS.bus Interface no later than t_{ACBTO}.

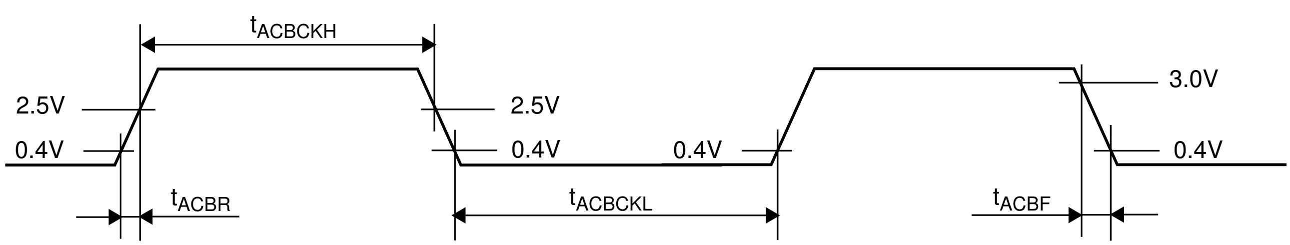


Figure 63. ACCESS.bus Signals (ACBCLK and ACBDAT) Rising Time and Falling Time

11.0 Device Characteristics (Continued)

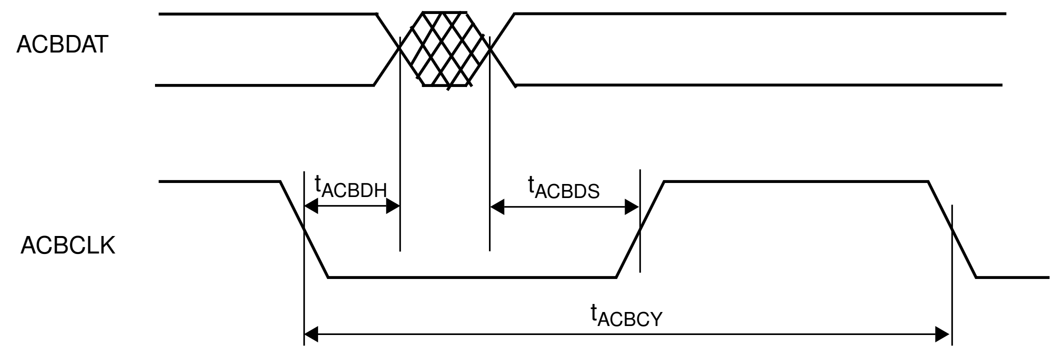


Figure 64. ACCESS.bus Data Bit Timing

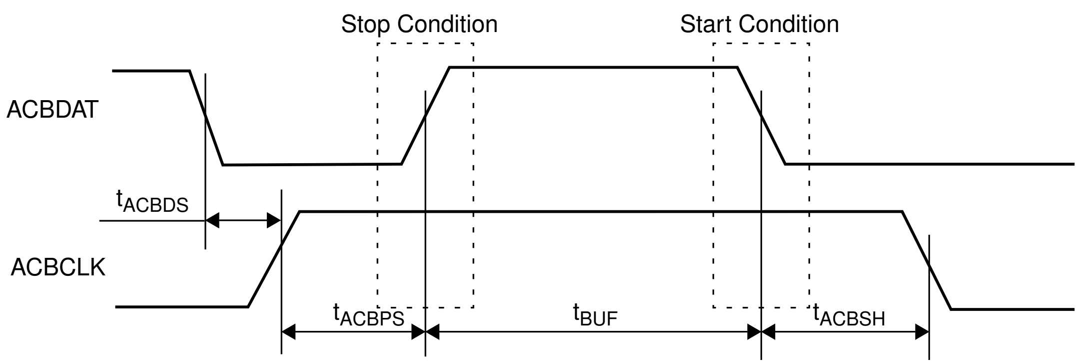


Figure 65. ACB Start and Stop Condition Timing

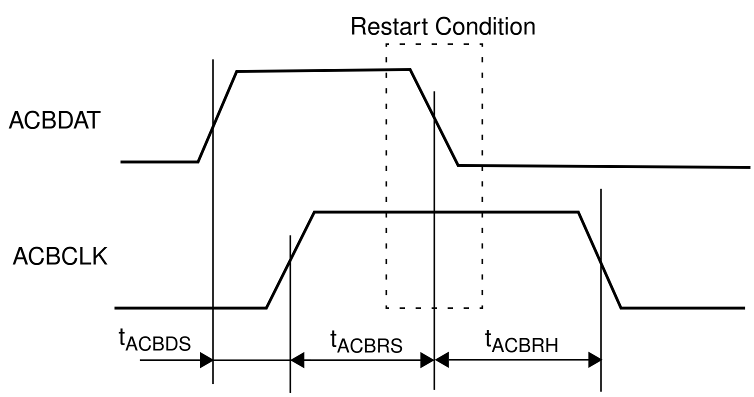


Figure 66. ACB Restart Condition TIming

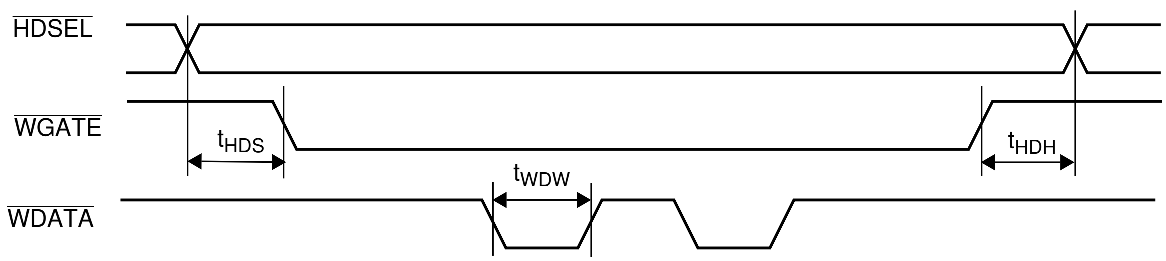
11.0 Device Characteristics (Continued)

11.5.7 FDC Timing

FDC Write Data Timing

Symbol	Parameter	Min	Max	Unit
t_{HDH}	$\overline{\text{HDSEL}}$ Hold from $\overline{\text{WGATE}}$ Inactive[1]	100		µs
t_{HDS}	$\overline{\text{HDSEL}}$ Setup to $\overline{\text{WGATE}}$ Active[1]	100		µs
t_{WDW}	Write Data Pulse Width[1]	See t_{DRP}, t_{ICP} and t_{WDW} values in table below		

1. Not tested. Guaranteed by design.



t_{DRP} t_{ICP} t_{WDW} Values

Data Rate	t_{DRP}	t_{ICP}	t_{ICP} Nominal	t_{WDW}	t_{WDW} Minimum	Unit
1 Mbps	1000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	ns
500 Kbps	2000	6 x t_{CP}[1]	125	2 x t_{ICP}	250	ns
300 Kbps	3333	10 x t_{CP}[1]	208	2 x t_{ICP}	375	ns
250 Kbps	4000	12 x t_{CP}[1]	250	2 x t_{ICP}	500	ns

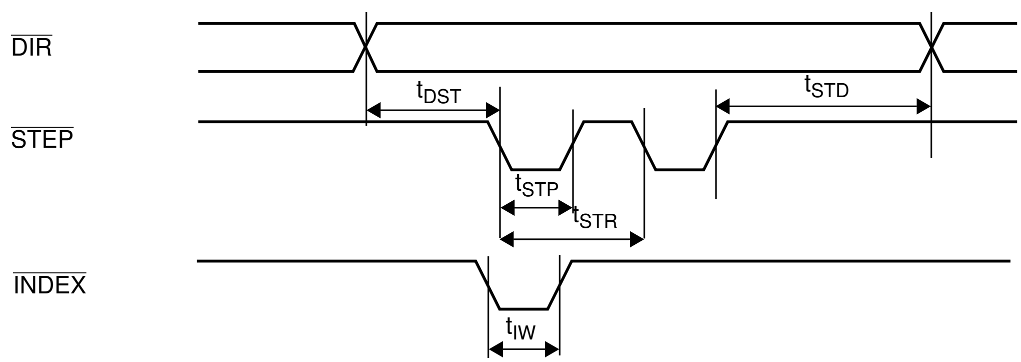
1. t_{CP} is the clock period defined for CLKIN in *Clock Timing* on page 241.

11.0 Device Characteristics (Continued)

FDC Drive Control Timing

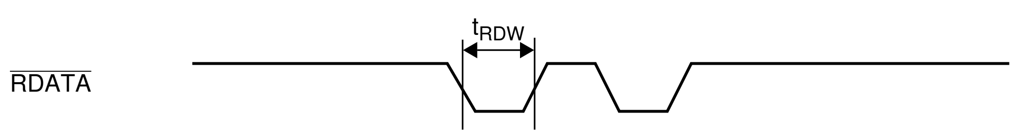
Symbol	Parameter	Min	Max	Unit
t_{DST}	$\overline{\text{DIR}}$ Setup to $\overline{\text{STEP}}$ Active[1]	6		µs
t_{IW}	Index Pulse Width	100		ns
t_{STD}	$\overline{\text{DIR}}$ Hold from $\overline{\text{STEP}}$ Inactive	t_{STR}		ms
t_{STP}	$\overline{\text{STEP}}$ Active High Pulse Width[1]	8		µs
t_{STR}	$\overline{\text{STEP}}$ Rate Time[1]	0.5		ms

1. Not tested. Guaranteed by design.



FDC Read Data Timing

Symbol	Parameter	Min	Max	Unit
t_{RDW}	Read Data Pulse Width	50		ns



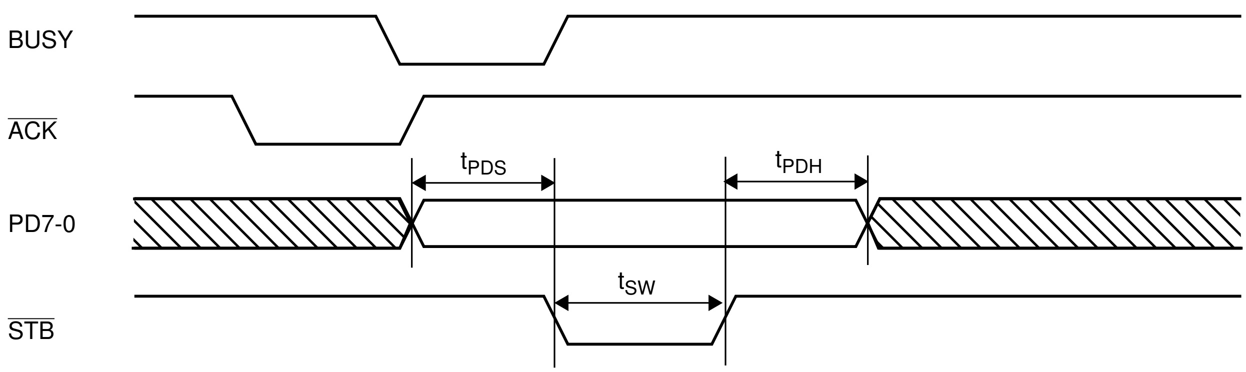
11.0 Device Characteristics (Continued)

11.5.8 Parallel Port Timing

Standard Parallel Port Timing

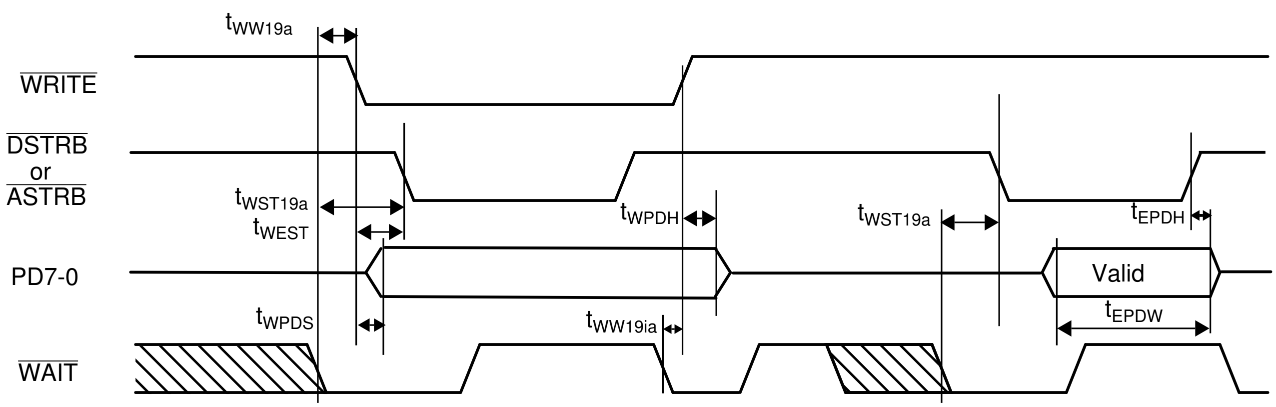
Symbol	Parameter	Conditions	Typ	Max	Unit
t_{PDH}	Port Data Hold	These times are system dependent and therefore are not tested.	500		ns
t_{PDS}	Port Data Setup	These times are system dependent and therefore are not tested.	500		ns
t_{SW}	Strobe Width	These times are system dependent and therefore are not tested.	500		ns

Typical Data Exchange



Enhanced Parallel Port Timing

Symbol	Parameter	Min	Max	EPP 1.7	EPP 1.9	Unit
t_{WW19a}	$\overline{\text{WRITE}}$ Active from $\overline{\text{WAIT}}$ Low		45		✔	ns
t_{WW19ia}	$\overline{\text{WRITE}}$ Inactive from $\overline{\text{WAIT}}$ Low		45		✔	ns
t_{WST19a}	$\overline{\text{DSTRB}}$ or $\overline{\text{ASTRB}}$ Active from $\overline{\text{WAIT}}$ Low		65		✔	ns
t_{WEST}	$\overline{\text{DSTRB}}$ or $\overline{\text{ASTRB}}$ Active after $\overline{\text{WRITE}}$ Active	10		✔	✔	ns
t_{WPDH}	PD7-0 Hold after $\overline{\text{WRITE}}$ Inactive	0		✔	✔	ns
t_{WPDS}	PD7-0 Valid after $\overline{\text{WRITE}}$ Active		15	✔	✔	ns
t_{EPDW}	PD7-0 Valid Width	80		✔	✔	ns
t_{EPDH}	PD7-0 Hold after $\overline{\text{DSTRB}}$ or $\overline{\text{ASTRB}}$ Inactive	0		✔	✔	ns



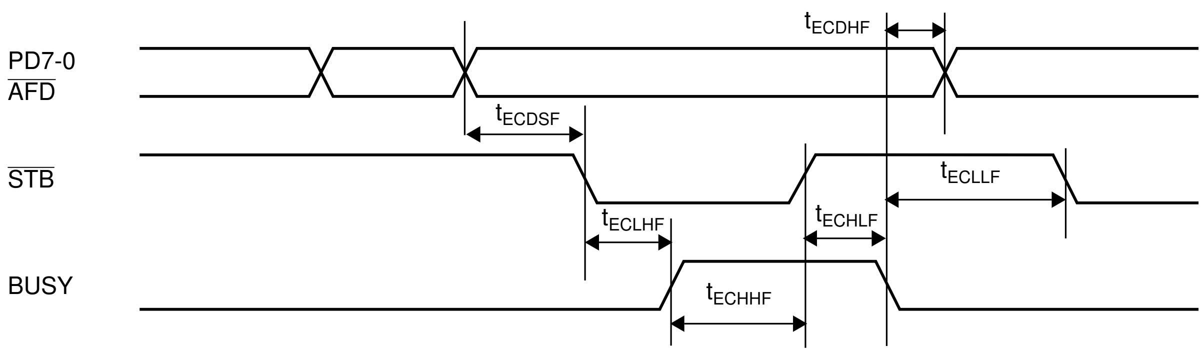
11.0 Device Characteristics (Continued)

Extended Capabilities Port (ECP) Timing

Forward Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSF}	Data Setup before $\overline{\text{STB}}$ Active	0		ns
t_{ECDHF}	Data Hold after BUSY Inactive	0		ns
t_{ECLHF}	BUSY Active after $\overline{\text{STB}}$ Active	75		ns
t_{ECHHF}	$\overline{\text{STB}}$ Inactive after BUSY Active[1]	0	1	s
t_{ECHLF}	BUSY Inactive after $\overline{\text{STB}}$ Active[1]	0	35	ms
t_{ECLLF}	$\overline{\text{STB}}$ Active after BUSY Inactive	0		ns

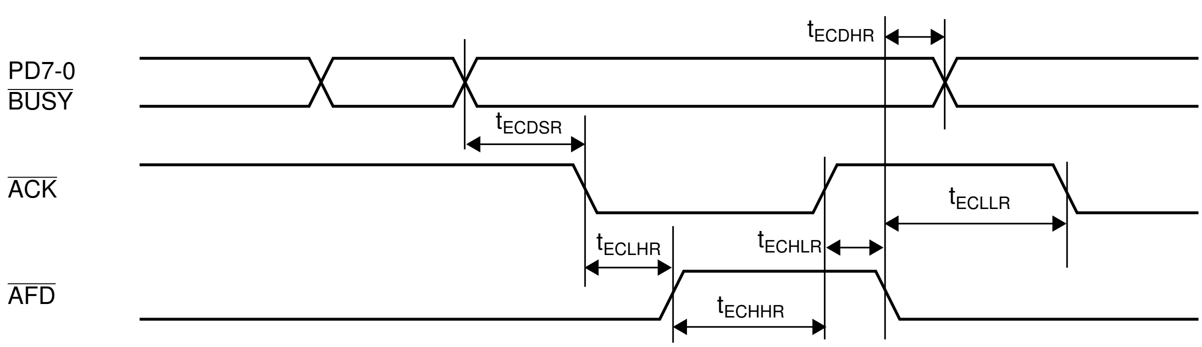
1. Not tested. Guaranteed by design.



Reverse Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSR}	Data Setup before $\overline{\text{ACK}}$ Active	0		ns
t_{ECDHR}	Data Hold after $\overline{\text{AFD}}$ Active	0		ns
t_{ECLHR}	$\overline{\text{AFD}}$ Inactive after $\overline{\text{ACK}}$ Active	75		ns
t_{ECHHR}	$\overline{\text{ACK}}$ Inactive after $\overline{\text{AFD}}$ Inactive[1]	0	35	ms
t_{ECHLR}	$\overline{\text{AFD}}$ Active after $\overline{\text{ACK}}$ Inactive[1]	0	1	s
t_{ECLLR}	$\overline{\text{ACK}}$ Active after $\overline{\text{AFD}}$ Active	0		ns

1. Not tested. Guaranteed by design.



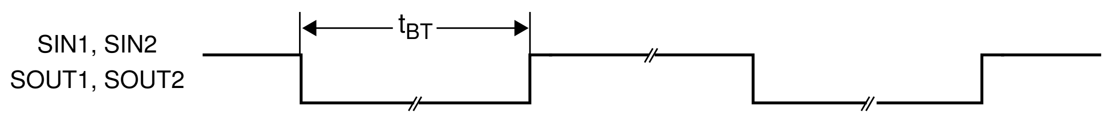
11.0 Device Characteristics (Continued)

11.5.9 Serial Ports 1 and 2 Timing

Serial Port Data Timing

Symbol	Parameter	Conditions	Min	Max	Unit
t_{BT}	Single Bit Time in Serial Port[1]	Transmitter	$t_{BTN} - 25^2$	$t_{BTN} + 25^2$	ns
		Receiver	$t_{BTN} - 2\%^2$	$t_{BTN} + 2\%^2$	ns

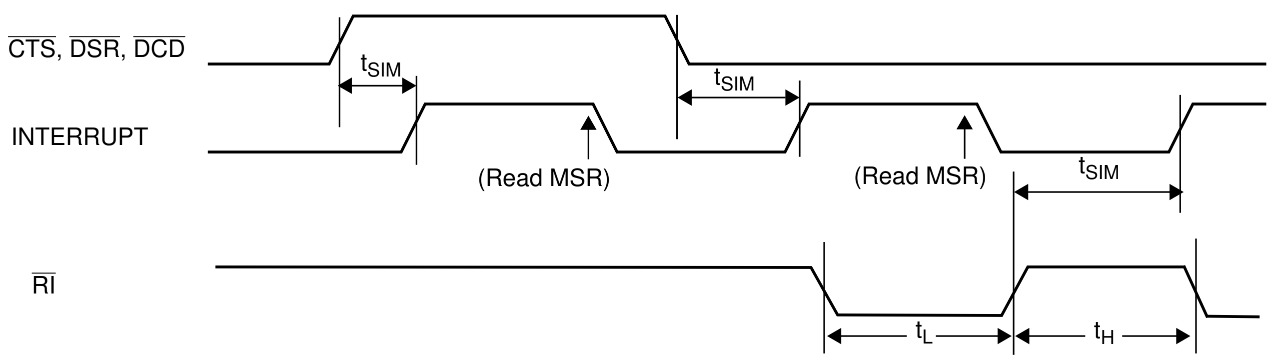
1. Not tested. Guaranteed by design.
2. t_{BTN} is the nominal bit time in the Serial Port; it is determined by the setting of the Baud Generator Divisor registers.



Modem Control Timing

Symbol	Parameter	Min	Max	Unit
t_L	$\overline{RI2,1}$ Low Time[1,2]	10		ns
t_H	$\overline{RI2,1}$ High Time[1,2]	10		ns
t_{SIM}	Delay to Set IRQ from Modem Input		40	ns

1. Not tested. Guaranteed by characterization
2. This value also applies to $\overline{RI2,1}$ wake-up detection in the SWC module.



11.0 Device Characteristics (Continued)

11.5.10 SWC Timing

Inputs at V_{SB} Power Switching

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{EWIV}	67	External Wake-up inputs valid[1]	At V_{SB} power On, after the 32 KHz clock is stable[2]	1 s	1.25 s
t_{PBOP}	68	$\overline{\text{PWBTOUT}}$ pulse time[1]	Resume by $\overline{\text{SLPS3}}$, $\overline{\text{SLPS5}}$ after Power Fail	100 ms[3],	100.03 ms

1. Not tested. Guaranteed by design.
2. No V_{BAT}; the 32 KHz internal clock is stopped while V_{SB} is Off (see *Low Frequency Clock Timing* on page 242).
3. Except when generated by $\overline{\text{PWBTIN}}$ pulse.

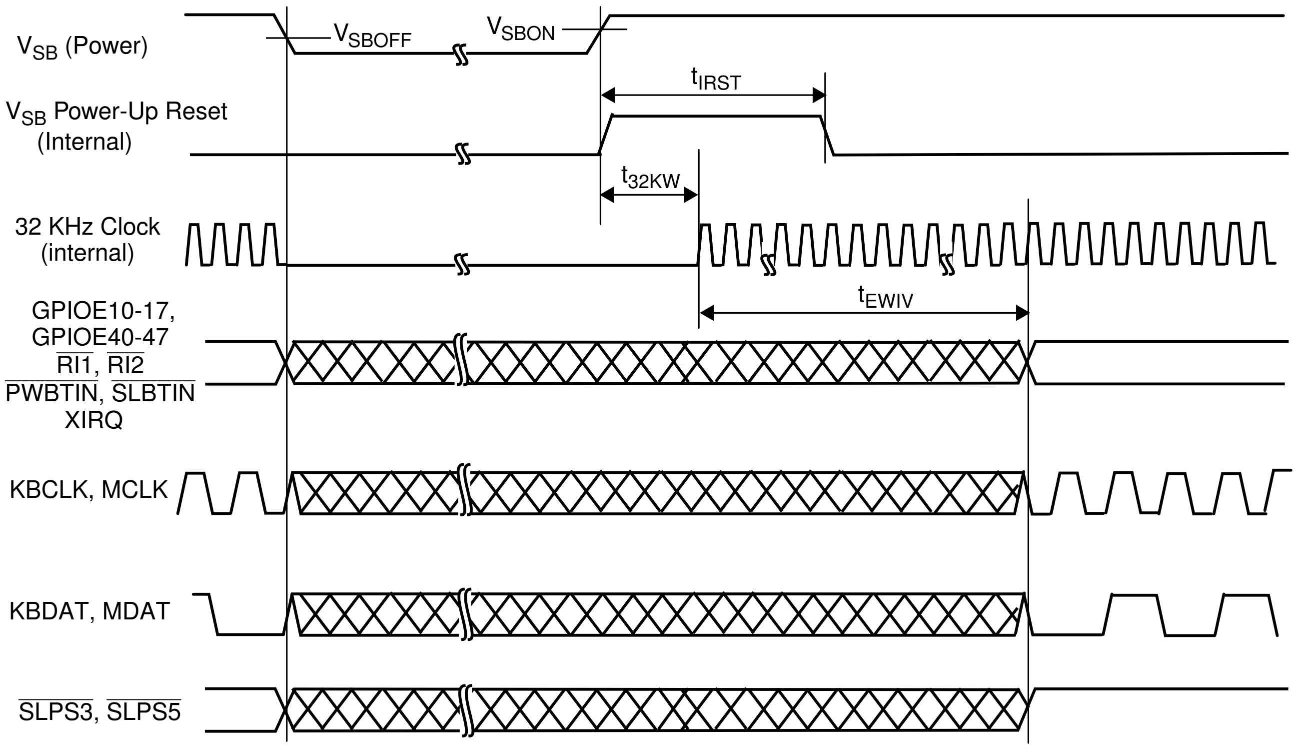


Figure 67. Inputs at V_{SB} Power Switching (No V_{BAT})

11.0 Device Characteristics (Continued)

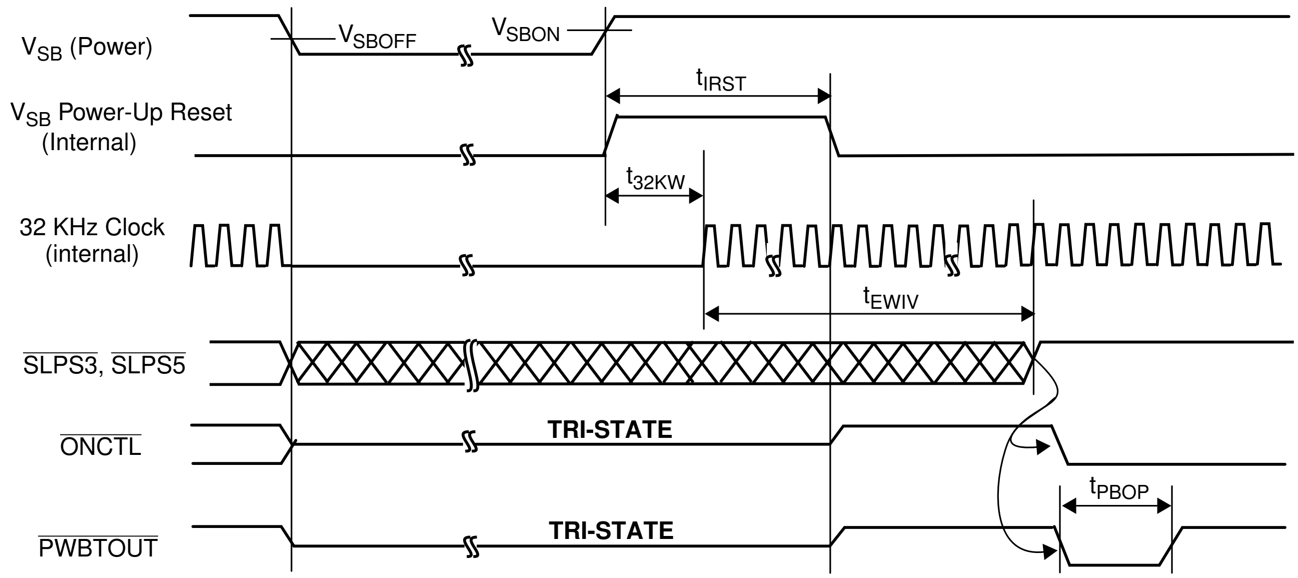


Figure 68. Resume by $\overline{SLPS3}$, $\overline{SLPS5}$, After Power Fail (No V_{BAT})

Wake-Up Inputs at V_{DD} Power Switching

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{EWIV}	69	External Wake-up inputs valid[1]	After V_{DD} power On	1 s	1.25 s
t_{VDFH}	69	VDDFELL high time[1]	After V_{DD} power Off	1 s	1.25 s
t_{KBMID}	69	Keyboard and Mouse Wake-up inputs disable[1]	After V_{DD} power Off, if VDDFELL is enabled	2 s	2.25 s

1. Not tested. Guaranteed by design.

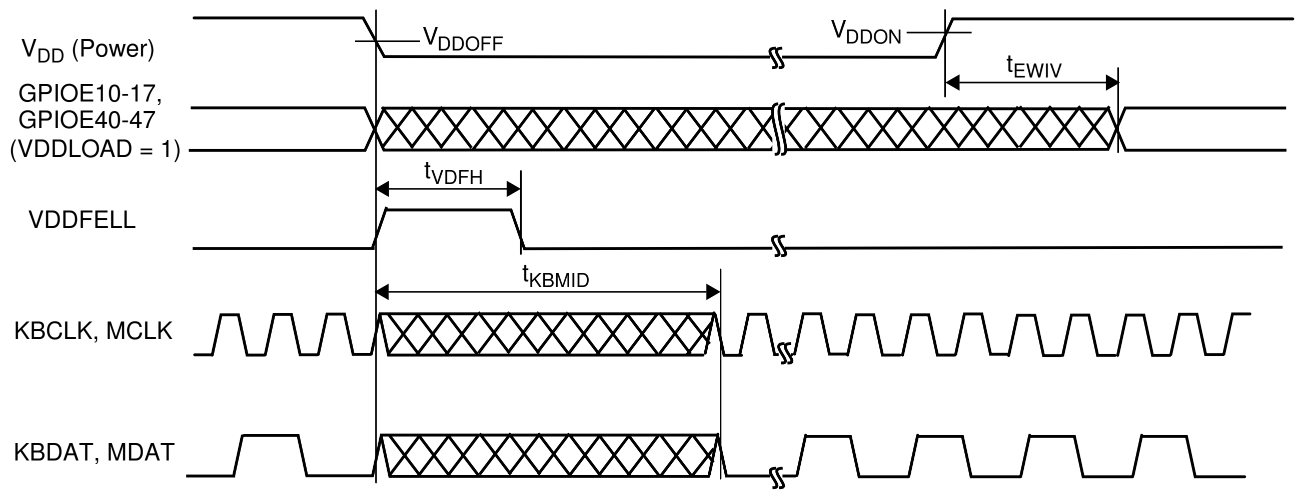


Figure 69. Wake-Up Inputs at V_{DD} Power Switching (VDDFELL Enabled)

11.0 Device Characteristics (Continued)

Power Button Override

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{PBOV}	70	Power Button Override[1]	After $\overline{\text{PWBTIN}}$ active	3.89 s	3.92 s
t_{OVEX}	70	Power Button Override Extension[1]	After the end of t_{PBOV}	0.2 s	0.24 s
t_{PBID}	70	$\overline{\text{PWBTIN}}$ disable time[1]	After a Power-Off event	1 s	1.25 s

1. Not tested. Guaranteed by design.

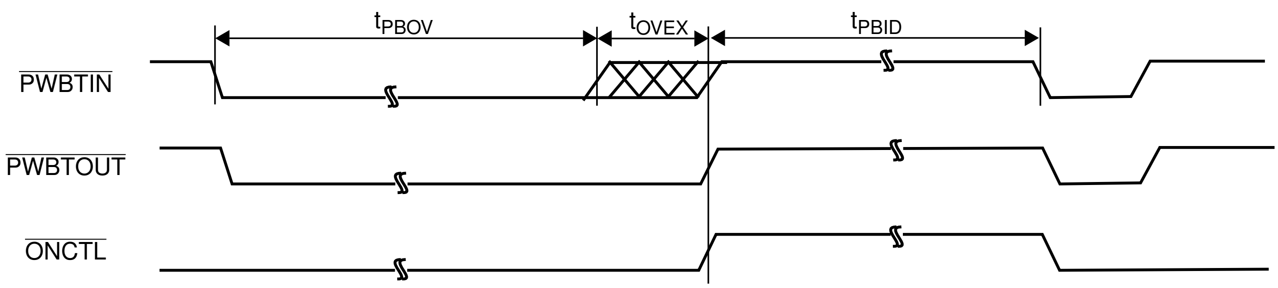


Figure 70. Power Button Override Timing

11.0 Device Characteristics (Continued)

Crowbar

Symbol	Figure	Description	Reference Conditions	Min	Max
t_{CBTO}	71, 72	Crowbar Timeout[1]	After $\overline{\text{ONCTL}}$ active, or V_{DD} power fall	0.5 s[2]	20 s[2]
t_{CBPBO}	71, 72	Crowbar generated, $\overline{\text{PWBTOUT}}$ pulse time[1]	After completion of Crowbar Timeout	4 s	4.25 s
t_{PBID}	71, 72	$\overline{\text{PWBTIN}}$ disable time[1]	After a Power-Off event	1 s	1.25 s

1. Not tested. Guaranteed by design.
2. Set by CRBAR_TOUT (see Section 9.3.11 on page 188).

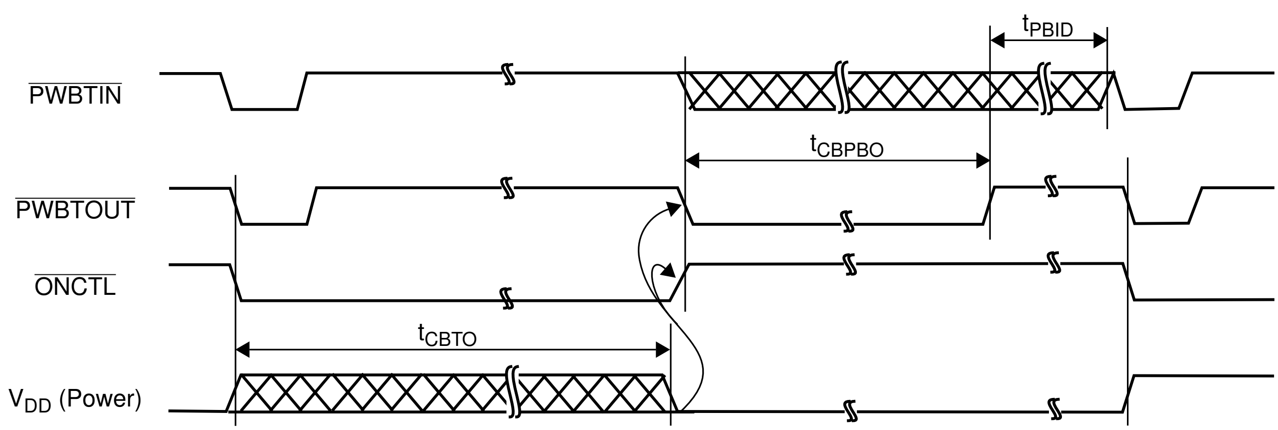


Figure 71. Power-On Crowbar Timing

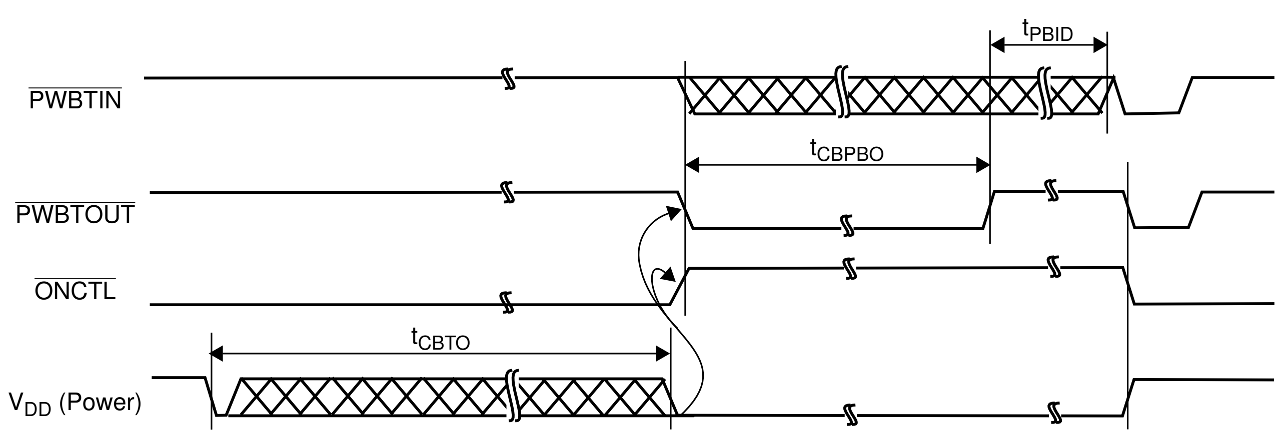
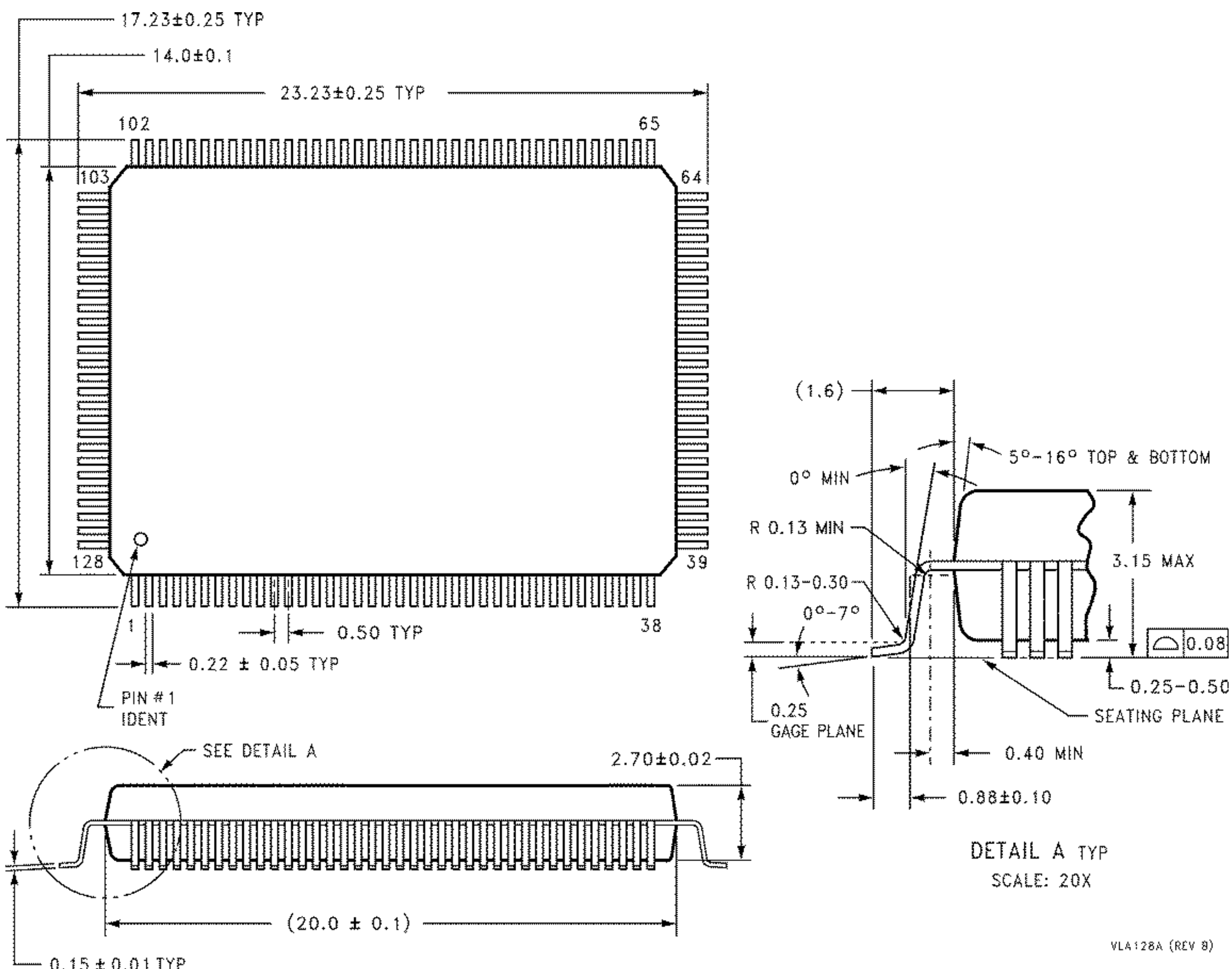


Figure 72. Power-Fall Crowbar Timing

Physical Dimensions

All dimensions are in millimeters



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