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ADO CONCENTRATOR

SERVICE MANUAL

AMPEX

Prepared by

AVSD Technical Publications
Ampex Corporation
401 Broadway
Redwood City, CA 94063

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Issued: September 1984

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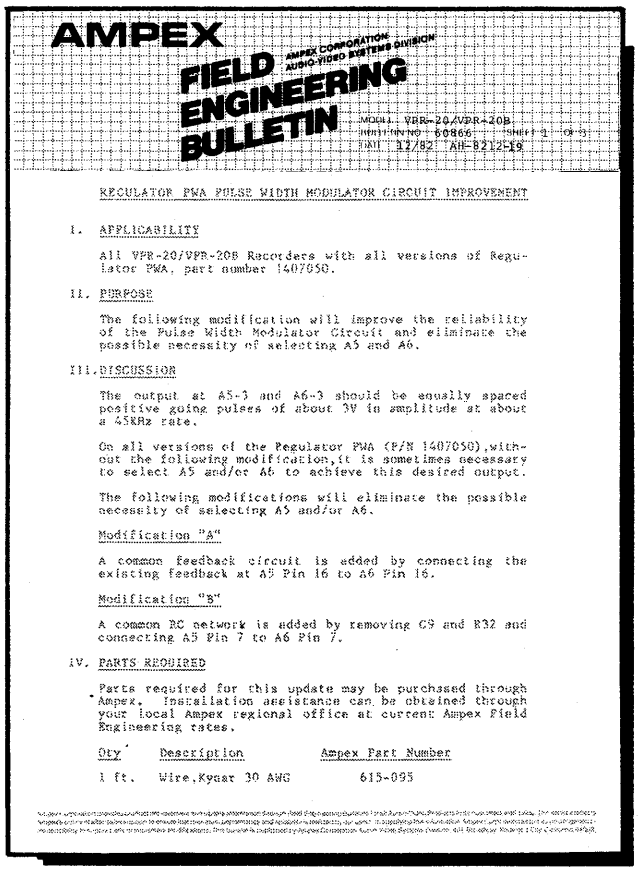

AMPEX

AMPEX CORPORATION AUDIO-VIDEO SYSTEMS DIVISION

FIELD ENGINEERING BULLETIN

MODEL: VPR-20/VPR-20B
MFG'S DWG NO: 60866 SHEET 1 OF 3
DATE: 12/82 AH-8212-19

REGULATOR PWA PULSE WIDTH MODULATOR CIRCUIT IMPROVEMENT

I. APPLICABILITY

All VPR-20/VPR-20B Recorders with all versions of Regulator PWA, part number 1407050.

II. PURPOSE

The following modification will improve the reliability of the Pulse Width Modulator Circuit and eliminate the possible necessity of selecting A5 and A6.

III. DISCUSSION

The output at A5-3 and A6-3 should be equally spaced positive going pulses of about 3V in amplitude at about a 45KHz rate.

On all versions of the Regulator PWA (P/N 1407050),without the following modification,it is sometimes necessary to select A5 and/or A6 to achieve this desired output.

The following modifications will eliminate the possible necessity of selecting A5 and/or A6.

Modification "A"

A common feedback circuit is added by connecting the existing feedback at A5 Pin 16 to A6 Pin 16.

Modification "B"

A common RC network is added by removing C9 and R32 and connecting A5 Pin 7 to A6 Pin 7.

IV. PARTS REQUIRED

Parts required for this update may be purchased through Ampex. Installation assistance can be obtained through your local Ampex regional office at current Ampex Field Engineering rates.

Qty	Description	Ampex Part Number
1 ft.	Wire,Kynar 30 AWG	615-095

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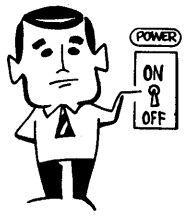
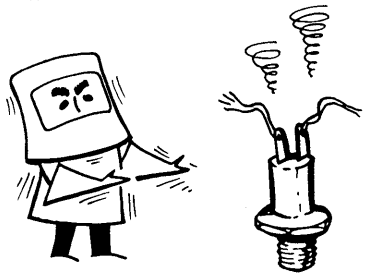
SAFETY AND FIRST AID SUGGESTIONS

Regardless of how well electrical equipment is designed, personnel can be exposed to **dangerous electrical shock** when protective covers are removed for maintenance or other activities. Therefore, it is incumbent on the user to see that all safety regulations are consistently observed and that each individual assigned to the equipment has a clear understanding of first aid related to electrical hazards.

In addition, the following safety practices must be followed:



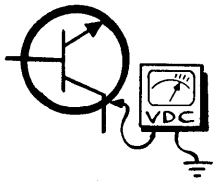
1 Do not attempt to adjust unprotected circuit controls or to dress leads with power **on**.



2 Do not touch heavily loaded or overheated components without precaution to avoid burns.

3 Do not assume that all danger of electrical shock is removed when power is **off**. Charged capacitors can retain dangerous voltages for a long time after power is removed. These capacitors should be discharged through a suitable resistor before any circuit points are touched.

4 Always avoid placing parts of the body in series between ground and circuit points.



5 Remember that some semiconductor cases and solid-state circuits carry high voltages.

6 Don't take chances. Be fully trained. Ampex equipment should be operated and maintained by fully qualified personnel.

If someone seems unable to free himself while receiving an electrical shock, **turn power off** before attempting to render aid. A muscular spasm or unconsciousness can make a victim unable to free himself from the electrical power.

WARNING

DO NOT TOUCH VICTIM OR HIS CLOTHING BEFORE POWER IS REMOVED OR YOU MAY ALSO BECOME A SHOCK VICTIM.

If power cannot be removed immediately, **very carefully** loop a length of dry nonconducting material (such as rope, insulating material, or clothing) around the victim and pull him free of the power. Carefully avoid touching him or his clothing until free of power. Immediately start the appropriate first aid procedures.

GOOD PRACTICES

In maintaining the equipment covered in this manual, please keep in mind the following standard good practices:

1 When connecting any instrument (oscilloscope, waveform monitor, etc.) to a high-frequency output, use the appropriate termination resistor at the input of the instrument, unless the instrument is terminated internally.

2 When inserting or removing printed wiring assemblies (PWAs), cable connectors, or fuses, always turn off power to the affected portion of the equipment. After power is removed, allow sufficient time for the power supplies to bleed down before reinserting PWAs.

3 When troubleshooting, remember that FETs and other metal-oxide-semiconductor (MOS) devices may appear defective because of leakage between traces or component leads on the printed wiring board. Clean the printed wiring board and recheck the MOS device before assuming it is defective.

4 When replacing MOS devices, follow standard practices to avoid damage caused by static charges and soldering.

5 When removing components from PWAs (particularly ICs), use care to avoid damaging PWA traces.

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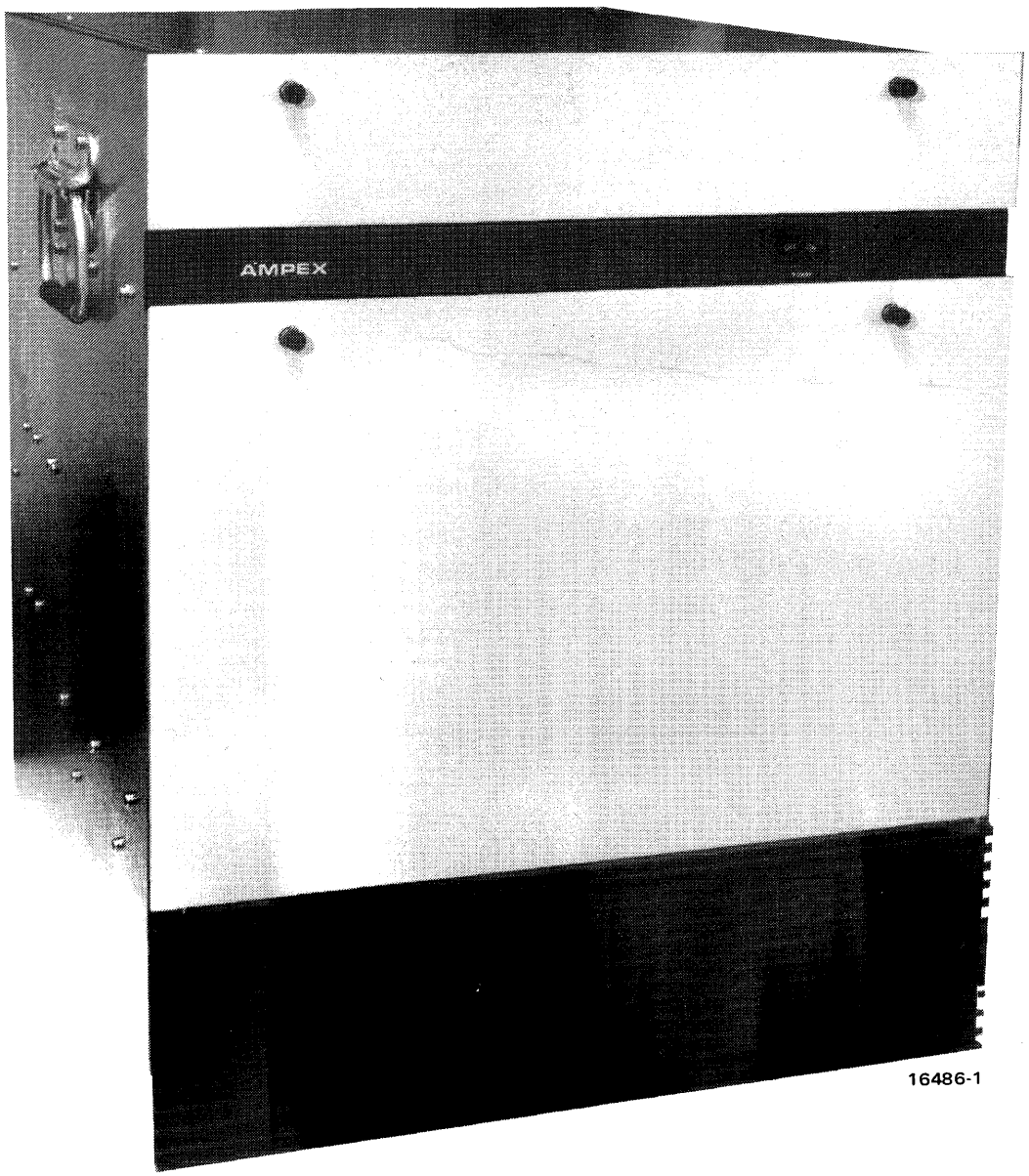


ADO Concentrator

SECTION 1
GENERAL INFORMATION

1-1 SCOPE OF THE MANUAL

This manual provides information to facilitate installation and maintenance of the Concentrator, Ampex Part No. 1464600. This unit is an accessory for, and is installed in, the Ampex Digital Optics (ADO) System. To avoid confusion, descriptions in this manual assume a four-channel concentrator connected to a system containing eight control units, four signal systems, and two hub boxes. (The Hub Box Assembly, Ampex Part No. 1464405, is also an ADO accessory.) Application of this information to other system configurations is always obvious.

1-2 PURPOSE OF THE EQUIPMENT

The purpose of the concentrator is to improve the quality of video effects produced by the system, to make them easier to produce, and to relieve the burden of work on the switcher.

1-3 CAPABILITIES

The concentrator makes possible something known as video channel combines. Combines consist of two to four channels combined in such a way as to make scenes in the various channels appear to be one behind the other. For example, Figure 1-1 illustrates a combine with scene B in front followed by scene A, which is followed by scene D. This combine appears over a gray background. The concentrator can supply a background of any color desired.

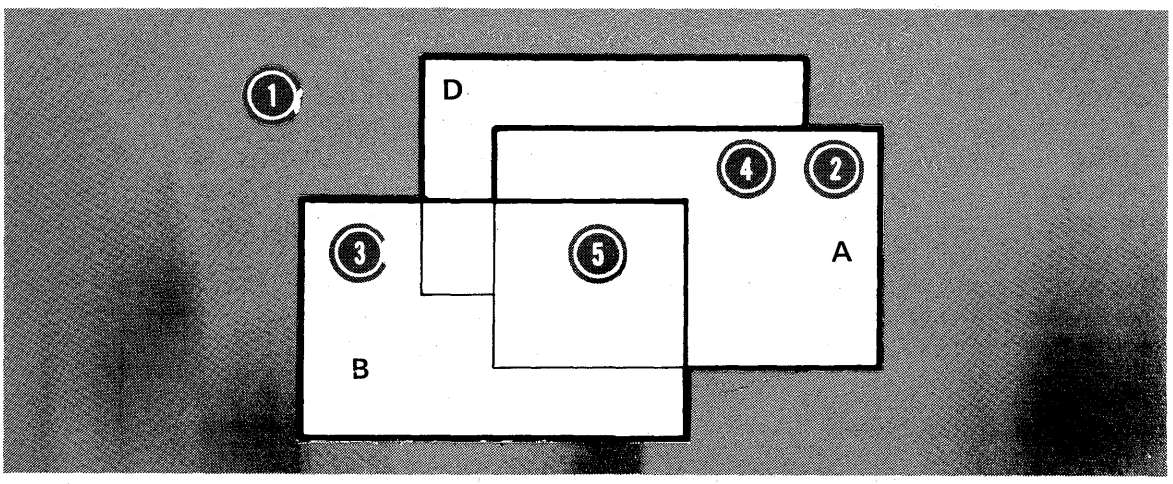


Figure 1-1. Combine Example

Channels in a combine can have various degrees of transparency. This allows scenes in back of others to partially show through, as is the case in Figure 1-1 which illustrates channels A and D showing through channel B. Channels can also be dimmed if desired. Changes in transparency and dimness of channels, like changes in priority, can be programmed to occur automatically.

Because timing differences between video channels are completely eliminated, combines produced by the concentrator come together perfectly. The concentrator can do soft edge keying when provided with a soft key from the signal system.

The concentrator can also produce two independent combines simultaneously. Of course, they must be controlled from two different control units and must use different video channels.

1-4 FUNCTIONAL DESCRIPTION

A concentrator, connected to an ADO system, receives digital video from channel A, B, C, and D signal systems. (See Figure 1-2.) The video is processed to produce combines and the processed video is returned to one or more of the signal systems supplying a video input for the combine. A combine can be programmed from any one of the eight control units and can use any combination of video inputs from channels A through D. Program data that defines a combine to be produced is fed to the concentrator from a control unit via a hub box. A remote terminal should be connected to the concentrator for diagnostic purposes.

1-5 PHYSICAL DESCRIPTION

The concentrator chassis contains power supplies, cooling fans, and a section for PWAs. (See Figures 1-3, 1-4, and 1-5.) The +5 volt and -5 volt supplies are for TTL and ECL circuits, respectively. The PWA section is accessed by a separate hinged panel. All connections to the concentrator chassis are made by connectors located at the rear of the unit.

1-6 STANDARD AND OPTIONAL EQUIPMENT

A standard concentrator contains the basic assembly, Ampex Part No. 1464402, a line voltage kit, and a two-channel kit. The line voltage kit may be either a 120-Vac kit or a 230-Vac kit. These are Ampex Part Numbers 1464407 and 1464408, respectively. Two-channel kits are available for NTSC/PAL-M and PAL-I applications. The two-channel NTSC/PAL-M kit is Ampex Part Number 1464409. The two-channel kit for PAL applications is Ampex Part Number 1464410.

Optional kits are available to convert standard concentrators to four-channel units. There are two such kits, one for NTSC/PAL-M and one for PAL applications. They are Ampex Part Numbers 1464403 and 1464557, respectively.

1-7 SPECIFICATIONS

Specifications for the concentrator are listed in Table 1-1. Ampex reserves the right to make product and specification changes at any time without notice.

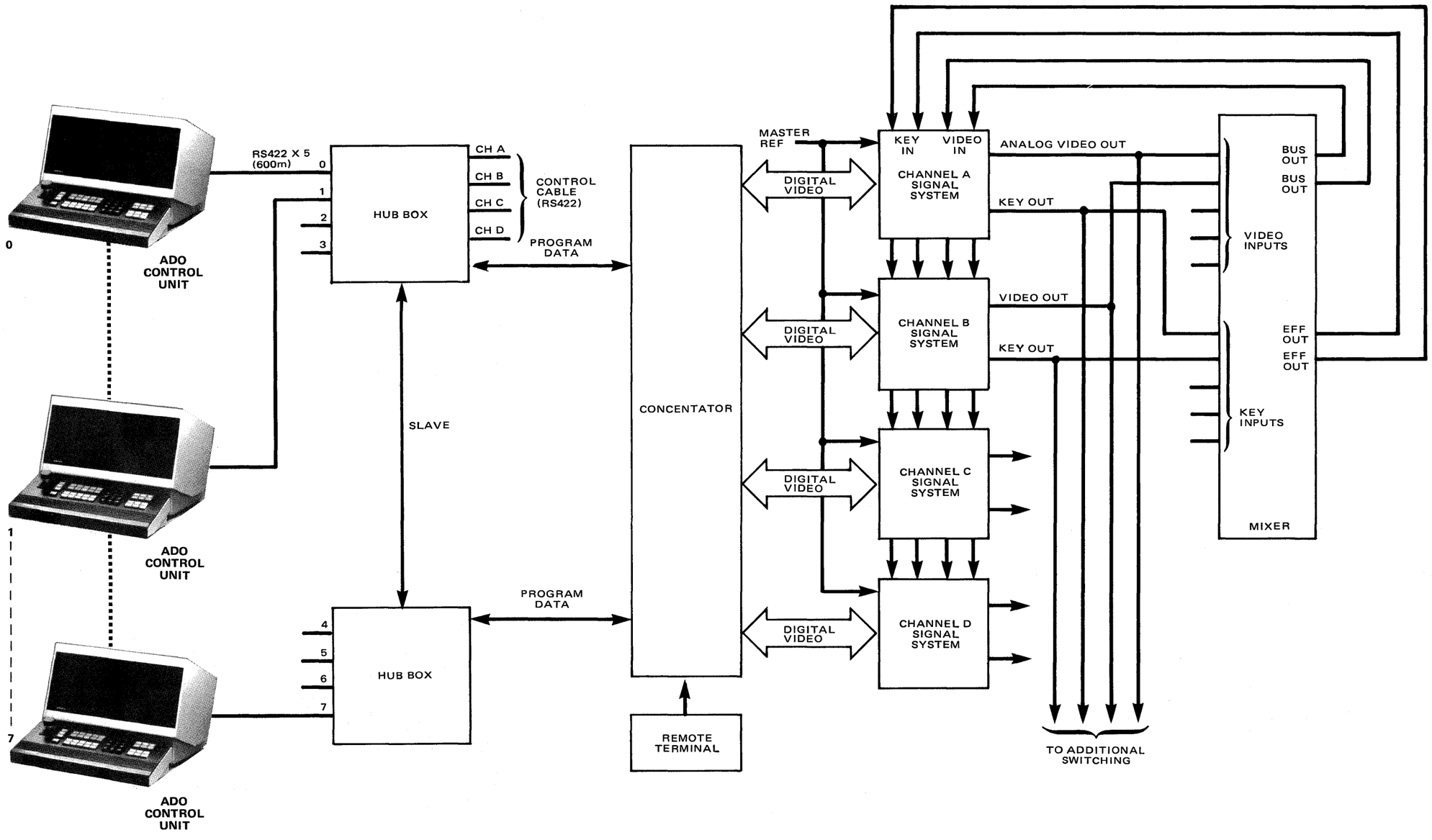


Figure 1-2.
Concentrator Interconnection Diagram

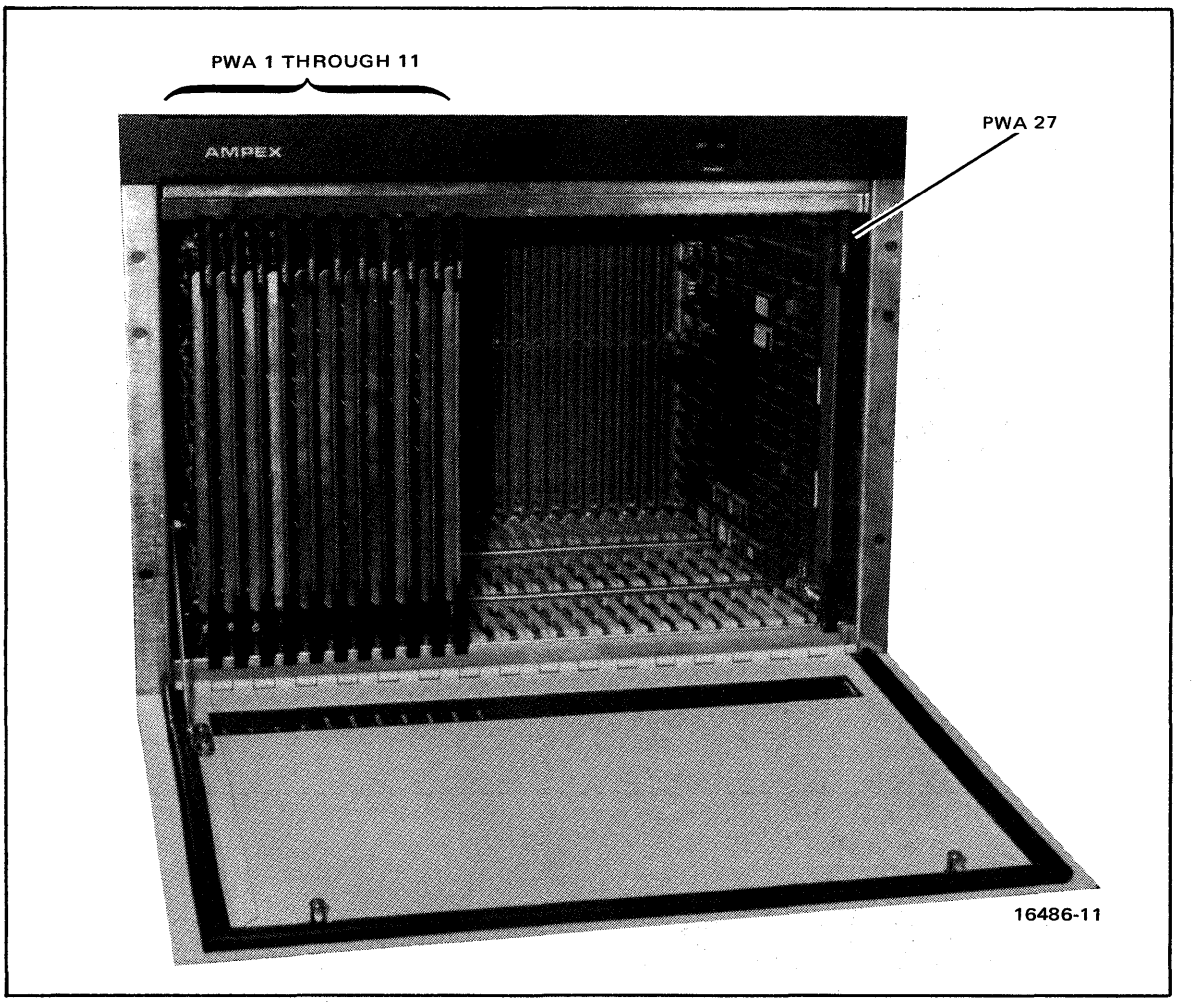


Figure 1-3. Concentrator—Front View

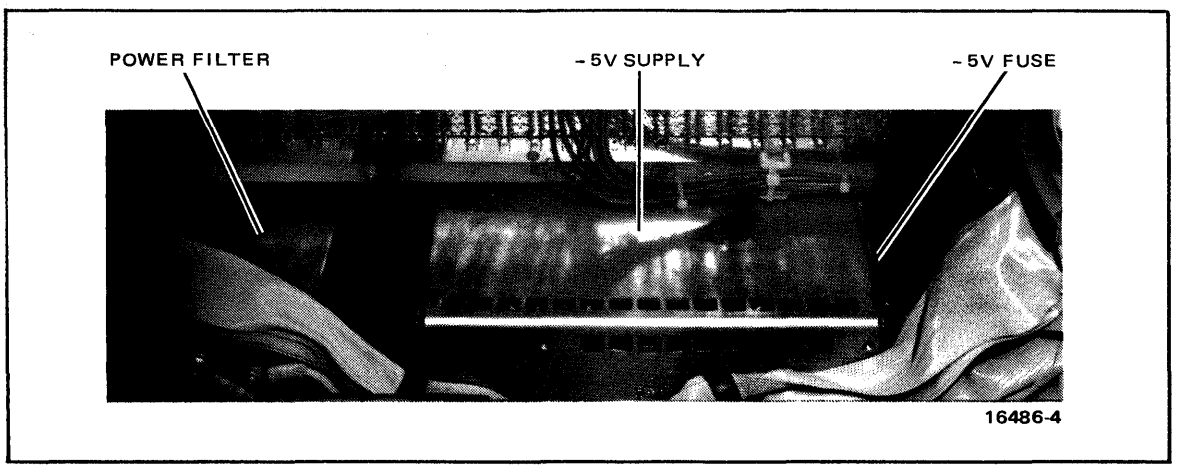


Figure 1-4. Concentrator—Rear View

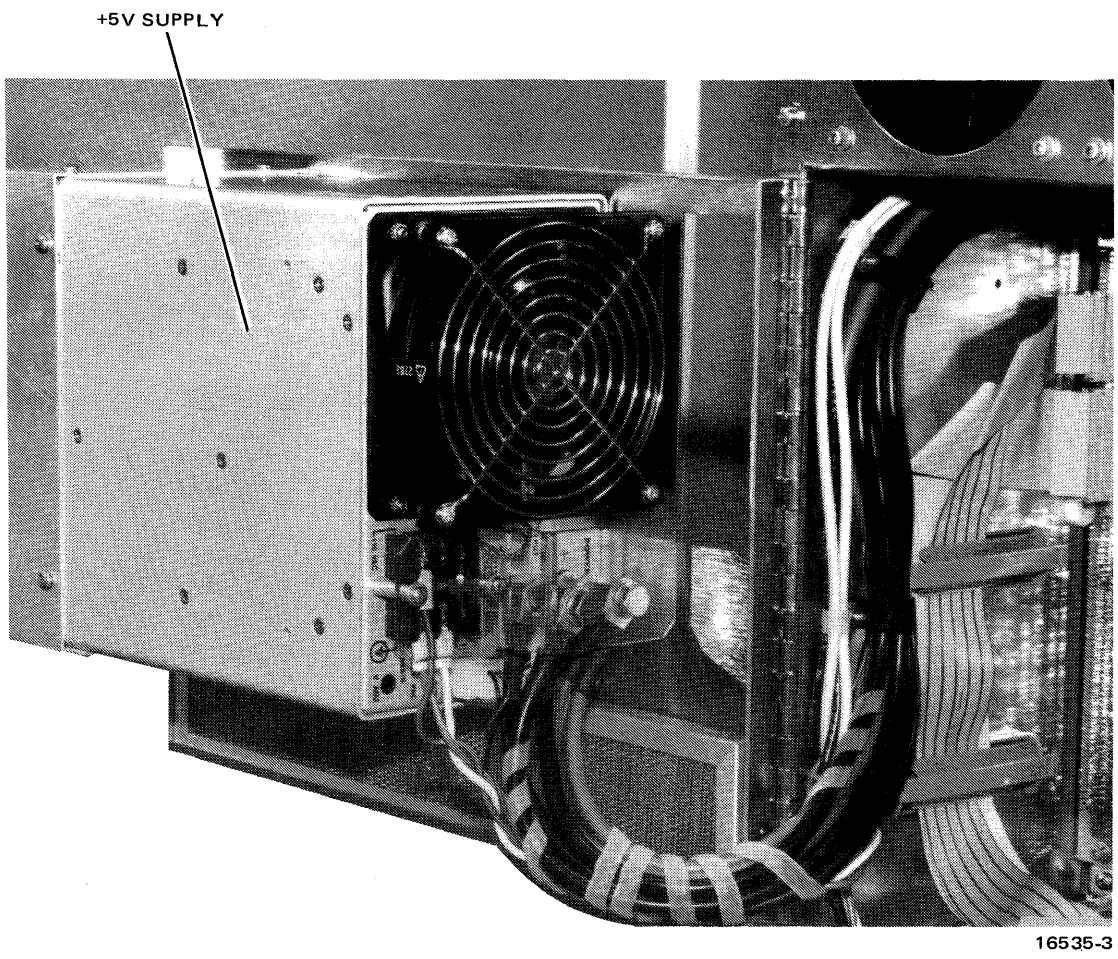


Figure 1-5. Concentrator Rear Door

Table 1-1. Specifications

Size:	22-3/4 in. x 19 in. x 22 in. (578 mm x 483 mm x 560 mm)
Weight:	151 lb (68 kg)
Power requirements:	Power requirements will vary depending on the options. The current will not exceed 30A at 120 Vac or 15A at 230 Vac in any case.

SECTION 2
INSTALLATION

This section provides information for unpacking, inspecting, mounting, and interconnection of the concentrator.

2-1 UNPACKING

The concentrator is shipped from the factory in a specially constructed packing case. Caution should be exercised in unpacking to prevent damage to cabinet finish or associated parts. Check contents of the packing case and check packing materials for accessory items. Check all items against the packing list to ensure shipment is complete. Carefully examine the contents for damage that may have occurred during shipment. Notify the carrier and the Ampex representative of any shortage or damages. If it is anticipated that equipment will be moved or reshipped, retain all shipping containers and packing materials.

2-2 INSTALLATION SITE

The area chosen for the concentrator should be adequately ventilated and relatively dust free. Cooling air is drawn into the front of the concentrator and is discharged at the rear. The concentrator should not be close to any strong electromagnetic fields. Common sources of interference include fluctuating loads on nearby high-current lines, fluorescent lighting, heavy duty transformers, elevator motors, and radio, television, and amateur radio transmitting equipment.

2-3 RACK-MOUNTING INSTRUCTIONS

WARNING

BECAUSE OF THE WEIGHT OF THE CONCENTRATOR CHASSIS, TWO OR MORE PERSONS ARE NEEDED TO LIFT THE UNIT INTO PLACE IN THE RACK. FOR CONVENIENCE WHILE INSTALLING THE RACK-MOUNTING SCREWS, USE A BLANK PANEL OR OTHER SUPPORT FOR THE UNIT.

The concentrator chassis is designed to mount in a standard 19-in. (483 mm) rack and occupy 22.75 inches (578 mm) of vertical rack space. For concentrator chassis dimensions, refer to Figure 2-1. Allow adequate space behind the unit for cable connection, air flow, and servicing.

Mount the unit into a rack as follows:

STEP 1 With the two doors closed, remove the two screws (A) that hold the grill to the bottom front of cabinet. (See Figure 2-2.)

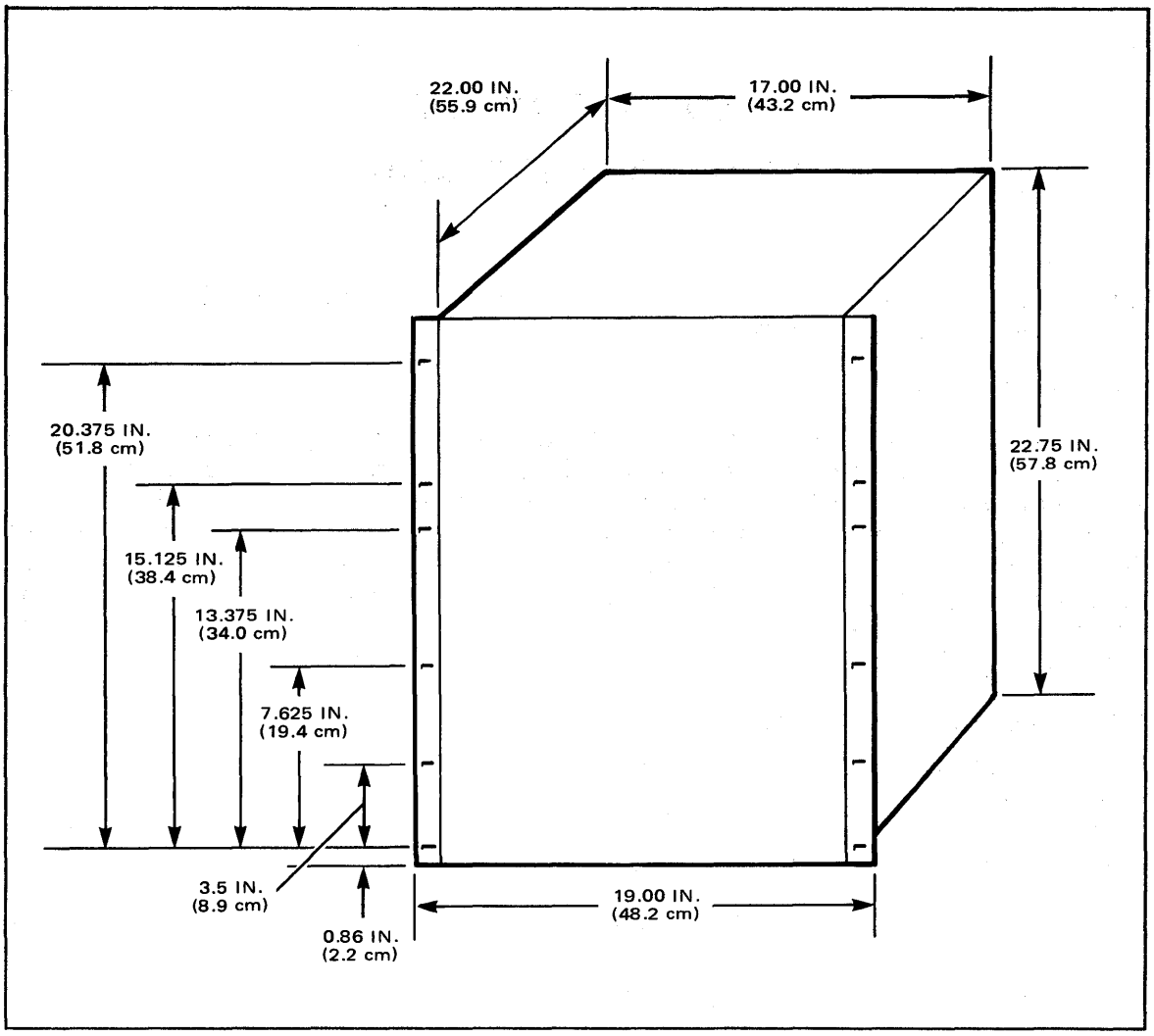


Figure 2-1. Concentrator Chassis Dimensions

STEP 2 Remove the two screws (B) that hold each of the two grill mounting clips.

Note

It is necessary to remove handles from sides of cabinet before mounting unit into rack (four screws each handle).

STEP 3 Place unit into the 19-in. rack and secure with four screws (B).

STEP 4 Turn latches (C) counterclockwise to release top door. Open door and install two mounting screws, one each side. Close and secure door.

STEP 5 Turn latches (D) counterclockwise to release bottom door. Open door and install six mounting screws, three each side. Close and secure door.

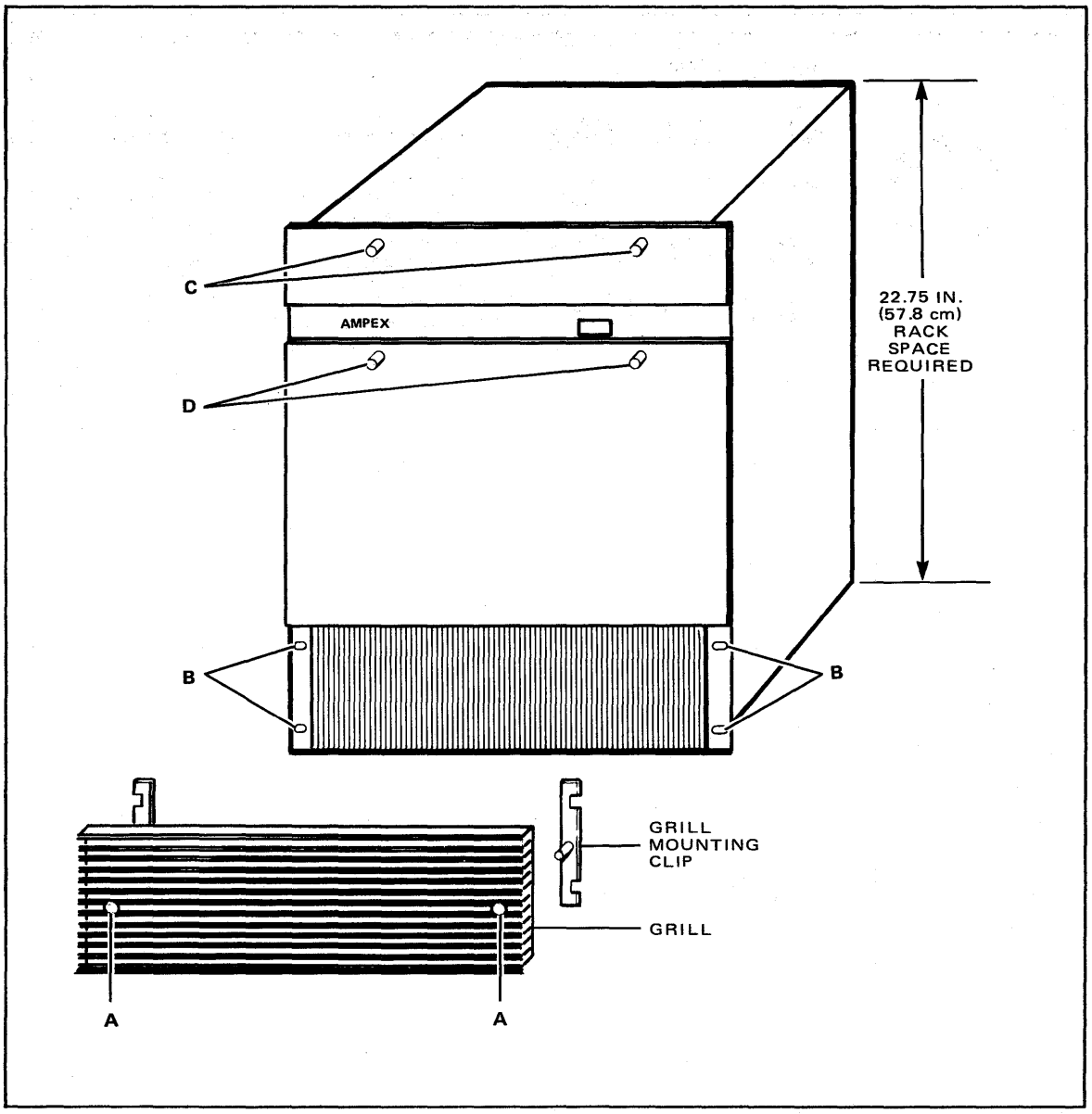


Figure 2-2. Concentrator Chassis

STEP 6 Loosen bottom four screws and install the slotted grill mounting clips. Tighten screws.

STEP 7 Reinstall grill (two screws).

2-4 POWER AND SIGNAL CONNECTIONS

All connections to and from the concentrator are made to connectors at the rear of the chassis. (See Figure 2-3.) These connectors and their functions are listed in Table 2-1.

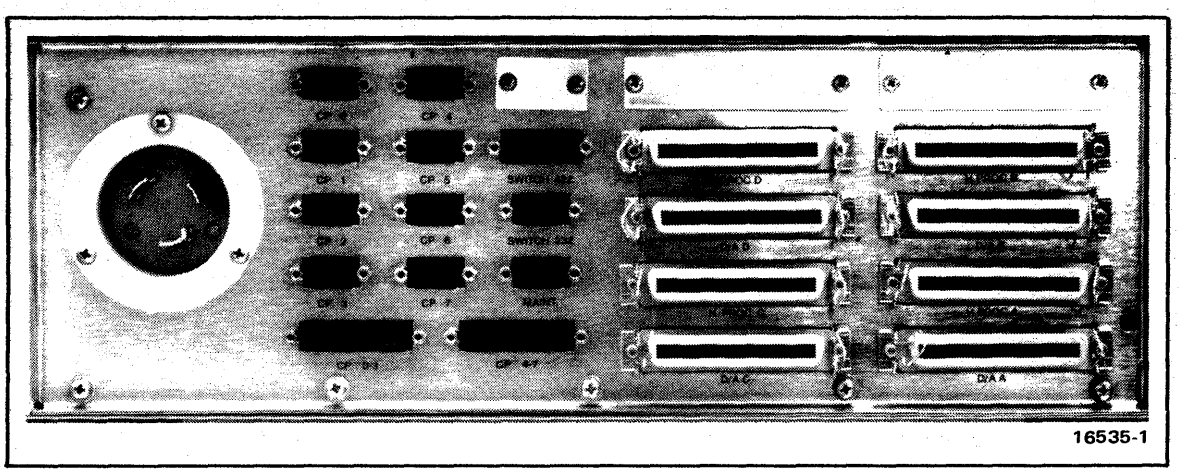


Figure 2-3. Concentrator Connectors

Table 2-1. Functions of Chassis Connectors

Connector	Function
H PROC A H PROC B H PROC C H PROC D	Digital video from channels A through D
D/A A D/A B D/A C D/A D	Digital video to channels A through D
CP 0 CP 1 CP 2 CP 3 CP 4 CP 5 CP 6 CP 7	Digital control data from control units 0 through 7
CP 0-3	Digital control data from control units 0 through 3 via the hub box
CP 4-7	Digital control data from control units 4 through 7 via the hub box

(Continued next page)

Table 2-1. Functions of Chassis Connectors (Continued)

Connector	Function
SWITCH 422	Not used in this application
SWITCH 232	Not used in this application
MAINT	Diagnostic routines from remote terminal

SECTION 3
THEORY OF OPERATION

3-1 INTRODUCTION

Note

Before reading Section 3, refer to paragraphs 1-3 and 1-4 for a description of capabilities and functions of the concentrator.

This section describes processing of digital video signals received from signal systems in the ADO format. An ADO channel contains seventeen digital lines designated Y0 through Y7, 9THBIT, and CK0 through CK7. For convenience, a brief description of these signals is presented here:

- The Y0 through Y7 lines represent luminance strength as a binary number. The most significant bit, carried by line Y7, is the sign bit with 0 and 1 representing positive and negative signs, respectively. The highest value the bits can represent is 01111111, which is equivalent to +127 to the base 10. The lowest value is 10000000, which in twos complement form is equivalent to -128.

- The 9THBIT line is used in two different ways. During sync pulses it is used to double the dynamic range of the luminance signal so that synchronizing waveforms can be generated by the same digital-to-analog converter that produces picture luminance. At certain other times it is used to carry serial digital control data from the signal system to the concentrator.

- The CK0 through CK7 lines alternately carry chrominance and key data. Key data is used in the ADO format to define the transparence of a channel as an inverse function. (The higher the value of the key number, the less transparent the channel.) Chrominance and key strength are represented as binary numbers with values from -128 to +127 in the same manner as luminance strength. When the key number is at its minimum value, -128, the channel is completely transparent. The highest number, +127, represents a completely opaque channel.

3-2 GENERAL

Video channel combines are produced in the concentrator by processing binary numbers representing picture elements. Channels to be combined are first synchronized so that binary numbers representing corresponding picture elements in different channels arrive at processing logic in the concentrator during the same cycle of processing clocks. Numbers representing corresponding picture elements are combined to produce new numbers to represent corresponding picture elements

in combined video. Numbers are combined by taking a percentage of each and adding the products. Total percentages taken for all numbers comes to 100%. This 100% includes the percentage of background that is summed. The process of reducing numbers to some percentage of their original value is referred to in this section as cutting.

3-3 SYNCHRONIZING VIDEO CHANNELS

Synchronization (with each other) of the video channels in a combine is necessary even though all video channels are generated in synchronization with a master reference. This is so because delays in cables and equipment cause small timing differences to accumulate. When a combine is made, the control unit operator selects one video channel as a reference. The concentrator then synchronizes other video channels in the combine with reference video.

Video channels in a combine are synchronized with reference video in the I/O PWAs. Digital video from channels A, B, C, and D is fed to I/O PWAs in slots 1, 2, 3, and 4, respectively. (See Figure 3-1.) Along with each video channel is a LINE REF signal which defines the timing for that channel. Timing signals derived from the LINE REF signals are fed from each I/O PWA to the clock PWA. The timing signals from the reference channel are refined and returned to the I/O PWAs for all channels in the combine. The I/O PWAs then synchronize their video outputs with these timing signals. The LINE REF signal for each channel is a direct result of the output video reference signal applied to each channel.

3-4 CUTTING

The amount that a number, representing a picture element from a channel, is cut depends to a large degree on the key of the channel at that picture element. For example, in Figure 1-1 point 1 is on the background. The numbers from all three channels will be cut to 0% for this point since the key will be the minimum value of 10000000. At point 2, 100% of the channel A number will be added to 0% of the channel B and D numbers. At point 3, the channel B number will be cut slightly and the channel A and D numbers will be cut to 0%. If a key of 01011111 is assumed for channel B, the channel B number will be cut to 87.5% at point 3.

The position of the channel, in the front to back sequence of channels in a combine, also affects how a number is cut. This is referred to as the priority of the channel. For example, in Figure 1-1 channel B has the highest priority, channel A is second, and channel D has the lowest priority. The channel D number at point 4 is cut to 0% since it has a lower priority than channel A, which is completely opaque with a key of 01111111 at this point. The channel A number at point 5 is cut to 12.5% since it has a lower priority than channel B, which has a key of 01011111 at this point.

Cutting is accomplished by first processing key data according to priority and then multiplying bytes of processed key data by bytes of corresponding luminance and chrominance data. Binary numbers representing key are first converted to binary fractions to make them compatible with ICs that perform the arithmetic functions. In the binary fraction notation, the maximum value of a number is one, written as 1.0000000, and the minimum value is zero, written as 0.0000000.

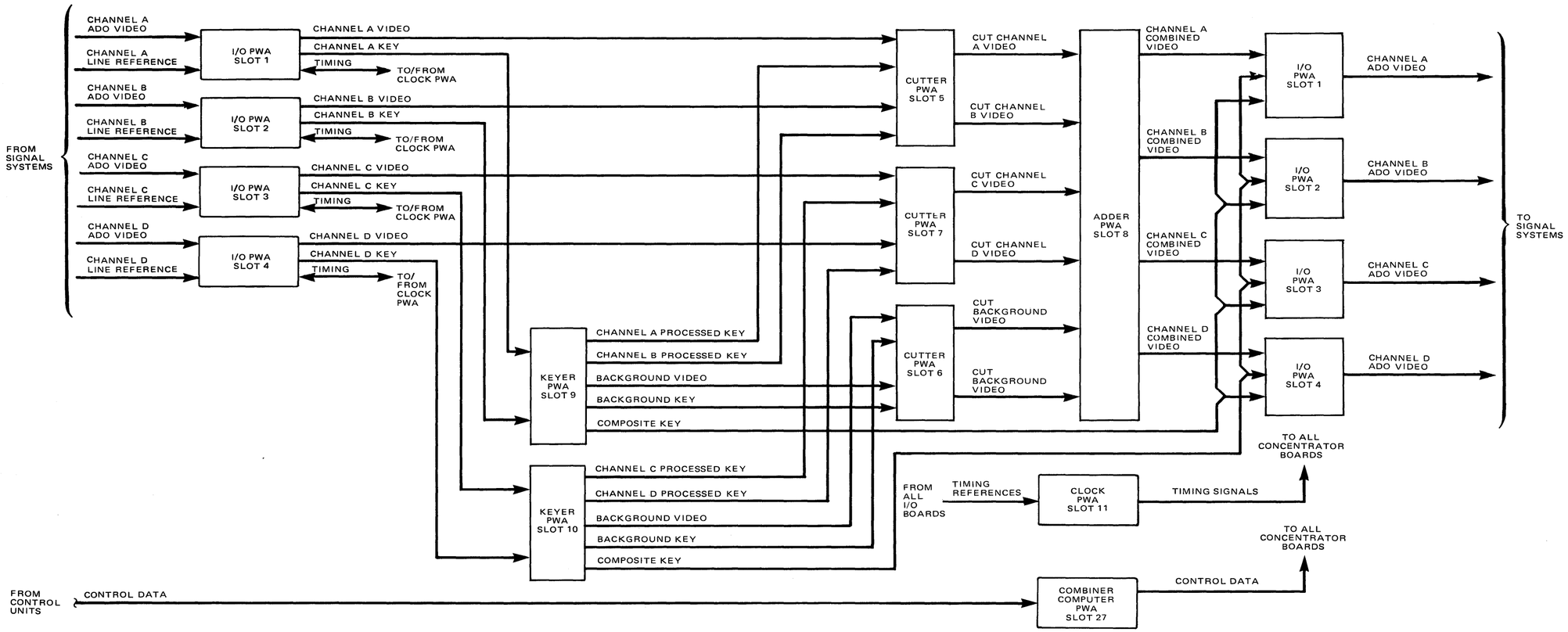


Figure 3-1.
Concentrator Block Diagram

Key data received with chrominance in video channels A through D is demultiplexed by the I/O PWAs and fed to Keyer PWAs. (Refer to Figure 3-1.) Keyer PWAs convert the key data to the binary fraction form. The Combiner Computer PWA sends control data to Keyer PWAs, thereby defining the priority of channels for each of two combines. The key input for each channel is then converted to a processed key output, reflecting its priority in a combine. The processed key for each channel is fed to a Cutter PWA which also receives luminance and chrominance data for the channel. Luminance and chrominance bytes are multiplied by the corresponding key bytes to produce cut video outputs.

In addition to processing key data for each channel, the Keyer PWAs also produce two background video signals. One of these is available for each of the two combines which can be produced simultaneously. A key signal is produced for each background to cut areas in the raster covered by channel video inputs. The background video and key signals are fed to a Cutter PWA in slot 6 which cuts these video signals.

3-5 ADDING

Cut video data is added by the Adder PWA in slot 8. This PWA contains circuitry for performing two adding operations simultaneously. Any combination of inputs can be fed to either adder section. The outputs of either adder section can be fed to any of the four channel outputs.

A video combine from the Adder PWA is fed to the same I/O PWAs that provided video for the combine. The control unit operator can select signal systems that are to receive the combined video. Gating in I/O PWAs is provided to select combined video from the Adder PWA to feed back to the analog section of the signal system. Gating may also select the input from the digital section of the signal system to feed back to the analog section. In this case, the video is first synchronized with the combined video.

Gating into and out of the adder sections, and gating in the I/O PWAs that select video to feed to signal systems, is controlled by data from the Combiner Computer PWA.

3-6 I/O PWA

An I/O PWA provides an interface between one signal system and the concentrator. There are four slots in the concentrator for these boards, enabling the concentrator to be connected to up to four signal systems at a time. A board receives a digital video signal from the digital chassis of the associated signal system. The video signal is received in the ADO format. It is delayed by the board to bring it into synchronization with other video signals in the same combine. (Although all video signals are generated in sync with the house master reference, delays in equipment and cables cause small differences in timing to accumulate. These differences are eliminated by this synchronizing function.) The synchronized video signal is then reformatted for processing by other types of concentrator boards. When processing by other boards is complete, the video signal is returned to the I/O board. It is then

restored to the ADO format and fed to the analog chassis of the associated signal system. Delays produced by processing, after initial synchronization, are the same for all video signals in the same combine. Consequently, outputs of a combine to analog chassis are synchronized with each other.

Under some ADO system operating conditions, the video signal received by an I/O board from a signal system is not processed by other concentrator boards. In this case, the video signal is looped through the I/O board to become the output back to the signal system. A video signal that is looped through may be synchronized with its own LINE REF signal or it may be synchronized with video signals in other I/O boards, as already mentioned. Then it is delayed, to compensate for the time used to further process the other video signals, and fed to the analog chassis in synchronization with them.

In addition to the video processing functions of the I/O board, the board also stores control data received from the signal system. The data is stored in a RAM in the I/O board which is accessible to the Combiner Computer PWA.

3-7 Synchronization of Digital Video Inputs

Input video signals on I/O boards are synchronized with each other by delaying them an appropriate amount of time. One video input which has been selected as the reference is delayed a fixed amount. Video signals that are leading the reference are delayed more and lagging signals are delayed less, as necessary, to bring them into synchronization with the reference. Video signals are delayed by storing each byte of video data into a memory as it is received and then reading it out a short time later. Each I/O board contains a memory for this purpose. The memory on the board receiving the reference video alternates between read and write cycles. As each byte is received it is loaded into memory following a fixed sequence of addresses. After each loading, a byte which was stored a short time previously is read out. Read addresses follow the same sequence as write addresses but the read sequence trails the write sequence by a fixed number of write/read cycles. The delay produced by this storage scheme equals the number of cycles by which a read address trails the previous write address times the byte period.

The amount of delay required to synchronize other video signals with the reference video signal is achieved by the method of memory addressing. The address generated to store each byte, as it is received, is established by the location of the corresponding picture element in a frame. Addresses generated to read bytes from the delay memory are in step with read addresses generated on the I/O board receiving the reference video. Consequently, corresponding bytes in different video channels may be stored at different times but they are read out together.

Input video data is stored in the YCK RAM and the 9THBIT RAM to produce a delay. (See Figure 3-2.) The data is received by an I/O board on 17 parallel lines. Luminance lines Y0 through Y7, 9THBIT, and lines which carry chrominance and key data, CK0 through CK7, are fed to the input register. Bytes are clocked into this register by the DATACLK signal. This is a byte-time clock which is derived from input video clock ICLK by the arbitrator. Outputs of the input register are written into the YCK RAM or the 9THBIT RAM in the case of the 9THBIT signal by WRITE pulses. The arbitrator guarantees there is a write pulse for every byte of data.

Data carried on the 9THBIT line is not affected by video processing, which produces combines. Consequently, this line is always looped through the I/O board and fed back to the signal system with the processed version of the Y and CK data with which it was received. The 9THBIT data is stored in a separate RAM because this data is delayed longer than data stored in the YCK RAM. The additional delay compensates for time used to process Y and CK data. Control data carried on the 9THBIT line goes directly to the 9THBIT decode logic and is not affected by the delay.

3-8 Write Addresses

Write addresses are produced by the write address counter. This counter is preset to the highest address in use by the ECL INPUT PRESET pulse. (The highest address in use is NTSC/PAL-dependent.) The preset pulse is detected during the same picture element in each frame. After the preset the counter is decremented, at the byte rate, by the ICLK clock. After decrementing to zero, the counter presets to the highest address in use on the next ICLK pulse and then continues decrementing and presetting in this manner. When another preset pulse is detected in the next frame, it should find the counter at the preset address. Since write counters on all I/O boards are preset at the same picture element in their respective video inputs, corresponding picture elements are stored in the same addresses on all boards.

The ECL INPUT PRESET pulse is detected in control data received on the 9THBIT line. This line is fed to the 9THBIT decode logic which detects the pulse and produces the TTL INPUT PRESET pulse. This pulse is converted from TTL to ECL by the board clocks and control generator to produce the ECL INPUT PRESET pulse.

The preset number comes from the combiner computer. It is the same on all I/O boards. It is fed from the computer to the MCHBUS interface on the D0 through D7 lines. It is stored in a MCHBUS interface register selected by the A0-A7 lines. The register output is fed to the write address register on the L0 through L7 lines.

Write addresses from the write address counter are fed to the YCK address generator and the 9THBIT address generator on the W0 through W7 lines. When the state of the R/$\overline{W}$ signal to these address generators indicates a write cycle, the address is gated through. It is fed from the YCK address generator to the YCK RAM on the J0 through J7 lines and from the 9THBIT address generator to the 9THBIT RAM on the N0 through N7 lines.

3-9 Read Addresses

YCK RAM and 9THBIT RAM read addresses on I/O boards are synchronized with their counterparts on all other I/O boards. Read addresses for the YCK RAM and 9THBIT RAM are produced by the YCK address generator and the 9THBIT address generator, respectively. All read addresses on all I/O boards are preset at the same time, near the beginning of a frame, by the OUTPUT PRESET pulse. The YCK RAM addresses are preset to a number on the E0 through E7 lines and the 9THBIT RAM addresses are preset to a number on the B0 through B7 lines. The E0 through E7 numbers are the same on all boards as are the B0 through B7 numbers. After

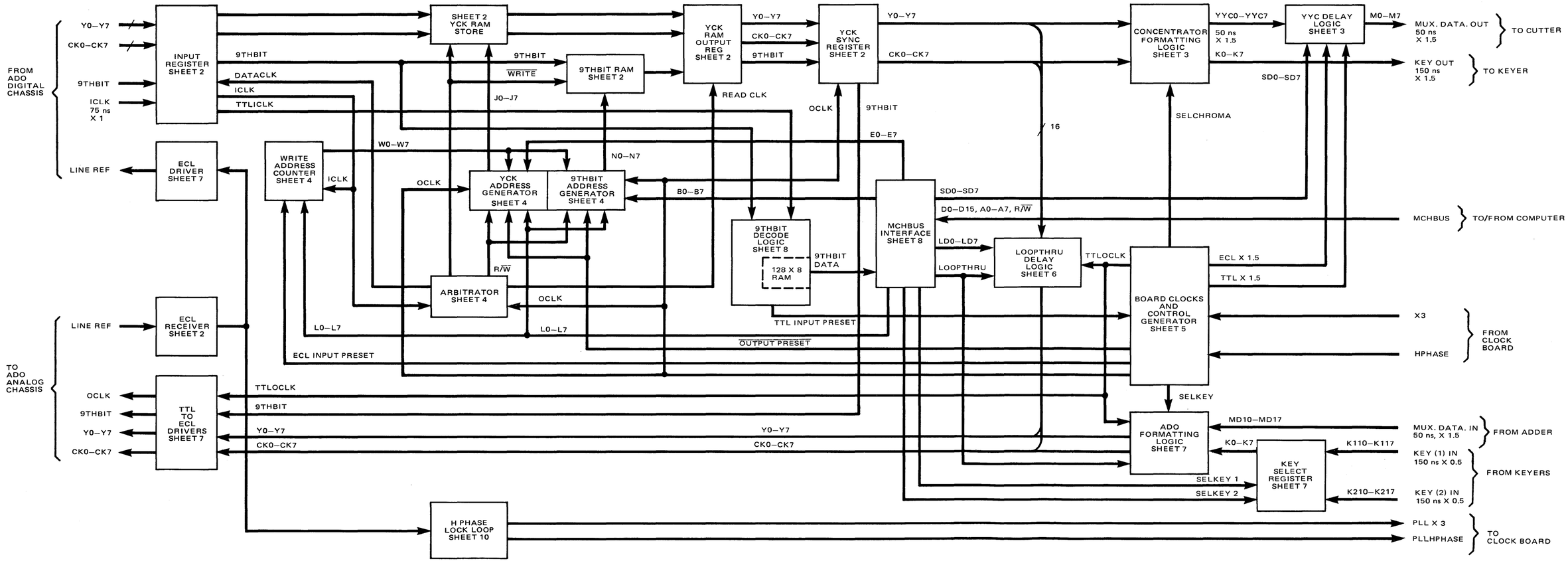


Figure 3-2.
I/O PWA Block Diagram

preset by the OUTPUT PRESET pulse, the addresses are decremented in step with read addresses on other boards by the OCLK clock. After decrementing to zero, read addresses are preset to the highest address in use. This is the same number used to preset the write address counter and is fed to the address generators on the L0 through L7 lines. After the preset, read addresses continue to decrement and recycle in the same manner as write addresses.

The OUTPUT PRESET pulse is generated by the board clocks and control generator. This pulse is derived from X3 IN and HPHASE IN signals from the clock PWA. X3 IN and HPHASE IN signals in turn are derived from the LINE REF signal fed to the I/O board receiving reference video. The LINE REF signal to an I/O Board is a composite sync from the analog chassis of the associated signal system. It is fed to the H phase lock loop. The loop generates X3 OUT and HPHASE OUT signals which are phase locked to the LINE REF input. These signals are fed to the Clock PWA. The Clock PWA selects X3 OUT and HPHASE OUT signals from the I/O board receiving the reference video and gates them back to all I/O boards. Since all boards generate the OUTPUT PRESET pulse from the same inputs, this pulse occurs simultaneously on all boards.

When the OUTPUT PRESET pulse occurs, the reference video signal is always at the same picture element. Consequently, the reference video write address is always the same at this time. The value of the E0 through E7 number is selected to make the read addresses for reference video trail write addresses for reference video by the desired number of write/read cycles. The value of the B0 through B7 number is selected to trail the E0 through E7 number as required to compensate for video processing time in the concentrator. This causes 9THBIT RAM outputs to be in step with processed video bytes fed back to the signal system.

Preset numbers come from the Combiner Computer PWA. The E0 through E7 number is fed to the MCHBUS interface on the D8 through D15 lines. D0 through D7 lines carry the B0 through B7 number to the interface. These numbers are stored in registers in the interface which are selected by address lines A0 through A7.

The OCLK clock, which decrements read addresses, is produced by the board clocks and control generator. This signal, like the OUTPUT PRESET signal, is derived from the X3 IN and HPHASE IN signals, making it synchronous with its counterpart on all I/O boards.

Read addresses are fed to the YCK RAM on the J0 through J7 lines and to the 9THBIT RAM on the N0 through N7 lines when the state of the R/$\overline{W}$ signal indicates a read cycle.

3-10 Complete Synchronization of Digital Video

Video data loaded into the YCK RAM output register is synchronized with video in this register on other I/O boards to within one byte time. Complete synchronization is not achieved at this time because timing of the READ CLK signal on different I/O boards varies to accommodate the asynchronous nature of input video data. Data in the YCK RAM output register is clocked into the YCK sync register by the OCLK clock, which has the same timing on all I/O boards, to achieve complete synchronization.

3-11 Concentrator Formatting

The concentrator formatting logic converts outputs of the YCK sync register into the format used in the concentrator. Outputs of the YCK sync register consist of serial bytes of luminance data on the Y0 through Y7 lines and serial bytes of alternating key and chrominance data on the CK0 through CK7 lines. The byte period in each case is 75 nanoseconds. (See Figure 3-3.) This is converted by the concentrator formatting logic into two sets of eight lines with one set carrying luminance and chrominance data and the other set carrying key data. Lines carrying luminance and chrominance, YYC0 through YYC7, have a byte period of 50 nanoseconds. They carry two bytes of luminance followed by one of chrominance during three-byte periods. The lines carrying key data, K0 through K7, have a byte period of 150 nanoseconds. As can be seen from the diagram, two bytes of luminance, one of chrominance, and one of key are received and fed out of the concentrator formatting logic during 150 nanosecond periods. The time when a chrominance byte is on the CK0 through CK7 lines is identified by the SEL-CHROMA line to the formatting logic.

3-12 Compensating Delay for Key Processing

The YYC output of the concentrator format logic is delayed to compensate for time used in processing key data in the concentrator. This delay is produced by the YYC delay logic. The logic also converts ECL inputs to TTL outputs. ECL X 1.5 clocks data into the logic. The SD0 through SD7 input is a binary number specifying the number of periods of the ECL X 1.5 clock the delay will last. The TTL X 1.5 clocks TTL data out.

3-13 ADO Formatting

ADO formatting converts digital video returning from other parts of the concentrator back into the ADO format. This process is the reverse of that performed by the concentrator formatting logic.

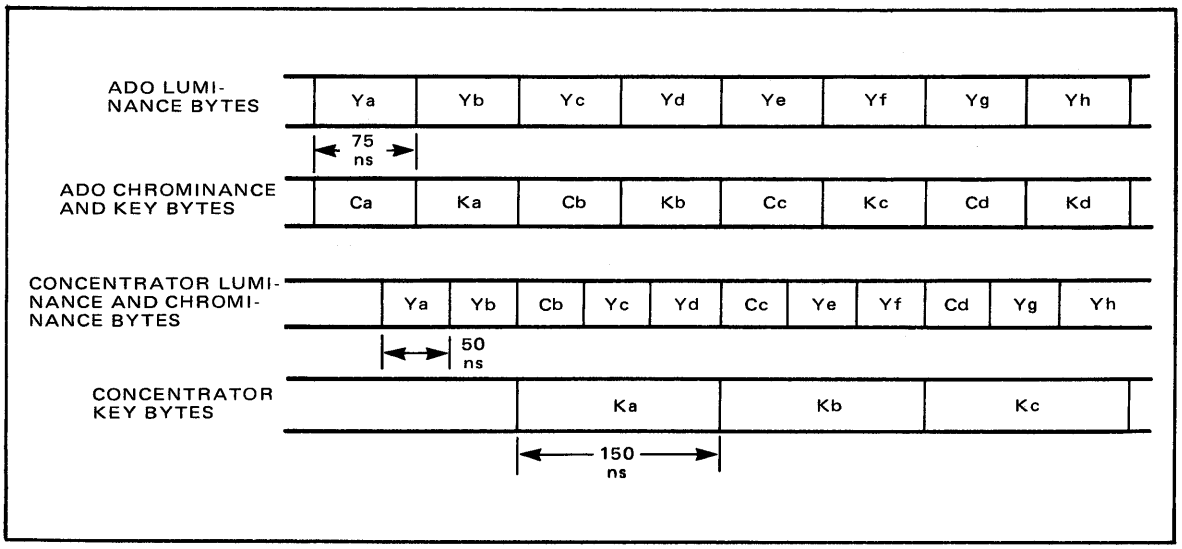


Figure 3-3. ADO and Concentrator Digital Data Formats

The key select buffers select the K1I0 through K1I7 or K2I0 through K2I7 inputs to feed to the ADO formatting logic depending on the state of $\overline{\text{SELKEY}}$ 1 and $\overline{\text{SELKEY}}$ 2 signals. Selected key data is fed to the logic on lines K0 through K7.

The ADO formatting logic receives luminance and chrominance data on MDI0 through MDI7 lines in the same format as the output of the concentrator formatting logic on YYC0 through YYC7 lines. The ADO formatting logic produces luminance outputs from MDI inputs. Luminance outputs are put on the Y0 through Y7 output lines.

Key and chrominance outputs are put on the CK0 through CK7 lines by combining key data received on the K0 through K7 lines with chrominance data received on the MDI0 through MDI7 lines. Timing to select from the key or chrominance source for the CK output is provided by the SELKEY input to the ADO formatting logic.

Outputs of the ADO formatting logic are tri-state. They are enabled by an inactive state of the LOOPTHRU signal except when video data is being looped through the I/O board. When these outputs are enabled they are converted from TTL to ECL by the TTL to ECL drivers. The outputs of the drivers are then fed to the analog chassis of the associated signal system.

3-14 Video Loopthrough Function

Video that is looped through the I/O board is delayed by the loopthrough delay logic and then fed to the analog chassis of the signal system through the TTL to ECL drivers. The delay is to compensate for delays that occur in video data that is processed by the concentrator. The LD0 through LD7 input to the delay is a binary number specifying the number of periods of the TTLOCLK clock that the delay is to last. Inputs to the logic are ECL. They are converted to TTL for internal use. Outputs of the logic are tri-state TTL. They are enabled by an active state of the LOOPTHRU signal when this function is used.

3-15 Input Register

This register receives data from the digital chassis of a signal system. It contains ECL receivers 1A, 1B, 1C, 1D, 2D and registers 2A, 2B, and 2C. (See sheet 2 of the I/O schematic in Section 5.) Inputs to the registers are clocked in on positive-going transitions of the DATACLK signal to pin 9.

The top eight lines, fed to pins 6, 7, 10, 5, 11, and 12 of IC 2A and to pins 6 and 7 of IC 2B, are luminance lines. These lines are in the order of increasing significance from top to bottom. The next eight lines are chrominance/key lines. These lines are also in the order of increasing significance from top to bottom. The input to pin 12 of IC 2C is the 9THBIT line.

3-16 YCK RAM

This RAM delays data to synchronize it with data received by other I/O boards. It contains ICs 6A, 4A, 4B, and 4C. Each of these ICs is a 256 X 4 ECL RAM. The J0 through J7 inputs are address lines. Contents of a selected address appear at pins 2, 4, 21, and 23. When the $\overline{\text{WRITE}}$ signal is strobed low, inputs at pins 6, 7, 18, and 19 are loaded into the RAM at the selected address.

3-17 9THBIT RAM

This RAM delays 9THBIT data to synchronize it with data received by other I/O boards and to compensate for video processing time in the concentrator. It contains IC 7C. Addresses are fed to this RAM on the N0 through N7 lines. These addresses are the same as J0 through J7 addresses during write operations. However, they trail J0 through J7 address by a fixed number of read/write cycles during read operations.

3-18 YCK RAM Output Register

This register contains ICs 7A, 5P, and 3D. Each of these ICs contains six D flip-flops triggered by a common clock to pin 9. Outputs of the YAC RAM and the 9THBIT RAM are loaded into this register by a high transition of the READCLK signal.

3-19 YCK Sync Register

This register contains ICs 7D 5D, and 4D. Each of these ICs contains six D flip-flops triggered by a common clock to pin 9. Outputs of the YCK RAM output register are loaded into this register by a high transition of the OCLK signal.

3-20 Concentrator Formatting Logic

This logic receives digital data in the ADO format and converts it to the format used in the concentrator. The logic contains ICs 6D, 5D, 5E, 4E, 2E, 3E, and 1E. (See sheet 3.)

The YYC1 through YYC7 signals are produced by 6D, 5D, 5E, and 4E. ICs 6D and 5D contain six D flip-flops triggered by a common clock to pin 9. (Only two of the flip-flops in 5D are used in this logic.) The Y0 through Y7 signals are clocked into these flip-flops by the ECL X 1.5 signal which has a 50-nanosecond period. (See the timing diagram in Figure 3-4.) Outputs of 6D and 5D are multiplexed with the CK0 through CK7 signals by ICs 5E and 4E to produce YYC outputs. ICs 5E and 4E are two-to-one multiplexers. Each one receives four pairs of inputs. One of each pair is selected to be gated through by the $\overline{\text{SELECHROMA}}$ input to pin 9.

The K0 through K7 outputs are produced by 2E, 3E, and 1E from CK0 through CK7 inputs. ICs 2E and 3E convert the CK inputs from ECL to TTL logic. The TTL signals are transferred to eight latches in 1E by high states of the KEYCLK signal. IC 1E has tri-state outputs which are always enabled by a low input to pin 1.

3-21 YYC Delay Logic

This logic delays YYC data to compensate for time used in processing key data in the concentrator. It also converts data from ECL to TTL. It contains ICs 7F, 7E, 7G, 6G, 5F, 4F, 3F, 2F, and 1F.

Delay is produced by storing data in RAMs 7F and 7E for a short period of time. Addresses to the RAMs follow a recycling sequence. As each address is accessed, the byte which was stored there on the previous address access, is read out. Then, the byte being read out is replaced by a new byte. The new byte remains until the

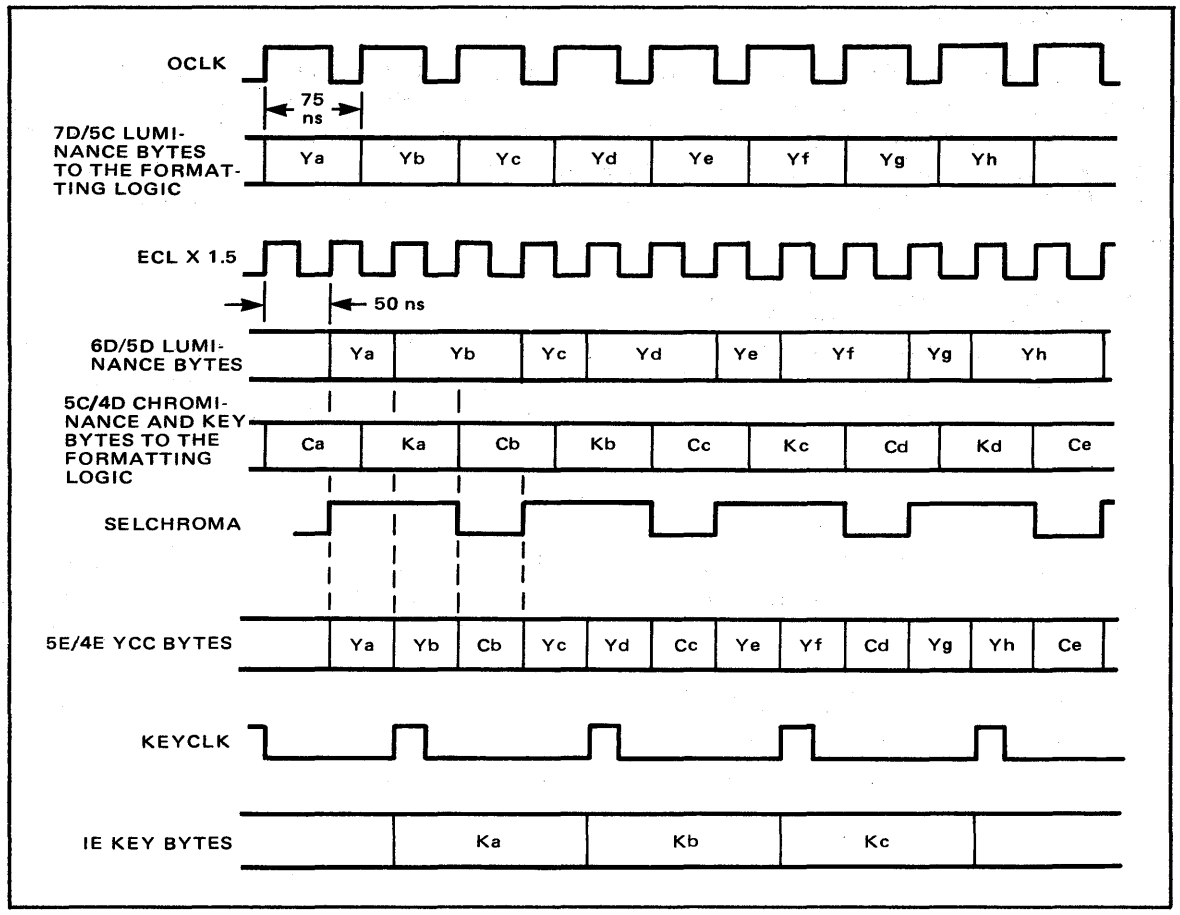


Figure 3-4. Concentrator Formatting Logic Waveforms

address sequence returns again to this address and it is read out and replaced. This read/write procedure causes bytes to be stored for the amount of time it takes for addresses to recycle.

Addresses for RAMs are produced by counter 6G/7G. This counter is decremented by the ECL X 1.5 clock. Each time the count reaches zero, the counter is preset to a binary number supplied on the SD0 through SD7 lines. Consequently, address recycle time is the period of the ECL X 1.5 clock times the SD number plus one additional period (since address 00000000 is also in the cycle).

Counter 6B/7G is put in preset mode when the clock goes low after decrementing to zero. (See Figure 3-5.) When counter 6G/7G receives the high clock transition that decrements it to zero, the carry in and S2 inputs of 6G go high. Since the carry in of 6G is high (inactive), the carry out is also high. This makes carry in and S2 inputs of 7G high. The high carry in to 7G makes 7G carry out high and input S1 of both ICs high. The high S1 and high S2 inputs to both ICs puts them in hold mode. When the clock goes low, the low input to S2 of 6G puts it in decrement mode. The low (active) carry in to 6G causes it to produce a low carry out at this time since it is at count zero. The low carry out of 6G to S2 of 7G puts 7G in decrement mode.

The low input to carry in of 7G produces a low carry out. This output sets S1 of both ICs low, converting the decrement mode of both ICs to preset mode. The following high transition of the clock presets counter 6G/7G.

Counter 6G decrements on high transitions of the clock after being preset. The high transition that produces the preset makes the carry out of both 6G and 7G high. The high output of 7G produces a high input to S1 of both 6G and 7G. The high carry out of 6G to S2 of 7G keeps 7G in the hold mode. When the clock goes low, the low input to S2 of 6G puts this IC in the decrement mode, causing it to decrement on the next high transition.

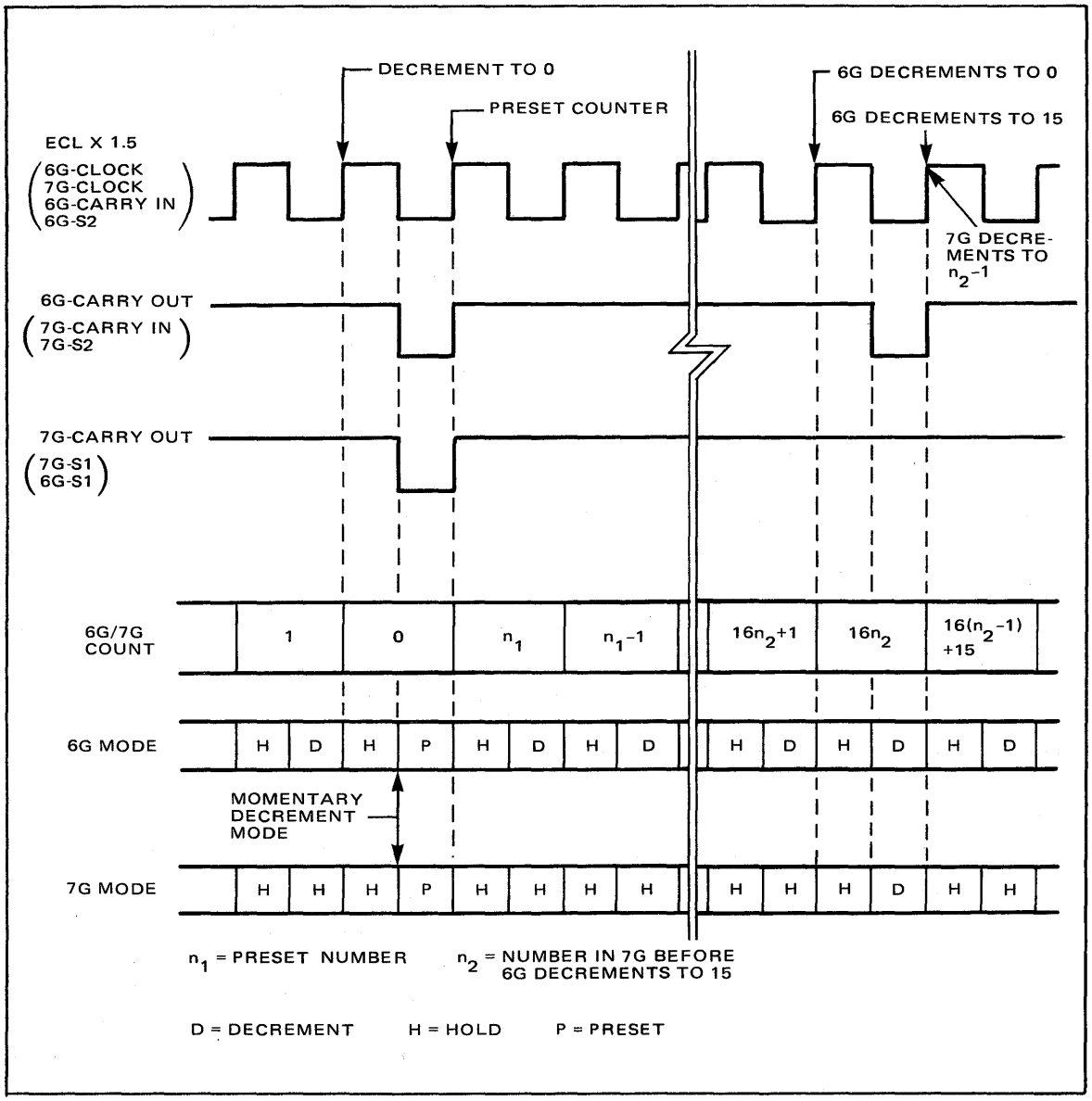


Figure 3-5. Decrementing Counter Modes

When the count in 7G is not zero and counter 6G decrements from zero to 15, counter 7G also decrements. The low clock to S2 of 6G puts this counter in decrement mode. The low carry out from 6G puts 7G in decrement mode. Since 7G does not produce a carry out in this case, both 6G and 7G remain in decrement mode until the clock goes high causing the decrement. After decrementing to 15 the carry out of 6G remains high until it is decremented to zero again. This output keeps 7G in hold mode.

The ECL X 1.5 signal, which clocks counter 6G/7G, also provides read/write control to RAM 7E/7F When this clock goes high, producing a new address, the RAM goes to the read state. After outputs settle the ECL X 1.5 clock to register 4F/5F goes high clocking RAM output data into the register. ECL X 1.5 goes low at this time, loading another byte into the RAM to replace the one just read out.

Outputs of register 4F/5F are converted to TTL by translators in 2F and 3F. The TTL signals are then synchronized with concentrator processing logic by clocking them into D flip-flops in register 1F with the TTL X 1.5 signal. Outputs of this register, which is tri-state, are enabled by the low input to pin 1.

3-22 Write Address Counter

The write address counter produces write addresses for the YCK RAM and the 9THBIT RAM. It contains ICs 9R and 9P. (See sheet 2 of the I/O PWA Schematic.) This counter is preset by the ECL INPUT PRESET pulse which is detected in the 9THBIT signal at a particular picture element of input video. The preset number is fed to the counter on the L0 through L7 lines. This number is the same on all I/O boards in a concentrator. The counter is decremented by the ICLK clock which is received by the I/O board with input video. Each time the counter is decremented to zero, it is preset again to the L0 through L7 number. W0 through W7 outputs are gated through the YCK address generator and 9THBIT address generator to address the RAMs for writing.

Mode control of ICs 9R and 9P is similar to that described for ICs 6G and 7G in the YYC delay logic. In this case, however, provision is made to put the ICs in preset mode when the ECL INPUT PRESET signal goes low. This low input is fed to S1 of both ICs through gate 9S-14. The clock input, instead of 9P carry out, is fed to S2 of 9R. As a result, both ICs go to preset mode when the preset pulse occurs and the clock input is low.

3-23 YCK Address Generator

The YCK address generator feeds addresses to the YCK RAM for writing and reading. It contains ICS 6N, 7N, 7R, 7P, 8R and 8P.

Read addresses are produced in the generator by a counter consisting of ICs 7R and 7P. This counter is preset by the OUTPUT PRESET pulse which is detected at a particular picture element in reference video. The preset number is fed to the counter from multiplexers 8R and 8P. These multiplexers select E0 through E7 inputs for the counter preset number when the OUTPUT PRESET signal, fed to pin 9 of 8R and 8P, is active (low). The counter is decremented by the OCLK signal which is derived from X3 IN and HPHASE IN signals from the I/O board receiving

reference video. When the counter decrements to zero, it is preset to the L0 through L7 number fed to multiplexer 8R/8P since the OUTPUT PRESET signal is high at this time. This counter is the same configuration as write address counter 9R/9P and mode control of the ICs is achieved in the same manner as described for the write address counter.

Addresses are fed from the YCK address generator to the YCK RAM through multiplexer 6N/7N. When the R/$\overline{W}$ input to this multiplexer is low, write addresses from write address counter 9R/9P are fed through. Read addresses, from counter 7R/7P, are fed through when R/$\overline{W}$ is high.

3-24 9THBIT Address Generator

The 9THBIT address generator feeds addresses to the 9THBIT RAM for writing and reading. It contains ICs 6M, 7M, 9M, 8M, 9N, and 8N. Logic configuration used for this address generator is the same as that used for the YCK address generator. 9THBIT read address counter 9M/8M is incremented by $\overline{OCLK}$ and preset by OUTPUT PRESET. Selection is controlled for output multiplexer 6M/7M by the R/$\overline{W}$ signal. Control of input multiplexer 9N/8N is controlled by the OUTPUT PRESET signal. The only difference between this address generator and the YCK address generator is that the OUTPUT PRESET low pulse presets it to B0 through B7 instead of E0 through E7. The difference between these two numbers produces the additional delay required for the 9THBIT signal.

3-25 Arbitrator

The arbitrator generates DATACLK, $\overline{WRITE}$, READCLK, and R/$\overline{W}$ signals. These signals are all synchronous with the X3 IN clock. They are generated as necessary to accommodate asynchronous timing of input video digital data.

3-26 Generation of the DATACLK Signal

The DATACLK signal is generated by logic on the left side of sheet 4 of the schematic diagram. This logic includes ICs 8T, 8S, 7S, and 8U. It also includes flip-flops 7T-15, 7U-2, 7U-15, and 3M-15.

The DATACLK signal is derived from the asynchronous ICLK signal. Transitions of the DATACLK signal follow transitions of the ICLK signal between 25 and 50 nanoseconds after ICLK transitions occur. The DATACLK transitions only occur in response to high transitions of the X3 IN signal.

The ICLK signal is clocked into flip-flops 7T-15, 7U-2, and 7U-15 by outputs of D flip-flops in IC 7S. These outputs are illustrated in Figure 3-6 along with an example of an ICLK signal. The period of the 7S outputs equals three periods of the 40.5-MHz clock. (This clock is a fanned-out version of the X3 IN signal.) Since the period of the 7S outputs is the same as the period of the ICLK signal, high transitions to the clock inputs of the flip-flops always find the ICLK signal in the same state in this example. This results in steady state outputs of the flip-flops. (This example only covers a few cycles of the illustrated signals. In a normal situation the phase of the ICLK signal will drift within limits with respect to outputs of IC 7S.)

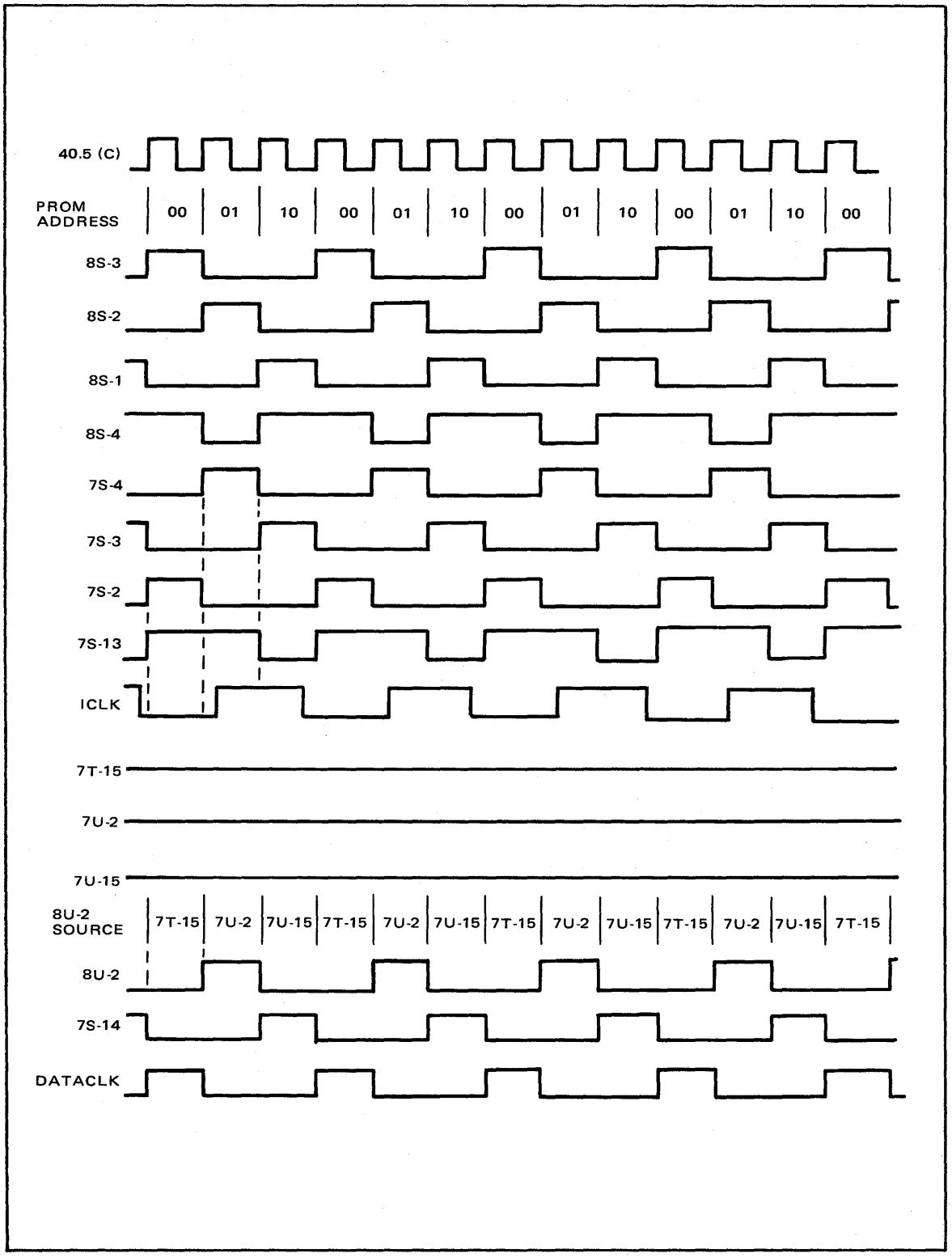


Figure 3-6. DATACLK Generation Idealized Waveforms, Example One

Outputs of the flip-flops are multiplexed by IC 8U. The source of the multiplexer output is identified, for each cycle of the 40.5 clock, in the waveform diagram. The multiplexer output, 8U-2, is clocked through a flip-flop in 7S to produce the 7S-14 output used in generating R/W, $\overline{\text{WRITE}}$, and READCLK signals. The 8U-2 output is also clocked through another flip-flop in 7S and flip-flop 3M-15 to produce the DATACLK output.

Figure 3-7 illustrates a second example of waveforms in Figure 3-6. In example two, high transitions of the ICLK signal coincide with high transitions of the 7S-2 output. When an ECL flip-flop is triggered with the data changing, the output oscillates for a maximum of 25 nanoseconds before settling at a high or low level. (The example illustrated shows it settling high after the first trigger, then low twice, and then high again.) As can be seen from the "8U-2 SOURCE" line, the output of each flip-flop is passed through the multiplexer for a 25 nanosecond period starting 50 nanoseconds after the flip-flop is triggered. This timing assures a good logic level output from the flip-flop during the time it is used. In example two, high transitions in the DATACLK signal follow high transitions in the ICLK signal by 25 nanoseconnds in some cases and 50 in others. These two cases represent the minimum and maximum delay that can occur.

Signals that clock flip-flops 7T-15, 7U-2, and 7U-15 are produced by ICs 8T, 8S, and 7S. IC 8T is a modulo 3 counter, 8S is a PROM, and 7S contains six D flip-flops. The counter sequences through counts 00, 01, and 10 and then presets back to 00 and continues the cycle. The counter is incremented by the 40.5 clock. The two least significant stages of the counter are used as address lines to the PROM, causing it to sequence through addresses 00, 01, and 10 and then repeat. Outputs of the PROM are clocked into flip-flops of IC 7S to produce glitch-free signals. Contents of addresses 00, 01, and 10 at pins 2, 3, and 4 are illustrated by the waveforms in Figure 3-7. When the counter is in count 10, the output of 7S at pin 13 puts it in the preset mode. Since all data inputs to the counter are open (low), the counter presets to 00 at the next increment.

Selection of the source for the output of multiplexer 8U is controlled by stage outputs of counter 8T. This causes the D0, D1, and D2 inputs to be passed during PROM addresses 00, 01, and 10, respectively.

3-27 Generation of the $\overline{\text{WRITE}}$ Signal

A low $\overline{\text{WRITE}}$ pulse always occurs during the second half cycle of the 40.5 clock following a high transition of the DATACLK signal. (See DATACLK and $\overline{\text{WRITE}}$ waveforms near the bottom of Figure 3-8.) This assures that every byte loaded into the input register will be loaded into a RAM. As already mentioned in the generation of the DATACLK signal, it makes transitions only at high transitions of the 40.5 clock. It makes a high transition between 25 and 50 nanoseconds after a high transition of the ICLK signal. In the case of a 50 nanosecond delay RAM loading is just completed by a low $\overline{\text{WRITE}}$ pulse when write addresses are changed by the next ICLK high transition. (See the third high transition of the ICLK signal in Figure 3-8.)

The $\overline{\text{WRITE}}$ signal is generated by the logic configuration containing flip-flops 7L-15, 7L-2, 8K-15, and 8K-2. When a high transition of 7S-14 occurs, 7L-2 is triggered high. (7S-14 leads DATACLK by one cycle of the 40.5 signal. See the 7S-14 and 7L-2 waveforms in Figure 3-8.) The high output of 7L-2 produces low data

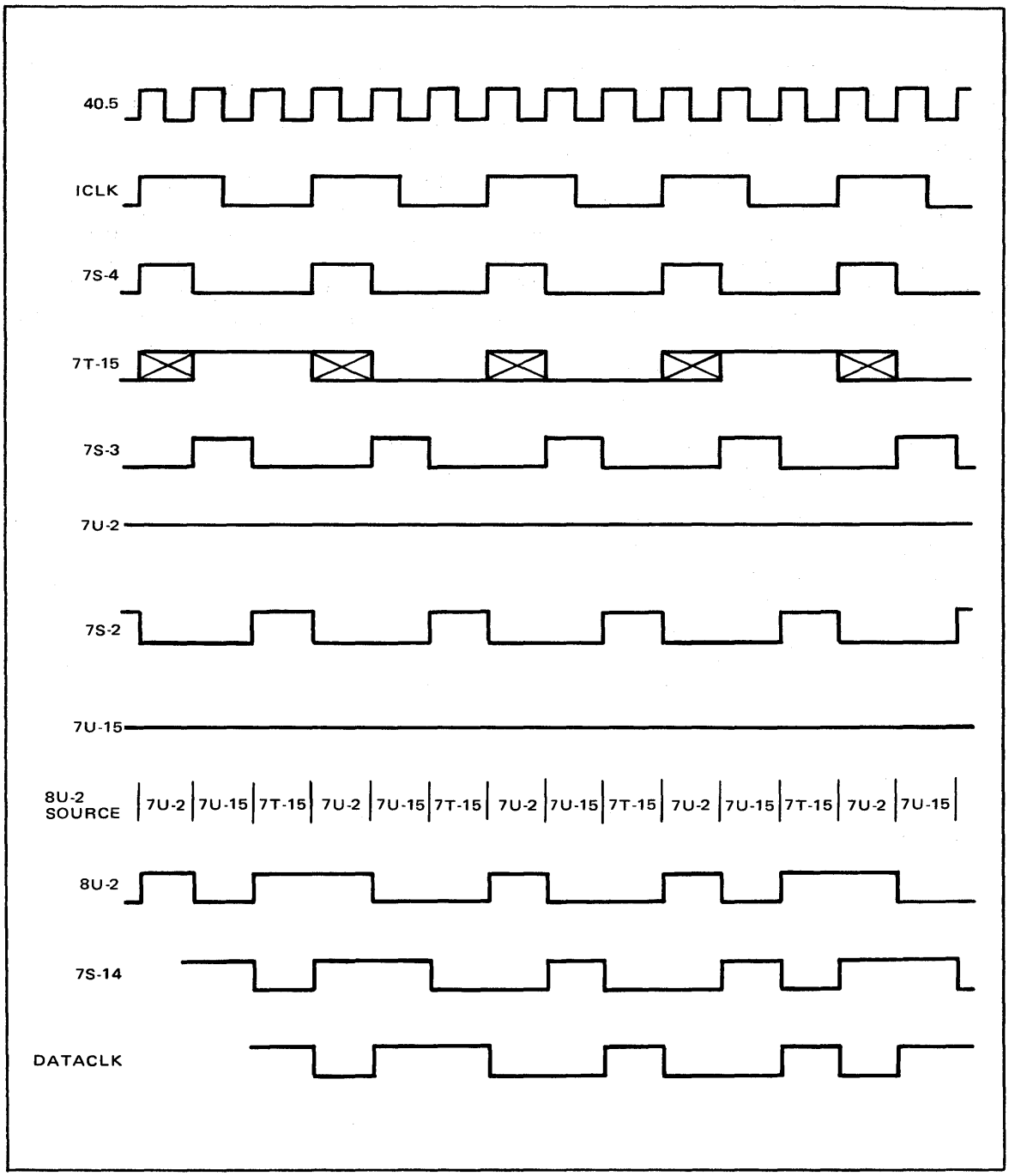


Figure 3-7. DATACLK Generation Idealized Waveforms, Example Two

inputs to both 8K flip-flops. The next 40.5 trigger makes R/$\overline{W}$ (8K-2) and 8K-15 go low. These inputs to pins 11 and 10 of gate 8L-7 cause it to produce a low $\overline{WRITE}$ pulse when clock 40.5 goes low. When R/$\overline{W}$ and 8K-15 go low, gate 8J-2 produces a high output which clears flip-flop 7L-2. The low output of 7L-2 causes either 8K-2 or 8K-15 to go high, preventing another $\overline{WRITE}$ pulse until 7S-14 goes high again.

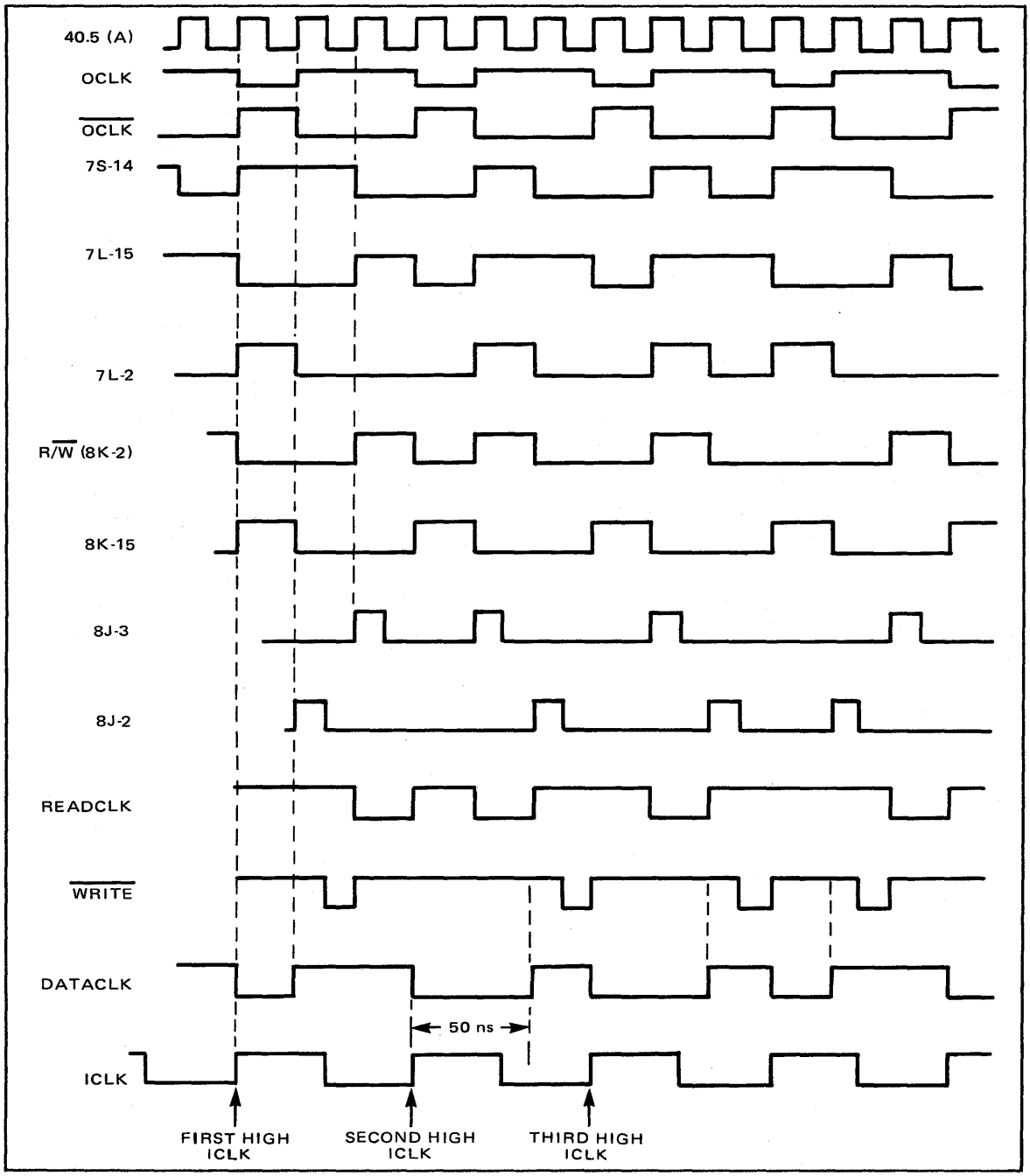


Figure 3-8. $\overline{WRITE}$ and READCLK Generation, Typical Idealized Waveforms

3-28 Generation of the READCLK Signal

A high transition of the READCLK signal clocks data into the YCK RAM output register. It is produced in response to a high transition of the OCLK signal.

If the high OCLK transition does not coincide with a high DATACLK transition, the READCLK signal goes low at the high OCLK transition. Then, after one cycle of the 40.5 clock, READCLK goes high. The second high transition of the OCLK signal in the waveforms of Figure 3-8 does not coincide with a high transition of the DATACLK signal. When the $\overline{\text{OCLK}}$ signal goes high, one cycle of the 40.5 clock before this OCLK transition, the output of flip-flop 7L-15 goes low. Since the output of 7L-2 is also low at this time, READCLK goes low at the following trigger of clock 40.5. Pins 4, 5, and 6 of gate 8J-3 are all low when READCLK goes low causing 7L-15 to go high. This in turn causes READCLK to go high at the next trigger.

When the high OCLK transition coincides with a high DATACLK transition, the READCLK signal remains high for one cycle of the 40.5 clock. Then, it goes low for one cycle of the 40.5 signal before making a high transition. The high state of the READCLK signal is required for address selection following the high DATACLK transition. The R/$\overline{\text{W}}$ signal, which is the inversion of READCLK, controls address multiplexers 6M, 7M, 6N, and 7N. The R/$\overline{\text{W}}$ signal must be low for one cycle of clock 40.5 after a high DATACLK transition to feed write addresses to the RAMs until the following low $\overline{\text{WRITE}}$ pulse ends.

The first high transition of the OCLK signal in waveforms of Figure 3-8 coincides with a high transition of the DATACLK signal. When the $\overline{\text{OCLK}}$ signal goes high, one cycle of the 40.5 clock before OCLK goes high, the output of flip-flop 7L-15 goes low. The output of 7L-2 will go high at this time because of the high transition of 7S-4. The high output of 7L-2 to pin 5 of gate 8L-3 prevents READCLK from going low on the following trigger of the 40.5 clock. However, the high state of clock 40.5 after the trigger produces a high output from gate 8J-2 to clear flip-flop 7L-2. This allows READCLK to go high after one additional cycle of clock 40.5.

3-29 Loopthrough Delay Logic

This logic delays Y and CK data that is to be looped through the I/O board. The delay causes this video to be synchronized with video outputs of other I/O boards. It compensates for processing time consumed in the concentrator to process video that is not looped through. The logic contains 7H, 5H, 5J, 7J, 4G, 5G, 5K, 6K, 4H, 4J, 3J, and 4K. (See sheet 6 of the I/O PWA Schematic.)

Data is delayed in the RAM consisting of IC RAMs 7H, 5H, 5J, and 7J. Addresses for the RAM are produced by counter 5N/4N. The operation of this RAM and counter is the same as the RAM and counter described in the YYC delay logic. In this case, the counter is decremented by the OCLK signal which also controls the read/right mode of the RAM. The amount of delay produced by this logic is controlled by preset number LD0 through LD7.

Outputs of the RAM are converted from ECL to TTL by translators 4G, 5G, 5K, and 6K. TTL outputs are clocked into D flip-flops in ICs 4H and 4J by the $\overline{\text{TTLOCLK}}$ signal. This signal goes high as the OCLK signal goes low, producing a write strobe to the RAM. Outputs of 4H and 4J are synchronized with ADO format

output data by clocking them into D flip-flops in 3J and 4K with the TTLOCLK signal. ICs 3J and 4K have tri-state outputs. These are enabled for loopthrough functions by an active (low) state of the $\overline{\text{LOOPTHRU}}$ signal.

3-30 Key Select Register

The key select register selects either the K1I0 through K1I7 data or the K2I0 through K2I7 data as the key output of the I/O board. It contains ICs 1H and 1G. (See sheet 7.) K1I data is clocked into 1H and K2I data is clocked into 1G by the TTL X 1.5 signal. Tri-state outputs of one or the other of these ICs are enabled at all times depending on whether the state of $\overline{\text{SELKEY 1}}$ or $\overline{\text{SELKEY 2}}$ is low. The enabled outputs are fed to ICs 3G and 3H of the ADO formatting logic.

3-31 ADO Formatting Logic

ADO format logic receives digital video data from other boards in the concentrator. It converts this data from the concentrator format to the ADO format. The logic contains ICs 2H, 2J, 2G, 3G, 3H, and 3K.

The MDI0 through MDI7 inputs contain luminance and chrominance data in the same format as the output of the concentrator formatting logic on the YYC0 through YYC7 lines. This data is clocked into 2H by the TTL X 1.5 signal. (See the 2H OUTPUT and TTL X 1.5 lines in Figure 3-9.) Outputs of IC 2H are clocked into IC 2J by the TTLOCLK signal. This produces luminance outputs in the ADO format as illustrated in the 2J OUTPUT line of Figure 3-9.

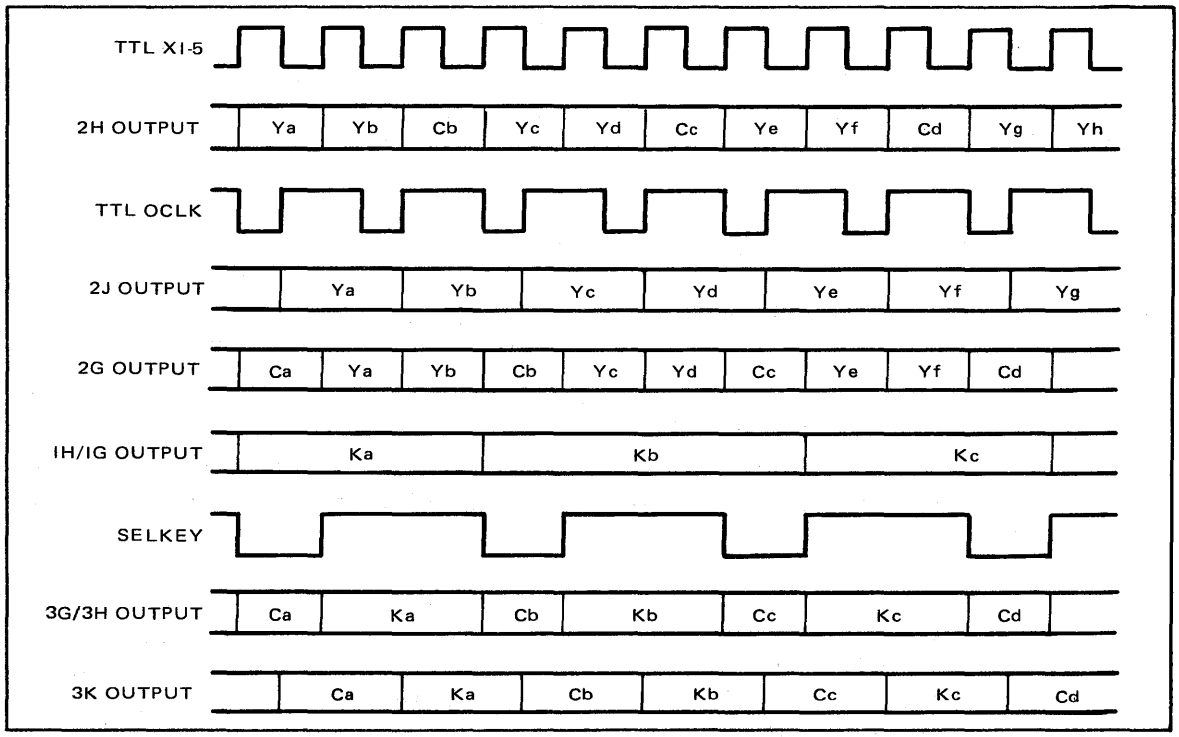


Figure 3-9. ADO Formatting Logic Waveforms

Outputs of 2G and 1H or 1G are multiplexed by 3G and 3H to alternately feed chrominance and key data to register 3K. This data is clocked in by the TTLOCLK signal to produce chrominance and key data in the ADO format.

3-32 TTL to ECL Drivers

TTL to ECL drivers receive digital video from ADO formatting logic or loopthrough delay logic and feed it to the analog chassis of the associated signal system. Drivers are contained in ICs 1J, 2K, 1K, 2L, and 1L. The source of inputs to the drivers is controlled by the LOOPTHRU signal.

3-33 H Phase Lock Loop

The H phase lock loop produces the PLLX3 and PLLHPHASE signals. It contains circuits illustrated on sheet 10 of the schematic.

The PPLX3 signal is an ECL square wave at a frequency of 40.5 MHz. This is 3 times the frequency of the ICLK input data clock. This signal is produced by converting the sine wave output of a crystal oscillator to ECL logic levels. The sine wave is generated at the junction of crystal Y1 and capacitor C19. Line receiver 8B converts it to an ECL square wave.

The PLLHPHASE signal is a line frequency signal. It is phase-locked to the LINE REF signal from the signal system. It is produced by dividing the frequency of the X3 signal. First the X3 signal is divided by three to produce a 13.5-MHz TTL signal. This signal is then divided by 858 or 864 for NTSC or PAL applications, respectively. Flip-flops 8G-2 and 8G-15 divide X3 OUT by 3. Translator 9L-5 converts the output of 8G to TTL. The counter containing IC counters 10L, 9K, and 10K divides the TTL signal frequency by 858 when there is no jumper between A and B at the preset input to 10L. A jumper between A and B causes the frequency to be divided by 864.

Phase lock is produced by an error voltage feeding back to the crystal oscillator. Phases of the PLLHPHASE and LINE REF signals are compared to produce the error signal at the output of diode bridge CR2/CR3/CR4/CR5. The phase relationship between these two signals is adjusted by potentiometer R75.

3-34 Board Clocks and Control Generator

The board clocks and control generator produces timing and control signals that are synchronous with reference video. The generator contains circuits illustrated on sheet 5 of the schematic.

Signals are produced by this generator from outputs of PROM 5L. This PROM is addressed by counter stage outputs from IC counter 4L. PROM outputs are converted to reliable ECL voltage levels by clocking them into D flip-flops in ICs 5M and 6L. The SELKEY, KEYCLK, TTLOCLK, and TTL X 1.5 signals are converted to TTL by translator 7K. Waveforms for signals produced by this generator are illustrated in Figure 3-10.

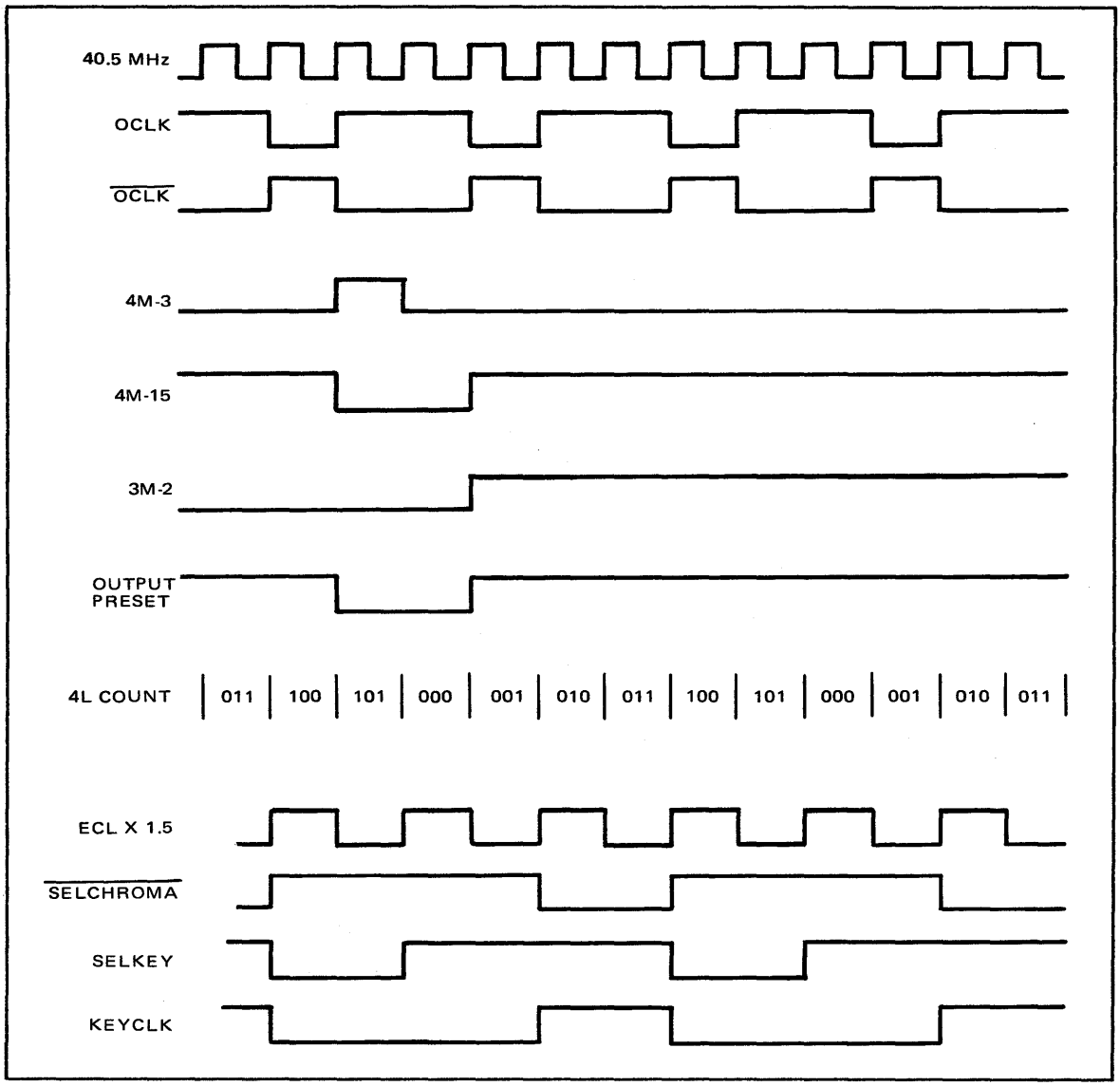


Figure 3-10. Board Clocks and Control Waveforms

Counter 4L is incremented by the 40.5 clock which is a fanned-out version of X3 IN. It is preset to zero at the start of each line by the output of flip-flop 4M-3. The counter is also preset by the high output of 6L-4, causing it to recycle every sixth increment.

3-35 9THBIT Decode Logic

The 9THBIT decode logic detects the $\overline{\text{TTL INPUT PRESET}}$ pulse which presets the write address counter. It also stores concentrator control bytes from the signal system. These bytes are stored in a RAM which is accessible to the Combiner Computer PWA. The logic contains ICs 5S, 6S, 6T, 2T, 2S, 6U, 5T, and 4T. (See sheet 8.)

3-36 Generation of the $\overline{\text{TTL INPUT PRESET}}$ Signal

The $\overline{\text{TTL INPUT PRESET}}$ signal goes low when the start code (see Table 3-1) for the last transmission of an even field is detected in the 9THBIT input. Data bits, received serially on the 9THBIT line, are shifted into register 5S by the TTLICLK clock. Parallel outputs of this register are fed to programmable array logic (PAL) 6S. When the last byte of an even field is in S5, it is detected by the PAL. The PAL produces a low $\overline{\text{TTL INPUT PRESET}}$ pulse at this time at output pin 15. Pin 14 of the PAL goes low when the first byte of each transmission is detected. This output clears flip-flop 6R, preventing the PAL from looking for a start code again until the flip-flop is triggered by the HRESET pulse which occurs before the next transmission.

Table 3-1. First 9THBIT Byte Format

Bits	Function
D0	Start code 101
D1	
D2	
D3	1 = Select key 1, 0 = Select key 2
D4	1 = Last transmission of the field
D5	1 = Odd field, 0 = Even field
D6	1 = Combiner Computer PWA data 0 = Video output processor data
D7	A/B switch position

3-37 Storage of Control Data

Control data for the concentrator is sent in 8-byte transmissions, with several transmissions per field. Data is received bit-serially on the 9THBIT line and is stored in RAM 4T. Serial data is assembled into bytes and stored at addresses established by the byte number and transmission.

Outputs of shift register 5S are fed to RAM 4T via register 5T. Register 5T is clocked at pin 11 by output QC of counter 6T. This counter output provides a rising edge every eight bits which converts the serial data into bytes. There are eight rising edges per transmission.

Addresses for RAM 4T to store control data are generated by counter 2T/2S. This counter is cleared at the beginning of the last transmission in a field. It is incremented once for each eight bits received. The clock for this counter is produced by toggling flip-flop 6U with the second stage output of bit counter 6T.

Counter 6T is taken out of load mode by the low output on pin 17 of PAL 6S when a start code is detected and bit D6 is high, indicating data is for the Combiner Computer PWA. During the time data is being stored in the RAM, the low output of 6U-8 keeps it in the write mode. After eight bytes have been stored, address line R2 goes low and toggles flip-flop 6U-9. This returns counter 6T to load mode in preparation for a subsequent data transfer and puts RAM 4T in read mode. An interrupt is generated by detecting the last transmission of each field. This indicates to the computer that new data is stored in RAM 4T.

3-38 KEYER PWA

There are two keyer PWAs in the concentrator that are interconnected to form the keyer unit. The keyer unit receives key data from each channel. It produces a processed key data output for each channel which reflects the priority of channels in a combine. The keyer unit also produces background video data, background key data, and composite key data for each of two combines. Background video data does not have line or vertical sync pulses. After being cut by the background key data and added to combine data, background video data produces composite video. Composite key data output is available to a switcher to put the combine over a background provided by the switcher.

3-39 Key Data Processing

When key data is processed for a combine, data for a channel is modified by data from channels with higher priority. For example, in a combine with channel D having the highest priority followed by channel B and then channel C, channel D data is unaffected. Channel B data is modified by data from channel D and channel C data is modified by data from both channels D and B.

Channel D key data is fed to the key-requested input of the channel D key processor in the keyer unit. (See Figure 3-11.) Since none of the key for the combine is used ahead of channel D, the key-taken-previously input from the key-taken multiplexer will be zero for this example. Key-received output, which is the channel-D-processed key output of the keyer unit, will be the same as the key-requested input. (This assumes that no transparency or dimming is introduced by the channel key processor. These functions will be described later.) The key-taken-now output will also be the same.

The key-taken-previously input to channel B key processor will be the key-taken-now output of the channel D key processor for this example since channel B is next in priority after channel D. The key-taken-now output from channel D is fed to the

key-taken multiplexer in slot 10 PWA. From here it goes to the multiplexer in slot 9 PWA via the key-taken bus. The multiplexer in slot 9 PWA then feeds the key-taken signal to channel B key processor. The key-received output of channel B key processor will be the key-requested input when it is available as indicated by the key-taken-previously input. When not, it will be whatever is available. The key-taken-now output of this processor will be the sum of what is taken by channels D and B.

The key-taken-previously input to channel C key processor will be the key-taken-now output of channel B key processor for this example. The key-received output will be the key-requested input when it is still available after channels D and B processing. Otherwise it will be whatever is available. The key-taken-now will be the sum of what is taken by channels D, B, and C.

3-40 Background Video Data

Two background video data channels are produced by the keyer unit, one by the background video generator in each PWA. Either generator can produce data to be used in combine No. 1 or No. 2. Output of a generator is in synchronization with timing input from the Clock PWA. This puts it in synchronization with reference video of the combine for which it is produced.

3-41 Background and Composite Key Data

These two outputs are produced by a background and composite key generator in each Keyer PWA. Background key data is used to cut background video data produced in the same PWA. Key data will be used as the final combined key output. The two key outputs of this generator are produced from the key-taken-now data of the lowest priority channel in the combine. This would be channel C in the example just described.

3-42 Channel Key Processor

There are four channel key processors in the keyer unit, one for each channel. Key processors for channels A and B are in slot 9 PWA. Slot 10 PWA contains key processors for channels C and D. A processor produces a key-received and a key-taken-now output.

The key-received output of a channel is used to cut video data for the channel. It is produced by altering key data requested from an I/O board. Key data is decreased at some picture elements as a result of being covered by a higher priority channel. It is also decreased to introduce transparence and dimming. Key data from a channel is fed to multiplier logic in the channel key processor. (See Figure 3-12.) This logic converts signed binary numbers representing key strength to positive binary fractions as required by keyer and cutter logic. Data is then multiplied by a number between 0 and 1. If no transparency is desired, the number will be 1. Transparency increases as the number approaches 0. Multiplied data is then fed to the delay memory. This memory produces a delay to compensate for time used in producing the key-taken-previously signal when this channel has a lower priority than another channel or other channels. This is necessary so that key-requested data representing a picture element arrives at the priority processor at the same time as key-taken-previously data for the same picture element. The priority

KEY EXPANSION BUS

KEY PRIORITY SELECTOR

XF
XE
XD
XC
XB
XA

AD 8

SELECTED KEY TAKEN

8

AD
150BD
LATCH
JJ

PREVIOUS BKG KEY + PRESENT BKG KEY ADDER

BACKGROUND KEY

B
+ Σ
A
AC

LATCH
OC
3H
150BD

8
XB

LATCH
4J
150BD

8

LATCH
4H
150BD

8

KEY TAKEN TO KEY AVAILABLE CONVERTER

Y

PROM
A1- A8
Q1- Q8
5H

8
Z

KEY AVAILABLE/ KEY WANTED MUX

Z
X
AB
60,6H
SEL

y

A
+ Σ
B
7H,JJ

8

LATCH
8H
150 BD

8
XB

KEY AVAILABLE KEY WANTED COMPARITOR

Z
A
A<B
B
5J,6K

X

PREVIOUS KEY TAKEN + PRESENT KEY TAKEN ADDER

KEY PRIORITY SELECT

RAM DELAY COUNTER

KEY RAM DELAY

CD8-CD10
CD12-CD15
CD11

3
4
1

LATCH

4 KEY DELAY
CD11L

CSE

COMPUTER COMMAND LATCH

4C,3K

150BD

4

A0-A3
D
5L,5K
Q

8

LATCH
6L
150BD

X

8

M

LATCH
Q1- Q8
D1- D8
OC
150BD

8

LATCH
1Q- 8Q
1D- 8D
4K
150BD

8

121
113

B KEY IN
AH

LATCH
8K
OC
150BD
150 BD

M
8

PROM
A0- A7
D0- D8
7L
A8 A9
150BD

LATCH
D1- D8
Q1- Q8
8L
75NS

CD11L

8

.5X CLOCK (150 NS)
1X CLOCK (75NS)
3X CLOCK (25NS)
110
109
105
106
111
112

B KEY CLOCK GENERATOR
1L,2K,2L, 3K,3L

150BD
75NS
150BD

AH

TALLEY DETECTOR
10S PAL

PRE-TALLY B OUT
152

AE

C

TRANSP. REG
1D- 8D
1Q- 8Q
9C
CSA
150BD

CD0- CD7
8

DIMMERS REG
1D- 8D
1Q- 8Q
10C
CSA
150BD

CD8- CD16
8

X
Y
X P
10D

8
N

PRE / POST KEY MULTIPLIER

LATCH
2J
150BD

LATCH
5J
OE4
150BD

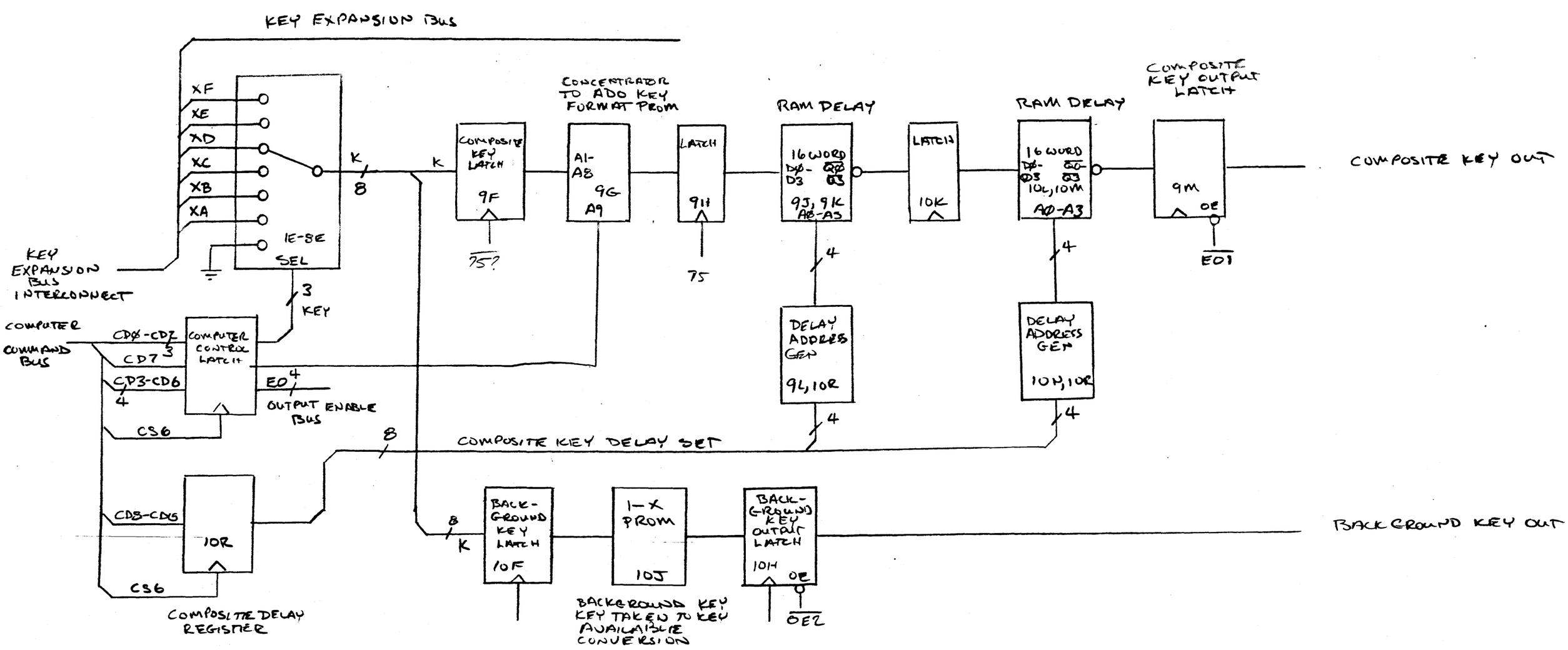
AC
8

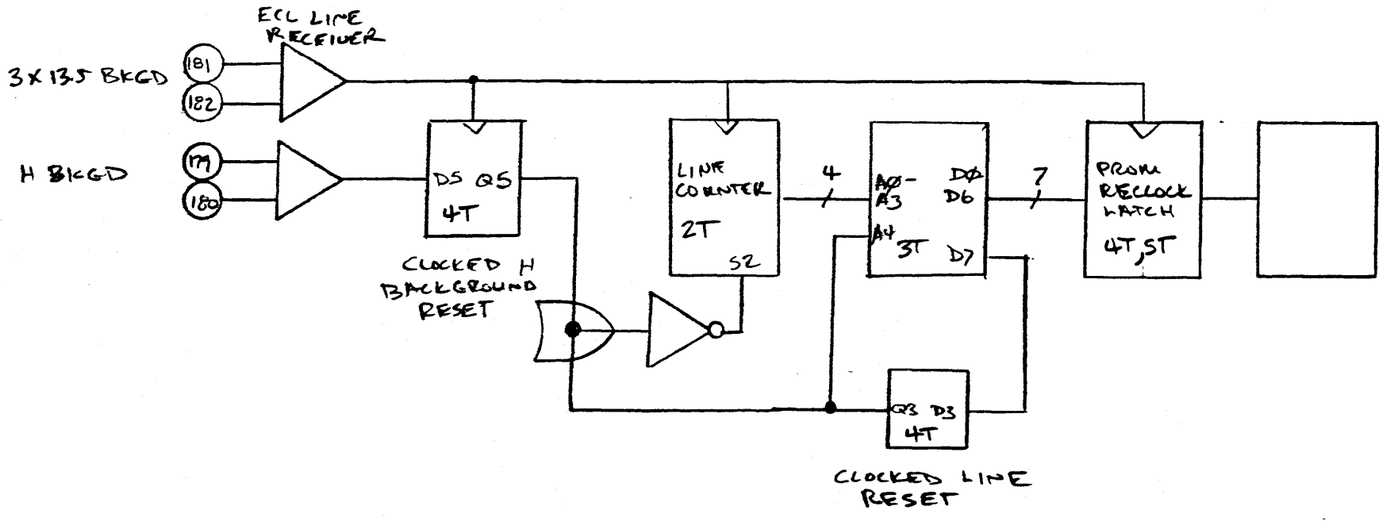
KEY B OR KEY D OUT TO CUTTER

COMPUTER BUS

CD 16

KEY B KEY GENERATOR





ADO CONCENTRATOR KEYER

COMPOSITE AND BACKGROUND KEY GENERATION

VERTICAL BLANKING

VBI (156)

VBO (156)

1 = TOP FIELD LINE
3 = CENTER
2 = BOTTOM HALF LINE

SD

6D 7P

LATCH

LATCH 8N

FRAME

3 R4-R6

BLANKING EDGE COUNTER

÷5

COUNTER 7N, 7S

4 RØ-R3

HCLK

2 LINE TYPE

H RATE SIGNAL GEN

H RATE SIGNAL LOGIC

CDØ-CD2

CD3-CD4

CD7

CSØ

LATCH 9N

D3

2 CNTR Ø

INT BACKGND

ADDRESS GEN A B Q LD CLR

÷5

10 Q

PROM A6-A9 8S

8

7R, 8R 6P

5

PROM/LATCH 8H, 7M

÷5

2 RB7-RB8

FRAME (168)

75

2

FRAME

EDGE TYPE PROM

9

Y BLANK VALUES PROM 6N

S

8 S

Y BLANK VALUES LATCH

÷5

LUM

T

8

CHROMA BLANK VALUES PROM PROM 5N

COLOR BLANK VALUES LATCH

OC

300

CR1+CR2

T

8

LATCH 6P

8

LUMA PIX VALUES PROM 5P

LATCH 5R

LATCH OC 4R

÷5

LUM

8W

Ø CORRECT 1ST ACTIVE 4P

1G 2G

CR1+CR2

CR2

CR1

LUM

BKGD CLKS

35

6

3

11

8

T

B

U

Y X.P X 4M

EDGE SHAPING MULTIPLIER

LATCH 2M

÷50

B + Σ A 1N, 2N

BLANKING CORRECTION ADDER

LATCH 1M

÷50

8

BACKGROUND VIDEO OUT

NOT USED

BACKGROUND VIDEO 8

OC LATCH 3R U

CDØ-CD7 OC LUM LATCH 3P U

CDØ-CD7 OC CR1 LATCH 2P U

CD8-CD16 OC CR2 LATCH 1P U

÷50

24

8

CS4

CS2

CS2

COMPUTER DATA DØ-D15

BUFFER 1R, 2R

CD 16

COMPUTER BUS

CD COMPUTER CS COMMAND BUS

BACKGROUND VALUE LATCHES

STROBE

R/W

A3

A2

A1

G2A

G2B

C

B

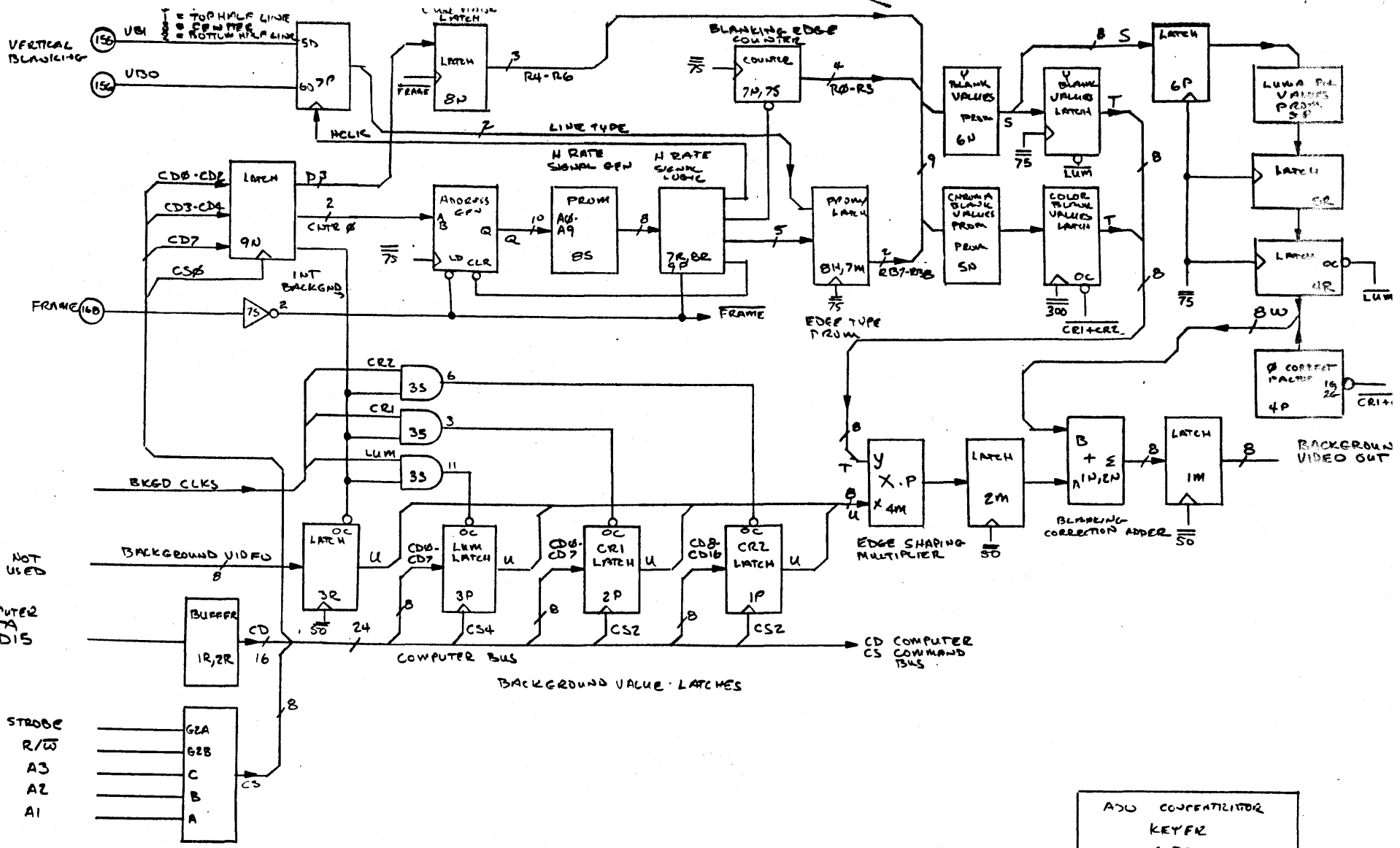
A

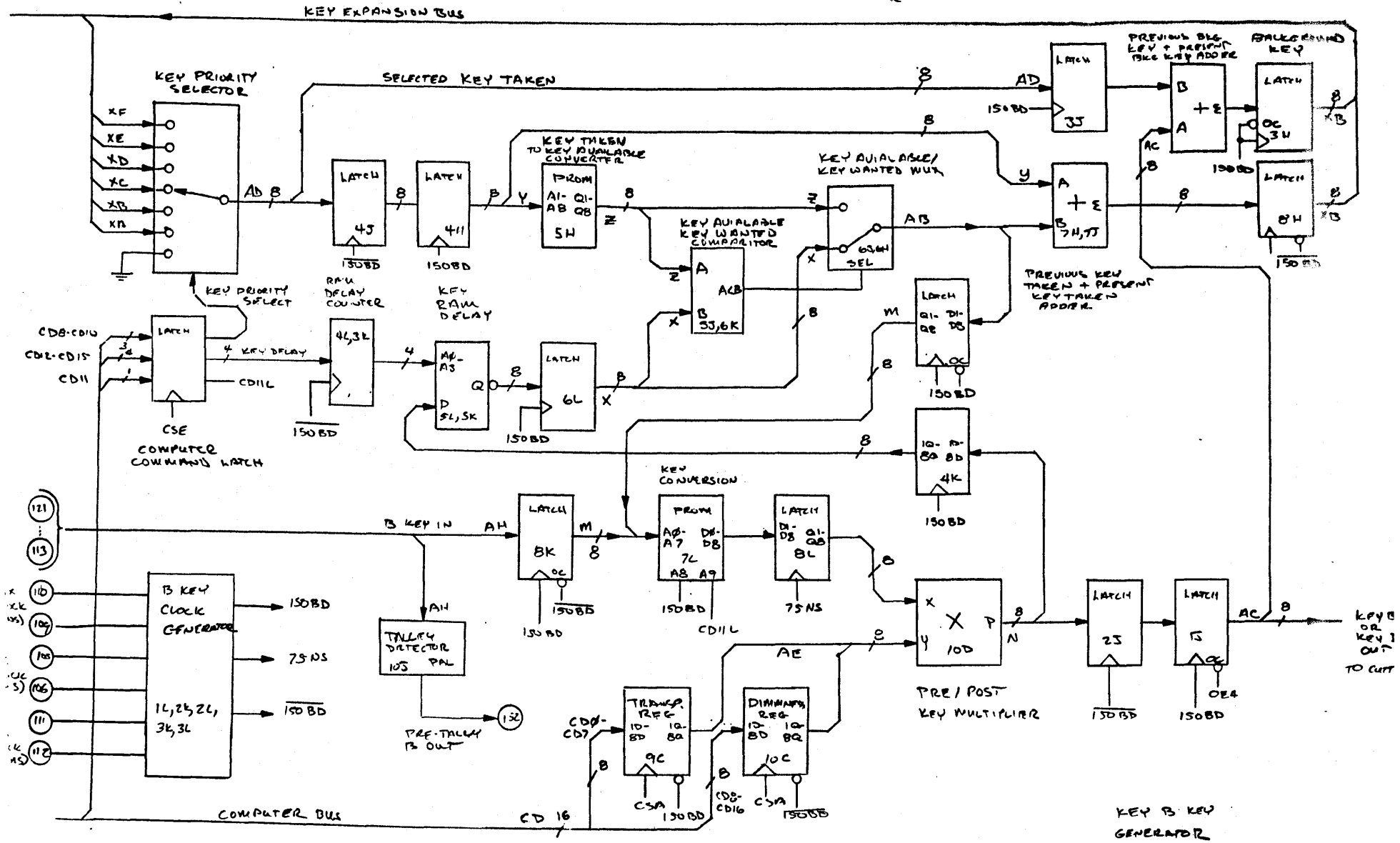
CS

8

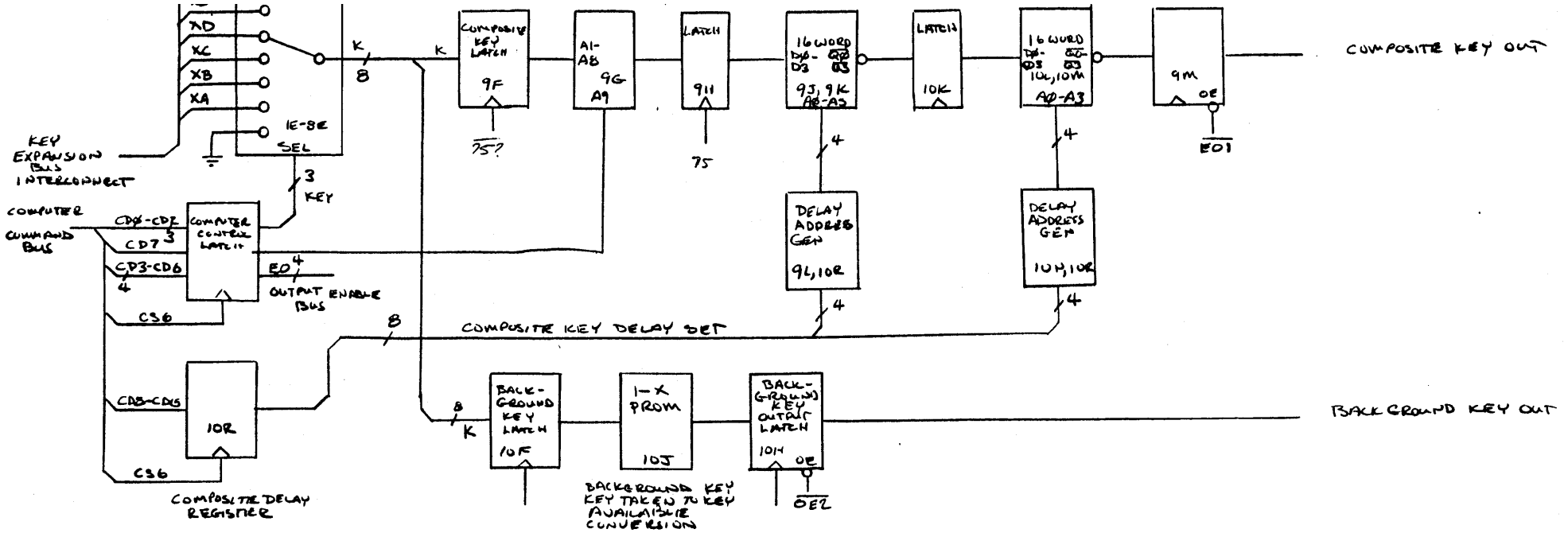
ADO CONCATENATOR KEYER COLOR BACKGROUND GENERATOR 2 OF 3

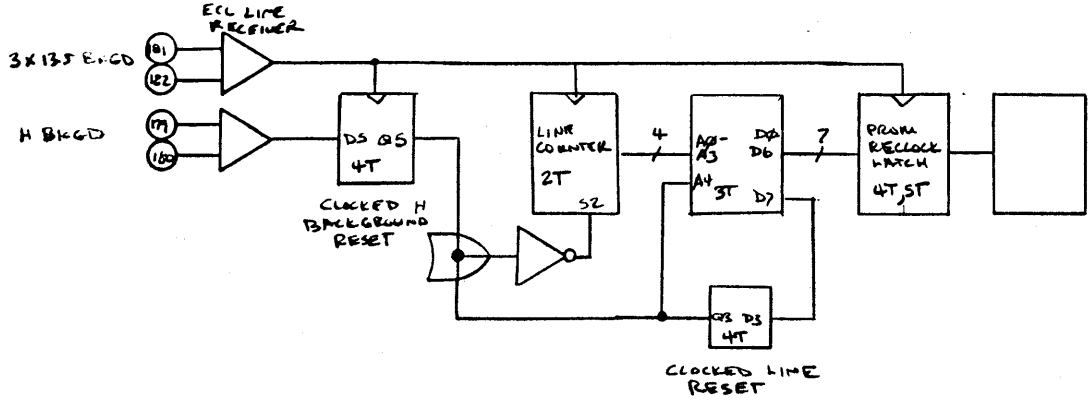
3-26C


VERTICAL BLANKING
VBH
VBO
T = TOP HALF LINE
C = CENTER
B = BOTTOM HALF LINE
HCLK
FRAME
LINE TYPE
R4-R6
BLANKING EDGE COUNTER
R0-R3
BLANK VALUES PROM
BLANK VALUES LATCH
LUMA BLK VALUES PROM
CHROMA BLANK VALUES PROM
COLOR BLANK VALUES LATCH
CD8-CD2
CD3-CD4
CD7
CSØ
INT BACKGND
H RATE SIGNAL GEN
H RATE SIGNAL LIGHT
EDGE TYPE PROM
CR2
CR1
LUM
BKGD CLKS
BACKGROUND VIDEO
NOT USED
COMPUTER ATA -D15
BUFFER
CD
COMPUTER BUS
CD COMPUTER CS COMMAND BUS
EDGE SHAPING MULTIPLIER
BLANKING CORRECTION ADDER
BACKGROUND VIDEO OUT
STROBE
R/W
A3
A2
A1
BACKGROUND VALUE LATCHES
ADJ CONFIDENCE KEYER COLOR BACKGROUNDS GENERATOR 2 OF 3


KEY EXPANSION BUS
KEY PRIORITY SELECTOR
SELECTED KEY TAKEN
XF
XE
XD
XC
XB
XA
AD B
LATCH 4J
LATCH 4H
150BD
RAM DELAY COUNTER
KEY RAM DELAY
PROM A1- Q1- AB QB 5H
KEY TAKEN TO KEY AVAILABLE CONVERTER
KEY AVAILABLE KEY WANTED COMPARITOR
A B ACB 33,6K
KEY AVAILABLE/ KEY WANTED MUX
6,9H SEL
AB
LATCH AD 150BD 3J
PREVIOUS KEY TAKEN + PRESENT KEY TAKEN ADDER
A B + Σ 7H,7J
LATCH 3H
BACKGROUND KEY
LATCH 8H
150BD
KEY PRIORITY SELECT
CD8-CD10
CD12-CD15
CD11
LATCH
4 KEY DELAY
CD11L
CSE
COMPUTER COMMAND LATCH
4L,3L
150BD
A0-A3 D Q 5L,5K
LATCH 6L
LATCH Q1- DB QB
150BD
121
113
116
106
105
106
111
112
B KEY IN
AH
LATCH 8K
150BD
KEY CONVERSION
PROM A0- A7 DB- DB 7L A8 A9
150BD
CD11L
LATCH D1- DB Q1- QB 8L
75NS
1Q- 8Q 8D 4K
150BD
B KEY CLOCK GENERATOR
1L,2L,3L,3L
150BD
75NS
150BD
TALLY DETECTOR 10J PAL
AH
PRE-TALLY B OUT
132
TRANSP. REG 1D- 8D 1Q- 8Q 9C
DIAGNOST. REG 1D- 8D 1Q- 8Q 10C
CD8- CD7
CD8- CD16
CSA
150BD
AE
X Y P 10D
PRE / POST KEY MULTIPLIER
LATCH 2J
LATCH 1J
150BD
OE4
AC
KEY B OR KEY A OUT TO CUFF
COMPUTER BUS
CD 16
KEY B KEY GENERATOR

2-26-5





A0 CONCENTRATOR KEYER
COMPOSITE AND BACKGROUND KEY GENERATION

5-26

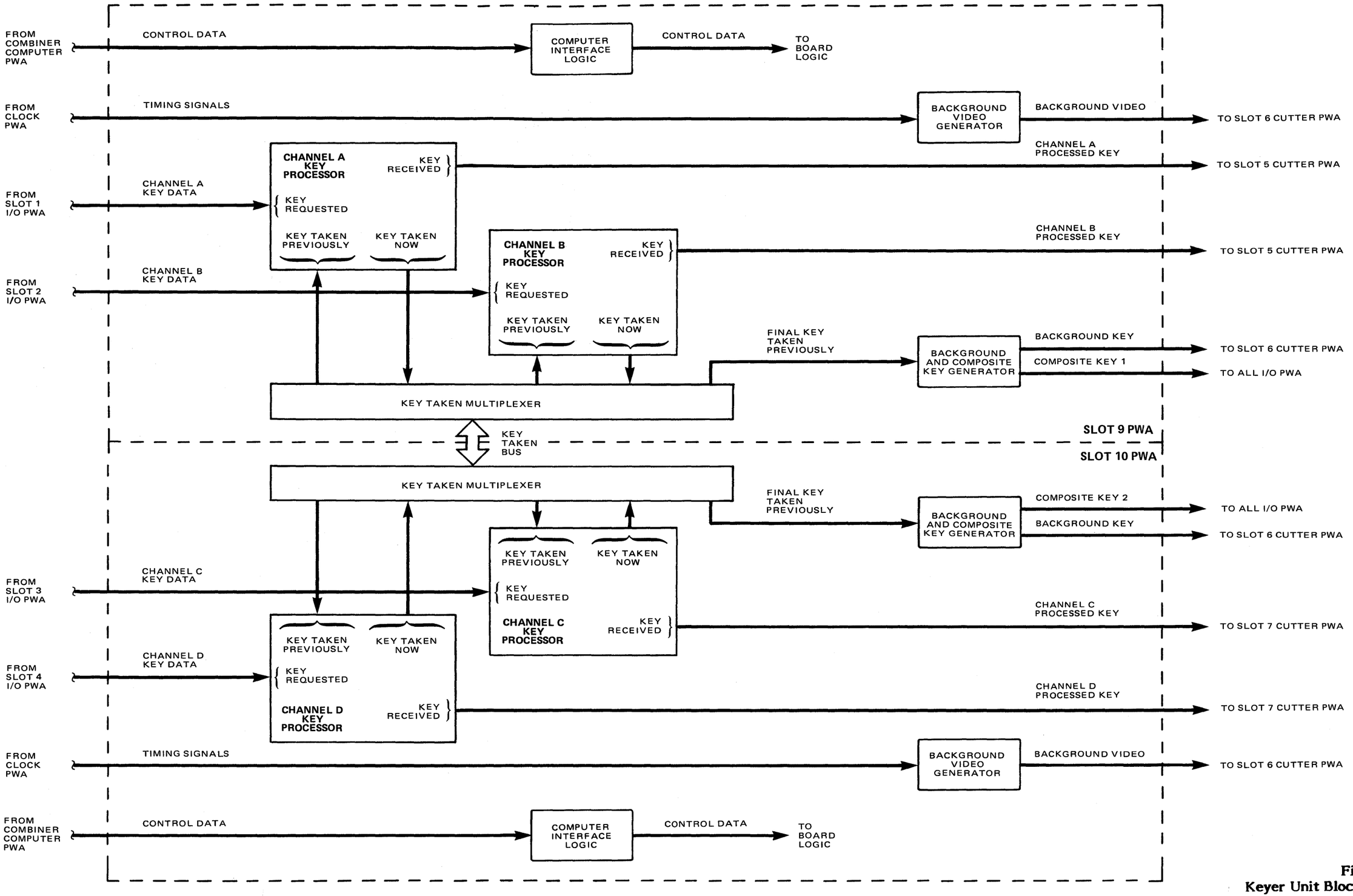


Figure 3-11.
Keyer Unit Block Diagram

processor produces a key-received output. This output will be the same as the key-requested input when the key-taken-previously input indicates it is available. At other times, key-received output will be what is available. Key-received output is fed to the multiplier logic which multiplies it by a number between 0 and 1. If no dimming is desired, the number will be 1. Dimming increases as the number approaches 0. The key-received number, less dimming if desired, is fed out of logic and becomes channel-processed key data to the Cutter PWA.

The key-taken-now output is produced in two ways: one way shows the effect of dimming, if it occurs, and one does not. Both key-taken signals are multiplexed onto the key-taken-now bus. The output which shows the effect of dimming is used to produce the background key data. This causes a scene to be dimmed to the background. This output is produced by the key-taken adder which adds the key-received-after-dimming signal to the key-taken-previously signal. The output used to produce the composite key signal does not show the effect of dimming since this would give the combine transparency in response to the dimming function. This output is produced by the priority processor by adding the key-taken-previously input to the key-received output.

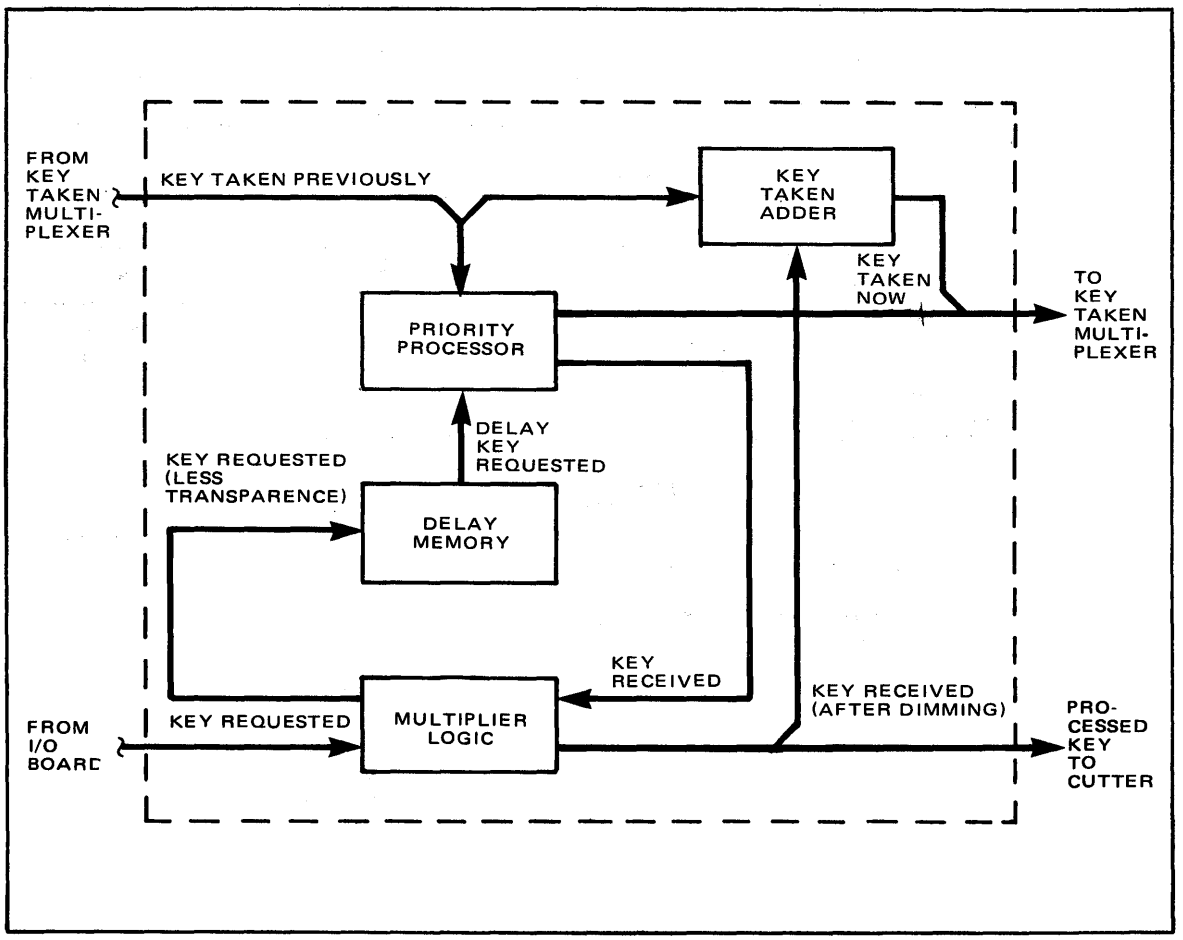


Figure 3-12. Channel Key Processor Block Diagram

3-43 Multiplier Logic

Multiplier logic in a channel key processor is illustrated on sheet 4 of the Keyer PWA schematic in Section 5. It contains ICs 8B, 7A, 8A, 9B, 10B, 10A, 2C, and 1C. This multiplier logic is in the channel A key processor when the PWA is in slot 9 and in the channel C key processor in slot 10. (The logic for channels B and D is on sheet 5. Because it is the same, it will not be described here.) Key-requested input is fed to register 8B. It is clocked in by the 0.5X clock fed to pin 11. Output of this register is enabled for one-half of each byte period by key data byte rate clock 0.5X. Register output is fed to address inputs of PROM 7A. This PROM converts the signed-number input to an unsigned binary fraction. The converted output is clocked into register 8A and fed to inputs of multiplier 10A. The transparency factor, held in register 9B is also fed to the multiplier at this time. The product of these two numbers is fed back to delay memory input register 4B. The key-received input to the multiplier logic is fed to PROM 7A from register 7B. The output of 7B is enabled by the 0.5X clock, causing it to be enabled during the time that 8B is inhibited. These inputs do not access the same addresses as the key-requested inputs since address line A8 is always low when key-received inputs are enabled and high when key-requested inputs are enabled. The PROM does not modify this input but effectively passes it through to register 8A. When 8A feeds key-received data to multiplier 10A register 10B is enabled and feeds the dimming factor to the multiplier. The product of these two numbers is clocked into register 2C and then 1C. The output of 1C is the channel-processed key data fed to the Cutter PWA. It is also fed to the key-taken adder.

3-44 Delay Memory

The delay memory contains registers 4B and 6A, RAMs 5B and 5A, and counter 4A. Delay is produced by storing data in RAMs 5B and 5A for a short period of time. Addresses to the RAMs follow a recycling sequence. As each address is accessed, the byte which had been stored there the previous time the address was accessed is read out. Then, the byte being read out is replaced by a new byte. The new byte remains until the address sequence returns again to this address and it is read out and replaced. This read/write procedure causes bytes to be stored for the amount of time it takes for addresses to recycle. Addresses for RAMs are produced by counter 4A. This counter is incremented by the 0.5X clock at the key data byte rate. Each time the counter recycles it is preset by the carry out signal to a binary number supplied on the G0 through G3 lines. Consequently, address recycle time, and delay time, are controlled by this number. Data is fed to the RAMs from register 4B. RAM outputs are clocked into register 6A.

3-45 Priority Processor

The priority processor contains ICs 4C, 4D, 5D, 5C, 6B, 6C, 6D, 7B, 7C, 7D, and 8D. Key-taken-previously data is clocked into register 4C during the time it is not affected by dimming. The data is then clocked into register 4D in step with delay memory outputs from register 6A. The key-taken-previously data is converted to its inverse by ROM 5D to obtain key-available. Key-available is compared to the key requested by comparators 5C and 6B. If key-available is equal to or greater than the key requested, the comparator output at 6B-7 goes low. This selects the key-requested input to multiplexer 6D/6C to be clocked into register 7B as the

key-received output. Otherwise, key-available is clocked in. The key-taken-previously output of 4D is fed to adder 7C/7D along with the key-received output of 6C/6D to produce the key-taken-now output. This sum is clocked into register 8D and put on the key-taken bus when the outputs of 8D are enabled.

3-46 Key-Taken Adder

The key-taken adder contains ICs 3C, 2D, 1D, and 3D. The key-taken-previously input is clocked into register 3C and fed to adder 2D/1D. The key-received-after-dimming signal is fed from register 1C to the adder. The sum of these two numbers is clocked into register 3D and put on the key-taken bus when the outputs of 3D are enabled.

3-47 Key-Taken Multiplexer

The key-taken multiplexers on PWAs in slots 9 and 10 are interconnected so that key-taken inputs to either one can be fed out of either one. The multiplexer on each board consists of 24 interconnected IC multiplexers. The eight IC multiplexers designated 1F through 8F (illustrated at the top of sheet 4) provide the key-taken-previously input to the channel A processor when this card is in slot 9. (In slot 10 this logic provides the key-taken-previously input to the channel C processor.) The source of inputs to these ICs is listed in Table 3-2. The table also lists the source of inputs for the same logic in slot 10. Selection of inputs to 4C and 3C on sheet 4 is controlled by bits from computer interface register 8C. ICs 1G through 8G at the top of sheet 5 provide the key taken input to channel B and D processors for slots 9 and 10, respectively. The key-taken input to the background and composite key generator is provided by 1E through 8E on sheet 3. Table 3-2 is also applicable to the multiplexer ICs on sheets 5 and 3.

3-48 Background and Composite Key Generator

The background and composite key generator contains the logic on the upper half of sheet 3. It generates background and composite key data. Background key data is

Table 3-2. Multiplexer Signal Sources

Signals	PWA Slot	Channel Source	Signals	PWA Slot	Channel Source
XA0-XA7	9	A	XA0-XA7	10	C
XB0-XB7	9	B	XB0-XB7	10	D
XC0-XC7	9	C	XE0-XE7	10	A
XD0-XD7	9	D	XF0-XF7	10	B

produced by registers 10F and 10H and PROM 10G. Key data taken from the multiplexer is clocked into 10F during the half of each byte time that data shows the effect of dimming. The output of 10F is converted to its inverse by PROM 10G. PROM outputs are clocked into register 10H and fed to slot 6 Cutter PWA. Composite key data is produced from key-taken data that is not affected by dimming. This data is clocked into register 9F and fed to PROM 9G. PROM 9G converts the data to the ADO number system of signed binary numbers. The PROM output is clocked into register 9H and fed to delay logic. The delay compensates for time used to process video data in the cutter and adder boards. The delay logic functions the same as that described for delay logic containing RAMs 5B and 5A on sheet 4. Delay is produced first by RAMs 9J and 9K and then by 10L and 10M. Two delays are used because one is not always adequate to produce the required amount of delay. Delayed key data is clocked into register 9M and fed to I/O PWAs.

3-49 Computer Interface Logic

The computer interface logic contains ICs on all four sheets of the schematic. It receives data bits, address bits, a read/write bit, and a strobe bit from the Combiner Computer PWA. The logic stores control bits required by the Keyer PWA. Computer interface logic contained on sheet 2 consists of ICs 1R, 2R, 2S, 9N, 1P, 2P, and 3P. Decoder 2S receives address lines, a read/write bit, and a board strobe. It decodes chip select pulses to load data in interface logic registers. Buffers 1R and 2R buffer the computer data bus and feed CD0 through CD15 data bits to interface registers. Register 9N holds bits to control the generation of background video synchronization pulses. Registers 3P, 2P, and 1P hold luminance and two chrominance bytes to generate the background video. Computer interface logic on sheet 3 consists of ICs 9E and 10P. Register 9E controls source selection of key-taken data to background and composite key generators. It also controls tri-state outputs of key data. Delay time of the composite key output is controlled by register 10P. Computer interface logic on sheet 4 consists of ICs 8C, 9B, and 10B. Register 8C controls the source selection of key-taken data to the channel A (or C in slot 10) key processor. It also controls the input delay for this processor. Registers 9B and 10B control transparency and dimming, respectively. ICs 8J, 9C, and 10C on sheet 5 perform the same functions in the channel B key processor as 8C, 9B, and 10B do in the channel A processor.

3-50 CUTTER PWA

A Cutter PWA cuts away video that is not to appear in a combine. The board has two independent cutter sections, each of which cuts video for one channel. The sections are designated A and B. (See Figure 3-13.) When the board is in slot 5, cutter section A cuts channel A video and section B cuts channel B. Section A cuts channel C when the board is in slot 7 and background video from the Keyer PWA in slot 9 when the Cutter PWA is in slot 6. Section B cuts channel D when the board is in slot 7 and background video from slot 10 when it is in slot 6. A cutter section receives a video and key input. It cuts the video as indicated by the key and produces a cut video output. Cutting is achieved by multiplying bytes of key data by bytes of video data. The board has a computer interface to communicate with the Combiner Computer PWA.

Bytes of key data, received at the key input to a cutter section, have a period of 150 nanoseconds. The video input byte period is 50 nanoseconds. Consequently, two

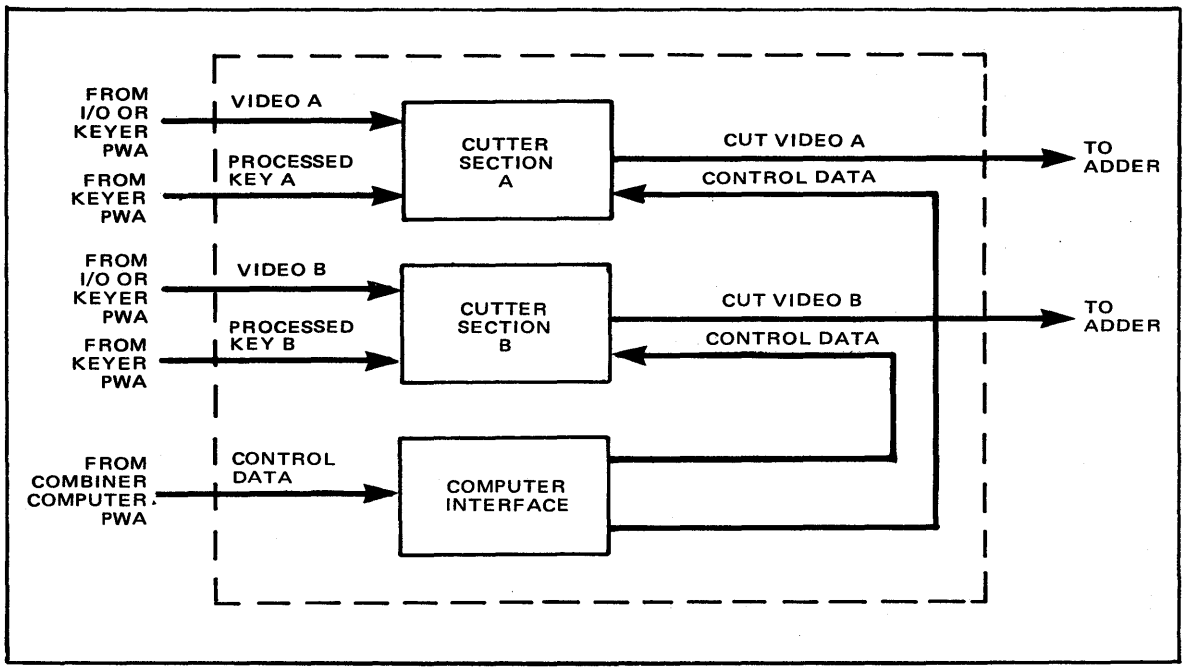


Figure 3-13. Cutter PWA Block Diagram

bytes of luminance are received for one of key. (See Figure 3-14.) Each byte of key is used to cut one byte of luminance. One-half of each byte of key is also combined with one-half of the following key byte to cut another byte of luminance.

Chrominance bytes are functionally grouped in pairs. (C1 and C2 in Figure 3-15 are a pair.) Each pair defines R—Y and B—Y for the same 300 nanosecond period. Since C1 and C2 in a pair represent the same time period, they are cut with the same key. A percentage of each key byte, in a group of four key bytes, is summed to produce a combined key for each functional pair of chrominance bytes. The two latest bytes in each group of four key bytes become the two earliest bytes in the next group.

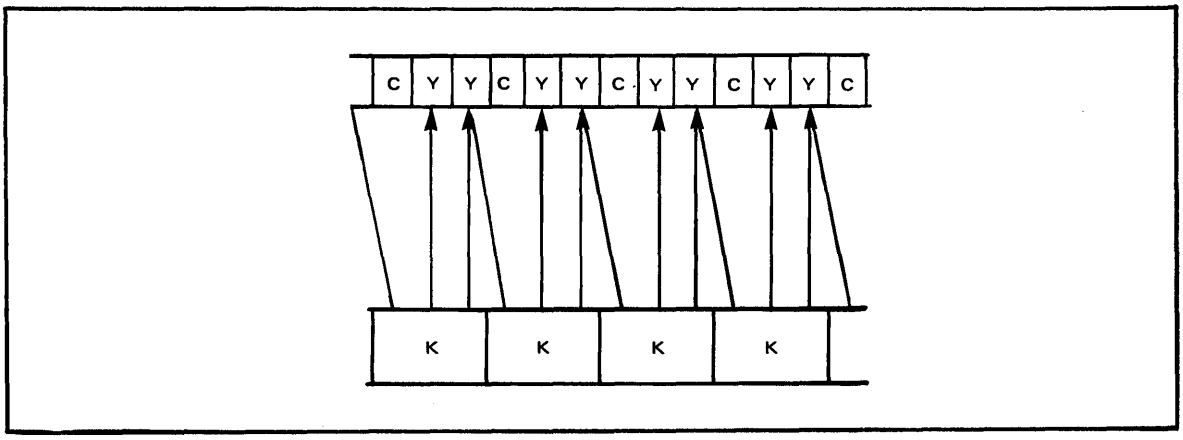


Figure 3-14. Luminance Key Assignments

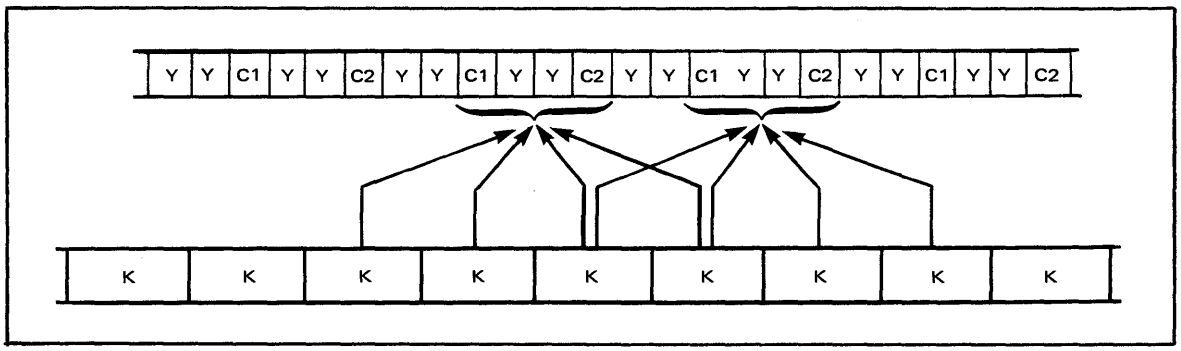


Figure 3-15. Chrominance Key Assignments

3-51 Cutter Section

The key input to a cutter is fed to a variable delay. (See Figure 3-16.) This delay compensates for differences in key processing time in the Keyer PWA. The output of the variable delay is fed to a tapped delay. This delay provides simultaneous access to sequences of key bytes as required to generated combined bytes. Outputs of the tapped delay are fed to the chrominance key processor and the luminance key processor which produce combined key bytes to cut chrominance and luminance bytes. Outputs of the two key processors are fed through a multiplexer to a multiplier. The key multiplexer feeds combined key bytes from the correct sources as required to multiply Y and C video bytes. Cut video from the multiplier is fed to the Adder PWA. Each cutter section has a timing generator to provide clock and control signals required in the section. The 3X and H inputs to a timing generator are from reference video for the combine employing the section.

3-52 Variable-Key Delay

The variable-key delay compensates for key processing time in the Keyer PWA. It also contains a switch to hold the key to its maximum or minimum value during blanking and a detector to recognize the presence of an active key signal for tallying. The variable key delay for cutter section A contains RAMs 1C and 1D, buffers in 2B, counters 1E and 3T, and PAL 2D. (See sheet 2 of the Cutter PWA schematic in Section 5.) Delay is produced by storing data in RAMs 1C and 1D for a short period of time. Addresses to the RAMs follow a recycling sequence. As each address is accessed, the byte which was stored there the previous time the address was accessed, is read out. Then, the byte being read out is replaced by a new byte. The new byte remains until the address sequence returns again to this address and it is read out and replaced. This read/write procedure causes bytes to be stored for the amount of time it takes for addresses to recycle.

Addresses for RAMs are produced by counter 1E. This counter is incremented by the 0.5XA clock. Each time the counter reaches 15, the carry-out presets the counter to the P0, P1, P2, and P3 number. This number controls the delay time.

3-53 Key Switch

The key switch is used to hold the key to a value of 1 or 0 during blanking. When a cutter unit receives reference video, the switch holds the key to a value of 1 during

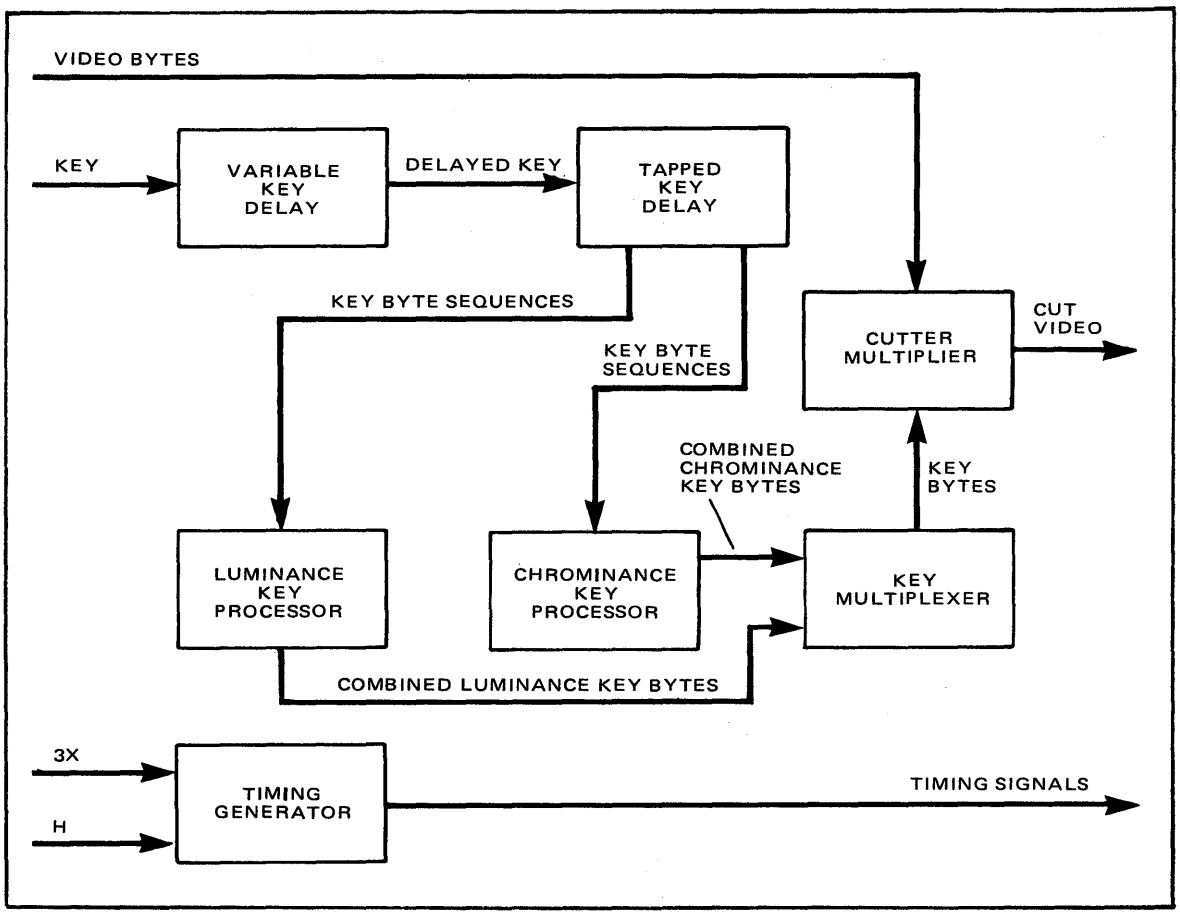


Figure 3-16. Cutter Section Block Diagram

blanking. This causes reference video sync pulses to go through the cutter unaltered. The switch produces a key value of 0 when reference video is not received. The switching function is produced by tri-state buffers in 2B. When $\overline{\text{KEY SWA}}$ to pins 1 and 19 of 2B goes low the outputs of 2B are enabled. If the P5 input to pin 2 is a one, the output is the maximum key value of 10000000. It is the minimum value of 00000000 when P5 is a zero.

3-54 Key Tally Detector

The key tally detector contains PAL 2D and counter 3T. If a channel is visible, the value of the key signal will go above and below a threshold value several times per frame. The detector counts these threshold crossings to detect a key signal present so that channel may be tallied. That portion of the PAL receiving the key input detects key values below the threshold. The output of this logic is fed to another portion of the PAL at pin 13. Input at pin 11 of the PAL is from a similar detector in the keyer. The input at pin 12 selects the input at pin 11 or 13 to be fed to ripple counter 3T. When counter 3T reaches a count of eight, input to 2M-1 inhibits the PAL output to the counter, causing it to stop. The state of the counter is fed to the computer interface and is available to the Combiner Computer PWA so that the computer may pass tally information along to an external device.

3-55 Tapped Key Delay

Tapped key delay for cutter section A consists of shift registers 3B, 4B, 3C, 4C, 3D, 3E, and 4E on sheet 3. Each of the eight key bits is fed to the serial input of one of these shift registers. Delayed bits with delays of one- to eight-byte clock periods are available at the QA through QH outputs.

3-56 Luminance Key Processor

A luminance key processor produces key bytes to cut luminance bytes. The processor for cutter section A consists of registers 6C, 6D, 8C, and 8D, PROMS 7C and 7D, and adders 9C and 9D. Each byte received by the processor is first used as is, then it is averaged with the next byte to produce a combined byte. Byte K0G through K7G from the tapped delay is clocked into register 6C by 1X while byte K0H through K7H is clocked into 6D. Bytes clocked into these registers are clocked in twice. This occurs because bytes shift in the tapped delay at the key byte rate which has half the frequency of the 1X clock. The first time a byte is clocked into 6D it is used unaltered to multiply a byte of luminance. The second time, it is averaged with the byte in 6C and the combined byte is multiplied by a byte of luminance. After the KH and KG bytes have been clocked twice the tapped delay is shifted. The byte that was KG becomes KH. It is then clocked into 6D and used once as is and once averaged with the current KG byte.

The outputs of 6C and 6D are modified by PROMS 7C and 7D. The first time bytes are clocked into these registers the 0.5X clock to address input pin 19 is low. This causes the number in 6D to go through the PROM unchanged and the 6C number to become zero.

The second time the same two key bytes are clocked into registers 6C and 6D, the 0.5X clock to address input pin 19 is high. This causes the numbers in 6C and 6D to be multiplied by one-half by PROMS 7C and 7D.

Outputs of PROMs 7C and 7D are clocked into registers 8C and 8D. The register outputs are added by adders 9C and 9D and fed to register 9H.

3-57 Chrominance Key Processor

The chrominance key processor produces combined key bytes to cut chrominance bytes. It consists of multiplexers 5B, 5C, 5D, 5E, 8G, and 8H, registers 6E, 9E, and 7G, PROM 7E, and adders 9F and 9G.

Four sequential bytes of key data are fed into the chrominance key processor to produce one combined key byte to cut chrominance data. The byte is used to cut a C1 and C2 pair.

When the process repeats to produce the next key byte, key data in the tapped key delay has shifted twice. Consequently, the two most recent bytes used in one combined key byte become the two earliest bytes used in the following combined byte.

Bytes of key data are fed into this processor one at a time at the 1X clock rate. As each byte is received, it is multiplied by a factor between 0 and 1, established by

its position in the sequence. The products produced by multiplying the four key bytes are accumulated in a register and the complete sum is fed out as a combined byte.

Key bytes, selected from the tapped key delay outputs by multiplexers 5B, 5C, 5D, and 5E, are clocked into register 6E by the 1X clock. Register outputs are fed to PROM 7E. The PROM multiplies each byte by a factor established by the A8 and A9 address inputs and the product is clocked into register 9E.

Outputs of 9E are fed to adders 9F and 9G. When the first product of a combined group is in 9E, multiplexers 8G and 8H feed zeros, hard-wired to the multiplexer A inputs, to the adders. The result of this addition, which is the same as the 9E input, is clocked into register 7G.

When subsequent products of the combined key byte are in 9E, the accumulated sum in 7G is fed to adders 9F and 9G by the multiplexers. When four products have been accumulated in register 7G, it holds a combined key byte. This is fed to register 7H.

3-58 Key Multiplexer

The key multiplexer consists of tri-state registers 7H and 9H. Key bytes, to cut luminance and chrominance, are clocked into 9H and 7H, respectively. A timing signal, which is low when luminance bytes are fed to the cutter multiplier, is fed to the output enable terminal of 9H at pin 1. The inversion of this signal is fed to 7H-1.

3-59 Cutter Multiplier

The cutter multiplier multiplies eight-bit key bytes by eight-bit luminance and chrominance bytes and produces a product rounded off to eight bits. Key bytes are binary fractions ranging in value from 0 to 1. Video bytes are signed binary numbers ranging from -128 to +128. Multiplication products are in the same format, and have the same range, as video inputs. The cutter multiplier consists of IC multiplier 3F, registers 1G, 1H, and 2H, adders 3H and 4H, and flip-flop 4G.

Video bytes are clocked into register 1G by 1.5X and fed to the X inputs of multiplier 3F. When luminance bytes are in 1G, the output of register 9H is fed to the Y inputs of 3F. The output of register 7H is fed to the Y inputs of 3F when chrominance bytes are in register 1G. The nine most significant bits from the multiplier output are clocked into register 2H and flip-flop 4G, rounded off to eight significant bits by adders 3H and 4H, and clocked into output register 1H. The outputs of 1H are fed to the Adder PWA.

3-60 Computer Interface

The computer interface consists of ICs 2N, 1S, 1T, and 2T on sheet 4. Decoder 2N decodes strobes to load control data in registers 1S and 1T and to clear key failure detector counters in IC 3T. Tri-state buffers in 2T put the count in 3T counters on MCHBUS data lines D0 through D7.

3-61 ADDER PWA

The Adder PWA receives cut video from Cutter PWAs. This consists of channels A, B, C, and D video and two cut video background matt channels. The Adder PWA adds any two combinations of input video channels simultaneously. The results of either addition can be fed out of the card on any combination of output channels, with the restriction that no output channel can carry both combined video signals at the same time. This restriction is imposed by software to protect output circuits of the board.

The six input video channels are fed to adders No. 1 and No. 2 via input buffers. (See Figure 3-17.) Input-enable signals for each channel are also fed to each adder. Those channels to be added together at any given time are gated into the same adder by active (low) states of associated enable signals.

Provision is made to delay the sum output of adders for one or two cycles of the ECL X 1.5 clock. The delay is controlled by delay-enable lines to the adders.

The output of each adder is fed to an associated output register. Either output register can gate its combined video input to any combination of output channels. Output enable lines to each register control the output gating.

Input enable, delay enable, and output enable signals are produced in the computer interface logic in response to control data received from the Combiner Computer PWA.

3-62 Input Buffers

The input buffers consist of ICs 1B, 1C, 1D, 1E, 1F, 1G, 1H, and 1J. (See the top of sheet 2 of the Adder PWA schematic in Section 5.) Input buffers 1B, 1C, 1D, and 1E receive cut multiplexed luminance and chrominance bytes from channels A, B, C, and D, respectively. Input buffers 1F and 1G receive similar bytes for two background matts. ICs 1H and 1J are spares.

3-63 Adder No. 1

Adder No. 1 contains most of the logic on sheets 2 and 3 of the schematic. This adder adds all eight input numbers together. In a case where two channels are being combined, there will be numbers from these two channel inputs and numbers from a background matt input. The remaining five inputs will be feeding zeros into the addition.

The eight input numbers (including the five inputs feeding zeros into the addition in the example just described) are added together in a series of two-number additions. First, channels A and B are added, channels C and D are added, background matts 1 and 2 are added, and the two spare inputs are added. Next, the sum produced from channels A and B is added to the sum produced from channels C and D while the sum produced from the two matts is added to the sum from the two spare inputs. The channel video sum is then added to the sum produced from background and spare inputs.

Inputs to adder No. 1 come through registers 2B, 2C, 2D, 2E, 2F, 2G, 2H, and 2J at the top of sheet 2. Data is clocked into these registers by the X 1.5 clock when master resets to pin 1 are inactive.

Channel A numbers in 2B are added to channel B numbers in 2C by adders 3B and 3C. The sum produced by this addition is clocked into register 4B. IC 3B adds the four least significant bits from 2B and 2C. The four most significant bits are added by 3C. When a carry occurs from the least significant bits it is fed to the higher-order addition from pin 3B-9.

The sum of channel A and channel B numbers in 4B is added to the sum of channel C and channel D numbers in 4E. This addition is produced by adders 4C and 4D and the sum is clocked into 4K.

The sum of channels A, B, C, and D in 4K is added to the sum of background channels and spare inputs in 4N. This addition is produced by adders 4L and 4M and the sum is clocked into 3N on sheet 3.

Ideally these additions should never add up to more than +127. This follows from the fact that the maximum value of numbers before being cut out is +127. For example, if 50% of +127 is added to 50% of +127, the result should be 100% of +127 or +127. However, round-off errors can cause sums in excess of +127 to occur. An example of this effect is seen in the case of cutting 01111111 (+127) to 50%, which gives 0111111.1 (+63.5). Rounded, this gives 01000000 (+64). Consequently, 50% of +127 plus 50% of +127 adds up to 10000000 which in this number system equals -128.

To prevent this reversal of sign from occurring, logic is included with the addition logic to detect sums in excess of +127. If such a sum is detected at any addition stage, a flip-flop is set. Outputs of these flip-flops are propagated through to set flip-flop 4R-19 on sheet 3. When flip-flop 4R-19 is set, the sum in 3N is not valid and the output of 4R-19 forces the output of multiplexer 3R/3P to 01111111. When 4R-19 is low, the number in 3N is fed through multiplexer 3R/3P.

The sum produced by adder No. 1 at multiplexer 3R/3P is fed out through delay logic containing 3L, 3M, 2K, and 2L. When no delay is required, the outputs of buffers in 3M are enabled by a low input to pins 3M-1 and 3M-19 to gate the data straight through. A delay of one clock period is produced by enabling the outputs of buffers in 2L instead. This feeds the outputs through flip-flops in 3L. When the outputs of flip-flops in 2K are enabled instead of outputs of 3M or 2L, data is clocked through flip-flops in 3L and 3K for a delay of two clock periods.

3-64 Output Register No. 1

Output register No. 1 contains IC registers 1K, 1L, 1M, 1N, and 1P. Outputs of the delay logic are clocked into these registers by the 1.5X clock. Outputs of registers 1K, 1L, 1M, and 1N go to channels A, B, C, and D, respectively. Register 1P is a spare. Data is fed to channels providing video for the combine summed in adder No. 1 by enabling outputs of the associated IC register with a low signal to pin 1. The outputs of these registers are tri-state. They connect to duplicate devices in output register No. 2 allowing either register to feed data to any channel.

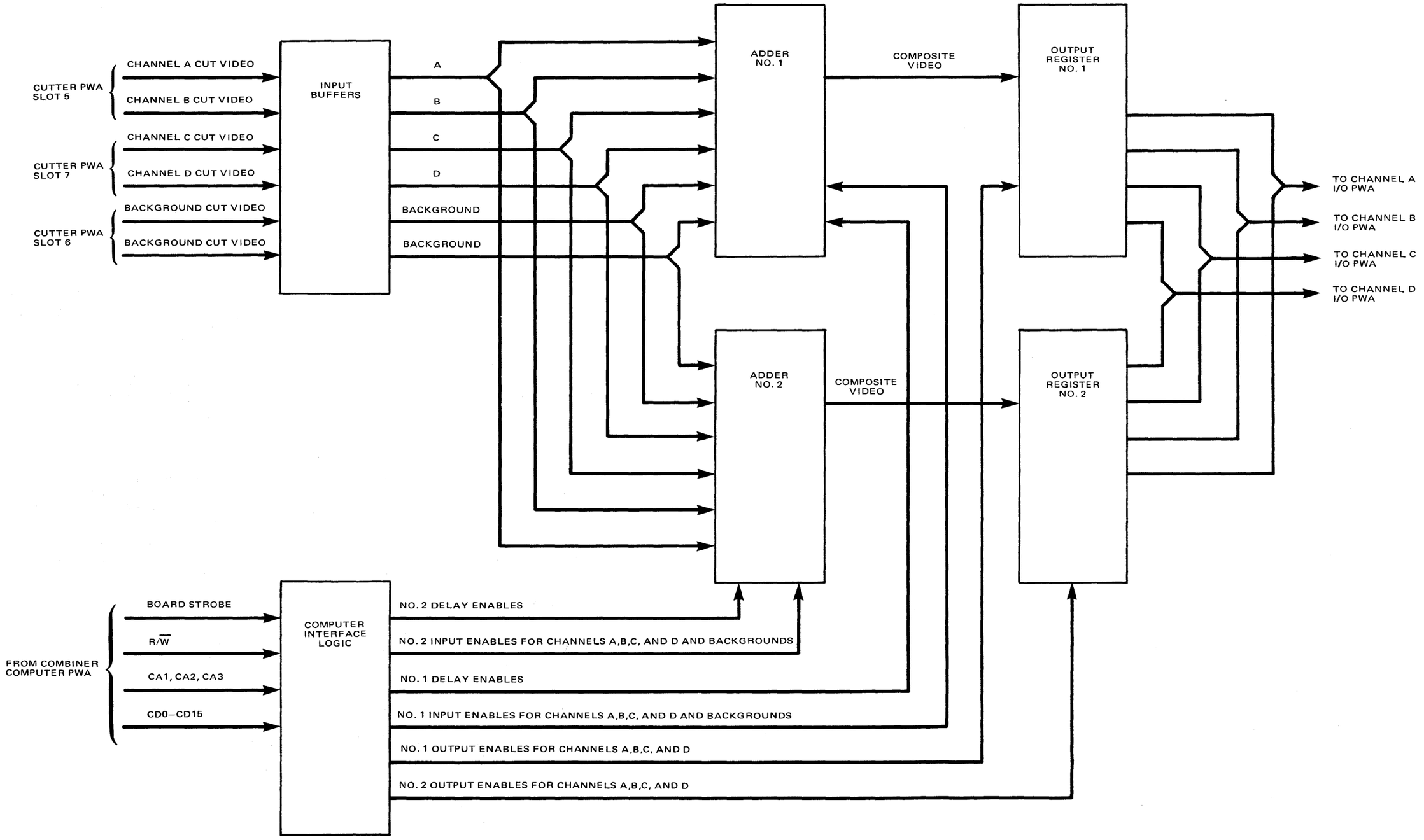


Figure 3-17.
Adder PWA Block Diagram

3-65 Adder No. 2 and Output Register No. 2

Adder No. 2 and output register No. 2 contain most of the logic on sheets 4 and 5. These devices are the same logic configurations as adder No. 1 and output register No. 1. They receive data from the same sources and feed outputs to the same destinations. The only difference between the No. 1 and No. 2 devices is the control signals they receive from the computer interface logic.

3-66 Computer Interface Logic

The computer interface logic contains ICs 3S, 1R, 1S, 2S, and 2R on sheet 3, and ICs 5S and 5R on sheet 5. IC 3S receives a write strobe and address lines from the combiner computer and decodes chip select signals CS0 and CS2. The CS0 signal loads data into 2S and 2R on sheet 2. Data is loaded into 5S and 5R on sheet 3 by CS2. The data to these registers is buffered by 1R and 1S on sheet 1.

Outputs of 2S on sheet 3 enable inputs to addition logic from channels A, B, C, and the background channels as required. Outputs at pin 19, 16, and 15 of IC 2R control the output delay of adder No. 1. Destinations of video outputs of adder No. 1 are selected by outputs of 2R at pins 12, 9, 6, 5, and 2.

Outputs of 5S and 5R on sheet 5 perform the same functions for adder No. 2 and output register No. 2 as outputs of 2S and 2R do for adder No. 1 and output register No. 1.

3-67 CLOCK PWA

The Clock PWA produces timing outputs for use by other PWAs in the concentrator. The outputs consist of X3 and HPHASE signals for channels A, B, C, and D, eight bank clocks, and GO0 through GO11 X3 and HPHASE signals are fed to each I/O PWA. The bank clock and GO0 through GO11 signals are fed to Keyer, Cutter, and Adder PWAs. Timing references, from which outputs are derived, are selected as appropriate for the combines in progress. Gating of selected timing references is controlled by data from the combiner computer.

3-68 X3 and HPHASE Signals

X3 and HPHASE signals are produced by channel I/O clocks selectors. (See Figure 3-18.) When channel A video is used in combine No. 1, the channel A I/O clocks selector gates through the X3A and HA signals to become X3-A and HPHASE-A signals to the channel A I/O PWA. It gates through the X3B and HB signals when channel A video is used in combine No. 2. When channel A video is not used in a combine, it is looped through the I/O PWA and fed back to the signal system. In this case, the CLK0 and H0 signals are gated through. Input selection for this multiplexing function is controlled by the E0 and E1 bits from the setup registers. X3 and HPHASE signals for other channels are produced by other I/O clock selectors in the manner described for channel A.

The CLK0 and H0 signals are produced by the channel A HPHASE adjust counter. This counter receives the PLLX3-A and PLLHPHASE-A signals from the channel A I/O PWA. The PLLX3-A signal is buffered and fed through to become the CLKO

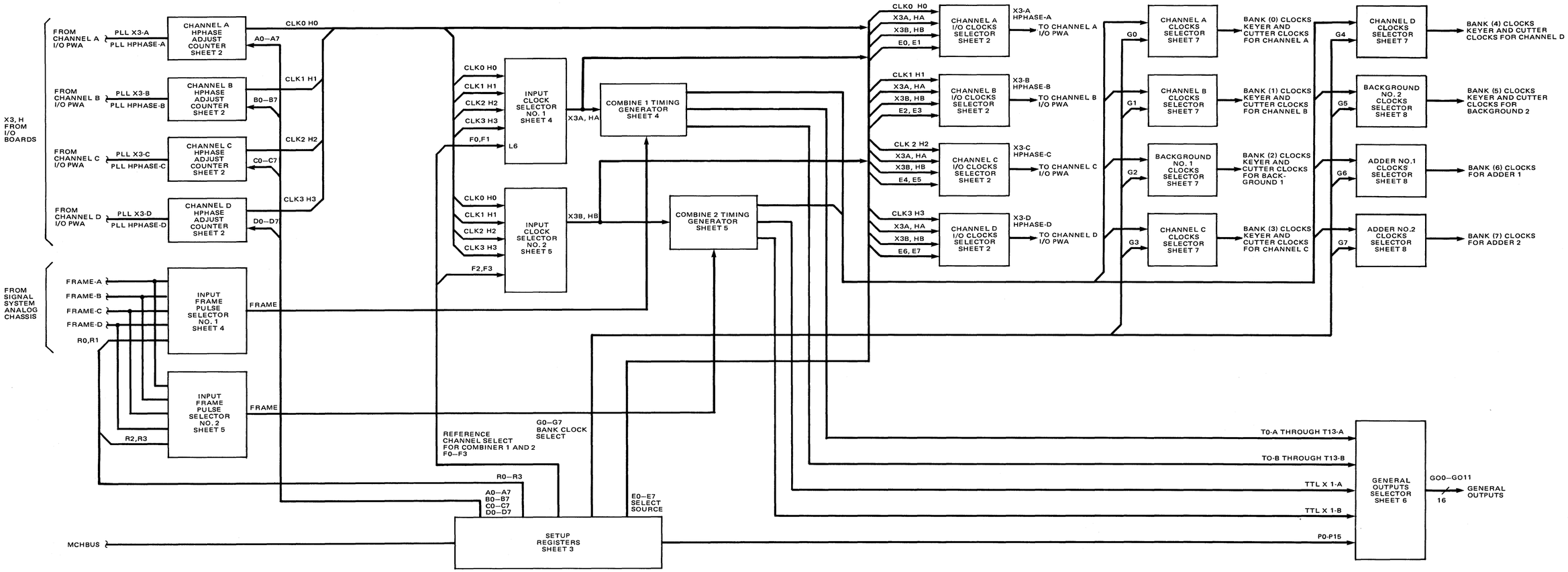


Figure 3-18.
Clock PWA Block Diagram

signal. The phase of the PLLHPHASE-A pulse is shifted some number of cycles of the CLKO signal to produce the H0 output. The amount of shift is controlled by the A0 through A7 bits from the setup registers.

CLK and H signals for other channels are produced by other HPHASE adjust counters in a similar manner to that described for the channel A signals.

The X3A and HA signals are produced by input clock selector No. 1. This selector receives CLK and H signals from HPHASE adjust counters for channels A through D and gates through the inputs from one channel. Selection is controlled by the F0 and F1 bits from the setup registers.

The X3B and HB signals are produced by input clock selector No. 2 in a similar manner to that described for the X3A and HA signals.

3-69 Bank Clock Signals

Bank clock signals are produced by the channel, background, and adder clocks selectors. The bank 0 clocks are used to clock channel A data in the Keyer and Cutter PWAs, in slots 9 and 5, respectively. (See Table 3-3.) Mnemonics for the bank 0 clocks are also listed in the table. The bank 0 clocks are produced by gating through timing signals from the combine No. 1 or No. 2 timing generator outputs. Selection from these two sources is controlled by the G0 signal from the setup register. Other bank clocks are produced in a similar manner. Pertinent data for each set of bank clocks is listed in the table.

Combine No. 1 timing generater produces timing signals for combine No. 1. The timing signals are derived from reference CLK and H signals selected by input clock selector No. 1. The reference signals selected will be from the channel providing reference video. This channel is selected manually by the control unit operator for combine No. 1.

Timing signals for combine No. 2 are produced by combine No. 2 timing generator from reference signals selected by input clock selector No. 2.

3-70 GO0 Through GO11 Signals

The GO0 through GO11 signals are produced by the general outputs selector. Each of these signals is produced by clocking through a corresponding T signal from a timing generator with a clock from the same generator. For example, GO0 is produced by clocking the T0-A or T0-B signal through. If the T0-A signal is clocked through, it is clocked by the TTLX1-A, since T0-A and TTLX1-A are both from the combine No. 1 timing generator. Table 3-4 lists the GO signals plus information on the destination and use of each signal.

3-71 HPHASE Adjust Counters

HPHASE adjust counters shift the phase of the PLLHPHASE signals received from I/O PWAs. Each adjust counter contains three IC counters. (See sheet 2 of the Clock PWA schematic in Section 5.) The counter for channe' A contains IC counters 3K, 4K, and 5K. The three duplicate configurations below the channel A counter are for channels B, C, and D, in that order.

Table 3-3. Clock PWA Bank Clocks

Bank Clock Number	Use	PWA Type	PWA Slot	Clock Mnemonics	Setup Bit
0	Channel A	Keyer and Cutter	9/5	X3, X1, X0.5, H	G0
1	Channel B	Keyer and Cutter	9/5	X3, X1, X0.5, H	G1
2	Background #1	Keyer and Cutter	9/6	X3, H	G2
3	Channel C	Keyer and Cutter	10/7	X3, X1, X0.5, H	G3
4	Channel D	Keyer and Cutter	10/7	X3, X1, X0.5, H	G4
5	Background #2	Keyer and Cutter	10/6	X3, H	G5
6	Adder #1	Adder	8	X3, X1.5, H	G6
7	Adder #2	Adder	8	X3, X1.5, H	G7

Table 3-4. Clock PWA GO Signals

Mnemonic	Channel or Combine	PWA Type	PWA Slot	Function	Setup Bit
GO0	CHA	Cutter	5	KEY SW	P0
GO1	CHB	Cutter	5	KEY SW	P1
GO2	CHC	Cutter	7	KEY SW	P2
GO3	CHD	Cutter	7	KEY SW	P3
GO4	Background #1	Cutter	6	KEY SW	P4

(Continued next page)

Table 3-4. Clock PWA GO Signals (Continued)

Mnemonic	Channel or Combine	PWA Type	PWA Slot	Function	Setup Bit
GO5	Background #2	Cutter	6	KEY SW	P5
GO6	Background #1	Keyer	9	FRAME	P6
GO7	Background #2 -	Keyer	10	FRAME	P7
GO8	Background #1	Keyer	9	VERTICAL BLANKING	P8
GO9	Background #1	Keyer	9	VERTICAL BLANKING	P9
GO10	Background #2	Keyer	10	VERTICAL BLANKING	P10
GO11	Background #2	Keyer	10	VERTICAL BLANKING	P11
GO12	Combine 1	Combiner Computer	27	FIELD IN-TERRUPT TO COMPUTER	P12
GO13	Combine 2	Combiner Computer	27	FIELD IN-TERRUPT TO COMPUTER	P13
GO14	Spare				P14
GO15					P15

The channel A counter is incremented by PLLX3 from the PWA in slot 1. The counter is preset by a pulse derived from the PLLHPHASE signal from the same PWA. The derived pulse is produced by flip-flops in 2K which produce a pulse with a 25 nanosecond width from the 75 nanosecond PLLHPHASE pulse. This limits the preset pulse to one cycle of the incrementing clock. When the channel A counter recycles, the carry out of 5K is clocked into flip-flop 5L. The output of this flip-flop is the H0 signal to the channel A I/O clocks selector. The value of the A0 through A11 preset number to the counter determines the phase shift produced by this counter.

3-72 Channel I/O Clocks Selectors

Channel I/O clocks selectors select the source for X3 and HPHASE signals to I/O PWAs. The selectors are illustrated on the right side of sheet 2. Multiplexers 3L, 4L, 3M, and 4M are contained in selectors for channels A, B, C, and D, respectively.

Multiplexer 3L selects the CLK0, X3A, or X3B input to be the X3 signal to channel A. The selection is controlled by the E0 and E1 bits which also control the selection of HO, HA, and HB to be the HPHASE signal. The HPHASE signal is clocked through flip-flop 2L by the X3 signal to put it into synchronization with this clock.

3-73 Setup Registers

The setup registers receive data from the Combiner Computer PWA to control the functioning of devices on the Clock PWA. The registers are contained on sheet 3.

TTL data is received on the D0 through D15 lines. The data is buffered and fed to registers 1N, 1R, and 1S which store P and R bits. The buffered data is also fed to TTL to ECL translators 2N, 2P, and 2R to produce ECL data K0 through K11. The K data is fed to registers in the lower center of the sheet to store A, B, C, D, E, and G bits.

Address bits, a read/write signal, and a bus strobe are received on the A1 through A7 lines, the R/$\overline{W}$ line, and the $\overline{BS}$ line. Address lines A5, A6, and A7 are decoded by 2U to produce clocks for the various registers. The decoder is enabled by low R/$\overline{W}$ and $\overline{BS}$ signals. Clocks J6 and J7 load TTL registers 1N, 1R, and 1S. J0 through J5 are converted from TTL to ECL by translators in 2T and 2S to clock data into ECL registers.

Functions of setup bits are listed in the table at the lower left corner of sheet 3. Table columns are headed by clocks decoded from the address bits and the lines represent data bits. The first column indicates that bits D0 through D11 control the phase adjustment of the HPHASE signal for channel A after being clocked into a register by J0. (Bits D0 through D11 become K0 through K11 when they are converted to ECL signals. K0 through K11 become A0 through A11 after they are clocked into 4N and 3N by J0. Bits A0 through A11 are fed to channel A HPHASE adjust counter to control the phase of H0.)

3-74 Input Frame Pulse Selector No. 1

Input frame pulse selector No. 1 selects a reference frame pulse for the generation of timing signals for combine No. 1. The selector consists of multiplexer 11H in the upper left corner of sheet 4. Selection is controlled by the R0 and R1 bits from the setup registers.

3-75 Input Clock Selector No. 1

Input clock selector No. 1 selects a reference CLK and H signal for the generation of timing signals for combine No. 1. The selector consists of multiplexer 6L in the upper right corner of sheet 4. Selection is controlled by the F0 and F1 bits from the setup registers.

3-76 Combine No. 1 Timing Generator

The combine No. 1 timing generator produces timing signals used throughout the concentrator to process combine No. 1. This timing generator contains all the logic on sheet 4 except multiplexers 11H and 6L.

Counter 8D, PROM 8E, and flip-flops in 8F produce ECLX1-A, ECLX0.5-A, and ECLX1.5-A clocks. Counter 8D is incremented by the X3 clock. It is reset by the HA pulse. Counter stage outputs are fed to address inputs of PROM 8E. PROM outputs are clocked into flip-flops in 8F to produce reliable logic levels. The output at pin 8F-15 is fed back to preset counter 8D after count 5.

The H0-A through H7-A signals are produced by counters 12L, 12M, and 12N, PROM 12T, latches in 11U, translators 6A and 7A, flip-flops in 6B and 7B, and gates in 6C and 7C. The counters count the X1 clock. They are cleared by the frame pulse and preset at the end of each line by the output of 12K-9. The counter outputs go to address inputs of PROM 12T. The PROM outputs are strobed into latches in 11U. Outputs of 11U latches are converted from TTL to ECL by translators 6A and 7A. The translator outputs are clocked into flip-flops in 6B and 7B. The flip-flop outputs are fed to gates in 6C and 7C. These signals have a minimum pulse width of 75 nanoseconds since the period of the X1 clock is 75 nanoseconds. The common input to gates 6C and 7C consists of low pulses with pulse widths of 25 nanoseconds and a period of 75 nanoseconds. This input limits the high output pulses of the gates to 25 nanoseconds.

The T0-A to T11-A outputs, which are fed to the general outputs selector, are produced from a logical combination of H signals and V signals by programmable array logic (PAL) in 9U and 9S. The outputs of the PALs are clocked into flip-flops in 8U and 8T by the X1 clock. The sixteen flip-flop outputs are designated T0-A through T15-A. The T14-A and T15-A outputs are spares.

The H signals are produced from the outputs of counter 12L, 12M, and 12N. These outputs are fed to PROMs 12R and 12S. The outputs of the PROMs are clocked into flip-flops in 11S and 11T which provide the H0 through H15 outputs.

The V signals are produced by counter 11J, PROMs 11K and 11L, and flip-flops in 11P and 11R. The counter counts line frequency pulses from 11S-9. It is preset to 0 by the frame pulse. The counter outputs are fed to PROMs 11K and 11L. PROM outputs are clocked into 11R and 11P.

3-77 Input Frame Pulse Selector No. 2

Input frame pulse selector No. 2 selects a reference frame pulse for the generation of timing signals for combine No. 2. The selector consists of multiplexer 11G in the upper left corner of sheet 5. Selection is controlled by the R2 and R3 bits from the setup registers.

3-78 Input Clock Selector No. 2

Input clock selector No. 2 selects a reference CLK and H signal for the generation of timing signals for combine No. 2. The selector consists of multiplexer 6K in the upper right corner of sheet 5. Selection is controlled by the F2 and F3 bits from the setup registers.

3-79 Combine No. 2 Timing Generator

The combine No. 2 timing generator produces timing signals used throughout the concentrator to process combine No. 2. This timing generator contains all the logic on sheet 5 except multiplexers 11G and 6K. It is the same configuration as combine No. 1 timing generator and operates in the same manner.

3-80 Channel, Background, and Adder Clocks Selectors

Channel, background, and adder clocks selectors produce the bank clocks. These selectors are illustrated on sheets 7 and 8.

The channel A clocks selector produces the bank 0 clocks. This selector contains 3F and 3E. Multiplexer 3F selects a set of clocks from the No. 1 combine timing generator or a set from the No. 2 generator. The selected clocks are resynchronized by flip-flops in 3E. Selection is controlled by the G0 bit from a setup register.

The remaining selectors are the same configuration as the channel A clocks selector and function in the same manner.

3-81 General Outputs Selector

The general outputs selector produces the GO0 through GO15 outputs. This selector is illustrated on sheet 6. Outputs G14 and G15 are spares.

The GO0 through GO3 signals are produced by 6S, 5S, and 5R. PAL 6S functions as a group of multiplexers. The P0 input is a control bit. This bit selects the T0-A or T0-B signal to be fed out at pin 6S-18. The P0 bit also selects the TTLX1-A of TTLX1-B clock to be fed out at pin 6S-17. The low state of P0 selects both -A signals and the high state selects both -B signals. The selected T0 signal is resynchronized by clocking it through a flip-flop in 5S with the selected TTLX1 signal. The P1, P2, and P3 inputs are also control bits. They select T1, T2, and T3 bits, respectively. For each -A signal that is selected, the TTLX1-A clock is also selected to clock the -A signal through a flip-flop. Selected -B signals are clocked by TTLX1-B.

The GO4 through GO13 signals are produced in a similar manner by logic configurations containing PALs 6U, 6N, and 6R.

3-82 COMBINER COMPUTER PWA

The Combiner Computer PWA receives data from control units, which define combines, and sends control data to devices on this board and to other concentrator boards as necessary to produce the combines as defined. This board contains a microprocessor, support logic, and several peripheral devices. (See Figure 3-19.) The devices consist of RAM and ROM with page control, an electrically eraseable ROM, a multiplier, an interrupt controller, a control unit interface, MCHBUS logic, a programmable timer, status switches, diagnostic LEDs, and a maintenance terminal interface. The peripheral devices communicate with the microprocessor via address, data, and control lines.

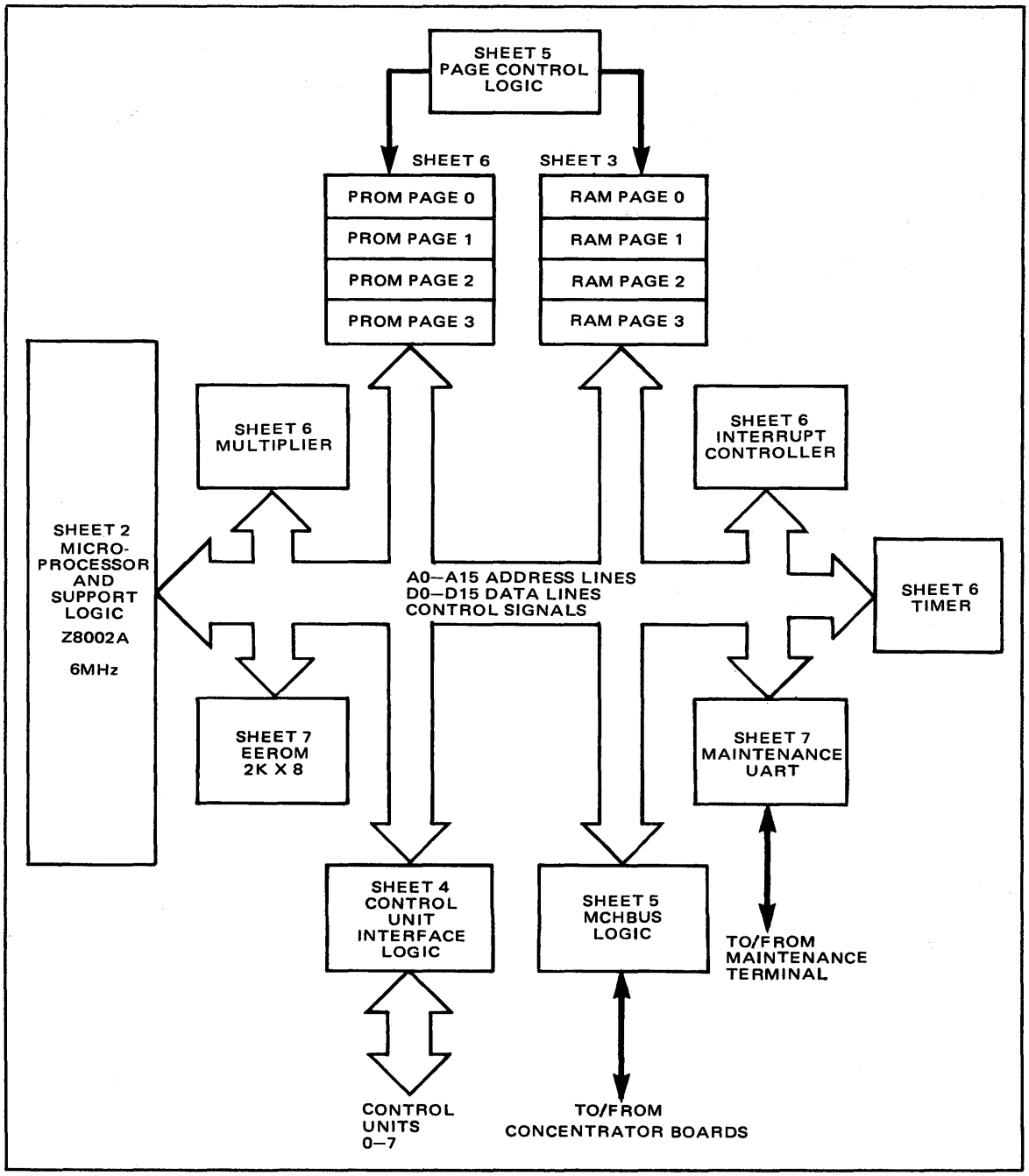


Figure 3-19. Combiner Computer PWA Block Diagram

3-83 Microprocessor

The microprocessor, IC 7M on sheet 2, is a Z8002A. (See Combiner Computer PWA schematic in Section 5.) IC 7M has a clock input and 16 bidirectional data and address lines designated AD0 through AD15. It also has three input control lines and nine output control lines.

Control inputs consist of $\overline{WAIT}$, $\overline{VI}$, and $\overline{RESET}$. An active $\overline{WAIT}$ input to 7M causes it to stop. This is used when required to communicate with slow devices. Vectored interrupt $\overline{VI}$ goes low when there is an interrupt condition. When this occurs, the microprocessor ascertains the source of the interrupt by communicating with the interrupt controller. The $\overline{RESET}$ input puts the microprocessor in its starting condition.

Control outputs consist of B/$\overline{W}$, R/$\overline{W}$, $\overline{MREQ}$, $\overline{DS}$, ST0, ST1, ST2, ST3, and $\overline{AS}$. The B/W lines indicates whether the computer wants a byte or a word when it addresses RAM. Read/write line R/$\overline{W}$ indicates whether data is to be loaded or retrieved from memory and other devices. Memory request line $\overline{MREQ}$ goes low to indicate that a RAM or ROM is to be accessed and high for other devices. Data strobe $\overline{DS}$ is used to strobe data in or out of the microprocessor. Status bits ST0, ST1, ST2, and ST3 tell what the microprocessor is doing. These outputs are useful in decoding equipment strobes. Address strobe $\overline{AS}$ is used to strobe addresses from the AD0 through AD15 lines into an external address register.

3-84 Microprocessor Support Logic

The microprocessor support logic contains everything on sheet 2 in addition to microprocessor 7M and the logic on sheet 7 that generates the $\overline{WAIT}$ input to 7M. Pulse generator 8T produces a reset pulse when power is applied or when the reset button on the board is pressed. Crystal-controlled oscillator 7C produces a TTL clock at a frequency of 4.9152 MHz to clock the 7M. Counters 8F and 9F divide the clock frequency to produce additional clocks at lower frequencies. Registers 6K and 6R store addresses from the computer to free the AD0 through AD15 lines to carry data. Bidirectional buffers 6L and 6P buffer the computer output except when the data strobe occurs during a read instruction. In this case, they buffer the computer input. Buffers in 7K buffer control line outputs of 7M. PAL 6G and decoder 3L decode control signals which select devices to be accessed. Decoder 3L is inhibited except when 6G decodes $\overline{DEVICES}$. This signal enables 3L which then decodes address lines A3, A4, and A5. Outputs of 6G and 3L are listed in Table 3-5 which indicates the function of each.

Table 3-5. Decoded Control Signals

Signal	Function
MCHBUS	Enables communication with other PWAs.
REGSEL	Enables register decoder 3F.
MEMORY	Selects RAM or ROM instead of other devices mapped into memory.
I/D	Indicates if ADO through AD15 carry instruction or data.

(Continued next page)

Table 3-5. Decoded Control Signals (Continued)

Signal	Function
DEVICES	Used to expand decoding by enabling decoder 3L.
VIAC	Vectored interrupt acknowledge.
REFRESH	Refreshes the dynamic RAM.
EEROM	Enables fetch from or write to the electrically eraseable ROM.
CHA	Enables communication with the control unit for combine No. 1.
CHB	Enables communication with the control unit for combine No. 2.
SWITCHER	Not used in this application.
MNTCE	Enables communication with diagnostic terminal.
TIMER	Enables programming of one of the three available timers.
INTCTLR-B	Allows communication with interrupt controller B.
INTCTLR-A	Allows communication with interrupt controller A.

The $\overline{\text{WAIT}}$ input to microprocessor M7 comes from gate 2L-6. (See sheet 7.) When a slow device is accessed that requires a wait of no more than one cycle of CPUCLK, the wait is produced by shift register 3R. An example is EEROM 6T which is also on sheet 10. When M7 is going to access 6T the $\overline{\text{EEROM}}$ signal is decoded. This is fed to pin 11 of NAND gate 3M, causing the load input of register 3R, at pin 9, to go high (inactive). Previously, the active load input had put ones into flip-flops A, B, and D of 3R and a zero into C. When $\overline{\text{EEROM}}$ goes low the zero is clocked into D followed by ones to produce a single wait state. When a wait of more than one cycle of CPUCLK but less than two is required, shift register 3P produces the wait period. This register receives a zero in both flip-flops B and C. The $\overline{\text{PAUSE}}$ input to pin 5 of gate 2L is from the interrupt controller. The length of this wait is variable depending on how long it takes the controller to generate a vector code. The input to pin 4 of gate 2L is for testing purposes.

3-85 Page Control Logic

The board contains eight pages of memory, four of PROM and four of RAM. Any four pages are directly addressable at any one time. Addressable pages are selected by control signals from the page control logic. (See sheet 5.) Control signals are decoded from bits held in page registers 5E and 4E. Decoding is performed by PAL 6E.

The bits in page registers that select current pages 0, 1, 2, and 3 are listed in the lower left table on sheet 5. The code for each page is listed in the table on the right. The code that selects the current page to be accessed is listed in the middle table.

3-86 RAM and Associated Logic

The RAM is illustrated on sheet 3 of the schematic. It contains four pages of 32K bytes each and consists of RAM ICs 8J through 8S and 9J through 9S. Each RAM IC has 64K addresses with one bit at each address. The 16 RAM ICs comprise a 64K address memory with a 16-bit word at each address. The 64K addresses are divided into four pages by the RAM0 and RAM1 signals. Each page contains 16K addresses with a high and low order 8-bit byte at each address.

RAM ICs require 16 address bits. They are fed to the A0 through A7 address lines in two bytes. The row address bits are clocked in by a low pulse to row address strobe input $\overline{RAS}$. Column address bits are clocked in by a pulse to $\overline{CAS}$. The D and Q terminals are data in and data out, respectively. The data output is tri-state and is enabled by an inactive (high) state of write input $\overline{W}$.

Associated logic consists of bidirectional buffers 7P and 7L, multiplexers 6S, 7R, 9H, and 9G, and flip-flop 7J-9.

Multiplexers 6S and 7R select eight lower or eight upper address bits for row or column address bits, respectively. The selected address bits are fed to the RAMS through buffers in 7S. These buffers are designed specifically to drive MOS loads that have special voltage and drive specifications.

An odd write strobe to RAMs 8J through 8S and an even one to 9J through 9S are produced by multiplexer 9H and buffered by memory drivers in 8H. The odd and even strobes load bytes RD0 through RD7 and RD8 through RD15, respectively. When byte/word signal B/$\overline{W}$ is in the byte state and a write pulse occurs on the R/$\overline{W}$ line, one of the strobes will be produced. Selection is controlled by address bit A0. When this bit indicates an odd address, the odd write strobe is produced. Otherwise, an even one is produced. The word state of B/$\overline{W}$ causes both an odd and an even strobe to be produced in response to a write pulse.

ICs 7P and 7L buffer the RAM data inputs and outputs. Direction is controlled by read/write signal R/$\overline{W}$. Tri-state outputs of the buffers are enabled by a low chip select input to pin 19. Chip select signals are produced by 9G and fed to the buffers when 8G gates are enabled by $\overline{RAMSEL}$. When R/$\overline{W}$ is in the write state, chip select is produced in response to write strobes to the RAM. An active state of data strobe $\overline{DS}$ produces chip select when R/$\overline{W}$ is in the read state.

3-87 ROM and Associated Logic

The ROM is illustrated on sheet 6 of the schematic. It contains four pages of 32K bytes each and consists of ROM ICs 5M, 5P, 5S, 5T, 4M, 4P, 4S and 4T. Each IC ROM contains 16K addresses with a byte at each address. Each page contains two IC ROMs.

Associated logic consists of decoder 6J. This IC decodes PROM 0 and PROM 1 signals from the page control logic. When the ROM has been selected for a fetch, $\overline{\text{PROMSEL}}$ is active. Then, a low strobe to the $\overline{\text{MREQ}}$ input causes the decoder to produce an output enable pulse to the ROMs in one page.

3-88 Electrically Eraseable ROM

The electrically eraseable ROM (EEROM) is IC 6T on sheet 7. This device contains 2K addresses with eight bits at each address. It is used to store setup numbers. A1 through A11 are the address inputs. D0 through D7 are data outputs. $\overline{\text{CE}}$ is the chip enable, $\overline{\text{WE}}$ is the write enable, and $\overline{\text{OE}}$ is the output enable.

3-89 Multiplier

The multiplier consists of IC multiplier 5F and decoder 4H on sheet 6 and register 5D on sheet 6. It is provided to save microprocessor time.

IC 5F multiplies a 16-bit X input by a 16-bit Y input and produces a 32-bit product. When the CLK-X input to 5F receives a high pulse, the leading edge clocks the 16-bit X input into the multiplier. The leading edge of a low pulse to input CLK-Y clocks the Y input in. A low input to TRIM puts the 16 most significant bits of the product on the MSP output lines. The 16 least significant bits are put on the LSP lines (which are also Y input lines) by a low input to TRIL. Decoder 4H decodes address lines A3, A4, and A5 to produce CLK and TRI inputs to the multiplier when $\overline{\text{DEVICES}}$ has been decoded by PAL 6G on sheet 2 and address line A6 is low. Decoded outputs are low during data strobe DS.

The mode of the multiplier is controlled by mode inputs TCX, TCY, RND, and FA. When all these inputs are low the X and Y inputs are treated as unsigned binary numbers and a 32-bit unsigned binary product is produced. A high TCX input causes the X input to be treated as a signed number with the sign in the most significant position and negative numbers in the twos complement form. The Y input is treated this way when TCY is high. The product is rounded off to 16 significant bits when RND is high. A high FA input causes the product to have a sign bit in the most significant position of both the most significant product and the least significant product. Register 5D is loaded with status bits from the lower data byte when $\overline{\text{STATUS OUT}}$ is decoded by decoder 3F on sheet 5. Bits D0 through D3 in this register control the state of mode signals to multiplier 5F.

3-90 Interrupt Controller

The interrupt controller contains IC interrupt controllers 2P and 2M. (See sheet 6.) When either of these ICs receives an interrupt it produces vectored interrupt signal $\overline{\text{VI}}$ to microprocessor 7M. IC 7M responds with interrupt acknowledge signal $\overline{\text{VIACK}}$.

When this is followed by data strobe $\overline{DS}$ from 7M the IC interrupt controller that sent the $\overline{VI}$ signal puts a code on data lines D0 through D7, identifying the source of the interrupt.

Interrupts I/O INT 0, I/O INT 1, I/O INT 2, and I/O INT 3 are from the I/O boards for channels A, B, C, and D, respectively. The interrupt is sent when the board has data for the computer that was received on the 9THBIT line. Interrupts TIMER 0, TIMER 1, and TIMER 2 are from timers 0, 1, and 2 in the programmable timer. These interrupts are generated when the corresponding timers time out. CHAINT and CHBINT indicate that data has been sent to the control unit interface for combine No. 1 and combine No. 2, respectively. MNTCEINT indicates the maintenance terminal interface has transmitted a character to the terminal or has received one from the terminal. SWITCHER interrupt is not used in this application.

3-91 Control Unit Interface

The control unit interface allows the concentrator to communicate with two control units at a time, one for combine No. 1 and one for combine No. 2. The interface is illustrated on sheet 4.

Serial digital data from control units is fed to line receivers in the top right corner of the sheet. Receiver outputs are fed to multiplexers 1A and 1B. Multiplexer 1A selects the control unit input for combine No. 1 and feeds it to universal asynchronous receiver transmitter (UART) 7B. IC 7B converts the bit serial input to a bit parallel byte serial output and feeds it to first in first out register (FIFO) 7A on the RD0 through RD7 lines. If a parity, frame, or overrun error occurs, an error indication is fed to pin 7A-24. (The microprocessor will not use data received with an error indication.) The microprocessor reads the data stored in the FIFO. Bytes of data are strobed onto the D0 through D7 lines in the order they were received by low pulses to the $\overline{CSA}$ input. Multiplexer 1B selects the input for combine No. 2 and feeds it to the computer via UART 9B and FIFO 9A. FIFO A EMPTY and FIFO B EMPTY outputs of 7A and 9A go to the microprocessor via status register 5C on sheet 5.

Data from the computer for a control unit is fed to register 6D. If the data is for combine No. 1 control unit it is fed to TD0 through TD7 inputs of UART 7B. UART 7B serializes the data and feeds it to demultiplexer 3C. IC 3C connects to line drivers that feed serial data to the eight control units. The serial input to 3C goes to the line driver that is connected to the control panel controlling combine No. 1. Data for combine No. 2 line driver goes via UART 9B and demultiplexer 2C.

The selection function for combine No. 1 multiplexer and demultiplexer is controlled by signals CHA0, CHA1, and CHA2. These signals are produced by bits stored in register 3B. This register also stores bits to control combine No. 2 selection and bits that indicate if a control unit is connected for combines No. 1 and 2. Outputs of register 3B are connected to LEDs DS1 through DS7 for diagnostic purposes. Register 4D holds bits that turn line drivers on or off. Line drives in use must be turned on. Others may be off or on.

3-92 MCHBUS Logic

The MCHBUS Logic is an interface between the combiner computer board and other concentrator boards. It consists of decoders 1M, 1N, 1P, and 1T, bi-directional buffers 1S and 1R and buffer IC 1U on sheet 5. MCHBUS lines consist of board strobes and address lines out and bidirectional data lines.

Board strobes $\overline{BS1}$ through $\overline{BS32}$ are produced by the decoders. Decoder 2U does a preliminary decode of address lines A11 and A12 when $\overline{MCHBUS}$ is active to produce and enable to one of the other four encoders. The decoder receiving the enable decodes address lines A8, A9, and A10. The decoded board strobe goes low when data strobe $\overline{DS}$ to the decoder input goes low.

Address lines A1 through A7 from external address register 6K/6R on sheet 1 are fed to concentrator boards via buffers in 1U. The R/$\overline{W}$ output of buffer IC 7K on sheet 1 is also fed to the boards via IC 1U.

Computer data lines D0 through D15 are connected to concentrator boards via bi-directional buffers 1S and 1R. Direction of these buffers is controlled by R/$\overline{W}$. Buffer outputs are enabled when MCHBUS is decoded by PAL 6G on sheet 1 and $\overline{DS}$ goes low.

3-93 Programmable Timer

IC 2S on sheet 6 is the programmable timer. This IC contains three independent programmable timers that are controlled by the microprocessor. Timers are programmed by data fed to 2S on the D0 through D7 lines. The data is clocked in by $\overline{TIMER}$ from decoder 3L on sheet 2. One of the three internal timers is selected to receive program data by address lines A1 and A2 to 2S. When a timer times out, it produces an interrupt output on the corresponding timer output line.

3-94 Status Switches

The status switches provide information about system configuration to the microprocessor. They consist of dip switches 5A and 4B on sheet 5. Three of these switches indicate the type of switcher in the system. One indicates if the system uses NTSC or PAL video format. Other switches are spares. Switch outputs are fed to D0 through D15 data lines through tri-state buffers 5B and 4C. When $\overline{SW}$ is decoded by 3F these buffers are enabled and feed switch status data to the microprocessor.

3-95 Diagnostic LEDs

The diagnostic LEDs are provided to check the states of data lines for diagnostic purposes. This circuit contains LEDs DS9 through DS24 on sheet 5. It also contains registers 7U and 7T. When decoder 3F decodes $\overline{LED}$, data on DS0 through DS15 is clocked into 7U and 7T. The outputs of these registers are displayed by the LEDs.

3-96 Maintenance Terminal Interface

The maintenance terminal interface allows certain terminals, as defined in paragraph 4-4, to communicate with the microprocessor for diagnostic purposes. It consists of UART 3J and associated translators. (See sheet 7.) IC 1K is a dc to dc converter. It produces ±12V power required by the interface.

Inputs and outputs of 3J are TTL. Signals to and from a terminal use RS-232 standard. Translators in 2J convert the RS-232 signals to TTL. TTL is converted to RS-232 signals by translators in 1J.

Data for a terminal is received from the microprocessor in bytes at the D0 through D7 inputs. When UART 3J has data for a terminal, it sends request to transmit $\overline{\text{RTS}}$ to the terminal. If the terminal is ready to receive data it sends clear to receive $\overline{\text{CTS}}$ to 3J. The data is then sent bit-serially on the TD output of 3J. After sending a character to a terminal, 3J sends an interrupt to the interrupt controller.

Data for microprocessor 7M is received from a terminal bit-serially on the RD line. UART 3J assembles the bits into a byte and informs 7M that a character is ready by sending an interrupt. When 3J is addressed and receives data strobe DS it puts the byte on the D0 through D7 lines for the microprocessor.

SECTION 4
MAINTENANCE

4-1 INTRODUCTION

This section contains information on test equipment, circuit breakers, fuses, diagnostic terminals, and power distribution.

4-2 TEST EQUIPMENT

Table 4-1 lists standard test equipment used for troubleshooting the concentrator.

Table 4-1. Typical Test Equipment

Item	Description	Type
1	Multimeter	Volt-ohmeter
2	Oscilloscope	Dual Channel, 150 MHz
3	Digital Extender	Ampex Part No. 1409773

4-3 CIRCUIT BREAKER AND FUSES

Locations of the circuit breakers and fuses are illustrated in Figures 1-5 and 1-6. Table 4-2 describes these devices.

4-4 DIAGNOSTIC TERMINALS

Acceptable terminals for diagnostic input to the concentrator are an Ampex D175 or any terminal that has a fixed tab stop such as a Zenith Data Systems H19.

4-5 POWER DISTRIBUTION

Power distribution for 115 and 230 Vac applications are illustrated in drawing 1465060 in Section 5.

Table 4-2. Circuit Breaker and Fuses

Item	Description	Type
1	Circuit Breaker, 25A	Input protection for 120 Vac service
2	Circuit Breaker, 15A	Input protection for 230 Vac service
3	10A Slo Blo Fuse	Minus 5 Vdc power supply protection for 120 Vac service
4	5A Slo Blo Fuse	Minus 5 Vdc power supply protection for 230 Vac service

SECTION 5

PARTS LISTS AND SCHEMATICS

SECTION 5

PARTS LISTS AND SCHEMATICS

(CONTINUED)

NUMERICAL LIST OF ASSEMBLIES

NUMERICAL LIST OF SCHEMATICS

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -00
1	1464402-01	BASIC ASSEMBLY		1
2				
3	1464407-01	120V LINE VOLTAGE KIT	2	1
4	1464408-01	230V LINE VOLTAGE KIT		
5				
6	1464409-01	2 CHANNEL NTSC/PALM KIT	2	1
7	1464410-01	2 CHANNEL PAL KIT		
8				
9	1464568-01	3/4 CHANNEL NTSC/PALM KIT	1 2	1
10	1464569-01	3/4 CHANNEL PAL KIT		
11				
12	1465019-01	SOFTWARE KIT		1
13				
14	1809633-01	ADO CONCENTRATOR MANUAL, THEORY AND MAINTENANCE		1

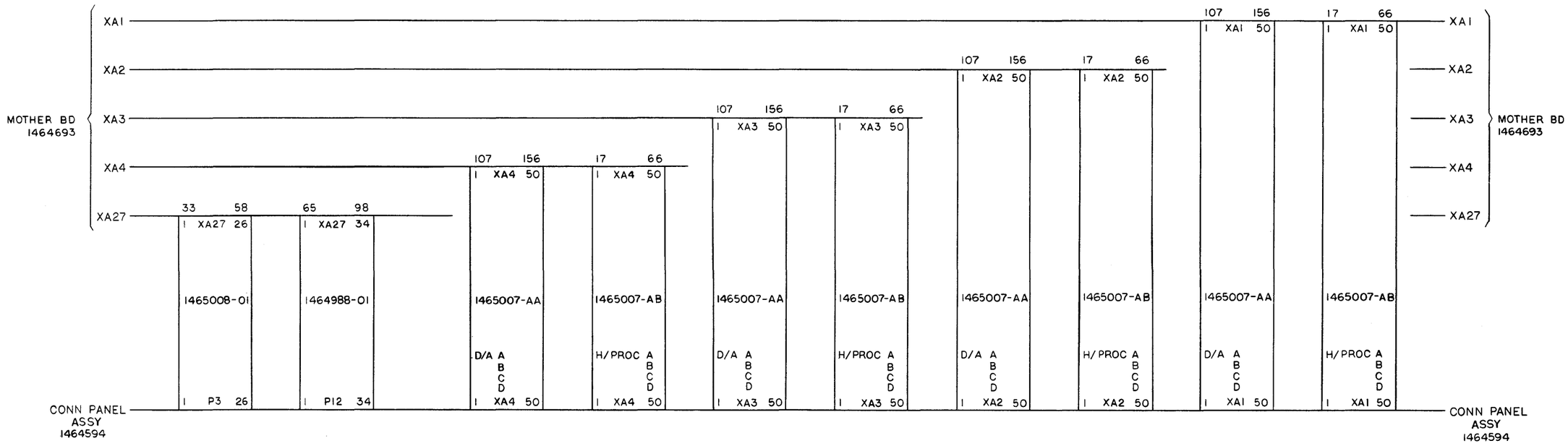
NOTES:

1. ITEM IS AN ACCESSORY AND WILL BE INCLUDED AS DIRECTED BY SALES ORDER.
2. SELECT ONLY ONE AS DIRECTED BY SALES ORDER.

LM-1464600

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1464552-01	CHASSIS ASSEMBLY		1
2	1464570	INTERCONNECT DIAGRAM, 120V/230V CONNECTOR PANEL-MB		(-)
3				
4	1464411-02	PWA, I/O PLL	XA1,2	2
5	1464488-02	PWA, COMPUTER	XA27	1
6	1464519-01	PWA, ADDER	XA8	1
7	1464522-01	PWA, CUTTER	XA5,6	2
8	1465118-01	MISCELLANEOUS PARTS KIT		1
9	6000017-30	NAMEPLATE, IDENTIFICATION		1

LM-1464402



Interconnect Diagram No. 1464570A.
120V/230V Connector Motherboard Panel

ITEM NO.	PART NUMBER		DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER	
					-01	-02
1	1403031-AA	FILTER			1	1
2	1403328-AB	LABEL, WARNING, SHOCK HAZARDS			1	1
3						
4	1420133-AB	PANEL, SIDE (RIGHT)			1	-
5	1420133-AC	PANEL, SIDE (LEFT)			1	-
6	1420134-AA	SUPPORT, DIGITAL CARD (BOTTOM)			1	-
7	1420134-AB	SUPPORT, DIGITAL CARD (TOP)			1	-
8	1420135-01	PANEL, BOTTOM			1	1
9	1420138-01	BRACKET, FILTER			2	2
10	1420160-01	COVER, TOP			1	-
11	1420173-01	SHIELD, FRONT FAN BRACKET			1	1
12	1465154-01	COVER, TOP			-	1
13	1420247-01	GRILL, BLOWER, MODIFIED			1	1
14	1465153-01	BRACKET, LOWER, FAN PANEL			-	2
15	1420377-AA	BRACKET, LOWER FAN PANEL (LEFT)			1	-
16	1420377-AB	BRACKET, LOWER FAN PANNEL (RIGHT)			1	-
17	1420378-01	BRACKET, AIR FLOW			1	1
18						
19	1420415-01	STRIP, AIR FLOW			1	-
20	1420429-01	LABEL, CARRYING HANDLE			2	2
21	1420465-AB	DOOR ASSEMBLY, DIGITAL			1	1
22	1420466-AB	DOOR ASSEMBLY, ANALOG			1	1
23	1464353-01	LABEL, SOFTWARE & OPTION			-	1
24	1464693-02	PWA, 2-4 CHANNEL CONCENTRATOR MOTHERBOARD			1	1
25	1464803-01	TRAY, UPPER COMPARTMENT			1	1
26						
27	6000055-02	LABEL, CLASS 'A' COMPLIANCE			1	1
28						
29						
30	089-134	HANDLE, PANEL, U-SHAPED, FOLDING			2	2
31						
32	283-347	SPACER, THREADED, PLAIN, 8-32, .500AF HEX, .250 LG, NYLON			4	4
33						
34	302-123	CLAMP, LOOP, OFFSET, .750 ID			2	2
35	302-160	CLAMP, LOOP, OFFSET, .250 ID			2	2
36	302-591	CLAMP, FLAT CABLE, NYLON			4	4
37						

ILM-1464552

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1464552 SHEET 2 OF 2	REV B

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01	-02
38	470-018	SCREW, CAP, SOC HD, HEX SOC DR, 6-32 X .375 LG		5	5
39	470-020	SCREW, CAP, SOC HD, HEX SOC DR, 6-32 X .500 LG		5	5
40	470-028	SCREW, CAP, SOC HD, HEX SOC DR, 8-32 X .438 LG		6	6
41	470-658	SCREW, CAP, BUT HD, HEX SOC DR, 8-32 X .312 LG, SST		6	6
42					
43	471-061	SCREW, MACH, PAD HD, XREC DR, 4-40 X .312 LG		8	8
44	471-071	SCREW, MACH, PAN HD, XREC DR, 6-32 X .500 LG		2	-
45					
46	473-324	SCREW, MACH, PAN HD, XREC DR, 4-40 X .250 LG, ASSEM WSR		4	4
47	473-330	SCREW, MACH, PAN HD, XREC DR, 6-32 X .250 LG, ASSEM WSR		4	-
48	473-331	SCREW, MACH, PAN HD, XREC DR, 6-32 X .500 LG ASSEM WSR		7	7
49	473-928	SCREW, MACH, PAN HD, XREC DR, 10-32 X .375 LG, ASSEM WSR		8	8
50					
51	475-044	SCREW, MACH, PAN HD, XREC DR, 8-32 X .375 LG, ASSEM WSR		52	50
52	475-058	SCREW, MACH, PAN HD, XREC DR, 6-32 X .375 LG, ASSEM WSR		15	15
53	475-124	SCREW, MACH, PAN HD, XREC DR, 10-32 X .500 LG, ASSEM WSR		4	4
54					
55	493-005	NUT, HEX, FINISHED, 4-40, NYLON LOCK		9	9
56	493-006	NUT, HEX, FINISHED, 6-32, NYLON LOCK		1	1
57					
58	496-005	NUT, HEX, CAPTIVE LOCK WASHER, 6-32		17	19
59	496-006	NUT, HEX, CAPTIVE LOCK WASHER, 8-32		12	12
60	496-007	NUT, HEX, CAPTIVE LOCK WASHER, 10-32		4	4
61					
62					
63	501-008	WASHER, PLAIN, .125 ID, .312 OD, .032 THK		-	2
64	501-009	WASHER, PLAIN #6, .156 ID, .375 OD, .049 THK		23	25
65	501-019	WASHER, PLAIN, #10, .203 ID, .438 OD, .032 THK		8	8
66	501-188	WASHER, PLAIN, #6, SMALL PATTERN		5	10
67	501-205	WASHER, PLAIN, #8, .188 ID, .438 OD, .047 THK		46	36
68					
69	502-003	WASHER, LOCK, HELICAL SPRING, #6		5	10
70	502-004	WASHER, LOCK, HELICAL SPRING, #8		6	6
71	502-400	WASHER, PLAIN, #8, SMALL PATTERN		6	14
72	502-444	WASHER, PLAIN, #6, .150 ID, .31 OD, .020 THK, NATURAL NYLON		4	-
73					
74	506-013	WASHER, 'D' #6		2	2
75	506-016	WASHER, 'D' #8		2	2
76					
77	530-324	ENCLOSURE PART, GUIDE, PC BOARD, (FOR .065 THK BOARD)		162	162
78					
79	1420133-AD	PANEL, SIDE (RIGHT)		-	1
80	1420133-AE	PANEL, SIDE (LEFT)		-	1
81	1420134-AC	SUPPORT, DIGITAL CARD (BOTTOM)		-	1
82	1420134-AD	SUPPORT, DIGITAL CARD (TOP)		-	1

LM-1464552

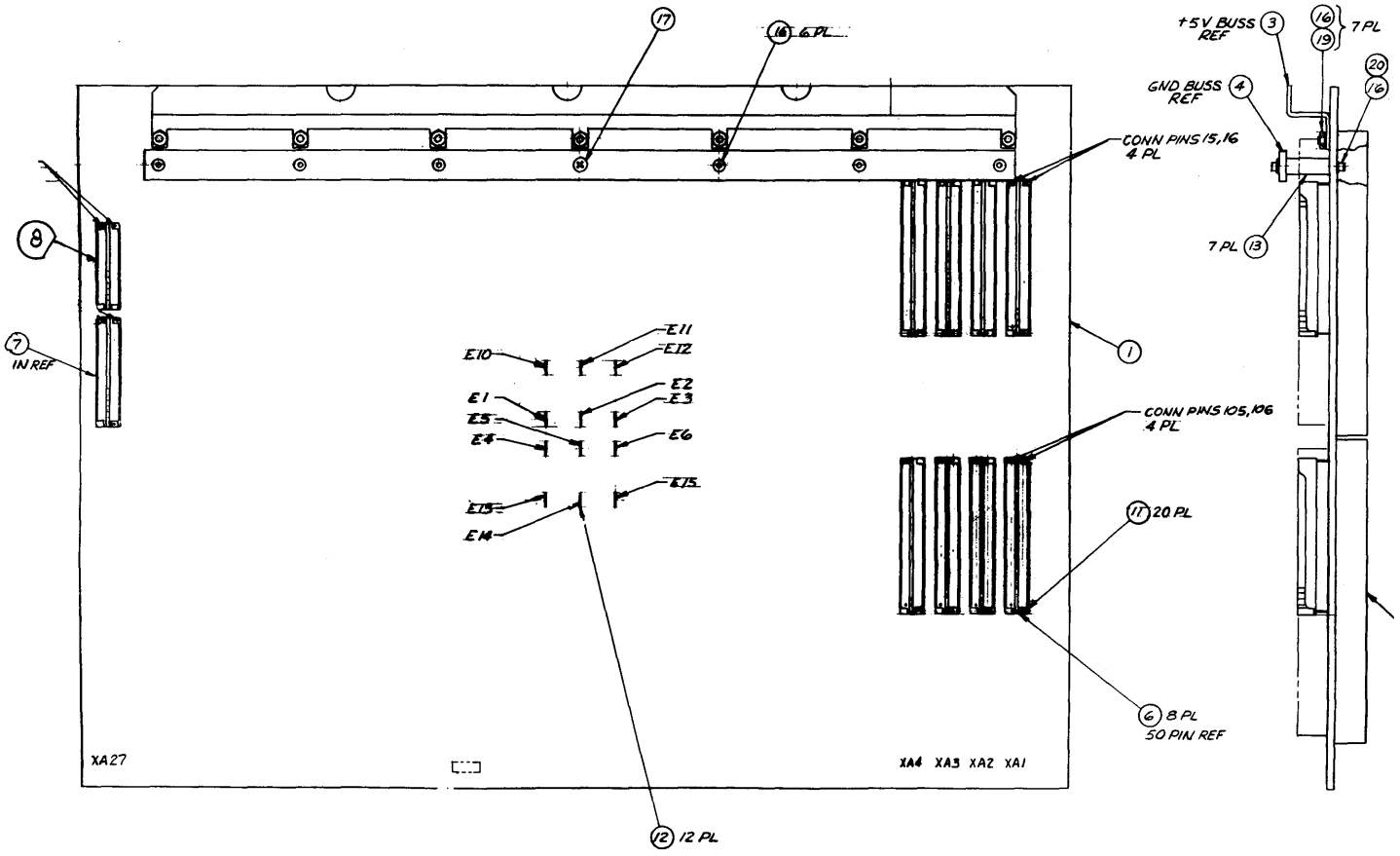
ITEM NO.	PART NUMBER		DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01	-02
1.					-02	
2.						
3.	1420163-02	BAR, BUS , +5V			1	1
4.	1420164-02	BAR, POWER BUS GROUND			1	1
5.						
6.	135-167	HEADER ASSY PART, KEYING, 50 PIN		XA1-4	8	8
7.	135-528	HEADER ASSY PART, KEYING, 34 PIN		XA27	1	1
8.	135-527	HEADER ASSY PART, KEYING, 26 PIN		XA27	1	1
9.						
10.	140-730	CONN, SIGNAL CIRCUIT, RECPT, P.C., .100 SPG		XA1-11,27	24	24
11.	177-165	CONN PART, CLIP		XA1-4,27	20	20
12.	187-397	TERMINAL, MALE QUICK DISCONNECT, LUG		E1-6, 10-15	12	12
13.	283-362	SPACER, THD., 4-40 X 1.25 LG, .250 AF HEX			7	7
14.						
15.						
16.	470-010	SCREW, CAP, SOC. HD., 4-40 X .375 LG			20	20
17.	471-328	SCREW, FLAT HD., XREC, 4-40 X .375 LG			1	1
18.						
19.	496-004	NUT, HEX, CAPTIVE WASHER, 4-40			7	7
20.	502-002	WASHER, LOCK SPRING, #4			7	7
21.						
22.	1	WIRE, SOLID, WIRE WRAP, 30 AWG			AR	AR

NOTES:

1 NOT REQUIRED, SELECTED BY COMPANY TO DO WIREWRAP.

2 AFTER WIREWRAP CUT PINS 60-66 & 150-156 ON CONNECTORS XA1-XA4.

LM-1464693



E REF DESIG
GND, E10-E15
-5V, E1-E6

Assembly No. 1464693-01E. Concentrator Motherboard PWA

AMPEX	Ampex Corporation Redwood City, California	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 2 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
1.	30		XA1	13		XA11	125	10A-CLK-H-TW+ } TWISTED PAIR	22
2.				14			128	H-TW- }	
3.				15			126	X3-TW+ } TWISTED PAIR	
4.				16		XA11	123	CLK-X3-TW- }	
5.				60		XA9	19	KEY1-KEYD4	
6.				61			22	KEYD1	
7.				62			24	KEYD5	
8.				63			20	KEYD2	
9.				64			21	KEYD0	
10.				65			25	KEYD7	
11.				66			23	KEYD3	
12.				68		XA9	18	KEY1-KEYD6	
13.				69		XA5	75	CUT1-MUXD5	
14.				70			76	MUXD4	
15.				71			82	MUXD1	
16.				72			81	MUXD0	
17.				73			80	MUXD3	
18.				74			79	MUXD2	
19.				75			73	MUXD7	
20.				76		XA5	74	10A-CUT1-MUXD6	
21.			XA1	78		XA2	78	KEY2-10-KEYD4	
22.			XA2	78		XA3	78		
23.			XA3	78		XA4	78		
24.			XA4	78		XA10	146	KEYD4	
25.			XA1	79		XA2	79	KEYD0	
26.			XA2	79		XA3	79		
27.			XA3	79		XA4	79		
28.			XA4	79		XA10	151	KEYD0	
29.			XA1	80		XA2	80	KEYD5	
30.			XA2	80		XA3	80		
31.			XA3	80		XA4	80		
32.			XA4	80		XA10	145	KEYD5	
33.			XA1	81		XA2	81	KEYD2	
34.			XA2	81		XA3	81		
35.			XA3	81		XA4	81		
36			XA4	81		XA10	149	KEYD2	
37.			XA1	82		XA2	82	KEYD1	
38.			XA2	82		XA3	82		
39.			XA3	82		XA4	82		
40.			XA4	82		XA10	150	KEYD1	
41.			XA1	83		XA2	83	KEYD6	
42.			XA2	83		XA3	83		
43.			XA3	83		XA4	83		
44.	30		XA4	83		XA10	144	KEY2-10-KEYD6	22
45.									

1464693

AMPEX	Ampex Corporation Redwood City California	CODE IDENT NO 92739	WIRE LEAD LIST	LM-1464693 SHEET 3 OF 18	REV. E

WIRE NO	GAUGE/ COND	FROM STA	FROM REF DES	FROM TERM	TO STA	TO REF DES	TO TERM	REMARKS	LM ITEM NUMBER -02
46.	30		XA1	84		XA2	84	KEY2-10-KEYD3	22
47.			XA2	84		XA3	84		
48.			XA3	84		XA4	84		
49.			XA4	84		XA10	148	KEY2-10-KEYD3	
50.			XA1	85		XA2	85	KEY1-10-KEYD4	
51.			XA2	85		XA3	85		
52.			XA3	85		XA4	85		
53.			XA4	85		XA9	146	KEY1-10-KEYD4	
54.			XA1	86		XA2	86	KEY2-10-KEYD7	
55.			XA2	86		XA3	86		
56.			XA3	86		XA4	86		
57.			XA4	86		XA10	143	KEY2-10-KEYD7	
58.			XA1	88		XA2	88	KEY1-10-KEYD5	
59.			XA2	88		XA3	88		
60.			XA3	88		XA4	88		
61.			XA4	88		XA9	145	KEYD5	
62.			XA1	89		XA2	89	KEYD1	
63.			XA2	89		XA3	89		
64			XA3	89		XA4	89		
65.			XA4	89		XA9	150	KEYD1	
66.			XA1	90		XA2	90	KEYD0	
67.			XA2	90		XA3	90		
68.			XA3	90		XA4	90		
69.			XA4	90		XA9	151	KEYD0	
70.			XA1	91		XA2	91	KEYD3	
71.			XA2	91		XA3	91		
72.			XA3	91		XA4	91		
73.			XA4	91		XA9	148	KEYD3	
74.			XA1	92		XA2	92	KEYD2	
75.			XA2	92		XA3	92		
76.			XA3	92		XA4	92		
77.			XA4	92		XA9	149	KEYD2	
78.			XA1	93		XA2	93	KEYD7	
79.			XA2	93		XA3	93		
80.			XA3	93		XA4	93		
81.			XA4	93		XA9	143	KEYD7	
82.			XA1	94		XA2	94	KEYD6	
83.			XA2	94		XA3	94		
84.			XA3	94		XA4	94		
85.			XA4	94		XA9	144	KEY1-10-KEYD6	
86.			XA1	150		XA11	168	10A-CLK-FRAME	
87.				151			130	CLK-10A-H-TW- } TWISTED PAIR	
88.				152			129	H-TW+	
89.				153			131	X3-TW- } TWISTED PAIR	
90.	30		XA1	154		XA11	132	CLK-10A-X3-TW+	22

AMPEX	Ampex Corporation Redwood City, California	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 4 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
91.	30		XA1	155		XA8	128	ADD-10A-MUXD7	22
92.									
93.				156			120	10A-MUXD2	
94.									
95.				158			124	10A-MUXD5	
96.									
97.				159			122	10A-MUXD4	
98.									
99.				160			121	10A-MUXD1	
100.									
101.				161			123	10A-MUXD3	
102.									
103.				162			119	10A-MUXD0	
104.									
105.			XA1	164		XA8	126	ADD-10A-MUXD6	
106.									
107.			XA1	169		XA2	169	CD14	
108.			XA2	169		XA3	169		
109.			XA3	169		XA4	169		
110.			XA4	169		XA5	171		
111.			XA5	171		XA6			
112.			XA6			XA7			
113.			XA7			XA8			
114.			XA8			XA9			
115.			XA9			XA10			
116.			XA10			XA11			
117.			XA11	171		XA27	171	CD14	
118.			XA1	170		XA2	170	CD15	
119.			XA2			XA3			
120.			XA3			XA4			
121.			XA4			XA5			
122.			XA5			XA6			
123.			XA6			XA7			
124.			XA7			XA8			
125.			XA8			XA9			
126.			XA9			X10			
127.			XA10			XA11			
128.			XA11	170		XA27	170	CD15	
129.			XA1	171		XA2	171	CD12	
130.			XA2			XA3	171		
131.			XA3			XA4	171		
132.			XA4	171		XA5	173		
133.			XA5	173		XA6			
134.			XA6	173		XA7			
135.	30		XA7	173		XA8	173	CD12	22

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AMPEX	Ampex Corporation Redwood City California	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 5 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
136.	30		XA8	173		XA9	173	CD12	22
137.			XA9			XA10			
138.			XA10			XA11			
139.			XA11	173		XA27	173	CD12	
140.			XA1	172		XA2	172	CD13	
141.			XA2			XA3			
142.			XA3			XA4			
143.			XA4			XA5			
144.			XA5			XA6			
145.			XA6			XA7			
146.			XA7			XA8			
147.			XA8			XA9			
148.			XA9			XA10			
149.			XA10			XA11			
150.			XA11	172		XA27	172	CD13	
151.			XA1	173		XA2	173	CD10	
152.			XA2			XA3			
153.			XA3			XA4	173		
154.			XA4	173		XA5	175		
155.			XA5	175		XA6			
156.			XA6			XA7			
157.			XA7			XA8			
158.			XA8			XA9			
159.			XA9			XA10			
160.			XA10			XA11			
161.			XA11	175		XA27	175	CD10	
162.			XA1	174		XA2	174	CD11	
163.			XA2			XA3			
164.			XA3			XA4			
165.			XA4			XA5			
166.			XA5			XA6			
167.			XA6			XA7			
168.			XA7			XA8			
169.			XA8			XA9			
170.			XA9			XA10			
171.			XA10			XA11			
172.			XA11	174		XA27	174	CD11	
173.			XA1	175		XA2	175	CD8	
174.			XA2			XA3			
175.			XA3			XA4	175		
176.			XA4	175		XA5	178		
177.			XA5	178		XA6			
178.			XA6			XA7			
179.			XA7			XA8			
180.	30		XA8	178		XA9	178	CD8	22

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AMPEX	Ampex Corporation Redwood City, California	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 6 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
181.	30		XA9	178		XA10	178	CD8	22
182			XA10			XA11			
183			XA11	178		XA27	178	CD8	
184.			XA1	176		XA2	176	CD9	
185			XA2			XA3			
186.			XA3			XA4			
187.			XA4			XA5			
188.			XA5			XA6			
189.			XA6			XA7			
190.			XA7			XA8			
191.			XA8			XA9			
192.			XA9			XA10			
193.			XA10			XA11			
194.			XA11	176		XA27	176	CD19	
195.			XA1	178		XA2	178	CD7	
196.			XA2			XA3			
197.			XA3			XA4	178		
198.			XA4	178		XA5	189		
199.			XA5	189		XA6			
200.			XA6			XA7			
201.			XA7			XA8			
202.			XA8			XA9			
203.			XA9			XA10			
204.			XA10			XA11			
205.			XA11	189		XA27	189	CD7	
206.			XA1	179		XA2	179	CD5	
207.			XA2			XA3			
208.			XA3			XA4	179		
209.			XA4	179		XA5	191		
210.			XA5	191		XA6			
211.			XA6			XA7			
212.			XA7			XA8			
213.			XA8			XA9			
214.			XA9			XA10			
215.			XA10			XA11			
216.			XA11	191		XA27	191	CD5	
217.			XA1	180		XA2	180	CD6	
218.			XA2			XA3			
219.			XA3			XA4	180		
220.			XA4	180		XA5	190		
221.			XA5	190		XA6			
222.			XA6			XA7			
223.			XA7			XA8			
224.			XA8			XA9			
225.	30		XA9	190		XA10	190	CD6	22

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AMPEX	Ampex Corporation Redwood City, California	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 7 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
226.	30		XA10	190		XA11	190	CD6	22
227.			XA11	190		XA27	190	CD6	
228.			XA1	181		XA2	181	CD3	
229.			XA2			XA3			
230.			XA3			XA4	181		
231.			XA4	181		XA5	193		
232.			XA5	193		XA6			
233.			XA6			XA7			
234.			XA7			XA8			
235.			XA8			XA9			
236.			XA9			XA10			
237.			XA10			XA11			
238.			XA11	193		XA27	193	CD3	
239.			XA1	182		XA2	182	CD4	
240.			XA2			XA3			
241.			XA3			XA4	182		
242.			XA4	182		XA5	192		
243.			XA5	192		XA6			
244.			XA6			XA7			
245.			XA7			XA8			
246.			XA8			XA9			
247.			XA9			XA10			
248.			XA10			XA11			
249.			XA11	192		XA27	192	CD4	
250.			XA1	183		XA2	183	CD1	
251.			XA2			XA3			
252.			XA3			XA4	183		
253.			XA4	183		XA5	195		
254.			XA5	195		XA6			
255.			XA6			XA7			
256.			XA7			XA8			
257.			XA8			XA9			
258.			XA9			XA10			
259.			XA10			XA11			
260.			XA11	195		XA27	195	CD1	
261.			XA1	184		XA2	184	CD2	
262.			XA2			XA3			
263.			XA3			XA4	184		
264.			XA4	184		XA5	194		
265.			XA5	194		XA6			
266.			XA6			XA7			
267.			XA7			XA8			
268.			XA8			XA9			
269.			XA9			XA10			
270.	30		XA10	194		XA11	194	CD2	22

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AMPEX	Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 8 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBEP -02
271.	30		XA11	194		XA27	194	CD2	22
272.			XA1	185		XA2	185	A7	
273.			XA2			XA3	185		
274.			XA3			XA4	185		
275.			XA4	185		XA11	179		
276.			XA11	179		XA27	179	A7	
277.			XA1	186		XA2	186	CD0	
278.			XA2			XA3			
279.			XA3			XA4	186		
280.			XA4	186		XA5	196		
281.			XA5			XA6			
282.			XA6			XA7			
283.			XA7			XA8			
284.			XA8			XA9			
285.			XA9			XA10			
286.			XA10			XA11			
287.			XA11	196		XA27	196	CD0	
288.			XA1	188		XA2	188	A6	
289.			XA2			XA3			
290.			XA3			XA4	188		
291.			XA4	188		XA11	180		
292.			XA11	180		XA27	180	A6	
293.			XA1	189		XA2	189	A4	
294			XA2			XA3			
295.			XA3			XA4	189		
296.			XA4	189		XA11	182		
297.			XA11	182		XA27	182	A4	
298.			XA1	190		XA2	190	A5	
299.			XA2			XA3			
300.			XA3			XA4	190		
301.			XA4	190		XA11	181		
302.			XA11	181		XA27	181	A5	
303.			XA1	191		XA2	191	A2	
304.			XA2			XA3			
305.			XA3			XA4	191		
306			XA4	191		XA5	136		
307.			XA8	184		XA9	184		
308.			XA9			XA10			
309.			XA10			XA11			
310.			XA11	184		XA27	184	A2	
311.			XA1	192		XA2	192	A3	
312.			XA2			XA3			
313.			XA3			XA4	192		
314.			XA4	192		XA8	183		
315.	30		XA8	183		XA9	183	A3	22

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AMPEX	Ampex Corporation Redwood City, California	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 9 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
316.	30		XA9	183		XA10	183	A3	22
317.			XA10	183		XA11	183		
318.			XA11	183		XA27	183	A3	
319.			XA1	193		XA2	193	RW	
320.			XA2			XA3			
321			XA3			XA4	193		
322.			XA4	193		XA5	166		
323.			XA5	166		XA6			
324.			XA6			XA7	166		
325.			XA7	166		XA8	186		
326.			XA8	186		XA9			
327.			XA9			XA10			
328.			XA10			XA11			
329.			XA11	186		XA27	186	RW	
330.			XA1	194		XA2	194	A1	
331.			XA2			XA3			
332.			XA3			XA4	194		
333.			XA4	194		XA5	185		
334.			XA5	185		XA6			
335.			XA6			XA7			
336.			XA7			XA8			
337.			XA8			XA9			
338.			XA9			XA10			
339.			XA10			XA11			
340.			XA11	185		XA27	185	A1	
341.			XA1	195		XA27	122	IOA-COMP-INT	
342.			XA1	196		XA27	129	BS1	
343.			XA2	13		XA11	122	IOB-CLK-H-TW+ } TWISTED PAIR	
344.				14			120	CLK-H-TW-	
345.				15			121	CLK-X3-TW+ } TWISTED PAIR	
346.				16		XA11	124	CLK-X3-TW-	
347.				60		XA9	116	KEY1-KEYD4	
348.				61			120	KEYD1	
349.				62			115	KEYD5	
350.				63			119	KEYD2	
351.				64			121	KEYD0	
352.				65			113	KEYD7	
353.				66			118	KEYD3	
354.				68		XA9	114	KEY1-KEYD6	
355.				69		XA5	149	CUT1-MUXD5	
356.				70			150	MUXD4	
357.				71			153	MUXD1	
358.				72			154	MUXD0	
359.				73			154	MUXD3	
360.	30		XA2	74		XA5	152	IOB-CUT1-MUXD2	22

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AMPEX	Ampex Corporation Redwood City, California	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 10 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
361.	30		XA2	75		XA5	145	10B-CUT1-MUXD7	22
362.				76		XA5	146	10B-CUT1-MUXD6	
363.				150		XA11	165	10B-CLK-FRAME	
364.				151			134	CLK-10B-H-TW- } TWISTED PAIR	
365.				152			133	H-TW+ }	
366.				153			135	X3-TW- } TWISTED PAIR	
367.				154		XA11	136	CLK-10B-X3-TW+ }	
368.				155		XA8	138	ADD-10B-MUXD7	
369.									
370.				156			132	MUXD2	
371.									
372.				158			135	MUXD5	
373.									
374.				159			134	MUXD4	
375.									
376.				160			131	MUXD1	
377.									
378.				161			133	MUXD3	
379.									
380.				162			130	MUXD0	
381.									
382.				164		XA8	136	ADD-10B-MUXD6	
383.									
384.				195		XA27	121	10B-COMP-INT	
385.			XA2	196		XA27	130	BS2	
386.			XA3	13		XA11	115	10C-CLK-H-TW+ } TWISTED PAIR	
387.				14			116	H-TW- }	
388.				15			118	X3-TW+ } TWISTED PAIR	
389.				16		XA11	119	10C-CLK-X3-TW- }	
390.									
391.									
392.									
393.									
394.				60		XA10	19	10C-KEY2-KEYD4	
395.				61			22	KEYD1	
396.				62			24	KEYD5	
397.				63			20	KEYD2	
398.				64			21	KEYD0	
399.				65			25	KEYD7	
400.				66			23	KEYD3	
401.				68		XA10	18	10C-KEY2-KEYD6	
402.				69		XA7	75	10C-CUT3-MUXD5	
403.				70			76	MUXD4	
404.				71.			82	MUXD1	
405.	30		XA3	72		XA7	81	10C-CUT3-MUXD0	22

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AMPEX | Ampex Corporation Redwood City, California	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 11 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
406.	30		XA3	73		XA7	80	IOC-CUT3-MUXD3	22
407.				74			79	MUXD2	
408.				75.			73	MUXD7	
409.				76		XA7	74	IOC-CUT3-MUXD6	
410.				150		XA11	166	IOC-CLK-FRAME	
411.				151			138	CLK-IOC-H-TW- } TWISTED PAIR	
412.				152.			140	H-TW+	
413.				153.			142	X3-TW- } TWISTED PAIR	
414.				154		XA11	139	CLK-IOC-X3-TW+	
415.				155		XA8	146	ADD-IOC-MUXD7	
416.				156			141	MUXD2	
417.				158			144	MUXD5	
418.				159			143	MUXD4	
419.				160			140	MUXD1	
420.				161			142	MUXD3	
421.				162			139	MUXD0	
422.				164		XA8	145	ADD-IOC-MUXD6	
423.				195		XA27	124	IOC-COMP-INT	
424.			XA3	196		XA27	131	BS3	
425.			XA4	13		XA11	113	IOD-CLK-H-TW+ } TWISTED PAIR	
426.				14			114	H-TW-	
427.				15			112	X3-TW+ } TWISTED PAIR	
428.				16		XA11	111	IOD-CLK-X3-TW-	
429.				60		XA10	116	KEY2-KEYD4	
430.				61			120	KEYD1	
431.				62			115	KEYD5	
432.				63			119	KEYD2	
433.				64			121	KEYD0	
434.				65			113	KEYD7	
435.				66			118	KEYD3	
436.				68		XA10	114	KEY2-KEYD6	
437.				69		XA7	149	CUT3-MUXD5	
438.				70			150	MUXD4	
439.				71			153	MUXD1	
440.				72			154	MUXD0	
441.				73			151	MUXD3	
442.				74			152	MUXD2	
443				75			145	MUXD7	
444.				76		XA7	146	CUT3-MUXD6	
445.				150		XA11	163	IOD-CLK-FRAME	
446.				151			141	CLK-IOD-H-TW- } TWISTED PAIR	
447.				152			144	H-TW+	
448.				153			146	X3-TW- } TWISTED PAIR	
449.	30		XA4	154		XA11	143	CLK-IOD X3-TW+	22
450.									

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AMPEX	Ampex Corporation Redwood City, California	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 12 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
451.	30		XA4	155		XA8	155	ADD-IOD-MUXD7	22
452.				156			150	MUXD2	
453.				158			153	MUXD5	
454.				159			152	MUXD4	
455.				160			149	MUXD1	
456.				161			151	MUXD3	
457.				162			148	MUXD0	
458.				164		XA8	154	ADD-IOD-MUXD6	
459.				195		XA27	123	IOD-COMP-INT	
460.			XA4	196		XA27	132	BS4	
461.			XA5	11		XA11	89	CLK-CUT1-IX3-TW+ } TWISTED PAIR	
462.				12			90	IX3-TW- }	
463.				13			70	IH-TW+ } TWISTED PAIR	
464.				14			69	IH-TW- }	
465.				26		XA11	158	CLK-CUT1-IKEYSW	
466.				29		XA9	31	KEY1-CUT1-IKEYD0	
467.				30			32	IKEYD1	
468.				31			33	IKEYD2	
469.				32			34	IKEYD3	
470.				39			26	IKEYD4	
471.				40			23	IKEYD5	
472.				41			29	IKEYD6	
473.				42		XA9	30	KEY1-CUT1-IKEYD7	
474.				44		XA9	122	PRE TALLY A	
475.				89		XA8	35	CUT1-ADD-IMUXD0	
476.				90			36	IMUXD1	
477.				91			38	IMUXD2	
478.				92			39	IMUXD3	
479.				93			40	IMUXD4	
480.				94			41	IMUXD5	
481.				95			42	IMUXD6	
482.				96		XA3	43	CUTA-ADD-IMUXD7	
483.				109		XA11	110	CLK-CUT1-IIX3-TW+ } TWISTED PAIR	
484.				110			109	IIX3-TW- }	
485.				111			79	IIH-TW+ } TWISTED PAIR	
486.				112			80	IIH-TW- }	
487.				116		XA11	160	CLK-CUT1-IIKEYSW	
488.				119		XA9	89	KEY1-CUT1-IIKEYD0	
489.				120			90	IIKEYD1	
490.				121			91	IIKEYD2	
491.				122			92	IIKEYD3	
492.				129			93	IIKEYD4	
493.				130			94	IIKEYD5	
494.				131			95	IIKEYD6	
495.	30		XA5	132		XA9	96	KEY1-CUT1-MUXD7	22

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AMPEX	Ampex Corporation Redwood City California	CODE IDENT NO. 92739	WIRE ROUTING LIST	1464693 SHEET 13 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
496.	30		XA5	134		XA9	152	PRE TALLY B	22
497.				136		XA6	136	A2	
498.				155		XA8	44	CUT1-ADD-I1MUXD0	
499.				156			45	I1MUXD1	
500.				159			46	I1MUXD2	
501.				160			48	I1MUXD3	
502.				161			49	I1MUXD4	
503.				162			50	I1MUXD5	
504.				163			51	I1MUXD6	
505.				164		XA8	52	CUT1-ADD-I1MUXD7	
506.			XA5	168		XA27	133	BS5	
507.			XA6	11		XA11	95	CLK-CUT2-IX3-TW+ } TWISTED PAIR	
508.				12			96	IX3-TW-	
509.				13			82	IH-TW+ } TWISTED PAIR	
510.				14			83	IH-TW-	
511.				26		XA11	161	CLK-CUT2-IKEYSW	
512.				29		XA9	131	KEY1-CUT2-IKEYD0	
513.				30			130	IKEYD1	
514.				31			129	IKEYD2	
515.				32			128	IKEYD3	
516.				39			126	IKEYD4	
517.				40.			125	IKEYD5	
518.				41			124	IKEYD6	
519.				42			123	IKEYD7	
520.				73			142	IMUXD7	
521.				74			141	IMUXD6	
522.				75			139	IMUXD5	
523.				76			140	IMUXD4	
524.				79			135	IMUXD2	
525.				80			136	IMUXD3	
526.				81			133	IMUXD0	
527.				82		XA9	134	KEY1-CUT2-IMUXD1	
528.				89		XA8	71	CUT2-ADD-IMUXD0	
529.				90			72	IMUXD1	
530.				91			73	IMUXD2	
531.				92			74	IMUXD3	
532.				93			75	IMUXD4	
533.				94			76	IMUXD5	
534.				95			78	IMUXD6	
535.				96		XA8	79	CUT2-ADD-IMUXD7	
536.				109		XA11	58	CLK-CUT2-I1X3-TW+ } TWISTED PAIR	
537.				110			60	I1X3-TW-	
538.				111			46	I1H-TW+ } TWISTED PAIR	
539.				112			48	I1H-TW-	
540.	30		XA6	116		XA11	164	CLK-CUT2-I1KEYSW	22

1464693

AMPEX	Ampex Corporation Redwood City, California	CODE IDENT NO 92739	WIRE ROUTING LIST	1464693 SHEET 14 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
541.	30		XA6	119		XA10	131	CLK-CUT2-11KEYD0	22
542.				120			130	KEY2 CUT2-11KEYD1	
543.				121			129	KEY2-CUT2-11KEYD2	
544.				122			128	11KEYD3	
545.				129			126	11KEYD4	
546.				130			125	11KEYD5	
547.				131			124	11KEYD6	
548.				132		XA10	123	KEY2-CUT2-11KEYD7	
549.				136		XA7	136	A2	
550.				145		XA10	142	KEY2-CUT2-11MUXD7	
551.				146			141	11MUXD6	
552.				149			139	11MUXD5	
553.				150			140	11MUXD4	
554.				151			136	11MUXD3	
555.				152			135	11MUXD2	
556.				153			134	11MUXD1	
557.				154		XA10	133	KEY2-CUT2-11MUXD0	
558.				155		XA8	80	CUT2-ADD-11MUXD0	
559.				156			81	11MUXD1	
560.				159			82	11MUXD2	
561.				160			83	11MUXD3	
562.				161.			84	11MUXD4	
563.				162			85	11MUXD5	
564.				163			86	11MUXD6	
565.				164		XA8	88	CUT2-ADD-11MUXD7	
566.			XA6	168		XA27	134	BS6	
567.			XA7	11		XA11	59	CLK-CUT3-1X3-TW+ } TWISTED PAIR	
568.				12			62	1X3-TW- }	
569.				13			32	1H-TW+ } TWISTED PAIR	
570.				14			31	1H-TW- }	
571.				26		XA11	155	CLK-CUT3-1KEYSW	
572.				29		XA10	31	KEY2-CUT3-1KEYD0	
573.				30			32	1KEYD1	
574.				31			33	1KEYD2	
575.				32			34	1KEYD3	
576.				39			26	1KEYD4	
577.				40			28	1KEYD5	
578.				41			29	1KEYD6	
579.				42		XA10	30	KEY2-CUT3-1KEYD7	
580.				44		XA10	122	PRE TALLY C	
581.				89		XA8	53	CUT3-ADD-1MUXD0	
582.				90			54	1MUXD1	
583.				91			55	1MUXD2	
584.				92			56	1MUXD3	
585.	30		XA7	93		XA8	58	CUT3-ADD-1MUXD4	22

1464693

AMPEX	Ampex Corporation Redwood City California	CODE IDENT NO 92739	WIRE ROUTING LIST	1464693 SHEET 15 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
586.	30		XA7	94		XA8	59	CUT3-ADD-1MUXD5	22
587.				95			60	1MUXD6	
588.				96		XA8	61	CUT3-ADD-1MUXD7	
589.									
590.				109		XA11	63	CLK-CUT3-11X3-TW+ } TWISTED PAIR	
591.				110			64	11X3-TW- }	
592.				111			45	11H-TW+ } TWISTED PAIR	
593.				112			42	11H-TW- }	
594.				116		XA11	156	CLK-CUT3-11KEYSW	
595.				119		XA10	89	KEY2-CUT3-11KEYD0	
596.				120			90	11KEYD1	
597.				121			91	11KEYD2	
598.				122			92	11KEYD3	
599.				129			93	11KEYD4	
600.				130			94	11KEYD5	
601.				131			95	KEY2-CUT3-11KEYD6	
602.				132			96	KEY2-CUT3-11KEYD7	
603.				134		XA10	152	PRE TALLY D	
604.				136		XA8	184	A2	
605.				155		XA8	62	CUT3-ADD-11MUXD0	
606.				156			63	11MUXD1	
607.				159			64	11MUXD2	
608.				160			65	11MUXD3	
609.				161			66	11MUXD4	
610.				162			68	11MUXD5	
611.				163			69	11MUXD6	
612.				164		XA8	70	CUT3-ADD-11MUXD7	
613.				168		XA27	135	BS7	
614.				170		XA8	174	CD15	
615.				171			176	CD14	
616.				172			175	CD13	
617.				173			178	CD12	
618.				174			179	CD11	
619.				175			181	CD10	
620.				176			180	CD9	
621.			XA7	178		XA8	182	CD8	
622.			XA8	9		XA11	25	CLK-ADD-1X1.5-TW- } TWISTED PAIR	
623.				10			26	1X1.5-TW+ }	
624.				11			9	1X3-TW- }	
625.				12			10	1X3-TW+ }	
626.				13			29	11X1.5-TW+ }	
627.				14			30	11X1.5-TW- }	
628.				15			22	11X3-TW- } TWISTED PAIR	
629.				16		XA11	23	CLK-ADD-11X3-TW+ }	
630.	30		XA8	174		XA9	170	CD15	22

1464693

AMPEX	Ampex Corporation Redwood City, California	CODE IDENT NO. 92739	WIRE LEAD LIST	LM-1464693 SHEET 16 OF 18	REV. E

WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
631.	30		XA8	175		XA9	172	CD13	22
632.				176			171	CD14	
633				178			173	CD12	
634.				179			174	CD11	
635.				180			176	CD9	
636.				181			175	CD10	
637.				182		XA9	178	CD8	
638.			XA8	188		XA27	136	BS8	
639.			XA9	9		XA11	94	CLK-KEY1-IX.5-TW+ } TWISTED PAIR	
640.				10			93	CLK-KEY1-IX.5-TW- }	
641.				11			74	IX1-TW-	
642.				12			73	IX1-TW+	
643.				13			86	IX3-TW+ } TWISTED PAIR	
644.				14		XA11	88	CLK-KEY1-IX3-TW- }	
645.				35		XA10	71	KEY EXP-DA0	
646.				36			72	DA1	
647.				38			73	DA2	
648.				39			74	DA3	
649.				40			75	DA4	
650.				41			76	DA5	
651.				42			78	DA6	
652.				43			79	DA7	
653.				44			80	DB0	
654.				45			81	DB1	
655.				46			82	DB2	
656				48			83	DB3	
657.				49			84	DB4	
658.				50			85	DB5	
659.				51			86	DB6	
660.				52			88	DB7	
661.				53			35	DC0	
662.				54			36	DC1	
663.				55			38	DC2	
664.				56			39	DC3	
665.				58			40	DC4	
666.				59			41	DC5	
667.				60			42	DC6	
668.				61			43	DC7	
669.				62			44	DD0	
670.				63			45	DD1	
671.				64			46	DD2	
672.				65			48	DD3	
673.				66			49	DD4	
674.				68			50	DD5	
675.	30		XA9	69		XA10	51	KEY-EXP-DD6	22

1464693

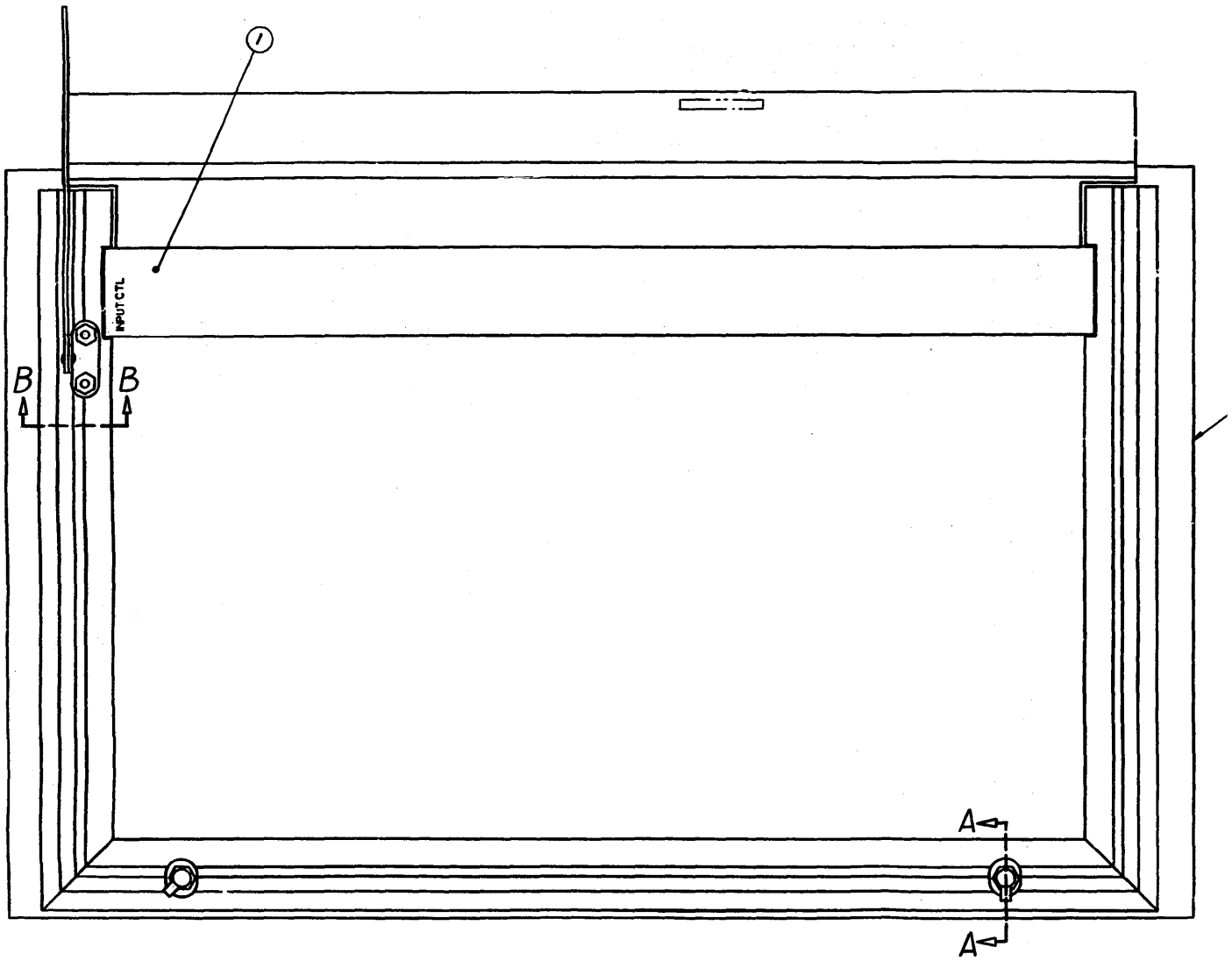
AMPEX | Ampex Corporation Redwood City, California | CODE IDENT NO 92739 | WIRE ROUTING LIST | 1464693 SHEET 17 OF 18 | REV. E

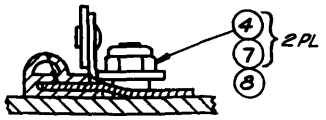
WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
676.	30		XA9	70		XA10	52	KEY-EXP-DD7	22
677.				71			53	DE0	
678.				72			54	DE1	
679.				73			55	DE2	
680.				74			56	DE3	
681.				75			58	DE4	
682.				76			59	DE5	
683.				78			60	DE6	
684.				79			61	KEY-EXP-DE7	
685.				80			62	DF0	
686.				81			63	DF1	
687.				82			64	DF2	
688.				83			65	DF3	
689.				84			66	DF4	
690.				85			68	DF5	
691.				86			69	DF6	
692.				88		XA10	70	KEY-EXP-DE7	
693.				105		XA11	81	CLK-KEY1-11X1-TW+ } TWISTED PAIR	
694.				106			78	11X1-TW-	
695.				109			91	11X.5-TW } TWISTED PAIR	
696.				110			92	11X.5-TW+	
697				111			106	11X3-TW+ } TWISTED PAIR	
698.				112			105	11X3-TW-	
699.				155			148	VF1	
700.				156			145	VB0	
701.				168			162	FRAME	
702.				179			75	MH-TW+ } TWISTED PAIR	
703.				180			76	MH-TW-	
704.				181			85	MX3-TW+ } TWISTED PAIR	
705.				182		XA11	84	CLK-KEY1-MX3-TW-	
706.			XA9	188		XA27	139	B59	
707.			XA10	9		XA11	51	CLK-KEY2-1X.5-TW+ } TWISTED PAIR	
708.				10			52	1X.5-TW+	
709.				11			39	1X1-TW-	
710.				12			38	1X1-TW+	
711.				13			53	1X3-TW+	
712.				14			54	1X3-TW-	
713.				105			44	11X1-TW+	
714				106			43	11X1-TW-	
715.				109			55	11X.5-TW-	
716.				110			56	11X.5-TW+	
717.				111			65	11X3-TW+ } TWISTED PAIR	
718.				112			61	11X3-TW-	
719.				155			150	VB1	
720.	30		XA10	156		XA11	149	CLK-KEY2-VB0	22

AMPEX	Ampex Corporation Redwood City, California	CODE IDENT NO. 92739	WIRE ROUTING LIST	1464693 SHEET 18 OF 18	REV. E

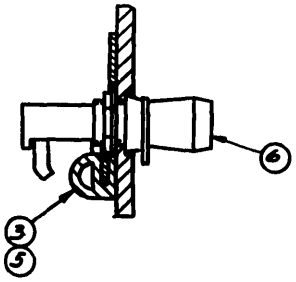
WIRE NO	GAUGE/ COND.	FROM STA	FROM REF DES.	FROM TERM	TO STA	TO REF DES.	TO TERM	REMARKS	LM ITEM NUMBER -02
721.	30		XA10	168		XA11	159	CLK-KEY2-FRAME	22
722.				179			41	MH-TW+ } TWISTED PAIR	
723.				180			40	MH-TW- }	
724.				181			50	MX3-TW+ } TWISTED PAIR	
725.				182		XA11	49	CLK-KEY2-MX3-TW- }	
726.			XA10	188		XA27	140	BS10	
727.			XA11	153		XA27	125	FLD-INT-2	
728.				154			126	FLD-INT-1	
729.	30		XA11	188		XA27	141	BS11	22

1464693





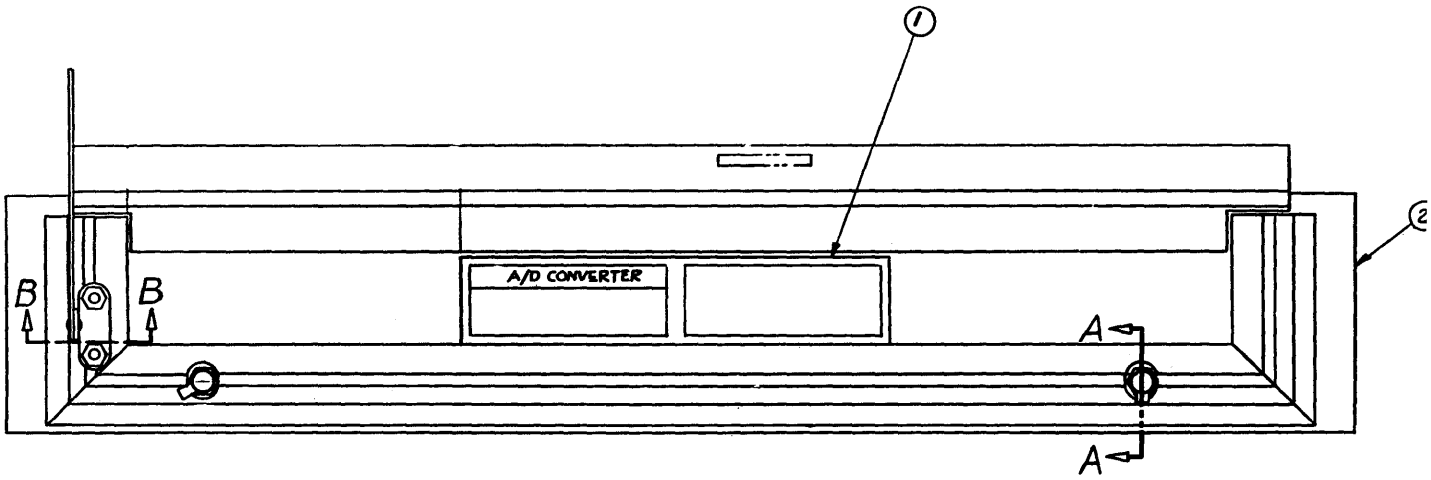
SECTION B-B
SCALE: 2/1

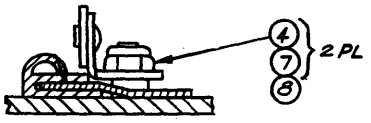


SECTION A-A
SCALE: 2/1

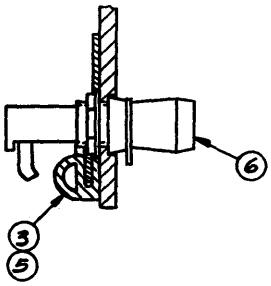
1	8	530-297	ENCLOSURE PART, SUPPORT BAR, 6.00LG
2	7	493-006	NUT, LOCKING, NYLON, HEX, 6-32
2	6	310-209	LATCH ASSY, ADJUSTABLE PAWL
AR	5	269-414	RUBBER, EXTRUSION, SILICONE, P SHAPE
2	4	280-344	SPACER, UNTHREADED, PLAIN, #6, .250 OD, .125 LG
AR	3	087-614	ADHESIVE, BASE, SILICONE, SEALER, 1 PART, ACETIC ACID
1	2	1420448-02	DOOR, DIGITAL
1	1	1420142-01	LABEL, DIGITAL DOOR
01	ITEM NO	PART NUMBER	DESCRIPTION

Assembly No. 1420465-01D. Digital Door Assembly





SECTION B-B
SCALE: 2/1



SECTION A-A
SCALE: 2/1

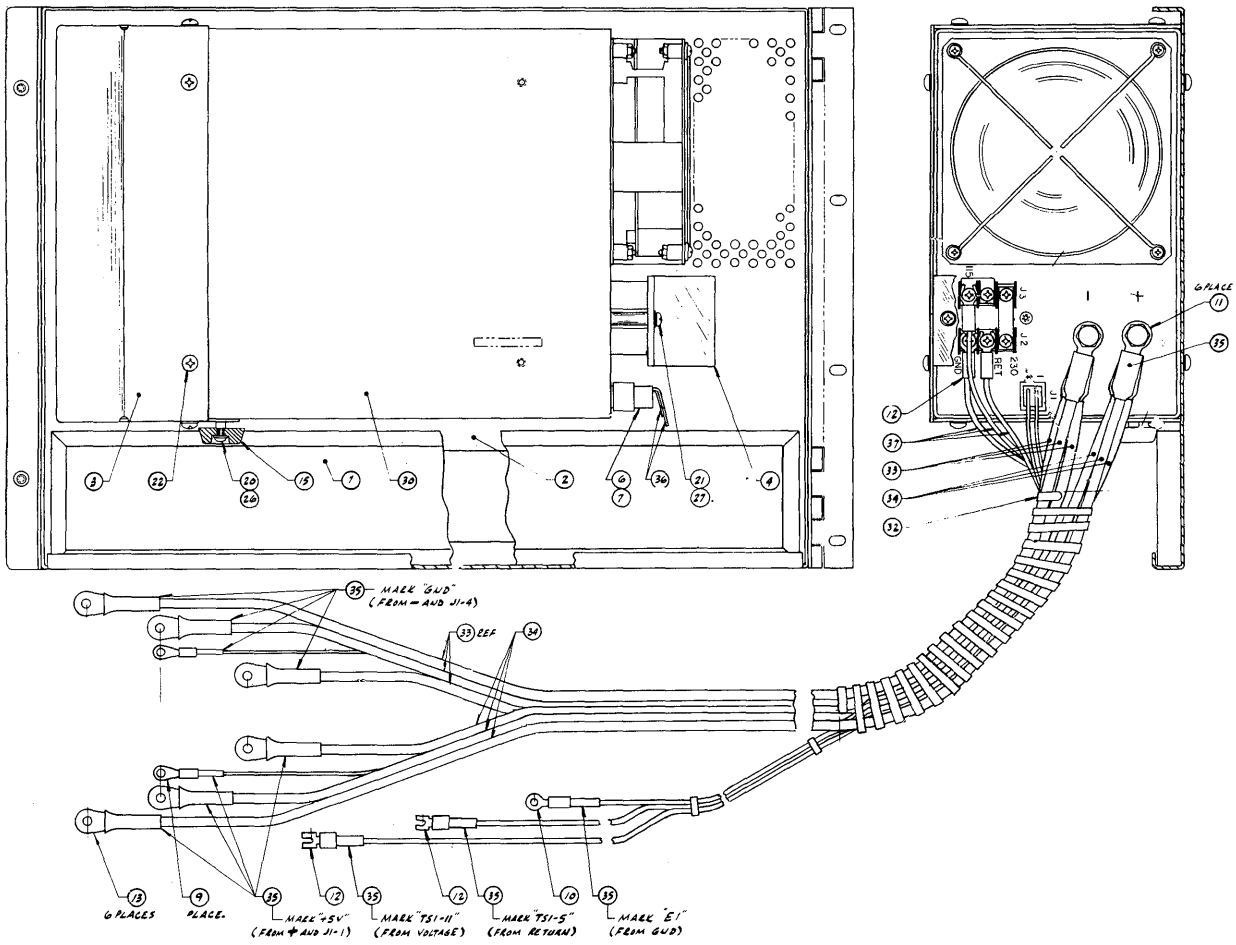
1	8	530-502	ENCLOSURE PART, SUPPORT BAR, 4.31 LG
2	7	493-006	NUT, LOCKING, NYLON, HEX, 6-32
2	6	310-289	LATCH ASSY, ADJUSTABLE PAWL
AR	5	269-414	RUBBER, EXTRUSION, SILICONE, P SHAPE
2	4	280-344	SPACER, UNTHREADED, PLAIN, #6, .250 OD, .125 LG
AR	3	087-614	ADHESIVE, BASE, SILICONE, SEALER, 1 PART, ACETIC ACID
1	2	1420447-02	DOOR, ANALOG
1	1	1420143-01	LABEL, ANALOG DOOR
01	ITEM NO	PART NUMBER	DESCRIPTION

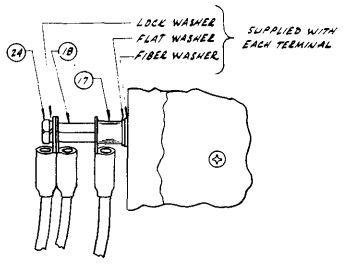
Assembly No. 1420466-01D. Analog Door Assembly

1465025-AA +5V POWER SUPPLY ASSEMBLY (120V) REV. A
1465025-AB +5V POWER SUPPLY ASSEMBLY (230V)

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -AA	-AB
1	1420401-01	FILTER, REAR		1	1
2	1464567-01	DOOR, REAR		1	1
3	1464983-01	DEFLECTOR, FAN EXHAUST		1	1
4	1465000-01	GUARD, TERMINAL BLOCK		1	1
5					
6	166-582	CONNECTOR PART, PLUG, RECTANGULAR, 6 POS		1	1
7	167-555	CONNECTOR PART, CONTACT, PIN, MALE, 24-18 AWG		2	2
8					
9	171-006	TERMINAL LUG, CRIMP, RING TONGUE, #8 STUD, 22-18 AWG, RED		2	2
10	171-016	TERMINAL LUG, CRIMP, RING TONGUE, #10 STUD, 12-10 AWG, YEL		1	1
11	172-374	TERMINAL LUG, CRIMP, RING TONGUE, 5/16 STUD, 6 AWG		6	6
12	172-394	TERMINAL LUG, CRIMP, SPADE TONGUE, #6 STUD, 12-10 AWG, YEL		5	5
13	172-396	TERMINAL LUG, CRIMP, RING TONGUE, #8 STUD, 6 AWG		6	6
14					
15	250-173	BUMPER, RECESSED, RUBBER, .969 OD, .375 HIGH		1	1
16					
17	280-187	SPACER, UNTHREADED, PLAIN, .315 ID, .437 OD, .500 LG		2	2
18	283-529	SPACER, THREADED, PLAIN, 5/16-18, .375 AF HEX, .75 LG		2	2
19					
20	473-326	SCREW, MACH, PAN HD., XREC DR, #4-40 X .375 LG, ASSEM WSHR		1	1
21	473-330	SCREW, MACH, PAN HD., XREC DR, #6-32 X .250 LG, ASSEM WSHR		2	2
22	475-072	SCREW, MACH, PAN HD., XREC DR, #8-32 X .250 LG, ASSEM WSHR		10	10
23					
24	480-145	BOLT, MACH, HEX HD., 5/16-18, .500 LG, STEEL, CAD PLATE		2	2
25					
26	501-008	WASHER, PLAIN, .125 ID, .312 OD, #4		1	1
27	501-009	WASHER, PLAIN, .156 ID, .375 OD, #6		2	2
28					
29					
30	570-584	POWER SUPPLY, SWITCHER, SINGLE OUTPUT, +5V, ±10%		1	1
31					
32	600-070	SLEEVING, SPIRAL WRAP (22 INCHES)		A/R	A/R
33	617-637	WIRE, STRANDED, INSULATED, 6 AWG, BLACK		A/R	A/R
34	617-854	WIRE, STRANDED, INSULATED, 6 AWG, RED		A/R	A/R
35		SLEEVING, SHRINKABLE		A/R	A/R
36		WIRE, STRANDED, INSULATED, 22 AWG		A/R	A/R
37		WIRE, STRANDED, INSULATED, 12 AWG		A/R	A/R

LM-1465025





POSITIVE & NEGATIVE TERMINAL CONSTRUCTION

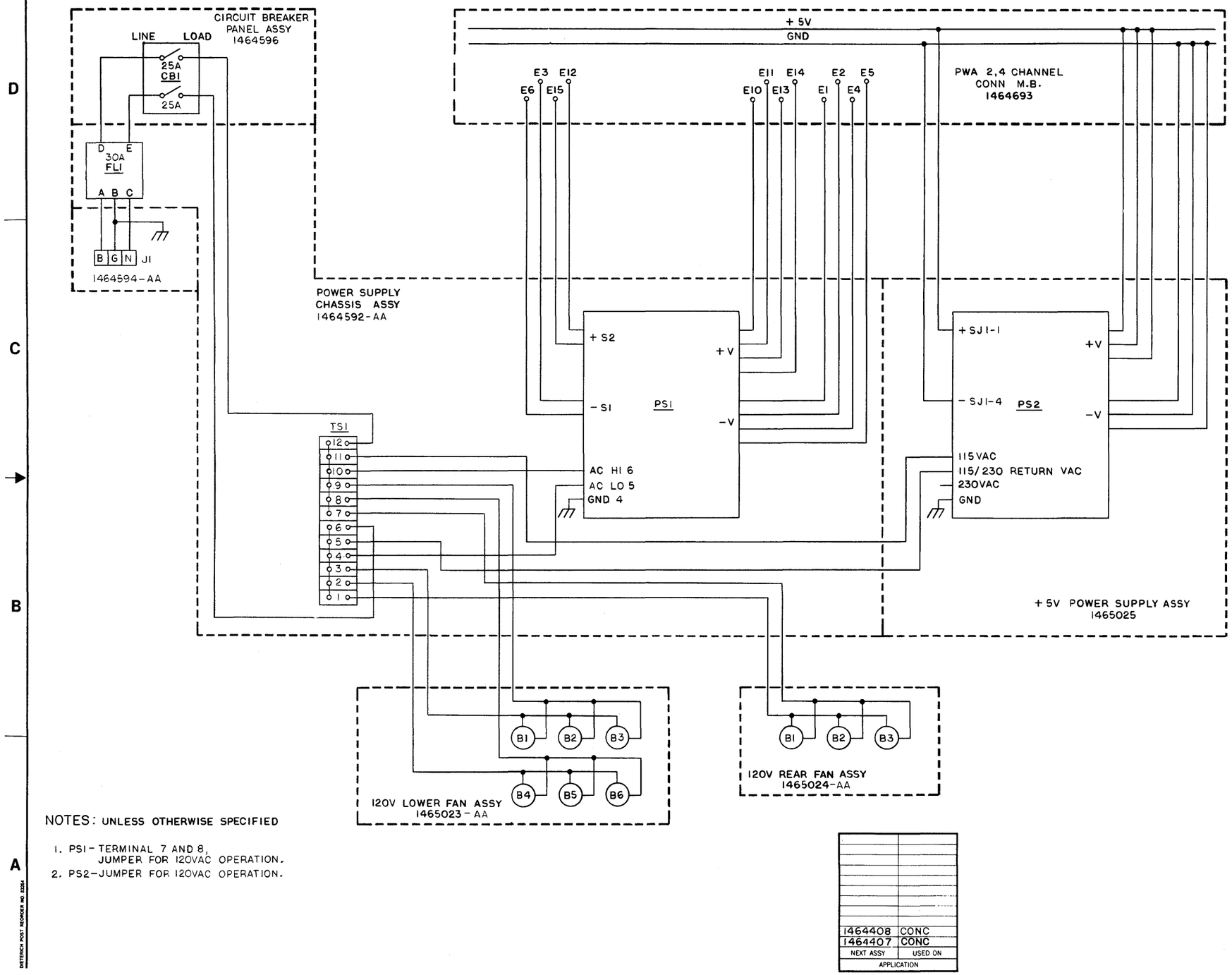
REMOVE THE TWO HEX NUTS FROM EACH TERMINAL AND DISCARD. RE-ASSEMBLE SUPPLIED HARDWARE AS SHOWN

-AA 20V SHOWN
-AB 230V

Assembly No. 1465025-AA A. +5V DC Power Supply Assembly (120 AC)
Assembly No. 1465025-AB A. +5V DC Power Supply Assembly (230 AC)

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1464592-AA	POWER SUPPLY CHASSIS ASSEMBLY		1
2	1464594-AA	CONNECTOR PANEL ASSEMBLY		1
3	1464596-01	CIRCUIT BREAKER PANEL ASSEMBLY		1
4	1465023-AA	LOWER FAN ASSEMBLY		1
5	1465024-AA	REAR FAN ASSEMBLY		1
6	1465025-AA	+5V POWER SUPPLY ASSEMBLY		1
7	1465060	WIRING DIAGRAM 120V/230V AC/DC INTERCONNECT		(-)
8	1420244-03	A.C. CABLE ASSEMBLY, NTSC		1

LM-1464407



NOTES: UNLESS OTHERWISE SPECIFIED

1. PS1 - TERMINAL 7 AND 8, JUMPER FOR 120VAC OPERATION.
2. PS2 - JUMPER FOR 120VAC OPERATION.

1464408	CONC
1464407	CONC
NEXT ASSY	USED ON
APPLICATION	

DIETZGEN POST REORDER NO. 5334

Schematic No. 1465060—.
120V/230V Interconnect
(Sheet 1 of 2)

CIRCUIT BREAKER PANEL ASSY 1420217-02
LINE
LOAD
15A CB1
15A
D E 20A FL1
A B C
Y G X J1
1464594-AB
+5V
GND
E3 E12 E6 E15
E11 E14 E10 E13
E2 E5 E1 E4
PWA 2,4 CHANNEL CONN M.B. 1464693
POWER SUPPLY CHASSIS ASSY 1464592 - AB
+S2
+V
-S1
PS1
-V
AC HI 6
AC LO 5
GND 4
TS1
12
11
10
9
8
7
6
5
4
3
2
1
+SJ1-1
+V
-SJ1-4
PS2
-V
115VAC
115/230 RETURN VAC
230VAC
GND
+5V POWER SUPPLY ASSY 1465025
B1 B2 B3 B4 B5 B6
230V LOWER FAN ASSY 1465023-AB
B1 B2 B3
230V REAR FAN ASSY 1465024-AB

NOTES: UNLESS OTHERWISE SPECIFIED

1. PS1 - REMOVE TERMINAL 7 AND 8 FOR 230VAC OPERATION.
2. PS2-REMOVE TERMINAL LINK J2 TO J3 FOR 230VAC OPERATION.

Schematic No. 1465060—. 120V/230V Interconnect (Sheet 2 of 2)

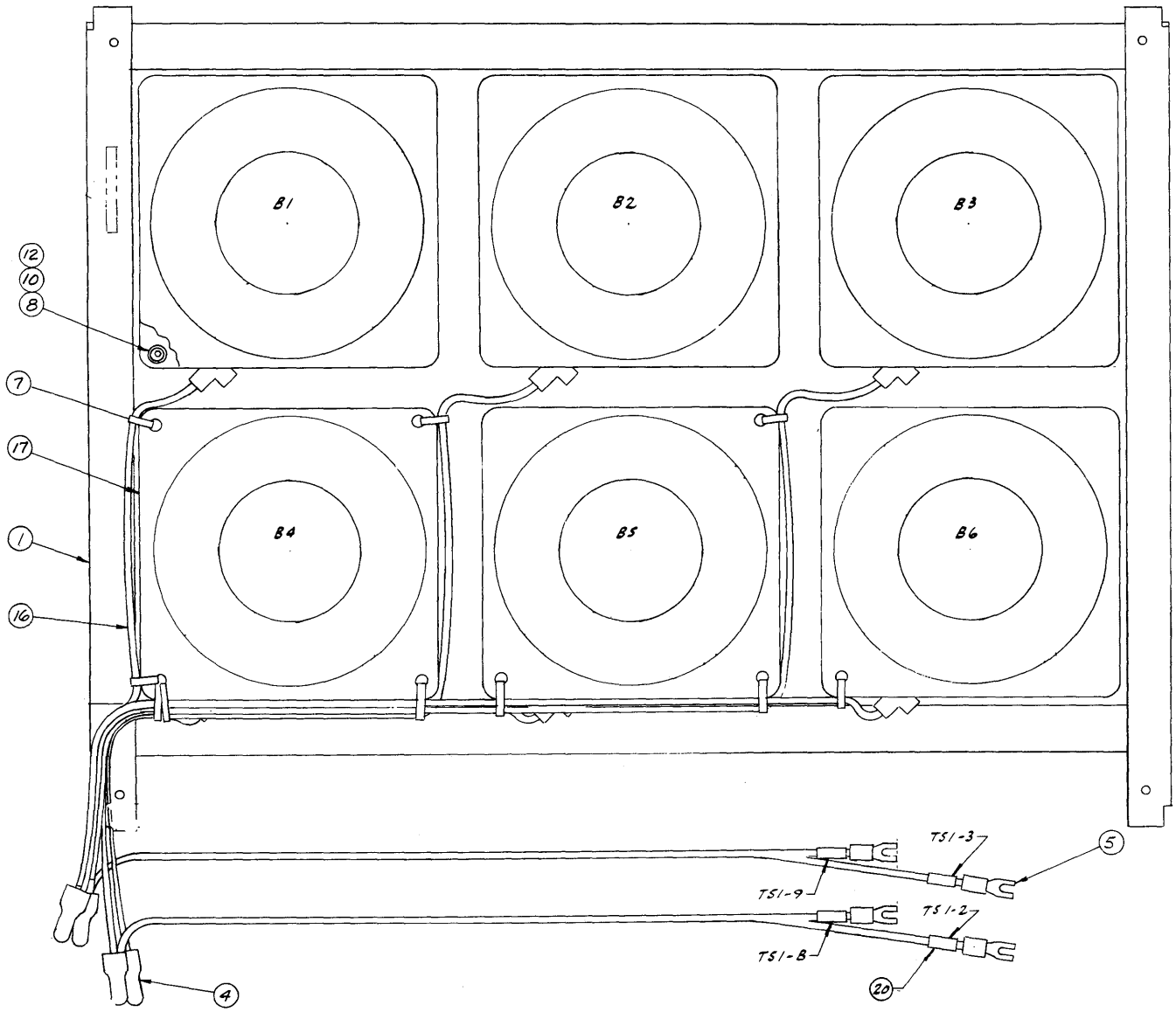
ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1464592-AB	POWER SUPPLY CHASSIS ASSEMBLY		1
2	1464594-AB	CONNECTOR PANEL ASSEMBLY		1
3	1420217-02	CIRCUIT BREAKER PANEL ASSEMBLY		1
4	1465023-AB	LOWER FAN ASSEMBLY		1
5	1465024-AB	REAR FAN ASSEMBLY		1
6	1465025-AB	+5V POWER SUPPLY ASSEMBLY		1
7	1465060	WIRING DIAGRAM, 120V/230V AC/DC INTERCONNECT		(-)
8	1420209-01	A.C. CABLE ASSEMBLY, 230V		1

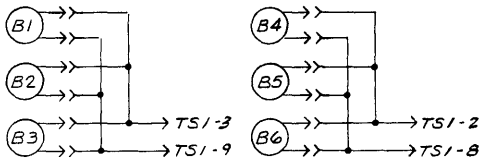
LM-1464408

1465023-AA LOWER FAN ASSEMBLY (120V) REV. A
1465023-AB LOWER FAN ASSEMBLY (230V)

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER	
				AA	AB
1	1420375-01	PANEL, LOWER FAN		1	1
2					
3					
4	187-401	TERMINAL, SPLICE, 18-12 AWG		4	4
5	171-004	TERMINAL LUG, SPADE, #6, 16-14 AWG		4	4
6					
7	302-379	STRAP, CABLE		A/R	A/R
8	470-021	SCREW, CAP, SOC HD., #6-32 X .62 LG		24	24
9					
10	501-009	WASHER, PLAIN, #6		24	24
11					
12	502-003	WASHER, SPRING LOCK, #6		24	24
13					
14					
15	591-317	FAN UNIT, AXIAL, 96/112 CFM, 220V	B1-6	-	6
16	591-140	FAN PART, CORD SET		6	6
17	591-320	FAN UNIT, AXIAL, 96/112 CFM, 120V	B1-6	6	-
18	616-031	CABLE, MOLDED, 2 COND, 18 AWG		A/R	A/R
19					
20	CD726	SLEEVING, SHRINKABLE		A/R	A/R

LM-1465023





SCHEMATIC

-AA 120V SHOWN

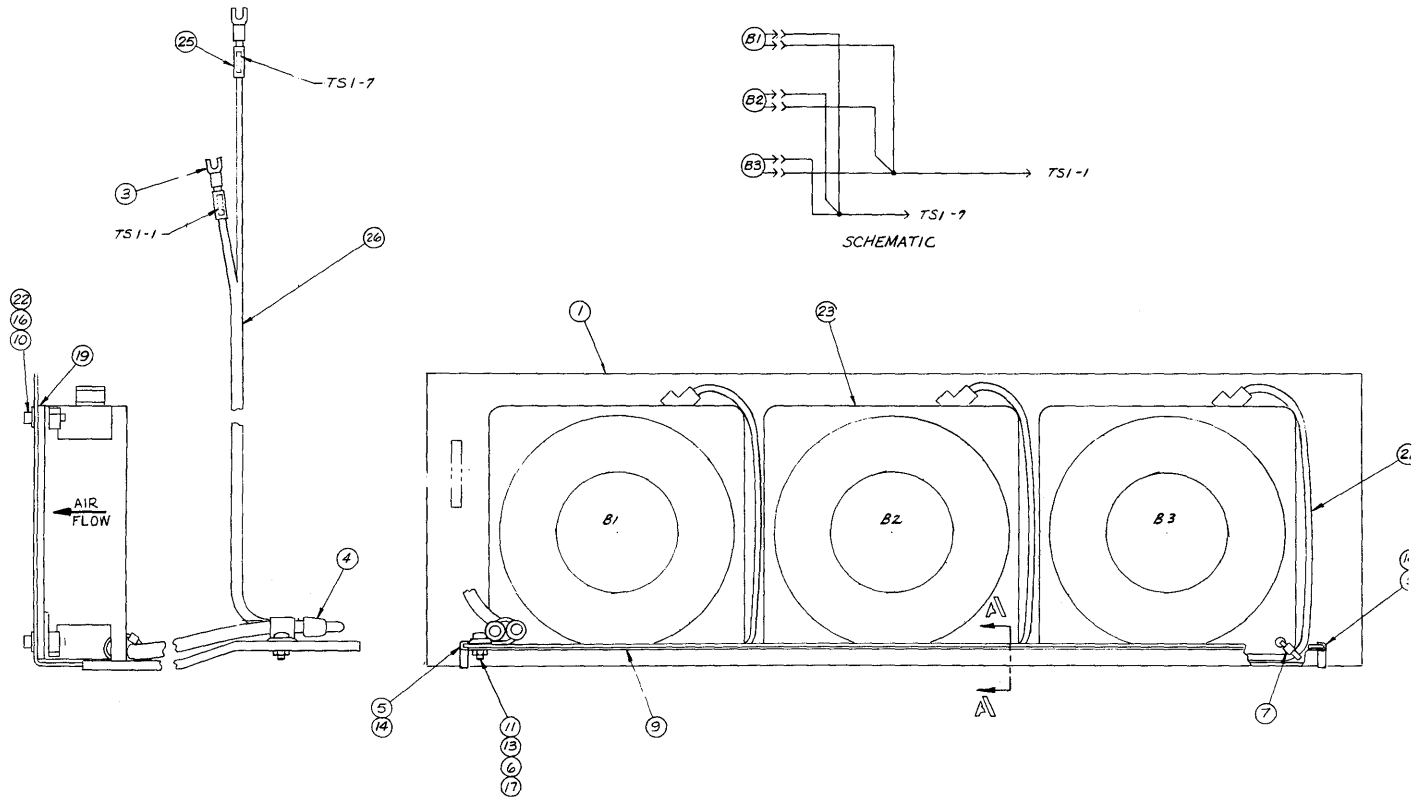
-AB 230V

Assembly No. 1465023-AA/AB A. Lower Fan Assembly

1465024-AA REAR FAN ASSEMBLY (120V) REV. A
1465024-AB REAR FAN ASSEMBLY (230V)

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER	
				AA	AB
1	1420149-02	BRACKET, REAR FAN		1	1
2					
3	171-004	TERMINAL LUG, SPADE, #6, 16-14 AWG		2	2
4	187-401	TERMINAL, SPLICE, 18-12 AWG		2	2
5	260-052	GROMMET, CATERPILLAR		A/R	A/R
6	302-200	CLAMP, CABLE, .375 ID		1	1
7	302-379	STRAP, CABLE		5	5
8					
9	225-469	TAPE, POLYESTER. .007 THK, 1.00 WIDE, (32.00 IN)		A/R	A/R
10	470-023	SCREW, CAP, HEX SOC., #6-32 X .875 LG, ALLOY STL		12	12
11	471-070	SCREW, PAN HD., #6-32 X .44 LG		1	1
12					
13	496-005	NUT, KEP, #6-32		1	1
14	018-438	ADHESIVE, BASE, CYANOACRYLATE, 1 PART		A/R	A/R
15					
16	501-009	WASHER, PLAIN, #6		12	12
17	506-013	WASHER, D		1	1
18					
19	591-277	FAN PART, FINGER GUARD		3	3
20	591-317	FAN UNIT AXIAL, 96/112 CFM, 220VAC	B1-3	-	3
21	591-140	FAN PART, CORD SET		3	3
22	591-280	FAN UNIT, MTG CLIP		12	12
23	591-320	FAN UNIT, AXIAL, 96/112 CFM, 120V	B1-3	3	-
24					
25	CD726	SLEEVING, SHRINKABLE		A/R	A/R
26	616-031	CABLE, MOLDED, 2 COND, 18 AWG		A/R	A/R

LM-1465024



-AA 120V SHOWN
-AB 230V

Assembly No. 1465024-AA/AB A. Rear Fan Assembly

1464592-AA POWER SUPPLY CHASSIS ASSEMBLY (120V) REV. C
1464592-AB POWER SUPPLY CHASSIS ASSEMBLY (230V)

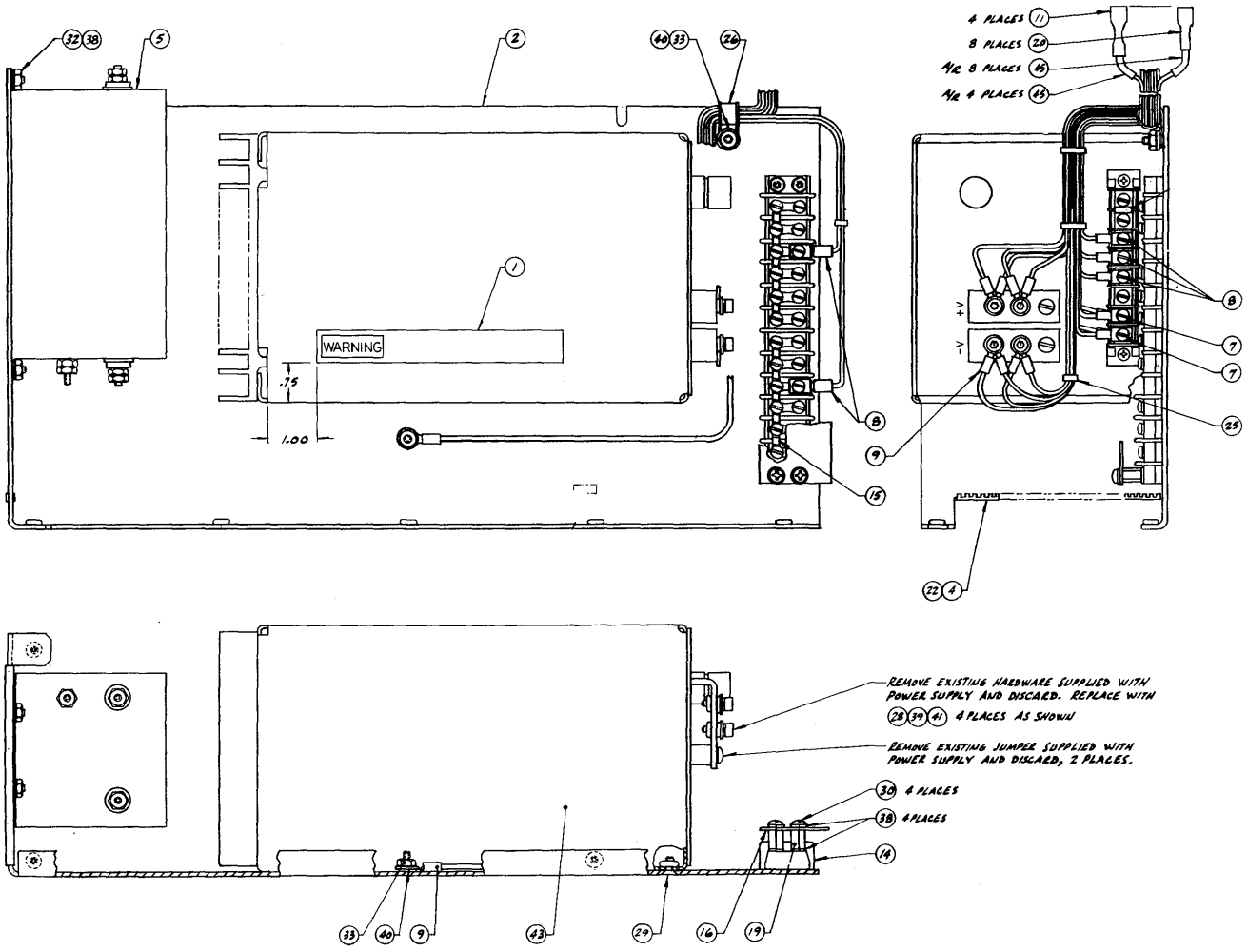
ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -AA	-AB
1	1403328-AB	LABEL, WARNING		1	1
2	1464593-01	TRAY, POWER SUPPLY		1	1
3	1465060	WIRING DIAGRAM, 120V/230V AC/DC INTERCONNECT		A	A
4	018-438	ADHESIVE, BASE, CYANOACRYLATE, BONDING, 1 PART		A/R	A/R
5	052-031	FILTER, RF INTERFERENCE, 30A, 115/250 VAC, 50-60 Hz	FL1	1	-
6	052-259	FILTER, RF INTERFERENCE, 20A, 115/250 VAC, 50-60 Hz	FL1	-	1
7	171-003	TERMINAL LUG, CRIMP, SPADE TONGUE, 22-18 AWG, RED		4	4
8	171-004	TERMINAL LUG, CRIMP, SPADE TONGUE, 16-14 AWG, BLUE		5	5
9	171-007	TERMINAL LUG, CRIMP, RING TONGUE, 16-14 AWG, BLUE		9	9
10					
11	172-363	TERMINAL, QUICK DISCONNECT, FEMALE, 22-18 AWG, RED		4	4
12					
13					
14	180-009	TERMINAL STRIP, BARRIER, 12 TERMINALS	T1	1	1
15	180-142	TERMINAL STRIP PART, JUMPER CLIP, BARRIER	(T1)	10	10
16	180-392	TERMINAL STRIP PART, MARKER STRIP, 12 TERM	(T1)	1	1
17					
18					
19	283-057	SPACER, THREADED, PLAIN, #6-32, .250 AF, .375 LG, ALUM	(T1)	4	4
20	187-395	TERMINAL, QUICK DISCONNECT, FEMALE, 16-14 AWG, BLUE		8	8
21					
22	260-052	GROMMET, NYLON, CATERPILLAR		A/R	A/R
23					
24					
25	302-335	STRAP, CABLE, .095 WIDE X 4.00 LG, NATURAL NYLON		A/R	A/R
26	302-429	CLAMP, LOOP, OFFSET, .438 ID, .375 WIDE, BLACK		1	1
27					
28	470-037	SCREW, CAP, SOC. HD., HEX SOC DR., #10-32 X .438 LG		4	4
29	471-343	SCREW, MACH, FLAT HD., U-CUT, #8-32 X .250 LG		4	4
30	473-330	SCREW, MACH, PAN HD., XREC DR., #6-32 X .250 LG, ASSEM WSHR		4	4
31					
32	496-005	NUT, HEX, CAPTIVE LOCK WASHER, #6		4	4
33	496-006	NUT, HEX, CAPTIVE LOCK WASHER, #8		2	2
34					
35					
36					
37					

LM-1464592

AMPEX | Ampex Corporation, Redwood City, California | CODE IDENT NO. 92739 | LIST OF MATERIALS | LM-1464592 SHEET 2 OF 3 | REV C

ITEM NO	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -AA	-AB
38	501-009	WASHER, PLAIN, #6, .375 OD		12	12
39	501-070	WASHER, PLAIN, #10, .500 OD		4	4
40	501-205	WASHER, PLAIN, #8, .438 OD		6	6
41	502-005	WASHER, LOCK, HELICAL SPRING, #10		4	4
42					
43	570-611	POWER SUPPLY, SWITCHER, SINGLE VDC OUT, 5V	PS1	1	1
44					
45	CD726	SLEEVING, SHRINKABLE		A/R	A/R
46	CD739	WIRE, STRANDED, INSULATED, 20 AWG		A/R	A/R
47	CD740	WIRE, STRANDED, INSULATED, 14 AWG		A/R	A/R

LM-1464592

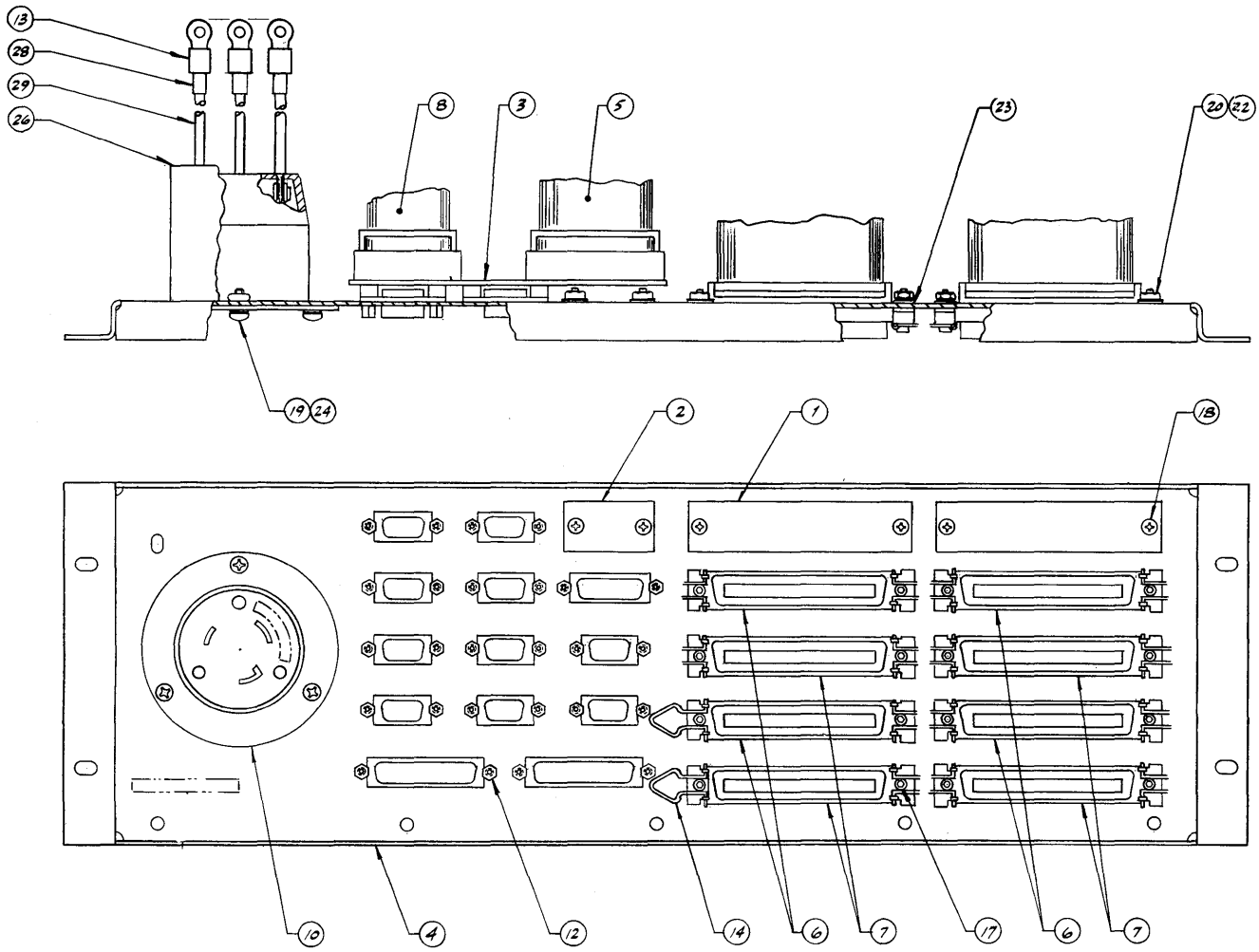


Assembly No. 1464592-AA/AB C. Power Supply Chassis Assembly

1464594-AA CONNECTOR PANEL ASSEMBLY (120V)
1464594-AB CONNECTOR PANEL ASSEMBLY (230V)

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -AA	-AB
1	1420239-AA	COVER, CONNECTOR HOLE		2	2
2	1420239-AB	COVER, CONNECTOR HOLE		1	1
3	1464420-01	PWA, CONTROL INTERCONNECT		1	1
4	1464595-01	CONNECTOR PANEL		1	1
5	1464988-01	CABLE, CONTROL PANEL, 34 PINS		1	1
6	1465007-AA	CABLE, CONNECTOR PANEL, 50 PINS		4	4
7	1465007-AB	CABLE, CONNECTOR PANEL, 50 PINS		4	4
8	1465008-01	CABLE, CONTROL PANEL, 26 PINS		1	1
9					
10	145-640	CONNECTOR, POWER CIRCUIT, 3 MALE CONTACTS; 30A, 125V		1	-
11	145-712	CONNECTOR, POWER CIRCUIT, 3 MALE CONTACTS; 30A, 250V		-	1
12	167-077	JACK SCREW ASSEMBLY (1 SET OF 2)		13	13
13	171-016	TERMINAL LUG, CRIMP, RING TONGUE, 12-10 AWG, YELLOW		3	-
14	177-163	CONNECTOR PART, BAIL LOCK (1 SET OF 2)		8	8
15	187-396	TERMINAL, QUICK DISCONNECT, FEMALE, 12-10 AWG, YELLOW		-	3
16					
17	470-011	SCREW, CAP, SOC HD., HEX SOC DR., #4-40 X .438 LG		16	16
18	471-061	SCREW, MACH, PAN HD., XREC DR., #4-40 X .312 LG		6	6
19	475-058	SCREW, MACH, PAN HD., XREC DR., #6-32 X .375 LG		3	3
20	496-004	NUT, HEX, CAPTIVE LOCK WASHER, #4		6	6
21					
22	501-088	WASHER, PLAIN, #4, .312 OD		6	6
23	501-169	WASHER, PLAIN, SMALL PATTERN, #4, .250 OD		16	16
24	501-188	WASHER, PLAIN, SMALL PATTERN, #6, .267 OD		3	3
25					
26	600-143	SLEEVING, SHRINKABLE, 2.00 EXP ID		A/R	A/R
27					
28	CD726	SLEEVING, SHRINKABLE		A/R	A/R
29	CD740	WIRE, STRANDED, INSULATED, 10 AWG		A/R	-
30	CD740	WIRE, STRANDED, INSULATED, 12 AWG		-	A/R
31					
32	1464570	INTERCONNECT DIAGRAM, 120V/230V CONN PANEL/MOTHER BD		B	B
33	1465060	WIRING DIAGRAM, 120V/230V AC/DC INTERCONNECT		A	A
34					
35					
36					
37					

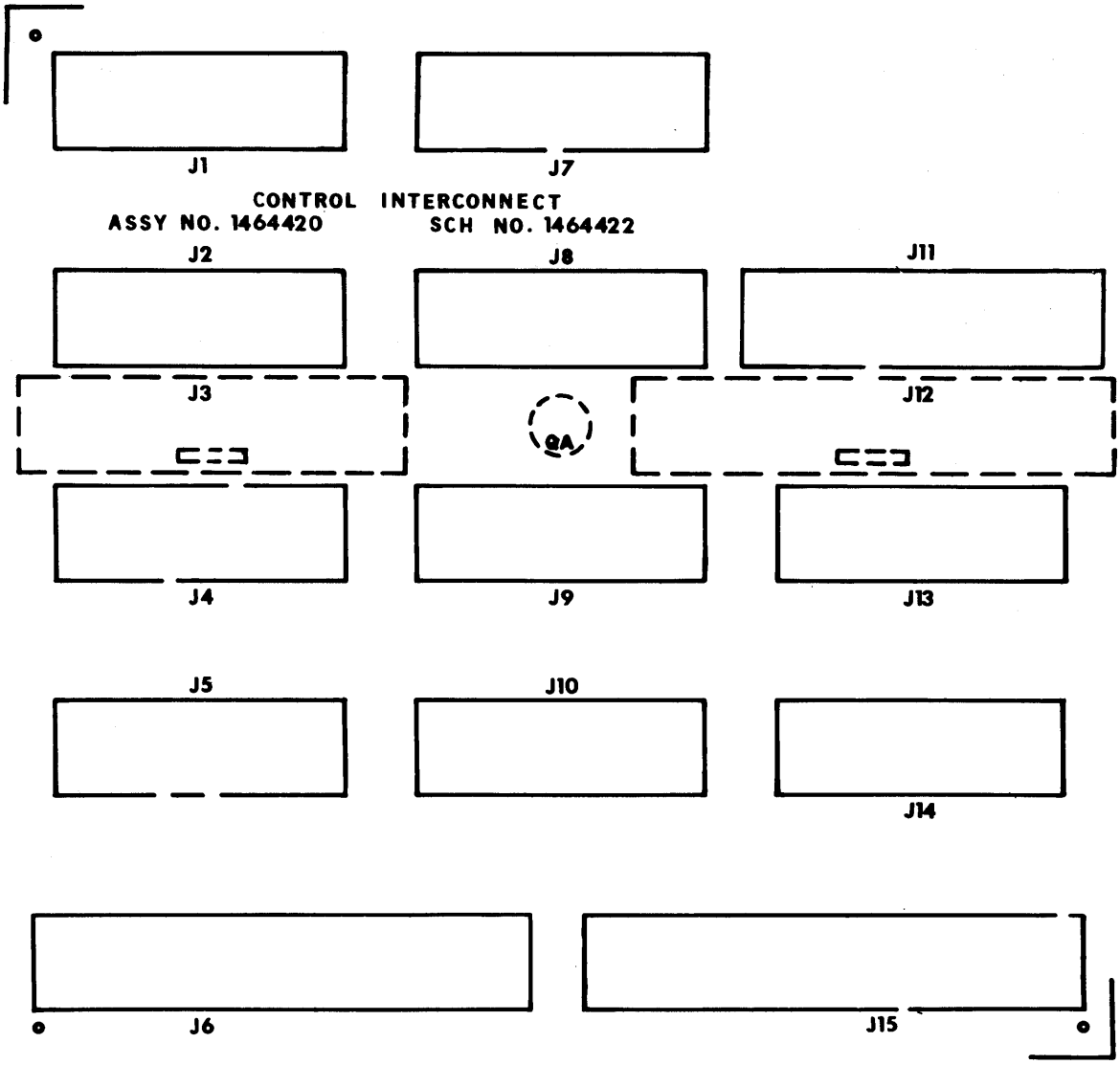
LM-1464594



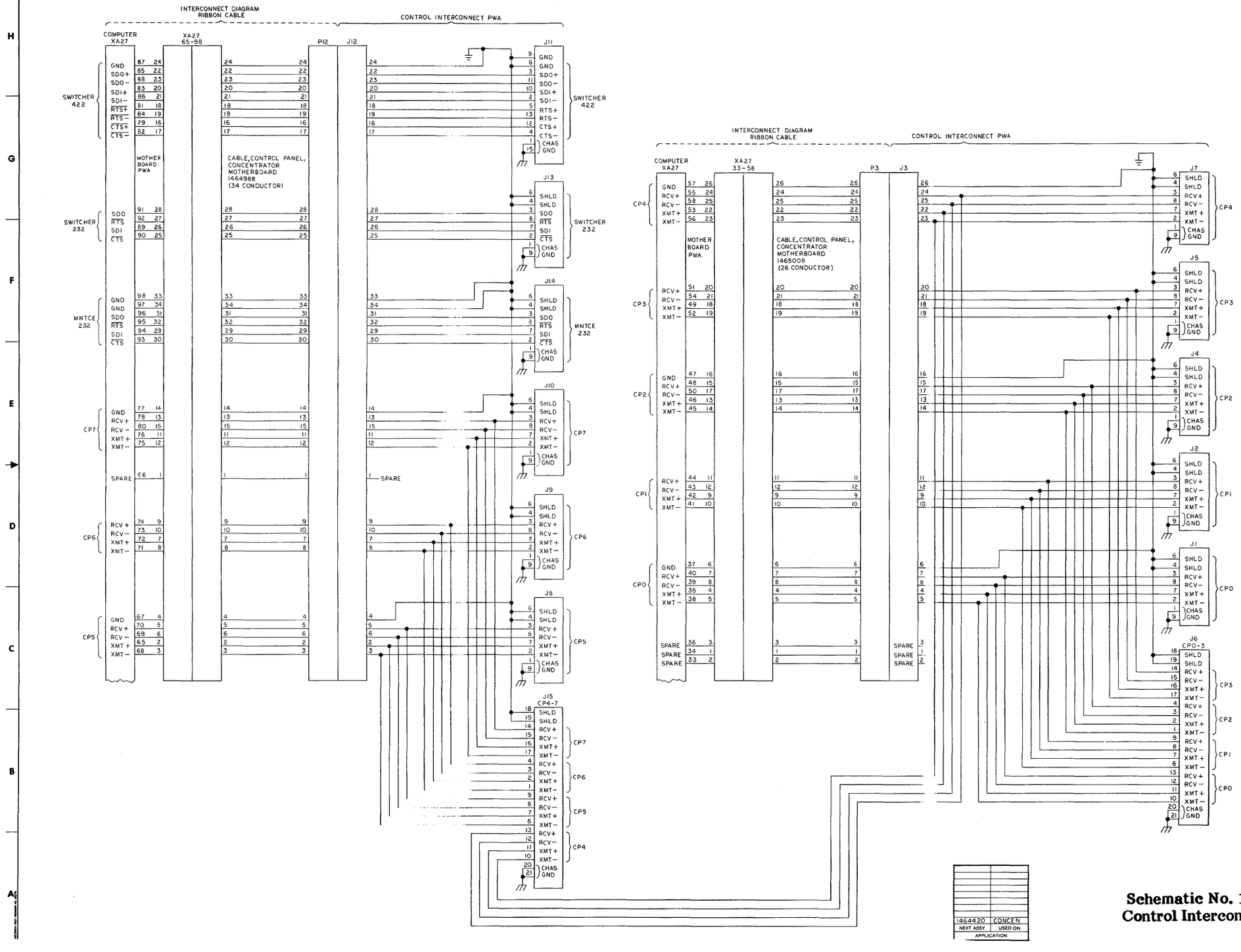
Assembly No. 1464594-AA/AB A. Connector Panel Assembly

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1464421	PRINTED WIRING BOARD		-01
2				
3	1464422	SCHEMATIC		(A)
4				
5	135-168	HEADER ASSY, 26 PIN	J3	1
6	135-341	HEADER ASSY, 34 PIN	J12	1
7				
8	140-647	CONNECTOR, RECEPT, 9 SOC	J1,2,4,5,7-10, 13,14	10
9	140-708	CONNECTOR, RECEPT, 25 SOC	J6,15	2
10	177-013	CONNECTOR, RECEPT, 15 SOC	J11	1

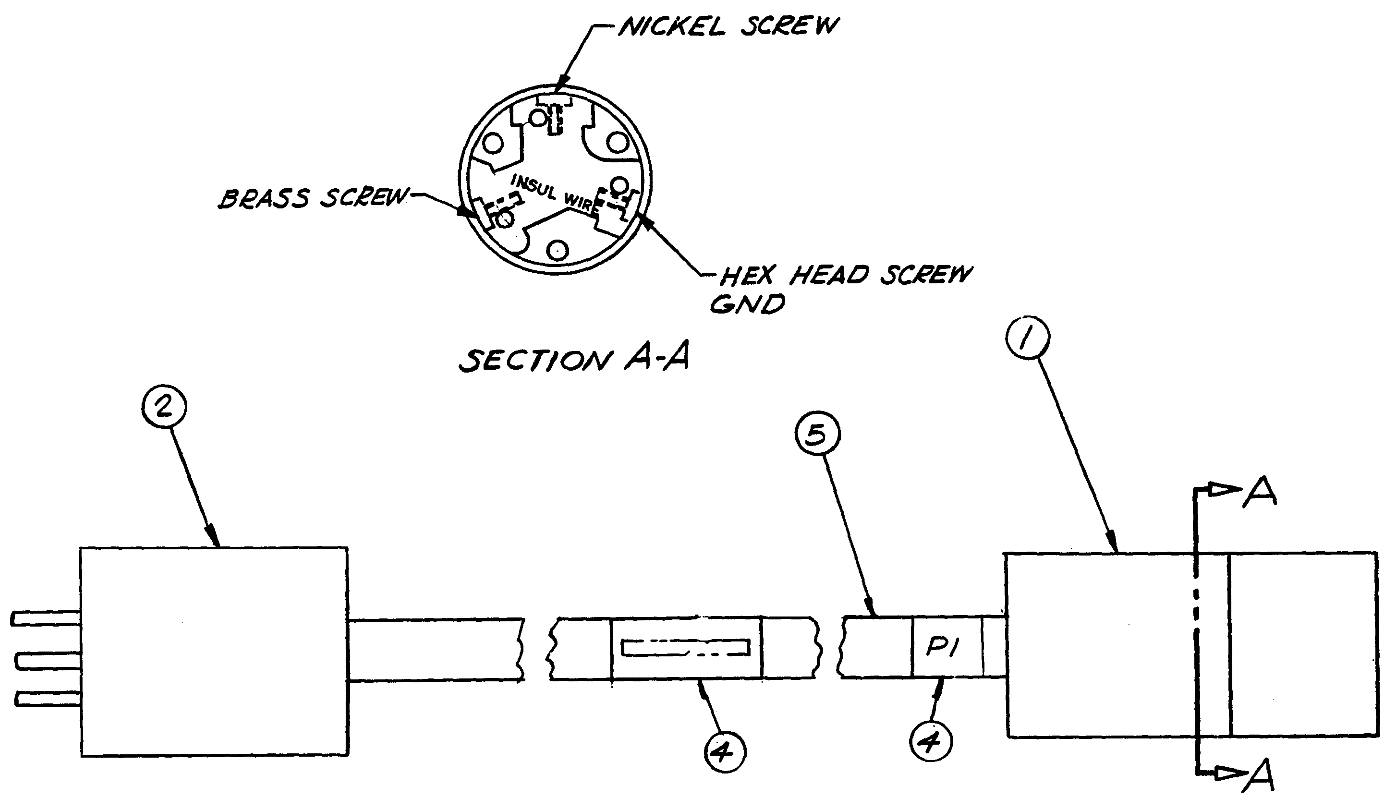
LM-1464420



Assembly No. 1464420-01C . Control Interconnect PWA



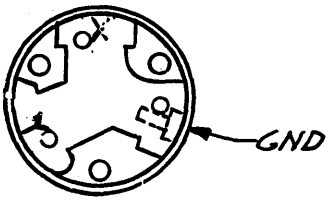
Schematic No. 1464422—.
Control Interconnect PWA



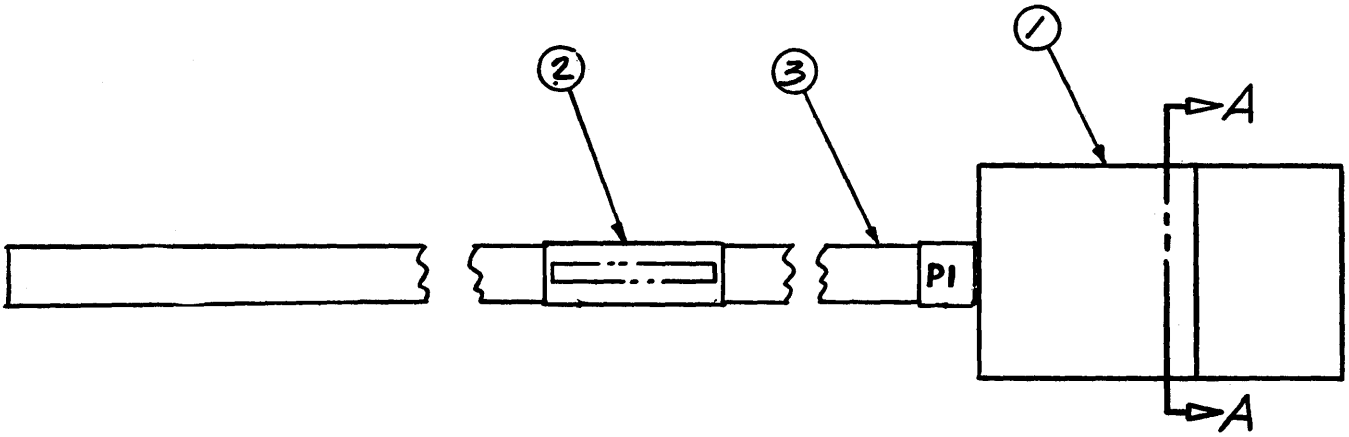
WIRE COLOR	P1	ITEM 2
0	BRASS	BRASS
9	NICKEL	NICKEL
5	GND	GND

-03	-02	-01	ITEM NO.	PART NUMBER	DESCRIPTION
A/R	~~1~~	–	5	616-015	CABLE, 3 COND., 10 AWG.
A/R	A/R	AR	4	600-097	TUBING, THERMOFIT, BLACK,
–	A/R	AR	3	~~616-042~~	CABLE, 3 COND., 12 AWG
1	1	1	2	145-639	CONNECTOR, MALE
1	1	1	1	145-637	CONNECTOR, FEMALE

Assembly No. 1420244-03E. 120V AC Cable Assembly



WIRE COLOR	P1
0	Y
9	X
5	GND

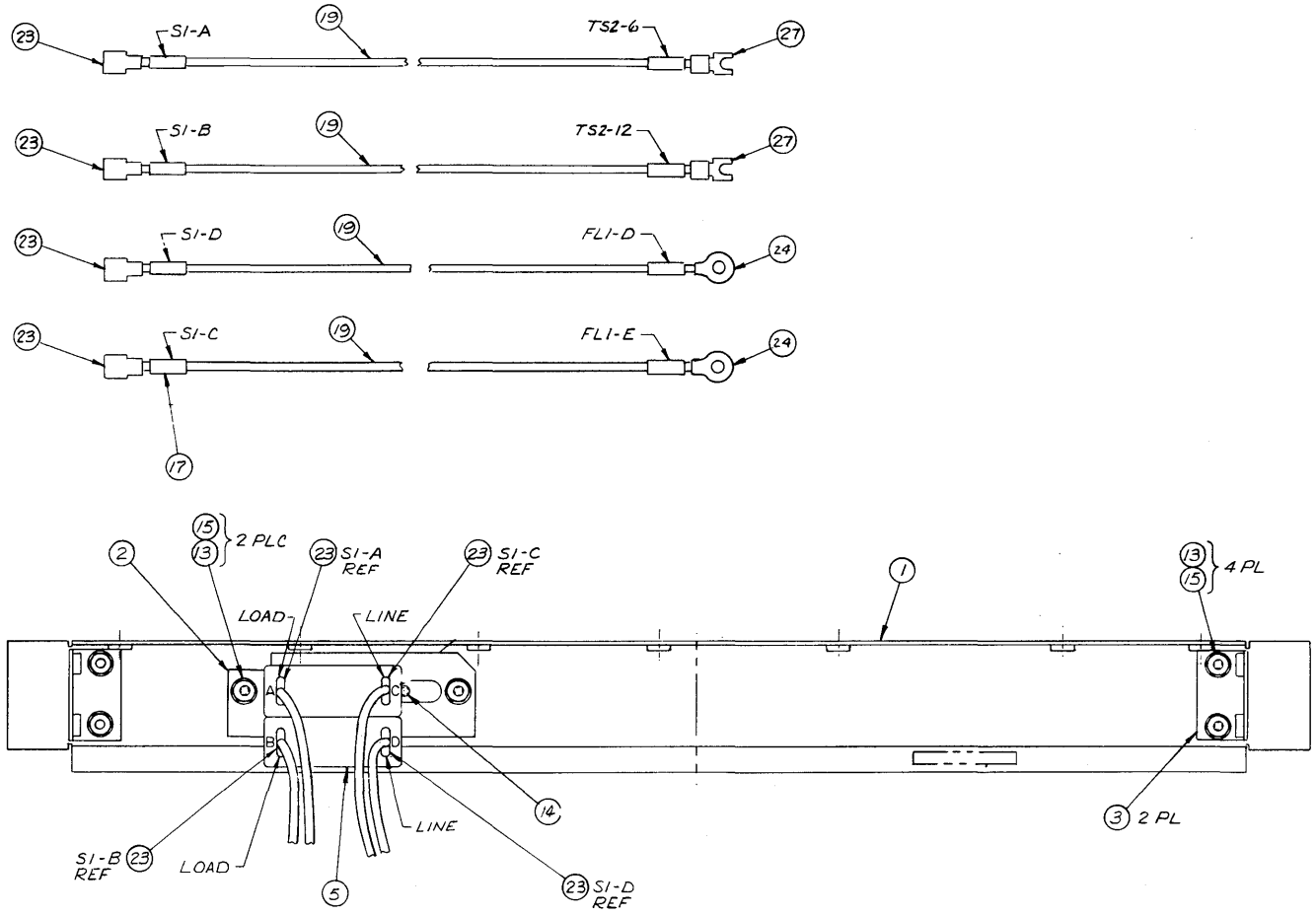


AR	3	616-042	CABLE, 3 COND, 12 AWG		
AR	2	600-097	SLEEVING, SHRINKABLE, BLACK		
1	1	145-638	CONNECTOR, FEMALE		
01	ITEM NO.	PART NUMBER		DESCRIPTION	

Assembly No. 1420209-01A. 230V AC Cable Assembly

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1464597-01	PANEL, CIRCUIT, BREAKER		1
2	1464598-01	PLATE, MTG.		1
3	1420166-01	BRACKET, CKT, BREAKER PANEL		2
4				
5	1465026-01	CIRCUIT BREAKER, 25 AMP, 125V	CB1	1
6	1465060	WIRING DIAGRAM, 120V/230V AC/DC INTERCONNECT		A
7				
8				
9				
10				
11				
12	302-379	STRAP, CABLE		A/R
13	496-005	NUT, KEP, #6-32		6
14	473-309	SCREW, FLAT HD., 82°, XREC, UNDERCUT HD, 6-32 X .312 LG		2
15	501-009	WASHER, PLAIN, #6		6
16				
17	CD726	SLEEVING, SHRINKABLE		A/R
18				
19	CD740	WIRE, STRANDED INSULATED, 10 AWG		A/R
20				
21				
22				
23	187-396	TERMINAL QUICK DISCONNECT, 10-12 AWG, YEL		4
24	171-016	TERMINAL LUG, CRIMP, RING TONGUE, 12-10 AWG, YELLOW		2
25				
26				
27	172-394	TERMINAL LUG CRIMP, SPADE, #6 STUD, #12-10 AWG		2

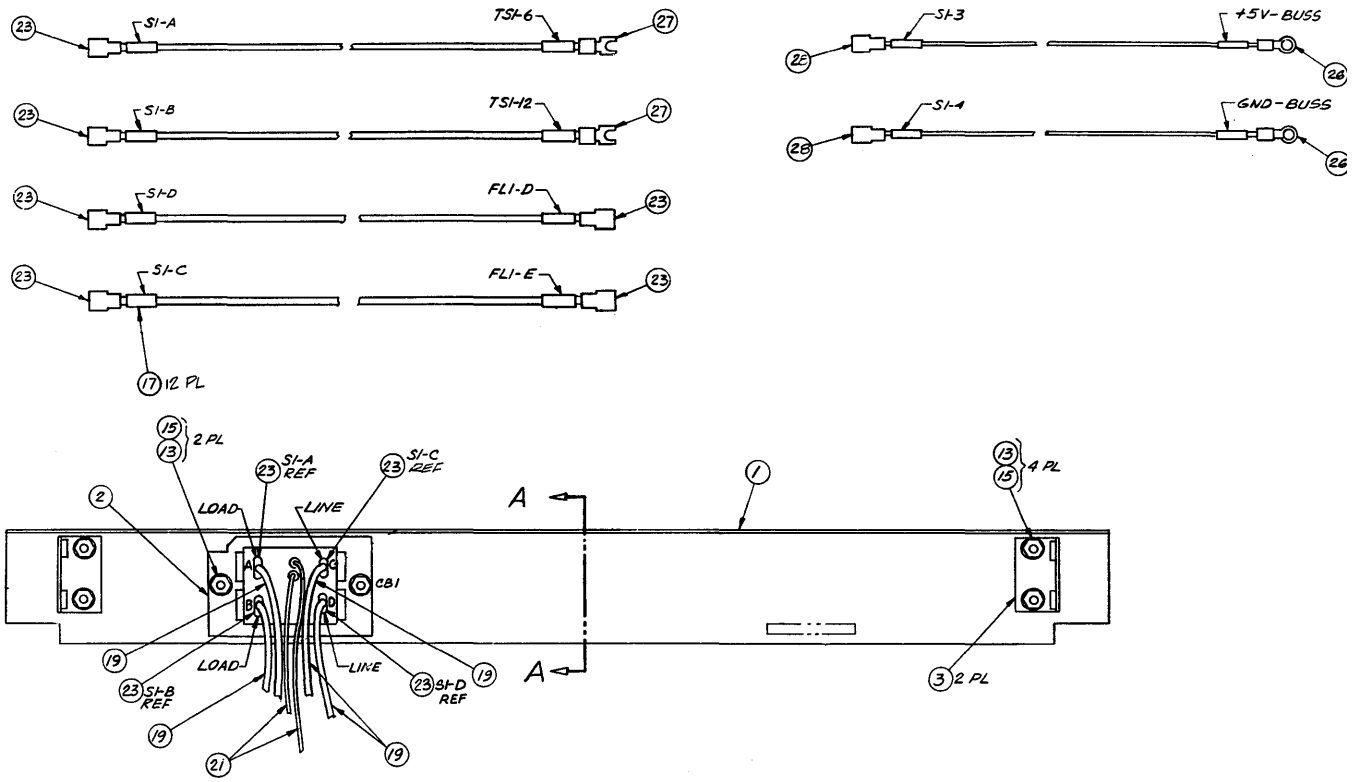
LM-1464596



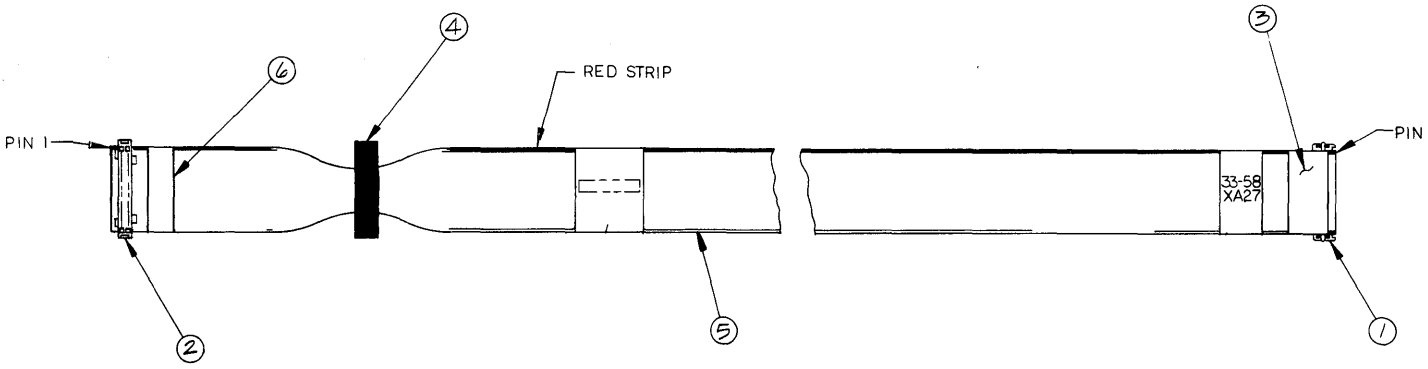
Assembly No. 1464596-01B. 120V Circuit Breaker Panel Assembly

ITEM NO.	PART NUMBER	D	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01	-02
1	1420141-01		PANEL, CIRCUIT BREAKER		1	1
2	1420147-01		PLATE, MOUNT		1	1
3	1420166-01		BRACKET, CKT BREAKER PANEL		2	2
4						
5	1464253-01		CIRCUIT BREAKER, 15 AMP, 250V	CB1	-	1
6						
7						
8						
9	283-400		SPACER, UNTHREADED PLAIN, .171 ID X .250 OD X .187 LG		2	2
10						
11						
12	302-379		STRAP, CABLE		A/R	A/R
13	496-005		NUT, KEP, 6-32		6	6
14						
15	501-009		WASHER, PLAIN, #6		6	6
16						
17			SLEEVING, SHRINKABLE		A/R	A/R
18						
19			WIRE, STRANDED INSULATED, 12 AWG		A/R	A/R
20						
21			WIRE, STRANDED INSULATED, 22 AWG		A/R	A/R
22						
23	187-396		TERMINAL QUICK DISCONNECT, 10-12 AWG, YEL		6	6
24						
25	187-399		TERMINAL QUICK DISCONNECT, 18-22 AWG, RED		2	-
26	171-178		TERMINAL LUG CRIMP, RING, #10 STUD, #22-18 AWG		2	2
27	172-394		TERMINAL LUG CRIMP, SPADE, #6 SUTD, #12-10 AWG		2	2
28	187-358		TERMINAL, QUICK DISCONNECT, 18-22 AWG		-	2

LM-1420217

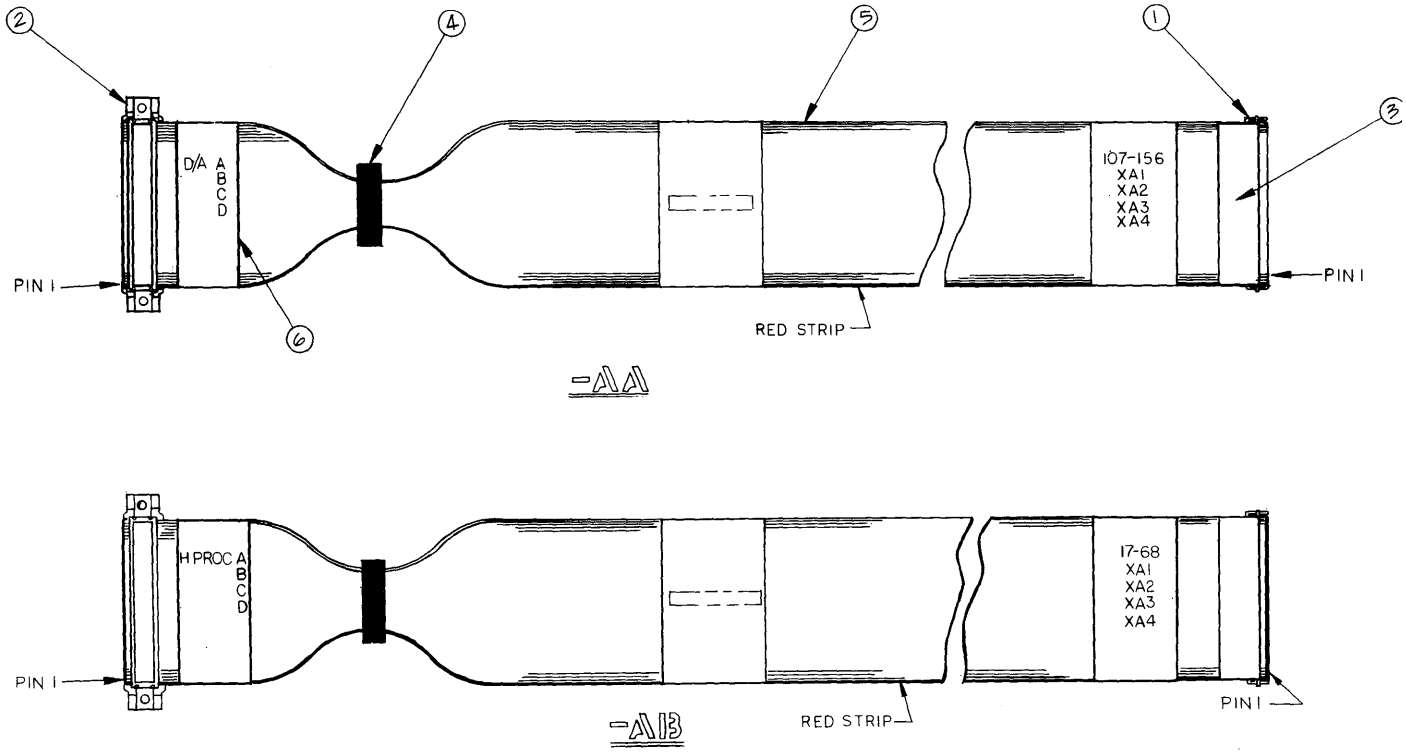


Assembly No. 1420217-02E. 230V Circuit Breaker Panel Assembly



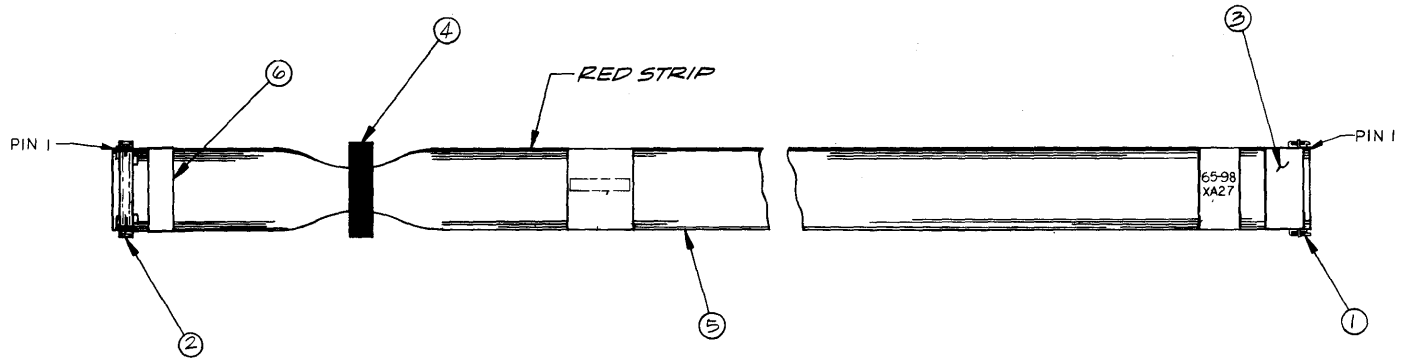
AR	6		TUBING, SHRINK, 1.00 I.D.
AR	5	616-868	CABLE, RIEBON, 26 CONDUCTOR, 28 AWG.
1	4	226-089	CORE, MAGNETIC, FERRAMIC H MAT'L
1	3	177-328	STRAIN RELIEF, CONN. PART
1	2	140-567	CONNECTOR, SIGNAL CIRCUIT 26 CONTACT
1	1	140-895	CONNECTOR, SIGNAL CIRCUIT 26 PINS
01	ITEM NO	PART NUMBER	DESCRIPTION

Assembly No. 1465008-01A. Control Panel Cable



A/R	A/R	6		TUBING, SHRINK, 2.50 I.D.
A/R	A/R	5	6116-692	CABLE, RIBBON, 50 CONDUCTOR, 26 AWG
1	1	4	226-089	CORE, MAGNETIC, FERRAMIC H MAT'L., 1.250 O.D. X .750 I.D.
1	1	3	177-164	STRAIN RELIEF, CONN. PART
1	1	2	140-689	CONNECTOR, SIGNAL CIRCUIT, 50 CONTACTS
1	1	1	140-276	CONNECTOR, SIGNAL CIRCUIT, 50 PINS
AB	AA	ITEM NO.	PART NUMBER	DESCRIPTION

Assembly No. 1465007-AA/AB B. Digital Motherboard Connector Panel Cable



AR	6		TUBING, SHRINK, 1.00 I.D.	
AR	5	646-724	CABLE, RIBBON, 34 CONDUCTOR, 28 AWG	
1	4	226-089	CORE, MAGNETIC, FERRAMIC H MAT'L.	
1	3	177-329	STRAIN RELIEF, CONN. PART	
1	2	140-565	CONNECTOR, SIGNAL CIRCUIT, 34 CONTACTS	
1	1	140-896	CONNECTOR, SIGNAL CIRCUIT, 34 PINS	
01	ITEM NO.	PART NUMBER	DESCRIPTION	

Assembly No. 1464988-01A. Control Concentrator Motherboard Panel Cable

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01	-02	-03
1	1464412	PRINTED WIRING BOARD		-01	-02	-02
2						
3	1464413	SCHEMATIC		(-)	B	C
4						
5	1409670-CD	LABEL, EXTRACTOR ARM		1	1	1
6	1409976-AA	INSULATOR, STIFFENER		1	1	1
7	1409976-AB	INSULATOR STIFFENER		1	1	1
8	1409997-AA	STIFFENER PWB		1	1	1
9	1409997-AB	STIFFENER PWB		1	1	1
10						
11	1464217-01	TRANSFORMER	T1	1	1	1
12						
13	1465067-01	PROM ASSY REF: MC10139 000-004	5L	1	1	1
14	1465068-01	PROM ASSY REF: PAL16R4 590-806	6S	1	1	1
15	1465069-01	PROM ASSY REF: MC10139 000-004	8S	1	1	1
16						
17						
18	064-652	CAPACITOR, CER., .01uF, 50V, ±20%	C1-8,16,19,22,23, 26-35,37,107,108	25	25	25
19	064-653	CAPACITOR, CER., .1uF, 50V, ±20%	C9-15,17,24,36,38-42,45-54,58,60-83, 85-96,99-106,109-113, 115-131,133-142	102	102	102
20						
21	034-225	CAPACITOR, MICA, 220pF, 500V, ±1%	C44	1	1	1
22	034-918	68pF, 500V, ±1%	C57	1	1	1
23	056-603	47pF, 500V, ±.5pF	C18	1	1	1
24	056-679	CAPACITOR, MICA, 27pF, 500V, ±.5pF	C25	1	1	1
25						
26	035-729	CAPACITOR, MYLAR, .0015uF	C55	1	1	1
27	035-730	CAPACITOR, MYLAR, .0047uF	C56	1	1	1
28	055-133	CAPACITOR, MYLAR, .0022uF	C59	1	1	1
29	055-166	CAPACITOR, MYLAR, .001uF	C43	1	1	1
30						
31	037-892	CAPACITOR, TANT., 47uF, 20V	C84,98	2	2	2
32	037-965	CAPACITOR, TANT., 120uF, 10V	C114,132	2	2	2
33						
34	038-254	CAPACITOR, VARIABLE, 9-35pF	C21	1	1	1
35						
36						

LM-1464411

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1464411 SHEET 2 OF 5	REV G

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01	-02	-03
37	017-272	CRYSTAL, 40.5 MHz	Y1	1	1	1
38						
39	013-599	DIODE, CD458	CR6,7	2	-	-
40	013-723	DIODE, FD777	CR2-5	4	4	4
41	581-555	DIODE, VARACTOR, MV3103	CR1	1	1	1
42	581-567	DIODE, LED, RED	DS1	1	1	1
43	013-599	DIODE, CD458	CR6		1	1
44						
45	540-040	INDUCTOR, FIXED, .22uH	L2	1	1	1
46	541-973	INDUCTOR, FIXED, 1uH	L1	1	1	1
47						
48	000-152	INTEGRATED CIRCUIT, 10125	1M,2E,F,3E,F,4G, 5G,K,6B,K,7K,9L	12	12	12
49	000-153	10104	9S	1	1	1
50	001-076	10174	8U	1	1	1
51	001-077	10176	2A,B,C,3D,P,R,S, 4D,F,P,R,S,5B,C,D,	24	24	24
			5F,M,P,6D,L,P,7A, 7D,S			
52	002-088	10135	8G	1	1	1
53	002-933	MCM68A10P (1)	4T	1	1	1
54	002-934	DM10422J	4A,B,C,5H,J,6A,7C, 7E,F,H,J	11	11	11
55	003-026	74F138	5U	1	1	1
56	587-205	10102	2M	1	1	1
57	587-324	10106	8J	1	1	1
58	587-532	10105	8L	1	1	1
59	587-536	74LS193	2S,T	2	2	2
60	587-550	10136	4L,N,5N,6G,7G,P,R, 8M,T,9M,P,R	2	12	12
61	589-512	10173	4E,5E,6M,N,7M,N, 8N,P,R,9N	10	10	10
62	589-813	74LS00	1U	1	1	1
63	589-814	74LS04	2U	1	1	1
64	589-815	74LS08	9H	1	1	1
65	589-820	74LS74	1S,6R	2	2	2
66	589-827	74LS164	5S	1	1	1
67	589-846	74S74	6U,10H	2	2	2
68	589-850	74S163	9K,10K,L	3	3	3
69	589-920	10231	3M,4M,7L,T,U,8K	6	6	6
70	589-934	74LS221	10D	1	1	1
71	590-326	10131	8H	1	1	1
72	590-330	10115	1A,B,C,D,N,2D	6	6	6
73	590-333	74LS163	6T	1	1	1
74	590-461	74LS112	9G	1	1	1
75	590-543	10116	8B,10G	2	2	2
76	590-564	10124	1J,K,L,2K,L,N,P,R, 3L,N,5R	11	-	-
77	590-584	74LS244	1T	1	1	1
78	590-586	74LS374	1F,5T	1	1	2
79	590-602	TL082CP	8D,E	2	2	2
80	590-842	INTEGRATED CIRCUIT, 74S157	3G,H	2	2	2

LM-1464411

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM- 1464411 SHEET 3 OF 5	REV G

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01	-02	-03
81	590-847	INTEGRATED CIRCUIT, 74LS245N	1P,R	2	2	2
82	590-947	INTEGRATED CIRCUIT, 74F374	1E, ,G,H,2G,H,J, 3J,K,4H,J,K	12	12	11
83	590-564	INTEGRATED CIRCUIT, 10124	1J,K,L,2K,L,N,P,R, 3L,N,5R,10E		12	12
84						
85						
86	039-163	NETWORK RESISTOR, 470 OHMS	U12-14,17,18,20-41, 44-52,54,56-76	58	58	58
87	039-200	330 OHMS	U1,7,11	3	3	3
88	039-378	47 OHMS	U2-6,8-10,15,16,55	11	11	11
89	039-424	82 OHMS	U42	1	1	1
90	039-238	NETWORK RESISTOR, 150 OHMS	U19	1	1	1
91	570-630	POWER CONVERTER, PM671	10M	1	1	1
92						
93	041-793	RESISTOR, C.C., 10M OHMS, 1/4W, 5%	R26	1	1	1
94						
95	066-652	RESISTOR, C.F., 470K OHMS, 1/4W, 5%	R11	1	1	1
96	066-663	220	R29	1	1	1
97	066-665	1K	R8,32,64,74	4	-	-
98	066-666	2.7K	R12	1	1	1
99	066-668	4.7K	R20,61	2	-	-
100	066-673	1M	R21,27	2	2	2
101	066-689	2.2K	R47,70	2	2	2
102	066-711	7.5K	R14	1	1	1
103	066-712	22K	R17	1	1	1
104	066-717	47K	R40,41	2	2	2
105	066-812	100	R30	1	-	-
106	066-818	470	R35,63,83,84,91	5	-	-
107	066-824	1.5K	R31,92	2	-	-
108	066-825	1.6K	R62	1	-	-
109	066-826	2K	R28	1	1	1
110	066-827	3.9K	R13	1	1	1
111	066-830	10K	R9,23,42,44	4	4	4
112	066-835	82	R1,3,18,34,37,39, 54,57,66,68,72,79, 81,86,88,90,93,95,97, 99	20	-	-
113	066-837	130	R2,4,19,33,36,38, 55,56,65,69,71,80, 82,85,87,89,94,96,98, 100	20	-	-
114	066-838	330	R16,76,77	3	-	-
115	066-839	560	R15	1	1	1
116	066-840	680	R5-7,25,50,51,53, 58-60	10	10	10
117	066-849	100K	R24	1	1	1
118	066-858	4.7M	R10	1	1	1
119	066-860	39K	R73	1	1	1
120	066-866	27K	R52	1	1	1
121	066-873	20K	R43	1	1	1
122	076-012	RESISTOR, C.F., 330K OHMS, 1/4W, 5%	R22	1	1	1
123	066-665	RESISTOR, C.F., 1K OHMS, 1/4W, ±5%	R8,32,74		3	3

LM-1464411

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM- 1464411 SHEET 4 OF 5	REV G

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01	-02	-03
124						
125						
126	062-941	RESISTOR, M.F., 2.21K OHMS, 1/4W, 1%	R45,46,49	3	3	3
127	062-949	RESISTOR, M.F., 2.67K OHMS, 1/4W, 1%	R48	1	1	1
128						
129	058-388	RESISTOR, VARIABLE, 1-50K OHMS	R75	1	1	1
130						
131	014-780	TRANSISTOR, MPS6514-5	Q1-5	5	5	5
132	014-781	TRANSISTOR, MPS6518-5	Q6	1	1	1
133						
134	143-981	JACK, P.C. TIP	REF:J1-A,B,C,J2-A,B	5	5	5
135						
136	173-024	TERMINAL, TURRET	GND 1-7	7	7	7
137	187-354	TERMINAL, PUSH-IN	TP1-8	8	8	8
138						
139	302-395	STRAP, CABLE, MOUSETAIL	REF:Y1	1	1	1
140						
141	471-060	SCREW, PAN HD., XREC, #4-40 X .250 LG		6	6	6
142						
143	493-005	NUT, HEX, NYLON, LOCK, #4-40		6	6	6
144	530-477	ENCLOSURE PART, INSERTER/EXTRACTOR		2	2	2
145						
146						
147						
148	582-280	I.C., MTG. HDW., SOCKET, 24 PIN	REF:4T	1	1	1
149	582-329	8 PIN	REF:8D,E	2	2	2
150	582-330	14 PIN	REF:1S,U,2U,5S,6R,U,9H,10H	8	8	8
151	582-331	16 PIN	REF:1A,B,C,D,J,K,L,M,N, 2A,B,C,D,E,F,K,L,M, 2N,P,R,S,T,3D,E,F,G,H,L,M,N,P,R,S, 4D,E,F,G,L,M,N,P,R,S,5B,C,D,E,F,G,K, 5L,M,N,P,R,U,6B,D,G,K,L,M,N,P,T,7A, 7D,G,K,L,M,N,P,R,S,T,U,8B,G,H,J,K, 8L,M,N,P,R,S,T,U,9G,K,L,M,N,P,R,S, 10D,G,K,L	103	-	-
152	582-333	20 PIN	REF:1E,F,G,H,P,R,T,2G,H, 2J,3J,K,4H,J,K,5T,6S	17	17	17
153	582-426	I.C., MTG. HDW., SOCKET, 24 PIN	REF:4A,B,C,5H,J,6A,7C, 7E,F H,J	11	11	11
154						
155						
156						
157	602-044	SHORTING PLUG, RED	J1,2	2	2	2
158						
159	932-035	FERRITE - BEAD	REF:Q2,5 BASE	2	2	2
160						
161	066-668	RESISTOR, C.F., 4.7K OHMS, 1/4W, ±5%	R20		1	1
162	066-818	RESISTOR, C.F., 470 OHMS, 1/4W, ±5%	R35,61,62,63,83, 84,91		7	7
163						
164	066-824	RESISTOR, C.F., 1.5K OHMS, 1/4W, +5%	R31		1	1
165						

LM-1464411

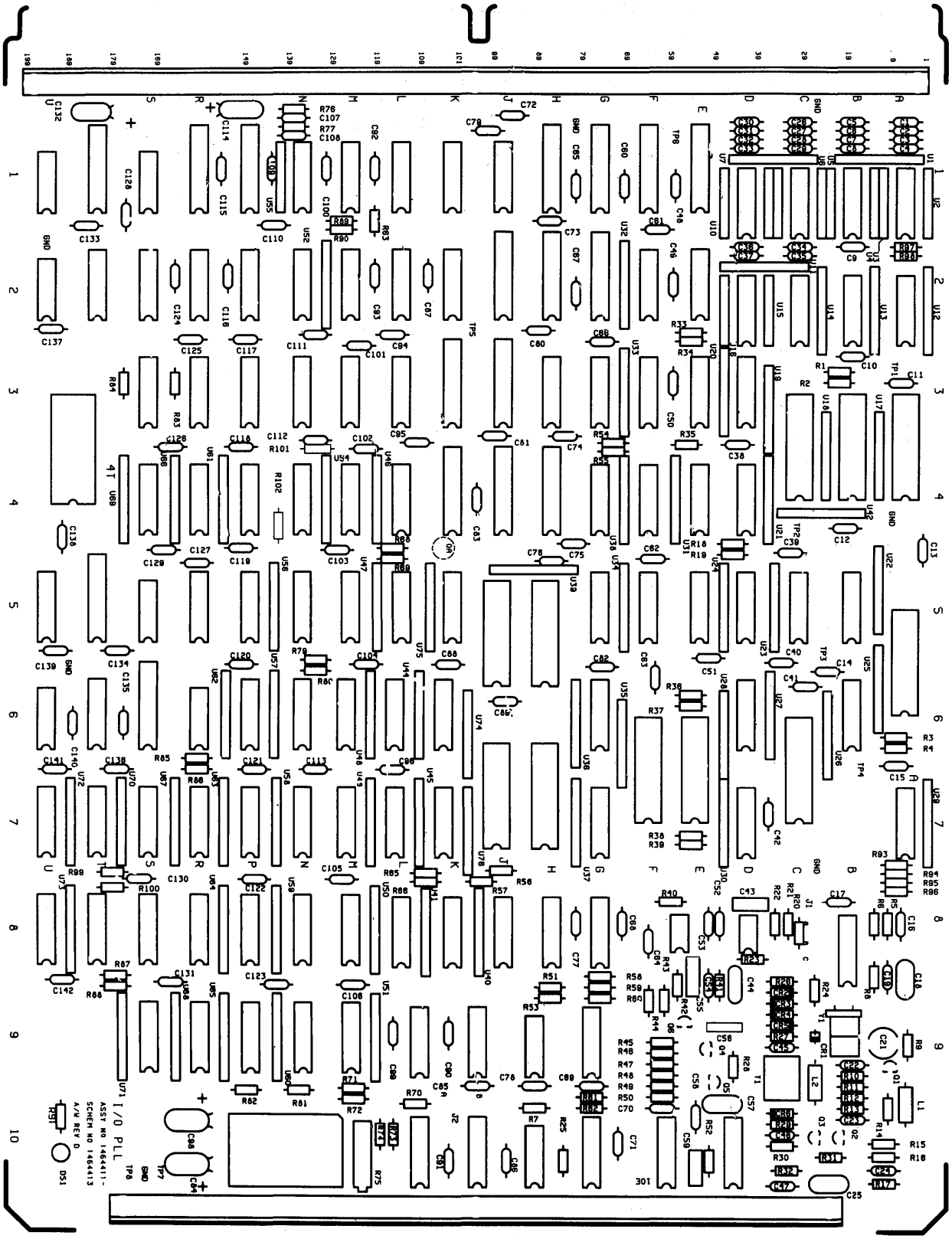
AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1464411 SHEET 5 OF 5	REV G

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -02	-03
166	582-331	I.C. MTG HDW, SOCKET, 16 PIN	REF: 1A,B,C,D,J,K,L,M,N, 2A,B,C,D,E,F,K,L,M, N,P, R,S,T,3D,E,F,G,H,L,M,N,P,R,S, 4D,E,F,G,L,M,N,P,R,S,5B,C,D,E,F,G,K, L,M,N,P,R,U,6B,D,G,K,L,M,N,P,T,7A,D, G,K,L,M,N,P,R,S,T,U,8B,G,H,J,K,L,M, N,P,R,S,T,U,9G,K,L,N,N,P,R,S,10D,E, G,K,L	104	104
167	066-835	RESISTOR, C.F., 82 OHMS, 1/4W, ±5%	R1,3,18,34,37,39,54, 57,66,68,72,79,81,86, 88,90,93,95,97,99, 101	21	21
168	066-837	RESISTOR, C.F., 130 OHMS, 1/4W, ±5%	R2,4,19,33,36,38,55, 56,65,69,71,80,82,85, 87,89,94,96,98,100, 102	21	21
169	066-812	RESISTOR, C.F., 100 OHMS, 1/4W, ±5%	R30,76,77	3	3
170	066-838	RESISTOR, C.F., 330 OHMS, 1/4W, ±5%	R16	1	1

NOTES:

1 STATIC SENSITIVE DEVICE, SPECIAL HANDLING REQUIRED PER AMPEX STD HEI-1.

LM-1464411



Assembly No. 1464411-03G. Input/Output Phase Lock Loop PWA, A1-A4

NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE 470 OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. STATIC SENSITIVE DEVICE. SPECIAL HANDLING REQUIRED PER AMPEX STANDARD HEI-1
4. ◇ = THRU 47 OHM RESISTOR NETWORK
5. ◇ = PULL DOWN RESISTOR NETWORK. PIN 1 COMMON.

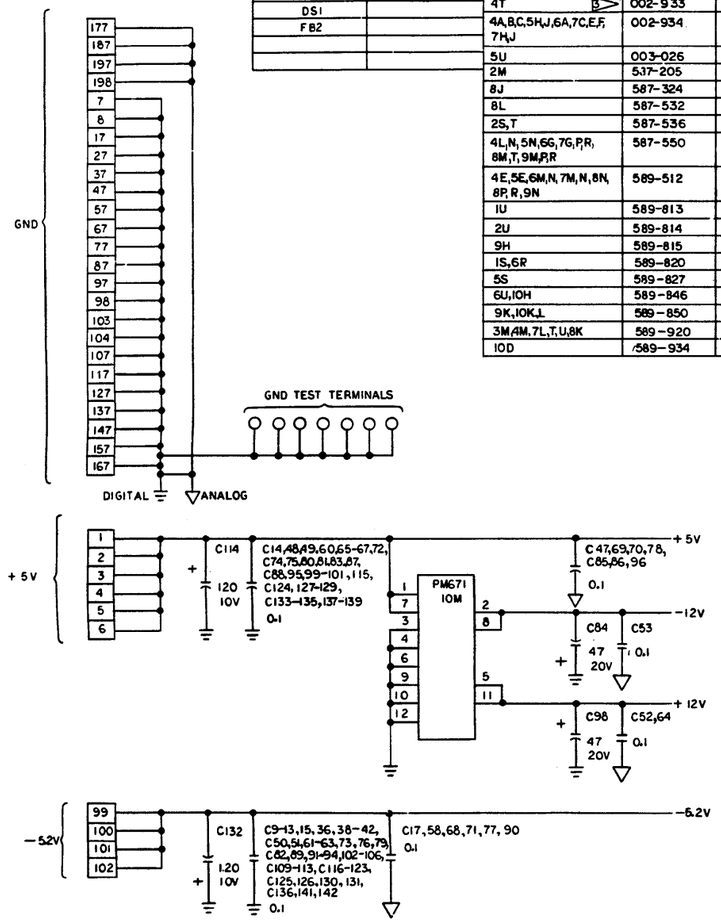
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C142	C20,97
CR6	
J2	
L2	
Q6	
R102	R64,67,78,92
TP8	
U76	U43,53
Y1	
10M	
T1	
DS1	
FB2	

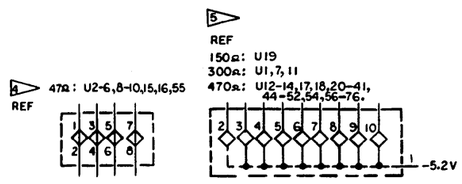
I.C. LIST

REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	GND PIN	POWER PINS -5.2V	+5V	-12V	+12V
1M,2E,F,3E,F,4G,5G,K, 6B,K,7K,9L	000-152	10125	16	8	9		
9S	000-153	10104	1,16	8			
8U	001-076	10174	1,16	8			
2A,B,C,3D,P,R,S,4D,F,P,R, 4S,5B,C,D,F,M,P, 6D,L,R 7A,D,S	001-077	10176	1,16	8			
8G	002-088	10135	1,16	8			
4T 3	002-933	MCM68A10P	1		24		
4A,B,C,5H,J,6A,7C,E,F, 7H,J	002-934	DM10422J	1,24	12			
5U	003-026	74F138	8		16		
2M	537-205	10102	1,16	8			
8J	587-324	10106	1,16	8			
8L	587-532	10105	1,16	8			
2S,T	587-536	74LS193	8		16		
4L,N,5N,6G,7G,P,R, 8M,T,9M,P,R	587-550	10136	1,16	8			
4E,5E,6M,N,7M,N,8N, 8P,R,9N	589-512	10173	16	8			
1U	589-813	74LS00	7		14		
2U	589-814	74LS04	7		14		
9H	589-815	74LS08	7		14		
1S,6R	589-820	74LS74	7		14		
5S	589-827	74LS164	7		14		
6U,10H	589-846	74S74	7		14		
9K,10K,L	589-850	74S163	8		16		
3M,4M,7L,T,U,8K	589-920	10231	1,16	8			
10D	589-934	74LS221	8		16		

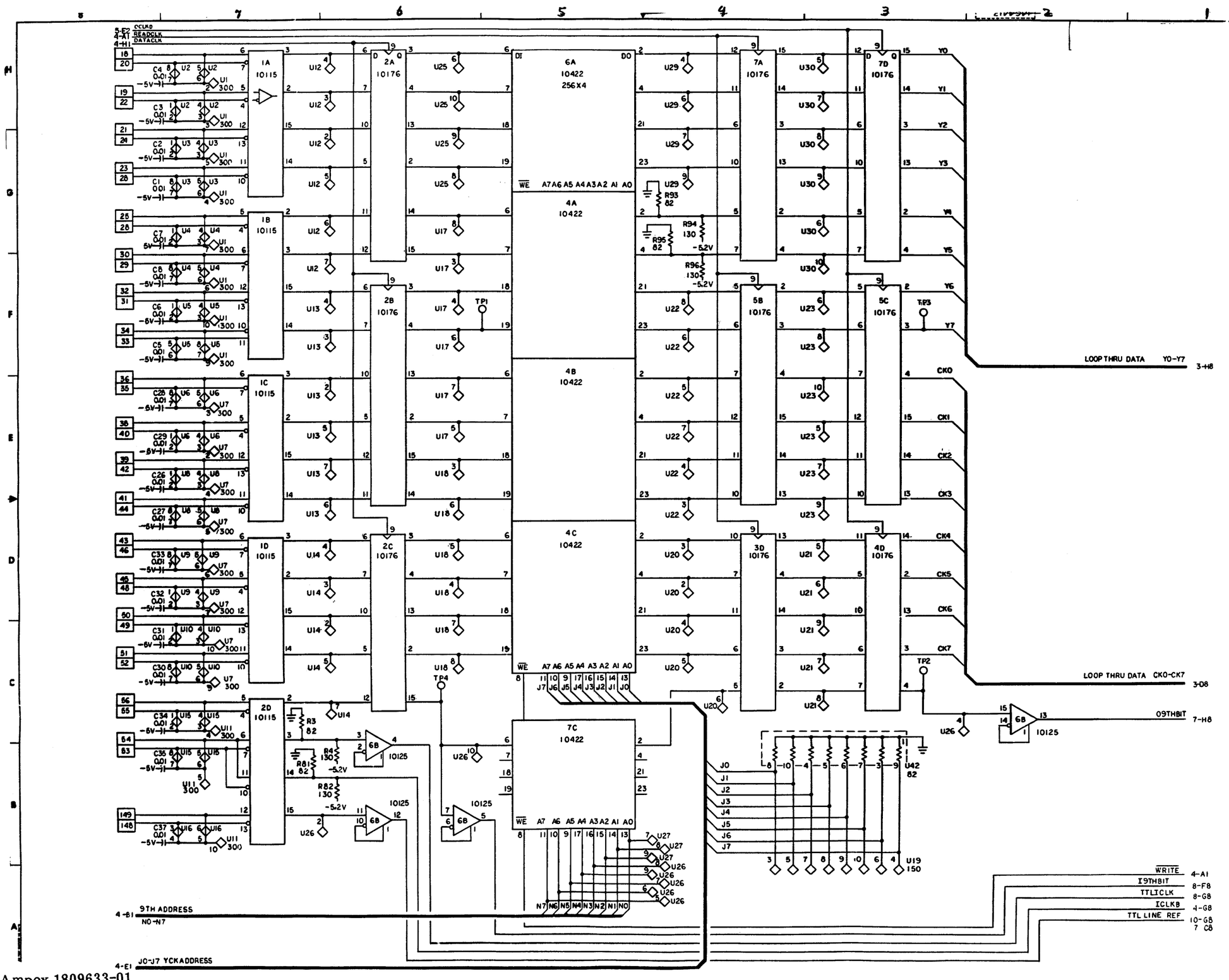
I.C. LIST

REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	GND PIN	POWER PINS -5.2V	+5V	-12V	+12V
8H	590-326	10131	1,16	8			
1A,B,C,D,N,2D	590-330	10115	1,16	8			
6T	590-333	74LS163	8		16		
9G	590-461	74LS112	8		16		
8B,10G	590-543	10116	1,16	8			
1J,K,L,2K,L,N,P R 3L,N,5R,10E	590-564	10124	16	8	9		
1T	590-584	74LS244	10		20		
5T	590-586	74LS374	10		20		
8D,E	590-602	TL082CP				4	8
3G,H	590-842	74S157	8		16		
1R,R	590-847	74LS245	10		20		
1E,F,G,H,2G,H,J,3J,K, 4H,J,K	590-947	74F374	10		20		
5L	1465067-01	MC10139	16	8			
6S	1465068-01	PAL16R4	10		20		
8S	1465069-01	MC10139	16	8			
U12-14,17,18,20-41, U44-52,54,56-76 5	039-163	470 OHMS			1		
U1,7,11 5	039-200	300			1		
U42	039-424	82	1				
U19 5	039-238	150 OHMS			1		
10M	570-630	PM671	3466, 10,12		1-5	2-8	11-15





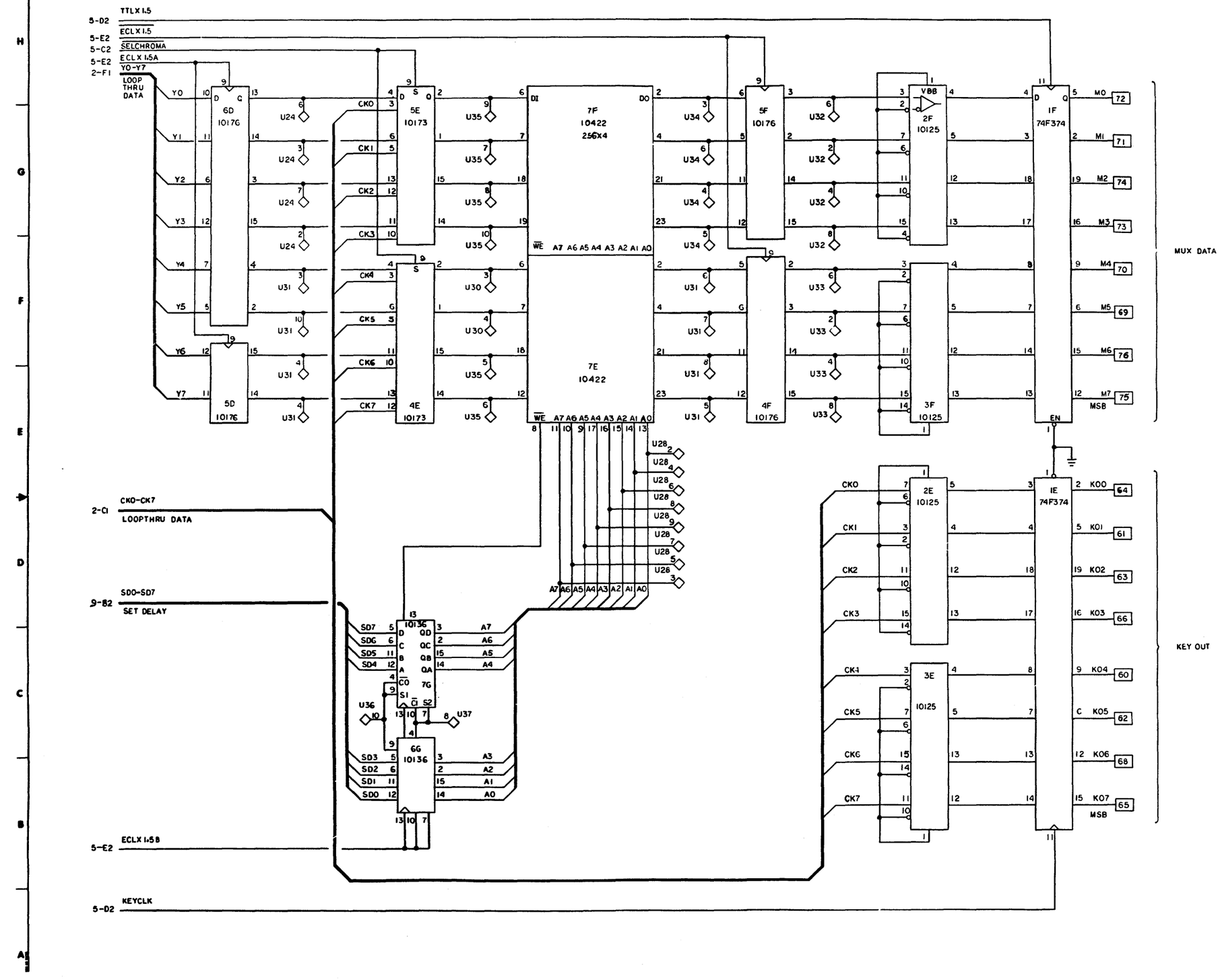
Schematic No. 1464413C.
Input/Output Phase Lock Loop PWA, A1-A4
(Sheet 1 of 11)



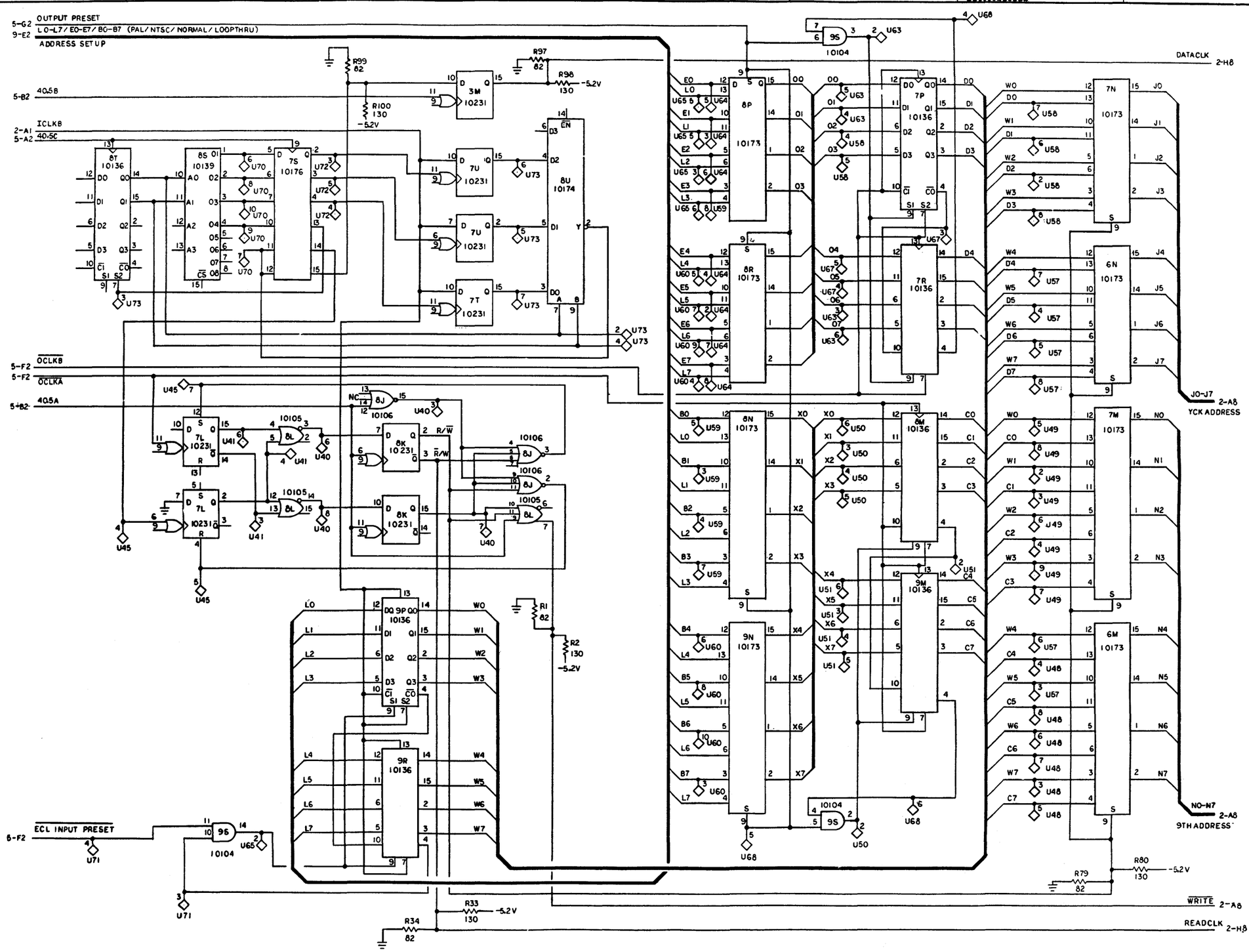
Ampex 1809633-01

Schematic No. 1464413C.
Input/Output Phase Lock Loop PWA, A1-A4
(Sheet 2 of 11)

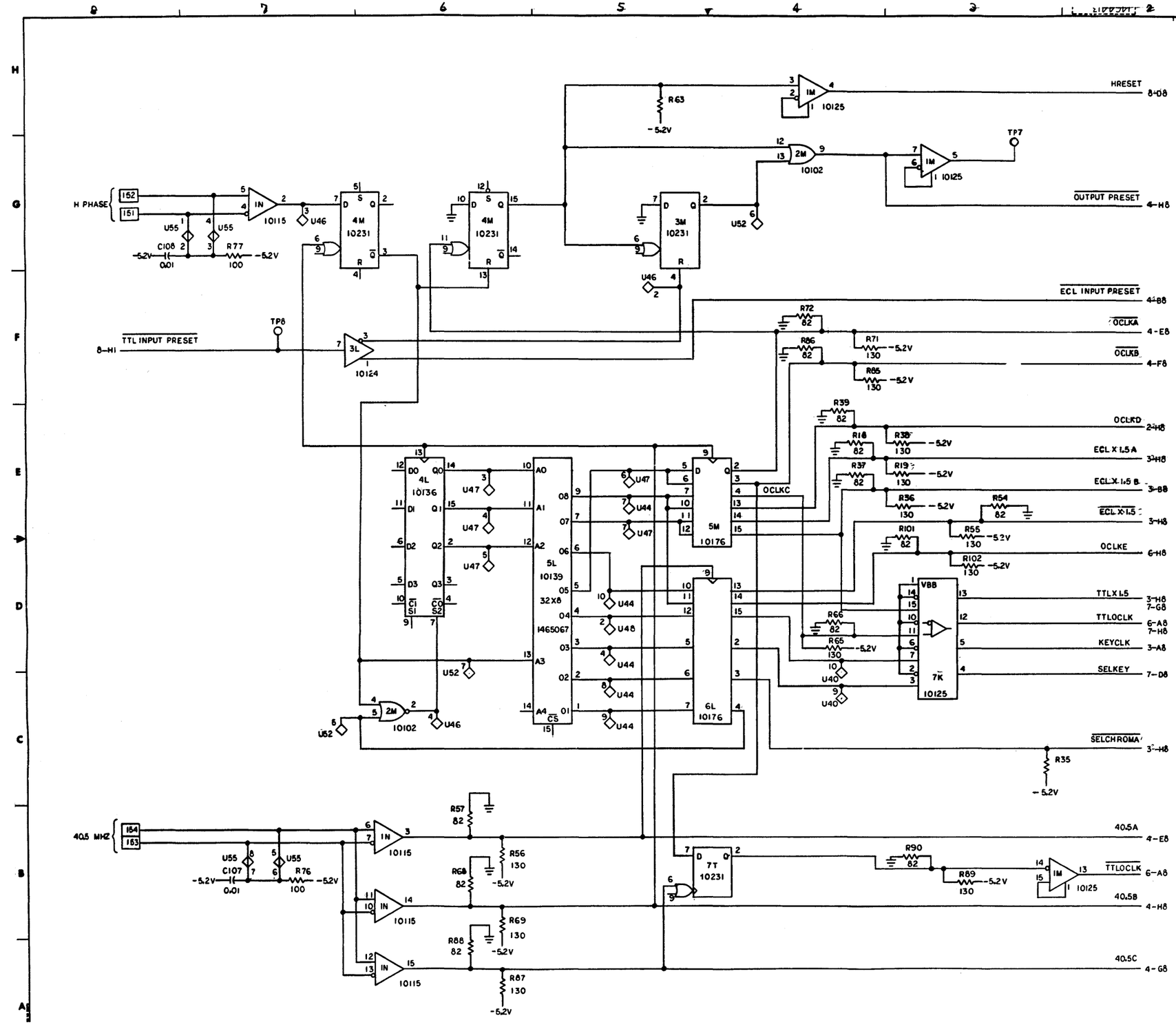
5-71/5-72



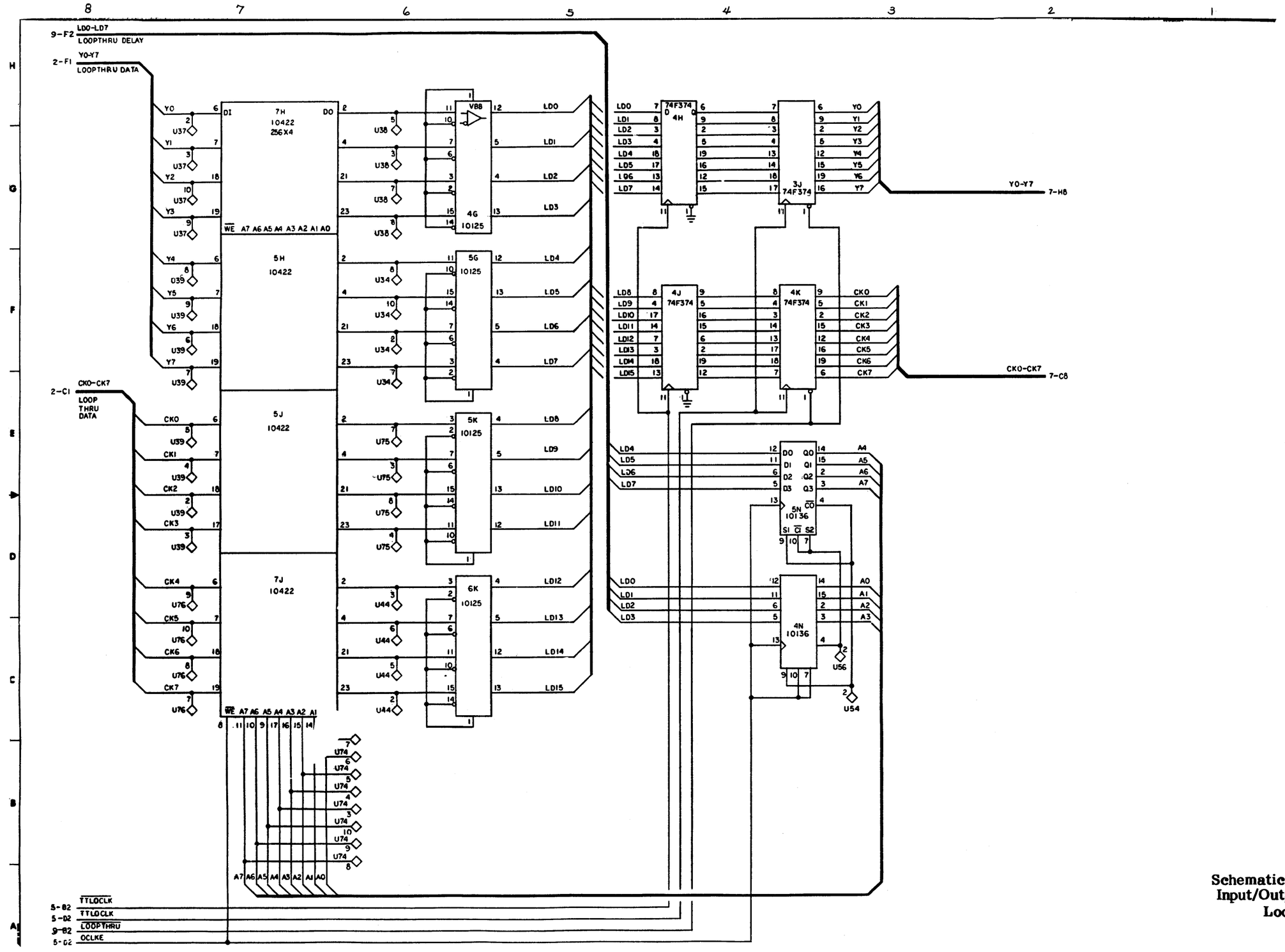
Schematic No. 1464413C.
Input/Output Phase Lock Loop PWA, A1-A4
(Sheet 3 of 11)



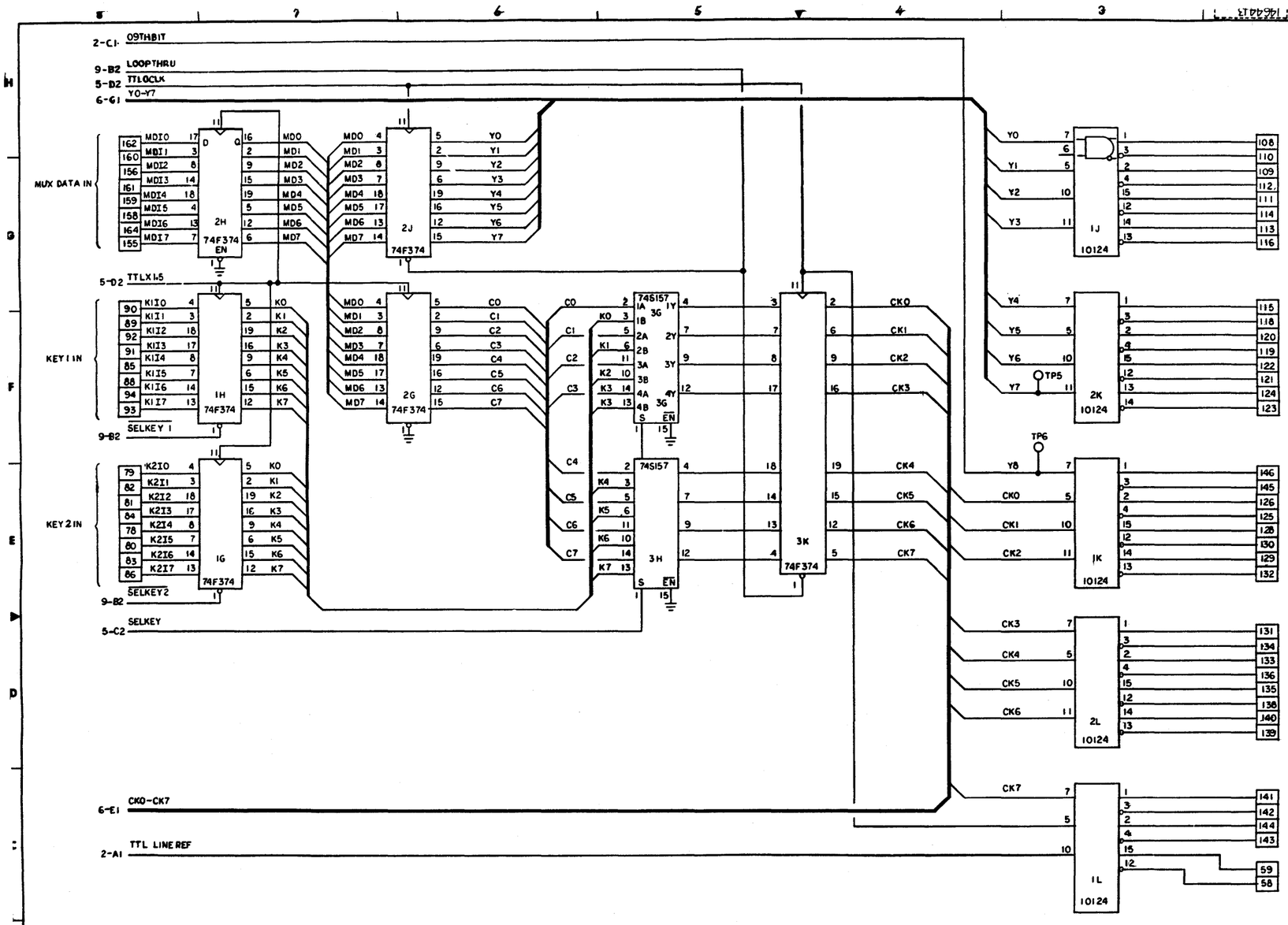
Schematic No. 1464413C.
Input/Output Phase Lock Loop PWA, A1-A4
(Sheet 4 of 11)



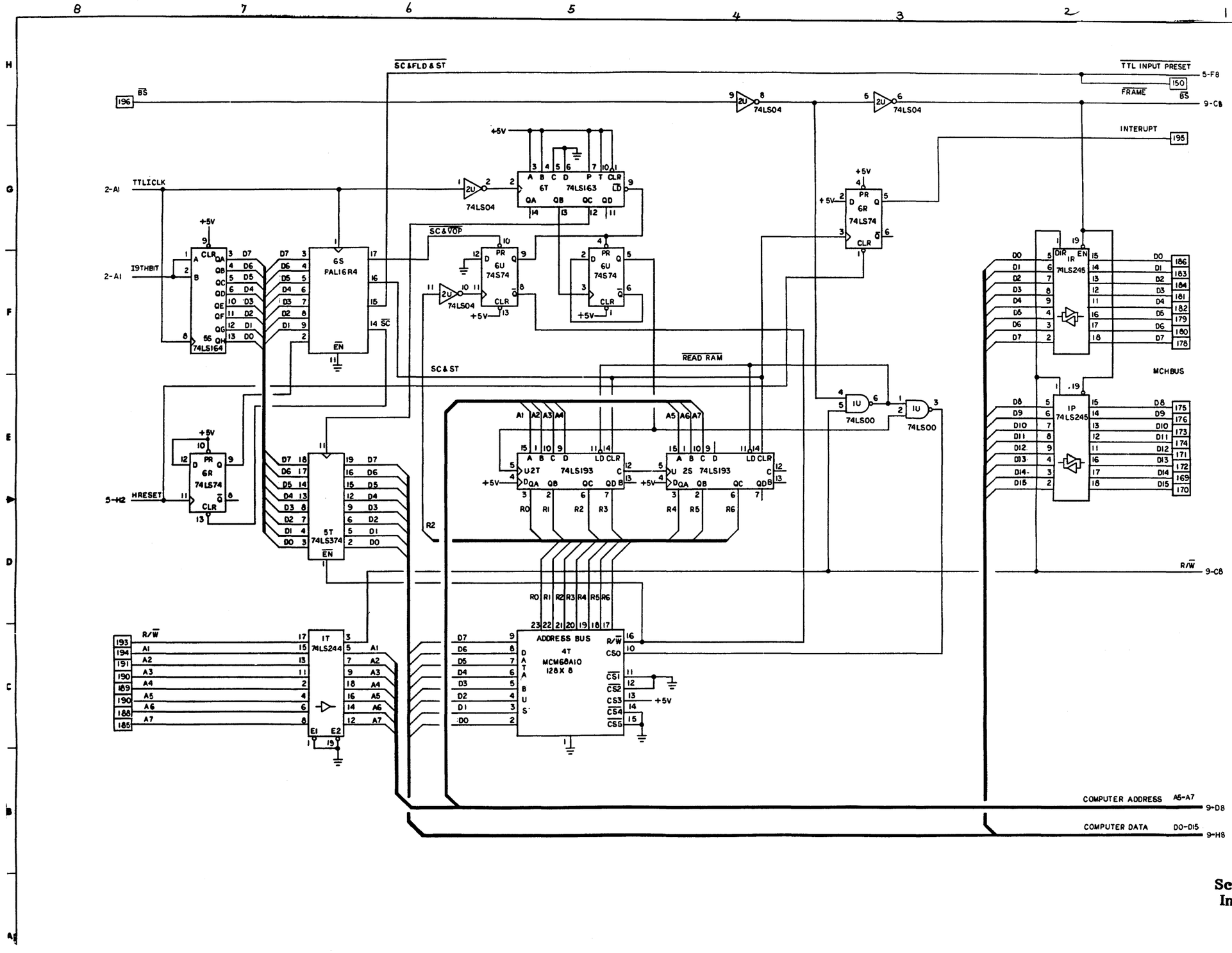
Schematic No. 1464413C.
Input/Output Phase Lock
Loop PWA, A1-A4
(Sheet 5 of 11)



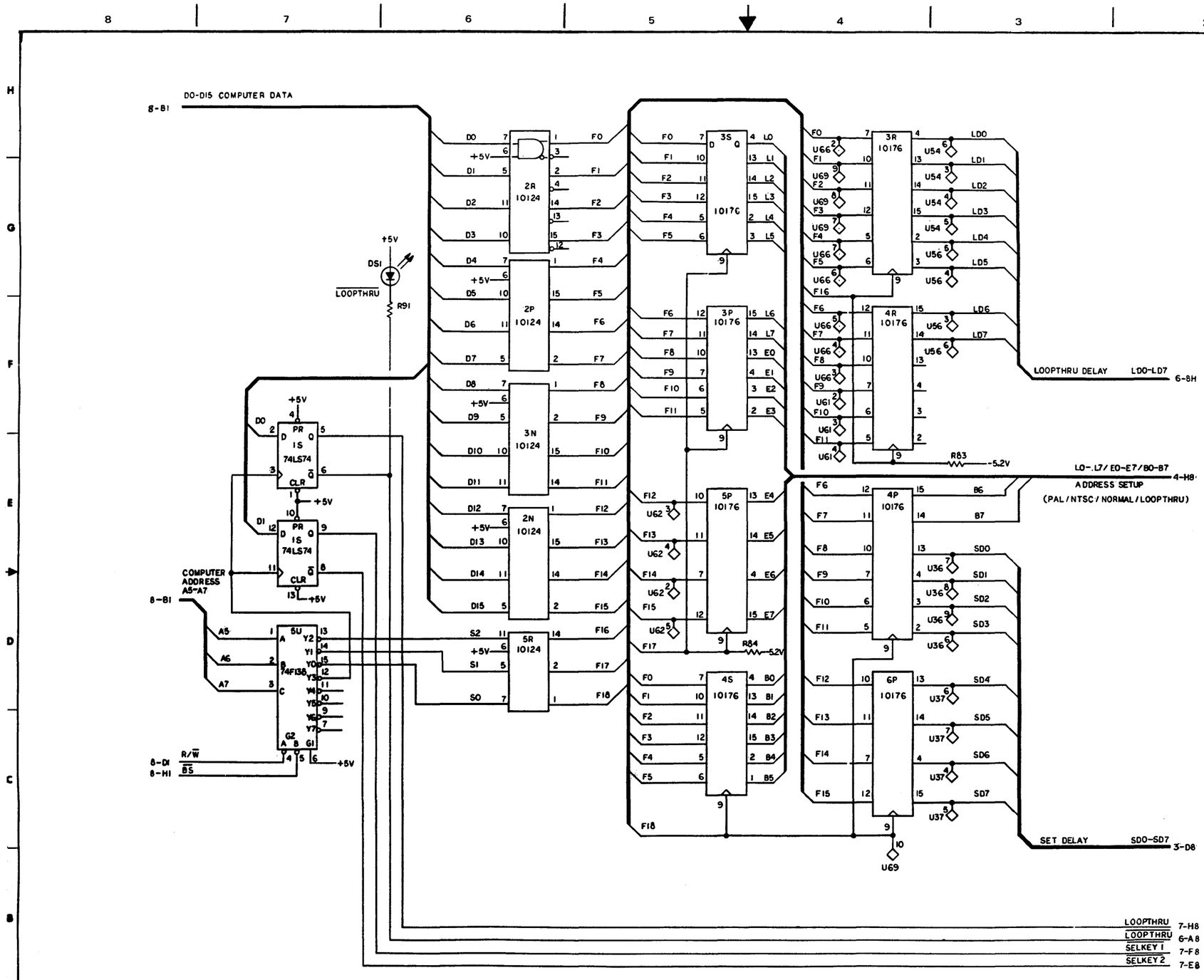
Schematic No. 1464413C.
Input/Output Phase Lock Loop PWA, A1-A4
(Sheet 6 of 11)



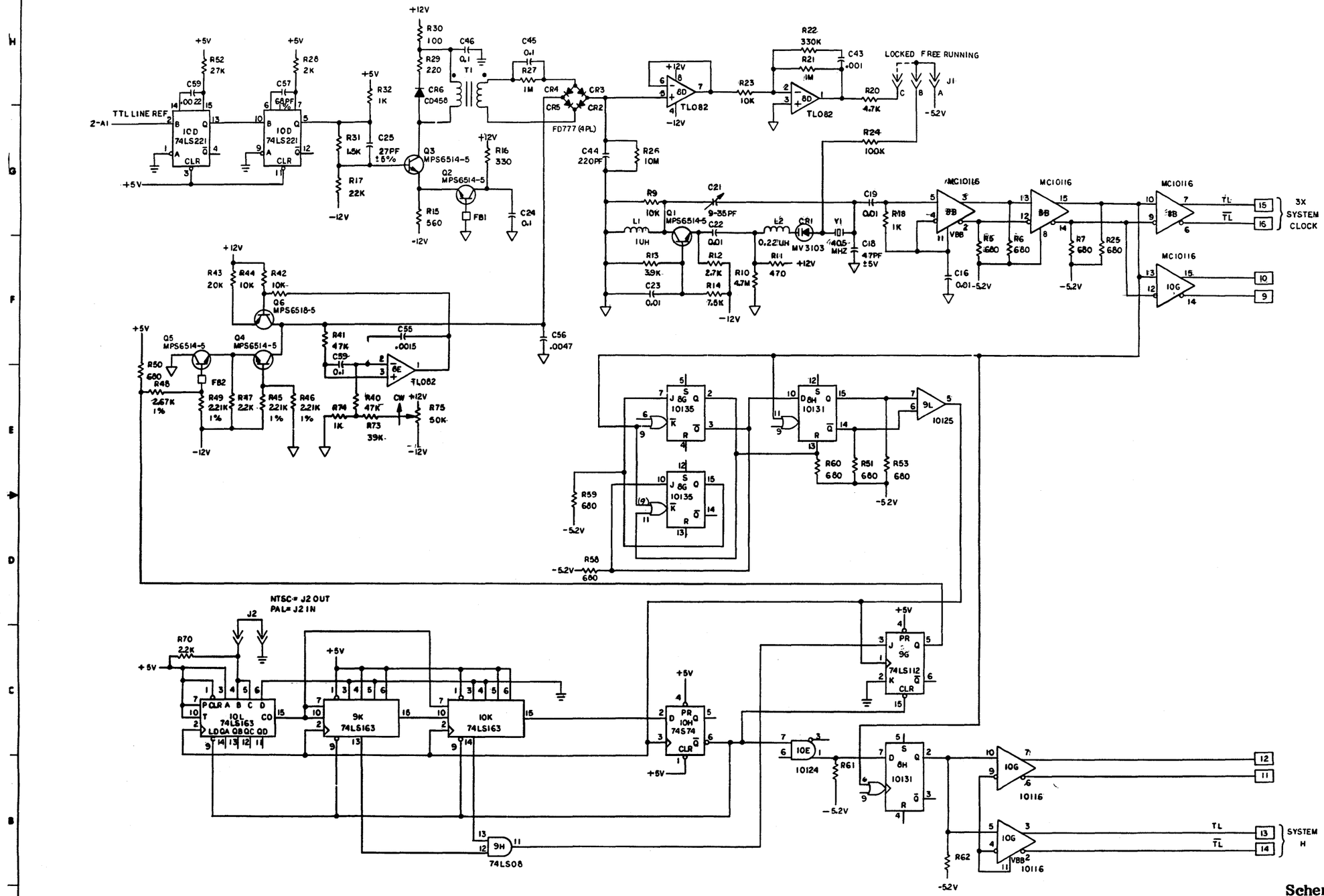
Schematic No. 1464413C.
Input/Output Phase Lock
Loop PWA, A1-A4
(Sheet 7 of 11)



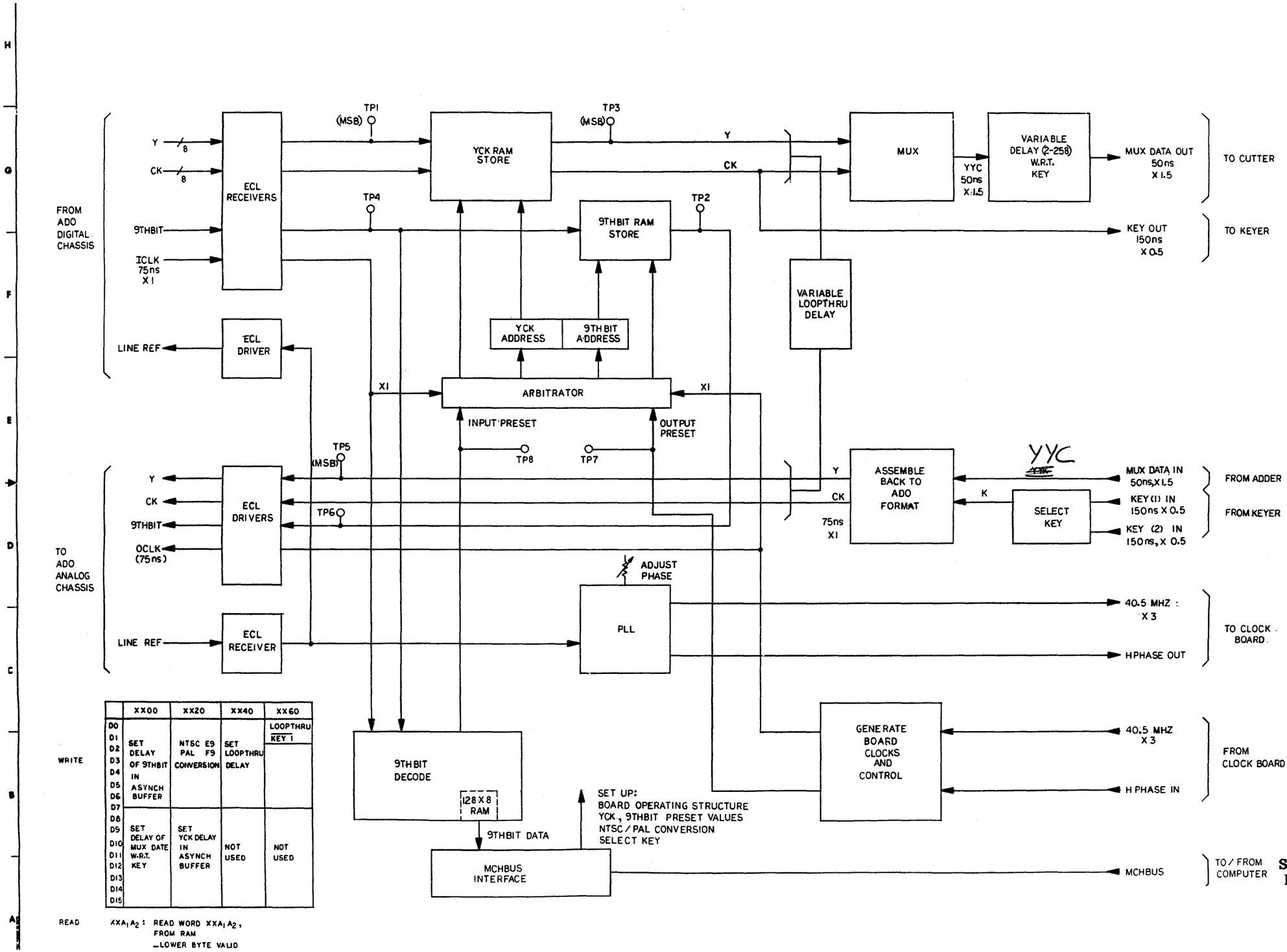
Schematic No. 1464413C.
Input/Output Phase Lock Loop PWA, A1-A4
(Sheet 8 of 11)



Schematic No. 1464413C.
Input/Output Phase Lock Loop PWA, A1-A4
(Sheet 9 of 11)



Schematic No. 1464413C.
Input/Output Phase Lock Loop PWA, A1-A4
(Sheet 10 of 11)



	XX00	XX20	XX40	XX60
D0				LOOPTHRU
D1				KEY 1
D2	SET DELAY OF 9THBIT IN ASYNCH BUFFER	NTSC E9 PAL F9 CONVERSION	SET LOOPTHRU DELAY	
D3				
D4				
D5				
D6				
D7				
D8				
D9	SET DELAY OF MUX DATE W.R.T. KEY	SET YCK DELAY IN ASYNCH BUFFER	NOT USED	NOT USED
D10				
D11				
D12				
D13				
D14				
D15				

WRITE

READ XXA_1A_2: READ WORD XXA_1A_2, FROM RAM —LOWER BYTE VALID

Schematic No. 1464413C.
Input/Output Phase Lock Loop PWA, A1-A4
(Sheet 11 of 11)

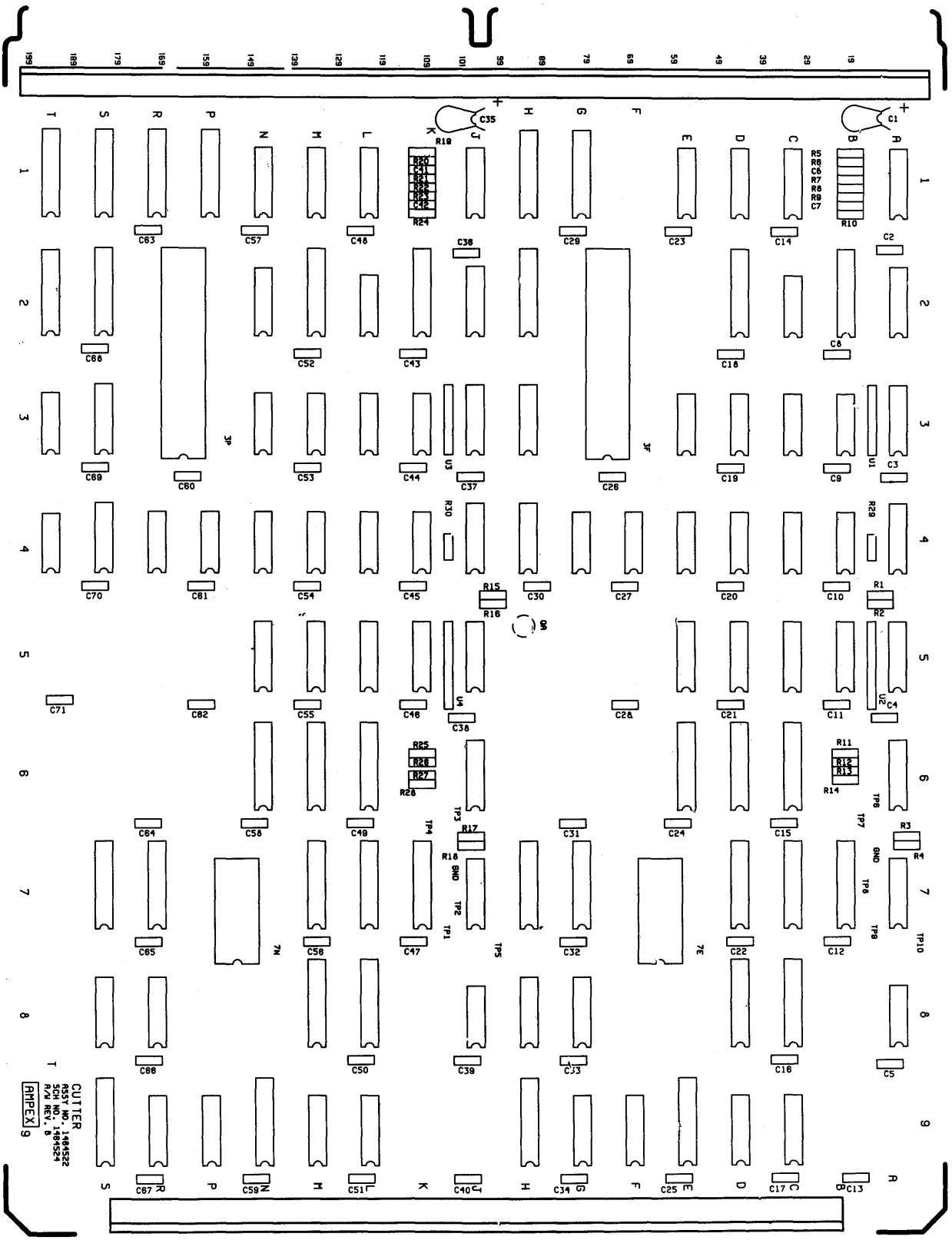
ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1				
2				
3	1464524	SCHEMATIC	(A)	
4				
5	1409670-BY	LABEL, EXTRACTOR ARM, PWA		1
6	1409976-AA	INSULATOR, STIFFENER		1
7	1409976-AB	INSULATOR, STIFFENER		1
8	1409997-AA	STIFFENER, PWB		1
9	1409997-AB	STIFFENER, PWB		1
10				
11	1464639-01	PROM ASSEMBLY REF: 000-004 10139	3A,J	2
12	1464640-01	REF: 589-940 TBP28S42	7C,L	2
13	1464641-01	REF: 589-940 TBP28S42	7D,M	2
14	1464642-01	REF: 000-038 87S181	7E,N	2
15	1464643-01	PROM ASSEMBLY REF: 002-968 PAL16R8	7B,K	2
16	1465086-01	PROM ASSEMBLY REF: 003-039 PAL14H4	2D,M	2
17				
18	064-652	CAPACITOR, CER., .01uF, 50V, 20%	C6,7,41,42	4
19	064-653	CAPACITOR, CER., .1uF, 50V, 20%	C2-5,8-34,36-40, 43-71	65
20				
21	037-965	CAPACITOR, TANT., 120uF, 10V, 20%	C1,35	2
22				
23	000-128	INTEGRATED CIRCUIT, 74S283	3H,S,4H,S,9C,D,F, 9G,L,M,P,R	12
24	000-151	10136	2A,J	2
25	002-168	MPY112K	3F,P	2
26	589-713	10176	4A,J,5A,J	4
27	589-823	74LS138	2N	1
28	589-824	74LS153	5B,C,D,E,K,L,M,N	8
29	589-827	74LS164	3B,C,D,E,K,L,M,N, 4B,C,D,E,K,L,M,N	16
30	589-838	74S04	4F,P,T,8A,J	5
31	589-846	74S74	4G,R	2
32	589-850	74S163	1E,N	2
33	590-221	AM27S07	1C,D,L,M	4
34	590-335	74LS273	1S,T	2
35	590-443	74S02	2C,L	2
36	590-464	10125	6A,J,7A,J	4
37	590-543	INTEGRATED CIRCUIT, 10116	1A,J	2

LM-1464522

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA | CODE IDENT NO. 92739 | LIST OF MATERIALS | LM- 1464522 SHEET 2 OF 2 | REV A

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
38	590-584	INTEGRATED CIRCUIT, 74LS244	2B,K	2
39	590-842	74S157	8G,H,R,S	4
40	590-855	74S374	1G,H,P,R,2H,S,6C, 6D,E,L,M,N,7G,H,R, 7S,8C,D,L,M,9E,H, 9N,S	24
41	589-935	74LS393	3T	1
42	589-751	INTEGRATED CIRCUIT, 74LS241	2T	1
43				
44	039-163	RESISTOR, NETWORK, 470 OHMS, 10 PIN SIP	U2,4	2
45	039-329	RESISTOR, NETWORK, 470 OHMS, 8 PIN SIP	U1,3	2
46				
47	066-811	RESISTOR, C.F., 51 OHMS, 1/4W, 5%	R5,7,8,10,19,21, 22,24	8
48	066-835	82	R2,3,12,14,16, 17,26,28	8
49	066-837	130	R1,4,11,13,15, 18,25,27	8
50	066-838	330	R6,9,20,23	4
51	066-818	RESISTOR, C.F., 470 OHMS, 1/4W, 5%	R29,30	2
52				
53	173-024	TERMINAL, TURRET, SWAGE	GND	2
54	187-354	TERMINAL, TEST POINT	TP1-10	10
55				
56	582-280	I.C. MTG HDW., SOCKET, 24 PIN	REF:7E,N	2
57	582-330	I.C. MTG HDW., SOCKET, 14 PIN	REF:2C,L,3B,C,D,E,K, 3L,M,N,T,4B,C,D, 4E,F,G,K,L,M,N,P,R,T, 8A,J	26
58	582-331	I.C. MTG HDW., SOCKET, 16 PIN	REF:1A,C,D,E,J,L,M,N,2A, 2J,N,3A,H,J,S,4A,H, 4J,S,5A,B,C,D,E,J,K,L,M,N,6A, 6J,7A,J,8G,H,R,S,9C,D,F,G,L, 9M,P,R	45
59	582-333	I.C. MTG HDW., SOCKET, 20 PIN	REF:1H,G,P,R,S,T,2B,D,H, 2K,M,S,T,6C,D,E,L,M, 6N,7B,C,D,G,H,K,L,M,R,S, 8C,D,L,M,9E,H,N,S	37
60	582-397	I.C. MTG HDW., SOCKET, 48 PIN	REF:3F,P	2
61				
62				
63	471-060	SCREW, PAN HD., X-REC, #4-40 X .250 LG		6
64	493-005	NUT, HEX, NYLON LOCK, #4-40		6
65				
66	530-477	ENCLOSURE PART, CARD INSERTER/EXTRACTOR		2

LM-1464522



Assembly No. 1464522-01A. Cutter PWA, A5-A7

NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. SCHEMATIC REFLECTS PWA 1464522-01.

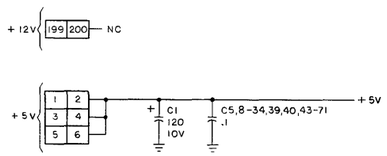
REFERENCE DESIGNATION	
LAST USED	NOT USED
C71 R30 TP10 U4	

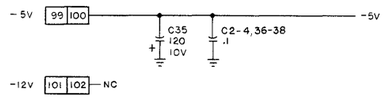
I.C. LIST

VENDOR P/N	AMPEX P/N	REFERENCE DES	GND PIN	POWER PINS +5V	POWER PINS -5V		
74S02	590-443	2C,L	7	14			
74S04	589-838	4F,P,T, 8A,J	7	14			
74S74	589-846	4G,R	7	14			
74LS138	589-823	2N	8	16			
74LS153	589-824	5B,C,D,E,K,L,M,N	8	16			
74S157	590-842	8G,H,R,S	8	16			
74S163	589-850	1E,N	8	16			
74LS164	589-827	3B,C,D,E,K,L,M,N 4B,C,D,E,K,L,M,N	8	16			
74LS244	590-584	2B,K,T	10	20			
74LS273	590-335	1S,T	10	20			
74S283	000-128	3H,S,4H,S,9C,D,F,G,L,M,P,R	8	16			
74S374	590-855	1G,H,P,R, 2H,S, 6C,D,E,J,M,N, 7G,H,R,S, 8C,D,L,M, 9E,H,N,S	10	20			
74LS393	589-935	3T	7	14			

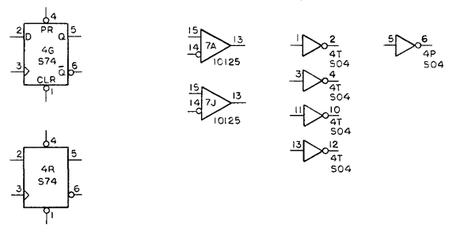
I.C. LIST

VENDOR P/N	AMPEX P/N	REFERENCE DES	GND PIN	POWER PINS +5V	POWER PINS -5V		
AM27S07	590-221	1C,D,L,M	8	16			
MC10116	590-543	1A,J	1,16		8		
MC10125	590-464	6A,J, 7A,J	16	9	8		
MC10136	000-151	2A,J	1,16		8		
MC10176	589-713	4A,J, 5A,J	1,16		8		
MPY112K	002-168	3F,P	36,37	12,13			
MCM10139	1464639-01	3A,J	16		8		
TBP28S42	1464640-01	7C,L	10	20			
TBP28S42	1464641-01	7D,M	10	20			
DM87S181	1464642-01	7E,N	12	24			
PAL 16R8	1464643-01	7B,K	10	20			
PAL 14H4	1465086-01	2D,M	10	20			



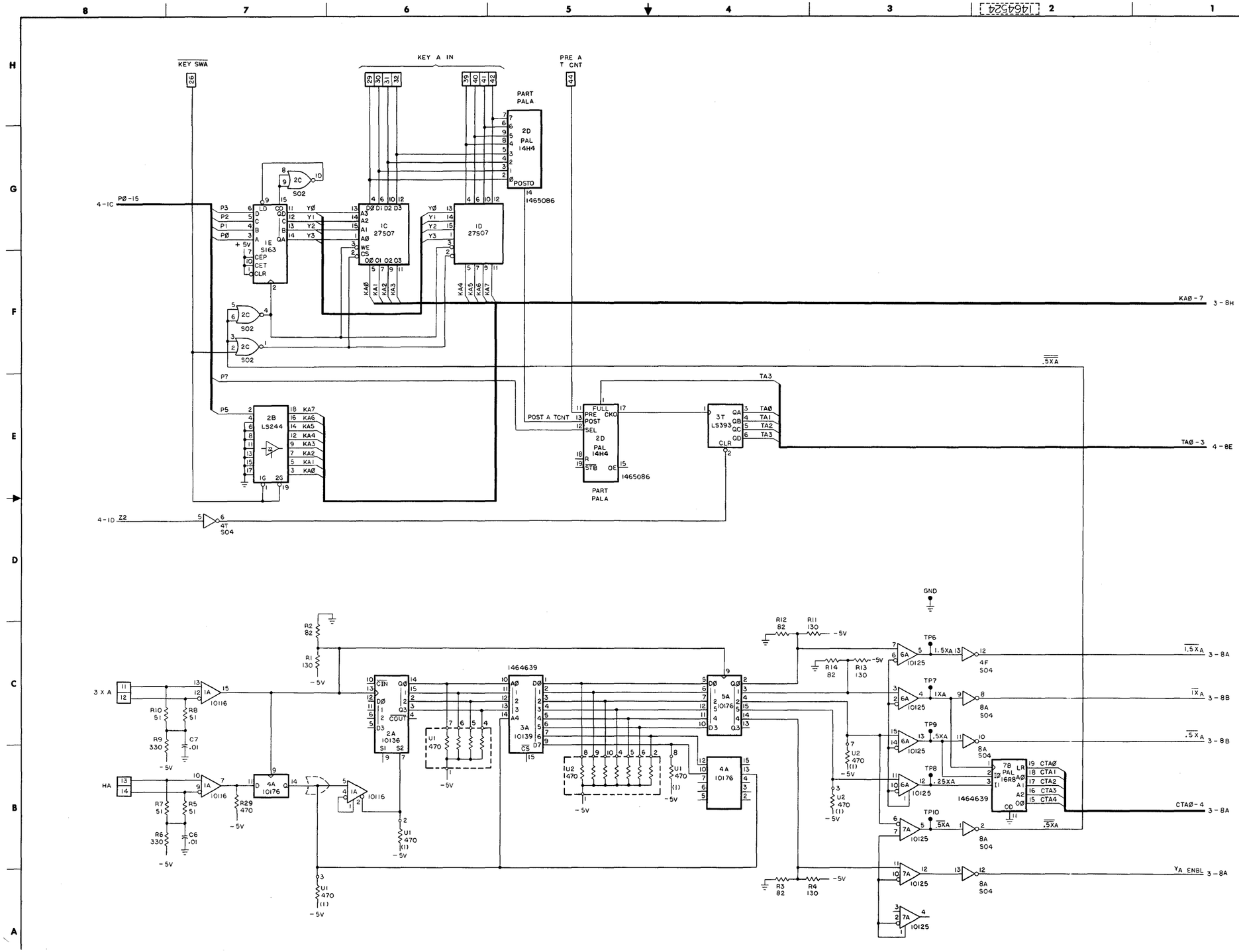


SPARES

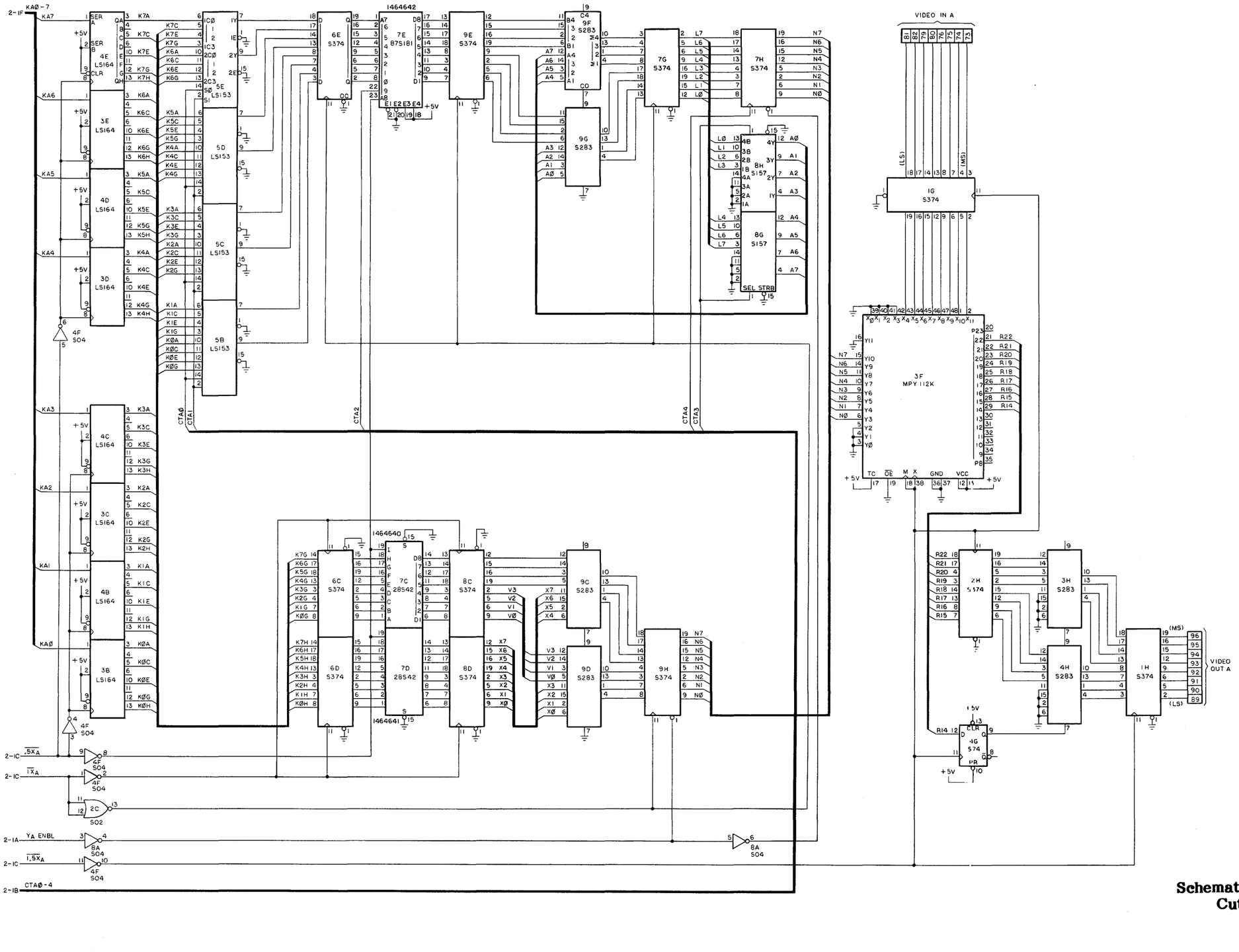


1464522	CONC
NEXT ASSY	USED ON
APPLICATION	

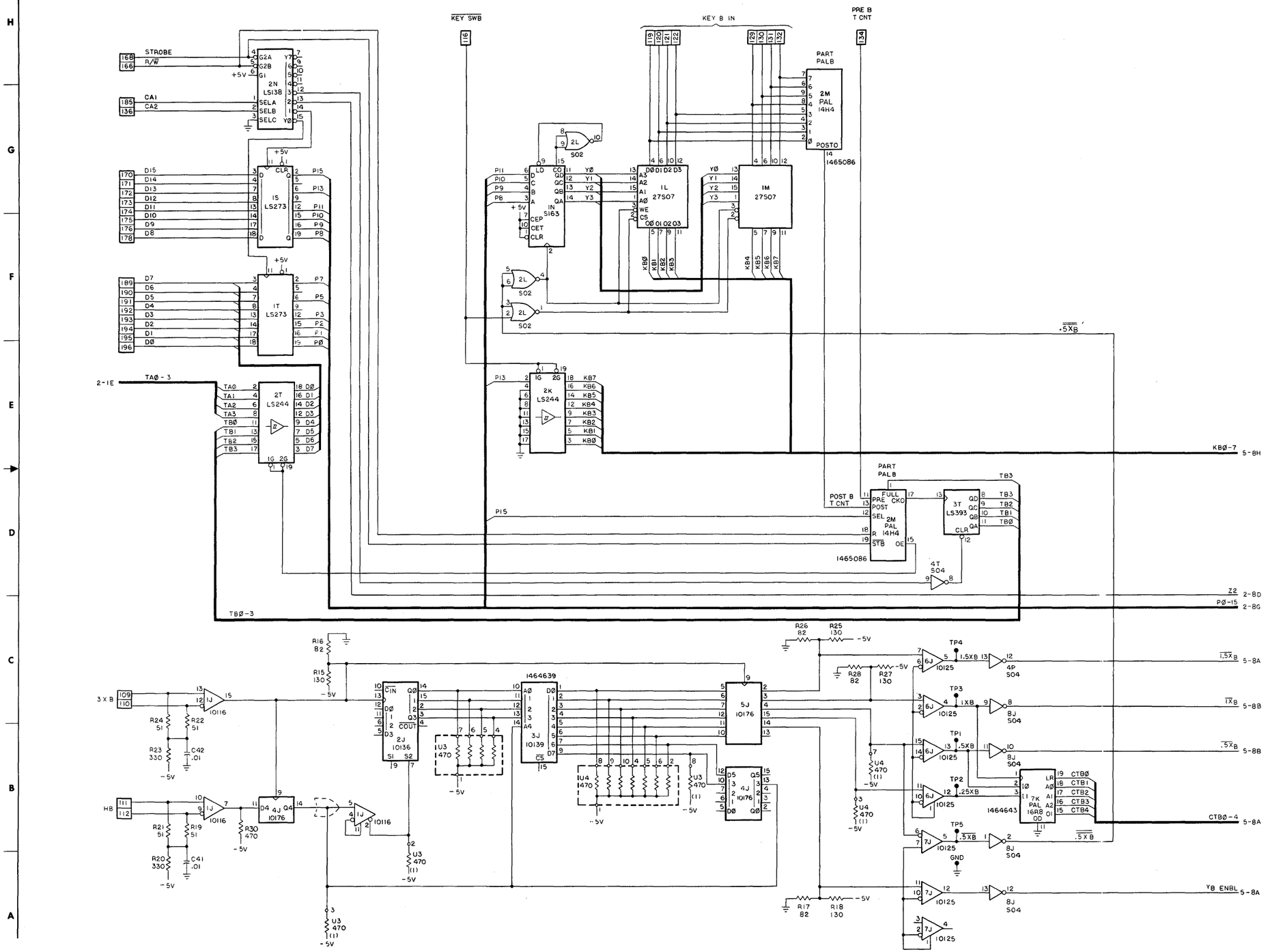
Schematic No. 1464524B.
Cutter PWA, A5-A7
(Sheet 1 of 5)



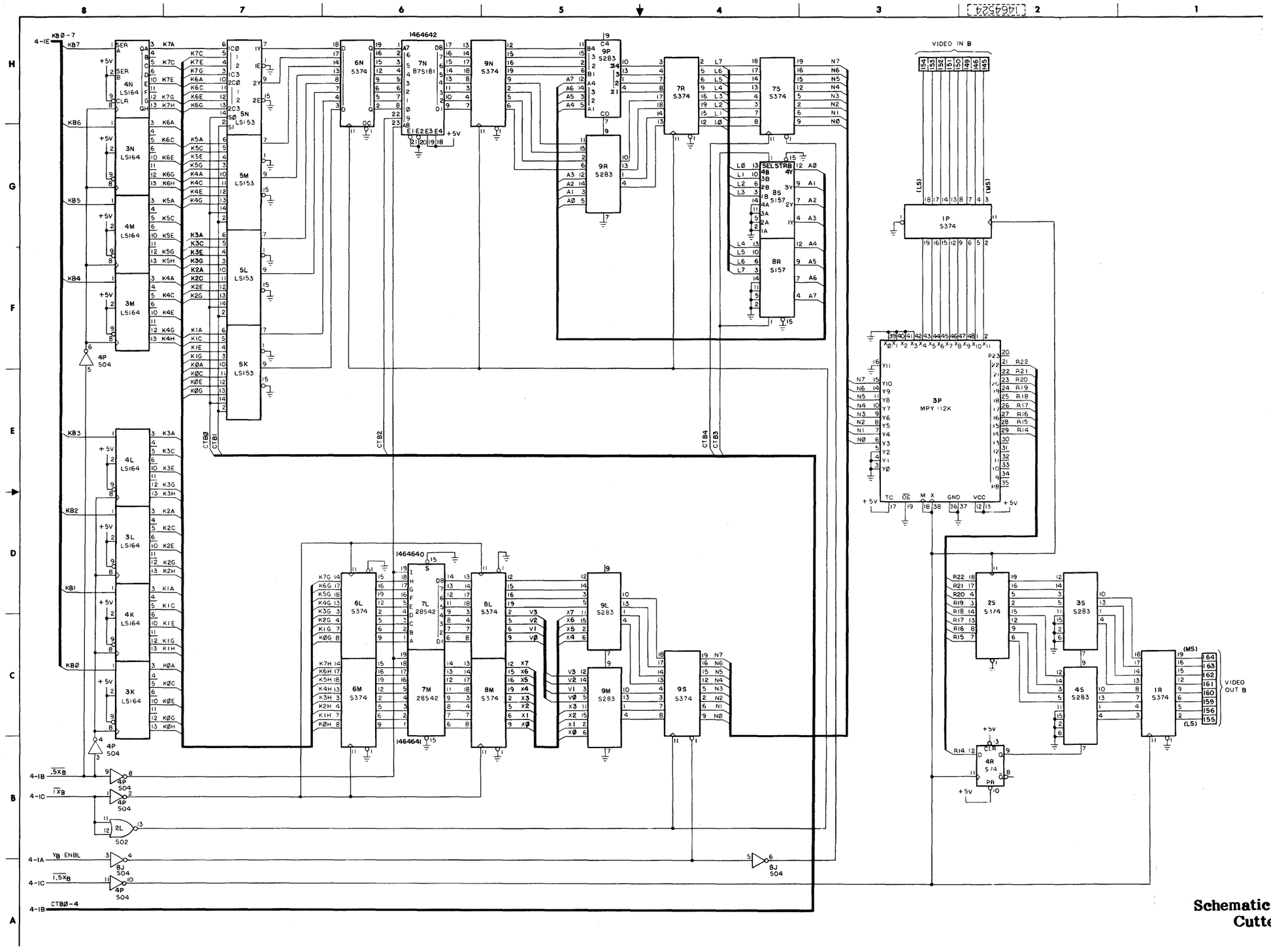
Schematic No. 1464524B.
Cutter PWA, A5-A7
(Sheet 2 of 5)



Schematic No. 1464524B.
Cutter PWA, A5-A7
(Sheet 3 of 5)



Schematic No. 1464524B.
Cutter PWA, A5-A7
(Sheet 4 of 5)



Schematic No. 1464524B.
Cutter PWA, A5-A7
(Sheet 5 of 5)

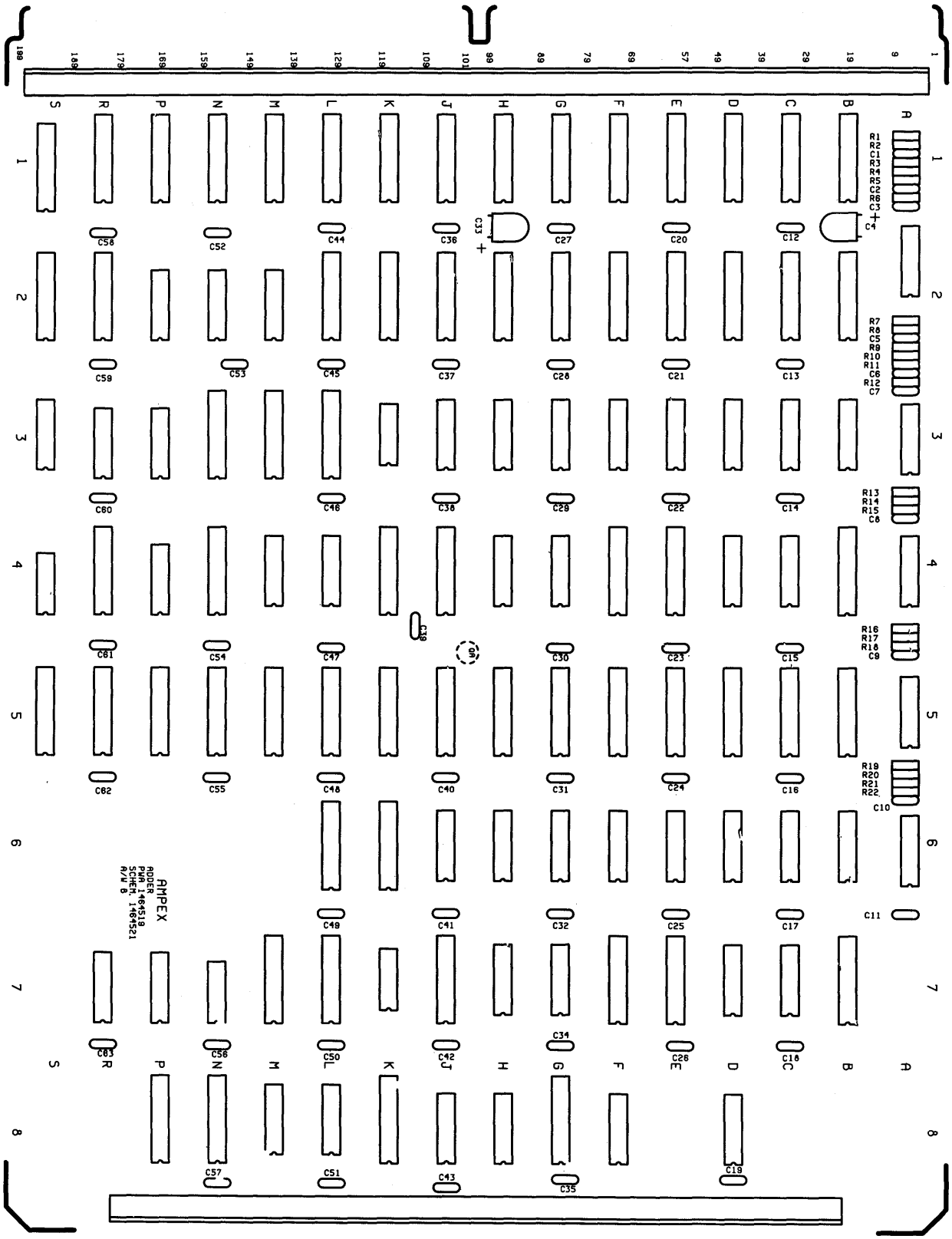
ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1				
2				
3	1464521	SCHEMATIC	(-)	
4				
5	1409670-BW	LABEL, EXTRACTOR ARM, PWA		1
6	1409976-AA	INSULATOR, STIFFENER		1
7	1409976-AB	INSULATOR, STIFFENER		1
8	1409997-AA	STIFFENER		1
9	1409997-AB	STIFFENER		1
10				
11				
12	064-652	CAPACITOR, CER., .01uF, 50V, 20%	C1,2,5,6	4
13	064-653	CAPACITOR, CER., 0.1uF, 50V, 20%	C3,7-32,34-63	57
14				
15	037-965	CAPACITOR, TANT., 120uF, 10V, 20%	C4,33	2
16				
17	002-181	INTEGRATED CIRCUIT, 74F283	2M,N,P,3B,C,D,E,F,G,H,J,4C,D,G,H,L,4M,P,6B,C,D,E,F,G,H,J,7C,D,7G,H,8D,F,H,J,L,M	36
18	589-713	10176	4A,5A	2
19	589-823	74LS138	3S	1
20	589-838	74S04	3K,7K	2
21	589-847	74S86	4S,7N	2
22	590-227	AM25S09	3P,R,7P,R	4
23	590-335	74LS273	2R,S,5R,S	4
24	590-464	10125	6A	1
25	590-543	10116	2A,3A	2
26	590-584	74LS244	1R,S	2
27	590-855	74S374	1K,L,M,N,P,2K,3L,3N,4B,E,F,J,K,N,4R,5K,L,M,N,P,6K,7B,E,F,7J,L,8G,K,N,P	30
28	590-868	74S244	1B,C,D,E,F,G,H,J,2L,3M,6L,7M	12
29	590-917	INTEGRATED CIRCUIT, 74S273	2B,C,D,E,F,G,H,J,5B,C,D,E,F,G,H,J	16
30				
31				
32				
33	066-811	RESISTOR, C.F., 51 OHMS, 1/4W, 5%	R1,2,4,5,7,8,10,11	8
34	066-818	RESISTOR, C.F., 470 OHMS, 1/4W, 5%	R13,16	2
35	066-835	RESISTOR, C.F., 82 OHMS, 1/4W, 5%	R15,18,19,21	4

LM-1464519

AMPEX	Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1464519 SHEET 2 OF 2	REV —

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
36	066-837	RESISTOR, C.F., 130 OHMS, 1/4W, 5%	R14,17,20,22	4
37	066-838	RESISTOR, C.F., 330 OHMS, 1/4W, 5%	R3,6,9,12	4
38				
39				
40	582-330	I.C. MTG HDW., SOCKET, 14 PIN	REF:3K,4S,7K,N	4
41	582-331	I.C. MTG HDW., SOCKET, 16 PIN	REF:2A,M,N,P,3A,B,C,D, 3E,F,G,H,J,S,P,R, 4A,C,D,G,H,L,M,P,5A,6A,B,C, 6D,E,F,G,H,J,7C,D,G,H,P,R,8D, 8F,H,J,L,M	46
42	582-333	I.C. MTG HDW., SOCKET, 20 PIN	REF:1B,C,D,E,F,G,H,J,K, 1L,M,N,P,R,S,2B,C, 2D,E,F,G,H,J,K,L,R,S,3L,M,N, 4B,E,F,J,K,N,R,5B,C,D,E,F,G, 5H,J,K,L,M,N,P,R,S,6K,L,7B, 7E,F,J,L,M,8G,K,N,P	64
43				
44				
45	471-060	SCREW, PAN HD., X-REC, #4-40 X .250 LG		6
46	493-005	NUT, HEX, NYLON LOCK, #4-40		6
47				
48	530-477	ENCLOSURE PART, CARD INSERTER/EXTRACTOR		2

LM-1464519



Assembly No. 1464519-01—. Adder PWA, A8

NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS. 1/4W. 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. SCHEMATIC REFLECTS PWA 1464519-01.

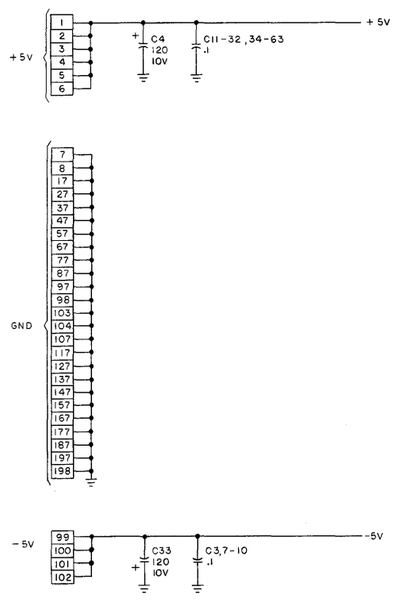
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C63	
R22	

I.C. LIST

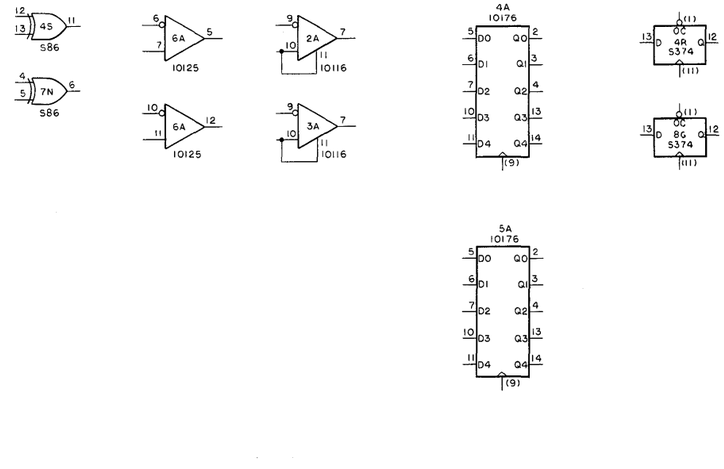
REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	GND PIN	POWER PINS +5V	POWER PINS -5V
3K,7K	589-838	74S04	7	14	
4S,7N	589-847	74S86	7	14	
3S	589-823	74LS138	8	16	
1R,S	590-584	74LS244	10	20	
1B,C,D,E,F,G,H,J,2L,3M,6L,7M	590-868	74S244	10	20	
2R,S,5R,S	590-335	74LS273	10	20	
2B,C,D,E,F,G,H,J 5B,C,D,E,F,G,H,J	590-917	74S273	10	20	
2M,N,P, 3,B,C,D,E,F,G,H,J, 4C,D,G,H,L,M,P, 6B,C,D,E,F,G,H, 6J, 7C,D,G,H, 8D,F,H,J,L,M	002-181	74F283	8	16	
1K,L,M,N,P, 2K,3L,N, 4B,E,F,J, 4K,N,R, 5K,L,M,N,P, 6K,7B, 7E,F,J,L, 8G,K,N,P	590-855	74S374	10	20	
3P,R, 7P,R	590-227	AM25S09	8	16	
2A,3A	590-543	MC10116	1,16		8
6A	590-464	MC10125	16	9	8
4A,5A	589-713	MC10176	1,16		8

I.C. LIST

REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	GND PIN	POWER PINS

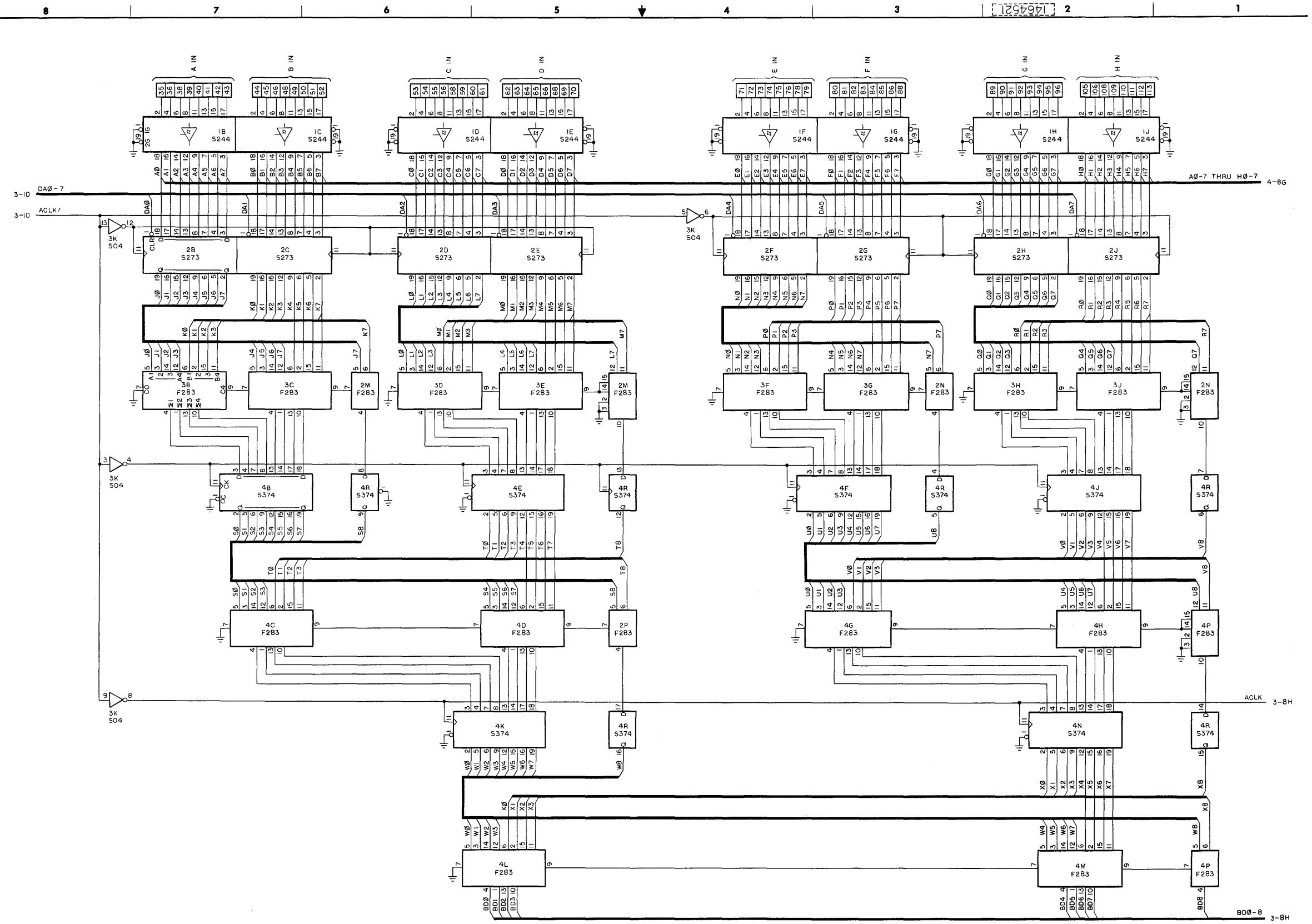


SPARES

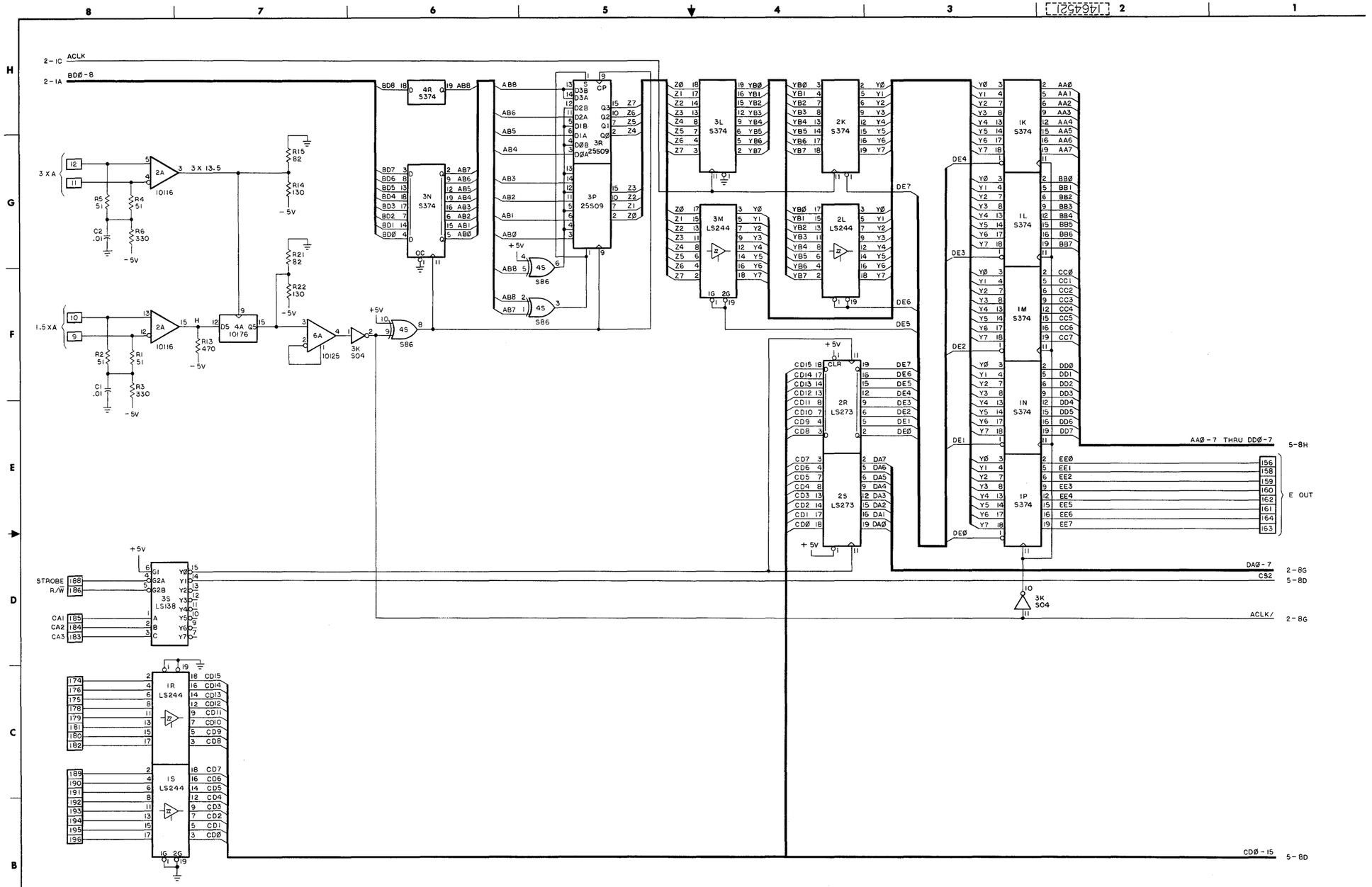


1464519	CONC
NEXT ASSY	USED ON
APPLICATION	

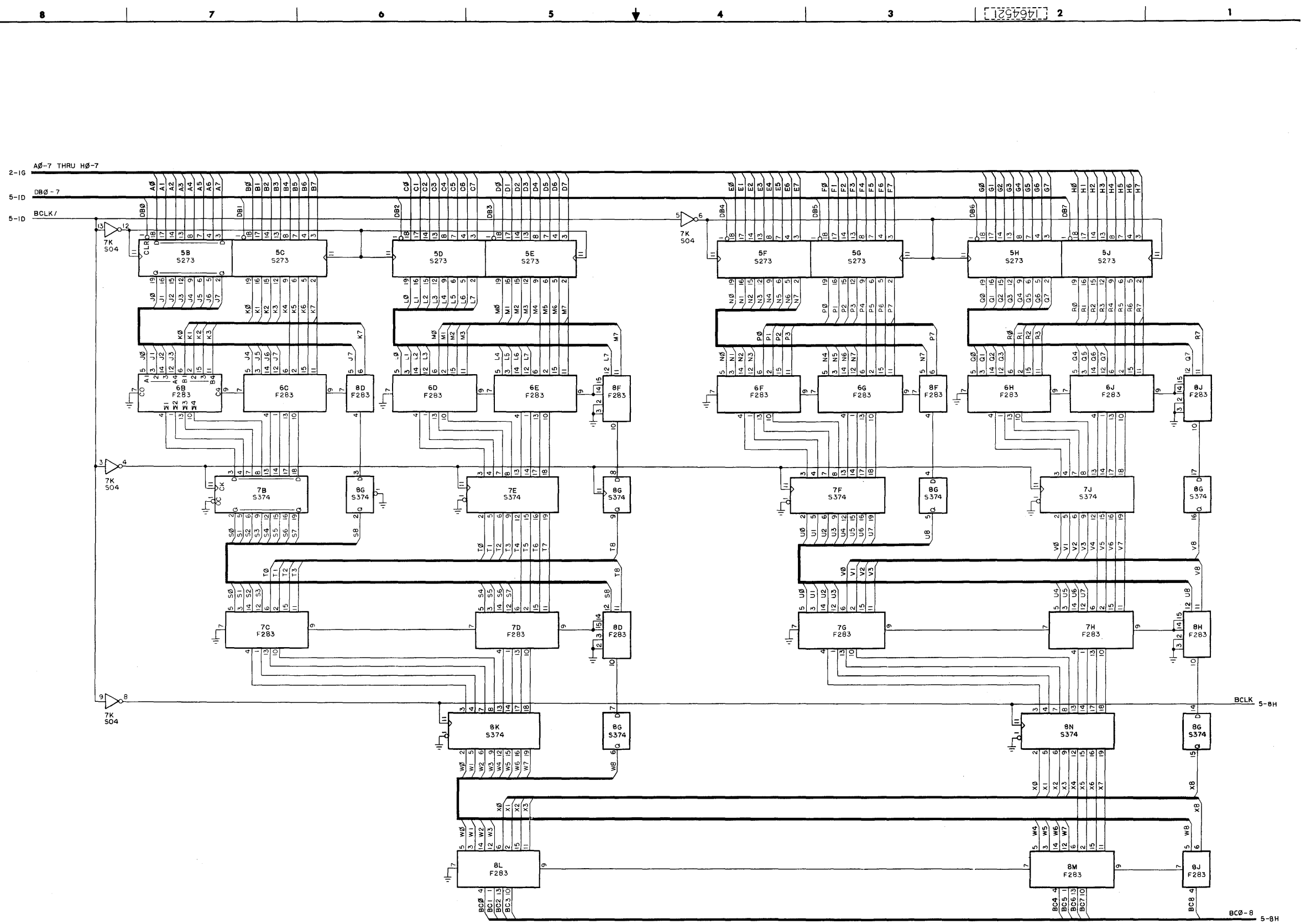
Schematic No. 1464521—.
Adder PWA, A8
(Sheet 1 of 5)



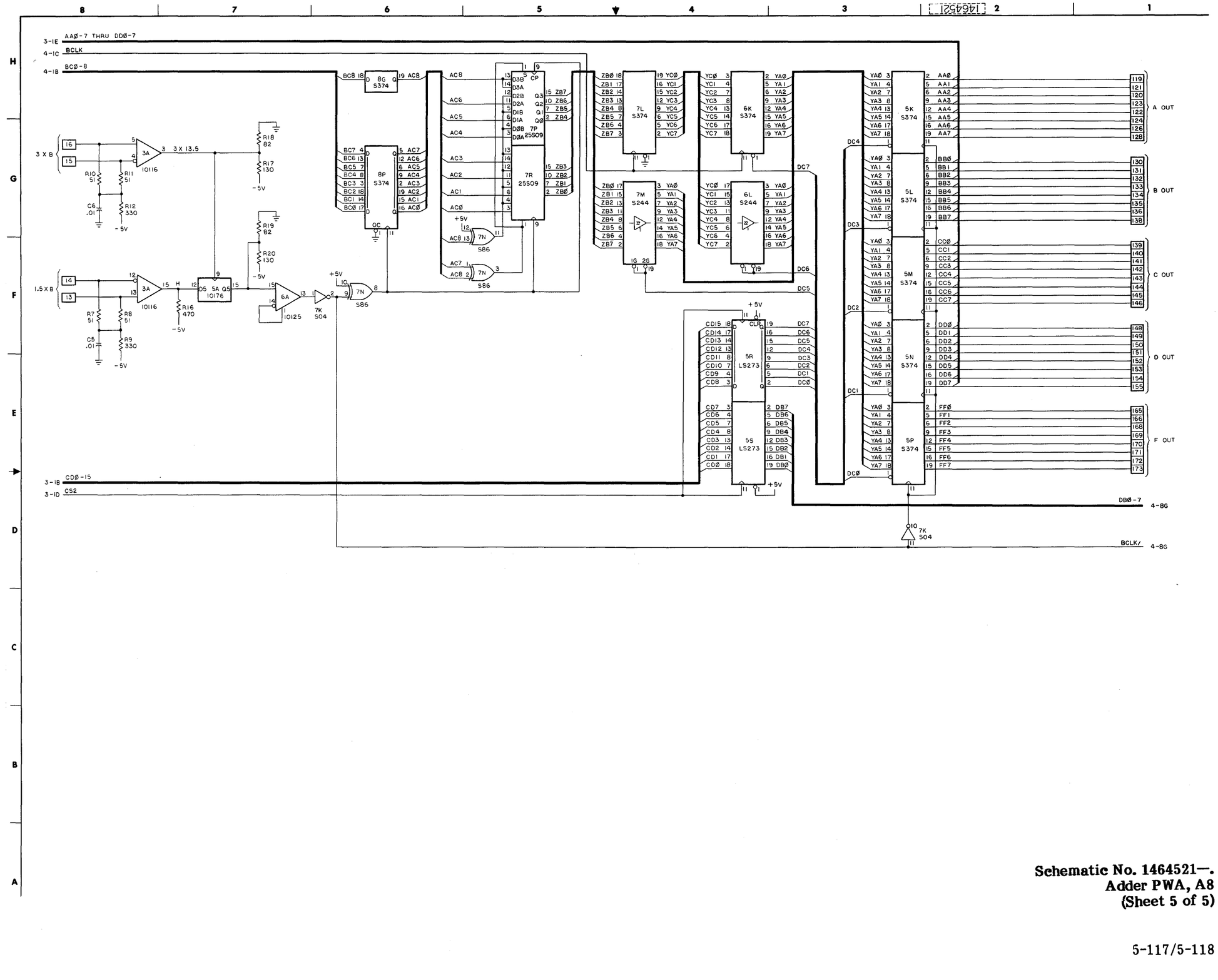
Schematic No. 1464521—.
Adder PWA, A8
(Sheet 2 of 5)



Schematic No. 1464521—.
Adder PWA, A8
(Sheet 3 of 5)



Schematic No. 1464521—.
Adder PWA, A8
(Sheet 4 of 5)



Schematic No. 1464521—.
Adder PWA, A8
(Sheet 5 of 5)

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1				
2				
3	1464527	SCHEMATIC		(A)
4				
5	1409670-BZ	LABEL, EXTRACTOR ARM, PWA		1
6	1409976-AA	INSULATOR, STIFFENER		1
7	1409976-AB	INSULATOR, STIFFENER		1
8	1409997-AA	STIFFENER, PWB		1
9	1409997-AB	STIFFENER, PWB		1
10				
11	1464657-01	PROM ASSEMBLY REF: 590-953 TBP28L22	8P	1
12	1464658-01	REF: 590-953 TBP28L22	5P	1
13	1464659-01	REF: 590-953 TBP28L22	5D,H,10G	3
14	1464660-01	REF: 589-940 TBP28S42	5N,6N,9G	3
15	1464661-01	REF: 000-004 10139	3T	1
16	1464662-01	PROM ASSEMBLY REF: 000-038 87S181	7A,L,8S	3
17	1465087-01	PROM ASSEMBLY REF: 003-038 PAL16H2	10E,J	2
18				
19				
20				
21				
22				
23	064-652	CAPACITOR, CER., .01uF, 50V, 20%	C1-3,47-49,77, 78	8
24	064-653	CAPACITOR, CER., .1uF, 50V, 20%	C4-7,9-36,38-46, 50-76,79-90	80
25				
26	037-965	CAPACITOR, TANT., 120uF, 10V, 20%	C8,37	2
27				
28	000-128	INTEGRATED CIRCUIT, 74S283	1N,2N,7C,D,H,J	6
29	000-151	10136	2T	1
30	002-168	MPY112K	4M	1
31	589-713	10176	2A,K,4T,5T	4
32	589-823	74LS138	2S	1
33	589-830	74LS174	8N	1
34	589-837	74S00	3S,9P	2
35	589-838	74S04	3A,B,K,L,5S,6S, 7S,10R	8
36	589-846	74S74	7R	1
37	589-850	INTEGRATED CIRCUIT, 74S163	4A,L,7N,9L,R,S, 9T,10N	8

LM-1464525

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1464525 SHEET 2 OF 3	REV —

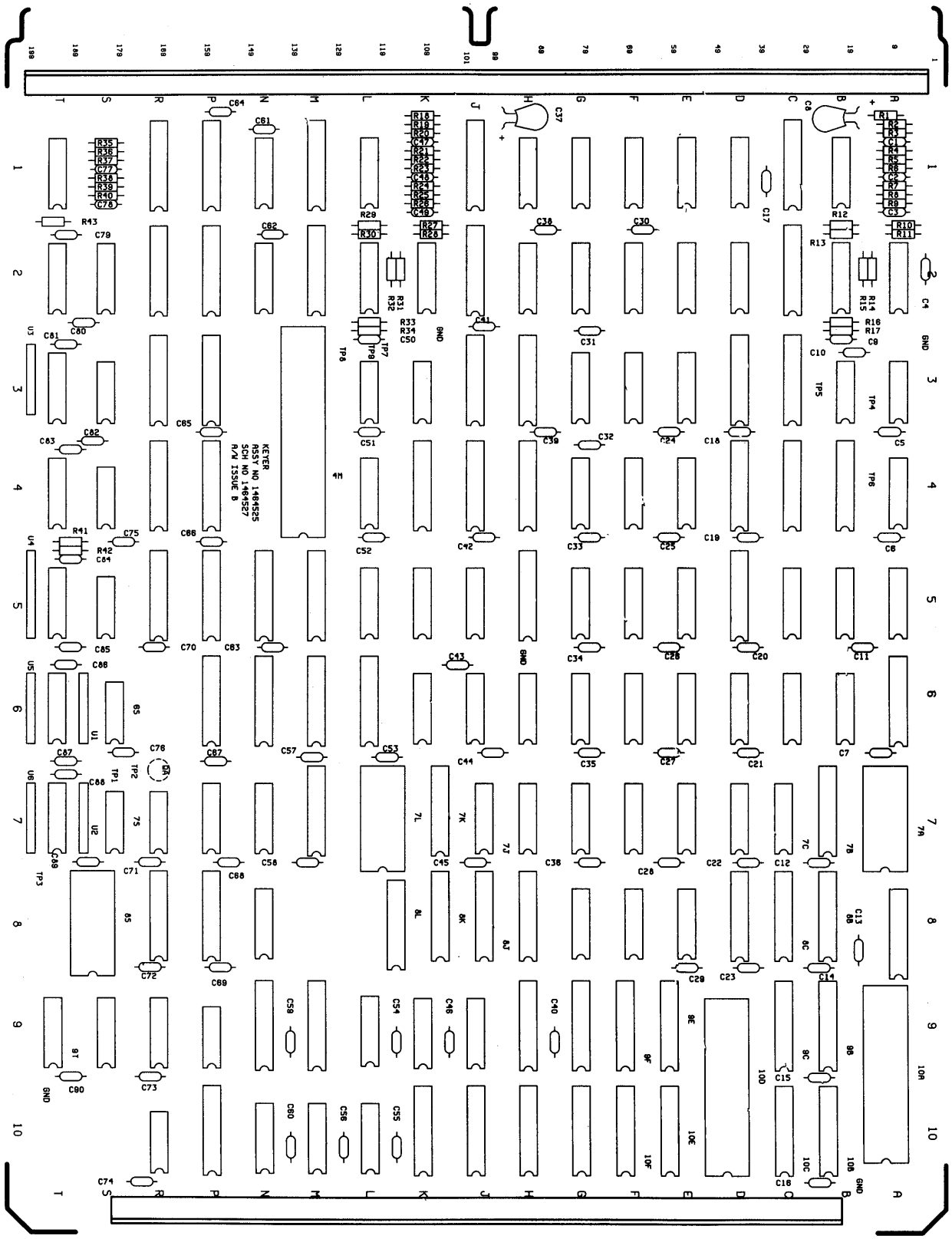
ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
38	589-937	INTEGRATED CIRCUIT, 74S174	7P	1
39	590-221	27S07	5A,B,K,L,9J,K, 10L,M	8
40	590-335	74LS273	8C,J,9E,N	4
41	590-443	74S02	4S	1
42	590-464	10125	2B,L,6T,7T	4
43	590-496	74LS151	1E,F,G,2E,F,G, 3E,F,G,4E,F,G, 5E,F,G,6E,F,G,7E,F,G, 8E,F,G	24
44	590-543	10116	1B,L,T	3
45	590-584	74LS244	1R,2R	2
46	590-586	74LS374	9B,C,10B,C	4
47	590-606	74LS283	1D,H,2D,H	4
48	590-842	74S157	6C,D,H,J	4
49	590-843	74S85	5C,J,6B,K	4
50	590-855	74S374	1C,J,M,P,2C,J,M, 2P,3C,D,H,J,P,R, 4B,C,D,H,J,K,R,5M,R,6A,L,M, 6P,7B,K,M,8A,B,D,H,K,L,R, 9F,H,M,10F,H,K	43
51	590-868	74S244	4P	1
52	590-917	74S273	10P	1
53	590-987	INTEGRATED CIRCUIT, MPY8HJ-1	10A,D	2
54				
55				
56				
57	039-163	RESISTOR NETWORK, 470 OHMS, 10 PIN SIP	U4	1
58	039-178	150 OHMS, 8 PIN SIP	U5,6	2
59	039-208	82 OHMS, 8 PIN SIP	U1,2	2
60	039-329	RESISTOR NETWORK, 470 OHMS, 8 PIN SIP	U3	1
61				
62				
63	066-811	RESISTOR, C.F., 51 OHMS, 1/4W, 5%	R2,3,5-8,19,20,22-25, 35,36,38,39	16
64	066-818	470	R14,15,31,32,43	5
65	066-835	82	R11,13,17,28,30, 34,41	7
66	066-837	130	R10,12,16,27,29, 33,42	7
67	066-838	RESISTOR, C.F., 330 OHMS, 1/4W, 5%	R1,4,9,18,21,26, 37,40	8
68				
69				
70	173-024	TERMINAL, TURRET, SWAGE	GND	5
71	187-354	TERMINAL, TEST POINT	TP1-9	9
72				
73	582-280	I.C. MTG HDW., SOCKET, 24 PIN	REF:7A,L,8S	3
74	582-282	I.C. MTG HDW., SOCKET, 40 PIN	REF:10A,D	2
75	582-330	I.C. MTG HDW., SOCKET, 14 PIN	REF:3A,B,K,L,S,4S,5S,6S, 7R,S,9P,10R	12
76	582-331	I.C. MTG HDW., SOCKET, 16 PIN	REF:1B,D,E,F,G,H,L,N,T,2A, 2B,D,E,F,G,H,K,L,N,S, 2T,3E,F,G,T,4A,E,F,G,L,T,5A, 5B,C,E,F,G,J,K,L,T,6B,C,D,E, 6F,G,H,J,K,T,7C,D,E,F,G,H,J, 7N,P,T,8E,F,G,N,9J,K,L,R,S,T, 10L,M,N	74

LM-1464525

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM- 1464525 SHEET 3 OF 3	REV —

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
77	582-333	I.C. MTG HDW., SOCKET, 20 PIN REF: 1C,J,M,P,R,2C,J,M,P,R, 3C,D,H,J,P,R,4B,C,D,H, 4J,K,P,R,5D,H,M,N,P,R,6A,L,M, 6N,P,7B,K,M,8A,B,C,D,H,J,K,L, 8P,R,9B,C,E,F,G,H,M,N,10B,C,E, 10F,G,H,J,K,P		65
78	582-397	I.C. MTG HDW., SOCKET, 48 PIN REF:4M		1
79				
80				
81	471-060	SCREW, PAN HD., X-REC, #4-40 X .250 LG		6
82	493-005	NUT, HEX, NYLON LOCK, #4-40		6
83				
84	530-477	ENCLOSURE PART, CARD INSERTER/EXTRACTOR		2

LM-1464525



Assembly No. 1464525-01—. Keyer PWA, A9, A10, NTSC

NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3 > PROM USED WITH NTSC AND PAL-M PWA 1464525.
4 > PROM USED WITH PAL PWA 1465110.
5 > STATIC SENSITIVE DEVICE. SPECIAL HANDLING REQUIRED PER AMPEX STD HE1-1.

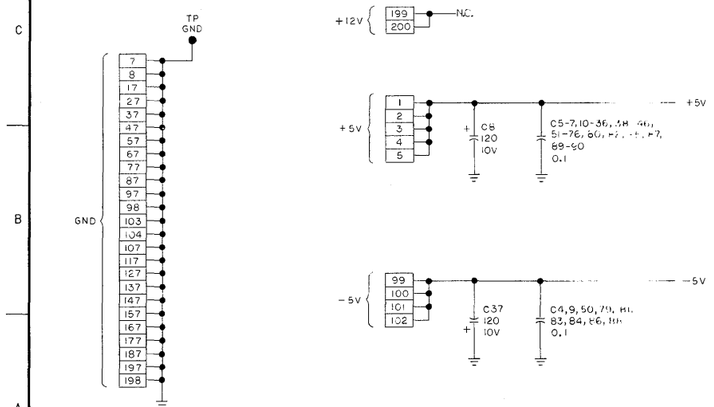
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C90	
R43	
TP9	
U6	

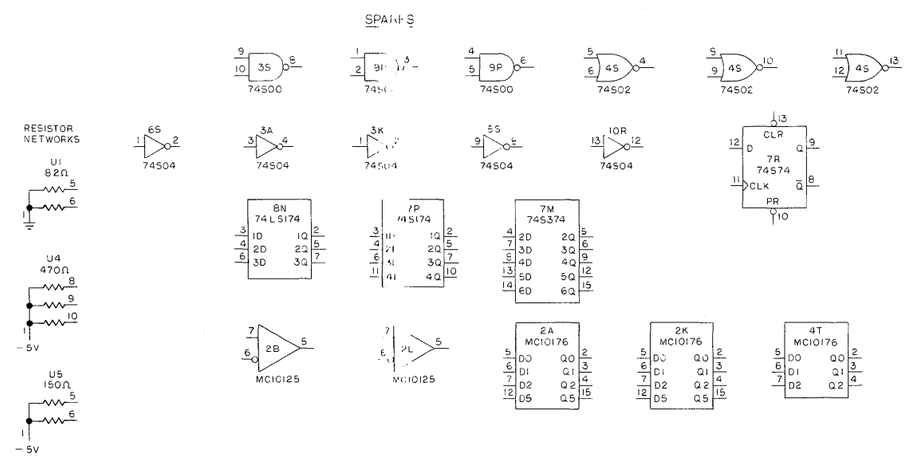
I.C. LIST

REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	GND PIN	POWER PINS +5V			
3S,9P	569-837	74S00	7	14			
4S	590-443	74S02	7	14			
3A,B,K,L,5S,6S,7S,	589-838	74S04	7	14			
10R							
7R	589-846	74S74	7	14			
5C,J,6B,K	590-843	74S85	8	16			
2S	589-823	74LS138	8	16			
1E,F,G,2E,F,G,3E,F,G,	590-496	74LS151	8	16			
4E,F,G,5E,F,G,6E,F,G,							
7E,F,G,8E,F,G							
6C,D,H,J	590-842	74S157	8	16			
4A,L,7N,9L,R,S,T, 10N	589-850	74S163	8	16			
8N	559-630	74LS174	8	16			
7P	589-937	74S174	8	16			
1R,2R	590-584	74LS244	10	20			
4P	590-868	74S244	10	20			
8C,J,9E,N	590-335	74LS273	10	20			
10P	590-917	74S273	10	20			
1D,H,2D,H	590-606	74LS283	8	16			
1N,2N,7C,D,H,J	000-128	74S283	8	16			
9B,C,10B,C	590-586	74LS374	10	20			
1C,J,M,P,2C,J,M,P,3C,D,	590-855	74S374	10	20			
3H,J,F,R,4B,C,D,H,J,							
4K,R,5M,R,6A,L,M,P,							
7B,K,M,8A,B,D,H,K,L,							
8R,9F,H,M,10F,H,K							

I.C. LIST

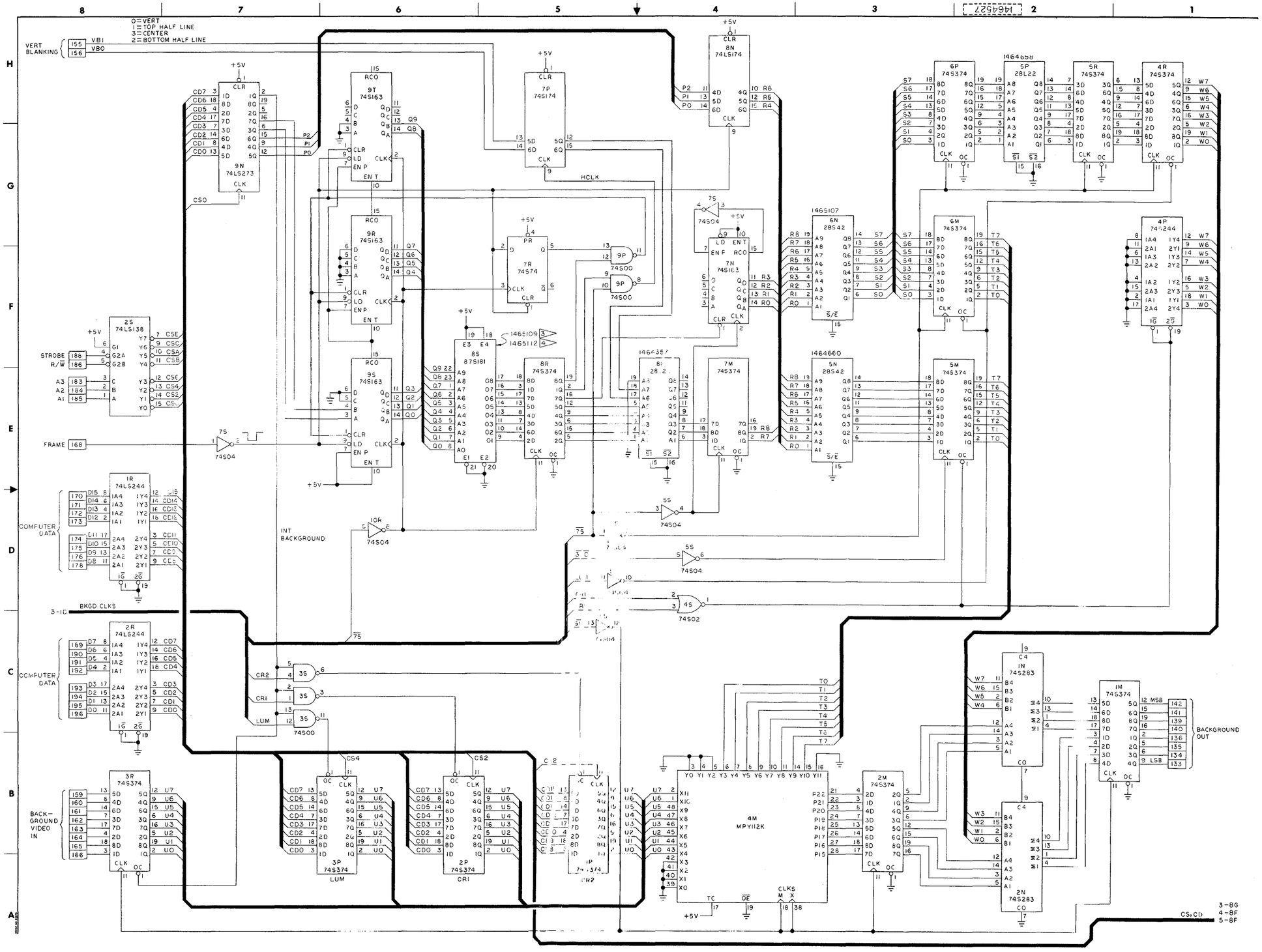
REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	GND PIN	POWER PINS +5V			
1B,L,T	590-543	MC10116	1,16		8		
2B,L,6T, 7T	590-464	MC10125	16	9	8		
2T	000-151	MC10136	1,16		8		
2A,K,4T, 5T	589-713	MC10176	1,16		8		
10A,D	590-987	MPY8HJ-1	32	30			
4M	002-168	MPY112K	36,37	12,13			
5A,B,K,L,9J,K,10L,M	590-221	27S07	8	16			
10J,10E	1465087-01	PAL16H2	10	20			
6P	1464657-01	TBP28L22	10	20			
5P	1464658-01	TBP28L22	10	20			
5D,H,10G	1464659-01	TBP28L22	10	20			
5N	1464660-01	TBP28S42	10	20			
3T	1464661-01	10139	16		8		
7A,L 5>	1464662-01	8T5181	12	24			
6N	1465107-01	TBP28S42	10	20			
9G	1465108-01	TBP28S42	10	20			
8S 3> 5>	1465109-01	8T5181	12	24			
8S 4> 5>	1465112-01	8T5181	12	24			



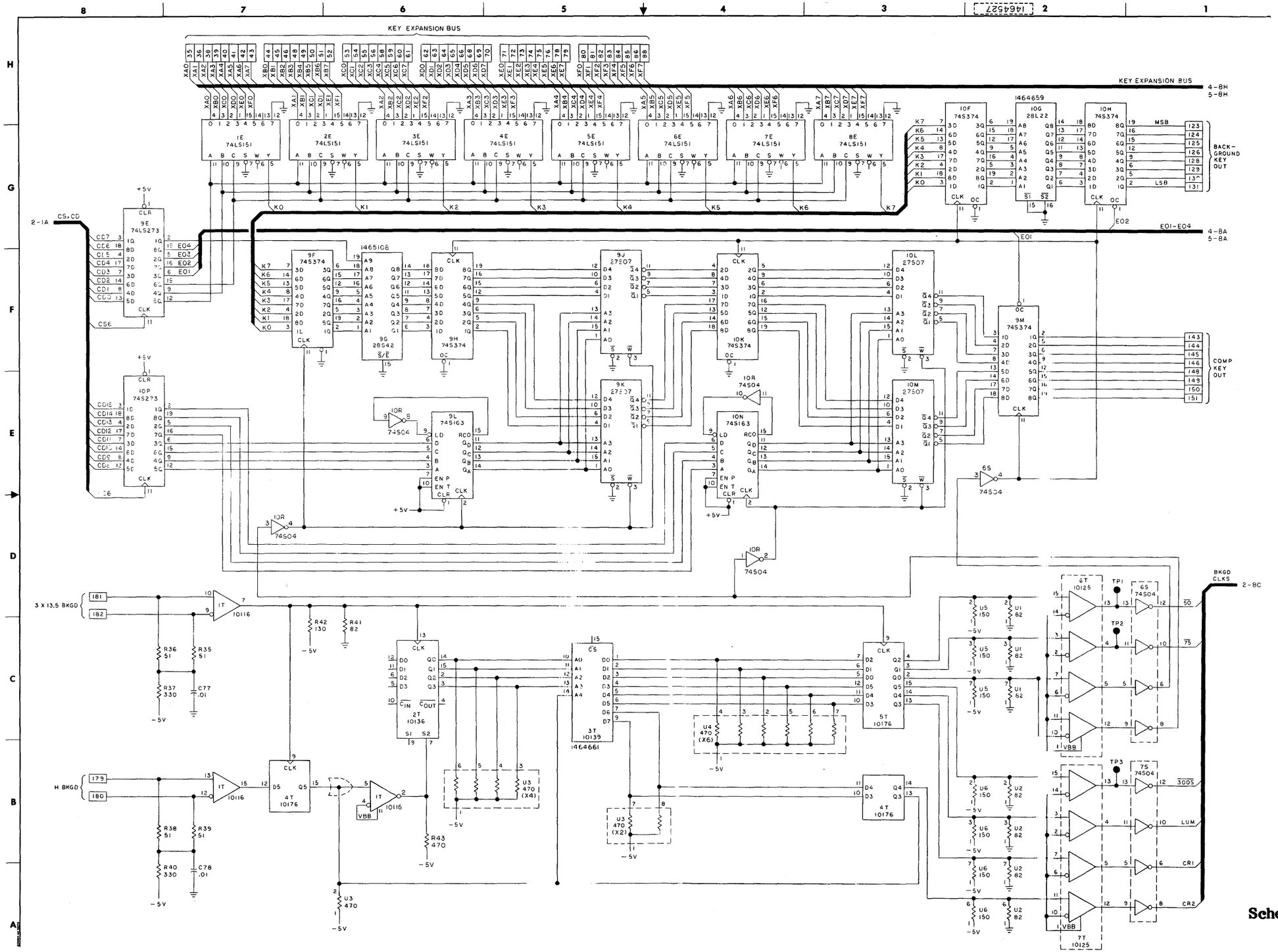


1465110	CONC
1464525	CONC
NEXT ASSY	USED ON
APPLICATION	

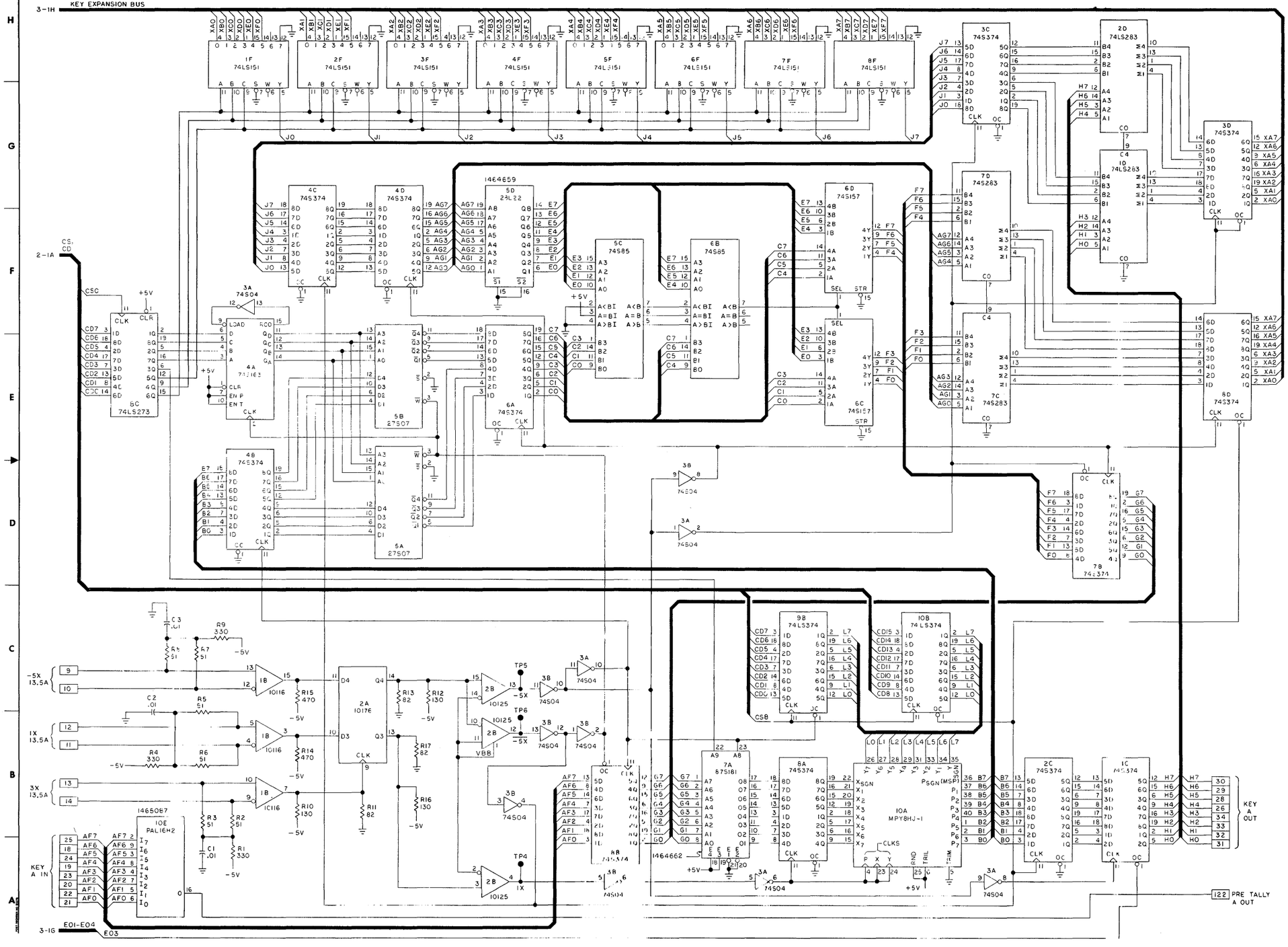
Schematic No. 1464527B.
Keyer PWA, A9, A10
(Sheet 1 of 5)



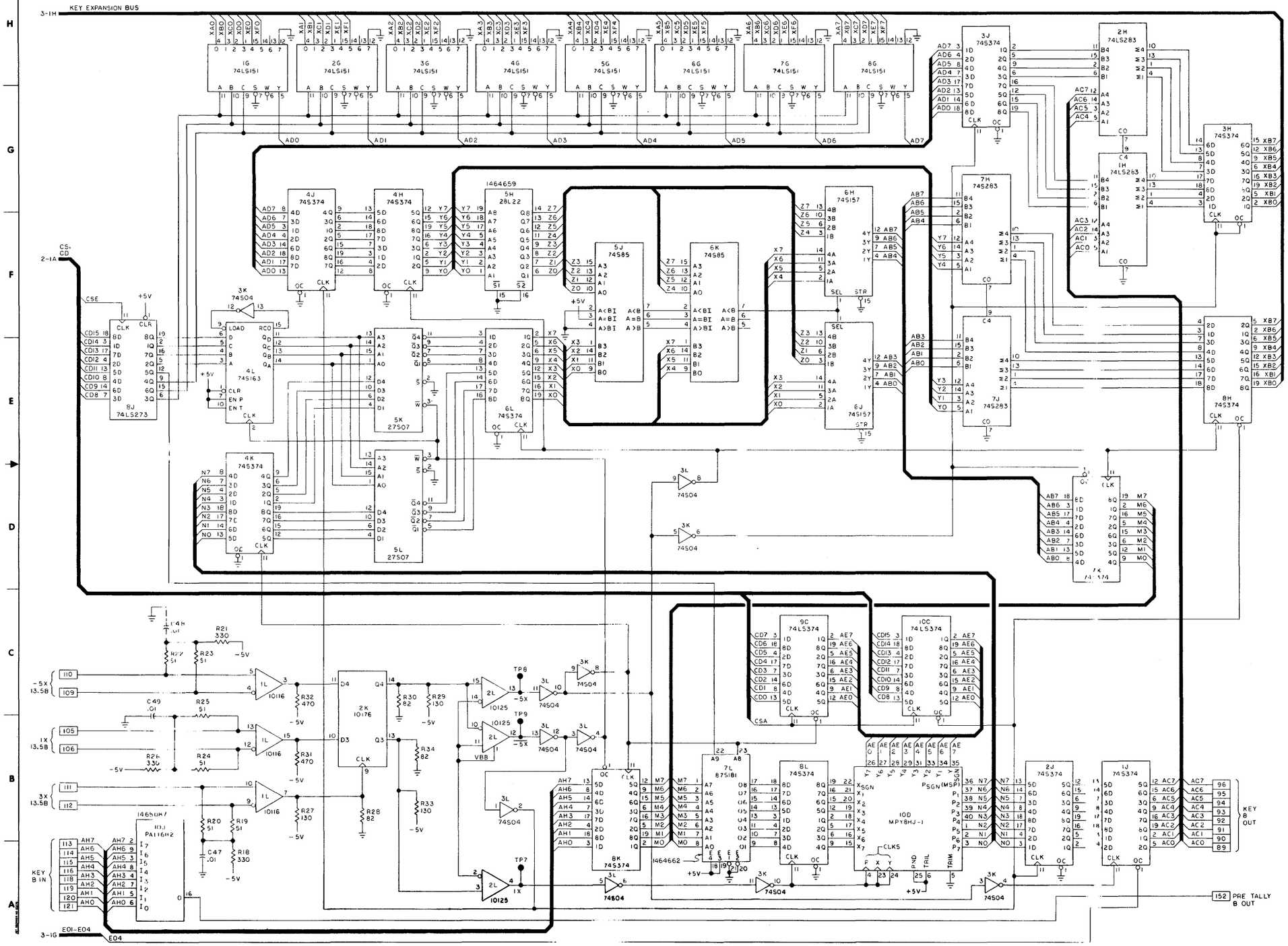
Schematic No. 1464527B.
Keyer PWA, A9, A10
(Sheet 2 of 5)



Schematic No. 1464527B.
Keyer PWA, A9, A10
(Sheet 3 of 5)



Schematic No. 1464527B.
Keyer PWA, A9, A10
(Sheet 4 of 5)



Schematic No. 1464527B.
Keyer PWA, A9, A10
(Sheet 5 of 5)

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1				
2				
3	1464527	SCHEMATIC		A
4				
5	1409670-BZ	LABEL, EXTRACTOR ARM, PWA		1
6	1409976-AA	INSULATOR, STIFFENER		1
7	1409976-AB	INSULATOR, STIFFENER		1
8	1409997-AA	STIFFENER, PWB		1
9	1409997-AB	STIFFENER, PWB		1
10				
11	1464657-01	PROM ASSEMBLY REF: 590-953 TBP28L22	8P	1
12	1464658-01	REF: 590-953 TBP28L22	5P	1
13	1464659-01	REF: 590-953 TBP28L22	5D,H,10G	3
14	1464660-01	REF: 589-940 TBP28S42	5N	1
15	1464661-01	REF: 000-004 10139	3T	1
16	1464662-01	REF: 000-038 87S181 (1)	7A,L	2
17	1465087-01	REF: 003-038 PAL16H2	10E,J	2
18	1465107-01	REF: 589-940 TBP28S42	6N	1
19	1465108-01	REF: 589-940 TBP28S42	9G	1
20	1465112-01	PROM ASSEMBLY REF: 000-038 87S181 (1)	8S	1
21				
22				
23	064-652	CAPACITOR, CER., .01uF, 50V, 20%	C1-3,47-49,77, 78	8
24	064-653	CAPACITOR, CER., .1uF, 50V, 20%	C4-7,9-36,38-46, 50-76,79-90	80
25				
26	037-965	CAPACITOR, TANT., 120uF, 10V, 20%	C8,37	2
27				
28	000-128	INTEGRATED CIRCUIT, 74S283	1N,2N,7C,D,H,J	6
29	000-151	10136	2T	1
30	002-168	MPY112K	4M	1
31	589-713	10176	2A,K,4T,5T	4
32	589-823	74LS138	2S	1
33	589-830	74LS174	8N	1
34	589-837	74S00	3S,9P	2
35	589-838	74S04	3A,B,K,L,5S,6S, 7S,10R	8
36	589-846	74S74	7R	1
37	589-850	INTEGRATED CIRCUIT, 74S163	4A,L,7N,9L,R,S, 9T,10N	8

LM-1465110

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
38	589-937	INTEGRATED CIRCUIT, 74S174	7P	1
39	590-221	27S07	5A,B,K,L,9J,K, 10L,M	8
40	590-335	74LS273	8C,J,9E,N	4
41	590-443	74S02	4S	1
42	590-464	10125	2B,L,6T,7T	4
43	590-496	74LS151	1E,F,G,2E,F,G, 3E,F,G,4E,F,G 5E,F,G,6E,F,G, 7E,F,G,8E,F,G	24
44	590-543	10116	1B,L,T	3
45	590-584	74LS244	1R,2R	2
46	590-586	74LS374	9B,C,10B,C	4
47	590-606	74LS283	1D,H,2D,H	4
48	590-842	74S157	6C,D,H,J	4
49	590-843	74S85	5C,J,6B,K	4
50	590-855	74S374	1C,J,M,P,2C,J,M, 2P,3C,D,H,J,P,R, 4B,C,D,H,J,K,R,5M,R,6A,L, M,6P,7B,K,M,8A,B,D,H,K,L, R,9F,H,M,10F,H,K	43
51	590-868	74S244	4P	1
52	590-917	74S273	10P	1
53	590-987	INTEGRATED CIRCUIT, MPY8HJ-1	10A,D	2
54				
55				
56				
57	039-163	RESISTOR, NETWORK, 470 OHMS, 10 PIN SIP	U4	1
58	039-178	RESISTOR, NETWORK, 150 OHMS, 8 PIN SIP	U5,6	2
59	039-208	RESISTOR, NETWORK, 82 OHMS, 8 PIN SIP	U1,2	2
60	039-329	RESISTOR, NETWORK, 470 OHMS, 8 PIN SIP	U3	1
61				
62				
63	066-811	RESISTOR, C.F., 51 OHMS, 1/4W, 5%	R2,3,5-8,19,20,22-25, 35,36,38,39	16
64	066-818	RESISTOR, C.F., 470 OHMS, 1/4W, 5%	R14,15,31,32,43	5
65	066-835	RESISTOR, C.F., 82 OHMS, 1/4W, 5%	R11,13,17,28,30, 34,41	7
66	066-837	RESISTOR, C.F., 130 OHMS, 1/4W, 5%	R10,12,16,27,29, 33,42	7
67	066-838	RESISTOR, C.F., 330 OHMS, 1/4W, 5%	R1,4,9,18,21,26, 37,40	8
68				
69				
70	173-024	TERMINAL, TURRET, SWAGE	GND	5
71	187-354	TERMINAL, TEST POINT	TP1-9	9
72				
73	582-280	I.C., MTG HDW., SOCKET, 24 PIN	REF:7A,L,8S	3
74	582-282	I.C., MTG HDW., SOCKET, 40 PIN	REF:10A,D	2
75	582-330	I.C. MTG HDW., SOCKET, 14 PIN	REF:3A,B,K,L,S,4S,5S,6S, 7R,S,9P,10R	12
76	582-331	I.C. MTG HDW., SOCKET, 16 PIN	REF:1B,D,E,F,G,H,L,N,T,2A, 2B,D,E,F,G,H,K,L,N,S,2T, 3E,F,G,T,4A,E,F,G,L,T,5A, 5B,C,E,F,G,J,K,L,T,6B,C,D, E,F,G,H,J,K,T,7C,D,E,F,G, H,J,7N,P,T,8E,F,G,N,9J,K, L,R,S,T,10L,M,N	74

LM-1465110

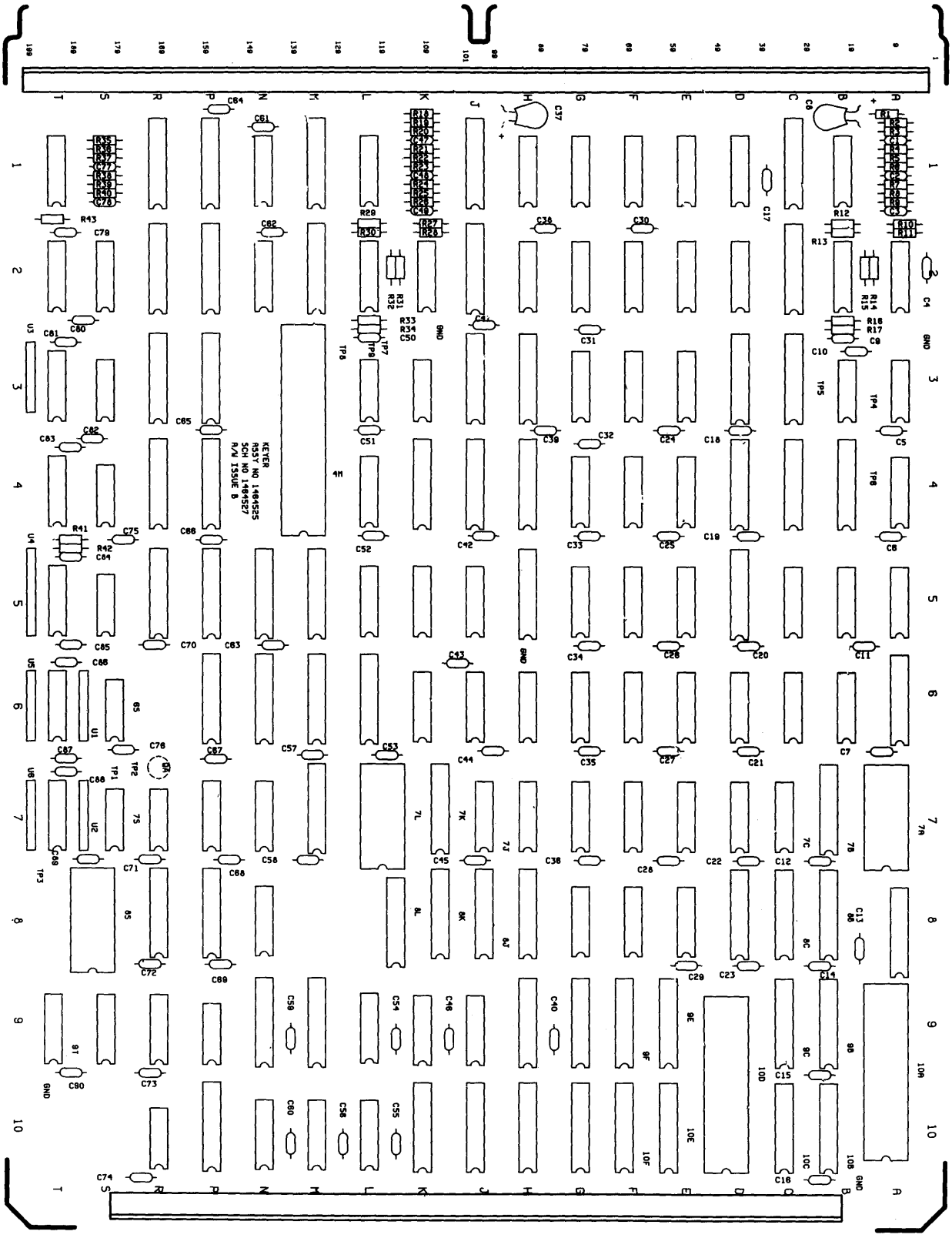
AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1465110 SHEET 3 OF 3	REV —

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
77	582-333	I.C. MTG HDW., SOCKET, 20 PIN	REF:1C,J,M,P,R,2C,J,M,P,R, 3C,D,H,J,P,R,4B,C,D,H,J,K, 4P,R,5D,H,M,N,P,R,6A,L,M,N, 6P,7B,K,M,8A,B,C,D,H,J,K,L, P,R,9B,C,E,F,G,H,M,N,10B,C, E,F,G,H,J,K,P	65
78	582-397	I.C. MTG HDW., SOCKET, 48 PIN	REF:4M	1
79				
80				
81	471-060	SCREW, PAN HD., X-REC, #4-40 X .250 LG		6
82	493-005	NUT, HEX, NYLON LOCK, #4-40		6
83				
84	530-477	ENCLOSURE PART, CARD INSERTER/EXTRACTOR		2

NOTES:

1. STATIC SENSITIVE DEVICE, SPECIAL HANDLING REQUIRED PER AMPEX STD HE1-1.

LM-1465110



Assembly No. 1465110-01—. Keyer PWA, A9, A10, PAL

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1				
2				
3	1464530	SCHEMATIC		(-)
4				
5	1409670-CA	LABEL, EXTRACTOR ARM		1
6	1409976-AA	INSULATOR, STIFFENER		1
7	1409976-AB	INSULATOR, STIFFENER		1
8	1409997-AA	STIFFENER, PWB		1
9	1409997-AB	STIFFENER, PWB		1
10				
11	1464663-01	PROM ASSY REF: 000-010 DM82S100	6N,R,S,U	4
12	1464666-01	REF: 000-004 MC10139	8B,E	2
13	1464669-01	REF: 000-038 DM87S181 [1]	8J,12T	2
14	1464672-01	REF: 000-038 DM87S181 [1]	8K,12S	2
15	1464675-01	REF: 000-038 DM87S181 [1]	8L,12R	2
16	1464678-01	REF: 000-010 DM82S100	8N,9S	2
17	1464681-01	REF: 000-010 DM82S100	9U,R	2
18	1464684-01	REF: 000-038 DM87S181 [1]	10J,11K	2
19	1464687-01	PROM ASSY REF: 000-038 DM87S181 [1]	10K,11L	2
20				
21				
22	064-652	CAPACITOR, CER., 0.01uF, 50V, ±20%	C49-56	8
23	064-653	CAPACITOR, CER., 0.1uF, 50V, ±20%	C2-48,57-75, 77-127	117
24				
25	037-965	CAPACITOR, TANT., 120uF, 10V, ±20%	C1,76	2
26				
27				
28	000-152	INTEGRATED CIRCUIT, MC10125	9D,E	2
29	000-153	MC10104	6H	1
30	001-076	MC10174	3L,M,4L,M,6K, 6L	6
31	001-077	MC10176	3C,E,N,P,R,S,T, 3U,4A,C,E,N,P, 4R,S,T,U,5A,C,E,6B,E, 7B,E,8C,F	26
32	002-050	MC10101	1B,C,D,E,F,L,M, 2B,C,D,E,F,3B, 6C,D,G,7C,D,G	19
33	002-929	74F163	8G,H,9G,12L,M, 12N	6
34	002-992	74LS491	10H,11J	2
35	587-550	INTEGRATED CIRCUIT, MC10136	3G,H,J,K,4G,H,J,K, 5G,H,J,K,8A,D	14

LM-1464528

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1464528 SHEET 2 OF 3	REV —

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
36	589-512	INTEGRATED CIRCUIT, MC10173	3D,F,4B,D,F,5B,5D,F	8
37	589-823	74LS138	2U	1
38	589-824	74LS153	11G,H	2
39	589-920	MC10231	2G,H,J,K,5L,M	6
40	590-326	MC10131	2L,M	2
41	590-330	MC10115	1G,J	2
42	590-564	10124DCQR	2N,P,R,S,T,6A,6F,7A,F	9
43	590-584	74LS244	1P,T,U	3
44	590-586	74LS374	1N,R,S,10L,M,11P,R	7
45	590-935	74F00	12H	1
46	590-940	74F74	5N,P,R,S,T,U,6M,7M,11E,F,12J,K	12
47	590-947	INTEGRATED CIRCUIT, 74F374	7J,K,L,8R,S,T,8U,11S,T,U	10
48				
49				
50				
51	039-178	NETWORK, RESISTOR, 150 OHMS	U1,43,45	3
52	039-200	330 OHMS	U35	1
53	039-208	82 OHMS	U2,42,44	3
54	039-264	4.7K OHMS	U57	1
55	039-329	470 OHMS	U3-29,32-34,38-41,46-56	45
56	039-378	NETWORK, RESISTOR, 47 OHMS	U30,31,36,37	4
57				
58				
59	143-981	JACK, P.C., TIP	A & B OF J1-14	28
60				
61				
62	173-024	TERMINAL, TURRET	GND	4
63				
64	471-060	SCREW, PAN HD., XREC, #4-40 X .250 LG		6
65				
66	493-005	NUT, HEX, NYLON LOCK, #4-40		6
67				
68	530-477	ENCLOSURE, PART, CARD		2
69				
70	582-280	I.C., MTG. HDW., 24 PIN	REF: 8J,K,L,10J,K,11K,L,12R,S,T	10
71	582-281	28 PIN	REF: 6N,R,S,U,8N,9R,S,U	8
72	582-330	14 PIN	REF: 5N,P,R,S,T,U,6M,7M,11E,F,12H,J,K	13
73	582-331	16 PIN	REF: 1B,C,D,E,F,G,J,L,M,2B,C,D,E,F,G,H,J,K,2L,M,N,P,R,S,T,U,3B,C,D,E,F,G,H,J,K,L,3M,N,P,R,S,T,U,4A,B,C,D,E,F,G,H,J,K,L,4M,N,P,R,S,T,U,5A,B,C,D,E,F,G,H,J,K,L,M,6A,B,C,D,E,F,G,H,K,L,7A,B,C,D,E,F,G,8A,8B,C,D,E,F,G,H,9D,E,G,11G,H,12L,M,N	106
74	582-333	20 PIN	REF: 1N,P,R,S,T,U,7J,K,L,8R,S,8T,U,10L,M,11P,R,S,T,U	20
75	582-416	I.C., MTG. HDW., 24 PIN	REF: 10H,11J	2
76				

LM-1464528

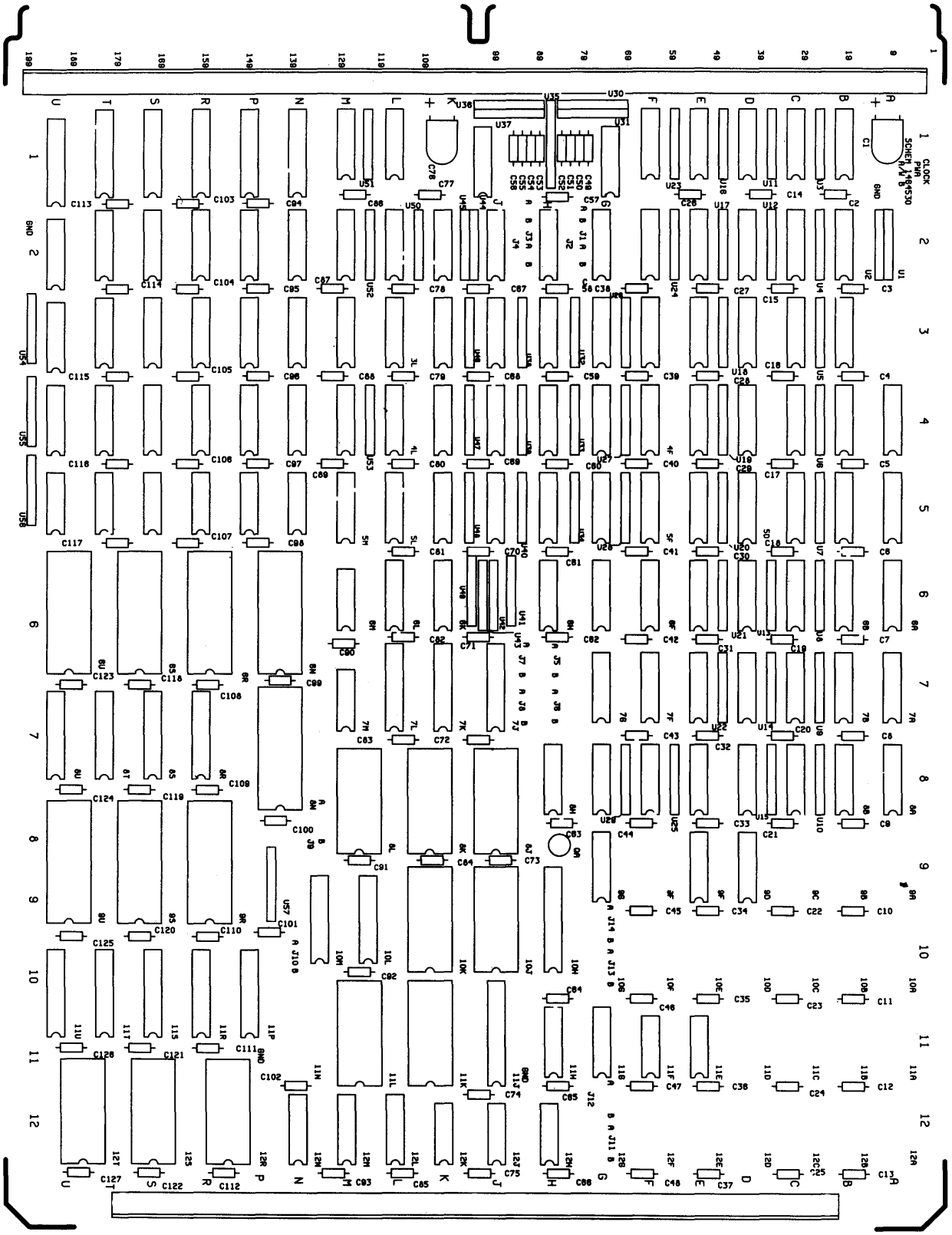
AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1464528 SHEET 3 OF 3	REV —

ITEM NO.	PART NUMBER		DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
77					
78					
79	602-044	SHORTING PLUG, RED		J1-14	14

NOTES:

1. STATIC SENSITIVE DEVICE, SPECIAL HANDLING REQUIRED PER AMEPX STD HE1-1.

LM-1464528



Assembly No. 1464528-01—. Clock PWA, A11, NTSC

NOTE: UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS.1/4W.5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.

(3) STATIC SENSITIVE DEVICE. SPECIAL HANDLING REQUIRED PER AMPEX STD HE1-1.

(4) USED ON 1464528(NTSC/PAL-M) ASSEMBLY ONLY.

(5) USED ON 1465111(PAL) ASSEMBLY ONLY.

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C127	
J14	
U57	

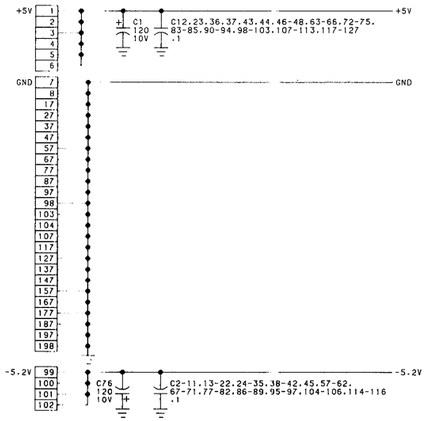
I.C. LIST

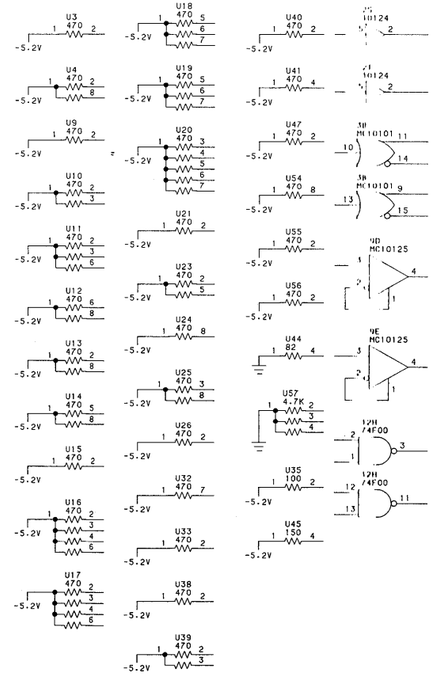
REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	GND PIN	POWER PINS +5V	POWER PINS -5.2V		
9D.E	000-152	MC10125	1.16	9	8		
6H	000-153	MC10104	1.16		8		
3L.M.4L.M.6K.L	001-076	MC10174	1.16		8		
3C.E.N.P.R.S.T.U.4A.C.	001-077	MC10176	1.16		8		
E.N.P.R.S.T.U.5A.C.E.							
6B.E.7B.E.8C.F							
1B.C.D.E.F.L.M.2B.C.D.	002-050	MC10101	1.16		8		
E.F.3B.6C.D.G.7C.D.G							
8G.H.9G.12L.M.N	002-929	74F163	8	16			
10M.11J	002-992	74LS491	12	24			
3G.H.J.K.4G.H.J.K	587-550	MC10136	1.16		8		
5G.H.J.K.8A.D							
3D.F.4B.D.F.5B.D.F	589-512	MC10173	16		8		
2U	589-823	74LS138	8	16			
11G.H	589-824	74LS153	8	16			
2G.H.J.K.5L.M	589-920	MC10231	1.16		8		
2L.M	590-326	MC10131	1.16		8		
1G.J	590-330	MC10115	1.16		8		
2N.P.R.S.T.6A.F.7A.F	590-564	10124DCQR	16	9	8		
1P.T.U	590-584	74LS244	10	20			
1N.R.S.10L.M.11P.R	590-586	74LS374	10	20			
12H	590-935	74F00	7	14			
5N.P.R.S.T.U.6M.7M.	590-940	74F74	7	14			
11E.F.12J.K							
7J.K.L.8R.S.T.U.11S.T.U	590-947	74F374	10	20			
6N.R.S.U	1464663	DM82S100	14	28			
8B.E	1464666	MCM10139	16		8		
(4)(3) 8J.12T	1464669	DM87S181	12	24			
(4)(3) 8K.12S	1464672	DM87S181	12	24			

I.C. LIST

REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	GND PIN	POWER PINS +5V	POWER PINS -5.2V		
(4)(3) 8L.12R	1464675	DM87S181	12	24			
8N.9S	1464678	DM82S100	14	28			
9U.R	1464681	DM82S100	14	28			
(4)(3) 10J.11K	1464684	DM87S181	12	24			
(4)(3) 10K.11L	1464687	DM87S181	12	24			
(5)(3) 8J.12T	1465113	DM87S181	12	24			
(5)(3) 8K.12S	1465114	DM87S181	12	24			
(5)(3) 8L.12R	1465115	DM87S181	12	24			
(5)(3) 10J.11K	1465116	DM87S181	12	24			
(5)(3) 10K.11L	1465117	DM87S181	12	24			

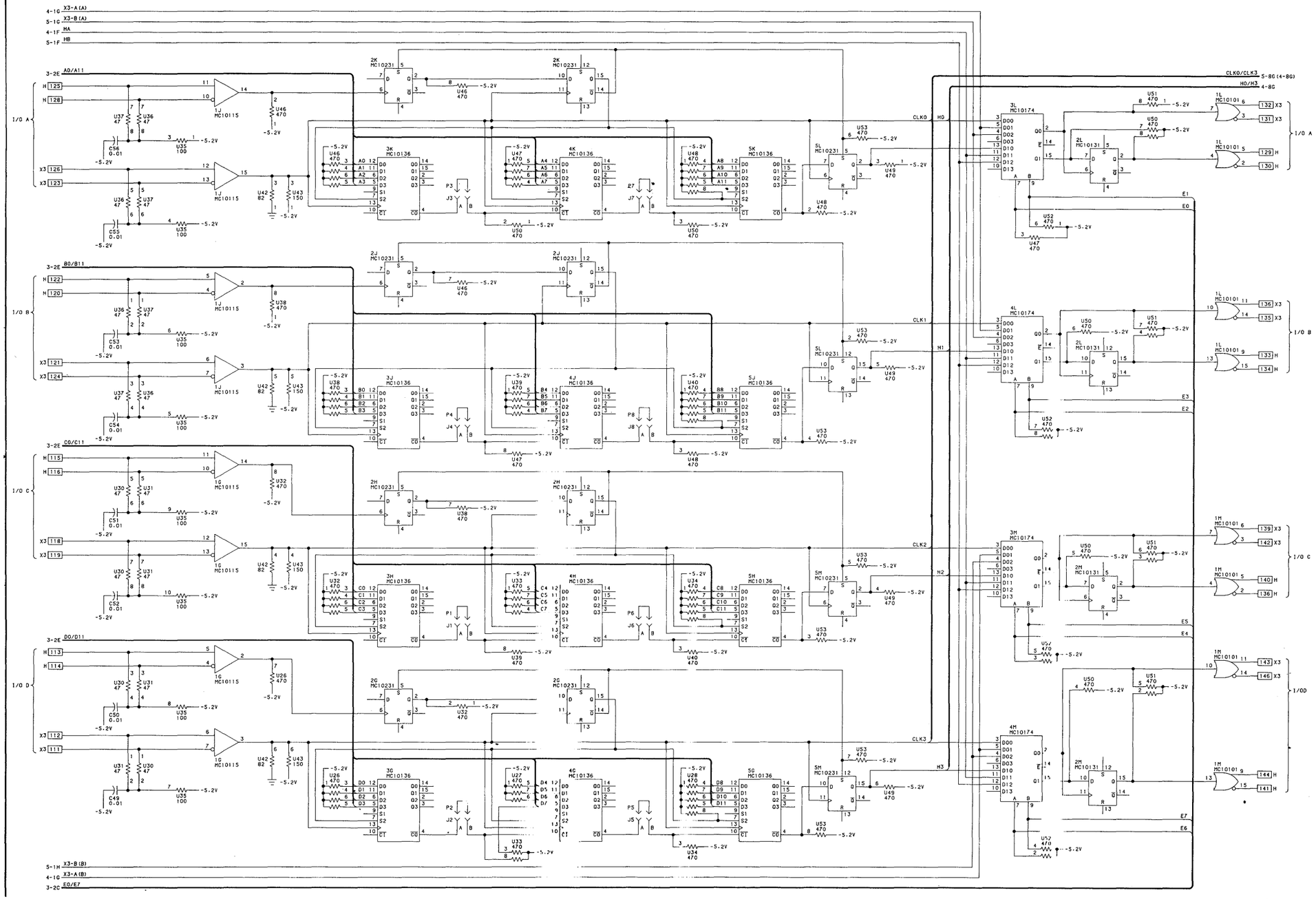
SPARES





1465111	CONC
1464528	CONC
NEXT ASSY	USED ON
APPLICATION	

Schematic No. 1464530B.
Clock PWA, A11
(Sheet 1 of 9)



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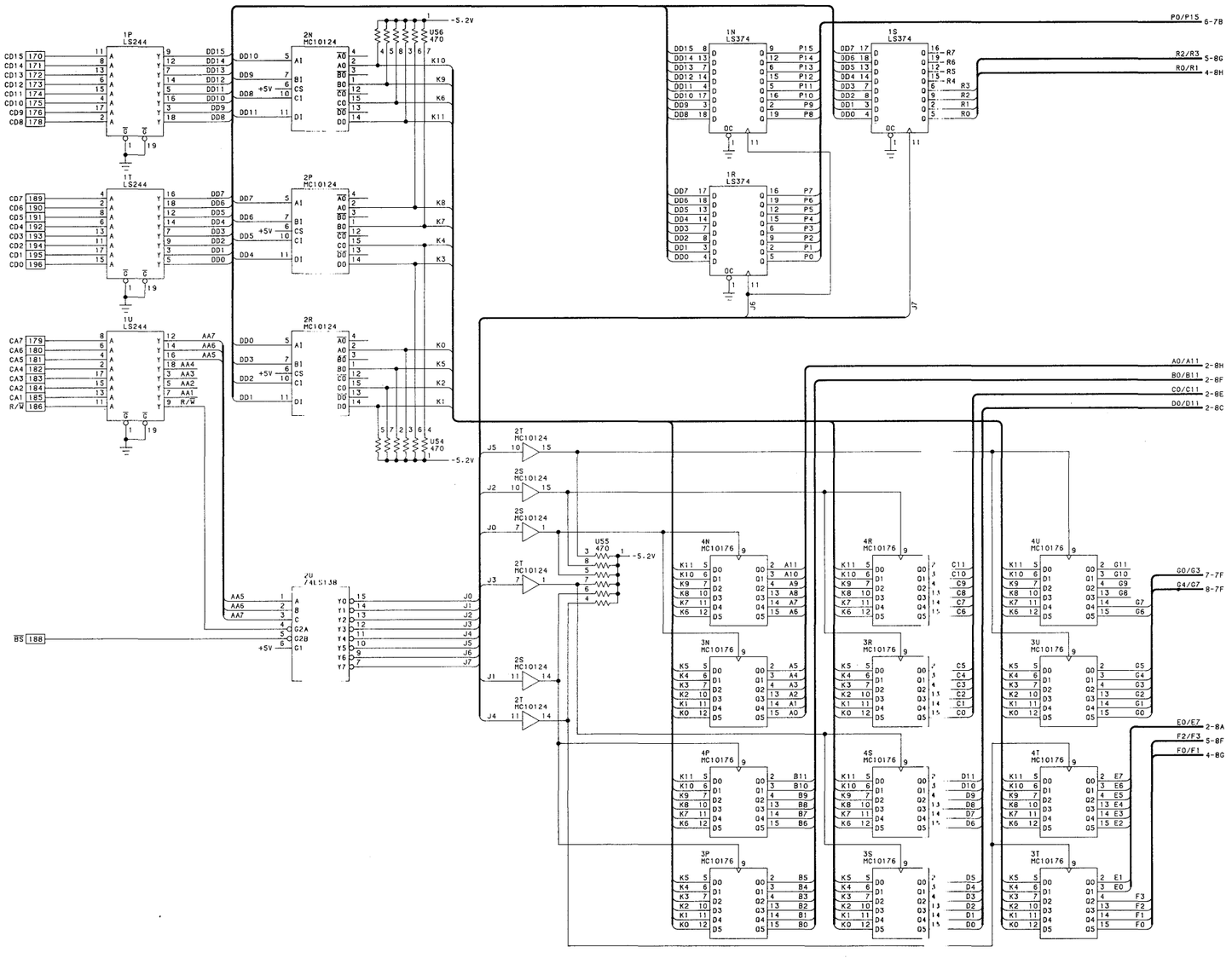
Clock PWA, A11
(Sheet 2 of 9)



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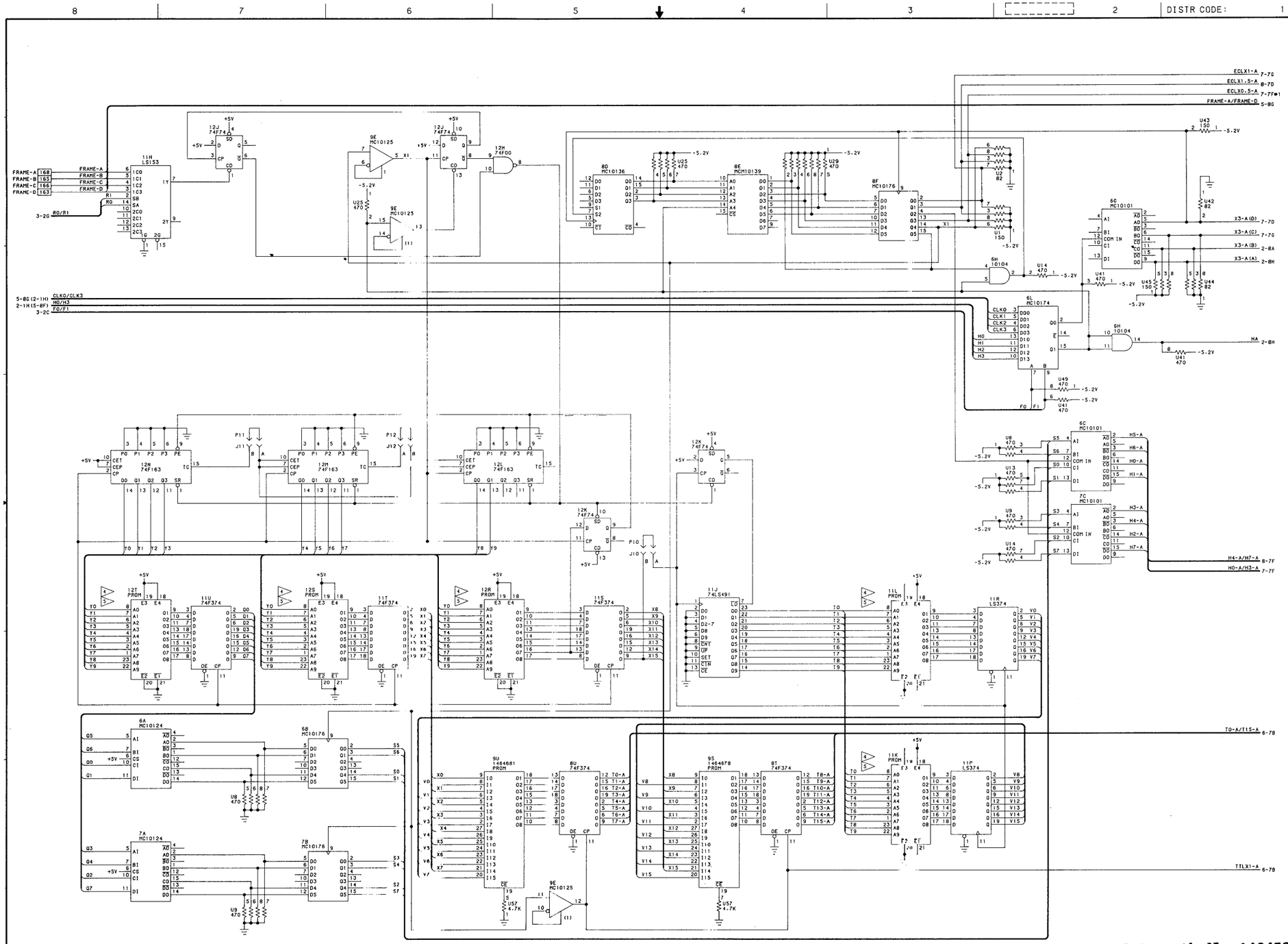
Clock PWA, A11
(Sheet 3 of 9)



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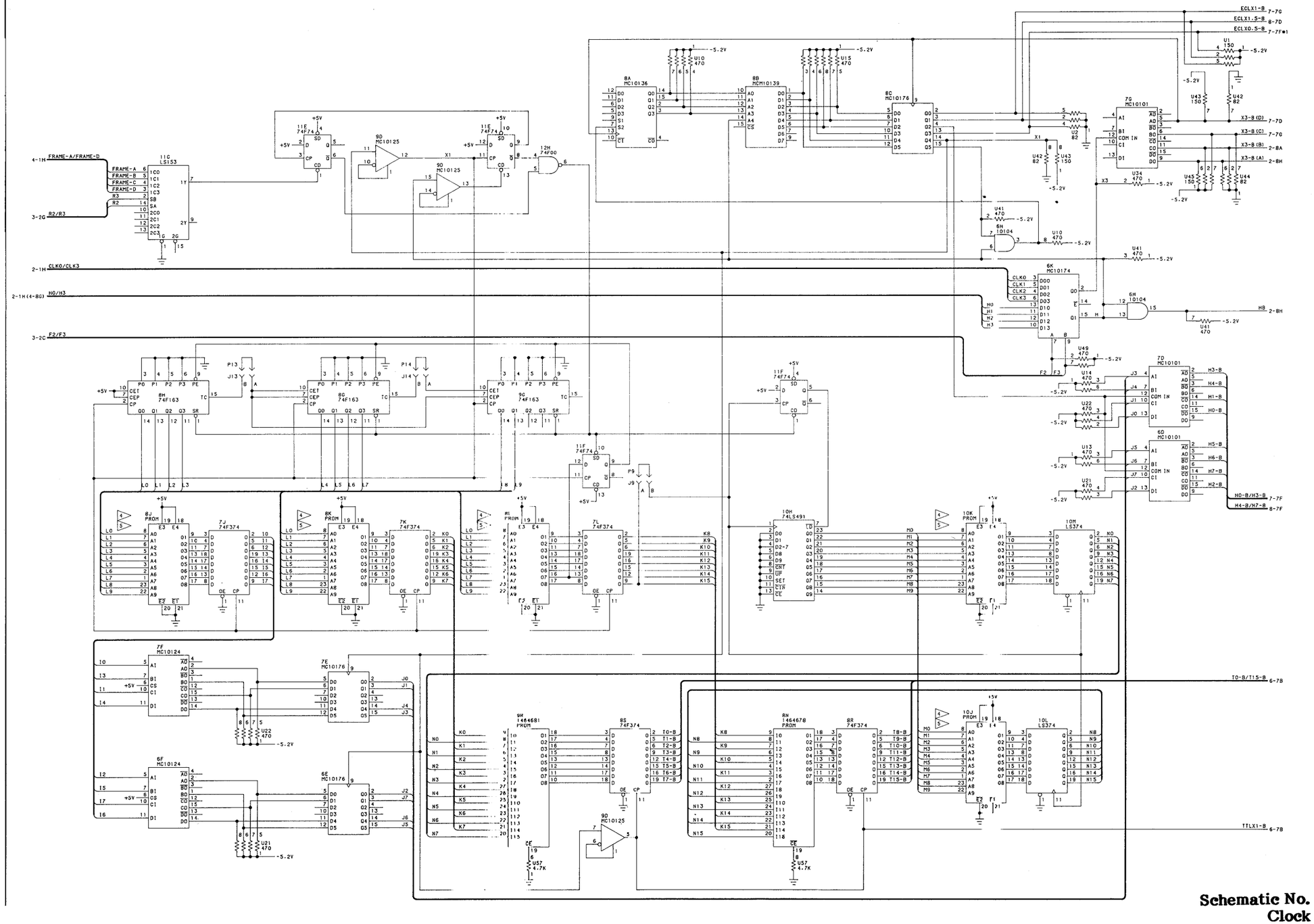
Clock PWA, A11
(Sheet 4 of 9)



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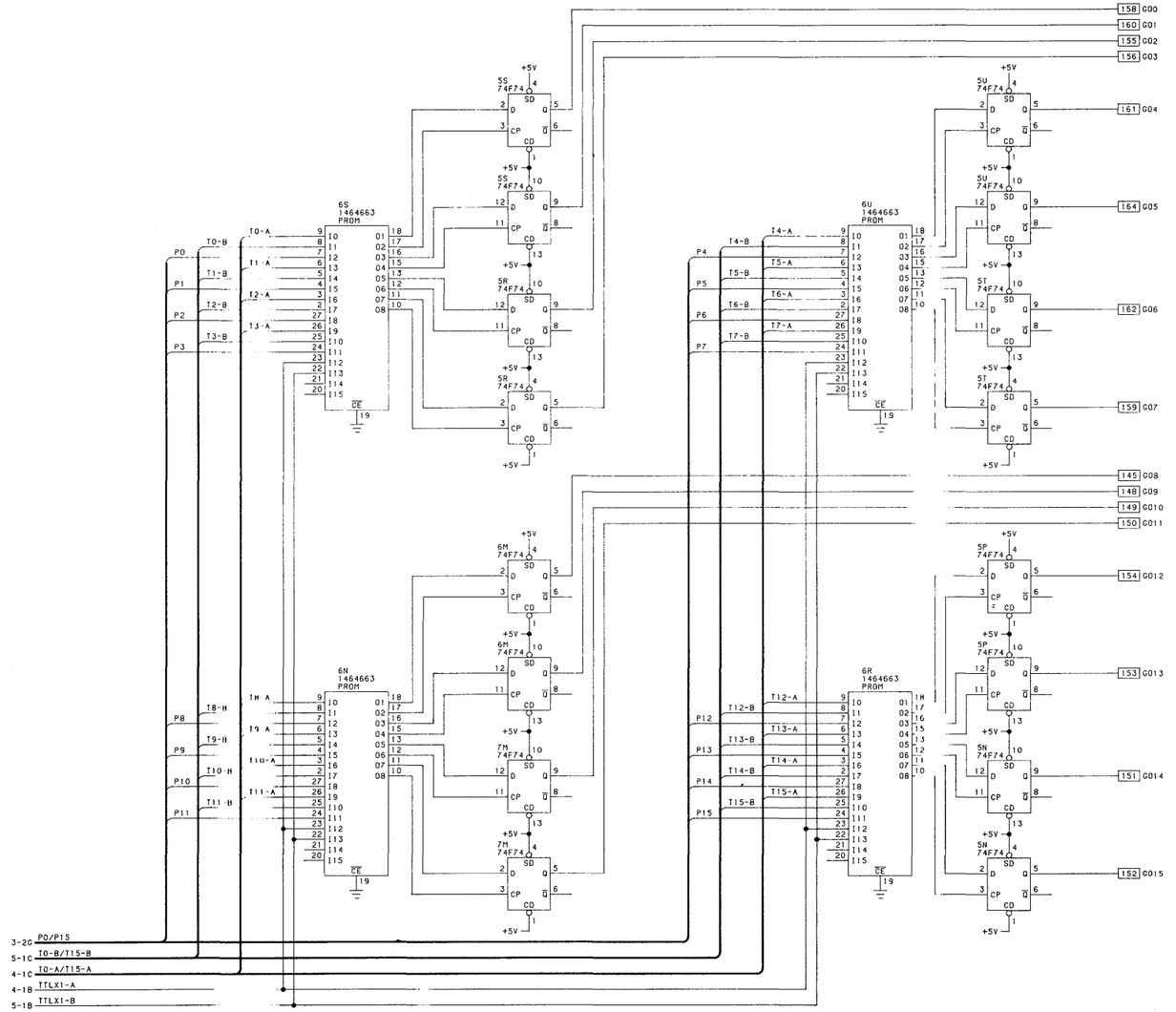
Clock PWA, A11
(Sheet 5 of 9)



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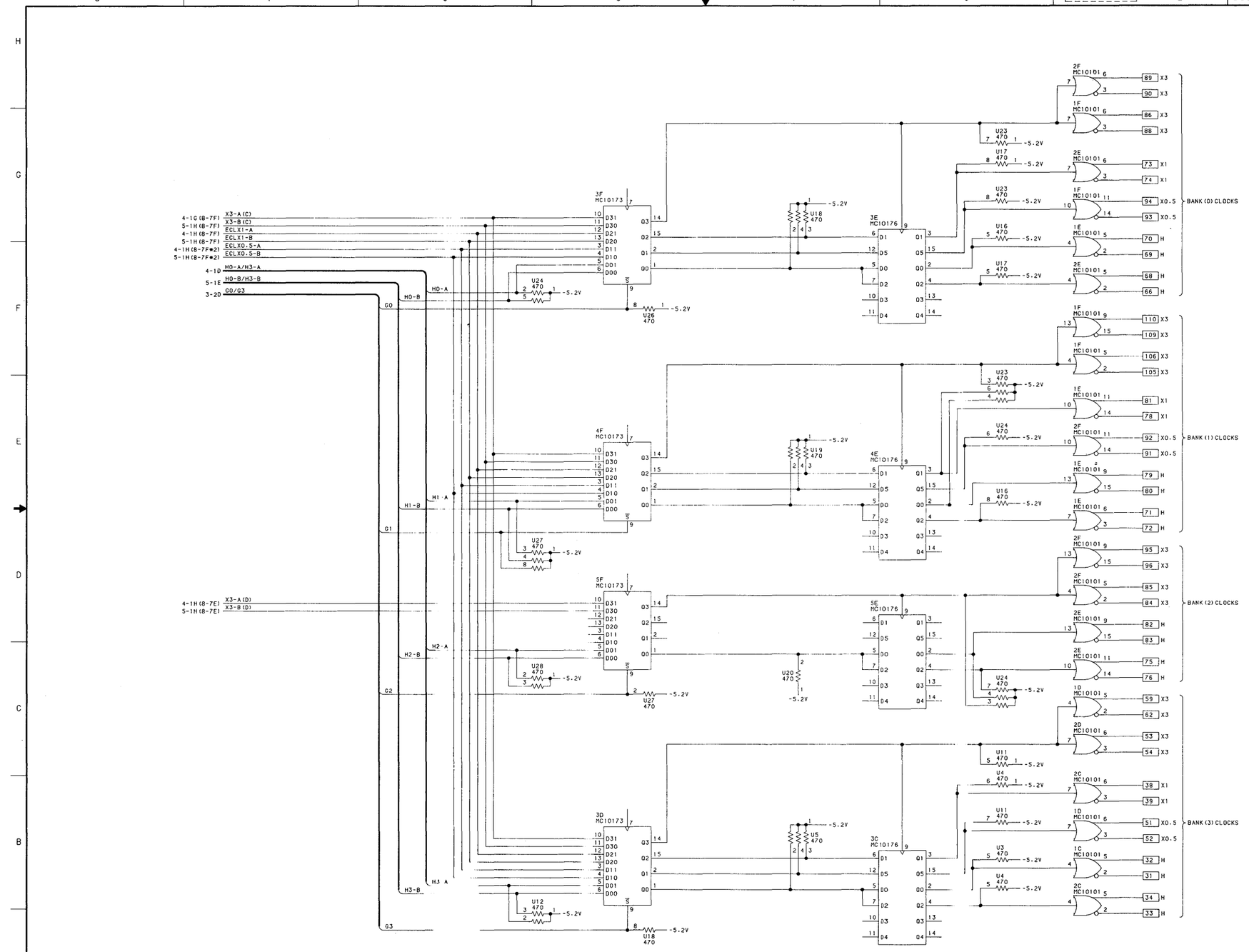
Clock PWA, A11
(Sheet 6 of 9)



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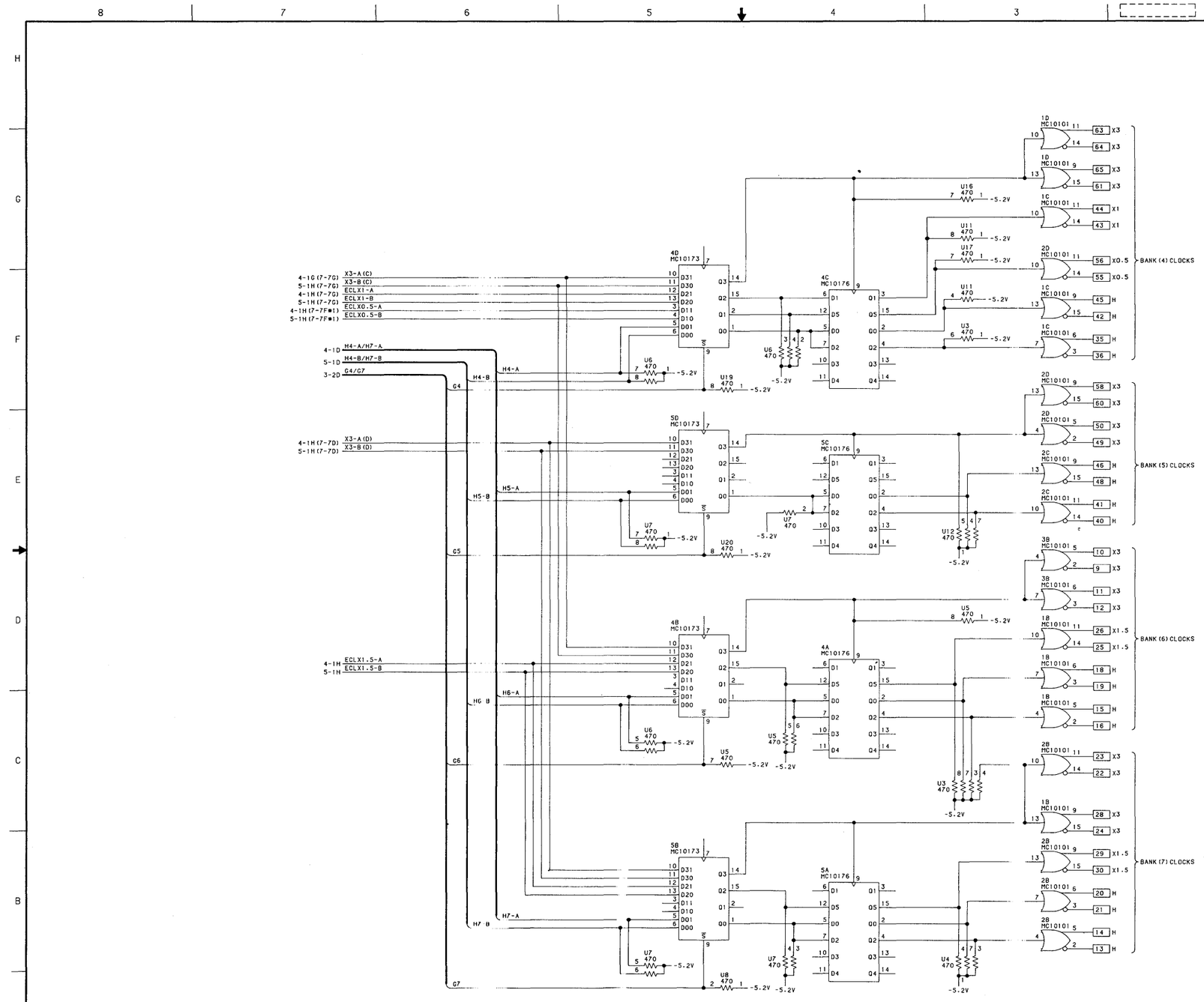
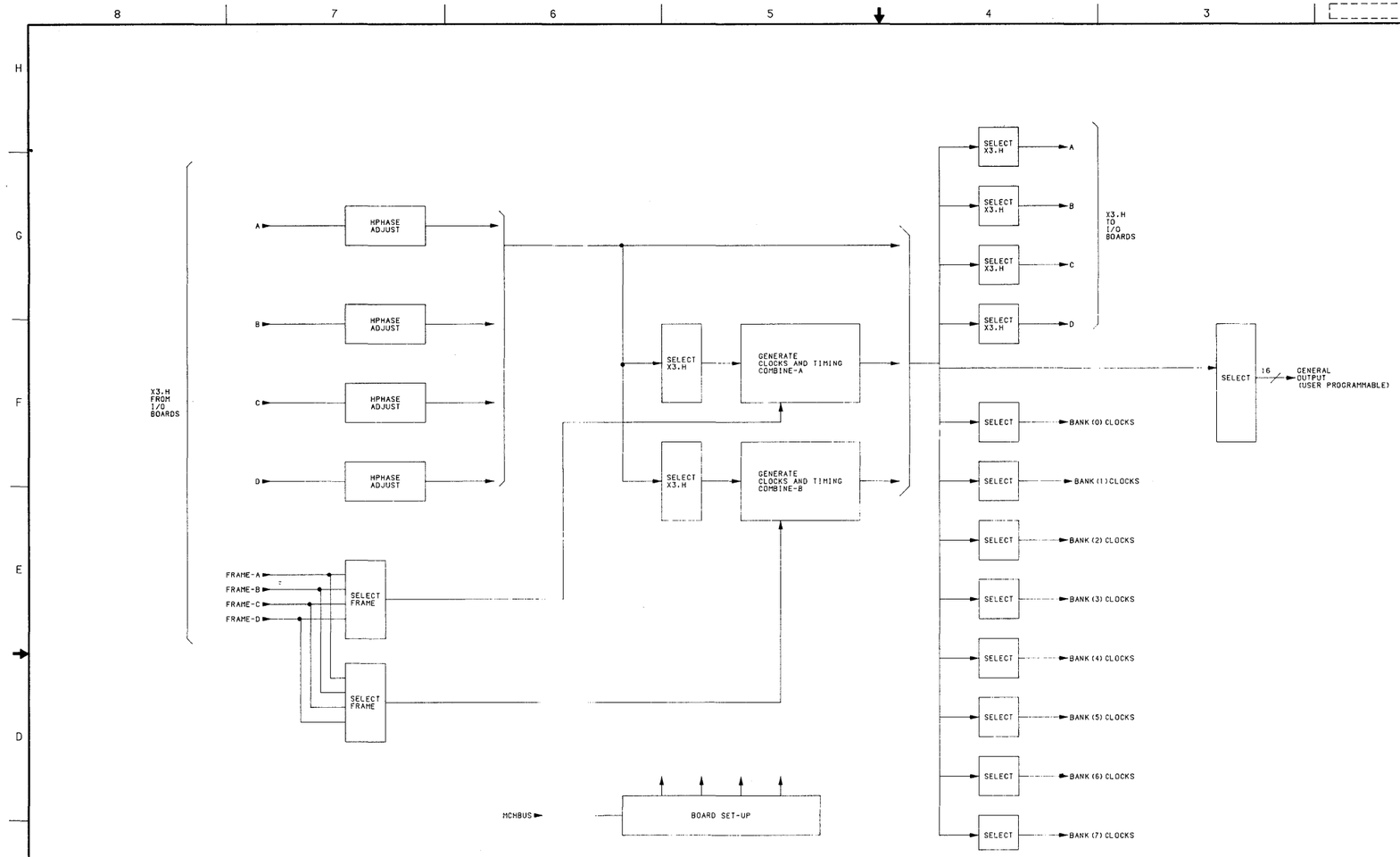
Clock PWA, A11
(Sheet 7 of 9)



Schematic No. 1464530B.
Clock PWA, A11
(Sheet 8 of 9)



	J0	J1	J2	J3	J4	J5	J6	J7
	XX00	XX20	XX40	XX60	XX80	XXA0	XXC0	XXE0
D0	SET CHANNEL (A) HPHASE	SET CHANNEL (B) HPHASE	SET CHANNEL (C) HPHASE	SET CHANNEL (D) HPHASE	SELECT X3.H FOR COMBINE-A 0-I/OA;1-I/OB 2-I/OC;3-I/OD	SELECT FOR BANK (0)	SEL G00	SELECT FRAME FOR COMBINE-A
D1						SELECT FOR BANK (1)	SEL G01	
D2					SELECT X3.H FOR COMBINE-B	SELECT FOR BANK (2)	SEL G02	SELECT FRAME FOR COMBINE-B
D3						SELECT FOR BANK (3)	SEL G03	
D4					SELECT X3.H FOR I/OA 0-SELF 1-COMBINE-A 2-COMBINE-B	SELECT FOR BANK (4)	SEL G04	SPARE
D5						SELECT FOR BANK (5)	SEL G05	
D6					SELECT X3.H FOR I/OB	SELECT FOR BANK (6)	SEL G06	
D7						SELECT FOR BANK (7)	SEL G07	
D8					SELECT X3.H FOR I/OC	SPARE	SEL G08	X
D9							SEL G09	
D10					SELECT X3.H FOR I/OD		SEL G010	
D11							SEL G011	
D12	X	X	X	X	X	X	SEL G012	
D13							SEL G013	
D14							SEL G014	
D15							SEL G015	

X-NOT LATCHED-IN HARDWARE
SPARE-AVAILABLE FOR USE

Schematic No. 1464530B.
Clock PWA, A11
(Sheet 9 of 9)

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1				
2				
3	1464530	SCHEMATIC		A
4				
5	1409670-CA	LABEL, EXTRACTOR ARM		1
6	1409976-AA	INSULATOR, STIFFENER		1
7	1409976-AB	INSULATOR, STIFFENER		1
8	1409997-AA	STIFFENER, PWB		1
9	1409997-AB	STIFFENER, PWB		1
10				
11	1464663-01	PROM ASSY REF: 000-010 DM82S100	6N,R,S,U	4
12	1464666-01	REF: 000-004 MC10139	8B,E	2
13	1465113-01	REF: 000-038 DM87S181 1	8J,12T	2
14	1465114-01	REF: 000-038 DM87S181 1	8K,12S	2
15	1465115-01	REF: 000-038 DM87S181 1	8L,12R	2
16	1464678-01	REF: 000-010 DM82S100	8N,9S	2
17	1464681-01	REF: 000-010 DM82S100	9U,R	2
18	1465116-01	REF: 000-038 DM87S181 1	10J,11K	2
19	1465117-01	PROM ASSY REF: 000-038 DM87S181 1	10K,11L	2
20				
21				
22	064-652	CAPACITOR, CER., 0.01uF, 50V, ± 20%	C49-56	8
23	064-653	CAPACITOR, CER., 0.1uF, 50V, ±20%	C2-48,57-75, 77-127	117
24				
25	037-965	CAPACITOR, TANT., 120uF, 10V, ± 20%	C1,76	2
26				
27				
28	000-152	INTEGRATED CIRCUIT, MC10125	9D,E	2
29	000-153	MC10104	6H	1
30	001-076	MC10174	3L,M,4L,M,6K,6L	6
31	001-077	MC10176	3C,E,N,P,R,S,T, 3U,4A,C,E,N,P	26
			4R,S,T,U,5A,C,E,6B, 6E,7B,E,8C,F	
32	002-050	MC10101	1B,C,D,E,F,L,M, 2B,C,D,E,F,3B, 6C,D,G,7C,D,G	19
33	002-329	74F163	8G,H,9G,12L,M, 12N	6
34	002-992	74LS491	10H,11J	2
35	587-550	INTEGRATED CIRCUIT, MC10136	3G,H,J,K,4G,H,J, K,5G,H,J,K,8A,D	14

LM-1465111

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1465111 SHEET 2 OF 3	REV —

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
36	589-512	INTEGRATED CIRCUIT, MC10173	3D,F,4B,D,F,5B, 5D,F	8
37	589-823	74LS138	2U	1
38	589-824	74LS153	11G,H	2
39	589-920	MC10231	2G,H,J,K,5L,M	6
40	590-326	MC10131	2L,M	2
41	590-330	MC10115	1G,J	2
42	590-564	10124DCQR	2N,P,R,S,T,6A,F, 7A,F	9
43	590-584	74LS244	1P,T,U	3
44	590-586	74LS374	1N,R,S,10L,M,11P, R	7
45	590-935	74F00	12H	1
46	590-940	74F74	5N,P,R,S,T,U,6M, 7M,11E,F,12J,K	12
47	590-947	INTEGRATED CIRCUIT, 74F374	7J,K,L,8R,S,T,U, 11S,T,U	10
48				
49				
50				
51	039-178	NETWORK, RESISTOR, 150 OHMS	U1,43,45	3
52				
53	039-208	NETWORK, RESISTOR, 82 OHMS	U2,42,44	3
54	039-264	NETWORK, RESISTOR, 4.7K OHMS	U57	1
55	039-329	NETWORK, RESISTOR, 470 OHMS	U3-29,32-34, 38-41,46-56	45
56	039-378	NETWORK, RESISTOR, 47 OHMS	U30,31,36,37	4
57	039-392	NETWORK, RESISTOR, 100 OHMS	U35	1
58				
59	143-981	JACK, P.C., TIP	A & B OF J1-14	28
60				
61				
62	173-024	TERMINAL, TURRET	GND	4
63				
64	471-060	SCREW, PAN HD., XREC, #4-40 X .250 LG		6
65				
66	493-005	NUT, HEX, NYLON LOCK, #4-40		6
67				
68	530-477	ENCLOSURE, PART, CARD		2
69				
70	582-280	I.C., MTG. HDW., 24 PIN	REF:8J,K,L,10J,K,11K,L, 12R,S,T	10
71	582-281	I.C., MTG. HDW., 28 PIN	REF:6N,R,S,U,8N,9R,S,U	8
72	582-330	I.C., MTG. HDW., 14 PIN	REF:5N,P,R,S,T,U,6M,7M, 11E,F,12H,J,K	13
73	582-331	I.C., MTG. HDW., 16 PIN	REF:1B,C,D,E,F,G,J,L,M, 2B,C,D,E,F,G,H,J,K, 2L,M,N,P,R,S,T,U,3B,C,D,E,F,G, 3H,J,K,L,M,N,P,R,S,T,U,4A,B,C, 4D,E,F,G,H,J,K,L,M,N,P,R,S,T,U, 5A,B,C,D,E,F,G,H,J,K,L,M,6A,B, 6C,D,E,F,G,H,K,L,7A,B,C,D,E,F, 7G,8A,B,C,D,E,F,G,H,9D,E,G,11G, H,12L,M,N	106
74	582-333	I.C., MTG. HDW., 20 PIN	REF:1N,P,R,S,T,U,7J,K,L,8R,S,T, 8U,10L,M,11P,R,S,T,U	20
75	582-416	I.C., MTG. HDW., 24 PIN	REF:10H,11J	2
76				

LM-1465111

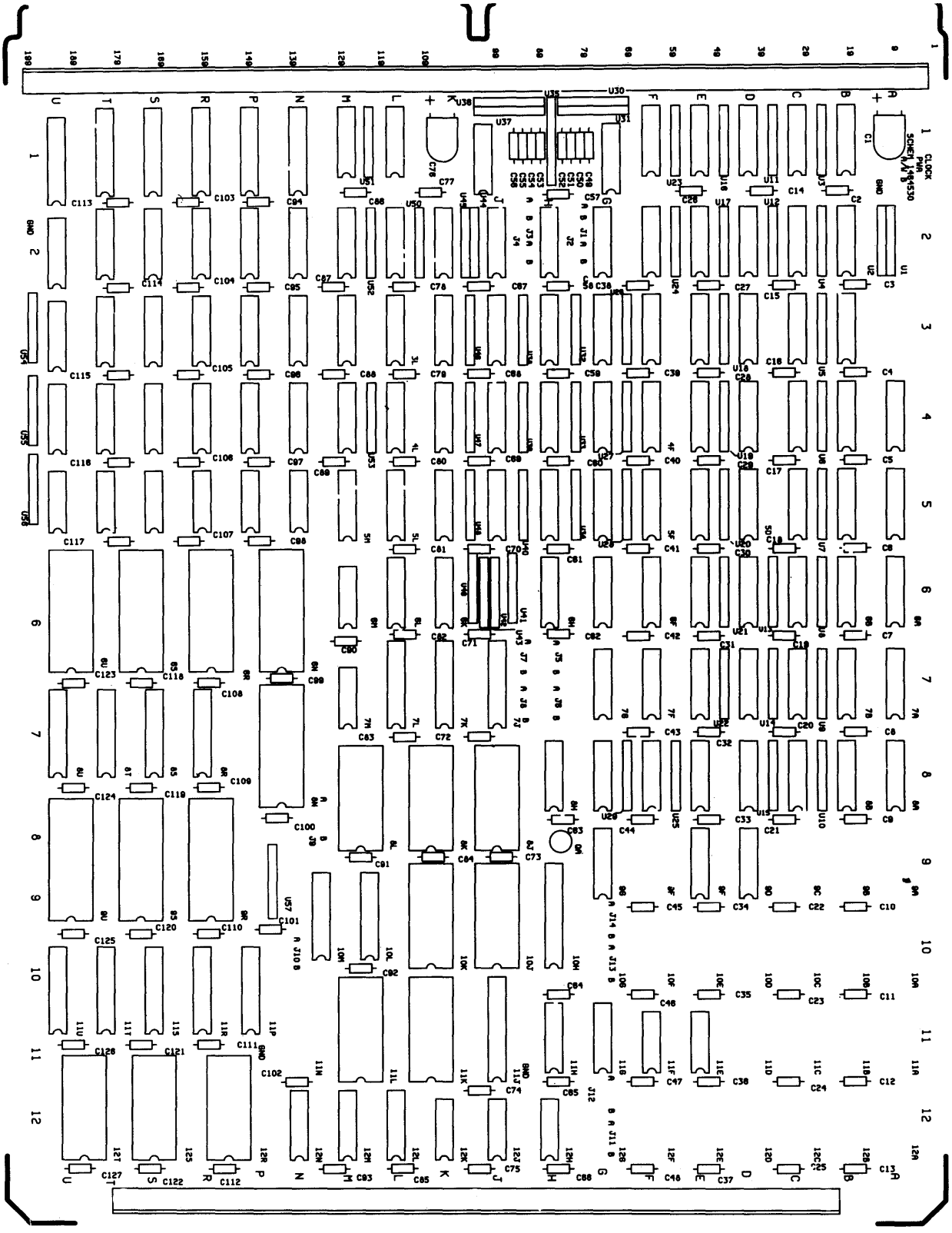
AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM-1465111 SHEET 3 OF 3	REV —

ITEM NO.	PART NUMBER		DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
77					
78					
79	602-044		SHORTING PLUG, RED	J1-14	14

NOTES:

1. STATIC SENSITIVE DEVICE, SPECIAL HANDLING REQUIRED PER AMPEX STD HE1-1.

LM-1465111



Assembly No. 1465111-01–. Clock PWA, A11, PAL

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1464489	PRINTED WIRING BOARD		-01
2				
3	1464490	SCHEMATIC		(-)
4				
5	1409670-CB	LABEL, EXTRACTOR ARM		1
6	1409976-AA	INSULATOR, STIFFENER		1
7	1409976-AB	INSULATOR, STIFFENER		1
8	1409997-AA	STIFFENER, PWB		1
9	1409997-AB	STIFFENER, PWB		1
10				
11				
12	1464566-01	PROM ASSY REF: 000-010 82S100	3T	1
13	1464567-01	REF: 002-117 D27128-25 [1]	4M	1
14	1464568-01		4P	1
15	1464569-01		5M	1
16	1465088-01	REF: 002-117 D27128-25 [1]	5P	1
17	1465089-01	REF: 000-010 82S100	6E	1
18	1465090-01	PROM ASSY REF: 000-010 82S100	6G	1
19				
20				
21	064-314	CAPACITOR, CER., 1.0uF, 50V, ±20%	C98	1
22	064-653	CAPACITOR, CER., 0.1uF, 50V, ±20%	C2-9,14,19-25,34-43,50,51,53-57,59-68,70-97,99	72
23	064-667	CAPACITOR, CER., 68pF, 100V, ±5%	C10-13,15-18,26-29,30-33,46-49	20
24				
25				
26	037-892	CAPACITOR, TANT., 47uF, 20V, ±20%	C45,58	2
27	037-965	CAPACITOR, TANT., 120uF, 10V, ±20%	C1,44	2
28				
29	581-567	DIODE, LED, RED	DS1-24	24
30				
31				
32	000-044	INTEGRATED CIRCUIT, WD1510-01 [1]	7A,9A	2
33	000-047	AM9519-1 [1]	2M,P	2
34	000-133	74S373	6K,R	2
35	000-138	74LS195	3P,R	2
36	000-148	INTEGRATED CIRCUIT, AM2966PCB [1]	7S,8H	2

LM-1464488

AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM- 1464488 SHEET 2 OF 3	REV —

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
37	001-042	INTEGRATED CIRCUIT, DS3692	2D,E,G,3D,E	5
38	001-054	74LS21	2L	1
39	001-061	DS1489	2J	1
40	001-953	DS1488	1J	1
41	001-977	MC68B50 1	3H,J	2
42	002-917	AM8253-5 1	2S	1
43	002-955	X2816AD-45 1	6T	1
44	589-369	74LS156	2C,3C	2
45	589-814	74LS04	2K	1
46	589-815	74LS08	3S	1
47	589-816	74LS10	3N	1
48	589-820	74LS74	7D,J,8D	3
49	589-823	74LS138	1M,N,P,T,2U,3F,L, 4H,6J	9
50	589-824	74LS153	9G,H	2
51	589-825	74LS157	3G,6S,7R	3
52	589-837	74S00	7H	1
53	589-838	74S04	7F	1
54	589-930	74LS27	6A	1
55	589-931	74LS30	3M	1
56	589-933	74LS161	8F,9F	2
57	590-193	9637A	1CA,1CB,1EA,1EB, 1G	5
58	590-328	74LS32	2T,7G,8G,9D	4
59	590-335	74LS273	4E,5E	2
60	590-496	74LS151	1A,B	2
61	590-565	74LS373	6D	1
62	590-584	74LS244	4C,5B,C	3
63	590-586	74LS374	3B,4D,5D,7T,U	5
64	590-725	NE555	8T	1
65	590-847	74LS245	1R,S,6L,P,7L,P	6
66	590-866	Z8002A 1	7M	1
67	590-868	74S244	1U,7K	2
68	590-932	CDP1854ACD	7B,9B	2
69	590-989	INTEGRATED CIRCUIT, TMS4164-15 1	8J,K,L,M,N,P,R,S, 9J,K,L,M,N,P,R,S	16
70	595-016	OSCILLATOR, HS-100P, 4.9152 MHz	7E	1
71	570-630	PWR CONVERTER, PM671	1K	1
72				
73	066-668	RESISTOR, C.F., 4.7K OHMS, 1/4W, 5%	R1,2,6	3
74	066-673	RESISTOR, C.F., 1M OHMS, 1/4W, 5%	R3,5	2
75	066-818	RESISTOR, C.F., 470 OHMS, 1/4W, 5%	R4	1
76				
77	039-027	RESISTOR, NETWORK, 470 OHMS	3A	1
78	039-163	470	U12,15	2
79	039-164	4.7K	U5,6,8,9,11,16,17	7
80	039-241	4.7K	U1,3	2
81	039-264	RESISTOR, NETWORK, 4.7K OHMS	U13,14	2

LM-1464488

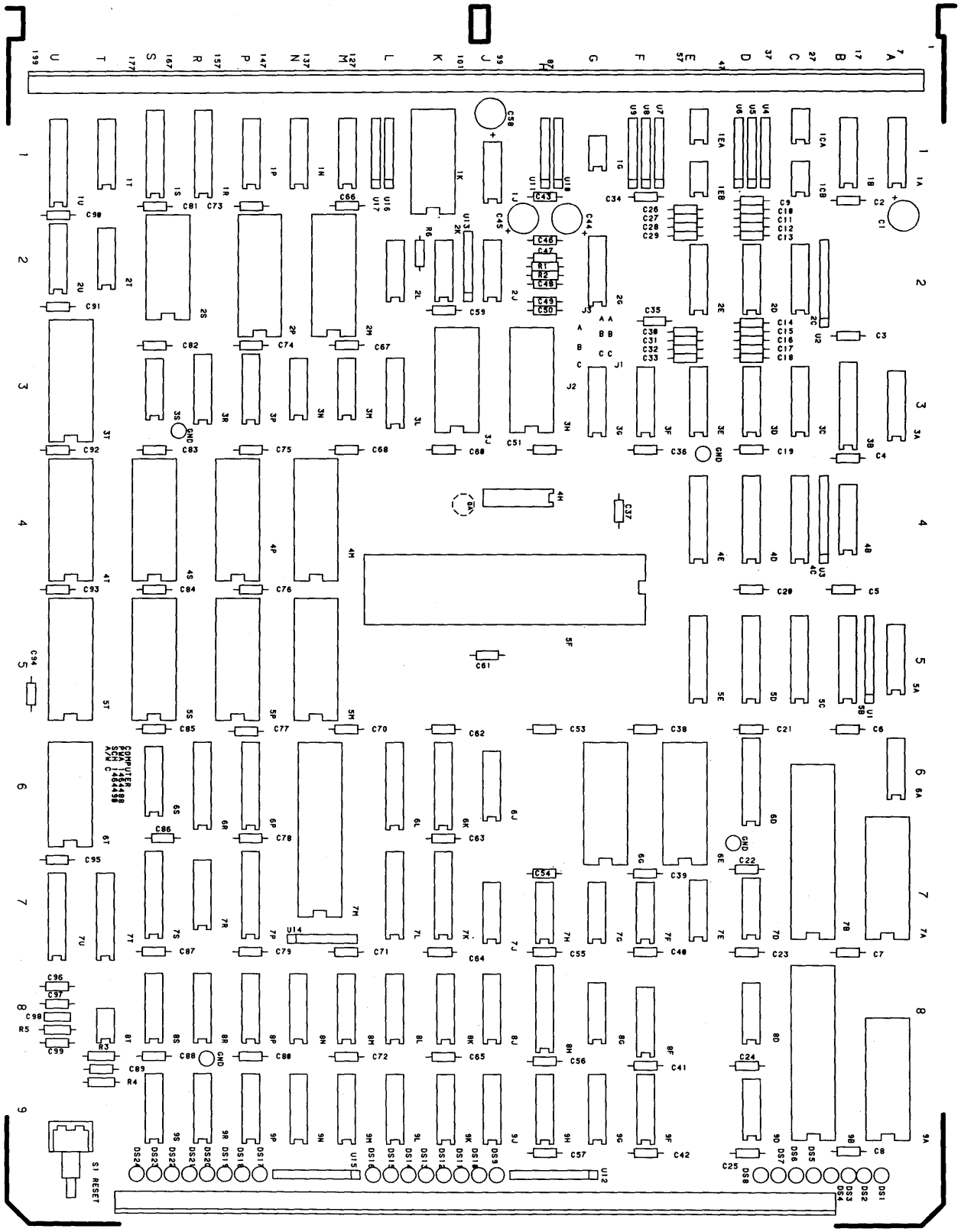
AMPEX | Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO. 92739	LIST OF MATERIALS	LM- 1464488 SHEET 3 OF 3	REV —

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
82	039-294	RESISTOR, NETWORK, 1K OHMS	U2	1
83	039-388	RESISTOR, NETWORK, 180 OHMS	U4,7,10	3
84				
85				
86				
87	119-492	SWITCH, ROCKER, 8 POS.	4B,5A	2
88	119-855	SWITCH, PUSH BUTTON, SPDT	S1	1
89				
90	143-981	JACK, P.C., TIP	REF: J1-A,B,C; J2-A,B,C; J3-A,B,C	9
91				
92	173-024	TERMINAL, TURRET	GND	4
93				
94	471-060	SCREW, PAN HD., XREC, #4-40 X .250 LG		6
95				
96	493-005	NUT, HEX, NYLON, LOCK, #4-40		6
97	530-477	ENCLOSURE PART, CARD, INSERTER/EXTRACTOR		2
98				
99				
100				
101	582-280	I.C., MTG. HDW., 24 PIN	REF:2S,3H,J,6T	4
102	582-281	28 PIN	REF: 2M,P,3T,4M,P,S,T,5M, 5P,S,T,6E,G,7A,9A	15
103	582-282	40 PIN	REF:7B,M,9B	3
104	582-329	8 PIN	REF: 1CA,1CB,1EA,1EB,1G, 8T	6
105	582-330	14 PIN	REF: 1J,2J,K,L,T,3M,N,S,6A, 7D,F,G,H,J,8D,G,9D	17
106	582-331	16 PIN	REF: 1A,B,M,N,P,T,2C,D,E, 2G,U,3C,D,E,F,G,L,P,R, 4H,6J,S,7R,8F,J,K,L,M,N,P,R,S, 9F,G,H,J,K,L,M,N,P,R,S	43
107	582-333	20 PIN	REF: 1R,S,U,3B,4C,D,E,5B, 5C,D,E,6D,K,L,P,R, 7K,L,P,S,T,U,8H	23
108	582-364	I.C., MTG. HDW., 64 PIN	REF:5F	1
109				
110				
111				
112				
113	602-044	SHORTING PLUG, RED	J1,2,3	3

NOTES:

1. STATIC SENSITIVE, SPECIAL HANDLING REQUIRED PER AMPEX STD HE1-1.

LM-1464488



Assembly No. 1464488-01—. Computer PWA, A27

NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTANCE VALUES ARE IN OHMS.1/4W.5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. STATIC SENSITIVE DEVICE SPECIAL HANDLING REQUIRED PER AMPEX STD HE1-1.
4. SEE SHEET 7 FOR +12V.

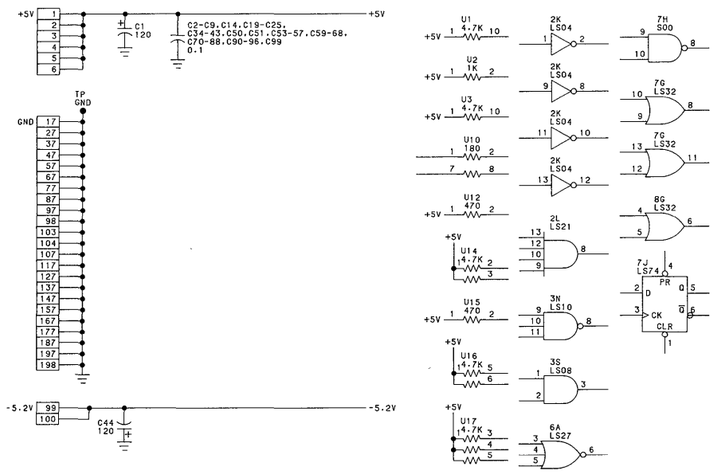
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C99	C52.C69
DS24	
J3	
P3	
R6	
S1	
U17	

I.C. LIST

REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	GND PIN	POWER PINS +5	-5	+12	-12
7A.9A [3]	000-044	WD1510-01	1	16			
2M.P [3]	000-047	AM9519-1	14	28			
6D	590-565	74LS373	10	20			
6K.R	000-133	74S373	10	20			
3P.R	000-138	74LS195	8	16			
2D.E.G.3D.E	001-042	DS3692	5.8	1			
2L	001-054	74LS21	7	14			
2J	001-061	DS1489	7	14			
1J	001-953	DS1488	7			14	1
3H.J [3]	001-977	MC68B50	1	12			
2S [3]	002-917	AM8253-5	12	24			
6T [3]	002-955	X2816AD-45	12	24			
2C.3C	589-369	74LS156	8	16			
2K	589-814	74LS04	7	14			
3S	589-815	74LS08	7	14			
3N	589-816	74LS10	7	14			
7D.J.8D	589-820	74LS74	7	14			
1M.N.P.T.22U.3F.L.4H.6J	589-823	74LS138	8	16			
9G.H	589-824	74LS153	8	16			
3G.6S.7R	589-825	74LS157	8	16			
7M	589-837	74S00	7	14			
7F	589-838	74S04	7	14			
6A	589-930	74LS27	7	14			
3M	589-931	74LS30	7	14			
8F.9F	589-933	74LS161	8	16			
1CA.1CB.1EA.1EB.1C	590-193	9637A	4	1			
7S.8H [3]	000-148	AM2966PCB	10	20			
2T.7G.8G.9D	590-328	74LS32	7	14			

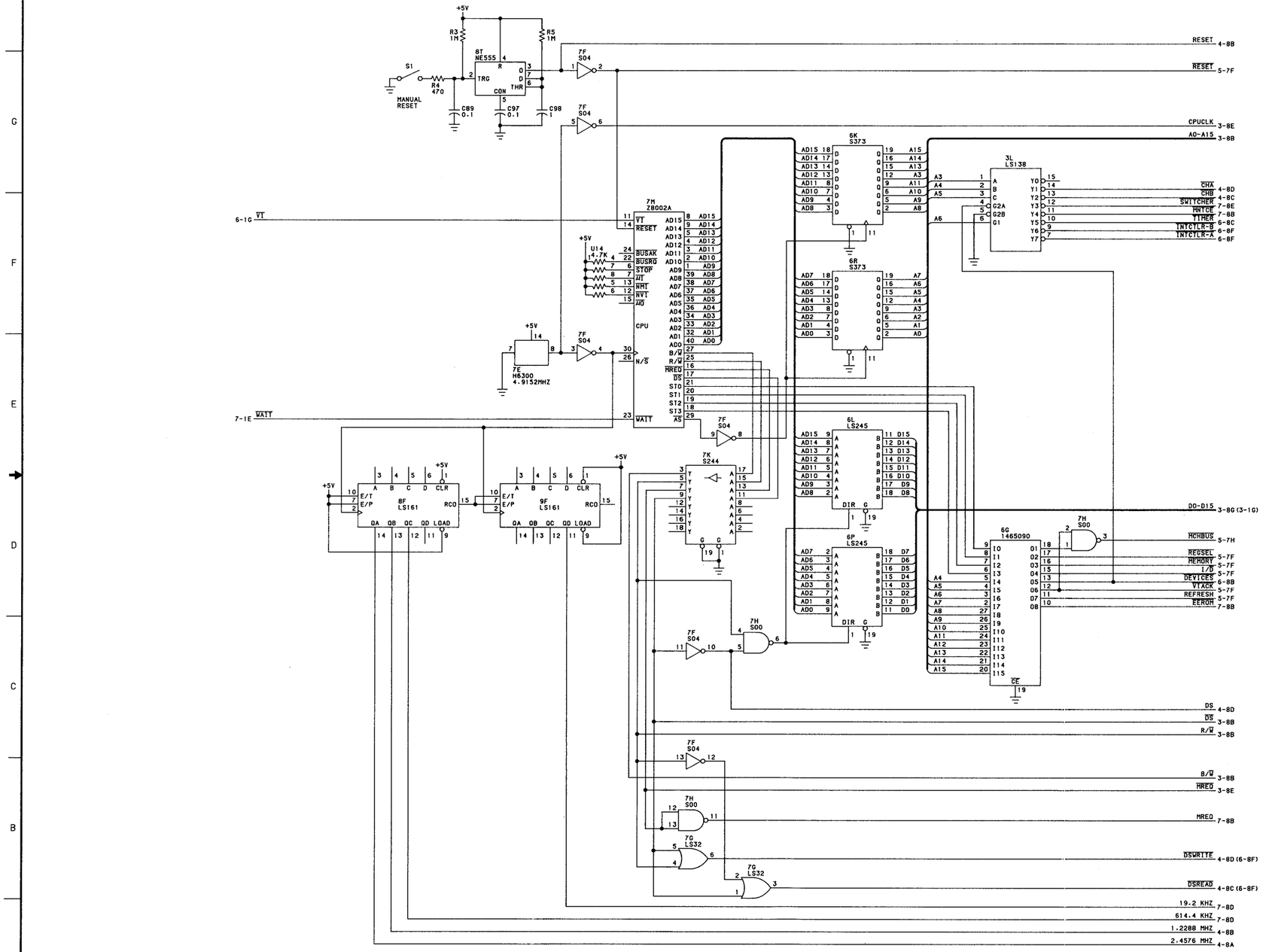
I.C. LIST

REFERENCE DESIGNATION	AMPEX P/N	VENDOR P/N	GND PIN	POWER PINS +5	-5	+12	-12
4E.5E	590-335	74LS273	10	20			
1A.B	590-496	74LS151	8	16			
4C.5B.C	590-584	74LS244	10	20			
3B.4D.5D.7T.U	590-586	74LS374	10	20			
8T	590-725	NE555	1	8			
1R.S.6L.P.7L.P	590-847	74LS245	10	20			
7M [3]	001-991	Z8002A	31	10			
1U.7K	590-868	74S244	10	20			
7B.9B	590-932	CDP1854ACD	3	1			
8J.K.L.M.N.P.R.S [3]	590-989	TMS4164-15	16	8			
9J.K.L.M.N.P.R.S							
5F [3]	003-068	ADSP.1016JD	45.46.47	48.49			
7E	595-016	H6300	7	14			
1K [4]	570-630	PM671				11.14	2.23
3T	1464566	82S100	14	28			
6E	1465089	82S100	14	28			
6C	1465090	82S100	14	28			
4M [3]	1465097	27128	14	28			
5M [3]	1465098	27128	14	28			
4S [3]	1465100	27128	14	28			
5S [3]	1465101	27128	14	28			
RESISTOR NETWORK							
3A	039-027						
U12.15	039-163						
U5.6.8.9.11.16.17	039-164						
U1.3	039-241						
U13.14	039-264						
U2	039-294						
U4.7.10	039-388						

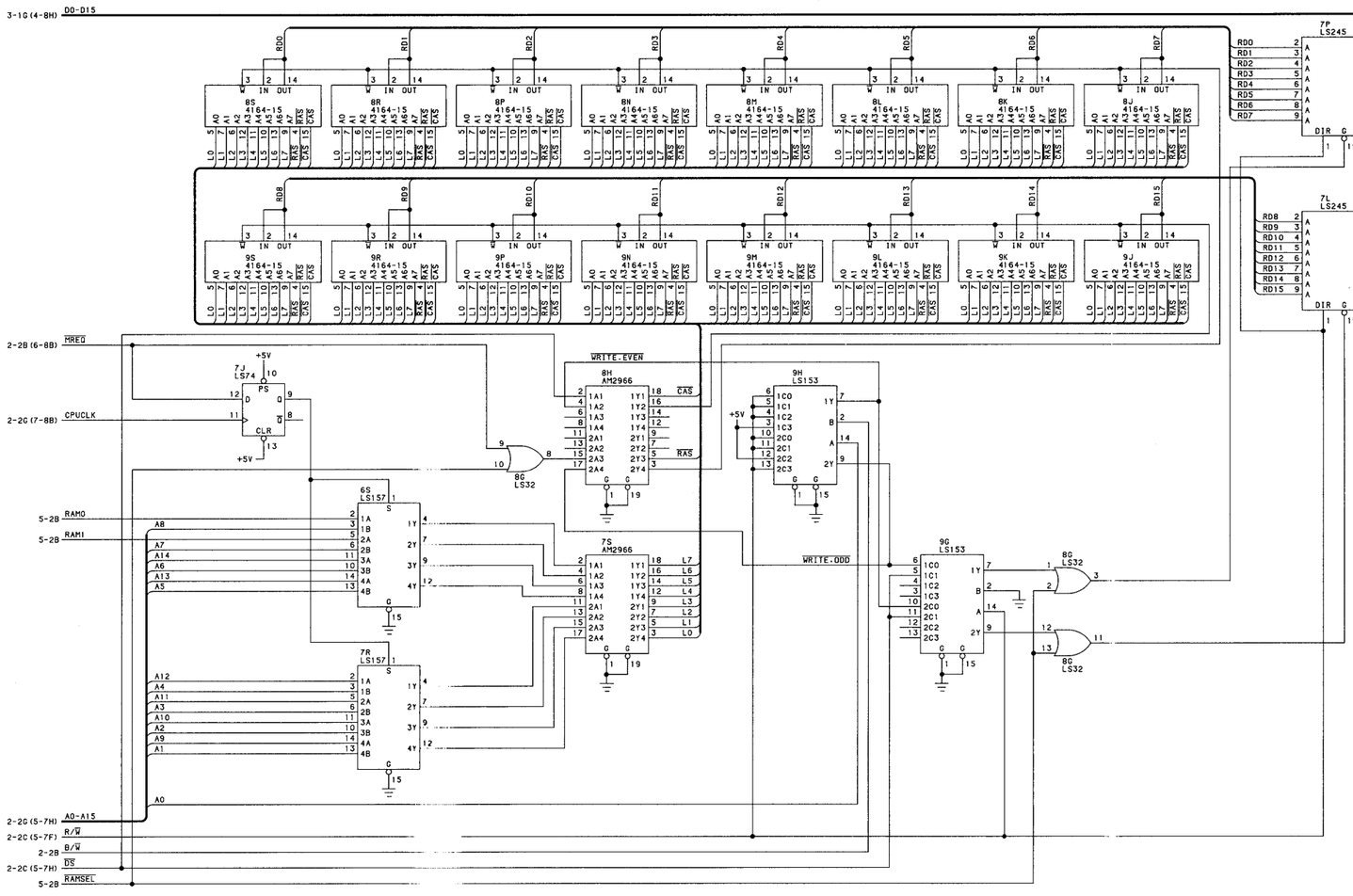


1464488	CONC
NEXT ASSY	USED ON
APPLICATION	

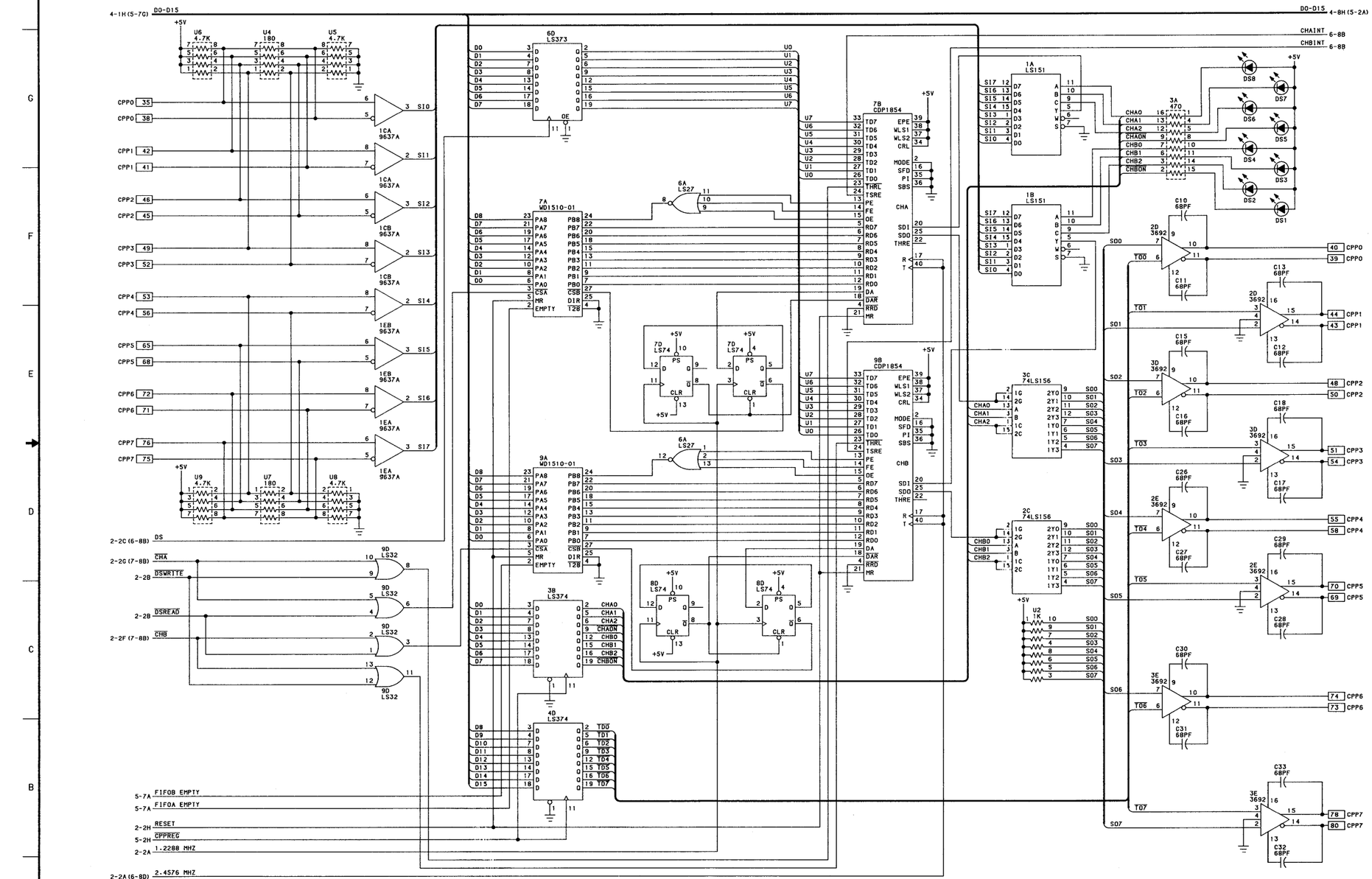
Schematic No. 1464490C.
Computer PWA, A27
(Sheet 1 of 8)



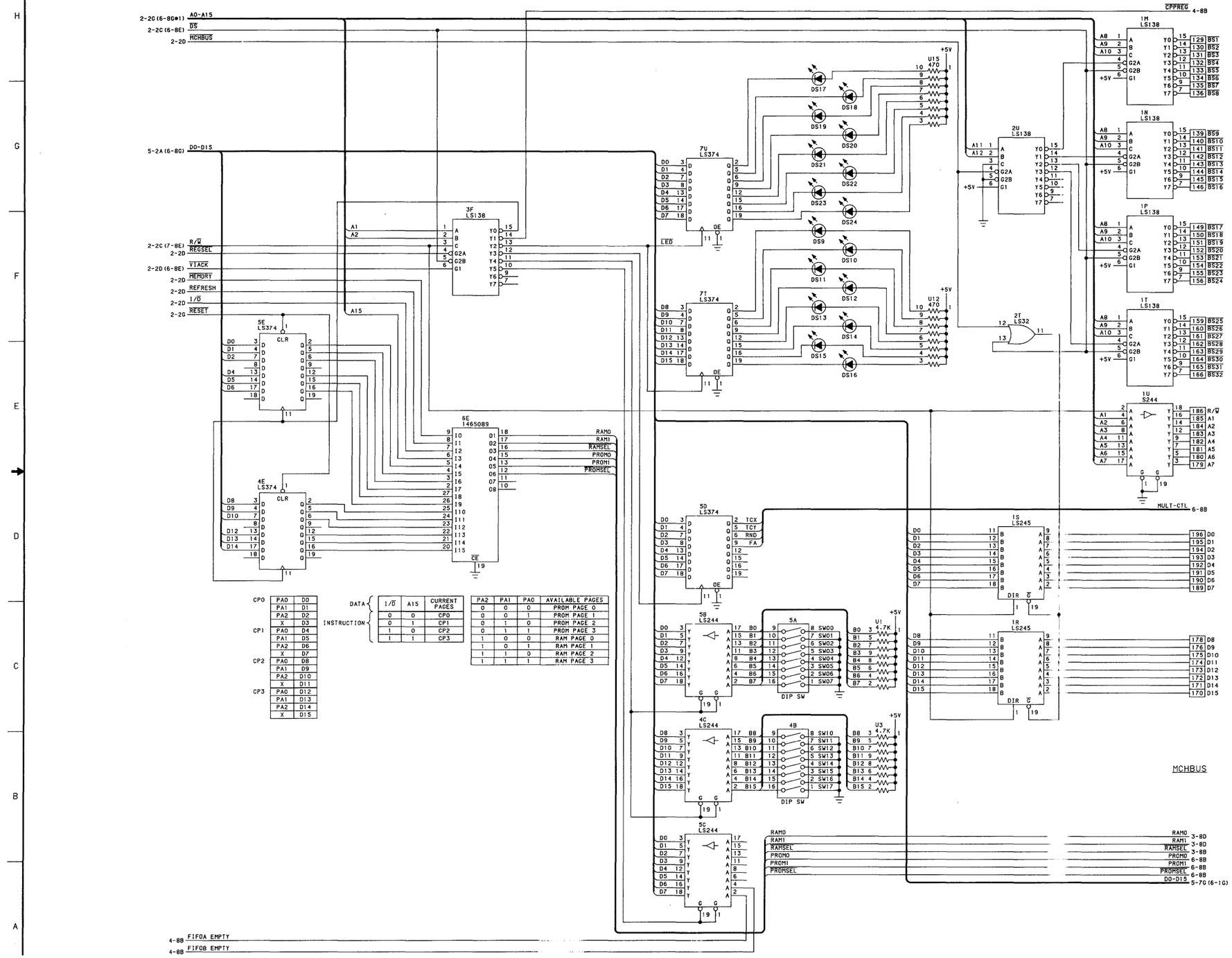
Schematic No. 1464490C.
Computer PWA, A27
(Sheet 2 of 8)



Schematic No. 1464490C.
Computer PWA, A27
(Sheet 3 of 8)



Schematic No. 1464490C.
Computer PWA, A27
(Sheet 4 of 8)



CP0	PA0	D0
	PA1	D1
	PA2	D2
	X	D3
CP1	PA0	D4
	PA1	D5
	PA2	D6
	X	D7
CP2	PA0	D8
	PA1	D9
	PA2	D10
	X	D11
CP3	PA0	D12
	PA1	D13
	PA2	D14
	X	D15

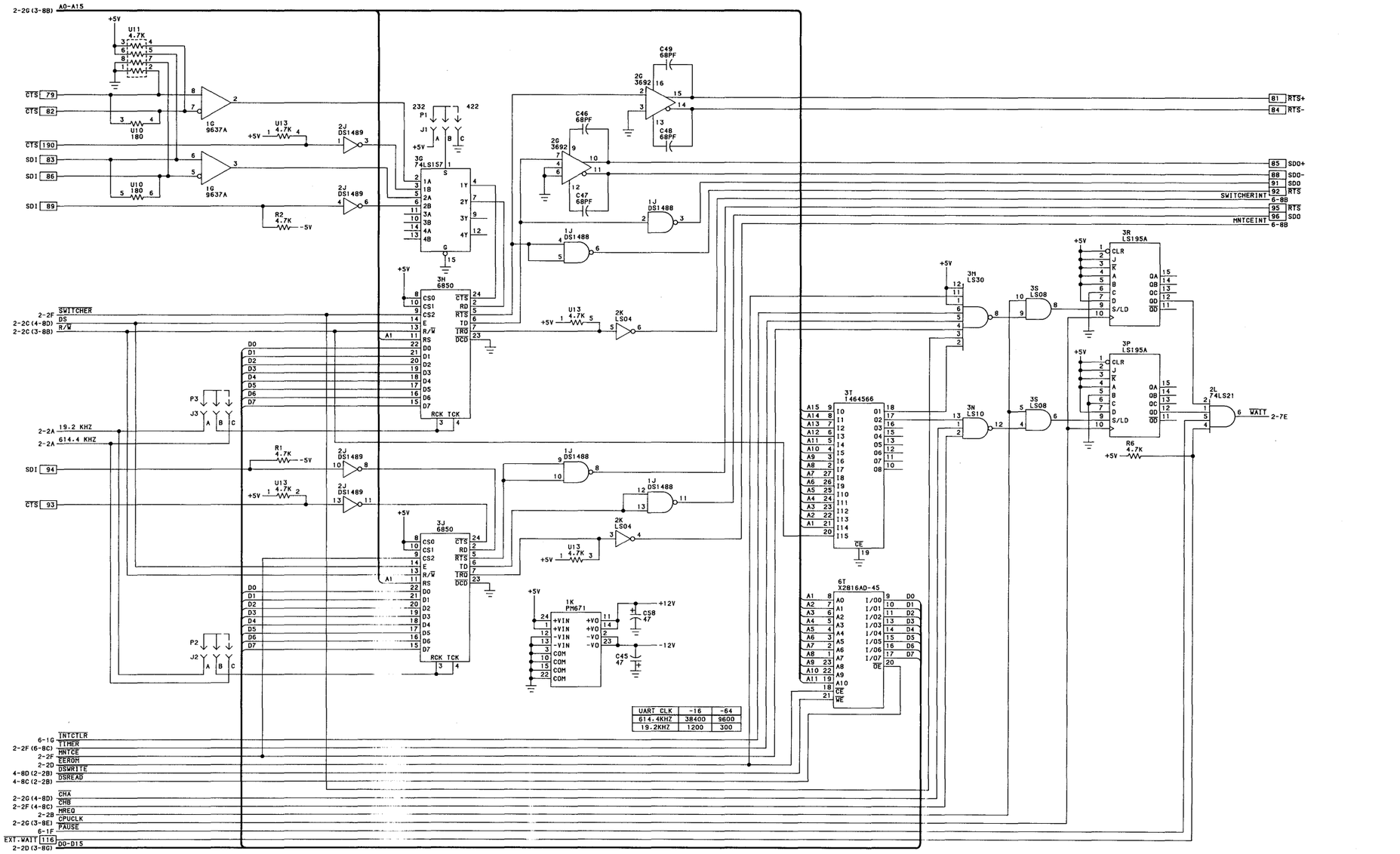
DATA / INSTRUCTION

I/O	A15	CURRENT PAGES
0	0	CP0
0	1	CP1
1	0	CP2
1	1	CP3

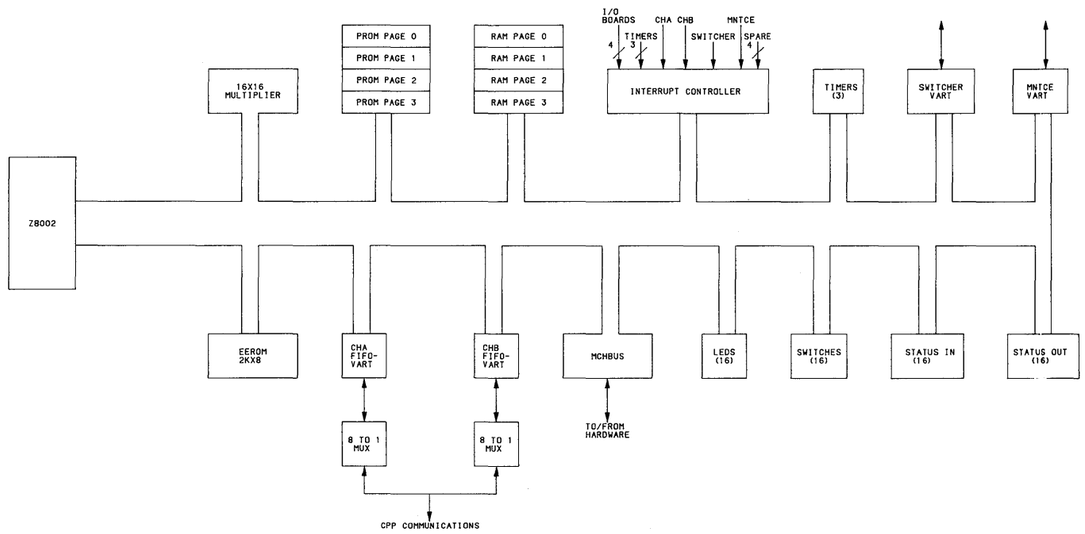
PA2	PA1	PA0	AVAILABLE PAGES
0	0	0	PROM PAGE 0
0	0	1	PROM PAGE 1
0	1	0	PROM PAGE 2
0	1	1	PROM PAGE 3
1	0	0	RAM PAGE 0
1	0	1	RAM PAGE 1
1	1	0	RAM PAGE 2
1	1	1	RAM PAGE 3

Schematic No. 1464490C.
Computer PWA, A27
(Sheet 5 of 8)

Schematic No. 1464490C.
Computer PWA, A27
(Sheet 6 of 8)



Schematic No. 1464490C.
Computer PWA, A27
(Sheet 7 of 8)



ADDRESS	READ	WRITE
DF76	SPARE	STATUS OUT
DF74	SPARE	LEDS
DF72	STATUS IN	CPP REG
DF70	SWITCH	PAGE REG

EEROM 2KX8	C800-D7FF

MCHBUS			
BOARD#	ADDRESS	IDENTITY	
	FFXX		
	FEXX		
	FDXX		
	FCXX		
	FBXX		
	FAXX		
	F9XX		
	F8XX		
	F7XX		
	F6XX		
	F5XX		
	F4XX		
	F3XX		
	F2XX		
	F1XX		
	F0XX		
	EFXX		
	EEXX		
	EDXX		
	ECXX		
	EBXX		
XA11	EAXX	CLOCK	
XA10	E9XX	KEYER	4-CHANNEL ONLY
XA9	E8XX	KEYER	
XA8	E7XX	ADDER	
XA7	E6XX	CUTTER	4-CHANNEL ONLY
XA6	E5XX	CUTTER	
XA5	E4XX	CUTTER	
XA4	E3XX	I/O-D	4-CHANNEL ONLY
XA3	E2XX	I/O-C	4-CHANNEL ONLY
XA2	E1XX	I/O-B	
XA1	E0XX	I/O-A	

DEVICE	ADDRESS	READ	WRITE
INTCTLR-A	DFFE	READ STATUS REG	LD COMMAND REG
	DFFC	READ DATA	WRITE DATA
INTCTLR-B	DFF6	READ STATUS REG	LD COMMAND REG
	DFF4	READ DATA	WRITE DATA
TIMER	DFEE	-	SET MODE
	DFEC	COUNTER 2	COUNTER 2
	DFEA	COUNTER 1	COUNTER 1
	DFE8	COUNTER 0	COUNTER 0
MNTCE PORT	DFE6	READ DATA	WRITE DATA
	DFE4	READ STATUS	WRITE CONTROL
SWITCHER PORT	DFDE	READ DATA	WRITE DATA
	DFDC	READ STATUS	WRITE CONTROL
CHB	DFD6	READ FIFO	WRITE TO VRT
CHA	DFCE	READ FIFO	WRITE TO VRT
SPARE	DFCX	-	
SPARE	DFB8	-	
SPARE	DFB0	-	
SPARE	DFA8	-	
SPARE	DFA0	-	
16X16 MULTIPLIER	DF98	READ LSP	
	DF90	READ MSP	
	DF88	-	WRITE Y INTO MULTIPLIER
	DF80	-	WRITE X INTO MULTIPLIER

Schematic No. 1464490C.
Computer PWA, A27
(Sheet 8 of 8)

ITEM NO.	PART NUMBER		DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1464525-01	PWA, KEYER		XA9	1
2	1464528-02	PWA, CLOCK		XA11	1

LM-1464409

ITEM NO.	PART NUMBER		DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1465110-01	PWA, KEYER			1
2	1465111-01	PWA, CLOCK			1

LM-1464410

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1464411-02	PWA, I/O PLL		2
2	1464522-01	PWA, CUTTER		1
3	1464525-01	PWA, KEYER		1
4	1464455-01	CABLE, ADO-CONCENTRATOR		4

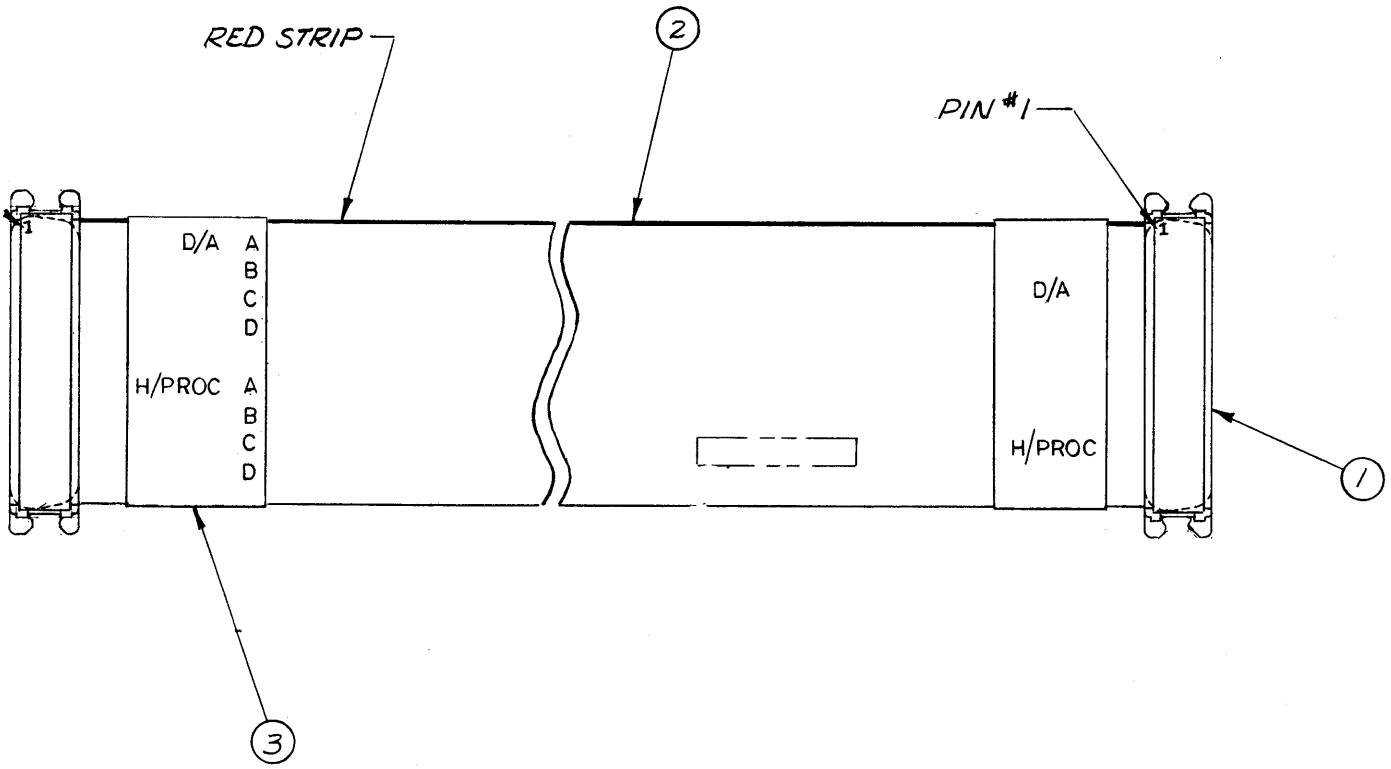
LM-1464568

ITEM NO.	PART NUMBER		DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1464411-02	PWA, I/O PLL			2
2	1464522-01	PWA, CUTTER			1
3	1465110-01	PWA, KEYER			1
4	1464455-01	CABLE, ADO-CONCENTRATOR			4

LM-1464569

ITEM NO.	PART NUMBER		DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1464455-01		CABLE, ADO-CONCENTRATOR		4
2	1809633-01		SERVICE MANUAL		1

LM-1465118



AR	3		SLEEVING, SHRINKABLE		
AR	2	616-692	CABLE, RIBBON, 50 CONDUCTOR		
2	1	140-690	CONNECTOR, FLAT CABLE, 50 CONT		
-01	ITEM NO.	PART NUMBER		DESCRIPTION	

PARTS LIST

Assembly No. 1464455-01A. ADO Concentrator Cable

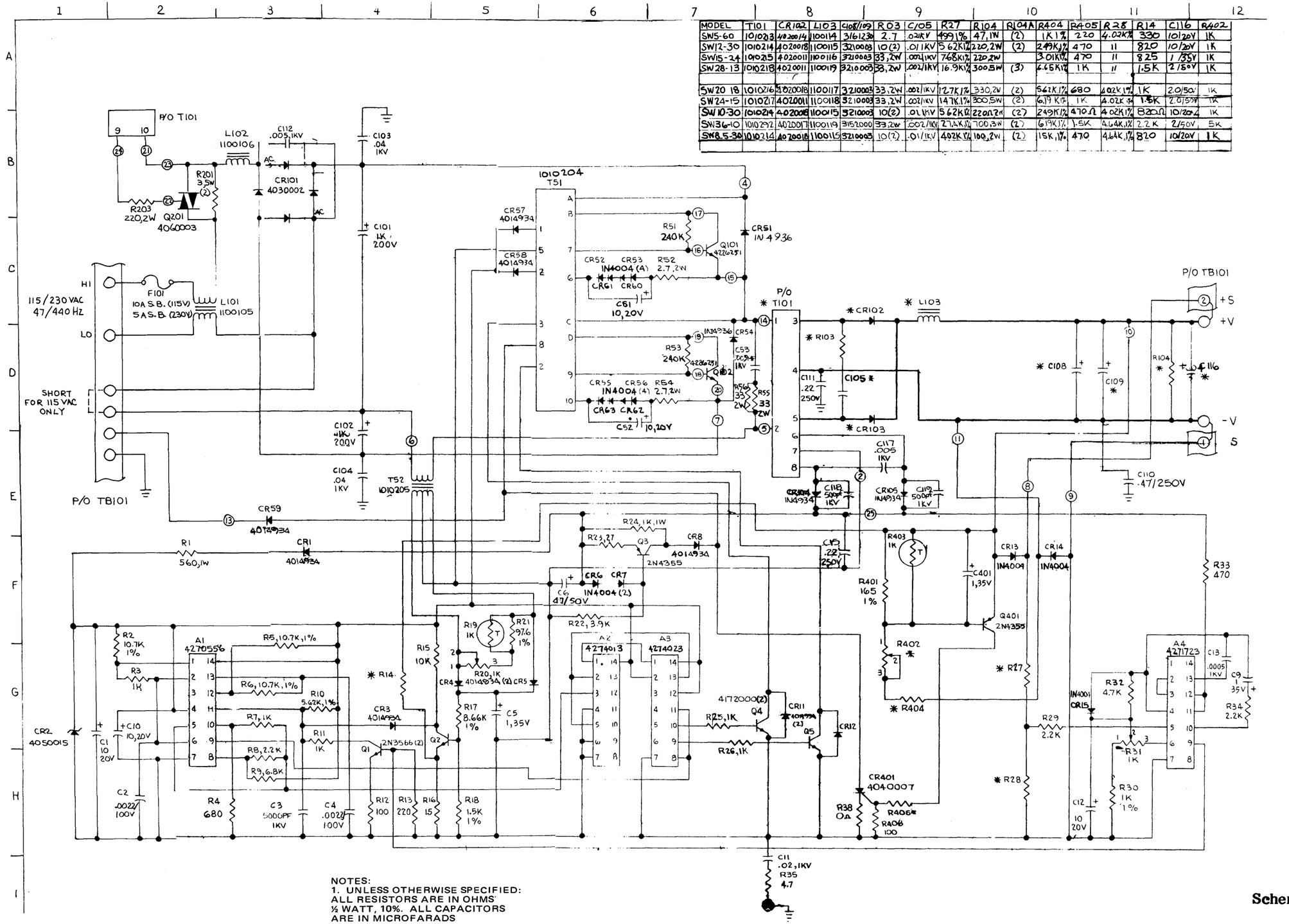
ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1	1465097-01	PROM ASSEMBLY, COMPUTER 27128 002-117 ▷1	4M	1
2	1465098-01		4P	1
3	1465099-01		4S	1
4	1465100-01		5M	1
5	1465101-01		5P	1
6	1465102-01	PROM ASSEMBLY, COMPUTER 27128 002-117 ▷1	5S	1
7	1465103	COMPUTER PROM INSTALLATION INSTRUCTIONS		1

NOTES:

▷1 STATIC SENSITIVE DEVICE, SPECIAL HANDLING REQUIRED PER AMPEX STD HE1-1.

LM-1465019

MODEL	T101	CR102	L103	C108/109	R03	C105	R27	R104	R104A	R404	R405	R28	R14	C116	R402
SW5-60	1010203	4020014	1100114	3/161230	2.7	.02KV	499 1%	47, 1W	(2)	1K 1%	220	4.02K 1%	330	10/20V	1K
SW12-30	1010214	4020018	1100115	3210003	10 (2)	.01 1KV	5.62K 1%	220, 2W	(2)	249K 1%	470	11	820	10/20V	1K
SW15-24	1010215	4020011	1100116	3210003	33, 2W	.001 1KV	768K 1%	220, 2W		301K 1%	470	11	825	1/35V	1K
SW28-13	1010218	4020011	1100119	3210003	33, 2W	.002/1KV	16.9K 1%	300.5W	(3)	665K 1%	1K	11	1.5K	2/50V	1K
SW20-18	1010216	4020018	1100117	3210003	33, 2W	.002/1KV	12.7K 1%	330, 2W	(2)	562K 1%	680	402K 1%	1K	2.0/50	1K
SW24-15	1010217	4020011	1100118	3210003	33, 2W	.002/1KV	14.7K 1%	300.5W	(2)	6.19 K 1%	1K	4.02K 1%	1.5K	2.0/50V	1K
SW10-30	1010219	4020018	1100115	3210003	10 (2)	.01 1KV	5.62K 1%	220 Ω 2W	(2)	249K 1%	470 Ω	4.02K 1%	820 Ω	10/20V	1K
SW36-10	1010252	4020017	1100119	3152000	33, 2W	.002/1KV	27.4K 1%	700, 3W	(2)	619K 1%	1.5K	4.64K 1%	2.2 K	2/50V	5K
SW8.5-30	1010214	4020018	1100115	3210003	10 (2)	.01/1KV	402K 1%	100, 2W	(2)	15K 1%	470	4.64K 1%	820	10/20V	1K



NOTES:
1. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE IN OHMS' ½ WATT, 10%. ALL CAPACITORS ARE IN MICROFARADS

2. COMPONENT DESIGNATIONS 1 THRU 99, 200 THRU 299 AND 400 THRU 499 ARE ON P.C. BOARDS.

3. *SEE TABLE

Schematic No. 9010221CC.
Todd Products Corp.
Case 102 SW Series

Table A1. Integrated Circuit Ampex Part Numbers

AMPEX PART NO.	MANUFACTURER'S PART NO.	MANUFACTURER	PAGE NO.
000-040	MC6810	Motorola	A-1
000-128 See 586-554			A-3
000-151 See 587-550			A-15
000-152 See 587-132			A-7
000-153 See 587-549			A-14
001-042 See 590-194			A-25
001-054 See 586-183			A-2
001-076 See 587-664			A-17
001-077 See 587-551			A-16
001-953	DS1488	Motorola	A-1
001-977 See 590-960			A-27
002-050 See 587-205			A-9
002-088 See 589-508			A-22
002-917 See 589-617			A-23
002-929 See 586-923			A-5
002-933 See 000-040			A-1
003-026 See 587-279			A-10
586-075	MC7400	Texas Instruments	A-1
586-076	SN7410N	Texas Instruments	A-2
586-108	SN7474	Texas Instruments	A-2
586-183	SN74H21N	Texas Instruments	A-2
586-554	SN7483N	Texas Instruments	A-3
586-688	SN74H04N	Texas Instruments	A-3
586-703	SN74151N	Texas Instruments	A-4
586-759	SN7408N	Texas Instruments	A-4
586-830	SN74S00N	Texas Instruments	A-4
586-918	SN7432	Texas Instruments	A-5
586-923	SN74163	Texas Instruments	A-5
586-978	SN74S112N	Texas Instruments	A-5
587-098	SN74S157N	Texas Instruments	A-6
587-131	MC10124L	Motorola	A-6
587-132	MC10125	Motorola	A-7
587-133	MC10116	Motorola	A-7
587-139	MC10131L	Motorola	A-8
587-150	SN74S86N	Texas Instruments	A-8
587-158	74S174PC	Fairchild	A-9
587-205	MC10102	Motorola	A-9
587-278	SN74S85N	Texas Instruments	A-10
587-279	SN74LS138N	Texas Instruments	A-10
587-285	MC10125	Motorola	A-11

Table A1. Integrated Circuit Ampex Part Numbers (Continued)

AMPEX PART NO.	MANUFACTURER'S PART NO.	MANUFACTURER	PAGE NO.
587-291	NE555V	Signetics	A-12
587-324	MC10106	Motorola	A-13
587-431	SN74221	Texas Instruments	A-13
587-532 See 586-703			A-4
587-536	74LS193	Texas Instruments	A-14
587-549	MC10104	Motorola	A-14
587-550	MC10136	Motorola	A-15
587-551	MC10176	Motorola	A-16
587-630	MC10115P	Motorola	A-16
587-664	MC10174	Motorola	A-17
587-750	74LS02	Fairchild	A-17
587-772	SN74LS161	Texas Instruments	A-17
587-777	SN74LS153N	Texas Instruments	A-18
587-778	SN74LS30N	Texas Instruments	A-18
587-814	SN74LS283N	Texas Instruments	A-18
587-895	74LS164	Fairchild	A-19
587-952	SN74LS27N	Texas Instruments	A-19
589-331	SN74LS273N	Texas Instruments	A-19
589-334	SN74LS393N	Texas Instruments	A-20
589-369	SN74LS156N	Texas Instruments	A-20
589-384	TL082	Texas Instruments	A-20
589-449	SN74LS244	Texas Instruments	A-21
589-457	SN74245	Texas Instruments	A-21
589-508	MC10135	Motorola	A-22
589-536	SN74S374J	Texas Instruments	A-22
589-537	SN74374	Texas Instruments	A-22
589-617	8253	Intel	A-23
589-713 See 587-551			A-16
589-751	SN74LS241	Texas Instruments	A-24
589-752	SN74LS373	Texas Instruments	A-24
589-813 See 586-075			A-1
589-814 See 586-688			A-3
589-815 See 586-759			A-4
589-816 See 586-076			A-2
589-820 See 586-108			A-2
589-823 See 587-279			A-10
589-824 See 587-777			A-18
589-825 See 587-098			A-6
589-827 See 587-895			A-19
589-830 See 586-108			A-2

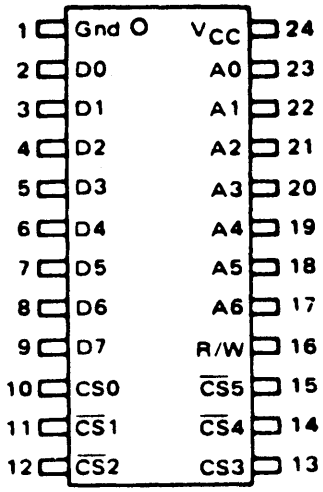
Table A1. Integrated Circuit Ampex Part Numbers
(Continued)

AMPEX PART NO.	MANUFACTURER'S PART NO.	MANUFACTURER	PAGE NO.
589-837 See 586-830			A-4
589-838 See 586-688			A-3
589-846 See 586-108			A-2
589-847 See 587-150			A-8
589-850 See 586-923			A-5
589-920 See 587-952			A-19
589-930 See 587-778			A-18
589-931 See 587-772			A-17
589-933 See 587-431			A-13
589-934 See 589-334			A-20
589-935 See 587-158			A-9
589-937 See 587-158			A-9
590-193	9637	Fairchild	A-25
590-194	DS3692	Fairchild	A-25
590-227	AM25S09	AMD	A-26
590-326 See 587-139			A-8
590-328 See 586-918			A-5
590-330 See 587-630			A-16
590-333 See 586-923			A-5
590-335 See 589-331			A-19
590-443 See 587-750			A-17
590-461 See 586-978			A-5
590-464 See 587-285			A-11
590-496 See 586-703			A-4
590-543 See 587-133			A-7
590-564 See 587-131			A-6
590-565 See 589-752			A-24
590-584 See 589-449			A-21
590-586 See 589-536			A-22
590-602 See 589-384			A-20
590-606 See 587-814			A-18
590-725 See 587-291			A-12
590-842 See 587-098			A-6
590-843 See 587-278			A-10
590-847 See 589-457			A-21
590-855 See 589-536			A-22
590-866	AM8002	AMD	A-26
590-868 See 589-449			A-21
590-917 See 589-331			A-19
590-932	CDP1854	RCA	A-27

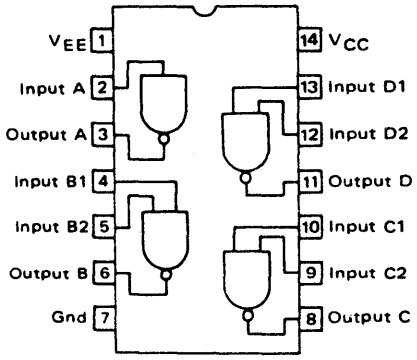
Table A1. Integrated Circuit Ampex Part Numbers
(Continued)

AMPEX PART NO.	MANUFACTURER'S PART NO.	MANUFACTURER	PAGE NO.
590-935 See 586-075			A-1
590-940 See 586-108			A-2
590-947 See 589-537			A-22
590-960	MC68B50	Motorola	A-27
590-987	MPY8HJ	TRW	A-28
590-989	TMS4164	Texas Instruments	A-28

MOTOROLA MC6810	AMPEX 000-040	128 X 8 BIT STATIC RAM



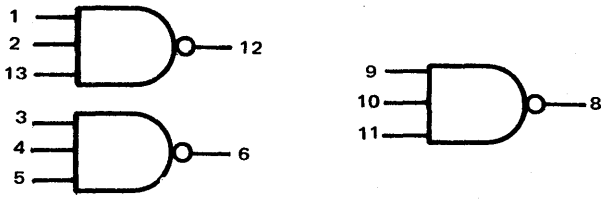
MOTOROLA MC1488	AMPEX 001-953	QUAD LINE DRIVER



MOTOROLA MC 7400	AMPEX 586-075	QUAD 2-INPUT NAND GATE

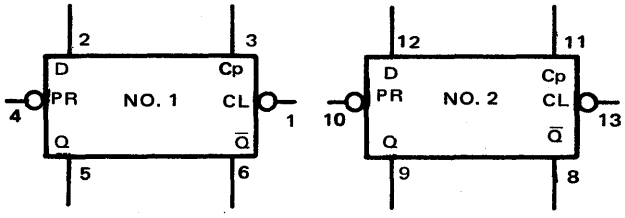
PIN 7 = GND
PIN 14 = V_{cc} (+5V)
3 = $\overline{1.2}$

TEXAS INSTRUMENTS SN 7410 N	AMPEX 586-076	3-INPUT NAND GATE



PIN 7 = GND
PIN 14 = V_{cc}
12 = $\overline{1.2.13}$

TEXAS INSTRUMENTS SN 7474	AMPEX 586-108	DUAL D-TYPE EDGE- TRIGGERED FLIP-FLOP



PIN 7 = GND
PIN 14 = V_{cc}

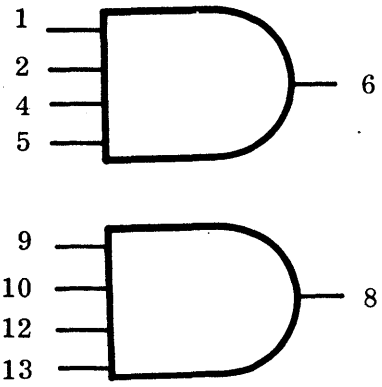
PR = PRESET
CL = CLEAR
Cp = CLOCK

t_n D	$t_n + 1$ Q
L	L
H	H

PR	CL	Q
L	H	H
H	L	L
L	L	ND

$t_n + 1$ IS TIME AFTER POSITIVE TRANSITION OF CLOCK

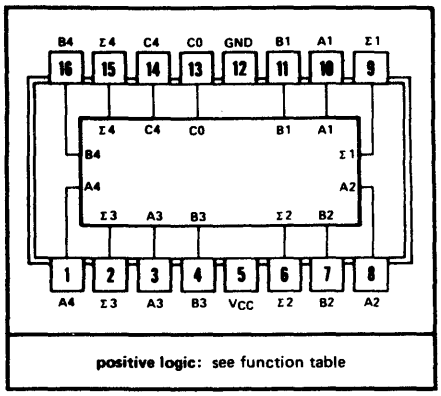
TEXAS INSTR SN 74H21N	AMPEX 586-183	DUAL 4-INPUT AND GATE TOTEM POLE OUTPUTS



VCC 14
GND 7

$Y = A \cdot B \cdot C \cdot D$

TEXAS INST	AMPEX	4-BIT BINARY FULL ADDERS WITH
SN7483N	586-554	FAST CARRY



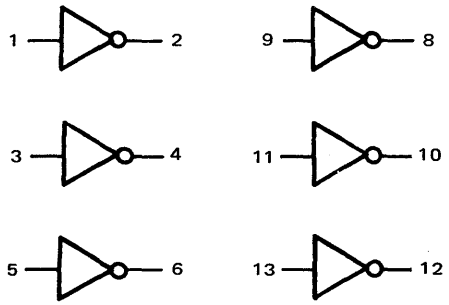
positive logic: see function table

FUNCTION TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A4	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

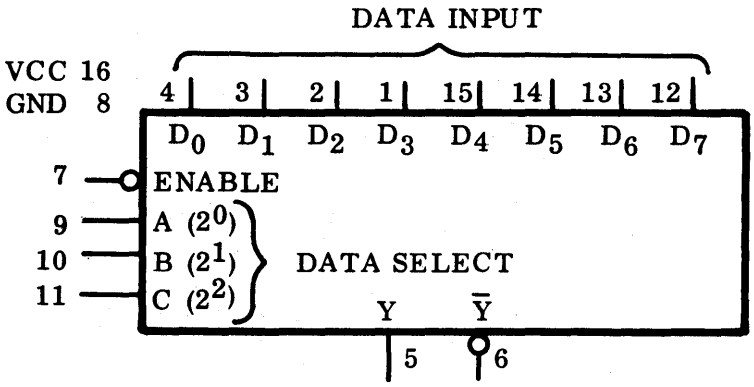
H = high level, L = low level

TEXAS INSTRUMENTS	AMPEX	HEX
SN 74H04N	586-688	INVERTER



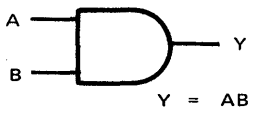
PIN 7 = GND
PIN 14 = +5V (V_{cc})

TEXAS INSTR	AMPEX	
SN 74151N	586-703	DATA SELECTOR (MULTIPLEXER)



1. ENABLE (PIN 7) HIGH, Y LOW, Y HIGH.
2. ENABLE LOW, OUTPUT Y FOLLOWS DATA SELECTED (INPUT) BY BINARY NUMBER AT DATA SELECT. PIN 6 (Y) WILL BE COMPLEMENT OF SELECTED DATA INPUT.

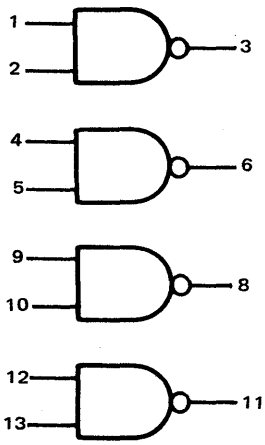
TEXAS INSTRUMENTS	AMPEX	
SN 7408 N	586-759	QUAD 2-INPUT AND GATE



A	1	4	9	12
B	2	5	10	13
Y	3	6	8	11

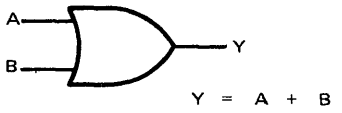
PIN 7 = GND
PIN 14 = V_{cc}

TEXAS INSTRUMENTS	AMPEX	
SN 74S00N	586-830	QUAD 2-INPUT NAND GATE



PIN 7 = GND
PIN 14 = +5V (V_{cc})

TEXAS INSTRUMENTS SN 7432	AMPEX 586-918	OR GATE



Y = A + B

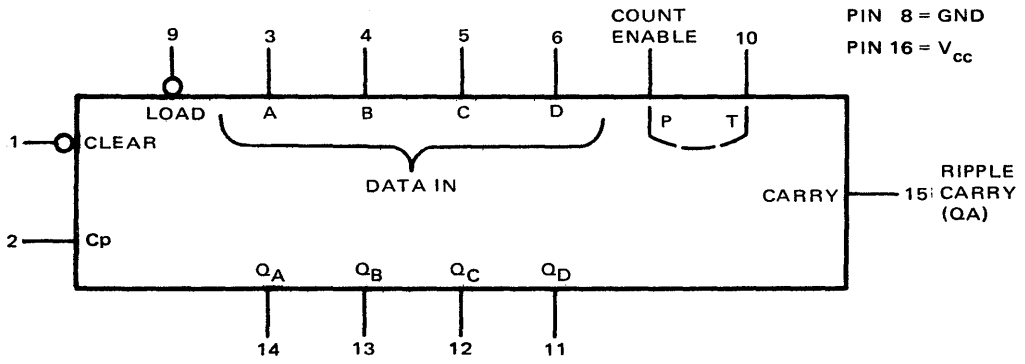
A	B	Y
1	2	3
4	5	6
9	10	8
12	13	11

PIN 7 = GND

PIN 14 = V_{cc}

TOTEM OUTPUT

TEXAS INSTRUMENTS SN 74163	AMPEX 586-923	SYNCHRONOUS BINARY COUNTER

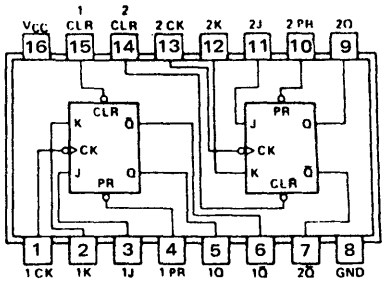


CLEAR AND LOAD SYNCHRONOUS WITH POSITIVE TRANSITION OF CLOCK PULSE.

TEXAS INSTRUMENTS SN74S112N	AMPEX 586-978	DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

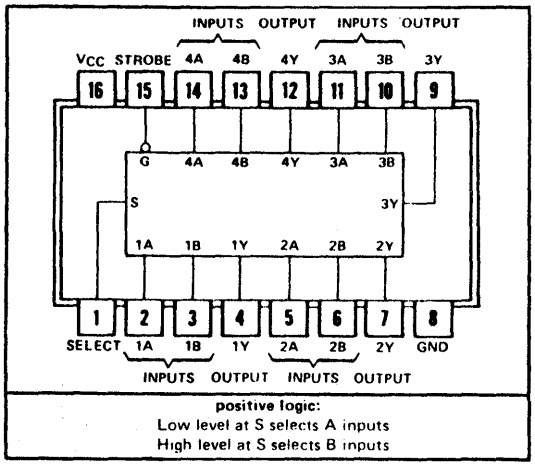
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54LS112/SN74LS112(J, N, W)
SN54S112/SN74S112(J, N, W)

TEXAS INST SN74S157N	AMPEX 587-098	QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS



positive logic:
Low level at S selects A inputs
High level at S selects B inputs

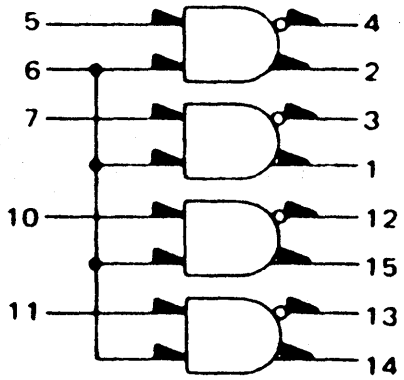
FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157, 'L157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

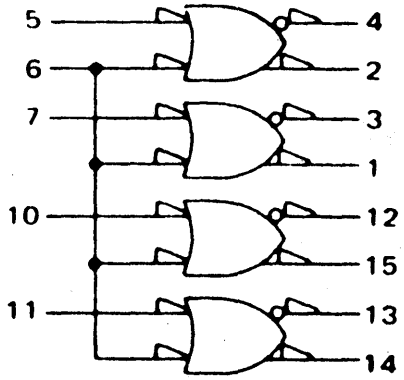
H = high level, L = low level, X = irrelevant

MOTOROLA MC10124L	AMPEX 587-131	QUAD MTTL TO MECL TRANSLATOR

POSITIVE LOGIC

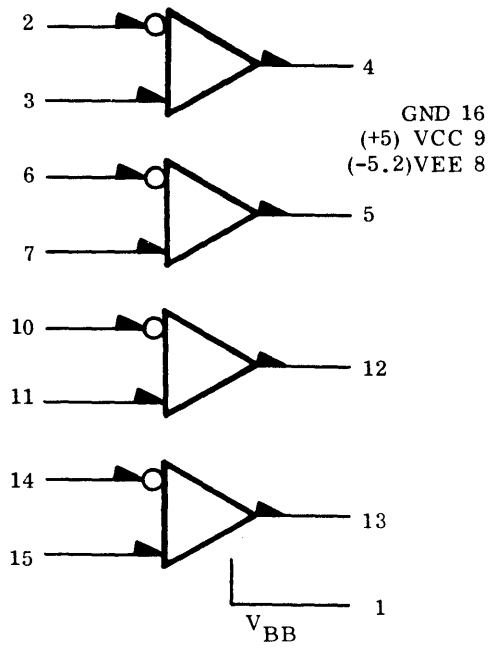


NEGATIVE LOGIC

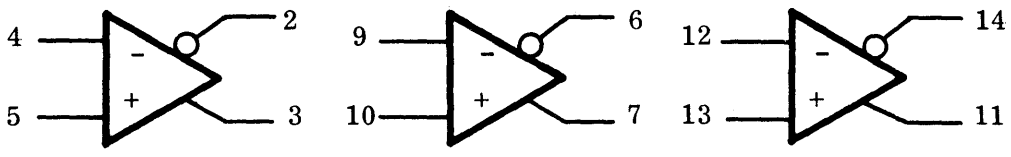


Gnd Pin 16
V_{CC} (+5.0 Vdc) Pin 9
V_{EE} (-5.2 Vdc) Pin 8

MOTOROLA	AMPEX	
MC10125	587-132	MECL TO MTTL TRANSLATOR
	POSITIVE LOGIC	



MOTOROLA	AMPEX	
MC 10116	587-133	TRIPLE LINE RECEIVER ECL

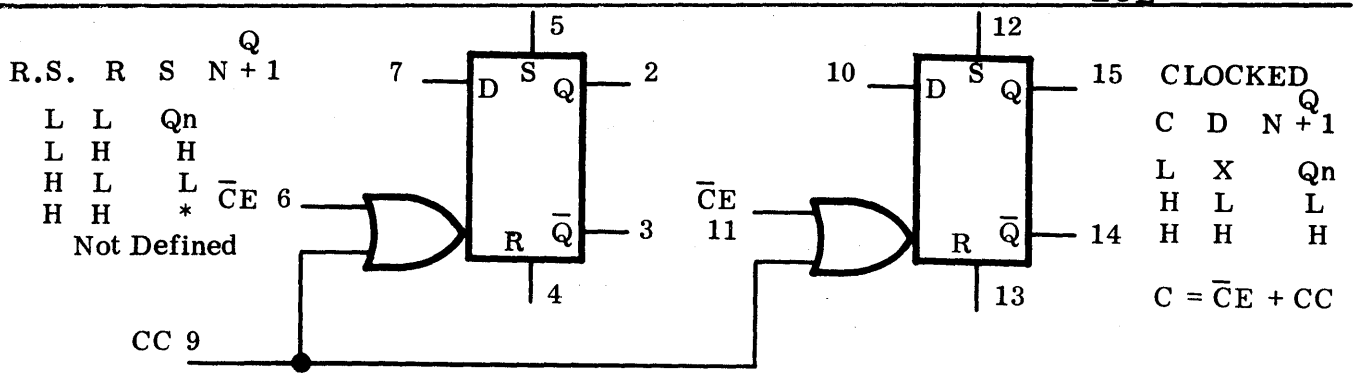


VBB 11 VEE 8
VCC_1 1 VCC_2 16

MOTOROLA
MC 10131 L

AMPEX
587-139

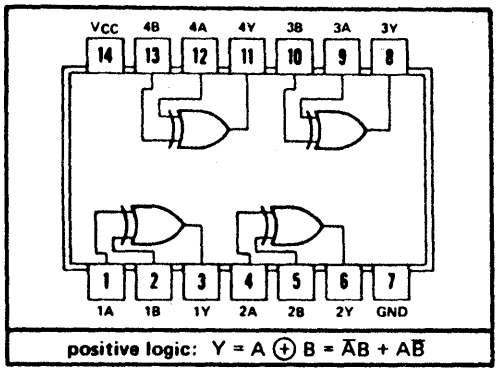
DUAL D FLIP FLOP
ECL



TEXAS INST
SN74S86N

AMPEX
587-150

QUADRUPLE 2-INPUT EXCLUSIVE-OR
GATES

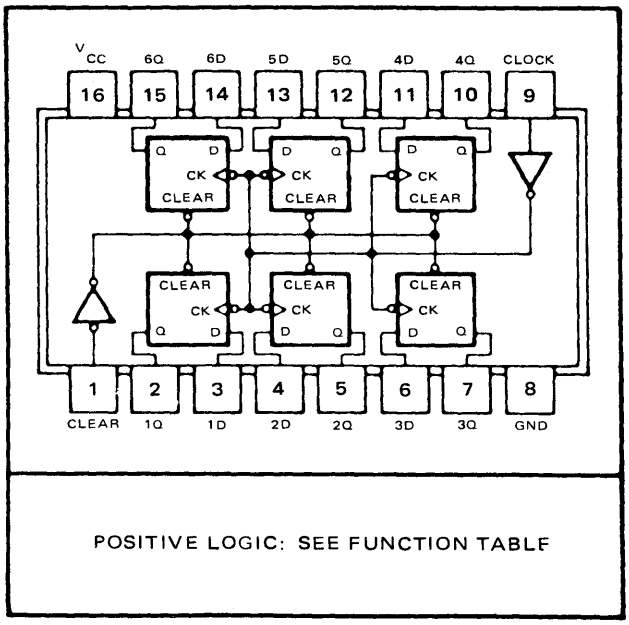


FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

FAIRCHILD 74S174PC	AMPEX 587-158	HEX/QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR



POSITIVE LOGIC: SEE FUNCTION TABLE

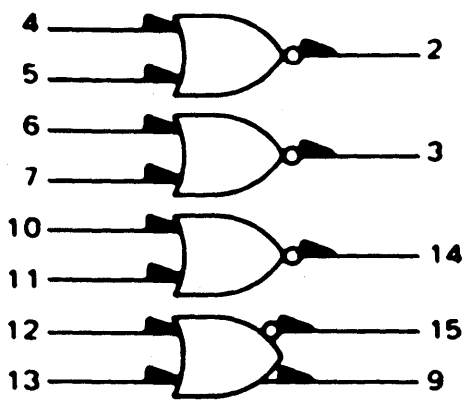
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$ †
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

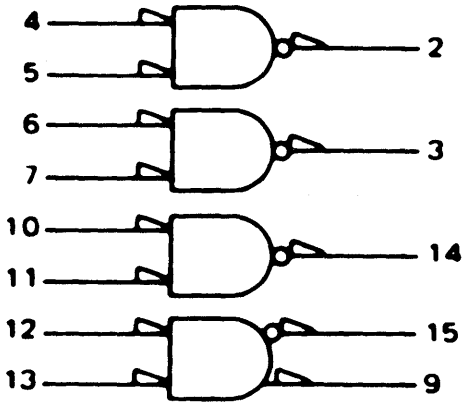
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established
† = '175, 'LS175, and 'S175 only

MOTOROLA MC10102	AMPEX 587-205	QUAD 2-INPUT NOR GATE

POSITIVE LOGIC

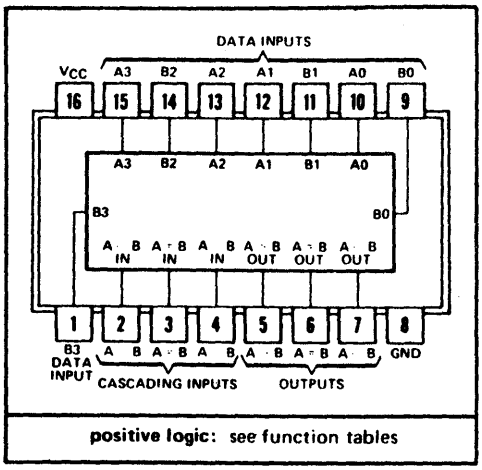


NEGATIVE LOGIC



V_{CC1} - Pin 1
V_{CC2} - Pin 16
V_{EE} - Pin 8

TEXAS INST	AMPEX	4-BIT MAGNITUDE COMPARATOR
SN74S85N	587-278	



positive logic: see function tables

FUNCTION TABLES

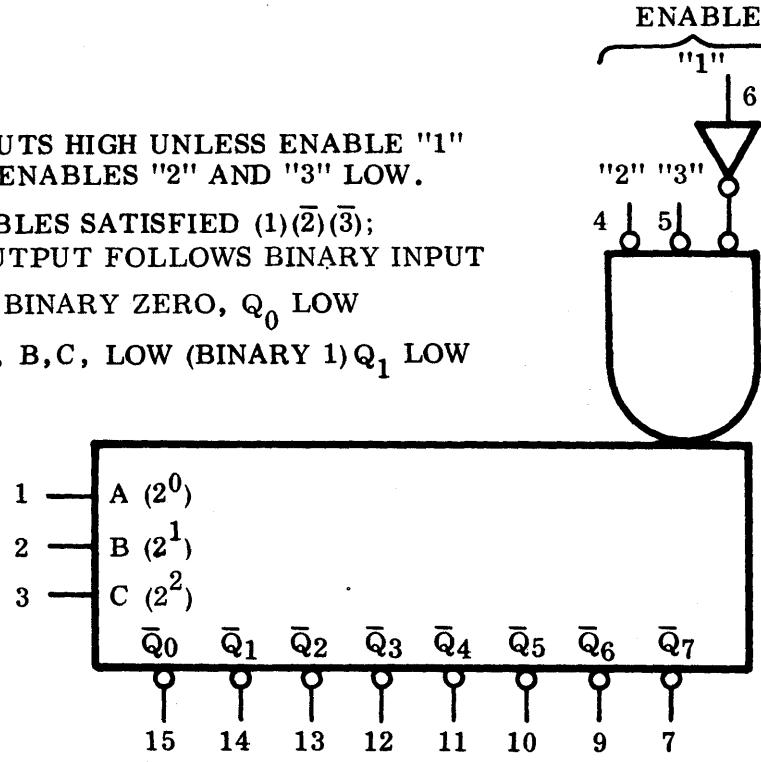
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

'85, 'S85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

TEXAS INSTR	AMPEX	3 TO 8 LINE DECODER/MULTIPLEXER
SN 74LS138N	587-279	

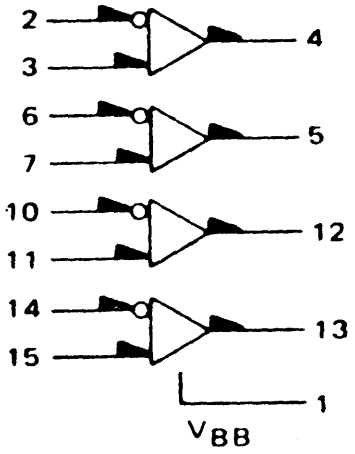
1. ALL OUTPUTS HIGH UNLESS ENABLE "1" HIGH AND ENABLES "2" AND "3" LOW.
2. WITH ENABLES SATISFIED (1)($\overline{2}$)($\overline{3}$);
   - LOW OUTPUT FOLLOWS BINARY INPUT
   - A,B,C: BINARY ZERO, Q_0 LOW
   - A HIGH, B,C, LOW (BINARY 1) Q_1 LOW



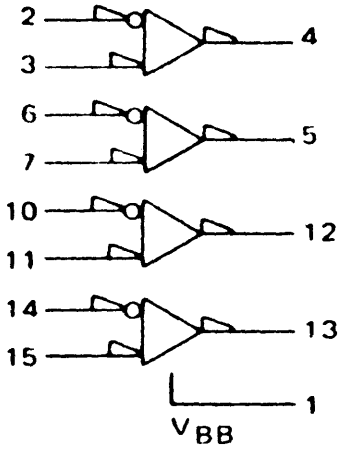
VCC 16
GND 8

MOTOROLA MC10125L	AMPEX 587-285	QUAD MECL TO MTTL TRANSLATOR

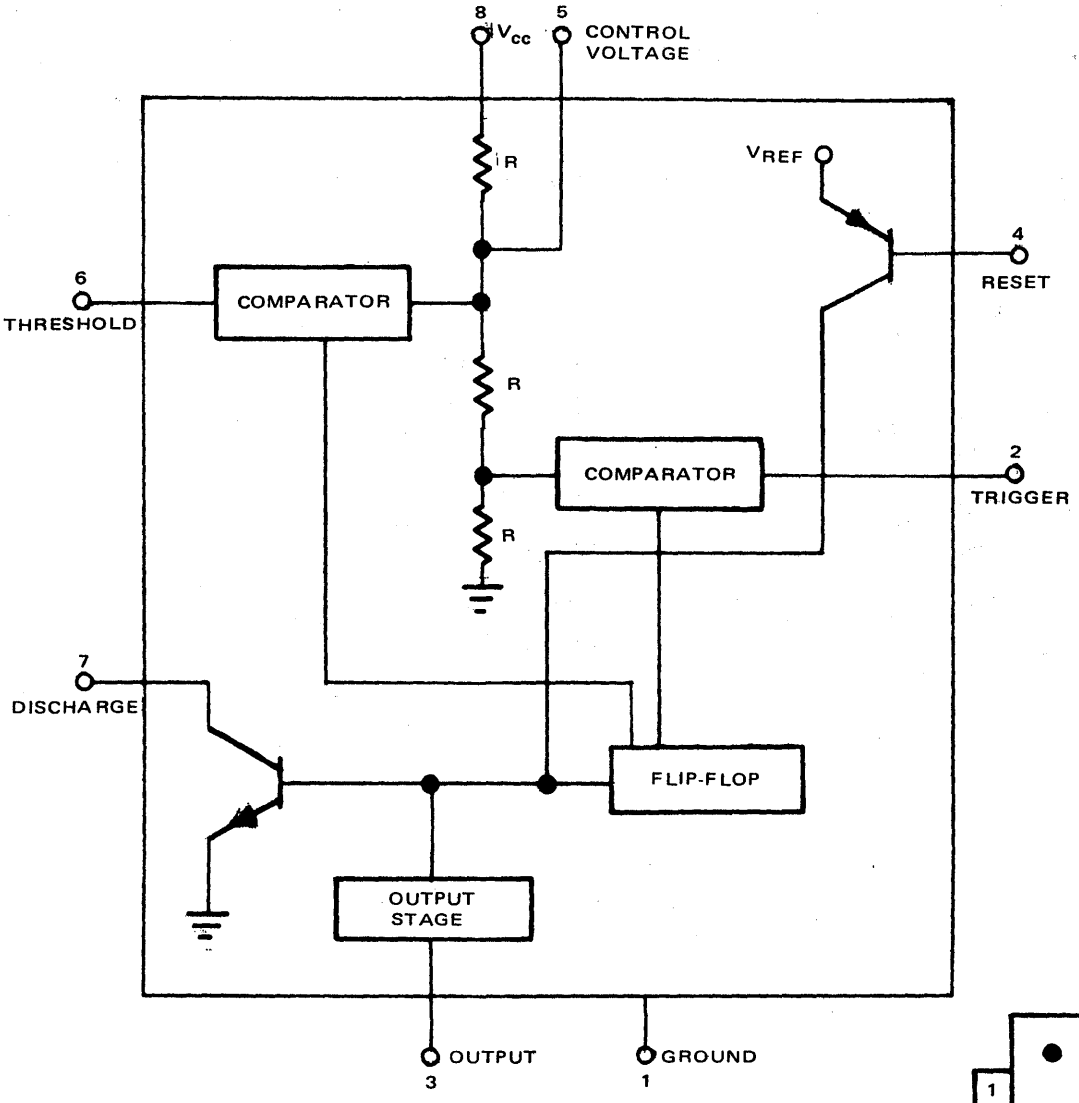
POSITIVE LOGIC



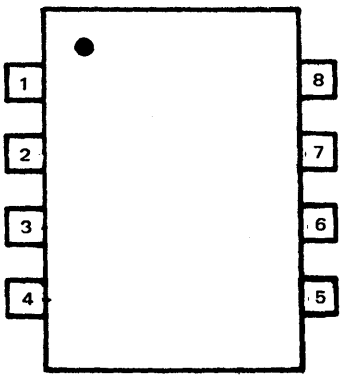
NEGATIVE LOGIC



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (-5.2 Vdc) = Pin 8

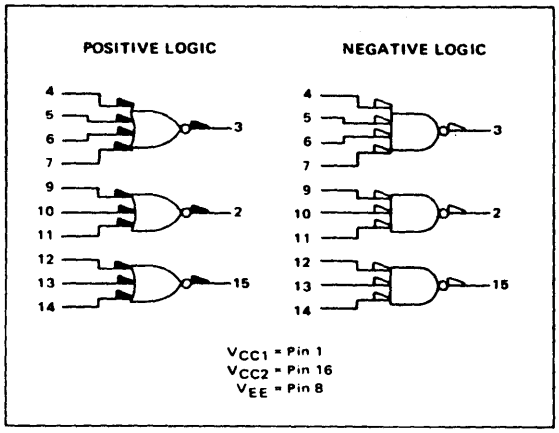


V PACKAGE
(TOP VIEW)



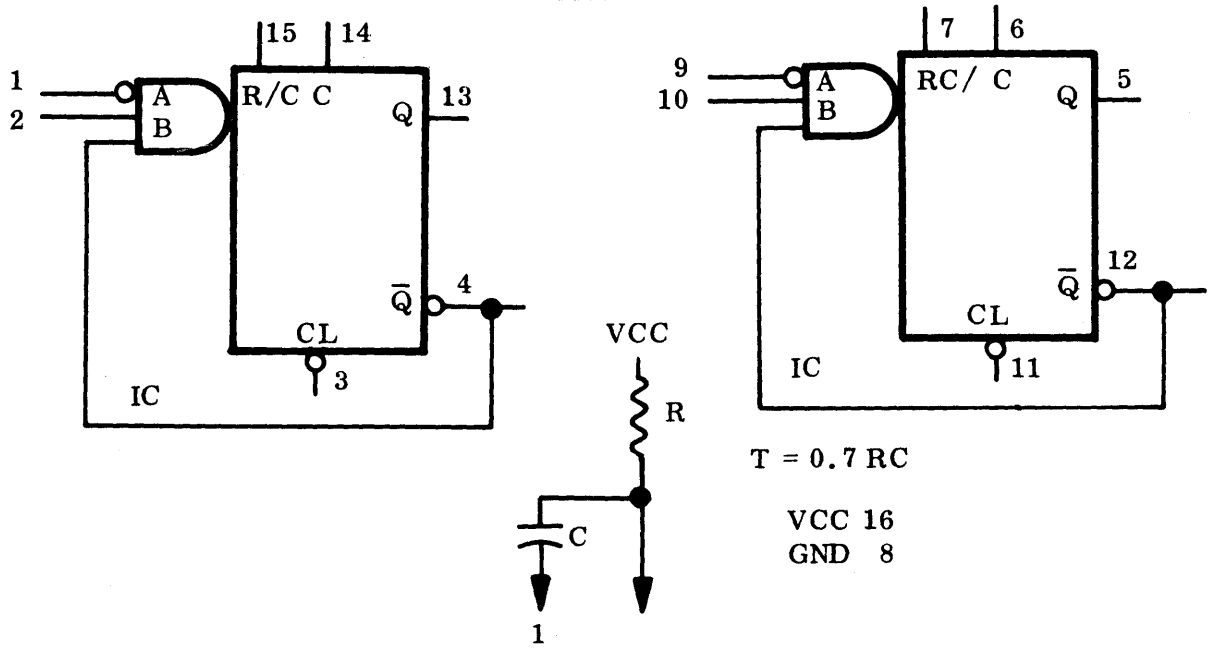
1. GROUND
2. TRIGGER
3. OUTPUT
4. RESET
5. CONTROL VOLTAGE
6. THRESHOLD
7. DISCHARGE
8. V_{cc}

MOTOROLA MC10106	AMPEX 587-324	TRIPLE 4-3-3 INPUT NOR GATE

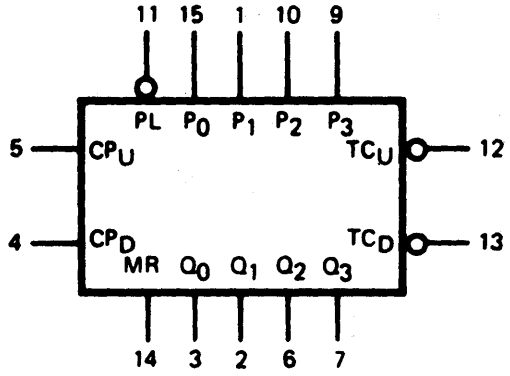


P_D = 30 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
Output Rise and Fall Time
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

TEXAS INST SN74221	AMPEX 587-431	NON-RETRIGGERABLE ONE SHOT SCHMITT TRIGGER INPUTS



FAIRCHILD/T.I.	AMPEX	PRESETTABLE 4-BIT/BINARY
74LS193	587-536	UP/DOWN COUNTER

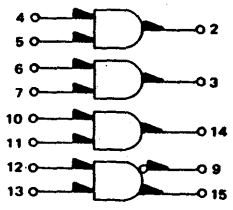


V_{CC} = Pin 16
GND= Pin 8

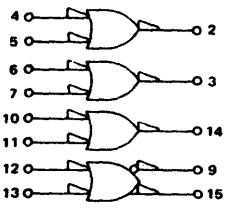
MOTOROLA	AMPEX	QUAD 2-INPUT AND GATE
MC10104	587-549	

P_D = 35 mW typ/gate (No load)
t_{pd} = 2.7 ns typ
Output Rise and Fall Times:
= 3.5 ns typ (10% - 90%)
= 2.0 ns typ (20% - 80%)

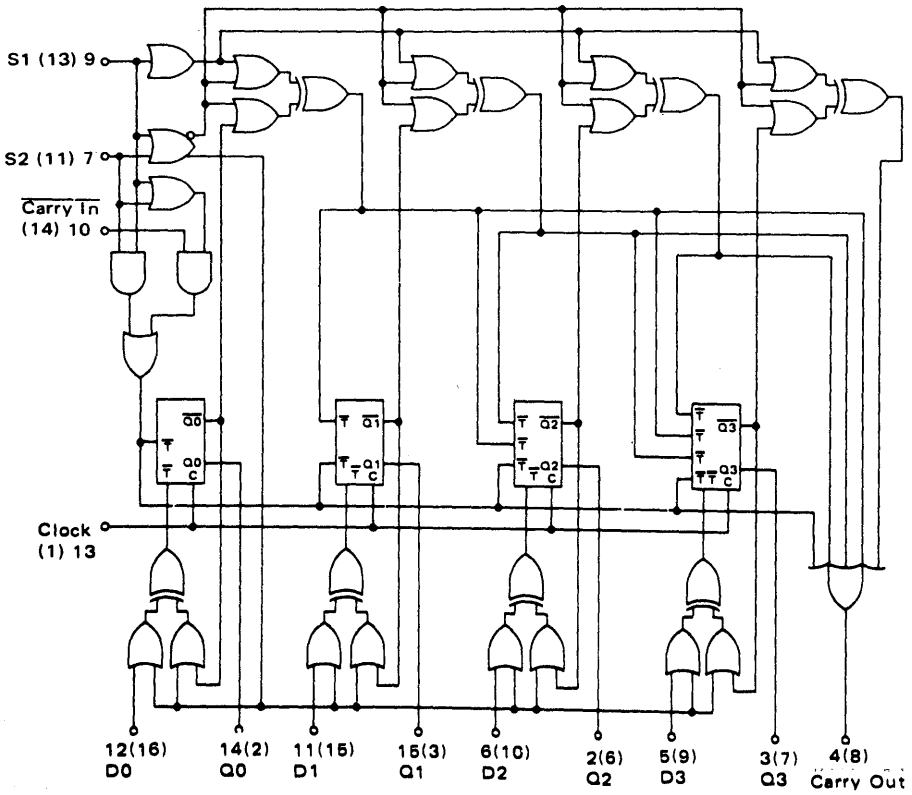
POSITIVE LOGIC



NEGATIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8



SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
H	H	ϕ	ϕ	ϕ	ϕ	H	ϕ	H	H	H	H	H
H	L	H	H	L	L	ϕ	H	H	H	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	H	H

ϕ = Don't care.

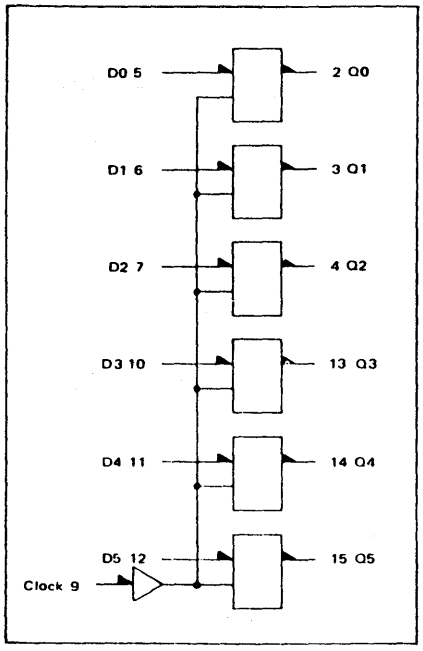
* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ
t_{pd} = 3.3 ns typ (C - Q)
= 7.0 ns typ (C - $\overline{C}_{out}$)
= 5.0 ns typ ($\overline{C}_{in}$ - $\overline{C}_{out}$)

MOTOROLA MC10176	AMPEX 587-551	HEX "D" MASTER SLAVE FLIP-FLOP



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

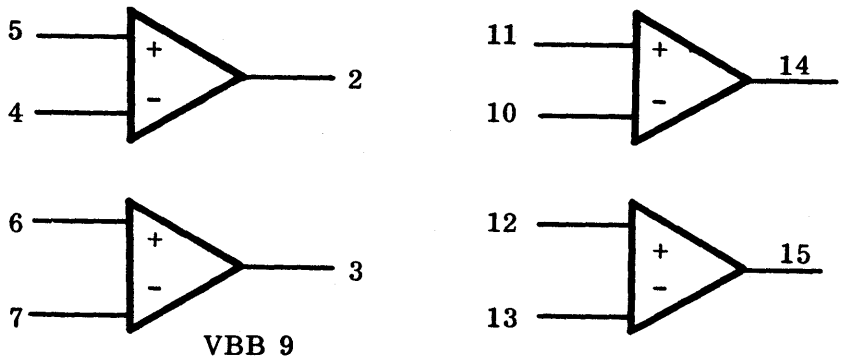
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ Don't Care

*A clock H is a clock transition from a low to a high state.

MOTOROLA MC 10115 P	AMPEX 5 87-630	QUAD LINE RECEIVER



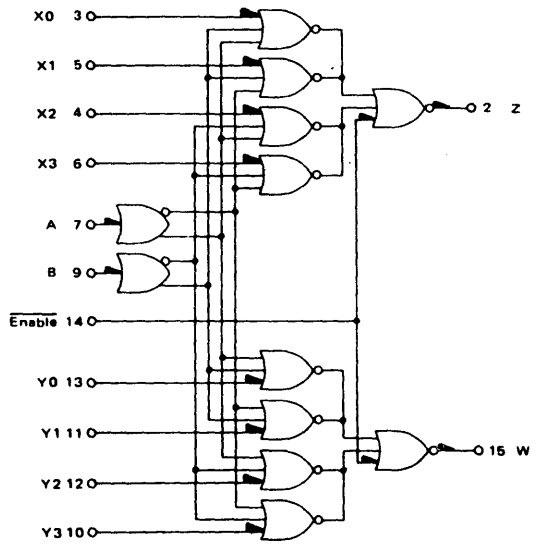
VBB 9
VCC 2 16
VEE 8

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

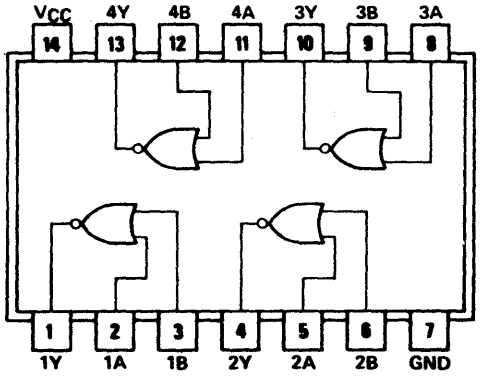
ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Z	$\overline{W}$
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

ϕ = Don't Care

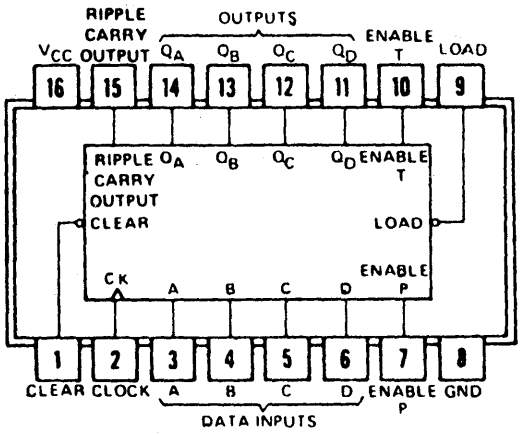


FAIRCHILD	AMPEX	QUADRUPLE 2-INPUT POSITIVE-NOR
74LS02	587-750	GATE

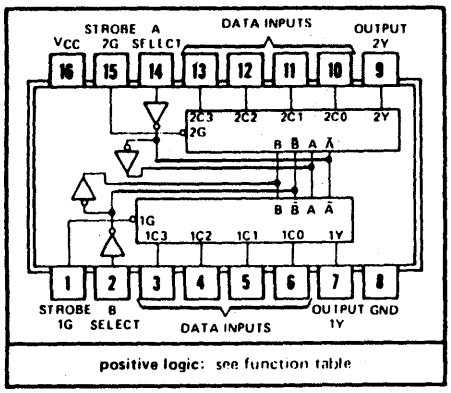
$Y = \overline{A+B}$



TEXAS INSTR	AMPEX	SYNCHRONOUS 4-BIT COUNTERS
SN74LS161	587-772	



TEXAS INST	AMPEX	DUAL 4-LINE-TO-1-LINE DATA
SN74LS153N	587-777	SELECTORS/MULTIPLEXERS



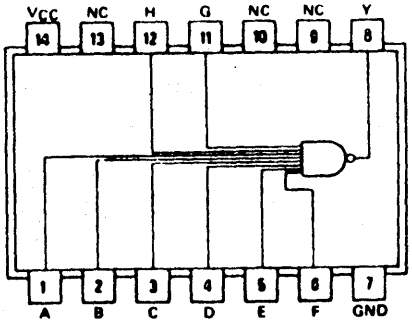
positive logic: see function table

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

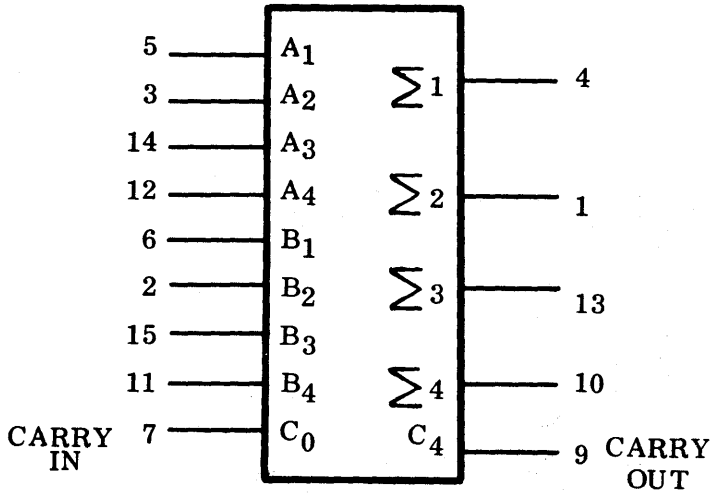
Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

TEXAS INST	AMPEX	8-INPUT POSITIVE-NAND GATES
SN74LS30N	587-778	



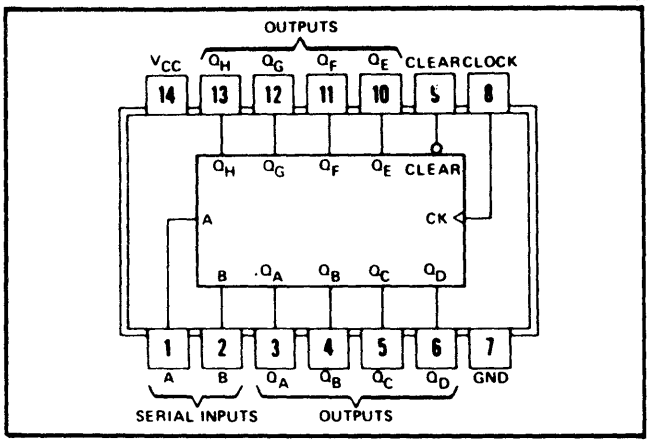
positive logic:
$Y = \overline{ABCDEFGH}$

TEXAS INST	AMPEX	4 BIT BINARY ADDER WITH
SN 74LS283N	587-814	FAST CARRY



PIN 8 = GND
PIN 16 = +5V

FAIRCHILD	AMPEX	8-BIT PARALLEL-OUT SERIAL
74LS164	587-895	SHIFT REGISTER

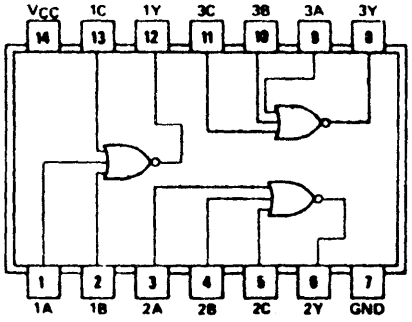


FUNCTION TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

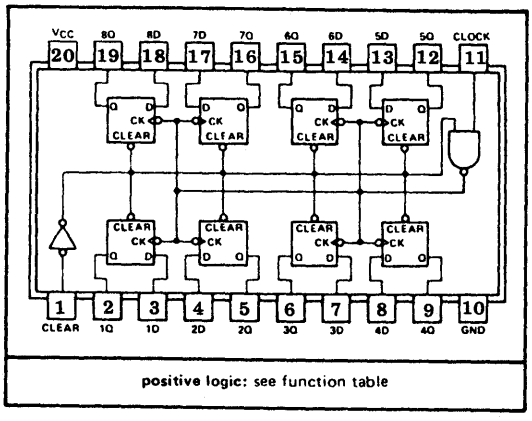
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

TEXAS INST	AMPEX	TRIPLE 3-INPUT POSITIVE-NOR GATES
SN74LS27N	587-952	



positive logic:
$Y = \overline{A+B+C}$

TEXAS INST	AMPEX	OCTAL D-TYPE FLIP-FLOP WITH CLEAR
SN74LS273N	589-331	

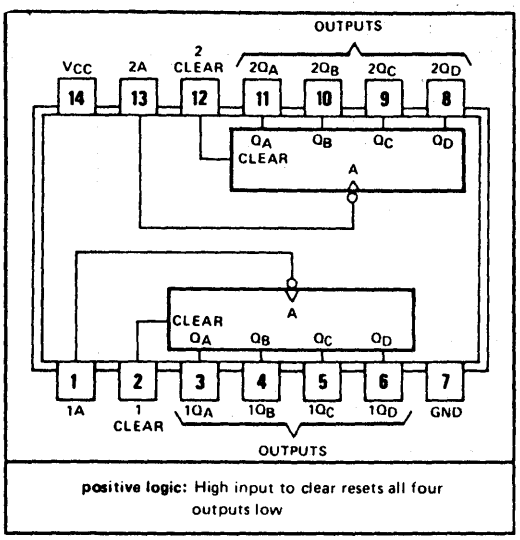


FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.

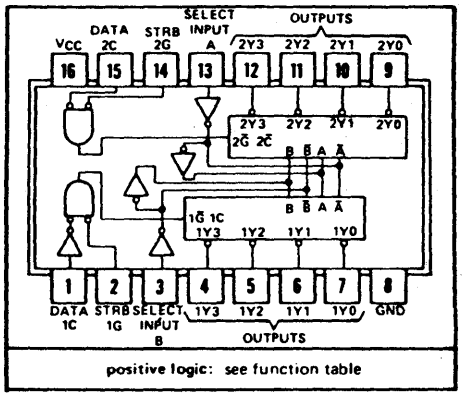
TEXAS INST	AMPEX	DUAL 4-BIT DECADE AND BINARY
SN74LS393N	589-334	COUNTERS



positive logic: High input to clear resets all four outputs low

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

TEXAS INST	AMPEX	DUAL 2-LINE-TO-4-LINE
SN74LS156N	589-369	DECODERS/DEMULTIPLEXERS

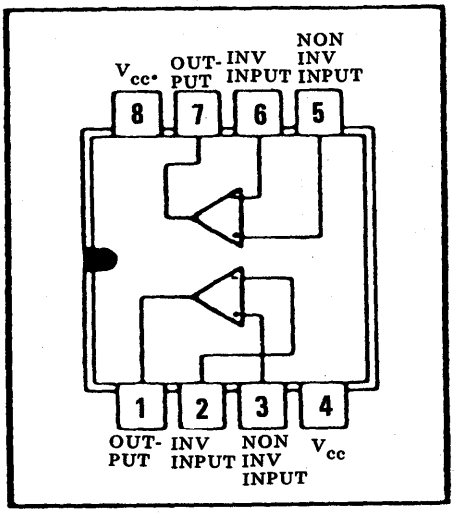


positive logic: see function table

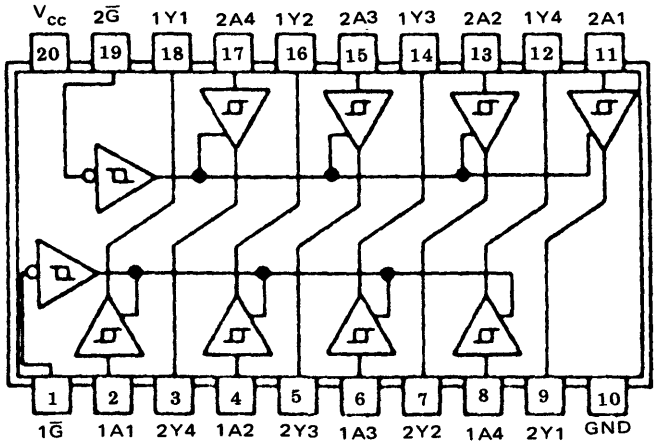
INPUTS				OUTPUTS			
SELECT		STROBE	DATA	1Y0	1Y1	1Y2	1Y3
B	A	1G	1C				
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA	2Y0	2Y1	2Y2	2Y3
B	A	2G	2C				
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

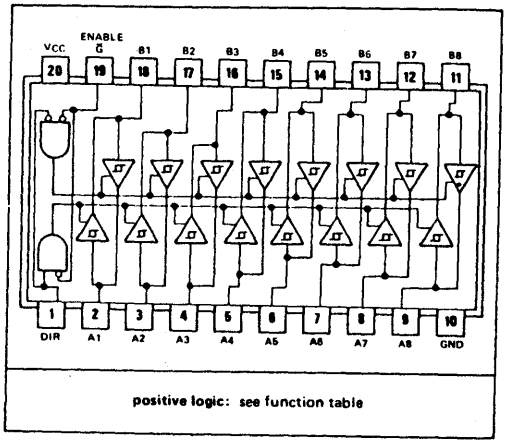
TEXAS INSTRUMENTS	AMPEX	JFET-INPUT OPERATIONAL
TL082	589-384	AMPLIFIERS



TEXAS INST SN74LS244	AMPEX 589-449	OCTAL BUFFERS/LINE DRIVERS/ LINE RECEIVERS NONINVERTED 3-STATE OUTPUTS



TEXAS INST SN74245	AMPEX 589-457	OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



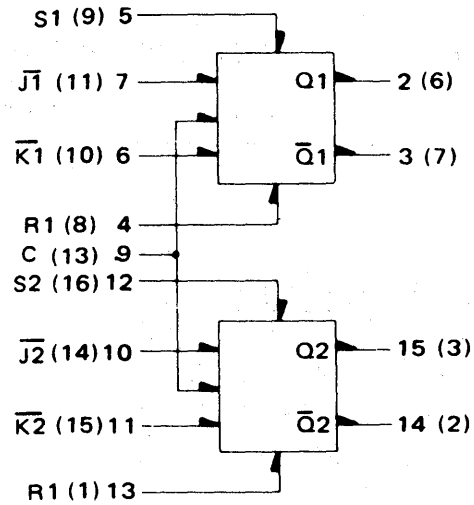
positive logic: see function table

FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

MOTOROLA	AMPEX	DUAL J-K MASTER-SLAVE
MC10135	589-508	FLIP-FLOP



CLOCK J-K TRUTH TABLE*

$\bar{J}$	$\bar{K}$	Q_{n+1}
L	L	$\bar{Q}_n$
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for J, K input condition present

N.D. = Not Defined

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

R-S TRUTH TABLE

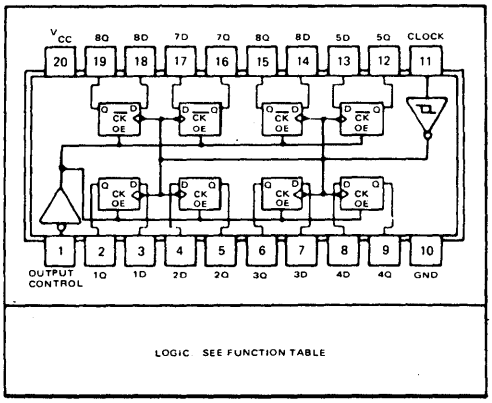
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

TEXAS INSTRUMENTS	AMPEX	OCTAL D-TYPE TRANSPARENT
SN74S374J	589-536	LATCH AND EDGE-TRIGGERED FLIP-FLOP

'LS374, 'S374
FUNCTION TABLE

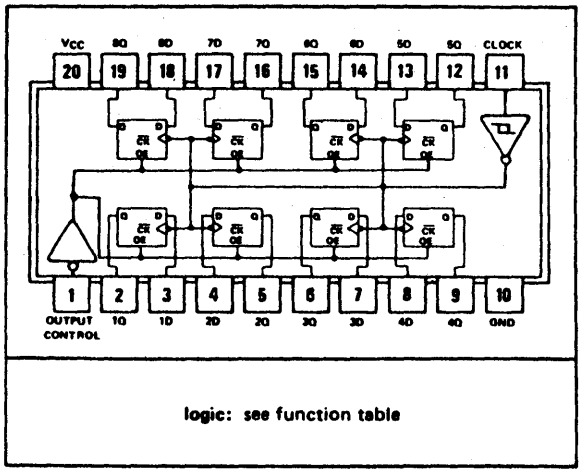
OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

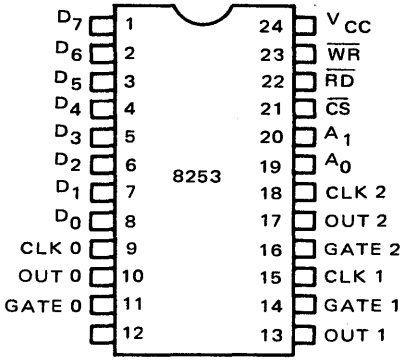
See explanation of function tables on page 3-8.

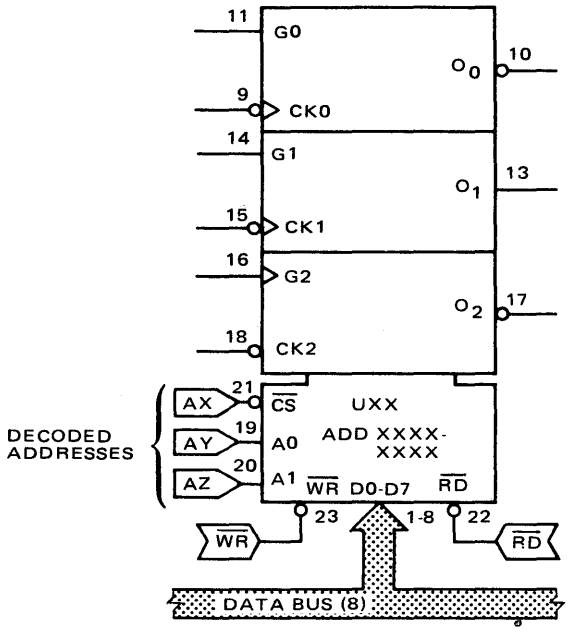


TEXAS INST	AMPEX	OCTAL D-TYPE TRANSPARENT LATCHES
SN74374	589-537	AND EDGE-TRIGGERED FLIP-FLOPS

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z



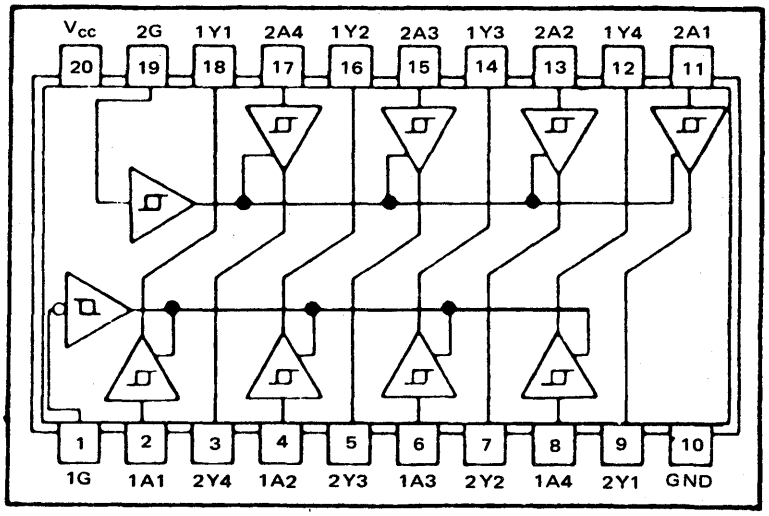




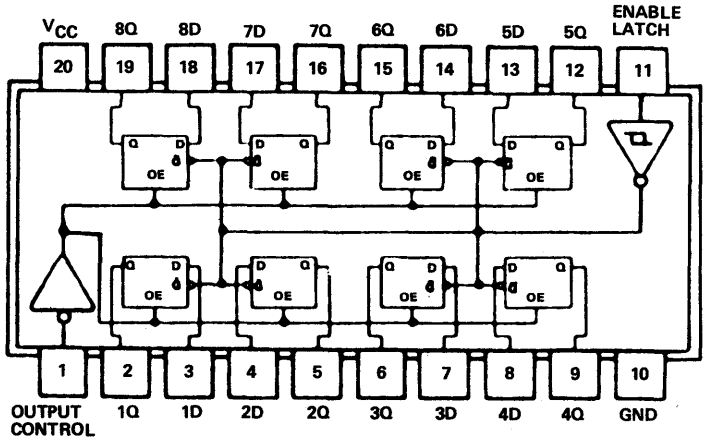
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	LOAD COUNTER NO. 0
0	1	0	0	1	LOAD COUNTER NO. 1
0	1	0	1	0	LOAD COUNTER NO. 2
0	1	0	1	1	WRITE MODE WORD
0	0	1	0	0	READ COUNTER NO. 0
0	0	1	0	1	READ COUNTER NO.1
0	0	1	1	0	READ COUNTER NO. 2
0	0	1	1	1	NO-OPERATION 3 STATE
1	X	X	X	X	DISABLE 3 STATE
0	1	1	X	X	NO OPERATION 3 STATE

D0-D7	Bidirectional data bus.
CLK 0, 1, 2	Counter clock inputs.
GATE 0, 1, 2	Enables counter (0, 1, 2) when high.
OUT 0, 1, 2	Counter outputs.
$\overline{WR}$	Write (asserted low)—allows data to enter counters and mode to enter control register.
$\overline{RD}$	Read (asserted low)—allows counter contents onto data bus.
$\overline{CS}$	Chip select (asserted low).
A0, A1	Two-bit address selects counter.

TEXAS INSTRUMENTS	AMPEX	OCTAL BUFFERS AND LINE DRIVERS
SN74LS241	589-751	WITH 3-STATE OUTPUTS



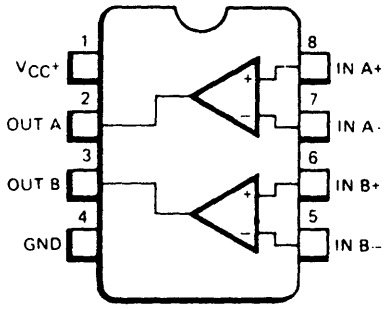
TEXAS INSTRUMENTS	AMPEX	OCTAL D-TYPE TRANSPARENT
SN74LS373	589-752	LATCH AND EDGE-TRIGGERED FLIP-FLOP



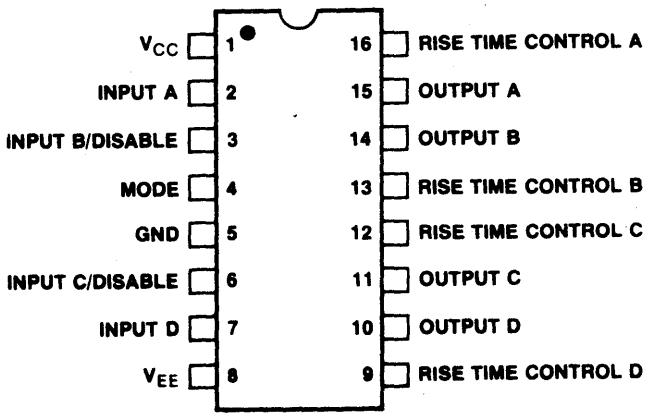
FUNCTION TABLE

OUTPUT ENABLE	ENABLE LATCH	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

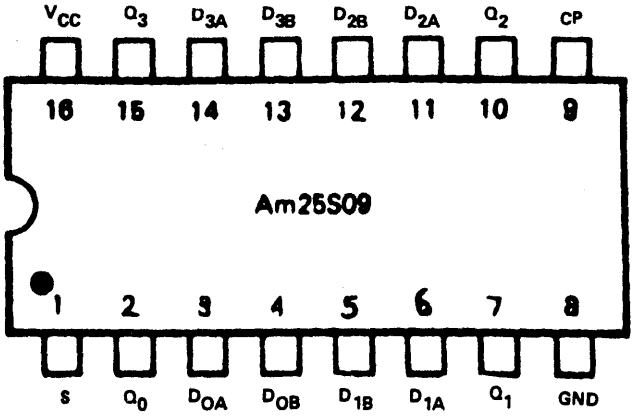
FAIRCHILD 9637	AMPEX 590-193	DUAL DIFFERENTIAL LINE RECEIVER



FAIRCHILD DS3692	AMPEX 590-194	DIFFERENTIAL LINE DRIVER

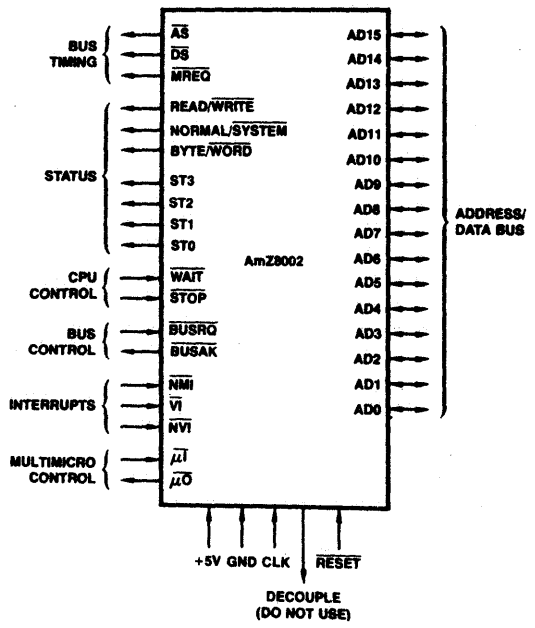


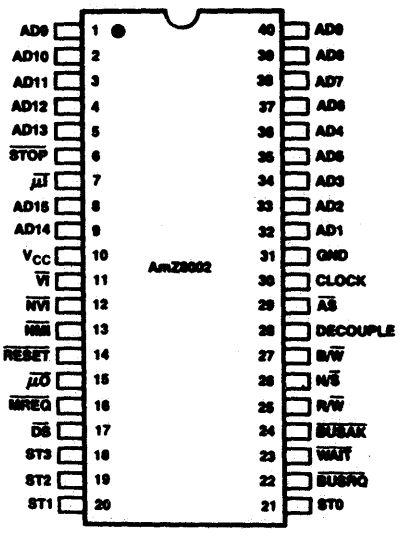
ADVANCE MIRCO DEVICES	AMPEX	QUAD TWO-INPUT
AM25S09	590-227	HIGH-SPEED REGISTER



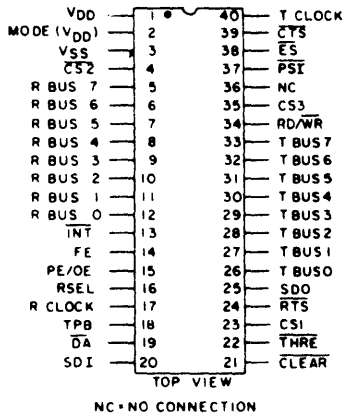
ADVANCED MICRO DEVICES	AMPEX	16-BIT MICROPROCESSOR
AMZ8002	590-866	

LOGIC SYMBOL





RCA CDP1854	AMPEX 590-932	UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER



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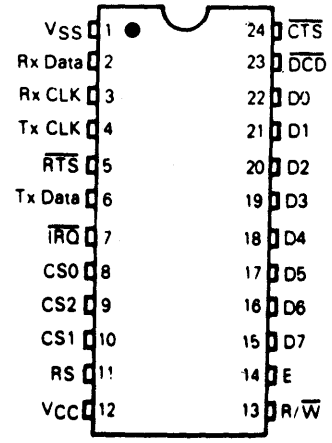

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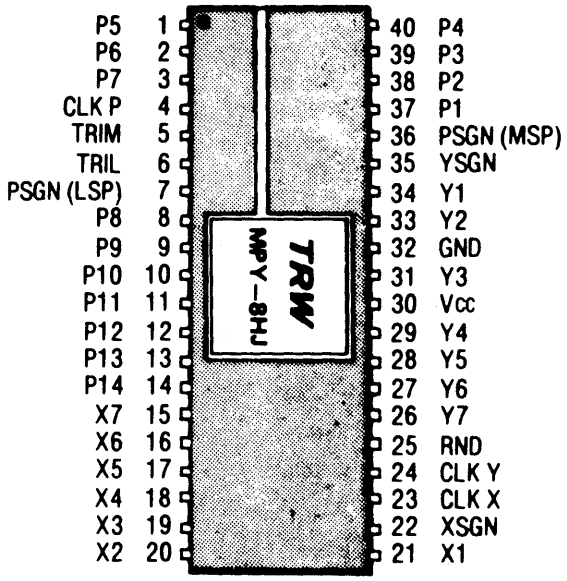

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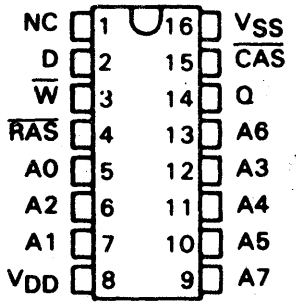

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