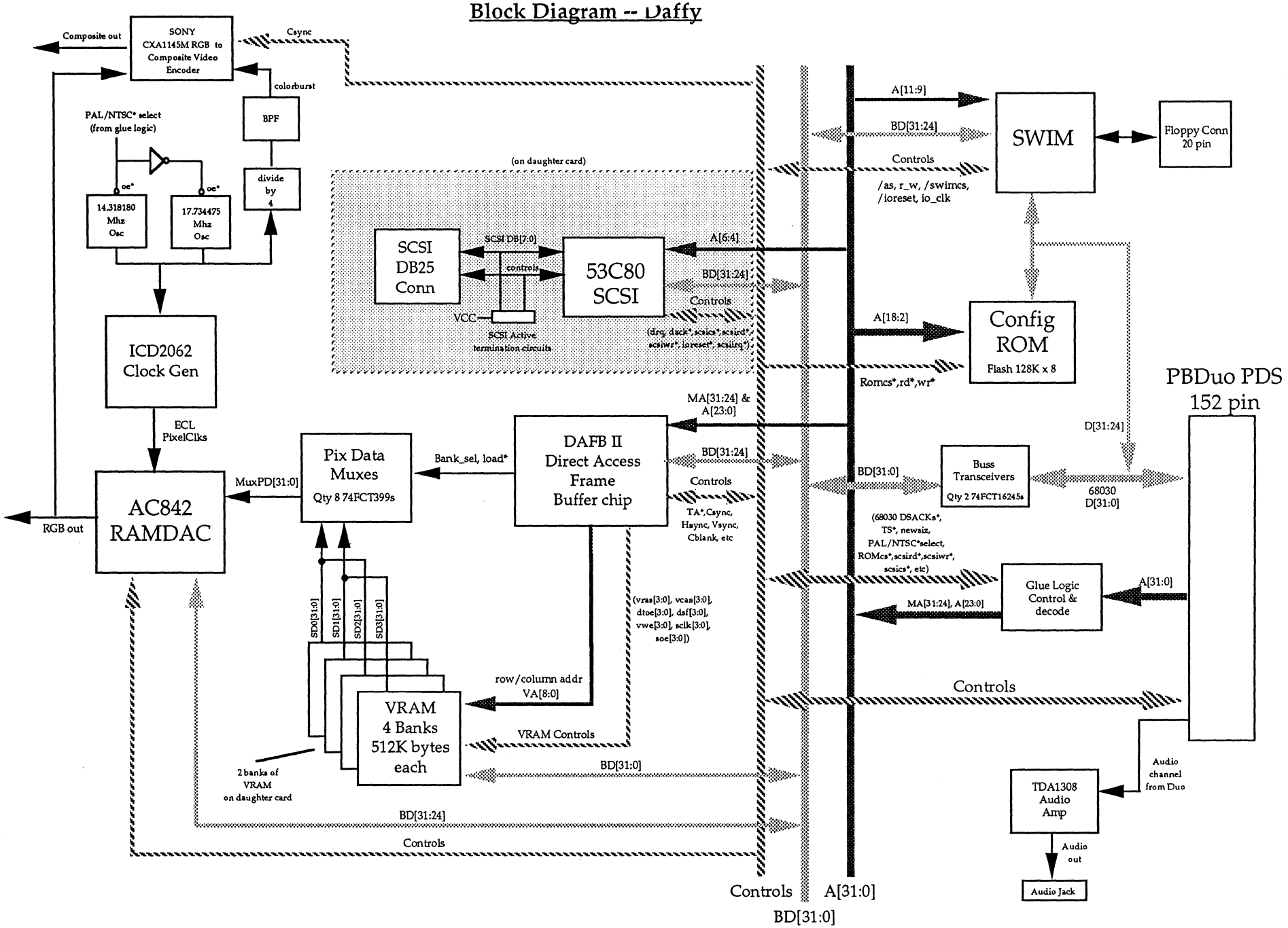
Block Diagram -- Daffy



rdn 7/15/93

REV.	ZONE	ECN#	REVISION	APPD	DATE
A			PRODUCTION RELEASE		

NOTE:
MANUFACTURERS RECEIVING APPLE APPROVED VENDOR STATUS FOR THEIR PRODUCT UNDER THIS PART NUMBER PLEASE NOTE: You must not change your part design, materials or manufacturing process from those used for the original samples submitted to and approved by Apple without written approval of Apple. Proposed changes determined by Apple to be significant, will require the manufacturer to submit new samples and/or data for review and approval prior to product shipments to Apple.

(Refer to burn-in specification 344S0128)

	METRIC				Apple Computer, Inc.
DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN BRACKETS [ ] ARE IN INCHES. TOLERANCES: X.X ± 0.3 [.01]; X.XX ± 0.13 [.005]; X.XXX ± 0.03 [.001]; ANGLEs ± 0.1 or as noted. DO NOT SCALE DRAWING	DRAFT B.T.	10/24/91	DESIGN CK	10/21/91	NOTICE OF PROPRIETARY PROPERTY. THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: (I) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (II) NOT TO REPRODUCE OR COPY IT (III) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART (IV) ALL RIGHTS RESERVED
	ENG APPD	1/8/91	MFG APPD	/ /	
	QA APPD	/ /	DESIGNER	/ /	TITLE: IC, ASIC, CMOS, DAFB II, (Direct Access Frame Buffer Controller II), 160-PIN PQFP
	RELEASE	/ /	SCALE: NONE		
	MATERIAL/FINISH NOTED AS APPLICABLE		SIZE A		DRAWING NUMBER 343S0128-A; SHT 1/98

1.0 SCOPE: This specifies the parametric requirements for the DAFB II ("Direct Access Frame Buffer Controller II") I.C., which is designed to control a video frame buffer and interface it to a 68040 system bus. The part was originally designed using the VTI VGT300-046 gate array, a 1µ CMOS process. This device is packaged in a 160-pin PQFP.

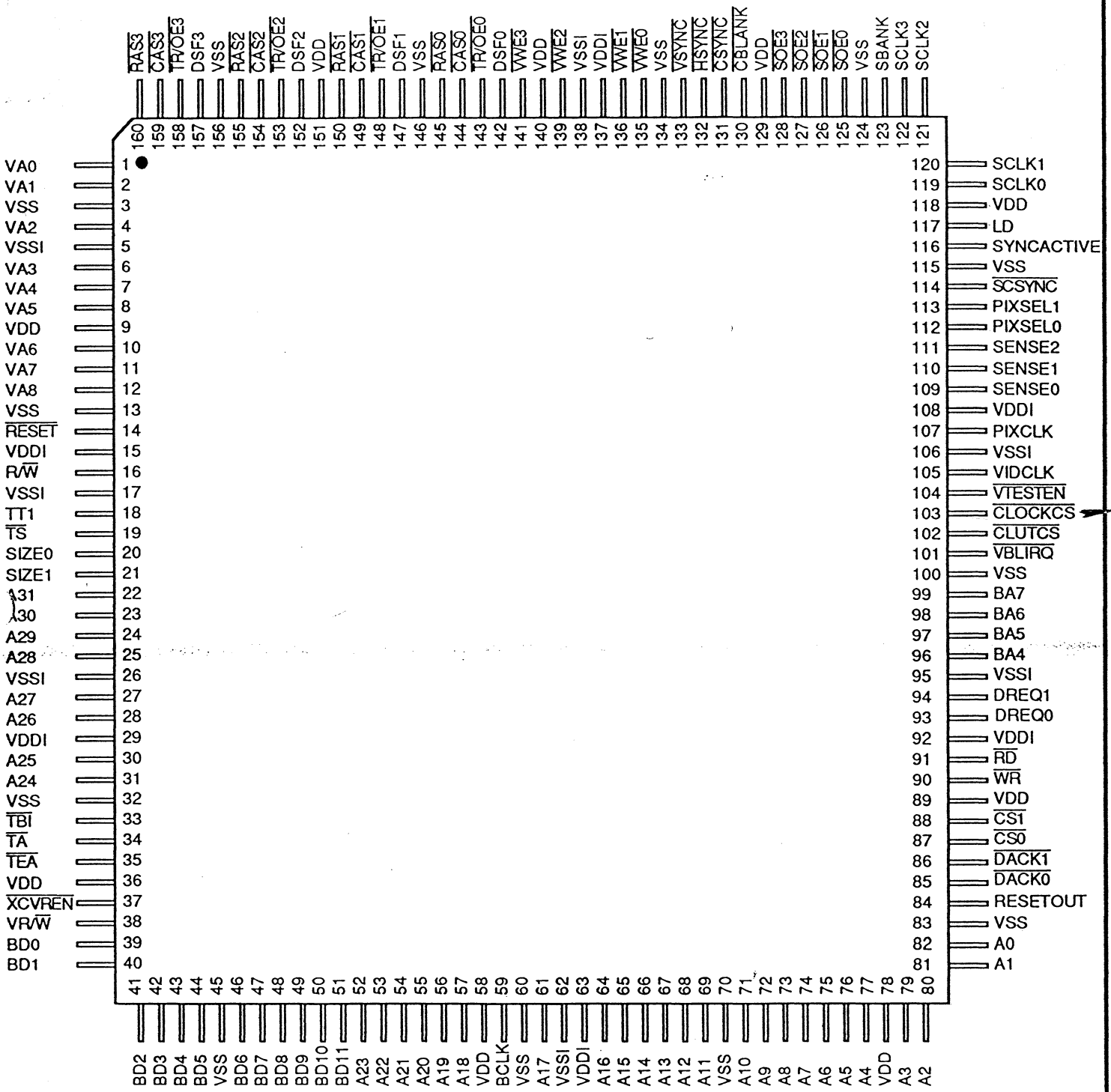


FIGURE 1. PIN CONFIGURATION

Apple Computer, Inc.

SIZE A | DRAWING NUMBER 343S0128-A | SCALE: NONE | SHT 2 OF 98

TABLE 1. PIN DESCRIPTION

Signal Name	Signal Description	Type	# of Pins
68040 Signals			
A(31-0)	Address Bus	Input	32
SIZE(1-0)	Transfer Size Bits	Input	2
TT1	Transfer Type Bit 1	Input	1
BD(11-0)	Buffered Data Bus (bits 11-0)	I/O	12
$\overline{TBI}$	Transfer Burst Inhibit	I/O	1
$\overline{TS}$	Transfer Start	Input	1
$\overline{TA}$	Transfer Acknowledge	I/O	1
$\overline{TEA}$	Transfer Error Acknowledge	I/O	1
R/$\overline{W}$	Read/Write Line	Input	1
VRAM Control Signals			
$\overline{VA(8-0)}$	VRAM Address Bus	Output	9
$\overline{RAS(3-0)}$	Row Address Strobe	Output	4
$\overline{CAS(3-0)}$	Column Address Strobe	Output	4
$\overline{TR/OE(3-0)}$	Data Transfer / Output Enable	Output	4
DSF(3-0)	Special Function Enable	Output	4
$\overline{VWE(3-0)}$	VRAM Write Enable	Output	4
SCLK(3-0)	Serial Data Output Clock	Output	4
$\overline{SOE(3-0)}$	Serial Data Output Enable	Output	4
SBANK	Serial Data Mux Bank Select	Output	1
SCSI Control Signals			
$\overline{CS(1-0)}$	SCSI Chip Select	Output	2
$\overline{RD}$	SCSI Read Enable	Output	1
$\overline{WR}$	SCSI Write Enable	Output	1
$\overline{DACK(1-0)}$	SCSI DMA Acknowledge	Output	2
DREQ(1-0)	SCSI DMA Request	Input	2
RESETOUT	SCSI Chip Reset	Output	1
External Chip Controls			
$\overline{XCVREN}$	Data Bus Transceiver Enable	Output	1
VR/$\overline{W}$	Data Bus Transceiver Direction Control	Output	1
$\overline{CLOCKCS}$	Clock Generator Chip Select	Output	1
$\overline{CLUTCS}$	CLUT/DAC Select	Output	1
PIXSEL(1-0)	Pixel Clock Selects	Output	2
BA(7-4)	Buffered Address Lines (bits 7-4)	Output	4
Video Timing Signals			
$\overline{HSYNC}$	Horizontal Video Synchronization	Output	1
$\overline{VSYNC}$	Vertical Video Synchronization	Output	1
$\overline{CSYNC}$	Composite Video Synchronization	Output	1
$\overline{CBLANK}$	Composite Video Blanking	Output	1
$\overline{SCSYNC}$	Switched Composite Video Synchronization	Output	1
SYNCACTIVE	$\overline{SCSYNC}$ Output Enable	Input	1

TABLE 1. PIN DESCRIPTION (CONT)

Signal Name	Signal Description	Type	# of Pins
Clocks			
BCLK	CPU Clock (25 or 33 MHZ)	Input	1
VIDCLK	12 - 30 MHz Video Clock	Input	1
PIXCLK	57 MHz TTL Pixel Clock	Input	1
LD	12 - 57 MHz Pixel Data Load Clock	Output	1
Other Signals			
$\overline{\text{RESET}}$	Asynchronous Reset	Input	1
$\overline{\text{VBLIRQ}}$	Interrupt Request	Output	1
SENSE(2-0)	Monitor Type Sense Lines	I/O	3
Test Signals			
$\overline{\text{VTESTEN}}$	Tristate Output Disable	Input	1
Core Power			
+5V	+5 Volts (V_{DDI})	Input	6
GND	Ground (V_{SSI})	Input	7
I/O Power			
+5V	+5 Volts (V_{DD})	Input	9
GND	Ground (V_{SS})	Input	13
TOTAL			160

NOTE:
1. All bidirectional and output signals are tristate pins.

TABLE 2. PIN I/O DEVICE CHARACTERISTICS

Pin #	Signal Name	Input			Output			Pad Macro
		TTL	Schmidt	CMOS	Tristate	BiDir	OD†	
1	VA0				√			PT6O05
2	VA1				√			PT6O05
4	VA2				√			PT6O05
6	VA3				√			PT6O05
7	VA4				√			PT6O05
8	VA5				√			PT6O05
10	VA6				√			PT6O05
11	VA7				√			PT6O05
12	VA8				√			PT6O05
14	$\overline{\text{RESET}}$		√					PC6D00
16	R/$\overline{\text{W}}$	√						PC6D00
18	TT1	√						PC6D00
19	$\overline{\text{TS}}$	√						PC6D00
20	SIZE0	√						PC6D00
21	SIZE1	√						PC6D00
22	A31	√						PC6D00
23	A30	√						PC6D00
24	A29	√						PC6D00
25	A28	√						PC6D00
27	A27	√						PC6D00
28	A26	√						PC6D00
30	A25	√						PC6D00
31	A24	√						PC6D00
33	$\overline{\text{TBI}}$	√				√		PT6O44
34	$\overline{\text{TA}}$	√				√		PT6O44
35	$\overline{\text{TEA}}$	√				√		PT6O44
37	$\overline{\text{XCVREN}}$				√			PT6O02
38	VR/$\overline{\text{W}}$				√			PT6O03
39	BD0	√				√		PT6O42
40	BD1	√				√		PT6O42
41	BD2	√				√		PT6O42
42	BD3	√				√		PT6O42
43	BD4	√				√		PT6O42
44	BD5	√				√		PT6O42
46	BD6	√				√		PT6O42
47	BD7	√				√		PT6O42
48	BD8	√				√		PT6O42
49	BD9	√				√		PT6O42
50	BD10	√				√		PT6O42
51	BD11	√				√		PT6O42
52	A23	√						PC6D00
53	A22	√						PC6D00
54	A21	√						PC6D00
55	A20	√						PC6D00
56	A19	√						PC6D00
57	A18	√						PC6D00
59	BCLK	√						PT6C12
61	A17	√						PC6D00
64	A16	√						PC6D00
65	A15	√						PC6D00

TABLE 2. PIN I/O DEVICE CHARACTERISTICS (cont'd)

Pin #	Signal Name	Input			Output			Pad Macro
		TTL	Schmidt	CMOS	Tristate	BiDir	OD†	
66	A14	√						PC6D00
67	A13	√						PC6D00
68	A12	√						PC6D00
69	A11	√						PC6D00
71	A10	√						PC6D00
72	A9	√						PC6D00
73	A8	√						PC6D00
74	A7	√						PC6D00
75	A6	√						PC6D00
76	A5	√						PC6D00
77	A4	√						PC6D00
79	A3	√						PC6D00
80	A2	√						PC6D00
81	A1	√						PC6D00
82	A0	√						PC6D00
84	RESETOUT				√			PT6O03
85	$\overline{\text{DACK0}}$				√			PT6O03
86	$\overline{\text{DACK1}}$				√			PT6O03
87	$\overline{\text{CS0}}$				√			PT6O03
88	$\overline{\text{CS1}}$				√			PT6O03
90	$\overline{\text{WR}}$				√			PT6O03
91	$\overline{\text{RD}}$				√			PT6O03
93	DREQ0	√						PC6D00
94	DREQ1	√						PC6D00
96	BA4				√			PT6O02
97	BA5				√			PT6O02
98	BA6				√			PT6O02
99	BA7				√			PT6O02
101	$\overline{\text{VBLIRQ}}$				√			PT6O02
102	$\overline{\text{CLUTCS}}$				√			PT6O02
103	$\overline{\text{CLOCKCS}}$				√			PT6O02
104	$\overline{\text{VTESTEN}}$		√					PC6D00
105	VIDCLK	√						PC6D00
107	PIXCLK	√						PC6D00
109	SENSE0			√		√		PT6O42
110	SENSE1			√		√		PT6O42
111	SENSE2			√		√		PT6O42
112	PIXSEL0				√			PT6O04
113	PIXSEL1				√			PT6O02
114	$\overline{\text{SCSYNC}}$				√			PT6O03
116	SYNCACTIVE	√						PC6D00
117	LD	√				√		PT6O45
119	SCLK0				√			PT6O04
120	SCLK1				√			PT6O04
121	SCLK2				√			PT6O04
122	SCLK3				√			PT6O04
123	SBANK				√			PT6O04
125	$\overline{\text{SOE0}}$				√			PT6O03
126	$\overline{\text{SOE1}}$				√			PT6O03
127	$\overline{\text{SOE2}}$				√			PT6O03

TABLE 2. PIN I/O DEVICE CHARACTERISTICS (cont'd)

Pin #	Signal Name	Input			Output			Pad Macro
		TTL	Schmidt	Pullup	Tristate	BiDir	OD†	
128	$\overline{SOE3}$				√			PT6O03
130	$\overline{CBLANK}$				√			PT6O02
131	$\overline{CSYNC}$				√			PT6O03
132	$\overline{HSYNC}$				√			PT6O03
133	$\overline{VSYNC}$				√			PT6O03
135	$\overline{VWE0}$				√			PT6O03
136	$\overline{VWE1}$				√			PT6O03
139	$\overline{VWE2}$				√			PT6O03
141	$\overline{VWE3}$				√			PT6O03
142	DSF0				√			PT6O03
143	$\overline{TR/OE0}$				√			PT6O03
144	$\overline{CAS0}$				√			PT6O04
145	$\overline{RAS0}$				√			PT6O04
147	DSF1				√			PT6O03
148	$\overline{TR/OE1}$				√			PT6O03
149	$\overline{CAS1}$				√			PT6O04
150	$\overline{RAS1}$				√			PT6O04
152	DSF2				√			PT6O03
153	$\overline{TR/OE2}$				√			PT6O03
154	$\overline{CAS2}$				√			PT6O04
155	$\overline{RAS2}$				√			PT6O04
157	DSF3				√			PT6O03
158	$\overline{TR/OE3}$				√			PT6O03
159	$\overline{CAS3}$				√			PT6O04
160	$\overline{RAS3}$				√			PT6O04

† OD stands for "Open Drain."

NOTE:

2. Pins 3, 13, 32, 62, 70, 83, 100, 115, 124, 134, 138, 146, and 156 ('V_{SS}' pins) are ground pins and have pad macro PC6VS2. Pins 9, 36, 63, 78, 89, 118, 129, 137, 140, and 151 ('V_{DD}' pins) are power pins and have pad macro PC6VD2. Pins 5, 17, 26, 95, and 106 ('V_{SSI}' pins) are ground pins and have pad macro PC6VS1. Pins 15, 29, 92, and 108 ('V_{DDI}' pins) are power pins and have pad macro PC6VD1. Pin 60 ('V_{SS}' pin) is a ground pin and has pad macro PT6C12. Pin 58 ('V_{DD}' pin) is a power pin and has pad macro PT6C12.

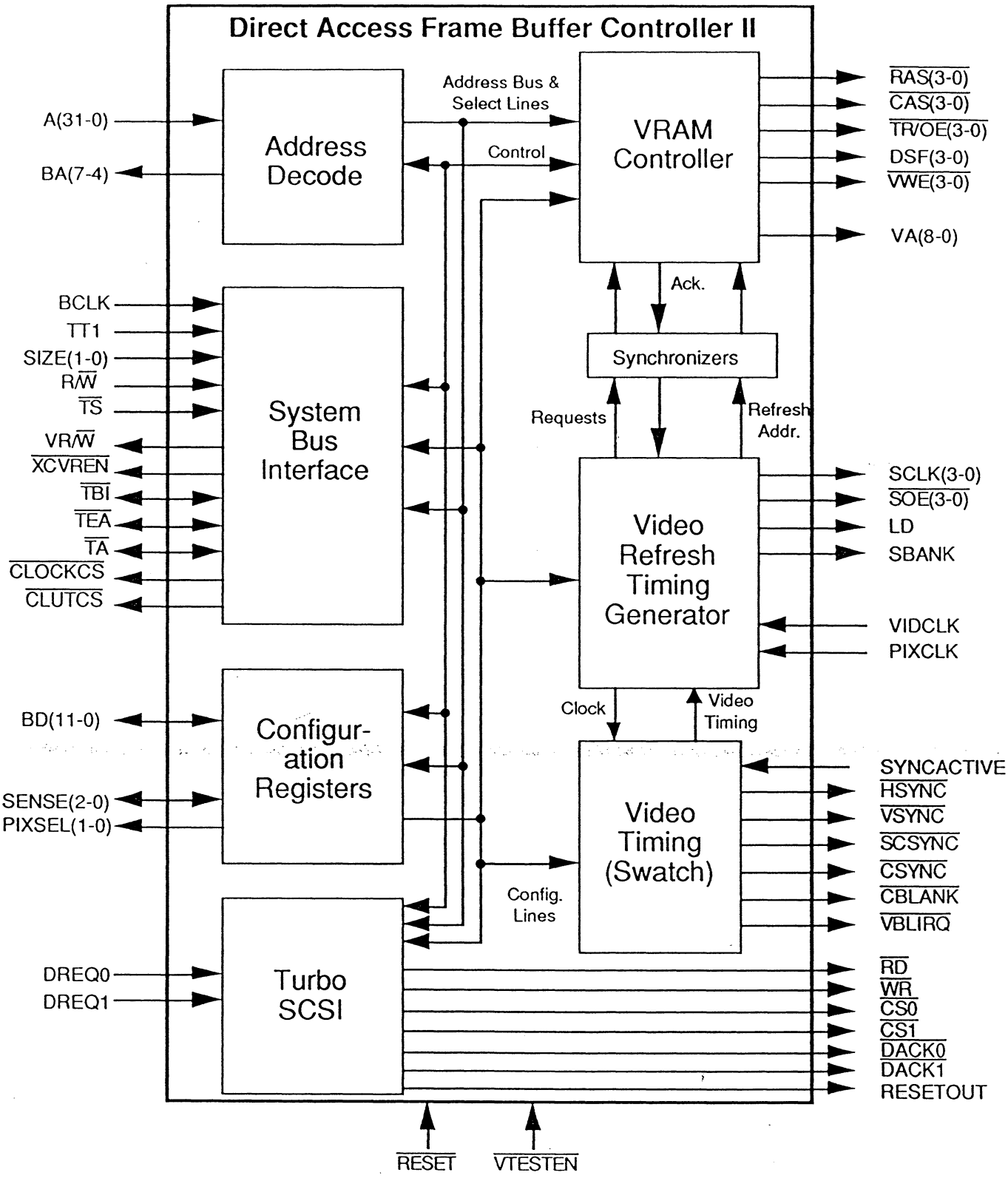


FIGURE 2. BLOCK DIAGRAM

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 8 OF 98

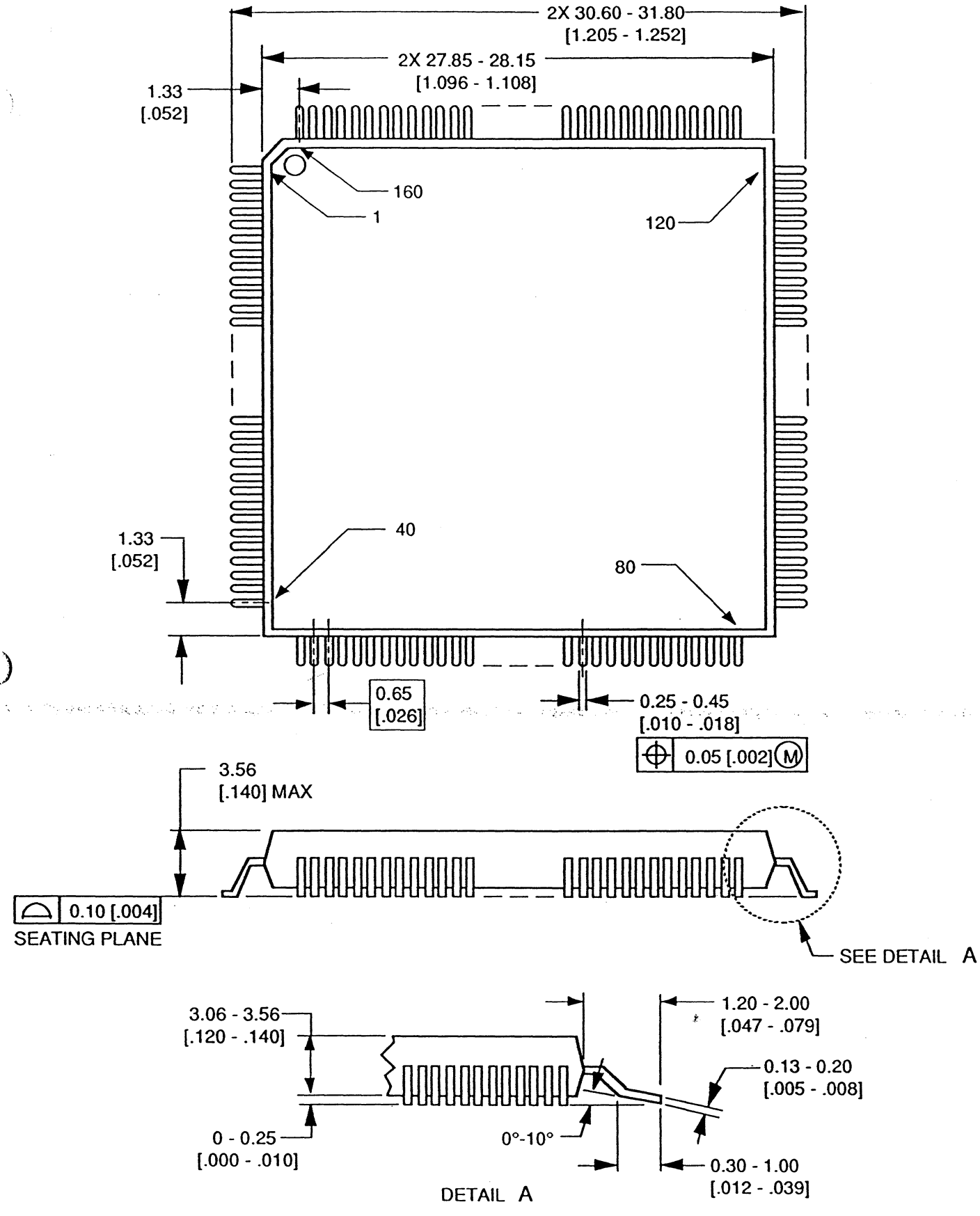


FIGURE 3. DIMENSIONS

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 9 OF 98

2.0 APPLICABLE DOCUMENTS (latest revision):

MIL-STD-202 Test methods for electronic and electrical component parts.
MIL-STD-883 Test methods and procedures for microelectronics.

0 REQUIREMENTS:

3.1 PHYSICAL:

3.1.1 PACKAGE: Void free plastic 160-pin PQFP package. Dimensions per Figure 3.

3.1.2 COMPONENT MARKINGS: The component shall be marked on the top side with the manufacturer's name (or industry recognized logo), manufacturing date code, fab and assembly codes for traceability, Apple part number (including current revision level), Maskwork Rights notice symbol (a circled "M" as shown in example below), copyright symbol (©), appropriate year(s), and the Apple name or logo.

EXAMPLE: 343S0128-A
Ⓜ Ⓒ 1991 Apple

3.1.3 DIE MARKINGS: The die shall be marked on the top metal layer with the Apple part number (no revision level), Maskwork Rights notice symbol (a circled "M" as shown in example below), copyright symbol (©), appropriate year(s), and the complete Apple name.

EXAMPLE: 343S0128
Ⓜ Ⓒ 1991 Apple Computer, Inc.

The © has the year associated with it. In no case does the circled "M" have an associated year. To emphasize these relationships the circled "M" must be physically isolated from any printed year.

3.1.4 SOLDERABILITY: Leads solderability must meet MIL-STD-202, Method 208. Prior to test, the devices shall be subjected to steam aging for a period of 8 hours.

3.2 ELECTRICAL:

3.2.1 ELECTROSTATIC DISCHARGE SENSITIVITY: The minimum electrostatic discharge voltage per pin is ±2000 volts as specified in MIL-STD-883, Method 3015.3 (i.e., C = 100 pF, R = 1.5KΩ).

3.2.2 LATCH-UP TEST: The minimum latch-up current for all pins except ground is 50mA in both positive and negative directions. This applies to full temperature and power supply ranges.

3.2.3 PIN CONFIGURATION: Per Figure 1.

3.2.4 PIN DESCRIPTION: Per Table 1.

3.2.5 PIN I/O DEVICE CHARACTERISTICS: Per Table 2.

3.2.6 BLOCK DIAGRAM: Per Figure 2.

3.2.7 ABSOLUTE MAXIMUM RATINGS: Per Table 3.

3.2.8 RECOMMENDED OPERATING CONDITIONS: Per Table 4.

3.2.9 DC ELECTRICAL CHARACTERISTICS: Per Table 5.

3.2.10 AC TIMING SPECIFICATIONS: Per Tables 6-11, Figures 4-45.

RESISTANCE TO SOLDERING HEAT PROFILES:

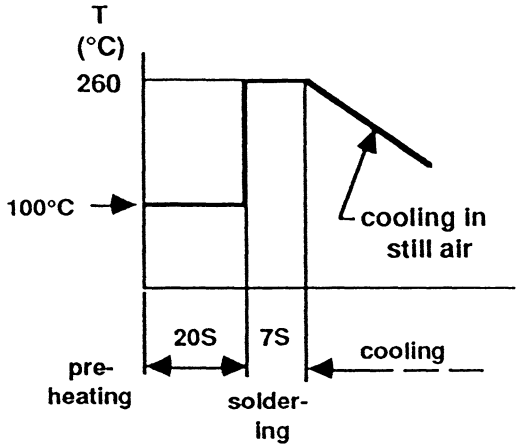


FIGURE A. WAVE/HAND SOLDERING

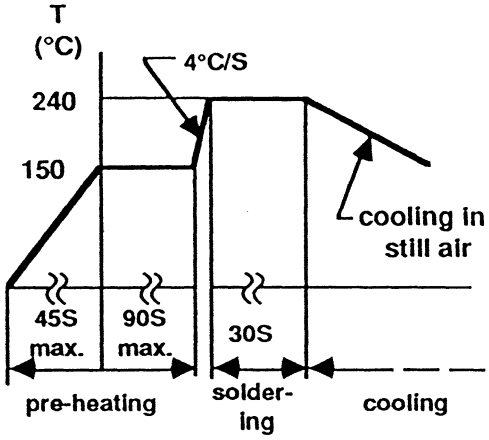


FIGURE B. INFRARED SOLDERING

3.3 ENVIRONMENTAL:

3.3.1 RESISTANCE TO SOLDERING HEAT:

a) Wave or hand soldering: With a 100°C preheat for 20 seconds, the components shall be totally immersed in molten solder, 260 ± 3°C for 7 ± 1 second per MIL-STD-202, Method 210, condition B (Per Figure A).

b) IR reflow solder: Preheat at 3°C/sec to 150°C, and using 60/40 solder, IR at 240°C for 30 seconds (Per Figure B).

c) Component must withstand two (section 3.3.1.b) IR reflow solder cycles with a cool-down in between.

d) Component must withstand one (section 3.3.1.b) IR reflow solder cycle followed, after a cooldown, by a (section 3.3.1.a) wave or hand soldering cycle.

After resistance to soldering heat test, there shall be no evidence of leaching or cracking and the parts shall meet all electrical and mechanical specifications.

3.3.2 **CLEANING:** Parts must be washable in standard flux removal solvent and must not trap any cleaning liquids.

4.0 **QUALITY ASSURANCE PROVISIONS:** Parts shall be inspected to assure compliance to the requirements of this specification.

5.0 **PACKAGING:** Parts shall be packaged according to requirements specified in purchase order for safe delivery at Apple or Apple designated contractor. (Parts requiring Tape & Reel shall meet the proper Tape & Reel specification per the purchase order.)

TABLE 3. ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	Supply Voltage	-0.3	7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Operating Temperature	0	70	° C
T_{STG}	Storage Temperature	-55	150	° C

TABLE 4. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	Supply Voltage	4.5	5.5	V
V_{IN}	Input Voltage	0	5	V
T_A	Operating Temperature	0	70	°C
T_{STG}	Storage Temperature	-55	150	°C

TABLE 5. DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_A = 0 to +70 °C)

SYMBOL	CHARACTERISTIC		CONDITION	MIN	MAX	UNIT
V_{DD}	Power Supply Voltage			4.5	5.5	V
I_{DDS}	Power Supply Current	Static	V_{DD} = 5.5V		225	mA
I_{DDQ}		Quiesent	V_{DD} = 5.5V		100	µA
V_{IL}	Input Low Voltage	TTL (4.)		-0.5	0.8	V
		CMOS (4.)		-0.5	0.3 x V_{DD}	V
V_{IH}	Input High Voltage	TTL (4.)		2.0	V_{DD}	V
		CMOS (4.)		0.7 x V_{DD}	V_{DD}	V
I_{IN}	Input Leakage Current		0V ≤ V_{IN} ≤ V_{DD}		10	µA
I_{OZ}	Tristate Leakage Current		V_{OUT} = 0V to V_{DD}		10	µA
V_{OL}	Output Low Voltage		I_{OL} = 4, 8, 12, 16 mA (3.)		0.4	V
			I_{OL} = 1 µA		0.05	V
V_{OH}	Output High Voltage		I_{OH} = 4, 8, 12, 16 mA (3.)	2.4		V
			I_{OH} = 1 µA	V_{DD} - 0.05		V
C_{IN}	Capacitance	Inputs			10	pF
C_{OUT}	V_{IN} = 0V, f = 1 MHz	Outputs			10	pF
C_{IO}		I/O's			10	pF

NOTES:

3. Maximum output low current, I_{OL}, and maximum output high current, I_{OH}, depend on the output macro cell being used. Macros PT6O02 and PT6O42 have an 4 mA drive capability, PT6O03 has an 8 mA drive capability, PT6O04 and PT6O44 have a 12 mA drive capability, and PT6O05 and PT6O45 have a 16 mA drive capability.

4. SENSE(2-0) are CMOS level inputs. All other inputs are TTL level.

TABLE 6. INPUT CLOCK AC TIMING SPECIFICATIONS (See Figures 4–5)

NUM	CHARACTERISTIC	MIN	MAX	UNIT
	Frequency of Operation (BCLK)		33	MHz
1[6]	BCLK Cycle Time	30		ns
2	BCLK Pulse Width High (measured @ 2.0 V)	12		ns
3	BCLK Pulse Width Low (measured @ 0.8 V)	12		ns
4, 5	BCLK Rise/Fall Time		4	ns
	Frequency of Operation (VIDCLK)	12	50	MHz
6[6]	VIDCLK Cycle Time	20		ns
7	VIDCLK Pulse Width High (measured @ 2.0 V)	6		ns
8	VIDCLK Pulse Width Low (measured @ 0.8 V)	6		ns
9,10	VIDCLK Rise/Fall Time		4	ns
	Frequency of Operation (PIXCLK)		58	MHz
11[6]	PIXCLK Cycle Time	17		ns
12	PIXCLK Pulse Width High (measured @ 2.0 V)	5		ns
13	PIXCLK Pulse Width Low (measured @ 0.8 V)	5		ns
14,15	PIXCLK Rise/Fall Time		4	ns
16,17	LD to VIDCLK Falling/Rising Edge	5	14	ns

NOTES:

5. All values in the previous AC Timing Specification tables are for worst case timing with V_{DD} = 4.5 - 5.5 V, V_{SS} = 0 V, T_A = 0 to +70 °C, worst case processing, and 50 pF load capacitances. Derate the maximum times by 0.5 ns/10 pF for VA(8-0) and LD, by 0.6 ns/10 pF for $\overline{\text{RAS}}$(3-0), $\overline{\text{CAS}}$(3-0), SCLK(3-0), SBANK, $\overline{\text{TBI}}$, $\overline{\text{TEA}}$, $\overline{\text{TA}}$, and PIXSEL0, by 0.9 ns/10 pF for $\overline{\text{TR/OE}}$(3-0), $\overline{\text{VWE}}$(3-0), DSF(3-0), $\overline{\text{SOE}}$(3-0), $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{CSYNC}}$, $\overline{\text{SCSYNC}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS1}}$, $\overline{\text{CS0}}$, $\overline{\text{DACK1}}$, $\overline{\text{DACK0}}$, RESETOUT, VR/$\overline{\text{W}}$, and by 1.3 ns/10 pF for all other outputs. Output high levels are measured at 2.4 V. Output low levels are measured at 0.4 V.

6. BCLK, VIDCLK, and PIXCLK are asynchronous signals.

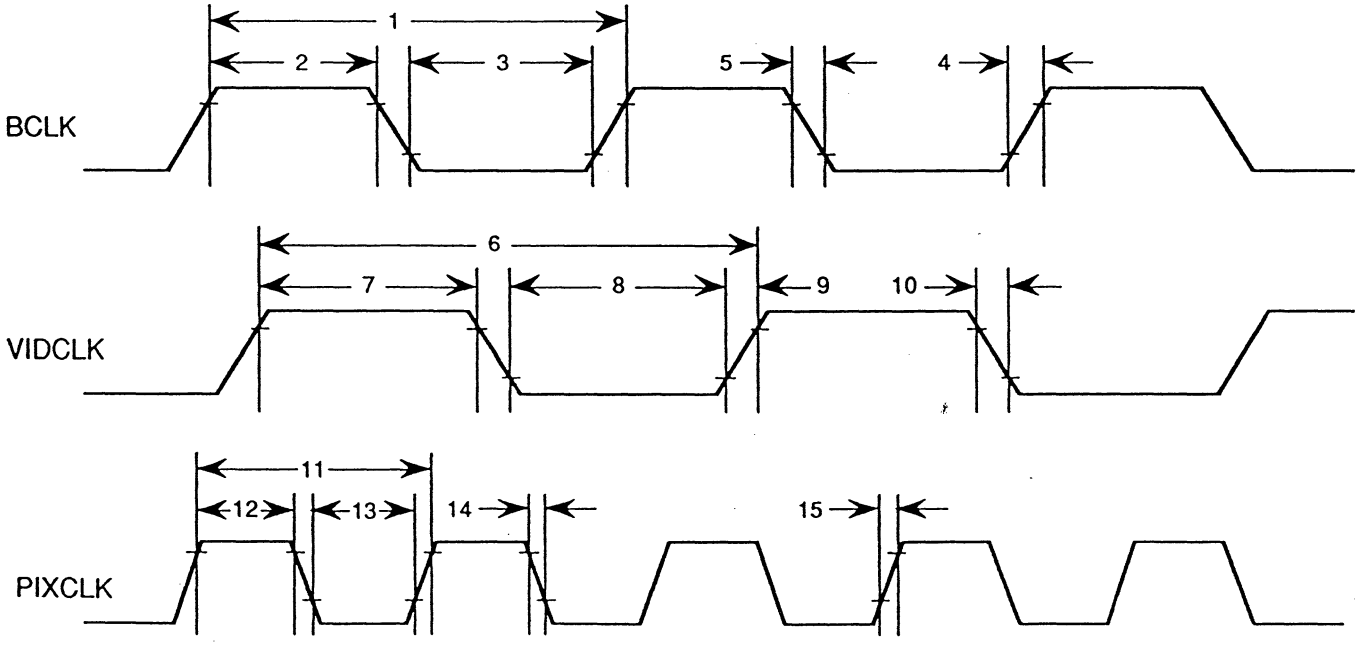


FIGURE 4. INPUT CLOCK TIMING

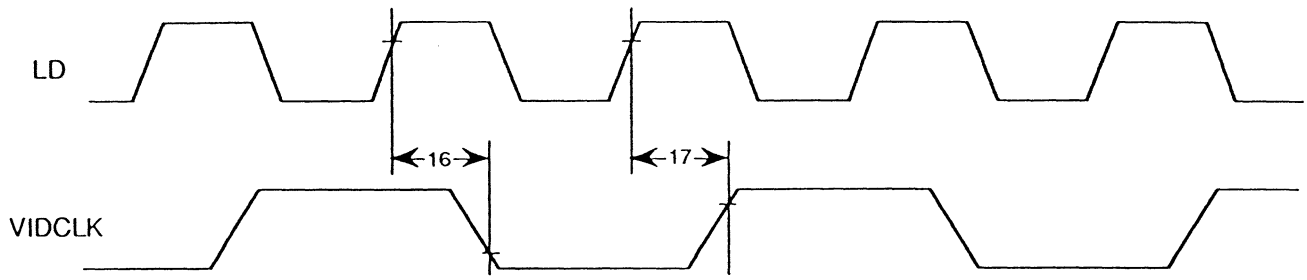


FIGURE 5. LD-to-VIDCLK INPUT CLOCK TIMING

TABLE 7. CPU INTERFACE AC TIMING SPECIFICATIONS (See Figures 6–9)

NUM	CHARACTERISTIC	MIN	MAX	UNIT
18	$\overline{TS}$, A(31-0), SIZE(1-0), TT1, R/$\overline{W}$ Valid to BCLK (Input Setup)	5		ns
19	BCLK to $\overline{TS}$, A(31-23,6-0), SIZE(1-0), TT1, R/$\overline{W}$ Invalid (Input Hold)	5		ns
20	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TBI}$ Active		12	ns
21	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TBI}$ Valid		18	ns
22	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TBI}$ Invalid (Output Hold)	4		
23	BCLK low to $\overline{TA}$, $\overline{TEA}$, $\overline{TBI}$ High Impedance		12	ns
24	BCLK to $\overline{XCVREN}$ Valid		19	ns
25	BCLK to $\overline{XCVREN}$ Invalid (Output Hold)	4		ns
26	R/$\overline{W}$ to VR/$\overline{W}$ Valid		12	ns
27	$\overline{XCVREN}$ High to VR/$\overline{W}$ Invalid (Output Hold)	1		ns
28	BD(11-0) Valid to BCLK (Write Setup)	6		ns
29	BCLK to BD(11-0) Invalid (Write Hold)	4		ns
30	BCLK to BD(11-0) Valid		34	ns
31	BCLK to BD(11-0) Invalid	8		ns
32	BCLK to BD(11-0) High Impedance		15	ns
33[7]	BCLK to $\overline{CLOCKCS}$ (Active High) Valid		22	ns
34[7]	BCLK to $\overline{CLOCKCS}$ (Active High) Invalid	6		ns
35[7]	$\overline{CLOCKCS}$ (Active High) Pulse Width	58		ns
36[7]	BCLK to $\overline{CLOCKCS}$ (Active Low), $\overline{CLUTCS}$ Valid		21	ns
37[7]	BCLK to $\overline{CLOCKCS}$ (Active Low), $\overline{CLUTCS}$ Invalid	5		ns
38[7]	$\overline{CLOCKCS}$, $\overline{CLUTCS}$ (Active Low) Pulse Width (25 MHz Read Cycle)	117		ns
39	$\overline{CLOCKCS}$, $\overline{CLUTCS}$ (Active Low) Pulse Width (33 MHz Read Cycle)	117		ns
40	$\overline{CLOCKCS}$, $\overline{CLUTCS}$ (Active Low) Pulse Width (25 MHz Write Cycle)	77		ns
41	$\overline{CLOCKCS}$, $\overline{CLUTCS}$ (Active Low) Pulse Width (33 MHz Write Cycle)	87		ns
42	A(7-4) to BA(7-4)		11	ns

NOTE: 7. $\overline{CLOCKCS}$ may be active high or active low, and is controlled by a programmable DAFB II register bit.

TABLE 8. VRAM INTERFACE AC TIMING SPECIFICATIONS (See Figures 10–34)

NUM	CHARACTERISTIC	MIN	MAX	UNIT
43	A(20-2) to VA(8-0) Valid (VRAM Read, Row Address)		14	ns
44	BCLK to VA(8-0) Valid (VRAM Read - Column Address, VRAM Read Transfer - Row & Column Address)		19	ns
45	BCLK to VA(8-0) Invalid (Output Hold)	4		ns
46	BCLK to $\overline{\text{RAS}}$(3-0) Valid		14	ns
47	BCLK to $\overline{\text{RAS}}$(3-0) Invalid	3		ns
48	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Read, 25 MHz)	157		ns
49	BCLK to $\overline{\text{CAS}}$(3-0) Valid		14	ns
50	BCLK to $\overline{\text{CAS}}$(3-0) Invalid	3		ns
51	$\overline{\text{CAS}}$(3-0) Pulse Width (VRAM Read, 25 MHz)	77		ns
52	A(31-0) to DSF(3-0) Valid		18	ns
53	A(31-0) to DSF(3-0) Invalid		18	ns
54	BCLK to $\overline{\text{TR/OE}}$(3-0) Valid		18	ns
55	BCLK to $\overline{\text{TR/OE}}$(3-0) Invalid	4		ns
56	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Write, 25 MHz)	117		ns
57	$\overline{\text{CAS}}$(3-0) Pulse Width (VRAM Write, 25 MHz)	37		ns
58	BCLK Low to $\overline{\text{VWE}}$(3-0) Valid		17	ns
59	BCLK Low to $\overline{\text{VWE}}$(3-0) Invalid	3		ns
60	BCLK to DSF(3-0) Valid (VRAM Block Write, Read Transfer)		14	ns
61	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Full Read Transfer, 25 MHz)	157		ns
62	$\overline{\text{CAS}}$(3-0) Pulse Width (VRAM Read Transfer, 25 MHz)	37		ns
63	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Split Read Transfer, 25 MHz)	117		ns
64	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM CBR Refresh, 25 MHz)	117		ns
65	$\overline{\text{CAS}}$(3-0) Pulse Width (VRAM CBR Refresh, 25 MHz)	157		ns
66	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Burst Read , 25 MHz)	517		ns
67	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Burst Write, 25 MHz)	357		ns
68[8]	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Read , 33MHz)	147		ns
69	$\overline{\text{CAS}}$(3-0) Pulse Width (VRAM Read/Write, 33MHz)	57		ns
70	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Write, 33MHz)	87		ns
71	BCLK to DSF(3-0) Invalid (VRAM Block Write, 33 MHz)	4		ns
72	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Read Transfer, 33MHz)	117		ns
73	$\overline{\text{CAS}}$(3-0) Pulse Width (VRAM Read Transfer, 33MHz)	57		ns
74	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM CBR Refresh, 33MHz)	117		ns
75	$\overline{\text{CAS}}$(3-0) Pulse Width (VRAM CBR Refresh, 33MHz)	147		ns
76	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Burst Read, 33MHz)	417		ns
77	$\overline{\text{RAS}}$(3-0) Pulse Width (VRAM Burst Write, 33MHz)	357		ns

NOTE: 8. 33 MHz cycle timings are for 100 ns VRAM and have all optional wait states active.

TABLE 9. VIDEO SIGNAL AC TIMING SPECIFICATIONS (See Figures 35-36)

NUM	CHARACTERISTIC	MIN	MAX	UNIT
78[9]	PIXCLK to $\overline{\text{CBLANK}}$ Valid		17	ns
79	PIXCLK to $\overline{\text{CBLANK}}$ Inalid		13	ns
80	PIXCLK to $\overline{\text{HSYNC}}$ Valid		17	ns
81	PIXCLK to $\overline{\text{HSYNC}}$ Invalid		14	ns
82	PIXCLK to $\overline{\text{VSYNC}}$ Valid		20	ns
83	PIXCLK to $\overline{\text{VSYNC}}$ Invalid		17	ns
84	PIXCLK to $\overline{\text{CSYNC}}$, $\overline{\text{SCSYNC}}$ Valid		17	ns
85	PIXCLK to $\overline{\text{CSYNC}}$, $\overline{\text{SCSYNC}}$ Invalid		14	ns
86	PIXCLK to SBANK Valid		13	ns
87	PIXCLK to SBANK Invalid		11	ns
88	PIXCLK to $\overline{\text{SOE(3-0)}}$ Valid		16	ns
89	PIXCLK to $\overline{\text{SOE(3-0)}}$ Invalid		13	ns
90	PIXCLK to $\overline{\text{VBLIRQ}}$ Valid		25	ns
91	PIXCLK to $\overline{\text{VBLIRQ}}$ Invalid		22	ns
92[10]	PIXCLK Rising Edge to LD Failling Edge		9	ns
93[10]	PIXCLK Falling Edge to LD Rising Edge		8	ns
94[9]	VIDCLK to $\overline{\text{CBLANK}}$ Valid		18	ns
95	VIDCLK to $\overline{\text{CBLANK}}$ Inalid		14	ns
96	VIDCLK to $\overline{\text{HSYNC}}$ Valid		17	ns
97	VIDCLK to $\overline{\text{HSYNC}}$ Invalid		13	ns
98	VIDCLK to $\overline{\text{VSYNC}}$ Valid		20	ns
99	VIDCLK to $\overline{\text{VSYNC}}$ Invalid		17	ns
100	VIDCLK to $\overline{\text{CSYNC}}$, $\overline{\text{SCSYNC}}$ Valid		17	ns
101	VIDCLK to $\overline{\text{CSYNC}}$, $\overline{\text{SCSYNC}}$ Invalid		14	ns
102	VIDCLK to SBANK Valid		16	ns
103	VIDCLK to SBANK Invalid		14	ns
104	VIDCLK to $\overline{\text{SOE(3-0)}}$ Valid		24	ns
105	VIDCLK to $\overline{\text{SOE(3-0)}}$ Invalid		21	ns
106	VIDCLK to $\overline{\text{VBLIRQ}}$ Valid		25	ns
107	VIDCLK to $\overline{\text{VBLIRQ}}$ Invalid		22	ns
108[11]	VIDCLK Rising Edge to LD Rising Edge (LD = VIDCLK divided by 1)		8	ns
109[11]	VIDCLK Falling Edge to LD Falling Edge (LD = VIDCLK divided by 1)		10	ns
110[11]	VIDCLK to LD Rising Edge (LD = VIDCLK divided by N, N = 2-255)		10	ns
111[11]	VIDCLK to LD Falling Edge (LD = VIDCLK divided by N, N = 2-255)		12	ns
112[12]	LD Pulse Width Low (LD = VIDCLK divided by N, N = 2-255)		1	Clk
113[12]	LD Pulse Width High (LD = VIDCLK divided by N, N = 2-255)		N-1	Clks

NOTES: 9. Either PIXCLK or VIDCLK is used to generate video timing, but not both at one time. DAFB II video signal timing depends on which clock is active.

10. When LD is derived from PIXCLK, it is inverted with respect to PIXCLK.

11. When LD is derived from VIDCLK, it is divided down by a programmable divisor.

12. The duty cycle of LD is not 50/50 when it is generated by VIDCLK divided by greater than 1. In this case, LD is low for one VIDCLK cycle and is high for the remainder of its period.

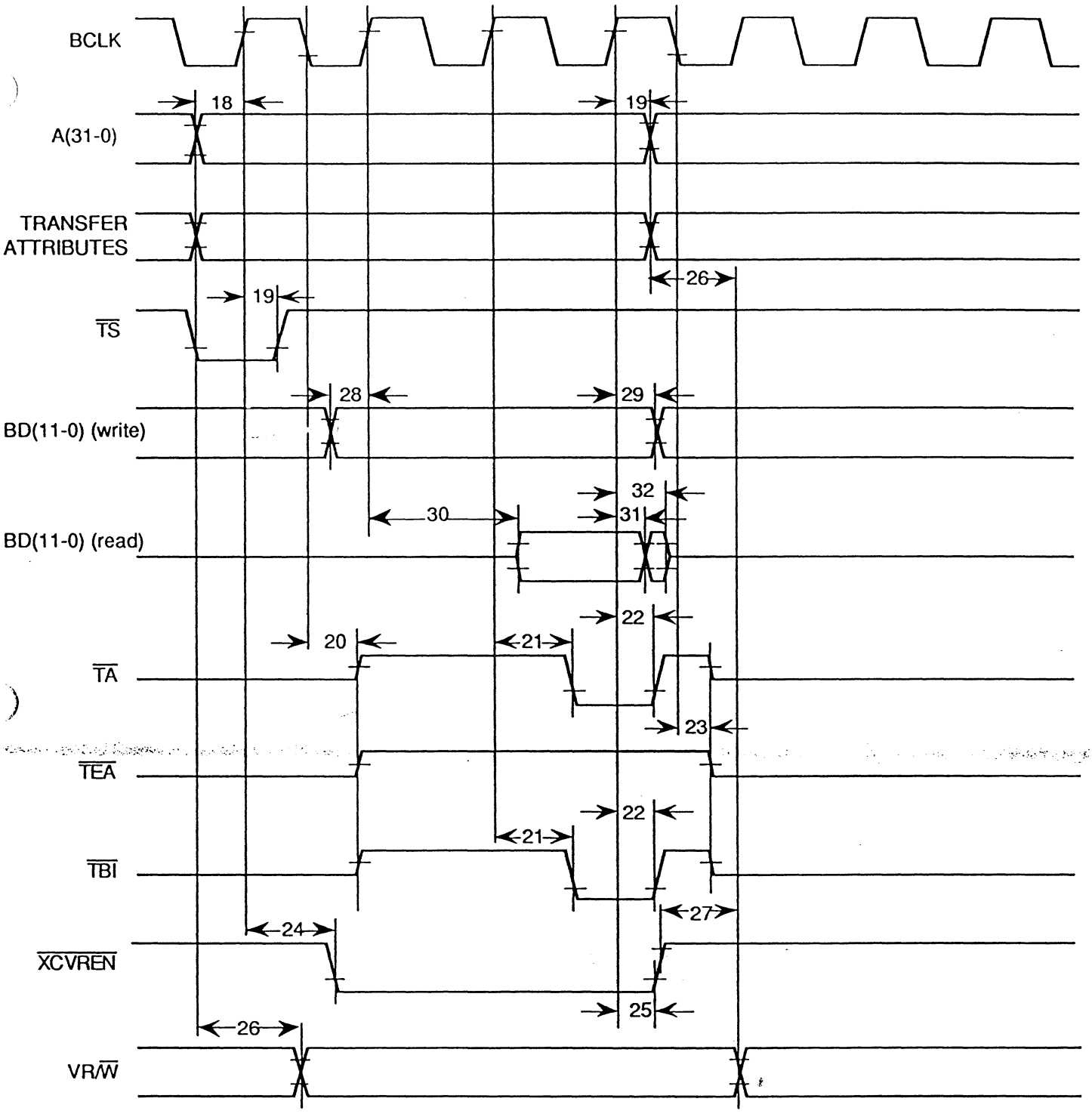
TABLE 10. OTHER SIGNAL AC TIMING SPECIFICATIONS (See Figures 37-38)

NUM	CHARACTERISTIC	MIN	MAX	UNIT
114	BCLK to PIXSEL(1-0) Valid		30	ns
115	BCLK to SENSE(2-0) Low Impedance		27	ns
116	BCLK to SENSE(2-0) High Impedance		20	ns
117	$\overline{\text{VTESTEN}}$ to DAFB II Outputs High Impedance		16	ns
118	$\overline{\text{VTESTEN}}$ to DAFB II Outputs Valid		25	ns
119[13]	$\overline{\text{RESET}}$ Low Time	5		Clks
129	SYNCACTIVE to $\overline{\text{SCSYNC}}$ Enable/Disable		17	ns

NOTE: 13. $\overline{\text{RESET}}$ low time is based on synchronizing it to BCLK and clearing DAFB II's internal state.

TABLE 11. SCSI SIGNAL AC TIMING SPECIFICATIONS (See Figures 39-45)

NUM	CHARACTERISTIC	MIN	MAX	UNIT
120	BCLK rising edge to $\overline{\text{CS(1-0)}}$, $\overline{\text{RD}}$ Low		23	ns
121	BCLK rising edge to $\overline{\text{CS(1-0)}}$, $\overline{\text{RD}}$ High		17	ns
122	BCLK rising edge to $\overline{\text{WR}}$ Low		23	ns
123	BCLK rising edge to $\overline{\text{WR}}$ High		17	ns
124	BCLK falling edge to $\overline{\text{WR}}$ High		18	ns
125	DREQ Valid to BCLK falling edge (to be seen in that cycle)	2		ns
126	BCLK rising edge to $\overline{\text{DACK(1-0)}}$ Low		21	ns
127	BCLK rising edge to $\overline{\text{DACK(1-0)}}$ High		21	ns
128	$\overline{\text{RESET}}$ Change to RESETOUT Change		17	ns



NOTE: 14. Transfer Attribute Signals are SIZE(1-0), TT1, and R/$\overline{W}$ for the following applicable waveforms.

FIGURE 6. DAFB II REGISTER READ/WRITE TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 18 OF 98

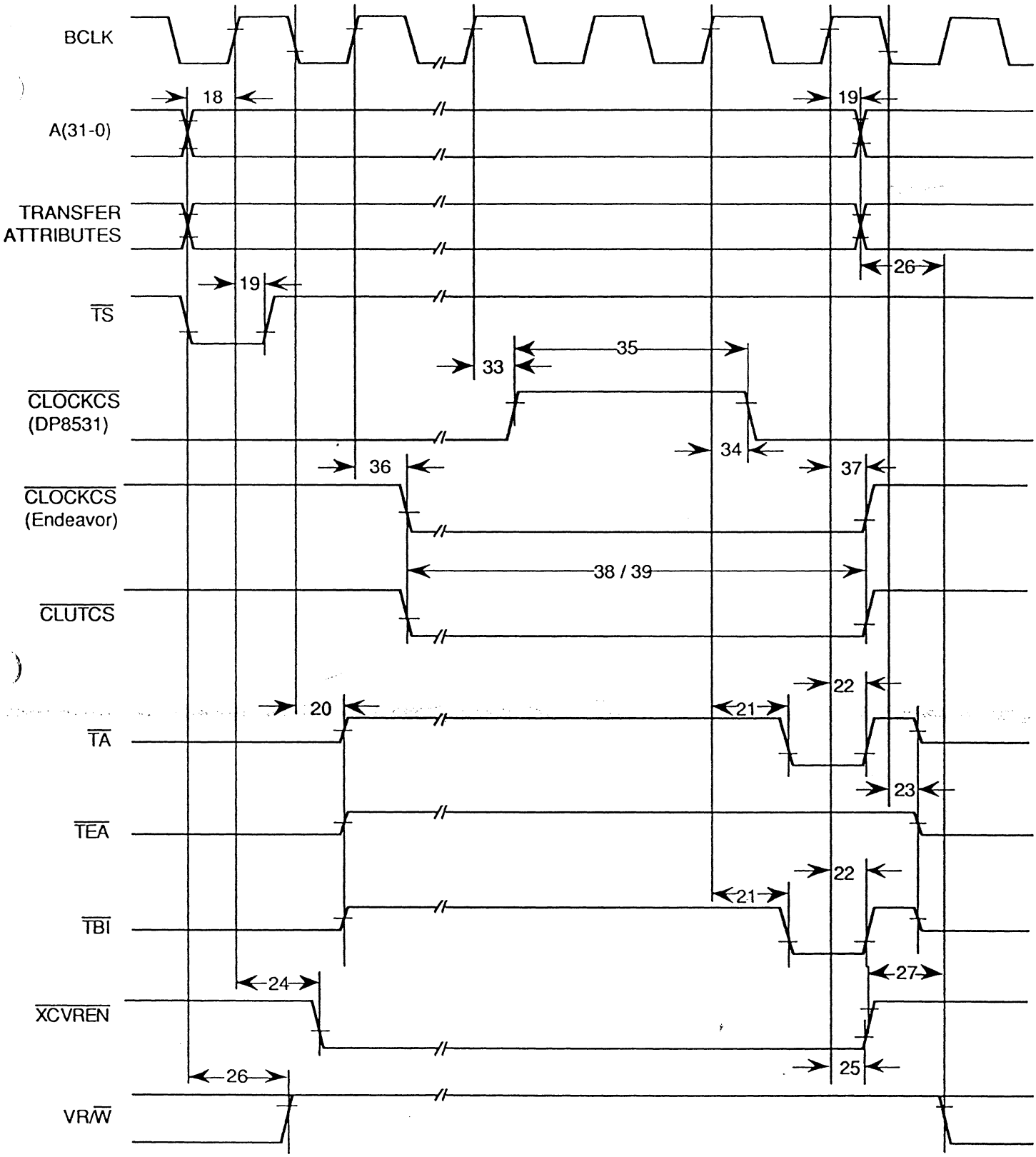


FIGURE 7. 25/33 MHz CHIP SELECTS (READ) TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 19 OF 98

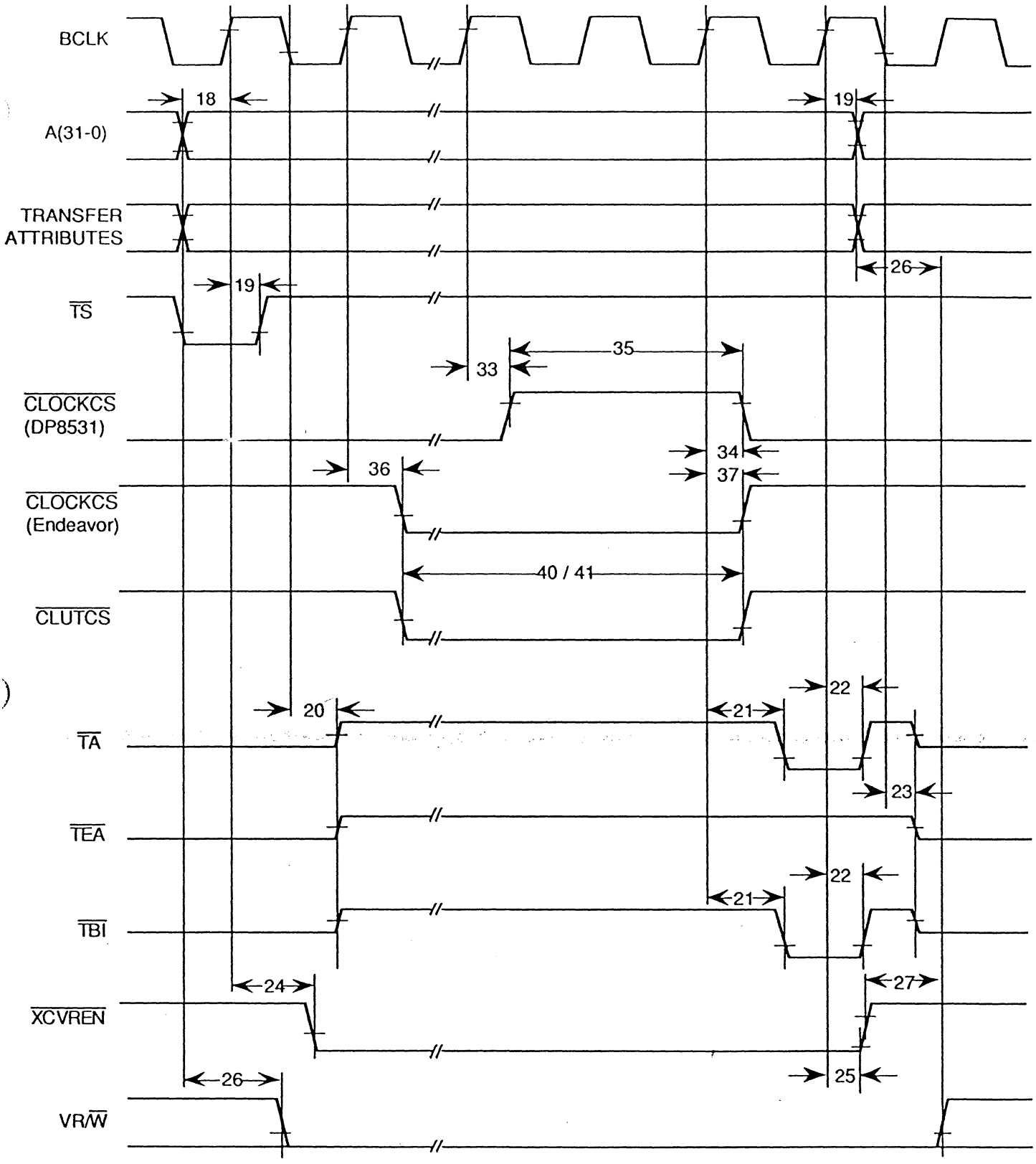


FIGURE 8. 25/33 MHz CHIP SELECTS (WRITE) TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 20 OF 98

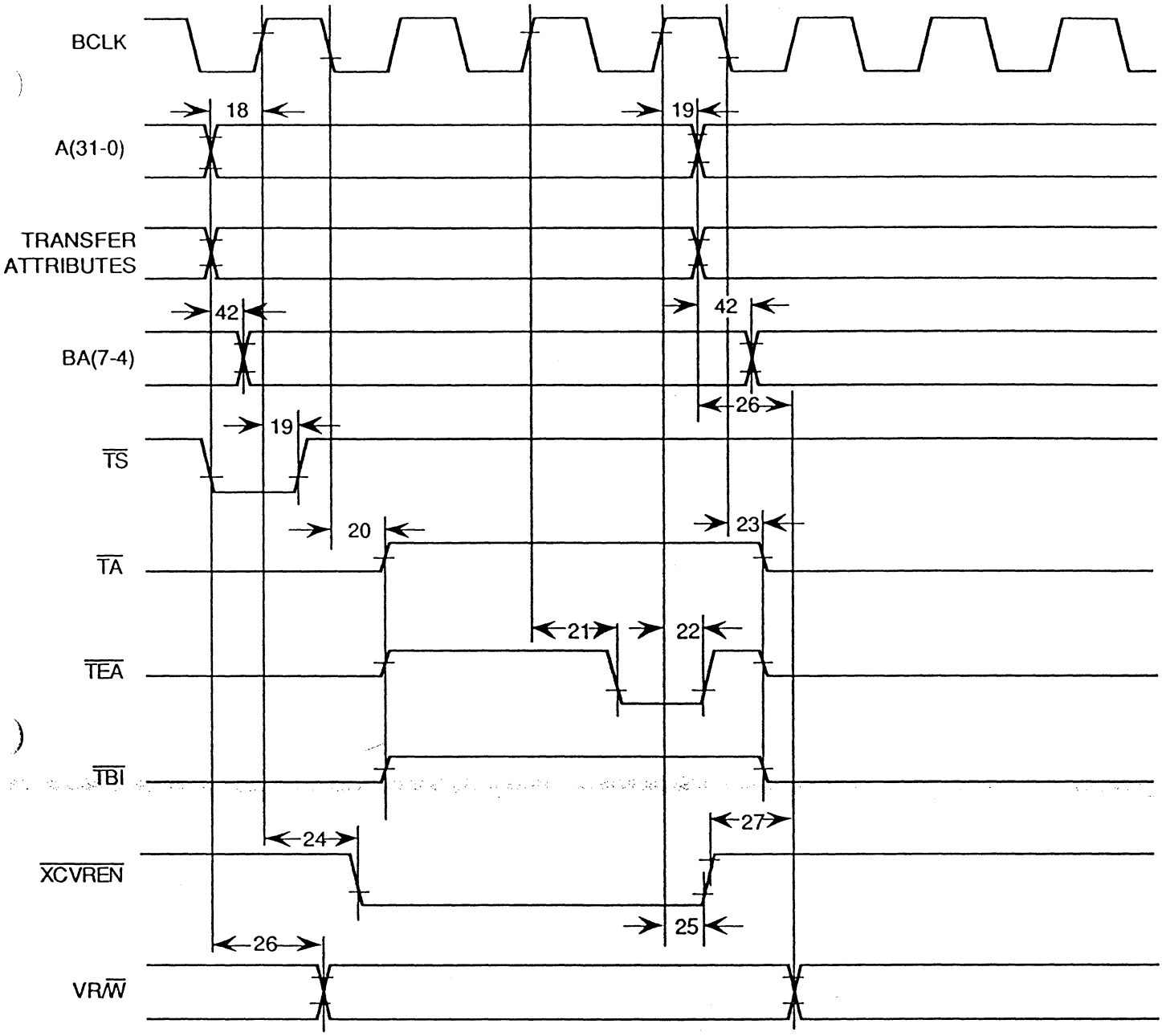


FIGURE 9. ILLEGAL MEMORY ACCESS TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 21 OF 98

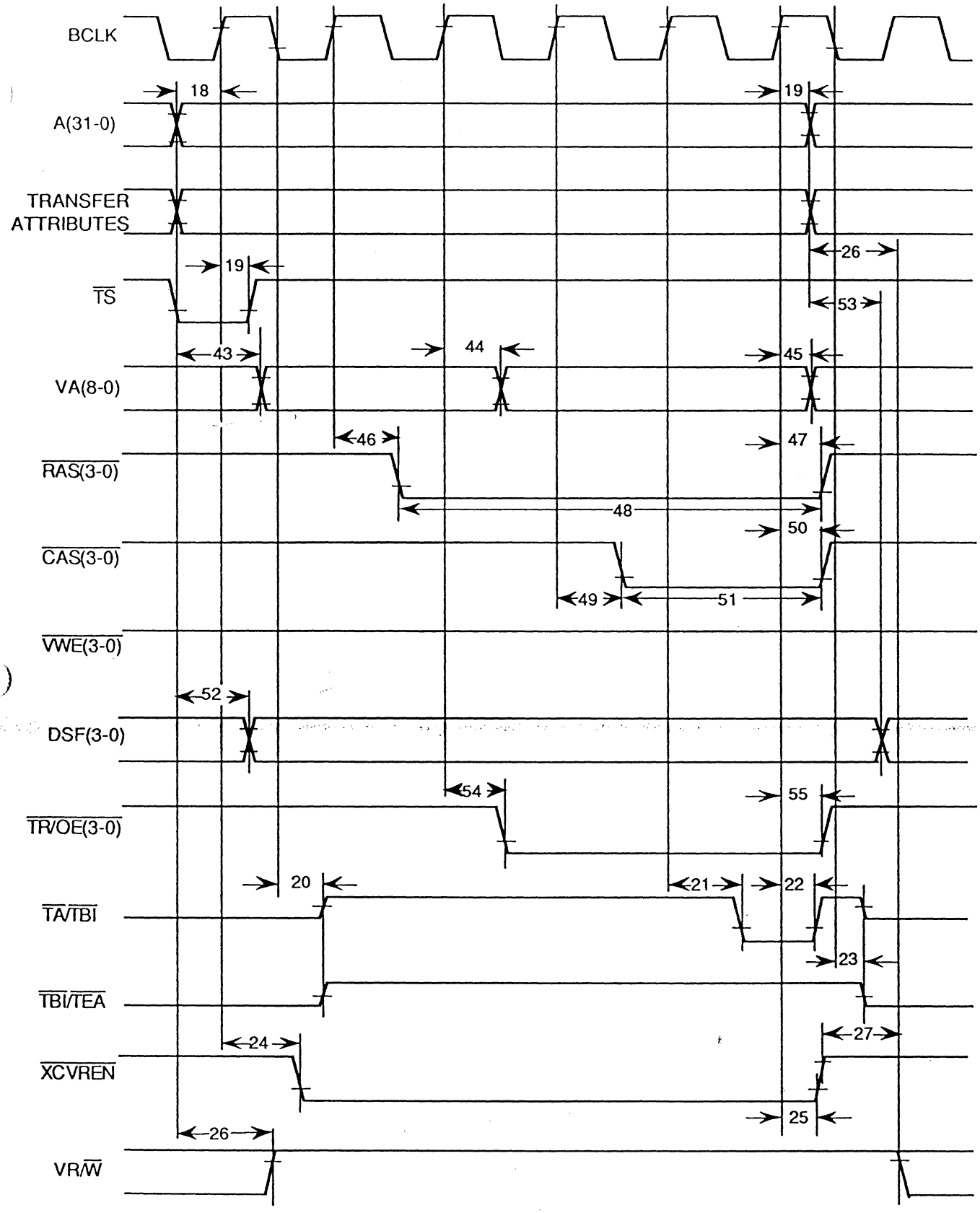


FIGURE 10. 25 MHz VRAM READ TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 22 OF 98

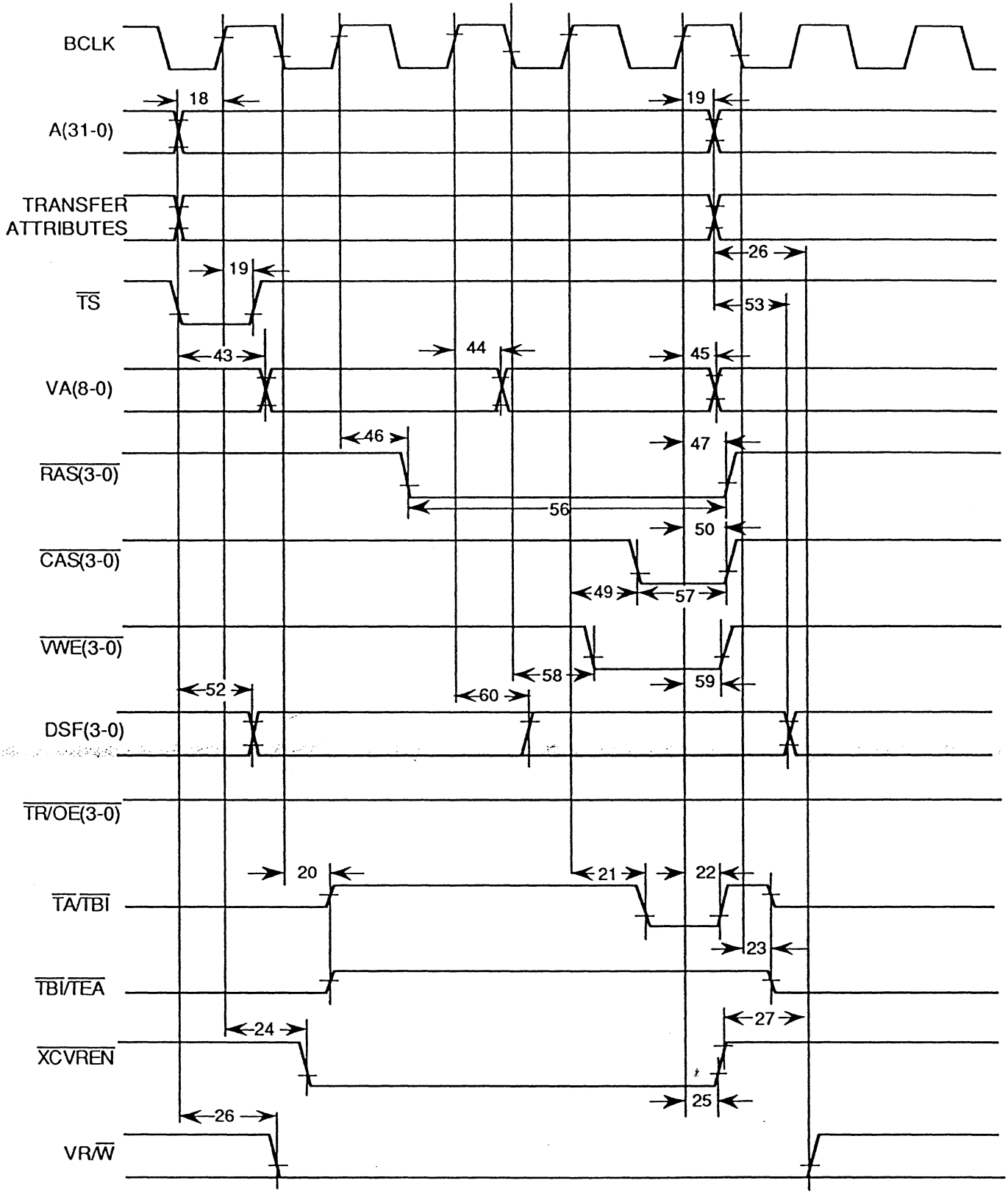


FIGURE 11. 25 MHz VRAM WRITE TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 23 OF 98

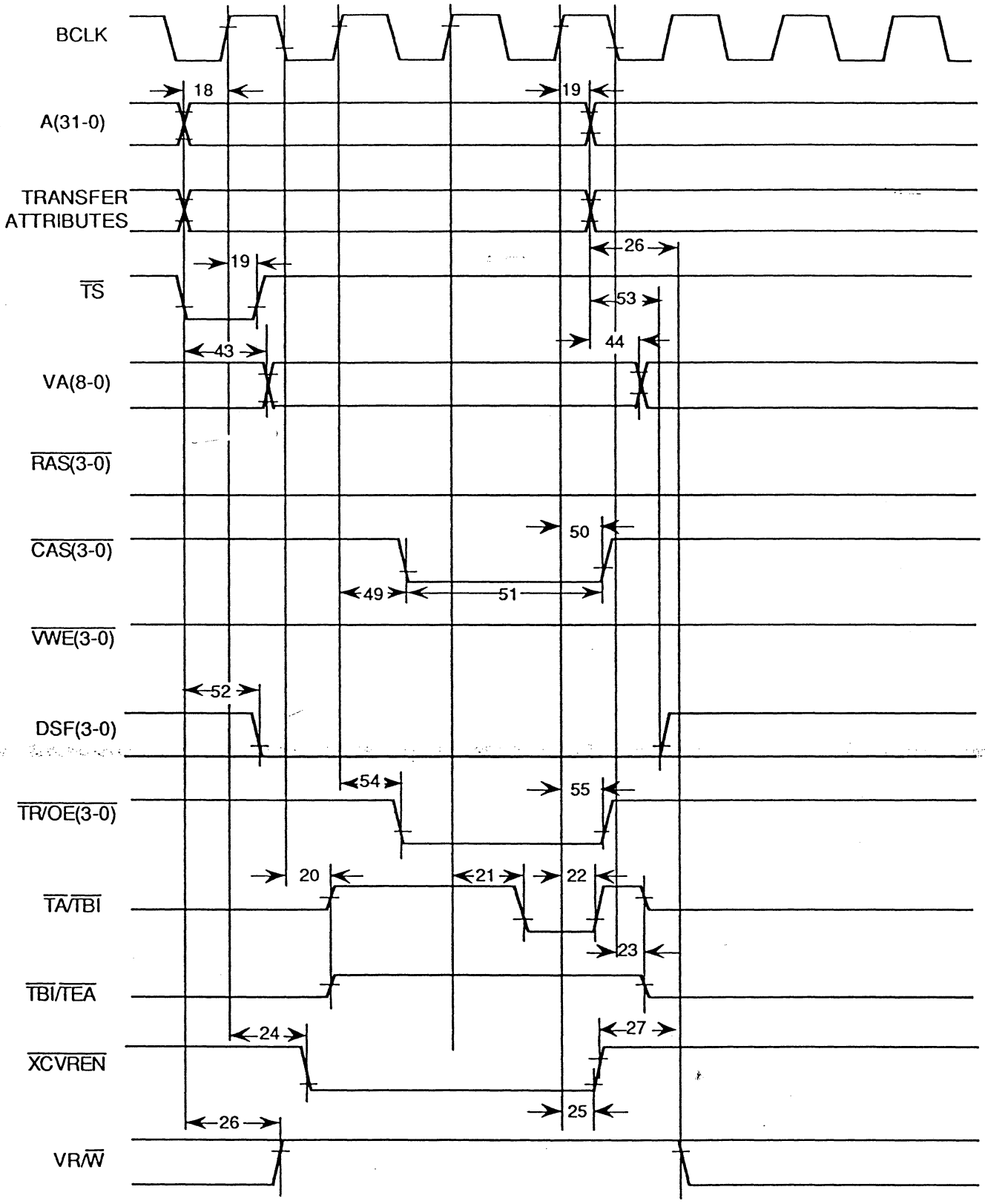


FIGURE 12. 25 MHz VRAM PAGE MODE READ TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 24 OF 98

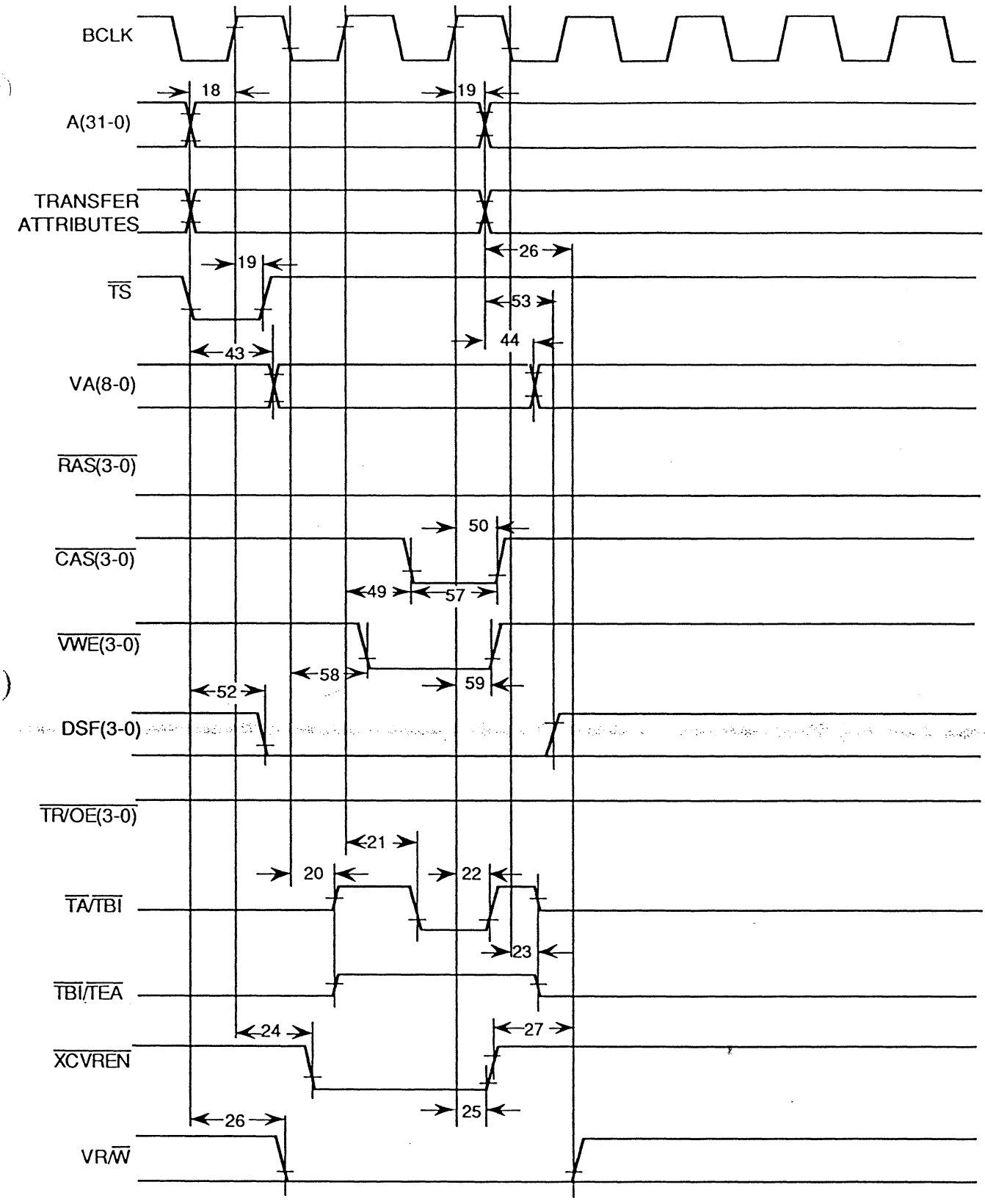


FIGURE 13. 25 MHz VRAM PAGE MODE WRITE TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 25 OF 98

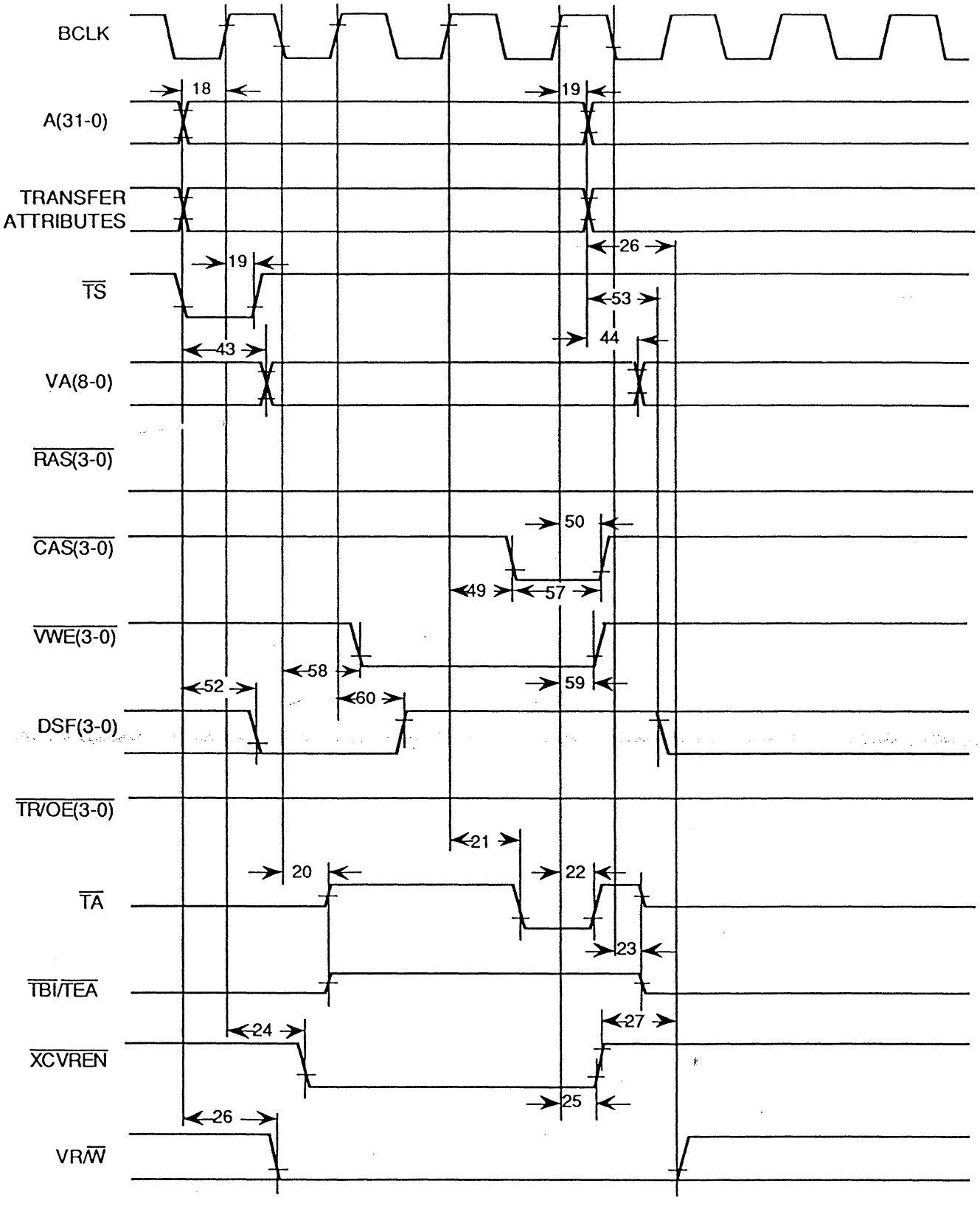


FIGURE 14. 25 MHz VRAM PAGE MODE BLOCK WRITE TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 26 OF 98

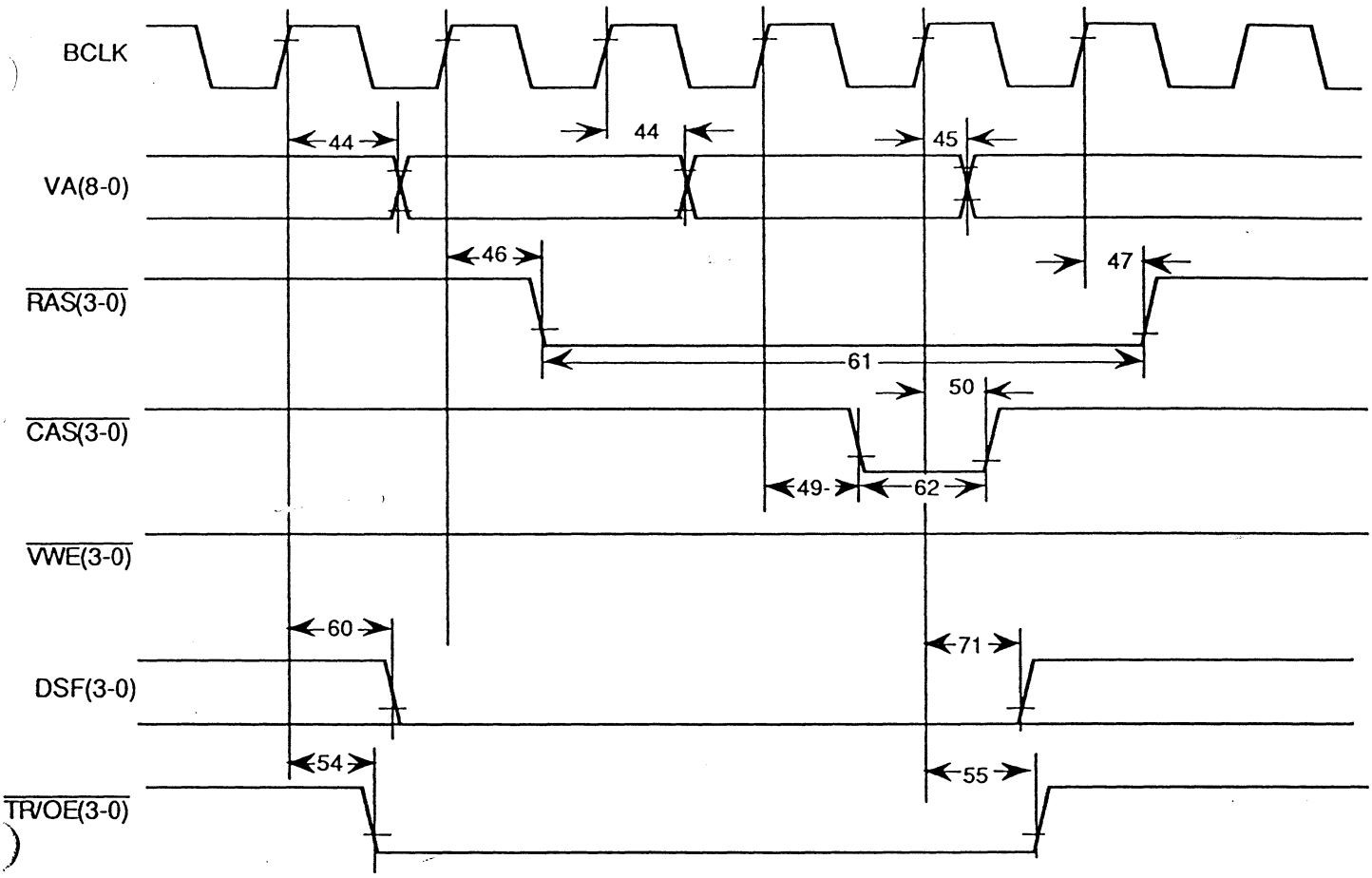


FIGURE 15. 25 MHz VRAM FULL READ TRANSFER TIMING

Apple Computer, Inc.

SIZE A | DRAWING NUMBER 343S0128-A | SCALE: NONE | SHT 27 OF 98

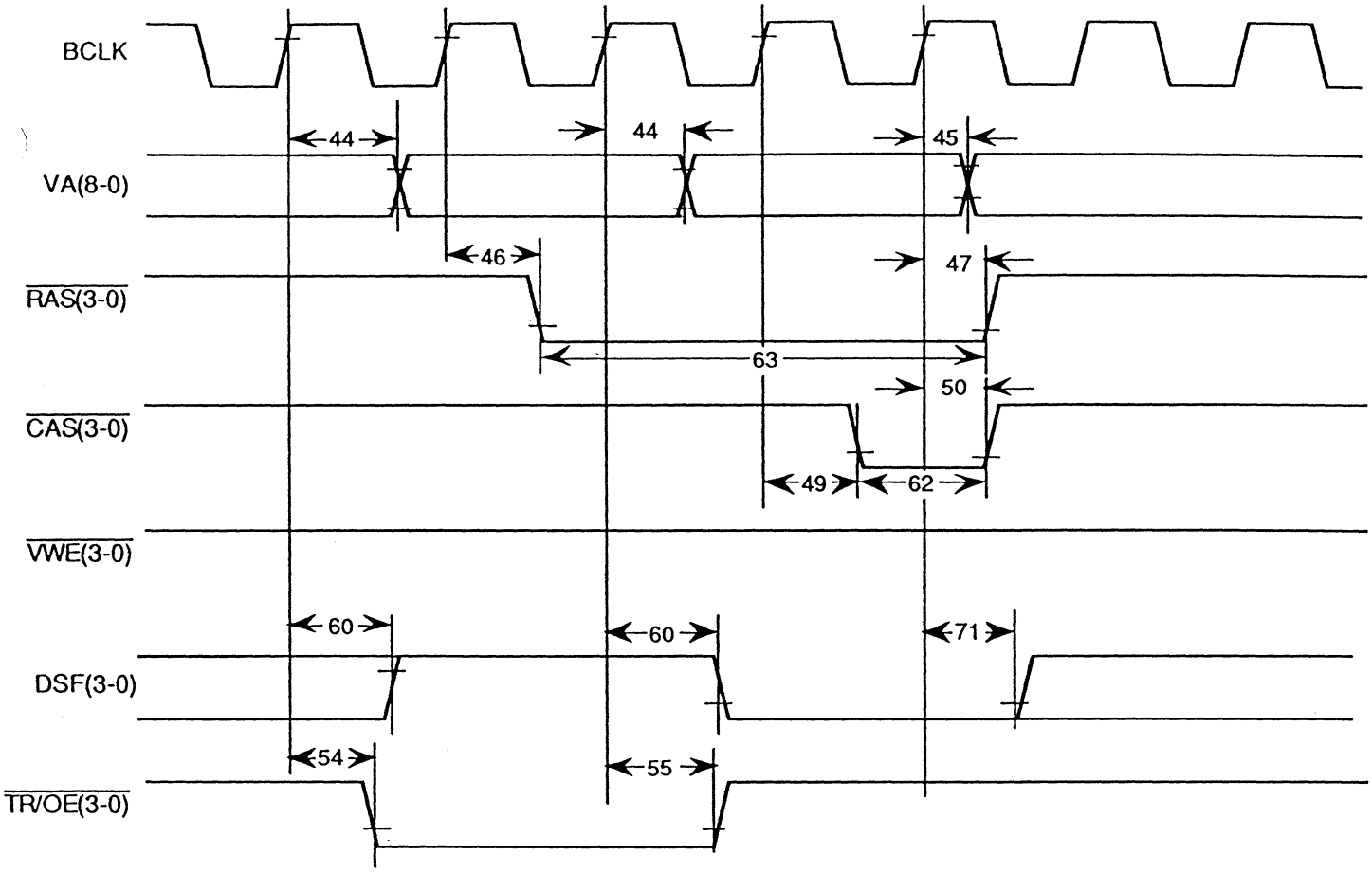


FIGURE 16. 25 MHz VRAM SPLIT READ TRANSFER TIMING

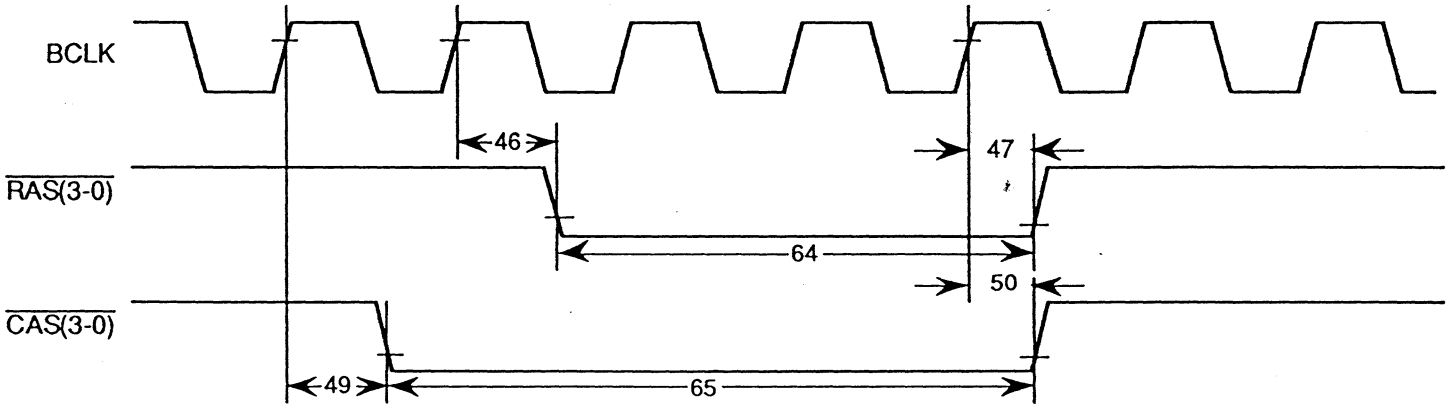


FIGURE 17. 25 MHz VRAM CBR REFRESH TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 28 OF 98

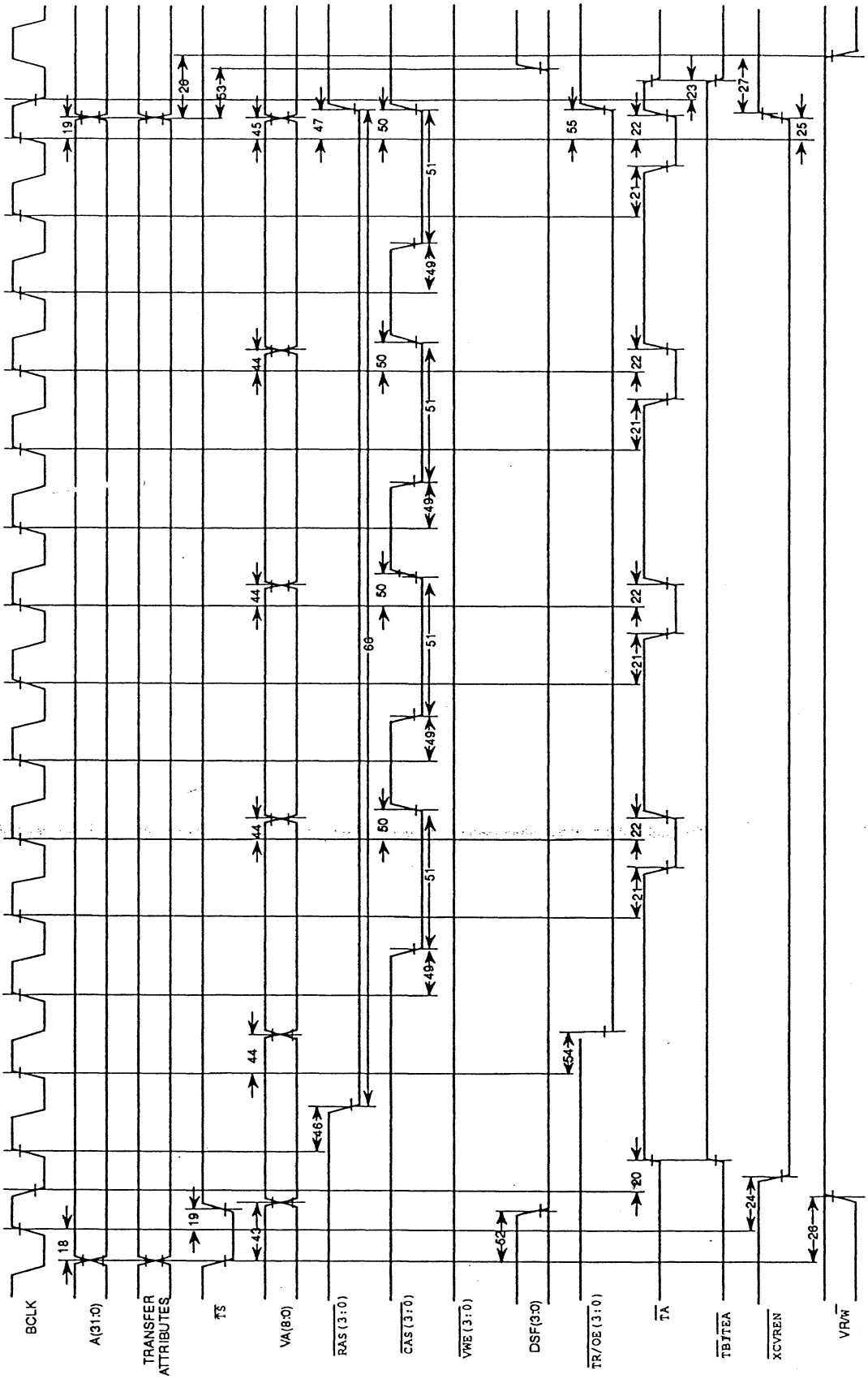


FIGURE 18. 25 MHz VRAM BURST READ TIMING

Apple Computer, Inc.

SIZE A | DRAWING NUMBER 343S0128-A | SCALE: NONE | SHT 29 OF 98

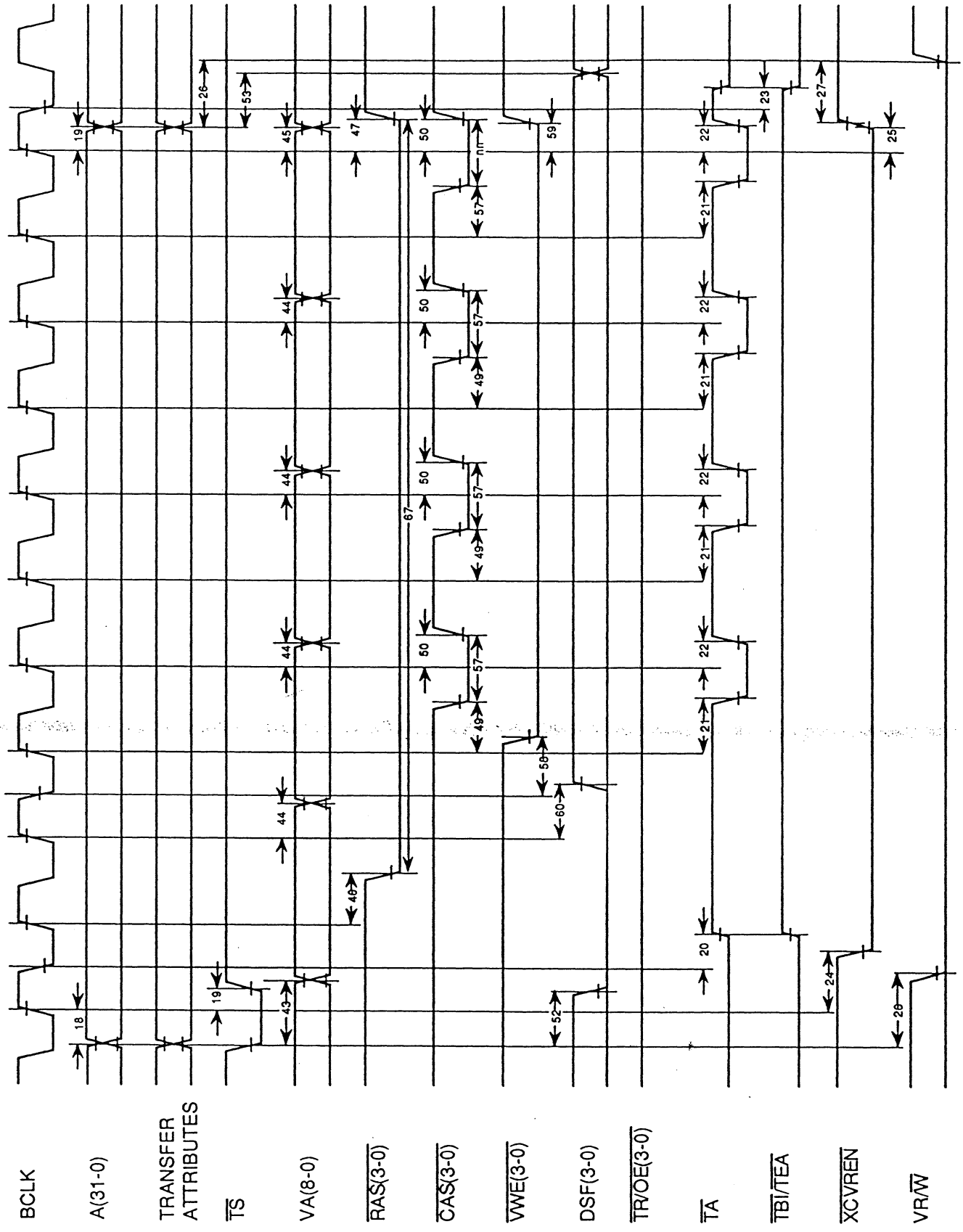


FIGURE 19. 25 MHz VRAM BURST WRITE TIMING

Apple Computer, Inc.

SIZE A | DRAWING NUMBER 343S0128-A | SCALE: NONE | SHT 30 OF 98

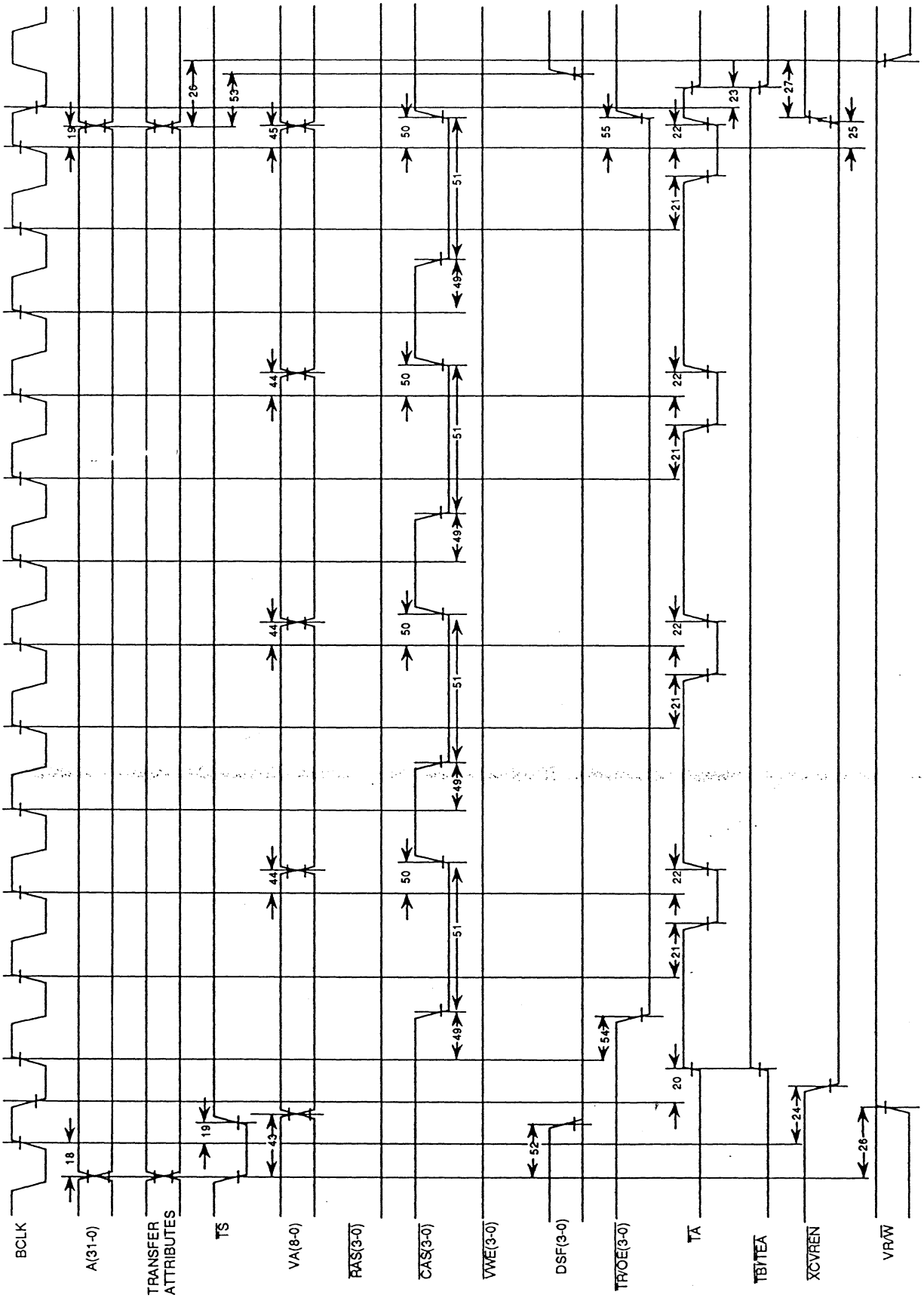


FIGURE 20. 25 MHz VRAM PAGE MODE BURST READ TIMING

Apple Computer, Inc.

SIZE A | DRAWING NUMBER 343S0128-A | SCALE: NONE | SHT 31 OF 98

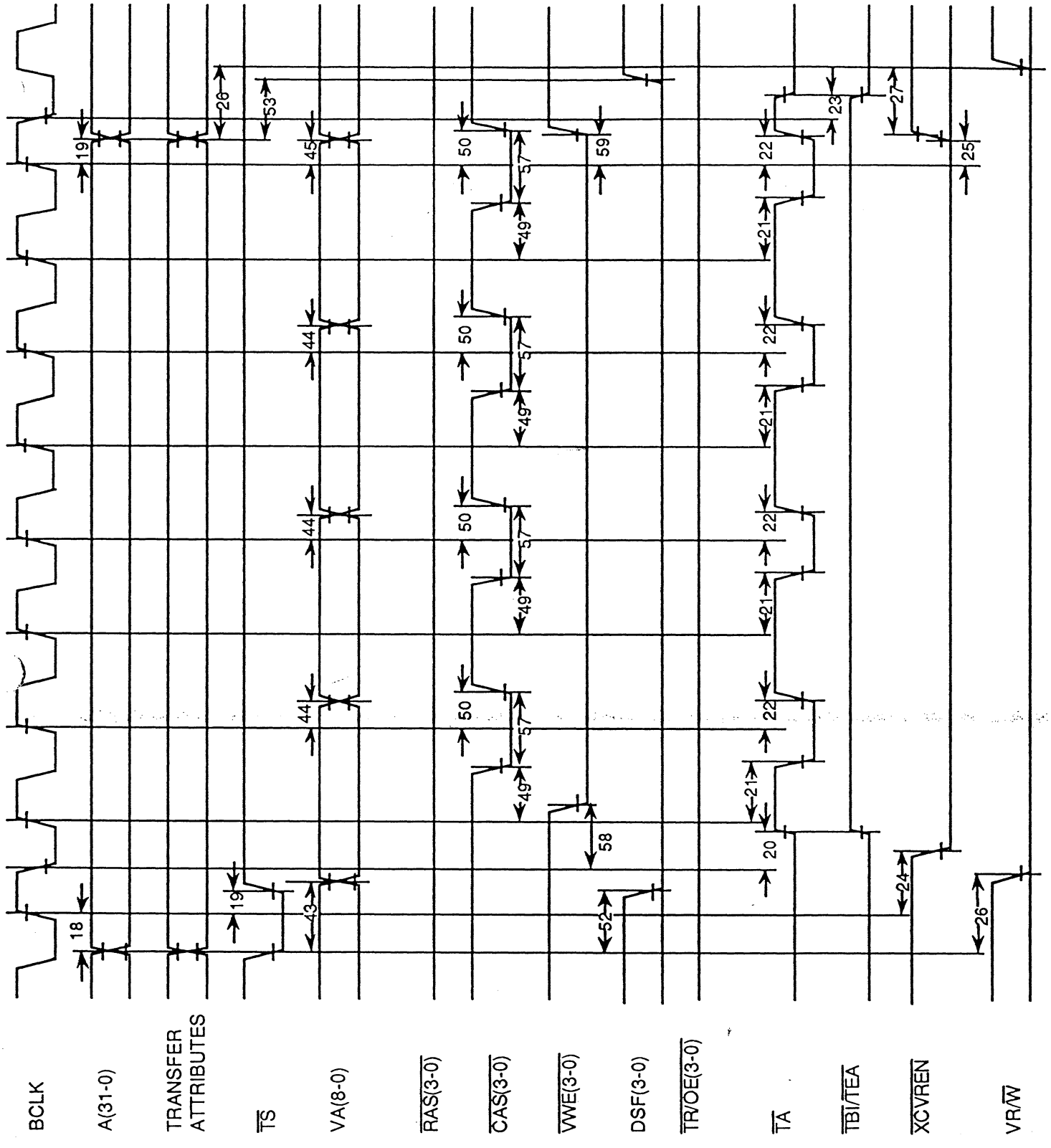


FIGURE 21. 25 MHz VRAM PAGE MODE BURST WRITE TIMING

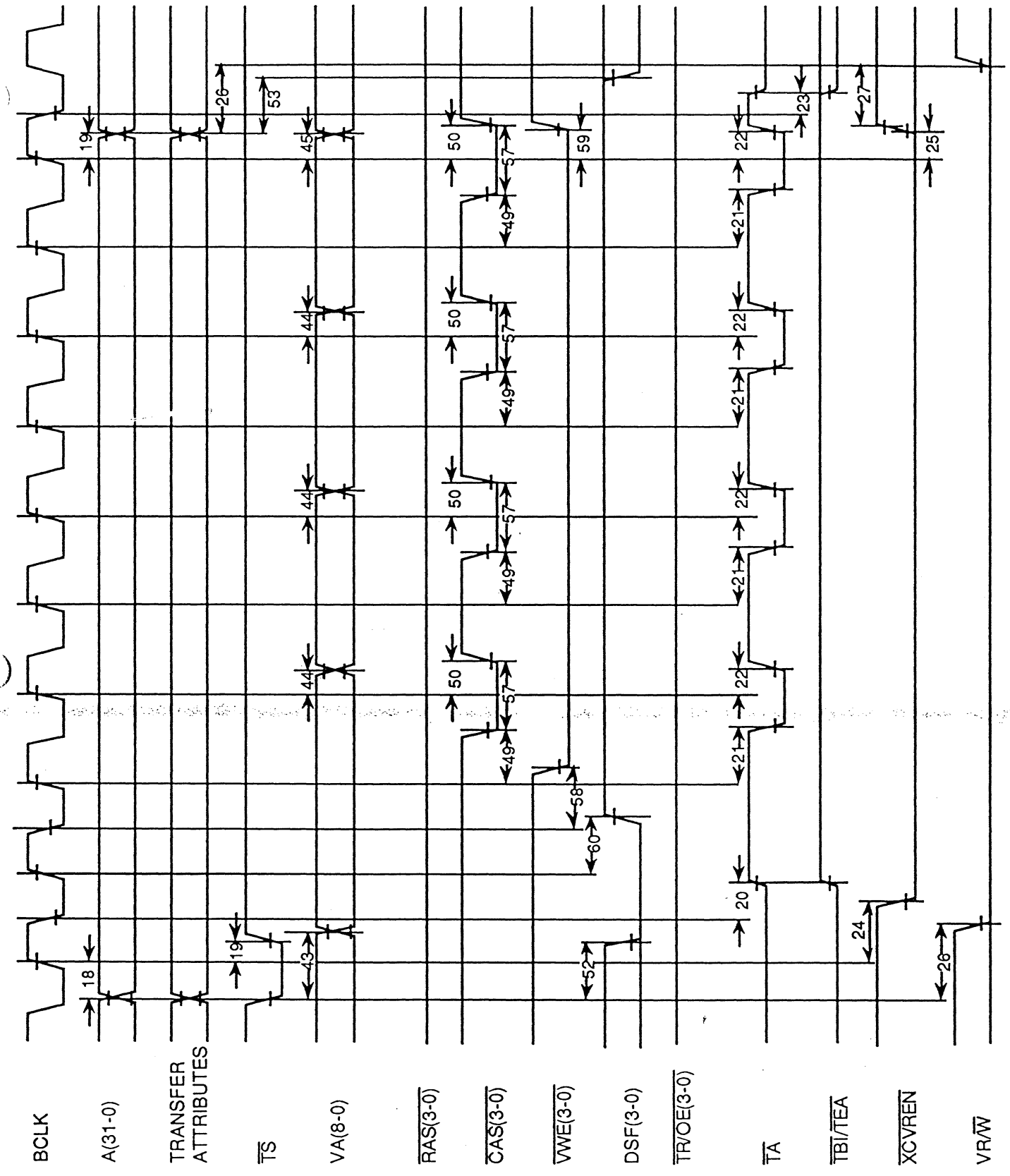


FIGURE 22. 25 MHz VRAM PAGE MODE BURST BLOCK WRITE TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 33 OF 98

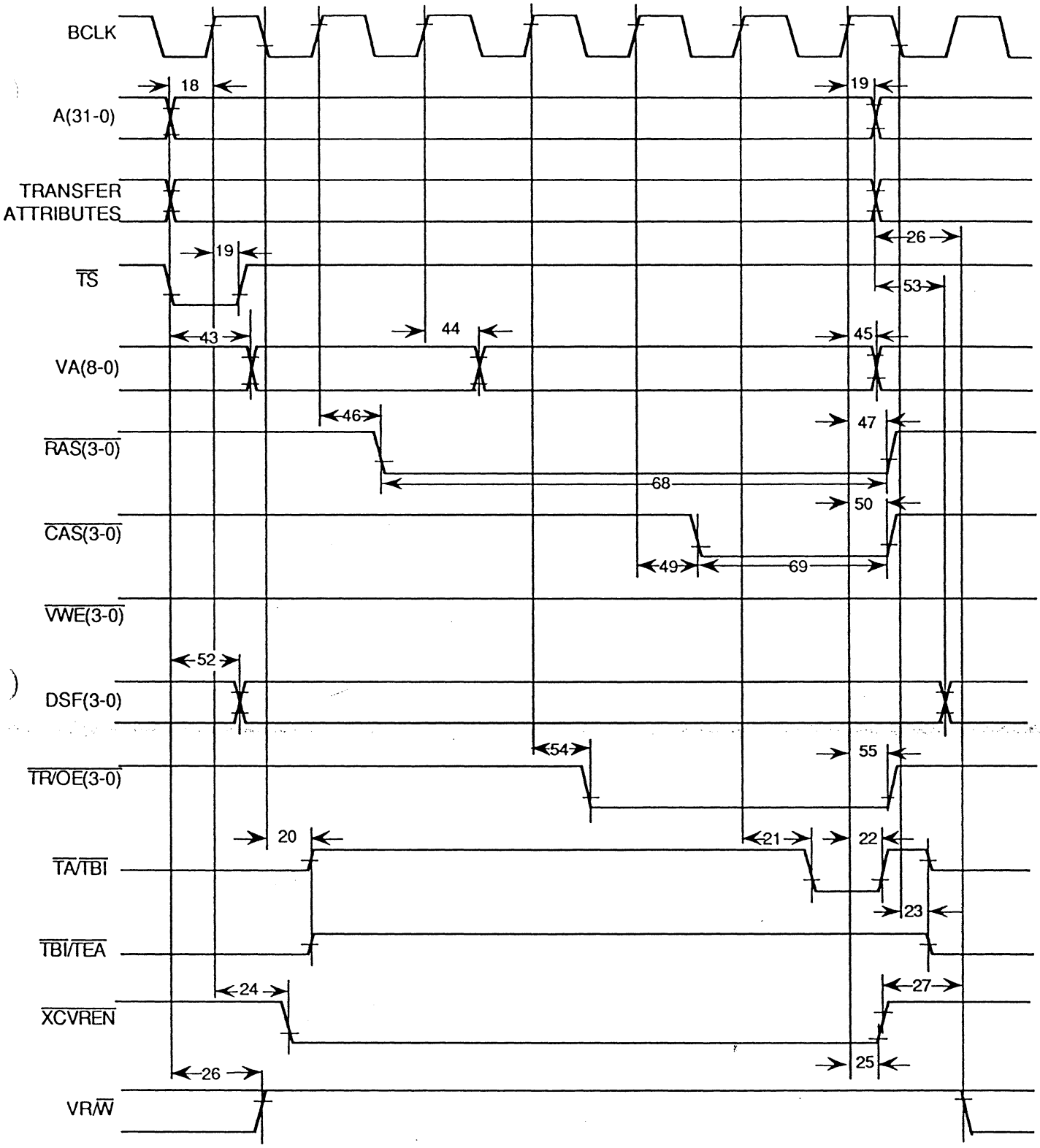


FIGURE 23. 33MHz VRAM READ TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 34 OF 98

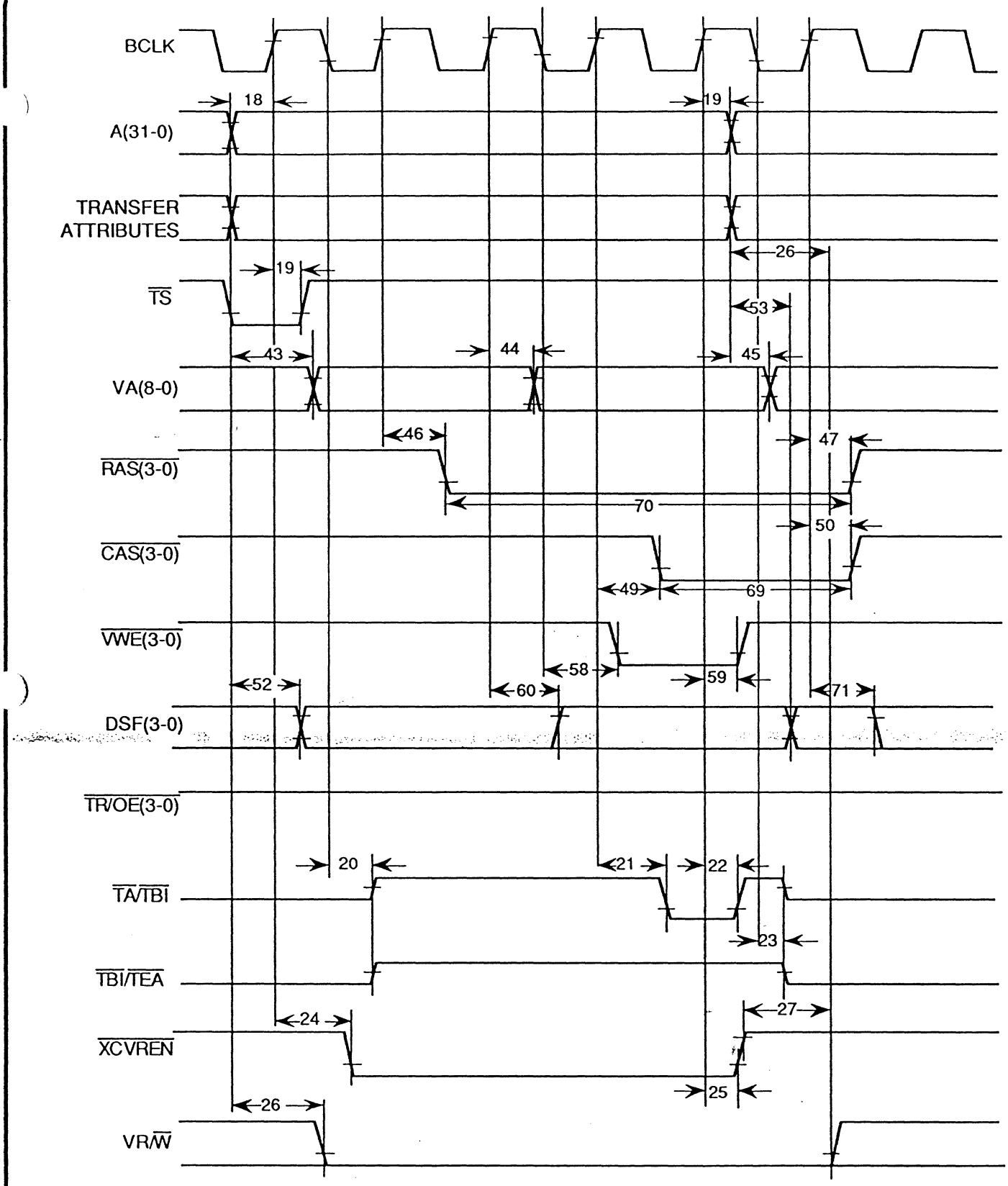


FIGURE 24. 33MHz VRAM WRITE TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 35 OF 98

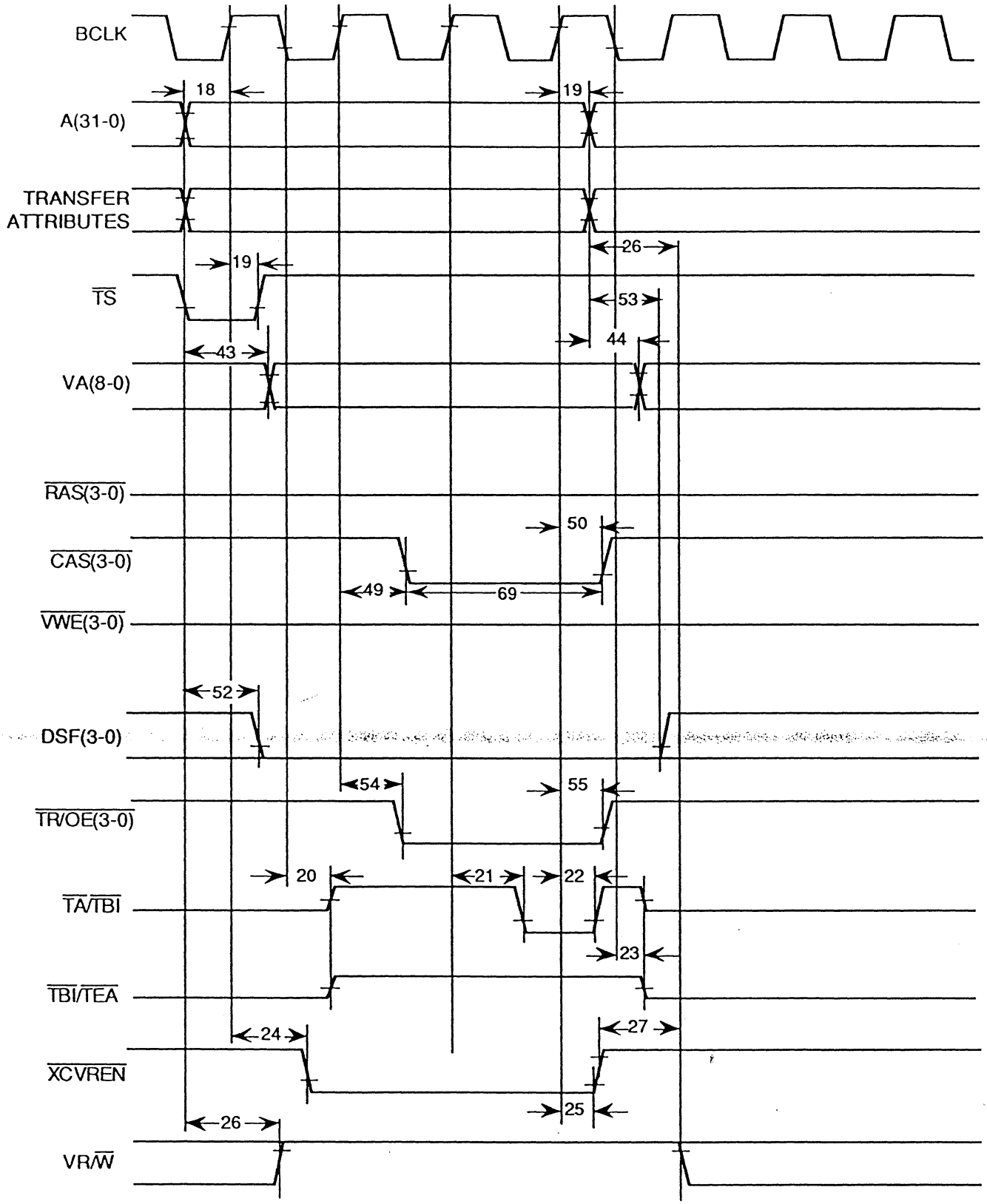


FIGURE 25. 33MHz VRAM PAGE MODE READ TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 36 OF 98

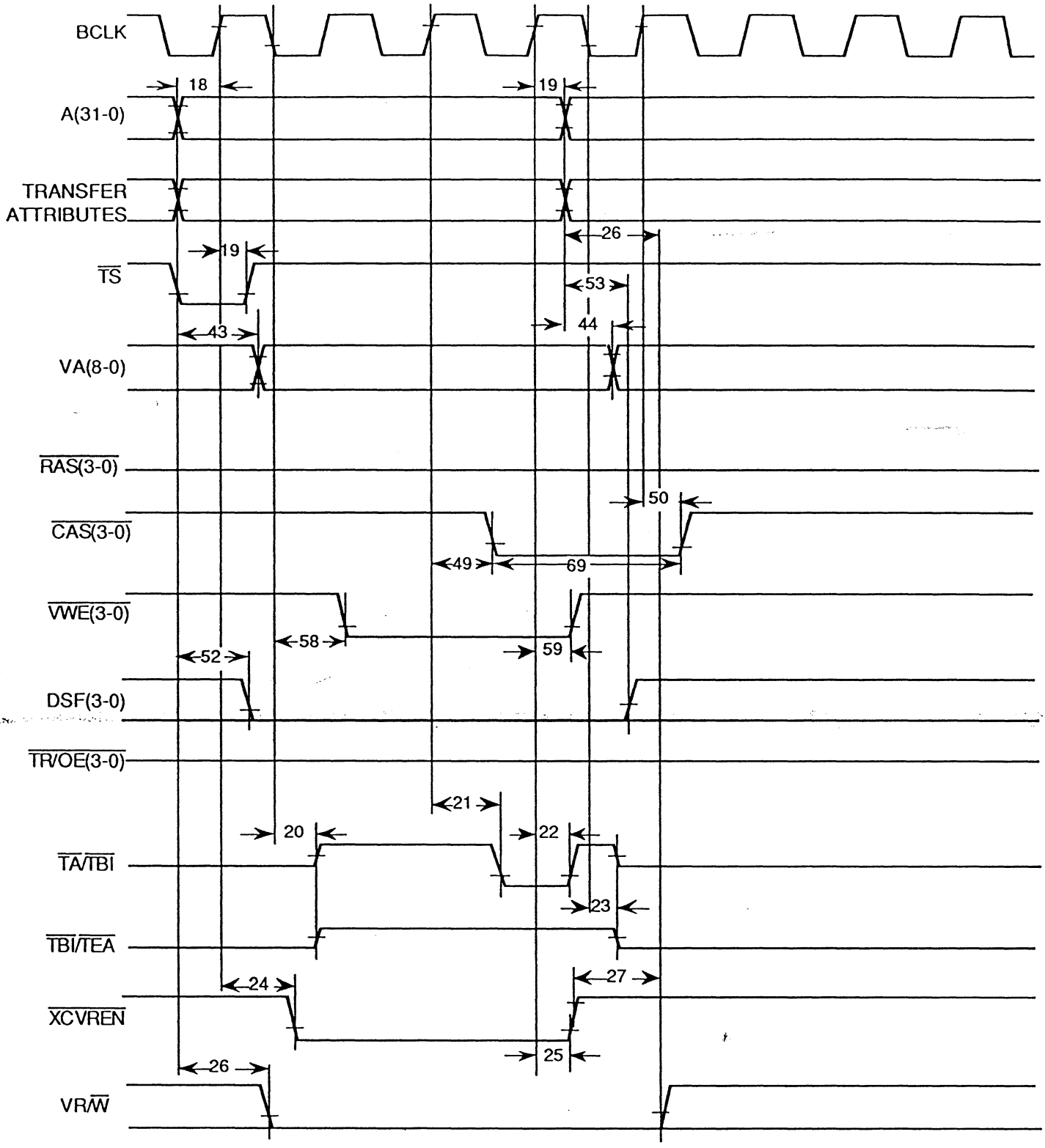


FIGURE 26. 33MHz VRAM PAGE MODE WRITE TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 37 OF 98

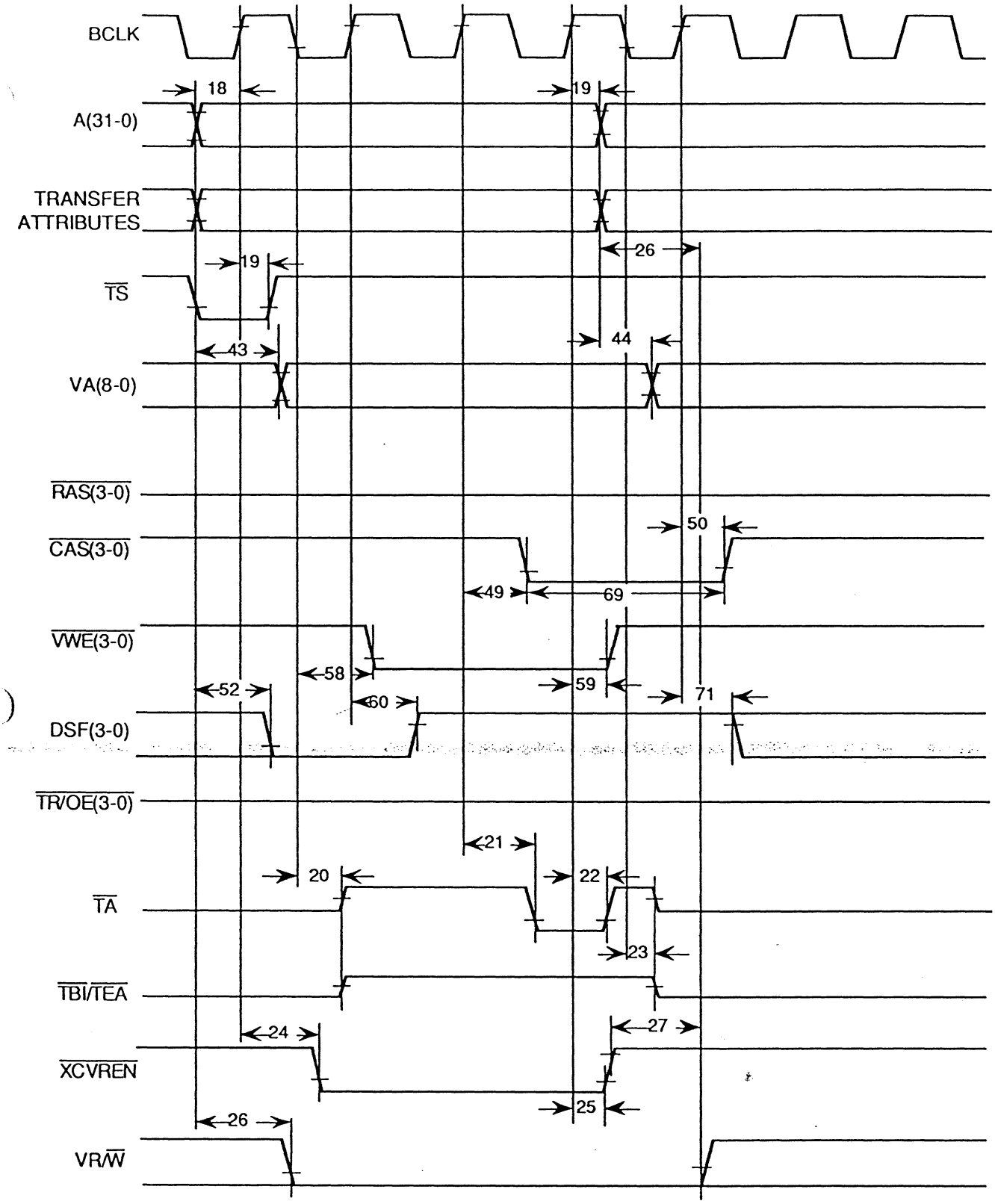


FIGURE 27. 33MHz VRAM PAGE MODE BLOCK WRITE TIMING

Apple Computer, Inc.

SIZE A | DRAWING NUMBER 343S0128-A | SCALE: NONE | SHT 38 OF 98

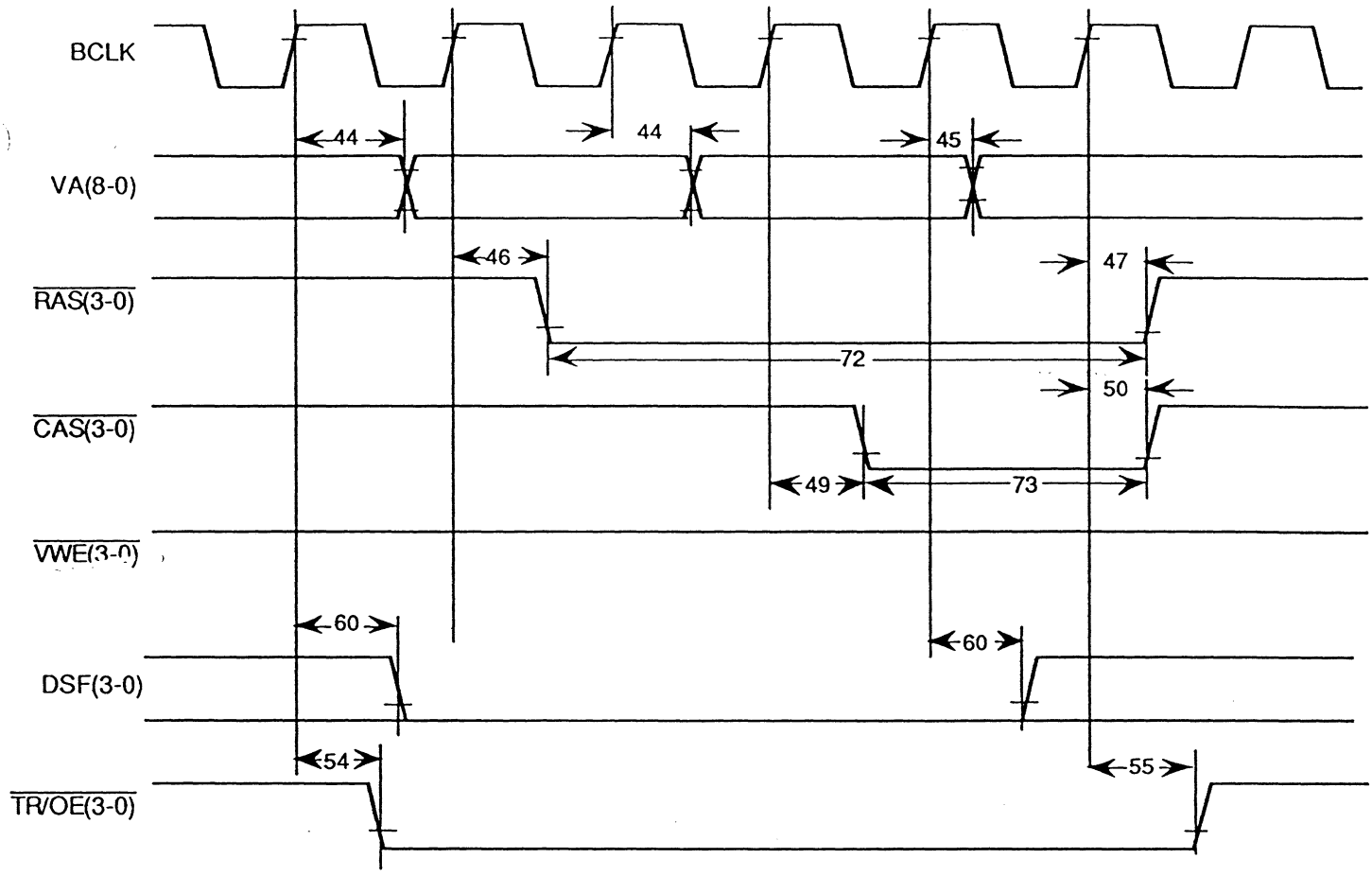


FIGURE 28. 33MHz VRAM FULL READ TRANSFER TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 39 OF 98

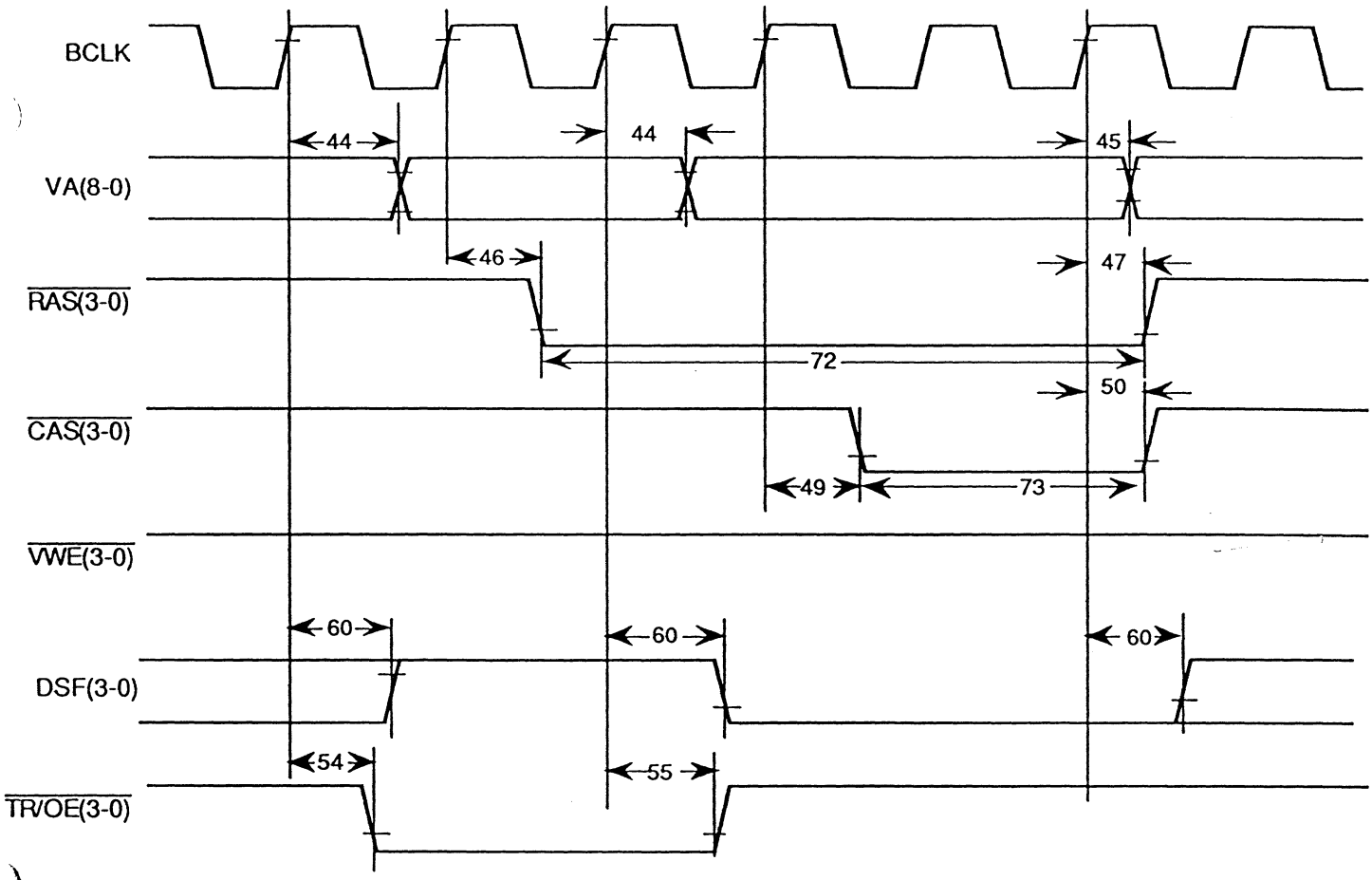


FIGURE 29. 33MHz VRAM SPLIT READ TRANSFER TIMING

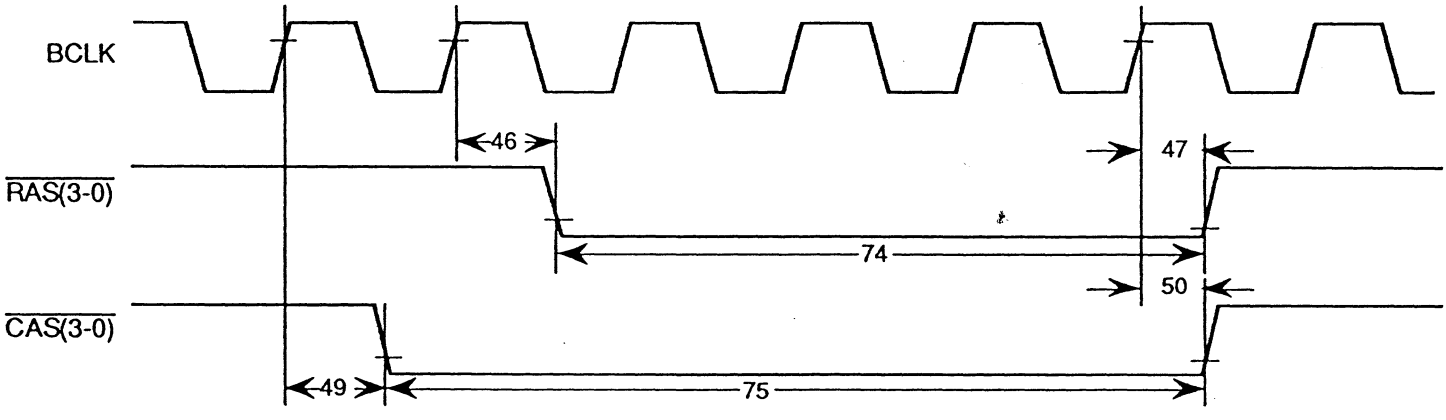


FIGURE 30. 33MHz VRAM CBR REFRESH TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 40 OF 98

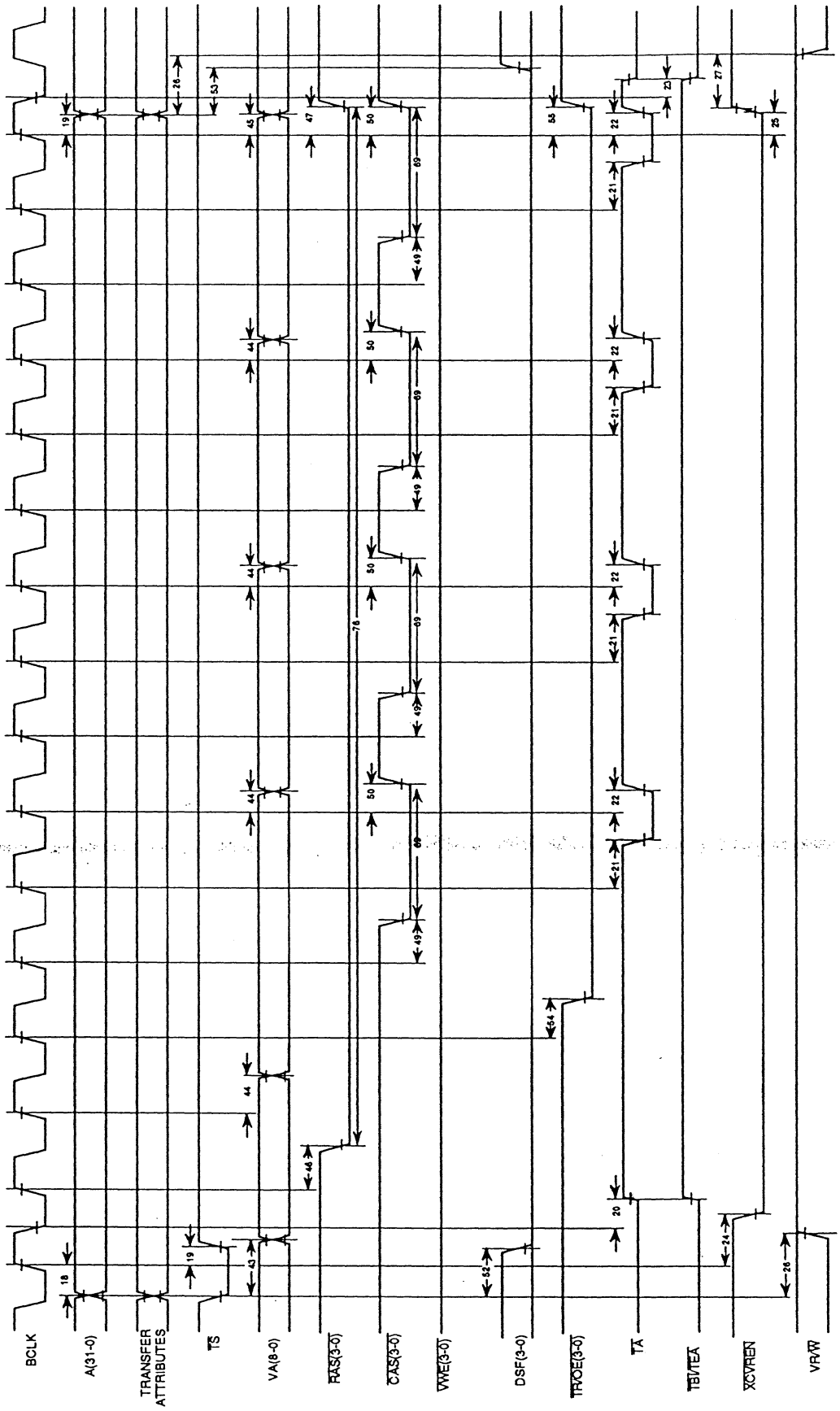


FIGURE 31. 33MHz VRAM BURST READ TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 41 OF 98

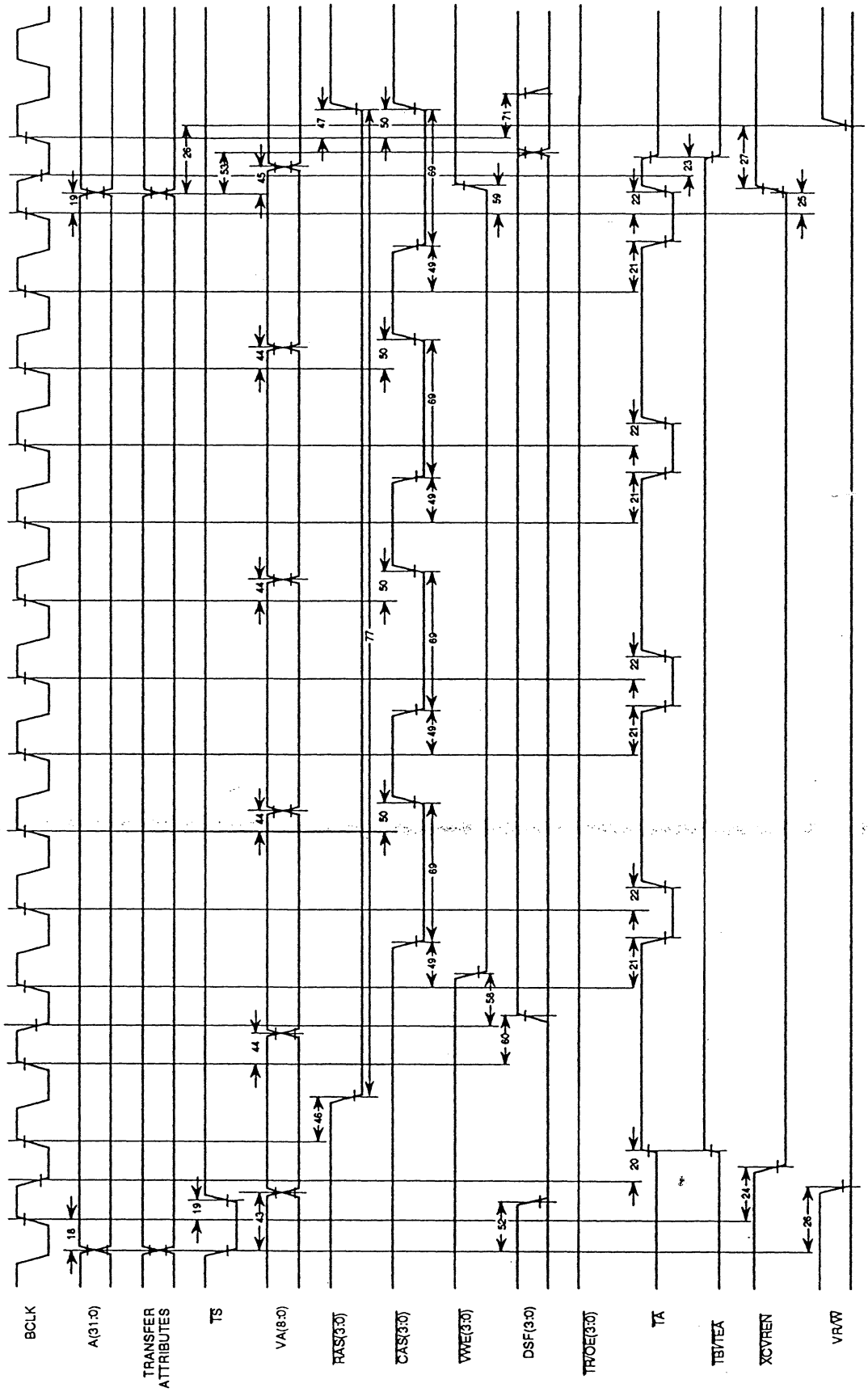


FIGURE 32. 33MHz VRAM BURST WRITE TIMING

Apple Computer, Inc.

SIZE A

DRAWING NUMBER 343S0128-A

SCALE: NONE

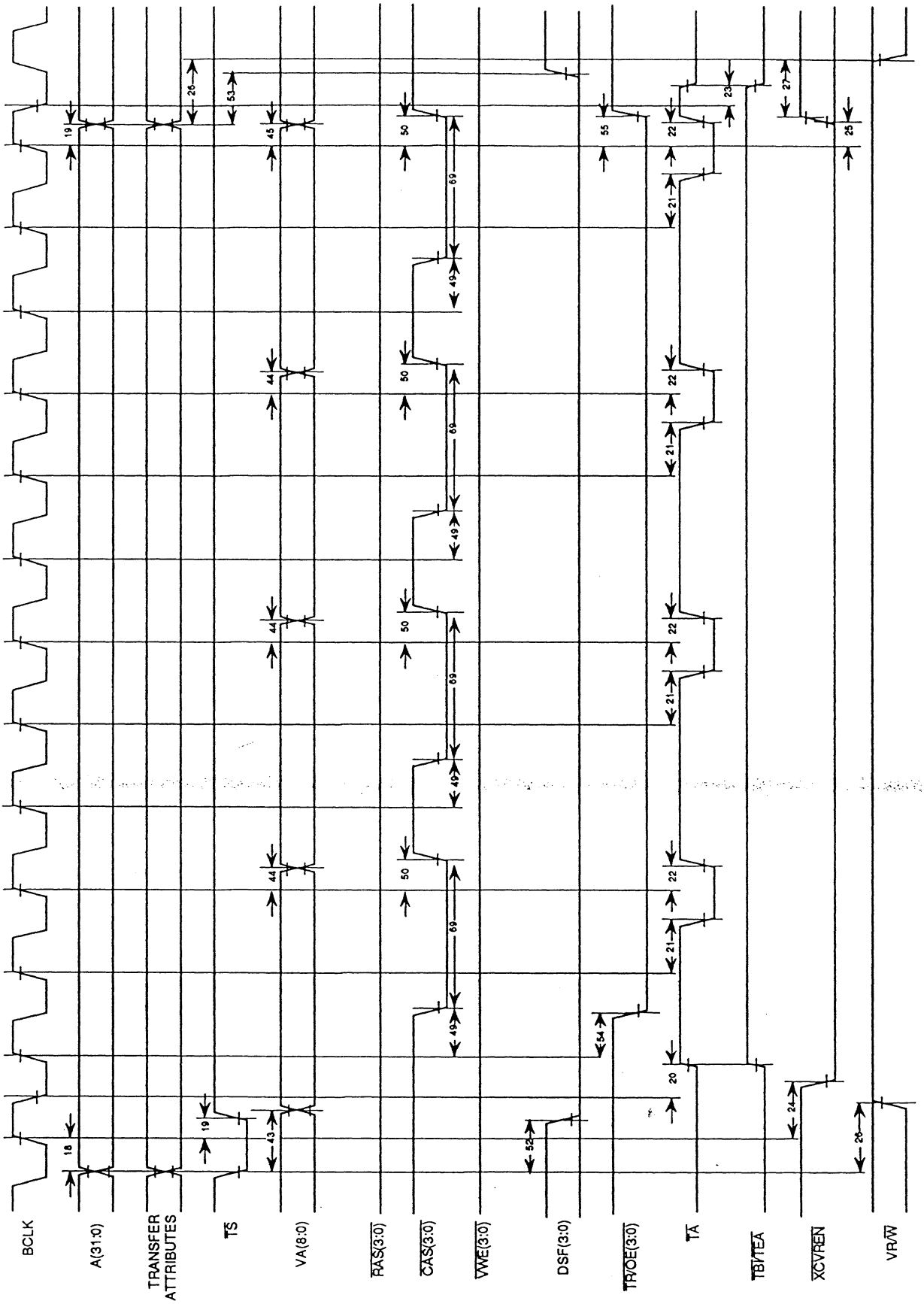


FIGURE 33. 33MHz VRAM PAGE MODE BURST READ TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 43 OF 98

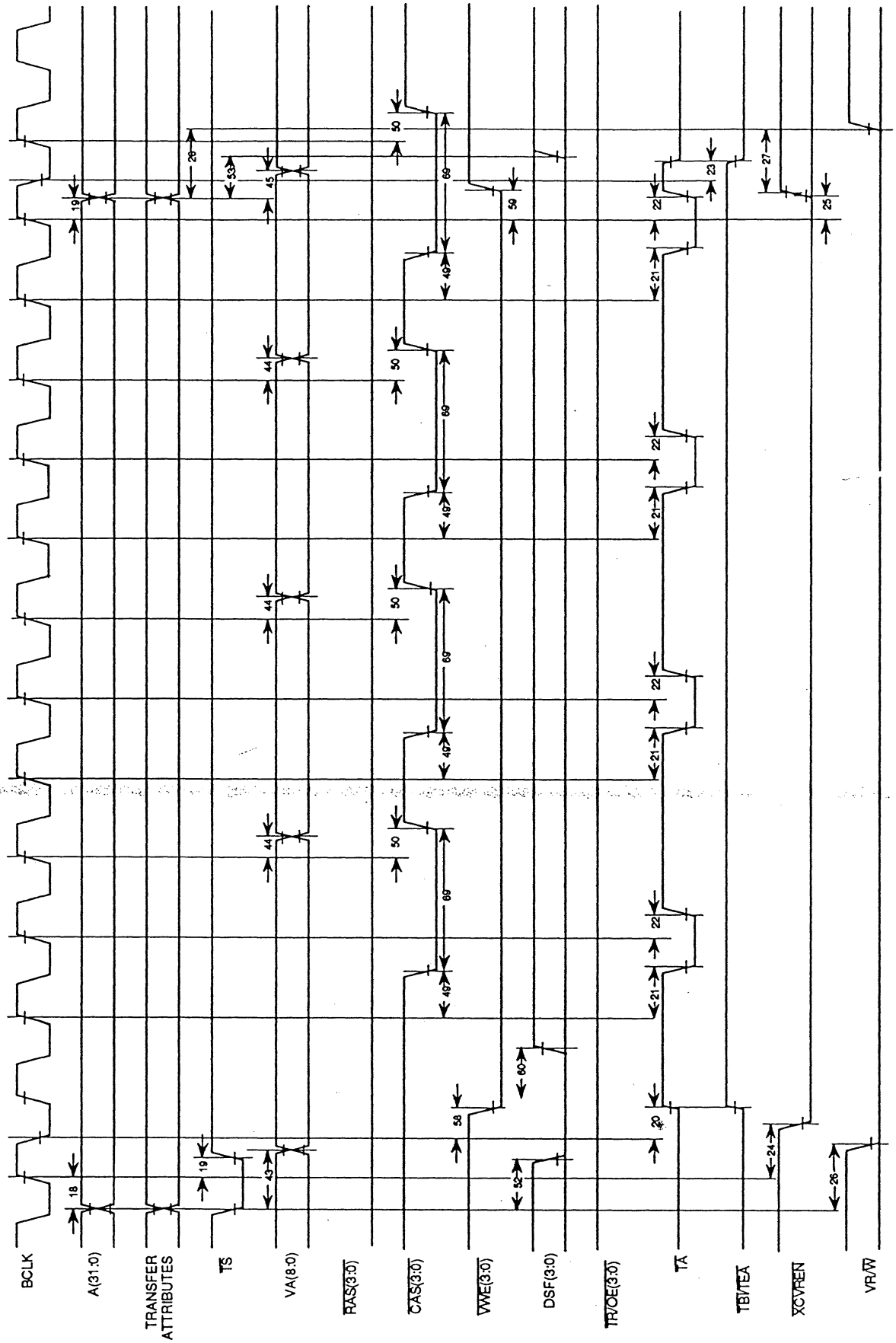


FIGURE 34. 33MHz VRAM PAGE MODE BURST WRITE TIMING

Apple Computer, Inc.

SIZE A

DRAWING NUMBER 343S0128-A

SCALE: NONE

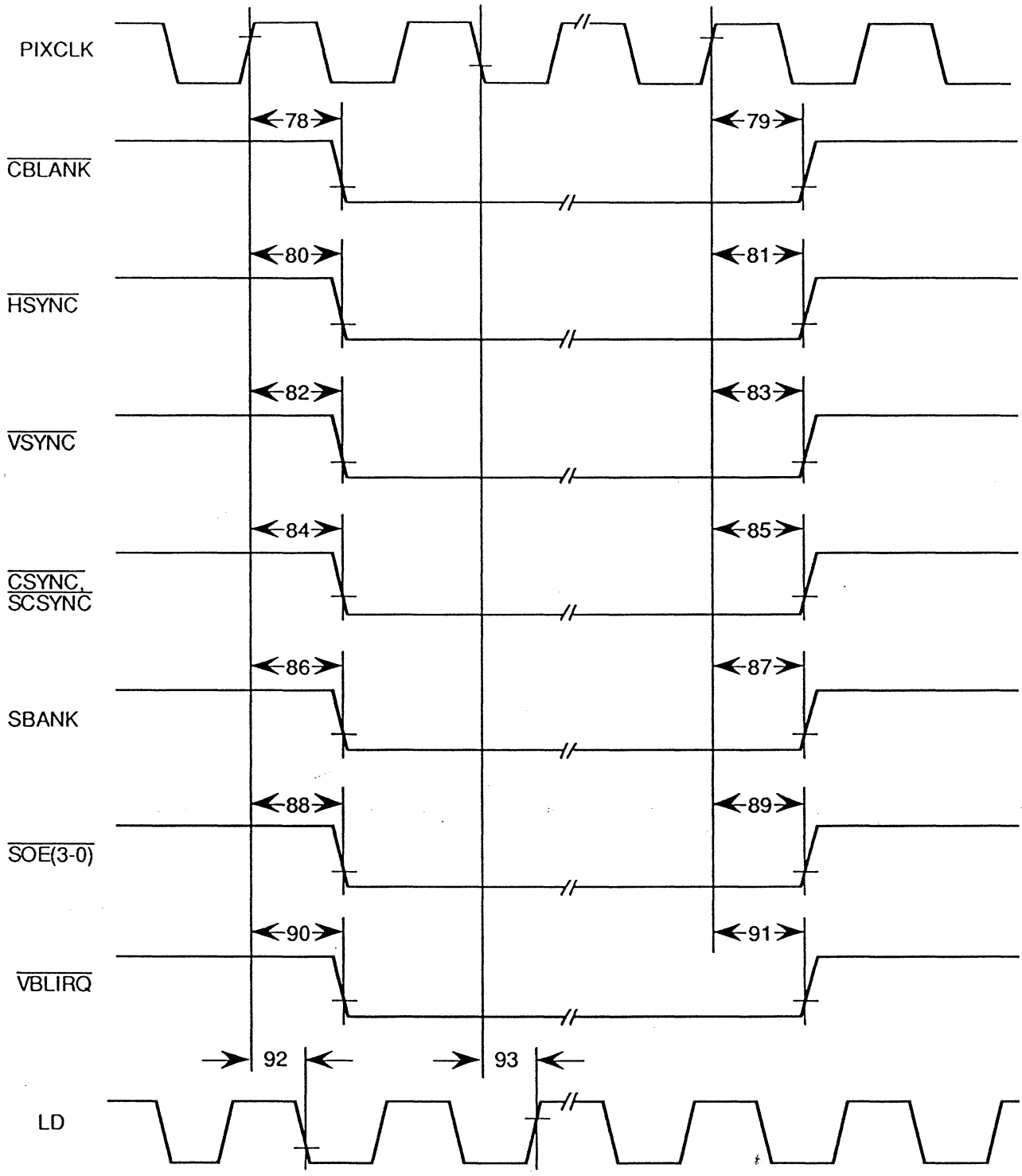
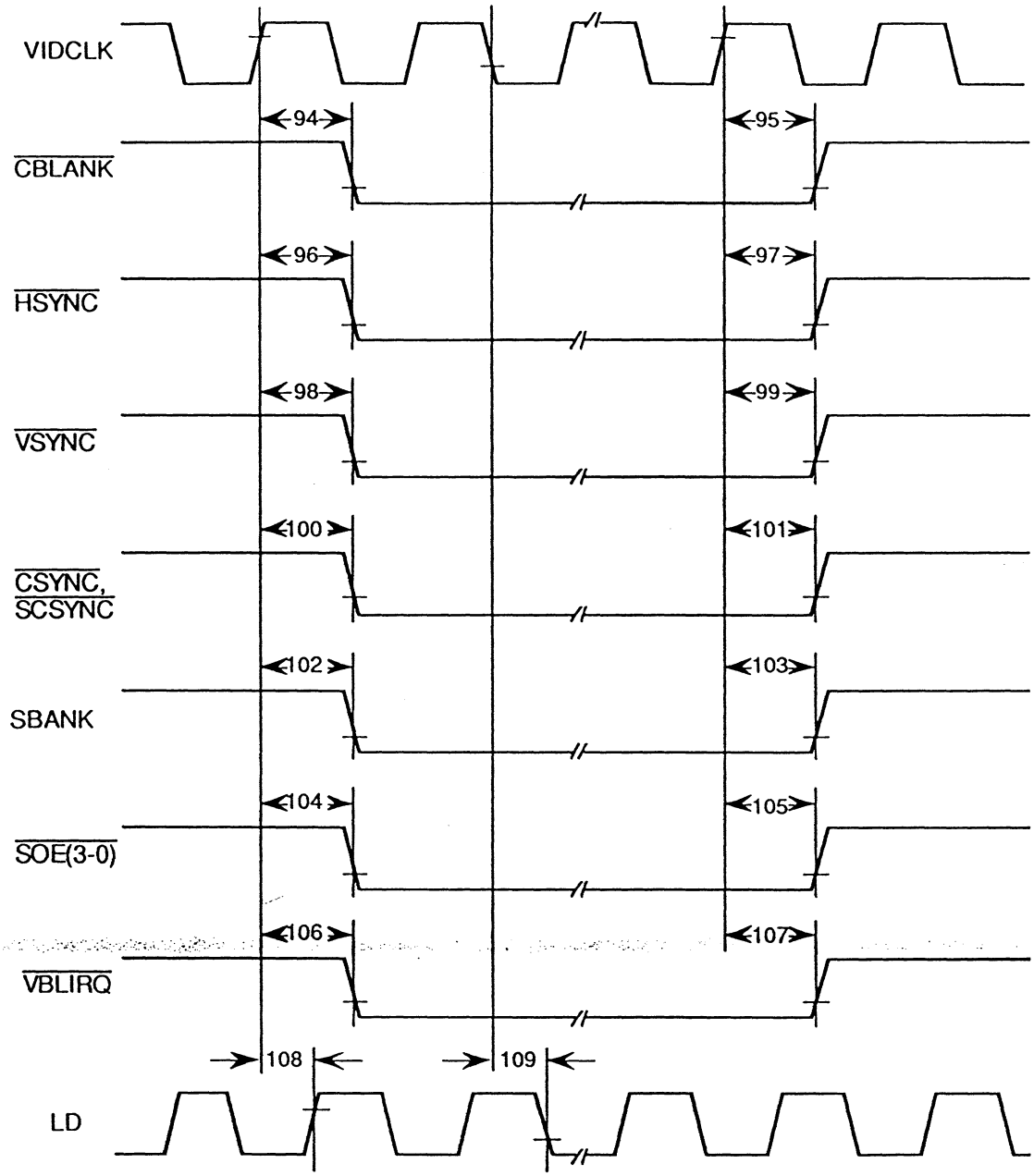


FIGURE 35. PIXCLK-DRIVEN VIDEO OUTPUT TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 45 OF 98



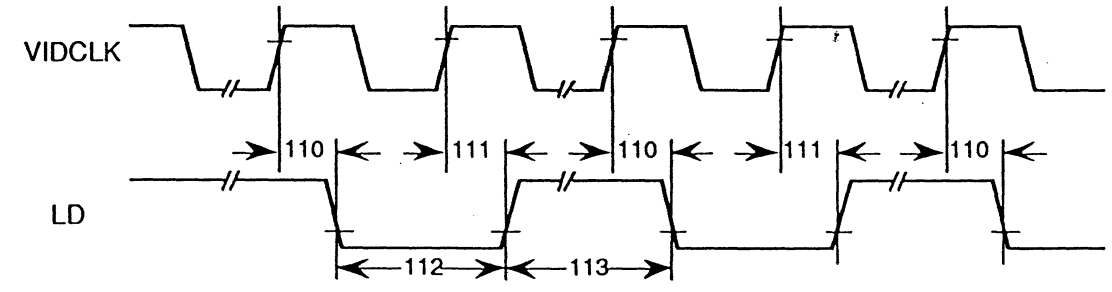


FIGURE 36. VIDCLK-DRIVEN VIDEO OUTPUT TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 46 OF 98

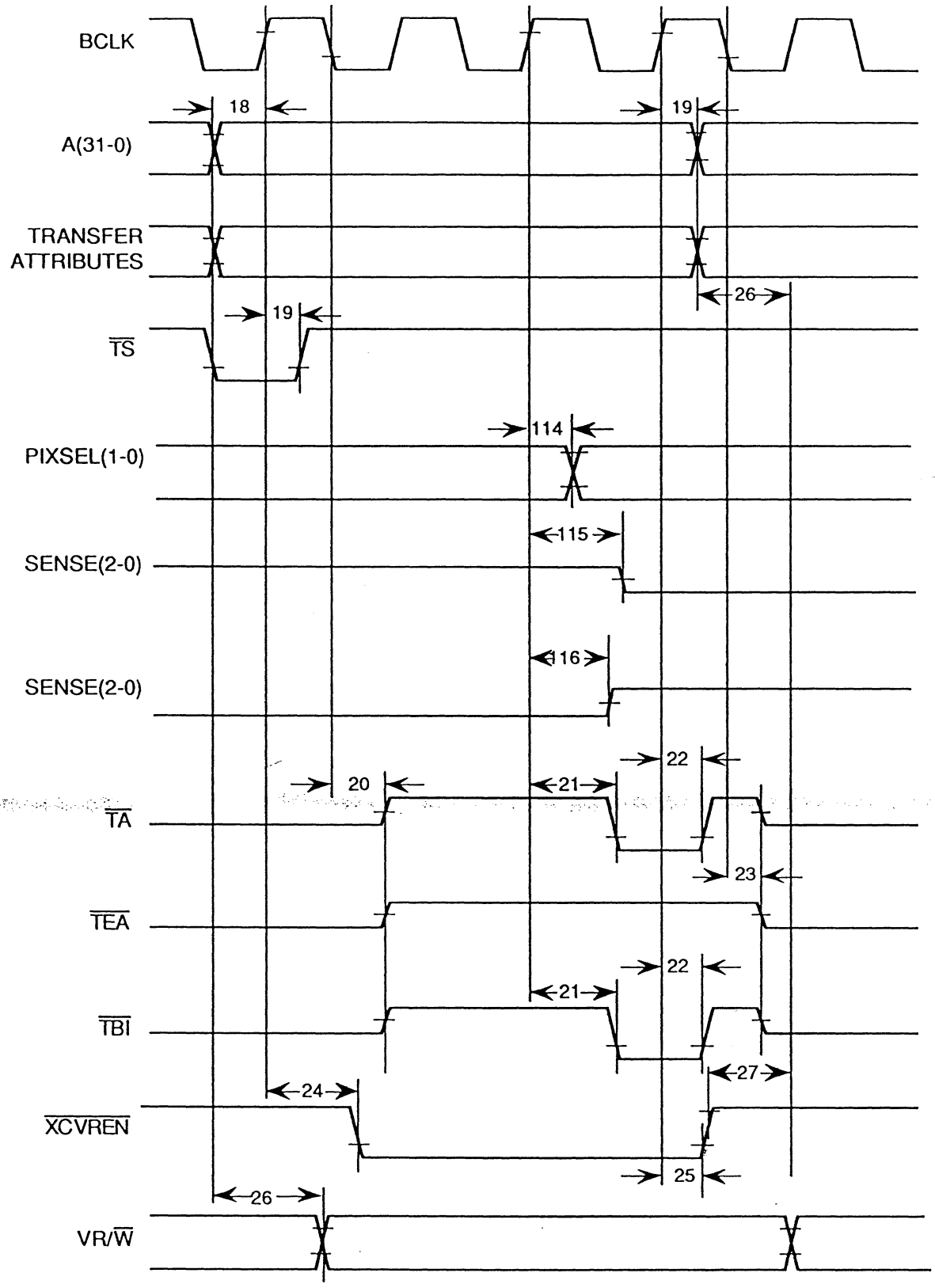


FIGURE 37. SENSE & PIXSEL WRITE TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 47 OF 98

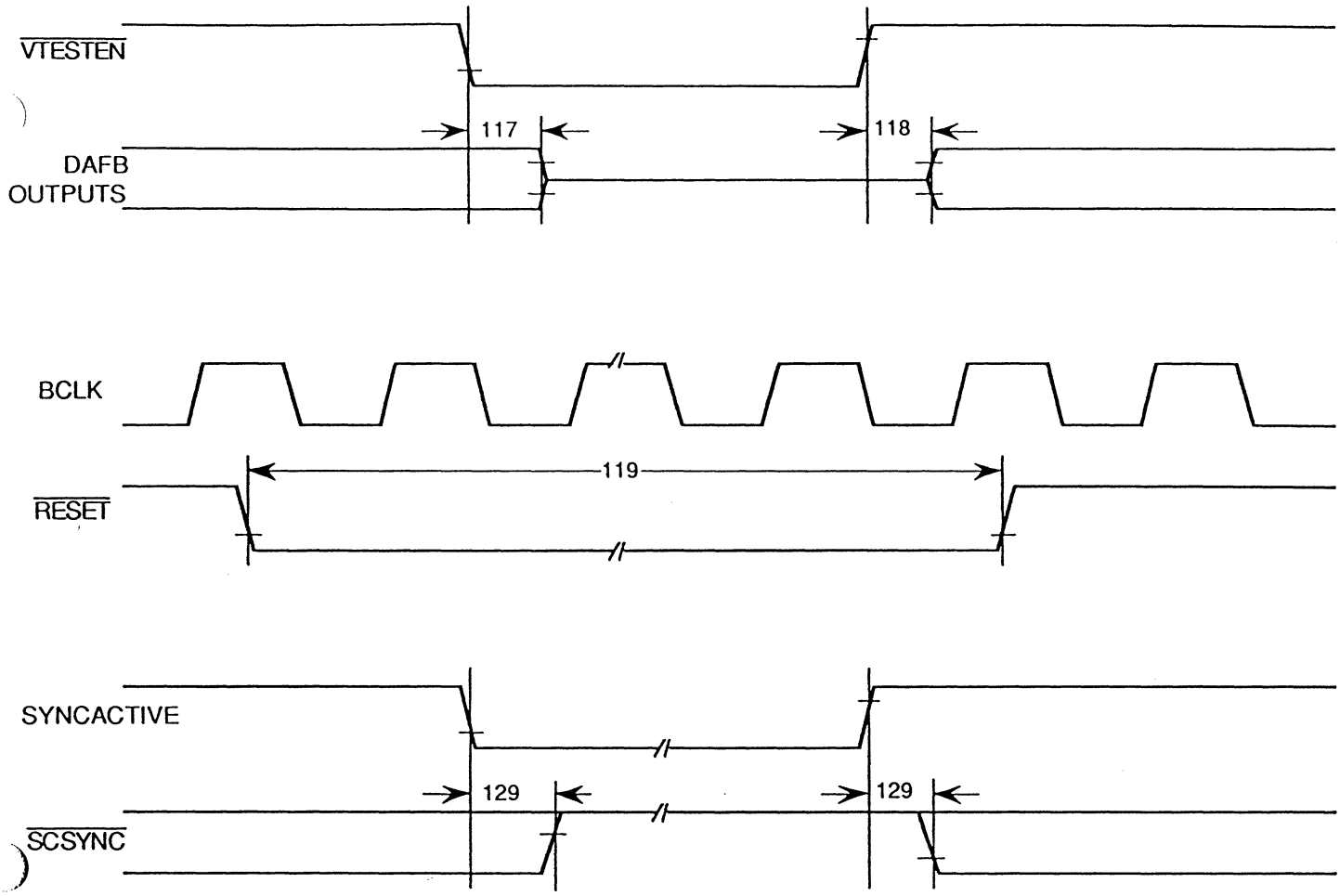


FIGURE 38. MISCELLANEOUS SIGNAL TIMING

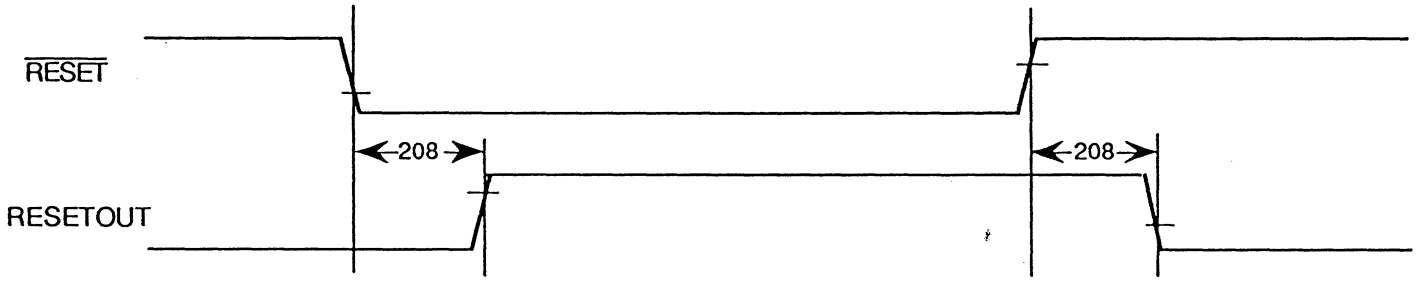
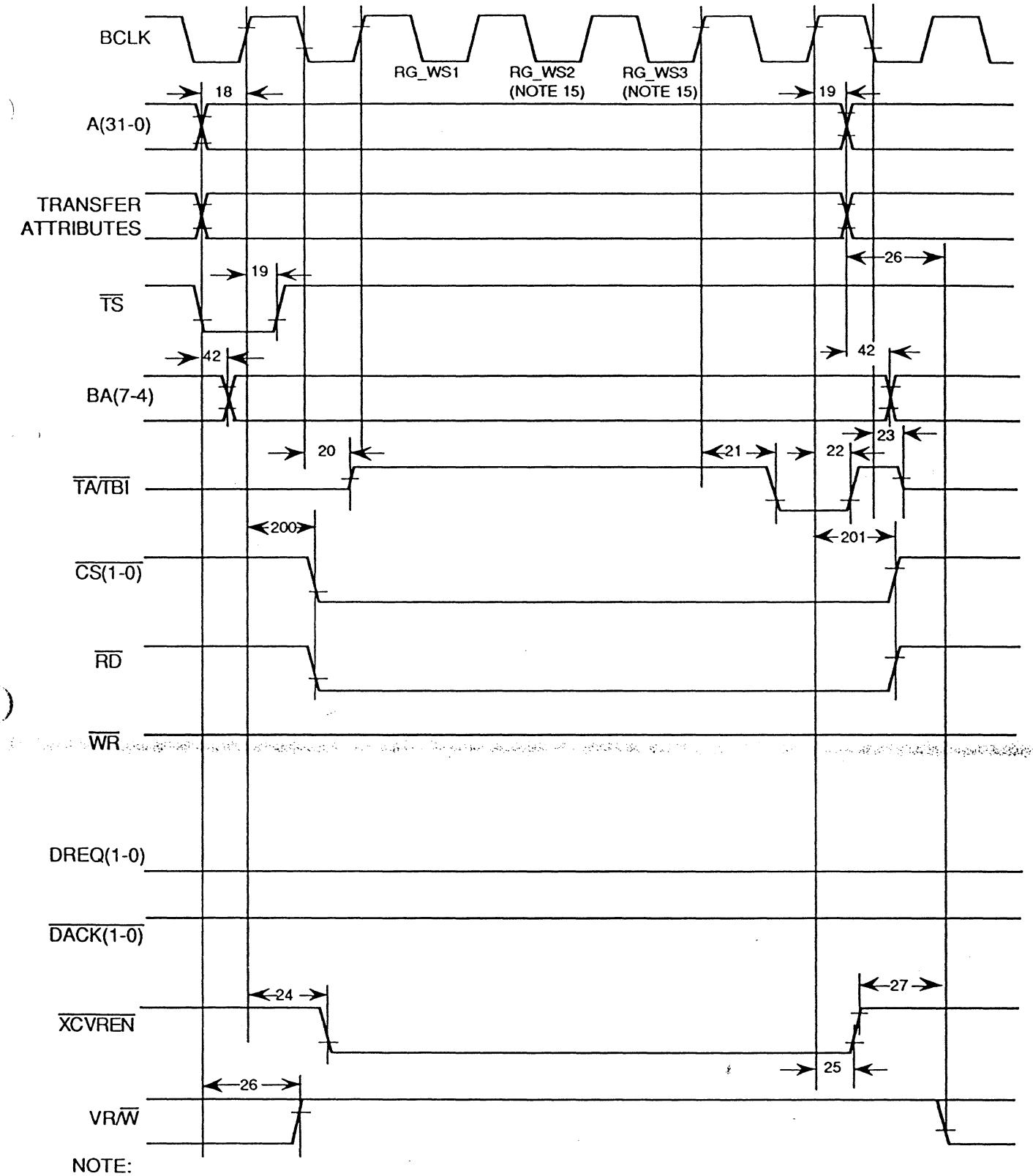


FIGURE 39. TURBO SCSI RESET OUT TIMING

Apple Computer, Inc.

SIZE A | DRAWING NUMBER 343S0128-A | SCALE: NONE | SHT 48 OF 98



NOTE:

15. Pictured above is a 6 clock register read cycle.
    For a 5 clock register read cycle, skip RG_WS3; for a 4 clock register read cycle, skip RG_WS3 and RG_WS2.

FIGURE 40. TURBO SCSI 53C96 REGISTER READ TIMING (6, 5, or 4 CLOCKS)

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 49 OF 98

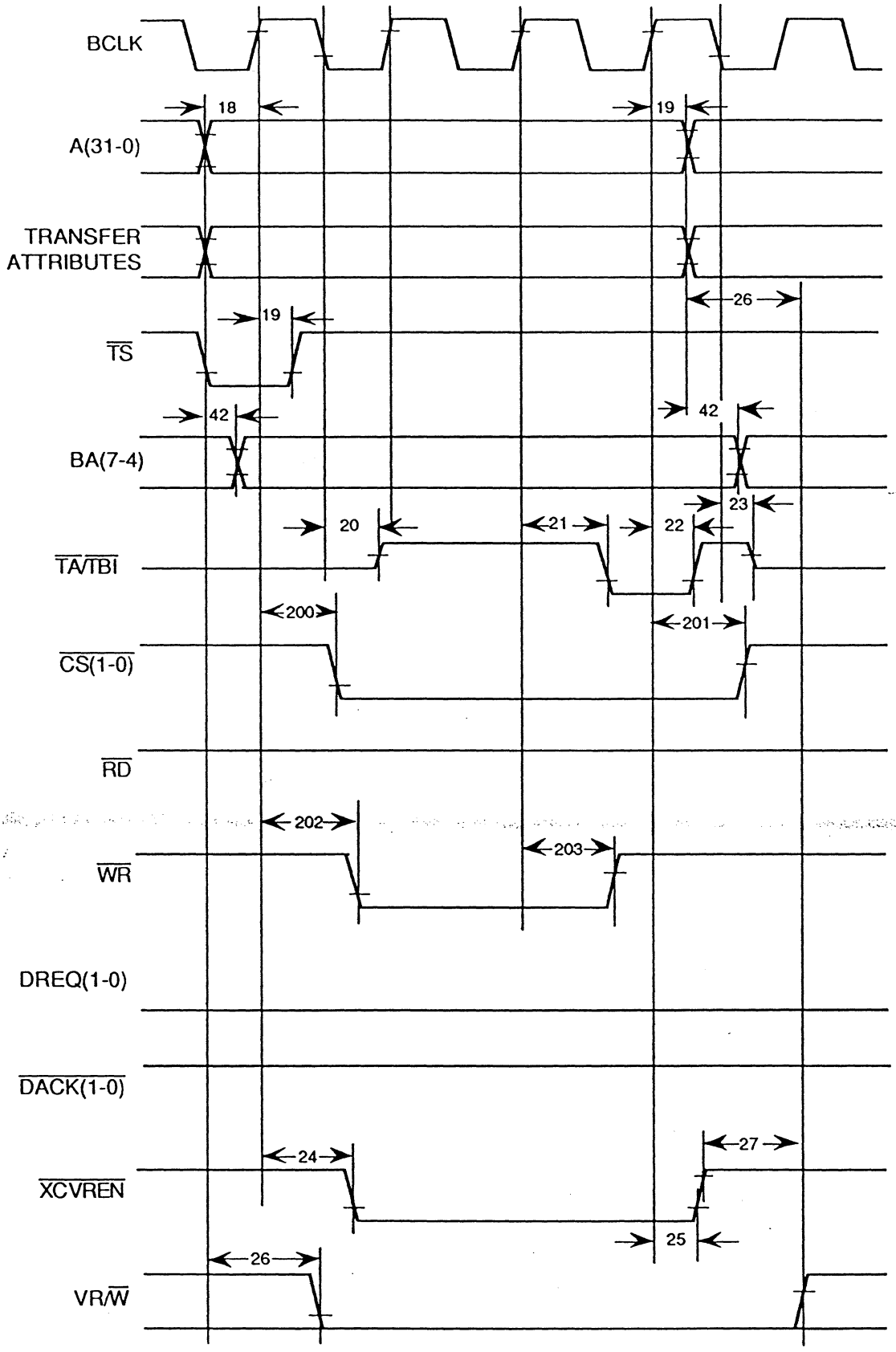


FIGURE 41. TURBO SCSI 53C96 REGISTER WRITE (4 CLOCKS)

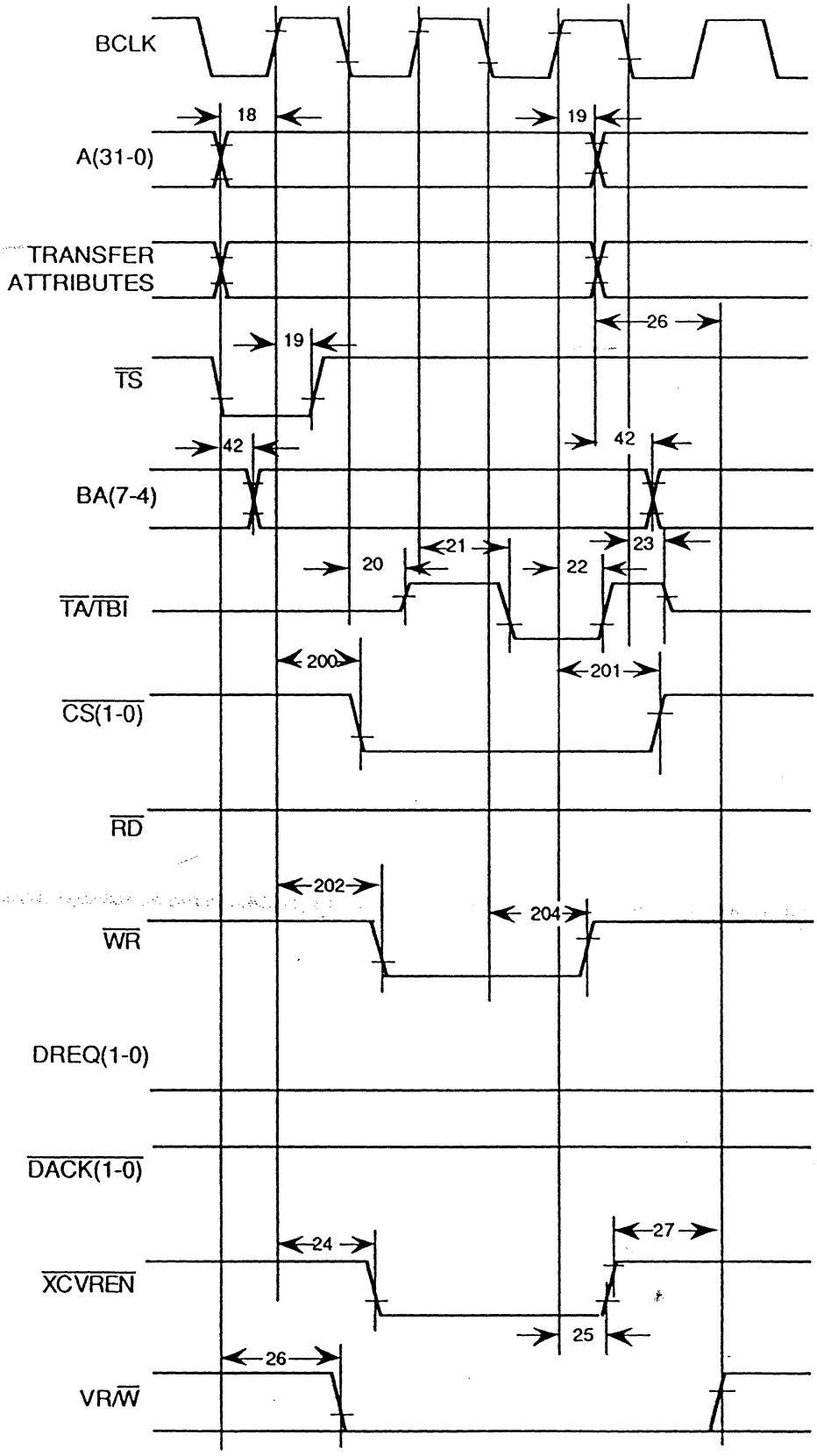
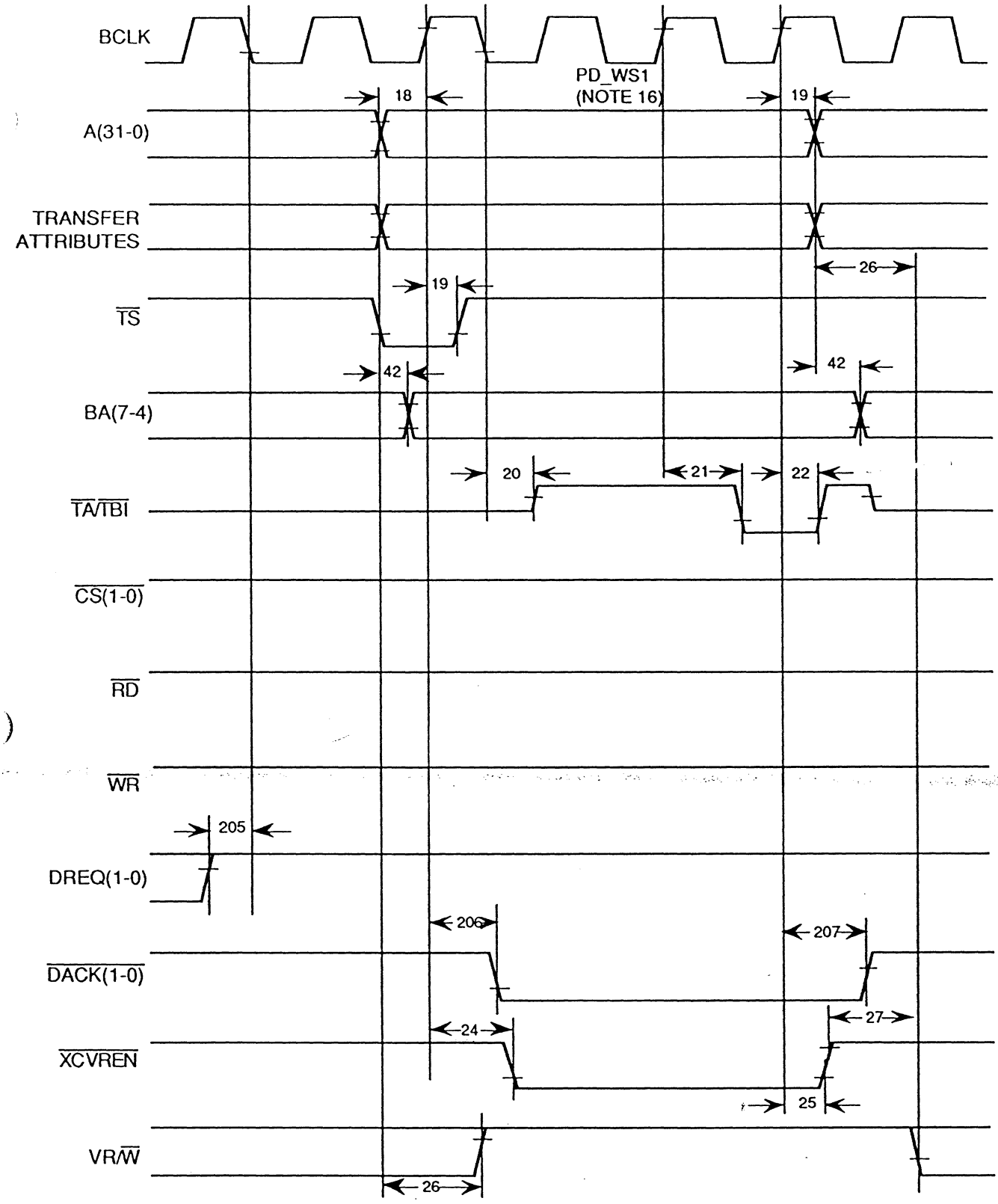


FIGURE 42. TURBO SCSI 53C96 REGISTER WRITE (3 CLOCKS)

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 51 OF 98



NOTE:

16. Pictured above is a 4 clock pseudo DMA read cycle. For 3 clock pseudo DMA read cycle, skip PD_WS1.

FIGURE 43. TURBO SCSI 53C96 PSEUDO DMA READ (4 or 3 CLOCKS)

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 52 OF 98

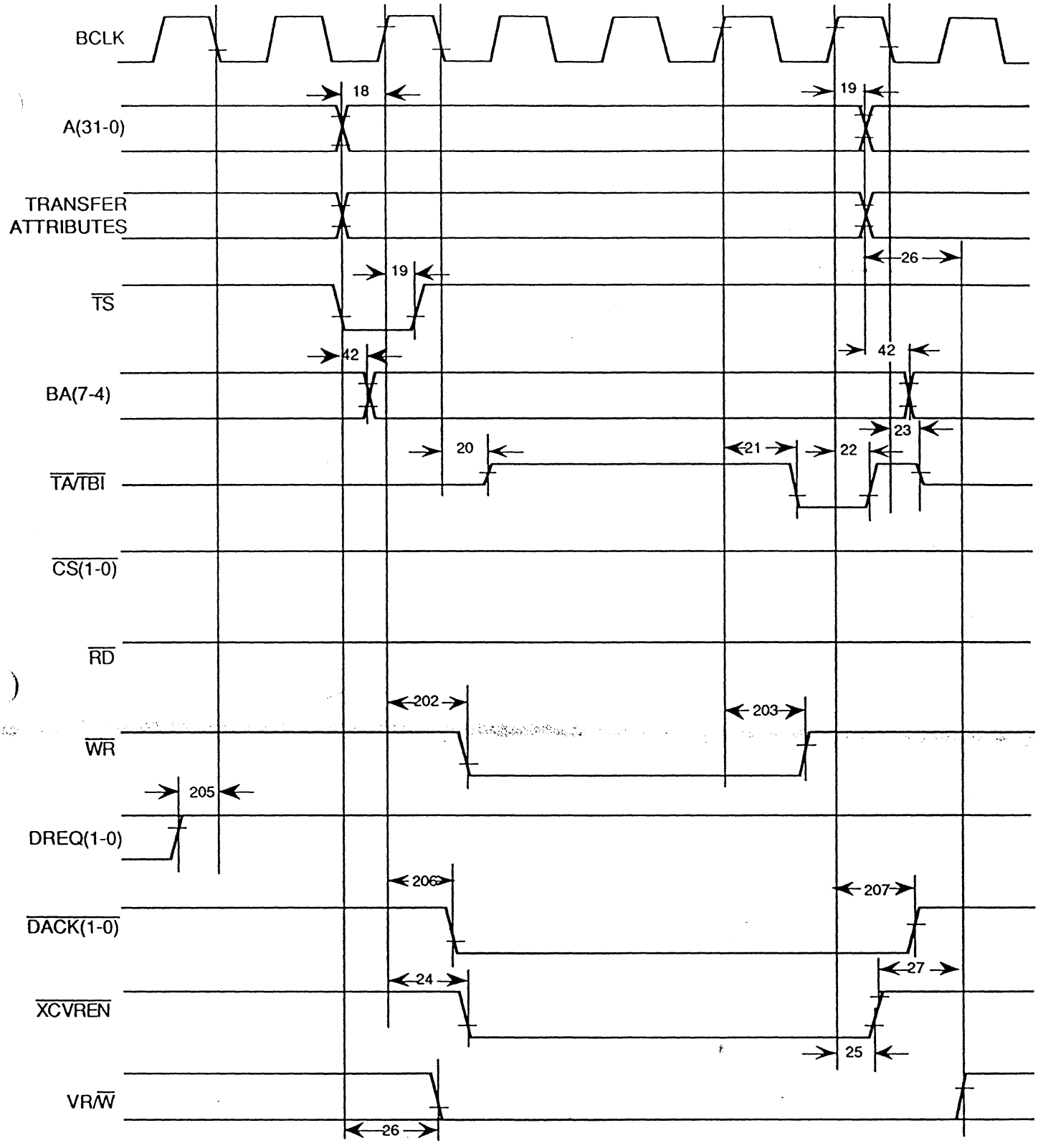
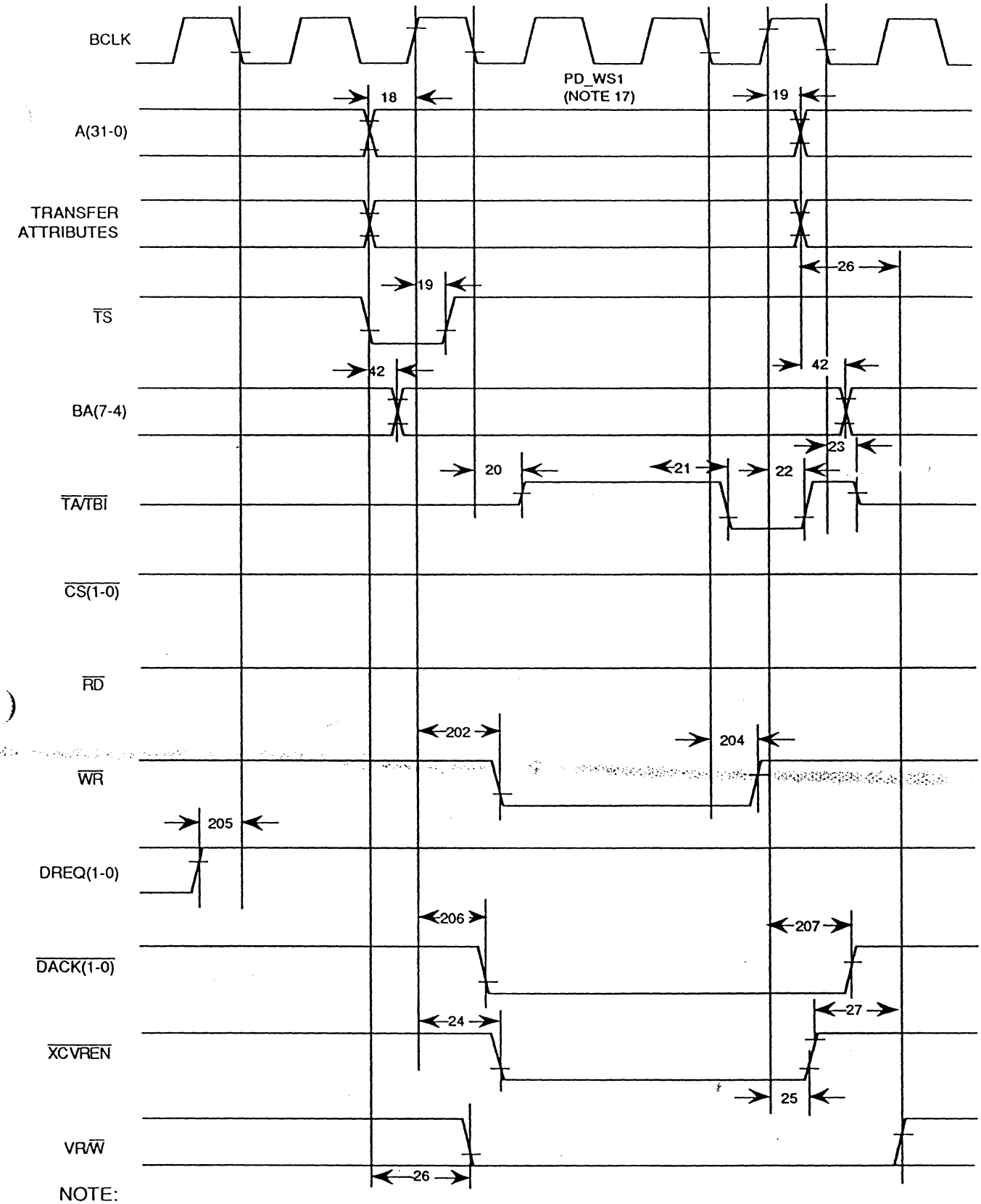


FIGURE 44. TURBO SCSI 53C96 PSEUDO DMA WRITE (5 CLOCKS)

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 53 OF 98



NOTE:

17. Pictured above is a 4 clock pseudo DMA write cycle.
    For a 3 clock pseudo DMA write cycle, skip PD_WS1.

FIGURE 45. TURBO SCSI 53C96 PSEUDO DMA WRITE (4 or 3 CLOCKS)

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 54 OF 98

5.0 **SUPPLEMENTARY INFORMATION:** The following is not to be used for the acceptance nor rejection of the part herein.

6.1 **REFERENCES:** The following is a list of all the pertinent ASIC deliverables filed in Document Control:

- SCHEMATIC NETLIST TAPE
- PRINTED LISTING OF FILE NAMES, CELL LIBRARY, SOFTWARE PROGRAM DESIGNATION, AND REVISION LEVEL
- LOGIC DIAGRAM PLOTS
- SPECIFICATIONS FOR PRIMITIVES AND MACRO CELLS
- SIMULATION TAPE AND LISTING
- CRITICAL TIMING ANALYSIS SIMULATION TAPE
- MASK DATA BASE TAPE
- PRODUCTION TEST PROGRAM TAPE AND LISTING
- TEST PROGRAM IN TAR FORMAT
- TEST LANGUAGE DOCUMENTS AND FILE LISTING
- TEST LOAD BOARD
- BONDING DIAGRAM

6.2 **INTRODUCTION:** The DAFB II I.C. is designed to control a video frame buffer and interface it to a 68040 system bus. It provides address decoding for all frame buffer components (VRAM, clock generator, and CLUT/DAC), VRAM control and timing, video timing generation (synchronization and blanking), and timing and control for the frame buffer pixel data bus. DAFB II also provides control and interface for two SCSI I/O channels.

As shown in Figure 46, a complete DAFB II-based frame buffer also includes the following components:

- Clock generator – a frequency programmable clock generator which produces the master frame buffer video clock.
- 74F245 data bus transceivers – isolates the frame buffer data bus from the system data bus (primarily to reduce system bus loading).
- Four 512 Kbyte banks of video RAM (VRAM) – the memory which contains the graphics image to be displayed. VRAM is dual ported memory: one port is accessible via the system bus, the other is used to output pixel data for refreshing the video display.
- 74F399 pixel data bus MUXes – used to MUX data from multiple VRAM banks in order to support pixel data rates higher than can be done with a single bank.
- AC842 CLUT/DAC – inputs pixel data from the 'F399s, video timing from DAFB II, and the pixel clock from the DP8531; unpacks the pixel data; and produces the output RGB analog video signal.

This frame buffer design features a programmable clock generator and CLUT/DAC which can be configured to support a wide range of video timings and pixel depths. It supports all of Apple's current video monitors, and also provides support for several forthcoming products. Figure 47 lists a number of specific monitor configurations which are supported.

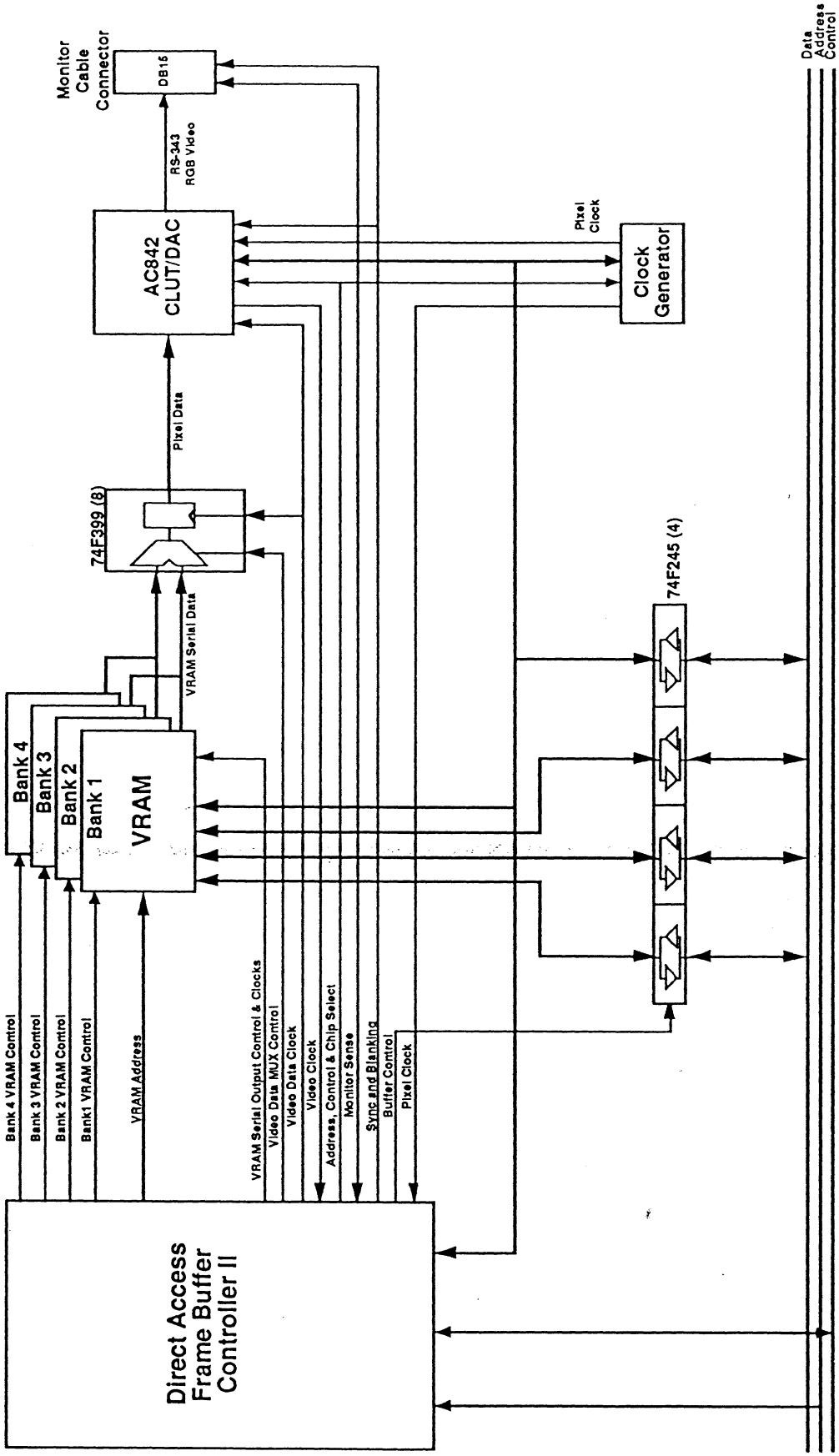


FIGURE 46. DAFB II-BASED FRAME BUFFER BLOCK DIAGRAM

Display Resolution	Bits Per Pixel					
	1	2	4	8	16	32
512 x 384 (12-inch landscape)	1	1	1	1	1	2
640 x 480 (13-inch landscape)	1	1	1	1	2	4
640 x 480 (NTSC)	1	1	1	1	2	4
640 x 480 (NTSC w/ conovlution)	2	2	2	2		
768 x 576 (PAL)	1	1	1	1	2	4
768 x 576 (PAL w/ convolution)	2	2	2	2		
832 x 624 (16-inch landscape)	1	1	1	1	2	4
640 x 870 (15-inch portrait)	1	1	1	2	4	
1152 x 870 (21-inch landscape)	1	1	1	2	4	

1 bank (0.5 Mbytes)
2 banks (1 Mbyte)
4 banks (2 Mbytes)
Not supported

FIGURE 47. SUPPORTED DISPLAY RESOLUTIONS

6.3 IMPLEMENTATION: DAFB II is composed of seven major functional blocks (as shown in Figure 2):

1) System Bus Interface
2) Address Decoding
3) Configuration and Status Registers
4) Video Timing (Swatch)
5) Video Refresh Timing Generator
6) VRAM Controller
7) Turbo SCSI Controller

Each of these seven functional blocks will be discussed in the following sections.

6.3.1 System Bus Interface: The System Bus Interface module provides the interface to the Eclipse system bus for the frame buffer. It generates all system bus cycle timing for interfacing DAFB II and other frame buffer components (clock, CLUT/DAC, VRAM, and data bus transceivers) to the system bus, and also generates chip selects for the CLUT/DAC and clock chips.

The module inputs system bus control information along with select lines for frame buffer, memory, chip, and register accesses from the Address Decode module. It outputs the $\overline{TA}$, $\overline{TEA}$, and $\overline{TBI}$ control signals to the system bus. It also controls the DAFB II data bus output driver, enabling it for the appropriate frame buffer access.

The core of the System Bus Interface module is a state machine which generates the system bus cycle timing and control signals. A diagram of the state machine is shown in Figure 48. The state machine normally resides in an idle state. From the idle state, a number of different types of

cycles may be started. A valid bus cycle to the frame buffer address space will cause a transition from the idle state:

- If the specified address is to super slot space ($9XXX XXXX) or to the unused portion of slot space, the state machine will issue a $\overline{TEA}$ and return to the idle state.
- If the bus cycle is for a DAFB II register (RCYC), a register cycle is begun. Burst operations are not supported for DAFB II registers, and an attempt to perform any operation to a register will result in the assertion of $\overline{TBI}$ along with $\overline{TA}$.
- If the bus cycle is intended for one of the other frame buffer chips (CCYC), the appropriate cycle type is initiated, a chip select is generated for the selected chip, and $\overline{TA}$ is asserted at the end of the cycle. Burst operations are not supported for frame buffer chips (but are supported for VRAM), and any access to a chip will result in the assertion of $\overline{TBI}$ along with $\overline{TA}$. For the CLUT/DAC and Endeavor, an extra state is inserted in the cycle if the frame buffer is being operated with a 33 MHz system bus.
- If the bus cycle is for frame buffer VRAM (MCYC), then the state machine enters a waiting condition until a transfer acknowledge arrives from the VRAM controller. If cycle is a line operation, then an end-of-line condition must also be true to end the cycle. Line operations are not allowed with word interleaved VRAM, so a $\overline{TBI}$ is asserted along with $\overline{TA}$ if this occurs.

6.3.2 Address Decoding: The Address Decoding block provides address decoding for frame buffer memory operations, configuration and status registers, and external chip selects. It provides outputs for accesses into frame buffer address space as a whole (slot and super slot space), VRAM memory space, external chip space(s), and individual select lines for each of the DAFB II registers. It also outputs a signal to the VRAM controller indicating when it is time to load a new line address, and produces a signal to enable the frame buffer's 'F245 data bus transceivers.

This module inputs address lines (31-2), along with the system bus control signals $\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{TBI}$, and TT1. The system bus control signals are used to generate an internal "bus transfer in progress" signal which is started by a $\overline{TS}$, and ended by a $\overline{TA}$ or $\overline{TEA}$. This signal is used to condition the decoded address lines to produce valid address-decoded select lines.

6.3.3 Configuration and Status Registers: DAFB II contains a large number of configuration and status registers. These are used for programming the behavior of the video timing block, setting up the VRAM addressing and video refresh scheme, configuring the frame buffer clock, detecting the type of display connected to the frame buffer connector, setting the VRAM operating mode, controlling and clearing interrupts, and resetting the DAFB II hardware. A complete description of the function of all the DAFB II registers is found in section 6.6.

The Registers module contains the physical registers used to hold the above configuration values. From these registers, configuration information is bused to other DAFB II modules, or is directed outside of the chip in the case of the 3 pixel clock select lines and the 3 monitor type sense lines. This module also inputs interrupt status from Swatch in order to make this information available via a 'register' read operation.

Individual register select lines come from the Address Decode module. These register select lines are combined with control signals from the System Bus Interface module to individually enable read/write operations from/to the registers. Data to be written to the registers is taken from the 12-bit external data bus input. Data to be read from the registers is enabled onto an internal, tristate 12-bit data bus. The System Bus Interface module then enables this internal bus onto the external 12-bit data bus.

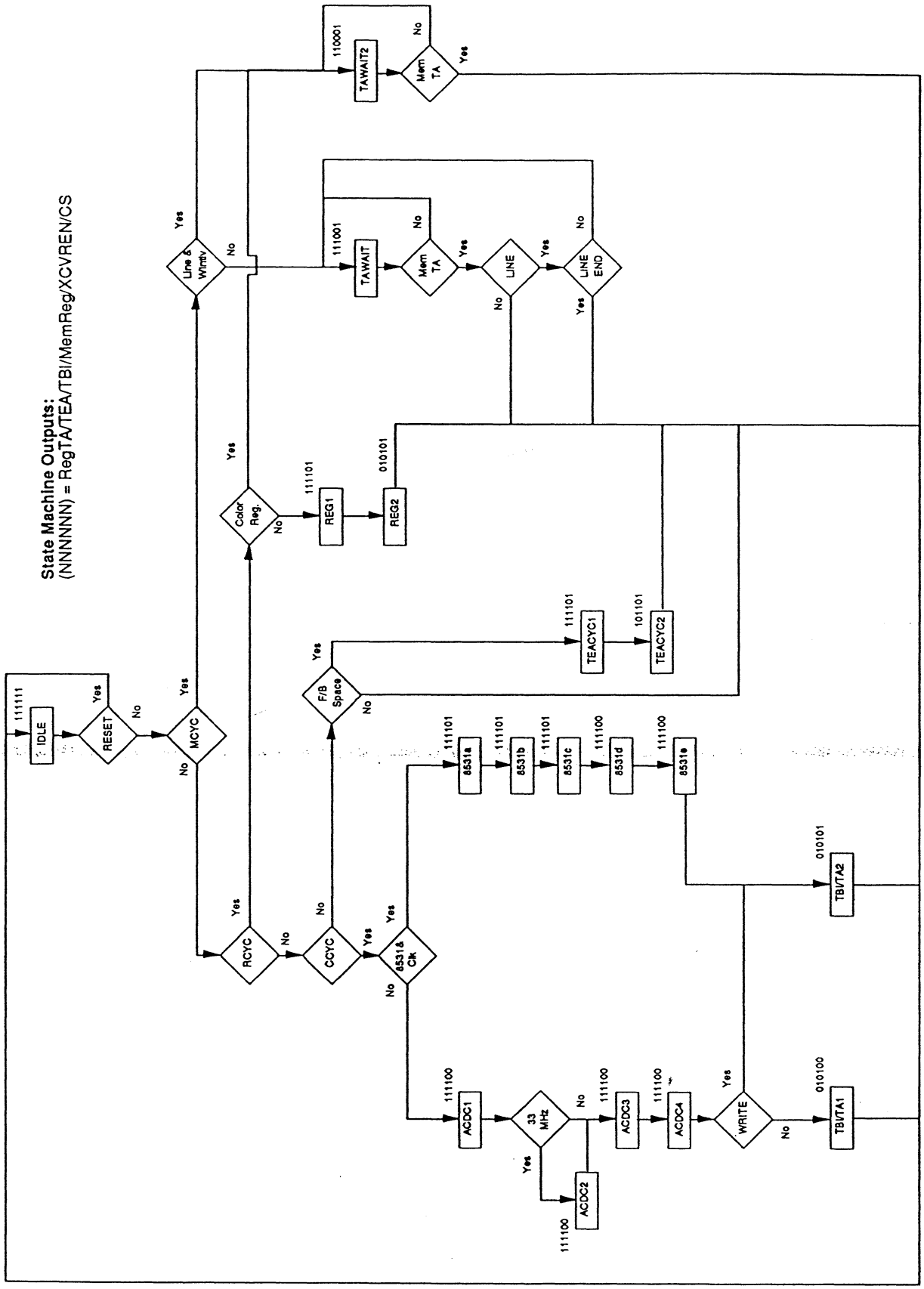


FIGURE 48. BUS INTERFACE STATE MACHINE DIAGRAM

Apple Computer, Inc.

SIZE A

DRAWING NUMBER 343S0128-A

SCALE: NONE

6.3.4 Video Timing (Swatch): Swatch is the video timing generator for DAFB II. It receives configuration information from the Registers module and a video clock from the Video Refresh Timing Generator, and then produces a number of video timing signals, including sync, blank, and video-related interrupts. It provides several other video timing signals to the Video Refresh Timing Generator for use in synchronizing the pixel data stream to the basic video timing.

Swatch is intended to be a generic, reusable video timing block for Apple video timing applications. DAFB II uses the standard version of Swatch, but with a number of modifications for performance and gate reduction:

- Since DAFB II does not support genlock to an external sync signal, the genlock circuitry in Swatch has been removed.
- Extra pipeline stages have been added to the horizontal timing section to allow it to operate at a higher clock frequency (up to 60 MHz). Several of the horizontal timing register values must be changed (decreased by 1) to allow for this pipelining.
- The vertical timing block has been modified to run at half the clock frequency of the horizontal timing block for performance reasons. The half speed clock is synchronized with the 'half line' signal from the horizontal timing block.
- Swatch timing can be locked to a phase of DAFB II's VIDCLOCK input signal. This permits proper generation of sync and blank relative to VIDCLOCK when LD is used as the main clock input to the CLUT/DAC (i.e., LD > 33 MHz).
- The horizontal blanking signal has been deleted as a Swatch output, and composite blanking signals (with DAFB II specific timing required by the Video Refresh Timing Generator) have been added. In addition, the standard Swatch pipeline delay has been deleted, and more flexible, programmable delay has been added to the one of the special composite blanking signals used by the Video Refresh module.
- A "Swatch enable" input signal has been added.
- An extra sync output, $\overline{\text{SCSYNC}}$, has been added. It is identical to the $\overline{\text{CSYNC}}$ ouput, but can be disabled via the SYNCACTIVE pin. When SYNCACTIVE is low $\overline{\text{SCSYNC}}$ is always high; when SYNCACTIVE is high $\overline{\text{SCSYNC}}$ mirrors the behavior of $\overline{\text{CSYNC}}$.

For more complete information about the internal operation of Swatch, consult the Swatch Specification, Version 2.01, February 15, 1990.

6.3.5 Video Refresh Timing Generator : The Video Refresh Timing Generator module generates all signals needed to do dynamic RAM refresh of the frame buffer VRAM, generates the addresses and control signals required to refresh the video display (i.e., it controls the VRAMs to generate the pixel data stream used by the AC842 to produce an analog video output), and controls the incoming video clocks to generate the required video output clock.

The module is controlled by display configuration data obtained from the Registers module. Based on the display format configuration, it generates video refresh timing and addresses. The video refresh generation is synchronized to the basic video timing information input from Swatch. At the beginning of every blanking interval (using a special blanking signal generated by a modified Swatch), the module computes the VRAM address at which pixel data for the next display line is located, and issues a request(s) to the VRAM Controller module for a read transfer cycle(s) to load the VRAM serial access memories (SAMs) with the pixel data (see section 6.5.2 for a description of SAM loading). The address for the SAM read transfer is also supplied to the VRAM Controller. Since this module and the VRAM Controller operate from asynchronous clocks, the request signal is synchronized to the VRAM controller clock before being passed to the VRAM controller. When the VRAM Controller acknowledges the SAM read transfer request(s), the

acknowledge is in turn synchronized to the video clock. Once the read transfer request(s) has been acknowledged, a request(s) is made for the VRAM Controller to run one or more refresh cycles. The request/acknowledge cycle is handled similarly to the read transfer cycle.

When the video timing signals from Swatch indicate that the active video portion of a horizontal line is to begin, the Video Refresh Timing Generator begins producing the VRAM serial clock(s) and output enable(s) required to clock data out of the VRAM SAM(s). A pixel load clock is also produced to clock the VRAM pixel data into the 'F399s and the AC842. A bank select signal is sent to the 'F399s to select pixel data from the proper VRAM bank(s). Depending on the display configuration, it may be required to reload the VRAM SAM(s) during the middle of an active video line. If so, one or more requests for split SAM read transfer cycles are sent to the VRAM Controller in a manner similar to that used at the beginning of a horizontal blanking interval. (A VRAM refresh is not performed, however.)

Requests to the VRAM Controller for SAM read transfer cycles and refresh cycles are controlled by a state machine, shown in Figure 49 on the following page. From the power-up idle state, the state machine first looks for the beginning of a blanking interval, and then issues a request for a SAM read transfer cycle. Following an acknowledge from the VRAM controller, if another read transfer is required (e.g., convolution is active), then an additional request is issued. After the acknowledge, it then issues a request for a refresh cycle and waits for that cycle to be acknowledged. If additional refresh cycles are required, as specified by the 'refresh count' value in the configuration register (see section 6.6.1), then requests are also issued for those cycles, with each cycle in turn being acknowledged by the VRAM Controller. The state machine then waits for the end of the blanking period. Once the active video line time has begun, the state machine continually checks to see if another blanking interval has started, in which case the above sequence is repeated, or if a mid-line split SAM read transfer(s) is required. A change in the QSF input signal is used to trigger the issuing of a split read transfer request. After a split read transfer request/acknowledge cycle has been completed, the state machine once again continually checks for a new blanking interval start, or for a change in QSF. This process repeats indefinitely.

The Video Refresh Timing Generator module also uses the configuration data from the Registers to select the correct incoming pixel data clock (either from the AC842 or directly from the clock generator), direct that clock to Swatch, and, if required, divide down the clock frequency by the amount specified by a configuration register.

6.3.6 VRAM Controller: The VRAM Controller module generates all VRAM memory cycles for the 4 VRAM banks based on VRAM cycle requests from the Address Decode module or the Video Refresh Timing Generator. The module is composed of four instances of a VRAM control state machine (one for each bank to support independent page mode for the 4 banks) along with additional logic for the generation of write-enable and DSF signals, row/column address MUXing, and logic for page hit detection. The VRAM controller operates synchronously with the System Bus Interface module (i.e., it is clocked by the system bus clock).

The core of the VRAM Controller module is the state machine which generates all VRAM cycles and control signals ($\overline{RAS}$, $\overline{CAS}$, DSF, $\overline{WE}$, and $\overline{TR/OE}$). A diagram of the state machine is shown in Figure 50a/b. The state machine normally resides in one of two idle states, one for page mode operation and one for "normal" operation. From the idle states, a number of different types of VRAM cycles may be started. A valid VRAM cycle request will cause a transition from the current idle state:

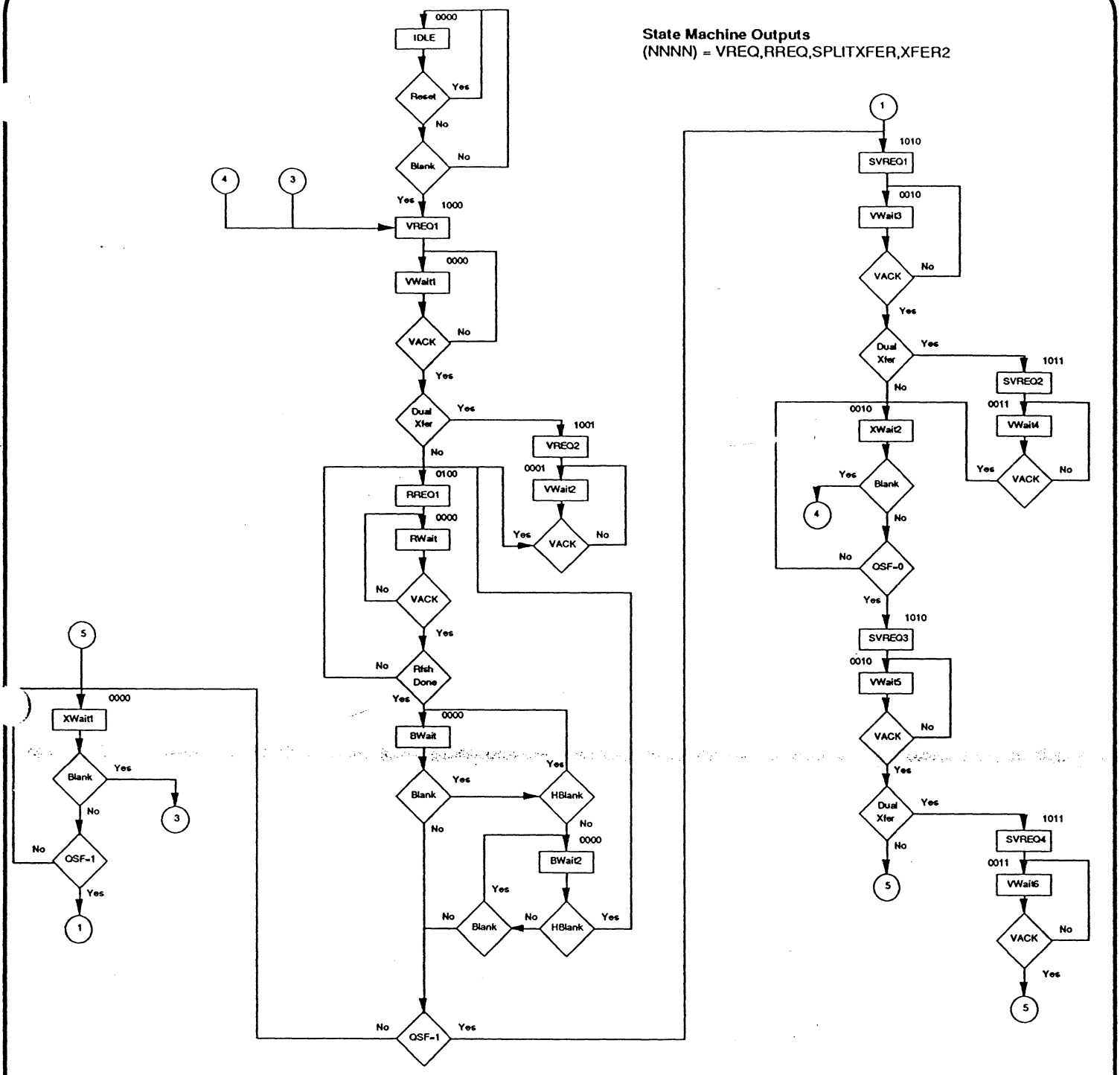


FIGURE 49. VIDEO REFRESH TIMING STATE MACHINE DIAGRAM

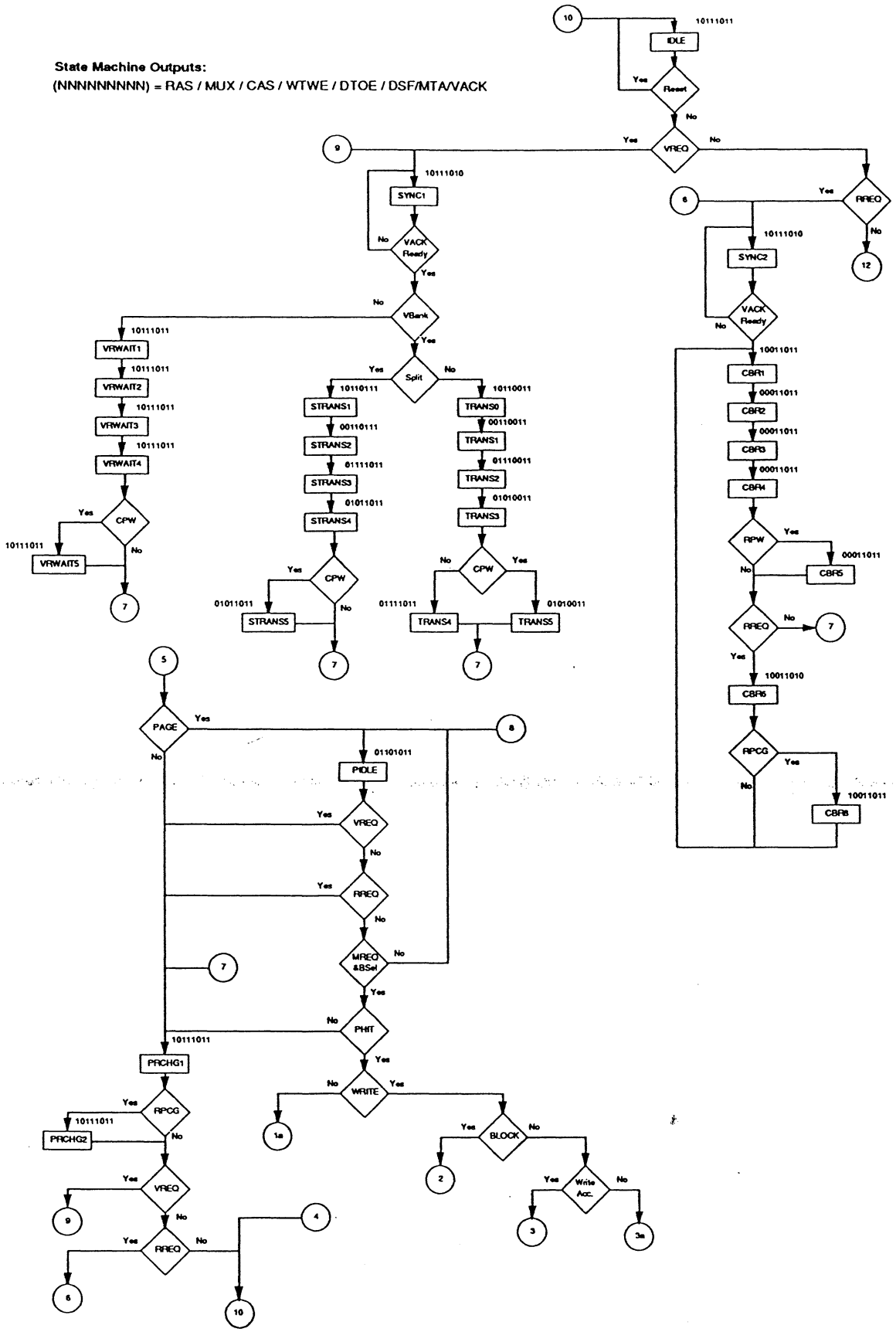


FIGURE 50a. VRAM CONTROLLER STATE MACHINE DIAGRAM

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 63 OF 98

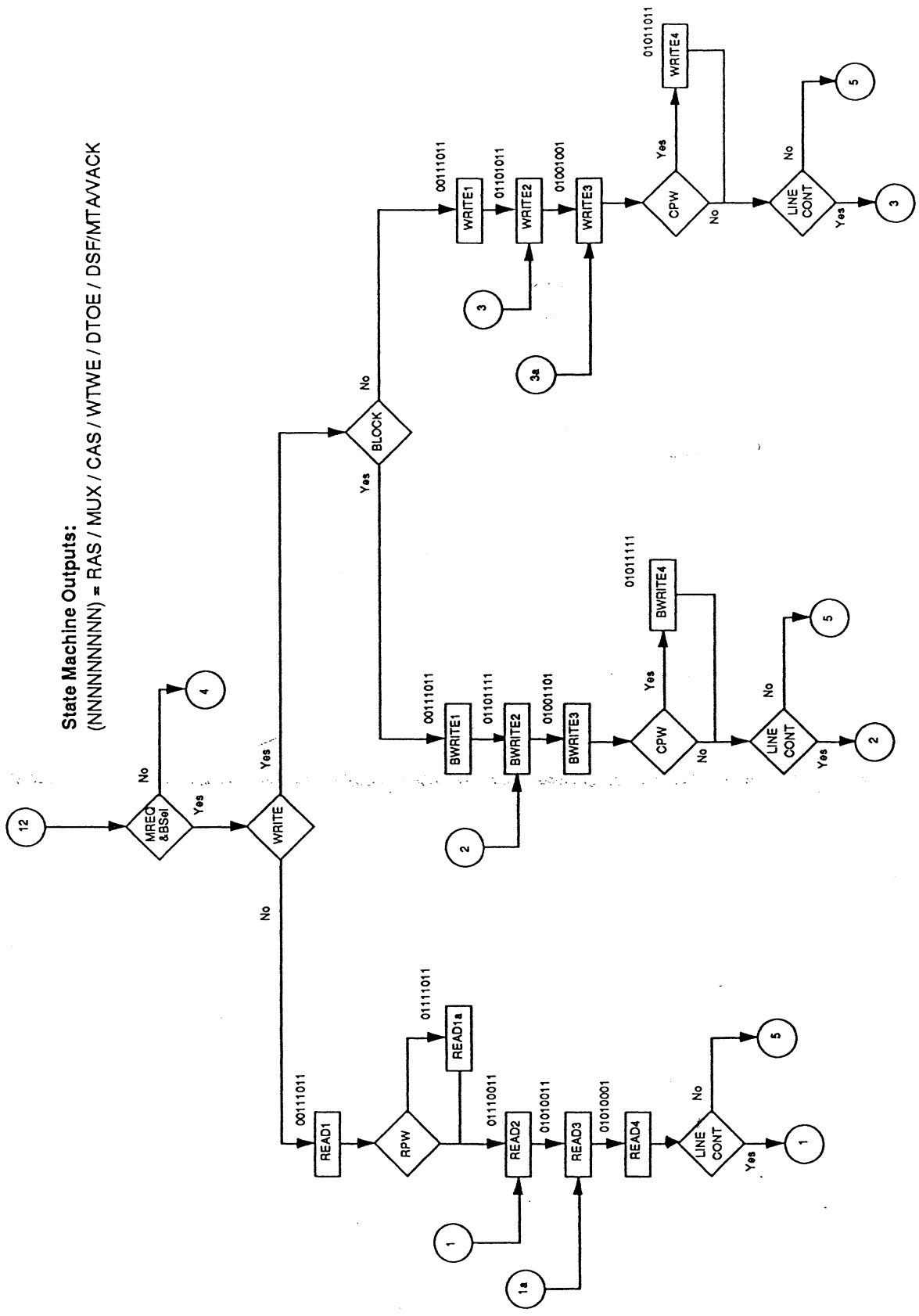


FIGURE 50b. VRAM CONTROLLER STATE MACHINE DIAGRAM

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 64 OF 98

- If the request (VREQ) is for a SAM read transfer cycle, then the state machine asserts an acknowledge signal (VACK) and enters a waiting state until all 4 state machines have synchronized (all banks perform read transfer cycles in tandem). Once synchronization has occurred, and if the bank is enabled (VBANK = 1), then either a full SAM read transfer or a split SAM read transfer cycle is performed based on the SPLITXFER input state. An extra wait state will be inserted if the 'extra $\overline{CAS}$ pulse width' configuration bit is set. If the bank is not enabled, it runs through a series of 'dummy' states which parallel the actual read transfer cycle of other banks in order to prevent the unselected bank from responding to an incoming memory cycle request while other banks are performing read transfer cycles.

- If the request (RREQ) is for a VRAM refresh cycle, then the state machine asserts an acknowledge signal (VACK) and enters a waiting state until all 4 state machines have synchronized (all banks perform refresh cycles together). Once synchronization has occurred, a $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle is performed. If RREQ is still asserted at the end of the refresh, then $\overline{CAS}$ is left low and another CBR cycle is performed. Extra wait states will be added if the 'extra $\overline{RAS}$ pulse width' and/or 'extra $\overline{RAS}$ precharge width' configuration bits are set.

- If the request is for a memory read cycle (MREQ, R/W = 'read', and the bank is selected) then a read cycle is performed. Following the first read cycle a check is made to see if the cycle is a line operation. If so, then an additional 3 read cycles are performed without raising $\overline{RAS}$. A line address generator supplies the 3 additional addresses needed for the line read. Once the cycle is finished, a check is made to see if page mode is active. If so, then the page-mode idle state is entered where $\overline{RAS}$ is held low. Otherwise the regular idle state is entered after one or more $\overline{RAS}$ precharge states.

- If the request is for a memory write cycle (MREQ, R/W = 'write', block write is false, and the bank is selected) then a write cycle is performed. Following the first write cycle a check is made to see if the cycle is a line operation. If so, then an additional 3 write cycles are performed without raising $\overline{RAS}$. A line address generator supplies the 3 additional addresses needed for the line write. Once the cycle is finished, a check is made to see if page mode is active. If so, then the page-mode idle state is entered where $\overline{RAS}$ is held low. Otherwise the regular 'idle' state is entered after one or more $\overline{RAS}$ precharge states. If the 'extra $\overline{CAS}$ pulse width' configuration bit is set, then one wait state will be added to the $\overline{CAS}$ pulse width.

- If the request is for a memory block write cycle (MREQ, R/W = 'write', block write is true, and the bank is selected) then a block write cycle is performed. Following the first block write cycle a check is made to see if the cycle is a line operation. If so, then an additional 3 block write cycles are performed without raising $\overline{RAS}$. A line address generator supplies the 3 additional addresses needed for the line block write. Once the cycle is finished, a check is made to see if page mode is active. If so, then the page-mode idle state is entered where $\overline{RAS}$ is held low. Otherwise the regular idle state is entered after one or more $\overline{RAS}$ precharge states. If the 'extra $\overline{CAS}$ pulse width' configuration bit is set, then one wait state will be added to the $\overline{CAS}$ pulse width.

If the state machine is idling in page mode and a SAM read transfer request, a refresh request, or a memory request to a different page occurs, then the state machine will perform one or more $\overline{RAS}$ precharge cycles. If the request is a memory request, then the idle state will be entered and the request will then be serviced. Otherwise (it's a SAM read transfer or refresh request), the request is serviced directly after the $\overline{RAS}$ precharge cycle(s) since the synchronization states satisfy the remainder of the $\overline{RAS}$ precharge requirement.

During all cycles but SAM read transfer cycles, the VRAM address is taken from the system address bus. During read transfer cycles the Video Refresh Timing Generator supplies the address. The VRAM controller keeps an internal 'read transfer in progress' register, and uses the address from the Video Refresh Timing Generator module when the register is set.

Each of the four state machines generates its own master $\overline{WE}$ signal for its respective bank. These signals are combined with the system bus SIZE control bits and the lower 2 address bits to generate the four actual $\overline{WE}$ signals for the VRAM byte lanes. The actual $\overline{WE}$ signals output to the VRAM banks are clocked on the falling edge of the bus clock in order to provide a stable $\overline{WE}$ signal for page mode write cycles ($\overline{CAS}$ falls on the rising edge of BCLK after a Transfer Start).

VRAM color register operations are specially handled. During a color register operation the state machine performs a 'normal' read or write cycle, but logic external to the state machine forces DSF to be asserted, thus causing the VRAMs to perform a color register operation instead of a normal read or write cycle.

6.3.7 Turbo SCSI Controller:

The Turbo SCSI module included in DAFB II interfaces a 68040-compatible bus to two 53C96[1] SCSI controller chips. Through the Turbo SCSI interface and 53C96 controllers, the 68040 system can communicate with two separate SCSI channels, each featuring SCSI-2 capabilities, including up to 10 MB/s[2] data rates on SCSI. Refer to Figure 51 to see how DAFB II interfaces to the 53C96 Channels.

The Turbo SCSI module acts exclusively as a slave to the 68040. The module interprets 68040 bus cycles, and when it detects accesses to the 53C96 chips, it outputs the appropriate control signals to the 53C96 chip accessed and acknowledges the completion of the cycle to the 68040. Turbo SCSI supports four kinds of accesses to the 53C96 chips: Register Write, Register Read, Pseudo DMA Write, and Pseudo DMA Read.

Turbo SCSI's two 53C96 interfaces have the same capabilities. Both have identical status/ configuration registers, and a single state machine controls both interfaces.

6.3.7.1 Turbo SCSI Address Space:

Turbo SCSI Channel 0's address space (for access to the Channel 0 53C96) is h50X0F000-h50X0F3FF. The address of the Status/Configuration Register for Channel 0 is hF9800024. Turbo SCSI Channel 1's address space (for access to the Channel 1 53C96) is h50X0F400-h50X0F7FF. The address of the Status/Configuration Register for Channel 1 is hF9800028. Address bits decoded for access to the 53C96 channels are A(31-24,17-10,8). A(10) selects which channel is being accessed (1 = Channel 1, 0 = Channel 0) and A(8) selects Pseudo DMA or Register Access (1 = Pseudo DMA Access, 0 = Register Access).

Because DAFB II passes A(7-4) to BA(7-4), which goes to the 53C96s' A(3-0) bits, 53C96 register access addresses appear at the second nibble. For example, to access Register 8 of a 53C96 on Channel 0, the address that should be put on the 68040 bus is h50X0F080.

[1] NCR's 53C96 is also marketed by Emulex (Emulex is actually the original designer) under the name ESP236. The Turbo SCSI interface is quite configurable, and therefore, is capable of controlling all of the following chips in the 53C9x family: 53C90A, 53C90B, 53C94, 53C95, 53C96. For Emulex parts, we support the ESP200, ESP216, ESP226, ESP236, FAS200, FAS216, FAS226, FAS236. Refer to the individual specifications for the above chips for more information on their respective features.

[2] 10MB/s data rates on SCSI are only capable if the FAS236 chip is utilized. 53C96 chips are capable of 5MB/s SCSI data rates.

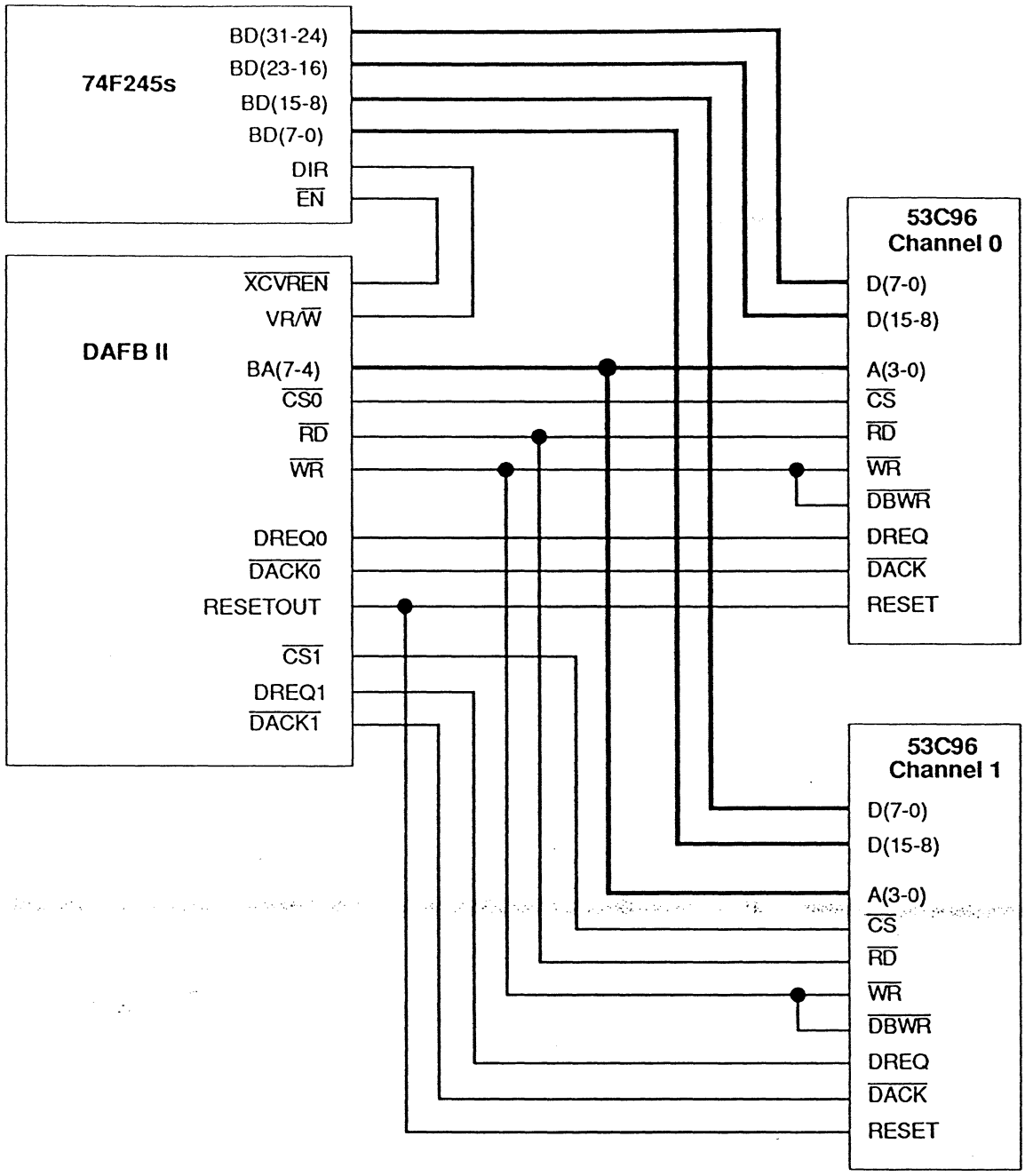


FIGURE 51. DAFB II TURBO SCSI INTERFACE TO 2 53C96 SCSI CHANNELS

To make data bus loading even on the BD(31-0) bus, it is recommended to attach the 53C96 Channels to different byte lanes. Because of this arrangement and the 68040's lack of dynamic bus sizing capabilities, an access to Channel 1 must have an address offset of 2 to put data on the correct byte lanes. For example, to access Register 8 of a 53C96 on Channel 1, the address that should be put on the 68040 bus is h50X0F482.

In the Blue O/S, a duplicate address space is created for the Turbo SCSI Channels to allow for non-serialized 68040 access to the channels. This space is h50F4F000 -h50F4F3FF for Channel 0 and h50F4F400 -h50F4F7FF for Channel 1. It is only recommended to use the higher performance non-serialized pages for Pseudo DMA accesses. Caution should be exercised when switching from serialized to non-serialized access to ensure that all serialized accesses complete

before the non-serialized cycles begin. To guarantee correct execution, code streams must be examined with the 040 pipeline in mind. One way of ensuring that all serialized accesses have completed before accessing a non-serialized page is to insert a NOP in the code right before accessing a non-serialized address. This forces all serialized accesses issued beforehand to complete in the correct order.

6.3.7.2 53C96 Register Accesses:

53C96 registers are accessed when Turbo SCSI decodes the 68040 address to be channel 0 or channel 1 register space. Register Writes are performed when the 68040 writes to Channel 0 or Channel 1 register space. Outputs asserted for Register Writes are $\overline{WR}$ and $\overline{CS0}$ or $\overline{CS1}$. Register Reads are performed when the 68040 reads from Channel 0 or Channel 1 register space. Outputs asserted for Register Reads are $\overline{RD}$ and $\overline{CS0}$ or $\overline{CS1}$. All 53C96 registers are 8-bit wide. Because of the 68040's lack of dynamic bus sizing, it is recommended that all accesses to these registers be byte (i.e. MOVE.B) accesses. Results are unpredictable otherwise.

6.3.7.3 53C96 Pseudo DMA Accesses:

The 53C96 chips provide a 16-bit DMA handshaking capability which is exploited by the Turbo SCSI interface through Pseudo DMA accesses. The full DMA capability of the 53C96 chips is utilized, but it is done through direct processor control—therefore the name Pseudo DMA. Pseudo DMA Writes are performed when the 68040 writes to Channel 0 or Channel 1 pseudo dma space and the accessed channel's DREQ pin is asserted . Outputs asserted for Pseudo DMA Writes are $\overline{WR}$ and $\overline{DACK1}$ or $\overline{DACK1}$. Pseudo DMA Reads are performed when the 68040 reads from Channel 0 or Channel 1 pseudo dma space. Outputs asserted for Pseudo DMA Reads are $\overline{DACK1}$ or $\overline{DACK1}$ (The $\overline{WR}$ pin is used as a R/W line for Pseudo DMA accesses, and is therefore deasserted during Pseudo DMA Reads). Because of the 68040's lack of dynamic bus sizing, it is recommended that all accesses to pseudo dma space be word (i.e. MOVE.W) accesses. Results are unpredictable otherwise.

6.3.7.4 Turbo SCSI Status/Configuration Registers:

Status/Configuration registers are provided for both channels. Bit 9 is the read-only DREQ status bit. It reflects the live state of DAFB II's DREQ0 (Channel 0) or DREQ1 (Channel 1) input. Because of the Pseudo DMA interface, it was deemed helpful to include this status bit, though the state of the bit should be completely predictable based on the state of the 53C96 chip. (The status of the DREQ line is not readable through a regular 53C96 register).

The remaining bits of the Status/Configuration registers are state machine configuration bits. These bits are all read/write, and though they may be changed dynamically, they are intended to be written at startup to setup the state machine for optimal control of each channel. This control is provided to allow the interface of either channel to take advantage of increased performance of future revisions of the 53C96 (FAS236) chip. The default settings for the configuration bits is for the slowest possible interface. Therefore, no programming of these registers is required (a chip can always be accessed more slowly than it's fastest rated speed!), though performance will be enhanced by matching the interface to the 53C96 chip capability. Listed below are the default and recommended settings for the configuration bits.

The default settings (loaded at system reset) for Turbo SCSI's State Machine is:
b111010001 = h1D1

This translates into:
Pseudo DMA Write Dreq Check enabled (bit 8 = 1),
Pseudo DMA Read Dreq Check enabled (bit 7 = 1),
Register Access Chip Select Deassertion Pulse Width Check enabled(bit 6 = 1),
5-clock Pseudo DMA Write access (bits 5-4 = b01),
4-clock Pseudo DMA Read access (bit 3 = 0),
4-clock Register Write access (bit 2 = 0),
6-clock Register Read access (bits 1-0 = b01).

The recommended settings for an Eclipse or Spike system running at 25 MHz with a 53C96 is:
b111101100 = h1EC (MOVE.L #$1EC, (A0)).

This translates into:
Pseudo DMA Write Dreq Check enabled(bit 8 = 1),
Pseudo DMA Read Dreq Check enabled (bit 7 = 1),
Register Access Chip Select Deassertion Pulse Width Check enabled(bit 6 = 1),
3-clock Pseudo DMA Write access (bits 5-4 = b10),
3-clock Pseudo DMA Read access (bit 3 = 1),
3-clock Register Write access (bit 2 = 1),
5-clock Register Read access (bits 1-0 = b00).

The recommended settings for an Eclipse or Spike system running at 33 MHz with a 53C96 is:
b001000001 = h041 (MOVE.L #$041, (A0)).

This translates into:
Pseudo DMA Write Dreq Check disabled(bit 8 = 0),
Pseudo DMA Read Dreq Check disabled (bit 7 = 0),
Register Access Chip Select Deassertion Pulse Width Check enabled(bit 6 = 1),
4-clock Pseudo DMA Write access (bits 5-4 = b00),
4-clock Pseudo DMA Read access (bit 3 = 0),
4-clock Register Write access (bit 2 = 0),
6-clock Register Read access (bits 1-0 = b01).

6.3.7.5 Turbo SCSI State Machine:

The Turbo SCSI circuitry is based on a single state machine that is used for both channels. Outputs for each channel are derived from the states and decode information. $\overline{RD}$ and $\overline{WR}$ are the only outputs shared by both channels. Refer to Figure 52 to see how the states are traversed. Below are the logic equations and definitions of terms that define the state machine in Figure 52:

Input descriptions (Register Accesses):

rd40	040 R/W signal
decRGChx	Internal DAFB II signal-register space decode of channel x
s1_rg_Chx	Internal DAFB II signal-stall for 1 cycle to assure correct deassertion time of $\overline{CS0}$ or $\overline{CS1}$ (only valid on assertion of Status/Configuration bit 6—CS PW Check) for channel x
rgwr3_x	Status/Configuration bit 2—Reg Write 3 Clks
rgrd4_x	Status/Configuration bit 1—Reg Read 4 Clks
rgrd6_x	Status/Configuration bit 0—Reg Read 6 Clks

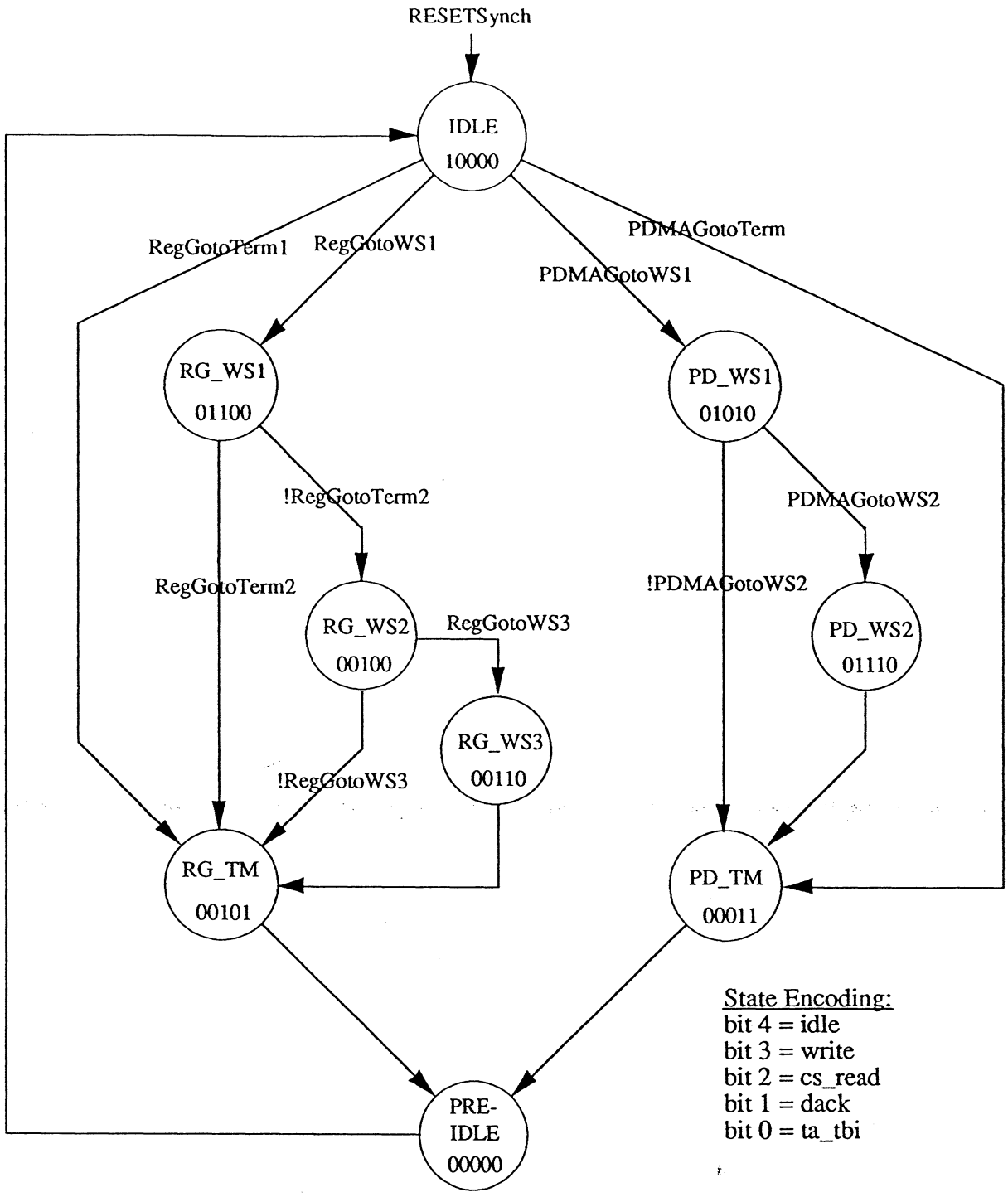


FIGURE 52. TURBO SCSI STATE MACHINE DIAGRAM

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Input descriptions (Pseudo DMA Accesses):

rd40	040 R/W signal
decPDChx	Internal DAFB II signal-pseudo DMA space decode of channel x
s1_pd_Chx	Internal DAFB II signal-stall for 1 cycle to assure correct recognition of synchronized dreq (only valid on assertion of Status/Configuration bit 8—DRQ Check Write on a Pseudo DMA Write cycle or on assertion of Status/Configuration bit 7—DRQ Check Read on a Pseudo DMA Read cycle) for channel x
dreqSyncx	Internal DAFB II signal-synchronized dreq for channel x
pdwr3_x	Status/Configuration bit 5—Ps DMA Write 3 Clks
pdwr5_x	Status/Configuration bit 4—Ps DMA Write 5 Clks
pdrd3_x	Status/Configuration bit 3—Ps DMA Read 3 Clks

State Machine Goto Terms Equations:

```
RegGotoTerm1    =   (!rd40 & rgwr3_0 & !/decRGCh0 & !s1_rg_Ch0)
                |   (!rd40 & rgwr3_1 & !/decRGCh1 & !s1_rg_Ch1);

RegGotoWS1      =   (!rd40 & !rgwr3_0 & !/decRGCh0 & !s1_rg_Ch0)
                |   (!rd40 & !rgwr3_1 & !/decRGCh1 & !s1_rg_Ch1)
                |   (rd40 & !/decRGCh0 & !s1_rg_Ch0)
                |   (rd40 & !/decRGCh1 & !s1_rg_Ch1);

RegGotoTerm2    =   !rd40
                |   (rd40 & !rgrd6_0 & rgrd4_0 & !/decRGCh0)
                |   (rd40 & !rgrd6_1 & rgrd4_1 & !/decRGCh1);

RegGotoWS3      =   (rgrd6_0 & !/decRGCh0)
                |   (rgrd6_1 & !/decRGCh1);

PDMAGotoTerm    =   (!rd40 & pdwr3_0 & !/decPDCh0 & dreqSync0 &
                    !s1_pd_Ch0)
                |   (!rd40 & pdwr3_1 & !/decPDCh1 & dreqSync1 &
                    !s1_pd_Ch1)
                |   (rd40 & pdrd3_0 & !/decPDCh0 & dreqSync0 &
                    !s1_pd_Ch0)
                |   (rd40 & pdrd3_1 & !/decPDCh1 & dreqSync1 &
                    !s1_pd_Ch1);

PDMAGotoWS1     =   (!rd40 & !pdwr3_0 & !/decPDCh0 & dreqSync0 &
                    !s1_pd_Ch0)
                |   (!rd40 & !pdwr3_1 & !/decPDCh1 & dreqSync1 &
                    !s1_pd_Ch1)
                |   (rd40 & !pdrd3_0 & !/decPDCh0 & dreqSync0 &


                    !s1_pd_Ch0)
                |   (rd40 & !pdrd3_1 & !/decPDCh1 & dreqSync1 &
                    !s1_pd_Ch1);

PDMAGotoWS2     =   (!rd40 & pdwr5_0 & !/decPDCh0)
                |   (!rd40 & pdwr5_1 & !/decPDCh1);
```

6.4 FRAME BUFFER MEMORY MAP: The frame buffer is mapped into the address space for NuBus slot 9. DAFB II will respond to all accesses in both slot space (F9000000 to F9FFFFFF) and super slot space (9000000 to 9FFFFFFF).

The memory map for a DAFB II-based frame buffer is shown in Figure 53. All valid frame buffer accesses occur in slot 9 space. There are no valid accesses in super slot 9 space, and accesses to that memory space will result in DAFB II asserting $\overline{TEA}$ to indicate an error condition for that bus access. Accesses to the unused portion of slot 9 space (F920 0000 to F97F FFFF, and F980 0400 to F9FF FFFF) also result in an error condition. Each of the separate addressing regions shown in Figure 53 are discussed in the following sections.

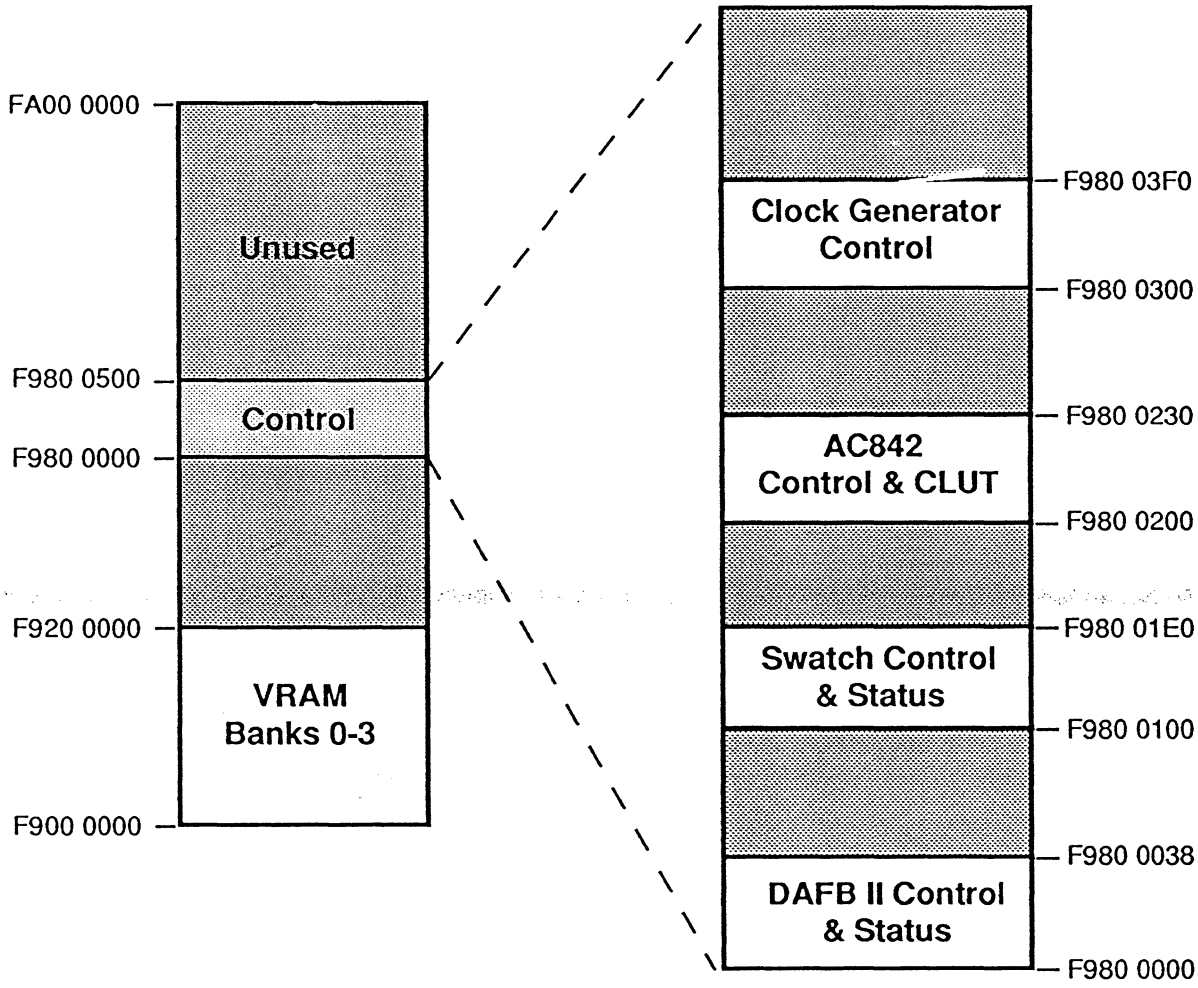


FIGURE 53. FRAME BUFFER MEMORY MAP

6.5 FRAME BUFFER VRAM: DAFB II supports frame buffers with 1, 2, or 4 banks of VRAM. Each bank contains 512K bytes of VRAM, and is organized as 128K by 32. A number of display resolutions are supported for each of the VRAM amounts, as shown earlier in Figure 47.

6.5.1 VRAM Addressing: A variety of VRAM bank addressing schemes are supported. The specific addressing scheme required depends on the specific display configuration chosen. The options are:

- *Linear addressing.* This is a simple contiguous linear addressing mode used for all configurations but those with 32 bpp or convolution. A maximum of 2 banks of VRAM are used, with bank 0 based at F9000000 and bank 1 directly following at F9080000.

- *Row/bank interleaved.* This addressing mode is used for display resolutions of 640 x 480 with 32 bpp (with or without convolution - see the following section on 1-8 bpp convolution addressing for a description of the convolution process). All four banks of VRAM are required for this mode. Memory is organized in rows, with each row being 1024 long words (or 1024 pixels, since each pixel is 32 bits) in length. Row 0 resides in bank 0, row 1 in bank 1, etc., with row N occurring in bank N modulo 4. This configuration is show in Figure 54. Row/bank interleaving can be used with fast page mode operation to increase the effective bandwidth into frame buffer memory for graphics operations such as scrolling and block moves. See Section 6.5.4 for a more complete description.

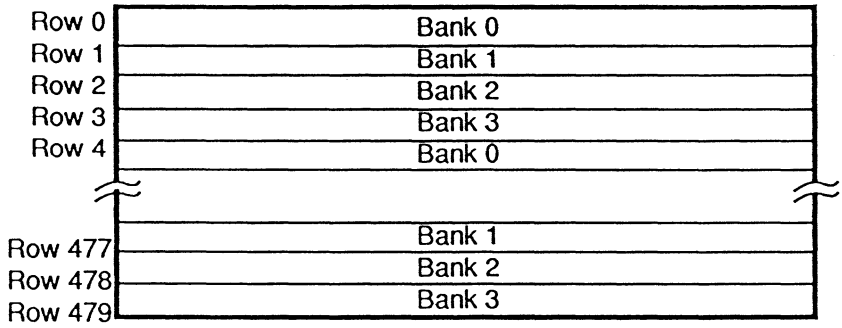


FIGURE 54. ROW/BANK INTERLEAVING

- *Word/bank interleaved.* This addressing mode is used for the 832 x 624 display resolution with 32 bpp, and for the 768 x 576 display resolution (PAL) with 32 bpp. All four banks of VRAM are required for this mode. Successive longwords in memory are located in alternating banks, with word N located in bank N modulo 2 for the first half the display, and located in bank (N modulo 2) + 2 for the second half of the display. This configuration is shown in Figure 55. Word/bank interleaving is required when data can not be clocked out of a single VRAM bank quickly enough (33 MHz typical limit on a single bank) to support the pixel data rate required by a particular configuration.

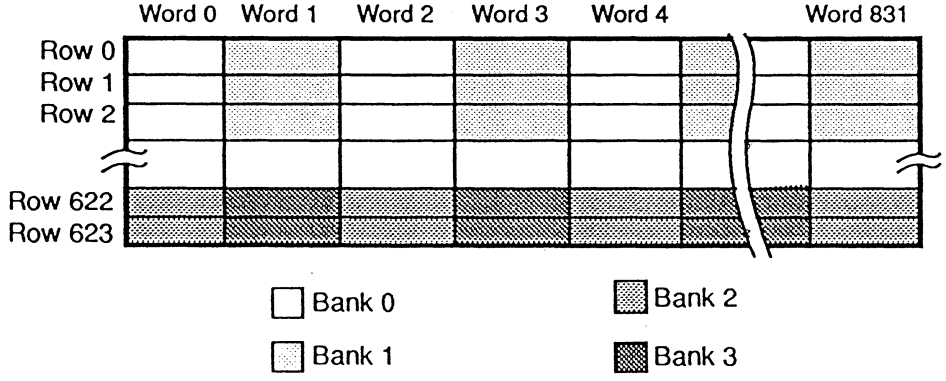
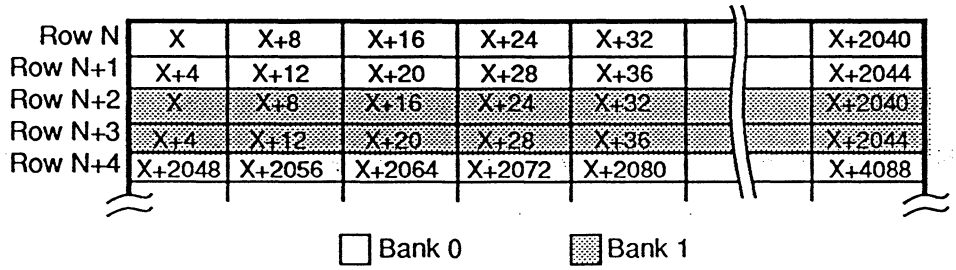


FIGURE 55. WORD/BANK INTERLEAVING

- *1-8 bpp convolution.* Convolution is a spatial filtering operation which is used to reduce flicker when using a DAFB II-based frame buffer to drive an interlaced monitor (e.g., NTSC or PAL timing). To produce the color or grey scale value for a given pixel, a weighted average is calculated from its 24-bit color value (after color table lookup) and the color values for the pixel above it and the pixel below it. The hardware which performs convolution is located in the CLUT/DAC. However, frame buffer pixel data must be presented to the AC842 CLUT/DAC in the proper order for convolution to work correctly. (i.e., first the pixel above the current pixel, then the pixel itself, and then the pixel below the current pixel. A fourth "dummy" pixel must also be sent to the CLUT/DAC.) When configured for 1-8 bpp convolution, DAFB II will send the correct sequence of pixel data words from frame buffer VRAM to the CLUT/DAC.

Two banks of VRAM are required to support convolution with 1-8 bpp. The memory addressing is organized such that four display lines are interleaved, with each line being 1024 bytes long. Even and odd numbered lines are interleaved on a long word basis, so that as the internal VRAM address is incremented for a bank, the first word will be from line N, followed by the first word from line N+1, followed by the second word from line N, and the second word from line N+1. (This is for internal frame buffer addressing only. The frame buffer VRAM appears "normal" to the 68040 processor due to address line interleaving hardware in DAFB II.) The two VRAM banks are interleaved such that the first bank contains line pairs that are odd and the second bank contains line pairs that are even. (See Figure 56.) This interleaving scheme allows the DAFB II video refresh hardware to access vertically adjacent pixels from four lines of the frame buffer memory in quick succession so they may be processed by the AC842 to produce a single (filtered) pixel.



X = Number of 1st longword in row N (bank 0)
or row N+2 (bank 1)

FIGURE 56. CONVOLUTION ADDRESSING

Note that VRAM addressing is transparent to the system once DAFB II has been configured. All VRAM appears as a single linear address space starting at the location specified by the 'Video Base Address' register (see section 6.6.1) and with an offset from one row to the next as specified by QuickDraw's 'rowBytes' parameter. Consequently, the programmer need not worry what particular addressing mode is actually in effect. The only exception to this is with color register loading/reading and block writes. See section 6.5.5 below for more information on block write and the VRAM color registers.

6.5.2 SAM Loading: DAFB II-supported frame buffer VRAM is dual ported – each bank includes a 256 x 32-bit serial access memory (or SAM - it functions much like a parallel-loaded shift register) used to clock pixel data out of the VRAM to be sent to the AC842. The SAM is loaded via a VRAM read transfer cycle which loads an entire VRAM row into the SAM. The frame buffer VRAM also features the capability to perform a split read transfer, which only loads one half of the SAM (i.e., 128 32-bit words). The split transfer capability eases timing requirements when reloads occur during the active display time.

DAFB II initiates a SAM read transfer at the beginning of every horizontal blanking interval (except during vertical blanking). With the exception of convolution, all VRAM banks perform a (split) read transfer cycle in parallel. For convolution modes, depending on the row and field numbers (convolution requires an interlaced display), two read transfer cycles may be performed to different VRAM banks. If the first data to be clocked out of the SAMs is located in the second half of the SAM (i.e., the VRAM QSF pin = 1), then a split read transfer is performed to load the first half of the SAM as soon as the active video line begins. One or more split transfers may also be performed during the remainder of the active line if it is required to keep the SAMs filled (i.e., whenever QSF toggles).

The address of the VRAM row loaded into the SAMs is determined by DAFB II based on the video base address, rowwords, interlace, row-interleave, and word-interleave registers, and internal video timing information such as vertical and horizontal blanking and row and field numbers. A new row address is calculated for each new horizontal line. The address is updated continuously in a 19-bit counter during the active video line time since a split SAM read transfer may be required.

6.5.3 VRAM Refresh: Since VRAM is dynamic memory, it must be refreshed periodically to retain its contents. A single refresh cycle refreshes the contents of a single row, and the entire VRAM must be refreshed once every 8 mS. Internally, each VRAM chip is organized as 512 rows of 256 columns, so 512 refreshes must be performed in 8 mS. DAFB II refreshes all VRAM banks in parallel, so only a single refresh cycle is needed to refresh all the frame buffer VRAMs. Also, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshes are performed, thus utilizing the VRAMs' internal refresh address counters. DAFB II performs VRAM refreshes at the start of each video horizontal blanking period, immediately after the SAM read transfer cycle(s) has been performed. During vertical blanking, when no SAM read transfer cycles are performed, refresh remains active and occurs at the beginning of each horizontal blanking period. The number of refresh cycles performed during each horizontal blanking period is dependent on the display resolution and timing, and is programmed via one of the DAFB II configuration registers (see the Frame Buffer Control Registers section).

Note: The SAMs are not dynamic memory, and therefore do not need to be refreshed.

6.5.4 Fast Page Mode: The frame buffer VRAM features a fast page mode for quickly accessing multiple column locations in the same VRAM row by performing multiple $\overline{\text{CAS}}$ cycles during a single active $\overline{\text{RAS}}$ cycle. In page mode, the initial VRAM access to a row occurs as a 'standard' VRAM access. However, at the end of the cycle, $\overline{\text{RAS}}$ remains active. As long as consecutive VRAM accesses are within the same row (rows consist of 256 long words) the VRAM access time is significantly reduced since only the column address need be supplied to the VRAM.

DAFB II provides support for fast page mode VRAM operation. Page mode is enabled or disabled simply by writing to a DAFB II register (see the Frame Buffer Control Registers section). After page mode has been enabled, all subsequent VRAM read/write operations will occur in page mode. Disabling page mode will cause the following VRAM operations to occur as 'standard' VRAM accesses. It should be noted that just as there is a performance increase for in-page 'hits', there is a performance penalty associated with each page 'miss' since $\overline{\text{RAS}}$ must be precharged before the next row access. However, since the DAFB II register operation to change page mode is relatively fast (only 3 clock cycles), page mode may be enabled/disabled on an operation by operation basis, thus allowing the VRAM to operated in the mode most efficient for the current graphics operation. For instance, drawing a vertical or steep line would result in consecutive accesses to different pages, so page mode should be left off to achieve best performance for this type of operation. However, an area fill would cause a number of consecu-

tive accesses to the same row, so turning on page mode for this type of operation should result in a performance increase.

DAFB II provides a special feature for the display resolution of 640 X 480 with 32 bpp. Since there must be 4 banks of VRAM to support this display resolution, and the banks are row-interleaved, each bank has its own page-hit logic. Thus each bank is operated (somewhat) independently of the others. This can benefit scrolling or moving operations which typically consist of a sequence of read and write cycles from different parts of frame buffer memory. In a non-interleaved memory structure these types of operations would cause continual page misses since consecutive reads and writes would be from different pages. However, with a 4-way row-interleaved memory structure, a scrolling or moving operation performs reads and writes within separate VRAM banks 3/4 of the time. And, since each bank(row) has its own page-hit logic, in-page hits would occur 3/4 of the time, resulting in significantly improved average performance for these memory bandwidth bound operations.

Table 12 indicates the number of clock cycles required from a system bus Transfer Start signal to read/write data from/to VRAM. Access times are shown for individual transactions (i.e., page mode off), in-page hits, and in-page misses. Both 25 MHz and 33 MHz clock speed options are shown. (33 MHz cycle times assume only the 'write access' wait state is active.)

TABLE 12. VRAM ACCESS TIMING

25 MHz Operation

Operation Type	Single Read	Single Write	Burst Read	Burst Write
isolated transaction (RAS precharged)	6	5	6,3,3,3	5,2,2,2
in-page miss (2 clock cycle penalty)	8	7	8,3,3,3	7,2,2,2
in-page hit	4	3	4,3,3,3	3,2,2,2

33 MHz Operation

Operation Type	Single Read	Single Write	Burst Read	Burst Write
isolated transaction (RAS precharged)	6	5	6,3,3,3	5,2,2,2
in-page miss (3 clock cycle penalty)	8	7	8,3,3,3	7,2,2,2
in-page hit	4	4	4,3,3,3	3,2,2,2

6.5.5 Block Write: DAFB II supports the Block Write (BW) feature found in the current generation of 1 Mbit VRAMs. The BW operation is capable of writing to 4 adjacent longwords in the frame buffer during the period normally used for writing to a single location, and is thus very useful for quick area fills. The data written to each of the 4 longwords is identical, and is taken from a "color register" located within the VRAM.

The VRAM color register is 32 bits wide. There is a separate color register for each of the 4 VRAM banks. A color register is loaded by writing to a special address (one for each of the 4 banks) in the frame buffer control space (see the Frame Buffer Control Registers section below). The frame buffer controller translates this access into the proper VRAM memory cycle needed to load the color register. Once a color register is loaded, its value persists until overwritten. The value in the color register may also be read by performing a read operation to the same address used to write data to the register.

The address specified for a BW operation is aligned in hardware to a 4-longword boundary (i.e., the 2 lower address bits to the VRAM are dropped). This 'aligned' address is used to determine which block of 4 longwords is affected by the BW. It is possible to enable/disable the BW operation on an individual byte basis within the affected 4 longwords. Since the data written into the frame buffer memory locations is taken from the VRAM color register, the 32-bit data present on the system data bus can be used to specify which bytes are actually written to. 16 of the 32 data bits are used to specify which of the 16 bytes in the 4 longwords are to be written to. Data bit 8N + M (where N is the longword byte number [0 - 3] and M is the longword number [0 - 3]) controls the writing of byte N of longword N. If the bit is a 1, the contents of color register byte N are written to the corresponding frame buffer byte. If the bit is a 0, then writing is disabled. For example, if the data bus contains 00001110 00001110 00001110 00001110 B, and the frame buffer is configured as 32 bpp under 32 bit QuickDraw, then the 'upper' byte (i.e., byte 0), or alpha channel, of each 32-bit pixel will be unaffected by the BW operation, and the 'lower' 3 bytes of the color register will be written to each of the four affected pixels.

The effects of this byte-wise write enable can vary depending on the configuration of the frame buffer. Figures 57, 58, and 59 illustrate how a BW operation would work in each of 3 different configurations: 32 bpp, 8 bpp, and 1 bpp.

(Note: The VRAMs also provide the capability for a 'write mask' to enable/disable writing on a bit-by-bit basis for each of the 32 bits in a longword. The same mask is applied to all 4 longwords in a BW operation. Support for the write mask capability is not implemented in DAFB II.)

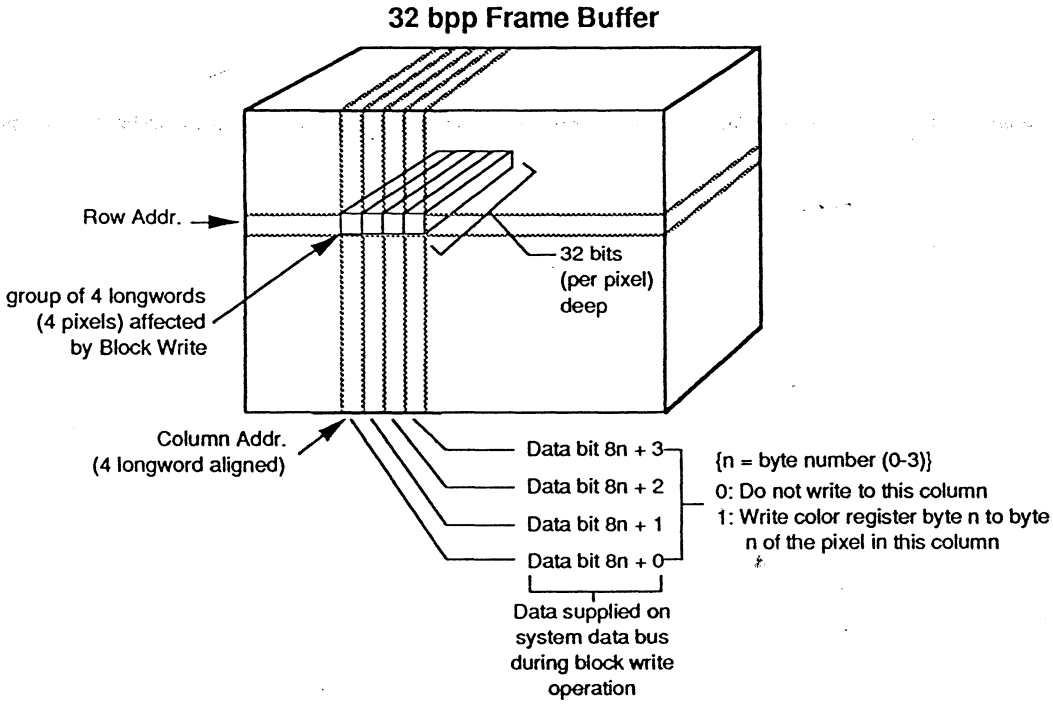


FIGURE 57. 32 BPP BLOCK WRITE

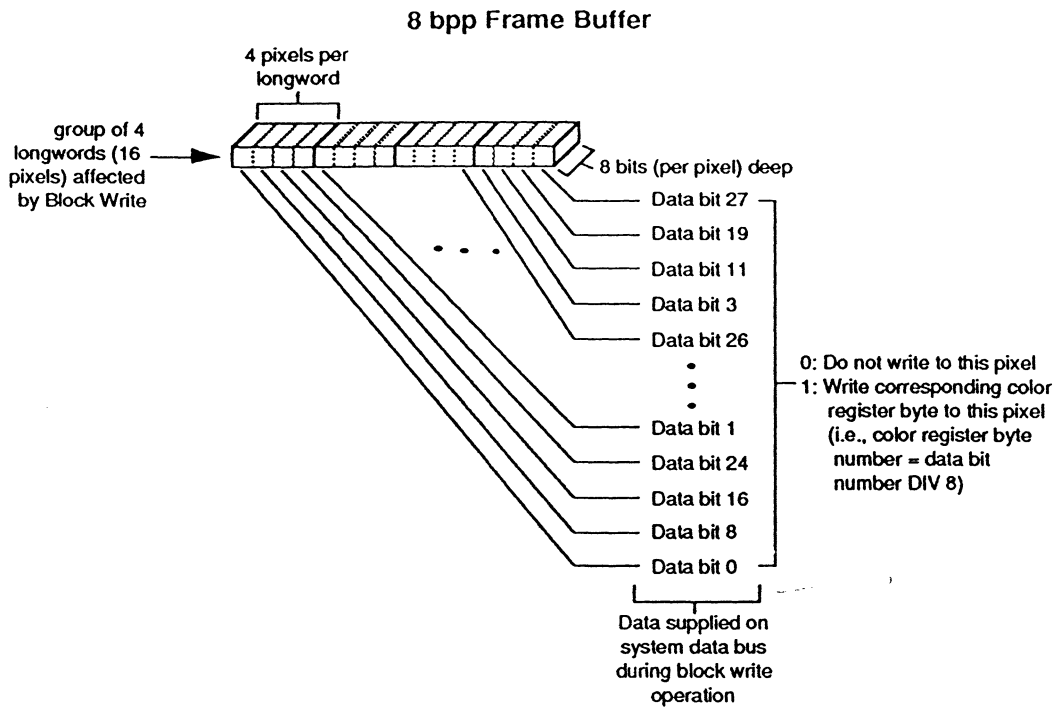


FIGURE 58. 8 BPP BLOCK WRITE

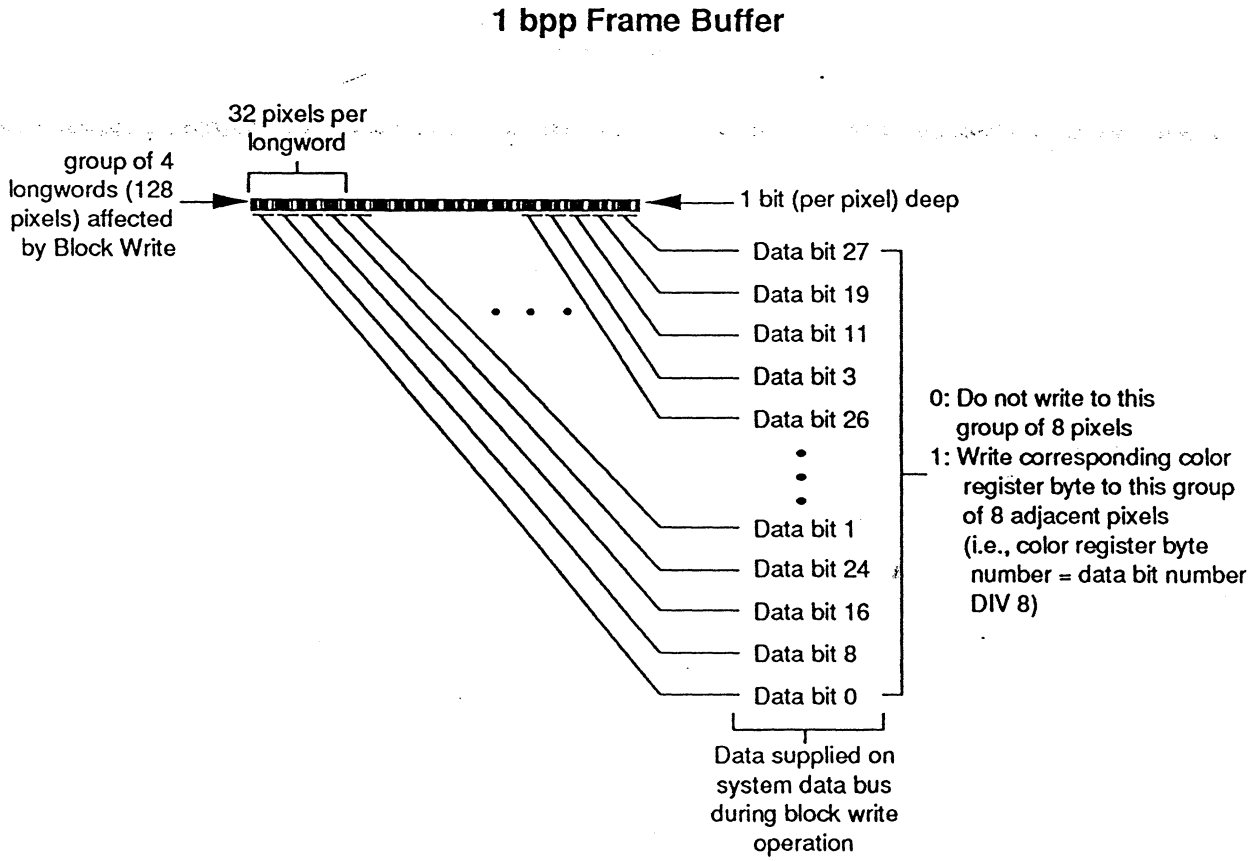


FIGURE 59. 1 BPP BLOCK WRITE

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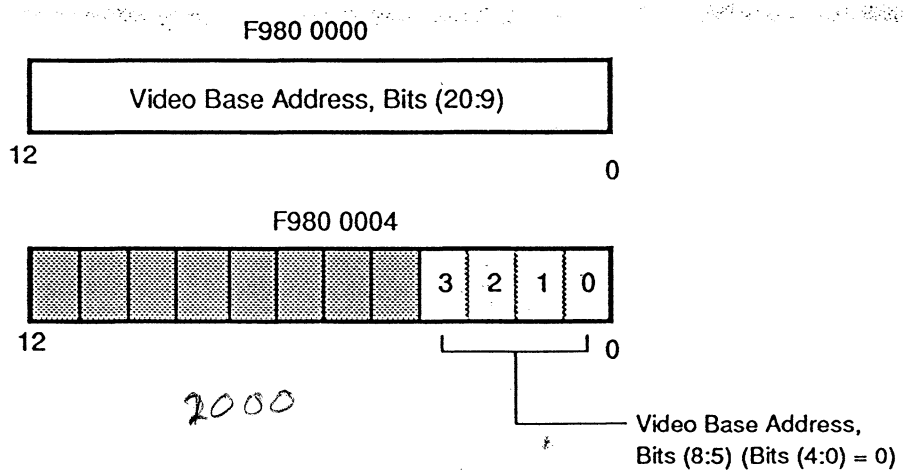
6.6 **FRAME BUFFER CONTROL REGISTERS:** As shown in Figure 53, the DAFB II frame buffer control space is divided into 4 segments:

- DAFB II configuration and status registers
- Swatch configuration and status registers
- AC842 configuration registers and CLUT
- Clock generator control registers

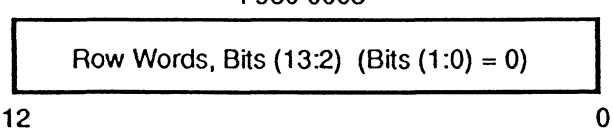
Note that although the Swatch video timing block registers are physically contained within DAFB II, they are assigned their own distinct address space. Three other control space segments are assigned to the frame buffer and SCSI chips external to DAFB II: the clock generator, the CLUT/DAC, and the SCSI chips. The Turbo SCSI external chip control registers are located in system I/O space, and are detailed in the NCR SCSI Controller chip specification (see section 6.8). Each of these five control space segments will be described in the following sections. (Note: all unused register bits are shown "grayed-out" in the following register diagrams. These bits may all be treated as "don't care".)

6.6.1 **DAFB II Configuration and Status Registers:** The DAFB II data bus is 12 bits wide and is resident on the 68040 system data bus bits 11:0. DAFB II registers range from 16 bits wide to 1 bit wide. The DAFB II configuration and status registers are shown below with a description of each register and its address.

Video Base Address Upper 16 bits of the 21 bits forming the base address of the video display. (The lower 5 bits are assumed to be zero.) Note that this is the lower 21 bits of the full 32-bit frame buffer address, so (for this register) the address of the first location in frame buffer VRAM is 0 (i.e, the lower 21 bits of F900 0000H are all zero). Since the video base address is over 12 bits long, it requires two of DAFB II's 12-bit registers. The first register contains bits 20:9, and the second register contains bits 8:5. The default video base address value is 0000H.



Row Words Bits 13:2 of the address offset to the next video scan line (Rowbytes/4). Default row words value is 000H.



Clock Configuration Multiple bit clock configuration register. This register contains a number of fields:

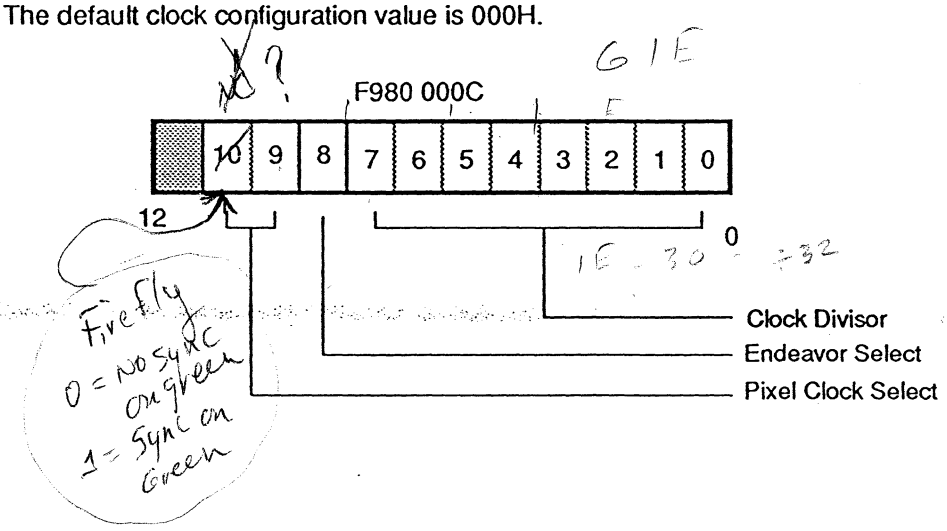
Clock Divisor: Divisor specifying the factor by which VIDCLK is divided down to generate the LD signal for the AC842. 255 = divide by 1, 0 = divide by 2, 1 = divide by 3, etc.

Endeavor Select: selects the Endeavor clock generator if 1, and the National DP8531 if 0.

Pixel Clock Select (1-0): Drives three external clock generator select lines for choosing between the 100 MHz oscillator, programmable clock generator (National DP8531 or Endeavor), or TTL-level PIXCLK input to DAFB II. (Since one of the external select lines is simply an inverted version of another, only two bits are required to specify the state of the lines.) The select line encoding is:

PIXSEL(1)	PIXSEL(0)	Selected Clock
0	0	PIXCLK (AC842 ECL clocks grounded)
1	0	100 MHz Oscillator
0	1	PIXCLK (AC842 ECL clocks grounded)
1	1	Programmable Clock Generator

The default clock configuration value is 000H.



DAFB II Configuration Multiple bit configuration register. This register contains a number of fields:

Word Interleave Enable: enables interleaving of the VRAM banks on a longword-by-longword basis. 1 = enabled, 0 = disabled. Should only be set when operating with 4 banks of VRAM.

Row Interleave Enable: enables interleaving of the VRAM banks on a row-by-row basis. 1 = enabled, 0 = disabled. Should only be set when operating with 4 banks of VRAM.

Interlace Enable: enables interlaced video. 1 = enabled, 0 = disabled. If interlace is enabled, RowWords should be set to twice the row words value that QuickDraw needs. Also, the active number of vertical half-lines must be odd.

Convolution Enable: enables convolution. 1 = enabled, 0 = disabled. Interlace must also be enabled if convolution is enabled. Convolution with requires 2 banks of VRAM.

Video Refresh Enable: enables video display refresh. 1 = enabled, 0 = disabled. If video refresh is disabled, sync and blank will still be generated and VRAM refreshes will occur, but no pixel data will be sent to the AC842.

Refresh Count: number of VRAM refresh cycles per horizontal retrace. 0 = 1 refresh cycle, 1 = 2 refresh cycles, etc.

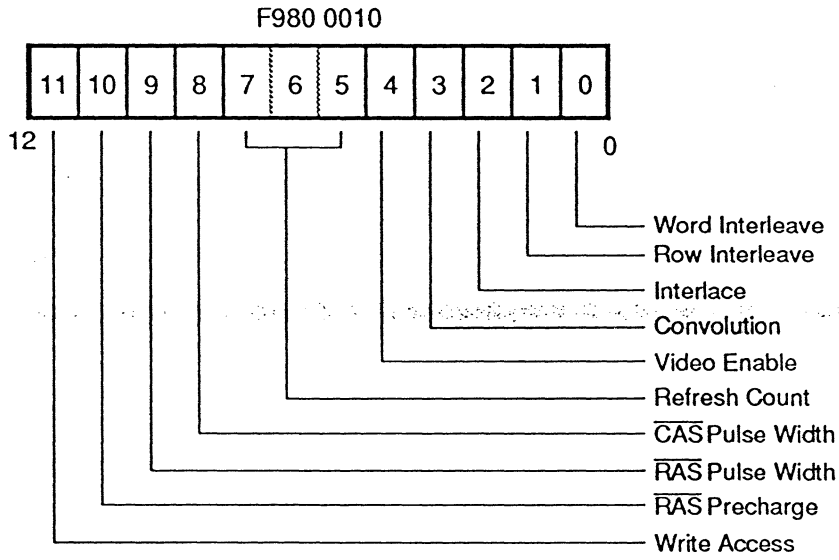
$\overline{CAS}$ Pulse Width: adds one extra clock cycle (i.e., a wait state) to the width of $\overline{CAS}$. 1 = enabled, 0 = disabled.

$\overline{RAS}$ Pulse Width: adds one extra clock cycle (i.e., a wait state) to the width of $\overline{RAS}$. 1 = enabled, 0 = disabled.

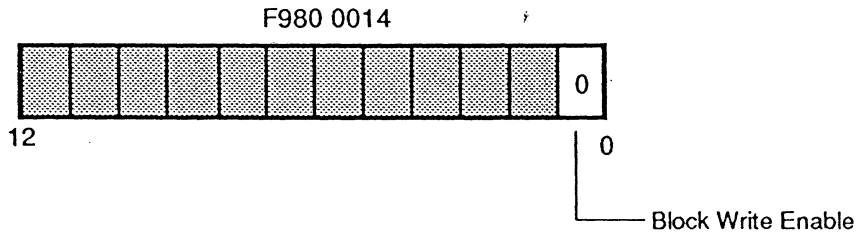
$\overline{RAS}$ Precharge: adds one extra clock cycle (i.e., a wait state) to the width of $\overline{RAS}$ precharge. 1 = enabled, 0 = disabled.

Write Access: adds one extra clock cycle (i.e., a wait state) to page mode write cycles. 1 = enabled, 0 = disabled.

Default DAFB II configuration value is F00H.



Block Write Enable This single bit register enables block write operations if 1, and enables 'standard' VRAM write operations if 0. Default block write enable value is 0.



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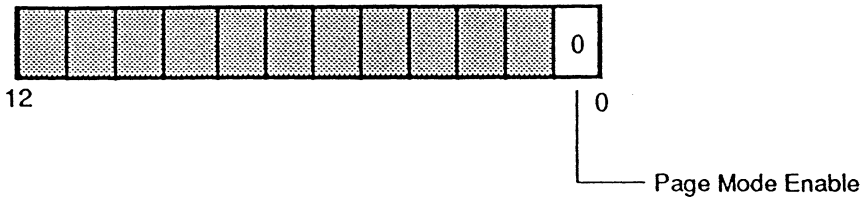
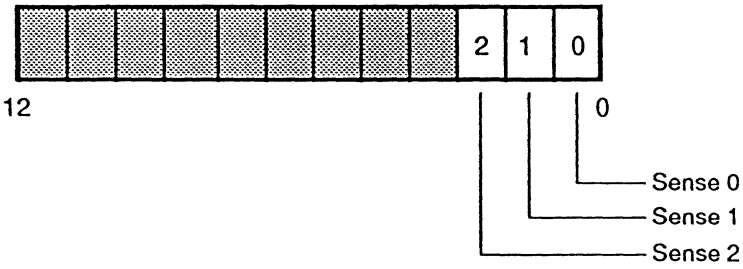
Page Mode Enable This single bit register enables fast page mode operations for VRAM if 1, and disables page mode 0. Default page mode enable value is 0.

F980 0018



Sense Lines Each of these 3 bits may be written to in order to drive or 3-state the 3 monitor sense lines, and may be read in order to determine the state of the lines. 0 = sense line driven, 1 = sense line hi-Z. The value driven onto the sense lines depends on the contents of the Test register (default of all zeros). The default value of the sense line register is 7H.

F980 001C



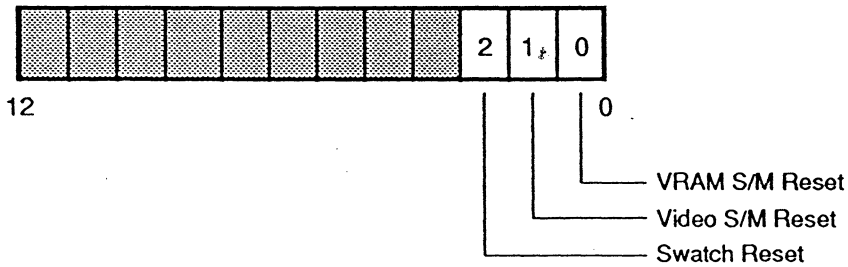
Reset Reset register. This register contains a number of fields:

VRAM State Machine Reset: resets the VRAM controller state machines to the idle state. 1 = reset, 0 = enabled.

Video Refresh State Machine Reset: resets the video refresh state machine to the idle state. 1 = reset, 0 = enabled.

Swatch Reset: resets the Swatch video timing generator . 1 = reset, 0 = enabled.

F980 0020



The default value of the reset register is 7H, i.e., all three reset lines are asserted. Each of the three sections of DAFB II controlled by this register must be explicitly taken out of reset by writing to this register in order for normal DAFB II operation to begin. The recommended startup procedure is to first program all other configuration registers (except the Swatch interrupt mask register which should only be written to after DAFB II is fully initialized) including the AC842 and clock generator registers, and then to release the three DAFB II sections from reset one at a time as follows:

- First, release Swatch from reset (i.e., write 3H to the reg.).
- Second, reassert the Swatch reset (7H).
- Third, again release Swatch from reset (3H).
- Fourth, release the VRAM state machines from reset (2H).
- Last, release the video refresh state machine (0H).

At least 4 of the selected video clock (PIXCLK or VIDCLK) periods should be allowed between successive writes to the reset register to assure that the change in the reset state has time to propagate through internal synchronization circuitry.

*** WARNING ***: If an access is made to VRAM (including color registers operations) while the VRAM controller is held in reset, DAFB II will 'hang' without returning a $\overline{TA}$ or $\overline{TEA}$.

Turbo SCSI Status/Config. 0 Turbo SCSI channel 0 configuration register. All register bits are read/write except for DREQ status, which is read only.

Reg Read 4 Clks Ch0/Reg Read 6 Clks Ch0: These two bits configure the state machine to allow Register Read Cycles for Channel 0 to be 4, 5 or 6 clocks. The settings are as follows:

Bit 1	Bit 0	# Cycles
1	0	4
0	0	5
X	1	6 (default)

Reg Write 3 Clks Ch0: This bit configures the state machine to allow Register Write Cycles for Channel 0 to be 3 or 4 clocks. The settings are as follows:

Bit 2	# Cycles
1	3
0	4 (default)

Ps DMA Read 3 Clks Ch0: This bit configures the state machine to allow Pseudo DMA Read Cycles for Channel 0 to be 3 or 4 clocks. The settings are as follows:

Bit 3	# Cycles
1	3
0	4 (default)

Ps DMA Write 3 Clks Ch0/Ps DMA Write 5 Clks Ch0: These two bits configure the state machine to allow Pseudo DMA Write Cycles for Channel 0 to be 3, 4 or 5 clocks. The settings are as follows:

Bit 5	Bit 4	# Cycles
1	0	3
0	0	4
X	1	5 (default)

CS PW Check Ch0: This bit, if asserted, configures the state machine to make sure that the CS deassertion pulse width is at least two clocks. If deasserted, the CS deassertion pulse width is at least one clock.

Bit 6	Meaning
1	Chip Select Deassertion Pulse Width at least 2 clocks (default)
0	Chip Select Deassertion Pulse Width at least 1 clock

DRQ Check Read Ch0: This bit, if asserted, configures the state machine to make sure that the DREQ deassertion synchronization delays on Pseudo DMA Reads to Channel 0 do not disrupt the next cycle. Whether or not to assert this bit is based on the version of the SCSI chip used and the number of clock cycles for a Pseudo DMA Read for Channel 0.

Bit 7	Meaning
1	DRQ Check on Read Enabled (default)
0	DRQ Check on Read Disabled

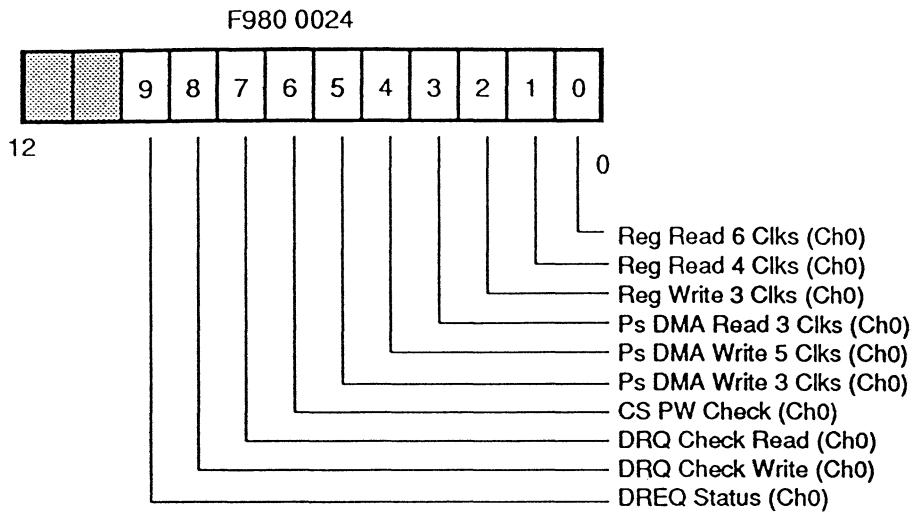
DRQ Check Write Ch0: This bit, if asserted, configures the state machine to make sure that the DREQ deassertion synchronization delays on Pseudo DMA Writes to Channel 0 do not disrupt the next cycle. Whether or not to assert this bit is based on the version of the SCSI chip used and the number of clock cycles for a Pseudo DMA Write for Channel 0.

Bit 8	Meaning
1	DRQ Check on Write Enabled (default)
0	DRQ Check on Write Disabled

DREQ Status Ch0: Read only (Writes do nothing). This bit reflects the live state of the DREQ signal on Channel 0. Because this bit is not readable in the 53C96, it is made available here.

Bit 9	Meaning
1	DREQ signal is asserted
0	DREQ signal is deasserted

The default Turbo SCSI channel 0 configuration value is 1D1H.



Turbo SCSI Status/Config. 1 Turbo SCSI channel 1 configuration register. All register bits are read/write except for DREQ status, which is read only.

Reg Read 4 Clks Ch1/Reg Read 6 Clks Ch1: These two bits configure the state machine to allow Register Read Cycles for Channel 1 to be 4, 5 or 6 clocks. The settings are as follows:

Bit 1	Bit 0	# Cycles
1	0	4
0	0	5
X	1	6 (default)

Reg Write 3 Clks Ch1: This bit configures the state machine to allow Register Write Cycles for Channel 1 to be 3 or 4 clocks. The settings are as follows:

Bit 2	# Cycles
1	3
0	4 (default)

Ps DMA Read 3 Clks Ch1: This bit configures the state machine to allow Pseudo DMA Read Cycles for Channel 1 to be 3 or 4 clocks. The settings are as follows:

Bit 3	# Cycles
1	3
0	4 (default)

Ps DMA Write 3 Clks Ch1/Ps DMA Write 5 Clks Ch1: These two bits configure the state machine to allow Pseudo DMA Write Cycles for Channel 1 to be 3, 4 or 5 clocks. The settings are as follows:

Bit 5	Bit 4	# Cycles
1	0	3
0	0	4
X	1	5 (default)

CS PW Check Ch1: This bit, if asserted, configures the state machine to make sure that the CS deassertion pulse width is at least two clocks. If deasserted, the CS deassertion pulse width is at least one clock.

Bit 6	Meaning
1	Chip Select Deassertion Pulse Width at least 2 clocks (default)
0	Chip Select Deassertion Pulse Width at least 1 clock

DRQ Check Read Ch1: This bit, if asserted, configures the state machine to make sure that the DREQ deassertion synchronization delays on Pseudo DMA Reads to Channel 1 do not disrupt the next cycle. Whether or not to assert this bit is based on the version of the SCSI chip used and the number of clock cycles for a Pseudo DMA Read for Channel 1.

Bit 7	Meaning
1	DRQ Check on Read Enabled (default)
0	DRQ Check on Read Disabled

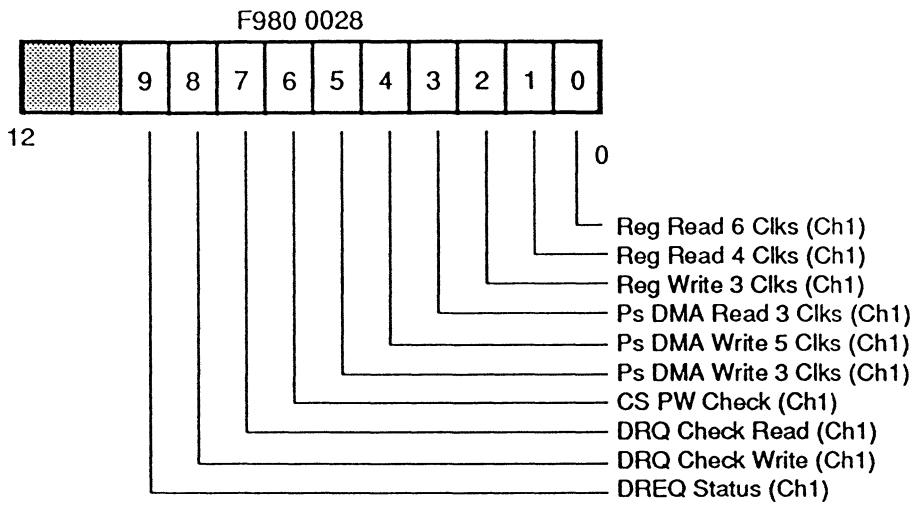
DRQ Check Write Ch1: This bit, if asserted, configures the state machine to make sure that the DREQ deassertion synchronization delays on Pseudo DMA Writes to Channel 1 do not disrupt the next cycle. Whether or not to assert this bit is based on the version of the SCSI chip used and the number of clock cycles for a Pseudo DMA Write for Channel 1.

Bit 8	Meaning
1	DRQ Check on Write Enabled (default)
0	DRQ Check on Write Disabled

DREQ Status Ch1: Read only (Writes do nothing). This bit reflects the live state of the DREQ signal on Channel 1. Because this bit is not readable in the 53C96, it is made available here.

Bit 9	Meaning
1	DREQ signal is asserted
0	DREQ signal is deasserted

The default Turbo SCSI channel 1 configuration value is 1D1H.



Test Register DAFB II Test register – for testing purposes only. This register contains a number of fields:

Sense Line Level: sets the level (high/low) that appears on the external sense lines when they are driven by DAFB II.

VBank Test Level: sets the level (high/low) on the four VBank lines between the Video Refresh block and the VRAM Controller block. Note: these levels may be overridden unless the VBank Test Enable bit is set to 1.

VBank Test Enable: disables the 'normal' VBank signals, thus enabling the VBank test signal. 1 = normal signals disabled, 0 = normal signals enabled.

XFER2 Test: when set to 1, asserts the XFER2 signal to the VRAM Controller block. This bit has no effect when set to 0.

SplitXFER Test: when set to 1, asserts the SplitXFER signal to the VRAM Controller block. This bit has no effect when set to 0.

RREQ Test: when set to 1, asserts the RREQ signal to the VRAM Controller block. This bit has no effect when set to 0.

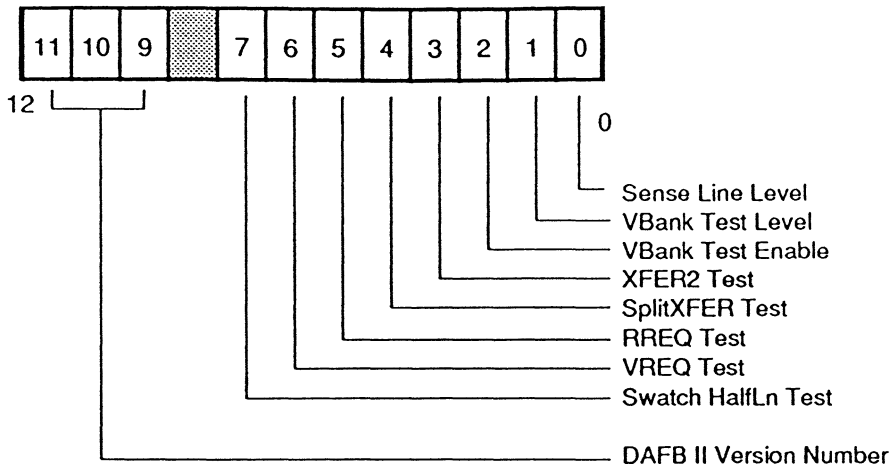
VREQ Test: when set to 1, asserts the VREQ signal to the VRAM Controller block. This bit has no effect when set to 0.

Swatch HalfLn Test: when set to 1, asserts the HalfLn signal from Swatch's horizontal timing block to Swatch's vertical timing block. This bit has no effect when set to 0.

DAFB II Version Number: version number of the DAFB II chip. These bits are read only.

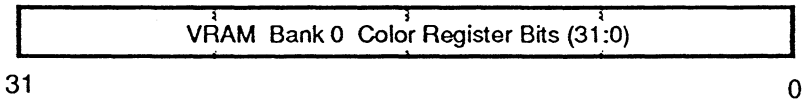
The default test register value is 200H.

F980 002C



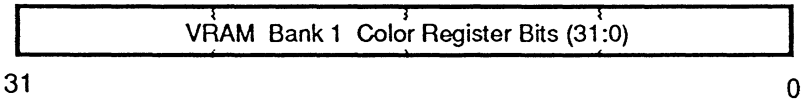
Color Register Bank 0 Performs a 32-bit color register operation to VRAM bank 0. There is no physical DAFB II register associated with this address. DAFB II translates an access to this address into the proper VRAM cycle for color register access.

F980 0030



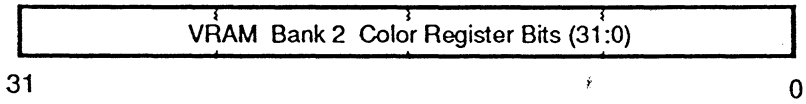
Color Register Bank 1 Performs a 32-bit color register operation to VRAM bank 1. There is no physical DAFB II register associated with this address. DAFB II translates an access to this address into the proper VRAM cycle for color register access.

F980 0034



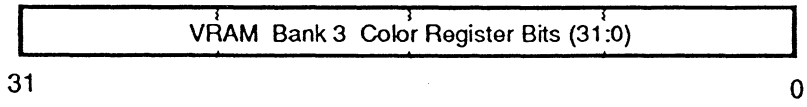
Color Register Bank 2 Performs a 32-bit color register operation to VRAM bank 2. There is no physical DAFB II register associated with this address. DAFB II translates an access to this address into the proper VRAM cycle for color register access.

F980 0038



Color Register Bank 3 Performs a 32-bit color register operation to VRAM bank 3. There is no physical DAFB II register associated with this address. DAFB II translates an access to this address into the proper VRAM cycle for color register access.

F980 003C



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6.6.2 Swatch Configuration and Status Registers: Swatch registers are written and read in the same manner as the DAFB II status and configuration registers. For more complete information on how Swatch register values affect video timing, consult the Swatch Specification, version 2.01, February 15, 1990.

6.6.2.1 General Swatch Registers

Swatch Mode Swatch configuration register. This register contains a number of fields:

Swatch Enable: enables Swatch operation. 0 = enabled, 1 = disabled. Swatch is completely halted if disabled.

VidLock Phase: sets the phase of the VIDCLK signal to which Swatch locks its timing generation. This configuration bit is only active when the PIXCLK input is used as the main DAFB II video clock.

Horizontal Active High: 1 = $\overline{\text{HSYNC}}$ active high, 0 = $\overline{\text{HSYNC}}$ active low. Does not affect $\overline{\text{CSYNC}}$ output.

Vertical Active High: 1 = $\overline{\text{VSYNC}}$ active high, 0 = $\overline{\text{VSYNC}}$ active low. Does not affect $\overline{\text{CSYNC}}$ output.

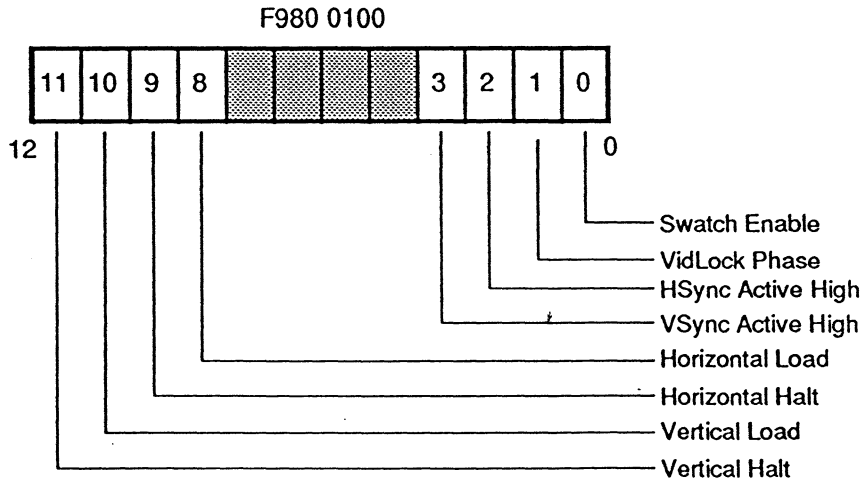
Horizontal Load: 0 = Load horizontal counter with CNTTEST - only used for test.

Horizontal Halt: 0 = Halt horizontal counter - only used for test.

Vertical Load: 0 = Load vertical counter with CNTTEST - only used for test.

Vertical Halt: 0 = Halt horizontal counter - only used for test.

The Swatch mode register defaults to all ones.



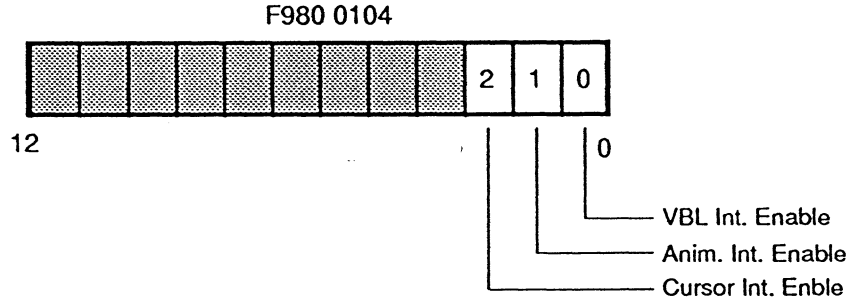
Interrupt Mask Interrupt mask register for Swatch interrupts.

VBL Interrupt Enable: 1 = vertical blanking interrupt enabled, 0 = VBL interrupt disabled.

Animation Interrupt Enable: 1 = animation line interrupt enabled, 0 = animation line interrupt disabled.

Cursor Interrupt Enable: 1 = cursor line interrupt enabled, 0 = cursor line interrupt disabled.

The interrupt mask register defaults to 0H (all interrupts disabled). Interrupts should not be enabled until DAFB II has been programmed and all DAFB II sections have been released from reset (see description of the reset register).

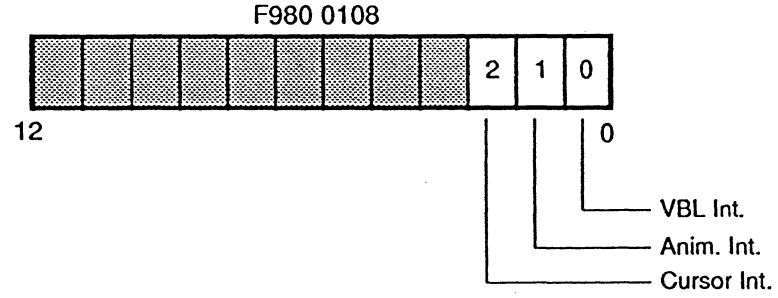


Interrupt Status Interrupt status register for Swatch interrupts (read only).

VBL Interrupt Status: 1 = vertical blanking interrupt asserted, 0 = VBL interrupt not asserted.

Animation Interrupt Status: 1 = animation line interrupt asserted, 0 = animation line interrupt not asserted.

Cursor Interrupt Status: 1 = cursor line interrupt asserted, 0 = cursor line interrupt not asserted.



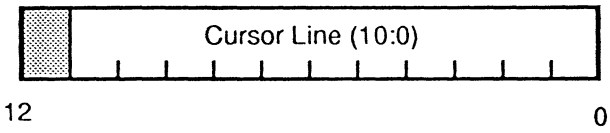
Clear Cursor Interrupt Access to this address (F980 010C) clears the cursor line interrupt source.

Clear Anim. Interrupt Access to this address (F980 0110) clears the animation line interrupt source.

Clear VBL Interrupt Access to this address (F980 0114) clears the vertical blanking interrupt source.

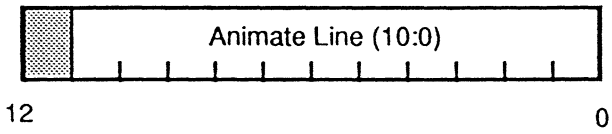
Cursor_Line This is the line of output video which will generate the cursor interrupt. It is specified in whole lines and is referenced from the vertical zero reference point, which is normally at the beginning of vertical sync. The cursor line register defaults to 000H.

F980 0118



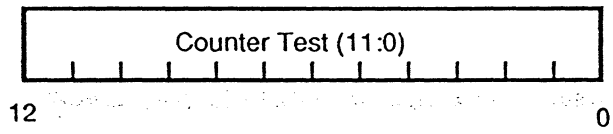
Animate Line This is the line of output video which will generate the animation interrupt. The first line of vertical blanking is counted as line number 0. The animate line register defaults to 000H.

F980 011C



Counter Test This value gets loaded into an internal Swatch counter when the appropriate load signal is asserted. Used for test purposes only. The counter test register defaults to 000H.

F980 0120



Timing Adjust Miscellaneous video timing adjustments. This register contains a number of fields:

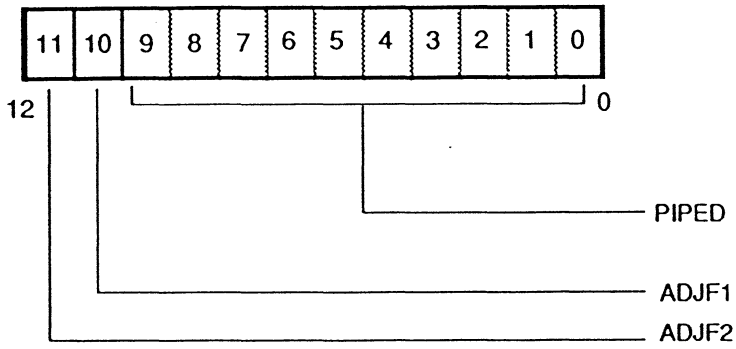
PIPED: Pipeline Delay. This parameter specifies the point in the horizontal timing at which pixel data from the VRAMs is started through the pixel data pipeline (VRAM to 'F399s to the AC842). It is equal to the number of pixel clocks from the horizontal zero reference point at which the pixel data pipeline is to be started.

ADJF1 and ADJF2: Half-line field adjustments. A special adjustment is available to suppress the half-lines that appear in interlaced modes. Interlaced displays typically end one field in the middle of a horizontal line and begin the next field in the middle of a horizontal line. For some applications it may be desirable for the active video to contain no half-lines. By using the ADJF1 and ADJF2 bits, the vertical active areas for field I and field II can include only full lines. ADJF1 (adjust field I) and ADJF2 (adjust field II) are used to increase the size of the front and back porches by one half-line from field I to field II, as shown in the following table:

ADJF2	ADJF1	Result
0	0	No adjustments necessary
1	0	Field II parameters are increased by 1
0	1	Field I parameters are increased by 1
1	1	not useful

The timing adjust register defaults to all zeros.

F980 0168



6.6.2.2 Swatch Horizontal Timing Registers: Swatch is composed of both horizontal and vertical timing generators. The horizontal timing generator is driven from either the PIXCLK or VIDCLK video clock input, whichever is selected as DAFB II's main video clock. Horizontal timing is specified by a number of parameters which control when transitions between different states in a horizontal line occur. These parameters and states are shown in Figure 60 below:

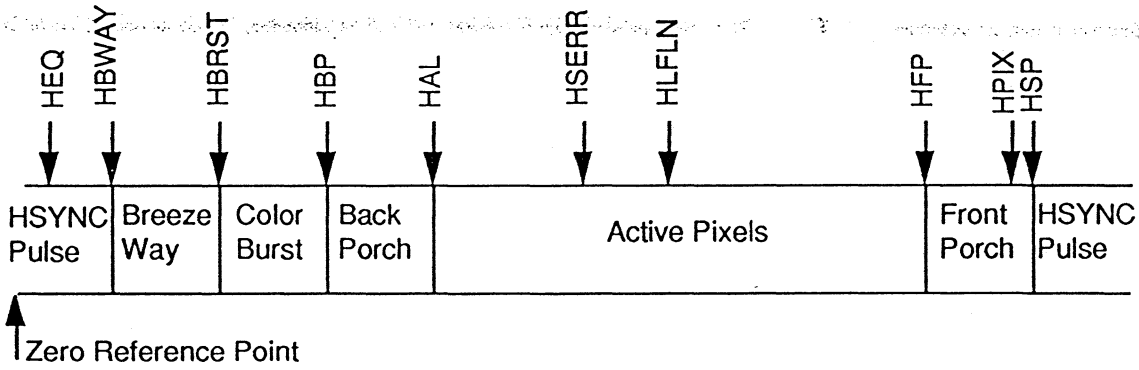
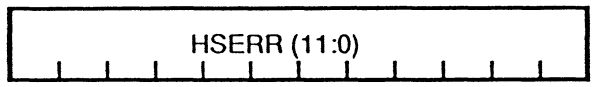


FIGURE 60. SWATCH HORIZONTAL TIMING STATES

All the Swatch horizontal parameters are specified as the number of clocks from a horizontal zero reference point (shown in the above figure). The zero reference point must be located within the horizontal sync period.

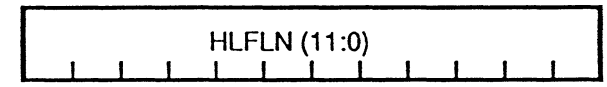
HSERR Where the serration pulse rises. Equal to the number of pixel clocks from the beginning of the horizontal sync period for the pulse in the first half of a line. Equal to the number of pixel clocks from the half line point for the pulse in the second half of a line. The HSERR register defaults to 000H.

F980 0124



HLFLN Half-line point where equalizing pulses or serrations fall. Equal to the number of pixel clocks from the horizontal zero reference point. The HLFLN register defaults to 000H.

F980 0128

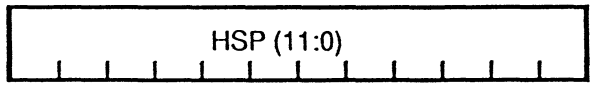


HEQ Horizontal equalizing pulse. Where an equalizing pulse would rise. Equal to the number of pixel clocks -1 from the beginning of the horizontal sync period for the pulse in the first half of a line. Equal to the number of pixel clocks - 1 from the half line point for the pulse in the second half of a line. The HEQ register defaults to 00H.

F980 012C

HSP Horizontal sync pulse. Where the horizontal front porch ends and the horizontal sync pulse begins. The only requirement for HSP programming is that the zero reference point be within the horizontal sync period, so HSP should be programmed to start before the zero reference point (i.e., at the end of the horizontal line). It is suggested that HSP be programmed to be one less than the number of clocks in a horizontal line. The HSP register defaults to 000H.

F980 0130

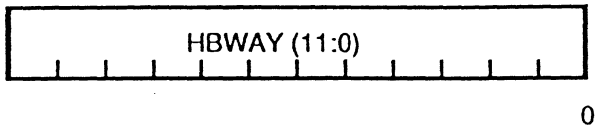


Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S0128-A
SCALE: NONE	SHT 93 OF 98

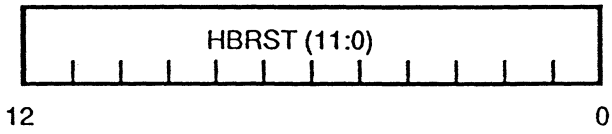
HBWAY Horizontal BreezeWay. Where the horizontal sync pulse ends. Equal to the number of pixel clocks -1 from the horizontal zero reference point. The HBWAY register defaults to 000H.

F980 0134



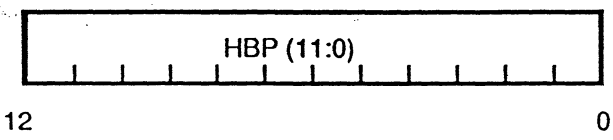
HBRST Horizontal Burst. Where the horizontal burst gate begins. Equal to the number of pixel clocks - 1 from the horizontal zero reference point. The HBRST register defaults to 000H.

F980 0138



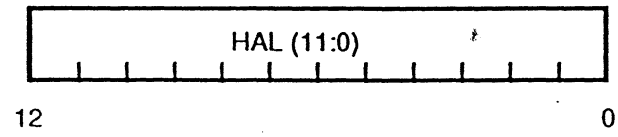
HBP Horizontal Back Porch. Where the horizontal burst gate pulse ends. Equal to the number of pixel clocks - 1 from the horizontal zero reference point. The HBP register defaults to 000H.

F980 013C

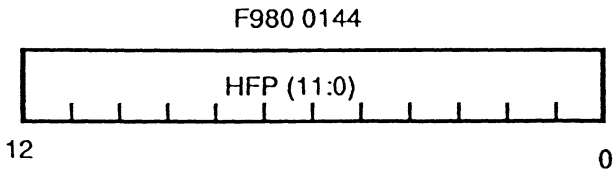


HAL Horizontal Active Line. Where the pixel data for a horizontal line begins. Equal to the number of pixel clocks -1 from the horizontal zero reference point. The HAL register defaults to 000H.

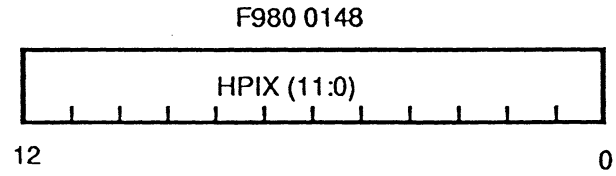
F980 0140



HFP Horizontal Front Porch. Where the pixel data for a horizontal line ends. Equal to the number of pixel clocks -1 from the horizontal zero reference point. The HFP register defaults to 000H.



HPIX Horizontal Pixels. HPIX is equal to the (total number of pixel clocks - 2) in a horizontal line. The HPIX register defaults to 000H.



6.6.2.3 Swatch Vertical Timing Registers: The vertical timing generator is driven from a clock which is only half the frequency of the horizontal timing generator clock. However, vertical state transitions can only occur at intervals of half a horizontal line (i.e., at the beginning and middle of a line). Vertical timing is specified by a number of parameters which control when transitions between different states in a video field occur. These parameters and states are shown in Figure 61 below:

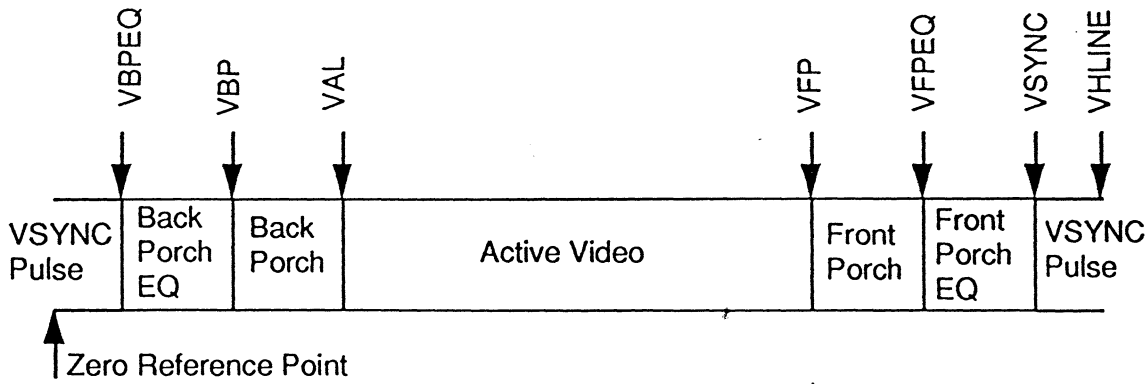
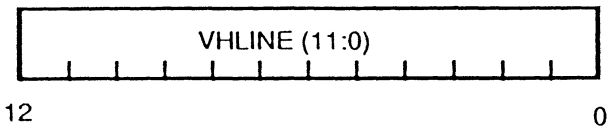


FIGURE 61. SWATCH VERTICAL TIMING STATES

All the Swatch vertical parameters are specified as the number of half-lines from a vertical zero reference point (shown in the above figure). The zero reference point is located within the vertical sync period.

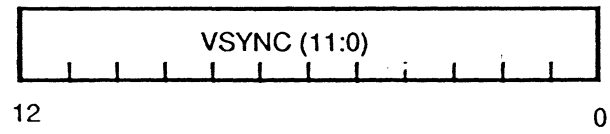
VHLINE Vertical Half Lines. The total number of half-lines in one field. VHLINE is odd for interlaced video and even for non-interlaced video. The VHLINE register defaults to 000H.

F980 014C



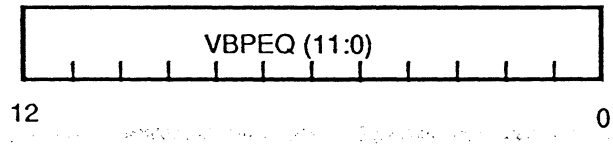
VSYNC Vertical Sync. Where the vertical sync pulse begins. For interlaced video it is VHLINE - 1. For non-interlaced video it is VHLINE - 2. The VSYNC register defaults to 000H.

F980 0150



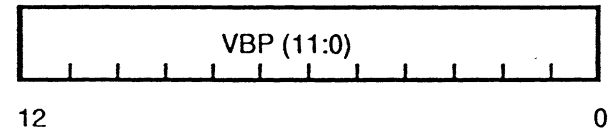
VBPEQ Vertical Back Porch Equalization. Where the vertical back porch with equalization pulses begins. Referenced from the vertical zero reference point. The VBPEQ register defaults to 000H.

F980 0154



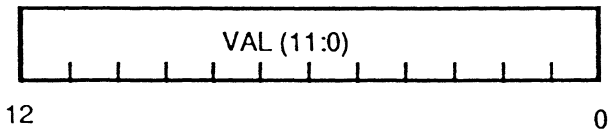
VBP Vertical Back Porch. Where the vertical back porch without equalization pulses begins. Referenced from the vertical zero reference point. The VBP register defaults to 000H.

F980 0158



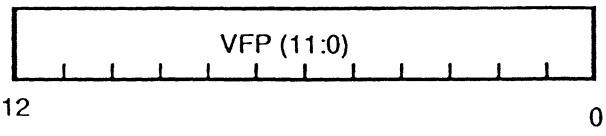
VAL Vertical Active Lines. Where the vertical active video area begins. Referenced from the vertical zero reference point. The VAL register defaults to 000H.

F980 015C



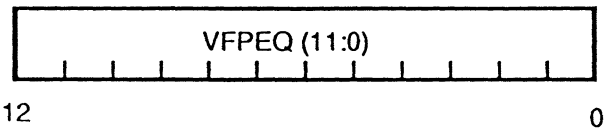
VFP Vertical Front Porch. Where the vertical front porch (without equalization pulses) begins. Referenced from the vertical zero reference point. The VFP register defaults to 000H.

F980 0160



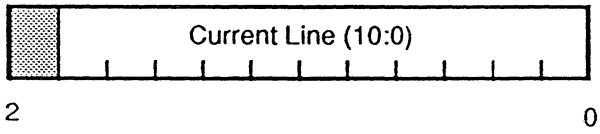
VFPEQ Vertical Front Porch Equalization. Where the vertical front porch with equalization pulses begins. Referenced from the vertical zero reference point. The VFPEQ register defaults to 000H.

F980 0164



Current Line Current active video line. This is a read only register which returns the number of the currently active scan line. Note that this is the number of whole lines, not half-lines. Since the video timing logic is asynchronous to the register logic, this register should be read successively until two consecutive read operations return the same line number.

F980 016C



6.6.3 AC842 Configuration Registers and CLUT: The AC842 CLUT/DAC is accessed at memory locations F980 0200 to F980 020C. However, DAFB II decodes the address range from F980 0200 to F980 02FF, and provides a chip select to the AC842 for any accesses within this range. Only address bits 5:4 are actually used by the CLUT/DAC for access to its internal registers and CLUT, and any combination of address bits 7:6 and 3:0 result in a chip select to the AC842. The AC842 has an 8 bit data bus which is located on bits 7:0 of the frame buffer data bus. Therefore, byte accesses to the CLUT/DAC must be aligned on byte 3 of the system data bus (i.e., address bits 1:0 must both be 1). For word or longword accesses, the upper data bus bytes are ignored. For further information on programming the AC842 CLUT/DAC see the Apple Computer AC842 CLUT/DAC Specification.

6.6.4 Clock Generator Control Registers: The DP8531 clock generator is accessed at memory locations F980 0300 to F980 033C. However, DAFB II decodes the address range from F980 0300 to F980 03FF, and provides a chip select to the clock generator for any accesses within this range. Only address bits 7:4 are actually used by the clock generator for access to its internal registers, and any combination of address bits 3:0 result in a chip select to the clock generator. The clock generator has a 4 bit data bus which is located on bits 3:0 of the frame buffer data bus. Therefore, byte accesses to the clock generator must be aligned on byte 3 of the system data bus (i.e., address bits 1:0 must both be 1). For byte-wide accesses, data bus bits 7:4 are ignored. For further information on programming the DP8531 clock generator, see the National Semiconductor DP8531/32/33 Programmable Clock Generator data sheet.

6.7 **DEVICE CHARACTERISTICS FOR EACH PIN:** Table 2 lists the I/O buffer configuration for every pin on the DAFB II ASIC.

6.8 **FURTHER READING:** Additional information relating to this design can be found in the following documents:

MC68040 32-Bit Microprocessor User's Manual, Motorola, 1990.

DP8531/32/33 Programmable Clock Generator Specification, National Semiconductor, 1989.

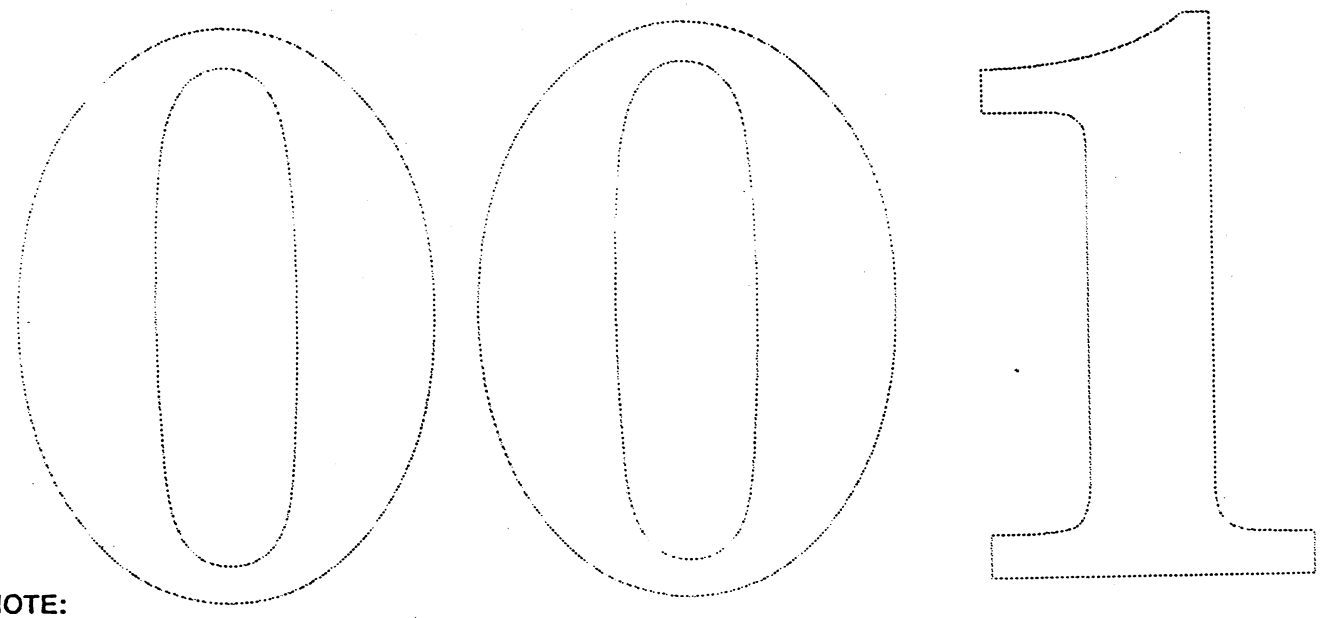
AC842 CLUT/DAC Specification, Apple Computer, 1990.

IC, VRAM, 128K X 8, 100ns, SRT, 40-PIN, SOJ, Apple Computer Drawing Number 333S0177-A, 1991.

Swatch Specification, Version 2.01, Apple Computer, 1990.

NCR 53C94, 53C95, 53C96 Advanced SCSI Controller, NCR, 1990.

REV.	ZONE	ECN#	REVISION	APPD	DATE
A			PRODUCTION RELEASE		



NOTE:
MANUFACTURERS RECEIVING APPLE APPROVED VENDOR STATUS FOR THEIR PRODUCT UNDER THIS PART NUMBER PLEASE NOTE: You must not change your part design, materials or manufacturing process from those used for the original samples submitted to and approved by Apple without written approval of Apple. Proposed changes determined by Apple to be significant, will require the manufacturer to submit new samples and/or data for review and approval prior to product shipments to Apple.

	METRIC				Apple Computer, Inc.
DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN BRACKETS [ ] ARE IN INCHES. TOLERANCES X.X ± 0.3 [.01] X.XX ± 0.13 [.005] X.XXX ± 0.03 [.001] ANGLEs ± 0.1 or as noted DO NOT SCALE DRAWING	DRAFT B.T. 8/21/91	DESIGN CK 8/21/91			NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: (i) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (ii) NOT TO REPRODUCE OR COPY IT (iii) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
	ENG APPD 4/24/91	MFG APPD //			
	QA APPD //	DESIGNER //			TITLE IC, ASIC, CLUT/DAC, AC/DC, AC843, 100 MHz, 68-PIN PLCC
	RELEASE //	SCALE: NONE			
	MATERIAL/FINISH NOTED AS APPLICABLE		SIZE A	DRAWING NUMBER 343S1075-01	SHT 1/33

1.0 SCOPE: This specifies the parametric requirements of a custom IC, AC843; 100 MHz CMOS CLUT/DAC in a 68-pin PLCC package.
Features include:

- 100 MHz Pipelined Operation in 1, 2, 4, 8 or 16 Bits Per Pixel (No Convolution)
- 60 MHz Pipelined Operation in Chunky Planar and 24 Bit Modes (No Convolution)
- 15 MHz Pipelined Operation Convolution Operation in 16-bit per Pixel Mode
- Software Selection of the Internal Pixel Clock
- Apple Convolution
- Scaled Pixel Clock TTL Output, VIDCLK, with 60 MHz range
- Chunky and 24 Bit TTL Pixel Ports
- Triple 8-bit D/A Converters
- 3 x 256 x 8 Dual Port Color Table
- RS-343A Compatible Outputs
- Standard MPU Interface

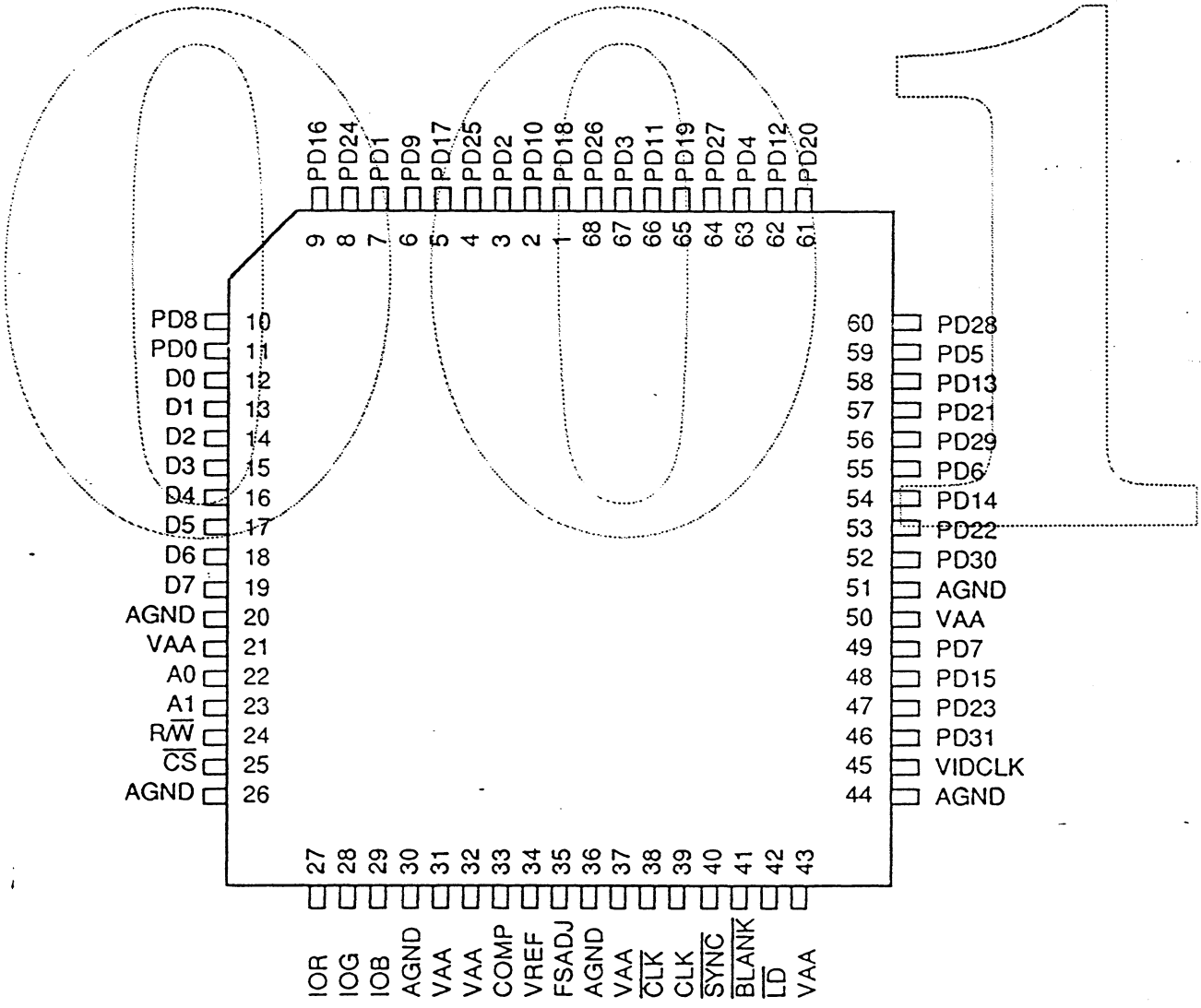


FIGURE 1. PIN CONFIGURATION

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S1075-01
SCALE: NONE	SHT 2 OF 33

TABLE 1. PIN IDENTIFICATION

PIN NO	PIN NAME	DESCRIPTION	TYPE
1	PD18	Pixel Data 18	Input
2	PD10	Pixel Data 10	Input
3	PD2	Pixel Data 2	Input
4	PD25	Pixel Data 25	Input
5	PD17	Pixel Data 17	Input
6	PD9	Pixel Data 9	Input
7	PD1	Pixel Data 1	Input
8	PD24	Pixel Data 24	Input
9	PD16	Pixel Data 16	Input
10	PD8	Pixel Data 8	Input
11	PD0	Pixel Data 0	Input
12	D0	Data Bus 0	Input/Output
13	D1	Data Bus 1	Input/Output
14	D2	Data Bus 2	Input/Output
15	D3	Data Bus 3	Input/Output
16	D4	Data Bus 4	Input/Output
17	D5	Data Bus 5	Input/Output
18	D6	Data Bus 6	Input/Output
19	D7	Data Bus 7	Input/Output
20	AGND	Analog Ground	Input
21	VAA	Analog Power	Input
22	A0	Command Control 0	Input
23	A1	Command Control 1	Input
24	R/$\overline{W}$	Read/Write Control	Input
25	$\overline{CS}$	Chip Select Control	Input
26	AGND	Analog Ground	Input
27	IOR	Red Video Current	Output
28	IOG	Green Video Current	Output
29	IOB	Blue Video Current	Output
30	AGND	Analog Ground	Input
31	VAA	Analog Power	Input
32	VAA	Analog Power	Input
33	COMP	Compensation	Input
34	VREF	Voltage Reference	Output
35	FSADJ	Full Scale Adjust Control	Input
36	AGND	Analog Ground	Input
37	VAA	Analog Power	Input
38	$\overline{CLK}$	Clock Differential	Input
39	CLK	Clock Differential	Input
40	$\overline{SYNC}$	Composite Sync Control	Input
41	$\overline{BLANK}$	Composite Blank Control	Input
42	$\overline{LD}$	Load Control	Input
43	VAA	Analog Power	Input
44	AGNP	Analog Ground	Input
45	VIDCLK	Video Clock	Output
46	PD31	Pixel Data 31	Input
47	PD23	Pixel Data 23	Input
48	PD15	Pixel Data 15	Input
49	PD7	Pixel Data 7	Input
50	VAA	Analog Power	Input
51	AGND	Analog Ground	Input

TABLE 1. PIN IDENTIFICATION (CONT'D,

PIN NO	PIN NAME	DESCRIPTION	TYPE
52	PD30	Pixel Data 30	Input
53	PD22	Pixel Data 22	Input
54	PD14	Pixel Data 14	Input
55	PD6	Pixel Data 6	Input
56	PD29	Pixel Data 29	Input
57	PD21	Pixel Data 21	Input
58	PD13	Pixel Data 13	Input
59	PD5	Pixel Data 5	Input
60	PD28	Pixel Data 28	Input
61	PD20	Pixel Data 20	Input
62	PD12	Pixel Data 12	Input
63	PD4	Pixel Data 4	Input
64	PD27	Pixel Data 27	Input
65	PD19	Pixel Data 19	Input
66	PD11	Pixel Data 11	Input
67	PD3	Pixel Data 3	Input
68	PD26	Pixel Data 26	Input

TABLE 2. PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
$\overline{\text{BLANK}}$	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 10. It is latched on the rising edge of VIDCLK. When $\overline{\text{BLANK}}$ is a logical zero, the pixel inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 11). $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Table 10. Therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of VIDCLK.
$\overline{\text{LD}}$	Load control input (TTL compatible). The PD[31:0] inputs are latched on the rising edge of $\overline{\text{LD}}$. The $\overline{\text{LD}}$ frequency depends on the format of pixel data, the number of bits per pixel, and whether convolution is enabled or not. $\overline{\text{LD}}$ may have any duty cycle, within the limits specified by the A.C. Characteristics section. If CLK and $\overline{\text{CLK}}$ are tied to AGND, $\overline{\text{LD}}$ becomes the master clock input (this mode of operation is recommended for PACKED CONVOLUTION or 24-bit convolution when the frequency of VIDCLK is greater than 50MHz).

TABLE 2. PIN DESCRIPTIONS (CON~

PIN NAME	DESCRIPTION
PD[31:0]	Pixel data inputs (TTL compatible). These inputs are used to specify pixel data in one of two formats, chunky or 24 bit. Chunky data specifies pixels from 1 to 8 bits per pixel. Thus each chunky word can contain from 4 to 32 pixels. Note that the high order, or more significant chunks are displayed first. 24 bit data contains one 24 bit pixel with PD[31:24] ignored. The pixel data inputs are latched on the rising edge of $\overline{LD}$. Unused inputs should be connected to AGND.
IOR, IOG, IOB	Red, green, and blue video current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 75Ω coaxial cable (Figure 16).
VAA	Analog power. All VAA pins must be connected.
AGND	Analog ground. All AGND pins must be connected.
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1µF ceramic capacitor must be connected between this pin and VAA. (Figure 16) connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full scale video signal (Figure 16). Note that the IRE relationship in Figure 11 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is: 1. For a 7.5 IRE Blanking pedestal IOG (MA) = 13628/RSET (ohms) The full scale output current on IOR and IOB for a given RSET is: IOR, IOB (MA) = 9734.5/RSET (ohms). 2. For a Ø IRE Blanking pedestal IOG (MA) = 13848/RSET (ohms) The full scale output current on IOR and IOB for a given RSET is : IOR, IOB (MA) = 9734.5/RSET (ohms)
VREF	Voltage reference pin. This is the output of the internal band gap reference. A .01 µF capacitor should be placed between this pin and VAA. Alternatively the internal reference may be overdriven by an external reference with a sufficiently low valued pull-up resistor.
CLK, $\overline{CLK}$	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 volt) operation. The clock rate is typically the pixel clock rate of the system or four times the pixel clock rate in convolution modes. If CLK and $\overline{CLK}$ are tied to GND*, $\overline{LD}$ becomes the master clock input (this mode of operation is recommended for PACKED CONVOLUTION or 24-bit convolution when the frequency of the internal clock and the frequency of $\overline{LD}$ are greater than 50 MHz. * GND defined as < TTL V_{IL} (0.8V)
VIDCLK	Clock output. This TTL compatible output is programmable to generate the CLK frequency divided by a scale factor programmable to 1, 2, 4, or 8. This signal must be buffered. VIDCLK is optimized to drive 12 inches of trace (20 pF) and one load (10 pF) totalling 30 pF at 60 MHz operation when ECL clocks are grounded and $\overline{LD}$ becomes the master clock input. $\overline{SYNC}$ and $\overline{BLANK}$ are latched into the device on the rising edge of VIDCLK.

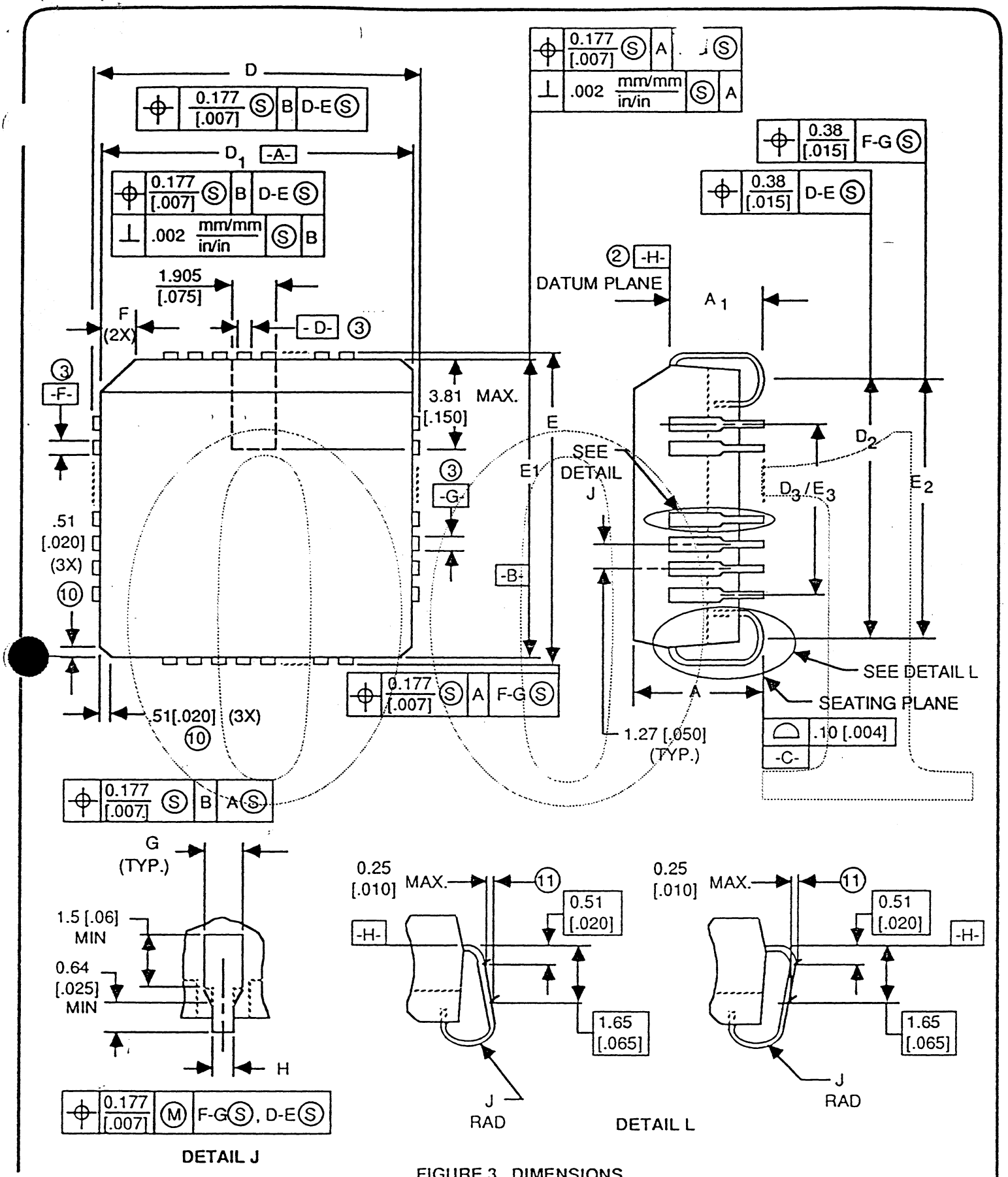


FIGURE 3. DIMENSIONS

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S1075-01
SCALE: NONE	SHT 7 OF 33

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	5.08	0.165	0.200
A_1	2.29	3.30	0.090	0.130
D	25.02	25.27	0.985	0.995
D_1	24.13	24.33	0.950	0.958
D_2	22.61	23.62	0.890	0.930
D_3	20.32 REF.		0.800 REF.	
E	25.02	25.57	0.985	0.995
E_1	24.13	24.33	0.950	0.958
E_2	22.61	23.62	0.890	0.930
E_3	20.32 REF.		0.800 REF.	
F	1.07	1.22	0.042	0.048
G	0.66	0.81	0.026	0.032
H	0.33	0.53	0.013	0.021
J	0.64	1.14	0.025	0.045

PLCC-68

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -H- LOCATED AT TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS PLASTIC BODY.
3. DATUMS D-E AND F-G TO BE DETERMINED WHERE CENTER LEADS EXIT PLASTIC BODY AT DATUM PLANE -H-.
4. TO BE DETERMINED AT SEATING PLANE -C-.
5. TRANSITION IS OPTIONAL.
6. PLASTIC BODY DETAILS BETWEEN LEADS ARE OPTIONAL.
7. DIMENSIONS D_1 AND E_1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .254[.010].
8. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN ONE OF THE ZONES INDICATED.
9. LOCATION TO DATUMS -A- AND -B- TO BE DETERMINED AT PLANE -H-.
10. EXACT SHAPE OF THIS FEATURE IS OPTIONAL.
11. THESE TWO DIMENSIONS DETERMINE MAXIMUM ANGLE OF THE LEAD FOR CERTAIN SOCKET APPLICATIONS. IF UNIT IS INTENDED TO BE SOCKETED, IT IS ADVISABLE TO REVIEW THESE DIMENSIONS WITH THE SOCKET SUPPLIER.
12. CONTROLLING DIMENSION: INCH.

FIGURE 3. DIMENSIONS (CONT)

2.0 APPLICABLE DOCUMENTS (latest revision):

MIL-STD-202 Test methods for electronic and electrical component parts.
MIL-STD-883 Test methods and procedures for microelectronics.

3.0 REQUIREMENTS:

3.1 PHYSICAL:

3.1.1 PACKAGE: Void free plastic 68-pin PLCC package. Dimensions per Figure 3.

3.1.2 MARKINGS: Manufacturer's name or logo and manufacturing date code, Apple part number, current revision level, mask and copyright symbols, year and Apple name or logo.

EXAMPLE: 343S1075-A

Ⓜ Ⓒ 1991 Apple

3.1.3 SOLDERABILITY: Leads solderability must meet MIL-STD-202, Method 208. Prior to test, the devices shall be subjected to steam aging for a period of 8 hours.

3.2 ELECTRICAL:

3.2.1 ELECTROSTATIC DISCHARGE SENSITIVITY: The minimum electrostatic discharge voltage per pin is ±2000 volts as specified in MIL-STD-883, Method 3015.3 (i.e., C = 100 pF, R = 1.5KΩ).

3.2.2 LATCH-UP TEST: The minimum latch-up current for all pins except ground is 50mA in both positive and negative directions. This applies to full temperature and power supply ranges.

3.2.3 PIN CONFIGURATION: Per Figure 1.

3.2.4 PIN IDENTIFICATION: Per Table 1.

3.2.5 PIN DESCRIPTION: Per Table 2.

3.2.6 BLOCK DIAGRAM: Per Figure 2.

3.2.7 ABSOLUTE MAXIMUM RATINGS: Per Table 3.

3.2.8 RECOMMENDED OPERATING CONDITIONS: Per Table 4.

3.2.9 STATIC PARAMETERS: Per Table 5.

3.2.10 DYNAMIC PARAMETERS: Per Table 6, Figures 4, 5a and 5b.

3.3 ENVIRONMENTAL:

3.3.1 RESISTANCE TO SOLDERING HEAT:

a) Wave or hand soldering: With a 100°C preheat for 20 seconds, the components shall be totally immersed in molten solder, 260 ± 3°C for 7 ± 1 second per MIL-STD-202, Method 210, condition B (Per Figure A).

b) IR reflow solder: Preheat at 3°C/sec to 150°C, and using 60/40 solder, IR at 240°C for 30 seconds (Per Figure B).

c) Component must withstand two (section 3.3.1.b) IR reflow solder cycles with a cool-down in between.

d) Component must withstand one (section 3.3.1.b) IR reflow solder cycle followed, after a cool-down, by a (section 3.3.1.a) wave or hand soldering cycle.

After resistance to soldering heat test, there shall be no evidence of leaching or cracking and the parts shall meet all electrical and mechanical specifications.

RESISTANCE TO SOLDERING HEAT PROFILES

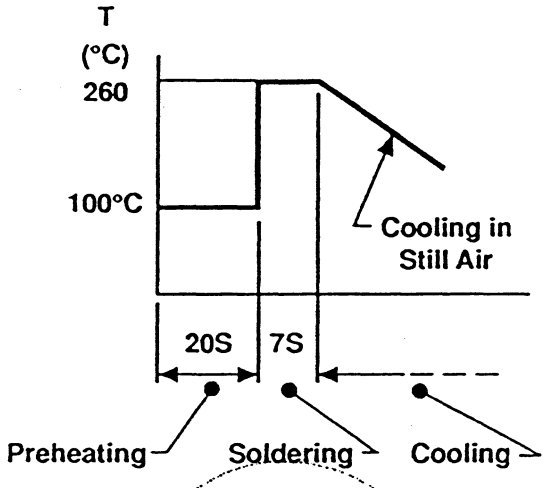


FIGURE A. WAVE/HAND SOLDERING

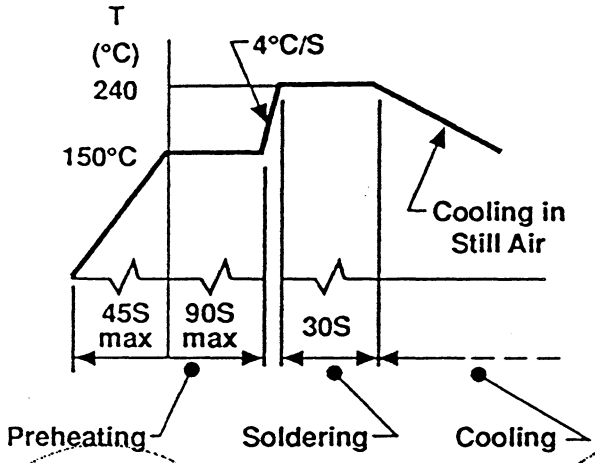


FIGURE B. INFRARED SOLDERING

3.3.2 **CLEANING:** Parts must be washable in standard flux removal solvent and must not trap any cleaning liquids.

4.0 **QUALITY ASSURANCE PROVISIONS:** Parts shall be inspected to assure compliance to the requirements of this specification.

5.0 **PACKAGING:** Parts shall be packaged according to requirements specified in purchase order for safe delivery at Apple or Apple designated contractor. (Parts requiring Tape & Reel shall meet the proper Tape & Reel specification per the purchase order.)

TABLE 3. ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS
VAA	Analog Power Supply (measured to AGND)		7.0	Volts
	Voltage on any Digital Pin	AGND -0.5	VAA +0.5	Volts
ISC	Analog Output Short Circuit Duration to any Power Supply or Common	indefinite		
TA	Ambient Operating Temperature	-55	+125	°C
TS	Storage Temperature	-65	+150	°C
TJ	Junction Temperature		+150	°C
PD	Power Dissipation		2100	mW
PD2	Power Dissipation, Low-Power Mode		1700	mW

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affected device reliability.

TABLE 4. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VAA	Power Supply	4.75	5.00	5.25	Volts
TA	Ambient Operating Temperature	0		+70	°C
RL	Output Load		37.5		Ω
RSET	FS Adjust Resistor		511		Ω
VREF	Reference Voltage (External)		1.235		V

TABLE 5. STATIC PARAMETERS

Test conditions (unless otherwise specified)
"Recommended Operating Conditions" See Table with RSET = 511Ω
The above parameters are guaranteed over the full temperature range
Blank Pedestal = 7.5 IRE, VREF = 1.235V

SYMBOL	PARAMETER	MIN	MAX	UNITS
	Analog Outputs			
	Resolution (each DAC)	8	8	Bits
	Accuracy (each DAC)			
IL	Integral Linearity Error		1	LSB
DL	Differential Linearity Error		1	LSB
	Gray Scale Error		±5	% Gray Scale

TABLE 5. STATIC PARAMETERS (CONT'D,

SYMBOL	PARAMETER	MIN	MAX	UNITS
	Digital Inputs (except CLK, $\overline{CLK}$, when $\overline{CLK}$ is not tied to AGND)			
VIH	Input High Voltage	2.0	VAA +0.5	Volts
VIL	Input Low Voltage	GND -0.5	0.8	Volts
IIH	Input High Current (Vin = 2.4V)		1	µA
IIL	Input Low Current (Vin = 0.4V)		-1	µA
CIN	Input Capacitance (f = 1 MHz, Vin = 2.4V)		10	pF
	Clock Inputs (CLK, $\overline{CLK}$)			
VKIH	Input High Voltage	VAA -1.0	VAA +0.5	Volts
VKIL	Input Low Voltage	GND -0.5	VAA -1.6	Volts
IKIH	Input High Current (Vin = 4.0V)		1	µA
IKIL	Input Low Current (Vin = 0.4V)		-1	µA
CKIN	Input Capacitance (f = 1 MHz, Vin = 4.0V)		10	pF
	Digital Outputs			
VOH	Output High Voltage	2.4		Volts
VOL	Output Low Voltage		0.4	Volts
IOH	Output High Current			
	D [7:0]	400		µA
	VIDCLK	800		µA
IOL	Output Low Current			
	D [7:0]	3.2		mA
	VIDCLK	4		mA
IOZ	3-state Current		10	µA
CDOUT	Output Capacitance		10	pF
	Internal Reference Voltage	1.18	1.26	Volts
	Reference Tempco		0.2	mV/°C
	Analog Outputs			
	Output Current			
	White Level Relative to Blank	17.69	20.40	mA
	White Level Relative to Black	16.74	18.50	mA
	Black Level Relative to Blank	0.95	1.90	mA
	Blank Level on IOR, IOB	0	50	µA
	Blank Level on IOG	6.29	8.96	mA
	Sync Level on IOG	0	50	µA
	LSB Size	65	73	µA
	DAC to DAC Matching		5	%
VOC	Output Compliance	-1.0	+1.2	Volts
RAOUT	Output Impedance		50	KΩ
CAOUT	Output Capacitance (f= 1 MHz, IOUT = 0 mA)		20	pF

TABLE 6. DYNAMIC PARAMETERS

SYMBOL	PARAMETER	FIGURE NO.	MIN/ MAX	VALUE	UNITS
Fmax	Clock Rate	—	max	100	MHz
LDmax	$\overline{LD}$ Rate (See Note 1)	—	max	64	MHz
1	R/$\overline{W}$, A0, A1 Setup Time	4	min	0	ns
2	R/$\overline{W}$, A0, A1 Hold Time	4	min	15	ns
3	$\overline{CS}$ Low Time	4	min	50	ns
4	$\overline{CS}$ High Time	4	min	25	ns
5	$\overline{CS}$ Asserted to Data Bus Driven	4	min	7	ns
6	$\overline{CS}$ Asserted to Data Valid	4	max	75	ns
7	Negated to Data Bus 3-Stated	4	max	15	ns
8	Write Data Setup Time	4	min	35	ns
9	Write Data Hold Time	4	min	0	ns
10	Pixel Data Setup Time	5a	min	3	ns
11	Pixel Data Hold Time	5a	min	2	ns
12	$\overline{SYNC}$ and $\overline{BLANK}$ Setup Time	5a	min	5	ns
13	$\overline{SYNC}$ and $\overline{BLANK}$ Hold Time	5a	min	2	ns
14	Clock Cycle Time	5a	min	10	ns
15	Clock Pulse Width High Time	5a	min	4.2	ns
16	Clock Pulse Width Low Time	5a	min	4.2	ns
17	$\overline{LD}$ Cycle Time	5a	min	15.62	ns
18	$\overline{LD}$ Pulse Width High	5a	min	5	ns
19	$\overline{LD}$ Pulse Width Low (See note 1)	5a	min	5	ns
20	VIDCLK Cycle Time	5a	min	30	ns
21	VIDCLK Pulse Width High	5a	min	12	ns
22	VIDCLK Pulse Width Low	5a	min	12	ns
23a	VIDCLK to $\overline{LD}$ Delay	5a	min	2	ns
	(When VIDCLK used to		max	10	ns (Note 6.)
	generate $\overline{LD}$) (See note 1)		max	15	ns
23b	$\overline{LD}$ to VIDCLK Delay (when $\overline{LD}$ is used to generate VIDCLK	5b	min	5	ns
			max	12	ns
24	Analog Output Delay -	5a	max	20	ns
25	Analog Output Rise/Fall Time	5a	max	2	ns
26	Analog Output Settling Time	5a	max	8	ns
	Clock and Data Feedthrough	—	max	-23	dB
	Glitch Impulse	—	max	75	pV-sec
	DAC to DAC Crosstalk	—	max	-23	dB
	Analog Output Skew	—	max	2	ns
	Pipeline Delay	—	min	6	Clocks
		—	max	102	Clocks

TA : 6. DYNAMIC PARAMETERS (CONT'D

SYMBOL	PARAMETER	FIGURE NO.	MIN/ MAX	VALUE	UNITS
IAA	VAA Supply Current (See Note 2)	—	max	420	mA
IAA_{LP}	VAA Supply Current Low Power Mode	—	max	275	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions (See Table 4)" with RSET = 511Ω. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. ECL input values are VAA - 0.8 to VAA - 1.8 volts, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10pF, D[7:0] output load ≤ 50 pF, VIDCLK output load ≤ 30pF. See timing notes in Figure 8. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

NOTES:

1. Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1KΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3dB test bandwidth = 2x clock rate.
2. At Fmax. IAA (typ) at VAA = 5.0V, TA = 20°C. IAA (max) at VAA = 5.25v, TA = 0°C.
3. Output delay time measured from 50% point of the rising clock edge to 50% point of full scale transition.
4. Output settling time measured from 50% point of full scale transition to output settling within ± 1LSB.
5. Output rise/fall time measured between 10% and 90% points of full scale transition.
6. VIDCLK IS ≥ 33MHz.

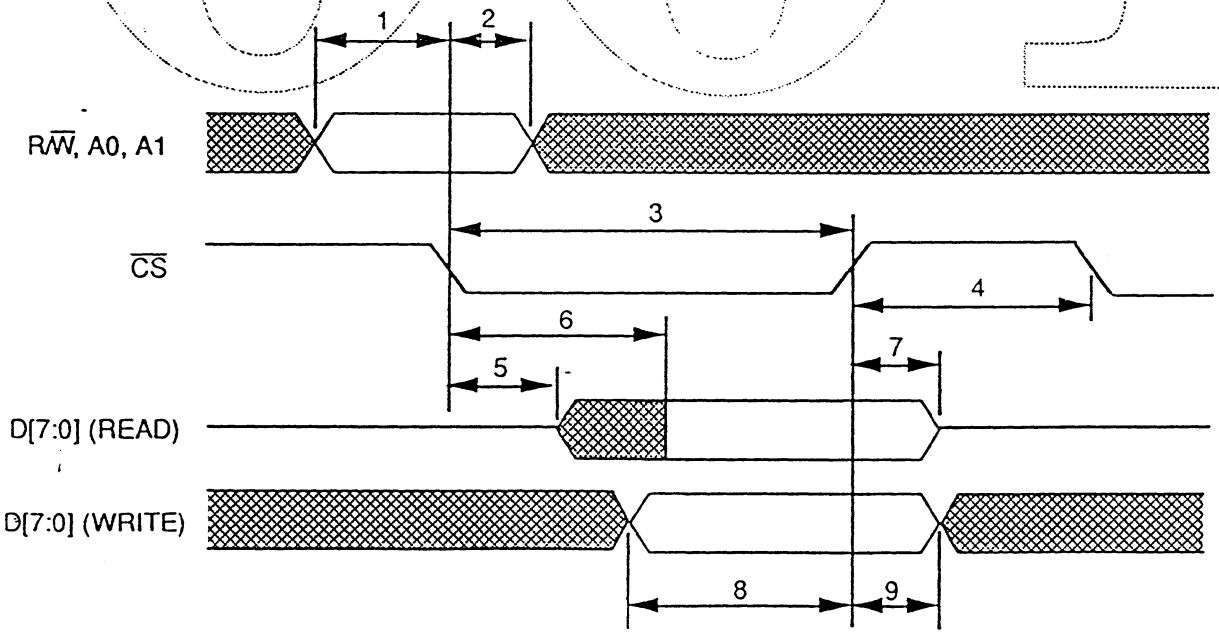


FIGURE 4. MPU READ/WRITE TIMING

Apple Computer, Inc.

SIZE A | DRAWING NUMBER 343S1075-01 | SCALE: NONE | SHT 14 OF 33

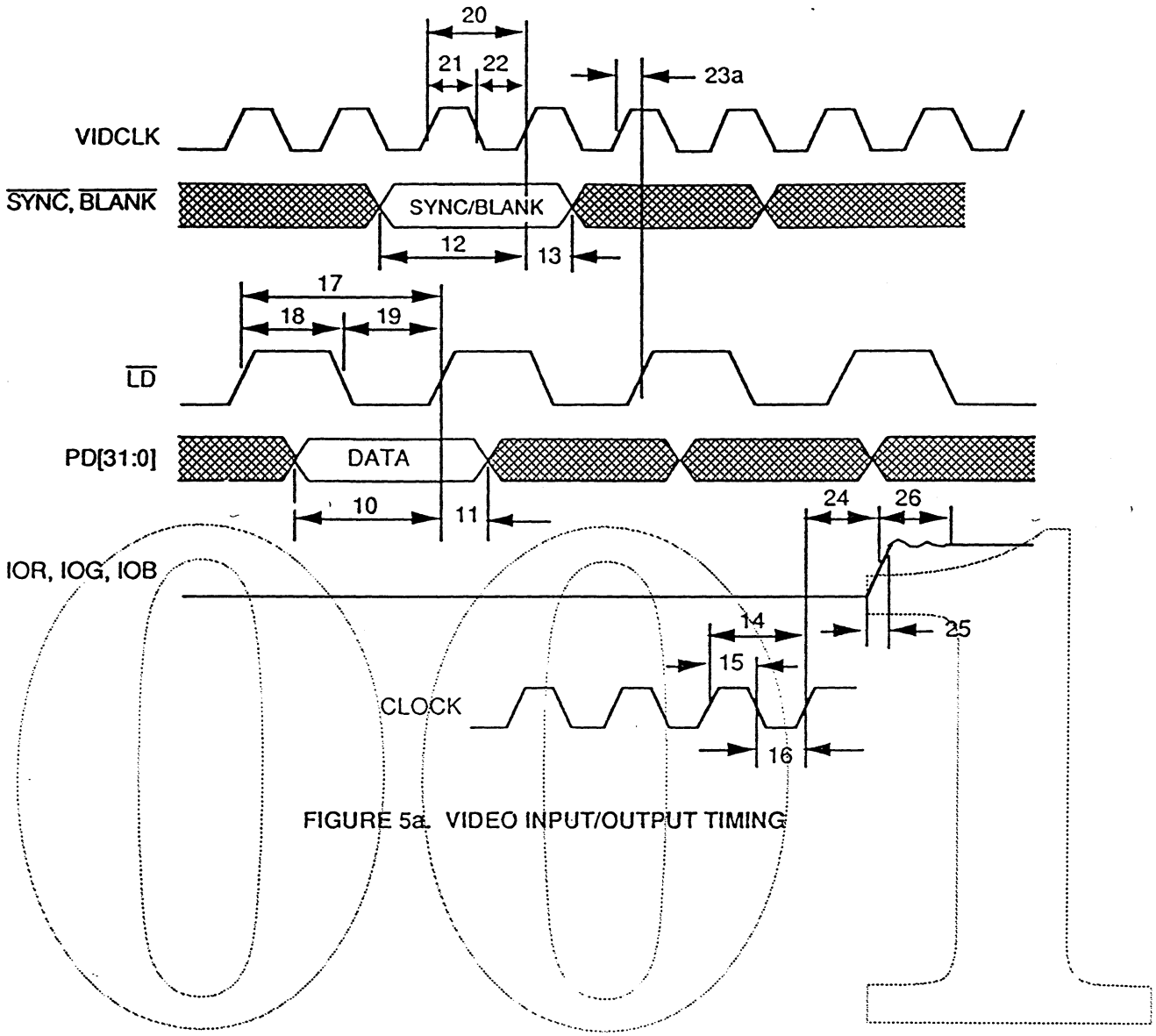


FIGURE 5a. VIDEO INPUT/OUTPUT TIMING

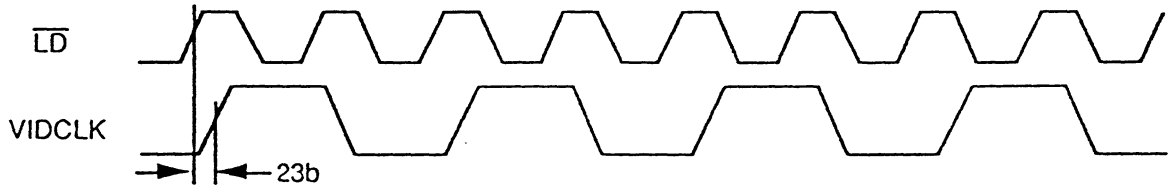


FIGURE 5b. $\overline{LD}$ to VIDCLK DELAY WHEN $\overline{LD}$ IS USED TO GENERATE VIDCLK

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S1075-01
SCALE: NONE	SHT 15 OF 33

6.0 **SUPPLEMENTARY INFORMATION:** The following is not to be used for acceptance nor rejection of the part herein.

6.0.2 REFERENCES: The following is a list of all the pertinent ASIC deliverables filed in Document Control:

- SCHEMATIC NETLIST TAPE
- PRINTED LISTING OF FILE NAMES, CELL LIBRARY, SOFTWARE PROGRAM DESIGNATION, AND REVISION LEVEL
- LOGIC DIAGRAM PLOTS
- SPECIFICATIONS FOR PRIMITIVES AND MACRO CELLS
- SIMULATION TAPE AND LISTING
- CRITICAL TIMING ANALYSIS SIMULATION TAPE
- MASK DATA BASE TAPE
- PRODUCTION TEST PROGRAM TAPE AND LISTING
- TEST PROGRAM IN TAR FORMAT
- TEST LANGUAGE DOCUMENTS AND FILE LISTING
- TEST LOAD BOARD
- BONDING DIAGRAM

6.0.1 PRODUCT DESCRIPTION:

The AC843 is designed specifically for Apple graphics needs of the future. The architecture enables the display of up to 1152 X 870 bit mapped color graphics (up to 16 bits per pixel). The multiple pixel ports and internal multiplexing enables TTL compatible interfacing (up to 64 MHz) to the frame buffer, while maintaining 100 MHz video data rates at 1, 2, 4, 8, or 16 bits per pixel. 24 bit chunky planar multiplexing enables a 24 bit or 12 bit chunky planar frame buffer to maintain 64 MHz video data rates. 24 bit mode enables a 32 bit frame buffer (upper byte ignored) to maintain 64 MHz video data rates. Convolved video data can maintain a rate of 16 MHz.

The AC843 contains triple 256 x 8 color lookup tables with triple 8-bit video D/A converters. On chip features include Apple convolution, 8 bit psuedo color lookup or triple 8 bit lookup for 16 and 24 bit modes, chunky, and chunky planar multiplexing, and built in logic block observation.

The AC843 generates a TTL compatible clock output which is programmable to be the fequency of the CLK input divided by a scale factor which can take on the values 1, 2, 4, or 8.

The AC843 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly-terminated 75-ohm coax directly, without requiring external buffering. A 7.5 IRE setup current can be enabled or disabled in software without changing external set resistors.

The differential and integral linearity errors of the D/A converters on the AC843 are guaranteed to be a maximum of ± 1 LSB over the full temperature range.

6.1 CIRCUIT DESCRIPTION:

6.1.1 MPU INTERFACE:

As illustrated in the functional block diagram (Figure 2), the AC843 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color lookup table. The dual-port lookup table RAM allows color updating without contention with the display refresh process.

The AC843 supports the same MPU signal definition and timing as the AC842, but slightly different internal, control register addressing to accommodate the extended functionality. As illustrated in Table 7, the read and write functionality of the internal address register, the color look up table and the test register remain the same as defined in the AC842 spec.

The 8-bit addr[illegible] egister (ADDR0-7) is used to address th[illegible] ernal RAM and registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0.

To write color data the MPU loads the address register with the address of the color lookup table RAM location to be modified. The MPU performs three successive write cycles (red, green, and blue) with A0 = 1 and A1 = 0. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location to be read. The MPU performs three successive read cycles (red, green, and blue) with A0 = 1 A1=0. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequency of red, green, and blue data.

When accessing the color lookup table RAM, the address register resets to $00 after a blue read or write cycle to location $FF. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb), unobervable from the MPU interface, that count modulo three. They are reset to Zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other eight bits of the address register (ADDR0-7) are accessible to the MPU.

The red, green, and blue test registers can be written (read) in the same way as the color lookup table RAM except that ADDR0-7 are ignored. When $\overline{\text{BLANK}}$ is active the test register is written (read) by first writing some value to the address register to clear ADDRa, b. The MPU then performs three successive write (read) cycles (red, green, and blue) with A0 = 1 and A1 = 1.

TABLE 7. ADDRESS REGISTER (ADDR) OPERATION

A [1:0]	R/W	PBCR [2:1]	ADDR0-7	ADDRESSED BY MPU
00	0	xx	D0-7	Write address register; D0-D7 –> ADDR0-7, 0 –> ADDRa, ADDRb
01	0	xx	8'h00-8'hFF	Write color table (three writes required for R, G & B)
01	1	xx	8'h00-8'hFF	Read color table (three reads required for R, G & B)
10	0	! = 2'b11	xx	Write control register 0; D0-D7 –> PBCR0
10	1	! = 2'b11	xx	Read control register 0; PBCR0 –> D0-D7
11	0	xx	xx	Write Test Register
11	1	xx	xx	Read Test Register

ADDITIONAL INFORMATION

Although the color lookup table RAM is dual-ported, if the pixel is addressing the same table entry being written to by the MPU during the blue write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Table 8b shows the new internal addressing scheme required to access the pixel bus control registers, PBCR and PBCR1. The A1 and A0 control inputs, in conjunction with the internal address register and PBCR [2:1], specify which control register will be accessed by the MPU. The single reserved encoding of the AC842 pixel bus control register, PBCR [2:1] == 2'b11, is used to enable the new, indirect addressing of the extended control space of the AC843. The pixel bus control registers may be written to or read by the MPU at any time.

When PBCR [2:1] ! =2'b11, read and write operations to address A [1:0] == 2'b10 directly access the PBCR. To preserve software compatibility with AC842, PBCR [2:1] is asynchronously reset to 2'b00 on power-up which initially limits access to only the PBCR. Assuming existing firmware does not incorrectly use the reserved encoding, AC843 will perform identically to AC842. Future firmware can be written to use the reserved encoding to access the extended functionality of the AC843.

When PBCR [2:1] == 2'b11, read and write operations to address A [1:0] == 2'b10 indirectly address both the PBCR and the PBCR1 registers. The two low order bits of the internal address register, ADDR0-1, are decoded to select either the PBCR or the PBCR1, as indicated below.

Tables 8a and 8b are the truth tables for reading and writing to the various AC843 internal registers and lookup tables. Figure 4 illustrates the MPU read/write timing when accessing the AC843.

TABLE 8a. TRUTH TABLE FOR READ/WRITE OPERATIONS

R/W	A1	A0	ADDRb	ADDRa	
0	0	0	x	x	Write address register; D0-D7 → ADDR0-7, 0 → ADDRa, ADDRb
0	0	1	0	0	Write red color; D0-D7 → RREG; increment ADDRa-b.
0	0	1	0	1	Write green color; D0-D7 → GREG, increment ADDRa-b
0	0	1	1	0	Write blue color; D0-D7 → BREG, write color palette RAM, increment ADDR0-7, increment ADDRa-b
0	1	1	0	0	Write red test; D0-D7 → RTEST, increment ADDRa-b
0	1	1	0	1	Write green test; D0-D7 → GTEST, increment ADDRa-b
0	1	1	1	0	Write red test; D0-D7 → BTEST, increment ADDRa-b
1	0	0	x	x	Read address register; ADDR0-7 → D0-D7, 0 → ADDRa, ADDRb
1	0	1	0	0	Read color lookup red; R0-R7 → D0-D7, increment ADDRa-b
1	0	1	0	1	Read color lookup green; G0-G7 → D0-D7, increment ADDRa-b
1	0	1	1	0	Read color lookup blue; B0-B7 → D0-D7, increment ADDR0-7, increment ADDRa-b
1	1	1	0	0	Read red test; RTEST → D0-D7, increment ADDRa-b
1	1	1	0	1	Read green test; GTEST → D0-D7, increment ADDRa-b
1	1	1	1	0	Read blue test; BTEST → D0-D7, increment ADDRa-b

TABLE 8b. TRUTH TABLE FC IXEL BUS CONTROL REGISTER (PBC READ/WRITE OPERATIONS

A [1:0]	R/W	PBCR [2:1]	ADDR0-1	ADDRESSED BY MPU
10	0	! = 2'b11	xx	Write control register 0; D0-D7 –> PBCR0,0 –> ADDRa, ADDRb
10	1	! = 2'b11	xx	Read control register 0; PBCR0 –> D0-D7,0 –> ADDRa, ADDRb
10	0	2'b11	2'h0	Write control register 0; D0-D7 –> PBCR0,0 –> ADDRa, ADDRb
10	1	2'b11	2'h0	Read control register 0; PBCR0 –> D0-D7,0 –> ADDRa, ADDRb
10	0	2'b11	2'h1	Write control register 1; D0-D7 –> PBCR1,0 –> ADDRa, ADDRb
10	0	2'b11	2'h1	Read control register 1; PBCR1 –> D0-D7,0 –> ADDRa, ADDRb
10	x	2'b11	!2'h0 | !2'h1	Error - Output TBD

EXTENDED REGISTER ADDRESSING PROCEDURE

In the AC843 redesign, an additional control register (PBCR1) is required for the 16 bit and DAC power down functions. An indirect addressing scheme is used to have this PBCR1 share the same control code as PBCR0. Because of the extra internal loading to this extra register, it is recommended to take an extra programming step to prevent possible data corruption to the PBCR0 and PBCR1 registers.

1. The AC843 is powered-up with direct addressing to PBCR0 only.
2. Write to PBCR0 with A0=0 & A1=1 for the desired mode setup or Write bit2 & 1 with 1 to PBCR0(with A0=0 & A1=1) to enable the indirect addressing.
3. Immediately Read from address register with A0 & A1 = 0 to prevent PBCR0 data from corruption.
4. Proceed with any operation desired or do the following for the AC843's extended functions.
5. Write 01 to the address registers with A0=0 & A1=0 to address PBCR1.
6. Write to PBCR1 with A0=0 & A1=1 for the desired mode setup.
7. Immediately Read from address register with A0 & A1=0 to prevent PBCR1 data from corruption.
8. Proceed with any operation desired.

6.1.2 PIXEL BUS INTERFACE:

The AC843 incorporates internal latches and multiplexers to enable pixel data to be transferred from a frame buffer at TTL data rates and to support variable depth pixel data. As illustrated in Figure 6, on the rising edge of $\overline{LD}$, PD [31:0] which contain pixel data for from 1 to 32 consecutive pixels (from 1 to 24 bits per pixel), are latched into the device. A VIDCLK signal output is provided that can be programmed to the CLK input frequency divided by a scale factor of 1, 2, 4, or 8. VIDCLK should be used to clock external circuitry to generate the basic video timing including $\overline{LD}$. $\overline{SYNC}$ and $\overline{BLANK}$ are latched into the device on the rising edge of VIDCLK. Note that with this configuration, the sync and blank timing will be recognized with the resolution of the VIDCLK frequency.

Depending upon the contents of the pixel bus control registers (PBCR and PBCR1) the AC843 outputs color information based on the pixel data inputs every clock cycle or if convolution is enabled every four clock cycles. The number of bits per pixel and the format of the pixel data specified in the PBCR and PBCR1 determines the number of clock cycles between loads on the pixel data bus. Figure 9 describes all the possible data formats on the pixel data bus.

There are two main data formats accepted by the AC843, chunky and packed. Chunky data can be from 1 to 16 bits per pixel. Each pixel time, the AC843 outputs color information based on the most significant chunk, followed by the next most significant, and proceeding until the least significant chunk.

16-bit data contains two pixels per 32-bit word. The most significant 16-bits are output first, followed by the least significant 16-bits. 24-bit data contains one pixel per 32-bit word with the upper byte PD [31:24] ignored.

CLK, $\overline{CLK}$ are +5 volt ECL differential inputs. Normally, CL. ., $\overline{CLK}$ are used to clock the video pipeline. They are also divided down to generate the VIDCLK output. The VIDCLK output frequency can be be programmed via the PBCR to be the master internal pixel clock frequency divided by a scale factor of 1, 2, 4 or 8. To meet internal setup and hold requirements $\overline{LD}$ must be timed appropriately with respect to the VIDCLK output. The VIDCLK output can be used to generate $\overline{LD}$ and VRAM shift clocks in a frame buffer system. When the ECL clocks are used to generate the master internal pixel clock, there must be at least one rising edge of VIDCLK for every rising edge of $\overline{LD}$. Alternatively, if the system requires clocking $\overline{LD}$ at greater than 50 MHz (PACKED CONVOLUTION for example), the master internal pixel clock can be switched to the $\overline{LD}$ signal (TTL levels < 60 MHz) which can be generated from a separate clock source. At 60 MHz, clock duty cycle becomes very important to maintain the 5ns pulse width requirement for the $\overline{LD}$ signal.

The AC843 supports two mechanisms for switching the main internal pixel clock to be derived from the $\overline{LD}$ signal: 1) CLK and CLK can be tied to ground* which is detected by internal logic to switch the clock source in hardware; 2) bit 4 of PBCR1 can be programmed to derive the main internal pixel clock from the ECL clocks or the $\overline{LD}$ signal. The software pixel clock selection mechanism was added to eliminate the unnecessary costs of grounding the +5V differential ECL clock signals. But to maintain hardware compatability with the AC842, the AC843 contains the hardware clock selection mechanism described above which will override the clock selection programmed by PBCR1[4]. Futhermore, on power-up, the pixel clock selection bit, PBCR1[4], is reset to select the ECL clock as the internal pixel clock.

PBCR1[4] is not modified to reflect the status of the hardware clock selection mechanism and, therefore, may not reflect the true status of the internal pixel clock selection. Only when the ECL clocks remain active will the software bit correctly reflect the internal pixel clock selection.

The maximum latency from setting PBCR[4] to the valid clock selection is 100 ns.

If standard chunky data is specified with convolution disabled, one rising edge of $\overline{LD}$ should occur every 32/(#bits per pixel) clock cycles. If standard chunky data is specified with convolution enabled, one rising edge of $\overline{LD}$ should occur every 8/(#bits per pixel) clock cycles. If chunky planar data is specified (convolution must be disabled), one rising edge of $\overline{LD}$ should occur every 8/(#bits per chunk) clock cycles. If 16-bit RGB data is specified, one rising edge $\overline{LD}$ should occur every 2 clock cycles; the master internal pixel clock can not be generated from the $\overline{LD}$ signal. If packed data is specified one rising edge of $\overline{LD}$ should occur every clock.

To maintain 100 MHz video data rates in 16 bit per pixel mode, the maximum VIDCLK frequency range has been extended to 50 MHz when the internal pixel clock is derived from the ECL clock inputs. For ECL clock rate is greater than 50 MHz, PBCR[6:5] must be programmed to divide the internal clock by two to generate the VIDCLK output. Additionally, to correctly resynchronize the pixel information latched at the positive edge of $\overline{LD}$ to internal ECL clock rate of AC843 requires the VIDCLK to $\overline{LD}$ delay to be tightened to 10 ns when VIDCLK is operated at greater than 33 MHz.

The timing diagram (Figure 6) illustrates the new timing spec in this mode of operation.

To simplify the interface timing for pixel data transfer rates greater than 50 MHz, the

* "Grounding" will be defined in the future as <TTL V_{IL}. (0.8V)

VIDCLK ≤ 33MHz

maximum VIDCLK frequency range has been extended to 60 MHz when the internal pixel clock is derived from the $\overline{LD}$ signal. In this mode of operation, the VIDCLK to $\overline{LD}$ delay is not required because the internal pixel clock of the AC843 is generated from the $\overline{LD}$ signal and resynchronizing the pixel data is not an issue. VIDCLK is only used to sample $\overline{SYNC}$/$\overline{BLANK}$.

By extending the VIDCLK frequency range to 60 MHz, $\overline{SYNC}$/$\overline{BLANK}$ will be sampled at the same rate as $\overline{LD}$ which eliminates the difficulty in the AC842 interface of synchronizing transitions in $\overline{SYNC}$/$\overline{BLANK}$ to the rising edge of the lower frequency VIDCLK output. To guarantee the 5 ns setup of $\overline{SYNC}$/$\overline{BLANK}$ with respect to LD, the timing spec 30, $\overline{LD}$ to VIDCLK delay, has been defined to allow $\overline{SYNC}$/$\overline{BLANK}$ to be asserted coincident with $\overline{LD}$. The timing is illustrated in Figure 7. $\overline{SYNC}$/$\overline{BLANK}$ timing will be recognized with resolution of VIDCLK which can be programmed via the PBCR to be the LD signal frequency divided by 1, 2, 4 or 8.

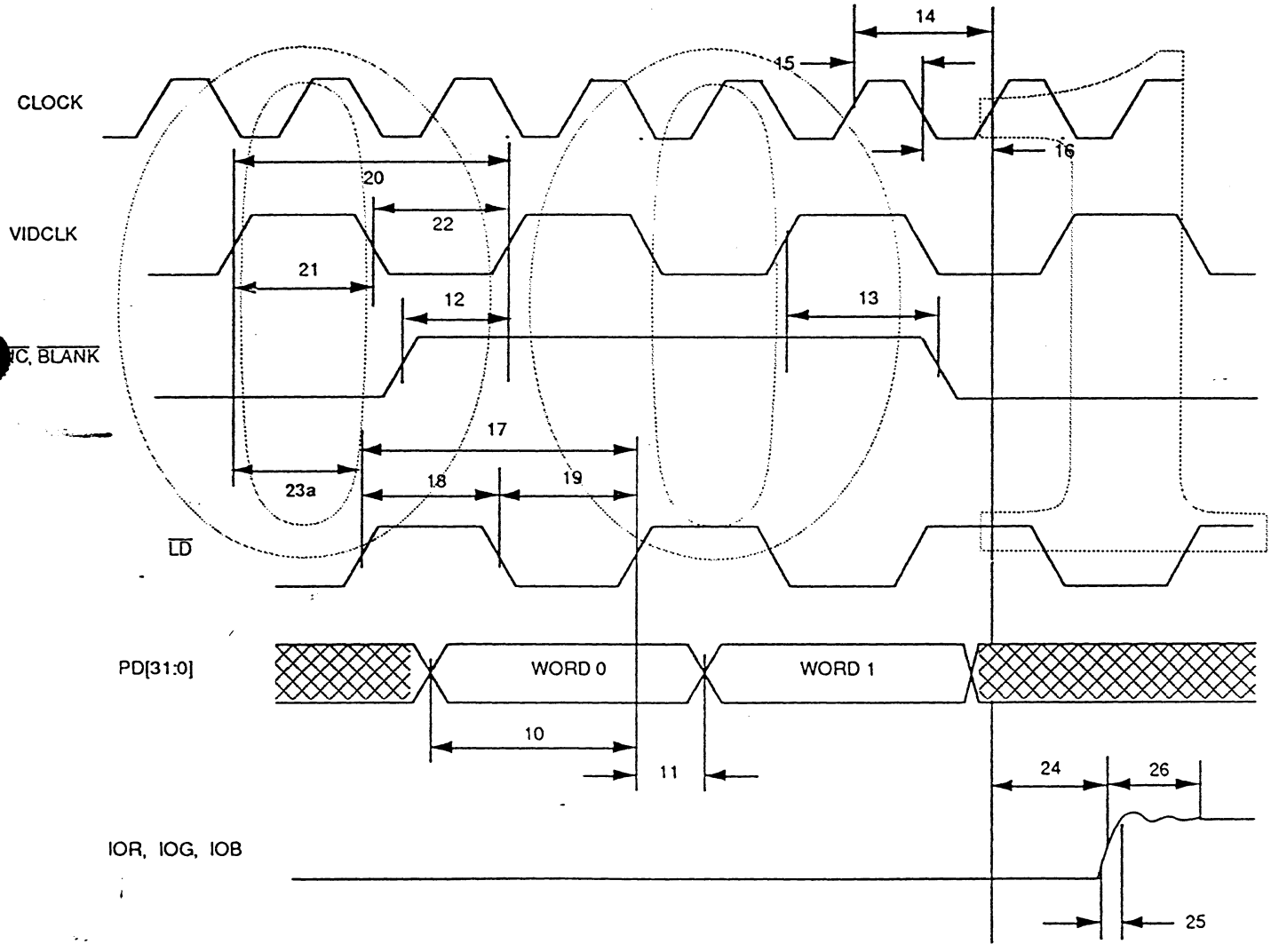


FIGURE 6. VIDEO INPUT/OUTPUT TIMING — ECL CLOCKS GENERATE PIXEL CLOCK : 100 MHz, VIDCLK FREQUENCY <= 50 MHz

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S1075-01
SCALE: NONE	SHT 21 OF 33

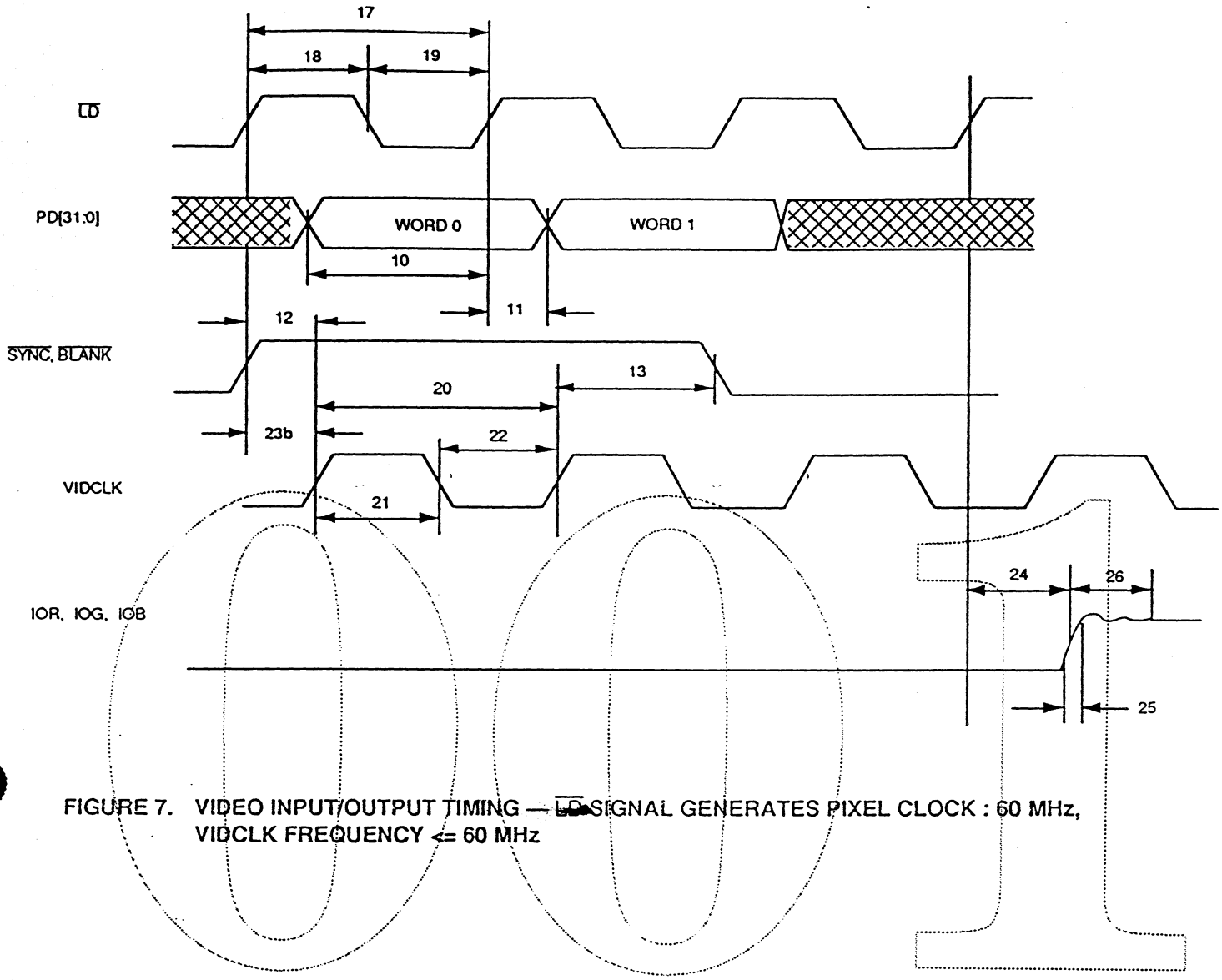


FIGURE 7. VIDEO INPUT/OUTPUT TIMING — $\overline{LD}$ SIGNAL GENERATES PIXEL CLOCK : 60 MHz, VIDCLK FREQUENCY <= 60 MHz

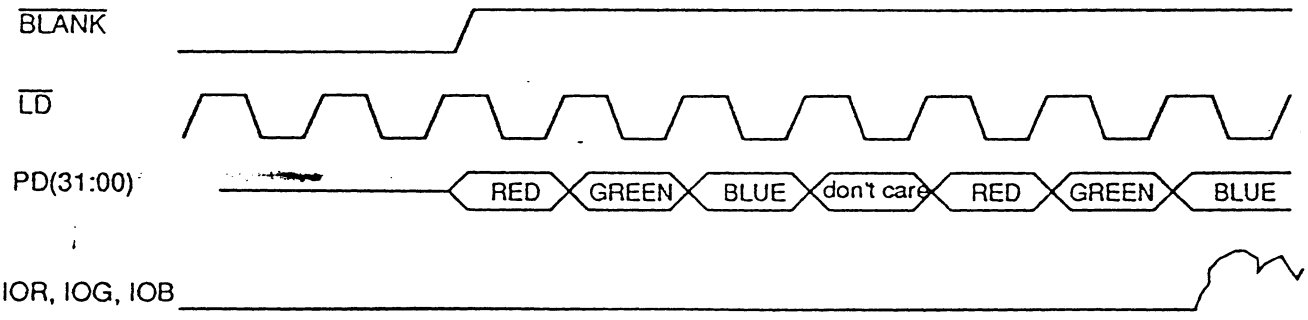


FIGURE 8. CHUNKY PLANAR VIDEO INPUT/OUTPUT TIMING

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S1075-01
SCALE: NONE	SHT 22 OF 33

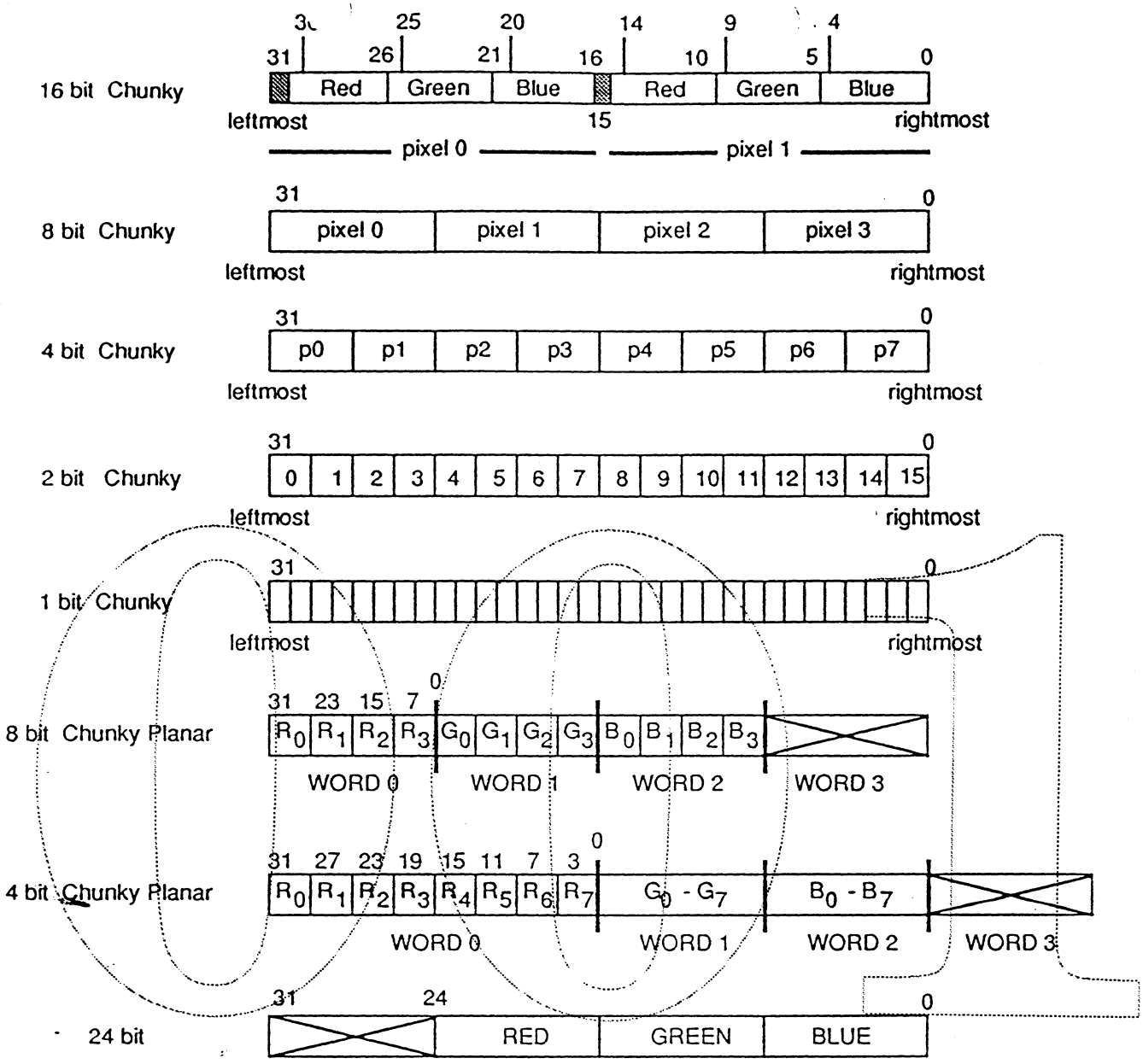


FIGURE 9. PIXEL DATA FORMATS

6.1.2.1 CHUNKY PLANAR:

In chunky planar mode the AC843 accepts 3 chunky format words (RED>GREEN>BLUE) on three rising edges of $\overline{LD}$ followed by one empty rising edge to make a four clock cycle. Only 8 bit and 4 bit chunky data is supported here. Internal multiplexers combine chunks from the three words starting with the most significant chunks proceeding to the least significant to produce 24 bit pixel values. Four bit chunks are zero extended in the most significant bits to form 8 bit chunks before being applied to a color table.
Figure 8 outlines this mode.

6.1.2.2 CONVOLUTION:

In convolution modes the AC843 accepts 3 words of either chunky or 24 bit data (line n-1>line n>line n+1) on three rising edges of $\overline{LD}$ followed by one empty rising edge to make a four clock cycle. Internal multiplexers and adder accumulators combine chunks or 24 bit pixel values from the words according to the formula ((line n-1) + (line n+1) + 2* (line n)+2)/4. This calculation is performed on the 24 bit pixel values after color lookup. Figure 10 outlines this mode.

The AC843 supports convolution operation for the 16 bit RGB pixel data format. Pixel data is clocked into the device in a similar procedure as described above for chunky data.

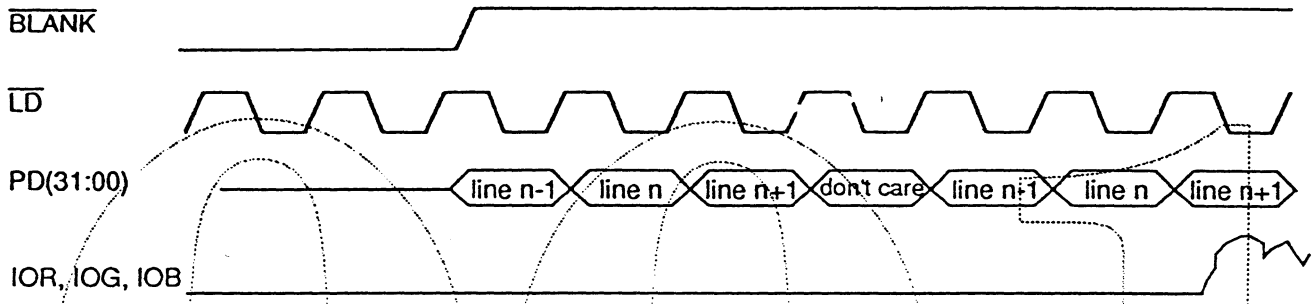


FIGURE 10. CONVOLUTION VIDEO INPUT/OUTPUT TIMING

6.1.2.3 COLOR SELECTION:

The AC843 supports table lookup for pixel data up to 24 bits per pixel. For 1-8 bit chunky data, on every clock a chunk is applied to the address inputs of the three (R, G, and B) color lookup tables. Chunks of less than 8 bits are zero extended in the most significant bits before being applied to the color tables. For Chunky Planar and 24 bit data each byte of the 24 bit pixel is applied to the address inputs of the corresponding individual color table (Note, chunky planar data with 4 bits per chunk is zero extended in the most significant bits before being applied to a color table).

In 16 bit per pixel mode, the five bits each of Red, Green and Blue color information are expanded to an 8 bit addresses, as shown below, and applied to the address inputs of the corresponding individual color table.

		Lookup Table Address		
	Pixel Data	Red	Green	Blue
16'b	x_R[4:0]_G[4:0]_B[4:0]	$R_4R_3R_2R_1R_0R_4R_3R_2$	$G_4G_3G_2G_1G_0G_4G_3G_2$	$B_4B_3B_2B_1B_0B_4B_3B_2$

Table 9 outlines the color selection process.

TABLE 9. LOOK-UP TABLE FOR COLOR SELECTION

Mode	PBCR4,3	PBCR2,1	Pixel	Lookup Table Address Red	Green	Blue
chunky 8 bits/pixel	11	00	$00	$00	$00	$00
chunky 8 bits/pixel	11	00	$01	$01	$01	$01
:	:	:	:	:	:	:
chunky 8 bits/pixel	11	00	$FF	$FF	$FF	$FF
chunky 4 bits/pixel	10	00	$F	$0F	$0F	$0F
chunky 2 bits/pixel	01	00	11	$03	$03	$03
chunky 1 bit/pixel	00	00	1	$01	$01	$01
24 bit chunky planar	11	01	$RrGgBb	$Rr	$Gg	$Bb
12 bit chunky planar	10	01	$0r0g0b	$0r	$0g	$0b
24 bit/pixel	11	10	$RrGgBb	$Rr	$Gg	$Bb

6.1.2.4 VIDEO GENERATION:

Every clock cycle, or every four clock cycles in convolution mode, the selected 24 bits of color information (8 bits each of red, green, and blue) are presented to the three 8-bit D/A converters. The $\overline{SYNC}$ and $\overline{BLANK}$ inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 11, and 12. Pixel Bus Control Register bit 7 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated. A 0 IRE pedestal will force the black level and blank level to be the same.

The Varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) contains sync information. Table 10 details how the $\overline{SYNC}$ and $\overline{BLANK}$ inputs modify the output levels.

The D/A converters on the AC843 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip band-gap reference and operational amplifier stabilizes the D/A converter's full scale output current against temperature and power supply variations.

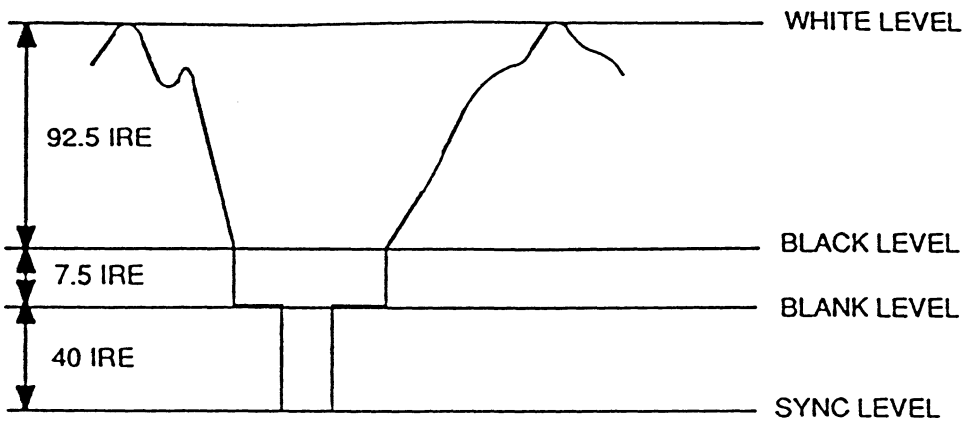
The AC843 contains triple 8-bit video D/A converters which can be disabled under software control to achieve low power dissipation when the video output is turned off. Bit 5 of PBCR1 can be programmed to enable or disable the DAC outputs.

When PBCR1[5] is set to 1'b1, all of the current references to the DACs are disabled and the outputs will be pulled to ground by the 75Ω parallel termination. This includes the SYNC current reference for the Green DAC output.

When PBCR1[5] is set to 1'b0, the DAC current references are enabled and the DAC outputs will settle to the appropriate levels in a maximum of 1 s (TBD) for a 0.1 µF compensation capacitor*.

* Apple currently uses four capacitors (0.01 µF, 0.1 µF, 1 µF, and 10 µF) in parallel between the COMP and VAA pins to provide compensation for the internal reference amplifier and improve power supply rejection.

RED, BLUE		GREEN	
mA	V	mA	V
19.25	0.722	26.84	1.007
1.44	0.054	9.09	0.341
0.00	0.000	7.65	0.287
		0.00	0.000



Note: 75Ω doubly-terminated load, RSET = 511Ω, Blank-pedestal = 7.5 IRE RS-343A levels and tolerances assumed on all levels. PBCR[7] = 1. VREF = 1.235V

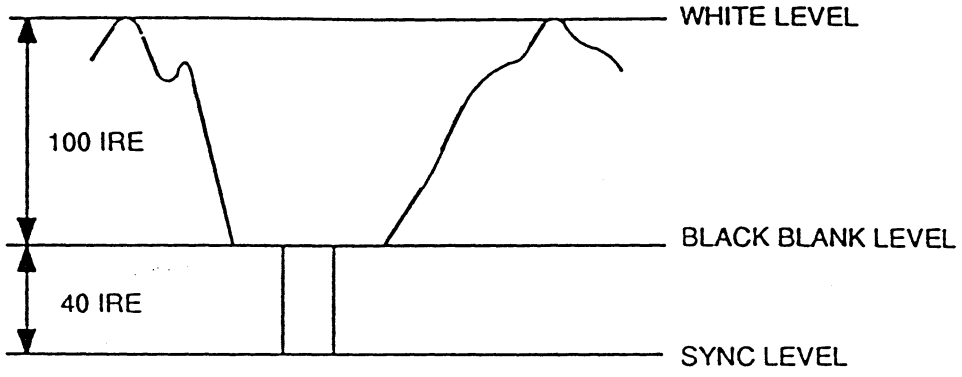
FIGURE 11. COMPOSITE VIDEO OUTPUT WAVEFORMS

TABLE 10. VIDEO OUTPUT TRUTH TABLE

DESCRIPTION	IOG (mA)	IOR, IOB (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE	26.84	19.25	1	1	$FF
DATA	(data * 0.0695) + 9.09	(data * 0.0695) + 1.44	1	1	data
DATA-SYNC	(data * 0.0695) + 1.44	(data * 0.0695) + 1.44	0	1	data
BLACK	9.09	1.44	1	1	$00
BLACK-BLANK	1.44	1.44	0	1	$00
BLANK	7.65	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full scale IOG = 26.84 mA. Blank pedestal = 7.5 IRE. RSET = 511Ω. PBCR[7] = 1. VREF = 1.235V

RED, BLUE		GREEN	
mA	V	mA	V
19.20	0.720	27.57	1.034
0.00	0.000	8.37	0.314
		0.00	0.000



Note: 75Ω doubly-terminated load, RSET = 511Ω, Blank pedestal = 0IRE. RS-343A levels and tolerances assumed on all levels. PBCR[7] = 0. VREF = 1.235V

FIGURE 12. COMPOSITE VIDEO OUTPUT WAVEFORMS

TABLE 11. VIDEO OUTPUT TRUTH TABLE

DESCRIPTION	IOG (mA)	IOR, IOB (mA)	$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	DAC Input Data
WHITE	27.57	19.20	1	1	$FF
DATA	(data * 0.075) + 8.37	(data * 0.075)	1	1	data
DATA-SYNC	(data * 0.075)	(data * 0.075)	0	1	data
BLACK	8.37	0	1	1	$00
BLACK-BLANK	0	0	0	1	$00
BLANK	8.37	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full scale IOG = 27.57 mA. RSET = 511 ohms. Blank pedestal = 0 IRE. PBCR[7] = 0. VREF = 1.235V

6.2 INTERNAL REGISTERS:

6.2.1 PIXEL BUS CONTROL REGISTER:

The pixel bus control register may be written to or read by the MPU at any time, and is not initialized. PBCR[0] corresponds to data bus bit D0.

When the indirect addressing of the control registers is enabled, PBCR[2:1] == 2'b11, the Extended Pixel Data Formats defined by bits [7:6] of PBCR1 will supersede the pixel data formats previously defined by bits [2:1] of PBCR. If the extended functionality of the AC843 is not utilized and the indirect addressing of the control registers is disabled, PBCR[2:1] != 2'b11, the pixel data formats are defined by bits [2:1] of PBCR, as defined in the AC842 spec.

The 16 bit RGB pixel data format can be selected by setting PBCR1[7:6] == 2'b11. When PBCR1[6] is programmed to enable 16 bit RGB, PBCR[4:3] must be set to 2'b11 to select 8 bit per pixel.

Pixel Bus Control Registers (PBCR and PBCR1)

PBCR - Pixel Bus Control Register

Bit 7	Pedestal Enable:	(0) 0 IRE pedestal (1) 7.5 IRE pedestal
Bit 6-5	VIDCLK Frequency Select:	(00) VIDCLK=CLK (01) VIDCLK=CLK/2 (10) VIDCLK=CLK/4 (11) VIDCLK=CLK/8
Bit 4-3	Bits Per Pixel	(00) 1bit (01) 2 bits (10) 4 bits (11) 8 bits
Bit 2-1*	Pixel Data Format:	(00) Standard Chunky (01) Chunky Planar (10) 24 bit (11) Indirect PBCR Addressing
Bit 0	Convolution Enable	(0) disable convolution (1) enable convolution

1001 1110

* On power-up, bit [2:1] initialized to 2'b00

PBCR1 - Pixel Bus Control Register 1

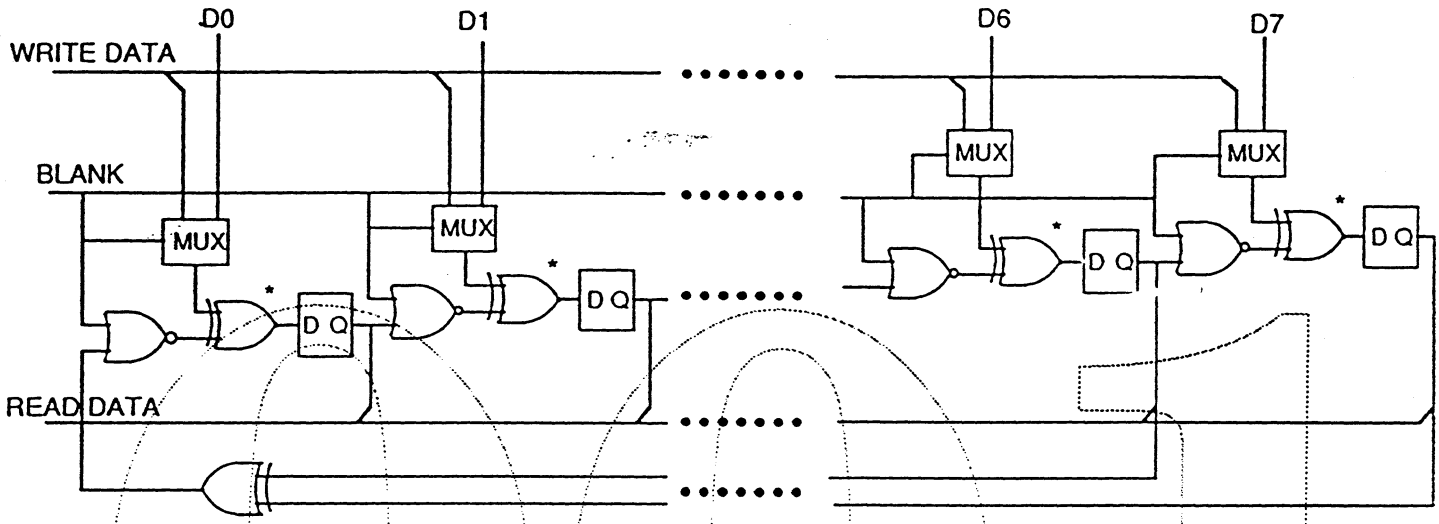
Bit 7-6*	Extended Pixel Data Format:	(00) Standard Chunky (01) Chunky Planar (10) 24 bit (11) 16 bit
Bit 5*	Low power mode	(1) - DAC outputs disabled (0) - DAC outputs enabled
Bit 4*	Pixel Clock Selection	(1) - $\overline{LD}$ signal (0) - ECL/$\overline{ECL}$ clock signals
Bit 3-1	Revision Number	(000) Fixed value first turn
Bit 0	Manufacturer Number	(0) AMD (1) - Reserved -

1100 0000

* On power-up, bits [7:4] are initialized to 4'b0000

6.2.2 TEST REGISTERS

The red, green and blue test registers are 8 bit signature analyzer registers. During blanking these registers are readable and writable. When blanking becomes inactive the registers generate parallel signatures based on the initial value stored in the register and the data on the input to the DACs. Every clock or every four clocks a new 8 bit value is combined from the DAC inputs with the current contents of the register. When blanking becomes active again the resultant signature can be read from each of the red, green and blue channels. A circuit diagram of the signature register is shown in Figure 13.



* Note: Some vendors may use Exclusive nor instead of Exclusive or.

FIGURE 13. TEST REGISTER FUNCTIONAL CIRCUIT DIAGRAM

6.3 $\overline{LD}$, VIDCLK and VIDEO TIMING COMPATIBILITY:

Normally $\overline{LD}$ is derived from VIDCLK and is a free running constant frequency clock. It clocks PD[31:0] into the internal latches. Thus the period of $\overline{LD}$ must be a multiple of the dot or pixel period. For example, if the part is in 8 bit per pixel chunky mode the $\overline{LD}$ period will be 4 times the pixel period, and if the part is in 1 bit per pixel chunky mode the $\overline{LD}$ period will be 32 pixel periods. As a result the active display period (BLANK = H) must be a multiple of the worst case $\overline{LD}$ period, or 32 pixel periods.

In the interest of compatibility, the AC843 can support local modification of the period of $\overline{LD}$ in the blanking period. For instance, to support a horizontal blanking period of 304 pixel periods (FP =32, HS = 128, BP = 144) in one bit per pixel mode a 16 pixel period cycle of $\overline{LD}$ can be inserted during horizontal blanking as shown in Figure 14. The internal pipeline will adjust to the new $\overline{LD}$ phase within some n clocks without disturbing the currently blanked video. Modifying the period of $\overline{LD}$ during unblanked video will produce undesirable results. In two bit per pixel mode or greater a 304 pixel period horizontal blanking period is not a problem as 16 goes into 304 evenly.

Since $\overline{SYNC}$ and $\overline{BLANK}$ are latched into the device by the rising edge of VIDCLK as opposed to $\overline{LD}$, there is more freedom with respect to the placement of the horizontal sync pulse during blanking than would be the case if $\overline{LD}$ latched $\overline{SYNC}$ and $\overline{BLANK}$. In order to produce correctly blanked video the signal $\overline{BLANK}$ should be generated in synchronism with the signal $\overline{LD}$.

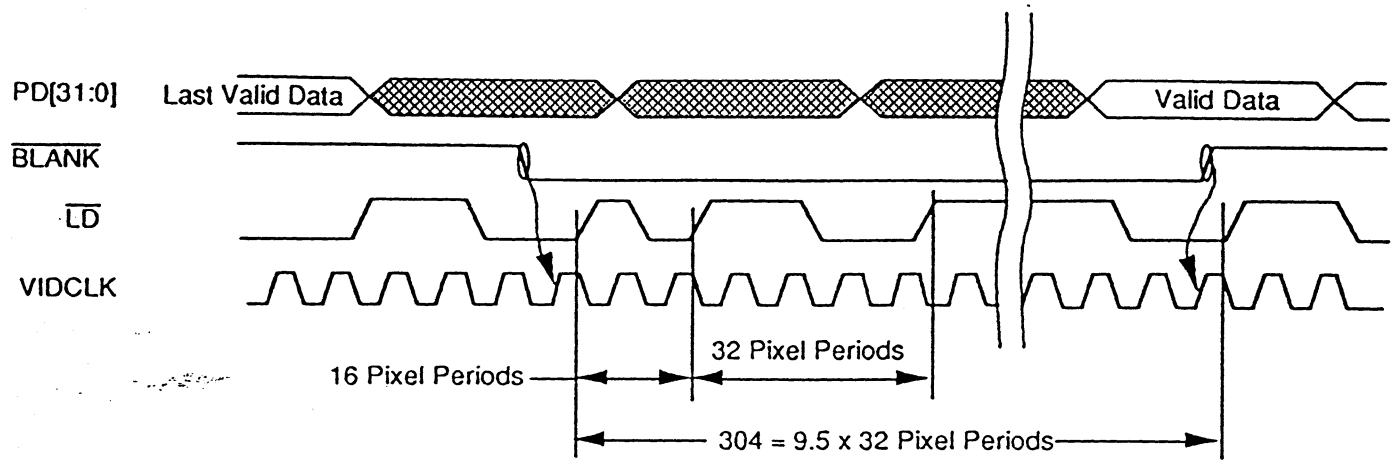


FIGURE 14. BACK PORCH WITH SHORT CYCLE

6.4 CLK INTERFACE:

Due to the high clock rates at which the AC843 may operate, it is designed to accept differential clock signals (CLK and $\overline{CLK}$). These clock inputs are designed to be generated by ECL logic operating at +5 volts. Note that the CLK and $\overline{CLK}$ inputs require termination resistors (220Ω resistor to VCC and a 330Ω resistor to GND). The termination resistors should be as close as possible to the AC843.

The CLK and $\overline{CLK}$ inputs must be differential signals due to the noise margins of the CMOS process. The AC843 can be operated using a single-ended TTL clock with CLK and $\overline{CLK}$ connected to ground. Here the AC843 automatically switches the internal clock to be derived from $\overline{LD}$. Alternatively, setting the appropriate PBCR1 bit will disable the ECL clock input and use the TTL $\overline{LD}$ clock as the pixel clock. The maximum frequency of $\overline{LD}$ is limited to 64 MHz.

Typically, $\overline{LD}$ is generated from the VIDCLK output or from a TTL oscillator when CLK and $\overline{CLK}$ are disabled. The designer must meet the timing requirements between VIDCLK and $\overline{LD}$ when VIDCLK is used to generate $\overline{LD}$.

6.5 POWER-ON RESET:

To maintain hardware and software compatability with the existing design, PBCR1 will be reset as follows on power-up.

Bit [7:6] = (00) 16 bit per pixel Disabled

Bit 5 = (0) DAC outputs enabled

Bit 4 = (0) ECL/$\overline{ECL}$ clock signals

Also, to maintain software compatability with the AC842, the MPU must have direct access to the PBCR on power-up. Therefore, the pixel data format or PBCR will be set to

PBCR[2:1] == 2'b00

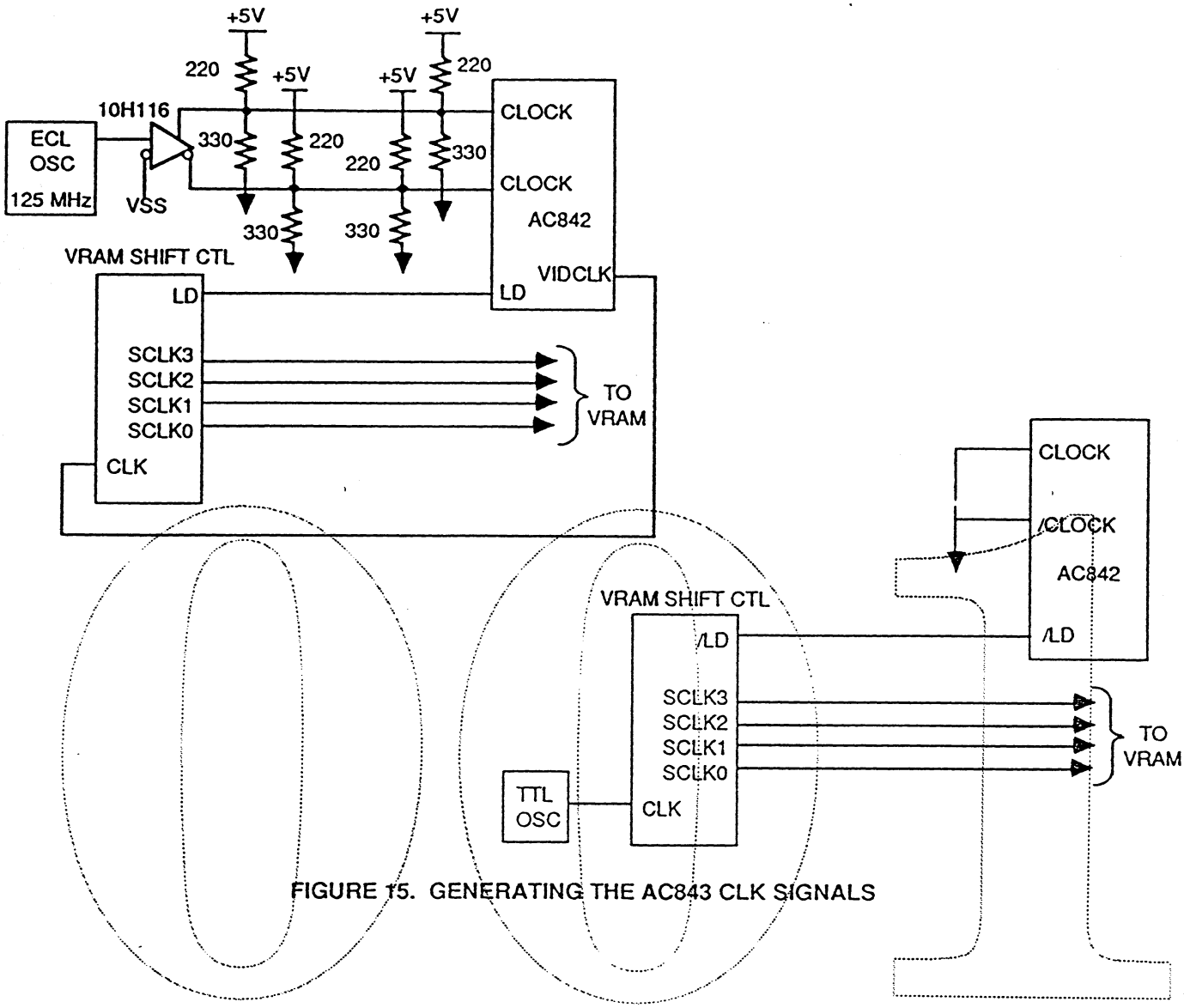


FIGURE 15. GENERATING THE AC843 CLK SIGNALS

Apple Computer, Inc.

SIZE	DRAWING NUMBER
A	343S1075-01
SCALE: NONE	SHT 31 OF 33

6.6 PC BOARD LAYOUT CONSIDERATION:

6.6.1 GENERAL:

It is recommended that a four layer PC board be used with the AC843. The layout should be optimized for lowest noise on the AC843 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

6.6.2 GROUND PLANES:

The ground plane area should encompass all AC843 ground pins, voltage reference circuitry, power supply bypass circuitry for the AC843, the analog output traces, any output amplifiers, and all the digital signal traces leading up to the AC843.

6.6.3 POWER PLANES:

The AC843 and any associated analog circuitry should have it's own power plan referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead. This bead should be located within three inches of the AC843.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all AC843 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

6.6.4 SUPPLY DECOUPLING:

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

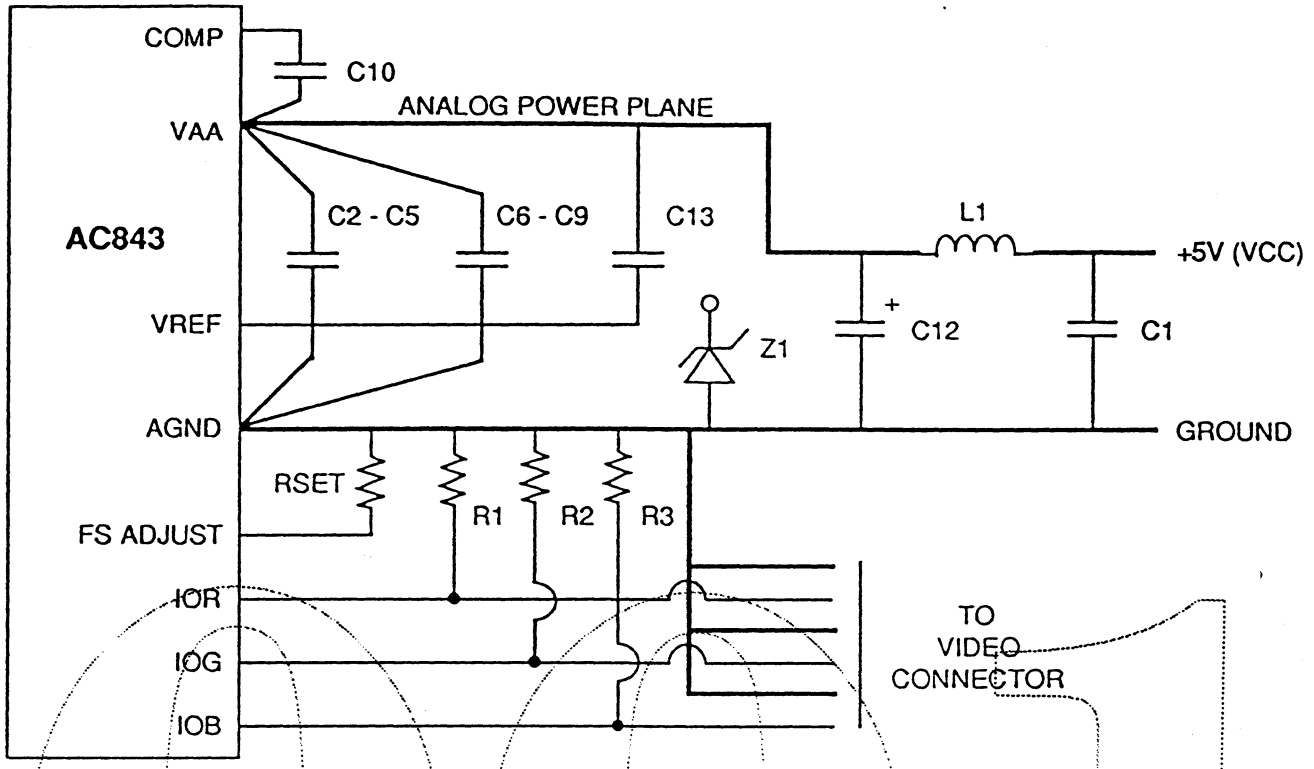
For the best performance, a 0.1 µF ceramic capacitor in parallel with a 0.01µF chip capacitor should be used to decouple each of the four groups of VAA pins (21, 31, 32, 37 and 50) to AGND. These capacitors should be placed as close as possible to the device. If chip capacitors are not feasible, radial lead ceramic capacitors may be used.

It is important to note that while the AC843 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

6.6.5 DIGITAL SIGNAL INTERCONNECT:

The digital inputs to the AC843 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not ovelay the analog power plane.

Due to the high clock rates involved, long clock lines to the AC843 should be avoided to reduce noise pickup.



LOCATION	DESCRIPTION
C1 - C5, C10	0.1 µF ceramic capacitor
C6 - C9, C13	0.01 µF ceramic chip capacitor
C12	33 µF tantalum capacitor
L1	Ferrite bead
R1, R2, R3	75-ohm 1% metal film resistor
RSET	511-OHM 1% metal film resistor
Z1	1.2V ±2% Voltage Reference (optional)

FIGURE 16. TYPICAL CONNECTION DIAGRAM