V-SERIES PRODUCT SPECIFICATION
DISTRIBUTION LIST
EMSG - MISSION VIEJO

SPECIFICATION NO: 1994 2382 SPECIFICATION TITLE: V300 SYSTEM PRODUCT SPEC

REVISION LETTER: F DATE OF ISSUE: 1-25-89

ATLANTA, GA.

L. BELL
S. BURROUGHS
C. HAMMER
T. NIESGODA
J. SANDERS
J. STOSSEL
K. WHEELWRIGHT

ATLANTA, GA.
C. FILLINGIM

FRAZER, PA.

R.A CRIST 300 LINDENWOOD

LIEGE, BELGIUM

J. WERY

MC LEAN, VA.

R. BROCHU
M. GAFFNEY

MISSION VIEJO, CA.

R. ABALOS MS 380

CONTINUED - MISSION VIEJO, CA.

D.	ABALOS	MS 105
F.	BEUGER	MS 380
R.	BIGHAM	MS 195
D.	BRITTLE	MS 275
R.	CAIRNS	MS 235
C.	DOOLING	MS 165
J.	GEORGE	MS 135
B.	GOULD	MS 175
F.	HAAS	
D.	HANSON	MS 205
R.	HARRIS	MS 135
A.	HATCH	MS 150
J.	HORKY	MS 170
M.	KALLAL	MS 105
C.	KING	MS 225
W.	LESH	RSM115
C.	LEUTHEN	MS 170
J.	MARTIN	MS 195
R.	MATHEWS	MS 225
V.	MCCLELLAND	MS 165
R.	MENDOZA	MS 135
J.	MOLASH	MS 135
B.	MORRIS	MS 135
W.	MURRAY	MS 165
S.	PATRICK	MS 275
B.	POTTER	MS 165
B.	POTTER	MS 135
L.	POTTER	MS 165
R.	QUAYLE	MS 135
J.	RUCKER	MS 520
H.	SOHL	MS 165
S.	SOLOMON	MS 135
A.	SPIELBERG	MS 152
T.	STERNAL	
D.	STONE	MS 285

For changes in this distribution list, contact D. Patten, M.V. Release and Configuration.

V-SERIES PRODUCT SPECIFICATION
DISTRIBUTION LIST
EMSG - MISSION VIEJO

SPECIFICATION NO: 1994 2382 SPECIFICATION TITLE: V300 SYSTEM PRODUCT SPEC

REVISION LETTER: F DATE OF ISSUE: 1-25-89

CONTINUED - MISSION VIEJO, CA.

W.	TERRY	MS 215
W.	THOMAS	MS 285
R.	TYNAN	MS 380
T.	VECCHIARELLI	MS275 (2 COPIES)
R.	WARREN	MS 135
P.	WORCESTER	MS 135
J.	YETTER	MS 165

PAOLI, PA.

G.	SMOLNIK	(TIC)

PASADENA, CA.

J.	BURTON	
W.	TREINEN	CC 6130
J.	VANZWALUWENBURG	

TREDYFFRIN, PA.

A.	WORKS	

WAYNE, PA.

R.	WOLFE	

For changes in this distribution list, contact D. Patten, M.V. Release and Configuration.

Company Confidential

V300 SYSTEM

PRODUCT SPECIFICATION

1994 2382

UNISYS

ENTRY-MEDIUM SYSTEMS GROUP

ORANGE COUNTY

UNISYS

Entry-Medium Systems Group
Orange County

1994 2382

V300 SYSTEM

Company Confidential

PRODUCT SPECIFICATION

REVISIONS

REV LTR	REVISION ISSUE DATE	PAGES REVISED, ADDED, DELETED OR CHANGE OF CLASSIFICATION	PREPARED BY	APPROVED BY
F	1/24/89	Updated Sec. 3, RAM Characteristics P. 12, MTBF to 5,500 hrs based on 150 systems over 12 month period per REE 98727B	S. Solomon S. Solomon	V. McClelland

1994 2382

Burroughs Corporation

COMPUTER SYSTEMS GROUP
PASADENA PLANT

V300 SYSTEM

COMPANY CONFIDENTIAL

PRODUCT SPECIFICATION

REVISIONS

REV LTR	REVISION ISSUE DATE	PAGES REVISED, ADDED, DELETED OR CHANGE OF CLASSIFICATION	PREPARED BY	APPROVED BY
A	10/5/84	Initial Issue	N. Fleming	E. Keeley R. Okimoto C. Miller M. Emm L. Wasserman S. Davis
B	6/2/85	Sec. 3.1 - MTBF Changed to 750 hours. Changed MCPX to MCP1.0 throughout text.	N. Fleming	
C	6/10/85	Provided description of the RAM Disk feature and description of B4900 to V-Series upgrade kits. Added Appendix B on RAM Disk Performance.	N. Fleming	E. Keeley
D	8/23/85	1) Changed RAM Disk to QWIK Disk. 2) Updated list of peripherals for connection to V300.	N. Fleming	E. Keeley
E	12/17/85	Revised Appendix B ECN 50172	N. Fleming	M. Emm B. Patterson S. Davis E. Keeley R. Okimoto

PS90

1994 2382

Burroughs Corporation

COMPUTER SYSTEMS GROUP
PASADENA PLANT

V300 SYSTEM

COMPANY CONFIDENTIAL

PRODUCT SPECIFICATION

REVISIONS

REV LTR	REVISION ISSUE DATE	PAGES REVISED, ADDED, DELETED OR CHANGE OF CLASSIFICATION	PREPARED BY	APPROVED BY
A	10/5/84	Initial Issue	N. Fleming	E. Keeley R. Okimoto C. Miller M. Emm L. Wasserman S. Davis
B	6/2/85	Sec. 3.1 - MTBF Changed to 750 hours. Changed MCPX to MCP1.0 throughout text.	N. Fleming	
C	6/10/85	Provided description of the RAM Disk feature and description of B4900 to V-Series upgrade kits. Added Appendix B on RAM Disk Performance.	N. Fleming	E. Keeley
D	8/23/85	1) Changed RAM Disk to QWIK Disk. 2) Updated list of peripherals for connection to V300.	N. Fleming	E. Keeley
E	12/17/85	Revised Appendix B ECN 50172	N. Fleming	M. Emm B. Patterson S. Davis E. Keeley R. Okimoto

PS90

TABLE OF CONTENTS

1 FUNCTIONAL DESCRIPTION

1.1 OVERVIEW

The V300 System is essentially the B4900 architecture with expanded memory capability. It will execute an enhanced medium systems instruction set and run under MCP/VS operating systems. The V300 will also run under MCPIX for some applications requiring B4900 emulation (e.g., in a shared environment with B29/39/4900 Systems also running under MCPIX). It will also support the QWIK Disk feature under MCPIX. Initial release of the V380 will be with MCPIX ASR 7.0.

The V300 is expected to be competitive with the IBM 3033S/3032/168/158/4341-2 systems, memory sizes being equivalent, and in COBOL environments.

The V300 Processor/Memory performance is equivalent to that of the B4900. The Memory capacity is 8 times that of the B4900.

Packaging and physical size will the same as the B4900 but styling will be different.

Reliability is expected to be the same as a similarly configured B4900 system.

Performance models will be offered to compare with the B3955, the B4925 and the B4955. These will be the V310, V340 and V380 models respectively.

The potential for additional throughput capacity under MCP IX is made available using the QWIK Disk feature. This will permit part of the main memory to be treated as a fast disk device.

1.2 HARDWARE DESCRIPTION

1.2.1 MAJOR SUBSYSTEMS

Memory Subsystem

Presuming fully populated boards, there are 1.25* or 5 Megabytes per memory module. The following combinations are valid:

4 modules - 5 megabytes*
2 modules - 10 megabytes
4 modules - 20 megabytes
8 modules - 40 megabytes

* This is found in the V310-1 only; it consists of four 1.25 MB storage modules.

As in the B4900 models, the processor's performance is relative to the number of memory cards (up to four).

2 modules - 95 percent of full performance
4 or 8 modules - full performance

Note- In B4900 emulator mode, memory utilization, as seen by MCPIX, will be limited to 5 megabytes. The remaining memory may be allocated to QWIK Disk and accessed using I/O operations.

I/O Processors

The minimum system requires at least one IOP module. This configuration will support up to four DLP bases (nominally a 32 DLP capacity). The second IOP module will support an additional four bases. The V340 is limited to one IOP module.

Each IOP is capable of an 8 megabyte data transfer rate. The effective transfer rate (with connect/disconnect overhead) is about 6 megabytes per second which is restricted by the present DLP design. The second IOP has the same characteristic. The cumulative bandpass is twice that of one

IOP. The IOP also contains the required firmware to support the QWIK Disk function.

1.2.1 MAJOR SUBSYSTEMS (Continued)

The upper limit of channel capacity (DLP quantity) is 64, regardless of space and power considerations.

QWIK Disk consumes Channel 40. No other devices may be assigned to this channel.

DLP's

Each IOP can accommodate four MLI connections. This will provide connection to four DLP bases per IOP. The I/O cabinet contains up to three DLP bases.

Since the use of two IOP's would allow connections of up to eight DLP bases, two more I/O cabinets (expansion cabinets) can be added to provide space for all DLP's.

ODT

The primary ODT is driven by the Maintenance Processor via the Console DLP. In this mode, the ODT is shared between maintenance (off line) use and operating system use. A second ODT may be connected via the Uniline 2B DLP and a direct connect line.

Cabling design allows up to 50 feet of ODT cable to be utilized so that neither the primary nor the secondary ODT are restricted to placement on top of the I/O Cabinet.

1.2.2 PERIPHERAL DEVICES

A list of devices which have been considered for qualification and support on the V300 is shown in Appendix A.

1.3 APPLICATION AND SYSTEM SOFTWARE

The V300 System is designed to be compatible with previous Medium Systems products and to support previous languages and application programs.

The V300 will operate only with MCP/VS 1.0 (and later) and MCP IX (ASR 7.0 & later releases). Operation with MCP IX is limited to 5 megabytes of memory capacity when shared with B29/39/4900 series systems. In this case, the B29/39/4900 series system must also be using MCP IX.

Any application may use the QWIK Disk feature, providing its files can be reconstructed should a loss of power occur.

1.4 SERVICE FEATURES

The Maintenance Subsystem provides the means to monitor and regulate system functions, and also the means to check and isolate system malfunctions to field replaceable units (FRUs). (See also Section 3.2 - RAM Design Elements.)

In order to achieve the above, both on-site and remote diagnostics will be provided which are compatible with previous medium systems service features.

On-Site Maintenance

Tests on diskette media and procedures will be provided to allow the Field Engineer to use the Maintenance Processor in diagnosing the fault.

Remote Maintenance

The remote port of the Maintenance Processor communicates through the user acoustic modem to a remote support service center.

The utilization of remote support capabilities will provide second level diagnostic expertise for problems not solved by means of state verification and module diagnostics.

1.4.1 DLP's

The DLP's will be maintained using the Maintenance Processor. The maintenance philosophy for DLPs is card replacement.

1.4.2 POWER MODULES

Component and/or subassembly replacement is not planned for power module repair in the field. The recommended procedure is replacement of the power module after it has been determined that the power module is defective. (Test and field documentation will not support component or subassembly repair/replacement.)

1.4.3 SUPERVISORY CIRCUITS

Replacement is at the card assembly level. (However, Test and field documentation includes information on the supervisory circuits to enable the Customer Service Engineer to maintain this hardware to the component level.)

1.4.4 AC CONTROL AND DISTRIBUTION HARDWARE

Test and field documentation is provided with the AC control and Distribution hardware to assist the CSE in maintaining this hardware to the component level. A troubleshooting procedure and flow chart will be provided.

2 V300 SPECIFICATION/PERFORMANCE

Performance of the V300 can be considered in the following context:

under MCP IX
under MCP IX using QWIK Disk
under MCP/VS 1.0
under MCP/VS 1.0 using QWIK Disk

2.1 V300/MCP IX

In this mode, the system will behave in a manner identical to the B4900. Performance data for the B4900 applies here.

2.2 V300/MCP IX/QWIK Disk

In this mode, the additional feature of a fast pseudo disk device can be used to speed up throughput. Generally, the performance of any application(s) will improve to the extent of the I/O's that can be done to the QWIK Disk. This will be a function of the files that can be accommodated in the space available.

At maximum memory of 40 megabytes, if 5 megabytes are allocated to MCP IX; 35 megabytes will be available for QWIK Disk operations. If less than 5 megabytes can be allocated to the MCP, then the additional difference may be added to the QWIK Disk.

2 V300 SPECIFICATION/PERFORMANCE (Continued)

QWIK Disk Peripheral Summary

Table 1 outlines performance-related characteristics for QWIK Disk and other peripherals, including REACT's solid-state QWIK Disk. Sizes are based on 100-byte interlaced.

	QWIK Disk	5N	3680 9494-12	659-2 9494-10	REACT	206
Capacity (MB)	< 40	5.5 (su) 21 (eu max)	434 (actr) 868 (drive)	482 (actr) 964 (drive)	2 - 128	112 (drive)
Transfer Rate (MB/sec)	1.5	.656 (1 X 2)	3	1.2	4 (?)	1.2
Avg. Seek	0	0	16 MS	22 MS	560 NS	25 MS
Avg. Latency	0	5 MS	8.3 MS	8.3 MS	0	8 MS
Avg. to Data		5 MS	24.3 MS	30.3 MS		33 MS
Connectivity (Exch)	1X1	8X20	4X16 (Dual Host)	8X16	4X	8X16

TABLE 1

2 V300 SPECIFICATION/PERFORMANCE (Continued)

QWIK Disk Performance Summary/Projections

Table 2 provides QWIK Disk performance highlights. Appendix B documents in more detail the results of the QWIK Disk benchmarks performed thus far. The various configurations for QWIK Disk and non-QWIK Disk are also listed. All tests were run with empty peripherals and otherwise "antiseptic" environments.

For consistency, performance improvements are expressed as "factors" and are computed as:

Factor = Old Time / New Time

Due to the limited availability of 5N Disk, most comparative measurements were against 206/207-base systems. Since 206/207 head movement was minimized, 5N Disk should perform about two times these figures.

See Appendix B for more extensive QWIK Disk performance information.

PERFORMANCE HIGHLIGHTS

- QWIK Disk access is 5.5 over 5N and 9 over 206 (with little head movement).
- AVG. QWIK Disk I/O's cost about 2.4 milliseconds with minimum transfer time.
- Compiler rate ranges improve significantly with QWIK Disk

  COBOL9: 1100 - 2100 Records per minute
  SPRITE: 2100 - 2500 Records per minute

- QWKMEM (MCP overlays) versus QWIK Disk resident overlaying shows minimal improvement.
- System throughput can be improved by factors up to 1.6 with a QWIK Disk-Resident MCP versus a 206 MCP.
- Single-thread I/O-bound DMSII and ISAM tasks improve by factors of 1.3 to 4.7 with low buffering.
- Heavy transactions processing mixes improved by 1.3 to 4.0 with all or partial sets of files (databases) in QWIK Disk.
- The base MCP IX 7.0 will consume 8.1 MB, if QWIK Disk resident.
- QWIK Disk optimizes I/O's; it does not eliminate I/O's; it is still slower than memory buffering.

TABLE 2

2 V300 SPECIFICATION/PERFORMANCE (Continued)

2.3 V300-MCP/VS 1.0

Present outlook is for the performance to be equal to that of MCP IX under equivalent workloads.

2.4 V300-MCP/VS 1.0/QWIKDisk

The composite performance in this environment is expected to be similar to that under MCP IX.

3 RAM CHARACTERISTICS

3.1 RAM ATTRIBUTES

3.1.1 RELIABILITY - MAINFRAME

Reliability goals for the typically configured V300 mainframe have been derived from the 1984 CARES for the B4900. The V300 will specify the ET1100 (MTBF spec'd at 10,000 hours) instead of the B4900's MT983 (MTBF spec'd at 1800 hours) as the primary ODT. Since CARES data for the mainframe includes the ODT but does not give an indication of the type of ODT (MT983, TD830, ET1100, etc.) or quantity (1 or 2) actually used, it is not possible to subtract out the effect of the ODT MTBF from the mainframe MTBF. It is expected that the V300 with the ET1100 ODT will exceed the goal based on the B4900 CARES.

MTBF is : 5,500 HOURS.

NOTE: MTBF has been updated based on field performance of 150 systems over a 12 month period.

3.1.2 AVAILABILITY

The assumption for availability is that the system is operated 6760 hours per year (130 hour, 6 day week). It is assumed that an FE takes 2.5 hours to respond and repair the system.

All time for response and repair comes from the normal operating time.

Mainframe only	99.6%

3.1.3 MAINFRAME MTTR

The average mainframe mean time to repair is 1 1/2 hours distributed as follows:

Processor/IOP	1.8
Memory (one module)	1.5
Power/Cooling	1.0
Maintenance Subsystem	2.0
DLP Subsystem	1.6

The tabulated repair times for peripherals are determined from the stated MTTR in the appropriate Product Specification.

3.1.3 MAINFRAME MTTR (Continued)

The mainframe MTTR is itself the weighted average of the repair times of its component elements. For the DLP subsystem, the MTTR for the Typical System configuration has been determined from that specified in IOSO PDA of January 1981.

The computed MTTR includes the time to restore the system to full operation, combining times for diagnosing the problem, replacement of the faulty card, and verification of the fix. The expertise available at the Remote Diagnostic centers will be used for the estimated small percentage of failures that cannot be diagnosed by the tools at a site.

3.2 RAM DESIGN ELEMENTS

3.2.1 PROCESSOR MAINTAINABILITY

The V300 is designed for maintainability by inclusion of hardware and firmware specifically for maintenance within each system module, in addition to the System Maintenance Controller (SMC) resident in the Processor/Memory cabinet, and the independent Maintenance Processor (MP) resident in the I/O Cabinet. Maintenance hardware within each module includes both shift chains and error detection circuitry.

Shift Chains

All internal state is accessed for maintenance purposes through data paths called shift chains. The Processor, Memory Control, Memory Storage and IOP contain shift chains. Internal state may be directly accessible "surface" state, such as shift registers, or other shiftable logic elements; other internal state is termed "hidden" state, such as Control Store or scratchpad RAM, which are indirectly accessed. Such hidden storage elements are accessed through the directly shiftable logic.

The ability to access all internal state is required for high coverage diagnostic test; this also enables the internal state of the processor modules to be set up and displayed via the Maintenance Processor and Operator's Display Terminal (ODT). The capability of recording a trace of the processor

while executing instructions is also provided.

3.2.1 PROCESSOR MAINTAINABILITY (Continued)

Additional shift chains and comparators provide for generating stop conditions on which clocks are disabled, freezing the modules for examination. This conditional stop logic complements the error detection circuitry within the Processor modules.

Error Detection Circuitry

The parity of the control store is checked in all modules that are microprogrammed. Additionally, the Execute Module verifies that the contents of its redundant control registers match.

Within the Memory Storage modules, special logic has been added to verify memory data and correct single-bit memory errors transparent to the rest of the system. Special logic can also enable testing of this error-correct circuitry. The means to reconfigure the memory storage subsystem in event of failure of one Memory module or of one bank of one module, is provided.

The following errors are typical of those which are detected during the FETCH Phase:

1. Improper literals (undigit in length, length too long, invalid data type)

2. Invalid Indirect Field Length

3. Illegal undigits in index registers or indirect addresses

4. Undigits in resolved AF or BF (non-test and non-literal)

5. Invalid opcode

6. Code limit error where FETCH attempts to read the next consecutive instruction beyond the program limit.

7. Indirect address limit errors

3.2.1 PROCESSOR MAINTAINABILITY (Continued)

The following errors are typical of those which are detected during the Execute phase.

1. Undigits in addresses (READ/WRITE CONTROL will detect any undigits in those addresses sent to it and set the appropriate STATE Toggle. However, the XM detects undigits in addresses in all other cases)

2. Undigit arithmetic

3. Invalid I/O Descriptor

4. Literal not allowed

5. Invalid branch addresses (not Mod 2, improper undigits, limit error)

The detection of any software errors is reported to the MCP. The detection of any hardware errors is reported to the MP.

3.2.1 PROCESSOR MAINTAINABILITY (Continued)

SNAP Overview

SNAP is defined as the process of capturing and storing the state of a machine. The purpose of SNAP is to obtain a picture of the Processor at the occurrence of an error, thus providing necessary information to assist in debugging of a hardware or software related problem.

The V300 has three levels of SNAP, defined as:

Operational SNAP

Diagnostic SNAP

Maintenance SNAP

- Operational SNAP

Operational SNAP is always performed for hardware errors (physical hardware or microcode). This SNAP results in the disabling of all System Clocks in an orderly manner, with no attempt made to restart System operation. A SNAP Picture will be taken after System Clocks have been stopped and written to the Memory location allocated for the SNAP Picture.

Operational SNAP can be summarized as always occuring on hardware/microcode failures only. It should never occur as a result of program problems in either the MCP or User programs.

- Diagnostic SNAP

Diagnostic SNAP differs from Operational SNAP in that this level is entered as a result of failure to isolate a problem using Software Trouble Analysis tools, such as dumps.

Diagnostic SNAP is optionally performed, in the V300 as in the B4900, as a result of those program error conditions which would unconditionally have caused a SNAP in previous Medium Systems. SNAP's occuring in this mode will result in System operation being interrupted, a SNAP Picture being

taken, and System operation being re-instated as in previous Medium Systems.

3.2.1 PROCESSOR MAINTAINABILITY (Continued)

- Maintenance SNAP

An operational or diagnostic SNAP Picture will not always provide the information necessary to properly diagnose a problem. The ability to obtain a Picture of the System as close as possible to the occurence of the failure is necessary and the Maintenance SNAP provides this capability. Selection of the conditions which cause a Maintenance SNAP Picture is made using the Processor's conditional stop logic. The Maintenance SNAP halt may optionally be graceful so that System operation can be restarted following the SNAP event or immediate, in which case a halt load is required.

Maintenance Processor (MP)

The Maintenance Processor (MP) is a microprocessor-based system that controls the following devices and interfaces: one ODT, two 5 1/4 inch minidisk drives, an interface to the Console DLP, the UIO test bus, a Remote Link port, and one host port to the SMC.

The SMC accepts descriptors from the MP, interprets them, and performs the operation requested. The SMC allows the MP to perform system level functions such as:

- System Initialization
- Mode Control
- Display Panel Emulation
- System Maintenance
- System Monitoring

This is by controlling clock and manipulating state of the Processor Memory Modules under control of programs executing in the Maintenance Processor.

3.2.2 POWER SUBSYSTEM MAINTAINABILITY

The following indicators and controls are provided to facilitate maintenance of the power and cooling subsystems:

1. DC Voltage Fail Detection and Indicators

Each of these indicates the status of a specific DC voltage within the system. One is provided for each of the following voltages:

+5V Processor/Memory Cabinet

+5V I/O Cabinet

+12V I/O Cabinet

-12V I/O Cabinet

During normal operation, each DC voltage is tested for the following conditions:

Undervoltage (UV) : The magnitude of the DC voltage may be too low at one or more locations within the system to ensure correct operation.

Overvoltage (OV) : The magnitude of the DC voltage may be too high at one or more locations within the system to ensure correct operation.

Catastrophic Overvoltage (COV): The magnitude of the DC voltage may be high enough at one or more locations to cause component damage. Unlike UV and OV, this condition cannot be disabled. Subsequent power up is not possible until the circuit breaker turned off, then on again.

When any of these conditions occur, the DC fail indicator for the voltage(s) in error will light and the power subsystem will shut down. No differentiation is made among the three error conditions.

When two or more modules are paralleled for one common DC voltage, no differentiation is made to indicate which of the power modules caused the voltage failure condition.

3.2.2 POWER SUBSYSTEM MAINTAINABILITY (Continued)

2. Cooling Subsystem Fail Detection

When the ambient air temperature (measured at the plenum chamber) exceeds 42 + or - 2 degrees Celsius, or if one or more of the fans or blowers stops turning, this indicator will light and a high active signal, ALOT, is sent to the processor. About 40 seconds later, the the system will power down.

3. PROM Address indicators, Branch indicator,

Single Pulse Switch, Single Pulse Push Button

These features, when used with the information provided with the schematic diagram, facilitate maintenance of the supervisory card to the component level.

Since the supervisory card is a PROM based finite state machine, the PROM address gives a unique and complete indication of the current state. Future state is predetermined by the test conditions and is indicated on the detailed flow chart provided with the schematic diagram. In the case of a branch-on-test-condition block in the flow chart, the branch indicator LED shows the state of the tested input and thus whether the branch is to be taken.

The single pulse switch, when in the "maintenance" position, allows the supervisory card state machine to be single-pulsed with the single pulse push button. The CSE can then step through the supervisory card sequencer flow and, with the aid of the hardware and documentation features just described, can troubleshoot the supervisory card to the component level.

4. Disable Switches

A switch is provided to disable the sensing of OV and UV on each of the DC voltages. A separate switch is provided for each voltage. These switches allow the CSE to troubleshoot the power subsystem by preventing nuisance power down actions while adjusting voltages, running voltage margins, etc. COV is not disabled by these switches.

3.2.2 POWER SUBSYSTEM MAINTAINABILITY (Continued)

A switch is provided to disable the distribution of the POWERUPOK signal to the system. This switch is used to prevent the processor/memory and I/O circuits from doing anything while the CSE is troubleshooting the power subsystem.

5. Additional Features: Voltage and Temperature Warning

In an effort to provide the customer and the CSE with some information concerning the environment, circuits are provided to monitor the peak value of the AC input voltage and the ambient air temperature.

If the peak voltage of the AC input voltage is less than 85 + or - 2% of the nominal value, a high active signal, VWRN, is sent to the Processor. Power down is NOT imminent unless the AC input voltage decreases further to a point where the power modules can no longer operate properly (AC less than 80% of nominal). In that case, power down is initiated through the DC voltage monitoring circuits described previously.

If the ambient air temperature, measured in the air plenum chamber, increases beyond 37 + or - 2 degrees Celsius, a high active signal, TWRN, is sent to the processor. Power down is NOT imminent unless the ambient air temperature increases to a point where power down is initiated through the cooling subsystem monitoring circuit described earlier.

These two signals set bits in the processor result descriptor which are tested by the MCP. Entries are made for either condition in the maintenance log along with a time/date stamp. These entries may allow the CSE to correlate other mainframe and peripheral errors to climatic or electrical environment disturbances.

3.3 RAM SUPPORT PLAN

Elements of the plan for maintenance of the Processor/Memory are grouped as follows:

Maintenance Flow Diagrams
High Level Processor Tests
Processor Tests
IOP Pre-Tests
Self-Tests (module resident confidence tests)
Diagnostic Module Tests (path tests)
CRAM Verification Test
Low Level Hardware Tests
I/O Subsystem Tests
Memory Tests
Margin capability
Maintenance Kit
Microfiche Reader (this item must be provided by the Field Engineering organization)

3.3.1 CONTROL STATE TESTS

MAINTENANCE FLOWS

The maintenance flows provide guidance as to how the various maintenance tools are to be applied.

HIGH LEVEL TESTS FOR THE PROCESSOR

These include control-state tests of all instructions; a worst-case test for the pipe-line machine; and a set of normal-state confidence tests.

PROCESSOR TESTS

The processor tests consist of the following suites of test programs:

PRETEST(1-9), ALLORDERS(1-8), and DOUBLECHECK(1-4)

These confidence tests contain processor instruction test cases of increasing difficulty. Each control state test routine is loaded into memory from minidisk via the MP's shift chain path into main memory.

IOP PRE-TESTS

These routines use the IIO and RAD operations in addition to the subset used by the processor tests, and initiate basic I/O operations to the IOP and I/O subsystem. Data, result descriptors, and scratch-pad address (RAD) are checked.

MEMORY TESTS

A complete diagnostic test of all system memory is provided. This test routine executes in the V300 Processor. By means of special microcode, a localized region of memory can be verified to be good, prior to loading processor or memory test routines.

3.3.2 MODULE CONFIDENCE TESTS

These tests dynamically verify the operation of each module of the central system and the interfaces between modules. Test microcode executes in the Fetch, Execute, IOP, and SMC modules, and in the Maintenance Processor itself.

A subset of the tests within the Fetch and Execute modules check the interfaces to each other and to the Memory module, and verify the path through the Interface Module to the Memory module(s). These tests are brought in from minidisk and executed under control of the CSE.

Self tests for the MP are invoked upon power up. The MP self-test is executed whenever its program memory is reloaded from diskette. A failure in these tests, or an error detected during system operation, initiates the diagnostic procedure.

In addition to the diagnostic self test incorporated in the PROM memory of the MP, there is a standalone test program which is brought in from minidisk that executes diagnostics for all the MP interfaces and attached devices.

3.3.3 DIAGNOSTIC MODULE TESTS

The primary tool for diagnosing failures are module tests which detect single static faults. These are hand generated path tests. These tests exist for all processor modules. A failure detected by one of these tests causes a message on the ODT with a recommendation of which card or cards to replace.

3.3.4 LOW LEVEL HARDWARE TESTS

The basic ability of registers on shift chains to hold ones and zeros, and to be cleared and shifted, is verified. The shift chains are then utilized to write and read hidden state, testing RAM address lines and data cells. These tests are executed via the Maintenance Processor.

3.3.5 I/O SUBSYSTEM TESTING

Confidence, diagnostic, and maintenance test programs plus associated driver programs are available to assist the operator or Customer Service Engineer (CSE) in the maintenance of the DLP's and peripheral paths. DLP diagnostics can be on-line or off-line.

The Device Confidence and Maintenance tests written in Peripheral Test Language are run on-line by a Peripheral Test Driver and can be used by an operator or CSE to determine if further maintenance attention (by CSE) is needed.

The PTL tests for card reader, magnetic tape, and disk devices can be run stand-alone without the MCP when the type of failure precludes on-line testing.

The Device and DLP Maintenance programs may be used by the CSE to isolate a fault to one of the following areas:

Message Level Interface (MLI)
DLP Base Module
DLP
Peripheral device

If a DLP is suspected, the Customer Service Engineer can use the available documentation in the UIO T&F Package to determine the appropriate diagnostic routine for the DLP in error. Diagnostics unique to each DLP type are provided. Each diagnostic is in the form of a data file stored on a mini disk and is executed by a common DLP Test Bus program. Through use of these diagnostic routines, the CSE can determine which of the lowest replaceable units shall be replaced to effect a repair of the module.

The common front end card is replaceable at the card level. If a fault is traced to the UIO base module, either the Maintenance Card or the Distribution Card is replaceable at the card level.

In the case of QWIK Disk, reads and writes are written from/to Channel 40 (the QUIK Disk). In the event of a failure, the IOP path tests and memory test are used.

3.3.6 MAINTENANCE/SPARES KITS

A maintenance kit will be provided with the System which will supply the necessary accessories (card extenders, etc.) to the required for maintenance. One is required per site.

Spares Kits are being made available to provide recommended spares to the Field Engineering District.

3.3.7 PREVENTATIVE MAINTENANCE

The following preventative maintenance tasks are required 4 times a year in an office environment. The CSE should be able to perform them in no more than 3/4 hour.

1. Clean/replace air filters
2. Clean screens
3. Check dust buildup in system

3.3.8 MARGIN CAPABILITY

The margin capability of the V300 is +/- 5% on frequency and voltage (measured at worst case chips). These margins are not applied simultaneously.

Frequency Margin

With the voltage set to the nominal of 5.05 at the backplane bus bar, the system should run with cycle times of 104, 110 and 116 nanoseconds.

Voltage Margin

With the frequency set to the nominal of 110 nanoseconds, the system should run at 5.20, 5.05 and 4.90 volts measured at the backplane bus bars. This margin takes into account a 100 millivolt difference across the board and a 100 millivolt peak to peak power supply ripple.

The +/- 12 volt supply drives only the DLP subsystem and the Maintenance Processor. With the frequency set at 110 ns and the 5V supply at 5.05V at the DLP-0 backplane, the system should function properly at any combination of the +12V and -12V margins shown below.

12V margins measured at connection to DLP backplane:

	High	Low
+12	+12.5V	+11.5V
-12	-12.5V	-11.5V

3.4 FAULT TOLERANCE

The typical configuration allows for the following:

- loss of a channel to tape or disk, will result in some performance loss but will still permit processing to continue due to I/O subsystem redundancy.

- in a 2 IOP configuration, if the paths are set up with one behind each IOP, loss of an IOP may be offset by processing through the four remaining MLI paths.

- loss of a bank of memory in a Memory Module or loss of a whole Memory Module can be overcome by reconfiguring Memory, via the Maintenance Processor to remove that element. A halt load will be required.

- some timing-related failures can be temporarily overcome by reducing the Processor clock frequency via the Maintenance Processor until the FE can correct the problem.

In a shared systems environment, up to four systems may access the same files and back up each other in the event of a failure in any one system. Note - QWIK Disk files cannot be shared.

QWIK Disk must be considered a volatile device. Its use must be limited to files than can be restored in the event of power loss or double bit error.

4 MIGRATION AND COEXISTENCE

4.1 HARDWARE

INSTRUCTION SET COMPATIBILITY

The instruction set for V300 is described in the V Series Instruction Set specification (PS 1987 1045). This is an enhanced version of the B4900 set. With these instructions the V300 can address more than 5 million bytes.

The V300 will execute the B4900 Instruction Set under MCPIX provided the appropriate B4900 firmware is loaded.

DATA

The V300 will support all data types of the B4900 (i.e., the same as B4800 with the exception of internal stored ASCII and variable length floating point). The results of undigit arithmetic will not be compatible with the B4800 but undigit arithmetic operations will be detected.

4.2 SOFTWARE

Programs running under MCPIX ASR 7.0 will operate in a fully compatible manner with the B4900.

QWIK Disk functions as an I/O device and, as such, is not part of the software environment.

Existing user programs will be supported without need of recompilation under MCP 1.0. Users will have to recompile to take advantage of new features. At a future release, users who wish to recompile will be able to take full advantage of the increased memory supported by MCP 1.0. (for example, greater than 1 MD user programs will be supported.)

Shared systems must be using the same MCP. Systems using different MCPs can communicate through BNA.

COBOL and WFL users must recompile to be able to take advantage of >99 mix environment.

There will be a warning message generated on all uses of slash parameters indicating that slash parameters will be deimplemented in a future release. The use of WFL style parameter passing to tasks will be allowed on MCP 1.0 and all future releases of that product.

Customers that use time accounting statistics recorded in the Run Log for significant business purposes (e.g., service bureaus) should be informed to expect slight changes to a programs chargeable profile under MCP 1.0. Certain MCP functions which prior MCPs were unable to charge against the requesting program are now correctly charged. Time accounting under MCP 1.0 is considerably more accurate than that provided by an previous MCP.

MCP 1.0 does not support the obsolete "Remote SPO" capability.

The most significant potential compatibility impact of MCP 1.0 on customer software is caused by the seemingly trivial expansion of the two-digit mix number to a four-digit task number. Customers use of larger memories necessarily requires the capability to schedule and execute more than 98 tasks, which thus requires the expansion of this data element. A very small percentage of user-written programs (most commonly categorized as in-house utilities) may be impacted by one or more of the following:

-- All log files (RLOG, SLOG, MLOG) records which included a two-digit mix number have been slightly reformatted to accomodate a four-digit task number. All user written programs which read these files (including unbound RLGOUT, SLGOUT, and MLGOUT), will require minor modifications.

-- Programs which acquire console output message text from any source (SLOG file, SPOM BCT, etc.) and depend on specific locations for key words or values will require slight modification. However, programs which employ generalized text-scanning techniques to evaluate these messages will be unaffected, unless they specifically expect to find only a two-digit mix number. Although the text of all console output messages remains identical to

that provided by MCPIX ASR 6.8, it may be shifted to the right one or two positions due to the expanded task number which precedes it.

-- Programs which use the "Mix Table" communicate (BCT 214/6x) will need to be modified sometime during a supported transition period. Responses to this BCT include a two-digit mix number. A new BCT has been implemented in MCP 1.0 which provides the same data, but reformatted for a four-digit task number. Programs which use the old BCT must be modified to use the new BCT. A transition period is provided in the ASR 6.8 (and later) versions of MCPIX, and MCP 1.0, and must be completed before implementation 1.0. Both MCPIX (6.8 and later) and MCP 1.0 (and later) provide a new supported BCT which identifies the MCP currently running. This can be used to determine which variation of the "Mix Table" BCT to use. Thus, affected programs may be modified before MCP 1.0 is implemented. Further, MCP 1.0 will support the old style Mix Table BCT if the system is Cold Started with a MAX-TASKS value of less than 100. Customers that have affected programs can run them under MCP 1.0 as long as they specify less than 100 for MAX-TASKS.

-- Most WFL programs must be recompiled sometime during a supported transition period. Beginning with the ASR 6.8 release of the WFL compiler, generated WFL code files are fully compatible with both MCPIX and MCP 1.0. All code file generated by any WFL compiler version preceding the ASR 6.8 release are potentially incompatible with MCP 1.0. MCP 1.0 will also support pre-6.8 WFL programs if the system was Cold Started with a MAX-TASKS value of less than 100. This support will be withdawn in a future release. Thus, all WFL programs must be compiled with a 6.8 (or later) release of the compiler sometime between the implementation of WFL 6.8 and a future MCP release.

-- Some programs might determine their mix number by extracting it from the ID of a "work file." This practice should be rare, since the MCP has always supported a BCT which provides this information more elegantly. In MCP 1.0, the two positions of a Work File ID which used to contain a two-digit mix number now contain an encoded task number. Programs which extract mix numbers from Work File IDs may experience problems with their use of that data. However, one again, if the system is cold started with a

MAX-TASKS value of less than 100, all imaginable uses of that data should work. Thus, a transition period is provided in MCP 1.0. New features planned for future releases (TASKING) will invalidate this practice.

V Series systems running MCP 1.0 will require not more than 20% of the total system memory for the MCP in addition to the memory required to support the expected work load. The memory actually in use by MCP 1.0 at any given moment will vary considerably depending upon the actual workload presented.

4.3 SYSTEM CONFIGURATION COMPATIBILITY

The V300 can be loosely coupled via the SSP with other V Series systems running MCP/VS 1.0. The V300 can be shared with B29/39/4900 Systems running MCPIX provided the V300 is also running under MCPIX.

The V300 will support the DLPs and peripherals of the B2900/B3900/B4900 with the exception of the ICMD; there is compatibility with existing single system B2900/B3900/B4900 configurations.

Those peripherals which were connected to previous systems but are not listed in the Appendix, are not supported on the V300. Programs requiring those devices may need to be modified.

The QWIK Disk feature consumes channel 40, and as such, channel 40 cannot be used by another device.

Channel 40 can be accessed via the first IOP only in a two-IOP configuration.

5 PHYSICAL DESCRIPTION AND INSTALLATION REQUIREMENTS

5.1 PACKAGING

5.1.1 CABINETS

The V300 is housed in two adjoining cabinets, a Processor Cabinet and an I/O Cabinet, neither of which is stand alone (Figure 5-1). The Processor Cabinet contains the Processor, I/O Processor, Memory,and required power and cooling subsystem,

The I/O Cabinet contains up to three UIO DLP Bases, one or two 5 1/4 inch Floppy Disks, a Maintenance Processor, and required power and cooling subsystem. The I/O Cabinet supplies DC power to the minidisk drives.

For systems requiring additional DLP's or data comm lines, one or two Expansion Cabinets can be attached to the Processor Cabinet. The maximum configuration will accommodate up to eight DLP Bases.

The cabinet dimensions of each cabinet (Processor Cabinet or I/O Cabinet) with top, side and end panels are:

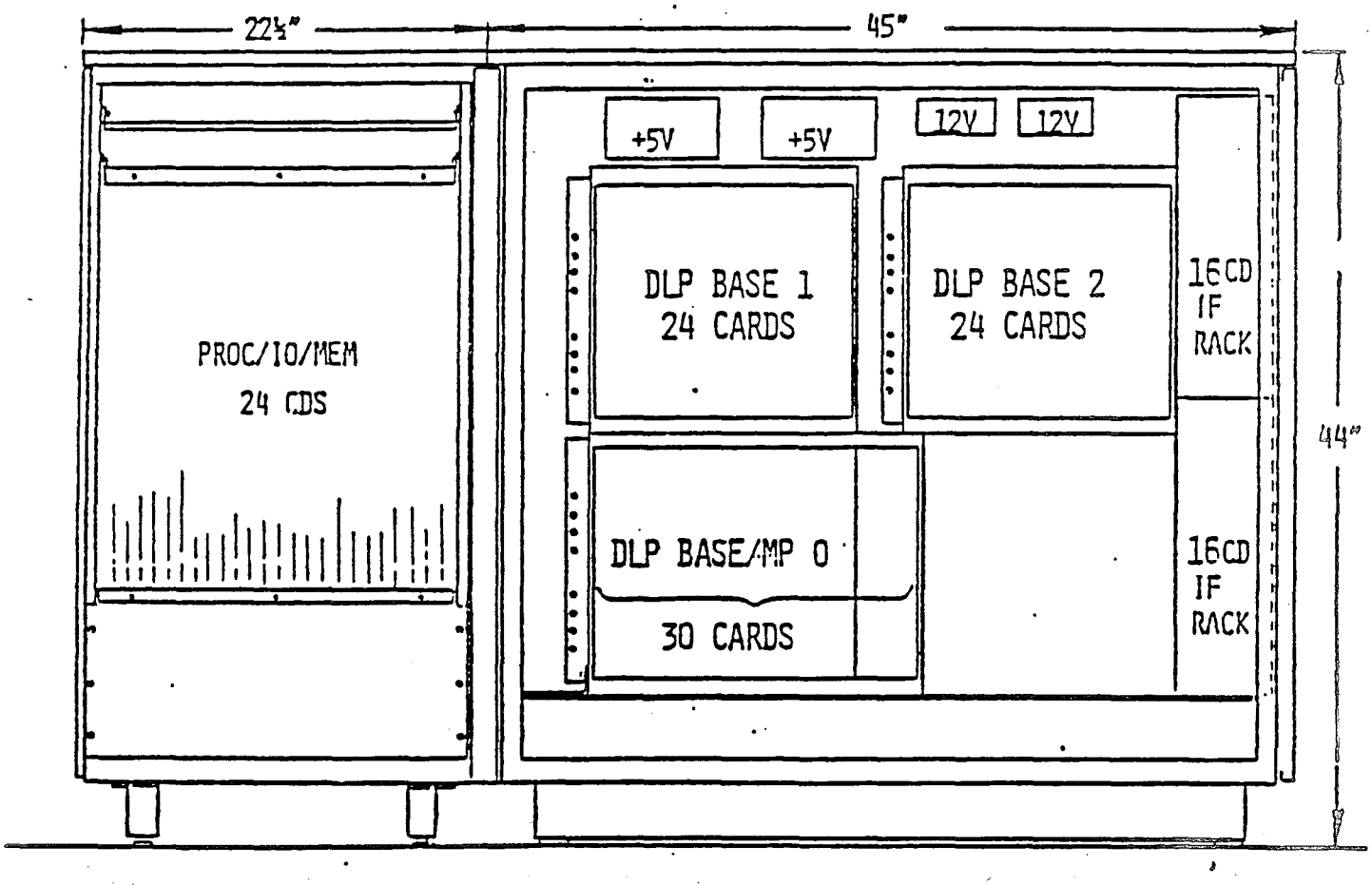
	PROCESSOR CABINET	I/O CABINET/EXPANSION CABINET
Length	22.5 inches	45 inches
Height	44 inches	44 inches
Width	29 inches	29 inches

FOOTPRINT

Processor & I/O Cabinet*	13.6 sq. ft.
Processor, I/O Cab., & Exp. Cab.	22.7 sq. ft.
Processor, I/O Cab., & 2 Exp. Cab.	31.8 sq. ft.

* Volume is 49 cu ft.

FIGURE 5-1 V300 CABINETS



5.1.1 CABINETS (Continued)

Logic Cards

The System utilizes two logic card sizes:

Processor logic card - 16 inches X 22 inches
DLP & MP logic card - 10 inches X 13 inches

The Processor card has been designed to accommodate up to 500 20-pin chips. The usable number of chip positions is restricted because of the etch routability.

The processor/memory will be built using multiwire technology and a minimum of sockets.

The DLP card is presently in production. Conventional printed circuit board technology is used for the DLPs and the Maintenance Processor.

Backplanes

Processor/Memory

The Processor/Memory backplane will be a wire wrapped assembly. which will accept up to 19 cards. Figure 5-2 shows the card layout for a fully configured processor.

DLP Base and MP

These backplanes are the same as those in B3900/4900 production.

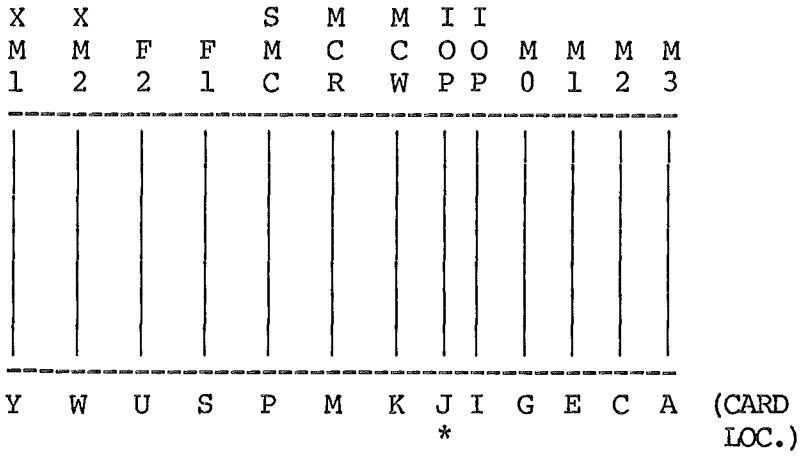
Peripheral Interface Rack

Model 1 V300 I/O and I/O Expansion Cabinets have provision for only card-edge style interface cards (paddle boards) and require host-end-adapter cables to interface with the "D" style Corporate standard shielded peripheral cables.

Model 2 V300 I/O and I/O Expansion Cabinets have provision for only "D" style interface cards and do not require host-end-adapter cables.

Both Models 1 and 2 comply with Corporate EMI standards.

FIGURE 5-2 CARD ASSIGNMENTS - PROCESSOR/MEMORY BP



* denotes second IOP

5.1.2 POWER MODULES

Primary power for the system logic is provided by multiple 5V 200A modules. These modules are interchangeable with modules from any qualified vendor.

An additional pair of modules is utilized to provide the +/- 12V supply.

5.2 SITE REQUIREMENTS

5.2.1 POWER REQUIREMENTS

The V300 requires AC power services distributed to each cabinet in the system via customer provided power conduits. The electrical requirements are indicated below:

	PROCESSOR CABINET	I/O - EXPANSION CABINET
Nominal Voltage	200 to 240	200 to 240
Current	40A	30A
Heat Dissipation	10000 BTU/HR	8800 BTU/HR

Additional details regarding power "quality" are provided in the V300 Installation Manual 1987 1219.

5.2.2 COOLING REQUIREMENTS

The Processor, Memory, and I/O subsystems with all options installed, dissipate approximately 5530 Watts (18840 Btu/Hr). The system is designed to operate in an ambient temperature range of 13 degrees Celsius to 40 degrees Celsius. Air conditioning is required if ambient air temperature cannot be maintained in this temperature range by any other means during system operation.

Water condensation on the hardware must be avoided.

The Processor cabinet has been designed to allow the direct entry of cooled air into the bottom of the cabinet. Use of this feature will result in more reliable operation (i.e. an MTBF figure beyond that specified).

5.3 INSTALLATION REQUIREMENTS

Some aspects of installation requirements and procedures are presented here; detailed instructions and customer provided environment parameters are contained in the V300 Installation Manual.

5.3.1 CABINET INSTALLATION

The Processor Cabinet and the I/O Cabinet are first removed from their individual shipping containers. The tops of each shipping container are removed and reassembled to provide a ramp to slide the cabinet from the pallet base. Shock mount snubbing within the I/O cabinet is removed.

A spacer positioned on the left side of the Processor Cabinet is used to bolt the cabinets together. Similarly, the Expansion Cabinet(s) is connected to the right side of the Processor Cabinet.

AC power input connections are made through the base of each cabinet. Peripheral signal cables pass through the base on the left side of the I/O Cabinet or Expansion Cabinet; the end panel skin is removed to access this area. Levelers for use on uneven floors are provided on each cabinet. (Reference the Installation Manual for a step by step procedure).

Placement of the cabinets should be such that a three-foot clearance is provided at the front and the back for maintenance.

No special tools are required for installation.

Note- The current version of the I/O Cabinet has card-edge connectors in the peripheral interface panel, and requires host cable adapters to interface to new peripheral cables featuring D type connectors at the host end. These adapters are identified in the V300 Systems Index.

-Installation Time

Installation time for a typical V300 System, from receipt of the two crated units (Processor and I/O cabinets), to power on and completion of self tests is estimated to be 8 working hours.

5.3.2 B4900 TO V Series UPGRADE

Both the B4925 and the B4955 can be upgraded to their V Series counterparts, V340 and V380 respectively. The upgrade involves the removal and replacement of the following:

- Skins
- Memory Modules
- Test and Field documents
- Diskette Set
- MCR card (if necessary - older units)

Installation Time:

The following are the maximum times for one experienced CSE to install and verify the upgrade changes.

Item	Maximum Time
Exchange Processor and I/O Cab. Skins	3 Hr
Exchange One Expansion Cabinet Skin set	1 Hr
Exchange MCR card and Memory (20 MB)	30 Min
Exchange MCR card and Memory (10 MB)	15 Min
Verify function of hardware (20 MB)*	1 Hr 30 Min
Verify function of hardware (10 MB)*	1 Hr 15 Min

*Consists of running path tests, function tests, allorders, and memory tests.

5.4 SHIPPING REQUIREMENTS

The preferred method of domestic shipment is via common carrier. For domestic shipment the shipping container is constructed on a pallet providing a 4 1/2 inch ground clearance. Additionally, casters fit into the skids of the pallet to permit its use as a production-floor dolly. The cabinets are shrouded in plastic, and foam pads cushion the corners to prevent movement within the container. The shipping container has the pallet base, four side walls and a top of sufficient strength to permit its use as a ramp. The cabinets are shipped with the fully loaded cabinet weight resting on slotted sections of vibration-damping foam rather than resting on its levelers.

For export shipment, the walls and top of the container are wood. All shipping containers are specified to meet the rough handling test procedures outlined by Corporate Standard B90-05.

The gross weight of the Processor Cabinet is 644 pounds; the gross weight of the I/O Cabinet is 806 pounds; the gross weight of the Expansion Cabinet is 719 pounds.

5.5 STYLING

The appearance of the V300 System will conform to the Corporate Industrial Design sketch.

6 ENVIRONMENTAL/PRODUCT SAFETY

6.1 ENVIRONMENTAL

The V300 System complies with Corporate Environmental Standards listed in the following sections.

6.1.1 ELECTRICAL ENVIRONMENT

The V300 complies with all applicable portions of Corporate Standard 1257 6013, Class 2.

The V300 is designed to operate in the presence of electrostatic discharges as specified in the current revision of the Electrical Environment Standard, ST 1257 6013 (Class 2). The applicability of the proposed Electrostatic Discharge Standard, not yet approved, is being investigated.

6.1.2 ACOUSTIC

The V300 does not comply with the Corporate Standard 1257 4703 for acoustic noise. The specified limit is 60 dBA, while the V300 produces 64.3 dBA. A corporate waiver has been granted.

6.1.3 MECHANICAL

The V300 complies with the mechanical requirements of Corporate Standard 1257 5999 for equipment weighing in excess of 500 lbs., except the cabinets will be mounted on levelers rather than casters.

6.1.4 CLIMATIC

The V300 complies with climatic stresses specified in Corporate Standard 1257 6005, Climatic Environmental, Office Class.

6.1.5 ELECTROMAGNETIC EMANATIONS

The V300 complies with the limits for Electromagnetic Emanations specified in Corporate Standard 1257 5718, Class A. In addition, the V300 will be verified as complying with the FCC regulations, Part 15. The V300 will be designed for VDE compliance. Certification by the VDE will not be obtained by Engineering.

6.2 PRODUCT SAFETY

The V300 is UL listed and CSA certified; it does not comply with BSI, IEC, or VDE safety requirements.

There are several aspects of the Burroughs Product Safety Standard ST 1257 4893, specifically hi-pot and primary conductor spacings, that are aimed at IEC 435 compliance; there are no plans to comply with these requirements.

A provisional corporate waiver has been granted. The system can not be marketed in countries requiring IEC, VDE, or BSI certification.

7 HARDWARE/SOFTWARE DESCRIPTION

7.1 HARDWARE DESCRIPTION

The hardware components of the V300 System are essentially the same as those of the B4900 with the exception of the memory subsystem and appearance hardware such as skins.

7.1.1 COMPONENT TECHNOLOGY

The predominant circuit technology used in the V300 is Schottky TTL. Both Texas Instrument "AS" and Fairchild "FAST" Advanced Schottky parts are also used. The control stores have been implemented from 1Kx4 and 4Kx4 bipolar RAM parts.

The same Processor and I/O Cabinet frames used on the B4900 System are being used on the V300 System. They have been designed to pass stringent vibration and shock requirements and to eliminate most shipping brackets. The B4900 shipping

container designed to meet stringent shipping requirements, is being used for the V300.

The V300 will utilize the 5 1/4 inch minidisk and the 3-card Maintenance Processor.

7.1.2 ARCHITECTURAL DESCRIPTION

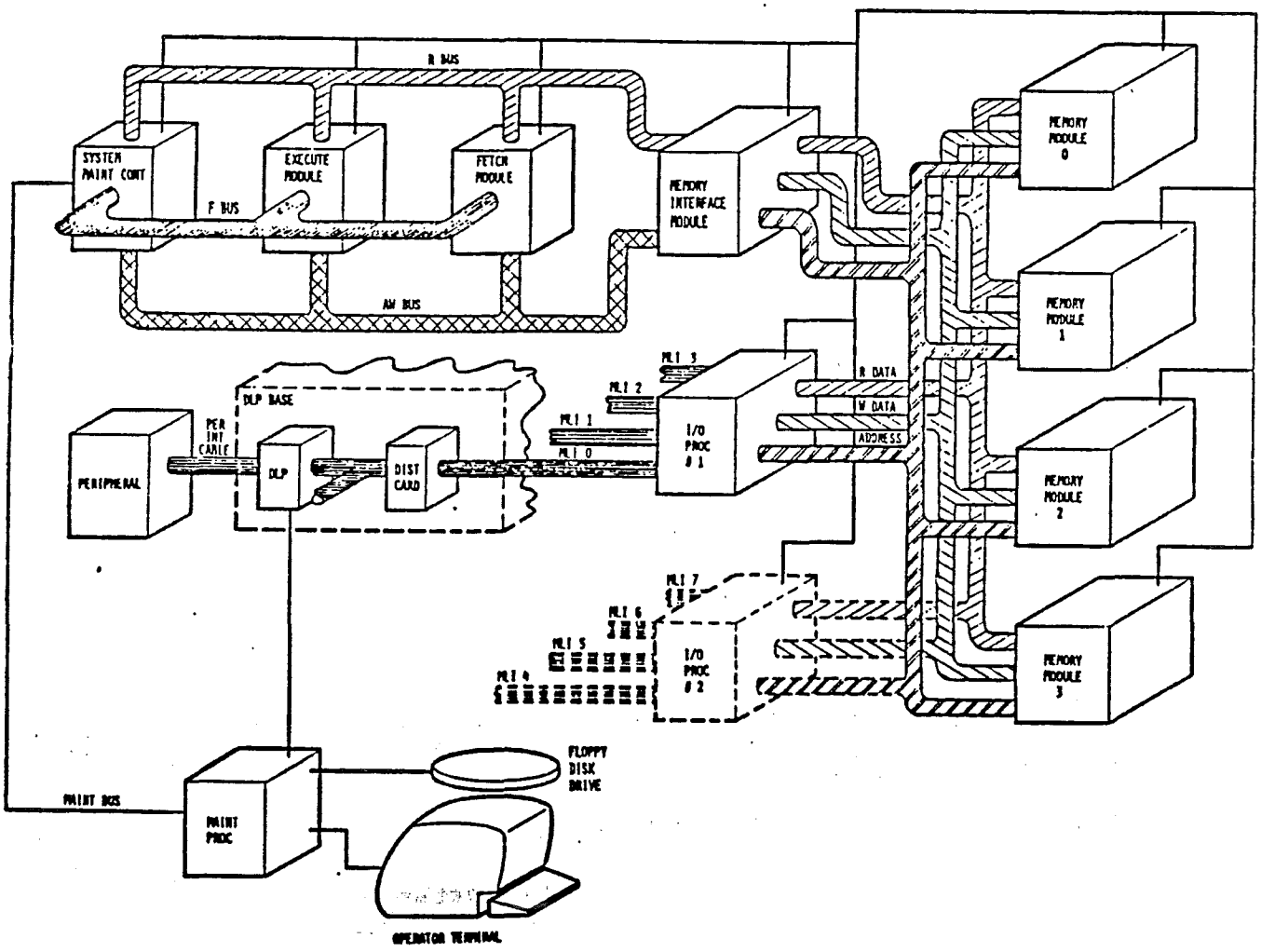
The V300 is a multimodule/multibus architecture. In addition to the intermodule buses, the individual modules have been designed around internal buses (Figure 7-1). A general description of the modules and buses follows. Finally a brief comment on the flow of instructions is provided. For more detailed description, the B4900 Architecture Specification (EDS 1987 1193) is applicable.

Module descriptions: general

The instructions are pipelined and the data path is forty bits or ten digits. Module operations work on a 110 nanosecond cycle time or multiple of that, and bus transfers occur in a 110 nanosecond period.

In order to maximize the benefits of pipelining, a branch prediction algorithm has been included and is used for all conditional branch instructions. This will attempt to anticipate which direction the branch will go, based upon its previous behavior, and begin prefetching instructions in that direction.

FIGURE 7-1 FUNCTIONAL BLOCK DIAGRAM



7.1.2 ARCHITECTURAL DESCRIPTION (Continued)

Module Descriptions

Fetch Module (FM)- This module is designed to fetch and format instructions for effective execution by the execute module. It contains queues to prefetch instructions (separate state machine) and queues with which to pass formatted instructions on to the execute modules. All address indexing and indirection is resolved in this module. The Fetch Module also contains the branch prediction logic and the interlock control. The latter is required to preserve proper instruction execution in the pipe. The primary state machine is microcoded in a form and manner similar to that of the execute module. Current microcode depth is 4K words (approx 60 bits per word). For more detailed information refer to the B4900 Execute Module Specification.

Execute Module (XM) -

This module contains a two page (two instruction) queue. While one page is being accessed by the XM, the other page is being filled by the Fetch module.

The XM picks up instructions from the queue and executes them. It receives the instructions via the fetch bus, and operands via the read bus; it generates commands and stores results via the AW bus. It is microcoded and contains a 16K word control store (80 bits per word). Refer to EDS 1984 0230 for design detail.

Memory Interface Module (MIM) -

This module acts as an intermediary between the fetch and execute modules and the memory modules. It contains a sixteen deep request queue (attached to the AW bus) All requests for memory are done base relative. The MIM contains all base limit pairs and produces the absolute addresses. It also contains all global state items, including exception flip flops. Refer to EDS 1982 8037 for additional information.

7.1.2 ARCHITECTURAL DESCRIPTION (Continued)

I/O Processor Module (IOP) -

This module interfaces to the I/O subsystem. It receives I/O initiates from the processor and passes the operations on to the MLI/DLP subsystem; or in the case of QWIK Disk, to or from a protected area of main memory. Once initiated, it is capable of initializing, carrying out the data transfers and storing result descriptors in memory totally independent of the Processor. Unlike the processor, the IOP uses a 16 bit data path. The IOP is also microprogrammed and contains a 1K word control store. For more detailed information, refer to EDS 1983 6915.

System Maintenance Controller (SMC)-

The purpose of the SMC is to act as a dynamic interface between the Maintenance Processor and the remainder of the system. It connects to all modules via a maintenance bus and to the Maintenance processor using a MP interface bus. It also contains a copy of the measurement register for monitoring by external hardware monitors. (This register will not be actively utilized until availability of MCP 1.0). (Refer to EDS 1987 1227 for design details.)

Maintenance Processor-

This is essentially a redesigned form of the Universal Console. It connects to the SMC and acts as a maintenance tool as well as a controller of the Operator Control Station. It is microprocessor based (8085) and is microprogrammed. It contains 64K words of control store. It can read and write 5 1/4 inch diskettes via the one or two drives provided. For further design information, see EDS 1987 1227.

Memory Module-

The memory module is essentially part of the processor in the sense that it contains more than 50 percent logic. Each module contains 192 storage elements in four banks. The memory word is 48 bits in width (40 data, 8 error code). The module is capable of accepting a read or write command and then decoupling from the processor while the operation is in progress. It operates synchronously, so the Read Write controller and the IOP are responsible for knowing when to

reconnect.

7.1.2 ARCHITECTURAL DESCRIPTION (Continued)

The memory module will correct and report single bit errors and report double bit errors. More design information is provided in EDS 1987 1102.

Bus Descriptions

Read Bus-

This bus is a 40 bit data path, driven solely by the Read Write controller. It is capable of passing certain memory interface module (MIM) internal information or memory data to the fetch or XM modules. The data passed is always in response to a request in the AW queue. Since it is only sourced by one module, no contention resolution is required. The specific behavior of the read bus (protocol etc.) is described in EDS 1982 8037.

AW Bus-

The AW bus is also a 40 bit data path. As it can be sourced from either fetch or XM modules, it contains contention resolving logic. With the exception of branch of control messages which also go to the fetch module from the XM, and measurement commands which go to the SMC from the XM, all requests are directed to the MIM request queue. This bus protocol is covered in EDS 1987 8037.

Fetch Bus-

This is also a 40 bit data path. It is sourced only by the fetch module, and sinked by the XM or XMs. Its sole function is to pass formatted instructions to the XMs. It passes them at will unless the XMs have raised the "page full" indicator. The Fetch bus protocol is covered in EDS 1984 0255.

Memory Address Bus-

This bus represents the path for addresses to memory from either the MIM or the IOP(s). It is a 24 bit bus, because the addresses are (pseudo) binary at this point and that the module selects and digit mark signals represent the remainder of the address. The Memory Address bus is covered in EDS 1987 1102.

7.1.2 ARCHITECTURAL DESCRIPTION (Continued)

Memory Read Data bus-

This bus is a 40-bit data path that passes the requested data to the MIM. The Read data bus protocol is discussed in EDS 1982 8037.

Memory Write Data bus-

This bus is a 40-bit data path that sends the write data to the memory module. The read modify write operation is done internal to the memory modules. The Write data bus protocol is also discussed in EDS 1982 8037.

MLI buses-

These are the standard 16 bit data paths for communication with the DLPs. The MLI bus protocol is covered in 2323 7399 Interface.

Maintenance bus-

This bus has 16 control lines and a 1-bit serial data path. The data path has two or more connections from each module, a data in and a data out. It is used to move machine state into and out of the modules. Initialization of the control stores is done on this path. The maintenance bus is described in EDS 1987 1227.

Processor Operation

Since most B4900/V300 modules contain RAM control store, they must be initialized at power up time. This is done by the operator using the ODT and the appropriate diskettes.

Using related steps, the desired programs are brought into memory and the Fetch module has its program counter pointed to the desired location in memory.

At this point the System is placed in a running mode.

The Fetch module initiates requests for instructions (predicting the likely path for branches). It queues up several instructions at a time. It removes each one, and resolves its addresses for indexing and indirection. It also

checks the possible interlocks of the operands against the contents of the Lock Unit.

7.1.2 ARCHITECTURAL DESCRIPTION (Continued)

If all looks good, it passes the resolved addresses and the op code to the input queue of the execute module. When ready, the execute module pulls the instruction from the queue, generates memory requests for operands via the AW bus and receives the operands via the Read bus.

The execute modules carry out the requirements of the instruction and send the result (where applicable) to the memory via the AW bus.

The following description reflects the initial V300 I/O interface. Future enhancements may alter this interface.

In the case of I/O operations, the XM sends a signal to the IOP, telling it that an I/O has been generated. The memory is divided in such a way that the operating system base zero is actually above the physical address zero of the physical zero memory. The space "underneath" MCP base zero is used by the IOT as a scratchpad and communication area. When the signal is received, it looks in the assigned locations in "subzero" memory for the word link addresses.

All actual I/O in terms of initiation, data transfer and termination is performed by the IOP. Upon completion of the I/O, it signals the processor, and the normal interrupt mechanisms to the MCP take over.

IOP Operation

The following description reflects the initial V300 I/O operation. Future enhancements may alter this functionality.

The IOP is sensitive to a signal from the Processor indicating that an attempt has been made to initiate an I/O. It reads memory to locate the link addresses and initiates the I/O to the DLP. It is then disconnected and available for more initiates or interrupts from the DLPs.

When reconnected, it moves data from or to memory and with a minimum of local buffering, as appropriate, completes the I/O operation by writing a result descriptor.

The IOP also supports a QWIK Disk function. I/O to the QWIK Disk is received in the same manner as other I/Os. The I/O operation is directed to Channel 40. The IOP sensing this emulates the combined DLP/Drive function, but moves data to and from a protected memory area. Result reporting is done in the same fashion as for other I/O devices.

Each IOP operates independently and responds to the I/Os of its own channels.

7.2 SOFTWARE DESCRIPTION

The initial V300 hardware will be available to run under MCPIX ASR 7.0. No changes are required in the software. All system software which runs on the B4900 will run on the V300. The V300 will also run under MCP 1.0 and execute an enhanced version of the Medium Systems instruction set.

The MCP 1.0 operating system is a new MCP which utilizes the V Series architecture and firmware available with the V Series processor. The MCP 1.0 operating system, and features in other programs dependent upon MCP 1.0 features will be available.

The MCP 1.0 operating system contains features equivalent to MCPIX at the ASR 6.8 release. However, not all MCPIX utilities and intrinsics are needed on MCP 1.0. In addition it has the following features and capabilities.

Tailored I/O Paths

Tailored I/O paths, first introduced in MCPIX, have been expanded under MCP 1.0. Tailored I/O paths will be available for all commonly accessed peripheral devices (disk/pack - both sequential and random access methods: tape: printers: card readers: and device backup files. Including printer, punch, and pseudo card readers). In addition, more processing is performed at file open time than in previous MCPs (including tailored I/O path selection, I/O queue element construction and the caching of pointers to key I/O structures). This results in a much shorter and more efficient I/O path, particularly since a queue element does not need to be constructed for each I/O.

Enhanced Physical I/O Interface

MCP 1.0 emulates the new V Series Enhanced Physical I/O Interface to the I/O subsystem. Firmware execution of the majority of this interface is expected to be available in a future MCP release providing further performance improvements. This interface will allow V Series processors to utilize the "multiple initiate" capability of our DLPs and is easily extensible to support Local Area Network style I/O subsystems.

7.2 SOFTWARE (Continued)

The MCP 1.0 operating system performs its system maintenance duties by creating, executing, and destroying independent Runners - tasks with special privileges and addressing rights. Some independent Runners exist the entire time the system is running, while others are created for short periods to perform specialized functions. The advantage of Independent Runners is that they can execute in parallel - the suspension of one (while waiting for, say, a slow peripheral) does not inhibit the execution of others. System maintenance becomes more reliable and efficient.

Independent Runners on MCP 1.0 release perform such varied functions as I/O Complete processing, I/O Error recovery, device status polling, resource management and log transfer processing.

System Event Mechanism

The MCP 1.0 operating system supports a System Event Mechanism for co-ordination of internal operating system functions and for the co-ordination of the operating system with user program requests. This low overhead Event Mechanism eliminates many costly and distributed evaluation routines in the MCP, replacing them with a centralized mechanism for resolving intertask and inter-independent Runner co-ordination issues.

This mechanism is currently restricted to the MCP, though a future release may allow user tasks to create events and interact with other tasks sharing common events.

Isolation of Memory References

Access to memory by any task or operating system function is isolated to those memory regions that are essential to the task or function. In other words, no software component has addressability to all of memory at any instant in time except the MCP 1.0 Memory Manager.

7.2 SOFTWARE (Continued)

Memory Size

MCP 1.0 is able to address and make use of more than 5MB of memory. In fact, the amount of memory that can be addressed is 36 QUADRILLION (36 X 10**15) bytes.

Timesharing Area

The 300 KD limit on the timesharing area has been eliminated.

Multiple Processors

The MCP 1.0 design is such that support of "tightly coupled" multiple processors will be possible on a subsequent release.

Expanded Number of Programs

The MCP 1.0 operating system raises the limits on the number of programs running on a system from 99 to 9999. However, the present limitation that the number of active data bases plus the number of programs invoking data bases must be less than or equal to 99 is still maintained.

Expanded Peripheral Support

The MCP 1.0 operating system raises the limits on the number of peripherals attached to the system subject to the following limitations.

1. The number of disk devices that can be connected to a processor is increased from 39 to 99.

2. The total number of disk and pack devices connected to a processor is increased from 99 to 10000.

3. All, some or none of the disk and pack devices can be shared among all or some of the processors comprising a Shared System. It may, however, be necessary to purchase multiple Shared System Processors to achieve a configuration involving large numbers of shared devices.

7.2 SOFTWARE (Continued)

4. Sets of packs are allowed to be shared by only some of the processors in a Shared System. Thus, in a three processor system, some packs would be accessible by all three processors, some by processors 0 and 1, some by 1 and 2, some by 0 and 2, and some just by individual processors. In fact, of the packs accessible from an individual processor, some could allow shared file access while others prohibit it.

5. Up to 10,000 non disk/pack devices (tapes, printers, etc.) can also be connected to a processor.

It is important to realize that while the software will allow the declaration of up to 10,000 disk/pack devices, this does not imply that the hardware released with the Operating System will be capable of supporting such a configuration. Hardware limitations on the number of channels and the number of devices per channel mean that only about 1,000 peripherals can be connected to a V Series processor. The software limits have been set very high so that there will not be a major software change necessary when hardware becomes available that allows connection of more than 1,000 peripherals.

Expanded Debug Capabilities

The MCP 1.0 operating system will include an enhanced DEBUG module as part of the MCP. This module will support

1. Debug sessions concurrently active on more than one task (previous MCPs allowed only one task per system to be TRACING).

2. Interactive debug via a uniline or ODT terminal. It may also be possible to provide interactive debug via the remote maintenance link on 7.0 MCP 1.0. In future releases, interactive debug may be expanded to use any datacomm connection to the system.

7.2 SOFTWARE (Continued)

Interactive debug will include, but not be limited to

a. setting and executing until multiple breakpoints

b. stopping on reference and/or modification of particular memory regions

c. tracing (with output directed to hard copy or to the terminal) or single-instructing

d. examination and/or modification of memory within the debugged task subject to security restrictions.

3. Debug of the interaction of multiple user programs (intended primarily to assist in systems development).

4. Debug of portions of the MCP without having to trace periodic functions that are known to work.

5. Examination of MCP structures in symbolic form rather than as raw memory.

6. An optional DEBUG LOG (standard log-file format) can be maintained that logs the major state transitions of the MCP and will be useful in debugging coordination problems.

7. New control commands are implemented to invoke the various debug options for either a user program(s) or for the MCP as a whole.

8. Special debug functions for the new System Event Mechanism.

9. Remote maintenance through the maintenance processor.

Expanded Hardware Support

MCP 1.0 adds hardware support for M680 disk.

8 INTERNATIONAL SPECIAL ENGINEERING REQUIREMENTS

POWER

The V300 can accommodate nominal AC voltages between 200V and 240V AC, with steady state variations of +10 to -20% and power frequencies in the range of 47 to 63 Hz. This allows world wide installation except in the following countries for the reasons cited.

Country	Reason	
Puerto Rico	frequency	60Hz +/- 6Hz
Iran	voltage	+/- 15%
Isolated Mining Districts in South America	frequency	25Hz
Some Remote Areas of Australia	voltage	440 VAC

GOVERNMENT REQUIREMENTS

EMI

The V300 complies with FCC (Class A).

The V300 is designed for VDE compliance. Certification by the VDE will not be obtained by Engineering.

SAFETY

The V300 is UL listed and CSA certified.

9 V300 SERIES PERFORMANCE LEVELS

9.1 V310-1 PERFORMANCE LEVEL

The V310-1 performance level includes the items listed in the following table and in the quantities indicated.

STYLE NO.	M&E NO.	DESCRIPTION	QUANTITY
V310-1			
	1994 2507	V310 CP - Processor Cabinet	1
	1987 1169	1.28 MB Memory Module 2	4
	1994 2598	Processor Cabinet End Panel	1
	1987 1136	5V 200A Power Module	2
	1997 5465	Fetch Adapter 1A	1
	1998 5258	V310 Firmware/Diagnostics	1
	1987 1151	System Maintenance Kit	1
	1989 9152	900 Processor Cab Ship Kit	1
	1998 5233	V310 IOC - I/O Cabinet 2	1
	1984 0313	Maintenance Processor	1
	1998 5316	V310 DLP Base Backplane 6A	2
	1984 0115	DLP Base Support Kit	1
	1987 1136	*5V 200A Power Module	1
	1987 1128	*5V Power Extension Kit	1
	1988 0905	*Minidisk Drive Module	1
	1993 5154	DLP Test Support Kit	1
	1972 3287	DLP Maintenance Kit	1
	1989 9178	900 I/O Cabinet Ship Kit	1
	2346 9703	Console DLP	1
	3390 5431	Operator Display Terminal	1
	1990 9829	15 Ft Primary ODT Cable Kit	1
	2395 2039	*Remote Support Data Set	0-1

*See Paragraph 9.5 for notes.

9.2 V310-2 PERFORMANCE LEVEL

The V310-2 performance level includes the items listed in the following table and in the quantities indicated.

STYLE NO.	M&E NO.	DESCRIPTION	QUANTITY
V310-2			
	1994 2507	V310 CP - Processor Cabinet	1
	1994 2390	5MB Memory Module	2
	1994 2598	Processor Cabinet End Panel	1
	1987 1136	5V 200A Power Module	2
	1997 5465	Fetch Adapter 1A	1
	1998 5258	V310 Firmware/Diagnostics	1
	1987 1151	System Maintenance Kit	1
	1989 9152	900 Processor Cab Ship Kit	1
	1998 5233	V310 IOC - I/O Cabinet 2	1
	1984 0313	Maintenance Processor	1
	1997 5374	*DLP Base Module 6	1
	1998 5316	V310 DLP Base Backplane 6A	1
	1990 9365	DLP Base Cable Kit 1	1
	1984 0115	DLP Base Support Kit	1
	1987 1136	*5V 200A Power Module	1
	1987 1128	*5V Power Extension Kit	1
	1988 0905	*Minidisk Drive Module	1
	1993 5154	DLP Test Support Kit	1
	1972 3287	DLP Maintenance Kit	1
	1989 9178	900 I/O Cabinet Ship Kit	1
	2346 9703	Console DLP	1
	3390 5431	Operator Display Terminal	1
	1990 9829	15 Ft Primary ODT Cable Kit	1
	2395 2039	*Remote Support Data Set	0-1

*See Paragraph 9.5 for notes.

9.3 V340 PERFORMANCE LEVEL

The V340 performance level includes the items listed in the following table and in the quantities indicated.

STYLE NO.	M&E NO.	DESCRIPTION	QUANTITY
V340			
	1994 2507	V340 CP - Processor Cabinet	1
	1994 2390	5MB Memory Module	2
	1994 2598	Processor Cabinet End Panel	1
	1987 1136	5V 200A Power Module	2
	1993 4843	Fetch Adapter 1	1
	1997 5325	V340 Firmware/Diagnostics	1
	1987 1151	System Maintenance Kit	1
	1989 9152	900 Processor Cab Ship Kit	1
	1998 5233	V340 IOC - I/O Cabinet 2	1
	1984 0313	Maintenance Processor	1
	1997 5374	*DLP Base Module 6	2
	1990 9365	DLP Base Cable Kit 1	1
	1990 9373	DLP Base Cable Kit 2	1
	1984 0115	DLP Base Support Kit	1
	1987 1136	*5V 200A Power Module	1
	1987 1128	*5V Power Extension Kit	1
	1988 0905	*Minidisk Drive Module	1
	1993 5154	DLP Test Support Kit	1
	1972 3287	DLP Maintenance Kit	1
	1989 9178	900 I/O Cabinet Ship Kit	1
	2346 9703	Console DLP	1
	2346 0397	Host Transfer Sequential DLP	2
	---- ----	Line Printer DLP	1
	---- ----	Magnetic Tape DLP	1
	3390 5431	Operator Display Terminal	1
	1990 9829	15 Ft Primary ODT Cable Kit	1
	2395 2039	*Remote Support Data Set	0-1

*See Paragraph 9.5 for notes.

9.4 V380 PERFORMANCE LEVEL

The V380 performance level includes the items listed in the following table and in the quantities indicated.

STYLE NO.	M&E NO.	DESCRIPTION	QUANTITY
V380			
	1994 2507	V380 CP - Processor Cabinet	1
	1994 2390	5MB Memory Module	2
	1994 2598	Processor Cabinet End Panel	1
	1987 1136	5V 200A Power Module	2
	1996 3727	*IOP Module	1
	1993 4850	Fetch Adapter 2	1
	1997 5333	V380 Firmware/Diagnostics	1
	1987 1151	System Maintenance Kit	1
	1989 9152	900 Processor Cab Ship Kit	1
	1998 5233	V380 IOC - I/O Cabinet 2	1
	1984 0313	Maintenance Processor	1
	1997 5374	*DLP Base Module 6	2
	1990 9365	DLP Base Cable Kit 1	1
	1990 9373	DLP Base Cable Kit 2	1
	1984 0115	DLP Base Support Kit	1
	1987 1136	*5V 200A Power Module	1
	1987 1128	*5V Power Extension Kit	1
	1988 0905	*Minidisk Drive Module	1
	1993 5154	DLP Test Support Kit	1
	1972 3287	DLP Maintenance Kit	1
	1989 9178	900 I/O Cabinet Ship Kit	1
	2346 9703	Console DLP	1
	2346 0397	Host Transfer Sequential DLP	2
	---- ----	Line Printer DLP	1
	---- ----	Magnetic Tape DLP	1
	3390 5431	Operator Display Terminal	1
	1990 9829	15 Ft Primary ODT Cable Kit	0-1
	1990 9837	50 Ft Primary ODT Cable Kit	0-1
	2395 2039	*Remote Support Data Set	0-1

*See Paragraph 9.5 for notes.

9.5 NOTES:

1. One IOP module is always included (parts listed) in the basic Processor Cabinet and will support up to four DLP bases (nominally a 32 DLP capacity). The V310-1, V310-2 and V340 performance levels can include only one IOP. The V380 performance level includes two IOP's.

2. One DLP Base Module is always included (parts listed) in each basic I/O Cabinet. One additional DLP Base Module is provided in the V310-2 performance level. Two additional DLP Base Modules are provided in both V340 and V380 performance levels.

3. One 5V 200A Power Module is always included (parts listed) in each basic I/O Cabinet and provides power for the first DLP Base. A second 5V 200A Power Module is provided in each of the V300 performance levels to provide power for the second and third DLP bases.

   The 5V Power Extension Kit is required whenever the second 5V 200A Power Module is installed.

4. One Minidisk Drive is always included (parts listed) in each basic I/O Cabinet. Each of the V300 performance levels provide a second Minidisk Drive.

5. The Remote Support Data Set is shipped only with USMG machines.

6. An Expansion Cabinet is available and is similar to the I/O Cabinet; it does not include a minidisk drive or a maintenance processor.

10 MEDIA/SUPPLIES

T&F documentation is supplied mainly on microfiche. Approximately five percent of the documentation is on hard copy.

Test routines are supplied on 5 1/4 inch minidisks with backup on magnetic tape.

There are no supplies provided with the system.

The CSE will require a Microfiche reader to access the T&F documentation - Visidyne Model SK II-A.

APPENDIX A - ASSOCIATED PERIPHERALS

This Appendix lists the peripheral devices that are approved for connection to the V300-series systems and the DLP's that provide the connectivity for each peripheral.

PRODUCT	HOST CONNECTION
Card Readers	
B9115/16/17 300/600/800 CPM 80 Col.	X 110-90 Card Reader DLP (BCL) (2346 8879)
Card Punches	
* B9212/13 (150-300 CPM) Mod 2 B9212/13 (150-300 CPM) Mod 3	X 112-90 Card Punch DLP (BCL) (2346 8887)

* Card Punch Mod 2 has a peripheral cable with a Winchester connector and requires a (1) DLP Interface Cable Kit and (2) Signal Cable to connect to the V300 DLP Interface Cards.

DLP Interface Cable Kit (2114 9661) consists of:

Interface PCB
Interface PCB Schematic
Installation Instructions

Signal Cables

1090 4084	25 Foot Signal Cable
1090 4092	30 Foot Signal Cable
1090 4100	35 Foot Signal Cable
1090 4118	50 Foot Signal Cable
1090 2161	100 Foot Signal Cable

APPENDIX A - ASSOCIATED PERIPHERALS (Continued)

PRODUCT	HOST CONNECTION
Printers (Impact)	
(Train)	
B9247-13/16 (750 LPM)	X 247-91 750 LPM Train Printer DLP (2346 9174)
B9247-14 (1100 LPM) B9247-15 (1500 LPM)	X 247-93 1100/1500 Train Printer DLP (2346 9182)
(Buffered)	
B9246-21/24 (2000 LPM) B9246-6 (650 LPM) B9246-10 (1000 LPM) B9246-12 (1250 LPM)	X 246-92 Buffered Printer DLP (2346 9778)
Printers (Image Page Printer)	
B9290-30 Laser Printer 30 PPM	X 293-30 Image Page Printer DLP (2346 0322)

APPENDIX A - ASSOCIATED PERIPHERALS (Continued)

PRODUCT	HOST CONNECTION
Reader Sorters	
B9137-3 (1625 DPM) B9137-4 (1000 DPM) B9190-1 (1000 DPM) B9190-2 (1625 DPM)	X 337-90 Reader Sorter DLP (2346 8994)
B9138-1 (2600 DPM) B9195 (2600 DPM)	X 338-90 Reader Sorter DLP (2346 9810)
DP 1800	* X 399-90 Off-load Reader Sorter DLP (1993 4876)
Head Per Track Disk	
B9471-6 5N DFEU B9470-1 (5.9 MB) B9470-11 (5.9 MB)	** X 373-90 5N Disk File DLP (2346 8986)
Bx377-6 5N DF Exchange #	

* The Off-load Reader Sorter requires the backplane provided in the DLP Base Module 6 (1997 5374) or the UIO Backplane Kit (1997 5382).

** The 5N Disk File DLP is not to be ordered for new V300 installations. The 5N Disk File DLP is listed here to indicate that it may be used with a V300 system when it is available at an existing site.

\# The 5N Exchange cannot be housed in the V300 system cabinets. The 5N Exchange capability is available only with the inherent 2X in each 5N subsystem. Therefore, the 5N cannot be shared by more than two systems without a B2900 DLP Exchange Cabinet (1973 4763 B2095-90) with a 5N Exchange or a B4800 Exchange Cabinet (B1973 0282 B4098) with a 5N Exchange.

APPENDIX A - ASSOCIATED PERIPHERALS (Continued)

PRODUCT		HOST CONNECTION
Disk		
B9387-41/42	DPD Controller	*X 304-90 Host Transfer DLP
B9484-5	206 Disk Pack Drive(LAK/PAK)	(2346 9497)
B9494-2/4	207 Disk Pack Drive(LAK/PAK)	
B9387-51/52	DPD Controller	*X 304-90 Host Transfer DLP
B9484-5	206 Disk Pack Drive(LAK/PAK)	(2346 9497)
B9494-2/4	207 Disk Pack Drive(LAK/PAK)	
B9484-12/13	677 Memorex 250MB (LAK/PAK)	
B9494-5	659 Memorex 478MB (PAK)	
B9494-10	659 Memorex 2 Spindle 956MB (PAK)	
# B9387-51/52	DPD Controller	X 304-91 Sequential Host
B9484-5	206 Disk Pack Drive(LAK/PAK)	Transfer DLP
B9494-2/4	207 Disk Pack Drive(LAK/PAK)	(2346 0397)
B9484-12/13	677 Memorex 250MB (LAK/PAK)	
B9494-5	659 Memorex 478MB (PAK)	
B9494-10	659 Memorex 2 Spindle 956MB (PAK)	
B9389	Controller (3680)	X 304-91 Sequential Host
B9399	Dual String Controller	Transfer DLP
B9494-12	Memorex 1 spindle 1.1GB (PAK)	(2346 0397)

* The "nonstandard" Host Transfer DLP (2346-9497) is not to be ordered for new installations but is listed here to indicate that it may be used with a V300 system when it is available at an existing site.

\# The following are required for B9387 DPD Controllers with SEQ HT DLP: I/O Data Bus Kit Split (3310 9414), Host Intrf. BLT-A (3310 9398), Host Signal Cables (Various), and System Ground Cable (Various), See B9387 System Index 2607 4955 for quantities, cable connectors and lengths.

Disk Pack Drive Exchange

BX387-1 Disk Pack Drive Exchange

Exchange is compatible with the Model 206 and 207 DP Drives and with Model 677 and 659 Memorex DP Drives.

APPENDIX A - ASSOCIATED PERIPHERALS (Continued)

PRODUCT	HOST CONNECTION
Magnetic Tape (NRZ,PE)	
B9499-11 MEC B9495-82/83 MTTU B9495-88 MTTU	X 393-90 NRZ Mag Tape DLP (2346 9844)
B9499-11 MEC B9495-82/83 MTTU B9495-88 MTTU	X 395-91 PE Mag Tape DLP (2346 8937)
Magnetic Tape (GCR)	
B9499-21/22/23/24 GCR TCU B9495-24 GCR/PE MTU 200 IPS B9495-32/33 5G PE/GCR MTU	X 395-92 GCR Mag Tape DLP (2346 9752)
B9495-32M PE/GCR TCU B9495-32 5G PE/GCR MTU	
B9495-33M PE/GCR TCU B9495-33 5G PE/GCR MTU MTU	
BT3200 Magnetic Tape (PE/GCR)	
B3261/2 PE/GCR MTC BT3266 PE/GCR MTU 125 IPS	*X 395-93 FIPS TAPE DLP 2 (2346 1189)
B3281/2 PE/GCR MTC BT3266 PE/GCR MTU 125 IPS BT3288 PE/GCR MTU 200 IPS	
BT3201/2 PE/GCR MTC BT3266 PE/GCR MTU 125 IPS BT3288 PE/GCR MTU 200 IPS	
B3241 PE/GCR MTC BT3244 PE/GCR MTU 75 IPS	

* The X 395-93 FIPS Tape DLP is not a separately orderable DLP. It is provided only with the BT3200 Magnetic Tape peripheral.

APPENDIX A - ASSOCIATED PERIPHERALS (Continued)

PRODUCT	HOST CONNECTION
ODTs	
ET1100	X 342-91 Console DLP (2346 9703)
ET1210	
Data Comm	
Qualified Terminals	X 351-94 Uniline DLP (1988 1077)
B874 DCP	V 303-90 Host Transfer DLP (2346 9497)
CP3682 Data Comm Processor	X 368-90 PE Mag Tape DLP (2346 8937)
B974	X 320-2 HC2 ISC DLP (3219 4250)

For Data Sets, Terminals and Line Procedures qualified for the B874, refer to the B874 System Index (2607 9251).

Processors	
B9321-5 ISC HUB16 (3219 4250)	X 320-2 HC2 ISC DLP
V300 as Host	X 376-95 Shared System Processor (2346 9836)
V300 or B4900 as Sharing	X 376-96 SSP B4900 Adapter Kit
B3900/Model 3 as Sharing	X 376-94 SSP B3900/M3 Adapter Kit

APPENDIX A - ASSOCIATED PERIPHERALS (Continued)

PRODUCT		HOST CONNECTION
Peripheral Switches		
Style	Description	Periheral Supported
B9420-1	PSII Basic Unit	B9190-1 Reader Sorter 1000 DPM
B9420-IU	PSII Upgrade Unit	B9190-2 Reader Sorter 1625 DPM
CB330	B9420-1 10 Foot Cable (PSII to Periheral)	B9195 Reader Sorter 2600 DPM B9290-30 Laser Printer 30 PPM
B9420-2	PSII Basic Unit	B9246-6 650 LPM Printer
B9420-2U	PSII Upgrade Unit	B9246-12 1250 LPM Printer
CB331	B9420-2 10 Foot Cable (PSII to Peripheral)	B9246-20 2000 LPM Printer B9246-21 2000 LPM Printer
B9420-3	PSII Basic Unit	B9247-15 1500 LPM Printer
B9420-3U	PSII Upgrade Kit	B9116 Card Reader
CB209	B9420-3 25 Foot Cable (PSII to Peripheral)	B9212 150 CPM Card Punch B9213 300 CPM Card Punch
B9420-DC	Data Comm Kit	Data Com Interfaces
B9420-DCU	Data Comm Upgrade Kit	

APPENDIX B - QWIK DISK PERFORMANCE