Burroughs

SERIES E 2100

DIRECT ACCOUNTING COMPUTER

INSTRUCTION BOOK

Section IV

●

ELECTRONIC CIRCUIT DESCRIPTION

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For Form 3737

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Electronic Circuit Description

INTRODUCTION

This machine employs combination diode-transistor circuits which utilize the speed and cost advantage of diode gating, together with the current amplification and speed characteristics of non-saturating emitter follower output circuitry. The basic logic elements include the AND gate, OR gate and the AND-OR combination. A Heavy Buffer (emitter-follower circuit) is also provided for use whenever an increase in output drive current is required. One additional logic element, the Inverter, employs a common emitter circuit for both logical inversion and for re-establishing signal voltage levels after a signal has been attenuated by a logical chain.

A number of circuits are provided to Control the various operations. These include the basic Flip-Flop, the Reset Standardizer, the Clock Timing circuits, etc. These Control elements cause the Keyboard-Printer and the Arithmetic and Memory unit to operate together as an integrated system.

In addition to the Logic and Control elements, there are a number of circuits such as the Memory Driver and Sense-MR that are associated with Reading from and Writing into the Memory.

Finally, there are a number of miscellaneous circuits such as the Indicator circuit, which employs neon lamps for trouble shooting, various voltage wetting circuits, etc.

SIGNAL VOLTAGE LEVELS

The waveform below shows the range of voltage levels for a High, Low and Unstable signal:
A signal voltage level between +1.0 volts and -1.0 volts is a "high" signal and between -3.0 volts and -5.0 volts a low signal. Signal levels between -1.01 volts and -2.99 volts are considered unstable.

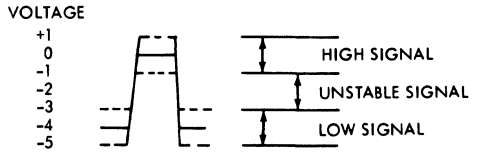


FIGURE IV-1

Many of the following circuit drawings show in parathenses the voltage levels of significant points under static conditions.

LOGIC CIRCUITS

"AND" Gate

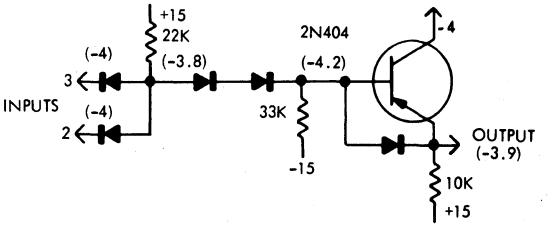


FIGURE IV-2

The diodes at input pins 2 and 3 form the diode gate together with the 22K ohm source resistor connected to +15 volts. If either or both of the inputs are low, for example -4.0 volts, then the output of the gate will be low (-4.0 volts less approximately .2 volts diode drop or -3.8 volts). Current flow from -15 volts thru the 33K ohm resistor, the two series level shifting diodes and the 22K ohm resistor to +15 volts shifts the level down to approximately -4.2 volts at the base of the transistor.

The emitter-follower circuit involving the 2N404 transistor at the gate output provides current to drive succeeding logical elements. With an emitter-follower a large current amplification can be obtained but the voltage gain is slightly less than 1 and there is no inversion of the input signal. In the case of a p-n-p emitter-follower the emitter output signal is always slightly positive with respect to the input signal at the base. For this reason the transistor conducts and there is emitter and collector current at all times. With the signal at the base of the transistor low due to one or both gate inputs being low, the output will be -4.2 volts less a small transistor drop or approximately -3.9 volts.

With both gate inputs at the high level, for example ground, the output of the gate diodes will be high (+.2 volts), at the base of the transistor -.2 volts due to the level shifting diodes and the output at the emitter will be near ground (-.1 volt approximately).

At the output of the AND gate, there is some stray capacity to ground and since a capacitance will not allow an instantaneous change of voltage, it affects the rise time of the signal. During the time the emitter-follower output is at the low level, the stray capacity becomes charged to -4 volts. In order for the emitter to closely follow the base when the input goes to ground a fast discharge path must be provided for this capacity. The diode connected between the emitter and base provides a low resistance discharge path around the transistor.

As the various signals pass thru a stage of logic the voltage levels deteriorate slightly with -4 volt signals becoming less negative and ground signals less positive. For example, a signal which at the input to a series of logic elements was at ground might deteriorate as follows:

After the first stage -.25 volts, second stage -.44 volts, third stage -.62 volts, fourth stage -.8 volts and fifth stage -.97 volts. This signal would then be very close to the -1 volt lower limit which the various circuits will accept as a high signal. As a rule, signals are never routed thru more than four stages of logic before they are applied to a circuit which will re-establish the -4 volt and ground levels.

"OR" Gate

The electrical circuit for a three input positive OR gate is shown below:

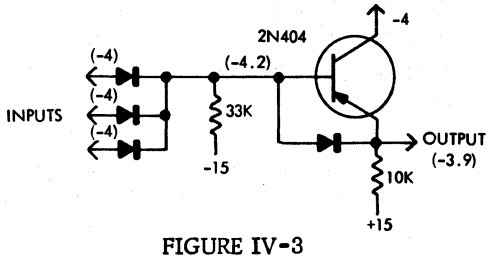


FIGURE IV-3

The three input diodes form the OR gate together with the 33K resistor connected to -15 volts. With all three inputs at the low level, -4 volts for example, the voltage at the base of the transistor will be approximately -4.2 volts. The transistor will be conducting and the output will be low (-4.2 volts less .3 volts transistor drop or -3.9 volts). The level shifting diodes are not necessary in the OR circuit since the diode voltage drop at the input is in the opposite direction to the transistor base-emitter drop.

When one or more of the OR gate inputs are high (ground) the voltage at the base will be ground less the diode voltage drop or -.2 volts. The transistor will be conducting and the output will be at approximately ground level.

At the output of the OR gate, there is a certain amount of stray capacity as with the AND gate and a diode is provided to discharge the stray capacity when the output voltage level switches from -4 volts to ground.

"AND-OR" Gate

The electrical circuit for a positive AND-OR gate is shown below:

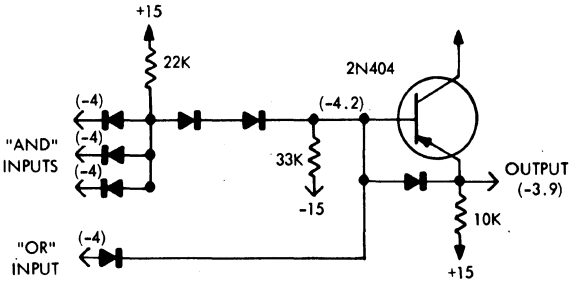


FIGURE IV-4

It consists of a basic 3 input diode AND gate, together with an OR input, level shift diodes and emitter-follower output circuit. This circuit may be expanded to include as many as 8 AND inputs as provided on the logic cards LCE and LCD. The Output will be high when the 3 AND inputs are high or whenever the single OR input is high. The Output will be low when the OR input is low and at least one AND input is low. The diode between the emitter and base is provided to discharge any stray capacity when the output voltage level switches from -4 volts to ground.

Heavy Buffer

The Heavy Buffer is an emitter-follower circuit that is used following logic elements whenever an increase in output drive current is required without inversion of the input signal. The output of the H.B. circuit, shown below, will be high when the input is high and low when the input is low. The 2N404 conducts at all times because a high input does not reverse bias the base-emitter junction.

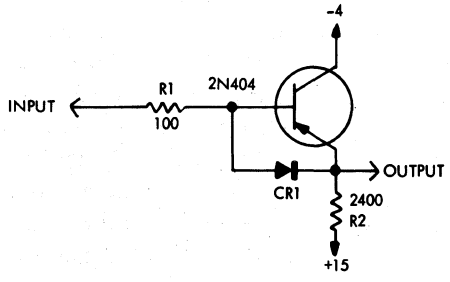


FIGURE IV-5

In addition to a power gain without any inversion of the input signal, the H.B. also provides isolation between groups of logical elements and reduces tendency for stages of logic to oscillate. The 100 ohm resistor R1 is provided in series with the input as an oscillation suppressor. The diode CR1 connected between the base and emitter discharges any stray capacity at the output when it switches from -4 volts to ground. In this way, the emitter can closely follow the base when the logic switches from a low input to a high input.

Inverter

The Inverter, as the name implies, provides a logical inversion of signals applied to its input. In addition, it re-establishes the -4 volt and ground levels to signals whose levels may have deteriorated after passing thru various stages of logic. Inverter circuits as shown below are included on Logic Cards A, B and C.

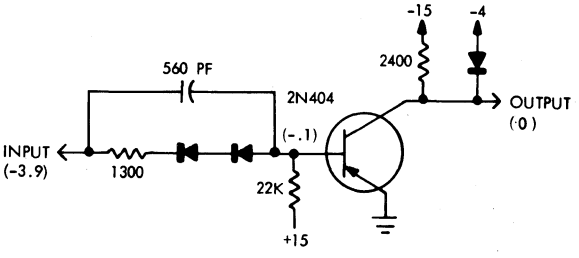


FIGURE IV-6

A grounded-emitter amplifier is used to perform the inversion. It must provide a high output signal (ground) when the input signal level is low (-3 to -5 volts) and a low output (volts) when the input is high (+1 to -1 volt). In addition, the Inverter provides isolation between groups of logical stages which prevents any tendencies toward oscillation.

If the input signal level is low, current will flow from the input thru the 1300 ohm resistor, the two series diodes and the 22K resistor to +15 volts. The base of the transistor will be

slightly negative and it will conduct in saturation from -15 volts thru the 2400 ohm resistor and the collector-emitter to ground. With the transistor conducting the output signal level will be at ground.

If the input signal level is high, current will flow from the input, thru the 1300 ohm resistor, the two series diodes and the 22K resistor to +15 volts. The base will be slightly positive with respect to the emitter and the transistor will be cut off. The output will be at -4.2 volts due to current flow from -15 volts thru the 2400 ohm resistor and the clamp diode to -4 volts.

The two series diodes provide a voltage drop of .2 to .4 volts to insure that a deteriorated high input level (-1 volt) will cut off the transistor and produce a low output. The 560 PF capacitor is used to compensate for the phenomenon known as Stored Base Charge which involves the storage of minority charge carriers in the base region of a transistor conducting in saturation. These stored charges limit the speed with which the transistor can be turned off and the 560 PF capacitor is selected to provide minimum turnoff time.

CONTROL CIRCUITS

Flip-Flops

Each Flip-Flop (FF) card contains two independent flip-flop circuits. Each circuit contains two 2N404 transistors connected in a bistable multivibrator circuit. The FF has two stable states or two conditions of equilibrium, Set and Reset, and is able to switch from one state to the other at a high rate of speed.

The FF has separate outputs from the Set and Reset stages. Since it is binary in nature, the outputs may be labeled "1" and "0" as shown on the block diagram below:

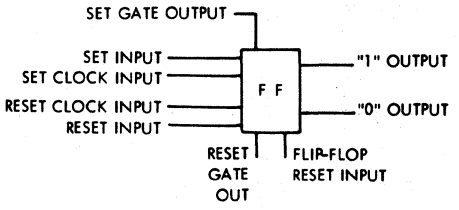


FIGURE IV-7

When the FF is Set the "1" output is high and the "0" output is low. When the FF is Reset, the "1" output is low and the "0" output is high.

Three inputs to the FF are provided. The Set and Reset inputs are gated with Clock pulses thru AND gates which are located on the FF card. The output from these gates will Set or Reset the FF respectively. Also this output maybe taken from the FF card to other circuits. The third input is the FF Reset input which is a direct means of resetting the FF.

When examining the FF circuit, reference Figure 9, the symmetry of the two stages is immediately apparent, the only difference being the direct Flip-Flop Reset Input thru the 11K ohm resistor R1.

Under static conditions, assuming the FF is Set, transistor Q1 will be ON (conducting). Its base-emitter will be forward biased due to current flow from -15 volts, thru resistors R9, R5 and R3 to +15 volts. With Q1 conducting heavily from -15 volts thru load resistor R8, the collector of Q1 will be at ground and the "1" output will be high. At this time transistor Q2 will be OFF (not conducting) due to its base-emitter being reverse biased. Since the collector of Q1 is at ground, current flow from -15 volts, thru R8, R6 and R7 to +15 volts will cause the base of Q2 to be slightly positive. With Q2 OFF, its collector is held at -4 volts due to collector load resistor R9 and clamp diode CR12 thus, the "0" output will be low.

Triggering

The FF is triggered from a negative voltage swing. It is designed primarily for triggering by the trailing edge of the clock pulse in conjunction with a logic control signal. It may, however, be triggered by any pulse that has a negative edge voltage swing of 2.5 volts minimum and pulse width of .6 μs (minimum) at the output of the Set or Reset gates. In addition to the Set and Reset input positive AND gates, a separate reset resistor input has been provided by which the FF can be directly reset without going thru logic circuitry. This input is labeled "Flip Flop Reset".

If, assuming the FF is Set, a logic signal is applied to the Reset Input together with clock pulses applied to the Reset Clock Input, the FF would reset as shown below:

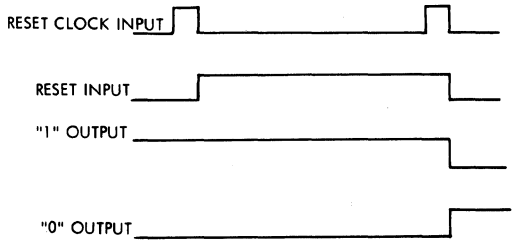


FIGURE IV-8

As the signal at the Reset Input goes from -4 volts to ground the Clock pulse goes from ground to -4 volts and the output of the Reset positive AND gate, made up of CR1, CR2 and R4, remains low. When the next clock pulse goes from -4 volts to ground, the gate output goes from -4 volts to ground. This positive going signal is coupled thru the 560 PF capacitor to the cathode of diode CR9; however, since its plate is only slightly positive, the diode disconnects and no change in the status of the FF occurs. The base of the OFF transistor Q2 cannot go more than .2 to .4 volts positive due to the clamping action of diodes CR10 and CR9. As the gated clock pulse ends, the gate output goes from ground to -4 volts. This negative signal is coupled thru the 560 PF capacitor and forward biased diode CR9 to the base of Q2. As the negative trigger pulse is applied to the base of Q2, it starts to conduct, its collector goes to ground making the "0" output high and, due to current flow thru voltage divider R5 and R3, the base of Q1 will go positive and Q1 will be cut off. As Q1 is cut off, its collector goes to -4 volts due to current flow thru resistor R8 and clamp diode CR11. The crossover or coupling resistors R5 and R6 are bypassed with capacitors C3 and C4. In this way, voltage changes at the collector of one stage are immediately coupled to the base of the other stage to speed up the switching time which, for the basic FF, is 1.1 μs maximum required to completely reverse the states.

If the FF is Reset and the same logic and clock signals were applied to the Set inputs, the switching analysis would be the same except that Q1 would be switched on and Q2 off.

Diodes CR5 and CR8 at the output of the Set and Reset gates are clamp diodes which prevent the output of the gates from going below -4 volts. In this way, any negative transient signals or voltage spikes that might occur on input lines at the low level will not get thru to trigger the FF.

Reset Resistor Input

The direct 11K resistor Reset Input requires a negative input signal that goes from ground to approximately -15 volts and remains at the lower level for 1 μs or more. The FF will reset on the leading edge of the negative going signal since it is coupled thru the 11K resistor R1 and diode CR9 to the base of Q2. If the FF already is Reset, when the resistor reset input goes negative, it will remain Reset.

Set & Reset Gate Output

The output of the Set & Reset gates are

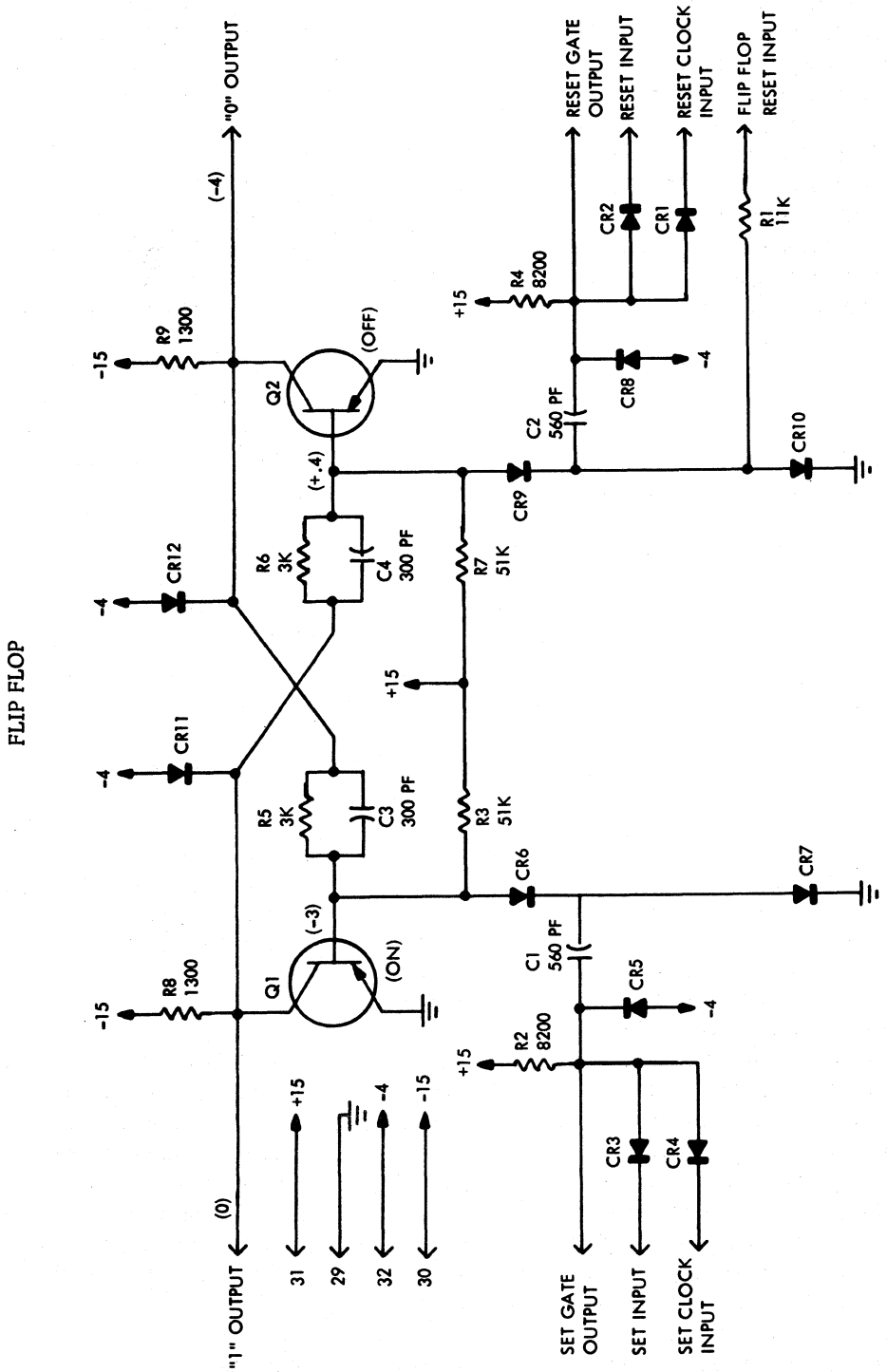

FLIP FLOP
"0" OUTPUT
(-4)
RESET GATE OUTPUT
RESET INPUT
RESET CLOCK INPUT
FLIP FLOP RESET INPUT
R9 1300
-15
Q2
(OFF)
+15
R4 8200
CR2
CR1
R1 11K
CR8
-4
C2 560 PF
CR10
(+.4)
CR9
R6 3K
C4 300 PF
R7 51K
CR12
-4
+15
CR11
-4
R5 3K
C3 300 PF
R3 51K
CR6
CR7
(-3)
C1 560 PF
R8 1300
-15
Q1
(ON)
CR5
-4
R2 8200
+15
+15
-4
-15
CR3
CR4
(0)
"1" OUTPUT
31
29
32
30
SET GATE OUTPUT
SET INPUT
SET CLOCK INPUT

FIGURE IV-9

accessible thru a direct connection which may be used in two ways. First a diode remotely located from the FF card may be connected to form a three input gate for additional logic control.

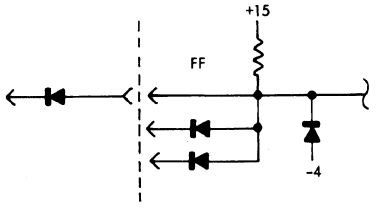


FIGURE IV -10

Second, the Set or Reset gate outputs may be wired directly to other FF inputs to provide faster triggering of successive flip-flops.

Pulse Standardizer

The logical symbol and circuit diagram for a typical Pulse Standardizer as used in this machine is shown below:

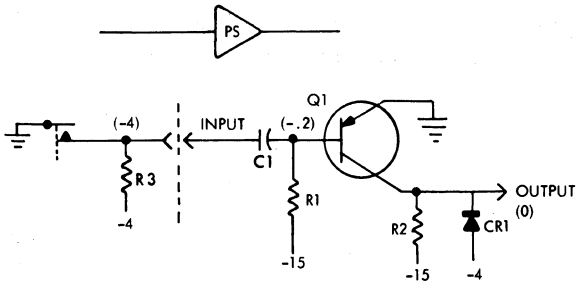


FIGURE IV-11

The circuit consists of a grounded emitter transistor (Q1), base input circuit (CIRI), collector load resistor (R2) and output clamp diode (CR1). In general the circuit requires a positive going, noise free input signal whose duration is equal to or longer than the output pulse. If the input signal is less in time than the standardized output pulse that the circuit is designed to produce, then the output will have the same duration as the input. The waveforms below show a typical input signal, from a relay for example, the signal at the base and the standardized 18μs negative output signal. Under static conditions the Input is low, -4 volts. Transistor Q1 is conducting in saturation due to resistor R1 connected to -15 volts which forward biases the base-emitter junction. Thus the base is clamped near ground by the base-emitter junction and C1 is charged to approximately 4 volts. The charge path for C1 is from -4 volts thru resistor R3 to the left hand plate and from the right hand plate thru the base-emitter junction to ground. With Q1 conducting the Output is at ground or is slightly negative. Diode CR1 is reverse biased and cutoff.

When the input signal switches from -4 volts to ground the positive going voltage signal is coupled thru C1 to the base of Q1 which cuts the transistor off. With Q1 cutoff current flow from -15 volts thru R2 and CR1 clamps the output to approximately -4 volts.

The transistor will remain cutoff until C1 discharges to a point where the base-emitter will become forward biased and the transistor will conduct. The discharge path for C1 is from -15 volts thru R1 to the right hand plate and from the left hand plate to the ground

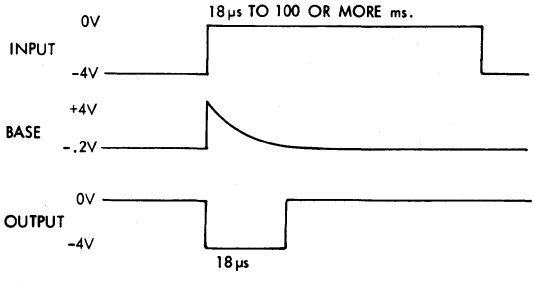


FIGURE IV-12

input source. Thus, it is primarily the time constant of C1 and R1 which determines the cutoff time for Q1 and the length of the negative output signal. Other factors including the rise time of the input signal and the switching time (from ON to OFF) of the transistor affect the discharge of the input capacitor and, consequently, the transistor cutoff time.

When the input signal returns to -4 volts, capacitor C1 again charges to approximately -4 volts thru resistor R3, and the Pulse Standardizer must not be triggered again until the capacitor has had sufficient time to recharge.

Reset Standardizers

The Reset Standardizer (RS) card provides direct reset pulses to the Flip Flop Reset Input for most of the flip-flops. Four output stages are triggered from a common input. Three of these stages; the outputs of which are labeled Reset 1 (R1), Reset 2 (R2) and Reset 3 (R3), produce pulses which can reset 20 FF each. The fourth output, labeled Delay Machine Reset (Δ MR), is a 12-20 μs pulse which is produced following the reset pulses and is used to initate electronic operation immdeiately after the FF's are reset.

A block diagram is shown below:

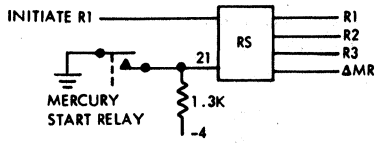


FIGURE IV-13

At the beginning of each machine operation, the RS is triggered when the Mercury Start Relay contacts pulse the RS input. The RS produces pulses at the R1, R2, R3 and ΔMR outputs. An additional trigger input is provided for Reset 1 only. This is the initiate R1 input which is provided so that the DDFF's can be reset independently of the Mercury Start pulse. Reset 1 output resets the following 15FF's; DDO thru DDMSD; DDU; and the DDT. A logic diagram of the entire Reset Standardizer card is shown on figure 14. Pin 21 is the trigger input from the Mercury Start Relay. Each time the relay is energized the R1, R2, R3 and Δ MR signals will be produced. The Reset 1 Standardizer may also be triggered independently by the logic circuits. For this reason, it is triggered by Reset 3 thru an Inverter stage which produces the same signal level as the logic circuits.

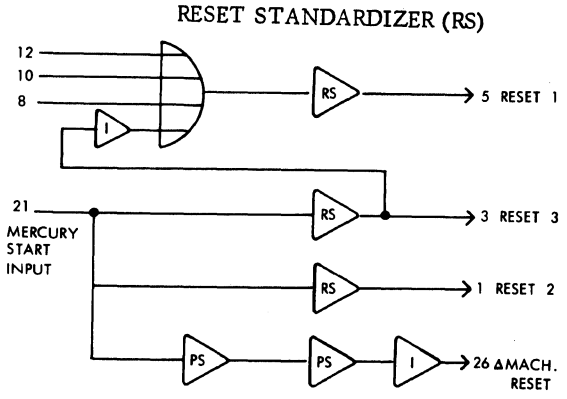


FIGURE IV-14

The three Reset Standardizer stages, as shown on figure 18, employ 2N1998 transistors which are connected in normally conducting pulse standardizer circuits. The output of each of these circuits is normally at ground. When the circuit is triggered the transistor is cut off for a period of time determined primarily by the resistor-capacitor (RC) in the base circuit. During this cutoff time, the output goes to -15 volts due to the 1K ohm resistor connected to -56 volts and the clamp diode connected to -15 volts.

Reset 2 (R2)

The required triggering input at pin 21 is a positive voltage step (-4.0 volt to ground) which must be noise free to give reliable circuit operation. For this reason, a relay (mercury start) with mercury wetted contacts is used to provide the trigger signal. Before the relay is energized, pin 21 is at -4 volts due to the 1.3K ohm resistor as shown on figure 13. Reset Standardizer R2 is conducting because its base-emitter is forward biased by the 2K ohm base resistor connected to -15 volts. Without a trigger the R2 output is at ground. The 1K ohm collector load resistor is located externally to the RS card due to power dissipation and physical size limitation. The transistor base will be slightly negative, and the pin 21 at -4 volts, thus, the input .1 UF capacitor will be charged to -4 volts

After the Mercury Start relay is energized, the input pin 21 will go to ground. This positive step voltage will be coupled by the .1 UF capacitor to the base of the 2N1998. The transistor base-emitter will be reverse biased and the transistor will be cut off. The collector will start for -56 volts but will be clamped at -15 volts by diode KK39TT. The Input and Output signals are shown below:

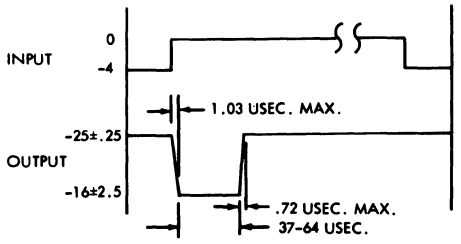


FIGURE IV-15

The output pulse will last until the .1 UF capacitor has discharged thru the 2K ohm resistor to the point where the base-emitter of the transistor is again forward biased. At this point the transistor will again conduct and its collector will return to ground. No output pulse is produced when the relay opens since the base-emitter will remain forward biased. The range of the output pulse length is due to parts tolerances, voltage supply variations, etc.

Reset 3 (R3)

The Reset Standardizer, R3, operates in the same manner as R2. Its collector is normally at ground, then goes to -15 volts for 37-64μs while the 2N1998 is cut off and returns to ground when the transistor again conducts. The Reset 3 output is also used to control an Inverter circuit which will trigger Reset 1.

Reset 1 (R1)

A four input OR gate, consisting of diodes V2CC, V4CC, V6CC, V14CC and the 16K ohm resistor connected to -15 volts, controls the triggering of R1. Reset 1 may be triggered directly by the logic at input pins 8, 10 or 12 and is also triggered each time Reset 3 is triggered thru diode V14CC.

The Inverter produces a ground signal when its transistor is conducting since the emitter is grounded. A -4 volt level is produced when the transistor is off due to the 2400 ohm resistor that is connected to -15 volts and the clamp diode that is connected to -4 volts. Before R3 is triggered, the Inverter is off due to current flow from ground at the R3 output thru the 24K ohm and 91K ohm resistors to +15 volts. The -4 volts from the collector of the Inverter is applied thru diode V14CC to the .1 UF capacitor at the input to the Reset 1 circuit. As Reset 3 is triggered, its output goes to -15 volts, the Inverter is switched on, the Inverter collector goes to ground and the positive voltage step is applied thru diode V14CC and the .1 UF capacitor to the base of Reset 1. This triggers R1 and produces the same pulse as R2 and R3. The pulse durations of R1, R2 and R3 may all be different but all will be in the range 37 to 64 μs. The Reset Standardizer circuits require a positive going signal for triggering. If the Mercury Start relay was used to trigger R1 directly thru an OR input, the output of the OR gate would remain high during the entire time the Mercury Relay was energized. This would prevent the Logic from triggering R1 thru the other OR inputs. For this reason R1 is triggered by R3 thru an Inverter which returns the OR input to -4 volts after the Reset 3 pulse ends and this allows the Logic to trigger R1 thru the other OR inputs.

Delay Machine Reset (Δ MR)

The Δ MR signal is produced each time the mercury start relay is energized. It can also be produced manually by depressing the Δ MR push button prior to single-shot Clock operation.

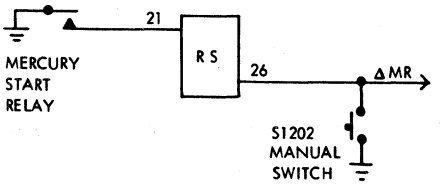


FIGURE IV-16

The signal is used together with program signals from the panel or the keyboard to set various flip-flops which must hold information prior to the start of the first electronic operation.

Although Δ MR is triggered by the start relay, it must not occur until after the R1, R2 and R3 pulses have terminated. It is produced by two Pulse Standardizers (PS) and an Inverter which employ transistors P20S, P14S and P7S. The first PS delays the ΔMR signal until after the Reset pulses have ended. The second PS produces a negative signal 12 to 20 μs in length and the Inverter converts this to the positive ΔMR signal.

Before the start relay is energized, the Input at pin 21 is at -4 volts. Transistor P20S is forward biased by the 56K ohm resistor E35N connected to -15 volts. With transistor P20S conducting thru the 2K ohm load resistor, its collector will be at approximately ground level.

The transistor P14S, used in the second PS stage, is normally conducting due to the 10K ohm resistor A17J and 47.5K ohm resistor A20J connected to -15 volts. The 10K ohm resistor establishes a threshold level for the PS base circuit so that any small voltage changes at it input will not cut it off. The P14S pulse standardizer controls the Inverter which produces the ΔMR signal and if a small positive transient were to cut off P14S, a ΔMR would be produced which could cause an erroneous electronic operation. With P14S conducting

thru the 3K ohm load resistor connected to -15 volts, its collector will be at approximate ground.

With the collector of P14S at ground, the Inverter P7S will be reverse biased due to the 2200 ohm resistor E12N and 30K ohm resistor B8K connected to +15 volts. The Inverter transistor will be off and its collector (ΔMR Output) will be low due to the 820 ohm resistor connected to -15 volts and the clamp diode connected to -4 volts

When the start relay is energized, pin 21 goes from -4 volts to ground. This positive step voltage is applied thru the 6200 PF capacitor to the base of the first PS and cuts it off. With P20S no longer conducting thru the 2K load resistor, the collector goes to -15 volts. Transistor P20S will remain cut off for 67 to 97 μs as determined by the discharge of the 6200 PF capacitor thru the 56K ohm base bias resistor. The negative voltage change at the collector of P20S is coupled thru the 680PF capacitor A29N but this does not alter the state of the second PS which continues conducting. When the 6200PF capacitor in the input to the first PS has discharged to the point where the base-emitter is again forward biased, the first stage will again conduct. Its collector will go from -15 volts to ground and this positive step voltage will trigger the second PS stage.

As the collector of P20S goes from -15 volts to ground, the positive signal is coupled thru the 680PF capacitor to the base circuit of the second PS which cuts off transistor P14S. As the collector current stops flowing thru resistor D15M, the collector goes to -5 or -6 volts which forward biases the Inverter transistor P7S. The second PS will remain cut off for 12 to 20 μs as the 680PF capacitor discharges thru the 47.5K ohm resistor. After the capacitor discharges to the point where the base-emitter of P14S is again forward biased, transistor P14S will again conduct and its collector will return to ground.

When transistor P14S is conducting and its collector is at ground, the Inverter transistor P7S is reverse biased and cut off. Its collector is clamped at -4 volts thus the ΔMR signal is low. When the second PS is triggered and its collector goes to -5 or -6 volts, the Inverter is forward biased and conducts. Its collector goes to ground and the ΔMR signal becomes high. The second PS is cut off for 12-20 μs thus the Inverter conducts for 12-20 μs. The ΔMR signal is shown below:

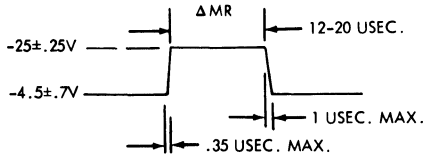


FIGURE IV-17

After the second PS again conducts, the Inverter will be reverse biased and the ΔMR signal will return to -4 volts. The 560PF capacitor is included to provide minimum turn off time for the Inverter transistor.

RESET STANDARDIZER

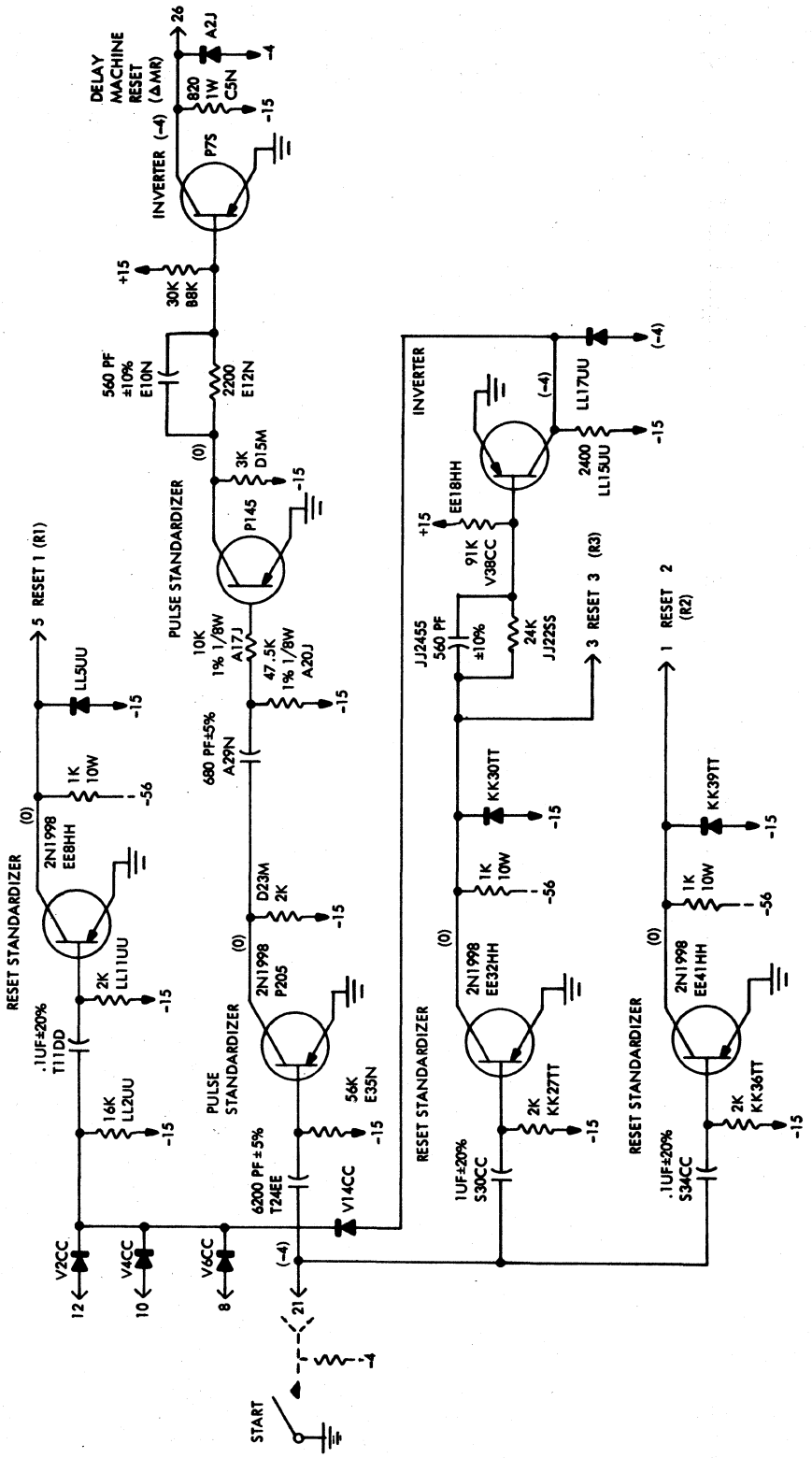


FIGURE IV-18

CLOCK SYSTEM

Clock pulses are the basic timing pulses used to synchronize the various electronic operations that take place during a machine cycle. The CLOCK is a continuous stream of regularly spaced pulses which are supplied to the Electronic Arithmetic and Memory Unit whenever the machine power is turned on. The GATED CLOCK is one or more pulses, occuring at the same time as CLOCK, which are supplied to the Electronic Unit only when gated by logic signals.

Since most electronic operations in the machine require CLOCK pulses, gated with logic, to begin each sequence of an operation, the basic speed at which the Electronic Unit operates is governed by the repetition rate at which CLOCK pulses occur. Since the Clock consists of 1 μs pulses separated by an 11 μs interval, the overall time period is 12 μs which is a pulse repetition frequency of approximately 85KC.

A block diagram of the Clock is shown below.

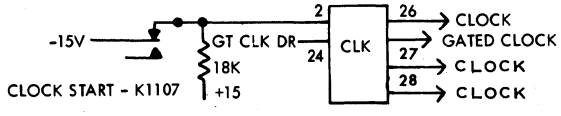


FIGURE IV-19

There are three clock outputs A, B and C which are current amplifiers that are driven by the clock multivibrator. Not all clock outputs are used on the E 2100. The clock card is designed to supply signals for future developments.

The Clock outputs are taken from pins 26, 27 and 28. The Gated Clock Driver signal is a logic signal which is applied at pin 24 to control the Gated Clock output at pin 25. Gated Clock pulses are produced only when the Gt. Clk. Dr. signal is high. A Clock start circuit is provided to ensure the Clock will start each time the machine is turned ON. The input level at pin 2 is -15 volts after the DC voltages are established when the machine is turned on. When the Clock Start relay K1107 is energized, the input level at pin 2 goes to +15 volts. This positive going signal is coupled into the Clock card thru a capacitor and insures that the Clock will start operating.

Clock Generator

The Clock Generator is a free-running oscillator or astable multivibrator circuit which uses two 2N1998 high speed switching transistors (R30T, Q1 and R21T, Q2) for its active elements. The circuit is actually two common emitter amplifiers or pulse standardizers connected so that the output of one feeds the input of the other, reference Figure 23.

When the DC voltages are applied to the Clock generator, one transistor will usually conduct more than the other due to the variations in the tolerances of the electrical components. In case both transistors come on conducting equally, a start input is provided by K1107 to guarantee the Clock Generator will start. With the Single Shot Clock removed from the machine, the inputs at pins 1 & 3 are floating.

Assuming transistor Q1 begins conducting more than Q2, the increasing current thru the 470 ohm load resistor will cause the collector voltage to become less negative. This positive going signal is coupled thru the 1800 PF capacitor to the base circuit of Q2. As the base of Q2 is pulled toward cut off by the positive signal, the collector current of Q2 thru the 1K load resistor C31L decreases and the collector of Q2 becomes more negative. This negative signal is coupled thru the 240PF capacitor, 31CC41, to the base of Q1, causing it to conduct even more. Once one transistor conducts more than the other, the switching action is very fast as one transistor is cut off and the other conducts heavily. The conducting transistor does not go into saturation because of the diode connected between its base and collector. The diode prevents the collector from becoming positive with respect to the base, thus, the transistor can be switched off more rapidly. Thus, V15CC & Z28HH are speed-up diodes.

During the time Q2 is cut off, its collector is 4 to 5 volts negative due to current flow from -15 volts thru the 1K resistor C31L, thru the base-emitter of Q3 and the 2400 ohm resistor to +15

volts. Q2 will remain cut off for 8 to 27 μs depending on the setting of the frequency adjustment control as the 1800 PF capacitor discharges thru it and the 20K ohm resistor in series. After the capacitor discharges to the point where the base-emitter of Q2 is again forward biased, transistor Q2 will begin to conduct.

As Q2 begins to conduct the increasing current thru the IK load resistor brings the collector of Q2 to ground. This positive voltage change is coupled thru the 240 PF capacitor and cuts off Q1. Transistor Q1 will remain cut off for .75 to 1.4 μs depending on the setting of the width adjustment control. After the 240 PF capacitor has discharged thru the width adjustment and 20K ohm resistor in series to the point where the base-emitter of Q1 is again forward biased. Q1 will again conduct and Q2 will be cut off. The diode C24L clamps the collector of Q1 at -4 volts during the time Q1 is cut off.

Each time the machine is turned on, a positive 30 volt signal is coupled from the Clock Start relay thru the 560 PF capacitor LL33UU to the base of Q2. This signal will momentarily reduce the conduction of Q2 and insures the Clock Generator will start operating. The output from the Clock Generator is taken from the collector of Q2 which is connected to the base circuit of the emitter-follower driver Q3.

Clock Driver

Transistor NN39RR (Q3) is connected in an emitter-follower circuit which provides current to drive the base circuits of the Clock and Gated Clock Output Drivers. The signal from the collector of Q2 will, when properly adjusted, be at or near ground for 1μs and negative for 11μs. When the base of Q3 is at ground, the emitter-follower will be conducting and its emitter will also be near ground. When the base of Q3 is negative the emitter-follower will conduct heavily and its emitter will go to -4 volts. Diode L43U is a lower clamp for the collector of Q3 and is connected to -4 volts. Diode C21L prevents the emitter from ever going above ground.

Clock Output Driver

The Clock Output Drivers Q4, Q5 and Q6 have the capacity for driving up to 32 flip-flops each and under full load, the output signal level from this emitter-follower will not deteriorate any further than -3.8 to -3.7 volts. The Clock Output waveform is shown below:

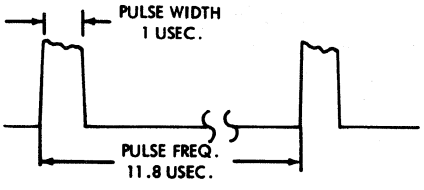


FIGURE IV-20

Gated Clock

Diodes V3CC & V9CC form a two input AND gate together with resistor C3L. This AND gate controls the output of the Gated Clock Output Driver. One input to the gate is the standard clock waveform from transistor Q3. The second input at pin 24 is controlled by the logic. Whenever the Gt Clk Dr Signal is high during Clock time, a Gated Clock Pulse will be produced. Waveforms are shown below:

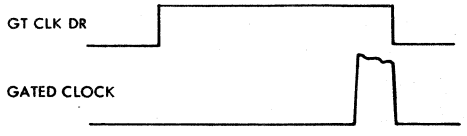


FIGURE IV-21

The Gated Clock Output has the capacity for driving up to 8 flip-flops.

Tests & Adjustments

Clock Pulse

Using an accurately calibrated oscilloscope, observe the Clock pulse at E3A-26 which is the output from the emitter of Q4. Synchronize the oscilloscope internally. The pulse width and frequency should be as shown below:

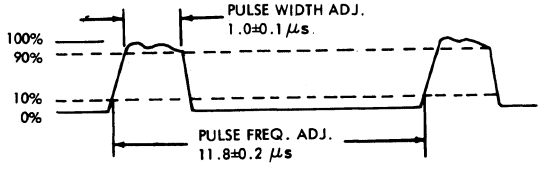


FIGURE IV-22

To Adjust:

(a) Turn the pulse width adjustment control.

(b) Turn the frequency adjustment control.

(c) Recheck the Clock pulse width and readjust the pulse width adjustment control if necessary.

Reason:

To ensure correct Clock pulses.

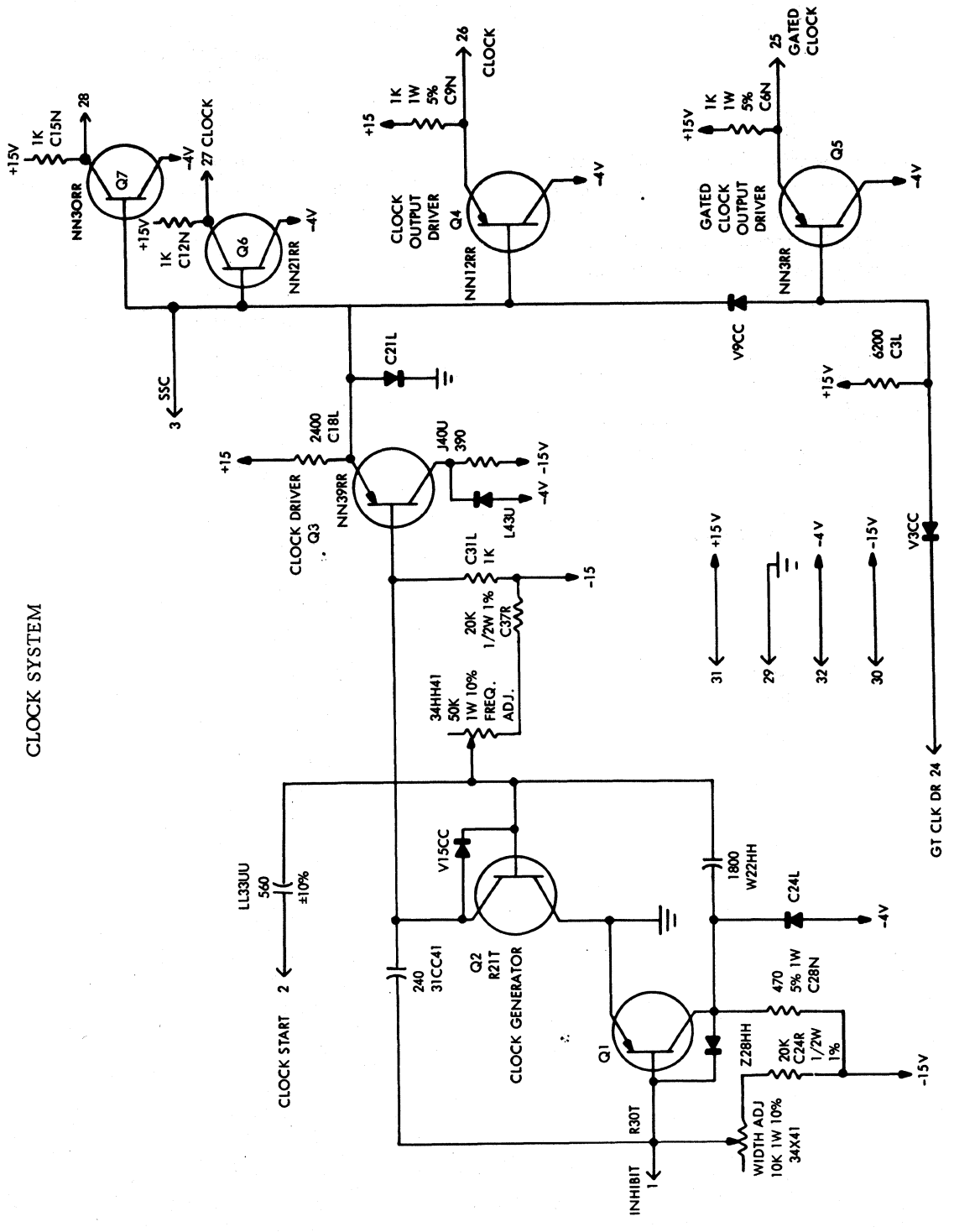

CLOCK SYSTEM
+15V
1K C15N
28
NN30RR
Q7
-4V
27 CLOCK
+15V
1K C12N
Q6
NN21RR
-4V
+15
1K 1W 5% C9N
26 CLOCK
CLOCK OUTPUT DRIVER Q4
NN12RR
-4V
+15V
1K 1W 5% C6N
25 GATED CLOCK
GATED CLOCK OUTPUT DRIVER Q5
NN3RR
-4V
V9CC
SSC 3
C21L
+15
2400 C18L
CLOCK DRIVER Q3
NN39RR
J40U 390
-4V -15V
L43U
+15V
6200 C3L
V3CC
C31L 1K
-15
20K 1/2W 1% C37R
34HH41 50K 1W 10% FREQ. ADJ.
31 +15 V
29
32 -4 V
30 -15V
GT CLK DR 24
LL33UU 560 ±10%
CLOCK START 2
V15CC
240 31CC41
Q2 R21T CLOCK GENERATOR
1800 W22HH
C24L
-4V
470 5% 1W C28N
Z28HH
20K C24R 1/2W 1%
-15V
Q1
R30T
WIDTH ADJ 10K 1W 10% 34X41
INHIBIT 1

FIGURE IV-23

SINGLE SHOT CLOCK

The Single Shot Clock (SSC) is used to produce an output pulse of approximately the same width and amplitude as the standard clock output. Its main purpose is an aid in trouble-shooting. The SSC output is triggered by operating a pushbutton switch S1204. When the SSC card is installed in the machine, the Clock Generator on the CLOCK card is inhibited and the signal produced by the SSC is used to drive the Clock Output Driver.

A block diagram of the Clock & Single Shot Clock Cards is shown below:

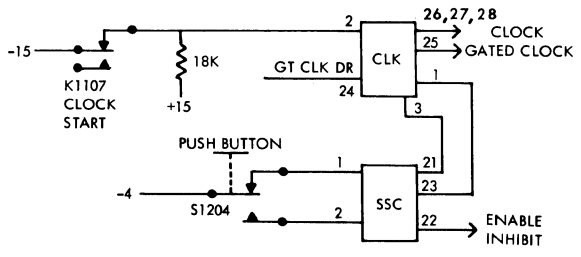


FIGURE IV-24

Each time the pushbutton is depressed, a single Clock pulse will be produced at pin 26 and/or pin 25 of the Clock card. The ENABLE INHIBIT signal is used to control the Inhibit Drivers which are associated with the Core Memory. When the SSC card is not installed and the Clock generator is running, the Inhibit Drivers are turned on shortly after a Clock pulse and turned off by the next Clock pulse. During SSC a Write operation might be initiated by depressing the button and the Inhibit Drivers would be turned on. They would remain on until the button was depressed again. This is not desirable because the Inhibit Drivers are not designed for continuous operation. The Enable Inhibit Signal from SSC will be high only as long as the button switch is depressed. Once it is released the Enable Inhibit will return to -4 volts and turn off the Inhibit Drivers.

The SSC circuitry, shown on figure 26, consists of a flip-flop which, under control of the Pushbutton S1204, triggers a pulse standardizer. The output of the pulse standardizer is then inverted to produce a positive pulse which drives the Clock Output Driver and a single Clock pulse results.

Transistor Q1, Q2 and associated components make up the SSC flip-flop. Before the button is depressed Q1 is conducting & Q2 is off. The two 1300 ohm resistors D35M and Z21S form a resistor OR gate together with the 22K ohm resistor connected to +15 volts. The -4 volts thru the normally closed contacts of the pushbutton forward biases Q1 and it conducts thru the 2400 ohm load resistor M30D. With Q1 conducting its collector is near ground. The two 1300 ohm resistors S19Z and Z17S form a resistor OR gate together with the 22K ohm resistor M24D connected to +15 volts. This OR gate controls the base circuit of Q 2. With one OR input not connected (button not depressed) and the other input at ground from the collector of Q1, transistor Q2 is reverse-biased and cutoff. Its collector is clamped at -4 volts due to the 2400 ohm load resistor M22D connected to -15 volts and the clamp diode M19D. The Enable Inhibit line is at -4 volts which prevents any Inhibit Drivers from conducting and the -4 volts from the collector of Q2 is also applied thru the OR gate to hold Q1 conducting.

When the button is depressed the -4 volts is switched from the OR input of Q1 to the OR input of Q2. This triggers Q2 and it conducts thru the 2400 ohm load resistor connected to -15 volts. With Q2 conducting its collector switches from -4 volts to ground and this input to the base of Q1 reverse biases Q1 & it cuts off, (the other OR input to Q1 is open since the button is depressed). As Q1 cuts off its collector is clamped at -4 volts due to the load resistor M30D and clamp diode M27D. The -4 volts from the collector of Q1 is fed back to the base of Q2 and insures it will continue conducting even if the pushbutton switch contact bounces. This feedback insures

only one trigger pulse into Q3 each time the button is depressed. During the time the button is depressed, the Enable Inhibit line will be at ground which will allow the Inhibit Drivers to conduct if a Write operation is in progress.

When the button is released, Q1 is again switched on and in turn Q2 is switched off due to the ground signal from the collector of Q1. Once Q2 switches off the -4 volts from its collector is fed back thru the resistor OR to keep Q1 conducting in case the pushbutton switch contact bounces on release. This insures that once Q2 is switched off when the button is released, it will not be triggered again and produce a second clock pulse for one switch depression. Once the button is released and Q2 switches off, its collector is clamped at -4 volts and the Enable Inhibit line is also at -4 volts which shuts off any Inhibit Drivers which may have been conducting.

Pulse Standardizer

since its base-emitter is forward biased by the 15K ohm resistor JJ34AA and the frequency adjusting Pot. at 31Y43 connected to -15 volts. When the pushbutton is depressed and the collector of Q2 switches from -4 volts to ground, the positive voltage signal is coupled thru the 330 PF capacitor 8FF19 to the base of Q3 and cuts it off. Transistor Q3 will remain cut off for 1 to 2 s as the 330 PF capacitor discharges thru 15K ohm base resistor and 10K Pot. Once the 330 PF capacitor discharges to the point where Q3 is forward biased, Q3 will again conduct. When Q2 is switched off after the pushbutton is released, no output pulse will be produced since a negative signal at the base of Q3 does not alter its conducting state.

Inverter

The Inverter circuit involving transistor Q4 inverts the negative clock pulse from the pulse standardizer Q3 and the Inverter output becomes the Single Shot positive Clock pulse which is routed to the Clock card, pin 3, to drive the Output Clock emitter-follower. When Q3 is conducting, its collector is at ground. This ground level causes the base-emitter of Q4 to be reversed biased due to the 4300 ohm resistor 26PP19 and 82K ohm resistor M17D connected to +15 volts. With Q4 cutoff, its collector is clamped at -4 volts by the 820 ohm load resistor connected to -15 volts and the clamp diode M8D. Thus, before the pulse standardizer is triggered, the single shot clock output is at -4 volts.

When theSSC button is depressed and Q3 cuts off, the base of Q4 goes negative due to the change current flow in the coupling network. With the base of Q4 negative, the transistor conducts and its collector goes to ground. It will remain at ground for 1 to 2 μs while Q3 is cutoff. After Q3 again conducts, Q4 will again be reverse biased, and the output will return to -4 volts. The 560PF capacitor is selected to provide minimum turn off time for Inverter transistor. Thus, for each depression of the Single Shot Clock push button, a single positive clock pulse is produced.

Clock Inhibit

When the SSC card is installed a circuit is completed from +15 volts thru a 8200 ohm resistor M4D to the base of Q1 transistor of the Clock Generator on the Clock card and this stops the operation of the Clock Generator during the time the SSC card is in use.

The Clock output, pin 26 and Gated Clock pin 25, when triggered by Single Shot Clock is shown below:

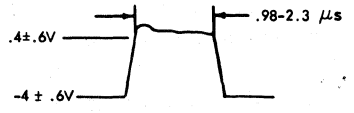


FIGURE IV-25

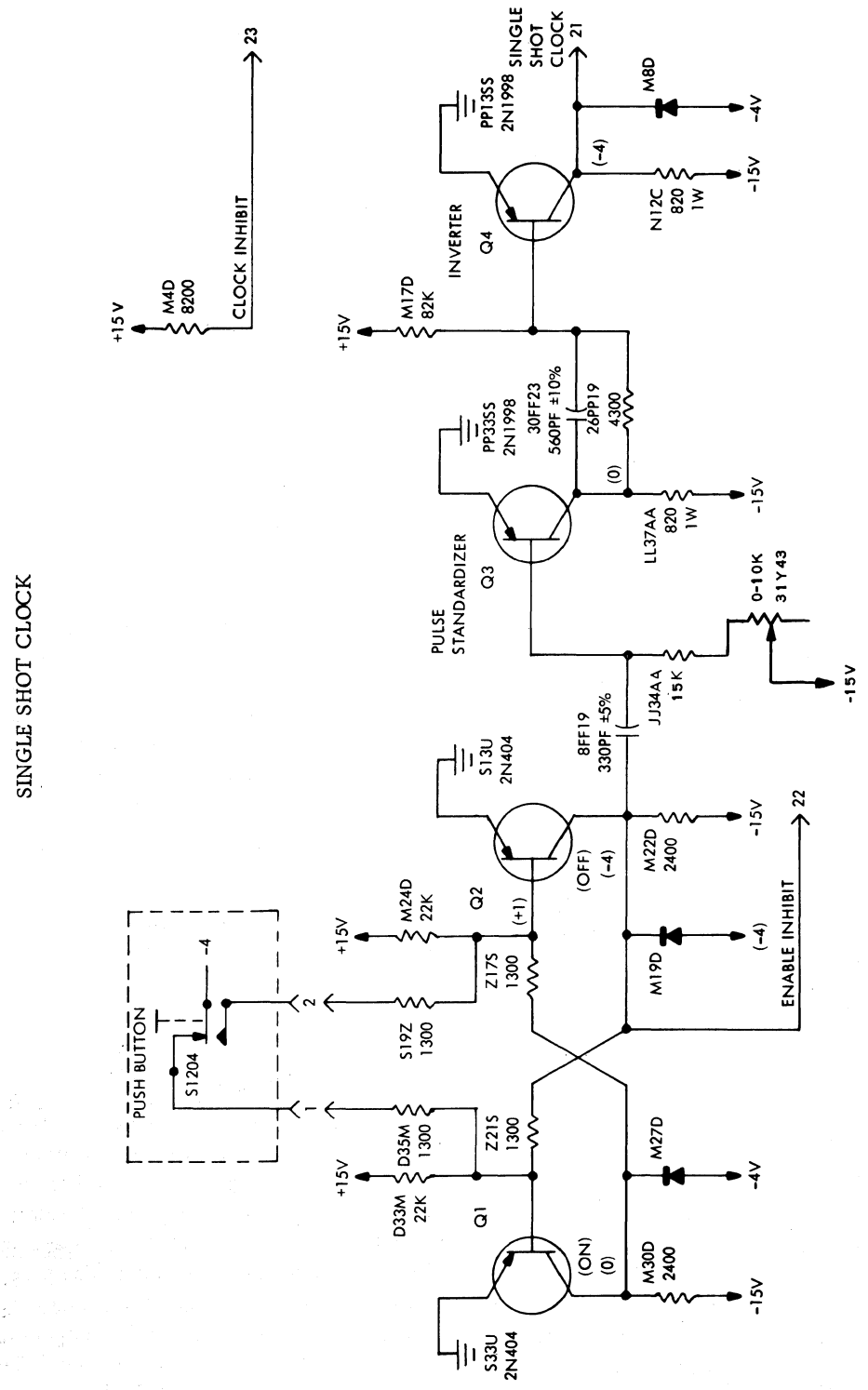

SINGLE SHOT CLOCK
+15 V
M4D 8200
CLOCK INHIBIT
23
INVERTER
Q4
PP135S 2N1998
SINGLE SHOT CLOCK
21
M8D
-4V
-15V
N12C 820 1W
(-4)
+15V
M17D 82K
PP33SS 2N1998
30FF23 560PF ±10%
26PP19 4300
(0)
LL37AA 820 1W
-15V
PULSE STANDARDIZER
Q3
0-10K 31Y43
-15V
JJ34AA 15K
8FF19 330PF ±5%
S13U 2N404
(OFF)
(-4)
M22D 2400
-15V
22
ENABLE INHIBIT
M19D
(-4)
Q2
(+1)
M24D 22K
+15V
Z17S 1300
S19Z 1300
PUSH BUTTON
S1204
-4
2
D35M 1300
Z21S 1300
+15V
D33M 22K
Q1
(ON)
(0)
M27D
-4V
M30D 2400
-15V
S33U 2N404

FIGURE IV-26

MEMORY CIRCUITS

MEMORY CARD

The purpose of the memory card is to store information in binary form. The memory card contains the four plane core memory package which consists of the magnetic cores, the X lines, Y lines, inhibit windings and sense windings. The memory card also contains disconnect diodes, which allow the read drivers to cause current flow in one direction through the X and Y lines and the write drivers to cause current flow in the same lines but in the opposite direction. The sense pre-amplifier is located on the memory card but is described elsewhere in this section. The Y lines furnish the word selection and the X lines furnish the digit selection. The following descriptions refer to the schematic on figure 27 and assume the read or write of a core selected at the intersection of the WD1 and DG1 lines.

Y Lines

The Y lines determine what is commonly termed word selection and also provide a half current for switching the core in either the read or write direction. During a read operation, current flows from the read driver Y1, through Y line WD1 & diode 38 to read driver Y6R. This provides a half current for all word one cores. The reverse of the current flow through this line occurs during the write operation.

X Lines

The X lines determine the digit selection and also provide a half current for switching the cores in either the read or write direction. During the read operation, current flows from the read driver X(1-5) through X line DG1, diode 51 to read driver X7R. This provides a half current to the digit one cores. The reverse of the current flow through this line occurs during the write operation.

The coincidence of the X and Y line currents flowing through a core in the same direction, causes the core to switch if it is not already magnetically oriented in this direction.

Inhibit Winding

The inhibit winding is used only on the write or clear memory operation. It is used during the write when a core is not to be switched and furnishes a half current in an opposing direction to the Y line current. This cancels the effect of the Y line and prevents the core switching.

Current will flow from -15 volts through the 28.7 ohm resistor, the 30.9 ohm resistor and the inhibit winding I1-CU, to the inhibit driver which is at ground level. The 28.7 ohm and 30.9 ohm resistors are for current limiting purposes. The 4700 pf capacitor is a peaking capacitor to help shape the leading edge of the inhibit signal. A full current is passed through each inhibit winding and causes all the cores to orient in the O state during a clear memory operation.

Sense Winding

The sense winding is covered under the heading SENSE PRE-AMPLIFIER.

Sense Amplifier - MR

The primary purpose of the Sense Amplifier - MR circuit is to provide a means of sensing the switching of magnetic polarity in a memory core and temporarily storing this information in a flip-flop in order to control the logic elements. The sense amplifier - MR circuit also provides a means of pulse amplitude discrimination and gating in order to set the flip-flop only at a precise time during the read sequence. This prevents erroneous setting of the flip-flop from low amplitude pulses generated by partial core switching, noise pulses or the switching of the cores during the write sequence.

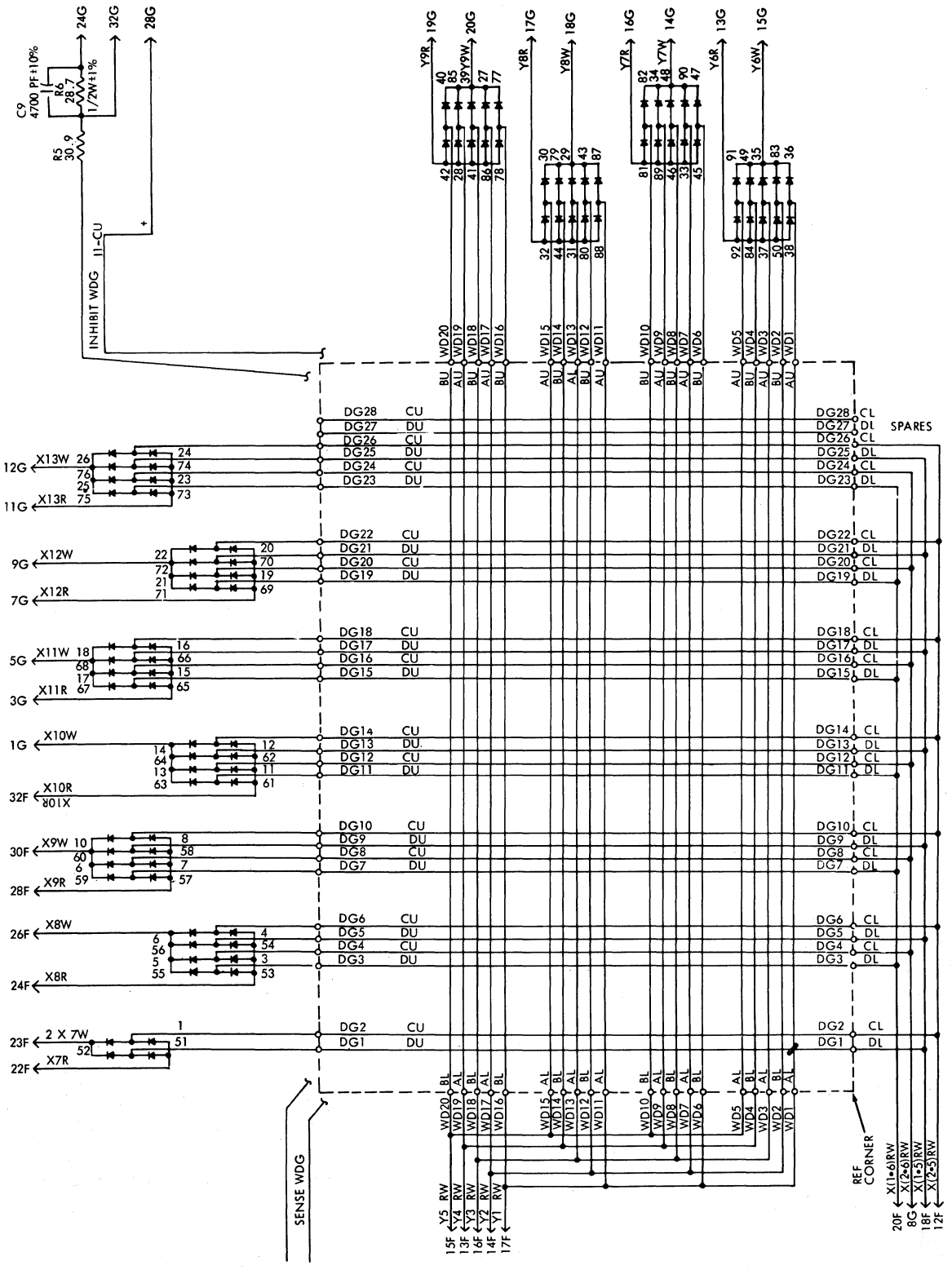

C9 4700 PF±10%
R6 28.7 1/2W±1%
R5 30.9
24G
32G
28G
+
11-CU
INHIBIT WDG
Y9R 19G
Y8R 17G
Y8W 18G
Y7R 16G
Y7W 14G
Y6R 13G
Y6W 15G
WD20 WD19 WD18 WD17 WD16
WD15 WD14 WD13 WD12 WD11
WD10 WD9 WD8 WD7 WD6
WD5 WD4 WD3 WD2 WD1
DG28 CU
DG27 DU
DG26 CU
DG25 DU
DG24 CU
DG23 DU
DG22 CU
DG21 DU
DG20 CU
DG19 DU
DG18 CU
DG17 DU
DG16 CU
DG15 DU
DG14 CU
DG13 DU
DG12 CU
DG11 DU
DG10 CU
DG9 DU
DG8 CU
DG7 DU
DG6 CU
DG5 DU
DG4 CU
DG3 DU
DG2 CU
DG1 DU
SPARES
REF CORNER
SENSE WDG
X13W
X13R
X12W
X12R
X11W
X11R
X10W
X10R
X9W
X9R
X8W
X8R
2 X 7W
X7R
Y5 RW
Y4 RW
Y3 RW
Y2 RW
Y1 RW
X(1•6)RW
X(2•6)RW
X(1•5)RW
X(2•5)RW

FIGURE IV-27

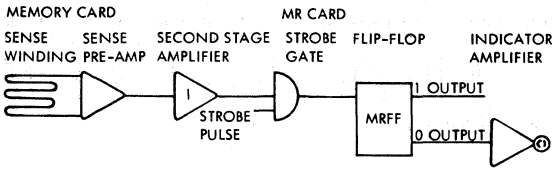


FIGURE IV-28

The following circuit descriptions refer to the schematic on figure 30.

Sense Pre-Amplifier

The sense winding and pre-amplifier are located on the memory card. The sense winding passes through all the cores on one plane of the memory and has a voltage induced in it when any of the cores through which it passes experiences a change or reversal (switch) of the flux. Due to the core orientation and the installation pattern of the sense winding, a switching core may induce a positive or negative pulse in the sense winding. Therefore, the following stage must be capable of handling both positive and negative pulses. The sense winding terminates in the primary of a 1:3 ratio pulse transformer and the two capacitors across the winding are noise suppressors. The sense pulse transformer has a center tapped secondary which is directly coupled to the bases of a pair of transistors which are connected in a symmetrical difference amplifier configuration and biased in the class AB range. The two 5uf capacitors from +15 and -15 to ground, at the bias voltage divider, are noise suppressors. The 825 ohm resistors, between +15 and -15, form a voltage divider to supply the base bias for the pre-amplifier stage. The 15uf capacitor across the 825 ohm resistor is a filter to provide a stable bias source. When a voltage is induced in the sense winding, it is applied to the primary of the 1:3 ratio pulse transformer.

The two 1100 pf capacitors across the winding are transient noise suppressors. The voltage on the primary of the transformer produces voltages in the bifilar wound, center tapped secondary, which are out of phase and equal in amplitude with respect to the center tap. The 1000 ohm resistor across the transformer is an impedance match for the transformer. The voltage applied at the base of QA is equal in amplitude but 180 degress out of phase with the voltage applied to the base of QB. Therefore, as long as the amplitude of the signals applied to the bases of QA and QB does not exceed the cut off level between the base emitter junctions, the signals produced at the collectors will be equal in amplitude but 180 degress out of phase. Since the collectors are parallel connected, signals below this amplitude will cancel. Any inequality in the signals below the cut off amplitude may be corrected by adjustment of the 5000 ohm potentiometer in the emitter circuits; only if the proper, calibrated test equipment is available. The 15uf capacitors across the balance pot are filters to prevent any change in the static emitter bias, when the pulse currents cause a dynamic change in the emitter current.

When the sense pulse amplitude exceeds the emitter base cut off, one of the transistors is driven into the cut off region and ceases to conduct. However, the other transistor continues to conduct and causes a change in the current flowing in the 4990 ohm collector load resistor KK29TT on the MR card. This current change causes an increased voltage drop in the resistor which, in turn, causes a positive pulse to appear at the output of the sense amplifier. This circuit produces a positive pulse at its output, regardless of the polarity of the pulse induced in the sense winding. It should be remembered, however, that the pulse at the output will be the difference in the signals produced by QA and QB or only that portion created by the sense pulse amplitude greater than the emitter-base bias.

Test & Adjustment

The test and adjustment for the balance and sensitivity controls requires the use of an

accurately calibrated oscilloscope with a differential pre-amp which is not presently available to service. The Balance Pots and sensitivity should not be tampered with since misalignment may allow weak noise pulses to get through the amplifier or prevent legitimate pulses of proper amplitude getting through the amplifier.

SECOND STAGE SENSE AMPLIFIER

The second stage amplifier, strobe gate, MR flip-flop and indicator circuits are located on the MR card. The signal from the pre-amplifier is developed across the collector load resistor KK29TT. Resistor KK29TT is located on the MR card in order to provide voltage wetting of the card contacts between the memory and MR cards. The signal developed across resistor KK29TT is coupled to the sensitivity control 34EE41 by capacitor BB26PP. Sensitivity control 34EE41 and resistor KK31TT form a voltage divider to supply base bias to transistor LL13NN.

The signal from the sense amplifier is attenuated by the sensitivity control in order to vary the gain in the second stage amplifier and is then applied to the base of transistor LL13NN. Resistors JJ2UU and LL6UU form a voltage divider to supply emitter bias for transistor LL13NN. Capacitor EE8RR is a filter to insure stability of the bias voltage. Resistor HH4RR is a stablizing resistor for transistor LL13NN and capacitor HH17TT is a bypass to stablize the emitter of transistor LL13NN. The attenuated positive pulse from the sense pre-amplifier is applied to the base of LL13NN which is biased near saturation. This causes LL13NN to cut off and reduce the current through the collector load resistor KK10TT which allows the collector voltage to go to -4 volts where it is clamped by diode Y15FF.. The second stage amplifier inverts and amplifies any signal applied to its base.

Strobe Gate

The negative pulse from the second stage sense amplifier is applied to one input diode (Y13FF) of the strobe gate which is a negative AND gate. If a simultaneous negative strobe pulse is applied to diode N13W of the gate, the voltage across the resistor C15L is reduced and the voltage on the base of transistor F20J is made more negative by an amount equal to the reduction across resistor C15L. Transistor F20J is an emitter-follower, biased on at normal and applying a negative signal to its base causes its emitter to go negative by approximately the same amount. This causes an increase in current and voltage drop across the emitter load resistor B17K. Test points are provided at terminals 2 and 24 of the MR card in order to observe the signals from the second stage amplifier and strobe gate.

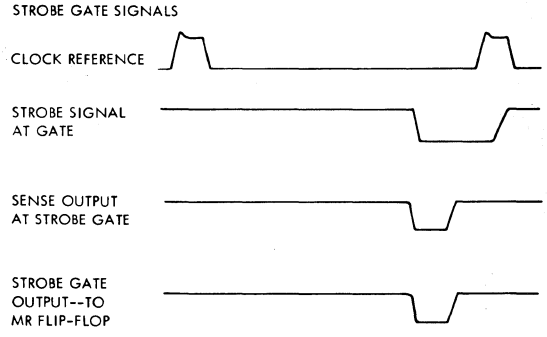


FIGURE IV-29

MR Flip-Flop

The signal from the strobe gate is applied to the input of the MR flip-flop. The MR flip-flop is of standard RTL configuration and is different from the usual flip-flop used in the E2100 in that it is directly coupled to the strobe gate and MR reset gate. This causes it to trigger at a given DC level rather than pulse amplitude. Since this is a negative trigger flip-flop and is

triggered by a negative pulse, it triggers on the leading edge of the pulse. Starting with the flip-flop in the reset state, transistor F37J will not be conducting and transistor N39R will be conducting.

Resistors B17K, P21X, B26K, P28X and C31L make up the base bias voltage divider for transistor F37J. The junction of resistors P28X and C31L is at approximately 0 volts during the reset condition due to transistor N39R conducting. The strobe is at its high level which causes the base of the emitter follower transistor F20J to be at 0 volts. Consequently, the emitter of F20J and the junction of resistors B17K and P21X are also at 0 volts. Due to the current flow from the resistors P21X and P28X through resistors B26K, the voltage on the base of F37J will be positive and the transistor will not conduct.

A negative change on the emitter of transistor F20J and the junction of resistors B17K and P21X voltage divider resistors P21X and B26K. This increases the voltage drop in resistor B26K which makes the base of transistor F37J negative and causes it to conduct. Up to this point, transistor N39R has been conducting due to the negative voltage applied to its base by the voltage divider consisting of resistors C28L, M35V, U40BB and C40L. Transistor F37J conducting causes the voltage at the junction of resistors C28L and M35V to go to ground level. This, through the voltage divider, causes the base of transistor N39R to be positive which turns it off.

Turning off transistor N39R reduces the current through resistor C31L which allows the collector voltage to go from 0 volts to -4 volts, where it is clamped by diode L23U. Changing the collector voltage of transistor N39R to -4 volts causes additional current through resistor P28X and B26K. This keeps the base of transistor J37J negative after termination of the signal from the strobe gate. Therefore, transistor F37J will continue conducting and the flip-flop will remain in its set state until it is reset. The capacitors P19X, P26X, M33V and U38BB are used to compensate for the stored base charge in transistors F37J and N39R. The flip-flop can be reset by applying the previous analysis to the reset input.

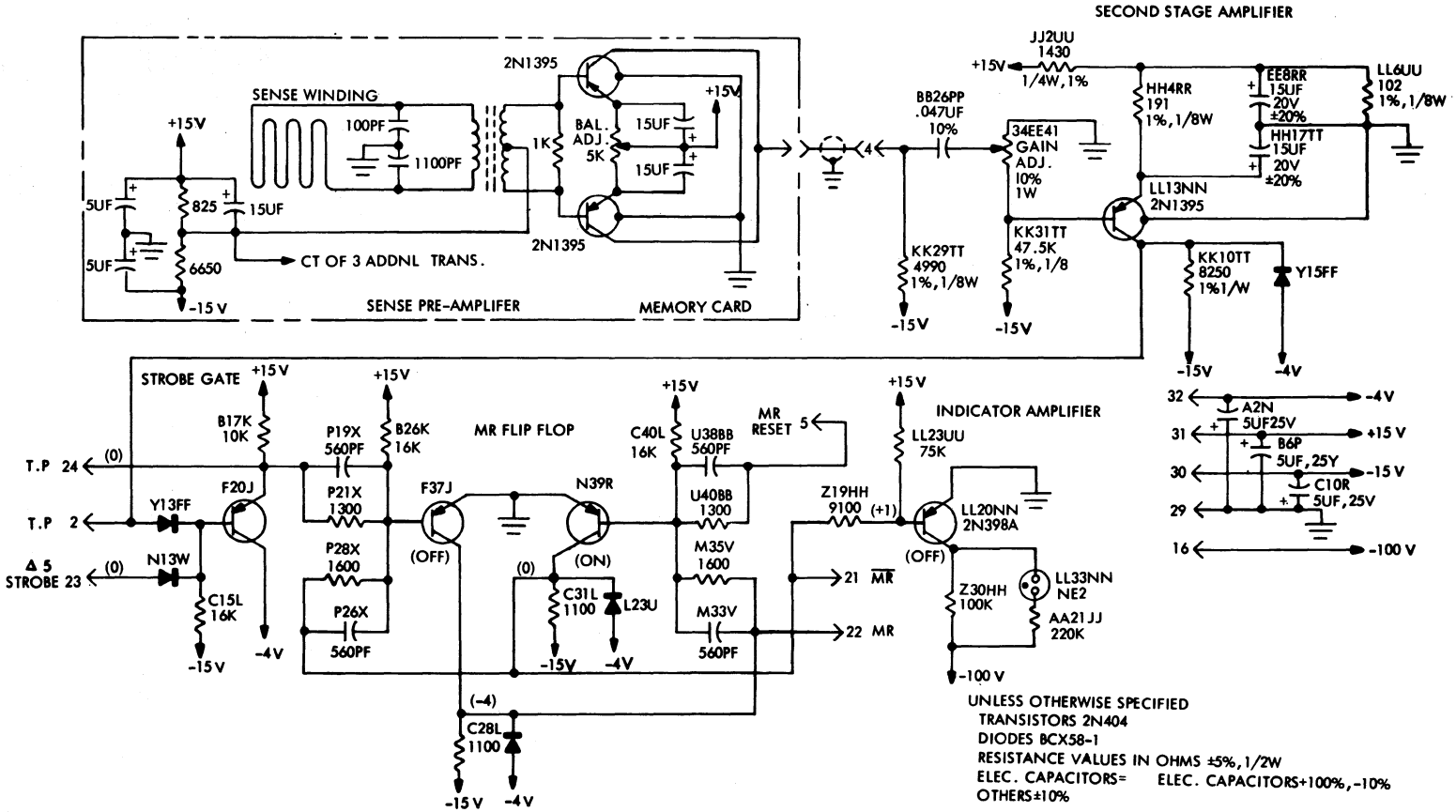
Indicator Circuit

The indicator circuit is connected to the reset side of the MR flip-flop and will be on when the flip-flop is set. The indicator circuit is a standart circuit and its description is covered elsewhere in this section.

Noise Filters

The three 5 microfarad capacitors A2N, B6P and C10R are used to filter or decouple any noise from the voltage supply lines to the MR card.

SENSE AMPLIFIER - MR



SENSE AMPLIFIER-MR

FIGURE IV-30

MEMORY DRIVER

There are two types of memory driver circuits, differing only in the output stages and commonly called driver pairs. Each is a two stage amplifier preceded by an AND gate. Four of these circuits are packaged on each MD card. The output stage of types one or two, completes the circuit between one end of a memory drive line and ground. The output stage of types three or four completes the circuit between the other end of the memory drive line and -15 volts.

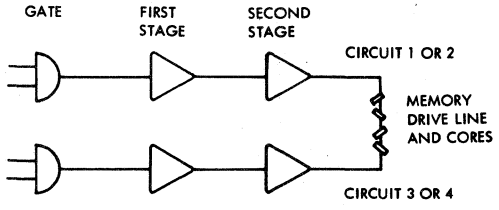


FIGURE IV-31

The following circuit descriptions refer to the schematic figure 33.

Input Gate --Circuits 1-2-3-4--

The input gate to the memory driver is basically a standard AND gate. A simultaneous positive signal at both inputs of the gate (diodes CR1 & CR2) reduces the voltage drop across the load resistor R1. This causes the voltage at the junction of the three diodes CR1, CR2 and CR3 to go positive, which through the level correction diode CR3 causes the base of Q1 to go positive. R2 is the base bias resistor for Q1. Q1 is an emitter follower and a positive voltage on its base causes a positive change in its emitter. A more detailed description of the AND gate may be found elsewhere in this section.

First Stage Amplifier --Circuits 1-2-3-4

The first stage amplifier is a driver for the output stage. The signal from the gate is developed across the voltage divider made up of R3 and R4. R3 and R4 serve as the emitter load for Q1 and base bias for Q2. Due to the voltage drop across R3, the signal applied to Q2 from the junction of R3 and R4 is slightly positive in respect to ground and cuts off Q2. The capacitor C1 is a peaking capacitor used to compensate for the stored base charge in Q2. Transistor Q2 is connected in a grounded emitter configuration which amplifies and inverts the signal and is normally conducting. The positive pulse applied to the base of Q2 cuts it off and reduces the current through the collector load resistor R5. This reduces the voltage drop across R5 and causes more current to flow through the voltage divider formed by R6 and R7.

Output Stage --Circuits 1-2--

The increased current through the base bias resistor R7 causes the voltage across it to increase, which makes the base of Q3 negative. This causes Q3 to conduct and its collector to go to approximately ground since the emitter is at ground level. This results in one end of the memory drive line being effectively at ground potential.

Output Stage --Circuits 3-4--

The increased current through the base resistor R7 causes the voltage across it to increase which makes the base of Q3 negative. This causes Q3 to conduct which causes current to flow from -15 volts through R9, R8, Q3 and into the memory drive line. R8 and R9 are current limiting resistors. Capacitor C2 is a peaking capacitor, used to shape the leading edge of the signal and improve its rise time. There is approximately 250 milliamperes of current flow from -15 volts through R9, R8, Q3 (circuit 3 0r 4), the memory drive line and Q3 (circuit 1 or 2) to ground.

Noise Filters

The two 5 microfarad capacitors 11B22 and 27B38 are used to filter or decouple any noise from the DC voltage supply lines to the memory driver card.

Driver Input and Output Signals

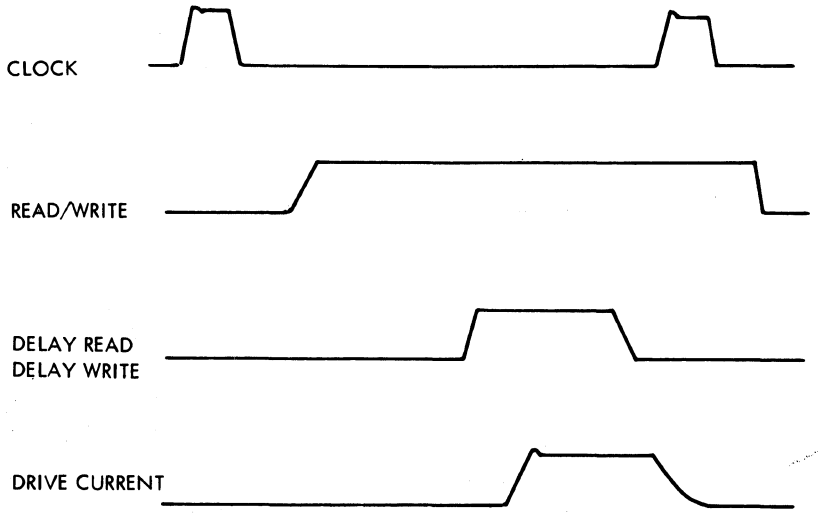


FIGURE IV-32

MEMORY DRIVER

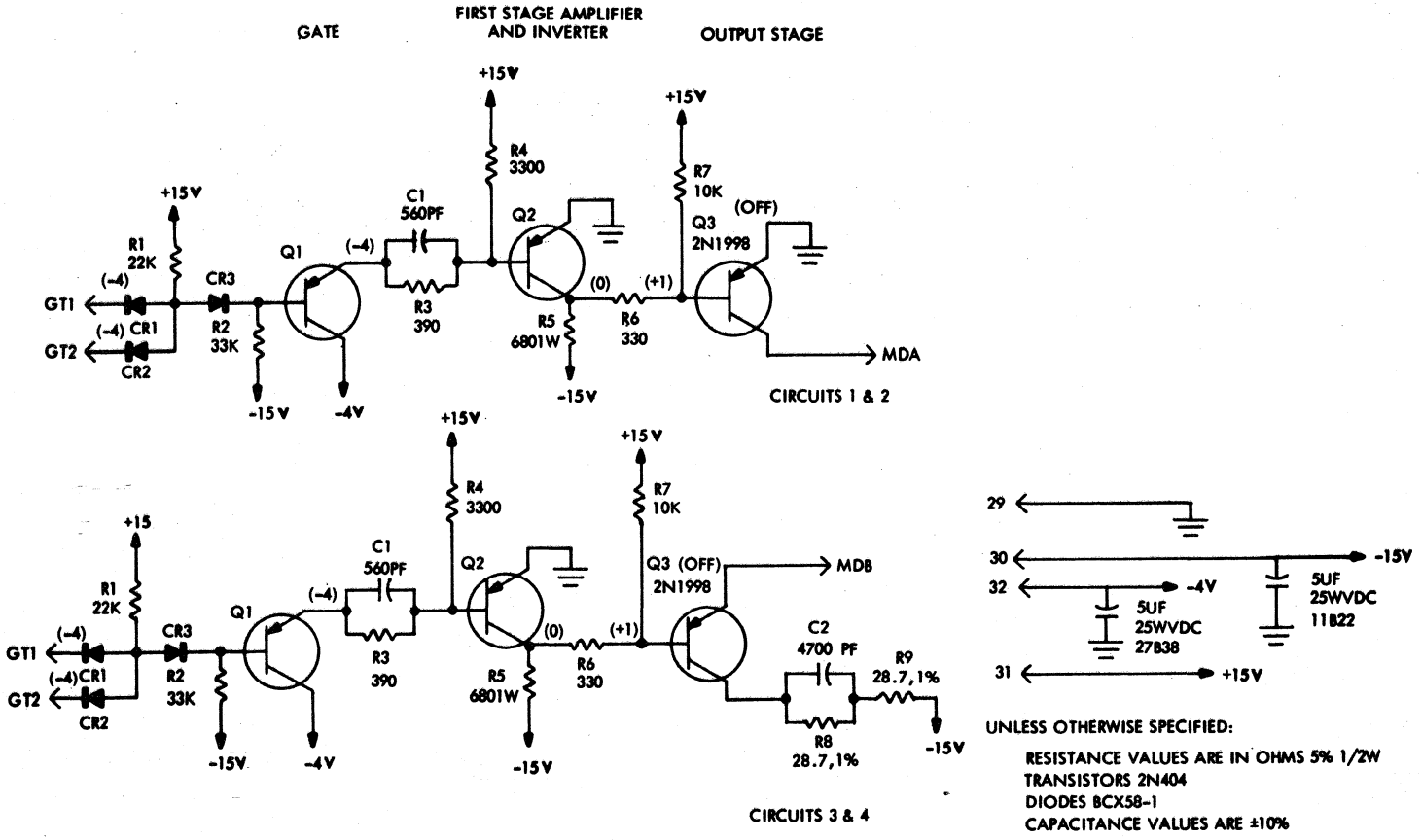


FIGURE IV-33

MEMORY TIMING A

The memory timing A circuit is used to provide some of the delayed signals and gating required by the core memory. The delayed signals are developed by a multivibrator and two pulse standardizers connected so that their delays are consecutively added. The DMV is a negative trigger circuit; therefore, it is preceded by an inverter to allow its use with the positive clock pulses. The output of the DMV is gated with write and enable inhibit to produce the gated inhibit signal. The enable inhibit signal is used only with single shot clock, otherwise, this input to the gate is disconnected. The delayed signal from the DMV is also used to trigger the first pulse standardizer which adds its delay to that of the DMV. The delayed signal from the first pulse standardizer is gated with GT-MR reset and used through a heavy buffer to produce the MR reset signal. The delayed output of the first pulse standardizer is also used to trigger the second pulse standardizer. The second pulse standardizer then adds its delay to that of the DMV and the first pulse standardizer to produce the delay three signal. Delay three is used by the memory timing B circuit. Test points are provided at terminals 21 and 13 of the MTA card in order to observe the delay one and delay two signals.

Memory Timing A Logic

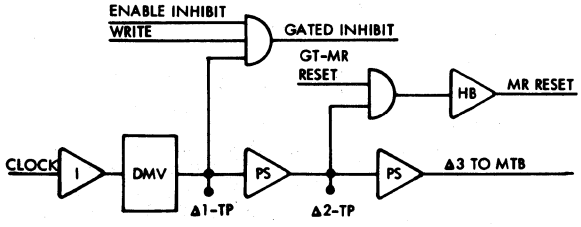


FIGURE IV-34

The following circuit descriptions refer to the schematic on figure 37.

Inverter

The inverter is a grounded emitter stage and is normally conducting due to the -4 volts applied to its input by the clock circuit. When a clock pulse occurs, a positive signal is applied to the base of transistor Q1 through capacitor N13W and the voltage divider consisting of resistors N15W and B13K. The capacitor N13W compensates for the stored base charge in Q1. The signal level applied to the base of Q1 is slightly above ground level due to the voltage drop in resistor N15W. The positive signal cuts off Q1 and reduces the collector current through resistor C15L. This allows the voltage at the collector to go negative and be clamped at -4 volts by diode U11BB. The voltage applied to the base of Q2 by the voltage divider resistors N19W and B21K will go negative due to the negative change on the collector of Q1.

DMV

Transistor Q2 is cut off and Q3 is conducting in their normal static state. The negative voltage applied to the base of O2 from the inverter stage causes it to conduct. The capacitor N17W is used to compensate for the stored base charge in Q2. When Q2 conducts, the current in resistor C28L increases causing a positive change in the voltage on the collector of Q2. This positive change on the collector of Q2 is coupled to the base of Q3 by capacitor N26Z until the capacitor discharges through the base bias resistor C30L. T_h is causes Q3 to be cut off for the duration of the RC time of capacitor N26Z and C30L. During the time Q3 is cut off collector current through resistor C36L is eliminated, allowing the voltage at the collector of Q3 to go negative and be clamped at -4 volts by diode A38J. The negative change at the collector of Q3 is applied to the base of Q2 by capacitor N21W and the voltage divider formed by resistors N23W and B21K. T_h is causes Q2 to continue conducting after the termination of the clock pulse, until the RC time of capacitor N26Z and resistor C30L allows Q3 to conduct.

When the discharge of capacitor N26Z allows Q3 to conduct the collector current through resistor C36L causes the collector voltage to go to approximately ground level. This ground level, applied to the voltage divider resistors N23W and B21K causes the base of Q2 to become positive and Q2 ceases to conduct. The DMV is now back to its static state.

Inhibit Gate

The inhibit gate is used to produce a signal (GT INHIBIT), which with other logic, allows the selected memory core on a bit plane to switch. The gate is basically a standard AND gate and its emitter-follower stage is always conducting.

Inhibit Gate Signals

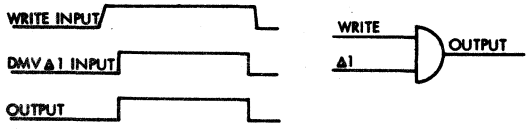


FIGURE IV-35

Assuming that the single shot clock is not being used, there is no input to terminal 25 and diode S9Z is inactive. Positive signals, simultaneously applied to diodes P29X and N31W by write logic and the DMV (delay one) cause the emitter follower to go to approximately ground level. The emitter of the emitter-follower changes a corresponding amount and produces the gated inhibit signal. A more detailed description of an AND gate may be found elsewhere in this section.

Pulse Standardizer Q5

Pulse standardizer Q5 is normally conducting in its static state. The negative signal from the DMV is applied to the base of Q5 through capacitor X33JJ. Since Q5 is conducting, the negative signal will not cause any change in its collector voltage, but capacitor X33JJ will charge through resistor JJ36SS. When the DMV times out, the positive signal from Q3 is applied to the base of Q5 by capacitor X33JJ and Q5 will cut off. When Q5 stops conducting, its collector no longer draws current through resistor JJ38SS and the voltage on its collector changes to -15 volts. Q5 remains cut off until capacitor X33JJ discharges through resistor JJ36SS and the base of Q5 again goes negative. After the RC time of capacitor X33JJ and resistor JJ36SS, transistor Q5 will conduct and its collector current through resistor JJ38SS causes the collector voltage to change to approximately ground level. This has produced the 15 volt delay two pulse.

Pulse Standardizer Q6

Pulse standardizer Q6 is normally conducting in its static state. The negative signal from pulse standardizer Q5 is applied to the base of Q6 through capacitor BB22RR. Since Q6 is conducting, the negative signal will not cause any change in its collector voltage, but capacitor BB22RR will discharge through resistor JJ36SS. When the collector of pulse standardizer Q5 goes positive, the 15 volt positive change is applied to the base of Q6 by capacitor BB22RR and causes Q6 to stop conducting. When Q6 stops conducting, its collector no longer draws current through resistor JJ28SS and the voltage on its collector goes to -4 volts where it is clamped by diode LL26UU. Q6 remains cut off until capacitor BB22RR discharges through resistor JJ30SS and allows the base of Q6 to go negative. The negative voltage on the base of Q6 causes it to conduct again and its collector current through resistor JJ28SS causes the voltage on the collector to go to approximately ground level. This has produced the 4 volt delay three pulse.

MR Reset Gate

The MR reset gate is a standard positive OR gate used in this application as a negative AND gate. The negative delay two signal from pulse standardizer Q5 applied to diode BB16KK at the same time the negative GT-MR reset signal is applied to diode BB14KK, causes the base of transistor Q7 to go to -4 volts. Transistor Q7 is an emitter follower and is always conducting. The -4 volt signal on its base causes additional current in resistor KK12TT and the emitter of transistor Q7 goes to approximately -4 volts. The signal developed by this gate is the MR reset signal.

Heavy Buffer

The heavy buffer is used to supply the current necessary to reset the MR flip-flops. The signal from the emitter of the MR reset gate transistor Q7 is applied directly to the base of Q8. Q8 is an emitter follower and any change in its base voltage causes an equal change in its emitter voltage. The signal from the emitter of Q8 is used directly to reset the MR flip-flops.

Noise Filters

The three 5 microfarad capacitors A2N, B6P and C10R are used to filter or decouple any noise from the DC voltage supply lines to the MTA card.

Memory Timing "A" Signals

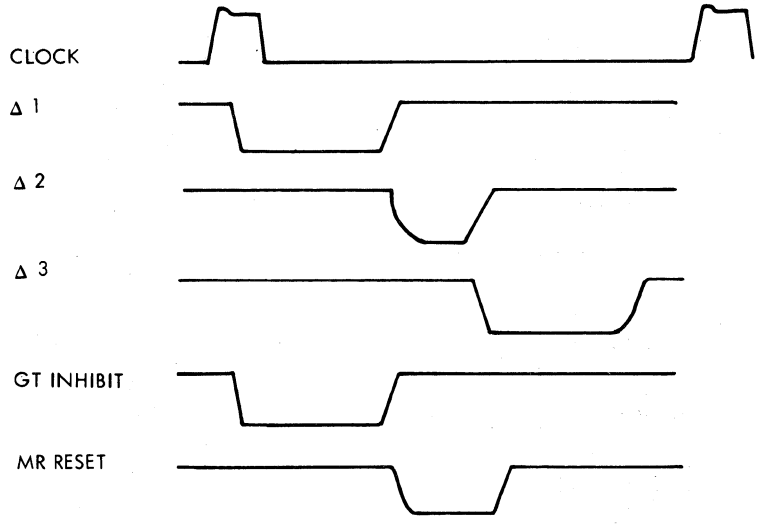


FIGURE IV-36

MEMORY TIMING "A"

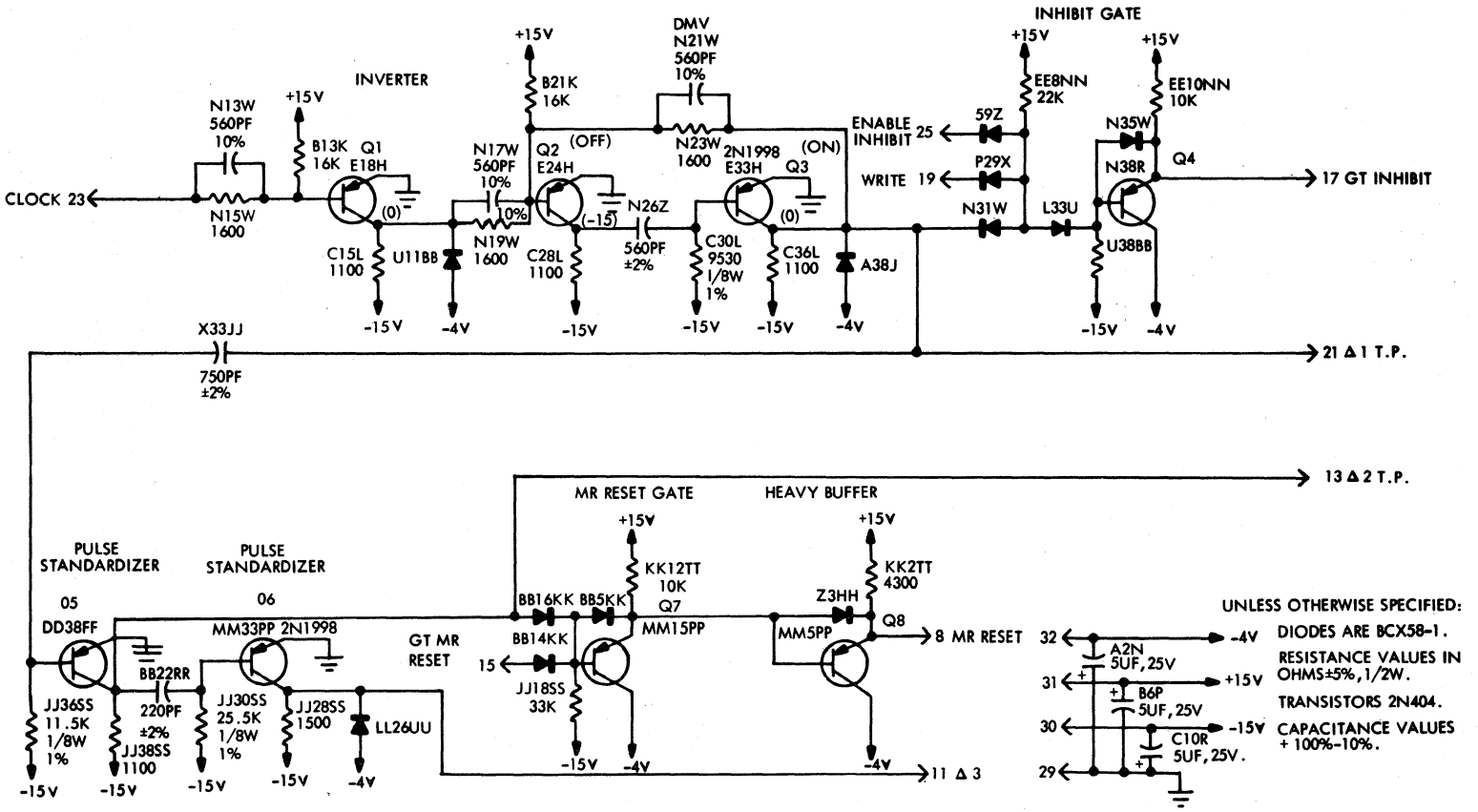


FIGURE IV-37

MEMORY TIMING B

The memory timing B circuit provides those delayed signals, not provided by the memory timing A circuit, but required by memory. MTA and MTB are essentially one unit but are separated due to the limited space available on one card. MTB provides the Delay Read, Delay Write and Strobe pulses. A negative AND gate (delay write gate) is used to gate the Delay Three signal with the Not Write signal. The output of this gate controls an inverter which produces the Delay Write signal. Another negative AND gate is used to gate the Delay Three signal with the Not Read signal. The output of this gate controls an inverter which produces the Delay Read signal. The output of the Delay Read gate also controls an inverter which triggers an adjustable pulse standardizer. The adjustable pulse standardizer produces Delay Four which is used to trigger another pulse standardizer which produces the strobe pulse.

Memory Timing B Logic

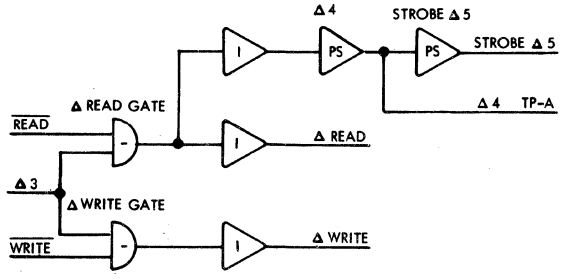


FIGURE IV-38

The following circuit descriptions refer to the schematic on Figure 40.

Delay Write Gate

The delay write gate is a standard positive OR gate used in this application as a negative AND gate. Transistor Q6 is connected in an emitter-follower configuration and is always conducting. The input to the base of Q6 is normally at ground level due to the Delay Three or Not Write signals being high. When the negative Delay Three signal is applied to Diode S14Z at the same time the Not Write signal goes low, the base of Q6 goes to -4 volts. Transistor Q6 emitter draws more current through resistor B32K and the voltage on the emitter changes to -4 volts producing a gated signal.

Delay Write Inverter

The inverter stage is biased normally off by the voltage divider resistors CC14LL and KK10TT. The emitter of Q6 is normally at ground level and the voltage drop in resistor CC14LL causes the voltage on the base of Q7 to be positive. When the emitter voltage on Q6 goes to -4 volts, the base of Q7 is made negative and Q7 conducts. Capacitor CC12LL is used to compensate for the stored base charge in Q7. When Q7 conducts, its collector current through resistor KK4TT causes the voltage at the collector to go to ground level. When the Delay Three signal is terminated, the emitter of Q6 goes to ground which through resistor CC14LL cuts off Q7. When Q7 ceases to conduct, its collector voltage goes to -4 volts where it is clamped by diode LL12UU. This change in the collector voltage of Q7 has produced the Delay Write signal.

Delay Read Gate

The delay read gate is identical to the delay write gate and the delay write circuit analysis may be used to describe it.

Delay Read Inverter Q2

The delay read inverter stage is identical to the delay write inverter stage and the same circuit analysis may be used to describe it.

Delay Read Inverter Q3

The inverter Q3 is used to invert the negative signal from the delay read gate in order to trigger the delay four pulse standardizer. Transistor Q3 is normally not conducting due to the positive voltage applied to its base by the voltage divider resistors R23Y and B34K. When Q3 is not conducting there is -15 volts on its collector due to no current flow in resistor C36L. When the signal from the emitter of the delay read gate Q1 goes to -4, a negative signal is applied to the base of Q3 which causes it to conduct. With Q3 conducting, its collector current through resistor C36L causes the voltage on the collector to go to ground level. This signal is used to trigger pulse standardizer Q4.

Pulse Standardizer Q4

Pulse standardizer Q4 is an adjustable pulse standardizer and is normally conducting. Its collector current through resistor JJ36SS causes the collector voltage to be at ground level. The 15 volt positive change on the collector of Q3 is applied to the base of Q4 through capacitor P31AA and causes transistor Q4 to cut off. Q4 will remain cut off until the capacitor P31AA discharges through the base bias resistors T35AA and 34CC41 and allows the base voltage to go negative. Resistor 34CC41 is adjustable in order to control the discharge time of capacitor P31AA which determines the length of the delay four period. With Q4 not conducting, the absence of its collector current through resistor JJ36SS lowers the collector voltage to -15 volts. After the RC time of capacitor P31AA and resistors T35AA and 34CC41, transistor Q4 will conduct and its collector current through resistor JJ36SS will cause the collector voltage to go to ground level. This produces the delay four signal which is used to trigger the strobe signal pulse standardizer. A test point is provided at pin 17 in order to observe the delay four signal.

Pulse Standardizer Q5

Pulse standardizer Q5 is normally conducting due to the negative voltage applied to its base through the base bias resistor JJ34SS. When Q5 is conducting, its collector current through resistor JJ28SS causes its collector voltage to be at ground level. The signal from the collector of Q4 is applied to the base of Q5 through capacitor X26JJ. The negative signals from the collector of Q4 do not affect Q5, since it is already conducting, but capacitor V26JJ discharges through resistor JJ34SS and transistor Q5. When the collector of Q4 goes positive, the signal is applied to the base of Q5 by capacitor X26JJ and Q5 stops conducting until capacitor X26JJ discharges through resistor JJ34SS. With transistor Q5 cut off, the absence of its collector current through resistor JJ28SS allows the collector voltage to go to -4 volts where it is clamped by diode LL26UU. After the RC time of capacitor X26JJ and resistor JJ34SS, Q5 again conducts and its collector current through resistor JJ28SS causes the collector to go to ground level. This has produced the delay five or Strobe Pulse used in reading information from the memory.

Test & Adjustments - Strobe

TEST EQUIPMENT REQUIRED: Dual trace oscilloscope. Jumper wires.

Preparatory conditions:

A. Clear memory.

B. Turn power off and remove the Print Control card (D3C).

C. Jumper the following points:

H7A-25 to -4 volts	(GT. INH)
F2A-8 to -4 volts	(S1)
G1C-6 to ground	(T2)
D3C-9 to -4 volts	(PC)

Test

1. Turn power ON to computer. First, depress and release the MR pushbutton. Next, hold the POR pushbutton down while momentarily depressing the MR pushbutton; then release the POR pushbutton. This provides a machine reset. FFP should now be ON, and FFA, FFB, and FFD should be OFF.

2. Remove the jumper at D3C-9 with the power ON. The computer should now be alternately in S3 and S4 of T2 with the DD's circulating. TO will also be ON at this time.

3. With a dual trace oscilloscope, observe the delay 5 Strobe Pulse on the A trace at H7B-15, and the output of the 2nd stage of the Sense Amplifier on the B trace at the output of each Sense Amplifier card.

   2ND STAGE SENSE AMPLIFIER OUTPUT:

1 Bit	H7C-2
2 Bit	H7D-2
4 Bit	H8A-2
8 Bit	H8B-2

Adjust

Adjust the strobe adjustment control, on the MTB card at H7B, until the negative leading edge of the delay 5 Strobe pulse occurs approximately 0.10 $\mp$ .05 microseconds after the negative leading edge of the earliest 2ND stage Sense Amplifier output pulse, at the negative 90% points of both pulses, as shown below. Trigger the oscilloscope (positive external) on the delay Read pulse at H7B-8.

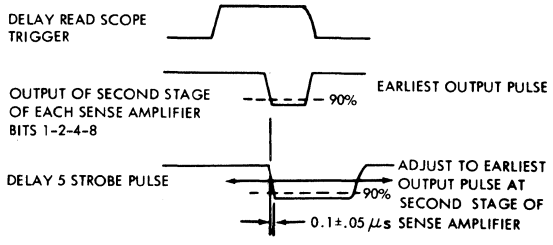


FIGURE IV-39

Turn power OFF. Remove the three remaining jumpers and replace the PC card.

MEMORY TIMING "B"

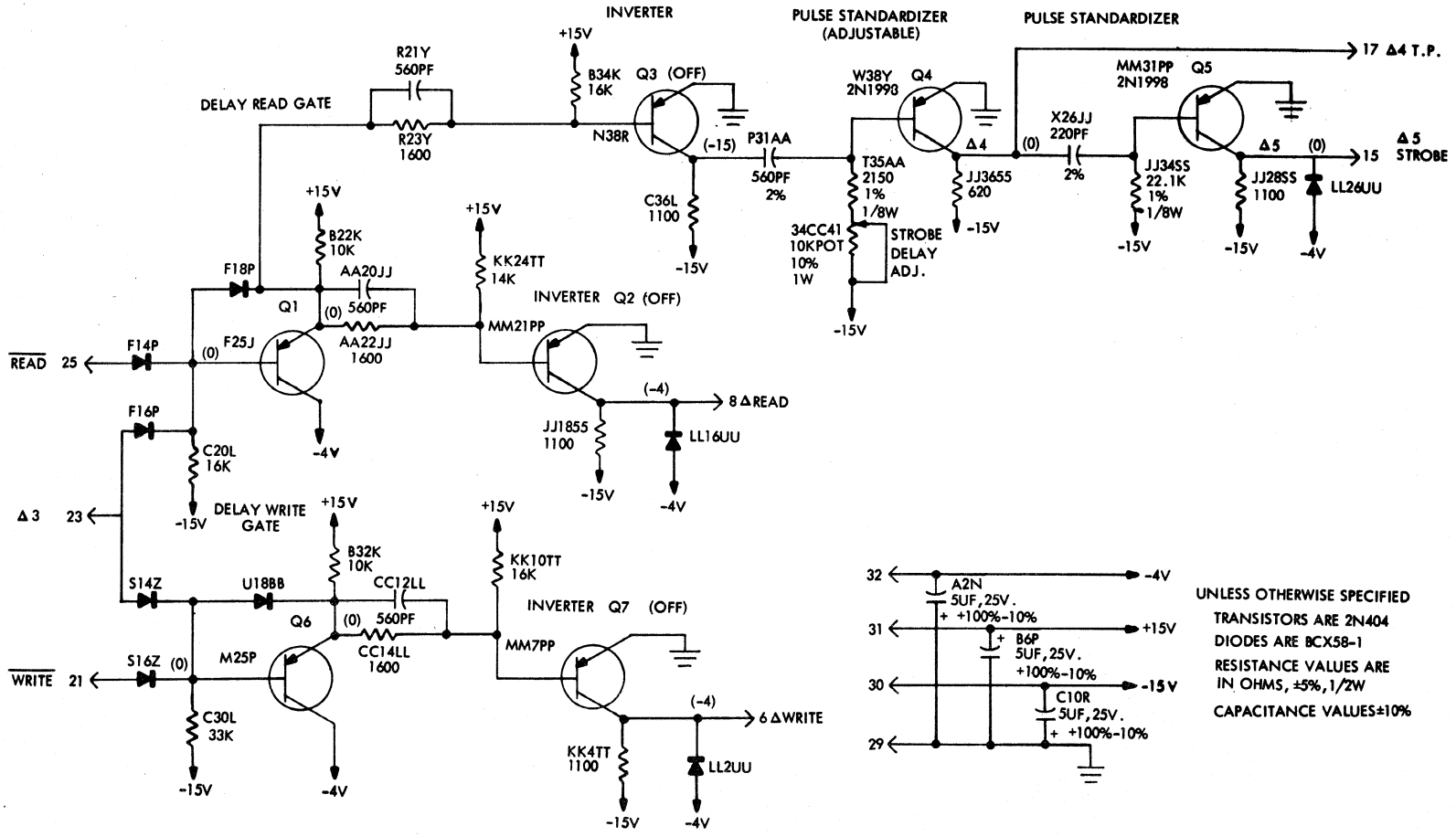


FIGURE IV-40

SPECIAL CONTROL CIRCUITS

MAGNETIC PICKUP PULSE GENERATOR

The function of the Magnetic Pickup and PG Amplifier is to produce an output pulse each time a tooth of the notched rack bar passes over the magnetic pickup head. The pulse must have sufficient amplitude to trigger the pulse generator circuits on the Print Control Card. A block diagram of the Magnetic Pickup and PG Amplifier is shown below:

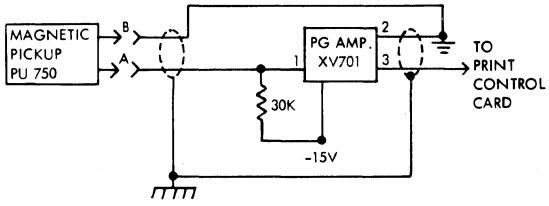


FIGURE IV-41

The Magnetic Pickup is a high voltage unit which produces an output when a tooth of the notched rack bar, moving at a relatively low speed, passes over it. The PG Amplifier is a sealed unit which plugs into a standard octal socket. The 30K resistor is connected externally so that minor adjustments can be made in the voltage reference level for pulses from the magnetic pickup, without changing the design of the sealed amplifier unit.

Magnetic Pickup

The magnetic pickup consists of a cylindrical permanent magnet with a coil of wire wound around a pole piece. In order to save space, the coil is wound on an insulated form which slips over the smaller diameter pole piece attached to the end of the magnet.

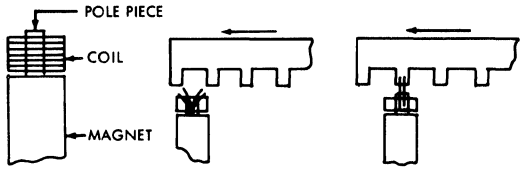


FIGURE IV-42

The magnetic pickup will produce a voltage output when any magnetic material (steel, iron, etc.) moves near the pole piece at the end of the pickup. The magnetic pickup makes use of the stray magnetic field which exists when a tooth on the notched rack bar is not positioned over the pole piece. As a tooth is brought near the head of the pickup, the magnetic lines of force shift and as they cut across the coil wound on the pole piece they generate a voltage in it. Since the pickup does use this stray magnetic field, no provisions for any return magnetic circuits or paths are necessary.

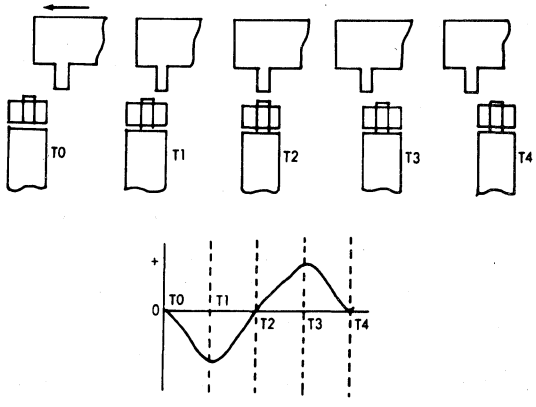


FIGURE IV-43

Exciting the pickup with protruding teeth on a bar keeps the magnetic material between teeth far enough from the head to prevent generating any stray signals or noise. The output voltage

from the pickup depends upon the rate of change of the magnetic field which, in turn, is a function of the speed of the tooth as it passes over the head, the size of the tooth and the spacing of the tooth as it passes over the head. In general, the output voltage varies directly with the speed and size of the tooth and inversely with the distance between the tooth and the head. A single tooth entering the magnetic field would generate the approximate voltage waveform shown above.

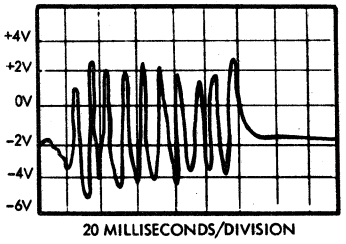


FIGURE IV-44

Due to the spacing of the teeth on the rack bar, as one tooth is leaving the field the next tooth is entering. Both are causing flux changes in the pickup coil at the same time but in opposite directions. The tooth leaving is causing a decreasing flux density; the tooth entering, an increasing flux density. The net result is to decrease the overall flux change in the head which reduces, slightly the output voltage. In general, the first positive voltage peak from the pickup is the smallest and the last the largest. The pulses due to teeth 2 thru 9 reach a steady state condition as shown above.

Pulse Generator Amplifier

The first pulse amplifier stage consists of a 2N1998 transistor and its associated circuitry as shown on figure 46. Under static conditions, current flows thru the 15K and 30K resistors in parallel and the magnetic pickup coil establishes a reference level of approximately -1.4 volts at pin 1. The base-emitter junction of the 2N1998 is forward biased, the transistor is conducting thru the 1330 ohm load resistor and its collector is at or near ground level. As a tooth on the notched rack bar moves across the magnetic pickup, the voltage signal described previously is applied to the base of the 2N1998. As the signal goes positive, the 2N1998 transistor is cut off and this triggers the pulse forming network, stages 2 and 3.

The 3600 ohm resistor in the base circuit aids in establishing a threshold level for the stage and prevents any small transient pulses (.2 to .8 volts in amplitude) from triggering the first stage. The first stage will remain cutoff until the input signal goes negative at which time it will again conduct.

Second Stage Amplifier

With the first stage conducting and its collector at ground, the base of the second stage amplifier will be positive due to the 3600 ohm and 47K ohm resistors connected to +15 volts. This reverse biases the second stage and it is cut off. With no significant current thru the 2K ohm load resistor, the voltage at the collector will be -15 volts. When the first stage transistor is switched off by the signal from the magnetic pickup, its collector goes negative and as a result the base of the second stage is forward biased, the transistor conducts and its collector goes from -15 volts to approximately ground. The second stage will conduct until the first stage conducts, at which time the second stage is cut off.

Pulse Standardizer

The pulse standardizer output transistor is normally conducting due to the 6800 ohm and 43K ohm resistors connected to -15 volts and its collector is at approximately ground. When the signal from the magnetic pickup switches off the first stage, the second stage switches on and its collector goes from -15 volts to ground. This positive voltage signal is coupled thru the 4700 PF capacitor to the base circuit of the pulse standardizer transistor and cuts it off. As the third stage cuts off its collector

goes from ground toward -15 volts. The length of time the pulse standardizer is cut off determines the duration of the negative output pulse from the P.G. amplifier. This time is determined primarily by the 4700 PF capacitor discharging thru the 43K resistor in the base of the third stage. The output pulse at pin 3 is shown below:

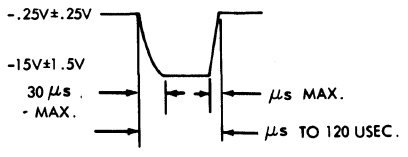


FIGURE IV-45

Once the 4700 P.F. capacitor has discharged to the point where the base-emitter of the pulse standardizer is again forward biased, the 2N404 will turn on and terminate the output pulse. This time may vary from 80μs to 120 μs.

An output pulse is generated each time a tooth of the notched rack bar passes over the magnetic pickup and triggers the first stage. No output pulse is produced when the first stage switches back on since this cuts off the second stage and its collector goes from ground to -15 volts, however, the negative voltage signal coupled to the pulse standardizer base circuit does not alter its conducting state.

MAG. PICK UP PULSE GENERATOR

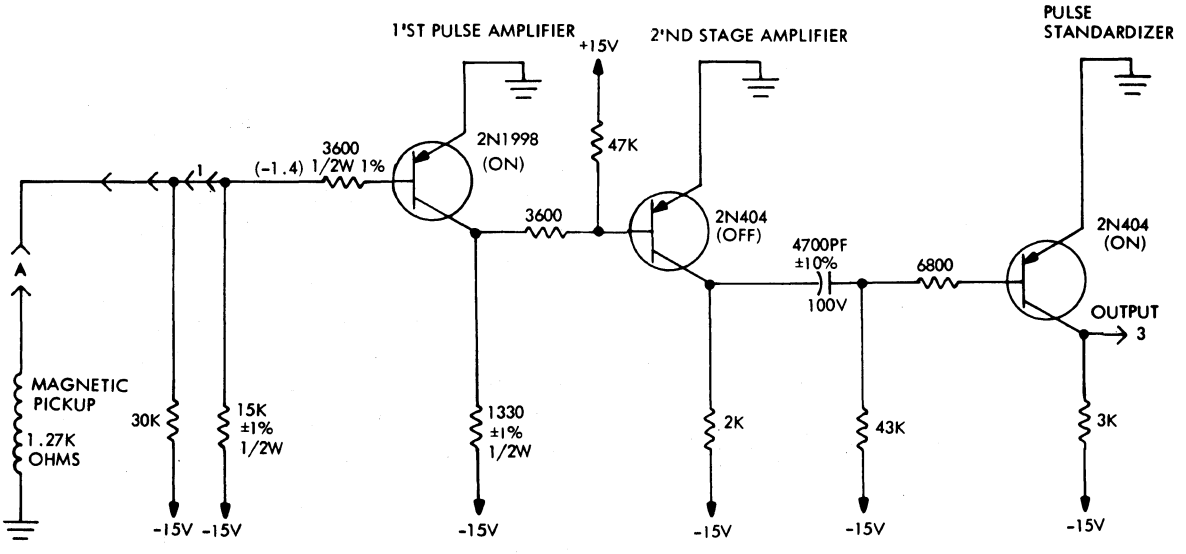


FIGURE IV-46

PRINT CONTROL

The function of the Print Control (PC) card is to convert input signals from the Amount Protection (AP) cam circuit and the Magnetic Pickup amplifier into output signals of the correct polarity, amplitude and duration to synchronize the input signals with standard Clock timing in the Electronic section.

A block diagram of PC card is shown below:

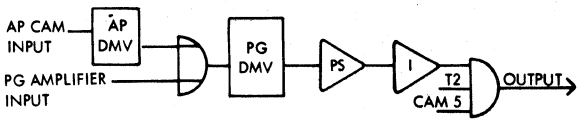


FIGURE IV-47

The AP Delay Multivibrator (DMV) provides a 9-12 millisecond guard period between the AP cam pulse and the first Pulse Generator (PG) pulse. The PG-DMV provides a 5-7 millisecond guard period between pulses from the PG Magnetic Pickup Amplifier. The PG-DMV also triggers a Pulse Standardizer (PS) whose output after inversion, becomes the PC card output signal under control of timing cam 5.

Amount Protection CAM Circuit

When the keyboard printer is in home position, the AP cam switch is closed and a ground signal thru a relay voltage wetter circuit appears at the AP cam Input to the P.C. card (pin 25):

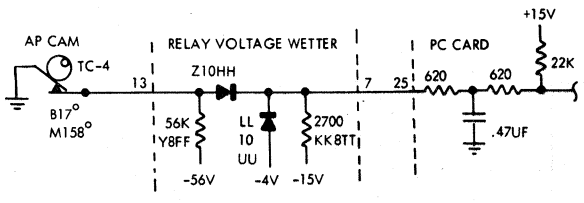


FIGURE IV-48

With reference to the P.C. schematic, figure 52, transistors M6P, EE11HH and associated parts make up the AP-DMV. Under static conditions, transistor EE11HH is conducting since its base-emitter junction is forward biased by the 75K ohm resistor connected to -15 volts. The collector of EE11HH is at ground or is slightly negative. Transistor M6P is off since its base-emitter junction is reverse biased due to current flow from the AP cam circuit thru the voltage divider resistors F1P, F3P and BSK to +15 volts. Resistors F1P and F3P also serve as a noise filter circuit, together with noise bypass capacitor S2JJ. With the 2N404 M6P biased off, its collector is near -15 volts.

At approximately 17 degrees of the keyboard-printer cycle, the AP cam switch opens and, due to the wetter circuit, the AP input goes to -4 volts (diode Z10HH of the wetter circuit disconnects since the plate is negative with respect to the cathode, and current flow from -15 volts thru resistor KK8TT and diode LL10UU brings the output to -4 volts). At this time, transistor M6P is switched on, base-emitter forward biased, and its collector goes from -15 volts to ground. This positive voltage swing developed across collector load resistor C8L is coupled thru capacitors P10CC and JJ6UU to reverse bias the 2N1998 transistor EE11HH and cut it off. The 2N1998 is used because of its fast switching characteristic. As EE11HH stops conducting, its collector goes from ground to approximately -12 volts established by current flow from -15 volts thru collector load resistor LL3UU resistors T15AA and B12K to +15 volts.

Transistor E11HH will remain off from 9 to 12 ms as capacitors P10CC and JJ6UU are discharged by current flow from -15 volts thru the 75K base bias resistor. During this time, the negative signal from the collector of EE11HH is coupled thru feedback resistor T13AA to forward bias M6P and keeps it conducting in case the AP cam bounces momentarily. This prevents the AP cam switch from generating more than one output pulse for a single machine cycle.

Transistor M6P conducts during the entire time the AP cam switch is open (17° to 158°, 141MS). Transistor EE11HH will remain cut off until P10CC and JJ6UU discharge to the point where its base-emitter is forward biased at which time it will again conduct. The approximate waveform at the collector of EE11HH is shown on Figure 51 in relation to the AP cam.

The signal at the collector of EE11HH is applied thru one of three 5100 ohm resistors (T15AA) to the Pulse Generator (PG) DMV. The three 5100 ohm resistors T15AA, H17R and T17AA) together with the 30K source resistor form a resistor OR gate to control transistor M14P.

All three resistor inputs are normally at ground level from conducting pulse standardizer stages and, together with the 30K resistor to +15 volts, the M14P transistor is reverse biased. When the AP-DMV is triggered and EE11HH is cut off, the AP input to the resistor OR goes to -12 volts which forward biases M14P and triggers the PG-DMV.

PG - Delay MV

The operation of the PG-DMV is similar to that of the AP-DMV. Transistor EE18HH is normally conducting, transistor M14P normally off. A signal going from 0 volts to -10 or -12 volts from the AP-DMV or the PG input will trigger the PG-DMV and turn M14P on. The positive going signal from the collector of M14P is coupled thru S22EE to cut off EE18HH. Resistor C19L is the collector load for M14P.

The period of the PG-DMV (EE18HH OFF) is 5 to 7 ms and is determined primarily by the RC discharge time of capacitor S22EE and resistor JJ15UU. The approximate waveform at the collector of EE18AH is shown on Figure 51 in relation to the AP cam and AP-DMV. The resistor T17AA is again an OR input to hold M14P conducting while EE18HH is off. In this way, once the PG-DMV is triggered and produces an output pulse, it cannot be triggered again until the end of the DMV period. Both the AP-DMV and the PG-DMV are safeguard circuits to insure only one pulse out of the PC card due to the AP cam switch and one pulse for each tooth of the Magnetic Pickup rack bar.

Print Control Gate Circuit

Since the output of the PC card is gated with TC5, the input must also be gated with TC5. TC5 prevents an output pulse from the PC card before 010° and after 167° of the cycle by the gate made up of diodes T39AA, CC39LL and resistor LL34UU. The Relay wetter for TC5 is wired to pin 13 of the PC card. TC5 also prevents the AP-DMV and PG-DMV being triggered by a noise pulse prior to 010°. If these circuits could be triggered by noise, the possibility exists that the AP pulse could be lost due to the timing condition of the DMV's and TC5. Assume for a moment that a noise pulse appeared on pin 25 at 008° of the cycle. This noise pulse would trigger the guard AP-DMV and would also cause an output pulse from transistor M35P, however, since TC5 is still low, no pulse would appear at pin 9. The signal from TC4 (the AP signal) cannot produce a pulse at 010° because the AP-DMV is still on from the noise pulse at 008°. The total number of pulses at pin 9 would be short by one and a misprint would result. To make the circuit impervious to noise prior to 010°; a transistor driver and gate circuit is used to disable the DMV circuits by holding the second stages off (a ground is provided for the collector), and providing a ground for the PG input. Before 010° the RW for TC5 provides -4V at pin 13. At this time the base of transistor EE28HH is negative and the transistor is on. This provides a forward bias for diodes S19Z, LL1UU and KK12TT keeping transistors M14P, EE11HH and EE18HH off and therefore prevents a trigger of the DMV circuits by noise. When TC5 makes at 010°, a ground is provided which will cause the base of transistor EE28HH to become positive and will turn the transistor off. When EE28HH is off; diodes S192, LL1UU and KK12TT will be reverse biased and will allow the AP and PG pulses to trigger the DMV's and produce an output pulse.

If a noise pulse should trigger the circuit from pin 18 or 25 after TC5 is made at 010°; a pulse will be produced and gated out at pin 9. The DMV which is on, will then block the normal pulse on pin 18 or 25 and thereby maintain the proper number of pulses from the PC circuit.

The PG circuit will produce pulses as the racks are restored to home position, however, TC5 will break at 167° of the cycle and transistor EE28HH blocks both the input and output of the PC card. This prevents pulses at pin 9 during the return of the racks.

Pulse Standardizer

Transistor M14P, part of the PG-DMV, is normally off and its collector is at -12 to -15 volts due to resistor C19L and the -15 volts supply. As the PG-DMV is triggered M14P conducts and its collector goes to ground. This positive going signal is coupled thru capacitor S32DD to trigger the pulse standardizer M28P. Under static conditions, the base-emitter of M28P is forward biased due to the 2K resistor T37AA and 47.5K resistor KK32TT connected to -15 volts. The 2N404 pulse standardizer is conducting and its collector is at ground. When the positive signal from M14P is coupled thru S32DD, the transistor is cut off and its collector goes to -4 or -5 volts due to the voltage divider from -15 volts, resistor C21L, resistor E25P and resistor B31K to +15 volts. The pulse standardizer will remain cut off for 12 to 22 μs determined primarily by the RC discharge time of S32DD thru KK32TT.

After S32DD discharges to the point where the base-emitter of M28P is again forward-biased, the transistor will conduct and its collector will return to approximately ground. The 2K resistor T37AA establishes a threshold level for the 2N404 Pulse Standardizer base-emitter circuit and prevents any small positive voltage fluxuations from momentarily cutting off the Pulse Standardizer. The signal at the collector of the Pulse Standardizer, after inversion, becomes the PC card output signal, any momentary cutoff of the P.S. would produce an erroneous PC output.

Inverter

The last stage of the PC card inverts the signal from the collector of M28P and produces the PC output signal. When the Pulse Standardizer is conducting (at normal) the inverter transistor's base-emitter is reverse biased due to the voltage divider from the collector of M28P, resistor F25P and resistor B31K to +15 volts. The 2N404 M35P is off and its collector is at -4 volts due to current flow from -15 volts thru resistor D38M and clamp diode A34J to -4 volts. When the pulse standardizer is cut off for 12-20 μs, its collector goes negative and the base-emitter of the Inverter is forward biased. The Inverter 2N404 conducts and its collector goes to ground. The signal at the collector of the Inverter is applied to diode T39AA which is one input to a two input AND gate. The other input to the AND gate is thru diode C37LL. If the second input to the AND gate is high as it will be after 010 , the output pulse at pin 9 of the PC card will be shown on Figure 51.

The output at pin 9 will remain at ground as long as the PS is cut off. After approximately 12 to 22μs the PS will again conduct and its collector will return to ground. The Inverter base-emitter will again be reverse biased and it will stop conducting. The 560 PF capacitor is used to speed up the turn off of the inverter stage. The output at pin 9 returns to -4 volts after the Inverter is cut off.

The net result of AP cam opening at 017 is to produce a 12 to 22μs pulse at pin 9 of the PC card. The delay between the cam opening and the output pulse is very small (less that 1μs).

Magnetic Pickup Input (Pin 18)

The output from the Magnetic Pickup pulse generator is a series of pulses which go from ground to -10 or -12 volts and have a duration of 80 to 120μs. It is these pulses that are applied at pin 18 of the PC card and from there to the base of the PG-DMV thru the H17R input of the resistor OR gate. This input, like the AP input, triggers the PG-DMV which, in turn, triggers the pulse standardizer and after inversion produces the output pulse at pin 9 of the PC card.

Print Control Synchronization

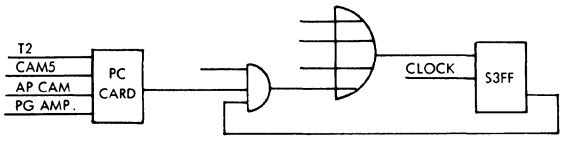


FIGURE IV-49

The PC card converts non-synchronous signals from the AP cam and Magnetic Pickup to a 12 to 22 μs. signal which, when gated with clock, will set the sequence 3 FF. The length of the PC output pulse insures that at least one full clock pulse will be gated to set sequence 3. If the PC output pulse occurs at a time that splits a clock pulse and the split pulse still sets the FF, then the next full clock will be blocked by S3 Reset output going low. If the split pulse does not set the FF, the next full clock pulse will. If the PC output is 17 or 18 μs and gates two full clock pulses to set S3, the first will set the FF, the second will be gated out by S3 Reset. The length of the PC output is such that it will set the S3FF once for each PC output pulse.

Approximate Timing:

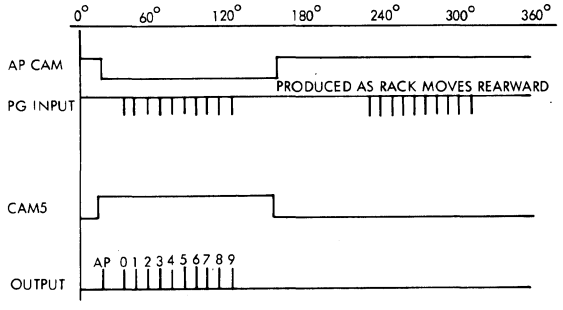


FIGURE IV-50

The above waveforms show the approximate timing for the signals in and out of the PC card. Although PG input pulses are applied to the PC card as the notched rack bar returns rearward, the TC5 signal at the output and gate will be low and there will be no output from the PC card.

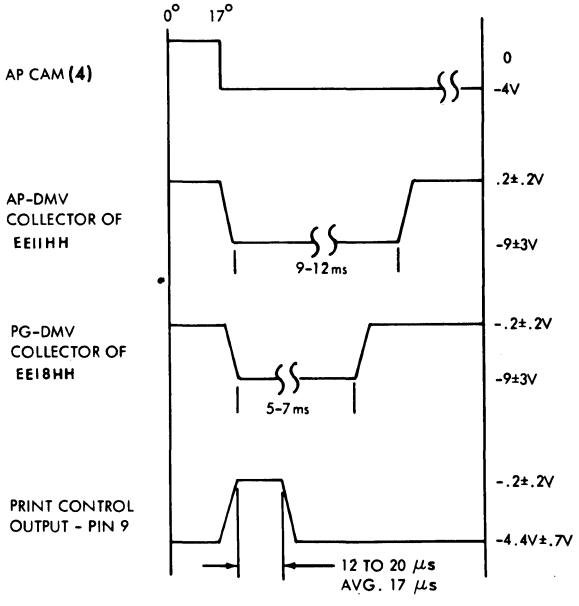


FIGURE IV-51

PRINT CONTROL

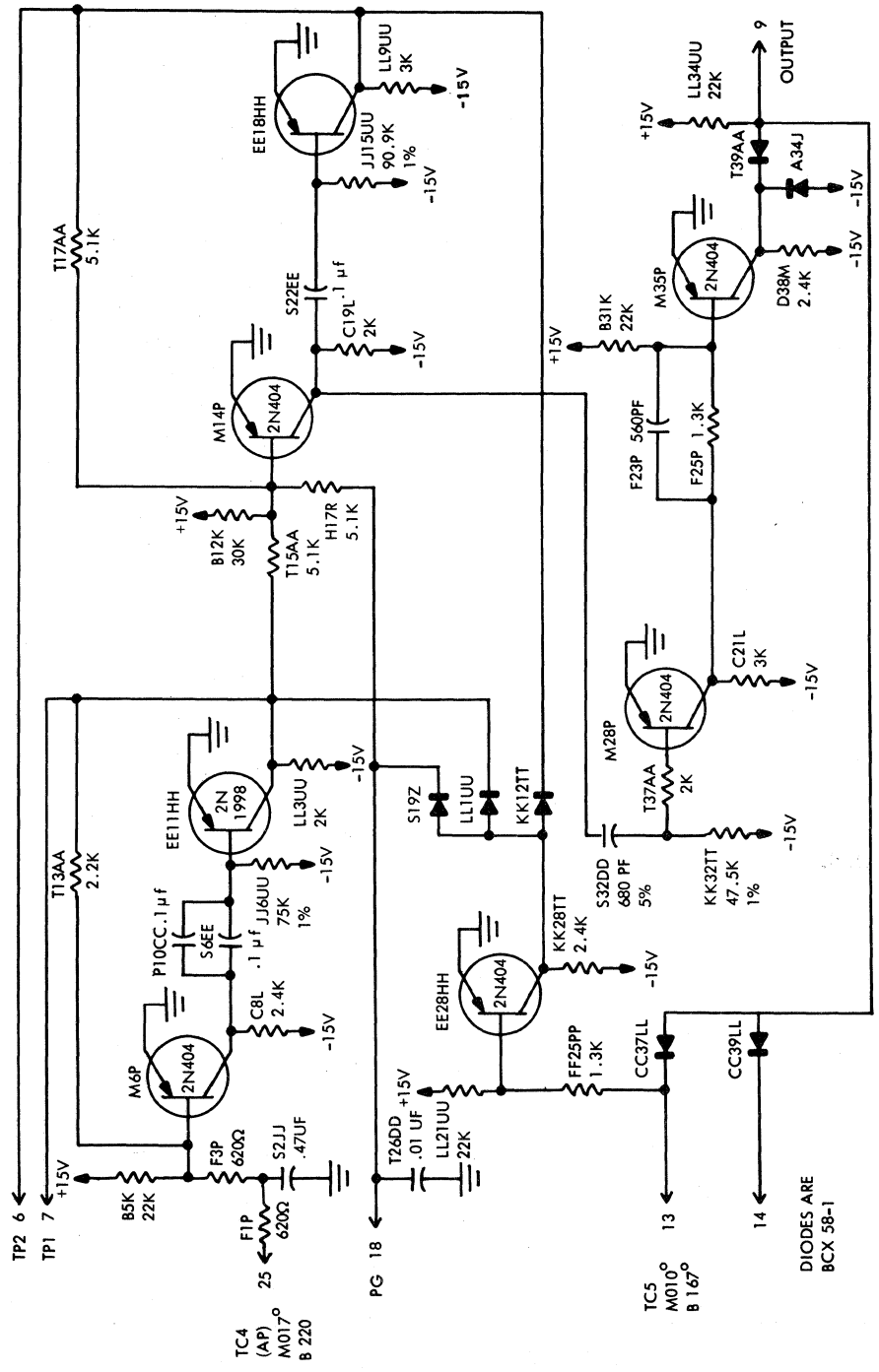


FIGURE IV-52

RACK STOP DRIVER

The Rack Stop Driver is a circuit that is used to obtain fast drop out of a solenoid. The circuit is driven from the reset output of a flip-flop. Its output is a positive voltage spike which acts to reverse the current in the solenoid. The current reversal allows the release of a rack stop solenoid clapper in approximately 2.5 ms. There are five identical Rack Stop Driver circuits on each Rack Stop card:

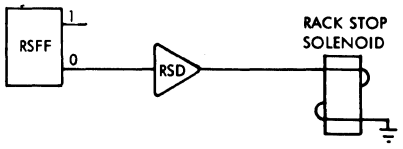


FIGURE IV-53

The block diagrams above show the connection from one Rack Stop flip-flop's reset output to the Rack Stop Driver and from the Driver to one RS solenoid.

The Rack Stop Driver (RSD) transistor is a 2N398A type PNP Germanium, which has a maximum collector to base and collector to emitter voltage rating of 105 volts. It is connected in a normally off inverter circuit which is controlled by a flip-flop. The RS flip-flop is set by the logic when a clapper is to be released. The RSD is connected to the reset output of the RS flip-flop since the reset output is at ground when the flip-flop is reset and the ground signal holds the RSD off.

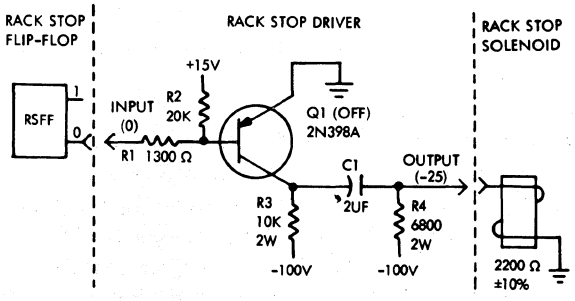


FIGURE IV-54

With a ground level at the input, the RSD is biased off by the current flow from ground thru R1 and R2 to +15 volts. The base of Q1 will be positive with respect to the emitter and this reverse bias condition keeps the RSD off. The collector will be at approximately -100 volts since there is essentially no current flow thru collector load R3.

A path for hold current (11 MA) thru the R.S. solenoid is provided from -100 volts thru R4 and the solenoid to ground. The voltage at the R.S. driver output is about -25V under these static conditions. With the voltage on the transistor side of C1 at -100 volts and the voltage on the solenoid side of C1 at -25 volts, the capacitor is charged to about 75 volts.

When the RSFF is set by the logic, its reset output goes to -4 volts. Transistor Q1 switches on and its base goes to -.2 or -.3 volts (clamped to nearly ground by the base-emitter junction). As the collector of Q1 goes from -100 volts to ground, the 100 volt positive signal is coupled thru C1 to reverse the current thru the solenoid. The current thru the solenoid will decrease from 11 MA to zero in about 1 millisecond as C1 discharges from +75 volts towards -25 volts. At 2.5 ms, or before, the clapper will release as shown below. After C1 is discharged, the current thru the solenoid will again build up in its original direction.

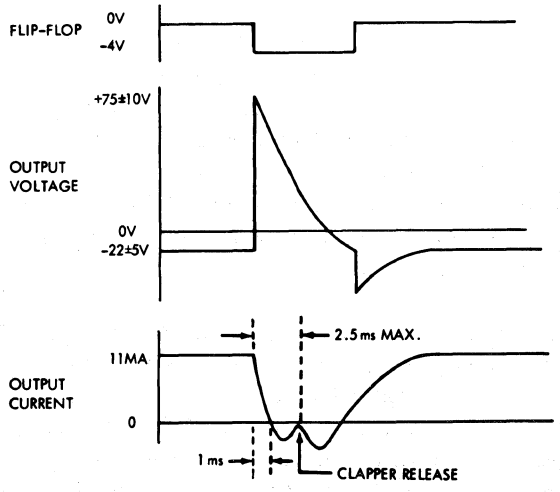


FIGURE IV-55

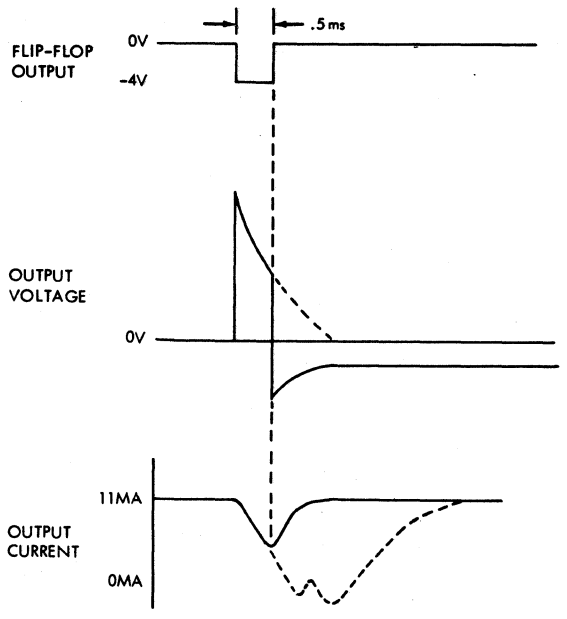


FIGURE IV-56

When a RSFF is set and the reset output goes to -4 volts, it must remain set for 2.5 ms to reliably release the solenoid clapper. If the FF is set and then reset within .5 ms, the clapper will not release. The waveforms above show the current decrease and recovery in the solenoid where the FF has been reset after .5 ms. The Amount Protection feature is possible because a .5 ms signal will not release the RS clapper.

When capacitor C1 is charged before the RSFF is set, the transistor side is (-) and the output side (+). After the RSFF is set and the clapper releases, the output will return to -25 volts while the transistor is still on. At this time, the transistor side of the capacitor is (+) and the output side (-). For these reasons a non-polarized 2 μf capacitor is used for C1.

The RSFF's are reset when the start relay drops late in the machine cycle. The reset output returns to ground and again reverse biases Q1. The voltage at the collector of Q1 starts toward -100 volts as C1 recharges and reaches -100V in about 20 ms. The negative voltage swing is coupled thru C1 to the RS driver output, however, the negative signal only momentarily affects the hold current and the RSD output returns to its static level of -25 volts.

MISCELLANEOUS CIRCUITS

Indicator

An Indicator circuit consisting of a transistor driver stage connected to a neon indicator lamp is provided to aid in trouble-shooting. Eight identical indicator circuits, including their respective indicator lamps, have been provided on each Indicator printed circuit card. One circuit and lamp is shown below:

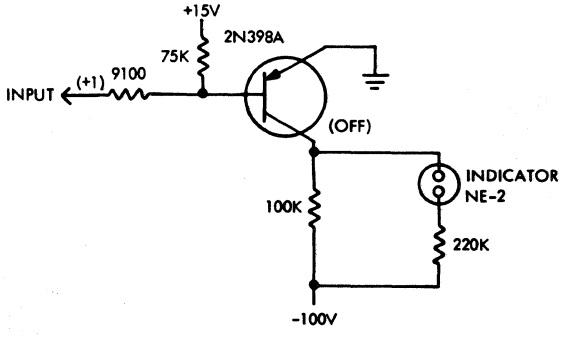


FIGURE IV-57

When the Input is high (+1.0 volts to -.2 volts) the 2N398A will be off due to its base-emitter being reverse biased by the 9100 ohm and 75K ohm resistors connected to +15 volts. The voltage at the collector will be near -100 volts and with no difference of potential across the neon lamp it will not be on. Thus, with a high input, the lamp is off.

When the Input is low (-4 volts to -5 volts) the transistor will be on due to its base-emitter being forward biased by the negative input signal in conjunction with the voltage divider to +15 volts. The collector will be at approximately ground and with 100 volts across the NE-2 and 220K ohm resistor, the lamp will be on. The

220K ohm resistor prevents excessive current flow through the NE-2.

The Indicator circuit is designed to take very little current from the circuit to which it is connected (.52ma maximum at -4.0 volts). For this reason, the input voltage requirements are strict and the indicator should be connected to Flip-Flop or Inverter outputs only for accurate operation.

Solenoid Driver

The Solenoid Driver is designed to drive or energize a solenoid which requires up to 125ma of current. There are three independent SD circuits on each Solenoid Driver Card. A block diagram of the Red Ribbon Solenoid and SD is shown below:

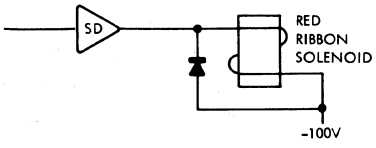


FIGURE IV-58

The SD may be controlled by a flip-flop or other logic circuits. It is turned on by a high input signal and off by a low input signal.

The input circuit, reference figure 59, involving the 2N404 transistor Q1 is an Inverter which also serves as a current driver for the 2N398A transistor Q2. When the input is low, the transistor Q1 will be forward biased due to resistors R1 and R2 connected to +15 volts. With Q1 conducting its collector will be at approximately ground. Resistors R3, R4 and R5 form a voltage divider between -15 volts and +15 volts to control the operation of transistor Q2. With the collector of Q1 at ground, the base of Q2 will be positive with respect to its emitter and Q2 will be off. Thus, with a low input signal, the solenoid is not energized.

When the input signal is high, the base of Q1 will be positive with respect to its emitter and Q1 will be cut off. With Q1 cut off, its collector will no longer be clamped at ground and will go negative as will the voltage at the base of Q2. With the base-emitter of Q2 forward biased Q2 will conduct (approximately 125ma) and energize the solenoid. The 2N398A transistor was selected since it will conduct up to 200ma and will withstand 105 volts between its collector-base and collector-emitter junctions.

The 220 ohm resistor R6 and .1 uf capacitor C1 provide some damping for the voltage spike which results when the current thru the solenoid is interrupted; however, the primary purpose of R6 and C1 is to decrease the rise time of the output pulse in order to prevent any noise pickup in the system. Fast switching of a high current in a wire might induce a voltage in an adjacent wire and C1 and R6 prevent this. The suppression of voltage spikes which result when a high inductance coil is de-energized must be provided external to the Solenoid Driver card.

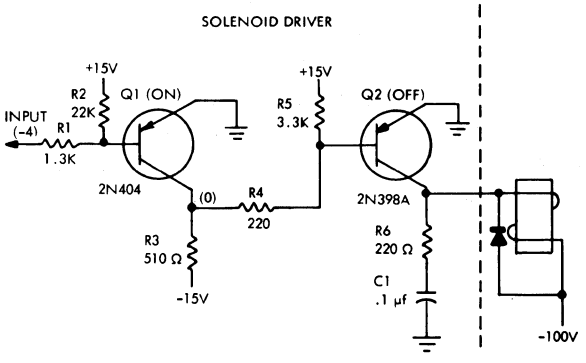


FIGURE IV-59

VOLTAGE WETTING CIRCUITS

Special Wetter and Relay Voltage Wetter

The relay voltage wetter card contains thirteen identical wetting circuits. They are used to insure a low resistance connection between relay contacts. The special wetter also contains nine of these same circuits in addition to nine special circuits that are used as part of the keyboard wetting.

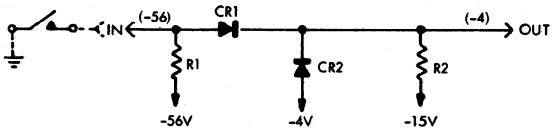


FIGURE IV-60

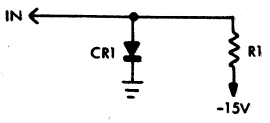


FIGURE IV-61

The relay wetter is shown in figure 60. Under static open input conditions, the input is at -56 volts due to the voltage applied through the resistor RI. The output is clamped at -4 volts by diode CR2. Current flows from -15 volts, through resistor R2 and clamp diode CR2 to -4 volts. Diode CR1 is back biased and not conducting due to its plate being more negative than its cathode. One side of the contacts in the input circuit is at ground level, therefore, the wetting voltage across the contacts is 56 volts. When the contacts are closed, the wetting voltage breaks down any resistive film that may be on the contacts, allowing a low resistance circuit. This low resistance contact causes the voltage at the input to be at ground level and the 56 volts to appear across resistor R1. The plate of diode CR1 is now at ground level, which forward biases it and causes current flow from -15 volts through resistor R2, diode CR1, to the contacts in the input circuit and to ground. Due to the low voltage drop in the diode CR1 when it is forward biased, the output of the wetter will be at approximately ground level or near the input voltage.

The special wetter card also contains nine special clamp circuits which assist in the contact wetting and help shape the trailing edge of the DD signal through the keyboard. A typical circuit is shown in figure 61. The static voltage on the special wetter input is -15 volts, applied through the resistor R1. When the input comes high it is upper clamped to ground by the CR1 diode. Due to the capacity of the long input lines from the keyboard to the Arithmetic and Memory unit, the resistor, R1 was made a low resistance. This forces the voltage on the input lines down faster and improves the shape of the trailing edge of the DDFF pulse. The use of this special camp circuit is shown further in figure 63.

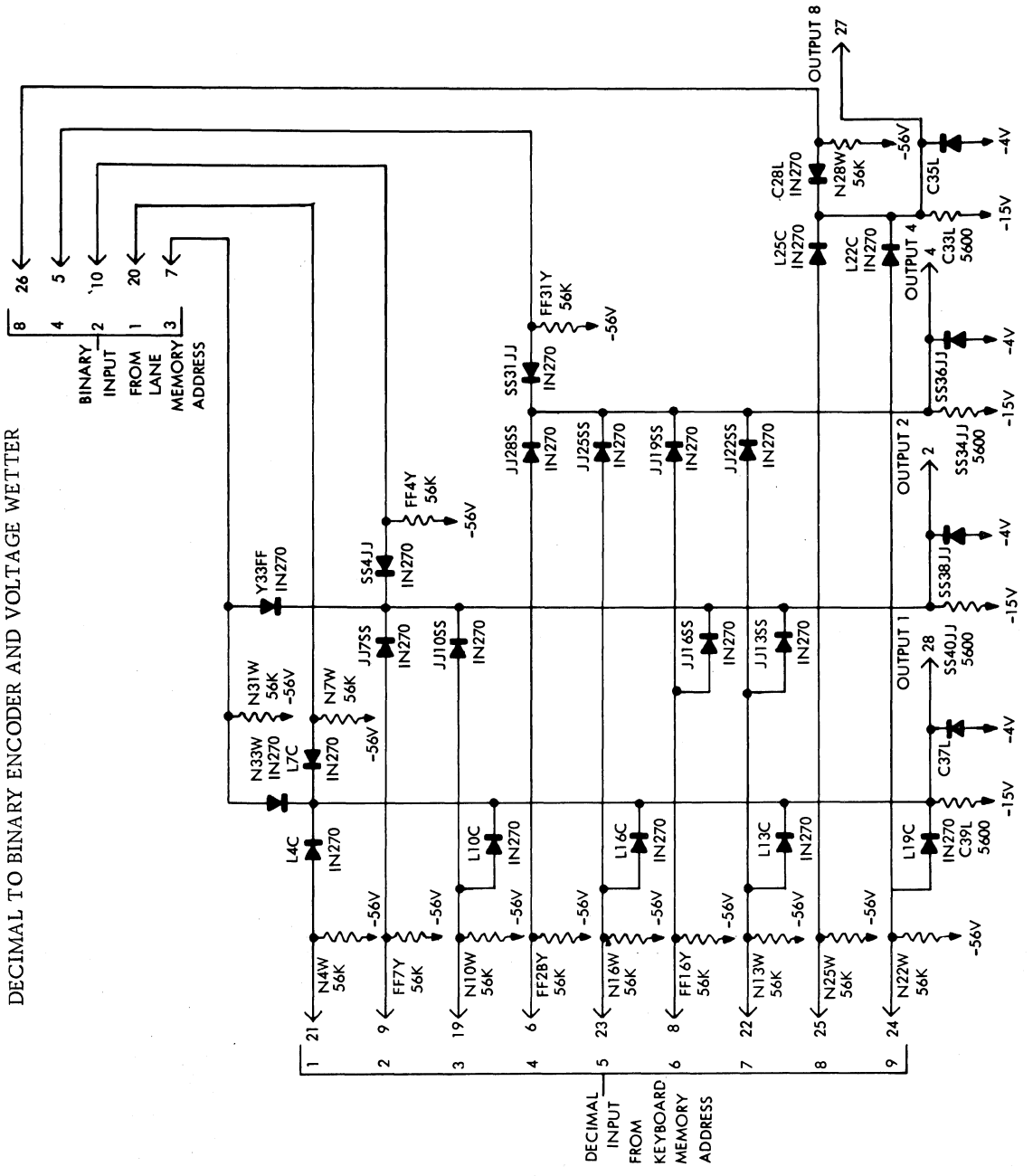

DECIMAL TO BINARY ENCODER AND VOLTAGE WETTER
BINARY INPUT FROM LANE MEMORY ADDRESS
DECIMAL INPUT FROM KEYBOARD MEMORY ADDRESS
OUTPUT 8
OUTPUT 4
OUTPUT 2
OUTPUT 1
-56V
-15V
-4V
IN270

FIGURE IV-62

Decimal to Binary Encoder and Wetter

The wetting for the memory address keys and lane switches is accomplished in the same way as described in the Relay Voltage Wetter. The input to the encoder is made up of signal levels from the keyboard memory selection switches or the lane control memory selection switches. The encoder itself is a combination of voltage wetter cirucits arranged in such a way that a deci mal or binary input results in a binary output. The binary input is from the lane switches and has been modified to include a 3 input. This allows the selection of all digits 0 thru 9 to be represented with two lanes of control. There is one Decimal to Binary Encoder and Wetter located on a card. Two of the encoders are used: one for the units and one for the tens digits for memory selection.

Disconnect Circuit

The Disconnect circuit is used to enable wetting of the keyboard switches prior to flip-flop control of the keyboard digit lines by the Digit Distributor. Figure 63 illustrates the wetting of the keyboard amount switches. In its static state (1), without a keyboard switch closed, the disconnect circuit has +35 volts applied at point C through start contacts and -4 volts at point A by the heavy buffer. The output at point B is +35 volts with diode CR2 forward biased and diode CR1 reverse biased. Th e only current flow is from -4 volts in the heavy buffer, through the back resistance of CR1, R1 and CR2 to +35 volts. The 39 volt drop appears across CR1.

Closing the keyboard switch (state 2) causes current to flow from -15 through R2, R1 and CR2 to +35 volts. The current through R2 causes the voltage drop across it to try to exceed 15 volts but when the voltage at the junction of CR3 and R2 reaches ground level, it is clamped by diode CR3. With the voltage at the junction of CR1 and R1 clamped at ground, the current through R1 causes the remaining 35 volts to appear across it. When the start relay is picked (state 3), the +35 volts is removed from the disconnect card at C13C15 which affects all 12 circuits on the card. Current then flows from -15 volts through R2 and CR1, which is now forward biased, to -4 volts at the heavy buffer. This causes the output at point B of the disconnect to be -4 volts. When the DDFF signal causes the input at point A to go to ground (state 4), the output also goes to ground and the 15 volts appears across R2. When the DDFF signal is terminated, the input returns to -4 volts and the output is also at -4 volts as in state 3.

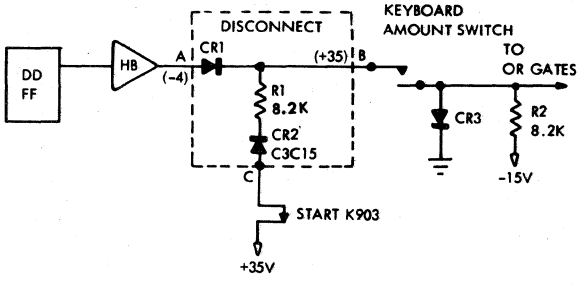


FIGURE IV-63