EK-RK067-UG-001

RK06/RK07
Disk Drive
User's Manual

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CHAPTER 1
INTRODUCTION

1.1 PURPOSE AND SCOPE

This manual provides information related to the capabilities, installation, operation, programming, and user maintenance requirements of the RK611/RK06 and RK611/RK07 Subsystems.

This manual is intended primarily for operating and programming personnel. Installation and service should be performed only by qualified DIGITAL field engineering and maintenance personnel.

The information is arranged as follows:

- Chapter 1 provides a general description of the subsystems, including capabilities, standard and optional features, and specifications.
- Chapter 2 provides separate drive, cartridge, and controller descriptions, concluding with a subsystem overview to familiarize the user with certain hardware and technical characteristics.
- Chapter 3 contains the details to be considered when selecting a location for installation of the subsystems.
- Chapter 4 describes the installation process for the subsystems and the dual port option. (Installation should only be performed by qualified DIGITAL field personnel.)
- Chapter 5 describes the procedures necessary to demonstrate that the drive and controller are suitable for user acceptance.
- Chapter 6 contains step-by-step procedures for the operation and control of the subsystems.
- Chapter 7 provides the programmer with general reference material, subsystem software requirements, and recommendations to facilitate the design of user programs.
- Chapter 8 provides the user with basic maintenance requirements and procedures.
- Chapter 9 contains a description of the subsystem dual port option, including control and operation procedures for systems with this option.

This manual will have a much higher value to the reader if he is already familiar with PDP-11 processors and peripherals.

1.2 GENERAL INFORMATION

The RK611/RK06 Disk Drive subsystem and the RK611/RK07 Disk Drive Subsystem, manufactured by Digital Equipment Corporation, both consist of an RK611 Disk Controller and up to eight RK06 and/or RK07 Disk Drives. Each RK06 or RK07 Disk Drive is a free standing, high performance, moving head device that is connected to the RK611 Controller via a daisy-chain bus arrangement. The RK611 Controller, which is located in associated cabinetry, provides an interface between the subsystem and a PDP-11 system via the Unibus. Both RK06 and RK07 drives can be used in one subsystem.

Dual access operation is a hardware option available to the RK06 and RK07 drives enabling either drive to be accessed through two different controllers. Figure 1-1 shows the system configuration for dual access operation. The eight RK06s or RK07s shown on this figure are daisy chained. The two RK611 Controllers can be attached to two different CPUs.

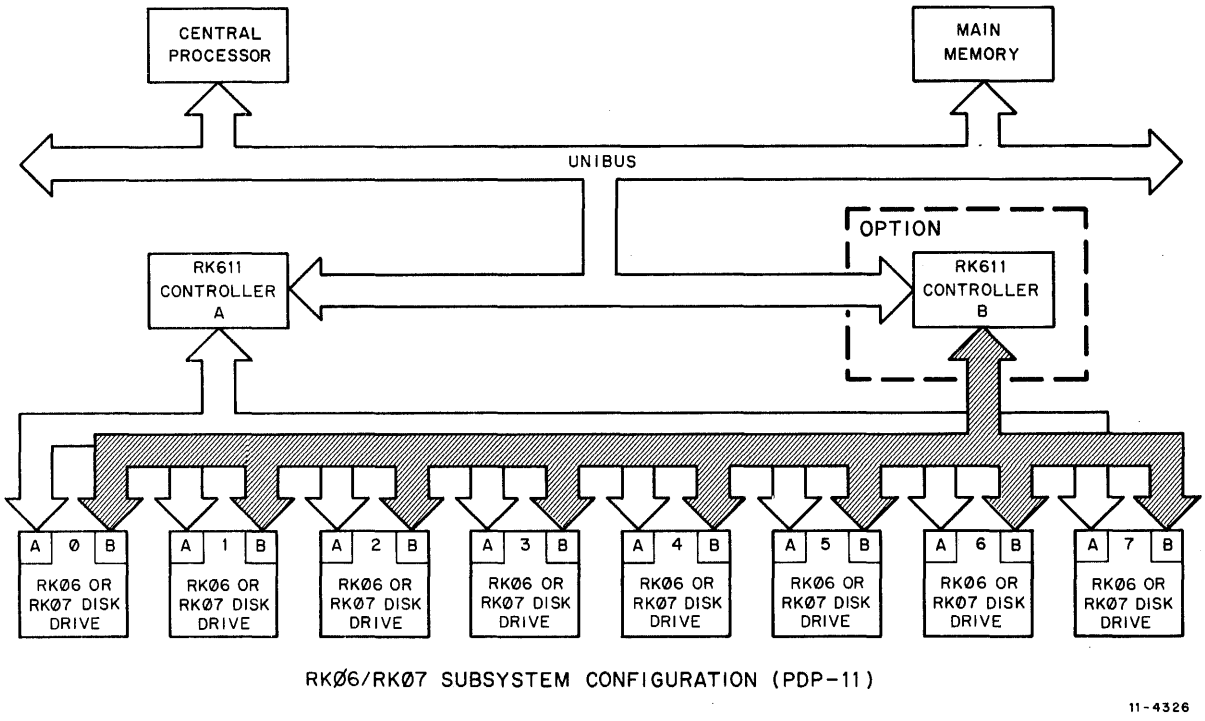


Figure 1-1 RK611/RK06-RK611/RK07 Dual Access System Configuration

1.2.1 Media

The storage medium for the RK06 Disk Drive is a top-loading, dual-platter, RK06K Disk Cartridge, which can be freely interchanged between any of the available RK06 Drives. It has a maximum formatted storage capacity of 6.3 million 18-bit words or 6.9 million 16-bit words. The RK07 Disk Drive uses a similar cartridge, the RK07K Disk Cartridge, as the storage medium. It also can be interchanged between any of the available RK07 Drives. It has a maximum formatted capacity of 12.6 million 18-bit words or 13.8 million 16-bit words. Note that an RK06K cartridge cannot be used on an RK07 Drive, nor an RK07K cartridge on an RK06 Drive.

Each dual-platter pack provides three recording surfaces that are serviced by three read/write heads and a servo surface that is monitored by a single read head. The recording surfaces provide three data tracks per cylinder with a maximum of 411 cylinders per RK06 disk pack or 815 cylinders per RK07 disk pack. Each track can accommodate either 20 (18-bit word) or 22 (16-bit word) sectors, while each sector can accommodate 256 data words. The servo surface provides positioning signals for the heads and timing signals for data transfer synchronization.

The high-density recording capability (required to achieve maximum storage capacities) is provided by the use of the modified frequency modulation (MFM) encoding technique. In addition, each RK06 and RK07 Disk Drive and the controller contain phase-locked oscillator (PLO) circuitry which maintains a constant bit density if a disk is subjected to minor speed variations.

For head positioning, the maximum seek time in the RK06 Disk Drive (411 cylinders) is 75 ms, while the minimum (track-to-track for one cylinder) is 8 ms, with an average access time of 38 ms. The maximum seek time in the RK07 Drive (815 cylinders) is 71 ms, and the minimum seek time is 6.5 ms. The average access time is 36.5 ms.

A data transfer rate of 4.3 μs per 16-bit word between the controller and the Unibus provides an average transfer rate of 232,500 words per second.

1.2.2 Diagnostic and Error Detection/Correction Capabilities

Diagnostic capabilities are enhanced by an extensive status/error reporting network, consisting of nine Unibus-addressable registers which monitor subsystem activities and are visible to the software.

For extended maintenance and serviceability, the RK611/RK06 and RK611/RK07 subsystems provide a software controlled diagnostic mode (DMD) of operation. When diagnostic mode is initiated, the drive interface lines are effectively disconnected from the Controller while the Unibus interface remains intact. With this arrangement, read or write commands can be initiated using simulated data and control techniques, while actual transmissions between the drives and the controller are disabled. In this manner, closed loop data transfers to and from main storage can verify controller operation in relation to data control.

The RK611 Controller provides data error detection and correction logic, which utilizes an error correction code (ECC) technique to detect and identify (for software correction) data error bursts up to 11 bits in length and to detect (but not identify) error bursts longer than 11 bits. In addition and in conjunction with ECC operation, each RK06 or RK07 Disk Drive has a head offset capability which allows the recovery of data from a cartridge that may have been written by a drive with slightly misaligned heads.

The data recovery features, operating in conjunction with the PLO clock system and the MFM recording technique, provide increased reading and recording reliability. However if a disk pack sector proves defective, in that hardware and software attempts to recover its data are unsuccessful, the operating system can mark the sector bad so that future attempts to use it will be prevented.

1.2.3 Maintenance Features

The following standard features enhance the reliability, availability, and serviceability of the RK611/RK06 and RK611/RK07 subsystems.

- The RK06 and RK07 drive interface is designed to allow a specific drive to be electrically isolated from the controller for maintenance purposes. This allows an off-line tester to be utilized without taking a drive off-line or cycling the system down. With this feature, software can reconfigure the system for continued operation while maintenance is performed.

- Service access to an RK06 or RK07 Disk Drive is from the top, front, or rear of the drive and not from the sides. Therefore, maintenance for a given drive in a multidrive system can be initiated without disabling intradrive cabling.

- The logic and power board cages can be extended, following removal of the rear panel of an RK06 or RK07 Disk Drive, to facilitate emergency maintenance.

- Mean-time-to-repair (MTTR) for emergency maintenance is improved by the inclusion of light emitting diodes (LEDs) on the front edge of certain logic boards. The LEDs provide a service engineer with an indication of the functionality of certain key logic areas.

- For the implementation of cartridge alignment procedures, a protection switch is available to the service engineer to provide write protection for the cartridge and control of head velocity to ensure alignment integrity.

- If an RK06 or RK07 Drive loses ac power, neither the drive nor cartridge will be harmed, no data will be lost, and the format will remain intact.

- When dual-access RK06 or RK07 Disk Drives are installed, the logic allows dual-access functionality to be tested utilizing only one of the two available controllers. This feature provides enhanced availability for multiprocessor systems by freeing one controller for normal dual-access operations.

1.2.4 Reference Documentation

These documents supplement the RK06/RK07 User's Manual.

Number	Title
EK-RK067-TD-001	RK06/RK07 Disk Drive Technical Description Manual
EK-RK611-TM-002	RK611 Controller Technical Manual
EK-RK067-SV-001	RK06/RK07 Disk Subsystem Service Manual
EK-RK06-IP-001	RK06 Illustrated Parts Breakdown
EK-RK07-IP-001	RK07 Illustrated Parts Breakdown

1.3 RK611/RK06 AND RK611/RK07 DISK SUBSYSTEM PERFORMANCE SPECIFICATIONS

Tables 1-1, 1-2, and 1-3 are performance specification summaries for the RK611 Controller, the RK06 Disk Drive, and the RK07 Disk Drive, respectively.

1.4 OPTIONS

Table 1-4 lists the several options currently available for the RK611/RK06 Disk Subsystem. As indicated, each drive is contained in an H969 "dedicated" cabinet and contains all the necessary cabling, as well as an RK06K-DC data cartridge. E models are single access and F models are dual access. Similarly, E model RK611 Controllers are single units and F model RK611 Controllers consist of two controllers. The RK611-C is a dual-access controller for the Disk Subsystem and a kit to convert an RK06E to an RK06F.

Table 1-5 lists the several options currently available for the RK611/RK07 Disk Subsystem. As indicated, each drive is contained in an H969 "dedicated" cabinet and contains all the necessary cabling, as well as an RK07-DC data cartridge. E models are single access and F models are dual access. Similarly, E model RK711 Controllers are single units and F model RK711 Controllers consist of two controllers. The RK711-C is a dual-access controller for the Disk subsystem and a kit to convert an RK07E to an RK07F.

Table 1-1 RK611 Controller Performance Specifications

Characteristics	Specifications
Required mounting space	Occupies one double system unit in an expansion box
Power requirements	+5 Vdc ± 5% @ 15 A +15 Vdc ± 5% @ 175 mA -15 Vdc ± 5% @ 400 mA
Number of drives/controllers	8 (max)
No. Unibus-addressable registers	16
Device base address	777440 (octal) switch-selectable
Device interrupt vector	000210 (octal) switch-selectable

NOTE
The RK611 Device base address overlaps the Look-Ahead Register in the RC11 Disk subsystem, and the RK611 Device Interrupt Vector overlaps the same vector in the RC11 subsystem.

Interrupt priority	Level 5 (plug-selectable)	
Small peripheral controller options	Up to three slots, one of which must be quad height. Other two can be quad or hex height.	
Data transfer rates:	22 Sector (16-bit data words)	20 Sector (18-bit data words)
Unibus to Controller (average word rate)	4.3 μs/word	4.6 μs/word
Drive to Controller (burst rate)	3.7 μs/word	4.2 μs/word
Time to update drive status	15 μs (maximum)	
Time to update drive attention	7.4 μs	
Error detection/correction	32-bit ECC word/sector (detection) 11-bit ECC word/sector (correction)	
Time for correction	Less than one revolution	
Maintainability	Diagnostic mode places all controller timing and data paths under software control.	
Number of sectors/track	Software-programmable for 20 or 22 sector format.	

Table 1-2 RK06 Disk Drive Performance Specifications

Characteristics	Specifications	
Storage type		
Medium	Dual-platter magnetic cartridge, DEC RK06K-DC	
Disk diameter	355 mm (14 in.) nominal	
Magnetic heads	3 read/write; 1 servo	
Recording capacity (formatted)	18-bit Word	16-bit word
Cylinders/cartridge	411	411
Tracks/cylinder	3	3
Tracks/cartridge	1233	1233
Sectors/track	20	22
Words/sector	256	256
Bits/word	18	16
Bits/sector	4608	4096
Bits/track	92,160	90,112
Bits/surface	37.88 M	37.04 M
Bits/pack	113.63 M	111.11 M
Bits/inch (inner track)	4040	4040
Tracks/inch	192.3	192.3
Electrical		
Voltage	See model designations in Section 1.5.	
Input Power		
Single access drives	500 W maximum at 60 Hz 450 W nominal at 60 Hz 550 W maximum at 50 Hz 500 W nominal at 50 Hz	
Dual access drives	550 W maximum at 60 Hz 500 W nominal at 60 Hz 600 W maximum at 50 Hz 550 W nominal at 50 Hz	
Start current		
Single access drives	10.5 A rms at 115 V/60 Hz 5.3 A rms at 230 V/60 Hz 11.0 A rms at 115 V/50 Hz 5.5 A rms at 230 V/50 Hz	
Dual access drives	11.3 A rms at 115 V/60 Hz 6.1 A rms at 230 V/60 Hz 11.8 A rms at 115 V/50 Hz 6.3 A rms at 230 V/50 Hz	
Power factor	0.80 minimum	

Table 1-2 RK06 Disk Drive Performance Specifications (Cont)

Characteristics	Specifications
AC-low detection	Less than 90 V (rms) for one cycle or more
Power cord	
Length	2.7 m (9 ft)
Plug type	NEMA 5-15P for 120 Vac (nominal) models NEMA 6-15P for 240 Vac (nominal) models
Operating environment	
Ambient temperature	10° C to 40° C (50° F to 104° F)
Maximum temperature rate of change	20° C/hour (36° F/hour)
Relative humidity	10% to 90% for a maximum wet bulb temperature of 28° C (82° F)
Maximum altitude	2440 m (8000 ft)
Bit transfer rate (unbuffered nominal)	4.30 M/s
Bit cell width	232.5 ns
Latency	
Rotational frequency	2400 rpm ± 2.5%
Average	12.5 ms (1/2 rotation) ±2.5%
Maximum	25.0 ms
Seek Times	
Average	38 ms
Maximum	75 ms
Start/Stop times	60 seconds maximum, 30 seconds nominal
Model Designations	
RK06-EA	90–128 Vac @ 60 ± 0.5 Hz
RK06-EB	180–264 Vac @ 60 ± 0.5 Hz
RK06-EC	90–128 Vac @ 50 ± 0.5 Hz
RK06-ED	180–264 Vac @ 50 ± 0.5 Hz

NOTE

Models RK06-FA through FD are the dual-access models corresponding to models EA through ED respectively.

Table 1-2 RK06 Disk Drive Performance Specifications (Cont)

Characteristics	Specifications
RK06K-DC Cartridge	
Temperature stabilization time	If the cartridge and drive are at approximately the same temperature, 30 min.; if there is some difference, up to two hours, depending on the difference.
Operating temperature range	16° C to 49° C (60° F to 120° F)
Allowable relative humidity (for operation)	8% to 90% for a maximum wet bulb reading of 28° C (82° F)
Storage temperature range (for recorded disks)	-40° C to 65° C (-40° F to 150° F)
Allowable relative humidity (for storage)	8% to 80% for a maximum wet bulb reading of 28° C (82° F)

Table 1-3 RK07 Disk Drive Performance Specifications

Characteristics	Specifications	
Storage Type		
Medium	Dual-platter magnetic cartridge, DEC RK07K-DC	
Disk diameter	355 mm (14 in.) nominal	
Magnetic heads	3 read/write, 1 servo	
Recording capacity (formatted)	18-bit word	16-bit word
Cylinders/cartridge	815	815
Tracks/cylinder	3	3
Tracks/cartridge	2445	2445
Sectors/track	20	22
Words/sector	256	256
Bits/word	18	16
Bits/sector	4608	4096
Bits/surface	73.43 M	75.11 M
Bits/pack	220.32 M	225.33 M
Bits/inch (inner track)	4040	4040
Tracks/inch	384.6	384.6
Electrical		
Voltage	See model designations in Section 1.5.	
Input power		
Single access drives	500 W maximum at 60 Hz 450 W nominal at 60 Hz 550 W maximum at 50 Hz 500 W nominal at 50 Hz	

Table 1-3 RK07 Disk Drive Performance Specificatons (Cont)

Characteristics	Specifications
Dual access drives	550 W maximum at 60 Hz 500 W nominal at 60 Hz 600 W maximum at 50 Hz 550 W nominal at 50 Hz
Start current	
Single access drives	10.5 A rms at 115 V/60 Hz 5.3 A rms at 230 V/60 Hz 11.0 A rms at 115 V/ 50 Hz 5.5 A rms at 230 V/50 Hz
Dual access drives	11.3 A rms at 115 V/60 Hz 6.1 A rms at 230 V/60 Hz 11.8 A rms at 115 V/50 Hz 6.3 A rms at 230 V/50 Hz
Power factor	0.80 minimum
AC-low detection	Less than 90 V (rms) for one cycle or more
Power cord	
Length	2.7 m (9 ft)
Plug type	NEMA 5-15P for 120 Vac (nominal) models NEMA 6-15P for 240 Vac (nominal) models
Operating environment	
Ambient temperature	10° C to 40° C (50° F to 104° F)
Maximum temperature rate of change	20° C/hour (36° F/hour)
Relative humidity	10% to 90% for a maximum wet bulb temperature of 28° C (82° F)
Maximum altitude	2440 m (8000 ft)
Bit transfer rate (unbuffered nominal)	4.30 M/s
Bit cell width	232.5 ns
Latency	
Rotational frequency	2400 rpm ± 2.5%
Average	12.5 ms (1/2 rotation) ± 2.5%
Maximum	25.0 ms

Table 1-3 RK07 Disk Drive Performance Specifications (Cont)

Characteristics	Specifications
Seek times	
Average	36.5 ms
Maximum	71.0 ms
Start/Stop times	60 seconds maximum, 30 seconds nominal
Model Designations	
RK07-EA	90–128 Vac @ 60 ± 0.5 Hz
RK07-EB	180–264 Vac @ 60 ± 0.5 Hz
RK07-EC	90–128 Vac @ 50 ± 0.5 Hz
RK07-ED	180–264 Vac @ 50 ± 0.5 Hz

NOTE
Models RK07-FA through FD are the dual access models corresponding to models EA through ED respectively.

RK07K-DC Cartridge	
Temperature stabilization time	If the cartridge and drive are at approximately the same temperature, 30 min.; if there is some difference, up to two hours, depending on the difference.
Operating temperature range	16° C to 49° C (60° C to 120° F)
Allowable relative humidity (for operation)	8% to 90% for a maximum wet bulb reading of 28° C (82° F)
Storage temperature range (for recorded disks)	-40° C to 65° C (-40° F to 150° F)
Allowable relative humidity (for storage)	8% to 80% for a maximum wet bulb reading of 28° C (82° F)

Table 1-4 RK611/RK06 Disk Subsystem Options

Option	Description
RK06-EA	Single-access RK06, H969 cabinet, 115 Vac/60 Hz
RK06-EB	Single-access RK06, H969 cabinet, 230 Vac/60 Hz
RK06-EC	Single-access RK06, H969 cabinet, 115 Vac/50 Hz
RK06-ED	Single-access RK06, H969 cabinet, 230 Vac/50 Hz
RK06-FA	Dual-access RK06, H969 cabinet, 115 Vac/60 Hz
RK06-FB	Dual-access RK06, H969 cabinet, 230 Vac/60 Hz
RK06-FC	Dual-access RK06, H969 cabinet, 115 Vac/50 Hz
RK06-FD	Dual-access RK06, H969 cabinet, 230 Vac/50 Hz
RK611-EA	RK06-EA Drive with RK611 Controller
RK611-EB	RK06-EB Drive with RK611 Controller
RK611-EC	RK06-EC Drive with RK611 Controller
RK611-ED	RK06-ED Drive with RK611 Controller
RK611-FA	RK06-FA Drive with two RK611 Controllers
RK611-FB	RK06-FB Drive with two RK611 Controllers
RK611-FC	RK06-FC Drive with two RK611 Controllers
RK611-FD	RK06-FD Drive with two RK611 Controllers
RK06C	Dual access kit
RK611-C	Dual access kit plus one Unibus controller
RK06K-DC	Drive data cartridge
RK06K-AC	Drive alignment cartridge
RK06K-EF	Drive error free data cartridge
70-12292-08	8 ft cable
70-12292-15	15 ft cable
70-12292-25	25 ft cable
70-12292-40	40 ft cable

Table 1-5 RK611/RK07 Disk Subsystem Options

Option	Description
RK07-EA	Single-access RK07, H969 cabinet, 115 Vac/60 Hz
RK07-EB	Single-access RK07, H969 cabinet, 230 Vac/60 Hz
RK07-EC	Single-access RK07, H969 cabinet, 115 Vac/50 Hz
RK07-ED	Single-access RK07, H969 cabinet, 230 Vac/50 Hz
RK07-FA	Dual-access RK07, H969 cabinet, 115 Vac/60 Hz
RK07-FB	Dual-access RK07, H969 cabinet, 230 Vac/60 Hz
RK07-FC	Dual-access RK07, H969 cabinet, 115 Vac/50 Hz
RK07-FD	Dual-access RK07, H969 cabinet, 230 Vac/50 Hz
RK711-EA	RK07-EA drive with RK611 controller
RK711-EB	RK07-EB drive with RK611 controller
RK711-EC	RK07-EC drive with RK611 controller
RK711-ED	RK07-ED drive with RK611 controller
RK711-FA	RK07-FA drive with two RK611 controllers
RK711-FB	RK07-FB drive with two RK611 controllers
RK711-FC	RK07-FC drive with two RK611 controllers
RK711-FD	RK07-FD drive with two RK611 controllers
RK07C	Dual access kit
RK611-C	Dual access kit plus one Unibus controller
RK07K-DC	Drive data cartridge
RK07K-AC	Drive alignment cartridge
RK07K-EF	Drive error free cartridge
70-12292-08	8 ft cable
70-12292-15	15 ft cable
70-12292-25	25 ft cable
70-12292-40	40 ft cable
RK6/7-TA	RK06, RK07 Field Test Box, 115 Vac/50 Hz or 60 Hz
RK6/7-TB	RK06, RK07 Field Test Box, 230 Vac/50 Hz or 60 Hz
RK07U	Upgrade kit to convert RK06 to RK07
RK6/7-TU	Upgrade kit to convert RK06-TA, TB to RK6/7-TA, TB

CHAPTER 2
SUBSYSTEM DESCRIPTION

2.1 INTRODUCTION

The following subsections provide separate drive, controller, and subsystem descriptions that are intended to give an overview of the RK611/RK06 and RK611/RK07 Disk Drive Subsystems and capabilities.

2.2 RK06 AND RK07 DISK DRIVES

The RK06 and RK07 are moving-head disk drives that function as random access mass storage devices (Figure 2-1). The drives perform under the direction of the RK611 Disk Controller and contain all of the response circuitry required to perform those operations for device status reporting and the storage of data.

The storage medium designed for the RK06 Drive is a dual-platter assembly, defined as the RK06K Disk Cartridge, which has a maximum formatted storage capacity of 6.3 million 18-bit words or 6.9 million 16-bit words. Similarly, the RK07 Drive uses a dual-platter assembly, the RK07K Disk Cartridge, as the storage medium. It has a maximum formatted storage capacity of 12.6 million 18-bit words or 13.8 million 18-bit words. As stated before, an RK06K cartridge may only be used in an RK06 Drive, and an RK07K cartridge will only operate in an RK07 Drive.

RK06 and RK07 Controls and Indicators

The following manual controls and indicators are located on the front of each RK06 and RK07 Disk Drive:

- RUN/STOP pushbutton switch with STOP indicator.
- UNIT SELECT plug with READY indicator
- Drive FAULT indicator
- WRITE PROT pushbutton switch with PROTECT indicator
- ACCESS A pushbutton switch with SELECT indicator
- ACCESS B pushbutton switch with SELECT indicator

The switches are selectively used (refer to Chapter 6) to place an associated drive on- or off-line, indicate operational status and error conditions, and provide controller access (whether the drive is a single- or dual-access type).

For drive power, an ON/OFF circuit breaker with a POWER indicator is located at the rear of each drive.

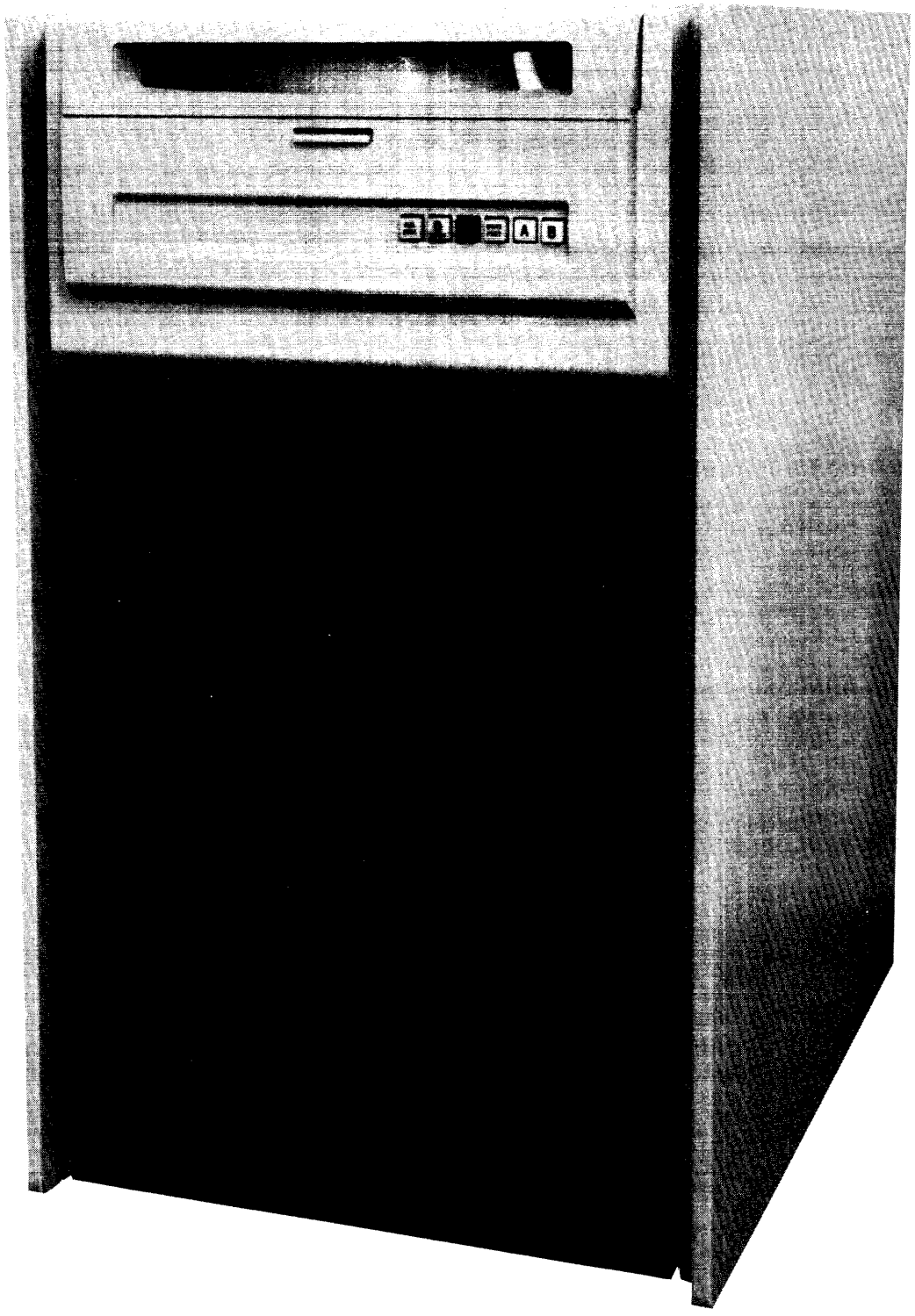


Figure 2-1 H969 Standalone Disk Drive Cabinet

2.3 RK06K AND RK07K DISK CARTRIDGES

The RK06K and RK07K Disk Cartridge assemblies contain two platters (Figure 2-2). Three of the disk surfaces (0, 1, and 2) are available for data storage (read/write surfaces), while the fourth surface (S) is a read-only servo surface that is used for head positioning and the derivation of timing.

Each RK06K disk surface is divided into 411 tracks, and each RK07K disk surface contains 815 tracks. The radial location of each track is defined as a separate cylinder position that is common to all surfaces. Under these conditions, a cylinder can be specified (cylinder address), via a Seek command from the controller, to cause the simultaneous positioning of all four heads to one of the 411 cylinder positions (0–410) for the RK06, or one of 815 cylinder positions (0–814) for the RK07. A single read/write head (0, 1, or 2) can then be defined (track address), via a Read or Write command, to select one of the three read/write surfaces. In this manner, a desired track is accessed for data transfer operations.

Data Track Formatting

During disk formatting procedures, each data track is located and recorded with header information via a Write Header command. The result of this operation effectively divides a track into a number of unique data storage segments that are defined as sectors (Figure 2-3). For 16-bit data words, a single track can accommodate 22 sectors, while for 18-bit data words a track can accommodate 20 sectors. In either case, sectors are the basic, addressable storage unit within the drives, and as such are the final coordinate of track selection during data transfer operations.

2.4 RK611 DISK DRIVE CONTROLLER

The RK611 Disk Controller presents a complete control and data interface to the PDP-11 Unibus (which serves both the central processor and main memory) and the RK06 or RK07 Disk Drives available to the system (Figure 2-4).

2.4.1 Command Control

The RK611 Control interface contains all of the logic required to receive, store, and decode the 13 separate disk commands (e.g., Start Spindle, Seek, Write, etc.) that can be executed by the controller. In addition, the control interface contains all of the logic required to receive and store the status information (i.e., modes, conditions, faults, and errors) delivered from a selected drive. To accommodate the exchange of information (commands/status) between the control interface and a selected drive, information is both sent (commands) and received (status) via a pair of bidirectional serial message lines that are defined as Message Line A and Message Line B.

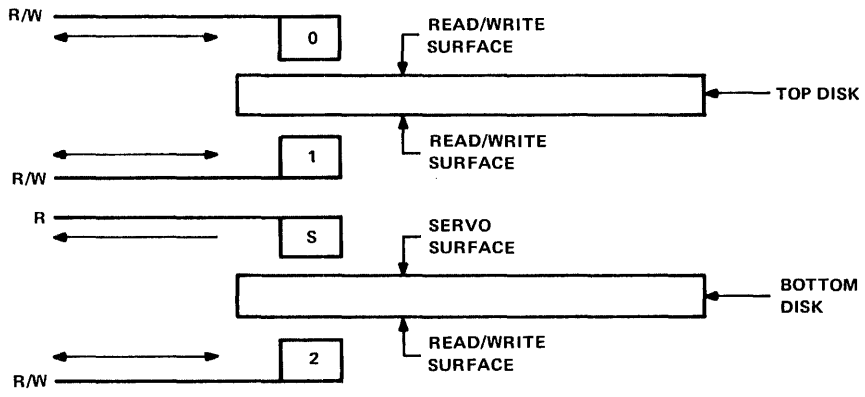
2.4.2 Data Control

The RK611 data interface contains all of the logic required to transfer data (16- or 18-bit words) between main memory and a selected drive. Since Unibus transfers require parallel data flow, while transfers to and from a disk require serial data flow, the data interface also contains parallel-to-serial (memory-to-disk) and serial-to-parallel (disk-to-memory) conversion logic. In addition, a bidirectional read/write data line is used to accommodate the exchange of serial data between the RK611 data interface and a selected drive.

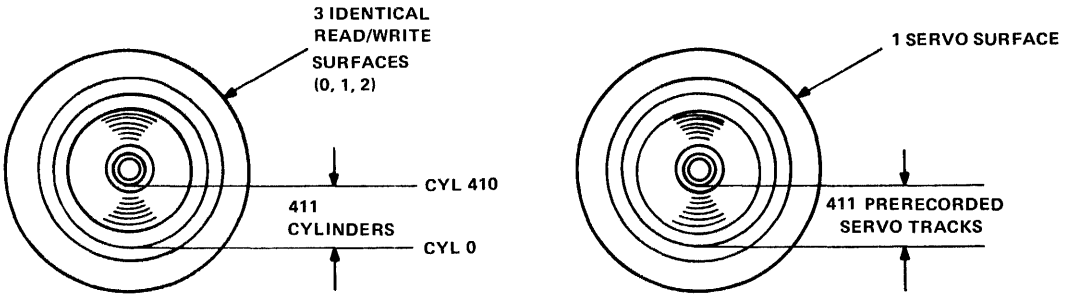
Finally, the data interface logic contains a 66-word data buffer (Silo), that is used to compensate for the timing differences that exist between the average Unibus data transfer rate (4.3 μs/word) and the burst transfer rate of the disk (3.7 μs/word).

2.4.3 Controller Registers

The controller contains 15 Unibus-addressable registers (Table 2-1). Nine of the 15 registers provide temporary storage for the manipulation of status and/or error information. This information, coupled with the inherent diagnostic capabilities of the controller, allows a programmer to create diagnostics that can be extremely effective as a fault isolation aid.

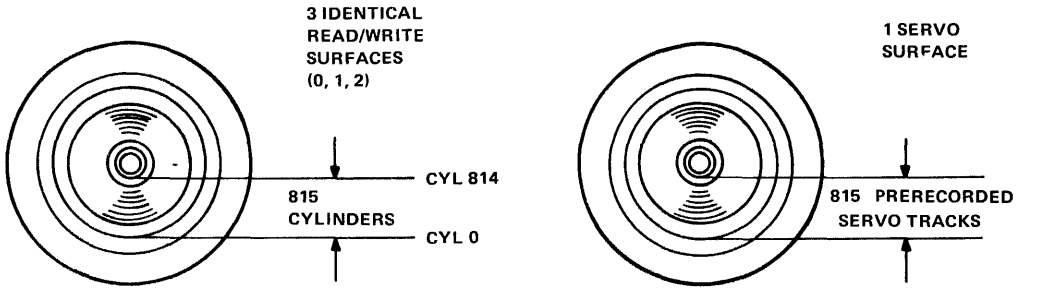


HEAD ORIENTATION



READ/WRITE SURFACES SERVO SURFACE (TIMING & POSITION)

RK06K DISK CARTRIDGE



READ/WRITE SURFACES SERVO SURFACE (TIMING & POSITION)

RK07K DISK CARTRIDGE

ADDRESSING
1. CYLINDER ADDRESS DEFINES 1 OF 411 TRACKS (FOR RK06K) OR 1 OF 815 TRACKS (FOR RK07K).
2. TRACK ADDRESS (R/W HEAD) DEFINES ONE R/W SURFACE.
3. SECTOR ADDRESS DEFINES 1 OF 20 OR 22 SECTORS/TRACK.

MA-0922

Figure 2-2 Read/Write Heads and Data Track Orientation

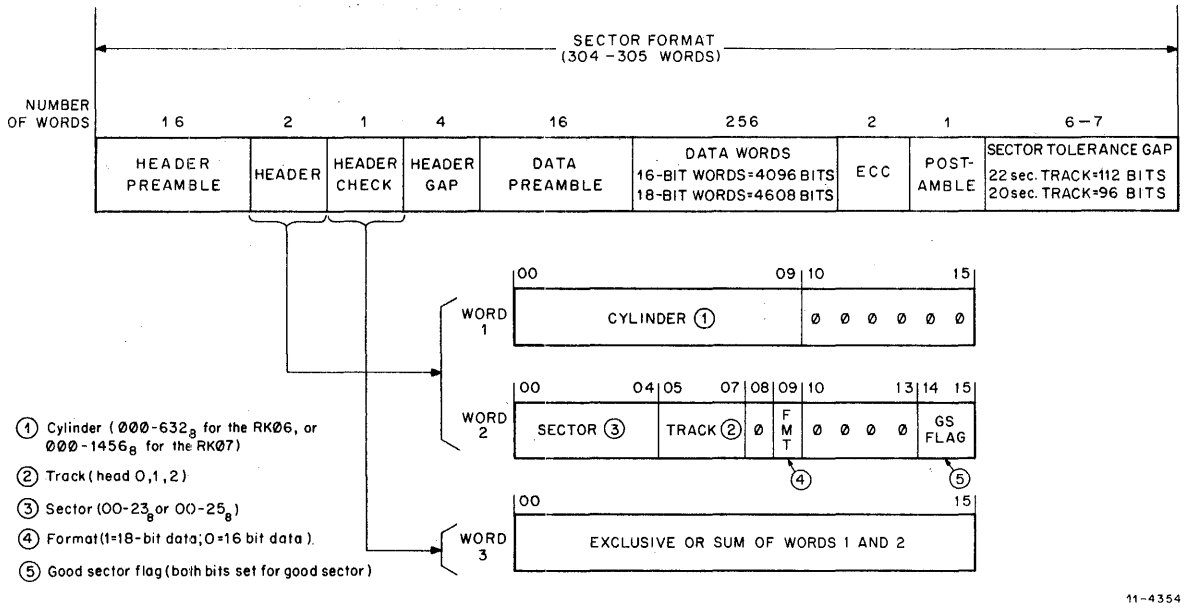


Figure 2-3 Sector Formats

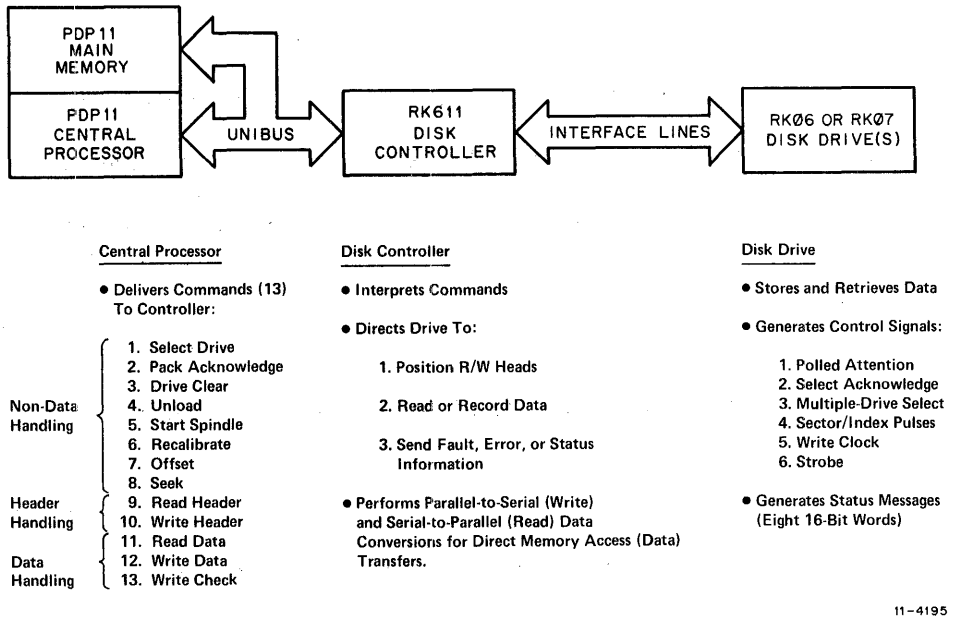


Figure 2-4 Basic RK06 or RK07 Disk Subsystem

Table 2-1 RK611 Unibus-Addressable Registers

Address (octal)	Type	Register	Basic Purpose
777440	R/W	Control/Status Register 1 (RKCS1)	Decode commands/controller status
777442	R/W	Word Count Register (RKWC)	Number of data words for transfer
777444	R/W	Bus Address Register (RKBA)	Main memory location for data word
777446	R/W	Disk Address Register (RKDA)	Desired track/sector address
777450	R/W	Control/Status Register (RKCS2)	Additional control information
777452	R	Drive Status Register (RKDS)	Drive status reports
777454	R	Error Register (RKER)	Additional drive status
777456	R/W	Attention Summary/Offset Register (RKAS/OF)	Drive status change state/head offset value
777460	R/W	Desired Cylinder Register (RKDC)	Cylinder address
777462*			Unused
777464	R/W	Data Buffer Register (RKDB)	Data word to/from Silo
777466	R/W	Maintenance Register 1 (RKMR1)	Drive message select/control
777470	R	ECC Position Register (RKECPS)	Error position information following correction sequence.
777472	R	ECC Pattern Register (RKECPT)	Error correction pattern following correction sequence.
777474	R	Maintenance Register 2 (RKMR2)	Shift register A for serial Message A.
777476	R	Maintenance Register 3 (RKMR3)	Shift register B for serial Message B.

NOTE
R/W = read/write (selected bits) in relation to Unibus. R = read only in relation to Unibus.

*The RK611 responds to this address with SSYN. However, if the bus cycle is a DATI, D (00:15) is undefined.

2.4.4 Silo Memory

During direct memory access (DMA) operations in which a device bypasses the central processor and gains a direct access to main memory, the storage depth of the Silo (66 words) compensates for the transfer rate differences that occur between controller/drive data exchanges and controller/Unibus data exchanges.

When writing, the Silo receives parallel data from the Unibus and transfers the data to a Data Shift Register for serialization. The serial data is then encoded using the modified frequency modulation (MFM) technique. When reading, the MFM encoded data is decoded and sent to the Data Shift Register for conversion to parallel data. The parallel data is then sent to the Silo for eventual transfer to the Unibus (Figure 2-5).

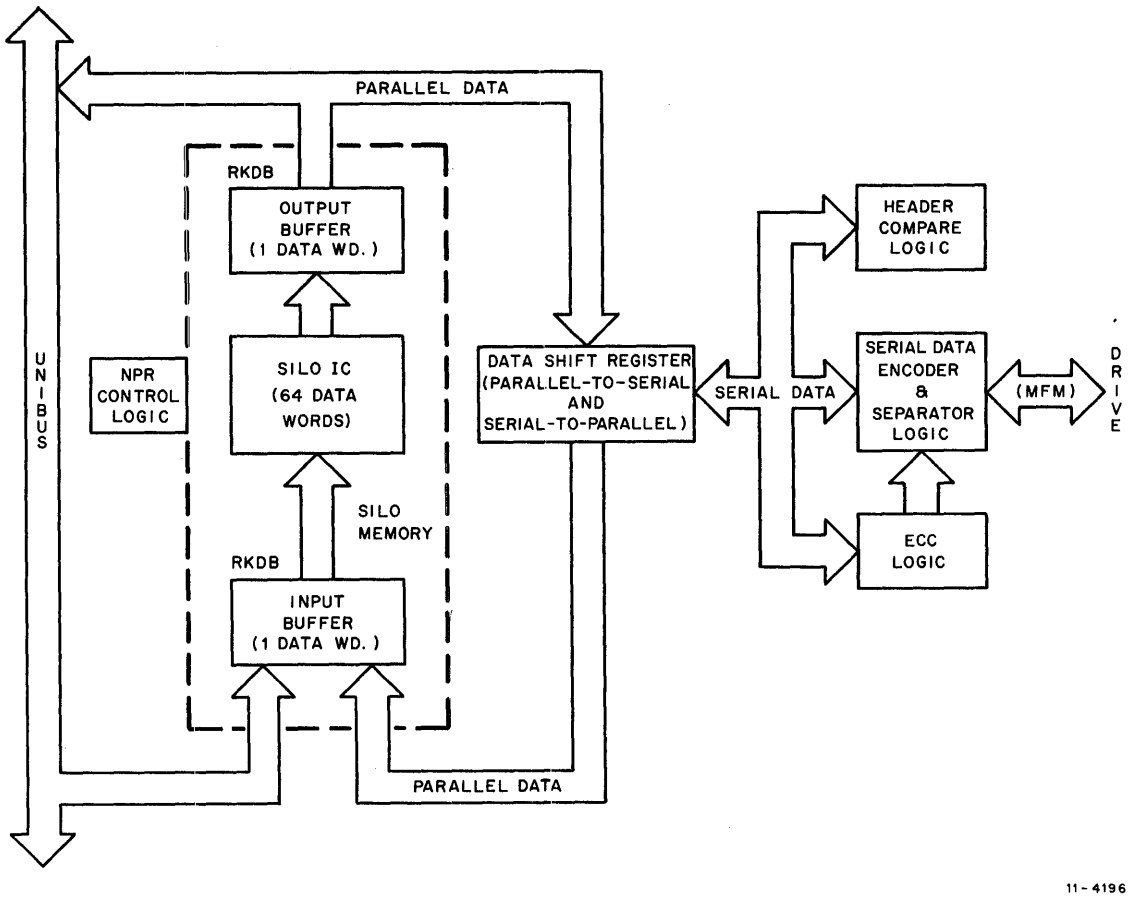


Figure 2-5 RK611 Data Interface

2.5 RK611/RK06 AND RK611/RK07 SUBSYSTEMS

The basic RK06 or RK07 Disk Drive subsystem consists of an RK611 Disk Controller and up to eight RK06 or RK07 Drives that can be connected to the subsystem via a daisy-chain bus arrangement. The controller interfaces to the system via a PDP-11 Unibus. However, if the optional dual-access RK06 or RK07 Drives are installed, an expanded subsystem can be configured. With the expanded subsystem, dual controllers (A and B) are installed which allow each drive to be accessed by either controller via appropriate dual-port selection (A or B). When two controllers are used in this manner, they may be connected to the same Unibus in a single-processor system, or each controller may be connected to a separate Unibus in a dual-processor system (Figure 1-1).

The following paragraphs describe RK06 or RK07 subsystem operations in relation to the functions performed by the controller/drive interface lines (17) under directives imposed by the Unibus-to-controller disk commands concluding with data formatting requirements and data error control operations.

2.5.1 Controller/Drive Interface

The following information describes the operations performed by the controller interface lines (Figure 2-6) that are common to all of the drives available to the system.

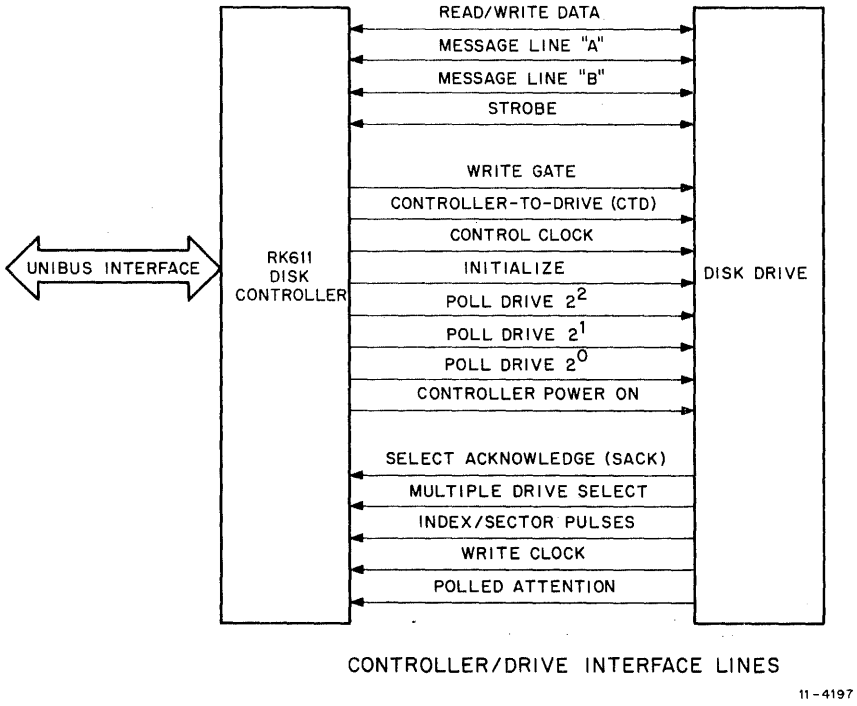


Figure 2-6 Interface Lines

Message A Line

This line transmits (from controller to drive) a drive selection code as the initial 3-bit portion of a 16-bit serial message, the remainder of which includes additional operational information (e.g., Seek, Start Spindle, Head Select Coding, etc.) for the desired drive (Figure 2-7a). Notice, in the Figure, that the control clock timing (T0–T15) reflects the availability of each one of the 16 bits of the message in relation to time.

With these timing considerations, the desired drive is selected by the initial coding (T0–T2) of the serial format. When drive selection recognition is achieved, the remaining drives ignore the remainder of the message (T3–T14).

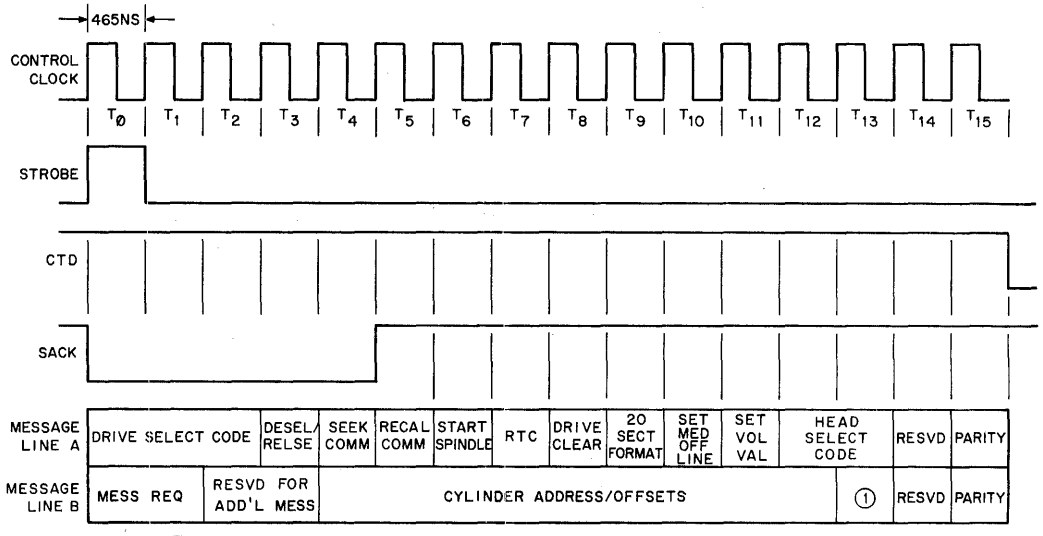
When the operational information has been assimilated by the selected drive, one of four possible 16-bit status messages can be returned from the drive (when requested by the controller) in a similar manner (Figure 2-7b).

Message B Line
In conjunction with the transmission of the Message A line (from controller to drive), a 16-bit message is simultaneously transmitted over the Message B line. The Message B line transmits additional operational information (e.g., cylinder address, offset values, etc.), including a status message selection code. When the operational information has been assimilated by the selected drive, the selected status message (if requested by the controller) is returned (Figure 2-7b).

Control Clock Line
As long as power is available to the controller, the 465 ns Control Clock signal is continuously generated.

Strobe Line
For message synchronization, separate strobe signals are generated in a manner which depends on the direction of the transmission:

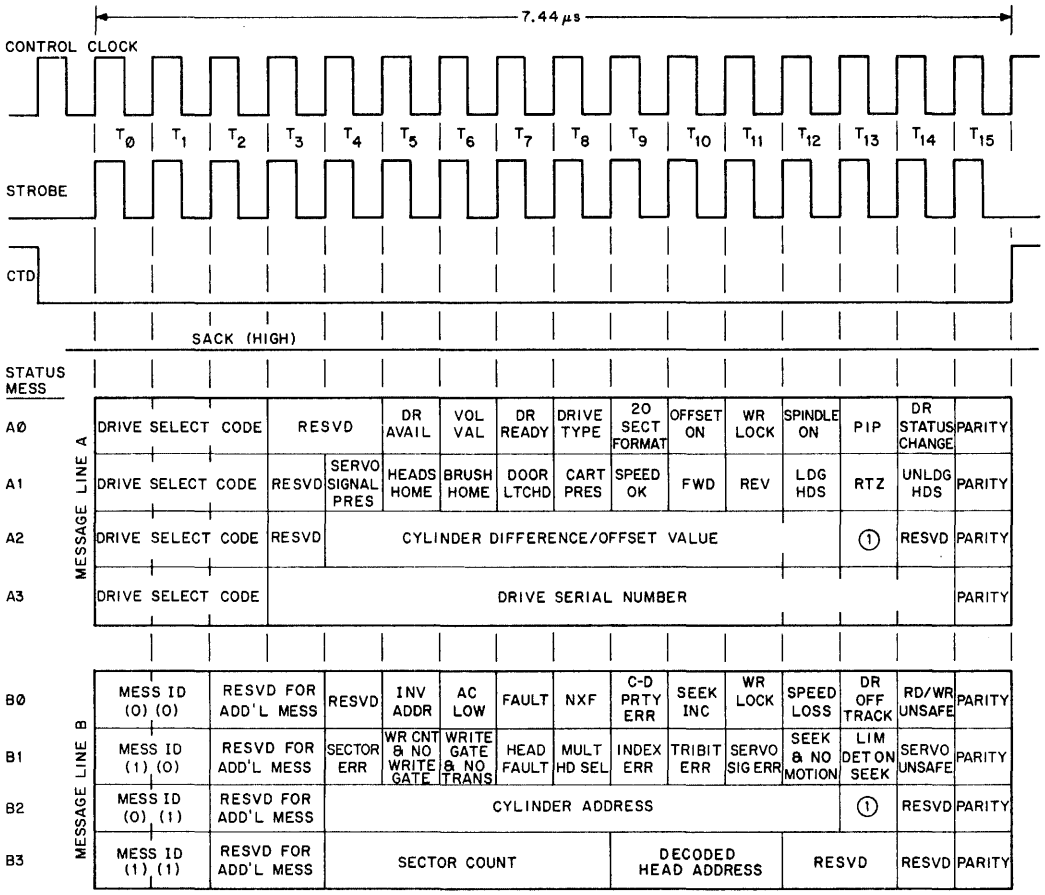
- **Controller-to-Drive Strobe** – During the transmission of Message lines A and B, a single strobe signal is generated as an enable for drive selection code identification (Figure 2-7a).
- **Drive-to-Controller Strobe** – During Message line A and B status reporting, separate strobe pulses (generated by the drive) clock each message bit into the controller (Figure 2-7b).



NOTE①: These bits are used only on the RK07.

a. Controller-to-Drive Transmissions

Figure 2-7 Controller/Drive Serial, 16-Bit Message Formats



NOTE①: These bits are used only on the RK07.

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b. Drive-to-Controller Transmissions

Figure 2-7 Controller/Drive Serial, 16-Bit Message Formats

Controller-to-Drive (CTD) Line

When the CTD line is asserted, the transmission of Message line A and B information from the controller to the drive is enabled. The CTD signal is normally asserted, remaining so for the entire 16 clock times (Figure 2-7a).

When the CTD signal is negated, the selected drive is allowed to transmit status information to the controller (Figure 2-7b).

Select Acknowledge (SACK) Line

When asserted, the SACK line provides a drive-to-controller indication that the drive select code has been recognized and the remaining bits of the message are being accepted. This occurs approximately 300 ns after the receipt of bit 5 (T4) of the controller-to-drive message. The line is negated within 100 ns of the receipt of another controller-to-drive message strobe.

Poll Drive (2^2 – 2^0.) Lines
These three binary-encoded drive address lines are used to poll all drives (0–7) available to the system to determine the attention status of each drive. Regardless of whether a drive is selected or not, the polling mechanism permits the controller to determine which drive (if any) has asserted any attention signal, without serially selecting each drive. The time required to update the attention status of all eight drives is 7.4 μs.

The Attention signal in a drive can be set by any one of the following conditions:

- The completion of a Start Spindle command.
- The completion of a Seek command.
- The completion of an Offset command.
- The beginning of an Unload Heads command.
- The completion of an RTC command (return offset heads to centerline).
- The occurrence of any fault condition.

Polled Attention Line
An Attention signal is activated within a drive when its Drive Status-Change flip-flop is set. However, the Attention line is not asserted to the controller until the unit number (number on the drive UNIT SELECT plug) of the drive is polled, via the Poll Drive (2^2 – 2^0) lines. Thus, each time a drive is polled, and its Drive Status-Change flip-flop is set, Attention will be reported.

The Attention signal is available to the controller approximately 400 ns after the detection of a polling address for the drive, and the signal is negated within approximately 160 ns after the polling address is removed.

Write Clock Line
This drive signal is derived from the servo surface and synchronized with the rotational speed of the disk to ensure the recording of a constant bit density on the data track.

Read/Write Data Line
This line carries encoded digital read data from the drive to the controller and encoded digital write data from the controller to the drive.

Write Gate Line
When active for a write operation, this signal enables the generation of write current in the selected drive. The drive recognizes the assertion of this signal under the following conditions:

- Drive selection achieved.
- Volume valid set (bit T6 of Status Message A0).
- No unsafe read/write condition exists in drive.
- No drive off-track error exists.
- No write protect mode exists.

Index/Sector Pulse Line
When a drive is selected, this line transmits the once-per-revolution index pulse and each of the sector pulses derived from the servo tracks. Index/Sector pulses are enabled when the drive asserts a Select Acknowledge (SACK) and remain enabled until the drive is deselected.

Multiple Drive Select Line
When asserted, this line indicates to the controller that more than one drive has simultaneously responded to a given selection code. To accomplish this, a selected drive monitors the Index/Sector pulse line for the presence of extraneous pulses. If pulses other than those originating from the desired drive are detected, the Multiple Drive Select line is asserted. However, since Index/Sector pulses cannot be generated if the heads of the desired drive are not loaded, the drive uses Control Clock pulses, inserted on the Index/Sector pulse line, to monitor and detect multiple selections.

Finally, the Multiple Drive Select signal is asserted within 300 ns of pulse detection from another drive and negated within 120 ns after the receipt of another message strobe.

Initialize Line
When asserted, this signal deselects all drives, resets all error conditons, and clears the Drive Status-Change flip-flop.

Controller Power on Line
When asserted, this line indicates that power has been applied to the controller, and a physical connection (via cable) has been established between the controller and the available drives. When the line is negated, all drives are deselected, and the Strobe and Control Clock logic is disabled in the drive to prevent any erroneous drive selection.

2.5.2 Subsystem Commands
The 13 subsystem commands (Figure 2-4) can be divided into two basic groups. One group (nondata handling) is concerned with the various operational requirements of the drives, while the second group (data or header handling) is concerned with the transfer of data and header information to or from a selected device.

2.5.3 Data Formatting
When the tracks of a disk are formatted via separate Write Header commands, the following information is recorded to identify each sector in relation to its radial and rotational position on a disk (Figure 2-3).

1. The Header Preamble field contains 16 words, consisting of 255 Zero bits and a single One bit (SYNC) that defines the start of valid information.

2. The Header field consists of two words:

    a. Word 1 contains the cylinder address which defines the radial location of the sector in relation to the 411 (for the RK06) or 815 (for the RK07) addressable cylinders on the disk.

    b. Word 2 contains the sector address—which defines the sector in relation to the number (20 or 22) of sectors per track—and the track address, which defines one of the three R/W heads (and therefore the appropriate R/W surface in relation to the disks) a Format (FMT) bit that is a zero to reflect 16-bit data, or a one to reflect 18-bit data words. Finally, the Good Sector flag (GS FLAG) bits are set to indicate that the sector is valid for the reading or writing of data.

3. The Header Check field consists of one word that is an exclusive-OR sum of header words 1 and 2. The check word is generated by software and extracted during read operations to verify the integrity of both the Header field and the check word.

4. The Header Gap field contains four words, consisting of 64 Zero bits, which provide the time required by the controller to complete a header check and accommodate mechanical tolerances within the drive.

5. The Data Preamble field contains 16 words, consisting of 255 Zero bits and a single One bit (SYNC) that defines the start of the Data field.

6. The Data field accommodates 256 16-bit data words (4096 bits) or 18-bit data words (4608 bits), depending on the format. The extra length required by 256 18-bit words is compensated by the reduction of the maximum number (20) of sectors allowed per track.

7. The Error Correction Code (ECC) field contains a 2-word correction code that is generated by the controller, during a write operation, by the total bit configuration of the 256-word Data field. The ECC field is read during read operations to verify the integrity of both the data and the ECC words.

8. The Data Postamble field consists of one word of Zero bits, which allows the write amplifier to be disabled, when writing, during an unused portion of the sector.

9. The Sector Tolerance Gap contains six or seven words (depending on the data format) of Zero bits, which ensures a differentiation between sectors that is required by the mechanical tolerances.

2.5.4 Servo Surface Operations

For the drive to affect head positioning and the reading and writing of data under the direction of the controller, radial (cylinder) and rotational (sector/index) coordinates are derived from factory-recorded servo track signals (tribits) that are continuously read by the servo head.

When a Seek command is initiated, a desired cylinder address is delivered to the drive from the controller. Within the drive, the difference between the desired and the current cylinder position is calculated. If the difference is other than zero, the head positioning circuitry is energized, and all of the heads (R/W and servo) are driven across the radius of the disk in the direction defined by the difference information. As the search for the desired cylinder position continues, increasing proximity to the cylinder gradually reduces the difference to zero, at which time the heads are appropriately positioned over the desired track. As stated, the servo tracks control this process by generating pulses that are derived from each servo track crossing and fed back to the head positioning circuits as the disk surfaces are radially traversed. When the number of pulses generated equals the number expected (difference minus track crossing equals zero), the desired cylinder is located.

Once the heads are loaded (regardless of whether they are stationary or in motion), the servo signals provide the generation of Sector and Index (once-per-revolution) pulses within the drive. The Sector/Index pulses define the position of each sector for the controller, providing rotational coordinates for read and write operations.

Finally, within the controller, the clock derived from the servo signals is used to synchronize the operation of a phased-locked oscillator (PLO). Synchronization of the PLO circuitry ensures a constant recording density, regardless of minor variations in the rotational speed of the disks.

2.5.5 Data Error Control

The RK611 Controller contains both data error detection and correction logic and a data error recovery capability. When properly supported by appropriate software procedures, these controller features minimize the disruptive effect of data errors from the disks.

Data Error Detection
The following defines the conditions under which data errors can be detected by the controller:

- Data bit errors indicated by the Error Correction Code (ECC) logic.
- The controller has detected a mismatch resulting from a comparison of header data.

For data error correction purposes, each sector contains a 32-bit Error Correction Code (ECC). The code is used with a combination of hardware and software procedures to provide the following:

- Detection and correction of Data field error bursts up to 11 bits in length.
- Detection, without correction, of error bursts from 12 to 32 bits in length.
- Reliable, but not absolute, detection of error bursts greater than 32 bits.

Data Error Correction
Error correction involves the use of error position (error burst location) and error pattern (error burst image) information, which is derived from a 32-bit Error Correction Code (ECC) configuration. Each sector contains an ECC that is written at the end of the Data field and reflects the configuration of the recorded data. The code is used to detect and correct (if possible) the data bits defined by an error burst pattern read from the disk. The controller contains the logic required to generate the ECC configuration during a write and extract the code during a read. However, the actual correction of the data bits defined by the error burst pattern is a software process that occurs after the data is in main memory.

Data Error Recovery
Data error recovery is a recommended sequence of attempted rereads that implements, under program control, both the head offset and error correction capabilities of the controller to improve the probability of a successful recovery. A complete error recovery routine consists of a maximum of 28 data recovery attempts, using error correction procedures with the following operations:

1. Using error correction, attempt to reread the sector 16 times at track centerline.

2. Using error correction, attempt to reread the sector twice, from each of the following head offset positions:

RK06	RK07
+400 microinches	+200 microinches
−400 microinches	−200 microinches
+800 microinches	+400 microinches
−800 microinches	−400 microinches
+1200 microinches	+600 microinches
−1200 microinches	−600 microinches

2.5.6 Bad Sector File
The bad sector file is a list of the bad sectors in the cartridge and is recorded on the highest number track and cylinder on the cartridge. This track is written in 22 sector, 16-bit word format.

2.5.6.1 Data Field Format – The data field in the first 10 sectors of the last track has the following format:

Word	
0	Cartridge serial number
1	Zeros
2	Zeros
3	Zeros for data cartridge, at least a single one for alignment cartridge
4, 5	Bad sector 1
6, 7	Bad sector 2
.	
.	
.	
n, n + 1	Last bad sector
n + 2	Ones filled
n + 3	Ones filled
.	
.	
254	Ones filled
255	Ones filled

Word 0 contains the octal cartridge serial number. Words 1 and 2 are filled with zeros and are reserved for future use. Word 3 identifies the cartridge either as a data or alignment cartridge. If word 3 contains any ones, words 4 through 255 shall also contain ones.

The list identifying bad sectors on a data cartridge is contained in two-word groups beginning with words 4 and 5. The first word of the two-word group contains the cylinder address of the defect, and the second word contains the track and sector address of the defect.

The defective sectors are listed in ascending order by cylinder, track, and sector address. After the pair of words identifying the location of the last bad sector, the remainder of the data field is ones filled.

2.5.6.2 Track Format – The bad sector file format consists of the same preambles, gaps, header, ECC, and postamble as those on any other 22 sector track. The data field of sectors 0, 2, 4, 6, and 8 will contain the addresses of all sectors identified as defective in 22 sector, 16-bit format, and the data field of sectors, 1, 3, 5, 7, and 9 will contain the addresses of all sectors identified as defective in 20 sector, 18-bit format. Sectors 10 through 21 will have words 0 through 3 of the data field record as specified in 2.5.6.1. Words 4 through 255 will be ones filled.

At least two even sectors and two odd sectors out of the first 10 sectors must be error free, and two even and two odd sectors out of the last 12 sectors must be error free.

CHAPTER 3
SITE CONSIDERATIONS AND PREPARATIONS

3.1 ENVIRONMENTAL CONSIDERATIONS

3.1.1 General
The RK611/RK06 or RK611/RK07 Disk subsystem is designed to operate in a light industry or a business environment.

3.1.2 Temperature
The operating temperature range of either Disk Subsystem is from 10° C to 40° C (50° F to 104° F); maximum gradient is 30° F per hour. The nonoperating temperature range is from –40° C to 66° C (–40° F to 151° F). The disk cartridge operating temperature range is from 15.6° C to 48.9° C (60° F to 120° F).

3.1.3 Relative Humidity
Humidity control is important in a data storage system as static electricity can cause errors in any CPU with memory. Either disk subsystem is designed to operate efficiently within a relative humidity range of 10% to 90%, with a maximum wet bulb temperature of 28° C (82° F) and a minimum dewpoint of 2° C (36° F). The nonoperating relative humidity range is from 10% to 95%, with a maximum wet bulb temperature of 46° C (115° F). The relative humidity range for the disk cartridge is 8% to 90%, with a maximum wet bulb temperature of 28° C (82° F).

3.1.4 Heat Dissipation
Heat dissipation of the RK06 or RK07 is 1500 Btu/hr nominal and 1700 Btu/hr maximum. By adding this figure to the total heat dissipation for the other system components, and then adjusting the result to compensate for such factors as the number of personnel, heat radiation from adjoining areas, sun exposure through windows, system efficiency, etc., the approximate cooling requirements for the system can be determined. It is advisable to allow a safety margin of at least 25 percent above maximum estimated requirements.

3.1.5 Acoustics
Most computer sites require at least some degree of acoustic treatment; however, the RK06 or RK07 Disk Subsystem will not contribute unduly to the overall acoustic problem. Acoustic materials should neither produce nor harbor dust.

3.1.6 Altitude
Computer system operation at high altitudes can result in heat dissipation problems. The maximum altitude specified for the RK06 or RK07 is 2440 m (8000 ft). However, maximum allowable operating temperatures are reduced by a factor of 1.8° C/1000 m (1° F/1000 ft) for operation at high-altitude sites. Thus, the maximum allowable operating temperature at 2440 m (8000 ft), for example, would be reduced to 28° C (82° F).

3.1.7 Radiated Emissions

The effects of radiated emissions can be reduced by:

1. Grounding window screens and other large metal surfaces
2. Shielding interconnection cables with grounded shields
3. Providing additional grounding to the system cabinets
4. In extreme radiation environments, providing a grounded cage for the system.

3.1.8 Vibration/Mechanical Shock/Attitude

The RK06 or RK07 is designed to operate within specifications in a moderately controlled environment, such as an office or computer facility, during the following sine vibration test, applied once in each of three orthogonal axes (sweep rate = 1 octave/min):

50–60 Hz	0.002 inch double-amplitude (DA) displacement
50–5000 Hz	0.25 G pk
500–50 Hz	0.25 G pk
50–5 Hz	0.002 inch DA

It is also designed to operate while a half sine shock pulse of 3 G pk and 10 ± 3 ms duration is applied once in either direction of three orthogonal axes (3 pulses total).

Performance of the RK06 or RK07 will not be affected by an attitude where the maximum pitch and maximum roll do not exceed ±5 percent.

3.1.9 Cleanliness

Although cleanliness is important in all facets of a computer system, it is particularly crucial in the case of a device such as the RK06 or RK07 Disk Subsystem. Disk cartridges are not sealed units, while loading, and are extremely vulnerable to dirt. Even such minute obstructions as smoke particles, fingerprint smudges, or dust specks can cause head crashes and catastrophic destruction of heads and/or disk surfaces, as shown in Figure 3-1.

The RK06 or RK07 is capable of operating in an ambient atmosphere containing not more than one million particles of 0.5 micron or larger per cubic foot of air.

During site preparation, there are a number of steps that may be taken to enhance subsequent cleanliness:

1. Seal all windows in the vicinity of the Disk Subsystem.

2. If partitions are to be installed, consider floor-to-ceiling walls which minimize the flow of dust.

3. If painting is to be done in advance of installation, select paint for walls, ceilings, and floors that will not tend to flake or powder excessively. (Waterbound distemper is generally unsatisfactory in this respect.)

4. Check that the flow of air from the air-conditioning system will tend to carry lint, etc., away from the Disk subsystem location. Provide filtration to inhibit dust and other particulants.

5. Select acoustical material that will neither produce nor harbor dust.

6. Avoid glass fiber tiles that could produce abrasive particles and floor coverings that tend to crack or crumble.

7. Provide closed cabinets for disk storage.

8. Clean and vacuum subfloor areas and air-conditioning systems just prior to installation.

9. Place impregnated mats at each entrance to reduce the amount of dust tracked in from other areas.

The disk drive air circulation system (Figure 3-2) is designed to supply clean air for:

1. Disk temperature control.

2. Cleaning of the shroud area by low pressure (3/4 inch of water) at 70 cfm of air.

3. Card cage cooling.

4. Power suply/power amplifier assembly cooling.

To ensure that exhausted air moves freely, floor air-conditioning outlets should not be placed at the rear of the drive.

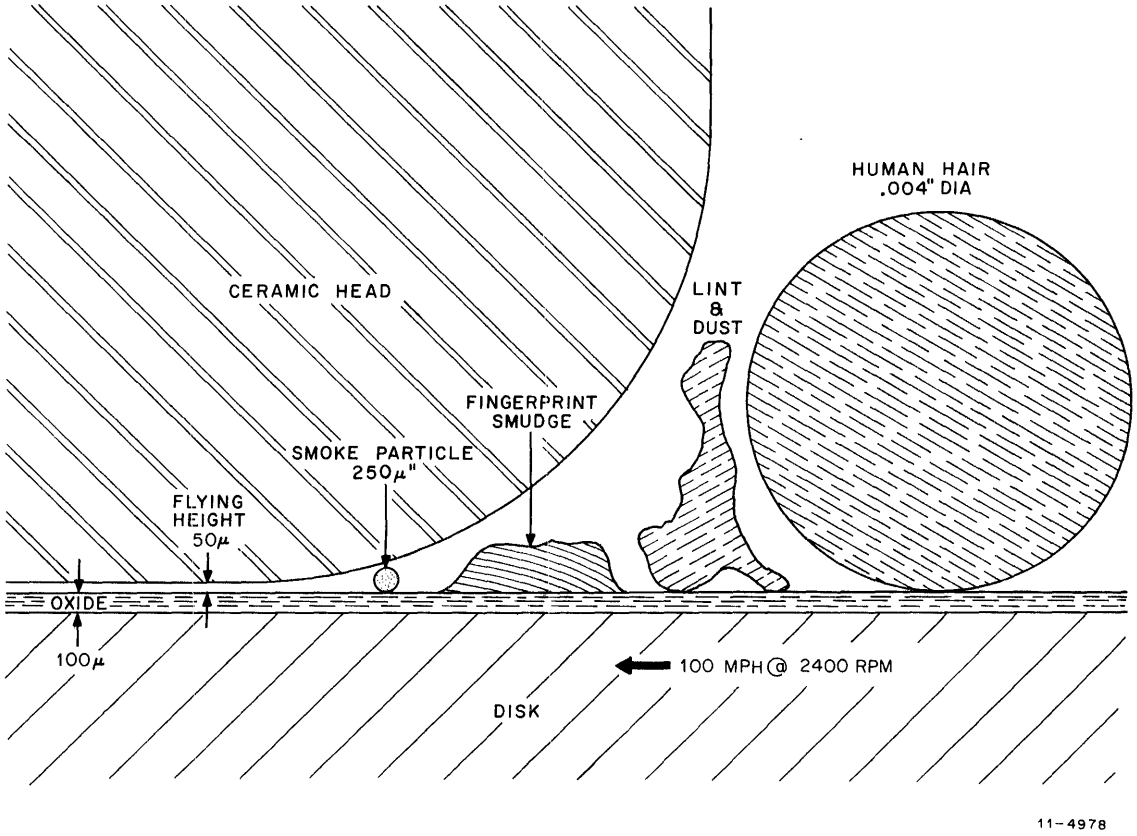


Figure 3-1 Relationship of Disk Head, Disk, and Contaminants

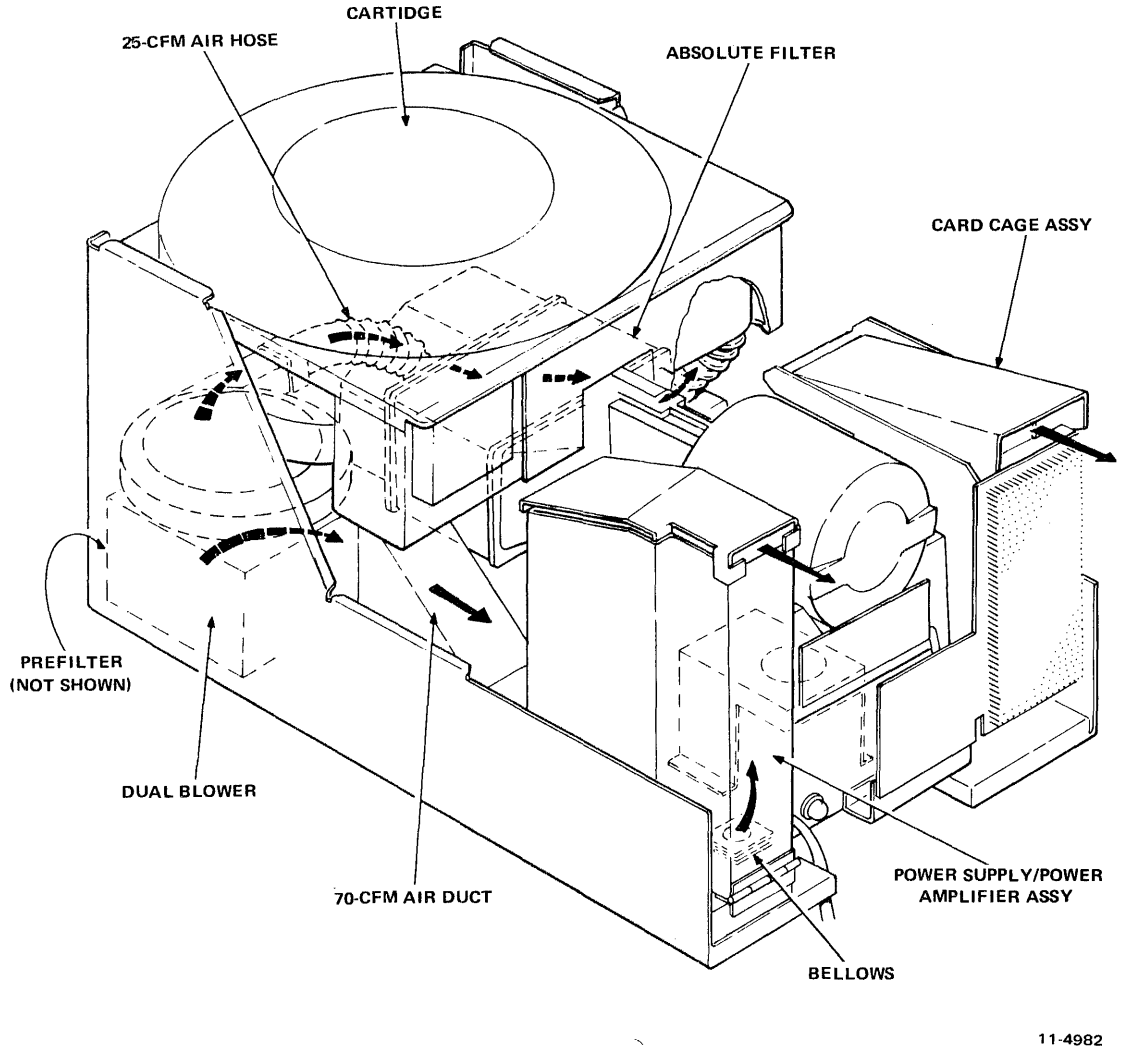


Figure 3-2 RK06/RK07 Disk Drive Air Supply and Distribution Subsystem

3.2 SITE PREPARATION

3.2.1 Space

Provision should be made for service clearances of 916 mm (36 in.) at the front and rear of the RK06 or RK07 disk drive. Space should also be made available in the system environment for storage of disk cartridges, each of which has a diameter of approximately 355 mm (14 in.) and a height of approximately 101 mm (4 in.). No more than five cartridges should be placed in a single stack.

3.2.2 Cabling

Each RK06 and RK07 Disk Drive is equipped with a molded line power cord with a length of 2.7 m (9 ft).

3.2.3 Power Requirements

Both 60 ± 0.5 Hz and 50 ± 0.5 Hz drives operate from 90–128 Vac or 180–264 Vac power sources at a power factor greater than 0.80. While operating at 60 Hz, the RK06 input power is 450 W nominal and 500 W maximum. While operating at 50 Hz, the input power is 500 W nominal and 550 W maximum. While operating at 60 Hz, the input power of the RK07 is 500 W nominal and 550 W maximum, or 550 W nominal and 600 W maximum while operating at 50 Hz.

Receptacles that will accept the 90–128 Vac plugs are designated variously as: DEC (12-05351), NEMA (5-15R), Hubbell (5000-M9), and General Electric (4050-ITA). Receptacles that will accept the 180-264 Vac plugs are designated variously as: DEC (12-11204), NEMA (6-15R), Hubbell (5662ST), and General Electric (4092-ITA). Appropriate circuit breakers are also necessary.

Digital Equipment Corporation must be notified of available input power well in advance of shipment, so that the proper drive may be shipped.

3.2.4 Floor Loading

The weight of the RK06 or RK07 (148 kg/325 lb) alone is not sufficient to place unusual stress on most office building or industrial plant floors. However, the added weight should be considered in relation to the weight of the existing computer system and possible future expansion.

3.2.5 Installation Constraints

The route the equipment will travel from the receiving area to the installation site should be studied in advance to ensure problem-free delivery. Among the factors to be considered are the height and location of loading doors; the size, capacity, and availability of elevators; the number and size of aisles and doors en route; and any restrictions, such as bends or obstructions, in the hallways. Any constraints should be reported to Digital Equipment Corporation as soon as possible so that the requirements of the individual installation site may be considered when the unit is packed for shipment.

3.2.6 Fire and Safety Precautions

The RK06 and RK07 Disk Drives present no unusual or additional fire or safety hazards to an existing computer system. Wiring should be carefully checked, however, to ensure that the capacity is adequate for the added load and for any contemplated expansion. The 60 Hz version of the RK06 or RK07 is UL-listed and CSA-certified. The 50 Hz version complies with IEC 435 standards.

CHAPTER 4
INSTALLATION

This chapter includes the procedures required for unpacking and installing the RK611/RK06 or RK611/RK07 Disk subsystem. Installation will only be performed by qualified DIGITAL personnel. If the equipment is installed by personnel not so qualified, the equipment will lose its CSA rating.

The drive is designed for installation as a free-standing device.

4.1 UNPACKING AND INSPECTION

When packaged for shipment, the RK06 or RK07 in its H969 cabinet weighs approximately 148 kg (325 lb). Although excessively heavy and bulky for single-person handling, the package does not require the use of a forklift or similar equipment for moving or lifting. Table 4-1 lists the special tools and test equipment required for the RK611/RK06 or RK611/RK07 Disk subsystem installation.

CAUTION

When moving or lifting the RK06 or RK07, always grasp the frame structure. Do NOT hold any part of the top or side covers.

Table 4-1 Special Tools and Test Equipment for RK611/RK06 or RK611/RK07 Disk Subsystem Installation

Part No.	Part
RK6/7-TA	Field Test Box (115 Vac, 50 or 60 Hz)
RK6/7-TB	Field Test Box (230 Vac, 50 or 60 Hz)
RK06K-AC	Alignment cartridge (RK06)
RK07K-AC	Alignment cartridge (RK07)
93-06058	Wrench
93-06240	Glass alignment tool
93-06076	Head installation/removal tool
93-06087	Head alignment tool
93-06122-01	Shim, 0.003 in.
93-06122-02	Shim, 0.00015 in.
93-06123-01	Shim, 0.020 in.
93-06123-02	Shim, 0.015 in.
93-06171	Head separation tool
29-19633	Mirror
29-20065	Magnifier
29-20906	Torque wrench
29-21487	Head torque wrench
29-21832	Hex ball driver set
29-22526	Screwdriver, 14.5-in., Phillips
93-06056	Carriage roll alignment tool

The procedure for unpacking the disk drive is as follows:

1. When delivered, the RK06 or RK07 is mounted on a shipping skid and covered by a cardboard carton (Figure 4-1). First, remove the two plastic straps that hold the carton secure to the skid.

2. Remove the lid from the top of the cardboard carton.

3. Remove the staples that fasten the three wooden slats to the bottom flanges of the cardboard-overlay carton. Also remove the staples from that portion of the carton that extends to the bottom of the skid.

4. Visually inspect the cabinet for outward signs of shipping damage. Retain the original packing materials and receipts in case any claims are filed for shipping damage. All damage claims should be promptly filed with the transportation company involved. DIGITAL should be notified immediately of any such claims.

5. Remove the rear and front covers; visually inspect for shipping damage.

6. Inspect for loose cable connectors, terminal points, and subassemblies.

7. Inspect the logic backplane in both (X and Y) axes for bent pins.

8. Pull rearward on the logic assembly and power supply assembly. Both assemblies will open 90 degrees for access to components. Ensure that all logic modules are in proper locations (refer to Figures 4-2 and 4-3).

9. Check the cable connectors and modules in the logic assembly (card nest) to ensure tightness.

10. Check the power supply assembly for loose cables, connectors, and connection of air distribution system bellows (Figure 3-2) and proper installation of the motor release pin.

11. Inspect the absolute filter area for proper attachment of hoses. Clean the foam prefilter if necessary.

12. Check the head cam area to ensure that the head arms are engaged properly on the head cam.

13. If any problems are encountered during execution of the above procedures, refer to the *RK06/RK07 Disk Subsystem Service Manual* for corrective procedures.

14. Close the hinged power supply and card nest assemblies and replace all access covers.

15. Remove both bolts securing the cabinet to the shipping skid.

16. Remove the skid blocks and position the cabinet leveling feet so that the cabinet rests on its casters.

17. Remove the cabinet from the shipping skid, using a ramp or other suitable device. At this point there are no other shipping restraints for the drive.

WARNING
Use care in moving the drive/cabinet.

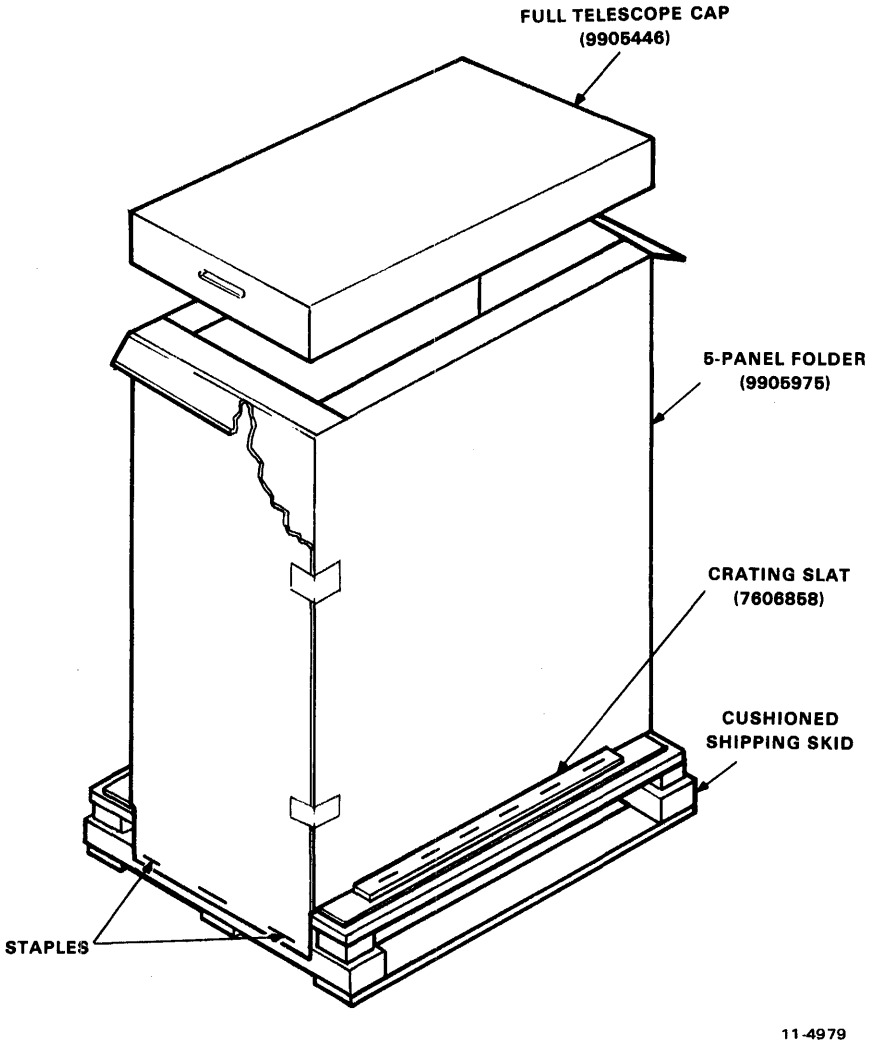


Figure 4-1 RK06/RK07 Shipping Package Configuration

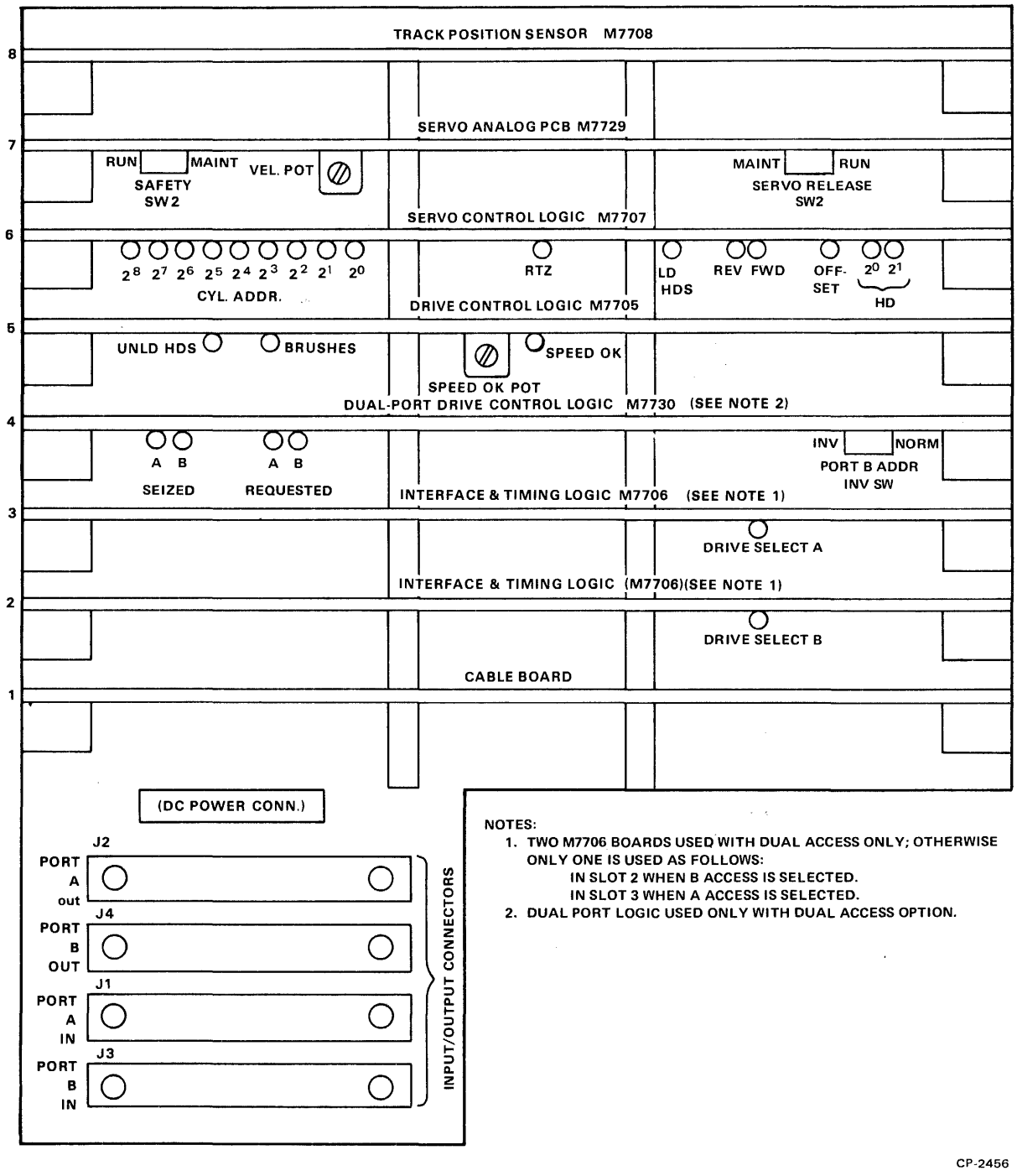


Figure 4-2 RK06 Disk Drive Logic Module Locations

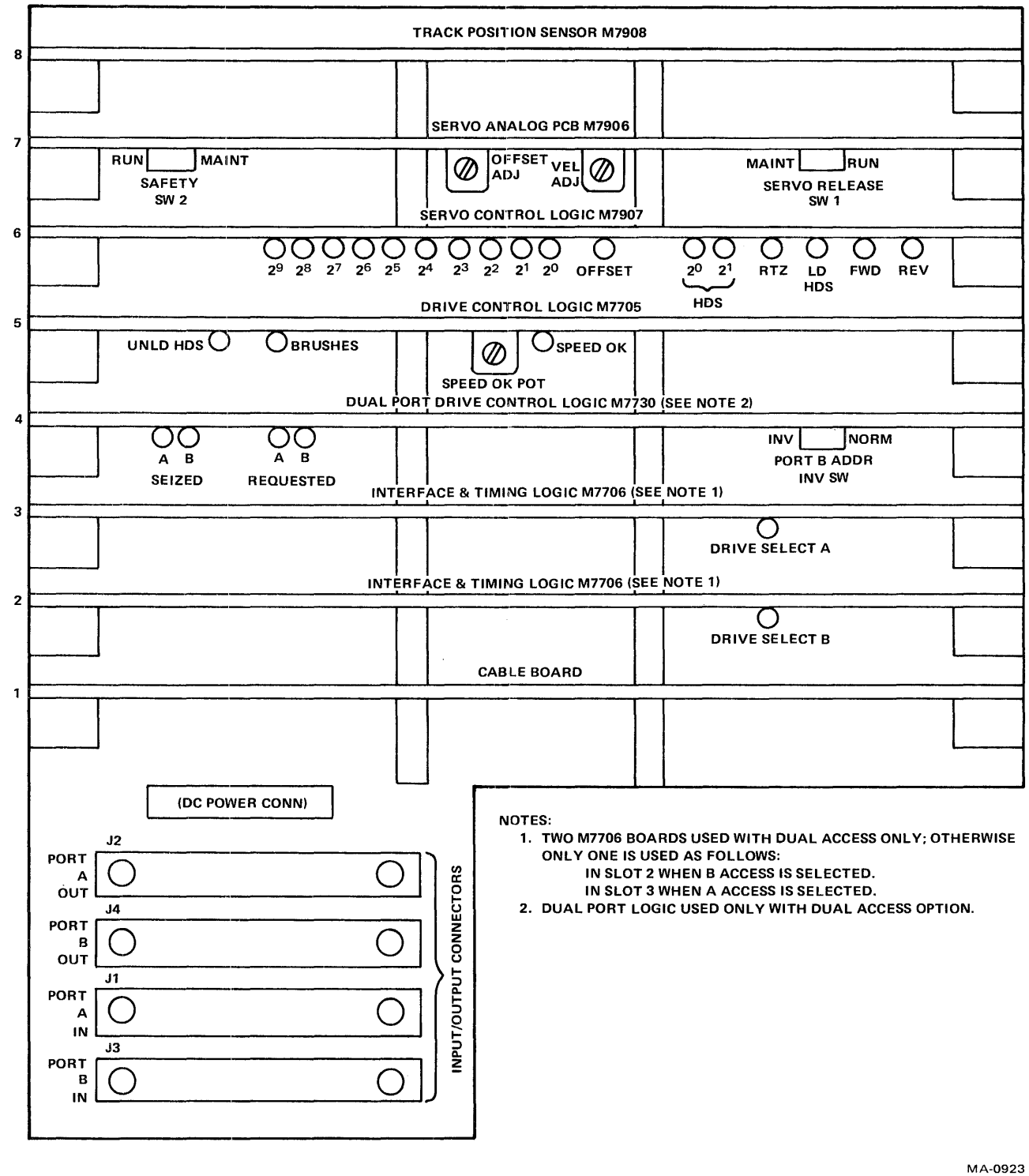


Figure 4-3 RK07 Disk Drive Logic Module Locations

4.2 SAFETY PRECAUTIONS

When performing the installation procedures in Paragraph 4.3, observe the following precautions to avoid injury to personnel or damage to the equipment.

1. Keep fingers and hands out of the area between the cartridge and the carriage while drive power is ON.

2. Always remove ac power cables when it is necessary to work inside the drive.

CAUTION

Always remove wristwatch before servicing the drive (linear-motor electromagnetic fields are destructive to watches).

3. Use only nonmagnetic tools near the recording area of the disk cartridge. Use care when working in the linear-motor area with ferrous materials. Keep read/write heads away from the electromagnetic area.

4. Avoid touching or blowing breath on read/write heads. Skin acids can etch and ruin heads; breath can cause condensation deposits that disfigure the gliding surface.

5. Never move the carriage assembly forward manually without a spinning disk in place or the head-separator tool installed.

6. Never remove or change modules without shutting down all internal drive power.

4.3 INSTALLATION PROCEDURE

The procedures for installing the RK611 Controller and the RK06 or RK07 Disk Drive are covered in the following paragraphs.

4.3.1 RK611 Controller

To install the RK611 Controller in a PDP-11 expander box:

1. Remove the RK611 from its shipping container.

2. Install the RK611 backplane into the designated expander box and secure with the screws provided in the accessories bag. Install power harnesses (2), using expander box instructions.

NOTE

For RK07 installations, the M7901 must be above ETCH E. If not, FCO no. M7901-003 must be added. (Step 3 is FCO no. M7901-003.) If the M7901 is above ETCH E, skip step 3. For all RK06 installations, skip step 3.

3. If the subsystem contains any RK07 Disk Drives, verify that the RK611 Controller has been modified to operate with RK07 Drives as well as with RK06 Drives. To make this verification, ensure that the following changes have been made to the M7901 module:

   a. On Side 2, the etch at pin E11-11 has been cut.
   b. On Side 2, the etch at pin E12-5 has been cut.
   c. On Side 1, a wire has been added, connecting E11-10 to E11-11.
   d. On Side 1, a wire has been added, connecting E12-5 to E17-2.

Table 4-2 RK611 Control Switch Configurations for Desired Unibus Address and Interrupt Vector

Switch Section	Unibus Bit	Switch Section	Unibus Bit
S1-1	A12	S2-1	NA
S1-2	A11	S2-2	D08
S1-3	A10	S2-3**	D07
S1-4	A09	S2-4	D06
S1-5	A08	S2-5	D05
S1-6*	A07	S2-6	D04
S1-7*	A06	S2-7**	D03
S1-8	A05	S2-8	D02

* For the standard address of 777440, these switches should be in the ON position; all others should be in the OFF position. Note that this address overlaps the Look-Ahead Register in the RC11 Disk Subsystem.

** For the standard vector of 210, these switches should be in the OFF position; all others should be ON. Note that this vector overlaps the interrupt vector in the RC11 Disk Subsystem.

4. Set the switch configuration for the desired Unibus address and interrupt vector into the M7900 module. Use Table 4-2 as a guide when making these settings.

5. If the controller is to be connected to a PDP-11/40 system, remove the M7234 from the processor. Remove W5 on the M7234 and replace the module in the backplane. This jumper must be removed to successfully run the RK06 or RK07 diagnostics.

6. Insert the modules into the RK611 backplane using Figure 4-4 as a guide.

7. Attach the transition connector assembly (PN-70-12415-0-0) to the cabinet containing the RK611 using the nuts and bolts provided.

8. Connect the flat cable (PN-BC06R-06) from the M7904 module to the Berg connector side of the transition connector. Refer to Figure 4-5 for placement of the striped edge of the cable.

9. If the RK06 or RK07 subsystem is to be dual ported, repeat this procedure for the second controller.

NOTE

Check for a different address and vector on the second controller.

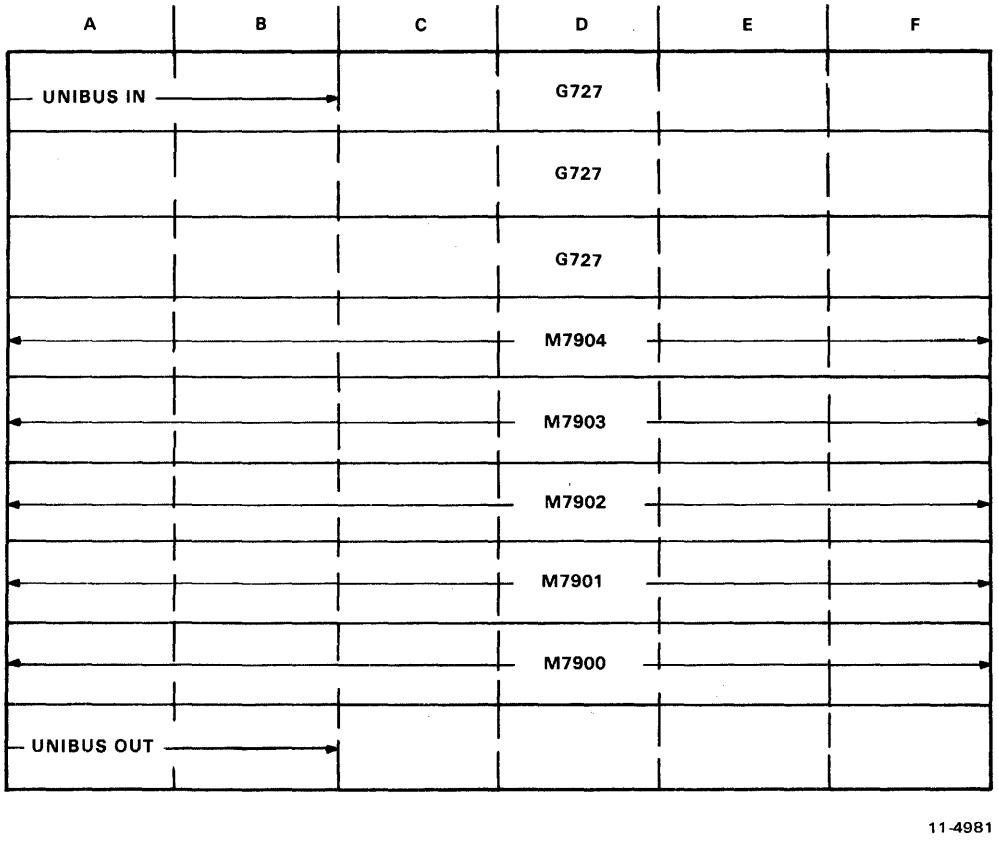
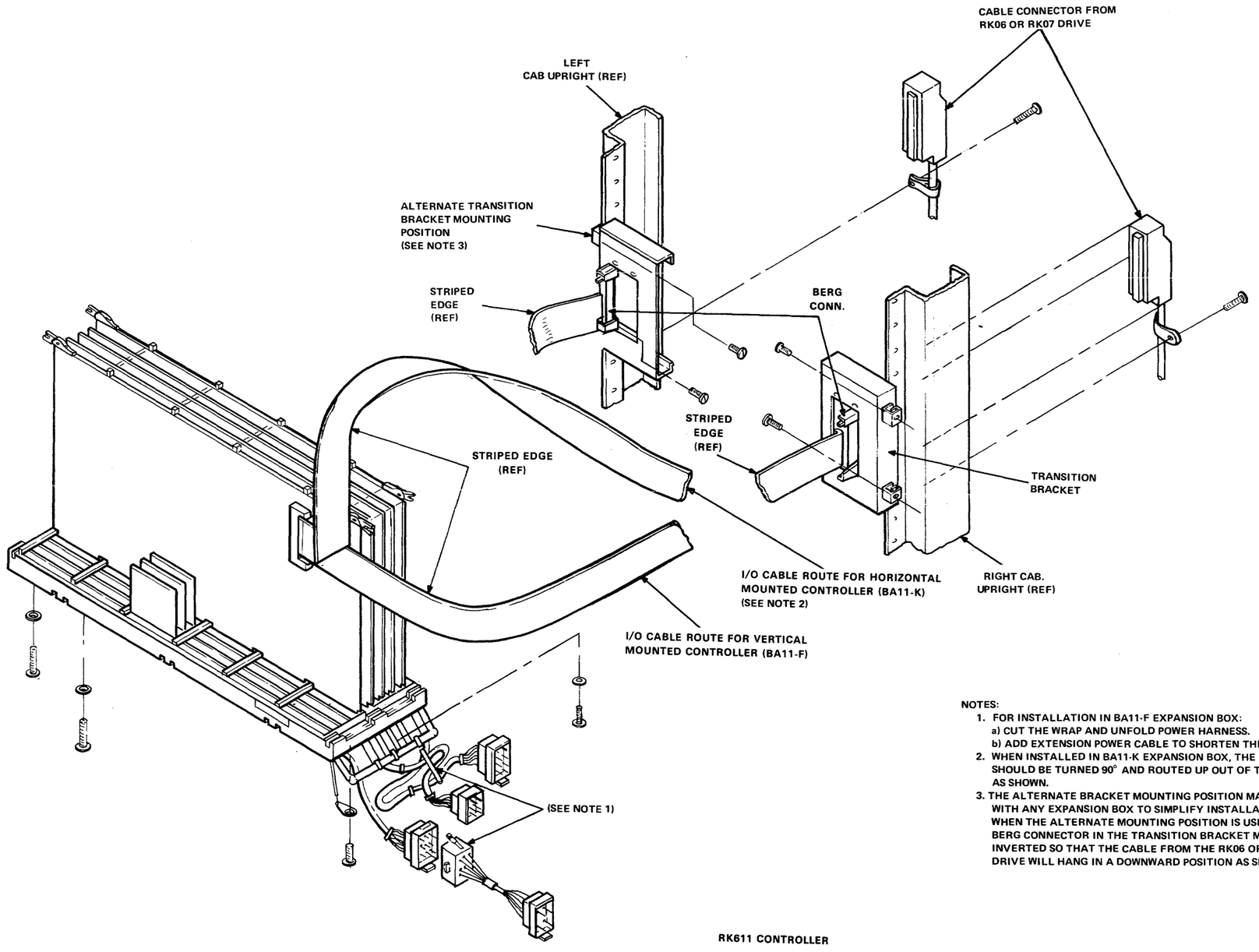


Figure 4-4 RK611 Controller Backplane (from Module Side)



NOTES:

1. FOR INSTALLATION IN BA11-F EXPANSION BOX:
   a) CUT THE WRAP AND UNFOLD POWER HARNESS.
   b) ADD EXTENSION POWER CABLE TO SHORTEN THE HARNESS.
2. WHEN INSTALLED IN BA11-K EXPANSION BOX, THE I/O CABLE SHOULD BE TURNED 90° AND ROUTED UP OUT OF THE BOX AS SHOWN.
3. THE ALTERNATE BRACKET MOUNTING POSITION MAY BE USED WITH ANY EXPANSION BOX TO SIMPLIFY INSTALLATION. WHEN THE ALTERNATE MOUNTING POSITION IS USED, THE BERG CONNECTOR IN THE TRANSITION BRACKET MUST BE INVERTED SO THAT THE CABLE FROM THE RK06 OR RK07 DRIVE WILL HANG IN A DOWNWARD POSITION AS SHOWN.

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Figure 4-5 RK611 I/O Connector Details

4.3.2 RK06 or RK07 Disk Drive

To install the disk drive:

1. Roll the drive cabinet to its designated location. Level the cabinet by lowering the four leveling feet attached to the cabinet until all weight is removed from the casters.

2. Remove the front and rear access covers from the drive.

3. Verify that the model number listed on the serial tag (Figure 4-6) corresponds to the site power requirements. Refer to the voltage ranges given in Figure 4-6, and if a discrepancy exists, correct it before continuing with the installation.

4. Connect a ground wire (PN-7212827-25) from the ground stud on the H969 cabinet to the ground stud on the cabinet containing the RK611 Controller (Figures 4-8 and 4-9).

5. Lower the card nest assembly to its horizontal (service) position and install a drive bus cable (PN-70-12292-xx) between the transition connector (PN-70-12415-0-0) of the controller cabinet and I/O connector J1 (A-IN) of the RK06 or RK07 (Figure 4-7 and Table 4-3). The standard drive cable length from controller to drive is 7.62 m (25 ft). However, optional cable lengths can be used if the total drive bus does not exceed 30.48 m (100 ft). (See Table 4-3 for part numbers.)

Table 4-3 Drive Bus Cables

Part No.	Length
70-12292-8	2.44 m (8 ft)
70-12292-12	3.66 m (12 ft)
70-12292-25	7.62 m (25 ft)
70-12292-40	12.19 m (40 ft)

6. On some drives, there are two rows of 12 zero ohm resistors on the M9016 module. They represent the last three digits of the drive serial number and must be clipped to give the BCD representation of these three digits. If they have not already been clipped, remove the top resistor of a pair to represent zero, or remove the bottom resistor for a one, for each of the 12-bit locations. Also, there is a pair of zero ohm resistors, representing the drive type, placed to the left of the serial number resistors. If neither has been removed, clip the top one if the drive is an RK06 or the bottom if the drive is an RK07.

   If the M9016 module does not have these resistors, the serial number must be wired to the back plane. To do this:

   a. Set up a table similar to this:

Table 4-4 Sample Table for Backplane Wiring

	A				B				C				
	800	400	200	100	80	40	20	10	8	4	2	1	
Row 1													
Row 2													
	A	A	A	A	A	B	A	B	B	B	A	A	
	0	1	1	1	1	1	1	1	1	1	1	1	Backplane
	6	4	4	4	4	4	4	4	4	4	4	4	Pin
	R	P	R	S	S	M	T	D	C	A	V	V	Assignments
	2	1	1	2	1	2	2	1	1	1	1	2	

b. For a serial number ABC, enter the BCD equivalent of digit A in Row 1, Column A; enter the BCD equivalent of digit B in Row 1, Column B; enter the BCD equivalent of digit C in Row 1, Column C.

c. Enter the complement of Row 1 in Row 2.

d. For every "1" in Row 1, wire the appropriate backplane pin (below Row 1 and Row 2) to pin D6H1 (+3 V). For every "1" in Row 2, wire the appropriate pin to A6T1 (ground).

e. If the drive is an RK06, wire 01V1 to A1T1 (ground). If the drive is an RK07, wire 01V1 to D6H1 (+3 V).

7. If the installation is multidrive, proceed to step 8; otherwise, proceed to step 10.

8. Connect drive bus cable (PN-70-12292-xx) from J2 (A OUT) of the previous drive to J1 (A IN) of the next drive. Repeat for each additional drive. The standard length between drives is 2.44 m (8 ft); however, optional length cables are available. Total drive bus length must not exceed 30.48 m (100 ft).

9. Daisy chain each drive, using a ground wire (PN-7212827-8) between the ground studs in the drive cabinets.

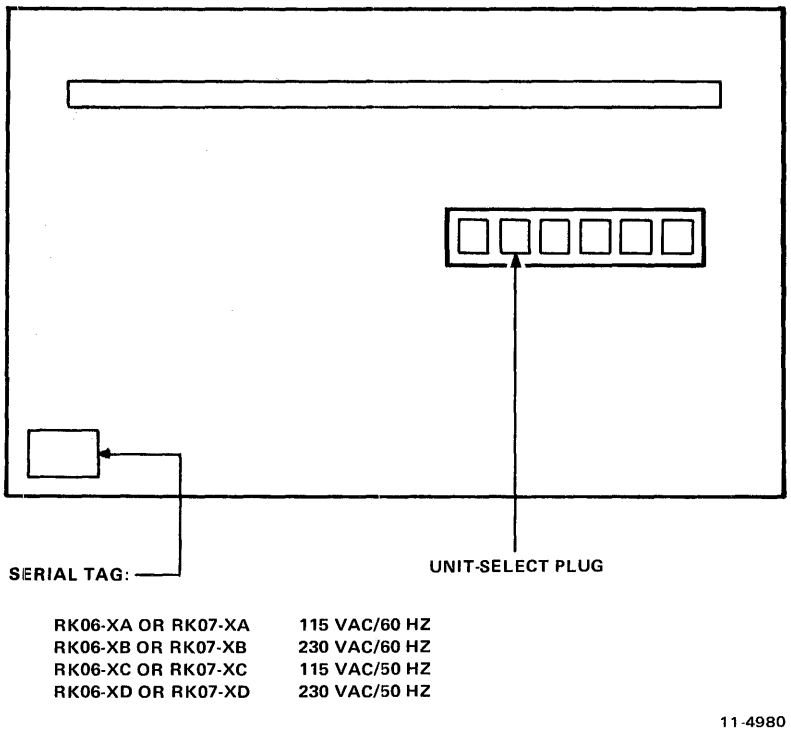

Figure 4-6 Serial Tag Location and Model Identifications (Tag Visible with Front Cover Removed)

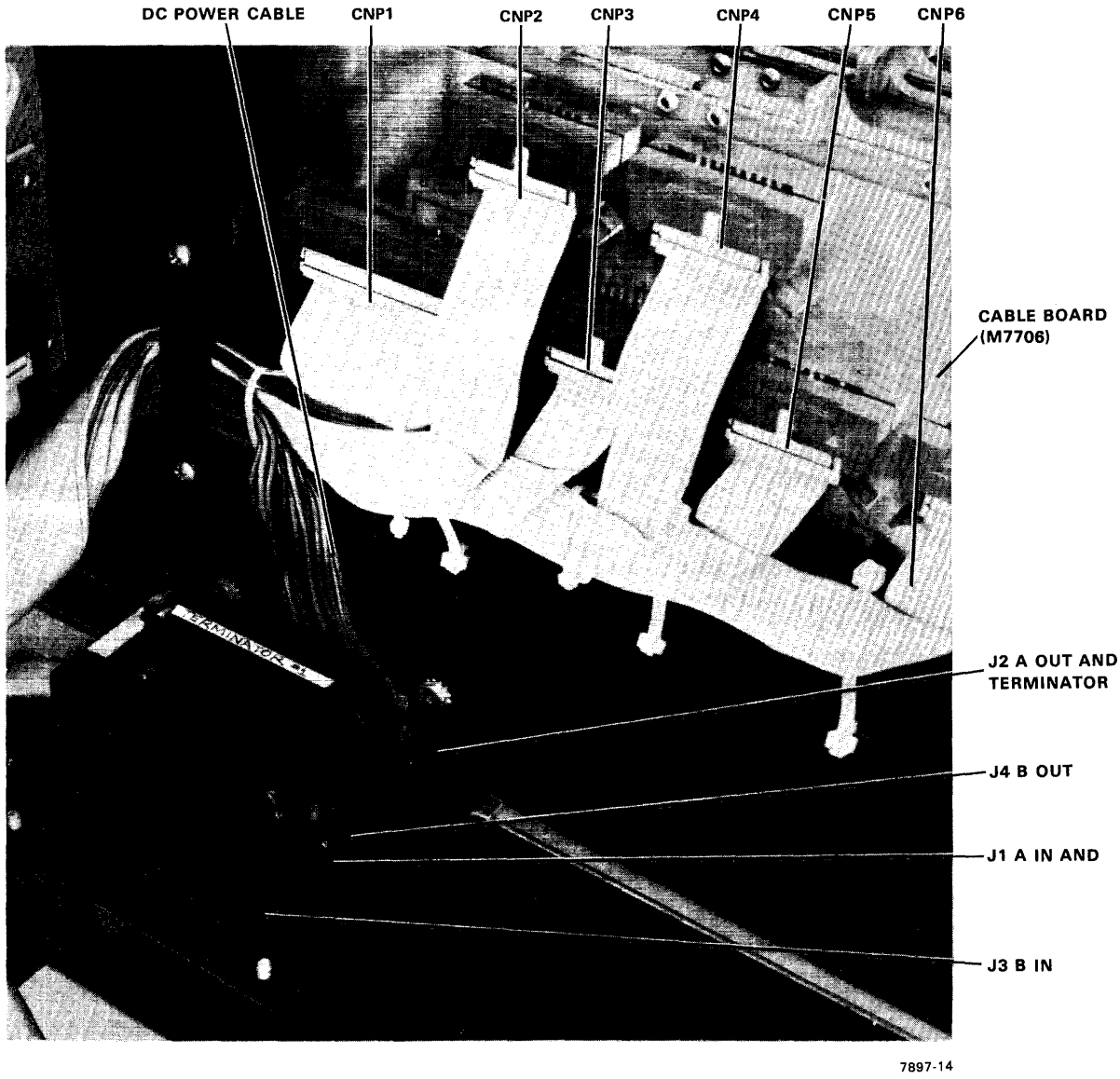

Figure 4-7 RK06/RK07 I/O Connector Details

CABLE CHART				
FROM		TO		REMARKS
CONNECTION	WITH	CONNECTION	WITH	
CONTROLLER	—	J1A IN	DRIVE	
CONTROLLER	—	J3B IN	DRIVE	
J2A OUT	DRIVE	NEXT DRIVE	DRIVE	OR TERMINATED (SEE NOTE)
J4B OUT	DRIVE	NEXT DRIVE	DRIVE	

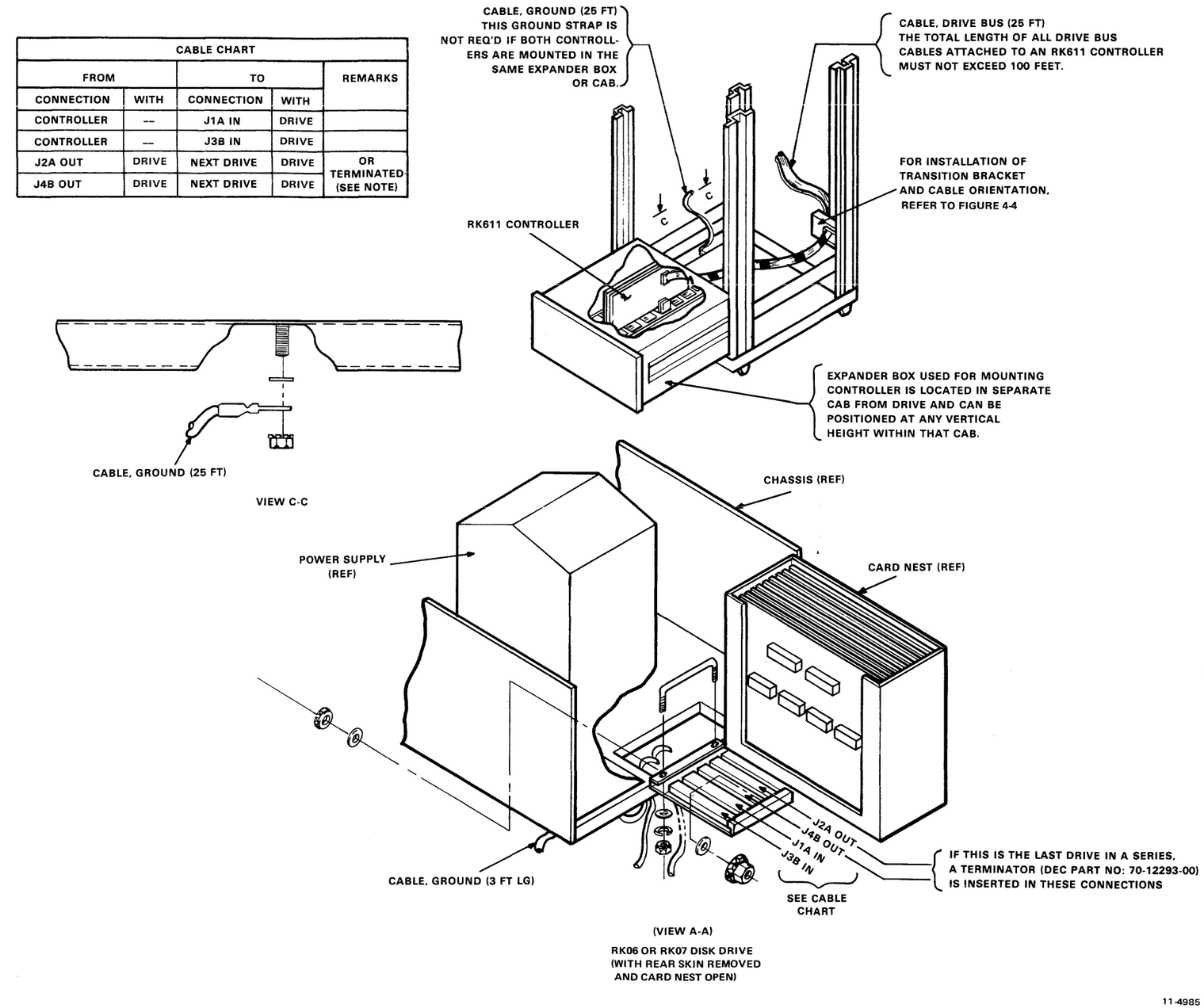

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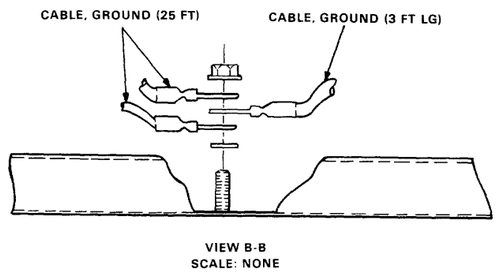
Figure 4-8 Dual-Access Disk Subsystem H969 Cabinet



VIEW B-B
SCALE: NONE

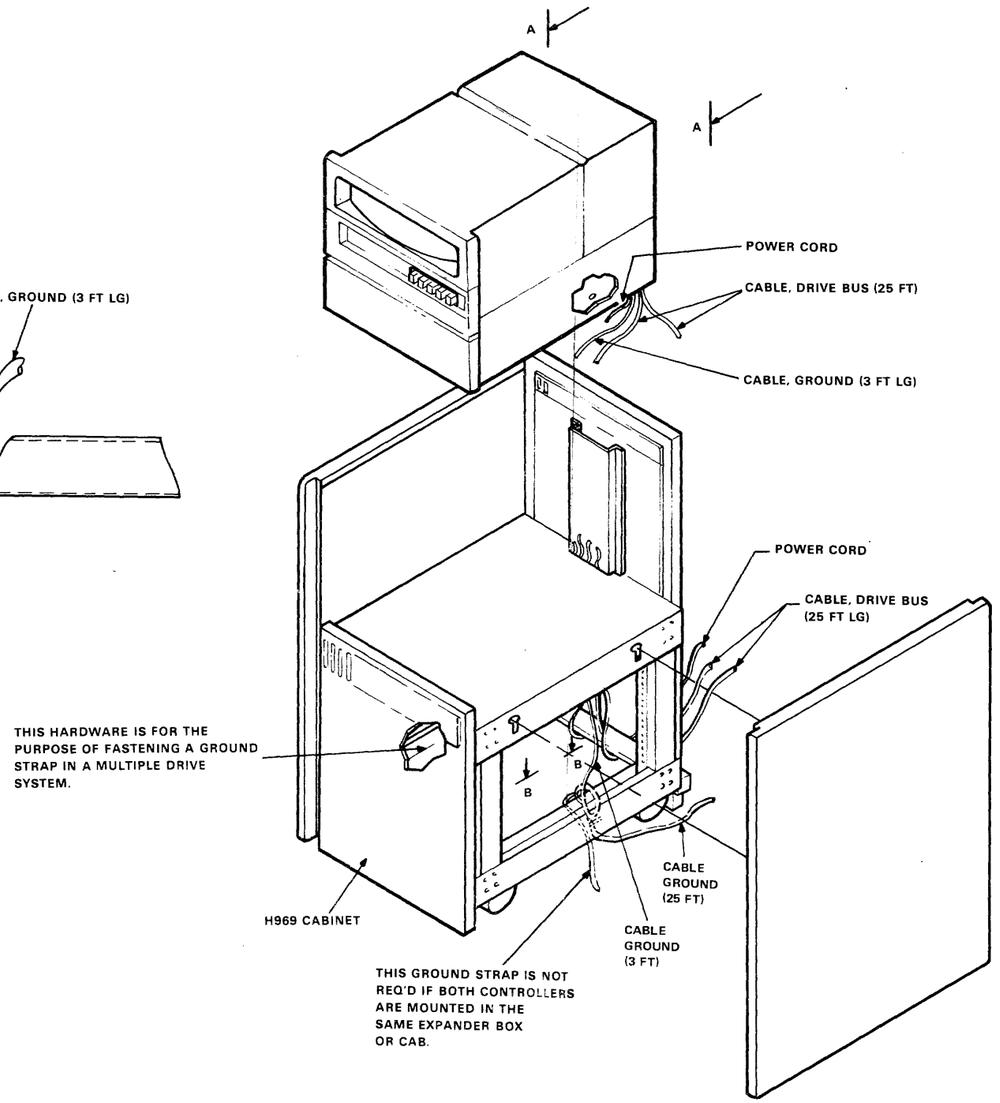


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Figure 4-9 Dual-Access Disk Subsystem H969 Cabinet

10. For the last drive, connect a drive bus terminator (PN-70-12293-0-0) to I/O J2 (Figure 4-7).

NOTE

For the dual-controller cabling configuration (Figure 4-7), the installation of the drive bus cable should follow the above sequence. The drive connectors used are J3 (B IN) and J4 (B OUT). A second drive bus terminator (PN-70-12293-0-0) must be connected to J4 (B OUT) of the last drive. The second controller may be mounted in the same expander box as the first or in another cabinet altogether. If the same box is used, a second transition connector is mounted in the cabinet to accommodate the second drive bus cable.

11. Ensure that circuit breaker CB1 is OFF. Connect the power cable to a power outlet whose voltage and frequency meet the requirements of the drive model (Figure 4-6).

12. Insert the proper drive-select plug into the unit select jack of the operator control panel (Figure 4-6). Table 4-5 lists the part numbers for each of the eight drives in the daisy chain configuration.

Table 4-5 Unit-Select Plugs for RK06/RK07 Disk Drives

Plug No.	Part Number
0	12-12691-0
1	12-12691-1
2	12-12691-2
3	12-12691-3
4	12-12691-4
5	12-12691-5
6	12-12691-6
7	12-12691-7

4.4 INSTALLATION CHECKS AND ADJUSTMENTS

To verify performance and adjust the disk subsystem:

1. Check controller power supply voltage.
2. Check drive power supply voltage.
3. Check head load/unload.
4. Check head alignment.
5. Check response to abnormal conditions.

The required actions are detailed in Paragraphs 4.4.1 through 4.4.5.

4.4.1 Controller Power Supply Voltage Checks

To perform the required voltage checks on the controller power supply, set controller power to ON and make measurements at the following points:

Test Point	Voltage
A04 A2	+5 Vdc ± 0.25 V
A04 B2	-15 Vdc ± 0.75 V
A04 C2	GND
A04 D2	+15 Vdc ± 0.75

If any voltage is out of tolerance, refer to the appropriate expander box manual for adjustment and/or repair procedures.

4.4.2 Disk Drive Power Supply Voltage Checks

To perform the required voltage checks on the disk drive power supply:

1. Ensure that the power cable is connected to a power outlet of the proper voltage and frequency rating.

2. Ensure that the RUN/STOP switch is in the STOP position.

3. Set circuit breaker CB1 to the ON position. The air system should start operating and the lid-lock solenoid will energize to enable the lid.

4. Check the five output voltages at the logic backplane:

Backplane Location	Voltage
B08A2	+5 Vdc ± 3%
D01E2	+25 Vdc ± 10%
C08D2	+15 Vdc ± 5%
C08B2	-15 Vdc ± 5%
A08R2	-5 Vdc ± 3%

If any voltage is not within tolerance, refer to the *RK06/RK07 Disk Subsystem Service Manual* for adjustment and/or repair procedures.

4.4.3 Head Load/Unload Checks

The following head load/unload checks are performed during the POWER ON sequence to ensure that operational status can be attained:

1. With power ON, install a scratch cartridge into the drive.

2. Depress the appropriate access select switch, either A or B.

3. Press the RUN/STOP switch. After approximately one second, the spindle will begin to rotate and the RUN/STOP light will extinguish.

NOTE

Power must be applied to the controller (or to the Field Test Box, if used) during performance of the load/unload checks.

4. When the disk reaches nominal speed (after approximately 30 to 60 seconds), the heads will load onto the disk surfaces and begin a slow movement toward the inner limit. After reaching this limit, they then return to cylinder zero. When head motion has stopped, the READY light on the operator control panel should be lit. The FAULT light should not be lit.

5. Press the RUN/STOP switch again. The READY light should extinguish and the heads move to their fully retracted position. When the drive has stopped, the RUN/STOP indicator will light. The drive motor should stop in approximately 20 seconds after the RUN/STOP switch is released.

4.4.4 Head Alignment Checks and Cartridge Care

Several principles should be understood before attempting any alignment procedures. A familiarity with these principles will hopefully discourage any "shortcuts" leading to possible damage or improper alignment.

1. Whenever head alignment exceeds ±200 microinches maximum, the heads should be realigned to within ±50 microinches.

2. Power must be applied to the drive for two hours prior to performing any head alignment procedures.

3. The cartridge should be mounted and spinning for a minimum of one-half hour prior to beginning head alignment.

4. Head alignment techniques assume that the drive being aligned is a properly working device. If the device is not working properly, do not attempt alignment.

5. To protect the alignment pack, Write Protect should always be set when the alignment pack is in the machine.

6. The SAFETY SWITCH on RK06 module M7729 or RK07 module M7906 (near the D end) forces Write Lock and disables the Servo Unsafe circuit. It is important to remove this special maintenance switch from its maintenance mode to re-enable the Servo Unsafe circuit.

7. Linear forces applied to the carriage during adjustments may cause the heads to unload and cause damage if the SAFETY SWITCH is not set to the MAINT position.

8. Lateral force on a carriage can cause the heads to tilt and possibly crash. Therefore, all procedures requiring the application of a lateral force to the carriage must be performed with the heads unloaded.

9. Positioner parts and fixtures are precision parts and must be handled carefully. The use of torque wrenches set to specified levels is mandatory to guarantee that tolerances will hold and thus prevent damaged parts.

10. When transporting cartridges by auto, always keep the cartridges in the passenger compartment – never in the trunk.

11. Always transport cartridges in their carrying case.

4.4.4.1 Head Alignment Using Program Control – To perform head alignment checks under program control:

1. Remove the rear cover from the RK06 or the RK07.
2. Ensure that power is removed from the RK06 or RK07 and the Field Test Box.
3. Connect the head alignment cable from the Field Test Box to the RK06 or RK07 Read/Write board (Figure 4-10 and Figure 4-11).
4. Apply power to the RK06 or RK07 and the Field Test Box.

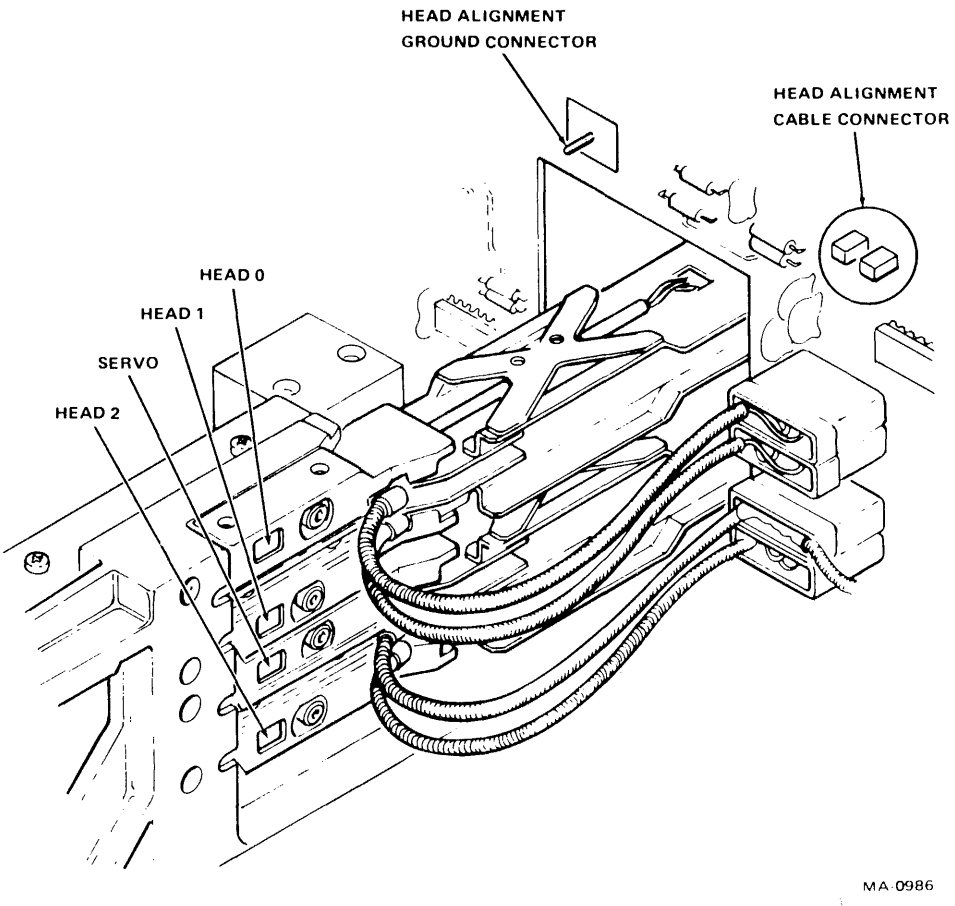


Figure 4-10 RK06 Head Assembly Area

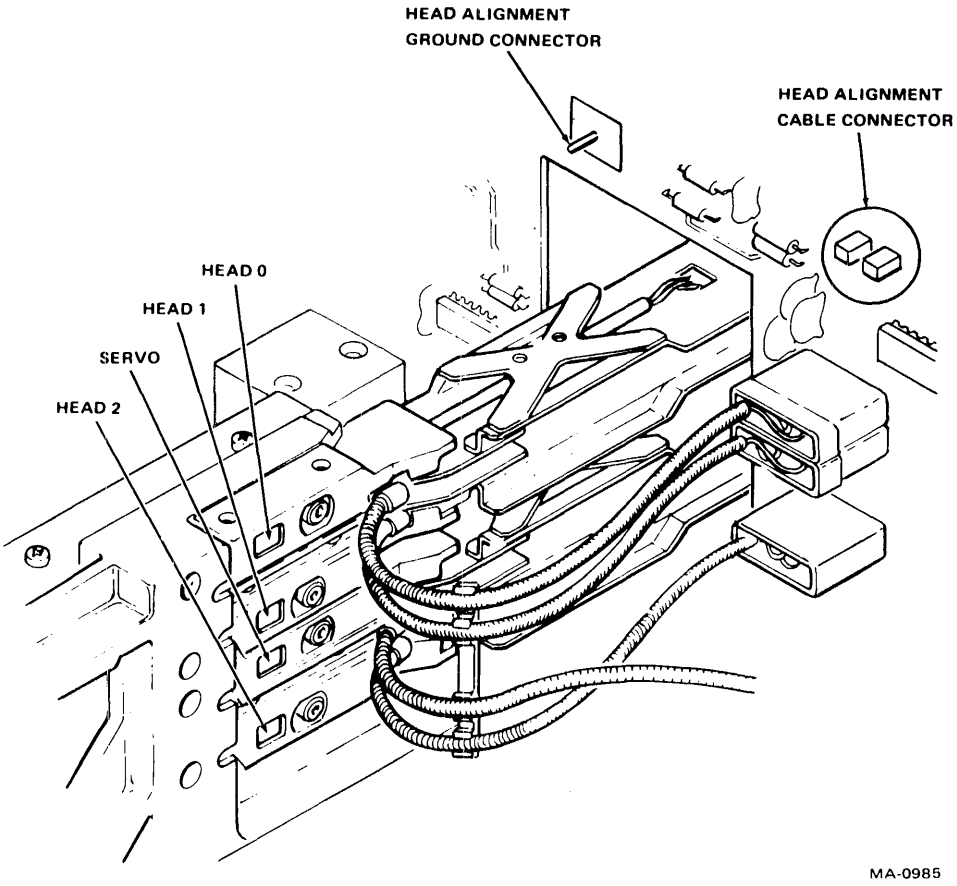


Figure 4-11 RK07 Head Assembly Area

5. Load MAINDEC-11-DZR6N and start at address 224.

   Per program instructions, install an RK06K-AC or RK07K-AC alignment cartridge, depending on the type of drive, and WRITE LOCK the drive.

   NOTE

   Prior to begining head alignment procedures, power should be applied to the drive for two hours; the cartridge should be mounted and spinning for at least one-half hour.

   To WRITE LOCK the drive, set the SAFETY SWITCH (S2) on the RK06 M7729 board or the RK07 M7906 board to the MAINT position. This action will also prevent the heads from unloading if a Servo Unsafe condition occurs.

6. Respond to program questions 1 through 5 as illustrated in the sample printout in Paragraph 4.4.4.2.

7. Mount the head alignment fixture on the appropriate head (Figures 4-10 and 4-11).

CAUTION
Make sure that the carriage does not tip beyond the point where the heads will fall out of the cam tower.

8. Torque the head alignment fixture mounting screw to 5 in/lb. Loosen the head mounting screw and then torque it to 2 in/lb. Turn both vertical screws of the head alignment fixture fully CCW.

9 Load the heads by typing the letter R.

10. Set the torque wrench to 5 in/lb. Tighten the forward vertical screw to move the head forward or the rear screw to move the head toward the rear. Since these screws cause oposite actions, the screw not in use must be turned fully CCW. Adjust until:

    a. The red LED on the meter is ON (steady state).

    b. The meter on the Field Test box reads 0 ± 50 microinches.

NOTE
If the needle deflects to the right of zero, move the head toward spindle; if to the left of zero, move away from spindle.

11. Unload the heads by typing the same head number again. Tighten the head to 5 in/lb.

12. Reload the heads by typing the letter R.

13. Check that the conditions of steps 10a and 10b are met.

14. Unload the heads by typing the next head number.

15. Remove the head alignment fixture and mount it on the next head.

16. Repeat steps 8 through 15 for each data head.

17. When all heads have been aligned, restart the program under its Exerciser mode and exercise the drive for two minutes. Recheck the alignment of all heads.

18. Remove the alignment cartridge and the Field Test Box; clear the WRITE LOCK condition.

19. Replace the rear cover removed in step 1.

4.4.4.2 Sample Printout

```
DZR6N-D - RK611/RK06-RK07 SUBSYSTEM VERIFICATION : PART 2


*** RK06-07 HEAD ALIGNMENT AID ***
FOR HELP TYPE H, ELSE CR
H
INSTRUCTIONS FOR USING RK06-RK07 HEAD ALIGNMENT AID :
**************************************************
MOUNT AN RK06 OR RK07 ALIGNMENT CARTRIDGE ON THE DESIRED
DRIVE, AND INSURE THAT THE DRIVE IS WRITE-LOCKED.
CONNECT THE ALIGNMENT INDICATOR TO THE DESIRED DRIVE,
VIA THE HEAD ALIGNMENT CABLE ONLY, AND CYCLE UP THE
DRIVE. AFTER MOUNTING THE PACK ON THE DRIVE,
THE OPERATOR SHOULD WAIT 30 MINUTES FOR THE DRIVE
TEMPERATURE TO STABILIZE, BEFORE PROCEEDING WITH
ALIGNMENT.

RESPOND TO ALL REQUESTS FOR PARAMETERS, BY ENTERING
THE DESIRED PARAMETER VALUE (NO <CR> NEEDED).
THERE ARE TWO MODES OF OPERATION : MANUAL MODE
ALLOWS SELECTION OF DRIVES AND HEADS BY TTY INPUT,
AND AUTO MODE ALLOWS DRIVES AND HEADS TO BE SELECTED
BY OFF-ON OPERATION OF DRIVE PORT SELECT SWITCHES.
IN EITHER MODE, UP TO 5 MINUTES OF SEEK EXERCISES
MAY BE REQUESTED FOR EACH DRIVE.
ALSO IN EITHER MODE, A VERIFY OPERATION ALLOWS HEAD
SELECTION WITHOUT THE UNLOADING AND LOADING OF
THE DRIVE BY THE PROGRAM, WHICH OTHERWISE OCCURS
TO ALLOW MANIPULATION OF THE ALIGNMENT TOOL.
TO RESTART EITHER MODE, TYPE ^Z .
TO RESTART ALIGNMENT AID, TYPE ^R .
TO SELECT NEW DRIVES IN MANUAL MODE, TYPE ^C .

FOR HEAD ALIGNMENT PROCEDURE, REFER TO FIELD
TEST BOX (RK06-07TA, RK06-07TB) OPERATOR'S MANUAL.

MANUAL OR AUTO MODE (M OR A)?
M


* MANUAL SELECT MODE *

ENTER DRIVE NO. (0-7):
0
DRIVE SER. NO.  ?

ALIGN, VERIFY OR EXERCISE (A, V, OR E)?
A
```

```
* MANUAL SELECT ALIGNMENT *

ENTER HEAD NO. (0-2)
0
TYPE <R> WHEN READY:
R
HEADS POSITIONED AT CYLINDER 365 (OCT)
HEAD 0 SELECTED

ENTER HEAD NO. (0-2) :
1
TYPE <R> WHEN READY:
R
HEADS POSITIONED AT CYLINDER 365 (OCT)
HEAD 1 SELECTED

ENTER HEAD NO. (0-2) :
2
TYPE <R> WHEN READY:
R
HEADS POSITIONED AT CYLINDER 365 (OCT)
HEAD 2 SELECTED

ENTER HEAD NO. (0-2) :
^Z

ALIGN, VERIFY, OR EXERCISE (A, V, OR E) ?
E
TYPE <R> WHEN READY
R


*RANDOM SEEK EXERCISES IN PROGRESS ON DRIVE 0
^Z

ALIGN, VERIFY, OR EXERCISE (A, V, OR E) ?
V


* MANUAL SELECT VERIFY *

ENTER HEAD NO. (0-2) :
2
HEADS POSITIONED AT CYLINDER 365 (OCT)
HEAD 2 SELECTED

ENTER HEAD NO. (0-2) :
^Z
```

4.4.4.3 Head Alignment Using the Field Text Box

1. Remove the rear cover from the RK06 or RK07.
2. Remove power from the RK06 or RK07 and from the Field Test Box.
3. Connect the head alignment cable from the Field Test Box to the RK06 or RK07 read/write board.
4. Attach the appropriate drive interface cable to the Field Test Box.
5. Apply power to the RK06 or RK07 and to the Field Test Box.
6. Install an RK06K or RK07K alignment cartridge, depending on the drive, and WRITE LOCK the drive.

NOTE

Prior to beginning head alignment procedures, power should be applied to the drive for two hours; the cartridge should be mounted and spinning for at least one-half hour.

To WRITE LOCK the drive, set the SAFETY SWITCH (S2) on the RK06 M7729 board or the RK07 M7906 board to the MAINT position. This action will also prevent the heads from unloading if a Servo Unsafe condition occurs.

7. Mount the head alignment fixture on the appropriate head (Figures 4-10 and 4-11).

CAUTION

Make sure that the carriage does not tip beyond the point where the heads will fall out of the cam tower.

8. Torque the head alignment fixture mounting screw to 5 in/lb. Loosen the head mounting screw and then tighten it to 2 in/lb. Turn both vertical screws of the head alignment fixture fully CCW.
9. Select the desired head and load to the actual cylinder address that corresponds to the underlined (for an RK06 alignment) or dotted (for an RK07 alignment) cylinder address switches on the Field Test Box. Refer to the switch settings that follow.

Switch	Position
EXERCISE/STATUS	EXERCISE
DRIVE SELECT	Desired Drive#
COMMAND TO RK06/7 switches	SEEK 22 SECTORS CLEAR ERROR & ATTENTION SET VOLUME VALID
SINGLE CYCLE/CONTINUOUS	SINGLE CYCLE
FUNCTION	SEEK ONLY

Switch	Position
SYNC	INT
CLOCK	FAST
HALT ON ERROR	NO
ADDRESSING	
(CYLINDER)	SWR
(UNDERLINED SWITCHES)	245_{10} (for RK06)
(DOTTED SWITCHES)	496_{10} (for RK07)
(HEAD)	SWR
(HEAD ADDRESS SWITCHES)	DESIRED HEAD#
(SECTOR)	ALL
PARITY (both switches)	ODD

Depress the INIT and START switches.

To change heads, simply change the head address switch setting and depress the START switch.

10. Set the torque wrench to 5 in/lb. Tighten the forward vertical screw to move the head forward or the rear one to move the head to the rear. Since these screws oppose each other, the screw not in use must be fully CCW. Adjust until:

    a. The red LED on the meter is ON (steady state).
    b. The meter on the Field Test Box reads 0 ± 50 microinches.

    NOTE
    If the needle deflects to the right of zero, move the head toward spindle; if to the left of zero, move away from spindle.

11. Unload the heads.

12. Tighten the head to 5 in/lb.

13. Load the heads and check that the conditions of steps 10a and b are still met.

14. Unload the heads; remove the head alignment fixture and mount it on the next head.

15. Load the heads and repeat the procedures of steps 8 through 15 until all data heads are aligned.

4.4.5 Response to Abnormal Conditions

The following procedures are for handling abnormal conditions encountered during a system installation.

4.4.5.1 Clearing an Unsafe Condition – Clearing of an unsafe condition can be accomplished by releasing the RUN/STOP switch on the front panel. Press the RUN/STOP switch again. If the fault no longer exists, the FAULT light will go off. When the READY light is on, the drive is ready for further operations.

4.4.5.2 Removing a Cartridge When Drive Power is Lost – If power to the driver is lost and it is necessary to remove the disk cartridge, use the following procedure:

1. Insert a small, flat-blade screwdriver into the opening above the door latch.
2. While pushing on the screwdriver, lift the pack loading door.
3. Ensure that the brush drive knob is turned fully clockwise.
4. Ensure that the head loading arms are fully retracted.
5. Remove the disk cartridge in the usual manner.

4.4.5.3 Detecting Head-to-Disk Interference – The read/write heads actually fly over the disk surface at an altitude of approximately 50 millionths of an inch. When for any reason the read/write heads touch the disk surface (a condition referred to as "head crash"), damage to either heads or disk surface is possible. If there is an audible ticking sound after the heads load or if the heads show an oxide buildup on the gliding surface when inspected, a head crash has probably occurred. The following procedure should be followed for recovery from a head crash:

1. Clean the oxide buildup from the head, using a head cleaning kit.
2. Reinspect the head, using an inspection mirror. If any scratches or oxide are visible, the head must be replaced. Refer to the *RK06/RK07 Disk Subsystem Service Manual* for the appropriate procedure.
3. If a head shows no visible scratches or oxides, install a scratch pack and load the heads onto the pack as in the head load/unload checks.
4. When the drive is ready, cycle the drive down by setting the RUN/STOP switch and reinspect the heads in question. If any oxide buildup is present, a catastrophic condition exists. Refer to the *RK06/RK07 Disk Subsystem Service Manual* for corrective procedures.

CAUTION

Never use a cartridge involved in a head crash until it has been inspected and found usable; i.e., there are no visible marks on the platter surfaces. Catastrophic crashes can be propagated from drive-to-drive under such conditions.

Never use an alignment cartridge in a drive that has experienced a head crash. Always use a scratch cartridge for testing.

4.5 POWER CONVERSION

The RK611/RK06 or RK611/RK07 Disk Subsystem is configured during manufacture to be either a 50-Hz or 60-Hz unit. (See Paragraph 1.4.) Although it is possible to change the frequency characteristics of the drive in the field, this requires such parts substitution as the power supply transformer and spindle motor pulley, plus a belt change.

Changing of voltage range (120 Vac to 240 Vac or vice versa) merely requires a circuit breaker change (CB1 at the rear of the drive).

4.6 DUAL ACCESS DRIVE INSTALLATION AND ACCEPTANCE

4.6.1 Dual Access Installation Procedure

Site preparation and environmental considerations for the RK06 or RK07 dual access disk drive are the same as those for the single access drives and are discussed in Chapter 3 of this manual. The adjustment and installation procedures for the RK06 or RK07 dual access drive are also identical with those of the single access drive, except for the added cables for dual access. Refer to the single access installation procedures described earlier in this chapter. Figure 4-12 is a dual access cable diagram.

4.6.2 Dual Access Acceptance Procedure

4.6.2.1 Dual Access Diagnostic – The Dual Access diagnostic (DZR6GA.X) must be run first to establish that a port can seize and release the drive. To accomplish this, perform the following procedures:

1. On each drive to be tested, the dual access test switch located on module M7730 must be placed in the invert position for the duration of this test. Refer to Figure 4-2 or 4-3 for the location of this switch. When in the invert position, this switch grounds bit 0 of the port B unit select lines and causes each drive to appear as two separate units to the RK611. The unit select switch will define the address of port A. Port B address will respond to the address of A + 1. Since each drive will appear as two units to the RK611, a maximum of four drives can be tested by this program at one time.

2. Use only even numbered UNIT SELECT SWITCHes on the drive operator panel. Any other drives on the system which have an address in conflict with any of the test addresses must be deselected (both ports switched off). The even numbered UNIT SELECT SWITCH on any drive can be removed and inserted into the current drive under test.

3. For this test, the RK611 is daisy chained to both ports of the RK06 or RK07. Refer to Figure 4-13 for the cable diagram.

4. Run the Dual Access diagnostic (DZR6G.X) to test dual access seizure and release.

5. After running the Dual Access diagnostics, return the dual port invert switch on module M7730 to its normal position. Return any UNIT SELECT SWITCHes borrowed for this test to their former drives.

6. Recable the RK06 or RK07 Drives for normal operation, as shown in Figure 4-12.

4.6.2.2 RK611, RK06, and RK07 Diagnostics – With the drives cabled for normal operation, run all RK611, RK06, and RK07 diagnostics through *both* ports.

4.6.2.3 RK06 and RK07 Performance Exerciser – To run the RK06 and RK07 Performance Exerciser (DZR6P.X), all disks must first be written with a predetermined data pattern through one of the systems. This is accomplished by starting the Performance Exerciser at address 200. The exerciser will automatically write all disks on the drive bus and begin testing data transfers immediately, without operator intervention. While the first system is undergoing testing, the second system can be entered into the performance tests by starting the exerciser at address 240. This will skip over the disk write portion of the test and allow the operator to manually begin the performance tests on the second system. Both systems will then be undergoing performance testing simultaneously.

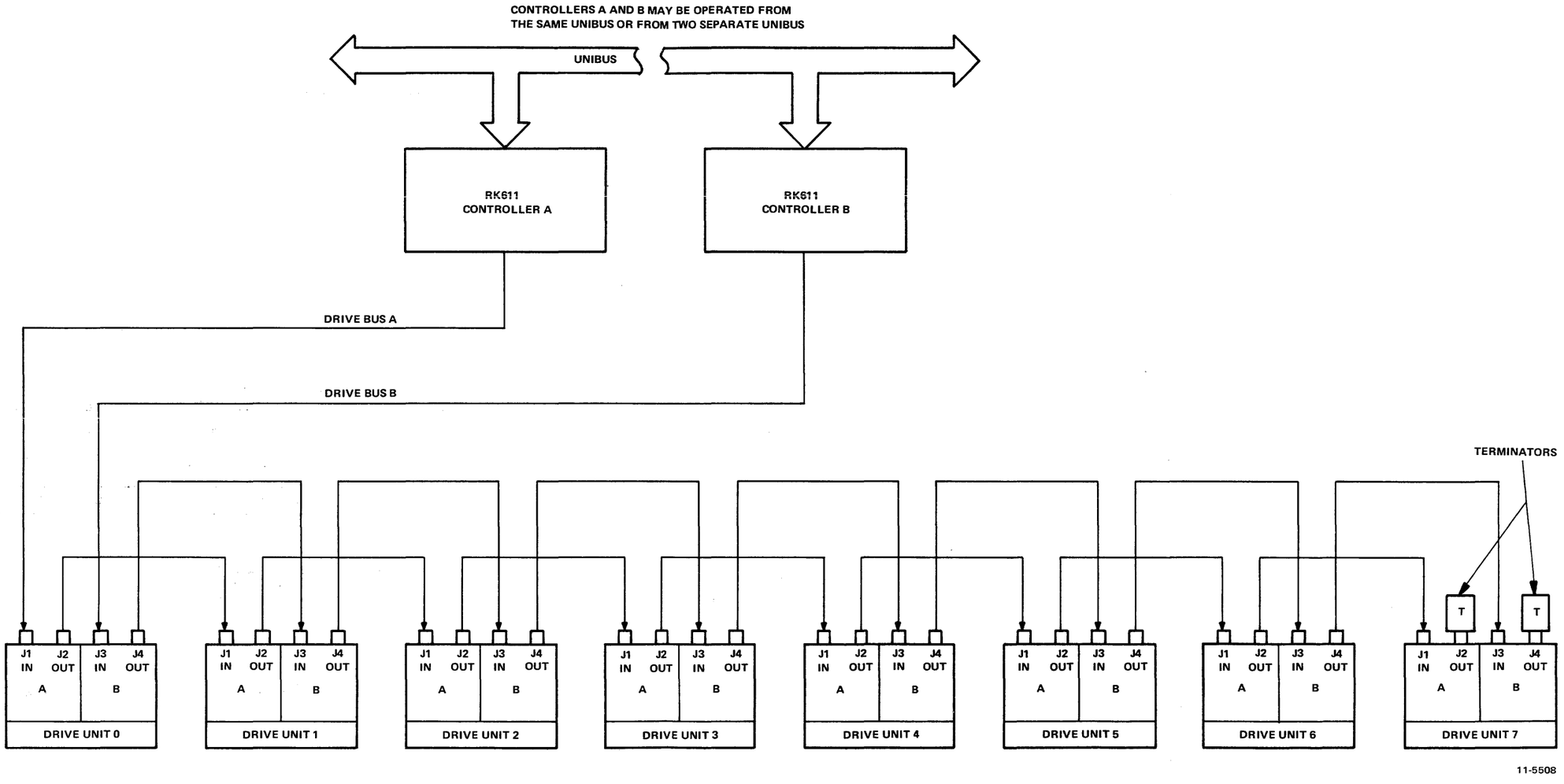


Figure 4-12 RK611/RK06 or RK611/RK07
Dual Access Cable Diagram

CHAPTER 5
FIELD ACCEPTANCE TEST PROCEDURE

Field acceptance testing is intended to demonstrate performance of the RK06 or RK07 Disk Drive and/or the RK611 Controller to the customer prior to his acceptance of the equipment.

5.1 ERROR DEFINITIONS/RATES

The RK611 has five registers that display the various error conditions that can exist in the Disk subsystem. Table 5-1 lists the various error indications and gives an explanation of their significance. Errors are broken down into five categories:

1. Control
2. Cartridge
3. Seek
4. Hard errors
5. Soft errors

These classifications aid in the identification of the various errors encountered in acceptance testing only.

5.1.1 Control Errors

A control error indicates an operational aberration in the execution of command and control functions. Any control error detected by a diagnostic program during acceptance testing indicates a hardware malfunction that must be corrected before testing can continue.

Table 5-1 RK611/RK06 and RK611/RK07 Disk Subsystem Diagnostic Errors

Error	Indicator Bit	Condition	Error Type
Programming Error (PGE)	RKCS2 bit 10	Register written (except CCLR, SCLR) with GO set.	Control
Illegal Function (ILF)	RKER bit 0	Illegal command in low-order 5 bits of RKCS1.	Control
Format Error (FPER)	RKER bit 4 or 5	Format or drive type error.	Control
Cylinder Overflow (COE)	RKER bit 9	Cylinder address exceeded.	Control
Invalid Disk Address (IDAE)	RKER bit 10	Invalid cylinder or track address detected.	Control
Unit Field Error (UFE)	RKCS2 bit 8	Drive selection problem.	Control

Table 5-1 RK611/RK06 or RK611/RK07 Disk Subsystem Diagnostic Errors (Cont)

Error	Indicator	Bit Condition	Error Type
Unibus Parity Error (UPE)	RKCS2 bit 13	Error in 16-bit data word from main memory.	Control
Nonexistent Drive (NED)	RKCS2 bit 12	Drive response problem.	Control
Drive Available Interrupt (DAINT)	RKDS bit 0	Drive is not available (dual-access only).	Control
Drive Error (DRERR)	Message BO:T (FAULT)	Any 1 of 21 drive error conditions.	Control
Bad Sector Error (BSERR)	RKER bit 7	Data transfer attempt to/from bad sector.	Cartridge
Header VRC Error (HVRC)	RKER bit 8	Header check, indicates bad header information.	Hard/Soft
Operation Incomplete (OPI)	RKER bit 13	Desired header cannot be found.	Seek
DTC Parity Error (DTC PAR)	RKCS1 bit 13	Parity error in message from drive.	Control
Write Check Error (WCE)	RKCS2 bit 14	Write check, indicates data from disk did not match data from memory.	Hard/Soft
Nonexistent Memory (NEM)	RKCS2 bit 11	No SSYN within 10 μs of MSYN assertion.	Control
Data Late Error (DLTERR)	RKCS2 bit 15	Data late to/from silo.	Control
Drive Timing Error (DTE)	RKER bit 12	Write clock loss during write; data loss during read.	Control
Data Check (DCK)	RKER bit 15	Data error detected by ECC.	Soft
Multiple Drive Select (MDS)	RKCS2 bit 9	More than one drive simultaneously selected.	Control
Error Correction Hard (ECH)	RKER bit 6	Data error uncorrectable using ECC.	Hard
Controller Time-Out (CTO)	RKCS1 bit 11	Command possibly not executed.	Control
Seek Incomplete (SKI)	RXER Bit 1	Seek operation did not complete.	Seek

5.1.2 Hard Errors
Any failure to read data correctly after a complete recovery sequence[1] with ECC enabled constitutes an irrecoverable, i.e., "hard" error. Errors that are not ECC-correctable include: (1) bursts greater than 11 bits in length and, (2) isolated dropped bits that are separated by more than 11 bits within a sector. The allowable error rate for hard errors is one error per 10^{12} bits read.

5.1.3 Soft Errors
A soft error is defined as any read error that is correctable by ECC and/or a complete recovery sequence. The allowable error rate for soft errors is one error per 10^9 bits read.

5.1.4 Cartridge Errors
A cartridge error caused by imperfections in the recording surface is regarded as cartridge-attributable or media-dependent. If the imperfection is less than 11 bits long, it is ECC-correctable and will appear as a soft error. If longer than 11 bits, it will appear as a hard error. On a given cartridge, attributable errors will always appear at the same cylinder, sector, and track addresses. The definitions of hard and soft errors (see 5.1.2 and 5.1.3) apply only to randomly distributed errors and do not take into account errors that are cartridge-attributable. Imperfections in the cartridge surface may be found by mapping the cartridge by means of the formatter program.

5.1.5 Seek Errors
Any positioning operation that terminates with seek incomplete, or with the positioner in an incorrect location, constitutes a seek error. The allowable error rate for seek errors is one error per 10^6 seek operations.

5.2 DIAGNOSTIC TESTING
When all installation procedures have been completed, the tests detailed in the following subsections should be performed. Table 5-2 briefly describes the diagnostic programs used in field acceptance testing of the RK611/RK06 or RK611/RK07 Disk subsystem. The total time required to run these tests (except DZR6Q[2]) in the absence of failures is 2.5 hours per drive.

5.2.1 RK611 Controller

5.2.1.1 General – In diagnostic testing, the RK611 is tested first. All five of the diskless controller diagnostics (Table 5-2, DZR6A-DZR6E) and the RK611 functional controller diagnostic (DZR6K in the Table) must run for two error-free passes before the remainder of the acceptance program can be carried out. Any failure detected by any of the diagnostics must be corrected, and all programs must be rerun before proceeding.

---

[1]A complete recovery sequence consists of 28 retries, 16 of which are at the nominal head position and 2 each at offsets of ±400, ±800, and ±1200 microinches (for the RK06) or ±200, ±400 and ±600 microinches (for the RK07), respectively.

[2]The run time of this diagnostic depends on the number of drives being tested.

Table 5-2 Diagnostic Programs Used in RK611/RK06 or RK611/RK07 Disk Subsystem Field Acceptance Tests

Program	Function
MAINDEC-11-DZR6A RK611 Diskless Controller Diagnostic Part 1	Reads and writes every RK611 register. Tests the interrupt mechanism. Tests the SILO loading logic. (Note: No drive is required for the execution of this program.)
MAINDEC-11-DZR6B RK611 Diskless Controller Diagnostic, Part 2	Tests the loading of drive bus messages by executing Class A commands. Some Part 1 tests execute commands that are partially maintenance mode and partially at normal speed in order to "fool" the controller and force errors (no drive is required).
MAINDEC-11-DZR6C RK611 Diskless Controller Diagnostic Part 3	Tests the loading of the drive bus message shift register for Class B commands. Tests index and sector pulse detection. Tests SILO and NPR transfers from memory in 16- and 18-bit mode. Tests nonexistent memory and Unibus parity error detection. Tests Read and Write MFM loopback. Tests Class B instruction errors (no drive is required).
MAINDEC-11-DZR6D RK611 Diskless Controller Diagnostic Part 4	Tests loading of drive bus message shift registers for Class C commands. Tests header generation for search operations. Tests write data NPR transfers to SILO. Tests header recognition. Tests cylinder, track, and sector increment after successful header search. Tests detection of all header-type errors. Tests ECC generation and writing. Tests partial sector write (zero fill). Tests 18-bit format ECC generation and data write (no drive is required).

Table 5-2 Diagnostic Programs Used in RK611/RK06 or RK611 or RK611/RK07 Disk Subsystem Field Acceptance Tests (Cont)

Program	Function
MAINDEC-11-DZR6E RK611 Diskless Controller Diagnostic Part 5	Tests multisector data transfers. Tests midtransfer seeks. Tests cylinder overflow checking. Tests NPR transfers to memory. Tests ECC error detection and correction in 16-and 18-bit modes. Tests write check in both 16- and 18-bit modes and forces.
MAINDEC-11-DZR6G Unibus RK06-RK07 Dual Port Drive Diagnostic (available Q4, FY78)	Tests write check errors (no drive is required). Ensures that port request, port seize, and timeout function correctly. Ensures that the release function operates correctly. Ensures that the timer inhibiting logic operates correctly. Ensures that data transfers function correctly through both parts.
MAINDEC-11-DZR6H Unibus RK06-RK07 Drive Diagnostic Part 1	Ensures that the drive can perform all static and cycle-up tests. Ensures that the drive can write and read headers in both 20- and 22-sector formats. Ensures that the disk can perform seek operations by doing several seek patterns. Checks error-detection logic by software error forcing.
MAINDEC-11-DZR6I Unibus RK06-RK07 Drive Diagnostic, Part 2	Ensures that the disk is capable of performing read and write data operations in both 20- and 22-sector formats. Performs worst case patterns, spiral writing and reading, and all offset operations. Reports unloading and loading times.

Table 5-2 Diagnostic Programs Used in RK611/RK06 or RK611/RK07 Disk Subsystem Field Acceptance Tests (Cont)

Program	Function
MAINDEC-11-DZR6J Unibus RK06-RK07 Drive Diagnostic, Part 3	Ensures that the disk is capable of performing all operator intervention functions properly. Checks error-detection logic by manual and by software forcing of errors.
MAINDEC-11-DZR6K RK611 Functional Controller Diagnostic	Tests those areas in the controller that cannot be tested in a diskless environment. Tests those areas of the drive that cannot be tested until controller operation in a diagnostic or maintenance mode has been tested.
MAINDEC-11-DZR6L RK06K-RK07K Cartridge Formatter	Writes and verifies header and data information on an RK06K or RK07K disk pack at all possible disk pack addresses. Uses the Bad Sector File to: (1) report the serial number or the cartridge being formatted, (2) determine whether the cartridge is an alignment cartridge, and abort the program if it is, and (3) identify the sectors that are to be marked "bad."
MAINDEC-11-DZR6M RK611/RK06-RK611/RK07 Subsystem Verification, Part 1	Provides a functional shakedown of the entire subsystem, including the Unibus interface and access to main memory. Employs worst case situations involving mechanical positioning, disk addressing, and data transfer. Measures drive operational timing. Provides numerous options that may be specified by the user. Reports errors as they occur.
MAINDEC-11-DZR6N RK611/RK06-RK611/RK07 Subsystem Verification, Part 2	Continues functional shakedown provided by Part 1. Employs worst case situations involving head offsetting, memory addressing and data transfer, Unibus cycle contention, and multiple-drive operations. Provides RK06 or RK07 head-alignment aid. Provides numerous options that may be specified by the user.

Table 5-2 Diagnostic Programs Used in RK611/RK06 or RK611/RK07 Disk Subsystem Field Acceptance Tests (Cont)

Program	Function
MAINDEC-11-DZR6P RK611/RK06-RK611/RK07 Performance Exerciser	Exercises in a random overlapped routine from one to eight RK06 or RK07 Drives connected to a common Unibus controller in a dedicated stand-alone mode. Generates read, write, and write/write check commands. Reports system errors upon occurrence. Maintains performance statistics on each drive.
MAINDEC-11-DZR6Q RK06-RK07 Drive Compatibility	Verifies the capability of each drive to write data that can be successfully read by all other drives and to completely overwrite data written by all other drives. Detects: (1) head misalignment, (2) positioner lateral misalignment, (3) spindle/cartridge interface runout, (4) improper levels of write current, and (5) incorrect addressing of read/write heads. Prints summary of compatibility test results for each drive. Reports unexpected errors as they occur.
MAINDEC-11-DZR6R RK611/RK06-RK611/RK07 User Defined Test	Provides a capability for entering, editing, saving, recalling, and executing test programs designed by the user. Provides an interactive command set for use in entering, storing, retrieving, editing, and executing tests.

5.2.1.2 Procedure

NOTE

In the following steps, repair or replace the failing module; rerun the program that detected the failure; then return to step 1.

1. Load diagnostic DZR6A; run two passes with no errors.
2. Load DZR6B; run two passes with no errors.
3. Load DZR6C; run two passes with no errors.
4. Load DZR6D; run two passes with no errors.

5. Load DZR6E; run two passes with no errors.

6. Load DZR6K; run two passes with no errors.

NOTE

Any failures occurring during program DZR6K may not necessarily be limited to the RK611 Controller. Thus, it should only be run on a known good drive.

CAUTION

Diagnostic program DZR6K modifies headers on certain tracks. Failure to halt the program, either during the "End of Pass" printout or by typing CTRL C may leave the pack formatted incorrectly and cause inaccurate error reporting in subsequent testing. If the formatting is left modified, the RK06K/RK07K Cartridge Formatter Program (DZR6L) must be run (using Mode 1) before any further testing can be performed.

At this point in the testing, the RK611 is functionally checked out. The only RK611 test not performed at this time is the Data Reliability Test.

5.2.2 RK06 or RK07 Disk Drive

5.2.2.1 General - This section of the diagnostic procedure covers the testing of the RK06 or RK07 Drive. With a high degree of confidence, any failures detected in these tests can be attributed to the Drive only. All programs listed in Paragraph 5.2.2.2 must run through the specified number of error-free passes before performing the remainder of the program. Any failure detected by any of the diagnostics in this section must be corrected and all programs rerun before proceeding.

5.2.2.2 Procedure

NOTE

In the following steps, repair or replace any failing component; rerun the program that detected the failure to verify the correction; then return to step 1.

1. Load diagnostic DZR6H; run two passes with no errors.

2. Load DZR6I; run two passes with no errors.

3. Load DZR6J; run one pass with no errors.

4. Load DZR6M; run one pass with no parameters out of the specified limits (printed by the diagnostic).

5. Load DZR6N; run two passes with no errors.

6. Load DZR6G; run two passes with no errors.

5.2.3 Cartridge Interchangeability Test

This test requires the use of at least two drives. If there is only one drive on the system being tested, it will be necessary to use another system containing an RK06 or RK07 to complete this test.

Load and run diagnostic DZR6Q. If any drive fails this test, make any necessary adjustments and rerun the program.

5.2.4 Data Reliability Testing

5.2.4.1 General – Data reliability testing consists of running diagnostic DZR6P to exercise the entire RK611/RK06 or RK611/RK07 Disk subsystem for at least one hour. At the end of this period, the statistics for each drive must be analyzed to determine whether or not the subsystem is to be accepted.

In analyzing the statistics for each drive, no control, seek, or hard errors are allowed during the testing. Refer to Paragraph 5.1 for error definitions. The occurrence of any of these errors is sufficient to reject a drive. If it is determined that an error is due to the cartridge, it is sufficient to reformat the cartridge, making sure that the failing sector is flagged bad. The Data Reliability Test may then be rerun.

If the excessive errors are caused by the drive, required corrective action must be performed and the acceptance restarted with the RK06 or RK07 diagnostic (Paragraph 5.2.2). If the errors are caused by the controller, the acceptance must be restarted with the RK611 diagnostic testing (Paragraph 5.2.1) after the corrective action has been taken.

5.2.4.2 Procedure – Load and start diagnostic DZR6P. Write the cartridge on all drives on the subsystem. After one hour of running, obtain the statistics for all drives. If the total number for all drives of "WORDS READ*65K" is less than 967, allow the subsystem to run for an additional 15 minutes and again obtain the statistics. Repeat until the total "WORDS READ*65K" is greater than 967. If the total number of SOFT DATA ERRORS is zero or one, accept the subsystem. If it is three or more, the failing component (drive or controller) must be fixed. If there were two SOFT DATA ERRORS, continue running the subsystem for an additional hour. At this point, obtain statistics and continue running until the total "WORDS READ*65K" is greater than 1934. If the total SOFT DATA ERRORS is still two, accept the subsystem. If the total is three or more, the failing component (drive or controller) must be fixed and acceptance restarted.

CHAPTER 6
OPERATOR'S GUIDE

6.1 INTRODUCTION

The following material describes the function of each of the external controls available to the user of an RK06 or RK07 Disk Drive and provides procedural information for subsystem operation.

6.2 OPERATOR CONTROLS/INDICATORS

The RK06 or RK07 Disk Drive contains the following power and control switches and indicators (Figure 6-1).

Rear Panel (Circuit Breaker):

- AC power ON/OFF switch with POWER indicator.

Front Panel (Control Panel):

- Combination RUN/STOP switch with a STOP indicator.
- UNIT SELECT switch with a READY indicator.
- FAULT indicator.
- WRITE PROT switch with a PROTECT indicator.
- ACCESS A ENABLE switch with a SELECT A indicator.
- ACCESS B ENABLE switch with a SELECT B indicator.

6.2.1 Power ON/OFF Circuit Breaker

When the three-wire plug is inserted into an outlet, ac power is applied to the rear panel circuit breaker on an RK06 or RK07 Disk Drive, and the red indicator lamp is illuminated. When the circuit breaker is switched to the ON position, ac power is applied to the drive and the blower motor is energized.

6.2.2 RUN/STOP Switch with STOP Indicator

The STOP indicator is illuminated during STOP conditions when the heads and brushes are home, the spindle is completely stopped, and the spindle motor is not energized. When the alternating action pushbutton is initially pressed (RUN) under these conditions, the spindle motor is energized, the STOP indicator is extinguished, and the heads are loaded. When these initial operational conditions are met (STOP indicator extinguished and heads loading), a RUN condition is entered. However, if the heads do not load (due to a malfunction), the spindle motor is immediately de-energized and the STOP indicator remains illuminated.

If the pushbutton is released (STOP) when the heads are loaded, the heads will be unloaded and the spindle motor de-energized. When these conditions are met (heads home and spindle stopped), the STOP indicator is again illuminated.

If the RUN/STOP switch is in the RUN position and the drive has been cycled down (heads unloaded and spindle completely stopped) due to an Unload command, a Start Spindle command from the controller can be used to restart the spindle and reload the heads. However, if the cycle down condition occurred as the result of an error, a Start Spindle command is not required, since the heads will immediately load when the error is cleared.

Finally, since the RUN/STOP switch has a mechanical memory, a power interrupt followed by power restoration will cause the drive to automatically cycle up if the switch is currently located in the RUN position.

NOTE

The drive cover (lid) is interlocked. This prevents the lid from being raised when the STOP light is extinguished (RUN) or drive power is off.

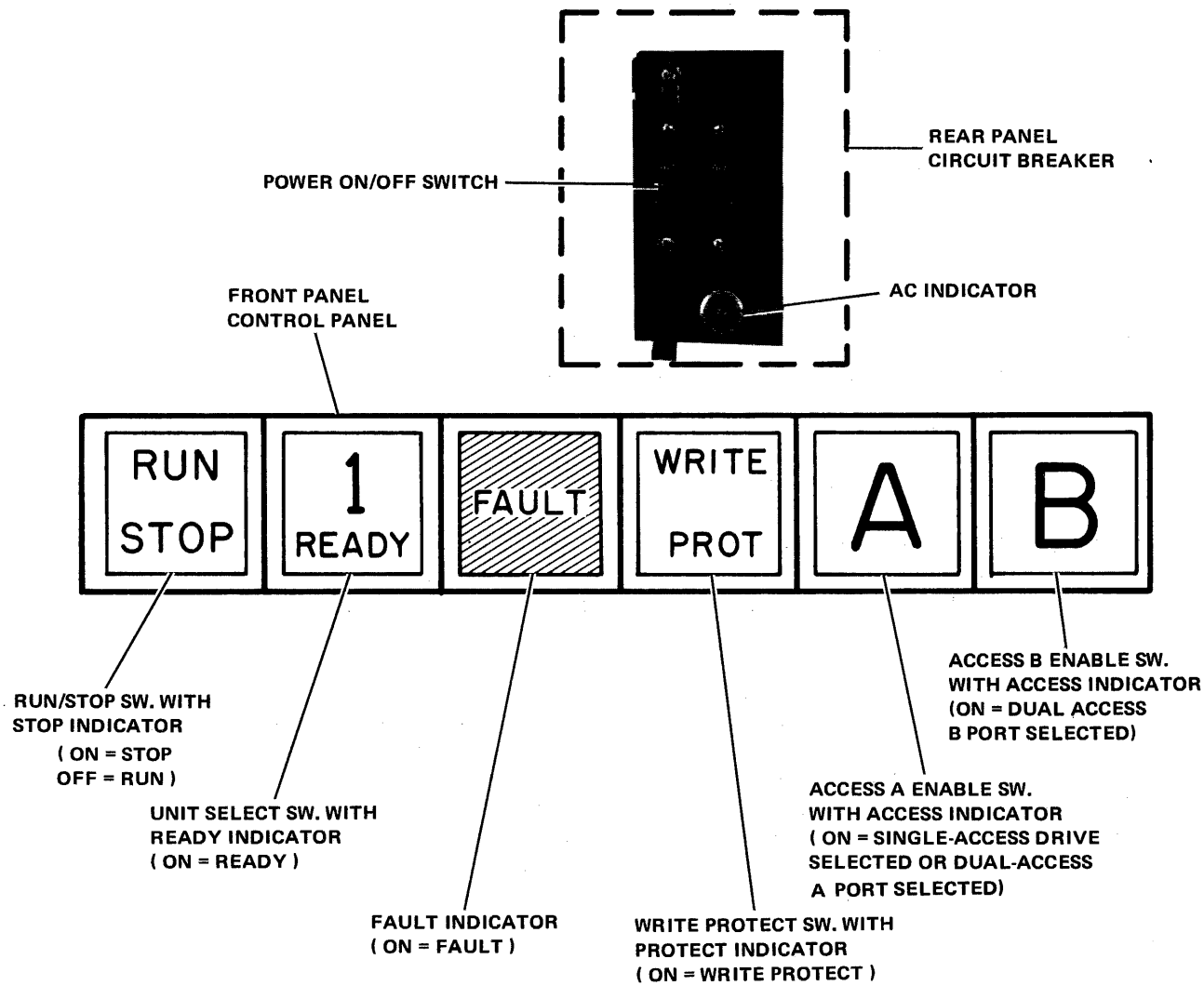


Figure 6-1 RK06 or RK07 Disk Drive Power and Control Switches

6.2.3 UNIT SELECT Switch with READY Indicator

The UNIT SELECT switch is a cam-operated assembly that is actuated by the insertion of a plastic plug. The face side of each actuator plug contains a single number (0-7), while the other side consists of raised plastic cam actuators that are separately configured to encode the plug with the number. With this arrangement, the insertion of a plug into any UNIT SELECT switch assembly will automatically encode the associated plug number when power is applied to the drive. When the heads of a drive are settled (not in motion), the numbered indicator on the UNIT SELECT switch assembly associated with the drive is illuminated (READY).

6.2.4 FAULT Indicator

The FAULT indicator is illuminated whenever one of the following error conditions is detected in the drive:

- More than one drive selected.
- Positioner, when detented, has moved too far (e.g., the drive has been jarred).
- A parity error has occurred in a message transmitted from the controller to the drive.
- A read/write unsafe condition in the drive (e.g., serve track error signals, write gate signal errors, etc.)
- A write lock error condition (i.e., the receipt of a Write Gate signal when the drive is in Write Protect mode).
- Low ac voltage in the drive.
- An incomplete Seek operation.
- The receipt of Write Gate or Seek signals while Volume Valid is reset.

6.2.5 WRITE PROT Switch with PROTECT Indicator

If a Write Gate signal from the controller is not currently asserted in a selected drive, initial depression of the WRITE PROT pushbutton will immediately set the drive in Write Protect mode, and the PROTECT indicator will be illuminated. When the alternating action pushbutton is again pressed, write protection is removed and the PROTECT indicator is extinguished. However, if a Write Gate signal is asserted in the selected drive when the switch is initially pressed, write protection will be inhibited and the PROTECT indicator will remain extinguished until the Write Gate signal is negated. Once the Write Gate signal is negated, the Write Protect mode is entered and the PROTECT indicator is illuminated.

6.2.6 ACCESS A ENABLE Switch with SELECT Indicator

The ACCESS A ENABLE switch is an alternating action pushbutton that is found on both single-access drives (Access A or Access B) and drives containing the dual-access option (Port A and Port B).

6.2.6.1 Single-Access Drive (A) – If Port A is configured for single access (i.e., the M7706 Interface and Timing Module is in Slot 3 of the drive card cage) and the switch is initially depressed, bidirectional communication with the controller is enabled via Port A. Under these conditions, when the drive is selected by the controller, the SELECT A indicator is illuminated. When the switch is again depressed (released), access by the controller is disabled and the SELECT A lamp cannot be illuminated.

6.2.7 ACCESS B ENABLE Switch with SELECT Indicator

The ACCESS B ENABLE switch is an alternating action pushbutton that is found on both single-access drives (Port A or Port B) and drives containing the dual-access option (Port A and B).

6.2.7.1 Single-Access Drive (B) – If the B port is configured for single access (i.e., the M7706 Interface and Timing module is in Slot 2 of the drive card cage) and the switch is initially pressed, bidirectional communication with the controller is enabled via Port B. Under these conditions, when the drive is selected by the controller, the SELECT B indicator is illuminated. When the switch is again pressed (released), access by the controller is disabled and the SELECT B lamp cannot be illuminated.

6.2.7.2 Dual-Access Drive (A and B) – If the ACCESS B ENABLE switch is independently pressed on a dual-access drive, the operations performed are similar to those previously described. However, if both the ACCESS B and ACCESS A switches are initially pressed, arbitration logic will determine, on a priority basis, which port (B or A) will be accessed by its associated controller (B or A).

6.3 OPERATING PROCEDURES

This material describes RK06K and RK07K Cartridge loading and cycle-up procedures that are required to place an RK06 or an RK07 Disk Drive on-line. The procedure assumes that ac power is available (red indicator lamp on the rear panel circuit breaker is on), the ac circuit breaker is on (blower motor is energized), and the STOP indicator lamp is illuminated on the control panel. If these conditions are met, initiate the following.

NOTE

An RK06K Cartridge may not be used on an RK07 Drive, and an RK07K Cartridge may not be used on an RK06 Drive.

6.3.1 RK06K and RK07K Cartridge Loading

1. Depress the drive lid release bar and raise the lid (Figure 6-2).
2. Prepare an RK06K or an RK07K Cartridge (Figure 6-3) for loading as follows:
   a. Lift the cartridge by grasping the top cover handle with the right hand (Figure 6-4).
   b. Support the cartridge with the left hand by holding the protection cover handle (Figure 6-5).
   c. Lower the top cover handle and push the handle slide to the left with the thumb of the right hand. Again raise the handle to its full upright position to release the protection cover (Figures 6-4 and 6-5).
3. Lift the cartridge from the protection cover and place it in the drive shroud with the top cover handle recess facing the rear of the machine (Figure 6-6).
4. Rotate the top cover handle a few degrees clockwise and counterclockwise to ensure that the shroud locating studs are properly seated within the cartridge housing detent slots.
5. Gently lower the top cover handle to a horizontal position to engage the drive spindle, and place the protection cover over the top cover (Figures 6-7 and 6-8).
6. Close the lid.

7. Depress one or both of the ACCESS A and B ENABLE switches, depending on the port capability.

8. If write protection is required, press the WRITE PROT switch.

9. Press the RUN/STOP switch (RUN). If the lid is properly closed and no drive errors exist (FAULT extinguished), the spindle will turn and the STOP indicator will be extinguished in approximately one second.

When the drive has completed the start spindle sequence and the heads are detented on Cylinder 0, the READY indicator on the numbered UNIT SELECT switch will be illuminated.

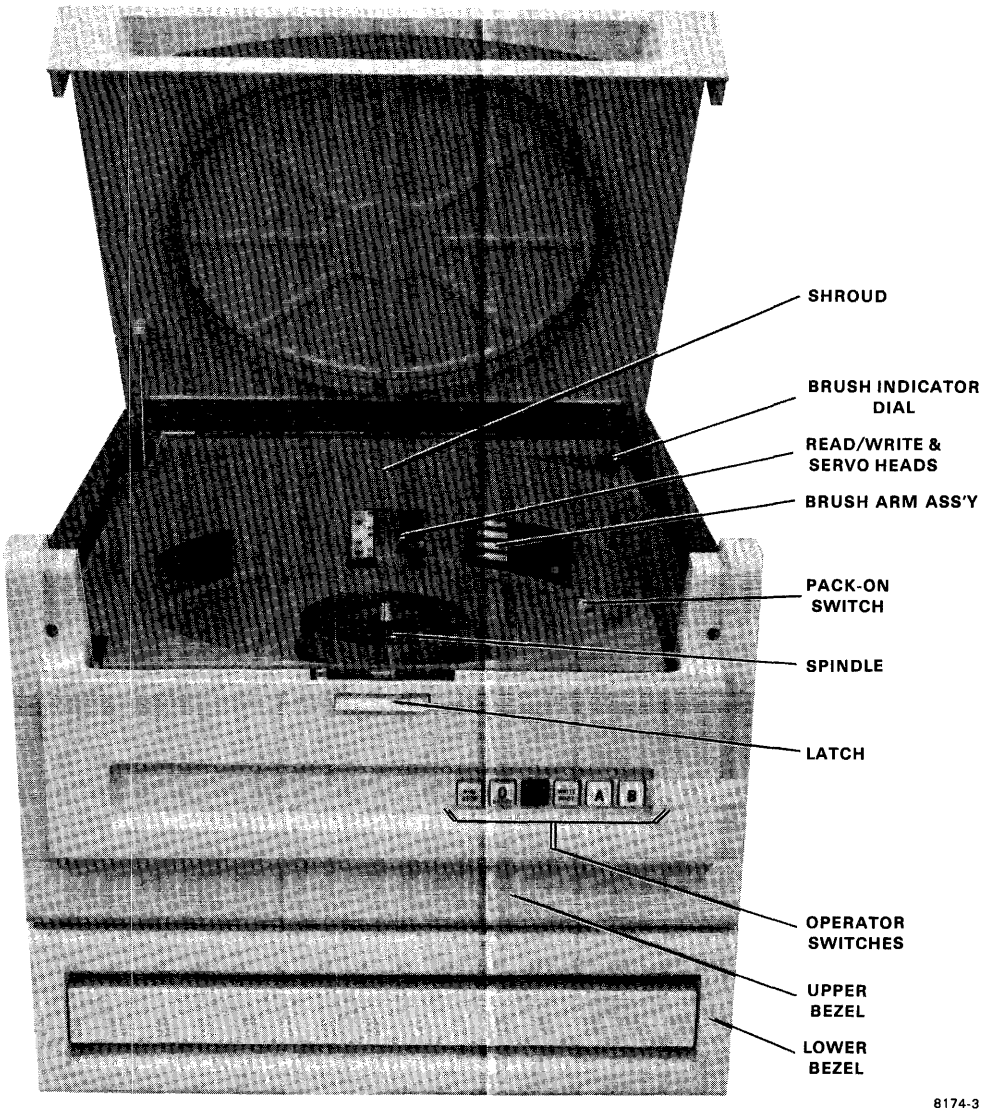


Figure 6-2 Typical Disk Drive with Lid Released

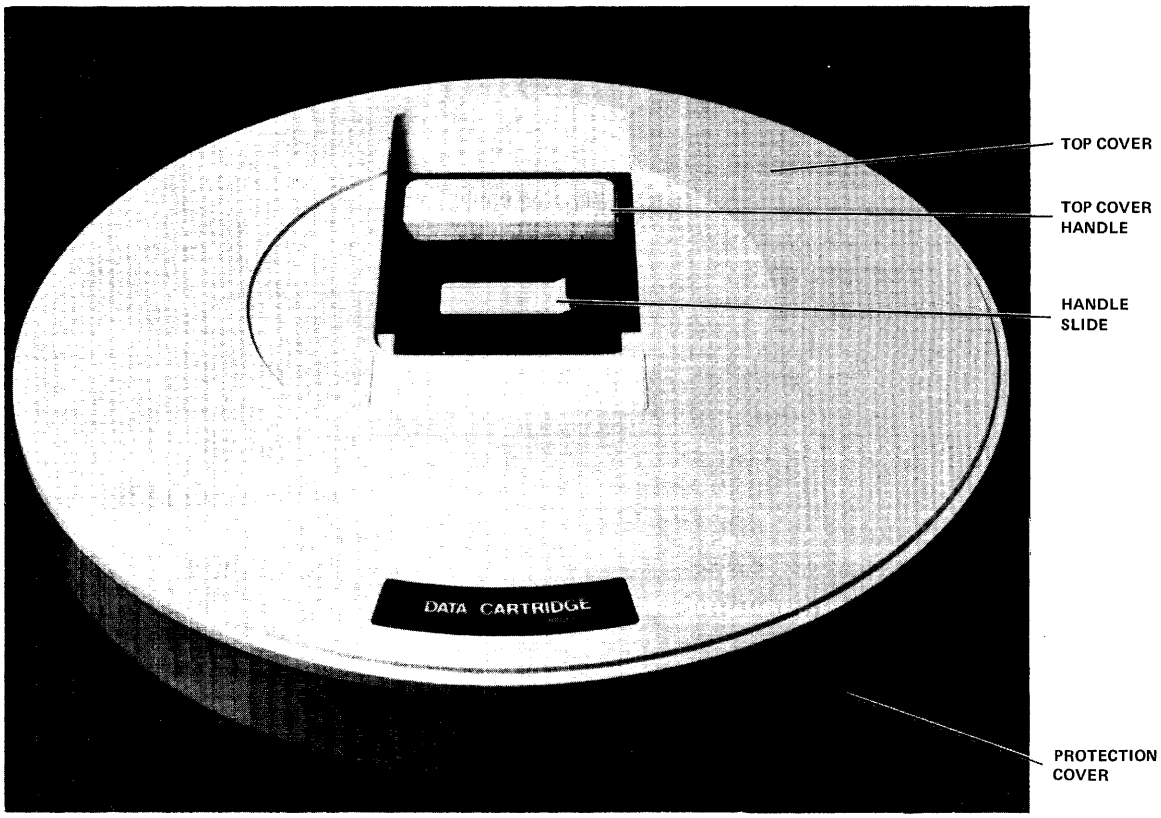


Figure 6-3 Typical Disk Cartridge

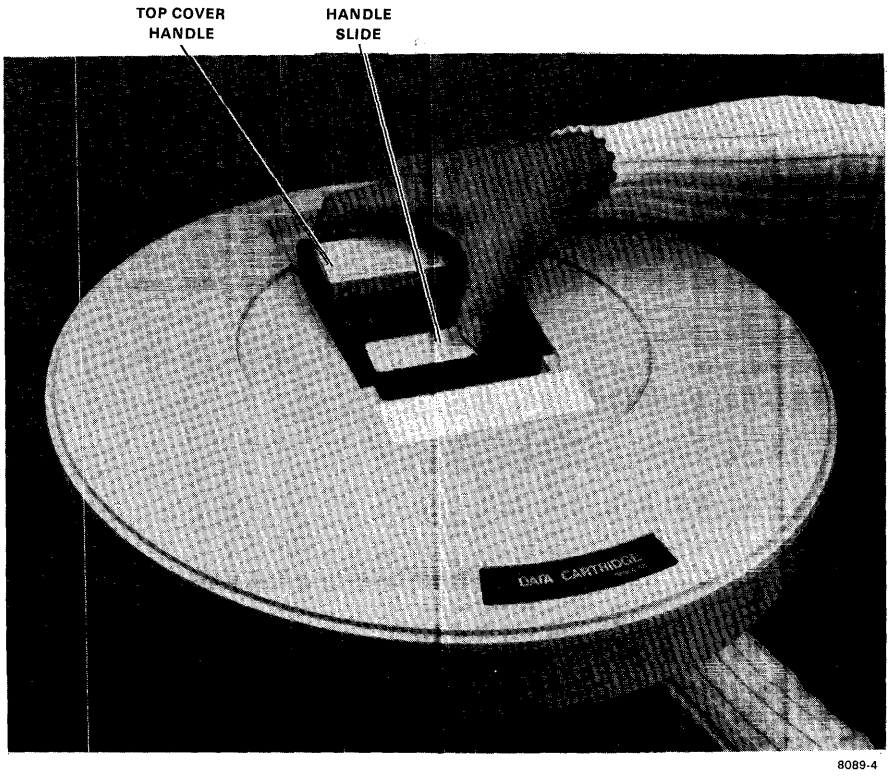


Figure 6-4 Engaging Lock Release

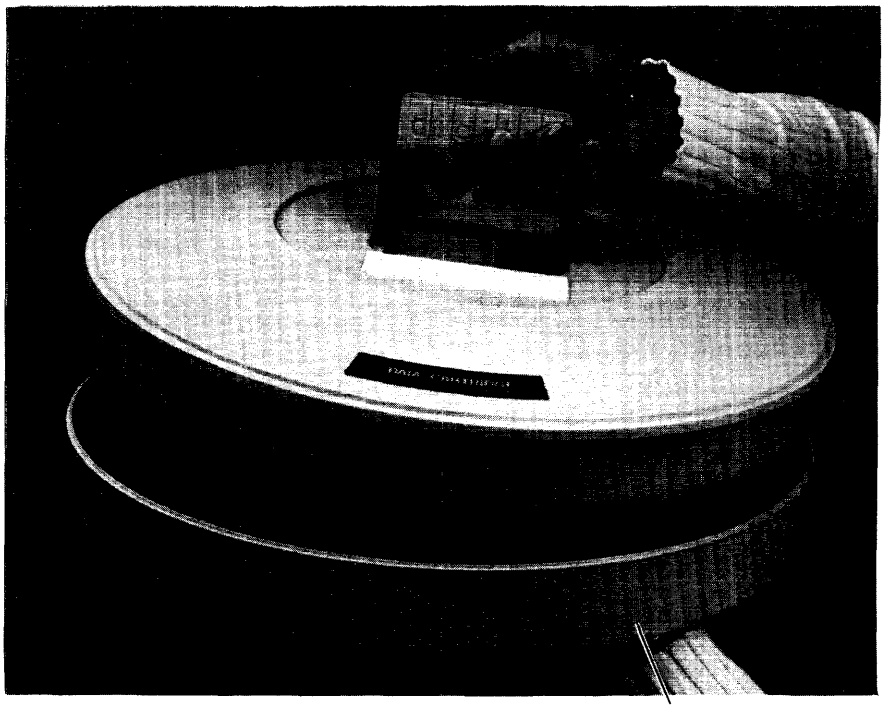


Figure 6-5 Releasing Protection Cover

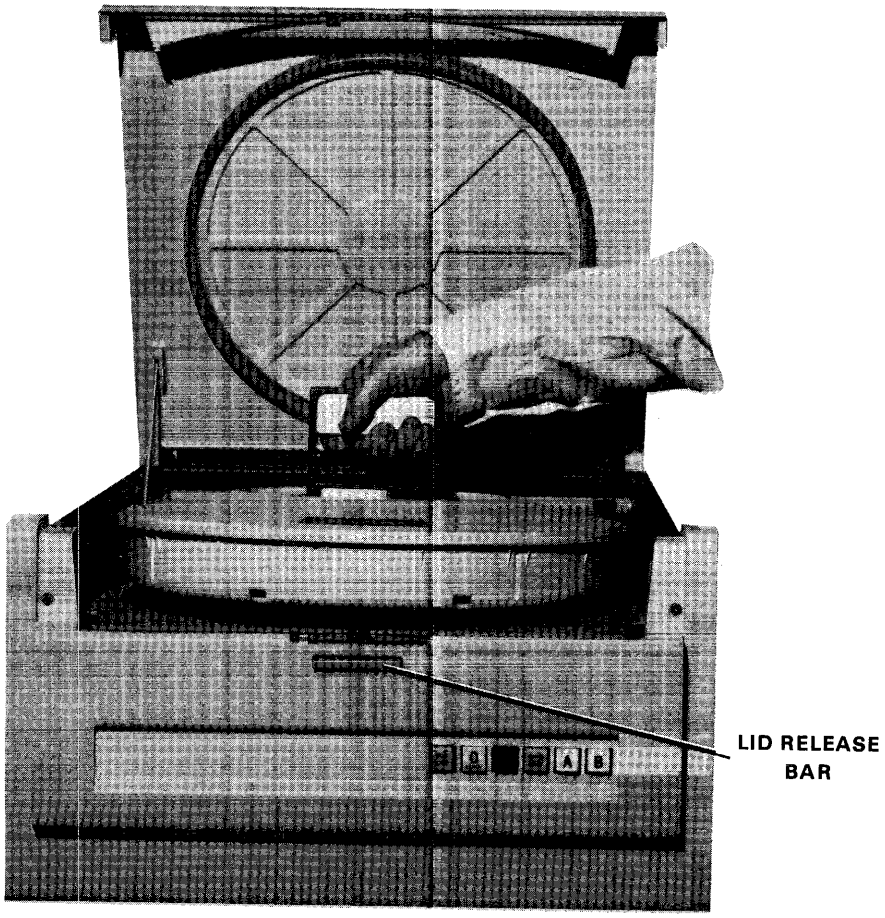


Figure 6-6 Positioning for Load

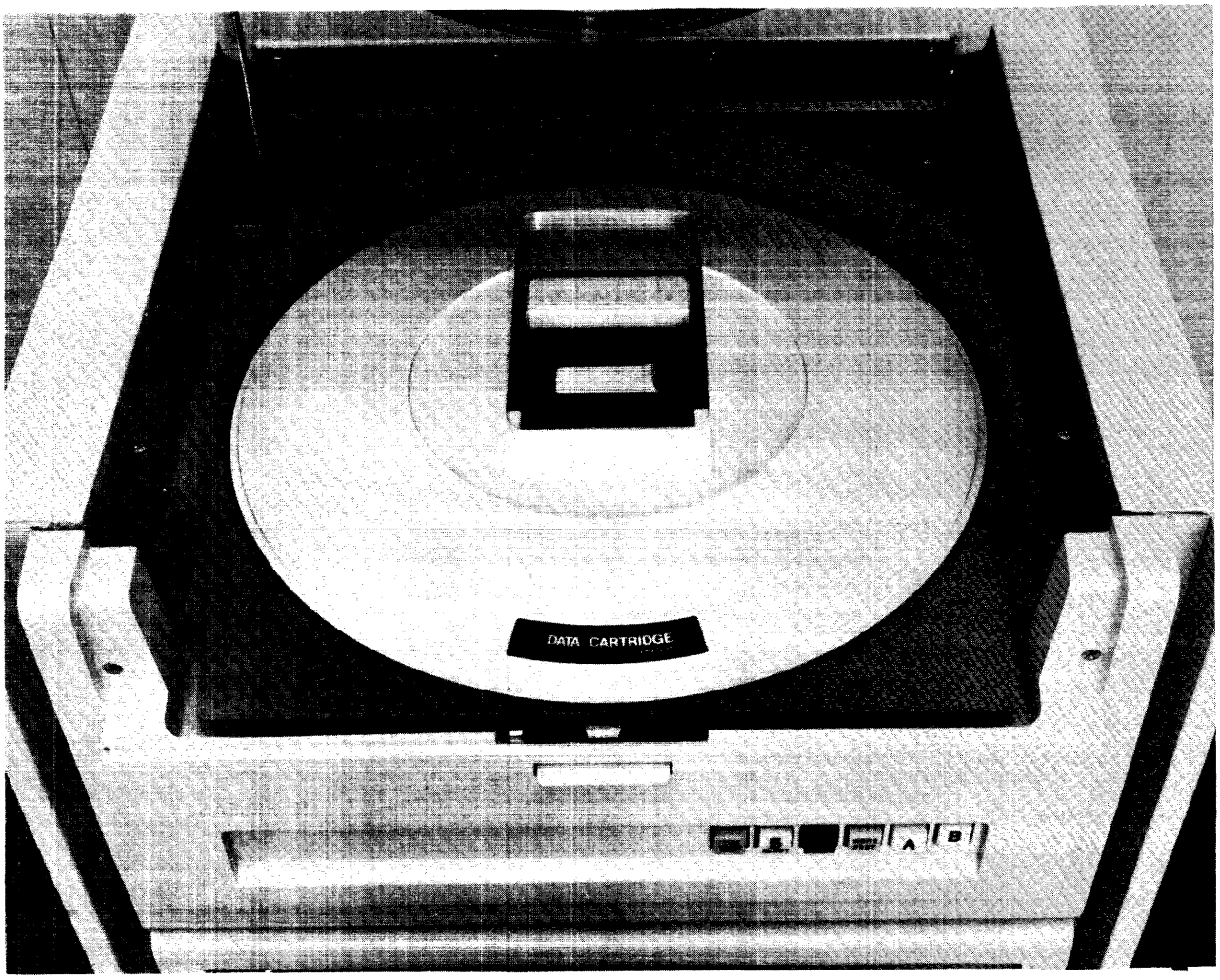


Figure 6-7 Cartridge Locked in Shroud 8089-1

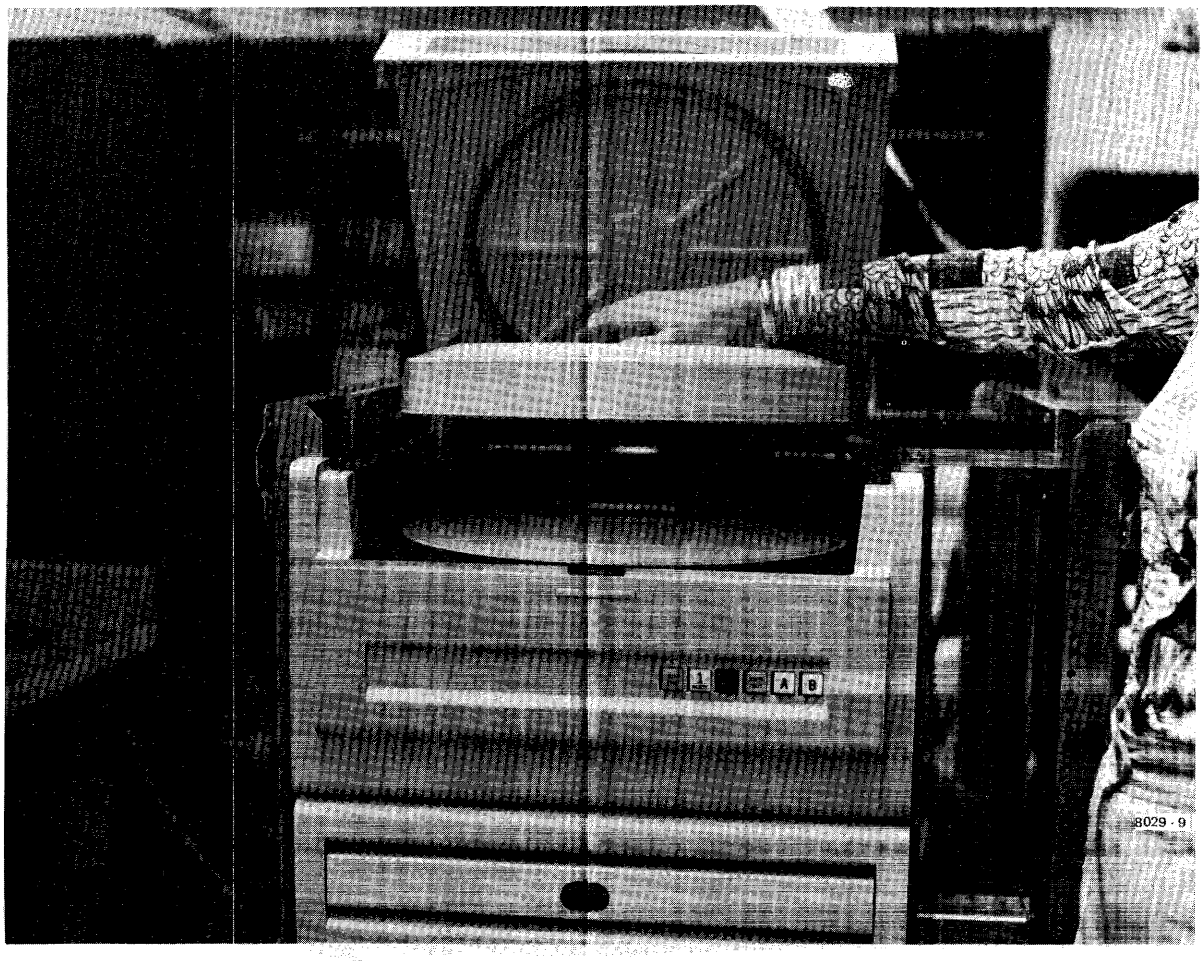


Figure 6-8 Installing Protection Cover

6.3.2 RK06K and RK07 Cartridge Unloading

1. Release the RUN/STOP switch (STOP).
2. Wait for the STOP indicator to illuminate.
3. Press the lid release bar and raise the lid.
4. Remove the RK06K or RK07K Cartridge as follows:
   a. Remove the protection cover and hold the cover in the left hand.
   b. Push the handle slide to the left before raising the top cover handle (Figure 6-9).
   c. Raise the top cover handle to a full upright position to release the cartridge from the drive spindle.
   d. Lift the cartridge up and out of the shroud, and place it in the protection cover.
   e. Lower the top cover handle to the horizontal position to lock the protection cover in place.

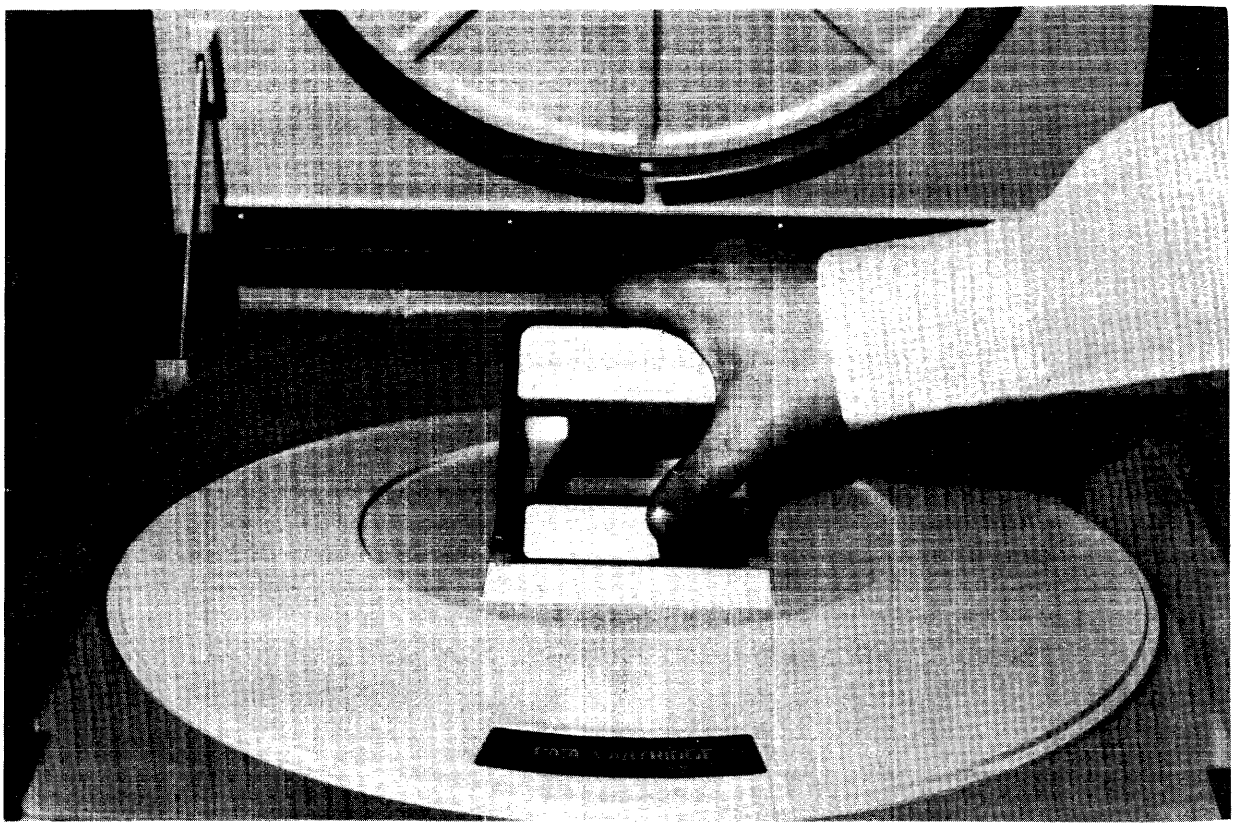


Figure 6-9 Engaging Lock Release

CHAPTER 7
PROGRAMMER'S GUIDE

7.1 INTRODUCTION

Since the Unibus provides a unified addressing structure in which device control, status, and data registers are directly addressed as memory locations, all operations on these registers are performed by normal memory reference instructions. Under these conditions, the RK06 or RK07 subsystem does not require a special class of input/output instructions to initiate the transfer of information or the manipulation of data.

With the exception of a Read Header command, data transfers use the nonprocessor request (NPR) facility of the Unibus for direct access to main memory, at a maximum transfer rate of 232,000 words per second (4.3 μs per word), in clock sizes ranging from 1 to 65,536 words. To achieve a smooth flow of data from a selected disk to main memory, the subsystem utilizes a first in/first out, 66-word data buffer known as a Silo.

A phase-locked clock system (PLO) and modified frequency modulation (MFM) recording technique add reliability to reading and writing operations regardless of minor changes in the rotational speed of a disk. In addition, program-controlled head offset positioning can correct any slight mechanical misalignment that may occur between read/write heads and a disk cartridge by allowing a head to be positioned about the track centerline in incremental steps. Also, error detection and correction hardware (ECC) provides adequate information for correcting any error burst of up to 11 consecutive bits within a sector

For increased reliability, parity checking is performed on the control information that is transferred between the drives and the controller. In addition, the controller also detects and flags data errors from the Unibus. Upon the indication of an error condition or the completion of a command, the controller can interrupt the processor. Thus extensive error indicators exist for on-line diagnosis, while numerous status indicators provide complete program control.

On multidrive systems, positioning operations can be overlapped (i.e., Seek operations may be performed on one or more drives before starting a transfer on another drive). Thus, while one drive is reading or writing, others can be positioning to a new cyclinder for the next transfer.

The following paragraphs provide detailed descriptions of controller register content and usage, followed by disk command descriptions and programming considerations related to the use of an RK06 or RK07 subsystem with a PDP-11 processor.

7.2 RK611 DEVICE REGISTERS

There are 15 usable, 16-bit device registers contained in the RK611 that are used to interface the controller with the RK06 or RK07 Drives and the PDP-11 Unibus (Figure 7-1). The 15 registers are loaded and/or read under program control to initiate selected disk commands and monitor subsystem status and error conditions. Device register bits are generally cleared by a Unibus Initialize (INIT), Controller Clear (CCLR), or Subsystem Clear (SCLR) operation. In the following descriptions (unless otherwise specified), it should be understood that the clearing of a bit by any one of these three methods is implied.

NOTE

The RK611 does not recognize DATOB (MOVB, BICB, etc.) bus cycles. All registers must be written as words.

7.2.1 Control/Status Register 1 (RKCS1)

The RKCS1 register (Figure 7-2) can be read or written via program control and as such is used to store the current disk command function code and operational status of the controller. In addition, the register can initiate command execution and enable a Controller Clear operation.

Go (GO) – Bit 0 – When the GO bit is set, the disk command Function Code (F1–F4) is executed. With the GO bit set, only two other device register bits can be set (Diagnostic Mode excepted), as follows:

- Controller Clear (CCLR), bit 15 in RKCS1, may be set via program control to initialize (general clear and preset) certain device registers within the controller. However, any status and/or error conditions set in the drives are not affected.
- Subsystem Clear (SCLR), bit 5 in RKCS2, may be set via program control to initialize both the controller and all of the drives.

When command execution is completed, the GO bit is reset and the controller is ready to accept a new command. However, the GO bit cannot be set if the Combined Error (CERR) bit is set. When CERR is set, the execution of a command can only occur following the initiation of a CCLR.

Function Code (F1–F4) – Bits 1–4 – The configuration of the Function Code bits (F1–F4), with the setting of the GO bit, allows the selected drive to respond to the following command control configuration.

Command	F4	F3	F2	F1	GO	Octal
Select Drive	0	0	0	0	1	01
Pack Acknowledge	0	0	0	1	1	03
Drive Clear	0	0	1	0	1	05
Unload	0	0	1	1	1	07
Start Spindle	0	1	0	0	1	11
Recalibrate	0	1	0	1	1	13
Offset	0	1	1	0	1	15
Seek	0	1	1	1	1	17
Read Data	1	0	0	0	1	21
Write Data	1	0	0	1	1	23
Read Header	1	0	1	0	1	25
Write Header	1	0	1	1	1	27
Write Check	1	1	0	0	1	31

Spare Bit – Spare bit 5 can be written and read back.

CONTROL AND STATUS REGISTER 1

RKCS1 — READ/WRITE — UNIBUS ADDRESS 777440

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CERR OCLR	DI	DCT PAR	CFMT	CTO	CDT	BA17	BA16	RDY	IE	0	F4	F3	F2	F1	GO

WORD COUNT REGISTER

RKWC — R/W — 777442

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 09	WC 08	WC 07	WC 06	WC 05	WC 04	WC 03	WC 02	WC 01	WC 00

BUS ADDRESS REGISTER

RKBA — R/W — 777444

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 09	BA 08	BA 07	BA 06	BA 05	BA 04	BA 03	BA 02	BA 01	BA 00

DISK ADDRESS (TRACK & SECTOR) REG.

RKDA — R/W — 777446

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	TA 2	TA 1	TA 0	0	0	0	SA 4	SA 3	SA 2	SA 1	SA 0

CONTROL AND STATUS REGISTER 2

RKCS2 — R/W — 777450

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MDS	UFE	OR	IR	SCLR	BAI	RLS	DS 2	DS 1	DS 0

DRIVE STATUS REGISTER

RKDS — READ ONLY — 777452

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SVAL	SDA	PIP	0	WRL	0	0	DDT	DRDY	VV	DROT	SPLS	ACLO	OFST	0	DRA

ERROR REGISTER

RKER — RO — 777454

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IDAE	COE	HVRC	BSE	ECH	DTYE	FMTE	DRPAR	NXF	SKI	ILF

ATTENTION SUMMARY AND OFFSET

RKAS/OF — R/W — 777456

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATN 7	ATN 6	ATN 5	ATN 4	ATN 3	ATN 2	ATN 1	ATN 0	OF 7	OF 6	OF 5	OF 4	OF 3	OF 2	OF 1	OF 0

DESIRED CYLINDER REGISTER

RKDC — R/W — UNIBUS ADDRESS 777460

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC

UNUSED

777462

DATA BUFFER

R/W — 777464

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 09	DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB 00

MAINTENANCE REGISTER 1

RKMR1 — R/W — 777466

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RD GATE	WRT GATE	ECCW	PCD	PCA	MEWD	MERD	MCLK	MIND	MSP	DMD	PAT	MS 3	MS 2	MS 1	MS 0

ECC POSITION REGISTER

RKECPS — RO — 777470

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	EPS 12	EPS 11	EPS 10	EPS 09	EPS 08	EPS 07	EPS 06	EPS 05	EPS 04	EPS 03	EPS 02	EPS 01	EPS 00

ECC PATTERN REGISTER

RKECPT — RO — 777472

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	EPT 10	EPT 09	EPT 08	EPT 07	EPT 06	EPT 05	EPT 04	EPT 03	EPT 02	EPT 01	EPT 00

MAINTENANCE REGISTER 2

RKMR2 — RO — 777474

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

MAINTENANCE REGISTER 3

RKMR3 — RO — 777476

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

11-4199

Figure 7-1 RK611 Device Registers

Interrupt Enable (IE) – Bit 6 – When the Interrupt Enable (IE) bit is set, the controller will be allowed to interrupt the processor under any of the following conditions:

- When Controller Ready (RDY), bit 7 in RKCS1, is set upon completion of a command.
- When any drive sets an associated Attention (ATN0–ATN7) bit (8–15) in RKAS/OF, with the set condition of Controller Ready (RDY).
- When any drive or the controller indicates the presence of an error by the setting of Controller Error (CERR), bit 15 in RKCS1.

In addition, via program control, an interrupt can be forced by the simultaneous setting of the Interrupt Enable (IE) and Controller Ready (RDY) bits in RKCS1. Finally, Interrupt Enable, bit 6, can be reset via program control as well as by conventional initialization (INIT, CCLR, SCLR).

Controller Ready (RDY) – Bit 7 – Controller Ready (RDY) is effectively a read-only bit. However, the bit can be externally set via conventional initialization (INIT, CCLR, SCLR) or internally set upon completion of a command. The RDY bit is reset when GO, bit 0 in RKCS1, is set.

Extended Bus Address (BA16, BA17) – Bits 8, 9 – The Extended Bus Address bits reflect Unibus upper address bits 16 and 17 and as such are an extension of the 16-bit RKBA register which contains the memory address required for the current data transfer.

Controller Drive Type (CDT) – Bit 10 – This bit specifies the type of drive that will be selected by the controller. To specify RK06 Disk Drives, the bit must be reset. For an RK07 Drive, the bit must be 1.

Controller Time-Out (CTO) – Bit 11 – Controller Time-Out is a read-only error bit that is set to indicate that GO, bit 0 in RKCS1, has been set for approximately 800 ms. Since this interval exceeds the time required to execute the longest possible drive operation (i.e., a Seek from cylinder 410 to cylinder 0 followed by a 65k word data transfer), the set condition of this bit indicates that the last command has not been completed due to a malfunction.

Controller Format (CFMT) – Bit 12 – The Controller Format bit specifies the number of sectors for each track in the selected drive. When bit 12 is set, a 20-sector format (18-bit data words) is defined for the sector counter located in the drive, and when the bit is reset, a 22-sector format (16-bit data words) is defined.

Drive-to-Controller Parity Error (DTC PAR) – Bit 13 – The DTC Parity Error is a read-only bit that is internally set to indicate that a parity error has been detected in a serial message received from the selected drive.

Drive Interrupt (DI) – Bit 14 – In relation to program control, Drive Interrupt (DI) is a read-only bit. When set, the bit differentiates between a drive-initiated interrupt and a controller-initiated interrupt.

The DI bit is set when any drive sets an associated Attention (ATN0–ATN7) bit (8–15 in RKAS–OF). Thus, if the Interrupt Enable (IE) bit is set, the setting of the DI bit with the set condition of Controller Ready (RDY), bit 7 in RKCS1, indicates a drive-initiated interrupt. The DI bit is reset by Unibus Initialize (INIT), Subsystem Clear (SCLR), or by the execution of Drive Clear commands to all drives asserting Attention.

Combined Error/Controller Clear (CERR/CCLR) - Bit 15 - As a Combined Error (CERR) indicator, bit 15 can be set by the controller, or any one of the drives, to indicate that a subsystem error has occurred (Table 7-1). However, when the bit is set via program control, a controller initialize (CCLR) operation is enabled which clears the controller and results in the clearing of bit 15 itself. Thus, if the bit is internally set (CERR) by an error that is followed by an external set (CCLR) to initialize the controller, bit 15 will be cleared. However, since only controller errors will be initialized by CCLR, any error originating in a drive will remain set in the drive.

CAUTION

When using a BIC instruction on the RKCS1 register, ensure that a 1 is set in bit 15 of the mask. If this is not done and CERR is set, a CCLR will occur, and the RK611 will be cleared. For example, to clear the interrupt Enable (IE) bit (bit 6 in RKCS1), the following instruction format is recommended:

BIC #100100, @RKCS1

Table 7-1 Combined Error (CERR)

Error	Indicator Bit	Condition
Programming Error (PGE)	RKCS2 bit 10	Register written (except CCLR SCLR) with GO set.
Illegal Function (ILF)	RKER bit 0	Illegal command in low-order 5 bits of RKCS1.
Format Error (FTER)	RKER bit 4 or 5	Format or Drive Type error.
Cylinder Overflow (COE)	RKER bit 9	Cylinder address exceeded.
Invalid Disk Address (IDAE)	RKER bit 10	Invalid cylinder or track address detected.
Unit Field Error (UFE)	RKCS2 bit 8	Drive selection problem.
UNIBUS Parity Error (UPE)	RKCS2 bit 13	Error in 16-bit data word from main memory.
Nonexistent Drive (NED)	RKCS2 bit 12	Drive response problem.
Drive Available Interrupt (DAINT)	RKDS bit 0	Drive is not available (dual-access only).
Drive Error (DRERR)	Message B0:T7 (FAULT)	Any 1 of 21 drive error conditions.
Bad Sector Error (BSERR)	RKER bit 7	Data transfer attempt to/from bad sector.
Header VRC Error (HVRC)	RKER bit 8	Header Check indicates bad header information.

Table 7-1 Combined Error (CERR) (Cont)

Error	Indicator Bit	Condition
Operation Incomplete (OPI)	RKER bit 13	Desired header cannot be found.
DTC Parity Error (DTC PAR)	RKCS1 bit 13	Parity error in message from drive.
Write Check Error (WCE)	RKCS2 bit 14	Write Check indicates data from disk did not match data from memory.
Nonexistent Memory (NEM)	RKCS2 bit 11	No SSYN within 10 μs of MSYN assertion.
Data Late Error (DLTERR)	RKCS2 bit 15	Data late to/from Silo.
Drive Timing Error (DTE)	RKER bit 12	Write Clock loss during write, data loss during read.
Data Check (DCK)	RKER bit 15	Data error detected by ECC.
Multiple Drive Select (MDS)	RKCS2 bit 9	More than one drive simultaneously selected.
Error Correction Hard (ECH)	RKER bit 6	Data error uncorrectable using ECC.
Controller Time-Out (CTO)	RKCS1 bit 11	Command possibly not executed.

7.2.2 Word Count Register (RKWC)

The RKWC register (Figure 7-3) is loaded with the two's complement of the number of data words to be transferred to or from main memory. The register is incremented by 1 after each bus cycle, and accommodates a maximum transfer of 65,536 words. The RKWC register can only be cleared by writing all zeros via program control.

7.2.3 Bus Address Register (RKBA)

The RKBA register (Figure 7-4) is initially loaded with the low-order 16 bits of the Unibus address that will reflect the main memory start location for a data transfer. With the low-order bit (0) always forced to 0, the RKBA register content is combined with high-order bits 8 and 9 of the RKCS1 register (BA16, BA17) to form a complete even-numbered word address. Following each data transfer bus cycle, the register is incremented by two to select the next even-numbered location.

7.2.4 Disk Address Register (RKDA)

For Read, Write, and Write Check commands, the RKDA register (Figure 7-5) is initially loaded to define the desired sector (1 of 20 or 22) and track (1 of 3 read/write heads) on the selected drive, from or to which the first block of a data transfer will be initiated. If the word count value indicates that a block of more than 256 data words is to be transferred, the Sector Address bits of the RKDA register will be incremented to select the next consecutive sector and the next track, if necessary, until a word count overflow indicates that data transfers are completed or an error occurs. In either case, completion of the command is indicated by the setting of the Controller Ready (RDY) bit in RKCS1 and an increment of the RKDA register to the next sector location.

Sector Address Bits 0–4 (SA0–SA4)

Sector Address bits 0–4 are configured (00–23) to select a value ($00–19_{19}$) for a 20-sector format (18-bit data words) or configured (00–25) to select a value ($00–21_{19}$) for a 22-sector format (16-bit data words). The Sector Address is incremented by one when the sector has been transferred.

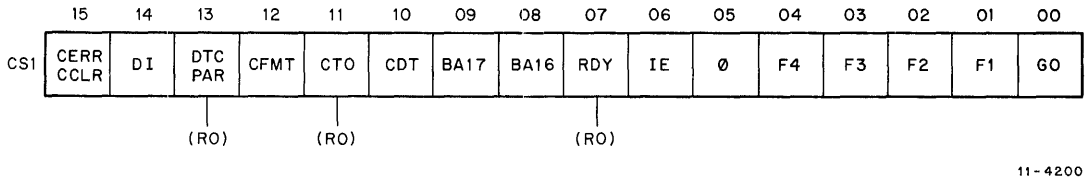


Figure 7-2 Control/Status Register 1

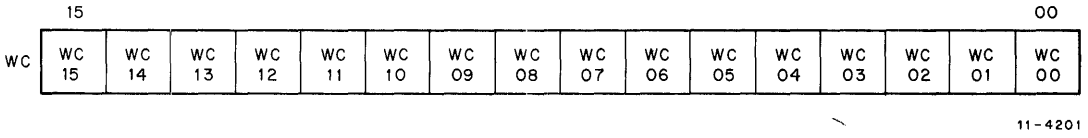


Figure 7-3 Word Count Register

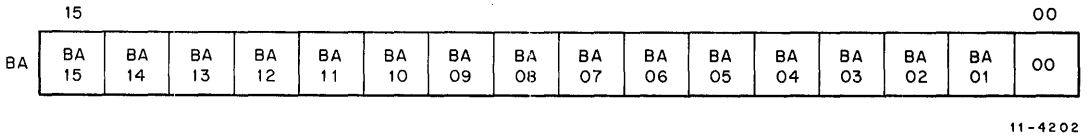


Figure 7-4 Bus Address Register

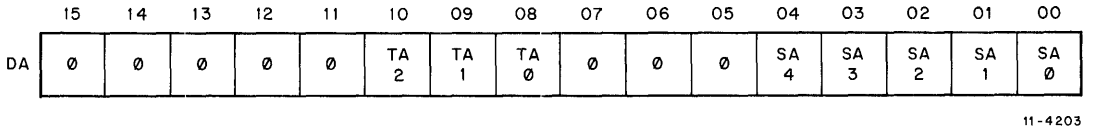


Figure 7-5 Disk Address Register

Spares – Bits 5–7 – Spare bits 5–7 are 0.

Track Address (TA0–TA2) – Bits 8–10 – The Track Address bits are configured (0–2) to select the appropriate read/write head associated with the desired track. The Track Address bits are incremented by one after the last sector (23_8 or 25_8) on the track has been transferred and the Sector Address has been reset to zero. Similarly, if transfers continue beyond the last sector of the last track (2) of a given cylinder, the Track Address is reset to zero and the Cylinder Address (in RKDC) is incremented by one. In this manner, subsequent sectors, tracks, and cylinders can be consecutively transferred until the word count equals zero. However, if the word count does not equal zero after the transfer of the last sector (19 or 20_{10}) on the last track (2) of the last cylinder (410_{10} for an RK06 or 814_{10} for an RK07), a Cylinder Overflow Error (COE) will occur.

Spares – Bits 11–15 – Spares bits 11–15 are 0.

7.2.5 Control/Status Register 2 (RKCS2)

The RKCS2 register (Figure 7-6) can be read or written via program control and is used to store the current drive select code, subsystem operational status, and Silo control information. In addition, the register can initiate a Subsystem Clear (SCLR) operation.

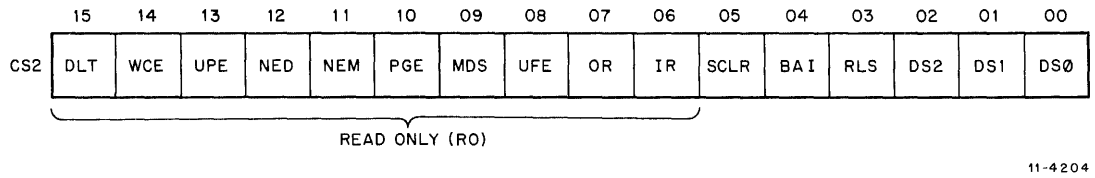


Figure 7-6 Control/Status Register 2

Drive Select (DS0–DS2) – Bits 0–2 – The Drive Select bits are configured ($0–7_8$) with the unit number of the drive to be currently selected.

Release (RLS) – Bit 3 – When the RLS bit is set and a command is initiated, the drive specified by DS0–2 will be released. The bit is used in dual-access configurations to effect the release of a drive from one controller and make it available to the other controller. This is necessary because once a drive is accessed by a specific controller, it is not available to the other unless one second has elapsed since the first controller accessed the drive.

Bus Address Increment Inhibit (BAI) – Bit 4 – When the BAI bit is set via program control, the RKBA register is prevented from incrementing during data transfers. This is primarily a diagnostic aid.

Subsystem Clear (SCLR) – Bit 5 – When the SCLR bit is set via program control, the controller is cleared and the Initialize line is asserted on the drive interface to clear all of the drives available to the system.

Input Ready (IR) – Bit 6 – Input Ready is a read-only bit that is set to indicate that the Silo input buffer is ready to accept a word. Conversely, the bit is reset to indicate that the Silo is full and cannot accept a word. The IR bit is also set by conventional initialization (INIT, CCLR, SCLR) or by the setting of the GO bit (0 in RKCS1).

Output Ready (OR) – Bit 7 – Output Ready is a read-only bit that is set to indicate that a word is in the Silo output buffer. The bit is cleared by conventional initialization (INIT, CCLR, SCLR) or by the setting of the GO bit (0 in RKCS1).

Unit Field Error (UFE) – Bit 8 – Unit Field Error is a read-only error bit that is set to indicate the following:

- The Drive Select code bits (T0–T2) in the current status message (A0–A3) received by the controller did not compare with the Drive Select (DS0 – DS2) code transmitted on the Message A line. The setting of this error bit is disabled by diagnostic mode operation.
- A Deselect bit (T3) was transmitted to a drive on the Message A line and the Select Acknowledge (SACK) signal was not negated.

Multiple Drive Select (MDS) – Bit 9 – Multiple Drive Select is a read-only error bit that is set by the assertion of the MDS signal line, via the selected drive, when a determination is made that at least one other drive has been simultaneously selected. This bit can only be cleared by a Unibus Initialize (INIT) or a Subsystem Clear (SCLR).

Programming Error (PGE) – Bit 10 – Programming Error is a read-only error bit that is set if any controller register is written (bits for CCLR and SCLR excepted) while the GO bit in RKCS1 is set. The error is disabled in diagnostic mode.

Nonexistent Memory (NEM) – Bit 11 – Nonexistent Memory is a read-only error bit that is set when the controller attempts to execute a bus cycle and SSYN is not returned within 10 μs of the assertion of MSYN.

Nonexistent Drive (NED) – Bit 12 – Nonexistent Drive is a read-only error bit that is set to indicate the following:

- A Select Acknowledge (SACK) signal from a selected drive has not been asserted on the interface in response to a message (other than a Release) sent to the drive.
- A complete status message (A0–A3, B0–B3) was not received from a selected drive within 20 μs of a message request from the controller.

Unibus Parity Error (UPE) – Bit 13 – Unibus Parity Error is a read-only error bit that is set to indicate that a parity error has been detected in a 16-bit data word format from main memory, during the performance of a Write or Write Check command. During 18-bit data word transfers, a Unibus parity error cannot be detected.

Write Check Error (WCE) – Bit 14 – Write Check Error is a read-only error bit that is set to indicate that a data word read from the disk during the execution of a Write Check command did not compare with the corresponding data word contained in main memory. If a write check error is detected and the BAI bit is not set, the RKBA register will contain the memory address of the next data word location (mismatched word address plus two).

Data Late Error (DLT) – Bit 15 – Data Late Error is a read-only error bit that is set to indicate the following:

- During the execution of a Write command, the Silo was empty when the disk required a data word.
- During the execution of a Read or a Write Check command, the Silo was full when the disk provided the next data word.

This error bit can be forced set under the following conditions:

- By loading the Data Buffer register (RKDB) when Input Ready (IR) (bit 6) is reset.
- By reading the Data Buffer register (RKDB) when Output Ready (OR) (bit 7) is reset.

NOTE

When RKCS2 is loaded under program control, the controller Sector/Index pulse separator logic is initialized. This action causes the controller to ignore the next sector or index pulse from the selected drive. Therefore, unnecessary loading of RKCS2 can increase latency time by an amount equivalent to 1.5 sectors.

7.2.6 Drive Status Register (RKDS)

The RKDS register (Figure 7-7) is a read-only register that is used to store the operational status of a selected drive. However, information obtained from the drive is not immediately available to program control until the information is validated (SVAL) by the setting of bit 5, which indicates that a complete status message has been received providing a valid update.

Status information bits set in the RKDS register can be cleared by conventional initialization (INIT, CCLR, SCLR). However, a Controller Clear (CCLR) operation does not affect status or error condition bits that are currently set in the drives. In addition, a Unibus Initialize (INIT) or Subsystem Clear (SCLR) operation can only reset status or error bits in a drive if the associated status or error condition no longer exists.

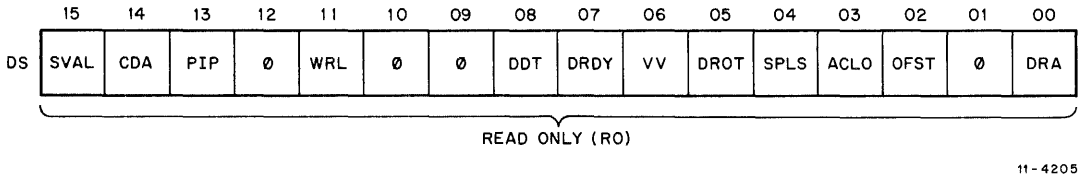


Figure 7-7 Drive Status Register

Drive Available (DRA) – Bit 0 – Drive Available is a read-only bit that is conditioned (message A0:T5) to dual-access operation as follows:

- When set by a selected drive, DRA indicates that the drive is available to accept commands from the controller.
- If an attempt is made to select a dual-access drive that is currently accessed by the other controller, the DRA bit will not be set. This is considered an error condition by the controller, resulting in the setting of controller Combined Error (CERR) bit in RKCS1 and the generation of a program interrupt (if enabled).

Spare – Bit 1 – Spare bit 1 is 0.

Offset (OFST) – Bit 2 – Offset is a read-only bit that is set (Message A0:T10) to indicate that the selected drive is in Offset mode.

Drive AC Low (ACLO) – Bit 3 – Drive AC Low is a read-only bit that is set (Message B0:T6) to indicate that ac power in the selected drive is low or has been interrupted. Following detection of an ac low condition, the heads will unload when the next Sector pulse occurs. This action allows the transfer of the current sector to be completed before the heads are unloaded.

If ac power is restored, the error condition can be reset within the drive by a Unibus Initialize (INIT), Subsystem Clear (SCLR), power up, or RUN switch reset.

Speed Loss (SPLS) – Bit 4 – Speed Loss is a read-only bit that is set (Message B0:T12) to indicate that spindle speed is unacceptably low.

Drive Off Track (DROT) – Bit 5 – Drive Off Track is a read-only bit that is set (Message B0:T13) to indicate that the Write Gate signal has been asserted while the heads are not properly positioned over the track centerline.

Volume Valid (VV) – Bit 6 – Volume Valid is a read-only bit that is set (Message A0:T6) to indicate that the Volume Valid flip-flop has been set in the selected drive by a Pack Acknowledge command. The set condition of the bit ensures the program that the cartridge and the unit number plug have not been changed since the last command was issued to the drive, and power has not been removed. The bit is reset when the cartridge, the unit number plug, or ac power is removed.

Drive Ready (DRDY) – Bit 7 – Drive Ready is a read-only bit that is set (Message A0:T7) to indicate that the selected drive is up to speed and the heads are properly positioned over a valid cylinder. Under these conditions, the drive is prepared to receive a command.

Disk Drive Type (DDT) – Bit 8 – Disk Drive Type is a read-only bit that is internally conditioned (Message A0:T8) to indicate the type of drive selected. For an RK06 Drive, the bit remains reset, and for an RK07 Drive, the bit is set. However, before any commands can be executed, the bit must compare with the condition of Controller Drive Type, bit 10 in RKCS1.

Spare – Bits 9 and 10 – Spare bits 9 and 10 are 0

Write Lock (WRL) – Bit 11 – Write Lock is a read-only bit that is set (Message A0:T11) if the selected drive is write protected.

Spare – Bit 12 – Spare bit 12 is 0.

Positioning in Progress (PIP) – Bit 13 – Positioning in Progress is a read-only bit that is set (Message A0:T13) to indicate that the heads are in motion.

Current Drive Attention (CDA) – Bit 14 – Current Drive Attention is a read-only bit that is the logical equivalent of the Drive Status-Change (DSC) bit in the drive defined by the Drive Select (DS0–DS2) bits in RKCS2. The assertion of the Attention line indicates any one of the following conditions:

1. Seek operation is completed.
2. Offset operation is completed.
3. Heads are unloading (Message A1:T14).
4. A FAULT condition (Message B0:T7) has been set in the drive which enables the setting of CERR (bit 15 in RKCS1) to indicate one or more of the following:
   a. AC low error (Message B0:T6).
   b. Nonexecutable function (Message B0:T8).
   c. Controller-to-drive message parity error (Message B0:T9).
   d. Seek incomplete (Message B0:T10).
      - Invalid address (Message B0:T5).
      - Seek and no motion (Message B1:T12).
      - Limit detected on seek (Message B1:T13)*.
      - Servo unsafe (Message B1:T14)*.
   e. Write lock error (Message B0:T11).
   f. Speed loss error (Message B0:T12)*.
   g. Drive off track (Message B0:T13).

*In addition to setting the CSA bit and asserting Attention, these drive fault conditions will cause the heads to be unloaded.

h. Read/Write unsafe (Message B0:T14).
   - Sector error (Message B1:T4)*.
   - Write current/no write gate (Message B1:T5)*.
   - Write gate/no transitions (Message B1:T6)*.
   - Head fault (Message B1:T7)*.
   - Multiple head select (Message B1:T8)*
   - Index error (Message B1:T9)*.
   - Tribit error (Message B1:T10)*.
   - Servo signal error (Message B1:T11)*.

NOTE
A Drive Status-Change (DSC) is also indicated by the setting (Message A0:T14) of bit 14 in RKMR2.

Status Valid (SVAL) – Bit 15 – Status Valid is a read-only bit that is set to indicate that the bits in both the Drive Status (RKDS) and Error (RKER) registers have been updated for the selected drive via receipt of a complete status message. The bit is cleared by conventional initialization (INIT, CCLR, SCLR): initiating a new command (writing into RKCS1), selecting a new drive (writing into RKCS2), or whenever an Attention signal is asserted by the selected drive for a drive status change.

7.2.7 Drive Error Register (RKER)

The RKER register (Figure 7-8) is a read-only register that is used to store the error status of a selected drive. However, error information obtained from the drive is not immediately available to program control until the information is validated (SVAL) by the setting of bit 15 in the RKDS register, which indicates that a complete status message frame has been received.

Error bits set in the RKER register can be cleared by conventional initialization (INIT, CCLR, SCLR). However, a Controller Clear (CCLR) operation does not affect error bits that are currently set in the drive. In addition, a Unibus Initialize (INIT) or Subsystem Clear (SCLR) operation can only reset error bits in a drive if the associated error condition no longer exists.

Illegal Function (ILF) – Bit 0 – Illegal Function is a read-only bit that is set to indicate that an illegal command (33_8, 35_8, 37_8) has been loaded into RKCS1.

Seek Incomplete (SKI) – Bit 1 – Seek Incomplete is a read-only bit that is set (Message B0:T10) to indicate that a seek operation has not been completed for one of the following conditions:

- An Invalid Address (Message B0:T5) bit has been set in the drive, indicating that the drive has received an invalid head or cylinder address.
- A Seek and No Motion (Message B1:T12) bit has been set in the drive, indicating that a Seek command was received by the drive but no track crossing pulses were detected within 10 ms.
- A Limit Detected on Seek (Message B1:T13) bit has been set in the drive, indicating that an inner limit or an outer limit was detected during a Seek operation. If this fault occurs, the heads are unloaded.
- A Servo Unsafe (Message B1:T14) bit has been set in the drive, indicating a servo runaway condition. If this fault occurs, the servo actuator is disconnected from the servo drive and connected to a battery that provides the necessary power to drive the heads to the home position.

*In addition to setting the CSA bit and asserting Attention, these drive fault conditions will cause the heads to be unloaded.

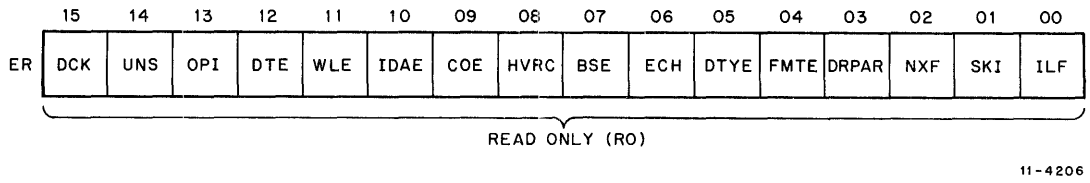


Figure 7-8 Drive Error Register

In addition to the setting of the SKI bit (Message B0:T10) in the RKER register, the occurrence of any one of these faults allows the CDA bit (bit 14) to be set in the RKDS register, the Attention signal to be asserted for the RKAS/OF register, the DSC bit (Message A0:T14) to be set in the RKMR2 register, and the Fault bit (Message B0:T7) to be set for the RKMR3 register.

Nonexecutable Function (NXF) – Bit 2 – Nonexecutable Function is a read-only bit that is set (Message B0:T8) to indicate that a Seek command or a Write Gate signal has been received by the selected drive while Volume Valid was reset. The occurrence of this fault allows the CDA bit (bit 14) to be set in RKDS, the Attention signal to be asserted for RKAS/OF, the DSC bit to be set in RKMR2, and the Fault bit to be set in RKMR3.

Control-to-Drive Parity Error (DRPAR) – Bit 3 – Control-to-Drive Parity Error is a read-only bit that is set (Message B0:T9) to indicate that the drive detected a parity error on a controller-to-drive message transmission. The occurrence of this fault allows the CDA bit (bit 14) to be set in RKDS, the Attention signal to be asserted for RKAS/OF, the DSC bit to be set in RKMR2, and the Fault bit to be set in RKMR3.

Format Error (FMTE) – Bit 4 – Format Error is a read-only bit that is set when the format status bit (Message A0:T9) returned from the selected drive does not compare with the CFMT bit (bit 12) in RKCS1.

Drive-Type Error (DTYE) – Bit 5 – Drive-Type Error is a read-only bit that is set when the drive-type status bit (Message A0:T8) returned from the selected drive does not compare with the CDT bit (bit 10) in RKCS1 (reset for RK06 or set for RK07).

Error Correction Hard (ECH) – Bit 6 – Error Correction Hard is a read-only bit that is set to indicate that a data error detected by the Error Correction Code (ECC) logic in the controller cannot be corrected using ECC.

Bad Sector Error (BSE) – Bit 7 – Bad Sector Error is a read-only bit that is set to indicate that a data transfer has been attempted to or from a sector that has at least one of the two Good Sector Flag bits (Header Word 2, bits 14 and 15) reset, indicating a bad sector.

Header Vertical Redundancy Check Error (HRVC) – Bit 8 – Header VRC Error is a read-only bit that is set to indicate that a VRC error has been detected on a sector header during a data transfer. If the Operation Incomplete (OPI) bit (bit 13) is also set, the sector in which the error occurred cannot be determined. However, if the OPI bit is reset, the VRC error was detected in the sector currently defined by the RKDA register (SAO–SA4).

Cylinder Overflow Error (COE) – Bit 9 – Cylinder Overflow Error is a read-only bit that is set to indicate that the RKWC register is not equal to zero following a data transfer from cylinder 410_{10} (for RK06) or 814_{10} (for RK07), track 2_{10}, and sector 19_{10} or 21_{10} (last logical sector).

Invalid Disk Address Error (IDAE) – Bit 10 – Invalid Disk Address Error is a read-only bit that can be set via an Invalid Address bit (Message B0:T5) from the drive, or by the controller, to indicate the following:

1. An Invalid Address (Message B0:T5) bit has been set in the selected drive, indicating that an invalid cylinder address (411_{10} through 511_{10} for the RK06 or 815_{10} through 1023_{10} for the RK07) and/or an invalid track address (3_{10}) has been detected with the receipt of a Seek command.

   In addition to setting the IDAE bit, either of these faults will set the SKI bit in the RKER register, the CDA bit in the RKDS register (while asserting an Attention signal for RKAS/OF), the DSC bit in RKMR2, and the Fault bit in RKMR3.

2. The controller detected an illegal desired cylinder (DC0–DC9) value (411_{10} through 814_{10}) in the RKDC register during the initiation of a command, if the drive (as defined by bit 10 of RKCS1) is an RK06. These cylinder values are allowed only on the RK07.

3. The controller detected an illegal track address (TAO–TA2) value (3_{10} through 7_{10}) in the RKDA register during the initiation of a command.

Write Lock Error (WLE) – Bit 11 – Write Lock Error is a read-only bit that is set (Message B0:T11) to indicate that the drive received the assertion of the Write Gate signal when it was in Write Protect mode. The occurrence of this fault allows the CDA bit to be set in RKDS, the Attention signal to be asserted for RKAS/OF, the DSC bit to be set in RKMR2, and the Fault bit to be set in RKMR3.

Drive Timing Error (DTE) – Bit 12 – Drive Timing Error is a read-only bit that is set to indicate the following:

1. The loss of Write Clock by the controller during a write.

2. The loss of encoded read data by the controller during a read.

Operation Incomplete (OPI) – Bit 13 – Operation Incomplete is a read-only bit that is set to indicate that following the positioning of the heads to a desired cylinder and the reading of 32 headers, the desired header could not be found. This error can result from any one of the following:

1. Head mispositioning

2. Incorrect head selection

3. Read channel failure

4. Improper pack formatting.

Drive Unsafe (UNS) – Bit 14 – Drive Unsafe is a read-only bit that is set (Message B0:T14) to indicate that any one of the following Read/Write Unsafe conditions, each of which causes the heads to be unloaded, has been detected.

1. Sector Error (Message B1:T5) indicates that Write Gate was asserted in the drive in coincidence with the trailing edge of a sector pulse.

2. Write Current/No Write Gate (Message B1:T5) indicates that write current has been detected in the drive without the assertion of Write Gate.

3. Write Gate/No Transitions (Message B1:T6) indicates that the drive received the assertion of Write Gate while no encoded write data has been received.

4. Head Fault (Message B1:T7) indicates that an electrical imbalance exists in the write signals that have been fed to the head, which could cause erroneous data to be recorded.

5. Multiple Head Select (Message B1:T8) indicates that more than one read/write head has been selected simultaneously.

6. Index Error (Message B1:T9) indicates that the once-per-revolution index pulse is either mispositioned or is missing.

7. Tribit Error (Message B1:T10) indicates that three successive tribits were missing from the servo track.

8. Servo Signal Error (Message B1:T11) indicates that no signals have been detected from the servo head.

In addition to the setting of the UNS bit in the RKER register, the occurrence of any one of these fault conditions allows the CDA bit to be set in the RKDS register, the Attention signal to be asserted for the RKAS/OF register, the DSC bit (Message A0:T14) to be set in RKMR2, and the Fault bit (Message B0:T7) to be set in RKMR3.

Data Check (DCK) – Bit 15 – Data Check is a read-only bit that is set to indicate that a data error was detected when the current sector was read.

7.2.8 Attention Summary/Offset Register (RKAS/OF)

The RKAS/OF register (Figure 7-9) can be read or written via program control and as such is used to store the head offset value required by an Offset command and the current condition of the Attention signal line that is monitored for each drive.

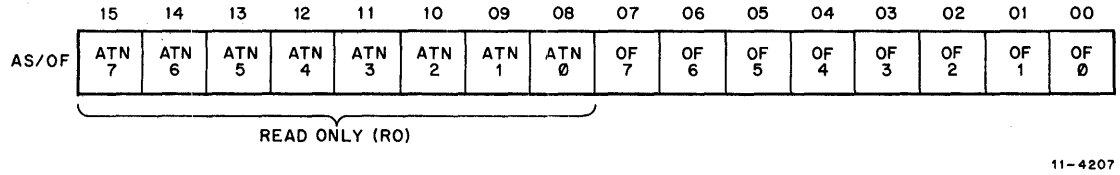


Figure 7-9 Attention Summary/Offset Register

Offset (OF0–OF7) – Bits 0–7 – The Offset field (OF0–OF7) defines both the magnitude (OF0–OF5) and direction (OF7) of head movement in relation to the centerline of a track. As shown below, each binary increment of the offset value (excluding OF6) produces a move of 25 microinches (for an RK06) or 12.5 microinches (for an RK07) in a positive (+) or negative (–) direction. A positive offset (OF7 = 0) provides head motion toward the spindle, while a negative offset (OF7 = 1) provides head motion away from the spindle. Therefore, an offset value of all zero would leave the heads positioned on the centerline of a desired cylinder.

NOTE
X = Don't care.

Sign		Magnitude						RK06 Offset	RK07 Offset
OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0	(μin)	(μin)
0	X	0	0	0	0	0	0	0	0
1	X	0	0	0	0	0	0	0	0
0	X	0	0	0	0	0	1	+25	+12.5
1	X	0	0	0	0	0	1	-25	-12.5
0	X	0	0	1	0	0	0	+200	+100
1	X	0	0	1	0	0	0	-200	-100
0	X	0	1	0	0	0	0	+400	+200
1	X	0	1	0	0	0	0	-400	-200
0	X	1	0	0	0	0	0	+800	+400
1	X	1	0	0	0	0	0	-800	-400
0	X	1	1	0	0	0	0	+1200	+600
1	X	1	1	0	0	0	0	-1200	-600

Once an Offset command has been executed, the selected drive will remain in offset mode if read commands (i.e., Read Data, Write Check, Read Header) or a Seek are subsequently initiated for the current cylinder. However, write commands (i.e., Write Data, Write Header) to the current cylinder, or any head motion initiating command to another cylinder, will disable the offset condition and allow the heads to be repositioned over the centerline of the desired cylinder.

Attention (ATN0–ATN7) – Bits 8–15 – The Attention indicators are read-only bits that reflect the unit number of each drive available to the system and the condition of an associated Drive Status Change flip-flop. All of the ATN bits are continuously monitored and updated (polled) every 7.4 μs. Under these conditions and during the update time alloted to a drive, an ATN bit will be set by the assertion of an Attention Line signal if the Drive Status-Change flip-flop is set. Thus, the clearing of the flip-flop within the drive will clear the associated ATN bit. The condition of the Drive Status-Change flip-flop is also noted in the controller by the conditioning (Message A0:T14) of the DSC bit (bit 14) in the RKMR2 register.

7.2.9 Desired Cylinder Register (RKDC)

The RKDC register (Figure 7-10) can be read or written via program control and is used to store the address of the desired cylinder. Following an initial load, the value in the RKDC register will be incremented by one whenever the track address (TA0–TA2) value in the RKDA register overflows during a data transfer. When the RKDC register is incremented and the RKWC register is not equal to zero, a single-cylinder seek is initiated by the controller.

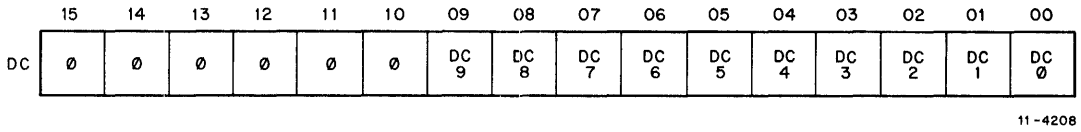


Figure 7-10 Desired Cylinder Register

Desired Cylinder (DC0–DC9) – Bits 0–9 – For an RK06 Drive, valid cylinder addresses range from the outer edge of the disk (0) to the center (410_{80}), requiring nine (DC–DC8) address bits to define the range ($000–632_8$). For an RK07 Drive, valid cylinder addresses range from the outer edge of the disk (0) to the center (815_{10}), requiring ten (DC0–DC9) address bits to define the range ($000–1456_8$).

Spares – Bits 10–15 – Spare bits 10–15 are zero.

7.2.10 Data Buffer Register (RKDB)

The RKDB register (Figure 7-11) can be read or written via program control. Reading from the register empties the Silo, while writing into the register fills the Silo. Both the RKDB register and the Silo are cleared by conventional initialization (INIT, CCLR, SCLR).

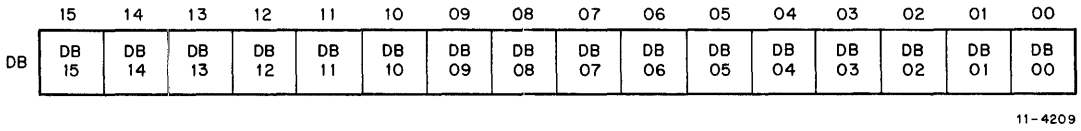


Figure 7-11 Data Buffer Register

7.2.11 Maintenance Register (RKMR1)

The RKMR1 register (Figure 7-12) can be read or written via program control and is primarily used to provide an operational analysis of the subsystem (i.e., RK611 Controller and the selected drive). This includes drive message analysis and parity testing and the initiation of a Diagnostic mode (DMD) of operation in which the controller can be isolated and exercised.

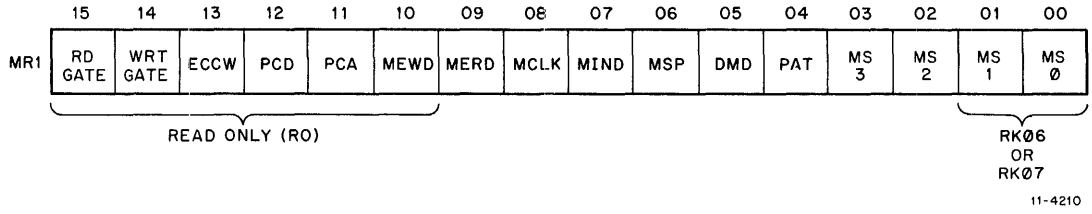


Figure 7-12 Maintenance Register 1

Message Select (MS0–MS3) – Bits 0–3 – The RK06 or RK07 Message Select (MS0 and MS1) bits define one of the four pairs of 16-bit status messages (A0–A3 and B0–B3) that can be simultaneously delivered to the controller on the Message A and Message B lines. When both messages are defined by the equivalent value, Message A is sent to the RKMR2 register as Message B is simultaneously sent to the RKMR3 register. The select bits are cleared by conventional initialization or by loading a command (other than Select Drive) into RKCS1.

Parity Test (PAT) – Bit 4 – When the Parity Test bit is set, the controller is forced to generate even parity for the messages sent to the drive on the Message A and Message B lines. Similarly, the controller makes an even parity check on the status messages returned from the drive.

Diagnostic Mode (DMD) – Bit 5 – When the Diagnostic mode bit is set, the controller is effectively disconnected from all of the drives and placed under the control of specific bits in the RKMR1 register (i.e., MSP, MIND, MCLK, MERD).

Maintenance Sector Pulse Bit 6 (MSP) – Bit 6 – When MSP is set in conjunction with the setting of the DMD bit, the receipt of a sector pulse from a drive is simulated.

Maintenance Index (MIND) – Bit 7 – When MIND is set in conjunction with the setting of the DMD bit, the receipt of an index pulse from a drive is simulated.

Maintenance Clock (MCLK) – Bit 8 – When DMD is set, MCLK replaces the internal controller clock derived from the data separator. The toggling (set, reset, etc.) of MCLK provides the clock pulses required to step through a controller command, including the simulated reading or writing of data.

Maintenance-Encoded Read Data (MERD) – Bit 9 – When DMD is set, MERD is used to simulate encoded serial data.

Maintenance-Encoded Write Data (MEWD) – Bit 10 – The MEWD bit is a read-only bit that is normally unconditionally set by the controller. A reset condition of the bit, when read in conjunction with the setting of DMD, indicates that the encoding logic has functioned properly during the simulated execution of a write command.

Precompensation Advance (PCA) – Bit 11 – Precompensation Advance is a read-only bit that is set to indicate that write precompensation logic within the controller has determined that the pulse required to record the current data bit must be advanced in time to ensure the reliability of the bit during subsequent reads.

Precompensation Delay (PCD) – Bit 12 – Precompensation Delay is a read-only bit that is set to indicate that write precompensation logic within the controller has determined that the pulse required to record the current data bit must be delayed in time to ensure the reliability of the bit during subsequent reads.

ECC Word (ECCW) – Bit 13 – ECC Word is a read-only bit that is normally set in the controller. A reset condition of the bit indicates that the timing logic is reflecting the ECC field within the sector.

Write Gate (WRT GT) – Bit 15 – Write Gate is a read-only bit that is set to indicate that Write Gate has been asserted by the controller.

Read Gate (RD GT) – Bit 14 – Read Gate is a read-only bit that is set to indicate that Read Gate has been asserted by the controller.

7.2.12 ECC Position Register (RKECPS)

The Error Correction Code (ECC) Position register (Figure 7-13) is a read-only register that is used store the error position value, which results from the successful execution of an ECC correction sequence. When an ECC correction sequence is not in progress, the RKECPS register contains one of two possible values (004066_8 or 005066_8). If the CFMT bit (bit 12) in RKCS1 is reset reflecting a 22-sector format (16-bit data words), the lesser value is contained in the register. However, if the CFMT bit is set, reflecting a 20-sector format (18-bit data words), the greater value is contained in the register.

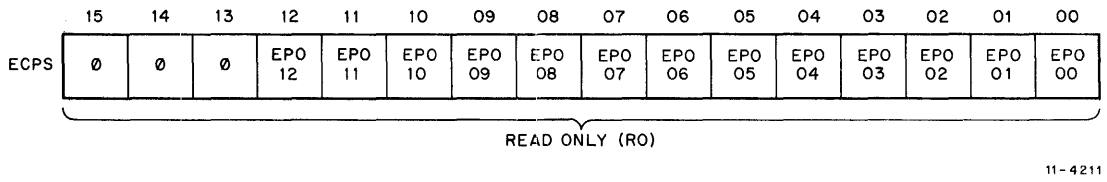


Figure 7-13 ECC Position Register

Error Position (EP00–EP12) – Bit 0–12 – The Error Position bits are read-only bits that define the start bit location of an error burst (containing from 1 to 11 error bits) within a 256-word Data field, following the completion of an ECC correction sequence. The position is valid if the error is ECC-correctable. If the detected error is not correctable using ECC, the register contains a constant (010040_8).

Spares – Bits 13–15 – Spare bits 13–15 are 0.

7.2.13 ECC Pattern Register (RKECPT)

The Error Correction Code (ECC) Pattern register (Figure 7-14) is a read-only register that contains an 11-bit error correction pattern from the ECC polynominal generator. The pattern is valid if the error is ECC-correctable.

Error Pattern (EPA0–EPA10) – Bits 0–10 – The Error Pattern bits are read-only bits that provide an 11-bit correction pattern for an error burst that does not exceed 11 bits in length and is, therefore, ECC-correctable.

Spares – Bits 11–15 – Spare bits 11–15 are 0.

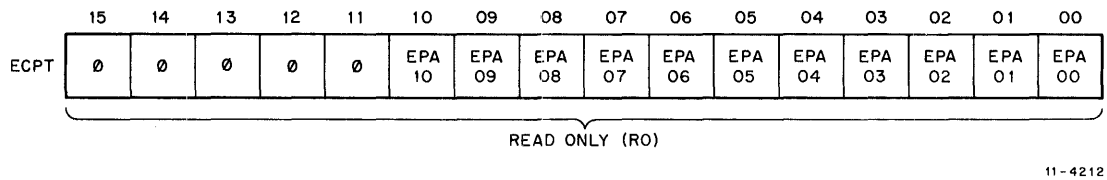


Figure 7-14 ECC Pattern Register

7.2.14 Maintenance Register 2 (RKMR2)

RKMR2 is a read-only register that is used for Message A controller-to-drive transmissions (commands), as well as Message A0–A3 drive-to-controller transmissions (status).

Controller-to-Drive (Message A) – For controller-to-drive transmissions (Figure 7-15), the 16-bit Message A shift register assembles disk commands, along with an appropriate odd parity bit, from various device registers and command logic within the controller. As the bits are assembled in the register, they are serially transmitted to the drives in coincidence with the transmission of Message B, with each bit position (0–15) directly related to an equivalent transmission time (T0–T15). For additional information, refer to Paragraph 2.5.1.

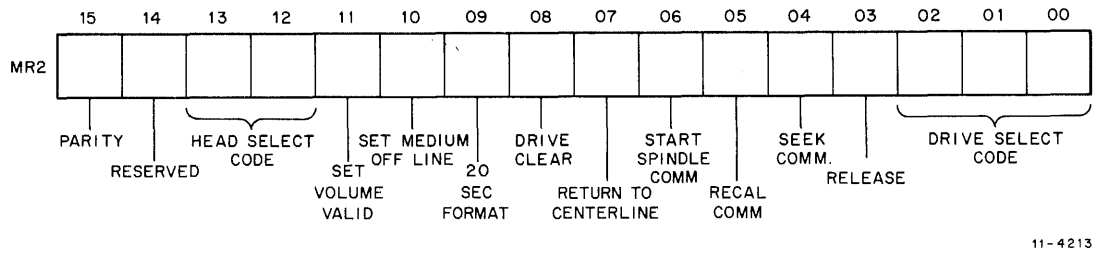


Figure 7-15 Maintenance Register 2 – Controller to Drive

Drive-to-Controller (Message A0–A3) – For drive-to-controller transmissions (Figure 7-16) the 16-bit Message A shift register assembles status information, along with an appropriate odd parity bit, from various status and error registers within the drive. As the bits are serially transmitted from the drive in coincidence with Message B status bits, they are assembled in the register with each bit position relating directly to an equivalent transmission time.

Since only one of four status messages can be stored in the Message A shift register at a time, a desired message (A1–A3), other than A0, must be previously defined by the execution of a Select Drive command.

7.2.15 Maintenance Register 3 (RKMR3)

RKMR3 is a read-only register that is used for Message B drive-to-controller transmissions (additional command parameters), as well as Message B0–B3 drive-to-controller transmissions (status).

Controller-to-Drive (Message B) – For controller-to-drive transmissions (Figure 7-17), the 16-bit Message B shift register assembles additional disk command information (including the status message request numeric of 0, 1, 2, or 3), along with an appropriate odd parity bit, from various device registers and command logic within the controller. As the bits are assembled in the register, they are serially transmitted to the drives in coincidence with the transmission of Message A, with each bit position (0–15) directly related to an equivalent transmission time (T0–T15). For additional information, refer to Paragraph 2.5.1.

Drive-to-Controller (Message B0–B3) – For drive-to-controller transmissions (Figure 7-18), the 16-bit Message B shift register assembles status information, along with an appropriate odd parity bit, from various status and error registers within the drive. As the bits are serially transmitted from the drive in coincidence with the Message A status bits, they are assembled in the register with each bit position relating directly to an equivalent transmission time.

Since only one of four status messages can be stored in the Message B shift register at a time, a desired message (B1–B3), other than B0, must be previously defined by the execution of a Select Drive command.

NOTE

Maintenance registers 2 (RKMR2) and 3 (RKMR3) only contain valid status messages following the execution of a Select command.

7.3 RK611 DISK COMMANDS

Disk commands are divided into two groups. One group (nondata handling) is concerned with the various operational requirements of the drive, while the second group (data or header handling) is concerned with the transfer of data or header information to or from a selected device. (Refer to Table 7-2.)

The controller recognizes a command by the configuration of the 4-bit command code (F4–F1) that is loaded into RKCS1. However, the command will not be decoded for execution until bit position zero (GO) of the register is set. In addition, two other RKCS1 bit positions are significant to command flow: The Ready (RDY) bit (bit 7) is set when the execution of a command is completed, and the combination Error/Clear (CERR/CCLR) bit (bit 15) will be set if a device or controller error occurs during execution. With these considerations and the simultaneous serialization of Message A and Message B (Figure 2-8a), using input derived from additional device registers, the disk commands can initiate the operations shown in Table 7-2.

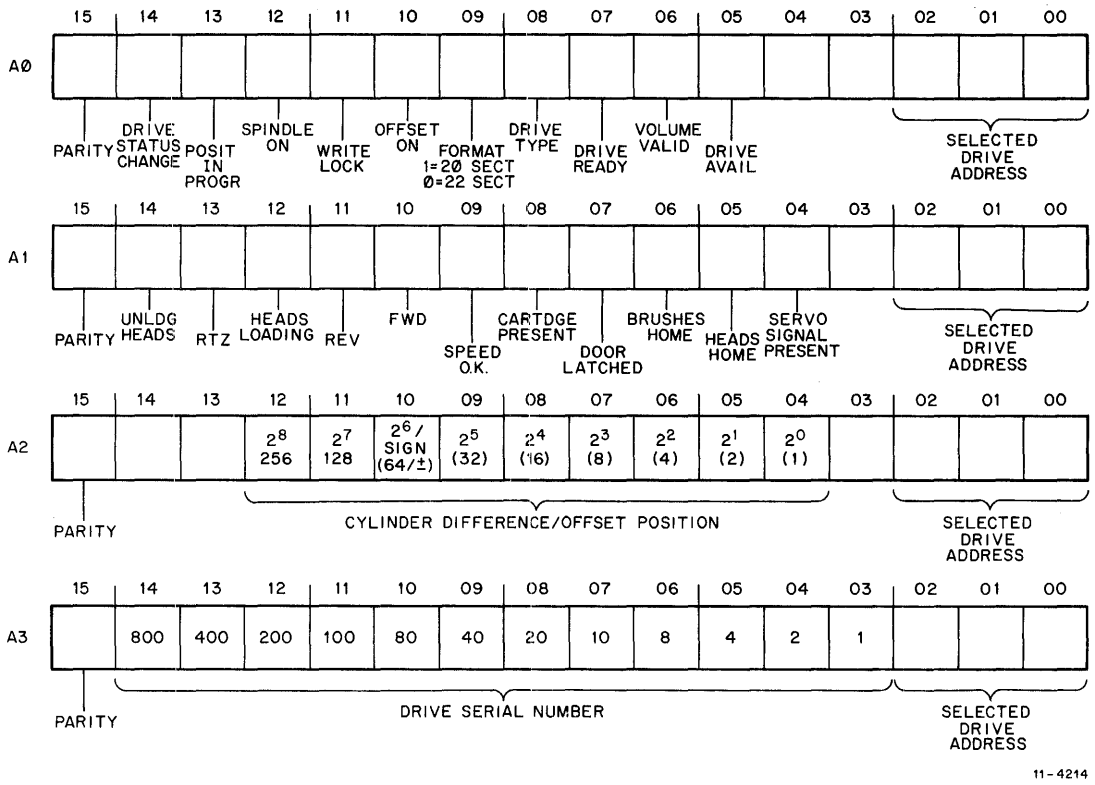


Figure 7-16 Maintenance Register 2 – Drive to Controller

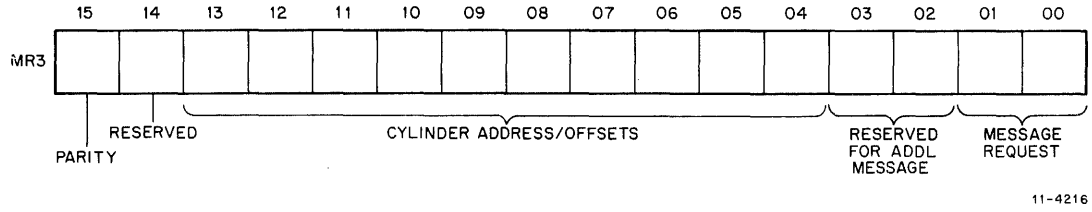


Figure 7-17 Maintenance Register 3 – Controller to Drive

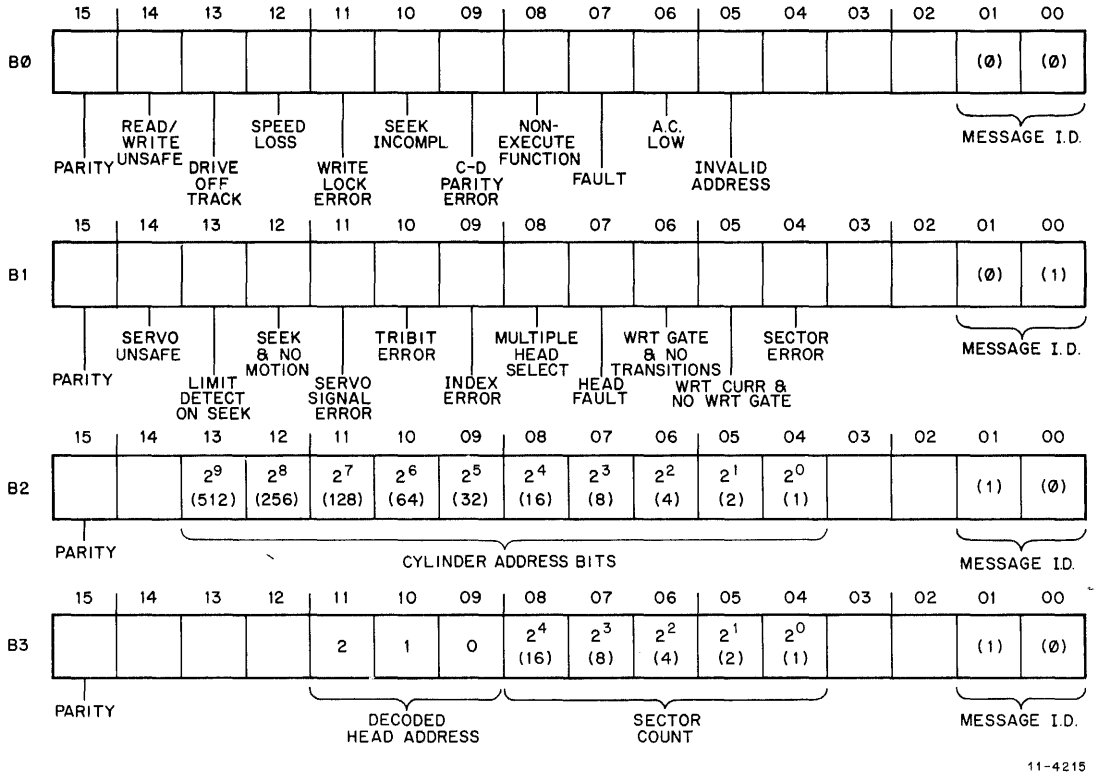


Figure 7-18 Maintenance Register 3 – Drive to Controller

Table 7-2 Disk Commands

Command	Function Code F4	F3	F2	F1	GO	Octal
Nondata Handling						
Select Drive	0	0	0	0	1	01
Pack Acknowledge	0	0	0	1	1	03
Drive Clear	0	0	1	0	1	05
Unload	0	0	1	1	1	07
Start Spindle	0	1	0	0	1	11
Recalibrate	0	1	0	1	1	13
Offset	0	1	1	0	1	15
Seek	0	1	1	1	1	17
Data or Header Handling						
Read Data	1	0	0	0	1	21
Write Data	1	0	0	1	1	23
Read Header	1	0	1	0	1	25
Write Header	1	0	1	1	1	27
Write Check	1	1	0	0	1	31

Select Drive (01) (Figure 7-19) – This command is basically used to select a drive and obtain the return of status information. This is accomplished by the setting of the Drive Select bits of Message A (T0–T2). However the command can also function as a release control to allow one of the dual ports of the selected drive to be freed for access by a second controller. The latter is accomplished by the setting of the Release bit of Message A (T3). When Messages A and B are sent, return status messages (A0 and B0) are requested. However, Select Drive is the only command with the ability to request (MS1, MS0) any one of the three pairs of additional message types (A1–A3 and B1–B3).

Pack Acknowledge (03) (Figure 7-20) – This command is used to set the Volume Valid flip-flop in a selected drive to indicate that the software has acknowledged the medium. This is accomplished by the setting of the Volume Valid bit in Message A (T11). When Messages A and B are sent, a return status is requested.

Drive Clear (05) (Figure 7-21) – This command is used to clear all error flags in the selected drive, provided the error(s) are no longer present. In addition, the command resets the Status-Change flip-flop in the drive. These actions are accomplished by the setting of the Drive Clear bit in Message A (T8). When Messages A and B are sent, a return status is requested.

Unload (07) (Figure 7-22) – This command is used to unload the heads in a selected drive and stop the spindle. This is accomplished by the setting of the Set Medium Off-Line bit in Message A (T10). When Messages A and B are sent, a return status is requested.

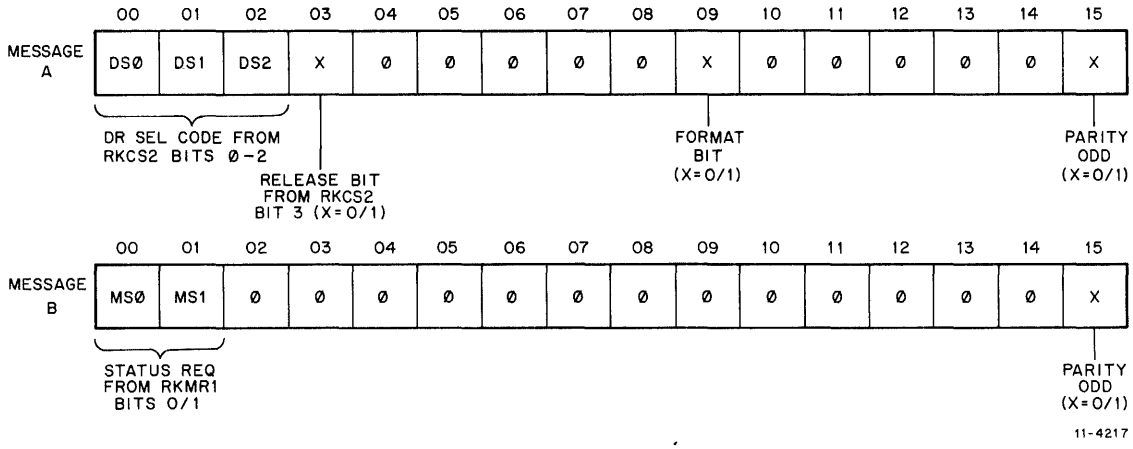


Figure 7-19 Select Drive Command

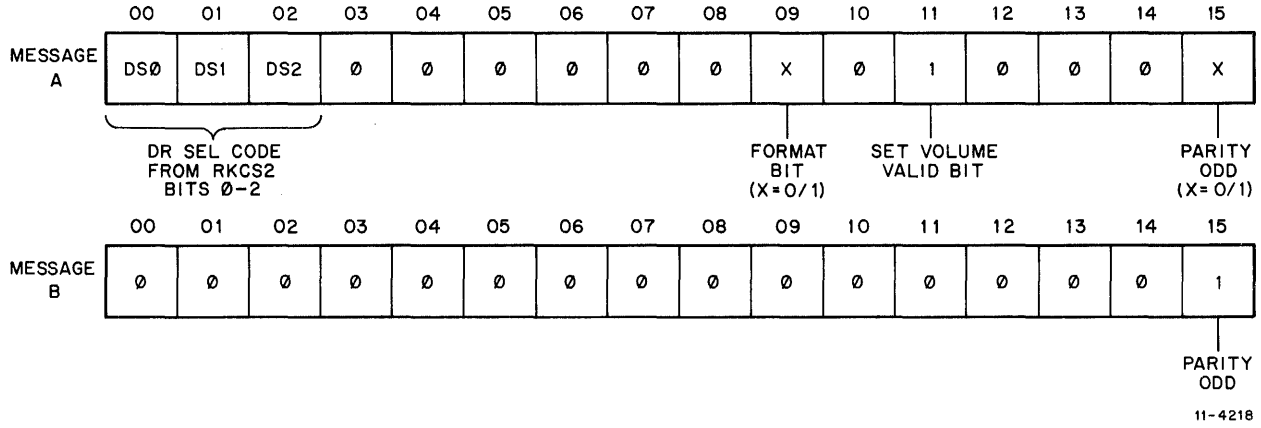


Figure 7-20 Pack Acknowledge Command

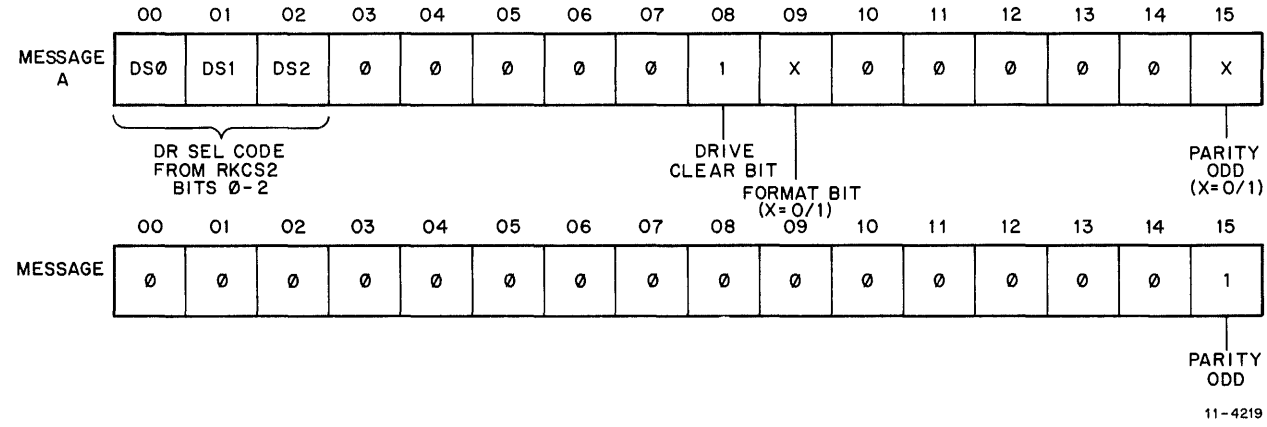


Figure 7-21 Drive Clear Command

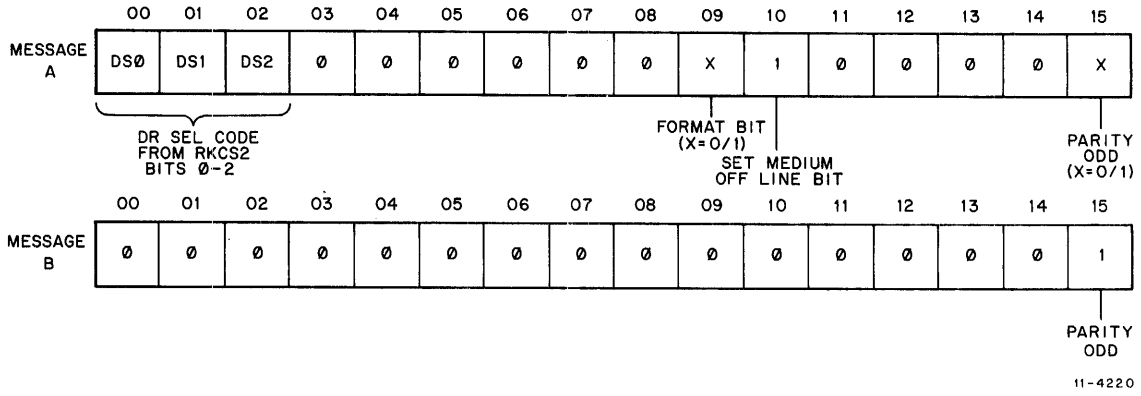


Figure 7-22 Unload Command

Start Spindle (11) (Figure 7-23) – This command is used to start the spindle, execute a brush clean cycle, and load the heads in a selected drive if the RUN/STOP switch is in a RUN state. This is accomplished by the setting of the Start Spindle bit in Message A (T6). When Messages A and B are sent, a return status is requested.

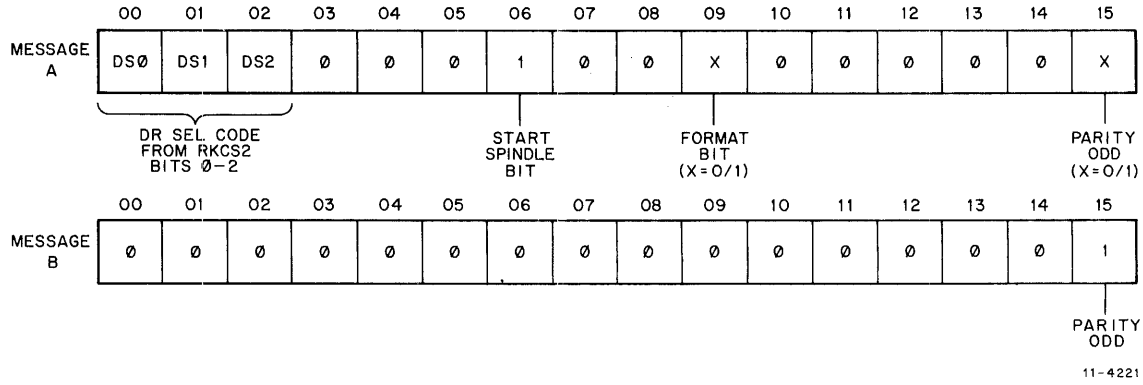


Figure 7-23 Start Spindle Command

Recalibrate (13) (Figure 7-24) – This command is used to relocate the heads to cylinder zero (address of the outermost cylinder on the disk) and to clear the drive's Cylinder Address register. This is accomplished by setting the Recalibrate bit in Message A (T5). When Messages A and B are sent, a return status is requested.

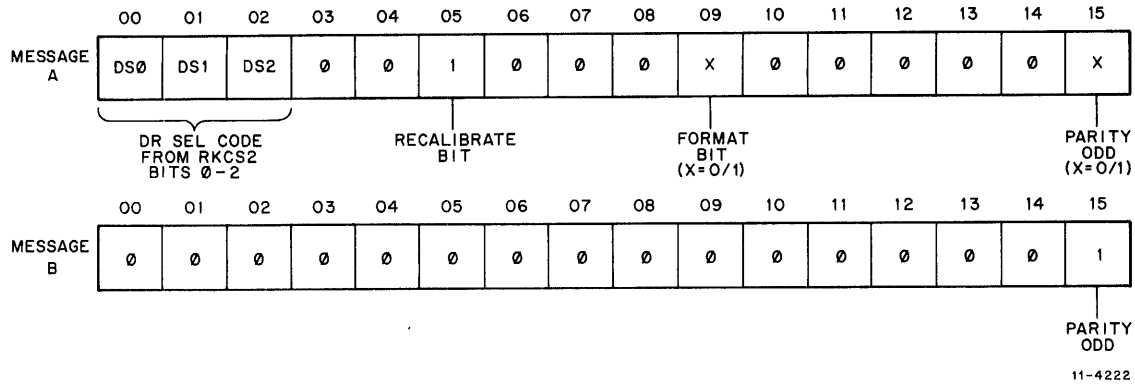


Figure 7-24 Recalibrate Command

Offset (15) (Figures 7-25 and 7-26) – This command directs the selected drive to position its heads a specified distance from the track centerline and to inhibit the recording logic. The distance (in micro-inches) and the direction (toward or away from spindle) that the heads are offset are determined by the value loaded into the Offset register (RKAS/OF). This is accomplished by configuring the Cylinder Address/Offset bits in Message B (T4–T12). When Messages A and B are sent, a return status is requested.

NOTE
Notice in Figures 7-25 and 7-26 that message bits are a reversal of register bits.

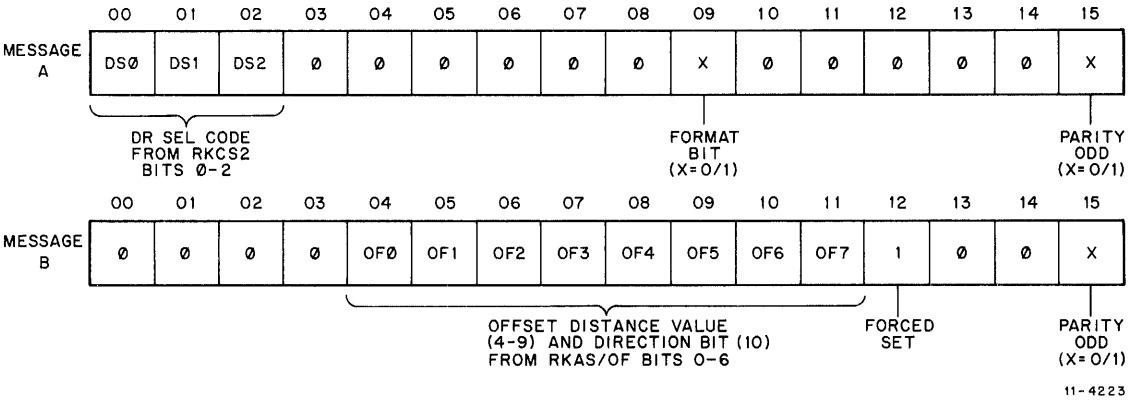


Figure 7-25 Offset Command

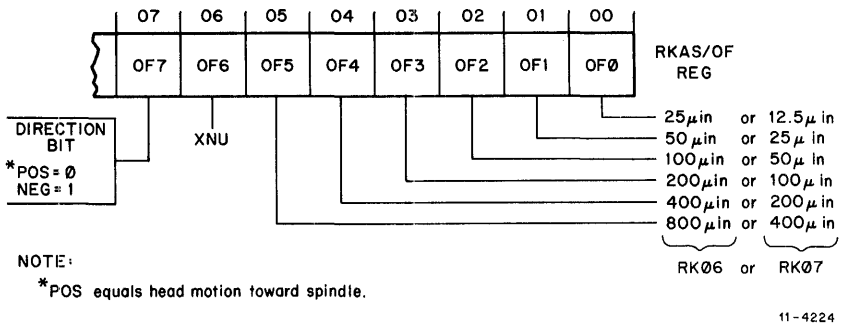


Figure 7-26 Offset Command Coding

Seek (17) (Figure 7-27) – This command directs the selected drive to relocate the heads over a new cylinder. The new cylinder address is derived from the Desired Cylinder register (RKDC). When Messages A and B are sent, a return status is requested. When the seek is completed, a drive Attention signal is asserted for polling.

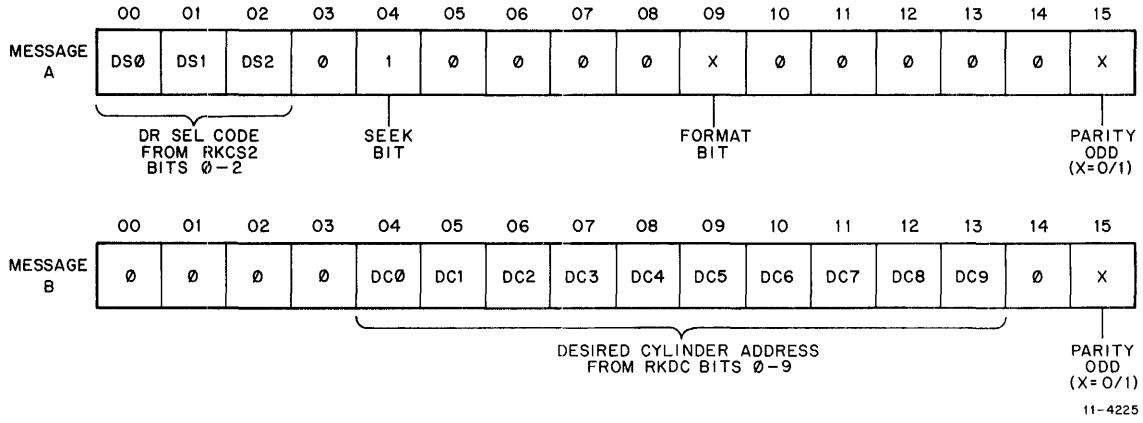
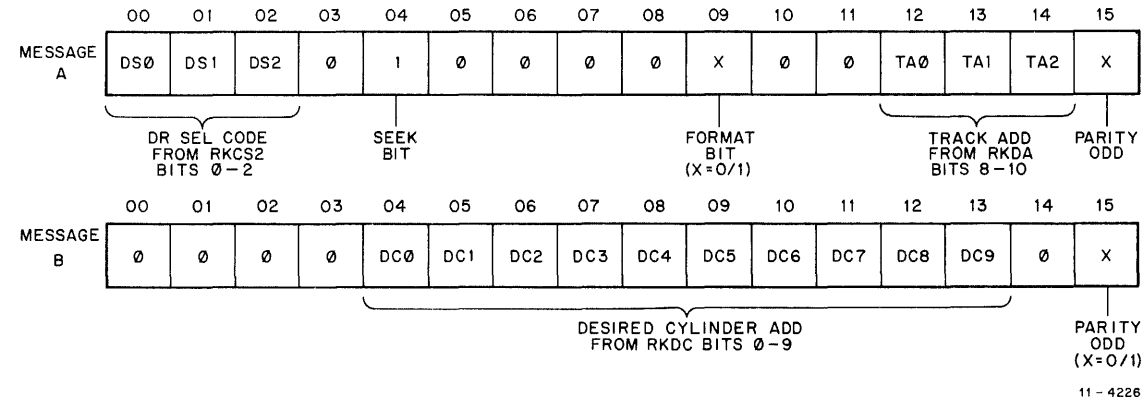
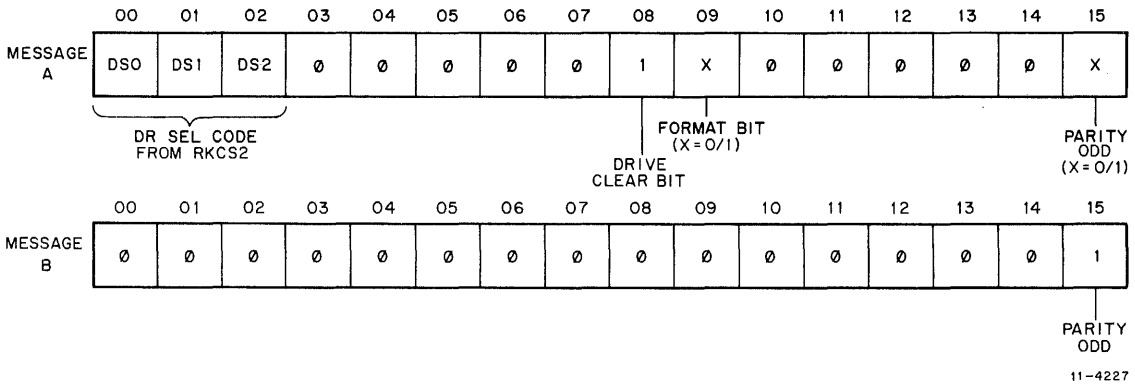


Figure 7-27 Seek Command

Read Data (21) – The following sequence is executed entirely by the RK611. A Seek to the cylinder in RKDC is performed. When the Attention signal from the selected drive becomes true, a drive status is requested. When the status is obtained, a Clear command is executed to clear the Attention signal. Headers are read and compared with the desired disk address until the correct sector is found. Transfer of data through the Silo data buffer to memory is initiated. When the sector data transfer is complete, the ECC logic is checked to ensure that the data read from the disk was error-free. If a data error occurred, the ECC correction algorithm is initiated to determine whether the error is correctable; when finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RKWC is checked; if nonzero, the data transfer operation is repeated into the next sector. The word count is checked at the end of each sector until it reaches zero, at which time the command is terminated by setting the Ready bit (Figure 7-28).



a. First Message



b. Second Message

Figure 7-28 Data Handling Commands

Write Data (23) – The following sequence is executed entirely by the RK611. A Seek to the cylinder in RKDC is performed. When the Attention signal from the selected drive becomes true, a drive status is requested. When the status is obtained, a Clear command is executed to clear the Attention signal. Transfer of data from memory to the Silo is begun, and headers are read and compared with the desired disk address until the correct sector is found. Preamble, Data (256 words), and ECC bits (32) are written on the disk. If the word count in RKWC goes to zero during the sector, the rest of the sector is zero-filled. After the sector transfer, the word count in RKWC is checked and, if nonzero, the data transfer operation is continued into the next sector. The word count in RKWC is checked at the end of each sector and, when it equals zero, the command is terminated by setting the Ready bit (Figure 7-28).

Read Header (25) – The following sequence is executed. A Seek to the cylinder in RKDC is performed. When the Attention signal from the selected drive becomes true, a drive status is requested. When the status is obtained, a Clear command is executed to clear the Attention signal. The three words of the first header encountered are read and placed in the Silo. The Ready bit is set. The three header words may now be retrieved by examining RKDB three times (Figure 7-28).

Write Header (27) – The following sequence is executed. A Seek to the cylinder in RKDC is performed. When the Attention signal from the selected drive becomes true, a drive status is requested. When the status is obtained, a Clear command is executed to clear the Attention signal. The RK611 then waits for Index from the drive. When Index is detected, zeros are written until sector pulse is detected. Then the header preamble, including sync 1 and the three header words are written. The all-zero gap, the data preamble (including sync 1) and all-zero data, ECC, postamble, and end-of-sector gap are written. This is repeated in each successive sector until Index is encountered again and the command is terminated. The Ready bit is set.

NOTE

All three words of the header (including the check word) are prepared by software and treated as data by the controller. Only one complete track can be formatted at a time. Either 20 or 22 headers (60 or 66 words) will be written depending on the state of the format bit (RKCS1 bit 12) at the beginning of the command. RKWC must be set to -60_{10} or -66_{10}, depending on format (Figure 7-28).

Write Check (31) – The following sequence is executed entirely by the RK611. A seek to the cylinder in RKDC command is performed. When the Attention signal from the selected drive becomes true, a drive status is requested. When the status is obtained, a Clear command is executed to clear the Attention signal. The selected drive provides data as in a Read command, and data is obtained from memory as in a Write command. The data are compared on a word for word basis until the word count reaches zero or until a failure to compare occurs. If the data fails to compare, the command is terminated immediately (Figure 7-28).

7.4 DIAGNOSTIC MODE (DMD)

When Diagnostic mode (DMD) is entered under program control, the drive interface lines are effectively disconnected from the controller, while the Unibus interface remains unchanged. Under these conditions, read/write commands (i.e., Read, Write, Read Header, Write Header, Write Check) can be initiated (using simulated data transfer techniques), while actual transmissions to and from the drives are disabled. In DMD, read/write commands are decoded normally, and messages are assembled in the shift registers for serial transmission. However, the output of each shift register is redirected to provide an alternate input to the opposite register, resulting in a message swap at the conclusion of a simultaneous transmission. Thus, message transmission to a drive is simulated by a message swap between shift register A (RKMR2) and shift register B (RKMR3).

Diagnostic mode is entered by the setting of the DMD bit in Maintenance register 1 (RKMR1), and subsequent operations are controlled and monitored by additional bits within the register. Data transfers are simulated by the continuous setting and resetting of the control bits (i.e., MCLK, MIND, MSP, MERD, PAT) in a predetermined sequence, while the program monitors the read-only bits (i.e., MEWD, WRTGT, RDGT, ECCW, PCA, PCD) for proper controller operation. In this manner, the data paths existing between main memory, the Silo, and the encoder/separator logic can be exercised and evaluated. In addition, since both read and write data originates in main memory and is effectively returned (directly or by monitor), a software comparison can be made to validate the integrity of the data paths.

Controller Modifications – In Diagnostic mode, the operation of the controller is modified by disabling the generation of certain error and control signals, while simulating and monitoring the generation of other signals, as follows.

Generation of these error conditions is inhibited:

1. Controller Time-Out (CTO) (bit 11 in RKCS1)
2. Programming Error (PGE) (bit 10 in RKCS2)
3. Unit Field Error (UFE) (bit 13 in RKCS2)
4. Drive Timing Error (DTE) (bit 12 in RKER)

Generation of these signals is simulated:

1. Index Pulse (MIND)
2. Sector Pulse (MSP)
3. Data/Control Clock (MCLK)
4. Read Data (MERD)
5. Even Parity (PAT) on Messages A and B (can only be done in real-time).

These signals are monitored:

1. Precompensation Advance (PCA)
2. Precompensation Delay (PCD)
3. Timing in ECC area of sector (ECCW)
4. Write Data (MEWD)
5. Read Gate (RD)
6. Write Gate (WRT)

Timing Considerations – The Maintenance Clock (MCLK) bit (bit 8 in RKMR1) can be alternately set and reset (by repeatedly loading RKMR1) to provide a program-controlled clock. Pulses generated by MCLK replace the data clock, used to control the transfer of data bits to and from the Encoder/Separator logic, and to generate control clock, used to synchronize message shifting operations. Predicating the generation of controller timing on the system clock allows a diagnostic program to monitor response conditions following the initiation of each write operation to RKMR1.

For the proper simulation of data transfers in Diagnostic mode, the following timing considerations must be adhered to (Figure 7-29).

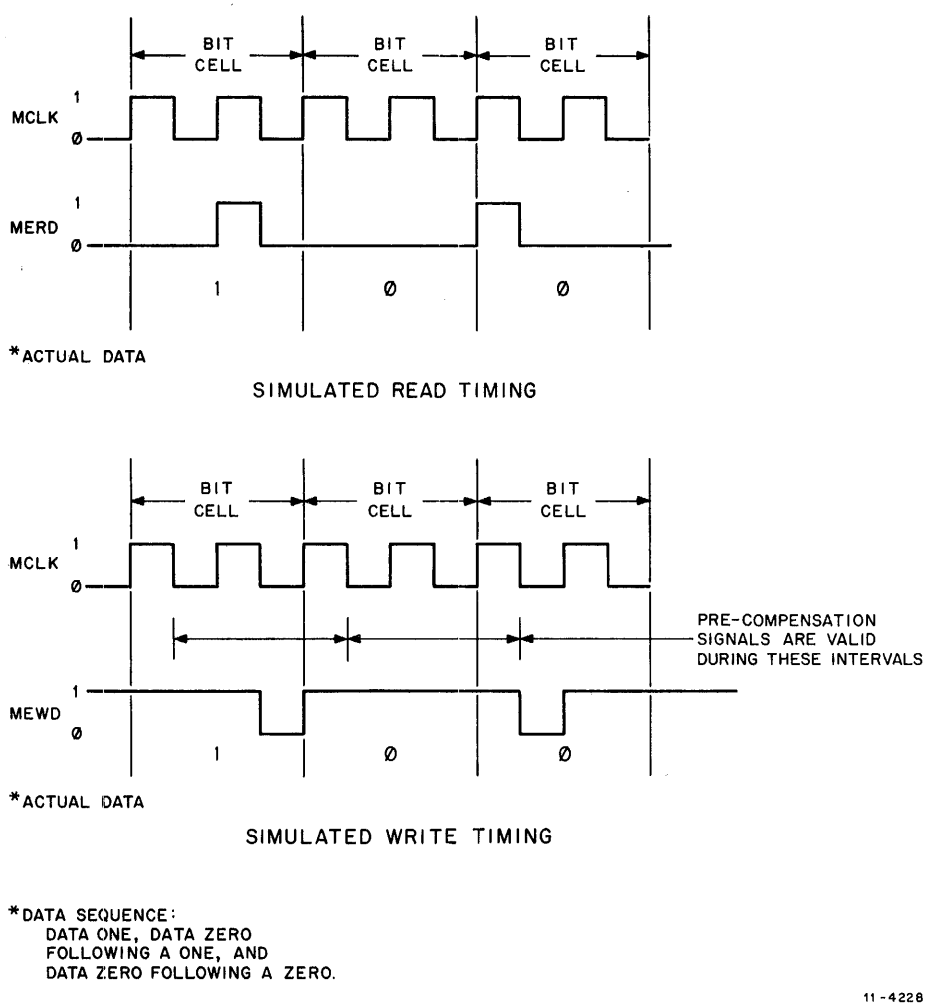


Figure 7-29 Maintenance Clock (MCLK) Timing

Data Clock

1. A set followed by a reset of the MCLK bit equals one data clock cycle.
2. Two data clock cycles are required to provide a bit cell for a single data bit (1 or 0); therefore, MCLK must be set and reset twice (1, 0, 1, 0).
3. A 16-bit word time is equal to 32 data clock cycles.
4. An 18-bit word time is equal to 36 data clock cycles.
5. An NPR time for a 16-bit word is equal to 37 clock cycles.
6. An NPR time for an 18-bit word is equal to 40 clock cycles.

Control Clock – One control clock cycle is equal to four times the duration of a data clock cycle; therefore, the MCLK bit must be set and reset four times (1, 0, 1, 0, 1, 0, 1, 0) to derive a control clock cycle.

Data Bit Simulation – To simulate read data transfers (Read, Write Check, Read Header), it is necessary to set and reset the Read Data (MERD) bit in conjunction with MCLK. A data bit of one can be simulated by the setting of the MERD bit. However, a data bit of zero can be simulated by either the setting or resetting of the MERD bit, depending on the condition of the previous data bit, i.e., a data zero following a one requires a reset condition, while a data zero following a zero requires a set condition.

To simulate write data transfers (Write, Write Header), the MERD bit is set and reset in conjunction with MCLK in the same manner described for read simulation. However for write data transfers, it is necessary to monitor the condition of the resultant Write Data (MEWD) bit.

7.4.1 Read Simulation

The following sequence of operations simulates the reading of a complete sector in Diagnostic mode.

1. With the exception of RKCS1, load the device registers required to support a normal Read command.
2. Set the Diagnostic mode (DMD) bit (bit 5 in RKMR1).
3. Load Command (F1–F4) bits (bits 1–4) and GO bit (bit 0) in RKCS1.
4. Toggle the Maintenance Clock (MCLK) bit (bit 8 in RKMR1) a sufficient number of times to assemble Message A (MR2) and Message B (MR3), and simulate transmission (message swap between MR2 and MR3).
5. Toggle (1, 0) the Maintenance Sector Pulse (MSP) bit (bit 6 in RKMR1) to simulate the generation of a sector pulse.
6. Toggle MCLK in conjunction with the Read Data (MERD) bit (bit 9 in RKMR1) to simulate the transfer of 128 of the 255 Header Preamble Zeros.
7. Check for the setting of the Read Gate (RDGT) signal (bit 15 in RKMR1).
8. Toggle MCLK in conjunction with MERD to simulate the transfer of the remaining 127 Header Preamble Zeros, concluding with the generation of a single One bit to reflect the SYNC bit.
9. Simulate the transfer of the three header words.
10. Simulate the transfer of the Gap bits (64 zeros).

11. If header compare is correct, following the simulation of 128 of the 255 Data Preamble Zeros, the RDGT signal bit will again be set and the remaining sector bits must be generated as follows:

    a. Remaining eight words of Data Preamble (127 zeros, 1 One bit)

    b. 256 words of 16- or 18-bit data (4096 or 4608 bits)

    c. Two words of ECC (32 bits)

    d. One word of Postamble (16 bits)

    e. Seven words of Gap (112 zeros) for 16-bit data or six words of Gap (96 zeros) for 18-bit data: both require approximately six NPR cycles (6 × 37 or 40 data clock cycles) to reach the end of a sector.

12. If the word count in RKWC is not equal to zero (indicating that another sector must be read), return to step 5 of the sequence and continue simulation. However, if the word count is equal to zero, 37 additional NPR cycles are required to complete the simulated transfers by unloading the Silo.

The 12 steps just described constitute a basic read simulation sequence. However, variations can be used to provide diagnostic information for error condition analysis or verification of the Error Correction Code (ECC) logic and its operation.

7.4.2 Write Simulation

The following sequence of operations simulates the writing of a complete sector in Diagnostic mode.

1. With the exception of RKCS1, load the device registers required to support a normal Write command.

2. Set the Diagnostic mode (DMD) bit (bit 5 in RKMR1).

3. Load Command (F1–F4) bits (bits 1–4) and set GO bit (bit 0) in RKCS1.

4. Toggle the Maintenance Clock (MCLK) bit (bit 8 in RKMR1) to produce the number of data clock cycles required to generate an NPR for each data word reflected by the word count in RKWC. For example, a WC value of 64_{10} will fill the Silo. Therefore, 64 NPR cycles must be generated to complete the operation (i.e., 37 data clock cycles times 64 for 16-bit data or 40 data cycles times 64 for 18-bit data, if the word count is greater than 64_{10}).

5. Toggle (1, 0) the Maintenance Sector Pulse (MSP) bit (bit 6 in RKMR1) to simulate the generation of a sector pulse.

6. Toggle MCLK in conjunction with the Read Data (MERD) bit (bit 9 in RKMR1) to simulate the writing of 128 of the 255 Header Preamble Zeros.

7. Check for the setting of the Read Gate (RDGT) signal bit (bit 15 in RKMR1).

8. Toggle MCLK in conjunction with MERD to simulate the writing of the remaining 127 Header Preamble Zeros, concluding with the generation of a single One bit to reflect the SYNC bit.

9. Simulate the reading of the three header words.

10. Simulate the Gap bits (64 zeros).

11. If header compare is correct, the Write Gate (WRTGT) signal bit (bit 14 in RKMR1) will be set, and the remaining sector bits may be written as follows:

    a. 16 words of Data Preamble (255 zeros, 1 One bit)

    b. 256 words of 16- or 18-bit data (4096 or 4608 bits)

    c. Two words of ECC (32 bits)

    d. One word of Postamble (16 bits)

12. If the number of data words to be written exceeds the length of one sector, return to step 5 of the sequence and continue; otherwise, write simulation is complete.

7.5 ERROR DETECTION AND CORRECTION

When a write data command (Write) is executed, a 32-bit Error Correction Code (ECC) is generated by the data and, following the recording of the data field, is written in the ECC field. When a read data command (Read, Write Check) is executed, the ECC field is also read to verify the integrity of the recorded data. If a read error is detected, the read function of the current command is disabled, and the ECC logic attempts to define both the position of the first error bit within the data field and the pattern of the error over an 11-bit range. If the data error is confined to no more than an 11-bit error burst, the error is correctable and the following indicators are set:

1. Data Check (DCK) error bit (bit 15 in RKER).

2. Controller Error (CERR) bit (bit 15 in RKCS1).

3. Ready (RDY) bit (bit 7 in RKCS1).

However, if the detected data error exceeds 11 bits, the error cannot be corrected and the following indicators are set:

1. Error Correction Hard (ECH) bit (bit 6 in RKER).

2. Data Check (DCK) error bit (bit 15 in RKER).

3. Controller Error (CERR) bit (bit 15 in RKCS1).

4. Ready (RDY) bit (bit 7 in RKCS1).

Thus, within less than one complete disk revolution, the program can determine if the error is correctable (DCK, CERR) or uncorrectable (ECH, DCK, CERR) via a check of the indicator bits. If the error is correctable, the ECC Position (RKECPS) register can be examined to determine the location of the first error bit within the error field, while the ECC Pattern (RKECPT) register can be examined to determine which of the 11 error burst bits must be corrected in main memory. In this regard, correction results from the exclusive-ORing of the 11 bits contained in the Pattern register with the 11 bits defined by the error burst (Figure 7-30).

However, if the error is detected as uncorrectable, the program can reread the error sector during subsequent disk revolutions, utilizing both ECC and head offset operations (if necessary) to improve the chances for an eventual correction and/or recovery. Thus, a standard data recovery routine consists of a sequence of 28 rereads, during which 16 ECC cycles are attempted at track center, and 12 ECC cycles are attempted in the six offset positions (two attempts per offset position).

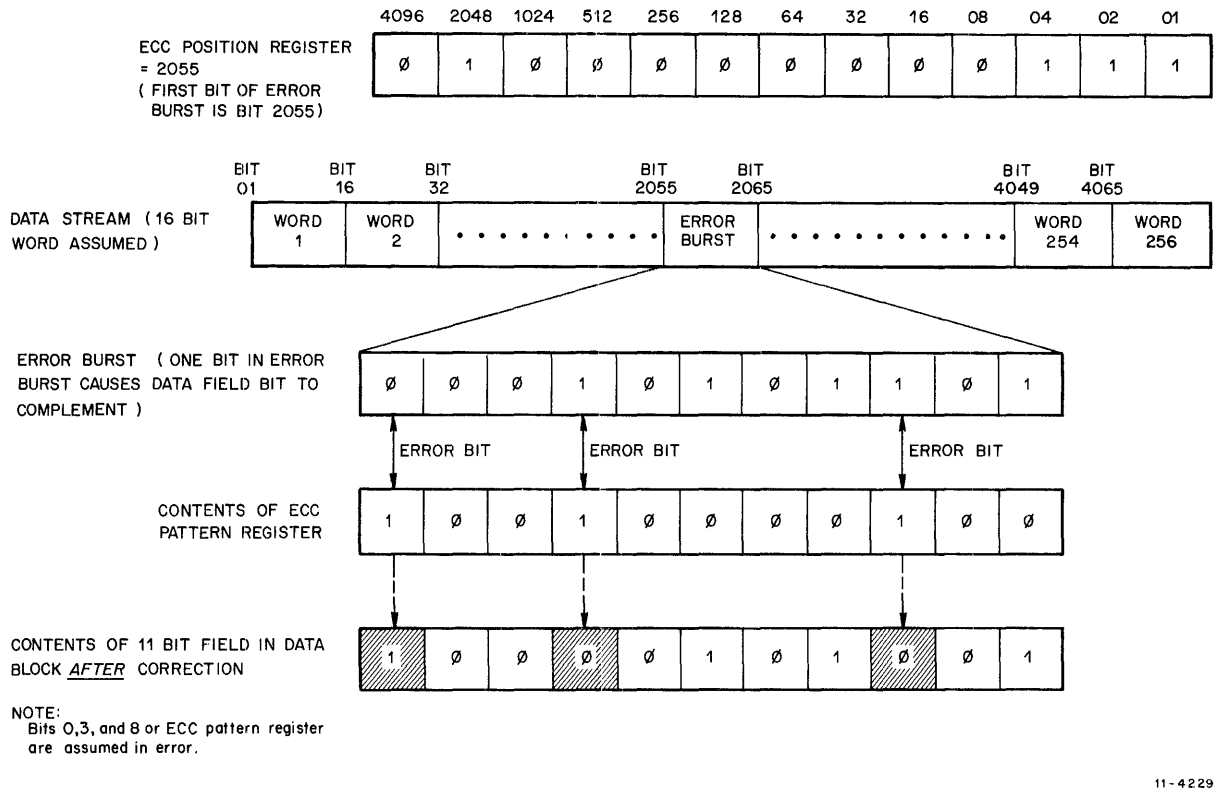


Figure 7-30 Error Correction Process

7.5.1 Correctable Error (DCK, CERR)

Figure 7-31 provides an example of the ECC correction process that is initiated by the controller when a correctable data error is detected (DCK, CERR).

In the example, an 11-bit error burst (bits 20–30) is detected in word 2 (bits 17–32) of a recorded data field. The 11-bit error burst, containing eight erroneous data bits (20–27), is delivered to main memory. Under ECC control, the RK611 loads the ECC Position (RKECPS) register with a value that is equal to the location of the first bit of the error burst (20_{10}). In addition, the ECC Pattern (RKECPT) register is loaded with an image of the 11-bit burst, that includes a One bit for every error bit (regardless of whether the error bit is an erroneous one or zero). Consequently, the program increments (through the Data field image area in main memory) a number of times that is equal to the value in RKECPS and locates the start location of the error burst. The error burst is then extracted from memory and exclusively ORed with the value contained in RKECPT. The result, including a complement of each of the eight error bits, is then returned to the 11 burst locations and the correction is complete.

One disk revolution is lost as a result of the execution of an ECC correction cycle. However, the Disk Address (RKDA) register has been incremented to the next sector. Therefore, only the GO bit (0) in RKCS1 must be reasserted to resume reading.

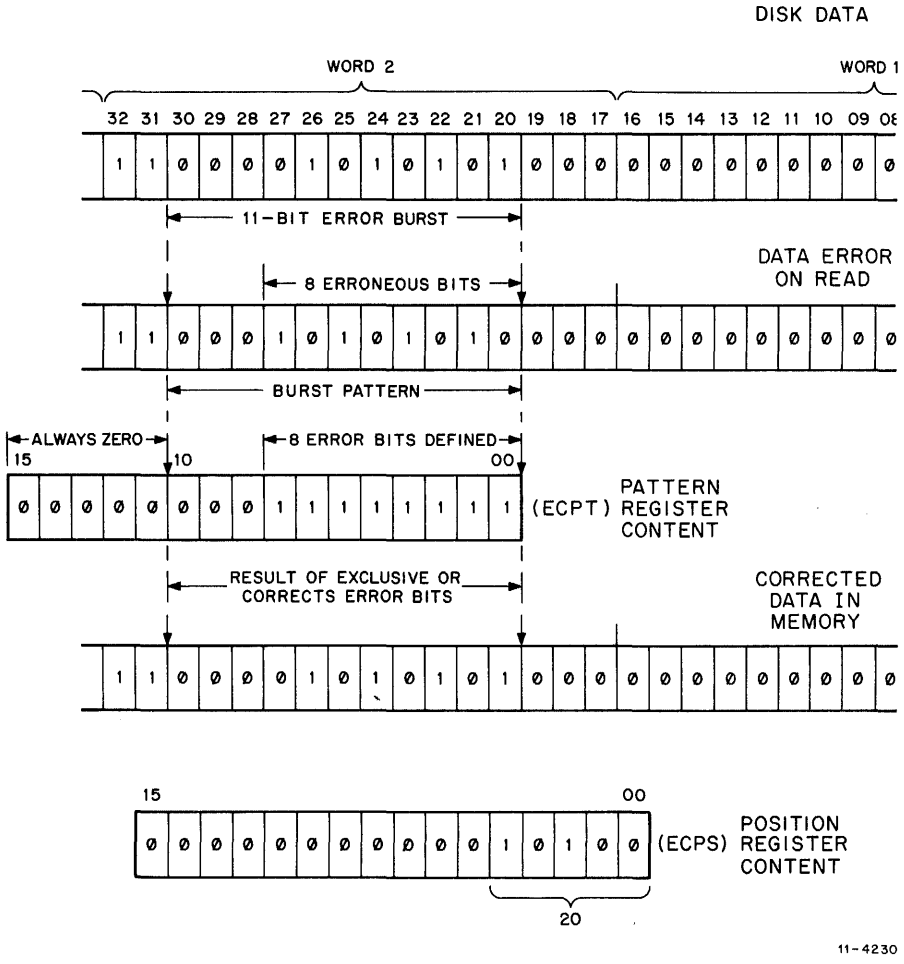


Figure 7-31 Example of 8-Bit Error Correction Process

7.5.2 Uncorrectable Error (ECH, DCK, CERR)

When an uncorrectable data error is indicated (ECH, DCK, CERR), an error burst has been detected that exceeds 11 bits in length—negating the value of the information contained in the ECC Position and Pattern registers. Under these conditions, the program must initiate a data recovery routine to provide a sequence of successive rereads (Figure 7-32).

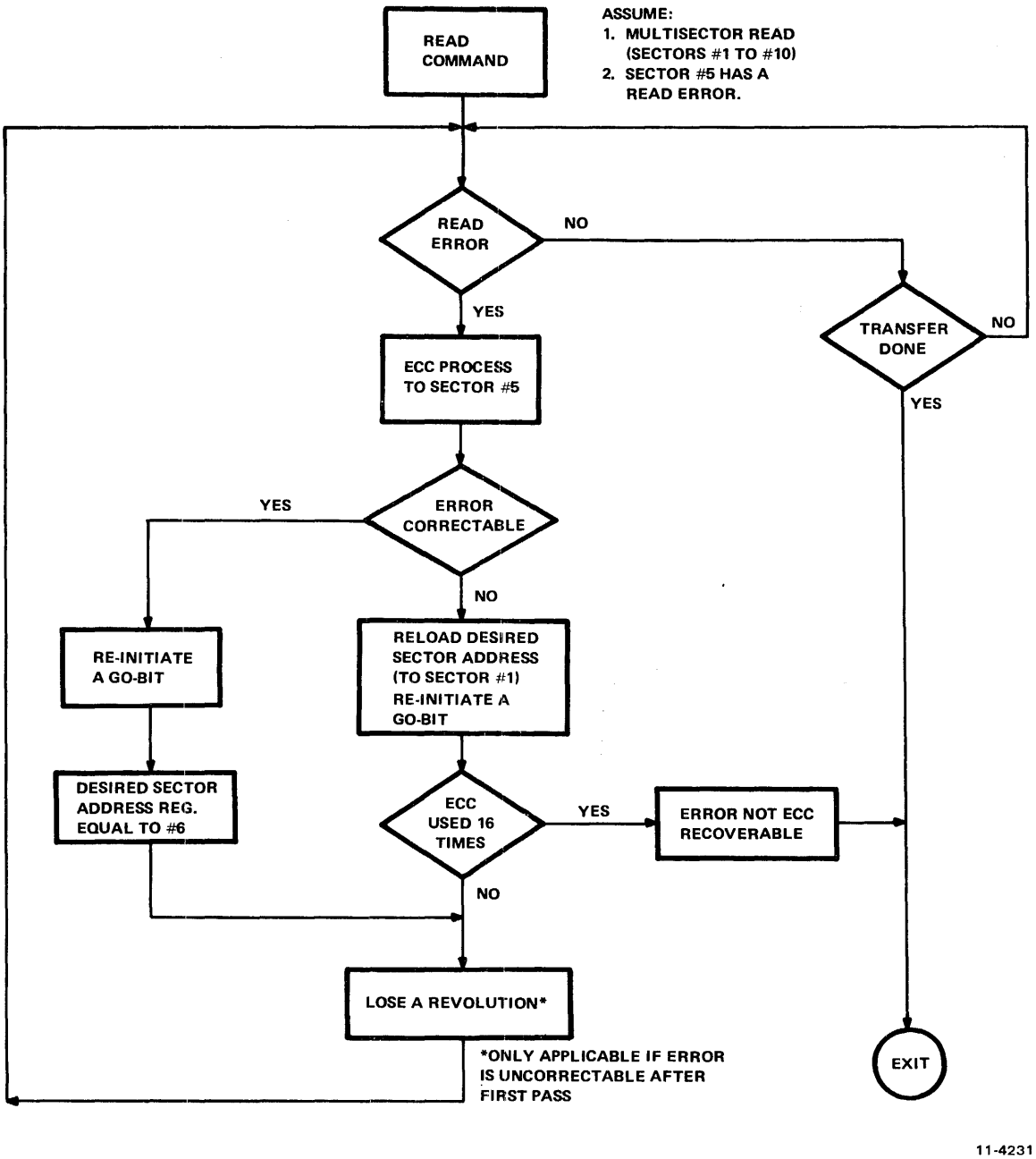


Figure 7-32 Data Error Flow

Any one of the 16 rereads at the track centerline could result in the recovery of data with or without an ECC correction cycle. Typically, this could occur if an error-producing material (e.g., dirt specks) either disappeared from that area of the disk surface or diminished to a point that allowed the data to become ECC-correctable.

If error data is recovered or corrected during any one of the 12 offset (±400, ±800, ±1200 for an RK06 or ±200, ±400, ±600 for an RK07) attempts (two rereads per offset position), it may indicate that the data on the entire track has been generated by a misaligned head. Under these conditions, it is possible that the remainder of the data will be recovered in the same offset position.

It should be understood that for every required reread cycle, the Disk Address (DA) register must be reloaded, and the GO bit (0) in RKCS1 reasserted. Thus a disk revolution is lost when an uncorrectable error is initially detected, and an additional revolution is lost every time a reread cycle is executed.

7.6 PROGRAMMING EXAMPLES

The following material provides several examples of RK06 subsystem programming, including Device Driver, ECC Correction, and Maintenance Register Read routines. RK07 subsystem programming is done in a similar manner.

7.6.1 RK06 Device Driver Routine

The RK06 Device Driver routine allows a user to establish communications with a device and determine subsystem status and availability.

```
,TITLE RK06 DEVICE DRIVER

;+
;CALLING SEQUENCE:
;       JSR   PC,RK06
;       DRIVE UNAVAILABLE RETURN
;       NORMAL RETURN
;
;INPUTS:
;       UNIT = DESIRED UNIT NUMBER IN BITS 0-2
;       DSKADR = TRACK/SECTOR ADDRESS
;       BUSADR = LOW ORDER 16 BITS OF UNIBUS ADDRESS
;       WCNT = TWO'S COMPLEMENT WORD COUNT
;       CYLADR = DESIRED CYLINDER ADDRESS
;       FUNCTN = DESIRED FUNCTION + IE + A16-A17
;       OFFSET = OFFSET VALUE FOR OFFSET FUNCTION
;
;OUTPUTS:
;       RK6ACT SET IF RK06 IS ACTIVE
;-
```

```
RKCS1=      177440      ;RKCS1 (base Unibus address)
RKCS2=      RKCS1+10    ;RKCS2
RKDS=       12          ;RKDS offset from RKCS1
RKER=       14          ;RKER offset from RKCS1
RKDC=       20          ;RKDC offset from RKCS1
RKOF=       16          ;RKOF offset from RKCS1
PACACK=     3           ;Basic Pack Acknowledge function
SELDRV=     1           ;Basic Select Drive function
SCLR=       40          ;Subsystem Clear
SVAL=       100000      ;Status Valid
DRDY=       000200      ;Drive Ready
VV=         000100      ;Volume Valid
DRA=        000001      ;Drive Available
UNS=        040000      ;Drive Unsafe
CERR=       100000      ;Controller Error/Controller Clear
DI=         040000      ;Drive Interrupt
IE=         000100      ;Interrupt Enable


UNIT:     .WORD  0      ;Desired unit # in bits 0-2
DSKADR:   .WORD  0      ;Track/sector address
BUSADR:   .WORD  0      ;Low order 16 bits of Unibus address
WCNT:     .WORD  0      ;Two's complement word count
CYLADR:   .WORD  0      ;Desired cylinder address
FUNCTN:   .WORD  0      ;Desired function + IE + A16-A17 + GO
RK6ACT:   .BYTE  0      ;1- if RK06 currently active
PROPRO:   .BYTE  0      ;1- if doing Seek/Recal/Offset function
OFFSET:   .WORD  0      ;Value to load into Offset register
```

```
RK06:   TSTB    RK6ACT                  ;Is the RK06 currently active?
        BNE     RK06                    ;Wait for it to become inactive
        MOV     #RKCS2,R2               ;Point to CS2 register
        MOV     #SCLR,($2)              ;Issue a Subsystem Clear
        MOV     UNIT,(R2)               ;Select the desired unit
        MOV     DSKADR,-(R2)            ;Load RKDA
        MOV     BUSADR,-(R2)            ;Load RKBA
        MOV     WCNT,-(R2)              ;Load RKWC
        MOV     #PACACK,-(R2)           ;Issue Pack ACK function
1$:     TSTB    (R2)                    ;Wait 15 μs for the serial message
        BPL     1$                      ;
        MOV     RKDS(R2),R1             ;Get Drive Status register
        COM     R1                      ;Complement bits
        BIT     #SVAL!DRDY!VV!DRA,R1    ;Can drive accept further commands?
        BNE     4$                      ;If NE no
        BIT     #UNS,RKER(R2)           ;Is this a Seek function?
        BNE     4$                      ;If NE yes
        MOV     CYLADR,RKDC(R2)         ;Load cylinder address
        CMP     #113,FUNCTN             ;Is this a recalibrate function?
        BEQ     2$                      ;If EQ yes
        CMP     #117,FUNCTN             ;Is this a Seek function?
        BEQ     2$                      ;If EQ yes
        CMP     #115,FUNCTN             ;Is this an Offset function?
        BNE     3$                      ;If NE no
        MOV     OFFSET,RKOF(R2)         ;Load offset value
2$:     INCB    POSPRO                  ;Indicate positioning command
3$:     ADD     #2,(SP)                 ;Show a good return
        INCB    RK6ACT                  ;Set RK06 active flag
        MOV     FUNCTN,(R2)             ;Load RKCS1
4$:     RTS     PC                      ;Return to users program

;INTERRUPT SERVICE ROUTINE

INTR:   MOV     #RKCS1,R2               ;Point to CS1 register
        TSTB    POSPRO                  ;Positioning in progress?
        BEQ     5$                      ;If EQ no
        BIT     #CERR!DI,(R2)           ;Positioning complete or error?
        BNE     5$                      ;If NE yes
        RTI                             ;Wait for positioning to complete
```

```
5$:     BIC     #CER!IE,(R2)        ;Clear IE without doing a CCLR
        CLRB    POSPRO              ;Reset positioning in progress
        TST     (R2)                ;Any errors?
        BMI     20$                 ;Yes, process directly
        TST     RKDS(R2)            ;Is current status valid?
        BMI     20$                 ;Yes it is
        MOV     #SELDRV,(R2)        ;Select drive to get fresh status
10$:    TSTB    (R@)                ;Wait 15 μs for the serial message
        BPL     10$                 ;
20$:    TST     (R2)                ;Any errors?
        BPL     40$                 ;If PL no
;+
;
;
;The user now handles any error conditions
;
;
;-
40$:    CLRB    RK6ACT              ;Set RK06 inactive
        RTI                         ;Return to user

        .END
```

7.6.2 ECC Correction Routine

The ECC Correction routine consists of three subroutines: the first determines if an ECC correction cycle is necessary; the second provides a set-up procedure; the third provides an ECC correction algorithm.

1. Determine if ECC correction is necessary:

```
35$:    BIT     #DLT!WCE!UPE!PGE!MDS!UFE,RKCS2    ;Controller error?
        BNE     RETRY                   ;Branch if controller error
        BIT     #SPAR!CTO,RKCS1         ;Controller time-out or message parity?
        BNE     RETRY                   ;Yes

        BIT     #DTE!HVRC,RKER          ;Drive timing or header error?
        BNE     RETRY                   ;Yes
        BIT     #ECH, RKER              ;Hard error?
        BNE     RETRY                   ;Yes
        TST     RKER                    ;Data check error?
        BMI     DMECC                   ;No, must be soft error
```

2. Error correction is accomplished in six steps:

   a. Calculate the byte offset to the start of the block transferred.

   b. Calculate offset to the first bad byte in the block.

   c. Convert correction pattern into two pattern words.

   d. Apply ECC correction using first pattern word.

   e. Apply ECC correction using second pattern word.

   f. Finish or continue previous function.

```
DMECC: MOV   RKWC,R0              ;Get negative words remaining
       ASL   R0                   ;Convert to bytes
       ADD   COUNT, R0            ;Calculate bytes actually transfered
       MOV   R0,-(SP)             ;And save it
       BEQ   DMOFST               ;Branch to do offset if no bytes transferred
       BIT   #HVRC,RKER           ;Header VRC error?
       BNE   40$                  ;Yes

       DEC   R0                   ;Calculate offset to start of block
40$:   BIC   #777,R0              ;Clear residue

       BIT   #DTE!ECH!HVRC,RKER   ;ECC Hard Error?
       BNE   DMOFST               ;Yes do offset

       MOV   RKECPS,R1            ;Get starting bit number
       DEC   R1                   ;Convert to relative bit number
       MOV   R1,-(SP)             ;Save starting relative bit number
       BIC   #↑C<17>,R1           ;Isolate shift count
       BIC   R1,(SP)              ;Clear shift count in relative bit number
       CLC                        ;Calculate offset to first bad byte in....
       ROR   (SP)                 ;...the block
       ASR   (SP)
       ASR   (SP)
       ADD   (SP),R0              ;Set offset to first byte in the transfer
       MOV   RKECPT,R3            ;Get correction pattern word
       CLR   (SP)                 ;Clear second pattern word
41$:   DEC   R1                   ;Any shifts to perform?
       BLT   42$                  ;If LT no
       ASL   R3                   ;This is in case the error burst...
       ROL   (SP)                 ;...crossed a 16-Bit word boundary
       BR    41$                  ;Continue shifting
42$:   CALL  DMECOR               ;Apply ECC correction
       MOV   (SP)+,R3             ;Retrieve second pattern word
       ADD   #2,R0                ;Update offset to next bad(?) Word
       CALL  DMECOR               ;Apply ECC correction
                                  ;Correction completed
                                  ;Finish or continue function
```

3. ECC Correction Algorithm – This routine calculates the memory address of the data word to be corrected and, using the supplied pattern word, performs an XOR of the pattern and data words.

```
DMECOR: CMP     R0,COUNT        ;Byte Offset Within Range?
        BHIS    50$             ;No

        MOV     ADRS,R1         ;Retrieve starting buffer address
        ADD     R0,R1           ;Calculate address of word to be corrected

        MOV     (R1),-(SP)      ;Prepare to do an XOR
        BIC     R3,(R1)         ;.NOT.pattern.AND.data word
        BIC     (SP)+,R3        ;.NOT.data word.AND.pattern
        BIS     R3,(R1)         ;Pattern.OR.data word
50$:    RETURN
```

7.6.3 Maintenance Register Read Routine

The Maintenance Register Read routine will transfer the content of the Maintenance registers (RKMR1, RKMR2, RKMR3) into a previously defined buffer; its address is in R0.

Maintenance Register Read:

R2 = Address of RKCS1

```
        CLR     R3
196$:   MOV     #100000,(R2)        ;Clear controller
MOV     UNIT,RKCS2(R2)              ;Reselect unit
        MOV     R3,RKMR1(R2)        ;Select drive serial message
        MOV     #1,(R2)             ;Issue select drive function
        TSTB    (R2)                ;Wait for the serial message
        BPL     .-2                 ;
        MOV     RKMR2(R2),(R0)+     ;Save content of MR2
        MOV     RKMR3(R2),(R0)+     ;Save content of MR3
        INC     R3                  ;Increment drive serial message count
        CMP     R3,#4               ;Done four messages yet?
        BNE     196$                ;No, loop
        RETURN
```

7.7 PROGRAMMING CONSIDERATIONS

The following provides a selection of programming information for the reader's consideration.

Flagging a Bad Sector

Since a Write Header command cannot be used to selectively write individual sectors, an entire track is written when the command is executed. Therefore, if a programmer desires to flag a bad sector, all currently recorded sector and data information from the desired track must be extracted and preserved elsewhere for rewriting along with the new information.

Unit Selection

When the Controller Clear (CCLR) bit (bit 15 in RKCS1) is asserted (via the Unibus), the Drive Select (DS0–DS2) bits (bits 0–2 in RKCS2) are cleared. Therefore, before the next command is initiated, unit selection must be reconfigured.

Start Spindle Command
If a Start Spindle command is initiated for a drive in which the heads have already been loaded, a controller interrupt can be returned on completion of the command, but an attention interrupt cannot be returned.

Unload Command
If an Unload command is initiated for a drive in which the heads have already been unloaded, a controller interrupt can be returned on completion of the command; but an attention interrupt cannot be returned.

Drive Error Unload/Reload
When a drive is in the RUN state and the heads unload due to a drive error (refer to Paragraph 7.2.6, Current Drive Attention - Bit 14), a successful error clear will result in a reload of the heads and the generation of two interrupts: the first interrupt will occur with the drive error, and the second interrupt will occur (up to 6 seconds later) when the heads reload.

Enabling an Interrupt
The Interrupt Enable (IE) bit (bit 6 in RKCS1) must be set prior to the initiation of an operation or an interrupt will not be generated.

Simultaneous Interrupts
If interrupt conditions simultaneously occur in the controller due to the overlapping of an operational and data transfer command (e.g., Seek done and Read Data done), the data transfer interrupt will take precedence and the operational interrupt will not be processed until another operation is completed. Therefore, to ensure that no interrupts are lost, a program should scan all interrupt indicators in conjunction with the recognition of an interrupt.

Drive Ready Requirement
A Seek, or any other head motion command, will be ignored by a drive if the Drive Ready (DRDY) bit is not asserted in the RKDS register when the command is initiated.

Dual-Access Operation
The programmer should be aware of a problem that can occur only with the Dual-Access Option. See Paragraph 9.4.3.

CHAPTER 8
CUSTOMER MAINTENANCE GUIDE

8.1 INTRODUCTION
User maintenance procedures are limited to the care and cleaning (external) of the RK06K or RK07K Disk Cartridge and the cleaning of the drive spindle assemblies.

8.2 PROFESSIONAL CARTRIDGE CLEANING
Professional cartridge cleaning is recommended every 6 months or whenever practicable. Complete cartridge cleaning procedures must be performed by either qualified DIGITAL Field Service personnel (in emergency or troubleshooting situations) or by a professional cleaning service. Application of cleaning procedures (to the actual recording surfaces) by unqualified personnel will void not only the warranty on the serviced cartridge, but the warranty for any drive on which the cartridge is operated.

8.3 USER CARTRIDGE CLEANING
The outer sides of a completely assembled cartridge may be cleaned by the user with a lint-free wiper, dampened with a solution of 9 percent water and 91 percent isopropyl alcohol. However, the cartridge must not be saturated, and all excess solvent must be removed with a dry wiper. This is necessary to prevent solvent from entering the seams of the assembly and contaminating the disks.

CAUTION

For cleaning purposes, use only a solution of 9 percent water with 91 percent isopropyl alcohol. Water, trichloroethylene, or other solvents are not permitted.

8.4 SPINDLE ASSEMBLY CLEANING
Using a lint-free wiper, dampened with the isopropyl alcohol (91 percent) solution, clean the spindle cone, magnet, and spindle rim (Figure 8-1), prior to the loading of a cartridge. However, do not saturate the assembly; remove all excess solvent with a dry wiper. This is necessary to prevent solvent from entering a loaded cartridge and contaminating the disks. In addition, ensure that the shroud is as free of lint and dust as possible before loading a cartridge. Dry lint and dust may be blown from the spindle area using filtered, dry air. However, do not use plant air which may contain water or oil; canned air is an acceptable substitute.

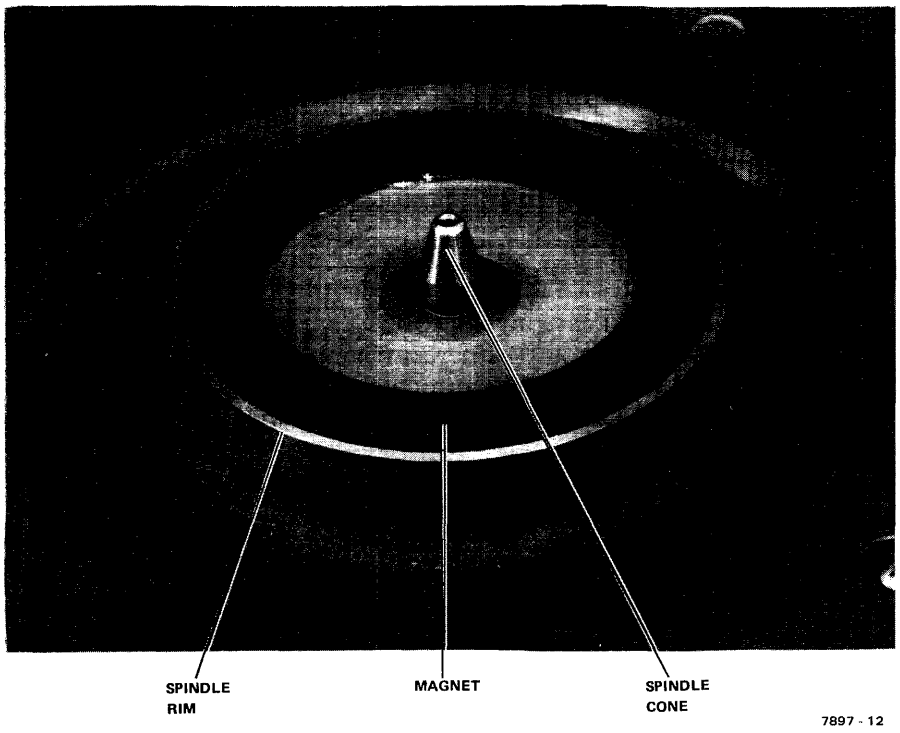


Figure 8-1 Spindle Assembly

8.5 CARTRIDGE CARE SUMMARY

The following listing summarizes care and cleaning considerations for the RK06K or RK07K Disk Cartridge:

1. Keep cartridges clean.

2. Use cartridges at computer room temperature only.

3. Manipulate cartridges by the top cover handle only.

4. When the protection cover is removed (for loading), do not touch disk surfaces, hub center cone, or surfaces.

5. When the protection cover is removed (for loading), interior metal hub surfaces must be clean.

6. When the protection cover is removed (for loading), ensure that the disks are not moved or rotated, since improper disk motion may generate plastic particles which can result in disk damage.

7. When loading or unloading an RK06 or RK07 Drive, insert and remove cartridges gently. In addition, do not use excessive force when manipulating the top cover handle.

8. If, during operation, a cartridge makes rumbling or continuous tinging sounds (or errors occur), discontinue use of the cartridge. Use of a damaged cartridge on other drives may damage the drives, resulting in additional damage to all other cartridges used thereafter.

9. Each cartridge should be professionally cleaned every 6 months and/or whenever a specific cartridge is not operating properly.

10. Cartridges are factory-repairable only. Disassembly in the field is not permitted, and such action will void the warranty on a cartridge, as well as any drive on which the cartridge may be operated.

CHAPTER 9
RK06/RK07 DUAL-ACCESS OPTION

9.1 RK611/RK06 and RK611/RK07 DUAL-ACCESS SYSTEM CONFIGURATION

Dual-access operation is an option available to the RK06 Drive enabling it to be accessed through two different controllers. Figure 9-1 shows the system configuration for dual-port operation. The eight RK06s or RK07s shown in Figure 9-1 are daisy-chained. The two RK611 Controllers can be attached to the same or to two different CPUs.

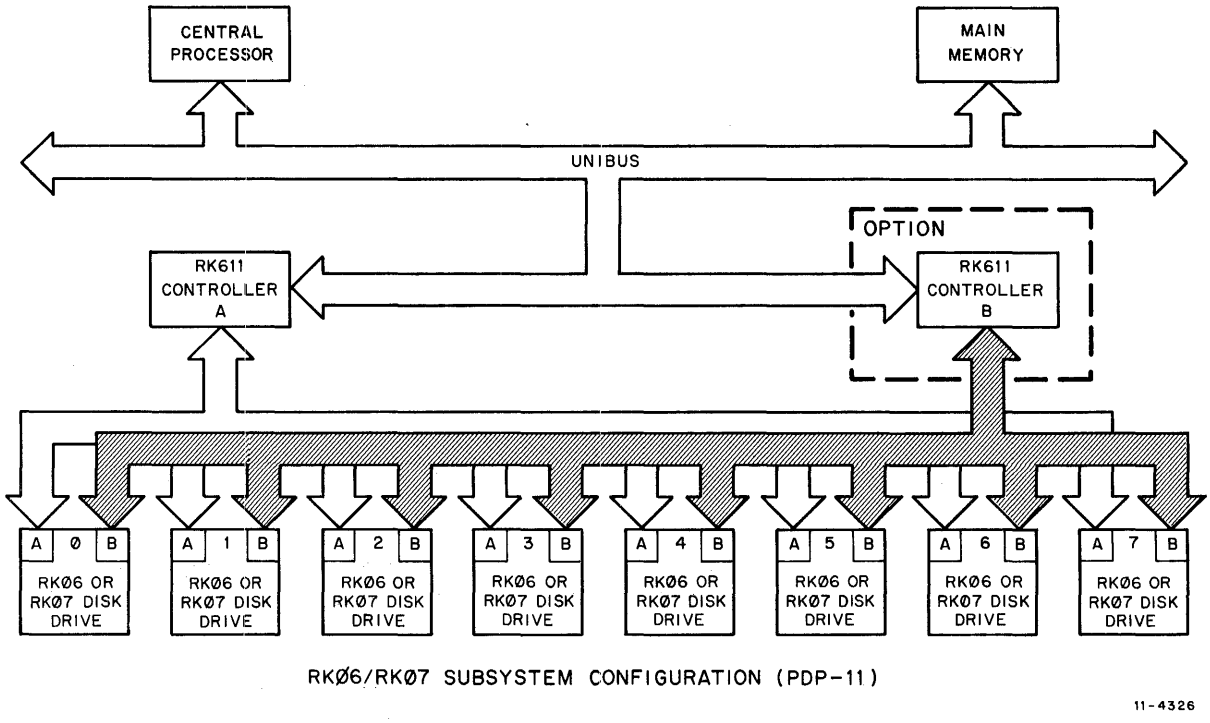


Figure 9-1 RK611/RK06 or RK611/RK07 Dual Access System Configuration

9.2 DUAL-ACCESS CONTROLS

A drive with the dual-access option has three modes of operation with respect to its two ports. Figure 9-2 shows the Port A and Port B control switches that determine which mode the drive is in. When these two switches are not pressed, all attempts to issue a command to the drive will generate a "non-existent drive" error in the controller issuing the command.

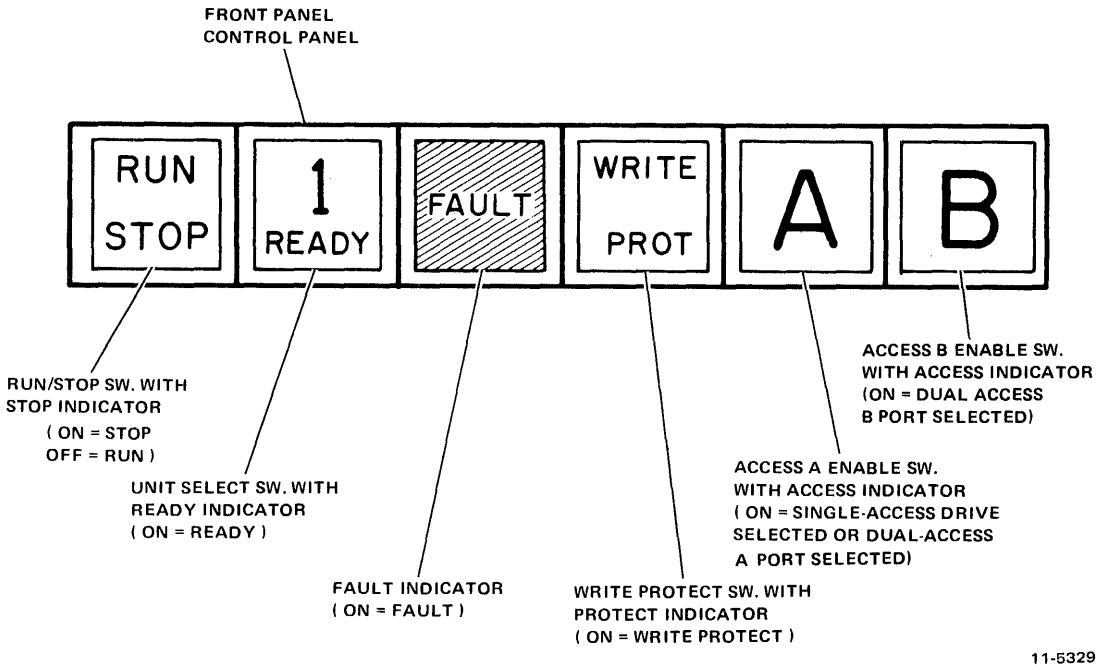


Figure 9-2 RK06 or RK07 Disk Drive Power and Control Switches

9.2.1 Port A Mode

With only the Port A enabling switch depressed, the drive will respond to Port A. Any attempt by Port B to issue a command to the drive will generate a "non-existent drive" error in the port B controller.

9.2.2 Port B Mode

With only the Port B enabling switch depressed, the drive will respond to Port B. Any attempt by Port A to issue a command to the drive will generate a"nonexistent drive" error in the Port A controller.

9.2.3 Dual-Access Mode

With Port A and Port B enable switches depressed, the drive is in the programmable mode. In this mode, the drive is initially available to both ports. Once the drive has been seized by one of the ports, that port has full control over the drive and can issue any legal command. A port seizes a drive if the controller selects the drive through that port and the drive was available.

9.3 DUAL-ACCESS LOGIC CIRCUITS

For the dual-access option, the drive houses two additional modules: an M7730 dual-port board and an M7706 interface and timing module. The two interface and timing modules interface with each controller. The dual-port board contains logic for controlling the access from both ports and acts as a multiplexer for commands and timing from each port to the remainder of the drive electronics. The dual-port option also uses a different backplane than the single-port option.

The logic for the dual-port option is located on the M7730 module and consists of:

1. Arbitration Circuits
2. Timing Counters and Decoders
3. Auto-Release Timer
4. Multiplexers.

9.3.1 Arbitration Circuits
These circuits determine and control the state of the multiplexers for operating the drive through the two ports.

9.3.2 Timing Counters and Decoders
These circuits control the timing of transmissions from the controller that has seized the drive.

9.3.3 Auto-Release Timer
This timing circuit generates a signal that will automatically release a port, if it has not been utilized within a one second period after it has gained access.

9.3.4 Multiplexers
These circuits act as a single-pole, double-throw switch for each signal used by a port for operation of the remainder of the drive.

9.4 DUAL-PORT OPERATION

9.4.1 Seizing a Drive in the Neutral State
When an RK06 or RK07 Drive is in the neutral state, it is equally available to each port. Neither port has priority over the other.

When a controller selects a drive, the drive will switch to the correct port to connect the drive with that controller.

If the two controllers simultaneously attempt to seize the drive, a high speed clock (in the dual port logic) in the drive will arbitrate, allowing only one of the controllers to seize the drive.

9.4.2 Attempting to Seize an Unavailable Drive
If a neutral drive is seized by a port and the other port attempts to seize the drive, the latter port will find the drive unavailable. This will assert the Combined Error bit in Control and Status Register 1 (bit 15 in RKCS1). Also, the Drive Available bit in the Drive Status Register (bit 0 in RKDS) will be cleared as a result of a port attempting to seize an unavailable drive.

In addition to clearing bit 0 in RKDS, a port attempting to seize an unavailable drive will set the port request flip-flop in that drive. The dual port logic checks the status of this flip-flop when the controller currently operating on the drive releases the drive. If the port request flip-flop is not set, this indicates that the port other than the one just in use did not attempt to seize the drive. The drive then returns to the neutral state and it may then be seized by either port. If, however, the port request flip-flop is set, this means the other port attempted to seize the drive when it was unavailable. In this case, the other port seizes the drive.

For example, assume Port A controls the drive. Port B tries to seize the drive and finds the drive unavailable. Thus, the Port Request flip-flop is set. When Port A is finished with the drive, it releases the drive with a release command. Since the Port Request flip-flop is set, Port B then seizes the drive.

9.4.3 Caution in Issuing a Release Command to an Unavailable Drive

The programmer should be careful, when designing software for use with the dual port option, to avoid the following problem. Assume Port A has seized the drive, and Port B attempts to seize it and finds it unavailable. Suppose Port B then attempts to cancel its port request. If the release command from Port B is completed before Port A actually releases the drive, there is no problem. If, however, Port A releases the drive while Port B is still in the process of issuing a release command, the Port B controller will find the attention asserted. The assertion of attention should have been prevented by the release of Port B. This race condition can be avoided by not allowing a port to release its port request to an unavailable drive.

9.4.4 Auto-Release Timer

At the initiation of every command to the drive by the port that has access, a one second release timer is started. (The exception to this is the release command.) This timer is restarted with every new command issued by the controller having access to the drive. If a port accessing the drive does not release the drive and the one second release timer times out, the other port's port-request flip-flop will be examined. If it is reset, the drive will go back to the neutral state. If the other port's port-request flip-flop had been set, the following events take place.

1. The drive becomes *deselected* from the port that had access.

2. The drive is *effectively* seized by the other port.

3. The other port's attention is asserted, signifying that the drive is now available.

9.5 START/STOP AND WRITE PROTECT IN DUAL ACCESS

When ac power is first applied to the RK06 or RK07, the drive is initially in the neutral state. The volume valid bit for each port is cleared. A pack acknowledge command is required for each port.

The drive will not seek or write through a port unless that port has its Volume Valid bit set.

If a port issues the Unload Heads command, the one second auto-deselect timer is disabled. This has been instituted to allow a change of cartridge and not have the drive return to the programmable state. If the drive were allowed to return to the programmable state after an unload command, the other port could seize the drive and issue a conflicting command.

Once the drive is cycled up, the completion of the head-loading sequence asserts the attention bit of the port having access to the drive. For one additional second, the drive will be seized by that port.

The port having access must issue a command to the drive within this time. Failing to issue a command within this time will cause the dual-port logic to examine the other port's Port Request flip-flop. If the flip-flop is not set, the drive will return to the neutral state. If the flip-flop is set, the drive will become seized by the other port and the other port's attention will be asserted.

If the drive is unavailable to a port and the RUN/STOP switch is changed, the port is notified by the assertion of its attention. The change is reported to the controller though the "spindle on" status bit.

When Write Protect is asserted, neither port will be able to do a write operation. There is no provision to Write Protect the drive through one port and not have it Write Protect through the other.

If the drive is seized to a port and the operator changes the status of the write protect switch, the other port is notified through the assertion of its attention. The change is reported to the controller through the Write Lock Status bit.

9.6 ERROR HANDLING IN DUAL ACCESS

9.6.1 Notifying the Controller of an Error

Errors occurring while the RK06 or RK07 is seized by one of the controllers are reported to and should be serviced by that controller. The other port is not notified of these errors. The exception is a parity error in a message to the drive on the other port.

If the drive had been in the neutral state and an error occurred, both Attention bits would be asserted. The fault bit would be read by both controllers when servicing the Attention set in the drive. However, only one of the controllers would service the error in the drive.

9.6.2 Clearing the Drive Errors and Resetting the Attention

Either controller may issue a drive clear at any time. The Attention in the drive will be cleared by a drive clear regardless of the drive's availability. However, to clear the flip-flops storing the error information, the drive must be seized to the port issuing the Clear command as mentioned. The controller-to-drive parity error is handled differently from the other errors and is discussed in greater detail as follows.

9.6.3 Multiple Drive Select and CTD Parity Errors in the Dual-Access Configuration

If a controller has seized a drive and multiple drive select is detected in the drive, the drive handles this as an unsafe condition and unloads the heads.

If a controller has seized a drive and multiple drive select is detected on the other port, the drive detects the condition but does not set fault and unsafe and does not unload the heads. The port detecting multiple drive select reports it to the controller regardless of whether it had access to the drive.

Controller-to-drive (CTD) parity errors are detected and stored separately for each port. Unlike all other errors, the CTD parity error flip-flop is cleared with a Drive Clear regardless of whether or not that controller has seized the drive. The Attention in the port is raised when a CTD parity error occurs.

9.7 INITIALIZE IN DUAL ACCESS

The RK06 or RK07 will honor an "initialize" issued separately from either port. The effect the "initialize" has depends upon the availability of the drive to the port issuing the command. The three drive conditions are described.

1. The drive is seized by a port. At this time, an initialize will:

   a. Clear that port's attention bit

   b. Clear the error flip-flops in the drive

   c. Cause the port to release the drive.

   If the other port's port-request flip-flop is cleared, the drive will be returned to neutral. If the other port's port-request flip-flop is set, the drive will become seized by the other port.

2. The drive is in neutral. At this time, an initialize will:

   a. Clear the port's attention bit

   b. Clear the error flip-flops in the drive.

3. The drive is seized by the other port. At this time, an initialize will:

   a. Clear the port's attention bit

   b. Cancel the port request if one is pending.

9.8 GETTING DRIVE STATUS IN DUAL-ACCESS MODE

If the drive is seized by one of the ports, that port's controller may interrogate any of the eight status multiplexers (A0, B0, A1, B1, A2, B2, A3, B3) within the drive.

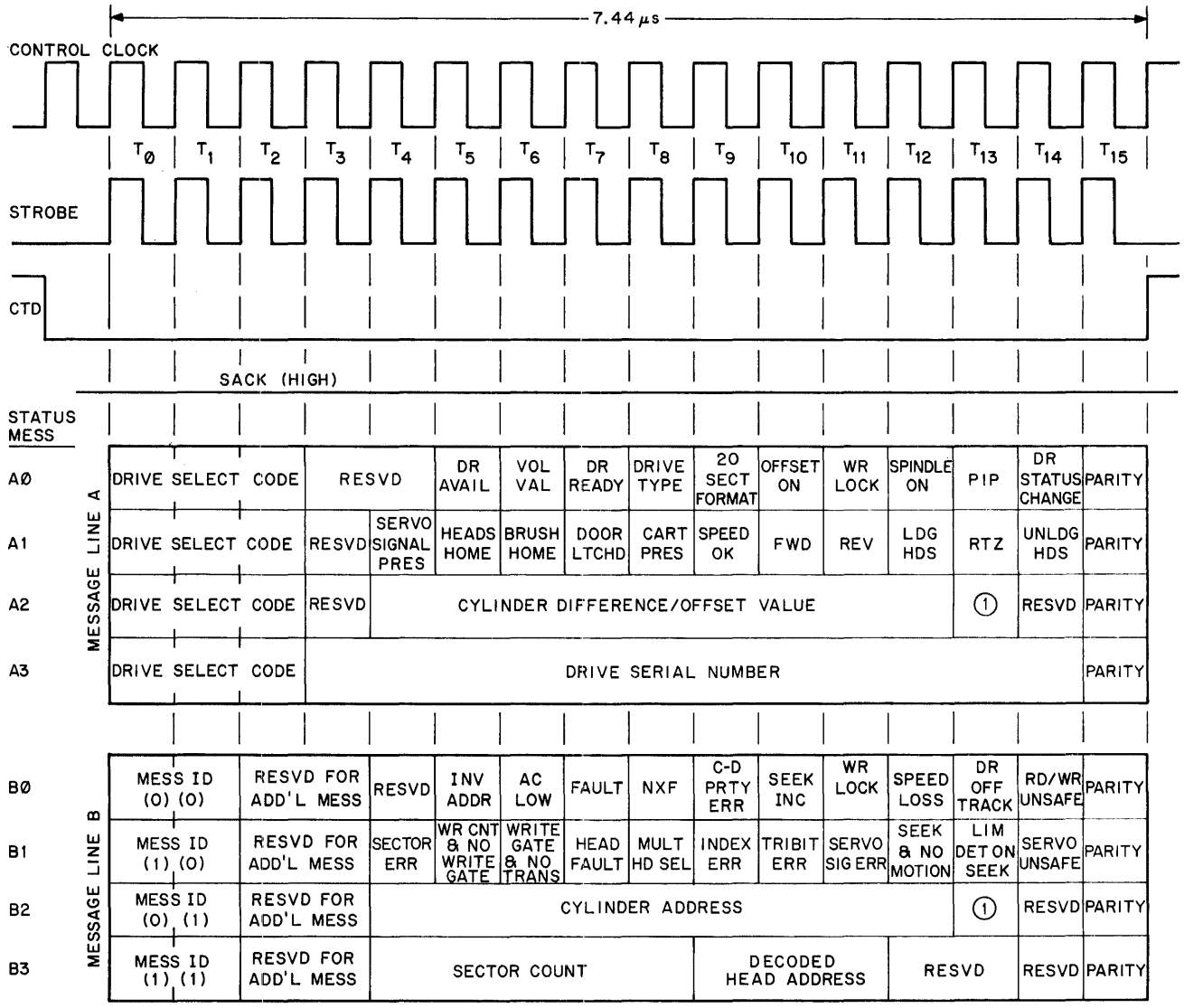
If the drive cannot be seized (busy with another port), only status multiplexers A0 and B0 may be read through the unseized port. This situation causes the Combined Error bit (bit 15 in RKCS) to be asserted in the controller of the unseized port. Refer to Figure 9-3 for the data bits contained in drive status messages A0 through B3.

9.8.1 Status Bits Pertinent to the Dual-Port Available at the Unibus Interface

1. **Drive available (DRA)** – This bit is set to the port that has access to the drive and reset to the other port. Read only.

2. **Volume Valid (VV)** – This bit is used to indicate when a disk cartridge may have been changed. There is a Volume Valid bit for each port.

3. **Ready (RD)** – Indicates that the selected drive is up to speed and its heads are settled over the specified cylinder. This bit will always be reset to a port not having access to the drive.



B.) DRIVE-TO-CONTROLLER TRANSMISSIONS

NOTE:
(1) – THESE BITS ARE USED ONLY ON THE RK07.

11-5328

Figure 9-3 Drive Status Bits Contained in A and B Messages

RK06/RK07 DISK DRIVE
USER'S MANUAL

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