INDUSTRIAL PRODUCTS

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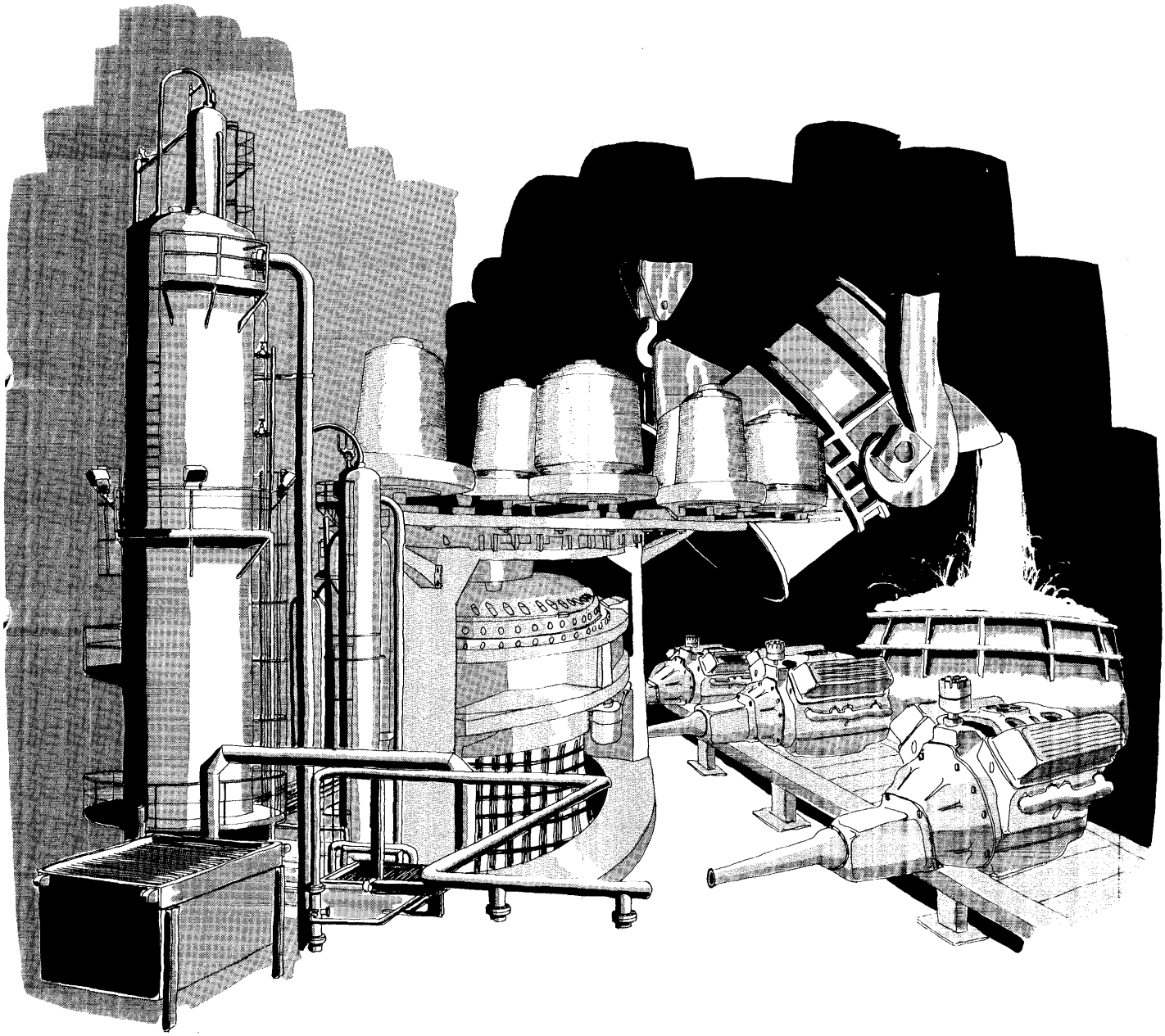
I/O SUBSYSTEM
USER GUIDE



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USER GUIDE

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FIGURES

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CHAPTER 1
GENERAL INFORMATION

1.1 SCOPE

This manual provides a complete description of the I/O Subsystem, including physical and functional level descriptions, installation instructions, programming information, and maintenance procedures.

1.2 GENERAL DESCRIPTION

The I/O Subsystem is a cabinet-mountable subsystem that monitors and/or controls industrial operations and equipment. The subsystem is a highly flexible input/output device capable of interrogating and driving digital and analog systems. The device interfaces with the LSI-11 or any other PDP-11 family computer. It provides real-time monitoring and control capability with minimal computer overhead. Applications range from simple monitoring functions to control of complex closed-loop systems. Environmental monitoring and control, batch mixing, material handling, quality control, and testing are but a few of the many applications for which the I/O Subsystem is suited.

Because of the modularity of the device and the various types of I/O modules offered, the I/O Subsystem is adaptable to many different applications. The subsystem may contain a few or as many as 8Ø I/O modules that are available to perform the following functions.

Inputs	Outputs
DC voltages	DC switching
AC voltages	AC switching
Change of state	One-shot dc switching
Contact closure	D/A conversion
A/D conversion	Pulse trains
Event counting	
Frequency measurement	

Each I/O module handles one or more bytes (eight bits) of I/O data.

Communication between the I/O modules and the processor is via a control module that interfaces their respective buses (Figure 1-1). These modules and buses are defined as follows.

H333 I/O Bus (D-bus)
This bus is etched on the lower half of the printed circuit backplane in the I/O area of all module chassis. All I/O modules and the I/O control module interface with this bus when plugged into the backplane connectors.

LSI-11 Bus
The LSI-11 bus is included only in the H333 chassis. It is etched on the upper half of the chassis backplane for all module positions and on the lower half for the first four module positions. This bus interfaces with all LSI-11 option modules including the I/O control module.

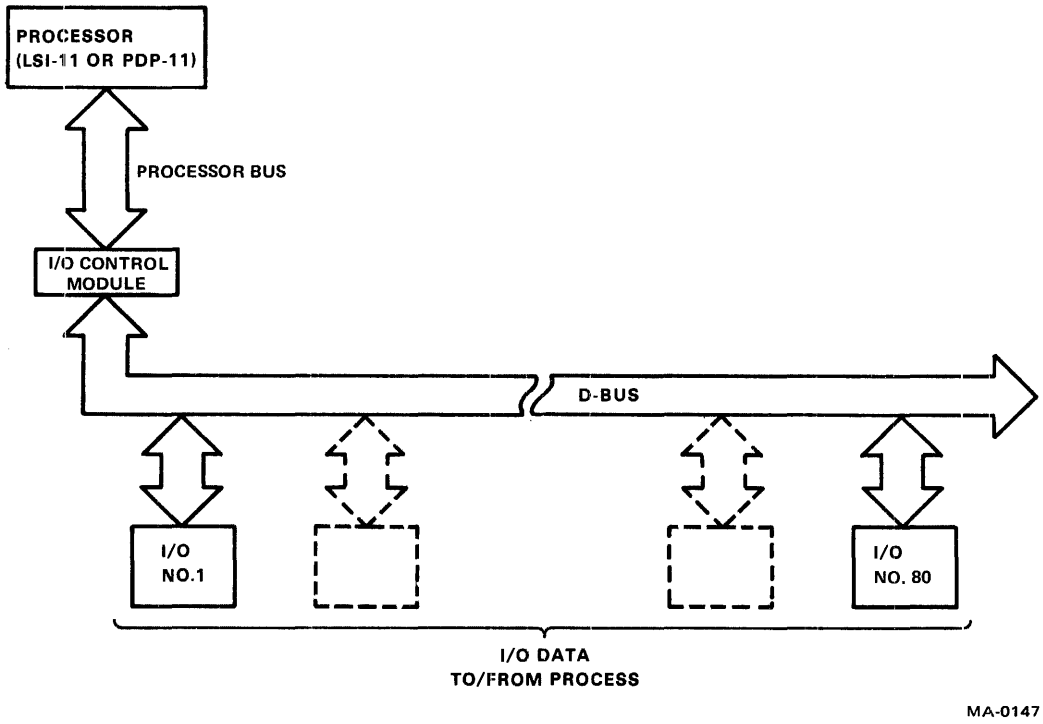

Figure 1-1 Processor I/O Interface

M8719 I/O Control Module
The M8719 interfaces with the UNIBUS via its etched edge connector, and with the D-bus via a cable connector on the opposite edge of the module. This module performs the data routing and control functions that provide communication between the I/O modules on the D-bus and the processor on the UNIBUS.

M7959 I/O Control Module
The M7959 interfaces with the LSI-11 bus via its etched edge connector, and with the D-bus via a cable connector on the opposite edge of the module. This module performs the data routing and control functions that provide communication between the I/O modules on the D-bus and the processor on the LSI-11 bus.

M7958 I/O Control Module
The M7958 interfaces with the LSI-11 bus on the top half of its etched edge connector and with the D-bus on the bottom half. This module performs the data routing and control functions that provide communication between the I/O modules on the D-bus and the processor on the LSI-11 bus.

I/O Modules
All I/O modules interface with the D-bus via an etched edge connector and with the I/O application via a cable connector on the module.

1.3 EQUIPMENT DESCRIPTION

Standard equipment for a subsystem depends on the chosen configuration (Table 1-1). Optional equipment depends on the application.

There are four basic hardware configuration designators IP11Ø, IPV1Ø, IP3ØØ, and IP11 (Table 1-1). All systems fall into one of these four categories. The fifth character in the designation will vary depending on the software provided. These software categories are identified in Table 1-2.

NOTE

IP11S is a designation that was used to denote IP112 systems shipped in early 1979. In this manual, all references to IP11Ø and IP112 apply equally to IP11S systems.

Table 1-1 Subsystem Configurations

		IP3ØØ	IP11	IP11Ø	IPV1Ø
Standard Equipment					
H96Ø-C	Cabinet A or B (115 or 23Ø Vac)	X			
H333	Chassis A or B (115 or 23Ø Vac)	X	X		
H334	Chassis E or J (115 or 23Ø Vac)			X	X
M7958	I/O control module	X	X		
M7959	I/O control module				X
M8719	I/O control module			X	
H787Ø	Power supply (part of H333-A or -B)	X	X		
H7872	Power supply (part of H334-E or -J)			X	X
*	Terminal	X			
DLV11-F	Serial line unit	X			
RXV11-B	Dual floppy disk and controller	X			
LSI-11	Microcomputer	X			
MSV11-DD	28K memory	X			
REV11-A	LSI-11 terminator, boot module	X			
TEV11	LSI-11 terminator module		X		
DW11-A	UNIBUS to LSI-11 bus converter module		X		

*Choice of LA36, VT52, or VT1ØØ

Optional Equipment	
H96Ø-C	Expansion cabinet A or B (115 or 23Ø Vac)
H334	Expansion chassis A, B, E, J, or X (A, E = 115 V; B, J = 23Ø V; X = nonpowered)
H332	Screw terminal mounting rack
BC4ØA	16/32-bit screw terminal strip
BC4ØB	8-bit screw terminal strip
BC4ØL	16/32-bit terminal strip for user mounted components
ATR16	Isothermal screw terminal assembly

Table 1-2 System Designations

Hardware Only	With Software: RSX-11M RSX-11S	RSX-11M+	RT11
IP11Ø	IP112 *	IP113	IP114
IPV1Ø	IPV12		IPV14
IP3ØØ	IP3Ø2		IP3Ø4
IP11	IP11		

*IP112 designator applies also to the old IP11S systems.

1.3.1 Hardware Configurations

The I/O Subsystem is available in the following configurations.

IP3ØØ Subsystem - The IP3ØØ is an independent, standalone subsystem with its own built-in LSI-11 microcomputer. The computer and its peripherals can occupy the first five module positions in the card cage. Figures 1-2 and 1-3 show the basic I/O Subsystem components, the LSI-11 computer, and their locations in the master chassis.

IP11Ø Subsystem - The IP11Ø (Figure 1-4) operates with a PDP-11 computer via a control module that plugs directly into the PDP-11. Interface with the I/O modules on the D-bus is via a cable from J1 of the control module to the D-bus input connector of the first subsystem chassis.

IP11 Subsystem - The IP11 operates externally to a PDP-11 host computer via a UNIBUS to LSI-11 bus converter module. Interface is by a cable that plugs into a backplane-to-cable adapter at the I/O Subsystem end and into the bus converter module at the PDP-11 end. Figure 1-5 shows the I/O Subsystem components and the backplane-to-cable adapter locations in the master chassis. IP11 systems are recommended for replacement or expansion purposes only. New PDP-11 based designs should be implemented with an IP11Ø configuration.

IPV1Ø Subsystem - The IPV1Ø (Figure 1-6) operates with an LSI-11 computer (e.g., a PDP-11/Ø3 or PDP-11/23) via a control module that plugs directly into the LSI-11. Interface with the I/O modules on the D-bus is via a cable from J1 of the control module to the D-bus input connector of the first subsystem chassis.

Expanded Subsystems - Any of the above subsystems can be expanded beyond the initial chassis. Up to seven chassis can be added to the subsystem; each accommodates ten additional I/O modules.

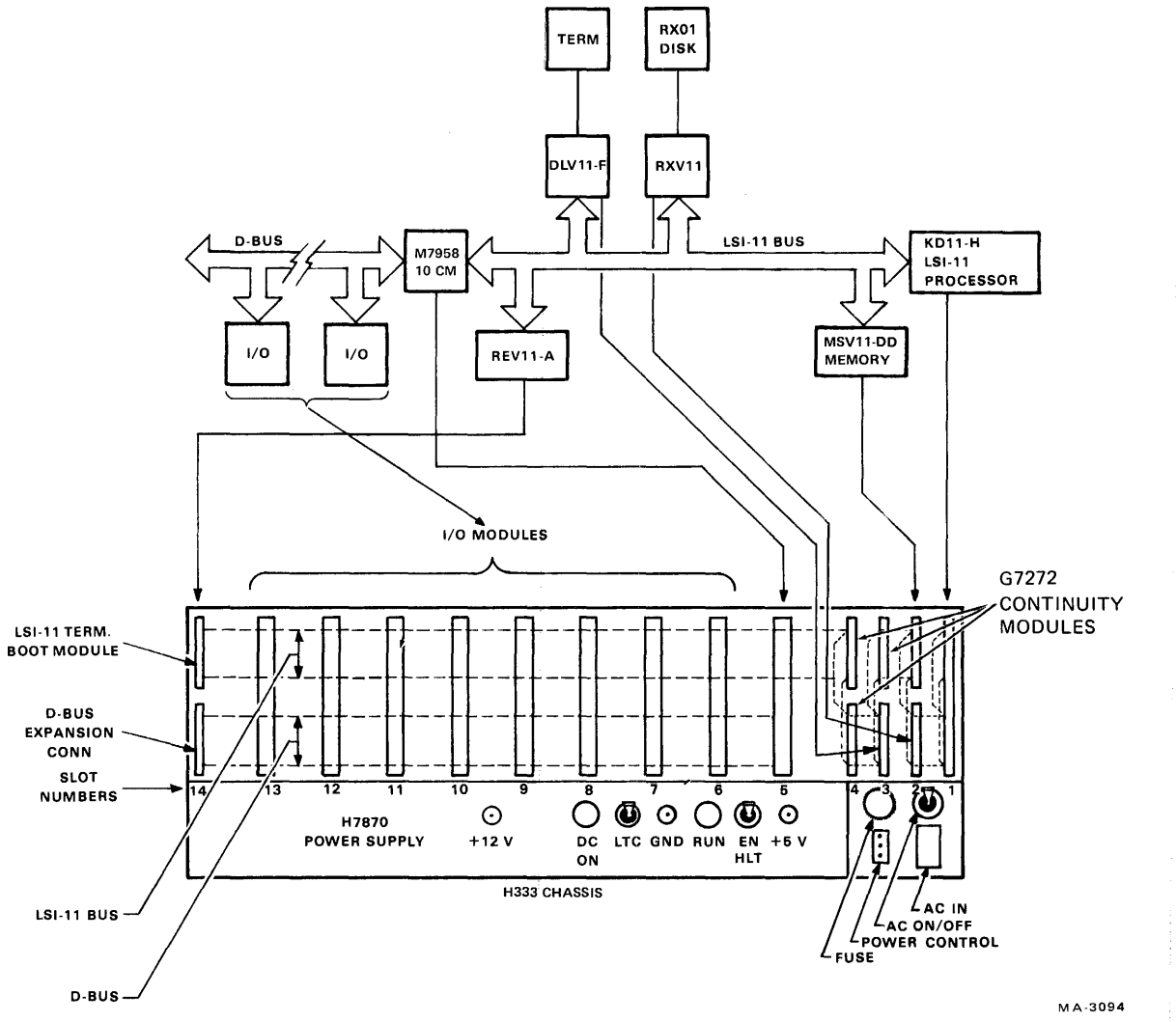

Figure 1-2 IP300 - LSI-11 Based Subsystem (Current Version)

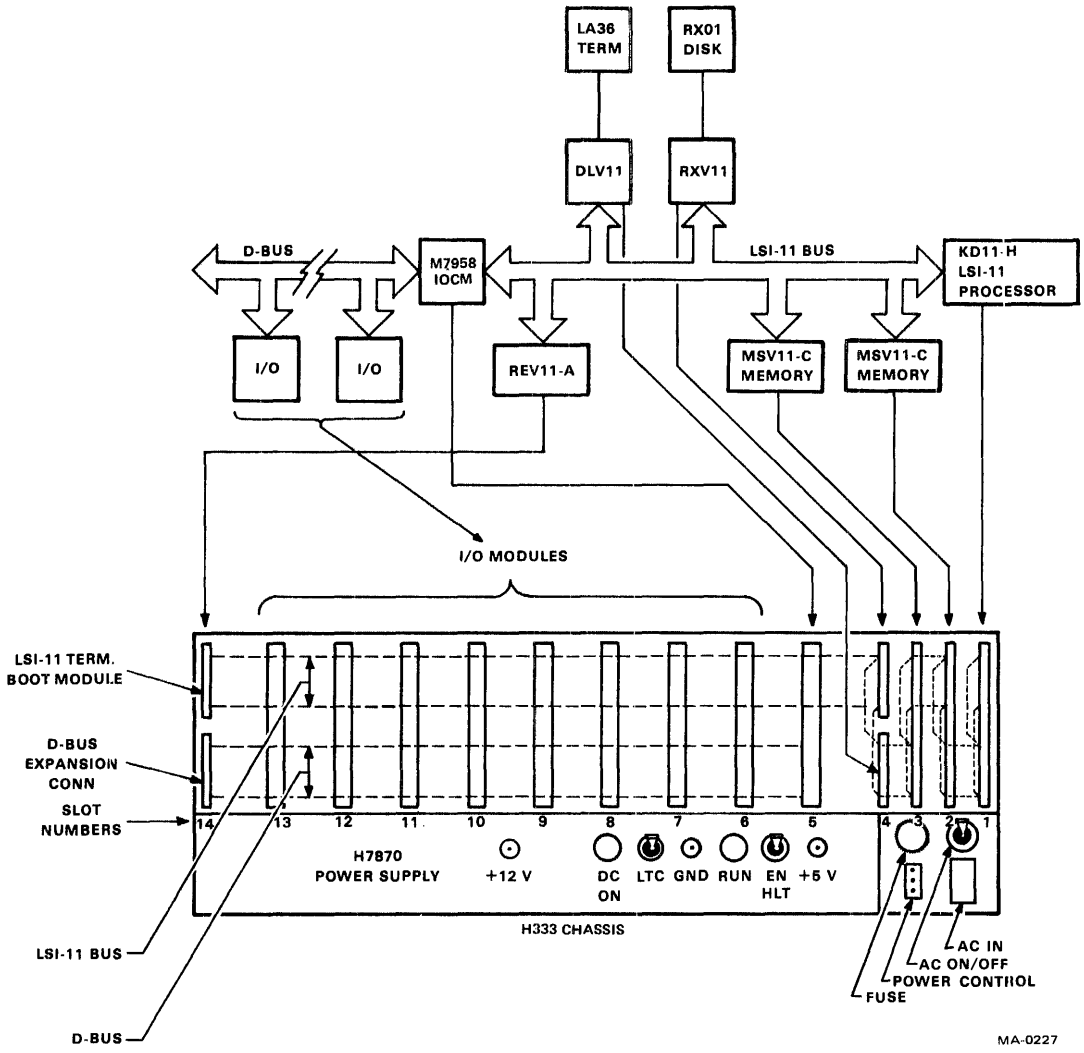

Figure 1-3 IP300 - LSI-11 Based Subsystem (Older Version)

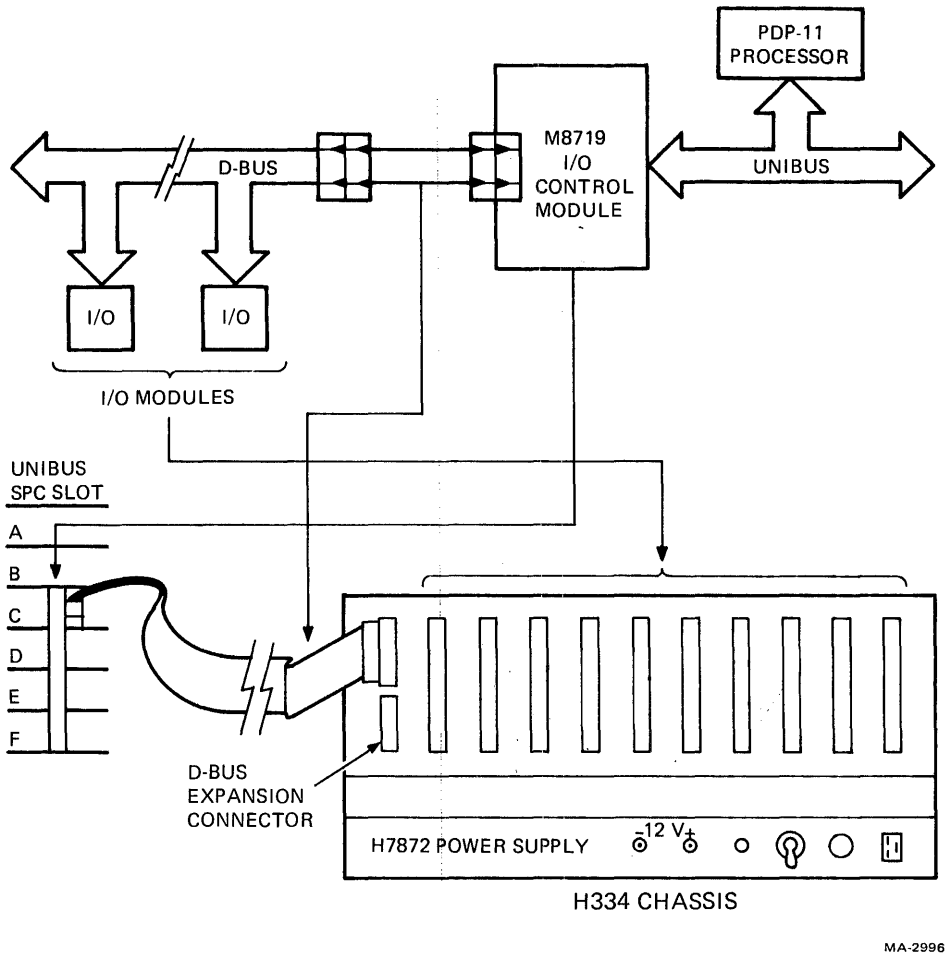

Figure 1-4 IP11Ø - PDP-11 Based Subsystem (Current Version)

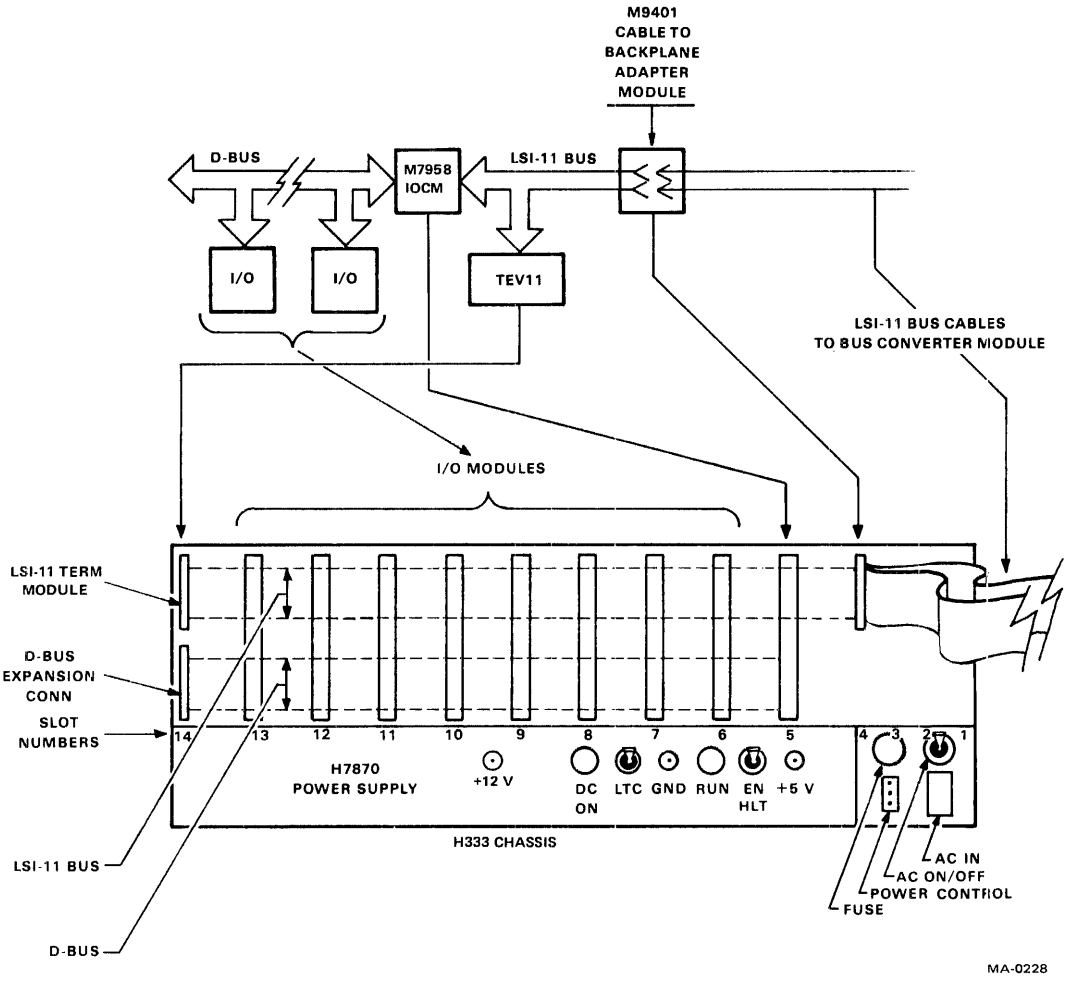

Figure 1-5 IP11 - PDP-11 Based Subsystem
(Not Recommended for New Systems)

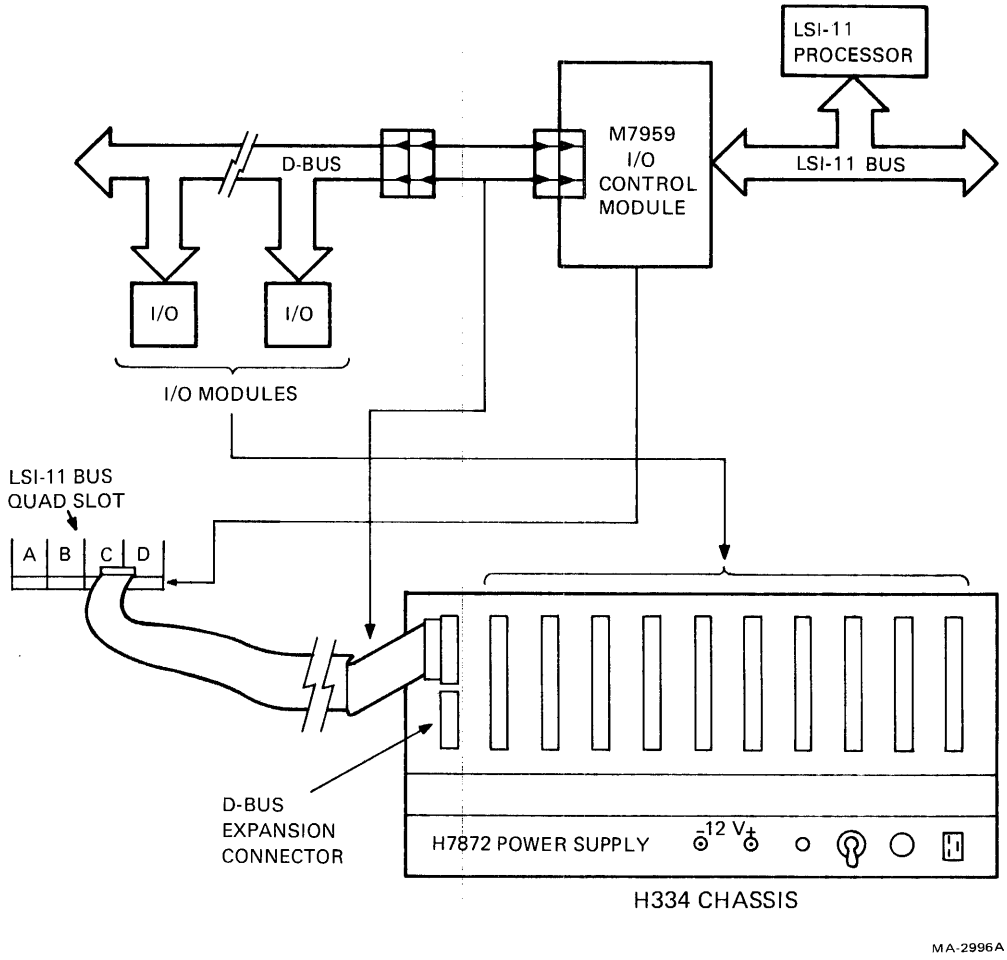

Figure 1-6 IPV11Ø LSI-11 Based Subsystem

1.3.2 Standard Equipment

H96Ø-C Cabinet - This 19-inch cabinet is standard with the IP3ØØ subsystem and is recommended for the IP11 and IP11S. The cabinet has four units* of mounting space and comes equipped with an 861 power controller and a blower assembly (Figure 1-7). The H96Ø-CA and H96Ø-CB versions are 115 and 23Ø Vac, respectively.

H333 Chassis - The H333 chassis comprises the H787Ø power supply, the module enclosure, and the M7958 I/O control module. The enclosure has quad-height spaces for eight I/O modules and the LSI-11 modules (Figure 1-2). A dual-height space is provided for the LSI-11 bus terminator/boot module, and just below it is a connector for expansion of the D-bus to additional chassis.

The LSI-11 bus and the D-bus are etched on the backplane of the enclosure. The LSI-11 bus occupies the top half of the backplane for all module positions and the bottom half for the LSI-11 positions. The D-bus is etched only on the bottom half of the

*A unit is any H333, H334, or H332 chassis.

eight I/O and IOCM positions. The M7958 interfaces with both buses, but the I/O modules, which use only the lower half of their etched edge connectors, interface only with the D-bus.

H334-E/J Chassis - The H334-E/J chassis comprises the H7872 power supply and the module enclosure. The enclosure has quad-height spaces for ten I/O modules and connectors for input and output of the D-bus which is etched on the C and D connectors of the enclosure backplane.

H787Ø Power Supply - The H787Ø power supply, used in both the H333 and the H334-A/B chassis, generates the dc operating voltages (+12 and +5 Vdc) required by the I/O Subsystem.

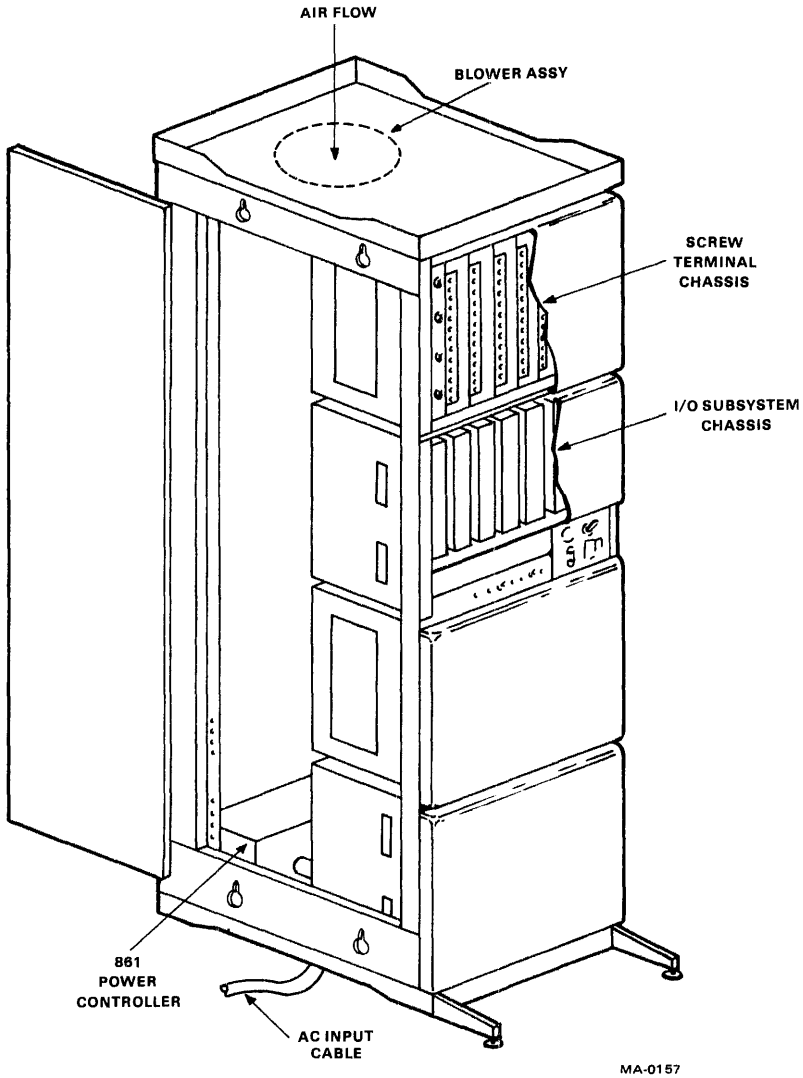

Figure 1-7 H96Ø-C Expansion Cabinet

H7872 Power Supply - The H7872 power supply is used in the H334 chassis only; it provides +12 Vdc for the I/O modules.

M7958 I/O Control Module - The M7958 is a quad-height module that mounts in the H333 chassis and originates the D-bus. This module, which bridges the two backplane buses, accepts LSI-11 signals and generates D-bus signals for routing data to and from the I/O modules.

M7959 I/O Control Module - The M7959 is a quad-height module that mounts in a quad slot in an LSI-11 processor; it originates the D-bus. A BCØ8R cable carries the D-bus to the I/O module chassis. This module accepts LSI-11 bus signals and generates D-bus signals for routing data to and from the I/O modules.

M8719 UNIBUS I/O Control Module - The M8719 is a quad-height module that mounts in a quad SPC slot in a PDP-11 processor; it originates the D-bus. A BCØ8R cable carries the D-bus to the I/O module chassis. This module accepts UNIBUS signals and generates D-bus signals for routing the data to and from the I/O modules.

LA36 Terminal - The LA36 DECwriter II is a medium sized, low cost, interactive data communication terminal. It is designed as an input/output device that can be used as a system command console or as a remote communication terminal. The LA36 interfaces with the LSI-11 bus via a cable to the DLV11-F (MØØ28) module.

VT52 Terminal (DECscope) - The VT52 is an upper- and lowercase ASCII video terminal whose display holds 24 lines of 8Ø characters.

VTlØØ Terminal - The VTlØØ is DIGITAL's latest video terminal with many new features not included in the VT52.

RXØ1 Disk - The RXØ1 Floppy Disk System is a compact, low cost, mass storage subsystem, capable of storing up to 256,256 bytes per drive in an industry-compatible format. The RXØ1 disk interfaces with the LSI-11 bus via the RXV11 (M7946) module.

LSI-11 Microcomputer - The LSI-11 is a 16-bit microcomputer with much of the speed and power of a minicomputer. As implemented in the I/O Subsystem, the microcomputer occupies the first position and half of the second position on the LSI-11 bus; the KD11-H (processor module) being first and an MSV11-DD (memory module) second.

DW11-A UNIBUS to LSI-11 Bus Converter Module - In the IP11, which operates with an external PDP-11 instead of the LSI-11 microcomputer, its LSI-11 bus must be adapted to the UNIBUS. This function is performed by the bus converter module which resides on the UNIBUS. The module mounts in an SPC slot in a UNIBUS processor. Interface with the LSI-11 bus is via a cable to the M94Ø1 (cable-to-backplane adapter module) which occupies a

dual-height module position on the LSI-11 bus in the I/O Subsystem. It is not recommended that the DW11-A based system (IP11) be used in new applications.

1.3.3 Optional Equipment

The following options may be purchased with the I/O Subsystem.

H334 Chassis - This chassis extends the D-bus to accommodate any I/O modules in addition to those in the first chassis. Each H334 chassis accommodates ten I/O modules. There may be as many as seven chassis for a total of 70 I/O modules in addition to those in the first chassis. The D-bus is etched on the lower half of the H334 chassis backplane, which also includes cable connectors for extending the D-bus from one chassis to another. There are five versions of the H334 chassis: H334-A, -E, and H334-B, -J are for 115 Vac and 230 Vac, respectively. Version H334-X is nonpowered. Versions -A, -B, and -X are for expansion or replacement purposes; versions -E and -J are recommended for new designs. The rules for using powered and nonpowered chassis in a particular application are discussed in Chapter 3.

H332 Screw Terminal Mounting Chassis - This chassis is mounted in the cabinet directly above an I/O module chassis; it holds the screw terminal assemblies which are mounted directly above each of the I/O modules. Each chassis accommodates up to ten screw terminal assemblies.

BC40 Screw Terminal Strips - These assemblies connect the customer's I/O lines to the I/O modules via convenient screw terminals. Each assembly consists of a 34 screw terminal barrier strip and an I/O cable connector mounted on a printed circuit board. The assemblies mount in the screw terminal chassis, one above each I/O module, and connect to them via preassembled cables supplied with the screw terminal assemblies. The BC40A is for 16- and 32-bit modules; the BC40B is for eight bit modules. The BC40L has an extra large printed circuit board for the user who needs space to add custom circuits, such as filters, attenuators, etc. It is equipped with turret terminals for easy component mounting.

ATR16 Isothermal Screw Terminal Assembly - The ATR16 connects thermocouple field wiring to an analog input subsystem. It accepts up to 16 thermocouple inputs and provides a single ambient temperature reference output.

I/O Modules - I/O modules provide the interface between the process and the D-bus. Connection to the D-bus is via the bottom two sections of the four-section, etched-edge connector. (The top two sections are not functional on I/O modules.) Connection to the process is via a cable connector on the opposite edge of the board. Table 1-3 provides a brief description of available I/O modules. (A more complete description is found in Chapter 6.) These modules are optionally selected by the customer to suit his particular application.

Table 1-3 Module Descriptions

Module No.	Description
M5010	Nonisolated, 32-bit, dc sense input module, input range is from -30 V to +55 V
M5011	Nonisolated, 16-bit, dc change-of-state input module with optional interrupt capability, input range is from -30 V to +55 V
M5012	Optically-isolated, 16-bit, dc input module with optional interrupt capability Module has individual input indicators on field side of isolation Input range is from -55 V to +55 V
M5012-YA	TTL compatible version of the M5012 without the input activity indicators
M5013	Transformer-isolated, 8-bit, ac input module with optional interrupt capability Module has individual input indicators on field side of isolation Inputs are protected from overvoltage transients by MOVs Nominal input is 120 Vac, 47 to 63 Hz
M5014	Dual 16-bit presettable up-counters, with internal frequency and time bases, for event counting or pulse width measurement Accommodates isolated or nonisolated, low level, high level, or TTL field connections
M5016	Quad, 8-bit up-counters with presettable overflow level, for prescaling and counting applications Accommodates isolated or nonisolated, low level or high level inputs
M5031	Optically-isolated, 16-bit, dc change-of-state input module with optional interrupt capability Input range is from -55 V to +55 V
M6010	Nonisolated, 32-bit, dc output module with zener-protected Darlington output switches

Table 1-3 Module Descriptions (Cont)

Module No.	Description
	Outputs are rated at 250 mA and 55 V maximum
M6010-YA	TTL compatible version of the M6010 with outputs rated at 40 TTL unit loads
M6011	Nonisolated, 16-bit, one-shot module with zener-protected Darlington output switches Outputs are rated at 250 mA and 55 V maximum Output timing is selectable from 100 microseconds to 5 seconds and is crystal-controlled
M6012	Optically-isolated, 8-bit, dc output module with zener-protected Darlington output switches Module has individual output indicators on field side of isolators Output current rating is 1 A per output up to a maximum of 4 A per module Maximum field voltage is 55 V
M6013	Transformer-isolated, 8-bit, ac output module Has individual output indicators on field side of isolation Outputs have MOVs for protection against overvoltage transients and a current rating of 2 A per output up to a maximum of 8 A per module
M6014	Dual, counter controlled, output pulse generators Frequency is selectable from 10 kHz to 0.2 Hz; duty cycle from 10% to 80% Has sign/direction and enable outputs All outputs are nonisolated and high level or TTL compatible
M6015	Optically-isolated, 16-bit, retentive, dc output module with zener-protected power FET output switches Outputs are grouped in four groups of four Groups are isolated from ground and from each other Output current rating is 0.25 A per output

Table 1-3 Module Descriptions (Cont)

Module No.	Description
	Output states are retained during a computer power failure as long as the user furnished field power supply is present
A014	A/D converter 12-bit, with built in multiplexer to accommodate 16 single-ended or eight differential inputs Input capability can be expanded to 240 single ended or 120 differential by using expansion multiplexer modules (A156 and/or A157)
A020	High common mode A/D converter, for applications requiring isolation from high common mode voltages, 14-bit magnitude plus sign, built-in multiplexer accommodates sixteen 2-wire or eight 3-wire inputs
A156	An expansion multiplexer that provides an additional 32 single-ended or 16 differential high level input channels for the A014 A/D converter Seven A156 multiplexers may be used to provide up to 224 additional analog inputs to the A014
A157	An expansion multiplexer that provides programmable gain for low level field inputs to the A014 A/D converter Accepts 16 differential inputs that can be independently programmed for any of eight different gains between 1 and 1000 A total of seven A157s can be used to provide up to 112 programmable gain inputs for the A014
A630	Four independent 10-bit D/A converters with current and voltage output options Voltage outputs are 0-10.23 V at 15 mA; current outputs are 0-20 mA or 4-20 mA
A631	Four isolated 12-bit D/A converters with current or voltage output options Outputs are group isolated from computer ground Voltage outputs are 0 - 10.2375 V at 5 mA; current outputs are 0 - 20.475 mA See A631 section in Chapter 6 for configuration constraints when using multiple A631 modules in current mode.

1.4 SPECIFICATIONS

1.4.1 Physical

Chassis Dimensions	
H333	40 cm X 48.26 cm X 27.28 cm (15.75 in X 19 in X 10.74 in)
H334	40 cm X 48.26 cm X 27.28 cm (15.75 in X 19 in X 10.74 in)
H332	40 cm X 48.26 cm X 27.15 cm (15.75 in X 19 in X 10.69 in)
Chassis Weight	
H333	19.5 kg (43 lb)
H334-A or -B	18.14 kg (40 lb)
H334-E or -J	8.62 kg (19 lb)
H334-X	5.44 kg (12 lb)
H332	7.71 kg (17 lb)

1.4.2 Environmental

The I/O Subsystem meets the requirements of DEC Standard 102 for a class C environment.

Temperature	
Operating (in DEC cabinet)	+5° to 50° C (41° to 122° F) ambient
Nonoperating	-40° to +66° C (-40° to +150.8° F)
Humidity	
Operating	10% to 95% relative humidity Maximum wet bulb: +32° C (89.6° F) Minimum dew point: +2° C (35.6° F)
Nonoperating	10% to 95% relative humidity

1.4.3 Power Requirements

Input voltage	100-127 or 200-254 Vac
Input current	
H7870	4.2/2.5 A maximum
H7872	1.4/1.0 A maximum
Input frequency	50 or 60 Hz ±3 Hz
Input power	
H7870	500 W maximum
H7872	170 W maximum
Ride through	If the input voltage is at or above 115 or 230 Vac, it may be interrupted for as long as three cycles without affecting the subsystem.

1.4.4 Performance

Operational modes	Programmed I/O Program interrupt

Number of digital I/O bits (maximum)	H333	256
	H334	320
	Subsystem	2032
System configuration	Chassis	8 maximum
	D-bus length	15 m (50 ft) maximum
I/O word selection	Directly addressable by byte, I/O module addresses are switch-selectable	
Maintenance features	1. Each module type has a unique generic code that enables checking of system configuration.	
	2. Maintenance interrupts enable checking of interrupt logic.	
	3. Maintenance mode test checks for data integrity of D-bus.	
	4. Output module data reads back.	
Interrupts	1. Address of highest priority interrupting module is available at time of interrupt service.	
	2. Priority is determined by proximity to control module, not by module address (on multibyte I/O modules, lower byte address has highest interrupt priority).	
D-bus Cycle times (nominal)	DATAI	4.8 microseconds
	DATAO	3.9 microseconds
	DATAIO	6.0 microseconds
Computer interface	The interface is direct to LSI-11 bus or UNIBUS and indirect to UNIBUS with DW11-A bus converter.	
Power Supply (H7870) Input	115 Vac, 47-63 Hz or 230 Vac, 47-63 Hz	

Outputs	+5 Vdc regulated, 14 A maximum +12 Vdc regulated, 6 A maximum
	NOTE **+5 V and +12 V combined loading are not to exceed 122 W.**
Features	Line time clock, switch-enabled
	Power sequencing signals (PWR OK/DC OK) for LSI-11
	Switchable HALT/ENABLE DC ON indicator
	LSI-11 RUNNING indicator
Cooling	Two fans provide 92 CFM for the power supply and LSI-11. The I/O modules are cooled by convection.
Heat dissipation	1706 Btu/hr maximum exclusive of heat dissipation due to field input circuits
	NOTE **Heat dissipation is a function of the type and number of I/O modules in use.**
Power Supply (H7872)	
Input	115 Vac, 47-63 Hz or 230 Vac, 47-63 Hz
Output	+12 Vdc regulated, 4 A maximum
Features	DC ON indicator
Cooling	Single fan provides 46 CFM for cooling the power supply.
Heat dissipation	560 BTU/hr maximum exclusive of heat dissipation due to field input circuitry.
	NOTE **Heat dissipation is a function of the type and number of I/O modules in use.**

1.5 APPLICABLE DOCUMENTS

Table 1-4 lists documents applicable to the I/O Subsystem.

Table 1-4 Applicable Documents

Title	Number	Description
Microcomputer Handbook	EB-Ø658376	General handbook containing LSI-11 family hardware, operation, processor, and software information (H)*
861 Power Controller Maintenance Manual	EK-861AB-MM	Operation and maintenance of the 861 power controller (M, H)*
Digital Site Preparation Guide	EK-CORP-SP	A general site preparation guide for equipment marketed by Digital Equipment Corporation (H)
LSI-11 User Manual	EK-LSI11-TM	Contains hardware descriptions and system information that enables the user to interface LSI-11 components. (H)*
DW11-A Unibus to LSI-11 Bus Converter Installation Manual	EK-DW11A-IN	Contains hardware descriptions and system information that enables the user to effectively utilize the DW11-A (H, S)*
DEC STD 1Ø2	-	Defines the environmental conditions to which products marketed by Digital Equipment Corporation must conform (L)
PDP-11 Peripherals Handbook	EB-Ø596176	A general handbook containing descriptions, specifications, interfacing, and programming information on PDP-11 peripherals and options (H)*
I/O Subsystem Acceptance Procedure	A-SP-H333-Ø-7	A procedure used by field service, after installation, to ensure that the I/O Subsystem is operational
I/O Subsystem Diagnostic	MD-11-CVPCAD-Ø	A test program that helps field service personnel isolate faults quickly

(M) In Microfiche Library
(S) Ships with device on hard copy (when not part of Microfiche Library)
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CHAPTER 2
SITE PREPARATION AND PLANNING

2.1 SCOPE

This chapter contains site preparation and planning information for I/O Subsystems. Included are recommended physical, electrical, and environmental requirements that facilitate equipment installation and maintenance, and optimize system performance.

The reader is referred to specific paragraphs in the Digital Site Preparation Guide for most system requirements; however, some information for I/O Subsystems in particular is included here.

2.2 GENERAL CONSIDERATIONS

Successful installation of an I/O Subsystem requires thorough planning and preparation of the proposed site. In particular, the reader is referred to the following paragraphs in the Digital Site Preparation Guide.

1.1	Introduction
1.1.1	Selecting a Site
1.1.2	Developing a Site

2.3 SITE PLANNING

Refer to the following paragraphs in the Digital Site Preparation Guide.

1.5.1	Space Requirements
1.5.5	Fire and Safety Precautions
1.5.5.3	Data Protection
1.5.6	Security
1.5.7	Operational Requirements

2.4 EFFECT OF ENVIRONMENT ON SYSTEM RELIABILITY

The computer area environment substantially affects overall system reliability. Temperature cycling and thermal gradients induce temporary or permanent microscopic changes in materials that can affect performance and/or endurance. High temperatures tend to increase the deterioration rate of most materials. High absolute humidity (dew point) causes moisture absorption that can result in dimensional and handling changes in paper and plastic media (line printer paper, cards, paper tape, magnetic tape, etc.).

Static electricity and airborne dust are hazardous to system reliability. Low humidity allows static electricity to build up, while high dust levels clog filters and reduce the effectiveness of the cooling system. Dust also reduces magnetic tape life and increases head wear, causing data errors in all moving magnetic storage media (drums, tapes, and disks). Vibration also causes slow degradation of mechanical parts, and when severe may cause errors on disks and drums.

Hardware logic errors can be caused by radio frequency pulses conducted through power mains or radiated through space. Such

pulses could come from nearby radar installations, broadcasting stations, or welding operations. Pulses can also come from arcs that occur when static electricity is discharged, or from arcing relay or motor contacts.

Any or all of the above environmental factors can be sources of eventual system or component failure. For more detailed information on these factors, refer to the following paragraphs in the Digital Site Preparation Guide.

1.8	Vibration
1.9	Lighting
1.10	Cleanliness
4.6.1	Static Electricity
Chapter 5	Temperature and Humidity

2.5 POWER REQUIREMENTS

Power requirements vary according to the system configuration selected, as discussed in Paragraph 2.7.4. Information on power requirements in general is found in Chapter 2 of the Digital Site Preparation Guide. Particular attention is called to the following paragraphs.

2.1	Introduction
2.3	Power Wiring and Color Coding
2.11	Power Controller

2.6 SYSTEM GROUND

The importance of good system grounding practices cannot be overemphasized. Refer to Chapter 3 of the Digital Site Preparation Guide for information on grounding and in particular to the following paragraphs.

3.1	Introduction
3.2	Safety Logic Ground
3.3	Common Grounding Practices
3.4	Grounding Requirements

2.7 SYSTEM CONFIGURATION

Although I/O Subsystem configurations differ according to individual customer requirements and options, a study of the following typical site requirements provides sufficient information for proper site planning.

2.7.1 System Configuration Diagrams

The I/O Subsystem diagrams in Figures 2-1 through 2-4 illustrate typical small and large system configurations as well as the physical location of cabinet-mounted components.

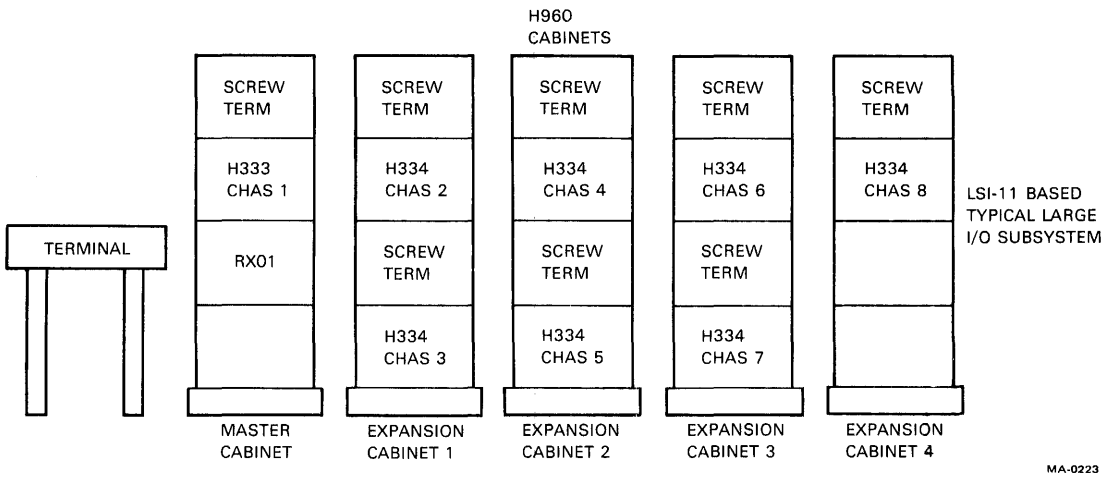


Figure 2-1 IP300 LSI-11 Based Configurations

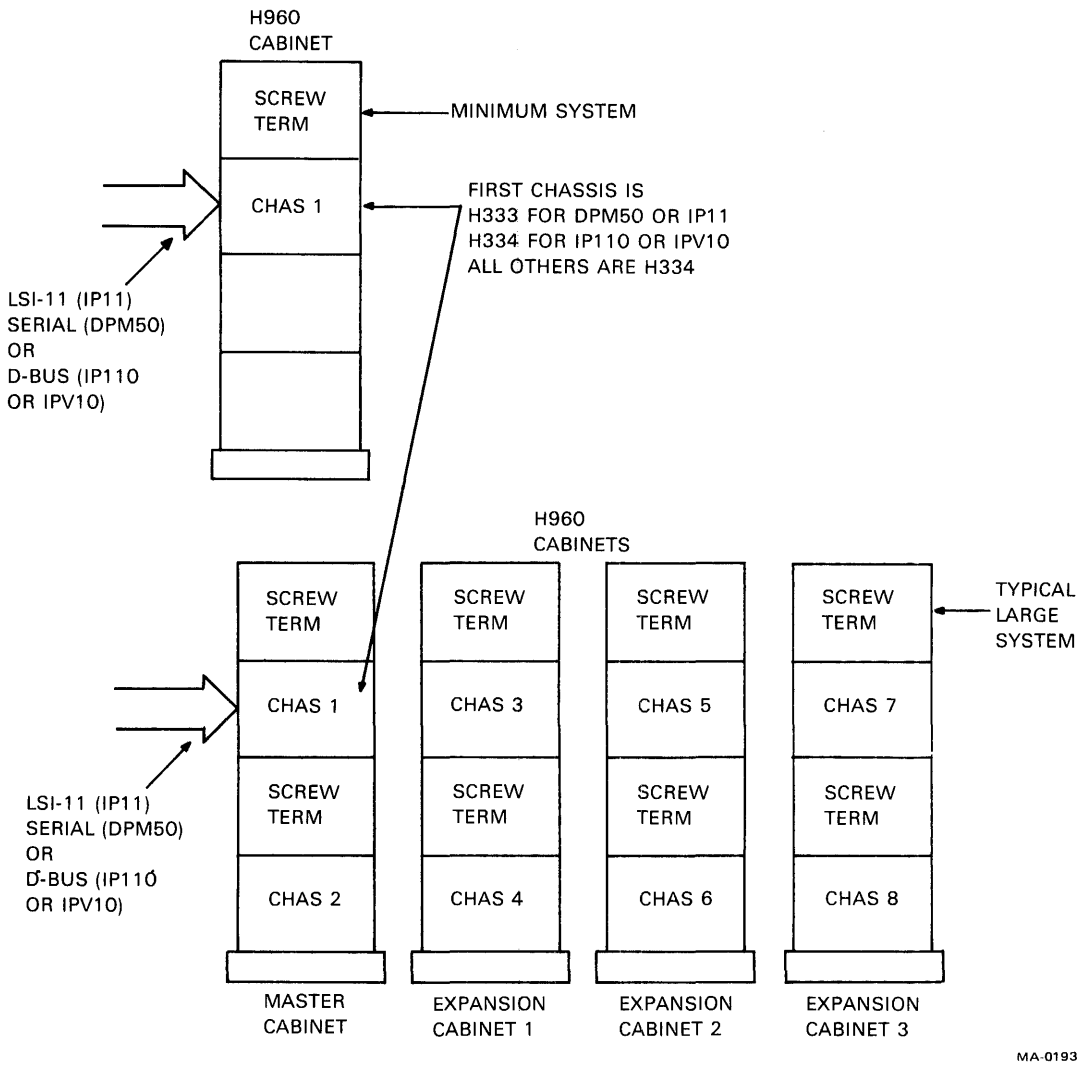


Figure 2-2 UNIBUS or Serial Bus Based Configurations

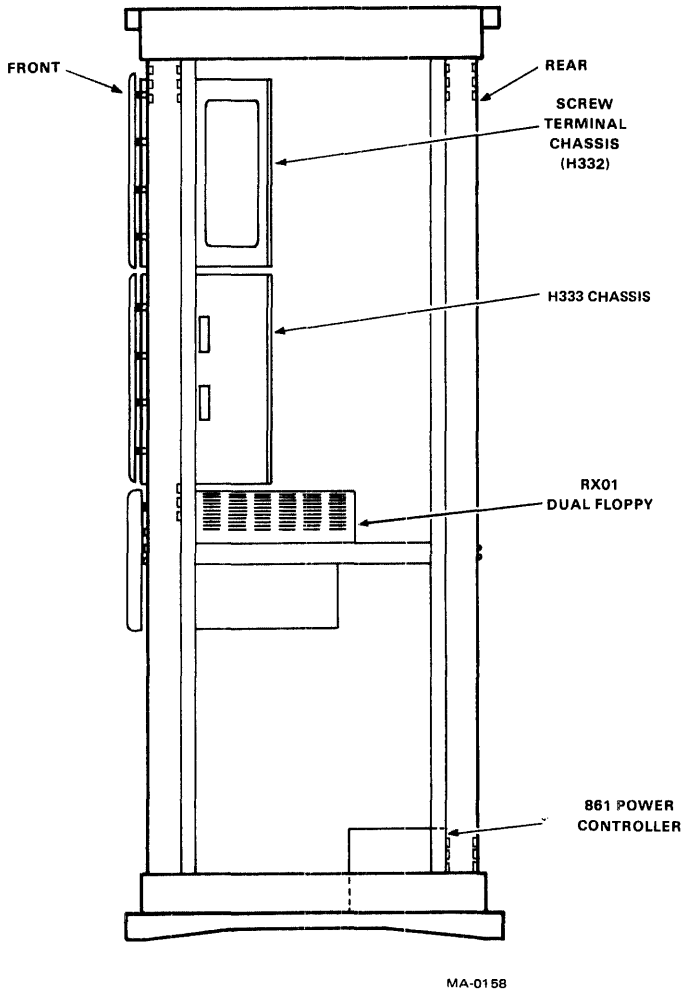


Figure 2-3 LSI-11 Based Minimum Configuration

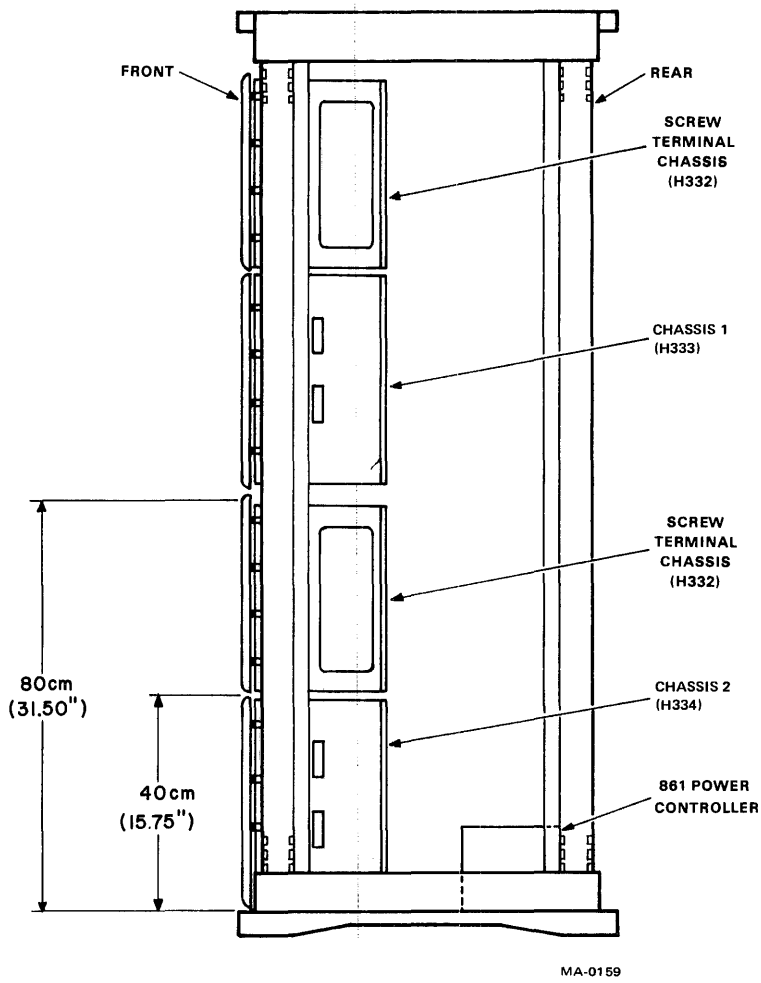


Figure 2-4 Expanded I/O Subsystem

2.7.2 Cabinet Space Requirements

Once the system configuration has been established, space requirements can be determined by studying Figure 2-5 which shows space requirements for single and multicabinet installations. In addition to the space required for the equipment cabinets, provision must be made for other site requirements, as discussed in Paragraph 2.3. Careful consideration should also be given to providing space for possible future expansion.

2.7.3 Cable Lengths

DEC cabinet interconnecting cables are of standard length and are factory installed. If the cabinets must be shipped separately because of shipping or receiving restrictions, the cabinet interconnecting cables should be protected from damage by a protective cover that does not present a safety hazard to operating personnel.

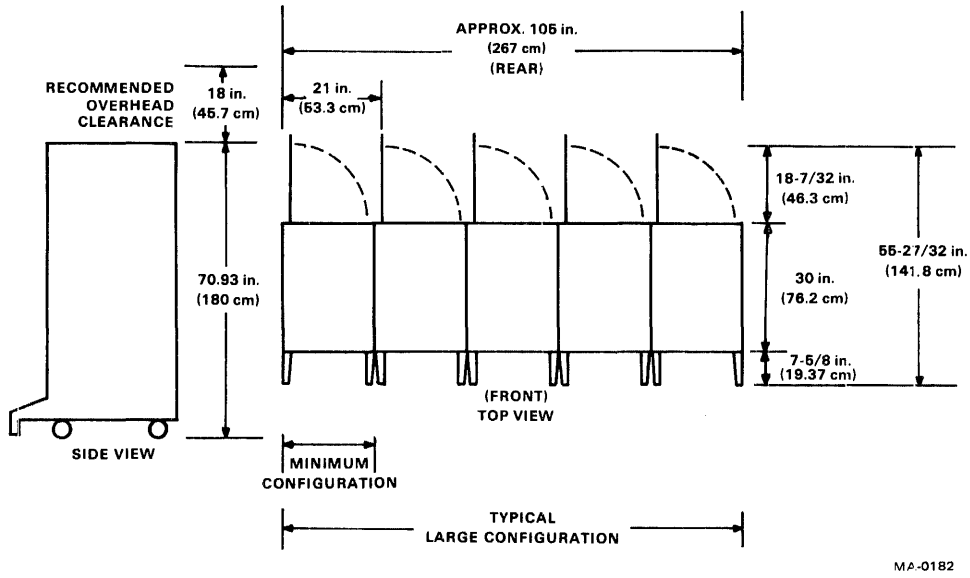


Figure 2-5 Cabinet Space Requirements

2.7.4 AC Power Connections

A 3-wire cable, 4.6 m (15 ft) long connects the site source power to the 861 power controller in the bottom of the H960 cabinet. All DEC-supplied cabinets used with I/O Subsystems include an 861 power controller and a single ac power cable. Power is distributed to the equipment within the cabinet from the power controller (Figure 2-6).

The customer site must supply one outlet for each cabinet. In most systems, it is convenient to provide a separate load center or circuit breaker panel for the system and to connect each receptacle to its own circuit breaker. Applicable plugs and receptacles are shown in Figure 2-7.

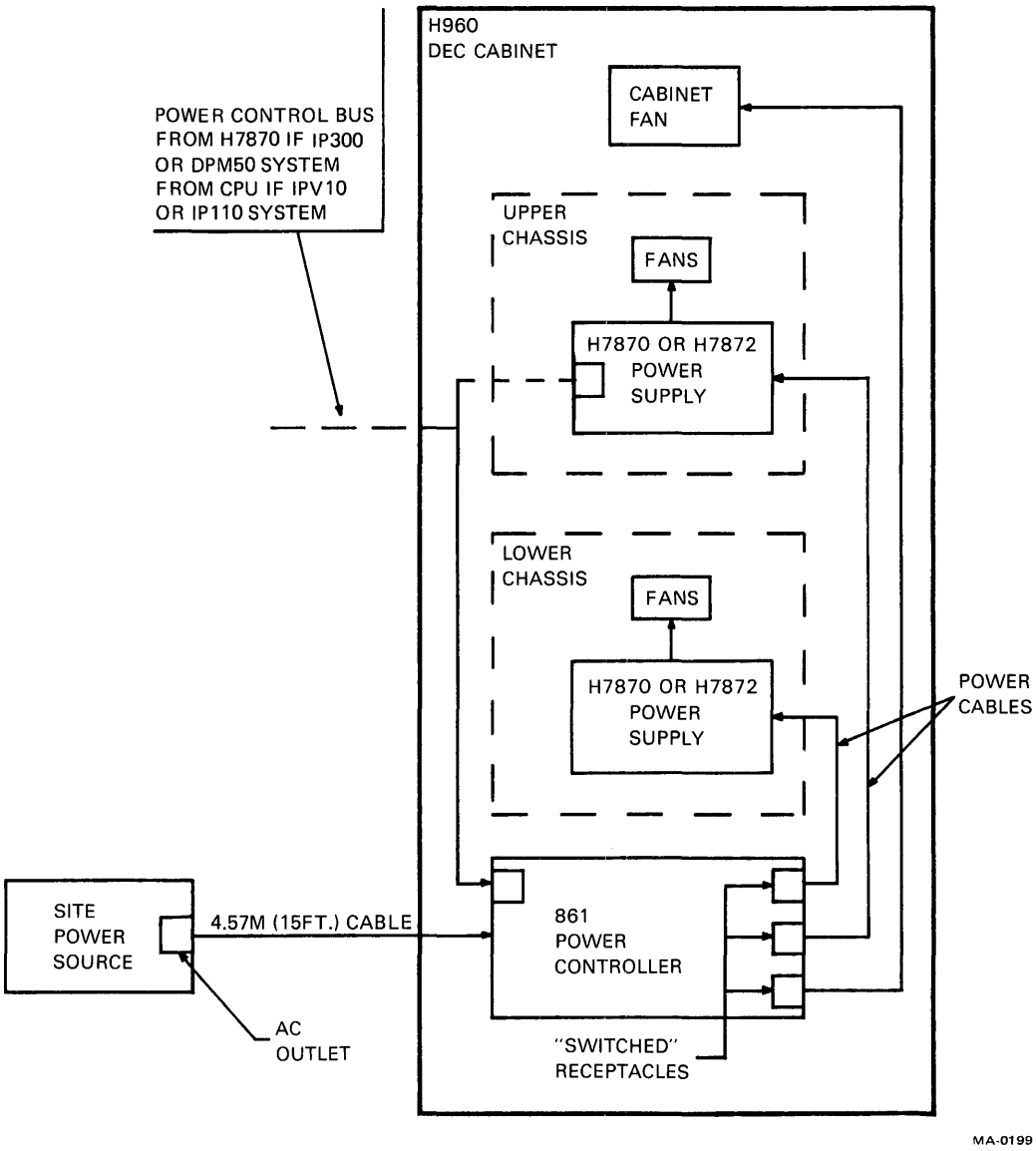
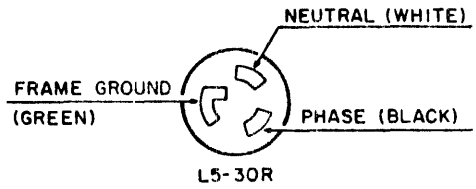
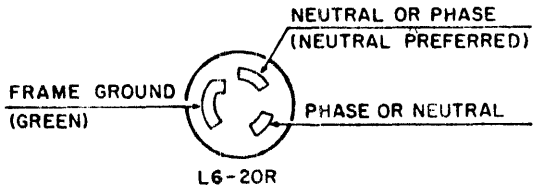


Figure 2-6 AC Power Distribution and Control



(a) 115 VAC, SINGLE PHASE, 24 AMPS
(SOCKET VIEW OF FEMALE RECEPTACLE)



(b) 230 VAC, SINGLE PHASE, 16 AMPS

POWER SOURCE	CONNECTOR	NEMA NO.	POWER CONTROLLER
115 VAC	Receptacle	L5-30R	861-C
Single phase	Plug	L5-30P	
230 VAC	Receptacle	L6-20R	861-B
Single phase	Plug	L6-20P	

11-4081

Figure 2-7 Plugs and Receptacles (861)

CHAPTER 3
INSTALLATION

3.1 INTRODUCTION

The information in this chapter is supported by illustrations and references to existing documentation relevant to integral units of an I/O Subsystem. It provides the user with information required to install and ensure proper operation of the I/O Subsystem. Figure 3-1 is an installation flow diagram that provides a quick reference for locating procedures via paragraph numbers that apply to the installation of the particular system purchased.

3.2 UNPACKING AND INSPECTION

The following information applies to all systems and configurations available as documented in this chapter.

NOTE

The customer must not unpack the system unless a DIGITAL representative is present; to do so voids the warranty.

3.2.1 Unpacking

If the shipment must be moved from the receiving area, make sure that doorways and passageways are wide enough to accommodate cabinet pallets before attempting to move equipment to its selected location. Regardless of where unpacking and inspection is done, containers must not be removed from the pallets until the shipment has been examined for possible damage. (Reimbursement for damaged goods removed from the pallet is difficult.)

Perform the following unpacking procedure.

1. Make sure that all containers are sealed. If any container is open, notify the customer and record it on the Installation Report or Field Service Report.

2. Check the shipment against the packing list to make sure that the correct number of containers has been received and that they are the correct ones. If shipment is incorrect, notify the customer and the Branch Service Manager or the Branch Supervisor. The customer should check with the carrier to locate any missing items.

3. Check all containers for external damage. Look for dents, protrusions, holes, and smashed corners. Notify the customer of any damage and record it on the Installation Report or Field Service Report.

4. Open each container beginning with the one marked "OPEN ME FIRST." Locate the packing slip and check the contents of each container against its respective slip. Identify any missing items on the Installation Report.

5. If reshipment is considered, retain packing materials

such as foam fillers and plastic inserts. In any case, retain the plastic (antistatic) bags in which any individual modules are shipped.

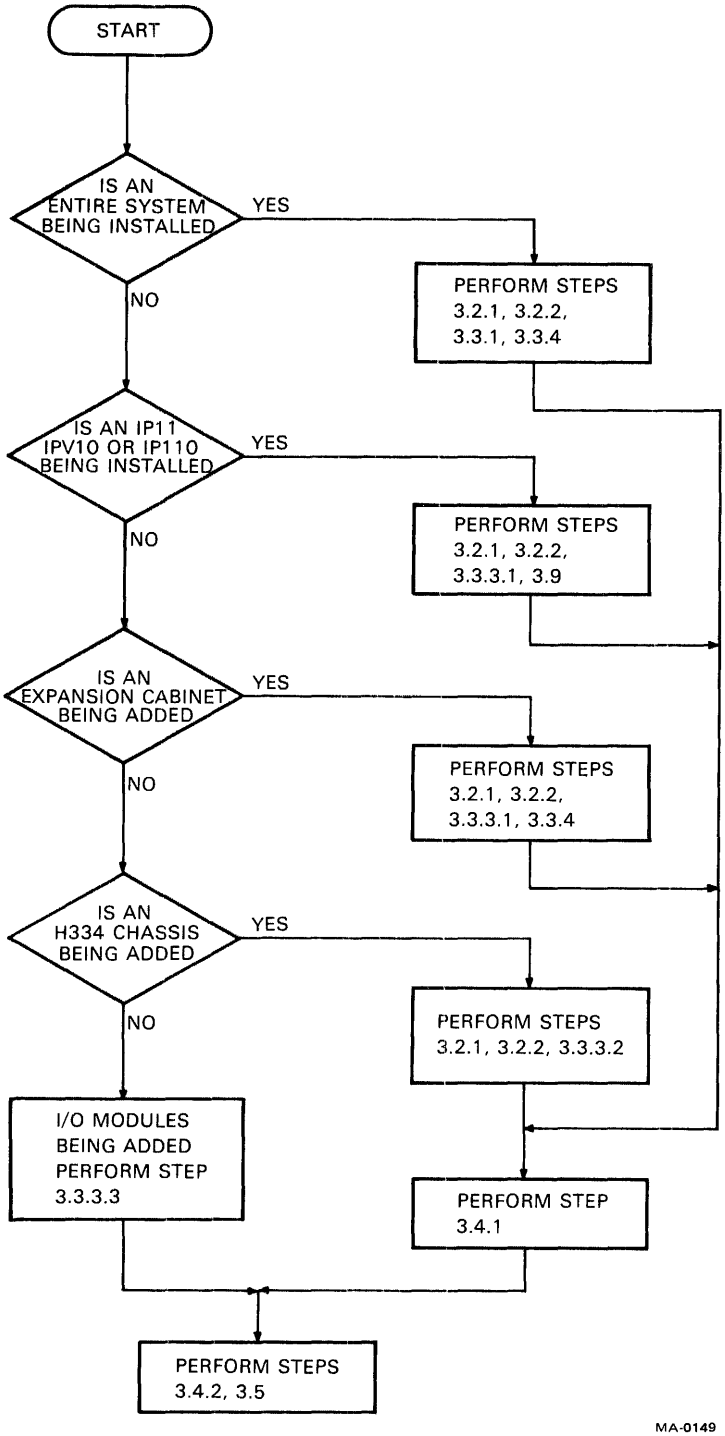


Figure 3-1 Installation Flow Diagram

3.2.2 Inspection

Perform the following inspection procedure.

1. Inspect the outside of the equipment and/or cabinet(s) for damage such as scratches, broken switches, broken stabilizer feet, etc.

2. Inspect the interior of the equipment and/or cabinet(s) for damaged components such as switches, indicators, etc., or for loose and broken cable connections. Make sure that all modules are securely seated in their connectors.

3. Notify the customer of any damage found and record it in the Installation Report. Notify the Branch Service Manager immediately of any serious damage found.

4. Inspect each cabinet and free-standing peripheral to make sure that it contains the items identified on the keysheet or transfer sheet. Check the ECO REV level and serial numbers against the keysheet or ECO status sheets. Record any missing items, incorrect serial numbers, or incorrect revision levels on the Installation Report.

5. When inspection has been completed, the equipment and the cabinet(s) can be removed from the shipping pallet. Remove the cabinet(s) as directed below.

    a. Unbolt the cabinet(s) from its shipping pallet. The bolts are located on the lower supporting side rails and can be reached from the inside of the cabinet.

    b. Raise the stabilizing feet above the level of the casters.

    c. Use wooden blocks and planks to form a ramp from the pallet to the floor and carefully roll the cabinet(s) onto the floor.

    d. Remove the four screws that secure the power supply in place in any powered H333 or H334 chassis. These screws are for shipping only and must be removed to allow access to the power supply.

3.3 INSTALLATION OF I/O SUBSYSTEM

This section covers installation of the I/O Subsystem and procedures for expanding an existing system. A full complement of related documents is included with the system shipment. The system may utilize additional functional I/O modules by adding H96Ø cabinets and H334 expansion chassis. Each H334 provides mounting space for up to ten functional I/O modules. A maximum of seven H334 expansion chassis can be added to a subsystem.

CAUTION

Before removing or replacing an I/O module or IOCM, turn off the power switch for the entire I/O subsystem (not just the single chassis). Failure to do so invariably damages the module.

3.3.1 Cabinet Installation

If the system being installed is a single cabinet configuration, it will consist of the following.

H960-C cabinet
H333 chassis if the system is an IP11 or IP300
H334 chassis if the system is an IPV10 or IP110

Options
- H332 screw terminal cage
- BC40 screw terminal assemblies
- ATR16 isothermal screw terminal assemblies
- H334 chassis
- I/O modules
- Other cabinet-mounted peripherals

Connections within the H960-C cabinet are completed prior to system shipment. Position the cabinet in its proper location and adjust the leveling feet to make sure that all leveling feet are resting firmly on the floor. A standard H960-CA cabinet is shown in Figure 3-2.

3.3.2 Intercabinet Connections (Expanded System)

If a larger system is purchased, additional cabinets and equipment are required as indicated in Paragraph 3.3. A larger system includes all parts listed in Paragraph 3.3.1, plus the following.

One to four H960-C cabinets
One to seven H334 chassis
Up to seven H332 screw terminal cages
Filler strips and hardware

When the unpacking and inspection procedures described in Paragraph 3.2 have been completed and the equipment has been moved to its selected location, proceed to the following steps.

1. Remove the side panel from the master cabinet. If the expansion cabinet(s) is to be installed as the configuration in Figure 3-3, remove the right side panel.

NOTE

Expansion cabinets do not have side panels. The panel removed from the master cabinet is installed on the last expansion cabinet in the configuration.

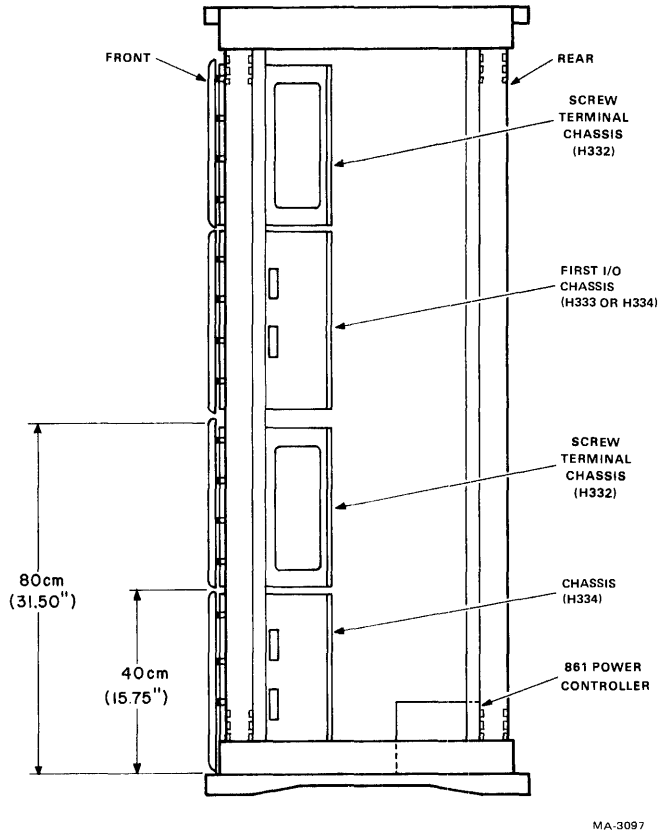


Figure 3-2 Standard H960-CA Cabinet with Expanded I/O Subsystem

2. The expansion cabinet(s) has two filler strips attached (Figure 3-4) that are placed between any two adjacent cabinets. Remove the socket-head screws and Kep nuts (four per filler strip) holding each filler strip to the expansion cabinet.

3. Move the master cabinet and the first expansion cabinet together and place filler strips between them, one at a time. Insert the socket-head screws through the respective holes in the cabinets and fillers.

4. Fasten the Kep nuts onto the screws and tighten securely.

5. Adjust the leveling feet until both cabinets are level and all leveling feet are resting firmly on the floor.

6. Continue the above steps until all cabinets are connected. Install the side panel removed in step 1 on the exposed side of the last cabinet.

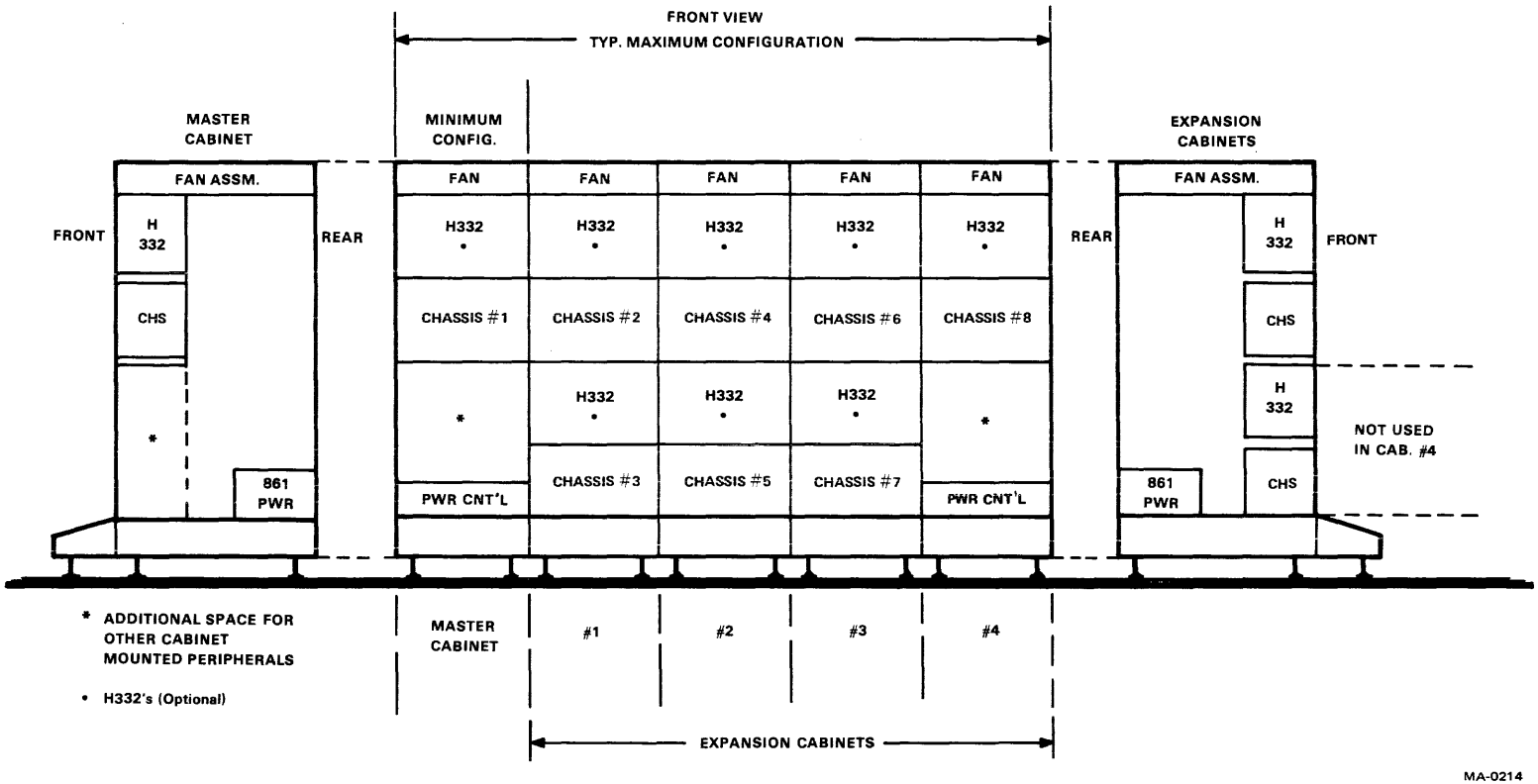


Figure 3-3 I/O Subsystem Front View

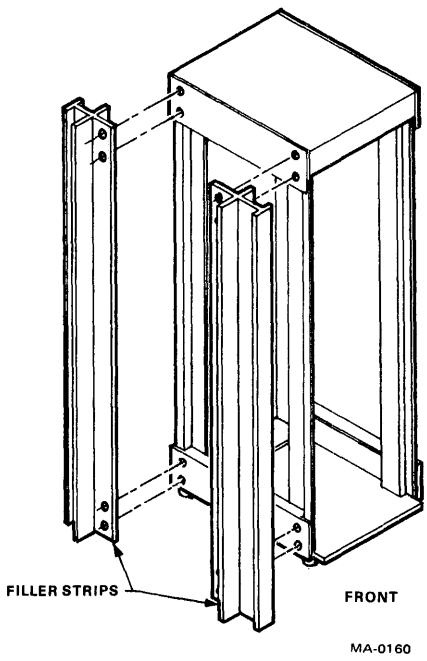
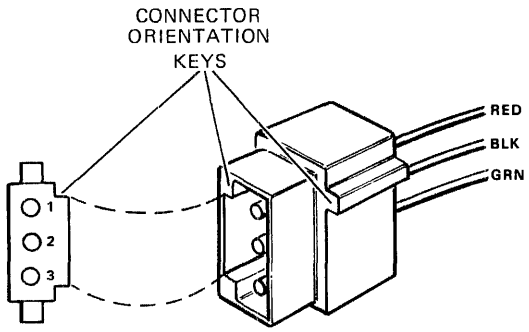


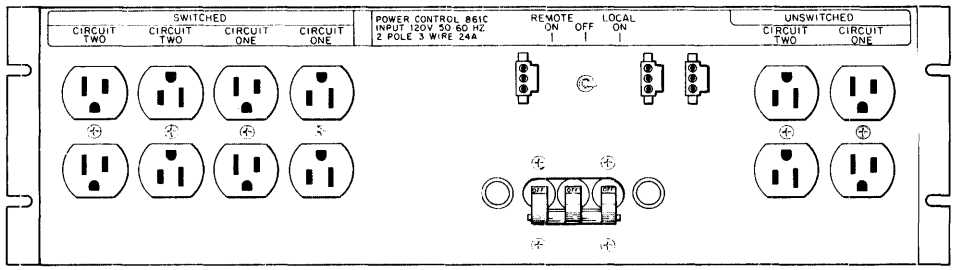
Figure 3-4 Cabinet Filler Strips

3.3.2.1 Ground Strapping Connections - Establish system frame ground in all cabinets by connecting all adjacent cabinet frames together, using the grounding straps provided. Exercise the grounding practices referenced in Chapter 2 of this manual and described in the Digital Site Preparation Guide (EK-CORP-SP).

3.3.2.2 Remote Power Connections - All cabinet power controllers must be interconnected by a remote switching control bus. This enables power to all cabinets to be turned on or off from a single control point. Refer to Figure 3-5 for instructions. All H787Ø and H7872 power supplies must be controlled by the master power switch.

3.3.2.3 D-bus Connections - Each expander is provided with a 18Ø cm (6 ft) BCØ8R shielded cable for interconnecting the D-bus between all cabinets. Figure 3-6 shows a maximum configuration and illustrates how the cables are connected. The top/bottom orientation of the cable connectors, as determined by the position of the striped cable wire, must be consistent throughout. The I/O modules in the H333 and H334 chassis are positioned in right to left sequence. If any slot between two I/O modules is empty, a daisy-chain continuity module (M9Ø19) must be inserted in connectors C and D of that location to maintain continuity of the D-bus.





To install remote switching power control bus:

1. Plug one end into any unused power control connector on the 861 power controller panel, shown above, and plug the other end into any unused connector in the 861 controller in the next cabinet.

2. When all controllers have been bused together in this manner, bus the one in the master cabinet to the H333 front panel power control connector (IP300 and DPM50 systems), or the CPU power control connector (IP11, IP110, and IPV10 SYSTEMS).

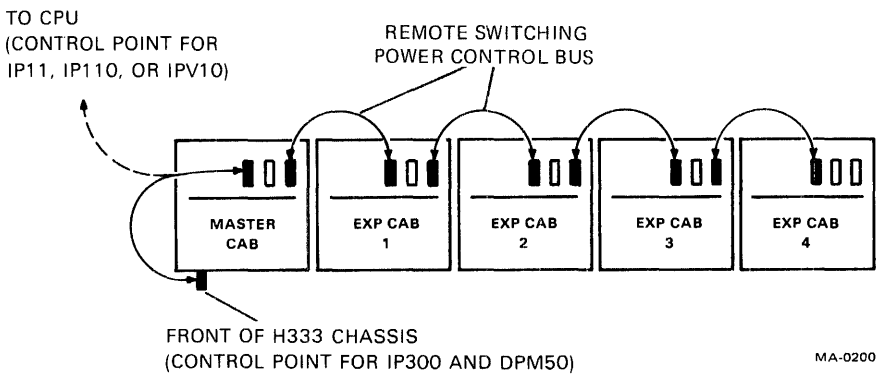


Figure 3-5 Remote Power Connections

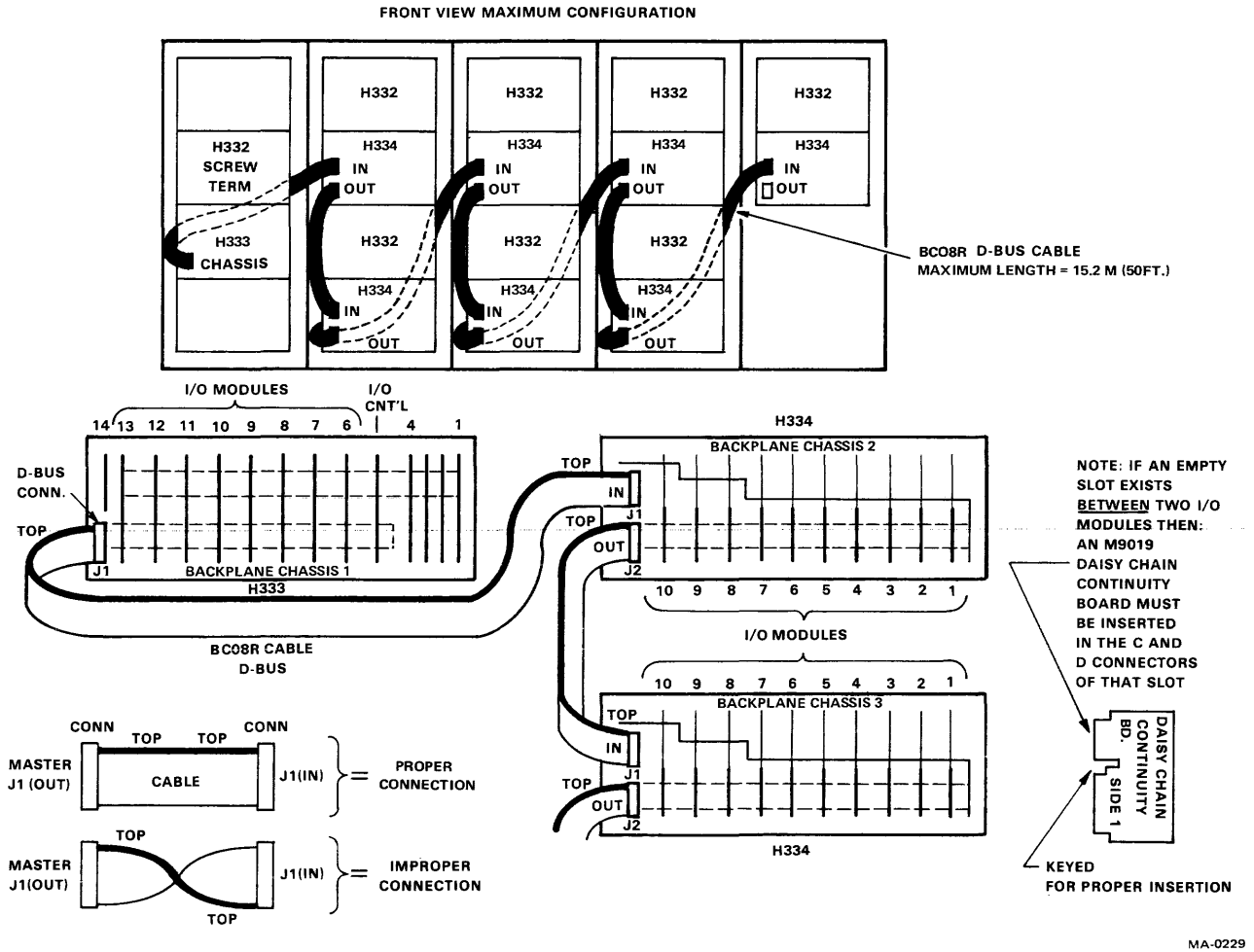


Figure 3-6 D-bus Intercabinet Connections

3.3.2.4 **DC Power Connections** - In the standard configuration, dc power to the module chassis (+12 V, +12 VB, and +5 V when required) is provided by the H7870 and H7872 power supplies included in the H333 and H334 chassis, respectively. Alternate configurations use only the H7870 power supply.

Standard and alternate power supply configurations for all I/O Subsystems are listed in Table 3-1. The table shows that an H333 chassis occupies the first position in all I/O Subsystems except the IP110 and IPV10. The H334 chassis occupies all subsequent positions and the first position of an IP110 or IPV10 system. In all systems the chassis are numbered one through eight.

The H334-X chassis does not include a power supply and must be powered by connecting it to a powered chassis. A 3-conductor, 1.8 m (6 ft) cable (Figure 3-7), is provided for this purpose. Figure 3-7 shows a typical power interconnection configuration.

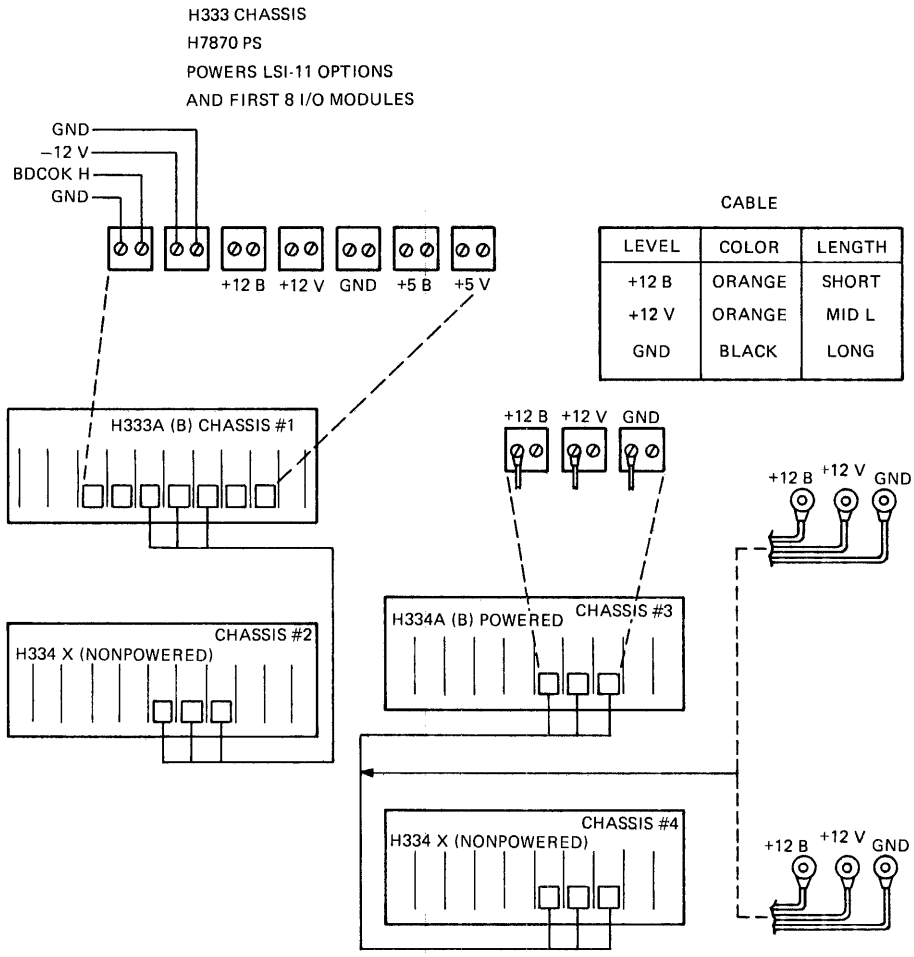
Table 3-1 System Power Supply Usage

Standard Configurations

System	115 V		230 V		Position
	Power Supply	Chassis	Power Supply	Chassis	1 2 3 4 5 6 7 8
IP300 or IP11	H7870	H333-A	H7870	H333-B	X
	H7872-A	H334-E	H7872-B	H334-J	X X X X X X X
IP110 and IPV10	H7872-A	H334-E	H7872-B	H334-J	X X X X X X X X

Alternate Configurations

System	115 V		230 V		Position
	Power Supply	Chassis	Power Supply	Chassis	1 2 3 4 5 6 7 8
IP300	H7870	H333-A	H7870	H333-B	X
	H7870	H334-A	H7870	H334-B	X X X X
	None	H334-X	None	H334-X	X X X
IP11	H7870	H333-A	H7870	H333-B	X
	H7870	H334-A	H7870	H334-B	X X X X
	None	H334-X	None	H334-X	X X X X
IP110 and IPV10	H7870	H334-A	H7870	H334-B	X X X X
	None	H334-X	None	H334-X	X X X X



1. EACH NONPOWERED H334 IS PROVIDED WITH A 6 FT POWER INTERCONNECT CABLE.
2. WHEN INSTALLING THE POWER INTERCONNECT CABLE MAKE SURE THAT THE +12 V AND +12 B WIRES ARE NOT INTERCHANGED.

MA-3000

Figure 3-7 Typical DC Power Connections

3.3.3 Expanding an Existing System

This section covers installation of new cabinets and additional chassis.

3.3.3.1 Adding New Cabinets - To add new cabinets to an existing system, remove system power and follow the procedures in Paragraphs 3.2 through 3.3.2.4.

3.3.3.2 Adding H334 Chassis to Existing System - The information in this section and the cabinet installation procedure in Paragraph 3.3.2 provides enough information for expansion to a maximum configured system.

If there is space available for adding a new chassis in the original cabinet, but not enough module slots, the customer may order a number of H334 chassis and I/O modules. He may also buy screw terminal assemblies to accommodate the H334 field wiring.

The following procedure describes the method for installing an additional H334 chassis and screw terminal assembly in the unused mounting space of an existing system.

1. Remove system power.

2. Remove the two pop-out panels and the mounting hardware from the front lower half of the expansion cabinet. These panels may be discarded.

3. Mount the H332 screw terminal cage and the H334 chassis in the cabinet (Figure 3-8).

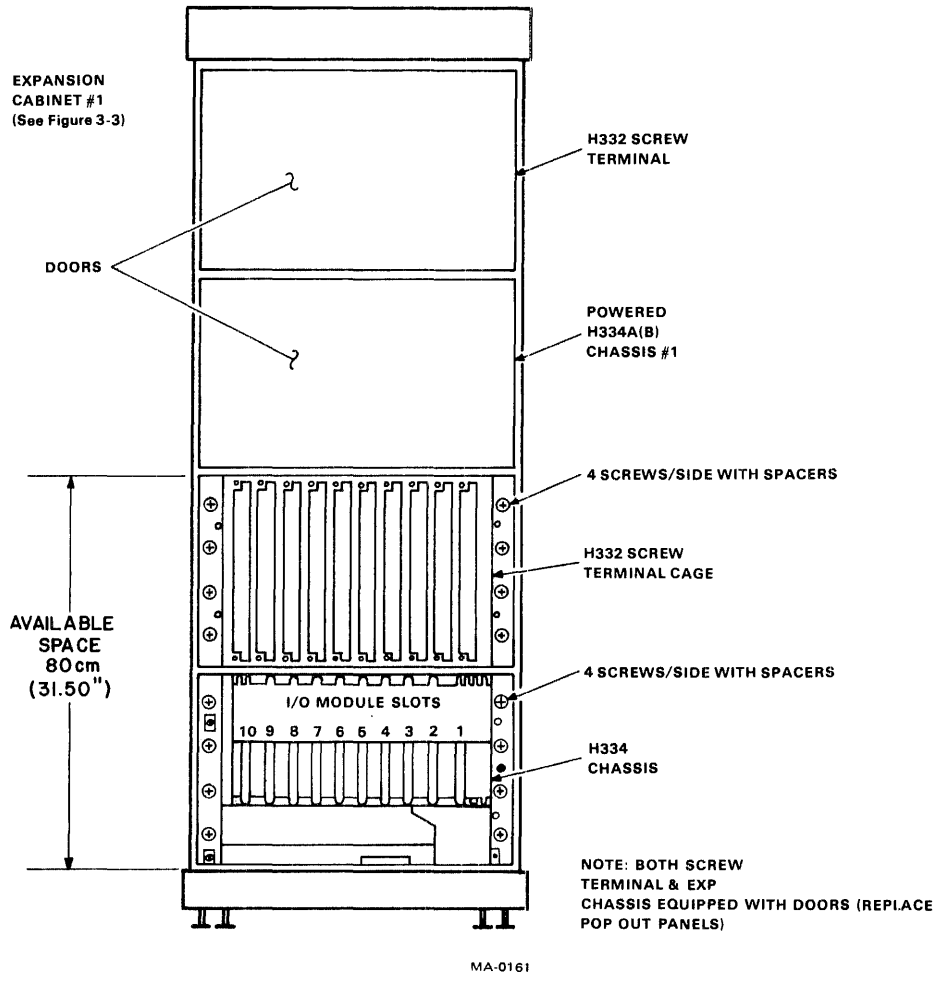


Figure 3-8 Example of I/O Expansion

NOTE

For shipping purposes only, the power supplies are secured in place with four screws through the bottom of the H334 chassis. Remove the screws at this time to allow access for future servicing.

4. Install the BC40ØA and/or BC40ØB screw terminal strips (Figure 3-9). Some installations substitute BC40ØL screw terminal strips in place of BC40ØAs in order to provide space for user mounted components. The BC40ØL and its installation are described in Chapter 6.

5. Install the D-bus cable as described in Paragraph 3.3.2.3 and shown in Figure 3-6.

6. Install the dc power harness as described in Paragraph 3.3.2.4 and shown in Figure 3-7.

7. Fasten the ground lug to the equipment rack side rail with the 1Ø-32 X 1/2 inch screw, 1Ø-32 Kep nut, and No. 1Ø external tooth lockwasher provided. The lockwasher must be placed under the ground lug and the nut fastened securely to ensure good contact with the equipment ground through the paint (Figure 3-1Ø).

3.3.3.3 **Adding New Modules to an Existing System** - Perform the following steps and insert the I/O modules into the H334 chassis.

CAUTION

I/O Subsystem modules utilize CMOS devices and require special handling to prevent damage from static charges. Each new module is in an antistatic plastic envelope to protect it from static voltages. Do not remove the module from the plastic envelope until just before installation. Hold the module by its handle while removing it from the envelope, manipulating its switches, and plugging it into its assigned location. Do not touch the module's contact fingers, components, or the printed wiring. If the module must be placed on a bench momentarily, place it on the plastic envelope. The plastic envelope should not be discarded since it may be necessary to repackage the module for reshipment. Warranty repairs will not be performed on modules returned without the plastic envelope.

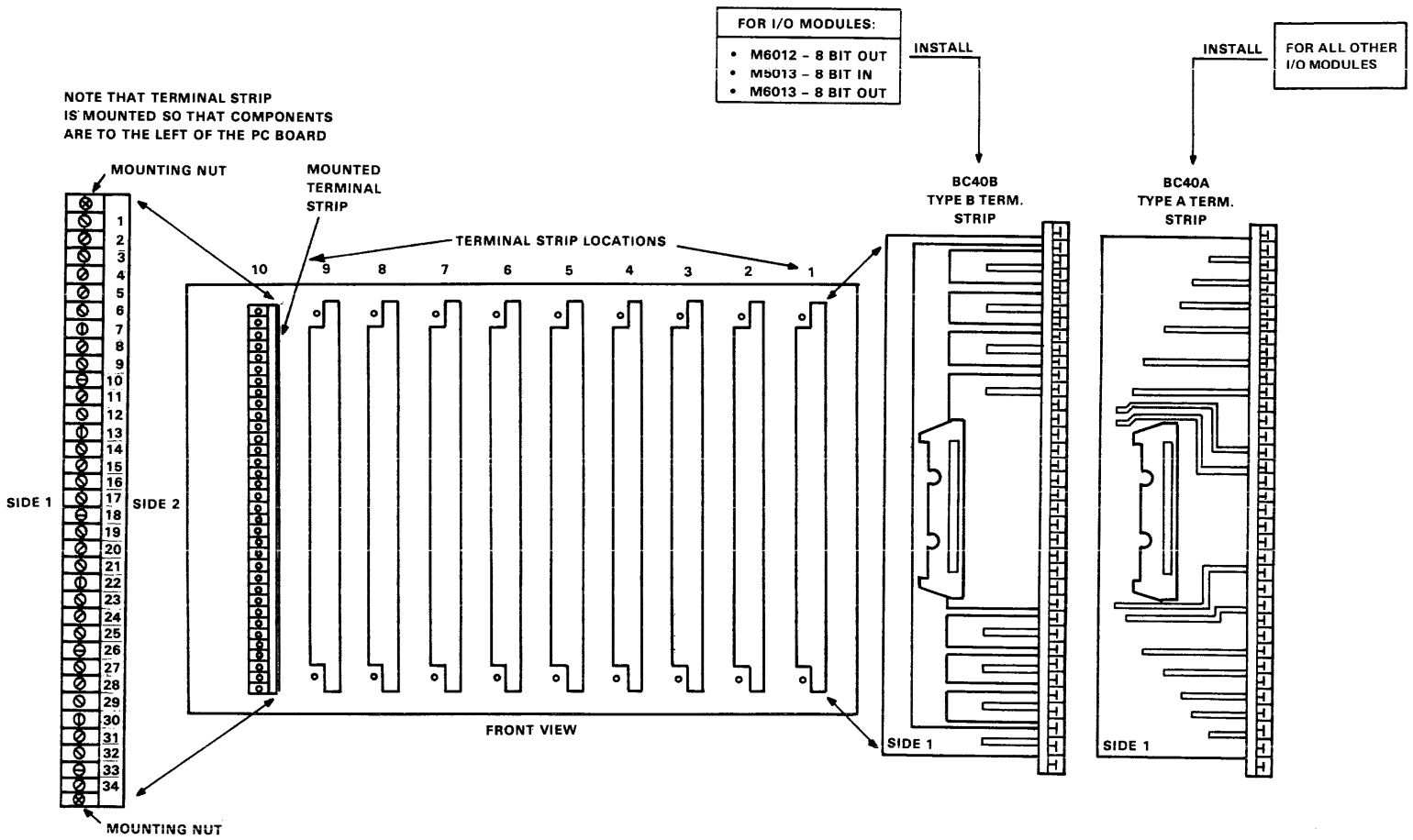


Figure 3-9 Terminal Strip Installation

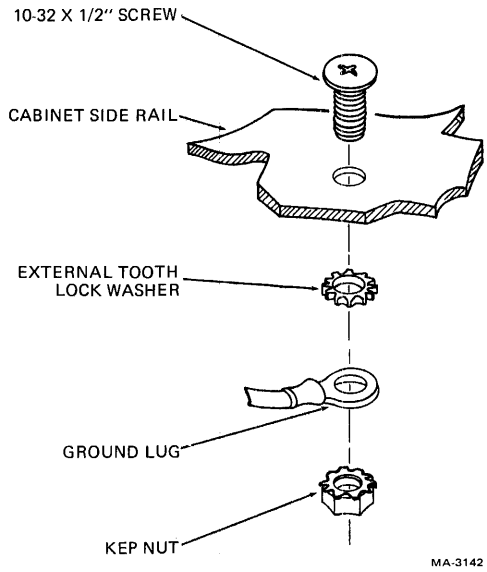


Figure 3-10 Ground Wire Fastening

1. Assign an address to each I/O module. Each module contains one or more switches which must be set in accordance with the I/O Subsystem address assignment plan. Switch implemenation is not identical for each module type; therefore, the individual module data sheets in Chapter 6 must be consulted to determine the correct selection procedure.

2. Make sure that fuses and LEDs are properly seated in their sockets. If an LED has become unseated, reinstall it with the cathode toward the dot etched on the printed circuit board. Do not force it past the stop in the socket.

3. Refer to Figure 3-11 and make sure that the terminal strip types and respective I/O modules are inserted into corresponding slot locations.

4. Install termination cables between J1 connectors on I/O modules and J1 connectors on terminal strip boards (Figure 3-12).

5. A plastic cover is supplied for each terminal strip. These plastic covers must be installed following field wiring to ensure the safety of operating personnel.

6. A plastic cover is supplied for both the screw terminal assembly and the H334 chassis (Figure 3-13). Again, for the safety of operating personnel, the plastic cover for the screw terminal assembly must be mounted after the field wiring is done and the individual strip covers have been installed. The plastic cover for the H334 chassis

can be installed when all I/O modules and their termination cables have been installed, and acceptance procedures run.

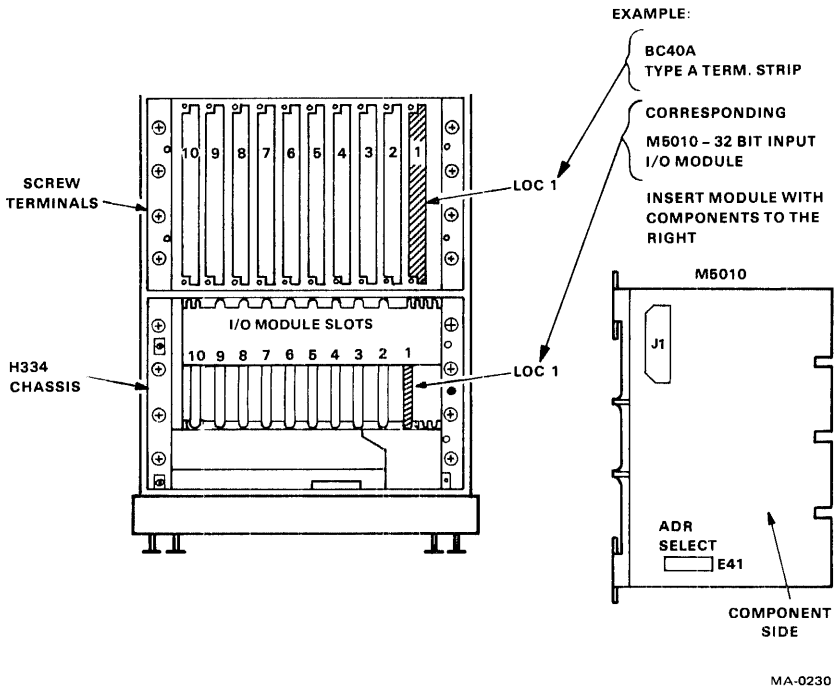


Figure 3-11 Module and Screw Terminal Configurations

3.3.4 Connecting to Primary Power

Before connecting to system primary power perform the following.

1. Check each 861 power controller to make sure that its power matches that required at the site. The 861-B requires 180-270 V, 47-63 Hz; the 861-C requires 90-135 V, 47-63 Hz.

2. Check the H333 model designation to make sure that its power matches site power and the 861 power controller. The H333-A requires 100-127 V, 47-63 Hz; the H333-B requires 200-254 V, 47-63 Hz. If necessary, model B can be reconfigured to work on model A voltages and model A reconfigured for B voltages.

3. Make sure that each powered H334 chassis matches the power requirements of the site. The H334-A and -B designations have the same meaning as for the H333 chassis. H334-E and -J designations are analogous to the H334-A and -B, except that they denote an H7872 power supply instead of an H7870.

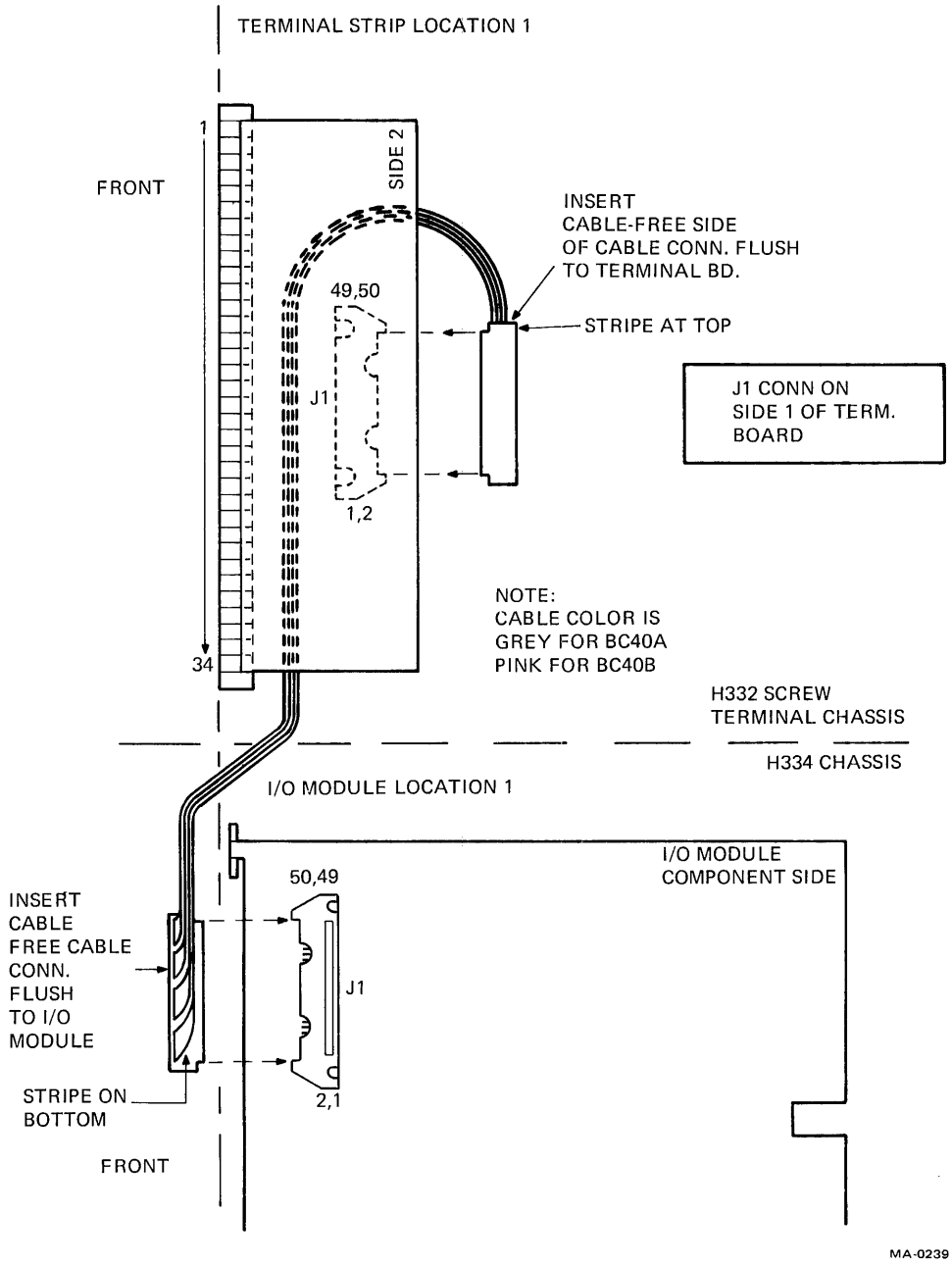


Figure 3-12 Termination Cable Installation

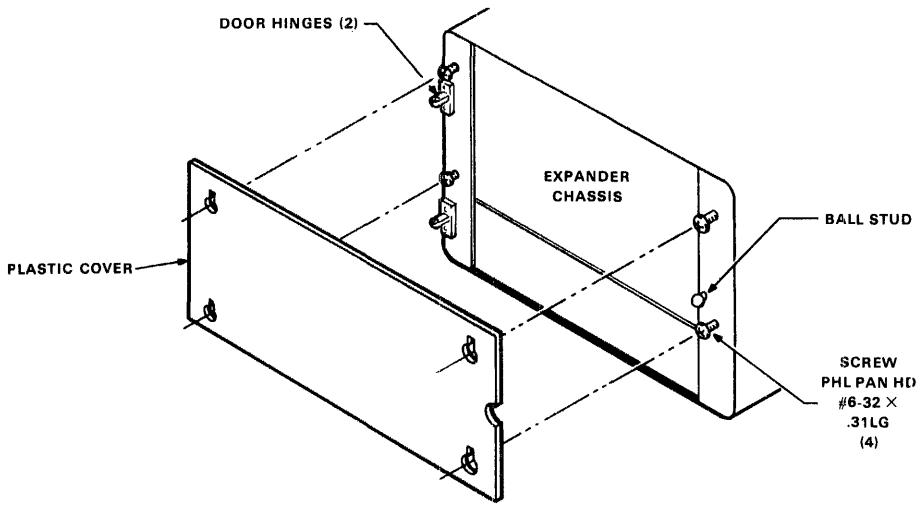


Figure 3-13 Plastic Cover Installation

The H333 chassis contains an H7870 power supply. The H334 chassis contains either an H7870 or an H7872 power supply. Internal jumpers select 115 V or 230 V operation in each case. Figures 3-14 and 3-15 show the required jumper configuration for each voltage selection.

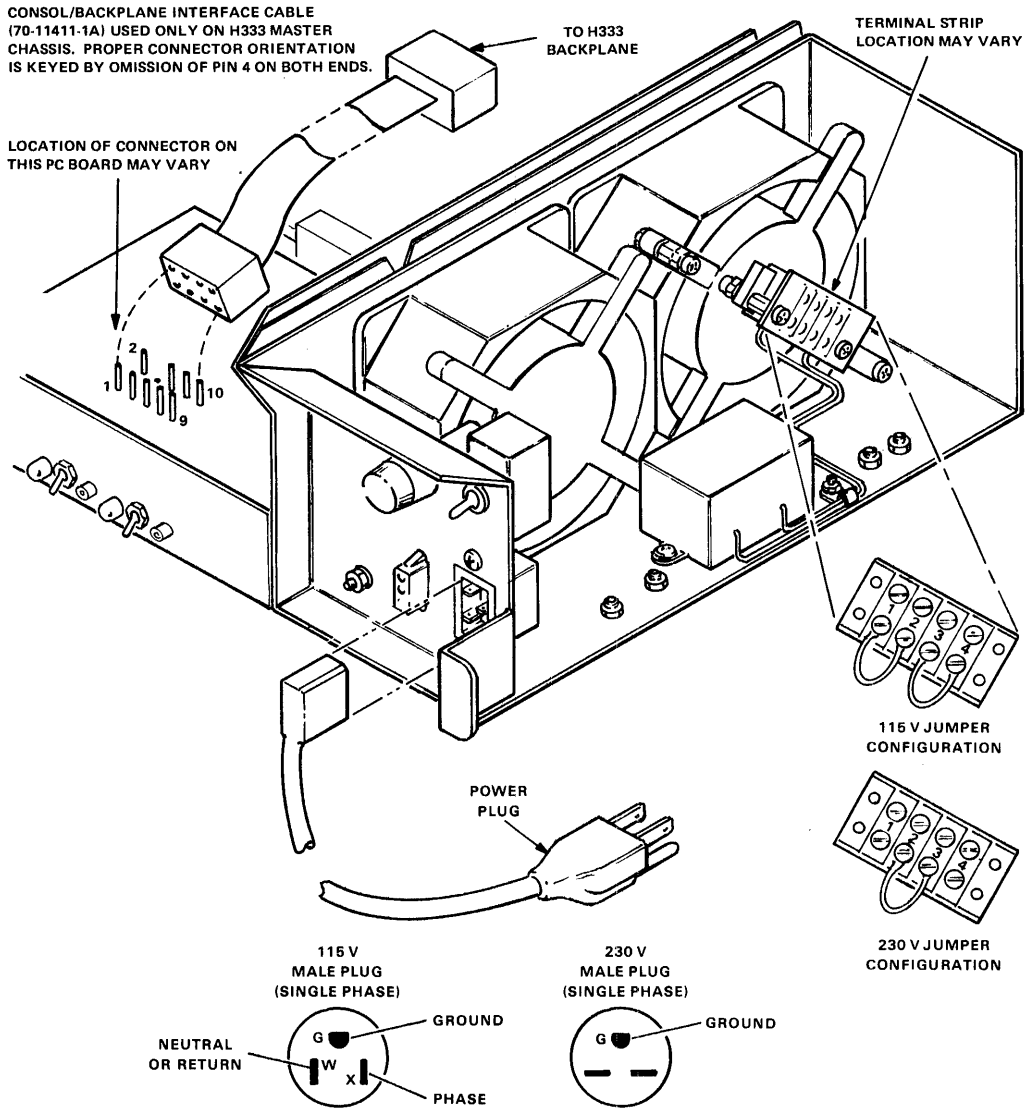
4. Make sure that the H333 chassis is equipped with a console/backplane interface cable (70-11411-1A). The backplane end of this cable may be observed between slots 4 and 5 of the chassis. If for any reason this cable is disconnected, it must be reinstalled with the orientation shown in Figure 3-14.

To connect the subsystem to primary power, proceed with the following steps.

1. Set the 861 power controller REMOTE, LOCAL ON/OFF switch to off. Plug each powered chassis into one of the 861 switched circuit outlets in its respective cabinet.

2. Plug the ac line cord from each cabinet into the primary power receptacle. Power controller indicators should come on.

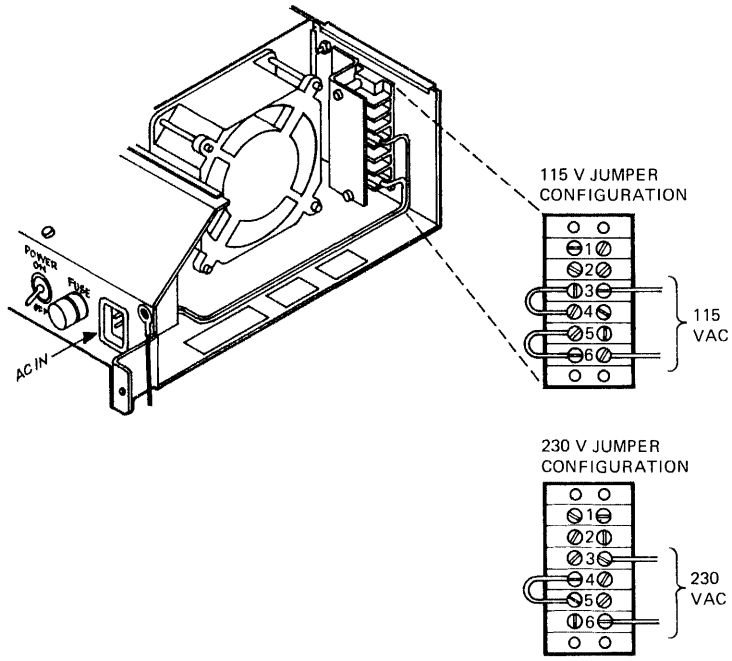
3. Set the circuit breaker switch on all 861s to the on position.



TYPE OF SERVICE	POLES	WIRES	POWER CONFIGURATIONS					FUSE	POWER SUPPLY JUMPER CONFIGURATION
			PLUG			RECEPTACLE			
			NEMA*	DEC PART NO	HUBBEL	DEC PART NO	HUBBEL		
115 V, 15 AMP	2	3	5-15 P	90-08938	5266-C	12-05351	5262	6.25 A 250 V SB	1-2, 3-4
230 V, 15 AMP	2	3	6-15 P	90-08853	5665-C	12-11204	5662	3 A 250 V SB	2-3

MA-0176

Figure 3-14 H7870 Power Supply Conversion



TYPE OF SERVICE	POLES	WIRES	POWER CONFIGURATIONS					FUSE	POWER SUPPLY JUMPER CONFIGURATION
			PLUG			RECEPTACLE			
			NEMA	DEC PART NO.	HUBBEL	DEC PART NO.	HUBBEL		
115 V, 15 AMP	2	3	5-15 P	90-08938	5266-C	12-05351	5262	2 A 250 V SB	3-4, 5-6
230 V, 15 AMP	2	3	6-15 P	90-08853	5665-C	12-11204	5662	1.5 A 250 V SB	4-5

MA-3001

Figure 3-15 H7872 Power Supply Conversion

3.3.5 Optional NEMA-12 Enclosure Considerations

If site environmental conditions dictate, the I/O Subsystem may be installed in a NEMA (National Electrical Manufacturers Association) type-12 industrial enclosure. The chosen NEMA enclosure must be at least 30.5 cm (12 in) deep. Figure 3-16 shows the mounting hole dimensions and spacing required. An important part of choosing such an enclosure is careful consideration of the power versus temperature constraints as discussed in a later paragraph.

NEMA enclosures are available in a variety of sizes to accommodate varying needs. Two types that are especially made for I/O subsystem service are described below. For information about ordering these enclosures or any custom enclosures refer to DIGITAL brochure number ED01315-126.

3.3.5.1 NEMA Enclosure Descriptions - The enclosures described here are NEMA type 12 standard industrial enclosures that have been especially designed for I/O subsystem service. As such, they conform to National Electrical Manufacturers Association (NEMA) type 12 (industrial use) specifications. That is, they are

intended for indoor use to protect the enclosed equipment against fibers, flyings, lint, dust, and dirt; and from light splashing, seepage, dripping, and external condensation of noncorrosive liquids. Note that there are other NEMA specifications that address different environments; and suitable enclosures can be obtained to meet these requirements.

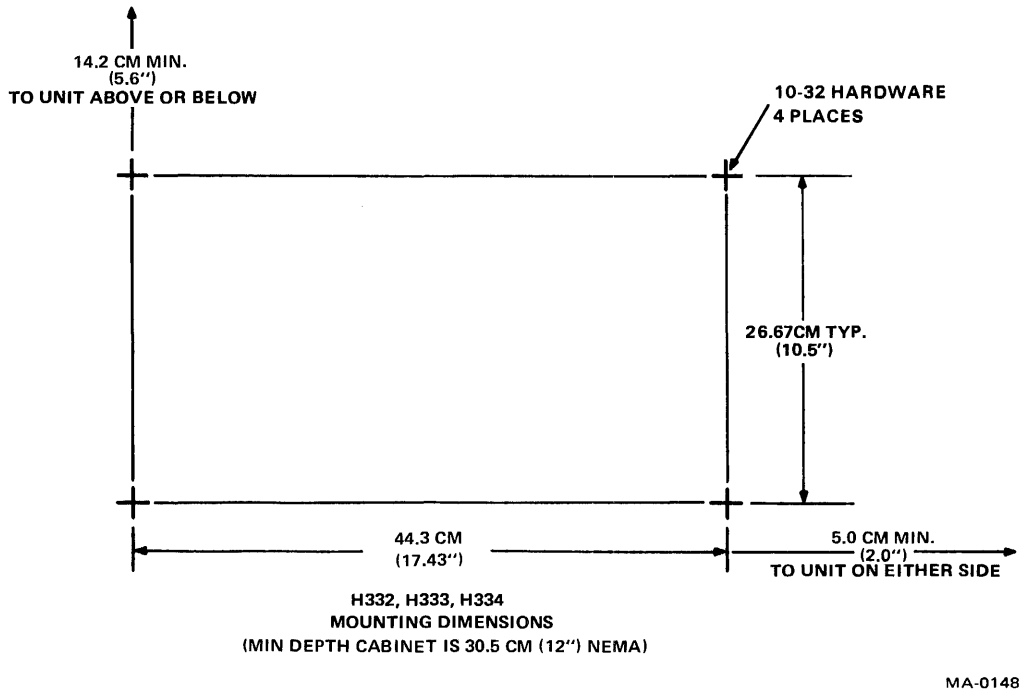


Figure 3-16 I/O Subsystem Rear Mounting Dimensions

These enclosures (Figure 3-17) are two-door floor-mounted cabinets. They are 6 feet tall, 5 feet wide, and one foot deep. They are mounted on one foot high floor stands, and are constructed of 12 gauge steel. Doors are equipped with neoprene gaskets that are attached with oil resistant adhesive and steel retaining strips. Three-point latching mechanisms, operated by oil-tight, key locking handles, hold the doors securely in place. Fans circulate internal air to reduce temperature gradients inside the enclosure. There are fittings at the top and bottom of the enclosure that allow the use of compressed air to aid in heat removal or to keep the internal atmosphere cleaner than ambient.

All enclosures have holes in the sides, top, and bottom that will meet most wiring installation requirements. When enclosures are delivered, these holes are sealed with oil and dust-tight plugs. The user unplugs only those holes needed for his installation.

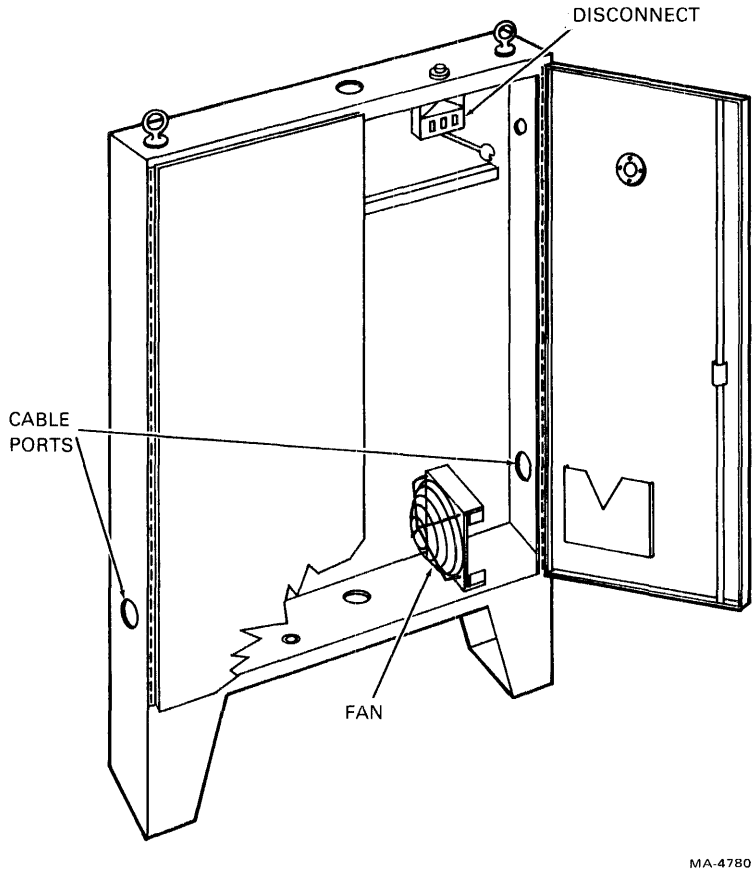


Figure 3-17 NEMA-12 Enclosure

Each enclosure contains a three-pole power disconnect that is attached via a rod through the door to its operating handle on the front of the enclosure. For the safety of operating personnel, the handle is interlocked so that the door cannot be opened unless the switch is in the off position. This safety feature can be negated by authorized maintenance personnel via a concealed release screw (Figure 3-18).

For the protection of plant maintenance personnel, the switch handle can be padlocked in the off position to prevent its being operated during maintenance of external equipment. A simple field alteration allows the switch to be padlocked instead in the on position, for applications that require that feature.

The significant difference between the two types of enclosures is in the chassis-mounting hole pattern on the rear panel, as discussed below.

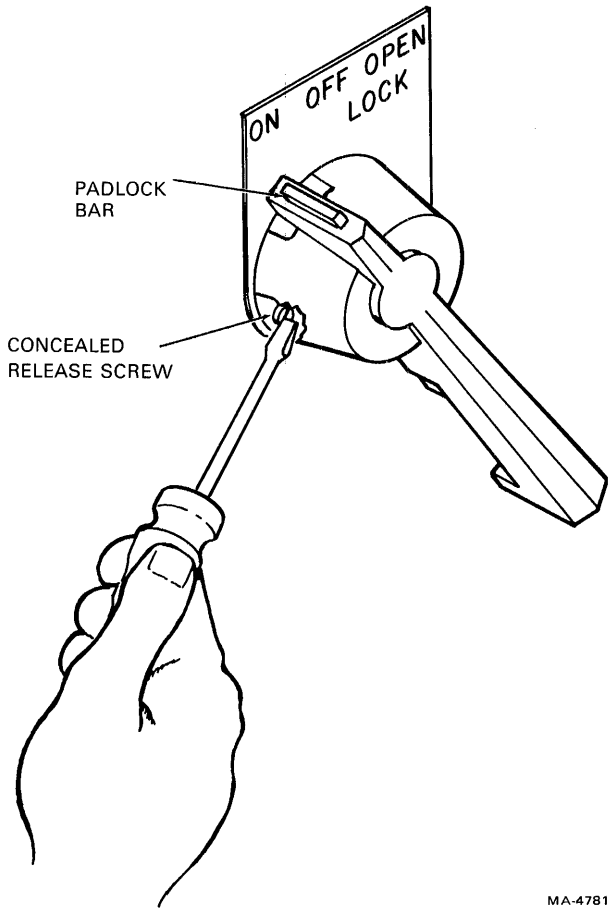


Figure 3-18 Typical Disconnect Operating Handle

Option 1 - This enclosure (Figure 3-19) is intended for use with I/O subsystems that use the standard BC4Ø screw terminals. Its rear panel hole pattern provides for the mounting of two module chassis and two H332 screw terminal chassis. It has one vertical and one horizontal cable race.

Option 2 - This enclosure (Figure 3-19) is intended for use with I/O subsystems that require ATR16 isothermal screw terminals. Its rear panel hole pattern provides for either one module chassis and ten ATR16 chassis, or one module chassis, one H332 screw terminal chassis, and eight ATR16 chassis. It has two vertical cable races.

Power Controller Option - Power to all I/O subsystem chassis and to the enclosure fans must be controlled from a single point as discussed in Paragraph 3.3.2.2. In addition, the user must provide filtering of the incoming ac that is used to power the I/O subsystem. The use of an 861 power controller (or equivalent) in each NEMA enclosure is recommended to satisfy these requirements. These controllers have switched outlets for all ac powered devices in an enclosure, and include a suitable ac line filter.

Multienclosure systems have their control bus connectors bussed together and to a master control point, which is used to turn on the entire system at once. The 861 power controller can be installed on the bottom left side of the enclosure.

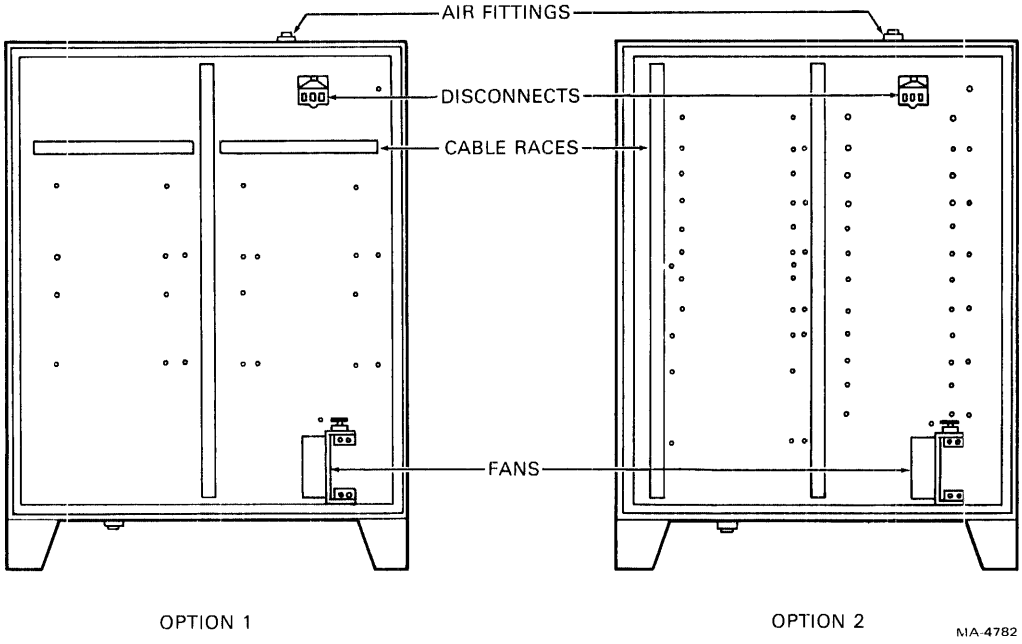


Figure 3-19 NEMA-12 Type Enclosures

3.3.5.2 **Maximum Power Dissipation** - When planning a NEMA-12 enclosure installation, the user must take into consideration the fact that the maximum allowable ambient temperature at the enclosure location can be less than what it would be for a standard DEC cabinet installation (i.e., 50° C). This is because, in the absence of an air purge, heat produced by the enclosed equipment becomes trapped inside the enclosure and can only escape by conduction through the walls of the enclosure. A standard cabinet, on the other hand, has a flushing fan that continuously circulates the ambient air. For a given site ambient temperature therefore, the temperature rise inside a NEMA-12 enclosure will be higher than that inside a standard DEC cabinet.

A complete description and evaluation of all the factors contributing to the temperature rise inside the enclosure is beyond the scope of this document. However, for the enclosures under consideration, a useful approximation of the amount of this temperature rise is

$$\Delta T = 1.67 \frac{P}{A}$$

Where ΔT = difference between inside and outside ambient temperatures (^{o} C)

P = Power dissipation of all equipment in the enclosure (watts - if power is in BTU/hr, use Ø.488 instead of 1.67)

A = The unobstructed outside surface area of the enclosure (sq ft)

The surface area of the enclosure (6'X5'X1') is 82 sq ft. If it is installed with the rear panel against a wall, the effective area is reduced to 52 sq ft.

The circulating fan increases heat transfer efficiency so that the maximum temperature at critical locations inside the enclosure can be 6Ø^{o} C (128.3^{o} F).

The following example demonstrates what this means to the user. The cabinet is installed against a wall, and the maximum ambient temperature at the intended site is expected not to exceed 38^{o} C (1ØØ.4^{o} F). Transposing the above formula gives

$$\begin{aligned} Pmax &= Ø.6\ A\ (T_1 - T_2) \\ &= Ø.6 \times 52\ (6Ø - 38) \\ &= 686 \text{ watts} \end{aligned}$$

where T_1 and T_2 are respectively the maximum temperature allowed at critical locations inside the enclosure, and the maximum temperature anticipated at the site.

At a site where the ambient temperature can reach 38^{o} C, this means that the total power dissipation of all equipment in the enclosure must not exceed 686 watts. When calculating the total power contribution of all the devices in the enclosure, remember to include the power used by the fan (53 W). In the above example, after allowing 53 W for the fan, there would remain 633 W (686-53) for I/O Subsystem power.

The relationship is shown by curve (a) of Figure 3-2Ø, which is a plot of maximum allowed enclosure power versus maximum ambient temperature of the site. Curve (a) is for the case where the enclosure is installed against a wall, reducing the effective surface area to 52 sq ft. Curve (b) is for the case where the enclosure is free standing so that its entire 82 sq ft surface area can radiate heat effectively. Note that these curves are only linear approximations of what occurs in this enclosure with a typical I/O Subsystem installation. They should not be used for other than I/O Subsystem installations, or other enclosures.

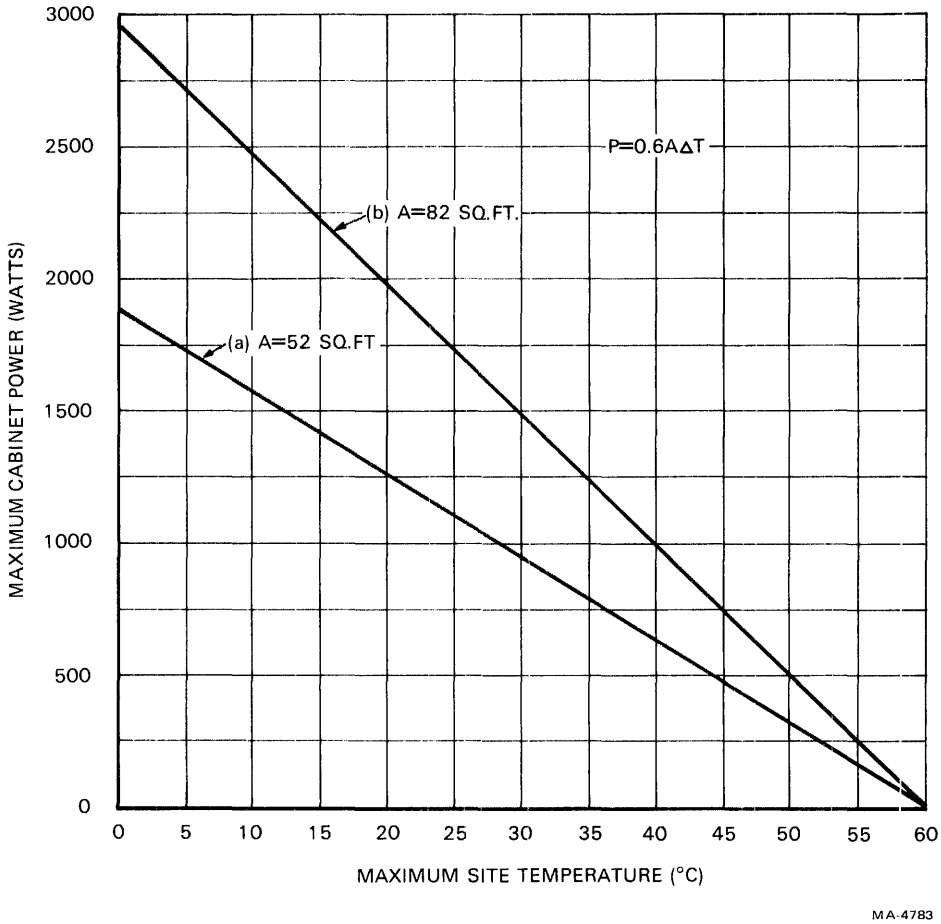


Figure 3-2Ø Cabinet Power Versus Site Temperature

3.3.5.3 Air Purging - Pipe fittings (1/2 in) are provided at the top and bottom of the enclosure for the installation of compressed air. Compressed air can be used to maintain a positive clean air pressure to eliminate dust. It can also be used for cooling.

3.3.5.4 NEMA Enclosure Installation

WARNING

NEMA type enclosures of this size are heavy and unstable. They must be bolted down or otherwise secured before opening the doors or THEY CAN TIP OVER.

When planning the installation of a multienclosure system, make sure that the enclosures are placed close enough together to allow the D-bus cable to reach from one chassis to the next in an adjacent enclosure. The five inch holes in the side of the enclosure can be used for this purpose, but the D-bus should not be exposed to the plant environment. It is recommended that conduit be used to join the enclosure.

When the enclosures have been unpacked and inspected, move them to their final locations, bolt them to the floor through the holes provided in the enclosure feet, and proceed as follows.

1. Connect all enclosures together with at least a number 12 AWG ground wire. Fasten these wires to the studs provided in the enclosure rear panel (Figure 3-21). Fasten them in the same manner as the chassis ground lugs (Paragraph 3.3.3.2, step 7) to ensure ground continuity between enclosures.

2. Install a power controller in a suitable location within each enclosure. The user must provide hardware to secure the controllers in place.

3. Place the H333, H332, and ATR16 chassis in their assigned locations and fasten with the 10-32 X 1/2 inch screws (provided with the chassis) to the tapped holes in the enclosure's rear panel. Attach each chassis ground lug to studs provided on the rear panel in the manner discussed in Paragraph 3.3.3.2, step 7. ATR16s should be mounted on spacers (provided) for maximum thermal isolation.

4. Remove the ac plug from the 15 foot cable attached to the power controller, cut the cable to length, and connect the black and white wires to two of the bottom contacts of the disconnect switch (Figure 3-21). Connect the green wire to one of the ground studs.

5. Remove the safety cap from the disconnect's top contacts, connect the enclosure ac input to these contacts, and replace the safety cap. Connect the ground wire to one of the ground studs.

6. Connect a power cord to the fan terminal strip (Figure 3-21). Plug the other end into one of the power controller switched outlets.

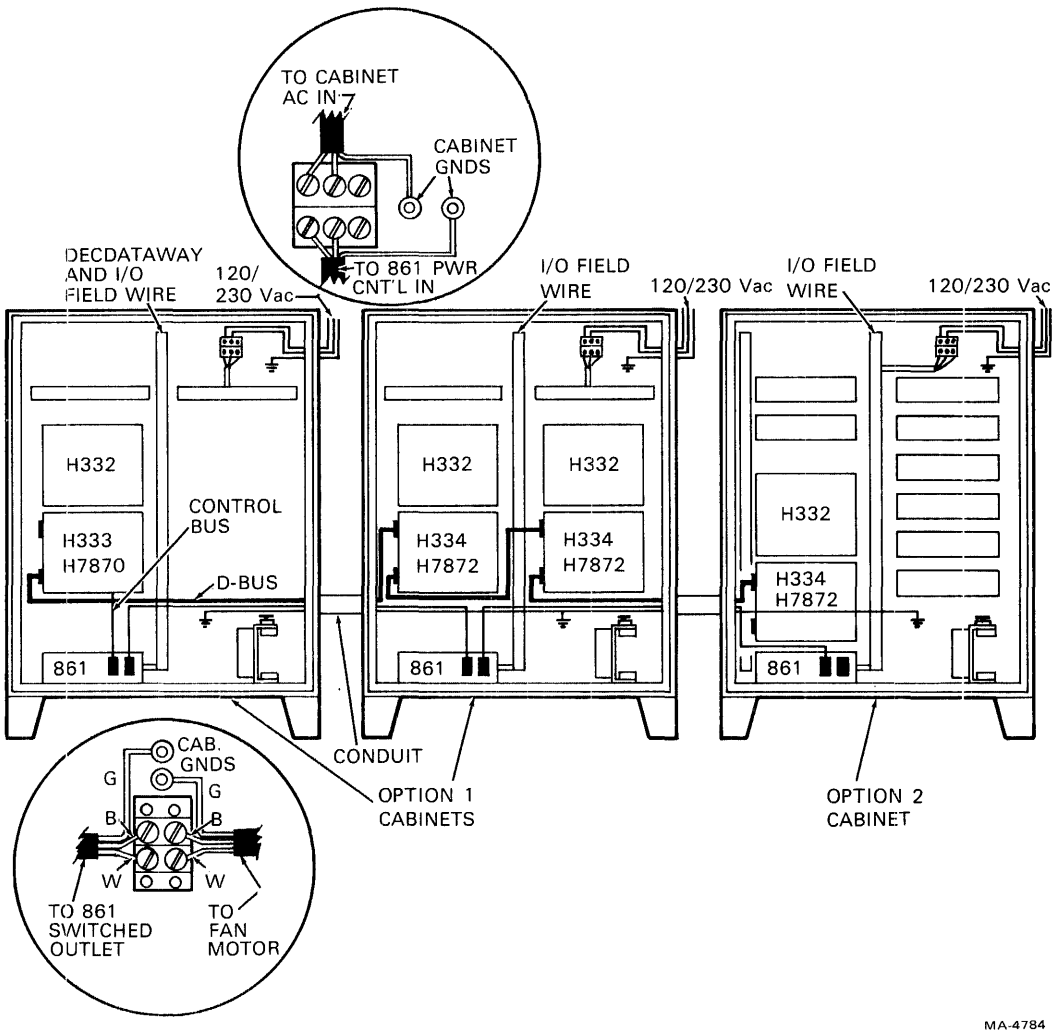


Figure 3-21 Typical NEMA-12 Cabinet Installation

7. Plug any H333 or H334 chassis power cord into a switched outlet on the 861 power controller.

8. Connect all enclosure power controllers together with a power control bus (Figures 3-5 and 3-22). Connect the main control point chassis to the power controller in its cabinet. Wire the spare disconnect contacts of all enclosures in series. Connect the one in the first enclosure to pin 1 of the control bus. Connect the one in the last enclosure to pin 3 of the control bus (Figure 3-22). This enables turning the system on and off when the doors are opened via the power switch on the front of the main control chassis. When the doors are closed, all disconnect switches must be turned on to turn on the system. Any one will turn it off.

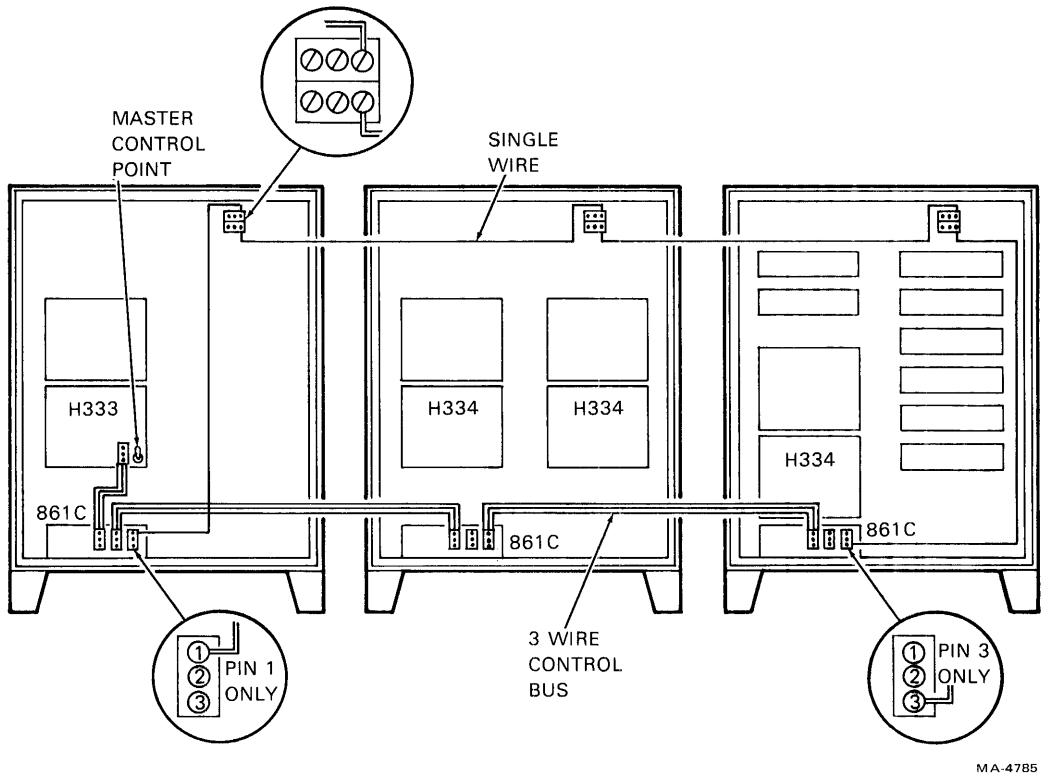


Figure 3-22 Typical Control Wiring

9. Interconnect all module chassis with the D-bus cables provided with each H334 chassis (Figures 3-6 and 3-21). The BCØ8R-Ø6 cables provided for a DEC cabinet installation are six feet long (the cable number suffix designates the length). Longer cables may be specified if necessary. Cables are available in 8, 9, 1Ø, 12, 15, 18, 25, and 3Ø foot lengths.

NOTE

A restriction here is that the combined length of all D-bus cables in a system must not exceed 5Ø feet.

1Ø. Connect to primary power as described in Paragraph 3.3.4.

3.3.5.5 NEMA Enclosure Field Wiring - General I/O subsystem field wiring considerations are discussed in later paragraphs. The NEMA enclosures discussed above have two features that make the task easier. First, the user has a choice of several cable ports that allow entry from the top, bottom, or sides. Second, there are cable races with snap-on covers to simplify the routing of the enclosure's internal wiring.

3.4 CHECKOUT PROCEDURES

3.4.1 Cabinet Power Check

The following procedure for applying system power ensures that all 861 power controllers, all H787Ø and H7872 power supplies, and the power control bus are operational.

1. Remove all I/O modules from all subsystem chassis.

2. Set each power controller REMOTE, LOCAL ON/OFF switch to LOCAL ON. All cabinet fans should be operating.

3. Turn on all H787Ø and H7872 power supplies. Power supply front panel dc indicators should come on.

4. Turn off the I/O subsystem master power switch. (This may be either the H333 chassis power switch or, if the system is an IP11Ø or an IPV1Ø, the PDP-11 CPU power switch.)

5. Set the REMOTE, LOCAL ON/OFF switch on all 861 power controllers to REMOTE. DC power to all H333 and H334 chassis should be off.

6. Turn on the system master power switch. DC power to all chassis should come on.

7. Check the dc voltages at the test points provided on the front panels of all H787Ø and H7872 power supplies. Voltages should be within ±3% of their nominal values. If adjustment is necessary, refer to Chapter 7. Note that the nominal value of the 5 V supply is 5.1 V.

8. Turn off the system master power switch and reinstall the modules that were removed in step 1.

9. When all modules have been installed, turn the system master power switch on.

3.4.2 Operational Check

Equipment operation is checked by running the Field Test Program and by performing the Acceptance Procedure (A-SP-H333-Ø-7). If multiple I/O modules are used, the rules for address selection given in Paragraph 4.2.1 must be followed before starting the Acceptance Procedure. For instructions on how to run the tests, refer to the Acceptance Procedure and the documentation included with the software.

3.5 SYSTEM CONFIGURATION PROCEDURES

3.5.1 Configuring the System for Operation

After installation and checkout of the new equipment by DIGITAL Field Service, the customer can begin to configure the system. To accomplish this, proceed as follows.

1. Use the information contained in the I/O module data sheets in Chapter 6 for each type of module included in the system.

2. Determine how the I/O modules will be organized on the D-bus, i.e., in what slot each module is to be installed, and the address to be assigned to each module. Then remove the modules from their present slots, select the addresses, and reinstall them in the desired order.

   I/O module address assignment is independent of the module's location on the D-bus, but is subject to the rules stated in Chapter 4, Paragraph 4.2.1.2. Although address and location are independent, location does determine priority for the interrupting type modules. It is highest for modules closest to the control module on the D-bus.

NOTE

When an I/O Subsystem is shipped with modules installed, the organization of the modules in the chassis is standardized for manufacturing and may require reorganization to suit the needs of the customer.

3a. The M8719 UNIBUS I/O control module is the bus interface module for IP11Ø subsystems. It must be configured for its assigned priority level, device address, and interrupt vector. The priority level is changed by replacing the priority plug located on the module. The M8719 normally has a priority level of six; however, this can be changed for special applications. Device address and interrupt vector are selected via switch packs E49 (for address) and E18 (for vector) on the module. The locations of the priority plug and switch packs is shown in Figure 3-23. The use of these switches for selecting device address and vector is illustrated in Figure 3-24.

3b. The M7958 I/O control module is the bus interface module for IP11, IP3ØØ, and DPM5Ø subsystems. It must be configured for its assigned device address and interrupt vector. This is done via the switch packs E34 (for address) and E7 (for vector) on the module. The location of these switch packs is shown in Figure 3-25. The use of these switches for selecting the device address and vector is illustrated in Figure 3-26. One of the switches on E34 is used for initialize select. This switch should be on.

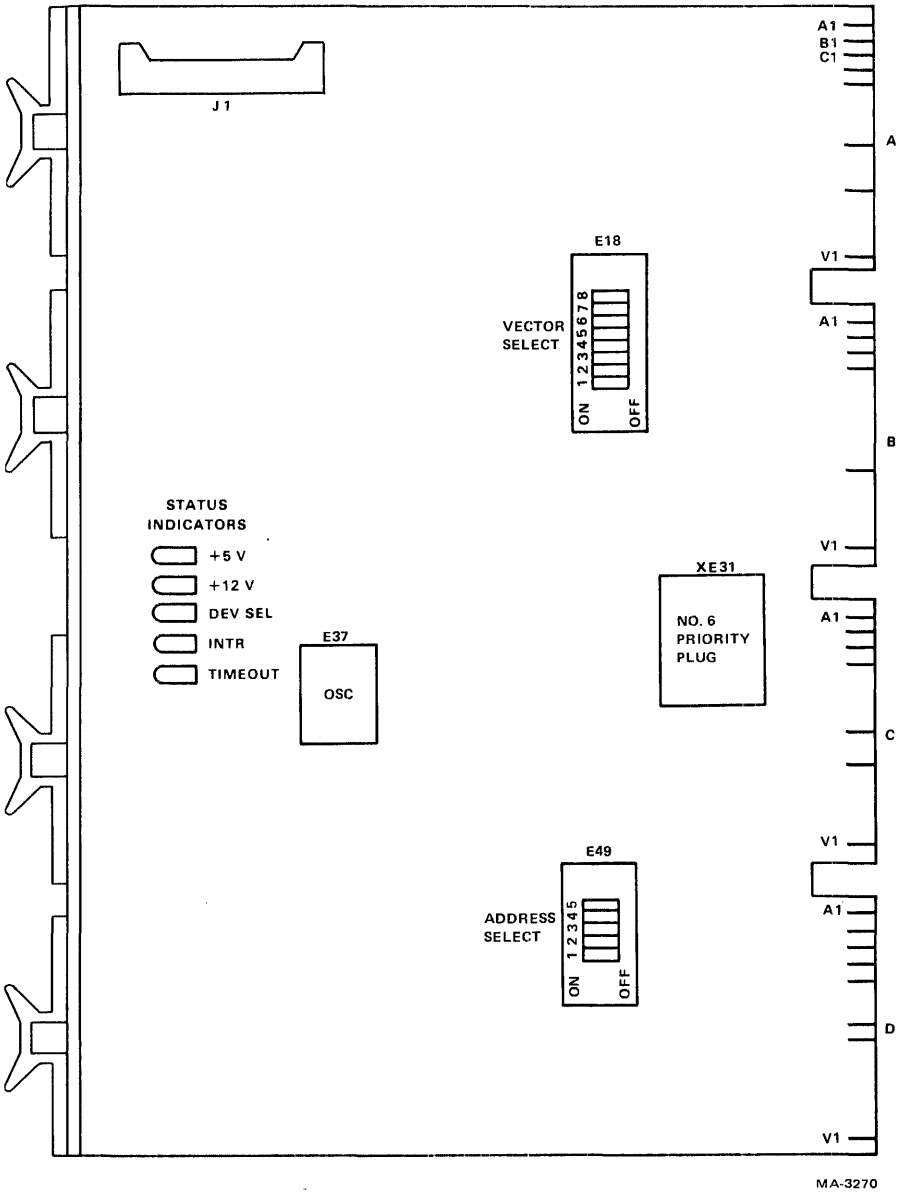


Figure 3-23 M8719 UNIBUS I/O Control Module

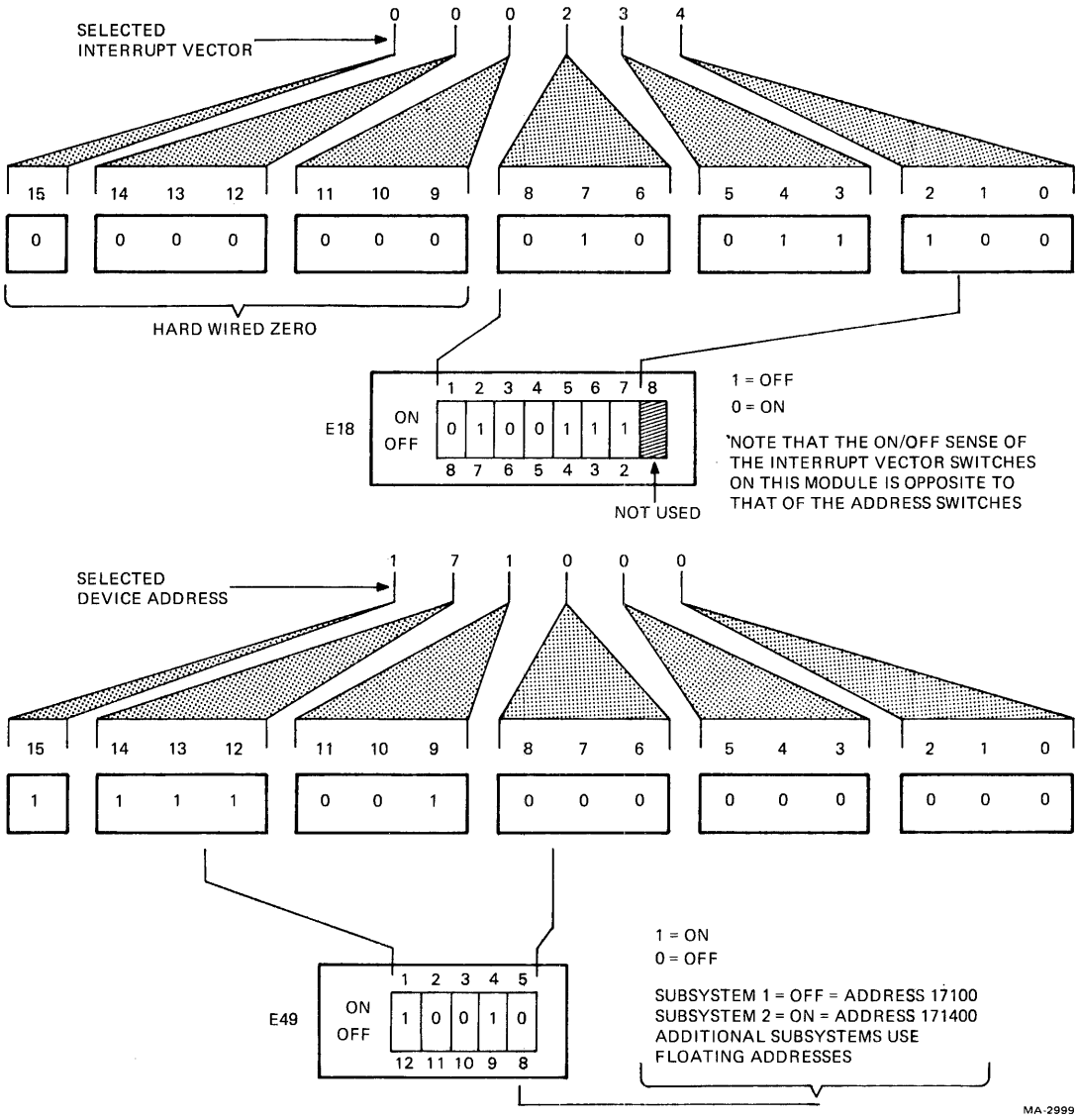


Figure 3-24 M8719 Address and Vector Selectors

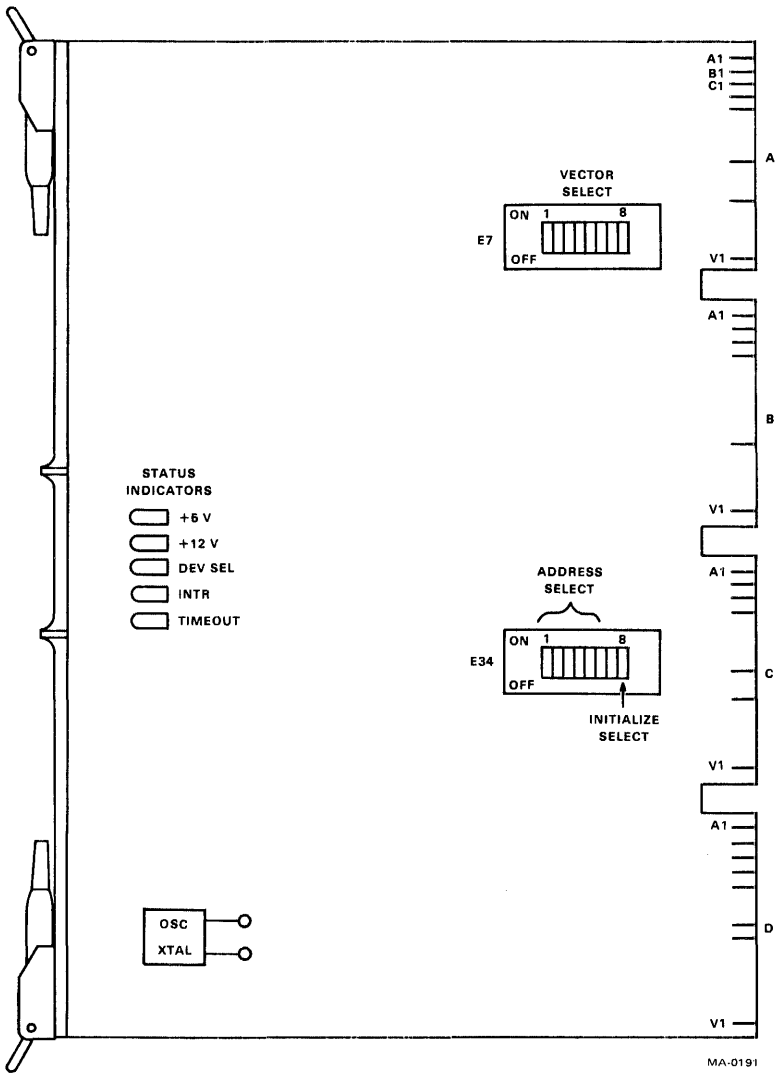


Figure 3-25 M7958 I/O Control Module

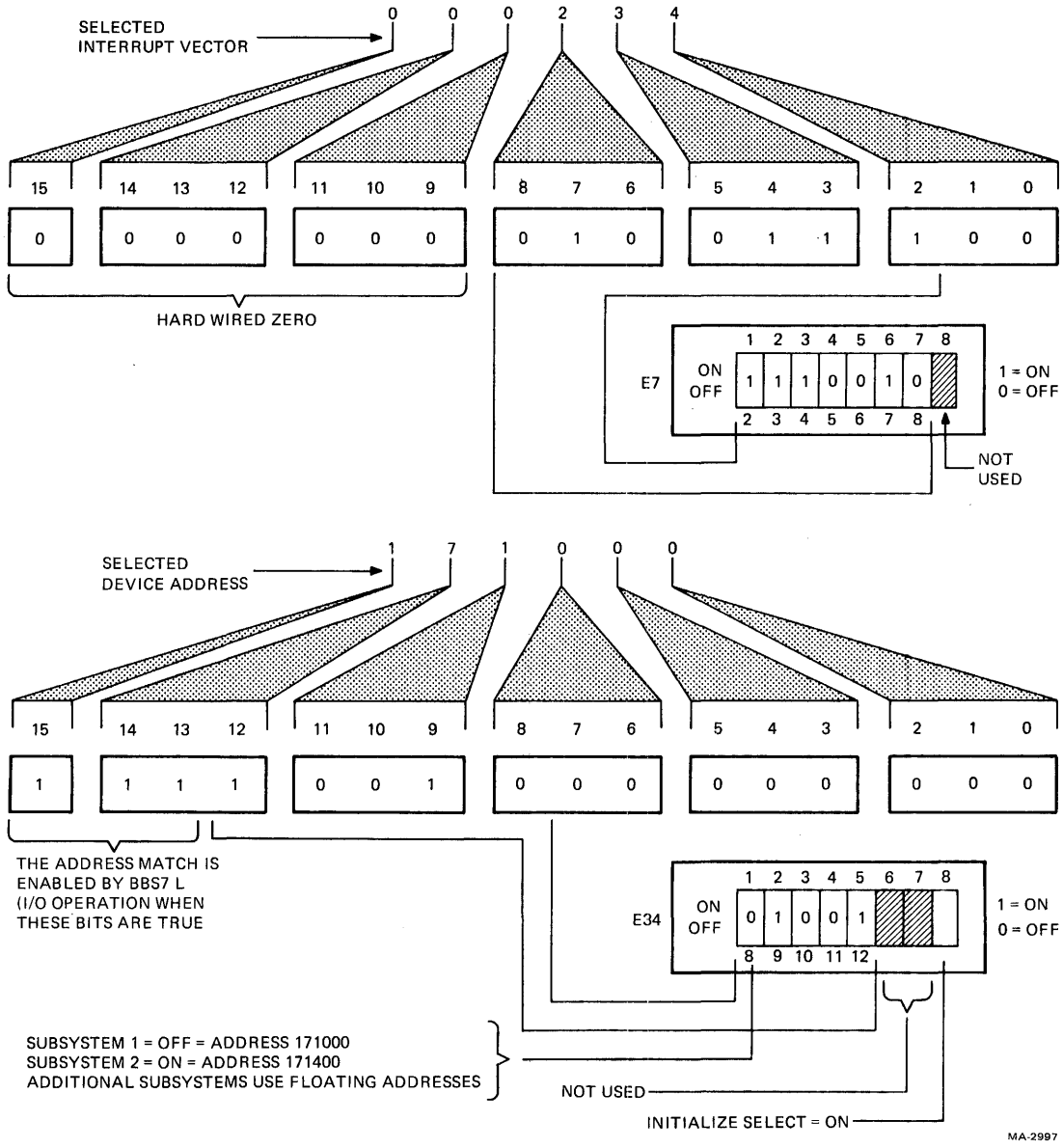


Figure 3-26 M7958 Address and Vector Selectors

3c. The M7959 I/O control module is the bus interface module for IPV1Ø subsystems. It must be configured for its assigned device address and interrupt vector. This is done via switch packs E7 (for address) and E12 (for vector). The location of these switch packs is shown in Figure 3-27. Their use is illustrated in Figure 3-28.

3.5.2 Screw Terminal Configuration

If the BC40A, BC40B, and BC40L screw terminal assemblies are used to connect the I/O modules to the customer field wiring, ensure that the I/O modules are not now connected to the wrong type of screw terminal assembly. This could happen as a result of the customer reorganizing modules in the chassis. The BC40A and BC40L screw terminals are for 16- or 32-bit modules; the BC40B is for 8-bit modules. If necessary, reposition the screw terminal assemblies.

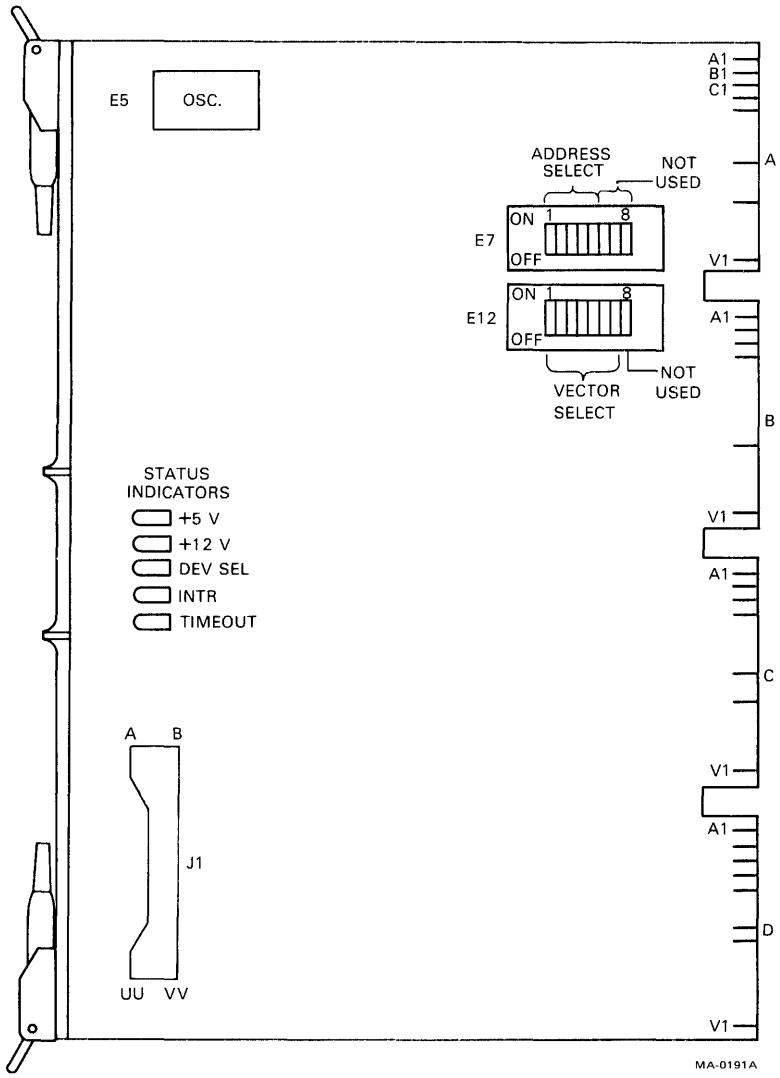


Figure 3-27 M7959 I/O Control Module

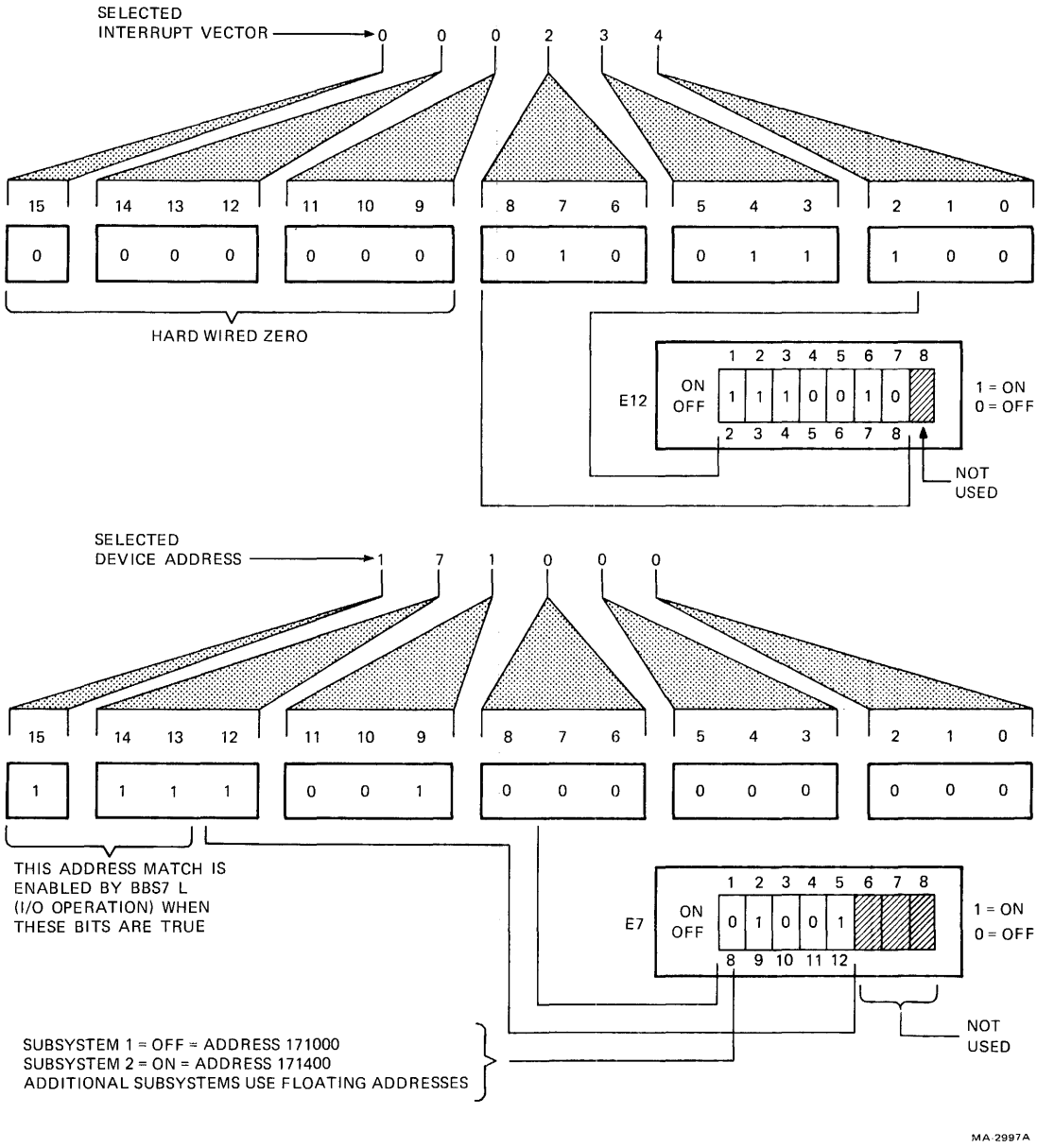


Figure 3-28 M7959 Address and Vector Selectors

3.6 CONFIGURATION RECORDS

The customer should keep a record that describes his I/O Subsystem. Three types of forms for simplifying this task are included in Appendix C. Sample copies of the forms are included in Figures 3-29 through 3-31.

The H333 module chart (Figure 3-29) allows the customer to record a complete map of the chassis, including the I/O modules, the IOCM, and any LSI option modules present. The page number column is a cross reference to the functional I/O module page containing more detailed information about the individual modules. This chart should be attached to the inside chassis front door.

The H334 module chart (Figure 3-30) fulfills a similar function for each H334 chassis present. One of these forms should be filled out for each chassis and attached to the inside chassis front door.

CUT ALONG DOTTED LINE

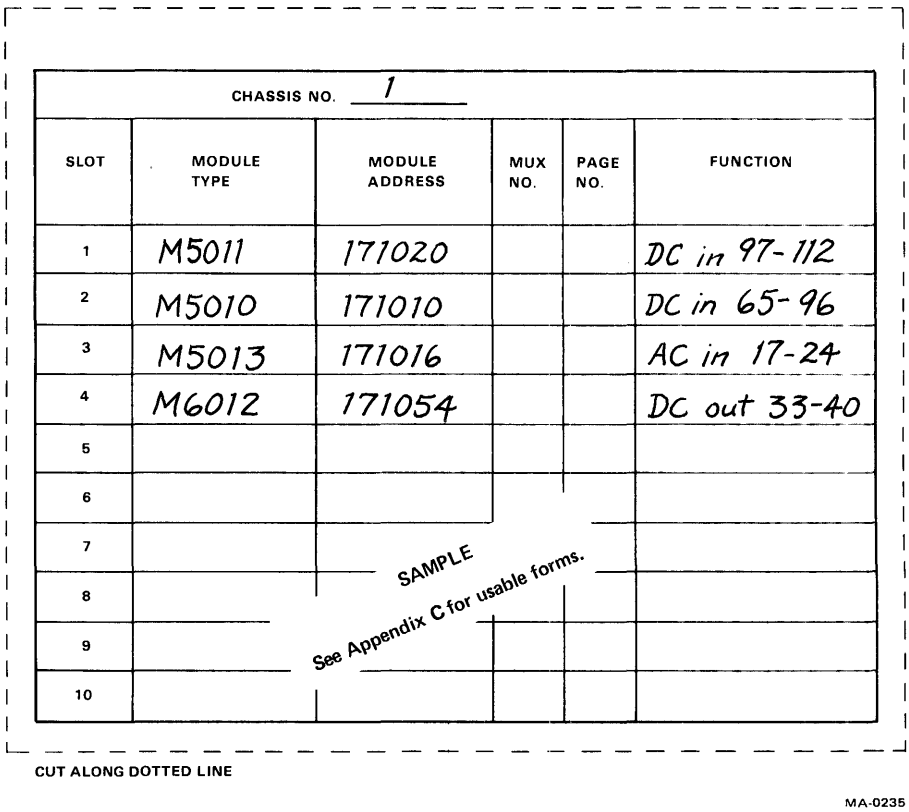
CHASSIS NO. 0

SLOT	LSI-11 BUS	D-BUS	MODULE TYPE	MODULE ADDRESS	MUX NO	PAGE NO	FUNCTION
1	X		KD11-H				Processor
2	X		MSV11-DD	000000-157777			Memory
	X		RXV11				Disk
3	X		DLV11-F				Terminal
	X		G7272				Continuity
4	X		G7272				Continuity
	X		G7272				Continuity
5	X	X	M7958	171000			
6		X	M5010			7	DC in 1-32
		X	M5010			8	DC in 33-64
8		X	M5013			9	AC in 1-8
9		X	M5013			10	AC in 9-16
10		X	M6013			11	AC out 1-8
11		X	M6013			12	AC out 9-16
12		X	M6010			13	DC out 1-32
13		X	M6011			14	DC out 41-56
14	X		REV11-A				Boot/Term

SAMPLE See Appendix C for usable forms.

MA-0234

Figure 3-29 H333 Module Chart



CHASSIS NO. 1

SLOT	MODULE TYPE	MODULE ADDRESS	MUX NO.	PAGE NO.	FUNCTION
1	M5011	171020			DC in 97-112
2	M5010	171010			DC in 65-96
3	M5013	171016			AC in 17-24
4	M6012	171054			DC out 33-40
5					
6					
7					
8					
9					
10					

Figure 3-30 H334 Module Chart

The functional I/O module chart (Figure 3-31) enables the customer to record all pertinent information about a particular module, such as type, generic code, addresses, bit use, interrupt options, etc. After completing the form it should be assigned a page number and put into a notebook. The page number should be recorded on the chassis module chart as a cross reference. The customer should duplicate this chart if site requirements exceed the number supplied in Appendix C.

3.7 SYSTEM RESTRICTIONS

To ensure proper operation, the following I/O Subsystem limitations should be observed.

1. D-bus cables must not exceed 15 m (50 ft) total length.

2. Vacant slots between I/O modules must have M9019 continuity modules plugged into the C and D connectors of those slots.

3. The I/O Subsystem is subject to the software restrictions stated in Chapter 4.

4. The M7958 must be the last option on the LSI-11 bus.

5. The M7958 can only be used in the H333 chassis and only in slot 5 or 6.

6. The M7959 does not implement the LSI-11/23 multiple priority interrupt protocol. Any LSI-11 options that require this protocol must be placed closer to the LSI-11/23 processor than the M7959.

TEAR OUT AND PUNCH FOR EQUIPMENT LOG BOOK

PAGE NO. 8

MODULE TYPE M5010 BYTE 1 OF 4

GENERIC CODE 141

BYTE ADDRESS 004 SINGLE SHOT TIMING N/A

MUX NO. N/A

MODULE LOCATION: CHASSIS NO. 0 FIELD POWER: COMMON ☑ AC ☐

SLOT NO. 7 ISOLATED ☐ DC ☑

POINT	INTR. ENAB.	BIT FUNCTION REMARKS
00	N/A	Low pressure boiler #1
01	↑	High pressure boiler #1
02		Over temp. boiler #1
03		Turbine #2 speed O.K.
04		Low fuel main tank
05		Aux. fuel ON
06	↓	Spare
07	N/A	Control room door unlocked

SAMPLE

See Appendix C for usable forms.

ADDITIONAL COMMENTS:

1. Boiler #1 pressure also on analog channel 73.
2. On low fuel call 555-2368 for delivery.

MA-3271

Figure 3-31 Functional I/O Module Chart

3.8 FIELD WIRING

Proper field wiring practices ensure minimum interference from outside sources. The techniques and restrictions discussed in this section will help to reduce outside interference.

3.8.1 General Wire and Cable Characteristics

In general, field wiring should utilize stranded, tinned-copper wire to ensure flexibility and high oxidation resistance. The dielectric strength of the conductor insulation should be 600 V or greater. Twisted pairs should be utilized throughout to minimize noise pickup and crosstalk. Typical wire sizes that might be used for field wiring are listed below, along with the resistance exhibited by each.

AWG Number	Resistance (Ohms) (per 1000 ft)
14	2.5
16	4.0
18	6.4
20	10.2

Twisted pairs may be arranged concentrically to form cables. All lays and pairs should be twisted in the same direction for greatest flexibility. Cables should be encased in Polyvinyl Chloride (PVC), polyethylene or Teflon™ insulation at least 0.034 inches thick (Teflon should be used if the ambient temperature will exceed 105° C).

3.8.2 Analog Signal Wiring

Uniform twisting and a high turns/foot ratio are desirable for analog signal wiring. Twisted pairs should be bundled together only if all signals have similar amplitude and frequency characteristics. Wire resistance must be considered as part of the load for current-output analog signal wires.

NOTE

Analog wiring and digital wiring should not be run together and should not be run near ac wiring.

3.8.3 Digital Signal Wiring

Multiple input signal wires can be twisted together with a single ground wire in the same cable. The number of signals cabled in this manner should be limited to the number of input points on a given I/O module. Input and output signal wires can be mixed in the same cable tray, but high level output wires should not be placed in the same cable with input wires. Interrupt type input wires should be run as twisted pairs only.

™Teflon is a registered trademark of E. I. DuPont.

3.8.4 Grounding

Ideally, all grounds should be separated into categories: power grounds, logic grounds, and analog grounds. Each ground category should be run directly to a ground electrode and tied to it at one point only. As a practical matter, this may not be feasible, but at the very least, a division should be made between analog and digital grounds.

3.8.5 Installing Field Wiring

The customer's devices may be connected to I/O Subsystem modules by fastening the field wiring to the optional screw terminals or by connecting it directly to his own 50-pin Berg type connector which is plugged directly into the I/O module. When selecting this connector, ensure that it does not have exposed wiring on the surface that comes into contact with the module. This could result in short circuits on the printed circuit etch (Figure 3-32). To ensure that proper practices are followed when installing field wiring, the user should review the field wiring information contained in Paragraphs 3.8 through 3.8.4 before proceeding with the following installation.

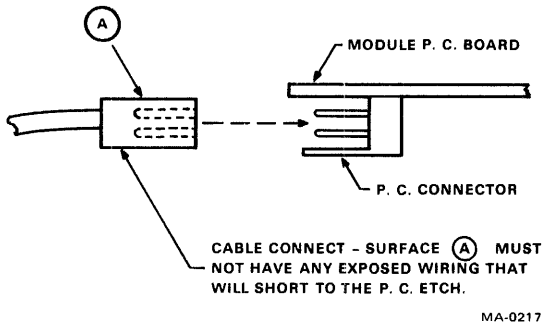


Figure 3-32 I/O Cable Connector Interface

1. Bring the field wiring through the bottom of the H960 cabinet.
2. Guide the wiring along the channel formed by the cabinet vertical supports and clamp it securely into place.
3. Fasten the field wiring to the screw terminals. Ensure that the wiring configuration for each is correct for the I/O module being interfaced. Screw terminal configurations for the most common digital I/O modules are shown in Tables 3-2 and 3-3; others are included with the module descriptions in Chapter 6. Knowing the type module being used in a particular slot enables the customer to select the correct configuration. Module numbers are listed at the top of the column corresponding to its required wiring configuration. Before connecting the field wire, ensure that the proper type screw terminal has been installed for each I/O module as described in Paragraph 3.3.3.3.

Table 3-2 Type A Screw Terminal 16/32-Bit (BC40A) I/O Module Field Termination Configurations

M5010/M6010/M6010-YA		M5011/M6011		M5012/M5012-YA/M5031		
Field Bit No.	Screw Terminal No.	Field Bit No.	Screw Terminal No.	Field Bit No.		Screw Terminal No.
00	1	00	1	00	+	1
01	2	01	2		-	2
02	3	02	3	01	+	3
03	4	03	4		-	4
04	5	04	5	02	+	5
05	6	05	6		-	6
06	7	06	7	03	+	7
07	8	07	8		-	8
10	9	10	9	04	+	9
11	10	11	10		-	10
12	11	12	11	05	+	11
13	12	13	12		-	12
14	13	14	13	06	+	13
15	14	15	14		-	14
16	15	16	15	07	+	15
17	16	17	16		-	16
Field	17	Field	17	Not		17
Common	18	Common	18	Used		18
20	19	Not Used	19	10	+	19
21	20		20		-	20
22	21		21	11	+	21
23	22		22		-	22
24	23		23	12	+	23
25	24		24		-	24
26	25		25	13	+	25
27	26		26		-	26
30	27		27	14	+	27
31	28		28		-	28
32	29		29	15	+	29
33	30		30		-	30
34	31		31	16	+	31
35	32		32		-	32
36	33		33	17	+	33
37	34	Not Used	34		-	34

NOTE
Two 8-position jumper strips are provided with the BC40A. These can be used to common the + or - terminals for the M5012 module on a per-byte basis. They can also be used with the M5012-YA to common the + terminals for connection to a user-furnished +5 V TTL supply.

Table 3-3 Type B Screw Terminal 8-Bit (BC40B)
I/O Module Field Termination Configurations

M6012		M5013/M6013	
Field Bit No.	Screw Terminal No.	Field Bit No.	Screw Terminal No.
00 FIELD +	1	00 LINE	1
00 SWITCH	2	00 SWITCH	2
00 FIELD -	3	00 NEUT	3
01 FIELD +	4	01 LINE	4
01 SWITCH	5	01 SWITCH	5
01 FIELD -	6	01 NEUT	6
02 FIELD +	7	02 LINE	7
02 SWITCH	8	02 SWITCH	8
02 FIELD -	9	02 NEUT	9
03 FIELD +	10	03 LINE	10
03 SWITCH	11	03 SWITCH	11
03 FIELD -	12	03 NEUT	12
Not used	13	Not used	13
	14		14
	15		15
	16		16
	17		17
	18		18
	19		19
	20		20
	21		21
	22		22
04 FIELD +	23	04 LINE	23
04 SWITCH	24	04 SWITCH	24
04 FIELD -	25	04 NEUT	25
05 FIELD +	26	05 LINE	26
05 SWITCH	27	05 SWITCH	27
05 FIELD -	28	05 NEUT	28
06 FIELD +	29	06 LINE	29
06 SWITCH	30	06 SWITCH	30
06 FIELD -	31	06 NEUT	31
07 FIELD +	32	07 LINE	32
07 SWITCH	33	07 SWITCH	33
07 FIELD -	34	07 NEUT	34

NOTES:
1. M6012 - All "Field +" terminals are common. All "Field -" terminals are common.

2. M5013/M6013 - All "Line" terminals are common. All "Neutral" terminals are common.

3.9 INSTALLATION OF PROCESSOR INTERFACE

The I/O subsystem can interface with either the LSI-11 bus or the PDP-11 UNIBUS. Four interface configurations are possible.

1. IP300 - LSI-11 bus interface
2. IP110 - UNIBUS interface
3. IP11 - UNIBUS interface
4. IPV10 - LSI-11 bus interface

The procedure for implementing each of these interfaces is given below. The user should disregard the three procedures not relevant to his system.

3.9.1 LSI-11 Based Subsystem Installation (IP300)

To configure the IP300, plug the LSI-11 modules into the first four and the fourteenth slots of the H333 chassis, (Figure 3-33). The standard configuration includes the following modules.

1	KD11-H	Processor quad-height
1	MSV11-DD	Memory dual-height
1	RXV11	Floppy disk control unit dual-height
1	DLV11-F	Serial line unit dual-height
1	REV11-A	Boot/terminator dual-height

The user is advised that any LSI-11 configuration different than the above is subject to the restrictions of the LSI-11 bus as covered in the LSI-11 User Manual. In addition, the I/O Subsystem imposes the following LSI-11 restrictions.

1. LSI-11 options are restricted to the first five and the fourteenth slots of the master chassis.

2. A vacant slot between LSI-11 modules must have G7272 continuity modules plugged into the A and C connectors of that slot.

3. Memory refresh must be performed by the MSV11-DD memory, not by the REV11-A or the processor.

3.9.2 UNIBUS IOCM Based Subsystem Installation (IP110)

The M8719 UNIBUS IOCM goes into the C, D, E, and F sections of any SPC slot in a PDP-11 backplane. When configuring a system, remember that the interrupt priority depends on the priority plug number (Figure 3-23) and the proximity to the processor on the UNIBUS. It is recommended that the M8719 be set at priority six (priority plug no. 54-08780-00), and located further from the CPU than any mass storage interfaces so that the relatively long I/O subsystem cycle time does not interfere with the mass memory, causing data late errors to occur. The M8719 is shipped from the factory with a priority level six plug.

To configure an IP110, plug one end of the BC08R D-bus cable (provided) into the D-bus input connector of H334 chassis number one (Figure 3-33). Plug the other end into J1 of the M8719 at the UNIBUS.

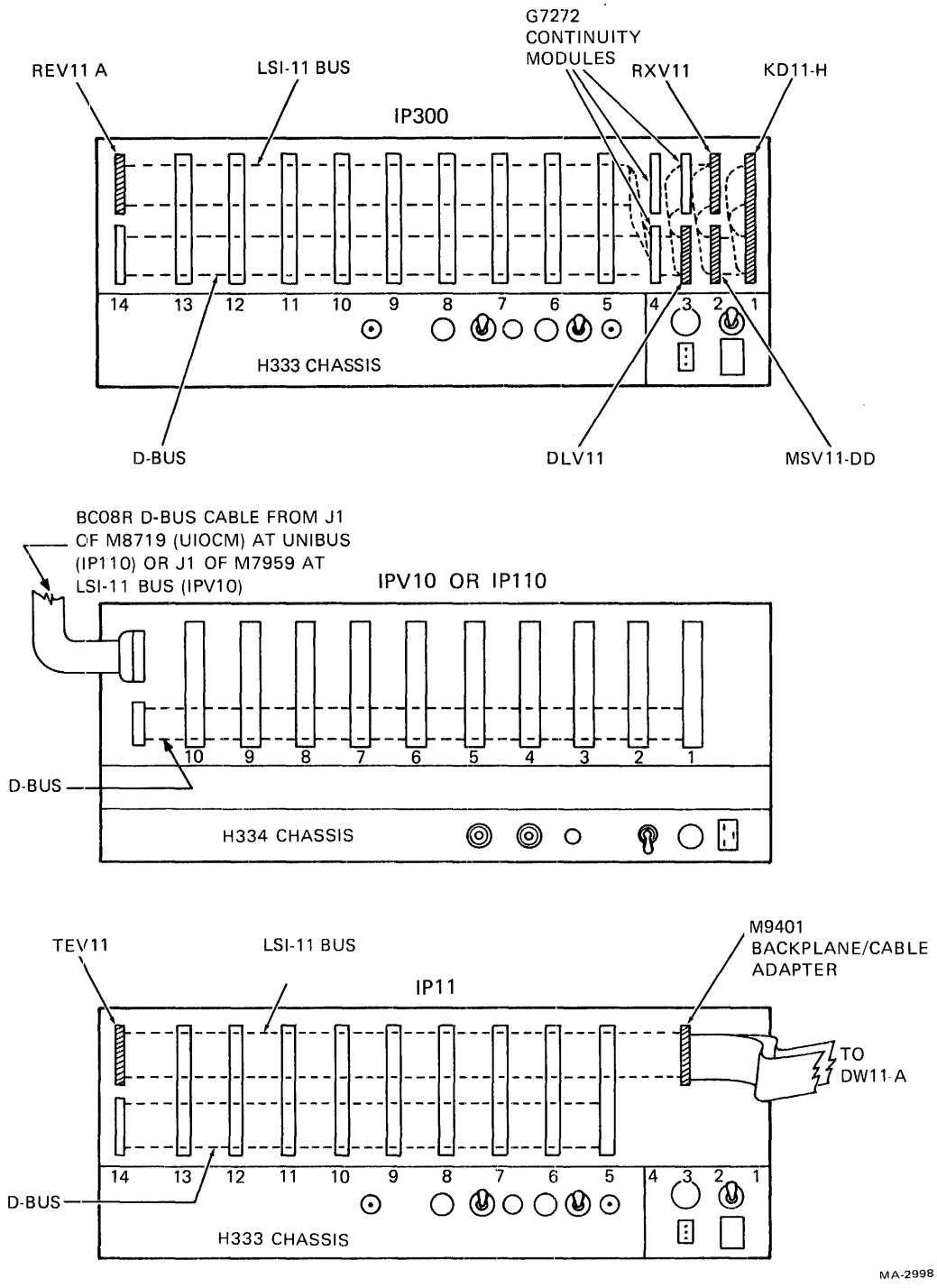


Figure 3-33 Processor Interface Configurations

3.9.3 UNIBUS to LSI-11 Bus Converter Based Subsystem Installation (IP11)

For an IP11 subsystem, install the DW11-A bus converter module in the UNIBUS. This unit must mount in the C, D, E, and F sections of an SPC slot. For further information about this module, refer to the DW11-A UNIBUS in the LSI-11 Bus Converter User Manual (EK-DW11A-IN).

Next, install the M9401 backplane to cable adapter module and the TEV11 terminator module in the locations shown in Figure 3-33. Finally, install the LSI-11 bus cable by plugging one end of each cable into the DW11-A at the UNIBUS and the other ends into the cable adapter module.

3.9.4 LSI-11 Based Subsystem (IPV10)

To configure an IPV10 subsystem, install the M7959 IOCM in an empty quad slot of an LSI-11 computer (e.g., a PDP-11/03 or PDP-11/23), plug one end of the BC08R D-bus cable (provided) into J1 of the M7959, and plug the other end into the D-bus input connector of H334 chassis number one (Figure 3-33).

4.1 SCOPE

This chapter contains general programming information for I/O Subsystems. The following topics are discussed.

4.2 Device Registers and Address Assignments
4.3 I/O Transfers
4.4 Device Priorities
4.5 Programming Requirements
4.6 Sample Programs

More detailed information on programming in general may be found by referring to the appropriate processor handbook.

4.2 DEVICE REGISTERS AND ADDRESS ASSIGNMENTS

The programmer is concerned with only three types of registers for the I/O Subsystem:

one CSR (control and status register),

one IAR (interrupting address register),

and as many IORs (input output register) as the particular subsystem may require, up to a maximum of 254.

There can be a total of 256 registers for the subsystem, each assigned a unique address in the processor's address space.

4.2.1 Address Assignments

4.2.1.1 Subsystem Addresses - The I/O Subsystem address range can be 171000 to 171377 or 171400 to 171777 depending on whether there are one or two subsystems. Additional subsystems would use floating addresses. Subsystem address selection is made on the I/O control module as explained in Chapter 3. The remainder of this chapter refers to addresses as if the subsystem address was 171000.

4.2.1.2 I/O Addressing Rules - Each subsystem is assigned 400 octal addresses in the processor's address space for I/O use. These addresses are selected by switches on the individual I/O modules and range from 171000 through 171377. A typical mapping of address assignments is shown in Figure 4-1. When assigning these addresses to specific I/O modules, the following rules must be adhered to.

1. Address bytes 171376 and 171377 are reserved for the IAR and CSR, respectively.

2. A single byte module may be assigned any byte address except those reserved for the IAR and the CSR.

3. A two byte module must be assigned two consecutive address bytes beginning with an even address.

4. A four byte module must be assigned four consecutive bytes beginning with an address that ends in zero or four.

5. The rules for assigning addresses to modules with more than four bytes are consistent with the above rules.

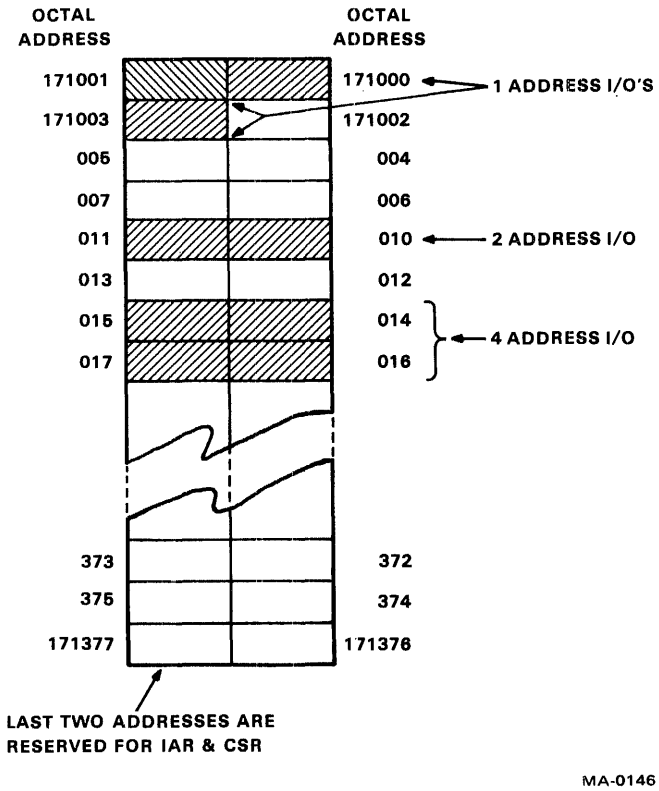


Figure 4-1 Typical Address Assignments

4.2.1.3 Interrupt Vector Addresses - The first I/O Subsystem will vector through memory locations 000234 and 000236. Additional subsystems will use floating vectors (refer to Appendix B).

4.2.2 Register Formats

Figures 4-2 through 4-4 show the register formats and Table 4-1 describes the functions of the CSR bits in detail.

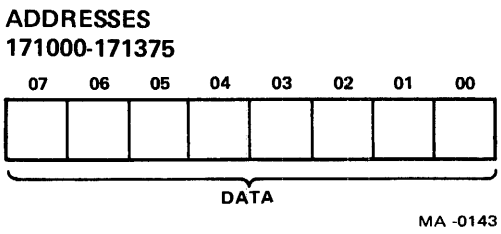


Figure 4-2 IOR Format

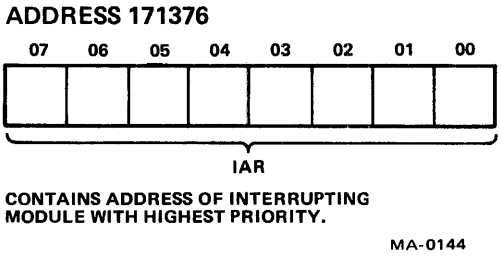


Figure 4-3 IAR Format

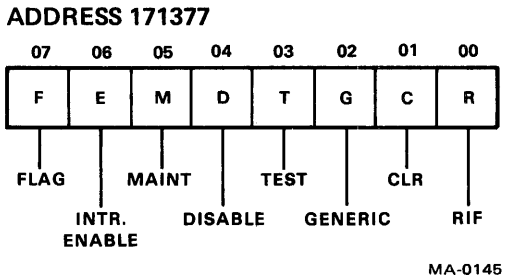


Figure 4-4 CSR Format

Table 4-1 CSR Bit Descriptions

Bit	Description
Ø7 (F) Read only	Flag bit=1 indicates that the subsystem requires service.
Ø6 (E) Read/write	Enable bit=1 enables the subsystem interrupt. If F=1 and E=1 and the processor status allows interrupts, the processor will be interrupted.
Ø5 (M) Read/write	Maintenance bit=1 forces a maintenance interrupt if E=1. If M=1, then F=1. M is cleared when the CSR has been read with R=1. Reading an IOR with M=1 results in data equal to the address of that IOR, whether or not there is a module installed with that address.
Ø4 (D) Read/write	Disable bit=1 sets the I/O disable mode on all applicable I/O modules. Clearing the D-bit automatically sets the C-bit.
Ø3 (T) Read/write	Test bit=1 sets the I/O test mode on all applicable I/O modules.
Ø2 (G) Read/write	Generic bit=1 causes an I/O module to respond with its identity code instead of normal data.
Ø1 (C) Write only	Clear bit=1 causes the subsystem to reset without requiring a reset instruction; self-clearing.
ØØ (R) Read/write	RIF (reset interrupt flag) bit=1 causes the I/O module being read to reset its internal interrupt flag. RIF is cleared when the I/O module or the CSR is addressed.

4.2.2.1 IOR - The I/O registers (IOR) are 8-bit registers that may contain field, address, status, or test information, to or from an I/O module, depending on the type of I/O module involved in the transaction. For a more detailed discussion, consult the specific I/O module descriptions in Chapter 6.

4.2.2.2 IAR - The interrupting address register (IAR) contains the address of the interrupting I/O module with the highest priority. The IAR is an 8-bit register at byte address 171376. If the IAR is read when there is no interrupting I/O module, the processor will trap through address ØØØØØ4. Therefore, the IAR should be read only after an interrupt.

4.2.2.3 CSR - The control status register (CSR) is an 8-bit read-write register that monitors the status and controls the operation of the subsystem. It is located in the last byte address in the subsystem's address space. The function of each bit is explained in Table 4-1. The CSR occupies address 171377.

4.3 I/O TRANSFERS

The I/O Subsystem operates by programmed I/O transfers and interrupt-driven transfers. In a typical application, there might be a programmed status monitoring mode and also an asynchronous mode in which the controlled system interrupts the processor for immediate service.

4.3.1 Programmed I/O Transfers

Programmed I/O transfers may be used to input or output 8-bit data or status bytes to or from the I/O modules. By including the device's address as the effective source or destination address, the user selects the input or output operation.

4.3.2 Interrupt I/O Transfers

Some of the input modules on the I/O Subsystem D-bus may initiate an interrupt type transfer by causing the subsystem to interrupt the processor. The module does this when its internal Flag bit is set. If priority conditions allow, the processor suspends operation of its present (background) program to service the subsystem. The subsystem has a hard-wired vector associated with it that it outputs to the processor. This vector is an address pointer, which allows automatic entry into the I/O Subsystem's service routine stored in the processor's memory. Part of this service routine must include instructions to reset the module's interrupt Flag bit. This is known as RIFing the module and is done by reading the module with the RIF bit in the CSR set.

4.4 DEVICE PRIORITIES

4.4.1 I/O Subsystem Priorities

Since the I/O Subsystem is an LSI-11 bus device, it is subject to priority rules on that bus. That is, the device electrically closest to the processor has the highest priority. In addition to bus priority, there is also the processor priority arbitration to consider. As explained in Chapter 1, the subsystem may be connected to a PDP-11 so the arbitration is not necessarily that of the LSI-11. The reader is referred to the appropriate processor handbook for details of its priority arbitration. When used with the UNIBUS PDP-11, the subsystem typically interrupts at priority level 6.

4.4.2 I/O Priority

When the I/O Subsystem has acquired control of the LSI-11 bus, one of its I/O modules on the D-bus is serviced. The interrupt control line is daisy-chained along the D-bus, creating a priority structure within the I/O Subsystem such that the I/O module electrically closest to the subsystem's I/O control module has the highest priority. This module will be serviced and its address will be in the IAR (interrupting address register). The IAR contains the address of the highest priority module with an interrupt pending. There is no inherent relationship between the

address of an I/O module and its physical proximity to the I/O control module. Therefore, it is possible to establish the subsystem interrupt priority without regard to the modules' addresses. Note, however, that the maintenance interrupt is always the highest priority interrupt.

4.5 CONFIGURATION REQUIREMENTS

4.5.1 Subsystem Requirements

At installation time, the subsystem must have its address and vector switches (on the I/O control module) set to the proper octal addresses as discussed in Paragraph 4.2 and in Chapter 3, Paragraph 3.5.1. This must be done before the system can be operated.

4.5.2 I/O Requirements

All I/O modules have one or more switches which must be set to select specific addresses, interrupt flags, or operating modes. Proper switch settings may be found by referring to the specific I/O modules in Chapter 6. It is first necessary to determine which modules should have the highest priority for interrupts so locations for plugging the modules into the D-bus can be assigned. The highest D-bus priority is obtained by the I/O module electrically closest to the I/O control module; the module furthest away has the lowest priority.

4.5.3 Trap Conditions

The following conditions cause the processor to trap through location 000004.

1. Attempting to write the IAR
2. Attempting to read the IAR when there is no interrupting module
3. Attempting to read a nonexistent I/O module address when M=0

In addition, some PDP-11s trap through location 000004 if an attempt is made to read or write a word with an odd address.

4.5.4 Software Restrictions

The following restrictions are effective for programs operating the I/O Subsystem.

1. At least 20 microseconds must elapse between setting the C-bit (bit 1) of the CSR and next addressing the subsystem.
2. The time from setting the subsystem interrupt (Flag bit) to the time the interrupt service routine reads the IAR must be at least 30 microseconds.

3. The time from clearing a module interrupt (RIFing the module) to the time the software enables additional subsystem interrupts, tests the F-bit of the CSR, or reads the IAR, must be at least 30 microseconds.

4. At least 200 ms must elapse after initial system power up before any I/O module is accessed by the software.

Sample Program Number 1
This is a general interrupt routine that:

1. Acquires the address of the interrupting module
2. RIFs the module
3. Performs the required service
4. Checks for further interrupts
5. Returns to the main program.

```
VECTOR:234

R0=%0

IAR:171376

CSR:171377

                MOV   #START,@VECTOR    ;SET INTERRUPT ROUTINE
                                        ;ADDRESS

                MOV   #340,@VECTOR+2    ;SET CPU PRIORITY TO 7 SO
                                        ;THAT SAME MODULE WILL
                                        ;NOT INTERRUPT AGAIN

                MPTS  #0                ;ENABLE CPU INTERRUPT

                BISB  #100,@CSR         ;ENABLE I/O SUBSYSTEM
                                        ;INTERRUPT

                WAIT                    ;WAIT FOR INTERRUPT

START:          MOVB  @IAR,R0           ;GET CONTENTS OF IAR -
                                        ;LOW BYTE OF INTERRUPTING
                                        ;MODULE'S ADDRESS
1
                BIC   #177400,R0        ;CLEAR THE HIGH BYTE OF R0

                ADD   #171000,R0        ;ADD IAR HIGH BYTE - R0 NOW
                                        ;CONTAINS COMPLETE ADDRESS
                                        ;OF INTERRUPTING MODULE
```

```
2                BISB #1,@CSR          ;SET RIF BIT
                 TSTB @RØ              ;READ MODULE - READING
                                       ;MODULE WITH RIF BIT SET
                                       ;WILL RIF THE MODULE

                 OTHER WORK
                 TEST GENERIC CODE
3                READ MODULE           ;PERFORM INTERRUPT SERVICE
                 PROCESS, ETC.

                 TSTB @CSR             ;GET CONTENTS OF CSR
4
                 BMI  START            ;IF F=1 SERVICE NEXT
                                       ;INTERRUPT

5                RTI                   ;RETURN FROM INTERRUPT
```

Sample Program Number 2
This program takes the contents of RØ, outputs it to an output module, and then reads and prints the contents of that module's output register. Subroutine PRINT will print the contents of R1.

```
  RØ=%Ø

  R1=%1

  ADOUT:   171XXX

  START:        MOV B   RØ,@ADOUT   ;PUT CONTENTS OF RØ IN OUTPUT
                                    ;REGISTER
                MOV B   @ADOUT,R1   ;PUT CONTENTS OF OUTPUT REGISTER
                                    ;IN R1
                BIC     #177400,R1  ;CLEAR HIGH BYTE OF R1

                JSR     PC,PRINT    ;PRINT THE CONTENTS OF R1
```

Sample Program Number 3
This subroutine monitors the contents of an input register and when its contents exceeds five clears an output register. The calling instruction is: JSR RØ,START

```
  RØ=%Ø

  ADIN:171304

  ADOUT:171305

  START:        MOV    #5,RØ        ;SET CONTENTS OF RØ=5

  FIRST:        CMPB   @ADIN,RØ     ;COMPARE INPUT TO QUANTITY 5

                BGT    FINAL        ;IF CONTENTS OF INPUT REG>5
                                    ;CLEAR OUTPUT REG

                BR     FIRST        ;IF NOT>5 COMPARE AGAIN
```

```
FINAL:      CLRB   @ADOUT     ;CLEAR OUTPUT REG
            RTS    RØ         ;RETURN TO MAIN PROGRAM
```

CHAPTER 5
PRINCIPLES OF OPERATION

5.1 SCOPE

This chapter provides a functional description of the I/O Subsystem. Overall system operation, and detailed discussions of the control modules are included. The reader should be familiar with the LSI-11 and other PDP-11 processors as well as the introductory material presented in Chapter 1. Detailed descriptions of I/O modules are included in Chapter 6.

5.2 FUNCTIONAL DESCRIPTION

The I/O Subsystem is a program-controlled industrial control subsystem. It is capable of monitoring and controlling complex industrial processes on a real-time basis. To accomplish this, the subsystem performs the following operations.

1. It transfers status information from the I/O addresses to the processor. (This type of transfer is called a DATAI.)

2. It transfers control data from the processor to the I/O addresses. (This type of transfer is called a DATAO.)

3. It generates service requests to the program in response to interrupts from the I/O modules. (These requests are called I/O interrupts.)

In addition to these basic functions, the subsystem is capable of performing various software-initiated maintenance functions for testing its own performance.

5.3 SYSTEM CONFIGURATIONS

The I/O Subsystem comprises a control module and a number of I/O modules that interface with it on a common data bus called the D-bus. A block diagram showing this configuration is shown in Figure 5-1. The number and type of I/O modules is a variable that is a function of the particular application.

There are three types of I/O control modules: M7958 and M7959 for LSI-11 Bus based I/O subsystems, and M8719 for UNIBUS based I/O subsystems. The difference between the three modules is best visualized by examining Figure 5-2, which illustrates an application of each.

Note that the M7958 and M7959 modules perform identical logical functions. The difference between the two is mechanical. The M7958 interfaces with the two buses in an H333 chassis via its printed circuit etched edge connector. The M7959 interfaces with the LSI-11 bus in an LSI-11 computer chassis via its printed circuit etched edge connector and with the D-bus via a cable.

The third I/O control module, the M8719, interfaces with the UNIBUS in a PDP-11 chassis via its printed circuit etched edge connector, and with the D-bus via a cable.

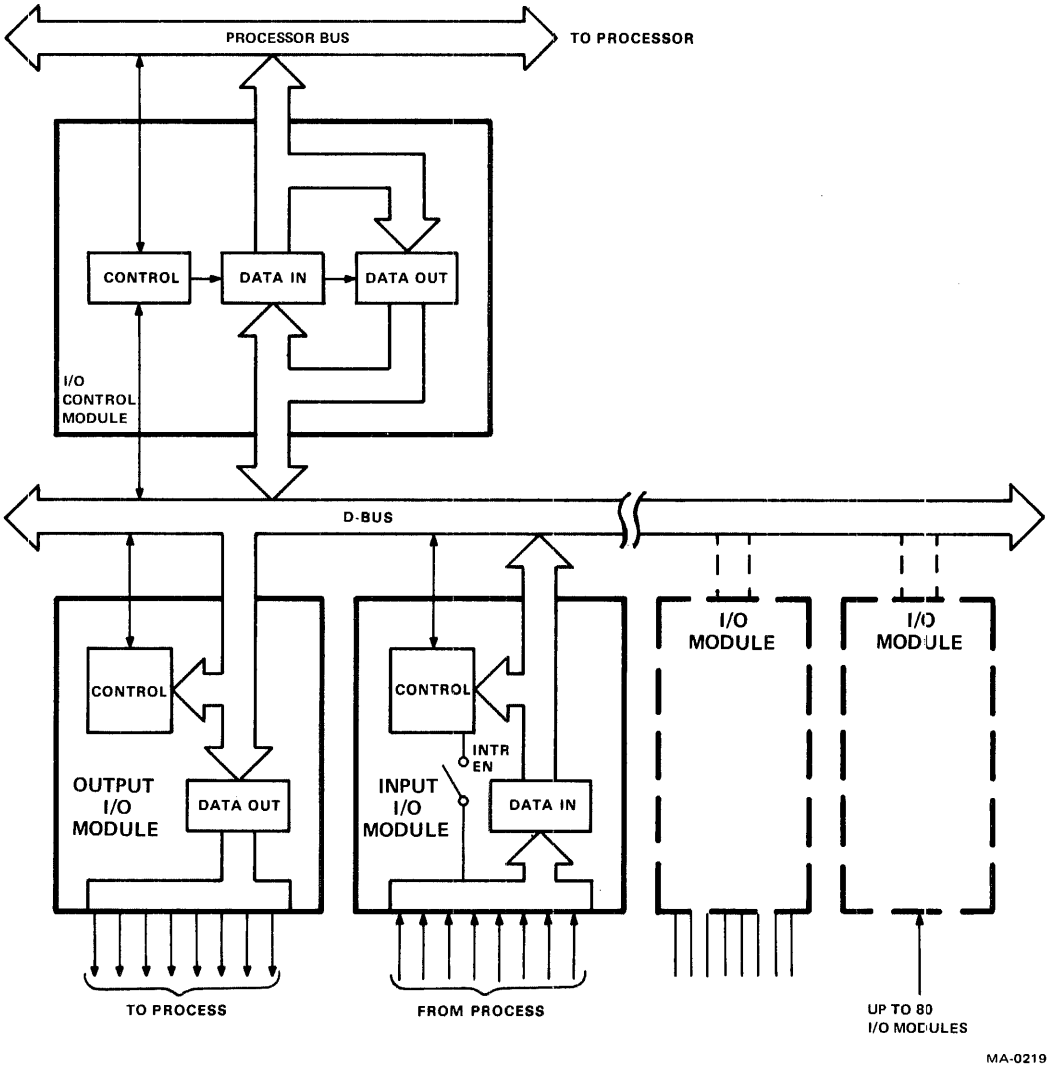


Figure 5-1 I/O Subsystem

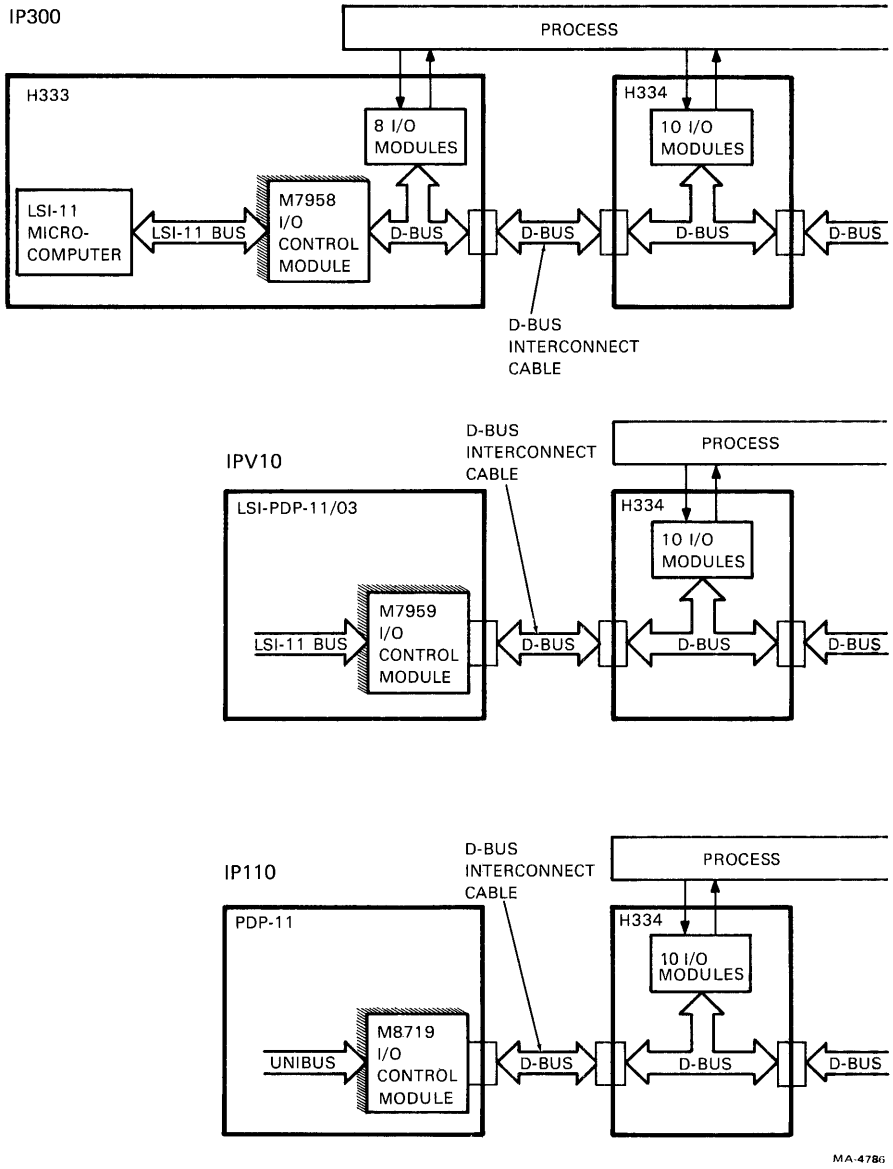


Figure 5-2 IOCM Applications

I/O subsystems using the M7958 I/O control module have space for 78 I/O modules when fully expanded. Up to 8Ø I/O modules are possible in the other two systems.

The following paragraphs contain separate descriptions of LSI-11 bus based and UNIBUS based systems. The reader may omit that description not pertinent to his application.

5.4 LSI-11 BUS BASED SUBSYSTEM

In an LSI-11 based subsystem, either the M7958 or the M7959 is the I/O control module of Figure 5-1. As is shown in the figure, all I/O modules reside on the D-bus, under control of the M7958 or the M7959, and provide inputs from, or outputs to, the process. The control module interfaces with both the D-bus and the LSI-11 bus. The major difference between the two buses is that the LSI-11 bus is 16 bits wide and the D-bus is only 8 bits. The D-bus also has its own unique timing. These differences are provided for by the control module, which derives D-bus timing and data control signals from standard LSI-11 bus signals. The following discussions of data transactions should aid in understanding the operation of the M7958 and M7959 I/O control modules. The reader should note that while the timing and data path of the LSI-11 bus and the D-bus differ, the data transfer protocols are identical.

5.4.1 M7958 and M7959 D-bus Cycles

The timing signals that control the I/O module data transactions on the D-bus constitute the D-bus Cycle. Derivation of a DATAI D-bus Cycle is shown in Figure 5-3. The first three signals at the top of the figure are the normal signals initiated by the processor when executing a DATAI. The remainder of the sequence involves signals internal to the I/O Subsystem. The order of signal sequence is indicated by arrows in the figure. If this timing diagram is related to the block diagrams of Figures 5-4 and 5-5, the functions performed during the sequence can be better visualized. In these figures, data paths are indicated by cross-hatching, and the relevant control signals by bold lines.

The D-bus Cycle breaks down into three parts: SETUP TIME, SYNC TIME, and DATA TIME. The cycle is initiated by the ADRO EN (address out enable) signal which starts the SETUP TIME phase of the cycle. SETUP TIME is defined by a delay which is part of the control circuitry in the IOCM; it allows sufficient time for settling of address data on the D-bus. At the end of this delay, D SYNC (D-bus sync) is asserted, causing the addressed I/O module to activate its internal MY ADDRESS signal. (MY ADDRESS is the signal produced by an I/O module's control circuits when it recognizes its address on the bus; it is the module's data transaction enabling signal.) The second part of the D-bus Cycle (SYNC TIME) is controlled by another delay circuit in the IOCM. This delay allows at least minimum time for the I/O module to prepare to transmit the appropriate data byte.

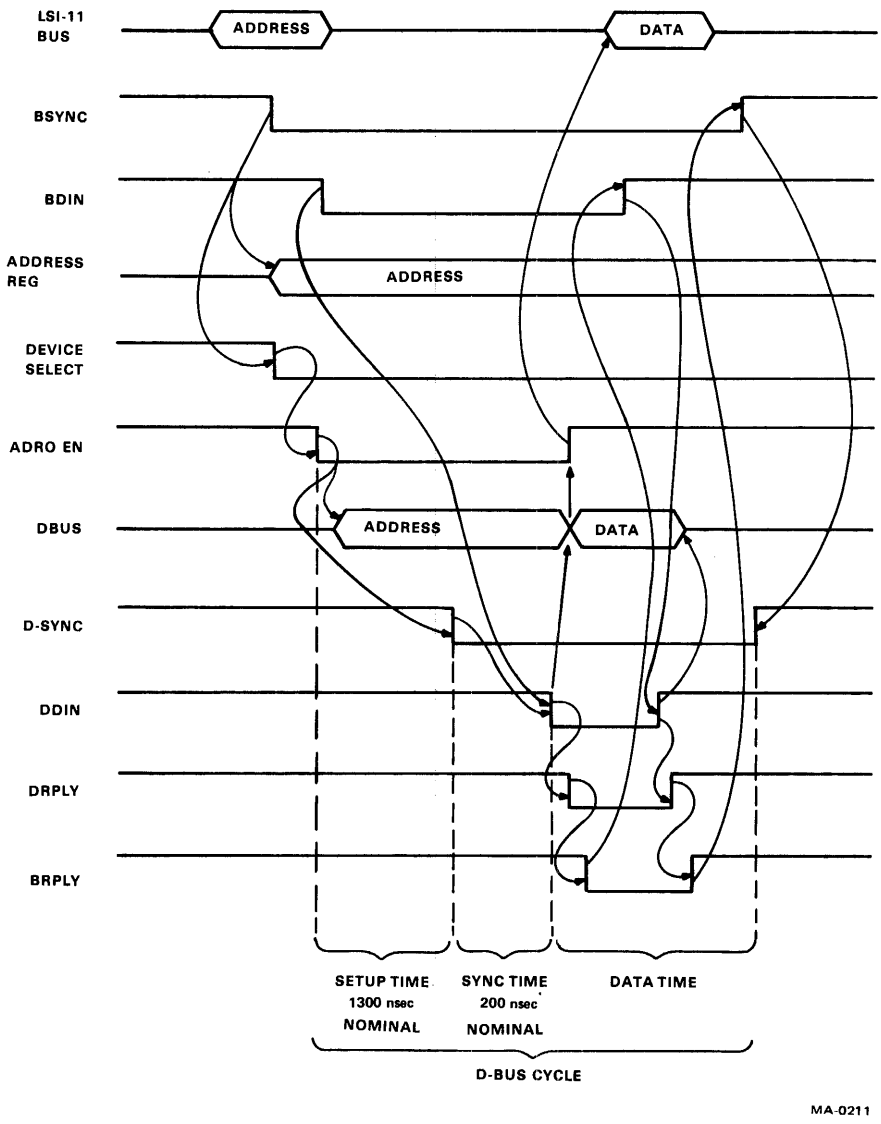


Figure 5-3 DATAI

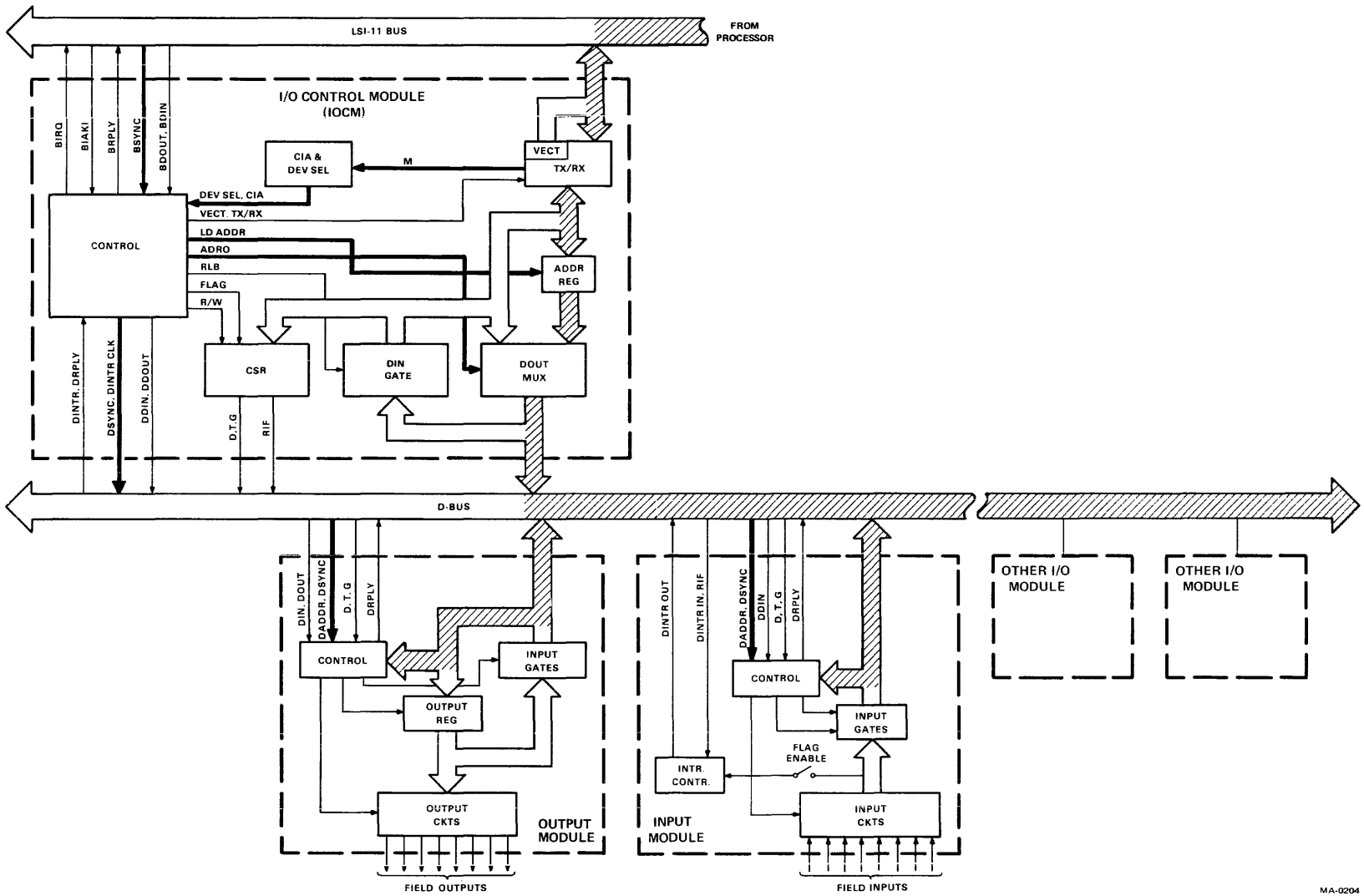


Figure 5-4 Addressing

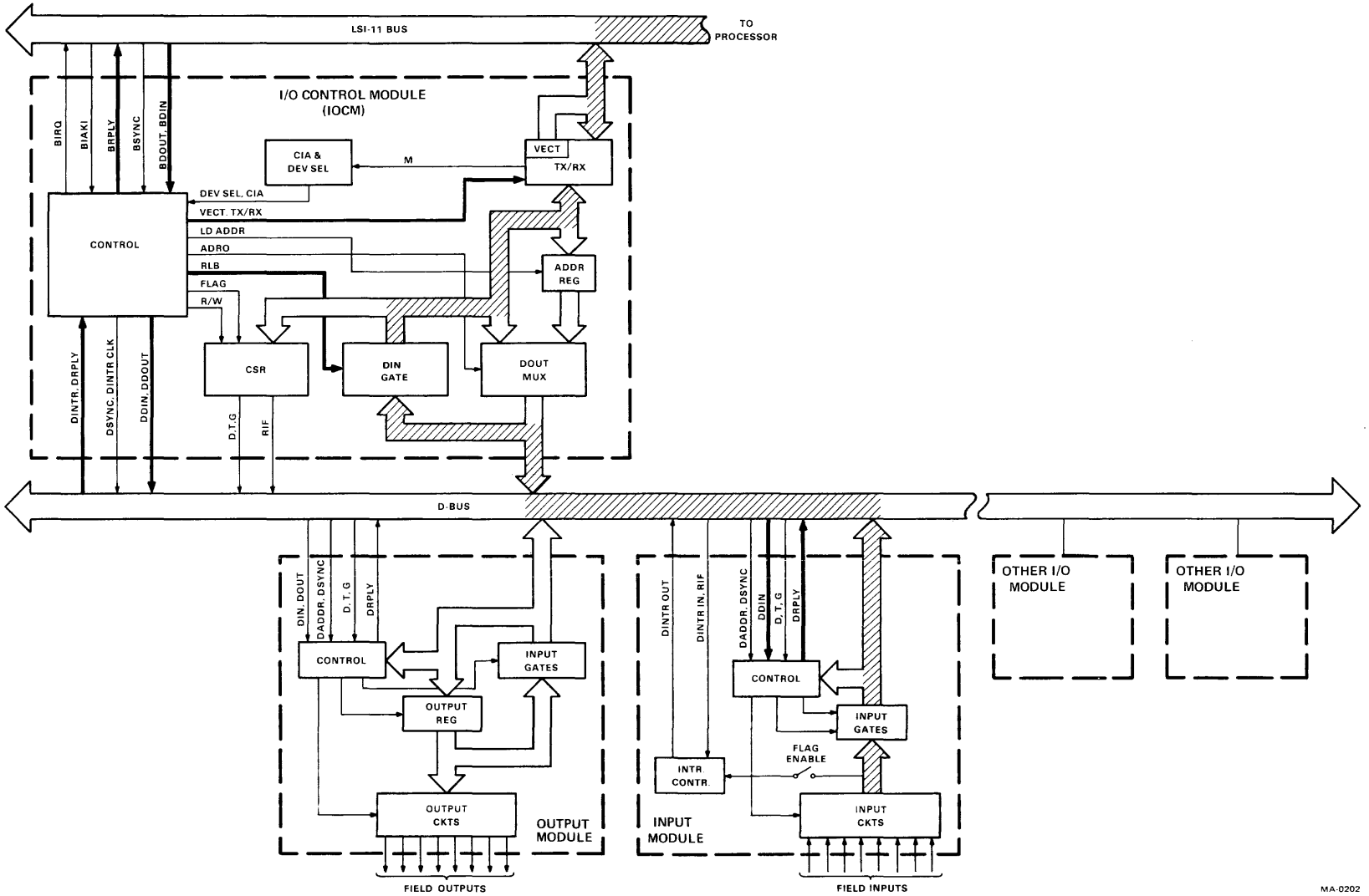


Figure 5-5 Data Input

At the end of this delay, D DIN (D-bus Data In) is asserted telling the selected module to put its data on the D-bus. The module does this and replies by asserting D RPLY. Upon receiving D RPLY, the IOCM puts the D-bus data on the LSI-11 bus, and asserts B RPLY indicating to the processor that it has done so. The processor accepts the data and negates B DIN indicating that the LSI-11 bus cycle is ending. The negation of B DIN causes the IOCM to negate D DIN, which causes the module to negate D RPLY. When the IOCM receives the negation of D RPLY, it negates B RPLY on the LSI-11 bus. The processor then negates B SYNC on the LSI-11 bus freeing the bus for the next processor transaction. The negation of B SYNC causes the IOCM to negate D SYNC, freeing the D-bus for the next I/O transaction.

For a DATAO, the device selection part of the cycle is the same as for a DATAI; however, after B SYNC is asserted, the LSI-11 removes the address from the bus, replacing it with data. The IOCM does the same on the D-bus (Figures 5-6 and 5-7). The LSI-11 waits for the bus data to settle and then asserts B DOUT, telling the IOCM that the data is valid. The IOCM waits because the D-bus is slower than the LSI-11 bus and then asserts D DOUT telling the addressed module to clock in the data. When the module has accepted the data, it asserts D RPLY, which the IOCM transmits to the LSI-11 as B RPLY. The LSI-11 then negates B DOUT, causing the sequential negation of D DOUT, D RPLY, B RPLY, B SYNC, and D SYNC as in a DATAI cycle, and freeing both buses for subsequent transactions.

Some instructions cause the processor to initiate a DATAIO cycle. In this case the D-bus Cycle has four parts: SETUP TIME, SYNC TIME, and two DATA TIMEs for reading and immediately rewriting the same address.

A modified D-bus Cycle occurs when the program reads the subsystem's IAR (interrupting address register). The IAR is read at the beginning of the interrupt routine when the main program is interrupted. (The IAR contains the address of the highest priority interrupting module on the D-bus.) The difference between the modified and ordinary D-bus Cycles is that D SYNC is inhibited in the modified cycle (SYNC TIME) and D ADDR is asserted instead. When D DIN occurs (DATA TIME), the module puts its address instead of data on the D-bus and the program reads the address of the interrupting module at the IAR address. Modified D-bus Cycle timing is shown in Figure 5-8.

5.4.2 M7958 and M7959 Interrupts

Some input modules can interrupt the processor for service if, for example, one of its field inputs changes state. If a change of state occurs, the module's flag flip-flop is set and initiates an interrupt sequence by putting the D INTR signal on the D-bus. This signal is daisy-chained along the D-bus and ORed with any D INTR signals from other modules. The interrupt control line (D INTR INH) is also daisy-chained along the D-bus. It ensures that if there is more than one module with an interrupt pending, the one that is serviced first is the one with the highest priority (the module physically closest to the IOCM on the D-bus).

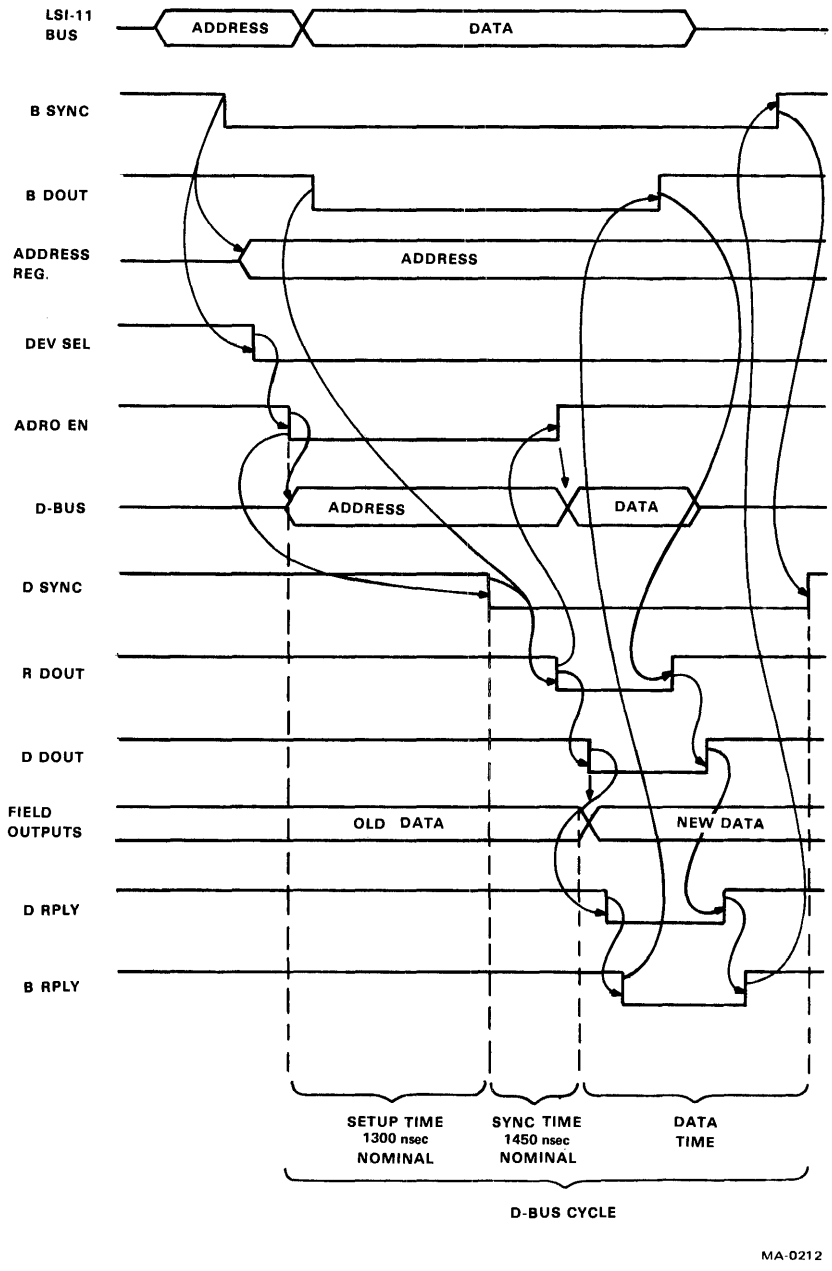


Figure 5-6 DATAO Timing

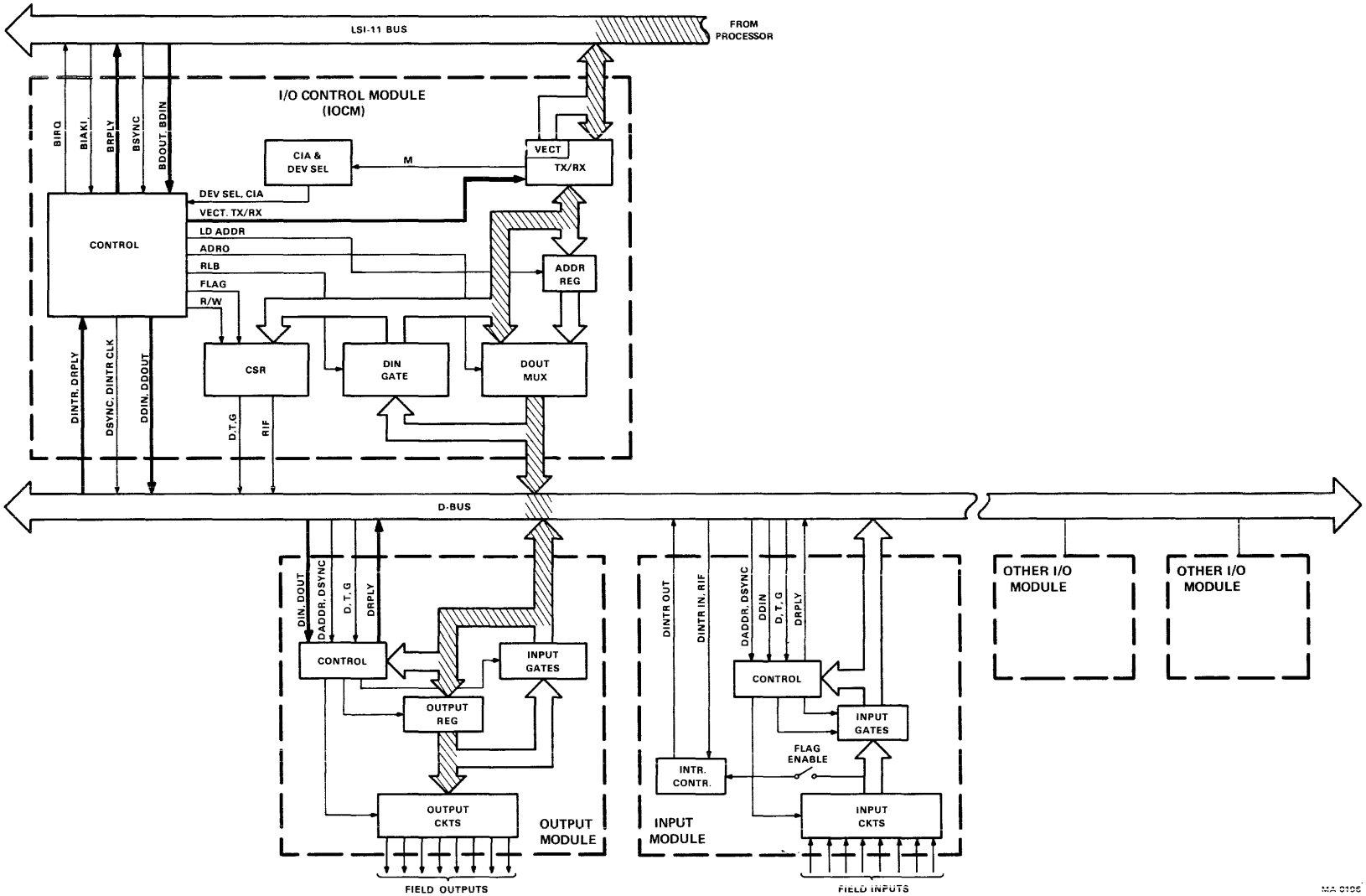


Figure 5-7 Data Output

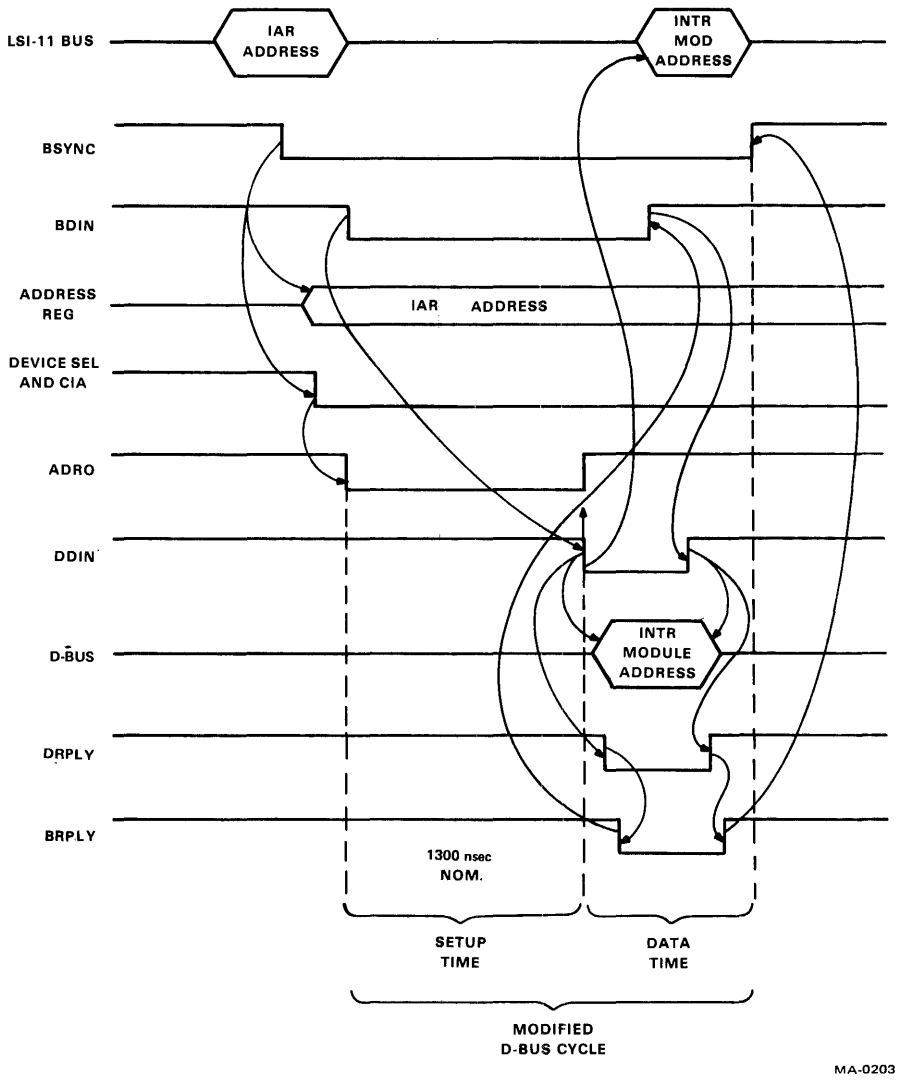


Figure 5-8 DATAI with Modified D-bus Cycle

When the D INTR signal is received by the IOCM, it initiates the LSI-11 interrupt sequence by setting the flag bit in the CSR (control and status register). This constitutes an I/O Subsystem interrupt request, and will be serviced if the enable bit in the CSR has been set by the program and the processor status allows interrupts. The signals involved in the LSI-11 interrupt sequence (B RPLY, B IRQ, and INTERRUPT VECTOR) are shown in Figure 5-9 along with I/O Subsystem interrupt signals (FLAG, D INTR, D RPLY, and RIF). The interrupt request/acknowledge sequence for the LSI-11 is covered in the Microcomputer Handbook.

When the program addresses the interrupting module after the RIF bit in the CSR has been set, the module's internal interrupt flip-flop will be reset. The timing diagram in Figure 5-10 will aid the reader in following the interrupt timing.

5.4.3 M7958 and M7959 Maintenance Mode

The IOCM has a maintenance mode that is activated when the program sets the M bit in the CSR. In this mode, the usual D-bus Cycle is not initiated when an attempt is made to read an I/O address. The address is put on the D-bus but D SYNC does not occur and there is no D RPLY. When the IOCM puts the D-bus data on the LSI-11 bus, the program reads back the address. This mode allows a diagnostic program to check the D-bus data lines for errors.

If the IOCM is in maintenance mode, it causes the CSR's F bit to be set. If the E bit is also set, subsystem interrupts are enabled and one occurs if the processor status allows. The M bit may be cleared by writing M=Ø in the CSR or by reading the CSR with R=1. Figures 5-11 and 5-12 show the signals, data paths, and timing of the maintenance cycle.

5.5 UNIBUS BASED SUBSYSTEM

In a UNIBUS based subsystem the IOCM is the M8719. As shown in Figure 5-1, all I/O modules reside on the D-bus under control of the IOCM and provide inputs from or outputs to the processor. The IOCM interfaces with both the D-bus and the UNIBUS. The major differences between the two buses are that the UNIBUS has 16 data lines and the D-bus has 8, and that the UNIBUS has separate address lines and the D-bus uses the same lines for addresses and data. The D-bus also has its own unique timing. These differences are provided for by the IOCM, which derives D-bus timing and data control signals from the standard UNIBUS signals. The following discussion of data transactions should aid in understanding the operation of the M8719.

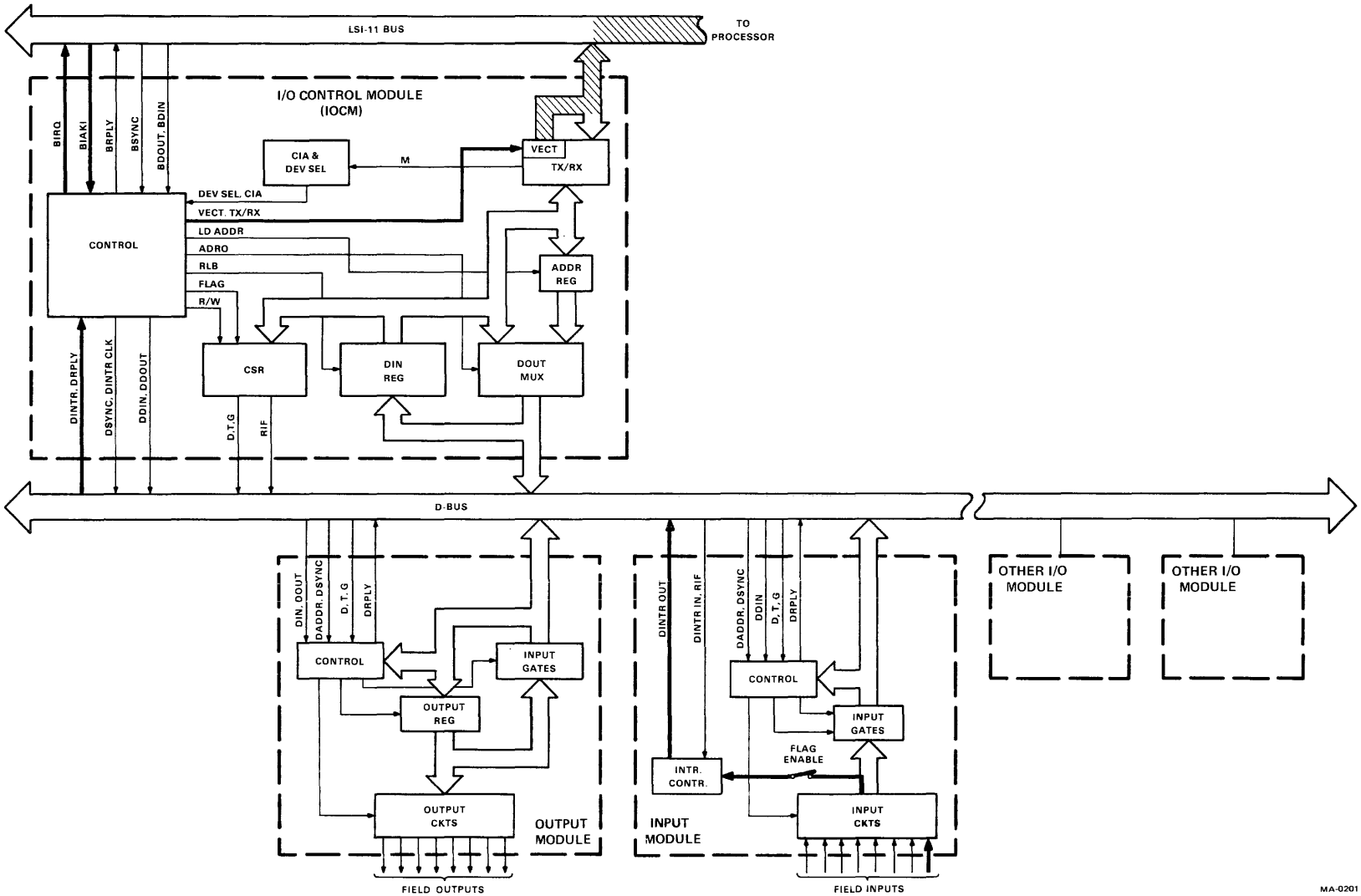


Figure 5-9 Interrupt Signals

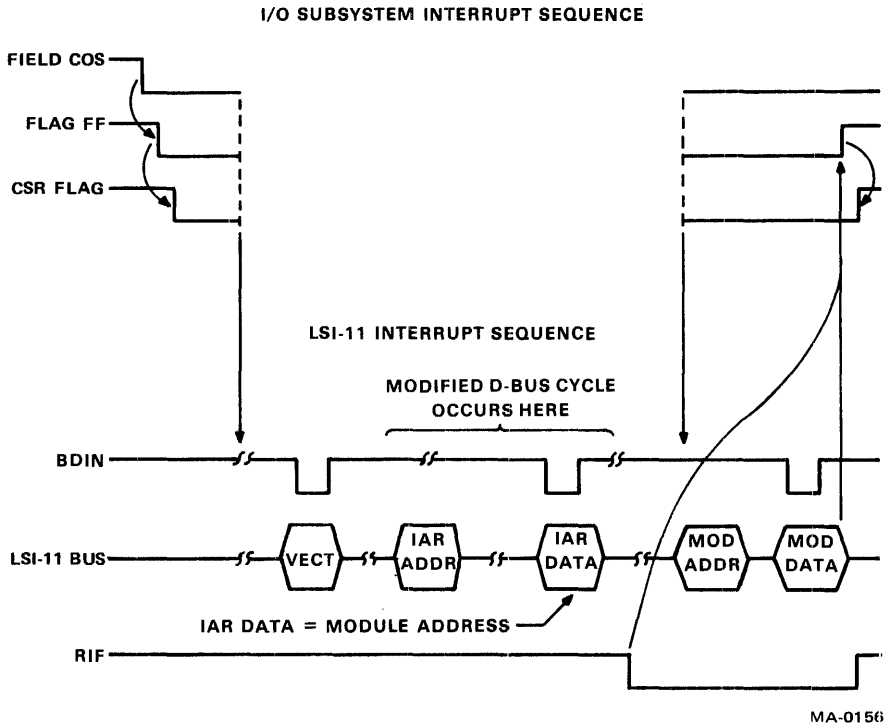


Figure 5-10 Interrupt Timing

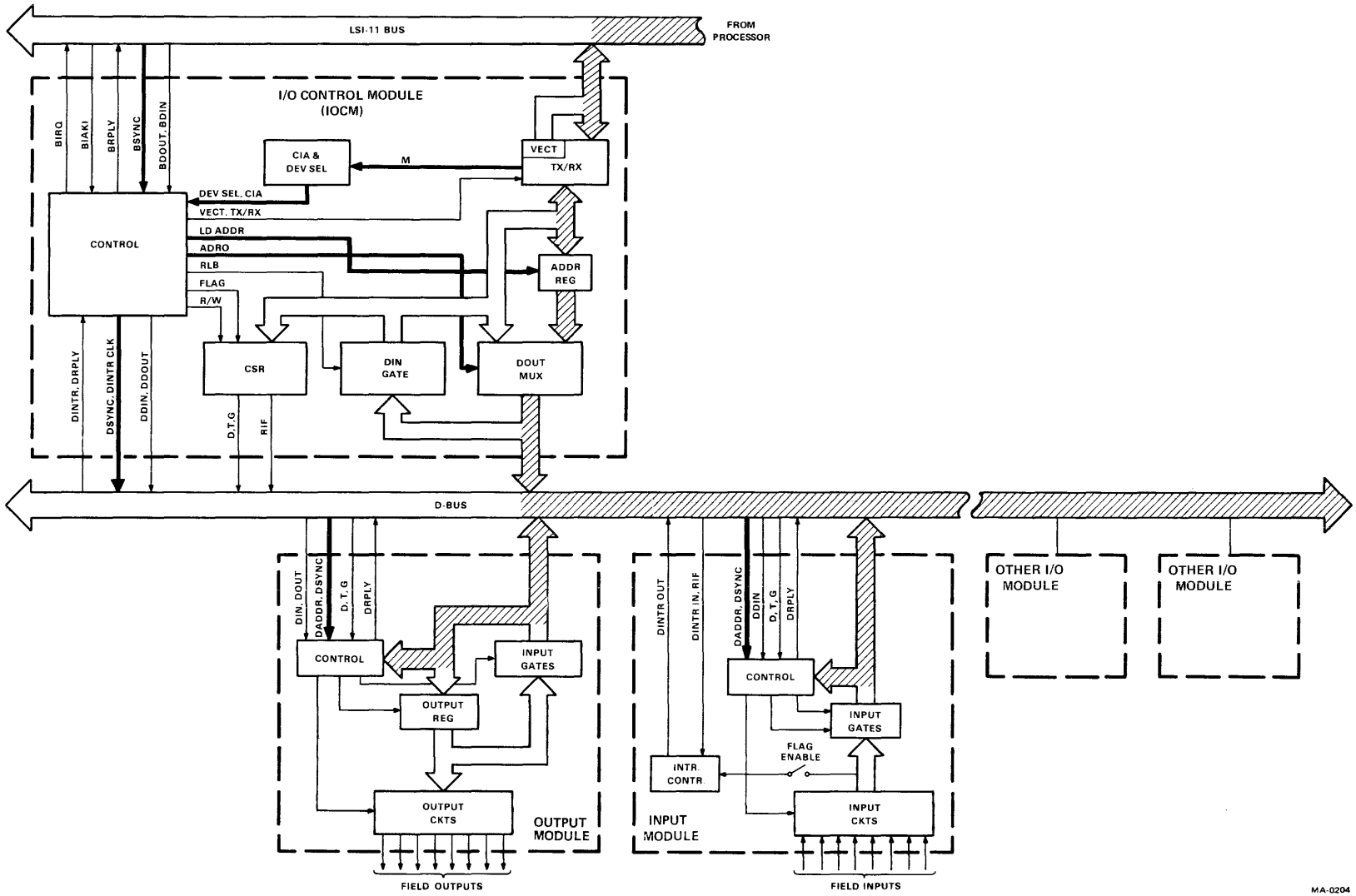


Figure 5-11 Maintenance Mode

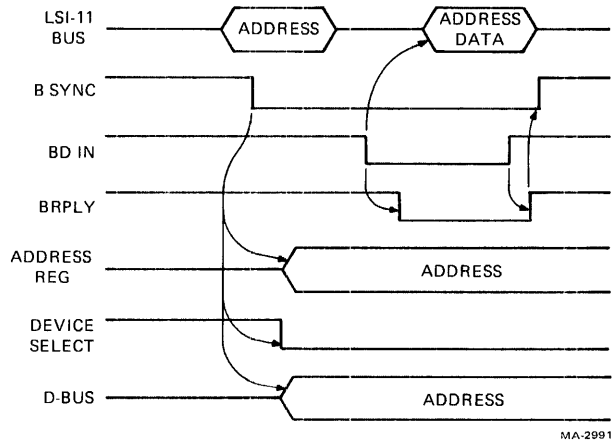


Figure 5-12 Maintenance Cycle Timing

5.5.1 M8719 D-bus Cycles

The timing signals that control the I/O module data transactions on the D-bus constitute the D-bus Cycle. Derivation of a DATAI D-bus Cycle is shown in Figure 5-13. The first four signals at the top of the figure are the signals initiated by the processor when executing a DATAI. The remainder of the sequence involves signals internal to the I/O Subsystem. The order of signal sequence is indicated by the arrows in the figure. If this timing diagram is related to the block diagrams of Figures 5-14 and 5-15, the functions performed during the sequence can be better visualized. In these figures, the active data paths are indicated by cross-hatching and the relevant control signals by bold lines.

The D-bus Cycle breaks down into three parts: SETUP TIME, SYNC TIME, and DATA TIME. The cycle is initiated by the MSYN (master sync) signal which starts the SETUP TIME phase of the cycle. SETUP TIME is defined by the 1500 DLAY signal which is produced by the IOCM control circuitry; it allows sufficient time for settling of address data on the D-bus. At the end of this delay, D SYNC (D-bus SYNC) is asserted, which causes the addressed I/O module to activate its internal MY ADDRESS signal. (MY ADDRESS is the name of the signal produced by an I/O module control circuit when it recognizes its address on the bus; it is the module's data transaction enabling signal.) The second part of the D-bus Cycle (SYNC TIME) is controlled by another delay circuit (2000 DLAY) in the IOCM. This delay allows at least a certain minimum time for the I/O module to prepare to transmit the appropriate data byte.

At the end of this delay, D DIN (D-bus Data In) is asserted telling the selected module to put its data on the D-bus. The module does this and replies by asserting D RPLY. Upon receiving D RPLY, the IOCM causes the D-bus data to be put on the UNIBUS data lines, and asserts BUS SSYN to indicate to the processor that it has done so. The processor accepts the data and negates MSYN to indicate that it has done so. The negation of MSYN causes the IOCM to negate D DIN, indicating to the module that the data has been

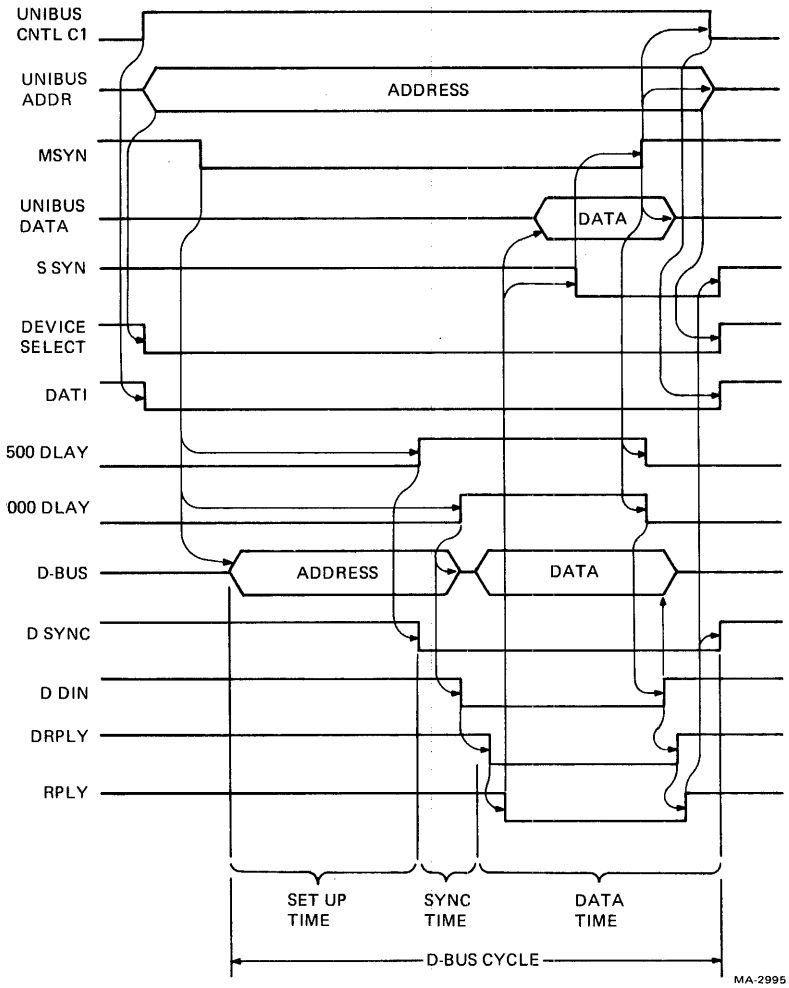


Figure 5-13 DATA I Cycle Timing

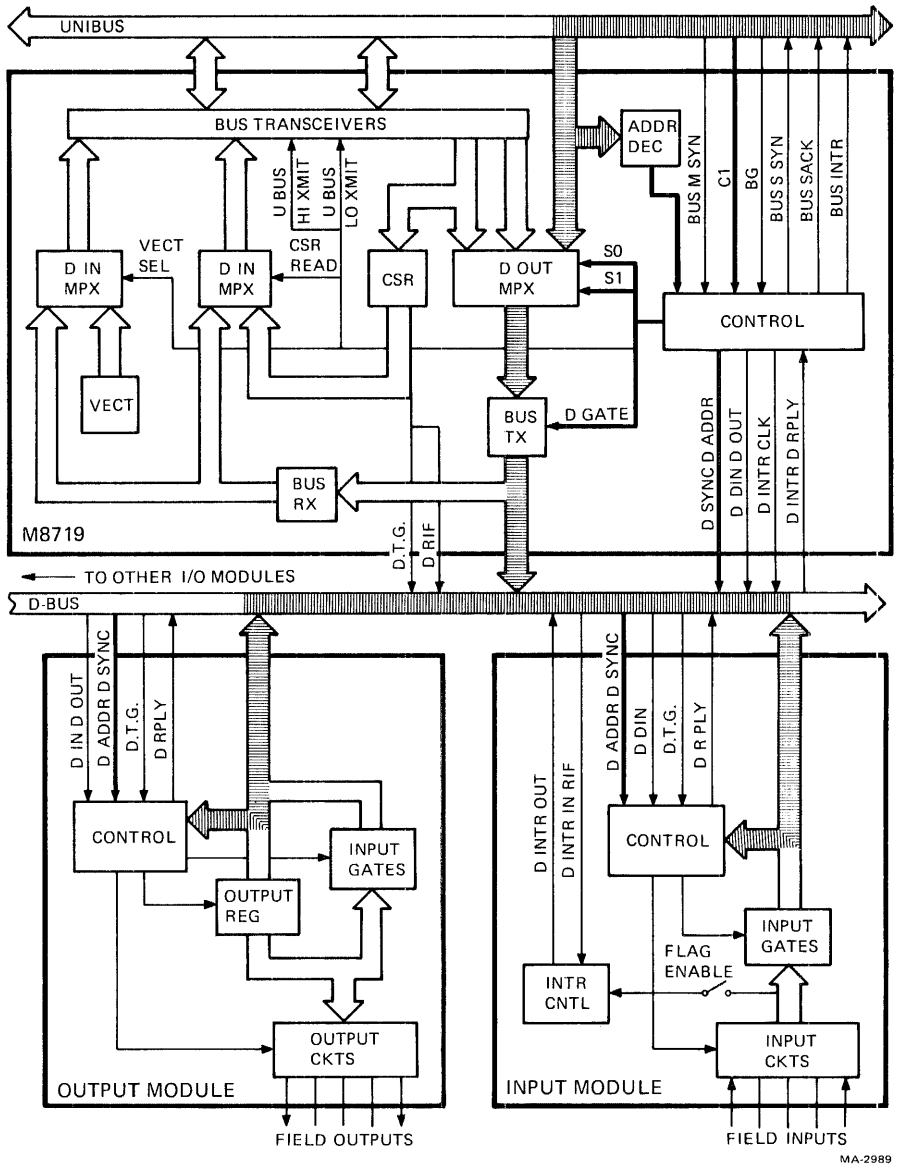


Figure 5-14 Addressing

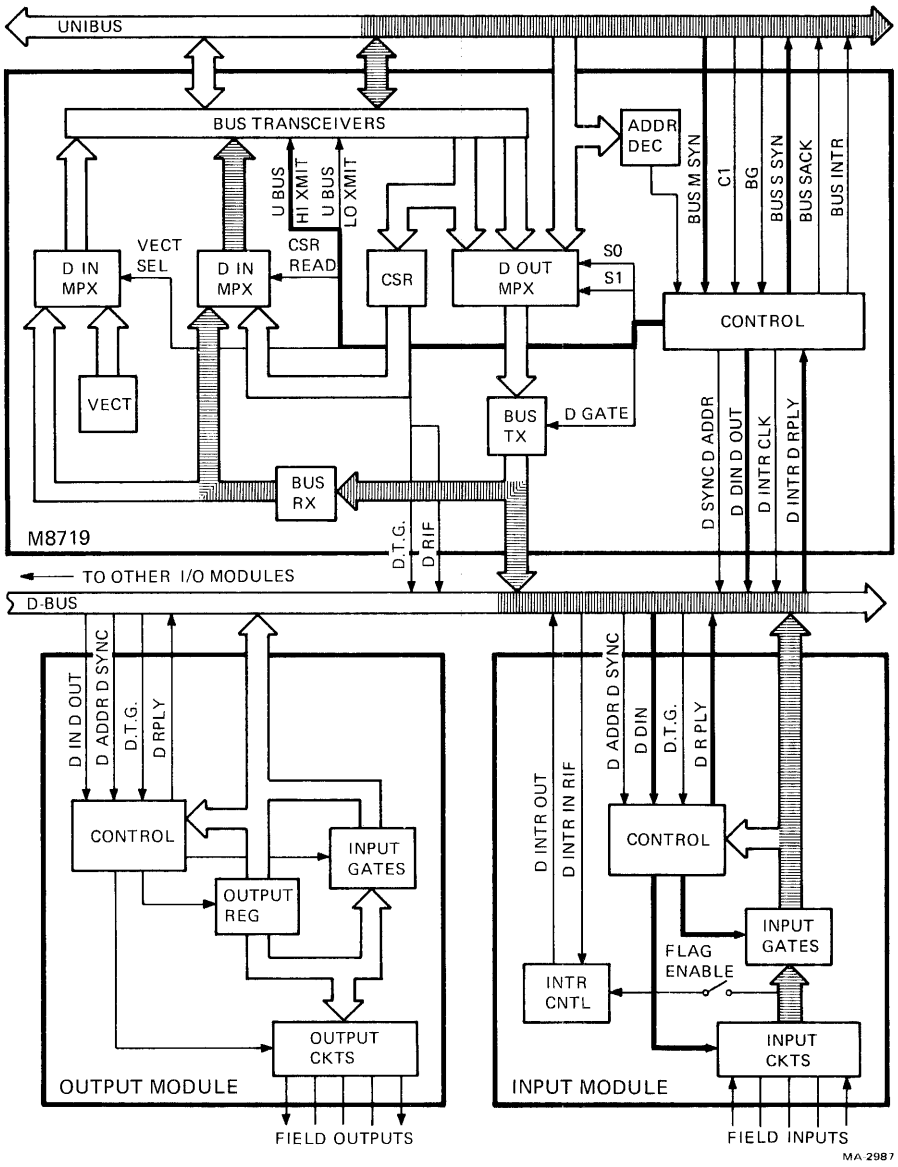


Figure 5-15 Data Input

received. The module then removes the data from the D-bus and negates D RPLY, causing the IOCM to negate D SYNC, and freeing the D-bus for the next I/O transaction. The IOCM simultaneously negates SSYN freeing the UNIBUS for the next processor transaction.

If the cycle is a DATO instead of a DATI, the sequence is almost the same as before. The difference is that the DATA TIME part of the cycle involves D DOUT instead of D DIN, resulting in a data transmission in the opposite direction (from the UNIBUS to the field outputs). This sequence is depicted in Figures 5-16 and 5-17. In a DATO, device selection is the same as in a DATI; however, after D SYNC is asserted, the IOCM waits for the I/O module address to be recognized from the D-bus, and replaces it with data from the appropriate byte of the UNIBUS. The IOCM waits for the data to settle, and then asserts D DOUT causing the selected module to clock the data into its register. The module indicates that it has accepted the data by asserting D RPLY. This causes the IOCM to assert SSYN on the UNIBUS, indicating to the processor that the data has been accepted. The processor acknowledges by negating MSYN, which causes the IOCM to negate D DOUT, indicating that the D-bus Cycle is ending. The module then negates D RPLY, causing the IOCM to negate D SYNC, freeing the D-bus for the next I/O transaction. The IOCM simultaneously negates SSYN, freeing the UNIBUS for the next processor transaction.

The I/O subsystem has no destructive read registers; therefore, the protocol for a DATIP is exactly the same as that for a DATI.

A modified D-bus Cycle occurs when the program reads the subsystem's IAR (interrupting address register). The IAR is read at the beginning of the interrupt routine when the main program is interrupted. (The IAR contains the address of the highest priority interrupting module on the D-bus.) The difference between the modified and ordinary D-bus Cycles is that D SYNC is inhibited in the modified cycle (SYNC TIME) and D ADDR is asserted instead. When D DIN occurs (DATA TIME), the module puts its address on the D-bus instead of data, and the program reads the address of the interrupting module at the IAR address. Modified D-bus Cycle timing is shown in Figure 5-18.

5.5.2 M8719 Interrupts

Some modules can interrupt the program for priority service if, for example, one of its field inputs changes state. If a change of state occurs, the module's flag flip-flop is set and initiates an interrupt sequence by putting the D INTR signal on the D-bus. This signal is daisy-chained along the D-bus and ORed with any D INTR signals from other modules. The interrupt control line (D INTR INH), which is also daisy-chained along the D-bus, ensures that if there is more than one module with an interrupt pending, the one that is serviced first is the one with the highest priority (the module in the lowest numbered slot of the lowest numbered chassis).

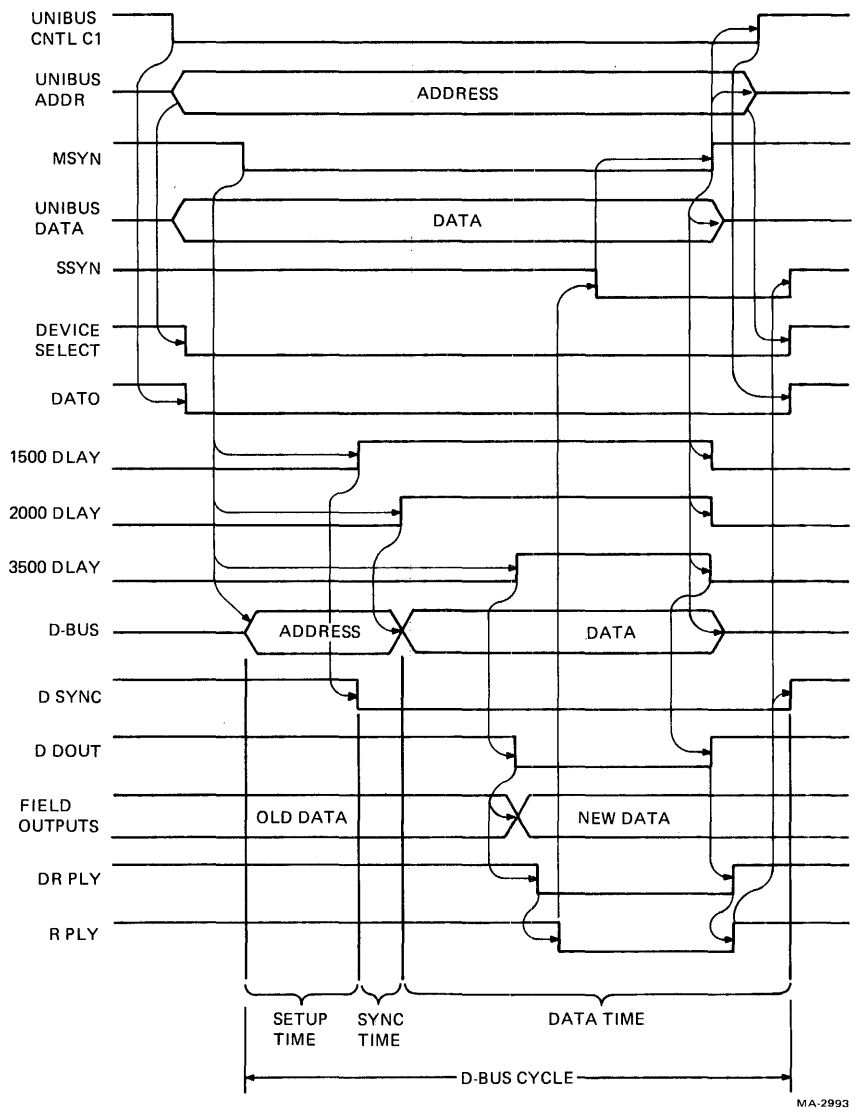


Figure 5-16 DATA O Cycle Timing

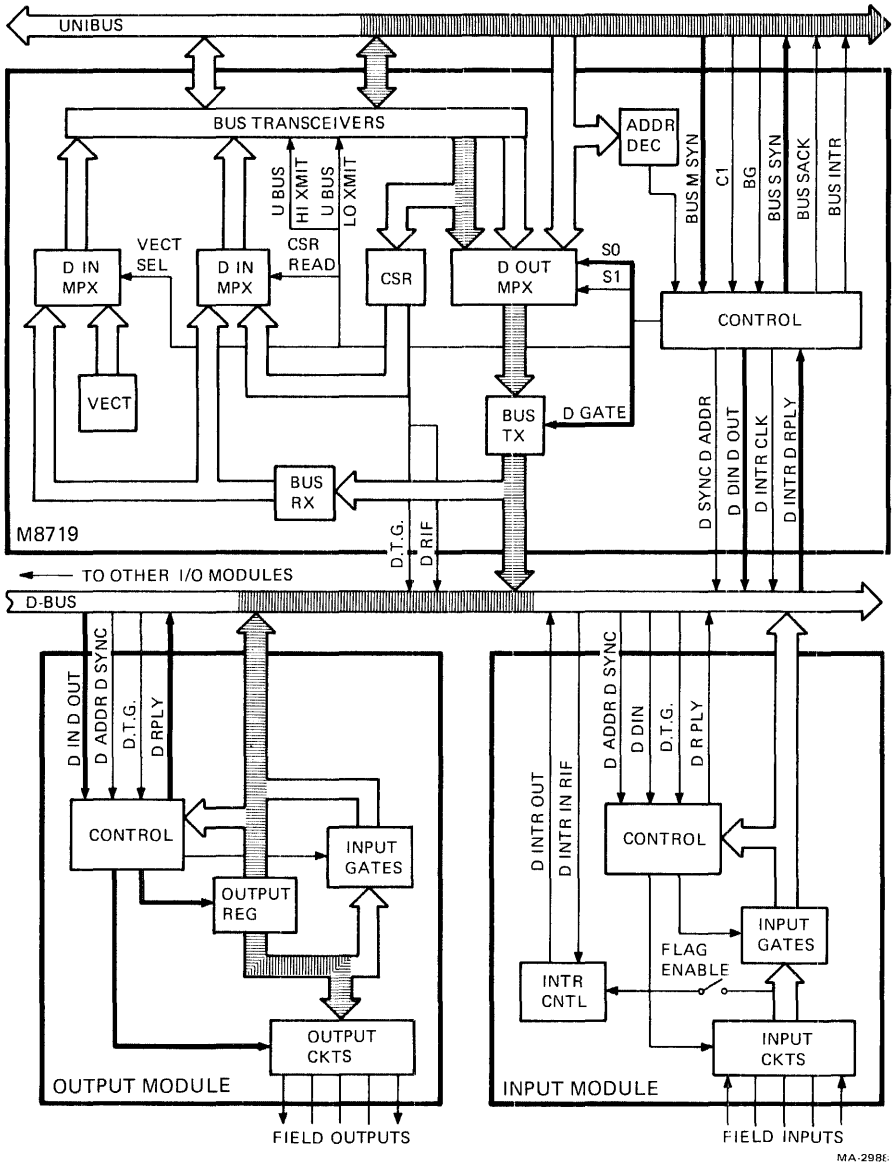


Figure 5-17 DATA Output
(Upper Byte Transfer Shown)

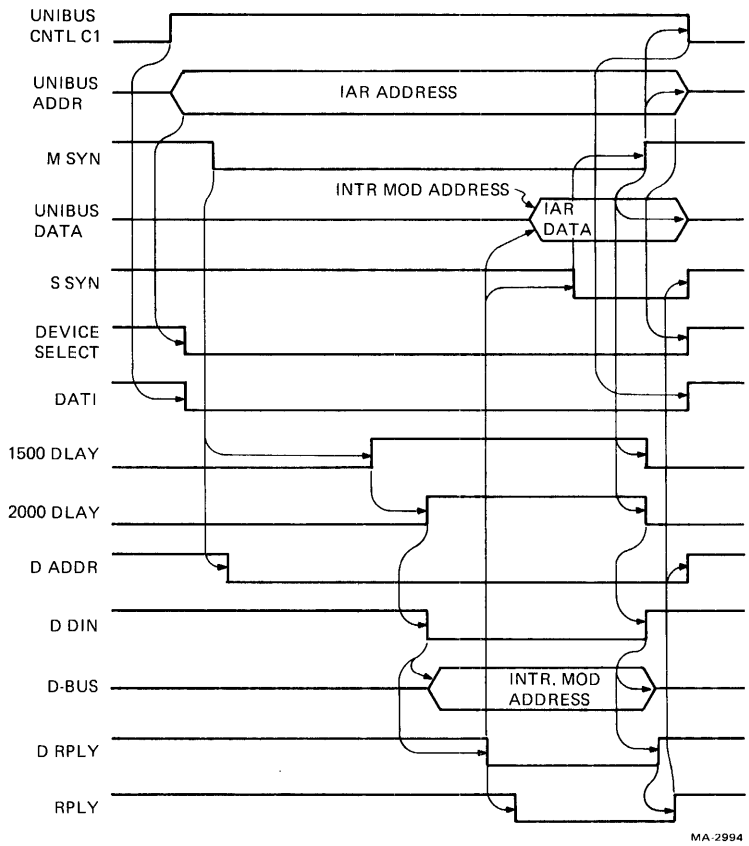


Figure 5-18 DATI with Modified D-bus Cycle

When the D INTR signal is received by the IOCM, the flag bit is set in the CSR (control and status register). This constitutes an I/O Subsystem interrupt request, and will be serviced if the enable bit in the CSR has been set by the program and the processor status allows interrupts. The signals involved in the PDP-11 interrupt sequence (BUS INTR, BR, BG, BUS SACK, and INTERRUPT VECTOR) are shown in Figure 5-19 along with the I/O Subsystem interrupt signals (FLAG, D INTR, D RPLY, and RIF). The interrupt signal sequences for the PDP-11 are covered in the PDP-11 Peripherals Handbook.

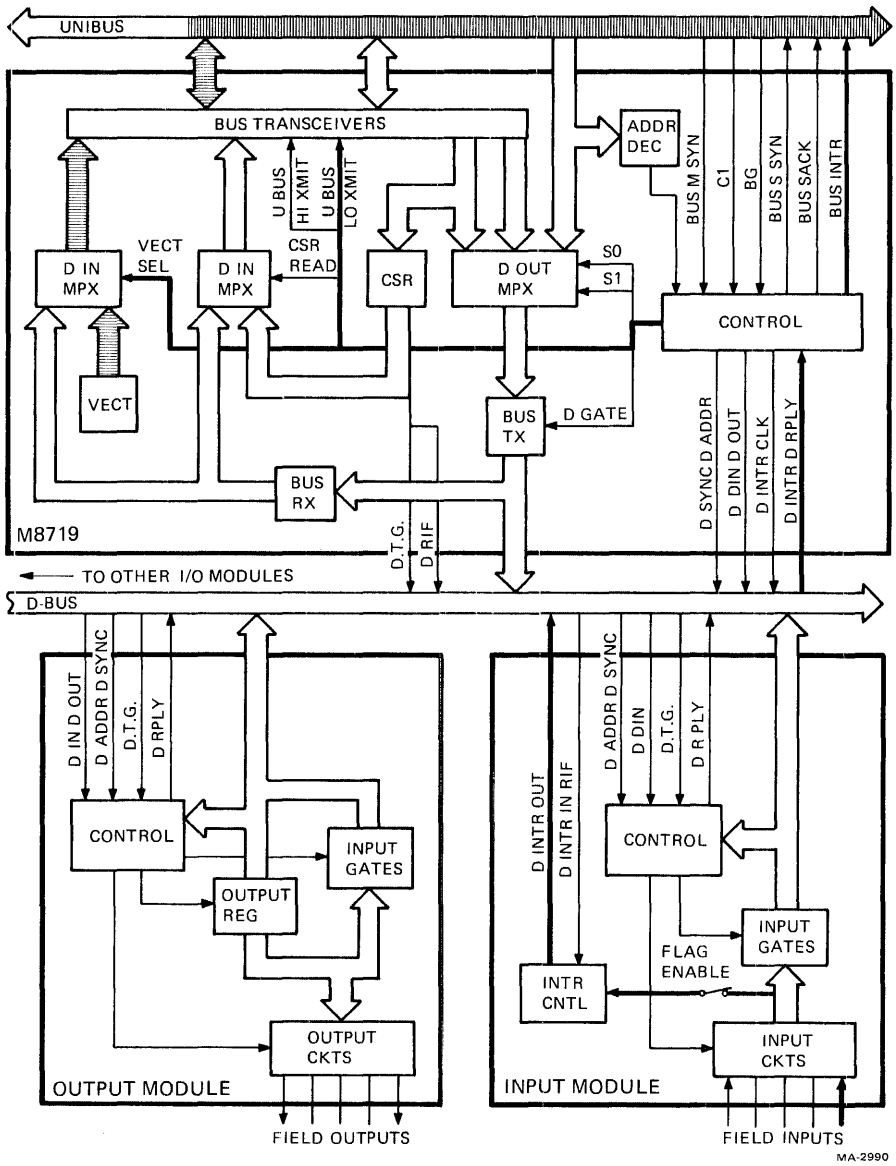


Figure 5-19 Interrupt

When the program addresses the interrupting module after the RIF bit in the CSR has been set, the module's internal interrupt flip-flop will be reset. The timing diagram in Figure 5-2Ø will aid the reader in following the interrupt timing.

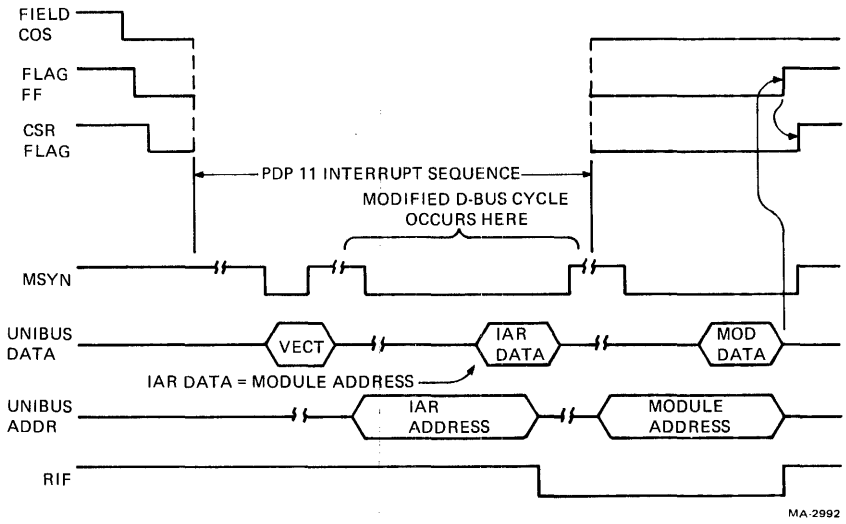


Figure 5-2Ø I/O Subsystem PDP-11 Based Interrupt Timing

5.5.3 M8719 Maintenance Mode

The IOCM has a maintenance mode that is activated when the program sets the M bit in the CSR. In this mode, the usual D-bus Cycle is not initiated when an attempt is made to read an I/O address. The address is put on the D-bus but D SYNC does not occur and there is no D RPLY. When the IOCM puts the D-bus data on the UNIBUS data lines, the program reads back the address. This mode allows a diagnostic program to check the D-bus data lines for errors.

If the IOCM is in maintenance mode, it causes the CSR's F bit to be set. If the E bit is also set, subsystem interrupts are enabled, and one occurs if the processor status allows. The M bit may be cleared by writing M=Ø in the CSR or by reading the CSR with R=1. Figures 5-21 and 5-22 show the signals, data paths, and timing of the maintenance cycle.

5.6 SYSTEM POWER SUPPLIES

There are two power supplies used with I/O subsystems. They are the H787Ø and H7872, intended respectively for the H333 and the H334 I/O module chassis. The difference between the two supplies is that the H787Ø provides power for both I/O modules and LSI-11 components, and the H7872 provides only I/O module power.

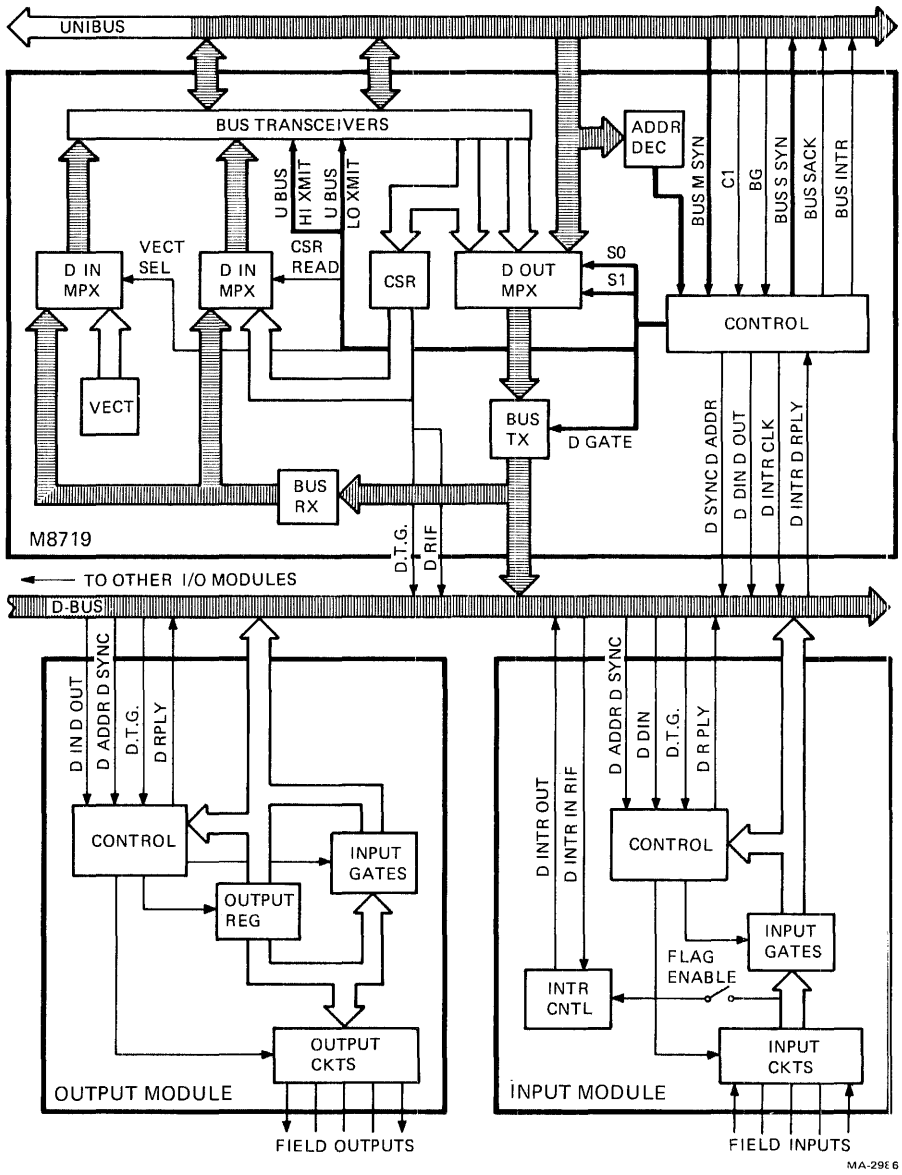


Figure 5-21 Maintenance Mode (M=1 in CSR)

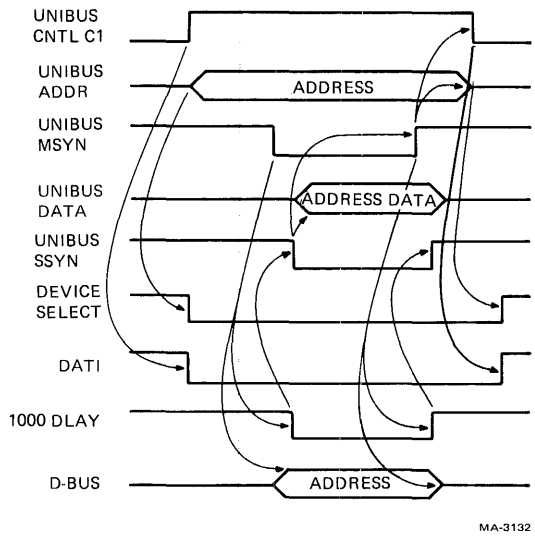


Figure 5-22 Maintenance Cycle Timing

If an LSI-11 bus is included in an I/O Subsystem, it appears only in the H333 chassis; therefore, the H333 chassis is the only one in which the H7870 is mandatory. However, since an H7870 can power I/O modules as well as LSI-11 options, some early systems use the H7870 in both the H333 and H334 chassis. In this case, one H7870 is used to power two H334 chassis, or if there are no LSI-11 modules present, the H333 chassis and one H334 chassis. This requires some interchassis wiring which is not the same for all system configurations. Details of this wiring are covered in the installation instructions of Chapter 3, Paragraph 3.3.2.4.

5.6.1 H7870 Power Supply

The H7870 power supply provides both +12 Vdc and +5 Vdc outputs as well as some LSI-11 control functions. The supply is a separate unit that slides into the bottom of the H333 or H334 chassis. AC power is input through the front panel via a line cord; dc voltages are output via a cable with a connector that plugs into the chassis. When used with the H333 chassis, there is an additional cable that carries the LSI-11 functions (i.e., B DCOK, B POK, B EVNT, B HALT, and S RUN) from the H7870 printed circuit board to the backplane of the H333 chassis. There is only one version of the H7870 power supply. Conversion from 115 V to 230 V operation is accomplished by manipulating internal jumpers and changing the fuse and line cord. The H7870 front panel controls and indicators (Figure 5-23) are described below.

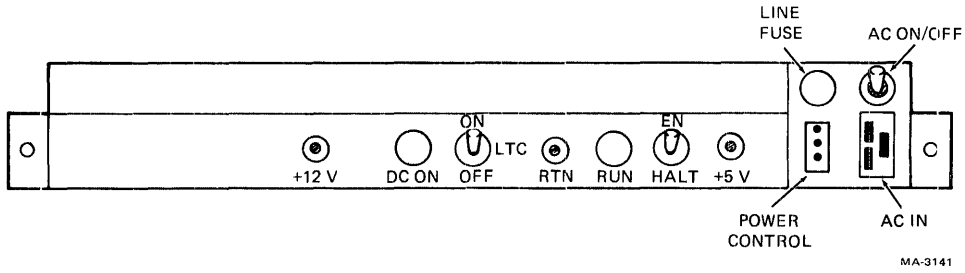


Figure 5-23 H7870 Power Supply

AC ON/OFF switch	Applies ac power to the H7870 and activates the power control outlet
Line fuse	Protects against ac line overload. Fuse rating is 6.25 A for 115 V operation, or 3 A for 230 V operation
Power control outlet	When connected to the power control bus, ties ac power ON/OFF control of all power controllers to the AC ON/OFF switch of the H333 chassis
Ground lug	Provides a safety ground connection to the power supply chassis
LTC switch*	When on, enables B EVNT L, which is an LSI-bus compatible line frequency signal generated by the H7870
EN/HALT switch*	When on, enables program execution by the LSI-11; when off, it places the processor in halt mode
DC ON indicator	When lit, indicates that dc power is on Should light when the ac ON/OFF switch is turned on.
RUN light*	When lit, indicates that the LSI-11 processor is running
+5 V test point*	For measuring +5 Vdc output
+12 V test point	For measuring +12 Vdc output
RTN test point	Meter return for dc voltage measurement

* Applies only if an LSI-11 is present in the H333 chassis.

5.6.2 H7872 Power Supply

The H7872 is a +12 Vdc regulated power supply used for powering the H334 chassis. The supply is a separate unit that slides into the bottom of the H334 chassis. AC power is input through the front panel via a line cord and +12 Vdc is output via a cable with a connector that plugs into the H334 chassis. There are two versions of the supply: H7872-A powered by 115 Vac, and H7872-B powered by 230 Vac.

5.6.2.1 H7872 Detailed Description - A functional block diagram and basic construction of the supply are shown in Figures 5-24 and 5-25 respectively.

Primary power (115 Vac or 230 Vac) is applied to the ac input connector via the proper line cord (Figure 5-25). The line fuse and barrier terminal strip jumper configuration are also functions of the type of service (115 Vac or 230 Vac) intended.

AC power from the terminal strip is applied to the stepdown transformer, the output of which is applied to the rectifier and filter circuit. The resultant dc power is applied to fuse F1 and through the series pass transistors to output connector P1. Fuse F1 protects the circuit board etch in the event of a circuit failure. Output current and voltage are monitored by the regulator circuit which controls the voltage drop across the pass transistors. This circuit provides output voltage regulation and foldback current limiting which ensures that the maximum current output never exceeds 7 A (3 A maximum if the output is shorted). The crowbar circuit shown shorts the power supply output to protect the subsystem from an overvoltage condition. Fuse F2 protects the circuit board etch in the event of crowbar SCR failure. The LED at the output lights when the output voltage is present. Output connector P1 is on the end of a cable that plugs into a mating connector on the H334 chassis. Test points TP1 and TP2 are located on the front panel, and provide a convenient means of measuring output voltage.

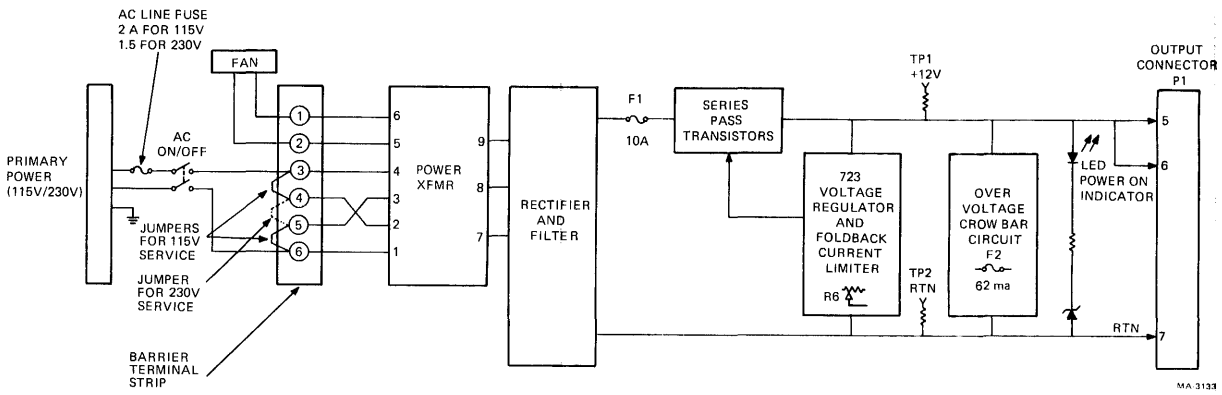


Figure 5-24 H7872 Power Supply Block Diagram

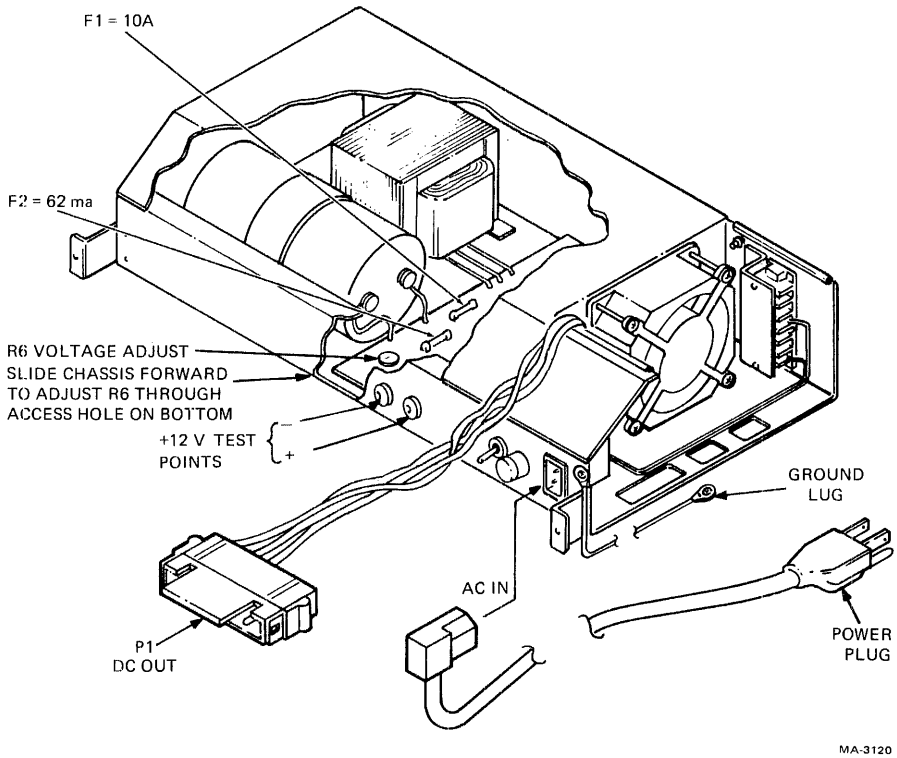


Figure 5-25 H7872 Power Supply

CHAPTER 6
FUNCTIONAL I/O MODULES

6.1 INTRODUCTION

This chapter contains data sheets for each functional I/O module used in the I/O Subsystem. Each sheet includes a functional description, specifications, and other pertinent data to aid the user in implementing the modules in his particular system. The sheets are arranged in the following order.

M5010	M6010	A014
M5011	M6010-YA	A156
M5012	M6011	A157
M5012-YA	M6012	A020
M5013	M6013	ATR16
M5014	M6014	A630
M5016	M6015	A631
M5031	Analog Input Subsystem - General	BC40L

The user should carefully read the data sheets for each module in his system, paying particular attention to any of the switch-selectable options that may pertain to his system.

6.2 MODULE INTERFACES

All I/O modules in this chapter provide an interface between field equipment and the D-bus. Standard D-bus signals are shown in Table 6-1-1; those that are relevant to a particular module are discussed in the individual module sections. The field interface connector configuration is shown for each type module for a customer providing his own field wiring terminations. Customers using optional DIGITAL-supplied screw terminal field wiring terminations are referred to Chapter 3 (Installation) for a description of field wiring configurations for each type module.

6.3 NUMBERING CONVENTIONS

To avoid confusion, the reader should remember that, in all module descriptions, octal numbers are used for channel numbers, generic codes, and addresses. Everything else is numbered decimally.

Table 6-1-1 D-Bus Interface Connector Pin Assignments

Pin	Connector C		Connector D	
	Side 1	Side 2	Side 1	Side 2
A	+12 V	Not Used	+12 V	Not Used
B	D MUX REL L	●	D AUTO ZERO L	●
C	+12 V	GND	+12 V	GND
D	+12 VB	"	+12 VB	"
E	D DØØL	"	D GBIT L	"
F	D DØ1 L	"	D TBIT L	"
H	D DØ2 L	"	D DBIT	"
J	D DØ3 L	"	D RIF L	"
K	D DØ4 L	"	D INTR OUT L	D INTR IN L
L	D DØ5 L	"	D INTR INH IN L	D INTR INH OUT
M	D DØ6 L	"	D INTR CLOCK L	"
N	D DØ7 L	"	D ADDR L	"
P	D DSYNC L	"	D MUX READY L	●
R	D DIN L	"	D ANA GUARD	●
S	D DOUT L	"	D ANA SIG	●
T	GND	D ANA ERROR IN L	GND	D ANA ERROR OUT
U	D RPLY L	"	D MUX STROBE L	●
V	D INIT L	"	D SYS CLOCK L	"

Notes
1. _____" = bussed connection
2. _____● = daisy-chain connection
3. Module connectors C and D are shown here with all D-bus signals, but a given I/O module uses only those signals relevant to its function. The only I/O module connections on connectors A and B (not shown) are jumpers AM2 to AN2 and AR2 to AS2.

FUNCTIONAL DESCRIPTION

The M5010 is a nonisolated dc sense module used for monitoring voltages or contact closures. The module accepts up to 32 inputs, structured as four 8-bit bytes, and sends them under program control to the processor. Provision is made for program-controlled testing, input disabling, and reading the module's generic code. The module also features an address selection switch and fuse protection.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-2-1 shows that field data entering through J1 is addressed and controlled by signals from the D-bus interface connector and is ultimately output to the D-bus. The sequence of control and data flow is as follows.

Data Paths

Each of the 32 field signals entering at J1 passes through a signal conditioning network that serves to protect the module's circuitry and enhances the integrity of the input signal. This network is made up of a diode, two resistors, and a capacitor. The diode protects the input circuit from high positive input voltages by becoming back-biased and the resistor combination protects from high negative inputs by dividing the current to favor protection of the series path. The series resistor and parallel capacitor constitute a low pass filter that provides moderate high frequency noise immunity.

After the above conditioning, each signal is applied to the input of a Schmitt trigger which converts the field input levels to CMOS levels required by the I/O subsystem.

All field signal common connector pins are bussed together and go to the module ground through a series fuse, F-1. This fuse protects the module from any common mode voltage difference between the field equipment and the I/O Subsystem.

From the outputs of the Schmitt triggers the signals go to the control gating section. This section also receives two control inputs from the D-bus interface connector: TBIT and DBIT, which under program control, may modify the data for testing. The output of this section is normal data, if these controls are not asserted. If the program causes TBIT to be asserted, the output is disabled and is read as all zeros. If both TBIT and DBIT are asserted, the output is read as all ones.

The 32 bits out of the input gating section are grouped into four 8-bit bytes for the input multiplexer. One of these bytes is selected under control of the A0 and A1 signals from the multiplexer control and is sent to the G multiplexer. The G multiplexer outputs normal data to the D-bus input gating, unless the GBIT is asserted. If the program asserts the GBIT, the G

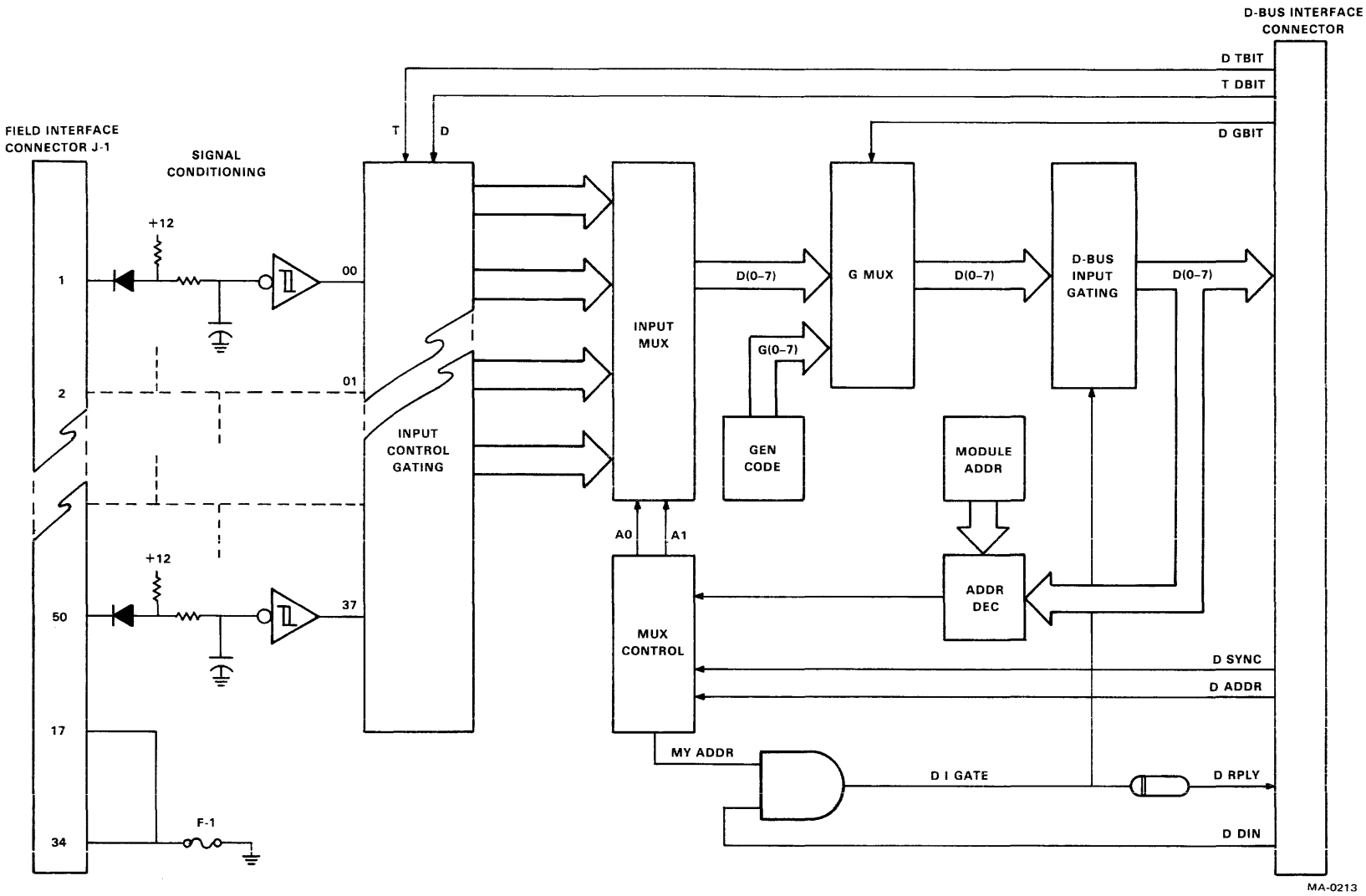


Figure 6-2-1 Module M5010, 32-Bit Nonisolated DC Sense, Simplified Block Diagram

multiplexer transmits the module's generic code to the D-bus input gating instead of normal data. Data is then strobed onto the D-bus by the DI GATE signal.

Control Signals
Control signals for the above sequence are initiated by the program, resulting in the following control sequence. When the program calls for a DATAI from one of the module's four addresses, the IOCM starts a D-bus Cycle and causes the address to be put on the D-bus. The module's address decoder decodes the address and, after a short delay for deskewing, D SYNC is asserted. This causes the multiplexer control to produce the AØ and A1 signals for the selection of the correct data byte by the input multiplexer. At this time MY ADDRESS is also produced. After a short delay, D DIN is asserted and ANDed with MY ADDRESS to give DI GATE, which strobes data onto the D-bus. After a short delay, DI GATE also produces D RPLY to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated, causing DI GATE to negate and remove data from the D-bus.

If a modified D-bus Cycle follows to read the IAR, the D ADDR signal clears the MY ADDRESS signal. This is necessary because in a Modified D-bus Cycle, D SYNC does not occur. This means that when D DIN occurred it would put the module's data on the bus again, where it would overlap the IAR data.

Address Selection
The four addresses for the module must be assigned according to the rules stated in Chapter 4. They are selected on the module by the eight-pole switch, E-41 (Figure 6-2-2). To illustrate the use of this switch an example of one possible address selection is shown in Figure 6-2-3.

Generic Code
The generic code for the M5Ø1Ø module is octal 141.

Pin Connections
The M5Ø1Ø module pin connections for J1, the I/O cable connector, are shown in Table 6-2-1.

Application Notes

1. If unused inputs of an M5Ø1Ø are left open circuited, they can be influenced by external noise. The random switching of these inputs could be a cause of confusion to the application program. It is, therefore, always good practice to tie these unused inputs high (a logic zero).

2. When used for contact closure detection, a pull-up at the user end of the field wire prevents the field wire from acting like an antenna.

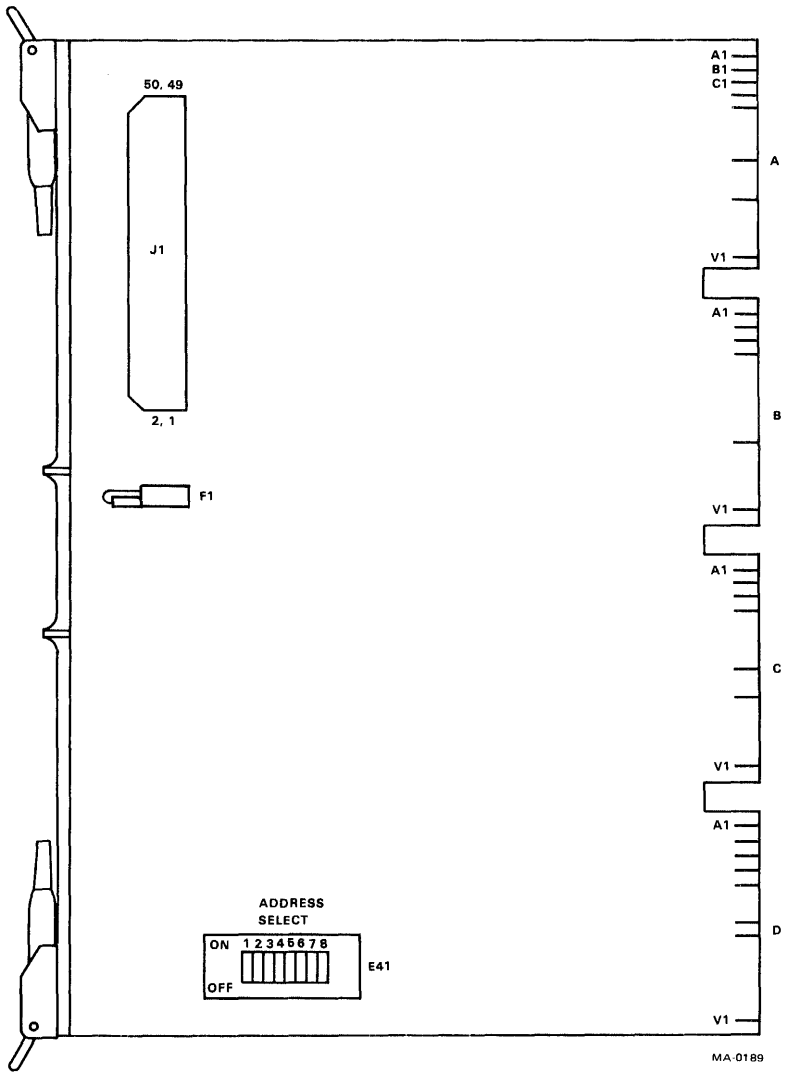


Figure 6-2-2 M5Ø1Ø 32-Bit DC Sense Module

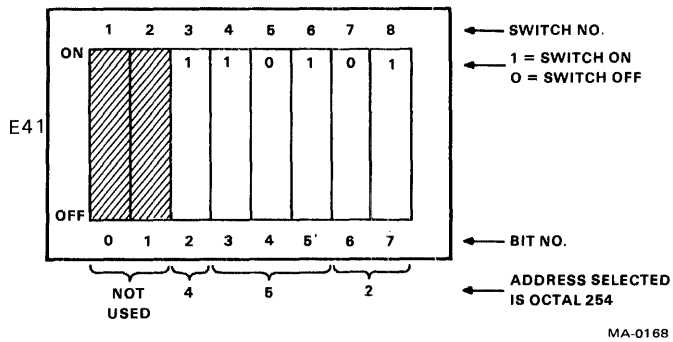


Figure 6-2-3 Address Selection Switch

Table 6-2-1 Module M5Ø1Ø I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	ØØ	2	Ø1
3	Ø2	4	Ø3
5	Ø4	6	Ø5
7	Ø6	8	Ø7
9	1Ø	1Ø	11
11	12	12	13
13	14	14	15
15	16	16	17
17	Common	18	Common
19	↑	2Ø	↑
21	|	22	|
23	|	24	|
25	|	26	|
27	|	28	|
29	|	3Ø	|
31	|	32	|
33	Common	34	Common
35	2Ø	36	21
37	22	38	23
39	24	4Ø	25
41	26	42	27
43	3Ø	44	31
45	32	46	33
47	34	48	35
49	36	5Ø	37

SPECIFICATIONS

Power Requirements

Voltage — Main supply: VS = 12 Vdc ± 2 Vdc
Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc

Operating current — 87 mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 73 mA maximum
Backup supply: 14 mA maximum

Standby current (backup supply) — 14 mA maximum

Input Characteristics	
Positive input voltage	+55 V maximum
Negative input voltage	-3Ø V maximum
Common mode input voltage	Ø V maximum
Logic zero threshold	8.2 V typical 12 V maximum
Logic one threshold	3.8 V typical 1.4 V minimum
Hysteresis	4.3 V typical
Input currents	At input = Ø V Ø.47 mA typical Ø.73 mA maximum At input = -3Ø V 2.Ø mA typical 2.7 mA maximum At input = +55 V Ø.Ø5 microamp typical 5Ø microamp maximum
Propagation delay	5.5 microseconds maximum
Fuse	Picofuse 62.5 mA
Mechanical	
Dimensions	Quad module, single width, 8-1/2 inch length
Field connector	Cable type BC4ØA or customer-supplied, 5Ø-pin Berg.
Environmental	Complies with DEC STD 1Ø2, Class C. Operates in convection cooled environment up to 6Ø degrees C ambient.
Heat dissipation	Ø.177 Btu/hr maximum due to module circuits 11.Ø Btu/hr maximum due to field inputs

FUNCTIONAL DESCRIPTION

The M5Ø11 is a nonisolated dc input module used for monitoring voltages or contact closures. COS (change-of-state) initiated interrupt capability is also provided. The module accepts up to 16 inputs, structured as two 8-bit bytes, and sends them under program control to the D-bus. Two additional bytes contain COS information. Provision is made for program-controlled testing, input disabling, and reading the module's generic code. The module also features an address selection switch, interrupt enable switches for all 16 bits, and fuse protection.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-3-1 shows that field data entering through J1 is addressed and controlled by signals from the D-bus interface connector and is ultimately output to the D-bus. Also shown is the interrupt selection and control circuitry, which provides the option of having the module initiate a processor interrupt when any input changes state. Data paths and their control are discussed below.

Data Paths

Each of the 16 field signals entering at J1 passes through a signal conditioning network that protects the module's circuitry and enhances the integrity of the input signal. This network is made up of a diode, two resistors, and a capacitor. The diode protects the input circuit from high positive input voltages by becoming back-biased; the resistor combination protects from high negative inputs by dividing the current to favor protection of the series path. The series resistor and parallel capacitor constitute a low pass filter that provides moderate high frequency noise immunity.

After the above conditioning, each signal is applied to the input of a Schmitt trigger which converts the field input levels to CMOS levels required by the I/O Subsystem.

All field signal common connector pins are bussed together and go to the module ground through a series fuse, F-1. This fuse protects the module from any common mode voltage difference between the field equipment and the I/O Subsystem.

From the outputs of the Schmitt triggers, the signals go to the control gating section. This section also receives two control inputs: TBIT and DBIT, from the D-bus interface connector, which under program control may modify the data for testing. The output of this section is normal data if these controls are not asserted. If the program causes TBIT to be asserted, the data output will be inverted. If DBIT is asserted, the output is disabled and is read as all zeros. If both TBIT and DBIT are asserted, the output is read as all ones.

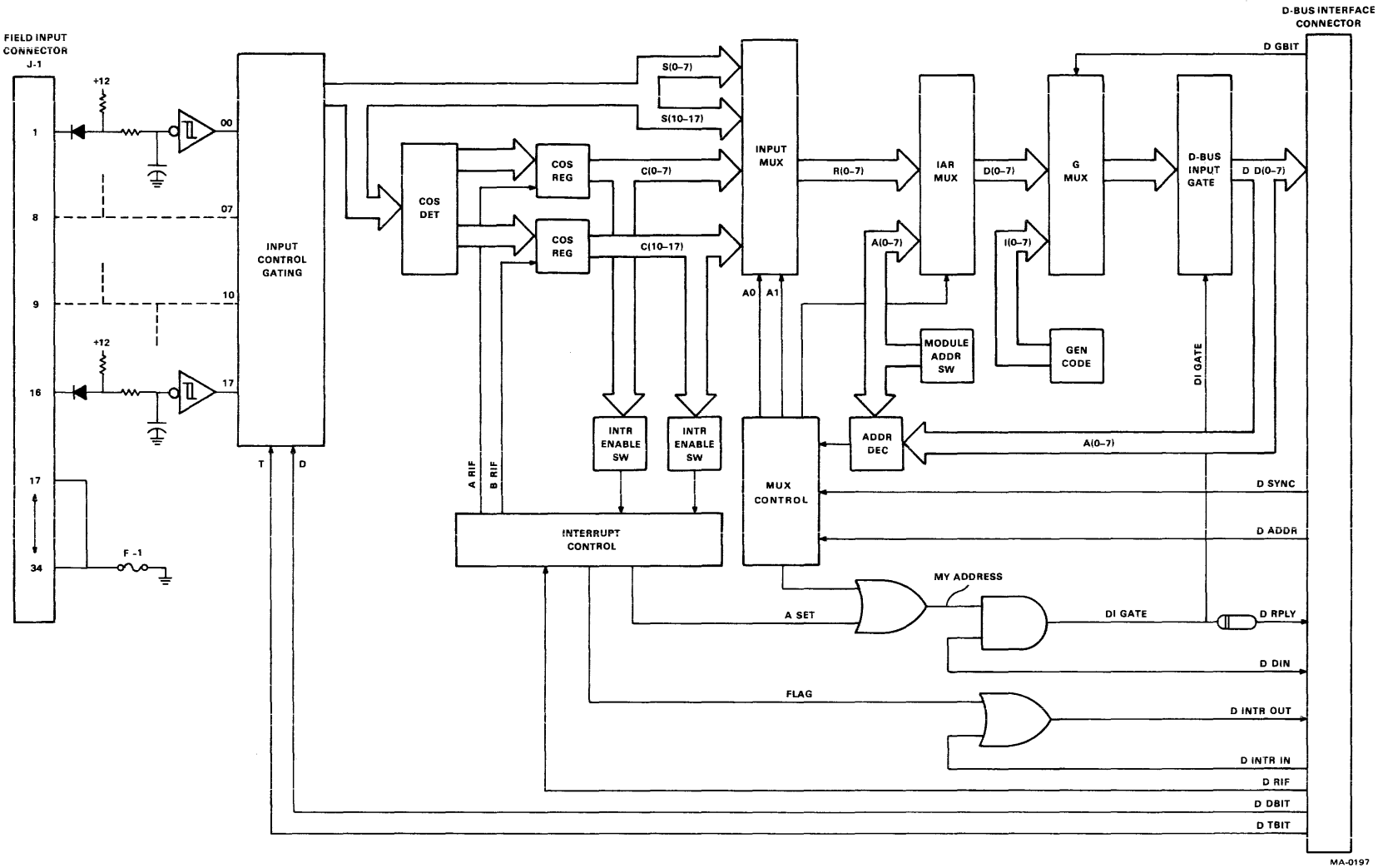


Figure 6-3-1 16-Bit COS Input Module M5011, Simplified Block Diagram

The 16 outputs of the input gating section are separated into two 8-bit bytes and go to both the input multiplexer and the COS detectors. If any of the field data bits changes state, this event is stored as a one in the COS register. The output of these registers also goes to the input multiplexer.

When the module is addressed, one of the four byte inputs to the input multiplexer is selected by the AØ and Al signals from the multiplexer control and sent to the IAR multiplexer. If the module has an interrupt pending, and there is no higher priority interrupt, the IAR multiplexer outputs the module's address when D ADDR is asserted. Similarly, the next section, the G multiplexer, outputs the module's generic code if the GBIT is asserted. The output of the G multiplexer then goes to the D-bus input gate where it is strobed onto the D-bus by the DI GATE signal.

Data Control Signals

Control signals for the above mentioned data paths are initiated by the program, resulting in the following typical control sequence. When the program calls for a DATAI from one of the module's four addresses, the IOCM starts a D-bus Cycle and causes the address to be put on the D-bus. The module's address decoder decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the multiplexer control to produce the AØ and Al signals for selection of the correct data byte by the input multiplexer. At this time MY ADDRESS is also produced. After a short delay, D DIN is asserted by the IOCM and ANDed with MY ADDRESS to give DI GATE which strobes the data onto the D-bus. DI GATE also produces D RPLY after a short delay to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated, causing DI GATE to negate and remove data from the D-bus.

If the processor reads the IAR in response to an interrupt from this module, a Modified D-bus Cycle is initiated by the IOCM. In this case, there is no D SYNC signal, but D ADDR occurs and causes the IAR multiplexer to output one of the module's addresses instead of data.

Interrupt Control Signals

If one of the field inputs changes state, a one is produced in the COS register corresponding to that bit. If that bit has been selected as an interrupting bit by one of the interrupt enable switches, it provides an input to the interrupt control section. This section produces a flag signal that results in a processor interrupt if all priority requirements are met. (The flag signal is an input to the INTR IN, INTR OUT daisy chain.) When the interrupt occurs, a Modified D-bus Cycle is initiated by the IOCM. As previously stated, this results in the D ADDR signal which selects the address input to the IAR multiplexer and causes the interrupt control section to produce A SET which results in MY ADDRESS. When D DIN is asserted, the module's address is put on the D-bus.

At this point the processor has identified the interrupting address. The appropriate interrupt service routine is then executed. If now the processor RIFs the module (reads the interrupting data address or the corresponding COS register with R=1 in the CSR), the interrupt control section resets the COS register to all zeros.

Address and Flag Selection
The four module addresses must be assigned according to the rules stated in Chapter 4. They are selected on the module by the 8-pole switch, E48 (Figure 6-3-2). To illustrate the use of this switch one possible address selection is shown in Figure 6-3-3. Interrupt enable selection for any or all of the 16 module inputs is provided by switch modules E24 and E28 for the low and high bytes respectively. The relationship of field signal numbers to switch numbers is shown in Figure 6-3-2.

Address Format
The module's four data addresses, as determined by the two least significant bits of the address word, are as follows.

Y1	Y0	Data (octal)
0	0	Field 00-07
0	1	Field 10-17
1	0	COS register 00-07
1	1	COS register 10-17

Generic Code
The generic code for the M5011 module is octal 121.

Pin Connections
The M5011 pin connections for J1, the I/O cable connector, are shown in Table 6-3-1.

Application Notes

1. If unused inputs of an M5011 are left open circuited, they can be influenced by external noise. The random switching of these inputs could be a cause of confusion to the application program. It is, therefore, always good practice to tie these unused inputs high (a logic zero).

2. When used for contact closure detection, a pull-up at the user end of the field wire prevents the field wire from acting like an antenna.

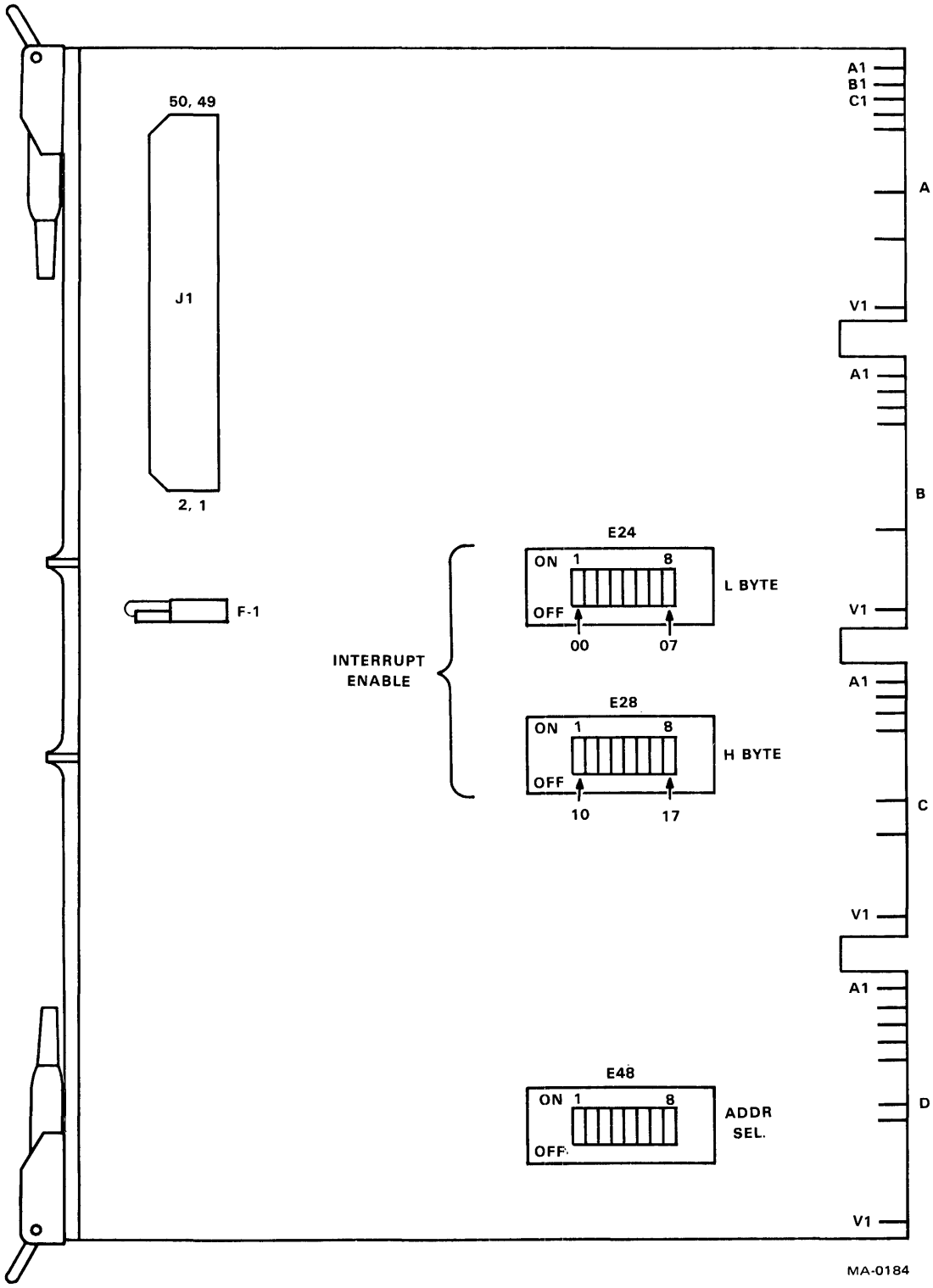


Figure 6-3-2 M5011 16-Bit COS Input

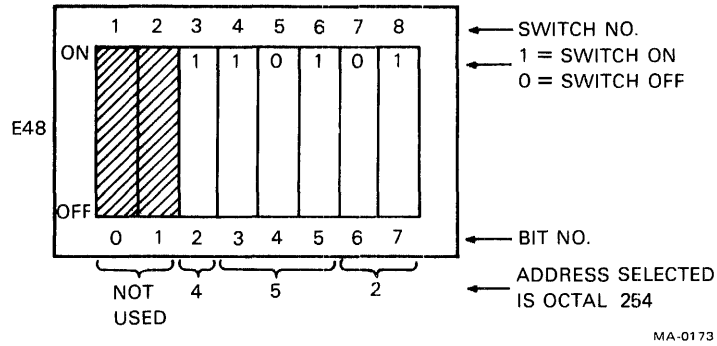


Figure 6-3-3 Address Selection Switch

Table 6-3-1 Module M5011 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	ØØ	2	Ø1
3	Ø2	4	Ø3
5	Ø4	6	Ø5
7	Ø6	8	Ø7
9	1Ø	1Ø	11
11	12	12	13
13	14	14	15
15	16	16	17
17	Common	18	Common
19	↑	2Ø	↑
21	|	22	|
23	|	24	|
25	|	26	|
27	|	28	|
29	|	3Ø	|
31	|	32	|
33	Common	34	Common
35		36	
37		38	
39		4Ø	
41		42	
43		44	
45		46	
47		48	
49		5Ø	

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc
Operating current	61 mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 37 mA maximum
Backup supply: 24 mA maximum

Standby current (backup supply)	24 mA maximum

Input Characteristics

Positive input voltage	+55 V maximum
Negative input voltage	-3Ø V maximum
Common mode input voltage	Ø V maximum
Logic zero threshold	8.2 V typical 12 V maximum
Logic one threshold	3.8 V typical 1.4 V minimum
Hysteresis	4.3 V typical
Input currents	When input = Ø V Ø.47 mA typical Ø.73 mA maximum When input = -3Ø V 2 mA typical 2.7 mA maximum When input = +55 V Ø.Ø5 microamp typical 5Ø microamp maximum
Propagation delay	5.5 microseconds maximum
Fuse	62.5 mA

Physical Characteristics	
Dimensions	Quad module, single width, 8-1/2 inch length
Field connector	Cable type BC40A or customer-supplied, 50-pin Berg
Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degrees C ambient
Heat dissipation	0.759 Btu/hr maximum due to module circuitry; 5.91 Btu/hr maximum due to field inputs

FUNCTIONAL DESCRIPTION

The M5Ø12 is an isolated dc input module used for monitoring voltages where noise immunity or common mode rejection is important. Interrupt capability on a per-byte basis is also provided. The module accepts up to 16 inputs, all optically isolated, structured as two 8-bit bytes, and sends them under program control to the D-bus. Provision is also made for program-controlled testing, input disabling, and reading the module's generic code. The module also features address and interrupt enable switches and individual input indicators.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-4-1 shows that field data entering through J1 is addressed and controlled by signals from the D-bus interface connector and ultimately output to the D-bus. Also shown is the interrupt control circuitry, which provides the option of the module initiating a processor interrupt when two of the inputs change. Data paths and their control are discussed below.

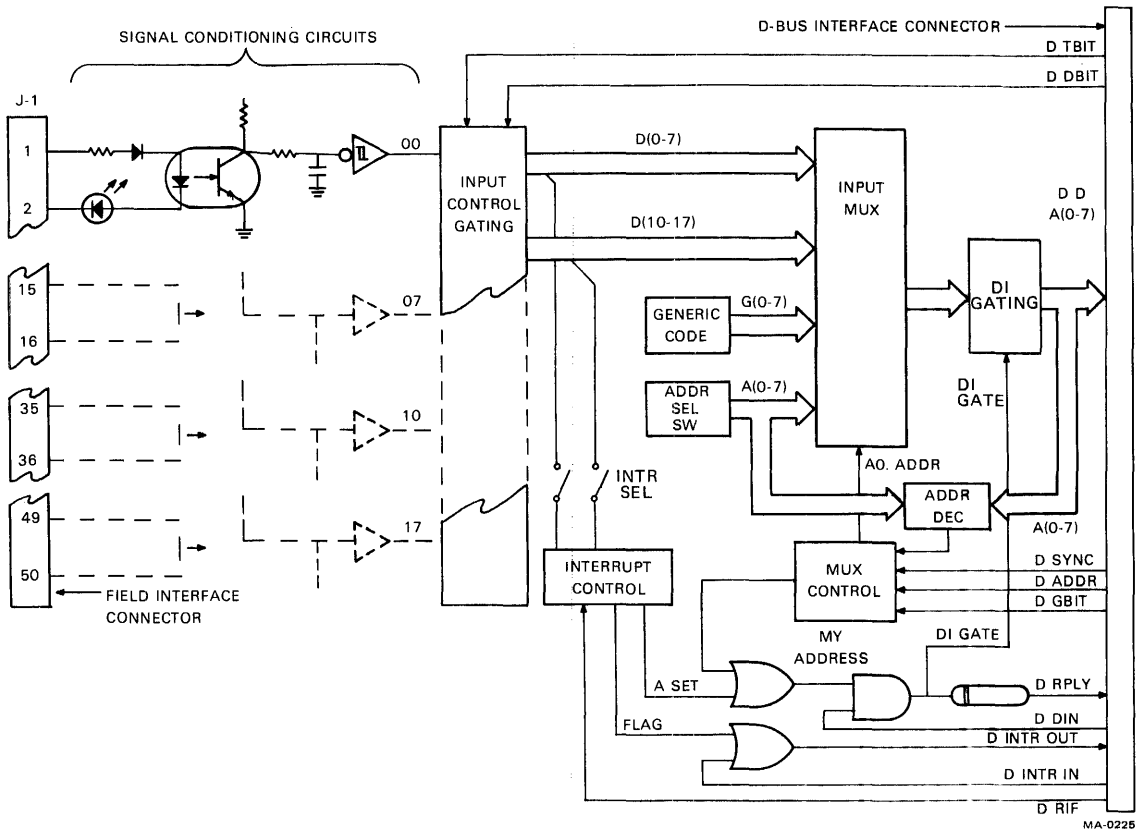


Figure 6-4-1 Module M5Ø12, 16-Bit Isolated DC Input Module, Simplified Block Diagram

Data Paths

Each of the 16 field inputs entering at J1 has a LED circuit that indicates input circuit activity. Each input also goes through an optical isolator that isolates the I/O Subsystem from noise or common mode voltages while allowing transmission of the desired dc signal. Following each isolator is a low pass filter for high frequency noise immunity and a Schmitt trigger which further improves noise immunity.

The 16 field signals from the output side of the Schmitt triggers go to the input gating section where they are separated into two 8-bit bytes. This section also receives two control inputs from the D-bus interface connector: TBIT and DBIT, which under program control, may modify the data for testing. The output of this section is normal data if these controls are not asserted. If the program causes TBIT to be asserted, the data output is inverted. If DBIT is asserted, the output is disabled and is read as all zeros. If both TBIT and DBIT are asserted the output is all ones.

The input multiplexer receives the two data bytes from the input gating section, plus the module's generic code and the address selection byte. This section is controlled by signals from the multiplexer control section and provides normal data out if: one of the module's two data bytes is selected; the modules's identity code if the GBIT signal is asserted; or one of the module's addresses if the D ADDR signal is asserted. The selected byte goes to the DI gating section where it is strobed onto the D-bus by the DI GATE signal.

Data Control Signals

Control signals for the above mentioned data paths are initiated by the program, resulting in the following typical control sequence. When the program calls for a DATAI from one of the module's two addresses, the IOCM starts a D-bus Cycle and causes the address to be put on the D-bus. The module's address decoder decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the multiplexer control to produce the AØ signal for the selection of the correct data byte by the input multiplexer. At this time MY ADDRESS is also produced. After a short delay, D DIN is asserted by the IOCM and ANDed with MY ADDRESS to give DI GATE which strobes the data onto the D-bus. DI GATE also produces D RPLY after a short delay to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated causing DI GATE to negate and remove data from the D-bus.

If the processor reads the IAR in response to an interrupt from this module, a Modified D-bus Cycle is initiated by the IOCM. In this case, there is no D SYNC signal but D ADDR occurs and causes the input multiplexer to output one of the module's addresses instead of data.

Interrupt Control Signals
If one of the interrupting field inputs (bit Ø7 or 17) changes state, a pulse is produced by the COS circuit corresponding to that bit. If that bit has been selected as an interrupting bit by one of the interrupt enable switches, it provides an input to the interrupt control section. This section produces a flag signal that results in a processor interrupt if all priority requirements are met. (The flag signal is an input to the INTR IN, INTR OUT daisy chain.)

When the interrupt occurs, a Modified D-bus Cycle is initiated by the IOCM. This results in the D ADDR signal which sets up the input multiplexer for address out and causes the interrupt control section to produce A SET which results in MY ADDRESS. When D DIN is asserted, the module's address is put on the D-bus.

At this point the processor has identified the interrupting address. The appropriate interrupt service routine is then executed. If now the processor RIFs the module (reads the interrupting address with R=1 in the CSR), the interrupt control section resets the flag.

Address Selection and Interrupt Enable
The two module addresses must be assigned according to the rules stated in Chapter 4. They are selected on the module via the 1Ø-pole switch in location E5Ø (Figure 6-4-2). Part of this switch is also used for enabling interrupts. To illustrate the use of this switch one possible combination of address and interrupt enable selection is shown in Figure 6-4-3.

Generic Code
The generic code for the M5Ø12 module is octal 122.

Pin Connections
The M5Ø12 module pin connections for J1, the I/O cable connector, are shown in Table 6-4-1.

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc $\pm$2 Vdc Backup supply: 14 Vdc $\geq$ VB $\geq$ (VS-Ø.7) Vdc
Operating current	14 mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 1Ø mA maximum
Backup supply: 4 mA maximum

Standby current (backup supply)	4 mA maximum

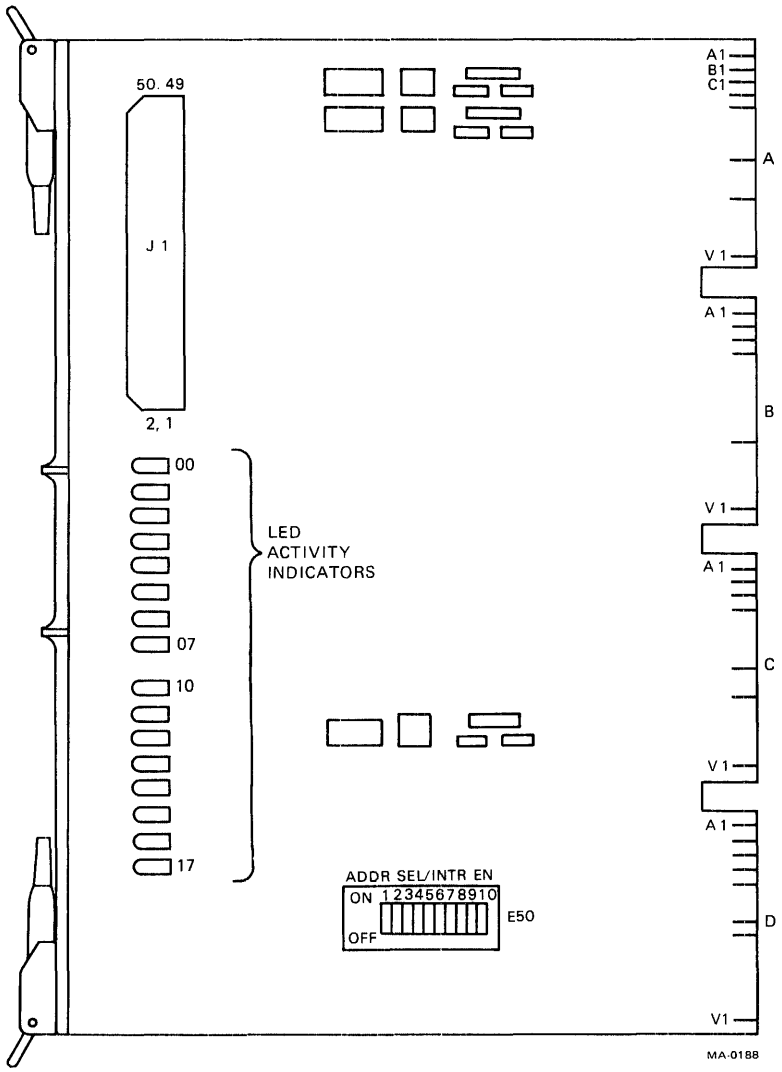


Figure 6-4-2 M5Ø12 16-Bit Isolated DC Input

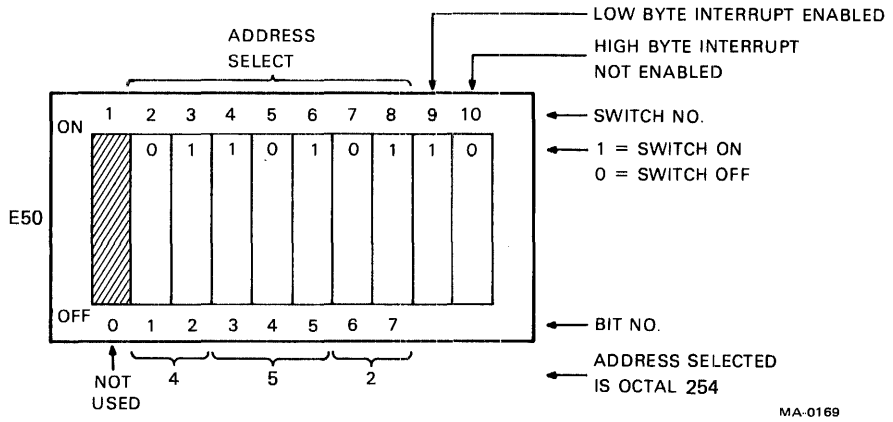


Figure 6-4-3 Address Selection and Interrupt Enable

Table 6-4-1 Module M5Ø12 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	ØØ+	2	ØØ-
3	Ø1+	4	Ø1-
5	Ø2+	6	Ø2-
7	Ø3+	8	Ø3-
9	Ø4+	1Ø	Ø4-
11	Ø5+	12	Ø5-
13	Ø6+	14	Ø6-
15	Ø7+	16	Ø7-
17		18	
19		2Ø	
21		22	
23		24	
25	Not	26	Not
27	Used	28	Used
29		3Ø	
31		32	
33		34	
35	1Ø+	36	1Ø-
37	11+	38	11-
39	12+	4Ø	12-
41	13+	42	13-
43	14+	44	14-
45	15+	46	15-
47	16+	48	16-
49	17+	5Ø	17-

Input Characteristics

Differential input voltage	55 V maximum
Logic zero threshold	5.1 V typical 3.86 V minimum
Logic one threshold	5.65 V typical 8.35 V maximum
Isolation voltage (between inputs or from inputs to ground)	1ØØØ V
Common mode source	2ØØ VA
Hysteresis	Ø.55 V typical

Input currents	When input = +12 V differential 2.55 mA typical When input = +55 V differential 20.1 mA maximum When input = -12 V differential 0.05 microamp typical 50 microamp maximum
Propagation delay	2.5 ms typical 6.2 ms maximum
Physical Characteristics	
Dimensions	Quad module, single width, 8-1/2 inch length
Field connector	Cable type BC40A or customer-supplied, 50-pin Berg
	NOTE **Two 8-position jumper strips are provided with the BC40A screw terminal assembly. These allow the user to connect the plus or minus inputs together, in 8-input groups, to facilitate field wiring when a common field power source is used.**
Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degrees C ambient
Heat dissipation	0.643 Btu/hr maximum due to module circuitry 60.72 Btu/hr maximum due to field inputs

FUNCTIONAL DESCRIPTION

The M5Ø12-YA is an isolated dc input module used for monitoring open collector TTL signals. Interrupt capability on a per byte basis is provided. The module accepts up to 16 inputs, all optically isolated, structured as two 8-bit bytes, and sends them under program control to the D-bus. Provision is made for program-controlled testing, input disabling, and reading the module's generic code. The module also features address and interrupt enable switches.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-5-1 shows that field data entering through J1 is addressed and controlled by signals from the D-bus interface connector and ultimately output to the D-bus. Also shown is the interrupt control circuitry, which provides the option of the module initiating a processor interrupt when two of the inputs change. Data paths and their control are discussed below.

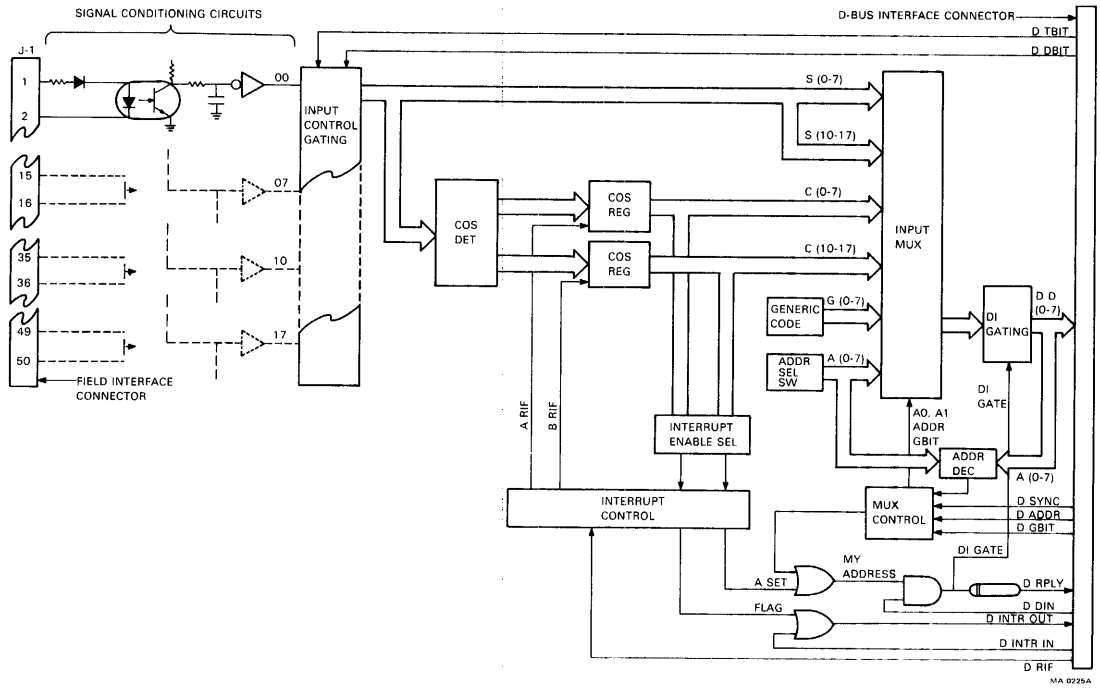


Figure 6-5-1 M5Ø12-YA 16-Bit TTL Compatible Input Module, Block Diagram

Data Paths
Field signals are input to the module through J1. There is a positive and a negative terminal for each input. The positive terminal of each input must be connected to a customer supplied power source. The negative terminal is connected to a TTL switching device.

Each of the 16 TTL field inputs entering at J1 goes through an optical isolator. The isolator is followed by a low-pass filter for high frequency noise immunity, and a Schmitt trigger. The 16 field signals from the output side of the Schmitt triggers go to the input gating section where they are separated into two 8-bit bytes. This section also receives two control inputs from the D-bus interface connector: TBIT and DBIT, which under program control can modify the data for testing. The output of this section is normal data if these controls are not asserted. If the program causes TBIT to be asserted, the data output is inverted. If DBIT is asserted, the output is disabled and is read as all zeros. If both TBIT and DBIT are asserted, the output is all ones.

The input multiplexer receives the two data bytes from the input gating section, plus the module's generic code and the address selection byte. This section is controlled by signals from the multiplexer control section and provides normal data out if one of the module's two data bytes is selected, the module's identity code if the GBIT signal is asserted, or one of the module's addresses if the D ADDR signal is asserted. The selected byte goes to the DI gating section where it is strobed onto the D-bus by the DI GATE signal.

Data Control Signals
Control signals for the previously mentioned data paths are initiated by the program, resulting in the following typical control sequence.

When the program calls for a DATAI from one of the module's two addresses, the IOCM starts a D-bus Cycle and causes the address to be put on the D-bus. The module's address decoder decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the multiplexer control to produce the A0 signal for the selection of the correct data byte by the input multiplexer. At this time MY ADDRESS is also produced. After a short delay, D DIN is asserted by the IOCM and ANDed with MY ADDRESS to give DI GATE, which strobes the data onto the D-bus. DI GATE also produces D RPLY after a short delay to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated causing DI GATE to negate and remove data from the D-bus.

If the processor reads the IAR in response to an interrupt from this module, a Modified D-bus Cycle is initiated by the IOCM. In this case, there is no D SYNC signal, but D ADDR occurs and causes the input multiplexer to output one of the module's addresses instead of data.

Interrupt Control Signals
If one of the interrupting field inputs (bit Ø7 or 17) changes state, a pulse is produced by the COS circuit corresponding to that bit. If that bit has been selected as an interrupting bit by one of the interrupt enable switches, it provides an input to the interrupt control section. This section produces a flag signal that results in a processor interrupt if all priority requirements are met. (The flag signal is an input to the INTR IN, INTR OUT daisy chain.)

When the interrupt occurs, a Modified D-bus Cycle is initiated by the IOCM. This results in the D ADDR signal that sets up the input multiplexer for address out and causes the interrupt control section to produce A SET, which results in MY ADDRESS. When D DIN is asserted, the module's address is put on the D-bus.

At this point the processor has identified the interrupting address. The appropriate interrupt service routine is then executed. If now the processor RIFs the module (reads the interrupting address with R=1 in the CSR), the interrupt control section resets the flag.

Address Selection and Interrupt Enable
The two module addresses must be assigned according to the rules stated in Chapter 4. They are selected on the module via the 1Ø-pole switch in location E5Ø (Figure 6-5-2). Part of this switch is also used for enabling interrupts. To illustrate the use of this switch one possible combination of address and interrupt enable selection is shown in Figure 6-5-3.

Generic Code
The generic code for the M5Ø12-YA module is octal 123.

Pin Connections
The M5Ø12-YA module pin connections for J1, the I/O cable connector, are shown in Table 6-5-1.

Application Information
The positive terminal of each input must be connected to a +5 Vdc source (not to exceed +7 Vdc). The negative terminal is connected to a TTL switching device. This should be an open collector driver, but it can also be a totem pole TTL output. An input is defined as a logical one if the input voltage is less than +Ø.8 V, and as a logical zero if the input current is less than 25Ø microamps.

Field connections for the M5Ø12-YA may be implemented with the BC4ØA screw terminal assembly. A typical interface is shown in Figure 6-5-4. Field wiring connected to the screw terminals is interfaced to the module via a cable provided with the screw terminal assembly. Field power connections may be commoned on a per-byte basis via the eight-position jumper strips provided with the BC4ØA. Note that the +5 V power supply shown must be furnished by the customer.

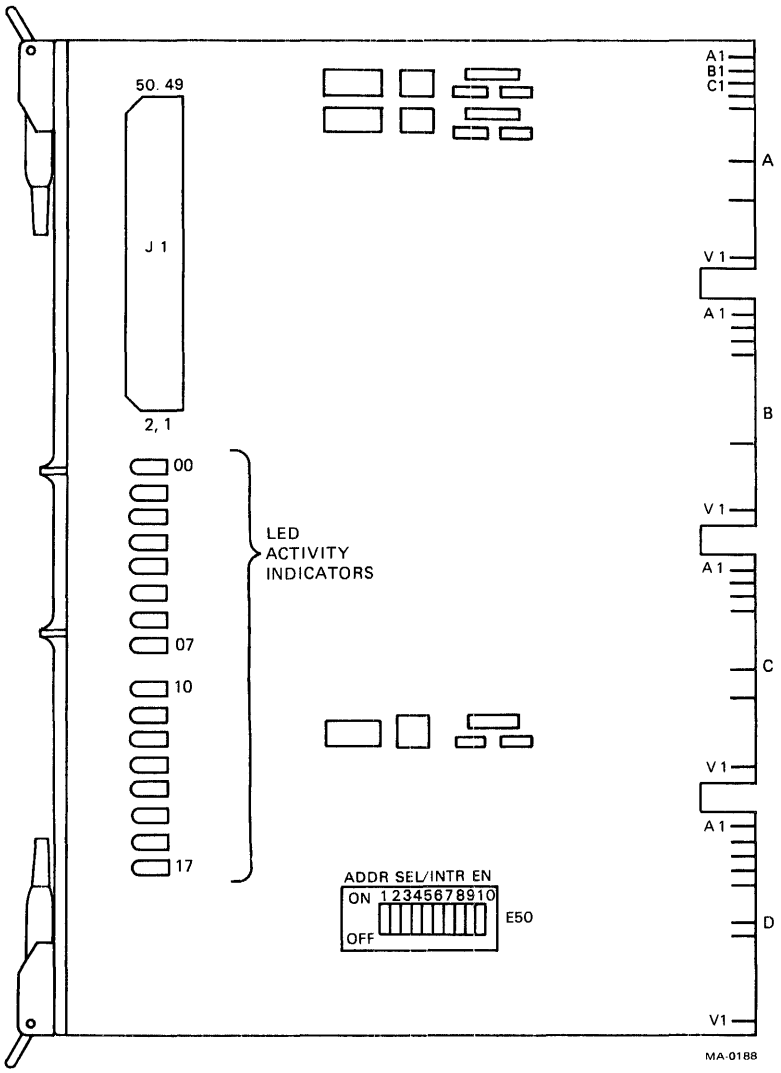


Figure 6-5-2 M5Ø12-YA 16-Bit TTL Compatible Input Module

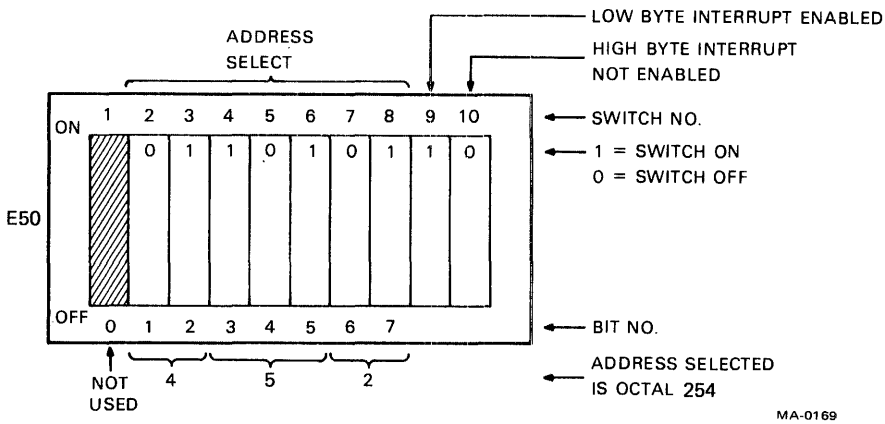


Figure 6-5-3 M5Ø12-YA Address Selection and Interrupt Enable Switch

Table 6-5-1 Module M5Ø12-YA I/O Pin Connections

Module I/O Connector Pin	Field I/O		Module I/O Connector Pin	Field I/O	
1	ØØ+		2	ØØ-	
3	Ø1+		4	Ø1-	
5	Ø2+		6	Ø2-	
7	Ø3+		8	Ø3-	TTL
9	Ø4+	To +5 V	1Ø	Ø4-	Driver
11	Ø5+	Supply	12	Ø5-	Inputs
13	Ø6+	*	14	Ø6-	
15	Ø7+		16	Ø7-	
17			18		
19			2Ø		
21			22		
23			24		
25	Not		26	Not	
27	Used		28	Used	
29			3Ø		
31			32		
33			34		
35	1Ø+		36	1Ø-	
37	11+		38	11-	
39	12+	To +5 V	4Ø	12-	
41	13+	Supply	42	13-	TTL
43	14+	*	44	14-	Driver
45	15+		46	15-	Inputs
47	16+		48	16-	
49	17+		5Ø	17-	

*Customer provided

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS - Ø.7) Vdc
Operating current	8 mA maximum **NOTE** **If the backup supply is implemented, total operating current is shared.** **Main supply: 4.3 mA maximum** **Backup supply: 3.7 mA maximum**
Standby current (backup supply)	3.7 mA maximum

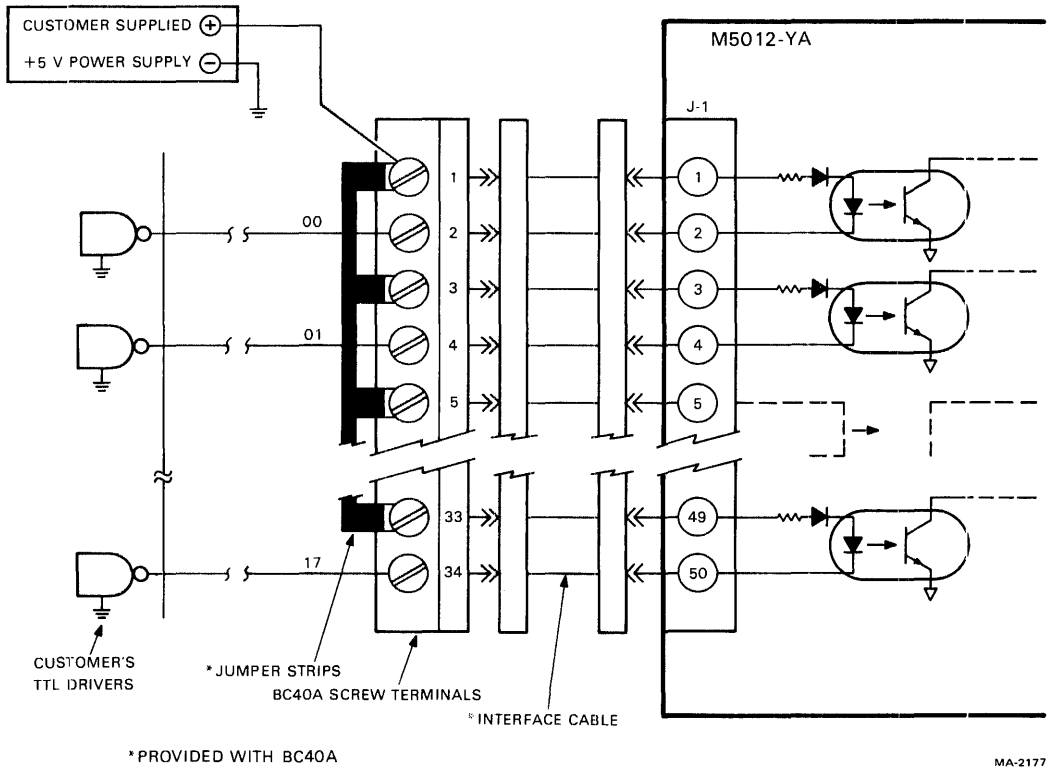


Figure 6-5-4 M5012-YA Typical TTL Field Interface

Input Characteristics

Connections	Positive terminal Operating: +5 Vdc, ±5 percent Absolute maximum: +7 Vdc Negative terminal Open collector or totem pole TTL driver
Input current (with +5 V supply)	3.2 mA maximum per input (2 TTL unit loads)
Logic levels	Logic one: $V_{in} \leq 0.8$ V Logic zero: $I_{in} \leq 250$ microamp
Isolation voltage	1000 V
Common mode source	200 VA
Propagation delay	Logic zero to logic one: 125 microseconds maximum Logic one to logic zero: 400 microseconds maximum

Physical Characteristics	
Dimensions	Quad module, single width, 8-1/2 inch length
Field connector	Cable type BC40A or customer-supplied 50-pin Berg connector
Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degrees C ambient
Heat dissipation	0.6 Btu/hr maximum due to module circuits; 1.1 Btu/hr maximum due to field inputs

FUNCTIONAL DESCRIPTION

The M5Ø13 is an ac input module used for monitoring ac voltage levels. An optional interrupt capability is also provided. The module accepts up to eight transformer isolated inputs and monitors their status. Provision is made for program-controlled testing, input disabling, and reading the module's generic code. The module also features an optional interrupt select switch, address selection switches, individual input indicators, and MOV input protection.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-6-1 shows that field data entering through J1 is addressed and controlled by signals from the D-bus interface connector and ultimately output as an 8-bit byte to the D-bus. Also shown is the interrupt selection and control circuitry which provides the option of the module initiating a processor interrupt when field input Ø7 changes state. The sequence of control and data flow is as follows.

Data Paths

The module provides status information for input circuits in the 9Ø-14Ø Vac range. Up to eight inputs can be monitored to determine their on or off conditions. Inputs less than 3Ø Vac are defined as off and those above 9Ø Vac as on.

The module block diagram and a typical field connection are shown in simplified form in Figure 6-6-1. As the figure shows, all inputs entering at J1 go through transformers which provide isolation from undesired field signals and also step down the field voltage. Each transformer primary has a series LED to indicate field circuit activity and a parallel metal oxide varistor (MOV) for overvoltage transient protection. A rectifier circuit and filter converts the secondary voltage to dc for input to the 555 threshold detector. The output of the A comparator is high whenever its input is above 5.6 Vdc, corresponding to a field input of 9Ø Vac or more. This resets flip-flop C providing a low output. The B comparator goes high when its input is below 2.8 Vdc, corresponding to a field input less than 3Ø Vac. When the B comparator goes high, it sets the C flip-flop providing a high output. The 555 output provides the CMOS logic levels necessary for the subsystem.

The threshold detector outputs go to the input control gating section which also receives two control inputs from the D-bus interface connector: DBIT and TBIT, which under program control may modify the data for testing. The output of this section is normal data if these controls are not asserted. If the program causes TBIT to be asserted, the output is inverted. If DBIT is asserted, the output is disabled and is read as all zeros. If both TBIT and DBIT are asserted, the output is all ones.

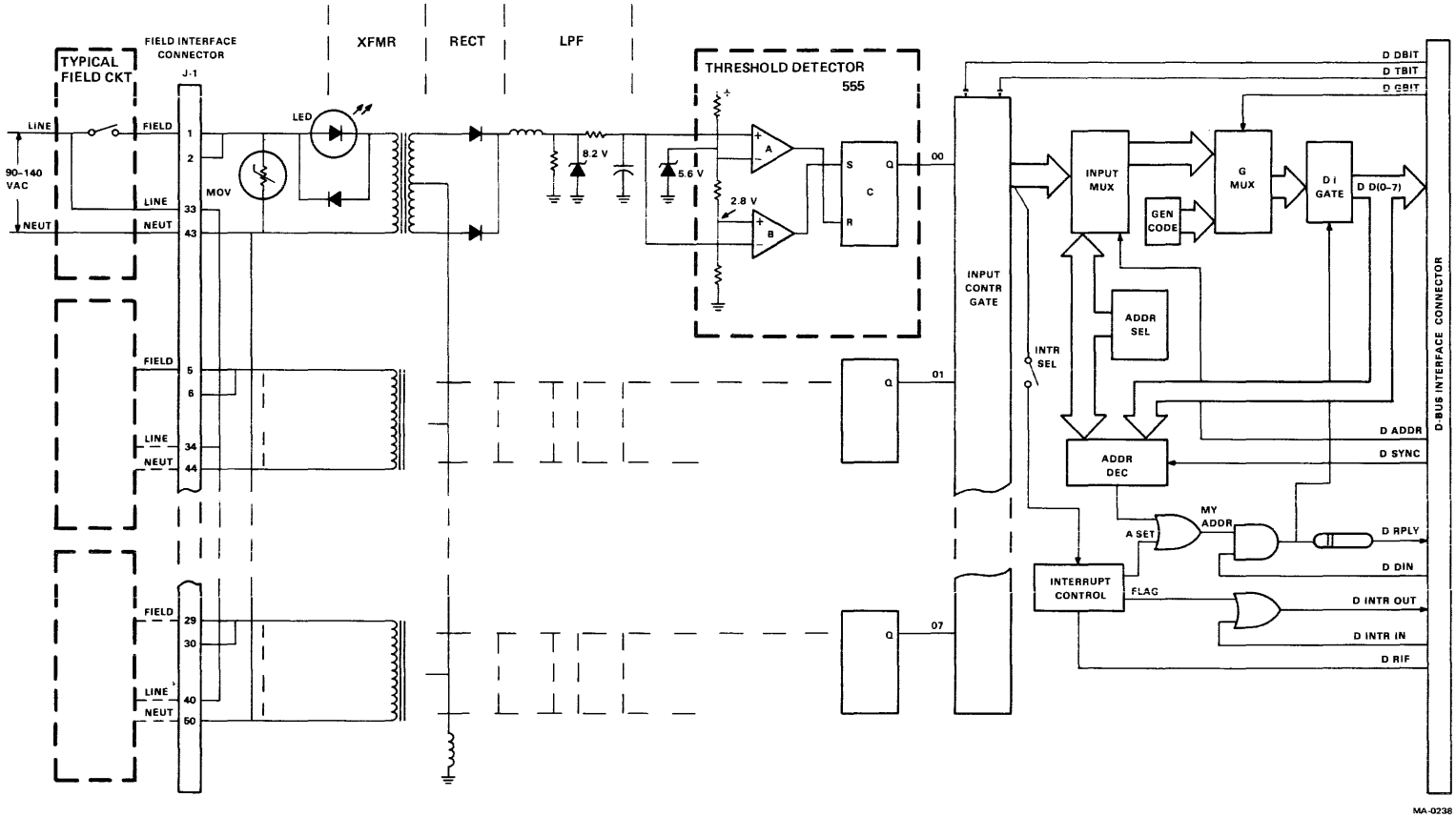


Figure 6-6-1 Module M5013 8-Bit AC Input
Simplified Block Diagram

The output of the control gating section then goes through the input multiplexer and the G multiplexer to the D-bus interface gating where it is strobed onto the D-bus by the DI GATE signal. If either the D ADDR or D GBIT signals are asserted, the output is either the module's address or its identity code, respectively.

Data Control Signals

Control signals for the above mentioned data paths are initiated by the program, resulting in the following typical control sequence. When the program calls for a DATAI from the module's address, the IOCM starts a D-bus Cycle and causes the address to be put on the D-bus. The module's address decoder decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the MY ADDRESS signal to be produced. After a short delay, D DIN is asserted by the IOCM and ANDed with MY ADDRESS to produce DI GATE which strobes the data onto the D-bus. DI GATE also produces D RPLY after a short delay to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated, causing DI GATE to negate and remove data from the D-bus.

If the processor reads the IAR in response to an interrupt from this module, a modified D-bus Cycle is initiated by the IOCM. In this case there is no D SYNC signal but D ADDR occurs and causes the input multiplexer to output the module's address instead of data.

Interrupt Control Signals

If the field input Ø7 changes state, and the interrupt option selection switch is in the on position, the interrupt control section produces a flag signal. If all priority requirements are met, the flag signal results in a processor interrupt. (The flag signal is an input to the INTR IN, INTR OUT daisy chain.) When the interrupt occurs, a Modified D-bus Cycle is initiated by the IOCM. This results in the D ADDR signal which selects the address input of the input multiplexer and causes the interrupt control section to produce A SET which results in MY ADDRESS. When D DIN is asserted, the module's address is put on the D-bus.

At this point the processor has identified the interrupting address. The appropriate interrupt service routine is then executed. If now the processor RIFs the module (reads the module's address with R=1 in the CSR), the interrupt control section resets the module's flag flip-flop.

Address and Interrupt Selection

The module data address must be assigned according to the rules stated in Chapter 4. It is selected on the module by the first eight switches of the 1Ø-pole switch in location E9 (Figure 6-6-2). An example of one possible address selection is shown in Figure 6-6-3 to illustrate the use of this switch. The ninth switch on this module is used to select the interrupt option.

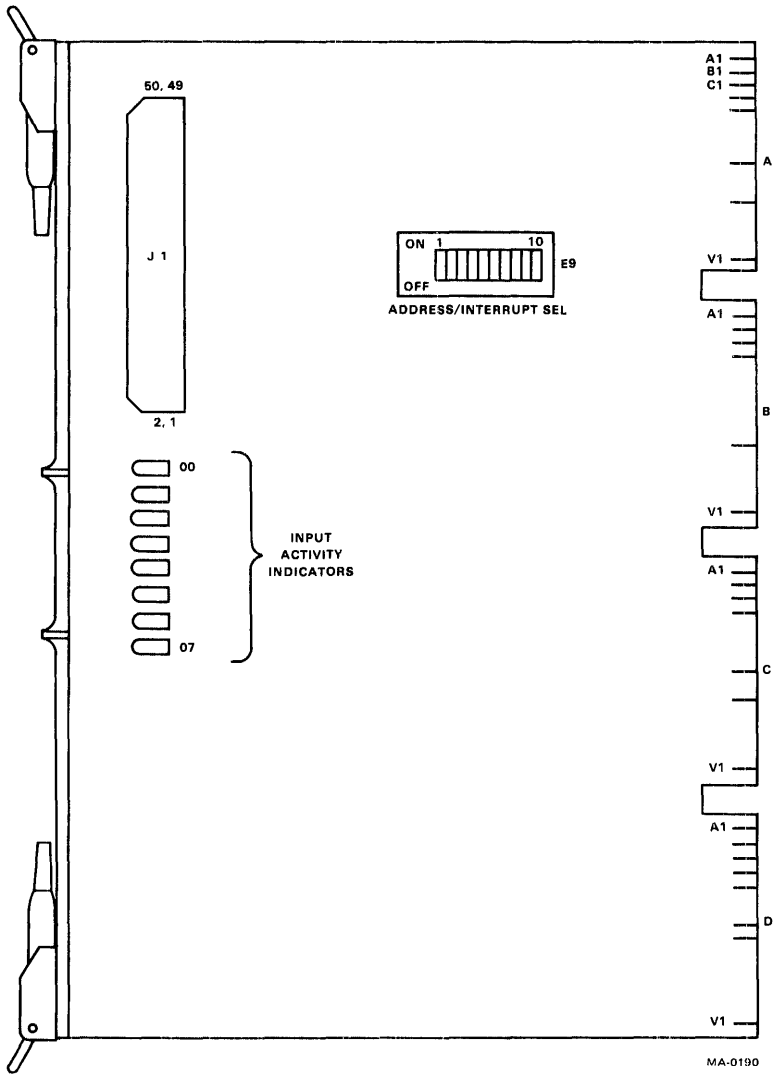


Figure 6-6-2 M5013 AC Input Module

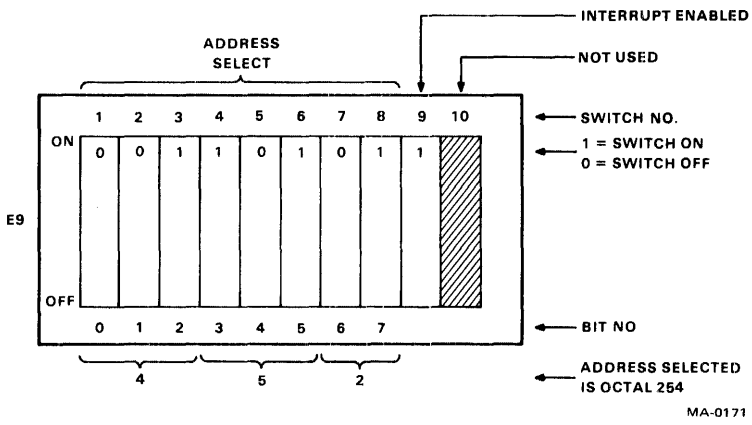


Figure 6-6-3 Address Selection and Interrupt Enable

Generic Code
The generic code for the M5Ø13 module is octal 1Ø1.

Pin Connections
The M5Ø13 module pin connections for J1, the I/O cable connector, are shown in Table 6-6-1.

Table 6-6-1 Module M5Ø13 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	ØØ	2	ØØ
3		4	
5	Ø1	6	Ø1
7		8	
9	Ø2	1Ø	Ø2
11		12	
13	Ø3	14	Ø3
15		16	
17	Ø4	18	Ø4
19		2Ø	
21	Ø5	22	Ø5
23		24	
25	Ø6	26	Ø6
27		28	
29	Ø7	3Ø	Ø7
31		32	
33, 35, 37, 39	Field ac line	34, 36, 38, 4Ø	Field ac line
41		42	
43, 45, 47, 49	Field ac neutral	44, 46, 48, 5Ø	Field ac neutral

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≤ (VS-Ø.7) Vdc
Operating current	146 mA maximum

NOTE
If the backup supply is implemented total operating current is shared.
Main supply: 133 mA maximum
Backup supply: 13 mA maximum

Standby current (backup supply)	13 mA maximum

Input Characteristics

Input line voltage	9Ø-14Ø Vac @ 47-63 Hz = logic 1 Ø-3Ø Vac @ 47-63 Hz = logic Ø
Input current	9.3 mA minimum @ 9Ø Vac minimum 25 mA maximum @ 14Ø Vac maximum
Turn-on time	8-2Ø ms @ 6Ø Hz 8-22 ms @ 5Ø Hz
Turn-off time	5-14 ms @ 5Ø-6Ø Hz
Contact resistance	Input remains in the logic Ø state with 22K in series with 12Ø Vac input
Isolation voltage	15ØØ Vrms from inputs to ground (Inputs are not isolated from each other)
Protection	MOV over-voltage transient protection of all inputs

Physical Characteristics

Dimensions	Quad module, triple width, 8-1/2 inch length
Field connector	Cable type BC4ØB or customer-supplied, 5Ø-pin Berg

Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degree C ambient
Heat dissipation	6.71 Btu/hr maximum due to module circuits; 92.4 Btu/hr maximum due to field inputs

FUNCTIONAL DESCRIPTION

The M5Ø14 input module contains two independent 16-bit counters. Each counter is a presettable up counter with internally generated frequency and time bases. Inputs may be isolated or nonisolated, low level, high level, or TTL. Typical applications include frequency measurement (e.g., RPM and flow meter), event counting, and pulse width measurement. Each counter has several switches that allow the selection of alternate time bases, input configurations, counting modes, and interrupt modes. Provision is made for program controlled testing, input and output disabling, and reading the module's generic code. Other features include LED input status indicators, fuse protection, and an address selection switch.

GENERAL DESCRIPTION

The M5Ø14 consists of two independent counters with a common D-bus interface. Figure 6-7-1 is a simplified block diagram of the module. Each counter receives X and Y inputs from field connector (J31) that are used singly or in combination depending on the application. Each counter has nine programming switches for selection of its input circuit configuration. A common generator produces the necessary frequency and time bases for both counters. Besides the field inputs, the figure also shows data inputs to the counters from the D-bus. This allows presetting the counters to any desired starting point. Presetting to zero allows 65,535 events to be counted. Output data from the counters is interfaced to the D-bus via a multiplexer.

DETAILED DESCRIPTION

The module consists of two printed circuit boards assembled in a mother-daughter configuration (Figure 6-7-2). The heavy dashed line in Figure 6-7-1 shows how the module's circuits are divided between the two circuit boards. The mother board (G67Ø) contains the counters, data paths, and interrupt logic. The daughter board (54-13585) contains input signal conditioning, counter control, and frequency and time bases.

Mother Board

The mother board is a multipurpose circuit board with circuits that are not used in the M5Ø14. One of these circuits is the self-test circuit used for factory testing the mother board when no daughter board is present. This circuit includes two gates in the interrupt logic which permit the counters to generate interrupts when they decrement to zero. The test circuit is disabled when the daughter board is present; the daughter board then controls all count and interrupt functions.

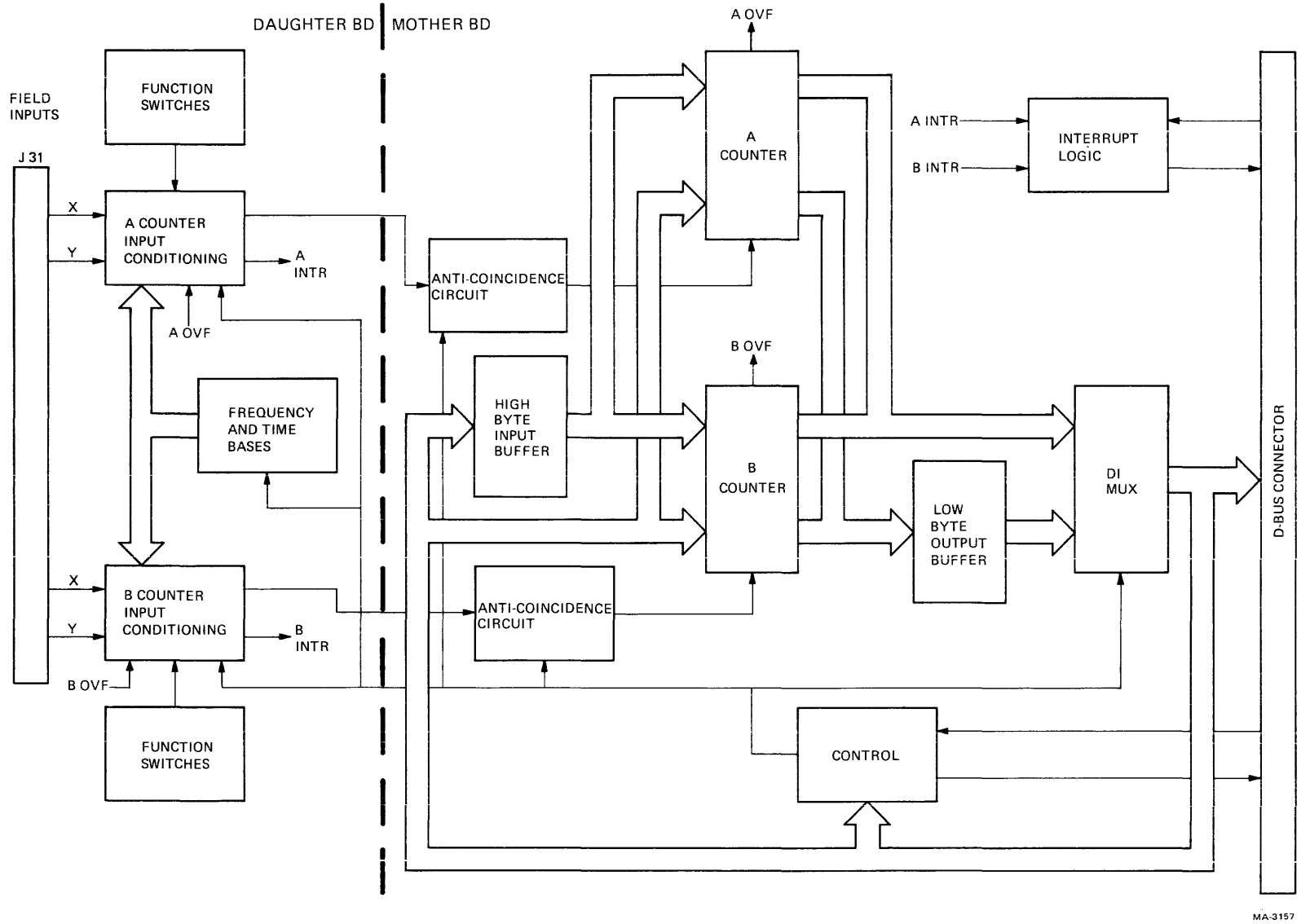


Figure 6-7-1 M5014 Counter Module, Block Diagram

In addition to the test circuit, each of the 16-bit counters has an extra flip-flop associated with its most significant bit. In the M5Ø14, this flip-flop is held reset and the counter operates as a 16-bit up counter. In the M6Ø14, which also uses the G67Ø, the MSB is always zero and the counter operates as a 15-bit down counter. The MSB from the bus is routed through the extra flip-flop which operates as the sign or direction bit of the M6Ø14.

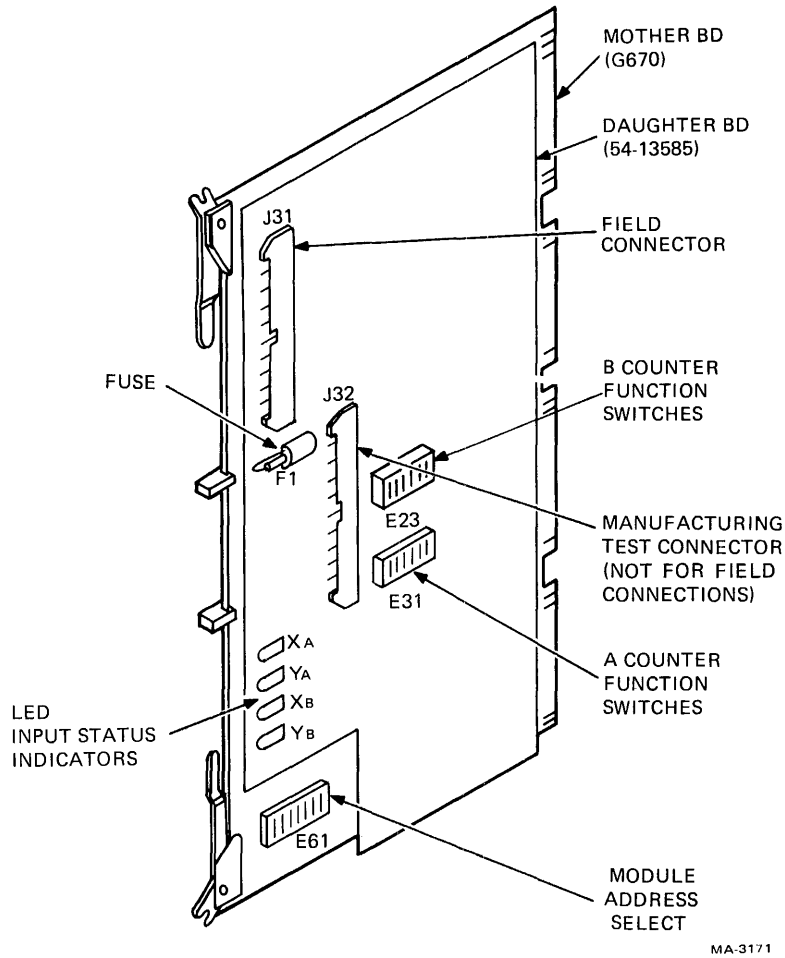


Figure 6-7-2 M5Ø14 Counter Module

Finally, the generic code circuit is capable of generating generic codes Ø44-Ø47 and 144-147. The least significant digit is chosen independently for the two counters by the daughter board. The M6Ø14 always provides generic code Ø44 for either counter. The M5Ø14 generates codes 144-147 independently for each counter.

Data Paths

The data paths of the mother board resemble those of other four-address D-bus modules with the following exceptions.

1. A set of gates in the input data path momentarily inhibits the bus data and forces the internal data lines to zero when the module is initialized. These gates are necessary because the counters can be cleared only by loading them with zeros. Upon assertion of D INIT, or at the beginning of D TBIT assertion, wide and narrow initialize signals are generated that respectively zero the data lines, and load the counters.

2. An input buffer is necessary for the high byte because 16 parallel bits must be loaded into the counters from an 8-bit bus. When the program wants to load one of the counters, it must write the high byte first. This data is stored in the common input buffer until the low byte is written, at which time both the buffered high byte and the low byte data are loaded into the counter.

3. An output buffer is necessary for the low byte to prevent data seen by the program from being changed between the readings of the high and low bytes, even though the counter itself may have changed. When the high byte of either counter is selected and read directly onto the D-bus, the corresponding low byte is loaded into the common output buffer for retrieval by a later instruction. Therefore, both bytes represent data at the same point in time.

4. The module has only one input and one output buffer which are shared by the two counters.

5. In the M6Ø14, the MSB of each counter is routed around the counter to the sign/direction flip-flop.

Anticoincidence Circuit

Each counter has an anticoincidence circuit that prevents counting during the reading of the high byte and storage of the low byte by a DATAI. It also delays these reading and storage operations, allowing the necessary data settling time that would be required if a count had occurred immediately prior to the DATAI. A simplified anticoincidence circuit and its timing are shown in Figures 6-7-3 and 6-7-4.

The circuit (Figure 6-7-3) consists of an analog switch, a decoder, and two delays. The purpose of the analog switch is to

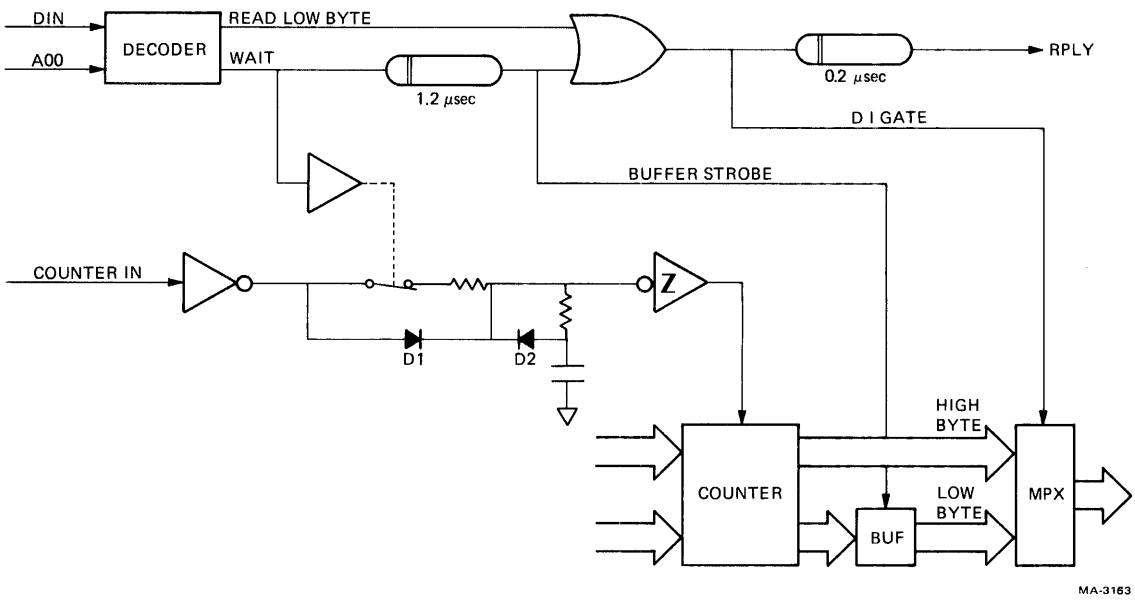


Figure 6-7-3 Anticoincidence Circuit

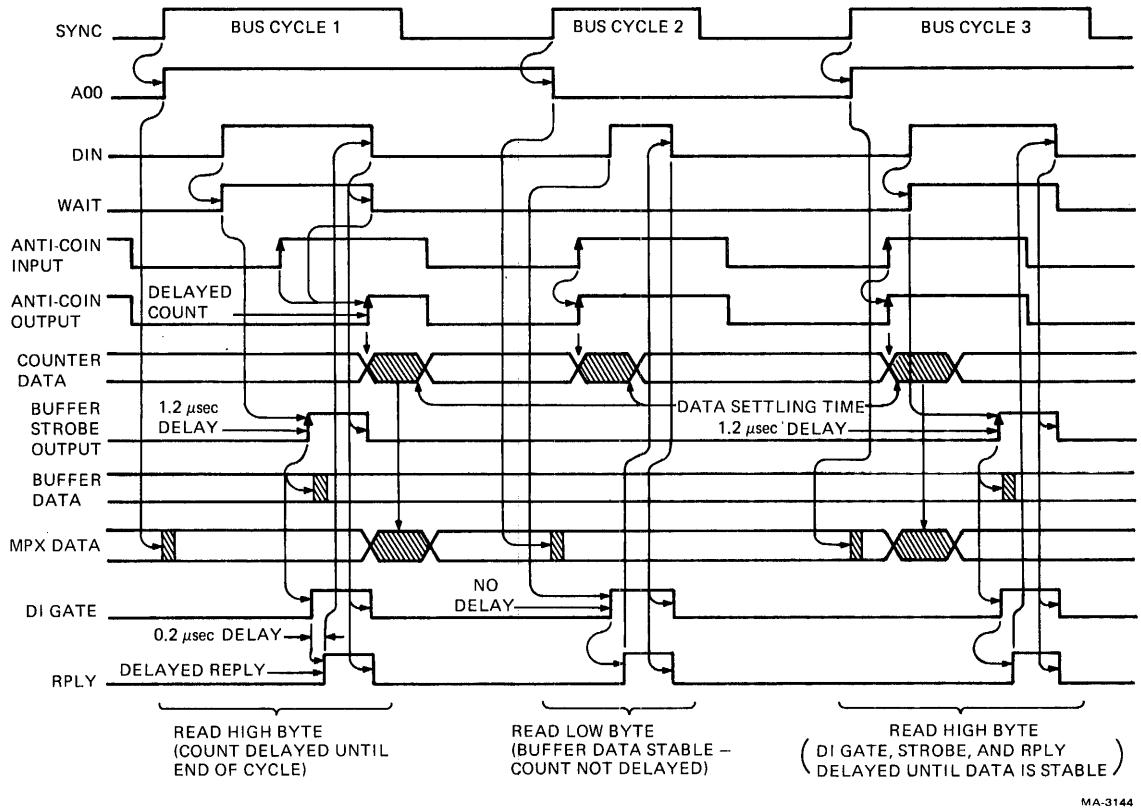


Figure 6-7-4 Anticoincidence Timing

disconnect the input to the counter (WAIT) while it is being read. When the input is disconnected, the voltage at the input of the Schmitt trigger (second inverter) is retained on the capacitor. Diode D1 removes the effect of an open switch upon the negative transition of COUNTER IN, which is not of interest to the counter. Diode D2 improves the noise immunity of the circuit by pulling the Schmitt trigger voltage away from the threshold when the switch is opened.

The first function of the anticoincidence circuit is to delay the leading edge of the counter input signal for the entire input portion of the bus cycle. In the first bus cycle of Figure 6-7-4, the decoder detects a high byte DATAI (i.e., the address A00H and DINH). This produces the WAIT signal that opens the analog switch, delaying the counter input (anticoincidence output) until after the D-bus has received RPLY, accepted the data, and negated DIN. Stable data is guaranteed at the input of the buffer, at the leading edge of BUFFER STROBE, and on the bus during the assertion of RPLY.

The second function of the anticoincidence circuit is to delay RPLY from the module to ensure stable data if the counter has changed immediately prior to the DATAI. The third bus cycle of Figure 6-7-4 is similar to the first except that the counter has already received the leading edge of the anti-coincidence output. The 1.2 microseconds delay of Figure 6-7-3 delays BUFFER STROBE and RPLY until the buffer input data and multiplexer data are again stable.

The anticoincidence function is unnecessary when the low byte is being read (A01L AND DINH) because it is the buffer, not the counter, that is being read. Since this data is always stable (except when the high byte is read), the decoder does not issue a WAIT signal to the analog switch and the 1.2 microseconds delay is bypassed. This is shown in the second bus cycle of Figure 6-7-4. A 0.2 microseconds delay of RPLY always exists for normal bus deskewing requirements.

Daughter Board

When the G670 mother board is equipped with a daughter board, all counter control and interrupt stimuli originate on the daughter board. The M5014 input counter uses the 54-13585 daughter board and the counters on the mother board operate as 16-bit up counters. The daughter board monitors only the overflow line from each counter which is asserted when the counter reaches the all ones state. (MSB information from each counter is also available to the daughter board, but is not used in the M5014.)

The 54-13585 daughter board contains two identical input conditioning and control sections, and one frequency/time base source. The daughter board provides electrical interface, frequency and time bases, mode selection, and counter enabling for the module's field inputs.

Figure 6-7-5 is a block diagram of the 54-13585 daughter board showing X and Y inputs entering at the field connector (J31). Each of these inputs interfaces to the module via an electrical and logical interface circuit. The outputs of these circuits are equipped with LEDs for indicating the logical sense of the X and Y signals. The X and Y signals are combined with the outputs of the frequency and time base selection circuit in the mode logic section. Output of the mode logic section goes to the mode select circuit where the appropriate combination of signal and frequency or time base is selected.

The outputs of the mode select circuit are A SIG and A WINDOW; they are respectively the counter input and time base signals. A WINDOW is input to the counter enabling circuit. This circuit causes the next true portion of A WINDOW occurring after a write command to be output as A EN. Finally, A EN enables A SIG, producing A CNTR IN, the signal that is ultimately counted. Several inputs from the mother board shown in Figure 6-7-5 provide the following control functions.

1. TBIT and DBIT provide the test and disable functions as discussed below.

2. WRØ and WR1 are inputs to the A counter enabling circuit that respectively indicate that the counter is to be armed and readied to count, or that the count is to be aborted. WR2 and WR3 serve the same purposes for the B counter enabling circuit.

3. A OVF and B OVF are interrupt control signals for the A and B counters respectively; they occur when the counters reach the all ones state.

4. SYS CLOCK is used to derive all the module's frequency and time bases.

Counter enable outputs are provided at J31 for both counters. These signals enable the user to synchronize the counting interval with other process activities.

Nine function selector switches for each input conditioning and control section allow the user to select logical sense, frequency and time base, mode, and interrupt options.

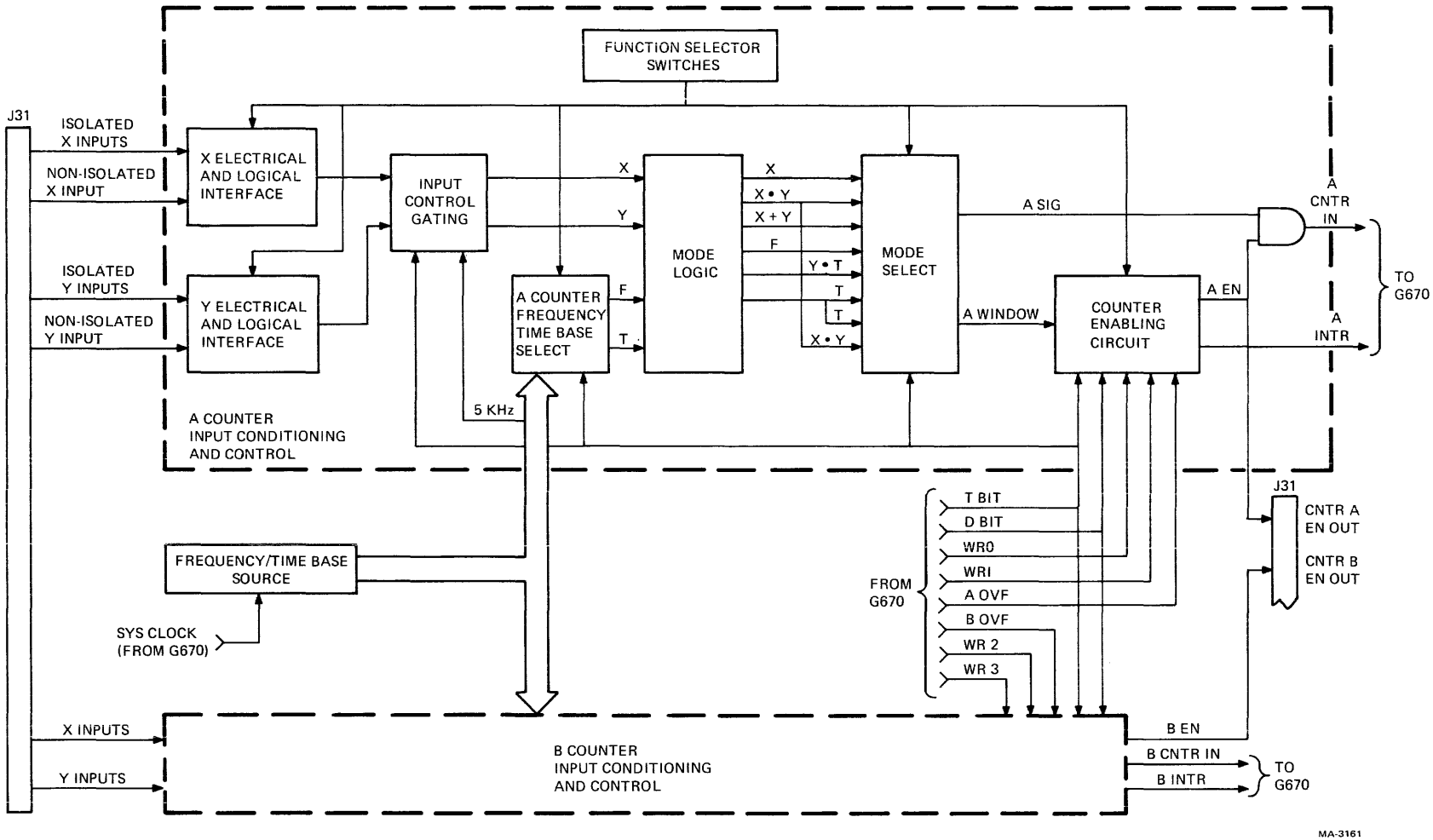


Figure 6-7-5 54-13585 Daughter Board Block Diagram

Electrical and Logical Interface Circuit

The module is equipped with four field input interface circuits; one for each input of each counter. These interfaces provide the user with several input options to accommodate varying field situations. Figure 6-7-6 shows some details of this circuit. Each X and Y input is capable of accepting isolated inputs of high or low levels, or nonisolated inputs of high or TTL levels. Specific applications are configured via function selector switches and a choice of input terminal options. The function selector switches shown in the figure as S1, S2, and S3 correspond to switches E31-1, E31-2, E31-3, E23-1, E23-2, and E23-3 for the A and B counters respectively. The proper use of these options enables the module to accept various combinations of X and Y inputs, even though they may differ in signal level, logical sense, or common mode voltage. Logical senses are independently selectable via switches S1 and S2. The TTL/HIGH LEVEL choice is made for both X and Y inputs of a given counter with S3. It should be noted that S3 affects only the nonisolated inputs. As the figure shows, isolated inputs use separate input terminals to accommodate different levels.

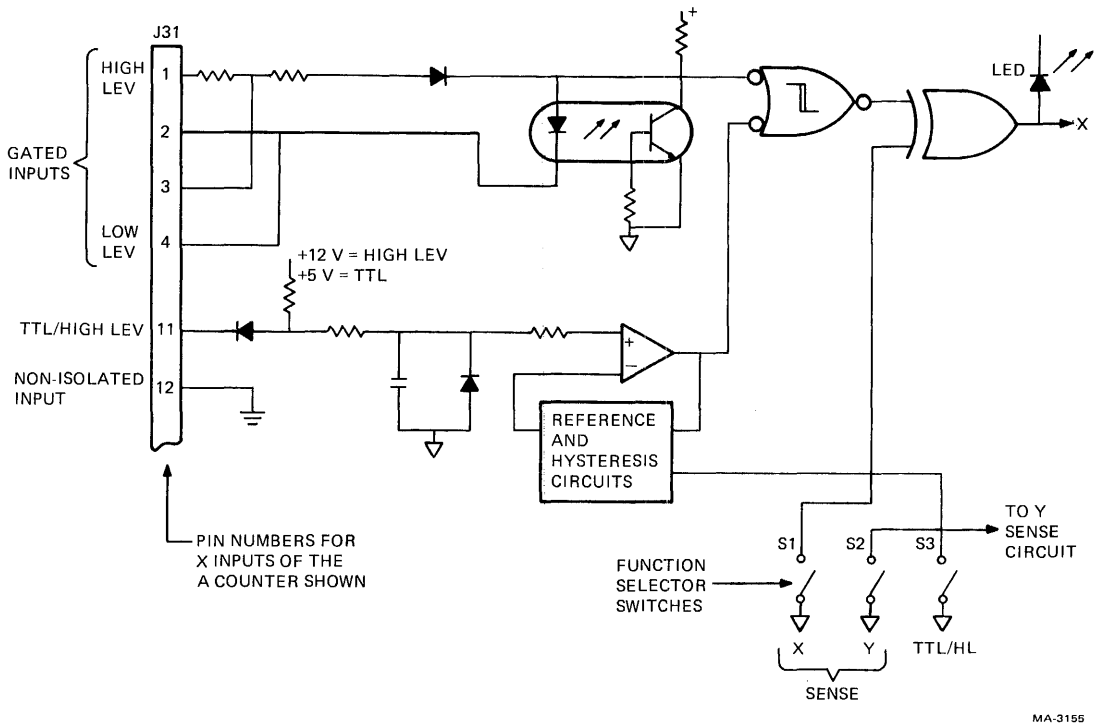


Figure 6-7-6 Electrical and Logical Interface Simplified Circuit

At the module input points, current flowing in the isolated input circuit constitutes a logical one, as does a low level to the nonisolated input circuit. The outputs of these two circuits are ORed to represent a single X or Y input. It is at the output of the OR gate that the logical sense may be inverted by switch S1 or S2. Each of the four interface circuits is equipped with a LED indicator. The LED is on for a true input.

Frequency and Time Base Select Circuit

The two input conditioning and control sections share a common frequency and time base source. From this source, the two frequency and time base selection circuits choose the desired inputs as a function of the position of switches E31-4 and 5, and E23-4 and 5, for the A and B counters respectively. These switches are shown as S4 and S5 in the block diagram of Figure 6-7-7. The time base part of this section actually multiplies its inputs by ten to arrive at its selected time base output. This is accomplished by a divide by ten counter that is started when the counter is armed by writing the low byte (by WRØ for the A counter or by WR2 for the B counter), and outputs one period for ten of its input periods. This ensures that the time base starts within 1Ø percent of its period after the counter has been armed.

When the TBIT is asserted, this section puts out a 5 kHz frequency and a ten second time base for test purposes. In this mode, loading the counter with zeros results in a count of 5Ø,ØØØ decimal. (This equals 141,52Ø octal which is represented as 3Ø3 in the high byte and 12Ø in the low byte.) When the DBIT is asserted, all field inputs and outputs are disabled. Asserting the DBIT and TBIT together prevents any field signals from being ORed with the test signals.

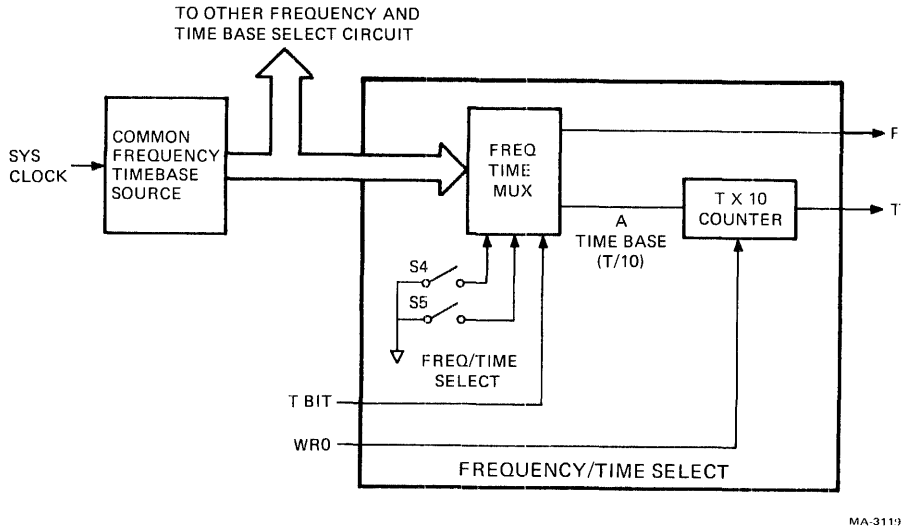


Figure 6-7-7 Frequency and Time-Base Select Circuit

Modes and Time/Frequency Bases

The counter has four operating modes: modes 1, 2, and 3 for frequency or event counting and mode 4 for measuring time periods. Typical applications of the four modes are illustrated in Figure 6-7-8. When modes 1, 2, and 3 are chosen, an appropriate time base (internal or external) is chosen. When an external time base is being used, the internal time base selection must be infinite. For periodic inputs, the frequency of the input is determined by:

$$f = n/T$$

where:
- f = the frequency of the input (events per second)
- n = the number of counts
- T = the chosen time base in seconds.

In mode 4 an internal frequency is selected and the period is determined by:

$$T = n/f$$

where:
- T = the length of the period in seconds
- n = the number of counts
- f = the internal frequency selection.

The resolution of T is therefore 1/f.

The propagation delays associated with the counter's X and Y inputs are listed below in the module's table of specifications and must be taken into consideration by the user for modes 2 or 3. Note that the specification lists significantly different delays for isolated and nonisolated inputs. If these delays and their tolerances are not considered, the logical AND or OR of these signals may result in counting invalid pulses or the negation of valid pulses. The specifications list maximum propagation delays; for purposes of calculation, the minimum delay can be assumed to be one half the maximum delay.

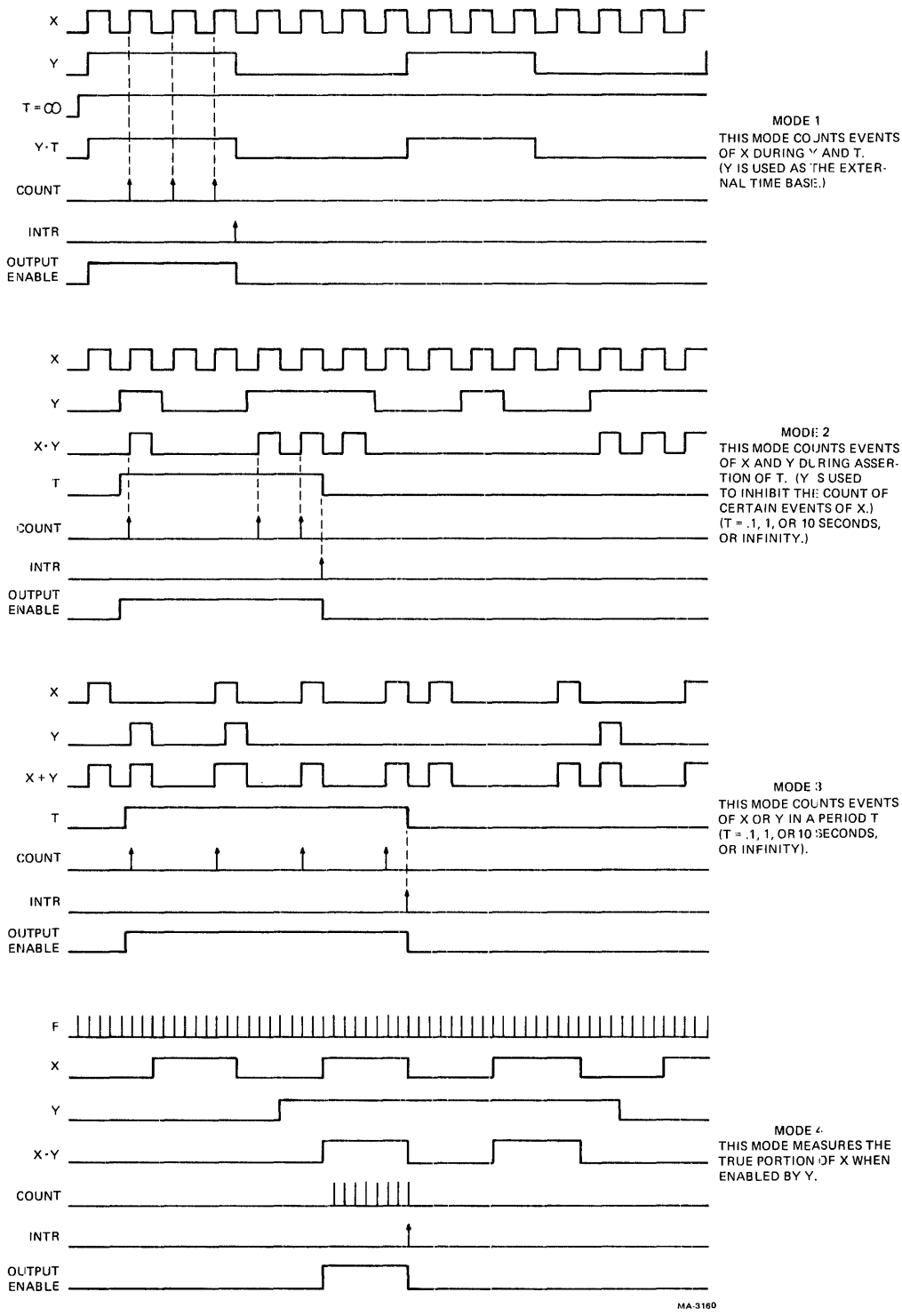


Figure 6-7-8 Counter Operating Modes

Counter Enabling and Interrupt Modes

The outputs of the mode select circuit consist of SIG, the signal that is to be counted, and the WINDOW signal, which determines the duration of the counting period. The WINDOW signal is asynchronous to the occurrence of any write commands. Synchronization is achieved by the counter enabling circuit (Figure 6-7-3). When the application writes a counter's low byte, WR is produced (WRØ for the A counter or WR2 for the B counter), and the counter is armed. The enabling circuit outputs a signal that starts on the first positive transition of WINDOW after the counter has been armed, and ends on the next negative transition. The output of the counter enabling circuit enables the counter input as illustrated in Figure 6-7-9.

Completion of the count always results in an interrupt, provided subsystem and processor priority conditions allow. Selection of the additional control functions via switches E31-4 and 5, or E23-4 and 5, configures this circuit so that the counter also does one of the following upon reaching the all ones count.

1. Count for the entire time period and ignore any overflows.

2. Interrupt when an all ones count is reached, but continue counting.

3. Interrupt and stop counting when an all ones count is reached.

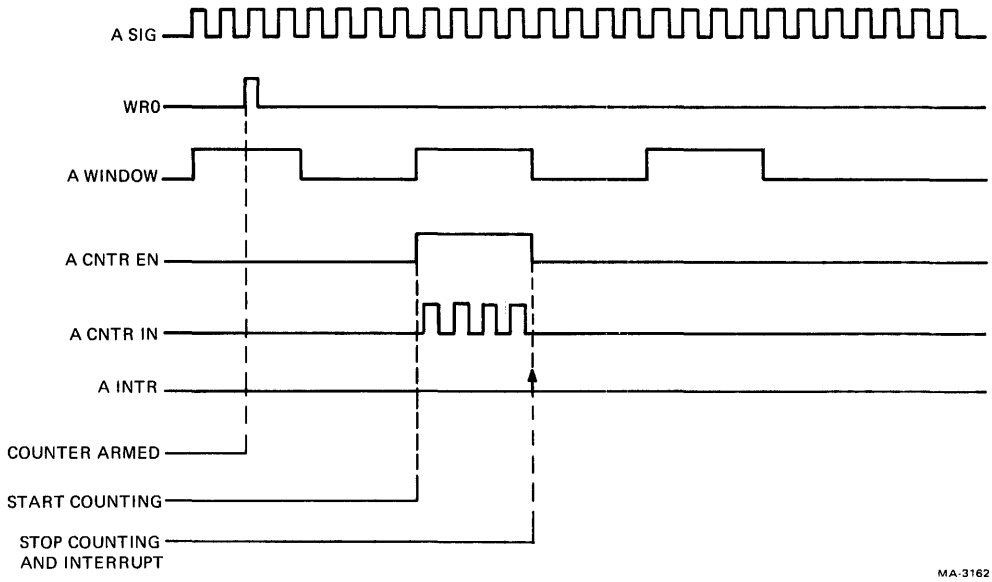


Figure 6-7-9 Counter Enable (Counter A Shown)

PROGRAMMING INFORMATION

The contents of the counter may be read at any time. The high byte must always be read first. When this is done, low byte data is stored in a common output buffer register. When the low byte is read, it is the data in the buffer that is read. Therefore, even though the counter may increment during the time between the high and low byte readings, both bytes contain data of a single point in time.

When a counter is loaded, the high byte must be loaded first. This data is not loaded directly into the counter but is stored in a common input buffer register until the low byte is loaded. At this time, both data bytes are loaded into the counter.

The counter is armed when the low byte is loaded and can begin counting within 10 percent of the time period selected by daughter board switches E31-8 and 9, or E23-8 and 9. For example, if the switches are set for a ten second counting interval, the counter can begin counting within one second.

A counter may be halted at any time by loading its high byte only. The counter contents are not altered by this action because the high byte is actually loaded into a buffer register as discussed previously. The counter can be read at this time. However, when the counter is restarted, the high byte should be reloaded before loading the low byte.

Address Selection

The four module addresses must be assigned according to the rules stated in Chapter 4. They are selected on the module by the 7-pole switch, E61 of the mother board (Figure 6-7-2). An example of one possible address selection is shown in Figure 6-7-10 to illustrate the use of this switch.

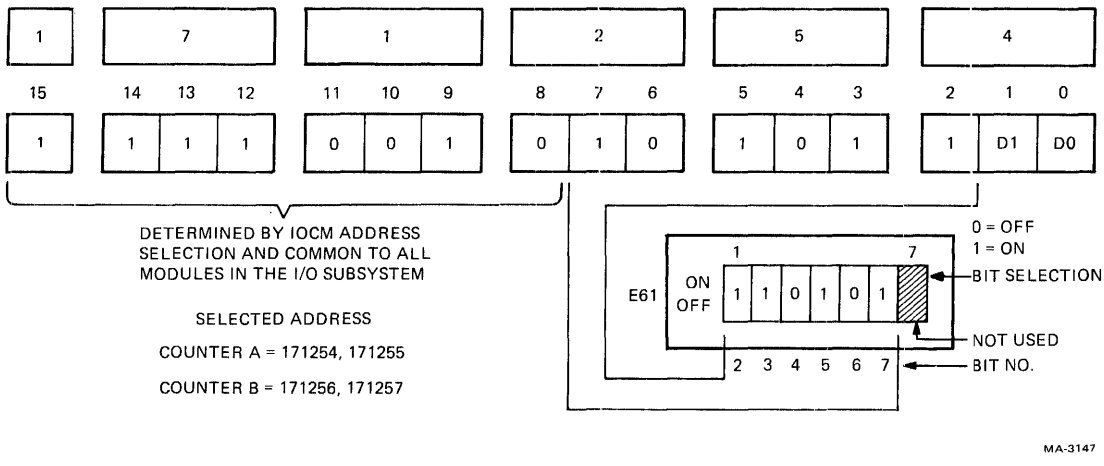


Figure 6-7-10 Address Selection Example

Address Format
The module's four data addresses as determined by the two least significant bits of the address word are as follows.

Y1	Y0	Bits	
0	0	00-07	counter A
0	1	10-17	
1	0	00-07	counter B
1	1	10-17	

Generic Code
The generic codes of the M5014 are a function of the operating mode and are as follows.

Mode	Generic Code
1	144
2	145
3	146
4	147

Note that because the modes for the two counters are chosen independently, the module may have two different generic codes. Refer to the section: Modes and Time/Frequency Bases, for an explanation of the four modes.

Pin Connections
The M5014 module pin connections for J31, the I/O cable connector, are shown in Table 6-7-1.

APPLICATION INFORMATION
A clear understanding of the M5014 input options, operating modes, and interrupt options is necessary to properly use the module. Before proceeding with field wiring and function selector switch configurations, it is recommended that the user review the following sections.

Modes and Time/Frequency Bases
Counter Enabling and Interrupt Options

Field Connections
Field connections for the M5014 may be implemented with the BC40A screw terminal assembly. Field wiring connected to the screw terminals is connected to the module's field interface connector (J31) via a cable provided with the screw terminal assembly. (The module's other cable connection, J32, is for manufacturing test purposes only and is not suitable for field interface.) There are several possible field wiring configurations. The particular configuration required depends on some user exercised options as described below.

Table 6-7-1 Module M5Ø14 I/O Pin Connections (J31)

Module I/O Connector Pin	Field I/O		Module I/O Connector Pin	Field I/O	
1	X ISO HIGH LEV +	Counter A	2	X ISO HIGH LEV -	Count A
3	X ISO LOW LEV +		4	X ISO LOW LEV -	
5	Y ISO HIGH LEV +		6	Y ISO HIGH LEV -	
7	Y ISO LOW LEV +		8	Y ISO LOW LEV -	
9	Not used		1Ø	Not used	
11	X NON-ISO IN		12	Common	
13	Y NON-ISO IN		14	Common	
15	ENABLE OUT		16	Common	
17	Common		18	Common	
19			2Ø		
21			22		
23			24		
25			26		
27			28		
29			3Ø		
31			32		
33	Common		34	Common	
35	X ISO HIGH LEV +		36	X ISO HIGH LEV -	
37	X ISO LOW LEV +		38	X ISO LOW LEV -	
39	Y ISO HIGH LEV +		4Ø	Y ISO HIGH LEV -	
41	Y ISO LOW LEV +	Counter B	42	Y ISO LOW LEV -	Count B
43	Not used		44	Not used	
45	X NON-ISO IN		46	Common	
47	Y NON-ISO IN		48	Common	
49	ENABLE OUT		5Ø	Common	

The user has a choice of isolated or nonisolated inputs. Isolated inputs may be high level (25-55 V) or low level (12-28 V). Moreover, isolated X and Y inputs need not be alike (i.e., one may be a high level and the other a low level). Nonisolated inputs may be high levels or TTL levels; however, nonisolated X and Y inputs must be alike because the TTL/HIGH LEVEL option is selected for both X and Y by a single switch.

The user may also use inverted logic levels. For example, suppose that the user's signal for true X input is one that turns current off (isolated input), or is a high level (nonisolated input). These are inverted inputs for the M5Ø14 but may be used if the X sense switch for that counter (S1 of E31 or E23) is placed in the on position. The same option for Y inputs is selected with the Y sense switch (S2 of E31 or E23).

The LED indicator for a given input will be on for a true field input regardless of whether it is an inverted input, as long as the sense switch for that input is properly set. The sense switch also enables the user to define an unused X or Y input as either true or false as required by the mode logic.

Examples of some possible field connections utilizing the BC40A screw terminal assembly are shown in Figures 6-7-11, -12, and -13. Table 6-7-2 contains a convenient summary of all screw terminal connections for the module.

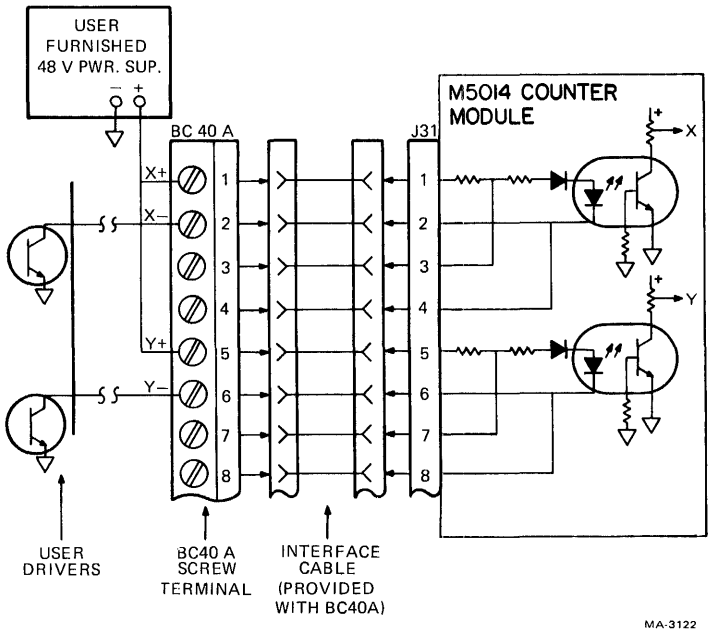


Figure 6-7-11 M5014 Isolated High Level Input Application

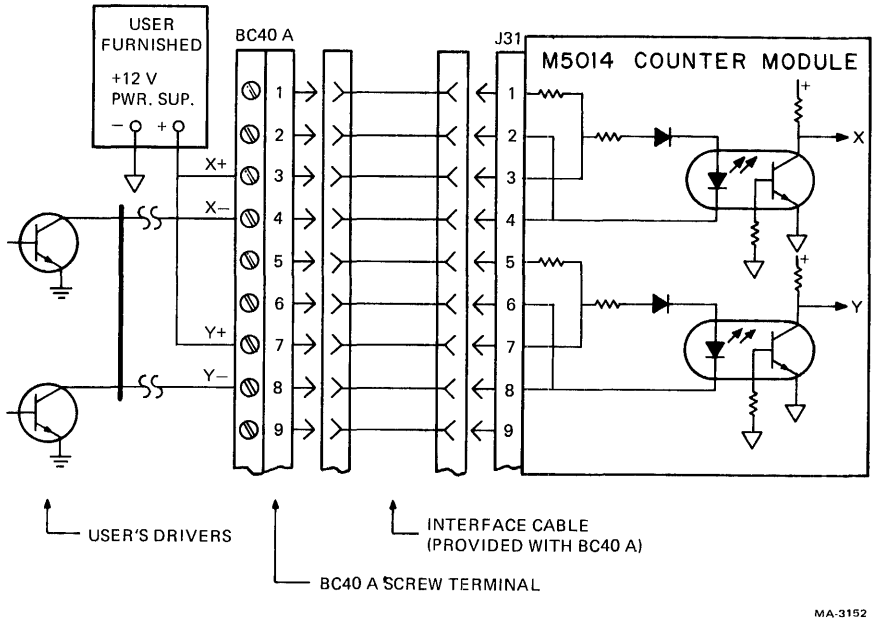


Figure 6-7-12 M5014 Isolated Low Level Input Application

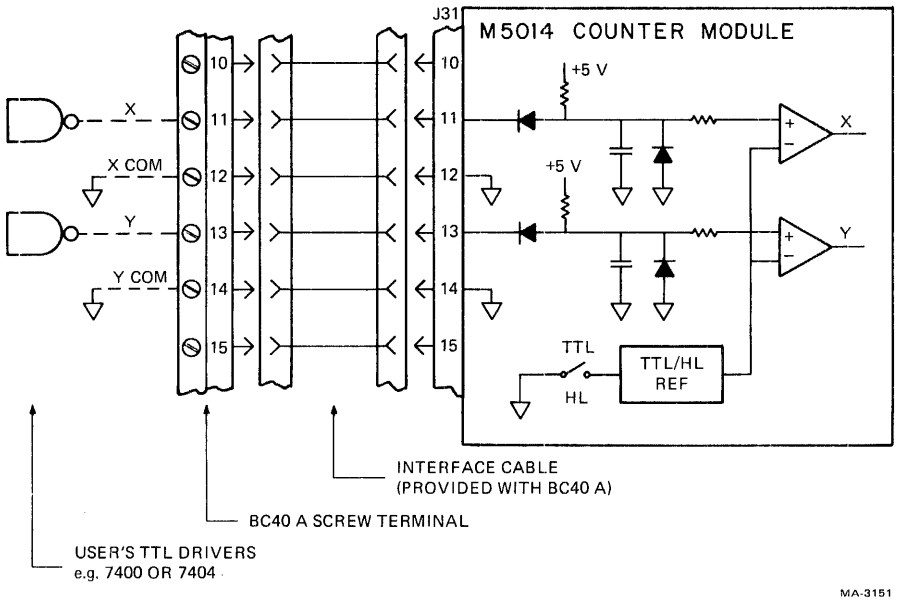


Figure 6-7-13 M5Ø14 Nonisolated TTL Input Application

Table 6-7-2 Module 5014 Field I/O Screw Terminal Connections

Field I/O					Screw Terminal Number
Counter A	Isolated	X	High level	+	1
				-	2
			Low level	+	3
				-	4
		Y	High level	+	5
				-	6
			Low level	+	7
				-	8
				Not used	9
				Not used	10
	Non-isolated	X	TTL/HL	input	11
				common	12
		Y	TTL/HL	input	13
				common	14
			Enable	output	15
				common	16
				common	17
				common	18
Counter B	Isolated	X	High level	+	19
				-	20
			Low level	+	21
				-	22
		Y	High level	+	23
				-	24
			Low level	+	25
				-	26
				Not used	27
				Not used	28
	Non-isolated	X	TTL/HL	input	29
				common	30
		Y	TTL/HL	input	31
				common	32
			Enable	output	33
				common	34

Function Selector Switches

Input senses, operating modes, interrupt modes, and frequencies or time bases are selected by switch packs E31 and E23 for the A and B counters respectively. The two counters are independent and may be configured differently from one another.

When the desired operating conditions have been established, switch selection may be facilitated by referring to Figure 6-7-14 which summarizes the possible configurations.

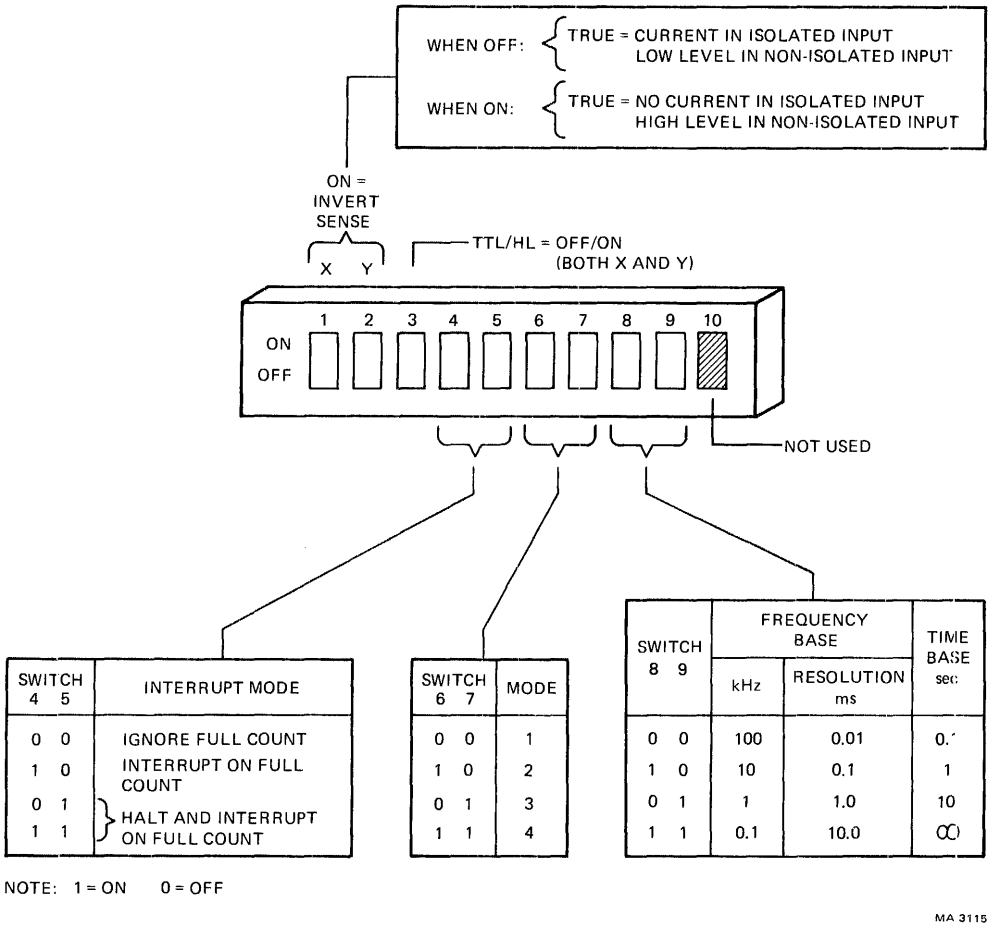


Figure 6-7-14 Function Selector Switches - Usage Summary

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc
Operating current	14Ø mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 1ØØ mA maximum
Backup supply: 4Ø mA maximum

Standby current (backup supply)	3Ø mA maximum

Isolated Input Characteristics

Maximum ratings

Positive input voltage	+55 V
Negative input voltage	-55 V
Short-term overload	Withstands accidental connection to 117 Vac (2 hrs maximum)

Thresholds	12-28 V	25-55 V
Logic zero	5.2 V typical 3.3 V minimum	8.7 V typical 5.5 V minimum
Logic one	5.5 V typical 7.8 V maximum	9.3 V typical 13.2 V maximum
Hysteresis	Ø.3 V typical	Ø.6 V typical

Input current	12-28 V	25-55 V
At input = +12 V, diff.	4.7 mA typical	
At input = +25 V, diff.	1Ø.6 mA typical 12.Ø mA maximum	
At input = +55 V, diff.		13.5 mA maximum
At input = -12 V, diff.	5Ø microamp maximum Ø.Ø5 microamp typical	5Ø microamp maximum Ø.Ø5 microamp typical

Isolation voltage	1ØØØ V 2ØØ VA for UL approval

Propagation delay	200 microseconds typical
	350 microseconds maximum
Maximum input frequency	1000 Hz (50 percent duty cycle)

Nonisolated Comparator Input Characteristics

Maximum ratings

Positive input voltage	+55 V
Negative input voltage	-55 V
Short-term overload	Withstands accidental connection to 117 Vac (2 hrs maximum)

Thresholds	(TTL mode)	(High-level mode)
Logic zero	1.7 V typical 2.3 V maximum	6.5 V typical 7.9 V maximum
Logic one	0.9 V typical 0.5 V minimum	4.2 V typical 3.2 V minimum
Hysteresis	0.8 V typical	2.3 V typical
Open circuit voltage	4.4 V typical 5.0 V maximum	11.2 V typical 13.5 V maximum

Input currents

At input = 0 V	
	-0.40 mA typical -0.57 mA maximum
At input = +55 V	
	0.05 microamps typical 50 microamps maximum
At input = -55 V	
	-2.24 mA typical -2.50 mA maximum
Propagation delay	4 microseconds maximum
Maximum input frequency	50 kHz (50 percent duty cycle)

Nonisolated Output Characteristics

Maximum ratings

Positive input voltage	55 V
Negative input voltage	-0.6 V
Low voltage output	0.4 V
Off leakage current	20 microamps
Sink current	250 mA

Output timing

Maximum times (microseconds)

Transition	V_{out} = 12 V, RL = 10K		V_{out} = 55 V, RL = 3.5K	
	Propagation Time	**Transition Time**	**Propagation Time**	**Transition Time**
Zero to one	0.3	0.1	0.6	0.2
One to zero	30	10	20	6

NOTE
Propagation time is referenced to the source of the activating signal.

Protection — The output circuits are protected from field overvoltage conditions by a 62 V zener diode across each output. Common mode protection is provided by a 1 A picofuse in series with the dc return

Internal frequency base range — 100 kHz, 10 kHz, 1 kHz, 100 Hz, ±0.1 percent, switch-selectable for each counter

Internal time-base range — 100 msec, 1 sec, 10 sec, ±0.1 percent and infinite, switch-selectable for each counter. Maximum delay from arming of counter to beginning of time base period = 10 percent of period

Physical Characteristics

Dimensions — Quad module, mother/daughter board set, triple width, 8-1/2 inches long

Field connector — Cable type BC40A or customer provided 50-pin Berg

Environmental Characteristics — Complies with DEC STD 102, Class C. Operates in convection cooled environment up to 60 degrees C

Heat dissipation — 6.7 Btu/hr. maximum from internal supply; 10.2 Btu/hr. maximum from field supply

FUNCTIONAL DESCRIPTION

The M5Ø16 input module contains four independent 8-bit up counters intended for prescaling and event counting applications. Each counter has variable radix overflow detection and overflow driven interrupt circuitry. High and low level isolated inputs and nonisolated inputs are provided. Several switches allow the counters to be individually programmed for interrupt, reset, and overflow level options. Provision is made for program controlled testing, input disabling, and reading the module's generic code. Other features include fuse protection and an address selection switch.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-8-1 shows the module's four field inputs entering at J1. Signal conditioning circuits for each input convert the isolated or nonisolated raw field inputs to module logic levels. The outputs of the signal conditioning circuits go to the control gating section. This section receives two control inputs: DBIT and TBIT, which provide a program controlled testing capability. When neither of the control signals is asserted, this section outputs normal data. If DBIT is asserted, all field inputs are disabled. Assertion of TBIT forces all counter inputs to a logical one; therefore, if the inputs are disabled, assertion of the TBIT causes all four counters to increment. Repeated assertions of TBIT make it possible to determine the radices of the counters.

Each output of the control gating section is input to an anticoincidence circuit. These circuits are controlled by the WAIT signal. Normally these circuits have no effect on the counter inputs. However, when a counter read operation takes place, the WAIT signal is asserted, causing the counter input to be delayed until the read operation is complete. This prevents the counter from incrementing while it is being read so that erroneous data is not put on the bus. Note that the anticoincidence circuit, as implemented on this module, only functions when the module's data register is being read (high byte). It has no effect on reading or writing the status register (low byte). A detailed discussion of the anticoincidence circuit under that heading is contained in the M5Ø14 input counter section.

Overflow information from the counters goes to the status register and the counter data to the data multiplexer. The selected data (i.e., counter data, status information, generic code, or the module's address) goes to the D-bus input gating section where it is strobed onto the D-bus by the DI GATE signal.

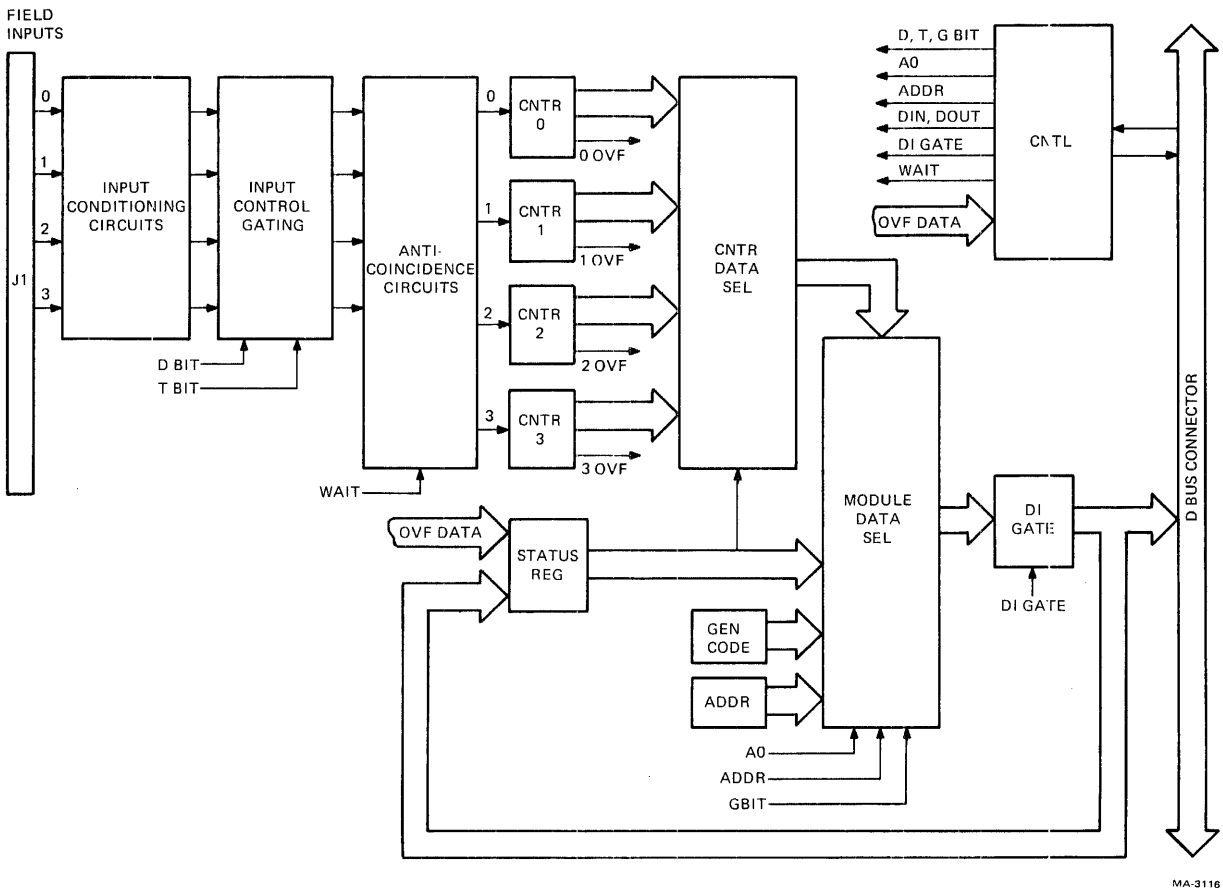


Figure 6-8-1 M5Ø16 Quad Input Counter/Prescaler Block Diagram

Counters

All four M5Ø16 module counters are alike. They are 8-bit up counters equipped with overflow detection and interrupt circuitry. Figure 6-8-2 shows the circuit for a typical counter. The switch packs corresponding to S1 through S1Ø are E17, E18, E19, and E2Ø for counters Ø, 1, 2, and 3 respectively.

One of the counter's data output bits is sampled via one of the switches, S1 through S8. The switch is preselected by the user according to the desired overflow detection point. For example, if the user wishes to detect a count of 1ØØØ (binary), he selects switch 3 (i.e., bit 2). The overflow detection (DET) flip-flop shown goes low momentarily when that bit resets (i.e., when the count changes from Ø111 to 1ØØØ). This causes the OVF flip-flop to set.

The OVF flip-flop is one of the overflow bits in the module's status register. If switch S9 is ON, the OVF flip-flop causes an interrupt. The interrupt and the overflow bits in the status register are cleared when the status register is read with the RIF bit set.

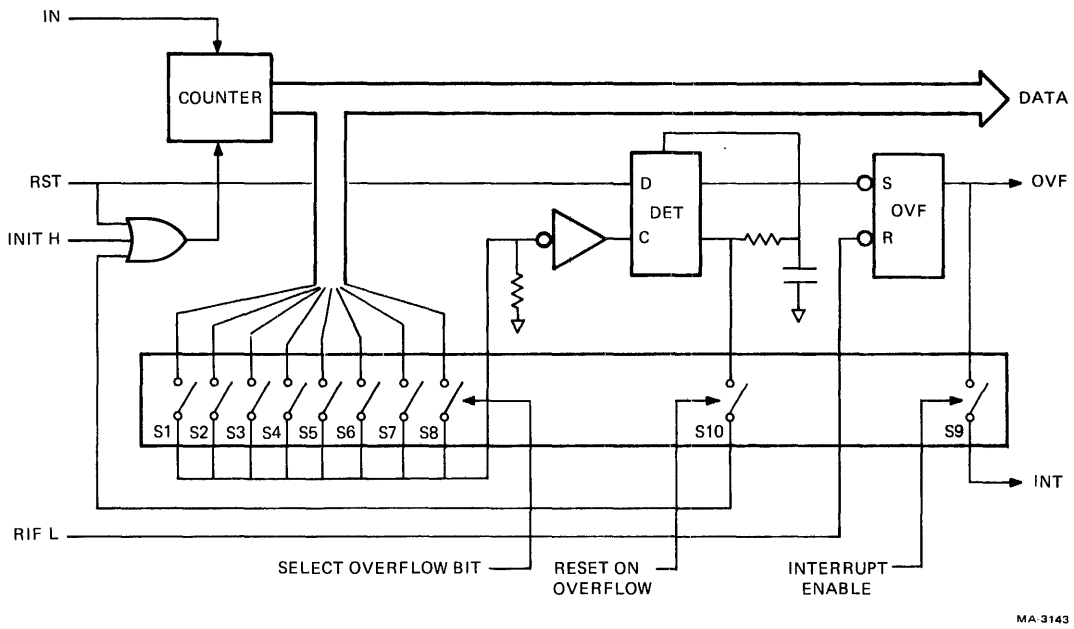


Figure 6-8-2 Counter Circuit

If switch S1Ø is ON, the counter resets on overflow. Therefore, when S1Ø is ON, the counter essentially becomes variable radix, appearing to be only the length selected by the overflow selection switch (i.e., switch 3 in the above example). With switch S1Ø off, the counter is always radix 256, eight bits, regardless of which bit is selected for overflow detection.

The software can reset the counter via the RST signal. A software initiated reset does not cause the DET and OVF flip-flops to respond as would an overflow.

Input Circuits

The module's isolated and nonisolated input circuits resemble those of the M5Ø12 and M5Ø1Ø modules respectively. The isolated inputs are dissimilar to those of the M5Ø12 only in that they accept higher frequency inputs, and they have separate terminals for high and low level inputs.

PROGRAMMING INFORMATION

The M5Ø16 module occupies two byte addresses on the bus. The low byte contains a status register which provides data selection and overflow information, as well as a clear enable bit. The high byte contains the data register. The single read-only data register serves all four counters and contains, at any given time, the contents of the counter currently selected by the two low order bits of the status register. This means that before reading the module's data register it is first necessary to select the desired counter by writing the appropriate bits in the status register.

When one of the module's counters overflows and causes an interrupt, the corresponding status register overflow bit identifies the interrupting counter.

To have a counter cleared after its data is read, a one must first be written in the status register's clear enable bit (bit 2). Then, when that counter's data is read, both it and the enable bit are cleared. A summary of data and status register information is shown in Figure 6-8-3.

Address Selection

The two module addresses must be assigned according to the rules stated in Chapter 4. They are selected on the module by the 7-pole switch, E42 (Figure 6-8-4). To illustrate the use of this switch an example of one possible address selection is shown in Figure 6-8-5.

Generic Code

The generic code for the M5Ø16 module is octal 142.

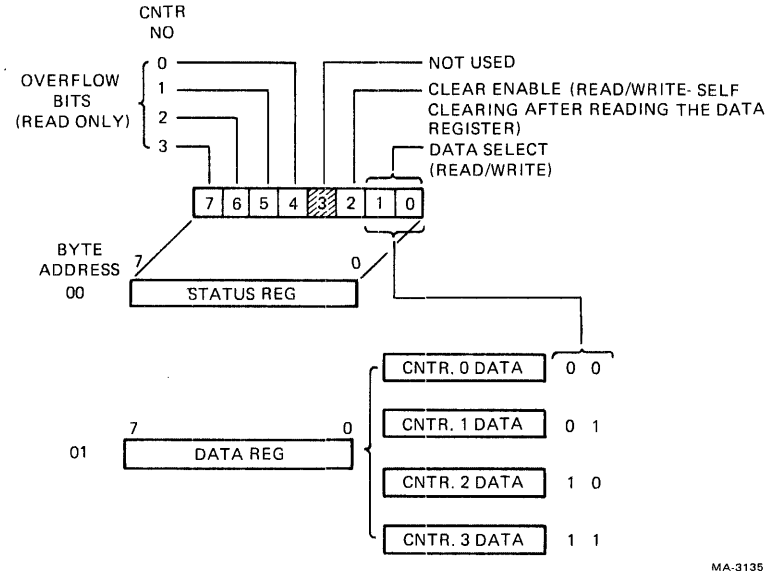


Figure 6-8-3 Register Information

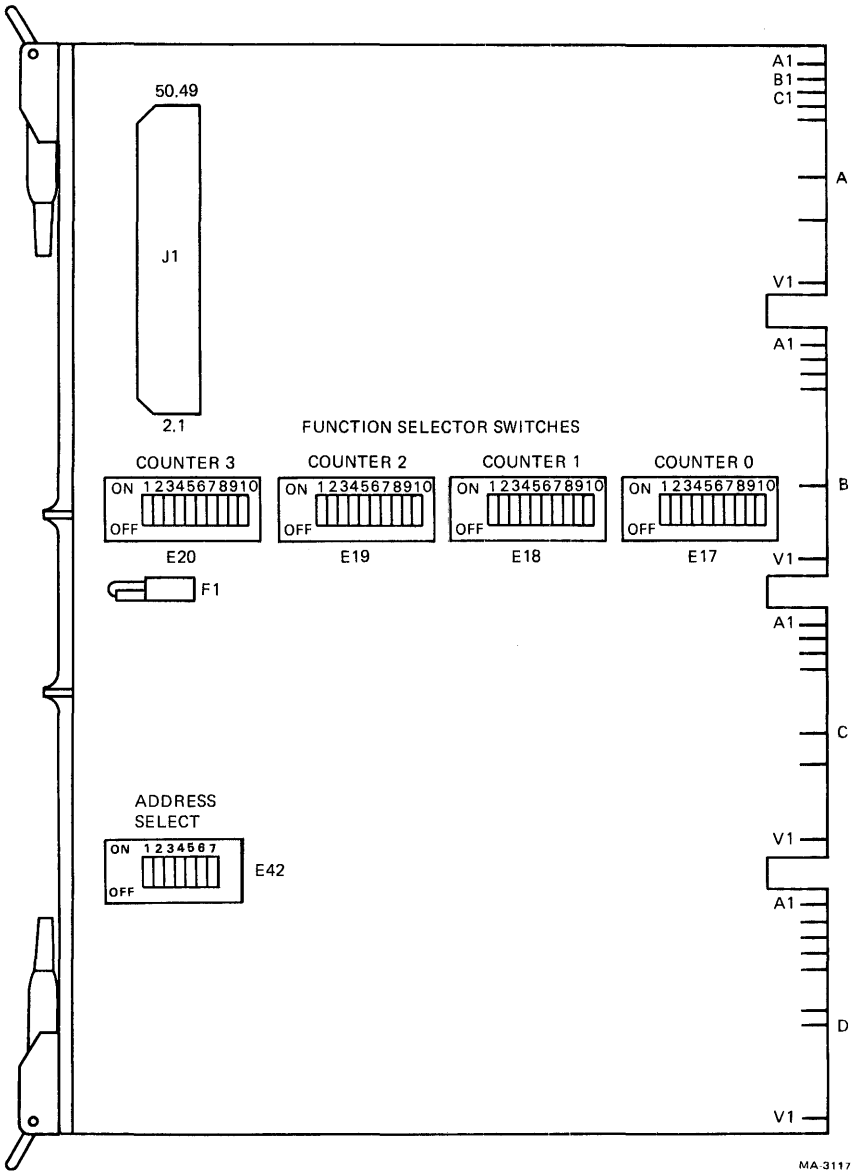


Figure 6-8-4 M5Ø16 Quad Counter/Prescaler

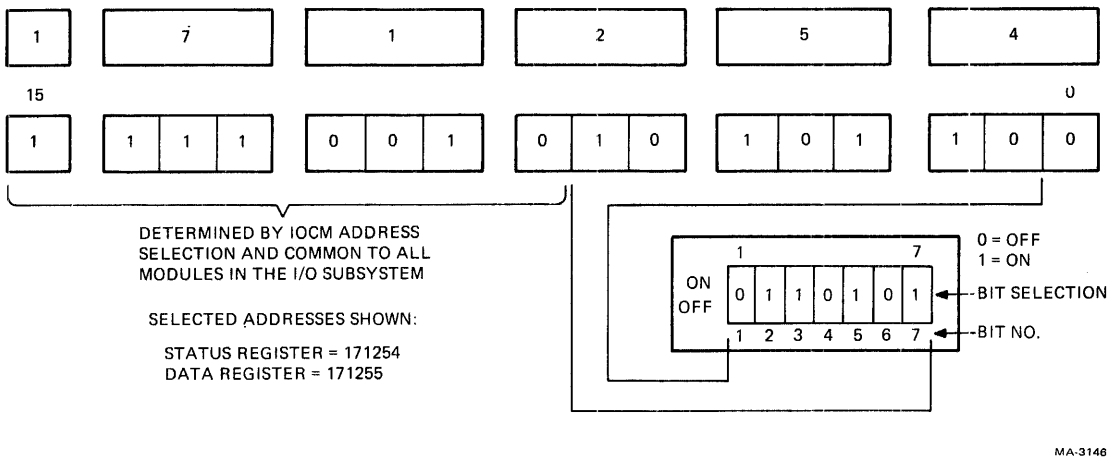


Figure 6-8-5 Address Selection Example

Pin Connections

The M5Ø16 module pin connections for J1, the I/O cable connector, are shown in Table 6-8-1.

Table 6-8-1 Module M5Ø16 I/O Pin Connections

Module I/O Connector Pin	Field I/O		Module I/O Connector Pin	Field I/O	
1	ISO HIGH LEV +	CNTR Ø	2	ISO HIGH LEV -	CNTR Ø
3	ISO LOW LEV +		4	ISO LOW LEV -	
5	NON-ISO IN		6	Common	
7	Not used		8	Not used	
9	ISO HIGH LEV +	CNTR 1	1Ø	ISO HIGH LEV -	CNTR 1
11	ISO LOW LEV +		12	ISO LOW LEV -	
13	NON-ISO IN		14	Common	
15	Not used		16	Not used	
17	Common		18	Common	
19	↑		2Ø	↑	
21			22		
23			24		
25			26		
27			28		
29			3Ø		
31	↓		32	↓	
33	Common		34	Common	
35	ISO HIGH LEV +	CNTR 2	36	ISO HIGH LEV -	CNTR 2
37	ISO LOW LEV +		38	ISO LOW LEV -	
39	NON-ISO IN		4Ø	Common	
41	Not used		42	Not used	
43	ISO HIGH LEV +	CNTR 3	44	ISO HIGH LEV -	CNTR 3
45	ISO LOW LEV +		46	ISO LOW LEV -	
47	NON-ISO IN		48	Common	
49	Not used		5Ø	Not used	

APPLICATION INFORMATION

Proper I/O module installation procedures are presented in Chapter 3, Paragraph 3.3.3.3. The M5Ø16 has the following additional requirements.

Field Connections

The field interface for this module is similar to that of other digital I/O modules. An example of the field wiring connections for each type of interface is shown in Figure 6-8-6 and 6-8-7. Screw terminal connections for all the module's counter inputs are listed in Table 6-8-2.

Function Selector Switches

Overflow, reset, and interrupt options for each of the four counters are individually selected on the module by the four 1Ø-pole switches, E17 through E2Ø (Figure 6-8-4). The four counters are independent and may be configured differently from one another. The option selection procedure is identical for each counter and is illustrated in Figure 6-8-8. Only <u>one</u> overflow level detection switch (1 through 8) should be ON at any one time or the counter may malfunction.

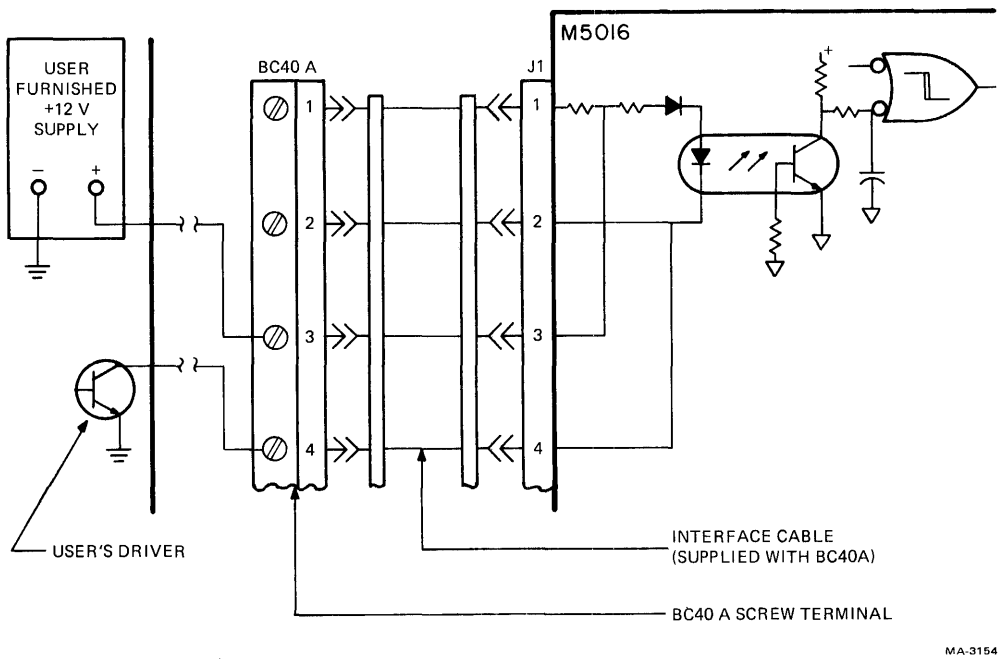


Figure 6-8-6 Counter Ø Isolated Low Level Input Application

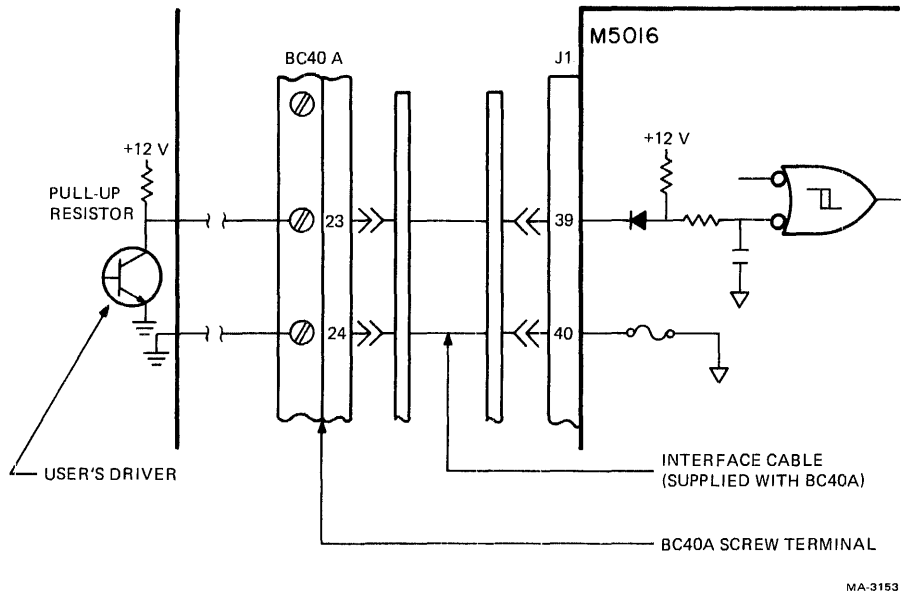


Figure 6-8-7 Counter 2 Nonisolated Input Application

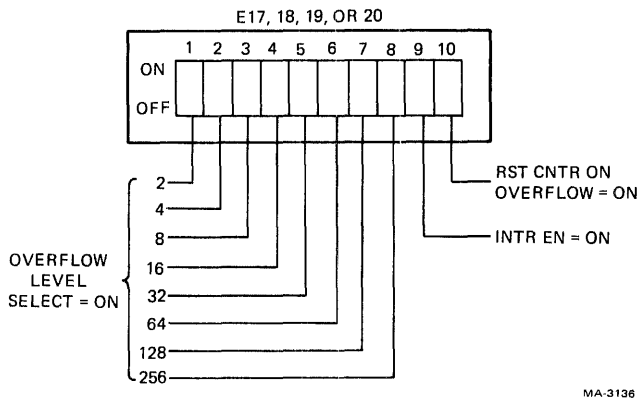


Figure 6-8-8 Function Selector Switches

Table 6-8-2 Module M5Ø16 Field I/O Screw Terminal Connections

Counter	Field I/O		Screw Terminal Number
Ø	ISO HIGH LEVEL	+	1
		-	2
	ISO LOW LEVEL	+	3
		-	4
	NON-ISO	Input	5
		Common	6
			7
			8
1	ISO HIGH LEVEL	+	9
		-	1Ø
	ISO LOW LEVEL	+	11
		-	12
	NON-ISO	Input	13
		Common	14
			15
			16
		Common	17
		Common	18
2	ISO HIGH LEVEL	+	19
		-	2Ø
	ISO LOW LEVEL	+	21
		-	22
	NON-ISO	Input	23
		Common	24
			25
			26
3	ISO HIGH LEVEL	+	27
		-	28
	ISO LOW LEVEL	+	29
		-	3Ø
	NON-ISO	Input	31
		Common	32
			33
			34

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc
Operating current	1Ø mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 3.2 mA maximum
Backup supply: 6.8 mA maximum

Standby current (backup supply)	6.8 mA maximum

Isolated Input Characteristics

Maximum ratings	Positive input voltage: +55 V Negative input voltage: -55 V Short-term overload: Withstands accidental connection to 117 Vac for two hours

Thresholds	Range	12-28 V	25-55 V
	Logic zero:	5.2 V typical 3.3 V minimum	8.7 V typical 5.5 V minimum
	Logic one:	5.5 V typical 7.8 V maximum	9.3 V typical 13.2 V maximum
	Hysteresis:	Ø.3 V typical	Ø.6 V typical
Input current			
At input = +12 V differential		4.7 mA typical	
At input = +25 V differential		1Ø.6 mA typical 12.Ø mA maximum	
At input = +55 V differential		13.5 mA maximum	
At input = -12 V differential		5Ø microamps maximum Ø.Ø5 microamps typical	5Ø microamps maximum Ø.Ø5 microamps typical

Isolation voltage	1ØØØ V 2ØØ VA for UL approval
Propagation delay	2ØØ microseconds typical 35Ø microseconds maximum
Maximum input frequency	1ØØØ Hz (5Ø% duty cycle)

Nonisolated Input Characteristics

Maximum ratings	Positive input voltage: +55 V Negative input voltage: -3Ø V Common mode input voltage: Ø V	
Thresholds	Logic zero:	6.7 V typical 9.7 V maximum
	Logic one:	4.1 V typical 1.7 V minimum
	Hysteresis:	2.6 V typical
Input currents		
At input = -3Ø V:		2.Ø mA typical 2.7 mA maximum
At input = +55 V:		Ø.Ø5 microamp typical 5Ø microamp maximum
Propagation delay		7.Ø microseconds maximum
Maximum input frequency		4Ø kHz (5Ø percent duty cycle)
Protection		Common mode protection is provided by a 62.5 mA Picofuse in series with the dc return

Physical Characteristics

Dimensions	Quad module, single width, 8-1/2 inch length
Field connector	Cable type BC4ØA or customer supplied 5Ø-pin Berg

Environmental Characteristics	Complies with DEC STD 1Ø2 Class C. Operates in convection cooled environment up to 6Ø degrees C
Heat dissipation	Ø.5 Btu/hr maximum due to module circuits; 5 Btu/hr maximum due to field inputs

FUNCTIONAL DESCRIPTION

The M5Ø31 is an isolated dc input module used for monitoring voltages or contact closures. COS (change-of-state) initiated interrupt capability is also provided. The module accepts up to 16 inputs, structured as two 8-bit bytes, and sends them under program control to the D-bus. Two additional bytes contain COS information. Provision is made for program-controlled testing, input disabling, and reading the module's generic code. The module also features an address selection switch, and interrupt enable switches for all 16 bits.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-9-1 shows that field data entering through J1 is addressed and controlled by signals from the D-bus interface connector and is ultimately output to the D-bus. Also shown is the interrupt selection and control circuitry, which provides the option of having the module initiate a processor interrupt when any input changes state. Data paths and their control are discussed below.

Data Paths

Each of the 16 field inputs entering at J1 goes through an optical isolator that isolates the I/O Subsystem from noise or common mode voltages while allowing transmission of the desired dc signal. Following each isolator is a low pass filter for high frequency noise immunity, and a Schmitt trigger which further improves noise immunity.

The 16 field signals from the output side of the Schmitt triggers, go to the input gating section, where they are separated into two 8-bit bytes. This section also receives two control inputs from the D-bus interface connector, TBIT and DBIT, which, under program control, may modify the data for testing. The output of this section is normal data if these controls are not asserted. If the program causes TBIT to be asserted, the data output is all ones. If DBIT is asserted, the output is disabled and is read as all zeros. If both TBIT and DBIT are asserted the output is all ones.

The 16 outputs of the input gating section are separated into two 8-bit bytes and go to both the input multiplexer and the COS detectors. If any of the field data bits changes state (in either direction), this event is stored as a one in the corresponding bit in the COS register. The output of these registers also goes to the input multiplexer.

The input multiplexer receives the two data bytes from the input gating section, two more from the COS registers, plus the module's generic code and its address byte. This section is controlled by signals from the multiplexer control section and provides normal data if one of the module's four data bytes is selected, the module's identity code if the GBIT signal is asserted, or one of

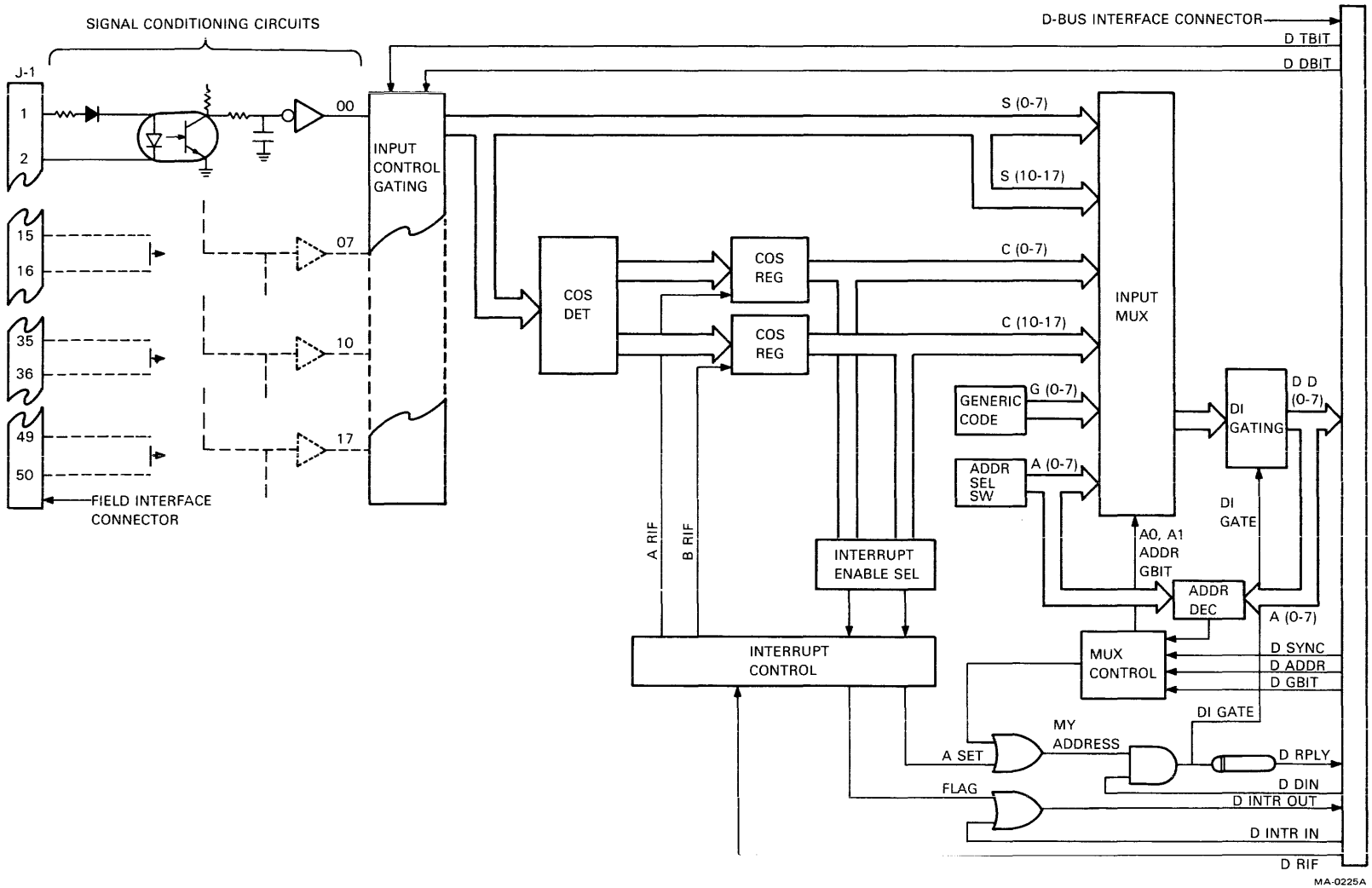


Figure 6-9-1 M5031 16-Bit Isolated COS Input Module Simplified Block Diagram

the module's addresses if the D ADDR signal is asserted. The selected byte goes to the DI gating section where it is strobed onto the D-bus by the DI GATE signal.

Data Control Signals

Control signals for the above mentioned data paths are initiated by the program, resulting in the following typical control sequence. When the program calls for a DATAI from one of the module's four addresses, the IOCM starts a D-bus Cycle and causes the address to be put on the D-bus. The module's address decoder decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the multiplexer control to produce the AØ and A1 signals for selection of the correct data byte by the input multiplexer. At this time MY ADDRESS is also produced. After a short delay, D DIN is asserted by the IOCM and ANDed with MY ADDRESS to give DI GATE which strobes the data onto the D-bus. DI GATE also produces D RPLY after a short delay to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated, causing DI GATE to negate and remove data from the D-bus.

If the processor reads the IAR in response to an interrupt from this module, a Modified D-bus Cycle is initiated by the IOCM. In this case, there is no D SYNC signal, but D ADDR occurs and causes the input multiplexer to output one of the module's addresses instead of data.

Interrupt Control Signals

If one of the field inputs changes state, the COS register bit corresponding to that field input is asserted. If that bit has been selected as an interrupting bit by one of the interrupt enable switches, it provides an input to the interrupt control section. This section produces a flag signal that results in a processor interrupt if all priority requirements are met. (The flag signal is an input to the INTR IN, INTR OUT daisy chain.) When the interrupt occurs, a Modified D-bus Cycle is initiated by the IOCM. As previously stated, this results in the D ADDR signal which selects the address input to the input multiplexer and causes the interrupt control section to produce A SET which results in MY ADDRESS. When D DIN is asserted, the module's interrupting address is put on the D-bus.

At this point the processor has identified the interrupting address. The appropriate interrupt service routine is then executed. If now the processor RIFs the module (reads the interrupting data address or the corresponding COS register with R=1 in the CSR), the interrupt control section resets the COS register.

Address and Flag Selection

The four module addresses must be assigned according to the rules stated in Chapter 4. They are selected on the module by the 8-pole switch, E41 (Figure 6-9-2). To illustrate the use of this switch

an example of one possible address selection is shown in Figure 6-9-3. Interrupt enable selection for any or all of the 16 module inputs is provided by switches located at E11 and E12, for the low and high bytes, respectively. The relationship of field signal numbers to switch numbers is shown in Figure 6-9-2.

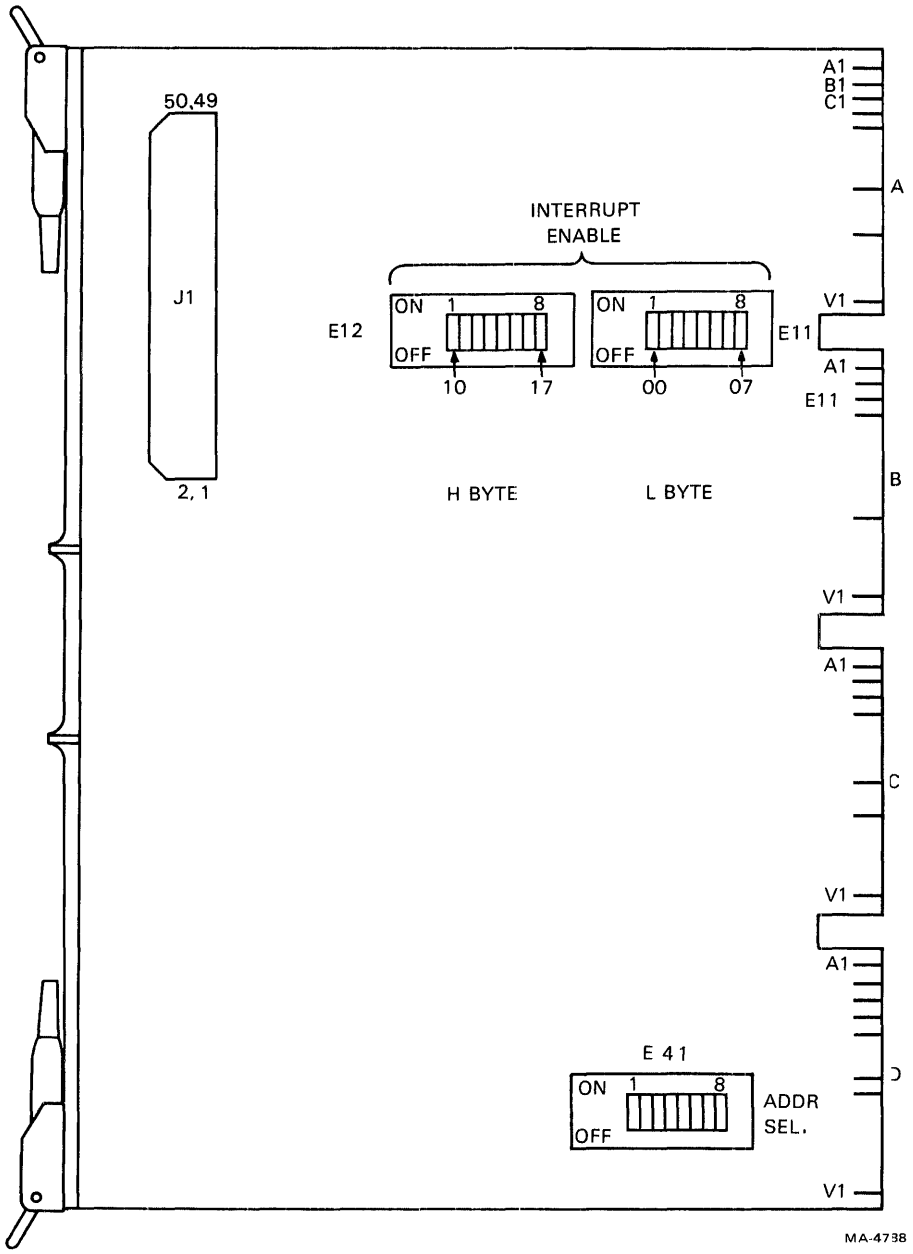


Figure 6-9-2 M5Ø31 16-Bit Isolated COS Input

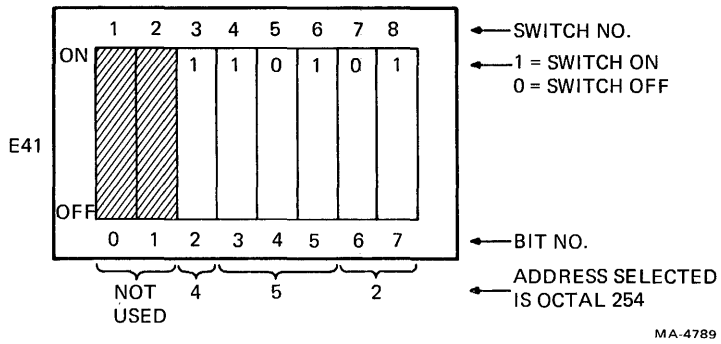


Figure 6-9-3 Address Selection Switch

Address Format
The module's four data addresses, as determined by the two least significant bits of the address word, are as follows.

Y1	Y0	Data (Octal)
0	0	Field 00-07
0	1	Field 10-17
1	0	COS register 00-07
1	1	COS register 10-17

Generic Code
The generic code for the M5031 module is octal 124.

Pin Connections
The M5031 pin connections for J1, the I/O cable connector, are shown in Table 6-9-1.

Table 6-9-1 Module M5031 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	00+	2	00-
3	01+	4	01-
5	02+	6	02-
7	03+	8	03-
9	04+	10	04-
11	05+	12	05-
13	06+	14	06-
15	07+	16	07-
17		18	
19		20	
21		22	
23		24	
25	Not	26	Not
27	Used	28	Used
29		30	
31		32	
33		34	
35	10+	36	10-
37	11+	38	11-
39	12+	40	12-
41	13+	42	13-
43	14+	44	14-
45	15+	46	15-
47	16+	48	16-
49	17+	50	17-

SPECIFICATIONS

Power Requirements	
Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc
Operating current	57 mA maximum

NOTE
If the backup supply is implemented, total operating current is shared
Main supply: 23 mA maximum
Backup supply: 34 mA maximum

Standby current (backup supply)	34 mA maximum
Input Characteristics	
Differential input voltage	55 V maximum
Logic zero threshold	4.1 V typical 1.6 V minimum
Logic one threshold	4.65 V typical 7.5 V maximum
Hysteresis	Ø.55 V typical
Isolation voltage (between inputs or from inputs to ground)	1ØØØ V maximum
Common mode source	2ØØ VA maximum, for UL approval
Input currents	When input = +12 V differential 3 mA typical When input = +55 V differential 2Ø.5 mA maximum When input = -12 V differential Ø.Ø5 microamp typical 5Ø microamp maximum
Propagation delay	2.5 ms typical 6.2 ms maximum
Physical Characteristics	
Dimensions	Quad module, double width, 8-1/2 inch length
Field connector	Cable type BC4ØA or customer-supplied, 5Ø-pin Berg

NOTE

Two 8-position jumper strips are provided with the BC40A screw terminal assembly. These allow the user to connect the plus or minus inputs together, in 8-input groups, to facilitate field wiring when a common field power source is used.

Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degrees C ambient
Heat dissipation	1.06 Btu/hr maximum due to module circuitry
	63 Btu/hr maximum due to field inputs

FUNCTIONAL DESCRIPTION

The M6010 module provides 32 program-controlled dc outputs. These outputs are single-wire, nonisolated, open-collector, Darlington switches used for controlling relays, solenoid valves, indicators, heaters, etc. Provision is made for reading the module's output status or generic code and for disabling all outputs. The module also features a common output fuse and address selection switches.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-10-1 shows that processor output data entering through the D-bus interface connector is addressed and controlled by signals from the D-bus and output to the field through J1. The sequence of control and data flow is as follows.

Data Paths

Data lines D(0-7) from the D-bus interface connector provide identical inputs to all four data output registers. One of the registers, as determined by the A0 and A1 signals, accepts a new data byte when DO CLOCK is asserted. The other three registers remain unchanged. From the output registers the data lines go through the output inhibit gates to the output switches. These gates inhibit all outputs when the DBIT is asserted. The on or off status of the individual output switches is determined by which data bits are asserted.

The output circuits are Darlington switches which can turn on or off a variety of dc circuits. Each of these switches is protected from field overvoltages by a zener diode across its output. The common side of all output switches is returned to ground through a common fuse which protects the module from common mode voltage differences between the field power supplies and the module.

The output data lines also go to the input multiplexer where one of the output bytes, as determined by the A0 and A1 signals, can be selected for process monitoring by performing a DATAI on its address. If the GBIT in the CSR of the IOCM is asserted, the module's identity code is read instead of an output byte. The selected input is then gated onto the D-bus by the DI GATE signal. The TBIT signal is not implemented on this module.

Data Control Signals

Control signals for the above mentioned data paths are initiated by the program, resulting in the following sequence of operation. When the program calls for an operation requiring a DATAO to one of the module's four addresses, the IOCM starts a D-bus Cycle and causes the address to be put on the D-bus. The module's address decoder decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the module to produce its internal MY ADDRESS signal as well as the A0 and A1 signals for the selection of the correct data byte. After a short delay, D

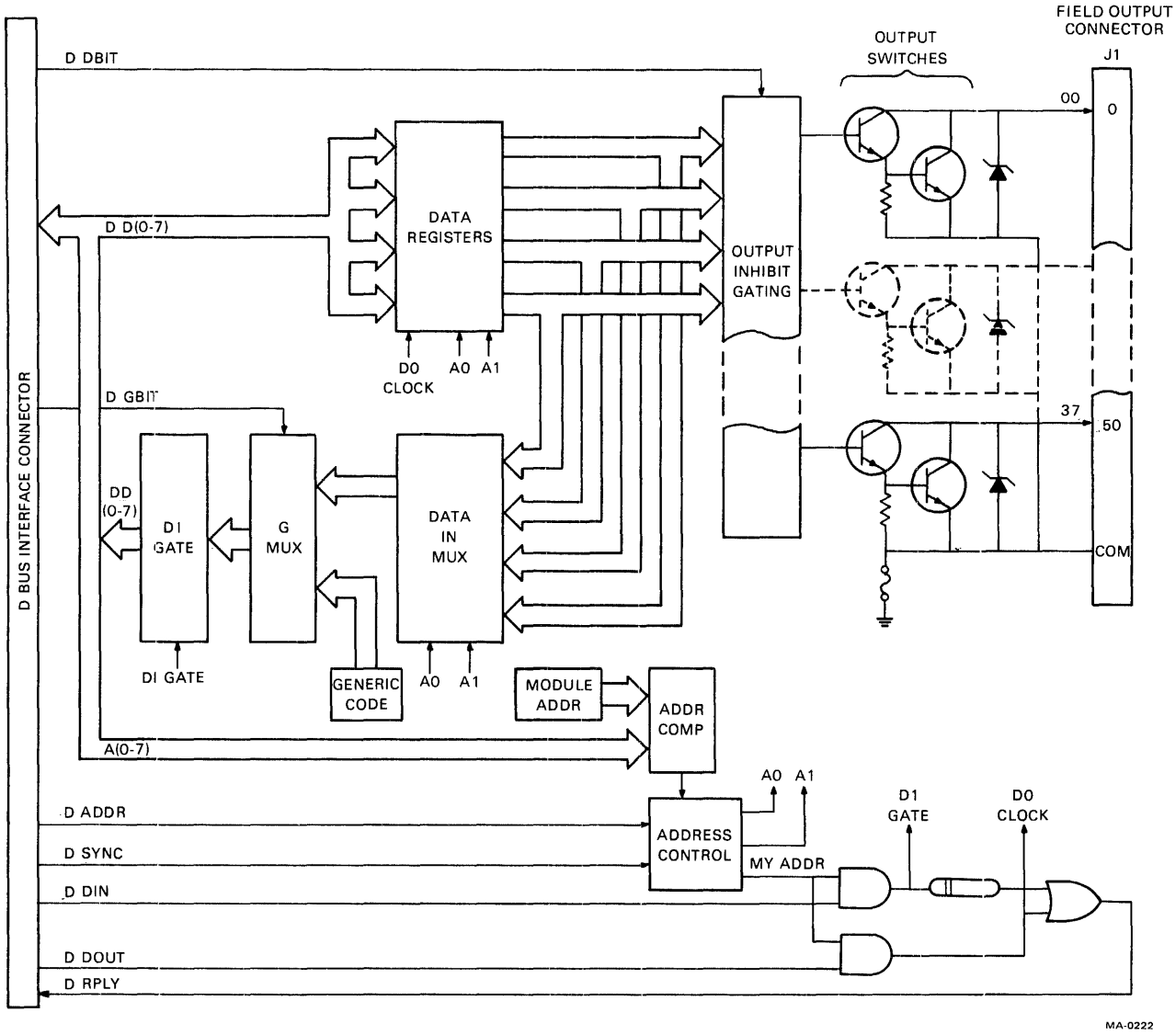


Figure 6-10-1 M6010 32-Bit DC Output Module, Simplified Block Diagram

DOUT is asserted and ANDed with MY ADDRESS to produce DO CLOCK, which strobes the new data byte into the output register. From there it goes to the output gating, output switches, and to J1, the field output connector. DO CLOCK also produces the D RPLY signal, which informs the processor that the data byte has been accepted for output. The processor then negates D DOUT, which negates DO CLOCK.

The status of the output data remains unchanged unless the program outputs to that address. If the program wants to read back the contents of an output register, it causes the processor to execute a DATAI on that address. When this is done, the processor first asserts the address as before and causes the IOCM to start a D-bus Cycle. This causes the address to be put on the D-bus and decoded

by the module's address comparator. Then, D SYNC is asserted after a short delay for deskewing. This results in the AØ and A1 signals for selecting the proper byte and also the MY ADDRESS signal. However, in this case, the next signal asserted by the IOCM is D DIN, which is ANDed with MY ADDRESS to produce DI GATE. This signal strobes the contents of the G multiplexer onto the D-bus. If the program has set the GBIT in the CSR of the IOCM, the G multiplexer contains the module's identity code instead of the selected data byte. DI GATE also produces D RPLY after a short delay to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated causing DI GATE to negate and remove data from the D-bus.

Address Selection
The four module addresses must be assigned according to the rules stated in Chapter 4. They are selected on the module by the 8-pole switch, E34 (Figure 6-1Ø-2). An example of one possible address selection is shown in Figure 6-1Ø-3 to illustrate the use of this switch.

Generic Code
The generic code for the M6Ø1Ø module is octal Ø41.

Pin Connections
The M6Ø1Ø module pin connections are shown in Table 6-1Ø-1 for J1, the I/O cable connector.

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc $\pm$ 2 Vdc Backup supply: 14 Vdc $\geq$ VB $\geq$ (VS-Ø.7) Vdc
Operating current	89.6 mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: Ø.2 mA maximum
Backup supply: 89.4 mA maximum

Standby current (backup supply)	3.9 mA maximum

Output Characteristics

Maximum ratings	Positive output voltage	+55 V
	Negative output voltage	-Ø.6 V
	Low voltage output	+1.4 V
	Off leakage current	2Ø microamp
	Sink current	25Ø mA per bit 8 A per module

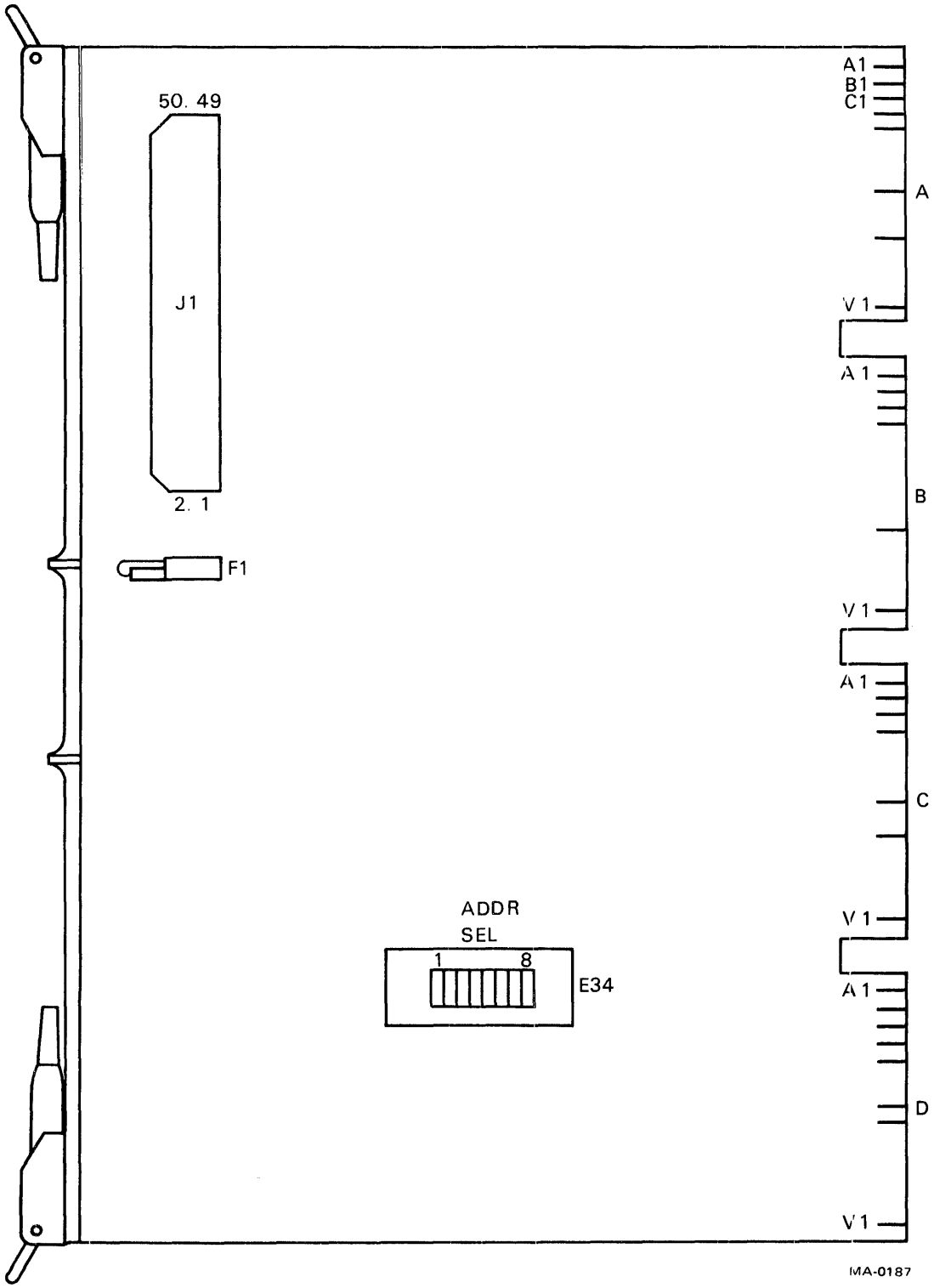


Figure 6-10-2 M6010 32-Bit DC Output

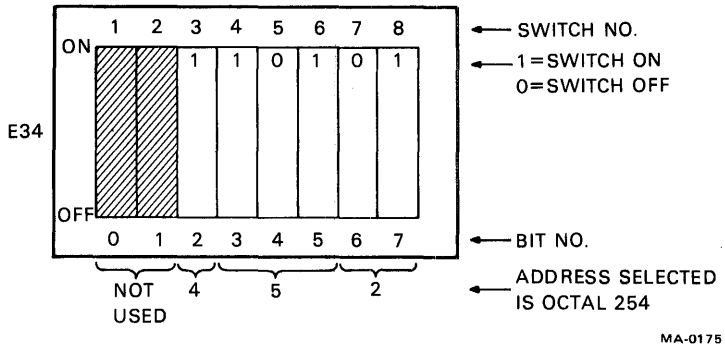


Figure 6-10-3 Address Selection Switch

Table 6-10-1 Module M6010 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	00	2	01
3	02	4	03
5	04	6	05
7	06	8	07
9	10	10	11
11	12	12	13
13	14	14	15
16	16	16	17
17	Common	18	Common
19		20	
21		22	
23		24	
25		26	
27		28	
29		30	
31		32	
33	Common	34	Common
35	20	36	21
37	22	38	23
39	24	40	25
41	26	42	27
43	30	44	31
45	32	46	33
47	34	48	35
49	36	50	37

Output Timing

Maximum Times (microseconds)

	V_{out} = 12 V, RL = 1ØK		V_{out} = 55 V, RL = 3.5K	
	Propagation Time	Transition Time	Propagation Time	Transition Time
Turn-on	Ø.8	Ø.Ø5	Ø.8	Ø.Ø5
Turn-off	3.6	3.9	1.8	2.4

NOTE

Propagation time is referenced to the point where the activating signal enters the module.

Protection

Output circuits are protected from field overvoltage conditions by a zener diode across each output. Common mode protection is provided by a 1 A Picofuse in series with the dc return.

Physical Characteristics

Dimensions

Quad module, triple width, 8-1/2 inch length

Field connector

Cable type BC4ØA or customer-supplied, 5Ø-pin Berg

Environmntal Characteristics

Complies with DEC STD 1Ø2 Class C. Operates in convection cooled environment up to 6Ø degrees C ambient

Heat dissipation

4.52 Btu/hr maximum due to module circuitry;
37.Ø Btu/hr maximum due to field power source

FUNCTIONAL DESCRIPTION

The M6010-YA module provides 32 TTL-compatible, program-controlled dc outputs. These outputs are single-wire, nonisolated, open-collector switches used primarily to provide TTL logic levels or to drive low power relays. Provision is made for reading the module's output status or generic code and for disabling all outputs. The module also features a common output fuse and address selection switches.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-11-1 shows the data flow from the D-bus through the module and to the field output connector.

Data Paths

Data lines D(0-7) from the D-bus interface connector provide identical inputs to all four data output registers. One of the registers, as determined by the A0 and A1 signals, accepts a new data byte when DO CLOCK is asserted. The other three registers remain unchanged. From the output registers the data lines go through the output inhibit gates to the output switches. These gates inhibit all outputs when the DBIT is asserted. The on or off status of the individual output switches is determined by which data bits are asserted.

The output circuits are open-collector switches that can be used to drive TTL logic or a variety of other low power dc circuits. Each of these switches is protected from field overvoltages by a zener diode across its output. The common side of all output switches is returned to ground through a common fuse that protects the module from common mode voltage differences between the field power supplies and the module.

The output data lines also go to the input multiplexer where one of the output bytes, as determined by the A0 and A1 signals, can be selected for process monitoring by performing a DATAI on its address. If the GBIT in the CSR of the IOCM is asserted, the module's identity code is read instead of an output byte. The selected input is then gated onto the D-bus by the DI GATE signal. The TBIT signal is not implemented on this module.

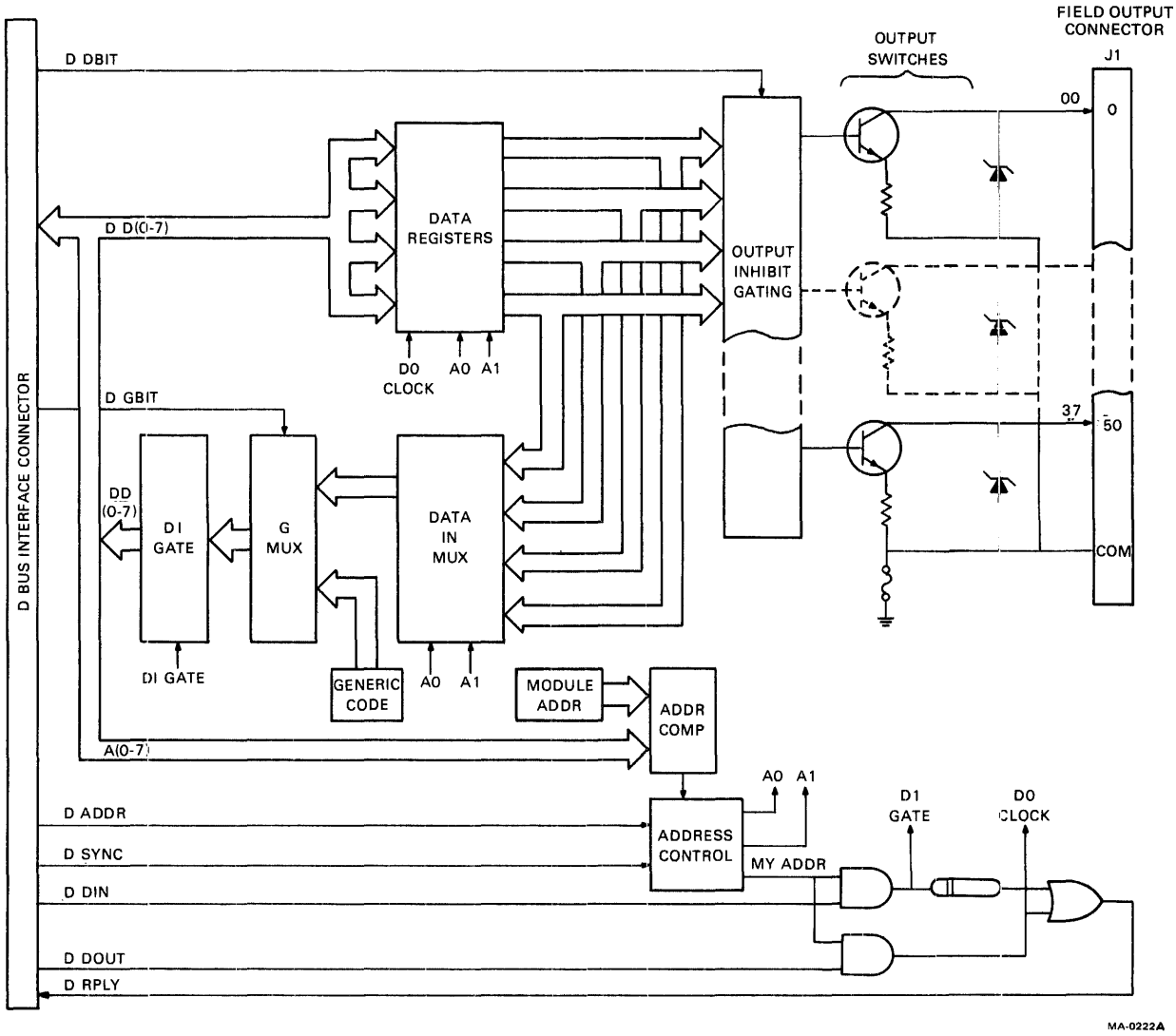


Figure 6-11-1 M6010-YA 32-Bit TTL-Compatible Output Module, Block Diagram

Data Control Signals
Control signals for the previously mentioned data paths are initiated by the program, resulting in the following sequence of operation. When the program calls for an operation requiring a DATAO to one of the module's four addresses, the IOCM starts a D-bus Cycle and causes the address to be put on the D-bus. The module's address decoder decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the module to produce its internal MY ADDRESS signal, as well as the AØ and A1 signals for the selection of the correct data byte. After a short delay, D DOUT is asserted and ANDed with MY ADDRESS to produce DO CLOCK, which strobes the new data byte into the output register. From there it goes to the output gating, output switches, and to J1, the field output connector. DO CLOCK also produces the D RPLY signal, which informs the processor that the data byte has been accepted for output. The processor then negates D DOUT, which negates DO CLOCK.

The status of the output data remains unchanged unless the program outputs to that address. If the program wants to read back the contents of an output register, it causes the processor to execute a DATAI on that address. When this is done, the processor first asserts the address as before and cause the IOCM to start a D-bus Cycle. This causes the address to be put on the D-bus and be decoded by the module's address comparator. Then D SYNC is asserted after a short delay for deskewing. This results in the AØ and A1 signals for selecting the proper byte and also the MY ADDRESS signal. However, in this case, the next signal asserted by the IOCM is D DIN, which is ANDed with MY ADDRESS to produce DI GATE. This signal strobes the contents of the G multiplexer onto the D-bus. If the program has set the GBIT in the CSR of the IOCM, the G multiplexer contains the module's identity code instead of the selected data byte. DI GATE also produces D RPLY after a short delay to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated causing DI GATE to negate and remove data from the D-bus.

Address Selection
The four module addresses must be assigned according to the rules stated in Chapter 4. They are selected on the module by the 8-pole switch, E34 (Figure 6-11-2). An example of one possible address selection is shown in Figure 6-11-3 to illustrate the use of the switch.

Generic Code
The generic code for the M6Ø1Ø-YA module is octal Ø43.

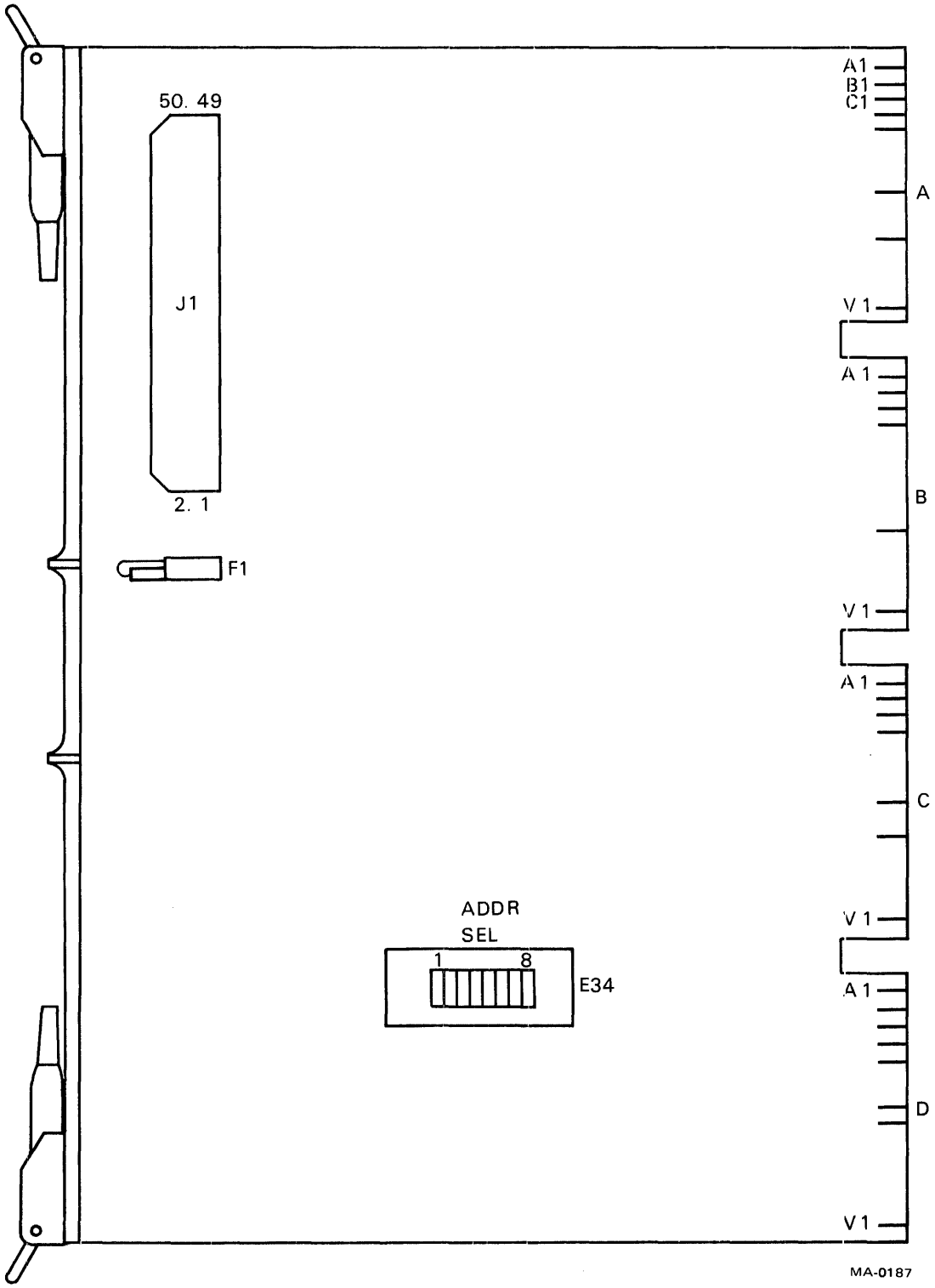


Figure 6-11-2 M6010-YA 32-Bit TTL-Compatible Output Module

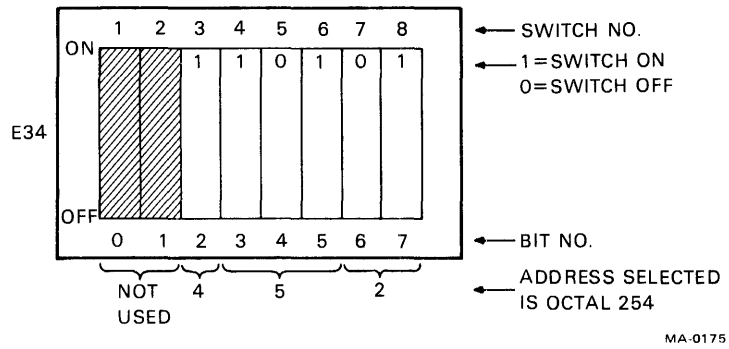


Figure 6-11-3 M6010-YA Address Selection Example

Pin Connections
The M6010-YA module pin connections are shown in Table 6-11-1 for J1, the I/O cable connector.

APPLICATION INFORMATION
Field connections for the M6010-YA module may be implemented with the BC40A screw terminal assembly. Connections are identical to those for the M6010 module listed in Chapter 3, Table 3-2. The user's load must provide pull-up resistors to the supply voltage (+5 V for TTL applications). A typical field interface using screw terminals is shown in Figure 6-11-4.

SPECIFICATIONS

Power requirements

Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS - 0.7) Vdc
Operating current	177 mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 1 mA maximum
Backup supply: 176 mA maximum

Standby current (backup supply)	4 mA maximum

Table 6-11-1 Module M6010-YA I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	00	2	01
3	02	4	03
5	04	6	05
7	06	8	07
9	10	10	11
11	12	12	13
13	14	14	15
15	16	16	17
17	Common	18	Common
19		20	
21		22	
23		24	
25		26	
27		28	
29		30	
31		32	
33	Common	34	Common
35	20	36	21
37	22	38	23
39	24	40	25
41	26	42	27
43	30	44	31
45	32	46	33
47	34	48	35
49	36	50	37

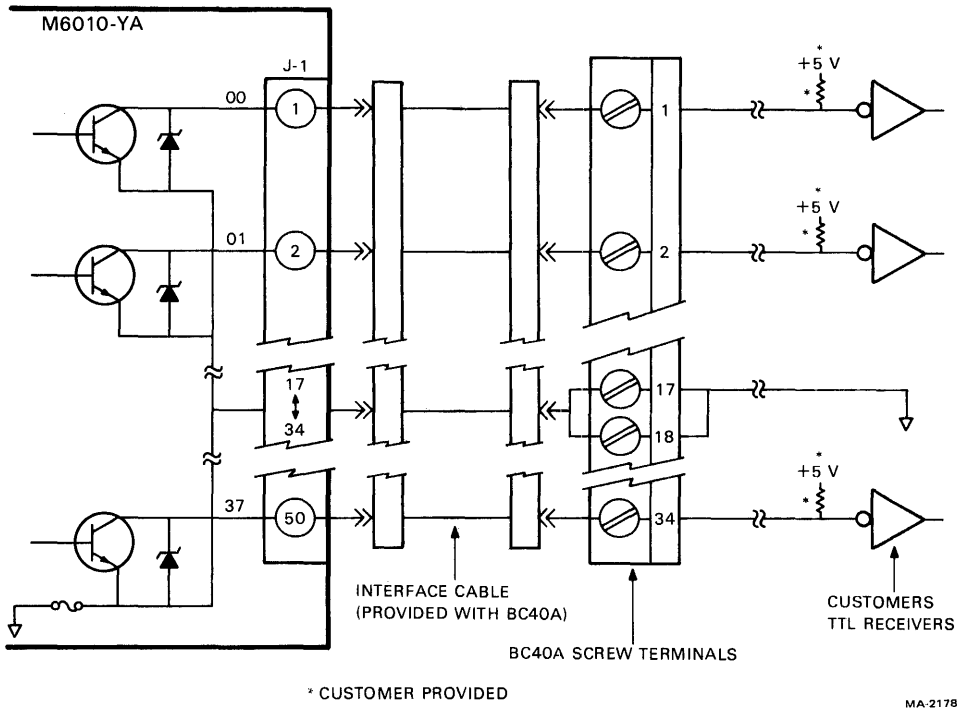


Figure 6-11-4 M6010-YA Typical TTL Field Interface

Output Characteristics

Maximum ratings

High level output voltage: +5 V ±5 percent for TTL loads; +55 V for non-TTL loads

Low level output voltage: +0.4 V

High level leakage current: 20 microamp

Sink current: 64 mA per bit (40 TTL unit loads)

Output timing

Maximum Times (ns)

	V_{out} = 5 V, RL = 78 ohms		V_{out} = 55 V, RL 860 ohms	
Transition	**Propagation Time**	**Transition Time**	**Propagation Time**	**Transition Time**
Zero to one	250	30	300	50
One to zero	1400	240	1600	330

NOTE

Propagation time is referenced to the point where the activating signal enters the module.

Protection	Output circuits are protected from field overvoltage conditions by a 62 V zener diode across each output. Note that this diode will not protect a TTL load, which normally has a maximum input voltage rating of +5.5 V. Common mode protection is provided by a 1 A Picofuse in series with the dc return.
Physical Characteristics	
Dimensions	Quad module, double width, 8-1/2 inch length
Field connector	Cable type BC40A or customer-supplied, 50-pin Berg
Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degrees C ambient
Heat dissipation	8.4 Btu/hr maximum due to module circuits; 2.7 Btu/hr maximum due to field power source

FUNCTIONAL DESCRIPTION

The M6011 module provides 16 program-controlled dc outputs. These outputs are nonisolated, single wire, one shot, open collector, Darlington switches used for operating devices that must be activated for only a short duration, such as relays, solenoid valves, etc. Output timing is selectable from 100 microseconds to 5 seconds on a per-byte basis via switches located on the module. Provision is made for reading the module's output status or generic code and for disabling all outputs. The module also features a common output fuse and switches for address selection.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-12-1 shows that processor output data entering through the D-bus interface connector is addressed and controlled by signals from the D-bus and output to the field through J1. The sequence of control and data flow is as follows.

Data Paths

The eight data lines D(0-7) entering at the D-bus interface connector go to both the address comparator and to the data out latches. Data is strobed into one of the holding registers by the A SET or B SET signal and held for output to the appropriate output register. The output register is clocked by the A SHIFT or B SHIFT signal for the high or low byte, respectively. The holding register is reset at this time so the outputs remain active for only one clock period.

The output circuits are Darlington switches which can be used to turn a variety of dc circuits on or off. Each of these switches is protected from field overvoltages by a zener diode across its output. Additionally, the common side of all output switches is returned to ground through a common fuse which protects the module from common mode voltage differences between the field power supplies and the module.

Data from the holding registers and the output registers is ORed and sent to the Data In multiplexer so that when the processor monitors the status of the output, it receives data corresponding to the logical OR of these two signals. This is desirable because once data is loaded into the holding register, it remains there until it is shifted into the output register where it remains for a full clock period. Once started, this sequence cannot be aborted; therefore, the output status includes the status of both registers.

From the output registers, the data lines go through the output inhibit gates to the output switches. These gates inhibit all outputs when the DBIT is asserted. The on or off status of the individual output switches is determined by which data bits are asserted. The TBIT is not implemented on this module.

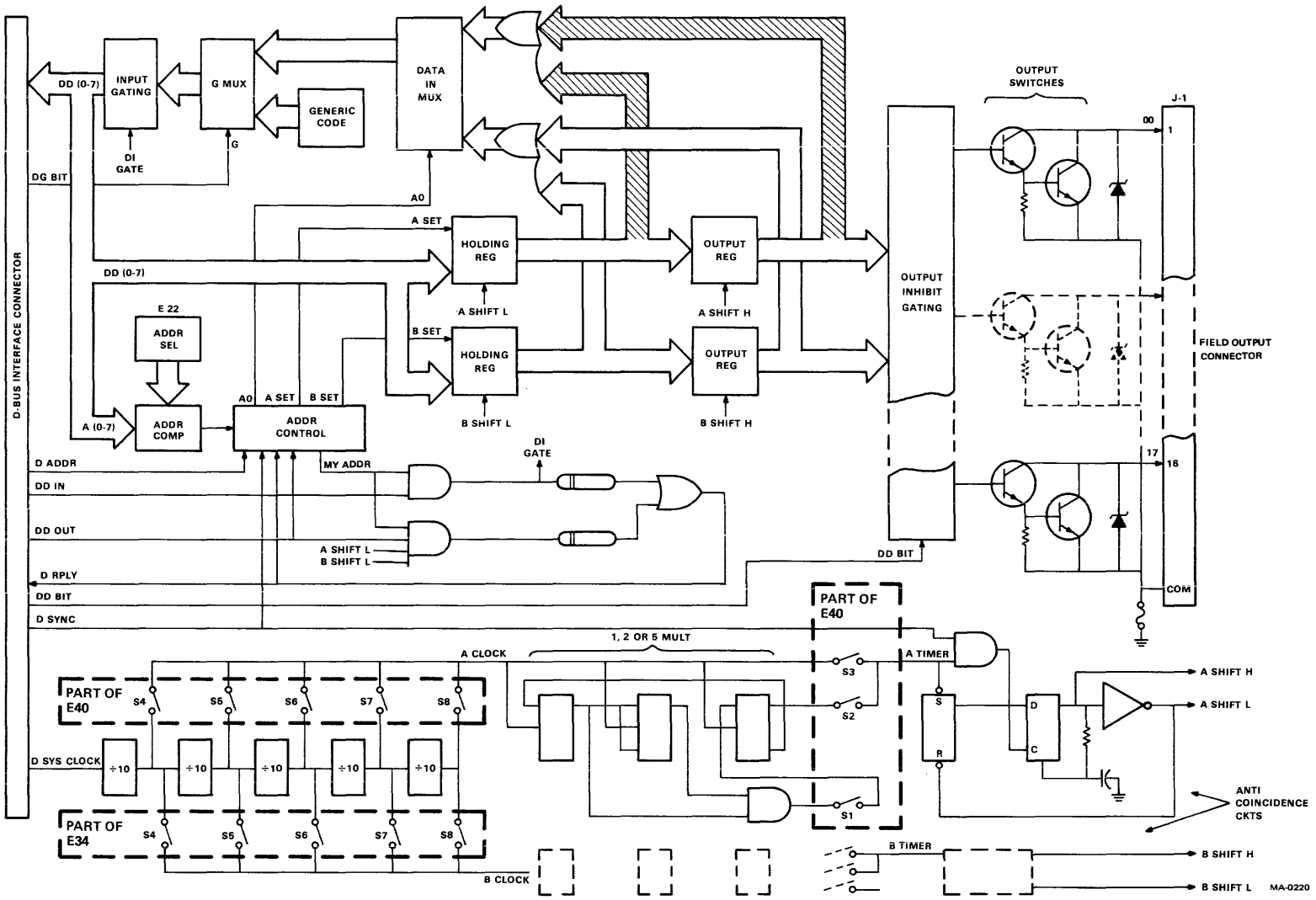


Figure 6-12-1 M6011 16-Bit One-Shot Output
Simplified Block Diagram

Data Control Signals

Control signals for the above mentioned data paths are initiated by the program, resulting in the following sequence of operation. When the program calls for an operation requiring a DATAO to one of the module's two addresses, the IOCM starts a D-bus Cycle and causes the address to be put on the D-bus. The module's address comparator decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the MY ADDRESS and AØ signals. After a short delay, D DOUT is asserted causing either the A SET or B SET signal, depending on the status of AØ. This selects the proper byte for output. D DOUT also produces D RPLY, informing the processor that data for output has been accepted from the D-bus.

The A SHIFT and B SHIFT signals that determine the duration of the output signal are independently adjustable via switches on the module. Figure 6-12-1 shows how these signals are derived (from the 1ØØ kHz D SYS CLOCK with countdown circuits) and selected for the desired interval using switch modules E4Ø and E34. The two circuits, though independent, are identical and operate as follows.

The first part of the divider circuit consists of five successive divide-by-1Ø circuits that multiply the system clock period of 1Ø microseconds to periods of Ø.1, 1, 1Ø, 1ØØ, and 1ØØØ ms (Figure 6-12-2). Any one of five periods may be selected to drive the A TIMER multiplier using one of the five switches (4 through 8) in location E4Ø. Similarly, the B TIMER is selected with the switches in location E34.

The A TIMER multiplier utilizes a 3-stage counter to further multiply the selected time period by either 1, 2, or 5, as selected by switches 1, 2, and 3 of location E4Ø. This provides the 15 different clock periods listed in Table 6-12-1.

Table 6-12-1 One Shot Timing Range

Multiplier	Basic Time (ms) Ø.1	1	1Ø	1ØØ	1ØØØ
x1	Ø.1	1	1Ø	1ØØ	1ØØØ
x2	Ø.2	2	2Ø	2ØØ	2ØØØ
x5	Ø.5	5	5Ø	5ØØ	5ØØØ

Switch usage is illustrated in Figure 6-12-2. One switch (4, 5, 6, 7, or 8) selects the basic time period. A second switch combination (1, 2, or 3) multiplies by 1, 2, or 5.

Since the D-bus Cycle and the one-shot timing are asynchronous, it is possible for the output to be activated just when the holding register is being loaded, resulting in erroneous outputs. This condition is avoided by the anticoincidence circuit (Figure

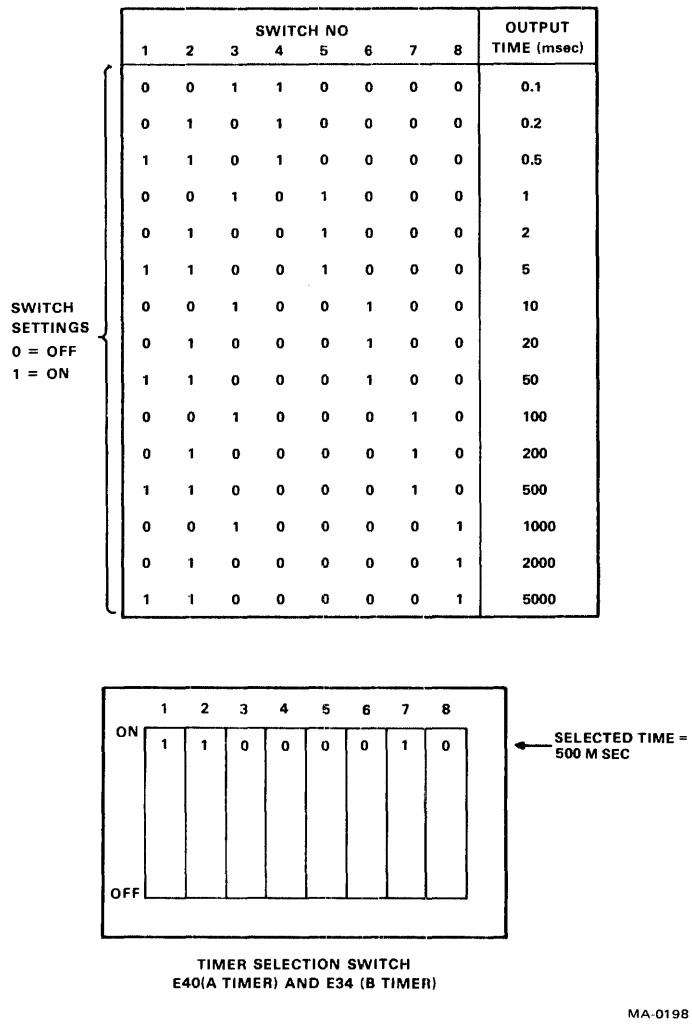


Figure 6-12-2 Timer Selection Switches

6-12-1). The module has two of these circuits; one for the A SHIFT signals and one for the B SHIFT signals, for the high and low bytes, respectively.

The A TIMER clock going low sets the first flip-flop which provides a data input for the second. The second flip-flop is clocked high by the A TIMER clock if D SYNC is not present. The output of this second flip-flop is delayed slightly and resets itself so that the output is a pulse (refer to timing diagram, Figure 6-12-3). This pulse is the A SHIFT H signal that loads the output register. The A SHIFT H signal is inverted to provide the A SHIFT L signal that clears the holding register. The inversion also provides delay so that the holding register is not cleared until after the output register is loaded. When the output register is clocked by the next A SHIFT H pulse, its data inputs are all low, so the outputs are reset. Thus, the asserted outputs for that byte have been activated for one A TIMER clock period.

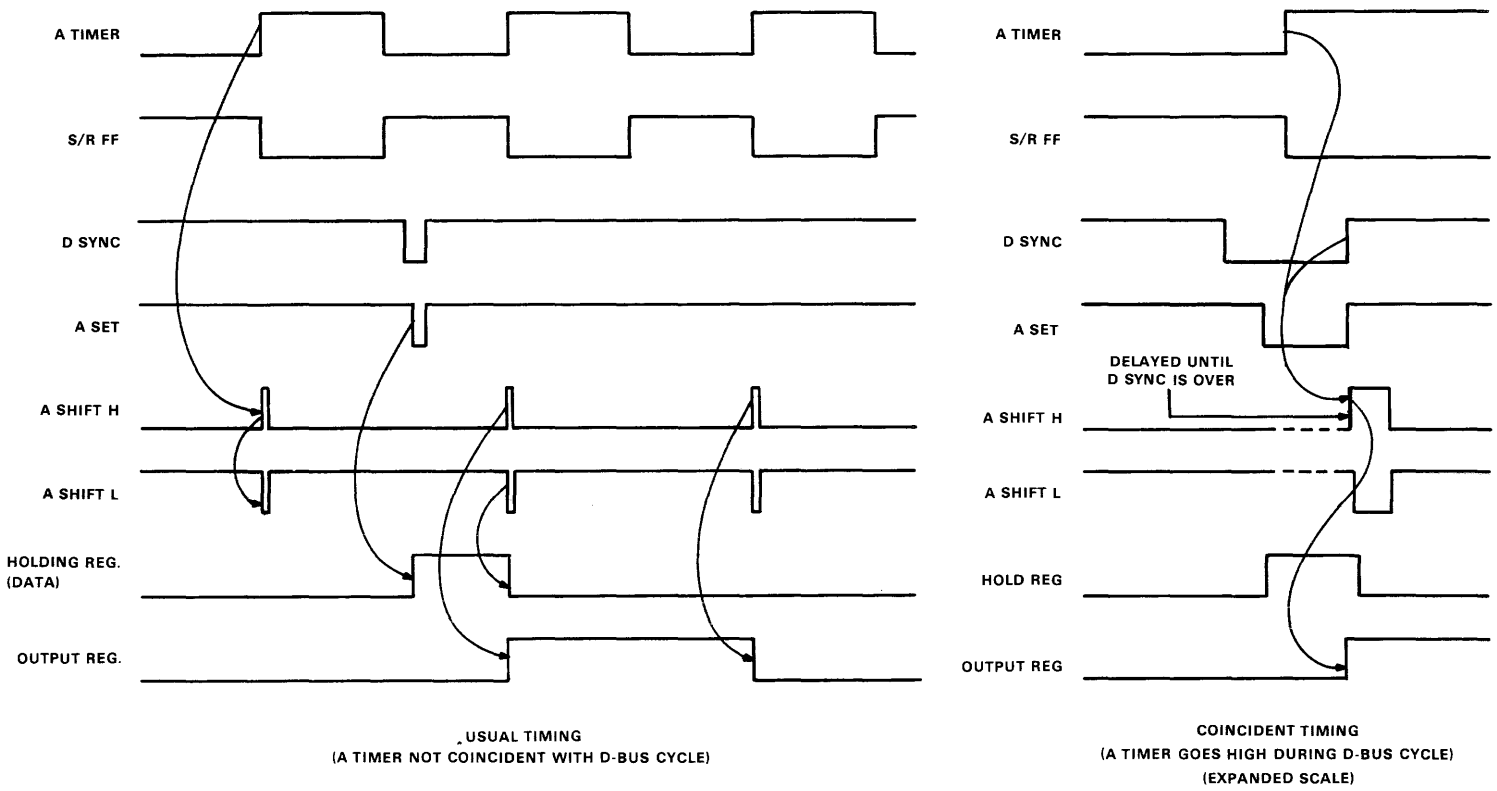


Figure 6-12-3 Anticoincidence Timing Diagram

The shift signals are disabled by the SYNC L signal which occurs during a D-bus Cycle. Thus, the holding register can be loaded, but the output register is not loaded until the end of the D-bus Cycle. This means the assertion of the outputs may be delayed as long as one D-bus Cycle.

The data registers can be monitored by causing the processor to perform a DATAI during the output interval. If this is done, the processor will first assert the address, as before, and cause the IOCM to start a D-bus Cycle. This causes the address to be put on the D-bus and decoded by the module's address comparator. Then, D SYNC is produced after a short delay for deskewing, resulting in the AØ and MY ADDRESS signals. The AØ signal selects the proper byte from the DATA IN MUX. This time, the next signal asserted by the IOCM will be D DIN, which is ANDed with MY ADDRESS to produce DI GATE. DI GATE strobes the contents of the G Mux onto the D-bus. If the processor has set the GBIT in the CSR of the IOCM, the contents of the G multiplexer will be the module's identity code instead of the selected data byte. DI GATE also produces D RPLY after a short delay, to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated causing DI GATE to negate and remove data from the D-bus.

Address Selection
The two addresses for the module must be assigned according to the rules stated in Chapter 4 and are selected on the module by the 8-pole switch, E-22 (Figure 6-12-4). An example of one possible address selection is shown in Figure 6-12-5 to illustrate the use of this switch.

Generic Code
The generic code for the M6Ø11 module is octal Ø21.

Pin Connections
The M6Ø11 module pin connections are shown in Table 6-12-2 for J1, the I/O cable connector.

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc
Operating current	78.2 mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 2.3 mA maximum
Backup supply: 75.9 mA maximum

Standby current (backup supply)	33.7 mA maximum

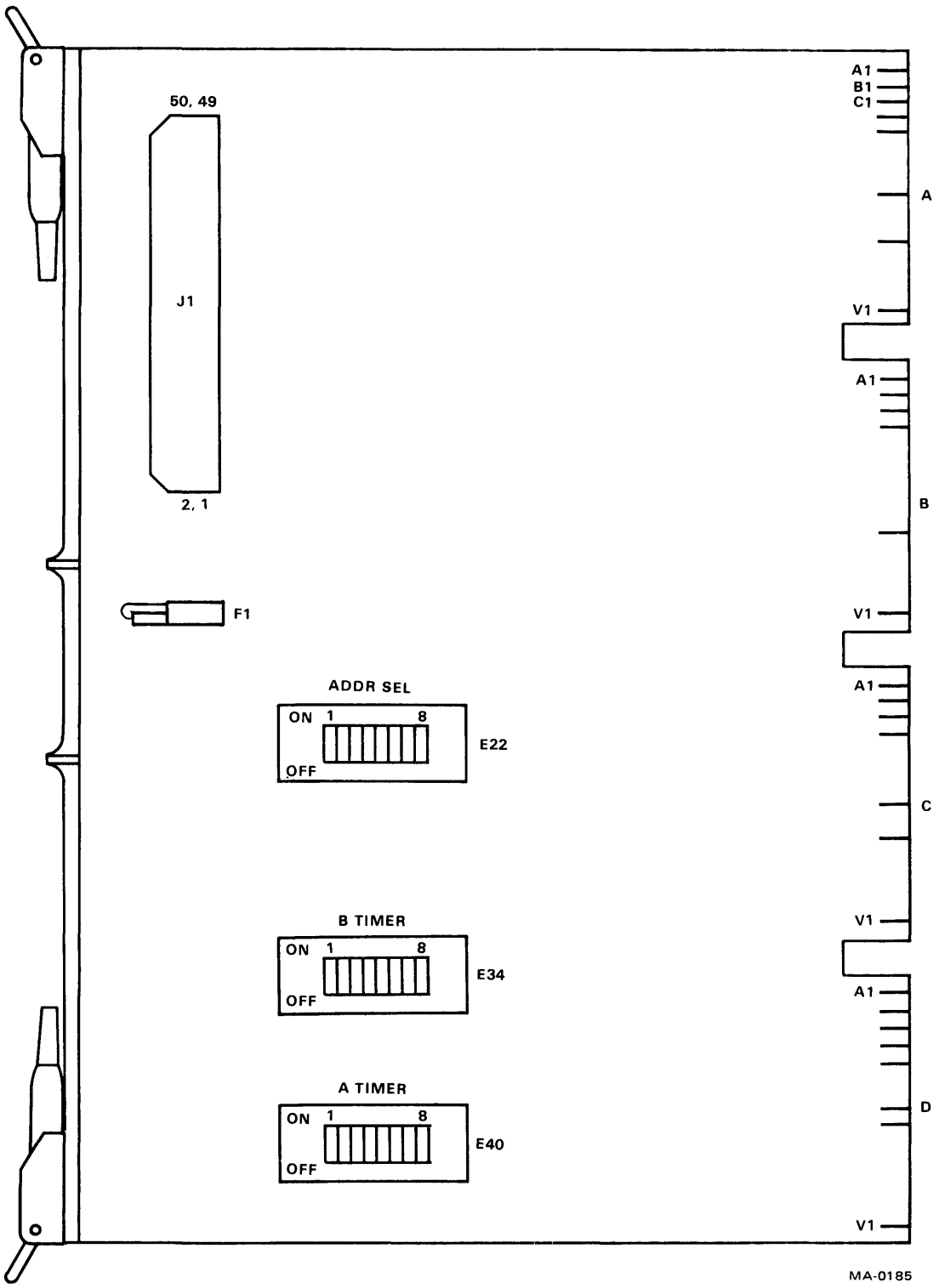


Figure 6-12-4 M6Ø11 16-Bit One Shot Output

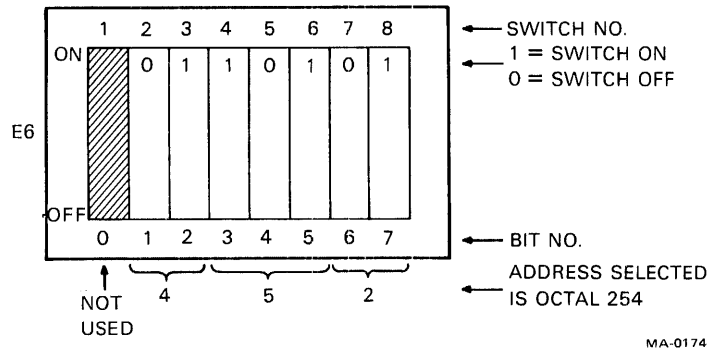


Figure 6-12-5 Address Selection Switch

Table 6-12-2 Module M6011 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	ØØ	2	Ø1
3	Ø2	4	Ø3
5	Ø4	6	Ø5
7	Ø6	8	Ø7
9	1Ø	1Ø	11
11	12	12	13
13	14	14	15
15	16	16	17
17	Common	18	Common
19	↑	2Ø	↑
21	|	22	|
23	|	24	|
25	|	26	|
27	|	28	|
29	|	3Ø	|
31	|	32	↓
33	Common	34	Common
35		36	
37		38	
39		4Ø	
41		42	
43		44	
45		46	
47		48	
49		5Ø	

Output Characteristics

Maximum ratings

Positive output voltage: +55 V
Negative output voltage: -Ø.6 V
Low voltage output: +1.4 V
Off leakage current: 2Ø microamp
Sink current: 25Ø mA per bit, 4 A per module

Output timing

Maximum Times (microseconds)

	V_{out} = 12 V, RL = 1ØK		V_{out} = 55 V, RL = 3.5K	
Transition	**Propagation Time**	**Transition Time**	**Propagation Time**	**Transition Time**
Turn-on	Ø.8	Ø.Ø5	Ø.8	Ø.Ø5
Turn-off	3.6	3.9	1.8	2.4

NOTE
Propagation time is referenced to the point where the activating signal enters the module.

One-shot timing range: 1ØØ microseconds to 5 sec ± (Ø.1 percent + 5 microseconds) switch-selectable on module

Protection

Output circuits are protected from field overvoltage conditions by a zener diode across each output. Common mode protection is provided by a 1 A Picofuse in series with the dc return

Physical Characteristics

Dimensions: Quad module, triple width, 8-1/2 inch length

Field connector: Cable type BC4ØA or customer-supplied, 5Ø-pin Berg

Environmental Characteristics

Complies with DEC STD 1Ø2 Class C. Operates in convection cooled environment up to 6Ø degrees C ambient

Heat dissipation: 3.83 Btu/hr maximum due to module circuitry; 18.58 Btu/hr maximum due to field power source

FUNCTIONAL DESCRIPTION

The M6Ø12 module provides eight program-controlled dc outputs. These outputs are isolated, three-wire, open-collector, Darlington switches used for controlling solenoid valves, relays, indicators, heaters, etc., where isolation from the controlled process must be maintained. Provision is made for reading the module's output status, generic code, and for disabling all outputs. The module also features individual output indicators and fuses, and address selection switches.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-13-1 shows that processor output data entering through the D-bus interface connector is addressed and controlled by signals from the D-bus and is output to the field through J1. The sequence of control and data flow is as follows.

Data Paths

The eight data lines D(Ø-7) entering at the D-bus interface connector go to both the address comparator and the data output register. The data output register, controlled by the MY ADDRESS and D DOUT signals, provides the output data to the output inhibit gating section. The output of this section, if not disabled by the DBIT signal, goes to the isolators and then to the eight LED indicators and output switches. Power for everything after the isolators is input from the field through J1 on the field common lines. The TBIT is not implemented on this module.

The output circuits are Darlington switches that can be used to turn a variety of dc circuits on or off. Each of these switches is protected from field overvoltages by a zener diode across its output and from inductive spikes by a diode clamp to the plus field supply. Additionally, each output is protected from field current overload conditions by a series fuse.

The state of the data output register can be read by means of the G multiplexer, which under control of the GBIT signal, selects either the output data or the module's identity code. This data is then strobed onto the D-bus by the DI GATE signal.

Data Control Signals

Control signals for the above mentioned data paths are initiated by the program, resulting in the following sequence of operation. When the program calls for an operation requiring a DATAO to the module, the IOCM starts a D-bus Cycle and causes the module's address to be put on the D-bus. The module's address comparator decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the module's address control section to produce the MY ADDRESS signal which enables the data output register. After a short delay, D DOUT is asserted to load the data into the output register. The register outputs drive the output

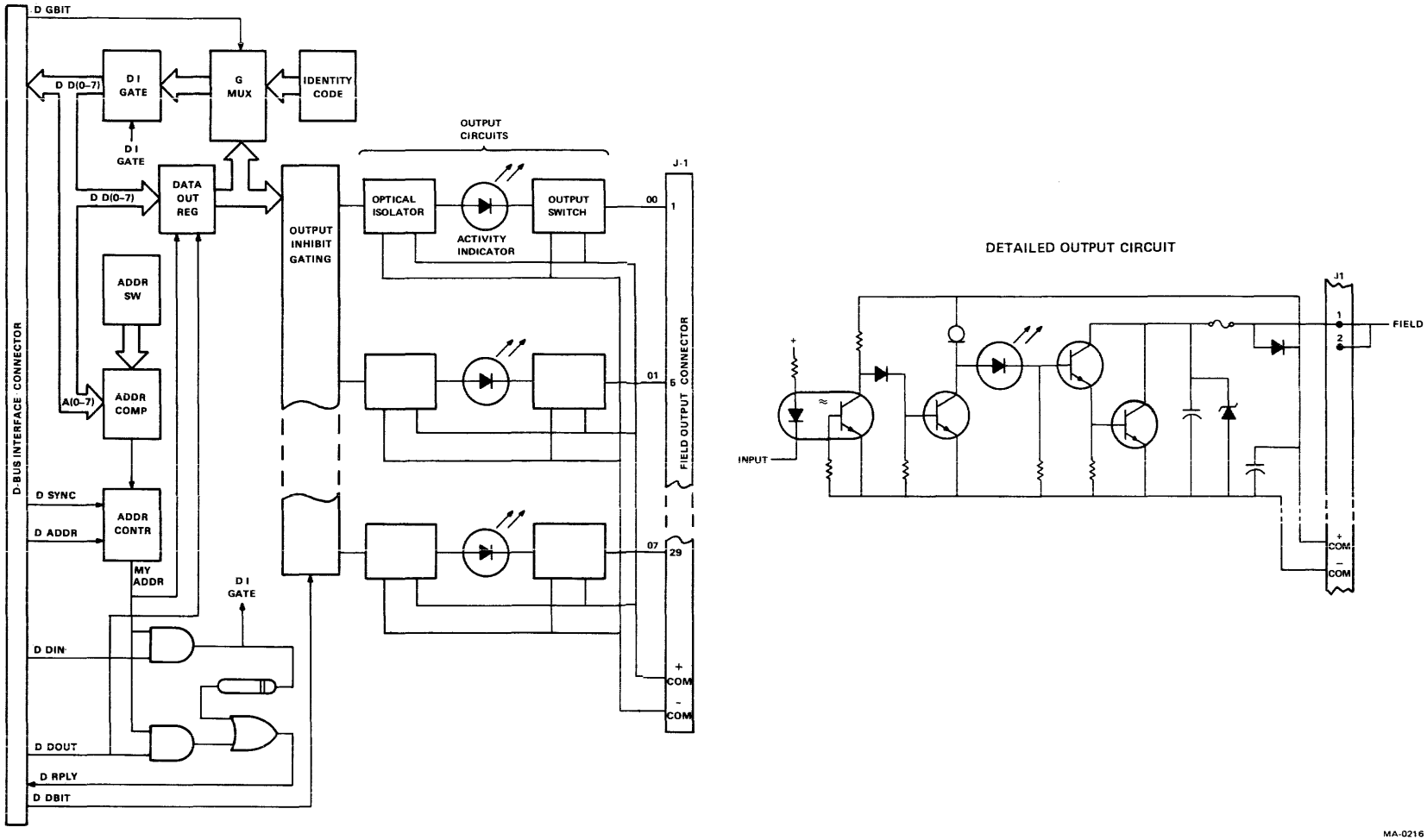


Figure 6-13-1 M6Ø12 8-Bit Isolated DC Output Module

inhibit gating, output switches, indicators, and J1, the output connector. D DOUT is also ANDed with MY ADDRESS to produce D RPLY, which informs the processor that the data has been accepted for output. The processor then negates D DOUT.

Output data remains unchanged unless the processor outputs a new data byte to that address. If the program wants to monitor that data, it causes the processor to perform a DATAI on that address. When this is done, the processor first asserts the address as before and causes the IOCM to start a D-bus Cycle. This causes the address to be put on the D-bus and to be decoded by the module's address comparator. Then D SYNC is asserted after a short delay for deskewing, resulting in the MY ADDRESS signal. However, in this case, the next signal asserted by the IOCM is D DIN, which is ANDed with MY ADDRESS to produce DI GATE. This signal strobes the contents of the G multiplexer onto the D-bus. If the program has set the GBIT in the CSR of the IOCM, the G multiplexer contains the module's identity code instead of output data. DI GATE also produces D RPLY after a short delay to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated, causing DI GATE to negate and remove data from the D-bus.

Address Selection
The single module address must be assigned according to the rules stated in Chapter 4. It is selected on the module by the 8-pole switch, E2Ø (Figure 6-13-2). An example of one possible address selection is shown in Figure 6-13-3 to illustrate the use of this switch.

Generic Code
The generic code for the M6Ø12 module is octal ØØ1.

Pin Connections
The M6Ø12 module pin connections for J1, the I/O cable connector are shown in Table 6-13-1.

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc $\pm$ 2 Vdc Backup supply: 14 Vdc $\geq$ VB $\geq$ (VS-Ø.7) Vdc
Operating current	2Ø2 mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 1.4 mA maximum
Backup supply: 2ØØ mA maximum

Standby current (backup supply)	2.3 mA maximum

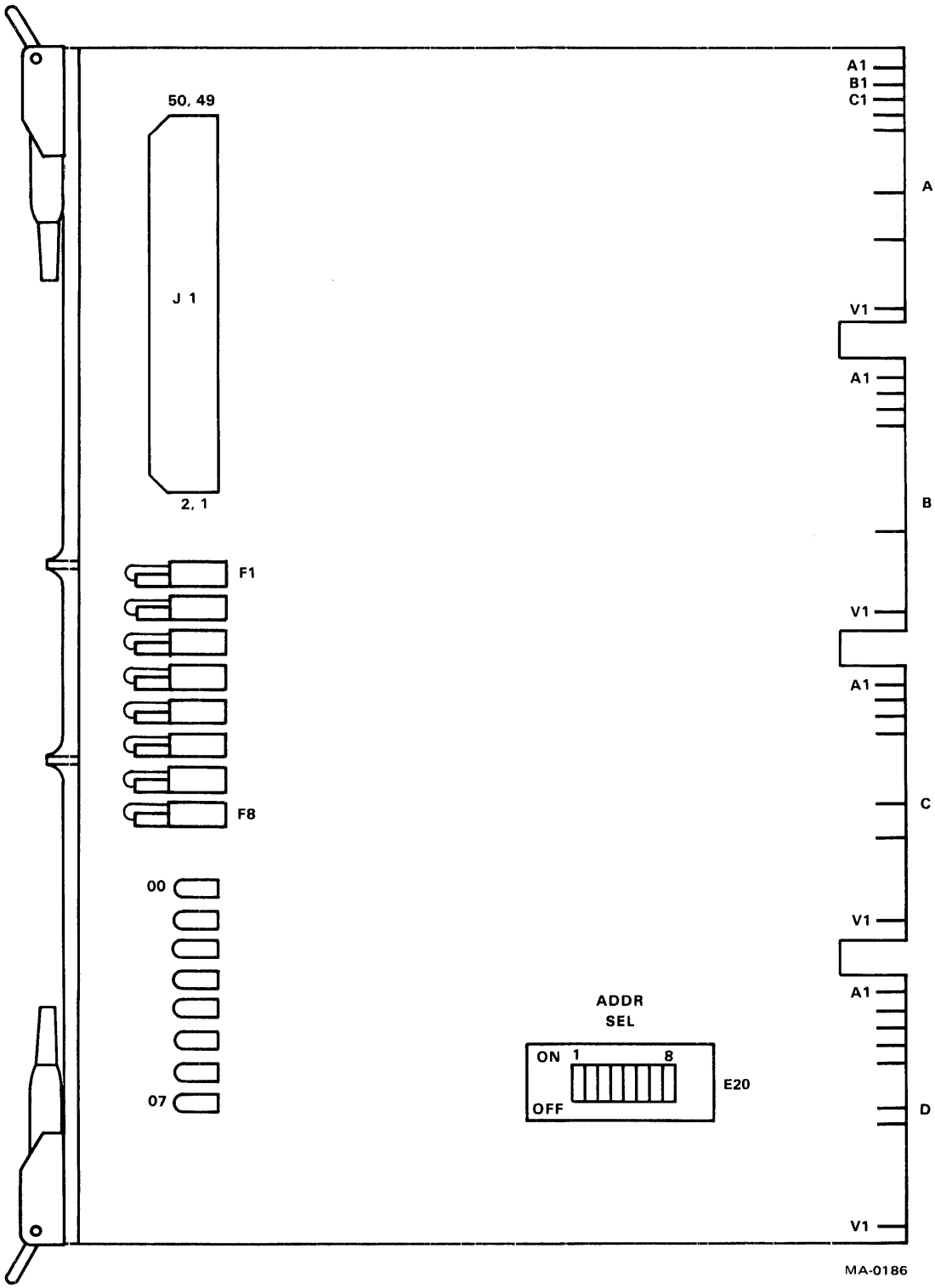


Figure 6-13-2 M6Ø12 8-Bit Isolated DC Output

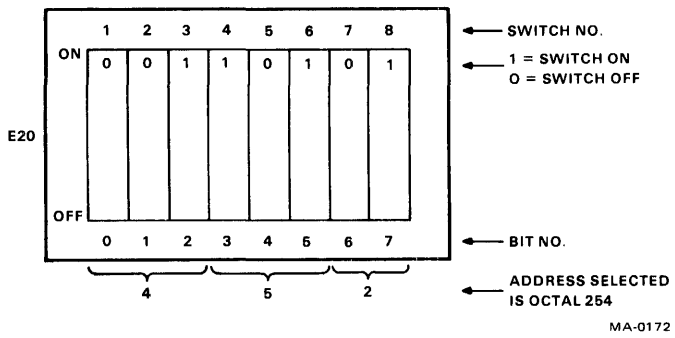


Figure 6-13-3 Address Selection Switch

Table 6-13-1 Module M6012 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	0	2	0
3		4	
5	1	6	1
7		8	
9	2	10	2
11		12	
13	3	14	3
15		16	
17	4	18	4
19		20	
21	5	22	5
23		24	
25	6	26	6
27		28	
29	7	30	7
31		32	
33, 35, 37, 39	Field +	34, 36, 38, 40	Field +
41		42	
43, 45, 47, 49	Field -	44, 46, 48, 50	Field -

Output Characteristics

Maximum ratings

Positive output voltage: +55 V

Negative output voltage: -Ø.6 V

Low voltage output: +1.8 V

Off leakage current: 2Ø microamp

Sink current: 1 A/bit, 4 A/module

Isolation voltage: 1ØØØ V output to ground - outputs not isolated from each other

Common mode source: 2ØØ VA

Field power supply current: 56 mA/module

Output timing

Maximum Times (microseconds)

Transition	V_{out} = 12 V, RL = 1ØK		V_{out} = 55 V, RL = 3.5K	
	Propagation Time	**Transition Time**	**Propagation Time**	**Transition Time**
Turn-on	8.6	Ø.1	12.6	Ø.2
Turn-off	45	56	24	2Ø

NOTE

Propagation time is referenced to the point where the activating signal enters the module.

Protection

The output circuits are protected from field overvoltage conditions by a zener diode across each output, and from inductive spikes by the clamping diode to the field power supply.

Output overload protection is provided by a 2 A fuse in series with each output. This fuse protects the module circuitry in case of a moderate overload, but can only protect the circuit board in the event of a shorted load.

Physical Characteristics	
Dimensions	Quad module, triple width, 8-1/2 inch length
Field connector	Cable type BC4ØB or customer-supplied, 5Ø-pin Berg
Environmental Characteristics	Complies with DEC STD 1Ø2 Class C. Operates in convection cooled environment up to 6Ø degrees C ambient
Heat dissipation	9.24 Btu/hr maximum due to module circuitry; 2.Ø2 Btu/hr maximum due to field power source

FUNCTIONAL DESCRIPTION

The M6Ø13 module provides eight program-controlled ac outputs. These outputs are transformer-isolated, three-wire, switches used for controlling alarms, machinery, pumps, blowers, etc. Provision is made for reading the module's output status, generic code, and for disabling all outputs. The module also features individual output indicators and fuses, and address selection switches.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-14-1 shows that processor output data entering through the D-bus interface connector is addressed and controlled by signals from the D-bus and is output to the field through J1. The sequence of control and data flow is as follows.

Data Paths

The eight data lines D(Ø-7) entering at the D-bus interface connector go to both the address comparator and the data output register. The data output register, controlled by the MY ADDRESS and D DOUT signals, provides data to the output inhibit gating section. The output of this section, if not disabled by the DBIT signal, provides output data to the output switch control oscillators that control the eight output switches. All power and output lines after the switch control transformers are electrically isolated from the rest of the module. The output switches go to J1, the output field connector.

The state of the data output register can be read by the G multiplexer, which under control of the GBIT signal, selects either output data or the module's identity code. This data is then strobed onto the D-bus by the DI GATE signal. The TBIT signal is not implemented for this module.

Data Control Signals

Control signals for the above mentioned data paths are initiated by the program, resulting in the following sequence of operation. When the program calls for an operation requiring a DATAO to the module, the IOCM starts a D-bus Cycle and causes the module's address to be put on the D-bus. The module's address comparator decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the MY ADDRESS signal that enables the data output register. After a short delay, D DOUT is asserted which strobes data out to the output inhibit gate, oscillators, transformers, output switches, and J1, the output connector. D DOUT is also ANDed with MY ADDRESS to produce D RPLY, which informs the processor that the data byte has been accepted for output. The processor then negates D DOUT.

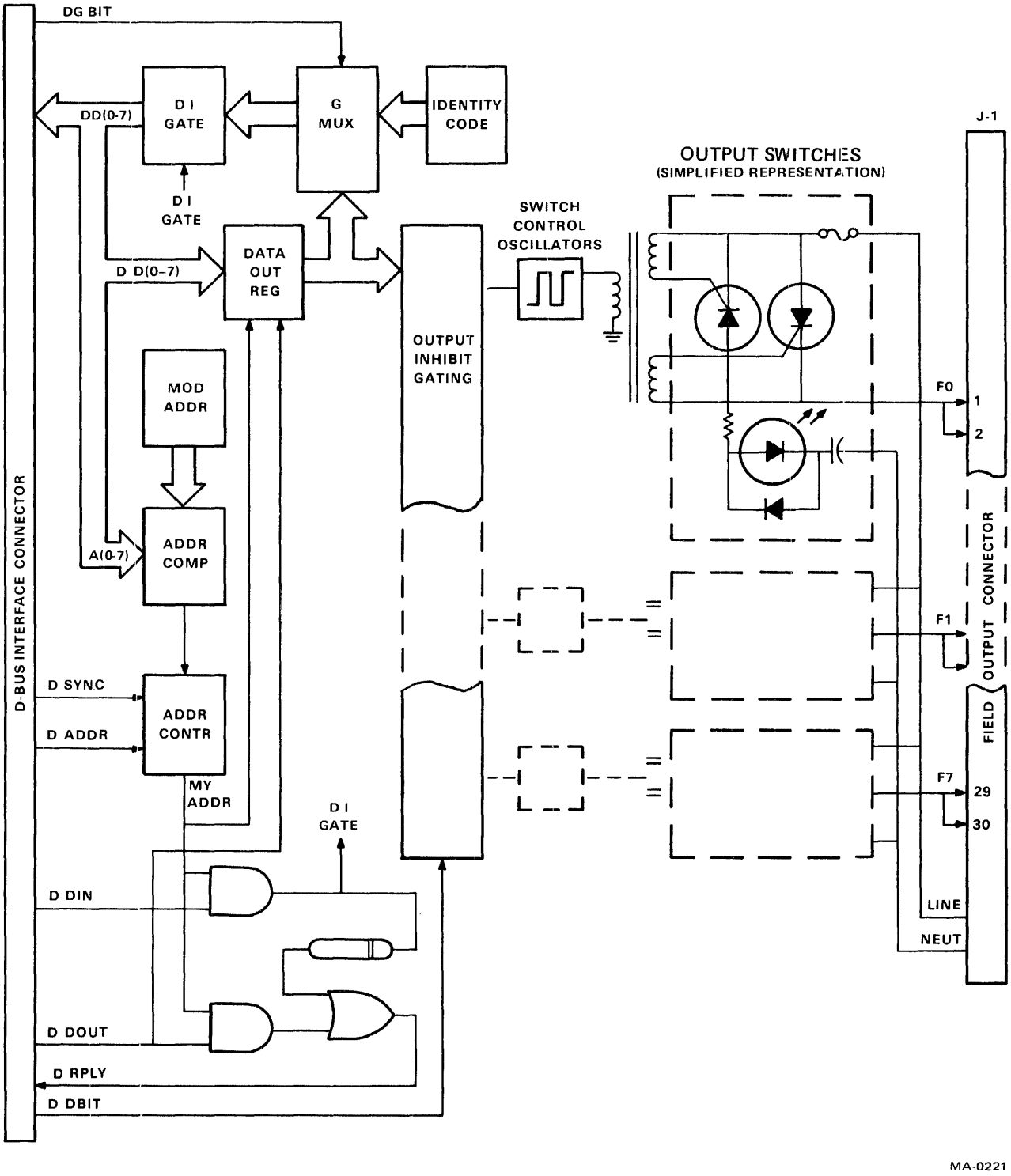


Figure 6-14-1 M6013 8-Bit AC Output Module

Output data remains unchanged unless the processor outputs a new data byte to that address. If the program wants to monitor that data, it causes the processor to perform a DATAI on that address. When this is done, the processor first asserts the address as before and causes the IOCM to start a D-bus Cycle. This causes the address to be put on the D-bus and decoded by the module's address comparator. Then D SYNC is asserted after a short delay for deskewing, resulting in the MY ADDRESS signal. However, in this case the next signal asserted by the IOCM is D DIN, which is ANDed with MY ADDRESS to produce DI GATE. This signal strobes the contents of the G multiplexer onto the D-bus. If the program has set the GBIT in the CSR of the IOCM, the G multiplexer contains the module's identity code instead of the output data. DI GATE also produces D RPLY after a short delay to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated, causing DI GATE to negate and remove data from the D-bus.

Output Switch Operation

The processor activates any or all output switches by writing a data word to the module's address. Any bit that is asserted has its corresponding output ac switch activated to turn on its assigned field device.

A simplified schematic of one of these switches and its control circuit is shown in Figure 6-14-2. The switch is implemented with two SCRs (silicon controlled rectifiers) which become activated by the 555 oscillator signal whenever its control bit is asserted. When the applied ac field signal forward biases one of the SCRs, and its gate input is positive with respect to its cathode, the SCR turns on and remains turned on as long as it is forward-biased, which is one-half cycle of the ac field voltage. On alternate half cycles, the other SCR conducts to provide a conducting path for an ac current.

Activity of the output switch is indicated by a LED circuit which is also turned on by the switch. The switch is protected from excessive current loads by a series fuse and from overvoltage transients by a MOV (metal oxide varistor). The fuse only protects the circuit board (not the module components) in event of a shorted load.

WARNING

The series fuse that protects the output circuit is a special part. If replacement of the fuse is necessary, it must be replaced with DEC part number 12-12442. DO NOT SUBSTITUTE. Replacement with other than the specified fuse may result in personal injury, equipment damage, or improper operation. A spare fuse holder and fuse is provided on the module to ensure that a replacement is always conveniently available.

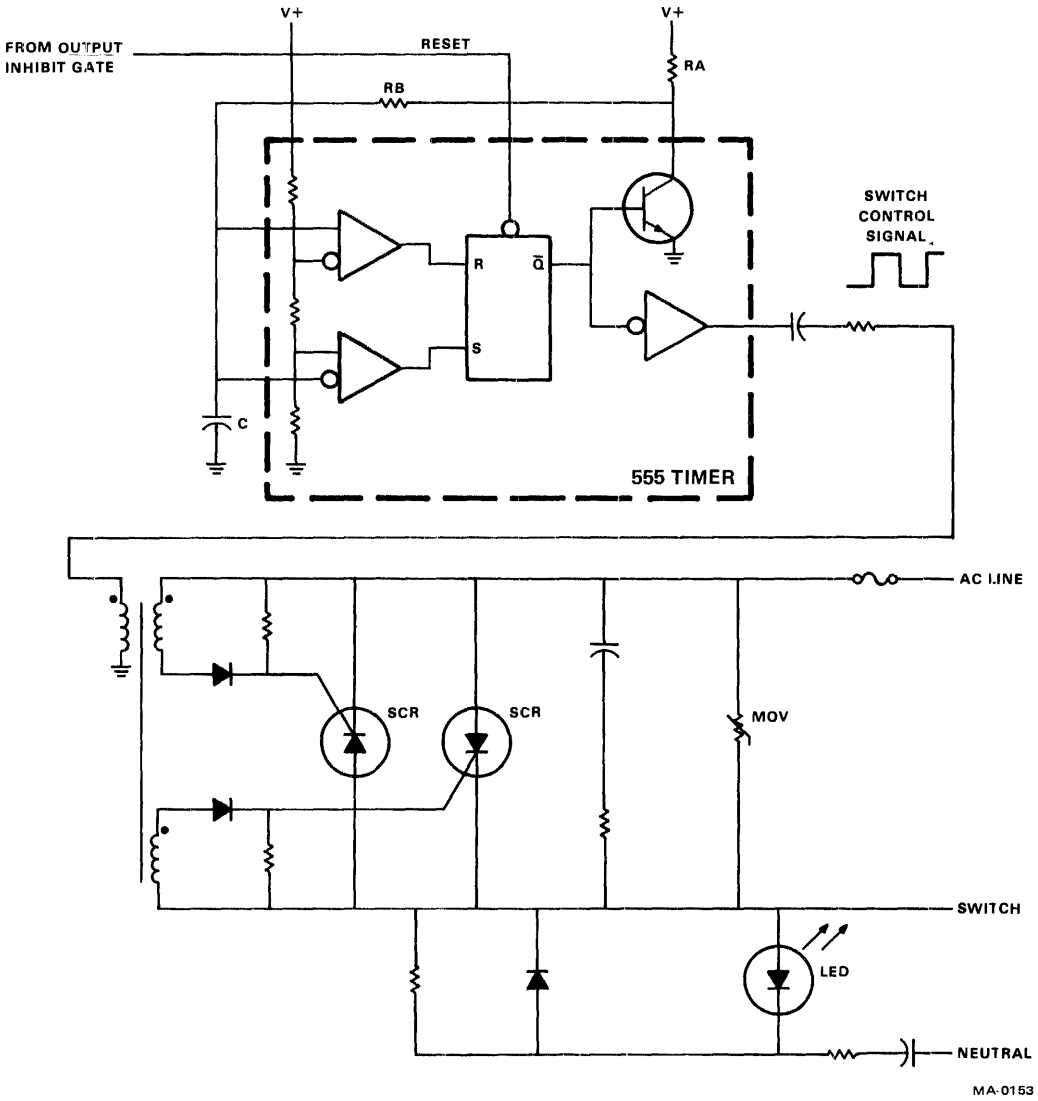


Figure 6-14-2 Output Switch and Control Oscillator

Address Selection

The single module address must be assigned according to the rules stated in Chapter 4. It is selected on the module by the 8-pole switch, E1 (Figure 6-14-3). An example of one possible address selection is shown in Figure 6-14-4 to illustrate the use of this switch.

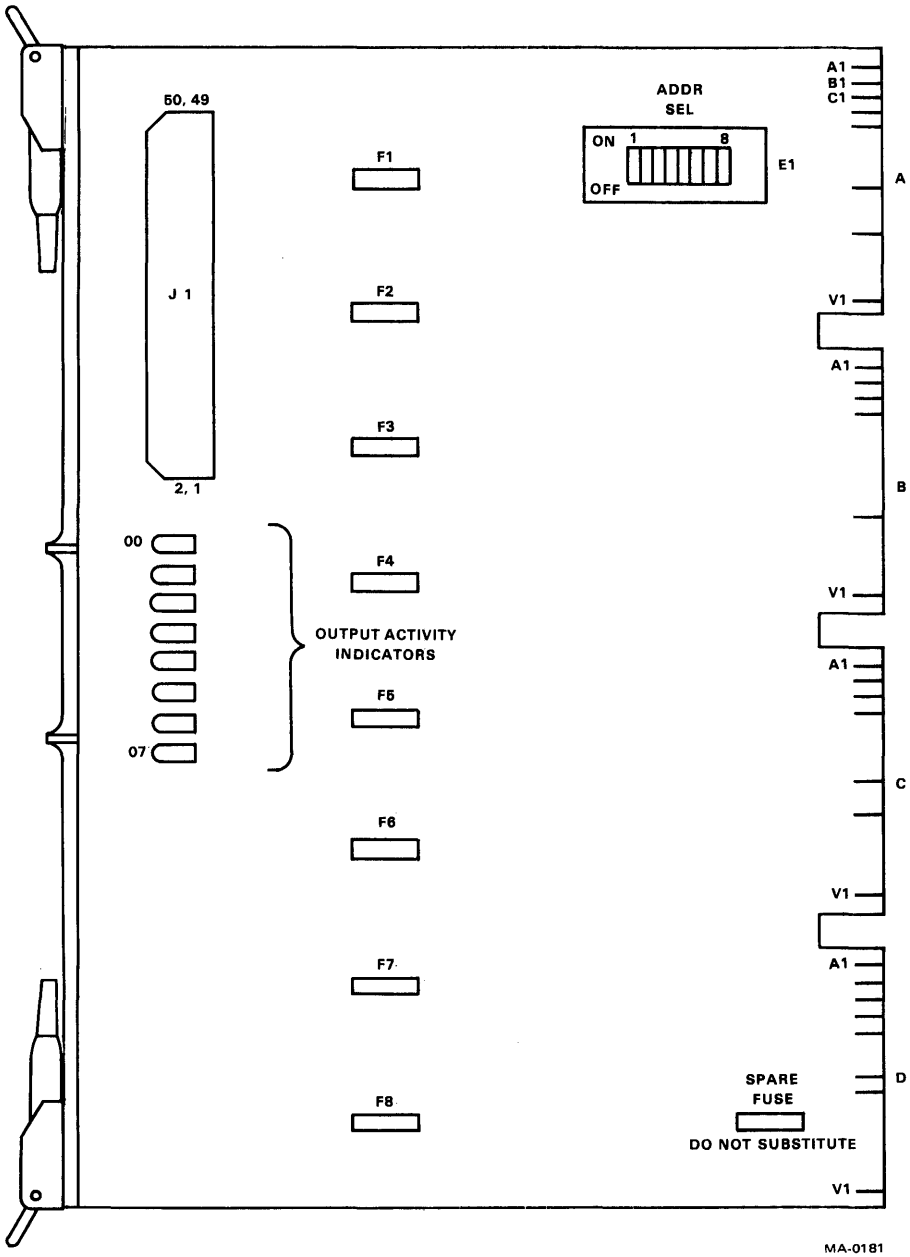


Figure 6-14-3 M6Ø13 8-Bit AC Output

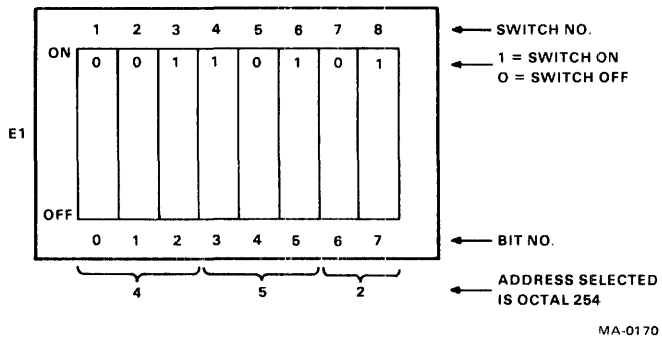


Figure 6-14-4 Address Selection Switch

Generic Code
The generic code for the M6Ø13 module is octal ØØ2.

Pin Connections
The M6Ø13 module pin connections for J1, the I/O cable connector are shown in Table 6-14-1.

Table 6-14-1 Module M6Ø13 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	Ø	2	Ø
3		4	
5	1	6	1
7		8	
9	2	1Ø	2
11		12	
13	3	14	3
15		16	
17	4	18	4
19		2Ø	
21	5	22	5
23		24	
25	6	26	6
27		28	
29	7	3Ø	7
31	Field ac line	32	Field ac line
33		34	
35		36	
37		38	
39		4Ø	
41		42	
43	Field ac neutral	44	Field ac neutral
45		46	
47		48	
49		5Ø	

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc
Operating current	173 mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 17Ø mA maximum
Backup supply - 3 mA maximum

Standby current (backup supply)	3 mA maximum

Output Characteristics

Line voltage	12-14Ø Vac @ 47-63 Hz
Operating current	38 mA minimum 2 A maximum per bit 8 A maximum per module
Surge current	3Ø A rms maximum for 32 ms Minimum time between surges = 1Ø seconds

NOTE
Output will not be damaged if turned on by overvoltage or dv/dt, provided maximum current ratings have not been exceeded.

On-state voltage	1.3 V maximum @ 2 A
Isolation voltage	15ØØ Vrms from output to ground The outputs are not isolated from each other
Notch voltage	5.4 V maximum
Turn-on time	54 microseconds maximum
Turn-off time	One-half line voltage cycle maximum

Protection

Overvoltage	Metal oxide varistor (MOV)
Overcurrent	Fuse: DEC part no. 12-12442 Do not substitute

Over-dissipation	Flameproof resistors in circuit where other component failure could cause over-dissipation
Physical Characteristics	
Dimensions	Quad module, triple width, 8-1/2 inch length
Field connector	Cable type BC40B or customer-supplied, 50-pin Berg
Indicators	LED indicators light when field circuit is on and ac voltage is greater than 90 Vac
Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degrees C ambient
Heat dissipation	7.55 Btu/hr maximum due to module circuitry; 34.3 Btu/hr maximum due to field power source

FUNCTIONAL DESCRIPTION

The M6Ø14 output counter provides two independent program controlled pulse train outputs for operating synchros, stepping switches, or other incremental devices. Pulse train frequency and duty cycle are switch-selectable; ranges are from 1Ø kHz to Ø.2 Hz and from 1Ø to 8Ø percent respectively. Sign/direction and enable outputs are also provided. All outputs are single wire, nonisolated, TTL compatible, open collector, high voltage switches. Provision is made for reading the module's generic code and for disabling all outputs. The module also features a common output fuse and switches for address selection.

GENERAL DESCRIPTION

The M6Ø14 consists of two counters for controlling output pulse train lengths, two frequency and duty cycle select circuits, and a common generator that produces the necessary frequencies for both outputs (Figure 6-15-1). A common isolated input allows the user to connect his own frequency source.

DETAILED DESCRIPTION

The module consists of two printed circuit boards assembled in a mother-daughter configuration (Figure 6-15-2). The heavy dashed line in Figure 6-15-1 shows the module's circuits divided between the two circuit boards. The mother board (G67Ø) contains the counters, data paths, and interrupt logic. The daughter board (54-13587) contains a common frequency source, frequency and duty cycle select circuits, output control circuits, and the output switches.

The M6Ø14 counters control the number of pulses produced by the module's PULSE outputs. To have one of these outputs produce n pulses, the program simply writes the number n into the appropriate counter. This action enables the PULSE output and a series of pulses is started. Each pulse causes the counter to decrement; when the counter reaches zero, the pulses stop and an interrupt is generated. The M6Ø14 counters operate as 15-bit down counters and can therefore produce up to 32,767 pulses per output word.

Mother Board

For a discussion of the mother board circuits, refer to the section on the M5Ø14 input counter, which uses the same G67Ø mother board.

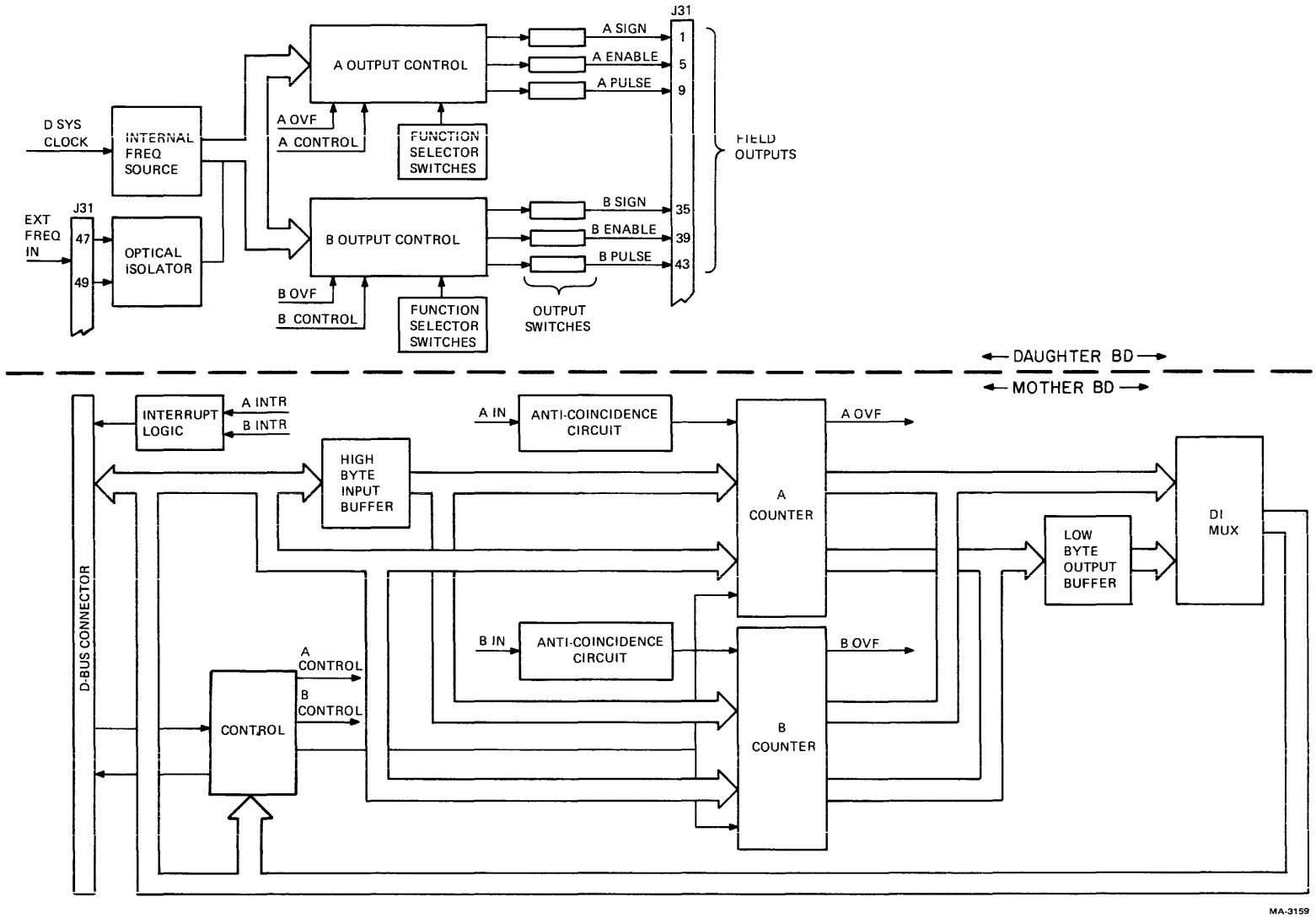


Figure 6-15-1 M6014 Dual Output Counter, Block Diagram

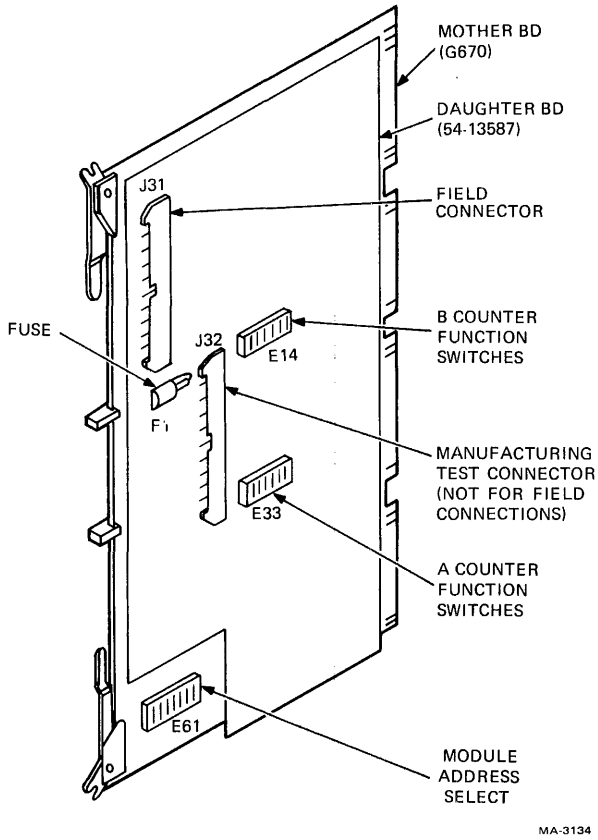


Figure 6-15-2 M6Ø14 Counter Module

Daughter Board

The M6Ø14 counter module uses the 54-13587 daughter board which provides two independent, program-controlled, pulse train outputs. Frequency and duty cycle of the outputs are preselected by the user via switches on the module. Outputs are initiated by the program and controlled by the counters on the mother board.

The daughter board contains a single internal frequency source that derives 15 frequencies from the system clock for selection by the user. An additional selection is available from an external source so that the user has the option of providing his own frequency (Figure 6-15-3). These selected frequencies are input to two switch-controlled circuits that enable the user to select different duty cycles for the A and B outputs.

The selector circuits produce the A CLOCK and B CLOCK signals. These are input to the output control circuits which, under control of the counters, produce the INPUT, EN, and INTR signals. These signals, along with the SIGN bit from the counter, go through the output inhibit gates to the output switches. These gates inhibit all outputs when the DBIT is asserted.

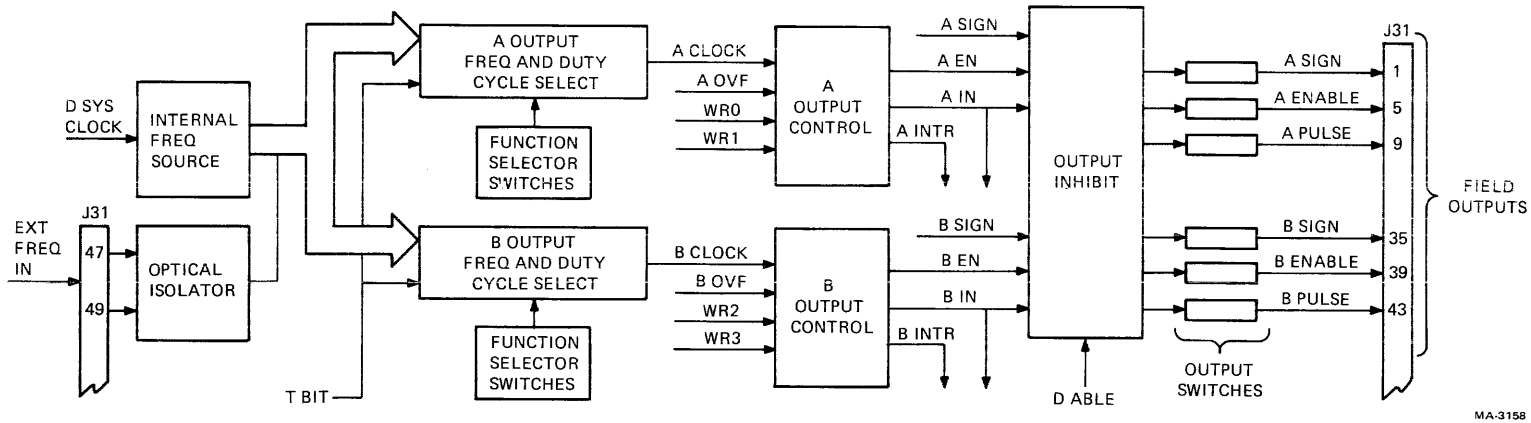


Figure 6-15-3 Daughter Board Block Diagram

Frequency and Duty Cycle Select

The circuit that determines the frequency and duty cycle of the PULSE output is shown in Figure 6-15-4. All frequencies (internal and external) are input to a multiplexer that selects one of the frequencies as a function of the E33-4 to E33-7 switch settings for the A counter or E14-4 to E14-7 for the B counter. (Switches E33-1 to E33-8 for the A counter, and E14-1 to E14-8 for the B counter are represented by switches 1 through 8 in Figure 6-15-4.) The selected frequency, which is ten times the final output frequency, is input to a divide-by-ten counter. This is a fully decoded decade counter. One of the counter's outputs is used to set the flip-flop shown and a subsequent one, selected by the duty cycle multiplexer, resets this flip-flop. The output of the flip-flop therefore has a duty cycle determined by the selected multiplexer output. One of eight possible duty cycles from 1Ø percent to 8Ø percent can be selected by use of switches E33-1, E33-2, and E33-3 for the A counter, and E14-1, E14-2, and E14-3 for the B counter.

Note that when an external frequency is selected with switches E33-4 to E33-7, or E14-4 to E14-7, the external frequency must be ten times the desired output frequency, and the output duty cycle is determined by switches E33-1, E33-2, and E33-3, or E14-1, E14-2 and E14-3. Also note that if switch E33-8 or E14-8 is on, the internal frequency and duty cycle select circuits are bypassed, and the PULSE output is the frequency and duty cycle of the external signal.

Assertion of the TBIT causes this circuit to select a 2 kHz, 5Ø percent duty cycle test frequency.

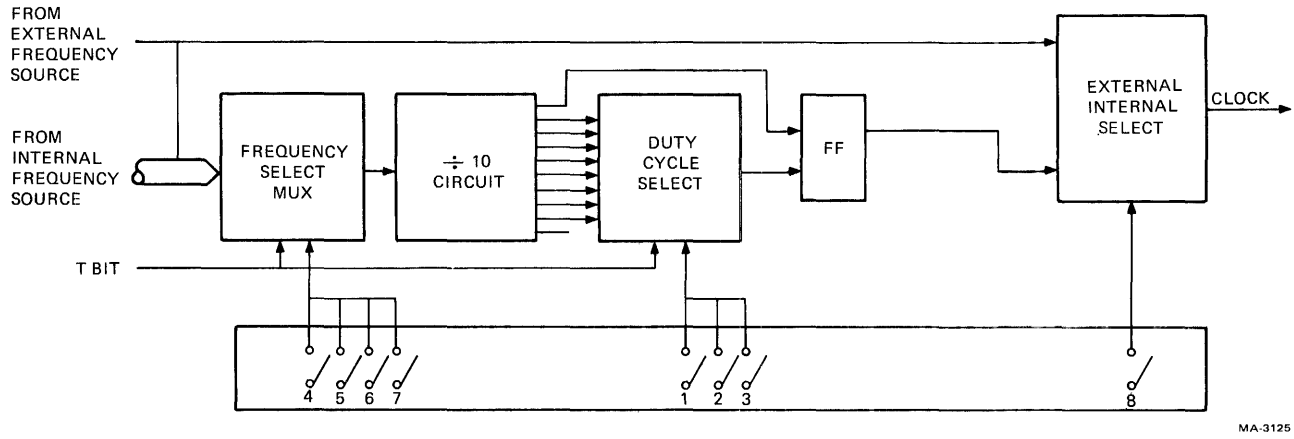


Figure 6-15-4 Frequency and Duty Cycle Select

Output Control Circuit

The output control circuit uses the counter's loading and overflow signals to start and stop the output pulse train. The control circuit and output timing for the A outputs are shown in Figures 6-15-5 and 6-15-6. Operation is as follows.

The 16-bit data word to the counter is written in two 8-bit bytes. The high byte is written first and stored in a buffer register on the module. When the low byte data is written, both it and the buffered high byte data are loaded into the 16-bit counter by WRØ. A SIGN OUT directly follows the sign bit of the high byte without waiting for the A CLOCk signal. If the 15-bit magnitude of the counter is now nonzero, A OVF L goes high, and the first leading edge of A CLOCK after this sets the EN flip-flop, turning on the A ENABLE output. The second leading edge of A CLOCK sets the PULSE flip-flop and A OUTPUT begins to produce pulses at the frequency and pulse width of A CLOCK. The counter is decremented as each pulse is produced. When the required number of pulses has been produced, the counter will have decremented to zero and A OVF L again goes low. On the next leading edge of A CLOCK, the EN flip-flop resets, turning off the A ENABLE output and causing an interrupt. As shown in Figure 6-15-6, the required number of pulses is produced within the true portion of A ENABLE.

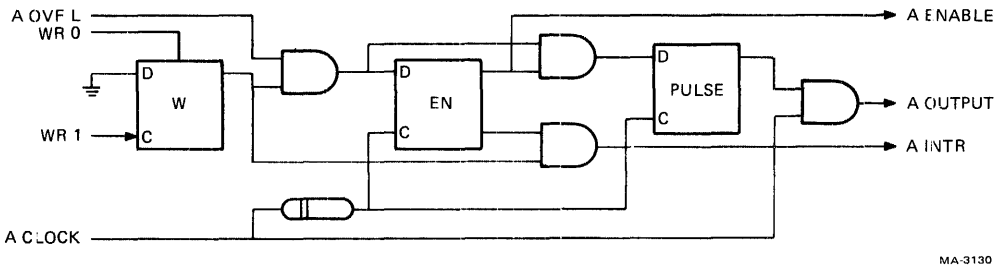


Figure 6-15-5 Output Control (for A Counter)

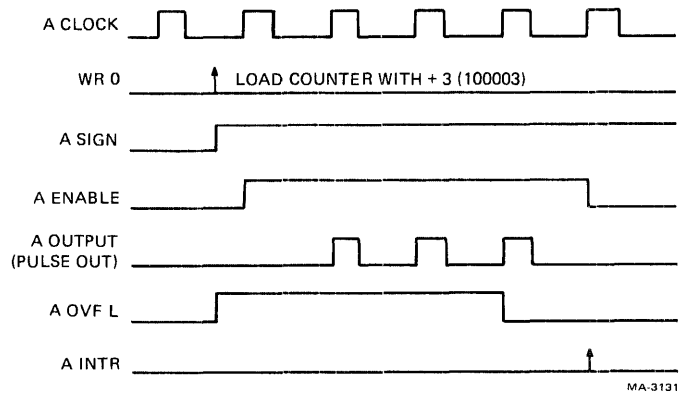


Figure 6-15-6 Output Control Timing

Should the user wish to abort the output pulse train, he can do so by writing the high byte of the counter. This resets the W flip-flop causing the pulse train to stop at the end of the current pulse period. In this case an interrupt is not generated and the counter still contains data corresponding to the number of additional pulses that would have been output had operation not been aborted.

Software Features

The contents of the counter may be read at any time. The high byte must always be read first. When this is done, the low byte data is stored in a common output buffer register. When the low byte is read, it is the data in the buffer that is read. Therefore, even though the counter may decrement during the time between the high and low byte readings, both bytes will contain data of a single point in time.

When a counter is loaded, the high byte must be loaded first. This data is not loaded directly into the counter but is stored in a common input buffer register until the low byte is loaded. At this time, both data bytes are loaded into the counter.

Address Selection

The four module addresses must be assigned according to the rules stated in Chapter 4. They are selected on the module by the 7-pole switch, E61 of the mother board (Figure 6-15-2). An example of one possible address selection is shown in Figure 6-15-7 to illustrate the use of this switch.

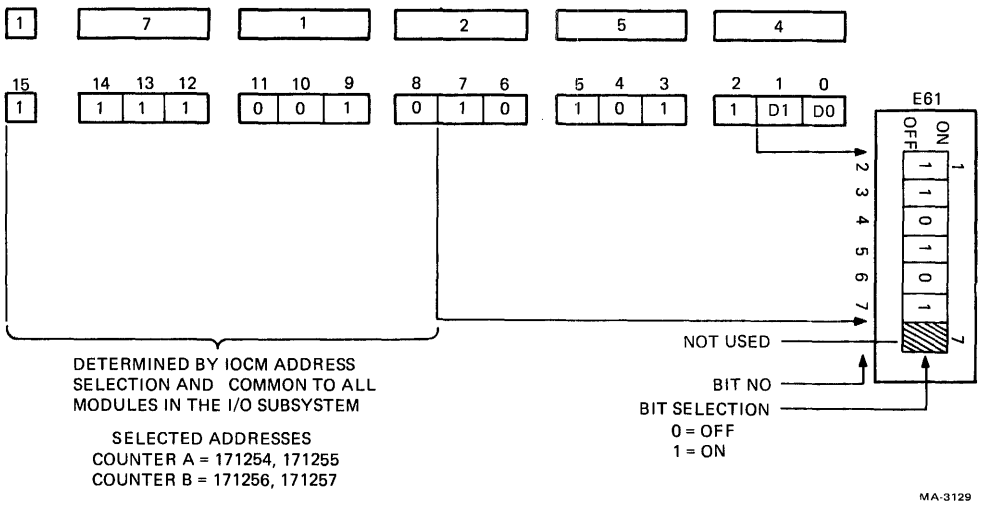


Figure 6-15-7 Address Selection Example

Address Format
The module's four data addresses as determined by the two least significant bits of the address word are as follows.

Y1	Y0	Bits	
0	0	00-07	counter A
0	1	10-17	
1	0	00-07	counter B
1	1	10-17	

Table 6-15-1 Module M6014 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	A SIGN OUT	2	Common
3		4	
5	A ENABLE OUT	6	Common
7		8	
9	A PULSE OUT	10	Common
11		12	
13		14	
15		16	
17	Common	18	Common
19		20	
21		22	
23		24	
25		26	
27		28	
29		30	
31		32	
33	Common	34	Common
35	B SIGN OUT	36	Common
37		38	
39	B ENABLE OUT	40	Common
41		42	
43	B PULSE OUT	44	Common
45		46	
47	ISO HIGH LEV IN +	48	ISO HIGH LEV IN -
49	ISO LOW LEV IN +	50	ISO LOW LEV IN -

Note:
Unlabeled pins are not used.

Generic Code
The generic code of the M6Ø14 is Ø44.

Pin Connections
The M6Ø14 module pin connections for J31, the I/O cable connector, are listed in Table 6-15-1.

APPLICATION INFORMATION

Proper I/O module installation procedures are presented in Chapter 3, Paragraph 3.3.3.3. The M6Ø14 has the following additional requirements.

Field Connections
The module's output drivers are able to drive the same type load as the M6Ø1Ø module outputs. They are TTL compatible; the outputs are not Darlingtons. The user's load must provide pull-up resistors to the supply voltage (+5 V for TTL applications).

The optional isolated input is common to both counters and may be high level, 25 volts to 55 volts, or low level, 12 volts to 28 volts. The maximum allowable frequency at this input is 1 kHz. Typical field interfaces for the A outputs and the isolated input are shown in Figure 6-15-8. The screw terminal configuration for all module field connections is shown in Table 6-15-2.

Function Selector Switches
Output frequency and duty cycle are selected by use of switch packs E33 and E14 of the daughter board for the A and B outputs respectively. The A and B outputs are independent from one another; frequency and duty cycle of one may be selected without regard to the other. The selection process can be facilitated by referring to Figure 6-15-9 which summarizes the possible selections.

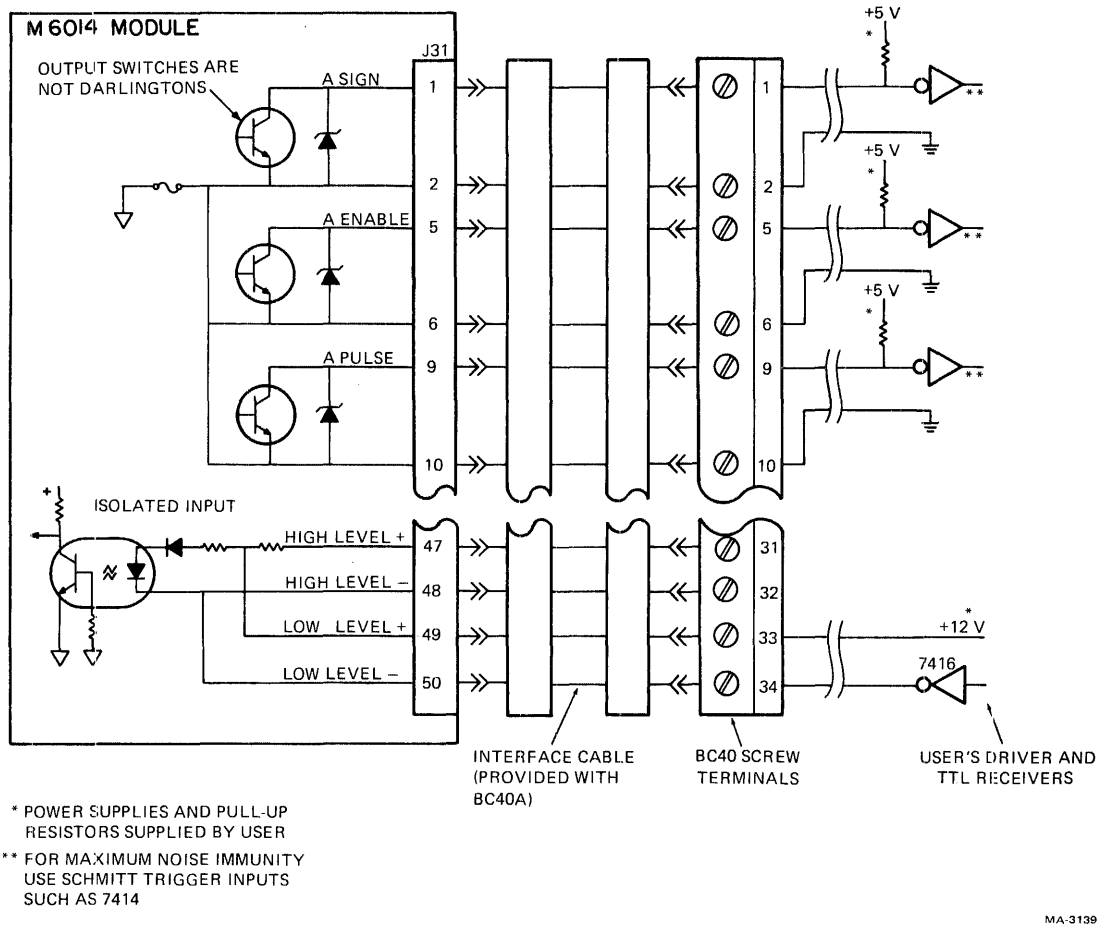


Figure 6-15-8 M6014 Typical TTL Interface

Table 6-15-2 Module M6Ø14 Field I/O Screw Terminal Connections

Field I/O		Screw Terminal Number
A SIGN	OUT	1
	Common	2
		3
		4
A ENABLE	OUT	5
	Common	6
		7
		8
A PULSE	OUT	9
	Common	1Ø
		11
		12
		13
		14
		15
		16
	Common	17
	Common	18
B SIGN OUT	OUT	19
	Common	2Ø
		21
		22
B ENABLE	OUT	23
	Common	24
		25
		26
B PULSE	OUT	27
	Common	28
		29
		3Ø
ISOLATED HIGH LEVEL IN	+	31
	-	32
ISOLATED LOW LEVEL IN	+	33
	-	34

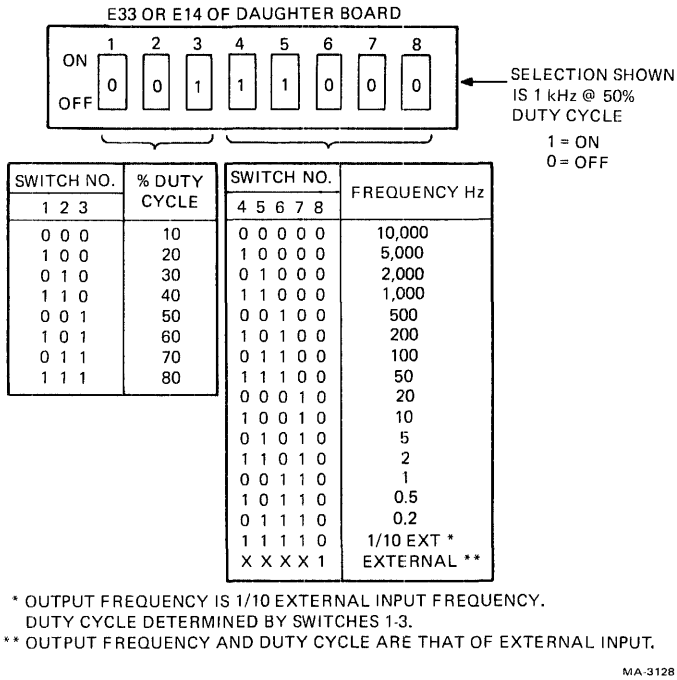


Figure 6-15-9 Frequency and Duty Cycle Selectors

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc
Operating current	135 mA

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 115 mA
Backup supply: 2Ø mA

Standby current (backup supply)	2Ø mA

Isolated Input Characteristics

Maximum ratings	Positive input voltage: +55 V maximum Negative input voltage: -55 V maximum Short-term overload: Withstands accidential connection to 117 Vac for two (2) hours

Thresholds	Range 12-28 V	25-55 V
	Logic Zero: 5.2 V typical 3.3 V minimum	 8.7 V typical 5.5 V minimum
	Logic One: 5.5 V typical 7.8 V maximum	 9.3 V typical 13.2 V maximum
	Hysteresis: Ø.3 V typical	 Ø.6 V typical
Input current At Input +12 V differential	5.Ø mA typical	
At Input +25 V differential	1Ø.6 mA typical 12.Ø mA maximum	
At Input +55 V differential		13.5 mA maximum
At Input -12 V differential	5Ø microamp maximum	5Ø microamp maximum
	Ø.Ø5 microamp typical	Ø.Ø5 microamp typical
Isolation voltage	1ØØØ V 2ØØ VA for UL approval	
Propagation delay	2ØØ microseconds typical 35Ø microseconds maximum	

Nonisolated Output Characteristics

Maximum ratings

High level output voltage:
+5 V ±5 percent for TTL loads
+55 V for non-TTL loads
Low level output voltage: +Ø.4 V
High level leakage current: 2Ø microamp
Sink current: 25Ø mA per output

Output timing

Maximum Times (microseconds)

Transition	V_{in} = 12 V, RL = 1ØK		V_{in} = 55 V, RL = 3.5 K	
	Propagation Time	Transition Time	Propagation Time	Transition
Zero to one	Ø.3	Ø.1	Ø.6	Ø.2
one to zero	3Ø	1Ø	2Ø	6

NOTE
Propagation time is referenced to the source of the activating signal.

Output circuit protection

The output circuits are protected from field overvoltage conditions by a 62 V zener diode across each output. Note that this diode does not protect a TTL load, which normally has a maximum input voltage rating of +5.5 V.

Common mode protection is provided by a 1 A Picofuse in series with the dc return.

Internal frequencies

10ØØØ, 5ØØØ, 2ØØØ, 1ØØØ, 5ØØ, 2ØØ, 1ØØ, 5Ø, 2Ø, 1Ø, 5, 2, 1, Ø.5, Ø.2 Hz ± Ø.1 percent

Switch-selectable for each counter

Internal duty cycles

1Ø, 2Ø, 3Ø, 4Ø, 5Ø, 6Ø, 7Ø, 8Ø percent
Switch-selectable for each counter

Physical Characteristics

Two quad modules assembled as a mother-daughter combination make up the M6Ø14 module.

Dimensions:

Quad module, triple width, 8-1/2 inch length

Field connector

Cable type BC4ØA or customer-supplied 5Ø pin Berg

Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degrees C ambient
Heat dissipation	6.5 Btu/hr maximum from internal supply 4.6 Btu/hr maximum from external supply

FUNCTIONAL DESCRIPTION

The M6Ø15 module provides sixteen program-controlled retentive dc outputs. These outputs are isolated, three wire, power FET switches. They can be used for controlling solenoid valves, relays, indicators, heaters, etc., where retention of existing output status must be maintained during a computer power failure. Provision is made for reading the module's output registers and generic code.

DETAILED DESCRIPTION

The simplified block diagram in Figure 6-16-1 shows that processor output data entering through the D-bus interface connector is addressed and controlled by signals from the D-bus and is output to the field through J1. The sequence of control and data flow is as follows.

Data Paths

The eight data lines D(Ø-7) entering at the D-bus interface connector go to both data output registers and to an address comparator in the I/O control section. One of the output registers accepts new data upon assertion of either AØH or AØL. The other register remains unchanged. Data from the output registers is applied to the output circuits. The eight low-byte output circuits (groups 1 and 2) accept new data upon assertion of LB STROBE. The eight high-byte circuits (groups 3 and 4) get new data if HB STROBE is asserted. The output circuits are connected to J1 for output to the field. If the D BIT is asserted, LB STROBE and HB STROBE are disabled. This allows testing of the output registers without affecting the output circuit switches. The T BIT is not implemented on this module.

Data Control Signals

Control signals for the above mentioned data paths are initiated by the program, resulting in the following sequence of operation. When the program calls for an operation requiring a DATAO to the module, the IOCM starts a D-bus Cycle and causes the module's address to be put on the D-bus. The module's address comparator decodes the address, and after a short delay for deskewing, D SYNC is asserted. This causes the module's address control section to produce the MY ADDRESS signal which enables the data output register. After a short delay, D DOUT is asserted to load the data into the output register. The register outputs drive the output circuits. After a delay, to allow for the propagation time of the optical isolators, these circuits are strobed, and the output switches assume their new states. D DOUT is also ANDed with MY ADDRESS to produce D RPLY, which informs the processor that the data has been accepted for output. The processor then negates D DOUT.

Output data remains unchanged unless the processor outputs a new data byte to that address. If the program wants to monitor that

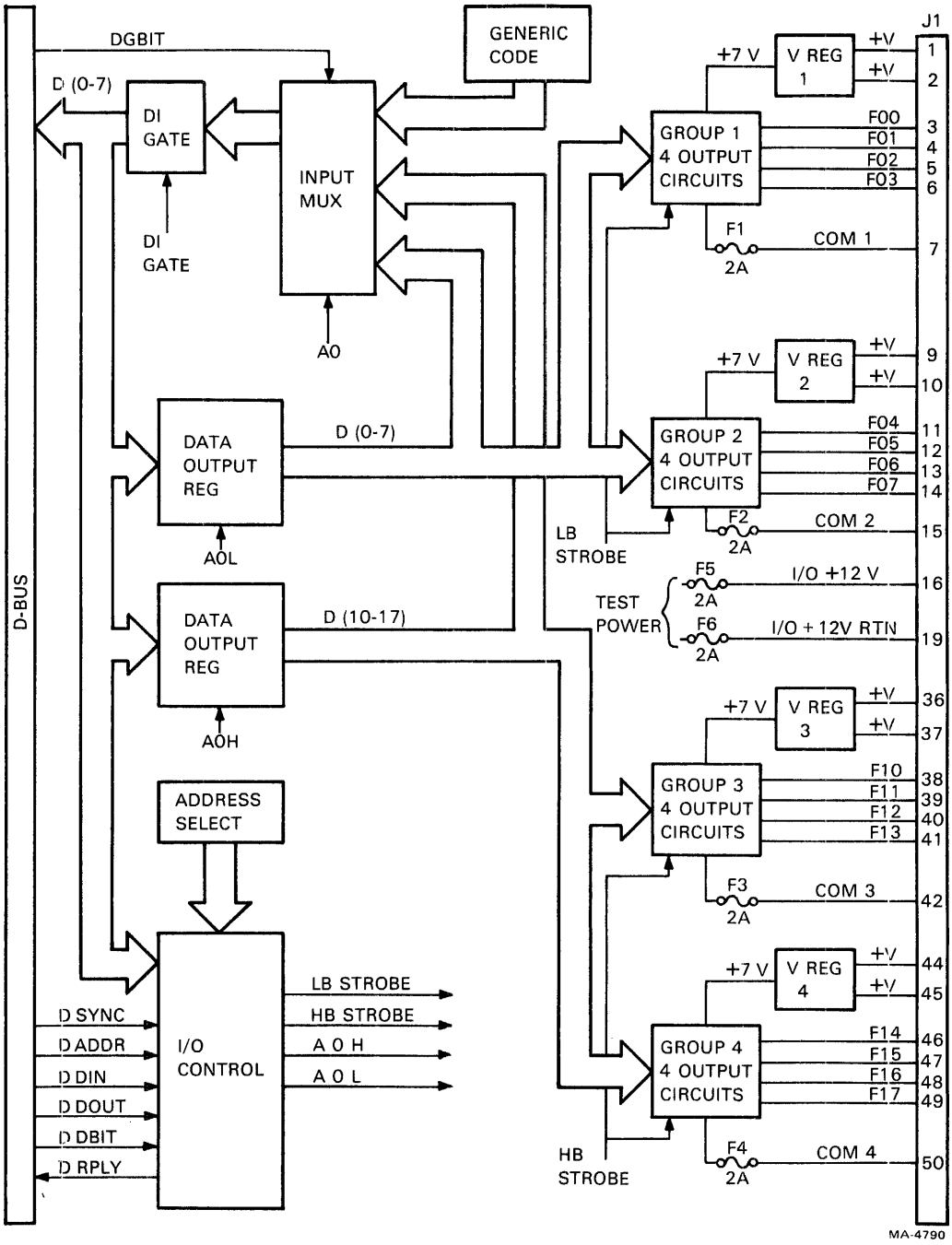


Figure 6-16-1 M6015 Retentive DC Output Block Diagram

data, it causes the processor to perform a DATAI on that address. When this is done, the processor first asserts the address as before and causes the IOCM to start a D-bus Cycle. This causes the address to be put on the D-bus and to be decoded by the module's address comparator. Then D SYNC is asserted after a short delay for deskewing, resulting in the MY ADDRESS signal. However, in this case, the next signal asserted by the IOCM is D DIN, which is ANDed with MY ADDRESS to produce DI GATE. This signal strobes the contents of the input multiplexer onto the D-bus. If the program has set the GBIT in the CSR of the IOCM, the input multiplexer contains the module's identity code instead of the output data. DI GATE also produces D RPLY after a short delay to notify the processor that data is on the D-bus. When data is received by the processor, D DIN is negated, causing DI GATE to negate and remove data from the D-bus.

Output Circuits

The output circuits are electrically isolated from the I/O subsystem by optical isolators. They are isolated from each other in groups of four. Groups receive their power from up to four user-furnished power supplies in the field. Each group has a voltage regulator and overload protection fuse.

Each group of four output circuits contains an output reset circuit (Figure 6-16-2). This circuit resets the group's output latches, and turns off its output switches, whenever field power is turned on or off, or falls below an acceptable value. This ensures that the output latches and switches will always be in the off state during a power-up or power-down transition. Consequently, when field power is first turned on, or when it fails and comes back up, the outputs will be all zeros until new data is written.

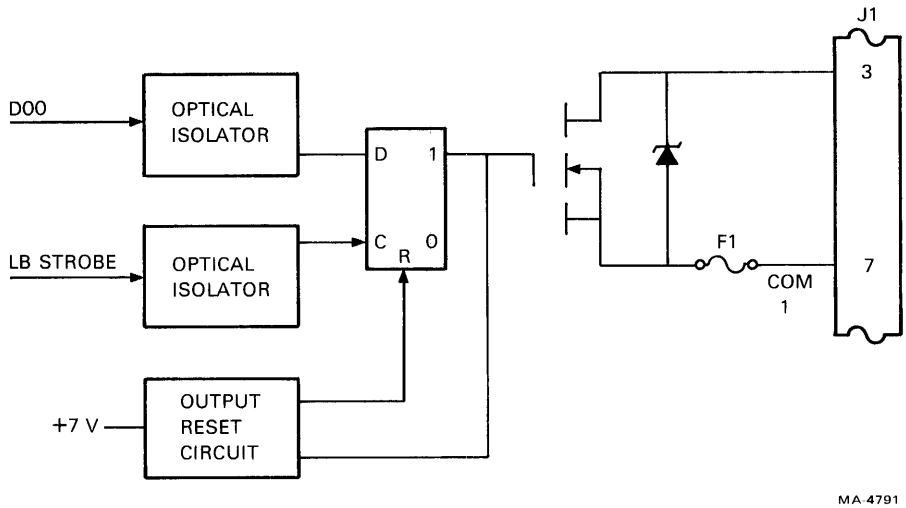


Figure 6-16-2 Single Output Circuit (Simplified)

Each of the sixteen output circuits drives a power FET switch that can be used to turn a variety of dc circuits ON or OFF. Each of these circuits is protected from field overvoltages by a zener diode across its output.

The state of the data output registers can be read by means of the input multiplexer. The addressed data byte is selected by the AØ signal. If the GBIT is asserted, this multiplexer will output the module's identity code. The selected data is then strobed onto the D-bus by the DI GATE signal.

The fused +12 V output provides power for a field service test device. It is not available to the user.

Address Selection
The two addresses for the module must be assigned according to the rules stated in Chapter 4 and are selected on the module by the 8-pole switch, E-6 (Figure 6-16-3). An example of one possible address selection is shown in Figure 6-16-4 to illustrate the use of this switch.

Generic Code
The generic code of the M6Ø15 module is octal Ø22.

Pin Connections
The M6Ø15 module pin connections are shown in Table 6-16-1 for J1, the I/O cable connector.

I/O Connections
Field connections for the M6Ø15 module may be implemented with the BC4ØA screw terminal assembly. Switch outputs and field power supply inputs using the BC4ØA are identified in Table 6-16-2.

Note that the four groups of four outputs are isolated from each other. Separate power supplies must be used if this isolation is to be maintained.

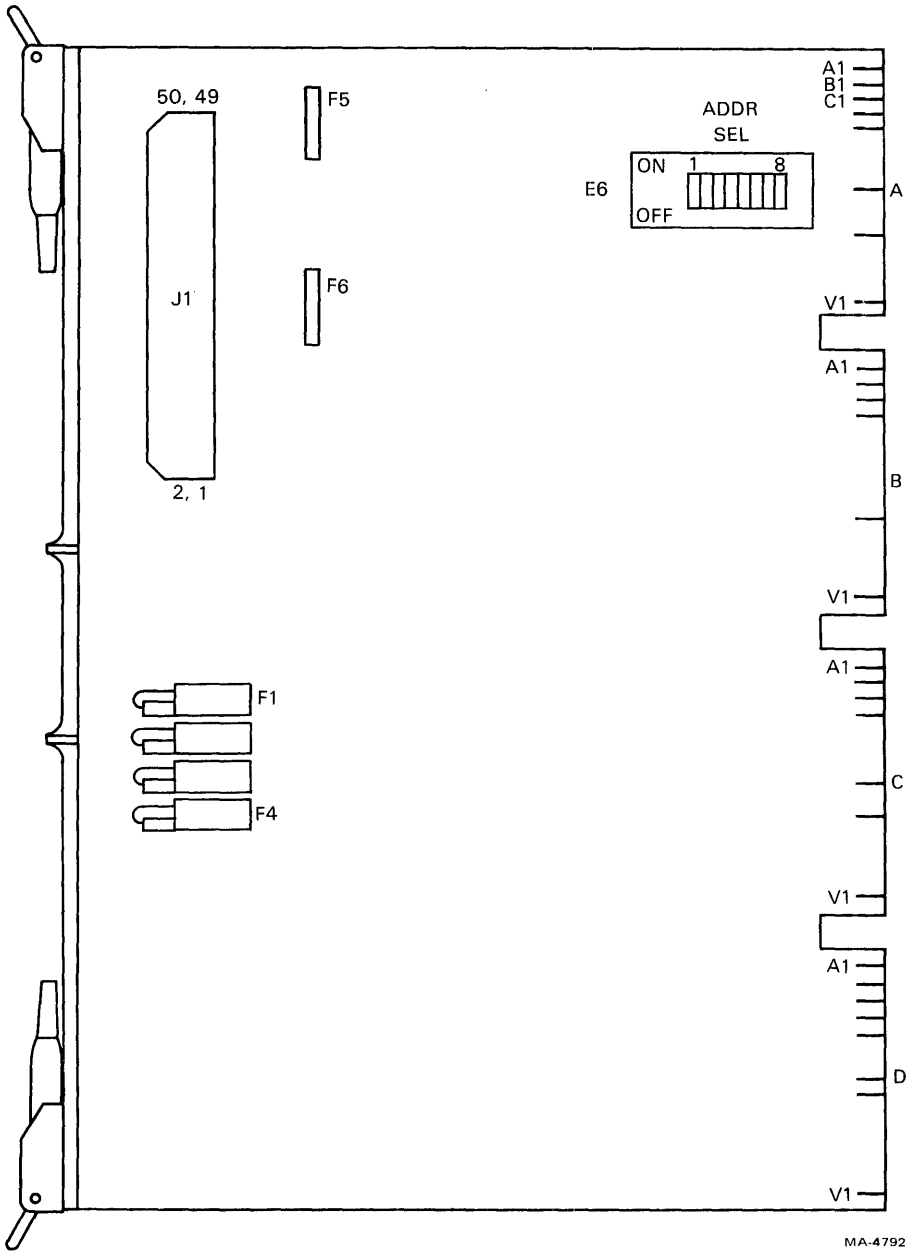


Figure 6-16-3 M6Ø15 16-Bit Retentive DC Output

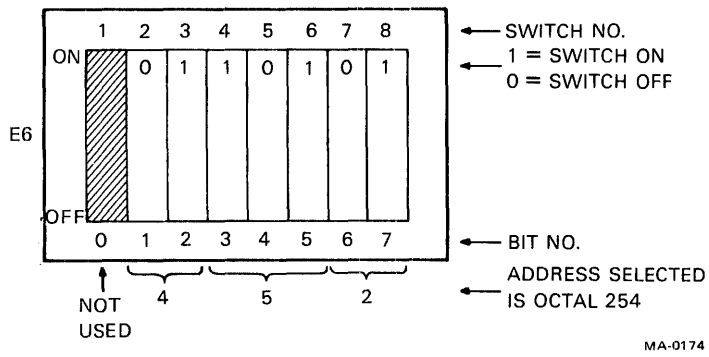


Figure 6-16-4 Address Selection Switch

Table 6-16-1 M6015 I/O Pin Connections

Module I/O Connector Pin	Field I/O		Module I/O Connector Pin	Field I/O	
1	+(12-30) V		2	+(30-55) V	
3	00	Group	4	01	Group
5	02	1	6	03	1
7	-Common		8	Not Used	
9	+(12-30)V		10	+(30-55) V	
11	04	Group	12	05	Group
13	06	2	14	07	2
15	-Common		16	+12 V OUT	
17	Not Used		18		
19	+12 V Return		20		
21			22		
23			24		
25			26		
27	Not Used		28	Not Used	
29			30		
31			32		
33			34		
35			36	+(12-30) V	
37	+(30-55) V		38	10	Group
39	11	Group	40	12	3
41	13	3	42	-Common	
43	Not Used		44	+(12-30) V	
45	+(30-55) V		46	14	Group
47	15	Group	48	16	4
49	17	4	50	-Common	

Table 6-16-2 M6015 Field I/O Screw Terminal Connections

Field I/O		Screw Terminal Number
Group 1	+(12-30) V	1
	+(30-55) V	2
	00	3
	01	4
	02	5
	03	6
	-Common	7
	Not Used	8
Group 2	+(12-30) V	9
	+(30-55) V	10
	04	11
	05	12
	06	13
	07	14
	-Common	15
	+12 V Out	16
	+12 V Return	17
	+12 V Return	18
		19
Group 3	+(12-30) V	20
	+(30-55) V	21
	10	22
	11	23
	12	24
	13	25
	-Common	26
	Not Used	27
Group 4	+(12-30) V	28
	+(30-55) V	29
	14	30
	15	31
	16	32
	17	33
	-Common	34

APPLICATION INFORMATION

Having a retentive output capability enables the user to prevent disruption of crucial parts of his application in the event of a computer power failure. The M6Ø15 provides this capability.

NOTE

In order to use the M6Ø15 as a retentive output module, the user must first implement whatever circuit changes may be necessary to update the system IOCM to the revision level listed below.

IOCM	Circuit Schematic Rev. Level
M7958	H
M7959	A*
M8719	C

***All versions of the M7959 are usable without modification.**

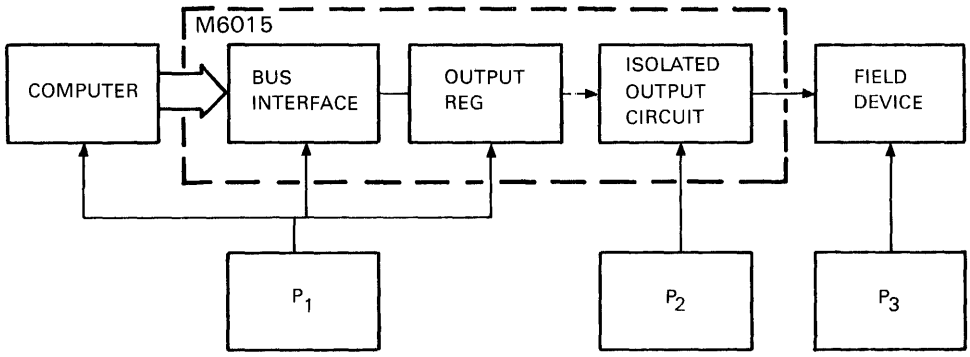
Normal Operation

To summarize briefly, the M6Ø15 provides 16 retentive outputs. The states of the output switches will remain intact during a computer power failure, assertion of the DBIT, or initialization. The module's output registers can be read by the computer, and these registers contain the data that was last written to them unless there has been a computer power failure. The significance of that data depends on what failure modes have occurred.

Power Failure Mode

When planning his system power distribution, the user must take into consideration its various failure modes and their possible effects on his application. In particular, he must consider how different failure modes affect the retentive feature of the M6Ø15. Refer to Figure 6-16-5 and the accompanying table.

The figure shows independent power sources for each part of the system (i.e., P1, P2, and P3). This independence, of course, relies on the design of the site's power distribution system. If the design is such that one or more parts of the system are not independent (such as, P1 and P2), they can fail simultaneously. The table summarizes the possible failure combinations and their consequences.



FAILURE MODES

FAIL = 0	CONTAINS DATA LAST WRITTEN		OUT REG = OUT SW
P_1 P_2 P_3	OUT REG	OUT SW	
1 1 1	T	T	T
1 1 0	T	T	T
1 0 1	T	F	F
1 0 0	T	F	F
0 1 1	F	T	F
0 1 0	F	T	F
0 0 1	F	F	F
0 0 0	F	F	F

T = TRUE
F = FALSE

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Figure 6-16-5 Power Failure Modes

Examination of the table shows the following.

1. A computer power failure will not affect the status of the output switches.

2. Any failure of the computer or output circuit power (i.e., P1 or P2) invalidates the contents of the output registers as an indicator of the output switch state. This is true because those failure modes result in either the output registers being cleared or the output latches being reset.

3. As long as the module's output power (P2) does not fail, its output switches will retain the data last written to them.

A consequence of 3, above, is that if the module's output circuits are independently powered, their states could be retained even when everything else (P1 and P3) has failed. The user must consider whether or not this is desirable for his system under all conditions.

Field Power Wiring
To ensure reliable operation of the M6Ø15's retentive outputs, the user must pay close attention to the module's output circuit field power supply wiring. In particular, he must make certain that the output impedance of the power supply is not inductive. Not taking this precaution can result in voltage transients on these wires. If these transients are large enough, they can cause the retentive outputs to be reset.

To guard against this, the M6Ø15 has a nominal amount of bypass capacitance on these inputs. Still, the module can be susceptible to this type of noise if the user's power supply lines are excessively inductive. If this be the case, he can compensate by adding additional bypass capacitance near the module.

Reading Output Switch States
If necessary, the user can monitor the states of the output switches by connecting them to an isolated input module (i.e., an M5Ø12). He will then be able to determine the status of the output switches even if there has been a power failure.

Isolated Output Application
The M6Ø15 can also be used advantageously in applications not requiring its retentive output feature. For example, if isolated outputs are needed, and the current required is less than 1/4 ampere, the M6Ø15 can be used to provide twice as many outputs per module as would an M6Ø12.

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc +2 V -1 V Backup supply: 14 Vdc $\geq$ VB $\geq$ (VS-Ø.7) Vdc
Operating current	13Ø mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 125 mA maximum
Backup supply: 5 mA maximum

Standby current (backup supply)	5 mA maximum

Output Characteristics

Maximum ratings

Positive output voltage	+55 V maximum
Negative output voltage	-Ø.6 V maximum
Saturation voltage	2 V maximum at Ø.25 A

Off leakage current	100 microamp maximum
Sink current	0.25 A/bit
Isolation voltage	1000 V maximum between any output and ground or between groups Group 1 = Outputs 0-3 Group 2 = Outputs 4-7 Group 3 = Outputs 10-13 Group 4 = Outputs 14-17
Common mode source	200 VA for UL approval
Field supply current (Vin = 12-55 V)	15 mA maximum per group of four outputs
Field supply voltage	12-35 V or 30-55 V

Output timing

Maximum Times (Microseconds)

	V_{in} = 55 V, RL = 220 ohms		V_{in} = 12 V RL = 10K	
Transition	**Propagation Time**	**Transition Time**	**Propagation Time**	**Transition Time**
Turn-on	210	40	210	20
Turn-off	210	40	210	40

NOTE
Propagation time is referenced to the source of the activating signal.

Output circuit protection	The output circuits are protected from field overvoltage conditions by a 62 V zener diode across each output Overload protection is provided by a 2 A Picofuse in series with the dc return (one per group of four outputs - four per module)
Dimensions	Quad module, double width, 8-1/2 inch length
Field connector	Cable type BC40A or customer-supplied 50 pin Berg

Environmental Characteristics	Complies with DEC STD 102 Class C Operates in convection cooled environment up to 60 degrees C ambient
Heat dissipation	6.2 Btu/hr maximum due to module circuitry, 273 Btu/hr maximum due to field power source

INTRODUCTION

The information in this section is specifically directed at analog input subsystems using the AØ14 converter and its expansion modules. It is not applicable to the AØ2Ø or any other converter.

High speed analog input requirements of the I/O Subsystem are implemented with the AØ14 A/D converter. The A156 and A157 multiplexers supplement the A/D converter by providing additional input capability. The A156 provides the same high level inputs as those built into the A/D converter. The A157 has programmable gain and is intended for use with low level signals.

Before referring to the material on a particular module type, the reader should understand the following discussion.

1. Input requirements of many applications cannot be met by the A/D converter module alone because its internal multiplexer is limited to 16 single-ended or eight differential inputs, and is not intended for use with low level inputs.

2. Expansion of the subsystem to accommodate more of the same type inputs as accepted by the A/D converter module is accomplished by adding A156 multiplexer modules. Up to seven may be used per AØ14, each adding 32 single-ended or 16 differential inputs. This gives an expansion capability of up to 24Ø single-ended or 12Ø differential inputs. A mix of single-ended and differential mode modules is also permissible, but all inputs on a given module will be the same. A switch on the module permits the user to select the desired mode.

3. If the subsystem is required to service low level inputs, the A157 multiplexer may be used. This module has 16 differential mode inputs with programmable gain to accept inputs of varying levels with the same module.

4. The subsystem can consist of the AØ14 A/D converter module by itself or supplemented by up to seven A156 or A157 multiplexer modules in any combination. A fully expanded analog input subsystem is shown in Figure 6-17-1.

5. An input subsystem consisting of the A/D converter and its expansion multiplexer modules is, as far as the programmer is concerned, just one module with a number of selectable inputs. Although the expansion multiplexer modules interface with the D-bus, they are addressed and controlled by the A/D module, which occupies four contiguous addresses on the D-bus.

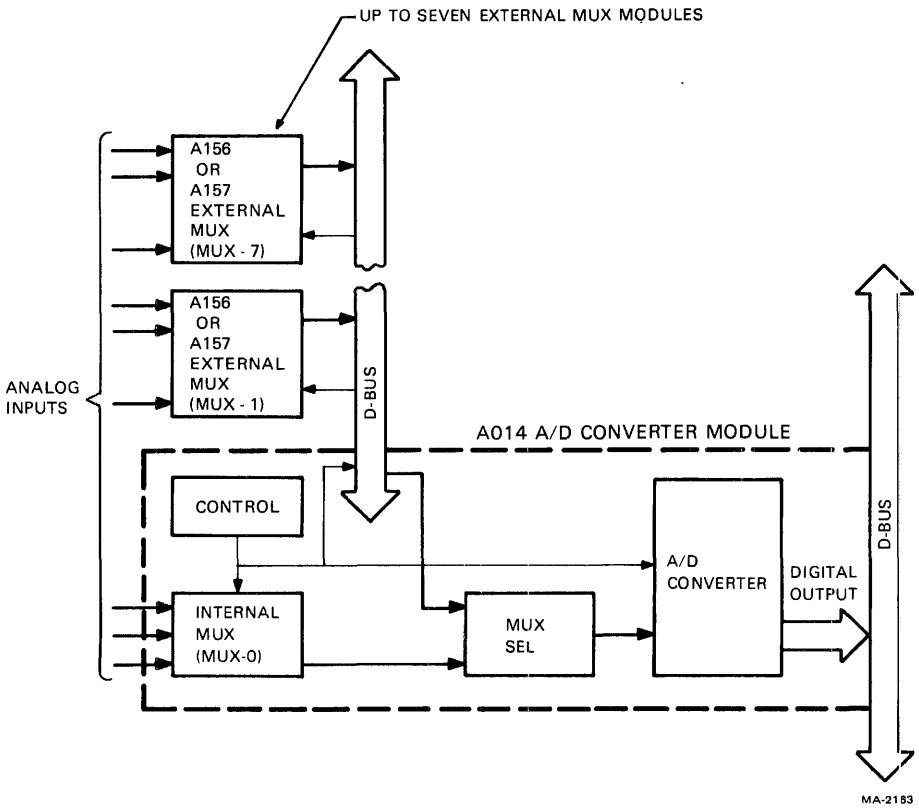


Figure 6-17-1 Analog Input Subsystem

SOFTWARE INTERFACE

General

All subsystem registers are contained in the four-byte address space occupied by the A/D module on the D-bus. These addresses may be anywhere in the I/O Subsystem address space (subject to the addressing rules in Chapter 4), but will be referred to here simply as A(Ø-3). Table 6-17-1 summarizes the register byte address assignments.

Table 6-17-1 Register Byte Address Assignments

Analog Subsystem Byte Address Assignment	I/O Data		
	Read	Read Generic	Write
	7 6 5 4 3 2 1 Ø	7 6 5 4 3 2 1 Ø	7 6 5 4 3 2 1 Ø
AØ	Converted data D(Ø-7)	A/D converter generic code	Processor trap
A1	Ø Ø Ø Ø C. Data D(8-11)	A/D converter generic code	Processor trap
A2	MUX No. Chan No.	Selected MUX generic code*	MUX No. Chan No.
A3	MUX Gain Status TO E D B	Selected MUX generic code*	MUX Gain GO

BUSY
DONE
ERROR
TIME OUT

*MUX number zero is the A/D's internal multiplexer and has the same generic code as the A/D.

A/D Converter Data Register
This is a 12-bit read-only register on the A/D module that contains the results of the most recent A/D conversion. The register is contained in the first two bytes of the module's address space (AØ and A1) as shown below.

A/D Byte Address	Data Register							
AØ	7	6	5	4	3	2	1	Ø
A1					11	1Ø	9	8

The eight LSBs, D(Ø-7), are in byte AØ and the four MSBs, D(8-11), are in the first four bit positions of byte A1.

Channel Number Register
This is a 5-bit read/write register that selects a channel on one of the input subsystem multiplexers. On a 32-channel module all five bits are needed to select the channel. But 32-channel operation is not always the case. For example, if the internal multiplexer is being used in differential mode, only eight channels can be addressed. In this case, only three of the five bits (Ø-2) are used to select a channel. The other two bits (4, 5) must be zero; if they are not, the event is detected as an error condition and the error bit in the status register is set.

The channel number register is in the A/D module's A2 address and stores the channel numbers as listed in Table 6-17-2.

Table 6-17-2 A/D Channel Number Register

A/D Byte Address	Channel Number Register (7 - - - - 4 | 3 | 2 | 1 | 0 Ø)					
A2	4	3	2	1	0	Chan. No.
	Ø	Ø	Ø	Ø	Ø	Ø
	Ø	Ø	Ø	Ø	1	1
	Ø	Ø	Ø	1	Ø	2
	Ø	Ø	Ø	1	1	3
	|	|	|	|	|	|
	|	|	|	|	|	|
	1	1	1	1	1	37

└Sets error bit in A/D status register if corresponding channel number does not exist on the selected multiplexer.

Multiplexer Number Register
This is a 3-bit read/write register that selects one of the eight possible multiplexers of an input subsystem. The A/D (internal multiplexer) is always multiplexer number zero. Expansion modules are encoded with multiplexer numbers one through seven by manipulating selector switches on the multiplexer modules. The multiplexer number register is in the A/D module's A2 address and stores the multiplexer number as listed in Table 6-17-3.

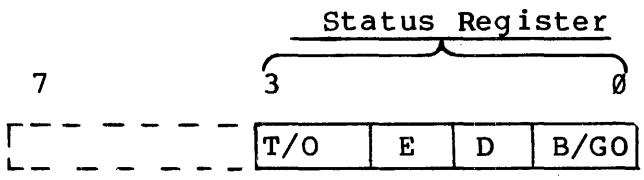
Table 6-17-3 Multiplexer Number Registers

A/D Byte Address	Multiplexer Number Register (7 | 6 | 5 | - - - - Ø)			
A2	7	6	5	Multiplexer Number
	Ø	Ø	Ø	Ø (A/D internal multiplexer)
	Ø	Ø	1	1
	Ø	1	Ø	2
	Ø	1	1	3
	1	Ø	Ø	4
	1	Ø	1	5
	1	1	Ø	6
	1	1	1	7

Status Register
This is a 4-bit register that contains A/D conversion status information and is located in the A/D module's A3 address byte. Status bit functions are described in Table 6-17-4.

Table 6-17-4 A/D Status Register

A/D Byte Address



Bit	Description
ØØ (Busy/GO) read/write	Reading this bit = 1 means an A/D conversion cycle is in progress. Setting this bit = 1 initiates the A/D conversion cycle.
Ø1 (DONE) read only	Done bit = 1 means that an A/D conversion cycle has been completed and data is available.
Ø2 (ERROR) read only	Error bit = 1 indicates one of the following errors has occurred. 1. A nonexistent channel has been selected 2. An illegal multiplexer gain has been selected 3. A time out error exists
Ø3 (TIME OUT) read only	Time out bit = 1 indicates that the addressed multiplexer has failed to respond to an A/D conversion cycle within the allotted time (approximately 1Ø ms after the GO bit was set).

Gain Register
This is a 4-bit register that contains the gain code of the selected multiplexer. It is a read-write register and can be accessed in the A/D converter's A3 byte.

The internal and A156 multiplexers always have unity gain (code zero), but the A157 multiplexer can be programmed for other gains by writing this register with the proper code. Writing an illegal gain code (a code other than zero for the A156 multiplexer, for example), will set the error bit in the status register. Gain codes are listed in Table 6-17-5.

Table 6-17-5 Gain Codes

A/D Byte Address	Gain Register 7 6 5 4	Gain	
A3			
	Ø Ø Ø Ø	1	(A156, AØ14, A157)
	Ø Ø Ø 1	2	
	Ø 1 Ø Ø	1Ø	
	Ø 1 Ø 1	2Ø	
	1 Ø Ø Ø	5Ø	A157
	1 Ø Ø 1	1ØØ	
	1 1 Ø Ø	2ØØ	
	1 1 Ø 1	1ØØØ	

The other codes have not yet been implemented.

Generic Code Registers

The generic codes are derived from 8-bit read-only registers. The A/D converter and A156 multiplexer modules each have two generic codes; one for the single-ended mode of operation, and one for the differential mode. Only one code is enabled at a time and is a function of the position of its mode switch.

If the GBIT is asserted when reading the AØ or A1 byte address of the analog subsystem, the A/D converter module responds with its own generic code. If the GBIT is asserted when reading the A2 or A3 byte addresses, the subsystem responds with the generic code of the selected multiplexer. If the selected multiplexer is number zero (internal multiplexer), the appropriate response is again the generic code at the A/D and all four addresses contain the same generic code. The subsystem generic codes are as follows.

Module	Generic Code	
	Differential Mode	Single-Ended Mode
AØ14	3Ø1	321
A156	322	342
A157	3Ø3	-

Sample Program

Analog conversions are accomplished by programs similar to the following. The program includes instructions for setting up the stack, selecting a multiplexer number, channel number, and gain code, and writing the GO bit, which starts a conversion. The program then waits for an interrupt. When the interrupt occurs, and is identified as an A/D interrupt, the A/D handler services the analog subsystem, reads the data, returns from the interrupt,

and repeats the cycle. The program's major functions are illustrated by the flow diagram of Figure 6-17-2.

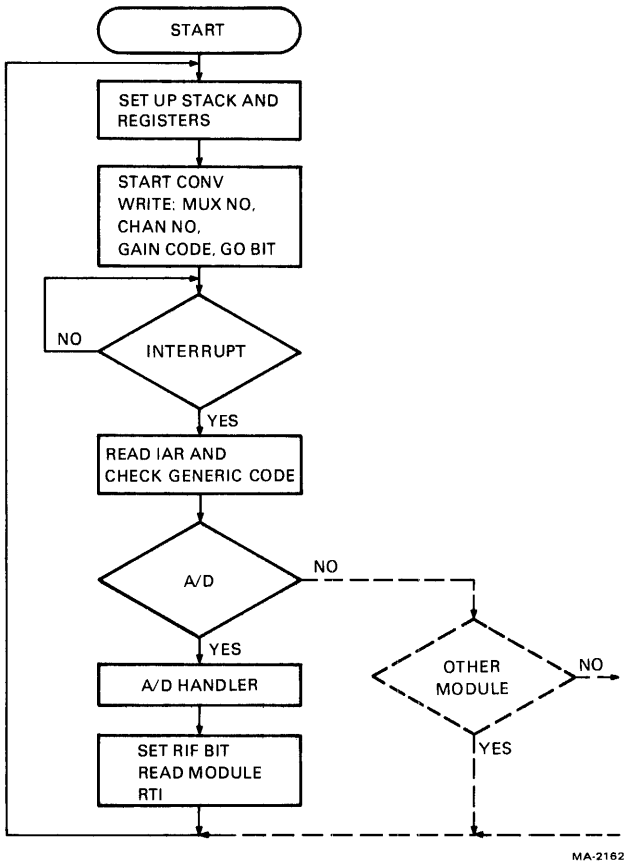


Figure 6-17-2 Sample Program Flow Diagram

SAMPLE A/D CONVERSION PROGRAM RT-11 MACRO VMØ2-12 PAGE 1

```
 1          .TITLE SAMPLE A/D CONVERSION PROGRAM
 2          000000          .ASECT
 3                          .ENABL AMA
 4
 5          000000          R0 = %0
 6          000001          R1 = %1
 7          000002          R2 = %2
 8          000003          R3 = %3
 9          000004          R4 = %4
10          000005          R5 = %5
11          000006          SP = %6
12          000007          PC = %7
13          000234          VECTOR = 234
14          171377          CSR = 171377
15          171376          IAR = 171376
16          171000          ADADR = 171000
17
```

```
18          001000. = 1000
19 01000    012706 START:   MOV     #700,SP         ;SET UP STACK
            000700
20 01004    012737          MOV     #INTR, VECTOR
                                                    ;SET UP VECTOR
            001070
            000234
21 01012    012737          MOV     #340, VECTOR+2
            000340
            000236
22 01020    112737          MOVB    #100, CSR       ;ENABLE SUBSYSTEM
                                                    ;INTR.
            000100
            171377
23 01026    106427          MTPS    #0              ;ENABLE CPU INTR.
            000000
24
25                                                  ;OTHER CODE
26
27 01032    113700 STCONV:  MOVB    MUXNO,R0        ;GET MUX NUMBER
            001216
28 01036    153700          BISB    CHANNO,R0       ;ADD IN CHANNEL
                                                    ;NUMBER
            001220
29 01042    110037          MOVB    R0,ADADR+2      ;MOV TO A2

            171002
30 01046    113700          MOVB    GAIN,R0         ;GET GAIN
            001222
31 01052    105200          INCB    R0              ;SET GO BIT
32 01054    110037          MOVB    R0,ADADR+3
                                                    ;MOV TO A3
            171003
33
34
35 01060    000001          WAIT                    ;INTERRUPT OR OTHER
                                                    ;CODE
36 01062    000240          NOP
37 01064    000137          JMP     START
            001000
38
39 01070    113700 INTR:    MOVB    IAR,R0          ;GET IAR
            171376
40 01074    042700          BIC     #177400,R0      ;CLEAR HIGH BYTE
            177400
41 01100    062700          ADD     #171000,R0      ;ADD OFFSET
            171000
42 01104    152737          BISB    #4,CSR          ;SET G BIT
            000004
            171377
43 01112    111001          MOVB    @R0,R1          ;GET GENERIC CODE
44 01114    142701          BICB    #30,R1          ;MASK S/E BIT
            000030
45 01120    122701          CMPB    #301,R1         ;A/D CODE?
            000301
```

```
46 01124  001002          BNE     1$              ;NO
47 01126  000137          JMP     ADHDLR          ;YES
          001132
48 01132                  1$                      ;OTHER I/O HANDLERS
49
50 01132  142737 ADHDLR:BICB     #4,CSR          ;CLEAR G BIT
          000004
          171377
51 01140  113701          MOVB    ADADR+3,R1      ;GET A3
          171003
52 01144  132701          BITB    #4,R1           ;ERROR?
          000004
53 01150  001025          BNE     ERROR           ;YES
54 01152  132701          BITB #2,R1              ;DONE?
          000002
55 01156  001000          BNE     DONE            ;YES
56
57
58                                                ;OTHER CODE
59
60 01160  105237 DONE:    INCB    CSR             ;SET RIF BIT
          171377
61 01164  113737          MOVB    ADADR+1,BUFF    ;GET HIGH BYTE,RIF

          171001
          001214
62 01172  042737          BIC     #177760,BUFF    ;MASK IRRELEVANT BITS
          177760
          001214
63 01200  000337          SWAB    BUFF            ;SWAP BYTES
          001214
64 01204  153737          BISB    ADADR,BUFF      ;GET LOW BYTE

          171000
          001214
65
66                                                ;PROCESS DATA
67
68 01212  000002          RTI                     ;RETURN FROM INTERRUPT
69
70
71
72
73 01214  000000 BUFF:    0
74 01216  000000 MUXNO:   0
75 01220  000000 CHANNO:  0
76 01222  000000 GAIN:    0
77
78 01224  000000 ERROR:   HALT
79        001000.END      1000
```

Software Restrictions

1. If a nonexistent multiplexer is addressed, internal control circuitry prevents further subsystem response and the processor traps. The condition is cleared by reading the AØ14 with the RIF bit set in the IOCM, or by initializing the D-bus.

2. At the completion of a conversion, the AØ14 must be read with the RIF bit set in the IOCM before any new data is written into the subsystem.

3. The channel number, multiplexer number, and gain must be reselected before each conversion.

Analog Field Wiring Practices

The DIGITAL Site Preparation Guide contains detailed information on field wiring practices. Particular attention should be paid to Section 1, Chapter 3 (System Grounding); Section 2, Chapter 1 (Process Connections Guide); and to the following useful guidelines.

Avoiding Spurious Signals

Confirm that the computer power supply ground is connected to power line (earth) ground.

Twisted Pair Input Lines

The effects of magnetic coupling on the input signals can be reduced for differential inputs by twisting the signal and return lines in the input cable.

Shielded Input Lines

The effects of electrostatic coupling on the input signals can be reduced by shielding the signal wires. This is especially important if the instrument or transducer has high source impedance. To prevent the shield from carrying current and thus developing ground loop voltages within the subsystem, connect it to ground at the instrument end only.

Allowing for Input Settling with High Source Impedance

All solid-state multiplexers inject a small amount of charge into their input lines when changing channels, causing a transient error voltage that is discharged by the input signal's source impedance. The analog subsystem shares this characteristic and also injects a small charge into the selected input line at the end of each conversion when the auto-zero switch is turned off. The AØ14 and A156 both allow 1Ø microseconds between receiving the GO bit and accepting the input data as valid. Normally, this is sufficient time for the input transient to settle out. However, more time may be needed when the multiplexer is switching into an input channel with high source impedance, particularly when large amounts of shunt capacitance exist in the interconnecting cables. Source impedance/cable shunt capacitance products greater than 1 microsecond should be avoided whenever conversions are to be made

at maximum rate with less than one-half LSB error. This means that cable shunt capacitance for a 1000 ohm source should not exceed 1000 pF ($10^3 \times 10^{-9} = 10^{-6}$), that shunt capacitance for a 100 ohm source should not exceed 0.01 microfarad ($10^2 \times 10^{-8} = 10^{-6}$), etc. Assuming twisted pair cable capacitance of 165 pF/m (50 pF/ft), these constraints translate into a maximum run of 6 m (20 ft) from a 1000 ohm source, 60 m (200 ft) from a 100 ohm source, etc. These values are consistent with good practice for avoiding noise pickup in long cable runs. Settling errors can be eliminated by increasing the time between conversions or incorporating a software delay between channel changes and program start commands.

Physical Restrictions

1. Analog subsystem signals are not carried from chassis to chassis by the D-bus cable; therefore, the A/D converter and all of its multiplexers must reside in the same (H333 or H334) chassis.

2. Although a small analog subsystem may use only part of its assigned chassis, it is recommended that the user not utilize any of the remaining module slots for digital I/O modules. To do otherwise may result in serious degradation of the analog subsystem's accuracy due to crosstalk.

A user may sometimes be willing to tolerate some degradation if it is not detrimental to his application. Predicting the degree of degradation is complicated by the number of possible configurations (hardware and software). Some insight into what to expect can be gained by examining the following measured effects of module placement on subsystem performance.

An M5013 ac input module was placed in the slot adjacent to the A014. Its inputs were exercised with a switched 120 V, 60 Hz signal while the effect of this activity on the performance of the A014 was monitored (Figure 6-17-3). The A014 channel input was configured with a 1000 ohm unbalanced source. Worst case effects over several minutes were recorded for this configuration. The measurement was repeated after moving the M5013 and its screw terminals left to increase the spacing between the M5013 and A014. Measurements were made with and without a grounded shield between the modules. Maximum deviations of the converted data are recorded in Table 6-17-6. Voltage spike amplitudes in the M5013 inputs are several hundred volts and represent an extreme condition. Lower level digital modules should produce less dramatic effects.

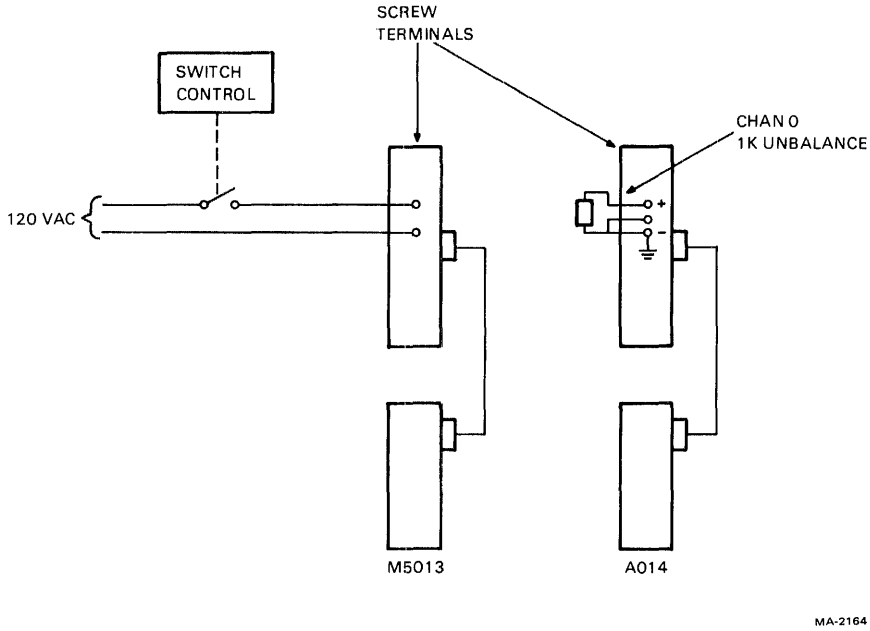


Figure 6-17-3 Crosstalk Measurement Configuration

Table 6-17-6 Crosstalk Error Measurements

Maximum Deviation of AØ14 Output (LSBs)

	No. of Empty Module Slots			
Spacing	Ø	1	3	6
No shield	±34	±13	±2	±2
Shield	±24	±13	±2	±2

Analog Input Subsystem Handshaking Signals

When an external multiplexer is selected, there are control signals passed between the A/D converter and the multiplexer via the D-bus. These signals are described below.

D MUX STROBE — Asserted by the A/D converter to an external multiplexer. Enables the addressed multiplexer to put data on the D-bus in response to D DIN or accept data in response to D DOUT.

D MUX READY — Asserted by the selected multiplexer when its analog data signal is valid. Negated by the multiplexer in response to D AUTO ZERO, when the analog auto-zero signal has settled.

D AUTO ZERO — Asserted by the A/D converter at the beginning of the auto-zero phase of the conversion cycle. This occurs after the internal sample and hold has acquired and held the signal data from the multiplexer. This signal places the preamplifier of the selected multiplexer in the auto-zero mode.

D MUX REL — Asserted by the A/D converter at the end of the conversion cycle. Places all subsystem multiplexers in the idle state.

D ANA ERROR — Asserted by the addressed multiplexer if:

1. A nonexistent channel has been written
2. A nonexistent gain has been written.

This signal sets the error bit in the A/D converter's status register.

The timing diagram of Figure 6-17-4 shows a typical sequence of handshaking signals. The exchange begins with the D MUX STROBE signal that is output by the A/D when a multiplexer other than zero is addressed. This occurs when the multiplexer's number is written in the analog subsystem's A2 byte. This causes the multiplexer to set its internal SEL flip-flop, store the multiplexer and channel number data, and put the selected analog signal on the D ANA SIG line of the D-bus.

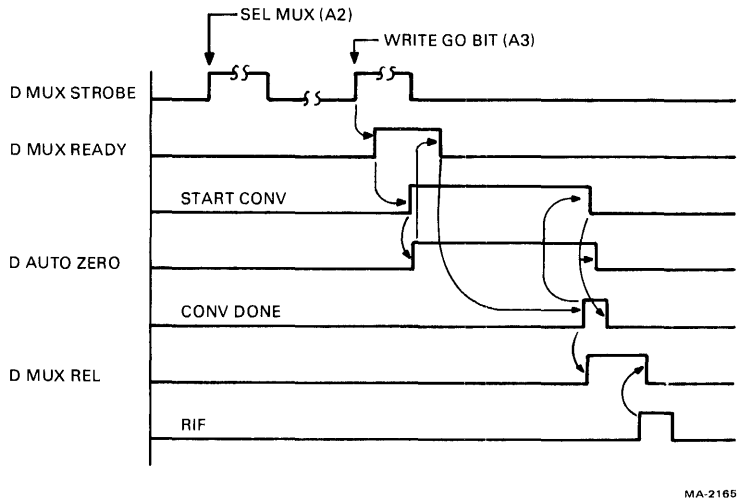


Figure 6-17-4 Analog Subsystem Handshaking

The A/D outputs the D MUX STROBE signal again when the program writes the GO bit in the subsystem's A3 byte. This time the selected multiplexer sets its internal GO flip-flop and after an appropriate time delay (for data settling), sets its READY flip-flop. This puts the D MUX READY signal on the D-bus. When the A/D converter receives this signal, its internal START CONV flip-flop is set. This puts the D AUTO ZERO signal on the D-bus. The multiplexer now puts its preamplifier in AUTO ZERO mode and after a suitable time delay negates D MUX READY. This enables the A/D to start conversion.

When the A/D finishes converting, it outputs the CONV DONE signal. This signal sets the A/D's DONE flip-flop producing the D MUX REL signal and resetting the START CONV flip-flop, which terminates the D AUTO ZERO and CONV DONE signals. D MUX REL clears the multiplexer's SEL and GO flip-flops, and is itself cleared when the A/D data is read with the RIF bit = 1 in the CSR.

FUNCTIONAL DESCRIPTION

The A014 is a 12-bit A/D converter module used to acquire analog field signals and convert them to digital data for transactions on the I/O Subsystem D-bus. The module has a built-in multiplexer that allows 16 single-ended or eight differential inputs. Additional inputs (up to 240 single-ended or 120 differential) can be accommodated by utilizing expansion multiplexer modules. Provision is made for program-controlled testing and for reading the module's generic code. The module features series fusible resistors and clamping diodes for input overvoltage protection, and switches for selecting the address and input mode.

GENERAL DESCRIPTION

The following discussion is based on the assumption that the reader has read and is familiar with the material in the preceding section, "Analog Input Subsystem - General."

A block diagram of the A014 module is shown in Figure 6-18-1. Analog field signals entering at J36 are converted and the results of the conversion are stored in the A/D data register. This data is put on the module's internal TS-Bus and then to the D-bus. The right side of the figure shows that the A/D data register shares the TS-Bus with several other registers. These registers contain additional information, such as A/D status, generic codes, channel number, and multiplexer number. This data is also output to the D-bus under appropriate addressing and control conditions. The relevant enabling signals are shown with each register and are derived from the I/O control section, discussed in a later paragraph.

Other parts of Figure 6-18-1 show the I/O data paths and the various control sections that regulate the module's channel selection, A/D conversion, and D-bus data transactions.

Physically the module consists of a motherboard and a daughterboard as shown in Figure 6-18-2. The functionality of the module is partitioned as shown by the heavy dashed line in Figure 6-18-1.

The remainder of this section covers the module's major functions in more detail.

Channel Selection

The top left of Figure 6-18-1 shows that all channels (analog field signals) are input to J36, the field interface connector, and through the fusible resistors to the internal multiplexers. The fusible resistors, along with clamping diodes, provide protection from field overvoltage conditions.

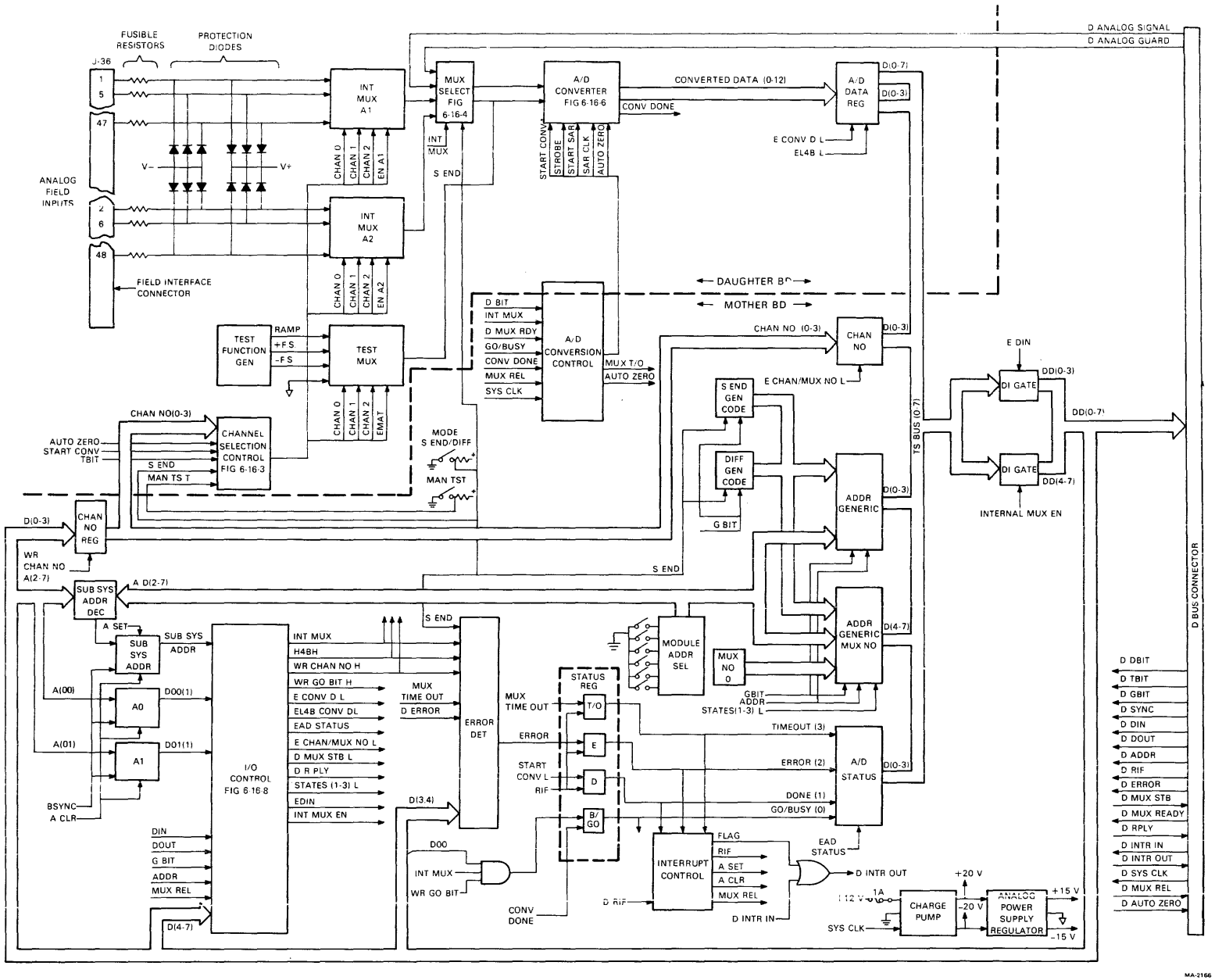


Figure 6-18-1 Module A014 A/D Converter, Block Diagram

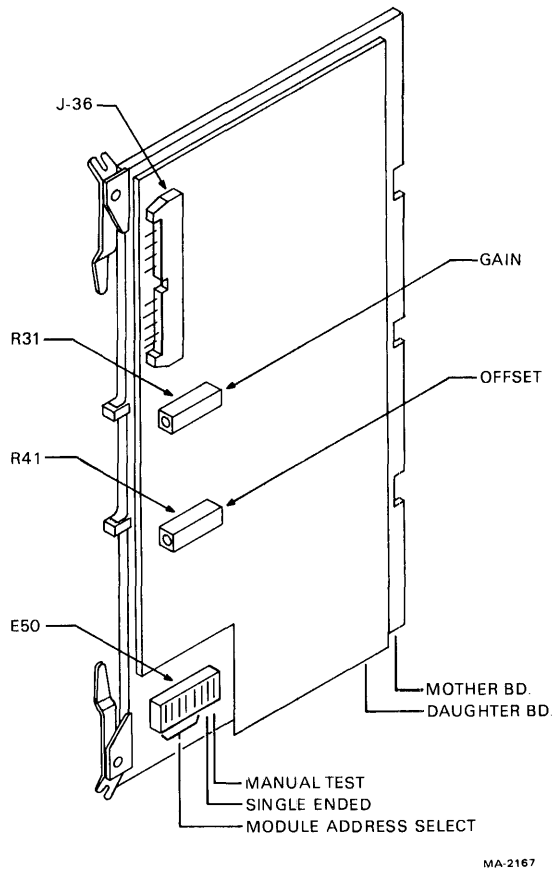


Figure 6-18-2 AØ14 A/D Converter Module

Channel selection controls cause the multiplexers to select a channel according to the contents of the channel number register and the position of the S END switch. Figure 6-18-3 shows the detailed logic of this part of the circuit in single-ended mode.

In addition to the field signal inputs, a test multiplexer selects one of four A/D test signals. These signals are created by a built-in test function generator and consist of a full-scale ramp function, a positive test voltage, a negative test voltage, and ground.

Multiplexer Select
The multiplexer select circuit selects either the internal or external multiplexer and also provides either a single-ended or differential input to the A/D converter. A simplified version of the multiplexer select circuit in Figure 6-18-4 shows a configuration where an external multiplexer is selected.

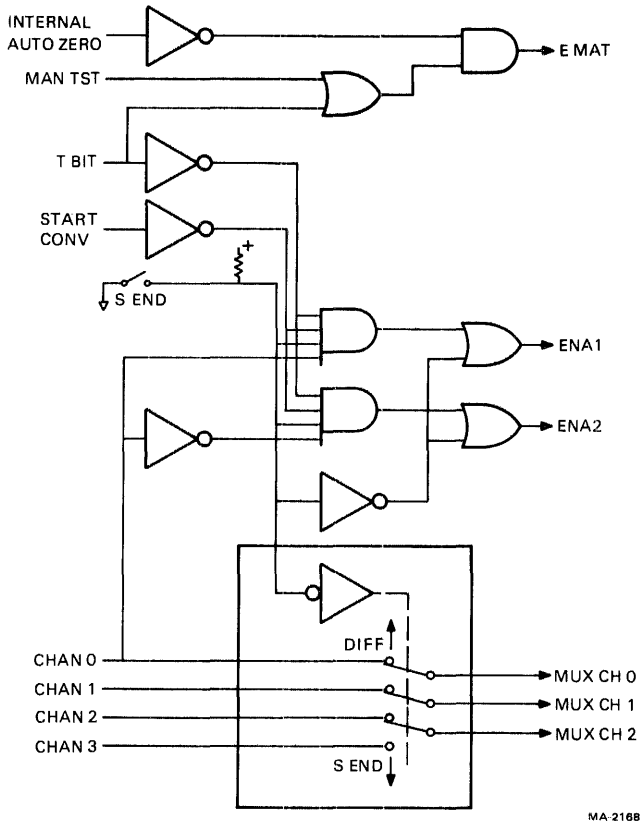


Figure 6-18-3 Channel Select Control

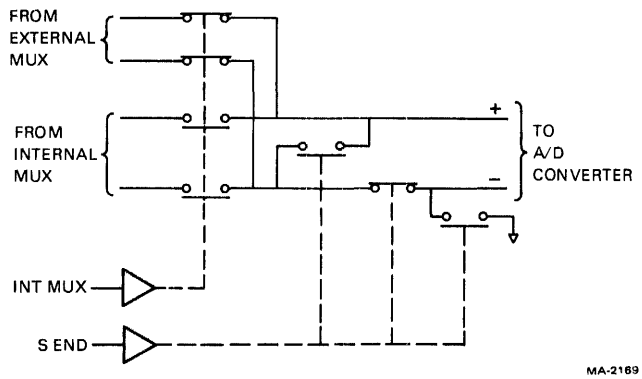


Figure 6-18-4 Multiplexer Select

A/D Conversion Section
The AØ14 A/D converter accepts bipolar inputs of ±1Ø.24 V (2Ø.48 V peak-to-peak). It utilizes a successive approximation conversion process and delivers a 12-bit, offset, binary-encoded output to the A/D data register (Figure 6-18-1).

Successive Approximation Conversion Process
Successive approximation refers to the type of conversion process utilized. This is a process whereby the input signal is examined first to determine if it is greater than or less than 1/2 full scale. If greater, a one is assigned to the MSB and the value of this bit (1/2 scale) is subtracted from the input; if less, a zero is assigned to the MSB and the input is left as is. This constitutes the first approximation. Whatever remains of the input signal is now less than 1/2 scale. A second comparison is then made to determine if the residual analog input is greater than 1/4 scale; if it is, a one is assigned to the second MSB.

These successive approximations continue for 1/8, 1/16 . . . scale, for as many iterations as there are output bits. A flow diagram for a typical successive approximation converter is shown in Figure 6-18-5.

Offset Binary Encoding and Resolution
This A/D converter is a 12-bit device that accepts bipolar inputs of ±1Ø.24 V full scale. Twelve bits allow 4Ø96 discrete output states, corresponding to 4Ø96 input voltage levels. One of these levels is used for Ø V. There are 4Ø95 states remaining; therefore, there can be no even division between the positive and negative inputs. Zero is considered to be a positive number and the extra level is assigned to the negative inputs. Therefore, full scale is one LSB less than minus full scale.

Since there are 4Ø96 levels and the peak-to-peak input voltage range is 2Ø.48 V (±,1Ø.24 V), the LSB has a weight of 2Ø.48/4Ø96 = 5 mV.

Without describing all 4Ø96 I/O conditions, the situation can be visualized by examining the abbreviated representation in Table 6-18-1.

A/D Converter Circuit Operation
The A/D converter accepts the analog input that has been selected by the multiplexers and converts it to a 12-bit digital word for input to the program.

A simplified schematic of the module's A/D section is shown in Figure 6-18-6. The converter is basically a differential input device that is reconfigured for single-ended operation when the multiplexer select circuit grounds its negative input.

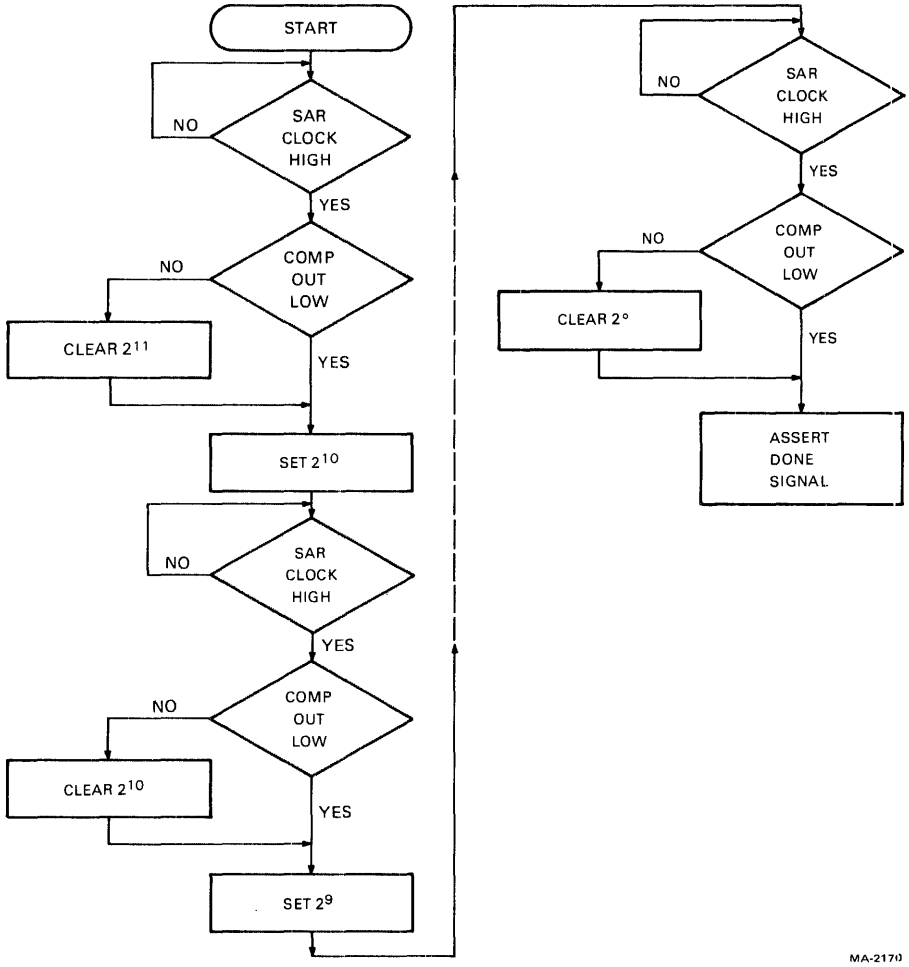


Figure 6-18-5 Successive Approximation, Flow Diagram

Table 6-18-1 Offset Binary Encoding

Input Magnitude	Binary Output Code	Input Voltage (Ideal) Nominal	Range
+FS - 1 LSB	1 1 1 1 1 1 1 1 1 1 1 1	+10.2350 V	>10.2325 V
+FS - 2 LSB	1 1 1 1 1 1 1 1 1 1 1 0	+10.2300 V	(10.2275, 10.2325) V
.	.	.	.
.	.	.	.
+FS/2	1 1 0 0 0 0 0 0 0 0 0 0	+5.1200 V	(5.1175, 5.1225) V
.	.	.	.
.	.	.	.
+2 LSB	1 0 0 0 0 0 0 0 0 0 1 0	+10 mV	(7.5, 12.5) mV
+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1	+5 mV	(2.5, 7.5) mV
Zero	1 0 0 0 0 0 0 0 0 0 0 0	0 V	(-2.5, +2.5) mV
-1 LSB	0 1 1 1 1 1 1 1 1 1 1 1	-5 mV	-(2.5, 7.5) mV
-2 LSB	0 1 1 1 1 1 1 1 1 1 1 0	-10 mV	-(7.5, 12.5) mV
.	.	.	.
.	.	.	.
-FS/2	0 1 0 0 0 0 0 0 0 0 0 0	-5.1200 V	-(5.1175, 5.1225) V
.	.	.	.
.	.	.	.
-FS + 1 LSB	0 0 0 0 0 0 0 0 0 0 0 1	-10.2350 V	-(10.2325, 10,2375) V
-FS	0 0 0 0 0 0 0 0 0 0 0 0	-10.2400 V	<-10.2375 V

Note:
Plus full scale can not be realized (see text).

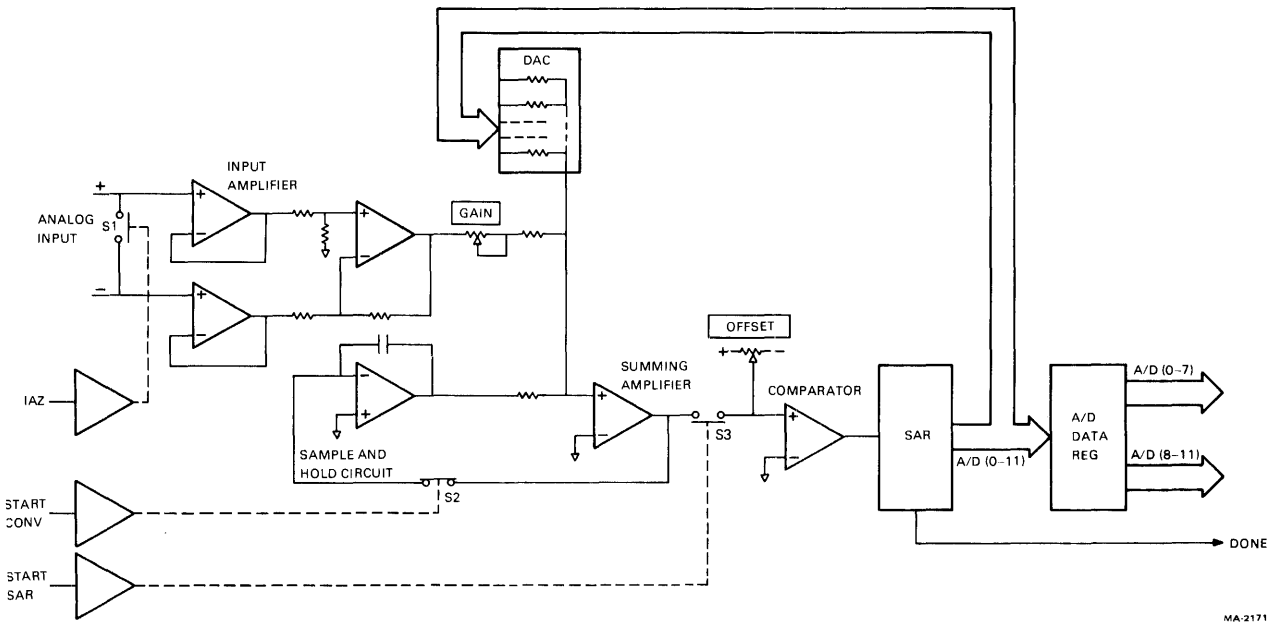


Figure 6-18-6 A/D Converter Section, Simplified Circuit Diagram

Operation of the converter is the same for either input configuration and is briefly illustrated by the subsystem timing diagram of Figure 6-18-7, which shows the A/D cycle.

The timing diagram shows that as soon as the selected multiplexer is enabled, the analog signal is sampled and continues to be sampled until a short time after the GO bit is written. At this point the multiplexer goes into auto-zero mode. After another short delay, the conversion starts. Conversion is then in progress until the DONE bit is set, at which time the output data can be read. Note that the A/D converter output is 12 bits, so two bytes must be read to get all the data.

The program initiates the conversion cycle by writing the GO bit in the status register. This action is asynchronous with the 100 kHz system clock, while the conversion cycle is synchronized to the system clock. The GO bit also starts the TIME OUT delay, which will result in a TIME OUT signal if the delay is not reset by D MUX RDY or an internal multiplexer ready signal. If it occurs, the TIME OUT signal sets the TIME OUT bit in the status register.

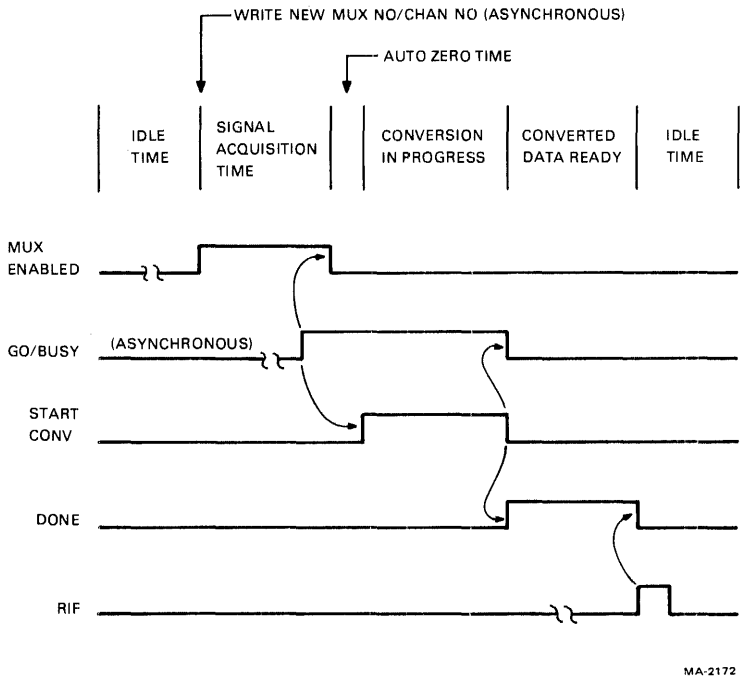


Figure 6-18-7 Analog Subsystem Timing

I/O Control Section

When the A/D converter (analog subsystem) is addressed, this event is decoded and, at D SYNC time, the SUBSYS ADDR flip-flop is set. At the same time, the two low-order address bits (DØØ,DØ1) are stored. These signals, plus the usual D-bus control signals (DIN, DOUT, GBIT), are the major inputs to the I/O control section of Figure 6-18-8. The figure shows that the DØØ and DØ1 flip-flops are decoded to produce one of the A(Ø-3) signals, which identifies the particular subsystem address that is being read or written (refer the section "Analog Input Subsystems - General," Table 6-17-1).

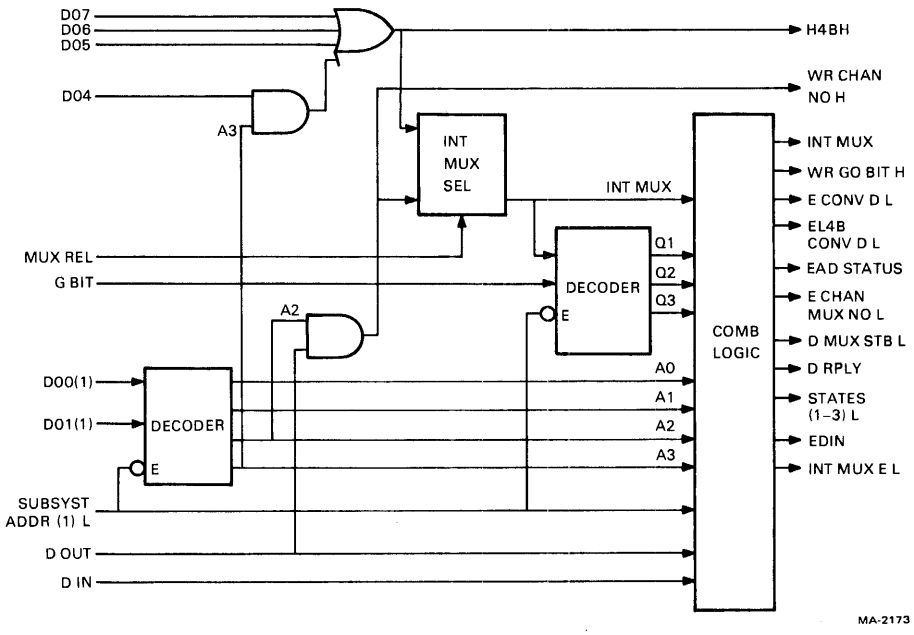


Figure 6-18-8 I/O Control

The GBIT and INTERNAL MUX signals are decoded to produce one of the Q(1-3) signals that selects the proper generic code.

The INTERNAL MUX SEL flip-flop is written when the A2 address is written, provided bits (5-7) are all zero (zero is the code for selecting the internal multiplexer).

The remainder of the I/O control section consists of combinatorial logic that creates the appropriate I/O control signals for each type of data transaction. Details of this logic are shown in the module's print set.

Error Detector
The error detection circuit sets the error bit in the module's status register. Details of this circuit are shown on the module's print set. The following conditions cause an output from the error detection circuit.

1. an EXT MUX ERROR signal
2. a MUX TIME OUT signal
3. writing an incorrect gain code
4. writing an incorrect channel number code.

Status Register
This register provides conversion status information to the program and initiates interrupts (Figure 6-18-1). For an explanation of the individual status bits, refer Table 6-17-4 of the "Analog Input Subsystem - General" section.

Interrupt Control Signals
Three of the status register bits (DONE, ERROR, and T/O) are input to the module's interrupt control section. When one of these bits is set, the interrupt control section produces a FLAG signal and if all priority conditions are met, a processor interrupt occurs (the FLAG signal is an input to the D INTR IN, D INTR OUT daisy-chain). When an interrupt occurs, a modified D-bus Cycle is initiated by the IOCM. This results in the D ADDR signal, which puts the module's address on the TS-Bus and causes the interrupt control section to produce the A SET and SUB SYS ADDR signals. When D DIN is asserted, the module's address is put on the D-bus.

At this point the processor has identified the interrupting address. The appropriate interrupt routine is then executed. If now the processor RIFs the module (reads the module's address with R=1 in the CSR of the IOCM), the interrupt control section resets the status bit that produced the flag.

Address, S END, and Manual Test Selection
The four analog subsystem addresses are selected on the A/D converter module according to the rules stated in Chapter 4. They are selected on the module by the 8-pole switch, E5Ø, shown in Figure 6-18-2. An example of one possible address selection is shown in Figure 6-18-9 to illustrate the use of this switch. Positions 7 and 8 are used for S END and MANUAL TEST as shown in the figure.

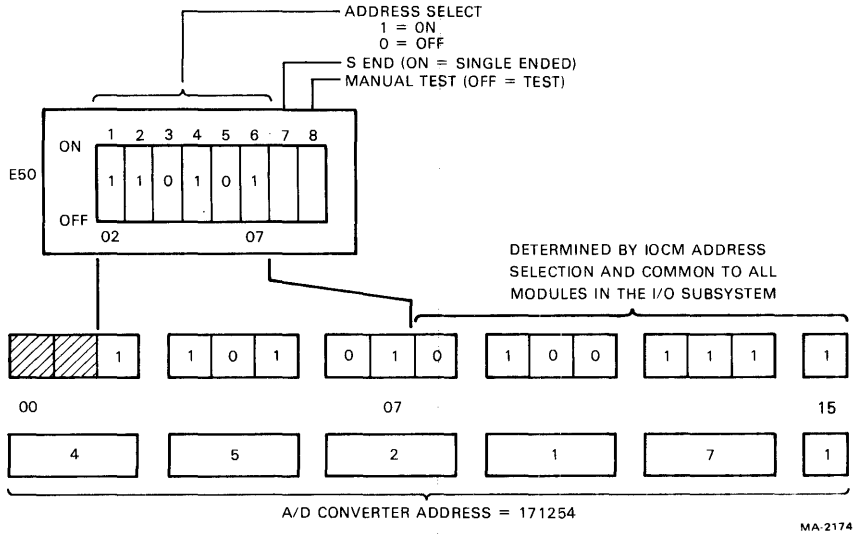


Figure 6-18-9 AØ14 Module - Address, S END, and Manual Test Selection

Generic Code
The AØ14 module may have one of two generic codes depending on the position of the S END switch: 3Ø1 DIFFERENTIAL and 321 SINGLE-ENDED.

Pin Connections
The AØ14 module pin connections for J36 the I/O cable connector are shown in Table 6-18-2.

Screw Terminal Connections
The reader should refer to Chapter 3, Paragraph 3.8.5, for general field interface information and then to Table 6-18-3 for this module's screw terminal configuration.

Calibration
Calibration of the A/D converter module is accomplished by means of diagnostics included with the I/O Subsystem. Instructions for using these diagnostics are included with the software package. Normally the module is calibrated and ready for service when received by the customer; however, if field adjustment is contemplated, the adjustments mentioned in the diagnostic (gain and offset) are identified in Figure 6-18-2.

To ensure compliance with specifications, all test equipment used for calibration of the AØ14 must have been accurately and recently calibrated. In addition, personnel doing the calibration should be familiar with aligning precision analog equipment. If you are not sure of the foregoing, DO NOT ATTEMPT TO CALIBRATE THE AØ14. Factory calibration is probably better than that which you will be able to accomplish.

Table 6-18-2 Module A014 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	00	2	01
3		4	
5	02	6	03
7		8	
9	04	10	05
11		12	
13	06	14	07
15		16	
17		18	
19		20	
21		22	
23		24	
25	Ground	26	Ground
27		28	
29		30	
31		32	
33		34	
35	10	36	11
37		38	
39	12	40	13
41		42	
43	14	44	15
45		46	
47	16	48	17
49		50	

Table 6-18-3 Type A Screw Terminal 16/32 Bit (BC40A)
A014 A/D Converter Module Field Termination Configuration

Field Channel Number			Screw Terminal Number
DIFF		S END	
	+	ØØ	1
ØØ	-	Ø1	2
			3
			4
	+	Ø2	5
Ø1	-	Ø3	6
			7
			8
	+	Ø4	9
Ø2	-	Ø5	1Ø
			11
			12
	+	Ø6	13
Ø3	-	Ø7	14
			15
			16
Ground		Ground	17
Ground		Ground	18
	+	1Ø	19
Ø4	-	11	2Ø
			21
			22
	+	12	23
Ø5	-	13	24
			25
			26
	+	14	27
Ø6	-	15	28
			29
			3Ø
	+	16	31
Ø7	-	17	32
			33
			34

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc (+2 or -1) Vdc Backup supply: 14 Vdc $\geq$ VB $\geq$ (VS-Ø.7) Vdc
Operating current	35Ø mA maximum

NOTE

If the backup supply is implemented, total operating current is shared.
Main supply: 3ØØ mA maximum
Backup supply: 5Ø mA maximum

Standby current (backup supply)	35Ø mA maximum

Input Characteristics

Voltage range	-1Ø.24 V to +1Ø.24 V, 1 LSB = Ø.ØØ5 V
Input impedance	Power on: >5Ø M ohm Power off: 1ØØØ ohm
Signal and common mode voltage capability	$\pm$12 V minimum
Channel to channel offset	$\pm$1ØØ microvolt maximum
Gain	Unity
Overall accuracy	$\pm$2 LSBs @ 25 degrees C ambient maximum $\pm$4 LSBs from Ø degrees C to 6Ø degrees C ambient, maximum

NOTE

This includes gain and offset errors which can be adjusted to zero, leaving nonlinearity as the only nonreducible error.

Nonlinearity (integral and differential)	$\pm$1/2 LSB maximum over temperature range
Common mode rejection	1ØØ dB minimum (dc to 6Ø Hz with 1K source unbalance)

Noise	No D-bus activity ±Ø.15 LSB typical ±1/2 LSB maximum D-bus activity ±Ø.3 LSB typical ±1/2 LSB maximum

NOTE

The above specifications refer to the 3-sigma limit of Gaussian noise. Spike noise generated by adjacent digital I/O modules may exceed these limits by a considerable margin. For guaranteed operation within the noise specification limits, digital and analog I/O should not be implemented in the same chassis. (See discussion in note 2 under Physical Restrictions in the section "Analog Input Subsystem - General.")

Conversion speed	59 microseconds average 54 microseconds minimum 64 microseconds maximum

NOTE

There is a 1Ø microsecond uncertainty due to the asynchronous relationship between start of a conversion and the system clock.

Bandwidth	No limitation beyond conversion speed. Internal sample-hold is provided.
Protection	Input circuits are protected from field overvoltages by diodes to ±13 V and by fusible resistors in series with each input. A 1 A fuse protects the circuit board etch in the event of circuit failure.
Physical Characteristics	Two quad modules assembled as a mother-daughter combination make up the AØ14 module.
Dimensions	Quad module, triple width, 8-1/2 inch length

Field connector	Cable type BC40A or customer-supplied 50-pin Berg connector
Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degrees C ambient.
Heat dissipation	15 Btu/hr maximum

FUNCTIONAL DESCRIPTION

The A156 multiplexer module is used in the H333 I/O subsystem to provide additional input channels to the AØ14 A/D converter. The module provides for either 32 single-ended or 16 differential input channels. Of these modules, 7 may be used to provide up to 224 additional channels for the AØ14. The module has fusible resistors and clamping diodes for input protection and switches for selecting the multiplexer number and single-ended or differential operating mode. Provision is made for reading the module's two generic codes that identify the module and its operating mode.

DETAILED DESCRIPTION

The following discussion of the A156 module is based on the assumption that the reader is familiar with the material in the preceding section, "Analog Input Subsystem - General."

A simplified block diagram of the module is shown in Figure 6-19-1. The upper portion of the figure shows the multiplexer and preamplifier section that selects an analog field signal from J1 and delivers it to the AØ14 via the D-bus. The lower part of the figure shows the data registers, D-bus interface circuits, and the module's major control functions. The following paragraphs contain detailed discussions of the major sections.

Multiplexer Preamplifier

The top left portion of Figure 6-19-1 shows that all channels (analog field signals) are input to the multiplexer via J1, the field interface connector, and the fusible resistors. The fusible resistors, along with clamping diodes, provide protection from field overvoltage conditions. The channel selection controls cause the multiplexer to select a channel according to the contents of the channel number register.

The selected channel is input to the preamplifier circuit which is configured by the three switches preceding it to operate in either single-ended or differential mode. For example, when sampling in single-ended mode, switch T is open and the other two (M and S) are closed; the opposite is true for differential mode.

When the multiplexer is selected, the SEL L switch is closed and the preamplifier output is connected to the A/D converter module via the D ANA SIG and D ANA GUARD lines on the D-bus. The other control signals for this section are provided by the channel select and preamplifier control section. Table 6-19-1 summarizes the operating state configurations.

Data Paths

Figure 6-19-1 shows that D-bus data input to the module is stored in the channel and multiplexer number registers. These are read-write registers that store the multiplexer and channel

selection data if the multiplexer data matches the setting of the module's multiplexer number select switches. The contents of these registers are transmitted to the output select circuit which also receives the module's read-only data from the generic code and multiplexer gain registers. This circuit outputs the multiplexer/channel number data unless the GBIT L or GAIN L signal is asserted, in which case it will output information from one of those registers. The selected data is input to the DI gating section where it is strobed onto the D-bus by the LO GATE L and HI GATE L signals.

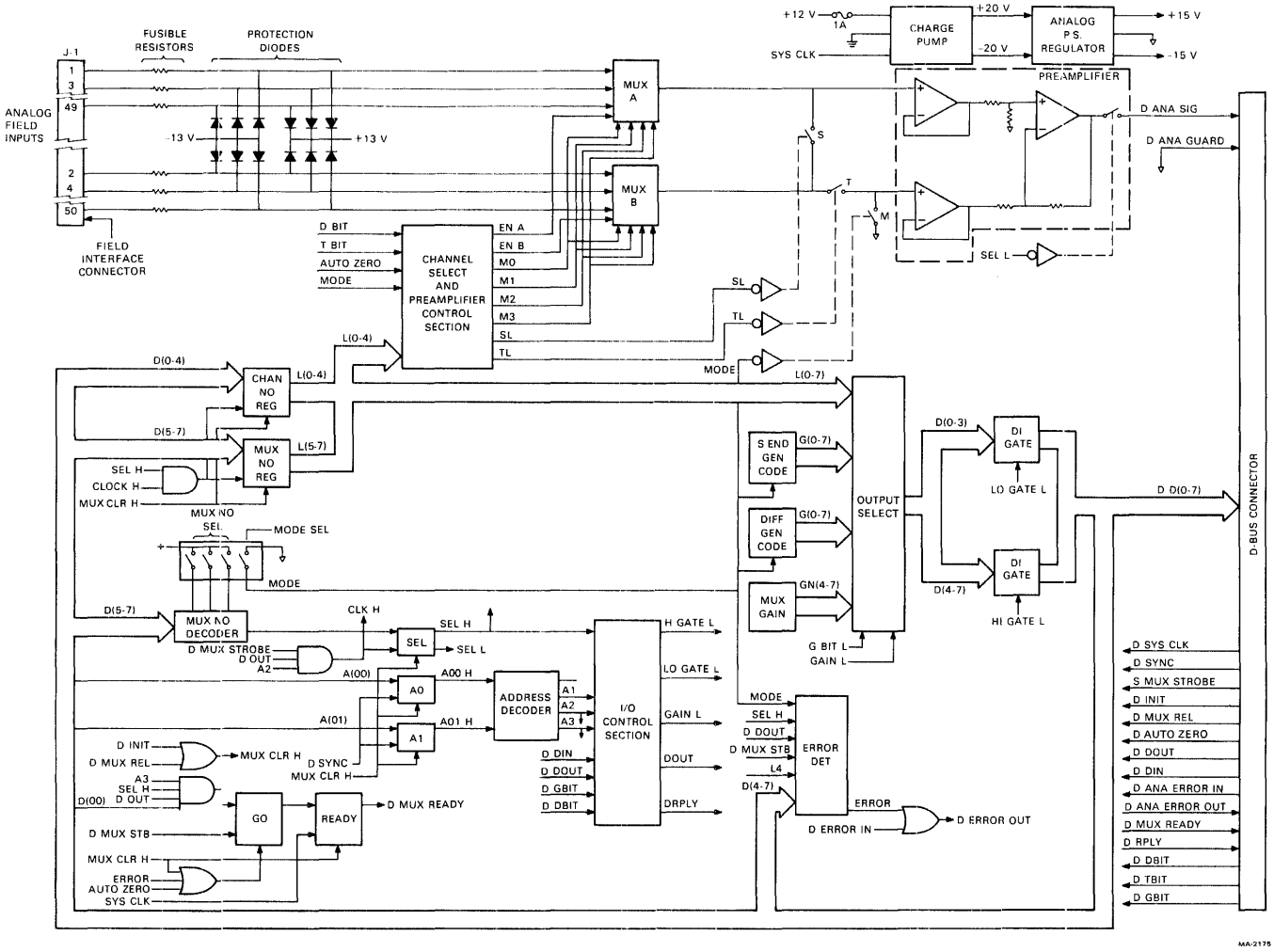


Figure 6-19-1 A156 Analog Multiplexer, Block Diagram

Table 6-19-1 A156 Operating States

Mode	State	Circuit Configuration				
		Switch			Mux	
		S	T	M	A	B
DIFF	Sample time	Ø	1	Ø	1	1
	Auto-zero time	1	1	Ø	Ø	1
S END EVEN CHAN	Sample time	1	Ø	1	1	Ø
	Auto-zero time	1	1	1	Ø	Ø
S END ODD CHAN	Sample time	1	Ø	1	Ø	1
	Auto-zero time	1	1	1	Ø	Ø

1 = on or enabled
Ø = off or disabled

Data Control Signals

When the program writes an external multiplexer number and channel number to the analog subsystem's A2 address, the A/D converter outputs the D MUX STROBE signal causing the multiplexer to decode its number and set its SEL flip-flop. (The SEL flip-flop is the module's data transaction enabling flip-flop; once set, it remains set until D MUX REL occurs.) This action causes the module to store the multiplexer number and channel number data (Figure 6-19-1).

When the program writes the GO bit in the subsystem's A3 byte, the selected module's GO bit is set. The GO flip-flop arms the READY flip-flop, which sets when the next system clock pulse occurs. This causes D MUX READY to be asserted, which indicates to the A/D converter module that the analog signal from the multiplexer will be valid on the next system clock pulse. On this clock pulse, the A/D accepts the analog data from the multiplexer and asserts D AUTO ZERO. Assertion of D AUTO ZERO disarms the READY flip-flop, which resets on the next system clock pulse, negating D MUX READY. Assertion of D AUTO ZERO also places the preamplifier in the auto-zero mode (Table 6-19-1).

When the program reads the A2 address of the analog subsystem, the multiplexer's I/O control section decodes the address byte, and when D DIN occurs, produces the HI GATE L and LO GATE L signals causing the module's multiplexer number and channel number to be put on the D-bus. If the A3 address is read, only the GAIN L and HI GATE L signals are produced. This puts the multiplexer gain code on the D-bus in bit positions 4-7. (The gain code for the

A156 module is zero.) At the same time, the A/D module supplies its status register contents in bit positions Ø-3.

Reading either the A2 or A3 byte with the GBIT asserted causes the module to place one of its generic codes on the D-bus. The A156 has different generic codes for single-ended and differential modes. The MODE switch selects the proper code. If either the DBIT or TBIT is asserted, the module is placed in the auto-zero mode.

When the A/D module asserts the D MUX REL signal, the A156 resets its SEL and GO flip-flops.

Multiplexer Number and Mode Selection

The multiplexer number and operating mode (differential or single-ended) are selected on the module by the 4-pole switch, E1 (Figure 6-19-2). An example of one possible multiplexer selection is shown in Figure 6-19-3 to illustrate the use of this switch.

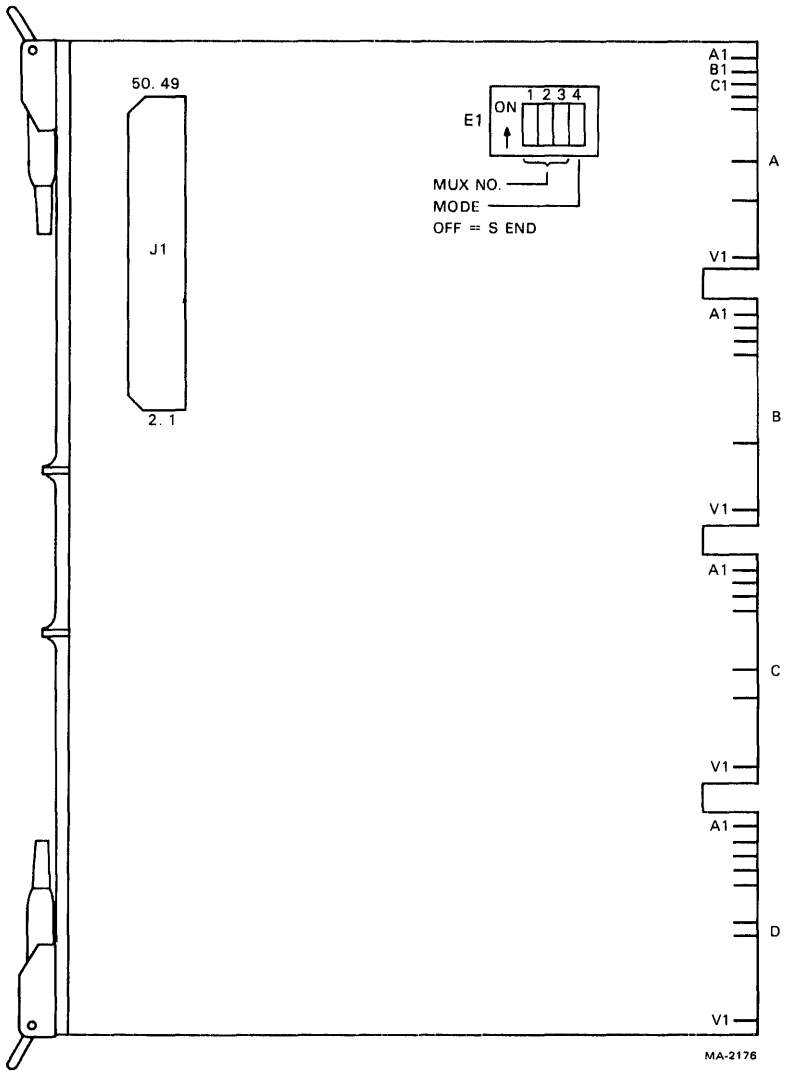


Figure 6-19-2 A156 Analog Multiplexer Module

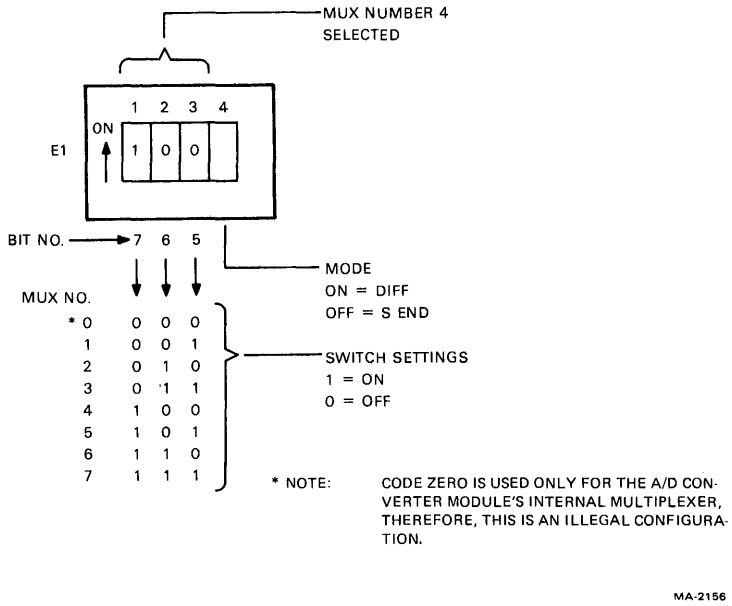


Figure 6-19-3 Multiplexer and Mode Selection

Software Restrictions

1. Once an A156 multiplexer has been selected, another external multiplexer cannot be selected without first doing one of the following.

   a. Starting an A/D conversion

   b. Reading the AØ14 with the RIF bit set in the CSR of the IOCM

   c. Causing a gain or channel error condition on the A156 module

2. The A156 must not be written during a conversion; this causes erroneous results.

3. The multiplexers are released at the end of a conversion; therefore, the multiplexer number, channel number, and gain registers contain invalid data and must be reprogrammed before another conversion is started.

Generic Codes

The generic code of the A156 module is octal 322 for differential mode and 342 for single-ended mode.

Pin Connections

The A156 module pin connections for J1 the I/O cable connector are shown in Table 6-19-2.

Table 6-19-2 Module A156 I/O Pin Connections

Module I/O Connector Pin	Field I/O Channel S END	DIFF	Module I/O Connector Pin	Field I/O Channel S END	DIFF
1	Ø0	+Ø0	2	Ø1	-Ø0
3	Ø2	+Ø1	4	Ø3	-Ø1
5	Ø4	+Ø2	6	Ø5	-Ø2
7	Ø6	+Ø3	8	Ø7	-Ø3
9	10	+Ø4	10	11	-Ø4
11	12	+Ø5	12	13	-Ø5
13	14	+Ø6	14	15	-Ø6
15	16	+Ø7	16	17	-Ø7
17 }			18 }		
19			20		
21			22		
23			24		
25 } Common			26 } Common		
27			28		
29			30		
31			32		
33 }			34 }		
35	20	+10	36	21	-10
37	22	+11	38	23	-11
39	24	+12	40	25	-12
41	26	+13	42	27	-13
43	30	+14	44	31	-14
45	32	+15	46	33	-15
47	34	+16	48	35	-16
49	36	+17	50	37	-17

Screw Terminal Connections

The reader should refer to Chapter 3, Paragraph 3.8.5, for general field interface information. The A156 uses the BC40A screw terminal assembly. Refer to Table 6-19-3 for this module's screw terminal configuration.

Table 6-19-3 Module A156 Screw Terminal Connections

BC40A Screw Terminal

Field Channel Number			Screw Terminal Number
DIFF		S END	
	+	Ø	1
Ø	-	1	2
	+	2	3
1	-	3	4
	+	4	5
2	-	5	6
	+	6	7
3	-	7	8
	+	1Ø	9
4	-	11	1Ø
	+	12	11
5	-	13	12
	+	14	13
6	-	15	14
	+	16	15
7	-	17	16
Common		Common	17
Common		Common	18
	+	2Ø	19
1Ø	-	21	2Ø
	+	22	21
11	-	23	22
	+	24	23
12	-	25	24
	+	26	25
13	-	27	26
	+	3Ø	27
14	-	31	28
	+	32	29
15	-	33	3Ø
	+	34	31
16	-	35	32
	+	36	33
17	-	37	34

SPECIFICATIONS

All specifications refer to the A156 when used in combination with the AØ14 A/D converter.

Power Requirements

Voltage	Main supply: VS=12 Vdc (+2 or -1) Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc
Operating current (A156 only)	79 mA maximum

NOTE

If the backup supply is implemented, total operating current is shared.
Main supply: 75 mA maximum
Backup supply : 4 mA maximum

Standby current (backup supply) (A156 only)	25 mA maximum

Input Characteristics

Voltage range	-1Ø.24 V to +1Ø.24 V, 1 LSB = ±Ø.ØØ5 V
Input impedance	Power on: ≥ 5Ø M ohm Power off: 1ØØØ ohm
Signal and common mode voltage capability	±12 V minimum
Channel to channel offset	±1ØØ microvolts maximum
Gain	Unity
Overall accuracy	±3 LSBs at 25 degrees C ±5 LSBs from Ø degrees C to 6Ø degrees C ambient, maximum
Common mode rejection	1ØØ dB min (dc to 6Ø Hz with 1K source unbalance)
Conversion speed	69 microseconds average 64 microseconds minimum 74 microseconds maximum

NOTE

There is a 1Ø microseconds uncertainty due to the asynchronous relationship between start of a conversion and the system clock.

Bandwidth	No limitation beyond conversion speed
Protection	Input circuits are protected from field overvoltages by diodes to ± 13 V and by fusible resistors in series with each input. A 1 A fuse protects the circuit board etch in the event of circuit failure.
Physical Characteristics	
Dimensions	Quad module, triple width, 8-1/2 inch length
Field connector	Cable type BC40A or customer-supplied 50-pin Berg connector
Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degrees C ambient.
Heat dissipation	5 Btu/hr maximum

FUNCTIONAL DESCRIPTION

The A157 multiplexer module is used in the H333 I/O subsystem to provide programmable gain of field inputs to the AØ14 A/D converter. The module accepts up to 16 differential inputs that can be independently programmed for any one of eight different gains. As many as seven of these modules may be used to provide a total of 112 programmable gain inputs. Provision is made for identification of the module by reading its generic code. The module has fusible resistors and clamping diodes for input protection and switches for assigning the multiplexer number.

DETAILED DESCRIPTION

The following discussion of the A157 module is based on the assumption that the reader is familiar with the material in a preceding section, Analog Input Subsystem - General.

A simplified block diagram of the module is shown in Figure 6-2Ø-1. The upper portion of the figure shows the multiplexer and preamplifier section that selects an analog field signal from J1, applies the appropriate gain, and delivers it to the AØ14 via the D-bus. The lower part of the figure shows the data registers, D-bus interface circuits, and the module's major control functions. The following paragraphs contain detailed discussions of the major sections.

Multiplexer/Preamplifier

The top left portion of Figure 6-2Ø-1 shows that all channels (analog field signals) are input to the multiplexer via J1, the field interface connector, and the fusible resistors. The fusible resistors, along with clamping diodes, provide protection from field overvoltage conditions. The channel selection controls cause the multiplexer to select a channel according to the contents of the channel number register.

The selected channel is input to the preamplifier section which is configured to provide a gain according to the contents of the gain register. The input section of the preamplifier provides a gain of 1 or 5Ø, depending on the state of the G7 bit; the output section provides a gain of 1, 2, 4, 1Ø, or 2Ø according to the state of bits G(4, 6, 7). Since the two amplifiers are cascaded, the overall module gain is the product of the input amplifier and output amplifier gains. Table 6-2Ø-1 shows the manner in which the gains are derived.

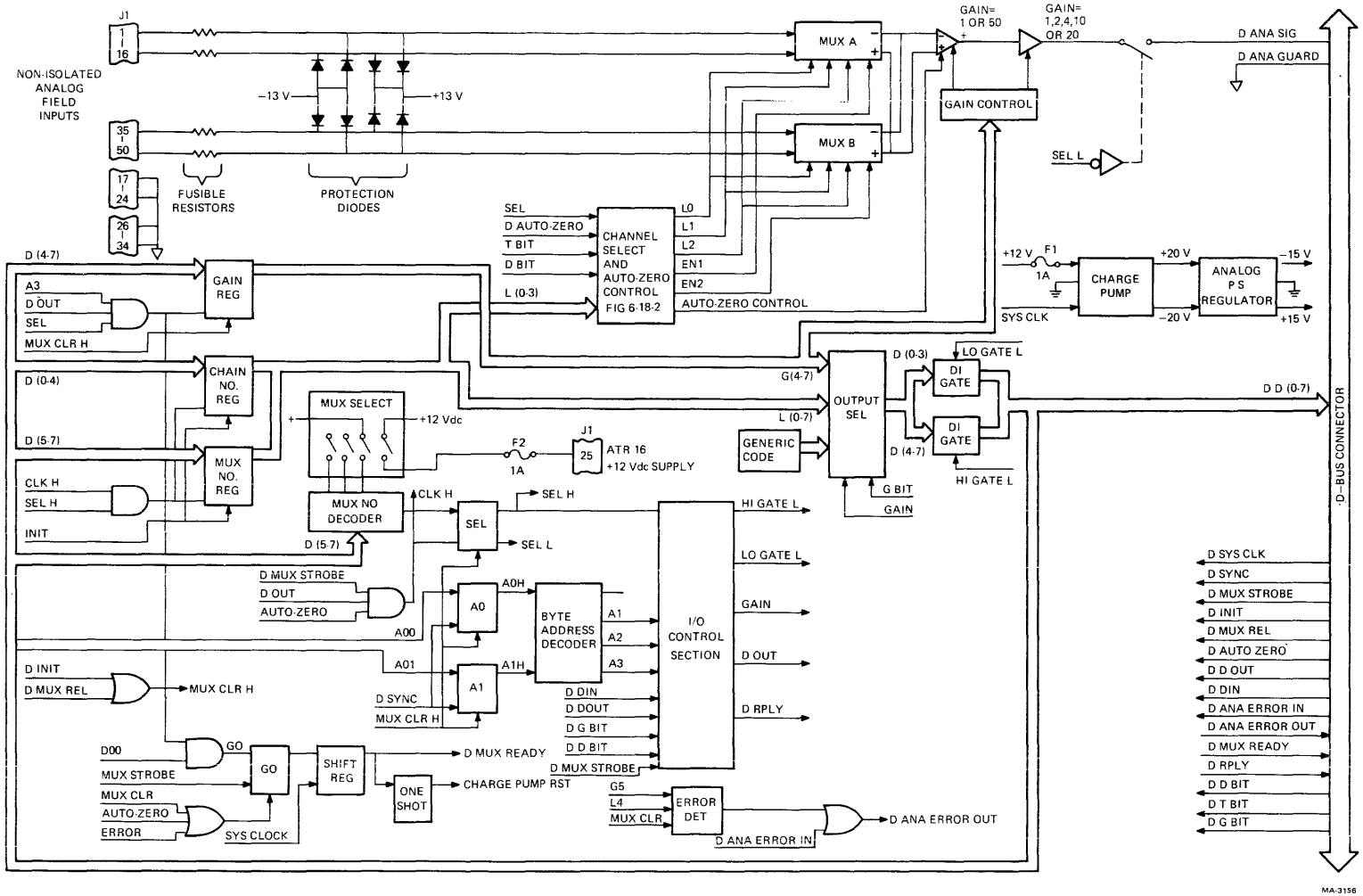


Figure 6-20-1 A157 Wide-Range Analog Multiplexer

Table 6-20-1 Gain Codes

7 6 5 4 ... 0	Input Amplifier Gain	Output Amplifier Gain	Overall Module Gain
0 0 0 0	1	1	1
0 0 0 1	1	2	2
0 1 0 0	1	10	10
0 1 0 1	1	20	20
1 0 0 0	50	1	50
1 0 0 1	50	2	100
1 1 0 0	50	4	200
1 1 0 1	50	20	1000

The other gains (those with G=5) are not implemented on this module, and if selected will result in an error.

When the multiplexer is selected, the SEL L switch is closed and the preamplifier output is connected to the A/D converter module via the D ANA SIG and D ANA GUARD lines on the D-bus. The other control signals for this section are provided by the channel select and auto-zero control section. Figure 6-20-2 shows the detailed logic of this section.

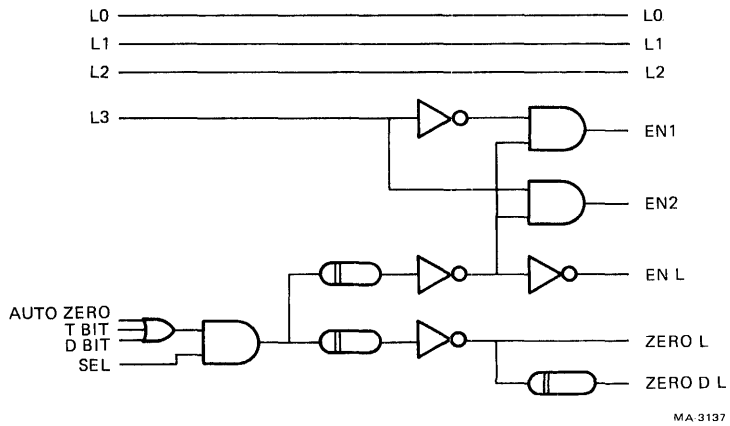


Figure 6-20-2 Channel Select and Auto-Zero Control

Data Paths

Figure 6-20-1 shows three read-write registers that store the channel number, multiplexer number, and gain. The contents of these registers are transmitted to the output select circuit, which also receives the module's read-only data from the generic code register. This circuit outputs the multiplexer/channel number data unless the GBIT H or GAIN H signal is asserted, in which case it outputs information from one of those registers. The selected data is input to the DI gating section where it is strobed onto the D-bus by the LO GATE L and HI GATE L signals.

Data Control Signals

When the program writes the multiplexer number assigned to an A157 and a channel number to the analog subsystem's A2 address, the A/D converter outputs the D MUX STROBE signal causing that multiplexer to decode its number and set its SEL flip-flop. (The SEL flip-flop is the module's data transaction enabling flip-flop; once set, it remains set until D MUX REL or D INIT occurs.) This action causes the module to store the multiplexer number and channel number data (Figure 6-20-1).

When the program writes the gain and the GO bit in the subsystem's A3 byte, the selected module stores the gain data and sets its GO bit. The GO signal is input to a shift register, which after a delay of 10 to 20 microseconds, syncs the module to the system clock. On the second clock pulse after the assertion of GO, the shift register outputs the D MUX READY signal to the D-bus and drives the RESET one-shot. (The RESET signal synchronizes the module's charge pump to the conversion cycle to ensure that large current surges on the power supply buses do not occur during conversion time.)

The D MUX READY signal indicates to the A/D converter module that the analog signal from the multiplexer is valid on the next system clock pulse. On this clock pulse, the A/D accepts the analog data from the multiplexer and asserts D AUTO ZERO (refer to timing diagram, Figure 6-20-3). Assertion of D AUTO ZERO to the multiplexer resets its GO flip-flop and places the preamplifier in the auto-zero mode as follows.

1. The multiplexers are disabled by EN H.

2. The holding capacitor is disconnected from the input by EN L (Figure 6-20-4).

3. The preamplifier plus and minus inputs are shorted by ZERO L.

4. The common mode voltage is connected to the preamplifier input by ZERO D L.

Two clock pulses after the GO flip-flop is reset, the D MUX READY signal is negated.

When the program reads the A2 address of the analog subsystem, the multiplexer's I/O control section decodes the address byte, and when D DIN occurs, produces the HI GATE H and LO GATE H signals causing the module's multiplexer number and channel number to be put on the D-bus. If the A3 address is read, only the GAIN H and HI GATE L signals are produced. This puts the multiplexer gain code on the D-bus in bit positions 4-7. At the same time, the A014 module supplies its status register contents in bit positions 0-3.

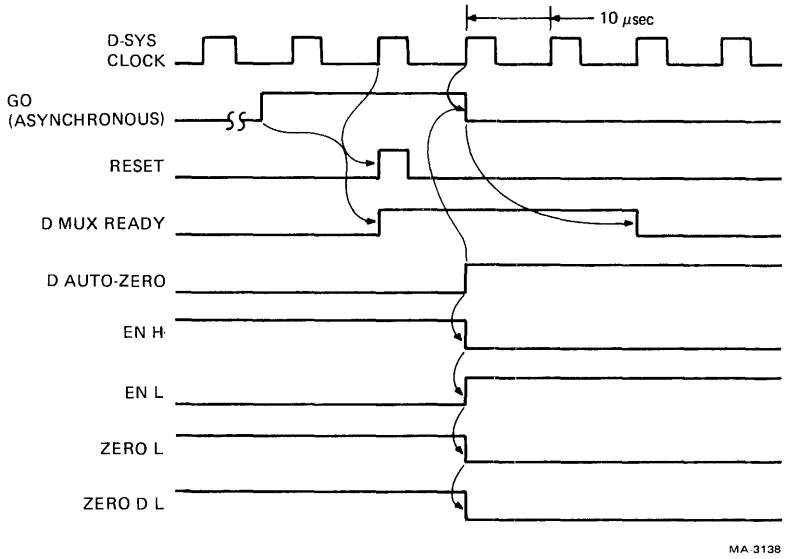


Figure 6-20-3 Auto-Zero Timing

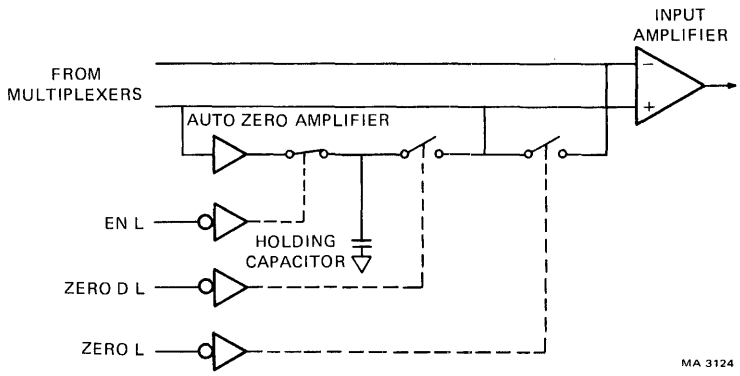


Figure 6-20-4 Auto-Zero Circuit

Reading either the A2 or A3 byte with the GBIT asserted, causes the selected A157 module to place its generic code on the D-bus. If either DBIT or TBIT is asserted, the module is placed in the auto-zero mode.

When the A014 module asserts the D MUX REL signal, the A157 resets its SEL and GO flip-flops, and clears its gain register.

Multiplexer Number and ATR16 Power Selection

The multiplexer number is selected on the module by the 4-pole switch, E3Ø (Figure 6-2Ø-5). An example of one possible multiplexer number selection is shown in Figure 6-2Ø-6 to illustrate the use of this switch. Only three of the switches select the multiplexer number; the fourth switch selects the ATR16 power option. (The ATR16 is an isothermal screw terminal assembly.) When the ATR16 is being used, switch 4 of E3Ø must be on; when the BC40A screw terminal assembly or a user-provided termination is being used, this switch must be off.

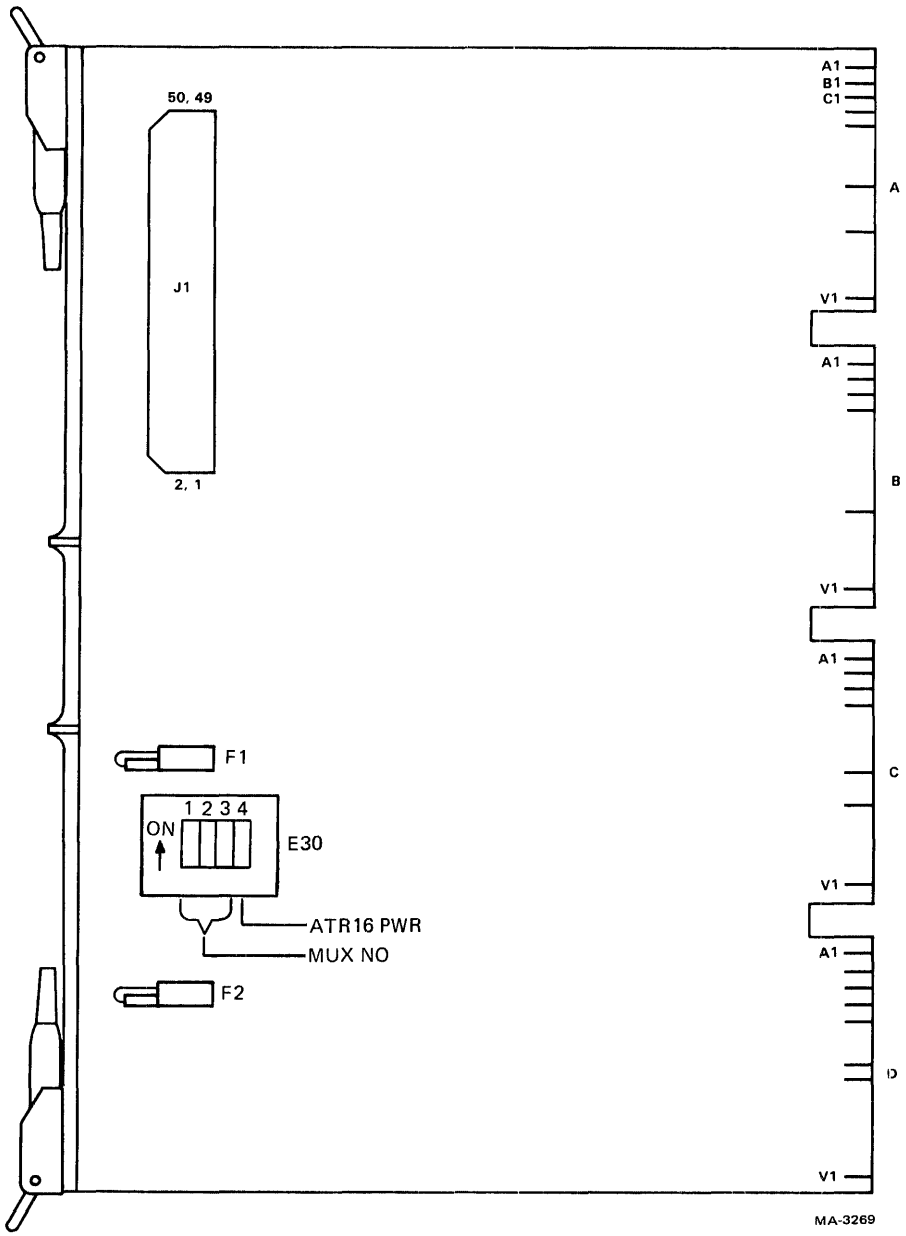


Figure 6-2Ø-5 Wide-Range Analog Multiplexer

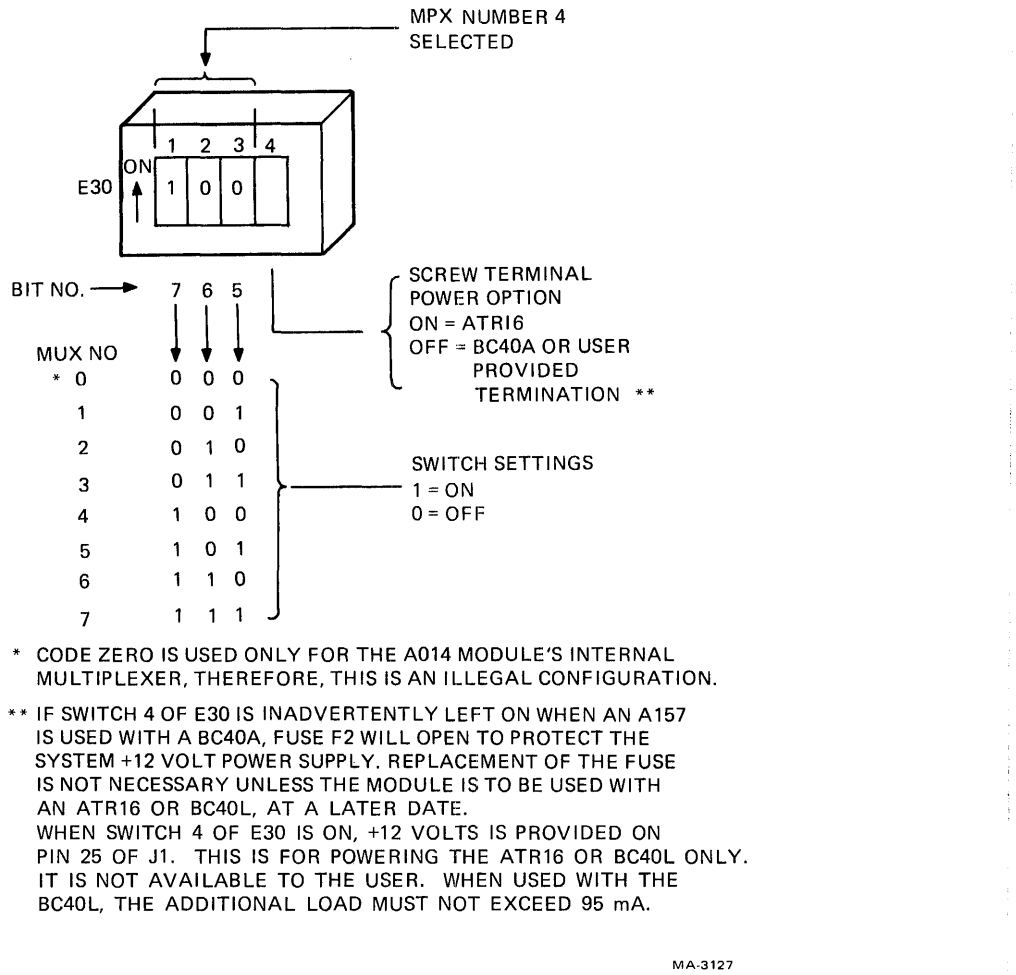


Figure 6-20-6 Multiplexer and ATR16 Power Select

Software Restrictions

1. The A157 registers must not be written during a conversion; this causes erroneous results.

2. The multiplexers are released at the end of a conversion; therefore, the multiplexer number, channel number, and gain registers contain invalid data after this time and must be reprogrammed before another conversion is started.

Generic Code

The generic code of the A157 module is octal 323.

Pin Connections

The A157 module pin connections for J1, the I/O cable connector are shown in Table 6-20-2.

APPLICATION INFORMATION

The reader should refer to Chapter 3, Paragraph 3.8.5 for general field interface information. The reader should also review the material under the heading Analog Field Wiring Practices contained in the section Analog Input Subsystems - General.

NOTE

A finite nonzero current flows into both inputs of the A157. It is the user's responsibility to provide a common mode return path for this current. For best performance and lowest noise, this return should be provided at the transducer end of the input cable.

Table 6-20-2 Module A157 I/O Pin Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1	ØØ +	2	ØØ -
3	Ø1 +	4	Ø1 -
5	Ø2 +	6	Ø2 -
7	Ø3 +	8	Ø3 -
9	Ø4 +	1Ø	Ø4 -
11	Ø5 +	12	Ø5 -
13	Ø6 +	14	Ø6 -
15	Ø7 +	16	Ø7 -
17		18	
19	Common	2Ø	
21		22	
23		24	
25	+12 V*	26	Common
27		28	
29	Common	3Ø	
31		32	
33		34	
35	1Ø +	36	1Ø -
37	11 +	38	11 -
39	12 +	4Ø	12 -
41	13 +	42	13 -
43	14 +	44	14 -
45	15 +	46	15 -
47	16 +	48	16 -
49	17 +	5Ø	17 -

*For ATR16 only

The A157 uses the BC40-A screw terminal assembly as configured in Table 6-20-3.

Table 6-20-3 BC40A Screw Terminal Configuration for the A157 Analog Multiplexer

A157	
Field Bit Number	**Screw Terminal Number**
00 +	1
−	2
01 +	3
−	4
02 +	5
−	6
03 +	7
−	8
04 +	9
−	10
05 +	11
−	12
06 +	13
−	14
07 +	15
−	16
Common	17
Common	18
10 +	19
−	20
11 +	21
−	22
12 +	23
−	24
13 +	25
−	26
14 +	27
−	28
15 +	29
−	30
16 +	31
−	32
17 +	33
−	34

SPECIFICATIONS

All specifications refer to the A157 when used in combination with the A014 A/D converter.

Power Requirements

Voltage	Main supply: VS = 12 Vdc (+2 or -1) Vdc; backup supply: 14 Vdc $\geq$ VB $\geq$ (VS-0.7) Vdc
Operating current (A157 only)	255 mA maximum

NOTE

If the backup supply is implemented, total operating current is shared.
Main supply: 250 mA maximum
Backup supply: 5 mA maximum

Standby current (backup supply) (A157 only)	3 mA maximum

Input Characteristics

Input impedance	Power on: >50 megohms Power off: 1000 ohms

Signal plus common mode voltage capability

Gain	Voltage Range (Volts)	Maximum Signal+CMV (Volts)	LSB (mV)
1	±10.24	±12	5
2	± 5.12	±12	2.5
10	± 1.024	±12	0.5
20	± 0.512	±12	0.25
50	± 0.2048	± 7	0.1
100	± 0.1024	± 9.5	0.05
200	± 0.0512	±10.75	0.025
1000	± 0.01024	±11.75	0.005

Gain	1, 2, 10, 20, 50, 100, 200, or 1000 programmable
Accuracy	±[2 +(0.008 X gain)] LSBs at 25 degrees C ±[4 +(0.008 X gain)] LSBs from 0 degrees C to 60 degrees C ambient, maximum

NOTE

This includes gain and offset errors which can be adjusted to zero.

Channel to channel offset	20 microvolts

Common mode rejection	85 dB minimum (DC to 60 Hz with 1K source unbalance)
Conversion speed	79 microsecond average 74 microsecond minimum 84 microsecond maximum

NOTES

1. There is a ten microsecond uncertainty due to the asynchronous relationship between start of a conversion and the system clock.
2. Conversion speed and accuracy specifications are independent of the order of channel selection.

Bandwidth	No limitation beyond conversion speed
Protection	The input circuits are protected from field overvoltages by diodes to ±13 V and by fusible resistors in series with each input. There are two one Amp fuses. One protects the circuit board etch in the event of charge pump circuit failure. The other protects the ATR16 power supply (see text).

Physical Characteristics

Dimensions	Quad module, triple width, 8-1/2 inch length
Field connector	Cable type BC40A, customer-supplied 50 pin Berg, or ATR16

Environmental Characteristics	Complies with DEC STD 102 Class C Operates in convection cooled environment up to 60 degrees C ambient
Heat dissipation	14 Btu/hr maximum

NCTIONAL DESCRIPTION
e A020 is an isolated, 14-bit plus sign, selectable gain, analog to gital converter. It is used to acquire analog field signals for I/O bsystems where a high degree of isolation from common mode voltages st be maintained. A built-in, program-controlled, mercury-relay ltiplexer selects one of a possible 16 two-wire or 8 three-wire alog field inputs. Provision is made for reading the generic code d for disabling all field inputs. Additional features include ries fusible resistors to protect the module's input circuitry and itches for address and range selection.

WARNING

The A020 module uses mercury-wetted relays. Although these components have metal cases, they contain glass capsules containing mercury and a gas under high pressure. Consequently, these modules are not as resistant to mechanical abuse as might otherwise be expected. The modules should NOT be subjected to unnecessary shock.

MERCURY IS A TOXIC SUBSTANCE. If a module is advertently dropped, or otherwise mistreated, it should be examined carefully to determine if any of the relay capsules have broken. If ANY evidence of mercury is detected on the outside of a relay case (this usually appears as a dull film on the relay, usually at the seam between the base and the metal case), the module should be set aside. Repairs should only be effected by technicians familiar with the precautions necessary for handling mercury.

GENERAL DESCRIPTION
The A020 contains an input multiplexer, an A/D converter, and a D-bus data interface (Figure 6-21-1). The input multiplexer and A/D converter are isolated from the rest of the module and operate at field potential. This allows direct connections to high common mode field inputs. Isolation from any input to ground is ±500 volts peak, as is the isolation between any two inputs.

The module has switches that allow the user to select among fourteen available ranges to accommodate different signal levels. Two of these ranges can be selected on a given module (i.e., some channels can utilize one of the fourteen ranges and the remaining channels another).

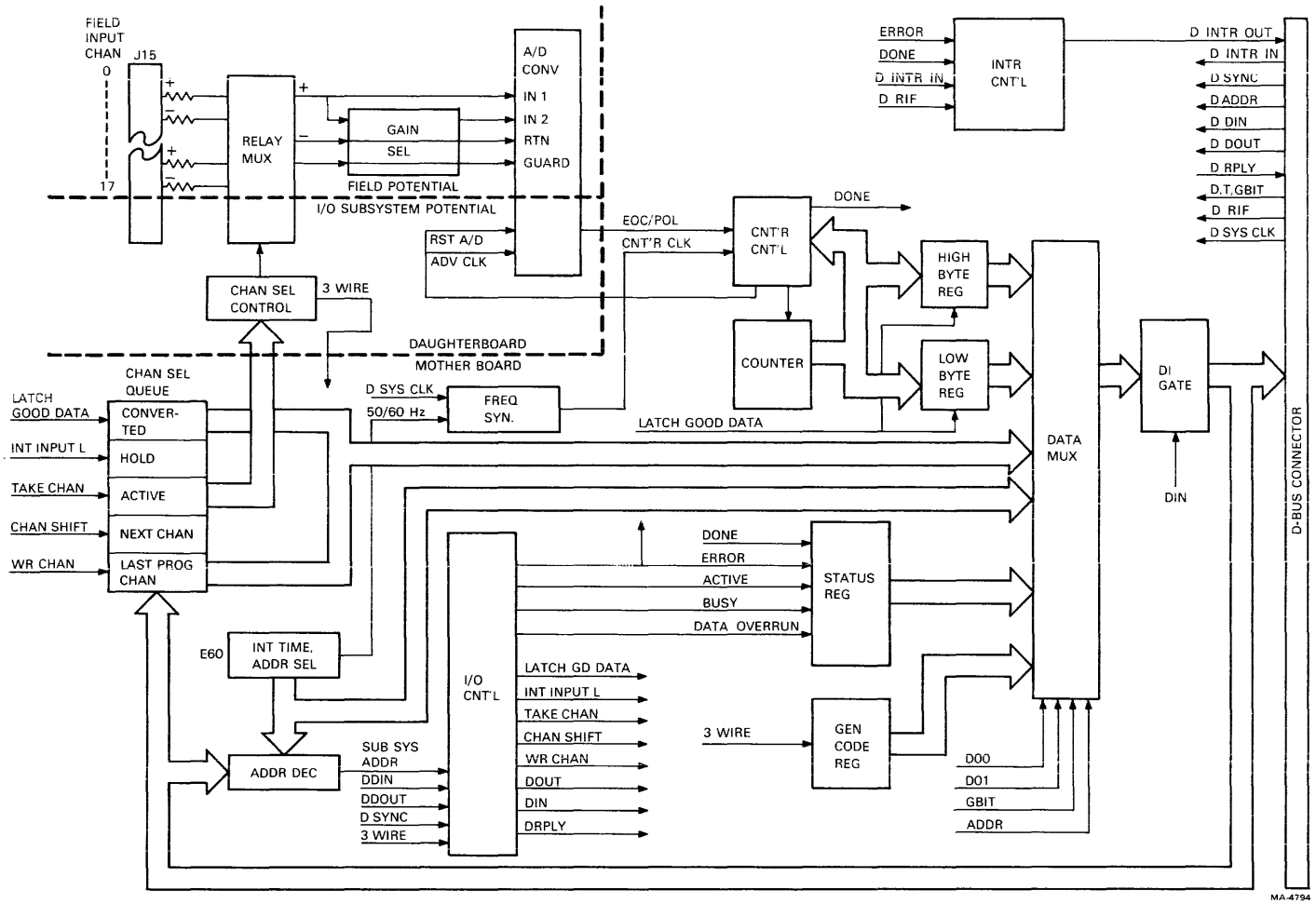


Figure 6-21-1 A020 Block Diagram

Two of the module's data registers contain the A/D converter's output which is 14 magnitude bits plus a sign bit and an overrange bit. Other data registers contain status, address, and generic code data.

DETAILED DESCRIPTION

The module consists of two printed circuit boards assembled in a mother-daughter configuration (Figure 6-21-2). The heavy dashed line in Figure 6-21-1 shows how the module's circuits are divided between the two boards. The daughter board (54-13442) contains the input multiplexer and the analog part of the A/D converter. The mother board (54-13729) contains the data registers, interrupt control circuits, multiplexer control circuits, the remainder of the A/D converter circuits, and the D-bus interface.

Since the A/D converter circuits are divided between the two circuit boards, it is necessary to have a few interconnecting control lines (Figure 6-21-1). Detailed descriptions of the two boards is simplified if the reader is first familiarized with the following discussion of the conversion process utilized.

A/D Conversion Process

The A/D converter on this module is a dual-slope integrating type. A typical converter of this kind contains an integrator, a comparator, a clock, and some control circuitry (Figure 6-21-3) and operates as follows.

At the beginning of a conversion cycle, the switch is in the Vin position. It remains in this position until the counter counts a predetermined number of clock pulses (a fixed interval of time, Tref - Figure 6-21-4). At the end of this time, the integrator output voltage has a value that is proportional to the average value of the input over the interval. That is

$$Vo = \frac{Vin}{RC} \ Tref$$

where:

Vo = the integrator output voltage
Vin = the input voltage
Tref = the sampling period
RC = the circuit time constant

The switch is now connected to the Vref position and simultaneously the counter is reset to zero. The integrator output now starts to decrease because Vref has a polarity opposite to that of Vin. At the same time, the counter starts counting again from zero. Since Vref is a constant, the integrator output always decreases with the same slope no matter what value it has at the time Tref. When the output of the integrator again reaches zero, the comparator output changes state and the counter is stopped. Since the charge gained by the integrator in time Tref is equal to the charge lost in time t, it follows that -

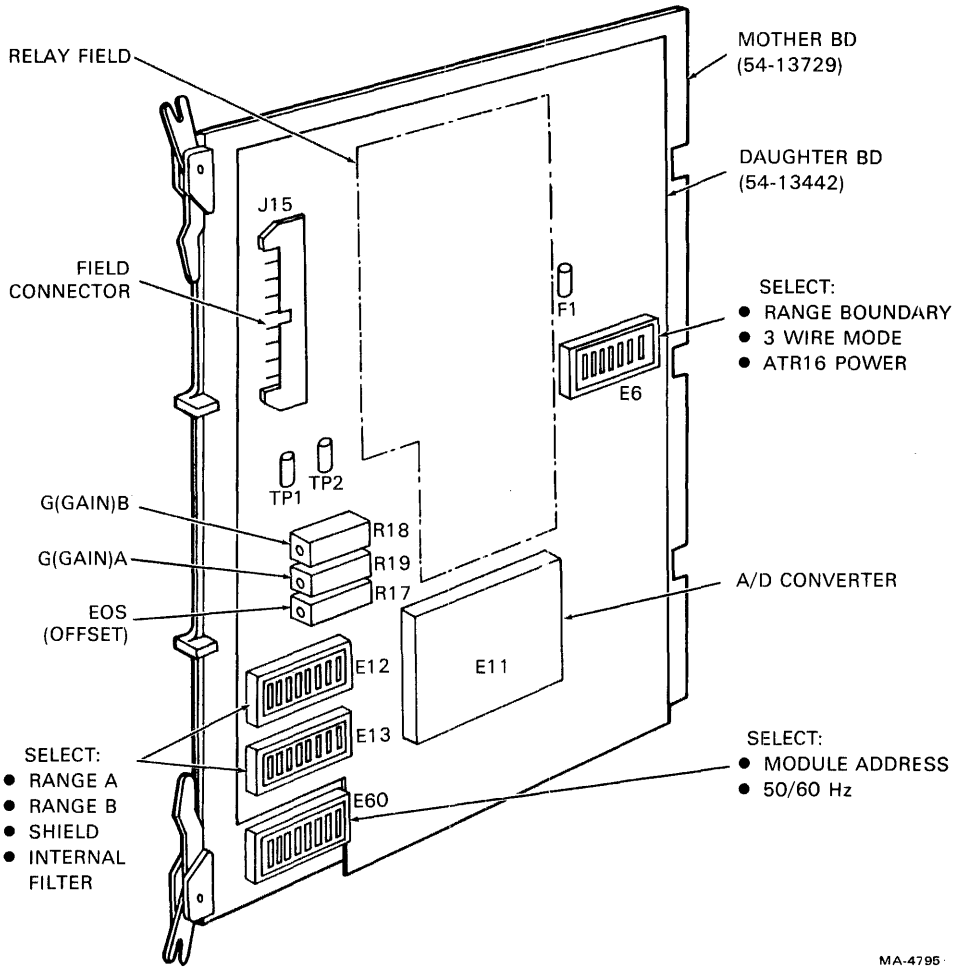


Figure 6-21-2 AØ2Ø A/D Converter Module

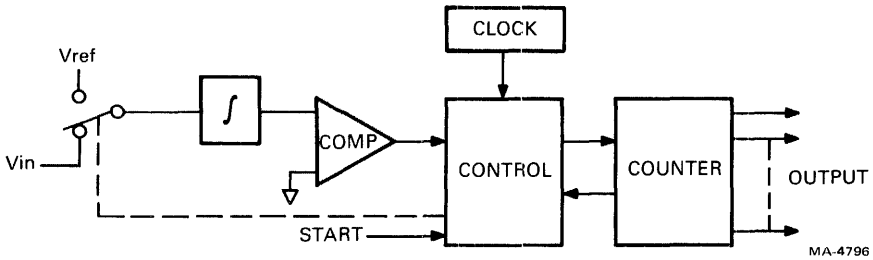


Figure 6-21-3 Simplified Dual Slope Converter

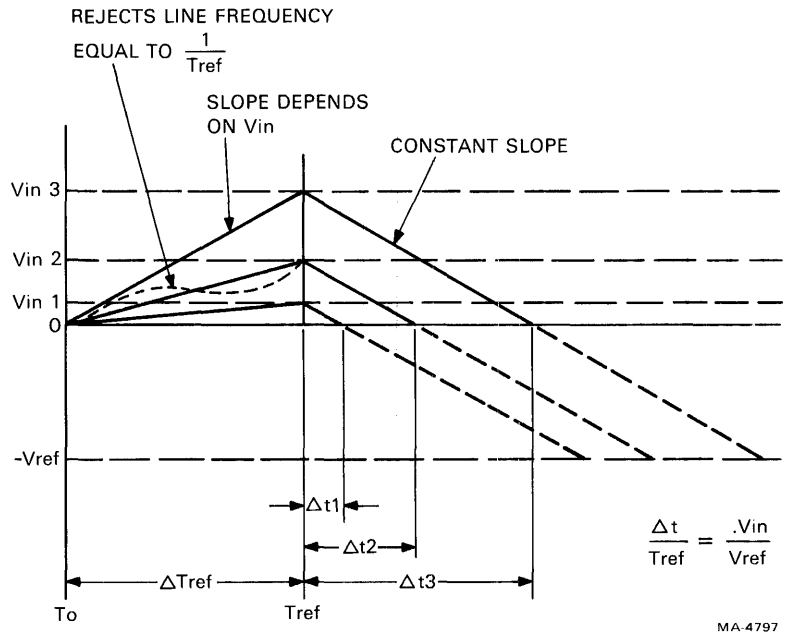


Figure 6-21-4 Dual Slope Converter Time Voltage Relationships

$$\frac{Vin}{RC} Tref = \frac{Vref}{RC}\Delta t$$

The circuit time constant is the same in each case, so -

$$Vin\ Tref = Vref\ \Delta t$$

$$\frac{Vin}{Vref} = \frac{\Delta t}{Tref} = \frac{\Delta count}{full\ count}$$

Therefore, the number in the counter is a binary representation of the input voltage.

The dual-slope integrating type of converter was chosen for the AØ2Ø because it exhibits excellent accuracy, linearity, and resolution characteristics, and is ideal for instrumentation applications. Further, integration inherently provides high frequency noise immunity and virtually total rejection of signals with periods equal to or multiples of the integration time. This is due to the fact that signals with that period will average out to zero over the sampling period (Figure 6-21-4).

Most converters of this type have an input integration time equal to the period of the power line frequency, since that is usually the most troublesome interfering signal. The AØ2Ø has switches that allow selection of a 16-2/3 ms or a 2Ø ms integration time for rejection of power line frequencies of either 6Ø or 5Ø Hz respectively.

Daughter Board

The AØ2Ø daughter board (54-13442) contains an input multiplexer, the A/D converter analog circuits, and the range selector switches. These are isolated from the rest of the module and operate at field potential. Part of the control circuitry for channel and range selection is also present on the daughter board, and is at I/O subsystem potential. The division of potential is indicated by the heavy dashed line in Figure 6-21-5 and is for the purpose of isolating high common mode field voltages from the rest of the subsystem.

Channel Multiplexer - This is a relay multiplexer and is therefore electrically isolated from the channel select controls, which are at I/O subsystem potential. The multiplexer is configured to select one of the sixteen 2-wire or eight 3-wire field inputs via selector switch E6-5. All multiplexer input lines are protected by fusible resistors.

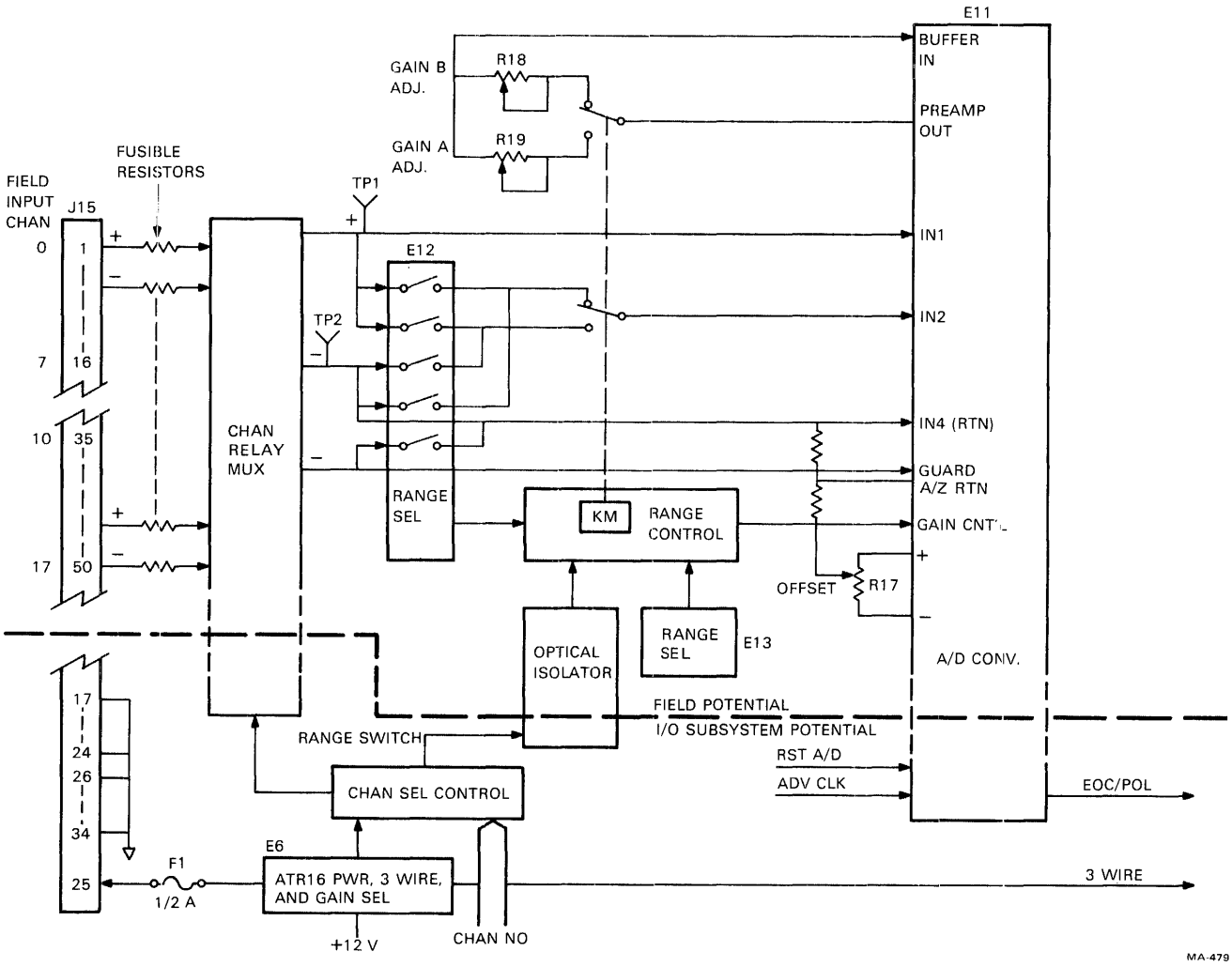


Figure 6-21-5 AØ2Ø Daughter Board

A/D Converter Analog Circuits - This is a sealed unit which is isolated from the I/O subsystem ground potential and operates at whatever field common mode potentials are present (up to 500 V peak). A block diagram of the unit is shown in Figure 6-21-6. Selected channel inputs from the multiplexer are adjusted by the

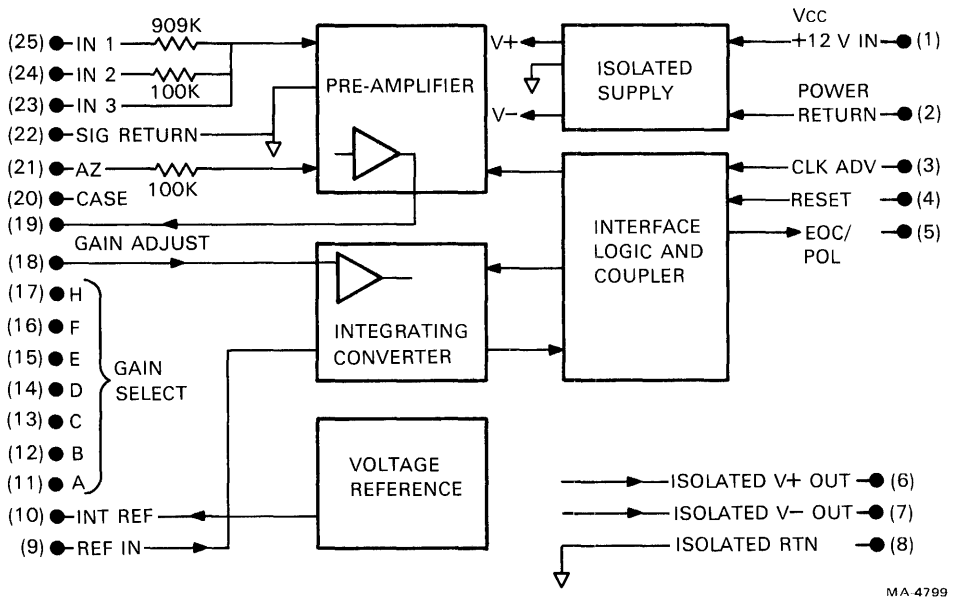


Figure 6-21-6 Isolated, Selectable Range Integrating Converter

input attenuator and/or preamplifier shown so that the input to the integrator is within a ±2.5 V full-scale range. Attenuation and preamplifier gain are selected by external switch settings. When input and reference integrations are completed, internal control circuits output POL/EOC (polarity/end of conversion) pulses through isolation transformers to external control circuits. Timing is controlled by isolated CLK ADV (clock advance) and RESET inputs as discussed in a later paragraph.

The analog section also contains its own power supplies which are powered by but isolated from the module's +12 V power.

Mother Board

The data registers and their control circuits on the mother board resemble those of other four address D-bus modules (Figure 6-21-1). Also shown are the channel select queue, a frequency synthesizer, and the counter circuit. These are discussed below.

Channel Select Queue - Throughput of the A020 is optimized by having the module keep track of not only the channel actively being converted, but also the channel that is to be converted next, and the one most recently converted. This is accomplished by a set of five registers that store this information (Figure 6-21-1).

Although there are five registers in the channel select queue, there are never more than four channel numbers stored at any given time. This is because the HOLD and CONVERTED registers contain the same number during input integration, and the LAST and NEXT registers contain the same number during reference integration. The following is a description of the contents of the five registers.

1. Last Program Channel Register - A read/write register that contains the last channel number written to the module.

2. Next Channel Register - An internal register that contains the channel number of the input signal to be integrated next.

3. Active Register - An internal register that contains the channel number of the input signal being integrated.

4. Hold Register - An internal register that holds the channel number of the signal just integrated until it is evaluated and the results transferred to the data register.

5. Converted Channel Register - A read-only register that contains the number of the channel for which conversion is complete and data is available.

Integration Timing Circuit - To ensure maximum rejection of interference at power line frequencies of either 60 or 50 Hz, input integration times of 16-2/3 and 20 ms are implemented on the A020. Integration time is determined by decoding the output of the counter and is changed by selecting a different decoder output and counter clock frequency. To obtain accuracy and stability, clock frequencies are phase locked to the I/O Subsystem's crystal-controlled 100 kHz system clock.

The A020 is shipped with the 16-2/3 ms integration time selected (for 60 Hz rejection). If site conditions require a 20 ms integration time (for 50 Hz rejection), the user may select that option; however, he must also recalibrate the A/D converter.

Counter and Timing Circuit - The counter on the A020 module provides the timing for the A/D converter cycle as well as the data output of the A/D converter. A conversion cycle (Figure 6-21-7) begins with the RST A/D (reset A/D) pulse. After a delay of 2 ms the counter is reset, and an A/D CLK ADV (A/D clock advance) pulse occurs. This begins the input integration period of the A/D, and starts the counter again.

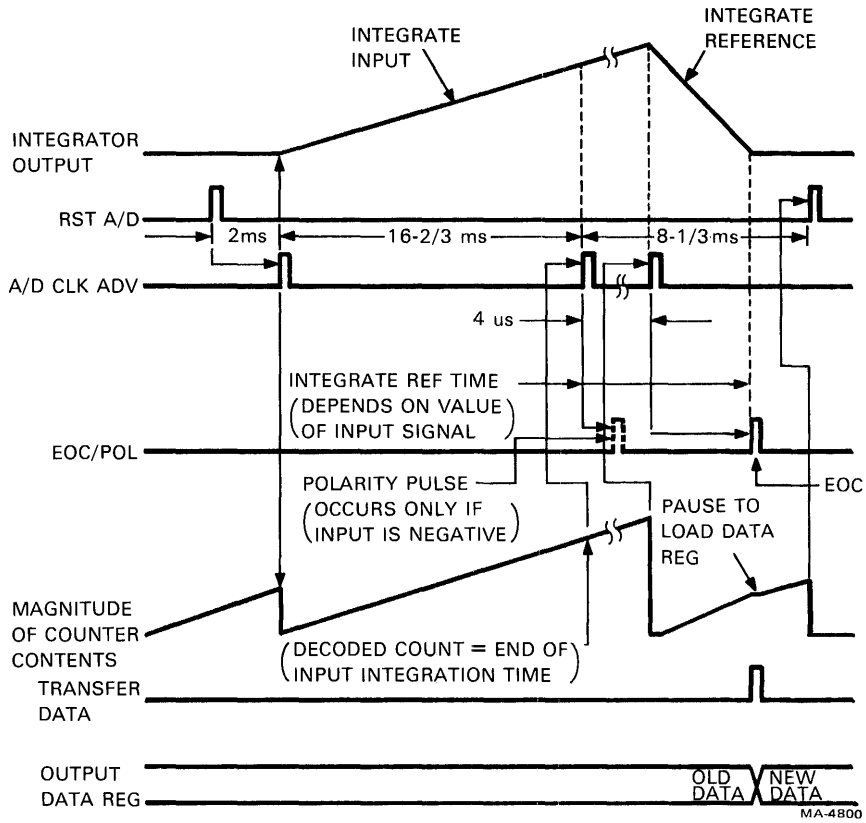


Figure 6-21-7 Conversion Cycle Timing (60 Hz Timing Shown)

The counter counts a number of clock pulses corresponding to the desired integration time (16-2/3 or 20 ms, for 60 or 50 Hz respectively). When this count is reached, a second A/D CLK ADV pulse is produced. At this time, a POL (polarity) pulse will occur if the input is negative. Four microseconds after the second A/D CLK ADV pulse, the counter is again reset. This produces a third A/D CLK ADV pulse. At this time, integrate input time ends, the counter restarts, and integrate reference time begins.

Integrate reference time continues until the A/D comparator input reaches zero. The comparator output will then change state causing the A/D to output the EOC (end of conversion) pulse. At this time, the counter is halted; its contents, which is a binary representation of the analog input signal, is transferred to the data register, and the counter resumes counting. When the counter reaches full scale, corresponding to an elapsed time of 8-1/3 or 10 ms (60 or 50 Hz), another RST A/D pulse occurs, denoting the start of a new conversion cycle.

Of the sixteen data register bits, fourteen bits (0-13) represent normal range data; a fifteenth (bit 15) is set if the input signal is in excess of the A/D converter's range as determined by the selected gain. A sixteenth (bit 14) is set if the POL (polarity) pulse occurs, indicating a negative input signal.

SOFTWARE INTERFACE

The A020 occupies four byte addresses on the D-bus. The data sent from the A020 to the computer can be one of six bytes determined by the two LSBs of the address, the GBIT signal, and the ADDR signal as listed in Table 6-21-1.

Table 6-21-1 Data Registers

7 ... Ø	Bit 1	Bit Ø	G Bit	ADDR
7 MAGNITUDE DATA Ø	Ø	Ø	Ø	Ø
Over-Range | Sign | 13 MAGNITUDE DATA 8	Ø	1	Ø	Ø
CONVERTED DATA CHANNEL | LAST PROGRAM CHANNEL	1	Ø	Ø	Ø
Busy | Ø | Ø | Ø | Data Over-Run | Error | Done | Active	1	1	Ø	Ø
G CODE	X	X	1	Ø
ADDRESS | Ø | Ø	X	X	X	1

X = don't care

Data Definitions

Output Data Coding - Sign + Magnitude - Sign bit is asserted for negative data. Magnitude is true binary.

Overrange Bit - Asserted when input is greater than Full Scale Range selected for that channel. Output data is therefore invalid.

Busy - When asserted, indicates channel queue is full and module cannot accept any new channels.

Done - Asserted when a conversion has been completed and data is available.*

Error - Asserted when there has been an attempt to program a new channel into a busy device, or an invalid channel (>17 octal for 2-wire mode, >7 for 3-wire mode) has been programmed. The A020 will not accept the new channel under these conditions.*

Data Overrun - Indicates previous data was not retrieved by the processor before new data was available. The new data is lost, as are all channel convert commands subsequent to the converted data channel.*

Active - Asserted whenever a channel is written. Negated one conversion cycle after channel queue is empty.

PROGRAMMING INFORMATION

To read one of the AØ2Ø analog inputs, write its channel number in the last four bits of the third byte. Since inputting a channel implies a desire to convert on that channel, no separate GO bit is provided. When the AØ2Ø interrupts, read its data registers.

If the AØ2Ø is operated in the mode of converting one channel at a time, each conversion may take up to 74 ms. Operation at maximum speed requires a continuous conversion and channel switching cycle. To accomplish this, the AØ2Ø can store up to four channels: two channels waiting to be converted, one that is actively being converted, and one representing the converted channel for which data is available in the data registers. To use the AØ2Ø most efficiently, first program two channels and wait for an interrupt. When the module interrupts, read the data registers and program two more channels. Subsequently, one new channel should be programmed after each interrupt and data read cycle. This sequence may be implemented by simply loading in channels at all times until the busy bit comes up. This mode allows up to 36 conversions per second with 6Ø Hz operation. Up to 31 conversion per second are possible with 5Ø Hz operation.

Assertion of the D-bit opens all input relays, allowing a test voltage to be applied via TP1 and TP2 without disconnecting field inputs. The T-bit is not used on the AØ2Ø.

The processor will trap if an attempt is made to write any other byte than the third.

Generic Code

The AØ2Ø may have one of two generic codes depending on the position of the MODE switch (E6-5). The location of the MODE switch is shown in Figure 6-21-9.

The codes are as follows.

324 for the 2-wire mode (switch OFF)
3Ø4 for the 3-wire mode (switch ON)

---

* Reset by RIFing the module. The last step in retrieving data should be to read the status word (fourth byte) with the RIF bit set in the CSR of the IOCM. The contents of the status word tells the program if any condition exists that invalidates the data just read.

FUNCTION SELECTOR SWITCHES

The module's switches are configured by the user to suit the application as follows.

Address Select

The four AØ2Ø addresses are selected on the module according to the rules stated in Chapter 4. They are selected on the module by switches E6Ø-1 through E6Ø-6 shown in Figure 6-21-8. An example of one possible selection is shown in the figure.

5Ø/6Ø Hz Select

Integration time is determined by switches E6Ø-7 and E6Ø-8 or by E6Ø-9 and E6Ø-1Ø (Figure 6-21-8). Only two of these switches may be on at any given time. If 6Ø Hz line frequency rejection is desired, turn on switches E6Ø-7 and E6Ø-8. If 5Ø Hz rejection is desired, turn on E6Ø-9 and E6Ø-1Ø.

ATR16 Power Select

Switch E6-1Ø (Figure 6-21-8), when on, selects the ATR16 power option. (The ATR16 is an isothermal screw terminal assembly.)

Mode Select

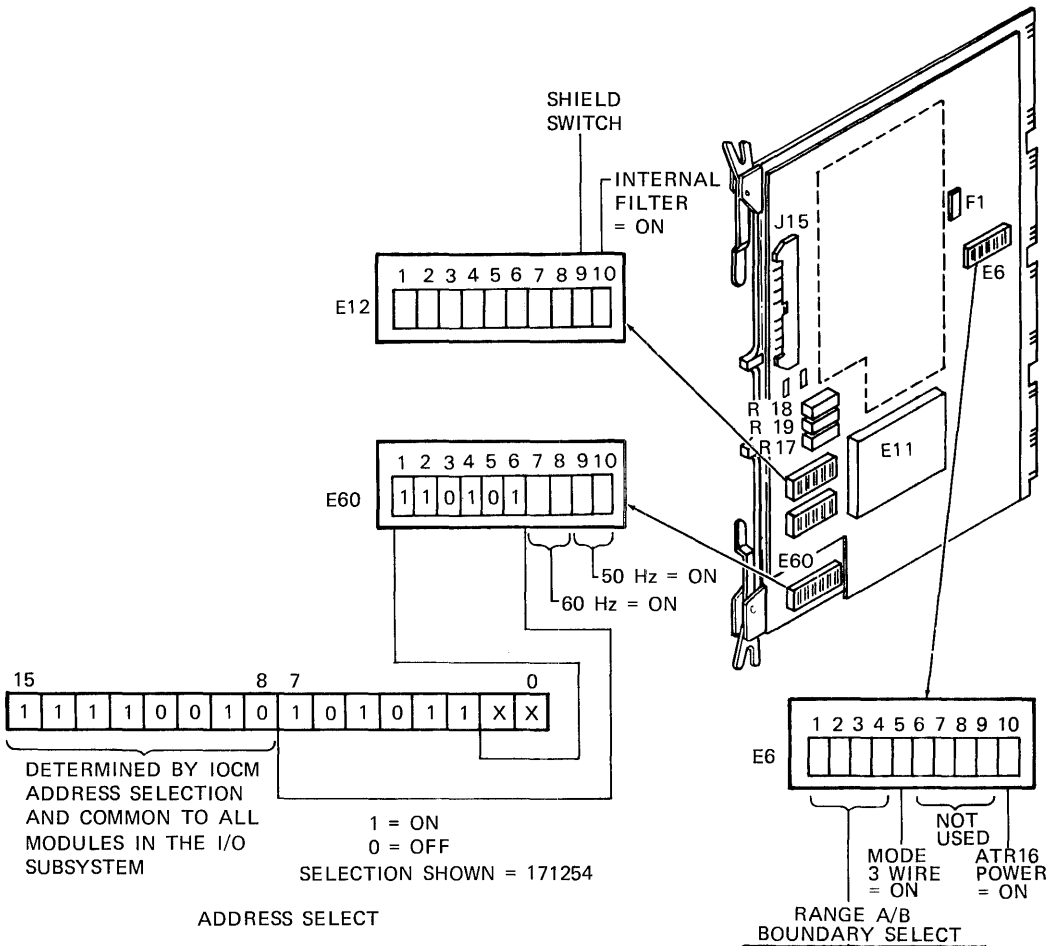
When switch E6-5 (Figure 6-21-8) is off, the AØ2Ø is set for sixteen channel 2-wire operation. When E6-5 is on, the AØ2Ø is set for eight channel 3-wire operation. In this mode, the upper eight channels are switched in parallel with the lower eight channels; that is, addressing channel Ø simultaneously switches channel 1Ø, channel 1 and channel 11 switch together, etc. The negative terminal of channels 1Ø through 17 are used as third wire (shield) inputs; the positive terminal of these channels should be left open. The shield input switches somewhat earlier than the two signal inputs and therefore switches all the common mode potential. This feature is useful when the three-wire mode is used with input filters so that commmon-mode switching transients through the filter capacitors are reduced.

Shield Switch

When E12-9 (Figure 6-21-8) is on, the high voltage shield is connected to the low side input of the A/D converter. This switch should always be ON when the AØ2Ø is in two-wire mode. In three-wire mode, the switch should generally be off when using shielded inputs, but on when using input filters. (Refer to application notes.)

Internal Filter Switch

When E12-1Ø (Figure 6-21-8) is on, a capacitor is connected across the inputs of the A/D converter. This capacitor provides high frequency filtering and is also used to implement open thermocouple detection. (Refer to applications information below.) This switch should be on at all times except if external filters are used, when it should generally be off to avoid errors due to charge dumping (appearing as interchannel crosstalk).



NOTE:

IF SWITCH 10 OF E6 IS INADVERTENTLY LEFT ON WHEN AN A020 IS USED WITH A BC40A, FUSE F1 WILL OPEN TO PROTECT THE SYSTEM +12 VOLT POWER SUPPLY REPLACEMENT OF THE FUSE IS NOT NECESSARY UNLESS THE MODULE IS TO BE USED WITH AN ATR16 OR BC40L AT A LATER DATE.
WHEN SWITCH 10 OF E6 IS ON, +12 VOLTS IS PROVIDED ON PIN 25 OF J1. THIS IS FOR POWERING THE ATR16 OR BC40L ONLY. IT IS NOT AVAILABLE TO THE USER. WHEN USED WITH THE BC40L, THE ADDITIONAL LOAD MUST NOT EXCEED 145 mA.

FIRST GAIN B CHAN NO.	SWITCH # SETTINGS 1	2	3	4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
10	0	0	0	1
11	1	0	0	1
12	0	1	0	1
13	1	1	0	1
14	0	0	1	1
15	1	0	1	1
16	0	1	1	1
17	1	1	1	1

MA-5248

Figure 6-21-8 AØ2Ø Module Switch Functions

Range Select Switches

The AØ2Ø has fourteen full scale input ranges. The user can select a single range for all channels or he may select two ranges and have one set of consecutive channels operate on one (range A) and the remainder on the second (range B).

There are switches to select the two ranges (Figures 6-21-9 and 6-21-1Ø), and to select the point at which the range changes from A to B (Figure 6-21-8). Because of the way attenuation and gain combinations are used to implement the different ranges, some ranges can be selected in more than one way. The recommended switch settings are shown in Figures 6-21-9 and 6-21-1Ø. Channels zero through seven are calibrated at the factory on the ±5 V range (range A). Channels ten through seventeen (octal) are calibrated on the ±5Ø mV range (range B). If the user selects other ranges, he must recalibrate the AØ2Ø. However, the user may change the range transition point without recalibrating.

To use a single range for all channels, do the following.

1. Select the desired range with the switches for range B using switches E12-1 through E12-6 and E13-8 through E13-1Ø (Figure 6-21-1Ø).

2. Set the range A/B boundary at channel zero by turning switches E6-1 through E6-4 off (Figure 6-21-8).

To use two ranges, do the following.

1. Select range A using switches E12-7 and E12-8, and E13-1 through E13-7 (Figure 6-21-9).

2. Select range B with switches E12-1 through E12-6, and E13-8 through E13-1Ø (Figure 6-21-1Ø).

3. Set the range A/B boundary to the lowest numbered range B channel number (Figure 6-21-8). All channel numbers less than the boundary number will be range A; all channel numbers equal to or greater than the boundary number will be range B.

Calibration

The AØ2Ø is calibrated at the factory for the ±5 V range on the lower channels (gain range A), and the ±5Ø mV range on the upper channels (gain range B). These were chosen both as representative high and low level ranges for intensive testing at the factory and as reasonable full scale range selections for a wide range of applications. If other ranges are desired they must be reselected and recalibrated. Calibration is done with software assistance. The calibration procedure is included with the diagnostic software package. The adjustments mentioned in the diagnostic (gain and offset) are identified in Figure 6-21-2. A Precision Voltage Source, EDC model VS-11N or equivalent, will be required.

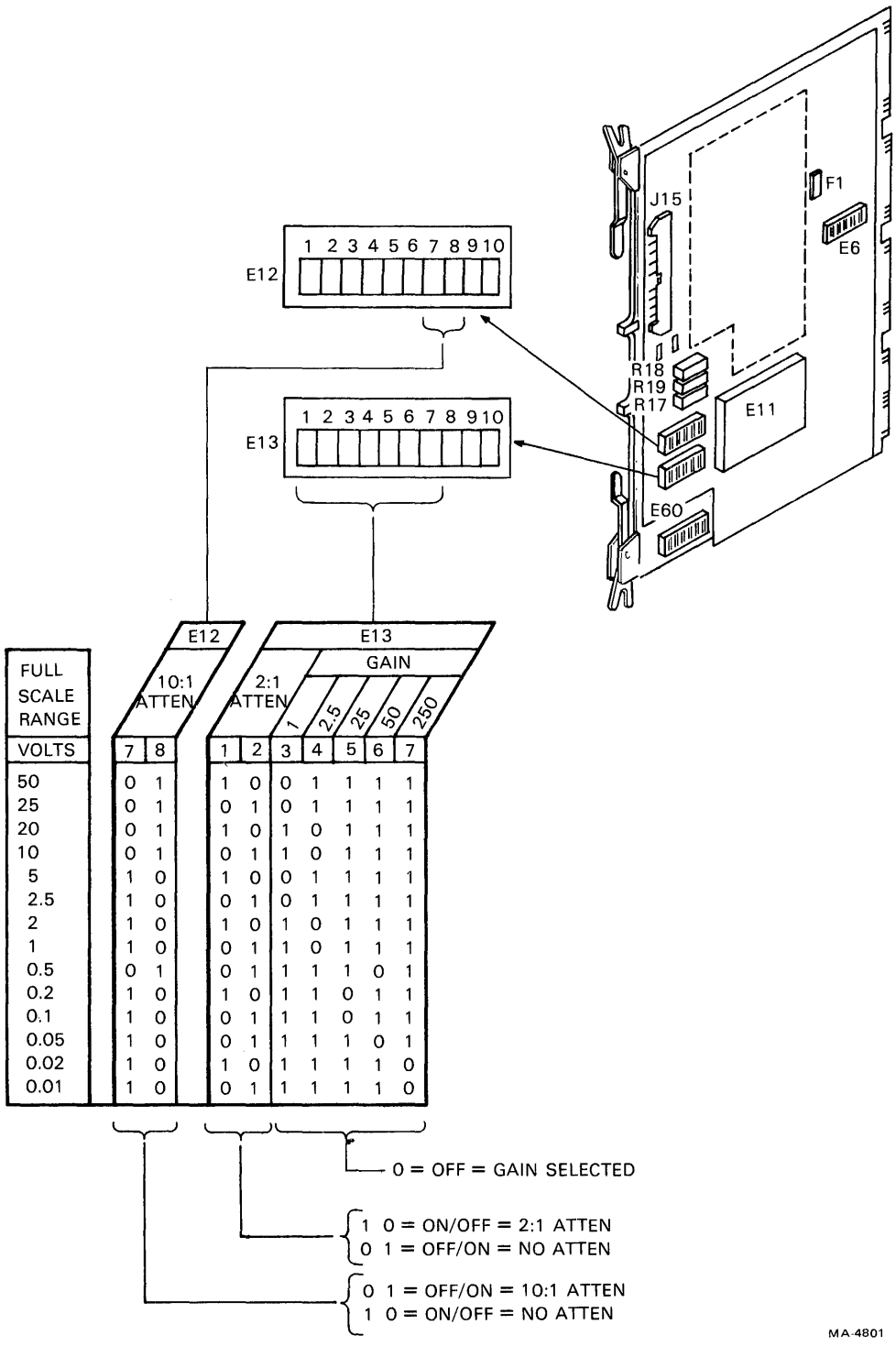


Figure 6-21-9 Full Scale Range A Selections

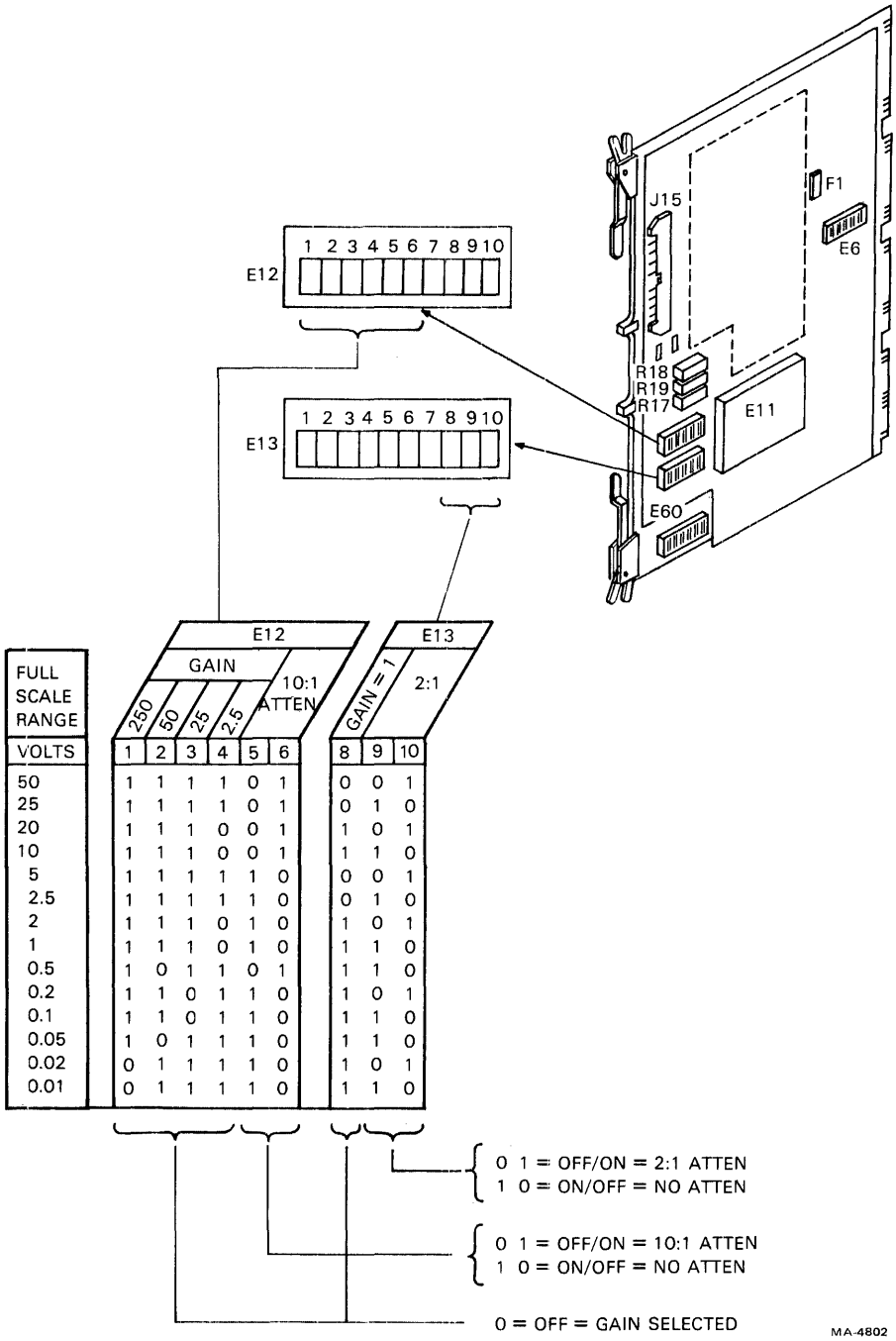


Figure 6-21-1Ø Full Scale Range B Selections

To ensure compliance with specifications, all test equipment used for calibration of the AØ2Ø must have been accurately and recently calibrated. In addition, personnel doing the calibration should be familiar with aligning analog equipment. If you are not sure of the foregoing, DO NOT ATTEMPT TO CALIBRATE THE AØ2Ø. Factory calibration is probably better than that which you will be able to accomplish.

The input amplifier is arranged as shown in Figure 6-21-11. Voltage limit constraints are ±5 V maximum at the input to the major gain block; the output of the entire section is scaled to ±2.5 V full scale. Whenever the input divider is used the input impedance drops to 1M ohm.

Possible full scale ranges selectable at the switches therefore include the following: ±5Ø V, ±25 V, ±2Ø V, ±1Ø V, ±5 V, ±2.5 V, ±2 V, ±1 V, ±5ØØ mV, ±2ØØ mV, ±1ØØ mV, ±5Ø mV, ±2Ø mV, and ±1Ø mV. In addition, sufficient range is provided in the gain pots so that all these ranges can be multiplied by 1.Ø24. This has the advantage that it makes the bit weights decimal multiples of the familiar and easily remembered powers of two.

Some examples of input voltages versus output codes are listed in Table 6-21-2 for the 1 volt full-scale range. Table 6-21-3 lists the LSB values for all the ranges.

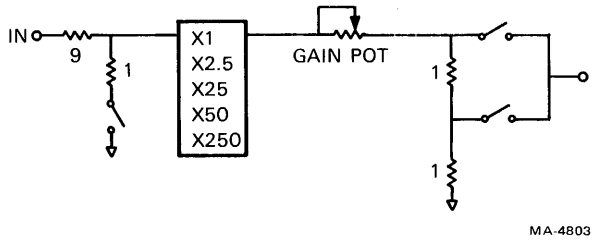


Figure 6-21-11 Analog Input Configuration

FIELD WIRING

Field wiring for the AØ2Ø can be implemented with either the ATR16 or the BC4ØA screw terminal assembly, or with a user designed interface.

Turn to the section on the ATR16 isothermal screw terminal assembly (in this manual) to find field wiring configurations for an AØ2Ø using that interface.

Table 6-21-2 Absolute Magnitude Code

Input Magnitude	Binary Output Code		Input Voltage (Ideal)	
	Sign	Magnitude	Nominal	Range
+FS-1 LSB	Ø	11 111 111 111 111	+Ø.999939 V	>(Ø.999ØØ8) V
+FS-2 LSB	Ø	11 111 111 111 110	+Ø.999878 V	+(Ø.999847, Ø.999ØØ8) V
.		.	.	.
.		.	.	.
.		.	.	.
+FS/2	Ø	1Ø ØØØ ØØØ ØØØ ØØØ	+Ø.5ØØØØØ V	+(Ø.499969, Ø.5ØØØ31) V
.		.	.	.
.		.	.	.
.		.	.	.
+2 LSB	Ø	ØØ ØØØ ØØØ ØØØ Ø1Ø	+122 uV	+(92, 153) uV
+1 LSB	Ø	ØØ ØØØ ØØØ ØØØ ØØ1	+61 uV	+(31, 92) uV
Zero	X*	ØØ ØØØ ØØØ ØØØ ØØØ	Ø	(-31, +31) uV
-1 LSB	1	ØØ ØØØ ØØØ ØØØ ØØ1	-61 uV	-(31, 92) uV
-2 LSB	1	ØØ ØØØ ØØØ ØØØ Ø1Ø	-122 uV	-(92, 153) uV
.		.	.	.
.		.	.	.
.		.	.	.
-FS/2	1	1Ø ØØØ ØØØ ØØØ ØØØ	-Ø.5ØØØØØ V	-(Ø.499969, Ø.5ØØØ31) V
.		.	.	.
.		.	.	.
.		.	.	.
-FS+2 LSB	1	11 111 111 111 110	-Ø.999878 V	-(Ø.999847, Ø.999ØØ8) V
-FS+1 LSB	1	11 111 111 111 111	-Ø.999939 V	<(Ø.999ØØ8) V

* X = Don't care

Table 6-21-3 Least Significant Bit Values

Whole Number Ranges		Ranges X 1.Ø24	
Full Scale Volts	LSB uV	Full Scale Volts	LSB uV
5Ø	3Ø51.76	51.2Ø	3125
25	1525.88	25.6Ø	1562.5
2Ø	122Ø.7Ø	2Ø.48	125Ø
1Ø	61Ø.35	1Ø.24	625
5	3Ø5.176	5.12	312.5
2.5	152.588	2.56	156.25
2	122.Ø7Ø	2.Ø48	125
1	61.Ø35	1.Ø24	62.5
Ø.5	3Ø.5176	Ø.512	31.25
Ø.2	12.2Ø7Ø	Ø.2Ø48	12.5
Ø.1	6.1Ø35	Ø.1Ø24	6.25
Ø.Ø5	3.Ø5176	Ø.Ø512	3.125
Ø.Ø2	1.22Ø7Ø	Ø.Ø2Ø48	1.25
Ø.Ø1	Ø.61Ø35	Ø.Ø1Ø24	Ø.625

Table 6-21-4 shows the AØ2Ø field wiring configurations to use with the BC4ØA screw terminal assembly.

Table 6-21-5 shows the pin connections for J15, the module's I/O cable connector, for the user who requires a custom AØ2Ø interface.

APPLICATION NOTES
The following discussions are provided to help the user cope with some of the typical problems in applying A/D converters in general, and the AØ2Ø in particular.

Gain, Resolution, and Accuracy
A common error in applying analog input equipment is to confuse resolution with accuracy. The number of bits and ranges is often given inordinate attention as a figure of merit of a data acquisition system, when in fact it is relatively meaningless.

Accuracy errors can be divided into three categories: those that are absolute, those that appear as a percentage of the input, and those that appear as a percentage of the selected full scale range.

Table 6-21-4 Module AØ2Ø Screw Terminal Connections

BC40A Screw Terminal

Field Channel Number				Screw Terminal Number
2-Wire		3-Wire		
Ø	+	Ø	+	1
	-		-	2
1	+	1	+	3
	-		-	4
2	+	2	+	5
	-		-	6
3	+	3	+	7
	-		-	8
4	+	4	+	9
	-		-	1Ø
5	+	5	+	11
	-		-	12
6	+	6	+	13
	-		-	14
7	+	7	+	15
	-		-	16
Common		Common		17
Common		Common		18
1Ø	+			19
	-	Ø Shield		2Ø
11	+			21
	-	1 Shield		22
12	+			23
	-	2 Shield		24
13	+			25
	-	3 Shield		26
14	+			27
	-	4 Shield		28
15	+			29
	-	5 Shield		3Ø
16	+			31
	-	6 Shield		32
17	+			33
	-	7 Shield		34

Table 6-21-5 Module AØ2Ø I/O Pin Connections

Module I/O Connector Pin	Field I/O Channel 2-Wire	Field I/O Channel 3-Wire	Module I/O Connector Pin	Field I/O Channel 2-Wire	Field I/O Channel 3-Wire
1	+ØØ	+ØØ	2	-ØØ	-ØØ
3	+Ø1	+Ø1	4	-Ø1	-Ø1
5	+Ø2	+Ø2	6	-Ø2	-Ø2
7	+Ø3	+Ø3	8	-Ø3	-Ø3
9	+Ø4	+Ø4	1Ø	-Ø4	-Ø4
11	+Ø5	+Ø5	12	-Ø5	-Ø5
13	+Ø6	+Ø6	14	-Ø6	-Ø6
15	+Ø7	+Ø7	16	-Ø7	-Ø7
17, 19 Not Used			18, 2Ø Not Used		
21, 23 Common			22, 24, 26, 28, 3Ø Common		
25 ATR16 Power					
27, 29 Common					
31, 33 Not Used			32, 34 Not Used		
35	+1Ø		36	-1Ø	ØØ Shield
37	+11		38	-11	Ø1 Shield
39	+12		4Ø	-12	Ø2 Shield
41	+13		42	-13	Ø3 Shield
43	+14		44	-14	Ø4 Shield
45	+15		46	-15	Ø5 Shield
47	+16		48	-16	Ø6 Shield
49	+17		5Ø	-17	Ø7 Shield

The category of absolute errors includes offset errors of all kinds, including initial, channel-to-channel, offset temperature drift, and noise. These are independent of gain or resolution. If the AØ2Ø, for example, has a 6 microvolt offset error and is being used on the ±1ØØ mV range where an LSB = 6 microvolts, there will be a one LSB error, while if it is used on the ±1Ø mV range where an LSB = Ø.6 microvolt, the error will simply become 1Ø LSBs. No advantage is gained in regard to these errors by increasing gain (i.e., changing to a lower range).

The second category of errors, those that appear as a percentage of the input, include gain errors, gain temperature coefficients, common mode errors, and crosstalk. If a 1Ø mV input is applied to an AØ2Ø with a Ø.Ø6% gain error set for the ±1ØØ mV scale, a gain error of one LSB will appear at the output; if the full scale range is reduced to ±1Ø mV, the digital output error will simply

become 10 LSBs. Similarly, if a 1000 volt p-p common mode signal is applied to the A020 in an input configuration that produces 160 dB of common mode rejection, the output error will be 10 microvolts no matter how many bits this is made to represent by changing the full scale range.

The final category of errors, those which appear as a percentage of full scale, include differential and integral nonlinearity. For example, differential nonlinearity, which is specified as ±1/2 LSB for the A020, would be 0.3 microvolt on the 10 mV range but 3 microvolts on the 100 mV range. The user must decide if this is significant in his application. Similarly, integral nonlinearity, at ±.01% of FSR, is 2 microvolts on the 10 mV range and 20 microvolts on the 100 mV range. In deciding how significant this error is, the user should take into account the fact that integral nonlinearity matters only if a large portion of the dynamic range is used; if the application involves controlling or monitoring an input around a narrow setpoint, integral nonlinearity errors simply translate into absolute accuracy errors, which can be adjusted out with the gain pots, software corrected, or ignored.

From the above discussion, it should be obvious that referring to total accuracy as a percentage of full scale input is virtually meaningless. A total accuracy figure should not, therefore, be the sole criterion for selecting an operating range. That is, one should not select a lower range in the belief that because the percentage of full scale is a smaller number this will result in a smaller total measurement error. Using a less sensitive higher range, often has no significantly greater error, and often has advantages in increasing dynamic range and reducing noise sensitivity.

This is not to say that the user is not interested in total accuracy, but only that estimation of this error requires a thorough understanding of all error components.

In addition to the above considerations of A/D converter measurement errors, the user must also consider the error of the transducer itself when calculating a total error.

Noise and Software Filtering

Noise, one of those errors that exists in absolute terms regardless of the range selected, is specified for the A020 at 3 microvolts RMS or 1/3 LSB RMS maximum, whichever is greater. This noise is internally generated in the A/D and is in addition to any externally imposed noise. Three-sigma peak noise is three times the RMS value for purely Gaussian noise. This all translates into 15 LSBs (3 uV RMS, X 3 = 9 uV pk ÷ 0.6 = 15) of peak noise on the ±10 mV range, 1.5 LSBs (9 ÷ 6) on the ±100 mV range, and 1 LSB (1/3 LSB x 3) on all less sensitive ranges. For low level signals, therefore, the lower order bits become meaningless if software filtering is not implemented. For high level signals, internal noise errors are comparable to quantization and differential nonlinearity errors. They can probably be ignored for most applications.

Software filtering can range from simple averaging to sophisticated autocorrelation algorithms. A common technique takes ten samples, discards the highest and lowest, and averages the remaining eight. Statistically, of course, the uncertainty of the results diminishes as the square root of the number of samples averaged. Averaging eight samples with a 15 LSB uncertainty, therefore, reduces the uncertainty to about 5 LSBs ($15/\sqrt{8}$); reducing a 15 LSB uncertainty to one LSB requires averaging 225 samples.

It is worthwhile noting that in the presence of noise, averaging can reduce quantization error to less than 1/2 LSB by simply keeping fractions of a bit in the arithmetic result. This means, for example, if eight samples from the AØ2Ø on the ±1ØØ mV range are averaged, the usual 9 microvolts of peak noise is reduced by 1/8 to 1/2 LSB or 3 microvolts, but quantization error is reduced by 1/8 to 1/16 LSB or Ø.375 microvolts. The same 3 microvolt uncertainty results after averaging eight samples from the device set to the ±1Ø mV range, with quantization error reduced to Ø.Ø375 microvolts. Again, increasing gain does not necessarily result in a significant improvement in performance.

High Common Mode Voltage Applications

The internal common mode rejection of the AØ2Ø is typically in excess of 17Ø dB. This is achieved when the common mode signals are applied through low source impedances (on the order of 1Ø ohms). Whenever higher source impedances are involved, however, common mode errors are increased, and special measures must be taken if best performance is to be achieved. A thorough understanding of the error mechanisms involved will enable the sophisticated user to make use of the considerable flexibility available in the AØ2Ø.

Common to Normal Mode Conversion - This phenomenon may be understood in the context of Figure 6-21-12. The common mode voltage appears directly at IN LO, but it appears at IN HI only after going through the capacitive voltage divider formed by the source unbalance Rs with the stray capacitance to ground Cs. (Cs is the sum of the A/D converter input capacitance, the line-to-line capacitance of the cable plugged into the module input connector, and the capacitance from the external wiring to ground.) The attenuation at IN HI with respect to IN LO causes a differential (normal mode) signal to appear across the input to the AØ2Ø. The magnitude of this error signal may be simply calculated as follows:

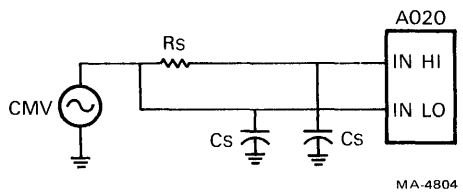


Figure 6-21-12 Source Unbalance

$$V_E = \frac{R_S}{R_S + |Zc|} Vcm$$

If, for example, R_S = 1K ohm and C_S = 100 pF, then at 60 Hz,

$$V_E = \frac{10^3}{10^3 + \frac{1}{10^{-10} \times 2\pi \times 60}} = 3.8 \times 10^{-5} V_{cm}$$

Thus, for a 1000-volt p-p common mode signal, the error voltage is 38 mV p-p.

Effects of Common to Normal Mode Conversion - Norman mode signals applied to the input of the A020 have two effects: excessive normal mode voltages cause dc errors by overloading the input, and in-range normal mode signals produce ac output errors that are attenuated by the normal mode rejection of the A/D converter.

The first effect is simple to understand. The normal mode error appears at the input as a modulation of the desired input signal. That is, if the input signal is 5 mV dc and the normal mode error is 10 mV p-p, the total differential input signal will vary between 0 and 10 mV. This total differential signal cannot be allowed to exceed 150 percent of the input range selected; otherwise, the A/D will run into internal voltage limits and rectify the error signal, causing dc errors.

The magnitude of the second effect, ac output errors, depends on the normal mode rejection of the A/D. The A020 has a notch filter characteristic at either 50 or 60 Hz (selected by switches). If the frequency of the error signal is within ±0.01% of these nominals (as the power line frequencies normally are in any locality served by a large power grid) the output errors will be reduced by at least 72 dB (4,000 to 1) from the input error (Figure 6-21-13). For small deviations from nominal, the output error degrades roughly linearly. If, for example, the power line frequency deviates by 0.1% from nominal (a near catastrophic condition in a large system), the A020 will provide approximately 60 dB (1,000 to 1) rejection to such frequencies applied differentially to its inputs. A 3 percent deviation - possible with some small diesel generators - would lead to approximately 32 dB of rejection, and might make input filters advantageous (refer to Differential Input Filters paragraph). It should be emphasized that these output errors appear as ac noise, and therefore may be simply eliminated by standard software averaging techniques.

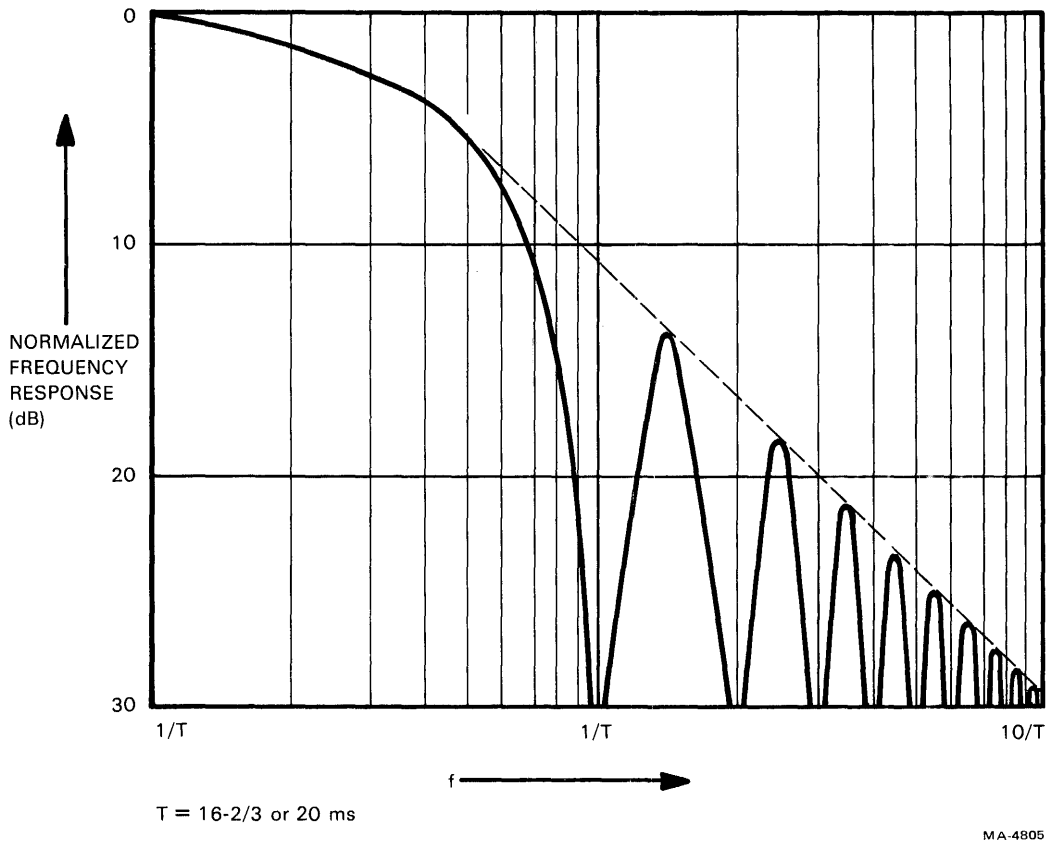


Figure 6-21-13 A020 Frequency Response

Handling High Impedance Sources
The following are three methods used to interface the A020 to high impedance sources.

Lower Gain - This is the easiest method, but involves the worst accuracy tradeoffs. If, for example, the ±100 mV range is selected for an application where the transducer produces an 8 mV full scale output, but the high source impedance produces up to 140 mV of peak normal mode error signal, the system will provide an LSB resolution of 6 microvolts, which is approximately equivalent to the resolution of a 12-bit A/D operating with a ±10 mV full scale range. Assuming 72 dB of NMR, 70 microvolts p-p of output noise will be produced.

This method is the most economical, allowing the 2-wire mode and therefore 16 channels per board to be used. It also requires no special external measures to be taken. The primary accuracy tradeoff is in integral nonlinearity; since the spec of ±0.01% is a percentage of full scale range, the linearity as a percentage of the transducer full scale output will be degraded. This may not be a serious problem, however, in applications where the dynamic range around the nominal input is small.

Shielded Inputs - The A02Ø may be used in a true 3-wire, shielded input mode by selecting the 3-wire option and opening the SHIELD switch. In order for this to be useful, the input leads must be shielded for their entire length from the transducer to the module input connector, and the shield must be grounded at the common mode source, (Figure 6-21-14). With R_{L1} = R_{L2} = 5ØØ ohms, the common mode rejection in this configuration has been measured at over 16Ø dB.

Differential Input Filters - Input filters provide another method to reduce the normal mode error signal at the A/D so that low full scale ranges may be used with high source impedances. In most cases, however, input filters substantially degrade performance. Consider the simple circuit (Figure 6-21-15).

The A02Ø in 2-wire mode provides about 1ØØ pF of stray capacitance to ground. When the channel relays switch, this stray capacitance must be charged to the common mode potential. One side of the channel switching will occur before the other, but since the charging time for the stray capacitance is nanoseconds, the 9Ø uF external capacitor will appear as a short, and half the charging current will flow through it creating an error voltage whose magnitude is the following.

$$V_s = \frac{1 \times 10^{-10}}{9 \times 10^{-5}} \times 1/2\ V_{cm}$$

In other words, this configuration would exhibit a common mode rejection of only 126 dB. In addition, the dielectric absorption (hysteresis) of a capacitor of this size leads to gross errors if the input varies over time scales of anything less than hours.

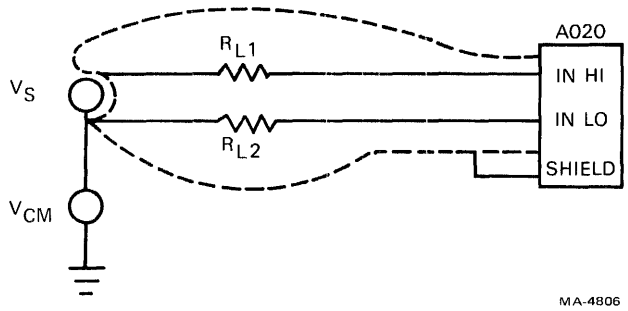


Figure 6-21-14 Shielded Input

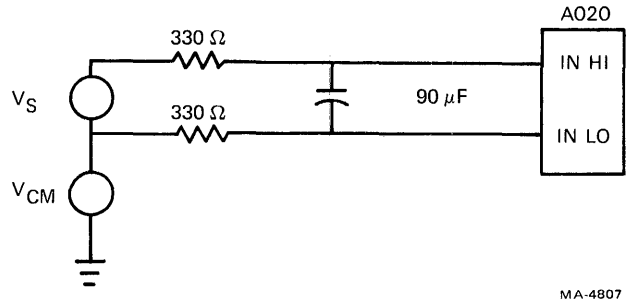


Figure 6-21-15 Input Filter

If input filtering appears to be the only solution to a high source impedance problem (or if it is necessary to reject a frequency other than 50 or 60 Hz or harmonics thereof), and poor common mode rejection cannot be tolerated, the 3-wire mode can be used to improve the CMR by approximately 20 dB (factor of 10). In this case, the SHIELD switch must be on and the INTERNAL FILTER switch must be off. The shield input must be brought back directly to the common mode source; the stray capacitance will be charged through the shield lead and not through the input filter.

Capacitive Source Errors

Capacitive sources can create serious errors when used with any multiplexed input device, including the A020. The problems become particularly serious when high common mode voltages are involved.

The problems occur because of spikes due to input and internal switching being generated on the input lines and imposing error voltages across the source capacitance. This capacitance is sometimes not deliberately present but arises from stray capacitance in long wiring runs.

No problem arises if the time constant of the source impedance and source capacitance is less than 300 microseconds. Such a source will have adequate time to settle between the time of input switching and the actual start of a conversion. Therefore, if the source resistance is 1K ohm, the capacitance may be as much as 0.3 mfd before problems are encountered; with Rs = 100 ohms, Cs may be up to 3 uF. Note that this precludes the use of input filters effective at 60 Hz unless special measures are taken (refer to section on using the A020 with high common mode voltages).

Open Thermocouple Detection

The internal filter provided in the input to the A020 may be used to implement open thermocouple detection without the enormous errors generated by schemes which apply constant voltage or current sources directly to inputs. In these older schemes, moderately high (approximately 10M ohms) resistors were often connected between the inputs and ground-referenced power supplies; since the full common mode voltage was applied through the resistor to the input, a simple voltage divider was formed which

would effectively reduce the common mode rejection to 80 dB for a 1K source impedance. This translates into a 20 mV error for a 200 volt common mode voltage, making the scheme unusable.

The technique that can be implemented with the A020 involves alternate high and low level conversions. Whenever it is desired to check a particular thermocouple, a conversion should be performed on a high level signal (such as the ATR16 reference temperature output or the ATR16 12-volt power available on the A020 input connector). The results of this conversion are not of interest and need not be in range. The purpose of this operation is to charge the internal filter capacitor to a level higher than the thermocouple full scale. A conversion should then immediately be done on the thermocouple of interest. If the thermocouple is good, the capacitor will discharge to the proper input level in the several milliseconds allowed for input settling; otherwise, the results of the conversion will be an overrange, indicating an open thermocouple.

Thermal Offsets

The joining of any two unlike metals forms a thermocouple. On a printed circuit board, copper conductors are soldered to components which may or may not have copper leads but are almost certainly not constructed of copper throughout. Stray thermocouples therefore exist all over the board, and wherever heat-producing components generate thermal gradients, thermocouple voltages will be produced.

The practical result of these effects in the A020 is an offset error voltage produced in the input multiplexer relays. This error is specified as a channel-to-channel offset, and is measured by scanning all sixteen channels at maximum rate for at least several minutes. The specification of scan mode and rate is important because the relay coils require significant power, all of which is dissipated as heat; the faster a channel is scanned the greater the thermal offset voltage. If one channel is continuously scanned for a long period of time, the thermal error can be on the order of 100 microvolts. Furthermore, an error will be generated not only in the channel being switched, but also in channels whose input relays are nearby and are therefore heated by the operating relay. Time constants for these thermal effects are on the order of minutes, so fast scanning of one or a few channels for several seconds will cause only small errors.

Since the number of variables is too large to allow useful specification characterization, it is recommended that the user experiment by shorting the inputs and observing the offsets produced for his scanning pattern if channels are to be scanned more than twice per second and low level signals are involved.

SPECIFICATIONS

General	
Resolution	14-bit plus sign
Number of channels	Sixteen 2-wire or eight 3-wire, switch selectable
Power Requirements	
Voltage	Main supply: VS = 12 Vdc ± 5% Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc
Operating current	2Ø5 mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 175 mA maximum
Backup supply: 3Ø mA maximum

Standby current (backup supply)	3Ø mA maximum
Warmup time	1Ø minutes (for module only; does not include temperature stabilization time for enclosure)
Input Characteristics	
Voltage ranges	± 1Ø mV and ± 1Ø.24 mV ± 2Ø mV and ± 2Ø.48 mV ± 5Ø mV and ± 51.2Ø mV ± 1ØØ mV and ± 1Ø2.4Ø mV ± 2ØØ mV and ± 2Ø4.8Ø mV ± 5ØØ mV and ±512 mV ± 1 V and ± 1.Ø24 V ± 2 V and ± 2.Ø48 V ± 2.5 V and ± 2.56 V ± 5 V and ± 5.12Ø V ± 1Ø V and ± 1Ø.24Ø V ± 2Ø V and ± 2Ø.48 V ± 25 V and ± 25.6Ø V ± 5Ø V and ± 51.2Ø V
Input Impedance	
1Ø and 2Ø mV range	1Ø Mohms minimum
All other ranges	Input divider off: 5Ø Mohms minimum Input divider on: 1 Mohm ± 1%
Power off	5Ø Mohms minimum
Maximum input overload	264 Vac RMS minimum with no damage
Bandwidth	2Ø Hz minimum

Throughput	31 conversions per second for 50 Hz operation; 37 conversions per second for 60 Hz operation; total or same channel
Common Mode Performance	
Common-mode voltage	±500 V peak from ground or between channels, minimum
Common-mode and crosstalk rejection	150 dB minimum at 60 or 50 Hz ± 0.1%, with a 10 ohm source impedance
RF common mode rejection	150 dB typical, 100 dB minimum, 5 kHz to 50 MHz
Normal mode rejection	60 dB minimum at 50 or 60 Hz, ±0.1%
Overload recovery time	By next conversion for overloads up to 50% over the selected full scale range; within four conversions for overloads between 50% and the maximum ratings
Accuracy	
Differential Nonlinearity	±1/2 LSB maximum
Nonlinearity	±0.01% of full scale range (±3 LSBs) maximum
Offset	
Initial	Adjustable to zero
Drift with temperature	2 microvolts/° C, maximum
Channel-to-channel	2 microvolts typical 10 microvolts maximum (varies with air flow over module)
Input bias current	1 nA maximum
Full Scale Temperature Coefficient	
With input divider	±60 ppm/° C maximum
Without input divider	±30 ppm/° C maximum

Equivalent input noise	3 microvolts or 1/3 LSB RMS, whichever is greater
Protection	Input circuits are protected from field overvoltages by fusible resistors in series with each input. There is a one half Amp fuse to protect the ATR16 power supply (see text).
Physical Characteristics	Two quad modules assembled as a mother-daughter combination make up the A02Ø module
Dimensions	Quad module, triple width, 8-1/2 inch length
Field connector	Cable type BC4ØA, or customer supplied 5Ø-pin Berg connector
Environmental Characteristics	Complies with DEC STD 1Ø2 Class C Operates in convection cooled environment up to 6Ø degrees C ambient
Heat dissipation	9 Btu/hr maximum

FUNCTIONAL DESCRIPTION

The ATR16 (Analog Temperature Reference - 16 Point) is an isothermal screw terminal assembly used for connecting thermocouple field wiring to an analog input subsystem. The assembly accepts up to 16 thermocouple inputs and provides a single ambient temperature reference output.

The ATR16 consists of a printed circuit board assembly enclosed in a thermal-insulated chassis. The circuit board assembly includes screw terminals for field inputs, a temperature transducer, and an output connector (Figure 6-22-1). A 3 m (10 ft) cable is included for connecting the ATR16 directly to the analog input module. (Refer the paragraph Output Cable Installation below for additional information on connecting the ATR16 to the input module.) Signal wire pairs from the field thermocouples are connected to the plus and minus terminal pairs labeled channel 0 through 7, and 10 through 17 (Figure 6-22-2). ATR16 construction is such that when field wiring is connected and the cover attached, the terminals are all at the same temperature and provide nearly identical reference junctions for all field inputs. The temperature inside the enclosure (i.e., the reference temperature) is monitored by the transducer; its output is connected to the pair of terminals marked HI and LO. The temperature transducer is powered by the analog subsystem through J1.

The ATR16 has provision for 16 field inputs; one of these may be used to read the output of the reference temperature transducer. Alternatively, if all channels are needed for thermocouples, the transducer output can be connected to one of the analog subsystem high level inputs (i.e., A014 or A156).

DETAILED DESCRIPTION

The ATR16 provides screw terminal pairs at a uniform temperature (i.e., isothermal reference junctions) and a transducer that measures this temperature. These items are discussed below.

Isothermal Reference Junction

In order that the output of the temperature transducer be a valid datum for all ATR16 screw terminals, they must all be at the same temperature. Two things are done to achieve this uniform temperature. First, the terminals are well insulated from any external thermal shocks in the operating environment, so that they will experience only gradual temperature changes. This is achieved in the ATR16 by providing a tight enclosure and extensive thermal insulation around the terminals.

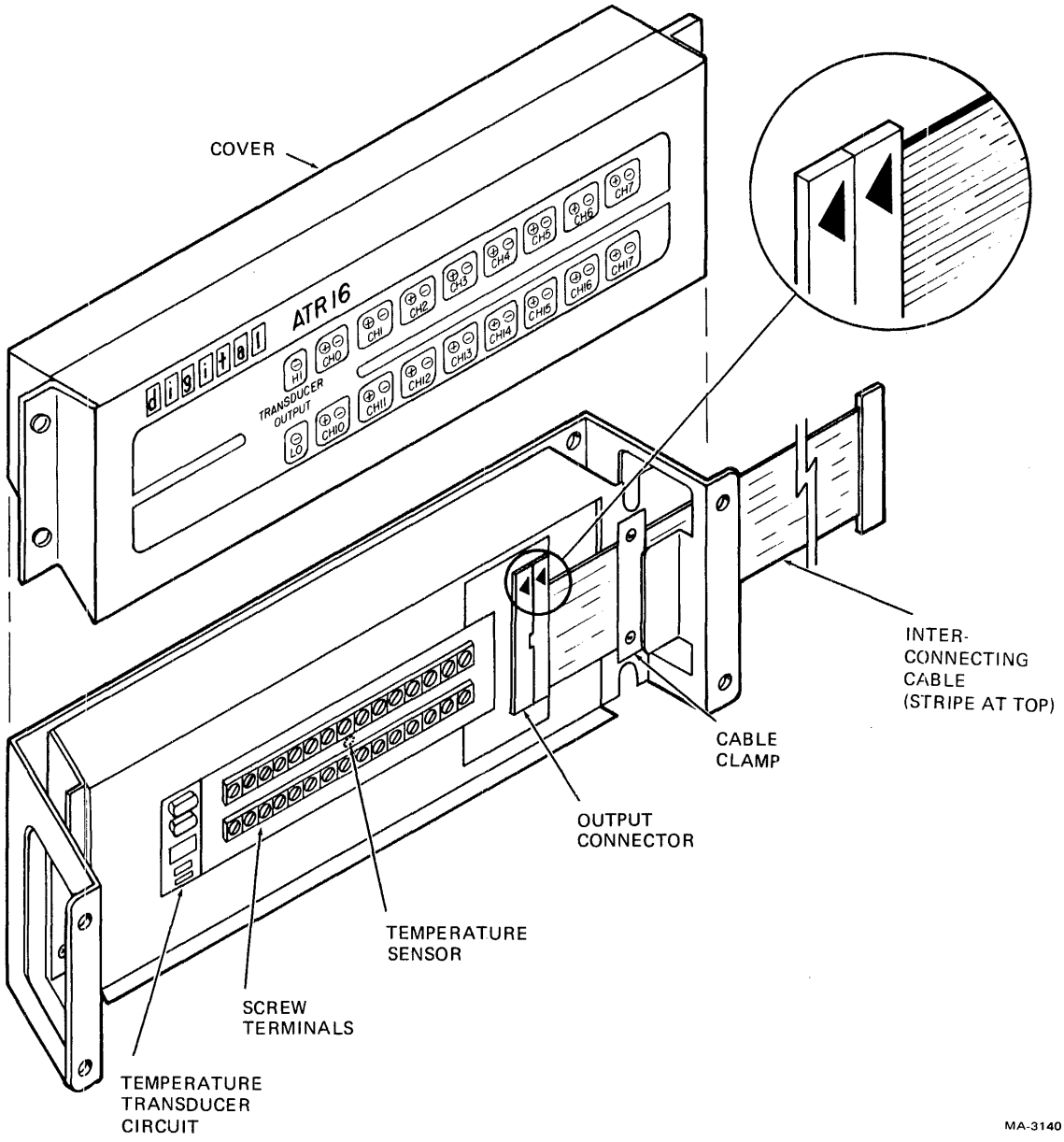


Figure 6-22-1 ATR16 Chassis Assembly

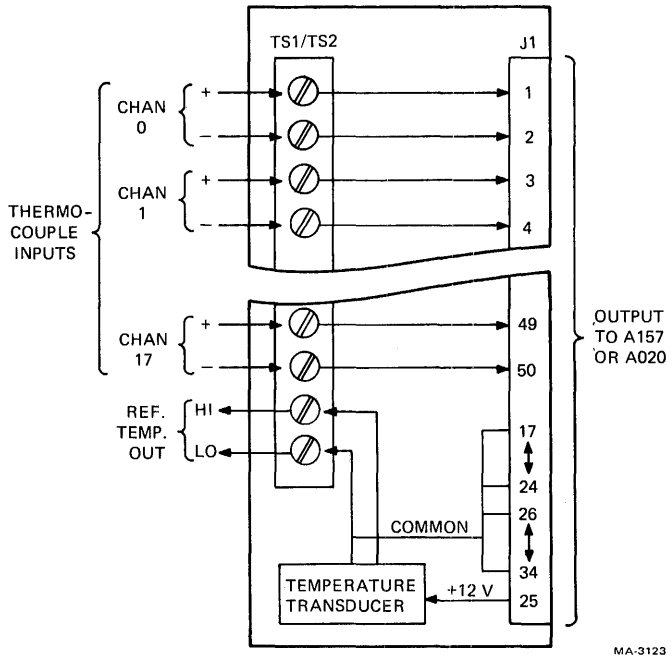


Figure 6-22-2 ATR16 Block Diagram

Second, a thermal bond is provided between all screw terminals to ensure that they are all at the same temperature. This is accomplished as follows. The printed circuit board assembly on which the terminal strips are mounted includes a copper plate that is sandwiched between the terminal strips and the printed circuit board (Figure 6-22-3). Each terminal passes through a hole in the copper plate so that no electrical contact is made. However, the hole is filled with thermal compound so that a good thermal bond is ensured. This thermal bond, combined with the high heat conductivity of the copper plate, minimizes thermal gradients between screw terminal pairs.

Temperature Transducer

The temperature transducer circuit produces an output voltage that is directly proportional to the reference temperature (i.e., the temperature of the screw terminals). The relationship is:

$$Vo = 0.1\ Tr$$

where:

Tr = internal ambient temperature in degrees C

Vo = transducer output voltage.

The operating range is from 5 degrees C to 60 degrees C which corresponds to an output voltage range of 0.5 V to 6.0 V.

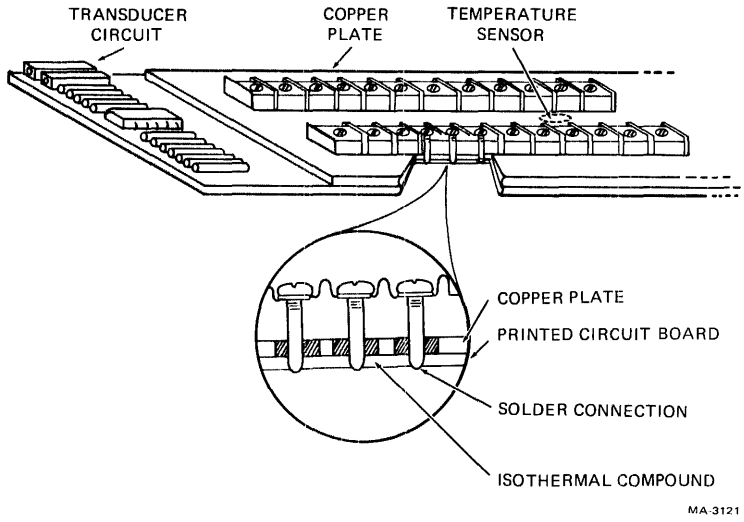


Figure 6-22-3 Isothermal Assembly

The circuit consists of a voltage reference, an operational amplifier, and a temperature sensing element (Figure 6-22-4). The sensor is a precision thermistor array located in the center of the copper plate that thermally bonds all the screw terminals. The rest of the circuit is located at one end of the printed circuit board assembly (Figure 6-22-1). The resistance of the thermistor array varies as a function of temperature. The voltage reference and operational amplifier circuit provide the necessary offset and gain to translate this into Vo, the desired output voltage.

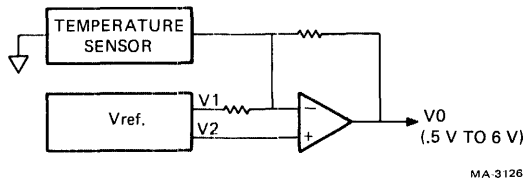


Figure 6-22-4 Temperature Transducer Circuit

MECHANICAL INSTALLATION

General

The ATR16 may be installed anywhere in the system that allows the 3 m (10 ft) interconnecting cable to reach its intended module interface. The chassis requires 13.33 cm (5.25 in) of vertical mounting space in a standard 48.26 cm (19 in) equipment rack and is 11.43 cm (4.5 in) deep.

DEC Cabinet

Using the hardware provided, install the chassis in the chosen location as follows.

1. Fasten the four speed nuts to the equipment rack mounting holes in the chosen location.

2. Fasten the four male/female hex standoffs to the speed nuts.

3. Place the ATR16 on the standoffs and fasten with four 10-32 X 5/8 inch truss head screws and four No. 10 internal tooth lockwashers.

4. Fasten the ATR16 ground lug to the equipment rack side rail with the 10-32 X 1/2 inch screw, 10-32 kep nut, and No. 10 external tooth lockwasher provided. The lockwasher must be placed under the ground lug and the nut fastened securely to ensure good contact with the equipment ground through the paint (Figure 6-22-5).

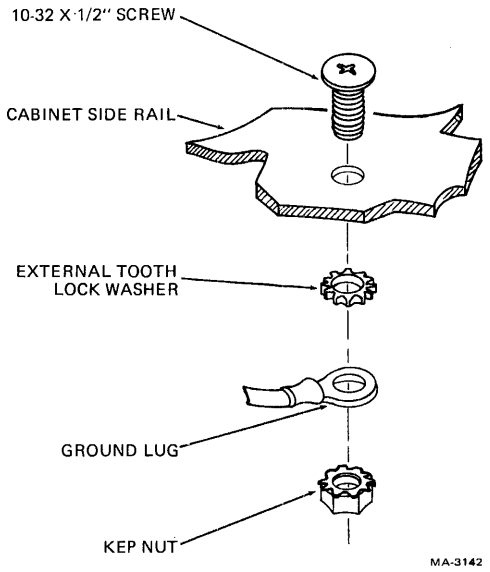


Figure 6-22-5 Ground Wire Fastening

Industrial Enclosure

The ATR16 may also be installed in a user supplied industrial enclosure. Mounting holes on the rear of the chassis facilitate this type installation. Figure 6-22-6 shows the mounting hole dimensions. When considering this type installation, provision must be made to ensure that the temperature inside the enclosure does not exceed 60 degrees C when the system reaches thermal equilibrium. It is recommended that the ATR16 be mounted on the

standoffs supplied with the unit rather than directly to the cabinet backplate; this improves the thermal isolation properties of the ATR16.

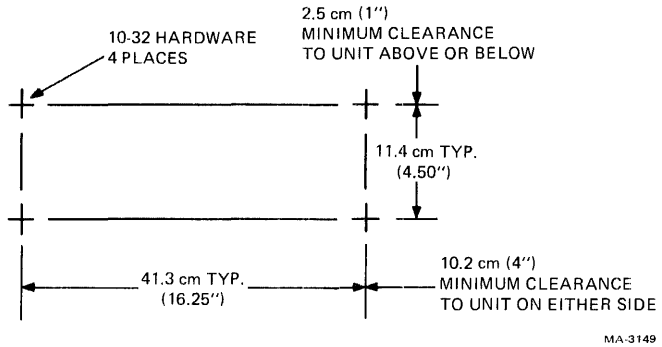


Figure 6-22-6 Rear Mounting Dimensions

ELECTRICAL INSTALLATION

Interconnecting Cable

To connect the ATR16 to its intended module interface, proceed with the following steps.

1. Remove the ATR16 cover.
2. Loosen the right cable clamp.
3. With the stripe up, bring one end of the interconnecting output cable through the right side of the ATR16 chassis. Guide the cable through the cable clamp and connect it to J1 on the printed circuit board assembly with the cable-free side of the connector against the printed circuit board.
4. Tighten the cable clamp.
5. Guide the other end of the cable through the cabinet to its intended module interface.
6. Plug the cable into the module with the cable-free side of the connector against the module and with the stripe down.

Field Wiring

To ensure that proper practices are followed when installing field wiring, the user should review the field wiring information contained in Chapter 3, Paragraphs 3.8 through 3.8.4 before proceeding with the following installation. This procedure is for bottom entry to a DEC-supplied H96Ø cabinet and can be modified to accommodate top entry or a user-supplied cabinet.

NOTE

To realize optimum thermal performance of the ATR16, it is recommended that the field wiring be of the smallest size consistent with the application.

1. Bring the field wiring through the bottom of the H96Ø cabinet.
2. Guide the wiring along the channel formed by the cabinet vertical supports and clamp it securely in place.
3. Loosen the left cable clamp of the ATR16.
4. Bring the field wiring into the left side of the chassis and through the cable clamp.
5. Fasten the field wiring to the screw terminals as shown in Figure 6-22-7 or 6-22-8.
6. Tighten the cable clamp.
7. Replace the ATR16 cover.

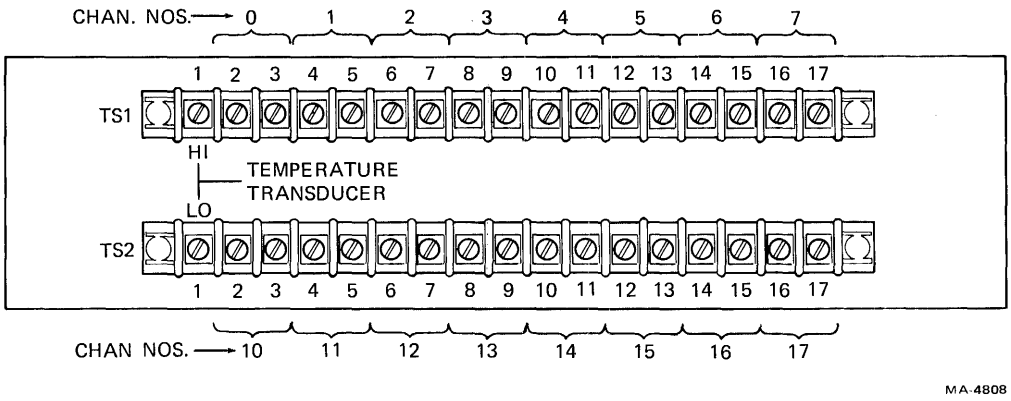


Figure 6-22-7 2-Wire I/O Connections (A157 or AØ2Ø)

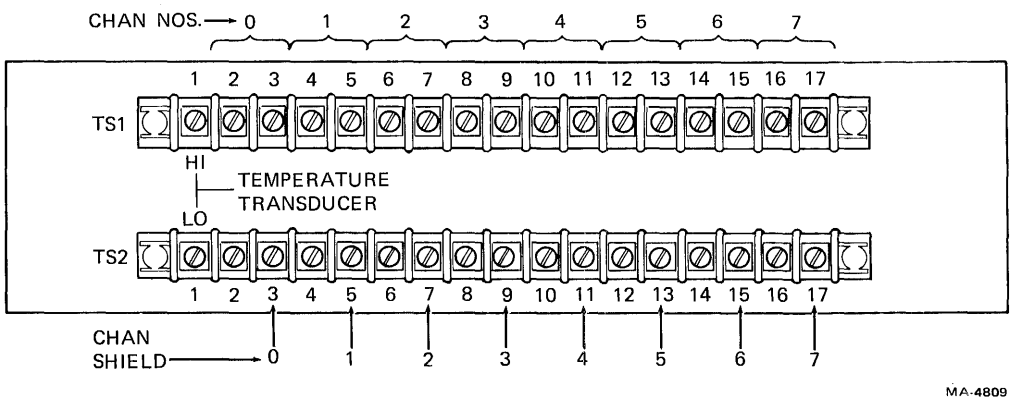


Figure 6-22-8 3-Wire I/O Connections (AØ2Ø only)

DC Power

Separate power supply connections are not required for the ATR16. Power (+12 Vdc) for the temperature transducer is input from the interfacing module via the interconnecting cable (Figure 6-22-2); however, a switch on the interfacing module must be in the on position to connect power to the cable. This switch is identified in Table 6-22-1 for each type interfacing module.

Table 6-22-1 ATR16 Power Switches

Interfacing Module	Power Switch Location
A157	E30-4
A020	E6-10 (on daughter board)

Transducer Output Connection

Temperature output may be connected to one of the ATR16 internal screw terminal pairs or it may be connected to an external screw terminal pair (i.e., A156 or A014). These two options are illustrated in Figure 6-22-9.

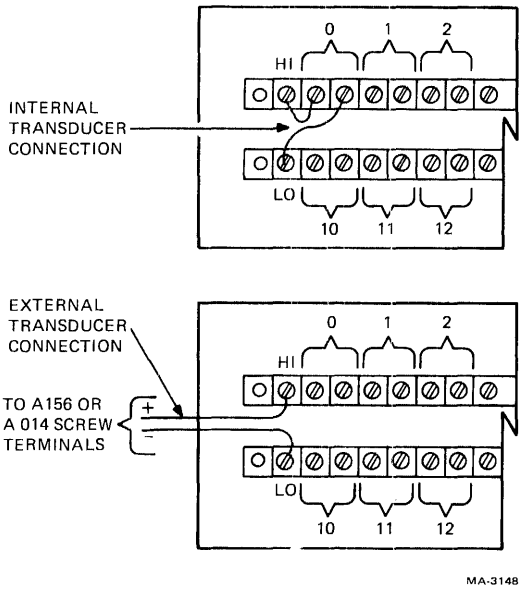


Figure 6-22-9 Transducer Output Connection Options

APPLICATION INFORMATION

Voltage output from a thermocouple circuit is a function of the materials employed and the temperatures of the two thermocouple junctions. If one of the junctions is at a known temperature, and the voltage is known, the temperature of the other junction can be determined.

The ATR16 enables the user to make this type measurement. For example, if Tm is the temperature of interest at the field thermocouple (Figure 6-22-1Ø), then:

$$Tm = f[f(Vm - 1Ø\ Vo)]$$

where:

Vm = thermocouple circuit voltage
Vo = temperature transducer output voltage.

The indicated functions are nonlinear and are evaluated by various analytical and/or lookup techniques that are beyond the scope of this document.

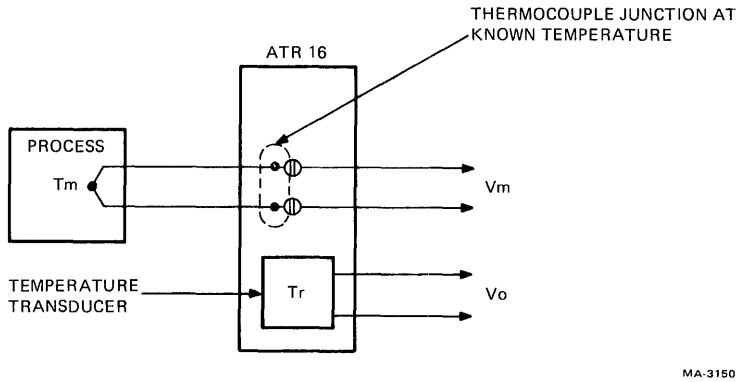


Figure 6-22-1Ø ATR16 Application

Note that the range of Vo is from Ø.5 V to 6.Ø V, corresponding to a temperature range of 5 degrees C to 6Ø degrees C. The range accommodated by the analog subsystem depends on which A/D converter and what gain is used. These factors also affect resolution. Table 6-22-2 lists the characteristics of the two converters that are pertinent to this discussion.

Table 6-22-2 A/D Converter Characteristics

A/D Converter	A014		A020	
Multiplexer	A014, A156, or A157	A157	A020	A020
Gain	1	2	1	2
Input Range	±10 V	±5 V	±10 V	±5 V
No. bits	12	12	15	15
LSB	5 mV	2.5 mV	600 microvolt	300 microvolt
Temperature Span	5 degrees to 60 degrees C	5 degrees to 50 degrees C	5 degrees to 60 degrees C	5 degrees 50 degrees
Resolution*	0.05 degrees C	0.025 degrees C	0.006 degrees C	0.003 degrees C

*Note that this resolution does not imply equivalent accuracy, which is a function of the ATR16 temperature transducer.

In order for the reference temperature (i.e., the temperature transducer output) to be valid, it must be read just before or after the field thermocouple voltage is read. This constraint becomes more critical if the ATR16 environment is subject to significant thermal shocks. The effect of ambient temperature step changes on the reference temperature for a given elapsed time can be described by the following transfer function:

$$Tr = To + Ts\ [1 - e^{-\frac{t}{\tau}}]$$

where:

Tr = reference temperature
To = reference temperature before step change
Ts = magnitude of step change
t = time in hours
τ = ATR16 thermal time constant.

The maximum slope given by this equation can be approximated as:

$$\frac{\Delta Tr}{\Delta t}\ (\text{maximum}) = 2 \times 10^{-4}\ Ts$$

In addition to their effect on reference temperature, thermal shocks to the ATR16 also produce thermal gradients on the screw terminals which show up as an error (i.e., the temperature of the terminals is different from the transducer output). The maximum value of this error for a given step change in the ambient temperature is shown in Figure 6-22-11a.

The maximum thermal gradient error will not be reached immediately, but will build up gradually and then decay. Therefore, the amount of error depends on how much time has elapsed since the thermal shock. The relationship between time and error is shown in Figure 6-22-11b.

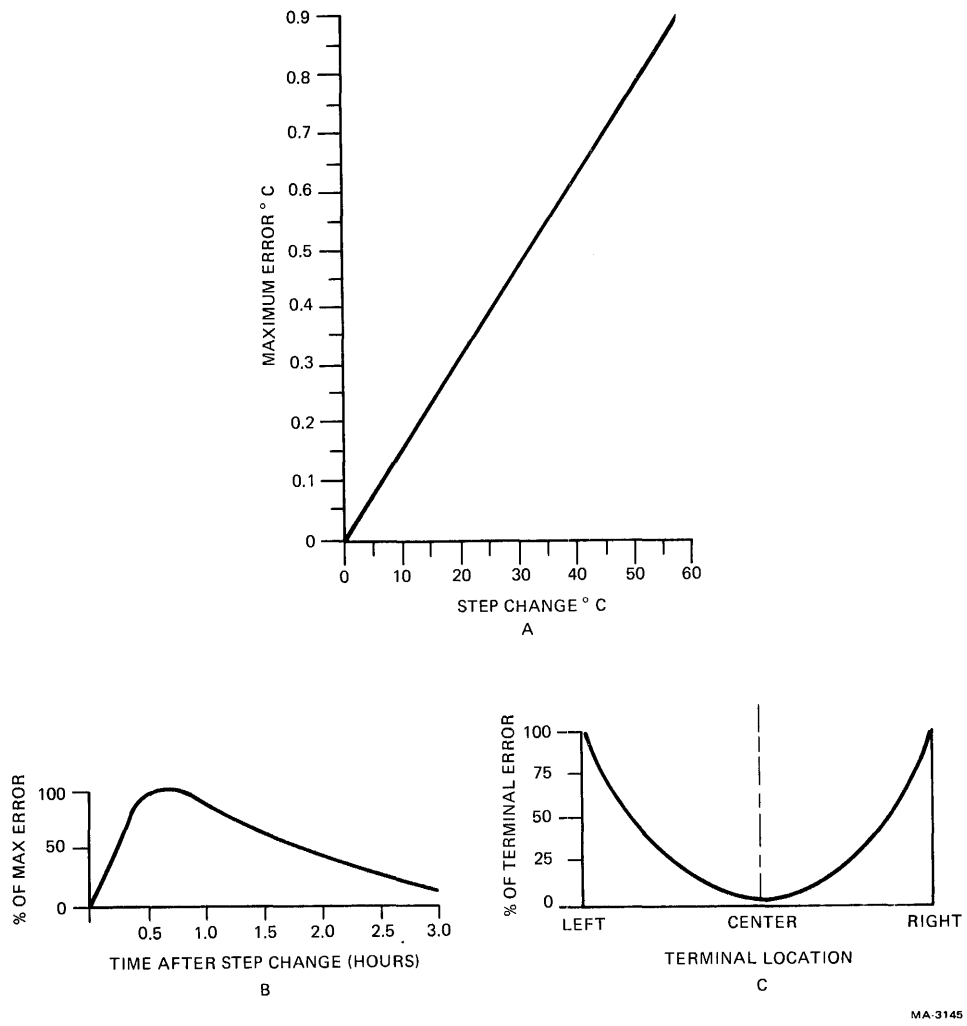


Figure 6-22-11 ATR16 Typical Characteristics

In general, the thermal gradient error is virtually nonexistent for terminals at the center of the screw terminal assembly where the sensor for the reference temperature transducer is located. The error increases for terminals toward either end, reaching a maximum at the outermost terminals (Figure 6-22-11c). It is therefore possible to nearly eliminate the effects of thermal gradient errors for a critical thermocouple by assigning it a center channel.

SPECIFICATIONS

Power Requirements	
Voltage	12 Vdc (+2 or -1) Vdc
Current	10 mA maximum
Input Characteristics	
Cross talk (channel to channel) including interconnecting cable)	with A157: 80 dB minimum at 60 Hz with 1K source unbalance with A020: 140 dB minimum at 60 Hz with 1K source unbalance
Common mode voltage	Limited by analog input of A020 or A157
Physical Characteristics	
Dimensions	13.33 cm (5.25 in) height 48.26 cm (19 in) width 11.43 cm (4.5 in) depth
Weight	3.2 Kg (7.1 lbs)
Environmental Characteristics	Complies with DEC STD 102, Class C. Operates in convection cooled environment up to 60 degrees C ambient.
Heat dissipation	0.053 Btu/hr maximum
Thermal Characteristics	
Transducer output (nominal)	Vo = 0.1 Tr (Tr in degrees C, V_o in volts)
Transducer accuracy	$\pm$0.25 degrees C maximum, under normal ambient temperature variations
Thermal time constant	1.5 hours

FUNCTIONAL DESCRIPTION

The A63Ø module comprises four independently addressable, 1Ø-bit, digital to analog converters (DACs) for use in the H333 I/O Subsystem. Current and voltage output options, with protection circuits, are provided for each converter. Provision is made for reading the output status, zeroing all outputs, and reading the module's generic code. The module features switches for address selection, calibration, and output mode selection.

DETAILED DESCRIPTION

A simplified block diagram of the DAC module is shown in Figure 6-23-1. At the left of the figure, the unit receives data and control signals from the D-bus, converts the digital data to an analog signal via one of the four DACs, and outputs this signal to the field through the interface connector. The following paragraphs elaborate on individual sections of the block diagram and discuss the module's control sequences and data flow.

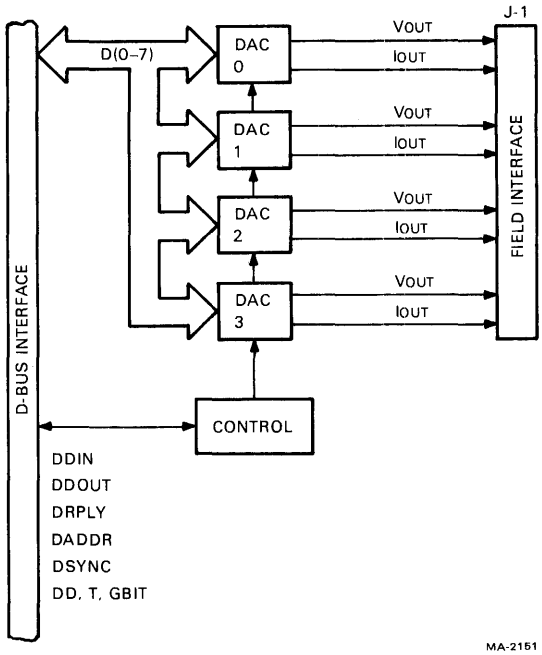


Figure 6-23-1 A63Ø DAC Module, Block Diagram

Register Formats

Each DAC channel occupies two addresses; a total of eight for the module. The converters are 10-bit devices; therefore, the input data word is transmitted in two bytes. The two most significant bits (MSBs) are in the D0 and D1 positions of the high byte and the eight least significant bits (LSBs) in the low byte (Figure 6-23-2). The high byte also contains four read-only status bits in positions D2-D5 when the TBIT is asserted. Bits D6 and D7 are not used.

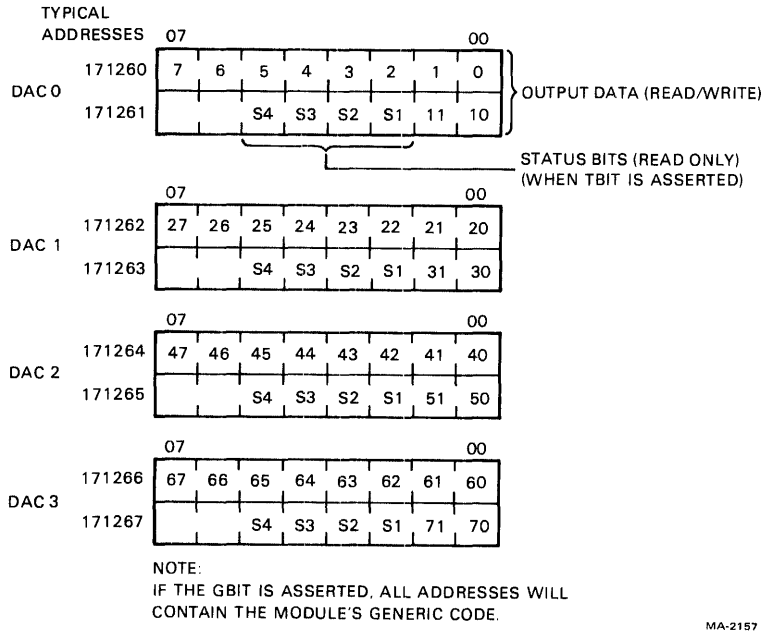


Figure 6-23-2 DAC Data Registers

Data Paths

When a data word is to be output to one of the four DACs, the high byte is output first and then the low byte. The high byte is strobed into one of the four holding registers by WR1, WR3, WR5, or WR7, depending on which of the four DACs has been addressed (Figure 6-23-3). When the low byte data is received, it and the two bits in the holding register are strobed into the 10-bit output register by WR0, WR2, WR4, or WR6.

The output register drives the output disable gates. When the DBIT is asserted, these gates force the data input to the DACs to zero.

The output disable gates drive CMOS switches that drive the D/A ladder networks. These devices produce analog signal outputs that are a function of the weights (binary values) of the asserted bits in the 10-bit data word.

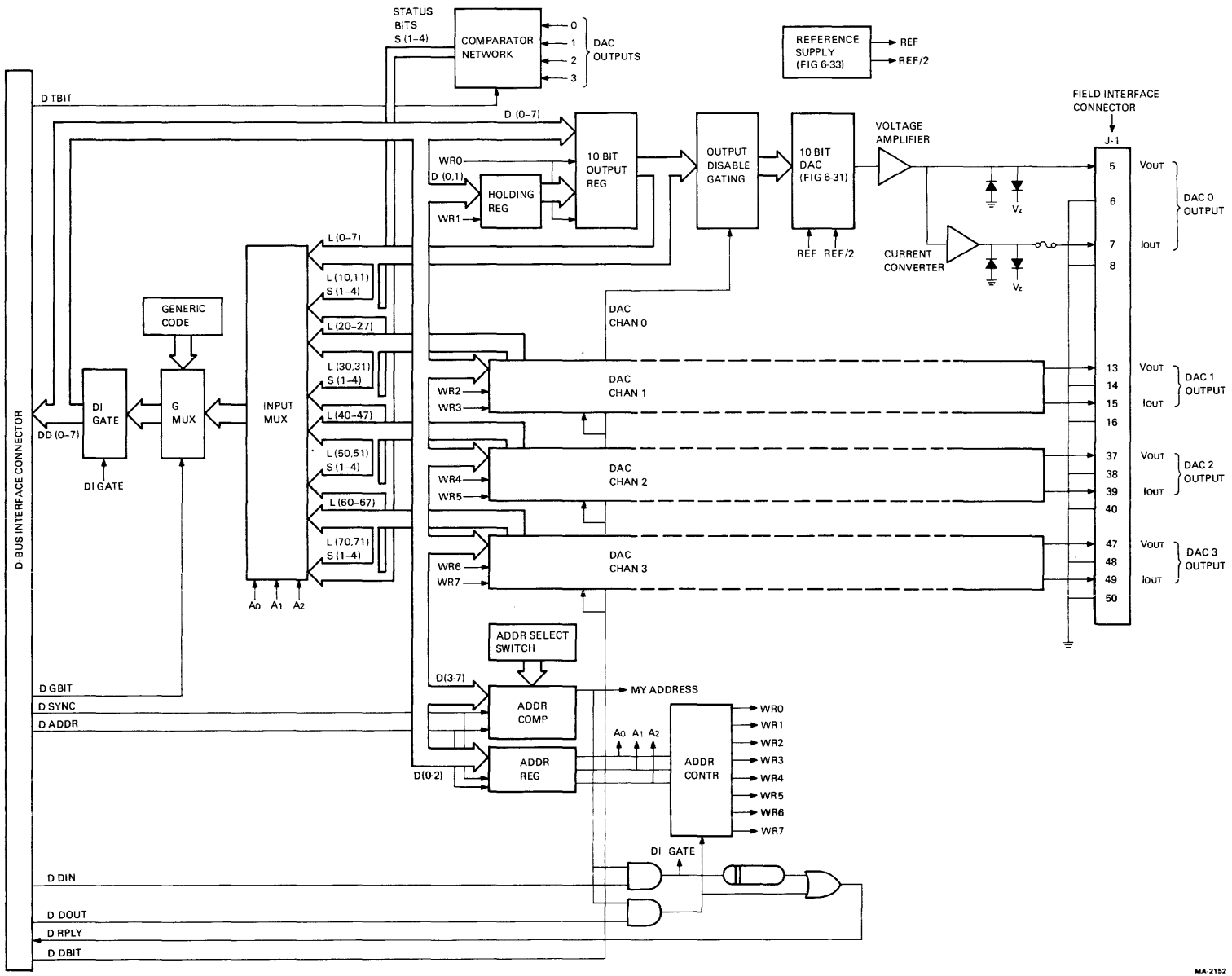


Figure 6-23-3 A630 Four-Channel DAC, Module Block Diagram

Each D/A ladder network drives a voltage output buffer amplifier; this amplifier drives a current converter circuit. Both the current and voltage output circuits go to the field interface connector at the right of the figure.

The voltage outputs also go to a comparator network that compares the outputs of the four DACs and provides output status information to the diagnostic program for maintenance use when the TBIT is asserted. These status bits are shown on the block diagram as bits S(Ø-4).

Finally, all output data registers and status information goes to the input multiplexer (at the left of Figure 6-23-3) where it can be read by the program under control of the AØ, A1, and A2 signals. The output of this multiplexer goes to the G multiplexer, which provides normal output data unless the GBIT is asserted. If the GBIT is asserted, this circuit puts out the generic code of the module. The G multiplexer output is then strobed onto the D-bus by the DI GATE signal.

Control Signals

Data transactions (DATAOs and DATAIs) to and from the DACs, as called for by the program, are controlled by D-bus Cycles originating in the IOCM. A data transaction begins with an addressing phase in which the module's address is put on the D-bus, followed by D SYNC. The module's address comparator decodes the address, and when D SYNC occurs, produces its internal MY ADDRESS signal. The lower three bits of the address are stored as the AØ, A1, and A2 signals. This completes the addressing part of the D-bus Cycle.

If the data transaction is a DATAO, by this time data will be put on the D-bus, and the next control signal asserted by the IOCM is D DOUT. This causes the WRØ-WR7 decoder to produce one of its outputs and strobe the data byte into the proper register. Figure 6-23-3 shows that D DOUT also produces the D RPLY signal telling the processor that output data has been received. The processor then negates D DOUT.

The DACs on this module have a 1Ø-bit input word, so a complete data transfer actually requires two D-bus Cycles or DATAOs. The high byte data is always output in the first cycle and the low byte in the second. For example, if the channel two DAC at base address 171260 is being addressed, the high byte data (address 171265) is output first and strobed into the 2-bit holding register by the WR5 signal. The low byte (address 171264) is then output and all ten bits are strobed into the output register by the WR4 signal. The output data remains unchanged until the processor outputs a new data word to the low byte address.

If the program wants to monitor the digital word of a DAC output, it causes the processor to perform DATAIs on its two addresses. In the case of a DATAI, the addressing part of the cycle is the same as for a DATAO. The lower three bits of the address that are

stored as AØ, A1, and A2 set up the input multiplexer for the correct byte, and when the processor asserts D DIN, this data is strobed onto the D-bus by the DI GATE signal. After a short delay, DI GATE produces D RPLY, notifying the processor that data is on the bus. The processor then causes the IOCM to negate D DIN. Again, two addresses must be read to get all ten bits of data, so another D-bus Cycle (DATAI) will follow.

Between the input multiplexer and the DI gates is the G multiplexer. This multiplexer outputs data from the input multiplexer unless the program has set the GBIT in the CSR of the IOCM. In that case, the module's generic code is put on the bus instead of normal data.

When the program sets the DBIT, it disables the output registers to all four DACs, which sets all their outputs to zero. The contents of the registers can still be read by the processor.

If the program sets the TBIT, the status bits are enabled and placed in the high byte of the data word being read.

CAUTION

When using the diagnostic test associated with the TBIT, the DBIT cannot be used to disable the DAC outputs; instead, the module's output cable must be disconnected to inhibit output signals to the customer's equipment. This is because the TBIT function for this module enables monitoring the output comparator network status bits while the DAC outputs are being exercised. While it is true that the DBIT disables (zeros) the DAC outputs to the customer, it is also true that it invalidates the output comparator signals.

DAC

Each channel consists of a set of analog switches, an R/2R ladder network, a voltage amplifier, and a current converter (Figure 6-23-4). The switches, driven by the output data word, switch the legs of the ladder between REF/2 and ground; the MSB is at the amplifier end and the LSB at the other end of the ladder. Each ladder leg that is switched to ground produces an incremental output according to its binary weight. The output of the ladder network is a current that is the sum of the contributions of the asserted bits of the data word.

The voltage amplifier converts the output current of the ladder network to a proportional voltage. The LSB (DØ) produces an output of 1Ø mV and succeeding bits are weighted to produce 2^n times this amount, where n is the bit number. Therefore, the MSB (D9) produces 1Ø mV times 512 or 5.12Ø V. If all bits are asserted,

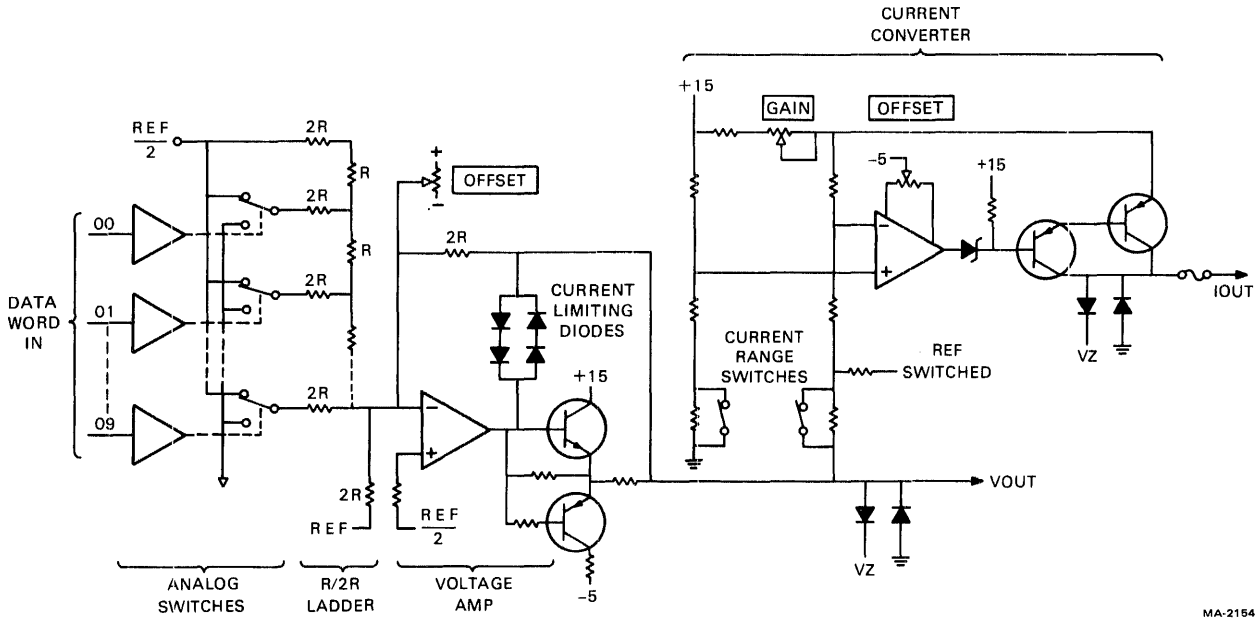


Figure 6-23-4 DAC Circuit

their combined weights add up to 10.230 V. Table 6-23-1 lists the weight of each bit.

Voltage amplifier output is current-limited and should not be loaded in excess of 15 mA. Clamp diodes provide output protection in the event of externally applied overvoltages.

In addition to the voltage output, each DAC has a unipolar current converter that outputs a current from 0 to 20 mA or from 4 to 20 mA. Switches on the module allow the user to select the desired current range independently for each DAC. Changing the current range requires recalibration of the current converter, but does not affect the voltage outputs.

The current converter is a self-balancing bridge arrangement that uses the voltage amplifier's output as its input (Figure 6-23-4). When the output of the voltage amplifier is changed, the current converter rebalances its bridge by changing the current delivered to its load. Therefore, it is able to produce a current proportional to the output of the voltage amplifier. When both switches at the current converter's inputs are opened, an offset and gain change are introduced, placing it in the 4 to 20 mA mode.

The current converter circuit includes offset and gain controls for calibration purposes. The output circuit is a Darlington amplifier circuit protected by a series fuse and clamping diodes. The output voltage of the current converter is limited by the power supply. It should not be expected to deliver an output voltage in excess of 10 V.

In the Ø to 2Ø mA mode, the LSB (DØ) produces an output of 19.55 microamp, and succeeding bits have binary-related weights such that the MSB (D9) produces a current of 19.55 microamp X 512 = 1Ø.ØØ978 mA. Table 6-23-2 lists the current produced by each bit.

Table 6-23-1 Voltage Output Bit Weights

Bit No.	Weight (mV)
Ø	1Ø
1	2Ø
2	4Ø
3	8Ø
4	16Ø
5	32Ø
6	64Ø
7	128Ø
8	256Ø
9	512Ø
Total (All bits asserted)	1Ø23Ø

Table 6-23-2 Current Output Bit Weights (Ø to 2Ø mA option)

Bit No.	Weight (microamp)
Ø	19.55
1	39.1Ø
2	78.2Ø
3	156.4Ø
4	312.81
5	625.61
6	1251.22
7	2502.44
8	5004.89
9	10009.78
Total (All bits asserted)	20000.00

In the 4 to 2Ø mA mode, normal current output with no bits asserted is 4 mA. The LSB causes a current increase of 15.64Ø microamp for a total output of 4Ø15.64Ø microamp. Succeeding bits have binary related weights such that the MSB (D9) causes an increase of 15.64Ø microamp X 512 = 8.ØØ782 mA, for a total output of 12.ØØ782 mA. Table 6-23-3 lists the contribution of each bit and the resulting current output when only that bit is asserted.

Both voltage and current outputs of a DAC can be used as long as the total module load does not exceed 8Ø mA.

Table 6-23-3 Current Output Bit Weights
(4 to 20 mA option)

Bit No.	Weight (microamp)	Offset (microamp)	Output (microamp)
0	15.640	+4000	4015.640
1	31.280	+4000	4031.280
2	62.561	+4000	4062.561
3	125.122	+4000	4125.122
4	250.244	+4000	4250.244
5	500.489	+4000	4500.489
6	1000.977	+4000	5000.977
7	2001.955	+4000	6001.955
8	4003.910	+4000	8003.910
9	8007.820	+4000	12007.820
Total (All bits asserted)	16000.000	+4000	20000.000

Internal Comparator

The module's four DAC outputs are input to a comparison network that generates the four status bits (Figure 6-23-3). These bits have the following significance:

S1 = 1 for V1 $\geq$ (V0 +30 mV)
S1 = 0 for V1 $\leq$ (V0 -30 mV)

S2 = 1 for V2 $\geq$ (V1 +30 mV)
S2 = 0 for V2 $\leq$ (V1 -30 mV)

S3 = 1 for V3 $\geq$ (V0 +30 mV)
S3 = 0 for V3 $\leq$ (V0 -30 mV)

S4 = 1 for V3 $\geq$ (V2 +30 mV)
S4 = 0 for V3 $\leq$ (V2 -30 mV)

The program monitors this status information by asserting the TBIT and reading the high byte of the DAC output. If the DACs are all in calibration, the status bits assume predictable states as a function of the four DAC inputs, thus providing diagnostic information to the program. Note that between the limits specified above for each status bit, the bits are undefined. This is shown graphically in Figure 6-23-5 for status bit S1.

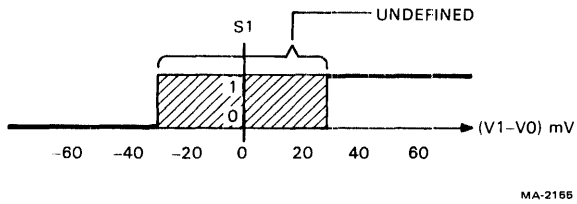


Figure 6-23-5 Status Bit S1

Reference Supply

There is a separate voltage supply on the module for producing the REF (10.240 V) and REF/2 (5.120 V) voltages used by the DAC circuits. A simplified schematic is shown in Figure 6-23-6. The circuit consists of a 6.2 V zener reference diode and operational amplifier buffers.

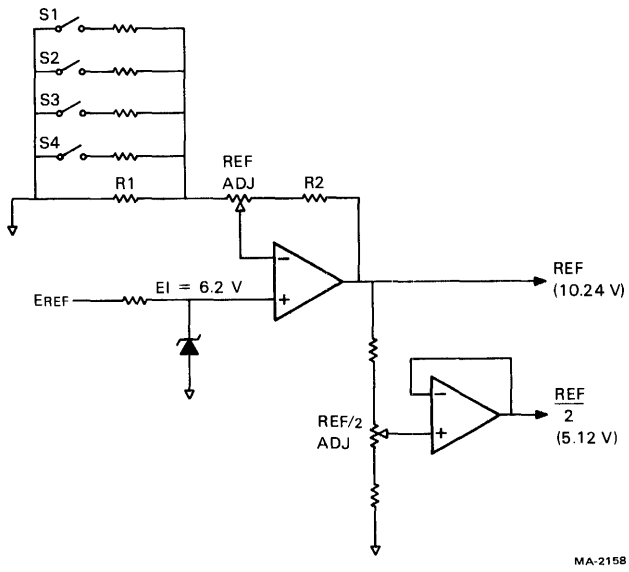


Figure 6-23-6 Reference Supply

The first amplifier circuit produces the REF voltage. For calibration purposes, switches 1-4 provide a coarse adjustment. (Switch 1 has the most significant effect.) The potentiometer provides fine adjustment.

REF/2 is produced by a voltage divider on the REF circuit output, with a potentiometer for adjustment and a voltage follower.

Charge-Pump Circuit

A separate power supply on the module provides +15 V and -5 V for all analog circuitry. The supply consists of a 50 kHz switching stage that drives two regulating charge pumps. The +15 V charge pump utilizes the 10.240 V reference supply as its reference.

Address Selection

The addresses for this module must be assigned according to the rules stated in Chapter 4. They are selected on the module by the 5-pole switch E21 shown in Figure 6-23-7. An example of one possible address selection is shown in Figure 6-23-8 to illustrate the use of this switch.

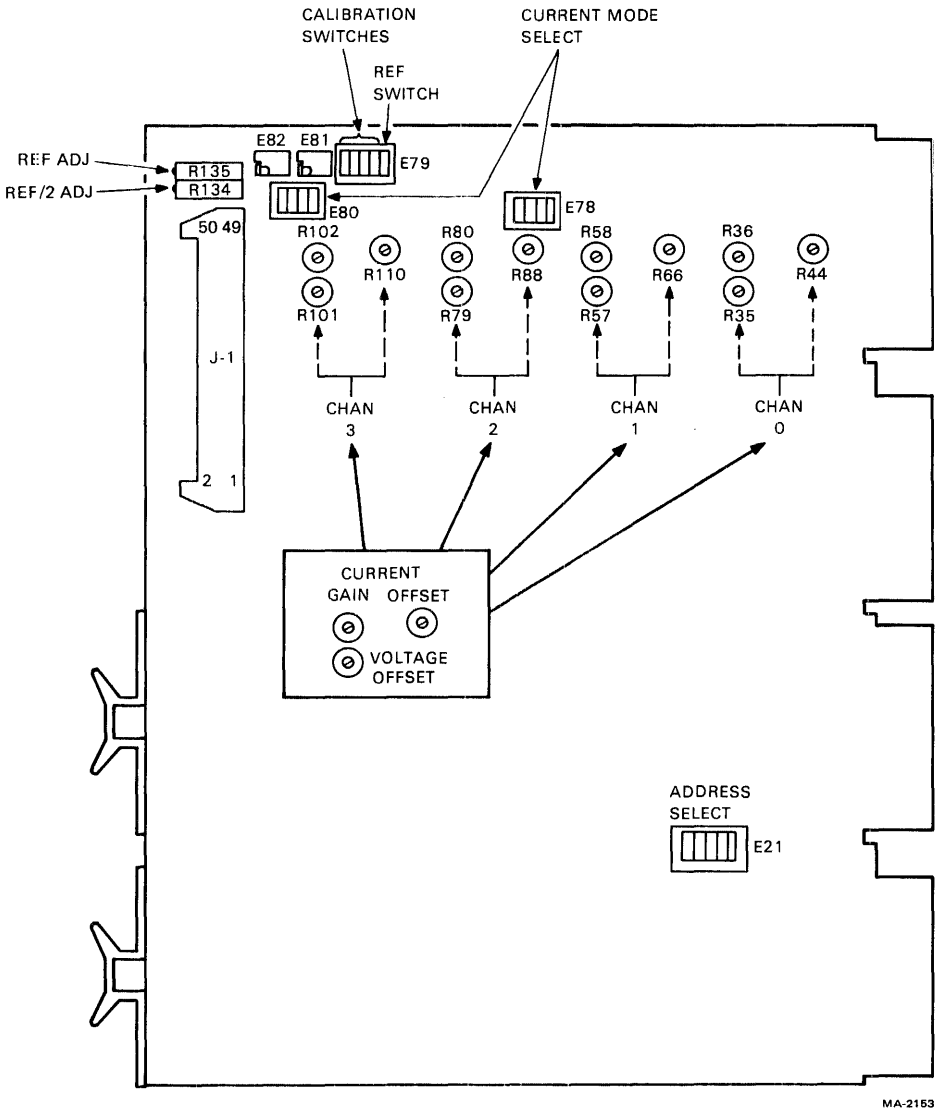


Figure 6-23-7 A630 DAC Module

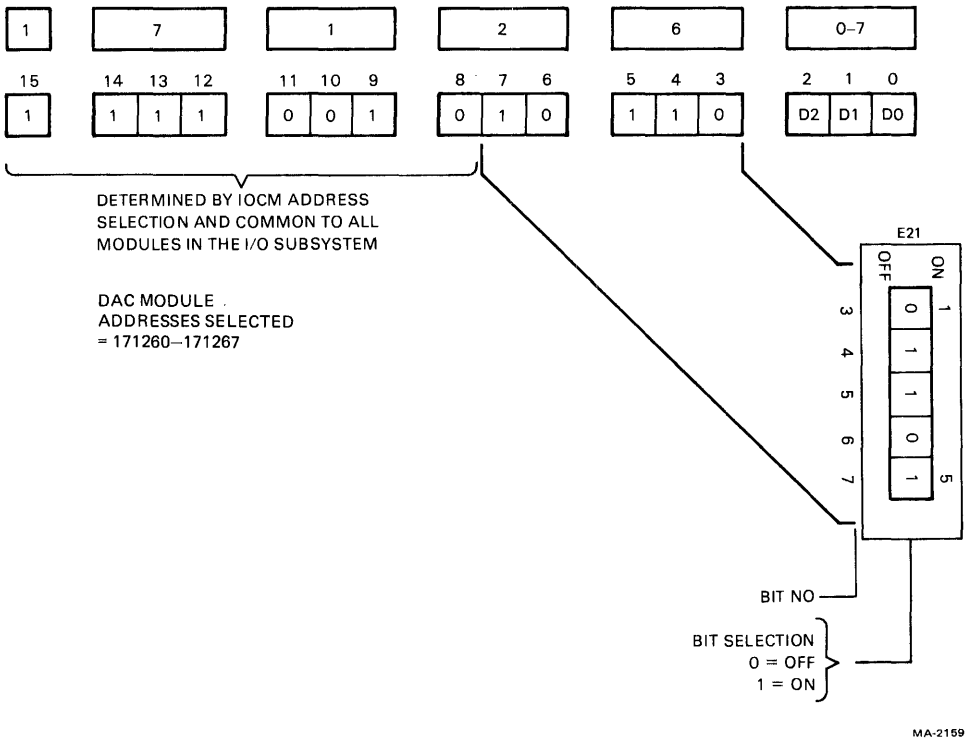


Figure 6-23-8 A630 Address Selection Example

Generic Code
The generic code of the A630 DAC module is 261.

Pin Connections
The A630 module pin connections for J1, the I/O cable connector, are listed in Table 6-23-4.

CALIBRATION

General
DAC module calibration is accomplished by means of diagnostics included with the I/O Subsystem. Instructions for using these diagnostics are included with the software package. Normally the DAC module is calibrated and ready for service when received by the customer; however, the customer may wish to change the current output option from the 4 to 20 mA range to the 0 to 20 mA range. (The module is shipped with the 4 to 20 mA range selected.) This necessitates recalibration of those outputs. If calibration is attempted without the diagnostic, be advised that the low end calibration point for the 0 to 20 mA current range is not zero but +1 LSB or 19.55 microamps.

Identification of adjustments and switches is provided in Figure 6-23-7. A careful study of this figure is recommended to avoid the frustration of selecting the wrong adjustment during the calibration procedure.

Table 6-23-4 Module A63Ø I/O Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1		2	
3		4	
5	Vout Chan Ø	6	Ground
7	Iout	8	Ground
9		1Ø	
11		12	
13	Vout Chan 1	14	Ground
15	Iout	16	Ground
17		18	
19		2Ø	
21		22	
23		24	
25		26	
27		28	
29		3Ø	
31		32	
33		34	
35		36	
37	Vout Chan 2	38	Ground
39	Iout	4Ø	Ground
41		42	
43		44	
45		46	
47	Vout Chan 3	48	Ground
49	Iout	5Ø	Ground

Details of the calibration switches are shown in Figure 6-23-9. These switches should be operated only during recalibration of the module.

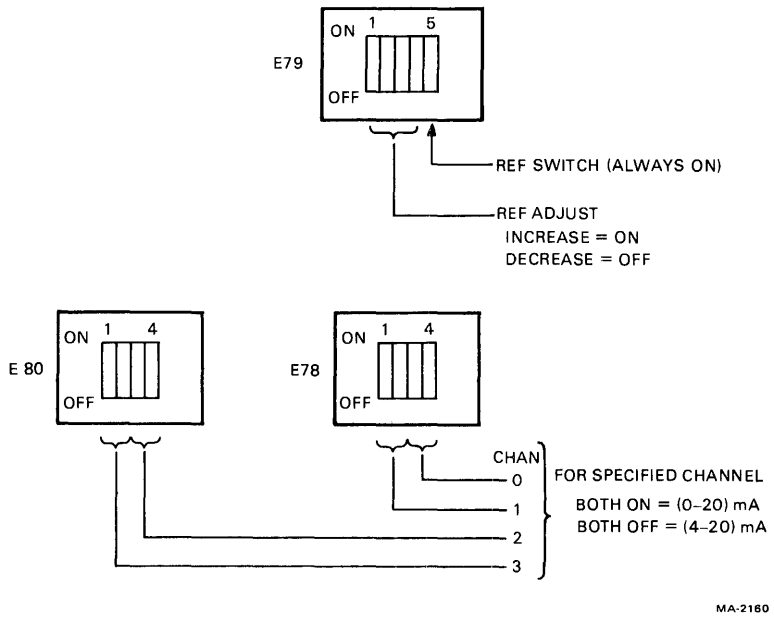


Figure 6-23-9 Voltage Reference and Current Mode Switches

Proper placement of the meter leads and precision resistor used during calibration is essential to achieve a valid calibration (Figure 6-23-10).

The A630 is accurately calibrated and sealed at the factory; it does not require recalibration at the time of installation. Field recalibration should only be attempted when a DAC malfunction is suspected. The malfunction should be verified by running the diagnostic before proceeding.

To ensure compliance with specifications, all test equipment used for calibration of the A630 must have been accurately and recently calibrated. In addition, personnel doing the calibration should be familiar with procedures for aligning precision analog equipment. If you are not sure of the foregoing, DO NOT ATTEMPT TO CALIBRATE THE A630. Factory calibration is probably better than that which you will be able to accomplish.

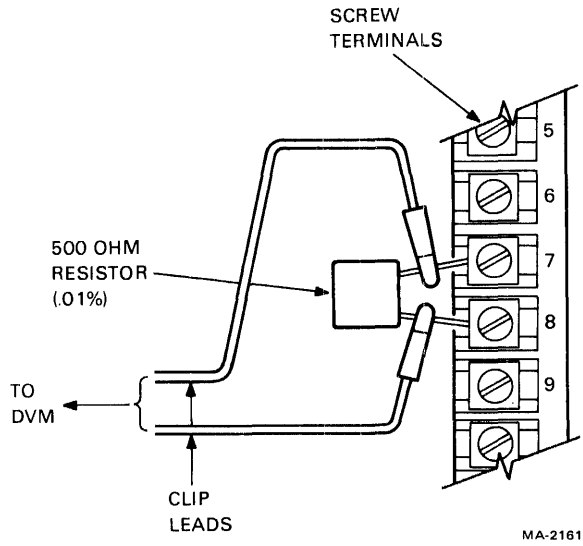


Figure 6-23-10 Calibration Resistor and Meter Lead Placement

Access to the adjustments and switches is permitted by putting the DAC on an extender module.

CAUTION
The system must be powered down before inserting or removing any module.

Equipment Needed

DVM	Weston Shlumberger model 443 or equivalent
Extender module	W904B
Resistor	500 ohm, 0.01 percent, 0.3 W, DEC part no. 13-09985-00

Screw Terminal Connections
The reader should refer to Chapter 3, Paragraph 3.8.5, for general field interface information. The A630 uses the BC40A screw terminal. Refer to Table 6-23-5 for this module's terminal configuration.

Table 6-23-5 Module A63Ø Screw Terminal Connections

BC4ØA Screw Terminal

Field Channel Number	Screw Terminal Number
	1
	2
	3
	4
ØØ Vout	5
ØØ Ground	6
ØØ Iout	7
ØØ Ground	8
	9
	1Ø
	11
	12
Ø1 Vout	13
Ø1 Ground	14
Ø1 Iout	15
Ø1 Ground	16
	17
	18
	19
	2Ø
Ø2 Vout	21
Ø2 Ground	22
Ø2 Iout	23
Ø2 Ground	24
	25
	26
	27
	28
	29
	3Ø
Ø3 Vout	31
Ø3 Ground	32
Ø3 Iout	33
Ø3 Ground	34

SPECIFICATIONS

Power Requirements

Voltage	Main supply: VS = 12 Vdc ± 2 Vdc Backup supply: 14 Vdc ≥ VB ≥ (VS-Ø.7) Vdc
Operating Current	36Ø mA maximum

NOTE
If the backup supply is implemented, total operating current is shared.
Main supply: 35Ø mA maximum
Backup supply: 1Ø mA maximum

Standby current (Backup Supply)	1Ø mA maximum
Number of channels	Four
Digital input	Natural binary, unipolar

Output Characteristics

General

Resolution	One part in 1Ø24 of full scale
Linearity	±1 LSB maximum between end points
Temperature drift	Gain: 2ØØ microvolt/degree C Offset: 2ØØ microvolt/degree C
Long term drift	Gain: 2 mV/initial 1ØØØ hr Offset: 2 mV/initial 1ØØØ hr
Total module output	8Ø mA maximum

Voltage

Output	Ø to 1Ø.23Ø V @ 15 mA maximum
Offset	Adjustable to zero on all outputs
Gain accuracy	4Ø mV maximum interchannel differential

Current

Output	Ø to 2Ø mA or 4 to 2Ø mA @ 1ØV maximum

Offset	Adjustable to zero or 4 mA on all outputs
Gain accuracy	Adjustable to 20 mA on all outputs
Protection	All outputs are protected from negative overvoltages by reference diodes to ground and from positive overvoltages by a 13 V zener clamp. The current outputs are additionally protected by a 1/16 A fuse.
Physical Characteristics	
Dimensions	Quad module, triple width, 8-1/2 inch length
Field connector	Cable type BC40A or customer-supplied 50 pin Berg
Environmental Characteristics	Complies with DEC STD 102 Class C. Operates in convection cooled environment up to 60 degrees C ambient.
Heat dissipation	13 Btu/hr maximum

FUNCTIONAL DESCRIPTION

The A631 module contains four group-isolated 12-bit digital to analog converters (DACs). It offers a choice of voltage or current outputs, and has the additional capability of retaining its output levels during a computer power failure. Provision is made for reading the outputs, resetting all outputs, and reading the generic code.

DETAILED DESCRIPTION

A simplified block diagram of the A631 is shown in Figure 6-24-1. At the left of the figure, the unit receives data and control signals from the D-bus. These signals are transmitted to the module's four DACs through optical couplers that isolate the analog circuits from the computer. Digital data bytes are converted to analog voltages or currents by the four DAC channels and are output through the field interface connector.

The figure also shows a RAM that stores the output data on the computer side of the isolation, a dc-to-dc converter that produces isolated dc power for the DAC circuits, a precision voltage reference, and a control section. The following paragraphs elaborate on individual sections of the block diagram and discuss the module's control sequences and data flow.

Register Formats

The four DACs of the A631 each occupy two byte addresses, a total of eight for the module. Data bytes written to the DAC registers are also written in a corresponding RAM location so that the data written to any DAC can be read by the processor.

A map of the RAM is shown in Figure 6-24-2. The figure shows that the eight LSBs, D(Ø-7), of DAC data occupy the low bytes in the DAC addresses. The four MSBs occupy the four low-order bits of the corresponding high bytes. The other four bits of the high bytes can be written to and read, but have no effect on the outputs. When the GBIT is asserted, all eight bytes contain the module's generic code.

Data Paths

The eight data lines, D(Ø-7), entering at the D-bus interface connector, go to the control section for address decoding, to the RAM for data storage, and to the data isolators for output to the DAC registers.

The data isolators are optical couplers that allow transmission of data from the computer to the DACs without any common mode connection between the two. The addressed DAC accepts the data and converts it to an analog voltage or current for transmission to the field through J1.

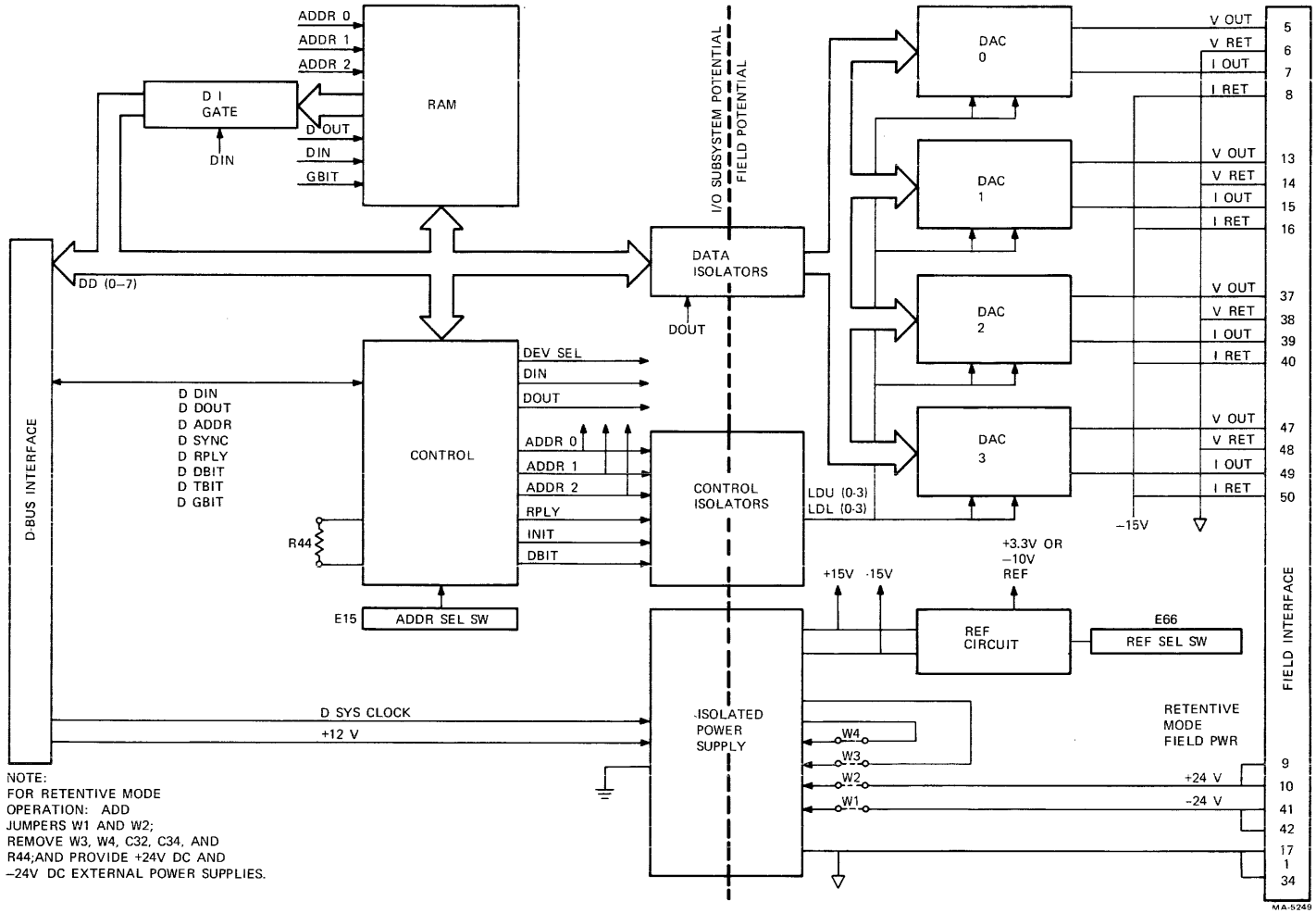


Figure 6-24-1 A631 DAC Block Diagram

Control Signals

Data transfers to and from the A631 module are initiated by the processor and are accomplished by DATAOs and DATAIs respectively. Bus protocol is the same as for other D-bus modules.

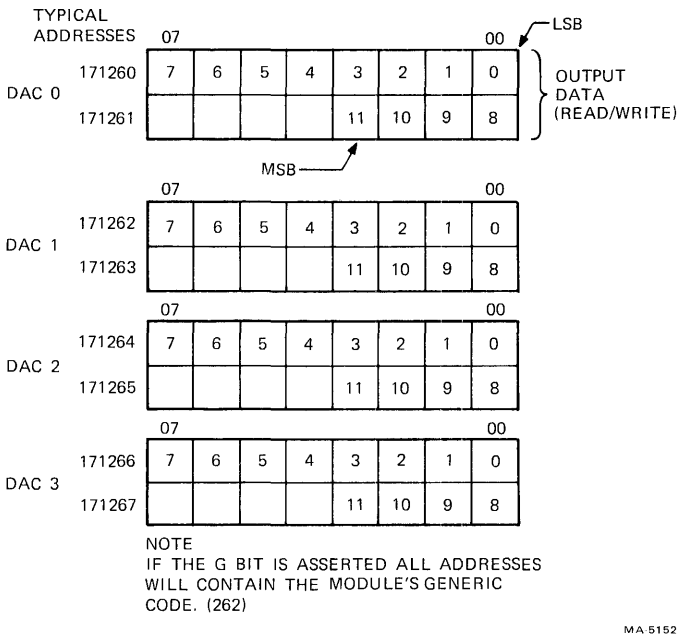


Figure 6-24-2 A631 DAC Data Registers

When the processor addresses any one of the A631 module's eight addresses, its MY ADDRESS signal is asserted, preparing the module for a data transfer. The module stores the lower 3 address bits as ADDRØ, ADDR1, and ADDR2. These signals are used to select the proper RAM location. They are also decoded on the field side of the isolators to produce one of the LDU (Ø-3), or LDL (Ø-3) signals. These signals strobe new data into the addressed DAC register at the proper time in the DATAO cycle. When addressing is completed, the module is ready for D DIN or D DOUT, according to whether the program is reading or writing data.

Data is written to the module's RAM at the same time data is written to a DAC register. When the program reads a DAC's output status, it receives data from the RAM, which normally contains the latest data written to any DAC register.

When the program sets the TBIT in the CSR of the IOCM, it can then exercise the module by writing and reading into and out of its RAM registers without affecting the current or voltage outputs. Setting the CBIT or DBIT resets all the module's DAC outputs to zero unless the retentive mode is implemented, but does not affect the contents of its RAM registers. Current and voltage outputs remain at zero when the CBIT and DBIT are cleared, until new data is written to them. Note that neither the CBIT, nor the DBIT, nor INIT will clear the module's memory. In fact, the only way to clear the RAM is to write zeros in it.

DAC Circuit

All four A631 DAC circuits are identical. A block diagram of one of them is shown in Figure 6-24-3. Note that all data and control signals are transmitted through optical isolators, as this part of the module is isolated from the computer.

The 12-bit data input to the DAC is in two bytes. The high byte, which contains the four MSBs, is written first and stored in the holding register. The low byte, which contains the eight LSBs, is written next. When the low byte is written, it and the four MSBs in the holding register are simultaneously loaded into the output register, which drives the DAC. All twelve bits are, therefore, input to the DAC at once. Note that there is a separate holding register for each DAC channel, therefore, operation of the four DAC channels is totally independent.

Digital to analog conversion of the 12-bit DAC input is accomplished by a single integrated circuit that contains a current switching R-2R ladder. Its output is a current that is proportional to the sum of the weights of the asserted bits of its 12-bit input.

The output of the DAC integrated circuit drives a separate operational amplifier that converts the output current of the ladder network to a proportional voltage. This amplifier uses a precision feedback resistor that is included in the DAC integrated circuit for this purpose. The output of this amplifier is the DAC channel's voltage output. The voltage amplifier output is also input to a second circuit that provides the DAC channel's current output. Both outputs are connected to the module's field interface connector.

Although separate voltage and current outputs are provided, they cannot be used simultaneously. When the module is calibrated, the DAC reference (see below) is configured according to whether the DAC is to be calibrated for voltage or current output. Since, the reference selection is made for all four DACs, they must all be used in the same (current or voltage) mode.

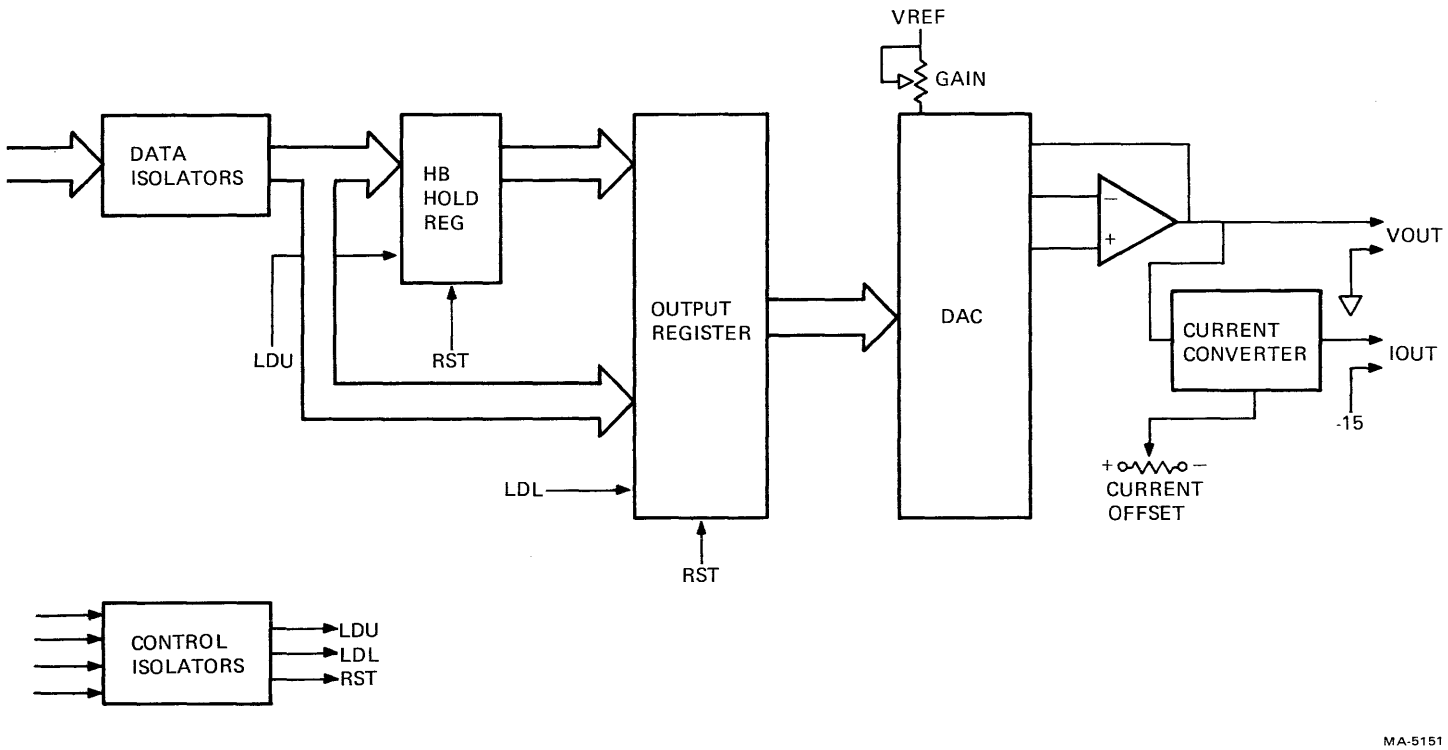


Figure 6-24-3 DAC Circuit

Conversion Bit Weights
A voltage or current output is the sum of the binary weights of the asserted bits in the 12-bit output data register. For a voltage output, the value of the LSB is 2.5 mV (Ø.ØØ25V), and the output can be any multiple of that value from zero (no bits asserted) to a full scale value of 1Ø.2375 V (all bits asserted = 2.5 mV x 4Ø95).

For example, if an analog output of 2.6Ø5 volts is required, the necessary 12-bit binary output word is computed as follows:

$$\frac{E\ out}{LSB} = \frac{2.6Ø5}{2.5 \times 1Ø^{-3}} = 1Ø42 \text{ decimal}$$

$$= Ø1Ø\ ØØØ\ Ø1Ø\ Ø1Ø \text{ binary}$$

The DAC current output LSB value is 5 microamps, and it has a full scale range of zero (no bits asserted) to 2Ø.475 mA (all bits asserted). Table 6-24-1 lists the weights of all the bits for both voltage and current outputs.

Table 6-24-1 Bit Values

Bit No.	Weight	
	Voltage Outputs (mV)	Current Outputs (microamps)
Ø	2.5	5
1	5	1Ø
2	1Ø	2Ø
3	2Ø	4Ø
4	4Ø	8Ø
5	8Ø	16Ø
6	16Ø	32Ø
7	32Ø	64Ø
8	64Ø	128Ø
9	128Ø	256Ø
1Ø	256Ø	512Ø
11	512Ø	1Ø24Ø
Total (All Bits Asserted)	1Ø237.5	2Ø475

DC Power and Operating Modes
The analog circuits of the A631 module require ±15 Vdc. These voltages are not available on the D-bus, and are supplied by a regulator circuit, the input of which is either the on-board dc-dc converter, or external ±24 Vdc power supplies furnished by the user.

If, as is normally the case, the on-board dc-dc converter provides the dc power, then when computer power is turned off, the analog circuits (i.e., the DAC output channels) no longer function.

If it is desired to have the DACs retain their existing outputs during a computer power shut-down, the user can implement the A631's retentive output option.

To implement the retentive mode, dc power for the DAC circuits must be provided by user-furnished +24 Vdc external power supplies (Figure 6-24-4). Jumpers W1 and W2, (shown in the figure) are added to connect the external power; jumpers W3 and W4, and capacitors C32 and C42, are removed to disconnect and disable the module's dc-dc converter. Not shown in the figure is a resistor (R44) in the control section that must be removed to disable the DBIT and INIT functions. These functions must be disabled because when the computer senses that power is being removed, it asserts INIT, which would clear the DAC outputs, thus defeating the purpose of the retentive option.

If the user wants the computer to reset the DAC outputs when its power goes down, but has an application that requires minimum noise, he can disable the A631's on-board dc-dc converter, and provide his own low-noise power supplies. This is accomplished by making the changes as described above for the retentive option, except that resistor R44 is left in the circuit.

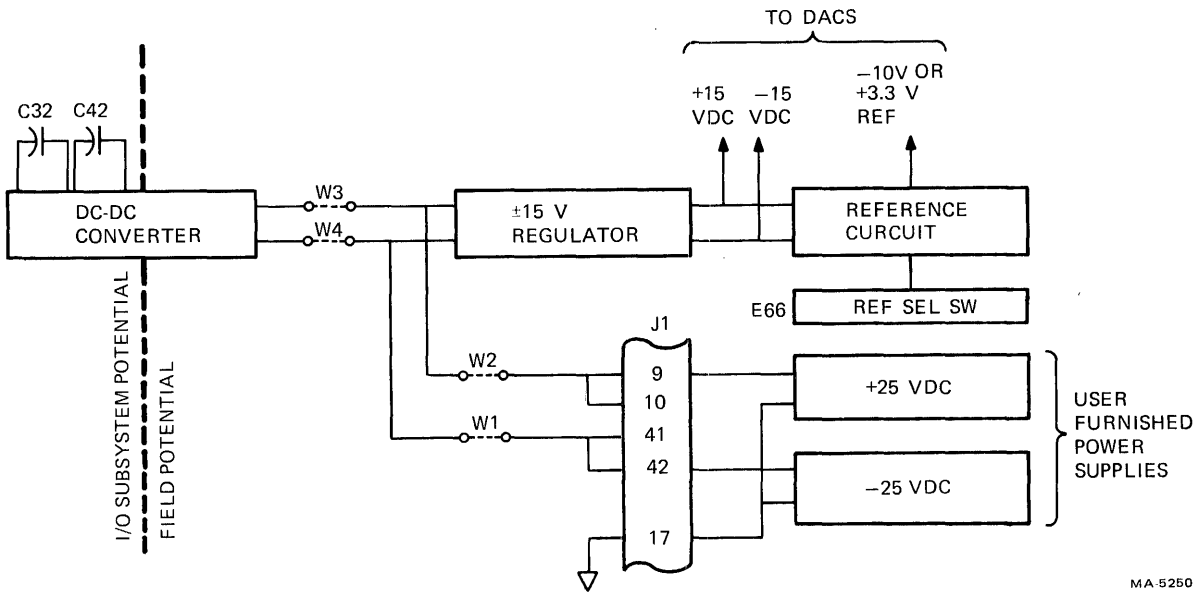


Figure 6-24-4 Isolated Power Options

Reference Circuit

The A631 includes a stable reference for the DAC circuits (Figure 6-24-5). This circuit provides -1Ø Vdc when the DAC's voltage outputs are used, or +3.3 Vdc when the current outputs are used. The input to the circuit is +1Ø V which is provided by a precision reference. This is followed by an operational amplifier circuit, the output of which is the appropriate reference level. Changing the reference from voltage to current mode is done before calibration with switches. The switches reconfigure the amplifier circuit from an inverting amplifier for the -1Ø V (voltage) mode to a voltage divider and voltage follower for the +3.3 V (current) mode. Switch settings are discussed under "Calibration".

Address Selection

The addresses for this module must be assigned according to the rules stated in Chapter 4. They are selected on the module by the 5-Pole switch E15 shown in Figure 6-24-6. An example of one possible address selection is shown in Figure 6-24-7 to illustrate the use of this switch.

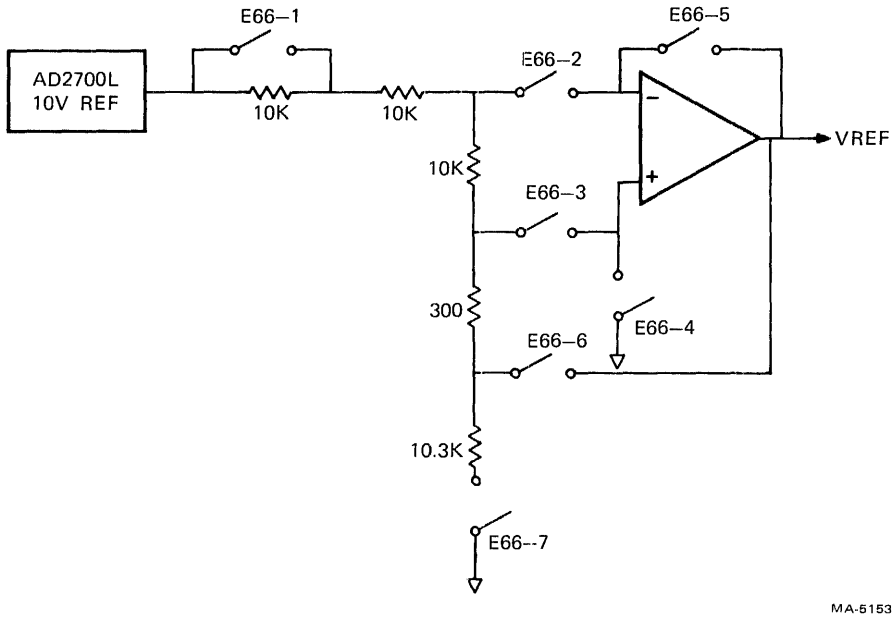


Figure 6-24-5 Reference Circuit

Generic Code

The generic code of the A631 DAC module is 262.

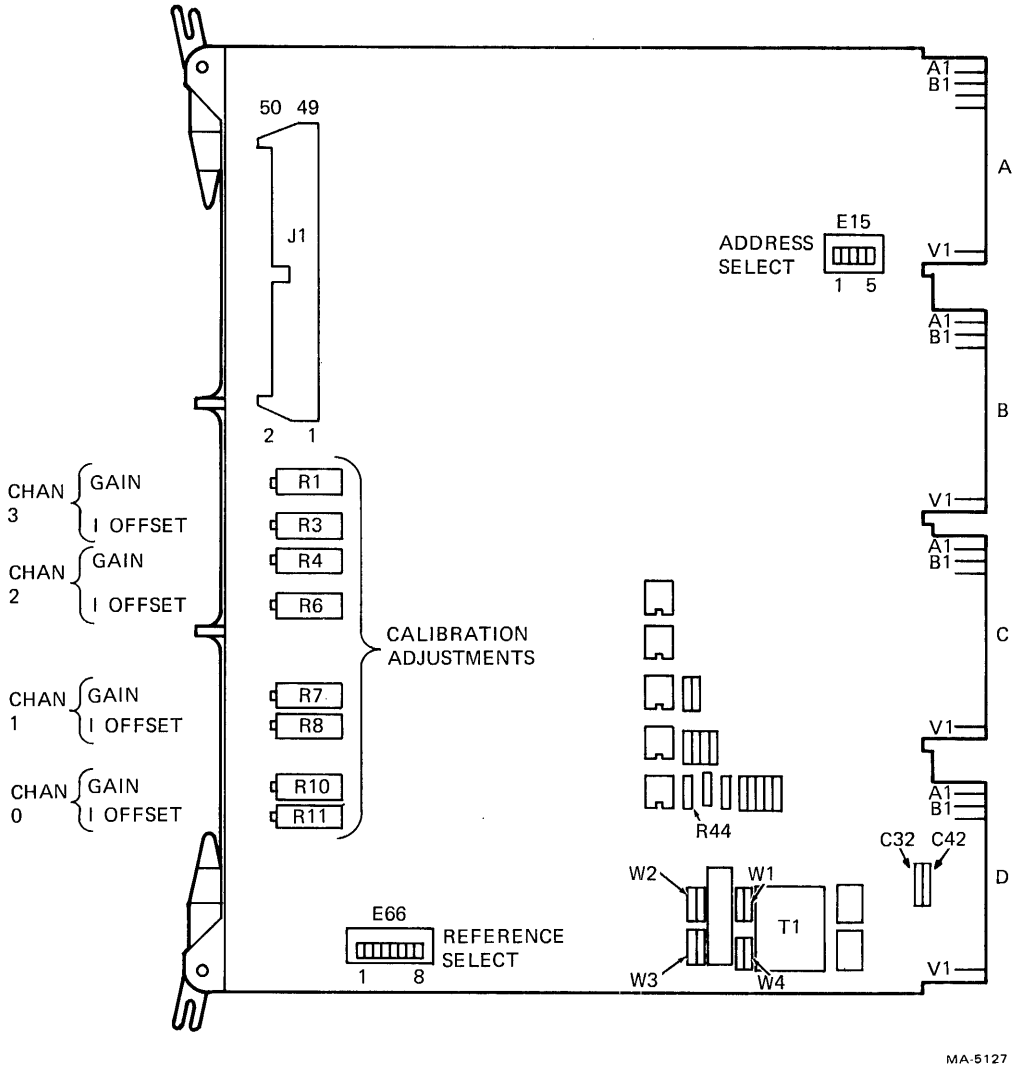


Figure 6-24-6 A631 DAC Module

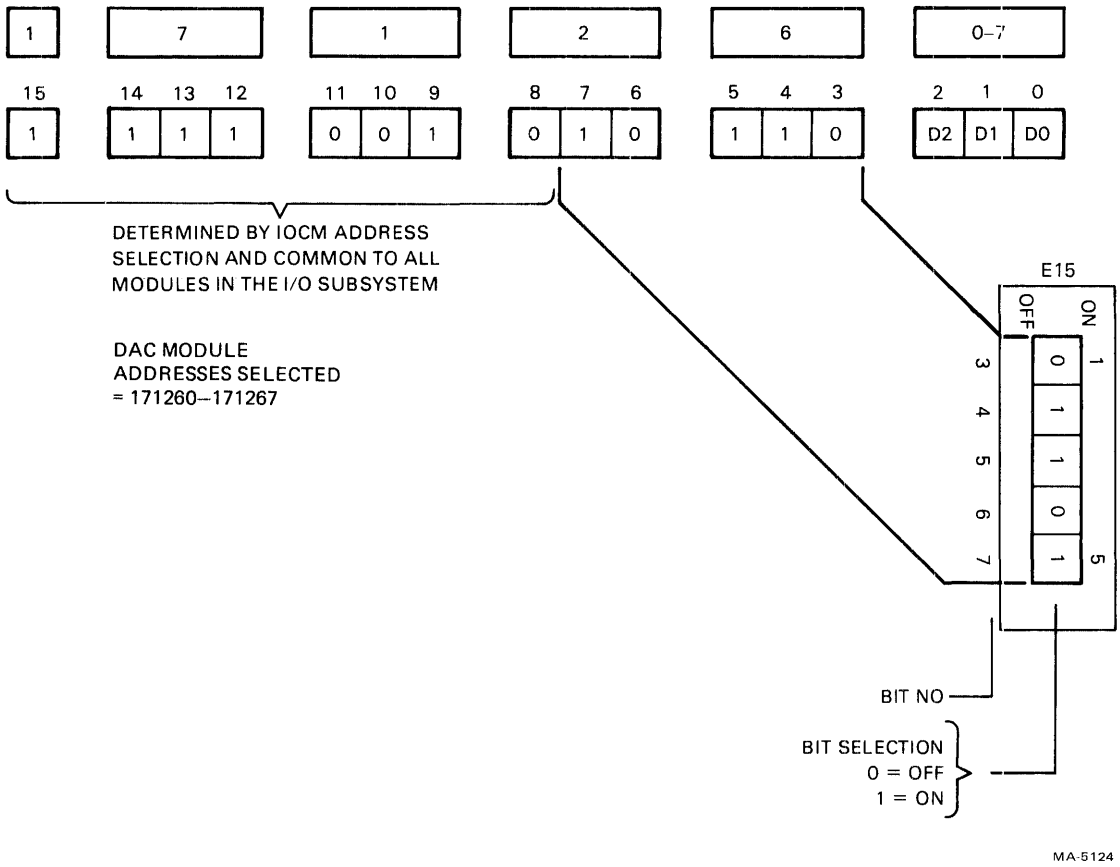


Figure 6-24-7 A631 Address Selection Example

Screw Terminal Connections

The reader should refer to Chapter 3, Paragraph 3.8.5, for general field interface information. The A631 uses the BC40A screw terminal assembly. Refer to Table 6-24-2 for this module's screw terminal configuration.

Pin Connections

The A631 module pin connections for J1, the I/O cable connector, are listed in Table 6-24-3.

Table 6-24-2 Module A631 Screw Terminal Connections

BC40A Screw Terminal Assembly

Field Channel Number	Screw Terminal Number
	1
	2
	3
	4
00 Vout	5
00 Vreturn	6
00 Iout	7
00 Ireturn	8
Field +24 Vdc*	9
Field +24 Vdc*	10
	11
	12
01 Vout	13
01 Vreturn	14
01 Iout	15
01 Ireturn	16
Field Power return*	17
Field Power return*	18
	19
	20
02 Vout	21
02 Vreturn	22
02 Iout	23
02 Ireturn	24
Field -24 Vdc*	25
Field -24 Vdc*	26
	27
	28
	29
	30
03 Vout	31
03 Vreturn	32
03 Iout	33
03 Ireturn	34

* For retentive mode only - user furnished

Table 6-24-3 Module A631 I/O Connections

Module I/O Connector Pin	Field I/O	Module I/O Connector Pin	Field I/O
1		2	
3		4	
5	Vout Chan Ø	6	Vreturn Chan Ø
7	Iout	8	Ireturn
9	Field +24 Vdc*	1Ø	Field +24 Vdc*
11		12	
13	Vout Chan 1	14	Vreturn Chan 1
15	Iout	16	Ireturn
17	Field Power Return	18	Field Power Return
19	↑	2Ø	↑
21	|	22	|
23	|	24	|
25	|	26	|
27	|	28	|
29	|	3Ø	|
31	|	32	|
33	↓ Field Power Return	34	↓ Field Power Return
35		36	
37	Vout Chan 2	38	Vreturn Chan 2
39	Iout	4Ø	Ireturn
41	Field -24 Vdc*	42	Field -24 Vdc*
43		44	
45		46	
47	Vout Chan 3	48	Vreturn Chan 3
49	Iout	5Ø	Ireturn

* For retentive mode only - user furnished.

APPLICATION NOTES

1. The current outputs of the A631 cover the range of Ø-2Ø mA. If it is desired to use this module as the source of an industry-standard 4-2Ø mA signal, the 4 mA offset must be provided by the application software. While this approach decreases the DAC's resolution by 2Ø percent, it has the advantage of protecting the process from certain types of computer failures. For example, if the computer fails in a way in which the I/O subsystem is reset, the DAC outputs will go to zero (except in retentive mode). The process then interprets this condition (DAC output less than 4 mA) as an error, and takes appropriate fail-safe action.

2. If the user requires retentive outputs (i.e., outputs that are unaffected by a computer power failure), he must provide ±24 Vdc power to the module. He must also add jumpers W1 and W2, remove jumpers W3 and W4, remove capacitors C32 and C42, and remove R44. The location of these components is shown in Figure 6-24-6. Note that high frequency noise on the outputs of the user-furnished ±24 Vdc power supplies will be reflected to some extent in the DAC outputs. For best results these power supplies should be the linear regulated type.

3. When the retentive feature of the A631 module is implemented, the user must also implement whatever circuit changes may be necessary to update the system IOCM. That is, the IOCM circuit must be the revision level listed below or later.

IOCM	Circuit Schematic Rev. Level
M7958	H
M7959	A*
M8719	C

* All versions of the M7959 are usable without modification.

Configuration Constraints

If the retentive feature of the A631 module is implemented, the module's current requirements are partially served by the external field power supplies, and there are no system constraints imposed by the A631. In addition, use of A631s in the voltage mode does not constrain the system. However, if the retentive feature is not implemented, each A631 module, when used in the current mode, can draw up to 450 mA from its +12 V power supply. If multiple current-mode A631 modules are used in a single chassis (or in two chassis powered by the same power supply), there exists the possibility of overloading that power supply, causing improper operation of the subsystem. This situation is avoided by observing the following configuration guidelines for each type of chassis.

H334-E and H334-J Chassis - Each of these chassis contains its own H7872 power supply. Maximum current for this supply is 4 Amperes. Overloads are avoided by observing one of the following guidelines.

1. Leave one slot unused. All nine remaining slots can then be filled with current-mode A631 modules. The unused slot must have an M9019 continuity module, unless it is the last slot in the I/O subsystem.

2. Use five or fewer current-mode A631 modules; the remaining slots can be used for any other module types (including voltage-mode A631 modules).

3. Use 6, 7, or 8 current-mode A631 modules, and make certain that the remaining current capacity of the H7872 power supply is not exceeded by computing the total current requirements of the modules used in the remaining slots.

H334-A, H334-B, and H334-X Chassis - These chassis are powered in pairs by the H787Ø power supply (Chapter 1, Paragraph 3.3.1; and Chapter 3, Table 3-1). The maximum current for the +12 V portion of this supply is 6 A. Since it usually powers two chassis, the current requirements of all modules in both chassis must be computed to make certain that multiple current-mode A631 modules do not overload it.

H333-A and H333-B Chassis - Each of these chassis is powered by a separate H787Ø power supply. Although this chassis accommodates only eight I/O modules, its +12 V power supply also powers the IOCM and any other LSI-11 modules that are present. The user must compute current requirements for all these modules, and make certain that the use of multiple current-mode A631 modules does not overload the +12 V power supply. In addition, the total power delivered by the power supply must be calculated (both +5 V and +12 V supplies) and determined not to exceed 122 watts.

Calibration

The DAC module is accurately calibrated at the factory and is ready for service in the voltage mode when received by the user. The customer may wish to change from the voltage to the current output option. This necessitates recalibration of the module.

When calibration is necessary, it is accomplished by means of diagnostics included with the I/O subsystem. Instructions for using these diagnostics are included with the software package.

Identification of adjustments and switches is provided in Figure 6-24-6. A careful study of this figure is recommended to avoid selecting the wrong adjustment during the calibration procedure.

Details of the reference voltage selection switches are shown in Figure 6-24-8. These switches should be operated only when changing the DAC outputs from voltage to current or vice versa.

Proper placement of the meter leads and precision resistor used during current mode calibration is essential to achieve a valid result, and is illustrated in Figure 6-24-9.

To ensure compliance with specifications, all test equipment used for calibration of the A631 must have been accurately and recently calibrated. In addition, personnel doing the calibration should be familiar with procedures for aligning precision analog equipment. If you are not sure of the foregoing, DO NOT ATTEMPT TO CALIBRATE THE A631. Factory calibration is probably better than that which you will be able to accomplish.

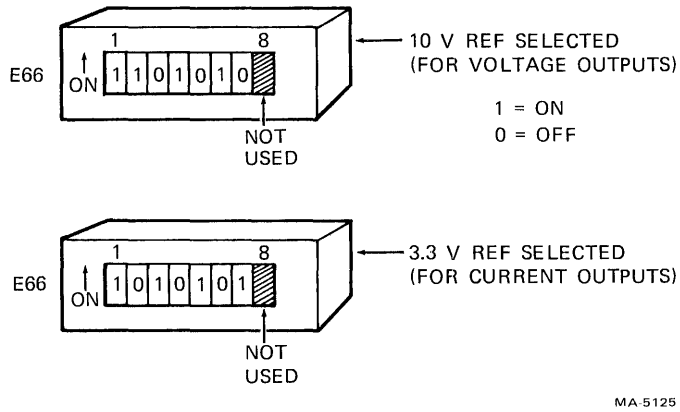


Figure 6-24-8 Reference Voltage Selector Switches

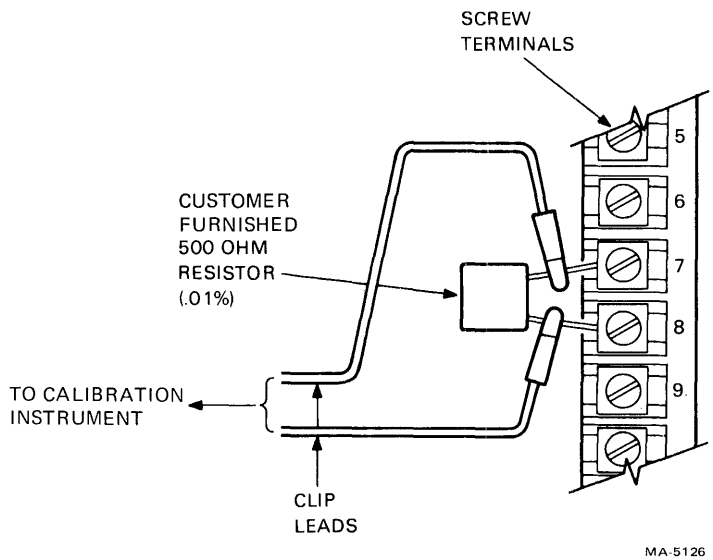


Figure 6-24-9 Resistor and Meter Lead Placement For Current Mode Calibration

CAUTION

The system must be powered down before inserting or removing any module.

Equipment Needed

Resistor	500 ohm, 0.01 percent, 0.3 W, DEC part no. 13-09985-00
Voltage reference	EDC model MV105G or equivalent

SPECIFICATIONS

Power Requirements From I/O Subsystem

Voltage	Main supply: VS = 12 Vdc + 2 Vdc - 1 Vdc Backup supply: VB = 14 Vdc $\geq$ VB $\geq$ (VS-0.7) Vdc
Current:	
Current mode:	Main supply: 450 mA maximum Backup supply: 10 mA maximum Total: 460 mA maximum
Voltage mode:	Main supply: 350 mA maximum Backup supply: 10 mA maximum Total: 360 mA maximum
Retentive mode:	Main supply: 90 mA maximum Backup supply: 10 mA maximum Total: 100 mA maximum

NOTE

If the backup supply is not implemented, the main supply provides the total currents listed above.

Power Requirements From Optional Field Power (Retentive Mode)

Voltage:	+ 24 Vdc $\pm$ 3 percent - 24 Vdc $\pm$ 3 percent
Current:	
Current mode:	+ 24 V supply: 100 mA maximum - 24 V supply: 150 mA maximum
Voltage mode:	+ 24 V supply: 120 mA maximum - 24 V supply: 40 mA maximum

Output Characteristics

Voltage Output

Range:	10.24 V
LSB:	2.5 mV
Max current output:	±5 mA
Gain accuracy:	Adjustable
Gain temp. coefficient:	30 ppm of full scale/°C maximum
Offset:	±1/2 LSB maximum
Offset temp. coefficient:	±50 microvolts/°C maximum
Integral nonlinearity:	±1/2 LSB maximum, over temp. range
Differential non-linearity:	1 LSB maximum, over temp. range, monotonic over temp. range
Slew rate:	0.1V/microsecond (with a load of 2 kohms in parallel with 150pf)
Output noise: (peak to peak with 2 kohm load)	2mV from 10 Hz to 10 kHz 20mV from 10 Hz to 100 kHz 150mV from10 Hz to 1 MHz
Capacitive loading:	0.1 microfarad will not cause instability but will degrade settling time
Settling time: (to 0.01% of final value)	150 microseconds (with a load of 2 kohms in parallel with 150 pf)
Channel interaction:	1/2 LSB maximum change in output over the temperature range, with a full-scale change in all other outputs

Current Output

Range:	0-20.48 mA
LSB:	5 microamps
Maximum load resistance:	500 ohms
Gain accuracy:	Adjustable
Gain temp. coefficient:	30 ppm of full scale/°C maximum
Offset:	Adjustable
Offset temp. coefficient:	0.4 microamps/°C maximum
Integral nonlinearity:	±1/2 LSB maximum, over temp. range
Differential nonlinearity:	1 LSB maximum, over temp. range, monotonic over temp. range

Slew rate:	Ø.2 mA/microsecond (with a load of 5ØØ ohms in series with 1ØØØ micro-henrys
Output noise: (peak to peak with a 5ØØ ohm load)	4 microamps from 1Ø Hz to 1 kHz 4Ø microamps from 1Ø Hz to 1ØØ kHz 3ØØ microamps from 1Ø Hz to 1 MHz
Settling time: (to Ø.Ø1% of final value)	1ØØ microseconds (with a load of 5ØØ ohms in series with 1ØØØ micro-henrys)
Channel interaction:	1/2 LSB maximum change in output over the temperature range, with a full scale change in all other outputs.

Isolation

Isolation voltage:	1ØØØ Vdc 1ØØØ Vac peak
Common mode source:	2ØØ VA for UL approval
Common mode rejection ratio:	12Ø dB from dc to 6Ø Hz 7Ø dB at 1Ø kHz 7Ø dB at 1ØØ kHz 6Ø dB at 1 MHz 3Ø dB at 1Ø MHz

Physical Characteristics

Dimensions:	Quad module, triple width, 8-1/2 inches long
Field connector:	Cable type BC4ØA or customer-supplied 5Ø pin Berg

Environmental Characteristics	Complies with DEC STD 1Ø2 Class C. Operates in convection cooled environment up to 6Ø°C ambient.
Heat dissipation:	22 BTU/hr maximum

FUNCTIONAL DESCRIPTION

The BC40L is a more versatile alternative to the BC40A screw terminal assembly. In addition to the standard screw terminals, it offers a convenient means of inserting signal conditioning circuit components into the I/O field interface. It makes possible the addition of series and/or parallel components to each interface circuit. Typical uses include the addition of pull-ups, attenuators, filters, etc.

DETAILED DESCRIPTION

The BC40L (Figure 6-25-1) is a specially designed screw terminal assembly. It is similar to the BC40A in that it has a screw terminal field interface, and a Berg connector module interface. With the exception of terminal 17, it makes the same electrical connections between these two. It is dissimilar to the BC40A in that it is larger (23.4 X 32.5 cm = 9.2 X 12.8 in), has a Berg connector I/O interface (can be connected directly to the ATR16), and has turret terminals for quick and easy installation of user designed signal conditioning circuits.

Each printed circuit conductor path from the field interface to the module interface is broken in two places. These breaks are bridged with wire jumpers (zero ohm resistors) that can be removed easily to allow the substitution of other series components (Figure 6-25-2 shows the schematic of two of those circuit paths.) Turret terminals are provided at these breaks so that the new series components can be mounted easily. In addition to these terminals are others that connect to two independent common potential buses (V_X and V_{XRET}) as well as some that are not connected to anything. The V_X and V_{XRET} terminals provide convenient power connections for devices such as pull-ups or zener diodes. The uncommitted terminals are provided so that they can be used as convenient tie points in more complex circuits.

INSTALLATION

The BC40L is the same height as, but wider than, a BC40A; and is installed in an H332 chassis in the same manner as a BC40A. It merely extends deeper into the chassis. Mounting hardware and plastic covers are provided. The plastic covers are for the safety of operating personnel and must be installed after field wiring is completed. The proper way to install the I/O module cable and the ATR16 cable (if used) is shown in Figure 6-25-3.

APPLICATION NOTES

General

BC40L screw terminal and Berg connector (J1) inputs are parallel. The Berg connector input is provided to accommodate an ATR16 cable which normally plugs directly into an A157 or A020. This does not cause any change in the field wiring to the ATR16 for these devices. It remains the same as listed in the ATR16 section of this manual.

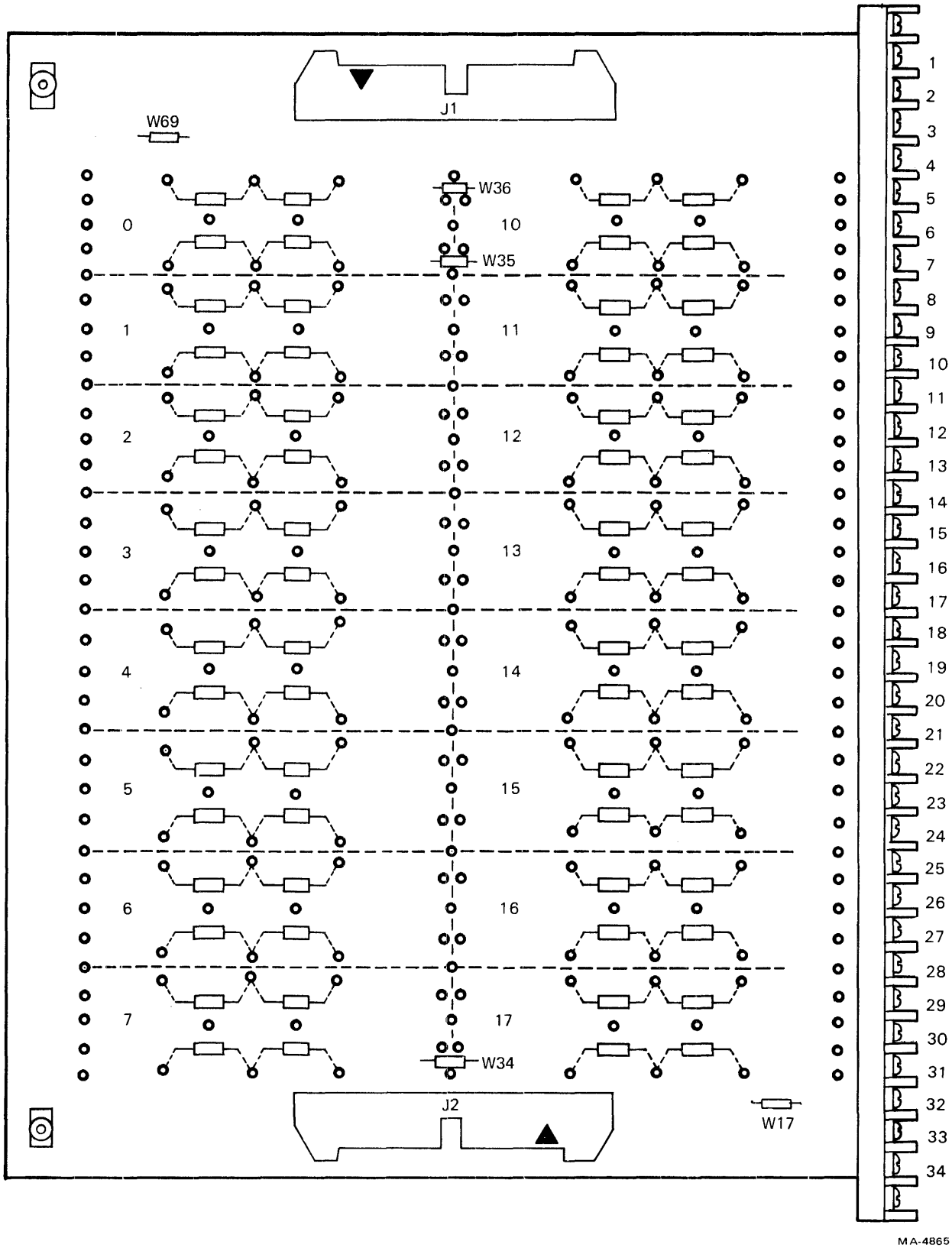


Figure 6-25-1 BC40L Screw Terminal Assembly

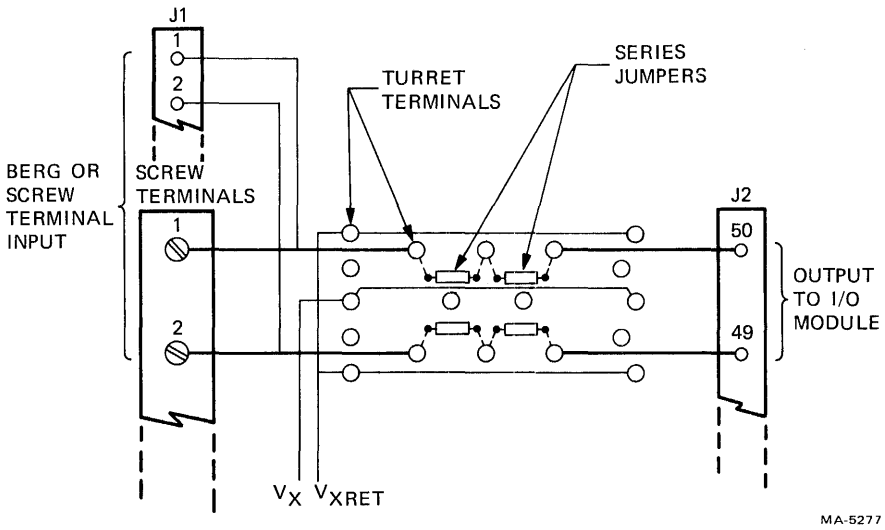


Figure 6-25-2 BC40L Circuits with Jumpers

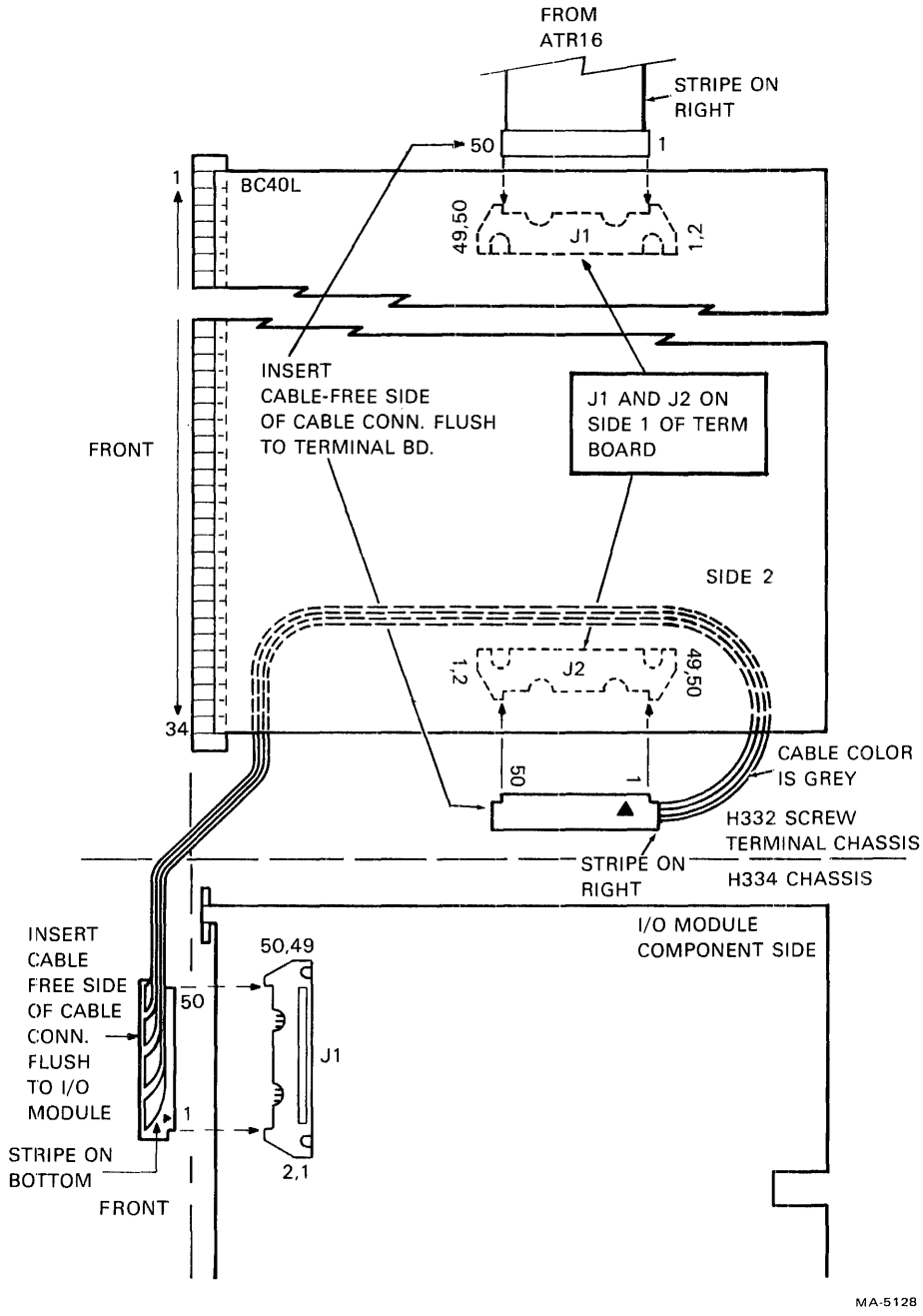


Figure 6-25-3 BC40L Cable Installation

If the interfacing module is not an A157 or AØ2Ø, then power is not available from the module, and any power requirements of the signal conditioning circuits must be met with a user furnished external power supply connected to screw terminals 17 and 18. In most cases, this will require at least the removal of jumper W17 to isolate screw terminal 17. This is because, in most cases the corresponding module terminal is common. It may also require the removal of jumpers W34 and W35, depending on whether or not the user needs to isolate his field circuit ground from the computer ground. The user must consider each type of module interface individually.

I/O Connections

Except as noted above for terminals 17 and 18, field wiring configurations for the BC4ØL screw terminals are the same as for the BC4ØA, and are listed for the individual modules elsewhere in this chapter. Some of the more common ones are grouped together in Table 3-2 of Chapter 3.

When using the BC4ØL screw terminals, all field wire connections are the same as when using a BC4ØA with the possible exception of terminals 17 and 18. The status of these terminals depends on several factors and is best visualized by referring to Figure 6-25-4. This figure is a much abreviated schematic of the BC4ØL, but it illustrates the key points (a complete schematic is included in the BC4ØL print set).

The important electrical difference between the BC4ØL and the BC4ØA is that screw terminal 17 and its connection to the module interface, J2, are isolated from screw terminal 18. As the figure shows, the circuits connected to screw terminals 17 and 18 have several wire jumpers. These jumpers allow some flexibility in the use of terminals 17 and 18.

For example, if the interfacing module is an A157 or AØ2Ø, and the signal conditioning circuits being added require power, there are two power options. First, the user can provide an external power supply for these circuits and connect it to the common potential buses via screw terminals 17 and 18. In this case, jumpers 17, 34, and 35 must be removed to isolate the voltage on these buses from the module and the ATR16.

Second, if +12V is suitable for the signal conditioning circuits, and current requirements are modest, then the +12V ATR16 power from the module can be used for the BC4ØL common potential buses. This is done by leaving the jumpers intact and turning on the appropriate module switch (i.e., E3Ø-4 on the A157, or E6-1Ø on the AØ2Ø). Note that this can be done whether an ATR16 is being used or not.

CAUTION

Maximum additional loads on the +12V module power from the A157 and AØ2Ø modules must not exceed 95 and 145 mA respectively. Using the +12V module power option for loads greater than this will cause improper operation of the subsystem.

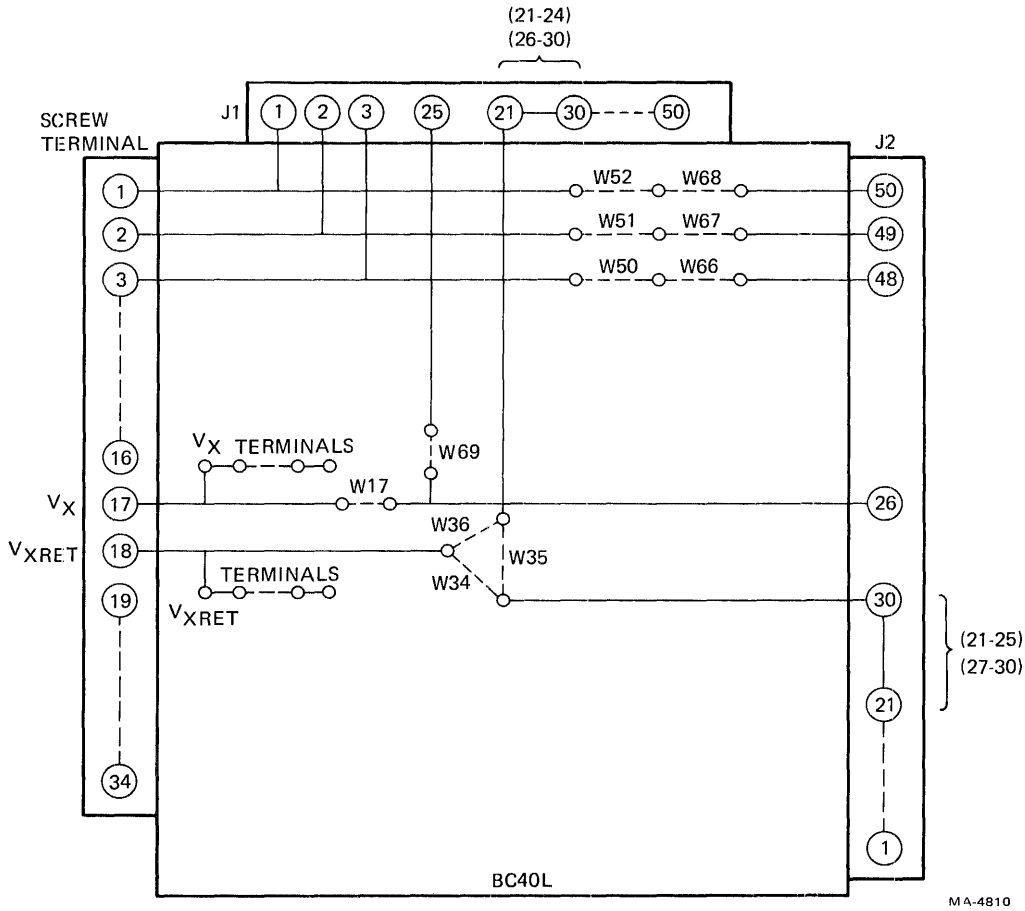
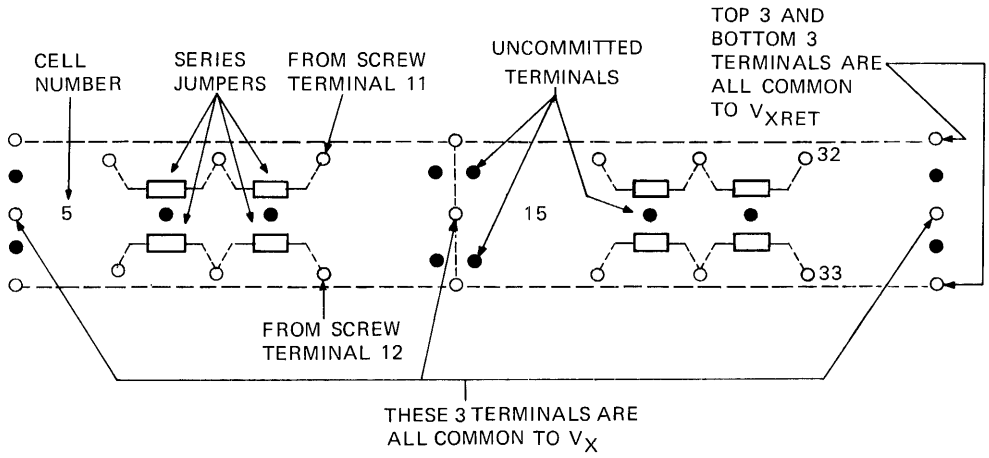


Figure 6-25-4 BC40L Simplified Schematic

Channel Number and Component Identification
Dotted lines have been included in Figure 6-25-1 to emphasize the iterative patterns of terminals, components and field channel numbers. Part of Figure 6-25-1 is repeated in Figure 6-25-5 which identifies these items and explains the significance of markings on the printed circuit board. Table 6-25-1 correlates cell numbers, screw terminal numbers, and Berg connector pin numbers.

Application Examples
Schematics and component layouts of ten circuits that might be implemented using the BC40L are shown in Figures 6-25-6 and 6-25-7.



NOTES

1. EACH TERMINAL GROUP CELL HAS SIX TERMINALS (SHOWN BLACK) THAT ARE NOT CONNECTED TO ANYTHING. THEIR PURPOSE IS TO SERVE AS CONVENIENT CIRCUIT NODE TIE POINTS.

2. EACH CELL IS IDENTIFIED BY A NUMBER ON THE PRINTED CIRCUIT BOARD, AND IS ASSOCIATED WITH TWO SCREW TERMINALS (TABLE 1). FOR EXAMPLE, CELL NUMBER 5 SHOWN, IS CONNECTED TO SCREW TERMINALS 11 AND 12. THE SCREW TERMINAL SIDE OF THE CIRCUIT AS VIEWED IN THE FIGURE IS ON THE RIGHT, AND THE MODULE SIDE ON THE LEFT IN ALL CASES.

MA-4811

Figure 6-25-5 Channel Number and Component Identifications

Table 6-25-1 Terminal Identification

BC40L Turret Terminal Cell Number	Screw Terminal Number	Pin Numbers J1	Pin Numbers J2
0	1	1	50
	2	2	49
1	3	3	48
	4	4	47
2	5	5	46
	6	6	45
3	7	7	44
	8	8	43
4	9	9	42
	10	10	41
5	11	11	40
	12	12	39
6	13	13	38
	14	14	37
7	15	15	36
	16	16	35
	17	25	26
	18	(21-24) (26-30)	(21-25) (27-30)
10	19	35	16
	20	36	15
11	21	37	14
	22	38	13
12	23	39	12
	24	40	11

Table 6-25-1 Terminal Identification (Cont)

BC40L Turret Terminal Cell Number	Screw Terminal Number	Pin Numbers	
		J1	J2
13	25	41	10
	26	42	9
14	27	43	8
	28	44	7
15	29	45	6
	30	46	5
16	31	47	4
	32	48	3
17	33	49	2
	34	50	1

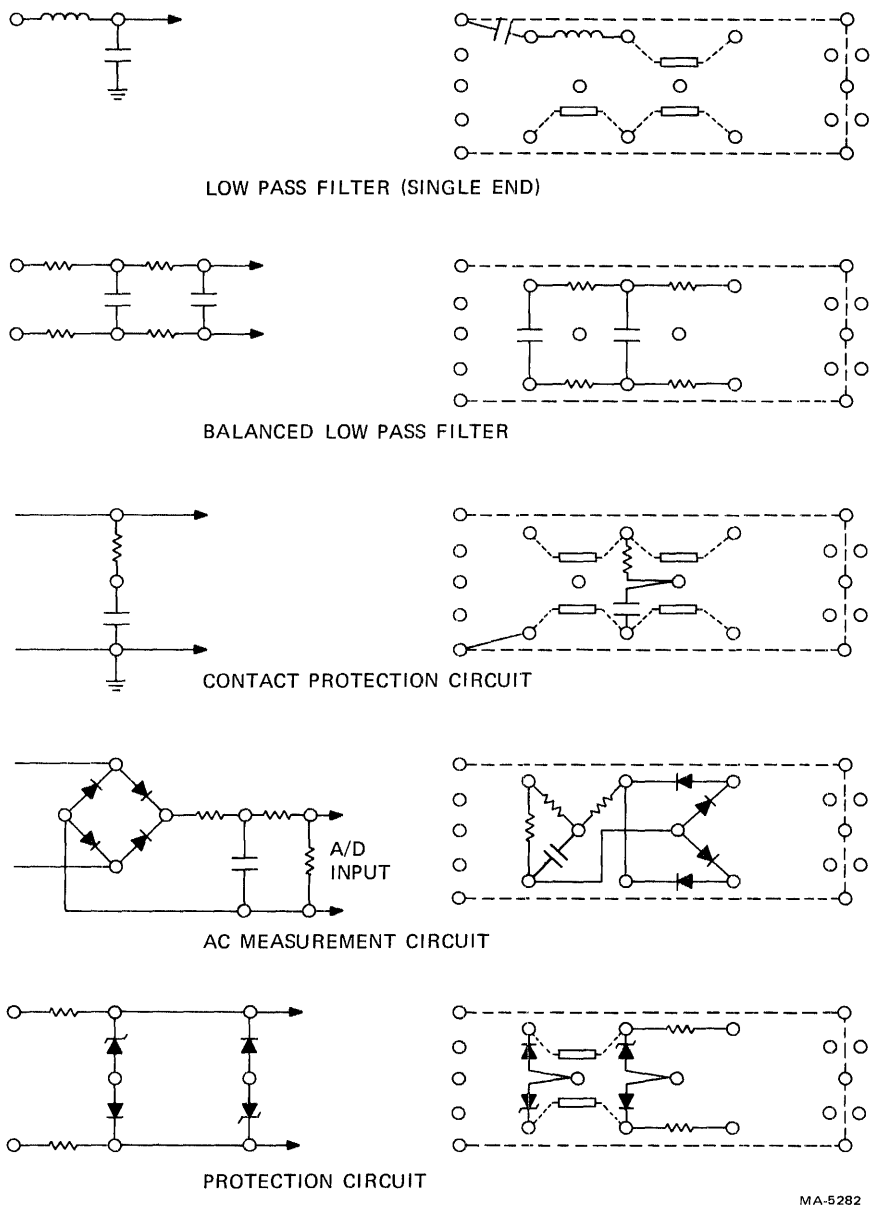


Figure 6-25-6 Application Examples

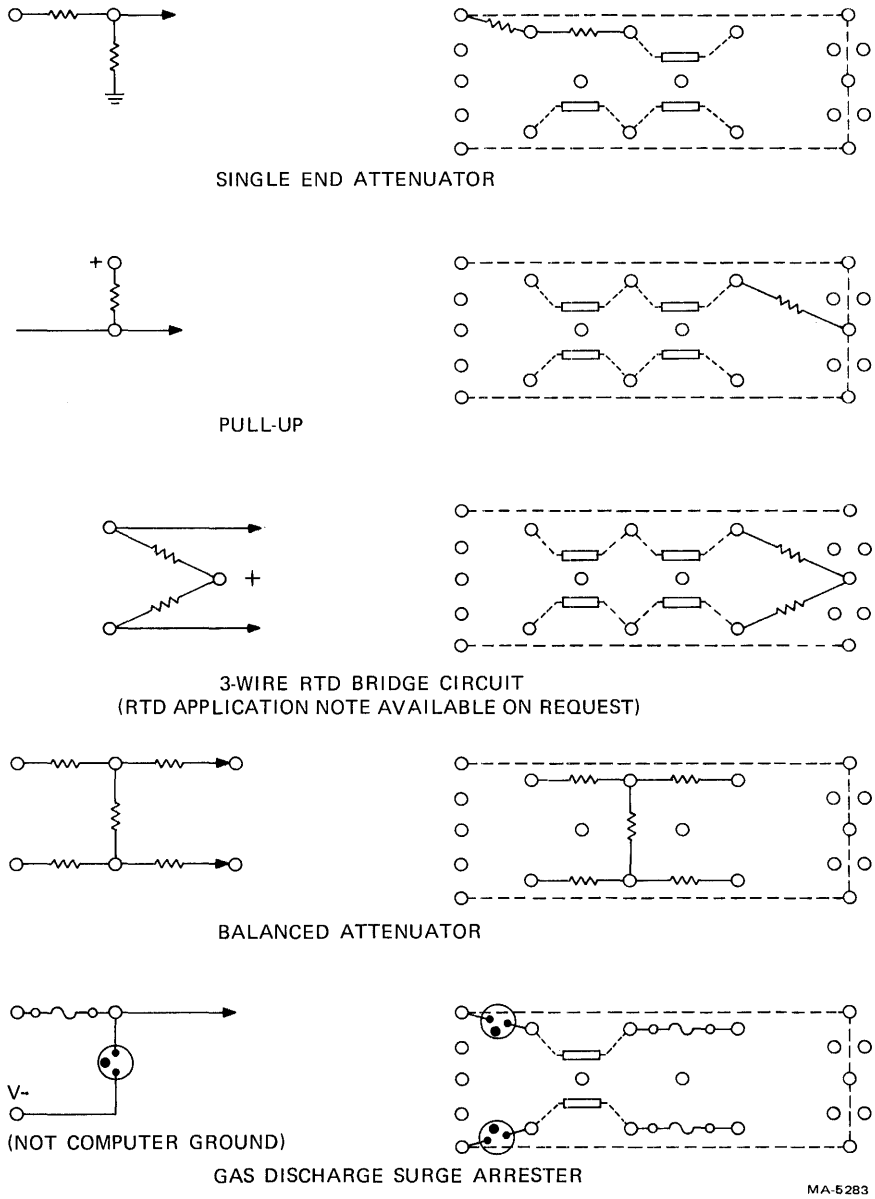


Figure 6-25-7 Application Examples

FUNCTIONAL DESCRIPTION

The A158 RMS input multiplexer offers a means of monitoring ac voltages, currents, and power consumption. It is particularly useful in power control and energy management applications. It is an analog multiplexer, and is intended to be used with the AØ14 analog input subsystem on the D-bus.

The module accepts up to eight pairs of voltages, and eight current input signals (Figure 6-26-1). A multiplexer selects a voltage input signal, and its corresponding current input. These are amplified and input to separate RMS-to-dc converters, and to a multiplier and averaging circuit. Three dc voltages are produced, representing the RMS voltage, the RMS current, and the average power of the selected inputs. These voltages, along with a fourth (a calibration reference), are input to the module's output multiplexer. One of the four, selected by the processor, is routed to the AØ14 via the D-bus, where it is converted to digital data.

The A158 is a product of DIGITAL's Computer Special Systems group. Additional information is available in CSS document number YM-C152C

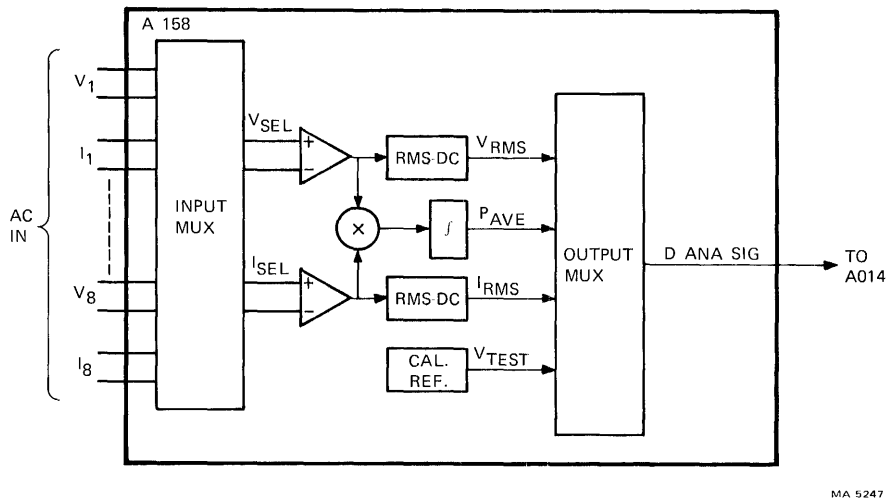


Figure 6-26-1 A158 Block Diagram

7.1 SCOPE

This chapter provides enough information to enable a person with minimum exposure to the I/O Subsystem to effect a repair in minimum time. Throughout this chapter, the reader is referred to sections in other chapters where more detailed information may be found about items such as switch settings, configurations, etc. This chapter concludes with a trouble analysis flowchart (Figure 7-2) that illustrates a logical approach to fault isolation. The chart is intended only as a useful guide to trouble analysis and does not exhaust all possibilities for system malfunction.

WARNING

Remember that the I/O Subsystem is a process controller, and its I/O modules may well control very sophisticated and perhaps even dangerous industrial processes. Therefore, before initiating any diagnostics that may affect field signals produced by the I/O modules, always check with the customer for any safety precautions and any restrictions on the operations that can be performed.

7.2 REQUIRED EQUIPMENT AND MATERIALS

In addition to standard hand tools, probes, etc., the following equipment and materials are required to perform maintenance procedures. The two dual extenders serve as a single quad.

Digital voltmeter	Weston Schlumberger model 443 or equivalent
Oscilloscope	Tektronix model 465 or equivalent
Voltage standard	E.D.C. model MV105G or equivalent*
Module extenders	Two W900 (multilayer extenders must be used)
Diagnostic	MD-11-CVPCAD-0
Print set	B-TC-H333

7.3 SPARES

It is recommended that the customer stock one spare for every ten modules (or fraction thereof) of a given type. The following fuses should be stocked in quantities of five each.

Fuse Type	DEC Part No.	Where Used
Picofuse 62.5 mA	90-09122	M5010, M5011, M5016, A630
Picofuse 1 A	12-10929-02	M6010, M6011, M5014, M6010-YA, A014, A156, A157, M6014

*The voltage standard must have been accurately calibrated within the last six months to achieve acceptable calibration of analog I/O modules.

Picofuse 0.5 A	12-09159-00	A020
Picofuse 2 A	12-11751	M6012, M6015
Special	12-12442	M6013
6.25, A 250 V, SB	90-07223-00	H7870 power supply (115 V)
3 A, 250 V, SB	90-07218-00	H7870 power supply (230 V)
2 A, 250 V, SB	9007216-00	H7872-A power supply (115 V)
1.5 A, 250 V, SB	9007213-00	H7872-B power supply (230 V)

WARNING

Use of any fuse other than the one specified for the M6013 module may result in personal injury, equipment damage, and/or improper operation. The module is equipped with a spare holder for this fuse to ensure that one is always conveniently available.

7.4 ADJUSTMENTS

Adjustments may be required for the power supplies and the analog I/O modules. Adjustment procedures for analog I/O modules are part of the I/O subsystem diagnostic program. Locations of the adjustments on these modules is shown in Chapter 6 of this manual. Power supply adjustment procedures are given below.

7.4.1 H7870 Power Supply Adjustment

Power supply voltage measurements can be made without removing the power supply; however, if adjustment is required, the supply must be removed. The adjustment potentiometers (marked on the module) are located on the printed circuit board inside the supply (Figure 7-1). Adjust the power supply as follows.

1. Remove power supply cover and slide power supply out until access to the adjustments is possible.

   NOTE

   In order to slide the supply out far enough to access the adjustments, it may be necessary to unplug the console/backplane interface cable. If this is done, proper orientation of the connector must be observed when reinstalling it (Chapter 3, Paragraph 3.3.4 and Figure 3-14).

2. Attach DVM probes to front panel test points +5 V and RETURN (R).

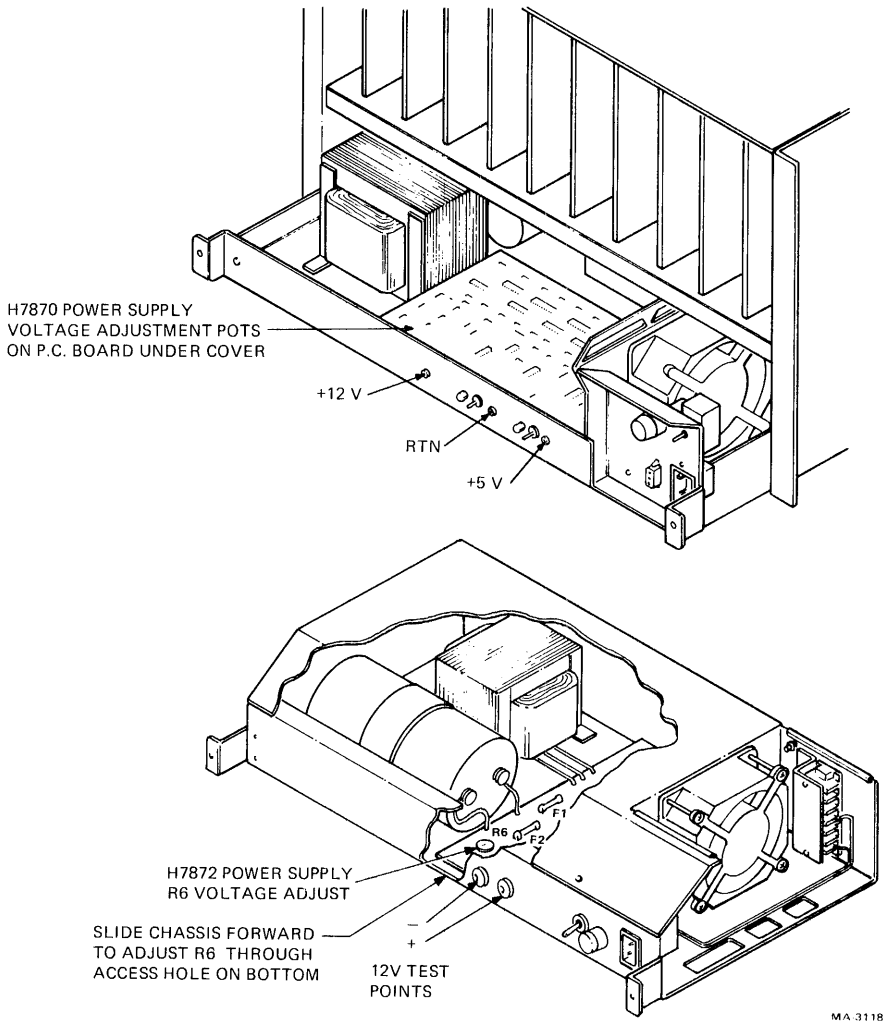


Figure 7-1 Power Supply Adjustments

3. Voltage reading should be +5.1 V ±Ø.15 V.

4. If reading is out of tolerance, correct by adjusting the +5 V potentiometer.

5. Move the (+) DVM probe to the +12 V test point.

6. Reading should be +12 V ±Ø.36 V.

7. If reading is out of tolerance, correct by adjusting the +12 V potentiometer.

8. Slide the supply back into the frame and replace the cover.

7.4.2 H7872 Power Supply Adjustment

Calibration of the H7872 +12 V output is accomplished by adjusting R6, which is accessible when the power supply is pulled forward in its chassis. Access for the adjustment tool is through a hole in the bottom of the power supply drawer (Figure 7-1). If adjustment is necessary, proceed as follows.

1. Remove the two screws that fasten the power supply to the chassis and slide it out until access to R6 is possible.

2. Attach DVM probes to the front panel test points + and -12 V.

3. Voltage reading should be +12 V $\pm$Ø.36 V.

4. If reading is out of tolerance, correct by adjusting R6 (Figure 7-1).

5. Slide the power supply back into the chassis and replace the fastening hardware.

7.5 CORRECTIVE MAINTENANCE

Corrective maintenance has been simplified in the I/O Subsystem. Most failures can be located in minimum time by using the maintenance tools available. This section includes maintenance feature descriptions and maintenance tips, which should be understood when solving a problem, and a corrective maintenance approach listing the basic failure analysis techniques. The flow diagram (Figure 7-2) is a useful guide to fault isolation.

7.5.1 Maintenance Features

The following is a list of maintenance features built into the I/O Subsystem.

1. Maintenance bit - a CSR bit that provides two functions:

   a. It generates a maintenance interrupt when the interrupt enable bit is set. After the interrupt is accomplished, reading the IAR (interrupting address register) returns the low byte of the CSR (control status register) address (377).

   b. With the maintenance bit set, reading any address returns the low byte of that address, whether or not there is a module with that address installed in the subsystem.

2. Some input modules are able to read the complement of the input data when the TBIT is set in the CSR. Many of the other modules have an additional built-in test capability that is activated by the TBIT.

3. Output modules are able to read back the data that was written out to them.

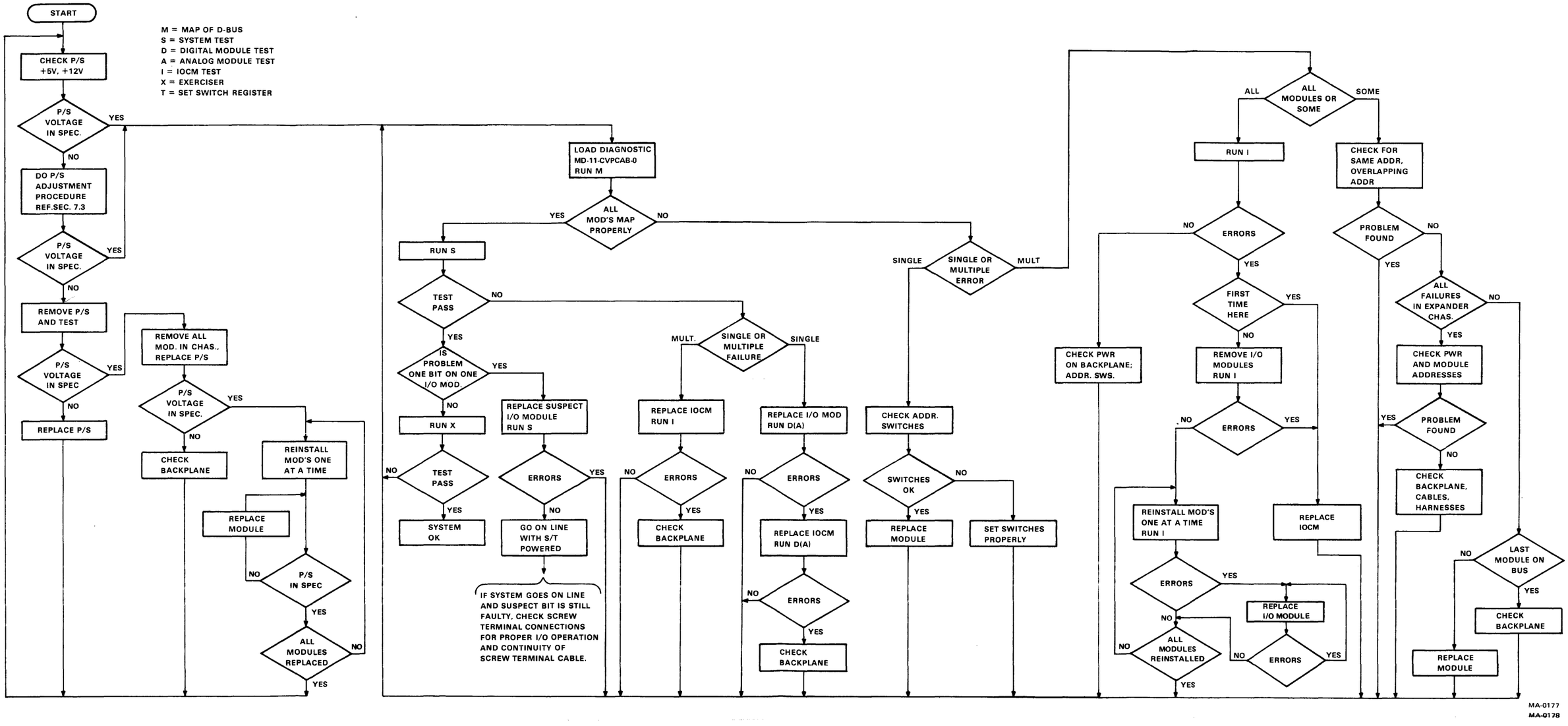


Figure 7-2 I/O Subsystem Trouble Analysis Flowchart

4. The A/D converter module (AØ14) has an on-board ramp feature that allows a basic check of the analog circuits.

5. The D/A converter module (A63Ø) contains circuits that allow the outputs of the four channels to be compared and the result of the comparison sent back when the module is read.

6. All modules can have their inputs/outputs disabled by setting the DBIT in the CSR.

7.5.2 Maintenance Tips

The following tips are important when performing maintenance on the I/O Subsystem.

1. Isolate the I/O control module. In an IP11 or IP3ØØ system, this is accomplished by removing the first I/O module; in an IP11Ø or IPV1Ø system, unplug the D-bus cable from the M8719 I/O control module.

2. Ensure that an I/O failure is not common to all I/O modules. For example, if you attempt to read a module's data and receive the low byte of the module's address, and other modules react the same, the problem is most likely to be in the control module.

3. I/O module addresses do not have to be contiguous.

4. I/O modules use from 8 to 64 bits depending on the type. Data is in 8-bit bytes; therefore, a 32-bit module has four bytes and requires four addresses. Module addresses must not overlap, i.e., if a 4-byte module has its address set to 171ØØØ, the next module must have its address set to 171ØØ4 or higher. If its address were set to 171ØØ2, an overlap condition would exist. Moreover, I/O module addresses must not overlap the CSR or the IAR, e.g., a 4-byte module cannot have its address set to 171374.

5. Multibyte modules must use appropriate address boundaries as discussed in Chapter 4, Paragraph 4.2.1.

6. The diagnostic prints an I/O module map (when the M option is selected), giving module types and addresses. The list begins with the lowest address. The listing will not match the physical module layout unless the addresses have been assigned in ascending order on the D-bus. For instance, the following situation might occur.

	Physical Module Layout		Printed Map	
Slot	Module	Address	Module	Address
1	M5Ø12	771ØØØ	M5Ø12	171ØØØ
2	M5Ø1Ø	771Ø2Ø	M6Ø1Ø	171Ø04
3	M6Ø1Ø	771Ø04	M5Ø11	171Ø1Ø
4	M5Ø13	771Ø15	M6Ø13	171Ø14
5	M6Ø13	771Ø14	M5Ø13	171Ø15
6	M5Ø11	771Ø1Ø	M5Ø1Ø	171Ø2Ø

NOTE

In addition to the module number and address, the module map includes the full name of the module.

7. All modules have switches for selecting addresses. These switches should be checked before replacing a suspect module.

8. A notebook containing the I/O module configurations and other pertinent information will normally be maintained in the vicinity of the system. When running the map option of the diagnostic, this list should be compared to the notebook to ensure that all I/O modules have responded.

9. If there is an empty slot(s) between I/O modules or between the IOCM and the first I/O module, a continuity module (M9Ø19) must be installed in the C and D connectors of the empty slot(s).

1Ø. The M7958 (IOCM) must be the last LSI-11 option on the LSI-11 Bus, not counting the bus terminator.

11. An I/O module or the IOCM must never be plugged into or removed from the subsystem with system power applied. This invariably damages the modules.

12. The IOCM and the I/O modules use CMOS logic; if failures require that ICs be replaced on these modules, precautions for handling static-sensitive components must be used.

13. On subsystems with multiple power supplies, system power should be controlled by the master power switch either on the H333 or PDP-11 CPU. If power supply problems require that individual power switches be cycled, the entire subsystem must be powered down and the I/O modules removed from the suspect chassis. After the modules are removed, the individual power switch for that chassis can be cycled.

14. If problems appear to be in the field wiring, the LEDs on the I/O modules should be checked for proper installation and seating. If a LED has become unseated, reinstall it with the cathode toward the dot etched on the printed circuit board.

15. There are timing restrictions that affect system programming (Chapter 4, Paragraph 4.5.4).

16. Memory refresh should be performed only by the MSV11-C or MSV11-D memory modules. Refresh by the CPU or by the REV11-A must be disabled or improper operation will result.

7.5.3 Basic Failure Analysis Procedure

Throughout this discussion it is assumed that only the I/O Subsystem has a problem and that the rest of the system is operational.

NOTE

Although the diagnostic disables the I/O modules from the field wiring, it is a good practice to remove all power from the field wiring to ensure that no output point will be inadvertently enabled.

7.5.3.1 Quick Checklist - The following is a list of the more common causes of failure and should be checked initially.

1. Check bus cables for proper installation (Chapter 3, Paragraph 3.3.2.3).

2. Ensure that switches on the control module are set properly (Chapter 3, Paragraph 3.5.1).

3. Ensure that there are no empty slots between I/O modules.

4. Check indicator lamps on power supplies (Figure 7-1) and control module (Figure 3-16 or 3-18):

   a. Power supplies - DC ON - is on

   b. Control module indicators - +5 V and +12 V ON - all others off.

5. Check screw terminal cables for proper installation (Chapter 3, Paragraph 3.3.3.3).

6. Check power supply voltages (Paragraph 7.3).

7.5.3.2 Diagnostic Check - Load and run diagnostic MD-11 CVPCAD-Ø.

1. Run the map (M) option and ensure that all I/O modules respond properly.

2. Run the system test (S) option.

3. Most faults will be located by running the above options. One notable exception is the final stage of an I/O module, which cannot be tested by the diagnostic. Therefore, if a problem is encountered with "BIT XX" on one of the I/O modules, and running the diagnostic indicates the module is functioning properly, the problem may still be on the module. If the application allows the use of field wiring during the test, the diagnostic subtests should be used to verify the operation of the I/O stages of the suspect module. If this fails to isolate the fault, the field wiring should be checked to see if the proper signals are present.

4. Determine whether the problem is associated with one module or more than one. A fault on the control module can make all I/Os appear faulty. One I/O module could cause a bus problem that would make all I/Os appear bad.

5. Bus fault isolation - Isolation of modules in the I/O subsystem is readily accomplished.

   a. Control modules are isolated from the I/O modules as follows:

      M7958 - remove first I/O module

      M7959 - unplug D-bus cable from J1 of M7959

      M8719 - unplug D-bus cable from J1 of M8719

   b. Removing any I/O module will open the bus in the (H333) chassis.

      NOTE

      Some bus signals in the H334 expansion chassis are bussed straight across the backplane and removing a module will not isolate them. In this case, all modules must be removed and then reinstalled one at a time to isolate a fault.

APPENDIX A
MNEMONIC DEFINITIONS

A.1 GENERAL

Some signal names in this list differ by a prefix only such as B DIN, D DIN, and R DIN. DIN stands for Data In in each case, but the spaced prefix further identifies the signal:

BUS XXX - UNIBUS signal
B XXX - LSI-11 bus signal
D XXX - D-bus signal.

The references identify a location where the signals may be observed, for example, IOC E6-8 stands for M7958 I/O Control, component E6 and pin 8 (refer to print set B-TC-H333).

Mnemonic	Definition
ADRO	Ref. IOC E6-8. Address Out - Asserted at the beginning of the D-bus Cycle Selects the address mode of the D-bus output multiplexer
AØØ	Ref. IOC E2-6. Address Bit - Assertion means an odd address has been selected Causes transceivers to transmit high byte
B IRQ	Ref. IOC E21-8. Bus Interrupt Request - Asserted by subsystem if its interrupt enable and flag signals are asserted Means some device on the LSI-11 bus requires service
B RPLY	Ref. IOC E35-1Ø. Bus Reply - Asserted in response to B DIN, B DOUT, and IAK transactions Indicates some device on the LSI-11 bus has accepted output data or placed input data on the bus
B SYNC	Ref. IOC AJ2. Bus Synchronize - Asserted by bus master to indicate it has placed address on bus
BUS BR	Bus Request - Assertion means a device is requesting control of the UNIBUS
BUS BG	Bus Grant - Assertion means a device is granted control of the UNIBUS
BUS SACK	Selection Acknowledge - Assertion means device acknowledges its selection as UNIBUS master
BUS INTR	Interrupt - Assertion means a device has put its interrupt vector on the UNIBUS

Mnemonic	Definition
BUS C1	Assertion means a data transaction from slave to master (DATI) Negation means a data transaction from master to slave (DATO)
BUS MSYN	Master Sync - Assertion means the UNIBUS master is starting a data transaction Negation means the UNIBUS master considers the transaction complete
BUS SSYN	Slave Sync - Assertion means that the UNIBUS slave has valid data on the UNIBUS or that it has accepted data from the UNIBUS
CIA	Ref. IOC E2-15. Control or Interrupt Address - Asserted when either the CSR or IAR is addressed
CLR	Ref. IOC E36-14. Clear Bit, bit Ø1 of the CSR - Assertion causes the subsystem to reset without requiring a reset instruction Self-clearing and write-only
C MAINT	Ref. IOC E37-3. Clear Maintenance - Clears the maintenance bit in the CSR
C RIF	Ref. E37-6. Clear RIF - Clears the RIF bit in the CSR
CSR	Control and status register
D ADDR	Ref. IOC E52-5. D-bus address - Assertion indicates start of modified D-bus Cycle that reads the address of the interrupting module
D-BUS	H333 I/O bus
DCE	Ref. IOCC E1-3. Data Cycle Enable - Assertion enables D-bus data transactions
D DIN	Ref. IOC CR1/CR2. D-bus Data Input Strobe - Assertion causes addressd I/O module to place appropriate data on the D-bus and to acknowledge the operation by asserting D RPLY
D DOUT	Ref. IOC CS1/CS2. D-bus Data Output Strobe - Assertion causes addressed I/O module to accept data from the D-bus and to acknowledge the operation by asserting D RPLY

Mnemonic	Definition
D GBIT	Ref. IOC DE1/DE2. D-bus Generic Bit, CSR bit Ø2 - Assertion causes an I/O module to respond with its identity code instead of normal data
DIN	Ref. IOC E1-14. Data In - Assertion produces the VECTOR signal during an interrupt transaction, and NO INTR DIN otherwise
D INTR	Ref. IOC DK2. D-bus Interrupt - Assertion at the IOCM means that some I/O module on the D-bus requires service. This signal is daisy-chained to all I/O modules.
DOUT	Ref. IOC E1-13. Data Out - Assertion enables the R DOUT signal, or writing into the CSR
D SYNC	Ref. IOC CP2. D-bus Synchronize - Strobes I/O modules at D-bus Cycle SYNC TIME and causes addressed module to store the output of its address decoder as the MY ADDRESS signal
DT LATCH	Ref. IOC E5-3. Data Time Latch - Indicates that the data phase of the D-bus Cycle is in progress
DBIT	Ref. IOC E36-3. Disable Bit, bit Ø4 of the CSR - Assertion implements I/O disable mode on all I/O modules
DEV SEL	Ref. IOC E2-1Ø. Device Select - Assertion means that an I/O Subsystem address has been decoded
D INIT	Ref. IOC E32-2. D-bus Initialize - Restores all I/O module logic to the startup state, and is asserted by B INIT, low backup supply voltage (when implemented), negation of the DBIT, or setting the CBIT
D INTR CLOCK	Ref. IOC DM2. D-bus Interrupt Clock - Stabilizes interrupt priority
DRIVE DBUS	Ref. IOC E55-3. D-bus Driver Strobe - Assertion enables D-bus output drivers
D RPLY	Ref. IOC CU2. Reply - Asserted in acknowledgment of D DIN or D DOUT by the addressed I/O module
D SYS CLOCK	Ref. IOC DV2. D-bus System Clock - 1ØØ kHz crystal-controlled oscillator signal for I/O module timing

Mnemonic	Definition
D TBIT	Ref. IOC E52-9. D-bus Test Bit, CSR bit Ø3 - Assertion implements I/O test mode on all I/O modules
EAB	Ref. IOC E9-1Ø. Enable Address on Bus - Assertion starts D-bus Cycle timing sequence
FLAG	Ref. IOC E33-8. FLAG Bit, CSR bit Ø7 - Assertion indicates that the I/O Subsystem requires service
GBIT	Ref. IOC E36-11. Generic Bit, CSR bit Ø2 - Assertion produces the D GBIT signal which causes an I/O module to respond with its identity code instead of normal data
INTR ENABLE	Ref. IOC E21-16. Enable Interrupt, CSR bit Ø6 - Enables subsystem interrupts If F = 1, E = 1, and the processor status allows interrupts, the processor will be interrupted
IOCM	Input/Output Control Module
IAR	Ref. IOC E4-6. Interrupting Address Register - Assertion produces the D ADDR signal and initiates the Modified D-bus Cycle that reads the address of the interrupting module
INIT	Ref. IOC E37-11. Initialize - Initializes IOCM Assertion clears the address register, interrupt control, timeout circuit, and the CSR
IOR	Input/Output Register
LOAD ADDR	Ref. IOC E1-2. Load Address - Initiated by B SYNC Assertion strobes the I/O module address into the address register of the M7958 Negation resets the SYNC TIME and DATA TIME flip-flops and clears the address register
MAINT	Ref. IOC E31-5. Maintenance Bit, CSR bit Ø5 - Assertion forces a maintenance interrupt if E=1. If M=1, then F=1. Reading an IOR with M=1 results in data equal to the address of that IOR, whether or not there is a module installed in that address
MAINT DATA	REF. IOC E3-6. Maintenance Data - Assertion enables a maintenance data input

Mnemonic	Definition
MY ADDRESS	Ref. I/O module MY ADDRESS flip-flop. Assertion indicates the module has been addressed The MY ADDRESS flip-flop is set when D SYNC occurs if the module's address decoder output is high If the decoder output is low, the flip-flop is reset
NO INTR DIN	Ref. IOC E17-6. No Interrupt Data In - Synchronizes all subsystem data reading operations except the interrupt vector
READ CSR	Ref. IOC E15-6. Read CSR - Enables the CSR output to the transceivers Also clears MAINT and RIF at the end of the current cycle
R DIN	Ref. IOC E1Ø-6. Data In - Assertion produces the D DIN signal to the D-bus
R DOUT	Ref. IOC E1Ø-8. Data Out - Assertion produces the D DOUT signal to the D-bus, after a short delay
REC LB	Ref. IOC E17-3. Assertion places the low byte of the LSI-11 bus onto the internal data bus of the M7958
REC HB	Ref. IOC E25-8. Assertion places the high byte of the LSI-11 bus onto the internal data bus of the M7958
RIF	Ref. IOC E31-9. Reset Interrupt Flag, bit ØØ of the CSR - Causes the I/O module being read to reset its internal interrupt flag RIF is cleared at the end of the cycle in which an I/O module or the CSR is addressed
R INIT	Ref. IOC E38-11. R Initialize - Produces the D INIT signal
R INTR CLOCK	Ref. IOC E38-6. R Interrupt Clock - Produces the D INTR CLOCK signal
R SYNC	Ref. IOC E1Ø-11. R Synchronize - Produces the D SYNC signal
SETUP TIME	Ref. IOC E12-6 and E9-4. SETUP TIME - The time from D-bus Cycle initialization until SYNC TIME that allows for stabilization of the address on the D-bus

Mnemonic	Definition
SYNC TIME	Ref. IOC E9-4 and E9-8. SYNC TIME - The time between SETUP TIME and DATA TIME that allows for address determination on the I/O modules prior to a data transaction
TBIT	Ref. IOC E36-7, CSR Bit Ø3. Test Bit - Produces the D TBIT signal
UBUS HI XMIT	Assertion causes the M8719 to route its internal data to the UNIBUS high byte
UBUS LO XMIT	Assertion causes the M8719 to route its internal data to the UNIBUS low byte
VECTOR	Ref. IOC E21-1. Transmit Interrupt Vector - Causes the subsystem interrupt vector to be put on the LSI-11 bus
WRITE CSR	Ref. IOC E18-11. Write CSR - Assertion causes the CSR to store new data
XMIT HB	Ref. IOC E25-12. Transmit High Byte - Assertion causes the M7958 internal data bus to be routed to the high byte of the transceiver input to be put on the high byte of the LSI-11 bus
XMIT LB	Ref. IOC E25-6. Transmit Low Byte - Assertion causes the M7958 internal data bus to be routed to the low byte of the transceiver input to be put on the low byte of the LSI-11 bus

APPENDIX B
FLOATING VECTOR ASSIGNMENTS

B.1 GENERAL

A floating vector convention is used for communication (and other) devices that interface with the PDP-11. These vector addresses are assigned in order, starting at 300 and proceeding upward to 777. Table B-1 shows the assigned sequence. The first vector address, 300, is assigned to the first DC11 in the system. If another DC11 is used, it would then be assigned vector address 310, etc. When the vector addresses have been assigned for all DC11s (up to a maximum of 32), addresses are then assigned consecutively to each unit of the next highest-ranked device (KL11, DP11, or DM11, etc.), then to the other devices in accordance with the priority ranking.

Table B-1 Priority Ranking for Floating Vectors (Starting at 300 and Proceeding Upward)

Rank	Device	Vector Size (Octal)	Maximum Number
1	DC11	10	32
2	KL11, DL11-A, DL11-C	10	16
3	DP11	10	32
4	DM11-A	10	16
5	DN11	4	16
6	DM11-BB	4	16
7	DR11-A	10*	32
8	DR11-C	10*	32
9	PA611 Reader	4*	16
10	PA611 Punch	4*	16
11	DT11	10*	8
12	DX11	10*	4
13	DL11-C, DL11-D, DL11-E	10	31
14	DJ11	10	16
15	DH11	10	16
16	GT40	10	1
17	LPS11	30*	1
18	DQ11	10	16
19	KW11W	10	1
20	DU11	10	16
21	ICS11/ICR11	4	12
22	IP11/IP110	4	16

*The first vector for the first device of this type must always be on a 10_8 boundary.

When the vector addresses have been assigned to all higher ranking devices, addresses are then assigned to each IP11Ø, (or IP11) beginning with the second one in the system. The first IP11Ø (or IP11) is always assigned vector address 234.

NOTE

Floating vectors range from address 3ØØ-777, but addresses 5ØØ-534 are reserved for special bus testers. In addition, address 1ØØØ is used for the DS11 Synchronous Serial Line Multiplexer. Refer to Appendix A of the PDP-11 Peripherals Handbook, 1976, for a complete discussion of UNIBUS addresses.

APPENDIX C
USER FORMS

Refer to Chapter 3, Paragraph 3.6 for instructions on the proper use of the forms in this section.

I/O MODULE USER PAGE

PAGE NO. _____

MODULE TYPE _____ BYTE _____ OF _____

GENERIC CODE _____

BYTE ADDRESS _____ SINGLE SHOT TIMING _____

MUX NO. _____

MODULE LOCATION: CHASSIS NO. _____ FIELD POWER: COMMON ☐ AC ☐

SLOT NO. _____ ISOLATED ☐ DC ☐

POINT	INTR. ENAB.	BIT FUNCTION REMARKS
00		
01		
02		
03		
04		
05		
06		
07		

ADDITIONAL COMMENTS:

I/O SUBSYSTEM USER GUIDE
EK-0PIOS-UG-005

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_____

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What features are most useful? _____

_____

_____

_____

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_____

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_____

Does this manual satisfy the need you think it was intended to satisfy? _____

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