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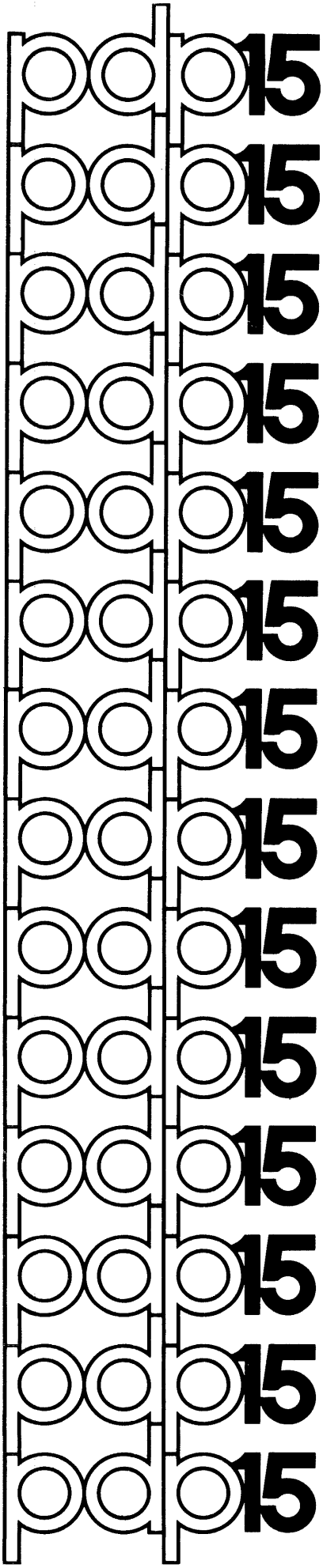

UC15

unichannel-15 system maintenance manual

digital equipment corporation

DEC-15-HUCMA-B-D

pdp15

UC15
UNICHANNEL 15 SYSTEM
MAINTENANCE MANUAL

digital equipment corporation · maynard, massachusetts

1st Edition, February 1973
2nd Printing (Rev) April 1973
3rd Printing, November 1973

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CHAPTER 1
SYSTEM AND PHYSICAL DESCRIPTION

1.1 GENERAL

The UNICHANNEL 15 System (UC15) consists of a programmable controller that interfaces a PDP-15 Central Processor to the PDP-11 Unibus (Figure 1-1). The Unibus contains 18 address lines, various control lines, and 16 data lines. Two additional lines are incorporated, giving a total of 18 data lines, in order to be compatible with the PDP-15 18-bit processor. The PDP-15 functions as the master processor; the programmable controller functions as a slave in carrying out the tasks initiated by the PDP-15. The programmable controller will normally be a PDP-11/05 Central Processor. Peripheral control occupies only a small part of the programmable controller's time. The rest of this time can be used for parallel processing of tasks as conceived by the system designer. (See *UNICHANNEL 15 Software Manual,* DEC-15-XUCMA-A.) The programmable controller runs its own program with 4K or 8K dedicated memory, hereafter referred to as local memory.

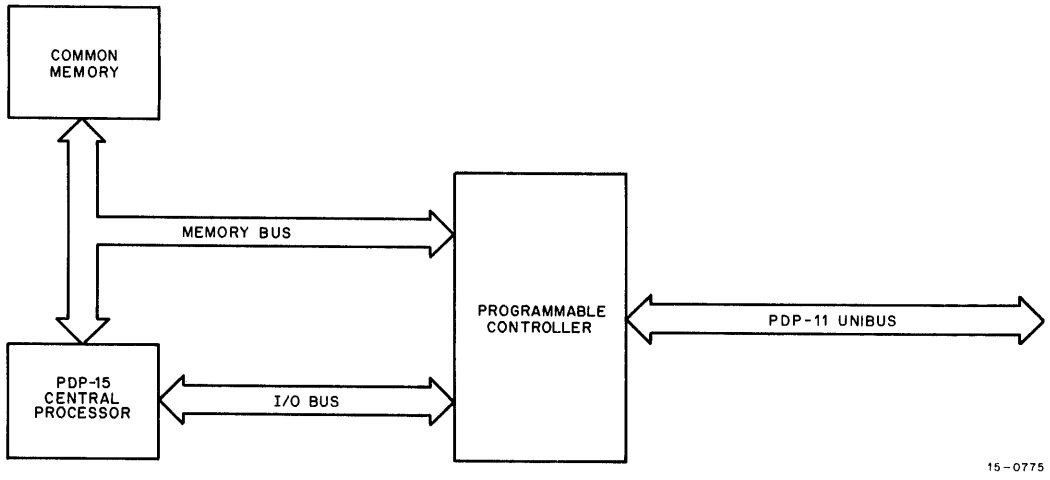

Figure 1-1 UC15 System Concept

1.2 COMMON MEMORY

The UNICHANNEL 15 System allows any Non-Processor Request (NPR) device on the Unibus to access PDP-15 memory so that data can be transferred between I/O devices and common memory.

The utilization of common memory allows ease of data transfer between common memory and secondary storage (disk, magnetic tape, etc.). The programmable controller can operate with a maximum 28K of common memory if no relocation option is employed. If local memory contains 4K, the programmable controller can address the lowest 24K of common memory. With 8K of local memory, the programmable controller can address only the lowest 20K of common memory. The Unibus can address the combined PDP-15/PDP-11 memory, which can extend up to 124K.

1.3 INTERRUPT LINK

The PDP-15 and the programmable controller communicate with each other through the use of device interfaces. The PDP-15 functions as a master processor by initiating and defining tasks, while the programmable controller functions as a slave device. When the PDP-15 initiates a new task, it interrupts the programmable controller with a message. The message is designated as a Task Control Block Pointer (TCBP) and points to a table (Task Control Block) in common memory where the task is defined. The programmable controller performs the task and signifies its completion by sending an interrupt back to the PDP-15 (Figure 1-2).

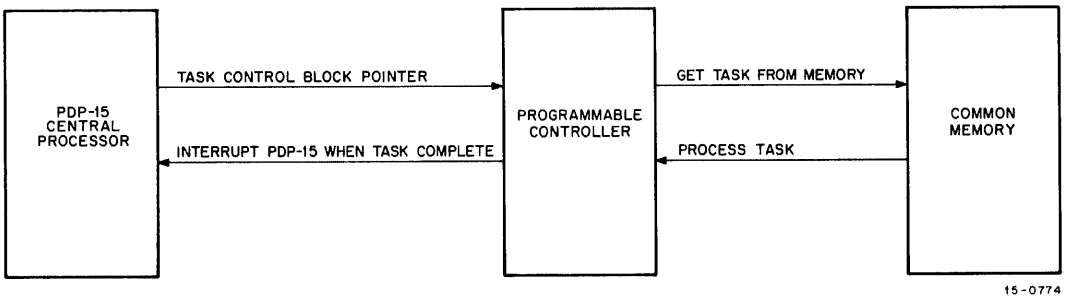

Figure 1-2 Simplified Flow Diagram

1.4 PROGRAMMABLE CONTROLLER HARDWARE

The UC15 System, in its standard configuration, consists of the following equipment (Figure 1-3):

- PDP-11 programmable controller
- DR15-C Device Interface
- Two DR11-C Device Interfaces
- MX15-B Memory Multiplexer
- Local memory

NOTE

The PDP-11, which functions as the programmable controller, can itself only process 16-bit words but controls peripherals that can process 18-bit words to provide compatibility with the PDP-15.

The DR15-C and the two DR11-C Device Interfaces provide the communication facility between the PDP-15 and the PDP-11. The PDP-15 can interrupt the PDP-11 and send data words to the PDP-11; however, the PDP-11, serving as a programmable controller, can only interrupt the PDP-15 indicating an error condition or job completion.

The MX15-B Memory Multiplexer functions as a memory bus switch to allow either the PDP-15 or the PDP-11 to communicate with the common memory.

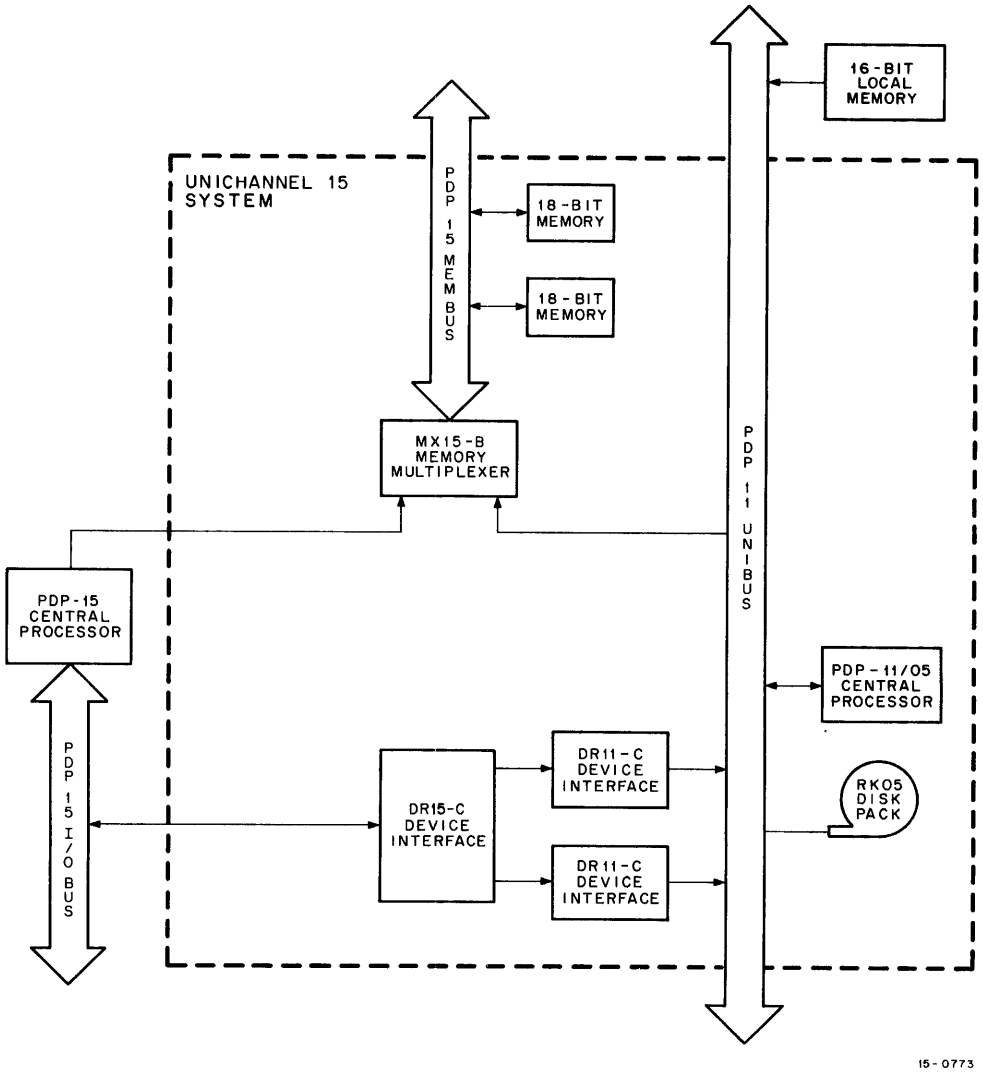

Figure 1-3 UC15 Hardware

1.5 UC15 CONFIGURATIONS

In the standard UC15 configuration, the programmable controller is a KD11-B Processor (PDP-11 family) with a 1 μs cycle time and 4K of local memory. Several variations are possible.

A different PDP-11 processor with a faster or slower cycle time can be utilized. However, it would be available only through Computer Special Systems.

Another possible variation is that any Unibus peripheral can be connected into the system.

16-bit direct memory access (DMA) devices, called NPR devices on the Unibus, can transfer only 16 bits of data to and from memory (the upper two of the 18 bits being defined as 0s). 18-bit NPR Unibus devices, such as the RK15 DECdisk Pack, will transfer the full 18-bit data words to and from common memory.

Byte oriented Unibus devices, such as DECtape, DEC cassette, paper tape, magtape, line printers, and communications interfaces, transfer data under control of the PDP-11 programmable controller, which is limited to 16 bits. Hence, format conversion for these devices from 16-bit or 8-bit formats to 18 bits (and vice versa) must be done by the PDP-15.

1.6 SPECIFICATION SUMMARY

- Sum of PDP-11 and PDP-15 memory limited to 124K.
- Normal configuration includes 4K of local memory, allowing 120K of shared memory.
- PDP-11, with 4K of local memory, can address only lowest 24K of common memory to access (1) task control blocks set up the PDP-15, and (2) data for byte oriented Unibus devices.
- Normal PDP-11/05 processor gives an NPR break a worst-case latency of 7 μs. Total worst-case latency time is 12 μs (7 μs NPR latency plus 5.0 μs for PDP-15 to do three I/O memory cycles, with addition of MX15-B multiplexer).
- Addressable Registers

  DR11-C/#0

CSR (API DONE, ENABLE API DONE INTR)	767770
Output Data Buffer (API 1, API 0 Address)	767772
Input Data Buffer (API 0, 1, 2, 3 DONE, Upper 2 bits of TCBP, LMS 0, 1)	767774
Interrupt Vector – 300	
Priority Level – BR5	

  DR11-C/#1

CSR (new TCBP, ENABLE TCBP INTR)	767760
Output Data Buffer (API 2, API 3 Address)	767762
Input Data Buffer (TCBP)	767764
Interrupt Vector – 310	
Priority Level – BR7	
DR15-C 18-bit Data Register (loaded by LIOR IOT)	

- Task Initiation

  Task Control Block Pointer

  PDP-15 LIOR IOT (706006) – clear flag, load TCBP, and interrupt PDP-11

  PDP-11 Interrupt vector 310 at priority level 7

- Task Completion

  PDP-11 loads one of the following four bytes with an API address:

767772	API level 0
767773	API level 1
767762	API level 2
767763	API level 3

  API logic interrupts PDP-15 at API address. If API (Automatic Priority Interrupt) option is not installed, a PI (program interrupt) is created with four skip IOTs for decoding.

- Bus Loading

  MX15-B

  2 PDP-15 memory bus load
  Drives 4 PDP-15 memory bus loads

  DR15-C/DR11-C

  1 Unibus load
  1 PDP-15 I/O bus load

- Power

DEC Channel 15	7A at 115V
(With RK15 DECdisk)	3.5A at 230V

- Voltage — 115 Vac ± 10%, 230 Vac ± 10%

- Frequency — 50 ± 2 Hz, 60 ± 2 Hz

- Environmental

Temperature	10° to 50°C
Relative Humidity	20% to 95%

- Installation

  UC15 hardware includes a UC15 cabinet and space for mounting PDP-11 peripherals. There are 2 spaces 10-1/2 in. high and 1 space 5-1/4 in. high. In addition, mounting space for 2 small peripheral controllers (SPC) exists within the PDP-11/05 processor.

- UC15 Cabinet Dimensions

Depth:	30 in. (0.76m)
Width:	21 in. (0.53m)
Height:	72 in. (1.83m)
Weight:	250 lbs (115 kg) – not including peripherals

- Unibus Compatibility

  Can be used with any PDP-11 family processor that does not use parity. On those systems with parity, the parity must be disabled.

- Memory Cycle

  MX15-B normally adds 200 ns to both the PDP-15 and the PDP-11 cycle times.

- DMA Facility to Common Memory

Maximum Transfer Rate	415K words/sec
Worst-Case Latency	6 μs (no DCH transfers in PDP-15) 12 μs (DCH transfers in PDP-15)
Average Latency	2.5 μs

- DMA Facility to PDP-11/05 Local Memory

Maximum Transfer Rate	1 million words/sec
Worst-Case Latency	7.2 μs
Average Latency	2.5 μs

CHAPTER 2
PROGRAMMING

The prime objective of PIREX software is to provide the users of software systems like RSX-PLUS, BOSS, or DOS with support for Unibus peripherals such as the RK15 DECdisk (*UNICHANNEL 15 Software Manual,* DEC-15-XUCMA-A-D).

2.1 TASK INITIATION AND COMPLETION

The PDP-15 and the PDP-11 programmable controllers communicate with each other through the use of interrupt requests that are transferred from one processor to the other via the DR15-C/DR11-C interrupt link. The PDP-15, which serves as the master, initiates tasks on the PDP-11 by transferring a 16-bit (expandable to 18) TCBP. The Task Control Block, located in common memory, contains the information needed by the PDP-11 to complete the task. If an error occurs or the task is completed, the PDP-11 informs the PDP-15 by sending an interrupt at an API level and address specified in the Task Control Block. The UC15 System contains four API interrupt levels; an API interrupt may be pending at each level. The system can be operated with PI or API; however, it is recommended that the API option be employed for more efficient operation.

NOTE

Data can be transferred from the PDP-15 to the PDP-11 via an interrupt request. However, only interrupt requests can be transferred from the PDP-11 to the PDP-15. Thus, the PDP-11 functions as a peripheral with respect to the PDP-15.

2.2 TASK INITIATION, DETAILED DESCRIPTION

Before the PDP-15 can initiate a task, the following conditions are established.

- The PDP-15 must set up a Task Control Block in common memory. The Task Control Block contains information as to the device being addressed, the priority level, type of message, etc.

- In order for the PDP-15 to interrupt the PDP-11 with a new TCBP, bit 6 (ENABLE TCBP INTR) of location 767760 in the PDP-11 must be set. In addition, bit 7 (new TCBP) of this location is set by the LIOR IOT; this occurs when a new TCBP is loaded in the DR15-C status register.

- In order for the PDP-11 to interrupt the PDP-15 after the task has been completed, a one-bit status register (DR15-C status register) must be set. This is accomplished by loading the PDP-15 accumulator with all 0s, except for a 1 in bit 17, and issuing the Write Status IOT (706122), which transfers the contents of the accumulator to the DR15-C status register.

- The PDP-15 must also test its DONE flag to make sure it is set. If the DONE flag is not set, a previous TCBP has not been accepted by the PDP-11. The PDP-15 must continue testing until the DONE flag is set. This is accomplished by the following coding:

```
LAC TCBP        /LOAD TCBP IN PDP-15 ACCUMULATOR
SIOA            /TEST; IF NEW TCBP SKIP
JMP. -1         /JUMP BACK AND TEST AGAIN
LIOR            /LOAD TCBP INTO DR11-C
```

After the above conditions have been met, the PDP-15 accumulator is loaded with the TCBP which points to the first address in the Task Control Block. The PDP-15 issues the LIOR IOT (706006) that transfers the TCBP to the PDP-11.

NOTE

In order to read the TCBP into the PDP-11, bits 6 and 7 of location 767760 must be set. Bit 6 indicates a new TCBP is in the DR15-C data register; bit 7 allows the PDP-15 to interrupt the PDP-11 at interrupt vector 310.

The PDP-15 interrupts the PDP-11 and reads the TCBP into the PDP-11 which is now handled by the PIREX software system. When the TCBP is read into the PDP-11, the TCBP DONE flag in the PDP-15 is set allowing additional TCBPs to be transferred in.

The PDP-11 now has the information necessary to complete the task. A typical task might be transferring a block of data words from a disk to common memory. The PDP-11 commands the disk to transfer the block of data to memory. The disk then proceeds to transfer the 18-bit data words through the multiplexer (MX15-B) to memory. When the block transfer is complete, the disk interrupts the PDP-11 and the PDP-11, in turn, using information in the Task Control Block, interrupts the PDP-15.

2.3 TASK COMPLETION, DETAILED DESCRIPTION

Upon completion of the task, the PDP-11 obtains an API level and an API address from the Task Control Block. It loads the API address in the appropriate byte of the DR11-C and sets the corresponding API flag. If the API option is not installed, the API flag will cause a PI. In this case, it is necessary to test the flag using a Skip chain (SAPI0, SAPI1, SAPI2, SAPI3 IOT instructions, Paragraph 2.5). If the API option is installed, the source of the interrupt is known since the interrupt will cause the new PC to come from a unique API address. In addition to the Skip chain IOTs, a series of clear API flags (CAPI0, CAPI1, CAPI2, and CAPI3) are provided to clear the flags. When the PDP-15 is interrupted by the PDP-11, it signifies that an error exists or that the task has been completed by the PDP-11.

2.4 REGISTER DESCRIPTIONS

The DR15-C contains an 18-bit data register and a 1-bit status register. Each of the DR11-Cs contains a Control and Status Register (CSR), an output data buffer, and an input data buffer. The register addresses are shown below; the bit format of each register is described in the following paragraphs.

DR15-C

18-bit data register	Loaded by LIOR IOT
1-bit status register	Loaded by LDRS IOT

DR11-C/#0

CSR	767770
Output data buffer	767772
Input data buffer	767774

DR11-C/#1

CSR	767760
Output data buffer	767762
Input data buffer	767764

2.4.1 DR15-C Registers

The 18-bit data register (Figure 2-1) is used to temporarily store the TCBP received from the PDP-15. The register is loaded with the contents of the PDP-15 accumulator (containing the TCBP) by the LIOR IOT instruction.

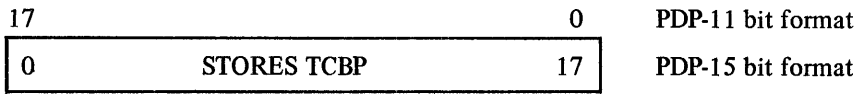

Figure 2-1 18-Bit Data Register

NOTE
Observe that PDP-15 bits range from 0 (MSB) to 17 (LSB), while PDP-11 bits range from 17 (MSB) to 0 (LSB).

The status register (Figure 2-2), when set, enables interrupts from the PDP-11, and when reset, disables the interrupts. Bits 16 through 0 of the status register are not implemented by the hardware.

Figure 2-2 1-Bit Status Register

NOTE
This register is set to a 1 by initialize and the CAF instruction. It can be cleared only by using the LDRS IOT (706122) instruction.

2.4.2 DR11-C Registers

The CSR, output data buffer, and input data buffer for DR11-C/#1 are described first, followed by a description of the same registers for DR11-C/#0.

DR11-C/#1 CSR 767760 (Figure 2-3)

Bits 15 through 8 – Not used.

Bit 7 – New TCBP flag – This bit is set to a 1 when the PDP-15 issues IOT 706006 (load I/O register and clear DONE flag), which places a new TCBP in the DR15-C data register.

Bit 6 – ENABLE TCBP INTR – This bit, if set, allows an interrupt on BR level 7 to interrupt vector 310 when a new TCBP is received from the PDP-15.

Bits 5 through 0 – Not used.

DR11-C/#1 Output Data Buffer 767762 (Figure 2-3)

Bit 15 – Not used.

Bits 14 through 8 – These bits contain the address for an API 3 break. If the API is enabled and no higher priority is present, a new value in these bits will cause an API break in the PDP-15.

Bit 7 – Not used.

Bits 6 through 0 – These bits contain the address for an API 2 break. If the API is enabled and no higher priority is present, a new value in these bits will cause an API break in the PDP-15.

DR11-C/#1 Input Data Buffer 767764 (Figure 2-3)

Bits 17 through 3 – These bits represent the TCBP. In cases where 18-bit addressing for the PDP-11 is used, bits 1 and 2 from input data buffer 767774 are appended to the TCBP to provide 18-bit addressing capability. Examples of 18-bit addressing are the PDP-11/45 Central Processor with memory management or the PDP-11/40 Central Processor with segmentation.

DR11-C/#0 CSR 767770 (Figure 2-4)

Bits 15 through 8 – Not used.

Bit 7 – API DONE – This bit is set to a 1 when none of the four API channels has a request pending.

Bit 6 – ENABLE API DONE INTR – This bit will enable an API interrupt if the API DONE flag (bit 7) is set.

NOTE

Bits 7 and 6 are not expected to be used in normal system programming.

Bits 5 through 0 – Not used.

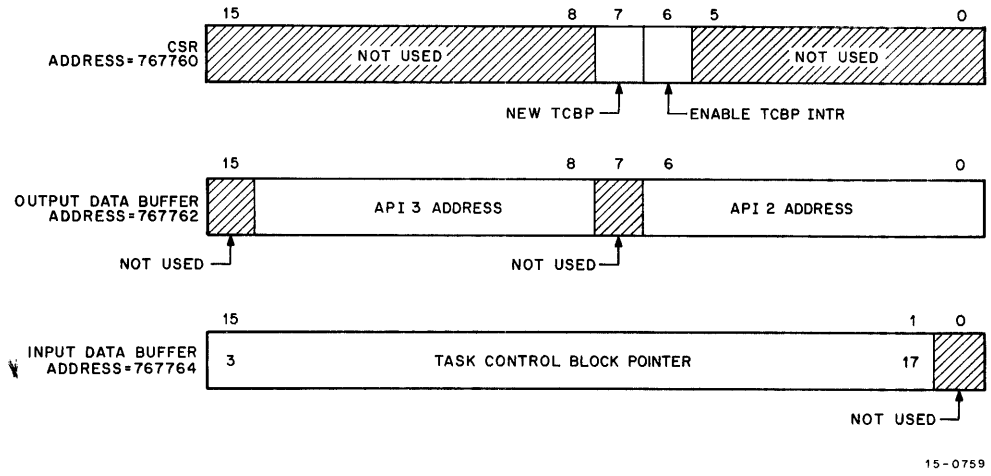

Figure 2-3 DR11-C/#1 Bit Formats

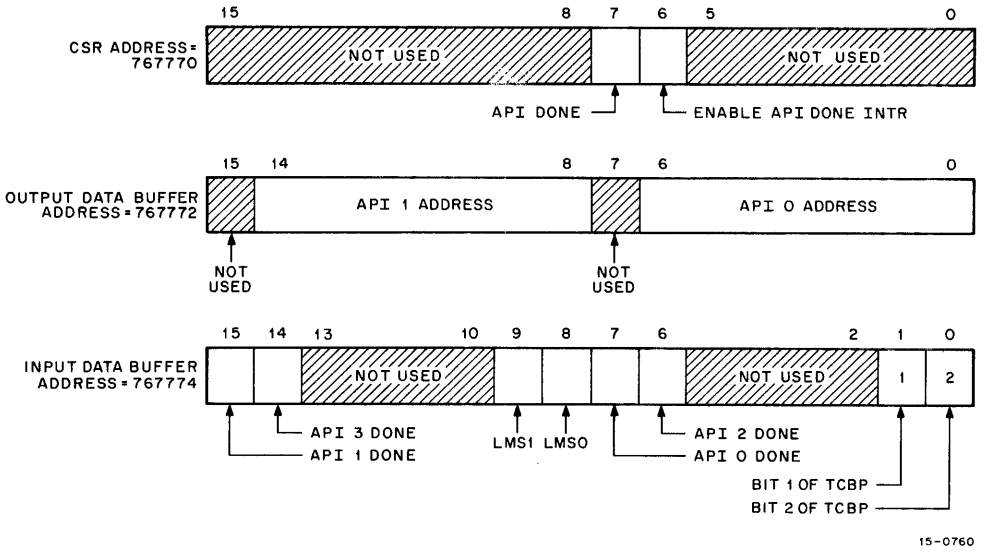

Figure 2-4 DR11-C/#0 Bit Formats

DR11-C/#0 Output Data Buffer 767772 (Figure 2-4)

Bit 15 – Not used.

Bits 14 through 8 – These bits contain the address for an API 1 break. If the API is enabled and no higher priority level is present, a new value in these bits causes an API break in the PDP-15.

Bit 7 – Not used.

Bits 6 through 0 – These bits contain the address for an API 0 break. If the API is enabled and no higher priority level is present, a new value in these bits causes an API break in the PDP-15.

DR11-C/#0 Input Data Buffer 767774 (Figure 2-4)

Bit 15 – API 1 DONE
Bit 14 – API 3 DONE
Bit 7 – API 0 DONE
Bit 6 – API 2 DONE

Where one of the above bits is set, it indicates that an API request at that level is not pending. It also indicates that the appropriate high or low bytes of the output data buffer can be loaded with a new API address in order to cause an API break. For example, if API 1 DONE is a 1, the API 1 address can be loaded in bits 14 through 8 of the output data buffer whose address is 767772.

NOTE
Bits 13 through 10 and bits 5 through 2 are not used.

Bit 8 – Local Memory Size (LMS) Bit 0 – The least significant bit of a two bit field which specifies the number of 4K word memory banks connected to the Unibus.

Bit 9 – Local Memory Size Bit 1 – The most significant bit of a two bit field which specifies the number of 4K memory banks connected to the Unibus.

LMS1	LMS0	
0	0	0 Local Memory
0	1	4K Local Memory
1	0	8K Local Memory
1	1	12K Local Memory

Bits 1, 0 – These bits are extension bits of the TCBP and are used when 18-bit addressing capability is desired.

In this case, bit 1 of the TCBP is located in bit position 01 and bit 2 is located in bit position 00. These bits, when used, represent bits 1 and 2 of the TCBP.

2.5 PDP-15 IOT INSTRUCTIONS

The PDP-15 uses a set of IOT (Input/Output Transfer) instructions to transfer data, control, or status information from a selected peripheral via the I/O bus to the PDP-15 accumulator or vice versa. These IOT instructions, which are used with the DR15-C interface, are described below.

706001 SIOA – Skip Input/Output Data Accepted

This IOT tests the TCBP DONE flag and, if set, skips the next instruction.

706002 CIOD – Clear Input/Output Done

This IOT clears the TCBP DONE flag.

706006 LIOR – Load Input/Output Register and Clear TCBP DONE flag

This IOT transfers the TCBP from the PDP-15 accumulator to the DR15-C 18-bit data register. The output of this register is seen by the PDP-11 at location 767764 and at bits 0 and 1 of location 767774.

This IOT also clears the TCBP DONE flag and forces New TCBP (bit 7 in location 767760) to a 1, causing the PDP-11 to do an interrupt (BR level 7) to interrupt vector 310.

706101 SAPI0 – Skip if API0 flag on 1

This IOT tests the API0 flag in the DR15-C and skips the next instruction if the flag is 1.

706121 SAPI1 – Skip if API1 flag on 1

This IOT tests the API1 flag in the DR15-C and skips the next instruction if the flag is 1.

706141 SAPI2 – Skip if API2 flag on 1

This IOT tests the API2 flag in the DR15-C and skips the next instruction if the flag is 1.

706161 SAPI3 – Skip if API3 flag on a 1

This IOT tests the API3 flag in the DR15-C and skips the next instruction if the flag is 1.

706104 CAPI – Clear API0 flag

This IOT clears the API0 flag in the DR15-C.

706124 CAPI1 – Clear API1 flag

This IOT clears the API1 flag in the DR15-C.

706144 CAPI2 – Clear API2 flag

This IOT clears the API2 flag in the DR15-C.

706164 CAPI3 – Clear API3 flag

This IOT clears the API3 flag in the DR15-C.

706112 RDRS – Read Status Register

This IOT clears the PDP-15 accumulator and loads the contents of the DR15-C status register into the accumulator.

NOTE

This action causes the ENABLE PI/API bit (bit 17) of the DR15-C status register to be transferred to bit 17 of the accumulator. The remaining bits of the status register are not implemented by the hardware. When the ENABLE PI/API bit is set, it allows the PDP-11 to interrupt the PDP-15.

706122 LDRS – Load Status Register

This IOT loads the contents of the PDP-15 accumulator into the DR15-C status register.

NOTE

This action causes bit 17 of the accumulator to be placed in the ENABLE PI/API bit (bit 17) of the DR15-C status register. The remaining bits of the status register are not implemented by the hardware.

2.6 OPERATION

If the PDP-11/05 does not have an associated Teletype®, the PDP-15 console Teletype can be connected to the PDP-11/05 via a KL8-E Cable Assembly, DEC Part No. 7008360, which is supplied with the PDP-11/05. To load programs into the PDP-11 local memory it is necessary to first load the ABSL 11 Loader into common memory. This permits a PDP-11 absolute format paper tape to be loaded into common memory with the PDP-15 tape reader. This loader also allows the program loaded into common memory to be transferred to the PDP-11 local memory where it can be run.

NOTE

In order to load any PDP-11 diagnostic, the ABSL 11 loader tape must be loaded. When this is loaded, load the diagnostic in the paper tape reader and press the CONTINUE button on the PDP-15. When the PDP-15 stops, load address 60000 in the PDP-11 (4K of local memory) and press the START button (with 8K of local memory, start at 100000). When the PDP-11 stops, the program has been relocated into PDP-11 local memory. To obtain a typeout from the program, disconnect the PDP-15 TTY (Teletype) console and reconnect it to the PDP-11. Connect the jumper plug (B-UA-UC15) to the PDP-15 console TTY lines. This prevents constant TTY interrupts from occurring and allows the paper-tape reader to operate.

The UC15 System basically operates in one of the following three modes.

a. Normal Operation – This mode of operation is employed with such system software as DOS or RSX-15. Details can be found by referring to the *UNICHANNEL 15 Software Manual* (DEC-15-XUCMA-A-D).

b. System Exerciser – Refer to the System Exerciser Diagnostic Program for details on the system exerciser.

c. Performing PDP-11 Diagnostics – Refer to Chapter 6 of this manual.

2.7 SYSTEM RESTRICTIONS

Certain restrictions are placed on the system due to the design criteria. These restrictions affect CAF (clear all flags), RESET operations, and the differences between various disk packs. Each restriction is described in the following paragraphs.

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CHAPTER 3
DR15-C LOGIC DESCRIPTION

3.1 GENERAL

This chapter contains block diagram and logic diagram descriptions of the DR15-C Device Interface and the DR15-C/DR11-C Interrupt Link. A detailed description of the DR11-C Device Interface can be found in the *DR11-C General Device Interface Manual,* DEC-11-HDRCA-A-D.

3.2 DR15-C SIMPLIFIED BLOCK DIAGRAM DESCRIPTION

Figure 3-1 is a simplified block diagram of the DR15-C and Figure 3-2 is a detailed block diagram. Figure 3-3 is an interface diagram showing the interrelationships between the DR15-C and the DR11-C.

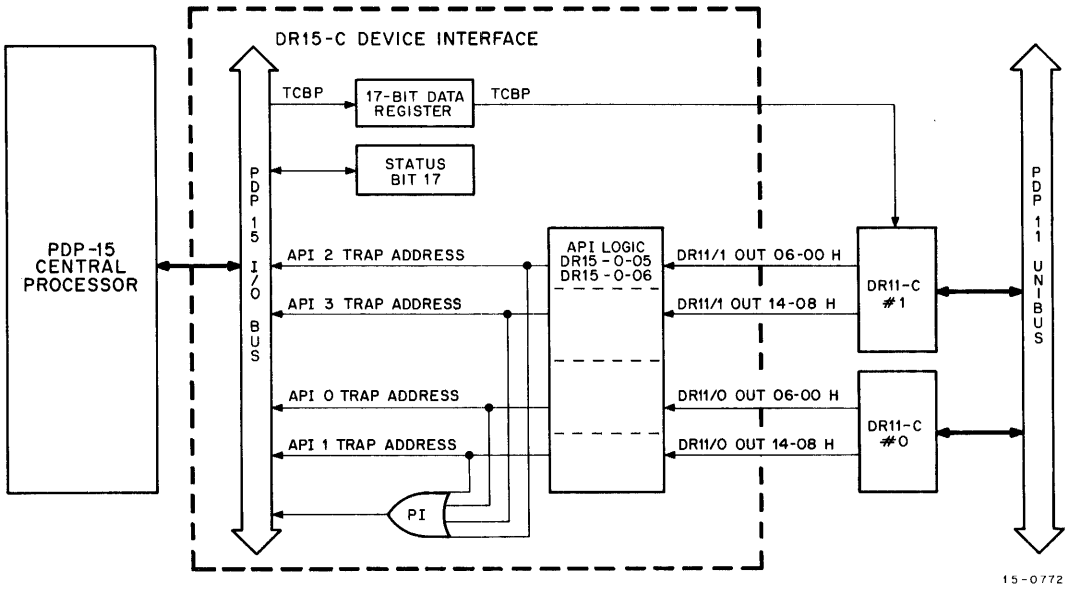


Figure 3-1 DR15-C Simplified Block Diagram

The DR15-C contains a 17-bit data register, a status register, and API and PI logic. The 17-bit data register is used for temporary storage of the TCBP. The lower 15 bits are subsequently transferred to DRINBUF at location 767764 in DR11-C/#1; the upper two bits are transferred to DRINBUF at location 767774 in DR11-C/#0 (Figure 3-3).

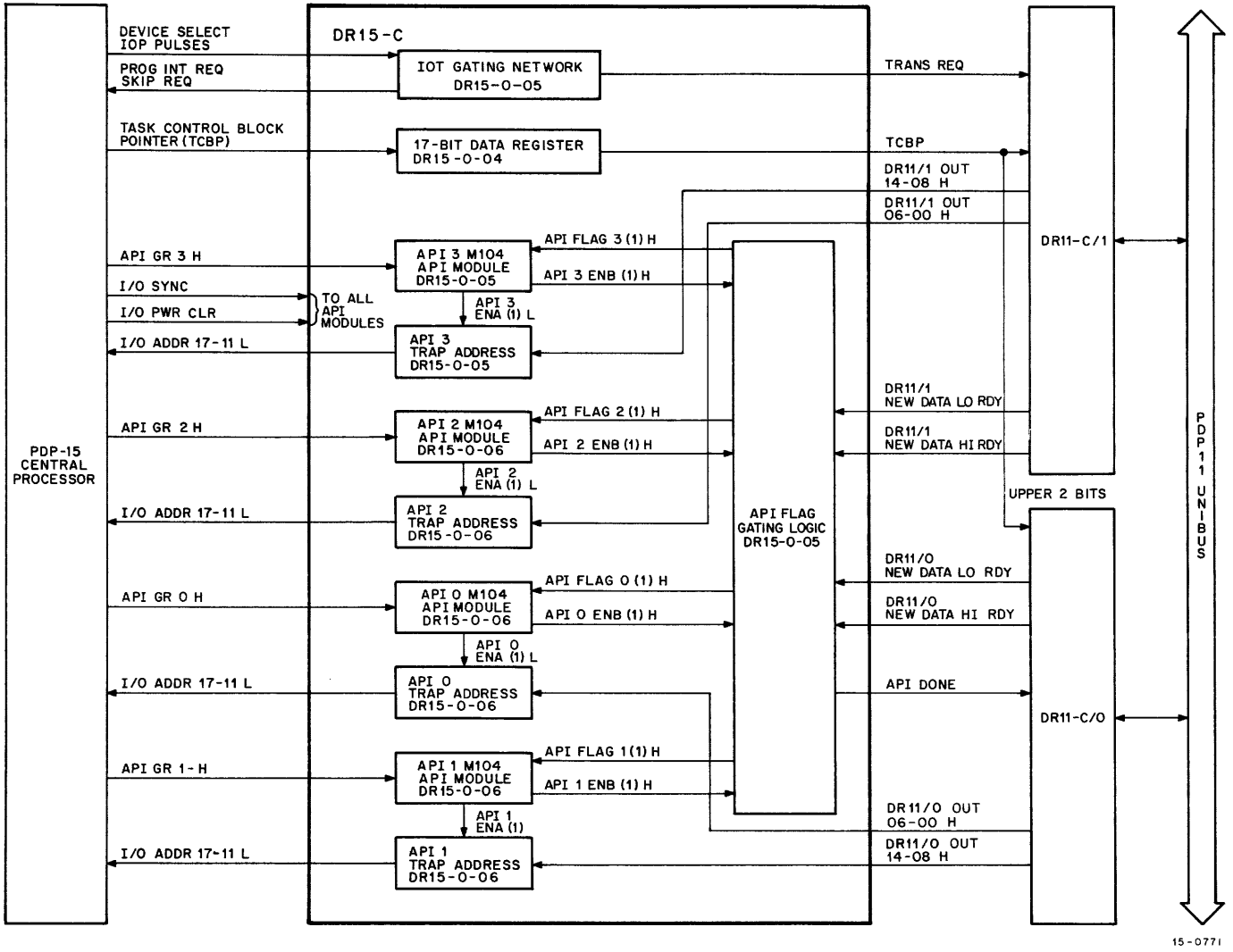


Figure 3-2 DR15-C Detailed Block Diagram

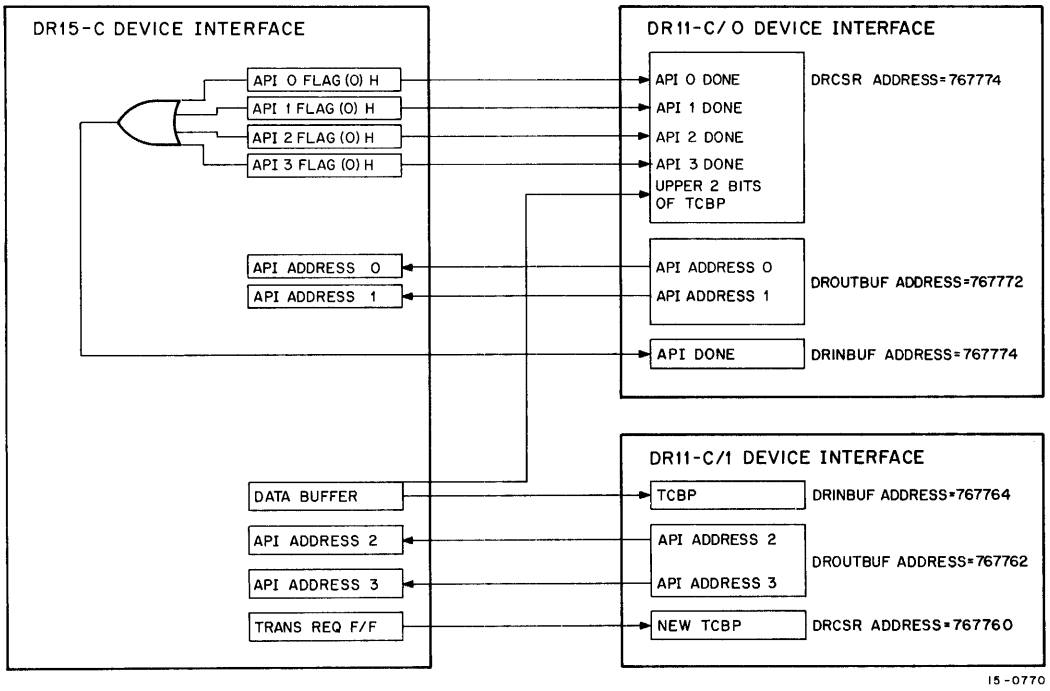


Figure 3-3 DR15-C/DR11-C Device Interface Diagram

The status register is a one-bit register connected to I/O bus bit 17. If this bit is a 1, it enables the PI or API logic in the DR15-C.

The API logic provides the PDP-11 with the ability to interrupt the PDP-15 after the PDP-11 has flagged an error condition or has completed a task. When the task is completed, the PDP-11 interrupts the PDP-15 and transfers an API level and trap address to the PDP-15. The API level and the trap address have previously been specified in the task control block. The trap address contains a JMS instruction to the device service routine which is then executed by the PDP-15.

The DR15-C also contains a PI facility which, when enabled, relieves the main program of the need for repeated flag checks by allowing the ready status of I/O device flags to automatically cause a program interrupt. The CPU can continue with execution of a program until a previously selected device signals that it has completed a task. At that time, the program in process is interrupted and the contents of the program counter (15 bits), memory protect mode (1 bit), bank or page addressing mode, and the link bit (1 bit) are stored automatically in location 000000 (Figure 3-4). The instruction in location 000001 is then executed, transferring control to an I/O service routine for IOT instructions. When completed, the routine restores the system to the status prior to the interrupt allowing the interrupted program segment to continue. Where multiple peripherals are connected to the PI, a search routine containing device-status testing (skipping) instructions must be added to determine which device initiated the interrupt request. The PI control is enabled or disabled by programmed instructions (IOTs). When disabled, the PI logic ignores all service requests, but such requests normally remain on-line and are answered when the PI is again enabled, unless they are cleared.

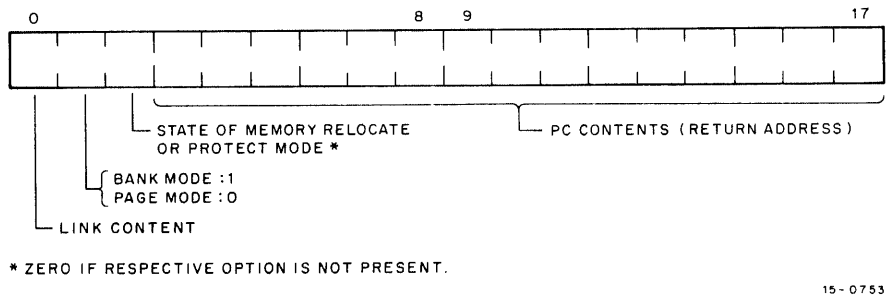


Figure 3-4 Memory Location 0 at Time of Program Interrupt

3.3 DR15-C LOGIC DIAGRAM DESCRIPTIONS

The DR15-C logic diagrams are tabulated and described in the following paragraphs.

Drawing No.	Title
D-CS-DR15-C-01	I/O BUS
D-CS-DR15-C-02	I/O BUS IN
D-CS-DR15-C-03	CONTROL IN
D-CS-DR15-C-04	TASK CONTROL BLOCK POINTER
D-CS-DR15-C-05	API CONTROL
D-CS-DR15-C-06	API ADDRESS
D-CS-DR15-C-07	PI CONTROL
D-CS-DR15-C-08	INTERFACE CABLES

3.3.1 I/O BUS Logic Diagram (DR15-C-01)

This diagram shows the I/O bus connector which is an M912 double-height double-sided FLIP CHIP connector used for interconnecting cables to peripheral devices.

3.3.2 I/O BUS IN Logic Diagram (DR15-C-02)

This diagram shows the M510 I/O bus receivers that are designed to receive PDP-15 I/O bus signals for positive logic devices. The receivers have a high input impedance and provide both noninverted and inverted versions of the input signal.

3.3.3 CONTROL IN Logic Diagram (DR15-C-03)

This diagram shows additional M510 I/O bus receivers for some of the DR15-C control signals.

3.3.4 TASK CONTROL BLOCK POINTER Logic Diagram (DR15-C-04)

This diagram shows the 17-bit data register used to store the TCBP. The D input to each flip-flop is connected to the appropriate PDP-15 accumulator bit via the I/O bus. The register is clocked by IOT 706004 (normally microcoded with IOP2 to produce IOT 706006). IOT 706002 causes the TCBP DONE flag to be cleared.

The output of the data register is connected to the DR11-C DRINBUF register as shown in Figure 3-5. Note that bit 17 of the DR15-C data register is connected to bit 1 of DRINBUF, and bit 0 of DRINBUF is subsequently always on a 0, which guarantees that the TCBP is treated as a word address rather than a byte address. If bit 0 could be a 1, the PDP-11 would trap on an odd address.

Note also that bits 3 through 17 (15 bits) of the TCBP are transferred to DR11-C/#1 DRINBUF.

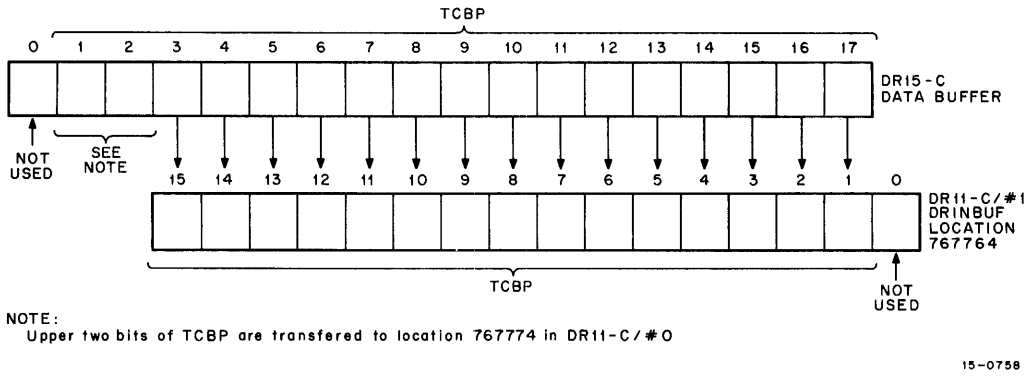


Figure 3-5 Routing of TCBP Bits

3.3.5 API CONTROL Logic Diagram (DR15-C-05)

This diagram shows the IOT logic and part of the API logic. A device code of 60_8 and a subdevice code of 0_8 are required to produce one of the following IOT instructions.

706001 SIOA – Skip on TCBP DONE flag. Indicates that PDP-11 has read TCBP. This IOT is generated if IOP1 is present.

706002 CIOD – Clear TCBP Done. This IOT is generated if IOP2 is present.

706006 LIOR – Load TCBP Register and Clear TBCP DONE Flag. This IOT is generated if IOP4 is present.

NOTE

The IOP1, IOP2, and IOP4 pulses are described in Chapter 5 of the *PDP-15 Reference Manual*, DEC-15-BRZC-D.

When IOT 706002 is generated, the DONE flip-flop is cleared as shown. When IOT 706004 is generated, the TRANS REQ flip-flop is set and the 17-bit data register is loaded with a new TCBP. TRANS REQ is transmitted to the DR11-C as a new TCBP bit (Figure 3-3). The new TCBP initiates a PDP-11 interrupt to location 310 at BR level 7. This location tells the PDP-11 a new job has been received and flags the PDP-11 to go to common memory to get the Task Control Block containing the necessary parameters to define the job. When the PDP-11 reads the TCBP, TRANS REQ is cleared, indicating that the PDP-15 can load a new TCBP. Upon completion of the task, the PDP-15 is interrupted by the API or PI logic.

To understand the API logic, assume an API request is desired on API level 3. The API trap address as specified in the Task Control Block is sent to the DR15-C on the lines labeled DR11-C/#1 OUT 14-08 H (Figure 3-2 and logic diagram DR15-C-06). In addition, a DR11/1 NEW DATA RDY HI signal is transferred to the DR15-C. This signal direct sets API3 FLAG (logic diagram DR15-C-05). The output of the flip-flop enables API 3 START H.

NOTE

API ENAB (1) L, which is the other input required for API 3 START H, is normally true when power is applied. The signal can be disabled by loading a 0 in bit 17 of the PDP-15 accumulator and issuing an LDRS 706122 IOT instruction which disables the interrupt logic.

API 3 START H is applied to the M104 API 3 module (logic diagram DR15-C-05) which causes the module to issue an API request [API 3 REQ (1) L] to the PDP-15. When the PDP-15 is free, it returns an API 3 GR H signal to grant the interrupt. This signal is applied to the M104 API module and causes the module to generate API 3 ENA (1) H. The API 3 ENA (1) H signal is applied to the M621 Data Bus Drivers on sheet DR15-C-06 to enable the 7-bit API address to be gated onto the I/O address lines.

API level 0 has the highest API priority, while API level 3 has the lowest API priority. If there are no API requests on API levels 0, 1, or 2, then the PDP-15 grants priority to API level 3. If there are requests of higher priority on these levels, they will be serviced first.

Each API module contains arbitration logic in order to ascertain which device on a particular priority level will be serviced. This is accomplished by granting priority on the basis of proximity to the I/O bus. For example, on API level 3, if the first and second device on this level both requested interrupts, the first device (closest to the I/O processor) is granted the request. This is accomplished by a signal daisy-chained from device to device. This signal is designated as API 3 EN IN at the input and API 3 EN OUT at the output. If API 3 EN IN is high at the input to a device, the device can be serviced. If the device is serviced, API 3 EN OUT will go low and disable any other devices on that priority level from being serviced.

The API logic for the other three API levels is similar to that described for API level 3. The associated address lines and NEW DATA READY signals for each API level are shown below (Figure 3-2).

Trap Address	Loaded In	Associated Data Ready
API 0	DR11-C/#0 (bits 6 through 0)	DR11/0 NEW DATA RDY LO
API 1	DR11-C/#0 (bits 14 through 8)	DR11/0 NEW DATA RDY HI
API 2	DR11-C/#1 (bits 6 through 0)	DR11/1 NEW DATA RDY LO
API 3	DR11-C/#1 (bits 14 through 8)	DR11/1 NEW DATA RDY HI

3.3.6 API ADDRESS Logic Diagram (DR15-C-06)

This diagram contains the M104 API modules for API levels 0 and 1 (the M104 modules for API levels 2 and 3 are shown on DR15-C-05). The diagram also shows the gating for enabling the API trap address to the PDP-15 I/O address lines. For example, the enable for the API level 3 trap address is API 3 ENA (1) L. When this signal goes true, the trap address is gated from the DR11-C to the I/O address lines.

NOTE

For API levels 0 and 1, I/O address bit 11 uses an M622 Data Bus Driver rather than an M621 I/O Bus Driver. The function performed by both gates, however, is exactly the same. A similar situation is applicable to I/O address bit 17 for API levels 2 and 3.

3.3.7 PI CONTROL Logic Diagram (DR15-C-07)

This diagram shows the M161 Octal-to-Decimal Instruction Decoder, the skip logic, and the PI logic. The instruction decoder is enabled by device code 61_8 and is employed to decode the skip and clear API flag instructions. If an API flag is raised, the program skips the next instruction. To understand the IOT logic, assume that the program issues a 706101 IOT. This IOT is applied to pin V2 of the M161 Octal-to-Decimal Instruction Decoder. The decoder is turned on by a 61_8 device code except when the 706104 IOT is present and SD 00 H is true. This is to disable the decoder for a 706144 or 706164 IOT instruction.

NOTE

IOT 706144 is a CAPI2 instruction and is shown on DR15-C-05. In this case, SD 00 H and SD 01 L must be true to enable the M115 NAND gate, which clocks the API2 FLAG flip-flop. IOT 706164 is the CAPI3 instruction and is shown on DR15-C-05. For this instruction, SD 00 H and SD 01 H must be true to enable the M115 NAND gate, which clears the API3 FLAG flip-flop.

With a 61_8 device code and the IOP1 pulse, IOT 706101 (SAPI0) is generated; with this device code and IOP2, IOT 706102 (RDRS) is generated; with this device code and IOP4, IOT 706104 (CAPI0) is generated.

When a 706101 IOT is issued, the inputs to the decoder are:

SD 01 H is low (Figure 3-6)
SD 00 H is low (Figure 3-6)
IOT 706101 H is high
IOT 706104 H is low

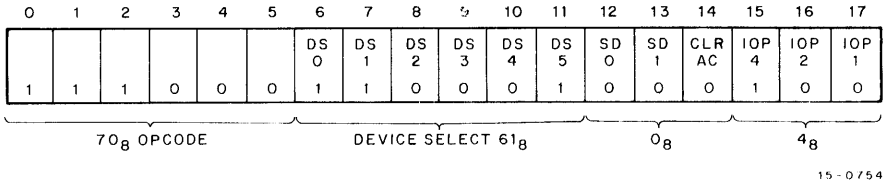


Figure 3-6 PDP-15 IOT Instruction Format

These inputs represent a binary 4 which enables output 4. This output is labeled SAPI0 L and is applied to an M112 NAND gate together with API0 FLAG (1) L. If the API0 flag is a 1, SKIP REQ L goes low and the next instruction in the program is skipped. If the API0 flag is a 0, the next sequential instruction in the program is executed. A similar situation exists for the skip instructions for API levels 1, 2, and 3.

In order to enable the PI/API facility, the API ENAB flip-flop must be set. This flip-flop is a one-bit status register whose D input is connected to bit 17 of the I/O bus and is clocked by IOT 706122 (Load Status Register). When the IOP2 pulse is generated it is ANDed with SD1 H from the decoder output to clock bit 17 from the I/O bus to the API ENAB flip-flop.

NOTE

SD1 is generated at the output of the octal-to-decimal decoder if SD 01 H is high, thereby encoding IOT 706102 to 706122 (Figure 3-6).

The contents of the one-bit status register designated API ENAB can be read back into bit 17 of the I/O bus. In order to do this a 706102 (706112 with the CLR AC bit set) IOT, together with SD0 H generates RD REQ L and DR I/O BUS 17 L signals to accomplish the transfer. SD0 H is high when the SD 00 H and the SD 01 H inputs to the octal-to-decimal decoder are both low.

The PI request (PI REQ) is enabled when the API ENAB flip-flop is set. If both an API request and PI request (both API and PI enabled) are made, the CPU services the API request first. If the API option is not installed, or if the API facility is not enabled, the PI request will be serviced. This is accomplished by ORing any API flag on a 1 to generate a PI request.

3.3.8 INTERFACE CABLES Logic Diagram (DR15-C-08)

The diagram shows the interface cables which connect the DR15-C to the DR11-Cs. The cable connections between the DR15-C and DR11-C are as follows:

DR11-C #1 CONN2	to	DR15-C B17
DR11-C #1 CONN1	to	DR15-C B18
DR11-C #0 CONN2	to	DR15-C A17
DR11-C #0 CONN1	to	DR15-C A18

CHAPTER 4
MX15-B LOGIC DESCRIPTION

4.1 GENERAL

This chapter contains logic diagram descriptions of the MX15-B Memory Multiplexer. The MX15-B allows either the PDP-11 or PDP-15 processors to access common memory. If both processors attempt simultaneous memory accesses, the PDP-15 takes precedence and performs the first memory access.

4.2 MX15-B LOGIC DIAGRAM DESCRIPTION

The MX15-B logic diagrams are tabulated and described in the following paragraphs.

Drawing No.	Title
D-CS-MX15-B-01	MX CONTROL
D-CS-MX15-B-02	11 ARRIVING
D-CS-MX15-B-03	11 ARRIVING
D-CS-MX15-B-04	UNIBUS DATA
D-CS-MX15-B-05	15 PORT
D-CS-MX15-B-06	MEMORY BUS
D-CS-MX15-B-07	PROCESSOR BUS
D-CS-MX15-B-08	BYTE REGISTER

4.2.1 MX CONTROL Logic Diagram (MX15-B-01)

This diagram consists of two sheets showing the control logic for the MX15-B. In order for the PDP-15 to access common memory, it must do one of the following three memory cycles.

a. Write cycle

b. Read cycle

c. Read-Pause-Write cycle

In order for the PDP-11 to access common memory it must do one of the following five cycles:

a. Write cycle

b. Read cycle

c. DATIP cycle

d. DATIP/DATOB cycle

e. DATOB cycle

Since the common memory does not respond to DATIP or DATOB cycles, the MX15-B must convert these cycles to simulate PDP-15 memory cycles to which the memory will respond. Both the PDP-15 and PDP-11 memory cycles are described in the following paragraphs, with the use of detailed flow diagrams for each cycle.

4.2.1.1 Synchronizer – The MX Control diagram incorporates a synchronizer circuit that provides the necessary arbitration logic for the PDP-11 and PDP-15 processors which operate asynchronously. The synchronizer also allows time for the address lines to settle before it permits M REQ to be sent to memory.

The synchronizer centers around the 15 REQ and 11 REQ flip-flops. The clock input to these flip-flops is delayed by 40 ns (M312 output pin S1). The reason for this is that in the 15 REQ flip-flop, for example, M REQ is at the D input and M REQ is also one of the signals necessary to clock the flip-flop. One of the requirements for a D-type flip-flop is that the signal at the D input must be present for 20 ns before the clock is applied, and since both D and C inputs are derived from the same source, a delay is inserted prior to the clock input. A similar situation applies to the 11 REQ flip-flop in that MSYN is applied to both D and C inputs. If both the 15 REQ and 11 REQ flip-flops are set at the same time, the 15 cycle takes precedence and occurs first.

An additional 50 ns delay is provided for a deskewing period in which the address lines are allowed to settle prior to an actual bus request being made. Termination of this delay allows REQ ACTIVE to set, which enables the M REQ signal to memory.

4.2.1.2 PDP-15 Read Cycle – A detailed flow diagram of the PDP-15 Read cycle is shown in Figure 4-1. The cycle is initiated by a memory request (M REQ) signal from the PDP-15. This signal is connected to the MX15-B multiplexer and is used to set the 15 REQ flip-flop (indicating a PDP-15 request in process) if the following conditions are satisfied:

a. 15 REQ (0) H – No 15 request in progress.

b. ENAB REQ (1) H – Indicates ADDR ACK has been received from memory and a new memory cycle can be synchronized (Paragraph 4.2.1.1).

c. PWR CLR H – No power clear.

d. ENAB REQ is cleared to inhibit further memory requests.

After a 50 ns delay to allow time for the synchronizer to settle, M REQ and the address of the memory location are sent to memory. The address precedes M REQ by the amount of time necessary for M REQ to be used as a clock to load the address in the memory controller. Upon receipt of the address, memory issues ADDR ACK which clears M REQ in the PDP-15, raises M BUSY, and generates MEM TO CP for a Read cycle. The trailing edge of ADDR ACK sets ENAB REQ and clears REQ ACTIVE (to allow additional requests). Note, 11 CYCLE (0) H is true because a PDP-15 cycle is in process. MEM TO CP is true only for PDP-15 Read cycle, and gates the MDLs from memory to the PDP-15 via the MX15-B (diagram MX15-B-05). This allows the data to be sent to the processor.

After a delay to allow for deskewing, memory places the data on the MDL and issues RD RST. RD RST is routed to the PDP-15 via the MX15-B (diagram MX15-B-05). The PDP-15 issues MRLS, upon receipt of the data, via the MX15-B. When memory receives MRLS, it issues MRLS ACK, which clears MRLS. The clearing of MRLS, in turn, clears MRLS ACK to complete the cycle.

4.2.1.3 PDP-15 Write Cycle – Figure 4-2 is a detailed flow diagram of the PDP-15 Write cycle. The sequence of events is identical with the PDP-15 Read cycle (Paragraph 4.2.1.2) until the time that ADDR ACK is received from memory. When this occurs, ENAB REQ is set, and M REQ is dropped (causing the 15 REQ flip-flop to reset). During a Write cycle, the MEM TO CP flip-flop is cleared to enable the MDL lines to do a CP-To-Memory transfer. This flip-flop is cleared at each cycle by Power Clear or by DATA ACK in a Read cycle.

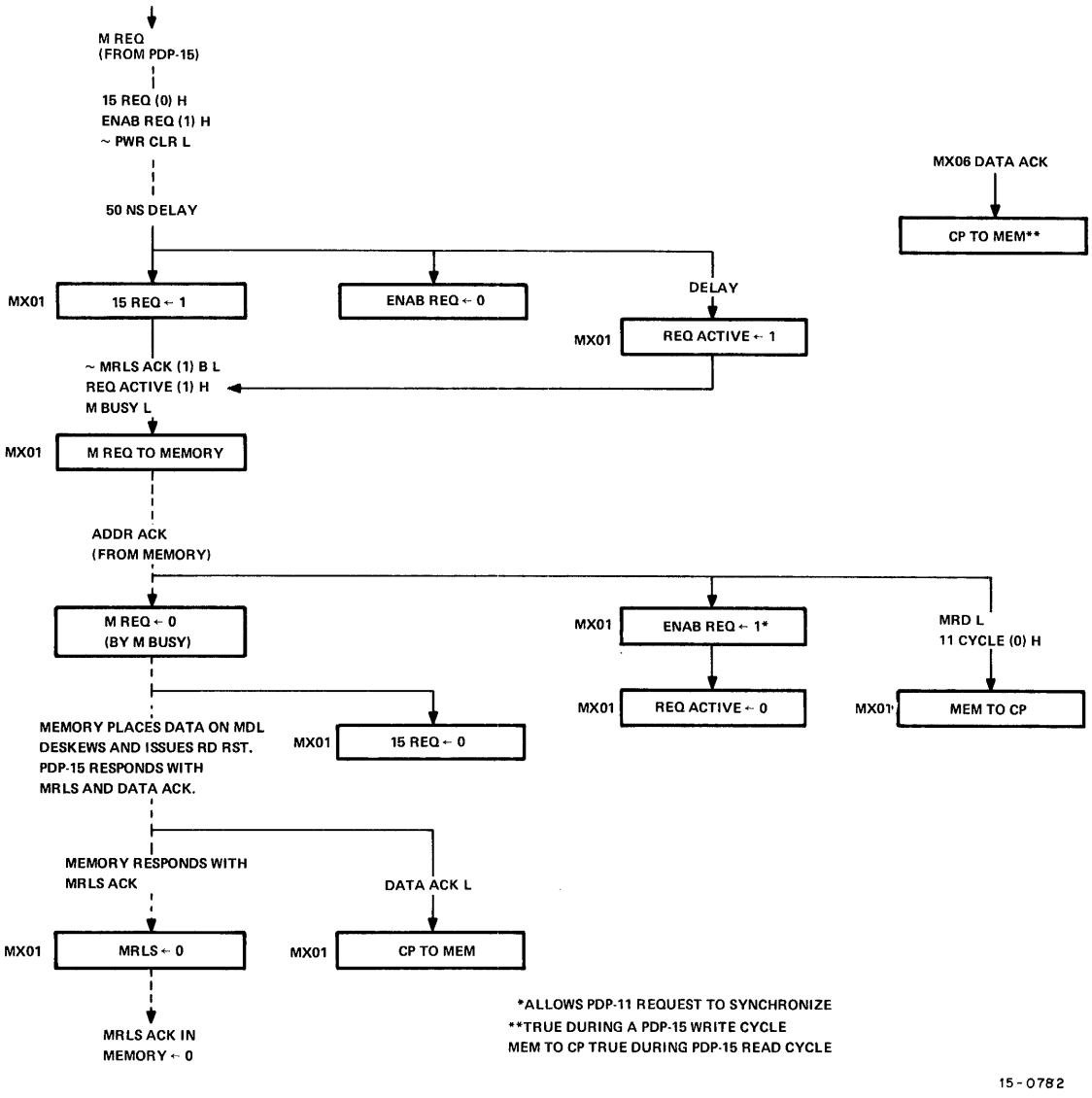


Figure 4-1 PDP-15 Read Cycle Flow Diagram

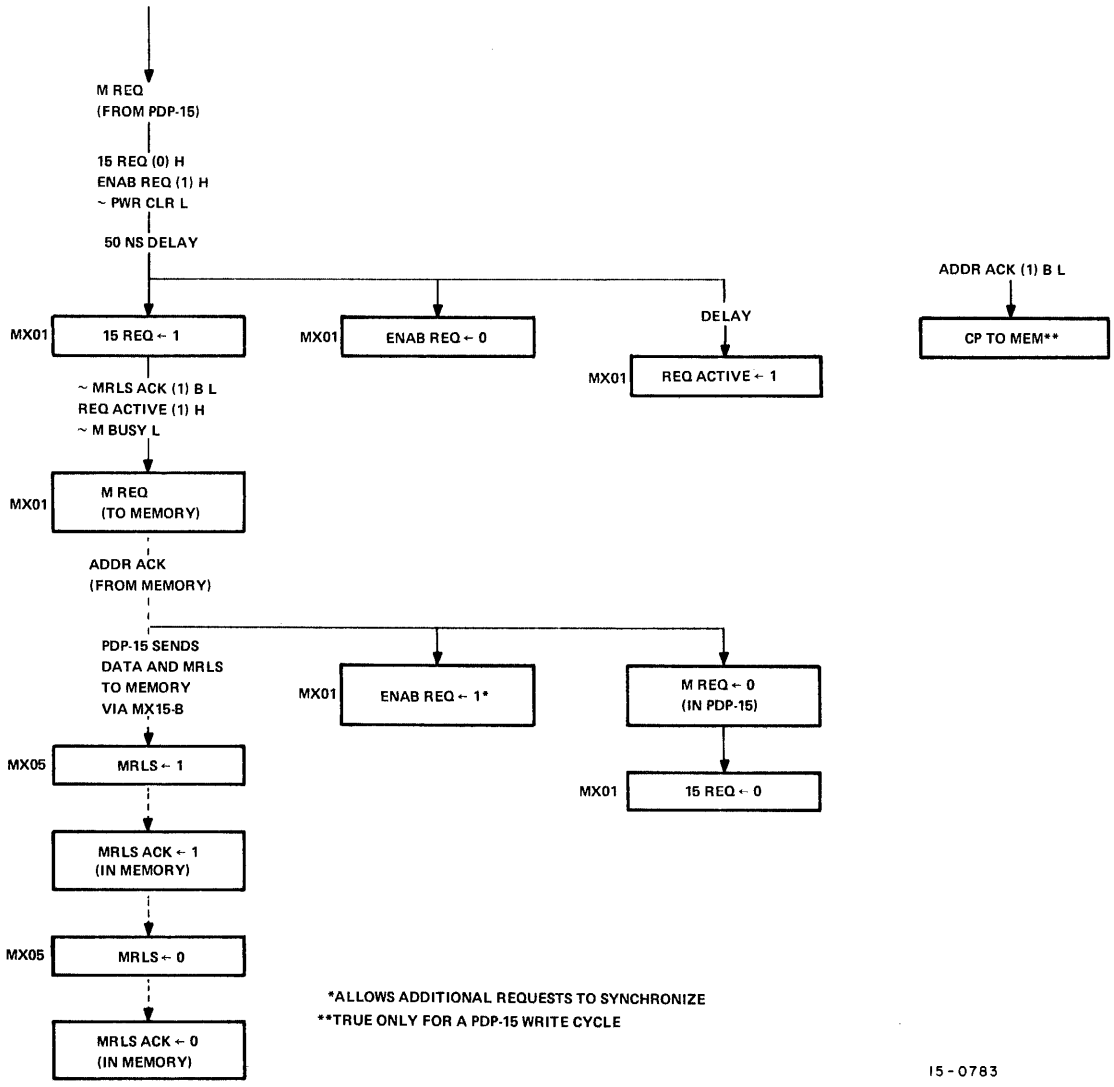


Figure 4-2 PDP-15 Write Cycle

After the data has stabilized, it is placed on the MDL accompanied by MRLS from the MX15-B. Upon receipt of the data, memory issues MRLS ACK. This signal clears MRLS in the processor. MRLS, going away, in turn clears MRLS ACK to complete the cycle.

4.2.1.4 PDP-15 Read-Pause-Write Cycle – The detailed flow diagram for the PDP-15 Read-Pause-Write cycle is shown in Figure 4-3. This flow is identical to the PDP-15 Read cycle until the time when RD RST is issued and memory places the data on the MDL (Paragraph 4.2.1.2). This represents the read portion of the Read-Pause-Write cycle.

Upon receipt of the data, the PDP-15 issues DATA ACK to memory to notify the memory that it has received the data and to remove it from the MDL. DATA ACK also directly resets a flip-flop which inhibits a MEM TO CP (read) transfer and enables a CP TO MEM (write) transfer (diagram MX15-B-01). This signal enables the M622 drivers on logic diagram MX15-B-05 for a CP TO MEM transfer.

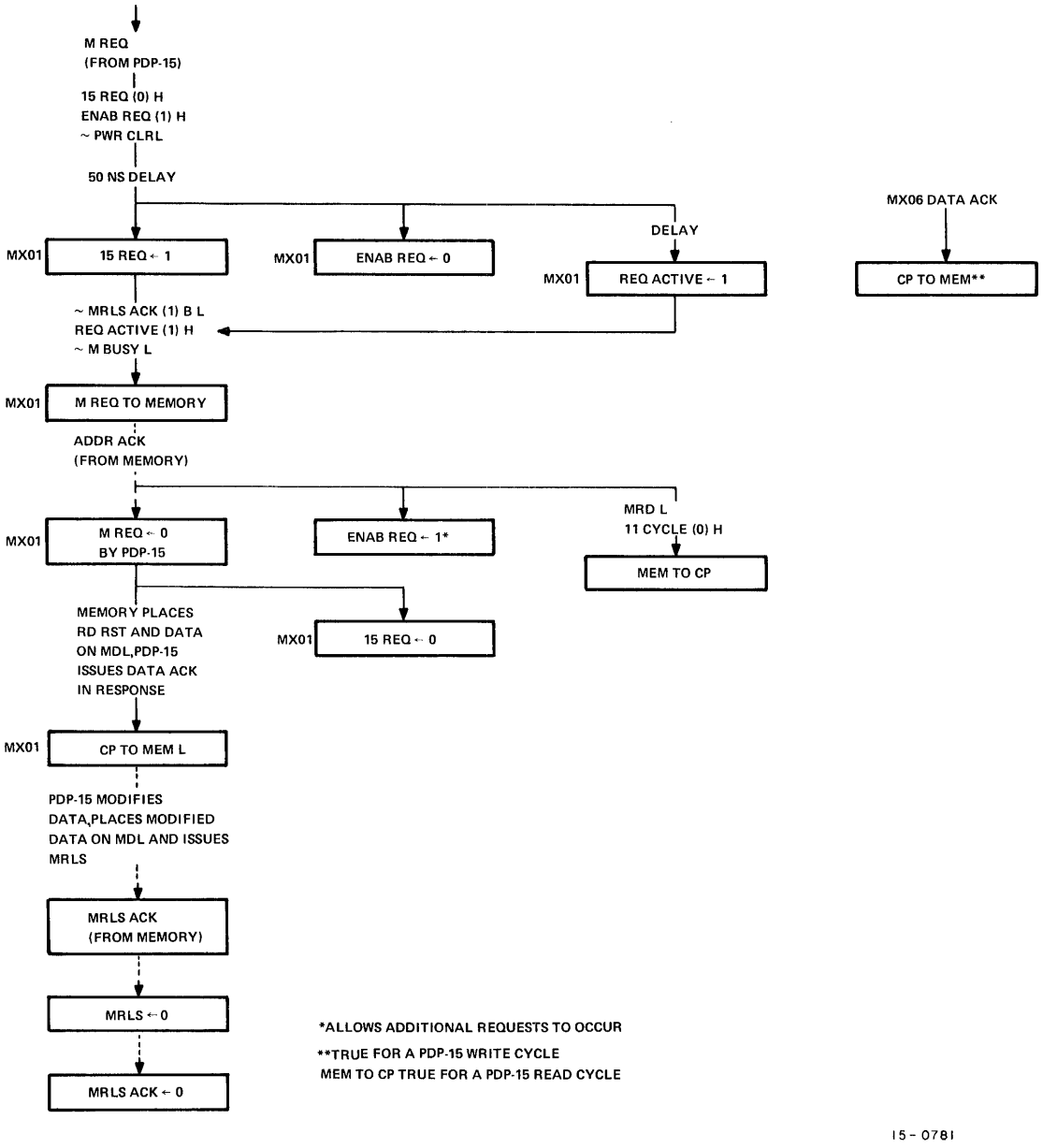


Figure 4-3 PDP-15 Read-Pause-Write Cycle

The PDP-15 modifies the data during the pause portion of the Read-Pause-Write cycle and, after the data has settled, places it on the MDL accompanied by MRLS. Upon receipt of the data, memory issues MRLS ACK. This signal clears MRLS which, in turn, clears MRLS ACK to complete the cycle.

4.2.1.5 PDP-11 Read Cycle – Figure 4-4 is a detailed flow diagram of the PDP-11 Read cycle. The PDP-11 Read cycle is initiated by MSYN from the PDP-11, provided the memory location to be read is not a local memory location or is not an I/O address (in other words, the address must normally lie between 4K and 124K or between 8K and 124K). If these conditions are met, MSYN is generated in the MX15-B.

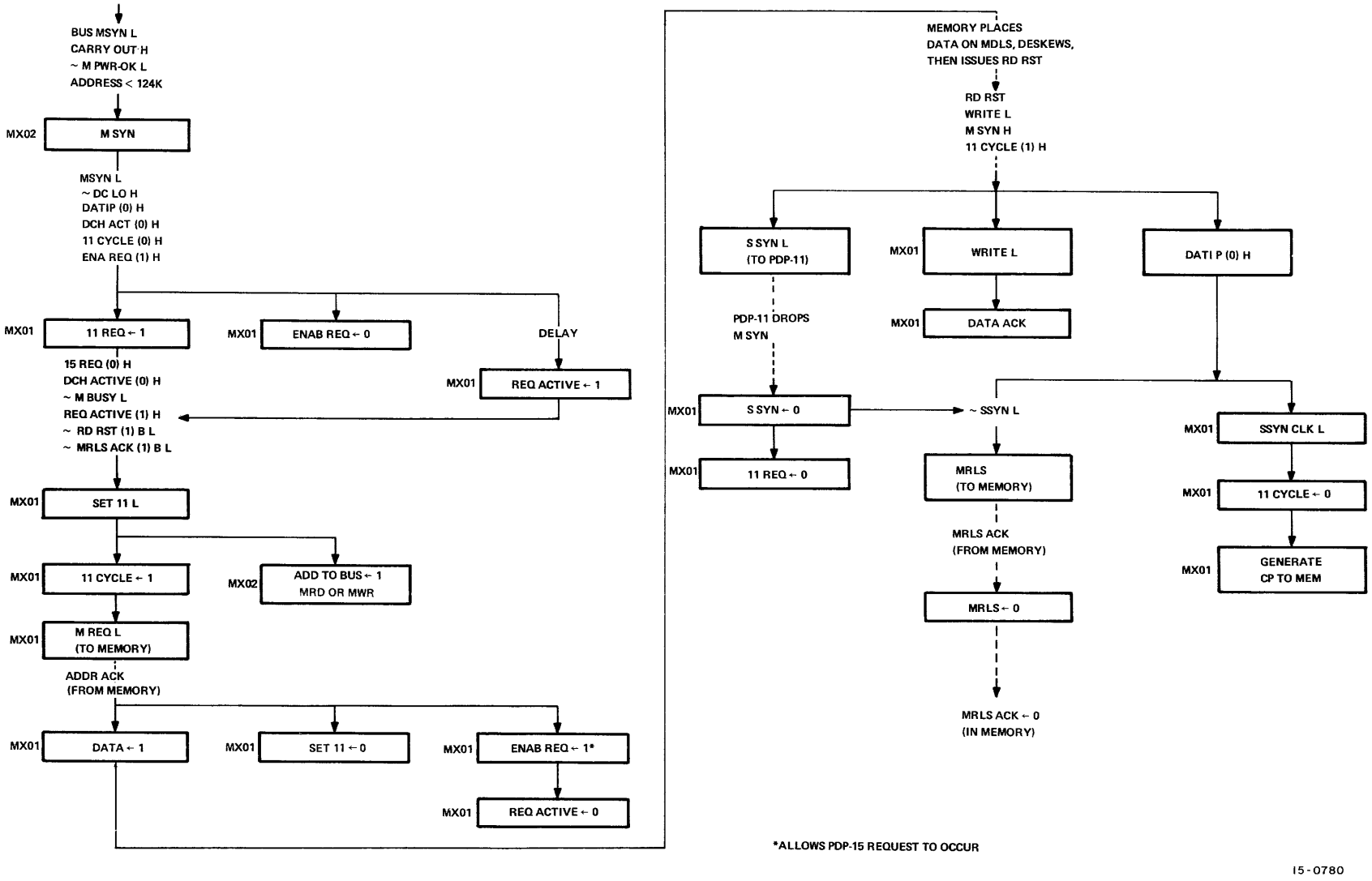


Figure 4-4 PDP-11 DATI Cycle Flow Diagram

Before a PDP-11 memory request can be honored, the 11 REQ flip-flop and the 11 CYCLE flip-flop must be set. In order to set the 11 REQ flip-flop, the following conditions are established:

a. DATIP (0) H – no DATIP cycle currently in progress

b. DCH ACT (0) H – no DCH cycle currently in progress by the PDP-15

c. 11 CYCLE (0) H – no PDP-11 cycle currently in progress

d. ENAB REQ (1) H – ADDR ACK has been received from memory and a new request can be synchronized

e. DC LO H – PDP-11 bus must be operative

In order to set the 11 CYCLE flip-flop, the following conditions are required:

a. 15 REQ (0) H – no PDP-15 request in progress

b. DCH ACTIVE (0) H – no DCH cycle in progress by the PDP-15

c. M BUSY L – memory is not busy

d. REQ ACTIVE (1) H – occurs as a result of delayed MSYN to allow the 11 REQ or 15 REQ flip-flop time to settle

e. RD RST (0) H – this signal must not be present in order to ensure proper communication with the PDP-15 memory

f. MRLS ACK (0) B H – this signal must not be present in order to ensure proper communication with the PDP-15 memory

NOTE

When the above conditions are met, SET 11 H is generated which sets 11 CYCLE indicating a PDP-11 memory cycle is in progress. SET 11 H also generates ADD TO BUS H, which enables the M621 drivers (MX15-B-03) to place the address of the memory location on the MDL.

In addition, an MRD (memory read) or MWR (memory write) signal must be sent to memory to indicate whether a read or write cycle is to be initiated. In this case, an MRD signal is sent to memory. MRD or MWR is generated as a result of the appropriate combination of C0 and C1 signals from the PDP-11. C0 and C1 are used to determine the direction of data transfer in the PDP-11 and are fed into a logic network on sheet MX15-B-02 to generate MRD or MWR.

With 11 CYCLE set, the MX15-B issues a memory request (M REQ L) and places the address on the MDL as described previously. Memory acknowledges receipt of the address with ADDR ACK, which performs the following three functions in the MX15-B.

a. Sets the DATA flip-flop to enable the MX15-B to accept data from the memory.

b. Stops the address from being sent to memory.

c. Sets the ENAB REQ flip-flop, which now will allow a PDP-15 request synchronization to occur.

Memory issues RD RST and places the data on the MDL. The MX15-B, upon receipt of RD RST, issues SSYN L to the PDP-11 (a read cycle, MSYN and 11 CYCLE still being true at this time). SSYN L causes the PDP-11 to drop MSYN which, in turn, causes the MX15-B to drop SSYN and to clear the 11 REQ flip-flop.

In addition, the MX15-B sends MRLS to memory to release it for further requests.

NOTE

When RD RST is received and SSYN is generated in the MX15-B, SSYN CLK is generated if the cycle is not a DATIP. The trailing edge of SSYN L clocks the DONE flip-flop to generate MRLS, and clears the 11 CYCLE flip-flop. The reset of 11 CYCLE generates ENAB 15 L to enable the PDP-15 memory drivers shown on sheet MX15-B-05.

Memory responds to MRLS with MRLS ACK. This signal clears MRLS in the MX15-B which, in turn, clears MRLS ACK in memory. Since the cycle described is a PDP-11 Read cycle, Write is low, which causes DATA ACK to be sent to memory.

4.2.1.6 PDP-11 Write Cycle – Figure 4-5 is a detailed flow diagram of the PDP-11 Write cycle. The flow is identical to the PDP-11 Read cycle (Paragraph 4.2.1.5) until the time that ADDR ACK is issued from memory, indicating that the memory has the address to be written into. At this time, the MX15-B drops ADD TO BUS and sets the DATA flip-flop if a PDP-11 cycle is requested [11 CYCLE (1) H]. Setting the DATA flip-flop directs the MDL lines (via the M622 bus drivers on diagram MX15-B-03) for a processor-to-memory transfer. The ENA REQ flip-flop is also set by ADDR ACK to allow a PDP-15 memory request to synchronize.

After the data has had time to settle on the MDL, MRLS is issued. MRLS generates SSYN CLK and causes the MX15-B to issue SSYN to the PDP-11. The PDP-11, upon receipt of SSYN, drops MSYN, which, in turn, causes SSYN to drop. The trailing edge of SSYN clears the DATA and 11 CYCLE flip-flops. Upon receipt of MRLS, memory responds with MRLS ACK. MRLS ACK clears MRLS in the MX15-B, which, in turn, causes MRLS ACK to drop.

4.2.1.7 PDP-11 DATIP/DATO Cycle – The detailed flow diagram for the PDP-11 DATIP/DATO cycle is shown in Figure 4-6. This cycle is identical to the PDP-11 Read cycle (Paragraph 4.2.1.5) until 11 CYCLE and SET 11 are true. At this point, the address lines have settled, and the address and M REQ are sent to memory.

NOTE

ADD TO BUS is generated on diagram MX15-B-01 due to SET 11 H. SET 11 is combined with the C0 and C1 control signals to determine whether the memory request is a MRD or MWR function as shown on MX15-B-02. In addition, ADD TO BUS is ANDed with the fact that the cycle is not a read or write cycle to produce DATIP L. This signal direct sets the DATIP flip-flop.

Upon receipt of the address, memory issues ADDR ACK which sets the DATA flip-flop, indicating that the address has been accepted and the data portion of the cycle is initiated.

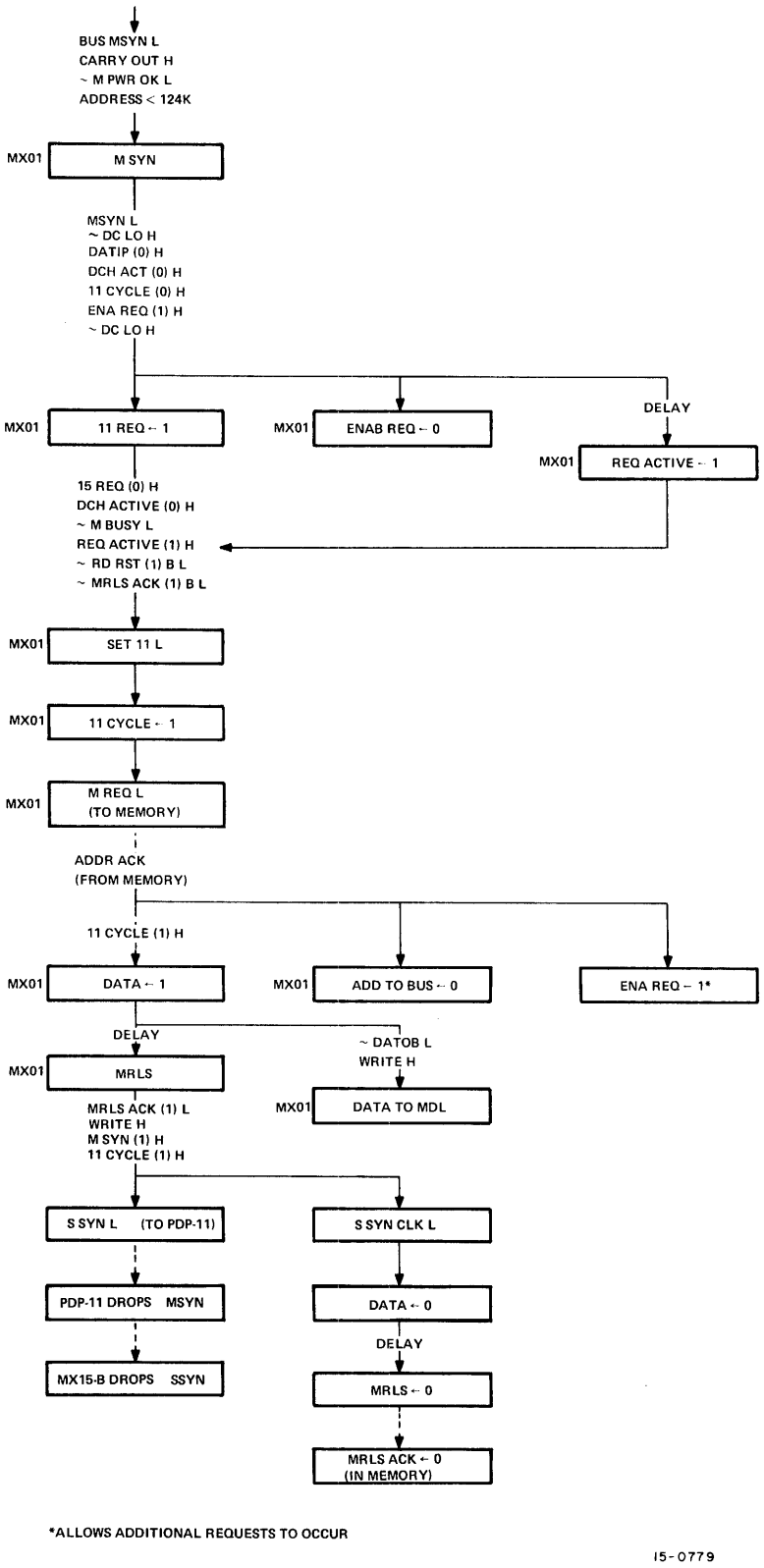


Figure 4-5 PDP-11 DATO Cycle Flow Diagram

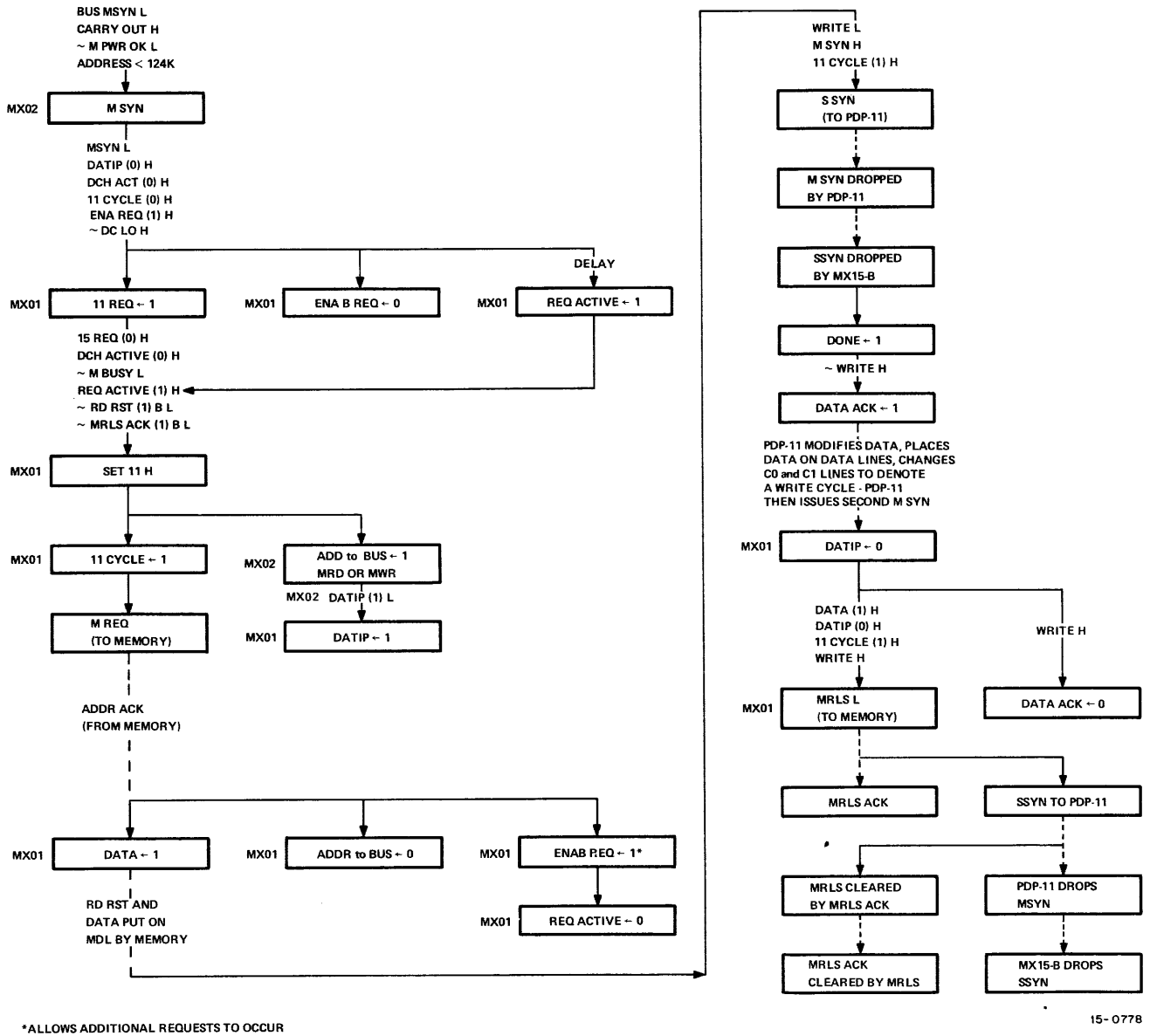


Figure 4-6 PDP-11 DATIP Cycle

DATA (1) H, BUS INIT L, and WRITE L are ANDed to generate MDL TO BUS to enable the MDL lines (diagram MX15-B-04). Also, ADDR ACK clears ADDR TO BUS to inhibit the address lines. Finally, ADDR ACK sets ENAB REQ and clears REQ ACTIVE to allow additional memory request synchronization from either processor. After the data lines have had time to deskew, memory issues RD RST and places the data on the MDL. Since WRITE L, MSYN, and 11 CYCLE (1) are high, SSYN is asserted and the data is sent to the PDP-11. The PDP-11 accepts the data and drops MSYN, which drops SSYN in the MX15-B. The PDP-11 modifies the data during the pause portion of the DATIP and changes the C0 and C1 lines to denote a Write cycle since the data must be written back into memory after being modified.

A second MSYN, which clears the DATIP flip-flop, is issued by the PDP-11. This flip-flop was unaffected by the first MSYN since the DATIP L was true and direct set the flip-flop. DATIP L is true due to the fact that control line C0 is low and control line C1 is high (MX15-B-02).

Since DATIP (0) is now true along with 11 CYCLE and WRITE, MRLS is generated and sent to memory. Memory responds with MRLS ACK which clears MRLS. The clearing of MRLS, in turn, clears MRLS ACK.

When the MX15-B issues MRLS, it also issues SSYN to the PDP-11. This causes MSYN to be cleared, which, in turn, forces the MX15-B to clear SSYN.

4.2.1.8 DATIP/DATOB Cycle – The PDP-15 does not perform byte operations and, thus, memory cannot be written into a byte at a time. Memory is written into 18 bits at a time. Hence, to perform a DATOB cycle in the PDP-15, it is necessary to simulate byte operations in the MX15-B logic. To accomplish this, a DATOB cycle is converted to a Read-Pause-Write cycle. During the cycle, the word is read out of memory and is transferred to a byte register in the MX15-B. The portion or byte of the word not to be modified by the PDP-11 is placed on the memory data lines from the MX15-B, while the portion of the word modified by the PDP-11 is placed on the memory data lines from the Unibus data lines. After the byte has been processed by the PDP-11 and both bytes (one byte from the MX15-B and one byte from the Unibus) are stable, a DATOB is performed in which both bytes are written back into memory.

Consequently, in a DATIP/DATOB cycle, the word is read out of memory and the appropriate byte is modified during the DATIP. During the DATOB, both bytes (modified byte from the Unibus and unmodified byte from the MX15-B) are written back into memory. A total of two PDP-11 bus cycles are required (Figure 4-6).

The DATIP/DATOB cycle is similar to the DATIP/DATO cycle until the point where the MX15-B drops the first SSYN (Figure 4-7). The following paragraphs describe a low byte operation from this point. The 18-bit word is read out of memory and is stored in a byte register in the MX15-B (Figure 4-8). The processor initiates the DATOB to write the low byte into memory. The signal which causes this action, LO DATA TO MDL H, is generated during a DATOB PDP-11 cycle if Address Bit 0 (ADDR BIT 0) is false.

The high byte, which is unaffected by the DATOB, is written back into memory from the MX15-B byte register. This action is caused by the signal designated HI BYTE TO MDL L. LO DATA TO MDL H and HI BYTE TO MDL L are used in conjunction with each other for a low byte operation. These signals are enabled during a PDP-11 DATOB as a result of the setting of the DONE flip-flop, which is set by the positive-going transition of SSYN.

NOTE

ADDR BIT 0 determines whether the DATOB is a low byte or high byte. If ADDR BIT 0 is true, a high byte operation is performed; if it is false, a low byte operation is performed.

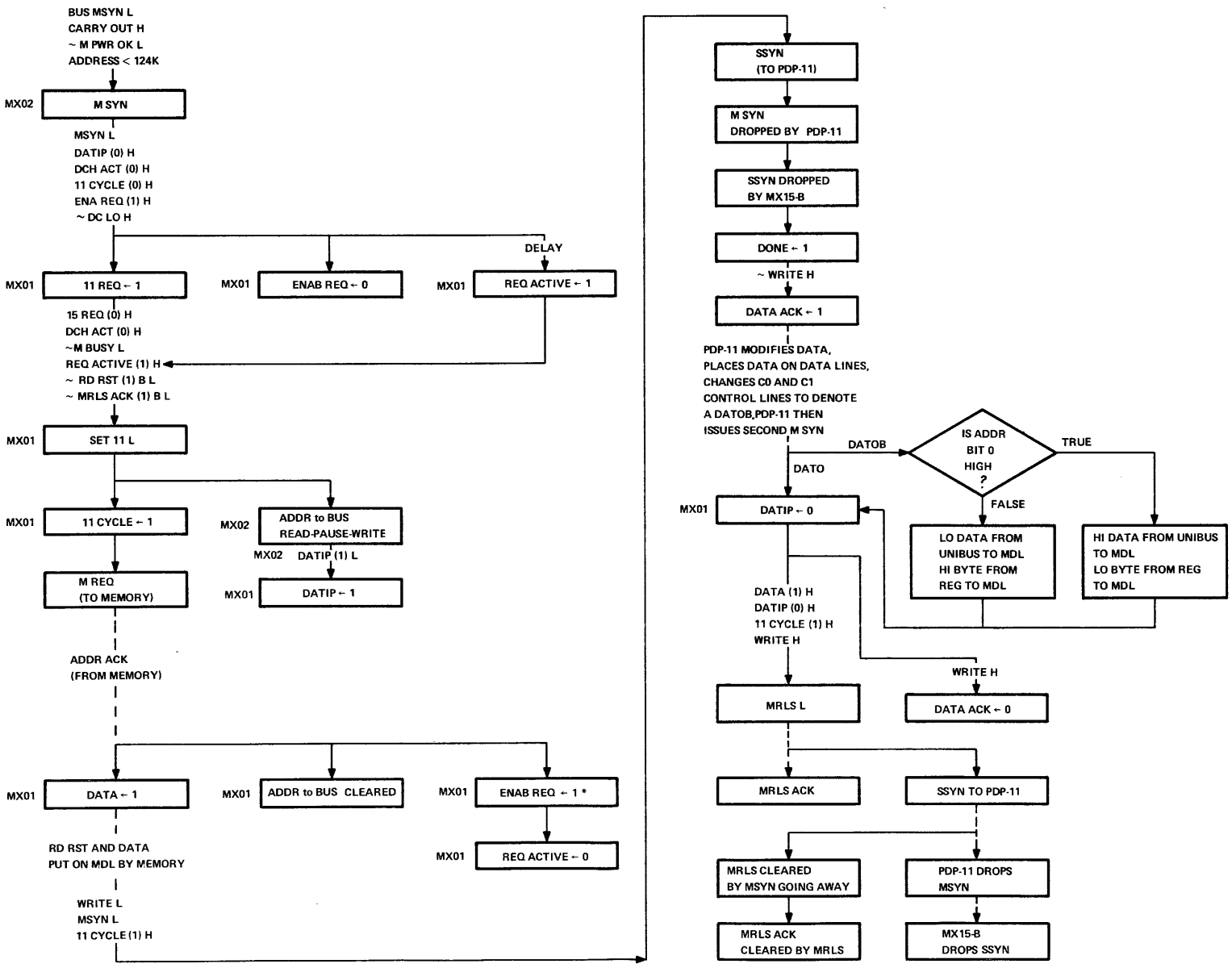


Figure 4-7 DATIP/DATOB Cycle

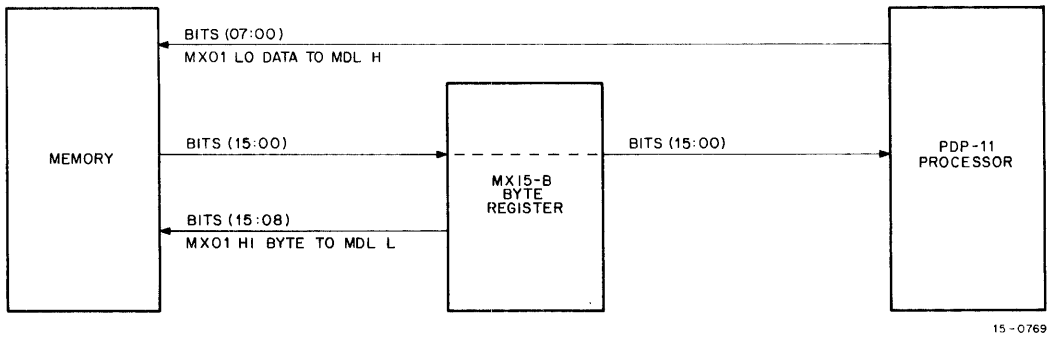


Figure 4-8 Low Byte Operation

If a high byte operation is performed, HI DATA TO MDL H causes the high byte to be written back into memory from the Unibus data lines and LO BYTE TO MDL L causes the data from the unmodified low byte to be written from the MX15-B register back into memory (Figure 4-9). HI DATA TO MDL H and LO BYTE TO MDL L are used in conjunction with each other to perform a high byte. As in the low byte, the positive-going transition from SSYN sets the DONE flip-flop which enables these signals.

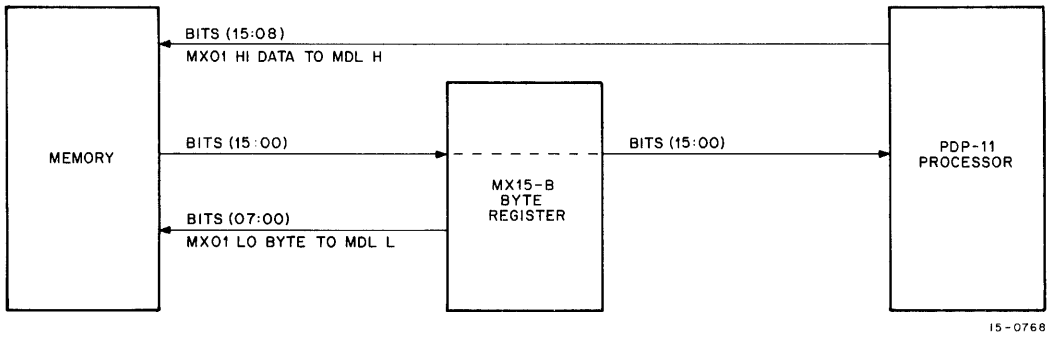


Figure 4-9 High Byte Operation

NOTE

The DATA flip-flop on drawing MX15-B-01 is inhibited from setting during a DATOB operation. If this flip-flop sets, DATA TO MDL L would be enabled and gate meaningless data onto the MDL.

4.2.1.9 PDP-11 DATOB Cycle – The PDP-11 DATOB cycle is similar to the PDP-11 DATIP/DATOB cycle (Paragraph 4.2.1.8) until the point where memory issues RD RST and places the data on the MDL. Figure 4-10 is a detailed flow diagram of the DATOB cycle.

NOTE

Since a DATOB is being performed, it is not necessary to set the DATIP flip-flop as in a DATIP cycle.

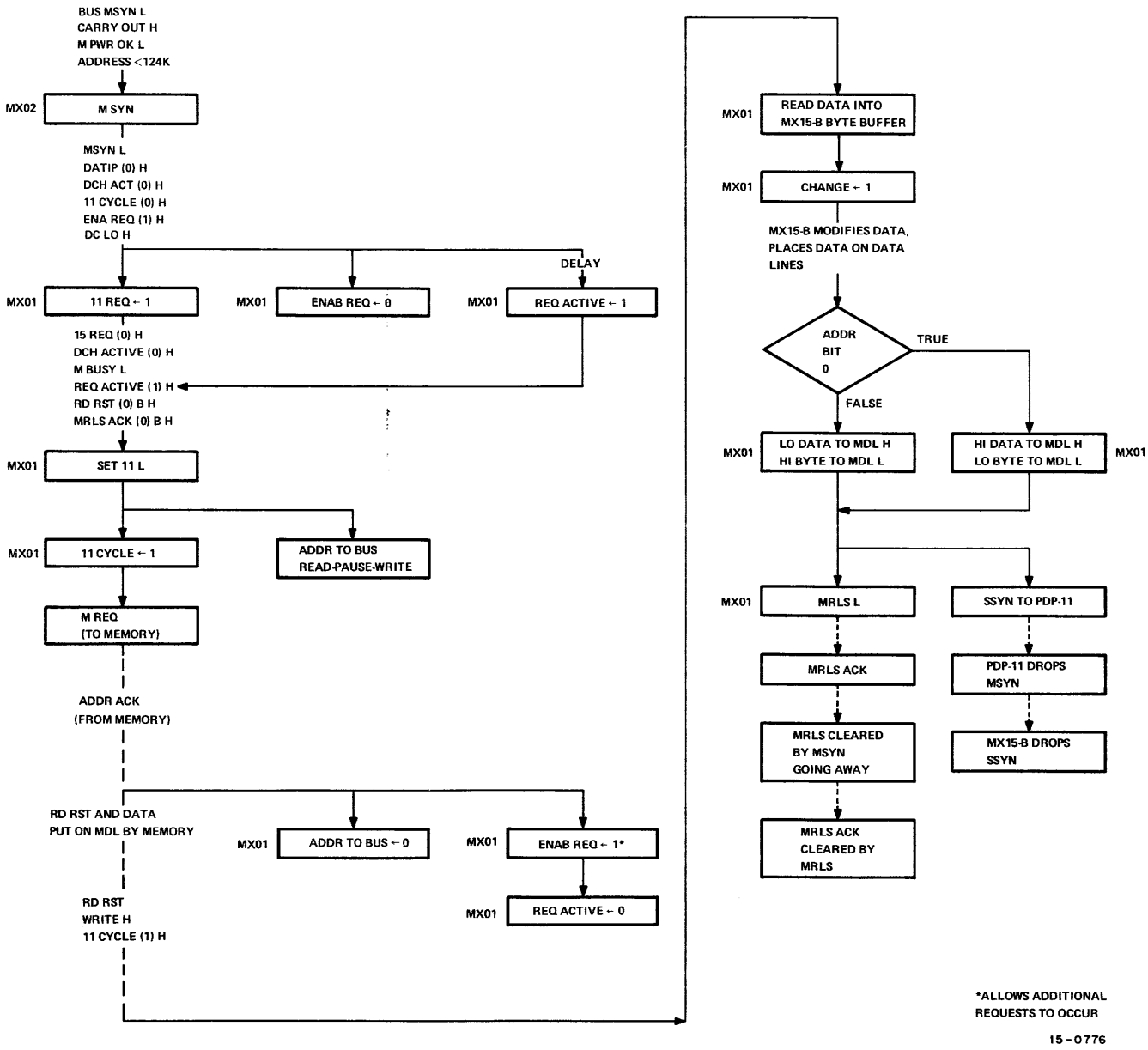


Figure 4-10 PDP-11 DATOB Cycle

At this point, the memory location has been addressed and the data is read out of memory into the MX15-B byte register. Although the C0 and C1 lines are encoded for a Write cycle, the read portion of a Read-Pause-Write operation is actually being implemented.

If ADDR BIT 0 is true, a high byte DATOB is performed. In this case, the low byte must be restored to the lower half of the memory location. A signal designated LO BYTE TO MDL L enables the lower half of the byte register (diagram MX15-B-08) to be written back into memory. The high byte is modified by the MX15-B as a result of the DATOB and is written back into memory by a signal designated HI DATA TO MDL H (diagram MX15-B-03). LO BYTE TO MDL L and HI DATA TO MDL H are used in conjunction with each other during a high byte operation and are both enabled by the setting of the CHANGE flip-flop during a PDP-11 DATOB cycle. This flip-flop is set by REG LOAD during a PDP-11 DATOB operation. REG LOAD is actually the inversion of RD RST (1) B L.

If ADDR BIT 0 is false, a low byte DATOB is performed. In this case, a signal designated HI BYTE TO MDL L causes the high byte to be written back into memory from the MX15-B byte register (MX15-B-08). The low byte is modified by the MX15-B and is written back into memory by a signal designated LO DATA TO MDL H (MX15-B-02). HI BYTE TO MDL L and LO DATA TO MDL H are used in conjunction with each other to perform a low byte operation. These signals are also enabled by the setting of the CHANGE flip-flop during a PDP-11 DATOB cycle.

Up to this point, the word has been read out of memory and the upper or lower portion (depending on ADDR BIT 0) has been modified. The entire word has been written back into memory and is accompanied by MRLS. Memory responds with MRLS ACK. MRLS ACK clears MRLS and MRLS, in turn, clears MRLS ACK. In addition, MRLS causes the MX15-B to issue SSYN to the PDP-11. This causes the PDP-11 to drop MSYN, which, in turn, causes the MX15-B to drop SSYN.

An important distinction to keep in mind as to the difference between a DATIP followed by a DATOB and a DATOB cycle is that two bus cycles are performed during a DATIP/DATOB, while only one memory cycle is performed in a DATOB. This is substantiated by noting the absence of SSYN after the word has been read out of memory and the absence of MSYN which would normally initiate the second memory cycle.

4.2.1.10 Power Clear Circuit – Power Clear in the UNICHANNEL 15 System can occur due to one of the following reasons.

PDP-11 Timeout – If MSYN from the PDP-11 goes away before ADDR ACK is returned from memory, the PDP-11 will time-out and cause a Power Clear to be generated.

NOTE

If either processor times out, a Power Clear is generated. This is built into the PDP-11/05. When automatically powering up in a "power fail" routine, it is important that there be a minimum 1 sec delay before attempting to access PDP-15 memory with the PDP-11/05.

MX15-B Marginal Power – If the voltage in the MX15-B drops below 4.7V, MX PWR-OK is produced and causes a Power Clear to be generated.

PDP-15 CAF Instruction – This instruction causes a power clear to the I/O bus.

PDP-15 Console Reset – When the PDP-15 console RESET pushbutton is depressed, the Reset pulse goes to memory and initializes memory to the power up state (Figure 4-11). Console RESET will generate power clear except when the PDP-11 is currently performing a memory cycle. Since both the PDP-11 and PDP-15 access the same memory asynchronously, Power Clear from the PDP-15 must be inhibited if the PDP-11 is performing a memory access.

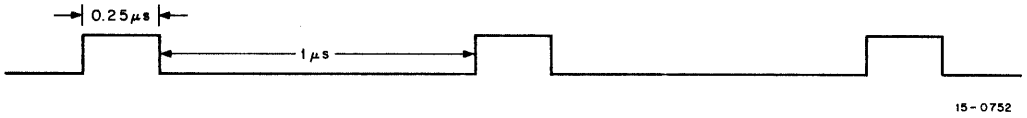


Figure 4-11 Console Reset Timing

This action is accomplished in the following manner. If MSYN is true and DC LO is not true (power is applied to the Unibus), the DISABLE PCL flip-flop is set (MX15-B-01) and disables further Power Clears until the PDP-11 memory cycle is completed or until the PDP-11 "times out." This allows convenient system initialization when a faulty PDP-15 program tries to access nonexistent memory, which hangs the bus and causes the PDP-11 to time-out.

4.2.2 11 ARRIVING Logic Diagram (MX15-B-02)

This diagram shows the Unibus receivers for bits 17 through 10. These receivers are used to gate address bits 17 through 10 onto the MDL. ADD TO BUS H is the enable signal used to gate address bits 17 through 10 onto the MDL. LO DATA TO MDL H is the enable signal used to gate data bits 17 through 10 (low byte) onto the MDL. Bits are routed to and from the MDL through various receivers and drivers. As an example, Figure 4-12 shows the various receivers and drivers associated with bit 10.

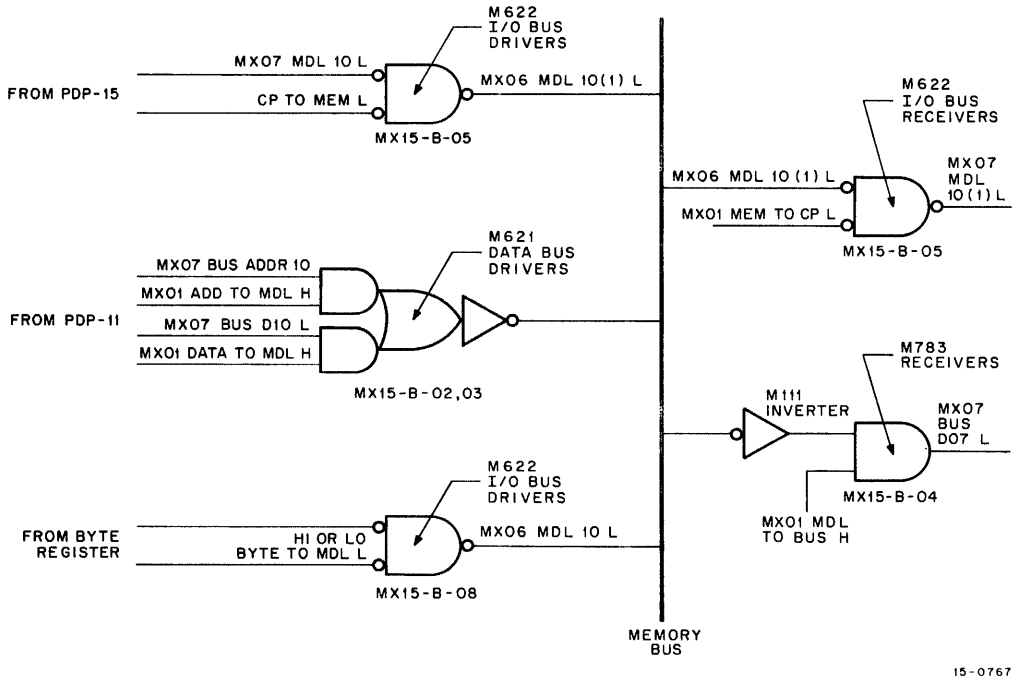


Figure 4-12 Bit 10 Memory Bus Drivers and Receivers

This diagram also shows the logic necessary to generate MSYN. Note that if bits 17 through 13 of the PDP-11 address are true, an address greater than 234K is indicated. All addresses greater than 124K are I/O addresses and inhibit MSYN from occurring. Figure 4-13 shows how bits 17 through 13 are decoded yielding 124K. Bit 0, which is the byte bit in the PDP-11, is not used.

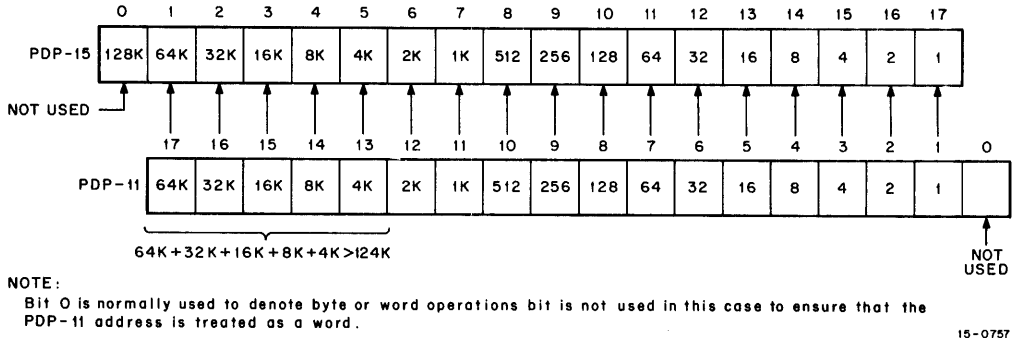


Figure 4-13 Decoding I/O Address

MSYN is also inhibited from occurring if PDP-11 local memory is being addressed. This is accomplished by CARRY OUT H. When this signal is low, local memory is being addressed and MSYN is inhibited. When the signal is high, common memory is being addressed and MSYN will occur.

The MRD and MWR functions are derived from the C0 and C1 control lines. For example, if both C0 and C1 are low, the inputs to pins T2 and U2 on B15 are high yielding DATOB L. WRITE L (at pin F2 of B11) and MWR L (at pin V2 of A16) are true indicating a write function. MRD L is inhibited by WRITE H. The specific combination of MRD and MWR denote the type of memory cycle as shown on diagram MX15-B-02. In this instance, a Clear/Write cycle is performed.

4.2.3 11 ARRIVING Logic Diagram (MX15-B-03)

This diagram shows the M784 Unibus receivers for PDP-11 bits 15 through 8. ADD TO BUS H is the enable signal used to gate address bits 9 through 0 onto the MDL. BUS D16 (MDL 01) and D17 (MDL 00) inputs are not utilized during byte operations.

4.2.4 UNIBUS DATA Logic Diagram (MX15-B-04)

This diagram shows the M783 Unibus drivers used to gate data from the MDL to the UNIBUS. The diagram also shows the G740 Jumper module and the M164 Parallel Adder module. These circuits are used to relocate the PDP-11 address so the PDP-11 can access common memory in those locations where common memory and local memory have the same addresses. This is necessary since the MX15-B Memory Multiplexer will not respond to addresses in local memory. For example, if the PDP-11 has 4K of local memory, the relocated addresses allow the PDP-11 to access 0 to 4K of common memory. This concept is shown in Figure 4-14. In order for the PDP-11 to access memory location 0 it addresses 8K. There is a two-fold reason why the address is relocated 8K. The address is first relocated by 4K to permit the PDP-11 to access 0 to 4K of common memory. A second relocation of 4K is provided due to the fact that memory locations are incremented by ones while PDP-11 addresses are incremented by 2. This second 4K relocation is actually accomplished by right-shifting the PDP-11 address, effectively dividing it by two. As a result, sequential PDP-11 addresses can access contiguous locations in common memory.

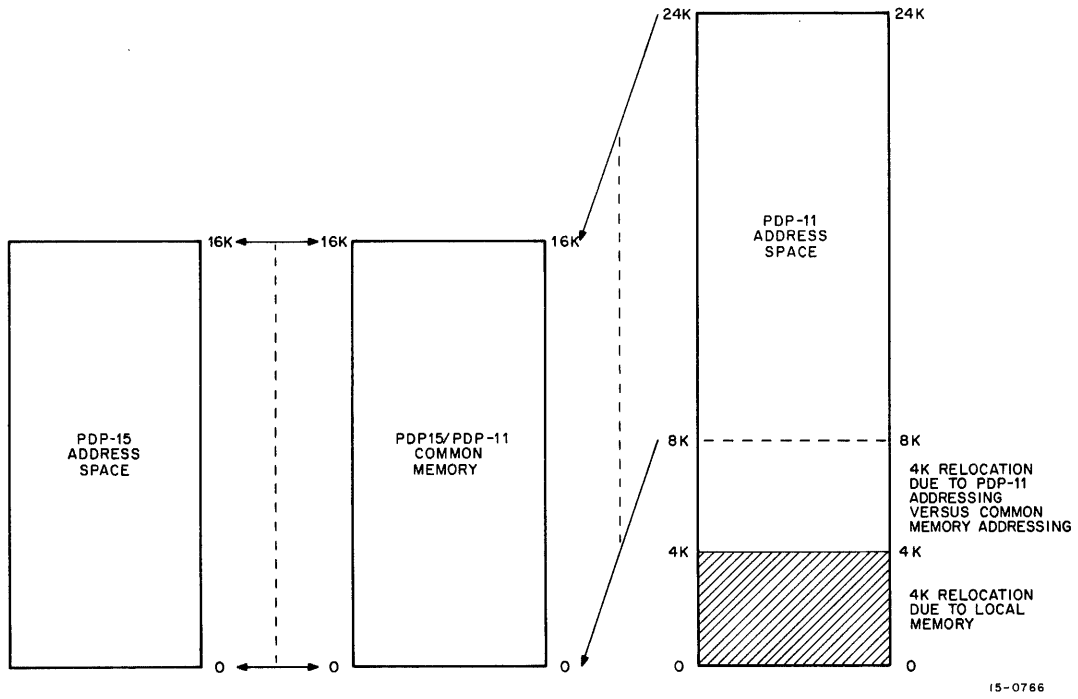


Figure 4-14 Common Memory Addressing Concept

Note that PDP-15 addresses address common memory locations on a one-to-one correspondence, with no relocation.

The following paragraphs describe how PDP-11 address relocation is implemented by the hardware. This involves a two-step process – to relocate the memory address due to the PDP-11 local memory and to provide for PDP-11 addresses (incremented by 2s) to sequentially access common memory (incremented by 1s).

The first step is accomplished by subtracting 1 from bits 17 through 13 of the address. Bit 13 represents 4K, as shown below, and subtracting 1 from bits 17 through 13 effectively subtracts a 4K block of addresses from 17 through 13. Bits 12 through 0 are appended to the address modified by the subtraction. These bits are not modified.

NOTE

Subtracting 1 from bits 17 through 13 is accomplished by adding 1 utilizing 2's complement addition. The 2's complement of 00001 is 11111. This subtraction is accomplished in the M164 Parallel Adder.

The partially modified address is placed on the Unibus address lines. When the address is sent to the memory address register, it is right-shifted one place, effectively dividing the address by two (Figure 4-15). The reason for this is that the PDP-11 addresses are incremented by two while the common memory locations are incremented by one. This right-shift of the address ensures that sequential PDP-11 memory addresses will access sequential memory locations.

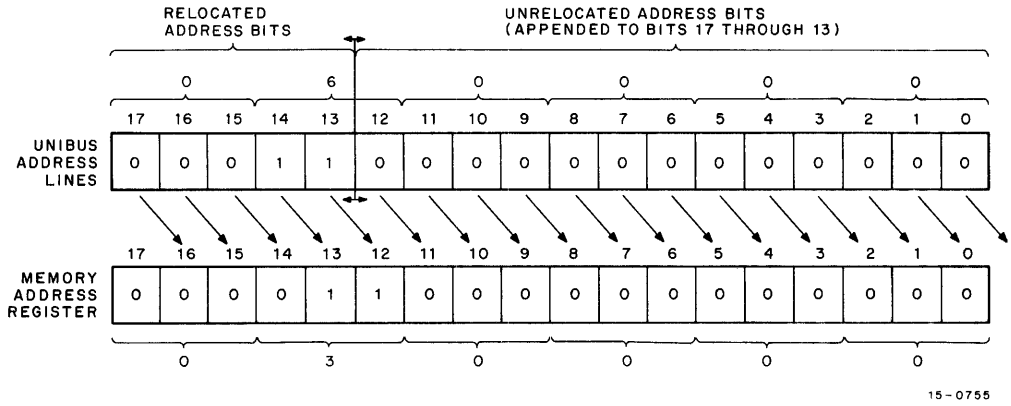
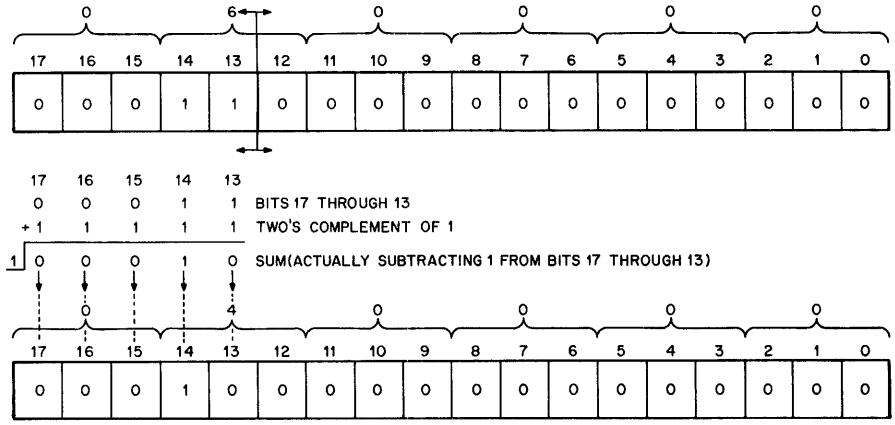


Figure 4-15 Right Shifting PDP-11 Memory Address

An example of PDP-11 address relocation is shown below.

Example: PDP-11 address = $60{,}000_8$. What memory location is accessed?

Step 1. Subtract 1 from bits 17 through 13.



Step 2. Right-shift modified address.

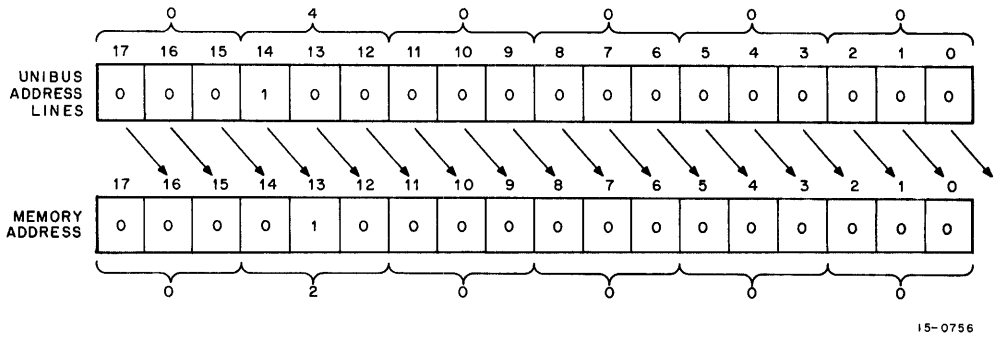


Figure 4-16 shows the entire relocation concept. For example, PDP-11 address 60,004 is relocated by 4K to 40,004, due to subtracting 1 from bits 17 through 13. Address 40,004 is right-shifted (divided by 2) yielding 20,002, which is the memory location that is accessed.

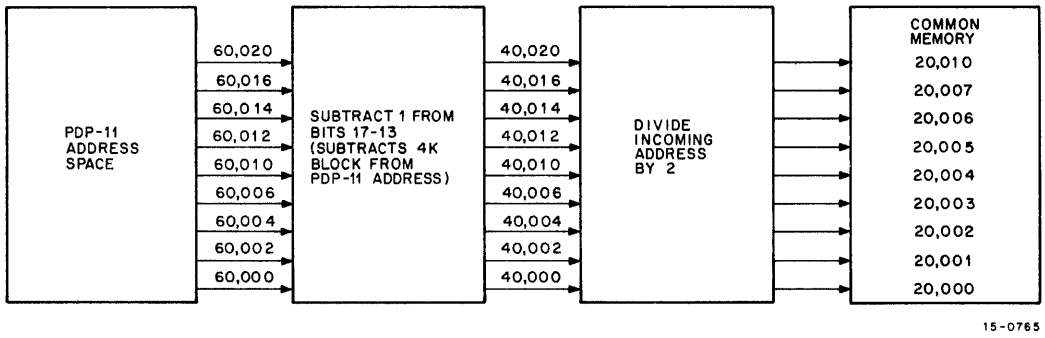


Figure 4-16 PDP-11 Address Relocation

If 8K of local memory is employed, a jumper on the G740 jumper module is cut for 8K. In this case, 2 is subtracted from bits 17 through 13 of the PDP-11 address. This effectively subtracts 8K from the PDP-11 address. This address is then divided by 2 to yield the desired address. Consequently, the relocation concept is the same except that a different number (2 as opposed to 1) is subtracted from bits 17 through 13.

4.2.5 15 PORT Logic Diagram (MX15-B-05)

This diagram shows the I/O bus drivers used to route data between memory and the PDP-15 Central Processor. Data is gated from memory to the PDP-15 by MEM TO CP L and is gated from the PDP-15 to memory by CP TO MEM L.

4.2.6 MEMORY BUS Logic Diagram (MX15-B-06)

This diagram shows the connections to the memory bus. The M904 is a single-size, double-sided coaxial cable connector. The M966 is a termination card.

4.2.7 PROCESSOR BUS Logic Diagram (MX15-B-07)

This diagram shows the connections to the PDP-15 and PDP-11 processors. The M904 and M966 modules are the same as used in the memory bus. The M920 module is a Unibus jumper module.

4.2.8 BYTE REGISTER Logic Diagram (MX15-B-08)

This diagram shows the 16-bit byte register. The register is clocked by REG LOAD. If the high byte is to be written back into memory, HI BYTE TO MDL L is generated; if the low byte is to be written back into memory, LO BYTE TO MDL L is generated.

CHAPTER 5
INSTALLATION

5.1 GENERAL

This chapter describes installation of the UC15 System. A list of recommended spare parts is also provided.

5.2 INSTALLATION

The UC15 System can be operated from 115 or 230 Vac ± 10%, single-phase, 50 or 60 ± 2 Hz. The primary power line must terminate in Hubbell wall receptacles, or their equivalent, to be compatible with the power line connector (Figure 5-1). The PDP-15 cabinet should be grounded to the building power transformer ground or the building ground point. Dimensions and service clearances for the UC15 System are shown in Figure 5-2.

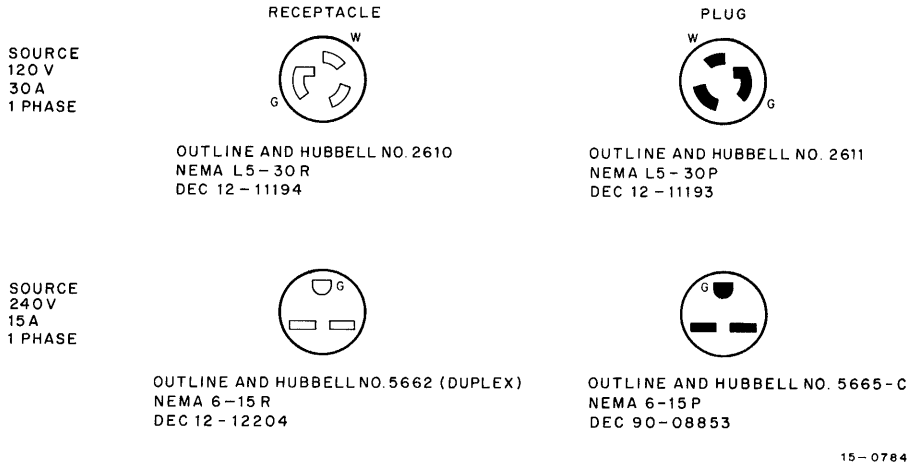


Figure 5-1 Hubbell Wall Receptacle Connector Diagram

5.2.1 Unpacking

The equipment may arrive as a complete system or as an add-on. Use the following procedure to unpack and position the cabinet.

1. Remove the outer shipping container, which may be either heavy corrugated cardboard or plywood. Remove all straps first, and then any fasteners and cleats securing the container to the skid. Remove any wood framing and supports.

2. Remove the polyethylene covers from all cabinets.

3. Remove the tape or plastic shipping pins from the rear access doors.

4. Unbolt the cabinets from their shipping skids. The bolts can be reached through the rear doors.

5. Raise the leveling feet so that they are above the level of the roll-around casters.

6. Form a ramp with wooden blocks and planks from each cabinet skid to the floor, and roll each cabinet down this ramp.

7. Roll the system to its proper location.

5.2.2 Cabinet Installation

In multiple cabinet installations, cabinets are shipped either individually or in pairs. These cabinets should be connected together at the site. To install the cabinets, use the following procedure.

1. Cabinets are joined by filler strips (Figure 5-3). After the cabinets are positioned, put the cabinets together and bolt both filler strips and cabinets together. Do not tighten the bolts securely.

2. Lower the leveling feet until they support the cabinet. Using a spirit level, check that all cabinets are level and that the feet are firmly against the floor.

3. Tighten the bolts that hold the cabinets together and again check the leveling feet.

4. Run a ground strap from the UC15 cabinet to the PDP-15 cabinet.

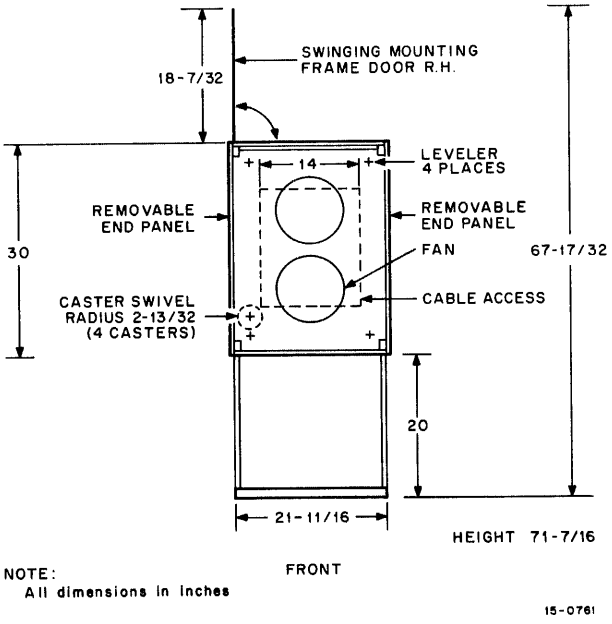


Figure 5-2 The UC15 Cabinet

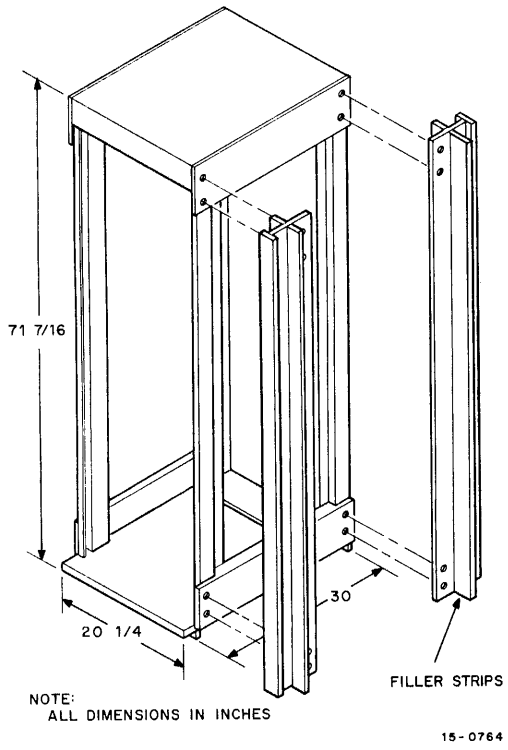


Figure 5-3 Cabinet Bolting Diagram

Figure 5-4 shows a typical UC15 installation configuration. Normally, the UC15 cabinet is bolted to the left side of the KP15 cabinet. Additional cabinets containing PDP-11 peripherals normally connect to the left side of the left-most cabinet (Figure 5-5a). If the PDP-15 system has extended memory cabinets, the UC15 cabinet should be positioned between the KP15 cabinet and the memory cabinet.

An optional cabinet configuration such as that shown in Figure 5-5b may be employed.

5.2.3 Visual Inspection

Visually inspect the items listed below.

1. Verify that all modules have been configured in accordance with the DR15-C and MX15-B module utilization list.

2. Ensure that all modules have been seated firmly in the system unit.

3. Inspect backplane wiring for broken wire or damaged pins. Repair or replace as required.

4. Ensure that the power cable is firmly attached to the correct fast-on tabs on the system unit backplane and that the Mate-N-Lok connector is firmly seated in the power distribution panel on the chassis.

5. Check the air filters at the top of the cabinet.

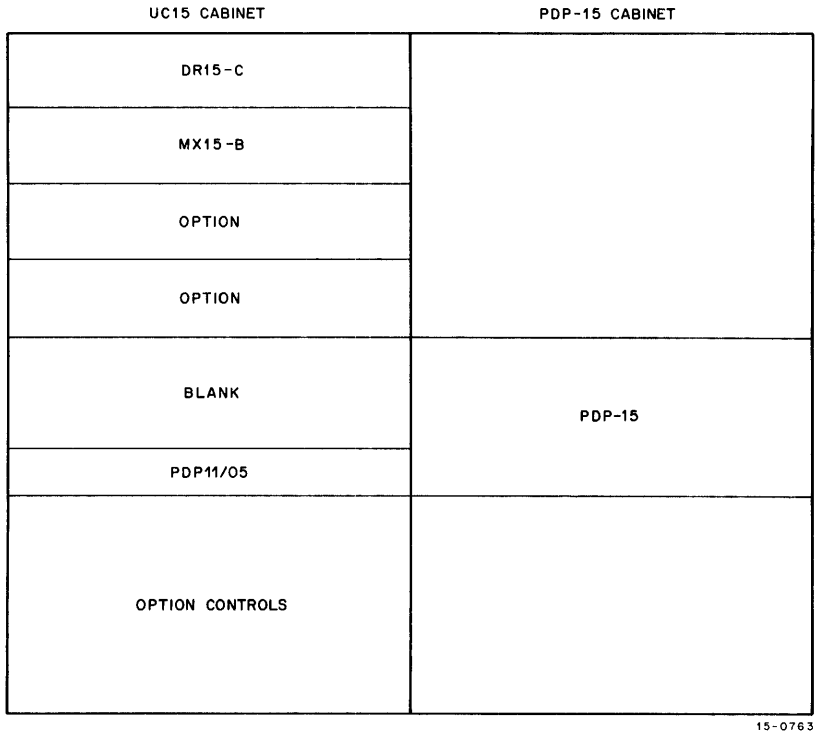
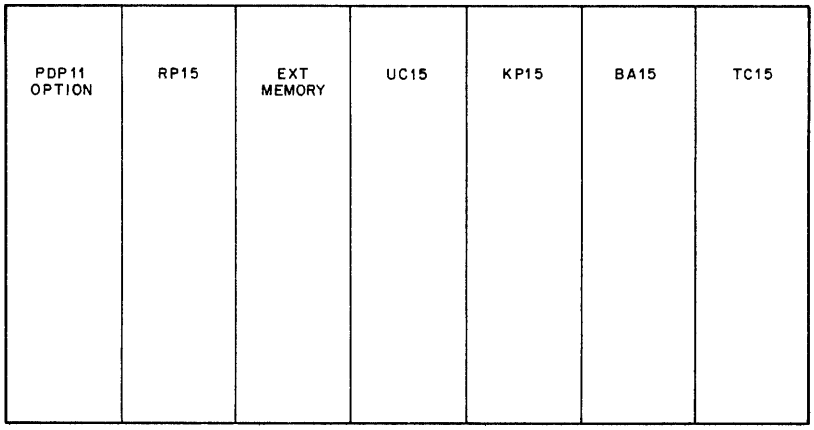
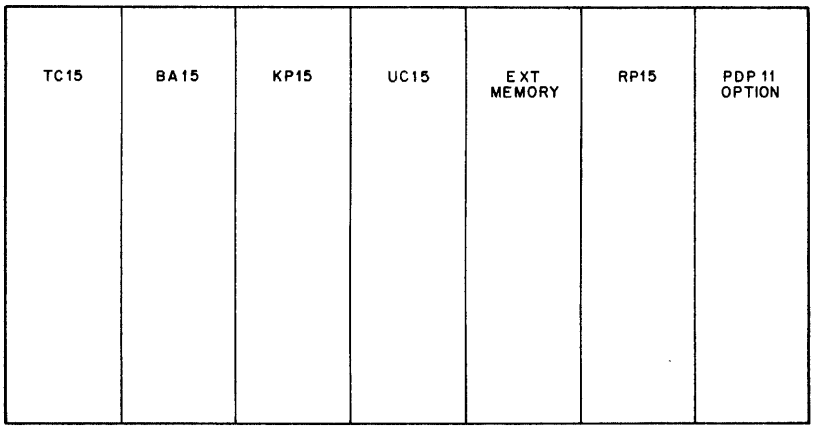


Figure 5-4 Typical UC15 Installation



a. Standard Configuration



b. Optional Configuration

15-0762

Figure 5-5 Cabinet Configurations

5.2.4 Electrical Installation

To power up the system, use the following procedure:

1. Connect the MDL, Unibus, and I/O bus cables as outlined in the configuration specification.

2. If there is an additional cabinet containing other PDP-11 peripherals, connect the Unibus between the cabinets.

3. Ensure that the MDL, Unibus, and I/O bus cables are terminated properly.

4. Check the G720 module and cut the jumpers for the amount of local memory desired (logic diagram MX15-B-05). Also, add jumper wires as shown in in note on logic diagram DR15-C-08.

5. If an MX15-A is connected to the MDL output cables, install ECO MX15-0007.

6. Connect remote power cord to the cabinet to the immediate right of the UC15 cabinet (this is normally the cabinet that houses the PDP-15).

7. Connect the ac power cord to the receptacle provided.

NOTE

After checking all cables, power up the PDP-15. At this time, power is applied to the MX15-B and DR15-C.

8. Check cabinet fans for proper operation.

9. Check +5 Vdc in the MX15-B Memory Multiplexer and the DR15-C Device Interface.

10. Power up the PDP-11/05 by turning the console Power switch to ON.

11. Check and adjust the PDP-15 processor clock for the correct cycle time. Write into the memory furthest from the PDP-15 using a DAC instruction. With an oscilloscope, sync CHANNEL A negative on CP WR ADR ACK located on F12 J2 and record time of positive transition of MRLS ACK on F28 D2 using CHANNEL B. With CHANNEL B, record the time of the negative transition of TS01* PH02 (H31N1). TS01* PH02 should occur at least 50 ns after MRLS ACK. If necessary, adjust the CP clock located on E30 to obtain a 50 ns window.

12. Once all cabinets have power applied, start customer acceptance procedure.

5.3 FIELD ADDITIONS TO UC15 SYSTEM

The UC15 is normally configured as an RK15 Disk System with an RK11-E Disk Controller mounted in special hardware below the PDP-11/05 processor.

When additional PDP-11 family options are mounted in the UC15 cabinet, a BA11 expander box may be installed below the PDP-11/05 processor. In these cases, perform the following steps.

1. Remove the RK11-E mounting frame, cooling assembly, and power wiring.

2. Mount the RK11-E inside the BA11 expander box with the other PDP-11 family options.

CHAPTER 6
MAINTENANCE

6.1 GENERAL

The maintenance philosophy employed in the UC15 System is to utilize diagnostic programs for isolating malfunctions and initiating corrective action. Individual diagnostics exist for both the PDP-15 and PDP-11 systems. These diagnostics are useful when malfunctions are isolated to a specific unit.

6.2 VISUAL INSPECTION

Before the diagnostics are run, the following visual inspection should be made.

1. Verify that all modules have been configured correctly in accordance with the DR15-C and MX15-B module utilization list.

2. Ensure that all modules have been seated firmly in the system unit.

3. Inspect backplane wiring for broken wires or damaged pins. Repair or replace as required.

4. Ensure that the power cable is firmly attached to the correct fast-on tabs on the system unit backplane and that the Mate-N-Lok connector is seated firmly in the power distribution panel on the chassis.

5. Clean air filters at top of cabinet.

6. Ensure that the MDL, Unibus, and I/O bus cables are terminated properly.

7. Check cabinet fans for proper operation.

8. Check +5 Vdc in the MX15-B Memory Multiplexer and the DR15-C Device Interface.

6.3 DIAGNOSTIC MAINTENANCE

A PDP-15 System Exerciser, provided with the system, allows the PDP-15 peripherals to be operated, the PDP-11 peripherals to be operated, or both PDP-15 and PDP-11 peripherals to be operated simultaneously. This diagnostic program is useful in isolating trouble to a particular unit and uncovers problems not readily apparent from normal diagnostics. These problems include bus conflicts, bus interference, or intermittent memory.

The UC15 diagnostic is employed to exercise common memory and the DR15-C/DR11-C Interrupt Link.

In order to isolate a malfunction to a particular unit in a dual-processor system such as the UC15, the following steps serve as a useful guide.

1. Use the DEP and EXAM switches on the PDP-11 to determine if the PDP-11 can access common and local memory.

2. If common and local memory cannot be accessed, remove devices from the Unibus to isolate the problem to either a device or the processor.

3. If only local memory can be accessed, the following short program may facilitate troubleshooting a write operation.

Write

```
500  START   MOV #700, R6        /INITIALIZE R6
             MOV R0, @ #41000    /IF TIMEOUT, TRAP TO LOCATION 4 WHICH CONTAINS 500
             BR START            /BRANCH TO START
4    TV      500
```

If only local memory can be accessed, the following program may facilitate troubleshooting a read operation.

Read

```
500  START   MOV #700, R6        /INITIALIZE R6
             MOV @ #41000, R0    /IF TIMEOUT, TRAP TO LOCATION 4 WHICH CONTAINS 500
             BR START            /BRANCH TO START
4    TV      500
```

4. Use the DEP and EXAM switches on the PDP-15 to determine if the PDP-15 can access common memory.

NOTE

If both processors can access common memory, it is probable that the MX15-B is operating correctly.

5. Do a JMP instruction with the PDP-15 to see if the PDP-15 can loop.

6. Do a BR. instruction in common memory with the PDP-11 to see if the PDP-11 can branch.

NOTE

If both processors continue to run, it is probable that the MX15-B is capable of alternating memory cycles between the two processors.

7. Load and run the UC15 diagnostic to exercise the memory/multiplexer link and to exercise the DR15-C/DR11-C Interrupt Link. This diagnostic performs a rigorous exercise of the DR15-C and the MX15-B. Detailed loading instructions are provided in the diagnostic listing. If there is a problem in the interrupt link, the DR11-C diagnostic should be run to localize the problem to the DR11-C or the DR15-C.

8. Load and run the system exerciser. Run all PDP-15 devices and determine if the PDP-15 is operating correctly. Run all PDP-11 devices and determine if the PDP-11 is operating correctly. Finally, run both PDP-15 and PDP-11 devices simultaneously. If a particular device proves inoperative, run the diagnostic associated with that device.

NOTE

In order to load any PDP-11 diagnostic, the ABSL 11 loader tape must be loaded (starting address 17720_8). When this is loaded, load the diagnostic in the paper-tape reader and press the CONTINUE button on the PDP-15. When the PDP-15 stops, load address 100000 in the PDP-11 and press the START button. When the PDP-11 stops, the program has been relocated into PDP-11 local memory. To obtain a typeout from the program, disconnect the PDP-15 TTY (Teletype) console and reconnect it to the PDP-11. Connect the jumper plug (7009195) to the PDP-15 console TTY lines. This prevents constant TTY interrupts from occurring and allows the paper-tape reader to operate.

9. For further testing, run the individual unit diagnostics as required.

6.4 TEST EQUIPMENT

The following test equipment is needed.

a. Oscilloscope – general purpose

b. Multimeter – Triplett or equivalent

c. Two Oscilloscope probes

d. Two double-height module extenders

e. Various hand tools

f. KM11 Maintenance Panel

6.5 RECOMMENDED SPARES

Table 6-1 is a list of recommended spares for the UC15 System.

Table 6-1
Recommended Spares

Module		Number Required
Type	Name	
M103	Device Selector	1
M104	I/O Bus Multiplexer (API)	1
M111	Inverter	1
M112	NOR gates	1
M113	NAND gates	1
M115	NAND gates	1
M133	Input NAND gates	1
M135	NAND gate	1
M161	Binary/Decimal Decoder	1
M164	6-Bit Adder	1
M216	D-type Flip-Flop	1
M246	D-type Flip-Flop	1
M311	Tapped Delay Line	1
M312	Delay Line	1
M510	I/O Bus Receiver	1
M611	Power Inverter	1
M621	Data Bus Driver	1
M622	Positive Input/Output Bus Driver	1
M627	NAND Power Amplifier	1
M688	UNIBUS Power Fail Driver	1
M783	UNIBUS Drivers	1
M784	UNIBUS Receivers	1
PDP-11/05	Spares Kit	1
M7860	General Device Interface (DR11-C)	1

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DEC-15-HUCMA-B-D

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