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TITLE: MICROPROCESSOR, CMOS, 12-BIT PARALLEL (6120)

1. GENERAL DESCRIPTION

This specification defines the detail requirements for a 40 pin single address, fixed word length, parallel transfer microprocessor using 12-bit, two's complement arithmetic. The processor recognizes the instruction set of Digital's PDP8-E minicomputer. The internal circuitry is completely static and is designed to operate at any speed between DC and the maximum operating frequency. Two pins are available to allow for an external crystal, thereby eliminating the need for clock generators and level translators. The crystal can be removed and the processor clocked by an external clock generator.

2. APPLICABLE DOCUMENTS (Per latest revision on date of order):

Digital Equipment Corporation (Digital)

A-PS-2100002-GS Integrated Circuits General Specification For

3. REQUIREMENTS

3.1 Mechanical:

3.1.1 Material: Dual-In-Line Plastic Package (DIP), Per A-PS-2100002-GS.

3.1.2 Configuration/Dimensions: 40 Pin Package Per A-PS-2100002-GS.

3.1.3 Pin Identification, Symbol, Active Level and Description: Per Figure 1.

3.2 Electrical: Per A-PS-2100002-GS and parameters specified herein.

3.2.1 Summary of Memory Reference Instructions: Per Table I.

3.2.2 Group 1 Operate Instructions: Per Table II.

3.2.3 Group 2 Operate Instructions: Per Table III.

3.2.4 Group 3 Operate Instructions: Per Table IV.

3.2.5 Programmed I/O Control Lines: Per Table V.

3.2.6 Main Memory Control Instructions: Per Table VI.

3.2.7 Memory Extension Instructions: Per Table VII.

3.2.8 Panel Mode Control Instructions: Per Table VIII.

3.2.9 Definition of 6120 Flag Bits and Miscellaneous Outputs: Per Table IX.

3.2.10 Absolute Maximum Ratings: Per Table X.

3.2.11 Electrical Characteristics: Per Table XI.

3.2.12 Capacitance Data: Per Table XII.

3.2.13 Switching Characteristics: Per Table XIII.

3.2.14 Memory Read Operation: Per Figure 3.

3.2.15 Memory Write Operation: Per Figure 4.

3.2.16 Memory Read, Modify, Write Operation: Per Figure 5.

3.2.17 External IOT Operation: Per Figure 6.

3.2.18 OR Switch Register (OSR): Per Figure 7.

3.2.19 Write to Switch Register: Per Figure 8.

3.2.20 Basic OPR Instruction Format: Per Figure 9.

3.2.21 Block Diagram: Per Figure 2.

3.2.22 Group 1 Microinstruction Format: Per Figure 10.

3.2.23 Group 2 Microinstruction Format: Per Figure 11.

3.2.24 Group 3 Microinstruction Format: Per Figure 12.

3.2.25 IOT Instruction Format: Per Figure 13.

3.3 Performance: Per A-PS-2100002-GS and parameters specified herein.

3.3.1 Basic Functional Block Diagram Description (See Figure 2).

3.3.1.1 Major Registers:

3.3.1.1.1 Accumulator (AC): The AC is a 12-bit register with which arithmetic and logical operations are performed. Data words may be fetched from memory to the AC or stored from the AC into memory. Arithmetic and logical operations involve two operands, one held in the AC and the other fetched from memory. The result of the operation is left in the AC. The AC may be cleared, complemented, tested, incremented or rotated under program control. The AC also serves as an input-output register. All programmed data transfers pass through the AC.

3.3.1.1.2 Link (L): L is a flip flop that serves as a high-order extension of the AC. It is used as a carry flip flop for 2's complement arithmetic. A carry out of the ALU complements L. L can be cleared, set, complemented and tested under program control and rotated as a part of the AC.

3.3.1.1.3 MQ Register (MQ): The MQ is a 12-bit temporary register which is program accessible. The contents of AC may be transferred to the MQ for temporary storage. MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and the MQ may also be exchanged.

3.3.1.1.4 Output Latch (OL): While accessing memory or I/O, all data or addresses generated by the 6120 on the DX bus are held in the OL for the time required on the bus. This frees the 6120 internal bus for other uses during these operations. The output latch can also be read to the 6120 internal bus so that it can function as a temporary holding register for internal operations.

3.3.1.1.5 Program Counter (PC): The 12-bit PC contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the PC is transferred to OL and the PC is then incremented by 1. When there is a branch to another address in memory, the branch address is set into the PC. Branching normally takes place under program control. A skip (SKP, SMA, SZA, SNL, etc.) instruction increments the PC by 1, thus causing the next instruction to be skipped. The skip instruction may be unconditional or conditional on the state of the AC and/or LINK. During an input-output operation, a device can also cause the next instruction to be skipped.

3.3.1.1.6 Temporary Register (TEMP): The 12-bit TEMP register latches the result of an ALU operation before it is sent to the destination register to avoid race conditions. The TEMP is also used as an internal register during instruction execution.

3.3.1.1.7 Instruction Register (IR): During an instruction fetch, the 12-bit IR contains the instruction that is to be executed by the 6120.

3.3.1.1.8 Stack Pointers (SP1 and SP2): The stack pointers are two twelve-bit registers which hold the address of the next stack storage location. PPCX or PACX instructions cause post-decrement of the contents of stack pointer SPX. RTNX or POPX cause a pre-increment of the contents of the stack pointer. Stack pointers are loaded from, and read into, the AC. They may also be used as program-controlled temporary registers.

3.3.1.2 Memory Extension Control Registers:

3.3.1.2.1 Instruction Field (IF): The 3-bit Instruction Field holds the memory field from which all instructions, all indirect address pointers and all directly addressed operands are obtained. It may be read into the AC, and loaded from the IB. It is cleared by RESET.

3.3.1.2.2 Instruction Buffer (IB): The 3-bit Instruction Buffer serves as a holding register for instructions which change the IF. Instead of changing the IF directly, field bits are loaded into the IB, and transferred to the IF at the next JMP, JMS, RTN1 or RTN2. The IB may be loaded from instruction bits, from the AC or from the ISF. The IB is cleared by RESET.

3.1.2.3 Data Field (DF): The 3-bit Data Field holds the memory field from which all indirectly addressed operands are obtained. The DF may be loaded from instruction bits, from the AC or from the DSF. It may be read into the AC. It is cleared by RESET.

3.3.1.2.4 Instruction Save Field (ISF): The 3-bit ISF is loaded with the contents of the IF upon granting of an interrupt. The ISF may be read into the AC. It is cleared by RESET.

3.3.1.2.5 Data Save Field (DSF): The 3-bit DSF is loaded with the contents of the DF upon granting of an interrupt. The DSF may be read into the AC. It is cleared by RESET.

3.3.1.3 Multiplex Busses:

3.3.1.3.1 External DX Bus: The 12-bit input/output multiplexor bus handles data, address and instruction transfers between the 6120 and the main memory, panel memory, switch register and peripheral devices on a time-multiplexed basis.

3.3.1.3.2 C0 and C1 Bus: The C0 and C1 bus is a bi-directional time-multiplexed bus used to transmit the two MSB of the extended memory address (Instruction or Data Field), the status of L and GT, the status of the BTSTRP and PNLTRP, or the PWRON and INTREQ. This bus is also used to receive I/O device transfer control commands, and to receive new data for L and GT flags.

3.3.1.3.3 EMA2 Bus: EMA2 is an output bus from the 6120 used to transmit the LSB of the extended memory address, the status of the Interrupt Enable flip flop (IEFF) or the status of the HLTFLG flip flop on a time-multiplexed basis.

3.3.1.4 Major State Generator: During an instruction fetch the instruction to be executed is retained internally and then executed. During the sequencing of the instruction the external request lines are sampled by the priority network. The state of this network decides whether the machine is going to fetch the next instruction in sequence or service one of the internal or external request lines.

3.3.1.5 Timing and State Control: The number of states for each instruction is defined in section 3.3.4. The following external operations occur:

A. A 15-bit address is sent on the C0, C1, EMA2 and DX lines for memory reference instructions. The LXMAR or LXPAR signals cause an external register to store the address information if required. When executing an input-output instruction, LXDAR causes an external register to be loaded with device address and control information.

B. Memory data is read for an input transfer (READ). ACK controls the transfer duration. If ACK is low during input transfers, the 6120 waits with the READ line low. The high state of the ACK signal causes the 6120 to continue after a synchronizing time of 1/2 minor cycle maximum. There is a minimum of 1/2 minor cycle plus 100 ns from the high state of ACK until the READ line is high.

C. Output memory transfers can be made following a read operation. The address is defined as given above. ACK controls the length of time for which the WRITE signal is low, similar to the READ line control. If the memory operation being performed is "write only", (for example, the execution of a DCA or JMS instruction) then the write is not preceeded with a read at the same location. Detailed timing diagrams for memory operations are shown in figures 3,4, & 5.

3.3.2 Internal Priority Structure:

3.3.2.1 General Description: The external request lines RESET, DMAREQ INTREQ; and the internal request flags HLTFLG, Bootstrap, Panel Trap and RUN/HLT flip flop are sampled in an internal priority network. The internal priority is RESET, DMAREQ, RUN/HLT, CPREQ, INTREQ, and IFETCH. The state of the priority network determines the next operation.

3.3.2.2 IFETCH: If no external or internal requests are pending, the 6120 fetches the next instruction pointed to by the contents of the PC. The IFETCH line is low during the cycle in which the instruction is fetched. External devices can monitor DX0-2 during IFETCH*READ to determine the functional class of the current instruction.

3.3.2.3 RESET: RESET initializes all internal flags and clears the AC, LINK and MQ. All memory extension bits (IF, IB, DF, ISF and DSF) are cleared. IEFF and IIFF are cleared. RUNHLT is set to the run state. The RUN line is held high by RESET.
The states of SP1 and SP2 are undefined at power up, and are unaffected by RESET.

Upon application of power, the internal timing generator is completely initialized within 30 clock pulses after power is within limits with RESET held low and ACK held high.

The 6120 remains in the reset state as long as the RESET line is low. LXMAR, LXPAR, READ, WRITE, MEMSEL, INTGNT and IFETCH are held high. IOCLR is held low. After RESET is changed from low to high, IOCLR is made high. LXDAR is held low for one minor cycle after IOCLR is high. DMAGNT and OUT are low. The first LXMAR or LXPAR occurs 5-1/2 minor cycles after IOCLR goes high. The PC is set to 7777(octal) and execution commences in control panel or main memory, depending on whether the STRTUP input is low or high respectively. If execution commences in control panel memory, the FZ flag is set, the Panel Data flag is cleared, and 7777 is deposited in location 0000 of control panel memory before beginning instruction execution at location 7777. If execution commences in main memory, location 0000 of main memory is not modified. ACK can be held low during reset to freeze the 6120 at a fixed point in the reset sequence. IOCLR will go high one and one half minor cycles after RESET and ACK are simultaneously brought high.

3.3.2.4 RUN/HLT: The RUN HLT flip flop is placed in the run state by RESET.

The RUN/HLT line changes the state of the RUN HLT flip flop. Pulsing the line low causes the 6120 to alternately run and halt. This is true whether executing in main memory or control memory. The RUN/HLT line is normally high. The 6120 recognizes the positive transition of the RUN/HLT signal. The HLT instruction (7402 octal) does not cause the RUN HLT flip flop to be cleared, but causes entry into panel mode with the HLTFLG set.

3.3 Memory:

3.3.3.1 General Description: Instructions are 12-bit words stored in memory. The 6120 makes no distinction between instructions and data; it can manipulate instructions as stored variables or execute data as instructions when it is programmed to do so. There are three general classes of instructions. They are referred to as Memory Reference Instructions (MRI), OPeRate instructions (OPR) and Input/OutpuT instructions (IOT). IOT instructions are further subdivided into external I/O instructions, Internal Control Instructions (ICI) and Stack Operation Instructions (SOI).

Before proceeding further, we will discuss the memory organization with which the 6120 interfaces.

3.3.3.2 Memory Organization: The 6120 has a basic addressing capacity of 4096 12-bit words. The addressing capacity is extended by the internal extended memory control hardware. The memory system is organized in 4096 word groups, called memory fields. The first 4096 words of memory are field 0. If a full 32K block of memory is installed, the uppermost memory field will be numbered 7. Two 32K word blocks of memory may be connected to the 6120. One of these blocks is known as main memory and the other is known as panel memory. In any given memory field, every location has a unique 4 digit octal (12 bit binary) address, 0000 to 7777 (0000 to 4095 decimal). Each memory field is subdivided into 32 pages of 128 words each. Memory pages are numbered sequentially from page 00, containing octal addresses 0000-0177, to page 37 (octal), containing octal addresses 7600-7777. The most significant 5 bits of a 12-bit memory address denote the page number and the 7 low order bits specify the address of the memory location within the given page.

During an instruction fetch cycle, the 6120 fetches the instruction pointed to by the IF, PC, and address strobes LXMAR or LXPAR. The contents of the PC are transferred to the OL. The PC is incremented by 1. The PC now contains the address of the 'next' sequential instruction. The OL now contains the address of the 'current' instruction which must be fetched from memory.

Bits 0-4 of the OL identify the current page, that is, the page from which instructions are currently being fetched. Bits 5-11 of the OL identify the location within the current page. (Page zero, by definition, denotes the first 128 words of memory within a field, octal addresses 0000-0177.)

3.3.4 Instructions: In the tables below, instruction time can be calculated by multiplying the number of minor cycles by twice the clock period. For example, with an 8 MHz clock, "AND" direct takes 1.75 microseconds to fetch and execute the instruction.

3.3.4.1 Memory Reference Instructions (MRI): The memory reference instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. Bits 0-2 of a memory reference instruction specify the operation code, or opcode, and the 9 low-order bits specify the operand address. Bits 5-11, the page address, identify the location of the operand on a given page, but they do not identify the page itself. The page is specified by bit 4, called the page bit. If bit 4 is a 0, the page address is interpreted as a location on page 0. If bit 4 is a 1, the page address is interpreted to be on the current page. The entire 12-bit address, consisting of the 7 low-order bits from the instruction and either 0 or the contents of the OL in the 5 high-order bits is known as the instruction address, or IA. The IF provides the 3 high-order bits of the complete 15-bit address, IA.

Other locations are addressed by utilizing bit 3. When bit 3 is a 0, the operand is directly addressed, and IA is the location of the operand. When bit 3 is a 1, the operand is indirectly addressed, and the contents of IA specify the location of the operand. To address a location that is not on page 0 or the current page, the absolute address of the desired location is stored in one of the 256 directly-addressable locations as a pointer address. The instruction addresses the operand indirectly through this pointer. Upon execution, the MRI operates on the contents of the location identified by the address contained in the pointer location. The pointer is obtained from the current Instruction Field; the data is in the current Data Field.

It should be noted that locations 0010-0017 (octal) in page 0 of any field are autoindexed. If these locations are addressed as indirect pointers, the contents are incremented by 1 and restored before they are used as the operand address. These locations may, therefore, be used for indexing applications. During the memory write operation, the DF appears on C0, C2, and EMA2. Indirect reference to auto index registers from page 0 work as defined whether the page bit is "1" or "0".

Data is represented in two's complement integer notation. In this system of notation, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most-significant bit. In the 12-bit word used in the 6120, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The number range for this system is +3777 to -4000 octal (+2047 to -2048 decimal).

TABLE I

SUMMARY OF MEMORY REFERENCE INSTRUCTIONS (SEE NOTES)

Mne-monic	Opcode	Operation	Operand Field	Minor Cycles
D	0	Logical AND direct (I=0) Operation: (AC)<=(AC)*(IA) Contents of the EA are logically ANDed with the contents of the AC and the result is stored in the AC.	IF	7
		Logical AND indirect (I=1, IA not 0010-0017) Operation: (AC)<=(AC)*((IA))	DF	10
		Logical AND autoindex (I=1, IA=0010-0017) Operation: (IA)<=(IA)+1, then (AC)<=(AC)*((IA))	DF	12

TABLE I (CONTINUED)

SUMMARY OF MEMORY REFERENCE INSTRUCTIONS

Mnemonic	Opcode	Operation	Operand Field	Minor Cycles
TAD	1	Binary add direct (I=0) Operation: (AC)<=(AC)+(IA) Contents of the EA are added with the contents of the AC and the result is stored in the AC; carry out complements the LINK. If AC is initially cleared, this instruction acts as a load from memory.	IF	7
		Binary add indirect (I=1, IA not 0010-0017) Operation: (AC)<=(AC)+((IA))	DF	10
		Binary add autoindex (I=1, IA=0010-0017) Operation: (IA)<=(IA)+1, then (AC)<=(AC)+((IA))	DF	12
ISZ	2	Increment and skip if zero direct (I=0) Operation: (IA)<=(IA)+1, then if (IA)=0, (PC)<=(PC)+1 Contents of EA are incremented by 1 and restored. If the result is zero, the next instruction is skipped. The state of the PWRON and INTREQ flags are placed on the C0 and C1 lines at the same time that the incremented result is written. The EMA2 line is at a logic 0 when the incremented result is written.	IF	8 if no skip 10 if skip
		Increment and skip if zero indirect (I=1, IA not 0010-0017) Operation: ((IA))<=((IA))+1, then if ((IA))=0, (PC)<=(PC)+1	DF	11 if no skip 13 if skip

TABLE I (CONTINUED)

SUMMARY OF MEMORY REFERENCE INSTRUCTIONS

Mnemonic	Opcode	Operation	Operand Field	Minor Cycles
ISZ (Continued)	2	Increment and skip if zero autoindex (I=1, IA=0010-0017) Operation: (IA)<=(IA)+1, then ((IA))<=((IA))+1, then if ((IA))=0, (PC)<=(PC)+1	DF	13 if no skip 15 if skip
DCA	3	Deposit and clear accumulator direct (I=0) operation: (IA)<=(AC); (AC)<=0 The contents of the AC are stored in EA, and the AC is cleared. The state of the LINK, GT and IEFF flags are placed on C0, C1 and EMA2 lines at the same time that (AC) is put on the DX lines.	IF	6
		Deposit and clear accumulator indirect (I=1, IA not 0010-0017) Operation: ((IA))<=(AC); (AC)<=0	DF	9
		Deposit and clear accumulator autoindex (I=1, IA=0010-0017) Operation: (IA)<=(IA)+1, then ((IA))<=(AC); (AC)<=0	DF	11

TABLE I (CONTINUED)

SUMMARY OF MEMORY REFERENCE INSTRUCTIONS

Mne-monic	Opcode	Operation	Operand Field	Minor Cycles
JMS	4	Jump to subroutine direct (I=0) Operation: 1. (IF)<=(IB); (CTRLFF)<=0 if prior PEX 2. (FZ)<=0 if IIFF=1 3. (IA)<=(PC) 4. (PC)<=IA+1 5. (IIFF)<=0 6. Clear prior PEX The contents of the PC are stored in the effective address. The state of the BTSTRAP, PNLTRP and HLTFLG flip flops is placed on C0, C1 and EMA2 at the time the PC is on the DX lines. The PC is incremented during the fetch operation so the contents of the EA now points to the next sequential address following the JMS (return address). The next instruction is taken from EA+1. The IF is updated after the address calculation and before storing the PC, so that the return address is stored in the field of the subroutine.	New IF	6
		Jump to subroutine indirect (I=1, IA not 0010-0017) Operation: 1. (IF)<=(IB); (CTRLFF)<=0 if prior PEX 2. (FZ)<=0 if IIFF=1 3. ((IA))<=(PC) 4. (PC)<=(IA)+1 5. (IIFF)<=0 6.Clear prior PEX	New IF	9

TABLE I (CONTINUED)

SUMMARY OF MEMORY REFERENCE INSTRUCTIONS

Mne-monic	Opcode	Operation	Operand Field	Minor Cycles
JMS (Continued)	4	Jump to subroutine autoindex (I=1, IA=0010-0017) Operation: 1. (IA)<=(IA)+1 2. (IF)<=(IB); (CTRLFF)<=0 if prior PEX 3. (FZ)<=0 if IIFF=1 4. ((IA))<=(PC) 5. (PC)<=(IA)+1 6. (IIFF)<=0 7. Clear prior PEX	New IF	11
JMP	5	Jump direct (I=0) Operation: 1. (IF)<=(IB); (CTRLFF)<=0 if prior PEX 2. (PC)<=IA 3. (FZ)<=0 if IIFF=1 4. (IIFF)<=0 5. Clear prior PEX The next instruction is taken from EA. The IF is updated at the conclusion of the instruction before the next fetch.	--	4
		Jump indirect (I=1, IA not 0010-0017) Operation: 1. (IF)<=(IB); (CTRLFF)<=0 if prior PEX 2. (PC)<=(IA) 3. (FZ)<=0 if IIFF=1 4. (IIFF)<=0 5. Clear prior PEX	--	7

TABLE I (CONTINUED)

SUMMARY OF MEMORY REFERENCE INSTRUCTIONS

Mnemonic	Opcode	Operation	Operand Field	Minor Cycles
JMP (Continued)	5	Jump autoindex (I=1, IA=0010-0017) Operation: 1. (IA)<=(IA)+1 2. (IF)<=(IB); (CTRLFF)<=0 if prior PEX 3. (PC)<=(IA) 4. (FZ)<=0 if IIFF=1 5. (IIFF)<=0 6. Clear prior PEX	--	9

TABLE I NOTATIONS:

IA — Instruction Address -- a 12-bit address derived from the memory reference instruction word and the PC. Bits 0-4 are 0 if bit 4 of the instruction was 0. Bits 0-4 are equal to bits 0-4 of the PC when the instruction was fetched if bit 4 of the instruction was a 1. Bits 5-11 are bits 5-11 of the instruction.

(IA) — "the contents of the memory location pointed to by the instruction address"

EA — Effective Address. Equal to IA if instruction bit 3=0; equal to (IA) if instruction bit 3=1.

((IA)) — "the contents of the location pointed to by (IA)"

TABLE I NOTATIONS (Continued):

Opcode	Bits 0-2 of the instruction
<=	"is replaced by"
I	Bit 3 of the instruction
*	Denotes logical AND operation
V	Denotes logical OR operation

3.3.4.2 Operate Instructions:

3.3.4.2.1 General Information: The operate instructions, which have an opcode of 7 (111), are divided into 3 groups. Group 1 operate instructions, which are identified by the presence of a 0 in bit 3, are used to perform logical operations on the contents of the accumulator and LINK. Group 2 operate instructions, which are identified by the presence of a 1 in bit 3 and a 0 in bit 11, are used primarily to test the contents of the accumulator and then conditionally skip the next instruction. Group 3 operate instructions have a 1 in bit 3 and a 1 in bit 11 and are used to perform logical operations on the contents of AC and MQ. The basic operate instruction format is shown in figure 9.

In most cases, operate instructions from a group may be microprogrammed with other operate instructions of the same group. In these instances, the actual code for a microprogrammed combination of two or more operate instructions is the bit-wise logical OR of the octal codes for the individual operate instructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 operate instructions performed first, logical sequence number 2 operate instructions performed second, logical sequence number 3 operate instructions performed third, and so on. Two operations with the same logical sequence number within a given group of operate instructions are performed simultaneously.

?.3.4.2.2 Group 1 Operate Instructions: Figure 10 shows the instruction format of group 1 operate instructions. Any one of bits 4 - 11 may be set (loaded with a binary 1) to indicate a specific group 1 operate instruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 instructions, which will be executed according to the logical sequence shown in figure 10. Bits 8, 9 and 10 are an exception to this rule, in that these three bits specify one of eight possible types of rotate instructions.

Table II lists commonly used group 1 instructions, their assigned mnemonics, octal number, instruction format, logical sequence and the operation they perform.

TABLE II

Commonly Used Group 1 Operate Instructions

All group 1 instructions require 6 minor cycles, except those performing an RTR, RTL, or BSW instruction (8 minor cycles).

Mne-monic	Opcode	Logical Sequence	Operation
NOP	7000	1	No operation--this instruction causes a delay in program execution, without affecting the state of the 6120.
IAC	7001	3	Increment accumulator--the contents of the AC is incremented by 1. Carry out complements the LINK.
BSW	7002	4	Byte swap--AC0-5 are exchanged with AC6-11 respectively. The LINK is not changed.
RAL	7004	4	Rotate accumulator left--the contents of the AC and LINK are rotated one binary position to the left. AC0 is shifted to LINK and LINK is shifted to AC11.
RTL	7006	4	Rotate two left--equivalent to two RAL's.
RAR	7010	4	Rotate accumulator right--the contents of the AC and LINK are rotated one binary position to the right. AC11 is shifted into the LINK, and LINK is shifted to AC0.
RTR	7012	4	Rotate two right--equivalent to two RAR's
R3L	7014	4	Rotate AC (but not LINK) left 3 places. AC0 is rotated into AC9, AC1 into AC10, etc.

TABLE II (CONTINUED)

Commonly Used Group 1 Operate Instructions

All group 1 instructions require 6 minor cycles, except those performing an RTR, RTL, or BSW instruction (8 minor cycles).

Mnemonic	Opcode	Logical Sequence	Operation
---	7016	4	This "unused" operate instruction performs a BSW operation at present. Use of this instruction is not recommended, since later versions of the 6120 might change this function.
CML	7020	2	Complement LINK--the contents of the LINK is complemented.
CMA	7040	2	Complement accumulator--the contents of the AC is replaced by its 1's complement.
CIA	7041	2,3	Complement and increment accumulator--the contents of the AC is replaced by its 2's complement.
CLL	7100	1	Clear LINK--the LINK is made 0.
CLL RAL	7104	1,4	Clear LINK, rotate left
CLL RTL	7106	1,4	Clear LINK, rotate two left
CLL RAR	7110	1,4	Clear LINK, rotate right
CLL RTR	7112	1,4	Clear LINK, rotate two right
STL	7120	1,2	Set the LINK--load binary 1 into LINK
CLA	7200	1	Clear accumulator--load AC with 0000
CLA IAC	7201	1,3	Clear and increment accumulator--load AC with 0001
GLK	7204	1,4	Get LINK--place LINK in AC11; clear AC0-10 and LINK
STA	7240	1,2	Set accumulator--make AC=7777
CLA CLL	7300	1	Clear AC and LINK

3.3.4.2.3 Group 2 Operate Instructions: Figure 11 shows the instruction format of group 2 operate instructions. Bits 4 - 10 may be set to indicate a specific group 2 instruction. If more that one of bits 4 - 7, 9, or 10 is set, the instruction is a micro-programmed combination of instructions, which will be executed according to the logical sequence shown in figure 11.

Skip instructions may be microprogrammed with CLA, OSR or HLT instructions. Skip instructions which have a 0 in bit 8, however, may not be microprogrammed with skip instructions which have a 1 in bit 8. When two or more skip instructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical "OR" of the individual conditions when bit 8 is 0; or, when bit 8 is 1, the decision will be based on the logical "AND".

TABLE III

Commonly Used Group 2 Operate Instructions

All Group 2 instructions require 7 minor cycles, except OSR and LAS (8 minor cycles).

Mnemonic	Opcode	Logical Sequence	Operation
NOP	7400	1	No operation--this instruction causes a delay in program execution, without affecting the state of the 6120.
HLT	7402	3	Causes the HLTFLG to be set, which causes entry into panel mode instead of executing the next instruction provided IIFF is not set. If IIFF is set, panel mode is entered after the JMP, JMS, RTN1 or RTN2 which clears IIFF. This instruction in panel mode does not cause a re-entry into panel mode, but does set HLTFLG.
OSR	7404	3	OR with switch register--the contents of an external device are "OR"ed with the contents of the AC, and the result stored in the AC. See Figure 7 for timing. The contents of the DF are available for device selection.
SKP	7410	1	Skip--the content of the PC is incremented by 1, to skip the next instruction.
SNL	7420	1	Skip on non-zero LINK--skip if LINK one
SZL	7430	1	Skip if LINK zero
SZA	7440	1	Skip on zero accumulator--skip if AC = 0000
SNA	7450	1	Skip on non-zero accumulator
SZA SNL	7460	1	Skip if AC=0000 or if LINK=1 or both
SNA SZL	7470	1	Skip if AC not 0000 and if LINK is zero
SMA	7500	1	Skip on minus accumulator (AC0=1)
SPA	7510	1	Skip on positive accumulator (AC0=0)

TABLE III (CONTINUED)

Commonly Used Group 2 Operate Instructions

All Group 2 instructions require 7 minor cycles, except OSR and LAS (8 minor cycles).

Mnemonic	Opcode	Logical Sequence	Operation
SMA SNL	7520	1	Skip if AC is minus or if LINK is 1
SPA SZL	7530	1	Skip if AC is plus and if LINK is 0
SMA SZA	7540	1	Skip if AC is minus or zero
SPA SNA	7550	1	Skip if AC is positive and non-zero
SMA SZA SNL	7560	1	Skip if AC is minus or if AC is =0000 or if LINK is 1
SPA SNA SZL	7570	1	Skip if AC is positive and nonzero, and if LINK is also zero.
CLA	7600	2	Clear accumulator (same as for CLA in operate group 1)
LAS	7604	2,3	Load accumulator from switch register
SZA CLA	7640	1,2	Skip if AC=0000, then clear AC
SNA CLA	7650	1,2	Skip on non-zero accumulator, then clear AC
SMA CLA	7700	1,2	Skip on minus AC, then clear AC
SPA CLA	7710	1,2	Skip on positive AC, then clear AC

3.3.4.2.4 Group 3 Operate Instructions: Figure 12 shows the instruction format of group 3 operate instructions, which require bits 3 and 11 to contain a 1. Bits 4, 5 and 7 are encoded to indicate a specific group 3 instruction.

If bits 6, 8, 9 or 10 are set to a one, instruction execution is not altered but the instruction becomes uninterruptable by either panel or normal interrupts. That is, the next instruction is guaranteed to be fetched barring a reset, DMAREQ or RUN/HLT flip flop in the HLT state. This is done to allow an external device to perform special operations such as extended arithmetic functions by use of the register transfer operations. See Section 3.3.7. See Table IV for Commonly-Used Group 3 Operate Instructions.

TABLE IV

Group 3 Operate Instructions

All Group 3 Instructions Require 6 Minor Cycles

Mne-monic	Opcode	Logical Sequence	Operation
NOP	7401	3	No operation--this instruction causes a delay in program execution, without affecting the state of the 6120.
MQL	7421	2	MQ register load--the MQ is loaded with the contents of the AC and the AC is cleared. The original contents of the MQ is lost.
MQA	7501	2	MQ "OR" with accumulator--the contents of the MQ is "OR"ed with the contents of the AC, and the result left in the AC. The MQ is not modified.
SWP	7521	3	Swap contents of AC and MQ--the contents of the AC and MQ are exchanged
CLA	7601	1	Clear accumulator
CAM	7621	3	Clear AC and MQ (actually a CLA MQL)
ACL	7701	3	Load AC with contents of MQ
CLA SWP	7721	3	Clear AC, then swap--the MQ is loaded into the AC; 0000 is loaded into the MQ

3.3.4.3 Input/Output Instructions

3.3.4.3.1 General Information: Input/output transfer instructions, which have an opcode of 6, are used to initiate the operation of peripheral devices and to transfer data between peripherals and the 6120. Three types of data transfer may be used to receive or transmit information between the 6120 and one or more peripheral I/O devices. Programmed data transfer provides a straight-forward means of communicating with relatively slow I/O devices, such as teletypes, cassettes, card readers and CRT displays. Interrupt transfers use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with I/O operations. Both programmed data transfers and program interrupt transfers use the accumulator as a buffer, or storage area, for all data transfers. Since data may be transferred only between the accumulator and the peripheral, only one 12-bit word at a time may be transferred. Direct Memory Access (DMA) transfers variable-size blocks of data between high-speed peripherals and the memory with a minimum of program control required by the 6120.

The input/output transfer instruction format is shown in figure 13. Bits 0-2 are always set to 6 (110) to specify an IOT instruction. The next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended. Device selection codes 00 and 2X specify internal operations, and may not be used by external devices. Up to 55 I/O devices can be specified. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

3.3.4.3.2 External Programmed Data Transfers: Programmed data transfer begins when the 6120 fetches an instruction from the memory and recognizes that the current instruction is an external IOT. An external IOT is any IOT (bits 0-2=110) whose device code (bits 3-8) is not 00 or 2X. The 6120 sequences the IOT instruction through an execute phase. Bits 0-11 of the IOT instruction are placed on DX 0-11; the data field is placed on C0, C1 and EMA2; and DATAF is asserted. LXDAR then falls, signalling the beginning of the IOT execute phase. These bits must be latched in an external register, since they are then removed to free the DX bus for I/O data exchanges. Following the fall of LXDAR, the 6120 generates a write signal. During the WRITE, the 6120 reads the SKIP, C0 and C1 lines. SKIP, C0, and C1 define the type of I/O operation. If C1 is low, the WRITE is followed by a READ and then LXDAR is made false. See Figure 6 for timing and Table V for the coding of the C0 and C1 lines during WRITE.

The control line SKIP, when low during the write portion of an IOT, causes the 6120 to skip the next instruction. This feature is used to sense the status of various signals in the device interface. The C0 and C1 lines are treated independently of the SKIP line.

TABLE V

PROGRAMMED I/O CONTROL LINES

External Programmed Data Transfers Require 9 Minor Cycles
If there is a read, 8 if not

Control lines		Operation	Description
C0	C1		
High	High	(Device)<=(AC)	The contents of the AC is sent to the device.
Low	High	(Device)<=(AC), CLA	The contents of the AC is sent to the device; then the AC is cleared.
High	Low	(AC)<=(AC)V(Device)	Data is received from a device, "OR"ed with the data in the AC, and the result stored in the AC.
Low	Low	(AC)<=(Device)	Data is received from a device and loaded into the AC.

3.3.4.3.3 Stack Operation Instructions: Certain IOT instructions are internally decoded to perform stack operations using internal stack pointers SP1 and SP2. These are internal IOT instructions; the LXDAR signal is not generated. If instructions are being fetched from main memory, the stacks are located in field 0 of main memory. If instructions are being fetched from panel memory, the stacks are located in field 0 of panel memory, except for the case of a ReTurN from control panel memory via a RTN1 or RTN2 instruction. In this case, the main memory stack is accessed by the instruction fetched from panel memory. Two separate stacks may be maintained--one for the PC, the second for the AC. An increment of the stack pointer is defined as a pop off the stack. The stack operations defined are Push PC+1 (PPC1 or PPC2), Push AC (PAC1 or PAC2), Pop to PC (RTN1 or RTN2), Pop to AC (Pop 1 or Pop 2), Read Stack Pointer (RSP1 or RSP2) and Load Stack Pointer (LSP1 or LSP2). These instructions are detailed below. "(SP)" is the contents of SP1 for PPC1, PAC1, RTN1, RSP1, or LSP1; otherwise, it is the contents of SP2. During all writes to memory, 0 appears on C0, C1 and EMA2.

Push PC on stack (PPC1=6205; PPC2=6245)--9 minor cycles

Step	Operation
1.	((SP))<=(PC)+1
2.	(SP)<=(SP)-1

Push AC on stack (PAC1=6215; PAC2=6255)--9 minor cycles

Step	Operation
1.	((SP))<=(AC)
2.	(SP)<=(SP)-1

Return (RTN1=6225; RTN2=6265)--9 minor cycles

Step	Operation
1.	(SP)<=(SP)+1
2.	(IF)<=(IB); (CTRLFF)<=0 if prior PEX
3.	(FZ)<=0 if IIFF=1
4.	(IIFF)<=0
5.	(PC)<=((SP))
6.	Clear prior PEX

Pop to AC (POP1=6235; POP2=6275)--9 minor cycles

Step	Operation
1.	(SP)<=(SP)+1
2.	(AC)<=((SP))

Read SP to AC (RSP1=6207; RSP2=6227)--5 minor cycles

Step	Operation
1.	(AC)<=(SP)

Load SP from AC (LSP1=6217; LSP2=6237)--5 minor cycles

Step	Operation
1.	(SP)<=(AC)
2.	(AC)<=0000

Caution: When switching between main and control panel memory, the stack pointers must be saved and restored.

3.3.4.3.4 Internal Control Instructions: The 600X and 62XX instructions provide for 6120 internal control operations. Table VI lists main memory control instructions. Table VII lists extended memory control instructions. Table VIII lists panel memory control instructions.

3.3.4.3.4.1 Main Memory Control Instructions

TABLE VI

MAIN MEMORY CONTROL INSTRUCTIONS

Note that these instructions apply only if the 6120 is executing instructions from main memory. (See Table VIII for similar instructions in panel mode.) Main memory control instructions require differing numbers of minor cycles. See the individual instruction.

Mnemonic	Opcode	Operation
SKON	6000	Skip if interrupt on, and turn off interrupt system. (7 minor cycles).
ION	6001	Turn on interrupt system. Neither INTREQ or any control panel request will be granted until after execution of the next instruction. (6 minor cycles).
IOF	6002	Turn off interrupt. The interrupt enable flip flop is cleared immediately. If INTREQ is low while this instruction is being processed, the interrupt will not be recognized. (6 minor cycles).

TABLE VI (CONTINUED)

MAIN MEMORY CONTROL INSTRUCTIONS

Mne-monic	Opcode	Operation
SRQ	6003	Skip if the device interrupt line is low. Note that this skip does not depend on the state of the memory extension control's interrupt inhibit flip flop. The SRQ merely tests the state of the INTREQ pin. (7 minor cycles).
GTF	6004	Get flags. The following bits are loaded into the AC:

AC Bit	Function
0	LINK
1	GT flag
2	1 if INTREQ is low; 0 if INTREQ is high
3	Power On flag (see 3.3.4.3.6)
4	1
5	0
6-8	ISF 0-2
9-11	DSF 0-2

(9 minor cycles).

Mne-monic	Opcode	Operation
RTF	6005	Return flags. Link is loaded from AC0, GT flag is loaded from AC1, AC6-8 are loaded into IB, AC9-11 are loaded into DF, interrupt inhibit flip flop is set, and bit 4 is loaded into the interrupt enable flip flop. The AC is then cleared. (8 minor cycles).
SGT	6006	Skip if the GT flag is set. (7 minor cycles).
CAF	6007	The AC, LINK and GT flag are cleared. Interrupt enable flip flop is cleared. IOCLR is generated with LXDAR high, causing peripheral devices to clear their flags. (7 minor cycles).
PR0	6206	These four opcodes have the same effect. The PNLTRP
PR1	6216	is set, causing the 6120 to enter panel mode instead of

TABLE VI (CONTINUED)

MAIN MEMORY CONTROL INSTRUCTIONS

Mnemonic	Opcode	Operation
PR2 PR3	6226 6236	executing the next instruction, provided the interrupt inhibit flip flop is not set. If the interrupt inhibit flip flop is set, the panel mode will be entered following the JMP, JMS, RTN1 or RTN2 which clears the interrupt inhibit flip flop. These instructions are a NOP in panel mode. (6 minor cycles).
WSR	6246	Write to switch register. The contents of the accumulator are written to an external device using a special I/O transfer. The AC is then cleared. See Figure 8 for timing. The contents of DF are available for device selection. DATAF is asserted. (7 minor cycles).
GCF	6256	Get current fields. The following bits are loaded into the AC: AC bit — Function 0 — LINK 1 — GT flag 2 — 1 if INTREQ is low; 0 if INTREQ is high 3 — PWRON flag 4 — Interrupt Enable Flip FLOP (IEFF) 5 — 0 6-8 — IF 0-2 9-11 — DF 0-2 (9 MINOR CYCLES).

3.3.4.3.5 Memory Extension:

3.3.4.3.5.1 The Memory Extension Control Instructions: The internal memory extension control extends the basic 4k addressing structure of the 6120 to 32K. It does so by appending three high-order bits to the memory address. These bits, which appear on C0, C1 and EMA2 lines, apply to addresses within main memory or control panel memory. The changing of memory fields is accomplished via internal control instructions. These instructions are listed in Table VII below.

The Instruction Field (IF) serves as an extension to the PC, providing three high-order bits during instruction fetches. Note that there is no carry from the most-significant PC bit into the IF. The IF is also used for directly-addressed operands, and for indirect address pointers.

The Data Field (DF) serves to extend the address of indirectly addressed operands, external IOTs, OSR and WSR functions.

The Instruction Save Field and Data Save Field are used to retain the contents of the IF and the DF which existed prior to an interrupt.

The Interrupt Inhibit Flip Flop (IIFF) is used to prevent interrupts from occurring under certain circumstances. Its use is more fully defined in 3.3.5.2.

TABLE VII

MEMORY EXTENSION INSTRUCTIONS

Memory extension instructions require 6 minor cycles, except for RIB which requires 9 minor cycles.

Mnemonic	Opcode	Operation
CDF	62X1	Change Data Field to X. X is loaded into DF.
CIF	62X2	Change Instruction Field to X. X is loaded into IB, and the IIFF is set. (The set state of IIFF causes the priority network to ignore interrupt requests). The contents of IB are loaded into the IF at the end of the next JMP, JMS, RTN1 or RTN2 instruction. At the same time IIFF is cleared.
CDF CIF	62X3	A microprogrammed combination of CDF and CIF. Both DF and IB are set to X.
RDF	6214	Load the contents of the Data Field register into bits 6-8 of the AC. DF0-2 goes to AC6-8, AC0-5 and 9-11 are unchanged.
RIF	6224	Load the contents of the Instruction Field register into bits 6-8 of the AC. IF 0-2 goes to AC6-8, AC0-5 and 9-11 are unchanged.
RIB	6234	Load the contents of the ISF and DSF into bits 6-11 of the AC. ISF0-2 goes to AC6-8 and DSF0-2 goes to AC9-11, AC0-5 are unchanged.
RMF	6244	Load the contents of ISF into IB, DSF into DF, and set the IIFF. This instruction is used to restore the contents of the memory field registers to their values before an interrupt occurred.

3.3.4.3.6 Panel Memory Control Instructions: The 6120's control panel is implemented in software. The software implementation of the control panel need not use any part of the main memory or change the processor state. This is an important feature, since the final version of a system may not have a control panel and the system designer would like to use the entire capacity of the main memory for the specific system application.

Panel mode is entered because of the occurance of any of four events. Each event sets a status flag, as well as causing the entry into panel mode. It should be noted that more than one event might happen simultaneously.

Flag	Set by	Cleared by
PWRON	RESET low and STRTUP low	PRS and PEX
PNLTRP	PRQ (main memory)	PRS and PEX
HLTFLG	HLT instruction (or any OPR2 instruction with bit 10 a 1)	PGO
BTSTRP	High-to-low transition of CPREQ	PRS if BTSTRP was set when status read

Panel mode entry is functionally similar to the granting of an interrupt with some important differences. Entry into panel mode for any reason is inhibited by the Interrupt Inhibit Flip Flop as described in Para. 3.3.5.2. Note that this means that a PRQ or HLT instruction executed when the IIFF is set will not be recognized until after the IIFF is cleared on the next JMP, JMS, RTN1 or RTN2. Entry into panel mode is also inhibited immediately following the ION instruction but will be recognized after the instruction following the ION is executed.

When a panel request is granted, the PC is stored in location 0000 of the control panel memory and the 6120 resumes operation at location 7777 (octal) of the panel memory. During PC write, 0 appears on C0, C1 and EMA2. The states of the IB, IF, DF, ISF and DSF registers are not disturbed by entry into the control panel mode but execution is forced to commence in field zero. The panel memory would be organized with RAM in the lower pages and ROM or PROM in the higher pages of field zero. The control panel service routine would be stored in the nonvolatile ROMs, starting at 7777 (octal).

A ConTRoL panel Flip Flop, CTRLFF, which is internal to the 6120, is set when the CPREQ is granted. The CTRLFF prevents further CPREQ's from being granted, bypasses the interrupt enable system and redefines several of the internal control instructions, as given in Table VIII.

TABLE VIII

PANEL MODE CONTROL INSTRUCTIONS

The number of minor cycles required is indicated after each instruction.

Mnemonic	Opcode	Description
PRS	6000	Read panel status bits into AC0-4, 0 into remainder of AC. The bits are read as follows: AC bit — Function 0 — BTSTRP 1 — PNLTRP 2 — 1 if INTREQ is low; 0 if INTREQ is high 3 — PWRON 4 — HLTFLG 5-11 — 0 Following the reading of the flags into the AC, the flags are cleared, with the exception of HLTFLG. BTSTRP is cleared only if a 1 was read into AC0. HLTFLG is cleared by the PGO instruction. (8 minor cycles).

TABLE VIII (CONTINUED)

PANEL MODE CONTROL INSTRUCTIONS

The number of minor cycles required is indicated after each instruction.

Mne-monic	Opcode	Description
ION	6001	Turn on interrupt system. The interrupt enable flip flop is set. (6 minor cycles).
IOF	6002	Turn off interrupt system. (6 minor cycles).
PGO	6003	Reset the HLTFLG flip flop. (6 minor cycles).
PEX	6004	Exit from panel mode into main memory at the end of the next JMP, JMS, RTN1 or RTN2 insruction. Clear PWRON and PNLTRP. (6 minor cycles).
RTF	6005	Load the following from the AC: AC bit — To 0 — LINK 1 — GT 4 — IEFF 6-8 — IB 9-11 — DF and set the IIFF. The AC is cleared following the load operation. (8 minor cycles).
SGT	6006	Skip if GT=1. (7 minor cycles).
CAF	6007	Clear the AC and LINK. The IEFF is cleared Generate IOCLR with LXDAR high. (7 minor cycles).
CPD	6266	Clear Panel Data Flag (PDF). Clears the panel data flag so that indirect data operands of panel mode instructions are obtained from main memory. The panel data flag is also cleared upon entry into panel memory. (5 minor cycles).
SPD	6276	Set panel data flag. Sets the panel data flag so that indirect data operands of panel mode instructions are obtained from panel memory. (5 minor cycles).

TABLE VIII (CONTINUED)

PANEL MODE CONTROL INSTRUCTIONS

The number of minor cycles required is indicated after each instruction.

Mnemonic	Opcode	Description
WSR	6246	Write to switch register. The contents of the AC are written to an external device using a special I/O transfer. The AC is then cleared. See figure 8 for timing. The contents of the DF are available for device selection. (6 minor cycles).
GCF	6256	Get current fields. The following bits are loaded into the AC: AC bit — Function 0 — LINK 1 — GT flag 2 — 1 if INTREQ is low; 0 if INTREQ is high 3 — PWRON 4 — IEFF 5 — 0 6-8 — IF 0-2 9-11 — DF 0-2 (9 minor cycles).

3.3.4.3.6 (cont.) As long as the CTRLFF is set, LXPAR is used for all instruction, direct data and indirect pointer references. Also, while CTRLFF is set, the INTGNT line is held high but the INTerrupt GraNT flip flop is not cleared. IOT's executed while CTRLFF is set do not clear INTGNT.

Indirectly addressed data references by control panel AND, TAD, ISZ or DCA instructions reference panel memory or main memory as controlled by a Panel Data Flag (PDF) internal to the 6120. If set, this flag causes indirect references from control panel memory to be to control panel memory using LXPAR. If cleared, this flag causes indirect references from control panel memory to be to main memory using LXMAR.

The PDF is cleared unconditionally whenever the panel mode is entered for any reason. It is also cleared by an instruction called CPD (Clear Panel Data) whose opcode is 6266. The PDF is set by an instruction called SPD (Set Panel Data), whose opcode is 6276. The state of the Panel Data flag is ignored when not operating in panel mode.

Extended memory operations are implemented for panel mode instructions by a 1-bit flag in the EMA logic (the Force Zero--FZ--flag) and by properly controlling and interpreting this flag in the EMA logic. This flag is always set when panel mode is entered and before the first panel mode memory operation (the store of the PC at control panel memory location 0000). As long as the FZ flag is set, zero appears on C0, C1 and EMA2 in place of the IF except for special C0, C1, EMA2 contents defined during write intervals, which remain undisturbed by FZ being set. The IF remains unchanged, however, and may be read by the RIF instruction. The data field is unaffected by the FZ flag and functions as defined above, using the panel data flag to determine whether operands are in main or control panel memory. In particular if FZ=0:

Control panel instruction fetch is to control panel field 0.
Control panel indirect address fetch is to control panel field 0.
Control panel current page or page zero direct data operations are to control panel field 0.
Control panel indirect data operations are specified by DF.
Main or control panel memory access is specified by the panel data flag.

The FZ flag is cleared in panel mode simultaneously with the (IF)<=(IB) transfer following the first panel mode instruction which may change the IF. These instructions are CIF (62X2), CDF CIF (62X3), RTF (6005), and RMF (6244). The (IF)<=(IB) transfer (and hence the FZ clear) takes place during the first JMP, JMS, RTN1, or RTN2 following the instruction. Once the FZ flag is cleared, the EMA logic operates in control panel memory as it does in main memory with the exception that the panel data flag controls whether indirect data operations are to control panel or main memory. In particular:

Control panel instruction fetch is specified by IF.
Control panel indirect address fetch is specified by IF.
Control panel current page or page zero data operations are specified by IF.
Control panel indirect data operations are specified by DF.
Main or control panel memory access is specified by the panel data flag.

Once the FZ flag is cleared in panel mode, it is not set until panel mode is entered again. The state of the FZ flag when not in panel mode is a "don't care".
Exiting from the control panel routine is normally achieved by executing the following sequence:

```
PEX
JMP I 0000            /location 0000 in control panel memory
```

The second instruction in this sequence may be any JMP, JMS, RTN1 or RTN2 instruction. The use of JMS is not recommended, since the programmer has no means of preserving the FZ and panel data flags.

The PEX instruction will cause the next JMP, JMS, RTN1 or RTN2 instruction to reset the CTRLFF. Location 0000 in the control panel memory contains either the original return address deposited by the 6120 when the control panel routine was entered or it may be a new starting address defined by the control panel routine. The IF and DF registers may also contain their original field designations or may have been altered by the control panel routine. If an exit is made from the control panel routine with the HLTFLG set, one instruction is executed in main memory before control panel mode is re-entered due to the HLTFLG being set. Note that this allows a software controlled single step operation of programs in main memory. Caution: Single step operation will not occur for any uninterruptable instructions or any instructions which set the IIFF. See Para. 3.3.5.2. Exiting from a control panel routine can also be achieved by activating the RESET line, since reset has a high priority than control panel request. If the RUN/HLT line is pulsed while the 6120 is in the panel mode, the 6120 will halt at the completion of the current instruction.

3.3.4.3.7 Summary of Internal Control Instructions

Device Code 00

Main memory control instructions are defined in Table VI. Control panel memory control instructions are defined in Table VIII.

Opcode	Main memory	Control panel memory
6000	SKON	PRS
6001	ION	ION
6002	IOF	IOF
6003	SRQ	PGO
6004	GTF	PEX
6005	RTF	RTF
6006	SGT	SGT
6007	CAF	CAF

Device Codes 20-27

Opcode	Mnemonic	Where defined
6200	$	
6210	$	
6220	$	
6230	$	
6240	$	
6250	$	
6260	$	
6270	$	

Opcode	Mnemonic	Where defined
62X1	CDF X	Table VII
62X2	CIF X	Table VII
62X3	CDF CIF X	Table VII
6204	$	
6214	RDF	Table VII
6224	RIF	Table VII
6234	RIB	Table VII
6244	RMF	Table VII
6254	$	
6264	$	
6274	$	
6205	PPC1	Paragraph 3.3.4.3.3
6215	PAC1	Paragraph 3.3.4.3.3
6225	RTN1	Paragraph 3.3.4.3.3
6235	POP1	Paragraph 3.3.4.3.3
6245	PPC2	Paragraph 3.3.4.3.3
6255	PAC2	Paragraph 3.3.4.3.3
6265	RTN2	Paragraph 3.3.4.3.3
6275	POP2	Paragraph 3.3.4.3.3
6206	PR0	Table VI
6216	PR1	Table VI
6226	PR2	Table VI
6236	PR3	Table VI
6246	WSR	Table VI, Table VIII
6256	GCF	Table VI, Table VIII
6266	CPD	Table VIII
6276	SPD	Table VIII
6207	RSP1	3.3.4.3.3
6217	LSP1	3.3.4.3.3
6227	RSP2	3.3.4.3.3
6237	LSP2	3.3.4.3.3
6247	$	
6257	$	
6267	$	
6277	$	

$--Unassigned instructions execute as an uninterruptable NOP. That is, the next instruction is guaranteed to be fetched. (5 minor cycles)

3.3.5 Interrupt Transfer:

3.3.5.1 Program Interrupt Transfers: The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced. It also provides a means of performing programmed data transfers between the 6120 and peripheral devices while executing another program. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device is ready.

The interrupt system allows external conditions to interrupt the computer program (which must be in main memory) by driving INTREQ low. If no internal higher priority requests are outstanding and the interrupt system is enabled, the 6120 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the IEFF in the 6120 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

3.3.5.2 Interrupt Timing: The IIFF prevents interrupts (both device and control panel) from occuring when there is a possibility that the IF is not equal to the IB. More specifically, the IIFF is set whenever the IB is loaded (ie, by the instructions CIF, CDF CIF, RMF or RTF), and cleared whenever the IF is loaded from the IB (i.e., at the proper phase of JMP, JMS, RTN1 or RTN2 instructions). Device interrupts are recognized only if IEFF is set, IIFF is cleared and INTREQ is low.

Upon recognition of an interrupt, the 6120 stores the PC in location 0000 of field 0 and clears IEFF. Zero appears on C0, C1 and EMA2 when the PC is stored. At the same time, INTGNT goes low. During the interrupt grant sequence, IF is loaded into ISF and DF is loaded into DSF. IF, IB and DF are then cleared. The next instruction is fetched from location 0001 of main memory field 0. INTGNT remains low until the trailing edge of the first LXDAR generated by a main memory IOT following the recognition of the interrupt. See figure 6.

The granting of an interrupt requires 4 minor cycles. If a control panel interrupt is granted while INTGNT is low, INTGNT will be forced high as long as CTRLFF is set but will return to the low state when CTRLFF is cleared.

CAUTION: Because of a synchronizing problem, the following instructions should not be executed in main memory with the interrupt system enabled:

LSP1, LSP2, RSP1, RSP2, SPD and CPD.

3.3.6 Direct Memory Access: Direct memory access, sometimes called data break, is the preferred form of data transfer to use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The 6120 is involved only in setting up the transfer; the transfers take place with no 6120 intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The external device generates a DMA request when it is ready to transfer data. The 6120 grants the DMAREQ by pulling the DMAGNT signal high at any point in any of the instructions, or between instructions, when the 6120 is not using the DX bus in performing a bus read, write or read-modify-write operation. The 6120 suspends its internal timing when the DMAGNT line is high. The DX lines, EMA2, C0 and C1 lines are put into a high-impedance state. LXPAR, LXMAR, MEMSEL, OUT, READ and WRITE are all held high by a device on each of these lines which only has a very small pull-up drive. These lines can then be pulled down by an external device. In this way, these control lines are stable until the external device can gain control of them. IFETCH and LXDAR are both held high. RUN is held low. The states of DATAF and INTGNT are undisturbed.

The external DMA device must not drive the bus until DMAGNT is high. The DMA device must:

a. Drive all signals with three-state devices.

b. Provide all address, data, LXPAR, LXMAR, and other control signals with the proper timing.

c. Return all control lines to the high state before relinquishing the bus.

d. Leave all drivers in a high-impedance state at or before DMAREQ is pulled high by the device.

After the DMAREQ line is pulled high, the 6120 negates DMAGNT, turns on the DX drivers, waits to allow address set-up time, and then, proceeds.

3.3.7 Register Transfer Operation: The register transfer operation is intended to operate with an external device which samples instructions at instruction fetch time. Upon recognizing an appropriate instruction, the external device forces the 6120 to give up its internal register states. The external device then performs operations on this data and returns modified states to the 6120. Register transfer is initiated by pulling the SKIP line low during the next instruction fetch time.

Pulling the SKIP line low during the read time of the instruction fetch operation of any instruction causes the following operation to occur in place of the normal execute cycle of that instruction:

A. IFETCH stays low and LXPAR, LXMAR and LXDAR stay high during the entire following sequence. This condition in conjunction with READ or WRITE pulses identifies these special bus transfers. In addition, the 6120 removes pullup drive from the SKIP line.

B. Two WRITE pulses are generated by the 6120 which output the following data in a fixed order.

WRITE pulse #1: MQ contents on the DX bus, DF contents on the C0, C1 and EMA2 lines.

WRITE pulse #2: AC contents on the DX bus, the LINK contents on C0, the GT flag on C1, IEFF on EMA2.

After the second WRITE pulse the 6120 releases the bus, similar to a DMA acknowledge. C0, C1, EMA2 and DX0-11 are put into a high-impedance state. LXPAR, LXMAR, MEMSEL, DATAF, READ, OUT and WRITE are held high by a device with only a small pullup capability (<600ua). IFETCH remains low. LXDAR is held high. The 6120 remains in this state until the SKIP line is pulled high by the external device. The state of INTGNT is undisturbed by the register transfer operation.

After the SKIP line is pulled high, the 6120 reapplies the SKIP line pullup drive and issues three READ pulses to reload the contents of the internal registers in a fixed sequence. This sequence is as follows:

READ pulse #1: AC on DX bus, LINK on C0 line, GT flag on C1 line.

READ pulse #2: MQ on DX bus

READ pulse #3: PC on DX bus

Note that the external device can re-establish the PC to cause execution anywhere in the current instruction field. There is no provision for modifying the current instruction or data fields.

During this second sequence, the external request lines are sampled in the normal manner to determine if the next major sequence is IFETCH, INTGNT, etc.

Special care must be taken in the external device design to insure that conflicts do not occur on the time-multiplexed SKIP line, between register transfer and IOT skip operations. The operation (not counting the bus release time) is 12 minor cycles.

3.3.8 Definition Of 6120 Flag Bits And Miscellaneous Outputs: Table IX describes all the 6120 internal flags and the discrete control outputs which do not have their timing defined in timing diagrams.

Set conditions - conditions (if any) under which the flag is jam set as a result of some instruction or other machine conditions.

Clear conditions - conditions (if any) under which the flag is jam cleared as a result of some instruction or other machine conditions.

Load conditions - conditions (if any) under which the contents of some register bit or condition is loaded into the flag in question. The source bit is also identified for each load condition.

Definition- the general meaning of the flag and its effect on machine operations. Conditions under which the state of the flag bit is transferred to some other flag, register bit or output is also discussed.

TABLE IX

CONDITIONS AND DEFINITIONS

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
L LINK	None- the STL instruction of the group 1 operate is a micro-microprogrammed combination of CLL and CML.	1.RESET=low 2.CLL(group 1 operate class)	Group 1 operate: 1.IAC causes (L)<=not(L) if there is a carry out. 2. RAL causes (L)<=(AC0) (RTL is two RAL's.) 4.RAR causes (L)<=(AC11) (RTR is two RAR's) 5. TAD: carry causes (L)<= not (L) 6.RTF:(return flags) causes (L)<=(AC0) 7.(L)<=(C0) during first read of register transfer operation.	The LINK is the general arithmetic flag of the 6120. It is tested by the group 2 operate SNL and SZL instructions. Group 1 rotates through the LINK. The GTF and GCF instructions cause the contents of the LINK to load into AC0. During the second write of the register transfer operation: (C0) <=(L)

TABLE IX (CONTINUED)

CONDITIONS AND DEFINITIONS

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
IEFF Intr. Enable Flip Flop	1.ION: (IEFF)<=1 suppress sampling of INTREQ and panel interrupts for one instruction.	1.RESET=low 2.IOF:(IEFF)<=0 before INTREQ sampled. 3.(IEFF)<=0 during INTGNT sequence. 4.SKON: (IEFF)<=0 after IEFF is tested for SKIP.	1.RTF: (IEFF)<=(AC4)	INTREQ is only honored if IEFF is a "1." The state of IEFF is tested by the SKON instruction. GCF performs(AC4)<=(IEFF) The contents of IEFF are available on EMA2 during the second write pulse of the register transfer operation.
IIFF Intr Inhib Flip Flop	1.CIF 2.CIF CDF 3.RMF 4.RTF for all four instructions (IIFF)<=1 before INTREQ or any panel mode request is sampled during this instruction.	1.RESET=low 2.JMP,JMS, RTN1,RTN2: (IIFF)<=0 before INTREQ or any panel mode request is sampled. This must occur after the time when the decision to clear FZ is made.	None	This flag suppresses any INTREQ or any panel mode request when there is a possibility that (IB)<>(IF). This is generally the interval from the time the IB is loaded until the next JMP,JMS,RTN1 or RTN2. Any JMP,JMS RTN1, or RTN2 executed with the IIFF set will cause the FZ flag to be cleared. This can be independent of the CTRLFF since the state of the FZ flag is a don't care when not in panel memory.

TABLE IX (CONTINUED)

CONDITIONS AND DEFINITIONS

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
CTRLFF ConTRoL panel Flip Flop	1.On entry into panel mode before the store of (PC) into 0000 of panel memory.	1.RESET=low 2.Next JMP,JMS, RTN1,or RTN2 instruction after PEX instruction: (CTRLFF)<=0	None	No panel mode request or INTREQ is honored while CTRLFF=1. While CTRLFF=1 all instruction, indirect pointer or stack accesses are to panel memory. Indirect accesses while CTRLFF is set are either to control panel or main memory as specified by the panel data flag.
FZ Force Zero Flag	1.On entry into panel mode before the store of (PC) into 0000 of panel memory.	1.First panel mode JMP,JMS, RTN1,or RTN2 which is executed with the IIFF set. In the case of the JMS, FZ must be cleared prior to the store of (PC+1) into the effective address location.	None	The Force Zero flag being set causes all instruction field accesses to control panel memory by the 6120 to be forced to field zero. Indirect data accesses are not affected by the FZ flag. After FZ is cleared, EMA operations occur to control panel memory exactly as they do in main memory.

TABLE IX (CONTINUED)

CONDITIONS AND DEFINITIONS

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
PDF Panel Data Flag	1.SPD instruction	1.Panel mode entry before the first instruction fetch. 2.CPD instruction.	None	1.The Panel Data Flag affects whether indirect data operations of TAD, AND, ISZ, or DCA instructions in panel mode access control panel or main memory. If PDF is set, those accesses are to control panel memory, otherwise they are to main memory. The state of PDF is a don't care when executing in main memory.
RUN HLT RUN HaLT flip flop	1.RESET=low	None	(RUN HLT)<= not(RUN HLT) on low to high transition of the RUN/HLT input line.	When the RUN HLT is cleared, the 6120 will halt after the first instruction in which this state is detected. While in the halt state, the machine will only respond to RESET and DMAREQ. When the RUN HLT is set, the 6120 will resume instruction execution

TABLE IX (CONTINUED)

CONDITIONS AND DEFINITIONS

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
HLTFLG	1.HLT instruction(any OPR2 with bit 10=1). Setting of HLTFLG must occur before HLTFLG is sampled as a panel interrupt request.	1.RESET=low 2.PGO instruction	None	One of the four control panel interrupt request flags. Panel mode will be entered following a HLT instruction unless RESET=low or IIFF is set. If IIFF is set, then panel mode will be entered following the JMP,JMS,RTN1, or RTN2 which clears IIFF. During the PRS instruction (AC4)<=(HLTFLG) does not clear HLTFLG.
PNLTRP PaNeL TRaP flag	1.PR0,PR1,PR2, PR3 instruction (main memory only). Setting of panel trap must occur before PNLTRP is sampled as a panel interrupt request.	1.RESET=low 2.PRS instruction after (AC1)<=(PNLTRP) action. 3. PEX instruction.	None	PNLTRP is a control panel interrupt request. Entry into panel mode is as defined for HLTFLG. PRS causes a (AC1)<=(PNLTRP) transfer followed by clearing the PNLTRP.

TABLE IX (CONTINUED)

CONDITIONS AND DEFINITIONS

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
BTSTRP BooT STRaP flag	1.High to low transition of CPREQ	1.RESET=low 2.PRS instruction after (AC0)<=(BTSTRP) but only if a "1"was loaded into AC0.	None	BTSTRP is a control panel request flip flop which is set by the falling edge of CPREQ. Entry into panel mode is as defined for HLTFLG. PRS causes a (AC0)<= (BTSTRP) transfer followed by clearing BTSTRP only if AC0 is loaded with a "1".
PWRON PoWeR ON flag	1.RESET=low and STRTUP= low.	1.RESET=low and STRTUP= high. 2.PRS instruction after (AC3)<=(PWRON) action. 3.PEX instruction	None	PWRON is a control panel request caused by RESET if the STRTUP input is low. Entry is directly into panel mode from the reset state when RESET goes high. PRS causes (AC3) <=(PWRON) followed by the clearing of PWRON.

TABLE IX (CONTINUED)

CONDITIONS AND DEFINITIONS

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
GT Greater Than flag	None	1.RESET=low	1.RTF instruction: (GT)<=(AC1) 2.The first READ of the register transfer sequence performs (GT)<=(C1)	The GT flag is a general flag which has no arithmetic significance within the 6120. It can be loaded with RTF or the first read of the register transfer sequence. GTF and GCF instructions cause (AC1)<=(GT). The SGT instruction tests the state of GT for skip if GT is set. The state of the GT flag is available on C1 during the first write pulse of the register transfer operation.
RUN output	1.Before first IFETCH after leaving the halt or reset state. Leaving the halt state is initiated by the RUN HLT flip flop being set. The set state is low.	1.RESET=low 2.Entering the halt state. The halt state is entered after execution is completed on the first instruction in which a reset state of RUN HLT is sampled."Clear" state is high.	None	Run is low whenever the 6120 is not in the halt or reset state.

TABLE IX (CONTINUED)

CONDITIONS AND DEFINITIONS

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
INTGNT INTer-rupt GraNT output	1. During INTGNT sequence before fore the store of (PC) in location 0000. The "set" state is low.	1. RESET=low 2. After completion of all required DX bus operations of the first external IOT which has INTGNT=low and CTRLFF=0. Internal processor IOTs or stack operations must not clear INTGNT. The "clear" state is high. INTGNT output is high if CTRLFF=1.	None	INTGNT indicates to the I/O devices that an interrupt request has been acknowledged. Also it can be used to externally change the meaning of the first external IOT of an interrupt routine. (Interrupt vectoring is an example).
DMAGNT Direct Memory Access GraNT output	1.DMAREQ=low and the 6120 is not in the reset state and not in the register transfer sequence and is not using the DX bus itself for any kind of external transfer. The "set" state is high.	1.RESET=low 2.DMAREQ=high. The "clear" state is low.	None	DMAGNT indicates to external devices that the processor DX bus C0, C1, EMA2 are tri-stated and that min. hold up is being maintained on LXPAR, LXMAR, OUT, READ, and WRITE. When the 6120 is doing successive memory or I/O operations to different addresses (not read-modify-write), outstanding DMA requests should be honored between these operations.

TABLE IX (CONTINUED)

CONDITIONS AND DEFINITIONS

Name	Set Conditions	Clear Conditions	Load Conditions	Definition/Actions
IOCLR I/O ClearR output	None	None	1.During RESET, LXDAR is low until after IOCLR goes high. 2.CAF instruction causes IOCLR to pulse low for >200 ns. LXDAR remains high.	Cause I/O devices to reset to a known state when in the reset mode or executing a CAF instruction.

3.3.9 Definition Of Terms And Symbols

( ) - Refers to the contents of the memory location pointed to by the memory address enclosed within the parenthesis or the contents of a register designated within the parenthesis.

(( )) - Is read: "the contents of the memory location pointed to by the contents of whatever is enclosed in the parenthesis." i.e. ((IA)) is read "the contents of the memory location pointed to by the contents of the memory address pointed to by the IA."

<> - Is read "is not equal to"

* - The symbol for the logical AND operation.

+ - Symbol for addition or positive number.

- - Symbol for subtraction or negative number.

1's complement -The 1's complement of a binary number is formed by complementing (inverting) each bit of the binary number.

2's complement - The binary number formed by adding a "1" to the 1's complement of a binary number. In the 6120, the 2's complement of a binary number represents the negative of that number.

<= - Is read "is replaced by." i.e. "(AC)<=(SP1)" is read "the contents of the AC is replaced by the contents of SP1."

Auto index registers(or locations) - Locations 0010-0017 (octal) in each memory field. When these locations are used as indirect addresses, their contents are incremented by one before the indirect operation.

AC - See 3.3.1.1.1

ACK - See Fig. 1

BTSTRP- See Table IX

C - Celsius, Capacitance.

CTRLFF - See Table IX

CPREQ - See Fig. 1

C0,C1 - See Fig. 1, 3.3.1.3.2

DF - See 3.3.1.2.3

DMA - Direct Memory Access. A method in which I/O devices perform data transfers directly to or from memory without passing through 6120 internal registers.

DMAGNT - See Fig. 1, Table IX

DMAREQ - See Fig. 1

DSF - See 3.3.1.2.5

DX BUS - Bidirectional data and address bus consisting of input/output signals DX0 through DX11.

DX0 through DX11 - See Fig. 1, 3.3.1.3.1

EA - Effective address:
= IA if bit 3 of the instruction =0
= (IA) if bit 3 of the instruction =1.

EMA - Extended Memory Addressing - refers to the use of the IF or DF contents to extend memory addressing from the basic 4096 words to 32,768 words.

EMA2 - See Fig. 1, 3.3.1.3.3

Field - A 4096 word block of memory. Within the 32,768 word memory address space of the 6120 there are eight 4096 word memory fields defined.

FZ - See Table IX

GT - See Table IX

High - The more positive of the two logic levels of the 6120 inputs or outputs.

HLTFLG - See Table IX

I - Bit 3 of a memory reference instruction. I=0 specifies direct page 0 or current page addressing; I=1; specifies indirect addressing.

I/O - Input/output transfers or peripheral devices.

IA - Instruction Address - a 12 bit memory address derived from the instruction word and the PC. Bits 0 - 4 are 0 if bit 4 of the instruction is 0. Bits 0-4 are equal to bits 0-4 of the PC contents when the instruction was fetched if bit 4 of the instruction is a 1. Bits 5-11 are bits 5-11 of the instruction.

IB - See 3.3.1.2.2

ICI - Internal Control Instructions. IOT instructions 600X, 62XX, used for internal processor control operations.

IEFF - See Table IX

IF - Instruction Field - See 3.3.1.2.1

FETCH - See Fig. 1

IIFF - See Table IX

INTGNT - See Fig. 1, Table IX

INTREQ - See Fig. 1

IOCLR - See Fig. 1, Table IX

IOT - Input/Output Transfer instruction. Refers to any instruction with a 6XXX opcode of which the 600X and 62XX instructions are internal operations rather than I/O operations.

IR - See 3.3.1.1.7

ISF - See 3.3.1.2.4

LINK (L) - See 3.3.1.1.2, Table IX

Low - The more negative of the two logic levels of the 6120 inputs or outputs

LXMAR - See Fig. 1

LXPAR - See Fig. 1

MRI - Memory Reference Instruction - AND, TAD, ISZ, DCA, JMP, OR JMS.

MQ - See 3.3.1.1.3

MEMSEL - See Fig. 1

MINOR CYCLE - Two complete cycles of OSCIN (250ns @ 8 MHz)

OL - See 3.3.1.1.4

Opcode - That part of the instruction contents which specifies the operation to be performed.

OUT - See Fig. 1

OSC IN - See Fig. 1

OSC OUT - See Fig. 1

Page - A 128 word block of memory within a 4096 word memory field. The page number is specified by the most significant 5 bits of the memory address

PC - See 3.3.1.1.5

PDF - See Table IX

PNLTRP- See Table IX

PWRON - See Table IX

RUN HLT flip flop - See Table IX

RUN - See Fig. 1, Table IX

RUN/HLT input - See Fig. 1

RESET - See Fig. 1

READ - See Fig. 1

SP1 - See 3.3.1.1.8

SP2 - See 3.3.1.1.8

SKIP - See Fig. 1

TEMP - - See 3.3.1.1.6

VSS - The most negative power supply voltage.

VCC - The most positive power supply voltage.

WRITE - See Fig. 1

Z - Symbol for impedance.

3.4 Environmental: Per A-PS-2100001-GS.

3.5 Process Compatibility Test Methods: Per A-PS-2100002-GS.

3.6 Laboratory Approvals/Flammability:

3.6.1 Laboratory Approvals: Not Applicable

3.6.2 Flammability: Not Applicable

3.7 Marking: Per A-PS-2100002-GS.

3.8 Workmanship: Per A-PS-2100002-GS.

3.9 Packaging and Shipping: Per A-PS-2100002-GS.

4. QUALITY ASSURANCE PROVISIONS: Per A-PS-2100002-GS.

5. REFERENCE: Not Applicable

TABLE X

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
DESCRIPTION	SYMBOL		
Operating Supply Voltage	V_{CC}	+4 to +7	Vdc
Input or Output Voltage Applied	V_O	V_{SS}-0.3, V_{CC}+0.3	Vdc
Storage Temperature Range	T_{STG}	-65 to + 150	^oC
Operating Temperature Range	T_A	-55 to + 125	^oC

TABLE XI

ELECTRICAL CHARACTERISTICS

PARAMETER NAME	PARAMETER SYMBOL	TEST CONDITION (1)	REQUIREMENTS MIN	REQUIREMENTS MAX	UNIT
High-Level Input Voltage	V_{IH}		$70\%V_{CC}$		V
Low-Level Input Voltage	V_{IL}			$30\%V_{CC}$	V
Input Leakage Current	I_{IL}	$0V<=V_{IN}<=V_{CC}$	–10	10	µA
Schmitt Trigger Upper Threshold	–		$60\%V_{CC}$		V
Schmitt Trigger Lower Threshold	–			$40\% V_{CC}$	V
High-Level Output Voltage	V_{OH}	$I_{OUT}=-1.6$ mA	$V_{CC}-0.4$		V
High-Level Output Current (Control Signal Holdup During DMAGNT— See 3.3.6) (LXMAR, LXPAR, READ, WRITE, OUT, MEMSEL)	I_{OS}	$V_{OUT}=V_{CC}-1.0V$	-0.2	-0.6	mA
		$V_{OUT}=0V$		–10	µA
High-Level Source Current For C0, C1, SKIP and INTREQ During Periods When the 6120 Samples These Signals	I_{OS}	$V_{OUT}=0V$	–1.6	–4.8	mA
Low-Level Output Voltage	V_{OL}	$I_{OL}=1.6$ mA		0.4	V
Output Leakage	I_{OL}	$0V<=V_{OUT}<=V_{CC}$ (2)	–10	10	µA
Supply Current	I_{CC}	$V_{CC}=5V$ (3)		400	µA

NOTES:

(1) $T_A=0^oC$ to $+70^oC$; $V_{CC}=4.75V$ to $5.25V$; $V_{SS}=0V$.

(2) Measured in High Z State.

(3) Specified at DC, SKIP and INTREQ Open-Circuited. All other inputs tied to V_{CC} or V_{SS}, all outputs open-circuited. Chip is in Reset State.

TABLE XII

CAPACITANCE DATA (TYPICAL)

Measured At (T_A=0°C to +70°C; V_{CC}=4.75V to 5.25V; V_{SS}=0V).

PARAMETER		REQUIREMENTS			UNIT
NAME	SYMBOL	MIN	TYPICAL	MAX	
Input Capacitance	C_{IN}		5		pF
Output Capacitance	C_O		8		pF
Input/Output Capacitance	$C_{I/O}$		12		pF

TABLE XIII

SWITCHING CHARACTERISTICS (1), (2), (3)

PARAMETER NAME	SYMBOL	MINOR CYCLES	TIMING AT 8 MHz MIN.	TYP.	MAX.
LXMAR, LXPAR, LXDAR pulse width	TL	1/2	65	---	---
LXMAR, LXPAR Low (Read)	TLLR	2-1/2	---	625	---
LXMAR, LXPAR Low (Write) (PPC, PAC, CP Interrupt)	TLLW	1-1/2	---	375	---
(DCA, JMS, Device Interrupt)	TLLW	2-1/2	---	625	---
LXMAR, LXPAR Low (Read-Modify-Write) (ISZ and Auto Increment)	TLLRW	4-1/2	---	1125	---
LXDAR Low (IOT) (Write Only)	TLLDW	3-1/2	---	875	---
(Write-Read)	TLLDW	4-1/2	---	1125	---
Address Setup Time	TAS	1/2	75	---	---
Address Hold Time	TAH	1/2	120	---	---
Read Access Time	TREAD	2	450	---	---
Read Setup Time	TRS		---	---	50
Read Hold Time	TRH		---	---	0
Read Pulse Width	TRP	1-1/4	275	---	---
Read Pulse Delay	TRD	1/4	10	---	---
Write Setup Time (All Non IOT)	TWS	3/4	65	---	---

TABLE XIII (CONTINUED)

SWITCHING CHARACTERISTICS (1), (2), (3)

PARAMETER		MINOR CYCLES	TIMING AT 8 MHz		
NAME	SYMBOL		MIN.	TYP.	MAX.
Write Pulse Width (All Non IOT)	TWP	3/4	120	---	---
Write Pulse Width (IOT)	TWIO	1-1/2	330	---	---
Write Hold Time	TWH	1/4	120	---	---
Write Setup Time (IOT)	TWSIO	1-1/2	295	---	---
Write Hold Time (IOT)	TWHIO	1/2	95	---	---
Max. Read ACK Delay for no Wait	TDA	---	---	150	---
Max. Delay to End of Read from ACK	TDR	---	---	290	---
Max. Write to ACK Delay for no Wait	TXA	---	---	-15	---
Max. Delay to end of WRITE from ACK	TXR	---	---	290	---

TABLE XIII (CONTINUED)

SWITCHING CHARACTERISTICS (1), (2), (3)

PARAMETER NAME	SYMBOL	MINOR CYCLES	TIMING AT 8 MHz MIN.	TYP.	MAX.
Switch register Oper. Strobe Delay	TSW	(1 min.)	200	---	---
Operating Frequency Range (MHz)	---	---	0**	---	8
Max. Write Falling to Data Valid	TWDV	---	---	---	65
Min. Write to LX Rising	TWLX	---	110	---	---

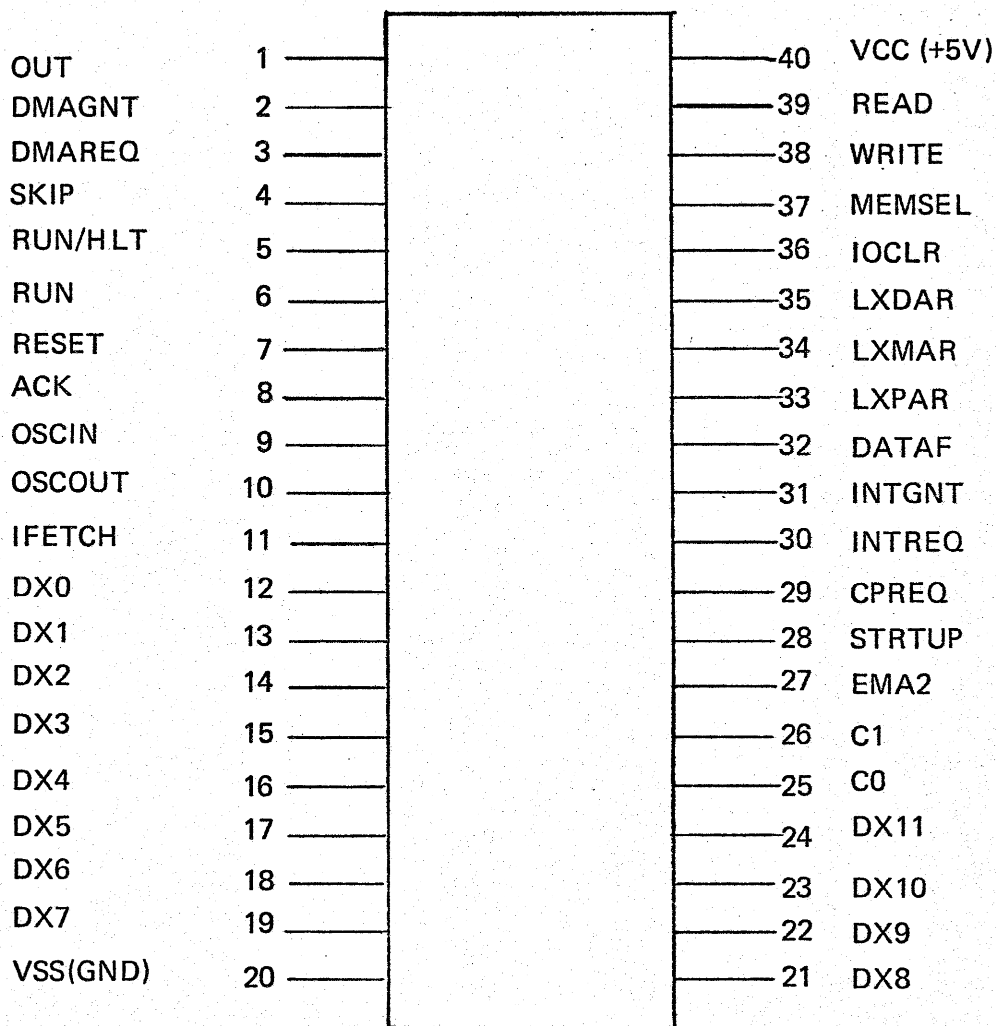
** Guaranteed but not tested

NOTES:

(1) AC Characteristics. The 6120 external timing is principally a function of clock frequency but internal delay variations cause timing variances. The basic timing in minor cycles (=2 clock periods) is given, together with expected variations and timing at an 8.0 MHz clock frequency. The timing is defined in Figures 3 through 8 VCC = +5.0 volts, TA = 0 to 70 degrees C, C_L = 50 pF. All units except minor cycles and frequency range are nanoseconds.

(2) Maximum rise and fall time on all inputs except CPREQ and RESET is 1 microsecond.

(3) All measurements taken with an input signal swing of 0.0 to 5.0 volts. All input rise and fall times 10-30 nanoseconds.



NOTE: Numbers Shown Denote Pin Numbers

FIGURE 1

PIN IDENTIFICATION, SYMBOL, ACTIVE LEVEL AND DESCRIPTION

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	OUT	Low	Bus timing control output which is low during all bus write or addressing operations. This signal is used to enable outbound bus drivers.
2	DMAGNT	High	Direct memory access grant output -- DX, C0, C1, and EMA2 lines are three-state.
3	DMAREQ	Low	Schmitt trigger input. Direct memeory access request -- DMA is granted at the end of the current bus operation. Upon DMA grant, the 6120 suspends program execution until the DMAREQ line is pulled high.
4	SKIP	Low	Input which causes the 6120 to skip the next instruction if low during an I/O instruction. Also used during register transfer operations (see 3.3.7).
5	RUN/HLT		Pulsing the RUN/HLT input causes the 6120 to alternately run and halt by changing the state of the internal RUNHLT flip flop on the positive transition of the RUN/HLT line.
6	RUN	Low	This output indicates the 6120 is fetching and executing instructions. It is low at all times except during the reset and halt states.

FIGURE 1 (CONTINUED)

PIN IDENTIFICATION, SYMBOL, ACTIVE LEVEL AND DESCRIPTION

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
7	RESET	Low	Schmitt trigger input. Clears the AC and the memory extension registers and loads 7777 (octal) into the PC. RUNHLT is set. The STRTUP line controls whether execution starts in control panel or main memory. RESET must be held low at least 42 clock cycles after the clock starts running in order to initialize the timing generator. LXDAR is held low while RESET is low, and remains low until after the positive transition of RESET.
8	ACK	High	This input indicates that peripheral or external memory is ready to transfer data. The 6120 read or write state gets extended as long as ACK is low. During this time the 6120 is in the lowest power state with clocks running.
9	OSCIN		Input to crystal oscillator amplifier. (Also external clock input).
10	OSCOUT		Output of crystal oscillator amplifier.
11	IFETCH	Low	Instruction fetch cycle output.
12	DX0	High	Multiplexed bidirectional data in, data out and address lines. (DX0=MSB,DX11=LSB).
13	DX1	High	See DX0

FIGURE 1 (CONTINUED)

PIN IDENTIFICATION, SYMBOL, ACTIVE LEVEL AND DESCRIPTION

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
14	DX2	High	See DX0
15	DX3	High	See DX0
16	DX4	High	See DX0
17	DX5	High	See DX0
18	DX6	High	See DX0
19	DX7	High	See DX0
20	VSS		Most negative supply voltage
21	DX8	High	See DX0
22	DX9	High	See DX0
23	DX10	High	See DX0
24	DX11	High	See DX0
25	CO		Multiplexed extended memory address (EMA) output MSB and peripheral device control line input from the peripheral device during and I/O transfer (Table V). LINK, PWRON and BTSTRP are brought to C0 during certain memory writes to facilitate testing (see ISZ, DCA and JMS). Also used during register transfer operations (see 3.9) and switch register operations.

FIGURE 1 (CONTINUED)

PIN IDENTIFICATION, SYMBOL, ACTIVE LEVEL AND DESCRIPTION

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
26	C1		Multiplexed EMA Bit 1 and peripheral control line. See C0. GT, INTREQ and PNLTRP flags appear on C1 during certain memory write and register transfer operations. See ISZ, DCA and JMS.
27	EMA		Low order extended memory address output. See C0. This signal is never used as input. IEFF and HLTFLG appear on EMA2 during certain memory writes. See DCA and JMS.
28	STRTUP		This input is tied to either VCC or VSS. If tied to VSS, the 6120 makes a panel request (caused by the PWRON flag) as soon as RESET goes to VCC. 7777 is stored in location 0000 of field 0 of panel memory. If STRTUP is tied to VCC, PWRON does not cause a panel request. Instead, the CPU starts running in location 7777 of field 0 of main memory. Location 0000 of main memory is not altered.
29	CPREQ	Low	Schmitt trigger input. External control panel request -- a dedicated interrupt which bypasses the normal device interrupt request structure. CPREQ causes a control panel interrupt request by setting the bootstrap flag with the negative going transition of CPREQ. Therefore, this input is transition rather than level sensitive. CPREQ is not an asynchronous input. To use this pin as a Control Panel Interrupt Request, synchronize CPREQ with the leading edge of IFETCH.

FIGURE 1 (CONTINUED)

PIN IDENTIFICATION, SYMBOL, ACTIVE LEVEL AND DESCRIPTION

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
30	INTREQ	Low	Peripheral device interrupt request input.
31	INTGNT	Low	Peripheral device interrupt grant output.
32	DATAF	Low	Output which is low whenever the Data Field is placed on the C0, C1 and EMA2 lines.
33	LXPAR	Low	Output which causes control panel memory address register to be loaded. Same as LXMAR, but for control panel memory operations.
34	LXMAR	Low	Output which causes main memory address register to be loaded. This signal goes to VSS during any main memory operation. Address is strobed into the main memory at the falling edge of LXMAR. This signal is quiescently in the high state. It must go high for at least TL nanoseconds between successive main memory cycles (see Timing).
35	LXDAR	Low	Output which causes device address register to be loaded. Same as LXMAR or LXPAR, except for IOT operations. Also used to distinguish between IOCLR signals. See IOCLR below.
36	IOCLR	Low	Output which is low when RESET is low, or when CAF instruction is given. Used to clear I/O flags. If caused by RESET, LXDAR is low during and after the trailing edge of IOCLR.

FIGURE 1 (CONTINUED)

PIN IDENTIFICATION, SYMBOL, ACTIVE LEVEL AND DESCRIPTION

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
37	MEMSEL	Low	Memory Select. During memory operations, this output pulses to VSS at bus read and write times.
38	WRITE	Low	Write Pulse. This output is low during all bus data write operations; memory, I/O, write to switch register, or register transfer output operations.
39	READ	Low	Read Pulse. This output is low during all bus read operations; memory, I/O, switch register or register transfer. It also serves the function of enabling inbound bus drivers.
40	VCC		Positive supply voltage

FIGURE 1 (CONTINUED)

PIN IDENTIFICATION, SYMBOL, ACTIVE LEVEL AND DESCRIPTION

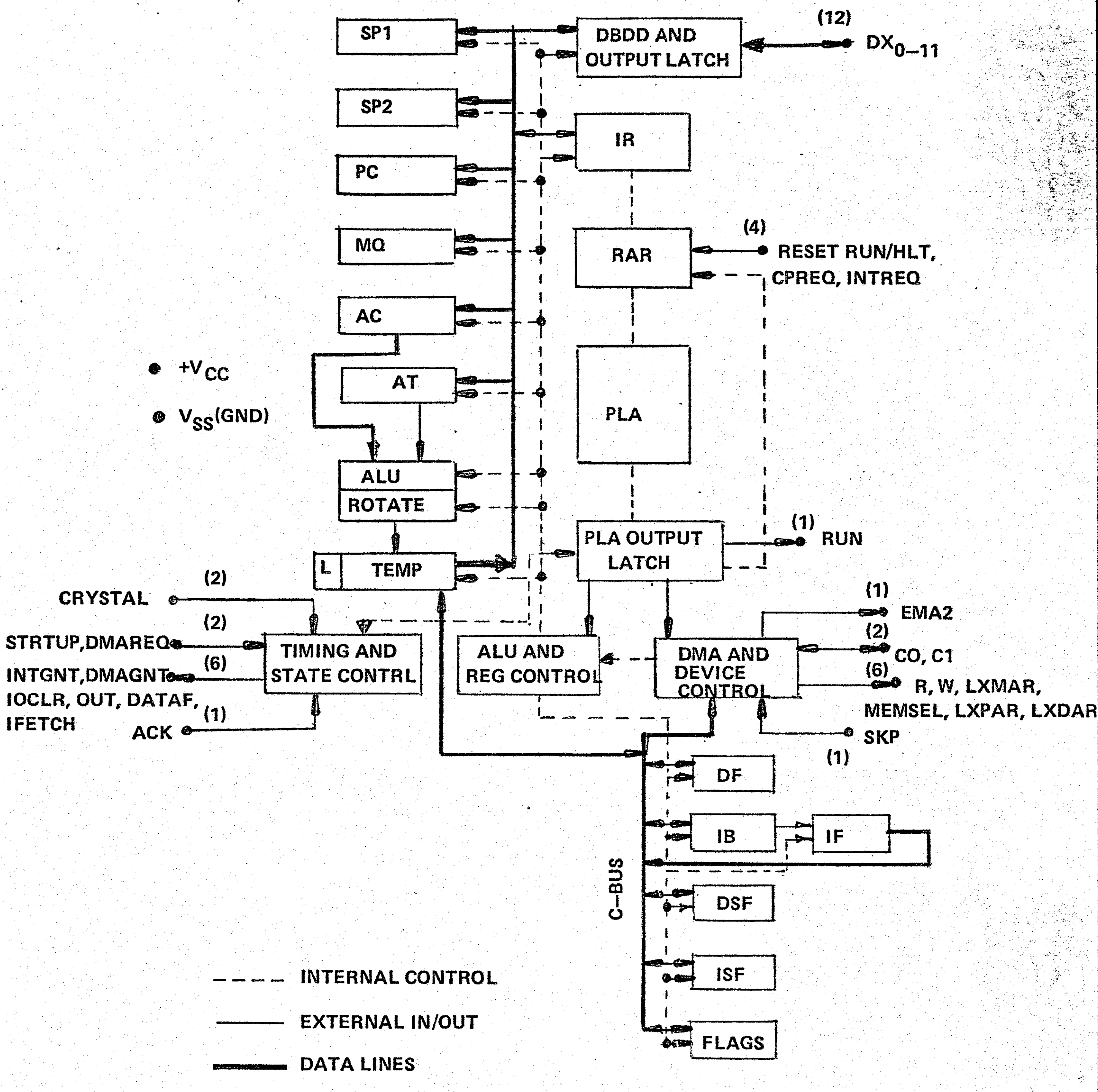


FIGURE 2

BLOCK DIAGRAM

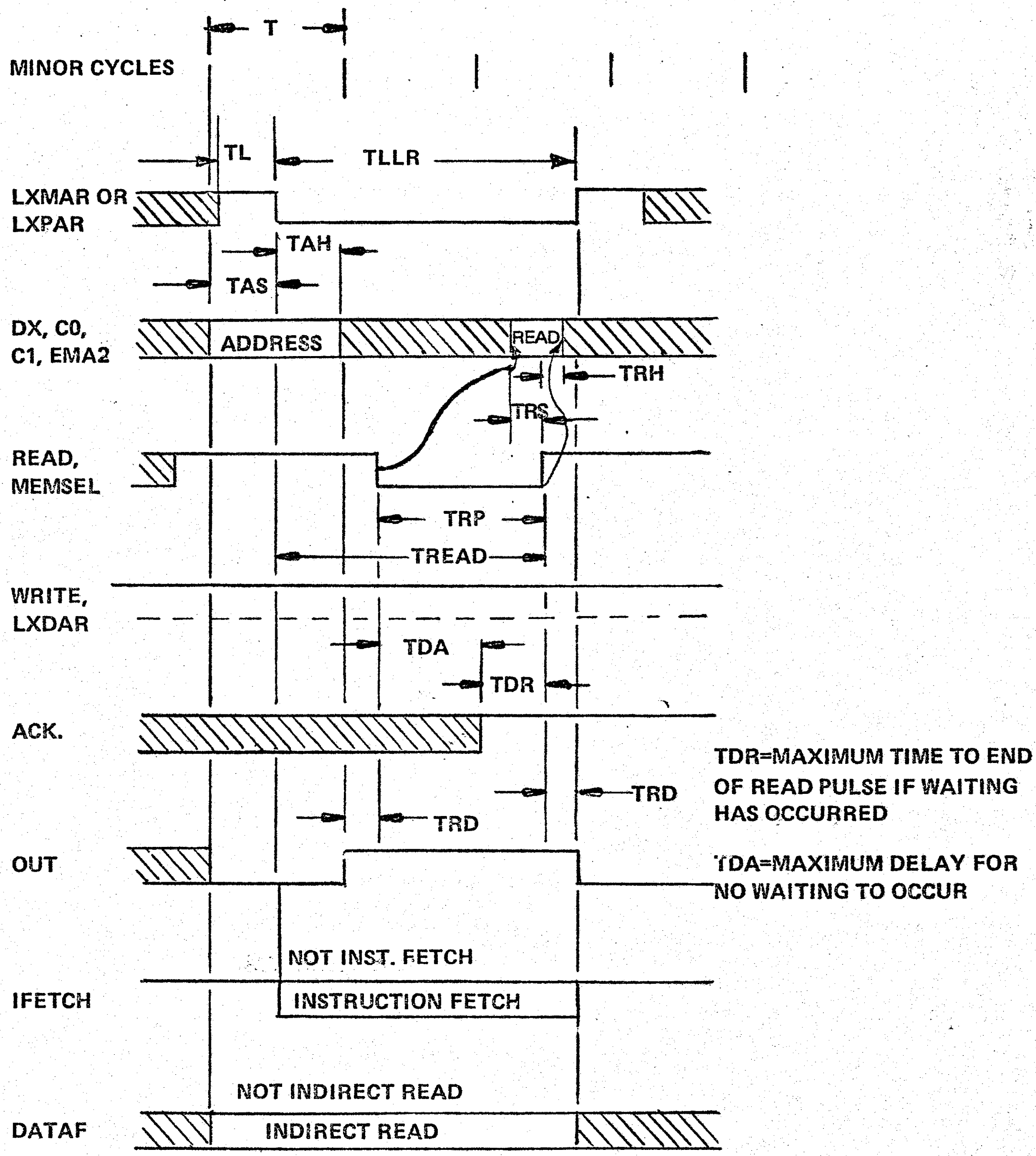
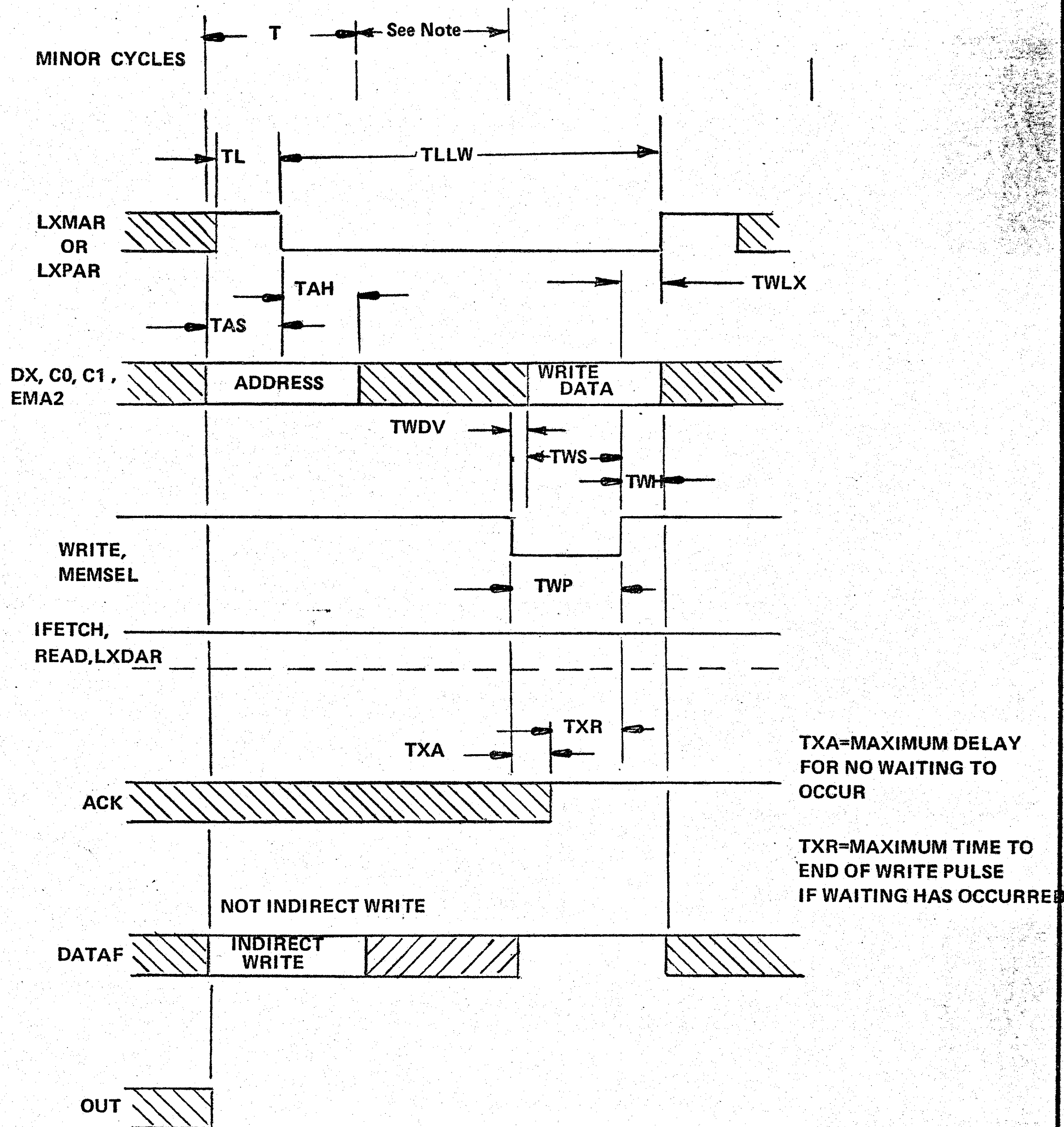


FIGURE 3
MEMORY READ OPERATION



NOTE: This cycle is deleted on PAC1, PAC2, PPC1, PPC2 and control panel interrupt write.

FIGURE 4
MEMORY WRITE OPERATION

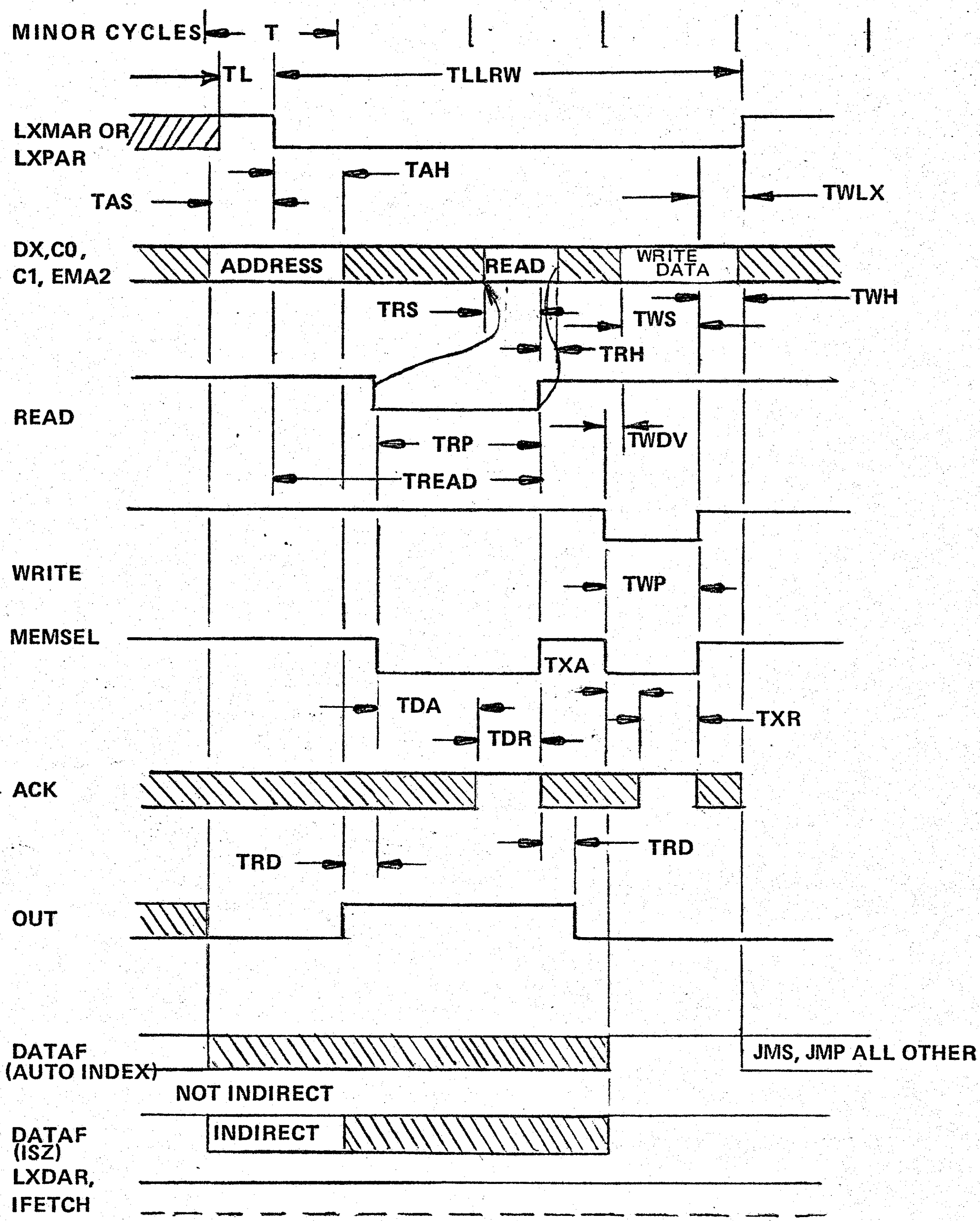


FIGURE 5

MEMORY READ, MODIFY, WRITE OPERATION

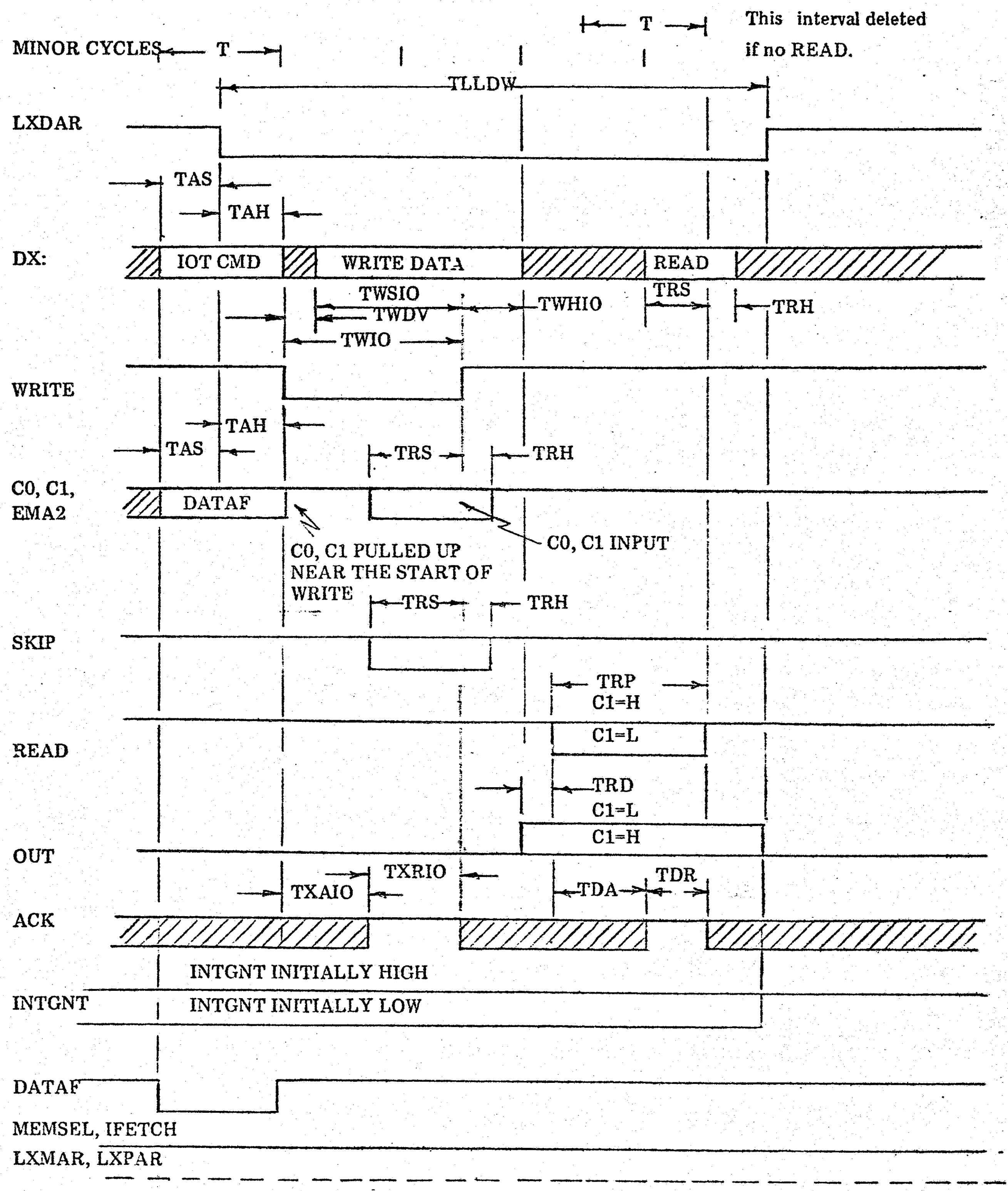


FIGURE 6
EXTERNAL IOT OPERATION
(DEVICE CODE ≠ 00 OR 2X)

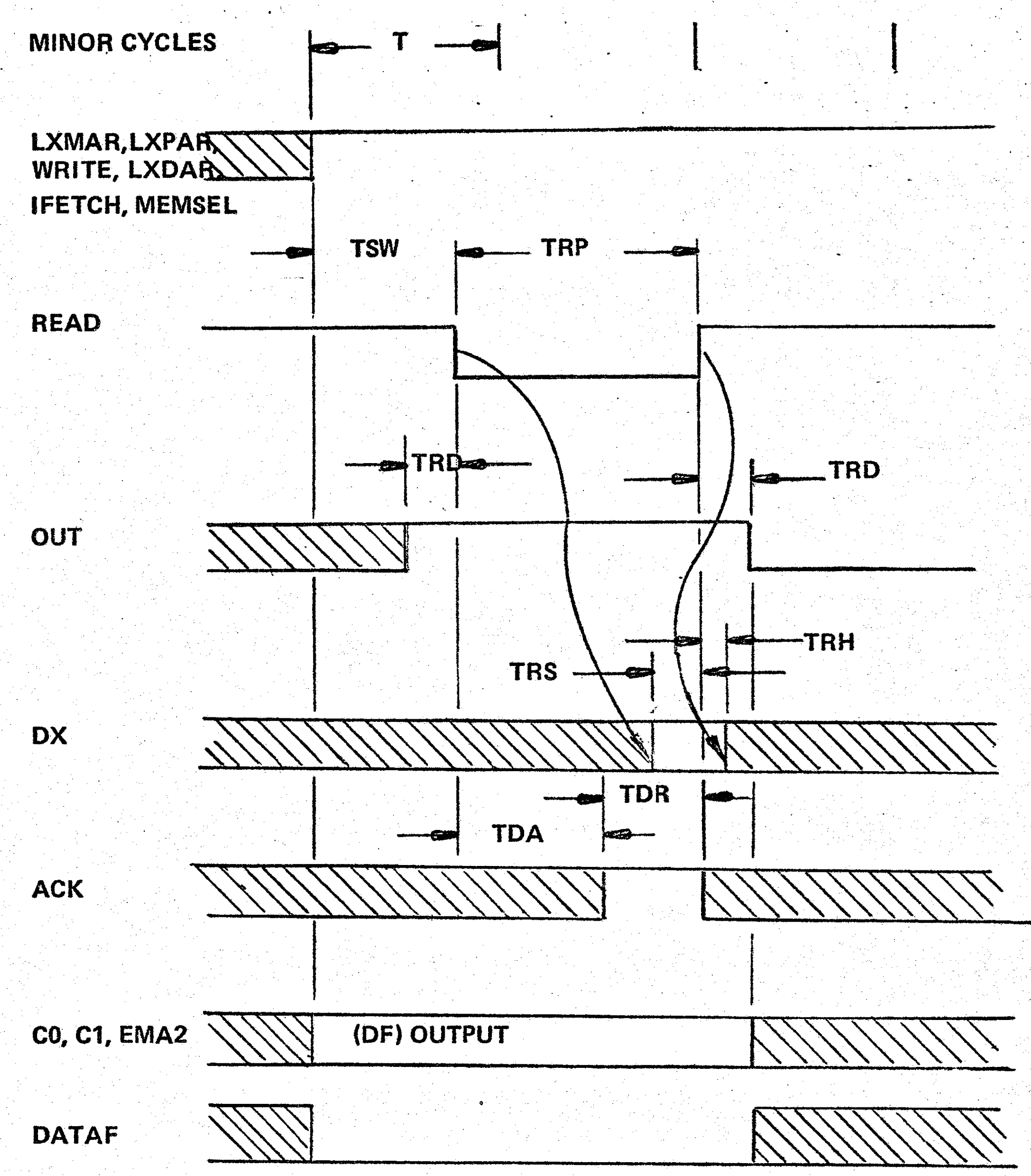


FIGURE 7

OR SWITCH REGISTER (OSR)

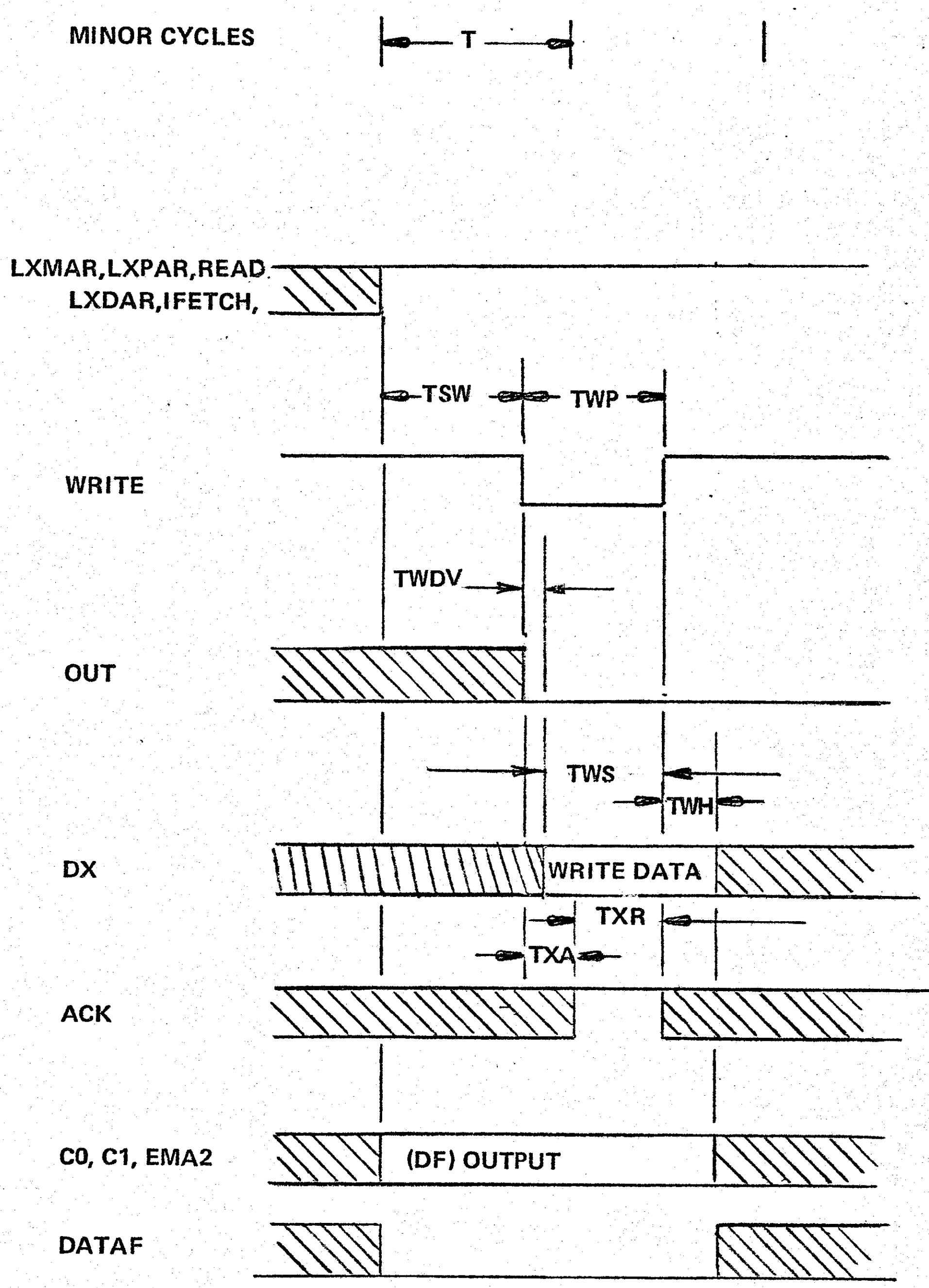


FIGURE 8

WRITE TO SWITCH REGISTER

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	A								B

MICROINSTRUCTION	A	B
GROUP 1	0	X
GROUP 2	1	0
GROUP 3	1	1

FIGURE 9

BASIC OPR INSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	CLA	CLL	CMA	CML	RAR / RTR	RAL / RTL	0 / 1	IAC

LOGICAL SEQUENCE:

1 – CLA, CLL
2 – CMA, CML
3 – IAC
4 – RAR, RAL, RTR, RTL, BSW

BIT			
8	9	10	OPERATION
0	0	0	NO SHIFT
0	0	1	BSW
0	1	0	RAL
0	1	1	RTL
1	0	0	RAR
1	0	1	RTR
1	1	0	R3L
1	1	1	DO NOT USE

FIGURE 10

GROUP 1 MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	SMA / SPA	SZA / SNA	SNL / SZL	0 / 1	OSR	HLT	0

LOGICAL SEQUENCE:

1 – (BIT 8=0) – SMA OR SZA OR SNL
(BIT 8=1) – SPA AND SNA AND SZL
2 – CLA
3 – OSR, HLT

FIGURE 11

GROUP 2 MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	MQA	*	MQL	*	*	*	1

* – CAUSES INSTRUCTION TO BE UNINTERRUPTABLE IF 1.

BIT 4	BIT 5	BIT 7	OPERATION
0	0	0	NO OPERATION
0	0	1	AC→MQ, O→AC
0	1	0	MQ V AC→AC
0	1	1	MQ→AC, AC→MQ
1	0	0	O→AC
1	0	1	O→AC, O→MQ
1	1	0	MQ→AC
1	1	1	MQ→AC, O→MQ

FIGURE 12

GROUP 3 MICROINSTRUCTION FORMAT

0	1	2	3	4	5	6	7	8	9	10	11
1	1	0									
			DEVICE SELECT CODE						OPERATION CODE		

FIGURE 13

IOT INSTRUCTION FORMAT