PDP-8/A OPERATOR'S HANDBOOK

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This document was set on DIGITAL's DECset-8000
computerized typesetting system.

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TABLES

CHAPTER 1
INTRODUCTION

There are two basic types of computers in the PDP-8/A family. The first type is the PDP-8/A, which uses semiconductor memories (MS8 and MR8). The second type is represented by a series of computers, each of which uses 8K or 16K core memory (MM8); this series consists of the 8A400, 8A420, 8A600, 8A620, 8A800, and 8A820 computers. When a reference applies to both types of computers, the designation "PDP-8/A" is used. "PDP-8/A semiconductor" refers to the semiconductor memory computer, while "8A400," for example, refers to a specific core memory machine and "8A" refers to the core memory machines in general.

The *PDP-8/A Operator's Handbook* includes instructions for packing, unpacking, and installing a PDP-8/A miniprocessor. All computers and modules are tested thoroughly at DIGITAL's manufacturing facilities before they are shipped. However, many switches and jumper wires can be arranged by the customer for specific purposes; furthermore, there is a need both to verify system interconnections and site preparations, and to detect possible hidden damage incurred during shipping. Consequently, a number of initial operating tests are also included in this handbook.

A PDP-8/A basic system can comprise a variety of components. The following three basic systems are the most common:

1. A basic PDP-8/A,* a memory, and a Limited Function Panel. (This computer does not include a KM8 Extended Memory Option module and, hence, must be a PDP-8/A semiconductor.)

2. A basic PDP-8/A, a memory, a Limited Function Panel, a KM8 Extended Memory Option module, a DKC8-AA I/O Option module, and a Programmer's Console. (Chapter 5 describes operating tests for this arrangement.)

3. A basic system as described in 2, but accompanied by a teletypewriter and diagnostic** programs. (Chapter 7 describes operating tests for this arrangement.)

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*A basic PDP-8/A is defined as a Central Processor Unit (CPU) and a chassis assembly (chassis, Omnibus, and power supply).

**Diagnostics are test programs written to find faults in the logic. The PDP-8/A programs are supplied on paper tape. Diagnostic programs are optional and may be ordered from the Software Distribution Center, 146 Main St., Maynard, MA, 01754.

CHAPTER 2
PACKING AND UNPACKING INSTRUCTIONS

2.1 UNPACKING INSTRUCTIONS
All PDP-8/A computers are packaged in two containers; the inner container holds the computer and some kind of protective material. The steps in this section are sufficiently general to apply to any PDP-8/A.

To unpack the PDP-8/A computer, proceed as follows.
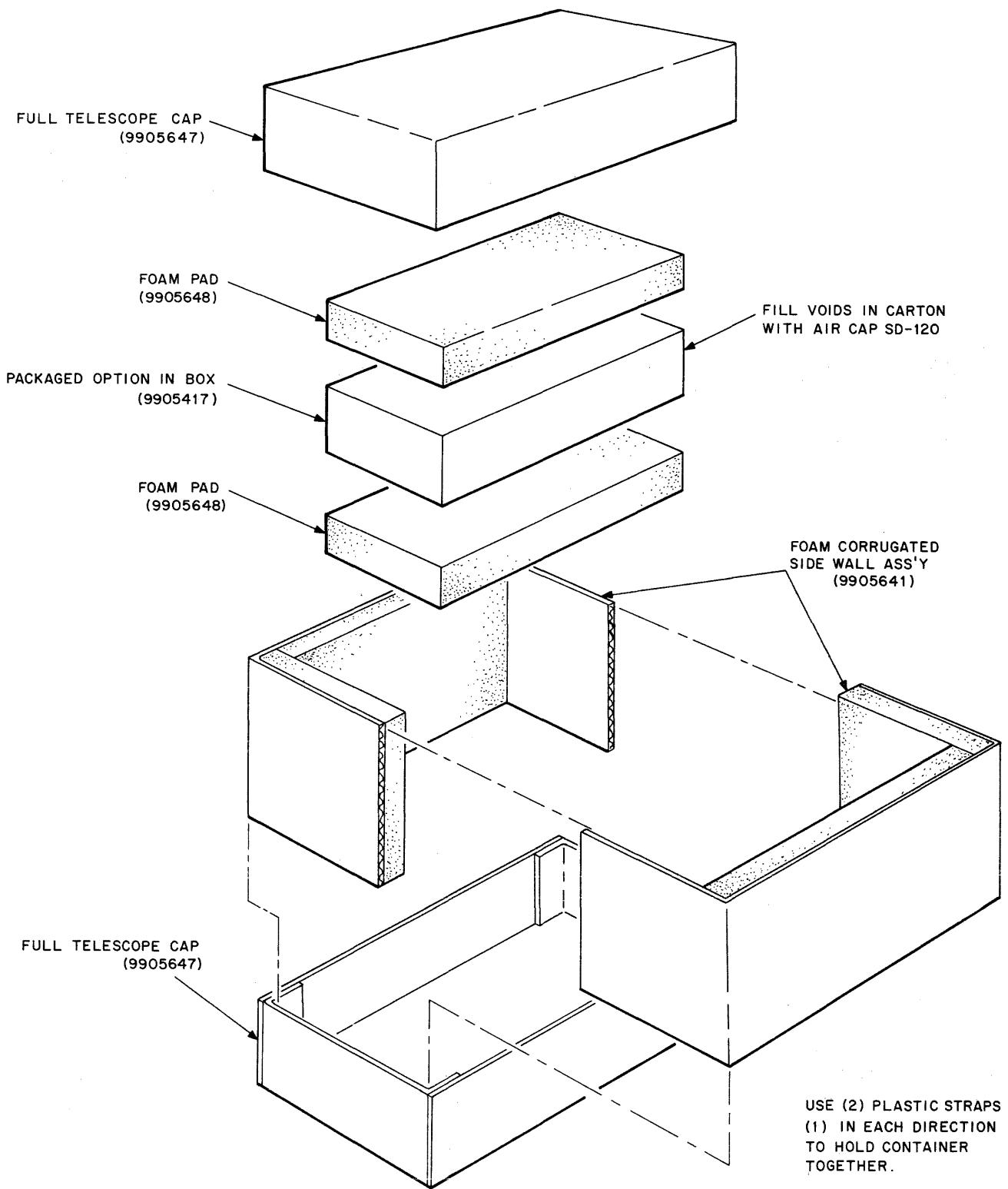
1. Open the outer carton and remove the inner carton.

2. Open the inner carton.

3. Carefully remove the cardboard from the top and sides of the computer.

4. Carefully remove the computer from the box.

5. Inspect the computer for damage. If the computer is damaged, notify the carrier immediately.

6. Unpack any other boxes included in the shipment.

7. Check that all equipment, software, manuals, etc., are present as specified on the shipping list inside the carton.

8. Save the cartons and packing material to use if the PDP-8/A is later repacked.

9. Refer to Chapter 4 for PDP-8/A installation procedures.

2.2 PACKING INSTRUCTIONS
Two types of packages are used for the PDP-8/A computers. The type used and the applicable packing instructions depend on the type of PDP-8/A chassis assembly.

2.2.1 BA8-C Chassis Assembly
The 8A420, 8A620, and 8A820 computers use a BA8-C chassis assembly (20-slot Omnibus). Figure 2-1 illustrates the packing procedure. The computer is first placed in the inner container (9905417), the empty space is filled with plastic protective material (AIR CAP, SD-120), and the container is sealed. The sealed inner container is surrounded with protective foam material which is then enclosed by the two telescope caps. Finally, the package is secured by two plastic straps.

FULL TELESCOPE CAP
(9905647)

FOAM PAD
(9905648)

FILL VOIDS IN CARTON
WITH AIR CAP SD-120

PACKAGED OPTION IN BOX
(9905417)

FOAM PAD
(9905648)

FOAM CORRUGATED
SIDE WALL ASS'Y
(9905641)

FULL TELESCOPE CAP
(9905647)

USE (2) PLASTIC STRAPS
(1) IN EACH DIRECTION
TO HOLD CONTAINER
TOGETHER.

08-1789

Figure 2-1   8A420, 8A620, 8A820 Packaging
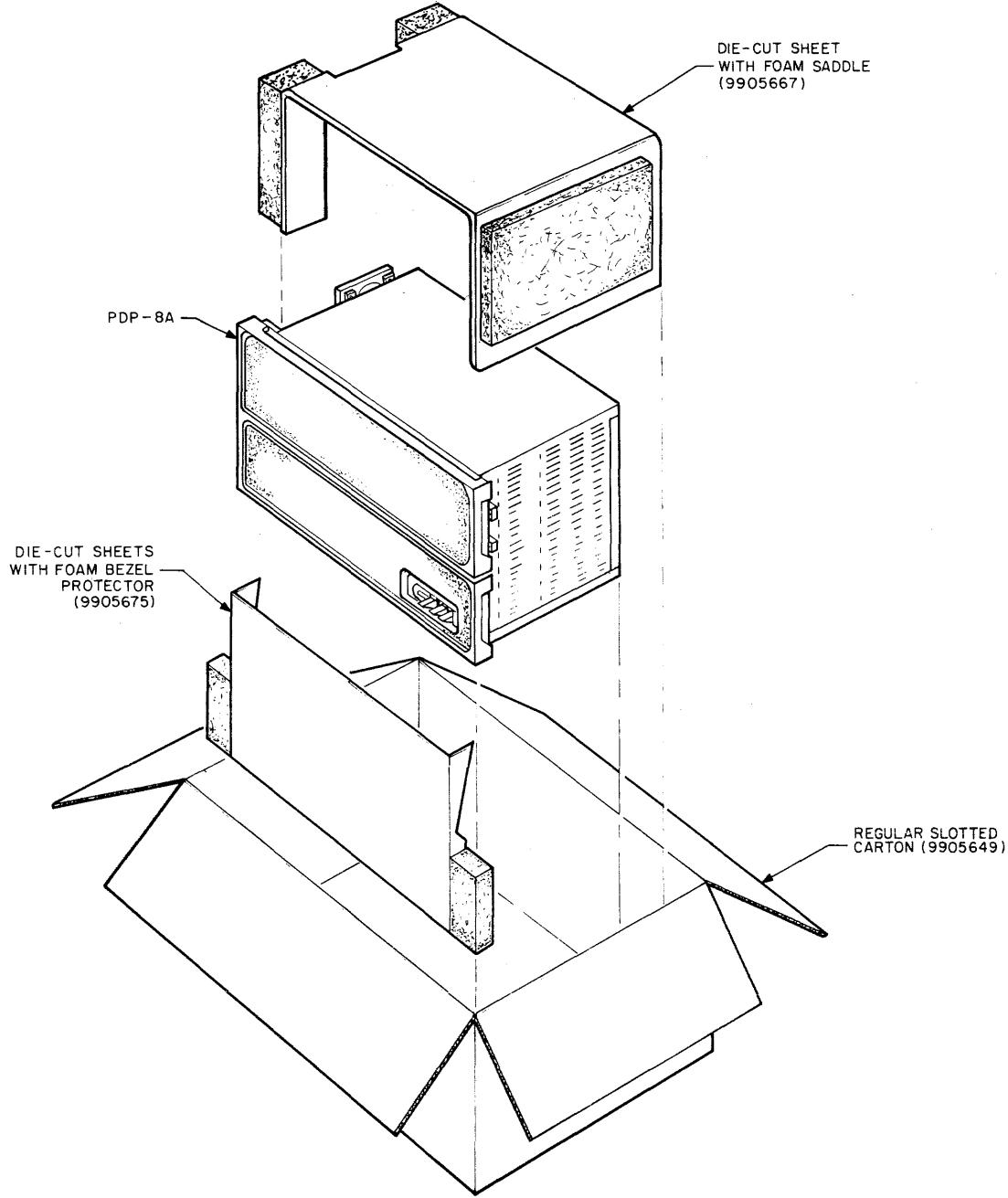
2.2.2 Other PDP-8/A Chassis Assemblies

CAUTION
The G8016 Regulator Board assembly used on PDP-8/A
semiconductor computers contains a battery. This battery,
while not of sufficient voltage to cause electrical shock,
represents a possible hazard if shorted. If repacking this
type computer, ensure that there is no loose metal, such as
solder, wire, or sheet metal parts, inside the cabinet.
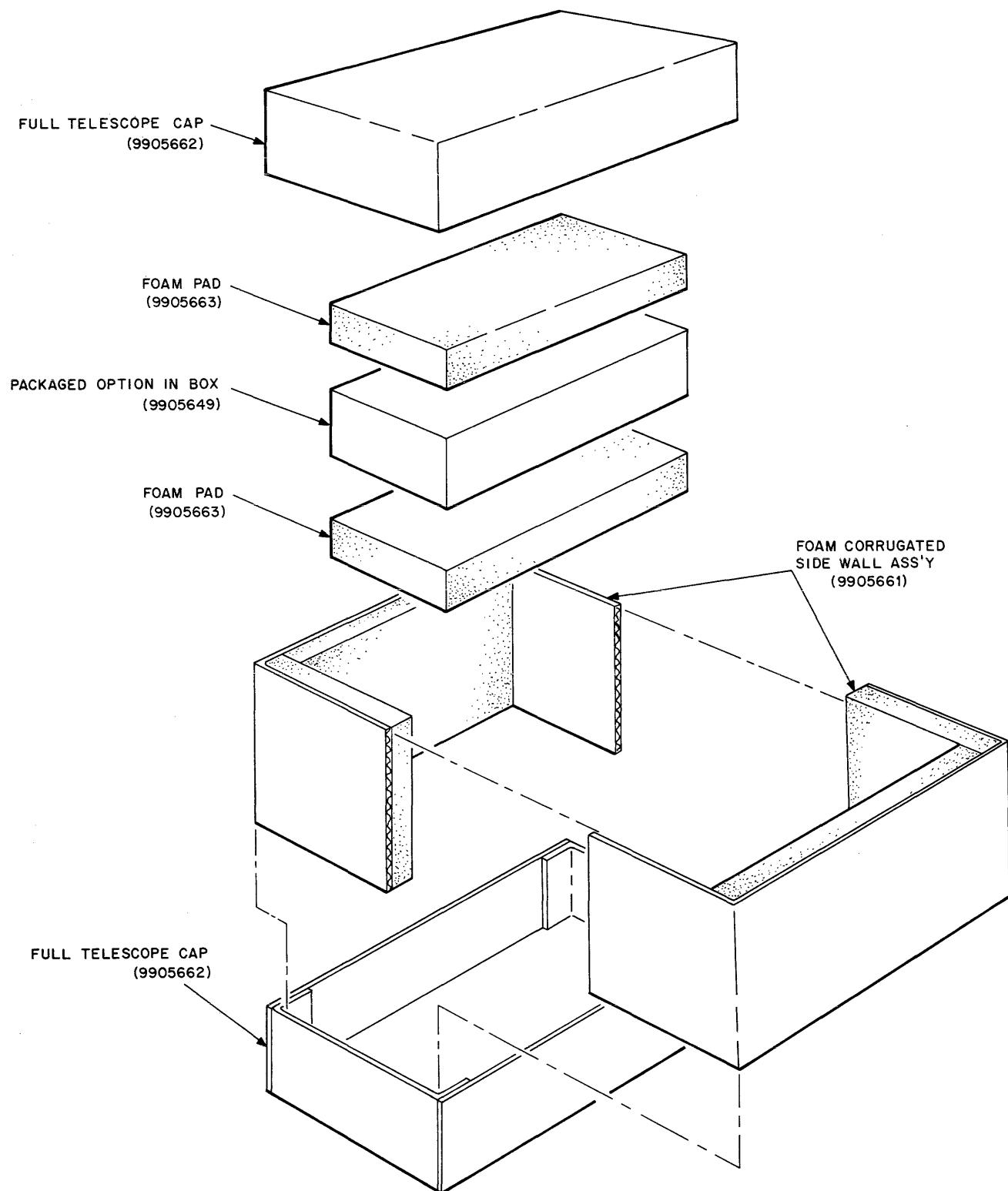
The PDP-8/A semiconductor computer and the 8A400, 8A600, and 8A800 computers use a chassis assembly that has a 10-slot or 12-slot Omnibus. To pack these computers, proceed as follows.

1. Place the computer in the smaller of the two shipping cartons with the back (side with power cord) of the computer against the side of the carton.

2. Place the beveled die-cut sheet with foam protector (part number 9905675) in front of the computer (Figure 2-2). If the Limited Function Panel and a pop panel are on the computer, the beveled edge should be down inside the carton. If the computer has a Programmer's Console, the beveled edge should be up so that the cut-out in the cardboard fits the Programmer's Console.

3. Place the die-cut sheet with foam saddle (part number 9905677) downward over the computer. The end with two pieces of foam should be fitted around the fans and the other end should be positioned so that the cardboard fits behind the cabinet mounting flange and the foam is against the side of the carton.

4. Close the flaps and seal the carton with tape.

5. Surround the sealed carton with protective foam material and enclose with telescope caps (Figure 2-3).

6. Strap in both directions using steel or plastic strapping.

DIE-CUT SHEET
WITH FOAM SADDLE
(9905667)

PDP-8A

DIE-CUT SHEETS
WITH FOAM BEZEL
PROTECTOR
(9905675)

REGULAR SLOTTED
CARTON (9905649)

08-1494

Figure 2-2   PDP-8/A Computer Packaging (Inner)

FULL TELESCOPE CAP
(9905662)

FOAM PAD
(9905663)

PACKAGED OPTION IN BOX
(9905649)

FOAM PAD
(9905663)

FOAM CORRUGATED
SIDE WALL ASS'Y
(9905661)

FULL TELESCOPE CAP
(9905662)

08-1790

Figure 2-3   PDP-8/A Computer Packaging (Outer)

3.1 GENERAL

A PDP-8/A computer is pictured in Figure 3-1, which shows both the Limited Function Panel (the panel on the bottom with three switches and three indicators) and the Programmer's Console. The Programmer's Console can be located remotely from the chassis; in such a case, or when the system does not include a console, a blank panel is attached instead. Both the panel and the console are latched to the chassis; they can be removed by pulling them off the latches. (Do not pull too vigorously; the panels are attached by cables to interior points.) When the panels are removed, the module boards are visible.

7288-5

Figure 3-1   PDP-8/A Computer

The PDP-8/A computers have three different mechanical assemblies that can be characterized by the number of available Omnibus slots; that is, the PDP-8/A semiconductor computer assembly has a 10-slot Omnibus, while the 8A computer assemblies have either a 12-slot or a 20-slot Omnibus. Table 3-1 relates the various PDP-8/A computers to some of the basic system components. Note that the 8A400 can be considered to be the basic 8A computer, having a core memory, an 8A CPU, and a 12-slot Omnibus. Thus, the 8A420 differs only in that it has a 20-slot Omnibus; the 8A600 differs in that it has a PDP-8/E CPU; the 8A620 differs in that it has a PDP-8/E CPU and a 20-slot Omnibus; the 8A800 differs in that it has an FPP-8A (not indicated in Table 3-1); and, the 8A820 differs in that it has an FPP-8A and a 20-slot Omnibus. Also, note that only the 8A computers that use a PDP-8/E CPU can be expanded.

Table 3-1
PDP-8/A Computer Assemblies

Computer	CPU	Memory*	Basic Power Assembly	Omnibus	Expandable ?
PDP-8/A	KK8-A	Semiconductor	H763	H9192 (10-slot)	No
8A400	KK8-A	Core	H9300	H9194 (12-slot)	No
8A420	KK8-A	Core	BA8-C	H9195 (20-slot)	No
8A600	KK8-E	Core	H9300	H9194 (12-slot)	Yes — as many as 20 slots can be added
8A620	KK8-E	Core	BA8-C	H9195 (20-slot)	Yes — as many as 20 slots can be added
8A800	KK8-A	Core	H9300	H9194 (12-slot)	No
8A820	KK8-A	Core	BA8-C	H9195 (20-slot)	No

*A KM8-A (or KM8-E) Extended Memory Option module must be included in all the 8A computers, since their basic memory capacity is 8K or 16K; the KM8 is optional with the PDP-8/A semiconductor computer, since the basic memory capacity can be less than, greater than, or equal to 4K.

In addition to the CPU, most DIGITAL PDP-8/E options will operate with the PDP-8/A computers. The following will not:

1. KP8-E Power Fail/Auto-Restart option
2. DK8-EA Line Frequence Real-Time Clock option
3. MM8-E 4K Core Memory
4. MM8-EJ 8K Core Memory

The KE8-E option (Extended Arithmetic Element) and the TD8-E DECtape Control will operate only with the 8A600 and 8A620 computers.

Modules can be inserted in almost any PDP-8/A Omnibus slot. There are, however, some restrictions and these are summarized in Table 3-2.

Notice that an M8320 module (Bus Loads) is inserted in slot 1 of the 8A600 and 8A620 computers. This module must be modified before it can be used in the 8A600 and 8A620 computers. If the modification has been accomplished, R55 (Figure 3-2) will have been removed; if R55 is present, carry out the procedure outlined in DEC ECO M8320-00007.
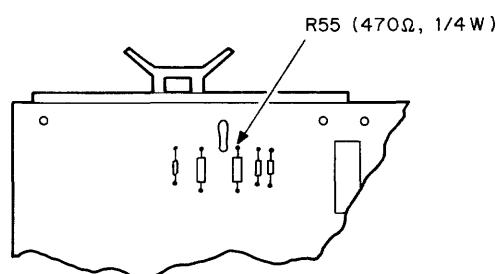
Table 3-2
PDP-8/A Computers, Dedicated Omnibus Slots

Omnibus Slot	8A600	8A600 + KE8-E	8A620	8A620 + KE8-E	PDP-8/A Semiconductor, 8A400, 8A420, 8A800, 8A820
1	M8320	M8320	M8320	M8320	M8315
2	M8316	M8316	M8316	M8316	M8316
3	M8317	M8317	M8317	M8317	M8317
4					
5					
6					
7					
8		M8300			
9		M8310			
10	M8300	M8341			
11	M8310	M8340			
12	M8330	M8330			
13					
14					
15					
16				M8300	
17				M8310	
18			M8300	M8341	
19			M8310	M8340	
20			M8330	M8330	

NOTES:

1. M8316 and M8317 are interchangeable in slots 2 and 3.

2. Module numbers are related to options as follows:

M8315	CPU (KK8-A)
M8316	I/O Option Board (DKC8-AA)
M8317	Extended Option Board (KM8-A)
M8320	Bus Loads
M8300	CPU
M8310	CPU
M8330	KK8-E Timing Generator

M8300, M8310, M8330 } KK8-E

R55 (470Ω, 1/4 W)

08-1785

Figure 3-2   Part of M8320 Module Showing R55,
Which is Removed for 8A Operation

3-3

3.2 CHASSIS DESCRIPTIONS

Three chassis types are available. The PDP-8/A semiconductor computer chassis is illustrated in Figure 3-3. (The front panels have been removed.) Modules are inserted in the Omnibus from the front of the unit. Both quad-and hex-size modules can be inserted; the fingers on connectors E and F of the hex size modules do not carry Omnibus signals. (Some hex modules do not have connectors E and F.) Figure 3-4 illustrates the dimensions of the same computer, as well as indicating the ac line and fuse locations.

G8016
REGULATOR
ASSEMBLY

POWER
CONTROL
FUSE

MASTER-SLAVE
SWITCH

CABLE TO CONNECT
LIMITED FUNCTION
PANEL

7288 4
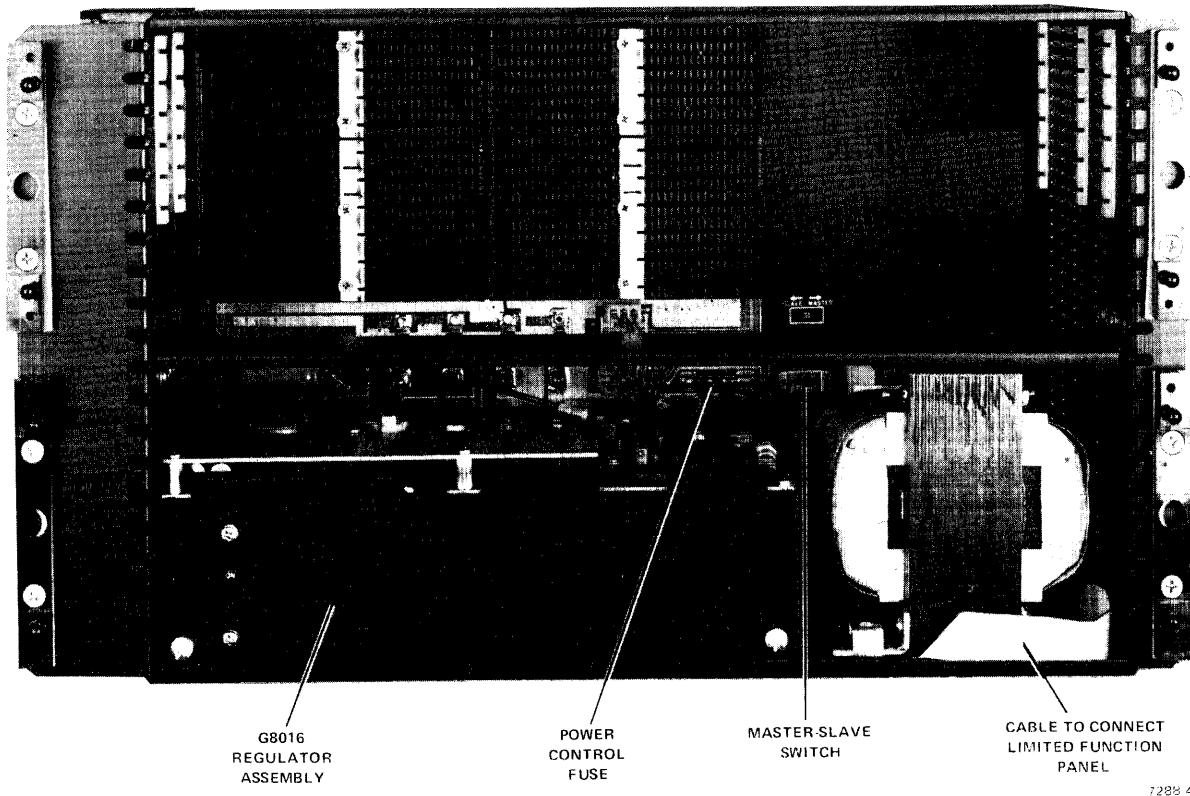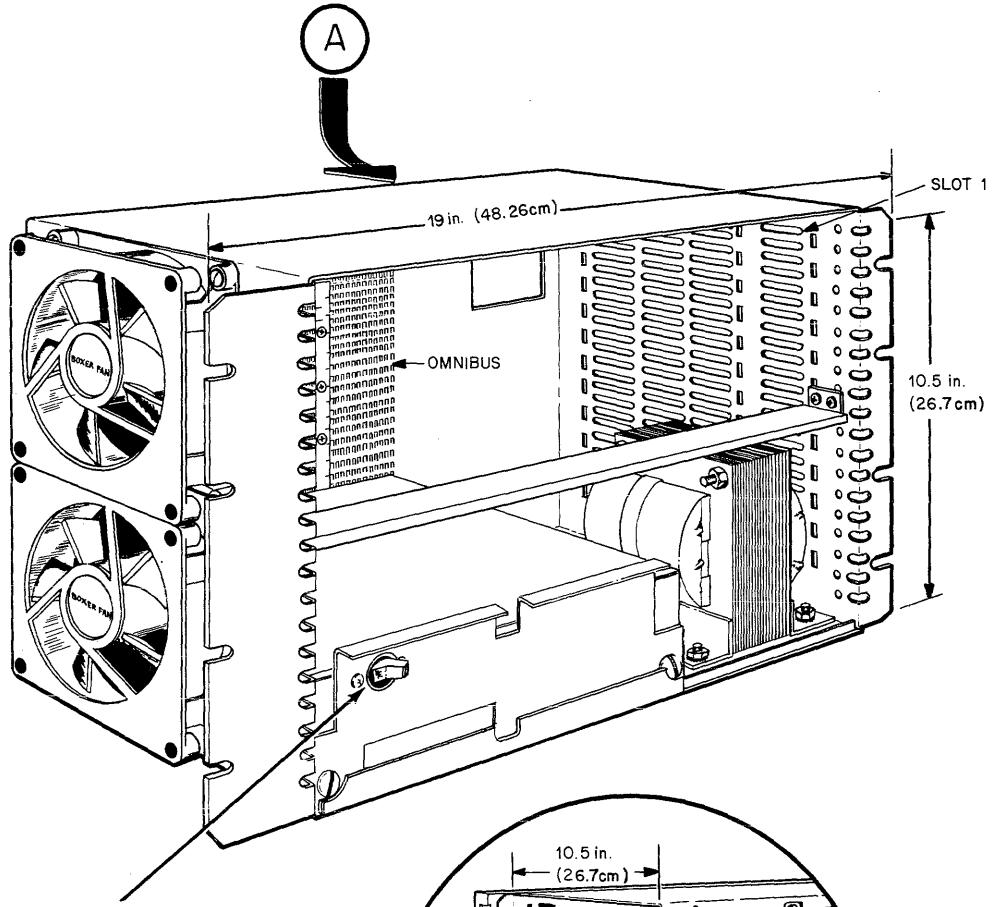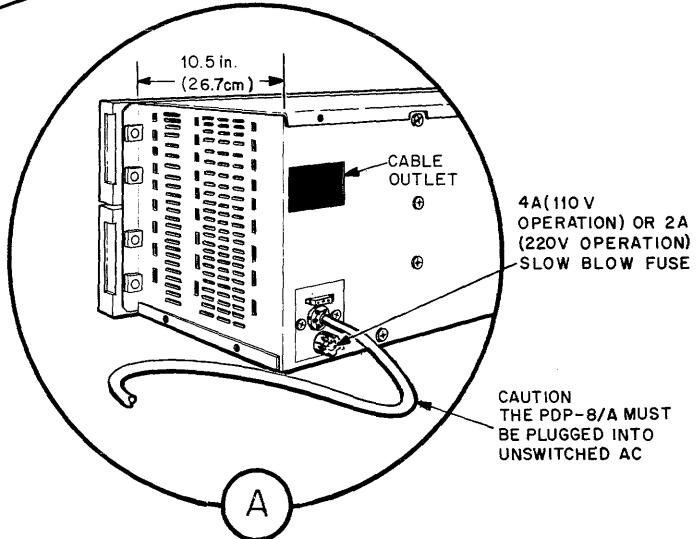
Figure 3-3   PDP-8/A Semiconductor Chassis

NOTE: This circuit breaker controls dc power applied to the OMNIBUS. It does not remove ac power from the power transformer or fans.

If you are servicing the power supply, you are advised to:
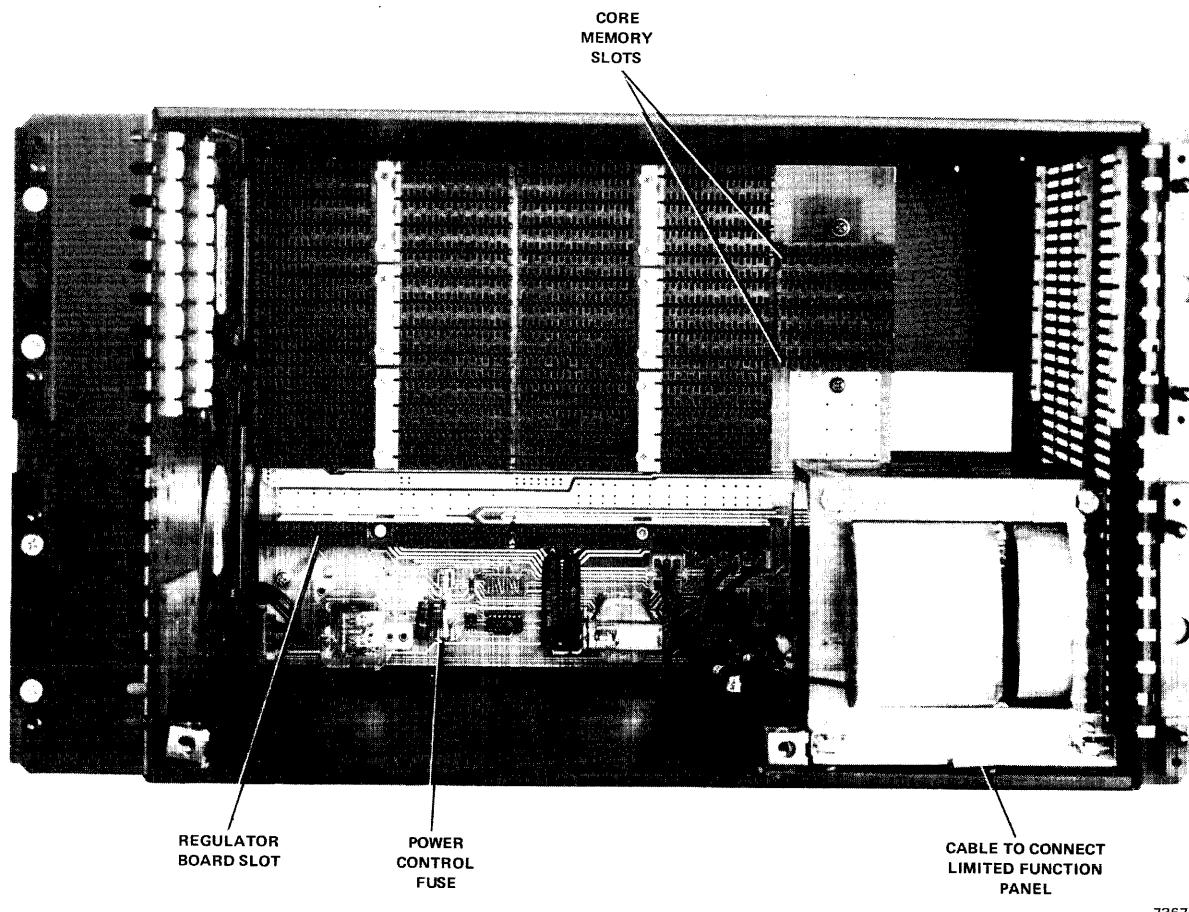
1. Turn PDP-8/A off.
2. Unplug the power cord.
3. Remove metal jewelry that could short the battery, heat up, and cause burns.

08-1146

Figure 3-4   PDP-8/A Semiconductor Computer Chassis Dimensions
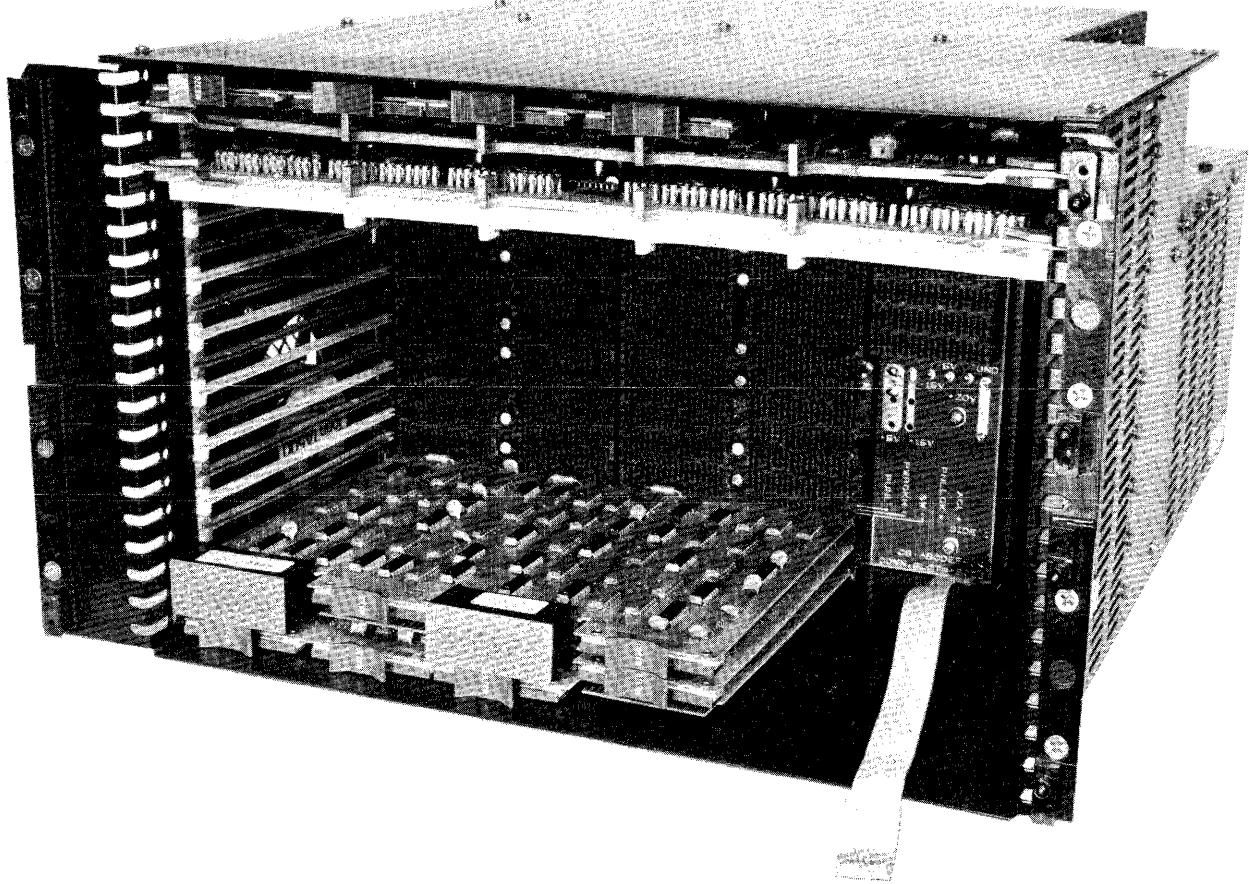
Figure 3-5 shows the chassis that is used with the 8A400, 8A600, and 8A800 computers. The dimensions are the same as the PDP-8/A semiconductor chassis; interior components are different. The G8018 Regulator Board assembly has been removed to show the connector in which the assembly is inserted. The Omnibus connector blocks in the connector "E" position are needed to accommodate the E connector of the core memory modules.
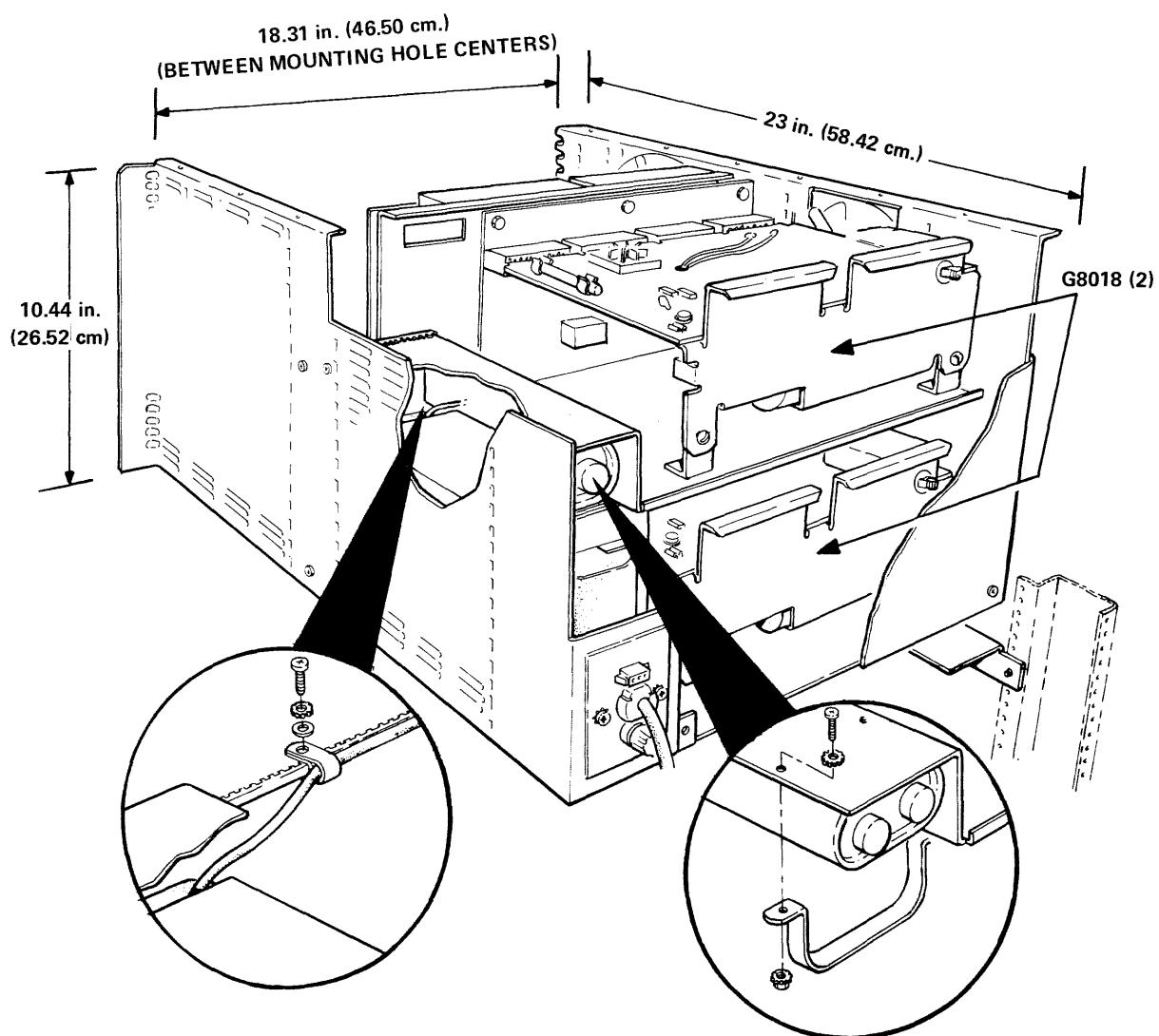
Figure 3-5   8A Chassis – H9300 (Transformer Cover Removed)

Figure 3-6 shows the chassis used with the 8A420, 8A620, and 8A820 computers. The example shown is an 8A620, containing the KK8-E CPU and Timing Generator and the Bus Loads module. The H9195 Omnibus is mounted on the center wall assembly (DEC Part Number 70-12561); modules are inserted from the front of the unit. Two G8018 Regulator Board assemblies are contained in the rear of the chassis; the regulator boards are inserted in PC board slots that are mounted on the rear of the center wall assembly. Figure 3-7 is an outline drawing that gives the chassis dimensions and illustrates the placement of the G8018 assembly.

7996-2

Figure 3-6   8A620 Chassis

18.31 in. (46.50 cm.)
(BETWEEN MOUNTING HOLE CENTERS)

23 in. (58.42 cm.)

10.44 in. (26.52 cm)

G8018 (2)
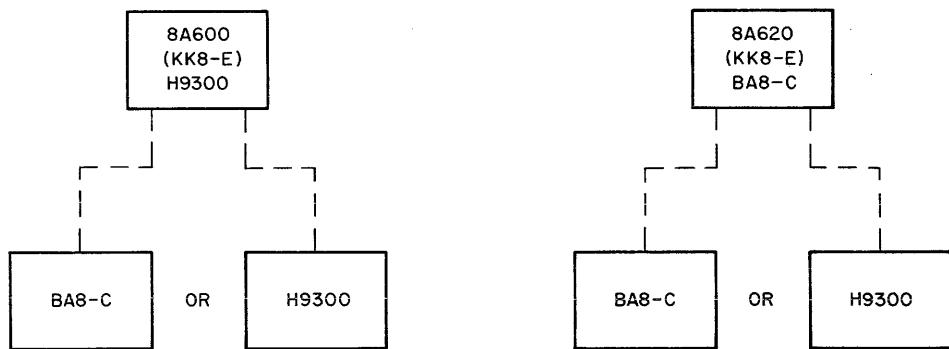
08-1788

Figure 3-7   8A420/8A620/8A820 Chassis Dimensions

3.3   EXPANSION TECHNIQUES

Table 3-1 noted that the 8A600 and 8A620 computers could be expanded. Either a BA8-C or an H9300 can be added to the basic chassis, increasing the system capacity accordingly. Figure 3-8 illustrates the basic chassis and the expansion possibilities available for each type.

The basic chassis is connected to the expander chassis by a ribbon cable. One cable connector is inserted into the bottom slot of the basic chassis (slot 12 or slot 20), the other connector is inserted into slot 1 of the expander chassis. The M8300, M8310, and M8330 modules must be removed from the basic chassis and placed in the appropriate Omnibus slots of the expander chassis, e.g., if expanding an 8A600 with a BA8-C chassis, insert the M8300, M8310, and M8330 modules in Omnibus slots 18, 19, and 20, respectively, of the BA8-C. If the computer includes a KE8-E option, this, too, must be removed from the basic chassis and inserted in the appropriate Omnibus slots of the expander.

3-8

```
        ┌──────────┐                              ┌──────────┐
        │  8A600   │                              │  8A620   │
        │ (KK8-E)  │                              │ (KK8-E)  │
        │  H9300   │                              │  BA8-C   │
        └──────────┘                              └──────────┘
         ┌───┘  └───┐                              ┌───┘  └───┐
         │          │                              │          │
     ┌───────┐  ┌───────┐                      ┌───────┐  ┌───────┐
     │       │  │       │                      │       │  │       │
     │ BA8-C │OR│ H9300 │                      │ BA8-C │OR│ H9300 │
     │       │  │       │                      │       │  │       │
     └───────┘  └───────┘                      └───────┘  └───────┘
```

NOTE:
Remove CPU modules from basic chassis and place them in expander chassis,
leaving bus loads in slot 1 of basic chassis.

08-1786

Figure 3-8   8A600/8A620 Expansion

3.4 PDP-8/A MODULE DESCRIPTIONS

The major units that constitute a PDP-8/A are described in the following paragraphs, along with the module switch settings. The most common switch settings are enclosed in boxes for easy identification.

CAUTION
**Switch settings may be accidently changed unless modules
are removed and inserted carefully.**

3.4.1 KK8-A Central Processor Unit (CPU)

The KK8-A, shown in Figure 3-9, is a multilayer hex module (M8315) which resides in the top slot of the Omnibus. The KK8-A has an Auto-Start feature, which is used to start the computer automatically when power is turned on.

> If you are not using the CPU Auto-Start feature, turn switch S1-7 ON and switches S1-1 through S1-6 and S1-8 OFF.

> If you are using the CPU Auto-Start feature, set switches as shown in Table 3-3.

CAUTION
**The direction of motion of the switch activating lever (slide
or rocker) varies with the switch manufacturer. Always
look for a printed ON on the switch assembly. If there is
no ON indication, look for a black dot on the rocker.
Depressing the end of the rocker with the dot on it puts the
switch in the ON position.**

3-9

REVISION LETT
ON UNDERSIDE
BOARD

S1-1

S1-8

D   C   B   A
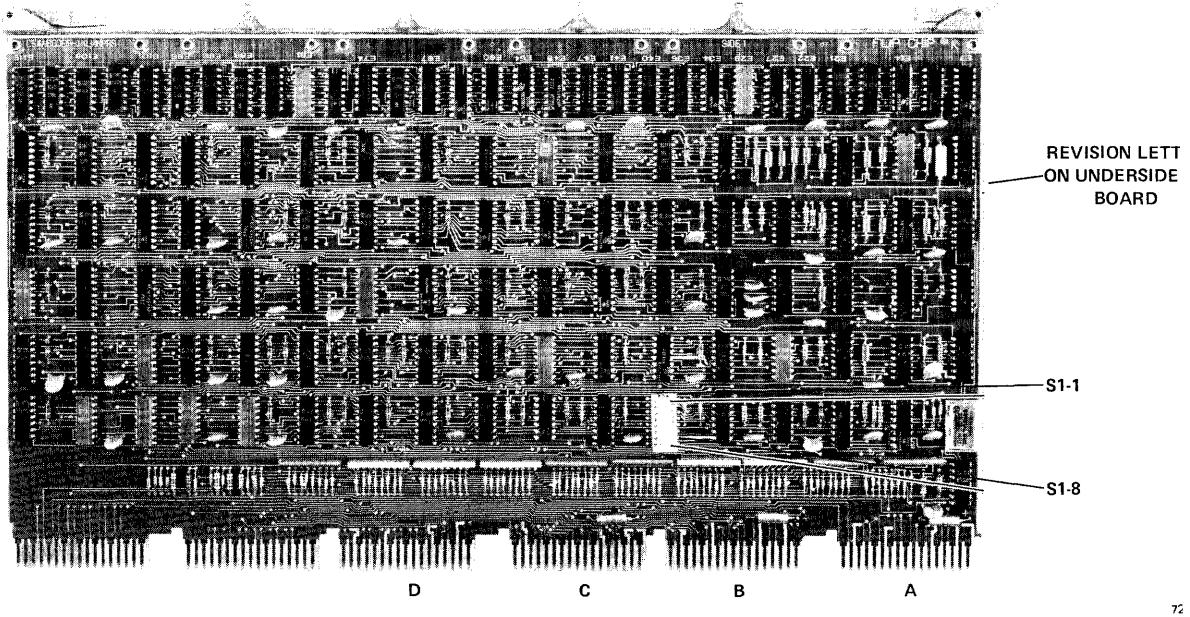
Figure 3-9   KK8-A (M8315) CPU Module

Table 3-3
KK8-A (M8315) Central Processor Unit Switch Settings

Switch	Function (When in the "ON" Position)
S1-1	Start in memory field 7; (OFF position specifies Field 0)
S1-2	Start at address 4000
S1-3	Start at address 2000
S1-4	Start at address 1000
S1-5	Start at address 0400
S1-6	Start at address 0200
S1-7	CPU Auto-Start Disabled
S1-8	OFF
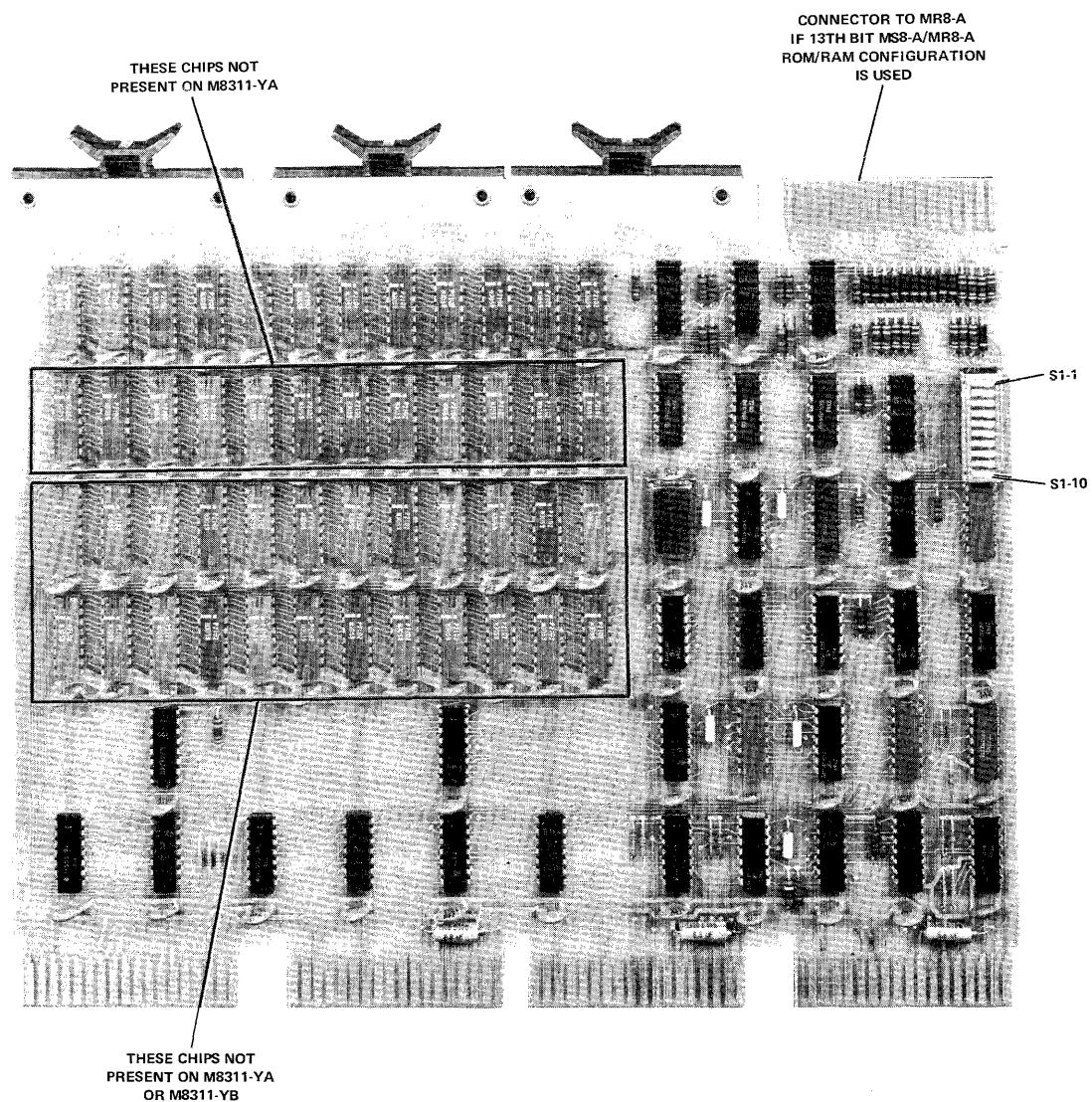
Starting address 0000 may be selected by leaving switches S1-2 through S1-6 OFF. Only one switch in the group S1-2 through S1-6 may be ON at any time. Failure to observe this precaution will result in a malfunction, even if the Auto-Start feature is not used.

3.4.2 MS8-A Read/Write Random Access Memory (RAM)

The MS8-A, shown in Figure 3-10, is a quad module (M8311), semiconductor, read/write, random access memory and is available in the following configurations:

Option	Memory Size	Module Number
MS8-AA	1K	M8311-YA
MS8-AB	2K	M8311-YB
MS8-AD	4K	M8311-YD

> If you are using a 4K RAM in Field 0, set switches S1-1 through S1-6 and S1-10 ON and turn S1-7, 8, and 9 OFF.

CONNECTOR TO MR8-A
IF 13TH BIT MS8-A/MR8-A
ROM/RAM CONFIGURATION
IS USED

THESE CHIPS NOT
PRESENT ON M8311-YA

S1-1

S1-10

THESE CHIPS NOT
PRESENT ON M8311-YA
OR M8311-YB

7015-8

Figure 3-10   MS8-A (M8311) Read/Write Random Access Memory

Set switches as shown in Table 3-4 if other memory configurations are used.

Table 3-4
MS8-A Read/Write Memory Switch Settings

S1-1,2, and 3	Field Selection			
	S1-1	**S1-2**	**S1-3**	**Field Selected**
	ON	ON	ON	0
	OFF	ON	ON	1
	ON	OFF	ON	2
	OFF	OFF	ON	3
	ON	ON	OFF	4
	OFF	ON	OFF	5
	ON	OFF	OFF	6
	OFF	OFF	OFF	7
S1-4 and 5	First Address			
	S1-4	**S1-5**	**First Address in this RAM**	
	ON	ON	0000	
	ON	OFF	2000	
	OFF	ON	4000	
	OFF	OFF	6000	
S1-6	ON for 4K Memory M8311-YD, OFF for 1K or 2K			
S1-7	OFF			
S1-8	ON for 2K Memory M8311-YB, OFF for 1K or 4K			
S1-9	ON for 1K Memory M8311-YA, OFF for 2K or 4K			
S1-10	Test switch, normally ON			

3.4.3 MR8-A Read-Only Random Access Memory (ROM)

The MR8-A, shown in Figure 3-11, is a quad module (M8312), read-only, random access memory and is available in the following configurations:

Option	Memory Size	Module Number
MR8-AA	1K	M8312-YA
MR8-AB	2K	M8312-YB
MR8-AD	4K	M8312-YD

THESE THREE CONNECTORS ARE REMOVED
TO PROGRAM THE ROM, BUT THEY MUST
BE IN PLACE FOR NORMAL OPERATION

CONNECTOR TO MS8-A
IF 13TH BIT MS8-A/MR8-A
ROM/RAM CONFIGURATION
IS USED

7230-1
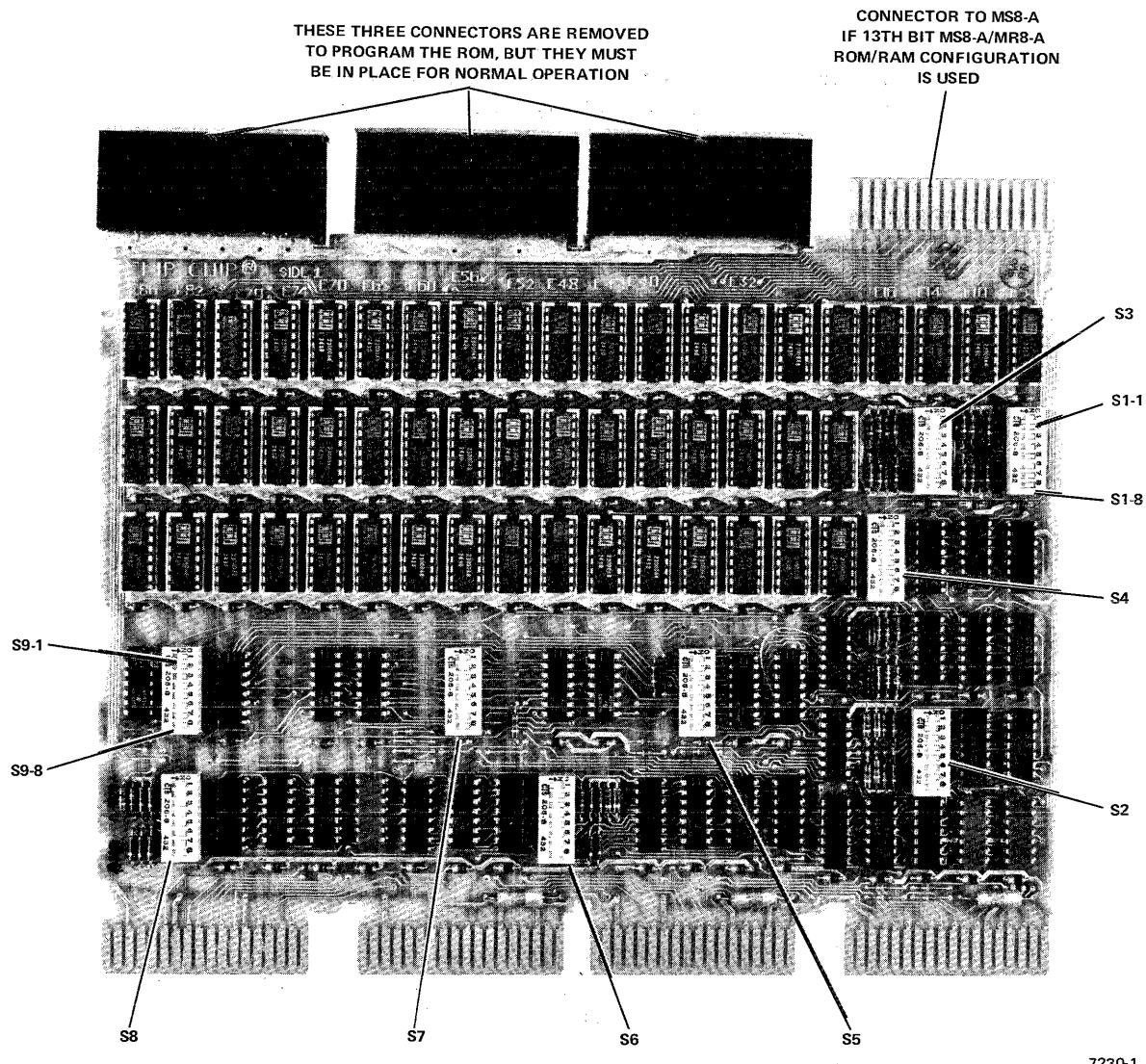
Figure 3-11 MR8-A (M8312) Read Only Memory (ROM)

The first address is always location 0000 of the selected memory field.

If you are using a 4K ROM in Field 0 with no connections to RAM, set the following switches ON: S1-1 through S1-8; S3-1 through S3-8; S5-1 through S5-8; S7-1 through S7-8; S8-1 through S8-8; S9-1 through S9-8; S4-1, 2, 3, 4, 6, 7; and S6-3 through S6-8. Set the following switches OFF: S2-1 through S2-8; S4-5, 8; S6-1, 2. If a RAM is used with top connectors, change S4-7 to OFF and S4-8 to ON.

Set switches as shown in Table 3-5 if other configurations are used.

CAUTION
All switches must be OFF when the M8312 is being pro-
**grammed (i.e., while data is being loaded into ROM).**
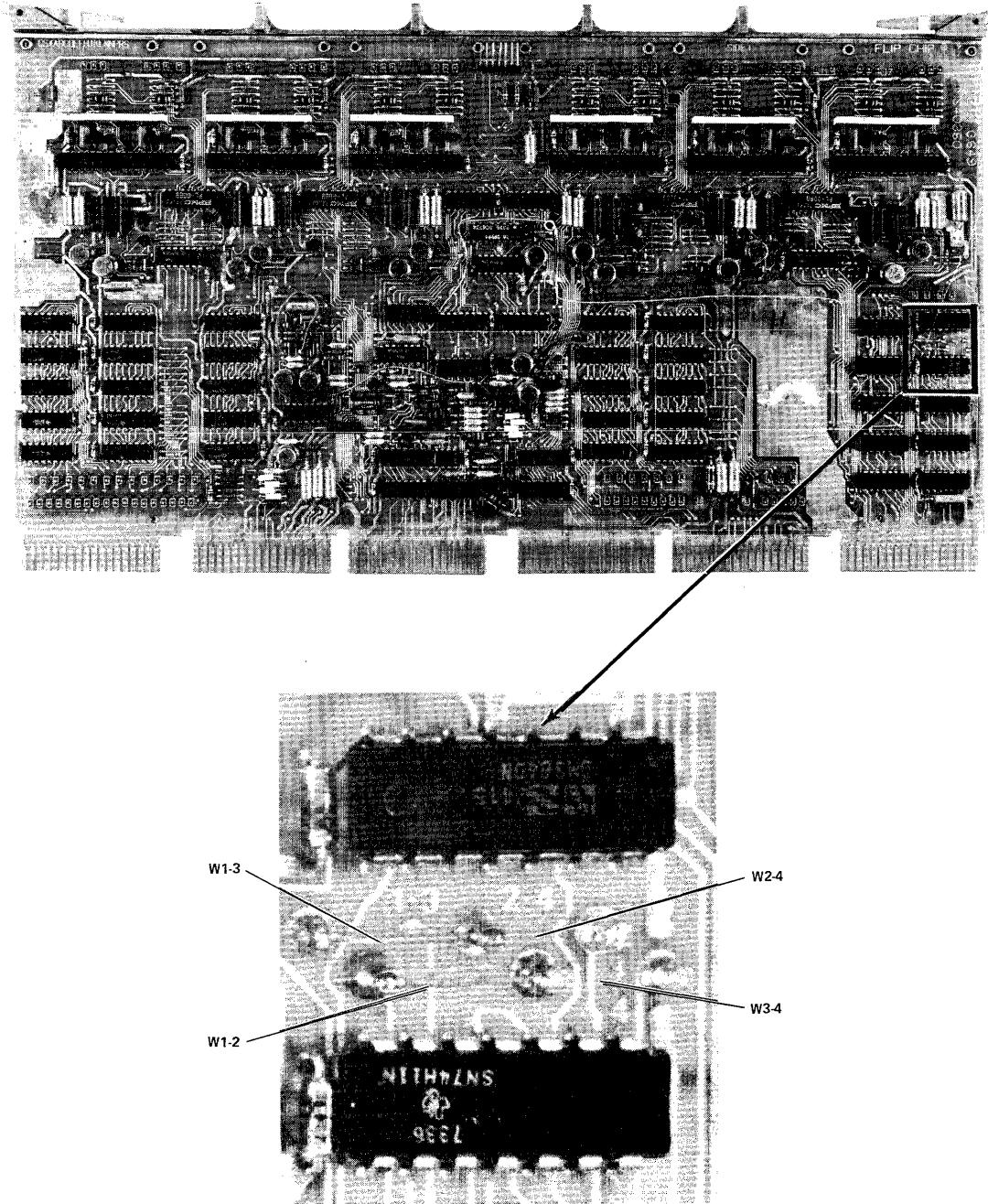
Table 3-5
MR8-A Read Only Memory Switch Settings

Switch	Function/Position			
S1-1 to S1-8	ON			
S2-1,8, and 5	Size Select Switch Settings			
	S2-1	**S2-8**	**S2-5**	**Memory Size**
	ON	ON	OFF	1K
	ON	ON	OFF	2K
	OFF	OFF	OFF	4K
S2-2 and 4	OFF			
S2-3,6 and 7	Field Select Switch Settings			
	Field	**S2-6**	**S2-3**	**S2-7**
	0	OFF	OFF	OFF
	1	ON	OFF	OFF
	2	OFF	ON	OFF
	3	ON	ON	OFF
	4	OFF	OFF	ON
	5	ON	OFF	ON
	6	OFF	ON	ON
	7	ON	ON	ON
S3-1 to S3-8	ON			
S4-1,2,3,4, and 6	ON			
S4-5	OFF			
S4-7	OFF for ROM/RAM Combination; otherwise ON			
S4-8	ON for ROM/RAM Combination; otherwise OFF			
S5-1 to S5-8	ON			
S6-1 and S6-2	OFF			
S6-3,4,5,6,7, and 8	ON			
S7-1 to S7-8	ON			
S8-1 to S8-8	ON			
S9-1 to S9-8	ON			

3.4.4 MM8-AA 8K Core Memory

The MM8-AA, shown in Figure 3-12, is a hex module (G649) with an H219-A Stack Assembly that contains 8K of core memory.

> If you are using core memory in Fields 0 and 1, install
> W1-3 and W1-2 and remove W2-4 and W3-4.

7388-2

Figure 3-12   MM8-AA 8K Core Memory

3-15

Install or remove jumpers as shown in Table 3-6 if other memory fields are in use.

Table 3-6
MM8-AA 8K Core Memory Jumper Installation

Fields Used	W1-3	W1-2	W2-4	W3-4
0 and 1	In	In	Removed	Removed
2 and 3	Removed	In	In	Removed
4 and 5	In	Removed	Removed	In
6 and 7	Removed	Removed	In	In

3.4.5 MM8-AB 16K Core Memory
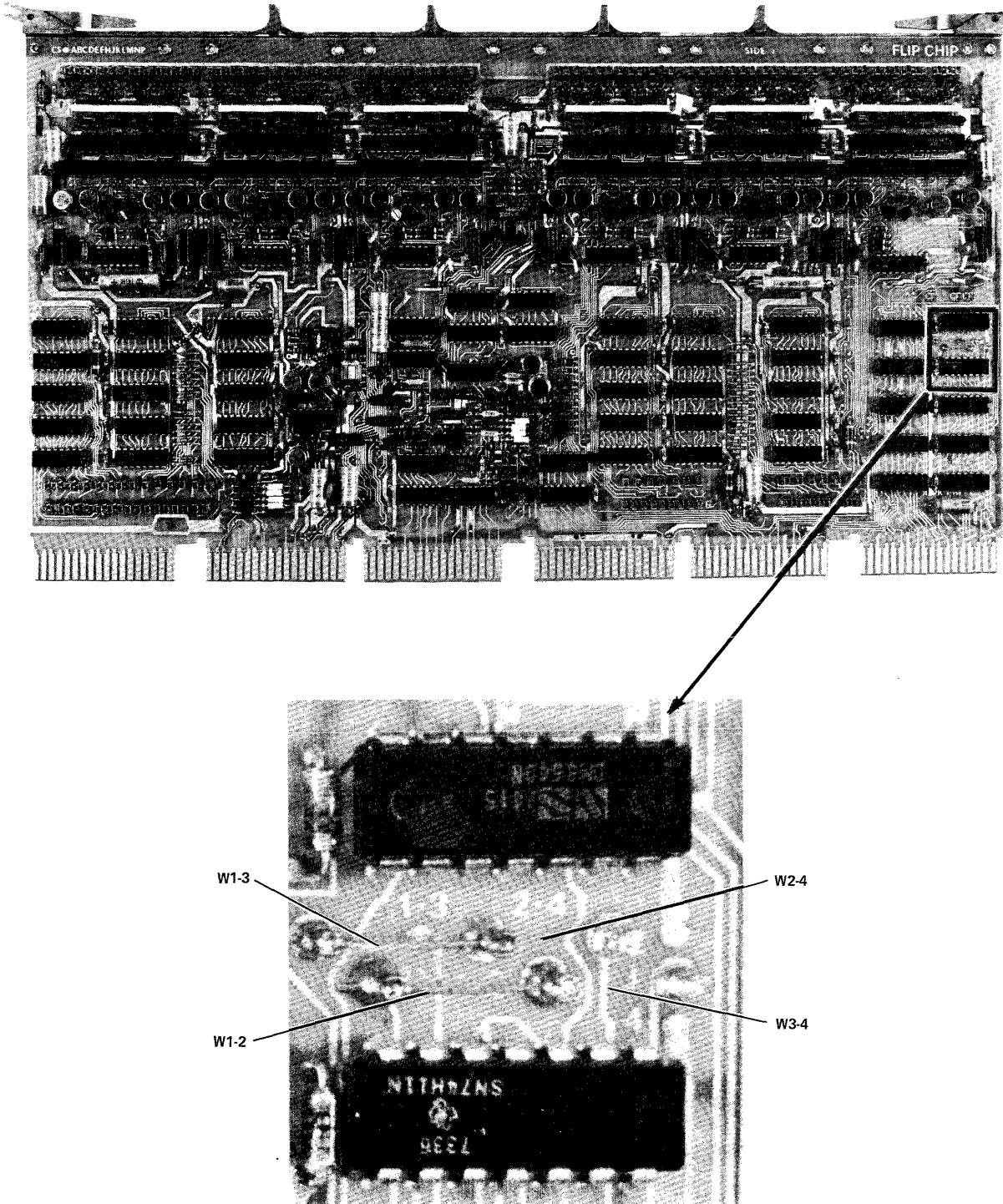
The MM8-AB, shown in Figure 3-13, is a hex module (G650) with an H219-B Stack Assembly that contains 16K of core memory.

> If the MM8-AB is installed in Fields 0 through 3, jumpers W1-3 and W1-2 should be installed and W2-4 and W3-4 should be removed.

Install or remove jumpers as shown in Table 3-7 if other memory fields are used.

Table 3-7
MM8-AB 16K Core Memory Jumper Installation

Fields Used	W1-3	W1-2	W2-4	W3-4
0 to 3	In	In	Out	Out
4 to 7	Out	In	In	Out

Figure 3-13   MM8-AB 16K Core Memory

3.4.6 DKC8-AA I/O Option Board

There are two DKC8-AA hex modules (M8316) in existence; one is defined as etch revision C (shown in Figure 3-14), the other as etch revision D (shown in Figure 3-15). The etch revision is identified on side 2 of the PC board (side 1 is the component side). Lettering similar to the following appears near the lower right corner (when viewing side 2).

    Option Board 1
    Side 2
    M8316
    5010900D

The letter D indicates the D etch revision. The information in this section is not totally applicable to each revision level; differences that exist are indicated in the description.
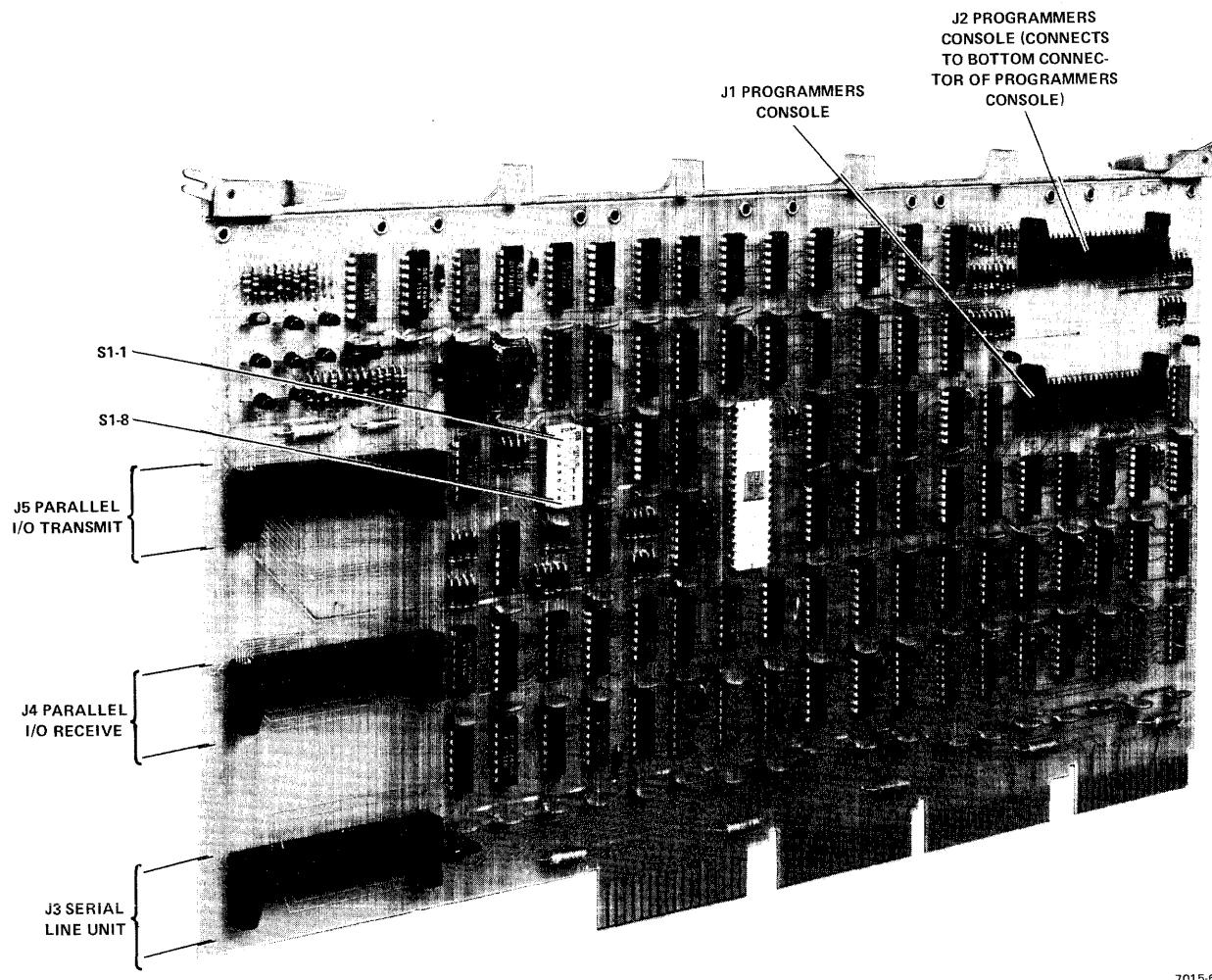
Figure 3-14   DKC8-AA (M8316) I/O Option Board

3-18

REVISION LETTER
ON UNDERSIDE
OF BOARD (SIDE 2)

J5
PARALLEL I/O
TRANSMIT

SIDE 1

J2 PROGRAMMER'S
CONSOLE (CONNECTS)
TO BOTTOM CONNECTOR OF
PROGRAMMER'S CONSOLE

F

J3
SERIAL
LINE UNIT

E

J4
PARALLEL I/O
RECEIVE

S1-1   S1-10

D

C

B

J1
PROGRAMMERS
CONSOLE

A

8071-1
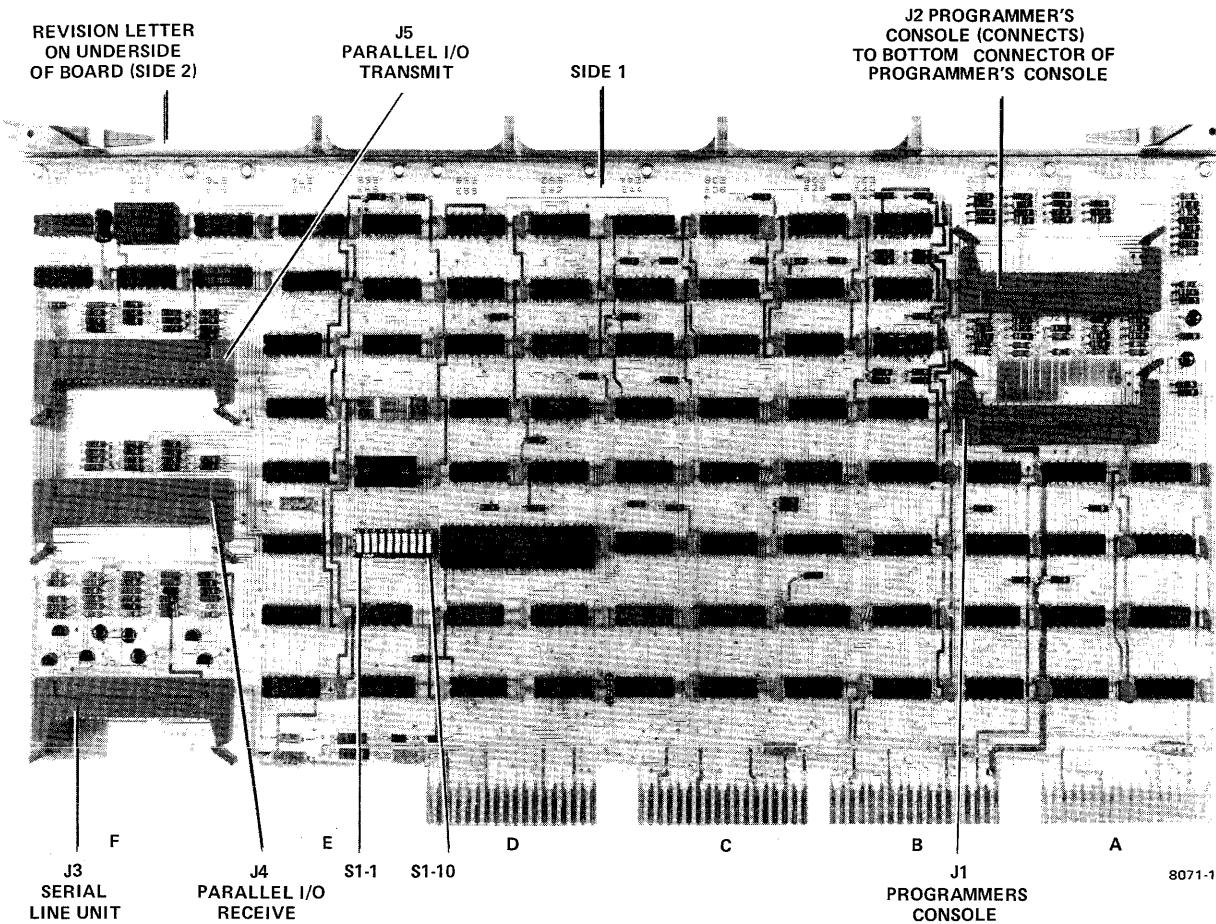
Figure 3-15   D Etch Revision of DKC8-AA (M8316) I/O Option Board

The DKC8-AA combines four options:

1. Serial Line Unit (SLU), 110 to 9600 (50 to 9600 for revision D) baud rate interface for Teletype,®
   VT50, or other compatible serial line unit

2. Real-Time Clock – Crystal controlled at 100 Hz

3. General-Purpose Parallel I/O – 12-bit I/O for user's device or another PDP-8/A

NOTE
The General-Purpose Parallel I/O on the D etch revision
of the M8316 module can be used as an interface for the
LA180. Data to the LA180 must be supplied in com-
plemented form. The IOTs are different from the LA8
interface designed for the LA180. A BC80-A cable, avail-
able from DIGITAL, must be used to connect the General-
Purpose Parallel I/O to the LA180.

®Teletype is a registered trademark of Teletype Corporation.

4. Console Logic – Logic to connect the KC8-AA Programmer's Console to the Omnibus

> Revision C: For Teletype (ASR33) operation without real-time clock software, set switches S1-4, 6, and 8 to the ON position; set switches S1-1, 2, 3, 5, and 7 to the OFF position.

> Revision D: For Teletype (ASR33) operation without real-time clock software, set switches S1-1, 3, 4, 6, 8, and 9 to the ON position; set switches S1-2, 5, and 7 to the OFF position. (S1-10 is a spare.)

For other operation, set switches as shown in Tables 3-8 and 3-9.

Table 3-8
DKC8-AA I/O Option Board Switch Settings, C-Etch Module

Switch	Function
S1-1,2 and 3	Baud Rate as shown in Table below:

S1-1	S1-2	S1-3	Baud Rate
OFF	OFF	OFF	110
OFF	OFF	ON	150
OFF	ON	OFF	300
OFF	ON	ON	600
ON	OFF	OFF	1200
ON	OFF	ON	2400
ON	ON	OFF	4800
ON	ON	ON	9600

Switch	Function
S1-4	Clear Data Available at Time State 1 (normally ON)
S1-5	ON enables Real Time Clock
S1-6	Test (normally ON, OFF for special testing)
S1-7	ON for 1 stop bit, OFF for two stop bits
S1-8	ON enables TTY filter in 20 mA CKT (used only for 100 baud)

Table 3-9
DKC8-AA Option Board Switch Settings, D-Etch Module

Switch	Function
S1-1, 2, 3, and 4	Baud rate as shown in table below:

S1-4	S1-3	S1-2	S1-1	Baud Rate
ON	ON	ON	ON	50
ON	ON	ON	OFF	75
ON	ON	OFF	ON	110
ON	ON	OFF	OFF	134.5
ON	OFF	ON	ON	150
ON	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	1200
OFF	ON	ON	ON	1800
OFF	ON	ON	OFF	2000
OFF	ON	OFF	ON	2400
OFF	ON	OFF	OFF	3600
OFF	OFF	ON	ON	4800
OFF	OFF	ON	OFF	7200
OFF	OFF	OFF	ON	9600
*OFF	OFF	OFF	OFF	19.2K

Switch	Function
S1-5	ON = Real Time Clock enabled OFF = Read Time Clock disabled
S1-6	ON = Test Switch (always ON)
S1-7	ON = 1 Stop Bit in SLU character OFF = 2 Stop Bits in SLU character
S1-8	ON = ASR/KSR 33 DR35 filter in (across SLU 20 mA REC'V Leads. ON if Baud Rate is 110 or below.) OFF - filter out
S1-9	ON = TS1 clears DATA AVAIL flip-flop in Parallel I/O Section OFF = DATA AVAIL not cleared by TS1

*Serial Line will *not* run at this baud rate.   This setting is *not* to be used.

3.4.7 KM8-A Extended Option Board

The KM8-A, shown in Figure 3-16, is a hex module (M8317) that combines the following options:

Power-Fail/Auto-Restart
Bootstrap Loaders – Provide commonly used I/O loaders
Memory Extension and Timeshare Control

> If you are using paper tape under control of the boot-
> strap switches, no Auto-Restart, and timeshare enabled,
> set the following switches ON: S1-1 through S1-4, S1-8,
> S2-1, S2-5 through S2-7; set the following switches OFF:
> S1-5 through S1-7, S2-2 through S2-4, and S2-8.

7299-1
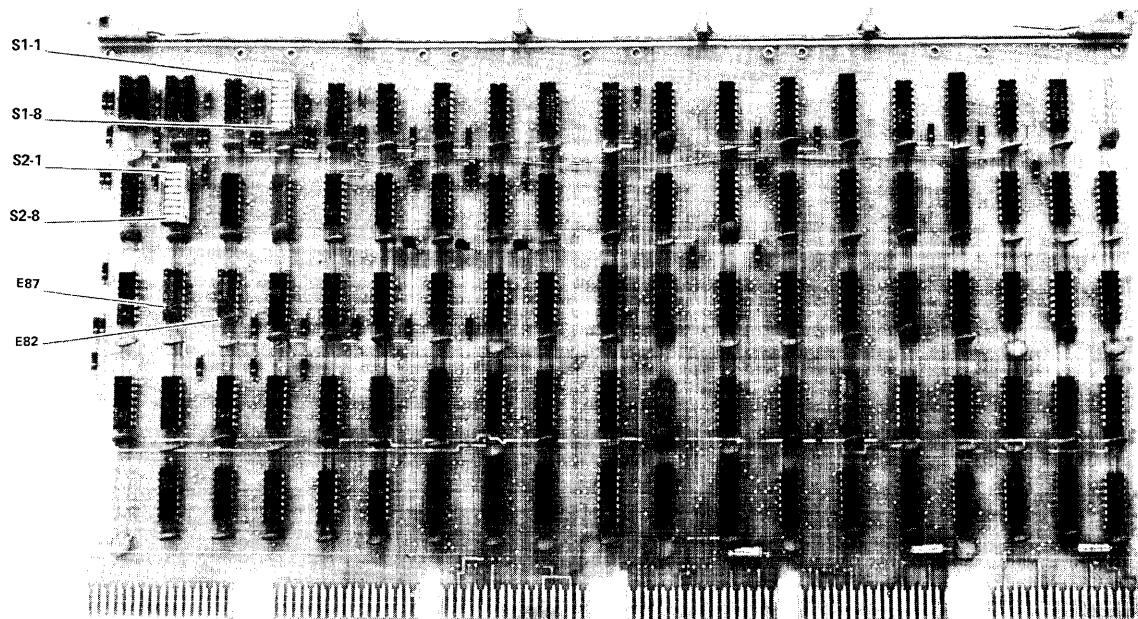
Figure 3-16   KM8-A (M8317) Extended Option Board

Other switch settings for the KM8-A are listed in Tables 3-10 through 3-14.

NOTE

There are three types of bootstrap ROMs used on the KM8-A. E82 and E87 have different labels for the different bootstrap ROMs. Switches on modules that have E82 and E87 (Figure 3-16) labeled 87A2 and 88A2 should be set according to Table 3-11. If E82 and E87 are labeled 158A2 and 159A2, use Table 3-12 for switch settings. For CL8 systems using the RX8-E, E82 and E87 are labeled 156A2 and 157A2; use Table 3-13. (If Table 3-13 is used, Auto-Restart address 0 must be selected, i.e., S2-2 is OFF, S2-3 is OFF, and S2-4 is OFF.)

Table 3-10
Auto-Restart Select Switch Settings

Restart Address	S2-2	S2-3	S2-4
0	OFF	OFF	OFF
200	OFF	ON	OFF
2000	ON	OFF	OFF
4200	ON	ON	OFF

Table 3-11
Bootstrap Select Switch Settings
for ROMs Labeled 87A2 and 88A2

Program	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	Memory Address
Hi-Lo RIM*	ON	ON	ON	OFF	ON	ON	ON	7737
RK8-E*	ON	OFF	ON	OFF	ON	OFF	ON	0024
TC08*	ON	OFF	OFF	ON	OFF	ON	ON	7613
RF08/DF32D*	OFF	ON	ON	ON	ON	OFF	OFF	7750
TA8-E*	OFF	ON	ON	OFF	ON	OFF	OFF	4000

*May only be used with 4K of Read/Write Memory in Field 0.

Table 3-12
Bootstrap Select Switch Settings for ROMs
Labeled 158A2 and 159A2

Program	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	Memory Address
Hi-Lo RIM	ON	ON	ON	OFF	ON	ON	ON	7737
RK8-E	ON	OFF	ON	OFF	ON	OFF	ON	0024
RX8-E	ON	OFF	OFF	ON	OFF	ON	ON	0033
RF08/DF32D	OFF	ON	OFF	ON	OFF	ON	OFF	7750
TA8-E	OFF	ON	OFF	OFF	OFF	ON	OFF	4000

Table 3-13
Bootstrap Select Switch Settings
for ROMs Labeled 156A2 and 157A2

Program	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	First ROM Address	First Memory Address
RX8E TEST	ON	ON	ON	ON	ON	OFF	ON	004	0000

Table 3-14
Bootstrap/Auto-Restart Switch Settings

Feature	Start Switch or Activating Signal	Switches		
		S1-6	S1-7	S1-8
Bootstrap Enabled And Auto Restart Disabled	BOOT Key	OFF	OFF	ON
Bootstrap Enabled And Auto Restart Enabled	BOOT Key or AC OK*	ON	ON	ON
Bootstrap Disabled And Auto Restart Enabled	AC OK*	ON	ON	OFF
Bootstrap Enabled And Auto Restart Disabled	AC OK*	ON	OFF	OFF
Bootstrap Enabled And Auto Restart Disabled	AC OK* or BOOT Key	ON	OFF	ON
Bootstrap And Auto Restart Disabled		OFF	OFF	OFF
		S2-1		
Time Share Enabled		OFF		
Time Share Disabled		ON		
		S1-4		
Bootstrap Activated In Run Or Stopped State		OFF		
Bootstrap Activated In Stopped State Only		ON		
Not Used		S1-5		

*Starts if power voltage becomes adequate.

3.4.8 Semiconductor Memory Power Supply

The H763 Semiconductor Memory Power Supply can supply 20 A at 5.0 V. It will support only semiconductor memory (RAM and ROM). The regulator (G8016, shown in Figure 3-17) plugs into a dedicated backplane slot near the bottom of the chassis. The power supply has battery backup for power failures. The machine will be totally supported for approximately 30–40 seconds after an ac line failure.
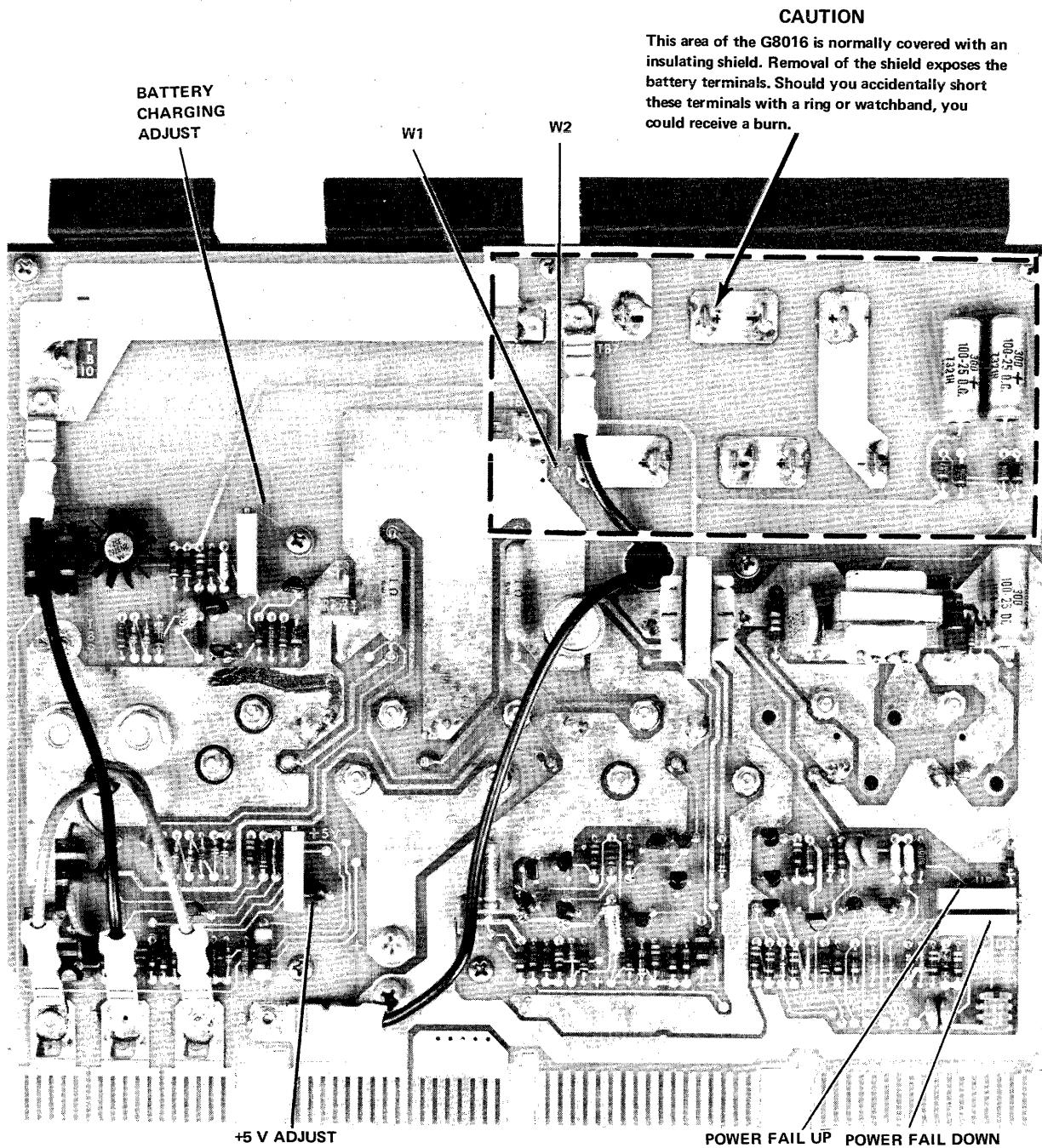
Figure 3-17   Semiconductor Memory Regulator Board (G8016)

To enable control of the PDP-8/A system power from the ON-OFF switch, set the MASTER/SLAVE switch to the MASTER (to the right) position. (The switch is identified in Figure 3-3.)

NOTE
All PDP-8/A dc power supply outputs are provided to drive logic inside the chassis. DIGITAL is not responsible for the performance of the PDP-8/A if any dc power is used outside of the chassis.

CAUTION
Refer to Appendix D (Omnibus Loading Chart) to ensure current rating is not exceeded.
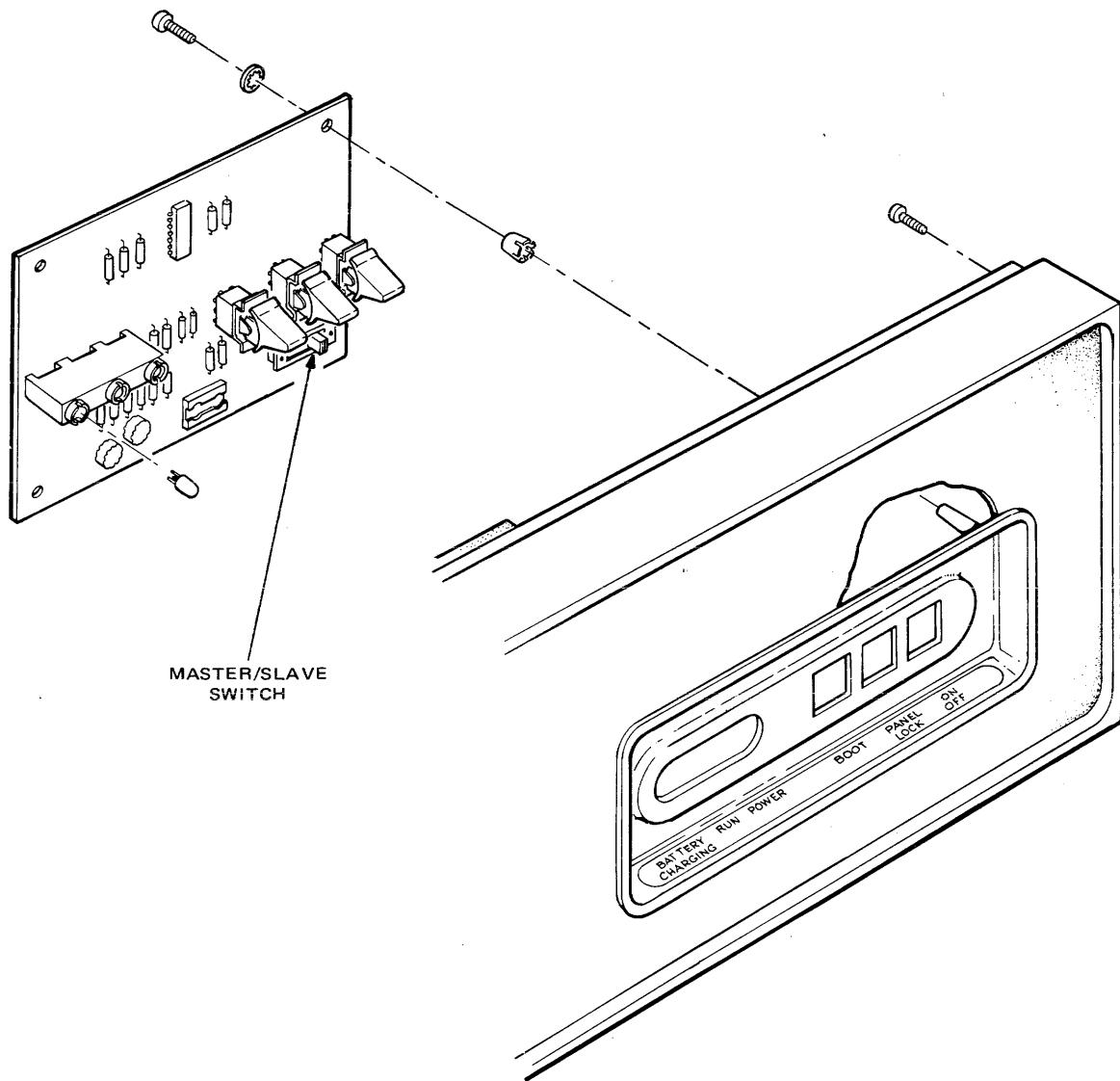
In the 8A computers, the MASTER/SLAVE switch is mounted on the printed circuit board that includes the ON/OFF, PANEL LOCK, and BOOT switches. This board is attached to the rear of the Limited Function Panel; remove the panel to gain access to the MASTER/SLAVE switch. The switch is illustrated in Figure 3-18; it is shown in the MASTER position (to the right when viewing the front of the switch).

3.4.9 Core Memory Power Supply Regulator
The core memory power supply supplies the following voltages at the currents specified:

+5 V at 25 A
−5 V at 2 A
+15 V at 2 A
−15 V at 2 A
+20 V at 4 A

The G8018 regulator (Figure 3-19) plugs into a dedicated backplane slot near the bottom of the chassis. (The board slot is pictured in Figure 3-5.)

MASTER/SLAVE
SWITCH

08-1787

Figure 3-18   8A Master/Slave Switch

ADJUSTMENT
TOOL MUST
ENTER HERE
FOR +5V
ADJUSTMENT

ADJUSTMENT
TOOL MUST
ENTER HERE
FOR +20 VOLT
ADJUSTMENT

+5V
CIRCUIT
BREAKER

POWER OK LIGHT
(LIT WHEN ALL DC
VOLTAGES ARE
PRESENT)

+20 V ADJUSTMENT

+5 V ADJUSTMENT   −5 V FUSE   POWER   POWER   +20 V FUSE   +15 V FUSE   −15 V FUSE
(2.5 A)   FAIL   FAIL   (4 A)   (2.5 A)   (2.5 A)
UP   DOWN

7404-1
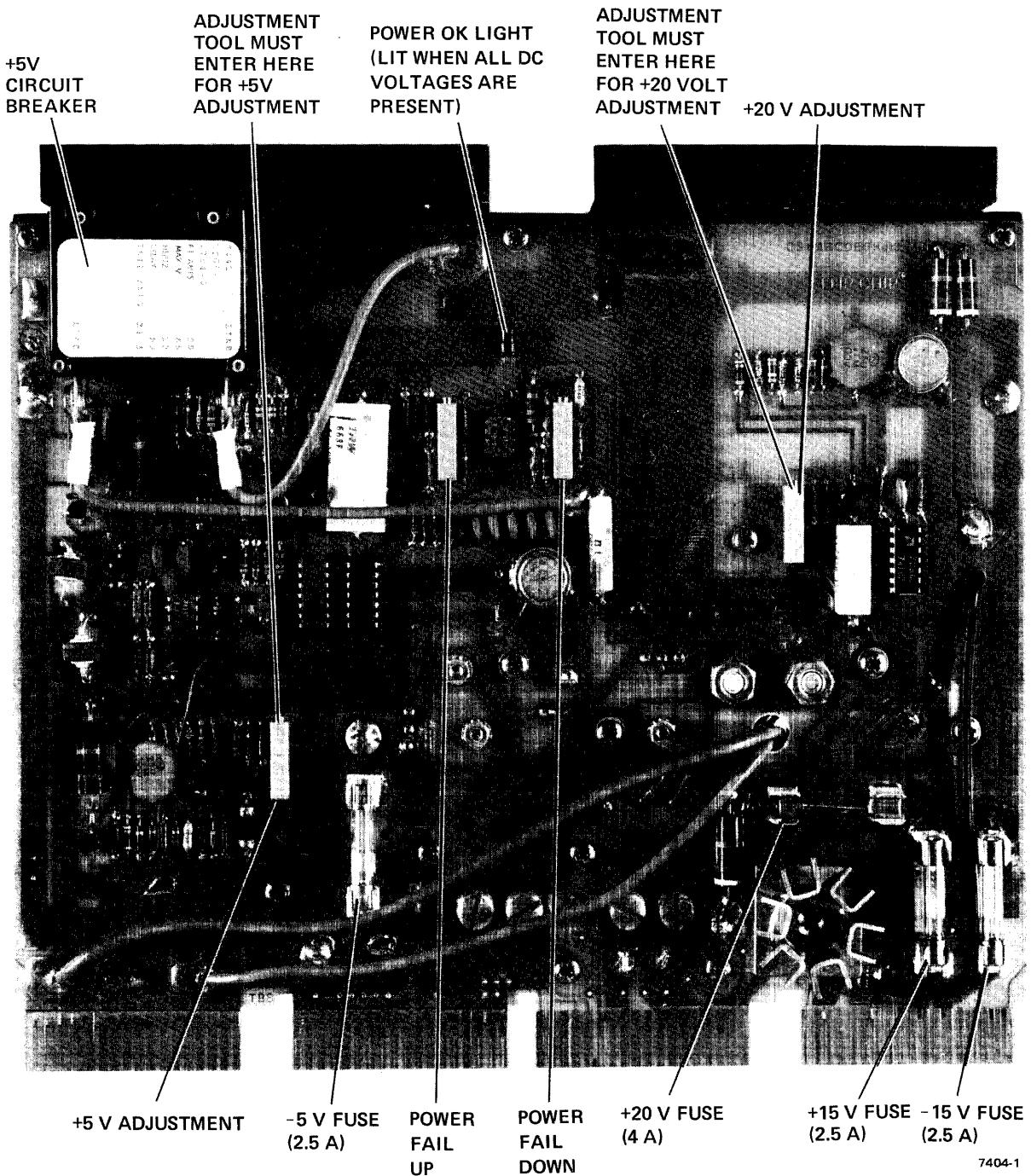
Figure 3-19   Core Memory Regulator Board (G8018)

3-28

3.4.10 Limited Function Panel (Figure 3-20)

The Limited Function Panel has three external switches and three indicator lights as defined below. (The MASTER/SLAVE switch is mounted in the rear of the panel for 8A computers.)
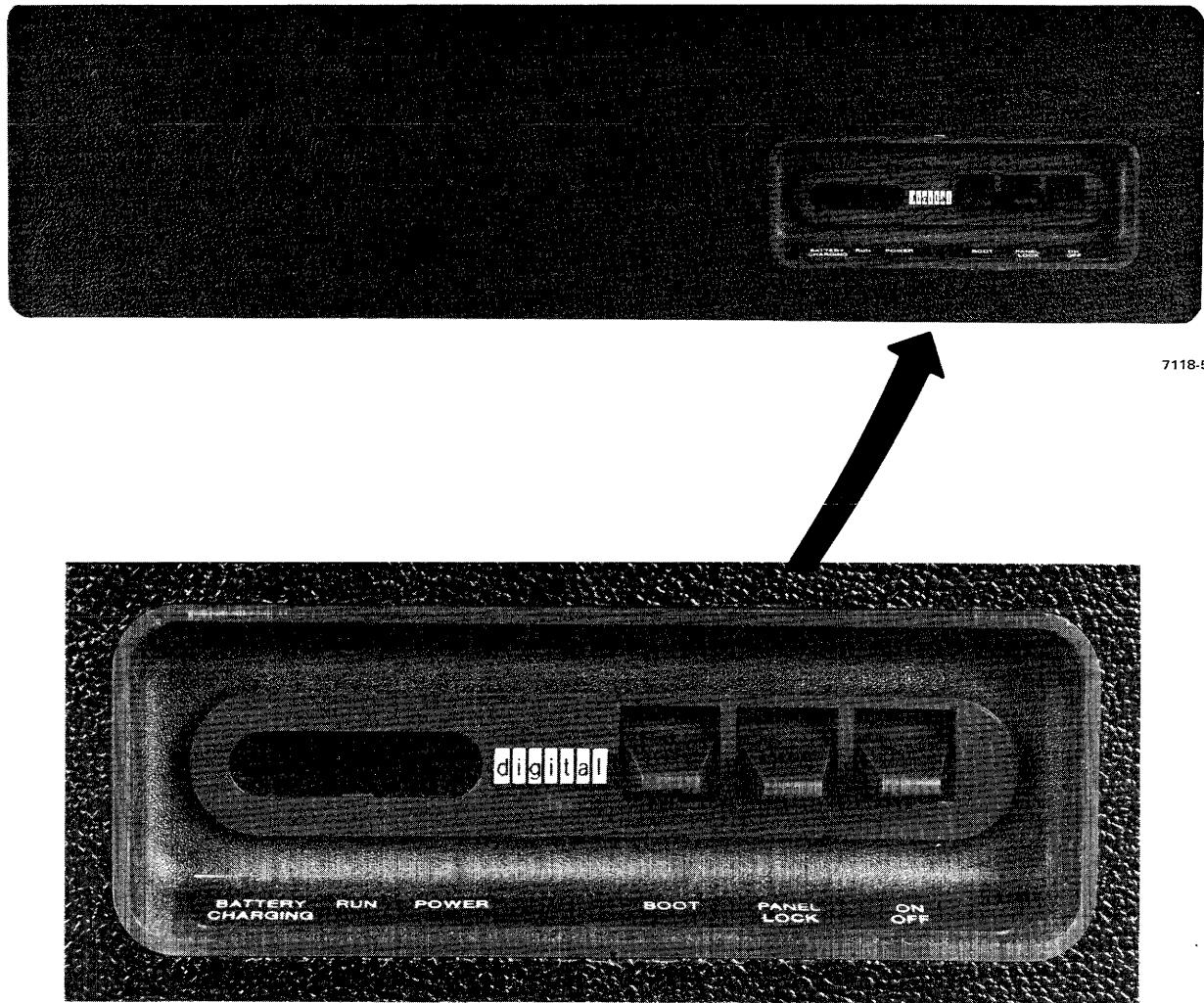
Figure 3-20   Limited Function Panel

Lights

The POWER light, which indicates that the PDP-8/A is operating on ac power.

The RUN light, which indicates that the PDP-8/A RUN flip-flop is set.

The BATTERY CHARGING light indicates either that the power supply battery is being charged (PDP-8/A semiconductor computer) or that both G8018 regulators are operating properly (8A420, 8A620, and 8A820 computers). The light is present on the 8A400, 8A600, and 8A800 computers but is not used.

Switches

The ON-OFF switch, which turns ac power on when in the up position. (This switch will not turn battery power on unless ac is present.) Turn power off before removing the power cord from the wall receptacle; otherwise, the PDP-8/A will run on battery power for as long as the battery lasts.

On those systems having a Programmer's Console, the PANEL LOCK switch disables the following switches: HLT/SS, E NEXT, E THIS, D THIS, D NEXT, LA, LXA, INIT, BOOT, and RUN. The down position activates the Programmer's Console; the up position panel-locks the console.

The BOOT switch initiates the bootstrap function (if it is enabled) on the KM8-A Extended Option Board (M8317). It is normally left in the down position. The BOOT switch is not affected by PANEL LOCK.

3.4.11 KC8-AA Programmer's Console (Figure 3-21)
The Programmer's Console has 7-segment LED displays of the Extended Memory Address (EMA), Memory Address (MA), and the Status Register. The console can be located up to 15 ft from the PDP-8/A. Two BC08R cables connect the console to the M8316 module (J1 and J2).
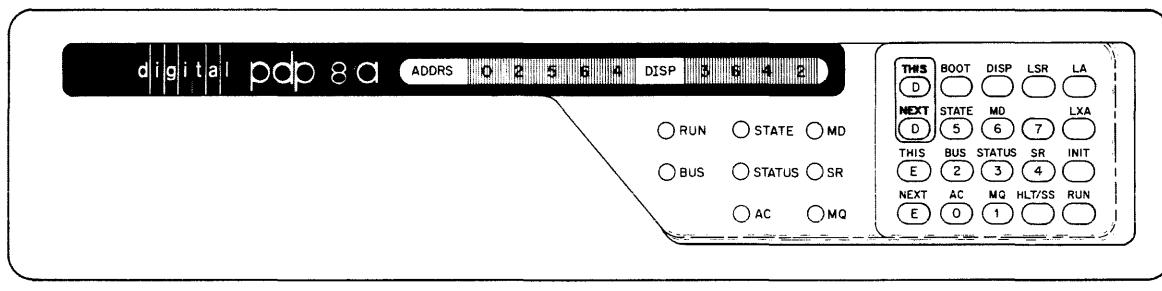
Figure 3-21   KC8-AA Programmer's Console

CHAPTER 4
INSTALLATION AND INITIAL POWER TURN-ON

4.1 ENVIRONMENTAL AND POWER REQUIREMENTS

Recommended operating conditions for the PDP-8/A are an ambient temperature of 5° to 50° C (41° – 122° F) and a noncondensing relative humidity of 10–95 percent. Voltage requirements are 90–132 Vac single phase (using approximately 3.2 A), or 180–264 Vac single phase (using approximately 1.6 A). Line frequency may be 49–51 Hz or 59–61 Hz, depending on the power transformer used in the power supply. Check the label at the rear of the computer to determine the correct voltage and frequency.

WARNING
Ensure that the ac outlet provides a non-current-carrying ground.

4.2 INITIAL POWER TURN-ON

After unpacking the computer, allow at least 30 minutes for the machine to stabilize to ambient temperature before applying power. This time should be increased to 1 hour or longer when the difference between storage or shipping temperature and the operating ambient temperature exceeds 30° F (17° C).

Install the equipment, using the following procedure:

1. Check switch settings on all modules. (See instructions in Chapter 3.)

2. Ensure that the regulator circuit breaker is ON. (The breaker is pictured in Figure 3-4.)

3. Turn OFF the ON/OFF switch on the Limited Function Panel (Figure 3-20).

4. Ensure that all ac power is received from the same branch circuit if the system has more than one power cord.

5. Plug in the power cord. If a power control is used, plug the power cord into the receptacle marked UNSWITCHED AC.

WARNING
Do not touch the computer after plugging it in until grounding has been checked.

6. Before touching the computer, check the frame to ground voltage to ensure that less than 10 Vac is present.

7. Without touching any metal part of the PDP-8/A, turn ON the power ON/OFF switch.

8. Repeat step 6. In case of difficulty, have an electrician check the socket into which the computer has been connected. (Refer to Appendix E for power connection information.) If no difficulty is encountered, the computer frame is properly grounded, and there is no danger in touching it.

9. Power is now applied to the PDP-8/A. The fans should be running, and the BATTERY CHARGING light should light momentarily or stay on. (The light is not used in the H9300 chassis assembly.) If none of the above occur, check the MASTER/SLAVE switch (refer to Paragraph 3.4.8). Turn the power OFF before checking the MASTER/SLAVE switch. This switch should be in the MASTER (to the right) position. Then turn the power ON. If the condition still exists, refer to the basic maintenance section in Chapter 9.

10. Turn the PDP-8/A power switch OFF and the Teletype LINE/OFF/LOCAL switch to the OFF position.

11. Connect the Teletype signal cable to the short cable (DEC Part Number BC05M-1F, plugged into J3 of the M8316) in the PDP-8/A. The cable connectors are keyed for proper mating.

12. Plug the Teletype into the same ac outlet as the PDP-8/A.

13. Turn the power ON/OFF switch on the PDP-8/A to ON.

14. Turn the Teletype LINE/OFF/LOCAL switch to LINE. Only the hum of the Teletype's running motor and the PDP-8/A fans should be heard.

CHAPTER 5
TESTING PDP-8/A WITHOUT PAPER TAPE DIAGNOSTICS

The procedures in this chapter are used to test the PDP-8/A computer from the Programmer's Console. No paper tape diagnostic programs are required for these tests.

5.1 PROGRAMMER'S CONSOLE
The Programmer's Console is shown in Figure 3-21 and is fully described in the *PDP-8/A Miniprocessor Handbook* and the *PDP-8/A User's Manual*. Its use in testing the PDP-8/A is described in detail as needed in the paragraphs below.

5.2 CENTRAL PROCESSOR TEST ROUTINES
When no MAINDEC diagnostics are available, small routines may be keyed into memory and run to check PDP-8/A operation. These tests will not completely check out a PDP-8/A but will locate the most common failures. All routines start at address 0200. If any failures occur, carefully examine each instruction of the routine. If the instructions are correct, switch power OFF and check all of the module switch settings. (All memory contents are lost when power is switched OFF and the routines must be reloaded.) If the routine is not entered properly, reenter the routine and try to run it again.

These routines are also useful when MAINDEC programs cannot be loaded because of a hardware problem.

5.3 ENTERING TEST ROUTINES FROM PROGRAMMER'S CONSOLE
The following procedure should be used to run Routine 1, the first PDP-8/A test.

    1.   Press MD, then DISP. This will let you see what you deposit.

    2.   Press, in order, 0 0 0 0 LXA. Select memory field 0.

    3.   Press, in order, 0 2 0 0 LA. Start loading instructions at address 200.

    4.   Press, in order, 7 0 0 1 D NEXT. Deposit an instruction.

    5.   Press, in order, 2 3 0 0 D NEXT. Deposit an instruction.

    6.   Press, in order, 5 2 0 1 D NEXT. Deposit an instruction.

    7.   Press, in order, 5 2 0 0 D NEXT. Deposit an instruction.

    8.   Press, in order, 0 2 0 0 LA. Now get ready to start at location 200.

    9.   To see the accumulator (AC), press AC, then DISP.

    10.   Press INIT, and RUN. Start the program.

All other routines should be entered into memory using this procedure.

5.4 CENTRAL PROCESSOR TEST ROUTINES
The following routines should be used to check the CPU:

Routine 1 – This program will increment the AC slowly so that the user can see that it is working. The internal numbering system of the PDP-8/A does not use 8 and 9.

0200	7001	/Increment the AC by 1; start here.
0201	2300	/Increment a location and skip if it is zero.
0202	5201	/Jump back 1.
0203	5200	/Start program over again.

Routine 2 – This routine should print a pattern of all printable characters. Omit this routine if your PDP-8/A is not equipped with a Teletype or similar terminal.

NOTE
**Ensure that the Teletype is set to LINE for routines 2
and 3.**

The following line will print out while this routine is running. Characters may or may not be printed after the letter Z, depending on the column width of the terminal. These extra characters should be disregarded. Disregard the first line printed.

!"#%$,()*+,-./0123456789:;≅==≡?@ABCDEFGHIJKLMNOPQRSTUVWYZ (Random Characters)

0200	7001	/Increment the AC by 1; start here.
0201	6046	/Transmit.
0202	6041	/Am I done transitting?
0203	5202	/No I am not done transmitting.
0204	5200	/Yes I am done. Jump back and start over.

Routine 3 – This routine will print what is typed on the terminal (echo characters). Type several sentences, ensuring that the terminal prints out what you type. Omit this step if your PDP-8/A is not equipped with a terminal.

0200	6031	/Has a key been pressed?
0201	5200	/No, go back and wait.
0202	6036	/A key was hit. Read it.
0203	6046	/Transmit the character to the printer.
0204	6041	/Am I done printing?
0205	5204	/No. Go back one.
0206	5200	/Yes I am done. Let's go back to wait for another key.

Routine 4 – The following program checks some of the Operate instructions. The program should halt at location 00216 (ADDRS should read 00217) with the AC cleared (AC = 0000)

0200	7240	/Clear the AC, then complement the AC.
0201	7001	/Increment the AC by 1.
0202	7640	/Skip if AC = 0, then clear the AC.
0203	7402	/Error halt. Computer should not halt here.
0204	7120	/Set the link to 1.
0205	7010	/Rotate the AC right 1. The AC should then equal 4000.
0206	7510	/Skip if AC bit 0 = 0.
0207	7410	/Skip unconditionally.
0210	7402	/Halt. Computer should not halt here.
0211	7001	/Increment the AC by 1.
0212	7002	/Byte swap. AC should equal 0140.
0213	1202	/Add 7640 to 0140.
0214	7420	/Skip if link equals 1.
0215	7402	/Halt on error.
0216	7402	/Good. Halt if AC = 0000.

Routine 5 – The following routine tests the ISZ instruction. The program should halt at location 00207 (ADDRS should read 00210) with the AC cleared (AC = 0000). To read the AC, depress AC and then DISP.

0200	7300	/Clear the AC and link.
0201	3300	/Store 0 in location 300.
0202	7001	/Index the AC.
0203	2300	/Index location 300.
0204	5202	/Jump back and do again.
0205	7440	/Done. Check if AC = 0000.
0206	7402	/Error (AC and location 300 should be zero).
0207	7402	/Good. Halt.

Routine 6 – This routine tests the JMS instructions. It should halt with ADDRS = 00215, with the AC cleared (AC = 0000). To read the AC, press AC, then DISP.

0200	7300	/Clear the AC and link.
0201	3300	/Zero pass counter.
0202	3204	/Zero entry.
0203	4204	/JMS to subroutine.
0204	0000	/Return address written here.
0205	1204	/Get return address.
0206	7041	/Complement and index the AC.
0207	1215	/Add to known good return address.
0210	7440	/Skip on 0 AC.
0211	7402	/Error halt.
0212	2300	/Increment pass counter.
0213	5202	/Do again.
0214	7402	/Good. Halt.
0215	0204	/Constant.

Routine 7 – This routine tests the Jump instructions. The program should halt at location 00214. (ADDRS should read 00215.) Run this test twice.

0200	5210	/Jump 210.
0201	7402	/Error halt.
0202	5206	/Jump 206.
0203	7402	/Error halt.
0204	5212	/Jump 212.
0205	7402	/Error halt.
0206	5204	/Jump 204.
0207	7402	/Error halt.
0210	5202	/Jump 202.
0211	7402	/Error halt.
0212	2300	/Loop to do this program 4096 times.
0213	5200	/Start program over again.
0214	7402	/Good. Halt after 4096 passes.

CHAPTER 6
LOADING THE RIM AND BINARY LOADERS

Programs in binary format may be used in machines with 4K or more of read/write memory. The RIM loader must be used to load the binary loader. The binary loader is then used to load a program in binary format.

The RIM and binary loaders reside in the highest 1K of a 4K memory. Machines with less than 4K of memory require the RIM loader to be loaded at addresses in the lowest 1K of memory. Use of the binary loader on machines with less than 4K of read/write memory is not recommended because of the length of the binary loader routine. Each test procedure will tell you where to load the RIM loader.

6.1 LOADING RIM LOADER

The RIM loader is a 17-instruction program needed to load the binary loader and other RIM formatted tapes. There are two methods of loading the RIM loader. The first method consists of manually loading each instruction through the Programmer's Console keys as described in the next few paragraphs. The second method consists of using the bootstrap option, if there is 4K or more of read/write memory and the KM8-A Extended Option Board (M8317) is in the computer. If using the second method, go directly to Paragraph 6.3.

Enter the RIM loader through the Programmer's Console keys as follows.

Press keys, in order, from left to right as they appear in the following steps.

1.	MD	DISP	/Enables memory data to the readout dislay.
2.	0000	LXA	/Sets instruction and data field to 0.
3.	XXXX	LA	/ADDRS should read the 0XXXX value. (See Note.)
4.	6032	D NEXT	/DISP should read 6032.
5.	6031	D NEXT	/DISP should read 6031.
6.	5357	D NEXT	/DISP should read 5357.
7.	6036	D NEXT	/DISP should read 6036.
8.	7106	D NEXT	/DISP should read 7106.
9.	7006	D NEXT	/DISP should read 7006.
10.	7510	D NEXT	/DISP should read 7510.
11.	5357	D NEXT	/DISP should read 5357.
12.	7006	D NEXT	/DISP should read 7006.
13.	6031	D NEXT	/DISP should read 6031.
14.	5367	D NEXT	/DISP should read 5367.
15.	6034	D NEXT	/DISP should read 6034.
16.	7420	D NEXT	/DISP should read 7420.
17.	3776	D NEXT	/DISP should read 3776.
18.	3376	D NEXT	/DISP should read 3376.
19.	5356	D NEXT	/DISP should read 5356.

20.	0000	D NEXT	/DISP should read 0000.
21.	0000	D NEXT	/DISP should read 0000.
22.	XXXX	LA	/ADDRS should be 0XXXX.

NOTE

If you have a 4K RAM, enter 7756. If you have less than 4K of RAM, enter 0156 for loading all tests except version A of the MS8-A test. (Enter 1756 for this case only.)

6.2 CHECKING THE RIM LOADER

After completing the RIM loader procedure, the program may be checked by repeating the first three steps and pressing E NEXT. Each time E NEXT is pressed, the next four digits of the program should appear in the DISP lights. When you are sure the RIM loader is in memory correctly, proceed to the binary loader procedure or load and run RIM Format MAINDECs (Chapter 7) if you have less than 4K of read/write memory in your system.

6.3 LOADING THE BINARY LOADER

NOTE

Do not use the binary loader procedure if the memory size is less than 4K.

1. Place the tape labeled Binary Loader (DEC-08-LBAA-PM) in the Teletype reader, with the START/STOP/FREE lever set to FREE. Position the tape so that the printed arrow on the tape points toward you, and the single row of data holes at the beginning of the tape is over the read head (Figure 6-1).

LEADER : SINGLE ROW OF DATA HOLES (HOLE "8")   PROGRAM DATA

08-0843
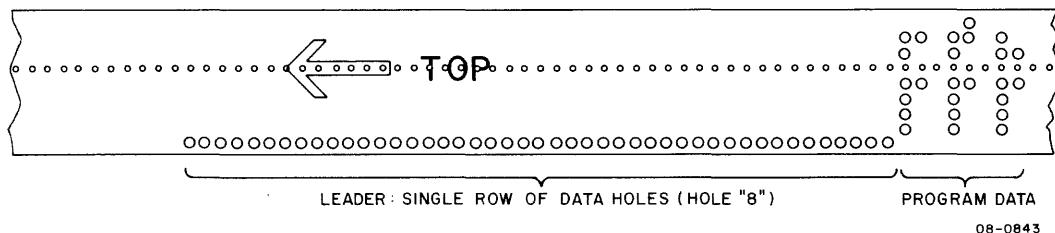
Figure 6-1 Paper Tape Leader

2. Ensure that the LINE/OFF/LOCAL switch of the Teletype is set to LINE, and the paper tape reader START/STOP/FREE lever is set to START. See Figure 6-2.

3. If the KM8-AA Extended Option Board (M8317) is not available, the RIM loader must be loaded at this time using the RIM loading procedure (Paragraph 6.1).

4. If the RIM loader was keyed in manually through the keys, press, in order, 7756, LA, INIT, and RUN. The RUN light should be on and the Teletype reader should be reading tape.

5. If the KM8-AA Extended Option Board (M8317) was set up for Hi-Lo RIM, ensure that the BOOT switch on the Limited Function Panel is down, and then press the BOOT key on the Programmer's Console twice. The RUN light should go on and the Teletype reader should read tape.

PAPER ROLL UNWINDS
COUNTER-CLOCKWISE

TAPE
UNWINDS
CLOCKWISE

TAPE
HOPPER

PUNCH
MECHANISM

PUNCH
OFF/ON

PAPER TAPE
READER
MECHANISM

ART/STOP/FREE

LINE/OFF/LOCAL

2428
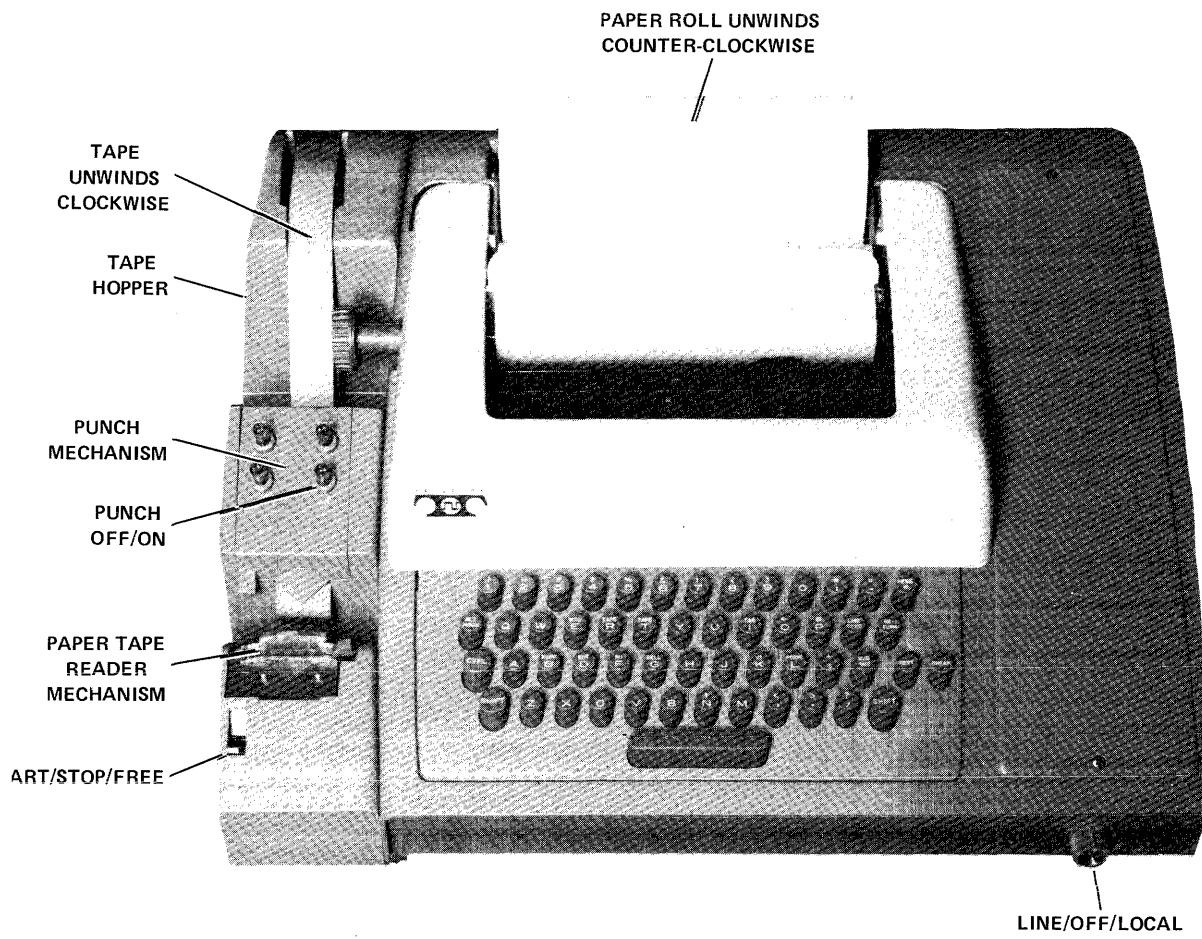
Figure 6-2 LT33 Teletype Controls

6. If the tape fails to read in or stops before the end of tape, reload the RIM loader using the RIM loader procedure (Paragraph 6.1).

7. After the tape is read to the trailing single row of data holes, press the HLT/SS key. The reader should stop reading tape. The binary loader should now be in memory.

6.4 LOADING BINARY FORMATTED PAPER TAPES

1. Press, in order, 7777, LA, MD, DISP, and E THIS. The DISP register should read 5301; if not, check the RIM loader and reload the binary loader.

2. If the content of address 07777 was 5301, press 7777, LA, and LSR.

3. Place the binary-formatted paper tape in .the reader, with the single row of data holes over the read head.

4. Place the Teletype LINE/OFF/LOCAL switch to LINE.

6-3

5. Place the reader switch in the START position.

6. Press INIT, then RUN. The reader should start reading tape.

7. The Programmer's Console RUN light should go out when the first bit of trailer (row of single data holes at the end of tape) is over the read head. The reader should automatically stop. Move the reader lever to STOP or FREE.

8. Press AC, then DISP. The DISP register should read 0000. If the DISP register does not equal 0000, the tape must be reloaded.

9. Now the program is ready to run.

MAINDECs are test programs designed to test the KK8-A or KK8-E CPU, the DKC8-AA I/O Option Board, the KM8-AA Extended Option Board, and read/write memory. The minimum PDP-8/A system that can be tested with MAINDEC programs consists of a box, an Omnibus, a power supply, at least 1K of read/write memory starting in location 0000 of field 0, and the following options:

Option	Description
KK8-E or KK8-A	CPU
DKC8-AA	I/O Option Board
KC8-AA	Programmer's Console
LT33-D	ASR33 Teletype

The PDP-8/A read/write memory can be any of the following:

Memory	Size and Type
MS8-AA	1K Semiconductor
MS8-AB	2K Semiconductor
MS8-AD	4K Semiconductor
MM8-AA	8K Core
MM8-AB	16K Core

If your machine has a MR8 Read-Only Memory, you should consult your local Field Service representative before attempting to run diagnostics.

7.1 CENTRAL PROCESSOR UNIT (CPU) TEST

The CPU test is a good overall test of the PDP-8/A. This test should be the only one run unless specific problems are encountered.

The CPU test checks the CPU for proper operation. The program first stops at step 7 to check the HALT instruction; it then tests the remaining instructions.

Two variations of the CPU test exist. One variation applies if the PDP-8/A has 4K or more of read/write memory; the other applies if it has less than 4K. In the steps below, the steps which are memory-size-dependent are enclosed in boxes. You should enter the information or do the operation indicated for your memory configuration. (Refer to the sticker on the back of the PDP-8/A.)

1. Load the RIM loader (Paragraph 6.1), starting with one of the following addresses:

> ≥4K: 7756   <4K: 0156

7-1

2. For systems with 4K or more of memory, load the binary loader (Paragraph 6.3).

   For systems with less than 4K of memory, proceed to step 3.

3. Place the PDP-8/A CPU test in the paper tape reader. Ensure that the header/trailer code (hole 8) is over the read head. The tape number is:

≥4K:	<4K:
MAINDEC-8-DJKKA-PB	MAINDEC-08-DJKKA-PM1

4. Run the appropriate loader:

≥4K:	<4K:
Press 0000 and LXA.	Press 0156 and LA.
Press 7777 and LSH.	
Press 7777 and LA.	

   Press INIT, then press RUN. Tape will read into memory.

≥4K:	<4K:
Tape will stop automatically.	Tape must be stopped when trailer is reached.
Press AC, then DISP.	Press HLT/SS.
DISP indicators should equal 0000.	

5. Set up location 0021 in the program as follows:

   a. Press 0021, then LA.

   b. Press 4000, then D THIS.

   c. Depress 0021 then LA. Depress 4000 then D THIS.

6. Start program as follows:

   a. Press 0000, then LSR.

   b. Press 0200, then LA.

   c. Press INIT.

   d. Press RUN.

7. Program will stop (RUN light will go off) with ADDRS = 00222.

   a. Press STATUS, then DISP. DISP indicators sould equal 4000.

   b. Depress AC, then DISP. DISP indicators should equal 7777.

8. Depress RUN. Allow the program to run for 10 minutes. If no errors are detected, the program will not halt.

9. While the program is still running, depress any key on the Teletype. Program should halt.

CHAPTER 8
ADDITIONAL DIAGNOSTIC TESTS

These programs should be run to isolate specific problems. They should not be run as a periodic confidence check.

8.1 MEMORY TEST

The MS8-A MOS Memory Test checks all locations in Memory Field 0 for proper operation. It relocates itself in memory and tests all of memory not occupied by the program. This test assumes that the CPU is functioning correctly.

1.   Load RIM loader (Paragraph 6.1), starting with address:

≥4K: 7756	<4K: 0156*

2.   Place tape labeled "1-4K MS8-A MOS Memory Test" (MAINDEC-08-DJMSA-A-PM) in the paper tape reader.

3.   Run RIM loader using one of the following:

≥4K:	<4K:
Press 0000, then LXA.	Press 0156,* then LA.
Press 7756, then LA.	

   a.   Press INIT, then RUN. Tape will read into memory.

   b.   Tape must be stopped when trailer is reached (Press HLT/SS.)

4.   Set up location 0021:

   a.   Press 0021 and LA.

   b.   Press 4000 and D THIS.

5.   Set up location 0023:

   a.   Press 0023 and LA.

   b.   Do one of the following:

If 4K: Press 7777 and D THIS.
If 2K: Press 3777 and D THIS.
If 1K: Press 1777 and D THIS.

---

*Use 1756 if the tape is Rev A (MAINDEC-08-DJMSA-A-PM). The revision letter is the single letter just before the final PM.

6. Start program as follows:

   a. Press 0000, then LSR.

   b. Press 0200, then LA.

   c. Press INIT, then RUN.

7. Allow program to run for 5 minutes. There should be no halts. At the end of 5 minutes, while program is still running:

   a. Press 0400, then LSR.

   b. Program will halt.

8.2 DKC8-AA TEST

The DKC8-AA I/O Option test program tests for proper operation of the serial I/O, parallel I/O, and real-time clock contained on the M8316 module. In addition to the paper tape(s), the following equipment is needed:

W987 Quad Module Extender

Three Termi-Point Jumpers (Available in a package of 100, type 915. Any length may be used, although 8 in. is probably most useful.)

BC08R cable (any stock length)

These items are supplied with the PDP-8/A maintenance kit, and may also be ordered separately using the numbers above. This test requires placing the DKC8-AA on a module extender; hence a table to support the Programmer's Console or cables to extend the panel cables should be available.

1. Turn PDP-8/A power OFF. Without altering the M8316 switch settings, remove the M8316 from the PDP-8/A. Be sure to provide enough slack in the Teletype cable and the parallel I/O cables to allow easy removal of the module. Plug the W987 Quad Extender into the slot previously occupied by the M8316, and plug the M8316 into the extender. Remove the parallel I/O cables (if used) from J4 and J5; be sure to mark the cables so they can be properly reinstalled at the end of this test. Plug one end of the BC08R cable into J4. Plug the other end of the BC08R cable into J5. There should be one fold and no twists in the cable. Do not remove the Teletype cable or the cables to the Programmer's Console. Turn PDP-8/A power ON.

2. Using the same procedure as for steps 1 – 4 of the CPU test (Paragraph 7.1), load the tape into memory.

<div align="center">

CAUTION
Do not use the loading procedure for the
memory test.

</div>

The tape to be loaded is:

≥4K:	<4K:
MAINDEC-08-DJDKA-PB1	MAINDEC-DJDKA-PM1

3. Without turning power off, remove the Teletype cable from J3 and install three Termi-Point jumpers as follows:

> J3-E to J3-H
> J3-K to J3-KK
> J3-S to J3-AA

Change S1-5 on the M8316 from OFF to ON. Make no other switch changes at this time.

4. Set up location 0021 as follows:

> Press 0021, then LA.

Deposit one of the following numbers by entering it via the numeric keys; then press D THIS:

> If 1K: Enter 6000.
> If 2K: Enter 6001.
> If 4K: Enter 6003.
> If 8K: Enter 6007.
> If 16K: Enter 6017.

5. Start program as follows:

a. Press 0000, LSR, and LXA.

b. Press 0200, INIT, and RUN.

6. Allow program to run for 5 minutes. There should be no halts while program is still running.

> Press 0400, then LSR.

Program will halt.

Then:

> | ≥4K: | <4K: |
> | Proceed to Step 9. | Proceed to Step 7. |

7. Omit this step if ≥4K.

Return S1-5 to OFF. Remove the Termi-Point jumpers from J3 and reinstall the Teletype cable. (Be sure it is installed so the printed "A" on the cable connector is at the same end as the printed "A" on J3.)

Load:

> MAINDEC-08-DJDKA-PM2

and then repeat steps 3, 4, and 5 of this test. Allow program to run for 5 minutes (no halts). Then:

> Press 0400 and LSR.

Program will halt.

8. Omit if $\geqslant$4K.

Return S1-5 to OFF. Remove the Termi-Point jumpers from J3 and reinstall the Teletype cable as described in step 7.

Load:

MAINDEC-08-DJDKA-PM3

and then repeat steps 3, 4, and 5. Allow program to run for 5 minutes (no halts). Then:

Press 0400 and LSR.

Program will halt.

9. Perform this step regardless of memory size.

For a C etch revision: Set S1-3 and S1-7 ON; leave S1-5 ON. For a D etch revision: Set S1-1, 2, 4, 5, and 7 ON; set S1-3 OFF. Continue, for either revision.

Remove the Termi-Point jumpers from J3; now connect:

J3-F to J3-J
J3-E to J3-M

Start program, as described in step 5, and allow program to run for 5 minutes (no halts). Then:

Press 0400 and LSR.

Program will halt.

Then do one of the following:

$\geqslant$4K:	<4K:
Proceed to Step 11.	Perform Step 10.

10. Skip this step if $\geqslant$4K.

For a C etch revision: Set S1-3, S1-5, and S1-7 OFF. For a D etch revision: Set S1-1, 3, and 4 ON; set S1-2 and 7 OFF. Continue, for either revision.

Remove Termi-Point jumpers from J3. Replace Teletype cable as described in Step 7.

Load:

MAINDEC-08-DJDKA-PM4

and repeat steps 3, 4, and 5. Allow program to run for 5 minutes. Then:

Press 0400 and LSR.

Program will halt.

11. Perform this step regardless of memory size.

Press 0000, then LSR.

Then do one of the following:

≥4K:	<4K:
Depress 400, then LA.	Press 1200, then LA.

Press INIT, then RUN.

The program should run for 30 seconds ± 0.5 second from the time the RUN button is pressed, and then halt.

Now:

≥4K:	<4K:
Press 4023, then LA.	Press 1223, then LA.

Press INIT, then RUN.

Program will halt.

For a C etch revision: Set S1-3 and S1-7 ON; set S1-8 OFF. For a D etch revision: Set S1-1, 2, 4, and 7 ON; set S1-3 and 8 OFF. Continue, for either revision.

Press 0001 and LSR.

Press RUN.

WARNING
Do not depress INIT.

The program should run for 30 seconds ± 0.5 seconds and then halt.

12. Perform this step regardless of memory size.

Turn PDP-8/A power OFF. For a C etch revision: Set S1-3, 5, and 7 OFF; set S1-8 ON. For a D etch revision: Set S1-1, 3, 4, 8, and 9 ON; set S1-2, 5, and 7 OFF. Continue, for either revision.

Remove all Termi-Point jumpers. Replace Teletype cable on J3, ensuring that the pin letters on the cable and board connector match. Remove the BC08R cable from J4 and J5. Reinstall parallel I/O cables (if used). Remove the W987 Quad Extender from the PDP-8/A, and reinstall the M8316. Be careful not to alter switch settings accidently while inserting the M8316.

8.3 KM8-A EXTENDED OPTION BOARD TEST

NOTE
Make sure you have the correct diagnostic program.
MAINDEC-08-DJKMA-A is for M8317 modules having
ROMs E82 and E87 labeled 87A2 and 88A2; MAIN-
DEC-08-DJKMA-B is for ROMs labeled 158A2 and
159A2.

The KM8-A Extended Option Board test program tests the circuitry contained on the M8317 module. As in the previous test, the module under test is placed on a W987 Quad Module Extender to allow the operator to alter switch settings without turning off power to the PDP-8/A. Again, it is advisable to have a table to support the Programmer's Console.

The series of tests below is designed for operation on a PDP-8/A with 4K or more of memory, since two of the three options on this module require at least 4K of memory. Also available for this option are test programs which will run in 1K of memory. Consult your local DIGITAL Sales Office if more information on the 1K programs is needed.

1. Turn OFF power to the PDP-8/A, and place the M8317 on the W987 Quad Extender. The M8317 must be plugged into slot 2 or 3 of the Omnibus.

2. Write on paper the position of all switches on the M8317, and then place all these switches in the OFF position. Unplug the controllers for any options that can be bootstrapped (such as the PC8-E, TA8-E, RK8-E controllers and the KA8-E positive I/O adapter), but leave the Teletype connected.

3. Turn power ON, and load RIM at address 7756 using the keys. Do not attempt to use the bootstrap; it was disabled at Step 2. Load the binary loader (Paragraphs 6.1 and 6.3).

4. Read in the tape (MAINDEC-08-DJKMA-PB1), using the binary loader (Paragraph 6.4).

5. Set up location 0021 by pressing 0021, then LA.

    Deposit one of the following numbers (depending on memory size) by entering it via the numeric keys and then pressing D THIS.

For 4K: Enter 7003.
For 8K: Enter 7007.
For 12K: Enter 7013.
For 16K: Enter 7017.
For 32K: Enter 7037.

    Start program:

    Press 0000, LXA, then LSR.
    Press 0200, INIT, then RUN.

6. Allow program to run for 10 minutes. Then:

    Press 0400 and LSR.

    Program will halt.

7. Turn S2-1 ON. Then:

      Press 4255 and LA.
      Press 0000, LSR, INIT, and then RUN.

Program will halt.

8. Set up for Bootstrap test:

      Press 4465, LA, INIT, then RUN.

Program will halt.

9. Test the paper tape bootstrap as follows:

Turn S2-5, S2-6, S2-7, S1-1, S1-2, S1-3, S1-6, S1-7, and S1-8 ON. Make sure that the Teletype reader lever is in either the STOP or FREE position.

Press:

      BOOT
      BOOT
      HLT/SS
      0000, then LSR
      4401, LA, INIT, and then RUN

Program will halt with ADDRS = 04462 if paper tape bootstrap is correct.

NOTE
There is no point in checking a bootstrap unless your PDP-8/A is equipped with the option (e.g., unless your PDP-8/A is equipped with an RK8-E, do not try to test the RK8-E bootstrap).

10. Check any other bootstraps as follows:

a. Repeat step 8.

b. Set switches according to Table 8-1 or 8-2, depending on the bootstrap you are testing.

NOTE
For those M8317 modules that have ROMs labeled 87A2 and 88A2, use Table 8-1 for bootstrap select switch settings. (See Figure 3-16 for switch and ROM locations.) For those modules that have ROMs labeled 158A2 and 159A2, use Table 8-2 for switch settings.

Leave S1-6, S1-7 and S1-8 ON.

c. Depress:

      BOOT
      BOOT
      HLT/SS

Table 8-1
Bootstrap Switch Settings
for ROMs Labeled 87A2 and 88A2 (E82 and E87)

Bootstrap	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	SR
Hi-Lo RIM	ON	ON	ON	OFF	ON	ON	ON	0000
RK8-E	ON	OFF	ON	OFF	ON	OFF	ON	0004
TC08	ON	OFF	OFF	ON	OFF	ON	ON	0001
RF08/DF32D	OFF	ON	ON	ON	ON	OFF	OFF	0002
TA8-E	OFF	ON	ON	OFF	ON	OFF	OFF	0003

Table 8-2
Bootstrap Switch Settings for ROMs (E82 and E87)
Labeled 158A2 and 159A2

Bootstrap	S2-5	S2-6	S2-7	S2-8	S1-1	S1-2	S1-3	SR
Hi-Lo RIM	ON	ON	ON	OFF	ON	ON	ON	0000
RK8-E	ON	OFF	ON	OFF	ON	OFF	ON	0004
RX8-E	ON	OFF	OFF	ON	OFF	ON	ON	0003
RF08/DF32D	OFF	ON	OFF	ON	OFF	ON	OFF	0001
TA8-E	OFF	ON	OFF	OFF	OFF	ON	OFF	0002

d. Enter the value of SR from Table 8-1 or Table 8-2, then press, in order:

LSR, 4400, LA, INIT, then RUN.

e. Program will halt with ADDRS = 04462 if bootstrap is correct.

11. Make sure the BATTERY CHARGING light on the Limited Function Panel is off. If this light is on, leave PDP-8/A power on but do not attempt the following test until the BATTERY CHARGING light is off.

NOTE
Unless you have experienced a recent power failure while the PDP-8/A was running or have unplugged the PDP-8/A power cord without first turning the ON/OFF switch to OFF, it is very unlikely that the BATTERY CHARGING light will be on by the time you get to this test.

12. Turn ON S1-1, 3, 6, 7, and 8; S2-3, 5, and 7. Turn OFF S1-2, 4, and 5; S2-1, 2, 4, 6, and 8.

13. Enter the following:

Press 4600 then LA. Press 0000, LSR, INIT, and RUN.

PDP-8/A will halt.

14. Depress 0002, LSR, INIT, and RUN.

15. Without operating the panel ON/OFF switch, unplug the power cord of the PDP-8/A from the wall receptacle. ADDRS should display 04764, and the RUN lights on the Limited Function Panel and the Programmer's Console should be off.

    Reinsert the power cord. The program should begin running again. Do not leave power cord unplugged any longer than necessary, since the batteries will discharge.

16. Repeat Step 15 four times.

17. Turn OFF power. Return the M8317 switches to the original positions, written down at Step 2. Remove the W987 Quad Extender, and replace the M8317 in the PDP-8/A box. Be careful not to disturb the switch settings on this module or any adjacent modules. Replace the Programmer's Console.

8.4 TESTING EXTENDED MEMORIES
A good test of extended memories, the CPU, and the memory extension control may be made by running the 1K to 32K Random Memory Reference Instruction Exerciser test. This test may also be used in systems with as little as 1K of memory.

1. Load the RIM loader, as described in Paragraph 6.1, starting with one of the following addresses:

≥4K: 7756	<4K: 0156

2. Place MAINDEC-08-DJEXA-PM in paper tape reader, enter same address as given for Step 1, and press:

   LA
   0000, then LXA
   INIT, then RUN

   Press HLT/SS when trailer is over read station.

3. Set up location 0021 by pressing 0021 and LA.

   Enter one of the following numbers (depending on memory size); then depress D THIS.

For 1K: Enter 4000.
For 2K: Enter 4001.
For 4K: Enter 4003.
For 8K: Enter 4007.
For 12K: Enter 4013.
For 16K: Enter 4017.
For 32K: Enter 4037.

4. Enter the following:

   Press 0000, then LSR.
   Press 0200, INIT, and RUN.

5. Run 2 minutes for each 1K of memory (4K: 8 minutes, 8K: 16 minutes, etc.).

CHAPTER 9
BASIC PDP-8/A MAINTENANCE

Table 9-1 lists some basic PDP-8/A problem symptoms and their possible causes.
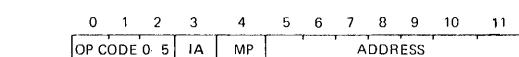
Table 9-1
Basic PDP-8/A Troubleshooting

Symptom	Possible Problem
No lights Fans not running	Fuse Blown Power Switch is OFF AC power not connected MASTER/SLAVE switch in wrong position
Fans running, but no lights	Circuit breaker on the regulator assembly is OFF.
RUN light does not come on after BOOT switch is activated	Check switches on KM8-A Extended Option Board (M8317). Switch settings are in Chapter 3, Tables 3-10 through 3-14.
BATTERY CHARGING light stays on	The battery requires a minimum of 15 hours of charging after a complete discharge. The light normally flashes on momentarily after power on if battery has been fully charged.
RUN light comes on when power switch is turned on	This function is switch selectable on KK8-A CPU Module (M8315) and KM8-A Extended Option Module (M8317).
RUN light stays on after AC power is unplugged	Do not unplug AC power unless PDP-8/A power is shut off. The PDP-8/A behaves as if there has been a power failure, and the battery supply takes over.
Peripheral will not BOOT with BOOT switch	BOOT switch on Limited Function Panel in wrong position, it should be down. PANEL LOCK should be down. Check switches on the Extended Option Board (M8317). Check switches on DKC8-A I/O Option Board (M8316). Switch settings are in Chapter 3.
Machine remains powered even with ON/OFF switch set to OFF.	Fuse in power control relay circuit is blown. Set ON/OFF switch to OFF, then unplug the power cord before attempting to change this fuse.
Light on the G8018 Regulator Board is out (8A computers)	Turn off power, remove regulator board, check +5 V circuit breaker and –5 V, ±15 V, and 20 V fuses.

APPENDIX A
INSTRUCTION SUMMARY

BASIC INSTRUCTIONS

			Cycles
AND	0000	logical AND	2
TAD	1000	2's complement add	2
ISZ	2000	increment, and skip if zero	2
DCA	3000	deposit and clear AC	2
JMS	4000	jump to subroutine	2
JMP	5000	jump	1
IOT	6000	in/out transfer	
OPR	7000	operate	1

```
 0   1   2   3   4   5   6   7   8   9  10  11
┌───────────┬──┬──┬─────────────────────┐
│OP CODE 0-5│IA│MP│      ADDRESS        │
└───────────┴──┴──┴─────────────────────┘
```
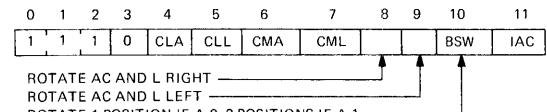
INDIRECT ADDRESSING
0 = DIRECT
1 = INDIRECT (ADD: 1 CYCLE)
MEMORY PAGE
0 = PAGE 0
1 = CURRENT PAGE

Memory Reference Instruction Bit Assignments

GROUP 2 OPERATE MICROINSTRUCTIONS (1 CYCLE)

			Sequence
SMA	7500	skip on minus AC	1
SZA	7440	skip on zero AC	1
SPA	7510	skip on plus AC	1
SNA	7450	skip on on-zero AC	1
SNL	7420	skip on non-zero link	1
SZL	7430	skip on zero link	1
SKP	7410	skip unconditionally	1
OSR	7404	inclusive OR switch register with AC	3
HLT	7402	halts the program	3
CLA	7600	clear AC	2

```
 0   1   2   3    4     5     6     7   8   9   10   11
┌───┬───┬───┬───┬─────┬─────┬─────┬───┬───┬─────┬───┐
│ 1 │ 1 │ 1 │ 1 │ CLA │ SMA │ SZA │SNL│   │ OSR │HLT│ 0 │
└───┴───┴───┴───┴─────┴─────┴─────┴───┴───┴─────┴───┘
```

REVERSE SKIP SENSING OF BITS 5, 6, 7

Logical Sequences:
1 (Bit 8 is Zero) - Either SMA or SZA or SNL
1 (Bit 8 is One) - Both SPA and SNA and SZL
2 - CLA
3 - OSR, HLT
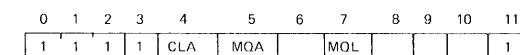
Group 2 Operate Instruction Bit Assignments

MQ MICROINSTRUCTIONS (1 CYCLE)

|		
NOP	7401	no operation
CLA	7601	clear AC
MQL	7421	load MQ from AC then clear AC
MQA	7501	inclusive OR the MQ with the AC
CAM	7621	clear AC and MQ
SWP	7521	swap AC and MQ
ACL	7701	load MQ into AC
CLA SWP	7721	load AC from MQ then clear MQ

```
 0   1   2   3    4     5    6     7    8   9  10  11
┌───┬───┬───┬───┬─────┬────┬─────┬────┬──┬──┬──┬──┐
│ 1 │ 1 │ 1 │ 1 │ CLA │MQA │     │ MQL│  │  │  │ 1 │
└───┴───┴───┴───┴─────┴────┴─────┴────┴──┴──┴──┴──┘
```
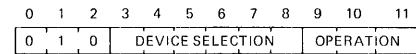
Logical Sequence:
1 - CLA
2 - MQA, MQL
3 - ALL OTHERS

MQ Microinstruction Bit Assignments

GROUP 1 OPERATE MICROINSTRUCTIONS (1 CYCLE)

			Sequence
NOP	7000	no operation	
CLA	7200	clear AC	1
CLL	7100	clear link	1
CMA	7040	complement AC	2
CML	7020	complement link	2
RAR	7010	rotate AC and link right one	4
RAL	7004	rotate AC and link left one	4
RTR	7012	rotate AC and link right two	4
RTL	7006	rotate AC and link left two	4
IAC	7001	increment AC	3
BSW	7002	swap bytes in AC	4

```
 0   1   2   3    4     5     6     7    8   9   10   11
┌───┬───┬───┬───┬─────┬─────┬─────┬───┬───┬─────┬───┐
│ 1 │ 1 │ 1 │ 0 │ CLA │ CLL │ CMA │CML│   │ BSW │IAC│
└───┴───┴───┴───┴─────┴─────┴─────┴───┴───┴─────┴───┘
```

ROTATE AC AND L RIGHT
ROTATE AC AND L LEFT
ROTATE 1 POSITION IF A 0, 2 POSITIONS IF A 1

Logical Sequences
1 - CLA CLL
2 - CMA CML
3 - IAC
4 - RAR, RAL, RTR, RTL, BSW

Group 1 Operate Instruction Bit Assignments

COMBINED OPERATE MICROINSTRUCTIONS (1 CYCLE)

CIA		7041	complement and increment AC
LAS		7604	load AC with switch register
STL		7120	set link (to 1)
GLK		7204	get link (put link in AC bit 11)
CLA	CLL	7300	clear AC and link
CLL	RAR	7110	shift positive number one right
CLL	RAL	7104	shift positive number one left
CLL	RTL	7106	clear link, rotate 2 left
CLL	RTR	7112	clear link, rotate 2 right
SZA	CLA	7640	skip if AC=0, then clear AC
SZA	SNL	7460	skip if AC=0 or link is 1, or both
SNA	CLA	7650	skip if AC≠0, then clear AC
SMA	CLA	7700	skip if AC<0, then clear AC
SMA	SZA	7540	skip if AC≤0
SMA	SNL	7520	skip if AC<0 or link is 1, or both
SPA	SNA	7550	skip if AC>0
SPA	SZL	7530	skip if AC≥0 and the link is 0
SPA	CLA	7710	skip if AC≥0, then clear AC
SNA	SZL	7470	skip if AC≠0 and link=0

INTERNAL IOT MICROINSTRUCTIONS
PROGRAM INTERRUPT AND FLAG (1 CYCLE)

SKON	6000	skip if interrupt ON, and turn OFF
ION	6001	turn interrupt ON
IOF	6002	turn interrupt OFF
SRQ	6003	skip on interrupt request
GTF	6004	get interrupt flags
RTF	6005	restore interrupt flags
CAF	6007	clear all flags

```
 0   1   2   3   4   5   6   7   8   9  10  11
┌───┬───┬───┬─────────────────┬─────────────┐
│ 0 │ 1 │ 0 │ DEVICE SELECTION│  OPERATION   │
└───┴───┴───┴─────────────────┴─────────────┘
```

IOT Instruction Bit Assignments

DKC8-AA I/O OPTION BOARD INSTRUCTIONS
SERIAL LINE UNIT IOT INSTRUCTIONS (1 Cycle)

Receive

KCF	6030	Clear Receive flag, do not set Reader Run.
KSF	6031	Skip if Receive flag is set.
KCC	6032	Clear Receive flag and AC, set Reader Run.
KRS	6034	Read Receive Buffer.
KIE	6035	Load AC11 into Interrupt Enable.
		AC11 = 1. Set interrupt Enable.
		AC11 = 0. Clear Interrupt Enable.
KRB	6036	Combined KCC & KRS.

Transmit

TFL	6040	Set Transmit Flag.
TSF	6041	Skip if Transmit flag is set.
TCF	6042	Clear Transmit flag.
TPC	6044	Load AC4-AC11 into transmit buffer and transmit.
SPI	6045	Skip if transmit or receive flag is set and if interrupt enable is set.
TLS	6046	Combined TCF and TPC commands.

GENERAL PURPOSE PARALLEL I/O INSTRUCTION (1 Cycle)

DBST	6570	Skip on Data Accepted, clear Data Accepted and Data Available.
DBSK	6571	Skip on Data Ready flag.
DBRD	7572	Read Data In to AC0—AC11.
DBCF	6573	Clear Data Ready flag, issue Data Accepted Out pulse.
DBTD	6574	Load AC0—AC11 into buffer and transmit Data Out.
DBSE	6575	Set Interrupt Enable to a 1.
DBCE	6576	Reset Interrupt Enable to a 0.
DBSS	6577	Issue a Strobe pulse.

REAL TIME CRYSTAL CLOCK INSTRUCTIONS (1 Cycle)

CLLE	6135	Load Interrupt Enable from AC11
		AC11 = 1, set Interrupt Enable
		AC11 = 0, clear Interrupt Enable
CLCL	6136	Clear Clock flag.
CLSK	6137	Skip if Clock flag = 1.

KM8-A EXTENDED OPTION BOARD INSTRUCTIONS

MEMORY EXTENSION/TIME SHARE CONTROL INSTRUCTIONS (1 Cycle)

GTF	6004	Jam Transfer the status of the flags and link into AC0, AC2, and AC4–AC11. (0 = cleared, 1 = set) AC0 = Link AC2 = Interrupt Request AC4 = Interrupt Enable AC5-11 = User Mode and Save Field
RTF	6005	Transfer the contents of AC5, AC6–AC11 to the user buffer flip-flop, the instruction buffer and data field, and inhibit processor interrupts until the next JMP or JMS instruction. User Field flip-flop and the Instruction Field are loaded at the conclusion of the next JMP or JMS instruction. The CPU loads the contents of AC0 into the Link and enables the interrupt system in response to this IOT.
CDF	62N1	Load the Data Field register with the program selected number N (N = 0–7).
CIF	62N2	Load the Instruction Buffer with the program selected number N (N = 0–7) and inhibit program interrupts until the next JMP or JMS instruction.
CDF CIF	62N3	Load the Data Field and Instruction Buffer with program selected number N (N = 0–7). Combines CDF and CIF.
RDF	6214	OR's the content of the Data Field register with AC6–AC8.
RIF	6224	OR's the contents of the Instruction Field register with AC6–AC8.
RIB	6234	OR's the contents of the Save Field with AC6–AC8 and AC9–AC11. The time share bit of the Save Field is ORed into AC5.
RMF	6224	Restores the contents of the Save Field register into the Instruction Buffer, Data Field, and (if time share is enabled) user buffer.
CINT	6204	Clear User Interrupt flip-flop.
SINT	6254	Skip if User Interrupt flip-flop is set.
CUF	6264	Clear User Buffer flip-flop (exit time share mode).
SUF	6274	Set User Buffer flip-flop (enter time share mode) following next JMP or JMS instruction.

POWER FAIL/AUTO RESTART (1 Cycle)

SPL	6102	Skip if AC Low flip-flop is set.
CAL	6103	Clear AC Low flip-flop.
SBE	6101	Skip if Battery Empty flip-flop is set.

A Communications Services Index that lists documentation available for the PDP-8/A may be obtained by writing:

>Digital Equipment Corporation
>Communications Services
>146 Main Street
>Maynard, Massachusetts 01754

A purchase order must accompany all documentation orders.

The following documents will be of interest to the PDP-8/A user:

- *PDP-8/A Miniprocessor Handbook*: Provides the user with a basic description of the PDP-8/A, basic interfacing information, and descriptions of DIGITAL interface hardware and basic operation and programming information.

- *Introduction to Programming* (1973 Edtion): Provides the experienced and inexperienced programmer the information necessary to program the PDP-8/A Miniprocessor.

- *PDP-8/A User's Manual* (EK-8A002-MM-001): Provides the user with detailed information on interfacing, troubleshooting, and maintenance.

- *OS/8 Handbook*: Provides the user the information to operate and program the PDP-8/A operating under the OS/8 system.

- *Illustrated Parts Breakdown* (EK-8A000-IP-001)

Diagnostics and supporting documentation are available from DIGITAL's Software Distribution Center. The PDP-8 Software Price List may be obtained by writing:

>Digital Equipment Corporation
>Software Distribution Center
>146 Main Street
>Maynard, Massachusetts 01754

The price list includes ordering instructions.

The following software kits are available for testing the PDP-8/A:

PDP-8/A Basic Software Kit (ZF006-RB)

MAINDEC-08-DJKKA-PB	PDP-8/A CPU Test
MAINDEC-08-DJKKA-D	PDP-8/A CPU Test Instructions
MAINDEC-08-DJMSA-PB	1–4K MS8-A MOS Memory Test
MAINDEC-08-DJMSA-D	1–4K MS8-A MOS Memory Test Instructions
MAINDEC-08-DJEXB-PB	2–32K Processor Exerciser
MAINDEC-08-DJEXB-D	2–32K Processor Exerciser Instructions
MAINDEC-08-DJMMA-PB	4–32K Memory Test
MAINDEC-08-DJMMA-D	4–32K Memory Test Instructions

PDP-8/A 1K and 2K Basic Software Kit (ZF007-RB)

MAINDEC-08-DJKKA-PM1	PDP-8/A CPU Test
MAINDEC-08-DJKKA-D	PDP-8/A CPU Test Instructions
MAINDEC-08-DJMSA-PM	1–4K MS8-A MOS Memory Test
MAINDEC-08-DJMSA-D	1–4K MS8-A MOS Memory Test Instructions
MAINDEC-08-DJEXA-PM	1–32K Random Memory Reference Instruction
MAINDEC-08-DJEXA-D	1–32K Random Memory Reference Instructions Exerciser Instructions
MAINDEC-08-DJEXB-PM	2–32K Processor Exerciser
MAINDEC-08-DJEXB-D	2–32K Processor Exerciser Instructions

1K and 2K DKC8-AA Option Software Kit (ZF207-RB)

MAINDEC-08-DJDKA-PM1	DKC8-AA Option Test 1
MAINDEC-08-DJDKA-PM2	DKC8-AA Option Test 2
MAINDEC-08-DJDKA-PM3	DKC8-AA Option Test 3
MAINDEC-08-DJDKA-PM4	DKC0-AA Option Test 4
MAINDEC-08-DJDKA-D	DKC8-AA Option Test Instructions

4K DKC8-AA Option Software Kit (ZF208-RB)

MAINDEC-08-DJDKA-PB1	DKC8-AA Option Test
MAINDEC-08-DJDKA-D	DKC8-AA Option Test Instructions

4K KM8-AA Option Software Kit (ZF209-RB)

MAINDEC-08-DJKMA-PB1	KM8-AA Option Test
MAINDEC-08-DJKMA-D	KM8-AA Option Test Instructions

1K, 2K KM8-AA Option Software Kit (ZF210-RB)

MAINDEC-08-DJKMA-PM1	KM8-AA Option Test 1
MAINDEC-08-DJKMA-PM2	KM8-AA Option Test 2
MAINDEC-08-DJKMA-PM4	KM8-AA Option Test 3
MAINDEC-08-DJKMA-D	KM8-AA Option Test Instructions

MR8-A ROM Software Kit (ZF211-RB)

MAINDEC-08-DJMRA-PM	MR8-A ROM Compare Test
MAINDEC-08-DJMRA-D	MR8-A ROM Compare Test Instructions

MR8-SA ROM Loader Software Kit (ZF204-RM)

MAINDEC-08-DJMRA-PB   MR8-A ROM Compare Test

MAINDEC-08-DJMRA-D   MR8-A ROM Compare Test Instructions
MAINDEC-08-DJMRB-PB   MR8-SA PROM Loader Program
MAINDEC-08-DJMRB-D   MR8-SA PROM Loader Program Instructions

MR8-FB 1K Software Kit (ZF196-RB)

MAINDEC-08-DHMRC-PB   MR8-FB PROM Compare Test
MAINDEC-08-DHMRC-D   MR8-FB PROM Compare Test Instructions
MAINDEC-08-DHMRE-PB   1K MR8-FB PROM Internal Test
MAINDEC-08-DHMRE-D   1K MR8-FB PROM Internal Test Instructions

These kits should be ordered by the kit number (i.e., ZF196-RB is the kit number for the 1K MR8-FB PROM).

APPENDIX C
WARRANTY AND MAINTENANCE SERVICES

WARRANTY STATEMENT

The PDP-8/A unit is warranted against defects in workmanship and material under normal use and service for a period of thirty (30) days from the date of shipment as indicated by the warranty seal located on the rear of the unit. Any such defect discovered by the buyer shall be corrected by DIGITAL at its nearest authorized factory repair depot as indicated on the following pages. It will be the buyer's responsibility to return the equipment prepaid. Transportation charges for the return to the buyer shall be paid by DIGITAL. As a condition of this warranty, shipping instructions for the return of the equipment must be obtained from the nearest authorized factory repair depot prior to shipment. Warranty service on the MR8-A Read-Only Memory can only be honored at the Westminister Manufacturing facility. DIGITAL does not assume any liability in connection with the shipment of the equipment. If DIGITAL determines that the equipment is not defective within the terms of this warranty, the buyer shall pay DIGITAL the cost of all transportation and labor at the then prevailing DIGITAL repair rates.

AUTHORIZED FACTORY RETURN WARRANTY REPAIR DEPOTS

NORTH AMERICA

CHICAGO
Digital Equipment Corporation
Depot Repair Department
5600 Apollo Drive
Rolling Meadows, Illinois 60008
Tel: (312) 640-5515

MAYNARD
Digital Equipment Corporation
Depot Repair Department
111 Powder Mill Road
Maynard, Massachusetts 01754
Tel: (617) 897-5111

KANATA
Digital Equipment of Canada, Ltd
Depot Repair Department
100 Herzberg Road
Kanata, Ontario, Canada
Tel: (613) 592-5111

SUNNYVALE
Digital Equipment Corporation
Deepot Repair Deprtment
310 Soquel Way
Sunnyvale, California 94086
Tel: (408) 735-9200

AUSTRALIA AND JAPAN

SYDNEY
Digital Equipment Australia Pty, Ltd.
Depot Repair Department
123–125 Willoughby Road
Crows Nest
N.S.W., Australia
Tel: (202) 439-2566

TOKYO
Digital Equipment Corp. International
Kowa Building 25 (Third Floor)
8-7 Sunban Cho
Chiyoda-ky, Tokyo, 102, Japan
Tel: (03) 264-7101

EUROPE

BRUSSSELS
Digital Equipment SA/DV
Depot Repair Deprtment
108 Rue d'Arion
B-1040 Bruxelies, Belgium
Tel: (02) 13-92-56

HOLLAND
Digital Equipment B.V.
Depot Repair Department
Kaap Hoorndreef 38
Postbus 9064
NL Utrecht
Tel: (02) 879051

MILAN
Digital Equipment S.P.A.
Depot Repair Department
Corso Garibaldi
1-20121 Milano, Italy
Tel: (02) 879051

MUNICH
Digital Equipment GmBH
Depot Repair Department
D-8000 Munchen 40
Wallensteinplatz 2, West Germany
Tel: 35-031

PARIS
Equipment Digital S.A.R.L.
Depot Repair Department
2 Place Gustave Eiffel
CIDEX L225
108, Rude d'Arion
94 533 Rungis, France
Tel: (01) 6877-2333

READING
Digital Equipment Co., Ltd.
Depot Repair Department
Building 8, Arkwright Road
Reading, Berkshire, England
Tel: ORE4 861196

STOCKHOLM
Digital Equipment AB
Depot Repair Department
Englundsvagen 7,3 TR
S-17141 Solina, Sweden
Tel: (08) 98-13-90

VIENNA
Digital Equipment Corp. Ges, G-B
Mariahilferstrasse 136
A-1150 Wien
Austria
Tel: (0222) 855186

ZURICH
Digital Equipment Corporation AG
Schaffhauserstr, 315
CH-8050 Zurich/Switzerland
Tel: (01) 464191

Omnibus Loading

Option	Module Number	+5 V	−15 V	+15 V	+20 V
PDP-8/A-AC AD		6.4 A	0.04 A		
PDP-8/A-AE AF		7.0 A	0.04 A		
PDP-8/A-AK AL		8.2 A	0.04 A		
PDP-8/A-BC BD		8.9 A	0.04 A		
PDP-8/A-FA FB		8.8 A	0.35 A		
KK8-A	M8315	5.0 A	0.04 A		
MM8-AA		1.60 A			2.0 A
MM8-AB		1.70 A			2.0 A
MS8-AA	M8311-YA	1.4 A			
MS8-AB	M8311-YB	2.4 A			
MS8-AD	M8311-YD	3.2 A			
MR8-AA	M8312-YA	2.15 A			
MR8-AB	M8312-YB	3.10 A			
MR8-AD	M8312-YD	5.00 A			
MR8-FB	M8349	3.8 A			
DKC8-AA	M8316	2.0 A	0.1 A		
KM8-AA	M8317	2.0 A	0.1 A		
KC8-AA	Programmer's Console	1.5 A			
DB8-E	M8326	0.80 A			
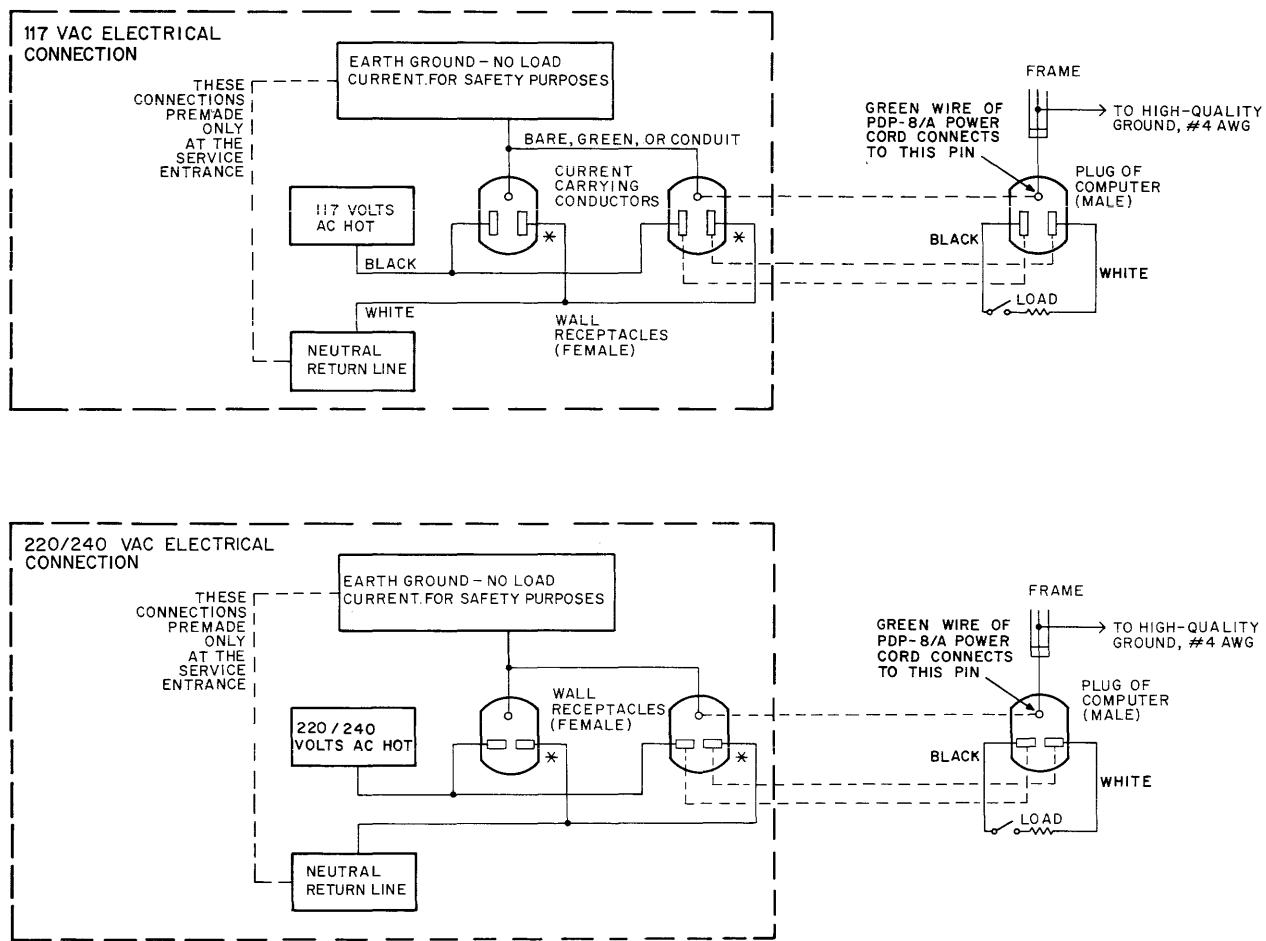
Omnibus Loading (Cont.)

Option	Module Number	+5 V	−15 V	+15 V	+20 V
DR8-E	M863	2.25 A			
DP8-E	M839, M866	1.80 A	0.05 A	0.105 A	
KL8-JA	M8655	1.0 A			
TA8-E	M8331	2.80 A			
Power Available G8016 Power Supply G8018 Power Supply		+5 V 20 A 25 A	−15 V 0.75 A* 2.0 A	+15 V 0.75 A* 2.0 A	

*Total current must not exceed 1.0 A.

The proper power connection for the PDP-8/A is shown in Figure E-1.

Figure E-1 PDP-8/A Electrical Connection

Reader's Comment

PDP-8/A OPERATOR'S HANDBOOK
EK-8A001-OP-002

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults do you find with the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

Would you please indicate any factual errors you have found. _____

_____

_____

_____

Please describe your position. _____

Name _____ Organization _____

Street _____ Department _____
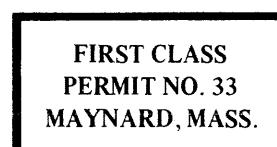
City _____ State _____ Zip or Country _____
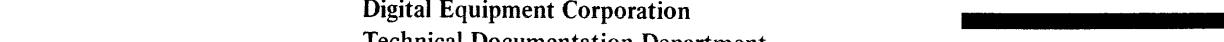
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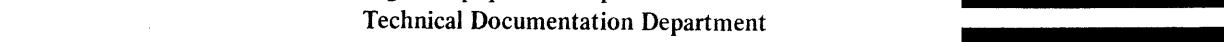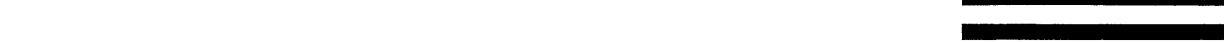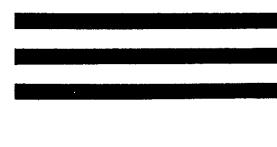
Digital Equipment Corporation
Maynard, Massachusetts

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