KA8/I
POSITIVE I/O BUS OPTION
FUNCTIONAL DESCRIPTION

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Instruction times, operating speeds and the like are included in this manual for reference only; they are not to be taken as specifications.

KA8/I
POSITIVE I/O BUS

INTRODUCTION

The DEC KA8/I Positive I/O Bus (Figure 1) consists of M660 and M661 Positive Level Driver modules and M516 Positive Bus Receiver modules. When these modules are inserted into the PDP-8/I they allow positive voltage levels on the PDP-8/I interface to external I/O options.

The positive levels are +0.2V for low logic states and +3.3V for high logic states, which allows direct TTL logic interfacing with the appropriate diode clamp protection.

The Positive I/O Bus reduces peripheral power requirements to only +5V and will accommodate cable lengths of up to 80 feet with a possible 64 optional loads. The actual cable length is dependent upon peripheral timing requirements and delays.

POWER

Nominal option power is 7.5W at +5 Vdc. This requirement is reduced by the power previously supplied for the replaced PDP-8/I Negative Bus modules which is 3.75W at +0.5 Vdc and 6.0W at -15 Vdc.

Input Signals

Logical one (1) is 2.4V (minimum).
Logical zero (0) is 0.4V (maximum).

Output Signals

Logical one (1) is 2.4V (minimum).
Logical zero (0) is 0.4V (maximum).

Driving Capabilities and Interface Restrictions

The Positive I/O Bus will drive 64 optional devices using the gating techniques described in the Basic System section of this manual. The optional current driving capabilities are described also.

Cable Lengths

Maximum of 80 feet for Alloy 135 coaxial cable.
Maximum of 14 feet for Flex-print cable.

Termination

100Ω terminations to ground for the clocking signals.

Basic System (Dwg. No. D-BS-KA8I-0-1)

The basic Positive I/O Bus system consists of two types of processor modules which are pin compatible with the present interface modules of the standard Negative I/O Bus. The processor modules consist of Positive Level Driver M660 and M661 which replace the Negative Output Converter M650 and the Positive Bus Receiver M516 replaces the Negative Input Converter M506.

Positive Level Driver M660 incorporates diode clamps and requires cable terminations which provide clean transistions to the high or low logic levels along the bus. The signal transistions are suitable for use as clocking signals. Positive Level Driver M661 incorporates diode clamps only with the signals being suitable for data and address information.

Two data break pulse signals and the buffered (B) WC OVERFLOW (0) and B ADD ACCEPTED (0) signals have clean transitions to the high level because of the data break device being at the cable end. The low transistion however, does have reflections;

therefore, it is suggested that the low level signal transistions be used as clearing, setting, or data signals in place of the clocking signals.

The input signals to the Positive I/O Bus are received by the M516 Positive Bus Receiver module which has diode clamps on its external inputs. The internal input signals are processed in a manner similar to those on the M506 Negative Input Converter. Activation of the external input signals to a ground level is directly compatible to the input ground levels of the PDP-8/I negative bus.

Loading Characteristics

Loading characteristics are defined in two ways: the first involves restrictive loading techniques, allowing 64 device selections with associated data transfers and timing which are applicable for devices using programmed data transfers; the second is the absolute current driving capabilities which are applicable for data-break transfers.

Figure 1 is a typical bus system which will be used for discussing restrictive loading techniques. In presenting this technique, it must be remembered that the option selection network provides the hold-off current for data and timing signals, thereby relieving bus loading. Loading for other signals is shared as follows.

Gate 1 - This is the device selection gate which constantly monitors 6 of the high-level MB bits (MB3-8) from the Positive Level Driver module M661 and which provides an OPTION IOT signal when the specified load is selected. The device control input to the NOR gate has the ability for a peripheral device to force the device selection when used in a data-break device. Both sides of the MB flip-flop (MB3-8) are provided for this decoding although only 6 of the 12 signals are used for a single IOT device code. This format allows current sharing of Gate 1 loading with a driving capability of 64 selection gates. Characteristics of the TTL logic gate are such that a maximum total of 1.6 mA is required for all inputs to hold gate 1 off and only 40 μA per input to activate it. For 64 devices, each requiring 1.6 mA and 6 input lines, the loading per line for the low level is only 17 mA $\left(\frac{64 \times 1\ mA}{6}\right)$.

Gates 3 and 4 - These gates represent the gating by device selection network which limits the data and timing bus loading to the single selected options.

The OPTION IOT signal provides the 1.6 mA necessary to hold the unselected option gates off. The 40 μA necessary for activation of any option gate is provided by the Positive I/O Bus. BAC 0 through 11 data signals from the M661 Positive Level Driver, at the NAND gate 4 output, are at a low level (DATA) and are used to clear, or load to zero, the appropriate flip-flops. The IOP-1, -2, and -4 timing signals from the M660 Positive Level Driver, at the NAND gate 3 output, are also at a low level (TIMING) and provide the return bus enabling signals with a minimum delay.

Maximum loading for data signals from the M661 Positive Level Driver modules is two high levels per option for a total load of 5.1 mA (4 μA X 2 X 64). Timing signals from the M660 Positive Level Driver require an additional current of approximately 33 mA for termination.

B INITIALIZE Signal

The output B INITIALIZE signal from NAND Gate 2 is a requirement in all options but cannot be gated by the OPTION IOT signal or shared like the MB signals.

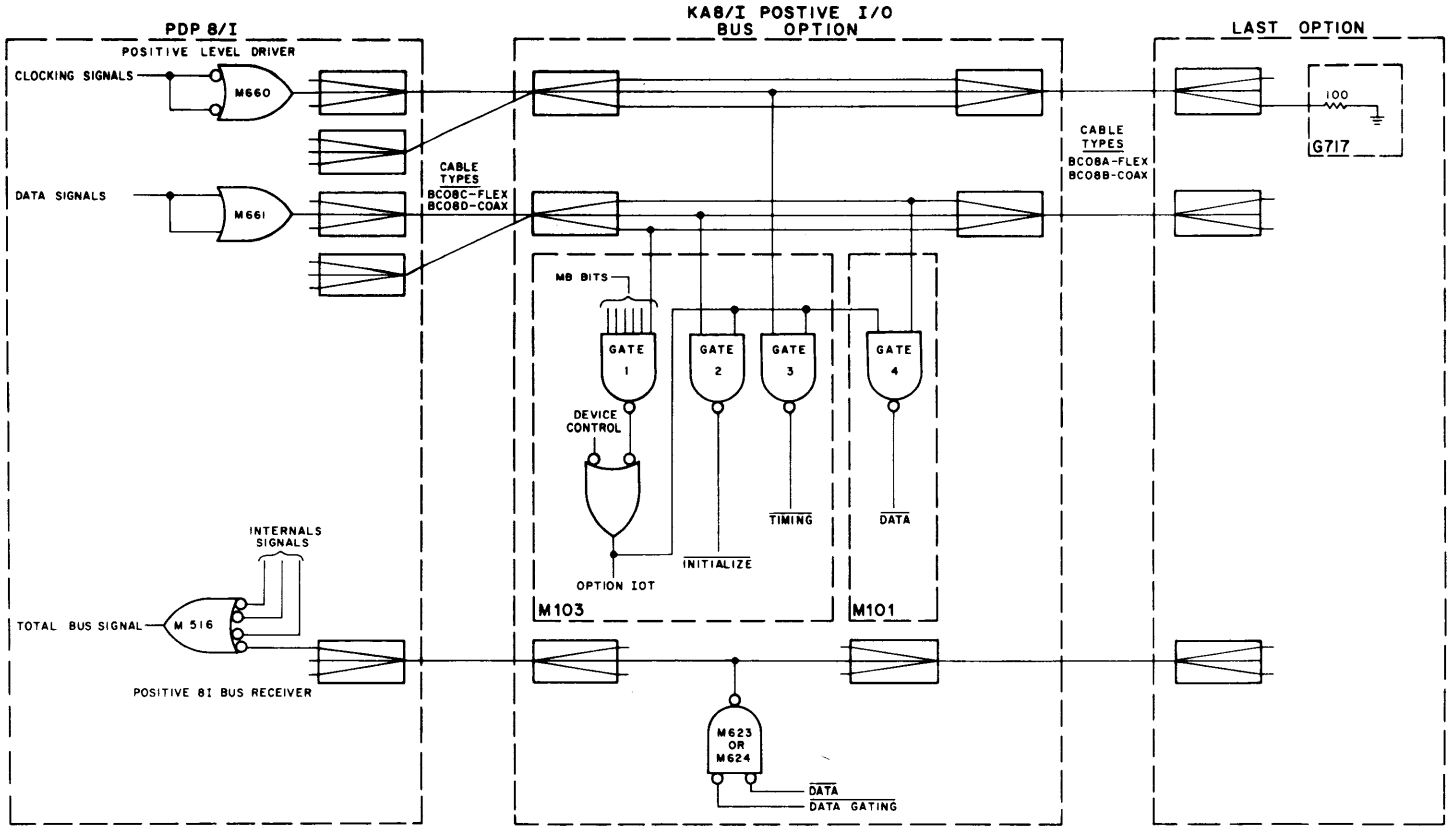


Figure 1 Representative Positive 8/I Bus

The low data signal required for 64 inputs, with one input per selection being 102 mA (64 X 1.6 mA) is provided by the M660 Positive Level Driver which uses an extra signal line to reduce cable attenuation. This extra signal line is not terminated and therefore, subject to partial positive transistions along the cable with reflections on the ground transistions. Because the B INITIALIZE signal is used to clear the system at machine initialization, it is acceptable for clearing the flip-flops.

If OPTION IOT gating is not used, absolute current driving capabilities are required to insure the worst case TTL logic levels of a minimum high level of 2.4V and a maximum low level of 0.4V. This capability is suited for data-break signals where either the data-break device or a multiplexing unit is alone on the line and also applies for the generalized case involving signals being utilized for programmed data transfers. The Positive I/O Bus will drive +5 mA at the high level and sink 20 mA at the low level. Only the M660 Positive Line Driver module provides the termination requirements where applicable. The number of TTL loads that can be accommodated with unrestrictive loading techniques is limited to the low level to 12.

Connections

Connections between the PDP-8/I processor and the first option are made by five sets of double cables, each having one double-sided cable connector and two single-sided cable connectors. Figure 2 shows the pin-to-pin connections for the processor interface cable. Correlation of the PDP-8/I cable allocations to the standard option al-

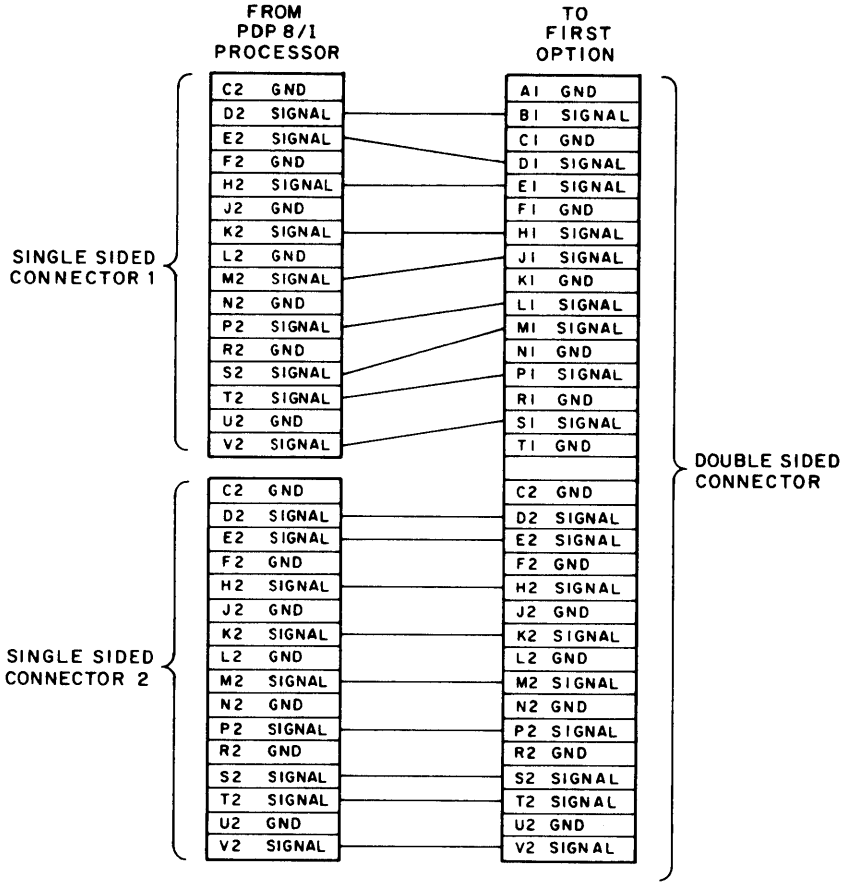


Figure 2 Processor Interface Cable Connection Diagram

locations are shown in Figure 3. Table 1 combines the information of the two figures and presents the signal pins within an option.

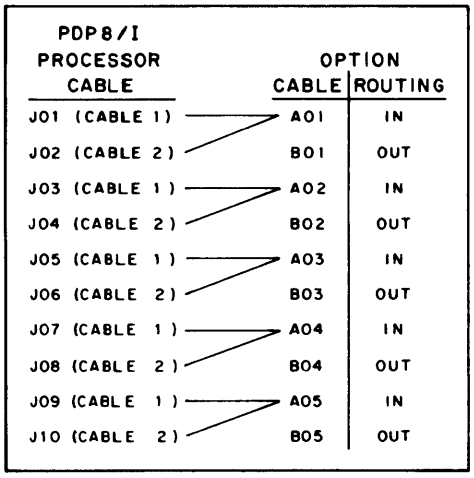


Figure 3 Correlation of PDP-8/I Cable Allocations to Standard Option Allocations Diagram

Cable allocations and routing in the equipment option, shown in Figure 3, is referenced by the (IN) and (OUT) notations. Cable A01 is a double-sided combination of the processor cables J01 and J02 with its input at A01 and its output at B01. Interface connections for the B INITIALIZE and EXT DATA ADD 0, -1, and -2 signals are added to the PDP-8/I processor cable. Connections for B INITIALIZE parallel this heavily loaded signal while the EXT DATA ADD 0, -1, and -2 connections eliminate the need for a separate cable at J11. Connections between the options are made by five sets of double cables with double-sided cable connector boards at each end.

Use of the specific option modules shown in Figure 1 is recommended in order to provide the diode clamps within these modules.

Resistive terminations of 100Ω on the G717 Resistor Terminating module are inserted into the last option position in the cable slot B01. The 100Ω terminated signals are BIOP1, BIOP2, BI04, BTS3(1), and BTS1(1).

Input Levels

Input levels to the PDP-8/I processor are provided by the +3.5V diode clamps located on the M516 Positive Bus Receiver and the open collector bus drivers in each option.

Cable Length

The 14 foot Flex-print cable minimizes cross-talk and is of sufficient length to connect the options together in the PDP-8/I cabinet. A maximum coaxial-cable length of 80 feet is conditioned by delay and cable attenuation.

Several of the open collector circuits effectively provide a wired OR circuit for returning signals, with the ground signals representing the active state of the input bus. Each of 64 options is allowed a single open collector connection for an input signal.

CAUTION

For 80 feet of coaxial cable a maximum peripheral delay path of 55 ns is required. A delay longer than this compromises the maximum cable length. Complex timing arrangement in data-break devices and partial transistions on unterminated lines also may reduce the allowed cable length.

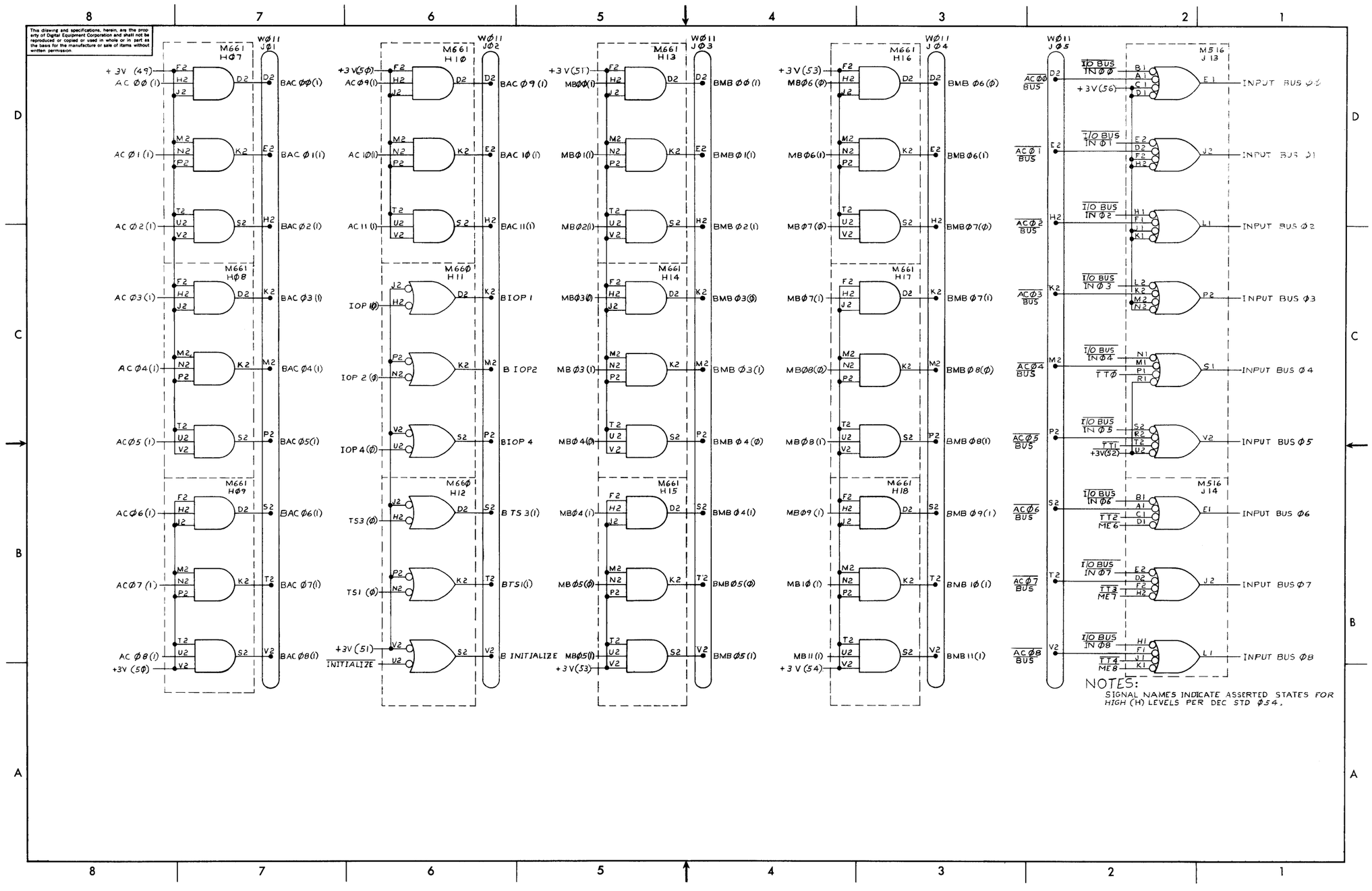
Delay On Processor I/O Strobe Signal

Extension of the delay on the PDP-8/I processor I/O strobe signal to 500 ns allows a maximum cable length of 80 feet to be used for programmed data transfers.

Table 1
Cable Allocation For Positive I/O Bus Peripherals

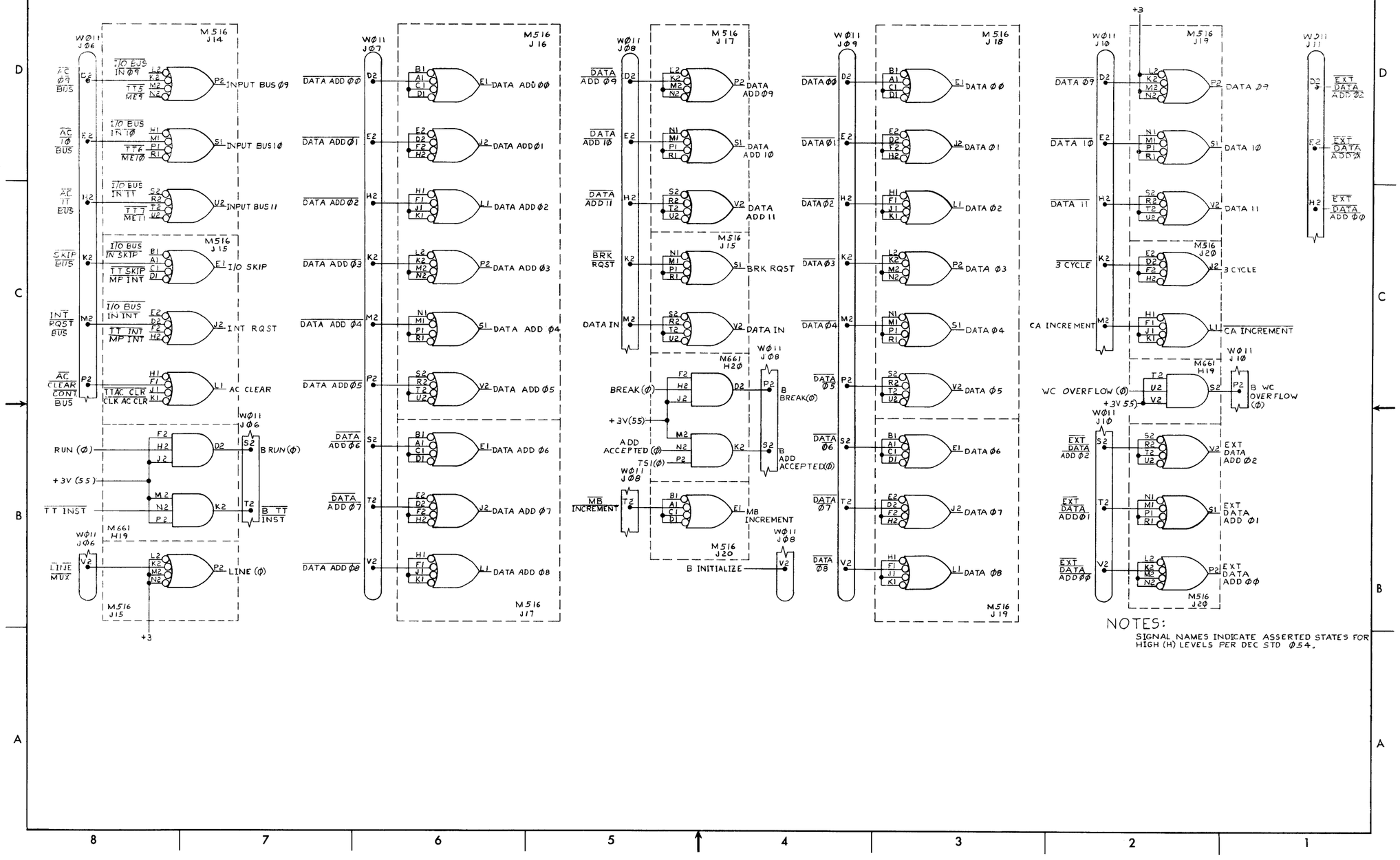
PIN	A01 B01	A02 B02	A03 B03	A04 B04	A05 B05
B1	BAC00 (1) H	BMB00 (1) H	AC00 BUS L	DATA ADD 00 L	DATA00 L
D1	BAC01 (1) H	BMB01 (1) H	AC01 BUS L	DATA ADD 01 L	DATA01 L
E1	BAC02 (1) H	BMB02 (1) H	AC02 BUS L	DATA ADD 02 L	DATA02 L
H1	BAC03 (1) H	BMB03 (0) H	AC03 BUS L	DATA ADD 03 L	DATA03 L
J1	BAC04 (1) H	BMB03 (1) H	AC04 BUS L	DATA ADD 04 L	DATA04 L
L1	BAC05 (1) H	BMB04 (0) H	AC05 BUS L	DATA ADD 05 L	DATA05 L
M1	BAC06 (1) H	BMB04 (1) H	AC06 BUS L	DATA ADD 06 L	DATA06 L
P1	BAC07 (1) H	BMB05 (0) H	AC07 BUS L	DATA ADD 07 L	DATA07 L
S1	BAC08 (1) H	BMB05 (1) H	AC08 BUS L	DATA ADD 08 L	DATA08 L
D2	BAC09 (1) H	BMB06 (0) H	AC09 BUS L	DATA ADD 09 L	DATA09 L
E2	BAC10 (1) H	BMB06 (1) H	AC10 BUS L	DATA ADD 10 L	DATA10 L
H2	BAC11 (1) H	BMB07 (0) H	AC11 BUS L	DATA ADD 11 L	DATA11 L
K2	BIOP 1 H	BMB07 (1) H	SKIP BUS L	BRK ROST L	3 CYCLE L
M2	BIOP 2 H	BMB08 (0) H	INTRQST BUS L	DATA IN L	CA INCREMENT L
P2	BIOP 4 H	BMB08 (1) H	AC CLR CONT BUS L	B BREAK (0) H	B WC OVERFROL (0) L
S2	BTS 3 (1) H	BMB09 (1) H	B RUN (0) H	B ADD ACCPT (0) H	EXT DATA ADD 2 L
T2	BTS 1 (1) H	BMB10 (1) H	B TTINST H	MB INCREMENT L	EXT DATA ADD 1 L
V2	B INITIALIZE H	BMB11 (1) H	LINE MUX L	B INITIALIZE H	EXT DATA ADD 0 L

NOTE: The L or H postscript indicates the logic level for the signal named (i.e., the logic situation named is true when the level noted exists).



NOTES:
SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH (H) LEVELS PER DEC STD Ø54.

Dwg. No. D-BS-KA8I-0-1 Positive I/O Bus Schematic Diagram (Part 1)



Dwg. No. D-BS-KA8I-0-1 Positive I/O Bus Schematic Diagram (Part 2)