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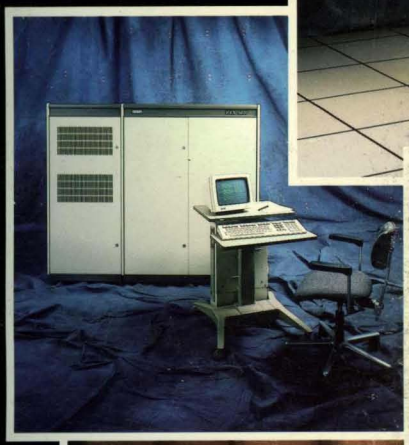
VAX Hardware Handbook

Volume 2–1986



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VAX Hardware Handbook

Volume 2–1986

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Volume 2 — 1986

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Preface

Volume 2 of the *VAX Hardware Handbook* describes the latest additions to Digital's VAX family. Included are seven recently introduced VAX systems — VAX 8800/8700, VAX 8650, VAX 8500/8550, and VAX 8200/8300 — each consisting of a 32-bit central processor, memory, console subsystem, operating system and system software, storage devices, communications equipment, and optional hardware and software products.

Volume 2 also describes the newer VAX family mass storage products — the HSC70 and KDB50 intelligent controllers, and the TA81 and TU81-Plus tape drives.

For basic concepts and features of VAX hardware and architecture refer to Volume 1 of the *VAX Hardware Handbook* and the *VAX Architecture Handbook*. For popular system configurations or to configure systems tailored to your applications, consult your nearest Digital Sales Office and the *VAX Systems and Options Catalog*. Other useful references are the *VAXBI Options Handbook, VAX Software Source Book,* and the *Networks and Communications Buyer's Guide.*

Chapter 1 ▪ Overview: Digital's Second-generation VAX Systems

Digital's VAX computers represent the only fully compatible, integrated, and fully networked family of computers available in the industry. Spanning a range from powerful large systems to individual workstations, these second-generation VAX systems include the VAX 8800, VAX 8700, VAX 8650, VAX 8600, VAX 8550, VAX 8500, VAX 8300, VAX 8200, and MicroVAX II systems. These systems expand users' choices and represent dramatic improvements in price and performance. All use the same VMS operating system — giving users access to more than 3,000 applications programs. And all take advantage of the most extensive computer networking products available in the industry today.

Table 1-1 gives a quick overview of the capabilities and options of the VAX systems discussed in the two volumes of the hardware handbook. Note that cost-effective upgrade options exist between numerous systems to further protect your investment.

Table 1-1 ▪ VAX System Comparison Chart

	MicroVAX II, VAXstation II/ VAXstation II/GPX	VAX-11/780	VAX 8200 VAX 8300	VAX 8500 VAX 8550	VAX 8600 VAX 8650	VAX 8700 VAX 8800
CPU Technology	ZMOS	Bipolar Schottky TTL	ZMOS	ECL Gate Array	ECL Gate Array	ECL Gate Array
Performance × VAX-11/780	0.9	1.0	8200: 1.0 8300: 1.6-1.9*	8500: 3 8550: 6	8600: 4.2 8650: 6	8700: 6 8800: 9-12*
MEMORY						
Type	256 Kbit Parity MOS	256 Kbit ECC MOS	256 Kbit ECC MOS	256 Kbit ECC MOS	256 Kbit ECC MOS	256 Kbit ECC MOS
Maximum Support	16 MB	64 MB	24 MB	80 MB	68 MB	128 MB
Minimum Support	2 MB	2 MB	4 MB	20 MB	8600: 4 MB 8650: 16 MB	32 MB
Cache Size	NA	8 KB	8200: 8 KB 8300: 8 KB × 2	64 KB	16 KB	8700: 64 KB 8800: 64 KB × 2
Cache Access Time	NA	200 ns	200 ns	45 ns	8600: 80 ns 8650: 55 ns	45 ns
I/O Max. Throughput	3.3 MB/s	13.3 MB/s	13 MB/s	16 MB/s	8600: 20 MB/s 8650: 26 MB/s	>30 MB/s

PROCESSOR OPTIONS						
Floating-point Accelerator	Standard	Optional	Standard	Standard	Optional	Standard
Data Types Supported	F, D, G	F, D	F, D, G	F, D, G, H	F, D, G, H	F, D, G, H
Extended Range Floating-point–G, H	Standard-G	Optional	Standard	Standard	Standard	Standard
Writable Control Store (WCS)	NA	Optional	NA	Standard	Standard	Standard
WCS Size	NA	2 Kword	NA	16 Kword	8 Kword	8700: 16 Kword 8800: 1 Kword × 2
WCS Word Size	NA	99 bits	NA	144 bits	86 bits	144 bits
CONFIGURATION						
VAXcluster Support	NA	Optional	Optional	Optional	Optional	Standard
HSC50/HSC70 Support	NA	Up to 15	Up to 15	Up to 15	Up to 15	Up to 15
I/O Buses	1 Q-Bus	1 SBI 4 UNIBUS 4 MASSBUS	1 VAXBI 1 UNIBUS	2 VAXBI 1 UNIBUS	2 SBI 7 UNIBUS 4 MASSBUS	4 VAXBI 2 UNIBUS
Ethernet Support	Optional	Optional	Standard	Standard	Standard	Standard
UPGRADE OPTION	None	None	8200: to 8300 8300: none	8500: to 8550 8550: none	8600: to 8650 8650: none	8700: to 8800 8800: none

*For multistream applications

▪ New Top-of-the-line Systems

The top-of-the-line *VAX 8800*, Digital's highest performance system, delivers 9 to 12 times the power of the standard VAX-11/780 system for both compute-intensive and interactive/multiuser environments.

Applications such as simulation, analysis, design, and complex modeling run extremely well on the VAX 8800. Similarly, users with the broad mix of applications found in the finance, service industries, manufacturing, education, and business also benefit from the performance of the VAX 8800.

The VAX 8800 design has been optimized for multiprocessing and includes up to 128 Mbytes of fully sharable ECC memory, two 64 Kbyte caches, very high bus bandwidths, and an intelligent console subsystem. The VAX 8800 uses Digital's new VAXBI bus architecture as its I/O bus system. With expansion to four VAXBI channels and greater than 50 Mbytes/s CPU/Memory bandwidth, the VAX 8800 sets new standards for flexibility and performance.

The *VAX 8700* is an expandable uniprocessor system that provides future growth to the larger VAX 8800 multiprocessor. A single VAX 8700 CPU has all the design attributes of the larger VAX 8800 processor and provides about one-half the performance. Both the VAX 8700 and the VAX 8800 can access up to four VAXBI channels and up to 128 Mbytes of memory.

▪ Power in Compact Packages

The other computers discussed in this volume — the VAX 8650, the VAX 8550 and VAX 8500, plus the VAX 8200 and VAX 8300 — deliver large-system functions with midrange pricing and packaging.

The *VAX 8650* CPU provides up to six times the performance of the VAX-11/780. Like the VAX 8600 (described in Volume 1), the VAX 8650 is a high-performance, general purpose VAX system designed for use in traditional data processing applications. The VAX 8650 computer uses advanced internal processor structures to overlap processing of multiple instructions. Its interconnect structure allows the choice of CI, UNIBUS, or MASSBUS adapter products.

The *VAX 8500* and *VAX 8550* are excellent choices for applications where cost per user is paramount, and where high performance is required in limited space. The VAX 8500's performance is three times that of the standard VAX-11/780, while the VAX 8550 delivers up to six times the performance of the VAX-11/780. Housed in compact packages that occupy only 5.6 square feet of floor space, VAX 8500/VAX 8550 systems address all technical and commercial applications.

The *VAX 8200* brings full VAX functionality and the performance of the VAX-11/780 in one-fourth the footprint. The *VAX 8300* has up to 1.9 times the power of the VAX 8200 and like the VAX 8800, it provides improved price/performance in many multistream applications such as in engineering, laboratory, realtime, and interactive multiuser environments. The VAX 8200/VAX 8300's 24 Mbytes (maximum) of main memory and low price make these systems the first choice for general purpose applications in office, manufacturing, commercial, and scientific applications. The VAX 8200/VAX 8300 complement the MicroVAX II wherever applications call for large system functions, such as VAXcluster support, large memory capacity, high system I/O performance, wide selection of peripherals, and broad configuration flexibility.

▪ VAXBI Bus — For the New Generation of VAX Systems

The VAX Bus Interconnect (VAXBI) is the new 32-bit synchronous bus for Digital's new generation of midrange and high-end VAX systems. Designed for high performance and high reliability, the VAXBI bus serves as the I/O bus for the VAX 8800, VAX 8700, VAX 8500, and VAX 8550 systems; and both the system and I/O bus for the VAX 8200 and VAX 8300 systems.

The VAXBI is a clocked synchronous bus with a 200-nanosecond cycle time. It supports 30-bit physical addressing, multiple processors, and up to 16 total nodes. A standard one-chip interface implements all bus protocols. This VAXBI interface incorporates into a single chip the contents of 2.5 printed circuit board assemblies — considerably reducing the power requirements, size, and cost of the second-generation computer systems.

With an increased aggregate throughput, the VAXBI bus provides substantial gains in communication speed within the system, while simplifying design efforts for developers of peripheral devices and for OEMs who incorporate the new VAX computers into their products. Destined to dramatically change the way computer interfaces are designed and used, the VAXBI reduces product development cycles and cuts design costs.

To protect customers' investments in existing equipment, Digital also offers a VAXBI-compatible UNIBUS adapter. This adapter makes it possible to continue using many standard and specialized peripherals currently supported by UNIBUS-based VAX computers.

▪ VAXcluster Configurations Increase VAX System Capacity

From the VAX 8800 to the VAX 8200, all Digital's high-end and midrange VAX computers can serve as part of a VAXcluster System.

VAXclusters link the computers and one or more shared mass-storage subsystems to form Digital's highest-capacity VAXcluster Systems. A VAXcluster port is standard on the VAX 8800 and is optional on all other systems. An Ethernet port for connecting to local area networks is included in all base configurations.

VAXclusters with multiple VAX 8800 computers and storage subsystems provide mainframe computing power and capacity. VAXcluster Systems can be created with more than 100 times the power of a VAX-11/780 system and more than 100 Gbytes of storage. And all of this power and capacity is available to every user.

▪ Features Common to All VAX Processors Systems

Processor Specific Features — All VAX processors implement the 32-bit VAX architecture, an extensive instruction set with numerous data types, and a 32-bit bus structure for high data throughput. This is coupled with a virtual address space of up to 4 Gbytes (2 Gbytes user accessible), sixteen 32-bit general purpose registers, twelve addressing modes, and thirty-two interrupt levels that together provide a versatile and efficient processor system.

Console Subsystem — All VAX systems employ a microprocessor-based console subsystem that allows the user, system manager, or service engineers to communicate with the system through the console terminal.

In console mode, the processor can be started or halted, self-tested, initialized to a known state, and single-stepped through instructions. Information in memory, storage locations, and internal registers can be examined and data can be deposited into these locations. Diagnostic maintenance and bootstrap programs can be loaded from the console load device and controlled by the console terminal.

When the remote diagnostic service is included as part of a Digital Field Service contract, the diagnostic testing can also be controlled through the console subsystem from a remote Digital test facility.

VMS Operating System — VAX system hardware is complemented by the VMS operating system, which is continually being enhanced to provide more capabilities and more efficient system operation. VMS is a powerful multiprogramming operating system capable of supporting many users in realtime, interactive timesharing, and multistream batch applications. It also provides support for online program development.

VAXELN Realtime Software Toolkit — For applications requiring realtime code development, the VAXELN Toolkit provides the resources. A VMS layered product, the VAXELN Toolkit generates tight execution code for a dedicated realtime processor on which the VAXELN kernel controls the use of shared system resources. At the same time, running on a VAX or MicroVAX system, the VAXELN Toolkit gives access to the rich software development resources of the VMS environment. Refer to your Digital sales representative for availability.

ULTRIX-32 Operating System Option — The ULTRIX-32 operating system has been added to the VAX system family to provide users with a commodity-software base for 32-bit systems. The ULTRIX-32 system is Digital's enhanced native-mode UNIX operating system. It offers the standard set of UNIX languages and utilities. Check with your local Digital sales representative for availability.

VAXcluster System Configurations — The VAXcluster architecture enables up to 16 VAX processors or HSC50/HSC70 intelligent mass-storage servers to be connected together through the SC008 Star Coupler unit to form a single high-performance system. Through the VAXcluster, the processing power of many VAX processors becomes available and each processor is allowed access to a common data file.

The HSC50 and HSC70 intelligent-mass storage I/O servers optimizes the system data throughput by controlling the operation of disk drives or tape drives and formatters. The SC008 Star Coupler unit forms the common connection point for the cables from the processors and intelligent servers.

By providing common access to data files, the cost of development software and support of multiple databases when a system is expanded is significantly reduced. When more processing power is required, the VAX system selected can be tailored to the new system requirements without adding unnecessary hardware or software.

Communication Capabilities — The full capabilities of the VAX hardware and software are further enhanced by the Digital Network Architecture (DNA). DNA enables communication between VAX systems and other Digital systems and between Digital systems and systems developed by other manufacturers.

Digital offers extensive capabilities that permit the linking of computers and terminals into flexible network configurations to increase the efficiency and cost-effectiveness of data processing operations. DECconnect is the integrated communications solution that brings ThinWire Ethernet and other communication options to the office. And Ethernet is Digital's high-speed local area communications network that enables computer systems and terminals, whether located centrally or at remote sites, to exchange information and to share resources.

Digital Storage Architecture (DSA) — DSA is Digital's framework of standardized interfaces that permits the addition of new products and technologies that operate with different host systems without the need to develop new controllers and device drivers. DSA allows an expanding group of mass-storage products, including disk and magnetic tape drives, to be implemented into an intelligent mass-storage subsystem that provides a high standard of data integrity, fast data throughput, and many reliability features.

The following sections describe the new VAX systems and indicate the configurations available for each. Block diagrams of the system hardware are located in the processor chapters.

▪ VAX 8800 High-performance System

Digital's VAX 8800 computer system is the highest performance member of the VAX family of computers. These high-performance systems implement the VAX architecture, continuing complete software compatibility with all other VAX systems. VAX 8800 systems are tightly coupled multiprocessing systems comprising two CPUs that share up to 128 Mbytes of memory.

The VAX 8800 CPU features virtual memory management, bootstrap loader, standard instructions for packed decimal, floating (D, F, G, and H data types) and fixed-point arithmetic, character, and string manipulations, two 64-Kbyte direct-mapped write-through cache memories, high-precision programmable realtime clock, time-of-year clock with battery backup, and two 16-Kword (144-bit words) writable control stores. The CPU also includes the memory controller and memory battery backup for a full 128 Mbytes of memory capacity. Standard with all VAX 8800s is a VAXcluster port, Ethernet port, and two VAXBI channels. The CPU also includes a console subsystem based upon a J-11 chip set with videoterminal, 30-Mbyte Winchester disk, RX50 floppy disk, and remote diagnostic port.

VAX 8800 systems are available with a VMS operating system that provides a reliable, high-performance environment for the concurrent execution of multiuser timesharing, batch, and realtime applications.

The following VAX 8800 System Building Block configurations are available:

- VAXcluster System Building Blocks
- VMS System Building Blocks

▪ VAX 8700 System

The VAX 8700 and VAX 8800 are similar systems. The VAX 8700 System can be transformed to a VAX 8800 by adding an upgrade kit. See Figure 1-2. The major difference between the two systems is that the VAX 8700 contains one processor and the VAX 8800 contains two. Also, the VAX 8700 contains one VAXBI I/O bus (with eleven usable slots) as a standard feature while the VAX 8800 has two (with five usable slots each).

▪ VAX 8650 System

The VAX 8650 computer system is a UNIBUS-based high-performance member of the VAX family. It is functionally identical to the 8600 but offers 44 percent more performance.

The VAX 8650's central processor uses 32-bit architecture with 4 Gbytes of virtual addressing space. It features virtual memory management, bootstrap loader, standard instructions for packed decimal, floating (D, F, G, and H data types) and fixed-point arithmetic, character and string manipulations, 16-Kbyte write back cache memory, high-precision programmable realtime clock, time-of-year clock with battery backup, and 8 Kwords (86-bit words) of writable control store. The CPU also includes the memory controller and battery backup for 68 Mbytes of memory.

Standard with the VAX 8650 is a DF112 modem for remote diagnosis. The CPU also includes a console subsystem with an RL02 disk drive, DCT11 microcomputer, console terminal, and remote diagnostic port. (The console terminal is not included. It must be selected from the menu.)

VAX 8650 systems can be ordered with the VMS or ULTRIX-32 operating system. VMS provides a reliable, high-performance environment for the concurrent execution of multiuser timesharing, batch, and realtime applications. The ULTRIX-32 operating system is a reliable, demand-paged, virtual-memory, timesharing native UNIX operating system.

The following VAX 8650 System Building Block configurations are available:

- VAXcluster System Building Blocks
- VMS System Building Blocks
- ULTRIX-32 System Building Blocks

▪ VAX 8550 and VAX 8500 Systems

Digital's VAX 8500 and VAX 8550 computer systems are gateways to Digital's high-end VAXBI systems. These high-performance systems implement the VAX architecture, continuing complete software compatibility with all other VAX systems. The control processor uses 32-bit architecture with 4 Gbytes of virtual addressing space.

The VAX 8500/VAX 8550 CPUs feature virtual memory management, bootstrap loader, standard instructions for packed decimal, floating (D, F, G, and H data types) and fixed-point arithmetic, character and string manipulations, a 64-Kbyte direct-mapped write-through cache memory, high-precision programmable realtime clock, time-of-year clock with battery backup, and a 16-K word (144-bit words) writable control store. The CPU also includes the memory controller for 80 Mbytes of memory capacity. Standard with all systems is an Ethernet port, and one VAXBI channel. The CPU also includes a console subsystem based upon a J-11 chip set with videoterminal, 30-Mbyte Winchester disk, RX50 floppy disk, and remote diagnostic port.

VAX 8500 and VAX 8550 systems can be ordered with a VMS operating system. VMS provides a reliable, high-performance environment for the concurrent execution of multiuser timesharing, batch, and realtime applications.

The following VAX 8500 and VAX 8550 System Building Block configurations are available:

- Preconfigured System Building Blocks
- VAXcluster System Building Blocks
- VMS System Building Blocks

▪ VAX 8200 and VAX 8300 Systems

Digital's VAX 8200 and VAX 8300 computer systems are midrange members of the VAX family of computers that use the VAXBI as both a system and I/O bus. These high-performance systems implement the VAX family architecture, making them software compatible with other VAX systems. The VAX 8200 is a single-processor system. VAX 8300 systems are tightly coupled multiprocessors, consisting of two VAX 8200 CPUs accessing up to 24 Mbytes of shared memory. The central processors use 32-bit architecture with 4 Gbytes of virtual addressing space.

Both the VAX 8200 and VAX 8300 CPUs feature virtual memory management, bootstrap loader, standard instructions for packed decimal, floating (D, F, G, and H data types) and fixed-point arithmetic, character and string manipulations, two 8-Kbyte for the VAX 8300 and 8-Kbyte for the VAX 8200 direct-mapped write-through cache memories, programmable realtime clock, and time-of-year clock with battery backup. The CPU also includes a console subsystem with an RX50 floppy disk.

Systems can be ordered with a VMS operating system. VMS provides a reliable, high-performance environment for the concurrent execution of multiuser timesharing, batch, and realtime applications.

The following VAX 8300 and VAX 8200 System Building Blocks are available:

- Preconfigured System Building Blocks
- VAXcluster System Building Blocks
- VMS System Building Blocks
- ULTRIX-32 System Building Blocks (VAX 8200)

Mass-storage Extensions

Mass-storage extensions are based on the Digital Storage Architecture (DSA), a carefully designed framework that provides the advantages of easy, incremental system growth, fine-tuned I/O performance, high data integrity, and file compatibility. DSA eliminates the need for the VMS operating system to support every unique storage device with its own driver. To optimize disk operation, the operating system communicates with an intelligent disk controller using Digital's standard Mass Storage Control Protocol (MSCP) to optimize disk operation. The controller can support several devices. When you want to add more storage, you simply plug in an additional device.

KDB50 Single-host Disk Controller

The KDB50 is a high-performance microprocessor-based VAXBI disk controller that has been designed for fast, reliable, and optimum RA-disk throughput on the new VAXBI systems.

Providing a usable, sustained transfer rate of over 1 Mbyte/s, the KDB50 connects up to four RA-series SDI disks to the VAXBI bus. Each RA-series disk drive ranges in capacity from 121 Mbytes to 456 Mbytes for a total capacity of over 2.8 Gbytes per KDB50.

The KDB50 connects directly to the VAXBI, providing the fast burst data rates (up to 3 Mbytes per second) needed to support high-throughput requirements. With improved I/O performance, VAXBI systems can respond to requests more quickly and move on to the next task. The result is better overall systems performance, higher user satisfaction, and improved CPU utilization.

HSC70 High-performance Mass-storage Server

The newest member of the HSC family of intelligent storage servers, the HSC70 enhances HSC50 performance with greater drive connectivity, I/O command handling performance, operational convenience, and reliability.

The HSC70 server offloads all disk management functions from the host systems and provides host-independent sharing of common data among a network of locally connected VAX-11/750 and larger processors. It connects both disk and tape drives to all of the host computers in the VAXcluster and supports a combination of eight disk and tape data channels. Each disk data channel supports four drives over the standard disk interface (SDI). Each tape data channel supports four tape formatters over the standard tape interface (STI) and, depending upon which formatter is used, from one to four tape transports can be supported by each formatter.

The HSC70 connects to one or more host computers by means of the 70 Mbit-per-second dual-path computer interconnect (CI) bus. The CI can accommodate up to 16 nodes or connected devices. Therefore, a single microprocessor-controlled HSC70 server can provide storage services for as many as 15 VAX host computers and as many as 32 mass-storage devices.

TA81 Magnetic Tape Subsystem

Midrange in price and performance, the TA81 conforms to the ANSI standard for Group Code Recording (6,250 bits per inch) and for phase encoded (PE) recording (1,600 bits per inch) on half-inch, nine-track tape. Read-after-write verification ensures that each bit written is verified immediately after it is recorded. Vertical parity is checked, character-by-character, when reading and writing. The TA81 uses error correction code (ECC) and cyclic redundancy check (CRC) when in group code recording (GCR) mode to make both single- and double-track error correction without CPU intervention.

TU81-Plus Magnetic Tape Subsystem

The TU81-Plus can store up to 140 Mbytes on a standard 8-Kbyte, 2,400-foot reel. It is the only native-mode industry-compatible tape drive offered for Digital's new VAXBI systems in stand-alone configuration. A 256-Kbyte cache buffer significantly improves tape streaming performance on most VAX systems.

With streaming tape technology and high-speed operation via prefetching of commands and data, the TU81-Plus is ideal for applications involving sustained tape input such as disk backup, data archiving, or recording data from high-speed test equipment. It also uses traditional start/stop technology for shorter data transfers of the type associated with journaling, transaction processing, and classical data processing.

▪ Main Memory Extensions

Main memory for VAX 8200 and VAX 8300 Systems is available in 2-megabyte and 4-megabyte boards to provide easy, cost-effective memory expansion. Each of these boards implements an advanced, highly intelligent design that encompasses data, address, error correcting code, and control logic.

Main memory for the VAX 8500/8550/8700/8800 systems is available in two types of memory boards. One type is a 4-megabyte board; the other is a 16-megabyte board that uses double-sided, surface-mount technology to provide larger memory per size of CPU. The MS86 memory board applies to the VAX 8650 and the MS88 for the VAX 8700/8800 systems. Refer to Table 1-1 for a listing of the maximum capacity of each of the processors discussed. Detailed description of the memory extensions are contained in each processor chapter.

▪ How to Order VAX Systems and VAXcluster Systems

The desired hardware configurations of the standard VAX systems and VAXcluster Systems are obtained by using the system building block menus contained in the current version of the *VAX Systems and Options Catalog*. The menus allow the user to select a basic system consisting of a VAX CPU, main memory, and software operating system license, and to add the required interfaces and devices. From the system menu, the user can select the system storage and load devices, communication interfaces, console terminals and operating system documentation, and software media. Using the system building blocks, VAX systems and VAXcluster configurations can be selected for specific applications without the purchase of unneeded hardware and software. The *VAX Systems and Option Catalog* can be obtained at any Digital sales office or from a Digital sales representative.

Chapter 2 ▪ VAX 8800 and 8700 Processor Systems

The VAX 8800 and VAX 8700 Processor Systems are the highest performance VAX Systems offered by Digital Equipment Corporation. These systems are general purpose, scalar computers suitable for nearly all computing environments. Their very high processor data rates coupled with the VAXBI input/output subsystem provide the highest VAX performance available in nearly all environments. The VAX 8700 can be readily upgraded to a VAX 8800.

The VAX 8800 and 8700 offer the same degree of software compatibility found in other members of the VAX product family. In these processors, a new high-speed internal bus plus integral highly accelerated floating-point operations contribute to overall performance. Both systems incorporate a new generation of input/output architecture—the VAX Bus Interconnect (VAXBI). The VAXBI bus provides the high-performance I/O subsystem. The VAXBI bus incorporates extensive reliability and data integrity features such as bus parity, transmit checking, and receive acknowledge, implemented in VLSI interface circuitry.

Currently, the VAX 8800 offers the highest multistream throughput of any VAX and is faster than any competitive system in its price range. Running multiple applications, the VAX 8800 provides ten to twelve times the performance of the VAX-11/780, while the VAX 8700 provides six times that of a VAX-11/780. Much of the performance is the product of sophisticated, custom, solid-state components, and high-speed bus architectures. The performance characteristics and data for both processors are listed in Appendix A. Some attributes of these systems are:

- Highest-performance VAX systems ever offered.
- Fastest VAX I/O throughput, delivering balanced CPU and I/O performance in all applications.
- Ten to twelve times the performance of the VAX-11/780 in the same 15.5 square feet of floorspace.
- Cost-effective incremental growth with VAXcluster configurations.
- Incremental CPU, I/O, and memory growth.

Figure 2-1 ▪ VAX 8800 Processor Unit

▪ VAX 8800 and VAX 8700 Physical Configuration

VAX 8800 and VAX 8700 processor subsystems occupy the same space as the VAX-11/780 or VAX 8650 processor — 15.5 square feet of floor space. The environmental requirements are the same as those of earlier VAX models so that there is no need to renovate your computer room. Both processors are air-cooled. The clean internal design and airflow patterns contribute to their noticeably low noise level.

The VAX 8800 and VAX 8700 processors are housed in an H9650 cabinet. The cabinet contains the power system, the cooling system, backplane (module card cage), and input/output bulkhead. A front-end cabinet houses the power system input transformer and battery backup unit. Expansion cabinets are available to house more VAXBI buses extending the VAX 8800/8700 Systems support to four VAXBI channels with up to two optional UNIBUS channels. Figure 2-2 shows the cabinet and locations of the components in the cabinet. Physical dimensions of the processors are listed in Appendix A.

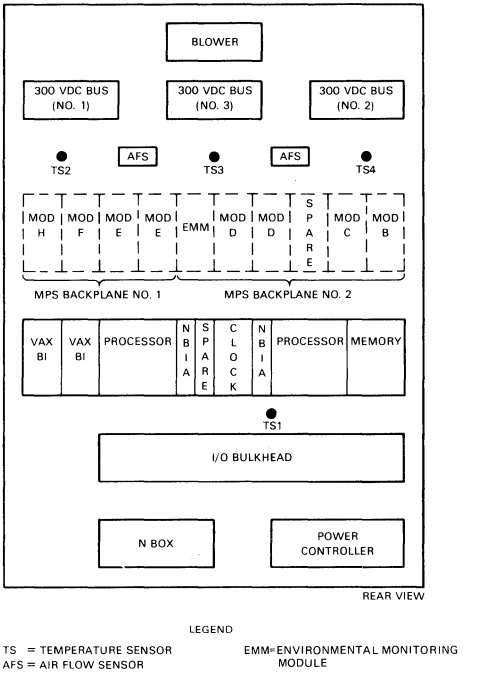

Figure 2-2 ▪ VAX 8800 Processor Configuration

System Expansion Cabinets

The H9652-EC/ED cabinet, shown in Figure 2-3, provides space for any combination of up to two BA32-BA/BB VAXBI expansion boxes or BA11-AW/AX UNIBUS expansion boxes. The cabinet includes 37 panel units.

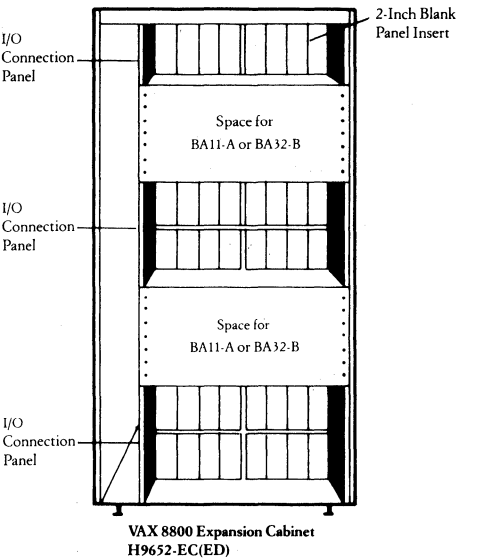

Figure 2-3 ▪ H9652-EC/ED VAXBI and UNIBUS Expansion Cabinet

▪ VAX 8800 and VAX 8700 Processor Organization

The VAX 8700, shown in Figure 2-4, has one processor. The VAX 8800, shown in Figure 2-5, has two processors. The VAX 8800 and VAX 8700 processors share common implementations and functions. In the following descriptions, unless a difference is identified, the implementation is identical for both processors.

A single console subsystem controls either the VAX 8800 or the VAX 8700.

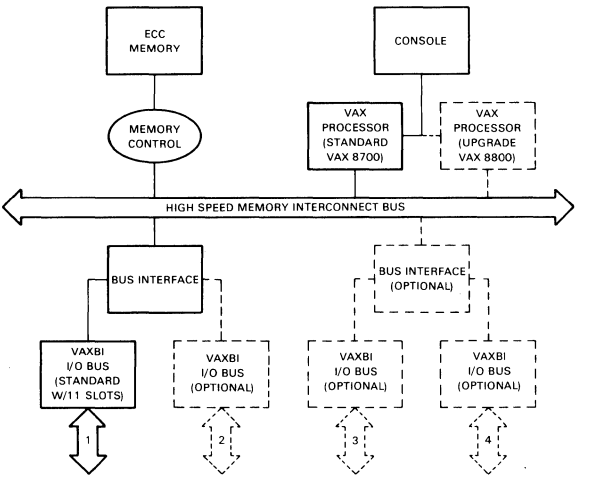

Figure 2-4 ▪ VAX 8700 System Configuration

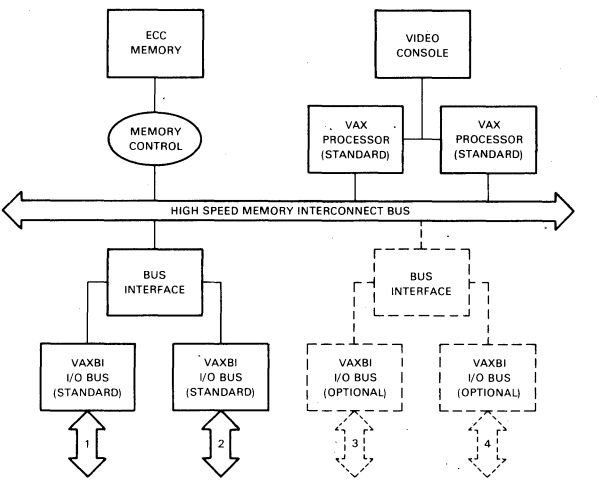

Figure 2-5 ▪ VAX 8800 System Configuration

Console Subsystem

The console subsystem controls the initialization and general operation of the VAX 8800 and VAX 8700 Computer Systems. The *VAX Hardware Handbook Volume 1* contains information that is basic to all VAX Console Subsystems. Please refer to that handbook for general information on VAX console subsystems. See Figure 2-6 for a block diagram of the VAX 8800 and VAX 8700 Console Subsystems.

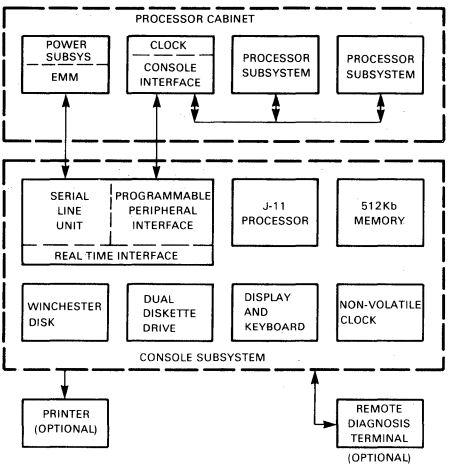

Figure 2-6 ▪ Console Subsystem Block Diagram

- CONSOLE PROCESSOR

  The console processor consists of a J-11 chip-based CPU with a Winchester disk and two diskette drives. Communication between the console processor and the CPUs is done by transferring data to and from the console interface on the clock module. The console processor contains an I/O option called the *Real-time Interface* (RTI). The RTI provides the physical communications path between the console and the console interface. The RTI provides the console device processor with several I/O ports including a programmable peripheral interface (PPI) and two serial-line units (SLU).

  The programmable peripheral interface (PPI) contains three 8-bit ports for transferring data, address, and control signals between the console and its interface. One of the SLUs is connected to the environmental monitoring module (EMM) in the power supply subsystem. The SLU connects the console processor with the EMM giving the console processor the ability to monitor and control the electrical power and environmental parameters of the processor system.

- CONSOLE SUBSYSTEM OPTIONS

  Two options are available for the console subsystem — a printer and a remote diagnostic link. The console processor contains a serial printer port. The remote diagnostic link is a service offered by Digital that permits a 15-minute response by qualified Digital service personnel and allows for remote fault isolation. Contact Digital Field Service for details.

- CONSOLE COMMAND LANGUAGE
  The VAX 8800 and VAX 8700 Console Subsystem uses a superset of the Console Command Language. The *VAX Hardware Handbook Volume 1* contains details of the console command language. Other sources of information on the language are the *VAX 8800/8700/8550/8500 Console User's Guide* and the *VAX 8800/8700 System Hardware User's Guide.*

▪ Central Processing Unit

The VAX 8800 and VAX 8700 processors are logically divided into functional *boxes* that receive power from a power subsystem. The division is logical, not physical: that is, there are no physical barriers such as partitions. Standard Field Service procedures have been developed specifically for these systems.

Each processor consists of three functional units and related buses. The functional units are the instruction (I) box, the execution (E) box, and the cache (C) box. There are five buses in the processor — the cache/ALU bypass bus, the cache data bus, the instruction buffer data bus, the virtual address bus, and the write data bus. Figure 2-7 shows a block diagram of the VAX 8800 and VAX 8700 processor configuration.

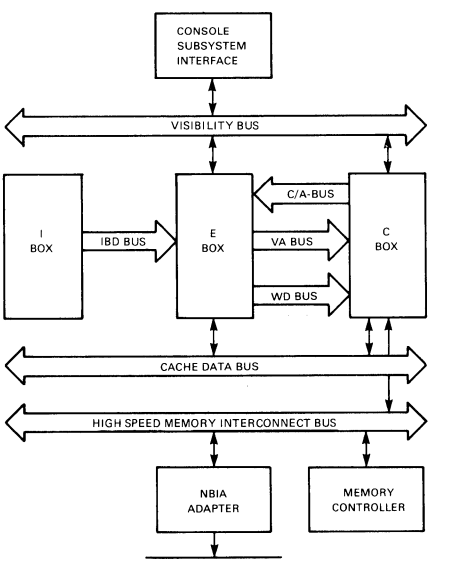

Figure 2-7 ▪ VAX 8800 and VAX 8700 Processor Block Diagram

Instruction Box

The instruction (I) box is the microcode store and control center. It contains the writable control store (WCS), the decoder module, and the microsequencer module. The Ibox

- Buffers the prefetched VAX instruction stream data received from the cache box.
- Decodes and controls microinstruction execution.
- Monitors and services microtraps, interrupts, and exceptions.
- Supplies instruction stream embedded data.
- Provides an interface between the console module and the rest of the processor.

As shown in Figure 2-8, the Ibox contains:

- An instruction buffer.
- An instruction decoder.
- A microsequencer.
- A writable control store.
- Condition code and microbranch logic.
- Interrupt and processor register logic.
- File address generator.
- Console gateway control.

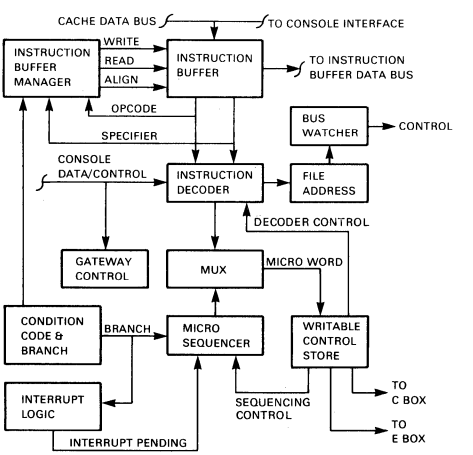

Figure 2-8 ▪ Instruction Box Block Diagram

- INSTRUCTION BUFFER
  The instruction buffer is a 4-longword, short-term memory device. It receives instruction stream data from the cache box and loads the received data into the specified write address. The buffer read/write operations are controlled by the instruction buffer manager. The buffer outputs the opcode byte, the current operand specifier, the general processor register number of the current specifier, and the specifier extension bytes.

- INSTRUCTION DECODER
  The instruction decoder consists of a 4K by 17-bit writable random access memory and a special address encoder. The address encoder is composed of discrete priority encoders and multiplexers. The dynamic RAMs perform three major functions.

  - They supply the microsequencer with part of the entry point address for opcode and specifier microroutines.
  - They assist the instruction buffer manager in controlling the instruction buffer.
  - They indicate which memory data register in the Ebox is to receive the data from memory for those specifiers requesting data.

- MICROSEQUENCER
  The microsequencer determines which one of several sources will supply the address of the next microword to be executed. The 14-bit-wide address is stored in micro-PC latches and is presented to the control store. Possible sources of the next microword to be executed include the following:

  - Next microaddress field possibly modified by branches.
  - Decoder entry point microaddress.
  - Execution or Cbox microtrap vector.
  - Machine check microtrap vector.
  - Trapped micro-PC from a micro-PC silo.
  - Microsubroutine return address from a microstack.
  - Console-supplied address.

- CONTROL STORE
  The microcode control store is a storage area of 16K by 144 bits and resides on a set of 16K by 1-bit writable RAMs. The RAMs are loaded during system initialization from the console subsystem by way of the gateway controller. Approximately 15 Kbits are used for processor control while approximately 1 Kbit is available for user-written code.

- CONDITION CODE AND MACROBRANCH LOGIC
  The condition code and macrobranch logic maintains the processor status word's condition code bits and seven processor state bits. Raw condition codes from various Ebox operations are used in the generation of microbranch conditions based on the raw condition codes and the size of the data being processed. These conditions are tested by the microsequencer's microbranch logic. The raw condition codes can also be compared to the current condition code bits to effect a macrobranch instruction or be stored as the new processor status longword condition code bits.

  The processor state bits are microprogramming aids that provide firmware writers with a method of controlling microcode flow. The bits can be set or cleared in a microroutine. Then the bits may be tested as conditions in later routines.

- INTERRUPT AND PROCESSOR LOGIC
  The interrupt and processor logic contains the priority interrupt hardware and the four internal processor registers. The interrupt portion of the logic monitors all hardware interrupts, encodes the level of the highest pending request, and compares it with the current priority level. If the encoded level is higher than the current level, the interrupt logic requests an interrupt. Interrupts are requested by asserting an interrupt pending signal.

  The internal processor registers control and supply data to the interrupt logic, microsequencer, and the memory management in the cache box.

- FILE ADDRESS GENERATOR
  The file address generator performs the following three functions:

  - It supplies addressing for the Ebox's register and slow data file.
  - It stores general register numbers that are referenced by operand specifiers.
  - It records changes made to the general registers in autoincrement and autodecrement operations.

- GATEWAY CONTROL
  The gateway control logic controls the data paths between the processor and the console interface. It controls the loading of the control store RAMs and micromatch register, and the loading of the decoder and cache control RAMs.

Cache Box

The cache box includes a 64-Kbyte physical indexed, direct mapped, and write-through cache memory. The cache box speeds address translations and provides a communication path for the processor to the memory interconnect bus. The cache box consists of a translation buffer, 64-Kbyte data store, and a memory interconnect interface. Figure 2-9 contains a block diagram of a cache box.

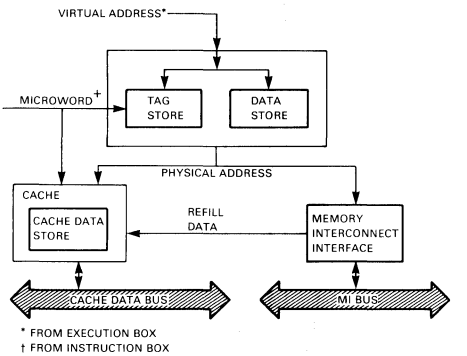

Figure 2-9 ▪ Cache Box Block Diagram

- TRANSLATION BUFFER

  The translation buffer is a 1 Kbyte cache of virtual to physical address translations. The buffer consists of a tag store and data store. The buffer is organized into 512 process translation slots and 512 system region translation slots.

  The tag store uses a portion of the virtual addresses to access a RAM array and compares the contents of the RAM with the remaining virtual address bits. When the comparison results are equal and the translation buffer's valid bit is set, the address is said to have *hit* and the contents of the data store are valid for that address.

  The data store uses a portion of the virtual address. If the tag store comparison results in a translation buffer *hit*, the page frame number concatenated with virtual address bits 0 through 8 is used as the physical address.

- DATA STORE CACHE

  The data store cache is a hardware mechanism that provides fast access to frequently used data. The cache is addressed by a physical address. If required read data is in the cache, that data is extracted and no memory request is required. If the required read data is not in the cache, a memory request for that data is initiated. The data from memory is passed to the requester and is also placed in the cache for subsequent use.

- MEMORY INTERCONNECT INTERFACE

The memory interconnect interface provides the processor(s) with a communications path for control and data signals. When a cache read request *misses*, the interface uses the missed address to build a command/address transaction. The transaction is sent to the memory subsystem. This procedure allows the translation buffer and the cache to be free to process other processor requests until the requested data arrives from memory. When the requested data arrives, the interface assumes control of the cache and loads the new data into the cache's data store.

Execution Box

The execution (E) box receives data from the Ibox and the Cbox, processes the data and returns the data to the Cbox. Figure 2-10 shows a block diagram of the Ebox.

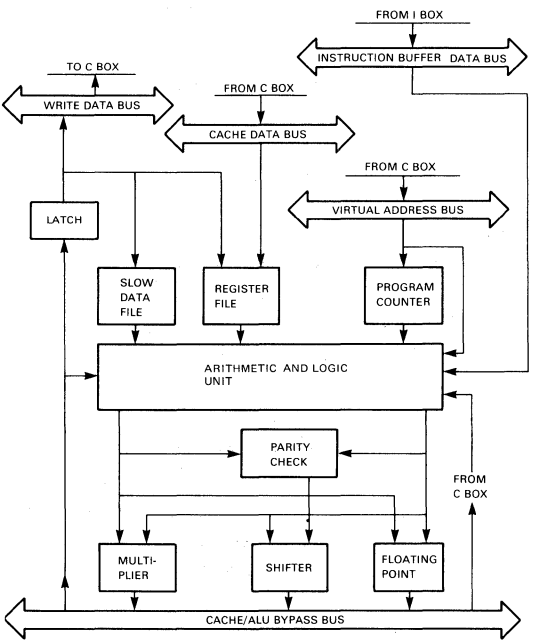

Figure 2-10 ▪ Execution Box Block Diagram

The Ebox

- Performs all processor-required arithmetic, logical, and bit-shift operations.
- Maintains the program counter and general registers.
- Maintains the processor registers.
- Controls data transfers between the Cbox, Ibox, and clock module registers.
- Provides condition code information to the instruction box microsequencer.

The Ebox consists of the following elements:

- A register file
- A data file
- Program counter logic
- Main arithmetic and logic unit
- Shifter
- Floating-point support logic
- Multiplier

The major elements of the Ebox are located on the data slice modules (SLC0 and SLC1) and the shifter module.

- REGISTER FILE
  The register file consists of 32 high-speed 36-bit registers. The registers hold 32 bits of data and 4 parity bits. There are 15 general registers, 9 temporary registers, and 8 memory data registers. The temporary registers serve as microcode scratchpad registers while the memory data registers store the data received from the cache.

- DATA FILE
  The file consists of 256 36-bit registers. The 36-bit registers contain 32 bits of data and 4 parity bits. Data file registers consist of processor registers, data-path constants, and diagnostic test patterns.

- PROGRAM COUNTER
  The program counter maintains the VAX program counter, the program counter incrementer, backup and trap program counters, and the virtual address file register. The program counter components perform the following functions.

- The program counter incrementer updates the program counter by adding an increment value equal to the size of the instruction stream data being processed. The increment value is from 0 to 6 and is supplied by the program counter increment generator in the Ibox.
- The backup program counter saves macroinstruction opcode addresses and restores the program counter if the instruction causes a macro exception. Saving the opcode allows a service routine to examine the opcode of a failing instruction and service the fault.
- The trap program counter maintains a history of recent program counter activity and provides microtrap service routines with the active program counter at the time a microtrap occurs.
- The virtual address file stores a copy of each virtual address sent to the cache. This copy is used as a backup if the address causes a microtrap.

- ARITHMETIC AND LOGIC UNIT
  The arithmetic and logic unit (ALU) is a 32-bit adder. It processes integer, floating-point, binary coded decimal data. The ALU performs addition and subtraction (carries propagated), and logical AND, OR, and Exclusive OR operations. In addition, the ALU
  - Multiplexes data received by the Data Slice Modules.
  - Supplies memory and register data to the cache.
  - Supplies virtual address to the cache translation buffer.
  - Routes data to and from the shift module.
  - Provides carry and condition codes to the instruction box.

- SHIFTER
  The shifter provides additional macro cell array and arithmetic logic unit operators that perform shift/rotate and multiply/divide operations on integer or floating-point data and manipulate the signed exponent of a floating datum. The shifter handles data in all formats in integer, floating-point, and binary-coded decimal modes of operation.

- FLOATING-POINT SUPPORT
  This system processes the sign and exponent fields of floating-point data. Included in the floating-point support logic are the shift count ALU, a priority encoder, and an exponent ALU.

- MULTIPLIER

  The multiplier is a 64-bit multiplier that enhances the speed of both integer and floating-point multiplication. It contains an *8-bit-at-a-time* multiplication algorithm that generates 8 result bits per cycle, and a *1-bit-at-a-time* division algorithm that generates 1 quotient bit per cycle. It also produces or generates the correct *two's complement* results for integer data.

Memory Box

The memory subsystem (M) box consists of a memory control logic module, from one to eight memory array boards, and a memory array bus. See Figure 2-11 for a block diagram of the Mbox with one array board.

The fully sharable 256 Kbyte ECC memory subsystem is suitable for both single and dual processors. Two types of memory array boards provide convenient memory subsystem configuration and easy expansion to a full 128 Mbytes for both the VAX 8800 and the VAX 8700 systems. The 4-Mbyte and 16-Mbyte memory array boards provide easy memory subsystem configuration, expansion, maintenance, and service. The 16-megabyte memory array board uses double-sided, surface-mount technology.

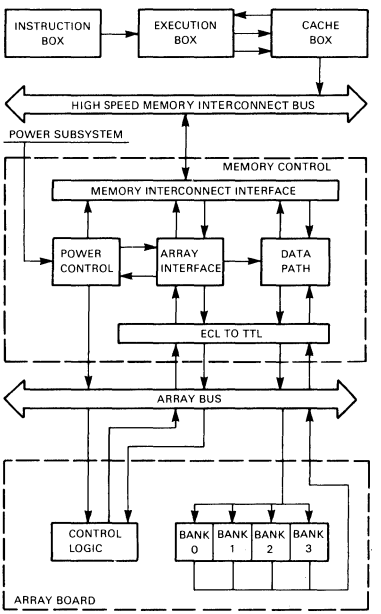

Figure 2-11 ▪ Memory Box Block Diagram

The memory control logic (MCL) module is located in the card cage. The 8-slot backplane can hold eight 4-megabyte memory array boards or eight 16-megabyte memory array boards. Early production (January to November, 1986) VAX 8800/VAX 8700 processors may require field backplane upgrade to reach 128 Mbytes. See the *Systems and Options Catalog* for details.

All VAX 8800 and VAX 8700 memory and memory controllers are shared and usable by system and user programs. Memory, processors, and the I/O subsystem occupy the same cabinet. The large memory provided in these VAX systems accommodates large working sets, many processes, and reduces page faulting.

The memory controller optimizes memory reads and writes with three-way interleaving, further allowing large blocks of data to move freely within the machine. Running at nearly 60 Mbytes per second, the memory interconnect bus ensures that processor-to-memory traffic operates with a minimum of delay or contention. Wait states are minimized and the system is nearly always doing meaningful work. To further protect data, a battery-powered backup power supply for the memory subsystem is a standard feature. It takes 10 minutes to perform a minimum battery backup.

- MEMORY CONTROL LOGIC MODULE
  The memory control logic (MCL) module provides control and a communications interface between the memory interconnect bus and the memory array boards. The single MCL module can control up to eight array boards, and can monitor operations on three arrays simultaneously.

- ARRAY BUS
  The memory array bus, or array bus, performs the transfer of data between the MCL module and the array boards at a data rate of 60 Mbytes a second. The array bus carries board select, command/address signals, and data between the MCL module and the memory arrays. There are separate data lines on the array bus for read data and write data.

- MEMORY ARRAYS
  Two types of memory array boards are available, 4-Mbyte (MS88-AA) and 16-Mbyte (MS88-CA). The MS88-AA memory array board has 156 total dynamic RAMs and 256K by 1 MOS RAMs. The MS88-CA memory array board has 624 total dynamic RAMs (arranged in four banks of 156 dynamic RAMs) for 16 megabytes of data storage. Each dynamic RAM chip has an effective 512 by 512 matrix array providing 256K (262,144) one-bit locations and 4 megabytes by 39 bits of storage. Dynamic RAMs are 150-nanosecond-access-time devices packaged in plastic leadless chip carriers (PLCC).

To achieve the 16-megabyte density, 256K by 1 dynamic RAMS are double-side, surface mounted on 3.3-inch-by-4.8-inch cards and connected to the L-series logic card with 44 pin connectors. These double-sided memory cards are called Standard Memory Units (SMUs). The MS88-CA array contains eight SMU cards. Logic card components include emitter-coupled logic and fast transistor-to-transistor logic devices. The MS88-CA is designed to mix with the MS88-AA array in a VAX 8800 or VAX 8700 backplane in any desired combination.

- DATA PROTECTION

  Data protection is provided in four areas — parity checking, error correction code, error logging, and battery backup.

  ERROR CORRECTION CODE (ECC) - The memory subsystem has 7 check bits for every 32 data bits to provide single-bit error correction and full double-bit error detection. The memory error correction code (ECC) automatically corrects single-bit errors and detects double-bit memory errors. The code also detects greater than double-bit errors if an even number of bits in error are detected. The ECC provides protection from nonrepeating errors by automatically correcting data. Detections and corrections are noted in the error log as a preventive maintenance aid.

  ERROR LOGGING - An integral part of the VMS operating system, error logging software records information related to the state of the system at the time of error. Error logging is useful for the efficient maintenance of hardware by providing a report that can help diagnose impending or persistent hardware problems. Some of the errors that are detected and logged include memory single- and double-bit errors, machine check traps for control store parity error, and cache parity error.

  BATTERY BACKUP MODE - The battery backup unit (BBU) supplies the power system with dc power during an ac power failure. The BBU provides power for the memory modules during short-term power losses. Battery mode is automatically entered when an interruption occurs in normal power. While in battery mode, the object is to save data in the arrays until normal power is restored. Consequently, only refresh cycles are allowed — command operations (writes and reads) are inhibited. To reduce the power drain on the battery, normal refresh sequences are suspended and battery mode refreshes are executed. Battery mode refreshes only the barest minimum of logic thereby making lower power demands on the battery. When normal power returns, the battery mode signals are removed and normal operation is resumed. The battery backup unit is described later in this chapter.

Processor Buses

Seven buses are in the processor subsystem. Two buses participate in controlling or connecting the processor components. The remaining buses are data paths between the processor's components.

- MEMORY INTERCONNECT (MI) BUS

  The high-speed memory interconnect (MI) bus is a synchronous backplane bus that interconnects the major system components of the processor, memory controller, and I/O adapters to provide a path that transfers data between the connected units. The MI bus supports the following functions:

  - Memory read/write operations (allows the processors and I/O adapters to access memory through bus read/write transactions).
    - > Write transactions support longword, masked quadword, and octaword writes).
    - > Read transactions support longword, octaword, and hexword reads.
  - I/O space read/write operations (allows the processors to access memory controller, I/O adapters, and BI I/O device registers through bus read/write transactions.
  - Interrupt handling (transmits interrupt requests generated by the memory controller and I/O adapters to both processors).
  - System initialization (allows the console to initialize all adapters connected to the MI bus).
  - Powerfail warning (provides alternating current low (ACLO) and direct current low (DCLO) signals to all devices connected to the MI bus).

- VISIBILITY BUS

  The visibility bus (V bus) is a slow-speed data bus that allows the console subsystem to access internally latched data in the CPU modules. The V bus has sixteen data lines and two control lines. The console operator can read internally latched data in the processor's modules during the execution of microdiagnostics and during system initialization. The V bus can be used only when the system clocks are stopped. The V bus

  - Monitors the state of the CPU(s) during microdiagnostic execution or in response to commands entered at the console during system debug procedures.
  - Verifies CPU module installation and revision during system initialization.
  - Detects write control store parity errors when loading microcode during system initialization.

Two registers (V bus control and V bus access) located in the clock module console interface allow the console subsystem to control and read the V bus. These registers

- Select the V bus input channel.
- Step the clocks that operate the V bus.
- Send serial V bus addresses to the CPU modules.
- Halt the operation of the V bus address shift register.
- Allow the console to read data from the V bus.

- DATA-PATH BUSES

There are five data-path buses in VAX 8800 and VAX 8700 processors. All five buses provide a data path between the components within the processor. The buses are identified in the following list.

- ALU bypass bus that carries bypass register data scheduled to be written.
- Cache data bus that provides a data path from the cache subsystem to the execution subsystem and instruction parser.
- Instruction buffer data bus that provides a data path for transfer to the execution subsystem. The data is byte, word, longword address displacements, absolute addresses, and immediate data. Branch displacements and literals are also transferred over this bus.
- Virtual address bus transfers virtual addresses from the execution subsystem to the cache subsystem.
- Write data bus transfers write data from the execution subsystem to the cache subsystem.

Power Subsystem

The power subsystem provides the electrical power in proper voltages to operate the processor. The power subsystem is divided into five functional groups—a controller, an Nbox (multifunction power converter assembly) port conditioner, module power supplies, an environmental monitoring module, and a battery backup unit. Figure 2-12 contains a simplified block diagram of the power subsystem.

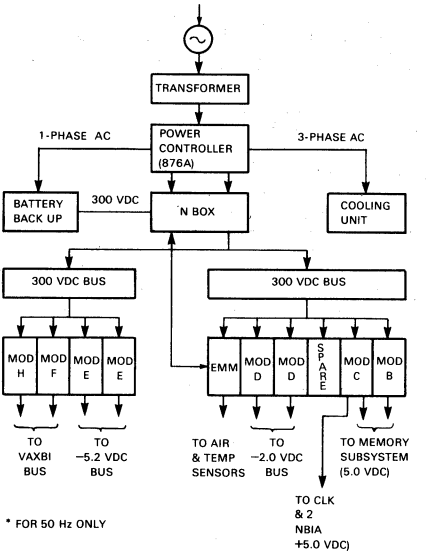

Figure 2-12 ▪ Power Subsystem Block Diagram

- CONTROLLER

  The controller requires input power to be 220-V, 3-phase, and A, B, C rotation sensitive. The controller module receives power from the main circuit breaker and distributes that power to three other modules in the power subsystem and to the air mover module. The output power from the controller module is distributed to four subsystems. The Nbox receives unswitched single-phase and switched three-phase ac power. The battery backup unit receives unswitched, single-phase, *country* power. The console subsystem receives unswitched single-phase 120 Vac. The air mover subsystem receives three-phase unswitched 120 Vac.

- POWER CONDITIONING (NBOX)

  The Nbox is a multifunction power converter assembly having five sections. Two sections convert three-phase 208 Vac power into 300 Vdc. An Interface Logic Module provides a logic signal interface for the environmental monitoring module and other power system components and controls battery backup operation. A control and startup power module converts single-phase 120 Vac to logic-level dc voltages and supplies the interface logic and environmental monitoring modules. A new box translator module converts logic signals for startup and initialization procedures.

- MODULAR POWER SUPPLIES
  The modular power supplies (MPS) consist of a group of dc power modules and a backplane. The modular power supplies regulate dc power for the CPU, memory subsystem, and I/O adapter modules. They are housed in the processor cabinet above their respective card cages.

- ENVIRONMENTAL MONITORING MODULE
  The environmental monitoring module (EMM) is a microprocessor-based, dual-function device. Its first function is to monitor the power, temperature, and airflow conditions within the processor cabinet reporting through the console subsystem. Its second function is to protect the system from damage from extremes in environmental conditions. The EMM responds to console subsystem commands during powerup and powerdown sequencing, initialization, and battery backup operations. The EMM also responds to the console subsystem during normal operation when it is routinely polled from the console. The EMM forces emergency shutdown outside of programmable limits.

- BATTERY BACKUP UNIT
  The battery backup unit (BBU) provides the power subsystem with 300 Vdc during utility ac-power outages. It can supply the dc power for memory refresh for a minimum of 9 minutes with 32 megabytes of memory composed of eight 4-megabyte arrays. It also supplies power for 128 megabyte arrays. The unit contains a 48-volt battery pack, a charging circuit, and a dc-to-dc converter.

Clock Subsystem

The clock subsystem generates, controls, and distributes timing signals to all the components of the processor system. The clock contains a console subsystem interface, an oscillator, a phase generator, clock control logic circuits, and clock signal distribution logic circuits. Figure 2-13 illustrates the clock subsystem and the signals it generates.

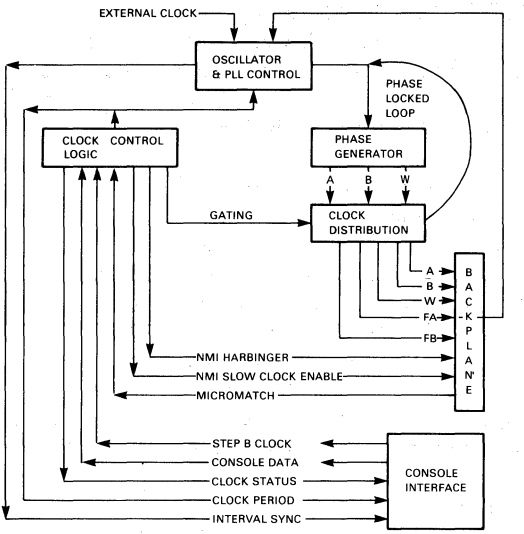

Figure 2-13 ▪ Clock Subsystem Block Diagram

The oscillator is the basic source of timing for the clock subsystem. It generates a reference signal that is sent to and used by the phase generator to produce two nonoverlapping clock phases.

Clock generation logic is controlled by the console subsystem with operator-initiated commands. Three registers in the clock logic are used for control of the system clocks by the console. A fourth register provides status information for the console operator. The clock control, clock period, and burst count registers control the clock. The timeout and status register provides the status information. The clock subsystem is controlled from the console. Using console commands, you can perform

- Start and stop the clocks.
- Burst the clocks; that is, cycle the clocks on and off for a specified number of cycles.
- Single-step the clocks; that is, increment instructions in bursts of one cycle.
- Enable a *clock stop* operation on a micromatch.
- Enable a *clock trap* operation on a micromatch.
- Change the clock period.
- Disable clock stalls.
- Control the timeout clock (MI Slow Clock Enable).

Input/Output System

The I/O subsystem communicates with devices outside the processor. Typical devices include disk and tape drives, printers, terminals, communications devices, and VAXcluster interconnects. The bus that handles I/O for the VAX 8800 and VAX 8700 processors is the VAX Bus Interconnect (VAXBI).

- VAX BUS INTERCONNECT

  The VAX Bus Interconnect (VAXBI) is a 32-bit synchronous bus that serves as the I/O bus for the processor system. VAXBI buses are connected to the processor system through MI-to-BI adapters as shown in Figure 2-14.

  The DB88 adapter serves as an interface between the memory interconnect (MI) and VAXBI bus. It is the I/O path to mass storage devices, Digital networks, communications devices, and other peripherals.

  DB88 includes a minimum of 1 NBIA module, 1 NBIB module, and two cables. The NBIA, an extended hex module mounted in the CPU backplane, contains the memory interconnect port and DB88 transaction buffers. The NBIB module, located in the VAXBI backplane, contains two VAXBI user ports. The MI port communicates directly with the MI bus. The VAXBI user ports communciate with the VAXBI bus.

  VAX 8800 and VAX 8700 systems can be configured with up to 4 VAXBI channels. See the *VAX Systems and Options Catalog* and *VAXBI Options Handbook* for configuration details.

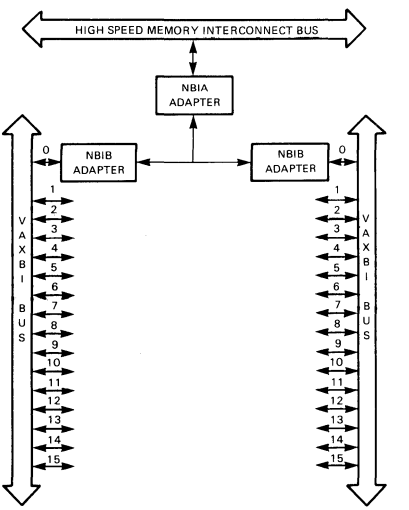

Figure 2-14 ▪ I/O Bus Block Diagram

Note

In Figure 2-14 (above), the NBIB adapter is shown installed at VAXBI Node Address 0. The drawing depicts a typical location. The NBIB adapter may be installed at any location with one exception. If a DWBUA UNIBUS adapter is in the configuration, it must be installed at VAXBI Node Address 0.

The VAXBI bus supports up to 16 VAXBI nodes with each adapter having a unique node identification value from 0 through 15. Node identification is determined by an identification plug that is inserted in the backplane. The VAXBI bus supports

- Memory read/write operations (allows direct memory access (DMA) transfers between an I/O device on the VAXBI bus and the memory subsystem through bus read/write transactions).
- I/O register read/write operations (allows the processors to access the I/O registers in I/O devices on the VAXBI bus through I/O space read/write transactions originated by the processors).
- Interrupt handling (enables I/O devices on the VAXBI bus to interrupt the processors through bus *interrupt* transactions directed to the NBIB node).
- System synchronization (provides NBI-generated clock signals to all nodes connected to the VAXBI bus).
- System initialization or reset (allows nodes to assert a reset line and initialize a simulated VAXBI bus powerfail sequence. Also halts and reboots both processors).
- Powerfail warning (provides alternating current low (ACLO) and direct current low (DCLO) signals to all VAXBI nodes).

- VAXBI BUS ADAPTERS

  Numerous types of adapters are available to connect a variety of devices to the VAXBI bus. Adapters are available to connect new devices as well as existing devices to the VAXBI bus. A VAXBI adapter to Digital's UNIBUS also exists. With appropriate adapters, the VAXBI bus can support existing and future peripheral equipment made by Digital.

  For details on the adapters and for configuration guidelines, refer to the current *VAX Systems and Options Catalog*. Technical description are given in the *VAXBI Options Handbook*.

▪ Mass-storage Subsystems

The mass-storage subsystems for VAX 8800 and VAX 8700 Computer Systems are varied. The KDB50 disk controller for the VAXBI is described briefly in Chapter 7 of this handbook and in the *VAXBI Options Handbook*.

▪ Reliability, Availability, and Maintainability

The VAX 8800 and VAX 8700 Systems have an enhanced Reliability, Availability, and Maintainability Program (RAMP) and diagnostic features in addition to the other VAX family features. The new features include:

- Environmental and power monitors (EMM) to protect the system should temperatures or power levels exceed safe limits.
- Automatic verification of hardware, firmware, and software revision compatibility.
- Electrically keyed modules and module slots. Different modules have different power requirements (voltages) at different contacts. The keys prevent improper installation and the possibility of applying a voltage that can damage the circuitry.
- System is reconfigurable to one CPU if the other CPU fails (VAX 8800 Processor Systems only).
- Automatic electrostatic discharge (ESD) provision to protect modules during installation.

Existing features in the VAX family of processors are:

- Error correction code (ECC) on main memory.
- Parity checking on internal RAMs.
- Memory Interconnect bus protocol checking, bus silo, and parity.
- Timing and voltage margining.
- Remote diagnostics package.

Reliability

Both processor subsystems are designed for high reliability through the maximum use of highly integrated semiconductor devices, a 22-layer printed circuit backplane, zero-insertion-force (ZIF) connectors, and nine-layer printed circuit logic modules. Extensive parity and data integrity protection has been implemented throughout the system. The remote diagnostics capability, extensive integral diagnostics, and high-reliability components all contribute to Digital's ability to offer a 12-month warranty on the CPU kernel. The VAXBI bus also enhances system reliability with its error detection and error logging logic.

Availability

Both the VAX 8800 and VAX 8700 Systems contain high availability features. System powerup, diagnostics, monitoring and control are performed efficiently by way of a realtime interface to the processor subsystem. An environmental monitoring module (EMM) constantly monitors temperatures and voltages throughout the processor subsystem. The EMM subsystem constantly reports status and conditions on the console.

Maintainability

The console subsystem contains a remote diagnostic port. The port allows an operator at a Digital Diagnostic Center to connect the malfunctioning system to a diagnostics engine at the center. Within seconds after the connection, the malfunctioning system is tested and a report made. All printed circuit boards are installed with zero-insertion-force connectors. This affords safe and easy removal of malfunctioning boards while maintaining installed signal integrity.

Chapter 3 ▪ VAX 8650 Processor

The VAX 8650 (Figure 3-1) is a high-performance system that provides the speed and power needed for single and multiuser large scale processing applications. Its high-performance mainframe computing is 44 percent faster than that of the powerful VAX 8600 system. If you already use VAX systems, all of your investments in equipment, training, and software are protected.

Conforming to the VAX architecture, the VAX 8650 processor is compatible with all other VAX processors. It supports the VMS operating system with its associated layered software products, and the ULTRIX-32 operating system.

Ideal for extensive scientific, engineering, and realtime applications — including artificial intelligence, simulation, and computer-aided design — the VAX 8650 also provides the I/O capacity for large timesharing applications in government, commercial, administrative, and academic environments.

The VAX 8650 processor incorporates customized emitter-coupled (ECL) gate-array logic and four-stage instruction pipeline processing. The customized ECL logic allows more components to be included on a module and provides a significant increase in processing speed. The pipeline processing of instructions enables the processor to operate on several instructions simultaneously, thereby reducing the number of cycles required for each instruction. The 16-kilobyte cache is a writeback memory used to decrease the access time of memory references.

The VAX 8650 processor includes virtual memory management; a bootstrap loader; standard instructions for packed decimal, floating point data types, and fixed-point arithmetic; and character and string manipulations. Also included are the 16-kilobyte write-back cache memory, high-precision realtime programmable clock, time-of-year clock with battery backup, and 8 kilowords (86-bit words) of writable control store.

The VAX 8650 processor includes a synchronous backplane interconnect (SBI) adapter. A second SBI adapter can be added to expand the I/O capabilities of the system. The communications path between the processor and main memory is through an internal memory bus, which effectively decreases the memory access time. The SBI is used only for communications between devices and memory and therefore the speed and efficiency of the I/O transfers are increased.

Some of the features and benefits of the VAX 8650 systems are:

- High-performance mainframe computing — 6 times the performance of the VAX-11/780.
- Up to 68 Mbytes of memory for large applications.
- Large-system CPU performance for VAXcluster Systems.
- Easy upgrade from the VAX 8600 system with the VAX 8650 Upgrade Kit.
- Proven, high-speed throughput in scientific and technical applications.
- Increased performance and reliability through customized emitter-coupled (ECL) gate-array logic and four-stage instruction pipeline processing.

Refer to Appendix A for performance specifications and related data for the VAX 8650 processors. For positioning relative to other systems, see the comparison chart (Table 1-1).

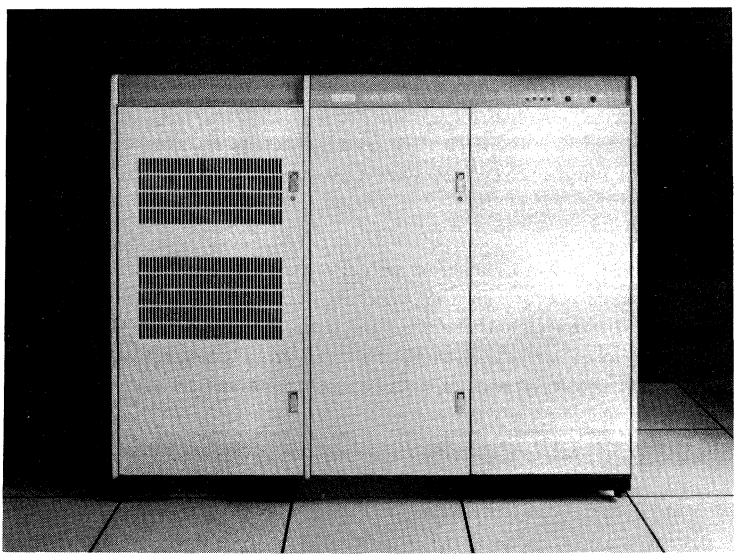

Figure 3-1 ▪ The VAX 8650 Processor

▪ VAX 8650 Physical Configuration

The VAX 8650 processor and console, shown in Figure 3-2, are contained in a CPU cabinet and an attached front-end cabinet. The CPU cabinet contains the processor, console logic, floating-point accelerator, space for up to 68 megabytes of main memory, an SBI adapter bus backplane, and an I/O adapter backplane. The modular power supplies, regulators, and power distribution network are above the logic area.

At the bottom of the CPU cabinet is the power control unit, which receives the system line power and the battery backup unit that supplies power to the memory in the event of a power failure. A blower unit at the top of the cabinet provides cooling for the power supplies and logic modules. The switches and indicators that monitor and control the system operation are on the panel at the top of the CPU cabinet. The signal cables between the cabinets and the communication and storage devices connect to I/O connector panels located at the rear of the cabinets. The connector panels have plates that can be removed to mount cable connectors.

The front-end cabinet includes the RL02 disk drive (a 10.4-megabyte, removable media, console load device), a UNIBUS backplane mounted in a BA11-A box for communication devices, and a step-down power transformer that is supplied when 50-hertz main power is used. The step-down transformer has voltage taps to ensure line power compatibility.

A UNIBUS expansion cabinet can be added to expand the system UNIBUS. A synchronous backplane interconnect (SBI) expansion cabinet can be added to extend the SBI interface, which is included in the main cabinet, and two SBI expansion cabinets can added when a second SBI adapter is used.

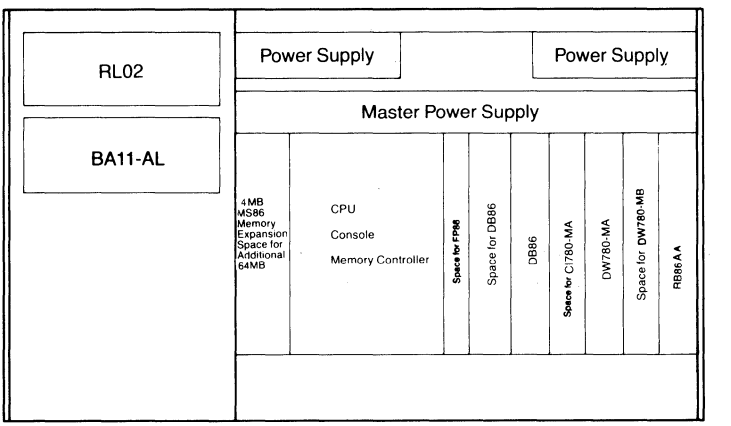

Figure 3-2 ▪ VAX 8650 Processor Configuration

System Expansion Cabinets

The expansion cabinets are available for mounting additional UNIBUS interfaces and for mounting a second SBI adapter. The H9652-F series of UNIBUS expansion cabinets is shown in Figure 3-3. The H9652-FA (-FB) cabinet includes a BA11-A mounting box and provides space for adding a second BA11-A mounting box. The H9652-FC (-FD) cabinet includes two BA11-A mounting boxes. No expansion boxes are mounted in the H9652-FE(-FF) cabinet. The BA11-A box contains a power supply and allows installation of DD11-CK (four-slot) and DD11-DK (nine-slot) for a total of six system units. Forty option panel spaces are available at the rear of the cabinets for mounting the I/O device connectors.

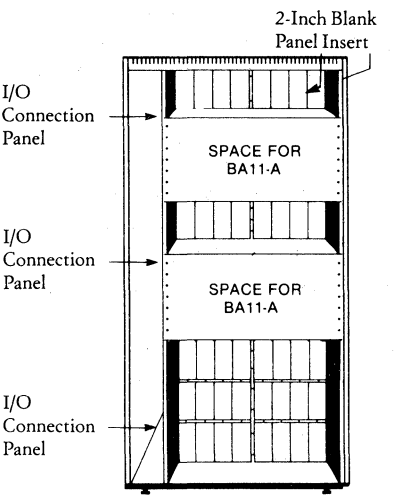

Figure 3-3 ▪ UNIBUS Expansion Cabinet Configuration

The H9652-CA (-CB) is a SBI expansion cabinet and is shown in Figure 3-4. The SBI expansion cabinet contains an SBI backplane and power supply. It provides four option panel spaces and space for an additional power supply.

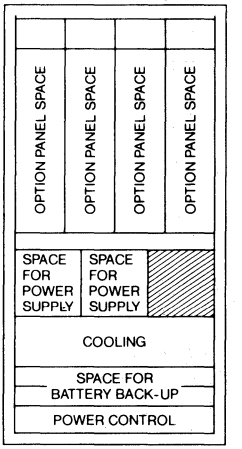

Figure 3-4 ▪ SBI Expansion Cabinet Configuration

▪ VAX 8650 Processor Organization

The functional organization and bus structure of the VAX 8650 processor are shown in Figure 3-5. The processor contains four main logic subsystem blocks: the instruction execution logic (Ebox), the instruction/data fetch logic (Ibox), and the memory control logic (Mbox), and the floating-point accelerator logic (Fbox). A system of internal buses form the address, data, and control signal paths within the CPU logic. The console subsystem connects to the Ibox through the C bus. The synchronous backplane adapter connects to the Mbox and provides the SBI bus for communication with the external devices.

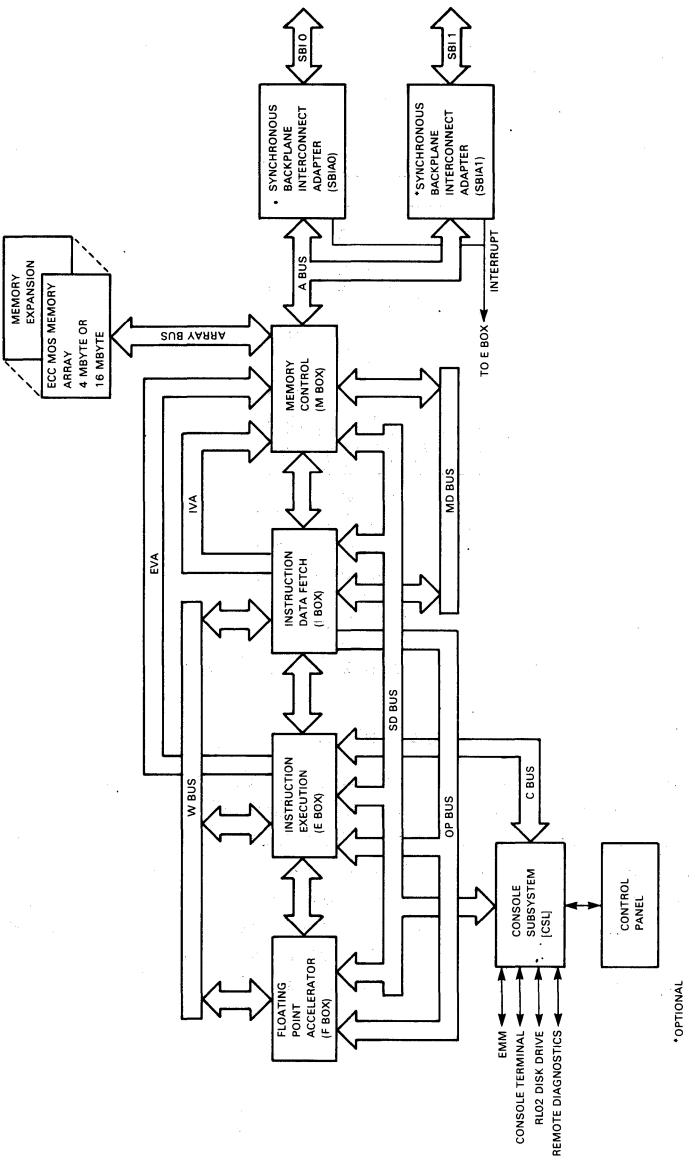

Figure 3-5 ▪ VAX 8650 Processor Components

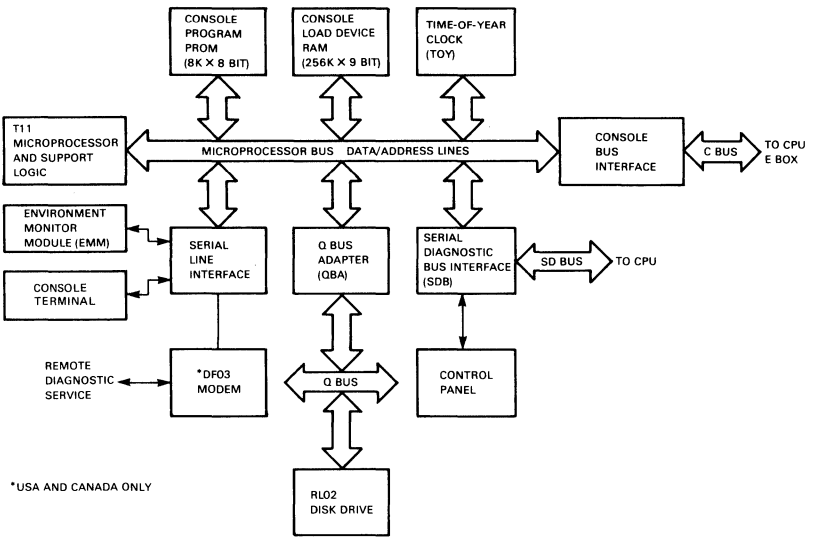

Figure 3-6 ▪ VAX 8650 Console Subsystem Components

Console Subsystem

The VAX 8650 console subsystem is a programmed interface between the VAX 8650 processor and the console terminal, console disk drive, remote diagnostic port, and the system environmental monitoring module. See Figure 3-6. The console subsystem is controlled by a T-11 microprocessor that supports a subset of the LSI-11 instructions. The console subsystem includes a 256-kilobyte, parity-assisted dynamic RAM, an 8-kilobyte PROM, three programmable serial-line interfaces and a time-of-year (TOY) clock. The three serial-line interfaces transmit information to and receive information from the console terminal, remote diagnostic line, and environmental monitoring module (EMM).

Note

The VAX 8650 console subsystem is the same as the VAX 8600 console subsystem. Differences between the systems are noted here.

The console software resides in the 256-kilobyte RAM and the 8-kilobyte PROM. The 8-kilobyte PROM stores the program executed by the T-11 during the powerup sequence. This program self-tests the microprocessor, performs hardware initialization, and loads the console software into the 256-kilobyte RAM from the console load device. The console software includes the diagnostic console program (DCON), macrocode control program (MCP), and the diagnostic control program (DC).

The console subsystem

- Includes a system clock control and time-of-year clock with battery backup.
- Performs the system power sequences and monitors the system environment.
- Includes EIA-compatible, serial-line interfaces for the console terminal, remote diagnostic port, and environment monitoring module.
- Includes the system and processor diagnostics programs.
- Provides memory storage for bootstrap and diagnostic programs.
- Provides self-diagnostic testing during system initialization.
- Includes powerup configuration programming.

In addition to the standard capabilities provided by all VAX processor subsystems, the VAX 8650 console subsystem provides local diagnostic testing in the diagnostic control mode, a mode to test the microcode, and a debug-trace test facility.

For detailed information on the VAX 8650 console subsystem, refer to the *VAX Hardware Handbook Volume 1–1986*.

▪ Central Processing Unit

The main logic elements in the CPU are the instruction/data fetch (Ibox), the instruction execution (Ebox), the memory control (Mbox), and the floating-point accelerator (Fbox). Each element contains a copy of the sixteen general-purpose registers to ensure immediate access to the general-purpose register data and system status information. See Figure 3-7 for the VAX 8650 System Configuration and the current *VAX Systems and Options Catalog* for configuration requirements.

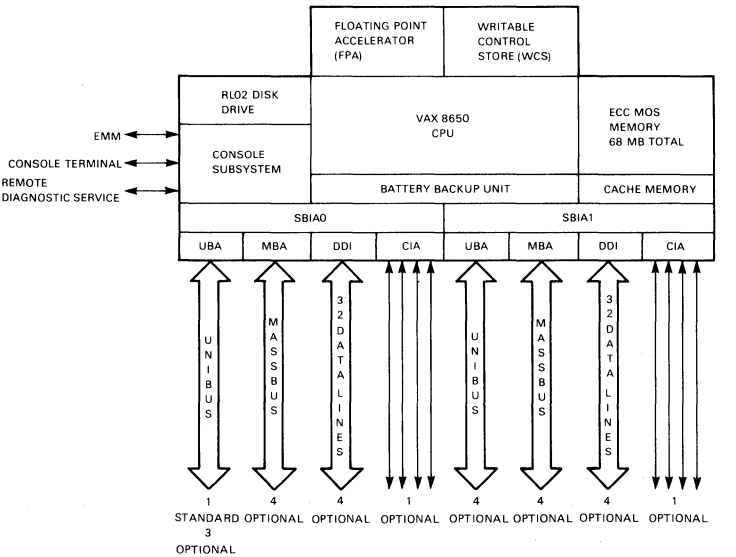

Figure 3-7 ▪ VAX 8650 System Hardware Configuration

Instruction Box Functions

The instruction box (Ibox), consisting of the instruction and data prefetch logic, is the interface between the Ebox and Fbox execution units and memory. It contains the following logic functions:

- 8-byte FIFO instruction buffer
- Dispatch RAM
- Memory data path
- Control store RAM
- General purpose register file and an R-log file
- Address and memory data path
- Write latch

All data transfers to and from the execution logic is through the Ibox, which receives the instruction stream of bytes from memory. From the memory information, the Ibox determines the information to retrieve and the activity to initiate in the Ebox. The Ibox performs the first three stages of the four stages required for instruction execution. It prefetches the instruction stream, decodes the instruction opcodes and specifiers, calculates the required address, fetches the operands, and initiates the read and write cycles. The execution of the instruction is then performed by the Ebox or the Fbox while the Ibox begins processing the next instruction.

The instruction buffer is an 8-byte buffer that stores a copy of the bytes fetched from memory. The primary function of the buffer and its associated logic is to prefetch instruction stream bytes and to align them contiguously. More than one instruction is usually contained in the instruction buffer; therefore, the next opcode and specifier will be available when the current instruction is completed. It also is used to fetch and align decimal-string operands.

The dispatch RAM contains a table of dispatch addresses for every macroinstruction and provides control information to the Ibox and address data paths. The address data path and associated control logic perform address calculations and branch displacements, and controls the start of the instruction buffer. Using the opcode in the instruction buffer as an address, the dispatch RAM sends a dispatch address to the Ebox control store.

The memory data path logic controls the data transferred between the Mbox and the Ibox. The data is aligned by a rotator in the data path before transfer to the execution units or to the instruction buffer.

The Ibox control store is a 256-bit by 52-bit RAM that processes the operand specifiers and branch instructions, updates the register (R-log) file, responds to specific Ebox commands and master reset, and assists in performing the microdiagnostics.

The general purpose register file contains the same information that is stored in the general purpose register files of the Mbox and Fbox. The file provides accessibility to the register data for addressing modes.

The R-log file stores the register information that may change during the instruction execution. The typical information stored in the R-log can be the current program counter values, the general purpose register address, the amount of change to a register, and whether the change was added to or subtracted from the register. This information is required during memory management faults to return the processor to the state prior to the condition that caused the fault.

The address data path performs address calculations and branch displacements, and initializes the IBUF. It also provides a backup file for the general purpose register and macro-level diagnostics.

A write latch is used to align the data and to store the resulting data from the Ebox and Fbox to be written to cache memory.

Execution Box Functions

The execution box performs logical, arithmetic, and other operations required to execute the instruction. The results are then transferred to the Ibox through the W bus, to be written into memory when required. The Ebox controls the system operation during system initialization and during console mode functions by executing the VAX instruction set and by processing both external and internal interrupts and exceptions. The Ebox includes the following logic elements:

- Data path logic
- Control store RAM
- Microsequencer logic
- Console interface
- Maintenance logic

The data-path logic includes a 32-bit binary arithmetic logic unit (ALU), shifter and data packer/unpacker logic, two scratchpad locations that contain copies of the general purpose registers, a virtual memory queue register, and a W bus register. The ALU performs arithmetic and logical operations and provides special functions to decrease the processing time for division, decimal arithmetic, and compare operations. The shifter and data/packer logic is used to pack and unpack floating-point data, to translate decimal data formats, to shift and rotate arithmetic data, and to perform other bit manipulations.

When an external interrupt and internal interrupt occur simultaneously, the internal request is processed first. External interrupts, sampled from the I/O adapters and received by the SBI adapters, are sent to the Ebox. The Ebox scans the SBI adapters to determine the highest priority request pending for each interrupt source. The internal interrupts are received from the console terminal, from the Mbox, and internally from the Ebox. Information is written into the control store RAM when the Ebox clocks are disabled or stalled. The microsequencer logic accesses the RAM in response to console operations and microprogram subroutines, traps, stalls, and subroutines. The console interface provides the path to initialize the control store during the program loading and startup sequence. It also allows the console to enable or disable the maintenance logic and to correct errors.

The control store is an 8-kilobit by 92-bit RAM that receives information when the Ebox clocks are stalled or disabled. The microsequencer accesses the control store information in response to microprogram control, instruction dependent dispatching, microprogram subroutines, microtraps, machine stalls, console operations, and microstore-related error conditions. The control store is initialized by the console interface during a system cold start and allows the console to enable or disable the maintenance logic and perform error correction operations. The maintenance functions are implemented through the clock logic hardware, console software, and the Ebox microword.

The Ebox control consists of context logic, memory port logic, and abort logic. The context logic generates data size information for the Ebox data path and references for the Ebox memory port and controls W bus transactions. The memory port logic performs functions associated with issuing and requeuing memory commands that are used for branch conditioning and memory management microcode. The Ebox initiates microtraps and creates microtrap vectors from the status information received from the Mbox. Abort logic cancels nonrecoverable operations caused by errors that are detected but do not result in a stall condition. Errors are recovered through the fault process and the processor is returned to the beginning of the microinstruction. The stall logic determines if an input or output stall condition exists in the Ebox microcycle.

The Ebox contains interrupt logic to process internal and external interrupt requests and to determine their priority. The internal interrupts are generated by the console subsystem, the Ebox, and the Mbox. The external interrupts are sampled from the I/O adapters through the A bus.

The Ebox contains two dual-ported scratchpad memories, each consisting of 256 32-bit registers. The scratchpad memories are used as internal temporary storage for the microcode and to store copies of the general purpose registers and constants. They are also used by the memory management and operation system.

A virtual-memory queue register provides physical and virtual addresses to the Mbox. The W bus registers are accessed by microcode through the W bus.

The maintenance functions are implemented through the clock logic hardware, console software, and the memory array modules and I/O adapters.

Floating-point Accelerator Functions

The floating-point accelerator (Fbox) decreases the time to perform floating-point instructions and some integer instructions. The Fbox logic contains 16 general purpose registers, and adder and multiplier logic.

Operands received from the adder are multiplied by the multiplier logic and the product is returned to the adder for rounding and normalization. During floating-point operations, the multiplier operates on the fractions and the adder operates on the exponent. During integer operations the entire two's complement number is multiplied.

The adder logic performs addition, subtraction, and division and handles the exponents for all the basic operations. The adder contains the logic to unpack the floating-point numbers, to align fractions, and to round and normalize the results. The operands are received from the OP bus and returned to the W bus. The Fbox receives general purpose register updates and Ebox data, and accesses some Fbox registers through the W bus.

Memory Controller Functions

The memory controller (Mbox) contains the logic for controlling memory operations and for communicating with the I/O subsystems and devices. The main logic elements of the Mbox are:

- 16-kilobyte cache memory.
- 512-location translation buffer.
- Error detection and correction logic.
- Port control logic.
- Memory arrays.
- Mbox control store.

The Mbox is the interface to the main memory arrays, to the SBI adapters, to the Ibox, and to the Ebox and Fbox. The Mbox connects to the memory through the memory array bus and to the SBI adapter through the A bus. Its function is to store memory write data and to supply memory read data in response to requests by the Ebox and Ibox and in response to direct memory access (DMA) requests. It also stores I/O write data and supplies I/O read data in response to requests by the Ebox. During DMA requests from an SBI adapter, the Mbox stores memory write data and supplies memory read data to the SBI. The virtual-to-physical address translation is performed by the translation buffer. The physical address memory mapping (PAMM) selects memory array modules and I/O adapters being accessed and is enabled by the PAMM logic in the Mbox. The cache memory provides fast access to the memory data.

The translation buffer is a 512-location cache memory used for storing 256 system-page-table entries and 256 process-page-table entries. During Ebox and Ibox references, the translation buffer is used to decrease the virtual-to-physical translation process. During normal operation the translation buffer is loaded from the page tables in memory by the microcode; during diagnostic operations, loading is through the SD bus.

The PAMM is a 1-kilobit by 5-bit RAM that maps the physical address space and is addressed by the high-order bits of the physical address. The output is decoded and used to select the array slot or I/O adapter being accessed. The PAMM is loaded during the system initialization through the SD bus and by system-level programs.

The 16-kilobyte cache is a writeback memory used to decrease the access time of memory references. The cache is arranged in two groups of 8 kilobytes each and provides byte parity and error correction code (ECC) on each longword.

The Mbox control store is a 256-bit by 80-bit RAM that controls the Mbox operations including port read and write functions, error recovery, cache refill and writeback operations, A bus transactions, register read and write operations, and the diagnostic functions. The control store is loaded from the SD bus during system initialization.

The port control logic provides arbitration during instruction operand fetching of the Ibox and read and write operations by the Ebox. The control functions of the Mbox include special byte-write logic that decreases the time to insert the bytes into longwords. It also includes the memory refresh logic for the 256-kilobyte MOS RAM integrated circuits in the memory array.

Each memory array module contains 4 megabytes of error correction code (ECC) MOS memory storage and the timing and control logic to refresh memory when the main power to the system fails. During read operations, the physical address from the memory controller is sent to an array together with a start command. The array loads four longwords with ECC from memory into a shift register/bus transceiver. The memory controller then shifts the data, one longword for each cycle, from the register to the A bus. The memory controller performs error correction on each longword it receives. During write operations, the memory controller sends the address and data to the array through the A bus. The data is loaded to the shift register on the memory array and the memory controller issues a start command to write the data in memory. The memory controller can then initiate a cycle in another array while the data is being written.

Synchronous Backplane Interconnect Functions

The synchronous backplane interconnect adapter (SBI adapter) is the interface between the SBI bus and the A bus. The SBI adapter provides the functions required to control MASSBUS and UNIBUS I/O operations. It establishes the protocol, provides the timing, and assembles the data for transmission in either direction. The SBI adapter contains the following logic elements:

- Buffer control and A bus logic
- Register file
- Clock logic
- SBI bus interface
- Interrupt control logic
- Data latches

The SBI adapter provides the processor and memory nexus functions to the SBI bus and generates the SBI clock signals. The nexus is a physical connection to the SBI bus. Command and address data are exchanged between the SBI adapter and the Mbox through the A bus. Interrupt information and interrupt polling are exchanged between the SBI adapter and the Ebox. The A bus and buffer control logic control the reading and writing of the SBI adapter register files, notify the Mbox when CPU or SBI adapter transactions occur, receive and buffer the timing signals for the A bus synchronous logic, and notify the Ebox when an interrupt condition is detected.

The register file stores the I/O data transferred through the SBI adapter. It is a dual-port 16-line by 32-bit register that operates synchronously with both the A bus and the SBI bus.

The interrupt logic notifies the CPU of errors detected during DMA transactions, fault conditions detected on the SBI bus, and programmed maintenance procedures. It also passes interrupt requests from SBI devices to the CPU.

The clock logic generates the timing signals for the SBI operations.

Data latches are used to hold or convert information transferred to or from the SBI bus. Information from the SBI bus is converted to the A bus format. The SBI adapter contains 35 registers that are accessed through the CPU transaction buffer. The registers are used to condition the SBI adapter during bootstrap operations, to record error information, to store vector addresses during the servicing of interrupts, and to establish maintenance and diagnostic functions.

The SBI bus interface logic samples the data transfer lines of the SBI during each cycle and transfers the results to the SBI bus protocol logic and to the data latches. It also transmits information to the SBI bus from the data latches. The SBI adapter protocol logic provides protocol checking and verifies the commands and data received by the SBI adapter.

Cache Memory

The cache memory provides the central processor with high-speed data access by storing frequently referenced addresses, data, and instruction items in the secondary memory. The cache memory significantly reduces the processor's effective memory access time. The cache memory in some of the VAX systems includes an instruction buffer that enables the processor to fetch and decode the next instruction while the current instruction completes execution.

An address translation buffer also is used to eliminate extra memory accesses during virtual-to-physical address translations. The buffer contains frequently used address translations.

Environmental Monitoring Module

The VAX 8650 processor includes a microprocessor-controlled environmental monitoring module (EMM) in the modular power supply area of the cabinet. The module samples and controls the environmental conditions in the processor and optional system cabinets. The module monitors and controls the dc regulator voltages and checks the regulator error status. It also monitors the cabinet air flow, cabinet air temperatures, and ac ground currents for excessive current flow. The functions of the EMM are monitored and controlled by console commands from the console subsystem. By controlling the dc regulator voltages from the console terminal, marginal voltage conditions can be established to help detect intermittent logic errors. For details of the operation of this module refer to the *VAX Hardware Handbook Volume 1–1986*.

Main Memory

VAX 8650 processors offer a choice of two high-reliability main memory arrays, a 4-megabyte (MS86-AA) array and the new 16-megabyte (MS86-CA) array. Both arrays can be used on the same system at the same time. The VAX 8650 uses a total of ten backplane slots in the processor cabinet. Two slots are reserved for the memory control logic. Eight slots are reserved for the memory storage arrays. Each extended-hex module slot provides power to the memory logic and electrical connection to a dedicated, high-speed I/O adapter bus. The bus provides a data transfer rate of up to 34.3 megabytes per second. All memory operations — addressing, data read, and data write — are pipelined in the VAX 8650. A cache reference can be completed during every cycle. Battery backup for main memory is a standard feature on VAX 8650 processors.

The VAX 8650 processor features convenient and flexible main memory expansion up to 68 megabytes. Current VAX 8650 memory storage and expansion options are shown in Table 3-1.

Table 3-1 ▪ VAX 8650 Storage and Expansion Options

SBB*	Minimum	Maximum	Expansion Arrays†
VAXcluster	32 MB	68 MB	MS86-AA and/or MS86-CA in increments of 4 and 16 Mbytes
VMS	16 MB	68 MB	MS86-AA and/or MS86-CA in increments of 4 and 16 Mbytes

* SBB = System Building Block

† The maximum number of slots available on the VAX 8650 memory backplane is eight. Each 4-megabyte MS86-AA array uses one slot, each 16-megabyte MS86-CA array occupies two slots except for the rightmost MS86-AA array that takes only one slot.

Other features of the memory arrays are:

- Up to 68 megabytes of main memory providing room for growth and support for the largest applications.
- Choice of 4 megabyte or 16 megabyte 256-kilobit dynamic MOS RAM memory expansion arrays for configuration flexibility and planned incremental expansion.
- Reduced memory access time as a result of a dedicated memory bus, pipelined references, and a greater cache hit rate.
- Use of premium quality, high-density memory components means greater reliability and lower maintenance costs.
- Standard Error Correction Code (ECC) offers exceptional reliability, data integrity, and lower service costs.

- MEMORY ARRAYS

  Two models of memory array boards, the MS86-AA and the MS86-CA, are available. MS86-CA boards have a greater storage capacity than the MS86-AA boards. Functionally, there is no difference between the boards. The boards are described in detail in the following paragraphs.

MS86-AA MEMORY ARRAY - The MS86-AA memory array board provides 4 megabytes of information per board for a total memory capacity of 32 megabytes. Each MS86-AA board contains 156 dynamic MOS RAM devices. Each RAM device has 256-kilobit by 1-bit capacity. The 150-nanosecond RAM devices are organized into four memory banks of 39 devices each forming an array matrix of 1 megabyte by 39 bits. Parity is 7-bits ECC per 32-bit longword. Each MS86-AA board can store 1,048,536 individual 32-bit longwords of data. With all eight of the VAX 8650 backplane memory slots occupied, the system attains a total physical memory capacity of 32 megabytes in 4-megabyte increments.

MS86-CA MEMORY ARRAY - The MS86-CA memory array consists of a mother board containing the control logic and eight daughter boards each holding 2 megabytes of memory. Double-sided surface mounting permits the attachment of 624 MOS RAM memory chips to the daughter boards. Each chip has a 256-kilobit capacity. This permits 16 megabytes in the space previously occupied by two 4-megabyte boards and gives the MS86-CA board at least four times the capacity of other memory array boards.

The memory chip is a single-voltage (5 V), 256 kilobit by 1, 150-nanosecond dynamic MOS RAM in a surface-mount package with a multiplexed row and column address. The array matrix is 4 megabytes by 39 bits (32 data bits, and 7 ECC).

Each MS86-CA board requires two of the eight available backplane memory slots. This limits the maximum memory configuration to four 16-megabyte boards and one 4-megabyte board for a total of 68 megabytes.

- REFRESH INTERVAL

  The refresh interval is approximately 13 microseconds or about one cycle in 36 (worst case). Refreshes are performed in one of two ways. In normal operation, refresh cycles are timed by the cycle timing chain. When in battery mode, the cycle is timed on a delay line. In both instances, the interval is timed and a refresh request is generated.

  In normal operation, refresh request is synchronized to the system clock. Then arbitration occurs, and the refresh must wait if a memory cycle is pending or is in progress. The memory cycle must wait if a refresh is pending or is in progress. When operating in battery mode, column address strobe (CAS) is shut off and the refresh addresses are chosen. No memory cycles are permitted. The refresh operation can be disabled. This prevents refreshes in normal operation but not in battery mode.

Input/Output Subsystems

The VAX 8650 uses the Synchronous Backplane Interconnect (SBI) bus as the input/output channel for the system. The SBI bus is the data path that connects both the CPU and main memory to the I/O subsystem adapters. All UNIBUS, MASSBUS, CI bus, and DDI bus devices communicate with the processor through the SBI bus. Figure 3-8 shows the basic configuration of the devices and adapters to the SBI.

For the details of the SBI bus, refer to the *VAX Hardware Handbook Volume 1–1986*. See the section on VAX 8600 I/O Subsystems for detailed information. For details of the adapters available for the SBI bus, see the section entitled Large VAX Processor UNIBUS Subsystem.

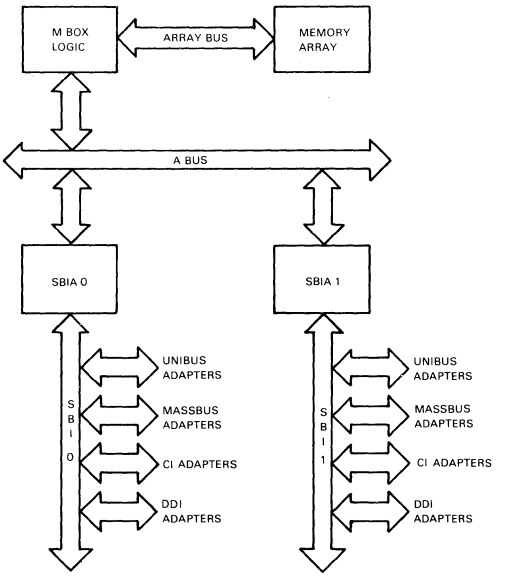

Figure 3-8 ▪ VAX 8650 SBI Bus Basic Configuration

- SYNCHRONOUS BACKPLANE INTERCONNECT ADAPTER
  The synchronous backplane interconnect (SBI) adapter is the interface between the SBI bus and the adapter bus. The SBI adapter provides the functions required to control MASSBUS and UNIBUS I/O operations. It establishes the protocol, provides the timing, and assembles the data for transmission in either direction. The SBI adapter contains the following logic elements:
  - Buffer control and adapter bus logic
  - Register file
  - Clock logic
  - SBI bus interface
  - Interrupt control logic
  - Data latches

  The SBI adapter provides the processor and memory nexus functions to the SBI bus and generates the SBI clock signals. The nexus is a physical connection to the SBI bus. Command and address data is exchanged between the SBI adapter and the Mbox through the adapter bus. Interrupt information and interrupt polling are exchanged between the SBI adapter and the Ebox. The adapter bus and buffer control logic controls the reading and writing of the SBI adapter register files, notifies the Mbox when processor or SBI adapter transactions occur, receives and buffers the timing signals for the adapter bus synchronous logic, and notifies the Ebox when an interrupt condition is detected.

  The register file stores the I/O data transferred through the SBI adapter. It is a dual-port, 16-line by 32-bit register that operates synchronously with both the adapter bus and the SBI bus.

  The interrupt logic notifies the processor of errors detected during DMA transactions, fault conditions detected on the SBI bus, and programmed maintenance procedures. It also passes interrupt requests from SBI devices to the processor. The clock logic generates the timing signals for the SBI operations. Data latches are used to hold or convert information transferred to or from the SBI bus. Information from the SBI bus is converted to the adapter bus format. The SBI adapter contains 35 registers that are accessed through the processor transaction buffer. The registers are used to condition the SBI adapter during bootstrap operations, to record error information, to store vector addresses during the servicing of interrupts, and to establish maintenance and diagnostic functions.

The SBI bus interface logic samples the data transfer lines of the SBI during each cycle and transfers the results to the SBI bus protocol logic and to the data latches. It also transmits information to the SBI bus from the data latches. The SBI adapter protocol logic provides protocol checking and verifies the commands and data received by the SBI adapter.

The I/O subsystems connect to the processor through the DB86 synchronous backplane interconnect adapters (SBI adapter 0 and SBI adapter 1). SBI adapter 0 is included with the system and SBI adapter 1 can be added in the processor cabinet. The SBI adapter 0 bus can be extended from the processor cabinet into an SBI expansion cabinet. A DW780 UNIBUS adapter (UBA) is included with the system and connects to SBI adapter 0, and one UBA option and an RB86 can be added within the processor cab to SBI adapter 0. The CI780 computer interconnect adapter (CIA) is optional and can also be connected to SBI adapter 0 for VAXcluster configuration.

- ADAPTERS

  UNIBUS, MASSBUS, CI, and DDI adapters can be installed on either SBI adapter 1 or 0. A maximum of four UBA options, four optional RH780 MASSBUS adapters (MBAs), four optional DR780 DR32 adapters (DDIs), or two CIA options can be installed on SBI adapter 1. A maximum of two CI780 interconnects per system can be installed. The combination of UBA, MBA, CIA, and DDI options on the SBI adapters depends on the total number and type of adapters installed.

  DISK DRIVE ADAPTERS - One UDA50 universal disk controller can be installed on the UNIBUS to control up to four disk drives from the RA family. The UDA50 is an intelligent controller designed for use with single processor systems that operate within the Digital Storage Architecture.

  A maximum of 16 high-speed lineprinters can installed, including LP25, LP26, and LP27 lineprinters. These printers provide hardcopy output: the LP25 prints at 300 lines per minute, the LP26 prints at 600 lines per minute, and the LP27 at 1,200 lines per minute. The printers connect to the system through the DMF32 printer port or through a separate controller that mounts on the UNIBUS.

  The UNIBUS also supports up to four RL02 (10.4-megabyte) removable-disk drives and a maximum of four TU81 magnetic tape drives. A total of eight disk drives or eight magnetic tape formatters can be connected in any combination to each MBA. The devices include the RM05 (256-megabyte) removable-disk drive and the TE16, TU77, and TU78 magnetic tape units.

  VAXCLUSTER ADAPTERS - The VAX 8650 processors are available in VAXcluster configurations. Each system includes the VAX 8650 processor, 32 megabytes of ECC MOS memory, the CI780 or DW780 adapter and connecting cables, and the DELUA Ethernet communications controller.

The CI780 computer interconnect (CI) adapter is a microprocessor controlled, high-speed interface that connects the SBI bus to the dual-path CI bus. Information is transferred at 70 megabits per second between the VAX 8650 and the VAXcluster components. The CI780 adapter cables connect to the SC008 Star Coupler unit through two receive and two transmit coaxial cables, each with a maximum length of 45 meters (147.6 feet). Through the VAXcluster, the overall system efficiency is greatly increased by sharing the processor loads and by providing access to common mass-storage facilities.

The DR780 DR32 device interconnect (DDI) is a high-performance, general purpose interface that permits communication between VAX processors and between VAX processors and user devices. It connects to the SBI bus and provides a 32-bit parallel data path and an 8-bit control path. The DDI transfers blocks of sequential data to and from memory at rates up to 6.67 megabytes per second through direct memory access (DMA) transfers.

ETHERNET ADAPTER - The DELUA (replacement product for the DEUNA) is a high-performance synchronous communication controller used in local area network applications. The DELUA connects to the UNIBUS and allows communication through the Ethernet network with Digital's systems and terminals and systems developed by other manufacturers. Used in four out of six system configurations, the DELUA permits data transfer rates of up to 10 megabits per second between processors or between processors and devices.

▪ Reliability, Availability, and Maintainability

In addition to the features included in all VAX processors, the VAX 8650 system incorporates many other features to ensure reliable operation, high system availability, ease of maintenance, and maximum performance. The hardware and software of the VAX 8650 incorporate the latest design techniques to assure efficient operation and maximum system dependability.

Approximately 15 percent of the logic circuits in the system are used to verify the operation of the system and the integrity of the data. More than 3,000 logic points on the processor backplane are available for analysis through the serial diagnostic (SD) bus and the console terminal.

Online diagnostic programs can be performed concurrently with the user mode of the VMS operating system without interrupting normal processor operations. If errors occur during the system operation, they are recorded and logged. The processor is restarted automatically and allowed to continue processing the instruction. Some of the reliability, availability, and maintenance features are:

- High availability design.
- Processor signal levels that can be monitored through the console terminal.
- Error correction code (ECC) implemented on memory, cache, and processor microprocessor control logic.
- Online diagnostics for the VAX/VMS operating system.
- System-error detection and logging.
- Autodiagnostic and remote diagnostic capabilities.
- Special maintenance capabilities provided by the console processor functions.

Battery Backup Unit

During short-term utility power interruptions, the contents of cache and the general purpose registers are written into main memory. The standard battery backup unit preserves main memory contents, so there is no memory or context loss when utility power is restored within the life of the battery backup. The battery backup unit is monitored by the processor. The processor provides a warning if the battery is discharged or otherwise faulty before it is needed.

Both boards are designed to survive temporary power failure (for a maximum of ten minutes) by providing battery mode operation. All circuits needed to maintain data are supplied power by the battery. All emitter-coupled logic and most unnecessary transistor-to-transistor logic are not supplied power in this mode. With the proper sequencing of signals, the array puts itself into battery mode when power is restored, then turns over to normal operation. There is an orderly conversion to battery and warm start. When in battery mode, the array ignores the timing chain and performs refreshes only and not memory cycles.

Error Checking Code

Automatic error checking and correcting of main memory and cache memory data eliminates many types of errors without interrupting the system operation. The memory's error correcting code (ECC) automatically corrects single-bit memory errors and detects double-bit memory errors. The ECC provides protection from nonrepeating errors by automatically correcting data and also detects greater than double-bit errors if an even number of errors is detected.

There is parity checking at RAMs and buses, and parity continuity is carried through all major data paths. Parity is kept not only for data but also for physical addresses and the microcode. Address parity and bad-data flags are *folded* into the ECC. Thus, storage words also contain information about error sources. Error detections and corrections are noted in the error log as an aid to preventive maintenance. Because there are separate selects to each memory array board, the control logic for storage selection is all in one place, and faults can be isolated to a single board.

Extensive parity checks and other fault checkers in the Mbox make it highly likely that errors will be detected and corrected, thus limiting their impact. If a transient error occurs, instruction execution pauses and the machine state is saved in memory for processing by an error-analysis program. That program provides information to Field Service for quick fault isolation.

Error Analysis and Reporting

The standard package of error analysis and reporting (SPEAR) program allows system maintenance to be deferred until a more convenient time. The program is based on the number of errors that occur and the customer is automatically notified when error rates exceed a specified value. The SPEAR program is a software maintenance tool that contains algorithms that analyze the machine check data collected by the processor. Intermittent failures that allow the processor to recover and continue operation are stored in an error file. The file is examined by the SPEAR program to determine the cause of the malfunction. The program detects specific patterns related to one error or to a series of errors.

High Availability Design

The VAX 8650 processor incorporates high availability design features that allow the system to recover rapidly from system errors by:

- Monitoring status information related to the error.
- Recording the information in an error log.
- Re-initiating the instruction in process when the error occurred.

When an error is detected that results in a machine check, up to 88 bytes of error status information can be recorded. Because most errors that occur on processors using LSI logic components are a result of intermittent failures, the processor is allowed to continue operating after the error information is stored. If the error is repeated, the stored information can be evaluated later and maintenance can be performed at the convenience of the customer.

Dynamic Fault Insertion

Dynamic fault insertion allows the fault detection logic to be checked while the VMS software is operating. Intermittent faults can be simulated by selecting the desired timing of the processor clock, and by inserting and removing a fault at the proper interval during one or more cycles. This is used to verify that the recovery logic in the processor is being executed correctly.

Serial Diagnostic Bus

The serial diagnostic (SD) bus is a network data path between the console subsystem and the processor that connects to the major logic elements in the processor. The bus verifies the system operation, diagnoses and isolates processor hardware faults, and provides a path from the console subsystem to control the operations of the processor. The SD bus and interface allow internal signal levels and signal levels transferred between modules through the system backplane to be accessed and displayed on the console terminal. This eliminates the need for the special test equipment normally required to monitor processor logic levels during maintenance.

The SD bus includes independent clocking and control, thereby enabling the console software to initialize the processor hardware, step the processor clock, monitor the state of various processor logic signals, and serially transfer data to the console where it can be verified. By stepping the processor clock, the console software is allowed to follow the progress of the processor operation and verify the logic response through the SD bus.

The SD bus consists of 24 serial data paths that connect to 24 separate visibility control channels included with the Fbox, Ebox, Ibox, and Mbox. A visibility channel in a processor module consists of an 8-bit visibility register and a multiplexer that selects internal logic information to be loaded into the visibility register. The console program reads a visibility channel by stopping the processor clock and by shifting an 8-bit address code to select a multiplexer channel. The register information is then transferred serially from the visibility register to the console subsystem and displayed on the console terminal.

Microhardcore Context Commands

The microhardcore is a diagnostic program used to verify the proper operation of the microhardcore (MCH) programs in the processor. The MCH program consists of 98 subtests that are grouped into eight processor-logic function test areas within the processor. The tests reside on the load media and the MCH program does not create or modify the files in the load device. One test group or all of the tests groups may be selected by the operator after the console diagnostics have been performed successfully. Only the selected tests are loaded into memory. Messages from the MCH program are displayed on the console or remote terminals.

The MCH context is entered by typing MCH in response to the diagnostic console prompt (>>>). Once the program is initiated, the version name and number is displayed and the microhardcore prompt (MC>) is displayed. A test group or help file may then be selected.

Debug and Trace Facility

The debug and trace facility is used to modify and interrogate the hardware state of the processor. The facility is enabled from the diagnostic context or the macrohardcore context by the debug command. A hexadecimal debugger (HEX) command set is included to allow the operator to modify and interrogate the state of the processor. When it is enabled, an additional angle bracket (>) is added to the normal console command prompt displayed on the console terminal. The HEX command set is described in detail in the *VAX Hardware Handbook Volume 1–1986.*

Parity Checks

The validity of the data and control information transferred between the processor elements is ensured by parity checks and a comparison of the stored information with information stored in another location. Most critical information has a parity indicator appended to it during the transfer. The checks performed on the VAX 8650 processor elements include cache memory parity checks, control store parity checks, general purpose register checks, internal bus parity checks, Ebox arithmetic parity checks, and control RAM parity checks. Each of the checks is described in the following paragraphs.

- CACHE MEMORY PARITY CHECKS

  When single-bit errors are detected during data transfers from the cache memory, the data is transferred with an indicator specifying that the data contains an error. A cache correction cycle is initiated to correct the single-bit error and to rewrite the corrected data into the cache memory. The logic element that requested the data issues a processor-interrupt request and a machine-check stack frame is generated. The instruction is re-executed and the corrected data is then accessed.

- CONTROL STORE PARITY CHECKS

  Single-bit errors associated with the control store logic of a controlling microprocessors in the processor can be corrected. When a control store parity error is detected, the processor is halted and the data containing the error is transferred to the console subsystem and corrected by the console ECC software. Then the microword is rewritten into the control store location and the instruction is automatically reissued without causing a fatal halt condition of the processor. When an Mbox parity error is detected, the bit in error is identified and recorded. However, the processor does not recover and resume operations.

- GENERAL PURPOSE REGISTER CHECKS
  Single-bit parity errors associated with the general purpose registers (GPRs) are correctable. Because of the multiple sets of GPRs in the VAX 8650, if an error is detected in the information stored in one GPR set, a copy of the information from a valid GPR is written into the GPR that contains the error.

- INTERNAL BUS PARITY CHECKS
  Parity is generated on the information transferred through the internal processor buses. The parity is produced and checked on 8-bit bytes and on 32-bit words on some of the buses.

- EBOX ARITHMETIC UNIT PARITY CHECKS
  The Ebox contains three sets of arithmetic logic units (ALUs) that receive the same inputs and perform the same functions. If the outputs of the three ALUs are not the same, a failure is recorded and the instruction is executed again.

- CONTROL RAM PARITY CHECKS
  Parity checks are performed on the outputs of the control RAM to ensure that the control functions are not in error.

Reliability and Maintainability Features

The design of the processor hardware includes many reliability and maintenance features such as:

- Socket-mounted RAMs — The RAM integrated circuits used on the VAX 8650 modules are mounted in sockets for easy removal and replacement. This feature eliminates the need to replace the entire module when a defective RAM is located, resulting in lower maintenance costs and faster repair.

- Logic Partitioning — Logic functions are grouped together on modules so that when a module is replaced due to a suspected failure, all the logic associated with that function is replaced.

- Cabinet Cooling — The processor cabinet allows conditioned air, ducted through a raised floor, to enter through the bottom of the cabinet. The air passes through the modules and the modular power supplies and is expelled through a plenum at the top rear of the cabinet. The plenum chamber is muffled to keep the overall noise level within the acoustic limits of 60 decibels per ampere.

- Multilayer printed circuit technology — Up to six layers of wiring are required to interconnect the devices mounted on a printed circuit board. This wiring is maintained at controlled impedance to guarantee signal integrity. The backplanes contain 16 layers of printed wiring in a laminated structure.

Chapter 4 ▪ VAX 8550 and VAX 8500 Processors

The VAX 8550 and VAX 8500 processors share the same advanced design technologies as the top-of-the-line VAX 8800. Both the VAX 8550 and VAX 8500 offer cost-effective processing power in a compact package. While the VAX 8500 defines a new standard for midrange VAX computing, the VAX 8550 extends this standard to high-performance VAX computing in the same compact footprint.

The VAX 8500, VAX 8550, VAX 8700, and VAX 8800 are all implemented with the VAXBI I/O subsystem and high-speed internal memory (MI) bus. The key attribute of the VAX 8550 and VAX 8500 systems is that they offer more CPU performance in less space than other systems offered by Digital.

The VAX 8550/VAX 8500's power, processor, memory, and primary I/O subsystems all fit in a 27-by-30-inch wide footprint. This efficient and cost-effective packaging includes the processor and integral hot floating point, a single high-speed VAXBI I/O channel, and 20 Mbytes of main memory that can be expanded to a total of 80 Mbytes. The second VAXBI channel and a VAXcluster interface can be configured in an I/O expander cabinet.

Continuing the tradition that made VAX systems the standard for 32-bit computing, VAX 8500 provides three times the performance of the VAX-11/780 and VAX 8550 performance is six times that of a VAX-11/780. The VAX 8550 and VAX 8500 are designed for all compute environments not requiring the more extensive expansion of the VAX 8700. The VAX 8500 also provides a lower-cost entry with future upgrade to VAX 8550 as requirements expand.

Some of the features and benefits of these systems are:

- Powerful performance in compact packaging.
- Advanced VAX technology, including high-speed VAXBI I/O.
- Low-cost multiuser solution across a wide variety of applications.
- Cost-effective, incremental growth with VAXcluster configurations.
- Full networking capabilities with standard Ethernet port.
- Full VAX/VMS software compatibility.

Figure 4-1 identifies the VAX 8550/VAX 8500 processors. Refer to Table 1-1 to compare these systems to other Digital VAX and MicroVAX systems.

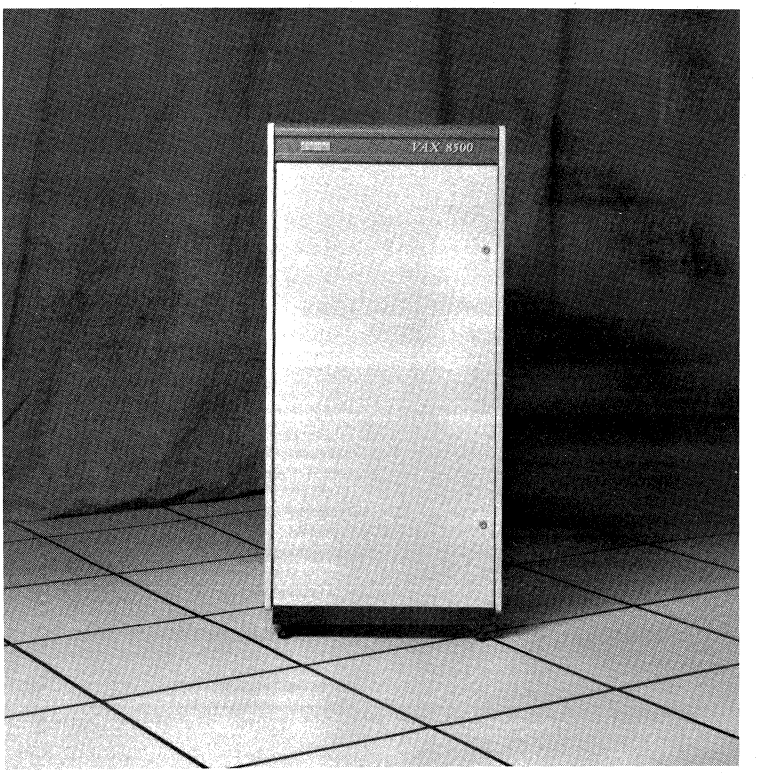

Figure 4-1 ▪ VAX 8550 and VAX 8500 Processors

▪ VAX 8550 and VAX 8500 Physical Configuration

The VAX 8550/VAX 8500's full complement of main memory, CPU modules, one VAXBI channel and Ethernet port require only 5.6 square feet of floorspace. These systems require less input power (57%), dissipate less heat (51%), and take up less space (66%) than the VAX-11/780. A new 22 layer backplane, innovative power supply distribution methods, and simplified internal cabling make the VAX 8550/VAX 8500 processors one of the most reliable and easy to maintain systems in their class. These air-cooled systems are based on a clean internal design with airflow patterns contributing to their noticeably low noise level.

Figure 4-2 shows the physical dimensions of the VMS version of both processor cabinets. Figure 4-3 shows a stand-alone configuration of the processors, and Figure 4-4 shows the VAXcluster configuration.

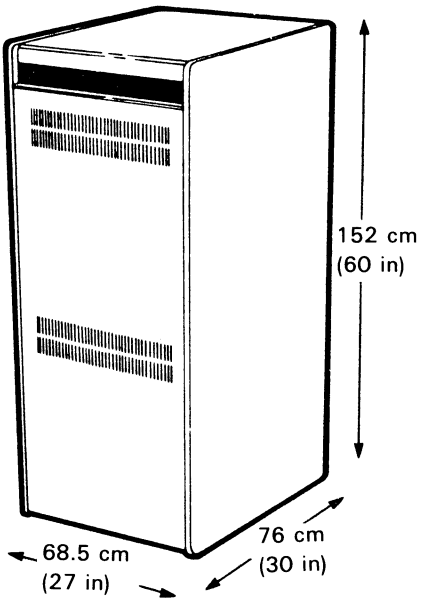

Figure 4-2 ▪ VAX 8550 and VAX 8500 Cabinet Dimensions

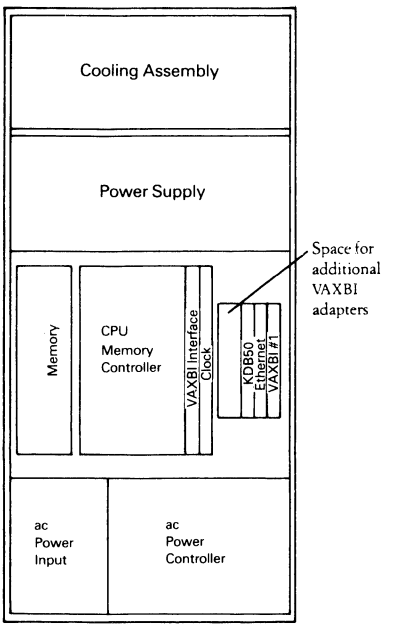

Figure 4-3 ▪ VAX 8550 and VAX 8500 Processor VMS Stand-alone Configuration

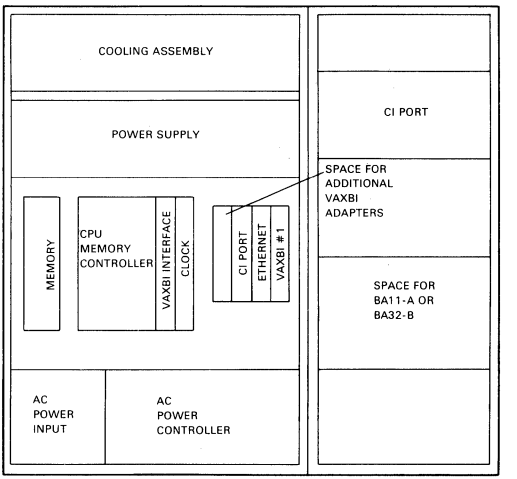

Figure 4-4 ▪ VAX 8550 and VAX 8500 Processor VAXcluster Configuration

▪ VAX 8550 and VAX 8500 Processor Organization

The VAX 8550 and VAX 8500 processors are functionally identical to the VAX 8700 processor. Therefore, descriptions of the VAX 8700/VAX 8800 processors in Chapter 2 are relevant for the VAX 8550/VAX 8500 processors.

The major differences between the systems are:

- VAX 8550/VAX 8500 have a smaller footprint than the VAX 8800/VAX 8700.
- The VAX 8550/VAX 8500 have a five-slot memory backplane; the VAX 8800/VAX 8700 have an eight-slot memory backplane.
- The VAX 8550/VAX 8500 have one NBIA module supporting a maximum of two VAXBIs; the VAX 8800/VAX 8700 have two, supporting four VAXBIs.

The similarities between the systems are:

- The console subsystem hardware is identical.
- All systems use the same tools and test equipment.
- Console code differences are transparent, contained in the same set of software.
- The modular power supplies (MPS) are identical.

Figure 4-5 is a block diagram of the VAX 8550 and VAX 8500 Processors. It may be compared to the VAX 8700 and VAX 8800 system configurations shown in Figures 2-4 and 2-5, respectively.

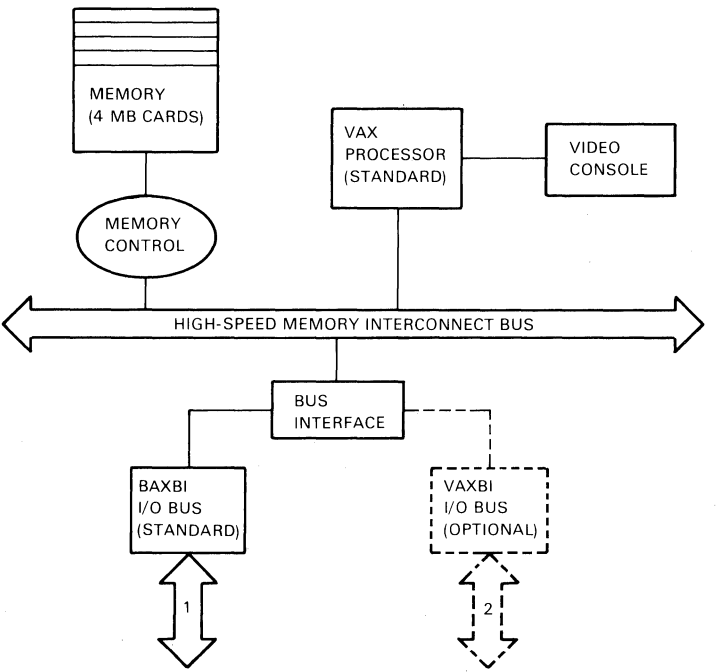

Figure 4-5 ▪ VAX 8550 Processor Configuration

Main Memory

The VAX 8550/VAX 8500 systems have 20 Mbytes of ECC memory composed of 256-bit dynamic RAM chips arranged in 4-Mbyte arrays. The memory is totally contained in the CPU cabinet and has a three-way interleaving controller with a memory array bus that provides a bandwidth of over 50 Mbytes per second. Individual 4-Mbyte and 16-Mbyte memory boards can be added up to a system maximum of 80 Mbytes.

VAXBI I/O Subsystem

The VAX 8550/VAX 8500 systems use the VAXBI bus for I/O. One VAXBI channel with five usable slots is standard with an option to expand to a maximum of two channels. With each channel capable of usable data rates of up to six times the UNIBUS, it is possible for the VAX 8550/VAX 8500 systems to achieve aggregate data rates of up to 16 Mbytes-per-second using two VAXBI channels. The high I/O bandwidth, reliability features, and inherent programmable features of the VAXBI make it ideally suited for high-performance peripherals and I/O intensive applications.

Many I/O devices on the VAX 8550 and VAX 8500 connect directly to the VAXBI. Native VAXBI interfaces include:

- Ethernet Port (standard)
- VAXcluster Port
- Disk Adapter (KDB50)
- Tape Adapter (TU81-Plus)
- Multifunction Communications Controller (DMB32)

UNIBUS Support for VAX 8500 and VAX 8550 Systems

The optional VAXBI to UNIBUS adapter (DWBUA) is available on both the VAX 8500 and VAX 8550 to aid in the migration of traditional UNIBUS devices. This option is available for new system orders and for field upgrades to existing VAX Systems.

Digital Networks and VAXcluster Systems

The VAX 8550/VAX 8500 systems include a VAXBI-to-Ethernet port as a standard feature. Ethernet is the recommended terminal and workstation communications method because its high-performance and extensive connectivity complements the performance capabilities of the VAX computers. Ethernet terminal servers should be used to attach terminals to the VAX 8550/VAX 8500s.

The VAX 8550 and VAX 8500 VAXcluster building blocks offer a standard VAXcluster port and the required adjacent expander cabinet. This allows the VAX 8550/VAX 8500 to be configured immediately into VAXcluster Systems, bringing to VAXclusters compact high-performance compute nodes. Check with your Digital sales representative for stand-alone VAX 8500 and VAX 8550 system upgrades to VAXcluster Systems.

▪ Reliability, Availability, and Maintainability

The VAX 8550 and VAX 8500 systems share all of the maintainability and reliability features of the top-of-the-line VAX 8800 system. ECL machines operating at cycle time of 45 nanoseconds, the VAX 8550/VAX 8500 are the fastest systems in their class. The memory subsystem is served by a technology-independent memory controller that eliminates the need for controller changes when new memory technologies become available.

The VAX 8550/VAX 8500's highly intelligent console system is a J-11 chip minicomputer with video interface, 1 Mbyte of memory, 30-Mbyte Winchester Disk, 800-Kbyte floppy disk drive and a remote diagnosis port. System powerup, diagnostics, monitoring, and control can be performed quickly and efficiently via a realtime interface to the CPU. An environmental monitoring subsystem within the CPU cabinet monitors temperatures in voltages throughout the CPU and continuously reports status conditions via the console. Electronically keyed modules allow the console to perform automatic hardware and software revision compatibility checks as well as checks for correct module placement.

Designed for high reliability, both systems use custom and semicustom semiconductor devices, a 22-layer backplane, ZIF (Zero Insertion Force) connectors, and 9-layer logic modules. Extensive parity and data integrity protection has been implemented throughout the various buses, cache memory, data buffers, and RAMs.

The VAXBI also enhances system reliability through the following features:

- All of the bus interface logic is compressed into a single integrated circuit, the VAXBI Interface Chip (BIIC).
- Because there are no cables on any VAXBI modules, maintenance is simplified and reliability is enhanced.
- BIIC contains complete self-test capabilities.
- Extensive error detection and logging logic is included in the VAXBI.
- Reliability has been proven by complete specification, simulation, and verification of the whole VAXBI.

Chapter 5 • VAX 8200 and 8300 Processors

The VAX 8200 and VAX 8300 processors are the kernels of Digital's midrange VAX Systems. These processors combine the latest developments in custom MOS VLSI (Metal Oxide Semiconductor, Very-Large Scale Integrated) circuit technology with the high-speed performance and multiprocessing capabilities of the VAXBI bus.

VAX 8200/8300 systems are distinguished by their ability to provide large system performance and functions at midrange processor prices. The VAX 8200 delivers VAX-11/780 performance at approximately half the price. It can be easily upgraded to a VAX 8300. The VAX 8300, with nearly twice the computational power of the VAX 8200, is especially appropriate for applications that are computationally intensive. With two processors, it offers a more cost-effective solution than the single processor VAX 8200 system for most applications demanding as little as 30 to 40 percent performance improvement. And, of course, both systems offer VAXcluster and UNIBUS support.

VAX 8200 systems support two general purpose, timesharing operating systems —VMS and ULTRIX-32. VAX 8300 systems support VMS only. Some of the features and benefits of the VAX 8200/8300 systems are:

- Big-system features in a small footprint.
- Economical additions to your VAXcluster System.
- High I/O throughput based on the VAXBI bus for balanced processor and I/O performance.
- Higher compute performance with the complete VAX instruction set in advanced VLSI circuitry.
- PDP-11 compatibility as an option in the form of VMS-layered emulation software.
- Easy expansion from the VAX 8200 (one central processor, 8-Kbyte cache) to the VAX 8300 (two processors, total of 16-Kbytes of cache).

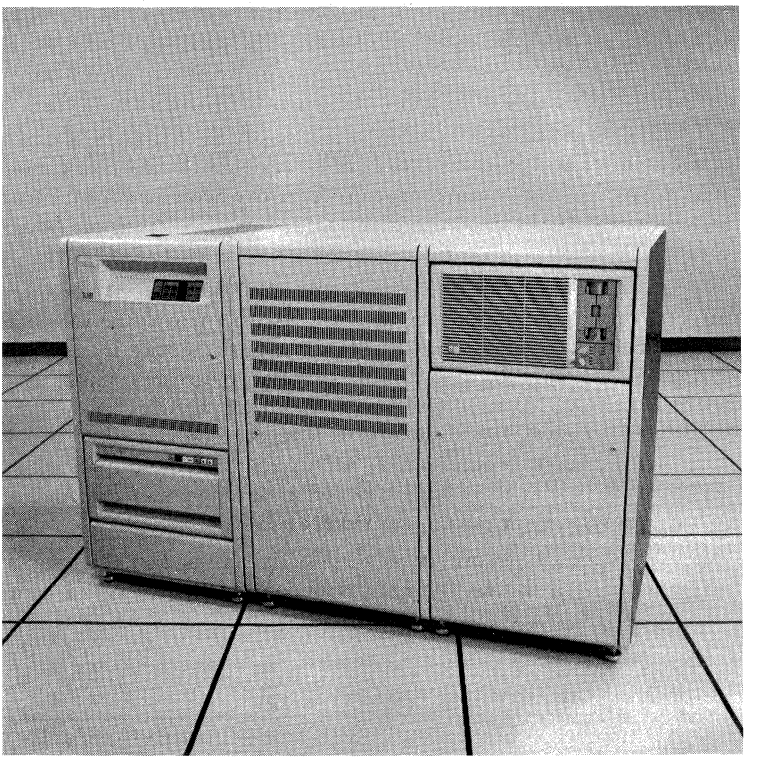

Figure 5-1 ▪ VAX 8200 and VAX 8300 Processors

In the following sections differences between the VAX 8200 and VAX 8300 are noted and explained. For performance specifications refer to Appendix A and the system comparison chart in Chapter 1 (Figure 1-1).

▪ VAX 8200/8300 System Configurations

VAX 8200 and VAX 8300 systems are housed in a cabinet that contains the VAXBI bus and the components that plug into the it — processors, memories, and I/O adapters. See Figure 5-2. The processor cabinet also contains its power subsystem, a 5.25-inch diskette drive, standard corporate bulkhead connector panels, and space for the memory's battery backup option. The cabinet can hold twelve VAXBI modules and has one power supply.

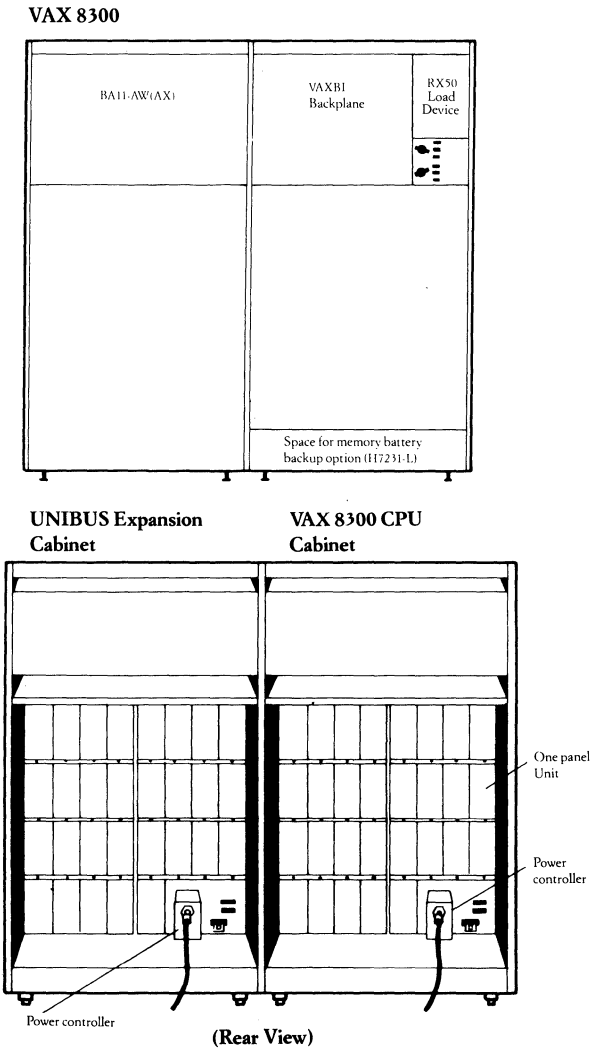

Figure 5-2 ▪ Processor Cabinet

UNIBUS support for VAX 8200 and VAX 8300 systems includes a BA11-AY/AZ expander box mounted in an adjacent cabinet shown in Figure 5-3. The VAX-cluster interface is also mounted in a similar but separate cabinet.

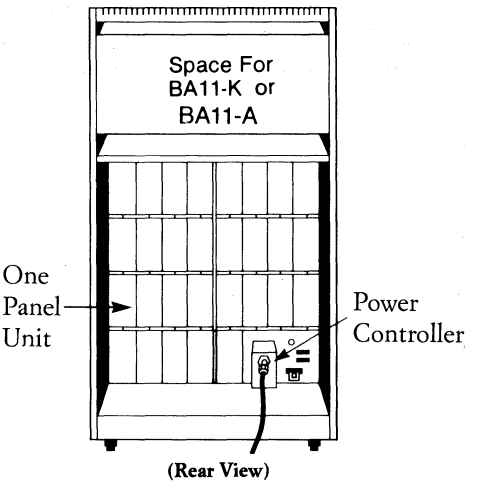

Figure 5-3 ▪ UNIBUS Expander Cabinet

VAX 8200/8300 systems are also available in the rackmount box shown in Figure 5-4. This box provides technical OEMs the most versatile VAX packaging yet for embedded applications.

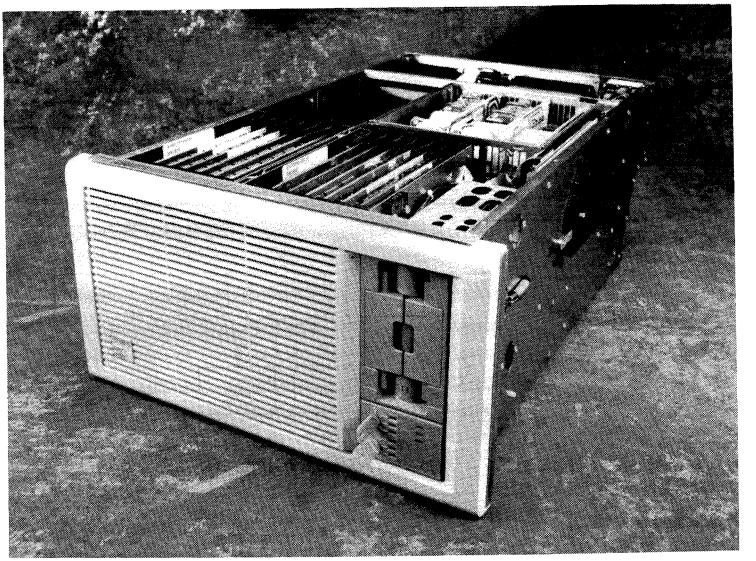

Figure 5-4 ▪ VAX 8200 and VAX 8300 Rackmount Box

The VAX 8200 System has one processor. The VAX 8300 System has two. Otherwise, both systems are functionally identical. Figures 5-5 and 5-6 give an overview of VAX 8200/8300 systems. The systems contain a processor, ECC memory modules, a second processor (with the VAX 8300), and a VAXcluster adapter or a disk adapter.

The processors are connected to memory by the VAXBI bus that also serves as the input/output bus for communications and storage peripherals. These are connected to the VAXBI bus with a variety of VAXBI adapters and interfaces.

An Ethernet adapter is standard with both systems. Optional adapters are available for a TU81-Plus magnetic tape drive and a multifunction adapter with synchronous and asynchronous serial lines and a printer port. Additional functions are provided by UNIBUS peripherals.

The console subsystem includes a serial-line interface for the console terminal, control panel, and an interface for the console load (diskette) device.

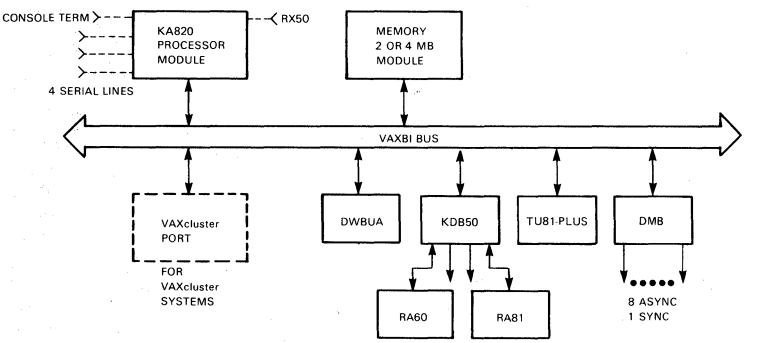

Figure 5-5 ■ VAX 8200 System Configuration

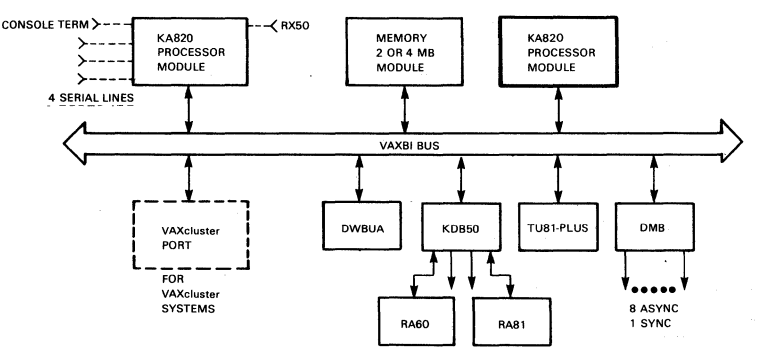

Figure 5-6 ■ VAX 8300 System Configuration

The configurations attainable with the VAX 8200 and VAX 8300 Systems are many and cannot be described here for practical reasons. There are a multitude of considerations when configuring a system — number of disk and tape drives, connections to local area networks, connections to wide area networks, and VAXclusters. Your local Digital representative has the information needed to configure a system best suited for your unique application.

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Console Subsystem

The console subsystem, included with each system, enables the system user, manager, and maintenance engineer to communicate with the processor through the console terminal and console command language. Console subsystem design is governed by the VAX Architecture. Both the architecture and the console subsystem are described in the *VAX Hardware Handbook Volume 1 — 1986*. Volume 1 also includes an overview of VAX console subsystems and the Console Command Language.

Processor microcode emulates the control-panel lights and switches of traditional computer systems with an ASCII console. The console subsystem functions are compatible with those of other VAX consoles. They allow you to

- Bootstrap the system.
- Examine and deposit data in registers and in memory.
- Run stand-alone programs without use of the operating system.
- Single step through VAX macrocode.
- Start and stop the processor.
- Test the hardware with the self-test microcode and macrodiagnostic programs.

The console subsystem performs these functions from a hardcopy terminal. Both processors of the VAX 8300 are controlled by a single console subsystem. The console is always in one of three states when power is on — Program I/O mode, Console mode, or Halted with Console Disabled.

▪ Central Processing Unit

The KA820 processor module is Digital's densest VLSI processor design to date. Equivalent to the 24-module VAX-11/780 processor, the KA820 is implemented on a single module with 8 custom VLSI chips that are the design equivalent of over 1.3 million transistors. Integral acceleration of D, F, and G floating-point instructions processing is standard.

Additional processor features include an asynchronous serial line for the console terminal, three low-speed serial lines for general use, and the interface to the console load device.

CPU Section

The block diagram of the KA820 module, shown in Figure 5-7, depicts the functional division of the CPU, VAXBI Interface, and Port Controller sections.

Three chips carry out processor functions according to 40-bit microinstructions stored in the control store chips. The Instruction/Execution chip is used for instruction decoding and execution. The Memory Interface chip is used for memory management, processor registers, and four serial-line units. The F chip is the floating point accelerator.

An onboard translation buffer caches address translation data (called page table entries or PTEs) for 512 pages of memory. The backup translation buffer parallels the minitranslation buffer in the I/E chip. And an onboard data cache holds data from the most recently accessed locations in memory.

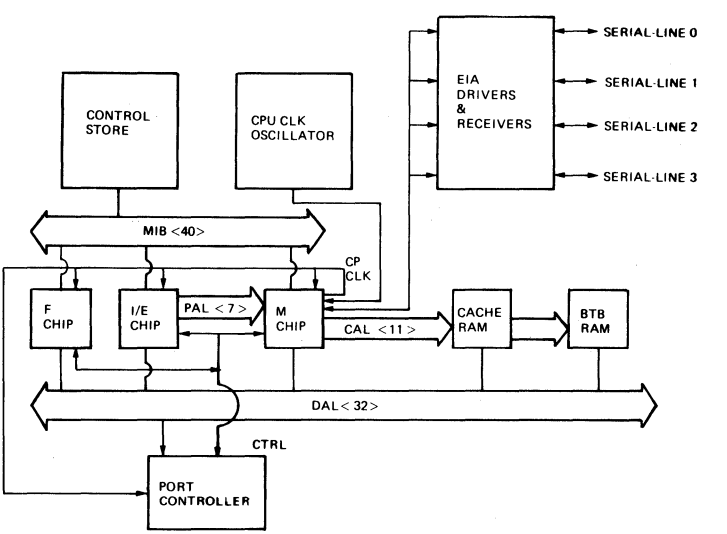

Figure 5-7 ▪ KA820 Processor Block Diagram

- INSTRUCTION/EXECUTION (I/E) CHIP
  The instruction/execution (I/E) chip is divided into four areas — instruction buffer, microsequencer, execution unit, and minitranslation buffer.

  INSTRUCTION BUFFER - The instruction buffer is a silo that holds up to eight bytes of prefetched VAX instructions. The CPU can execute sequences of instructions rapidly without waiting for memory read cycles to fetch instructions. The hardware tries to keep the instruction buffer full. The instruction buffer initiates a read function when it is not full and there is no other activity on the DAL bus that takes precedence. In addition, the instruction buffer sends information it gathers from decoding VAX instructions to the execution unit and the F chip.

  MICROSEQUENCER - The microsequencer determines the address of the next microinstruction to be executed (with two exceptions — at the beginning of a VAX instruction, and when the first part done flag is set following an interrupt or exception). When a new VAX instruction is being decoded, the microaddress generator determines the entry point of the microroutine to be executed. During the first half of the CPU clock cycle, the I/E chip drives the microaddress over the microinstruction bus. During the second half of the CPU clock cycle, the control store sends the addressed microinstruction word on the MIB bus to the execution unit. This prefetch function assures that the execution unit never waits for a microinstruction. A new microinstruction is available at the beginning of each 200-nanosecond CPU clock cycle.

  EXECUTION UNIT - The execution unit contains 16 general purpose registers (R0–R15), the arithmetic and logic units, the shifter, and data paths. It executes the microinstructions needed to implement the macroinstructions in the instruction buffer; move data and addresses to and from the registers; and move data and addresses on the DAL bus to the F and memory interface chips, backup translation buffer, cache, and port controller. When the execution unit derives a virtual address to be accessed, it sends that address to the minitranslation buffer for translation to a physical address.

MINITRANSLATION BUFFER - The minitranslation buffer (MTB) caches physical address translations for five pages of virtual memory — four data-stream pages and one instruction-stream page. The information for each address translation is called a page table entry (PTE). Each MTB location contains a tag and a page table entry. The tag tells whether there is a valid page table entry in the MTB for a given virtual address. The page table entry includes a 21-bit page frame number identifying the 512-byte page of physical memory to be used on references to the virtual address. With valid page table entries, the MTB generates the physical address from the valid entry and make the physical address available on the DAL bus without delay.

- MEMORY INTERFACE (M) CHIP

The memory interface (M) chip functions complement the instruction/execution (I/E) chip functions. They include

- Backup translation buffer tag store.
- Cache tag store.
- Internal processor register (IPR) implementation.
- Interrupt handling.
- Memory management.
- Processor clock generation.
- Serial-line unit implementation.
- Port controller interface.

The four RS423-compatible serial-line units on the memory interface chip connect terminals directly to the processor. Signal lines from the serial-line units are converted to the standard RS232 format off the module. You can set the baud rate of each serial-line unit separately by writing a location in the EEPROM or by writing to the appropriate transmit control and status (TXCS) register.

The baud rate on serial-line unit 0 can be changed, when the primary processor is in the console mode, by pressing the <BREAK> key on the console terminal. Available baud rates range from 150 to 19,200.

Each of the four serial-line units is implemented in a universal asynchronous receiver/transmitter (UART) in the memory interface chip. Each UART makes four privileged processor registers available to software — the Receive Control and Status Register, the Receive Data Buffer, the Transmit Control and Status Register, and the Transmit Data Buffer.

The serial-line units are full duplex. They transmit and receive data simultaneously. When interrupts are enabled, character transfer occurs one byte at a time. And each serial-line unit interrupts the processor at interrupt priority level (IPL) 14(hex) every time it receives or transmits a character.

- FLOATING POINT ACCELERATOR (F) CHIP

The floating-point accelerator (F chip) increases the arithmetic efficiency of the processor by speeding up execution of the integer and floating point arithmetic instructions:

- ADD (F, D, G)
- CMP (F, D, G)
- CVTL (F, D, G)
- DIV (F, D, G)
- EDIV
- EMUL
- MUL (F, D, G)
- POLY (F, D, G)
- SUB (F, D, G)

The accelerator chip operates in parallel with the instruction/execution chip. The instruction/execution chip makes decisions concerning the instruction being executed. The accelerator chip performs the calculations required for the instruction being executed.

The microinstruction bus supplies the accelerator chip with VAX opcodes and microinstructions. The opcodes come from the instruction/execution chip and microinstructions from control store. The data address line bus carries operand data between the accelerator chip and memory or the instruction/execution chip's general purpose registers.

- CONTROL STORE

Control store is an onboard memory that is used to store microcode that

- Controls VAX instruction execution.
- Invokes processor initialization, bootstrapping, and console functions.
- Performs processor self-test.

Control store consists of a 15-Kword by 40-bit ROM plus a 1-Kword by 40-bit ROM implemented in five ROM/RAM chips and protected by parity. The RAM stores microcode patches, making microcode changes as simple as software changes. Control store and the processor chip set are connected by the microinstruction bus (MIB) that is protected by parity checking.

- BACKUP TRANSLATION BUFFER
  There are two translation buffers — the minitranslation buffer described above and the backup translation buffer. The minitranslation buffer caches five physical address translations called *page table entries* while the backup translation buffer caches 512 page table entries. A cache hit in the minitranslation buffer incurs no delay, while a cache miss in the minitranslation buffer, which leads to a cache hit in the backup translation buffer, incurs a 200 nanosecond delay.

  The backup translation buffer has two storage locations. The memory interface chip is the tag storage location, and the backup translation buffer RAMs store the page table entries.

- CACHE RAM
  The cache memory is a direct-mapped write-through design. It consists of an 8-Kbyte array divided into 128 blocks of 64 bytes each. The cache RAM stores copies of data from main memory. A large and fast cache RAM helps increase system performance when processing large jobs. The CPU uses the portions of main memory stored in cache RAM to reduce response time.

  Like main memory, the cache RAM uses physical addresses to access the data. The cache tag store contains 128 tags — one for each block of data. Each tag includes 16 bits of a physical address with a parity bit and 4 valid bits with a parity bit. The 4 valid bits apply to the four octawords within a block of cache data.

VAXBI Interface Section

The VAXBI interface consists of the 32-bit, parity-protected BCI bus and the bus interconnect interface chip (BIIC). The BIIC implements the VAXBI bus protocol including a distributed arbitration scheme and bus error checking facilities.

Port Controller Section

The port controller and dedicated port controller interface (PCI) bus devices make up a third section of the KA820 module. The port controller buffers the transfer of addresses and data between the CPU and the PCI bus devices as well as between the CPU and the VAXBI interface.

The EEPROM is a 16 Kbyte nonvolatile memory on the PCI bus. It stores choices for KA820 options, VAX bootstrap macrocode, and the patches for control store microcode. A write protection circuit prevents the stored data from being changed accidentally. Microcode copies the bootstrap macrocode to an 8 Kbyte boot RAM on the PCI bus at the beginning of the boot process.

The electrically erasable programmable read-only memory (EEPROM) on the PCI bus contains 16 Kbytes of information defining options, the physical configuration, microcode patches, and VAX boot code. The data in the EEPROM remains valid if power is removed. When power is restored, EEPROM data is used by the microcode to initialize the processor and boot the system.

Digital distributes updates for the EEPROM with software and microcode patches on diskettes. The EEPROM utility is used to load update data into the EEPROM.

The PCI bus also runs off the KA820 module to connect to the battery-backed-up watch chip and the RX50 disketted drive controller (RCX50). The watch chip keeps the time of year for up to 100 hours without system power. The RX50 diskette drive is used to install software and microcode updates.

Main Memory

Main memory for VAX 8200 and VAX 8300 Systems is available in 2- or 4-megabyte boards. Both implement an advanced design that encompasses data, address, error correction and control logic within three complex CMOS (VLSI) gate arrays on the memory array board. Easy, cost-effective memory expansion is available in 2 Mbyte or 4 Mbyte increments.

Onboard memory logic eliminates the need for a separate memory controller. Operating on the VAXBI bus as a slave only, MS820 memory modules interface by way of the onboard BIIC. Onboard logic provides an aggregate I/O write bandwidth of up to 13.3 megabytes per second, an aggregate I/O read bandwidth of up to 10.0 megabytes per second, and up to 11.4 megabyte per second single device write bandwidth. Internal onboard interleaving between the two memory banks on the MS820 memory module improves system throughput and performance.

The 4-Mbyte MS820-B memory array uses the latest double-sided surface-mount technology. It uses 256 kilobit plastic leaded chip carrier (PLCC) dynamic RAMs mounted on both sides of a single VAXBI module. The 2-Mbyte MS820-A memory array uses 256 kilobit dual-inline-package (DIP) dynamic RAMS. Both modules use error correction code (ECC) to detect double-bit errors and to correct single-bit errors.

Maximum memory size in the 12-slot processor cabinet or in the rackmount box is 24 Mbytes. Maximum memory size in the 24-slot processor cabinet is 24 Mbytes with battery backup, or 48 Mbytes without battery backup. Memory in a VAX 8300 system is fully sharable between the two processors.

The H7231 battery back-up option provides protection from a temporary power outage by maintaining the contents of main memory for about ten minutes.

Power Subsystem

The VAX 8200 power supply is a high-frequency, hybrid, switching power supply. The unit contains nine regulated outputs for a total output power of 593 watts. The power supply has three main modules. Each module plugs into a slot on the power distribution board. The power supply has a volume of approximately 803 cubic inches and weighs 15 pounds.

One power supply is used in the processor cabinet and in the rackmount box. Input power can be 120 Vac at 60 hertz or 240 Vac at 50 hertz. The power supply is UL recognized, CSA certified, and VDE compliant.

Input/output Subsystem

VAX processors connect to peripheral devices, networks, and other VAX processors through the input/output (I/O) subsystems. These subsystems electrically connect the devices to memory, permitting fast and reliable transfer of information.

Both the VAX 8200 and the VAX 8300 use the VAXBI bus for I/O. For a technical description of the bus and the variety of disk, communication, network, and cluster adapters available as options, please refer to the *VAXBI Options Handbook.*

Mass Storage Subsystems

Digital offers a complete line of intelligent mass storage subsystems and storage devices designed specifically to operate with VAX processors and VAXcluster architecture. These subsystems and devices allow a user to select the mass-storage requirements that best suit the system application and to add storage capabilities when application requirements increase.

Chapter 7 of this volume includes a brief description of the KDB50 Disk Adapter and the HSC70 Intelligent I/O Server. The KDB50 is more fully described in the *VAXBI Options Handbook.* The *VAX Systems and Options Catalog* also provides detailed device descriptions, configuring information, and ordering codes.

Architectural information on mass storage subsystems can be found in *VAX Hardware Handbook Volume 1 — 1986* and the *Storage Systems Handbook.*

▪ Reliability, Accessibility, and Maintainability

The VAX 8200 and VAX 8300 are the most reliable and maintainable midrange VAX systems ever offered.

Central processor features that provide fault tolerance, error detection and diagnostics include

- 5 Kwords of self-test microcode
- Cache and translation buffer parity
- Microinstruction retry
- Microcode check sum
- Microcode parity

At the processor-component level, maximum use of VLSI circuit technology results in considerably fewer parts. For example, the VAX 8200 processor is mounted on one module as opposed to 24 on the VAX-11/780. Many electronic components are preconditioned prior to insertion to preclude the malfunctioning of an uncured component. And ECC memories and most VAXBI devices are implemented on single modules to increase system reliability.

The carefully-engineered power supply and packaging enhance the inherent reliability of VAX 8200 and VAX 8300 systems. Important features include

- The new VAXBI ZIF (Zero Insertion Force) connectors that provide easy insertion and removal of modules.
- Air flow monitoring.
- Power supply thermal monitoring.
- Module and control panel LEDs for self-test reporting.
- Backplane slot independence.
- All cable and intermodule connections by way of the backplane (no cables attached to modules).

The integrity of data and processes are protected by checking extensively for

- Parity errors
- VAXBI transaction errors
- Unforeseen microcode conditions
- Interrupts occurring at unexpected levels

The machine-check function is invoked following detection of a hardware error. The machine check passes control to appropriate exception-handling software. This lets the software evaluate the situation and respond appropriately. In addition, the KA820 module uses a microcode-based ASCII console and provides a serial-line unit that connects the console terminal to the KA820.

The KA820 module contains a self-test microcoded program. The program can be invoked manually or automatically. A console command is used to invoke it manually. When power is applied to the system, the program is invoked automatically.

Battery Backup Unit

The battery backup unit (BBU) option preserves memory content during a public utility power failure. The BBU is capable of supporting the memory modules for about ten minutes from a fully charged battery. It is intended to provide power for the memory modules during short-term power losses that occasionally occur. Battery mode is entered automatically when public utility power is interrupted. When system power is restored, normal operation is resumed.

Cooling Subsystem Monitoring

The processor cabinet is equipped with an air filter and an air-flow sensor. The sensor is mounted behind the backplane interconnect cage and in front of the power supply modules. The signal from the air-flow sensor is delayed by the sensor before going high if no air flow is detected. This allows the VAX to powerup. If no air flow is detected, the ac circuit breaker in the power supply is tripped, safely shutting down the VAX.

Error Correction Code

MS820 main memory has 7 check bits per 32 data bits to provide single-bit error correction and full double-bit error detection. The memory error correction code (ECC) automatically corrects single-bit errors and detects double-bit memory errors. Detections and corrections are noted in the error log as a preventive maintenance aid.

Self-test Routine

In order to ensure the system is functioning properly, a self-test routine runs automatically whenever you apply power or when a command is entered from the console. The routine verifies that the CPU hardware and the VAXBI nodes are functioning.

Two basic areas of the system are tested — the processor and the nodes on the VAXBI bus. The VAXBI bus connects each processor to options such as I/O controllers, bus adapters, memory arrays, and other processors. Each of these VAXBI options has its own self-test routine.

- PROCESSOR SELF-TEST ROUTINE

  The self-test routine has two speeds — normal and fast. Speed is selected by the initiator or user. In most situations, the normal test is used. The test takes 10 seconds and gives maximum coverage to system hardware. The fast self-test takes 0.25 second but checks only the cache memory and the F chip. The fast self-test is intended for realtime applications during recovering from a public utility power failure.

  Characters printed on the console terminal, the FAULT light on the control panel, and lights in the processor cabinet indicate the status of the self-test. When the self-test routine begins, all indicators report simultaneously.

As each section of the CPU hardware passes the test, a letter appears on the terminal. A different letter is assigned to each section of the CPU. Each CPU module has a red light that is on while the CPU self-test routine is running. The light turns off if the CPU passes the test. It the CPU fails the test, the red light stays on.

- MEMORY SELF-TEST ROUTINE

  The MS820 memory array module performs a self-test on powerup. During self-test, the MS820 tests the BIIC, ECC logic, address and control gate array, data-path gate arrays, and the MOS RAMs. Initialization is performed at the conclusion of the self-test for a cold powerup, but initialization is not performed for a warm restart. Initialization clears memory.

  Self-test and initialization takes about 5 seconds on the MS820-B module and about 3 seconds on the MS820-A module. Self-test without initialization, performed from a warm powerup, takes less than 0.25 seconds for either module.

Zero Insertion Force (ZIF) Connectors

System modules are connected to the VAXBI backplane by ZIF (Zero Insertion Force) connectors that are surface mounted to a backplane. ZIF connectors are keyed to ensure that backplane interconnect modules cannot be inserted upside down and also that the modules are positively seated. This ensures proper installation and prevents damage to both the module and the other components.

Chapter 6 ▪ VAX Privileged Registers

The VAX processor register space provides access to CPU control and status registers such as memory management base registers, processor status longword, and multiple stack-pointer registers. The VAX privileged registers are accessible only by move to processor register (MTPR) and move from processor register (MFPR) instructions, which are controlled by the kernel executive in the VMS operating system. The operating system manages these registers for the user; however, they are available to system programmers, operators, and maintenance personnel.

This chapter highlights the architecturally defined registers common to all VAX systems, the VAXBI registers, and the processor specific registers for the VAX 8800/8700, 8650, 8550/8500, and VAX 8300/8200 systems. Note that references to Volume 1 in the text refer to the *VAX Hardware Handbook Volume 1 — 1986.*

▪ Architectural Processor Registers

Table 6-1 lists the architectural processor registers by name, abbreviation, and address. Format for the system identification (SID) register and bit values for the VAX 8800/8700, 8650, 8550/8500, and 8300/8200 are shown in the figures below. Formats for the other VAX architectural registers are found in Volume 1, Chapter 10.

Table 6-1 ▪ VAX Architectural Processor Registers

Register Name	Abbreviation	Address
Kernel Stack Pointer	KSP	00
Executive Stack Pointer	ESP	01
Supervisor Stack Pointer	SSP	02
User Stack Pointer	USP	03
Interrupt Stack Pointer	ISP	04
P0 Base	P0BR	08
P0 Length	P0LR	09
P1 Base	P1BR	0A
P1 Length	P1LR	0B
System Base	SBR	0C
System Length	SLR	0D
Process Control Block Base	PCBB	10
System Control Block Base	SCBB	11

(continued on next page)

Table 6-1 ▪ VAX Architectural Processor Registers (Cont.)

Register Name	Abbreviation	Address
Interrupt Priority Level	IPL	12
Asynchronous System Trap Level	ASTLVL	13
Software Interrupt Request	SIRR	14
Software Interrupt Summary	SISR	15
Interval Clock Control/Status	ICCS	18
Next Interval Count	NICR	19
Interval Count	ICR	1A
Time-of-year	TODR	1B
Console Receive Control/Status	RXCS	20
Console Receive Data Buffer	RXDB	21
Console Transmit Control/Status	TXCS	22
Console Transmit Data Buffer	TXDB	23
Machine Check Status	MCSTS	26
Memory Management Enable	MAPEN	38
Translation Buffer Invalidate All	TBIA	39
Translation Buffer Invalidate Single	TBIS	3A
Performance Monitor Enable	PME	3D
System Identification	SID	3E
Translation Buffer Check	TBCHK	3F

System Identification Register

The system identification (SID) register specifies the VAX processor type and the hardware and software revision levels used in a particular processor. These values are included in the error log. The type field may be used by software to distinguish processor types.

Figure 6-1 shows two SID registers — one for the VAX 8800/8700 and 8550/8500 systems, and one for the VAX 8300/8200 systems. The VAX 8650 uses the VAX 8600 SID register format shown in Volume 1, page 10-3.

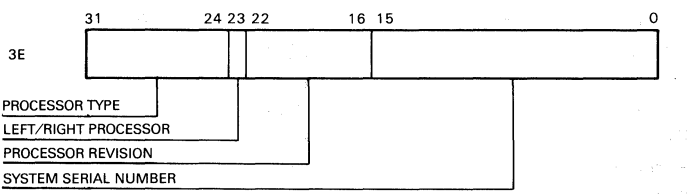

Figure 6-1 ▪ VAX 8800/8700 and VAX 8550/8500 SID Register Format

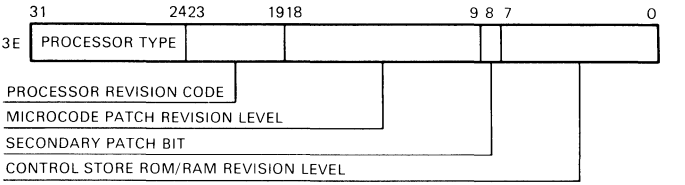

Figure 6-2 ▪ VAX 8300/8200 SID Register Format

▪ VAXBI Registers

Each VAXBI node is required to implement a minimum set of registers contained in specific locations within the node's nodespace. Table 6-2 lists the VAXBI registers and their addresses. All but the Slave-only Status register and the Receive Console Data register are on the BIIC.

Table 6-2 ▪ VAXBI Registers

Register Name	Abbreviation	Address
Device	DTYPE	*bb* + 00*
VAXBI Control and Status	VAXBICSR	*bb* + 04
Bus Error	BER	*bb* + 08
Error Interrupt Control	EINTRCSR	*bb* + 0C
Interrupt Destination	INTRDES	*bb* + 10
IPINTR Mask	IPINTRMSK	*bb* + 14
Force-bit IPINTR/STOP Destination	FIPSDES	*bb* + 18
IPINTR Source	IPINTRSRC	*bb* + 1C
Starting Address	SADR	*bb* + 20
Ending Address	EADR	*bb* + 24
BCI Control and Status	BCICSR	*bb* + 28
Write Status	WSTAT	*bb* + 2C
Force-bit IPINTR/STOP Command	FIPSCMD	*bb* + 30
User Interface Interrupt Control	UINTRCSR	*bb* + 40
General Purpose Register 0	GPR0	*bb* + F0
General Purpose Register 1	GPR1	*bb* + F4
General Purpose Register 2	GPR2	*bb* + F8
General Purpose Register 3	GPR3	*bb* + FC
Slave-only Status	SOSR	*bb* + 100
Receive Console Data	RXCD	*bb* + 200

*The abbreviation *bb* refers to the base address of a node; that is, the address of the first location of the nodespace.

Device Register

The device register contains a *device type* field and a *device revision* field. The *device revision* field identifies the revision level of the device. The *device type* field identifies the type of node.

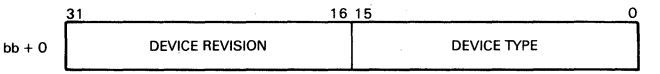

Figure 6-3 ▪ Device Register

VAXBI Control and Status Register

The VAXBI control and status register provides control and status information about the VAXBI bus. Control information output to this register can enable interrupts, change the arbitration mode, or perform a desired function. Status information input from this register includes the type and revision level of the primary interface to the VAXBI bus, error and error type, and *read for* or *done with* operation information.

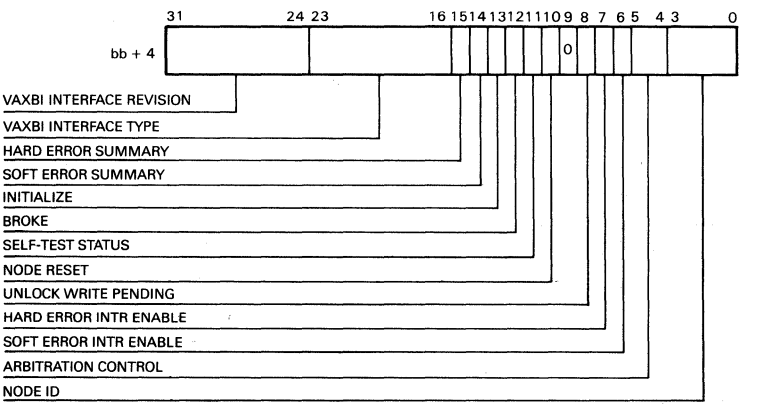

Figure 6-4 ▪ VAXBI Control and Status Register

Bus Error Register

Bits in the bus error register are set when there are errors in a VAXBI or loopback transaction.

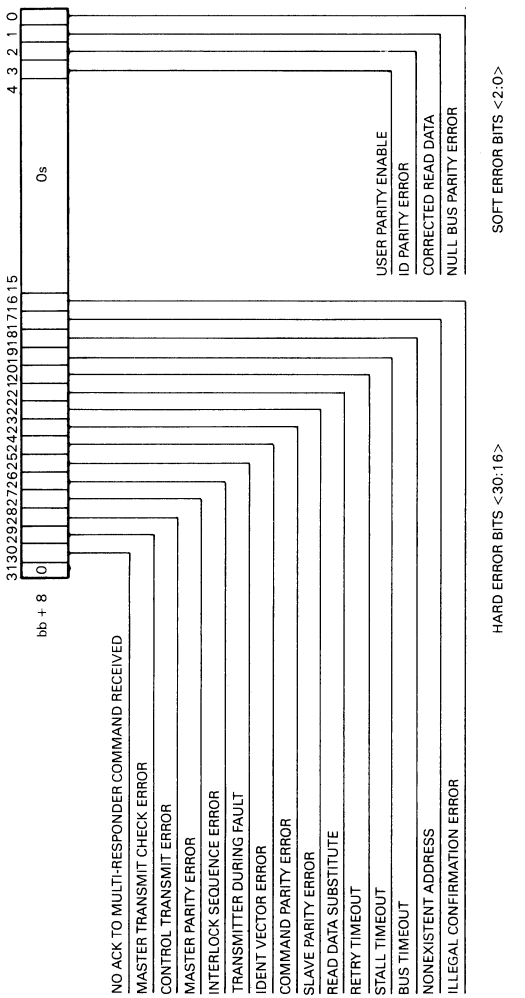

Figure 6-5 ■ Bus Error Register

Error Interrupt Control Register

The error interrupt control register controls the operation of interrupts initiated by a BIIC-detected bus error (which sets a bit in the bus error register) or by the setting of a force bit in this register.

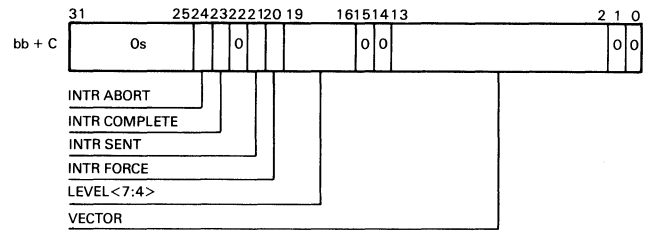

Figure 6-6 ▪ Error Interrupt Control Register

INTR Destination Register

The INTR destination register indicates which nodes are to be selected by INTR commands. The destination is sent out during the INTR command and is monitored by all nodes so that they may determine whether or not to respond.

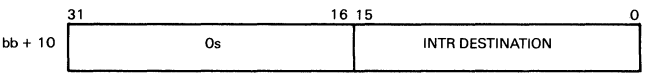

Figure 6-7 ▪ INTR Destination Register

IPINTR Mask Register

The IPINTR mask register indicates which nodes are permitted to send IPINTRs to this node. If a bit in the IPINTR mask field is a 1, IPINTRs directed at this node from the corresponding node will cause selection (assuming the IPINTREN bit in the BCI control and status register is set). If the bit is a 0, IPINTRs directed to this node will not cause selection.

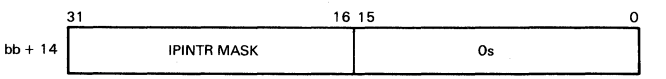

Figure 6-8 ▪ IPINTR Mask Register

Force-bit IPINTR/STOP Destination Register

The force-bit IPINTR/STOP destination register indicates which nodes are to be targeted by force-bit IPINTR or STOP commands sent by this node.

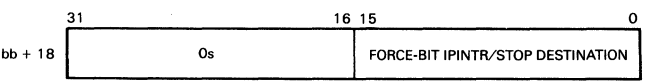

Figure 6-9 ▪ Force-bit IPINTR/STOP Destination Register

IPINTR Source Register

The IPINTR source register is used by the BIIC to store the decoded ID of a node that sends an IPINTR command to the node. Each bit corresponds to one node on the VAXBI bus.

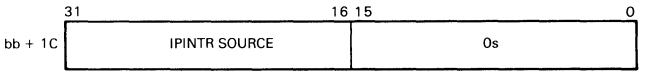

Figure 6-10 ▪ IPINTR Source Register

Starting Address Register

The starting address register defines the beginning of storage blocks in either memory or input/output space. If the starting address register is set to a value greater than or equal to the contents of the ending address register, no address will be recognized.

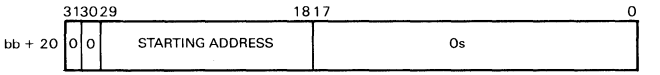

Figure 6-11 ▪ Starting Address Register

Ending Address Register

The ending address register defines the end of storage blocks in either memory or input/output space. If the starting address is set to a value greater than or equal to the contents of the ending address register, no addresses will be recognized.

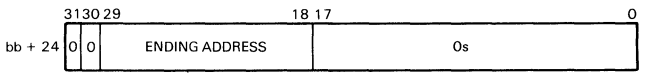

Figure 6-12 ▪ Ending Address Register

BCI Control and Status Register

The BCI control and status register provides control and status information about the BIIC. Control information output to this register can enable the BIIC to initiate VAXBI transactions, assert VAXBI signal lines, and output signal confirmation and event codes.

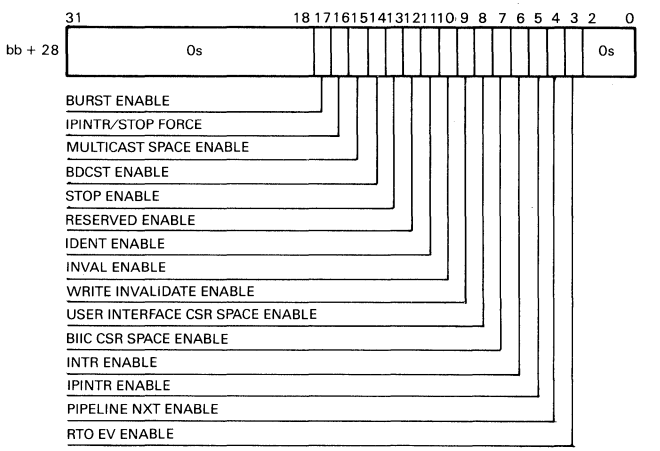

Figure 6-13 ▪ BCI Control and Status Register

Write Status Register

The write status register indicates which general purpose registers have been written to by a VAXBI transaction.

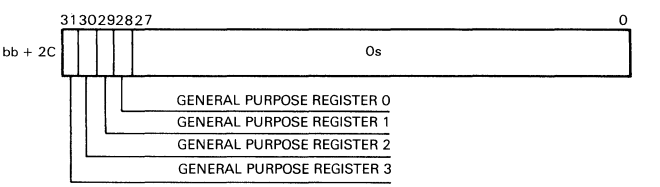

Figure 6-14 ▪ Write Status Register

Force-bit IPINTR/STOP Command Register

The force-bit IPINTR/STOP command register indicates the 4-bit command code for either an IPINTR or STOP transaction that is initiated by setting the IPINTR/STOP force bit. It is also used to determine whether the master's ID is transmitted during the command/address cycle of a transaction initiated by setting the IPINTR/STOP force bit.

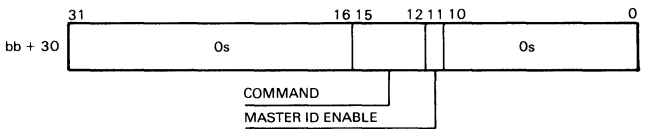

Figure 6-15 ▪ Force Bit IPINTR/STOP Command Register

User Interface Interrupt Control Register

The user interface interrupt control register controls the operation of interrupts initiated by the user interface.

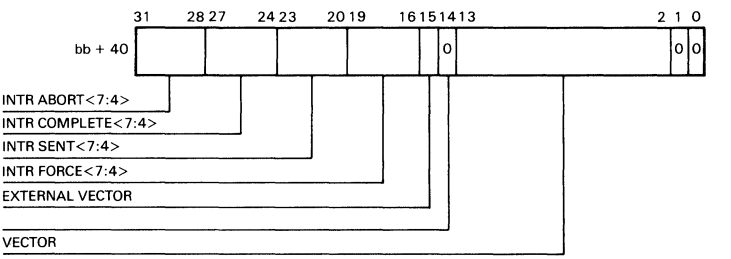

Figure 6-16 ▪ User Interface Interrupt Control Register

General Purpose Registers

The use of the general purpose registers is implementation specific. Whenever one of these registers is written, a bit is set in the write status register to indicate which register was written.

bb = F0	GENERAL PURPOSE REGISTER 0
bb = FA	GENERAL PURPOSE REGISTER 1
bb = FB	GENERAL PURPOSE REGISTER 2
bb = FC	GENERAL PURPOSE REGISTER 3

Figure 6-17 ▪ General Purpose Registers

Slave-only Status Register

The slave-only status register, which is outside BIIC CSR space, is used by slave-only nodes to implement a *broke* bit. This register must be implemented by nodes that have a device type code with zeros in bits 8 through 14.

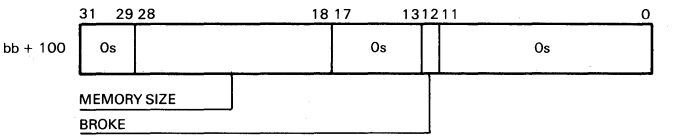

Figure 6-18 ▪ Slave-only Status Register

Receive Console Data Register

The receive console data register, which is implemented by VAXBI nodes that have a console on the VAXBI bus, is used to receive data from other consoles.

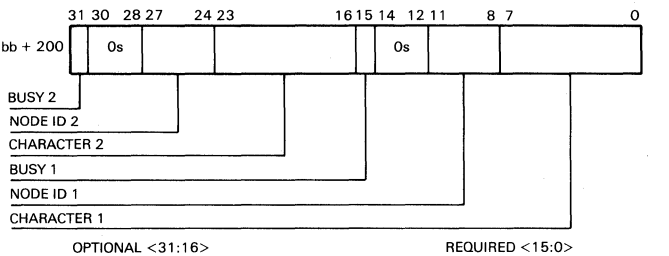

Figure 6-19 ▪ Receive Console Data Register

▪ VAX 8800/8700 Registers

In addition to the VAXBI registers there are three additional groups of registers that are of interest in VAX 8800 and VAX 8700 systems. The first group consists of the registers specific to the VAX 8800/8700 processors. The second group consists of the registers associated with the VAX 8800/8700 NBIA adapter, and the third group consists of the registers associated with the VAX 8800/8700 memory controller. Table 6-3 lists the processor-specific registers.

Table 6-3 ▪ VAX 8800/8700 Processor-specific Registers

Register Name	Abbreviation	Address (Hex)
Machine Check Status	MCSTS	26
NMI Interrupt Control	NICTRL	80
Interrupt Other Processor	INOP	81
NMI Fault/Status Register	NMIFSR	82
NMI Silo Data Register	NMISILO	83
NMI Error Address Register	NMIEAR	84
Cache On Register	COR	85
Revision Register 1	REVR1	86
Revision Register 2	REVR2	87
Clear Timeout Status	CLRTOSTS	88
Flush Write Buffer	FLUSHWB	89

Note that there are no bit digrams for INOP, CLRTOST, and FLUSHWB registers in the figures that follow. Data written to these registers is ignored. The bit diagrams in this chapter use the following conventions:

- 0 on read is treated as a zero.
- 0 on write means that software must supply zeros. Microcode does not force zeros or check for errors. These bits are read back as written.
- X on write is ignored.

Machine Check Status Register

The following is the read version of this register.

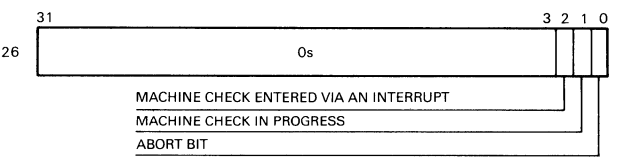

Figure 6-20 ▪ MCSTS Register

NMI Interrupt Control Register

This write-only register enables the types of interrupts taken by the processor.

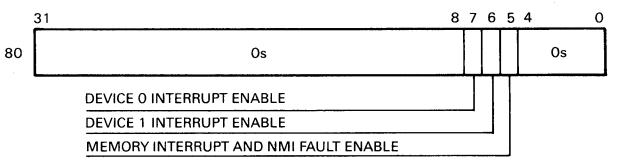

Figure 6-21 ▪ NICTRL Register

NMI Fault/Status Register

This register keeps a summary of faults and timeouts on the memory interconnect.

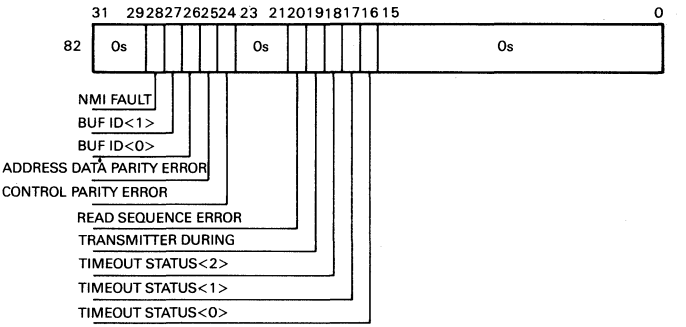

Figure 6-22 ▪ NMIFSR Register

NMI Silo Data Register

This read-only silo stores up to 256 transactions on the memory interconnect. It is initialized to lock on faults. Every read pops one value of a locked silo.

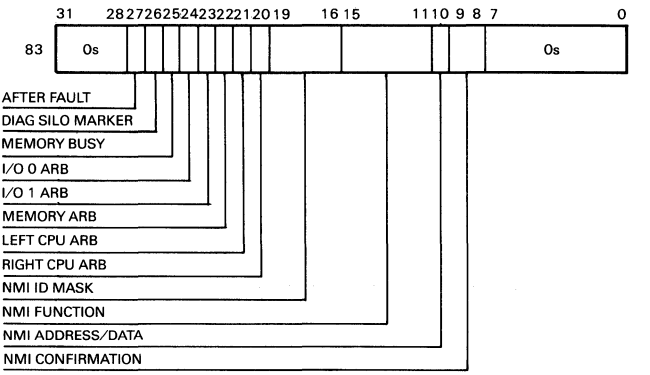

Figure 6-23 ▪ NMISILO Register

NMI Error Address Register

This register holds the address of a processor-memory transaction that has timed out on the memory interconnect.

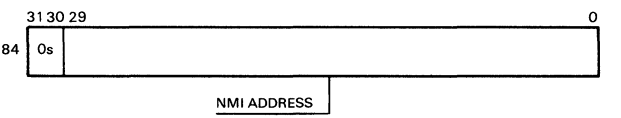

Figure 6-24 ▪ NMIEAR Register

Cache On Register

This read/write register controls the use of the cache memory.

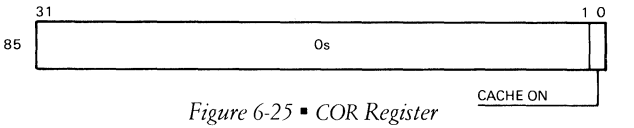

Figure 6-25 ▪ COR Register

Revision Register 1

This is a read-only register.

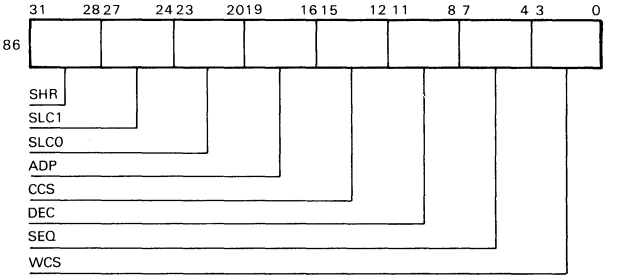

Figure 6-26 ▪ REVR1 Register

Revision Register 2

This is also a read-only register.

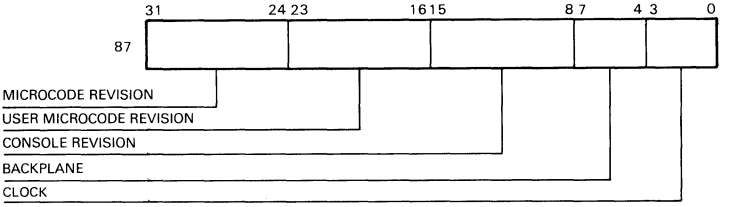

Figure 6-27 ▪ REVR2 Register

▪ NBIA Adapter Control/Status and Vector Registers

Table 6-4 lists the VAX 8800/8700 NBIA adapter registers. The registers are accessed by the processor by means of memory interconnect read/write (longword) transactions. The two reserved registers are not currently used. Note: In the address column, the X stands for 0 (NBIA 0) or 4 (NBIA 1).

Table 6-4 ▪ VAX 8800/8700 NBIA Adapter Registers

Register Name	Abbreviation	Address
Control/Status Register 0	CSR0	2X08 0000
Control/Status Register 1	CSR1	2X08 0004
Reserved	RSVD0	2X08 0008
Reserved	RSVD1	2X08 000C
BR4 Vector Register	BR4VR	2X08 0010
BR5 Vector Register	BR5VR	2X08 0014
BR6 Vector Register	BR6VR	2X08 0018
BR7 Vector Register	BR7VR	2X08 001C

The NBIA has two control/status registers.

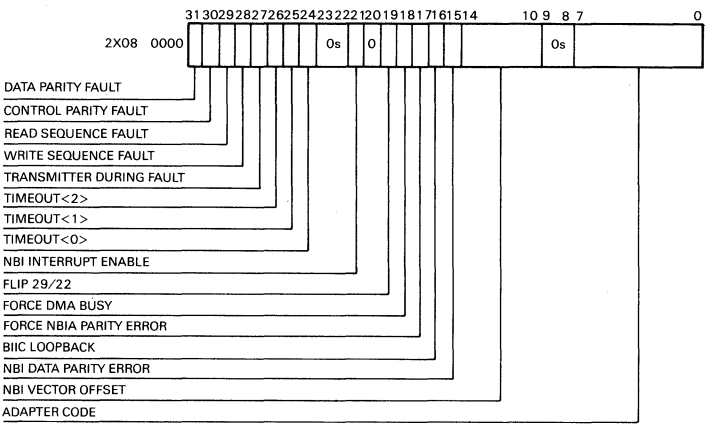

Figure 6-28 ▪ CSR0 NBIA Adapter Register

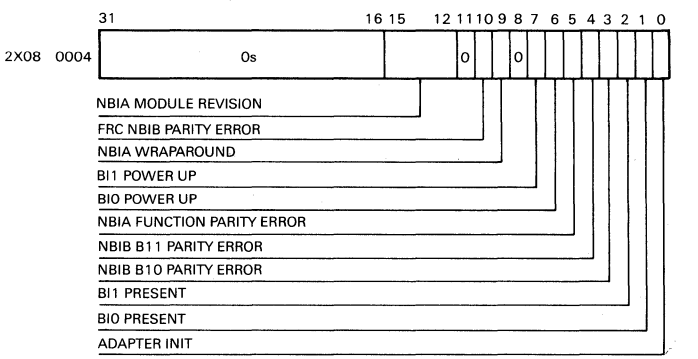

Figure 6-29 ▪ CSR1 NBIA Adapter Register

The NBIA has four read-only vector registers. When the NBIA is making a processor interrupt request at some level (BR4, BR5, BR6, or BR7), processor microcode reads the interrupt vector from the corresponding vector register. All four vector registers use the bit format shown in Figure 6-30.

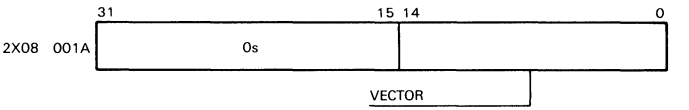

Figure 6-30 ▪ Format for BR4VR, BR5VR, BR6VR, and BR7VR Registers

▪ Memory Controller Register

Table 6-5 lists the control/status registers in the VAX 8800/8700 memory controller.

Table 6-5 ▪ VAX 8800/8700 Memory Controller Registers

Register Name	Address
Control/Status Register 0	3E00 0000
Control/Status Register 1	3E00 0004
Control/Status Register 2	3E00 0008
Control/Status Register 3	3E00 000C
Control/Status Register 4	3E00 0010
Control/Status Register 5	3E00 0014
Control/Status Register 6	3E00 0018

The first four registers are physical registers. The remaining registers are pseudo register addresses that perform specific functions.

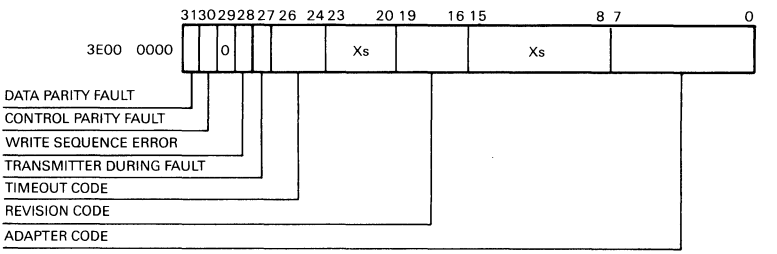

Figure 6-31 ▪ CSR0 Memory Controller Register

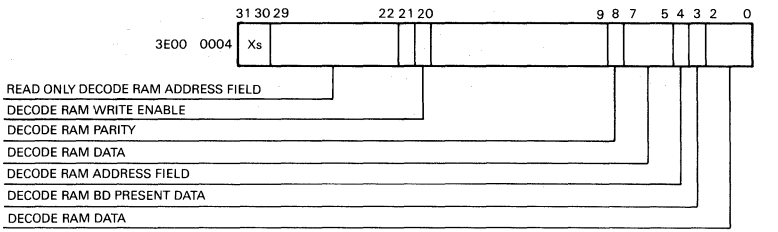

Figure 6-32 ▪ CRS1 Memory Controller Register

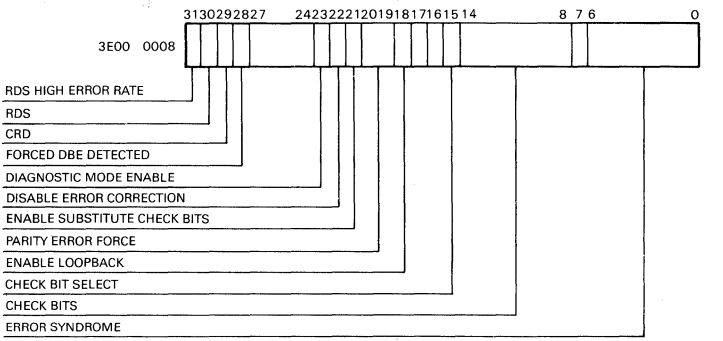

Figure 6-33 ▪ CSR2 Memory Controller Register

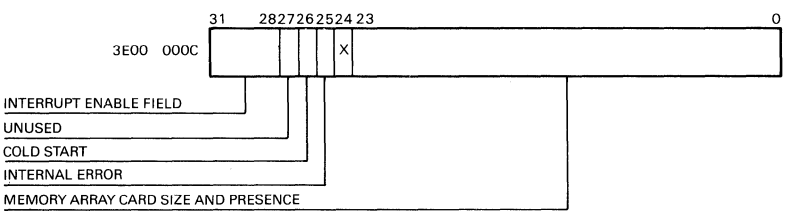

Figure 6-34 ▪ CSR3 Memory Controller Register

▪ VAX 8650 Registers

The VAX 8650 registers are the same as the VAX 8600 registers. See Volume 1, Chapter 10.

▪ VAX 8550/8500 Registers

The VAX 8550/8500 registers are the same as the VAX 8800/8700 registers described above.

- **VAX 8300/8200 Registers**

  See the VAXBI Registers section at the beginning of this chapter.

Chapter 7 ▪ Mass Storage Systems

Digital offers a complete line of intelligent mass-storage subsystems and storage devices designed specifically to operate with VAX processors and VAXcluster architecture. These subsystems and devices allow a user to select the mass-storage requirements that best suit the system application and to add storage capabilities when the application requirements increase. The storage subsystems and devices operate with the VAXBI, Q-Bus, UNIBUS, and VAXclusters to provide fast and reliable access to information. The interaction of the VAX processors normally required to access and manage data has been reduced by allocating many of the data tasks to the mass-storage subsystem and devices.

Digital Storage Architecture (DSA) is the framework governing the design and manufacture of an expanding group of mass-storage devices and intelligent controllers. The DSA provides leadership data reliability and integrity features. It allows efficient performance and ease of maintenance for all Digital storage subsystems and devices. New systems and devices that are developed by Digital can be easily added to the system without the need to replace existing storage devices or to generate new software.

Some of the features provided by DSA and storage subsystem design are:

- Advanced data integrity techniques.
- High-capacity, mass-storage devices.
- Intelligent controllers that provide error detection and improved throughput.
- Easy migration to new Digital mass storage products.
- Integrated host processor and storage subsystem engineering.
- Dual-access drive capabilities

▪ Intelligent Mass Storage Controllers

The HSC50, HSC70, and KDB50 intelligent mass storage controllers perform many of the functions required to effectively manage and control the storage and transfer of information. The HSC50 controller is a special-purpose storage controller that operates as a node in a VAXcluster. The HSC70 is the newest member of the HSC family of intelligent mass storage controllers. The HSC70 controller is designed to operate with multiple systems that must share information locally or where systems or applications require high-speed disk and tape I/O. The KDB50 controller is a new, high-performance microprocessor-based VAXBI disk controller designed for fast, reliable, and optimum RA-disk throughput performance on the new VAXBI-based computer systems.

HSC50 Controller

The HSC50 is an intelligent controller that performs many of the functions required to effectively manage and control the storage and transfer of information. The HSC50 is a special purpose storage controller that operates as a node within the VAXcluster architecture and coordinates the activities of up to 24 mass-storage devices including disk and magnetic tape drives. The HSC50 controller can serve several host processors connected to the VAXcluster CI bus.

The HSC50 is housed in a stand-alone cabinet, is independently powered, and electrically isolated from the CPUs and drives that it serves. It provides high-performance I/O throughput using a PDP-11-based microprocessor in conjunction with multiple, high-speed bit slice microprocessors. The HSC50 server offloads all disk management functions from the host systems and provides host-independent sharing of common data among a network of locally connected midrange and larger processors. Refer to the *VAX Hardware Handbook, Volume 1–1986* for more details on this controller.

HSC70 Controller

The HSC70 controller is a multichannel controller that connects both disk and tape drives to all of the host computers in a VAXcluster. The HSC70 supports a combination of eight disk and tape data channels. Each disk data channel supports four drives over the Standard Disk Interface (SDI). Each tape data channel supports four tape formatters over the Standard Tape Interface (STI) and, depending upon which formatter is used, from one to four tape transports can be supported by each formatter.

The HSC70 connects to one or more host computers by means of the 70-Mbit-per-second dual path Computer Interconnect (CI) bus. A CI can accommodate up to 16 nodes or connected devices, so a single HSC70 server can provide storage services for as many as 15 VAX host computers and as many as 32 devices. A fully configured HSC70 can provide attachment to over 14.5 Gbytes of mass storage. Any node can be a VAX or an HSC, so CPUs and HSC70 and HSC50 servers can be mixed in any combination to service any required balance of computing power and I/O bandwidth or connectivity.

Individual microprocessors control disk and tape operations and communications with host computers. In addition, a PDP-11-based microprocessor manages all of the internal work flow, performance optimizations, and error recovery.

The HSC70 architecture exceeds the HSC50 architecture with:

Greater Drive Connectivity — The HSC70's extended backplane can accommodate up to 8 HSC5X-BA data channels for a total drive connectivity of 32 compared to the HSC50's 24. (All 32 drives may be RA-series disk drives, or up to 16 of them may be TA-series tape formatters.)

Greater I/O Command Handling Performance — The HSC70 Master Control Microprocessor Module is based on the J-11 chip used in the PDP-11/73. (The HSC50 is based on the F-11 chip used in the PDP-11/23 +.) The increased command processing capability is supported by expanded program, control and data memories in the HSC70. Maximum I/O handling capability is approximately twice that of the HSC50. (Maximum steady data throughput remains the same at approximately 4.2 Mbytes/second.)

Greater Operational Convenience — Ease of use is improved through greatly shortened boot times with the use of an RX33 double-sided floppy disk drive as the load medium rather than the HSC50's TU58. An improved operator interface uses a combination of a VT220 and LA50 instead of the HSC50's LA12. Ease of use is further improved via improved operator handling, console terminal help, and improved installation and operational documentation.

Greater Reliability — Manufacturing process improvements and testing procedures have resulted in improved reliability for both the HSC70 and the HSC50.

With an I/O request rate up to twice that of the HSC50, depending on request size, the HSC70 is the ideal storage server for midrange to high-end cluster configurations and for stand-alone VAX 8650 and VAX 8800 processors, while the HSC50 remains the storage server of choice for low-range to midrange VAX processors and clusters. Table 7-1 compares the general specifications of these I/O servers.

Table 7-1 ▪ Comparison of HSC70 and HSC50 I/O Servers

	HSC70 I/O Server	HSC50 I/O Server
Connectivity:		
Data Channels	Up to 8	Up to 6
Devices	Up to 32	Up to 24
Memory Size:		
Data Memory	256 Kbytes	128 Kbytes
Program Memory	1,024 Kbytes	256 Kbytes
Control Memory	256 Kbytes	128 Kbytes
Processor Power	J-11 Processor	F-11 Processor
Boot/reboot Time (approximate)	1 minute	6 minutes
Auxiliary Power	Integral	Optional

The HSC70 controller *performance specifications* are as follows:

- CI port bandwith: 8.8 Mbytes/s (maximum)
- I/O request/second: up to 650
- Disk data-channel bandwidth:3.125 Mbytes/s (maximum each channel)
- Internal data bus: 13.3 Mbytes/s (maximum)

KDB50 Controller

The KDB50 single-host controller is the only method of connecting disk drives directly to the VAXBI bus. The KDB50 is mounted in two adjacent slots in the BI-Bus cage box and consists of two BI-modules and represents one BI-Bus interface. Up to four RA-series disk drives may be radially connected to each KDB50 controller. Currently, each RA-series disk drive can range in capacity from 121 Mbytes to 456 Mbytes for a total capacity of over 1,800 Mbytes per KDB50. Because the KDB50 disk controller is compatible with all DSA/SDI disk drives, both present and future generation disks will *plug and play* on the KDB50.

The KDB50 communicates with the disk drives using the SDI bus and SDI protocol and with the host using the VAXBI bus and the Mass Storage Control Protocol (MSCP). Two BI modules make up the KDB50 — the Standard Disk Interface (SDI) module and the processor module. The Standard Disk Interface module is the communication interface between the KDB50 processor module and the disk drives. The processor module contains a dual microprocessor and a Control Store Read Only Memory (CROM).

The KDB50 DSA performance optimizations make it ideal for use in many high-performance environments. Contained in microcode, these performance optimizations include:

Seek Ordering — The KDB50 uses its command buffer to look ahead into each disk drives workload and select the outstanding request that will result in the optimal seek from the disk drive's current position. In a heavily loaded subsystem, seek ordering can result in performance improvements of up to 35 percent.

Overlapped Seeks — To maximize parallel drive operation, the disk port driver initiates all requested seeks before initiating any data transfers. This feature effectively results in more efficient utilization of the subsystem and higher overall throughput. It is not necessary to wait for one drive to seek, transfer, and release the channel before giving another drive a seek command. The result is that multiple drives are placed on cylinder and on track, and are prepared to transfer data.

Rotational Optimization — As with conventional controllers, the KDB50 has one drive-to-controller data-transfer channel. Unlike conventional controllers, however, the KDB50 dynamically allocates this channel to the on-cylinder drive whose targeted starting sector is closest to the read/write heads. This feature, when combined with overlapped seeking, minimizes average rotational latency in multidrive subsystems and sustains effective and efficient throughput.

The KDB50 connects directly to the VAXBI providing the fast burst data rates needed to support high-throughput requirements. High I/O throughput applications run over 33 percent faster than on a comparably configured VAX-11/750 with a UDA50. With improved I/O performance, VAXBI systems can respond to requests more quickly and move on to the next task. The result is better overall systems performance, higher user satisfaction, and improved CPU utilization.

Device integrity and protection against loss of data is achieved via bad block replacement,* automatic revectoring to replaced blocks, the industry's most extensive error correction code (ECC) and error detection code (EDC). (The KDB50's 170-bit Read-Solomon ECC can correct up to eight 10-bit bursts in a single sector, compared to the single 11-bit burst correction power of more commonly used ECC. A unique feature of all SDI subsystems, EDC verifies ECC computation logic and the ECC correction process, checks controller data paths, and indicates a forced error in the rare event that an uncorrectable media error causes sector replacement.) The KDB50's extensive data protection capabilities also include multiple sector headers to verify read/write head position prior to data transfers, single point failure detection, and extensive self-testing capabilities.

The KDB50 disk controller *performance specifications* are as follows:

- Instantaneous transfer rate: 3.0 Mbytes/s maximum
- Steady state throughput: 1.0 Mbytes/s sustained
- Multiple controller throughput: 2.0 Mbytes/s sustained (2 × KDB50)
- Number of drives supported: 4

* The replacement blocks are not part of the total user-accessible disk capacity, so no shrinkage of available disk occurs because of bad blocks. This feature requires operating system support. Check appropriate Software Product Descriptions for versions and releases.

▪ Tape Storage Media Devices

Digital provides a complete series of industry-compatible magnetic tape devices to operate with the UNIBUS, Q-bus, and VAXBI bus on VAX systems and with the HSC50 and HSC70 intelligent controllers in VAXcluster Systems. The magnetic tape devices provide reliable medium- and high-density backup storage for Digital's disk storage devices.

TA81 Tape Storage Device

Offering midrange price and performance, the streaming tape TA81 is one of Digital's two dual-density HSC-based magnetic tape subsystems. The other is the high-performance, top-of-the-line TA78 system described in the *VAX Hardware Handbook Volume 1–1986*. The TA78 and the TA81 can be mixed on the same interface module, both acting as shared resources, available to users anywhere in the cluster.

Efficient design allows the TA81 with its integrated formatter to be compactly packaged in a single waist-high (41.6 inches high by 21.3 inches wide by 30.0 inches deep) cabinet with room for a disk drive in the same cabinet for a fully integrated disk and tape subsystem. An HSC5/5X-CA interface can support four TA81s.

The TA81 conforms to the ANSI standard for group code recording (6,250 bits per inch) and for phase-encoded recording (1,600 bits per inch) on half-inch, nine-track tape. It's engineered for high reliability and offers outstanding data integrity. Read-after-write verification ensures that each bit written is verified immediately after it is recorded. Vertical parity is checked, character-by-character, when reading and writing. Data integrity is ensured further by recording error correction code (ECC) and cyclic redundancy check (CRC) characters on the tape when in GCR mode. The TA81 tape system uses this information to make both single- and double-track error correction without CPU intervention.

With its streaming tape technology, the TA81 is ideal for applications involving sustained input/output such as high-capacity disk backup, or recording from high-speed test equipment. In backup mode, the TA81 tape system performs up to 50 percent faster than TU81s. Under VMS BACKUP, selection of optimized switch settings can provide up to 100 percent performance improvement over BACKUP performance using default settings when recording in GCR mode. The TA81 tape drive can also use traditional start/stop technology for slower data transfers. However, heavy transaction processing applications are better served by the high-speed TA78 subsystem.

Designed for simplified maintenance and ease of service, the TA81 has built-in diagnostic software and allows rapid access to all field-replaceable modules. The TA81 requires no adjustment or preventive maintenance except for routine, customer-performed head cleaning. At powerup, the tape subsystem runs self-test diagnostics and reports any detected problem so that it can be corrected before the drive is needed. In the unlikely event of unrecoverable error, the TA81 subsystem alerts the HSC Server. Run offline without CPU involvement, diagnostic software in both the TA81 and the HSC can be used to locate the problem with minimal impact on cluster operation.

For ease-of-use, the TA81 has a short (13-inch) tape path for fast manual loading, and all operator controls are conveniently located on the front panel.

The TA81 tape storage device *performance specifications* are as follows:

- Read/write speeds:
  - > Streaming — 25 and 75 ips
  - > Start/stop — 25 ips
- Data transfer rate: 468 Kbytes/s (maximum)
- Rewind speed: 192 ips (average)
- Rewind time (2400-foot tape): 150 seconds

The *media specifications* are as follows:

- Recording medium: 0.5-in magtape (ANSI Standard)
- Number of tracks: 9
- Recording method:
  - > GCR–ANSI Standard X3.54-1976
  - > PE–ANSI Standard X3.39-1973
- Recording density:
  - > GCR–6,250 bpi
  - > PE–1,600 bpi
- Capacity:
  - > GCR–140 Mbytes
  - > PE–40 Mbytes
- Transports: includes transport and formatter (no slave drives are supported)

TU81-Plus Tape Storage Device

The TU81-Plus is the only industry-compatible tape drive offered for Digital's new VAXBI-based systems running in native mode. A 256-Kbyte cache buffer significantly improves tape streaming performance on most VAX systems. Because both commands and data are buffered, the TU81-Plus operates at peak streaming speed more often, while reducing the frequency of *reposition hits* caused within the command reinstruct process. When the software selectable buffer is in operation, data is read into and out of the cache, allowing both the host processor and the tape drive to optimize their individual data transfer rates. Further optimizing performance, the TU81-Plus automatically selects speeds of 25 and 75 inches per second for streaming operations, and up to 25 inches per second for start and stop operations.

Efficient design allows the TU81-Plus and an RA-series disk drive to be packaged in a single waist-high cabinet. This disk/tape drive combination provides a compact, quiet, and fully integrated storage subsystem. The tape subsystem easily connects to a VAX processor through a shielded cable and a bus adapter. Mounting requires one quad slot. Two versions, a BI-Bus version and a UNIBUS version, are available.

The dual-density TU81-Plus conforms to the ANSI standard of 6,250 bits per inch for group coded recording (GCR) and 1,600 bits per inch for phase encoding (PE) on 0.5-inch, nine-track tape. The TU81-Plus can store up to 140 Mbytes on a standard 8-Kbyte, 2400-foot reel. The TU81-Plus requires no adjustments or preventive maintenance except for normal head cleaning. A simple 13-inch tape path for fast manual handling, and a membrane control panel with touch-sensitive switches also help to make the TU81-Plus convenient and easy to use.

With streaming tape technology and high-speed operation via prefetching of commands and data, the TU81-Plus is ideal for applications involving sustained tape input such as disk backup, data archiving, or recording data from high-speed test equipment. It also uses traditional start/stop technology for shorter data transfers of the type associated with journaling, transaction processing, and classical data processing.

The TU81-Plus offers exceptional reliability through a microprocessor-based servosystem, air bearings, gentle tape handling, and fewer mechanical parts. Character-by-character vertical parity at both densities, read-after-write verification, and automatic two-track error detection and correction (in GCR mode) during operation ensure data integrity. Self-test and diagnostics automatically check the drive and the controller for proper functioning each time the TU81-Plus is powered on and during rewind and, if a malfunction occurs, the TU81-Plus has extensive diagnostics for prompt failure isolation and identification.

The *performance specifications* of the TU81-Plus are as follows:

- Read/write Speeds:
  - > Streaming–75 and 25 ips
  - > Start-stop–25 ips
- Data transfer rate: 468 Kbytes/s (maximum)
- Capacity:
  - > GCR–140 Mbytes
  - > PE–40 Mbytes (8 Kbyte size)
- Rewind speed: 192 ips
- Rewind time: 150 seconds
- Cache buffer: 256 Kbytes, software selectable

The *media specifications* are as follows:

- Recording method:
  - > Tracks–9
  - > GCR–ANSI Standard X3.54-1976
  - > PE–ANSI Standard X3.39-1973
- Recording medium: 0.5-in ANSI Standard magnetic tape
- Recording Density:
  - > GCR–6,250 bpi
  - > PE–1,600 bpi
- Record length: variable to 64 Kbytes

Appendix A ▪ VAX Processor Specifications

▪ VAX 8200 Processors

Processor Type	
Cycle time	200 ns
Control store size	15 Kwords by 40 bits ROM, plus 1 Kword by 40 bits RAM
Internal data path	32 bits
Instruction buffer size	8-byte lookahead
Maximum system I/O rate	13.3 Mbytes/s
Cache memory	8 Kbytes
VAX Instruction Set	
Number of 32-bit registers	16
Number of basic operations	304
Number of priority interrupt levels	32
Number of addressing modes	9
Data types supported	Integer, floating point (D, F, G, and H), packed decimal, character string, variable bit fields, and numeric strings
Main Memory	
Virtual address capacity	4 Gbytes
Physical expansion capacity	24 Mbytes in 2- and 4-Mbyte increments
Error correcting code	7 bits/longword
Memory cycle times	
Octaword (128 bits) read	1.6 μs
Octaword write	1.2 μs
Longword (32 bits)read	1.0 μs
Longword write	600 ns
Operating Environment	
Temperature	
RX50 disk drive not in use	10°C to 40°C (50°F to 104°F)
RX50 disk drive in use	15°C to 32°C (59°F to 90°F)
Relative humidity	
RX50 disk drive not in use	10 to 90% noncondensing
RX50 disk drive in use	20 to 80% noncondensing
Maximum altitude	2,438 m (8,000 ft)
Maximum heat dissipation	6.08 MJ/h (5.76 kBtu/h)

Processor Power Requirements	
Line voltage	
60 Hz	120 V
50 Hz	240 V
Phases	1
Maximum ac power consumption	1.69 kW
Surge current	100 A
Physical Characteristics	
Weight (maximum)	250 kg (550 lb)
Height	106 cm (42 in)
Width	54 cm (22 in)
Depth	81 cm (32 in)
Area	0.44 m^2 (4.89 ft^2)

▪ VAX 8300 Processor

Processor Type	
Cycle time	200 ns
Control store size	15 Kwords (40-bits/word) of ROM per processor, plus 1 Kword (40-bits/word) of RAM per processor
Internal data path	32 bits
Instruction buffer size	8-byte lookahead/processor
Maximum system I/O rate	13.3 Mbytes/s
Cache memory	8 Kbytes/processor
VAX Instruction Set	
Number of 32-bit registers	16/processor
Number of basic operations	304
Number of priority interrupt levels	32
Number of addressing modes	9
Data types supported	Integer, floating point (D, F, G, and H), packed decimal, character string, variable bit fields, and numeric strings
Main Memory	
Virtual address capacity	4 Gbytes
Physical expansion capacity	24 Mbytes in 2- and 4-Mbyte increments
Error correcting code	7 bits/longword
Memory cycle times	
Octaword read	1,600 ns
Longword write	600 ns

Operating Environment	
Temperature	15°C to 32°C (59°F to 90°F)
Relative humidity	20 to 80% noncondensing
Maximum altitude	2,438 m (8,000 ft)
Maximum heat dissipation	6.08 MJ/h (5.76 kBtu/h)
Processor Power Requirements	
Line voltage	
60 Hz	120 V
50 Hz	240 V
Phases	1
Maximum ac power consumption	1.69 kW
Surge current	100 A
Physical Characteristics	
Weight (maximum)	260 kg (572 lb)
Height	106 cm (42 in)
Width	54 cm (22 in)
Depth	81 cm (32 in)
Area	0.44 m^2 (4.89 ft^2)

▪ VAX 8500 and VAX 8550 Processors

Processor Type	
Cycle time	45 ns
Writable control store size	16 Kwords (144-bits/word)
User accessible control store	1 Kword (144-bits/word)
Internal data path	32 bits
Instruction buffer size	16-byte lookahead
Maximum system I/O rate	16 Mbytes/s
Cache memory	64 Kbytes
VAX Instruction Set	
Number of 32-bit registers	16
Number of basic operations	304
Number of priority interrupt levels	32
Number of addressing modes	9
Data types supported	Integer, floating point (D, F, G, and H), packed decimal, character string, variable bit fields, and numeric strings
Main Memory	
Virtual address capacity	4 Gbytes
Physical expansion capacity	80 Mbytes
Error correcting code	7 bits/longword
Memory cycle times	
Hexword (256 bits) read	Max. 1260 ns, min. 495 ns
Octaword (128 bits) write	Max. 540 ns, min. 270 ns
Longword (32 bits) write	Max. 495 ns, min. 135 ns

Operating Environment	
Temperature	15°C to 32°C (59°F to 90°F)
Relative humidity	10 to 90% noncondensing
Maximum altitude	2,438 m (8,000 ft)
Maximum heat dissipation	12.66 MJ/h (12.00 kBtu/h)
Processor Power Requirements	
Line voltage	
60 Hz	208 V
50 Hz	240 V
Frequency tolerance	
60 Hz	59 to 61 Hz
50 Hz	49 to 51 Hz
Phases	3 (A,B,C)
Maximum ac power consumption	3.2 kW
Physical Characteristics	
Weight	295 kg (650 lb)
Height	152 cm (60 in)
Width	68.5 cm (27 in)
Depth	76.2 cm (30 in)
Area	0.5 m^2 (5.6 ft^2)

▪ VAX 8700 Processors

Processor Type	
Cycle time	45 ns
Control store size	16 Kwords (144-bits/word)
User writable control store	1 Kwords (144-bits/word)
Internal data path	32 bits
Instruction buffer size	16-byte lookahead
Maximum system I/O rate	30 Mbytes/s
Cache memory	64 Kbytes
VAX Instruction Set	
Number of 32-bit registers	16
Number of basic operations	304
Number of priority interrupt levels	32
Number of addressing modes	9
Data types supported	Integer, floating point (D, F, G, and H), packed decimal, character string, variable bit fields, and numeric strings

Main Memory	
Virtual address capacity	4 Gbytes
Physical expansion capacity	128 Mbytes
Error correction code	7 bits/longword
Memory cycle times	
Hexword (256 bits) read	Max. 1260 ns, min. 495 ns
Octaword (128 bits) write	Max. 540 ns, min. 270 ns
Longword (32 bits) write	Max. 495 ns, min. 135 ns
Operating Environment	
Temperature	15°C to 32°C (59°F to 90°F)
Relative humidity	10 to 90% noncondensing
Maximum altitude	2,438 m (8,000 ft)
Maximum heat dissipation	13.29 MJ/h (12.60 kBtu/h)
Processor Power Requirements	
Line voltage	
60 Hz	208 V
50 Hz	440 V
Frequency tolerance	
60 Hz	59 to 61 Hz
50 Hz	49 to 51 Hz
Power consumption	3.7 kW
Surge current	
60 Hz	500 A
50 Hz	250 A
Physical Characteristics	
Weight*	
60 Hz	668 kg (1474 lb)
50 Hz	802 kg (1769 lb)
Height	152 cm (60.5 in)
Width	188.0 cm (74.0 in)
Depth	76.2 cm (30.0 in)
Area	1.4 m^2 (15.5 ft^2)

▪ VAX 8800 Processors

Processor Type	
Cycle time	45 ns
Control store size	16 Kwords (144-bits/word)
User control store	1 Kword (144-bits/word)
Internal data path	32 bits
Instruction buffer size	16-byte lookahead
Maximum system I/O rate	30 Mbytes/second
Cache memory	64 Kbytes/processor

VAX Instruction Set	
Number of 32-bit registers	16
Number of basic operations	304
Number of priority interrupt levels	32
Number of addressing modes	9
Data types supported	Integer, floating point (D, F, G, and H) , packed decimal, character string, variable bit fields, and numeric strings
Main Memory	
Virtual address capacity	4 Gbytes
Physical expansion capacity	128 Mbytes
Error correction code	7 bits/longword
Memory cycle times	
Hexword (256 bits) read	Max. 1260 ns, min. 495 ns
Octaword (128 bits) write	Max. 540 ns, min. 270 ns
Longword (32 bits) write	Max. 495 ns, min. 135 ns
Operating Environment	
Temperature	15°C to 32°C (59°F to 90°F)
Relative humidity	10 to 90% noncondensing
Maximum altitude	2,438 m (8,000 ft)
Maximum heat dissipation (kernel)	28.22 MJ/h (26.75 kBtu/h)
Processor Power Requirements	
Line voltage	
60 Hz	156 to 220 Vrms
50 Hz	360 to 443 Vrms
Frequency tolerance	
60 Hz	59 to 61 Hz
50 Hz	49 to 51 Hz
Phases	3
Maximum ac power consumption	6.2 kW
Surge current	
60 Hz	500 A
50 Hz	250 A
Physical Characteristics	
Weight*	
60 Hz	705 kg (1555 lb)
50 Hz	836 kg (1849 lb)
Height	152 cm (60 in)
Width	188 cm (74 in)
Depth	76.2 cm (30 in)
Area	1.4 m^2 (15.5 ft^2)

*Weight is that of the FE and CPU cabinets and internal components only. The shipping container and console subsystem weight is not included.

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