DISK CONTROLLER 800741/0703/1900

MAINTENANCE

CONTENTS

ILLUSTRATIONS

1. GENERAL

1.01 This manual provides a physical and functional description and operating theory for effective field servicing of the dual density 5.25-inch and 8.0-inch Diskette Controller. This manual is applicable to the following:

(1) Main Disk Controller 800741

(2) Auxiliary Disk Controller 800703

(3) Auxiliary Disk Controller 801900

Features

1.02 The Disk Controller is supplied in a two-card set as a system component for Dynabyte 5.25-inch and 8.0-inch diskette storage systems. Features of this Controller include:

- Dynabyte S-100 Bus compatible.
- Single and double-density recording.
- Single density IBM 3740 soft-sector compatible.
- ROM bootstrap.
- Switch-optioned disk I/O port.
- Compatible with 5.25-inch and 8.0-inch media.
- Solder masked pc board.
- Each Disk Controller carries a 30-day warranty on parts and labor.
- Each Disk Controller printed circuit assembly (PCA) is burned in for a minimum of 72 hours.

1.03 Dynabyte maintains hardware and software compatability with the Dynabyte S-100 Bus only. The Disk Controller has the following hardware and software requirements:

(1) Z-80 Central Processor Unit (CPU). The software for the Disk Controller is written in Z-80 code.

(2) A 4 MHz clock rate from CPU.

(3) The RAM must operate without wait states

(4) PHANTOM* line must be enabled for RAM that occupies the memory address space from 0 to 256H.

The Disk Controller may not operate with all other S-100 Bus computers. Contact Dynabyte for specific applications.

2. PHYSICAL DESCRIPTION

2.01 The Dynabyte Disk Controller for 5.25-inch and 8.0-inch diskettes is implemented as two printed circuit assemblies (PCA)s.

Main Disk Controller

2.02 The Main Disk Controller, 800741, is an S-100 Bus card. Refer to Figure 2-1. This PCA measures 5 inches x 10 inches. A 100-pin edge connector mates with the S-100 Bus connector of the 5100/5200 Computer motherboard. This connector is offset by 5/8 inch from the pc board centerline, i.e., the Main Disk Controller cannot be inserted into a motherboard backwards.

2.03 Data, status and control signals are exchanged with the Auxiliary Disk Controller through a 50-conductor connector located along the top edge, Up to two auxiliary disk controllers may be connected.

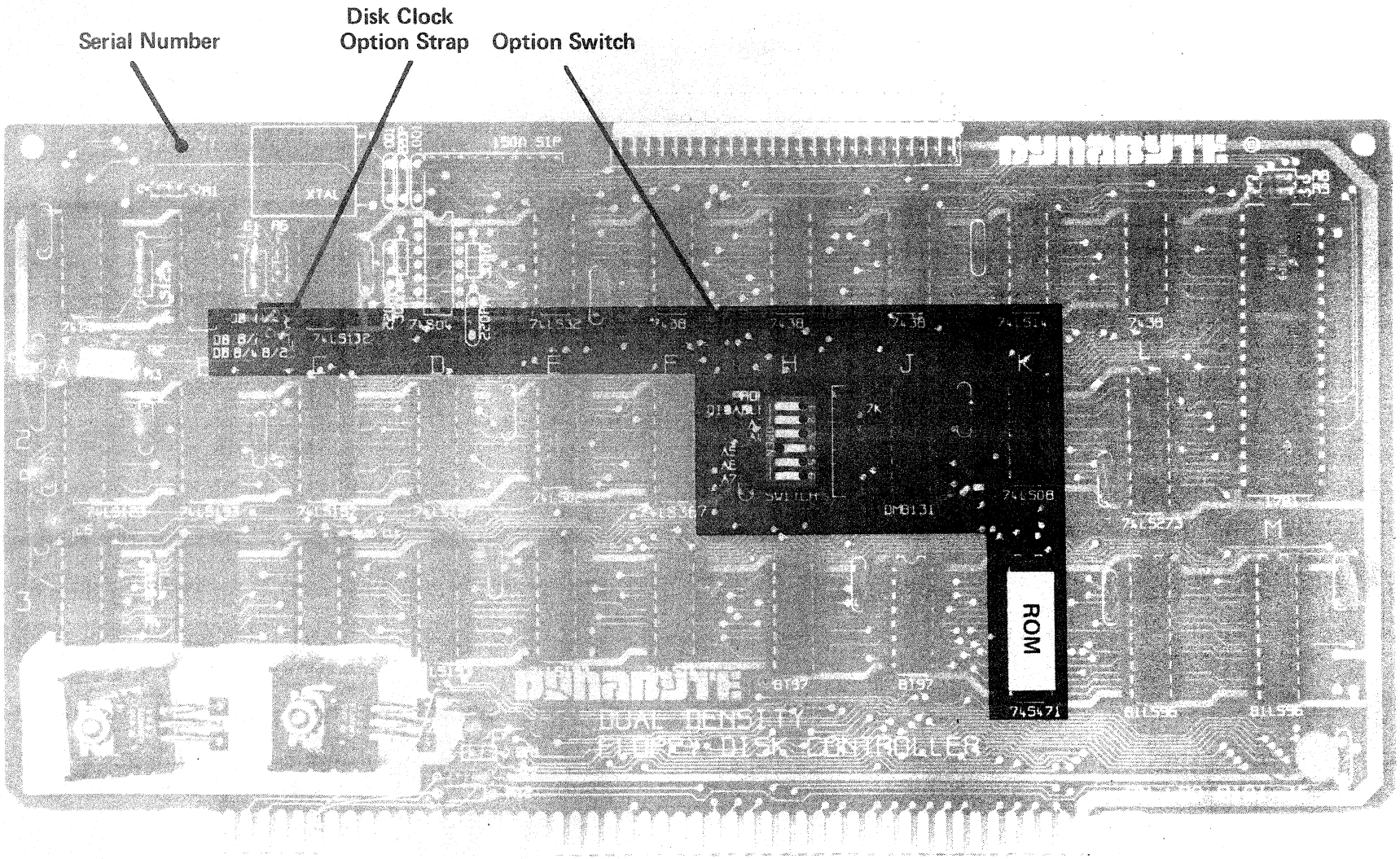


Figure 2-1 – Main Disk Controller – 800741

Table 2-1 – ROM Option Selection

Dynabyte Part Number	Mnemonic	Dynabyte Equipment
803952	RBOOT1A	5100 and 5010 Shugart 1D Drives, 5200 and 5010 Shugart 1D Drives, 5200 alone.
802033	RBOOT2	5100 and 5010 Remex 1D Drives, 5200 and 5010 Remex 1D Drives, 5200 alone.
802052	RBOOT3	5200 and 5010 Remex 2D Drives, 5200 and 5010 Remex 2D Drives, 5200 alone.
803971	RBOOT4A	5100 and two 5010 2D Drives.
804741	RBOOT5	5100 and two 5010 1D Drives.

Note:
(1) 1D is a single-surface diskette.
(2) 2D is a double-surface diskette.

Auxiliary Disk Controller

2.04 Two versions of Auxiliary Disk Controllers are available. Each has minor mechanical and electrical differences and measures 6.7 x 5.8 inches. The PCA mounts to the chassis on nylon retainers. Detents secure the PCA in place.

(1) The Auxiliary Disk Controller, 800703, is installed in the 5200 Computer Unit. Refer to Figure 2-2.

(2) The Auxiliary Disk Controller, 801900, is installed in the 5010 Dual Diskette Storage Unit. Refer to Figure 2-3.

2.05 The 50-conductor connector marked CONTROLLER INTERFACE exchanges data, status and control signals with the Main Disk Controller.

(1) Auxiliary Disk Controller, 800703, has a 34-conductor connector marked MINI DRIVE INTERFACE through which data, status and control signals are exchanged with two 5.25-inch diskette drives.

(2) Auxiliary Disk Controller, 801900, has a 50-conductor connector marked FULL SIZE DRIVE INTERFACE through which data, status and control signals are exchanged with two 8.0-inch drives.

2.06 Distinctive white silkscreened marking has been provided on the component side of the PCA.

(1) The card name, Dynabyte part number and a location for the serial number have been marked on the board. Some early controllers have the serial number etched on the pc board.

(2) Component reference designators are marked where practical. They facilitate locating the individual part on the schematic or replaceable parts list. Refer to Part 7.

The Main Disk Controller, integrated circuits and some major components derive their reference designators from the row-column matrix silk-screened onto the pc board. Refer to Figure 2-1. Columns are A to M and Rows are 1 to 3. An integrated circuit located at the lower right corner is M3. The Auxiliary Controller follows a similar convention.

2.07 The Main Disk Controller has two on-board regulators.

(1) U01 provides +5 Vdc and is provided with an insulated heat sink.

(2) U02 provides +5 Vdc and is provided with an insulated heat sink.

If it becomes necessary to change one of these regulators, coat the mating surfaces with a thermal conductive cream. Secure the regulator to the surface with a screw and nut.

NOTE

The PCA should never be inserted or removed from the bus when the ac line is connected to the computer.

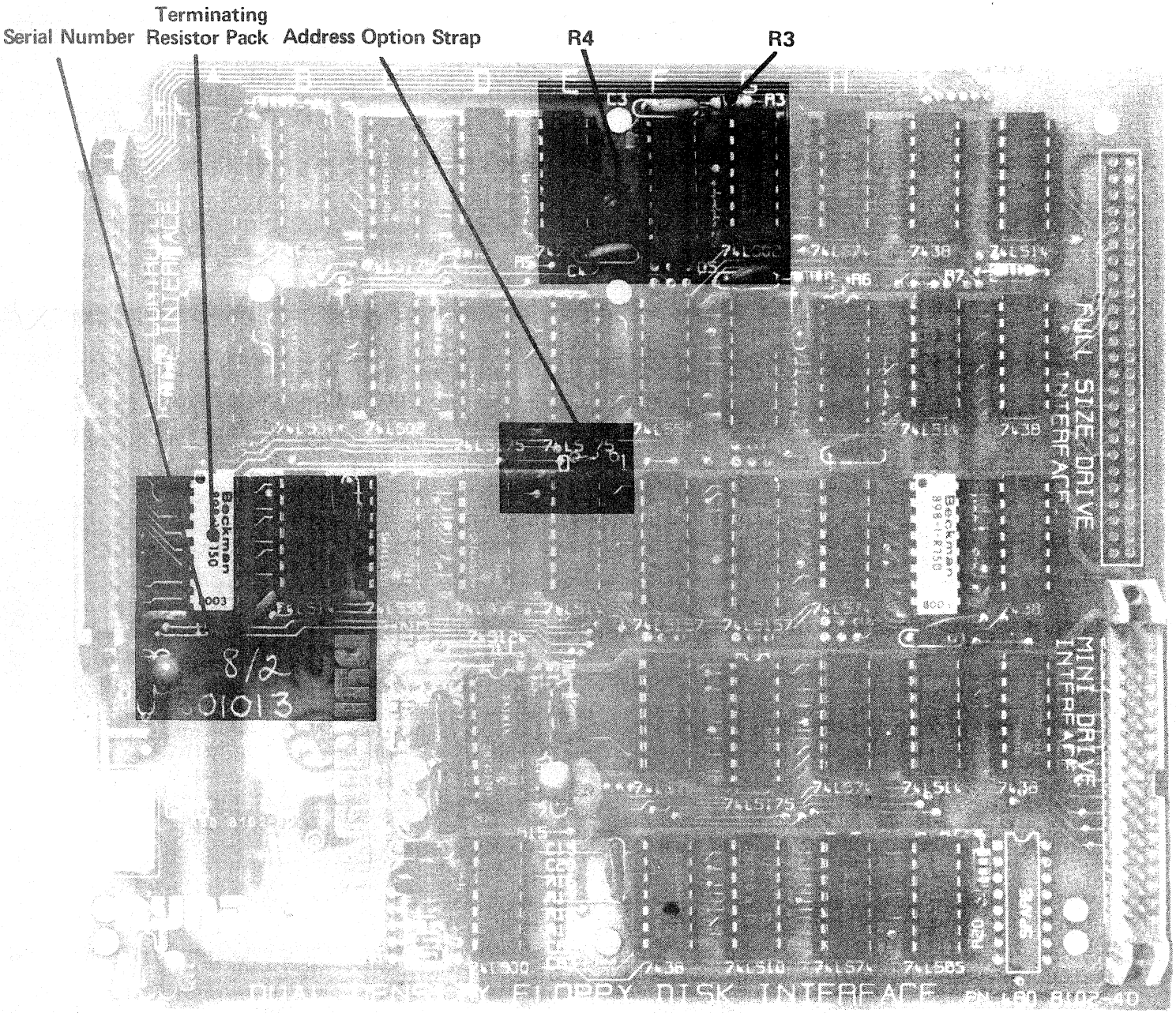


Figure 2-2 – 5200 Auxiliary Disk Controller – 800703

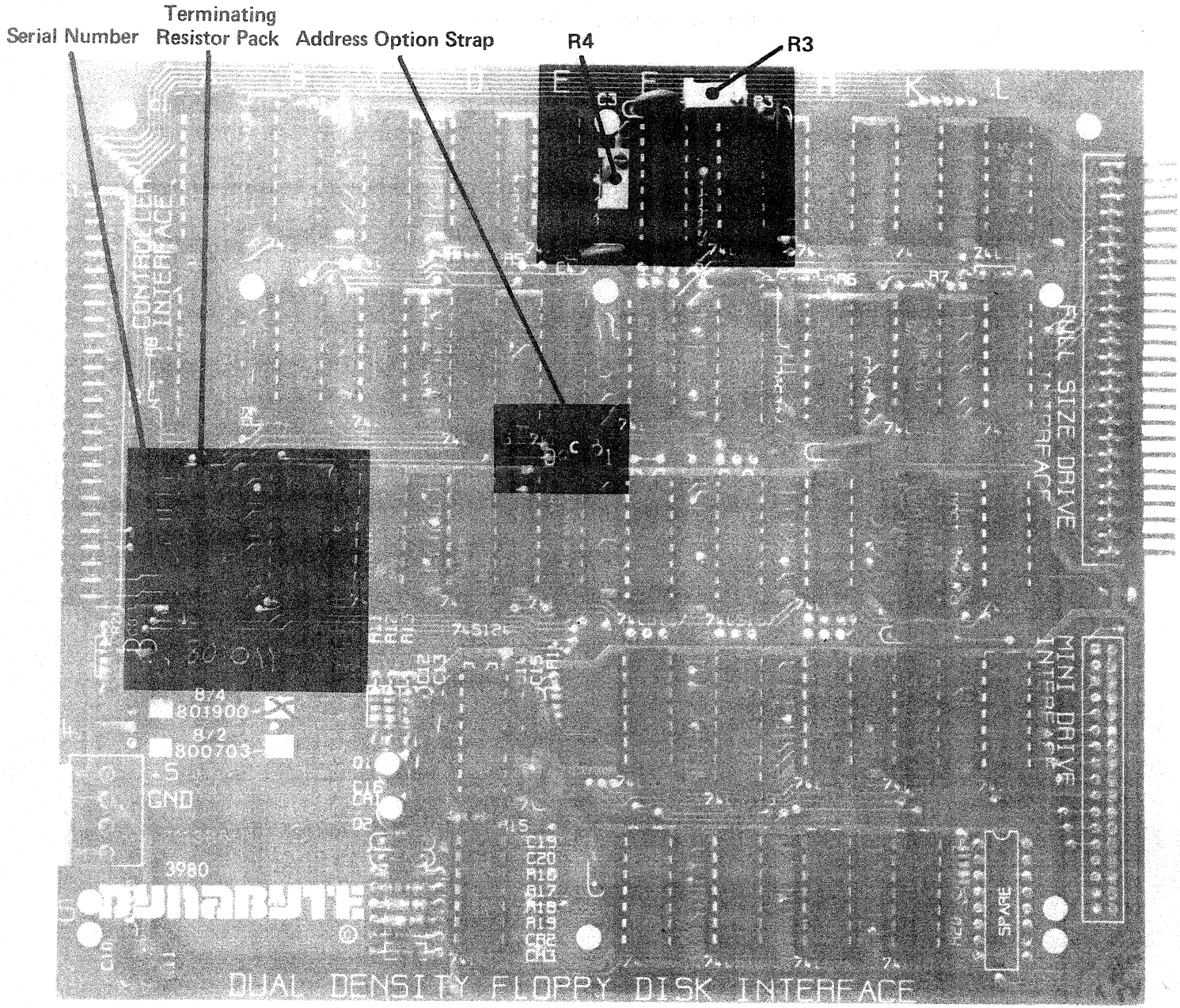


Figure 2-3 – 5010 Unit Auxiliary Disk Controller – 801900

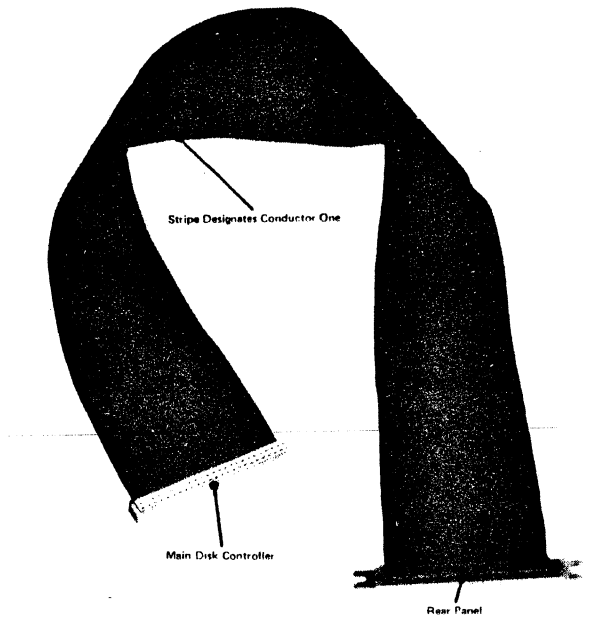


Figure 2-4 – 5100 Disk I/O Cable – 800228

Disk I/O Cables

2.08 The data, status and control signals are exchanged between the Main Disk Controller, Auxiliary Disk Controller and diskette drives through flat multi-conductor I/O cables. All appear similar. Figures 2-4 through 2-9 illustrate each.

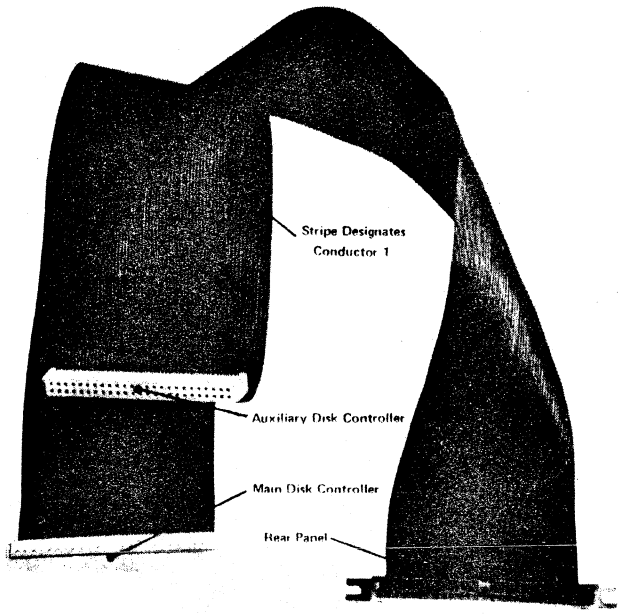


Figure 2-5 – 5200 Disk I/O Cable – 800247

2.09 *5100 Disk I/O Cable* illustrated in Figure 2-4 interconnects the Main Disk Controller to the 5100 Computer Unit rear panel. This cable extends the Disk I/O signals up to two external Auxiliary Disk Controllers, e.g., 5010 Units. This cable has 50 conductors and is 21 inches long.

2.10 *5200 Disk I/O Cable* illustrated in Figure 2-5 interconnects the Main Disk Controller to the 5200 Computer Unit rear panel and Auxiliary Disk Controller in the 5200 chassis. The cable extends the I/O signals to one additional Auxiliary Disk Controller, e.g., a 5010 Unit. This cable has 50 conductors and is 28 inches long.

2.11 *System Disk I/O Cables* illustrated in Figures 2-6 and 2-7 interconnect the 5100/5200 Computer Unit with one or two 5010 Units.

(1) System Disk I/O Cable, 800893, is used to interconnect a 5100/5200 and one 5010 Unit. This cable has 50 conductors and is 70 inches long.

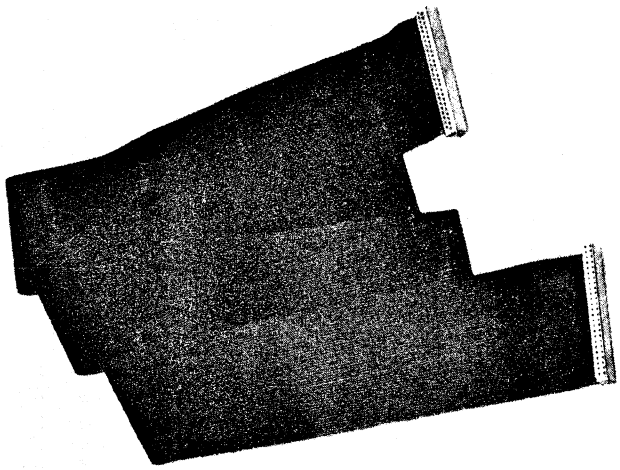


Figure 2-6 – System Disk I/O Cable – 800893

(2) System Disk I/O Cable, 804475, is used to interconnect a 5100 Computer Unit and two 5010 Units. This cable has 50 conductors and is 167 inches long.

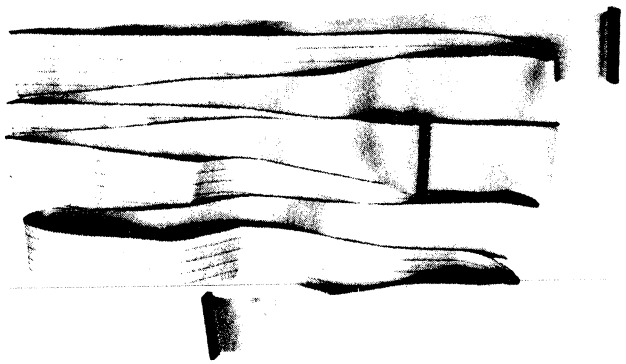


Figure 2-7 – System Disk I/O Cable – 804475

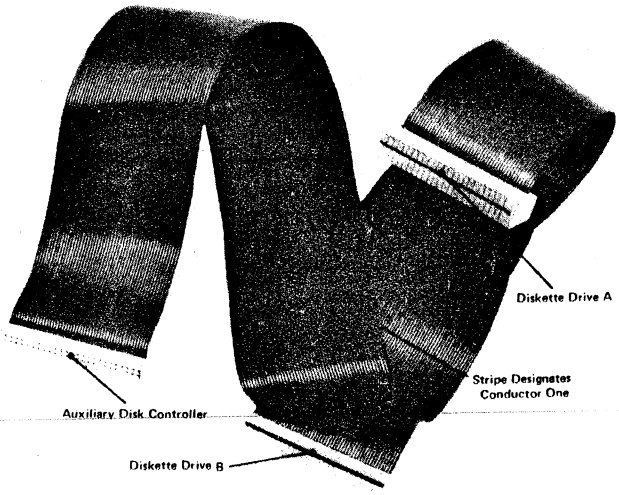


Figure 2-9 – 8–Inch Disk I/O Cable – 800855

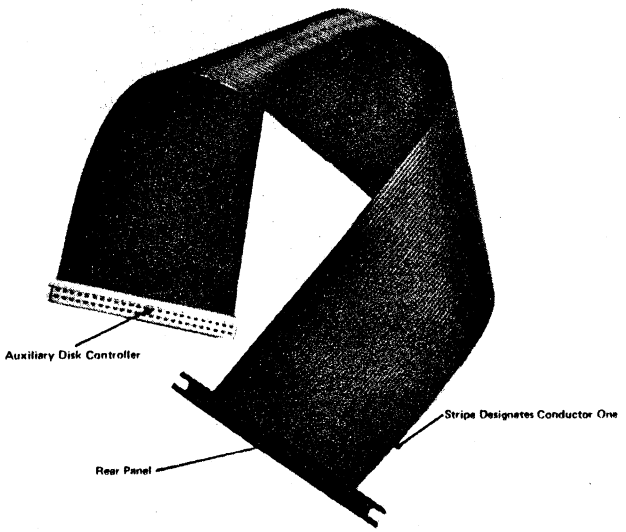


Figure 2-8 – 5010 Unit Disk I/O Cable – 801782

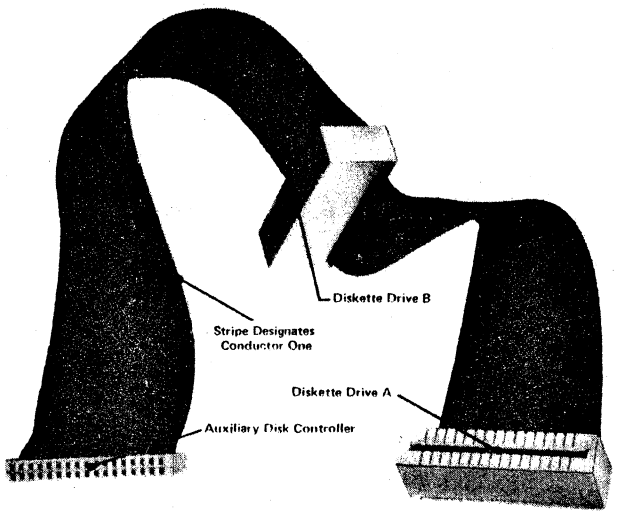


Figure 2-10 – 5.25-Inch Disk I/O Cable – 800437

2.12 *5010 Unit Disk I/O Cable* illustrated in Figure 2-8 interconnects the 5010 Unit rear panel with the Auxiliary Disk Controller in the 5010 Unit chassis. This cable has 50 conductors and is 14 inches long.

2.13 *8-Inch Disk I/O Cable* illustrated in Figure 2-9 interconnects the Auxiliary Disk Controller with the 8.0-inch disk drives. This cable has 50 conductors and is 44 inches long.

NOTE

Dynabyte terminates the striped conductor at connector Pin 1 on I/O cables. Frequently a . (dot) is painted on each mating connector to insure correct polarization.

2.14 *5.25-Inch Disk I/O Cable* illustrated in Figure 2-10 interconnects the Auxiliary Disk Controller with the 5.25-inch drives. This cable has 34 conductors and is 14 inches long.

Options

2.15 The six-position DIP switch on the Main Disk Controller performs two functions:

(1) Position 1 ROM Disable — Normally this is closed and enables the Bootstrap ROM located at position K3 on the pc board.

(2) Positions 2 through 6 set the decoding for the upper five I/O port bits. Normally these are factory set to all closed except position 4. This sets the Disk Controller I/O ports to 20H through 25H for Dynabyte Operating Systems. The first four ports are used by the LSI Controller integrated circuit at position M1. The last two ports are used for special control functions on the Main Disk Controller.

2.16 A Disk Clock Strap Option located at C1 sets the clock rate to the Auxiliary Disk Controller.

(1) Position DB8/4 sets the clock rate permanently for 8.0-inch drives.

(2) Position DB8/2 sets the clock rate permanently for 5.25-inch drives.

(3) Position DB8/4 8/2 switches the clock rate following the drive select line.

Normally this is factory strapped to the last position.

2.17 The ROM Bootstrap located at K3 contains a firmware subroutine which is phantomed into RAM when a RESET is issued from the 5100/5200 Computer Unit.

3. FUNCTIONAL DESCRIPTION

3.01 The basic function of a Disk Controller is to provide the control electronics necessary for reading and writing data to a diskette.

Diskette Storage

3.02 The Disk Controller stores files and programs on media which is made up of a 0.762 mm (0.003 inch) polyester disk and is enclosed in a matte vinyl jacket. The entire assembly is called a diskette or colloquially, a floppy disk. The polyester disk substrate is coated on both sides with 2.54 μm (100 microinch) ferrous oxide similar to that found on audio tape. The diskette is flexible and is intended to deform slightly as the revolving disk is pressed onto the surface on the read/write head in the disk drive.

3.03 The Operating System divides the available read/write area on the diskette into tracks or concentric circles. Individual tracks are further subdivided into sectors.

(1) 5.25-inch diskettes are organized into 77 tracks numbered 00H to 4CH. Each track has 32 double-density (DD) sectors.

(2) 8.0-inch diskettes are also organized into 77 tracks numbered 00H to 4CH. Each track has 26 single-density (SD) or 54 double-density (DD) sectors.

Information may be stored on one surface (1D) or both surfaces (2D) of a diskette. 2D storage requires drives with two read/write heads. The total storage capacities for 1D and 2D operation are tabulated in Part 4.

3.04 The disk formatting operation prerecords track and sector information onto the disk. The sector locations are determined logically or soft sectored. A single index hole in the disk is monitored by the disk drive electronics. An INDEX pulse is furnished to the Auxiliary Disk Controller each time the disk starts a new revolution. The diskette can then be accessed randomly by the Disk Controller for read/write operations.

3.05 Figures 3-1 and 3-2 illustrate the Main and Auxiliary Controllers in block diagrams and should be used in conjunction with the logic diagrams in Part 7 for the description which follows. Table 3-1 tabulates the S-100 Bus signals used by the Disk Controller.

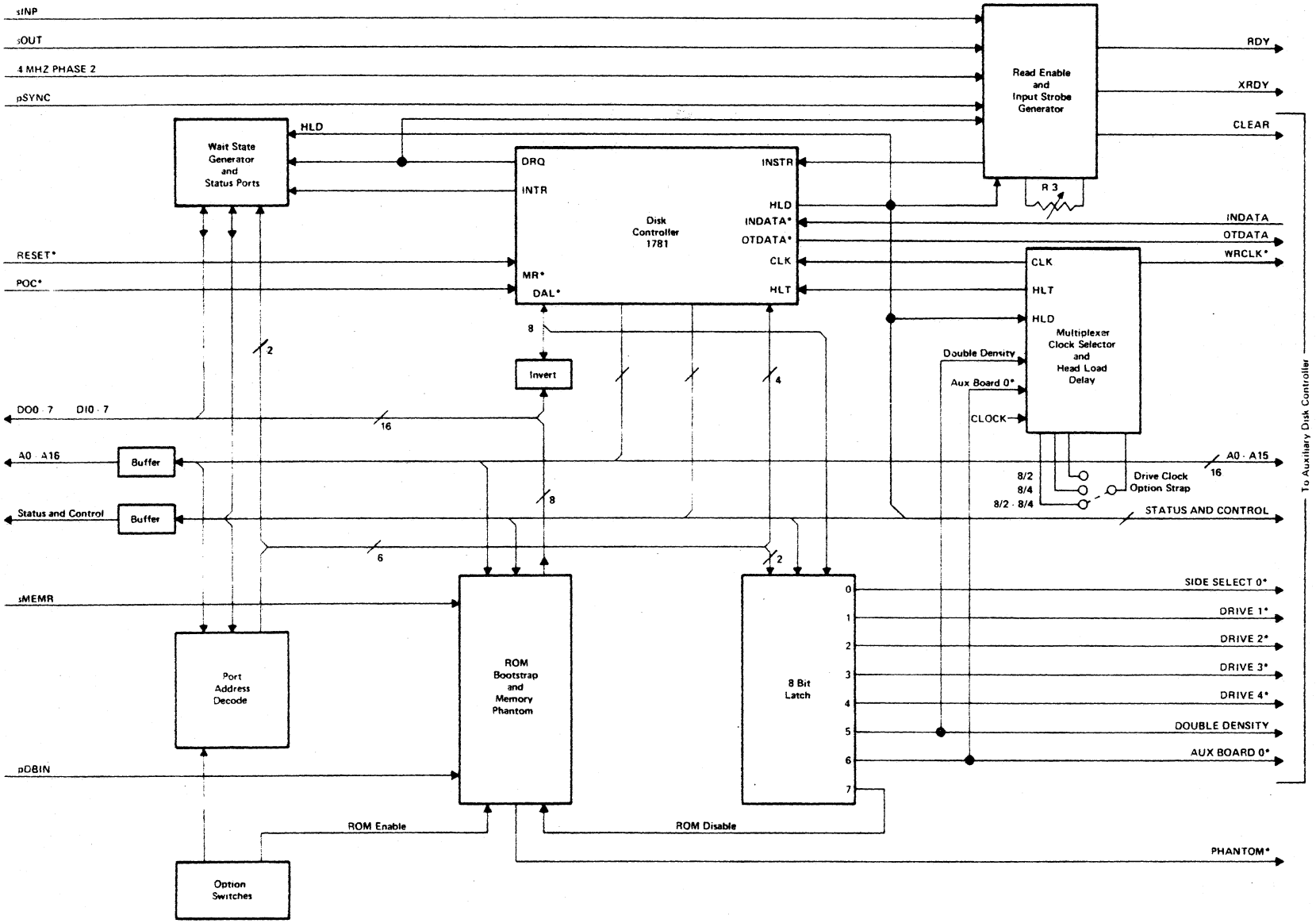


Figure 3-1 – Main Disk Controller Functional Block Diagram

1781 Disk Controller Device

3.06 The principle element of the Disk Controller 800741/0703/1900 is a *1781 Disk Controller* large scale integrated (LSI) circuit. Part 7 provides the technical data sheet on this OEM device. The sheet furnishes detailed functional descriptions on:

(1) Organization of the registers, CRC Logic, ALU and Timing/Control.

(2) Processor Interface.

(3) Diskette Interface.

(4) Head Positioning, Disk Read Operation.

(5) Disk Write Operation.

(6) Command Description and Flow Charts.

(7) Formatting the Disk.

(8) IBM 3740 Format.

(9) Non-IBM Formats.

This manual will confine its functional descriptions to the Main and Auxiliary Controller elements.

3.07 The main data transfer function performed by the *1781 Disk Controller* is to convert 8-bit parallel DAL* to serial OTDATA on write operations and serial INDATA to 8-bit parallel DAL* on read operations. Figure 7-4 details the function of each device line. Figure 3-1 summarizes and illustrates the most significant of these lines. Drive control lines have been omitted.

(1) Master Reset (MR*) is a logic low from RESET* or POC* and resets the *1781 Disk Controller* clearing the command register. The Not Ready, Status Bit 7, is reset when MR* is active.

(2) Data Access Lines (DAL*) is an eight bit inverted bi-directional bus used for transfer of data, control and status.

(3) Data Request (DRQ) performs two functions. It indicates the data register contains assembled data in read operations or the register is empty in write operations. The DRQ is reset when the CPU reads or loads the register.

(4) Input Strobe (INSTR) indicates INDATA is valid.

(5) Input Data (INDATA) is the date line from drive and is valid when INSTR is active.

(6) Output Data (OTDATA) is the date line to drive and is valid when OTSTR is active.

(7) Head Load (HLD) output controls the loading of the Read-Write Head against the media. The HLT input is sampled every 10 ns. When a logic high is detected on the HLT input, the head is assumed to be engaged.

(8) Head Load Timing (HLT) signal is generated by a multivibrator in the *Head Load Delay* since the drive does not furnish this signal when the media is engaged.

(9) Clock (CLK) is the internal time reference for the *1781 Disk Controller.*

Addressing

3.08 Data transfers are performed by programmed I/O. Five of the *Option Switch* positions set the Disk Controller address for the *Port Address Decode*. Dynabyte Disk Operating Systems use Ports 20H through 25H for the Disk Controller.

(1) Ports 20H to 23H are used by the *1781 Disk Controller* for I/O operations. These correspond to the 1781 I/O Ports 0 — 3 and their functions are described in Figure 7-4 under Processor Interface.

(2) Ports 24H and 25H are used by the other elements of the Disk Controller. Their functions are tabulated in Table 3-2.

Writing to Ports 24H and 25H set the individual *8-Bit Latch* functions.

(3) Side 0 SELECT* determines the surface accessed on 2D drives.

(4) DRIVE 1 through 4* determines the drive to be accessed. An Auxiliary Disk Controller is designed to support up to four drives. Dynabyte systems currently use only two drives per Auxiliary Disk Controller.

(5) DOUBLE DENSITY* determines the read/write mode.

Table 3-1 — Main Disk Controller S-100 Bus Signals

Name	Pin	Function
4 MHZ PHASE 2	24	The master timing signal for the bus.
A1 — A15	Various	Address Bit 1 through Address Bit 15.
CLOCK	49	2 MHz (0.5%) 40% — 60% duty cycle. Not required to be synchronous with any other bus signal.
DI0 — DI7	Various	Data In Bit 0 through Data In Bit 7.
DO1 — DO7	Various	Data Out Bit 0 through Data Out Bit 7.
PHANTOM*	67	A bus signal which disables memory during Disk Controller ROM access.
POC*	99	The Master Reset Signal. The Power On Clear signal for all devices. When this signal is low, it must stay low for at least 10 ms.
RESET*	75	Requests the reset of all bus master devices. Connects to the Front Panel Reset Switch and activates POC*.
XRDY	3	One of two ready inputs to the current bus master. The bus is ready when both these ready inputs are true. Sin Pin 72.
pDBIN	78	The control signal that requests data on the DI bus.
pSYNC	76	The control signal identifying the beginning of a processor cycle.
pWR*	77	The control signal signifying the presence of valid data on the DO bus.
RDY	72	See comment for Pin 3.
sINP	46	The status signal identifying the data transfer bus cycle from an input device.
sMEMR	47	The status signal identifying bus cycles which transfer data from memory to a bus master, which are not interrupt acknowledge instruction fetch cycle(s).
sOUT	45	The status signal identifying the data transfer bus cycle to an output device.

Table 3-2 – Disk Controller I/O Port 24H and 25H Function

Port	Name	Bit	Function
24H			STATUS
	HEAD LOAD	0	Indicates head is loaded.
		1—3	Not defined.
	INTRQ*	4	Indicates operation is complete.
		5—6	Not defined.
	INTRQ* or TIME OUT*	7	If this bit is active, the status of Bit 4 is read to determine if an operation is complete or timed out.
			CONTROL
	SIDE 0 SELECT*	0	Selects side (surface) 0.
	DRIVE 1*	1	Selects Drive 1.
	DRIVE 2*	2	Selects Drive 2.
	DRIVE 3*	3	Not Defined.
	DRIVE 4*	4	Not Defined.
	DOUBLE DENSITY*	5	Selects double density recording.
	AUX BOARD 0*	6	Selects Auxiliary Disk Controller 0.
	ROM ENABLE	7	Enables ROM Bootstrap.
25H			Status and control functions are similar to 24H except a wait state is generated.

(6) AUX BOARD 0* determines the Auxiliary Disk Controller addressed.

(7) ROM ENABLE provides for enabling the ROM Bootstrap phantoming operation during power on or reset. Refer to 3.09.

Reading from 24H and 25H furnished drive status, e.g., head loading.

Power On Clear – Reset

Each time the computer is powered on, the POC* line goes low clearing the CPU and the *1781 Disk Controller* through MR*. A similar function is performed when the operator keys the front panel RESET pushbutton. The *ROM Bootstrap* is overlaid into RAM starting at location 00H when the PHANTOM* line goes low. While the PHANTOM* is activated, all memory reads are from the *ROM Bootstrap*. An active PHANTOM* line does not inhibit writing to RAM however.

(1) The CPU reads the instructions starting at address 00H. These instructions direct the CPU to read Track 0, Sector 1, from Drive A. This particular operation is called the *ROM Bootstrap*.

(2) Track 0, Sector 1, is read. This sector contains additional instructions which are loaded into RAM for execution. This operation is called the *Disk Bootstrap*.

(3) The first two tracks, 0 and 1, contain the Operating System and are loaded from the top of RAM down.

(4) The CPU disables the *ROM Bootstrap* by setting Bit 7 of the *8-Bit Latch*.

(5) The PHANTOM* line goes high.

The *ROM Bootstrap* may also be optionally disabled by an option switch for special applications.

Timing

3.10 The *Wait State Generator* creates wait states by holding RDY or, optionally, XRDY lines low to the CPU. This element is necessary since the CPU can operate significantly faster than the *1781 Disk Controller*. Wait states are generated:

(1) During all I/O instructions to the *1781 Disk Controller*.

(2) During data transfer operations to insure synchronization.

Three Disk Controller timing functions are performed by the *Multiplexer Clock Selector And Head Load Delay*.

(3) Head Load Delay is performed by a multivibrator activated by HLD, the Head Load command. The multivibrator furnished HLT to the *1781 Disk Controller* after a period set to the drive head load time specifications. This is necessary since the drive does not furnish HLT when the head is in contact with the disk.

(4) The S-100 Bus CLOCK is counted down to generate WRCLK* the Write Clock, furnished to the drive.

(5) In addition S-100 Bus CLOCK is counted down to generate CLK to the *1781 Disk Controller*.

The AUX BOARD 0* line causes the multivibrator timing to change and both clock rates to change between 5.25-inch and 8.0-inch Disk Clock rates when the DB 8/2 8/4 Option Strap is in place. Refer to 3.13.

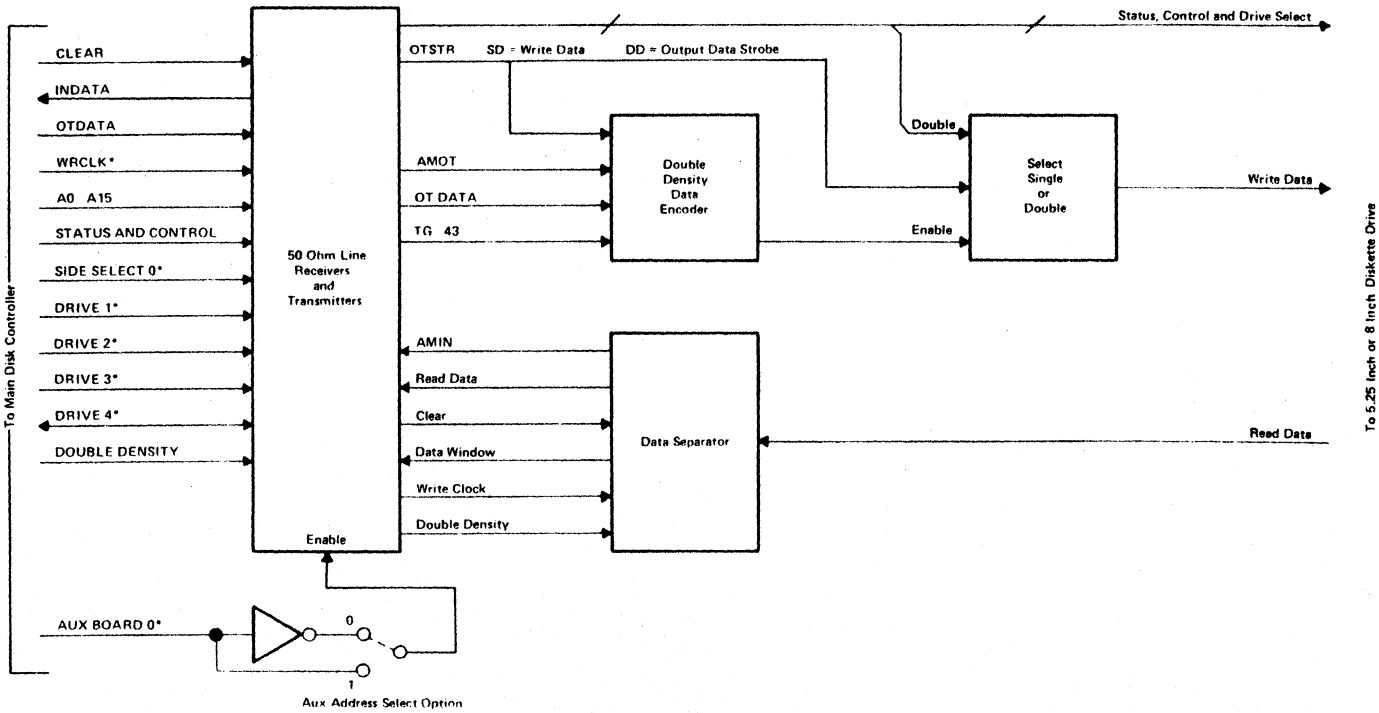


Figure 3-2 – Auxiliary Disk Controller Functional Block Diagram

Options

3.11 The Disk Clock Strap Options on the *Multiplexer Clock* Separator provide for the following:

(1) DB 8/2 sets the WRCLK* and CLK to the 5.25-inch diskette data rate. This is appropriate for a 5200 Computer Unit without a 5100 Unit connected.

(2) DB 8/4 sets the WRCLK* and CLK to the 8.0-inch diskette data rate. This is appropriate for a 5100 Computer Unit and one or two 5010 Units.

(3) DB 8/2 8/4 causes the WRCLK* and CLK to toggle between the 5.25-inch and 8.0-inch diskette data rates depending on which drive is selected. This is appropriate for a 5200 Computer Unit and 5010 Unit.

The *Bootstrap ROM*, discussed in 3.09, provides the Operating System with hardware system options for the particular system. For example:

(4) Number of disk drives,

(5) The sizes of the disk drives,

(6) Number of surfaces per disk drive.

The *Aux Select Option* strap determines whether the Auxiliary Disk Controller will be 0 or 1 in the disk storage system.

(7) The 5200 Auxiliary Disk Controller is normally strapped as 0. If a 5010 Unit is used in conjunction with a 5200 Computer Unit, the 5010 Auxiliary Disk Controller is strapped as 1.

(8) The first 5010 Auxiliary Disk Controller connected to a 5100 Computer Unit is strapped as 1 and the second 5010 Auxiliary Disk Controller is strapped as 0.

Read Operation

3.12 The Head Loaded, HLD, and a Data Request, DRQ, cause *Read Enable and Input Strobe Generator* to set CLEAR low initiating a read operation between the Auxiliary Disk Controller and the drive selected. When CLEAR high, the Auxiliary Disk Controller is in a passive mode and is not attempting to acquire data. It may be:

(1) Writing data to a drive, or

(2) Waiting to be accessed.

The Phase Lock Loop (PLL) within the *Data Separator* is locked on to the Write Clock while CLEAR is high. During a read operation, CLEAR is low. The PLL is locked to the drive Read Data Synchronization Field.

(3) When the *Data Separator* detects an address mark, AMIN is strobed high. The *1781 Disk Controller* acknowledges AMIN by holding CLEAR low. If an address field is not detected in a predetermined time interval, the CLEAR is set high.

(4) Data Window is the strobe indicating a data field is present.

(5) Read Data is output to the *1781 Disk Controller* as OTDATA for transfer to the CPU and RAM.

Write Operation – Single Density

3.13 In single density (SD) operation, the *1781 Disk Controller* encodes write data and outputs it to the Auxiliary Disk Controller. Also, in SD operation the OTSTR, Output Strobe, is Write Data which is gated through *Select Single or Double* without further processing.

Write Operation – Double Density

3.14 In double density (DD) operation, the *1781 Disk Controller* does not perform any encoding. OTDATA is write data in NRZ format strobed to WRCLK*.

(1) DOUBLE DENSITY line selects double in the *Select Single or Double*.

(2) AMOT high indicates Address Mark Out enabling Write Data to drive.

(3) OTDATA is encoded into double density MFM and strobed as Write Data to the drive by OTSTR.

(4) TG>43 enables precompensation circuits when the current addressed track is greater than 43.

4. SPECIFICATIONS

4.01 Table 4-1 summarizes the Disk Controller 800741/0703/1900 functional and physical performance specifications as a system unit. Minor deviations from these specifications which do not affect the Computer System operation are excluded from the Dynabyte, Inc., warranty.

4.02 Figure 7-3 includes the functional and physical performance specifications for the OEM Disk Controller integrated circuit.

Table 4-1 – Disk Controller 800741/0703/1900 Specifications

PARAMETER	CHARACTERISTIC
Main Disk Controller	
Controller Device	Western Digital FD1781
I/O Ports	20H through 25H
Mode	SD or DD
Capacity	Two Auxiliary Disk Controllers
Auxiliary Disk Controller	
Capacity	Two 1D/2D 5.25-inch or 8.0-inch drives
Format, SD	IBM 3470
, DD	Dynabyte Double Density
5.25-inch Media	Soft sectored
Heads, 1D	1
, 2D	2
Tracks Per Surface	77
Media, 1D	Dysan P/N 800439
, 2D	Dysan P/N 802067
Unformatted Capacity	
Surface, DD	480K Bytes
Formatted Capacity	
Sector Size, DD	128 Bytes
Sectors Per Track, DD	32
Surface, DD	315K Bytes
Transfer Rate, DD	250K Bytes per second
Encoding Method, DD	MFM
8-inch Media	Soft Sectored
Heads, 1D	1
, 2D	2
Tracks Per Surface	77
Media, 1D	Dysan P/N 800528
, 2D	Dysan P/N 800803
Unformatted Capacity	
Per Track, SD	5,212 Bytes
, DD	10,425 Bytes
Formatted Capacity	
Sector Size, SD	128 Bytes
, DD	128 Bytes
Sectors Per Track, SD	26
, DD	54

Table 4-1 – Disk Controller 800741/0703/1900 Specifications (Continued)

PARAMETER	CHARACTERISTIC
8-inch Media	
Formatted Capacity	
Surface, SD	256K Bytes
, DD	525K Bytes
Transfer Rate, SD	250K Bytes per second
DD	500K Bytes per second
Encoding Method, SD	FM
, DD	MFM
Main Disk Controller	
Power Requirements	
+16 Volt Bus	Regulated to +12 Vdc
+8 Volt Bus	Regulated to +5 Vdc
-16 Volt Bus	Regulated to -12 Vdc
Operating Temperature	10°C to 35°C (50°F to 95°F)
Dimension, Width	24.5 cm (10.0 inches)
, Depth	1.5 cm (0.6 inches)
, Height	12.7 cm (5.0 inches)
, Weight	215.5 g (7.6 ounces)
Auxiliary Disk Controller	
Power Requirement	
+5 Vdc	Supplied from chassis power supply.
Operating Temperature	10°C to 35°C (50°F to 95°F)
Relative Humidity	20% to 80%
Dimension, Width	17.0 cm (6.7 inches)
, Depth	14.7 cm (5.8 inches)
, Height	2.0 cm (0.8 inches)
, Weight	109.8 g (7.4 ounces)

Note:

(1) 1D single surface
2D double surface
SD single density
DD double density

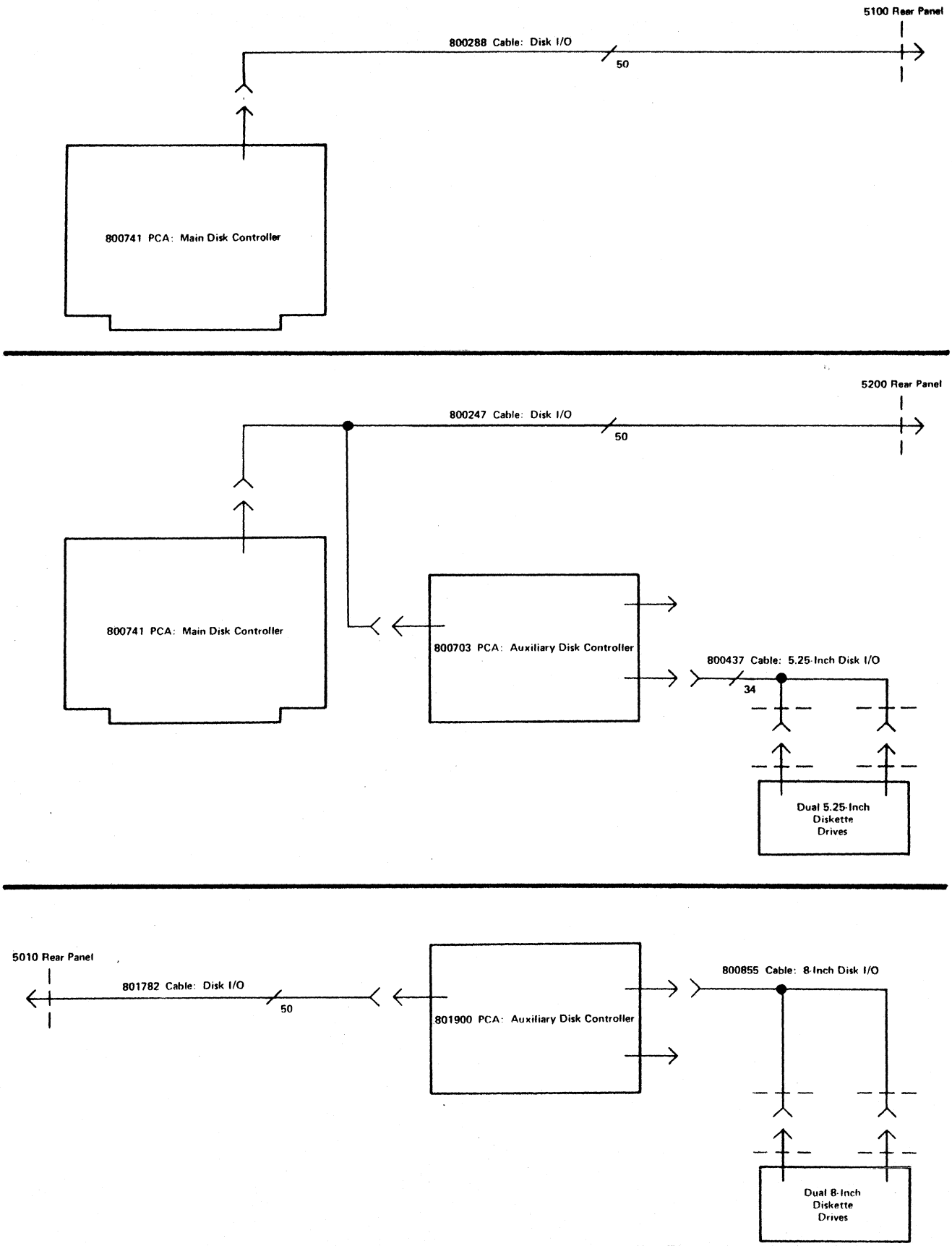


Figure 5-1 – I/O Cable Signal Paths Between Disk Controller Elements

5. INSTALLATION

)1 Refer to 5100/5200 Computer Unit Technical Manual for unpacking, inspection and return of material procedures. The Disk Controller is normally supplied as part of a Dynabyte Storage System. The following procedures are appropriate when replacing a Controller PC Assembly or I/O cable and will serve as a check list for installation.

Disk I/O Cables

5.02 Figure 5-1 illustrates the I/O Cable signal paths between Disk Controller elements. Part 2 illustrates each of these cables. A computer unit is connected to one or two Disk Storage Units with a System Disk I/O Cable.

NOTE

Always check to make certain the PCA options agree with the individual system equipment configuration before turning on the Dynabyte computer system.

ions

5.03 The basic controller design provides for various computer storage configurations through ROM, Switch and Strap Options on the Controller PC Assemblies.

5100/5010 Units

5.04 The following procedure will serve as an option check list when a 5100 Computer Unit and one or two 5010 Storage Units are used together or a single 5010 Unit is expanded to two 5010 Units.

STEP	PROCEDURE
1	For a 5010 Unit installation, check the Main Disk PC Assembly options: (1) Disk Clock Strap Option to DB8/4 8/2 position, (2) A ROM should be installed appropriate to drive manufacturer and number of surfaces. Refer to Figure 2-1 for the locations of these options.
2	Check the Auxiliary Disk Controller PC Assembly options for a single 5010 Unit installation: (1) Address Strap to 1, (2) Terminating resistor pack installed at A3.
3	For a two 5010 Unit installation, check the Main Disk Controller PC Assembly options: (1) Disk Clock strap option to DB8/4 position, (2) A ROM should be installed appropriate to drive manufacturer and number of surfaces. Refer to Figure 2-3 for the location of these options.
4	Check the Auxiliary Disk Controller PC Assembly options for a two 5010 Unit installation: (1) Unit 1 Address Strap to 0, (2) Unit 2 Address Strap to 1, (3) Unit 1 A3 vacant, (4) Unit 2 terminating resistor pack at A3. Refer to Figure 2-3 for the locations of these options.

5200 – 5200/5010 Units

5.05 The following procedure will serve as an option check list when a 5200 Computer Unit stands alone or is used with or expanded to include one 5010 Unit.

NOTE

Only one Terminating Resistor Pack should be installed in a Disk Storage System. The Resistor Pack should only be installed in the last Auxiliary Controller in the Disk Storage System.

STEP	PROCEDURE
1	For a stand-alone 5200 Computer Unit installation, check the Main Disk Controller PC Assembly options: (1) Disk Clock Strap Options to DB8/4 8/2 position. (2) A ROM should be installed appropriate to drive manufacture and number of surfaces. Refer to Figure 2-1.
2	If the system does not include a 5010 Unit, check the Auxiliary Disk Controller options in the 5200 Computer Unit: (1) Address Strap Option to 0, (2) Terminating Resistor Pack at A3.
3	If the system does include a 5010 Unit, check the Auxiliary Disk Controller PC Assembly options in the 5010 Unit: (1) Address Strap Option to 1, (2) Terminating Resistor Pack at A3.

5.06 The Main Disk Controller can be installed in any of the 12 card cage positions. As a matter of cabling convenience, it should be installed as shown in Figure 2-3 of the 5100/5200 Computer Unit Technical Manual.

STEP	PROCEDURE
1	Install the Main Disk Controller into the card cage. NOTE *The 50-conductor I/O cables are polarized with a stripe on conductor 1.*
2	Connect the Disk I/O Cable to the Main Disk Controller. Be sure the cable connector Pin 1 mates with Pin 1 silkscreened onto the Main Disk Controller PC Board.

6. MAINTENANCE

6.01 The Disk Controller 800741/0703/1900 is a result of several years of design, development and modern electronic manufacturing. The pc assembly is designed around the latest semiconductors and integrated circuits. All components operate at relatively low power. Each assembly is burned in at the Dynabyte factory for 71 hours before shipment. It can be expected to operate indefinitely.

6.02 No routine maintenance should be performed to the Main or Auxiliary Disk Controllers.

Customer Support Service

6.03 Maintenance and procedures described in this manual should be performed in accordance with local instructions and the individual user's maintenance plan. Maintenance and repair of the Disk Controller during the warranty period should be limited to returning the pc assembly to Dynabyte, Inc. The Dynabyte Customer Support staff is available by telephone for assistance in troubleshooting and recommendations for repairs. ... communications and material should be ...ected to:

DYNABYTE, INC.
Customer Support
521 Cottonwood Drive
Milpitas, CA. 95035
(408) 263-1221
Telex 346-359

The 5100/5200 Technical Manual, Part 6, outlines the procedure for returning material.

NOTE

Dynabyte Authorized Service Centers (ASC) are staffed with factory-trained technicians that are supplied with technical manuals and routinely receive service bulletins and design change information on Dynabyte equipment.

7. REFERENCE

Schematics and Replaceable Parts Lists

7.01 Figures 7-1, 7-2 and 7-3 will furnish the user with schematic diagrams of the Main and Auxiliary Disk Controller. Tables 7-1, 7-2 and 7-3 are replaceable parts lists of Main and Auxiliary Disk Controller pc assemblies indexed by reference designator appearing on the respective schematic. Enough information is furnished so the maintenance technician should be able to purchase replaceable parts from a local supplier or make a substitution if necessary. Disk Controller PC Assemblies, ROMs and I/O cables should be ordered directly from Dynabyte Customer Support Service.

Engineering Change Notices

7.02 Dynabyte makes changes to drawings and products through engineering change notices (ECN)s. Before a change to a product is approved or made:

(1) The implications to systems in the field are determined,

(2) Rework instructions are included for the equipment in the field when appropriate.

Dynabyte Customer Support Services receives copies of all ECNs and advises Dynabyte Authorized Service Centers through seminars and periodic bulletins.

7.03 There are no pertinent ECNs affecting the Disk Controller at the publication date.

OEM Devices

7.04 Figure 7-4 reproduces the Technical Data Data Sheet for the Disk Controller integrated circuit used on the Main Disk Controller.

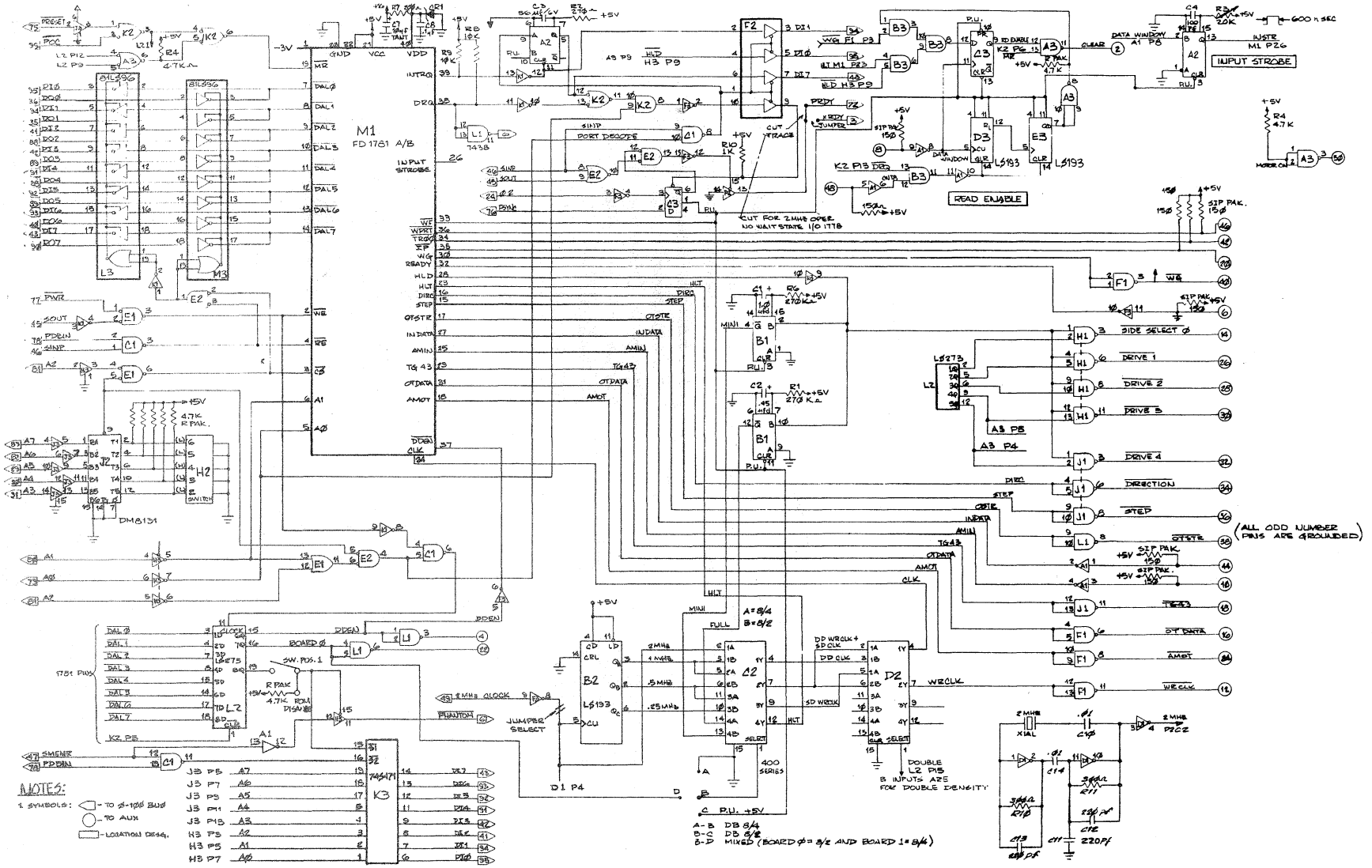


Figure 7-1 — Main Disk Controller — 800741 — Logic Diagram

Table 7-1 — Main Disk Controller — 800741 — Replaceable Parts List

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
	PCA: MAIN DISK CONTROLLER	DYNABYTE	800741	800741
	CABLE: 5100 DISK I/O	DYNABYTE	800228	800228
	CABLE: 5200 DISK I/O	DYNABYTE	800247	800247
C 01	C: FXD TANT 10% 35V 1.0UF	SPRAGUE	196D105X9035HA1	711530
C 02	C: FXD TANT 10% 35V 0.47UF	SPRAGUE	150D	706858
C 03	C: FXD TANT 10% 6V 68UF	SPRAGUE	196D686X9006KA1	706840
C 04	C: FXD CER 10% 1KV 100PF	CENTRALAB	DD101	703978
C 05	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 06	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 07	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 10	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 11	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 12	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 13	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 14	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 15	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 16	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 17	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 18	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 19	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 20	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 21	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 22	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 23	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 24	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 25	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 26	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
CR 01	DIODE: EIA 1N963	MOTOROLA	1N963	704770
P 01	CONNECTOR: 50-CONDUCTOR	AP PRODUCT	929838-01-25	703204
R 01	R: FXD CF 5% 0.25W 270K OHM	ROHM	R25J274	701728
R 02	R: FXD CF 5% 0.25W 200K OHM	ROHM	R25J204	711620
R 03	R: VAR CM 10% 0.25W 20K OHM	SPECTROL	63S203	704734
R 04	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078

Table 7-1 — Main Disk Controller — 800741 Replaceable Parts List (Continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
R 06	R: FXD CF 5% 0.25W 270K OHM	ROHM	R25J274	701728
R 07	R: FXD CF 5% 0.5W 200 OHM	ROHM	R50J201	704680
R 08	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 09	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 10	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 11	R: FXD SIP 7 X 150 OHM	BECKMAN	785-1-R150	704698
R 12	R: FXD SIP 7 X 4.7K OHM	BECKMAN	764-1-4-4.7K	704716
S 01	SWITCH: 6-POSITION SPST DIP	GRAYHILL	765B06	704824
U 01	IC: REGULATOR +5V	TI	7805C	703168
U 02	IC: REGULATOR +5V	TI	7805C	703168
U A1	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U A2	IC: DUAL MULTIVIBRATOR	TI	SN74LS123N	704878
U A3	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U B1	IC: DUAL MULTIVIBRATOR	TI	SN74LS123N	704878
U B2	IC: UP/DOWN COUNTER	TI	SNLS193N	704932
U B3	IC: QUAD 2-IN AND	TI	SN7408N	704860
U C1	IC: QUAD 2-IN NAND SCHMIDTT	TI	SN74LS132N	703582
U C2	IC: QUAD 2-TO 1-LINE MUX	TI	SN74157N	704914
U C3	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U D2	IC: QUAD 2-TO 1-LINE MUX	TI	SN74157N	704914
U D3	IC: UP/DOWN COUNTER	TI	SNLS193N	704932
U E1	IC: QUAD 2-IN OR	TI	SN7432N	703546
U E2	IC: QUAD 2-IN NOR	TI	SN7402N	703456
U E3	IC: UP/DOWN COUNTER	TI	SNLS193N	704932
U F1	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U F2	IC: HEX BUFFER	TI	SN74LS367N	707200
U F3	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U H1	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U H3	IC: HEX BUFFER	SIGNETICS	N8T97N	704968
U J1	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U J2	IC: 6-BIT COMPARATOR	NATIONAL	DM8131N	705004
U J3	IC: HEX BUFFER	SIGNETICS	N8T97N	704968
U K1	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U K2	IC: QUAD 2-IN AND	TI	SN7408N	704860
U K3	IC: RBOOT4A READ ONLY MEMORY	DYNABYTE	803971	803971

Table 7-1 – Main Disk Controller – 800[illegible] Replaceable Parts List (Continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
U K3	IC: RBOOT5 READ ONLY MEMORY	DYNABYTE	804741	804741
U K3	IC: RBOOT1A READ ONLY MEMORY	DYNABYTE	803952	803952
U K3	IC: RBOOT2 READ ONLY MEMORY	DYNABYTE	802033	802033
U K3	IC: RBOOT3 READ ONLY MEMORY	DYNABYTE	802052	802052
U L1	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U L2	IC: OCTAL D LATCH	TI	SN74LS273N	704950
U L3	IC: 5-BIT SHIFT REGISTER	TI	SN74LS96N	703726
U M1	IC: DISK CONTROLLER	WESTERN DI	FD1781-B	704986
U M3	IC: 5-BIT SHIFT REGISTER	TI	SN74LS96N	703726

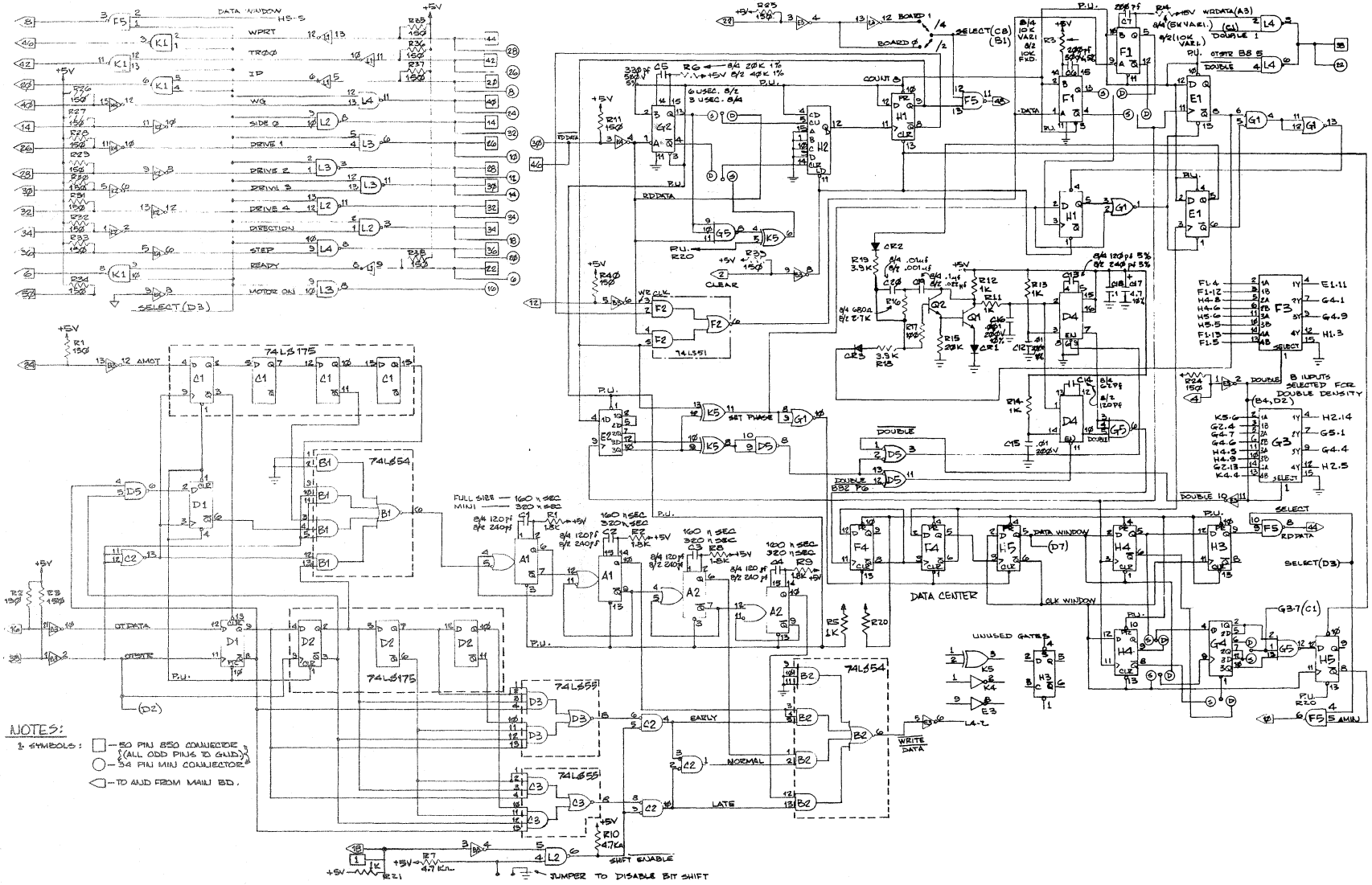


Figure 7-2 — 5200 Auxiliary Disk Controller — 800703 — Logic Diagram

Table 7-2 — 5200 Auxiliary Disk Contr — 800703 — Replaceable Parts List

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
	PCA: 5200 AUXILARY CONTROLLER	DYNABYTE	800703	800703
	CABLE: 5.25-IN DRIVE I/O	DYNABYTE	800437	800437
C 01	C: FXD MICA 5% 500V 240PF	CDE	CM05FD241J03	705400
C 02	C: FXD MICA 5% 500V 240PF	CDE	CM05FD241J03	705400
C 03	C: FXD CER 10% 1KV 220PF	CENTRALAB	DD201	705292
C 04	C: FXD CER 10% 1KV 220PF	CENTRALAB	DD201	705292
C 05	C: FXD CER 10% 1KV 470PF	CENTRALAB	DD471	703348
C 06	C: FXD MICA 5% 500V 240PF	CDE	CM05FD241J03	705400
C 07	C: FXD MICA 5% 500V 240PF	CDE	CM05FD241J03	705400
C 08	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 09	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 10	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 11	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 12	C: FXD CER 20% 50V .01UF	CENTRALAB	UK25-103	705310
C 13	C: FXD MICA 5% 500V 240PF	CDE	CM05FD241J03	705400
C 14	C: FXD MICA 5% 500V 120PF	CDE	CM05FD121J03	705616
C 15	C: FXD CER 20% 50V .01UF	CENTRALAB	UK25-103	705310
C 16	C: FXD MICA 5% 100V 1000PF	CDE	CD15FA102F03	705418
C 17	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 18	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 19	C: FXD CER 10% 50V .022UF	AVX	SR265C223KAA	705382
C 20	C: FXD MICA 5% 100V 1000PF	CDE	CD15FA102F03	705418
C 21	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 22	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 23	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 24	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 25	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 26	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 27	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 28	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 29	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
CR 01	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 02	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 03	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150

Table 7-2 – 5200 Auxiliary Disk Controller - 800703 – Replaceable Parts List (Continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
J 01	CONNECTOR: 4-CONDUCTOR	MOLEX	09-65-1041	705472
J 02	CONNECTOR: 50-CONDUCTOR	AP PRODUCT	929836-01-25	705508
J 04	CONNECTOR: 34-CONDUCTOR	AP PRODUCT	929836-01-17	705490
Q 01	TSTR: EIA 2N2222A	MOTOROLA	2N2222A	705328
Q 02	TSTR: EIA 2N2222A	MOTOROLA	2N2222A	705328
R 01	R: FXD CF 5% 0.25W 2.7K OHM	ROHM	R25J272	705202
R 02	R: FXD CF 5% 0.25W 2.7K OHM	ROHM	R25J272	705202
R 03	R: FXD CF 5% 0.25W 10K OHM	ROHM	R25J104	702952
R 04	R: VAR CM 10% 0.25W 10K OHM	SPECTROL	74W103	712556
R 05	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 06	R: FXD CF 5% 0.25W 40K OHM	ROHM	R25J403	705220
R 07	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 08	R: FXD CF 5% 0.25W 2.7K OHM	ROHM	R25J272	705202
R 09	R: FXD CF 5% 0.25W 2.7K OHM	ROHM	R25J272	705202
R 10	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 11	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 12	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 13	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 14	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 15	R: FXD CF 5% 0.25W 20K OHM	ROHM	R25J203	701764
R 16	R: FXD CF 5% 0.25W 2.7K OHM	ROHM	R25J272	705202
R 17	R: FXD CF 5% 0.25W 100 OHM	ROHM	R25J101	703024
R 18	R: FXD CF 5% 0.25W 3.9K OHM	ROHM	R25J392	705238
R 19	R: FXD CF 5% 0.25W 3.9K OHM	ROHM	R25J392	705238
R 20	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 21	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R A3	R: FXD DIP 15 X 150 OHM	BECKMAN	898-1-R150	705256
R K3	R: FXD DIP 15 X 150 OHM	BECKMAN	898-1-R150	705256
U A1	IC: DUAL ONE SHOT	NATIONAL	DM9602N	705166
U A2	IC: DUAL ONE SHOT	NATIONAL	DM9602N	705166
U B1	IC: 4-WIDE AND OR INV	TI	SN74LS54N	705076
U B2	IC: 4-WIDE AND OR INV	TI	SN74LS54N	705076
U B3	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U C1	IC: QUAD D FLIP FLOP	TI	SN74S175N	705184

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
U C2	IC: QUAD 2-IN NOR	TI	SN7402N	703456
U C3	IC: 2-WIDE 4-IN AND OR INV	TI	SN74LS551N	705094
U D1	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U D2	IC: QUAD D FLIP FLOP	TI	SN74S175N	705184
U D3	IC: 2-WIDE 4-IN AND OR INV	TI	SN74LS551N	705094
U D4	IC: DUAL VCO	TI	SN74S124N	705148
U D5	IC: QUAD 2-IN NAND	TI	SN74LS00N	703438
U E1	IC: QUAD 2-IN NOR	TI	SN7474N	705364
U E2	IC: QUAD D FLIP FLOP	TI	SN74S175N	705184
U E3	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U F1	IC: DUAL MULTIVIBRATOR	TI	SN74LS221N	705130
U F2	IC: DUAL 2-WIDE 2-IN AND OR	TI	SN74LS51N	705058
U F3	IC: QUAD 2-TO 1-LINE MUX	TI	SN74157N	704914
U F4	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U F5	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U G1	IC: QUAD 2-IN NOR	TI	SN7402N	703456
U G2	IC: DUAL MULTIVIBRATOR	TI	SN74LS123N	704878
U G3	IC: QUAD 2-TO 1-LINE MUX	TI	SN74157N	704914
U G4	IC: QUAD D FLIP FLOP	TI	SN74S175N	705184
U G5	IC: TRIPLE 3-IN NAND	TI	SN74LS10N	705040
U H1	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U H2	IC: UP/DOWN COUNTER	TI	SNLS193N	704932
U H3	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U H4	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U H5	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U K1	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U K2	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U K4	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U K5	IC: QUAD EXCLUSIVE OR	TI	SN74LS86N	705112
U L1	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U L2	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U L3	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U L4	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346

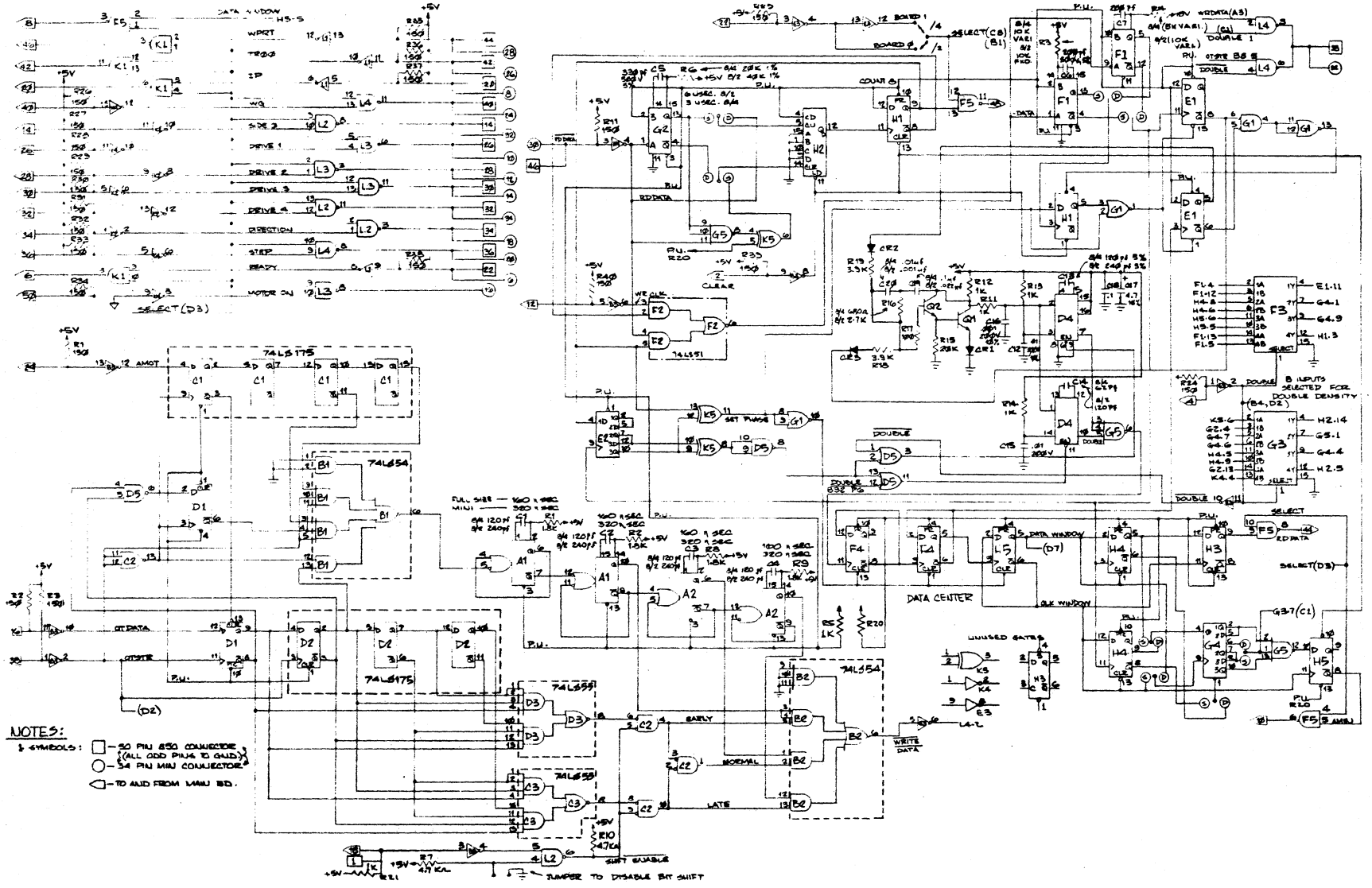


Figure 7-3 — 5010 Auxiliary Disk Controller — 801900 — Logic Diagram

Table 7-3 — 5010 Auxiliary Disk Co ller — 801900 — Replaceable Parts List

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
	PCA: 5010 AUXILARY CONTROLLER	DYNABYTE	801900	801900
	CABLE: 8-IN DRIVE I/O	DYNABYTE	800855	800855
	CABLE: 5010 DISK I/O	DYNABYTE	801862	801862
C 01	C: FXD MICA 5% 500V 100PF	CDE	CM05FD101J03	705598
C 02	C: FXD MICA 5% 500V 100PF	CDE	CM05FD101J03	705598
C 03	C: FXD CER 10% 1KV 220PF	CENTRALAB	DD201	705292
C 04	C: FXD CER 10% 1KV 220PF	CENTRALAB	DD201	705292
C 05	C: FXD CER 10% 1KV 470PF	CENTRALAB	DD471	703348
C 06	C: FXD MICA 5% 500V 100PF	CDE	CM05FD101J03	705598
C 07	C: FXD MICA 5% 500V 100PF	CDE	CM05FD101J03	705598
C 08	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 09	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 10	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 11	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 12	C: FXD CER 20% 50V .01UF	CENTRALAB	UK25-103	705310
C 13	C: FXD MICA 5% 500V 120PF	CDE	CM05FD121J03	705616
C 14	C: FXD MICA 5% 500V 62PF	CDE	CM05ED620J03	705436
C 15	C: FXD CER 20% 50V .01UF	CENTRALAB	UK25-103	705310
C 16	C: FXD MICA 5% 100V 1000PF	CDE	CD15FA102F03	705418
C 17	C: FXD TANT 10% 25V 10UF	SPRAGUE	196D106X9025KA1	707254
C 18	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 19	C: FXD CER 20% 100V .01UF	AVX	SR11E103MAA	706876
C 20	C: FXD CER 20% 100V .01UF	AVX	SR11E103MAA	706876
C 21	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 22	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 23	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 24	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 25	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 26	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 27	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 28	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
C 29	C: FXD CER 20% 12V .1UF	CENTRALAB	UK12-104	703294
CR 01	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 02	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150
CR 03	DIODE: SWITCH EIA 1N914	MOTOROLA	1N914	703150

Table 7-3 – 5010 Auxiliary Disk Controller – 801900 – Replaceable Parts List (Continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
J 01	CONNECTOR: 4-CONDUCTOR	MOLEX	RA09-75-1041	713060
J 02	CONNECTOR: 50-CONDUCTOR	AP PRODUCT	929838-01-25	703204
J 03	CONNECTOR: 50-CONDUCTOR	AP PRODUCT	929838-01-25	703204
Q 01	TSTR: EIA 2N2222A	MOTOROLA	2N2222A	705328
Q 02	TSTR: EIA 2N2222A	MOTOROLA	2N2222A	705328
R 01	R: FXD CF 5% 0.25W 1.8K OHM	ROHM	R25J182	705544
R 02	R: FXD CF 5% 0.25W 1.8K OHM	ROHM	R25J182	705544
R 03	R: VAR CM 10% 0.25W 10K OHM	SPECTROL	74W103	712556
R 04	R: VAR CM 10% 0.25W 5.0K OHM	SPECTROL	64W502	712538
R 05	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 06	R: FXD MF 1% 0.25W 20K OHM	ROHM	CRB 14 203	713294
R 07	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 08	R: FXD CF 5% 0.25W 1.8K OHM	ROHM	R25J182	705544
R 09	R: FXD CF 5% 0.25W 1.8K OHM	ROHM	R25J182	705544
R 10	R: FXD CF 5% 0.25W 4.7K OHM	ROHM	R25J472	703078
R 11	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 12	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 13	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 14	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 15	R: FXD CF 5% 0.25W 20K OHM	ROHM	R25J203	701764
R 16	R: FXD CF 5% 0.25W 680 OHM	ROHM	R25J681	705526
R 17	R: FXD CF 5% 0.25W 100 OHM	ROHM	R25J101	703024
R 18	R: FXD CF 5% 0.25W 3.9K OHM	ROHM	R25J392	705238
R 19	R: FXD CF 5% 0.25W 3.9K OHM	ROHM	R25J392	705238
R 20	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R 21	R: FXD CF 5% 0.25W 1.0K OHM	ROHM	R25J102	701620
R A3	R: FXD DIP 15 X 150 OHM	BECKMAN	898-1-R150	705256
R K3	R: FXD DIP 15 X 150 OHM	BECKMAN	898-1-R150	705256
U A1	IC: DUAL ONE SHOT	NATIONAL	DM9602N	705166
U A2	IC: DUAL ONE SHOT	NATIONAL	DM9602N	705166
U B1	IC: 4-WIDE AND OR INV	TI	SN74LS54N	705076
U B2	IC: 4-WIDE AND OR INV	TI	SN74LS54N	705076
U B3	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528

Table 7-3 — 5010 Auxiliary Disk Controller — 801 , — Replaceable Parts List (Continued)

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
U C1	IC: QUAD D FLIP FLOP	TI	SN74S175N	705184
U C2	IC: QUAD 2-IN NOR	TI	SN7402N	703456
U C3	IC: 2-WIDE 4-IN AND OR INV	TI	SN74LS551N	705094
U D1	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U D2	IC: QUAD D FLIP FLOP	TI	SN74S175N	705184
U D3	IC: 2-WIDE 4-IN AND OR INV	TI	SN74LS551N	705094
U D4	IC: DUAL VCO	TI	SN74S124N	705148
U D5	IC: QUAD 2-IN NAND	TI	SN74LS00N	703438
U E1	IC: QUAD 2-IN NOR	TI	SN7474N	705364
U E2	IC: QUAD D FLIP FLOP	TI	SN74S175N	705184
U E3	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U F1	IC: DUAL MULTIVIBRATOR	TI	SN74LS221N	705130
U F2	IC: DUAL 2-WIDE 2-IN AND OR	TI	SN74LS51N	705058
U F3	IC: QUAD 2-TO 1-LINE MUX	TI	SN74157N	704914
U F4	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U F5	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U G1	IC: QUAD 2-IN NOR	TI	SN7402N	703456
U G2	IC: DUAL MULTIVIBRATOR	TI	SN74LS123N	704878
U G3	IC: QUAD 2-TO 1-LINE MUX	TI	SN74157N	704914
U G4	IC: QUAD D FLIP FLOP	TI	SN74S175N	705184
U G5	IC: TRIPLE 3-IN NAND	TI	SN74LS10N	705040
U H1	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U H2	IC: UP/DOWN COUNTER	TI	SNLS193N	704932
U H3	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U H4	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U H5	IC: DUAL D FLIP FLOP	TI	SN74LS74N	704050
U K1	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U K2	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U K4	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U K5	IC: QUAD EXCLUSIVE OR	TI	SN74LS86N	705112
U L1	IC: HEX SCHMIDT INVERTER	TI	SN74LS14N	703528
U L2	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U L3	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346
U L4	IC: QUAD 2-IN NAND OC	TI	SN7438N	705346

FEATURES

- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
- READ MODE
  - Single/Multiple Record Read with Automatic Sector Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- WRITE MODE
  - Single/Multiple Record Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Selectable Head Settling and Head Engage Times
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers Comprehensive Status Information

APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/FORMATTER
NEW MINI-FLOPPY CONTROLLER

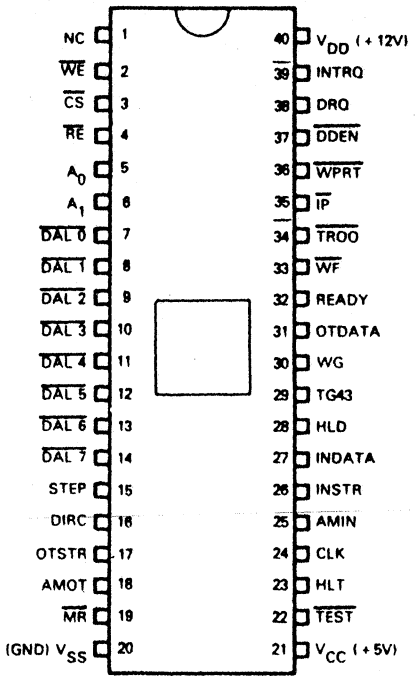
GENERAL DESCRIPTION

The FD1781 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accommodates the interface signals from most drive manufacturers. When in the single density mode the FD1781 is fully IBM-3740 compatible. In the double density mode, the type of encoding scheme is a function of the user's data recovery circuits. In this manner both M²FM or MFM is obtainable.

The processor interface consists of a 8-bit bi-directional bus for data, status, and control word transfers. The FD1781 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1781 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs.

PIN CONNECTIONS



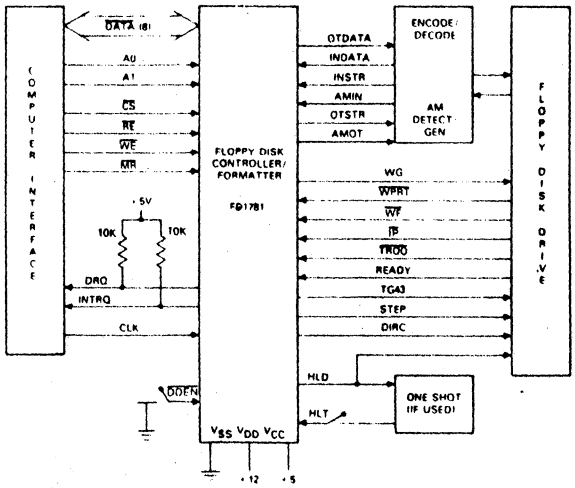
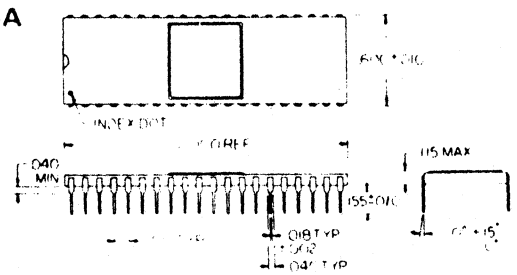


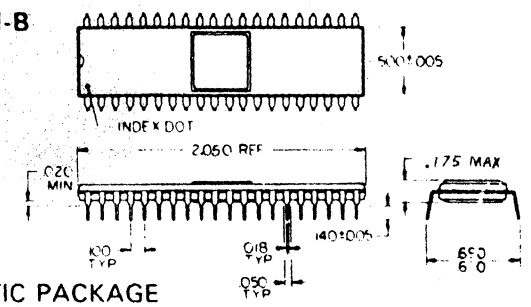
FIG. 1. 1781 SYSTEM BLOCK DIAGRAM

FD1781-A



CERAMIC PACKAGE

FD1781-B



PLASTIC PACKAGE

PRINTED IN U.S.A. 8/77 3K

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet

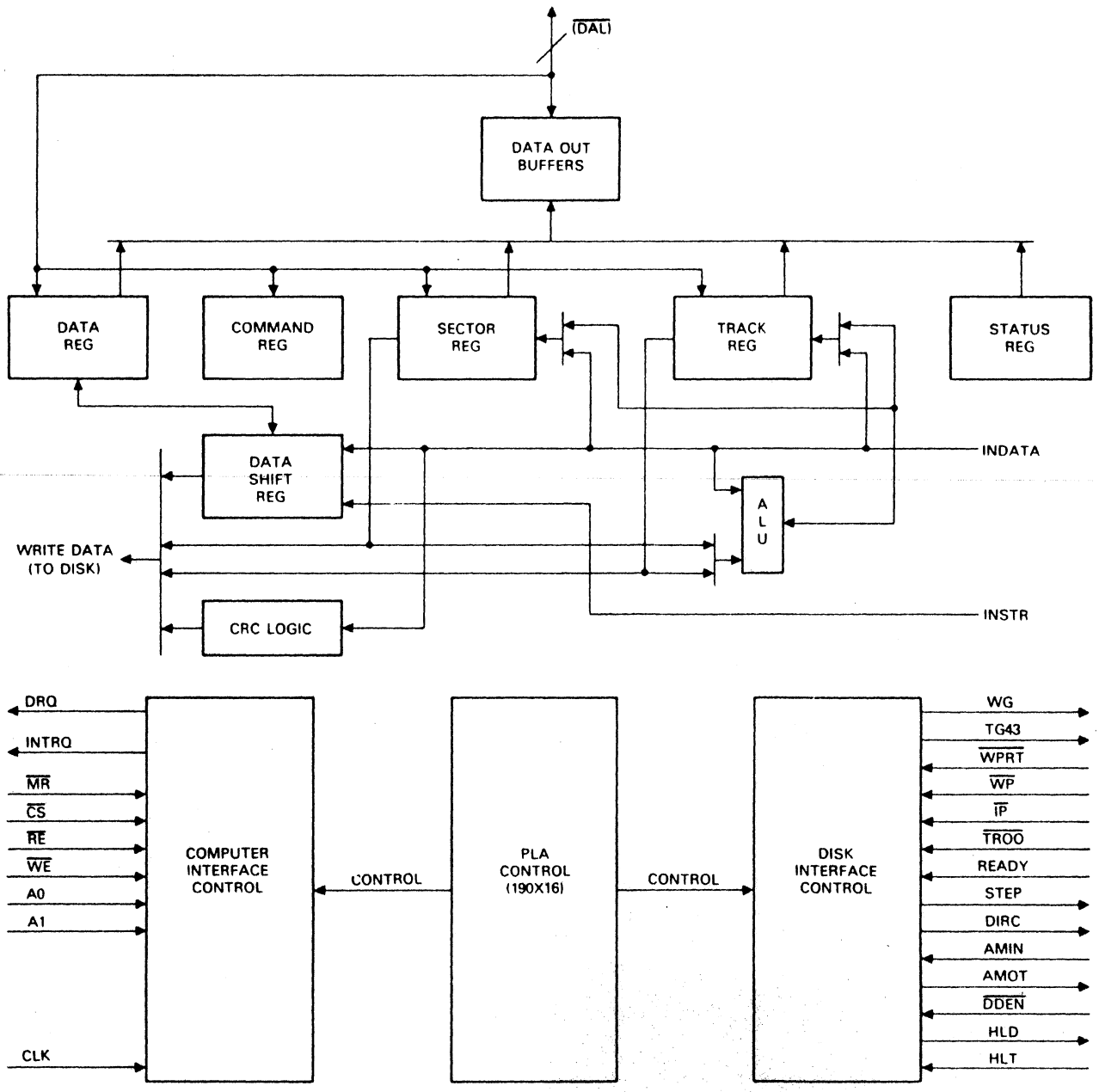


FIG. 3. FD1781 BLOCK DIAGRAM

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated above. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register — This 8-bit register assembles serial data from the Read Data input (INDATA) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register — This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Figure 7-4 — Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

Track Register — This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR) — This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) — This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) — This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic — This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) — The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control — All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1781 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density is assumed. When $\overline{DDEN}$ = 1, single density is assumed. During disk read operations, the user must provide both data recovery and address mark detection circuits external to FD1781 in both single and double density modes. Thus for disk read operations, the user must provide as an input to the FD1781 Data (INDATA) a strobe to indicate when the data is valid (INSTR) and address mark detect (AMIN). During disk write operations and in the double density mode, the FD1781 provides as outputs Data (OTDATA), a strobe to indicate validity (OTSTR) and Address Mark Out (AMOT). During disk write operation and in the single density mode, OTSTR becomes Write Data (WD) which is exactly the same as in the FD1771.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1781. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The least-significant address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1781 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

Figure 7-4 — Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

On Disk Write operations the Data Request is activated when the Data Register transfers its contents the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. The Clock (CLK) input is normally a free-running 2 MHz ±1% when in the double density mode and 1 MHz ±1% when in the single density mode. However when using a mini-floppy, the CLK is normally 1 MHz when in double density mode and 1/2 MHz when in the single density mode.

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step — A 2 μs pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC) — The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is preset.

TABLE 1
STEPPING RATES

CLK	2 MHz	1 MHz	1 MHz	1/2 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1		
R1 R0	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 1	$\overline{TEST}$ = 0	$\overline{TEST}$ = 0
0 0	3 ms	3 ms	6 ms	6 ms	Approx. 400 μs	Approx. 800 μs
0 1	6 ms	6 ms	12 ms	12 ms		
1 0	10 ms	10 ms	20 ms	20 ms		
1 1	20 ms	20 ms	40 ms	40 ms		

The Head Load (HDL) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify Operation, or a Seek or Step operation with the head load bit, h, a logic one, and remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HDL signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input every 10 msec. A high logic state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded after stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read Track and Write Track commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can

Figure 7-4 — Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

be read or written in Read or Write commands respectively by setting a logic 0 in Bit 3 of the command word. The sector length indicator specifies the number of 16 byte groups or 16 × N, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1781 before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the $\overline{\text{Write Protect}}$ status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1781 terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the $\overline{\text{Write Gate}}$ output becomes inactive.

Whenever a Read or Write command is received the FD1781 samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the Ready input.

COMMAND DESCRIPTION

The FD1781 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contain a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1, page four.

TABLE 2
COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	$\overline{s}$
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

TABLE 3
FLAG SUMMARY

TYPE I

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Do not load head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on last track
V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

TABLE 4
FLAG SUMMARY

TYPE II

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

b = Block length flag (Bit 3)

b = 1, IBM format (128 to 1024 bytes)
b = 0, Non-IBM format (16 to 4096 bytes)

a_1a_0 = Data Address Mark (Bits 1-0)

a_1a_0 = 00, FB (Data Mark)
a_1a_0 = 01, FA (User defined)
a_1a_0 = 10, F9 (User defined)
a_1a_0 = 11, F8 (Deleted Data Mark)

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

TABLE 5
FLAG SUMMARY

'PE III
s = Synchronize flag (Bit 0)
$\overline{s}$ = 0, Synchronize to AM $\overline{s}$ = 1, Do Not Synchronize to AM
TYPE IV
Ii = Interrupt Condition flags (Bits 3-0)
I0 = 1, Not Ready to Ready Transition I1 = 1, Ready to Not Ready Transition I2 = 1, Index Pulse I3 = 1, Immediate interrupt
E = Enable HLD and 10 msec Delay
E = 1, Enable HLD, HLT and 10 msec Delay E = 0, Head is assumed Engaged and there is no 10 msec Delay

The Type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1781 receives a command that specifically disengages the head. If the FD1781 does not receive any commands after two revolutions of the disk, the h[illegible]d will be automatically disengaged (HLD made i[illegible]ive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after two revolutions of the disk, the FD1781 terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD1781 terminates operation, interrupts, and sets the Seek error status

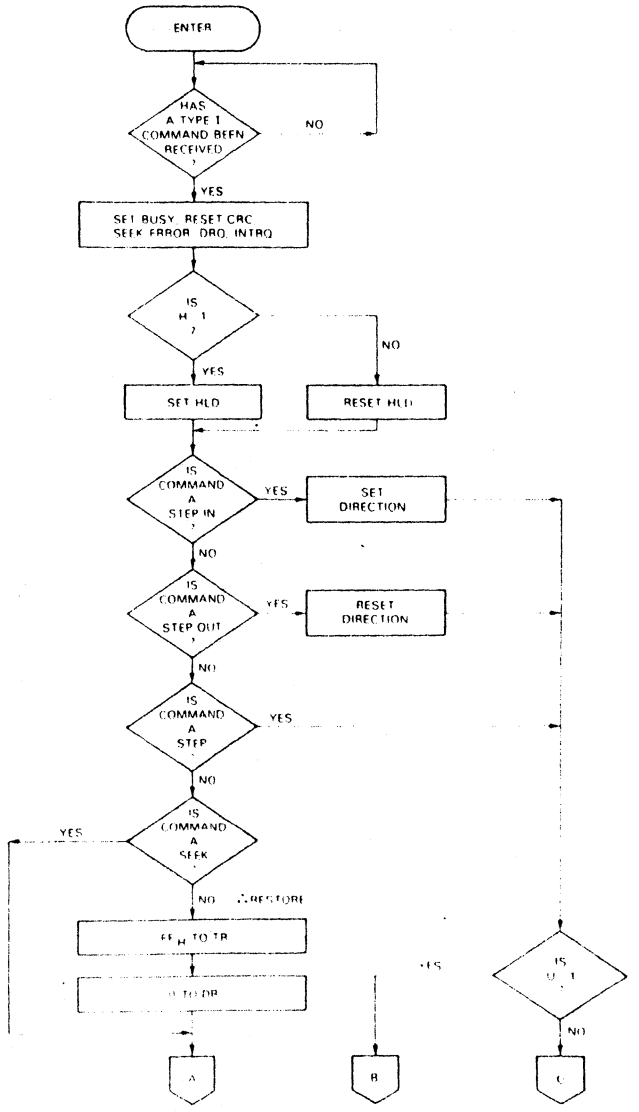


FIG. 4. TYPE I COMMAND FLOW

Figure 7-4 — Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

bit. Note that the Restore command is executed when MR goes from an active to an inactive state. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1781 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1781 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD1781 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

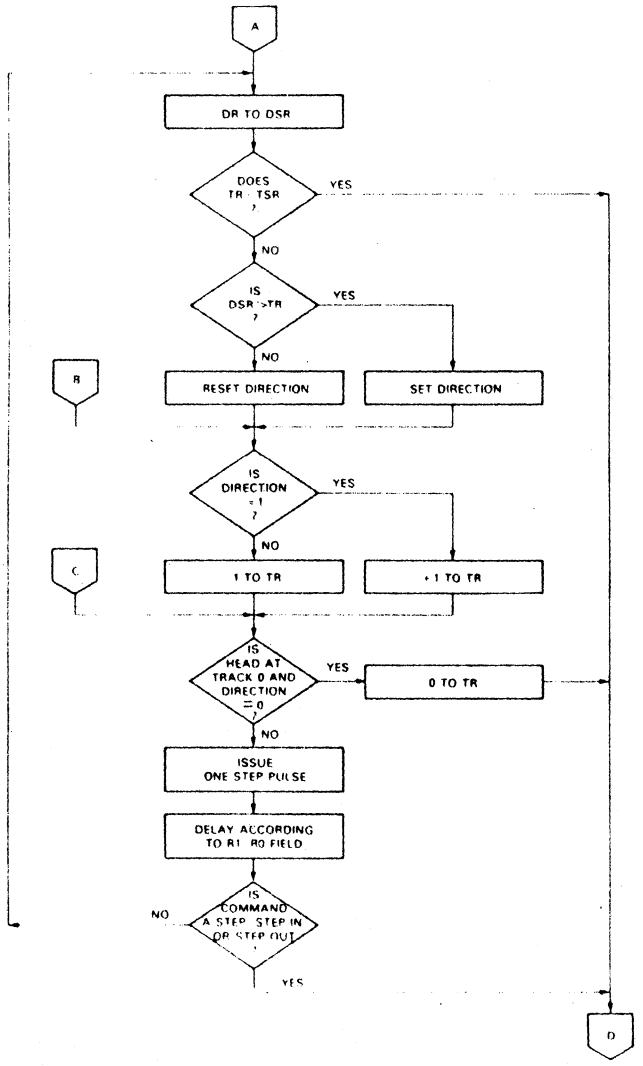


FIG. 5. TYPE I COMMAND FLOW

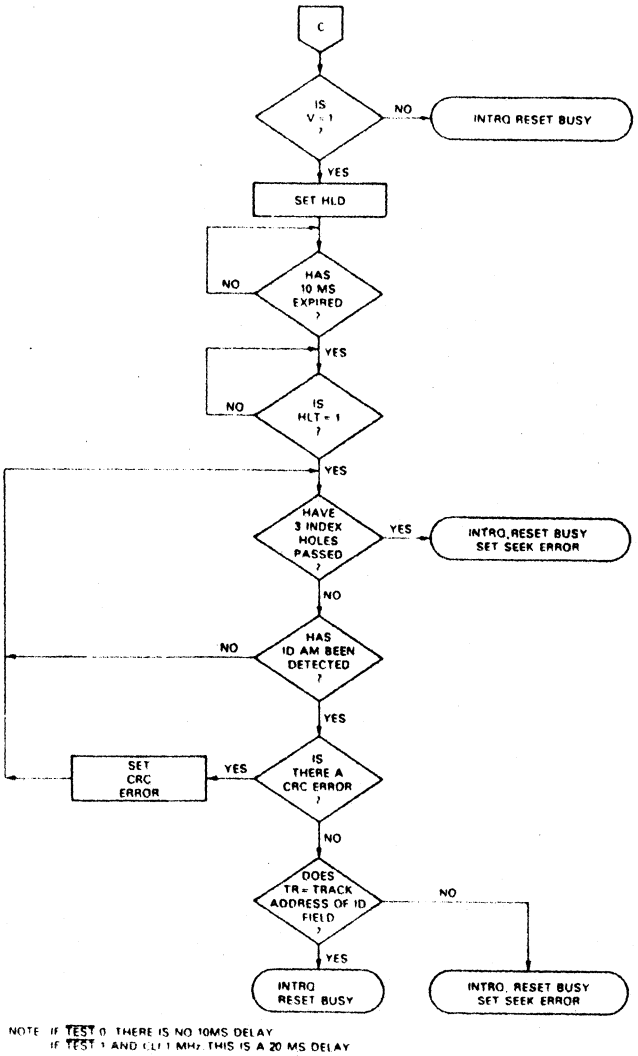


FIG. 6. TYPE I COMMAND FLOW

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

STEP-OUT

Upon receipt of this command, the FD1781 issues e stepping pulse in the direction towards track 0. If ..e u flag is on, the TR is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands include the Read Sector (s) and Write Sector (s) commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II Command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and Data Field format are shown below:

When an ID field is located on the disk, the FD1781 compares the Track Number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector gister. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD1781 must find an ID field with a Track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n = 0,1,2,3.

For b = 1

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b = 0

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the Type II Commands also contain a (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0 a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1781 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminated the command and generates an interrupt.

READ COMMAND

Upon receipt of the Read command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the corrected field; if not, the Record Not Found status bit is set and the operation is terminated.

GAP	ID AM	TRACK NUMBER	ZEROS	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	1	2
ID FIELD									DATA FIELD			

IDAM = ID Address Mark — DATA = $(FE)_{16}$ CLK = $(C7)_{16}$
Data AM = Data Address Mark — DATA = (F8, F9, FA, or FB), CLK = $(C7)_{16}$

Figure 7-4 — Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

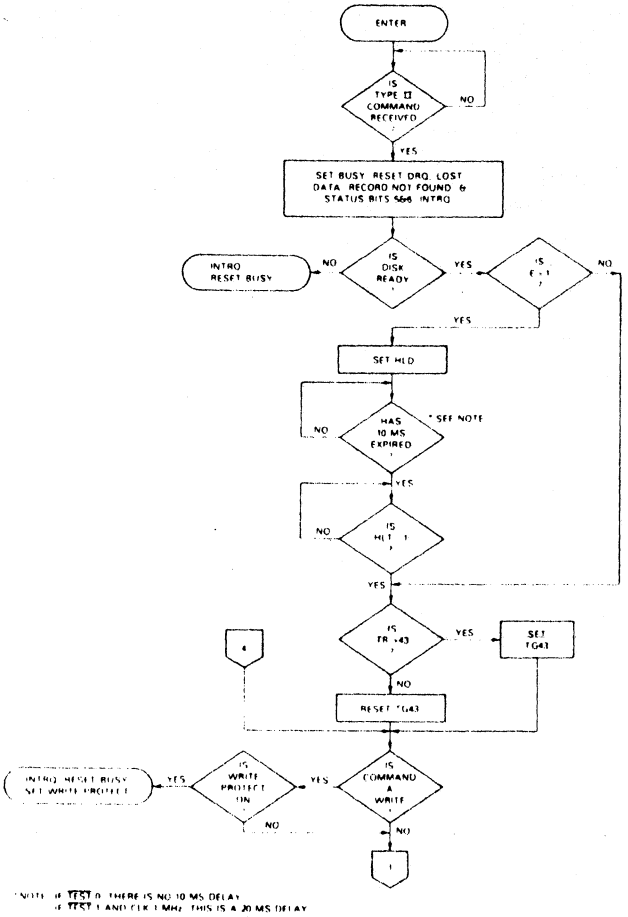


FIG. 7. TYPE II COMMAND

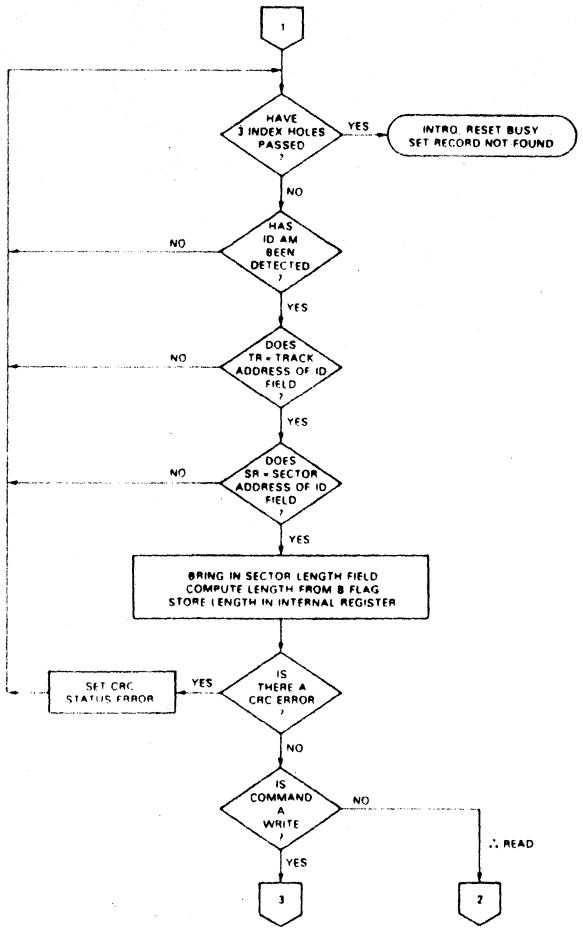


FIG. 8. TYPE II COMMAND

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below:

STATUS BIT 5	STATUS BIT 6	DATA 1	DATA 2	DATA 3
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	1	1

WRITE COMMAND

Upon receipt of the Write command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The FD1781 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a^1a^0 field of the command as shown below:

a^1	a^0	DATA 1	DATA 2	DATA 3
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	1	1

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

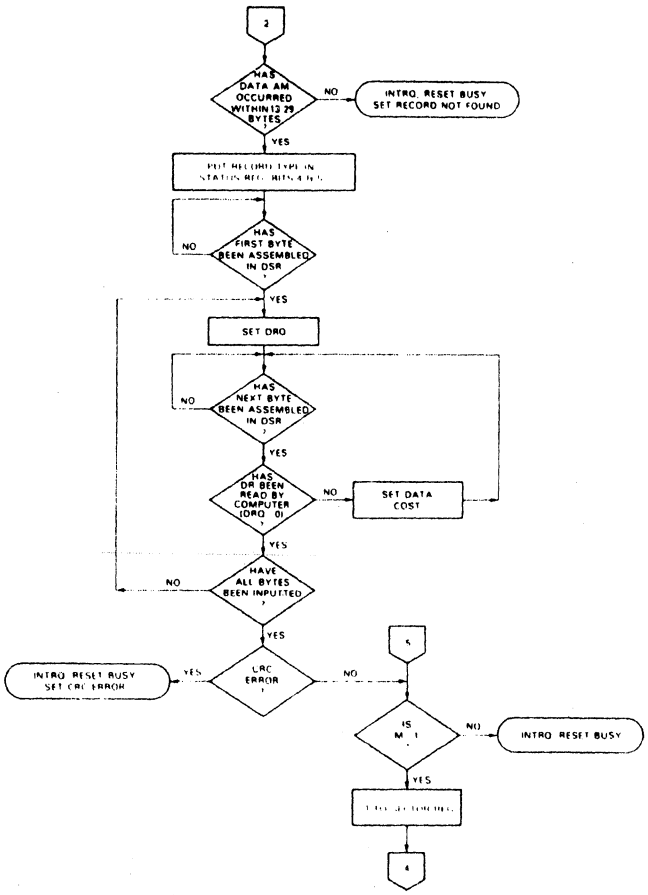


FIG. 9. TYPE II COMMAND

The FD1781 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	ZEROS	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

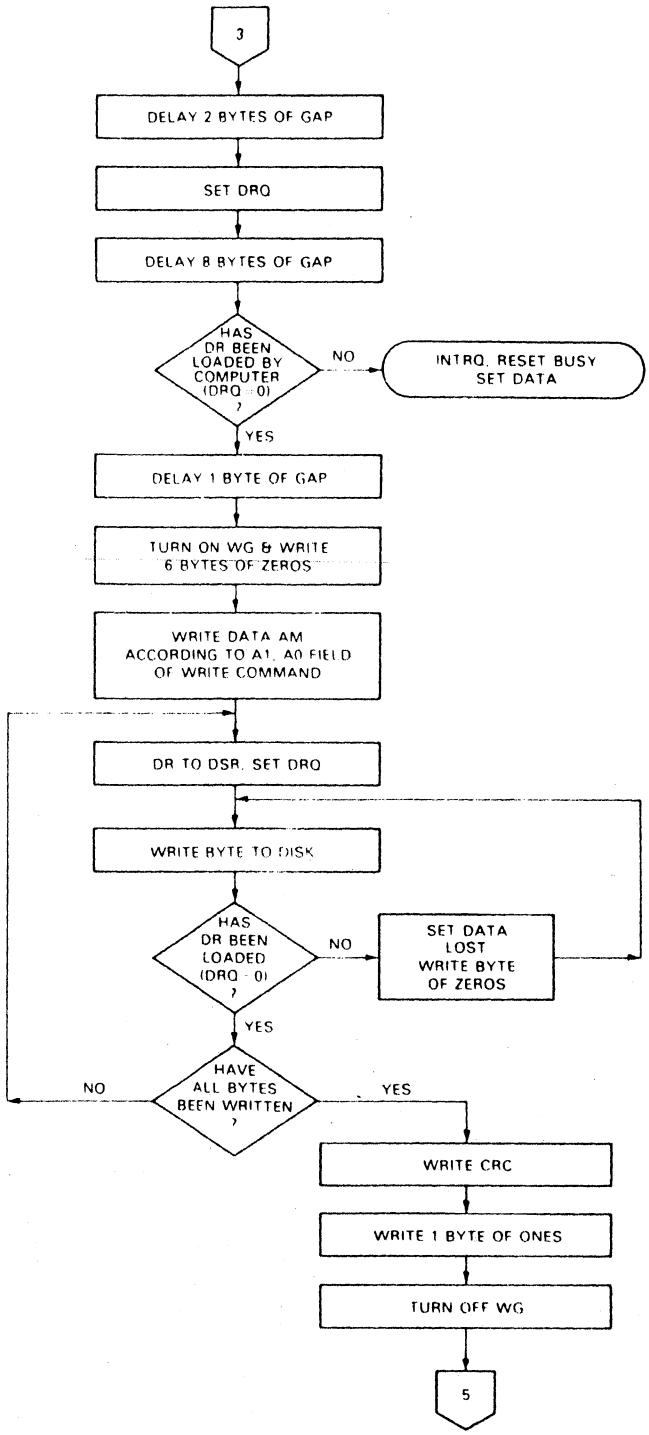


FIG. 10. TYPE II COMMAND

Although the CRC characters are transferred to the computer, the FD1781 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

Figure 7-4 — Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0 (S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

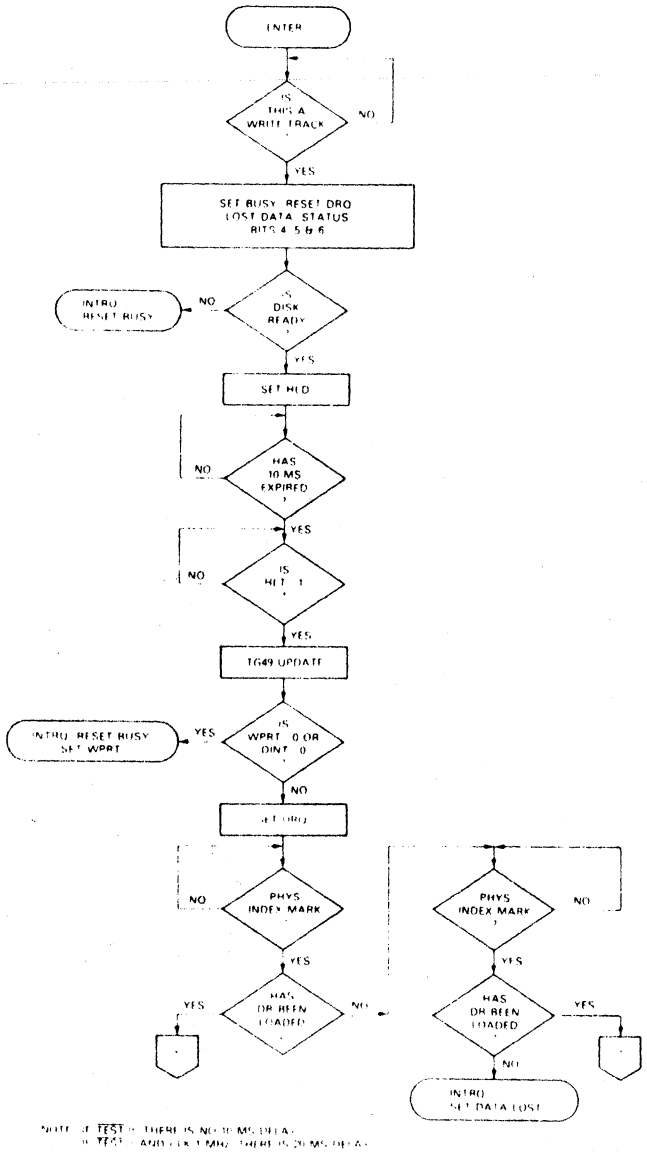


FIG. 11. TYPE III COMMAND WRITE TRACK

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK* (HEX)
F7	Write CRC Char.	FF
F8	Data Addr. Mark	C7
F9	Data Addr. Mark	C7
FA	Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	ID Addr. Mark	C7

*Single density only

DATA 1	DATA 2	DATA 3	TYPE OF ADDRESS MARK
0	0	0	Deleted Data mark
0	0	1	Data Mark (user defined)
0	1	0	Data Mark (user defined)
0	1	1	Data Mark
1	0	0	Index Address Mark
1	0	1	Undefined
1	1	0	ID Address Mark
1	1	1	Undefined

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

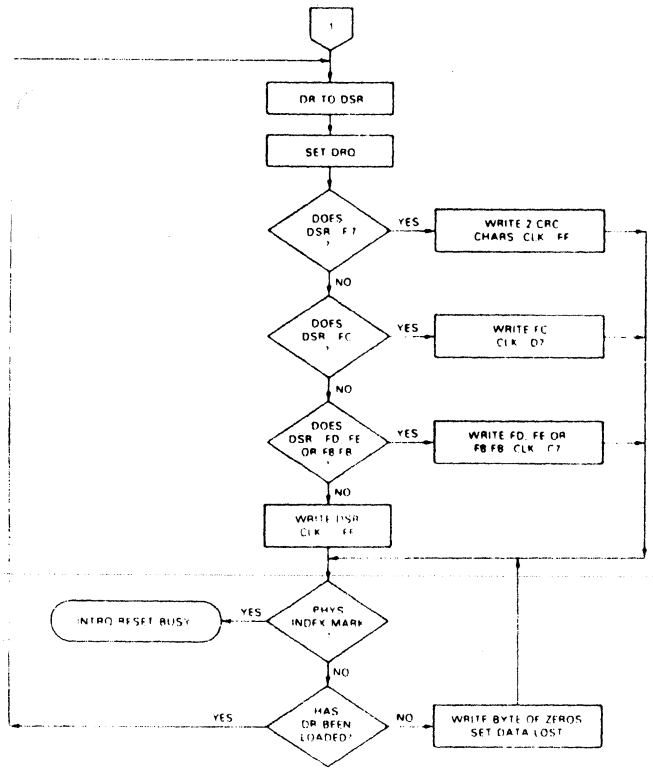


FIG. 12. TYPE III COMMAND WRITE TRACK

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

NOTE: If I_0-I_3 = 0, there is no interrupt generated but the current command is terminated and busy is reset.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)

7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

TABLE 6
STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Figure 7-4 — Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 Not Ready	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2 Track 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 Not Ready	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 RECORD TYPE/ WRITE PROTECT	On Read Record: It indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD1781 raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a clock mark of $(FF)_{16}$. However, if the FD1781 detects a data pattern on F7 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by a F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128, 256, 512, or 1024 bytes, or may be formatted in non-IBM 3740 with sectors length of 16 to 4096 bytes in 16 byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector and the following section details non-IBM formats.

IBM 3740 FORMATS—128 BYTES/SECTOR

Shown in Figure 13, is the IBM format with 128 bytes/sector. In order to format this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	00 or FF
6	00
1	FC (Index Mark)
26	00 or FF
* 6	00
1	FE (ID Address Mark)
1	Track Number
1	00
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	00 or FF
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	00 or FF
247**	00 or FF

*Write bracketed field 26 times

**Continue writing until FD1781 interrupts out. Approx. 247 bytes.

NON-IBM FORMATS

Non-IBM formats are very similar to the IBM formats except a different algorithm is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to Section V, Type II Commands with b flag equal to zero. Note that F7 thru FE must not appear in the sector length byte of the ID field.

In formatting the FD1781, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1781 does not require the index address mark (i.e., DATA = FC, CLK = D7) and it need not be present.

REFERENCES:

1. IBM Diskette OEM Information GA21-9190-1
2. SA900 IBM Compatibility Reference Manual — Shugart Associates.

Figure 7-4 — Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

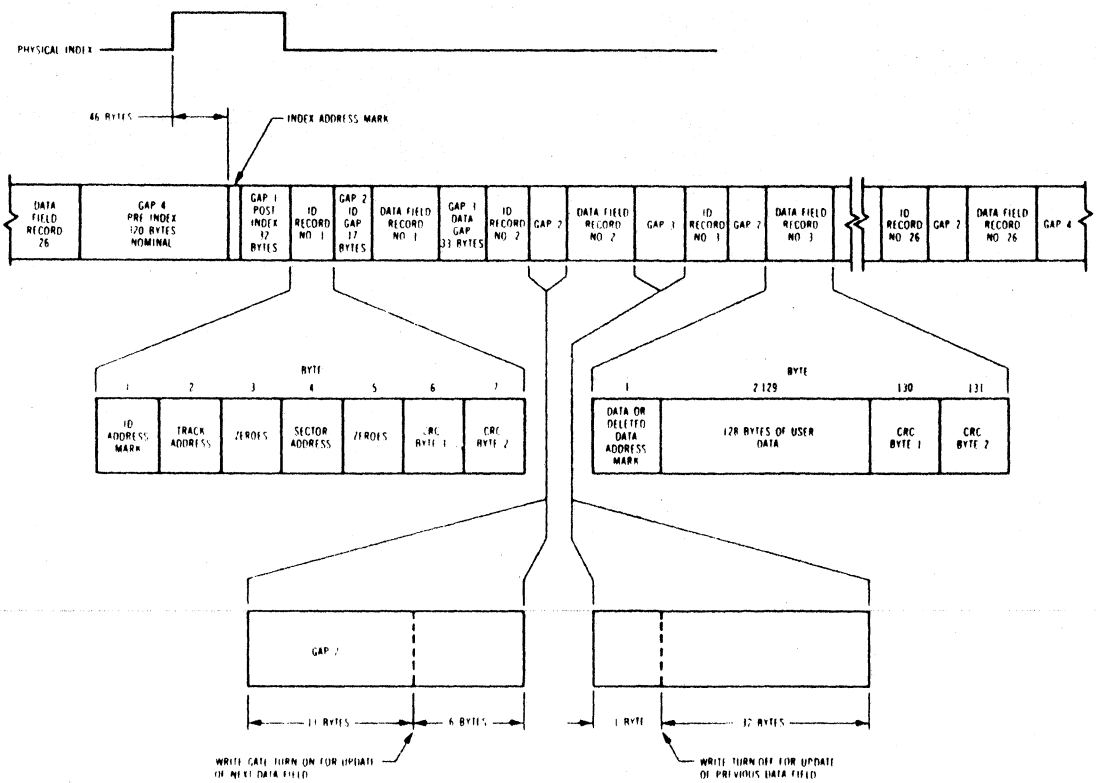


FIG. 13. TRACK FORMAT

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground)	+15 to −0.3V
Max. Voltage to Any Input With Respect to V_{SS}	+15 to −0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	−55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = +12.0V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

V_{DD} = 10 ma Nominal, V_{CC} = 30 ma Nominal

SYMBOL	CHARACTERISTIC	MIN.	TYPE.	MAX.	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	$I_O = -100\ \mu A$
V_{OL}^*	Output Low Voltage			0.45	V	I_O = 1.6 mA

NOTE: Vol ≤ .4V when interfacing with low Power Schottky parts ($1_o < 1$ ma)
*except WG, where $V_{OL} \leq .5$ volts.

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

TIMING CHARACTERISTICS

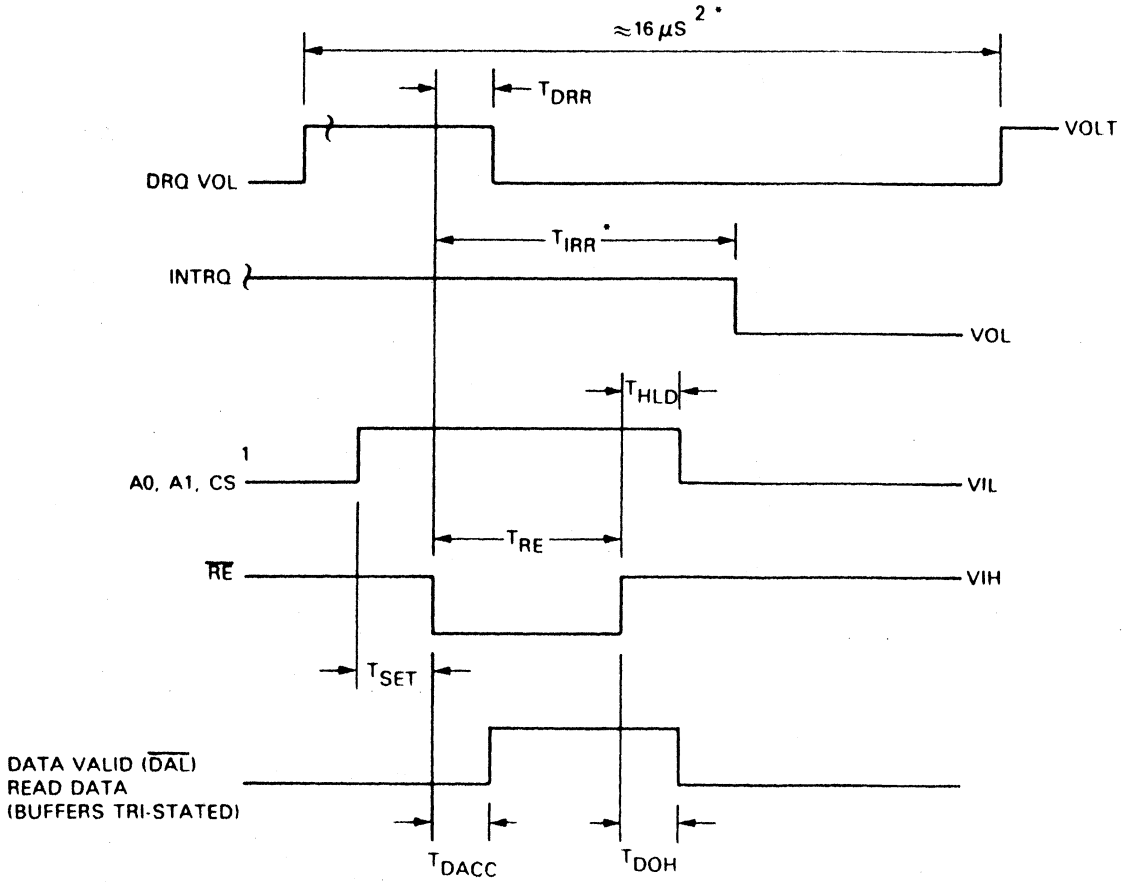
T_A = 0°C to 70°C, V_{DD} = +12V ±.6V, V_{SS} = 0V, V_{CC} = +5V ±.25V

NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz.

READ OPERATIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	500			nsec	C_L = 25 pf
TDRR	DRQ Reset from $\overline{RE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 25 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 25 pf

READ ENABLE TIMING



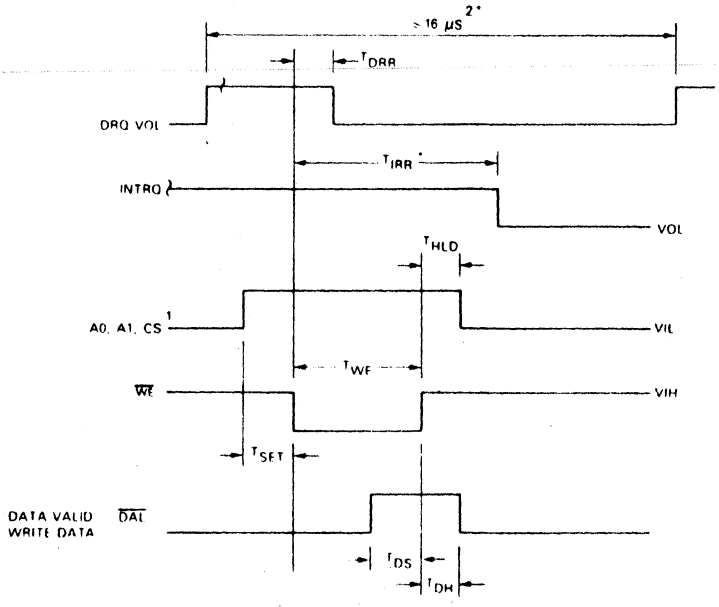
NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. FOR READ TRACK COMMAND. THIS TIME MAY BE 6* TO 16* μSEC WHEN S = 0.
*TIME DOUBLES WHEN CLK-1 MHz.

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

WRITE OPERATIONS

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	20			nsec	

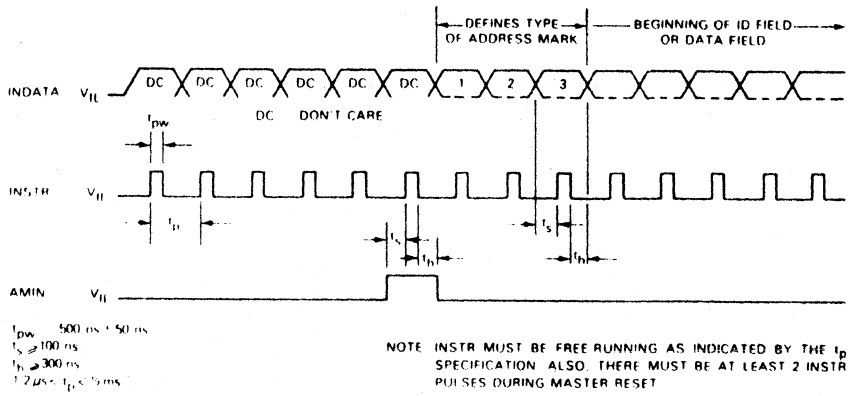
WRITE ENABLE TIMING



NOTE 1 $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED
2 WHEN WRITING DATA INTO SECTOR, TRACK, OR DATA REGISTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 8 μSEC AFTER THE RISING EDGE OF $\overline{WE}$. WHEN WRITING INTO THE COMMAND REGISTER, STATUS IS NOT VALID UNTIL SOME 12 μSEC LATER. THESE TIMES ARE DOUBLED WHEN CLK = 1 MHz

*TIME DOUBLES WHEN CLOCK = 1 MHz

INPUT DATA TIMING

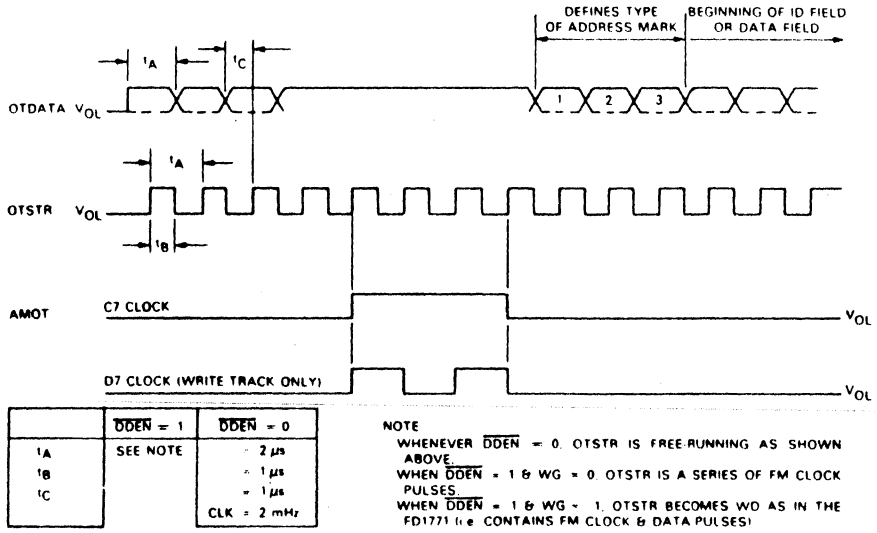


t_{pw} = 500 ns ± 50 ns
$t_s \geq 100$ ns
$t_h \geq 300$ ns
1.2 μs < t_p < 5 ms

NOTE INSTR MUST BE FREE RUNNING AS INDICATED BY THE t_p SPECIFICATION. ALSO, THERE MUST BE AT LEAST 2 INSTR PULSES DURING MASTER RESET

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

OUTPUT DATA TIMING



	DDEN = 1	DDEN = 0
tA	SEE NOTE	= 2 µs
tB		= 1 µs
tC		= 1 µs
		CLK = 2 mHz

NOTE
WHENEVER DDEN = 0, OTSTR IS FREE-RUNNING AS SHOWN ABOVE.
WHEN DDEN = 1 & WG = 0, OTSTR IS A SERIES OF FM CLOCK PULSES.
WHEN DDEN = 1 & WG = 1, OTSTR BECOMES WD AS IN THE FD1771 (i.e. CONTAINS FM CLOCK & DATA PULSES)

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty	175			nsec	2 MHz ±1% See Note
TCD_2	Clock Duty	210			nsec	
TSTP	Step Pulse Output	2000			nsec	These times doubled when CLK = 1 MHz
TDIR	Dir Setup to Step	12			µsec	
TMR	Master Reset Pulse Width	5			µsec	
TIP	Index Pulse Width	5			µsec	
TWF	Write Fault Pulse Width	5			µsec	

MISCELLANEOUS TIMING

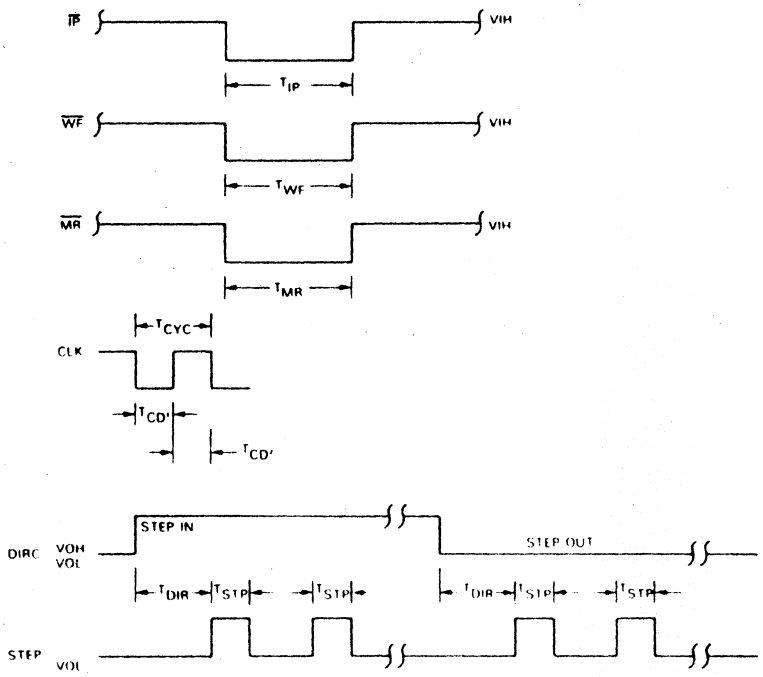


Figure 7-4 — Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V
40		V_{DD}	+12V
19	MASTER RESET	$\overline{MR}$	• A logic low on this input resets the device and clears the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive.
COMPUTER INTERFACE:			
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	• Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$.
3	CHIP SELECT	$\overline{CS}$	• A logic low on this input selects the chip and enables computer communication with the device.
5,6	REGISTER SELECT LINES	A0,A1	• These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:
4	READ ENABLE	$\overline{RE}$	• A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
2	WRITE ENABLE	$\overline{WE}$	• A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
38	DATA REQUEST	DRQ	• This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	• This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5.
24	CLOCK	CLK	• This input requires a free-running square wave clock for internal timing reference.
FLOPPY DISK INTERFACE:			
25	ADDRESS MARK DETECT IN	AMIN	• Indicates to the FD1781 that an address mark has been detected. The FD1781 assumes the next three data bits defines the type of address mark encountered.
26	INPUT STROBE	INSTR	• Indicates that INDATA is VALID.
27	INPUT DATA	INDATA	The external data recovery circuits present INDATA as an input to the FD1781. INDATA must be valid when INSTR is active, see timing.
31	OUTPUT DATA	OTDATA	• The FD1781 presents output data and is valid when OTSTR is active.

A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	Status Reg	Command Reg
0	1	Track Reg	Track Reg
1	0	Sector Reg	Sector Reg
1	1	Data Reg	Data Reg

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

28	HEAD LOAD	HLD	• The HLD output controls the loading of the Read-Write head against the media. The HLT input is sampled every 10 nsec. When a logic high is sampled on the HLT input the head is assumed to be engaged.
23	HEAD LOAD TIMING	HLT	
15	STEP	STEP	• Step and direction motor control. The step output contains a 2 μsec high signal for each step and the direction output is active high when stepping in, active low when stepping out.
16	DIRECTION	DIRC	
17	OUTPUT STROBE	OTSTR	• OTSTR when active indicates when the Output data is valid. The leading edge of OTSTR is centered about the data. (See timing) OTSTR becomes Write Data (WD) when $\overline{DDEN}$ = 1.
18	ADDRESS MARK OUT	AMOT	• AMOT when active informs the external data recovery circuits to write a unique data mark in double density mode. AMOT is valid for three data bits if CLK mark = C7.
29	TRACK GREATER THAN 43	TG43	• This output informs the drive that the Read-Write head is positioned between track 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	• This output is made valid when writing is to be performed on the diskette.
32	READY	READY	• This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{WRITE\ FAULT}$	$\overline{WF}$	• This input detects writing faults indications from the drive. When WG = 1 and $\overline{WF}$ goes low the current Write command is terminated and the Write Fault status bit is set. The $\overline{WF}$ input should be made inactive (high) when WG becomes inactive.
34	$\overline{TRACK\ 00}$	$\overline{TR00}$	• This input informs the FD1781 that the Read-Write head is positioned over Track 00 when a logic low.
35	$\overline{INDEX\ PULSE}$	$\overline{IP}$	• Input, when low for a minimum of 10 μsec, informs the FD1781 when an index mark is encountered on the diskette.
36	$\overline{WRITE\ PROTECT}$	$\overline{WPRT}$	• This input is sampled whenever a Write Command is received. A logic low terminated the command and sets the Write Protect Status bit.
37	$\overline{DOUBLE\ DENSITY}$	$\overline{DDEN}$	• This pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected.
22	$\overline{TEST}$	$\overline{TEST}$	• This input is used for testing purposes only and should be tied to +5V or left open by the user.

Figure 7-4 – Western Digital FD1781 Floppy Disk Formatter/Controller Data Sheet (Continued)

Table 7-4 – Disk Controller Replaceable Assemblies List

Reference	Description	Manufacturer	Manufacturer's Part Number	Dynabyte P/N
	PCA: MAIN DISK CONTROLLER	DYNABYTE	800741	800741
	PCA: 5200 AUXILARY CONTROLLER	DYNABYTE	800703	800703
	PCA: 5010 AUXILARY CONTROLLER	DYNABYTE	801900	801900
	CABLE: 5100 DISK I/O	DYNABYTE	800228	800228
	CABLE: 5200 DISK I/O	DYNABYTE	800247	800247
	CABLE: 5010 DISK I/O	DYNABYTE	801862	801862
	CABLE: SYSTEM DISK I/O	DYNABYTE	800893	800893
	CABLE: SYSTEM DISK I/O	DYNABYTE	804475	804475
	CABLE: 8-IN DRIVE I/O	DYNABYTE	800855	800855
	CABLE: 5.25-IN DRIVE I/O	DYNABYTE	800437	800437

DATE	BY	REVISION RECORD	DR	CK
	A	PCB RFV B		
	REL	ECN 575		

- RD GATE
- WRENBL
- -WR GATE
- +NRZ WRT DATA
- -NRZ WRITE DATA
- + WRITE CLOCK
- -WRITE CLOCK
- -EN WT COMP
- -REWRT CUR
- -VFO DATA
- -10 BYTES
- -WRITE GATE
- -MFM WRITE DATA
- EARLY
- LATE
- -AAF
- DCLK
- -DR SEL
- -MFM WRT DATA
- +MFM WRT DATA
- -MFM READ DATA
- +MFM READ DATA
- +CLK
- -CLK
- -VFO DATA
- +2X CLOCK
- -10 BYTES
- +NRZ RD DATA
- -NRZ RD DATA
- -AMF
- -HD SEL 4
- -SEEK COMP
- -TRK Ø
- -WR FLT
- -HD SEL 1
- -HD SEL 2
- -INDX
- -RDY
- -STEP
- -DR SEL 1
- -DR SEL 2
- -DR SEL 3
- -DIR IV

NOTES, UNLESS OTHERWISE SPECIFIED:
1. ○ DENOTES J1 RIBBON CONNECTOR (34 PIN)
   ▷ DENOTES J2 " " (20 PIN)
   ⬡ DENOTES J3 " " (50 PIN)

PCB 719593 B
PCA 807283 B

TOLERANCES (EXCEPT AS NOTED)	DYNABYTE	
DECIMAL	SCALE	DRAWN BY
		APPROVED BY
FRACTIONAL	TITLE WINCHESTER DATA SEPARATOR SCHEMATIC	
ANGULAR	DATE 9/81	DRAWING NUMBER 200588-A