SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-3W AI & 4-2W AI

LMH	0-2860	201
Cat.	Subject	Suffix

IBM Location
Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

2-3W AI & 4-2W AI

CATEGORY CODE

T03

P/N	5800307 5800000
EC	160015
STANDARD RESTRICTED	
CARD SIZE	1-6

T03AJ = 5800307
T03AA = 5800000
T03AF = 5800310

890971

+2.3MA AT 0.3V	D12	A T03AB AI	D10	-14.8MA AT 0.3V
+2.3MA AT 0.3V	D13			
+2.3MA AT 0.3V	D07	A T03AB BI	B07	-14.8MA AT 0.3V
+2.3MA AT 0.3V	B09			
+2.3MA AT 0.3V	B03	A T03AB CI	D04	-14.8MA AT 0.3V
+2.3MA AT 0.3V	D05			
+2.3MA AT 0.3V	B08	A T03AB DI	D06	-14.8MA AT 0.3V
+2.3MA AT 0.3V	D09			
+2.3MA AT 0.3V	D11	A T03AB EI	B10	-14.8MA AT 0.3V
+2.3MA AT 0.3V	B12			
+2.3MA AT 0.3V	B13			
+2.3MA AT 0.3V	D02	A T03AB FI	B02	-14.8MA AT 0.3V
+2.3MA AT 0.3V	B04			
+2.3MA AT 0.3V	B05			

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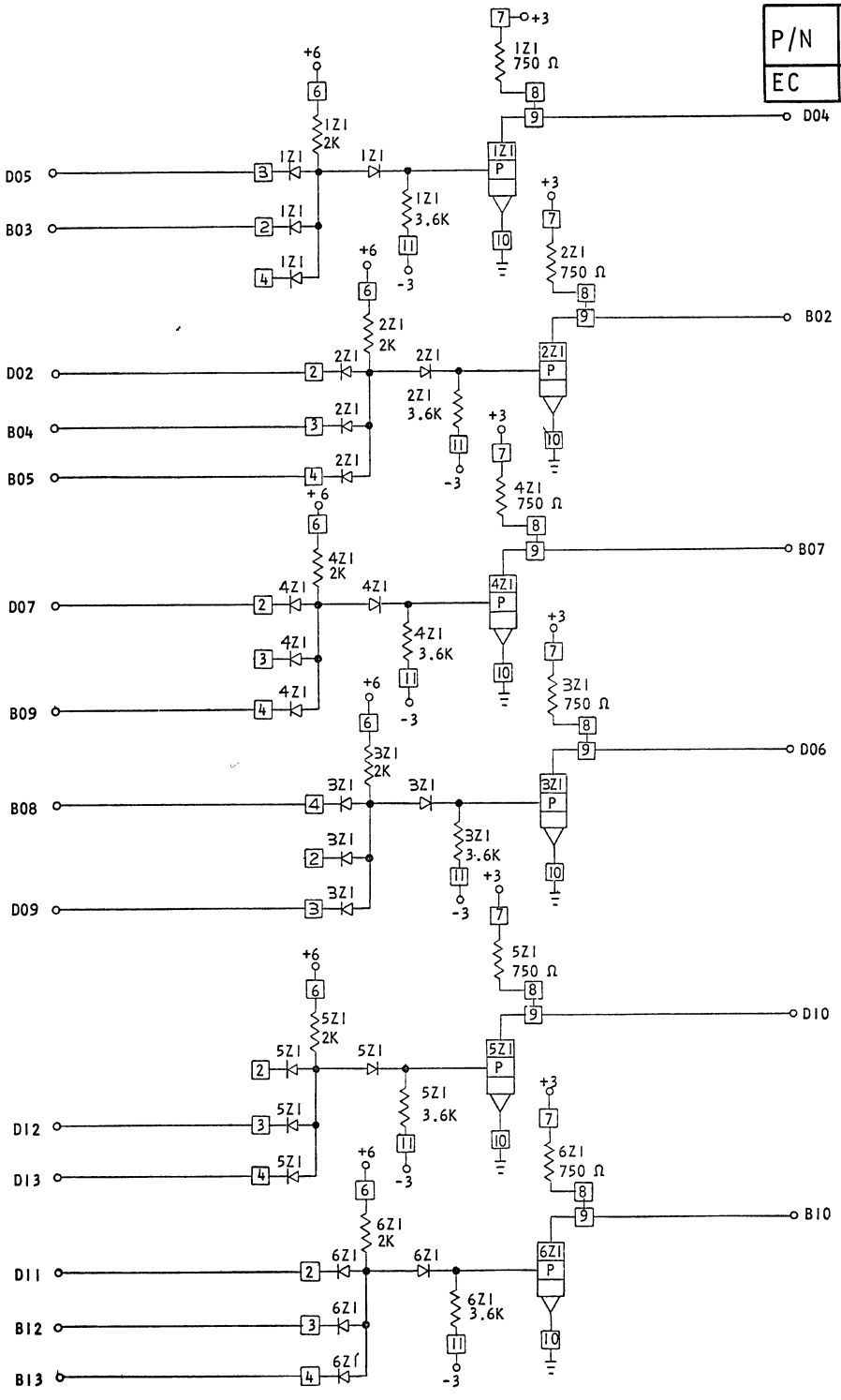
P/N	5800000
EC	160015



IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

5-3W AI

CATEGORY CODE

T03

P/N	5800002
EC	160016
STANDARD RESTRICTED	
CARD SIZE	1-6

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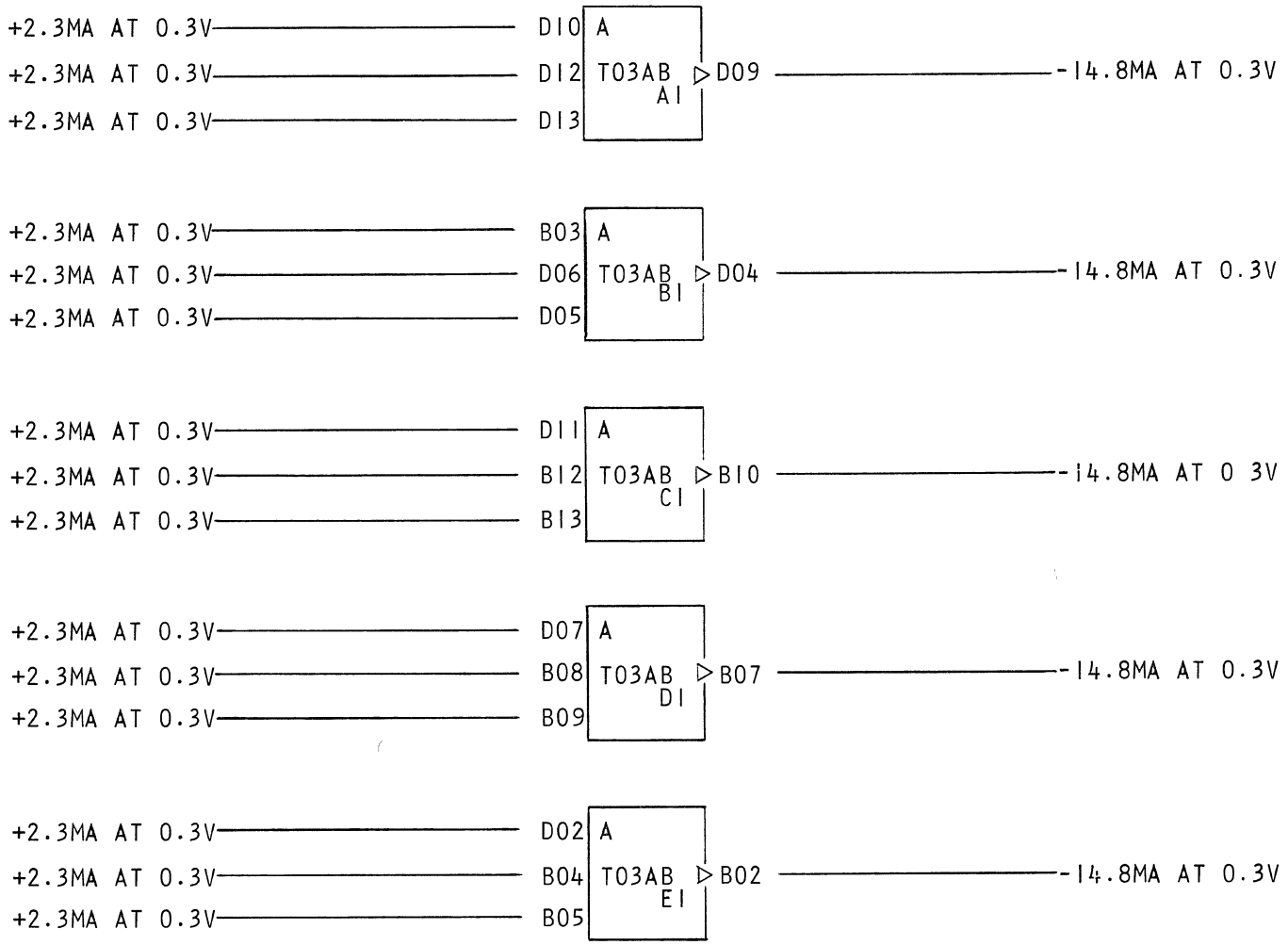
T03AA = 580[illegible]
T03AF = 5800311

890971



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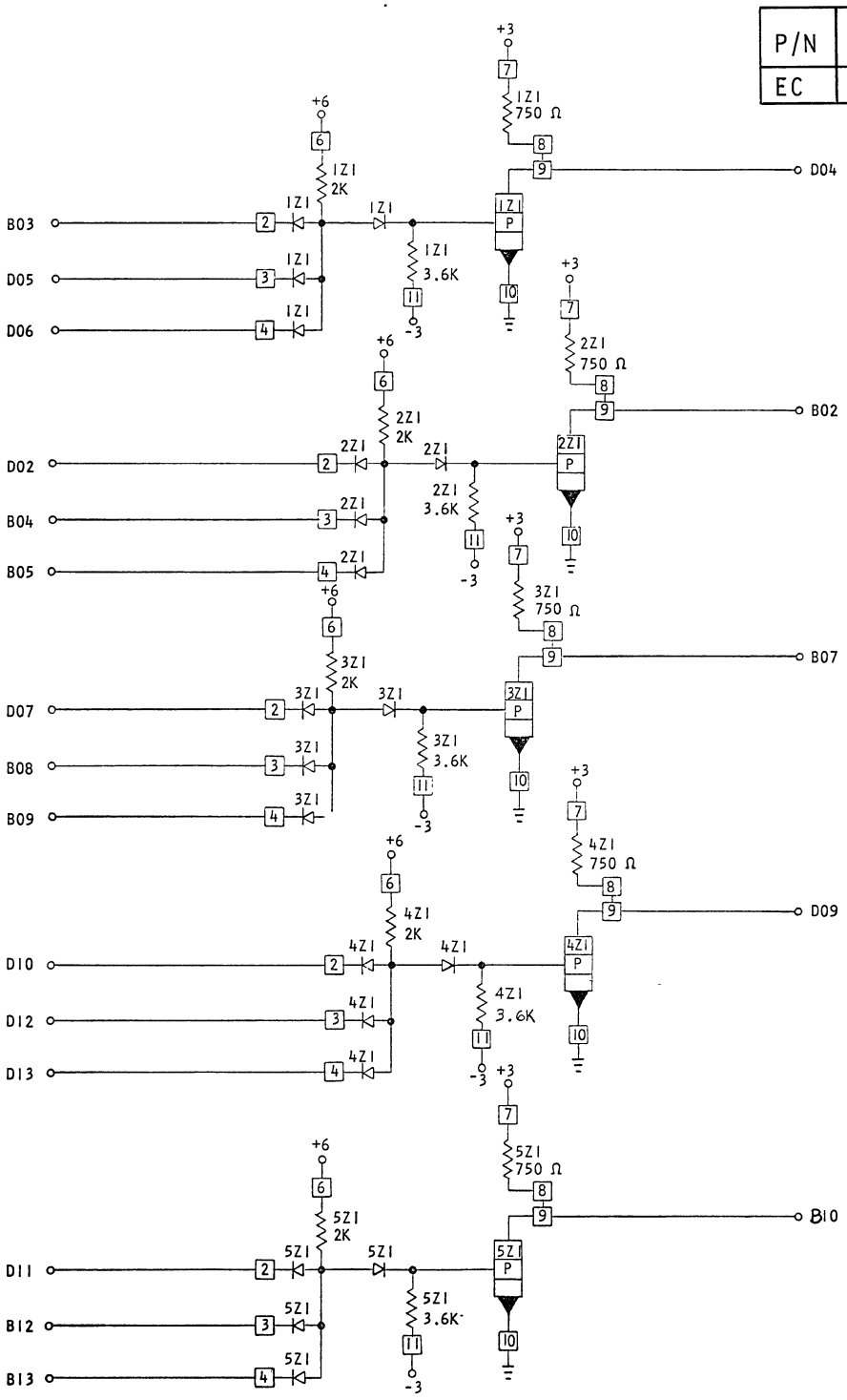
EC	160016



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-7W AI & 1-3W AI

LMH	0-2860	203
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

2-7W AI & 1-3W AI

CATEGORY CODE

T03

P/N	5800004
EC	160020
STANDARD ACTIVE	
CARD SIZE	1-6

T03AA = 5100244

890971

+2.3MA AT 0.3V — D11
+2.3MA AT 0.3V — D12
+2.3MA AT 0.3V — B13
+2.3MA AT 0.3V — D09
+2.3MA AT 0.3V — B09
+2.3MA AT 0.3V — D06
+2.3MA AT 0.3V — D07

A
T03AB AI ▷B10 — -14.8MA AT 0.3V

+2.3MA AT 0.3V — D02
+2.3MA AT 0.3V — B04
+2.3MA AT 0.3V — B05
+2.3MA AT 0.3V — B03
+2.3MA AT 0.3V — D04
+2.3MA AT 0.3V — B08
+2.3MA AT 0.3V — B07

A
T03AB BI ▷B02 — -14.8MA AT 0.3V

+2.3MA AT 0.3V — D10
+2.3MA AT 0.3V — B12
+2.3MA AT 0.3V — D13

A
T03AB CI ▷D05 — -14.8MA AT 0.3V

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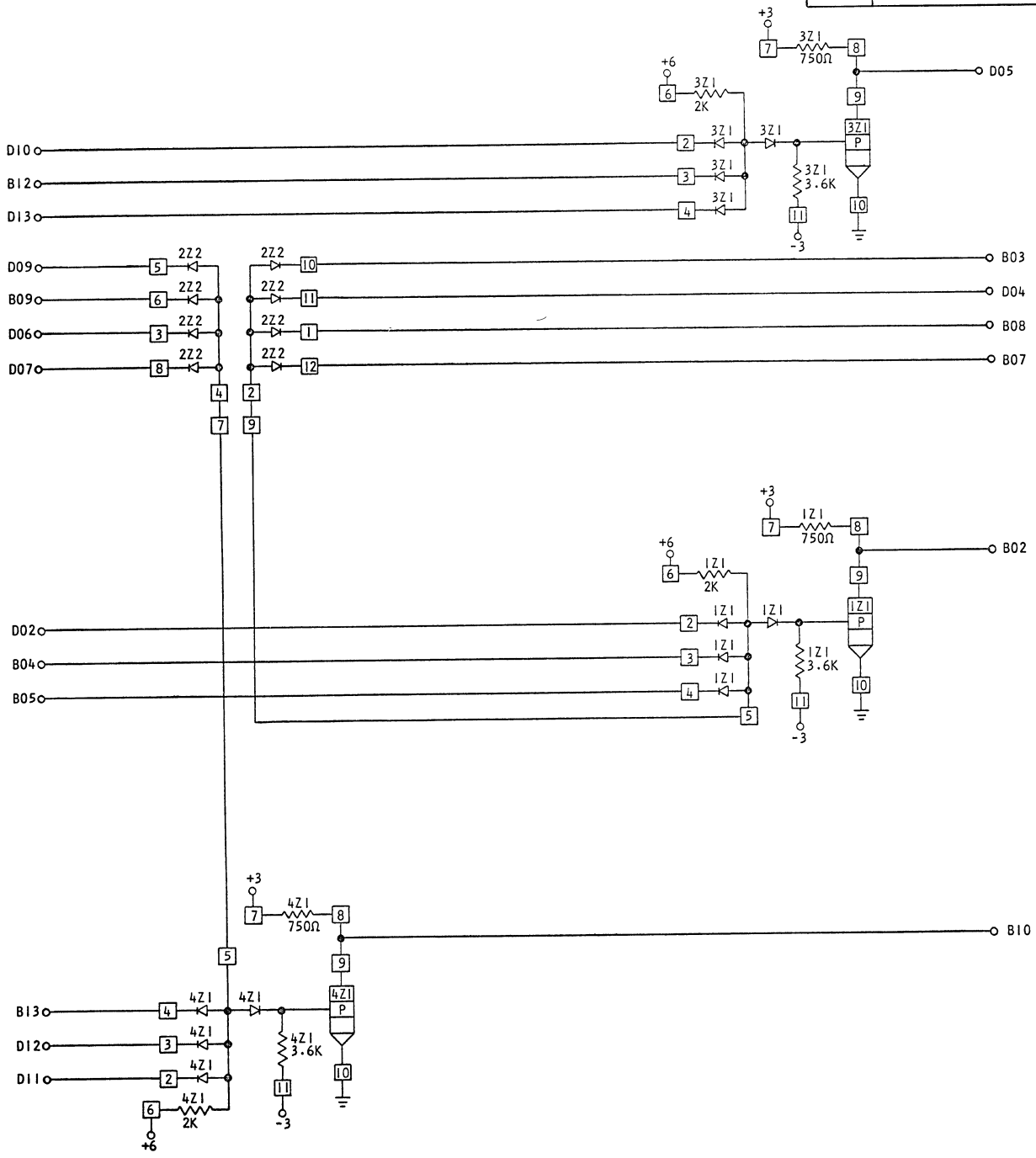
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-7W AI & 1-3W AI

P/N	5800004
EC	160020



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-11W AI & 2-3W AI

LMH	0-2860	204
Cat.	Subject	Suffix

IBM **Location Manufacturing Specification**

POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

1-11W AI & 2-3W AI

CATEGORY CODE

T03

P/N	5800005
EC	160017
STANDARD RESTRICTED	
CARD SIZE	1-6

T03AA = 5811242

890971

+2.3MA AT 0.3V — B07
+2.3MA AT 0.3V — B08
+2.3MA AT 0.3V — B09
+2.3MA AT 0.3V — D09
+2.3MA AT 0.3V — B10
+2.3MA AT 0.3V — D12
+2.3MA AT 0.3V — B13
+2.3MA AT 0.3V — D13
+2.3MA AT 0.3V — B12
+2.3MA AT 0.3V — D11
+2.3MA AT 0.3V — D10

A
T03AB AI ▷ D07 — -14.8MA AT 0.3V

+2.3MA AT 0.3V — B03
+2.3MA AT 0.3V — D05
+2.3MA AT 0.3V — D06

A
T03AB BI ▷ D04 — -14.8MA AT 0.3V

+2.3MA AT 0.3V — D02
+2.3MA AT 0.3V — B04
+2.3MA AT 0.3V — B05

A
T03AB CI ▷ B02 — -14.8MA AT 0.3V

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Applicability	ENDICOTT	ENDICOTT Responsibility	1-67 Date	1 of 2 Page

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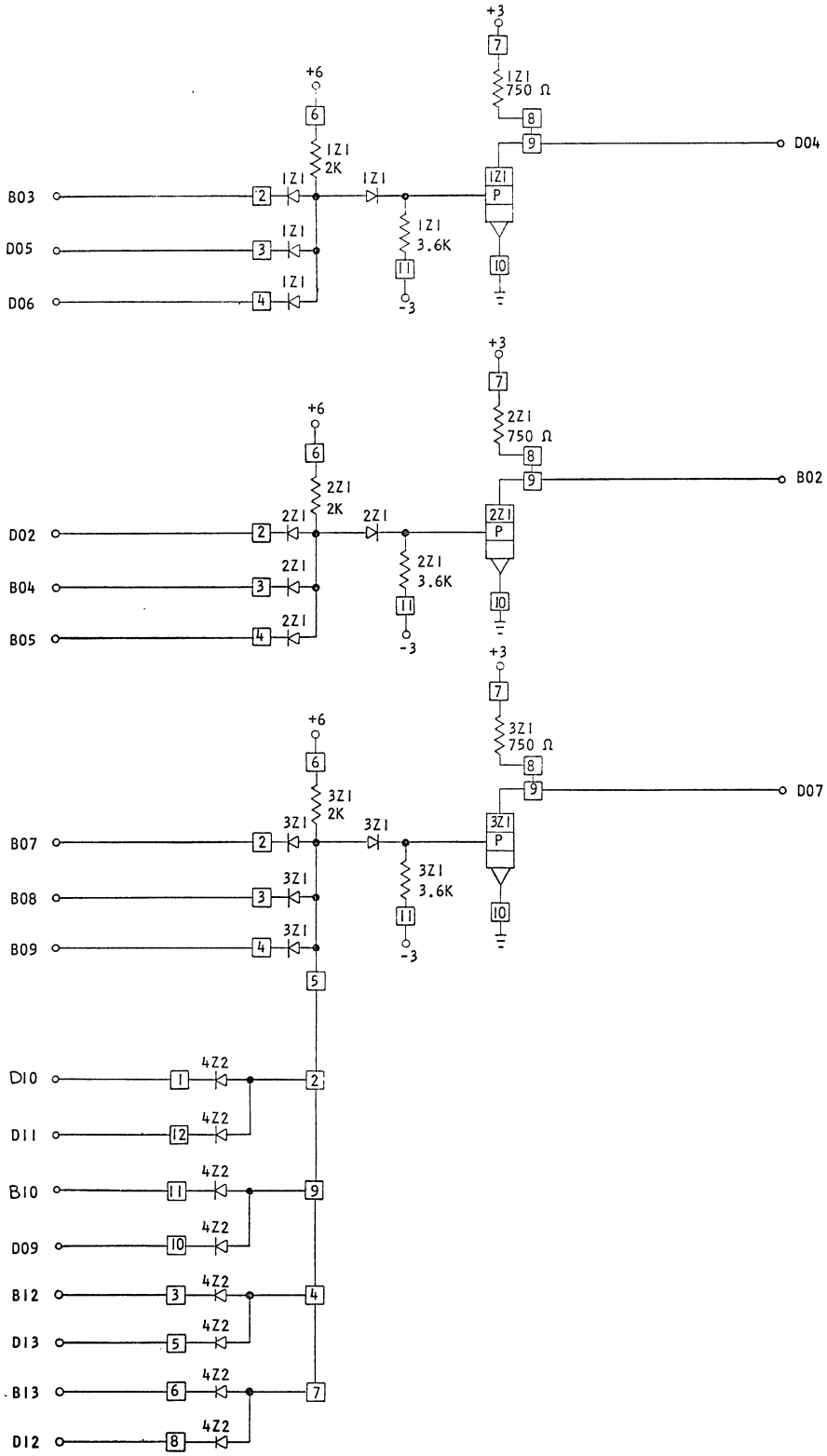
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-11W AI & 2-3W AI

P/N	5800005
EC	160017



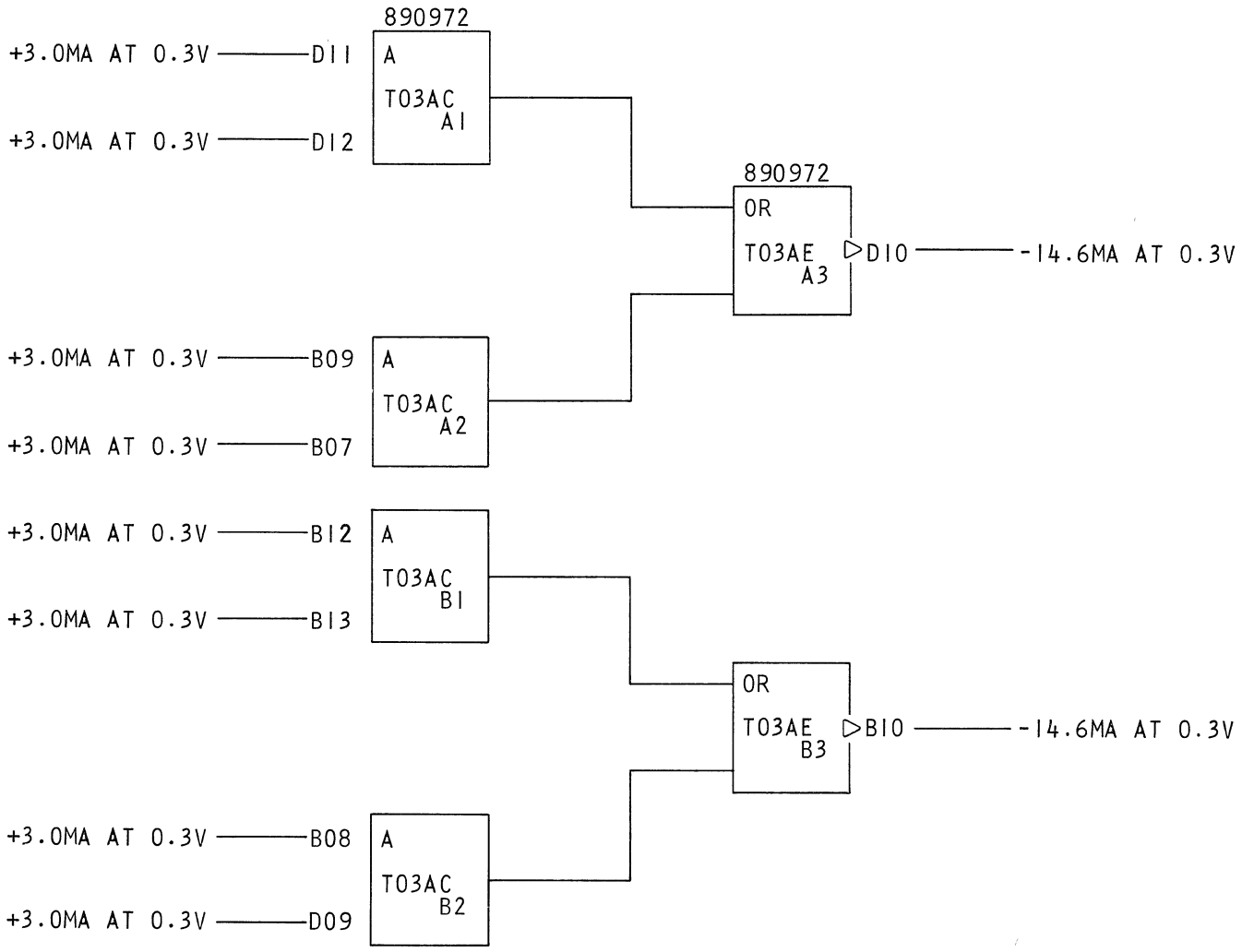
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

4-2W, 2W AOI

CATEGORY CODE

T03

P/N	5800006	
EC	160021	
STANDARD RESTRICTED		
CARD SIZE		1-6

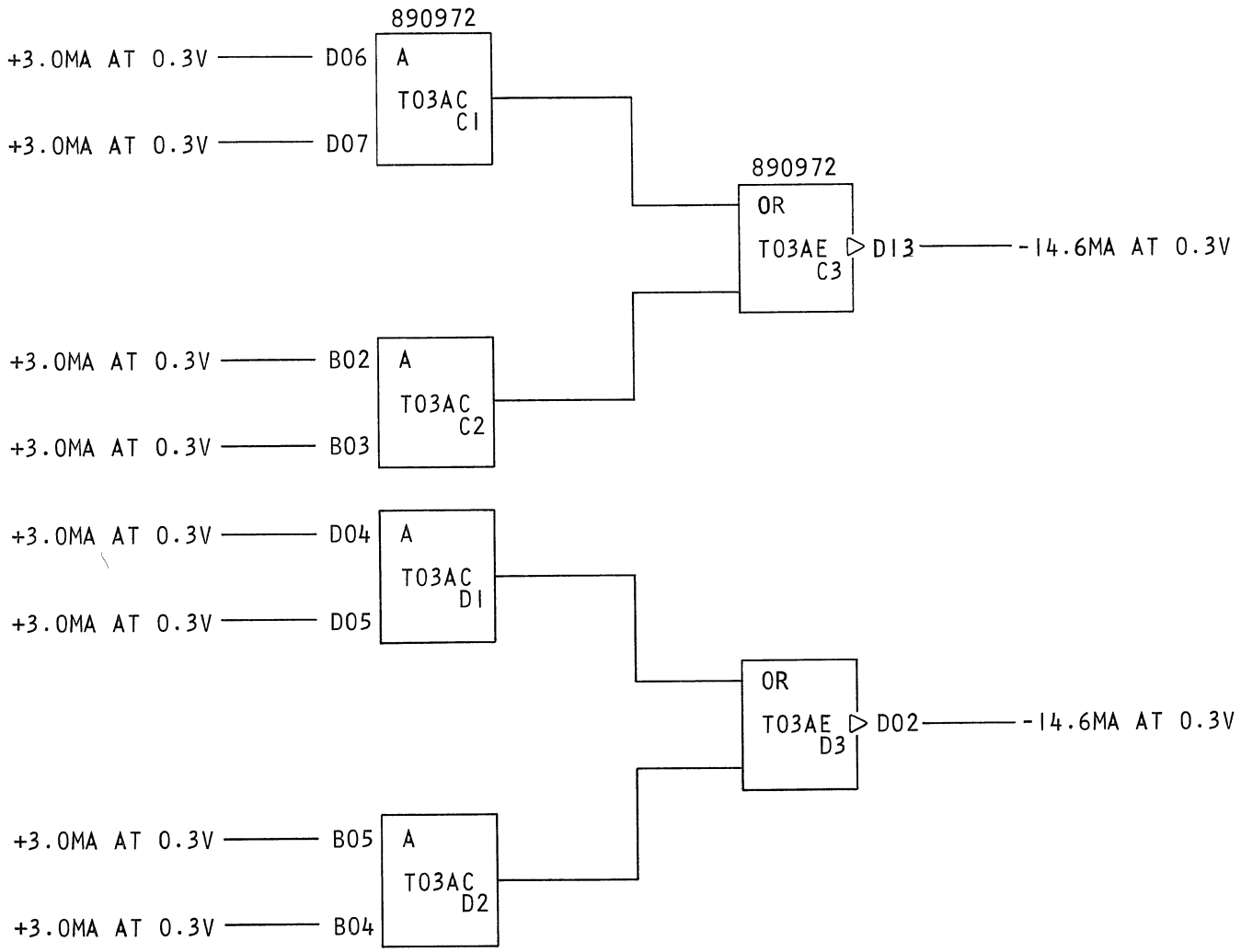


4-2W, 2W AOI

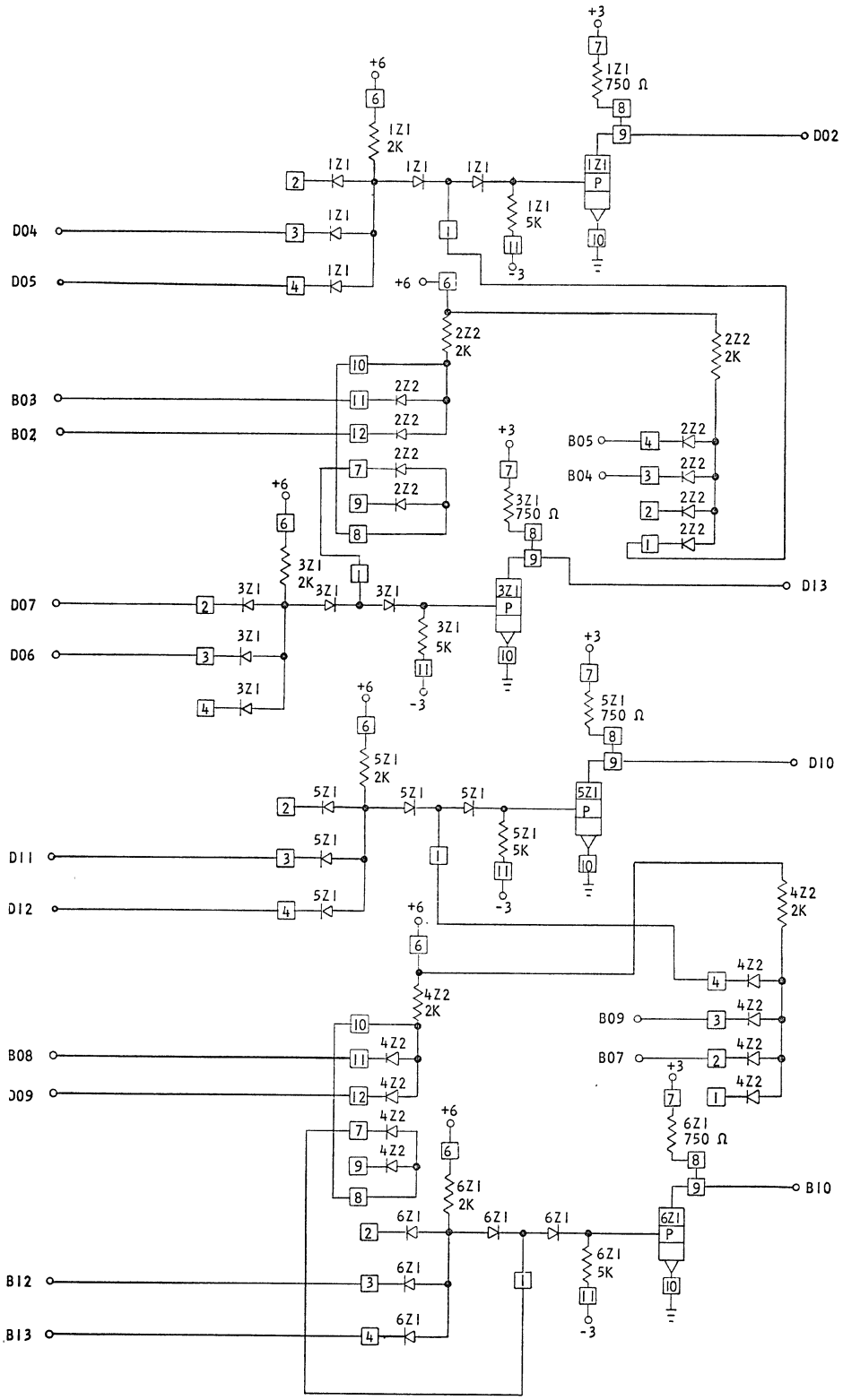
CATEGORY CODE

T03

P/N	5800006
EC	160021



P/N	5800006
EC	160021



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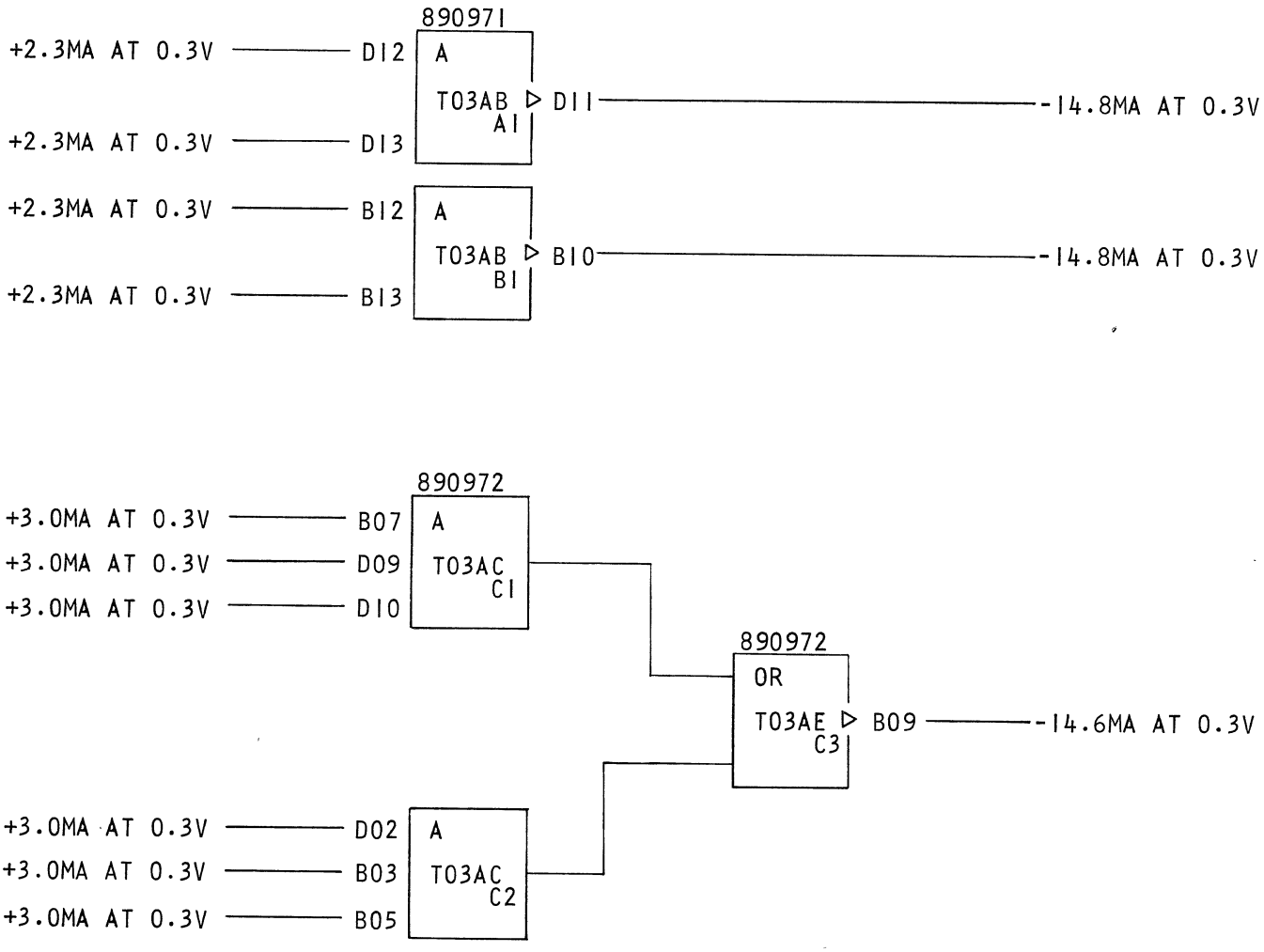
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2-3W, 3W AOI & 2-2W AI

CATEGORY CODE

T03

P/N	5800007
EC	162017
STANDARD RESTRICTED	
CARD SIZE	1-6

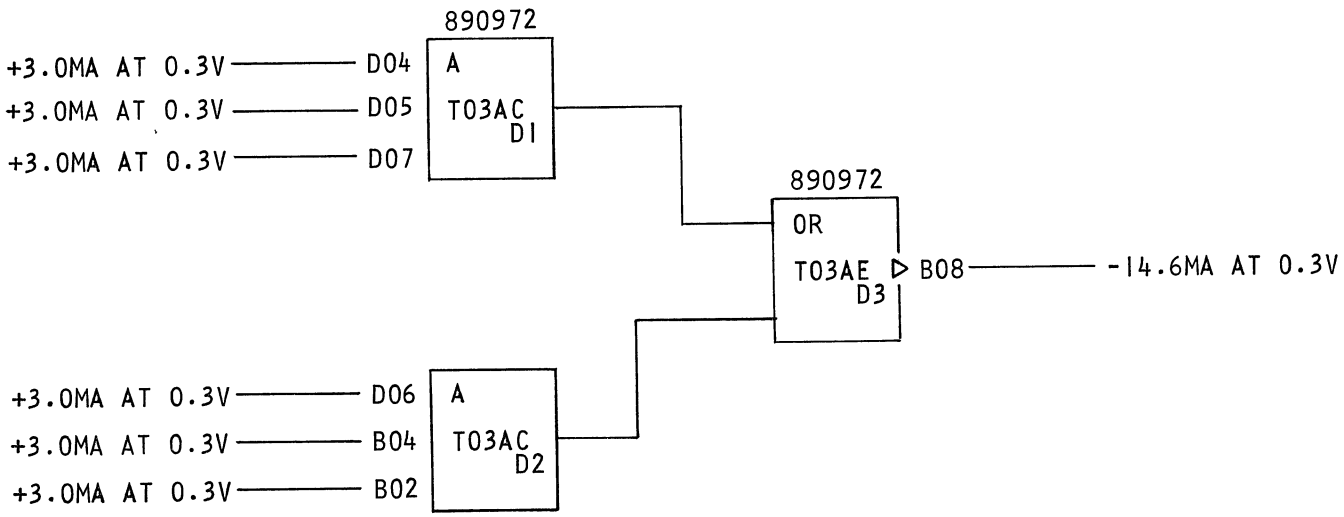


2-3W, 3W AOI & 2-2W AI

CATEGORY CODE

T03

P/N	5800007
EC	162017



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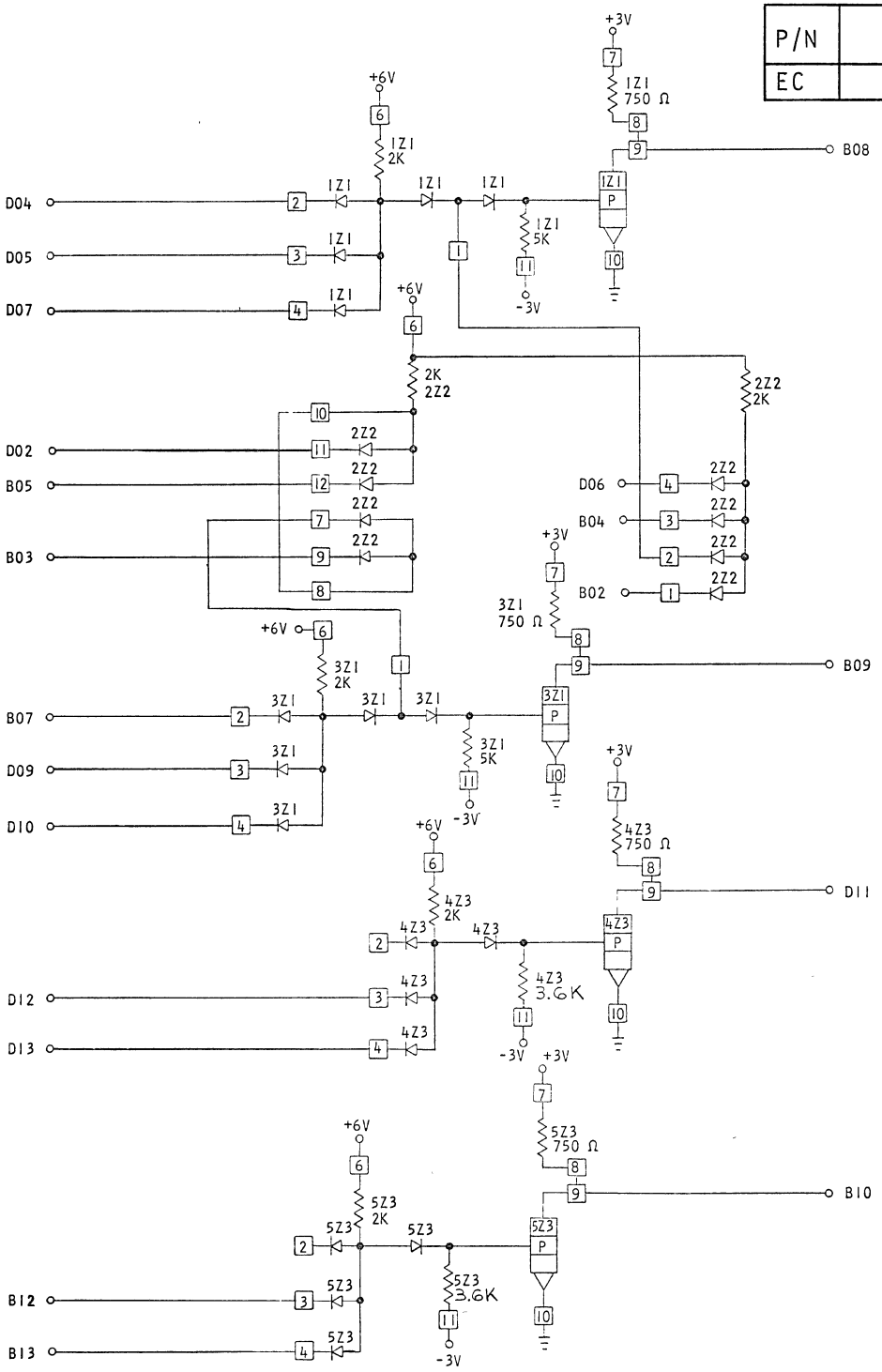
EC	162017



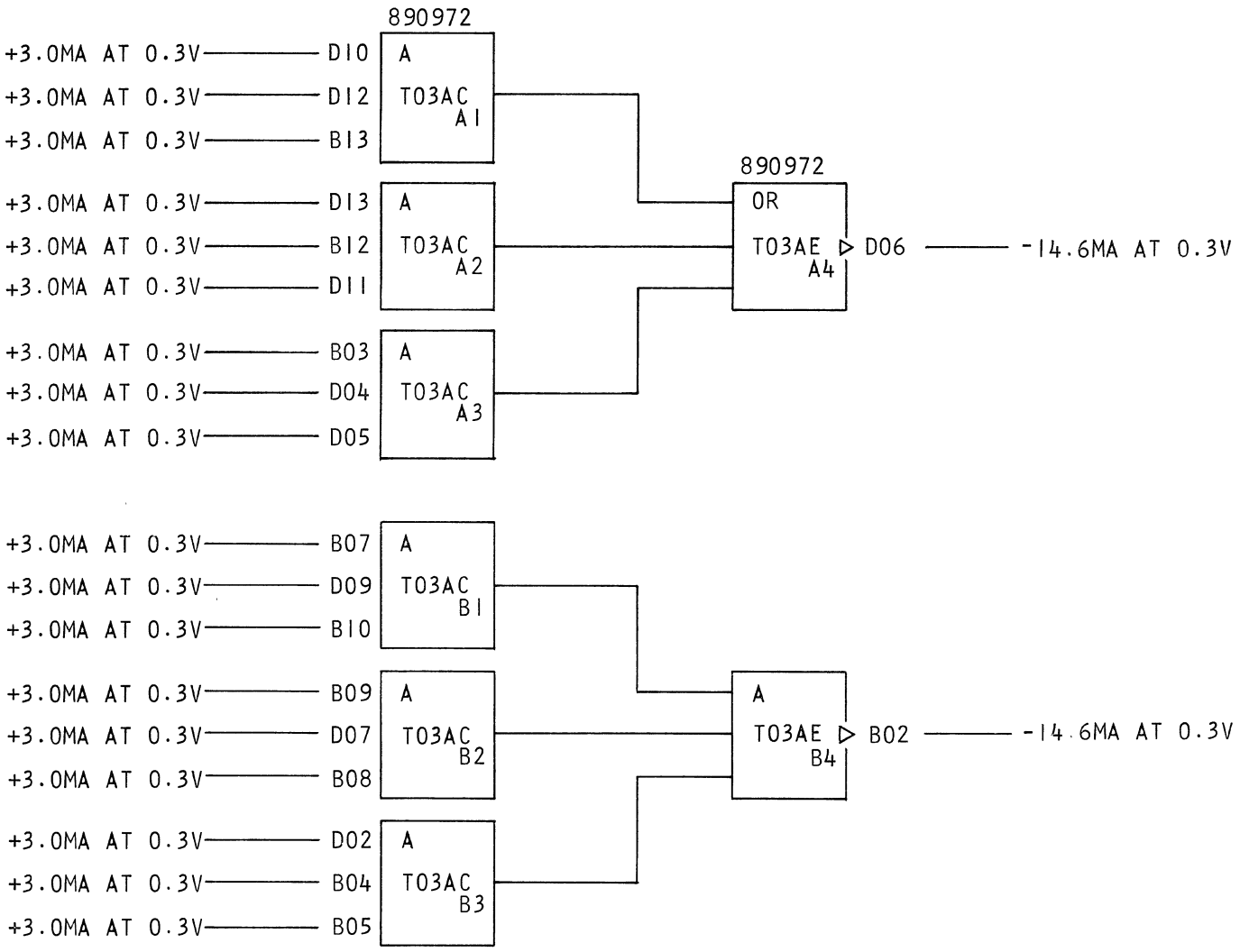
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

2-3W,3W,3W AOI

CATEGORY CODE

T03

P/N	5800008
EC	160024
STANDARD RESTRICTED	
CARD SIZE	1-6



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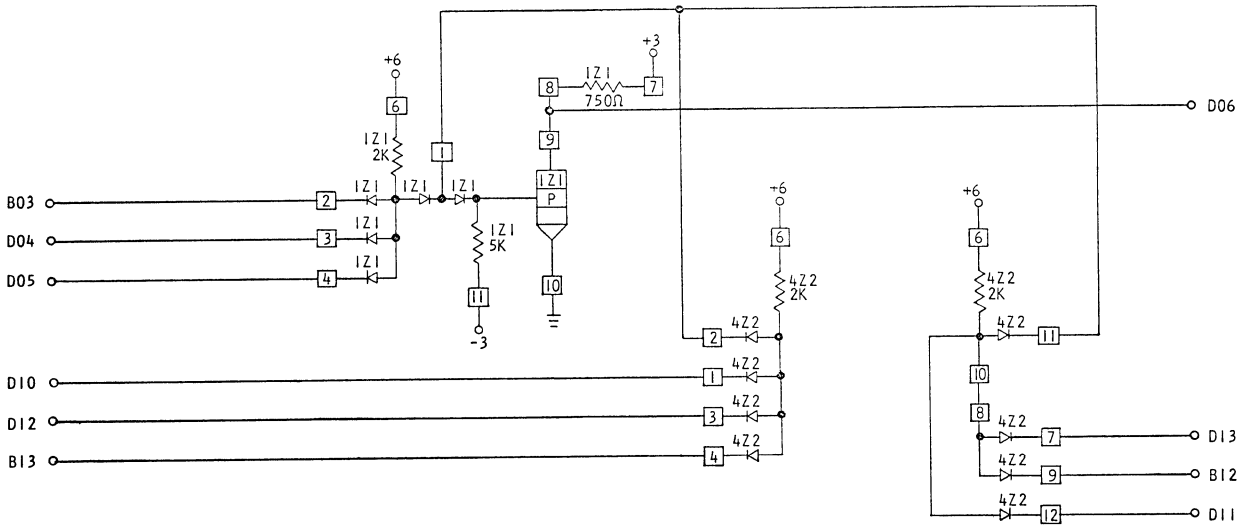
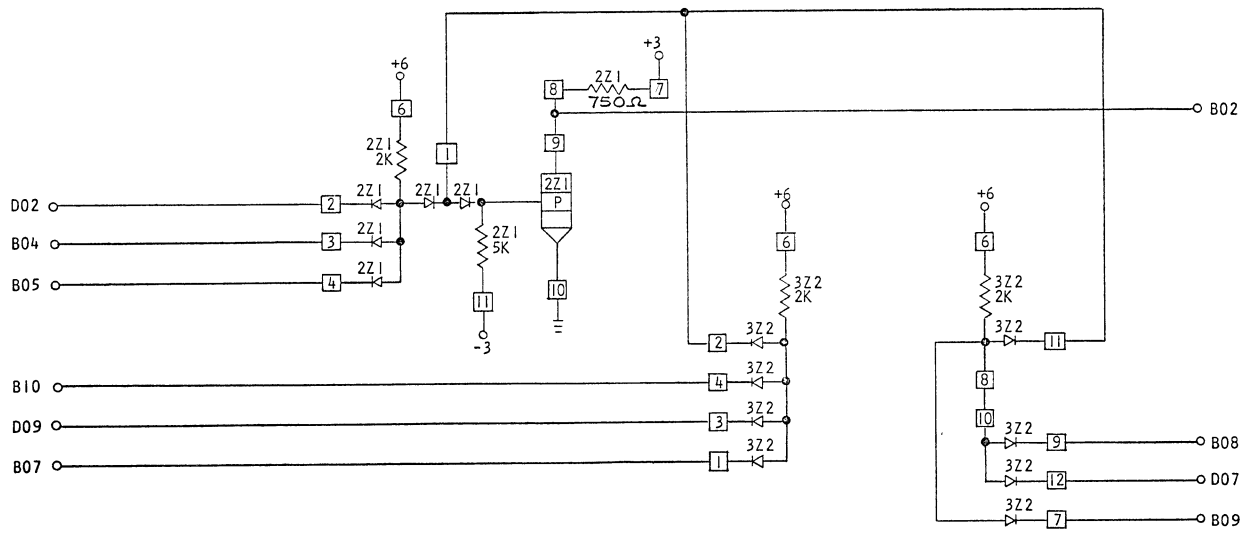
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-3W, 3W, 3W AOI

P/N	5800008
EC	160024





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POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

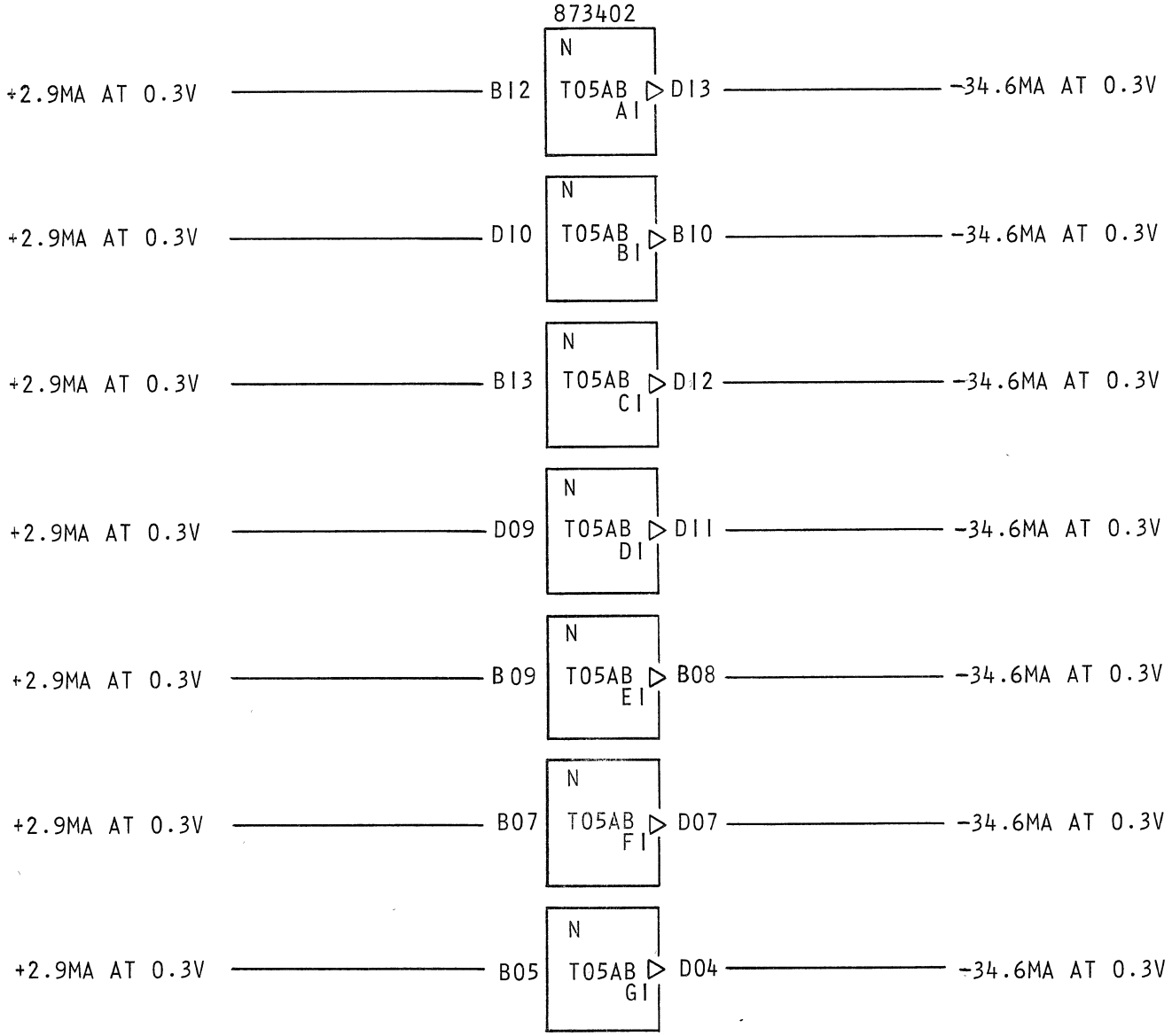
10 DCI'S

CATEGORY CODE

T05

P/N	5800009
EC	160134
STANDARD RESTRICTED	
CARD SIZE	1-6

873402



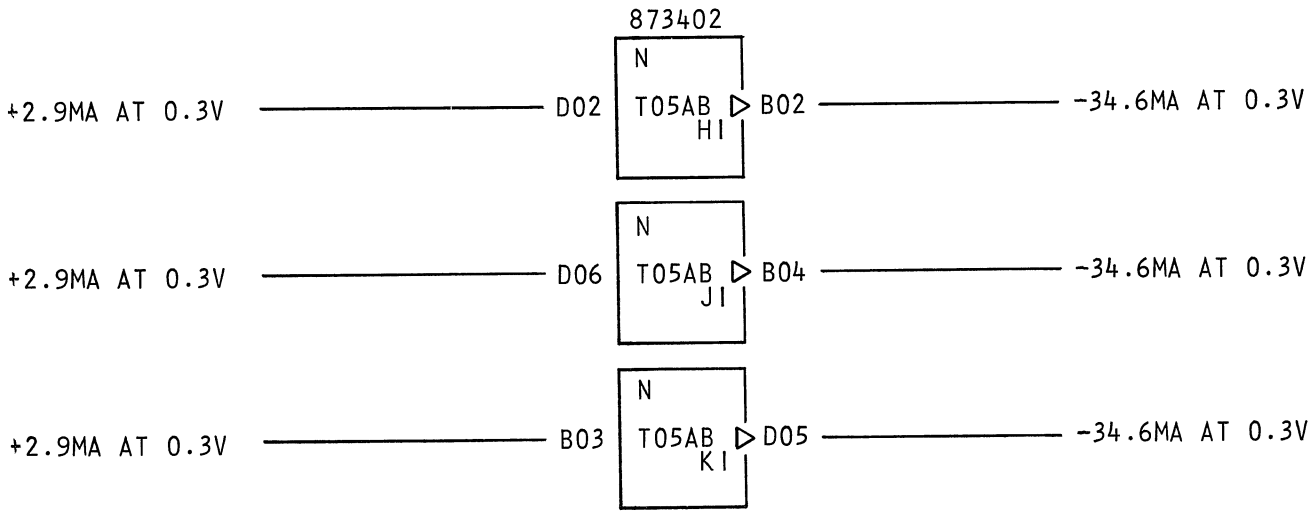
LMH Cat.	0-2860 Subject	208 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 10 DCI'S

10 DCI'S

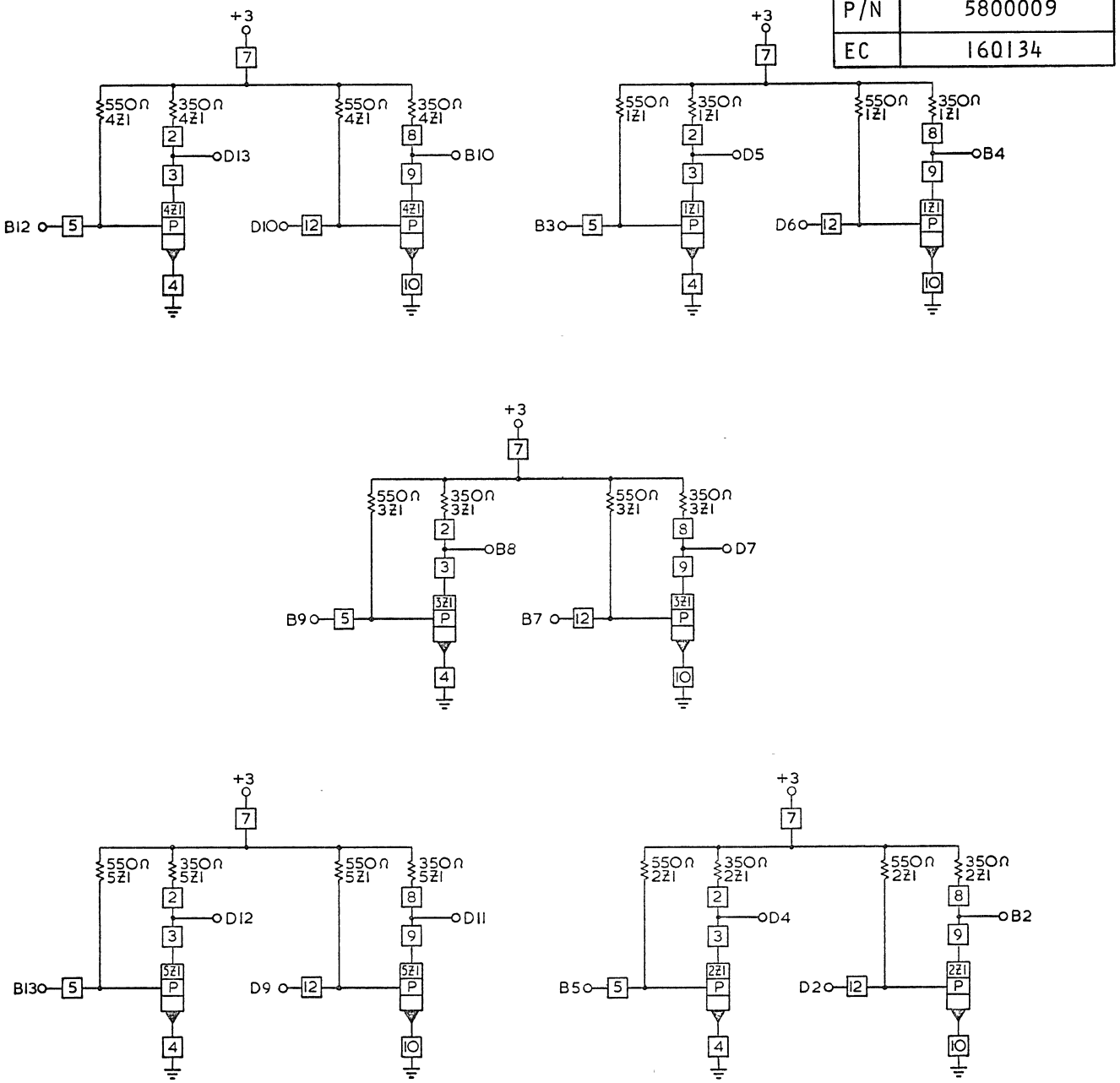
CATEGORY CODE

T05

P/N	5800009
EC	160134
STANDARD RESTRICTED	
CARD SIZE	1-6



P/N	5800009
EC	160134



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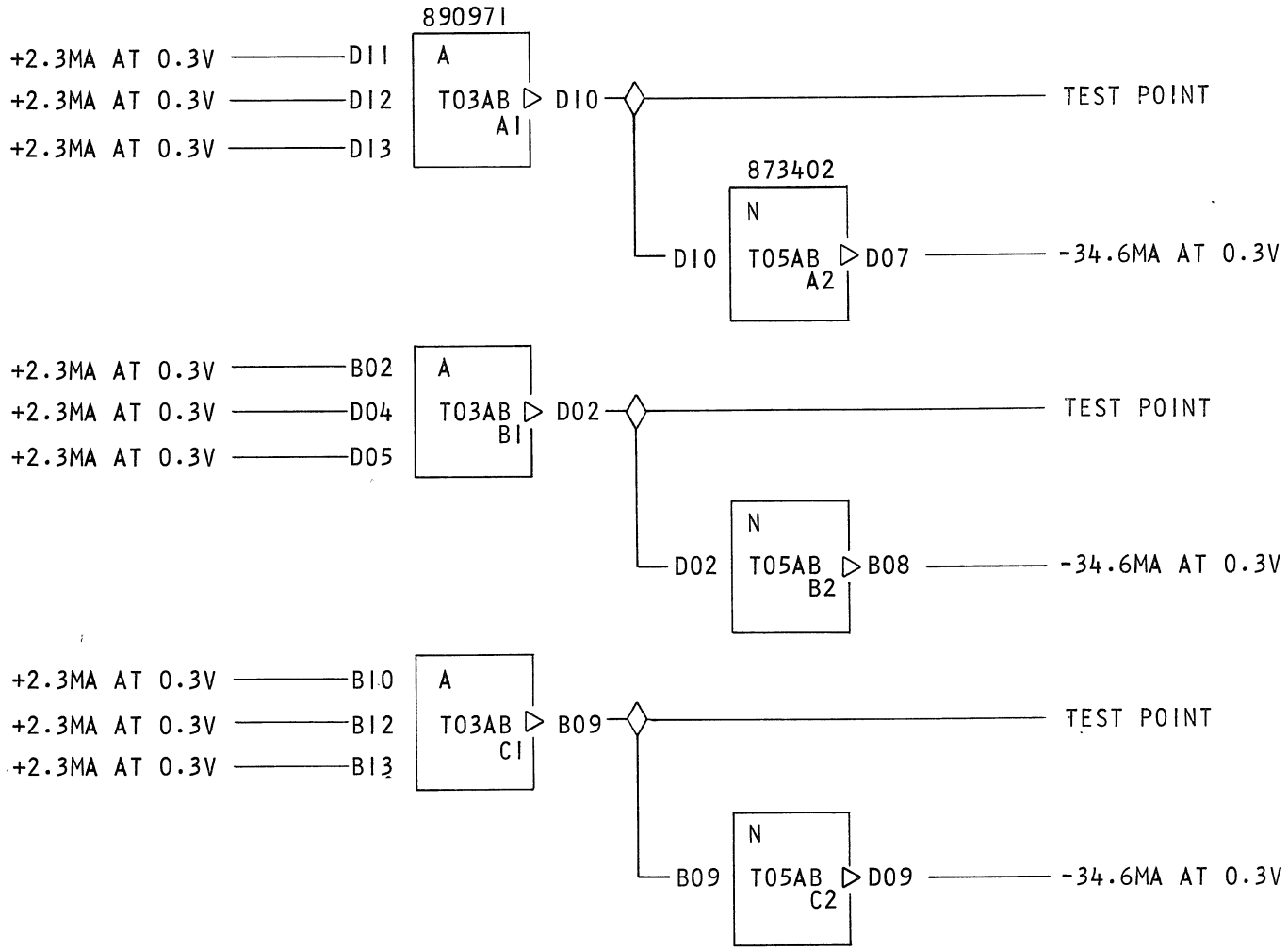
IBM Location
Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

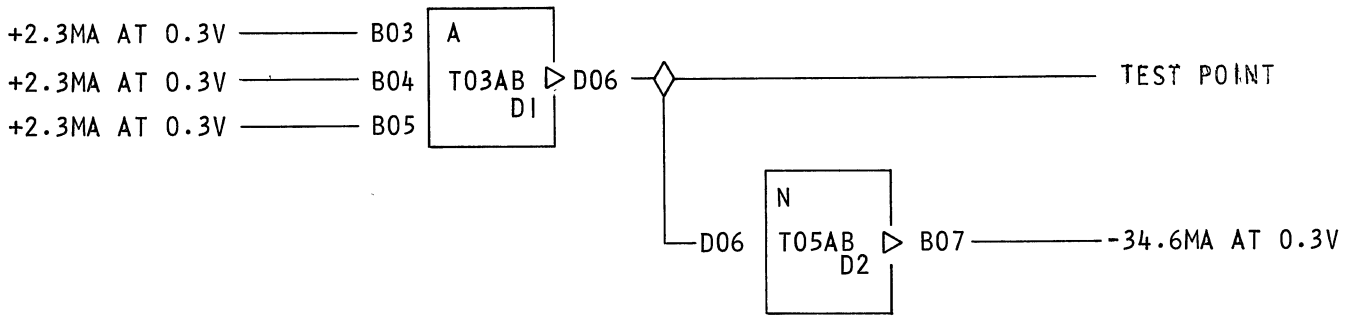
4-3W AI, DCI

P/N	5800015
EC	160135
STANDARD RESTRICTED	
CARD SIZE	1-6

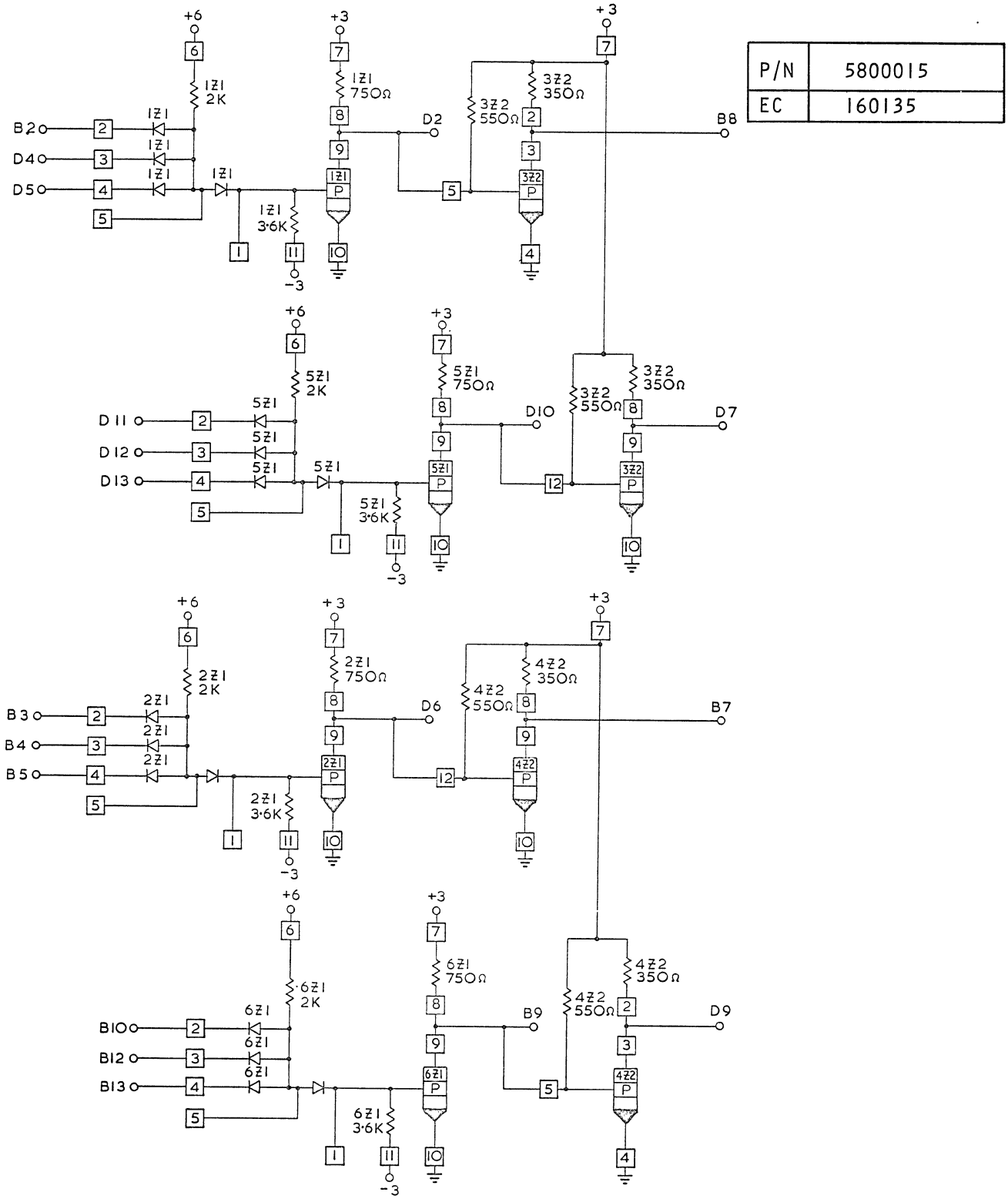


4-3W AI, DCI

P/N	5800015
EC	160135



P/N	5800015
EC	160135



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IBM Location Manufacturing Specification

NO POWER REQUIRED

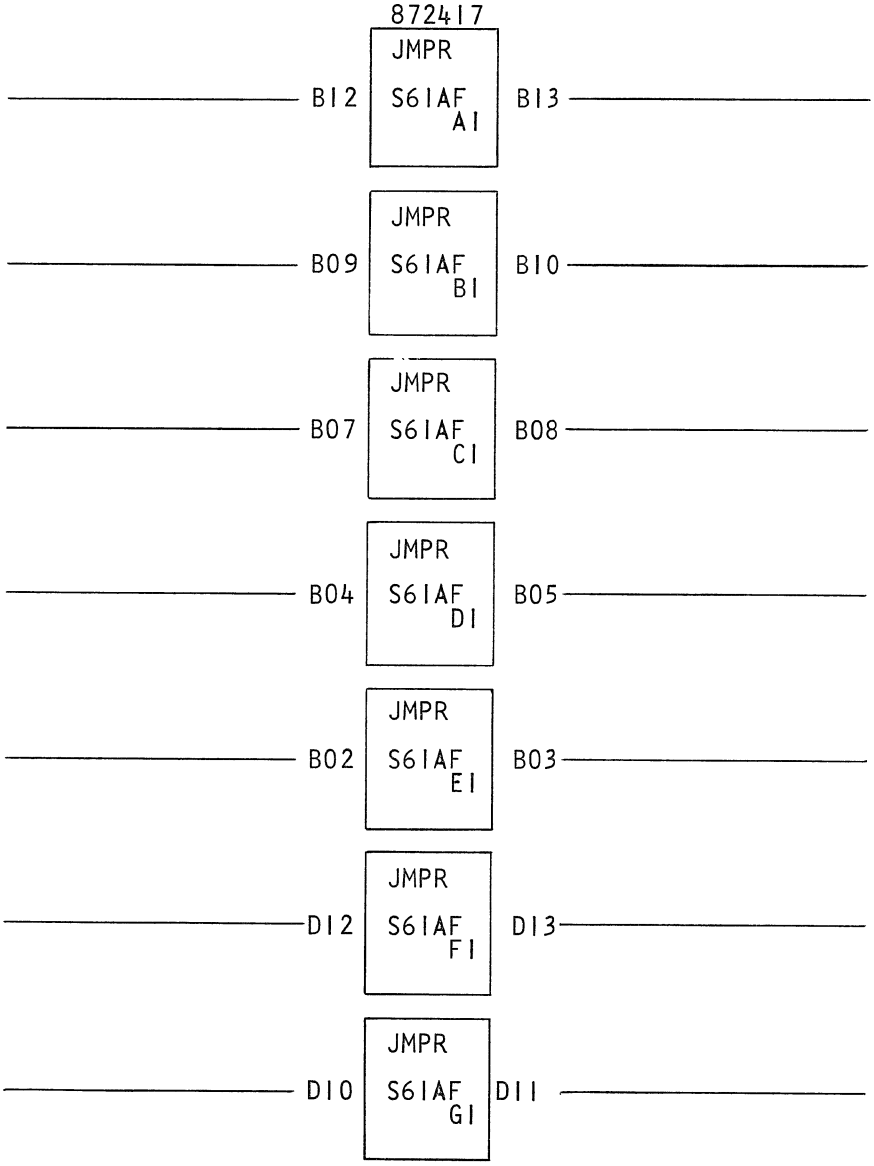
JMPR

CATEGORY CODE

S61

P/N	5800036
EC	163850 B
STANDARD ACTIVE	
CARD SIZE	1-6

872417

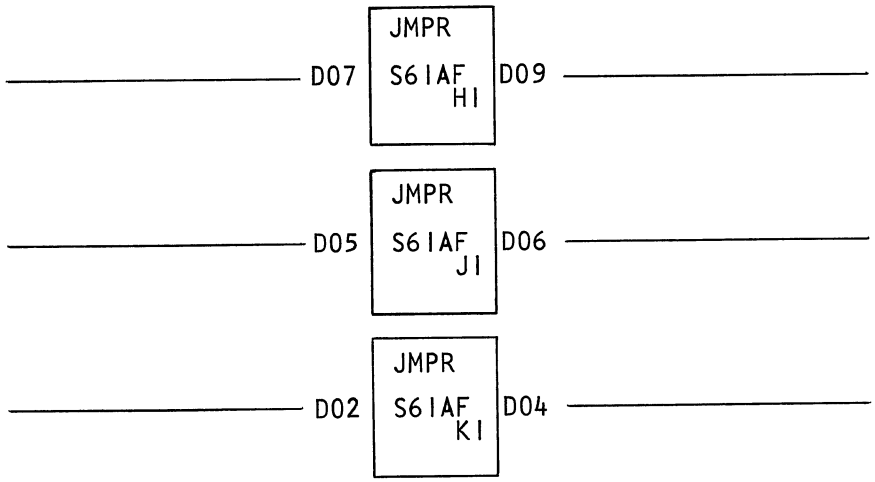


JMPR

CATEGORY CODE

S61

P/N	5800036
EC	163850 B



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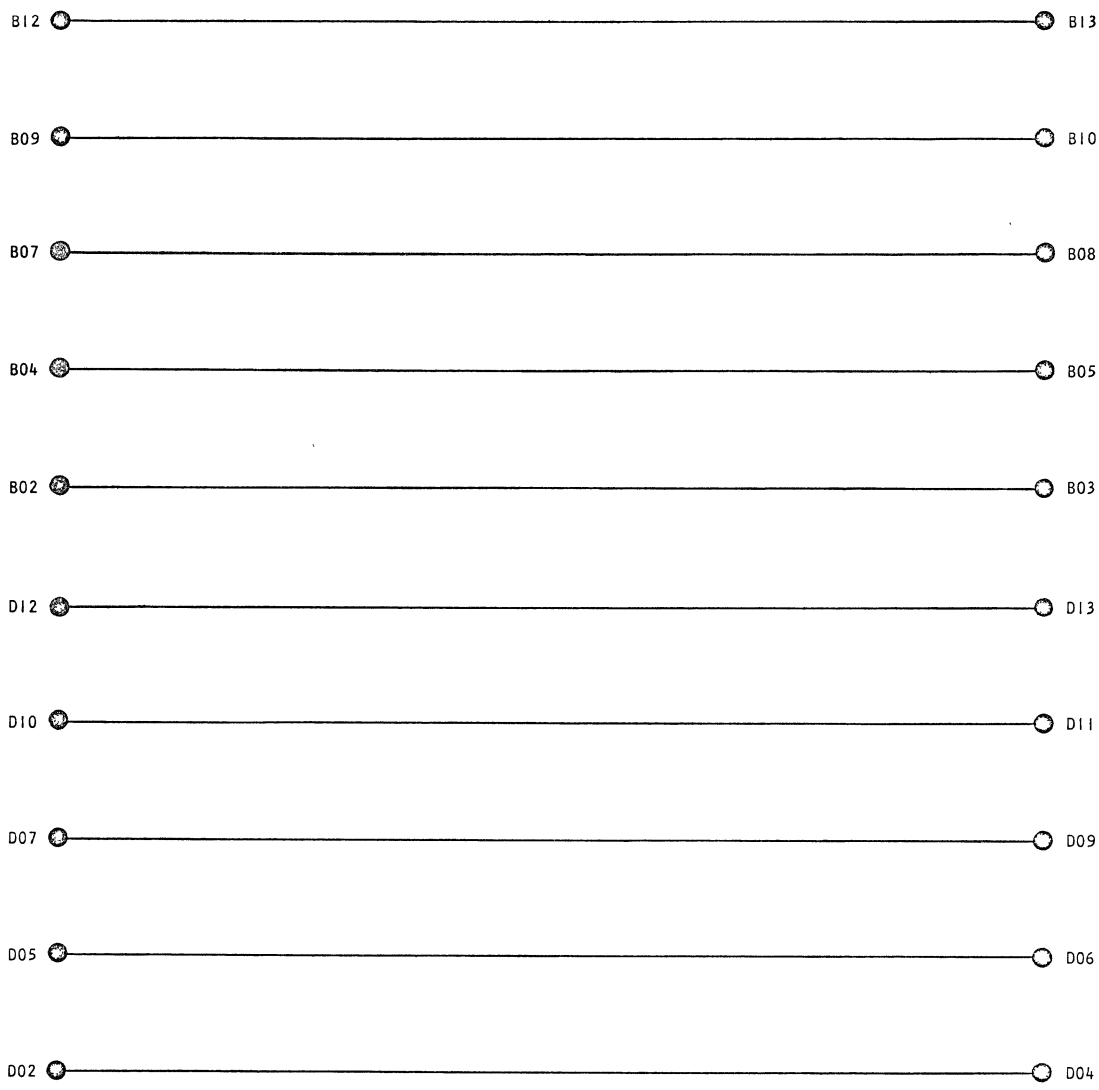
EC	163850B



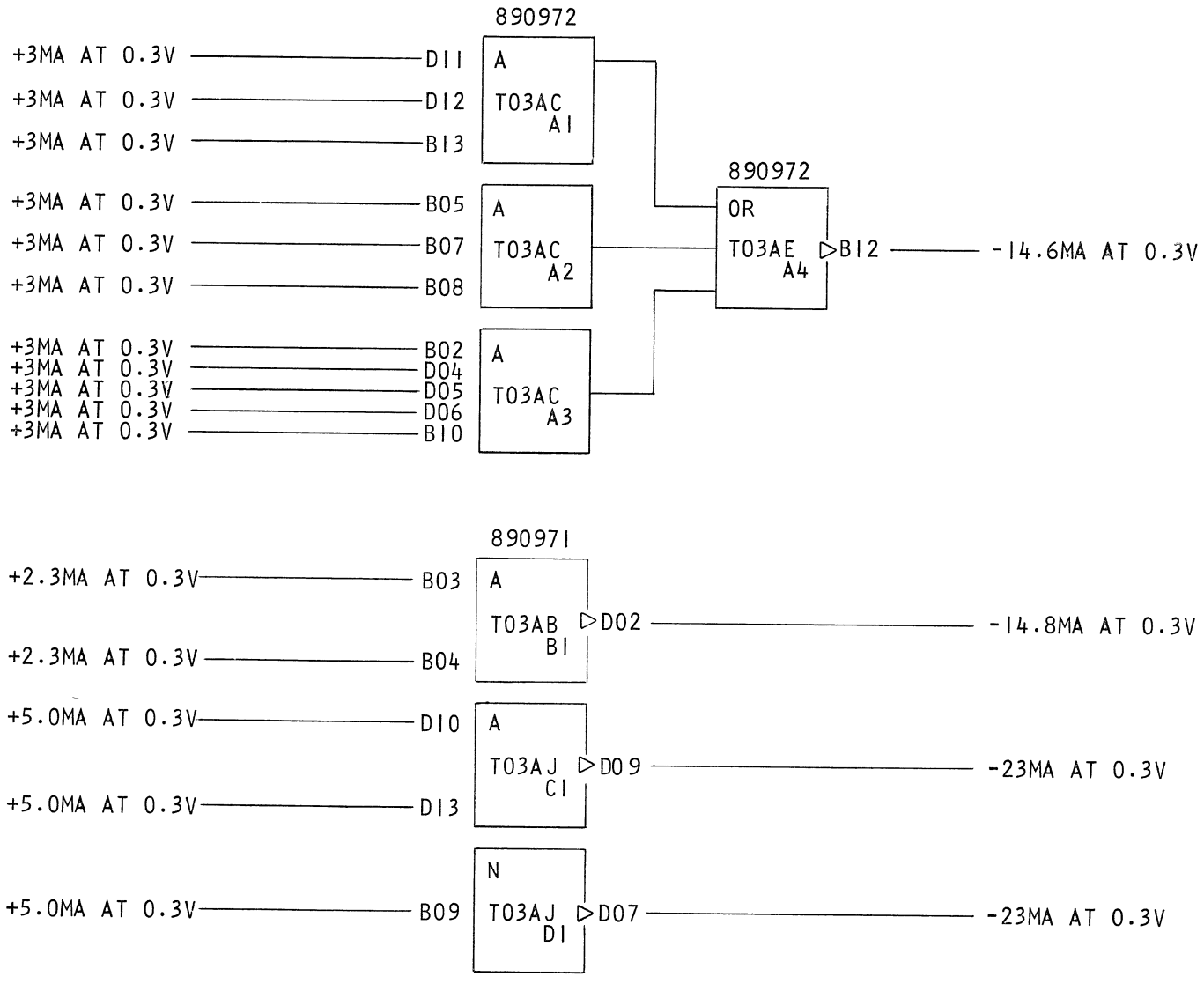
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

1-3W,3W,5W AOI & 1-2W AI & 1-1W API & 1-2W API

CATEGORY CODE

T03

P/N	5800061
EC	164896A
STANDARD ACTIVE	
CARD SIZE	1-6



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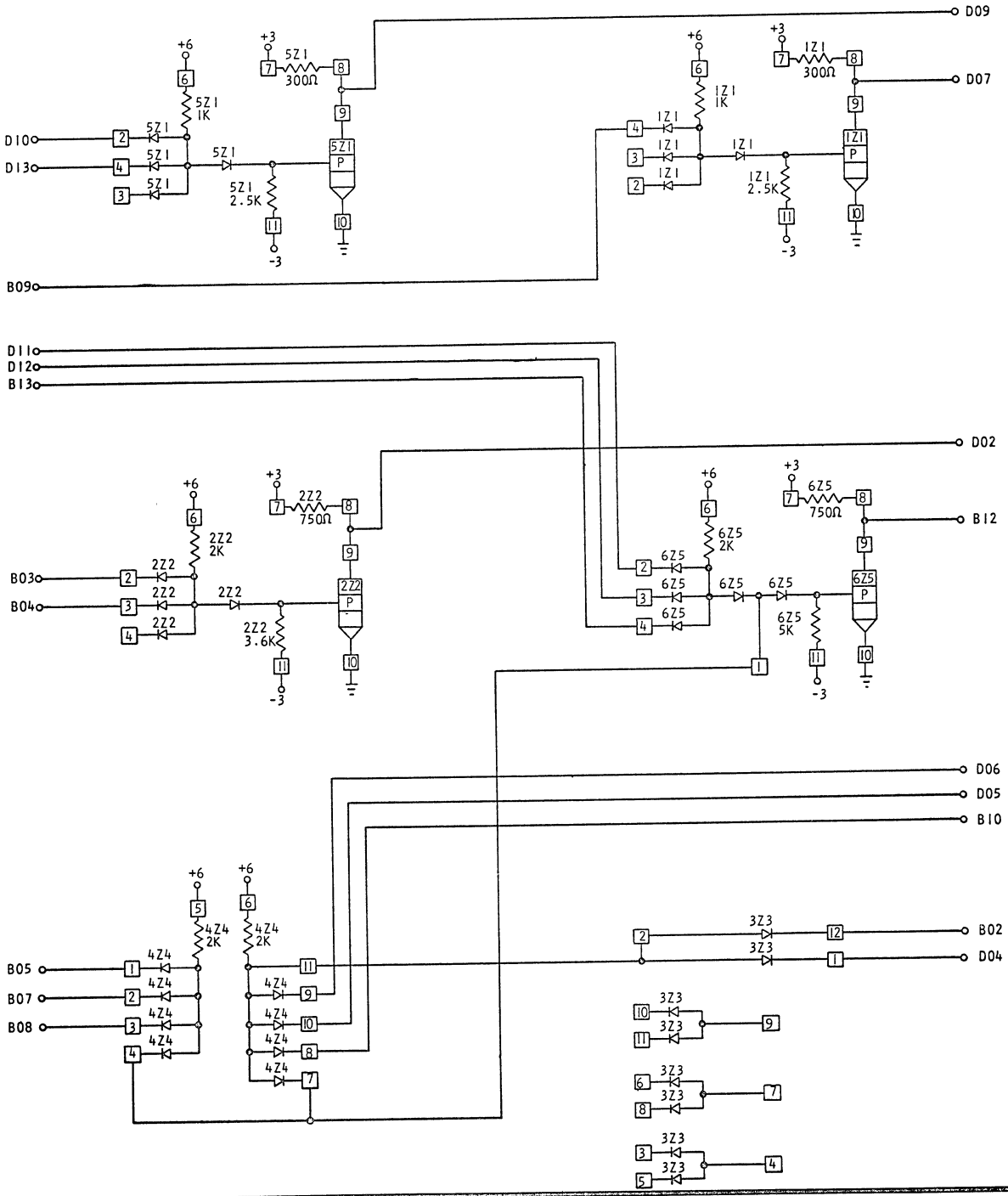
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-3W, 3W, 5W AOI & 1-2W AI & 1-1W API & 1-2W API

P/N	5800061
EC	164896A



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-2W,2W,2W,2W AOI & 1-2W,2W,3W,3W AOI

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Cat.	Subject	Suffix

IBM Location Manufacturing Specification

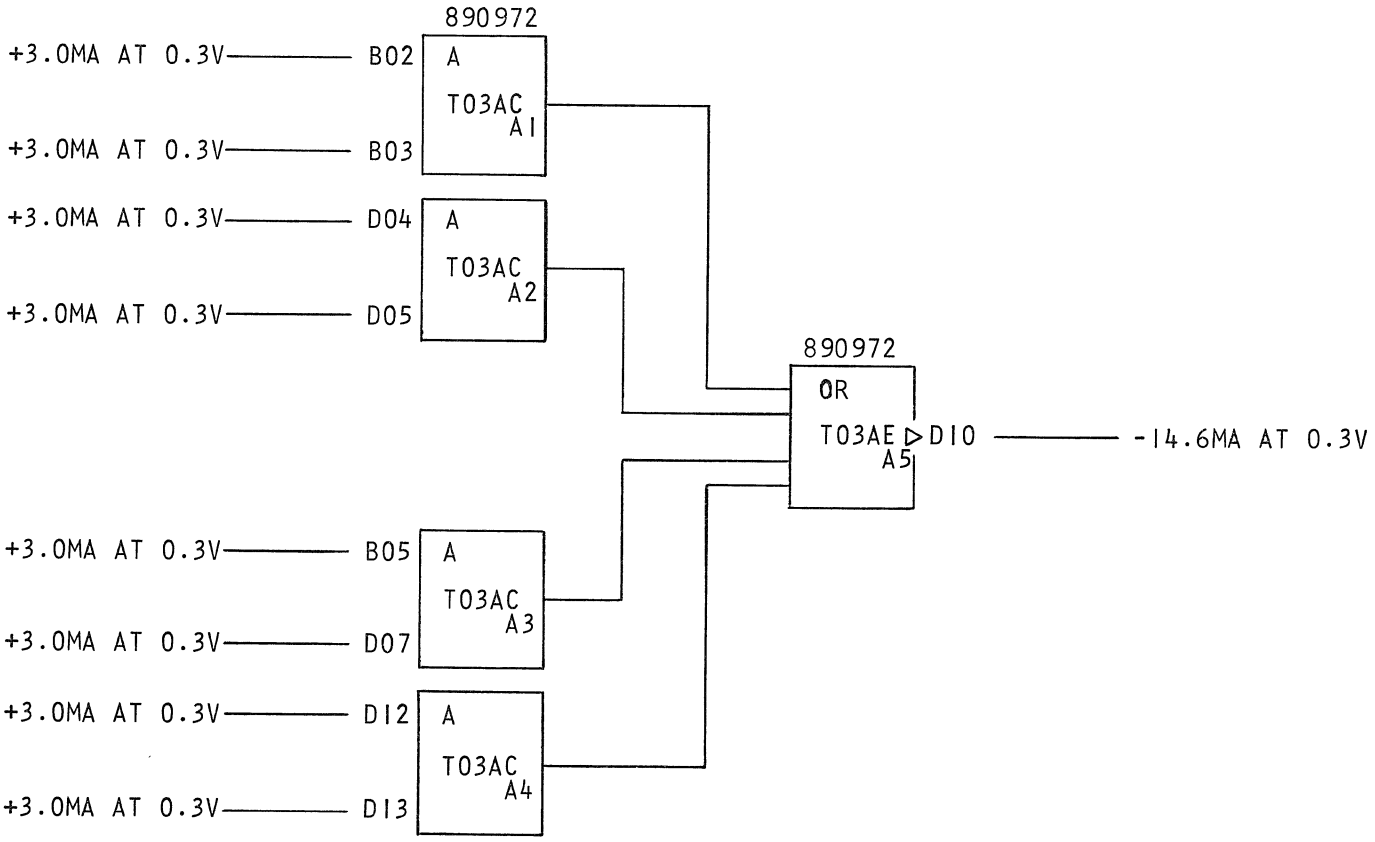
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1-2W,2W,2W,2W AOI & 1-2W,2W,3W,3W AOI

CATEGORY CODE

T03

P/N	5800064
EC	162222
STANDARD ACTIVE	
CARD SIZE	1-6



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERRING

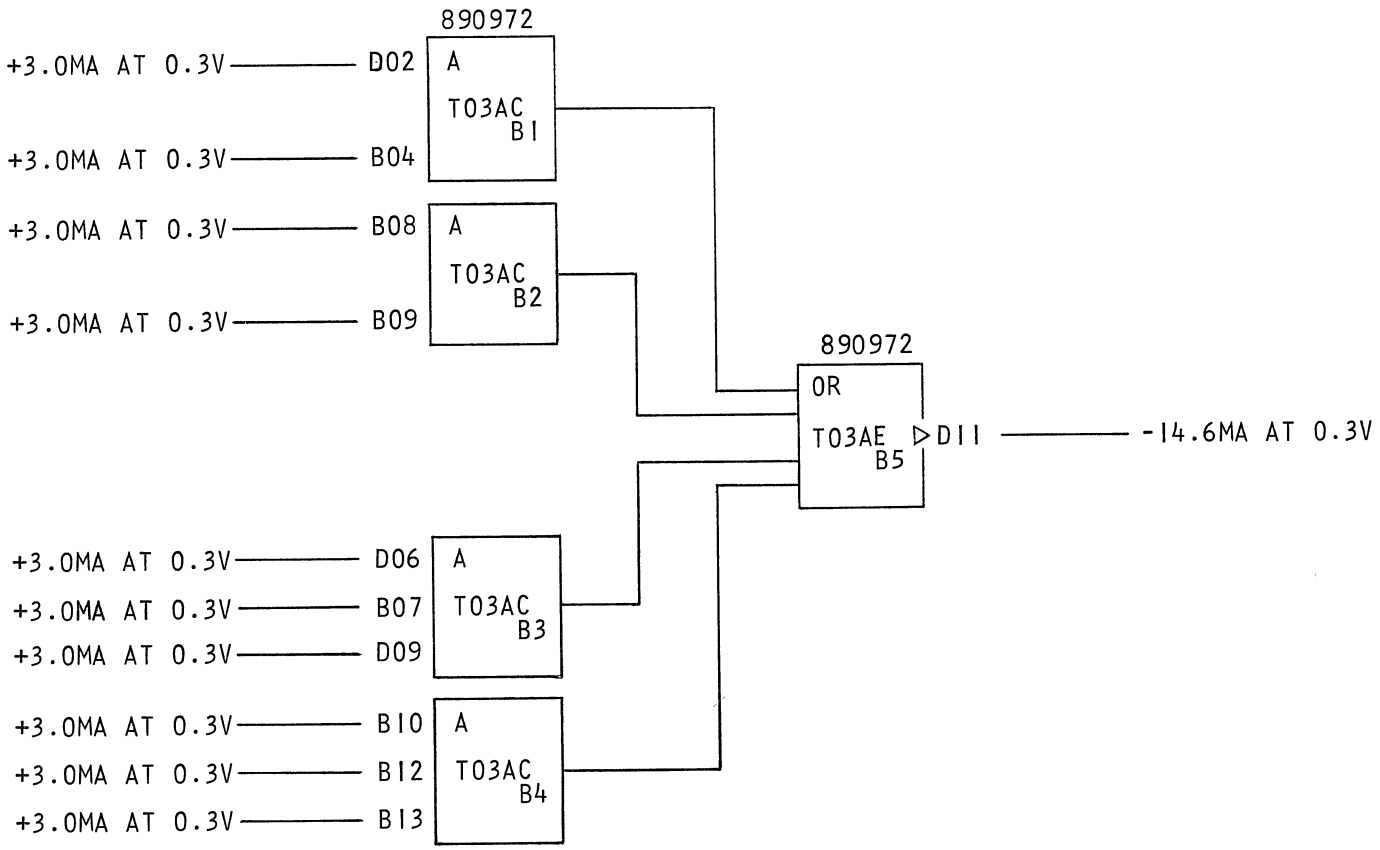
1-2W,2W,2W,2W AOI & 1-2W,2W,3W,3W AOI

P/N	5800064
EC	162222

1-2W,2W,2W,2W AOI & 1-2W,2W,3W,3W AOI

CATEGORY CODE

T03



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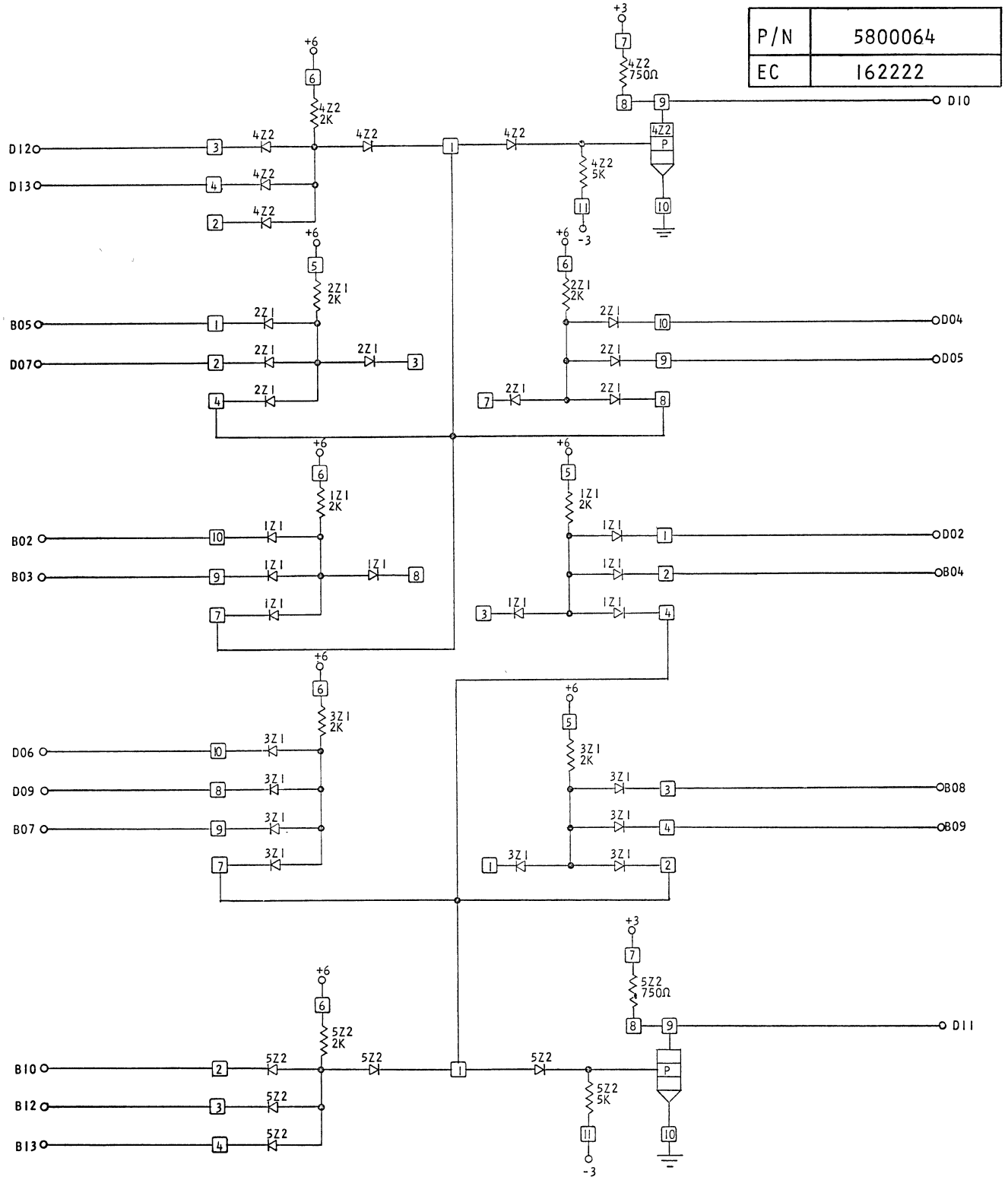

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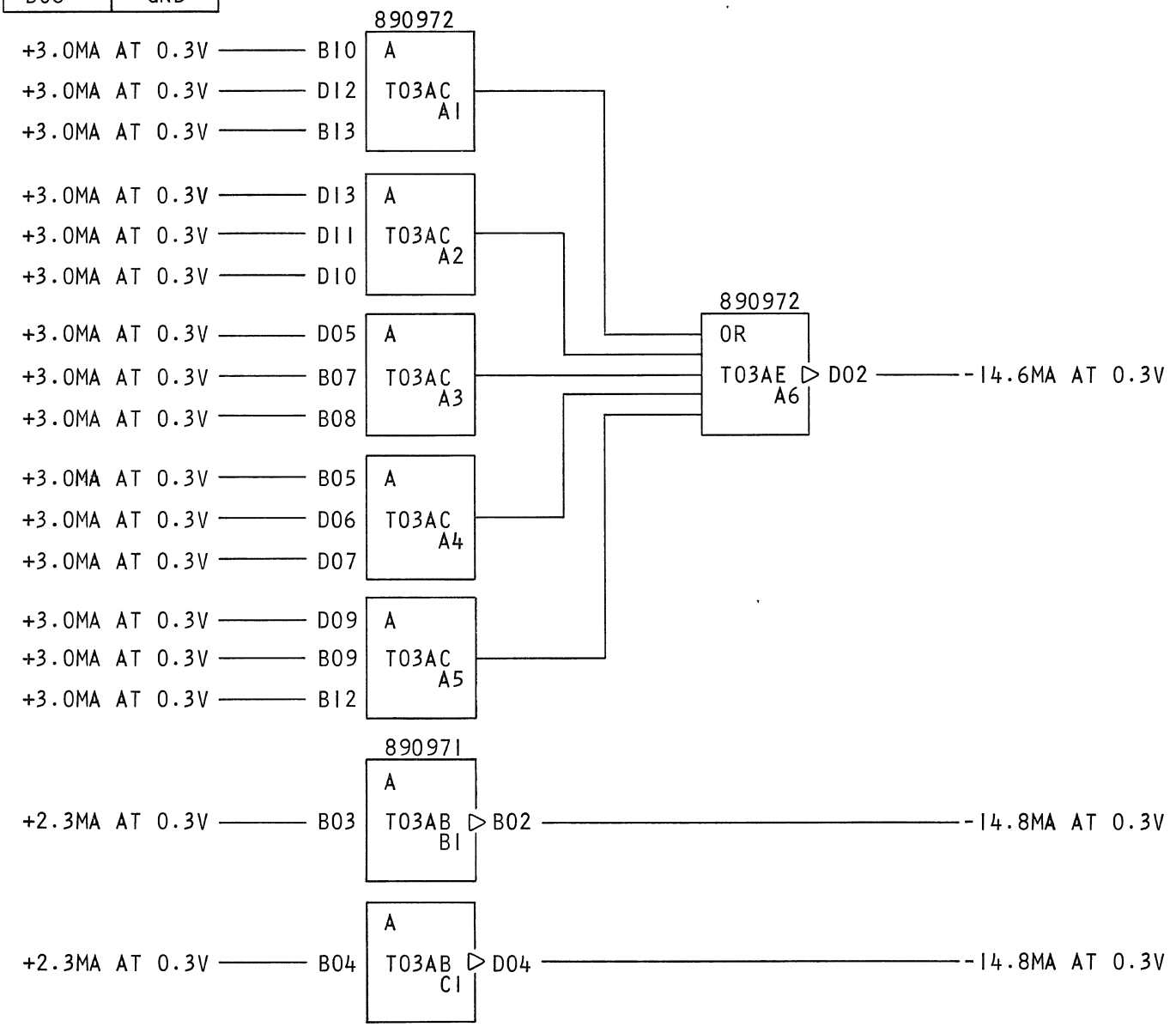
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1-3W, 3W, 3W, 3W, 3W AOI & 2-1W AI

CATEGORY CODE

T03

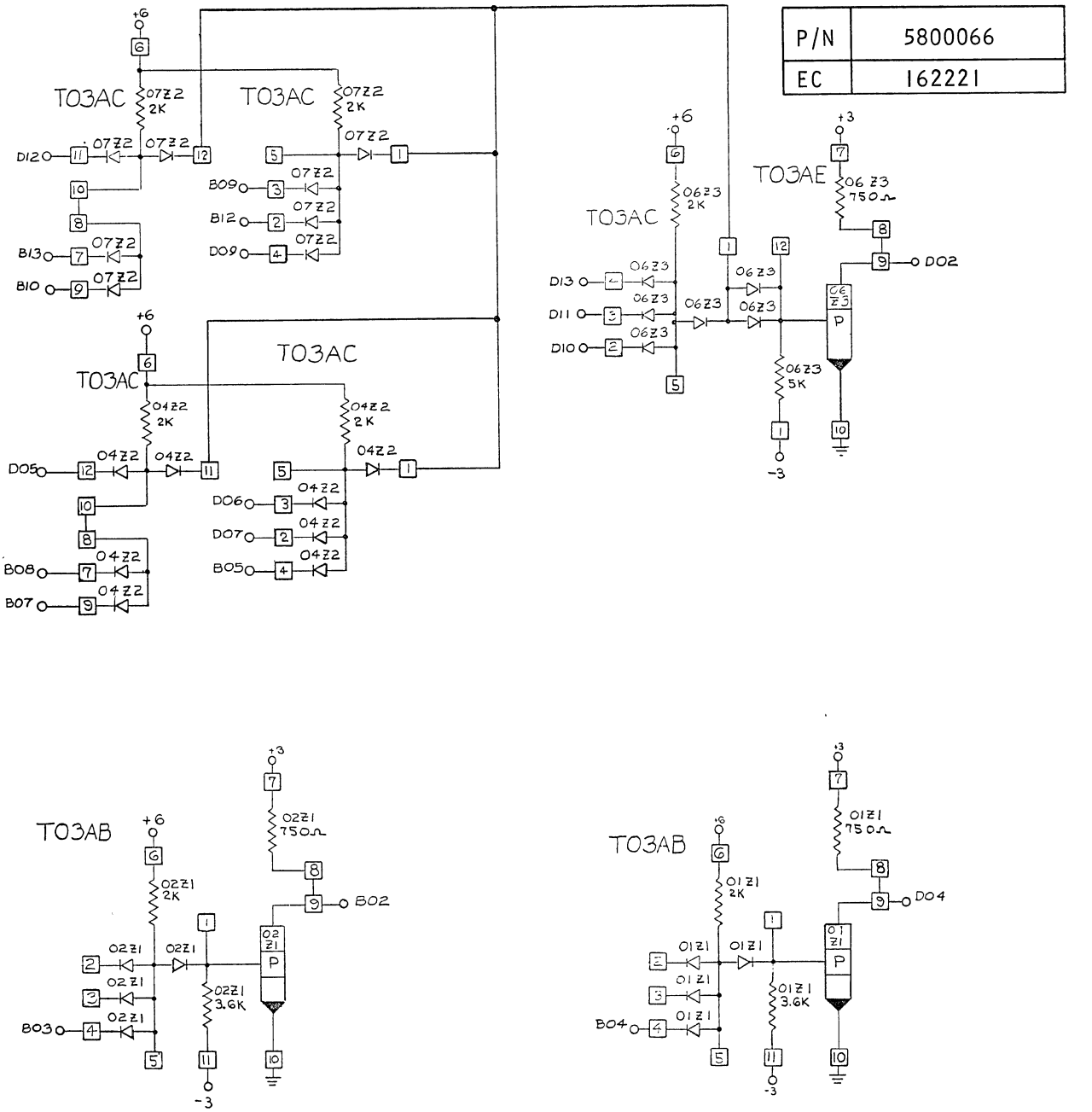
P/N	5800066
EC	162221
STANDARD RESTRICTED	
CARD SIZE	1-6



LMH	0-2860	213
Cat.	Subject	Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-3W,3W, 3W,3W,3W AOI & 2-1W AI

P/N	5800066
EC	162221



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Page	Date

IBM Location
Manufacturing Specification

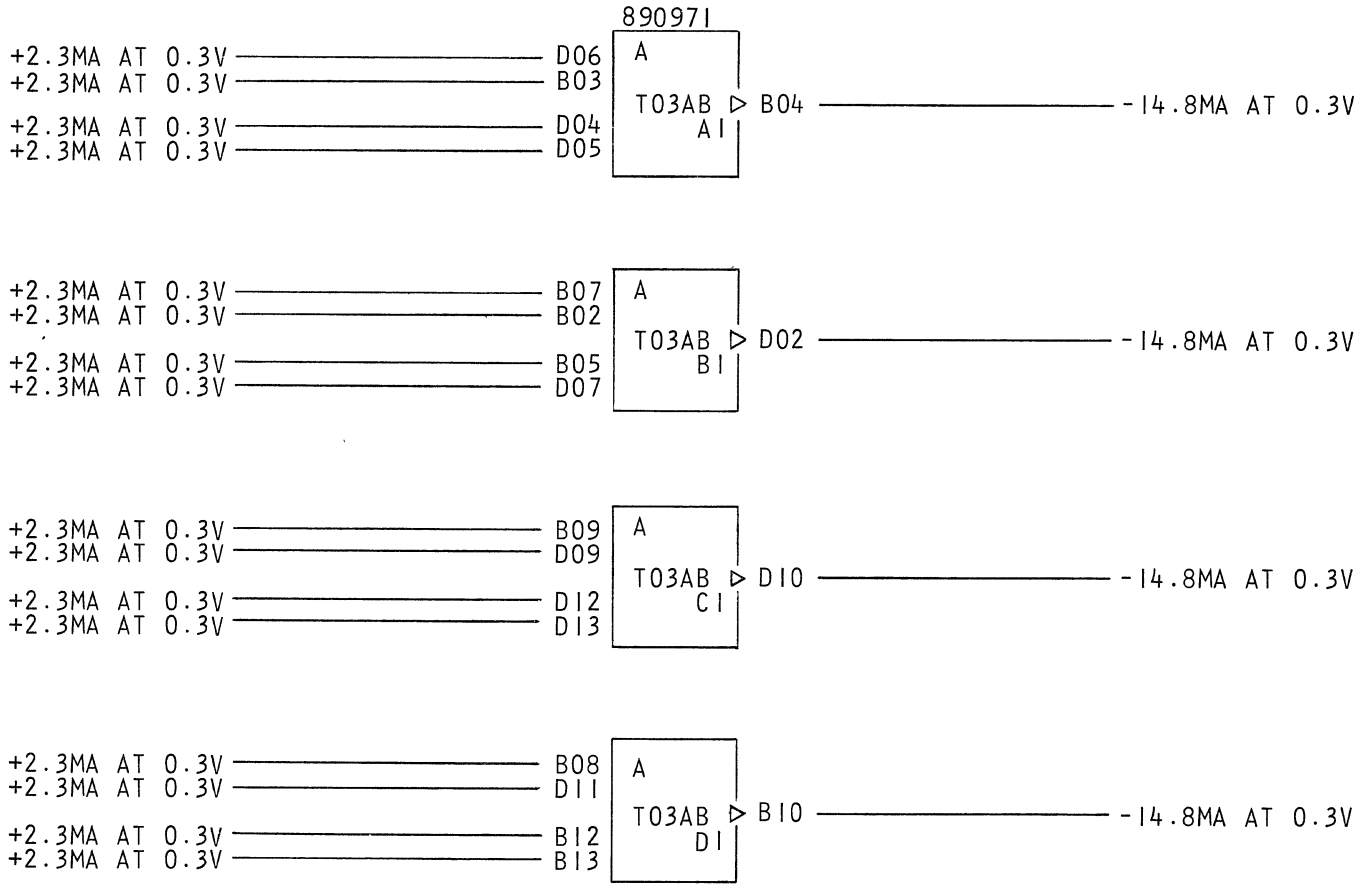
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

4-4W AI

CATEGORY CODE

T03

P/N	5800069
EC	162692
STANDARD ACTIVE	
CARD SIZE	1-6



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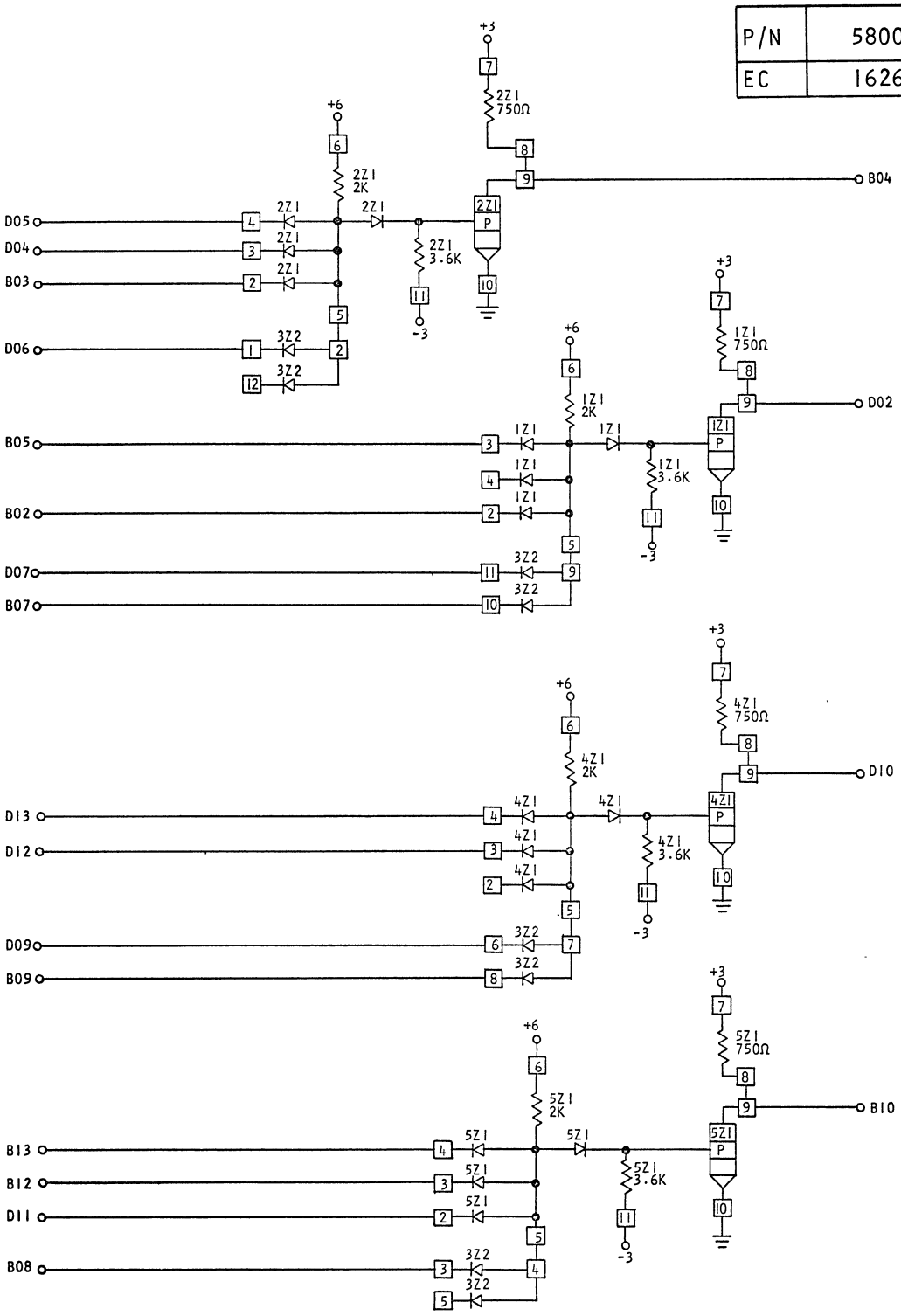
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-4W AI

P/N	5800069
EC	162692



IBM **Location Manufacturing Specification**

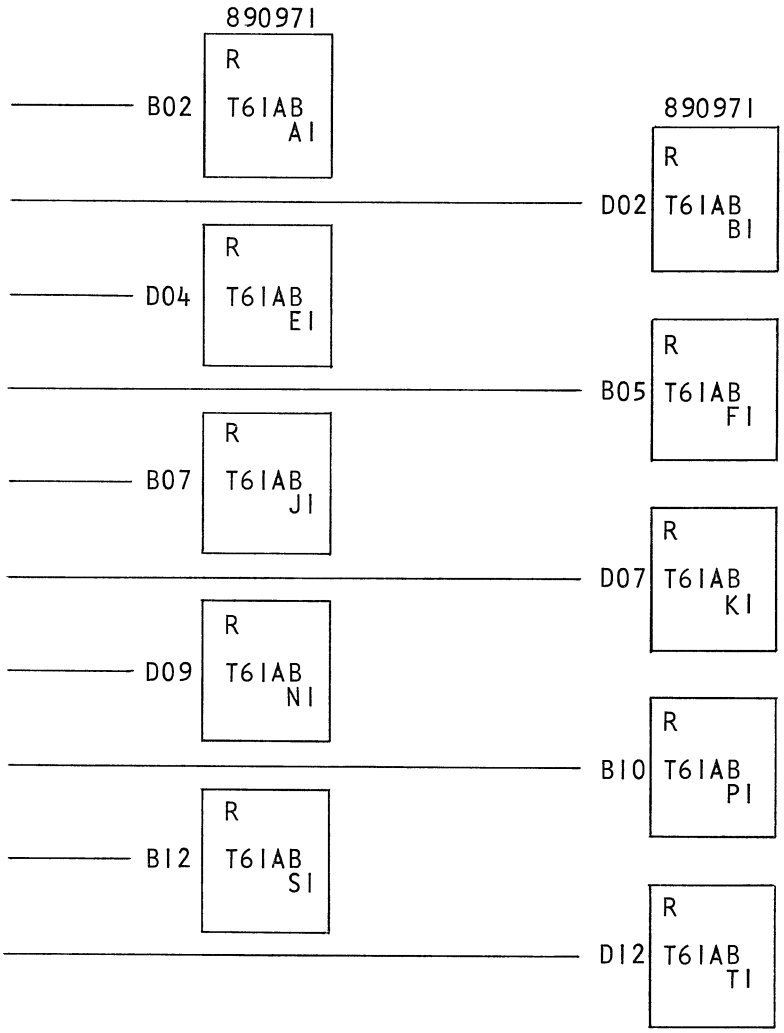
POWER REQUIRED	
PIN	VOLTS
B11	+6
D08	GND

20-750 OHM LOAD RESISTORS TO +6V

CATEGORY CODE

T61

P/N	5800099
EC	160521
SPECIAL RESTRICTED	
CARD SIZE	1-6

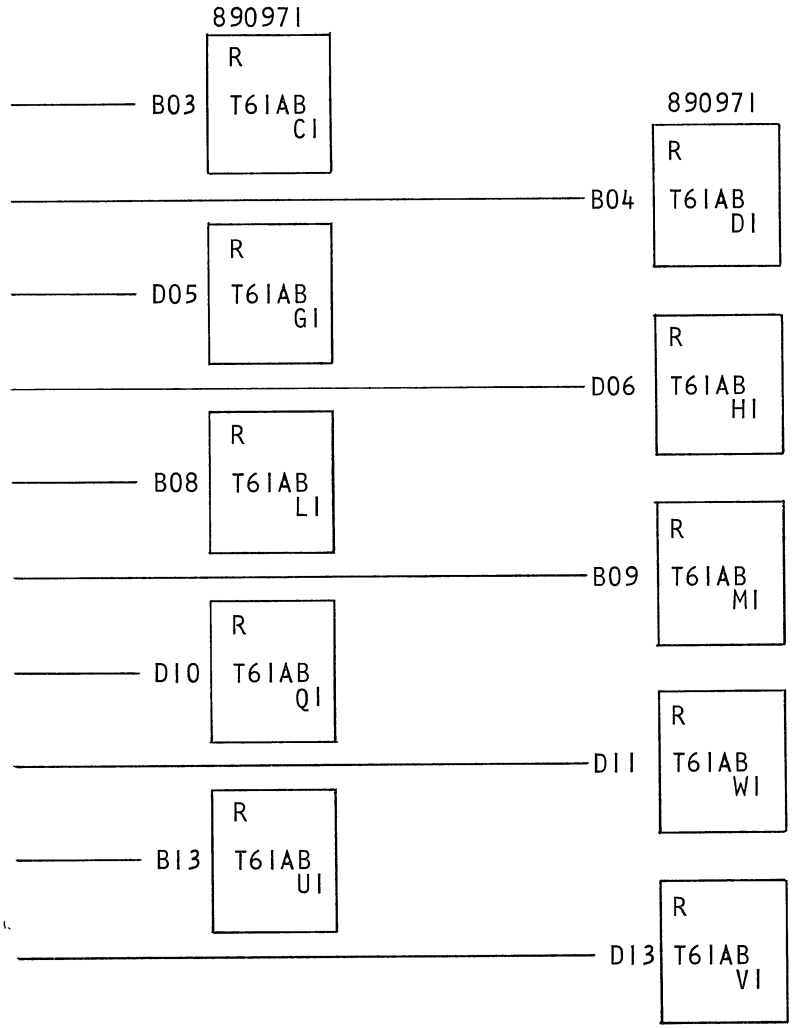


NOTE:
MAXIMUM LOAD CURRENT 8.4 MA AT 0.3 V FOR ALL RESISTORS

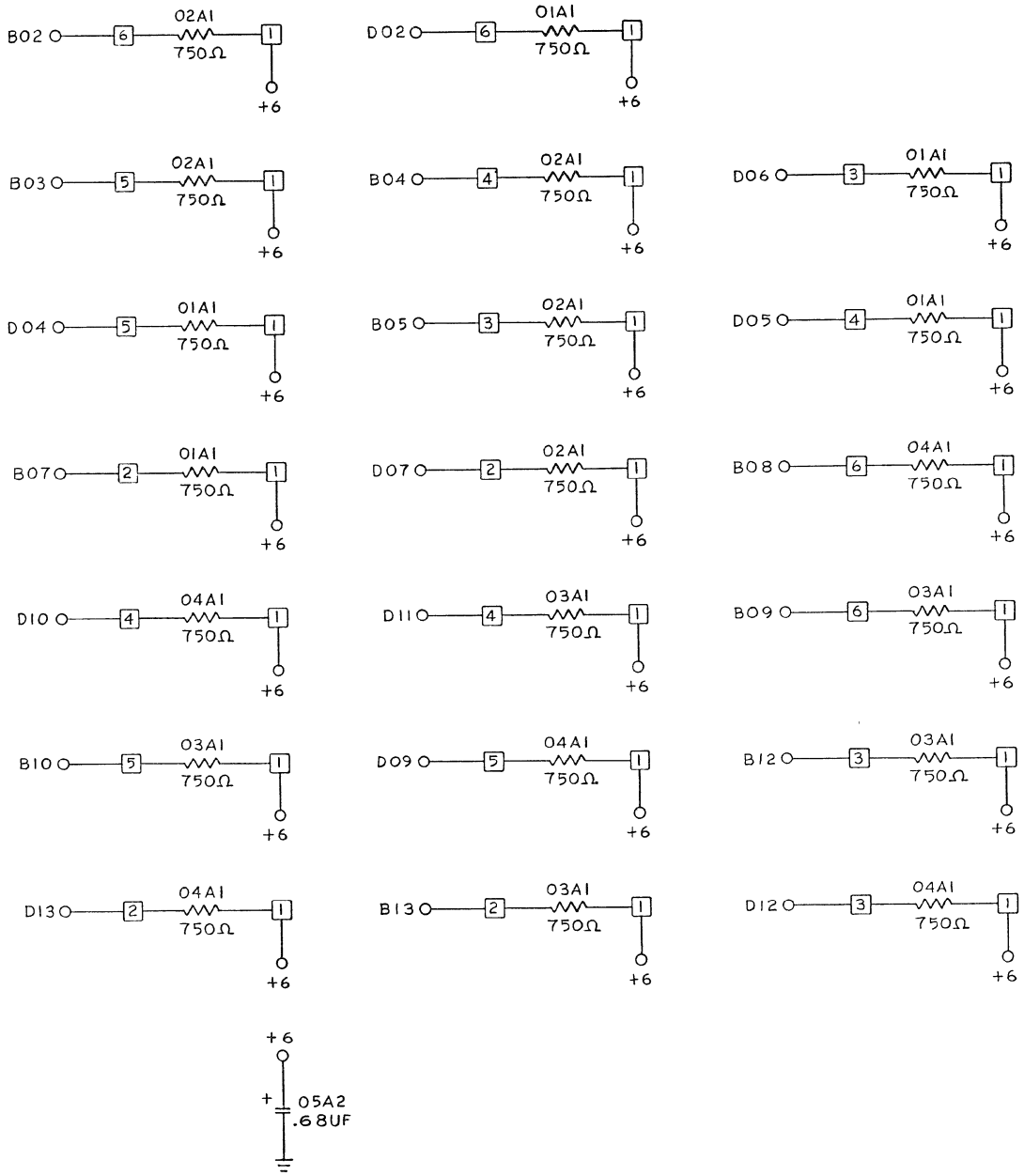
20-750 OHM LOAD RESISTORS TO +6V

T61

P/N	5800099
EC	160521



P/N	5800099
EC	160521



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-2W AI & 1-6W AI & 1-1W API & 1-2W,2W AOI

LMH	0-2860	217
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

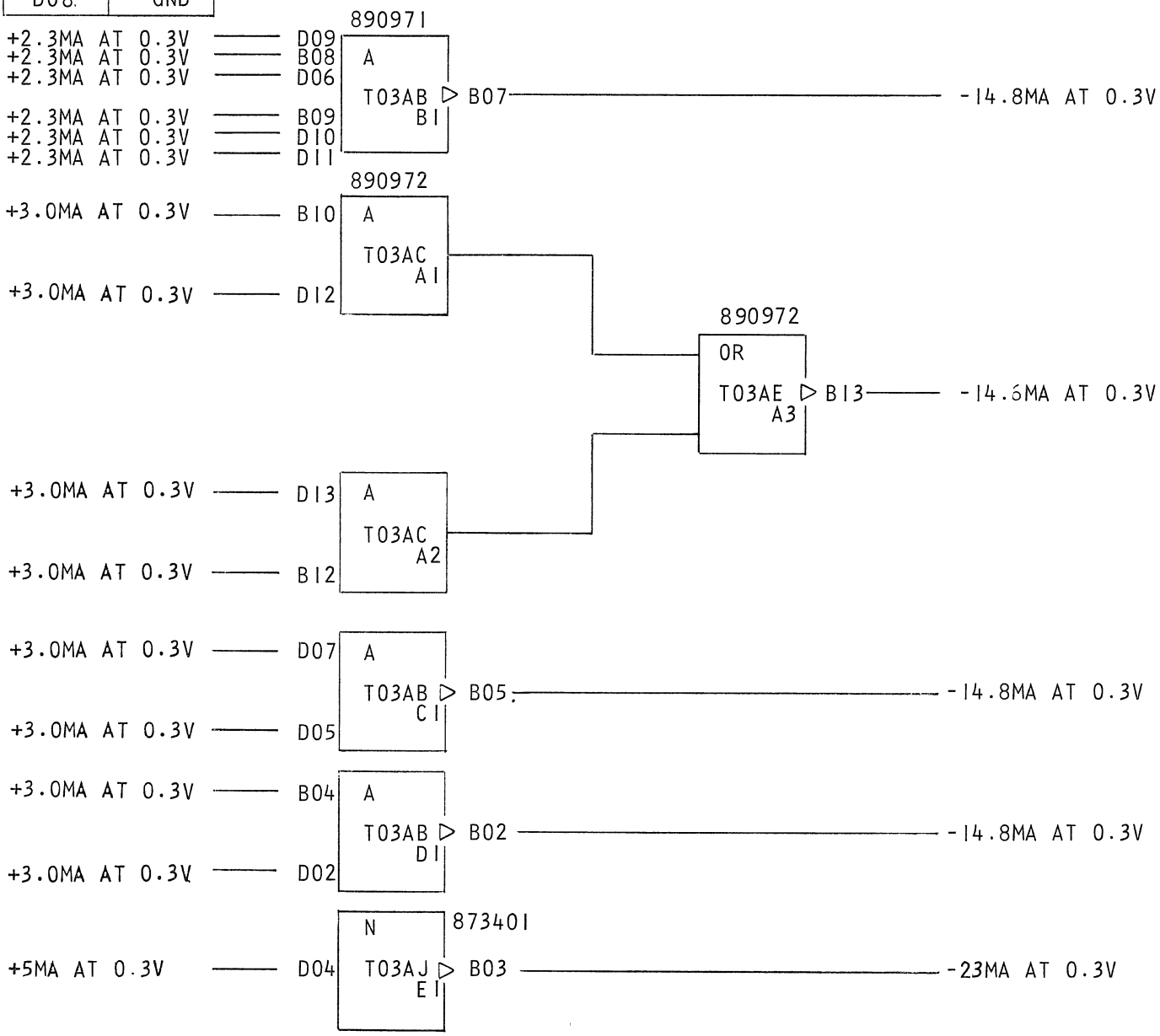
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2-2W AI & 1-6W AI & 1-1W API & 1-2W,2W AOI

CATEGORY CODE

T03

P/N	5800197
EC	162666
SPECIAL RESTRICTED	
CARD SIZE	1-6



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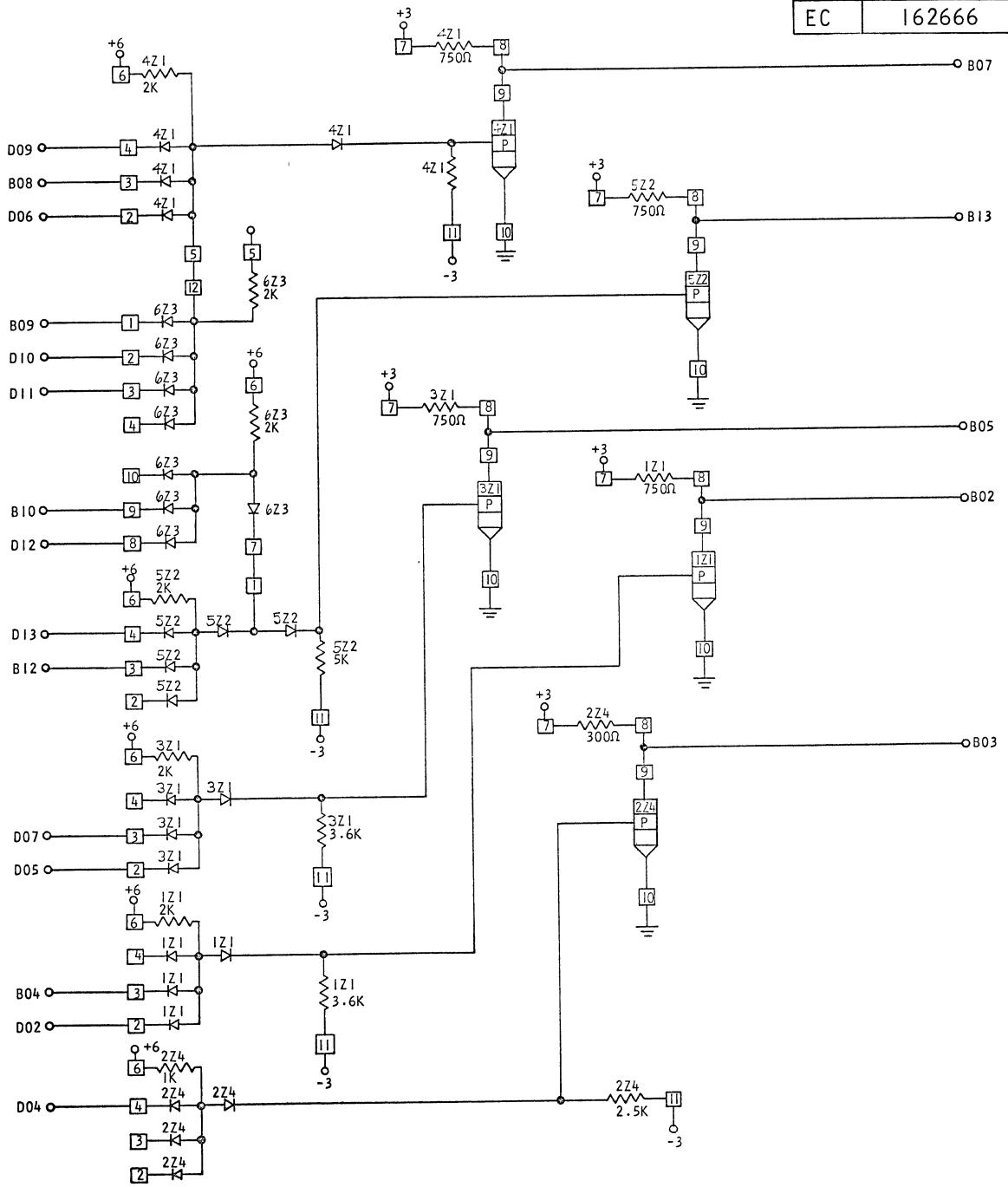
SLT LOGIC DIAGRAM & SCEMATIC - EQUIPMENT ENGINEERING
2-2W AI & 1-6W AI & 1-1W API & 1-2W,2W AOI

P/N	5800197
EC	162666



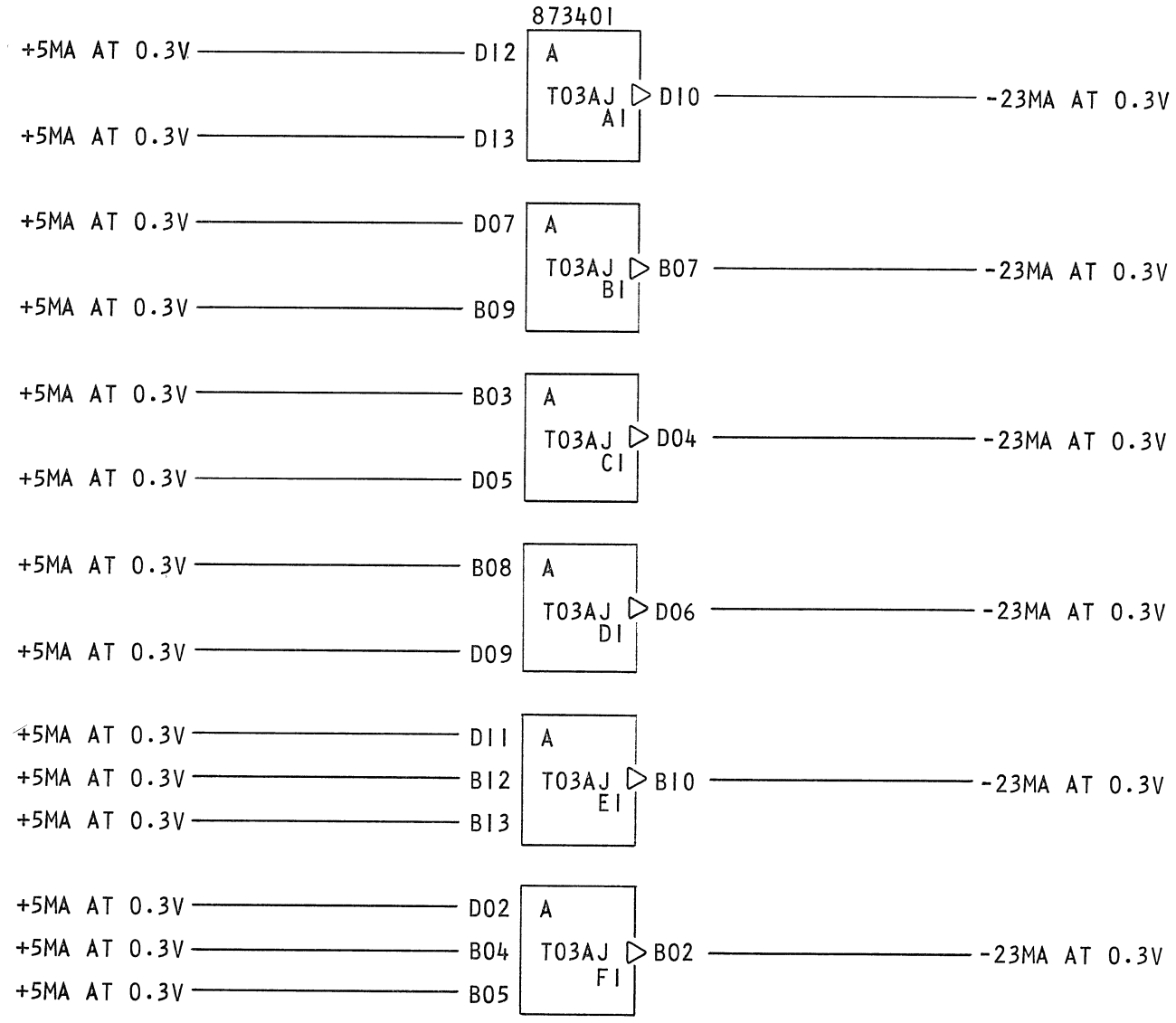
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2-3W API & 4-2W API

CATEGORY CODE

T03

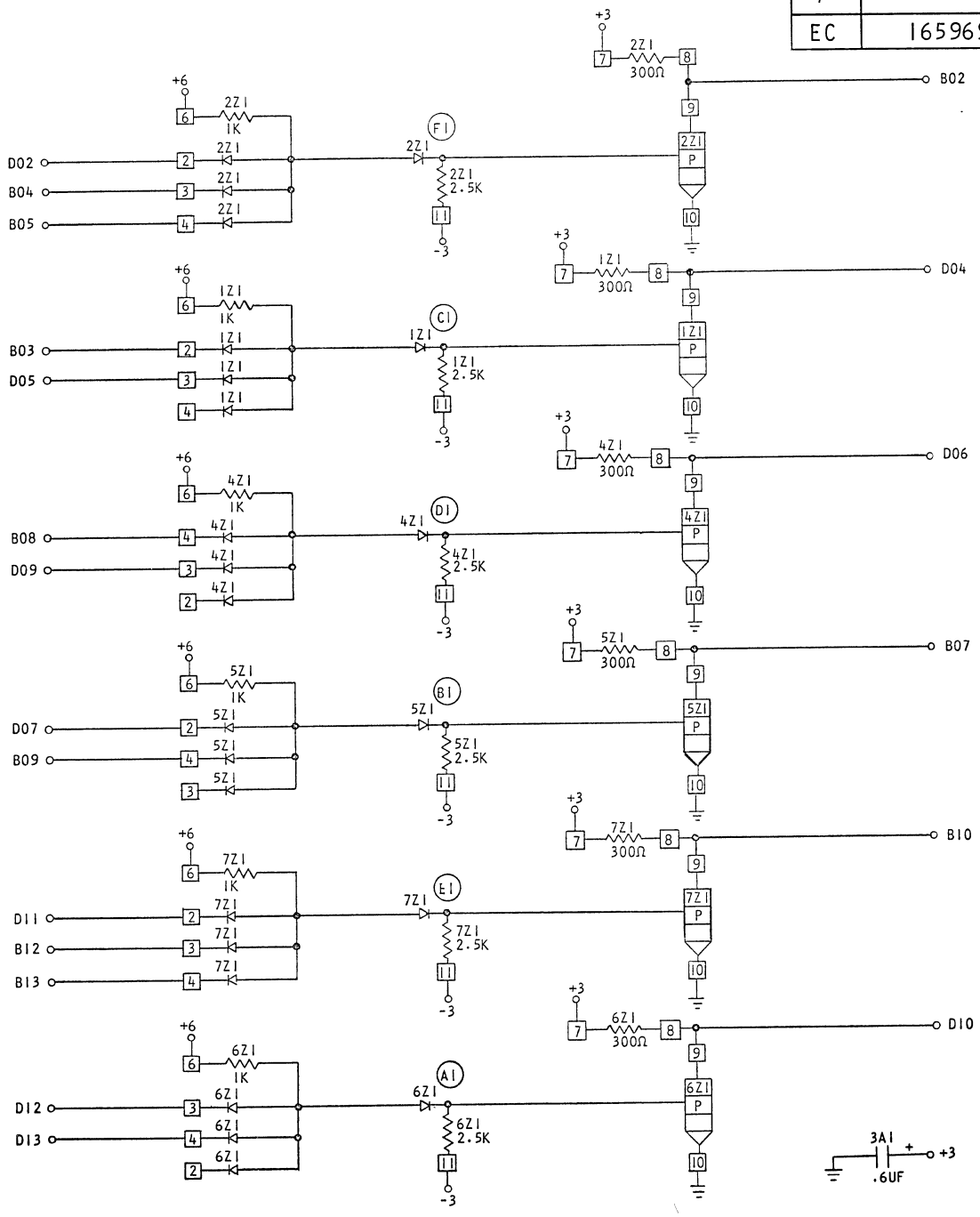
P/N	5800199
EC	165969
STANDARD RESTRICTED	
CARD SIZE	1-6



LMH Cat.	O-2860 Subject	218 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
-2-3W API & 4-2W API

P/N	5800199
EC	165969



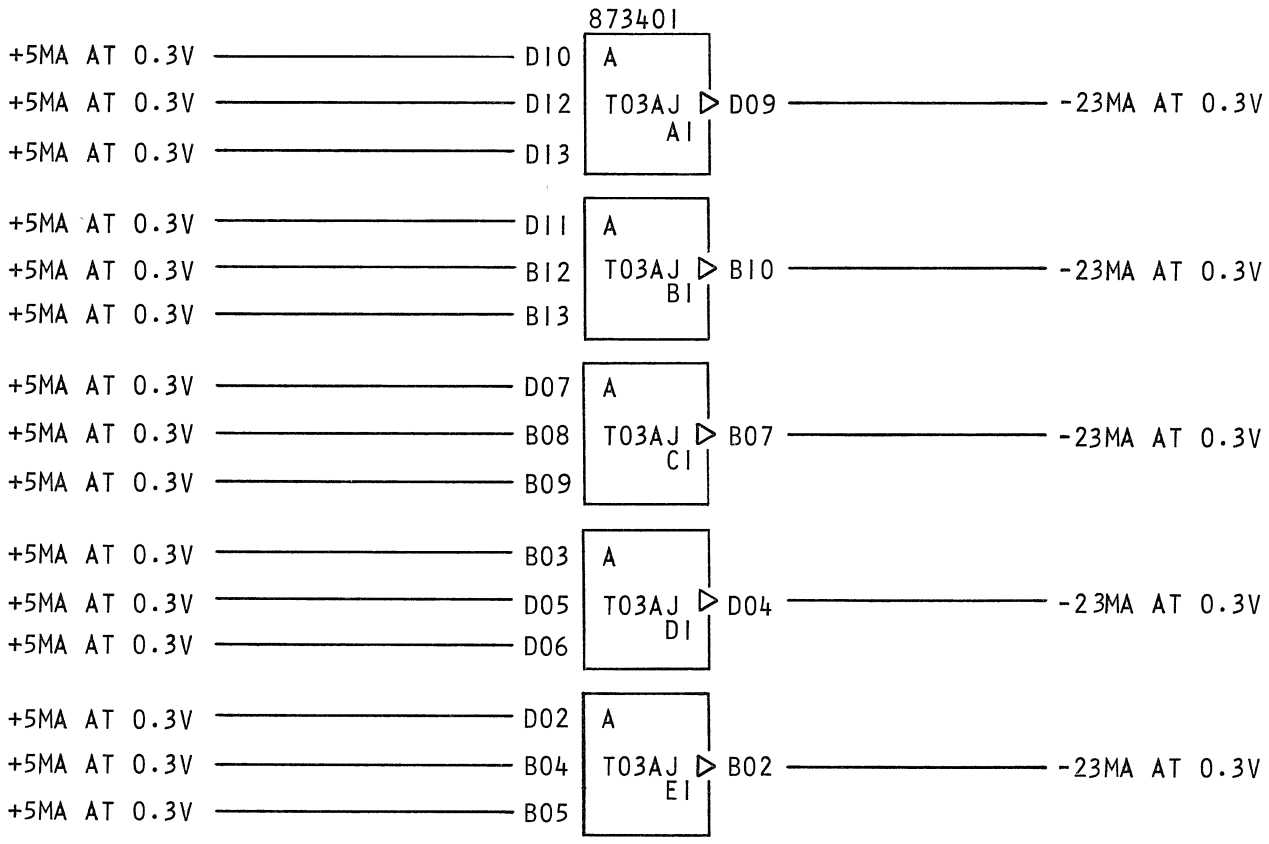
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

5-3W API

CATEGORY CODE

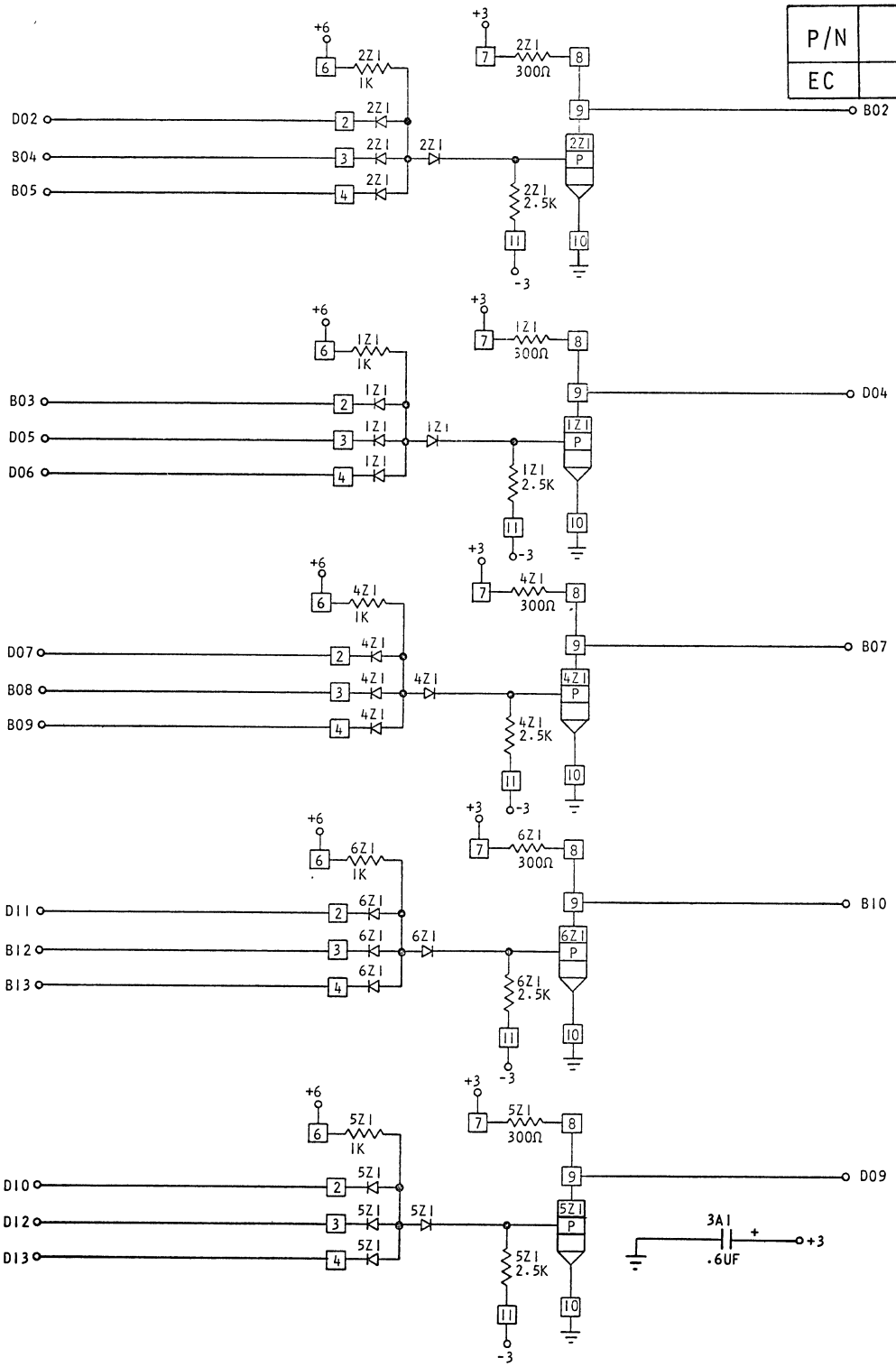
T03

P/N	5800200
EC	160018
STANDARD RESTRICTED	
CARD SIZE	1-6



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
5-3W API

P/N	5800200
EC	160018



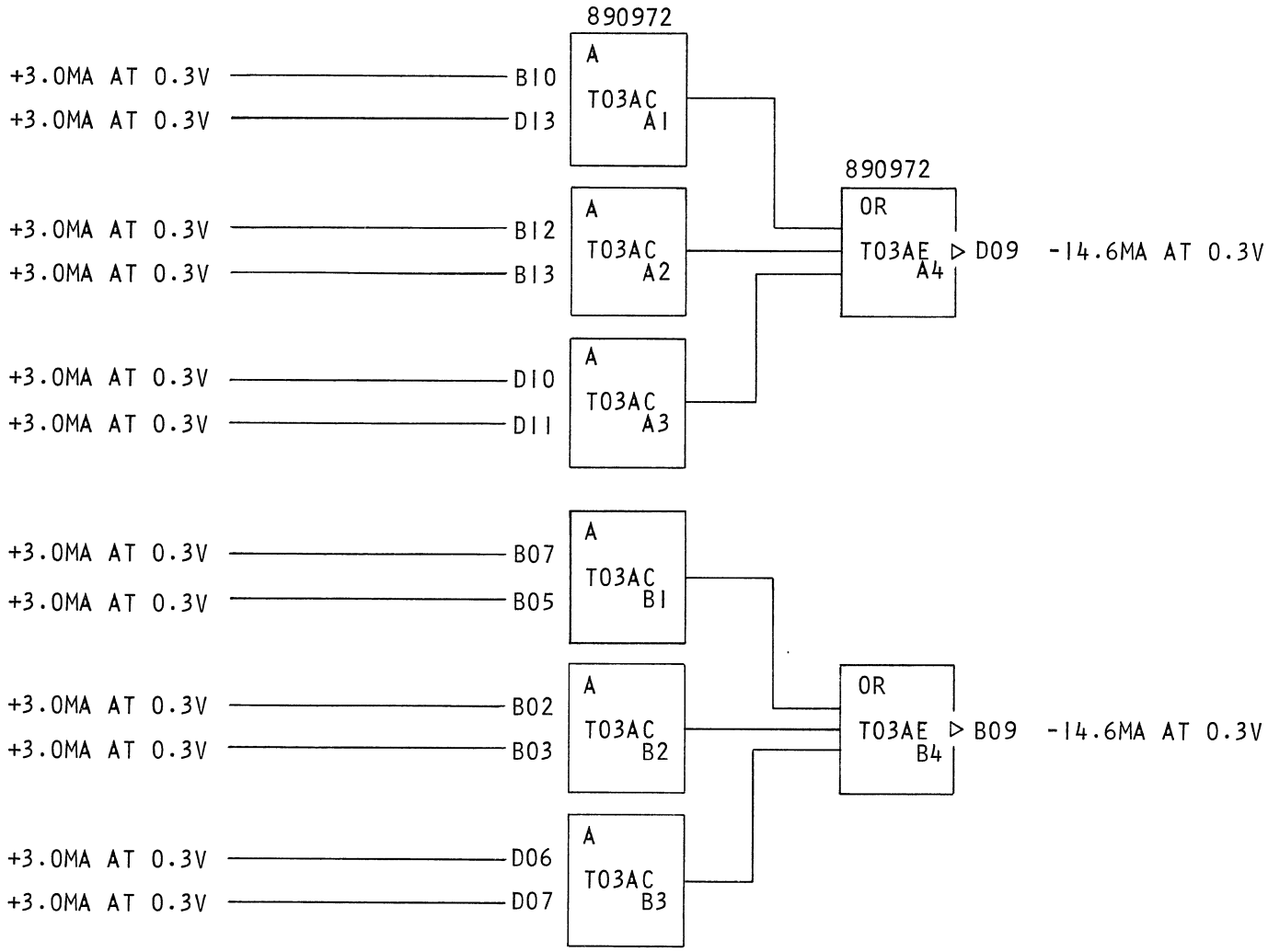
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2-2W AI & 2-2W,2W,2W AOI

CATEGORY CODE

T03

P/N	5800212
EC	160177
STANDARD RESTRICTED	
CARD SIZE	1-6

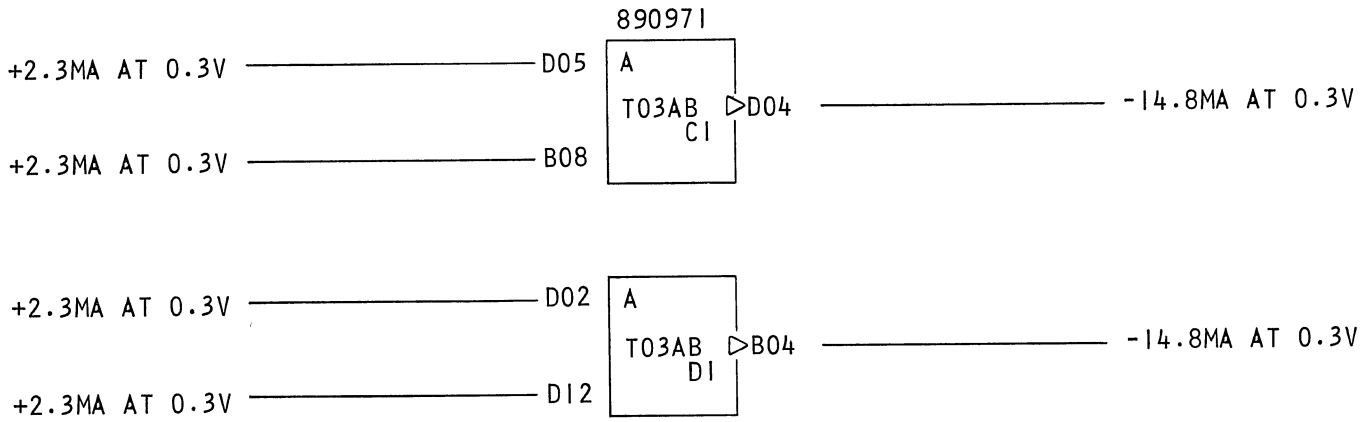


2-2W AI & 2-2W,2W,2W AOI

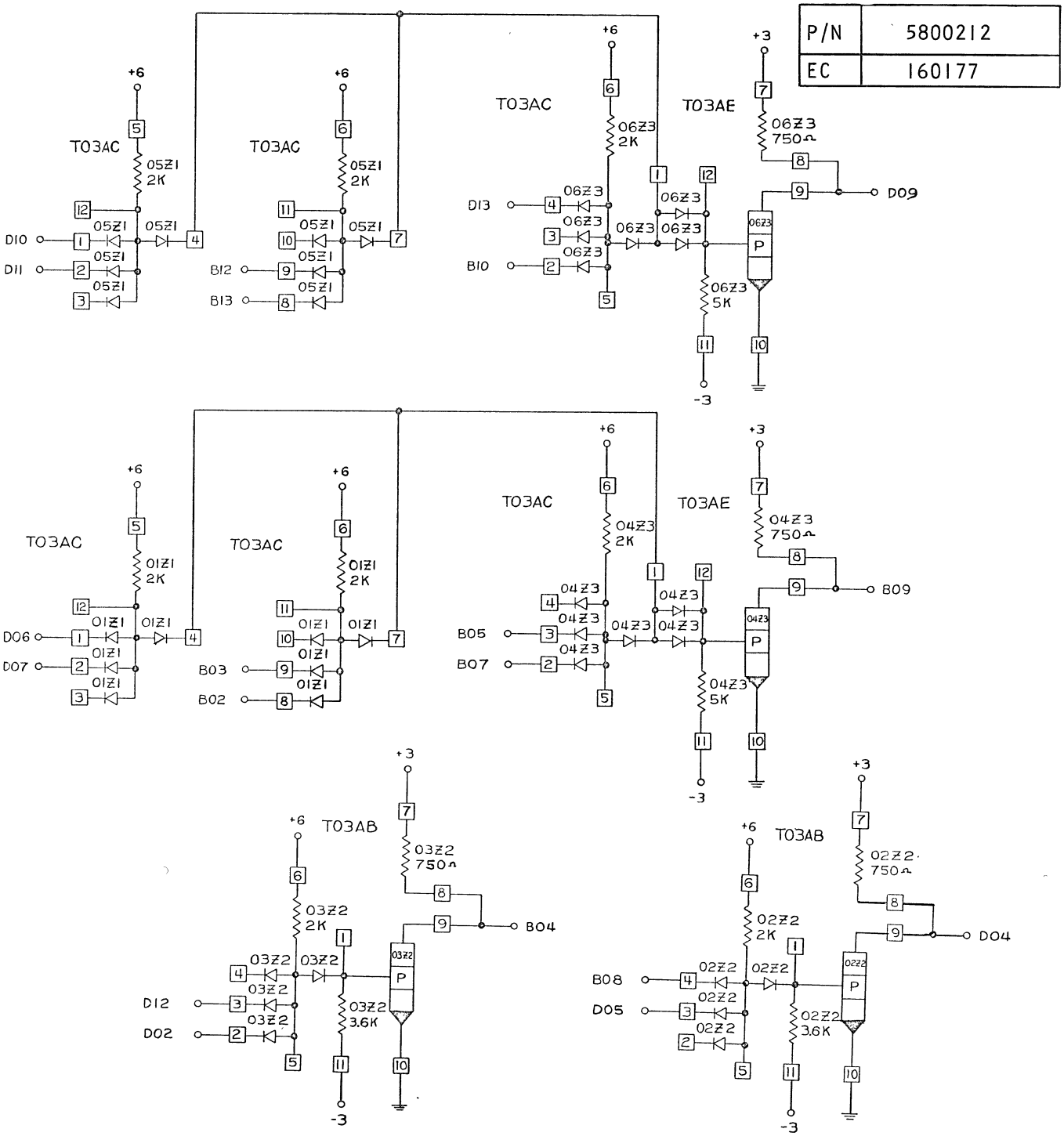
CATEGORY CODE

T03

P/N	5800212
EC	160177



P/N	5800212
EC	160177



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-5W AI W/L & 2-5W AI WO/L & 2-LD RES

LMH	0-2860	221
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

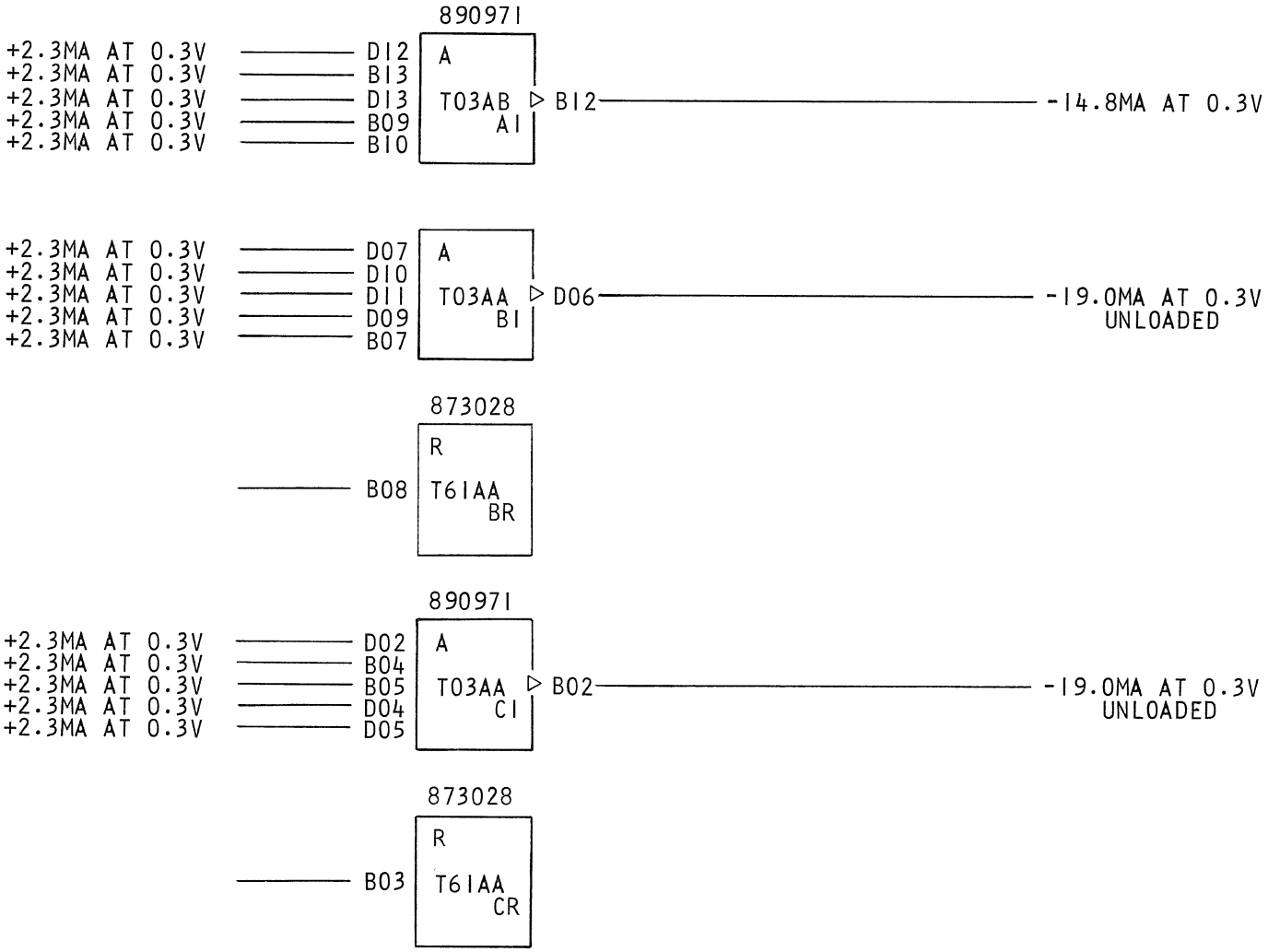
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1-5W AI W/L & 2-5W AI WO/L & 2-LD RES

CATEGORY CODE

T03

P/N	5800229
EC	160883
STANDARD RESTRICTED	
CARD SIZE	1-6



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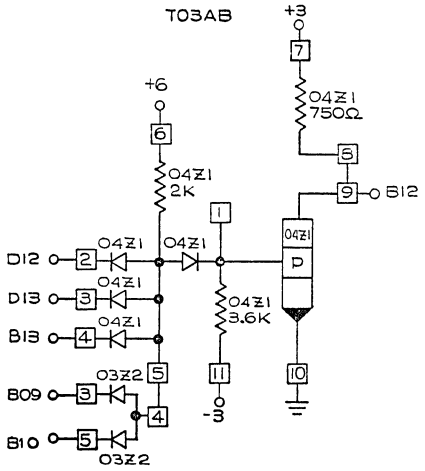
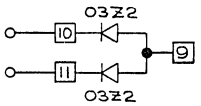
LMH Cat.	0-2860 Subject	221 Suffix

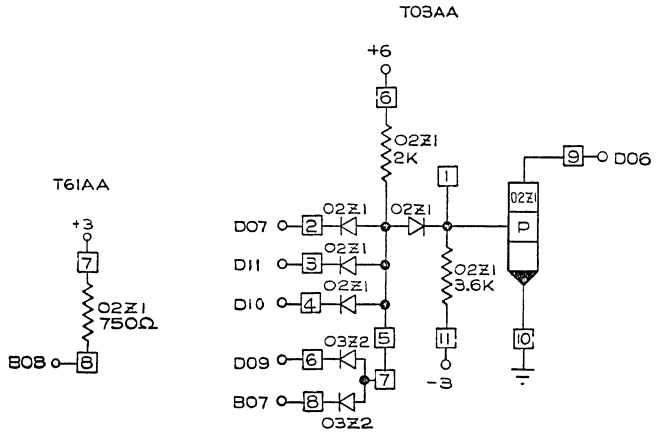
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-5W AI W/L & 2-5W AI WO/L & 2-LD RES

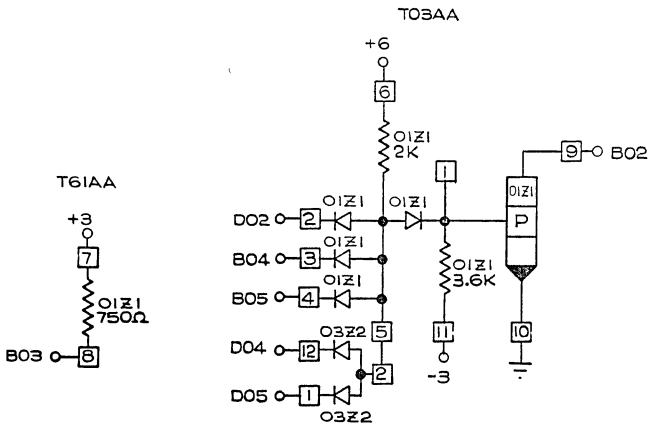
P/N	5800229
E C	160883





UNUSED COMPONENTS





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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-3W AI WO/L & 4-2W AI WO/L

LMH	O-2860	222
Cat.	Subject	Suffix

IBM Location
Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2-3W AI WO/L & 4-2W AI WO/L

CATEGORY CODE

T03

P/N	5800236
EC	168572 B
STANDARD RESTRICTED	
CARD SIZE	1-6

890971

+2.3MA AT 0.3V — D12
+2.3MA AT 0.3V — D13
A
T03AA AI ▷ D10 — -19.0MA AT 0.3V UNLOADED

+2.3MA AT 0.3V — D07
+2.3MA AT 0.3V — B09
A
T03AA BI ▷ B07 — -19.0MA AT 0.3V UNLOADED

+2.3MA AT 0.3V — B03
+2.3MA AT 0.3V — D05
A
T03AA CI ▷ D04 — -19.0MA AT 0.3V UNLOADED

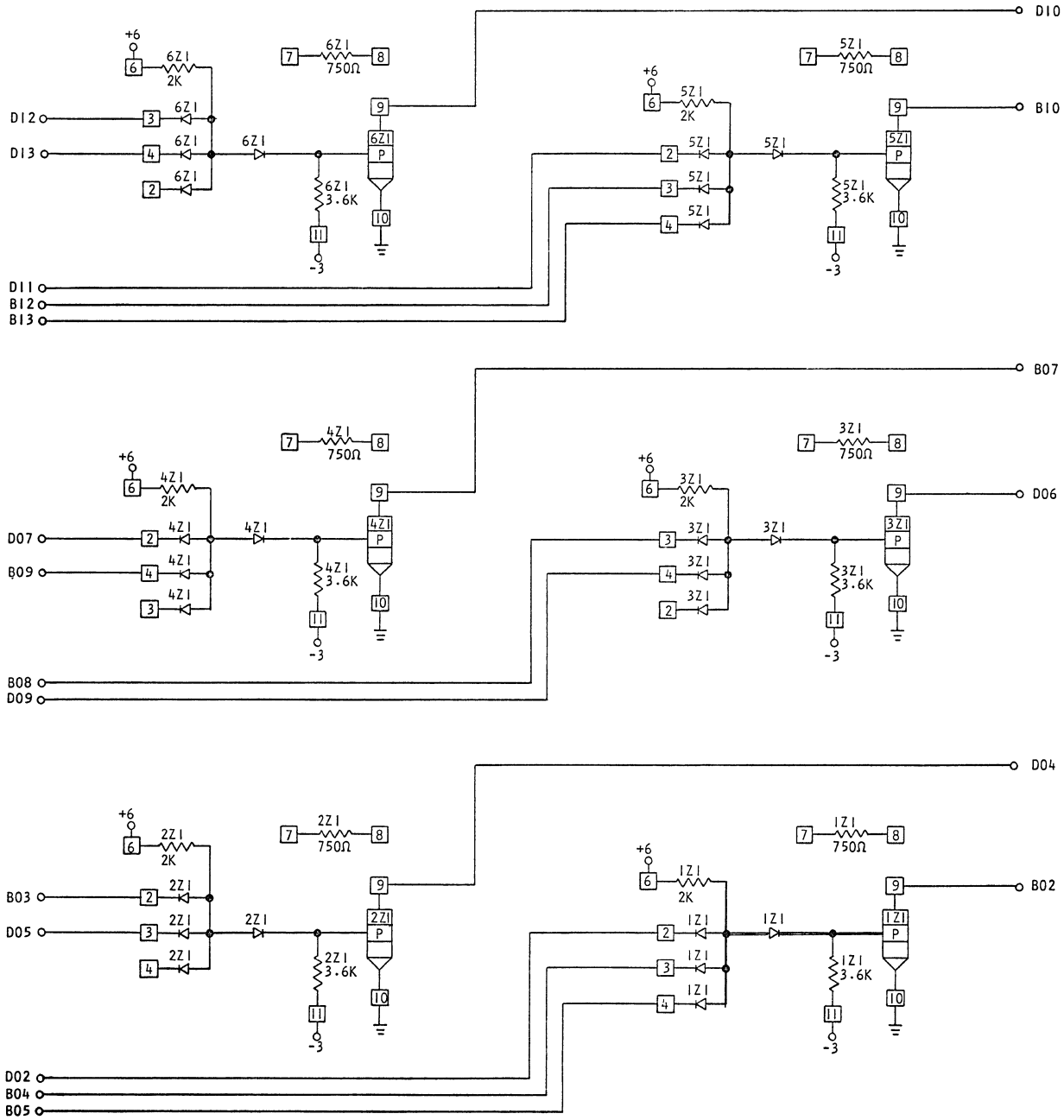
+2.3MA AT 0.3V — B08
+2.3MA AT 0.3V — D09
A
T03AA DI ▷ D06 — -19.0MA AT 0.3V UNLOADED

+2.3MA AT 0.3V — D11
+2.3MA AT 0.3V — B12
+2.3MA AT 0.3V — B13
A
T03AA EI ▷ B10 — -19.0MA AT 0.3V UNLOADED

+2.3MA AT 0.3V — D02
+2.3MA AT 0.3V — B04
+2.3MA AT 0.3V — B05
A
T03AA FI ▷ B02 — -19.0MA AT 0.3V UNLOADED

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-3W AI W0/L & 4-2W AI W0/L

P/N	5800236
EC	168572 B



IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

5-3W AI WO/L

CATEGORY CODE

T03

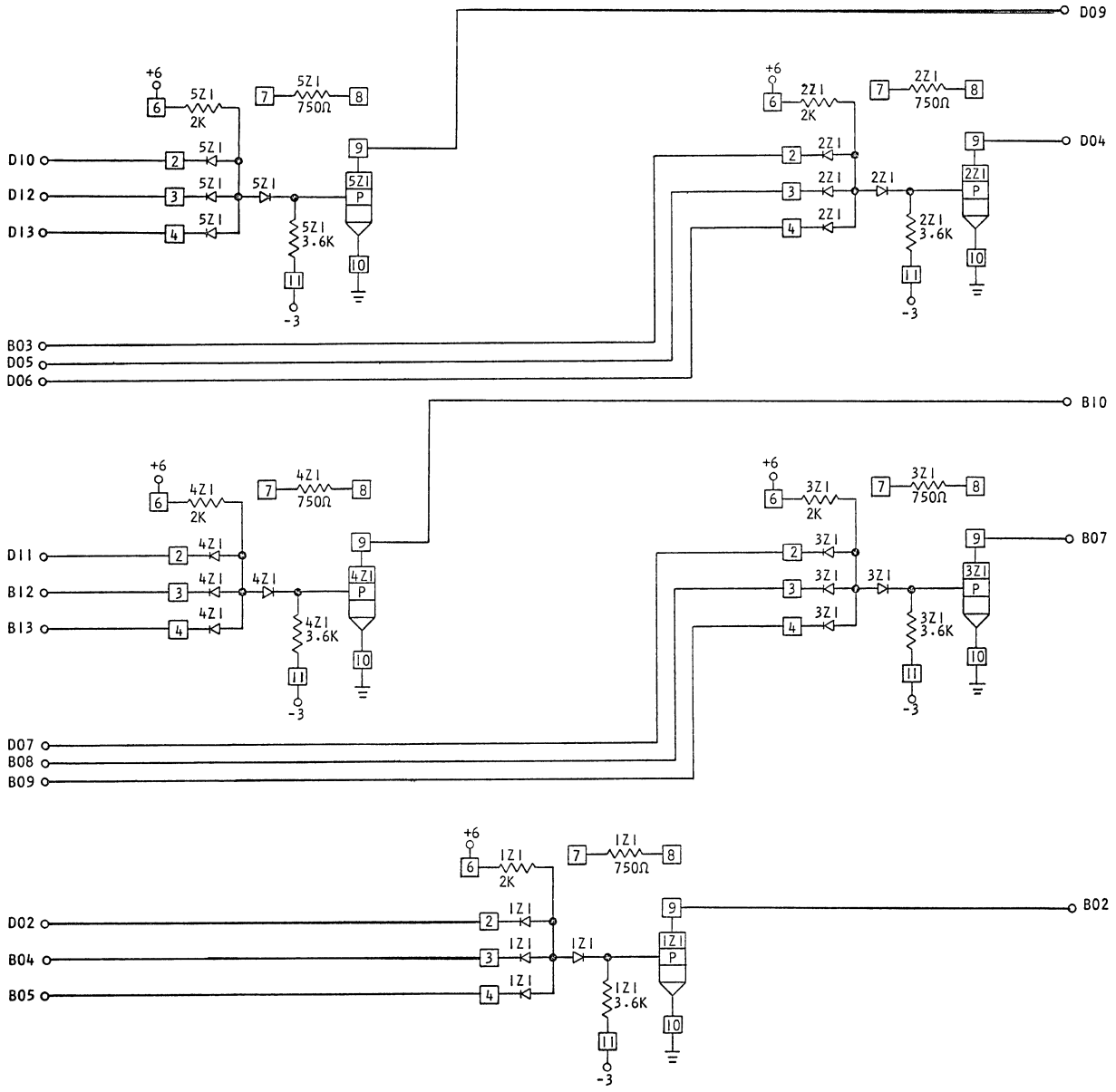
P/N	5800238
EC	162005
STANDARD RESTRICTED	
CARD SIZE	1-6

890971

+2.3MA AT 0.3V	D10	A T03AA AI	D09	-19.0MA AT 0.3V UNLOADED
+2.3MA AT 0.3V	D12			
+2.3MA AT 0.3V	D13			
+2.3MA AT 0.3V	B03	A T03AA BI	D04	-19.0MA AT 0.3V UNLOADED
+2.3MA AT 0.3V	D05			
+2.3MA AT 0.3V	D06			
+2.3MA AT 0.3V	D11	A T03AA CI	B10	-19.0MA AT 0.3V UNLOADED
+2.3MA AT 0.3V	B12			
+2.3MA AT 0.3V	B13			
+2.3MA AT 0.3V	D07	A T03AA DI	B07	-19.0MA AT 0.3V UNLOADED
+2.3MA AT 0.3V	B08			
+2.3MA AT 0.3V	B09			
+2.3MA AT 0.3V	D02	A T03AA EI	B02	-19.0MA AT 0.3V UNLOADED
+2.3MA AT 0.3V	B04			
+2.3MA AT 0.3V	B05			

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
5-3W AI W0/L

P/N	5800238
EC	162005



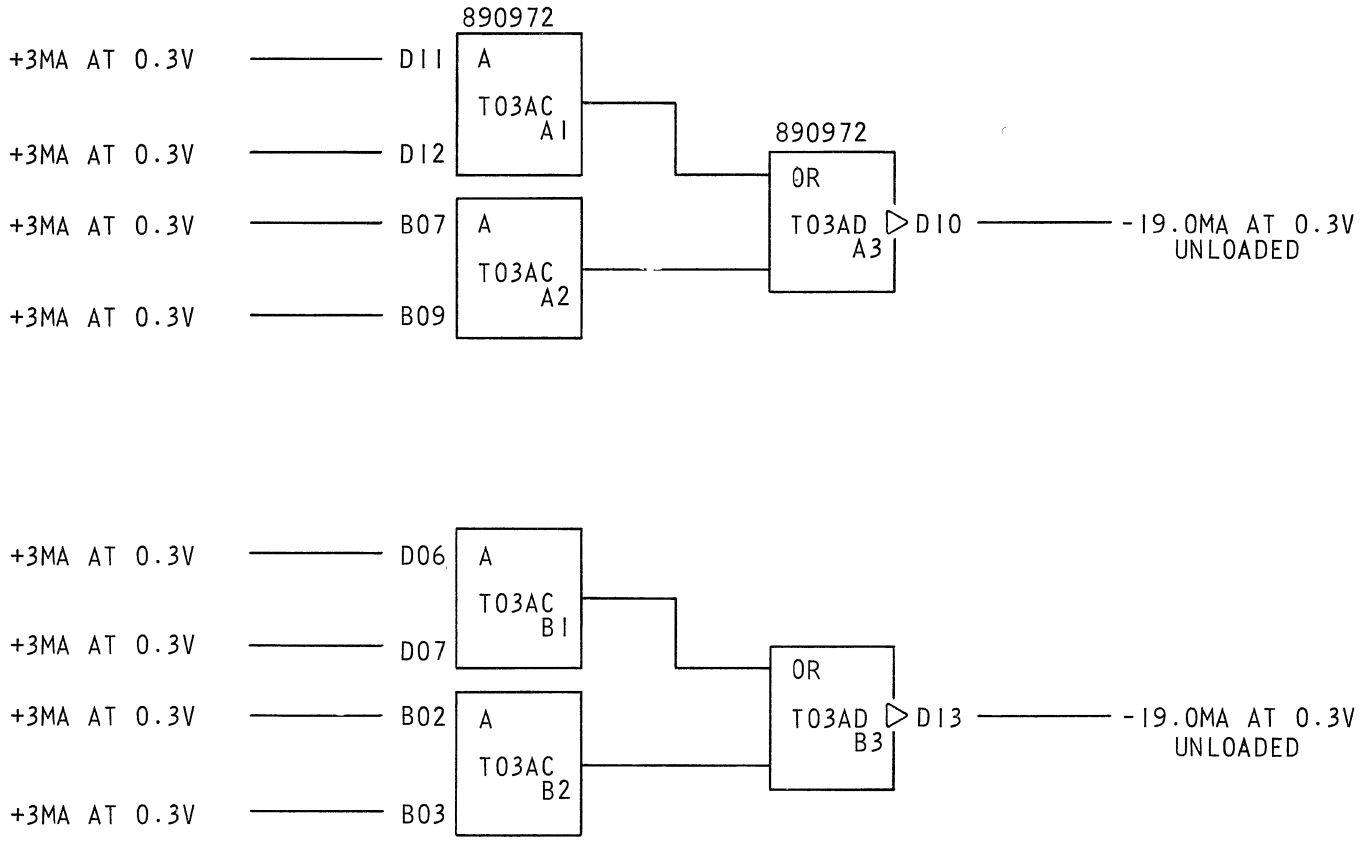
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D08	GND

4-2W,2W AOI W0/L

CATEGORY CODE

T03

P/N	5800240
EC	164897A
SPECIAL RESTRICTED	
CARD SIZE	1-6

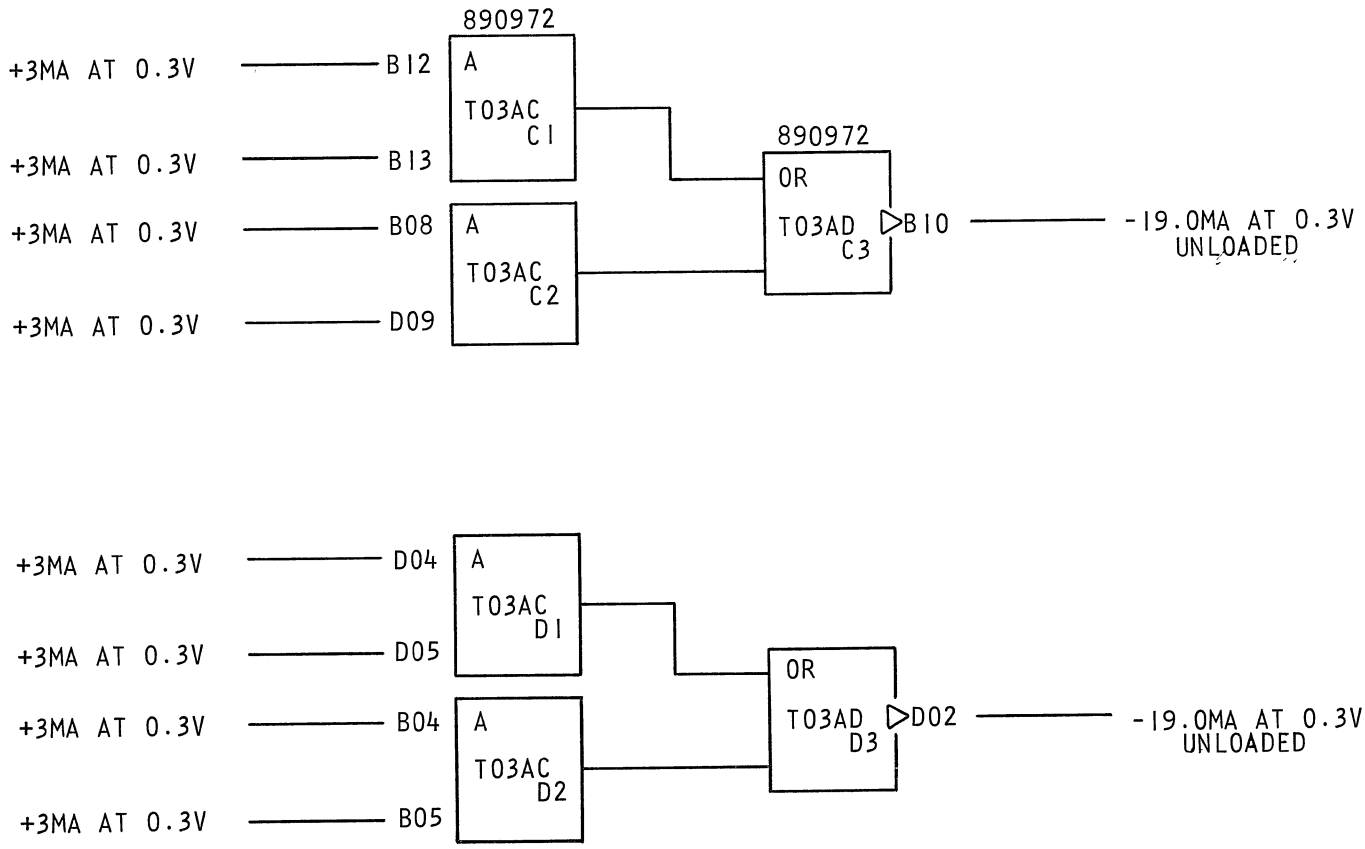


4-2W,2W AOI W0/L

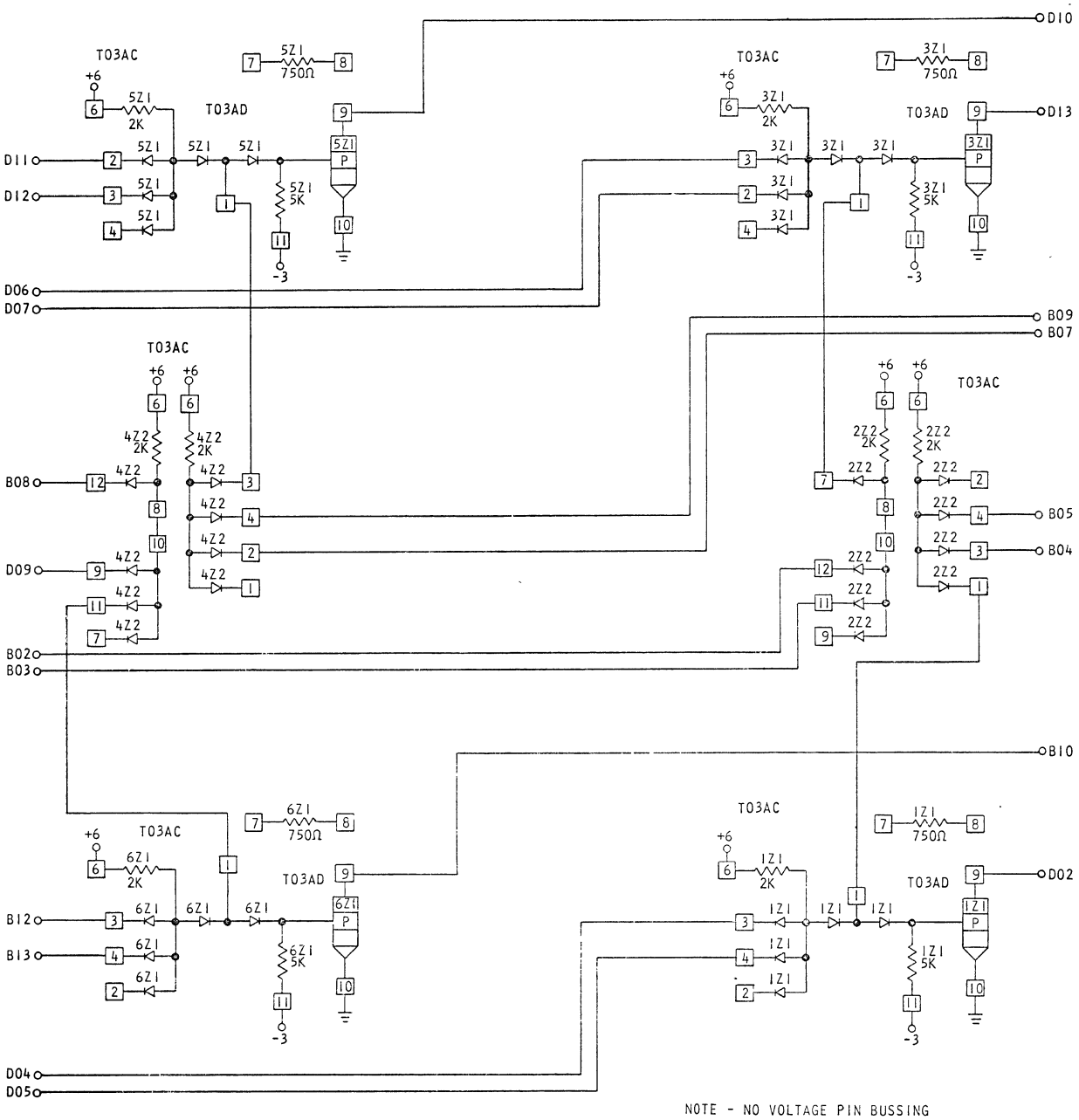
CATEGORY CODE

T03

P/N	5800240
EC	164897A



P/N	5800240
EC	164897A



NOTE - NO VOLTAGE PIN BUSSING

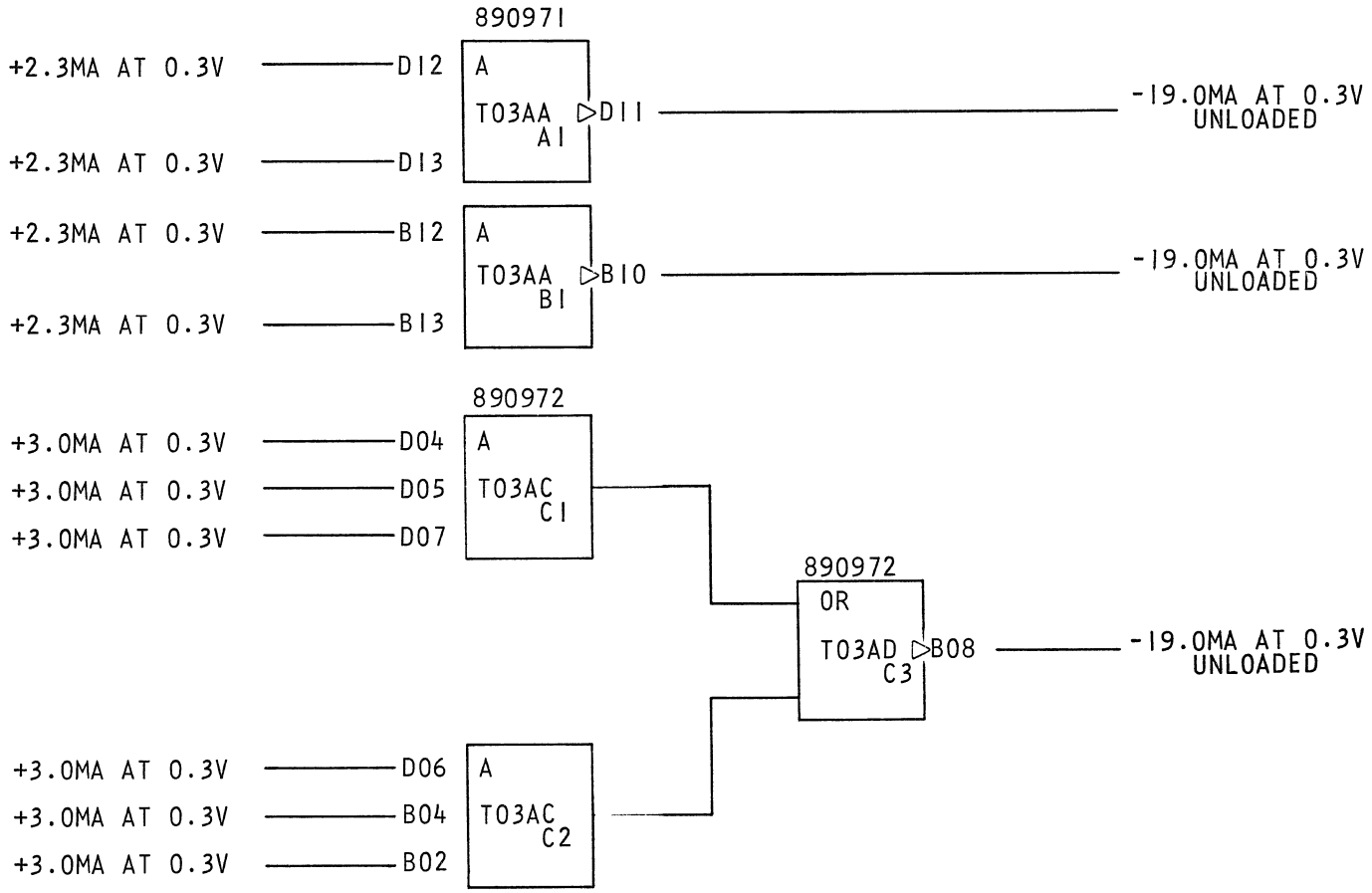
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D08	GND

2-3W,3W AOI & 2-2W AI WO/L

CATEGORY CODE

T03

P/N	5800241
EC	160023
STANDARD ACTIVE	
CARD SIZE	1-6

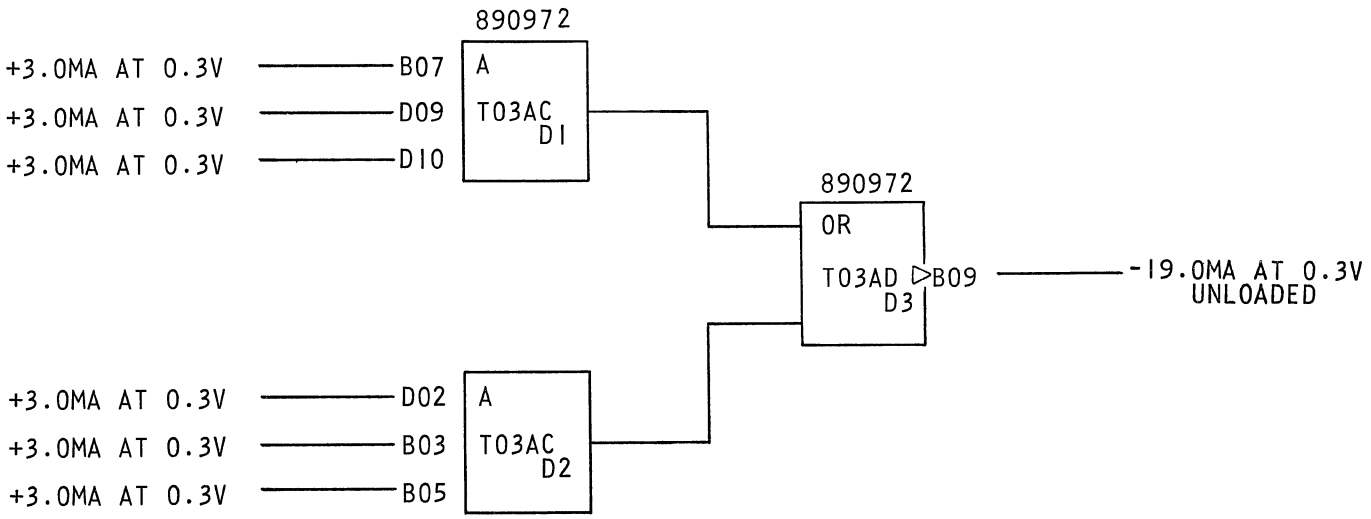


2-3W,3W AOI & 2-2W AI W0/L

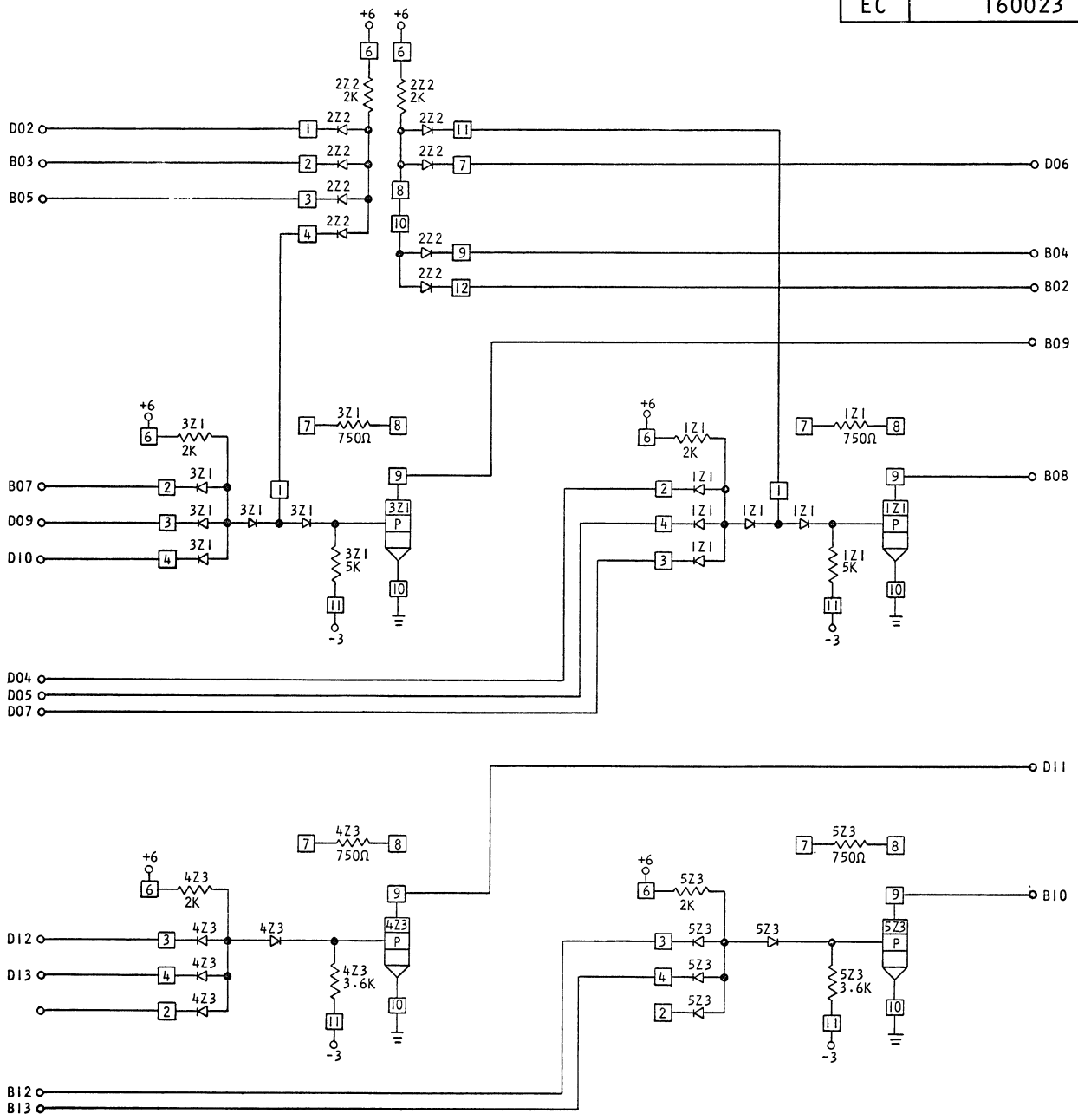
CATEGORY CODE

T03

P/N	5800241
EC	160023
STANDARD ACTIVE	
CARD SIZE	1-6



P/N	5800241
EC	160023



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-5W AI W0/L & 1-7W AI W0/L

LMH	0-2860	226
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D08	GND

2-5W AI W0/L & 1-7W AI W0/L

CATEGORY CODE

T03

P/N	5800242
EC	165334 A
STANDARD RESTRICTED	
CARD SIZE	1-6

890971

+2.3MA AT 0.3V — D02
+2.3MA AT 0.3V — D04
+2.3MA AT 0.3V — D05
+2.3MA AT 0.3V — D06
+2.3MA AT 0.3V — B03
+2.3MA AT 0.3V — B04
+2.3MA AT 0.3V — B05

A
T03AA AI ▷ B02 — -19.0MA AT 0.3V UNLOADED

+2.3MA AT 0.3V — D09
+2.3MA AT 0.3V — B10
+2.3MA AT 0.3V — D07
+2.3MA AT 0.3V — B08
+2.3MA AT 0.3V — B09

A
T03AA BI ▷ B07 — -19.0MA AT 0.3V UNLOADED

+2.3MA AT 0.3V — D11
+2.3MA AT 0.3V — B12
+2.3MA AT 0.3V — B13
+2.3MA AT 0.3V — D13
+2.3MA AT 0.3V — D10

A
T03AA CI ▷ D12 — -19.0MA AT 0.3V UNLOADED

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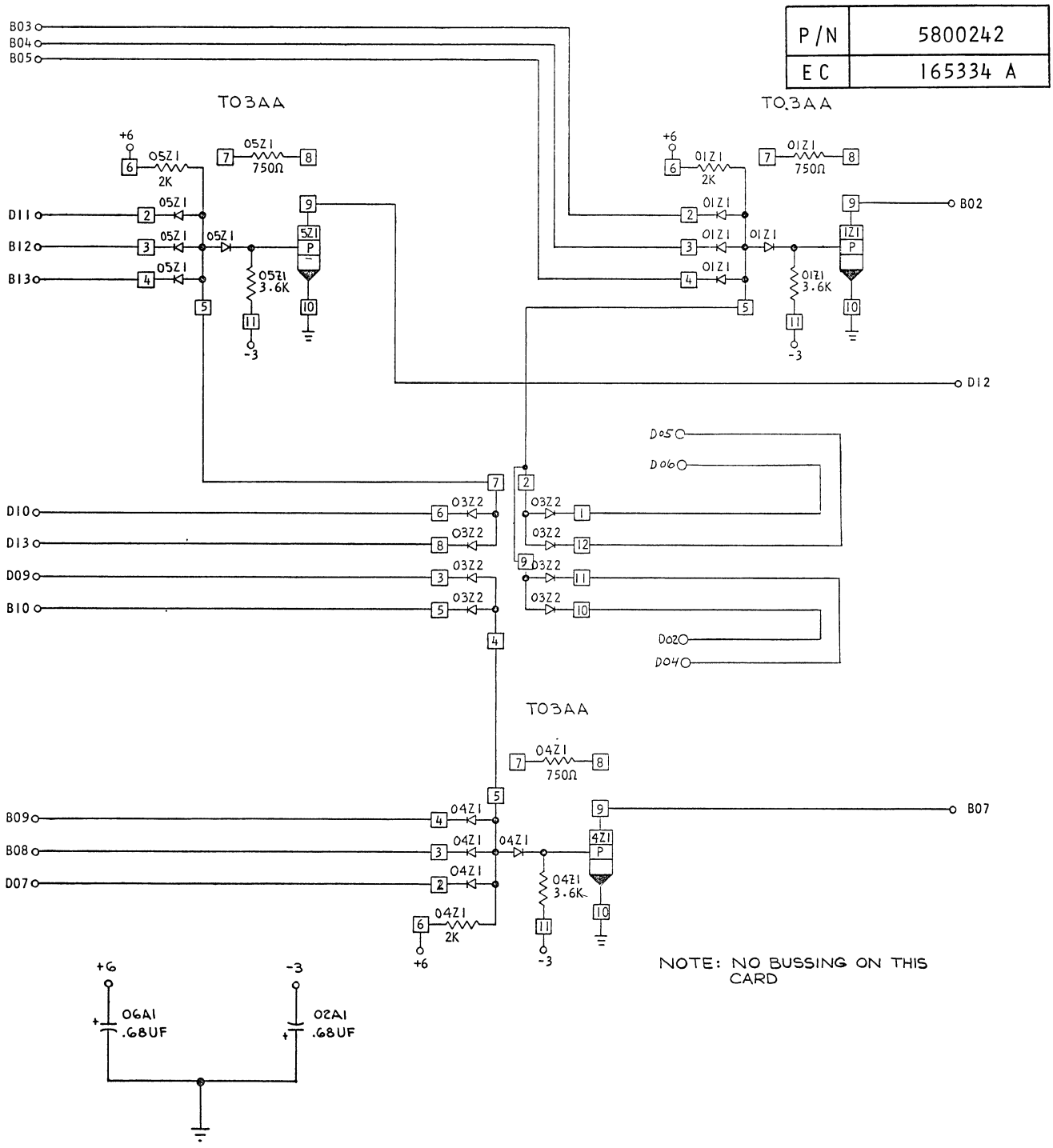
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-5W AI W0/L & 1-7W AI W0/L

P/N	5800242
EC	165334 A



IBM

Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

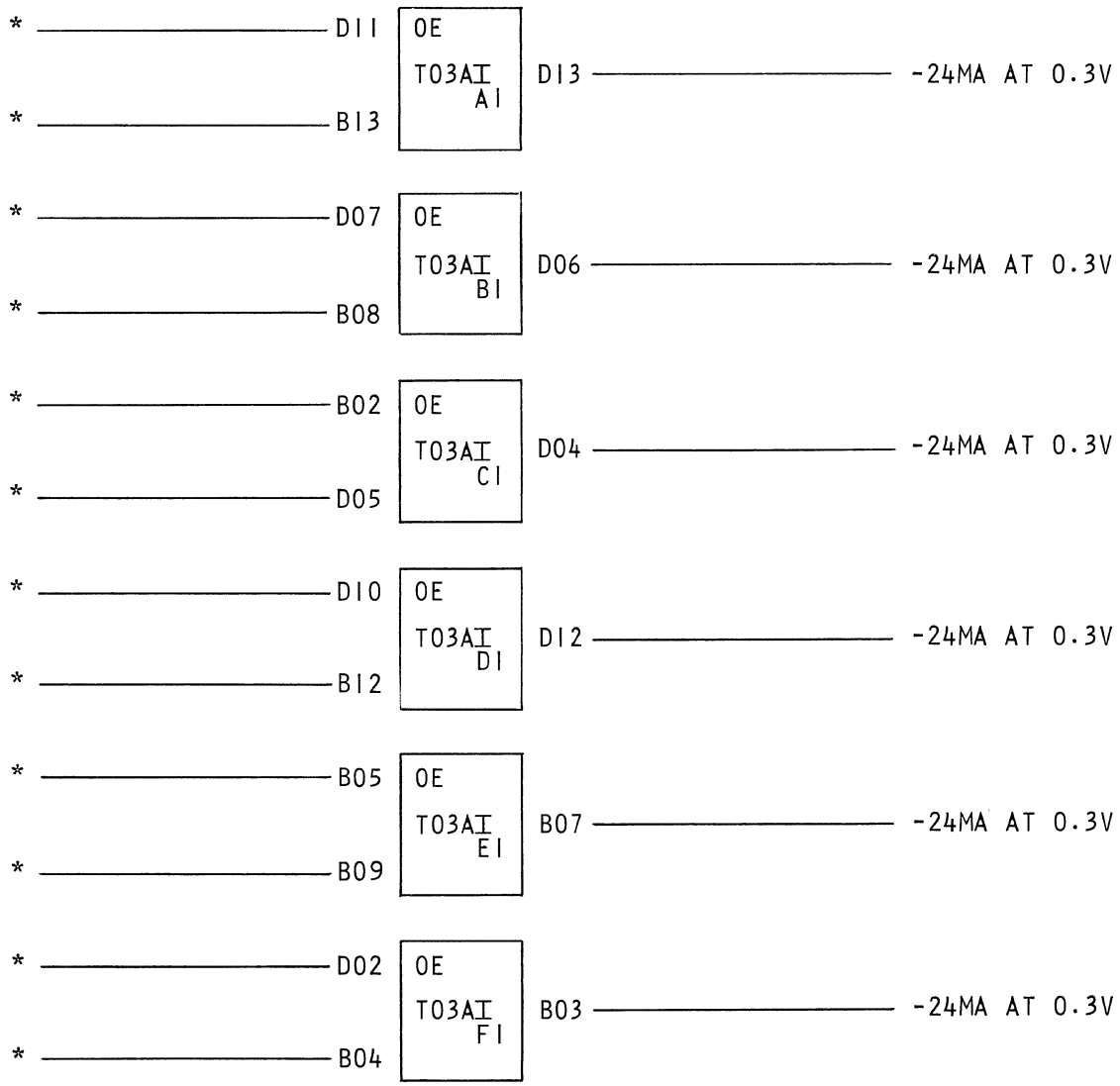
6-XOR

CATEGORY CODE

T03

P/N	5800243
EC	160223
STANDARD RESTRICTED	
CARD SIZE	1-6

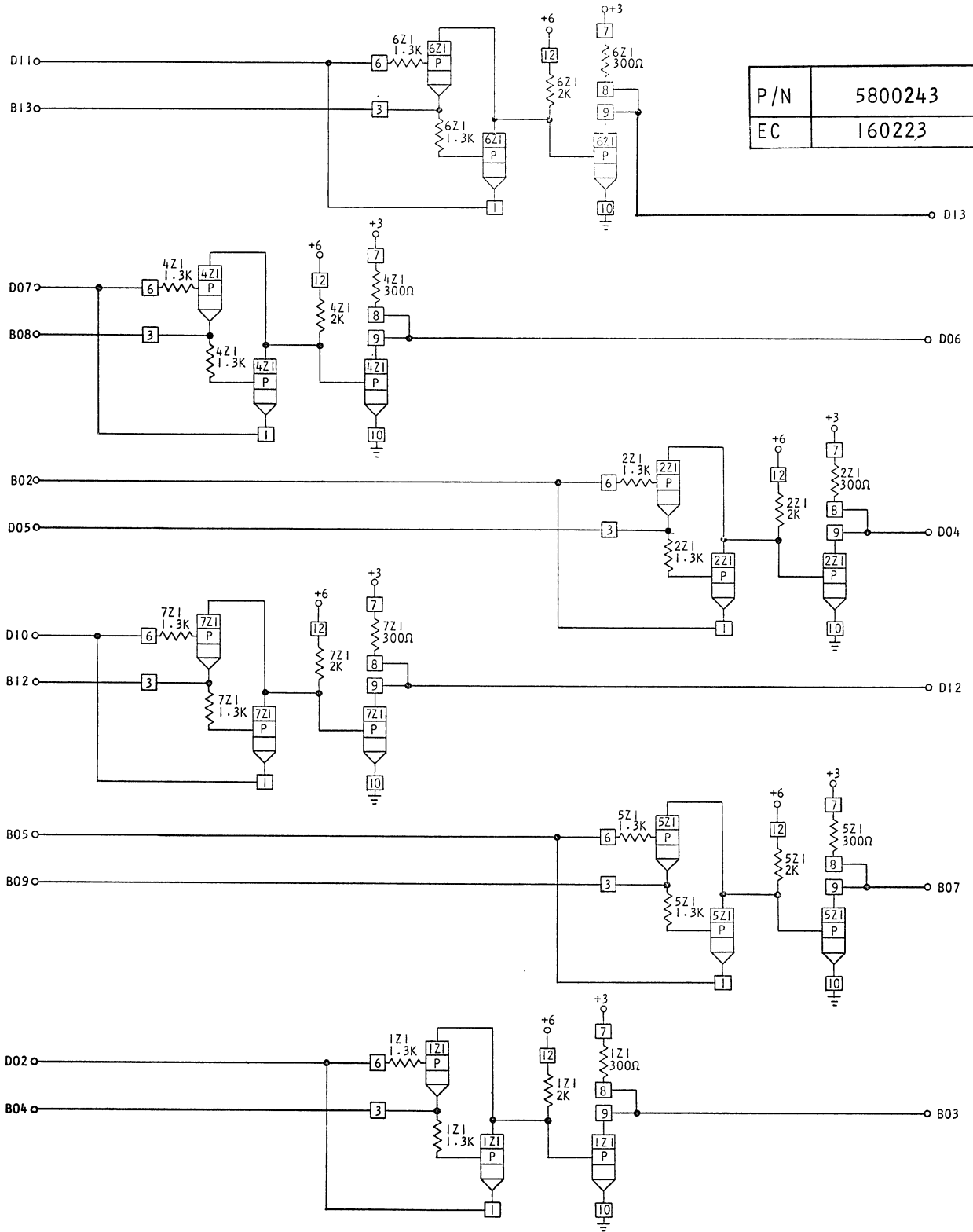
873400



* SPECIAL DRIVE RULES SEE CIRCUIT SPECIFICATION 873400

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6-XOR

P/N	5800243
EC	160223



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-7W AI WO/L & 1-3W AI WO/L

LMH	0-2860	228
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

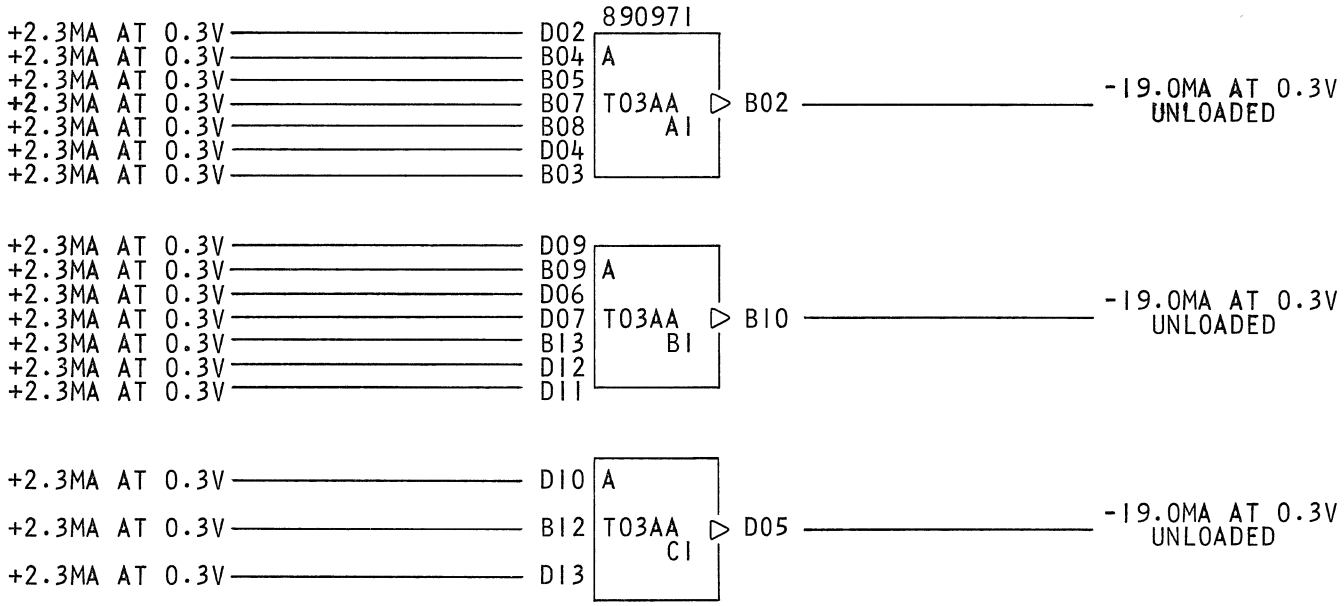
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

2-7W AI WO/L & 1-3W AI WO/L

CATEGORY CODE

T03

P/N	5800244
EC	163450A
STANDARD RESTRICTED	
CARD SIZE	1-6



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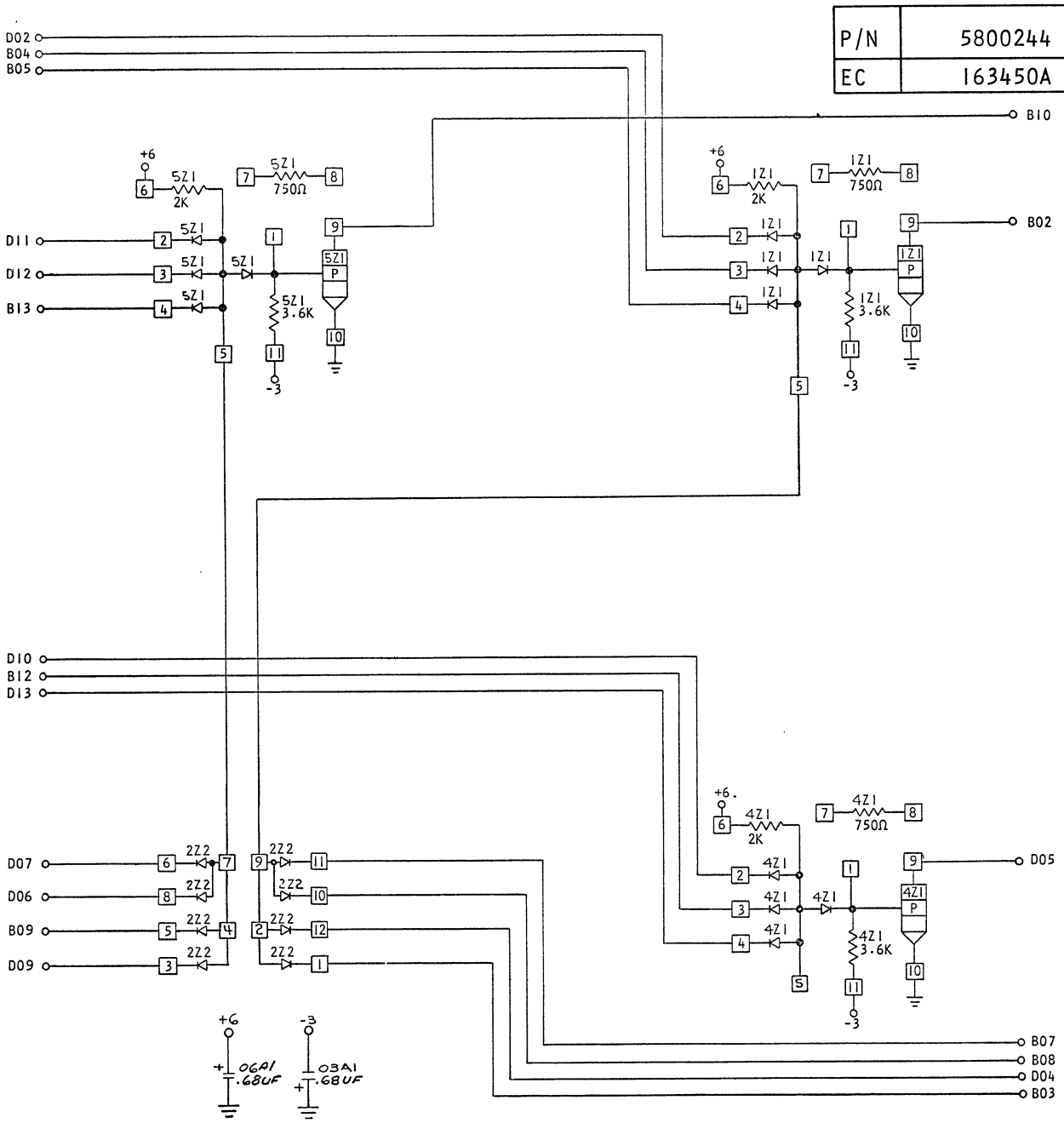
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-7W AI W0/L & 1-3W AI W0/L

P/N	5800244
EC	163450A



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POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D08	GND

1-11W AI WO/L & 2-3W AI WO/L

CATEGORY CODE

T03

P/N	5800245
EC	163201
STANDARD RESTRICTED	
CARD SIZE	1-6

890971

+2.3MA AT 0.3V — D12
+2.3MA AT 0.3V — B13
+2.3MA AT 0.3V — D09
+2.3MA AT 0.3V — B10
+2.3MA AT 0.3V — D13
+2.3MA AT 0.3V — B12
+2.3MA AT 0.3V — D11
+2.3MA AT 0.3V — D10
+2.3MA AT 0.3V — B07
+2.3MA AT 0.3V — B08
+2.3MA AT 0.3V — B09

A
T03AA AI ▷ D07 — -19.0MA AT 0.3V UNLOADED

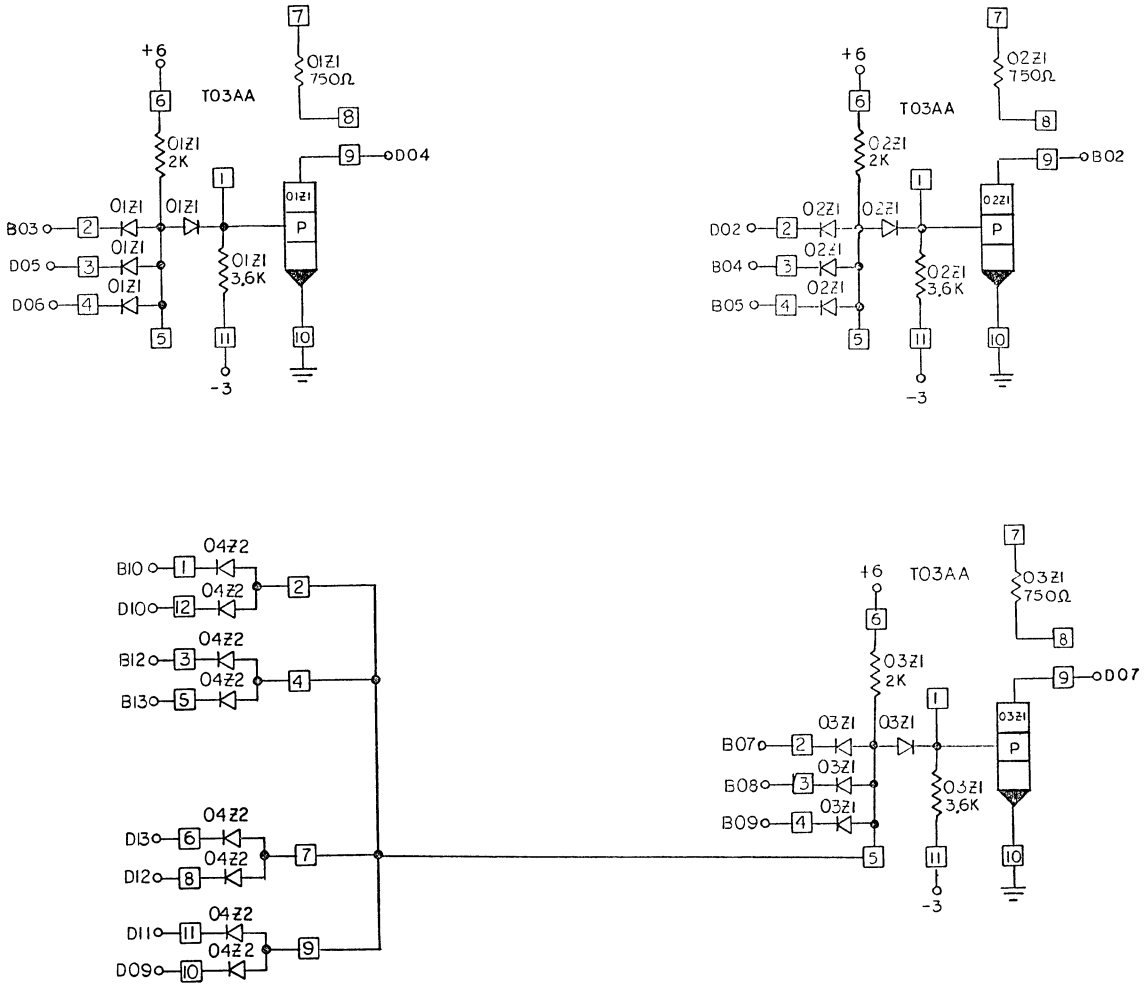
+2.3MA AT 0.3V — D02
+2.3MA AT 0.3V — B04
+2.3MA AT 0.3V — B05

A
T03AA BI ▷ B02 — -19.0MA AT 0.3V UNLOADED

+2.3MA AT 0.3V — B03
+2.3MA AT 0.3V — D05
+2.3MA AT 0.3V — D06

A
T03AA CI ▷ D04 — -19.0MA AT 0.3V UNLOADED

P/N	5800245
EC	163201



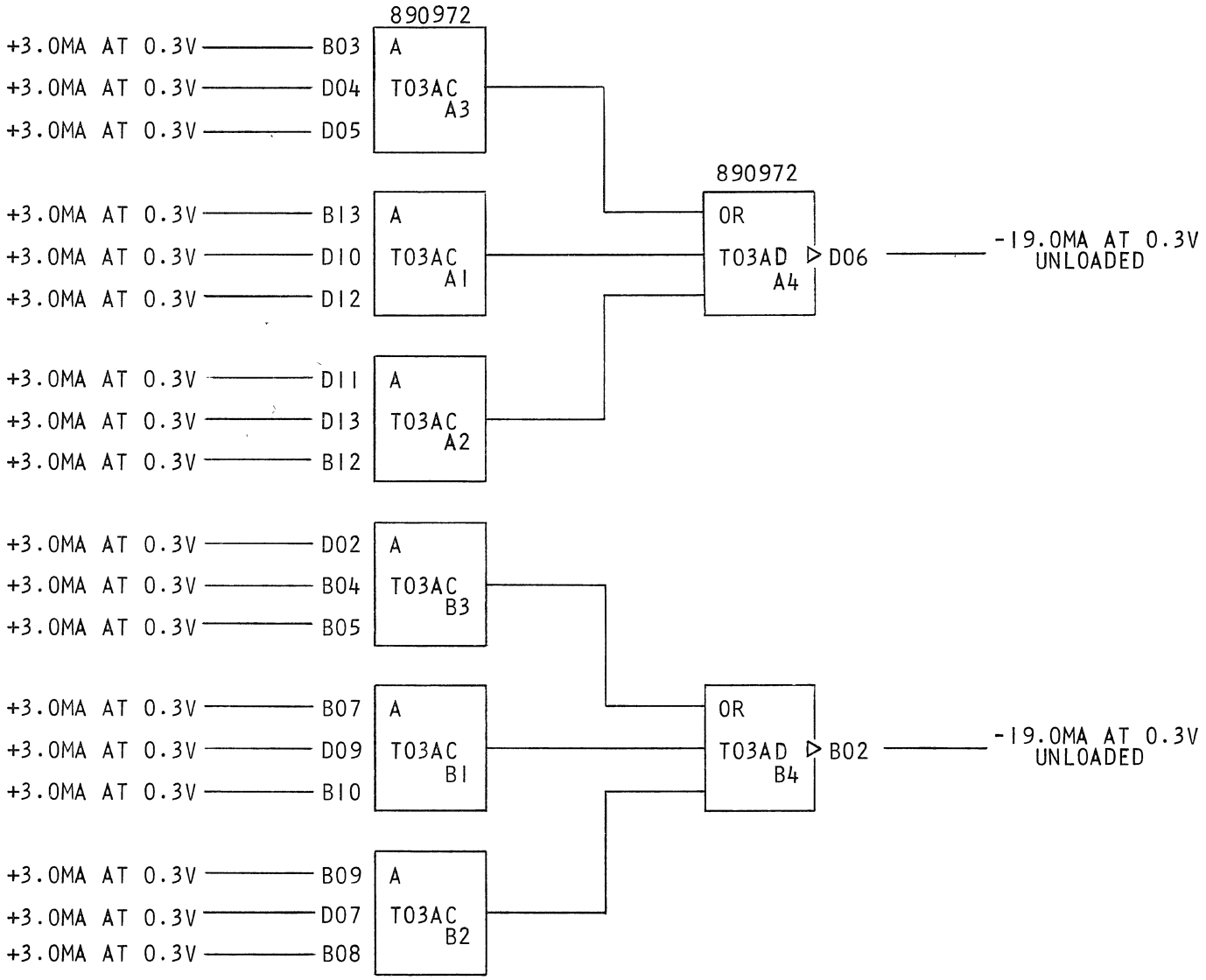
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

2-3W, 3W, 3W AOI WO/L

CATEGORY CODE

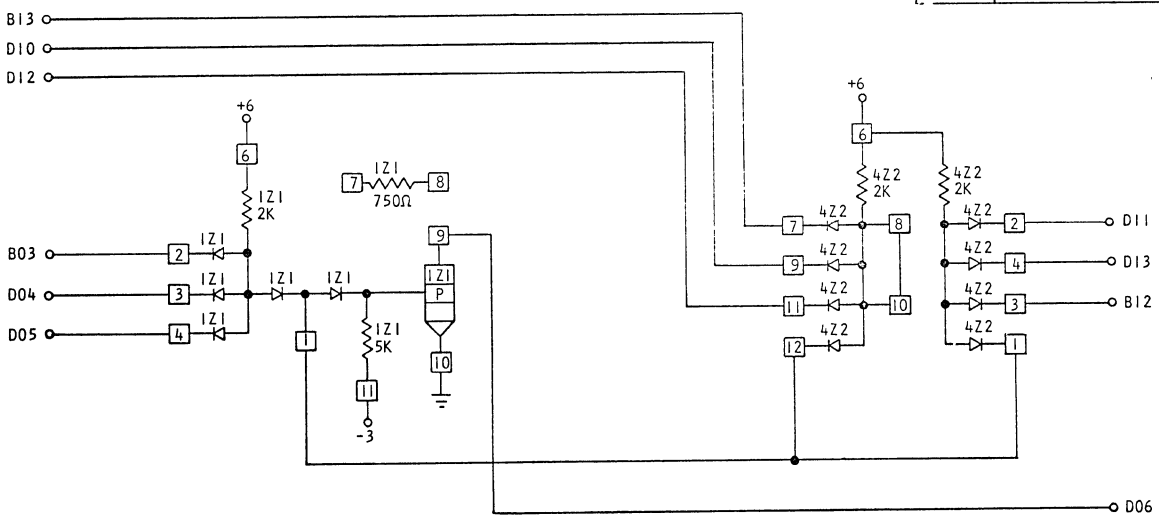
T03

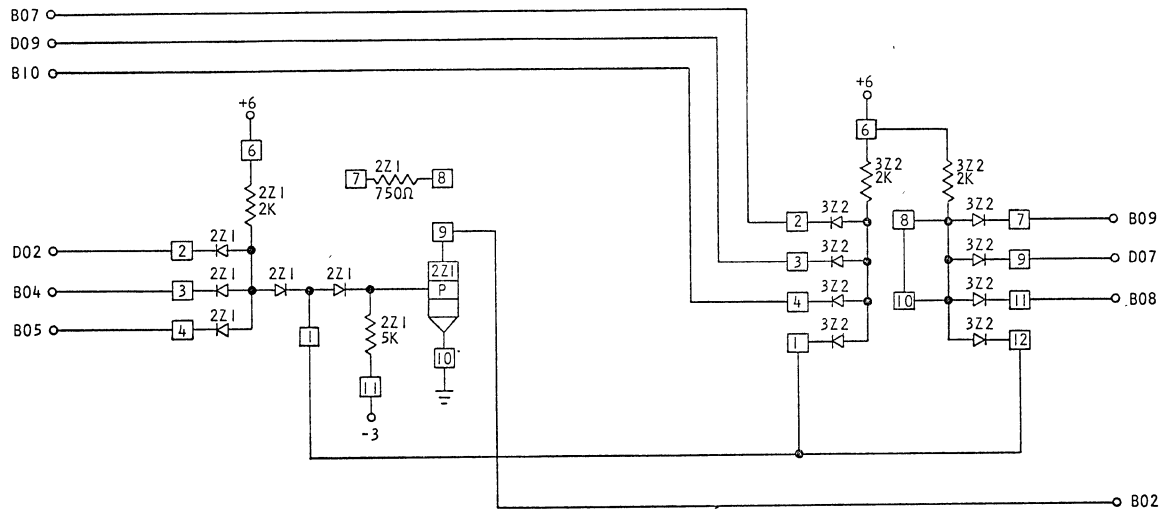
P/N	5800246
EC	160028
STANDARD RESTRICTED	
CARD SIZE	1-6



LMH	O-2860	230	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
Cat.	Subject	Suffix	2-3W,3W,3W AOI WO/L

P/N	5800246
EC	160028





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Page	Date

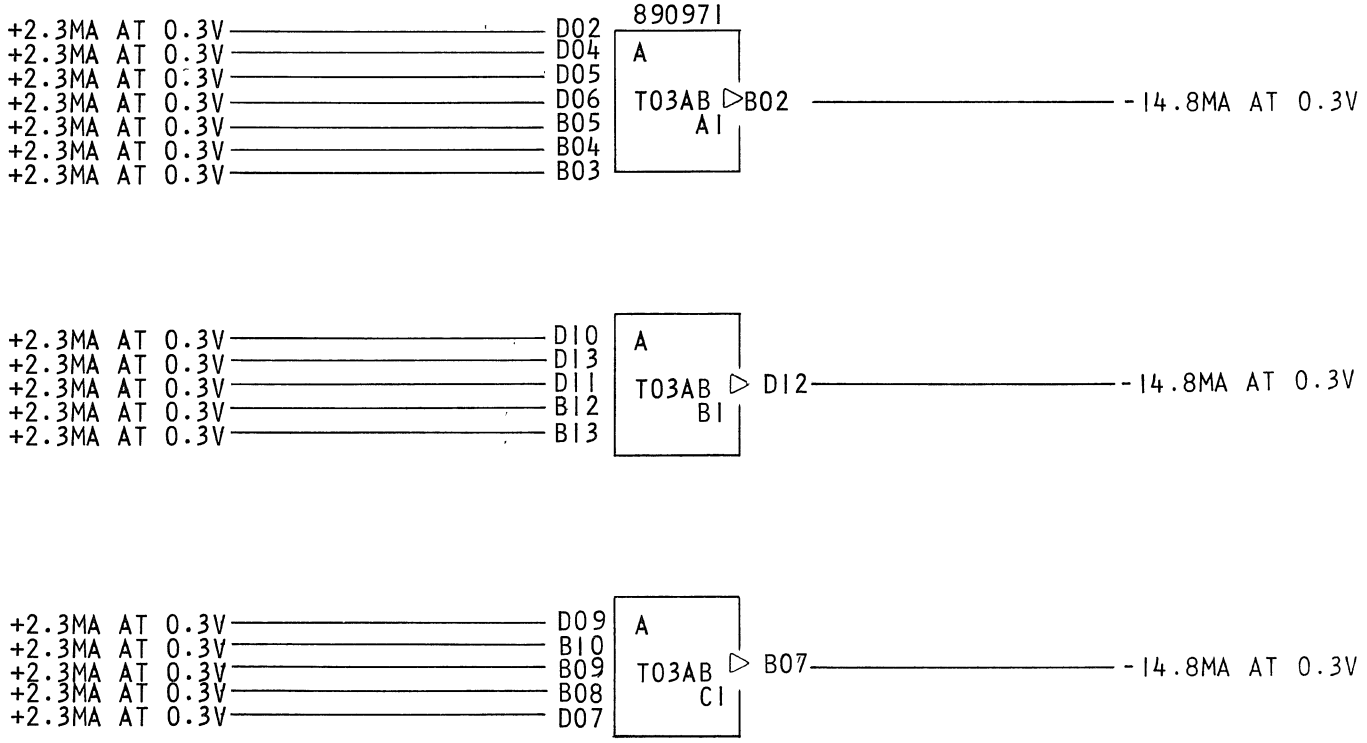
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

2-5W AI & 1-7W AI

CATEGORY CODE

T03

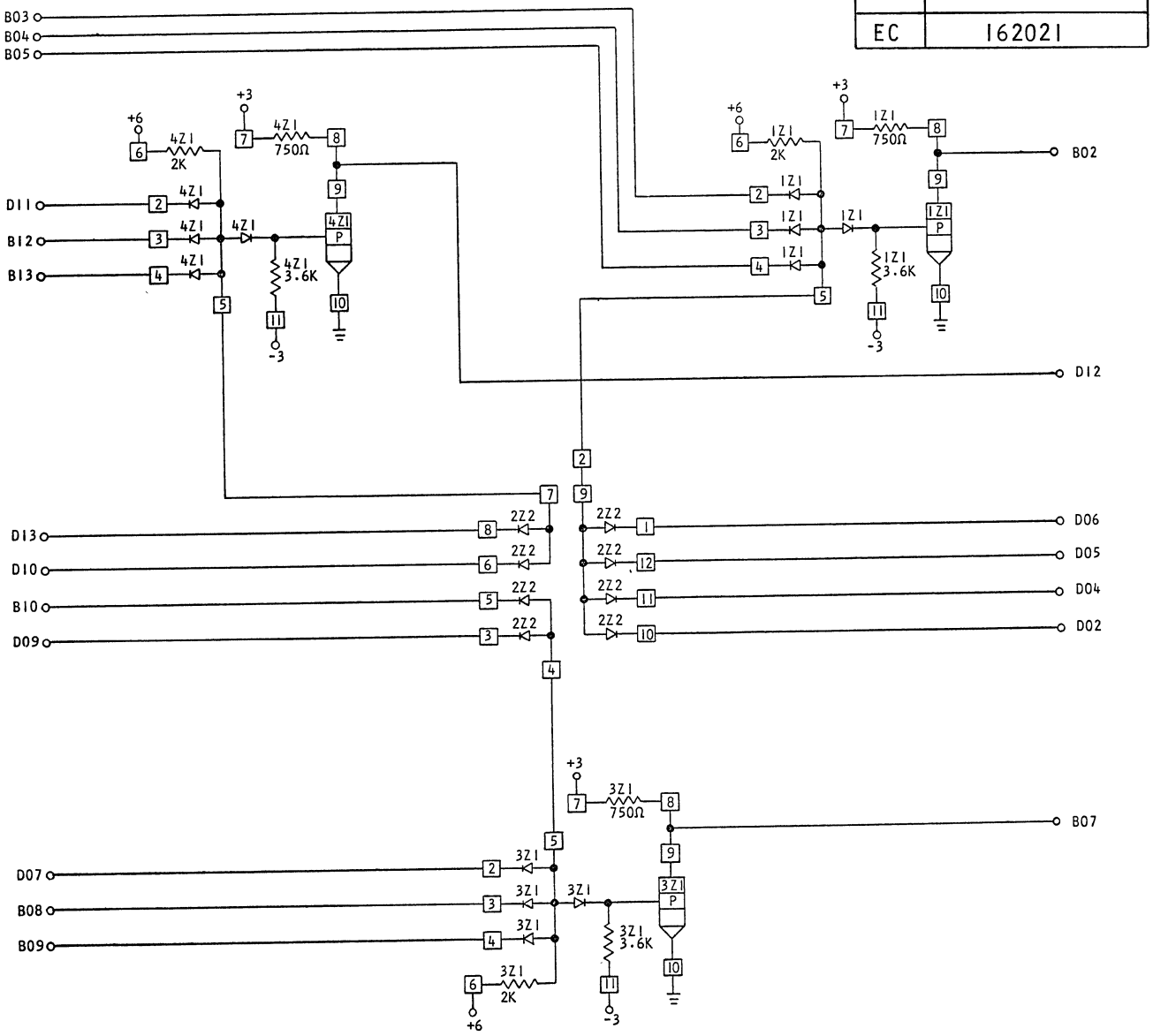
P/N	5800247
EC	162021
STANDARD RESTRICTED	
CARD SIZE	1-6



LMH Cat.	O-2860 Subject	231 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC -EQUIPMENT ENGINEERING
2-5W AI & 1-7W AI

P/N	5800247
EC	162021



2 OF 2 Page	1-67 Date	

IBM Location Manufacturing Specification

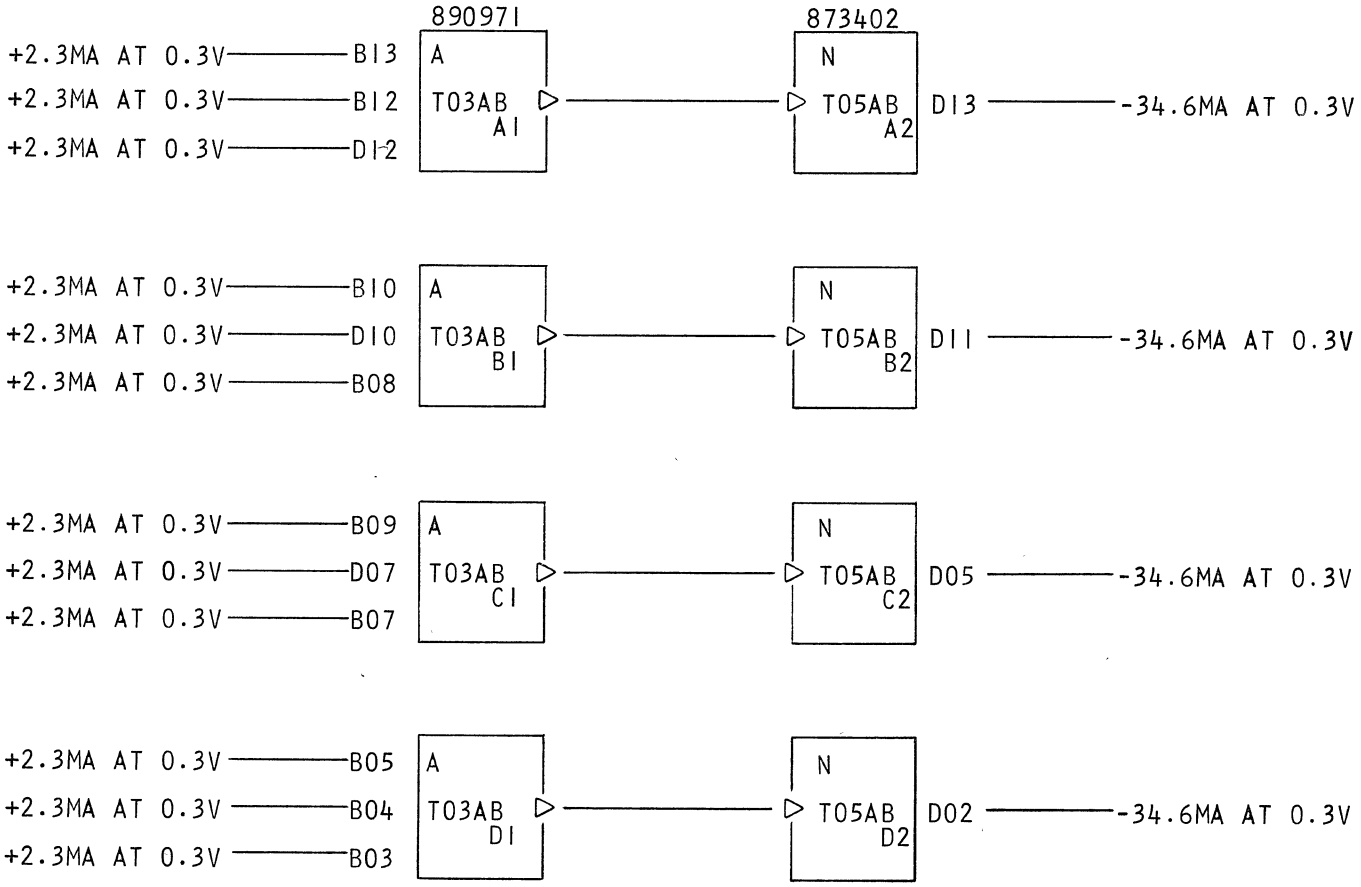
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

4-3W AII

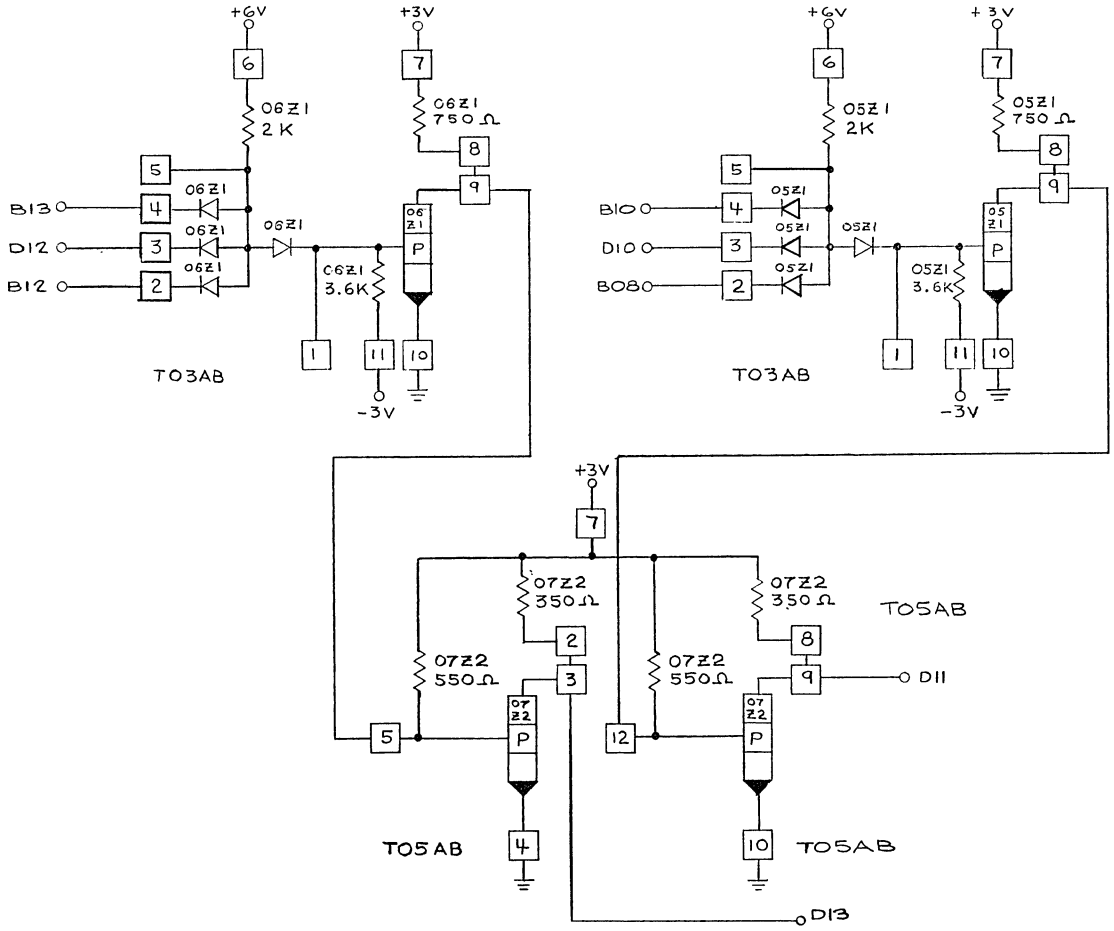
CATEGORY CODE

T03	T05

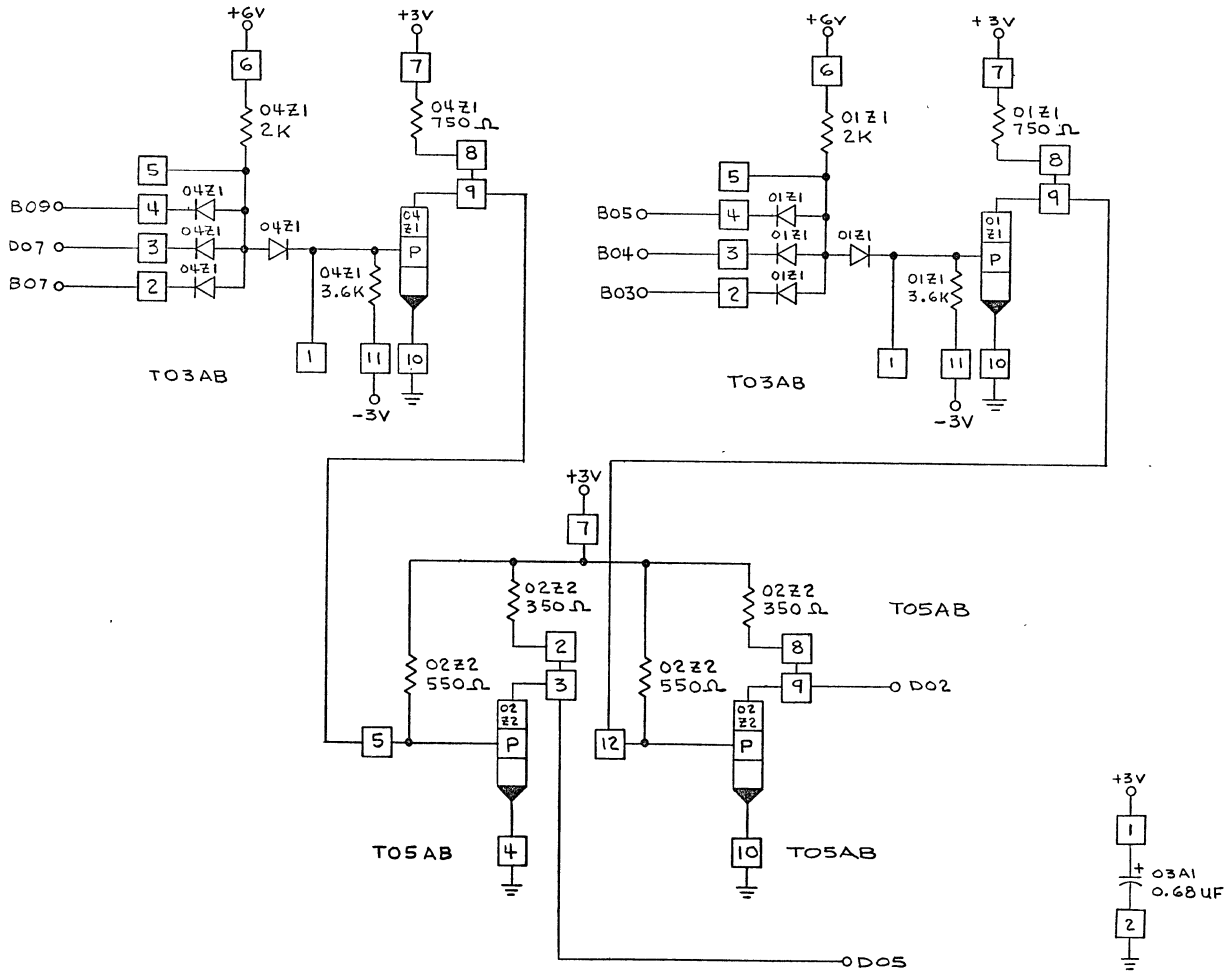
P/N	5800249
EC	163202
STANDARD RESTRICTED	
CARD SIZE	1-6



P/N	5800249
EC	163202



P/N	5800249
EC	163202



Printed in U.S.A.

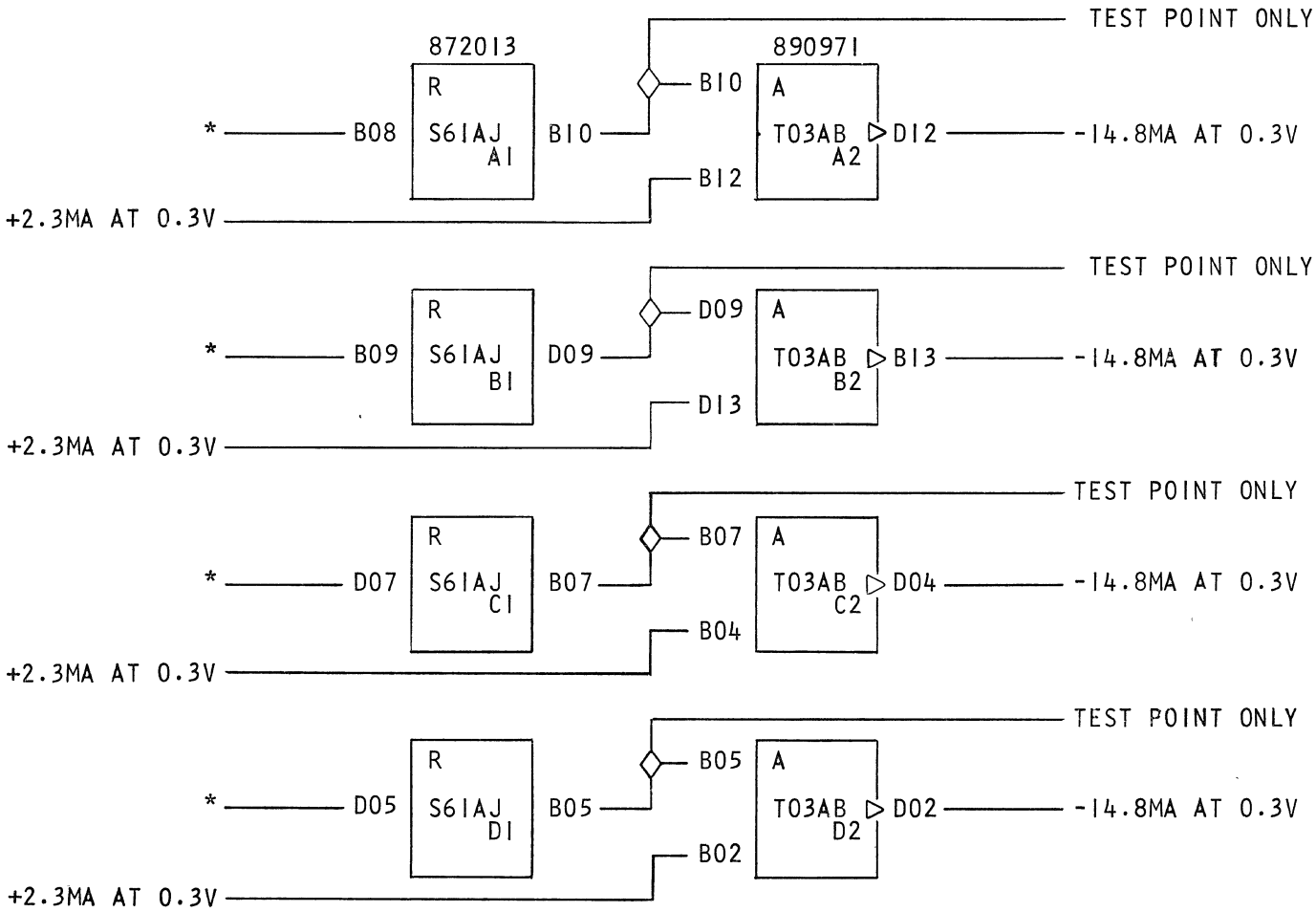
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

STANDARD INTERFACE TERMINATOR

CATEGORY CODE

T03

P/N	5800271
EC	160534
SPECIAL RESTRICTED	
CARD SIZE	1-6

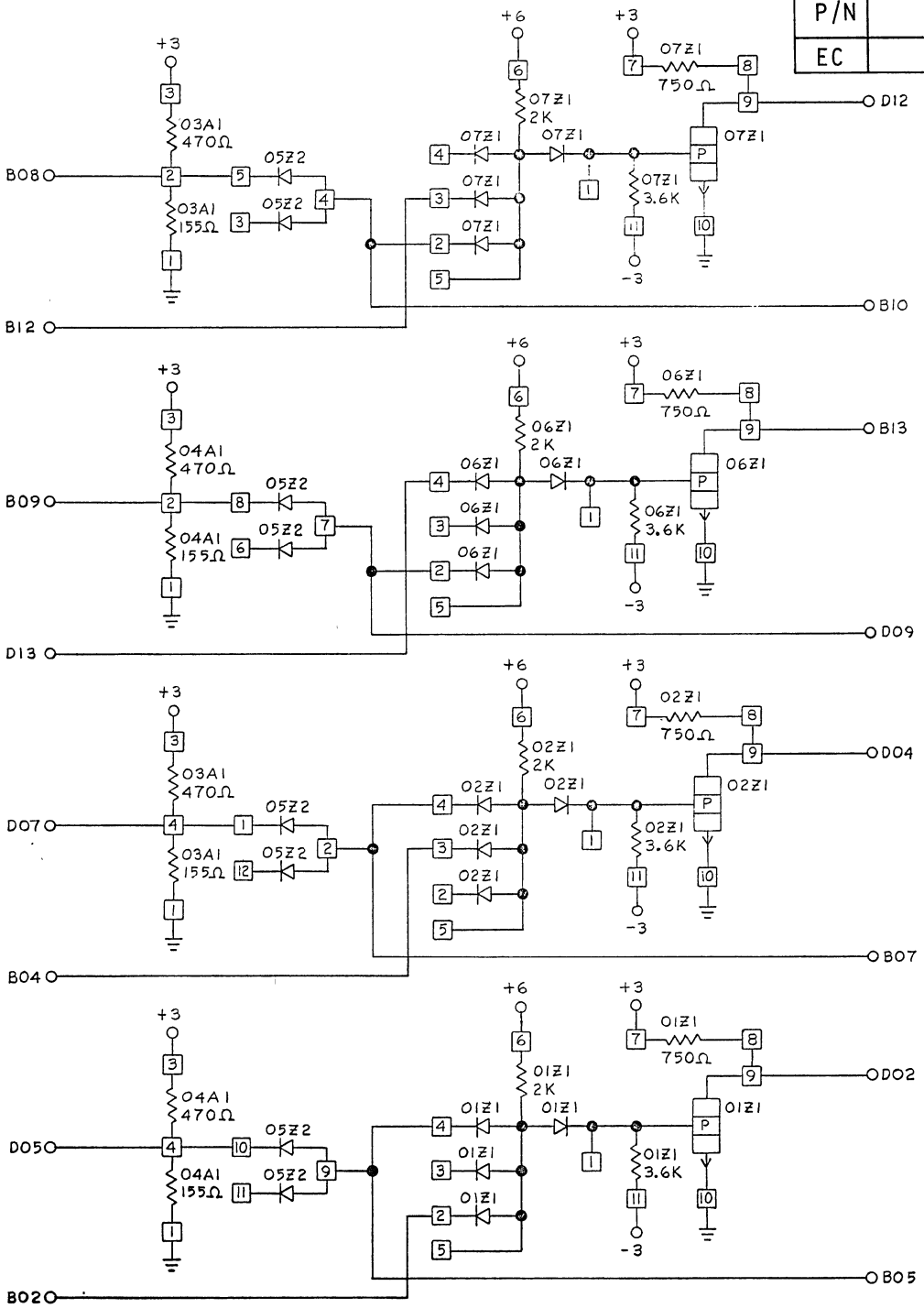


* SPECIAL DRIVE RULE SEE CIRCUIT SPECIFICATION 872013

LMH Cat.	0-2860 Subject	234 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
STANDARD INTERFACE TERMINATOR

P/N	5800271
EC	160534



IBM

Location
Manufacturing Specification

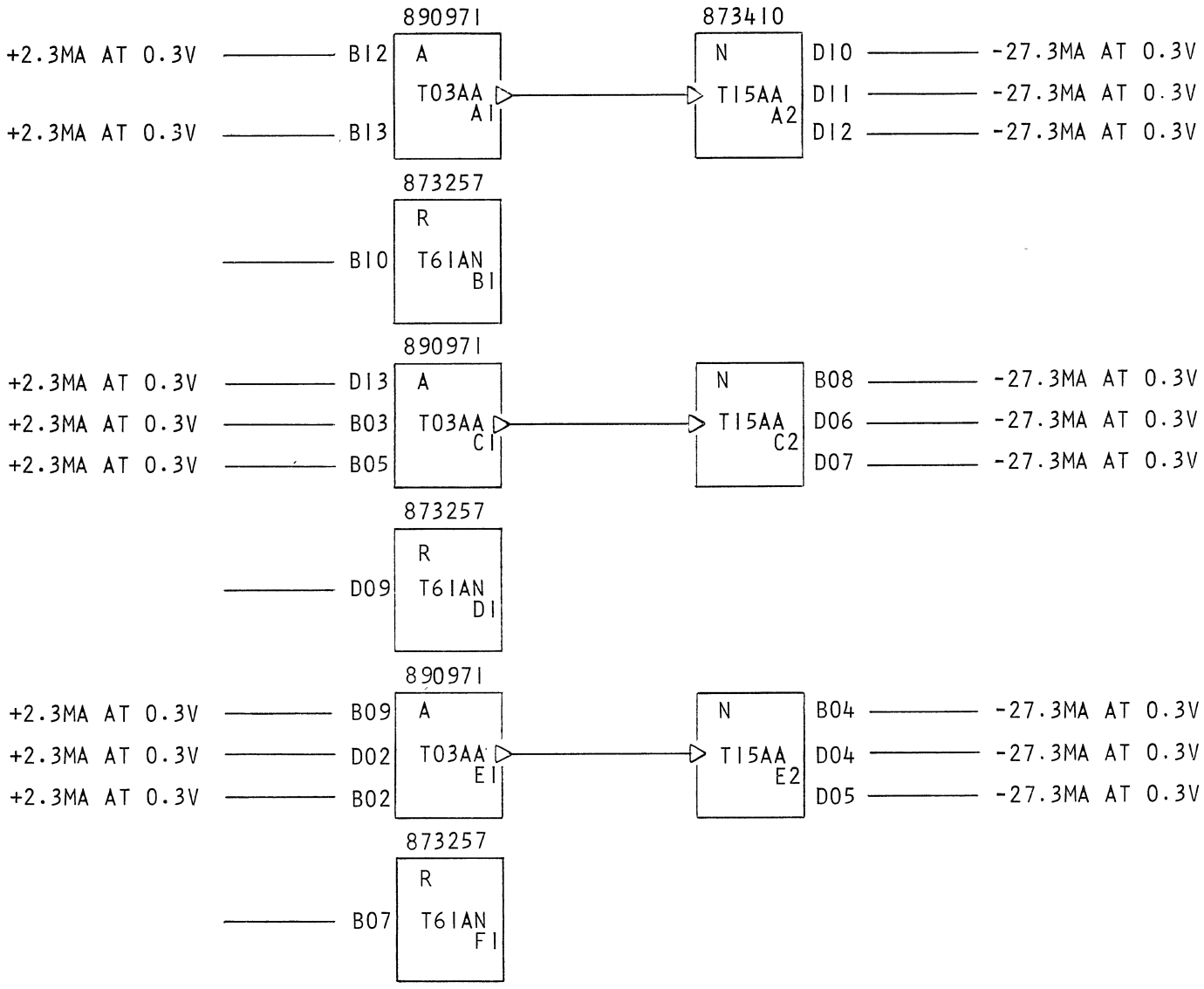
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1-2WA HPD, 2-3WA HPD

CATEGORY CODE

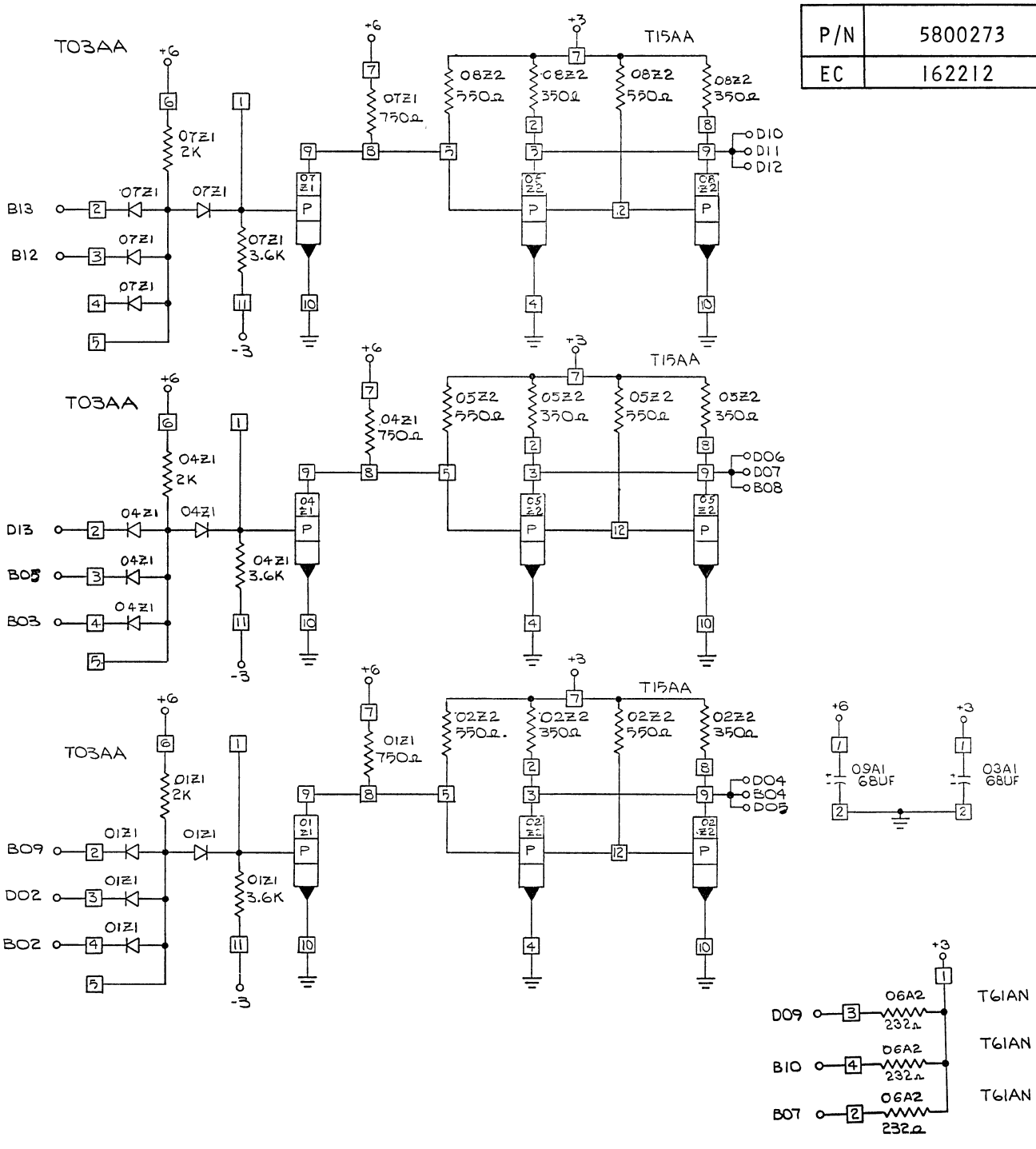
T03

P/N	5800273
EC	162212
STANDARD RESTRICTED	
CARD SIZE	1-6



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-2WA HPD, 2-3WA HPD

P/N	5800273
EC	162212



IBM Location Manufacturing Specification

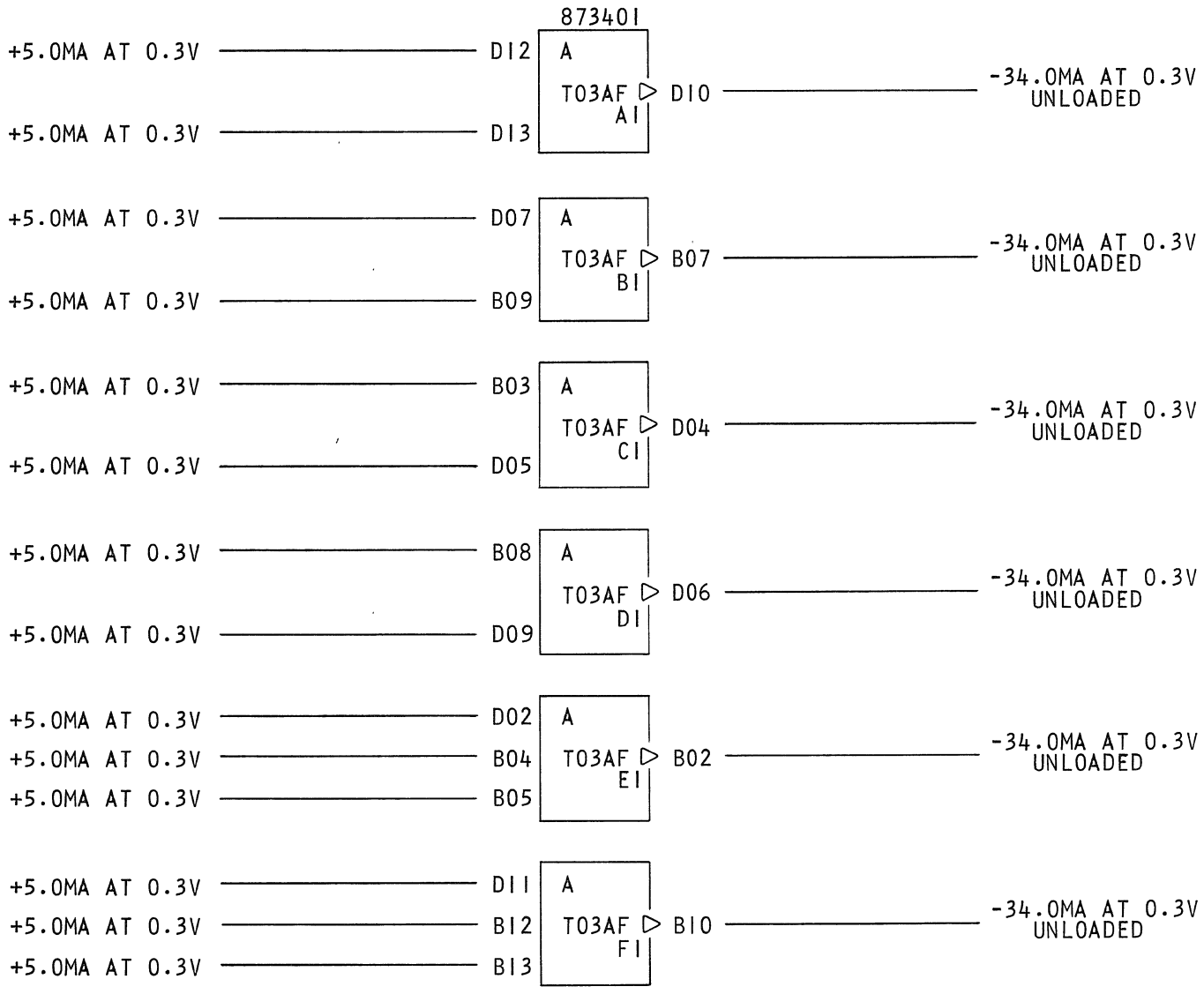
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D08	GND

2-3W API WO/L & 4-2W API WO/L

CATEGORY CODE

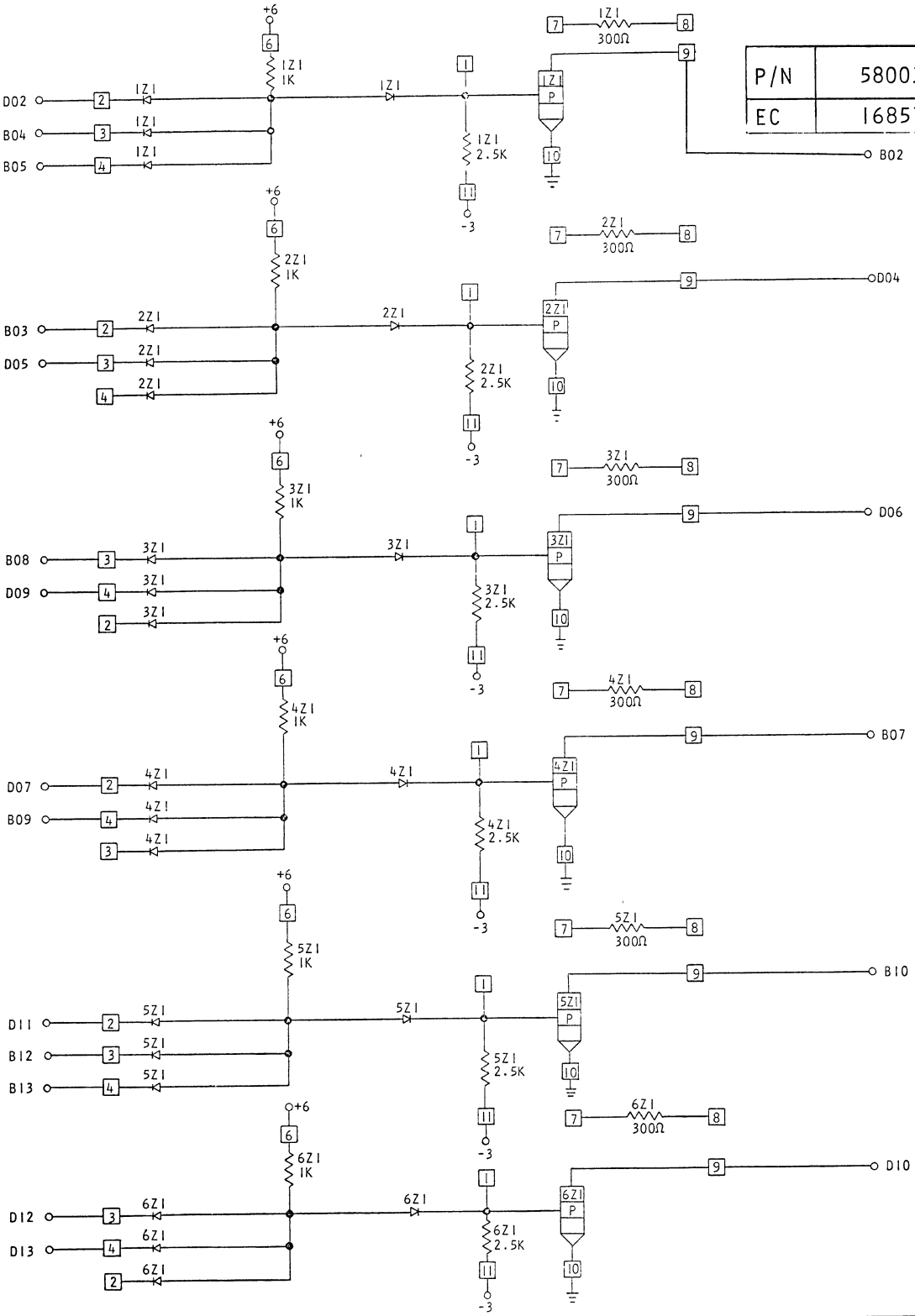
T03

P/N	5800310
EC	168573 B
STANDARD RESTRICTED	
CARD SIZE	1-6



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-3W API WO/L & 4-2W API WO/L

P/N	5800310
EC	168573B



IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D08	GND

5-3W API W0/L

CATEGORY CODE

T03

P/N	5800311
EC	162010
STANDARD	RESTRICTED
CARD SIZE	1-6

873401

+5MA AT 0.3V — D10
+5MA AT 0.3V — D12
+5MA AT 0.3V — D13

A
T03AF A1 ▷ D09 — -34MA AT 0.3V UNLOADED

+5MA AT 0.3V — D11
+5MA AT 0.3V — B12
+5MA AT 0.3V — B13

A
T03AF B1 ▷ B10 — -34MA AT 0.3V UNLOADED

+5MA AT 0.3V — D07
+5MA AT 0.3V — B08
+5MA AT 0.3V — B09

A
T03AF C1 ▷ B07 — -34MA AT 0.3V UNLOADED

+5MA AT 0.3V — D02
+5MA AT 0.3V — B04
+5MA AT 0.3V — B05

A
T03AF D1 ▷ B02 — -34MA AT 0.3V UNLOADED

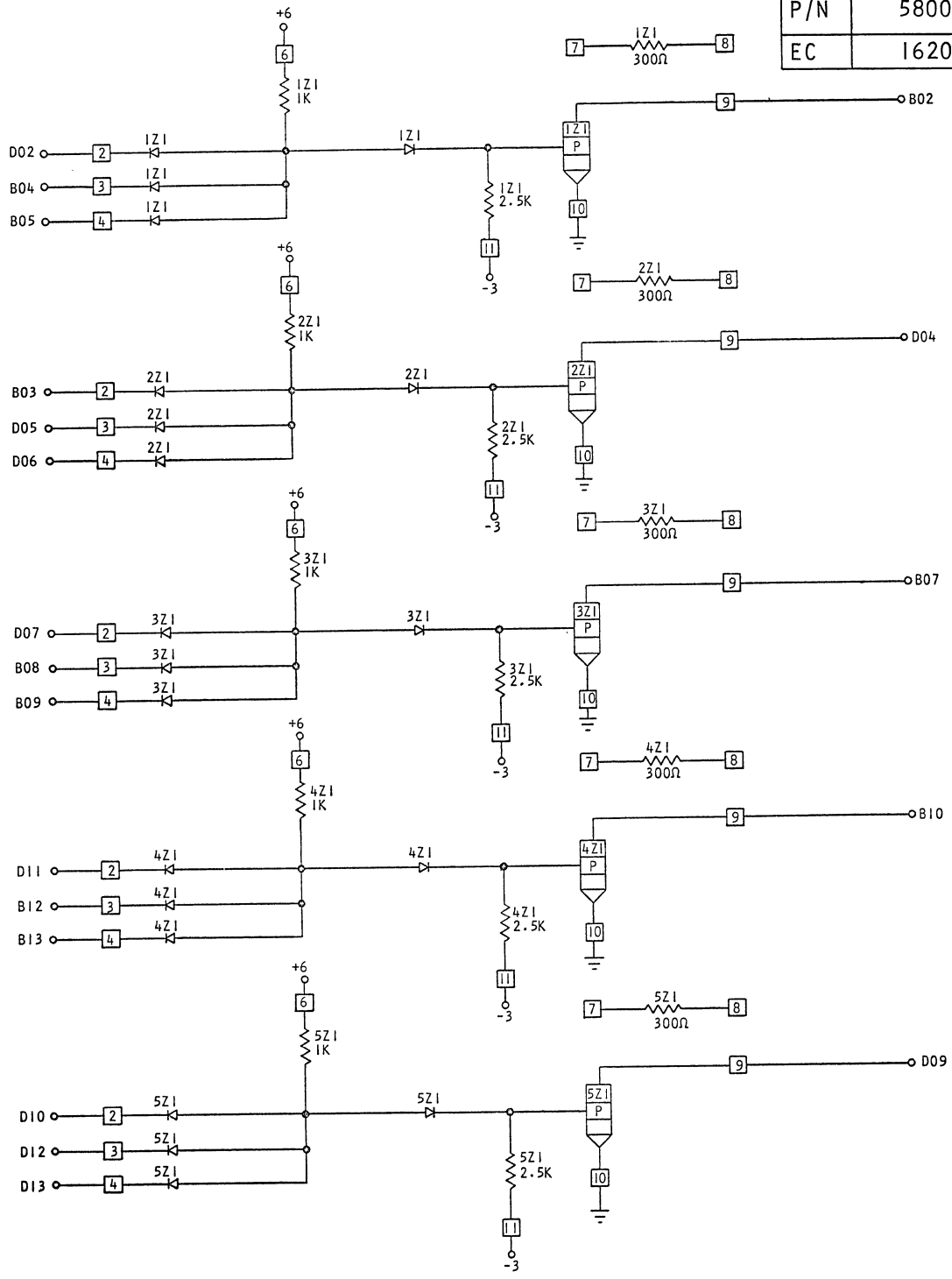
+5MA AT 0.3V — B03
+5MA AT 0.3V — D05
+5MA AT 0.3V — D06

A
T03AF E1 ▷ D04 — -34MA AT 0.3V UNLOADED

LMH	O-2860	238
Cat.	Subject	Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
5-3W API W0/L

P/N	5800311
EC	162010



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Page	Date

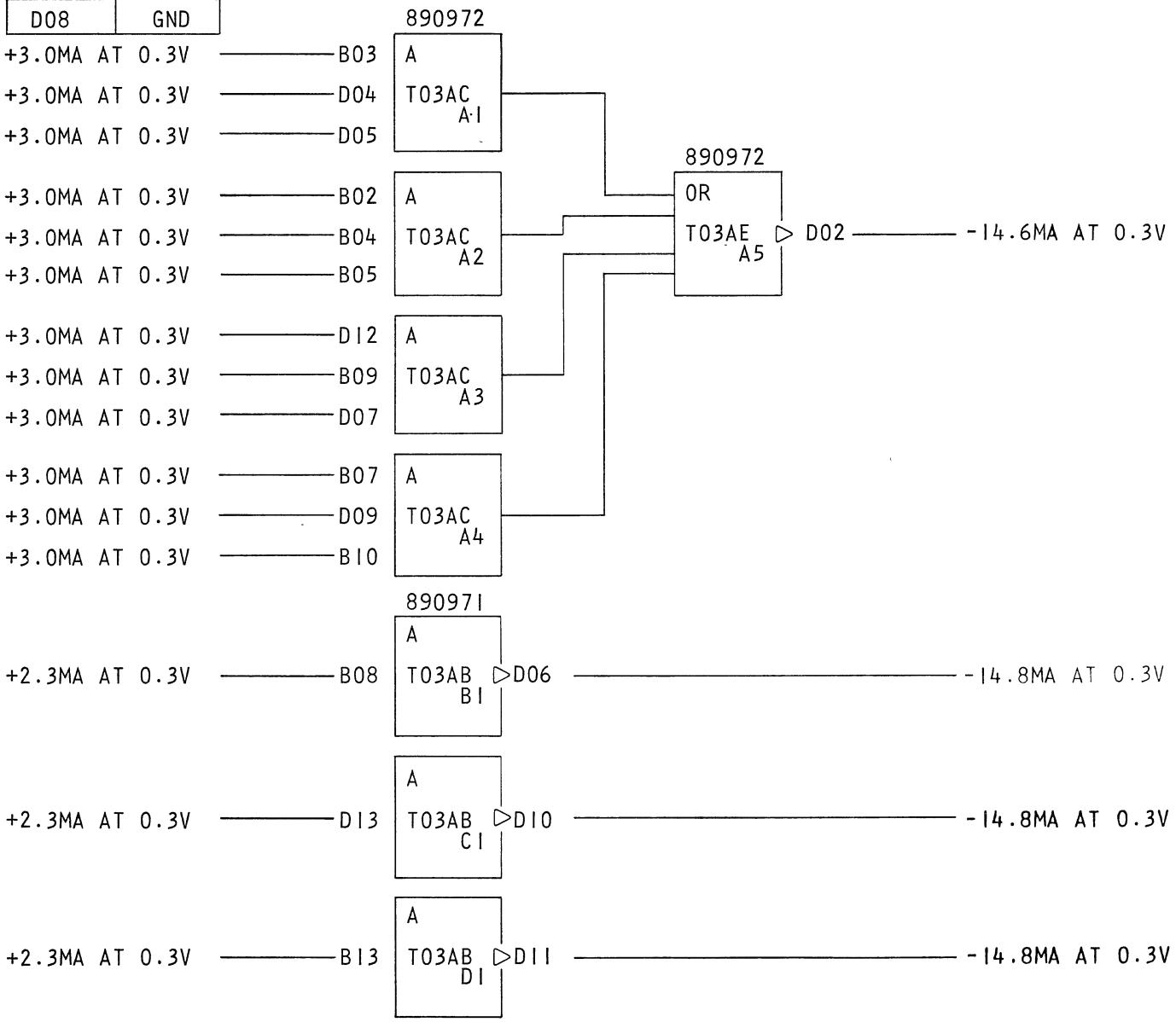
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

1-3W,3W,3W,3W AOI & 3-IW AI

CATEGORY CODE

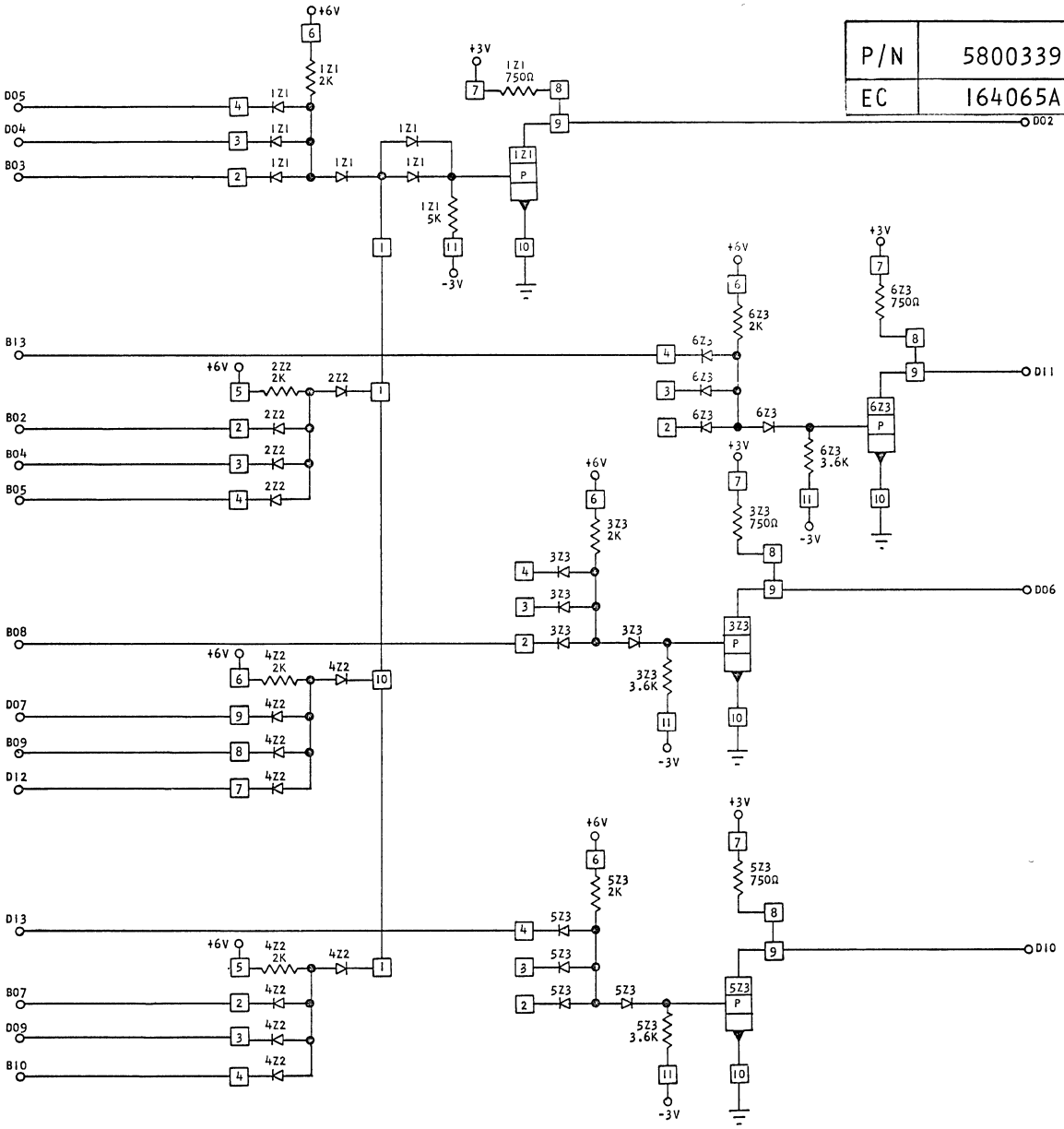
T03

P/N	5800339
EC	164065A
STANDARD RESTRICTED	
CARD SIZE	1-6

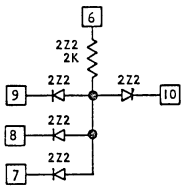


SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-3W, 3W, 3W, 3W AOI & 3-1W AI

P/N	5800339
EC	164065A



UNUSED COMPONENTS



NOTE: NO VOLTAGE PINS BUSSED

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-5W, 5W, 5W,AOI & 2-1W AOI

LMH Cat.	0-2860 Subject	240 Suffix

IBM Location Manufacturing Specification

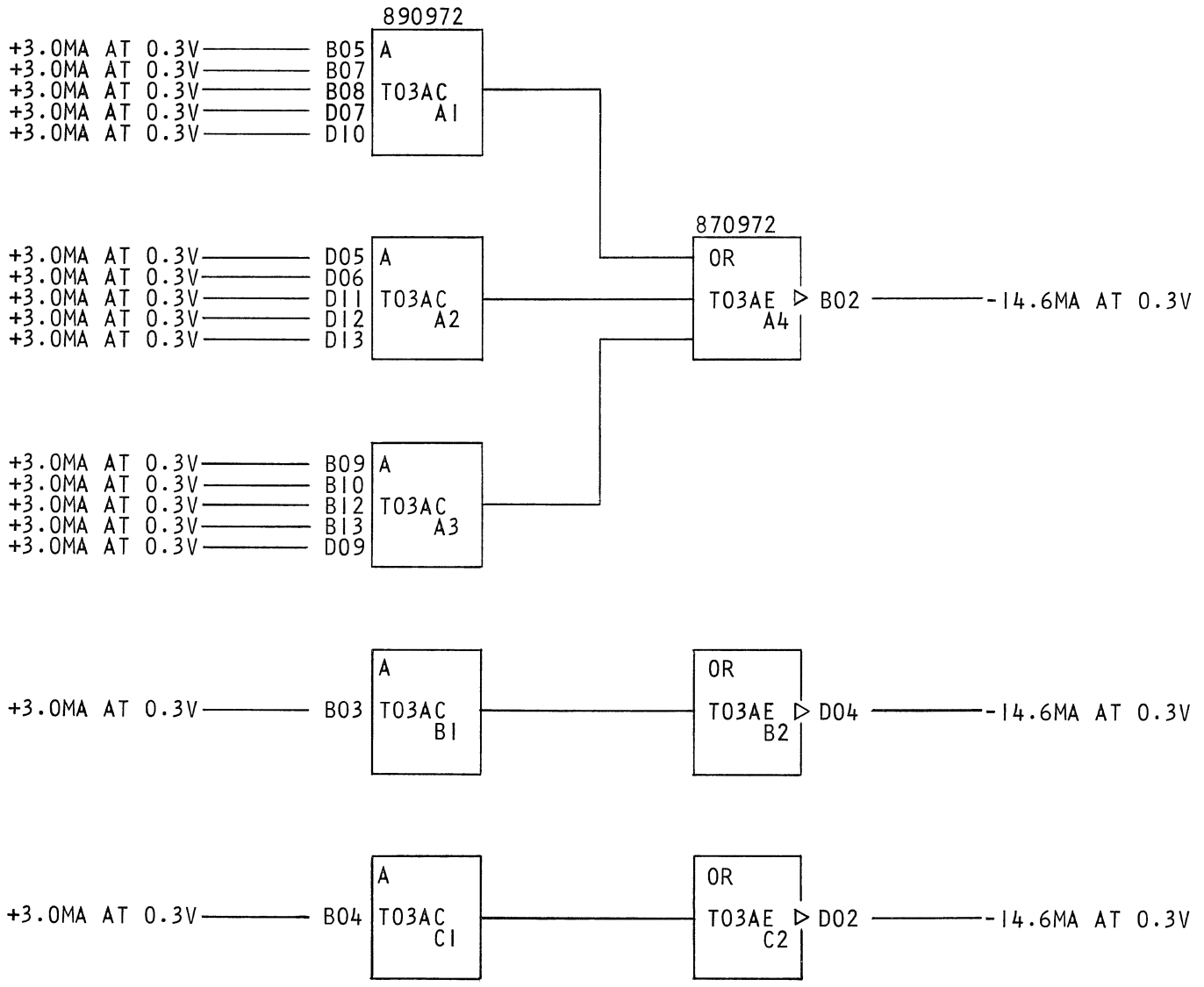
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1-5W, 5W, 5W AOI & 2-1W AOI

CATEGORY CODE

T03

P/N	5800342
EC	164067 A
STANDARD RESTRICTED	
CARD SIZE	1-6



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Applicability ENDICOTT		ENDICOTT Responsibility	1-67 Date / 1 OF 2 Page

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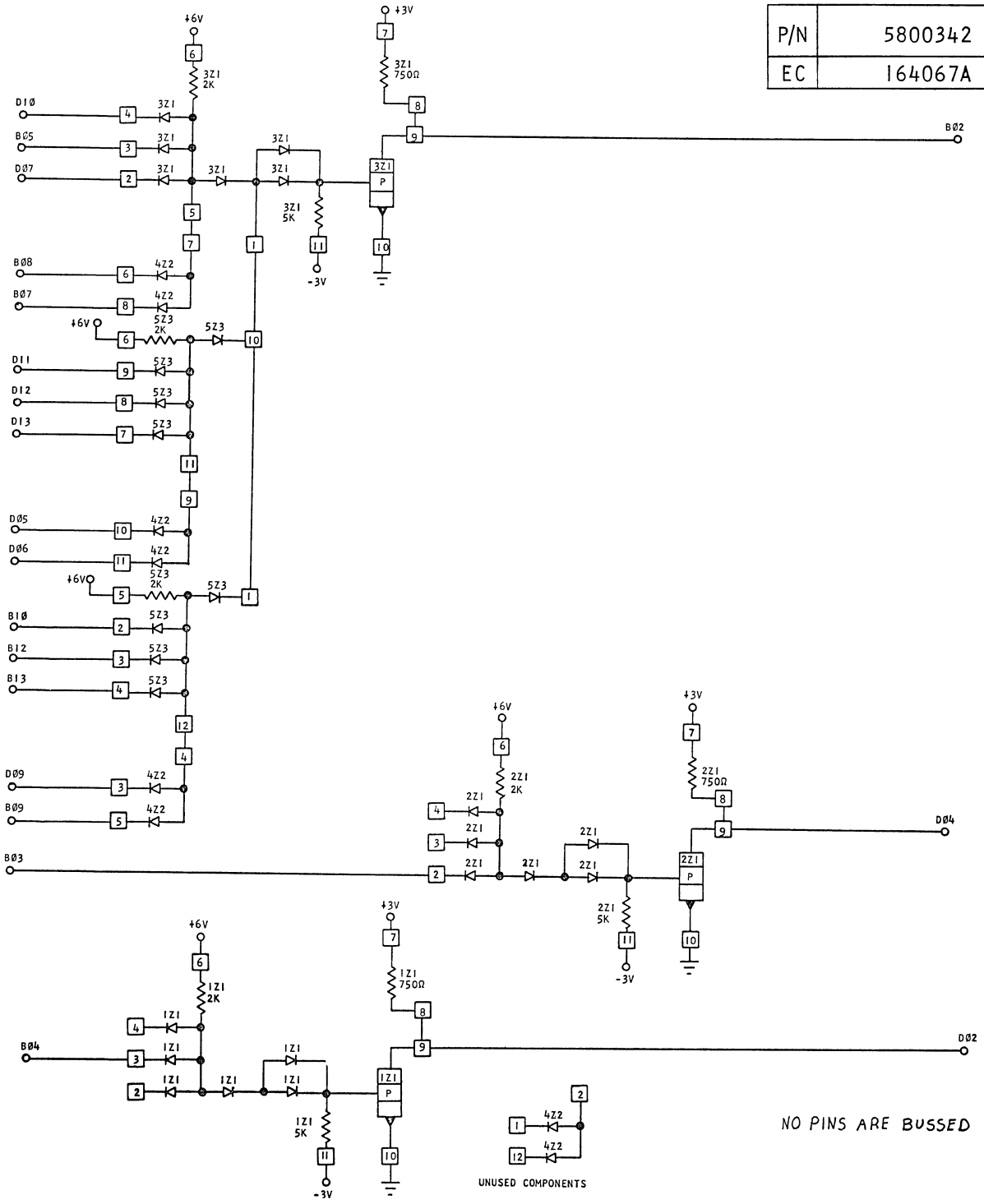
P/N	5800342
EC	164067A



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-IW DCI & 4 II WITH PROGRAMMABLE RESISTORS

LMH Cat.	0-2860 Subject	241 Suffix

IBM **Location Manufacturing Specification**

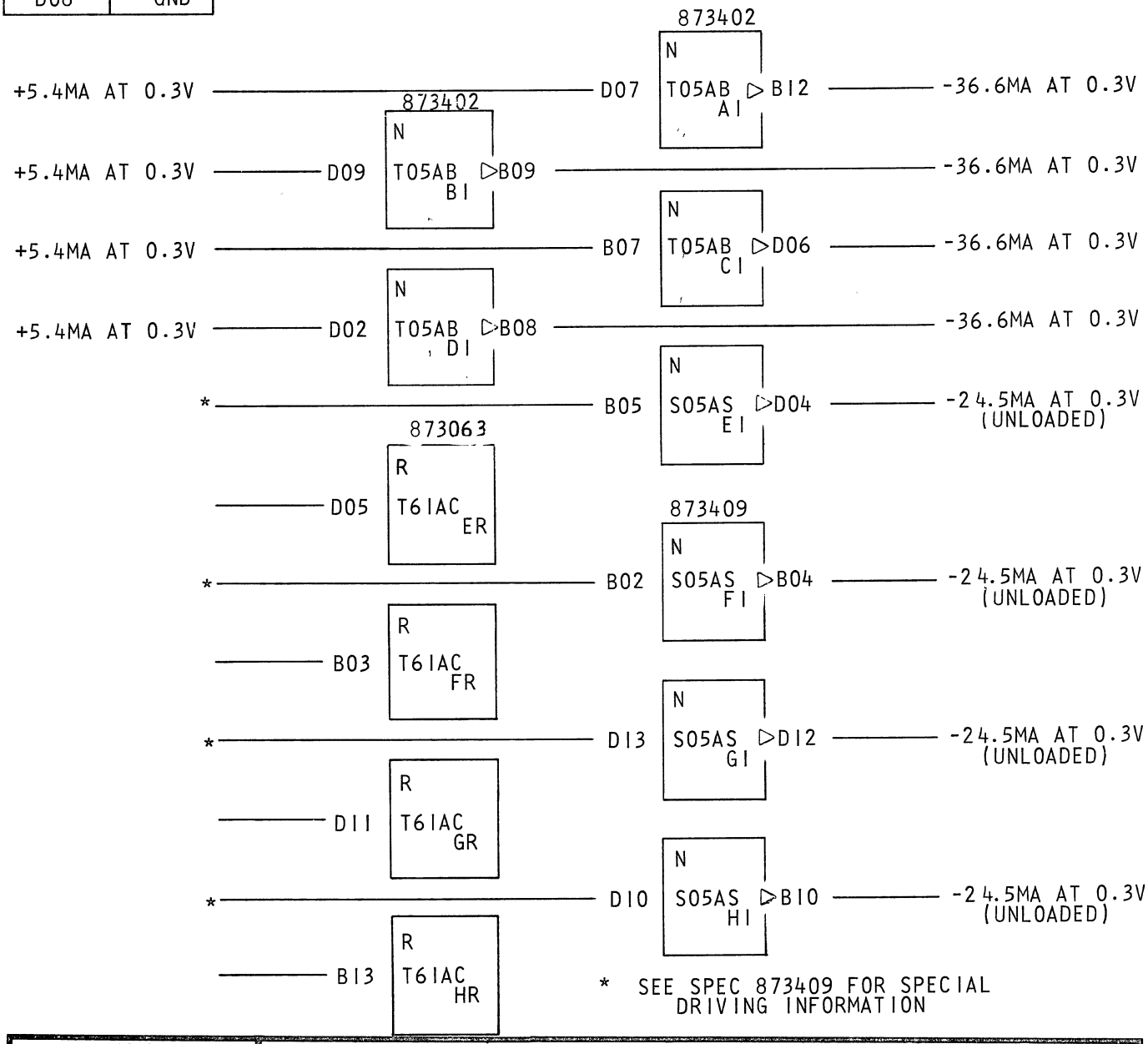
POWER REQUIRED	
PIN	VOLT
B06	-3
B11	+6
D03	+3
D08	GND

4-IW DCI & 4 II WITH PROGRAMMABLE RESISTORS

CATEGORY CODE

T05	S05

P/N	5800346
EC	160025
EXPERIMENTAL RSRD	
CARD SIZE	I-6



* SEE SPEC 873409 FOR SPECIAL DRIVING INFORMATION

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.		
ENDICOTT Applicability		ENDICOTT Responsibility	1-67 Date	1 of 2 Page

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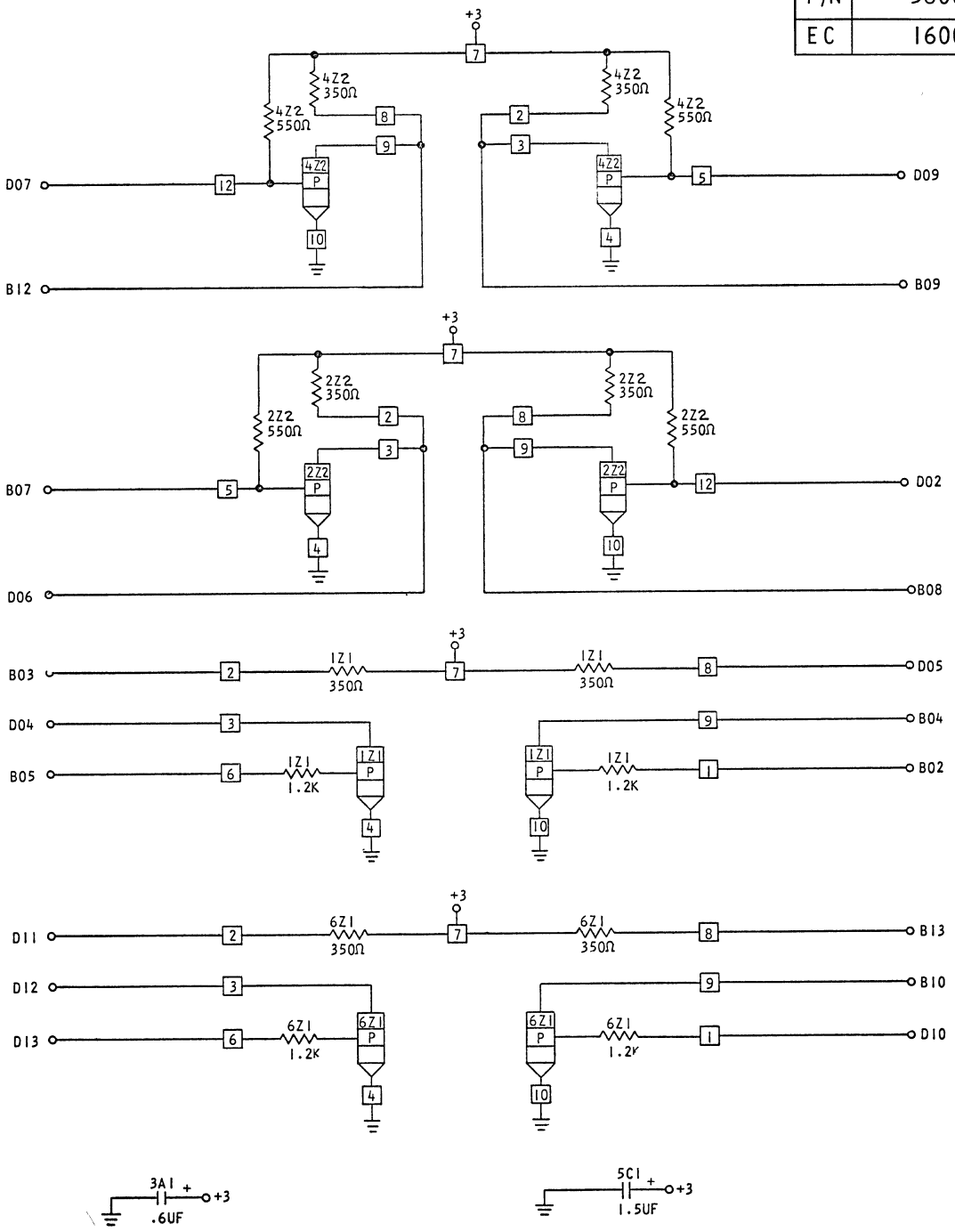
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-IW DCI & 4 II WITH PROGRAMMABLE RESISTORS

P/N	5800346
EC	160025



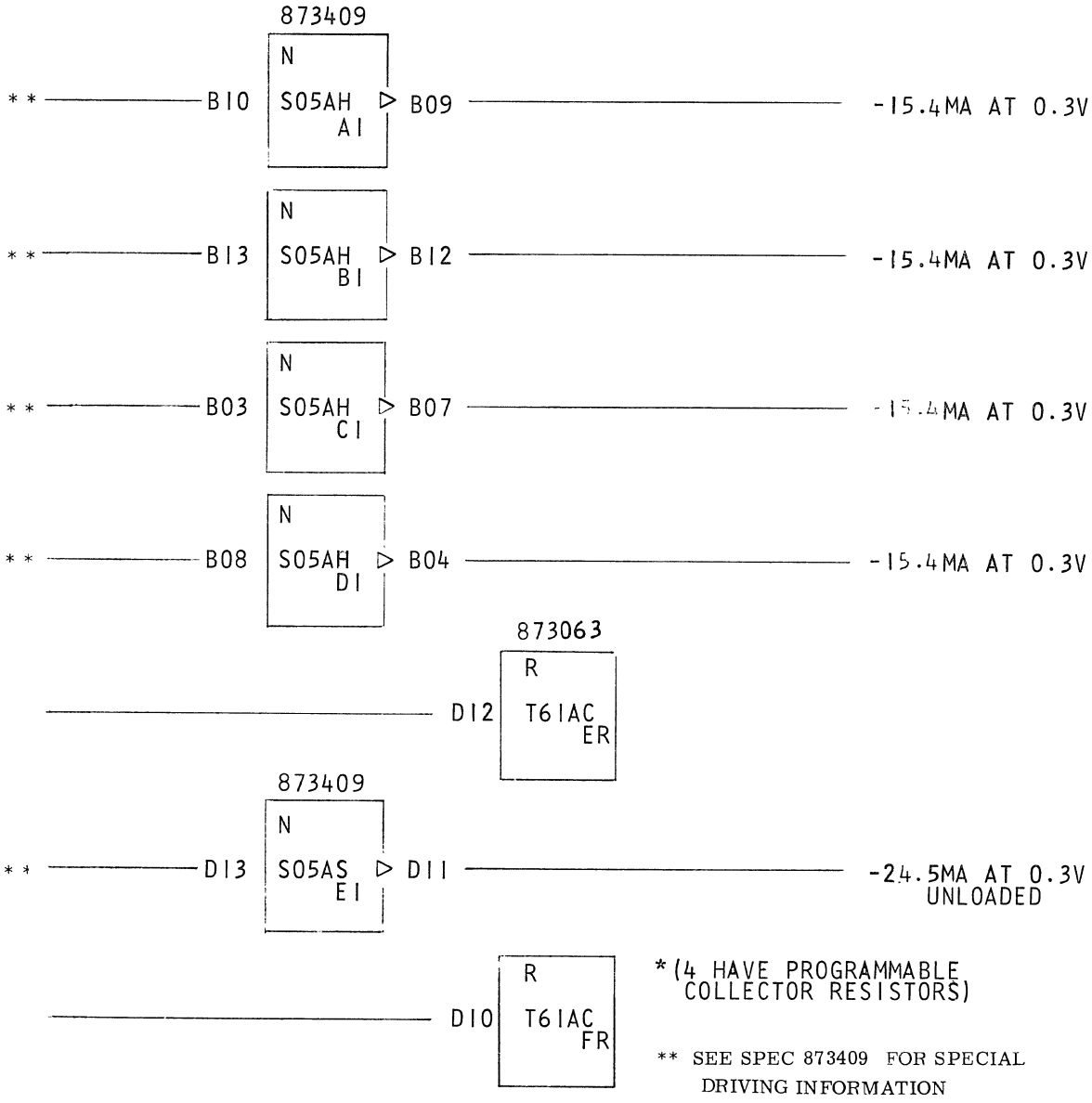
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

4II & 4II WO/L & 4PROGRAMMABLE RESISTORS

CATEGORY CODE

S05

P/N	5800347
EC	163874
STANDARD RESTRICTED	
CARD SIZE	1-6



*(4 HAVE PROGRAMMABLE COLLECTOR RESISTORS)

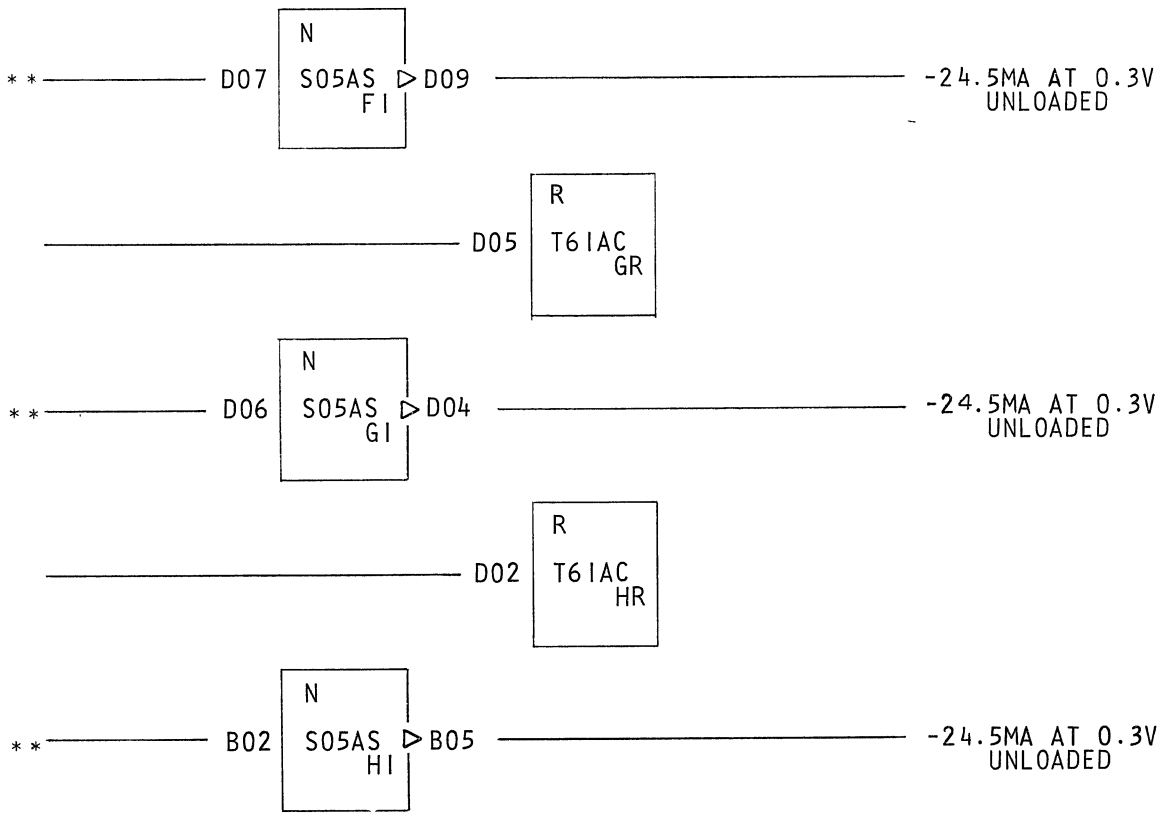
** SEE SPEC 873409 FOR SPECIAL DRIVING INFORMATION

4III & 4III W0/L & 4PROGRAMMABLE RESISTORS

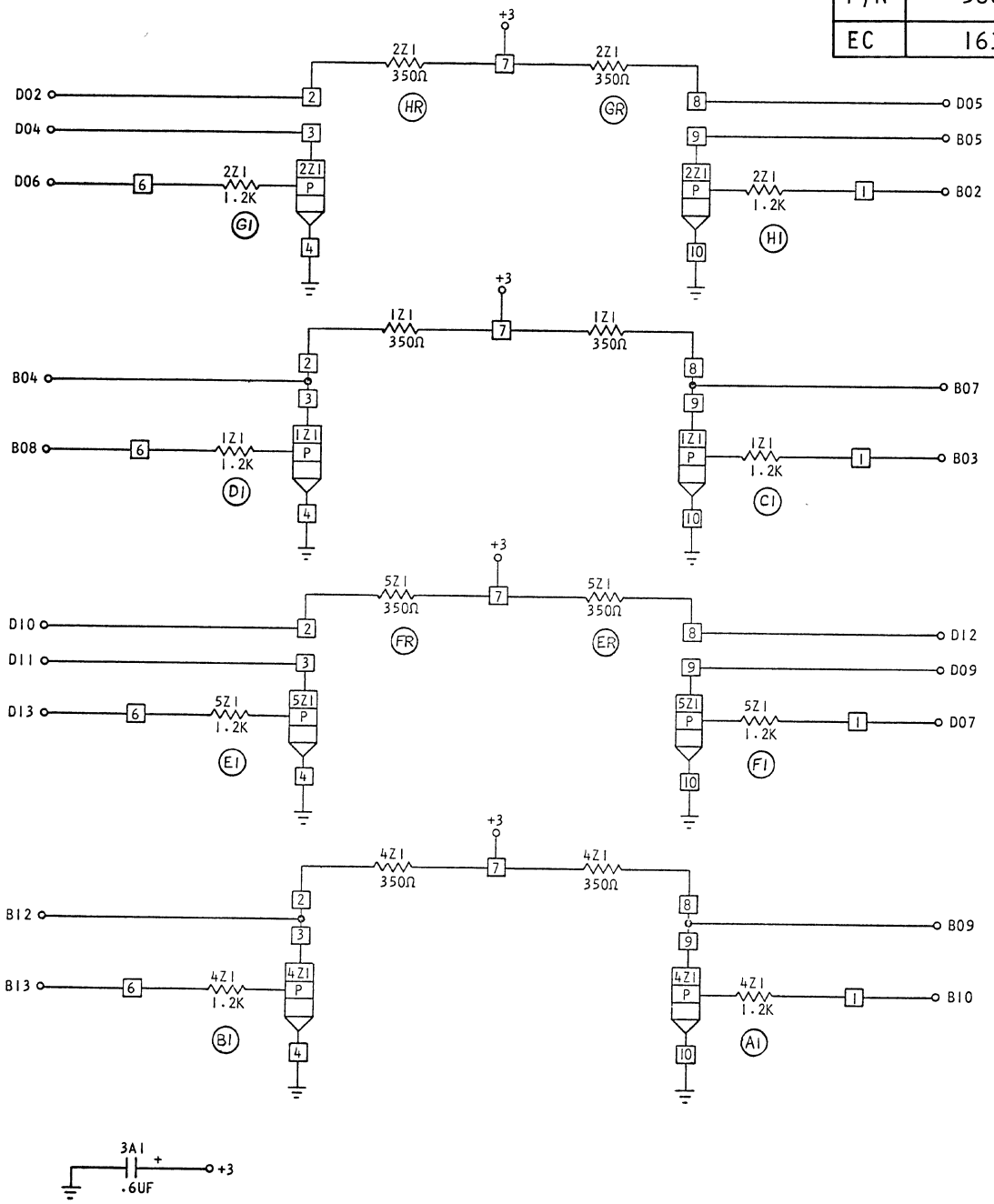
CATEGORY CODE

S05

P/N	5800347
EC	163874



P/N	5800347
EC	163874



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-3W API & 1-5W,5W AOI & 2-2W AI COMB.

LMH	0-2860	243
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

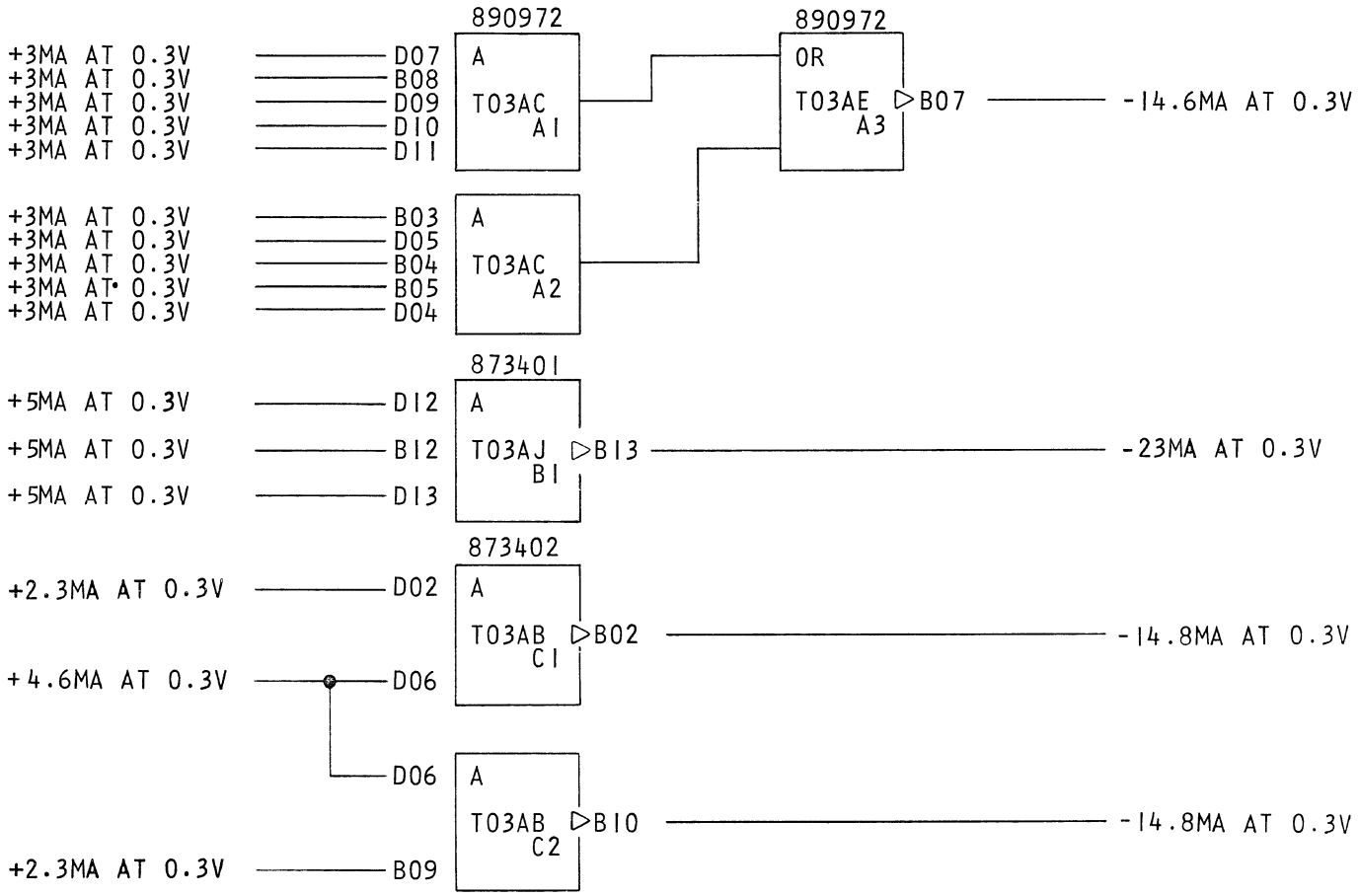
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1-3W API & 1-5W,5W AOI & 2-2W AI COMB.

CATEGORY CODE

T03

P/N	5800355
EC	162807
STANDARD RESTRICTED	
CARD SIZE	1-6



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Primary Standards Manual	Other standards manuals in which this document may be filed.			
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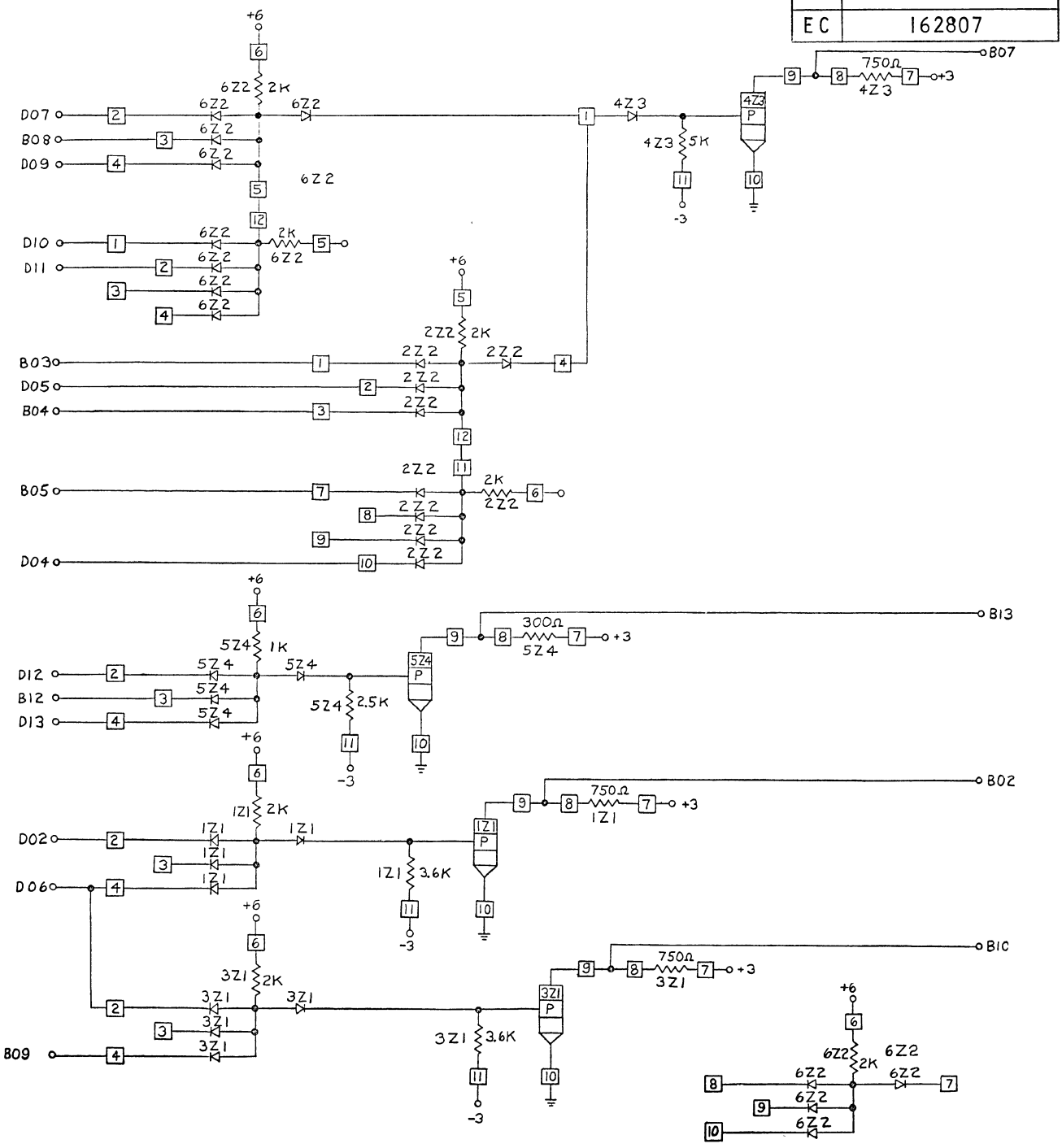
LMH	O-2860	243	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 1-3W API & 1-5W,5W AOI & 2-2W AI COMB.
Cat	Subject	Suffix	

P/N	5800355
EC	162807



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
LINE SENSE AMPLIFIER-LSA

LMH	0-2860	244
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

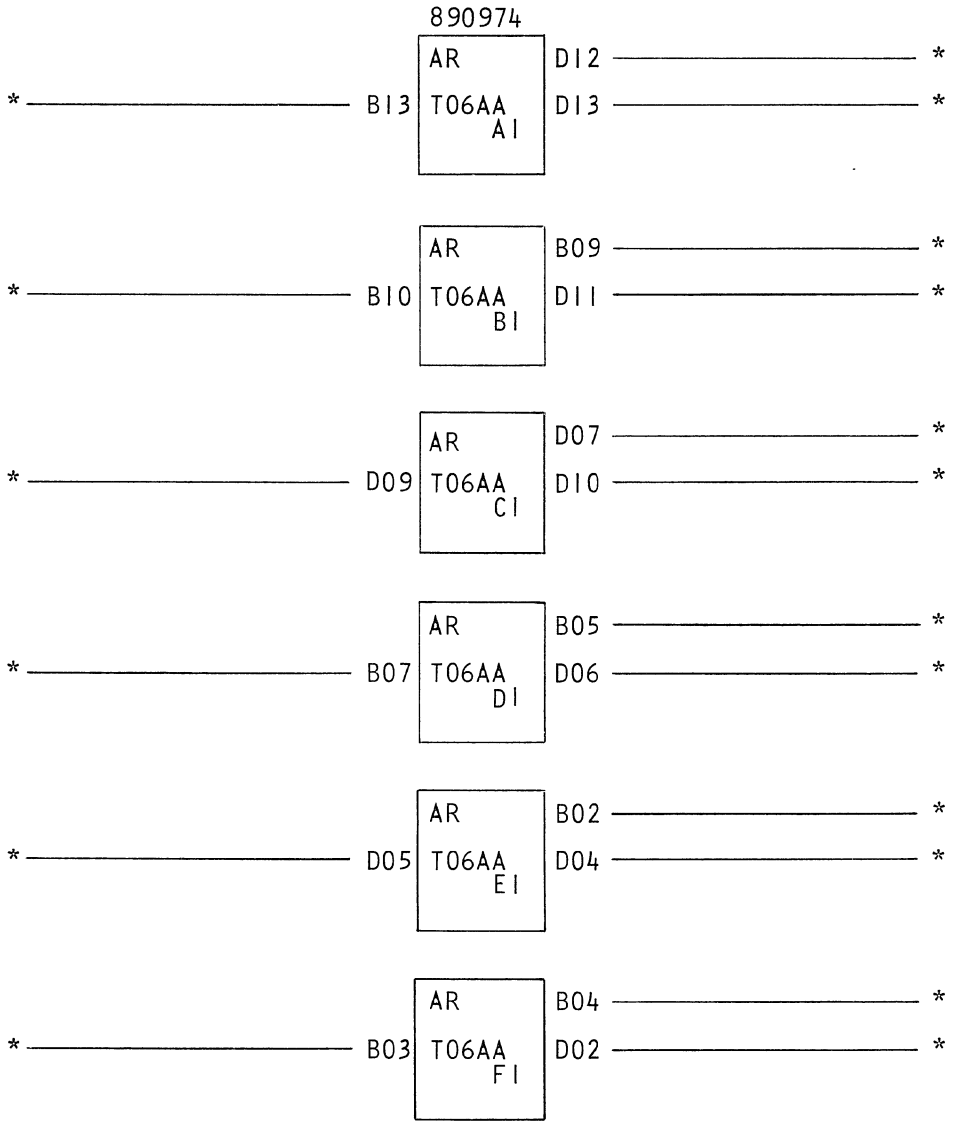
POWER REQUIRED	
PIN	VOLTS
B11	+6
D08	GND

LINE SENSE AMPLIFIER-LSA

CATEGORY CODE

T06

P/N	5800422	
EC	163200	
STANDARD RESTRICTED		
CARD SIZE		1-6



*SEE SPEC NUMBER 890974 FOR DRIVING AND LOADING INFORMATION

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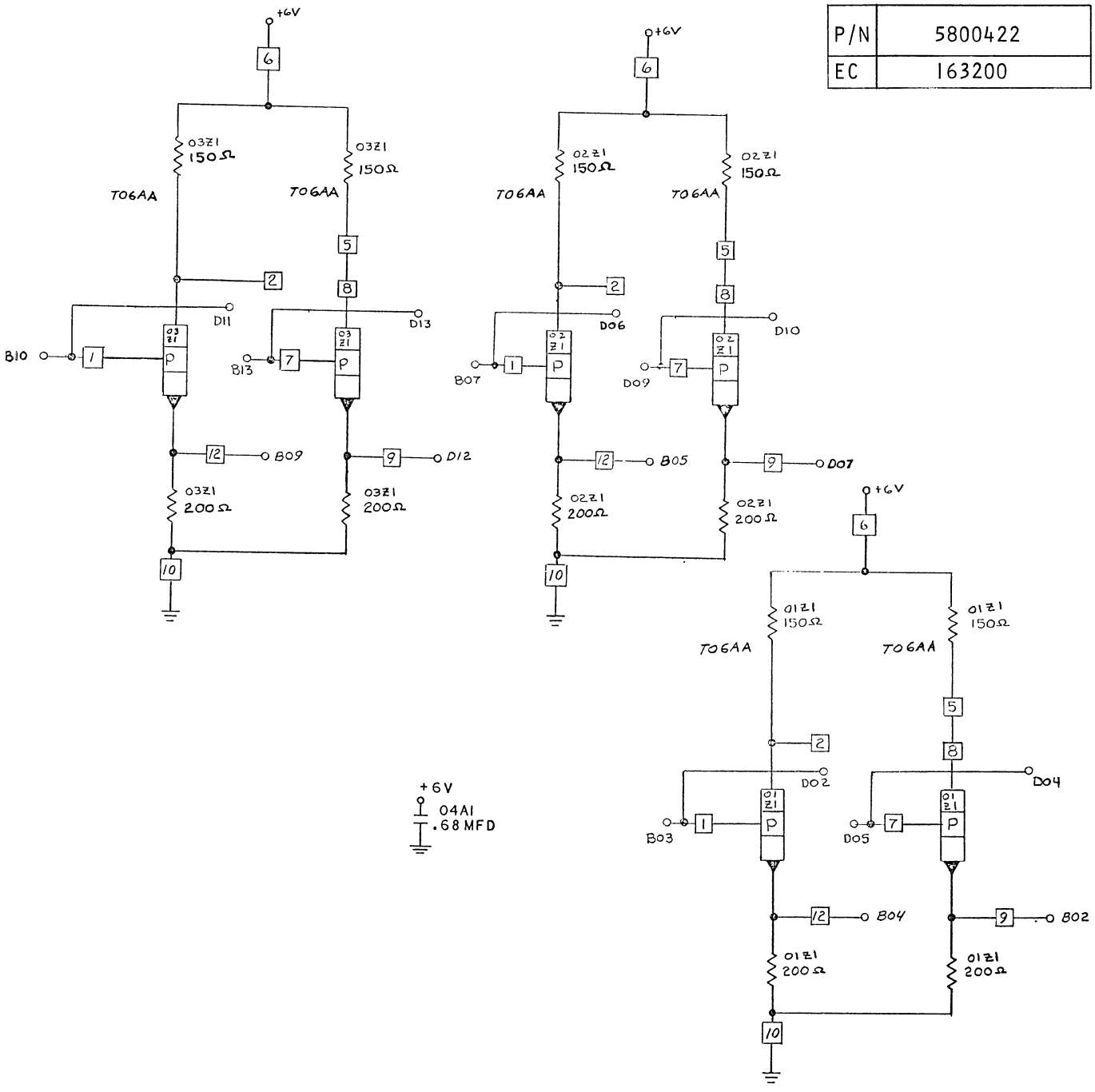
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
LINE SENSE AMPLIFIER-LSA

P/N	5800422
EC	163200



IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

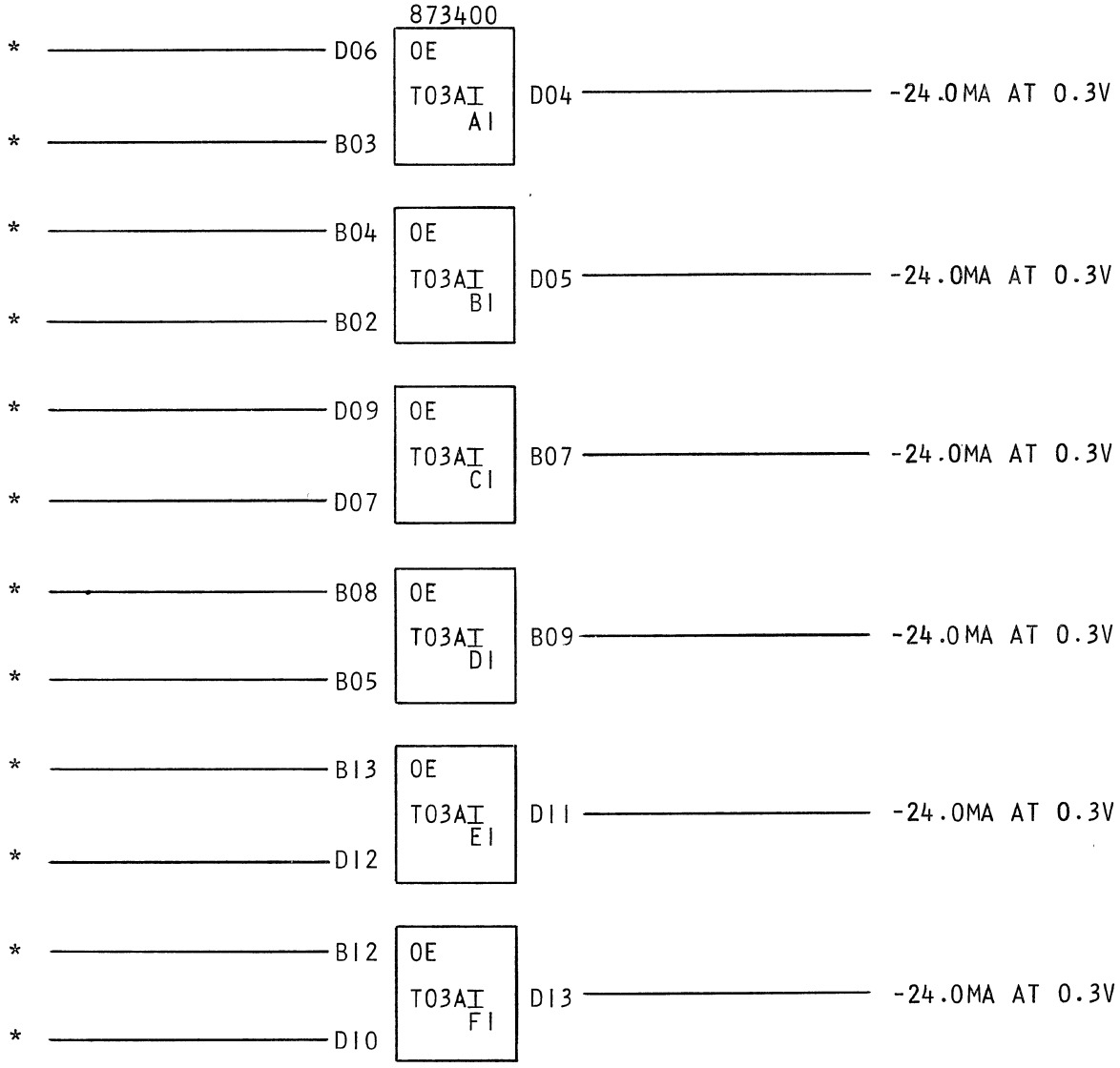
6-XOR

CATEGORY CODE

T03

P/N	5800428
EC	168225 B
STANDARD RESTRICTED	
CARD SIZE	1-6

873400

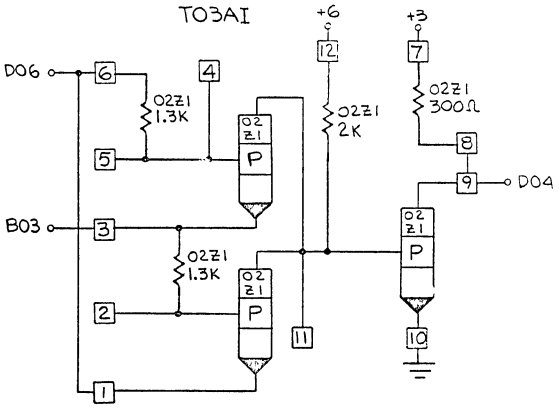


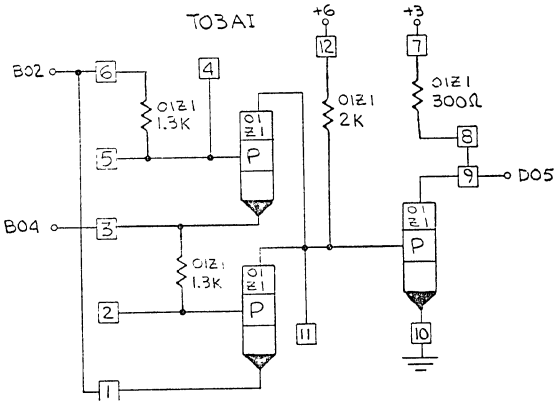
* SPECIAL DRIVE RULES SEE CIRCUIT SPEC 873400

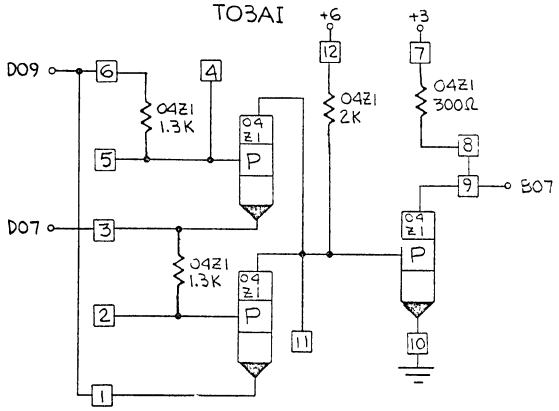
LMH Cat.	0-2860 Subject	245 Suffix

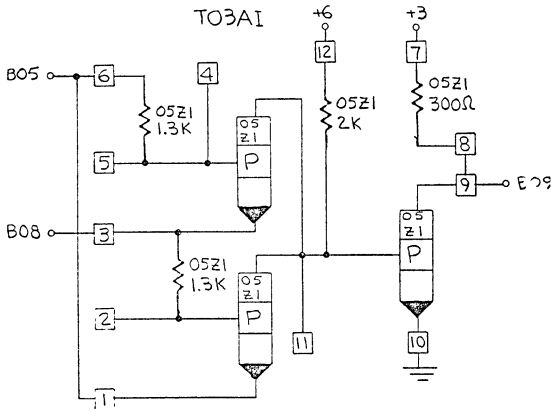
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6-XOR

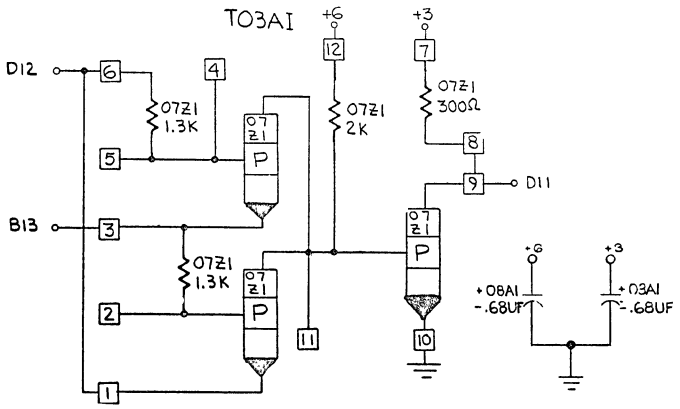
P/N	5800428
EC	168225B

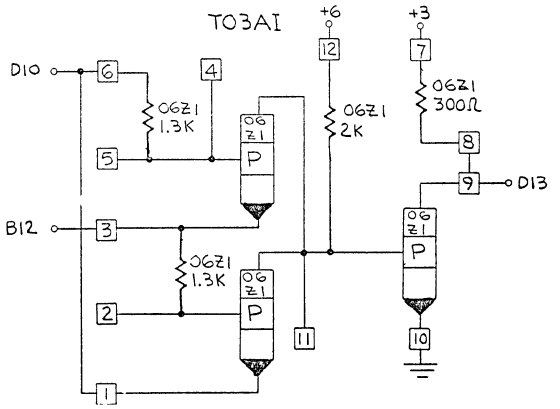












SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6-XOR LTH'S

LMH	0-2860	246
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
D08	GND

6-XOR LTH'S

CATEGORY CODE

T03

P/N	5800429
EC	163142
STANDARD RESTRICTED	
CARD SIZE	1-6

890985

DATA * — B03 ▷ *PH
CONTROL * — D04 — T03AK A1 — B02 — -24.0MA AT 0.3V

DATA * — B05 ▷ *PH
CONTROL * — D06 — T03AK B1 — D02 — -24.0MA AT 0.3V

DATA * — D10 ▷ *PH
CONTROL * — D05 — T03AK C1 — B07 — -24.0MA AT 0.3V

DATA * — B08 ▷ *PH
CONTROL * — D09 — T03AK D1 — D07 — -24.0MA AT 0.3V

DATA * — B12 ▷ *PH
CONTROL * — D13 — T03AK E1 — B09 — -24.0MA AT 0.3V

DATA * — B13 ▷ *PH
CONTROL * — D12 — T03AK F1 — B10 — -24.0MA AT 0.3V

*SPECIAL DRIVE RULES SEE CIRCUIT SPEC 890985

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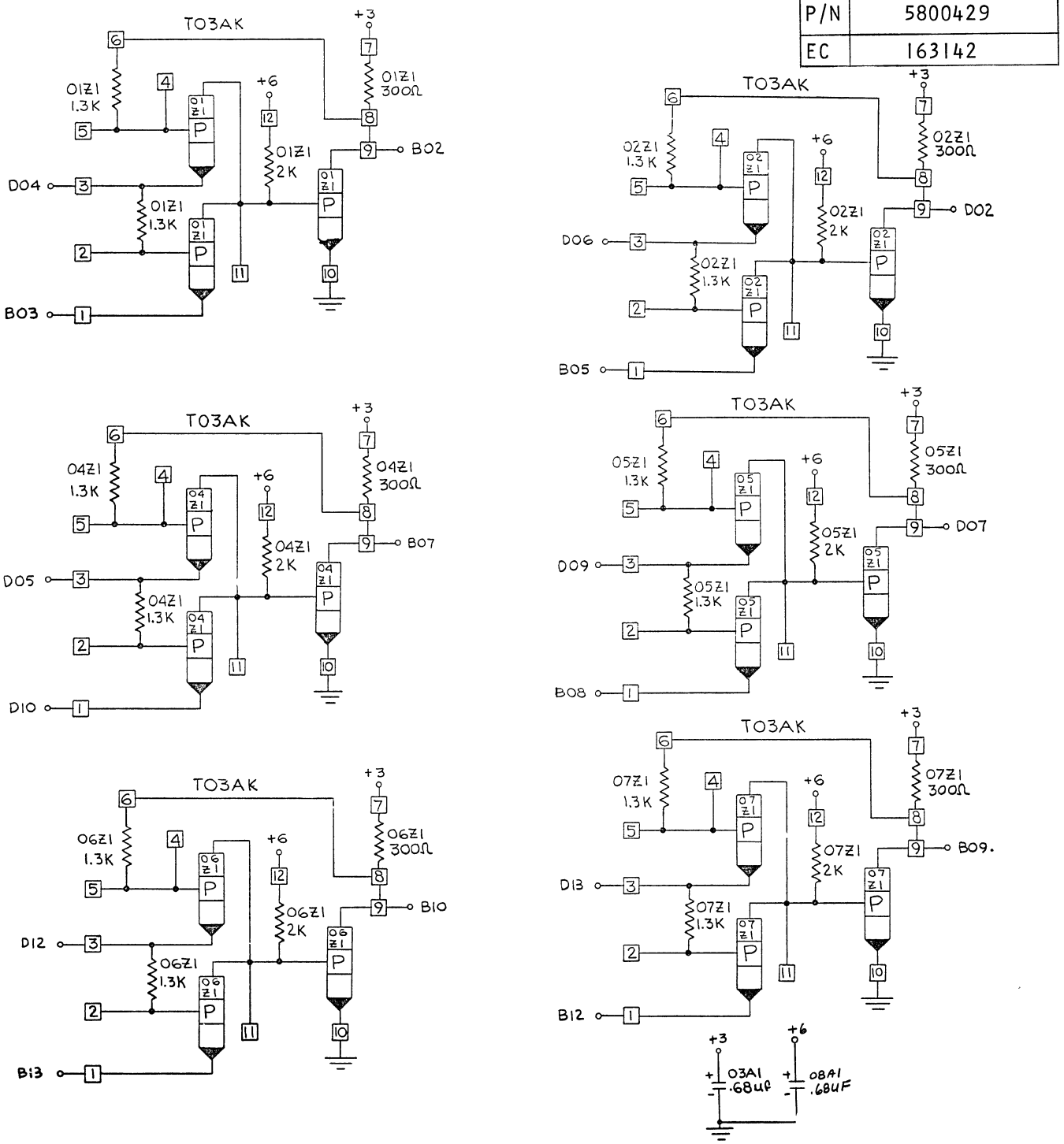
LMH Cat.	0-2860 Subject	246 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6-XOR LTH'S

P/N	5800429
EC	163142



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-2W,2W,2W,2W,2W AOI & 1-2W,2W,2W,2W AOI

LMH Cat.	0-2860 Subject	247 Suffix

IBM Location
Manufacturing Specification

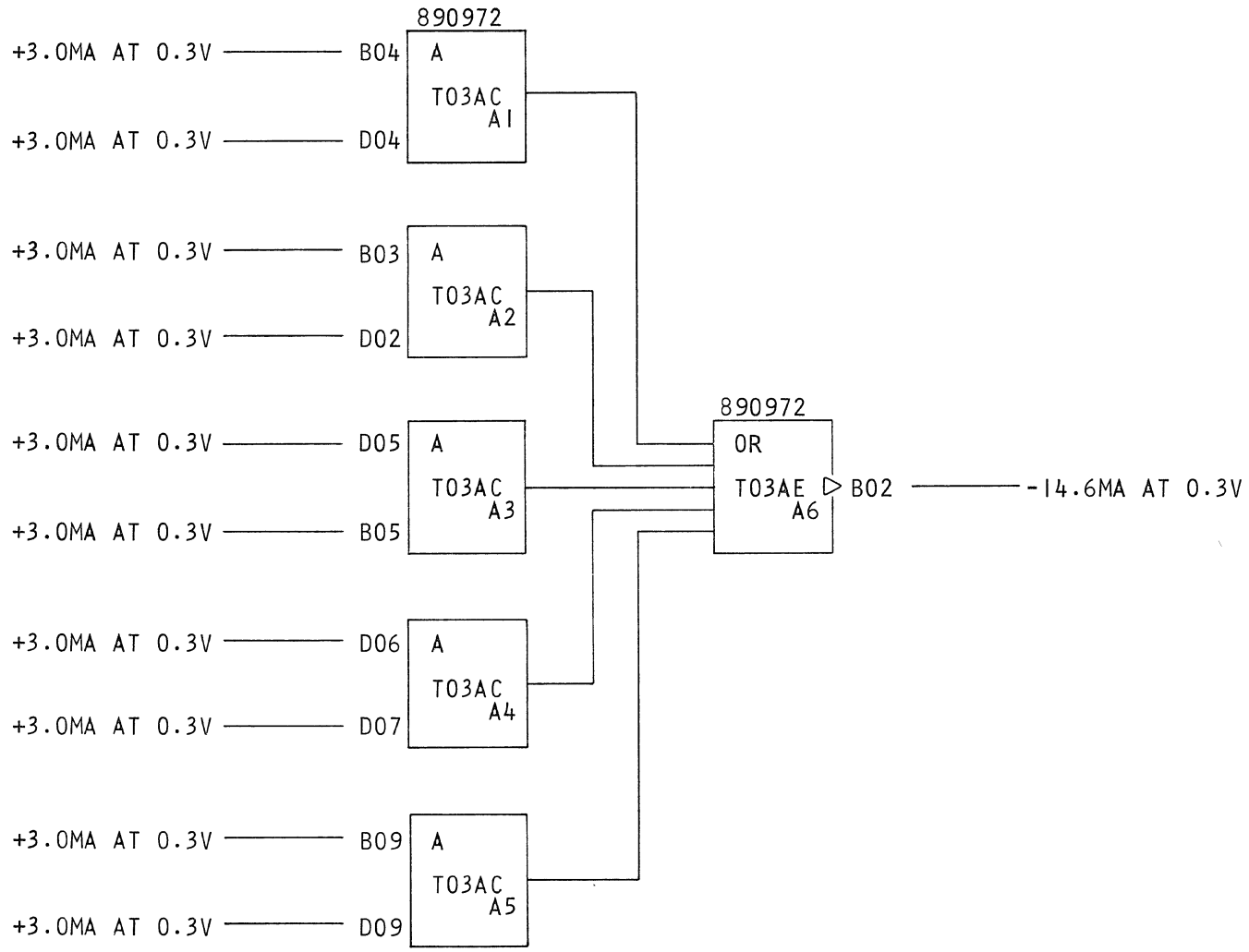
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1-2W,2W,2W,2W,2W AOI & 1-2W,2W,2W,2W AOI

CATEGORY CODE

T03

P/N	5800430
EC	166145 B
STANDARD RESTRICTED	
CARD SIZE	1-6

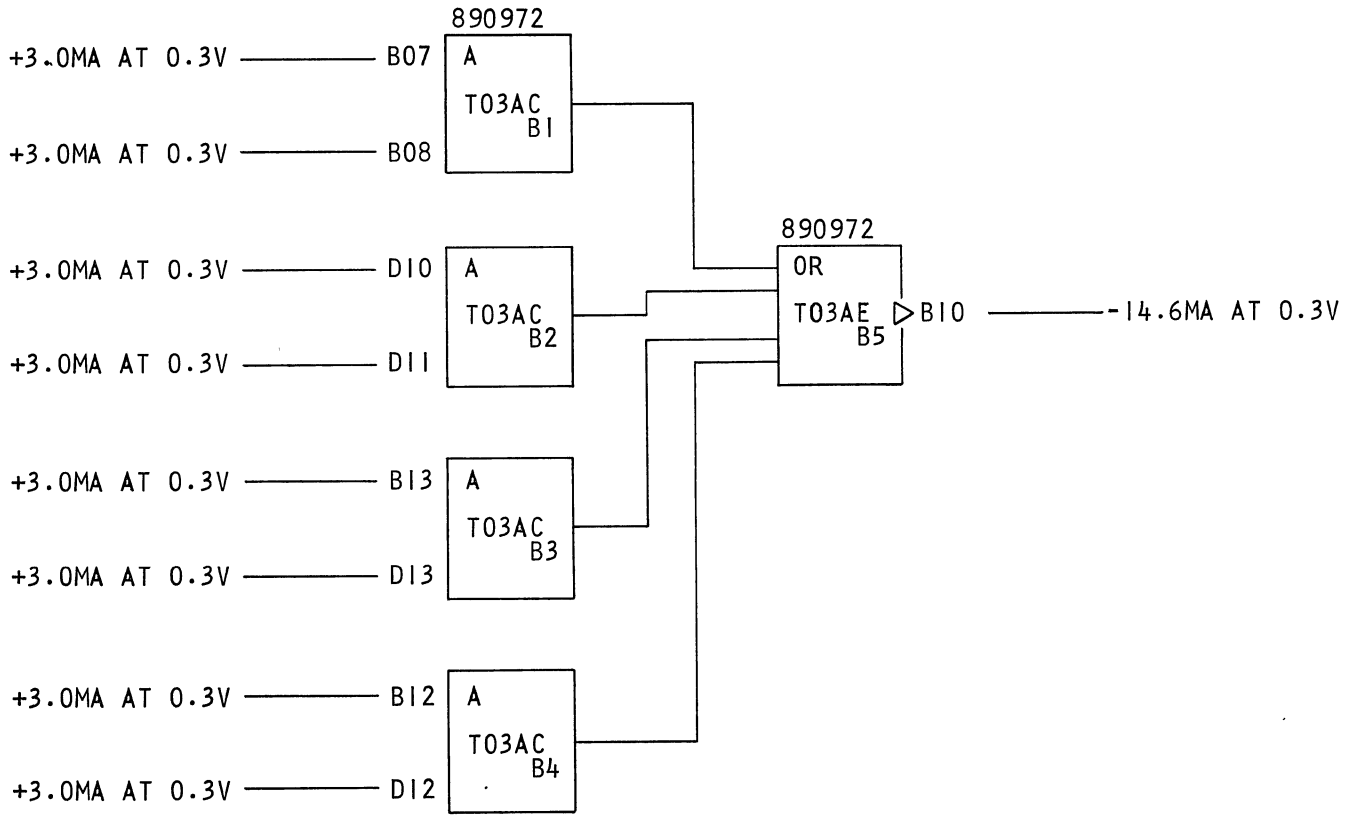


1-2W,2W,2W,2W,2W AOI & 1-2W,2W,2W,2W AOI

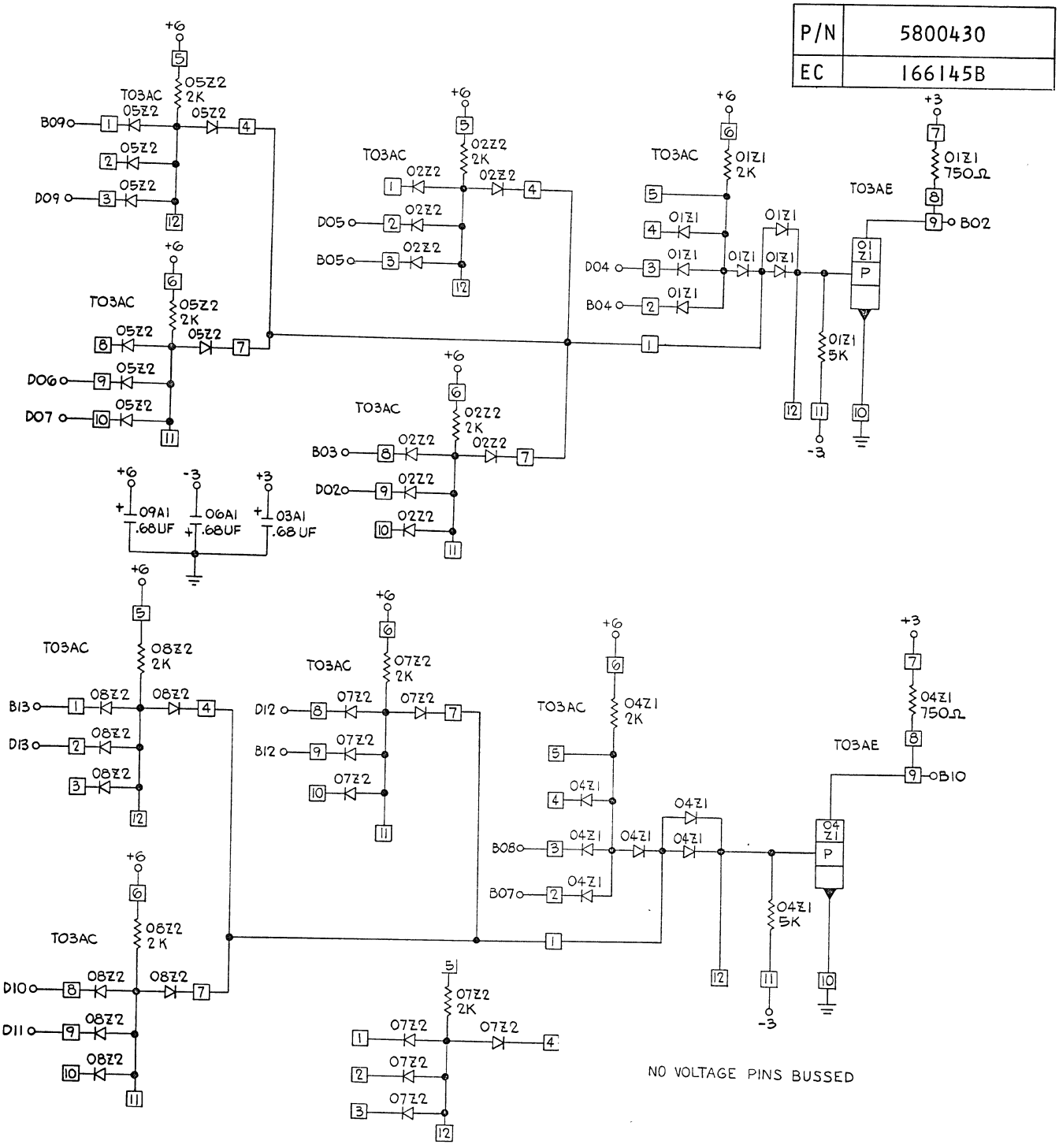
CATEGORY CODE

T03

P/N	5800430
EC	166145B



P/N	5800430
EC	166145B



IBM Location Manufacturing Specification

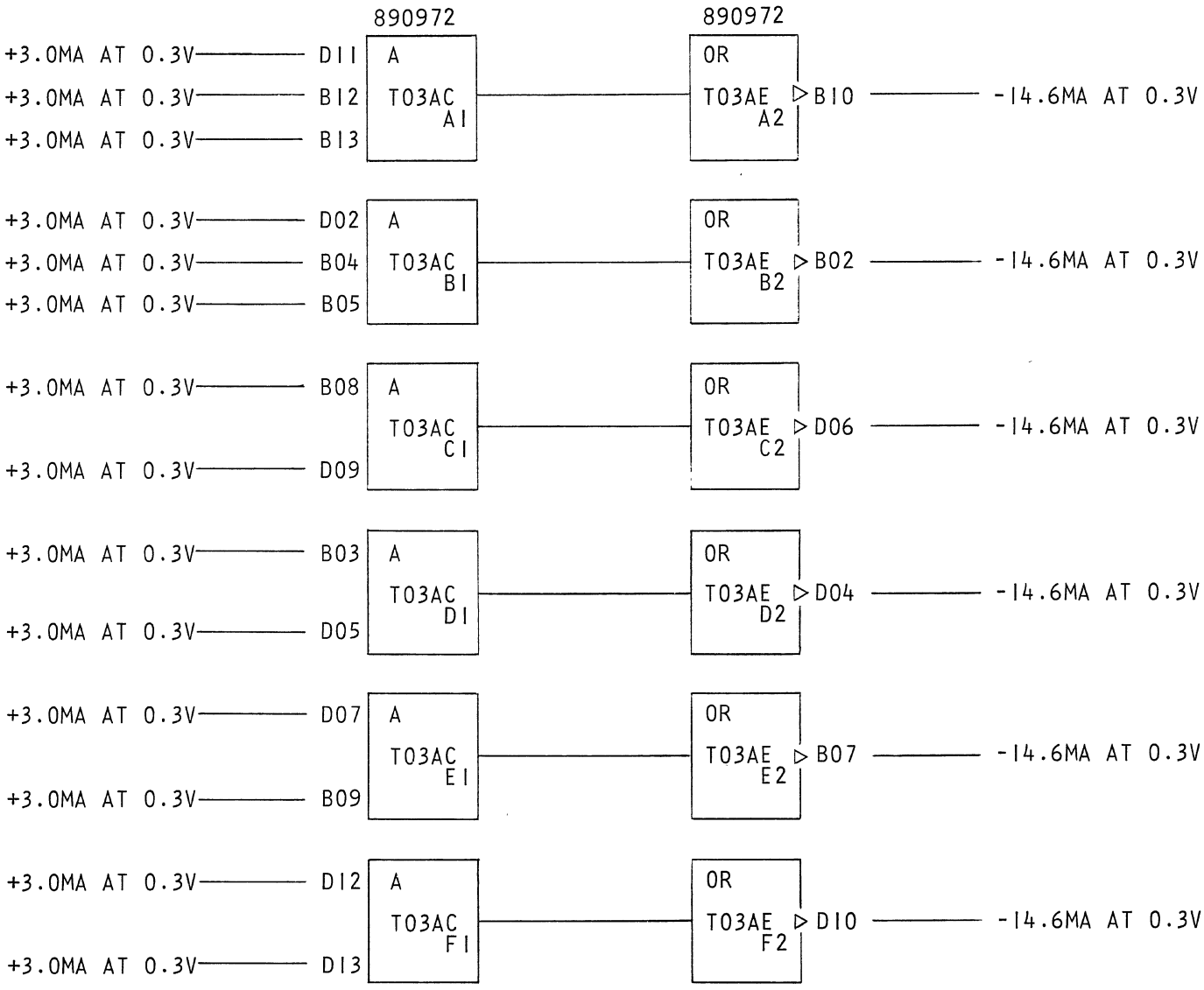
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2-3W AOI & 4-2W AOI

CATEGORY CODE

T03

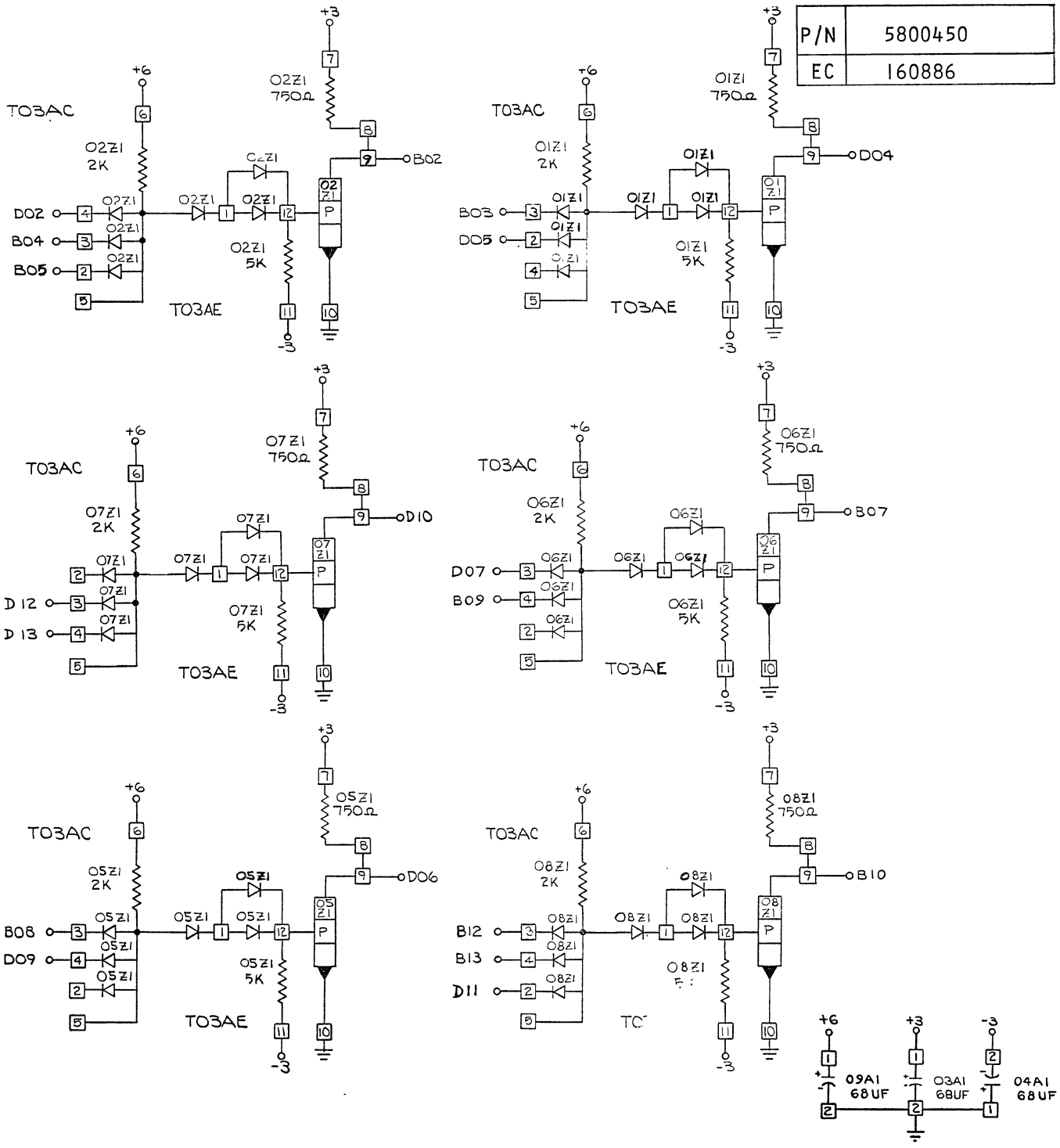
P/N	5800450
EC	160886
STANDARD RESTRICTED	
CARD SIZE	1-6



LMH Cat.	0-2860 Subject	249 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-3W AOI & 4-2W AOI

P/N	5800450
EC	160886



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-2W,2W,2W,2W,2W AOI"DOT OR" TO 1-2W,2W,2W,2W AOI

LMH	0-2860	250
Cat.	Subject	Suffix

IBM

Location
Manufacturing Specification

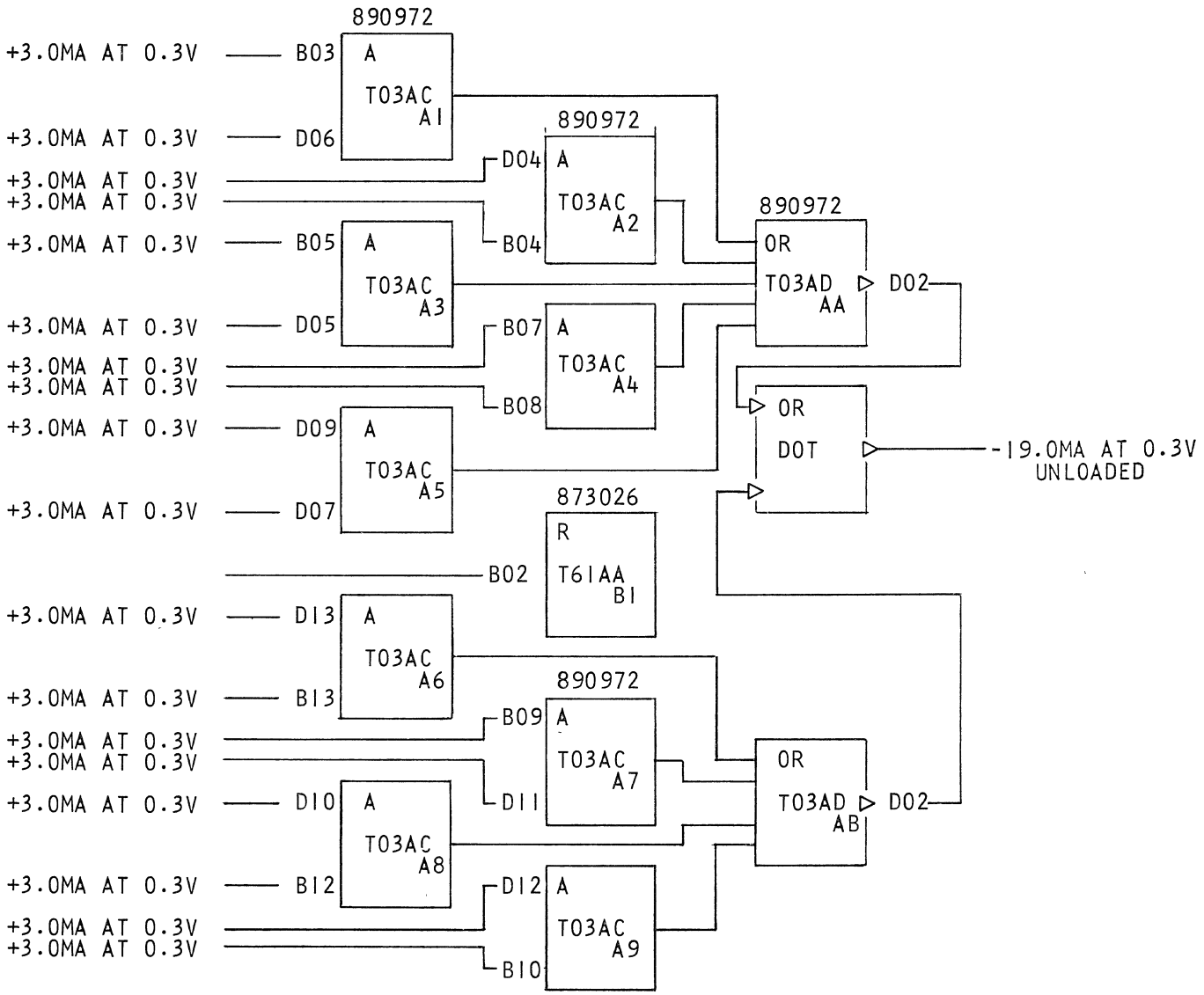
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1-2W,2W,2W,2W,2W AOI"DOT OR" TO 1-2W,2W,2W,2W AOI

CATEGORY CODE

T03

P/N	5800455
EC	163477
STANDARD	ACTIVE
CARD SIZE	1-6



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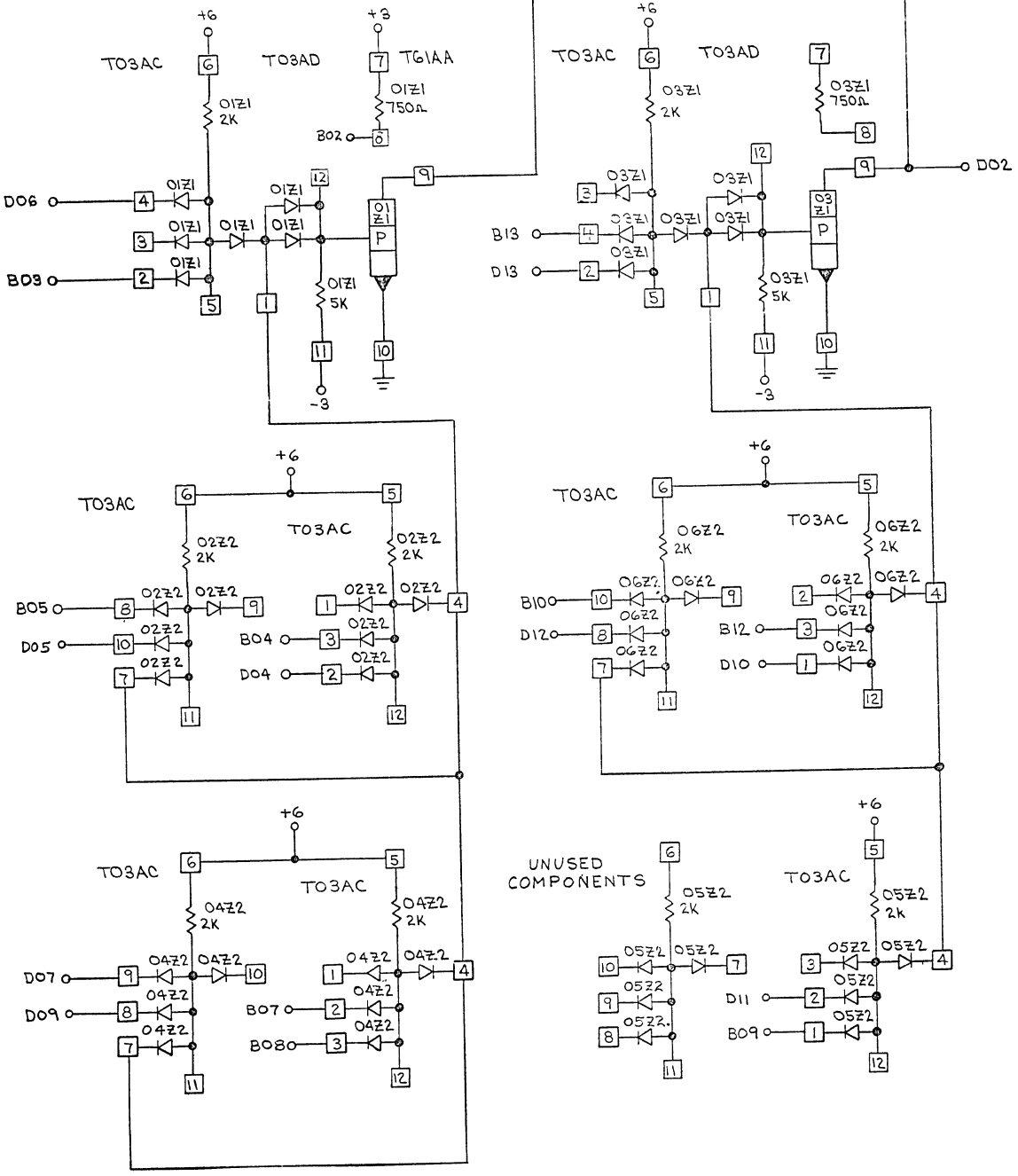
LMH Cat.	0-2860 Subject	250 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-2W, 2W, 2W, 2W, 2W AOI "DOT OR" TO 1-2W, 2W, 2W, 2W AOI

P/N	5800455
EC	163477



Page 2	Date 1-67

IBM Location Manufacturing Specification

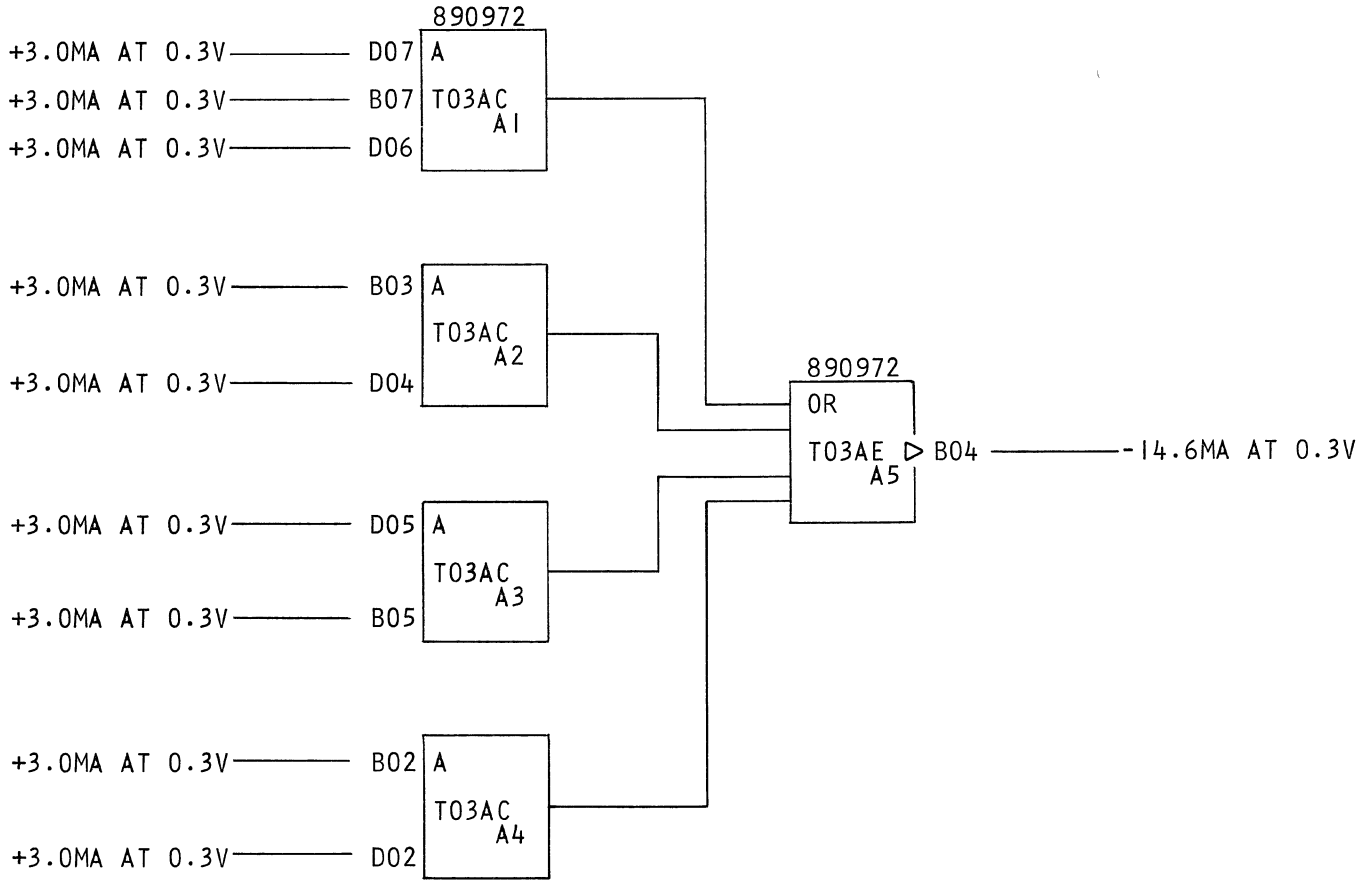
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2-3W, 2W, 2W, 2W AOI

CATEGORY CODE

T03

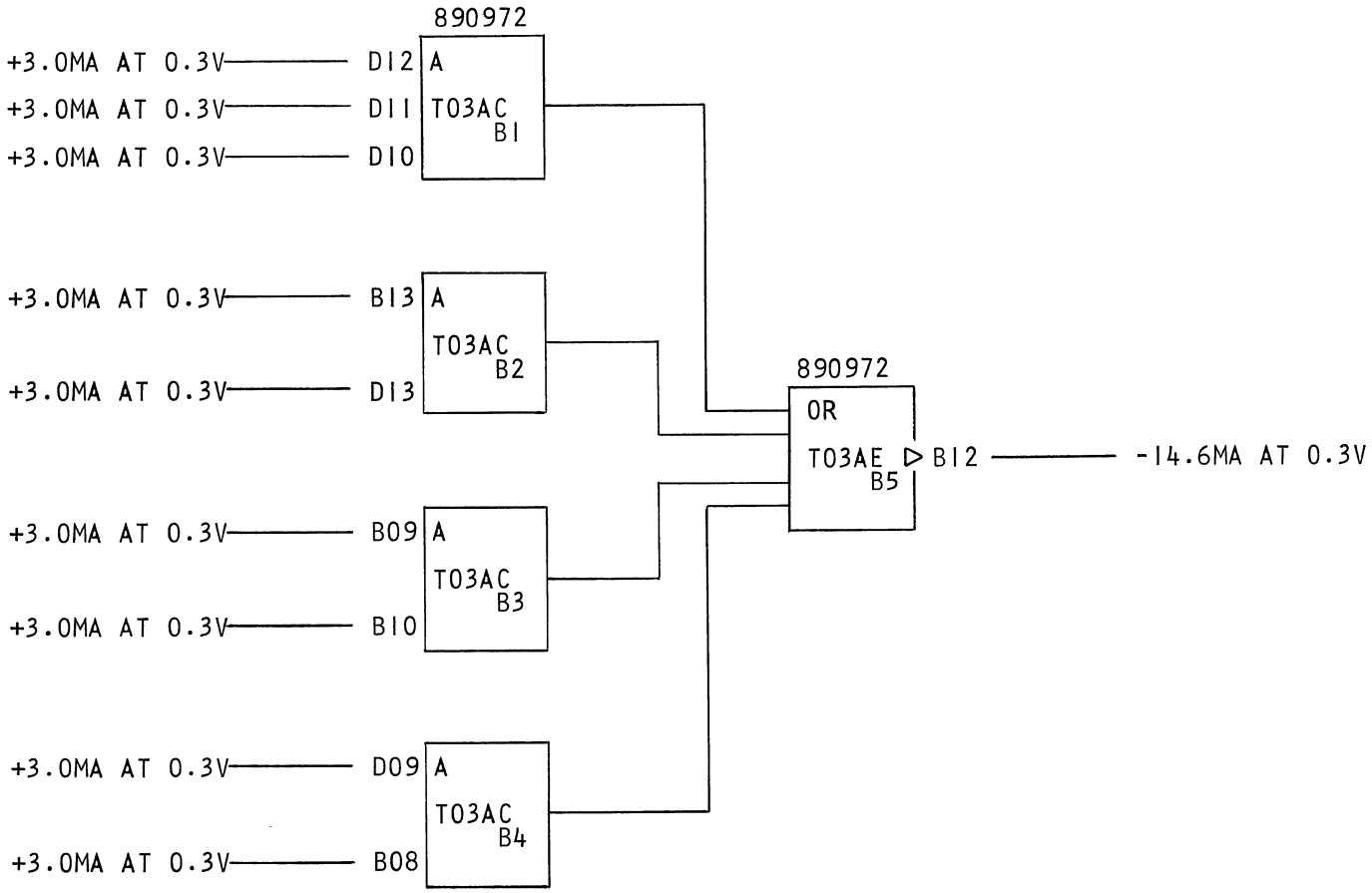
P/N	5800489
EC	160176
STANDARD RESTRICTED	
CARD SIZE	1-6



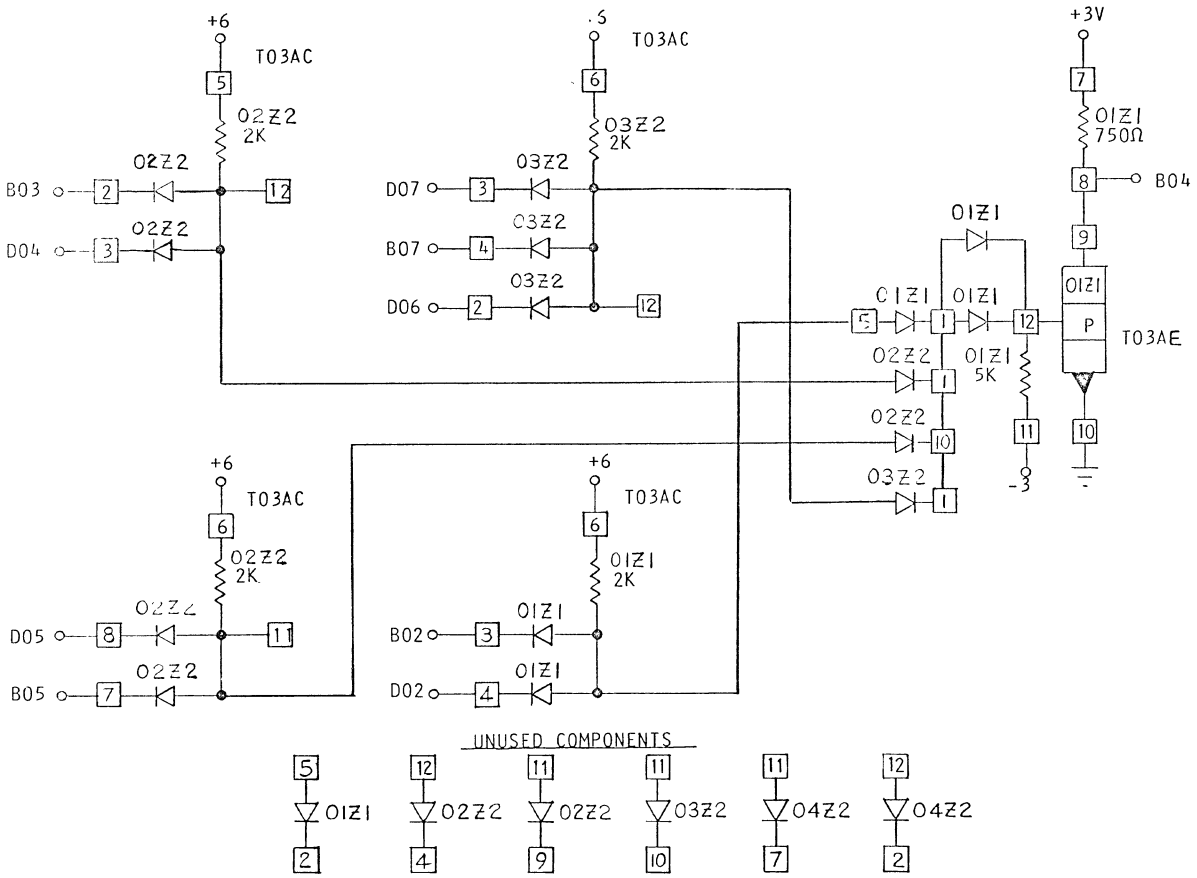
2-3W, 2W, 2W, 2W AOI

T03

P/N	5800489
EC	160176



P/N	5800489
EC	160176



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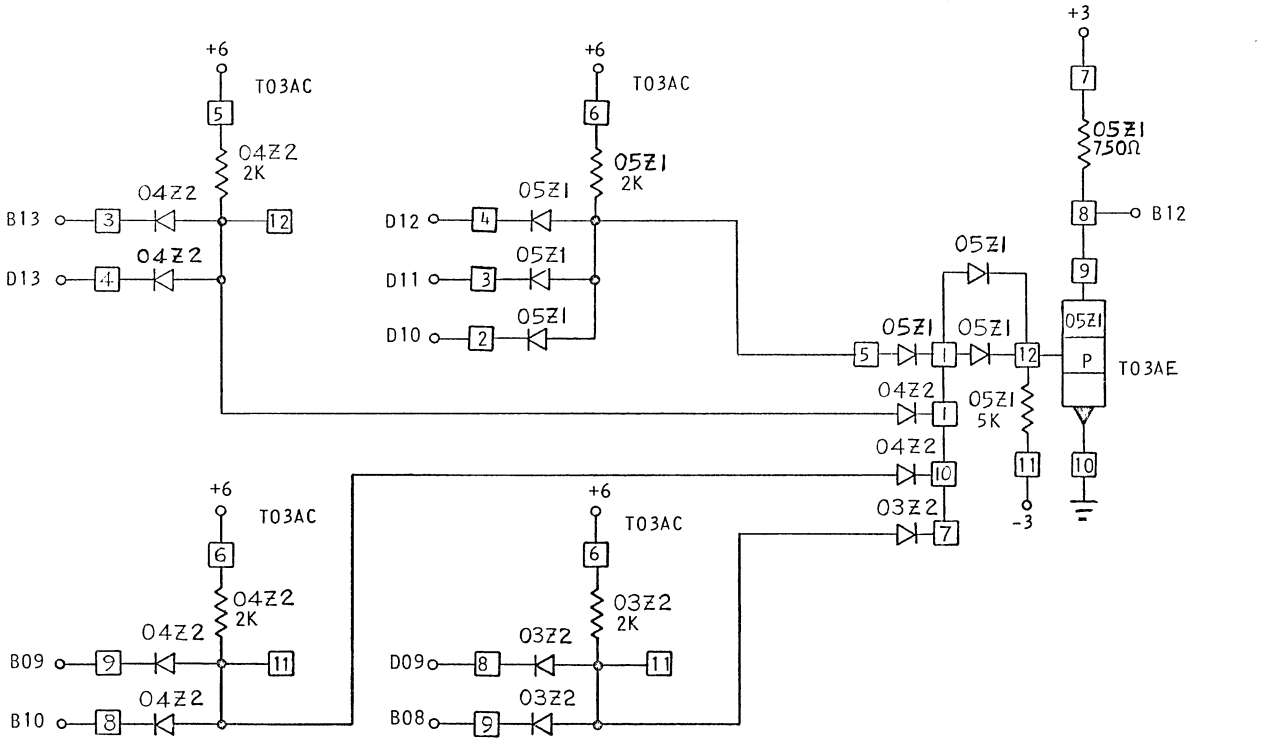
EC	160176



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINERING
10 LINE SENSE AMPLIFIERS

LMH Cat.	0-2860 Subject	252 Suffix

IBM Location Manufacturing Specification

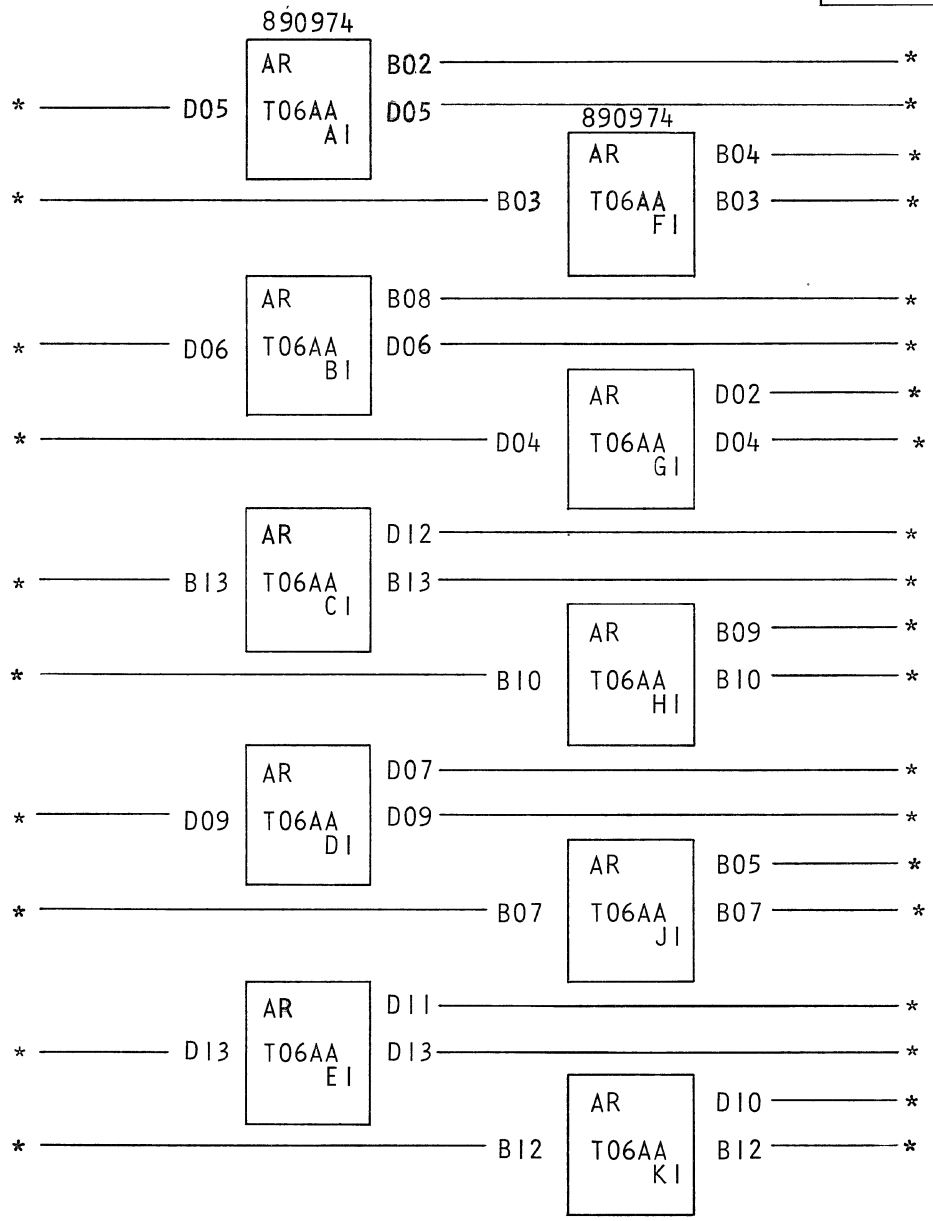
POWER REQUIRED	
PIN	VOLTS
B11	+6
D08	GND

10 LINE SENSE AMPLIFIERS

CATEGORY CODE

T06

P/N	5800494
EC	166610
STANDARD RESTRICTED	
CARD SIZE	1-6



* SEE SPEC 890974 FOR SPECIAL DRIVING AND LOADING INFORMATION.

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
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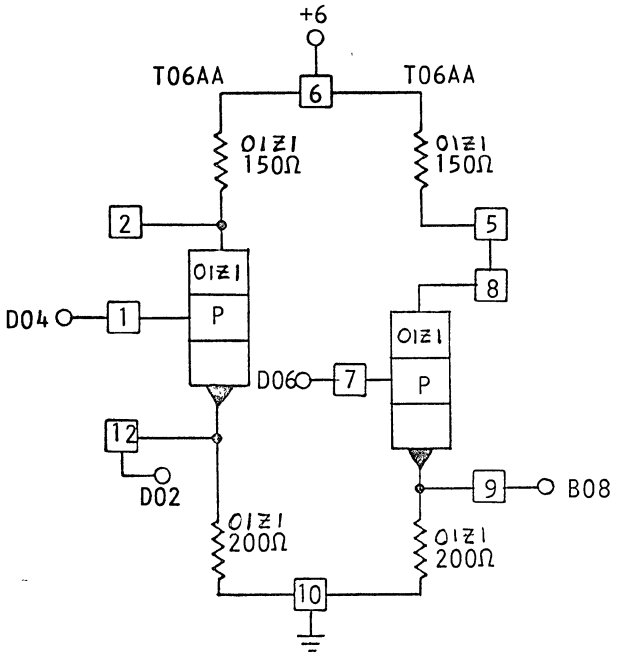
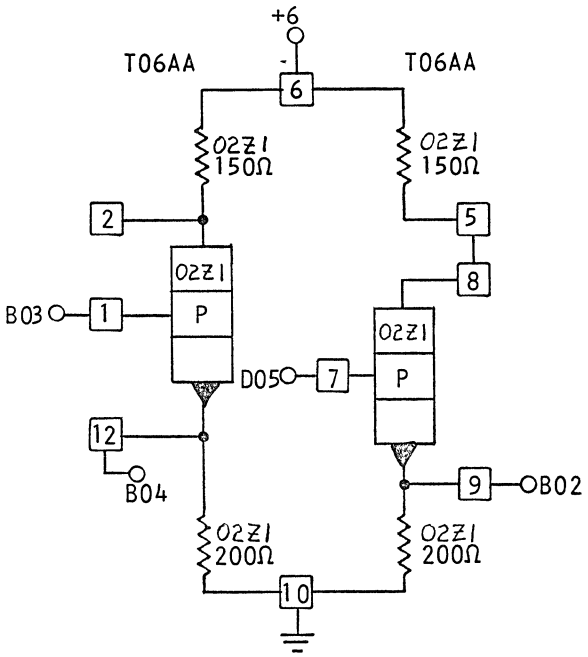
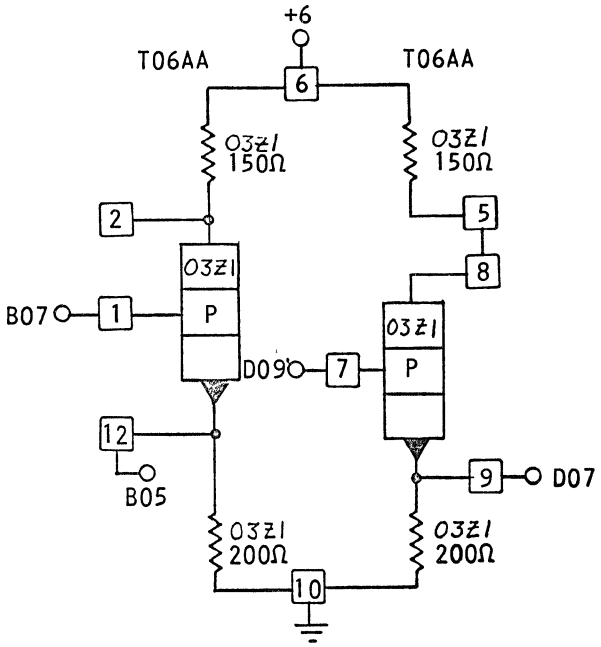
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
IO LINE SENSE AMPLIFIERS

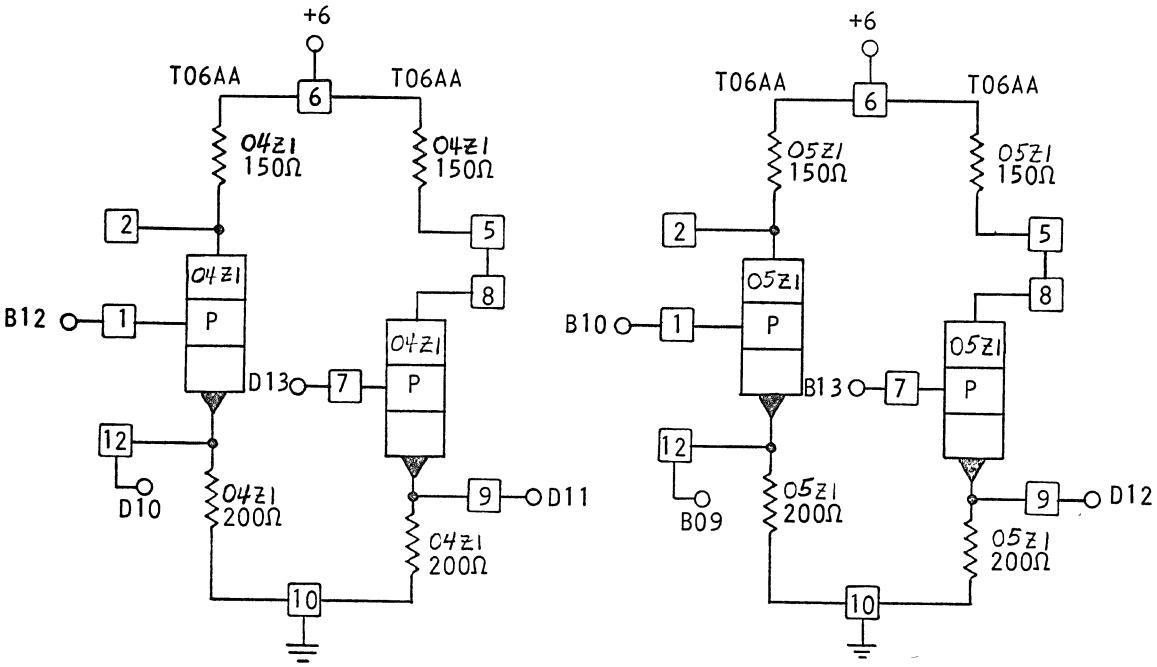
P/N	5800494
EC	166610







P/N	5800494
EC	166610



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
10 INVERTERS

LMH Cat.	0-2860 Subject	253 Suffix

IBM **Location**
Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
D03	+3
D08	GND

10 INVERTERS

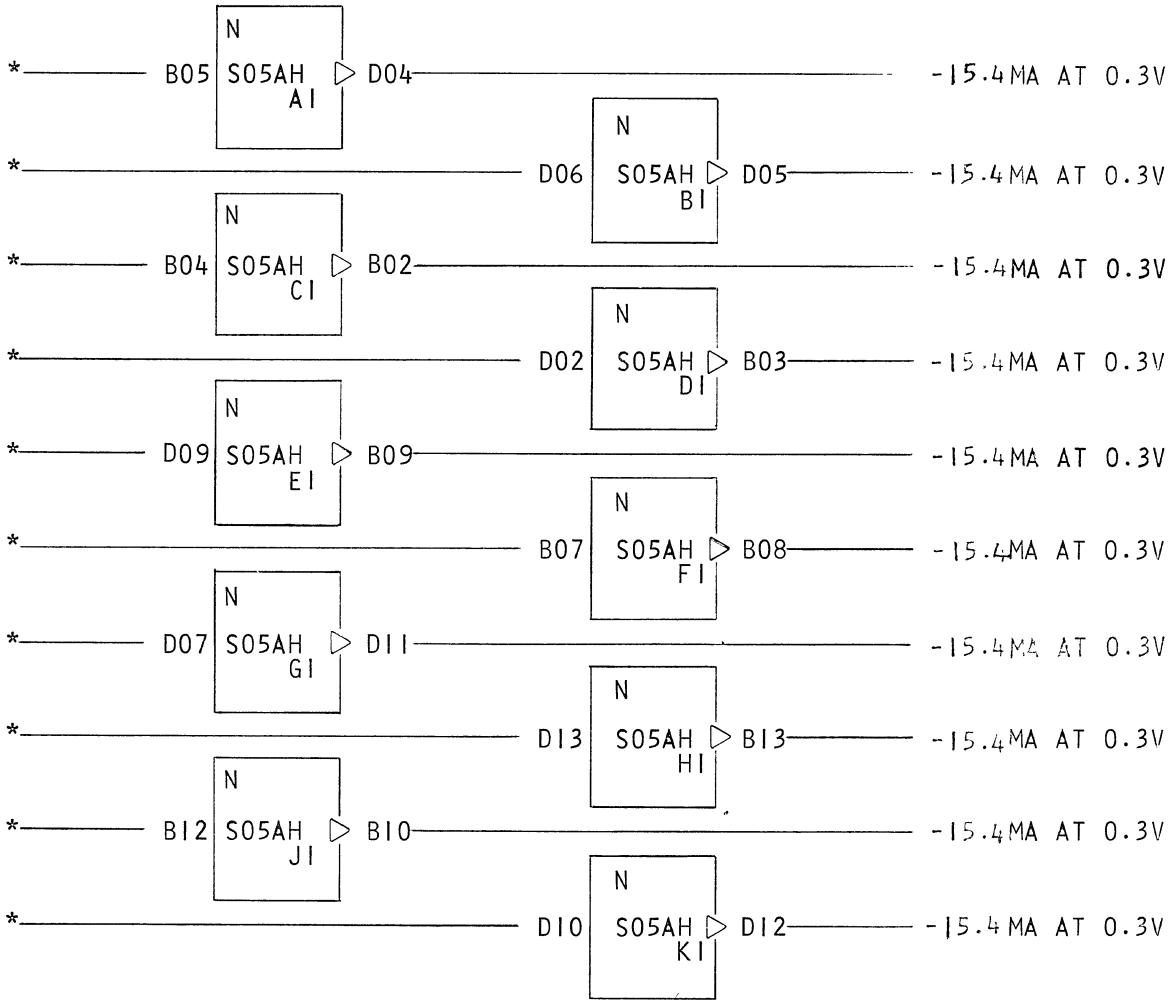
CATEGORY CODE

S05

P/N	5800509	
EC	160184	
STANDARD RESTRICTED		
CARD SIZE		1-6

T03AB = 5803421
T03AF = 5803447
S05AH = 5803457
TOPINT = 5803686

873409



*SPECIAL DRIVE RULE SEE SPEC 873409

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Applicability ENDICOTT		ENDICOTT Responsibility	1-67 Date	1 OF 2 Page

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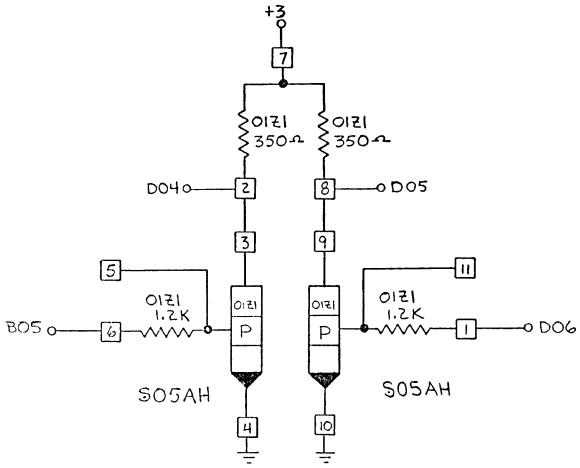
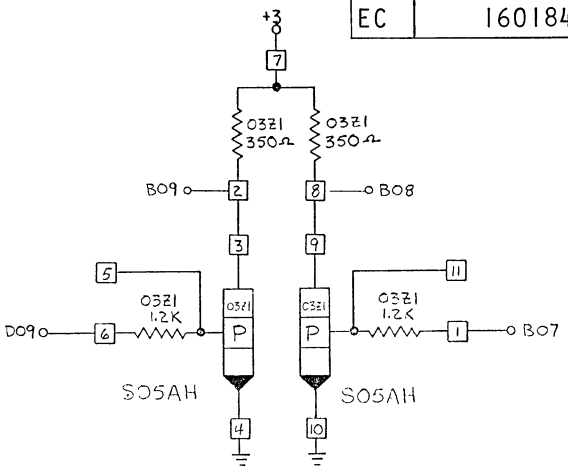
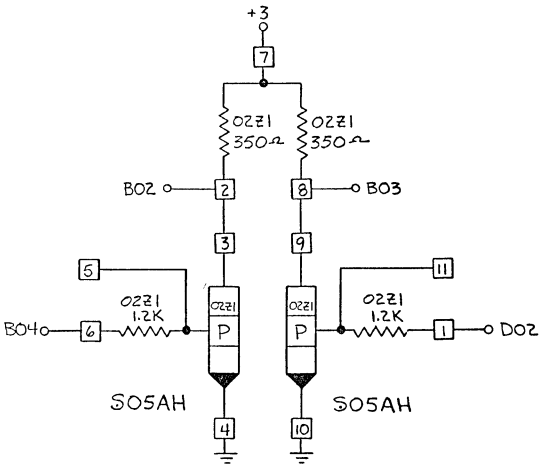
LMH Cat.	0-2860 Subject	253 Suffix

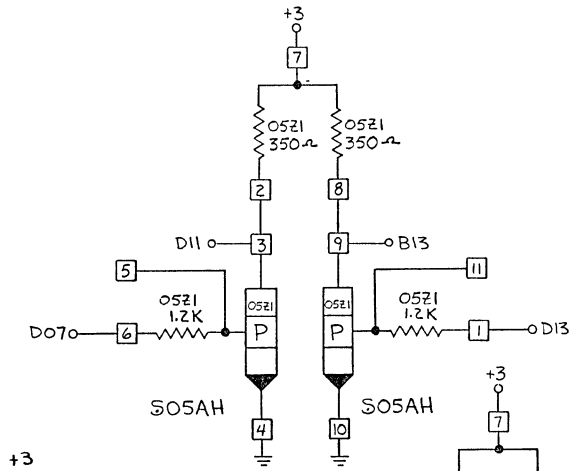
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
10 INVERTERS

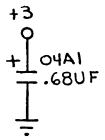
P/N	5800509
EC	160184

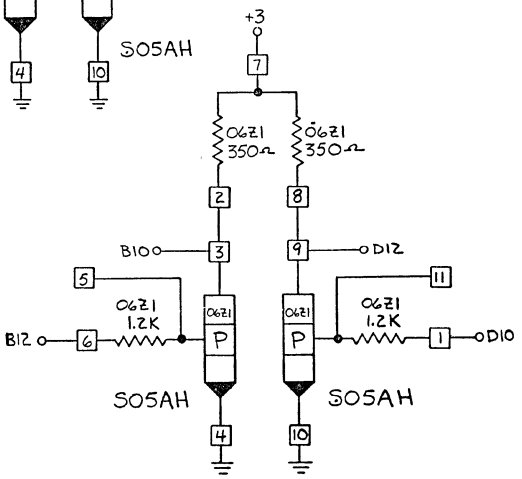












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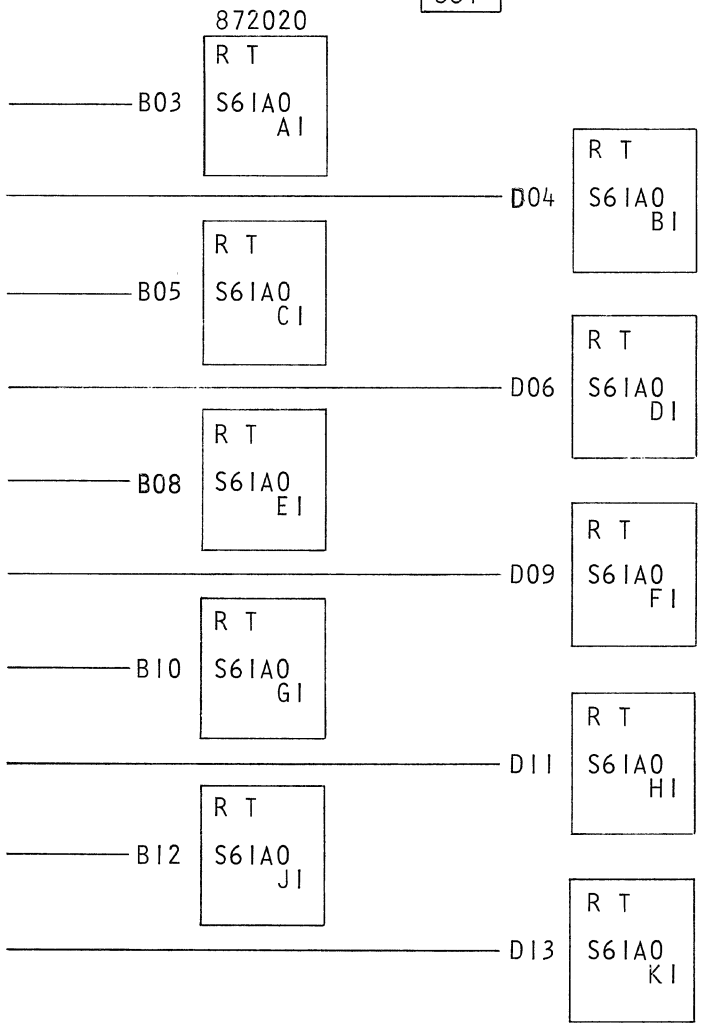
POWER REQUIRED	
PIN	VOLTS
D03	+3
D08	GND

10-95 OHM MULTIPLEX
TERMINATING RESISTORS TO +3V

CATEGORY CODE

S61

P/N	5800536
EC	160203
STANDARD RESTRICTED	
CARD SIZE	1-6

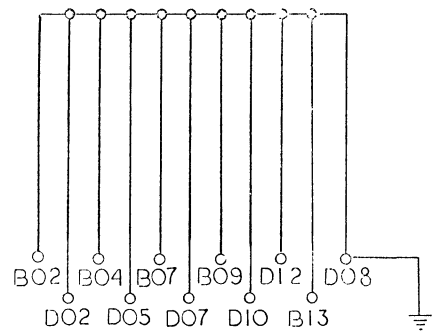


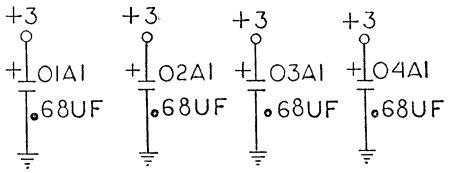
NOTE: ALL RESISTORS ±5% WITH A MAXIMUM LOAD OF 31.6MA AT 0.3V

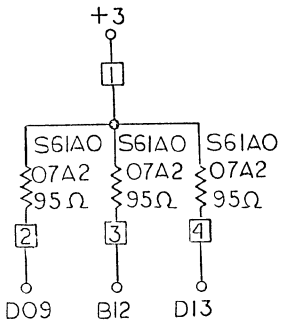
LMH Cat.	0-2860 Subject	254 Suffix

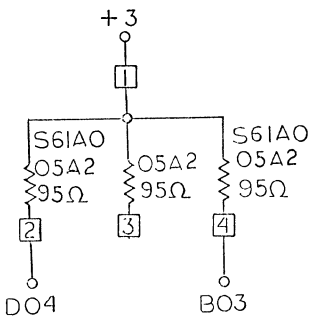
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
10-95 OHM MULTIPLEX TERMINATING RESISTORS TO +3V

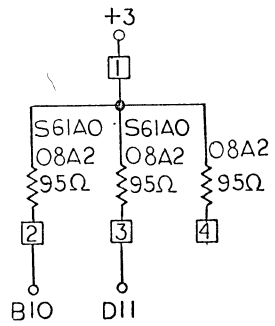
P/N	5800536
EC	160203

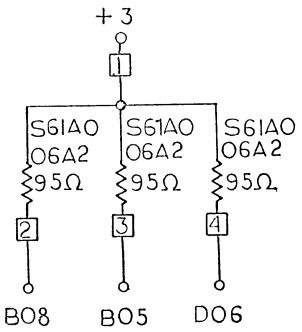












IBM

Location

Manufacturing Specification

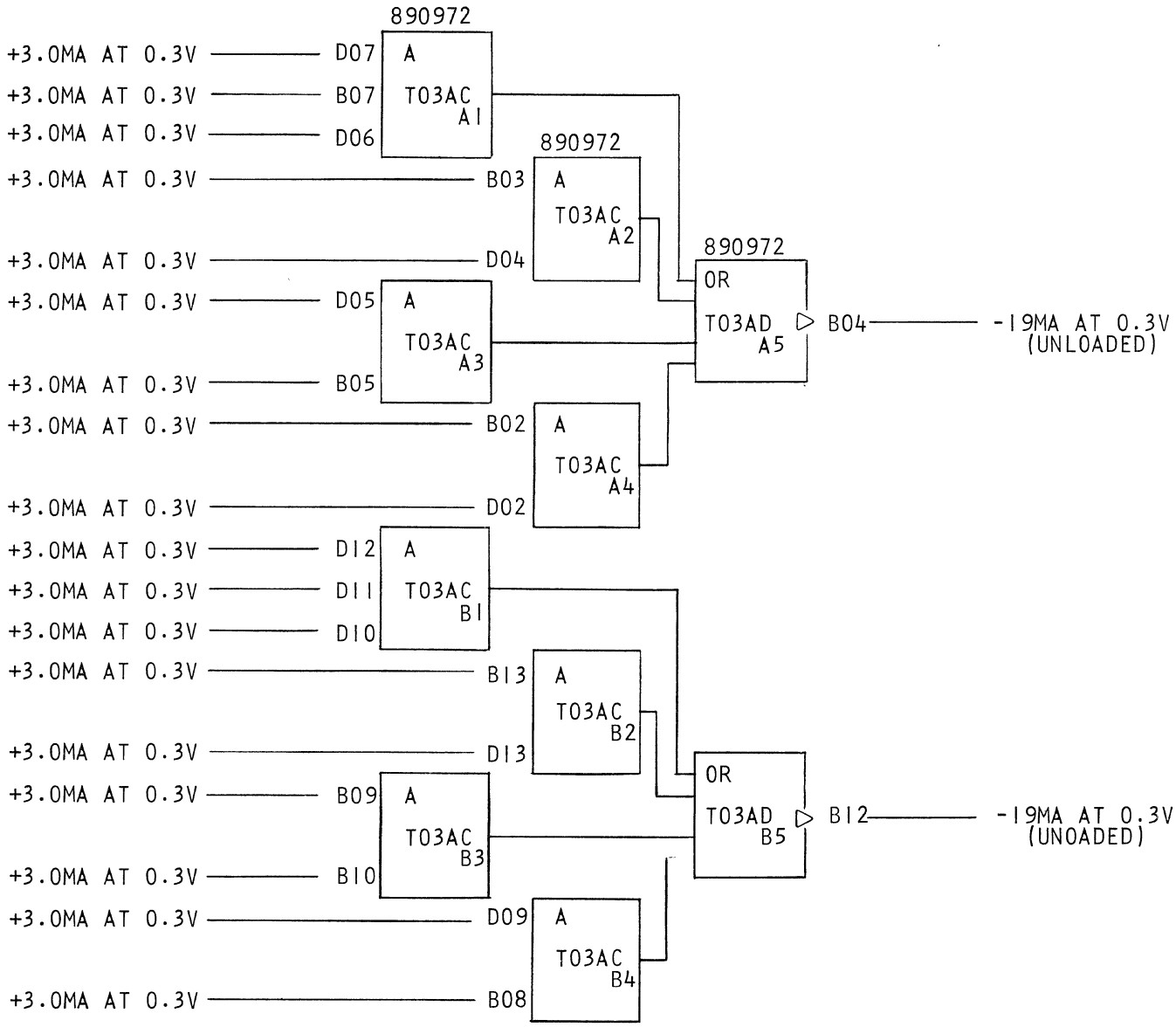
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2-3W, 2W, 2W, 2W AOI WO/L

CATEGORY CODE

T03

P/N	5800546
EC	163799
STANDARD RESTRICTED	
CARD SIZE	1-6



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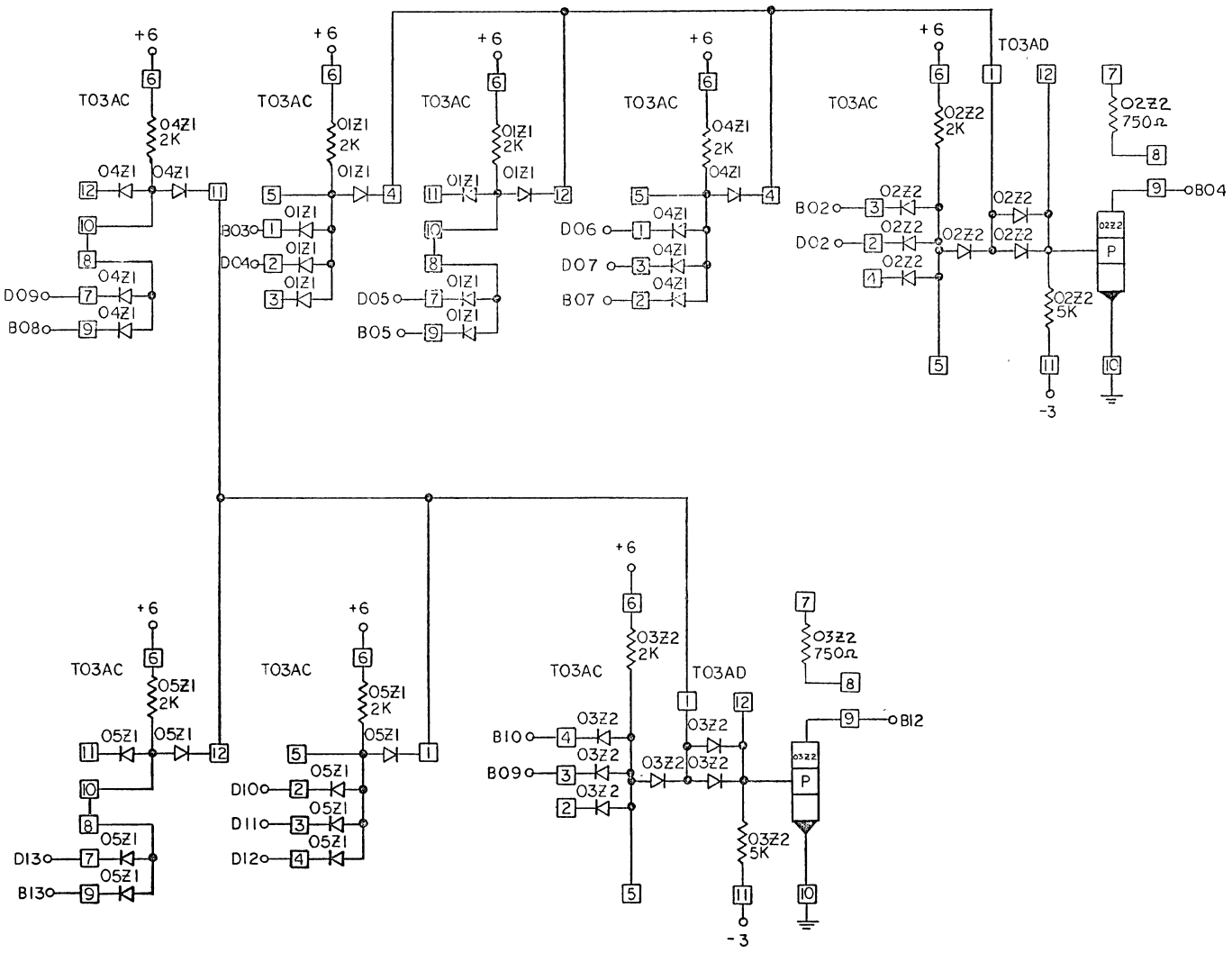
LMH Cat.	0-2860 Subject	255 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-3W, 2W, 2W, 2W AOI W0/L

P/N	5800546
EC	163799



Page 2	Date 1-67

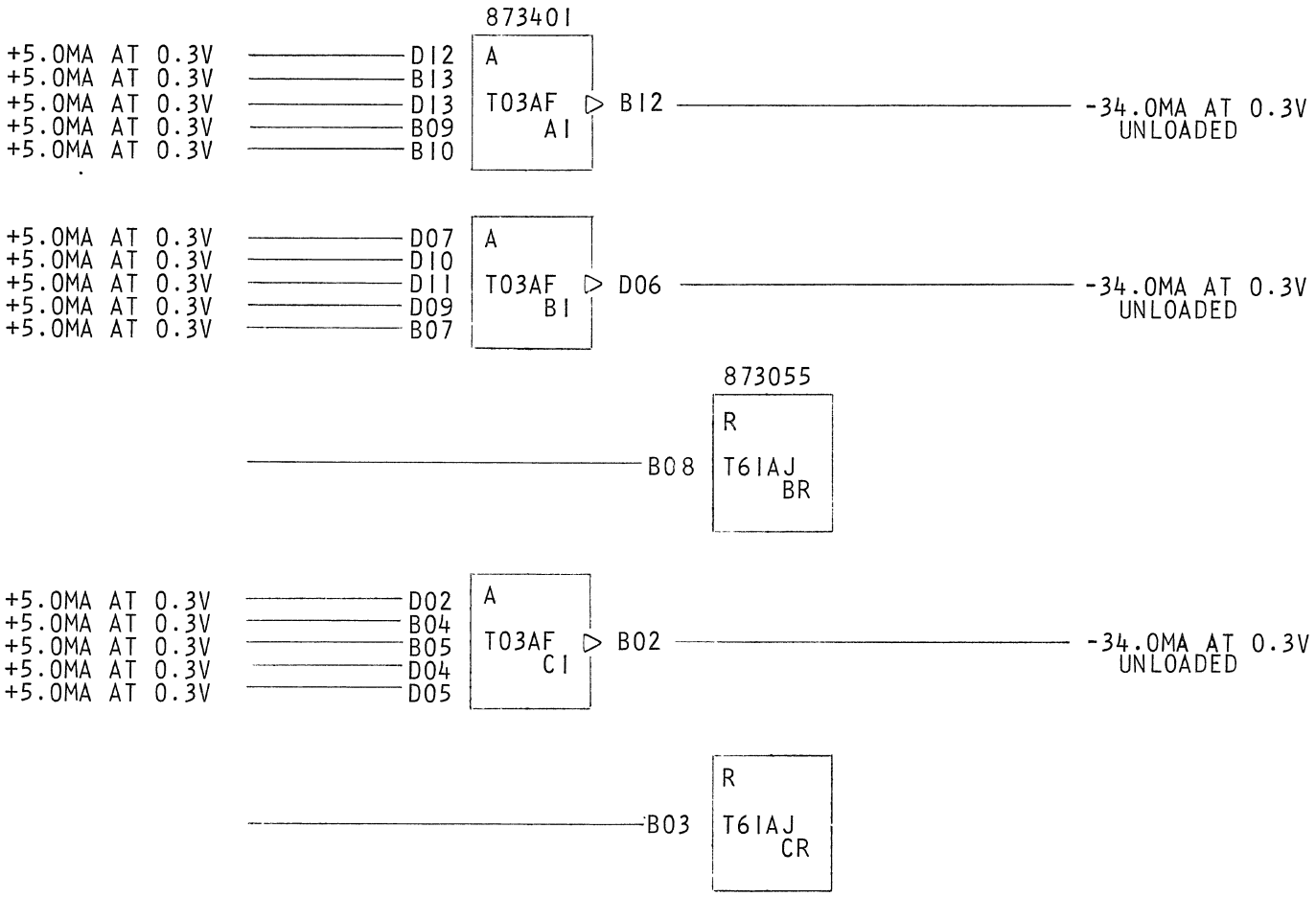
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1-5 API WO/L & 2-5W API WO/L & 2 PRGM RESISTOR

CATEGORY CODE

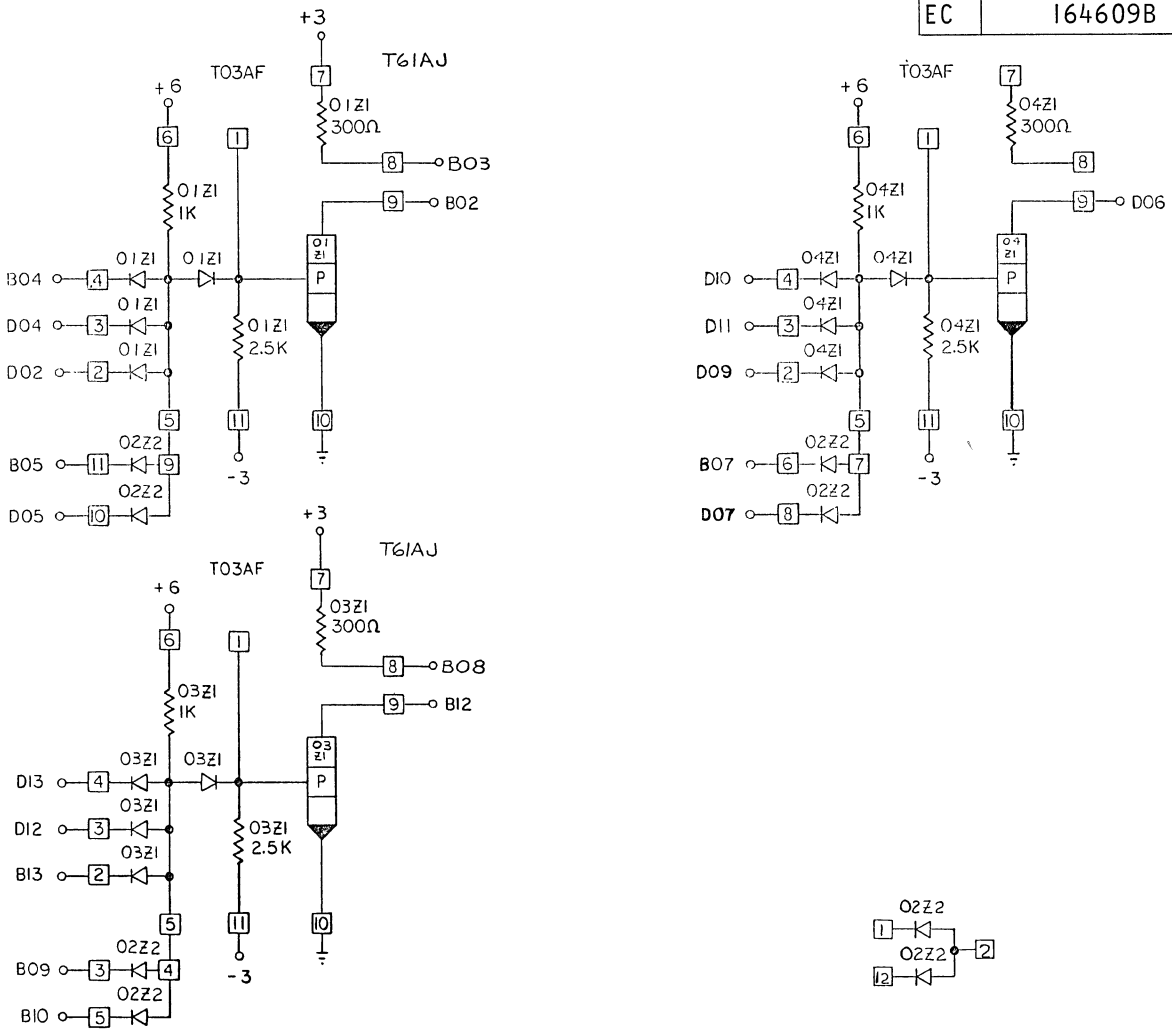
T03

P/N	5800612
EC	164609B
STANDARD RESTRICTED	
CARD SIZE	1-6



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-5W API W0/L & 2-5W API W0/L & 2 PRGM RESISTORS

P/N	5800612
EC	164609B



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
3-5W AINV INV

LMH	0-2860	261
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

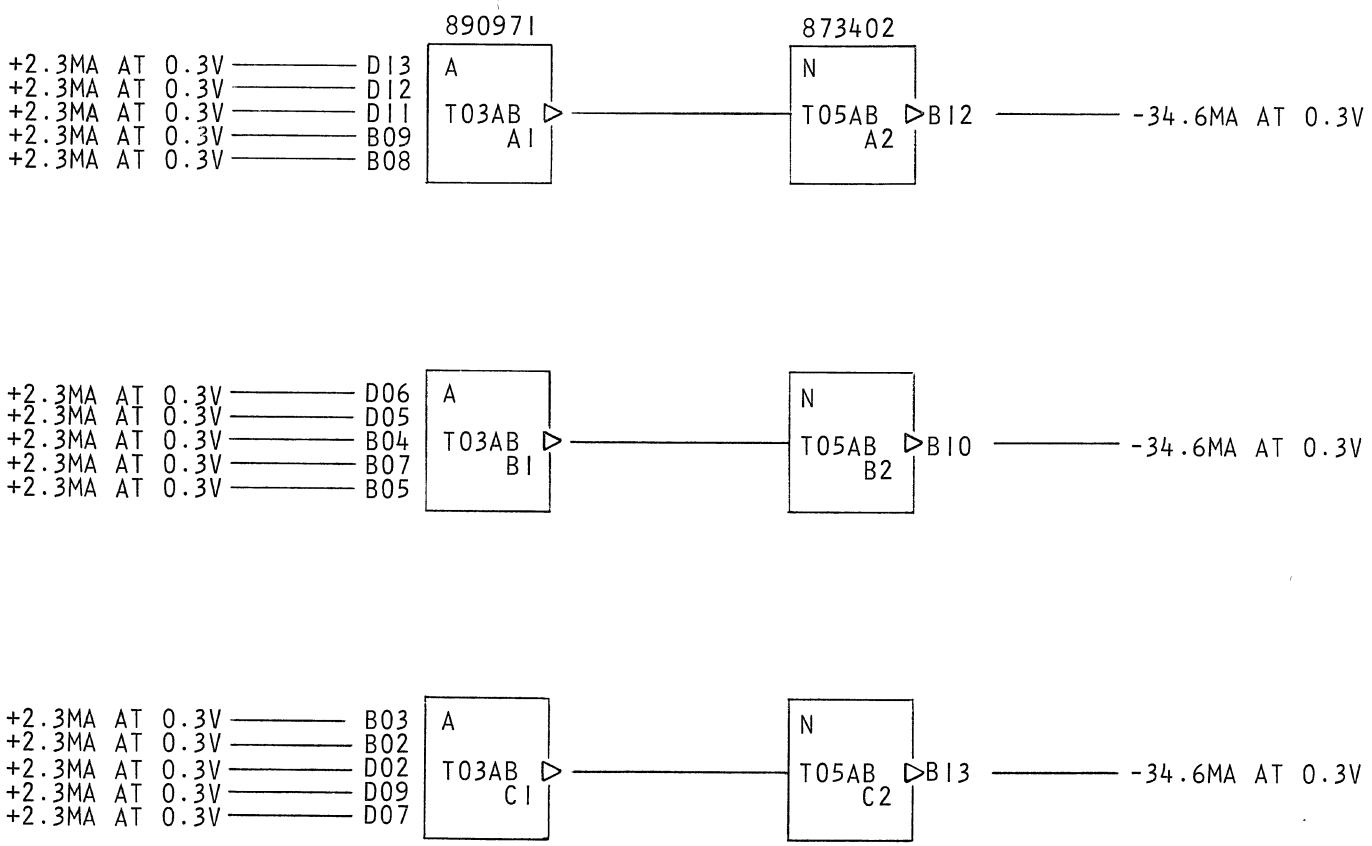
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

3-5W AINV INV

CATEGORY CODE

T03, T05

P/N	5800716	
EC	164694A	
STANDARD RESTRICTED		
CARD SIZE		1-6



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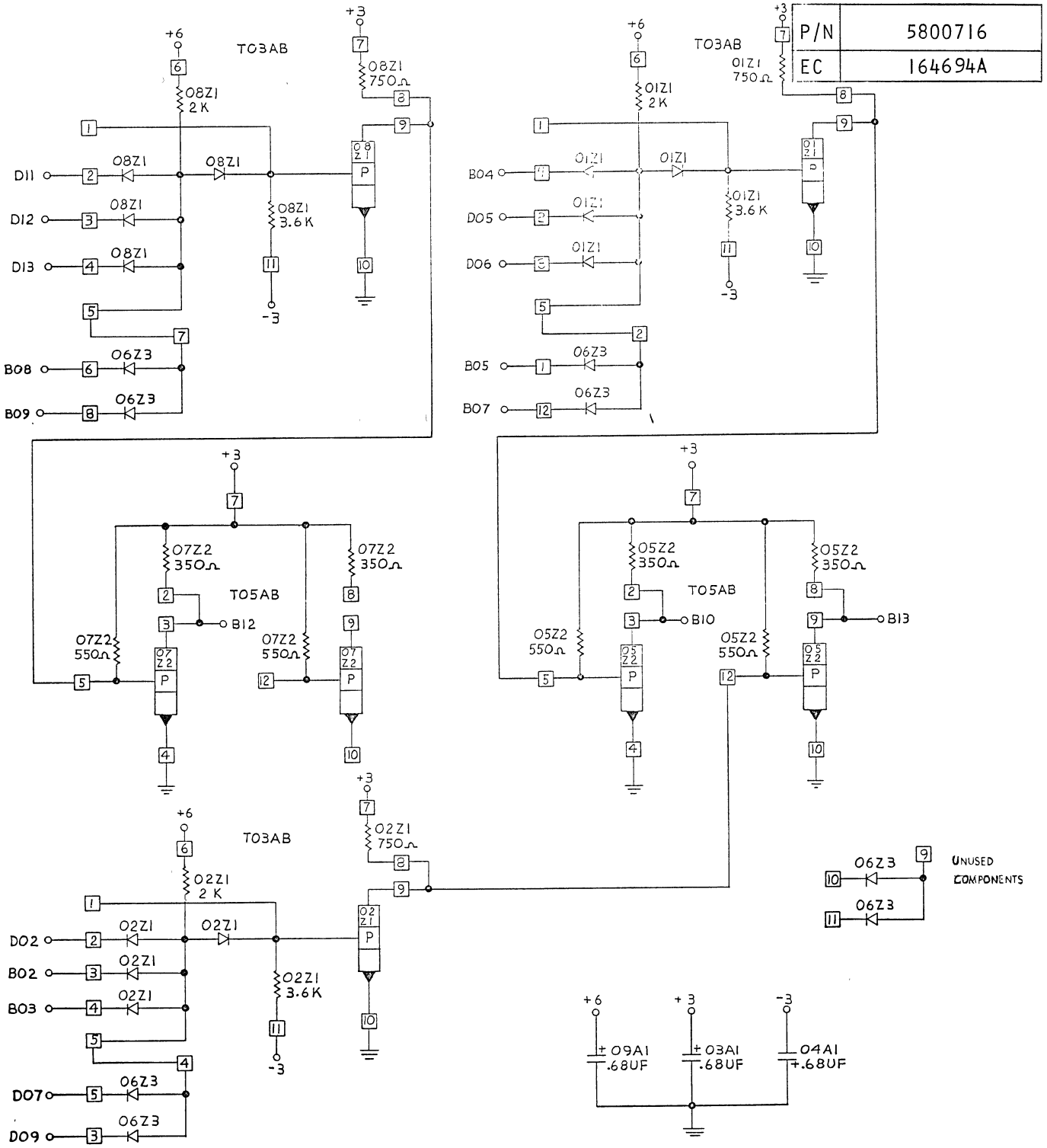
LMH Cat.	0-2860 Subject	261 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 3-5W AINV INV

P/N	5800716
EC	164694A



2 OF 2 Page	1-67 Date	

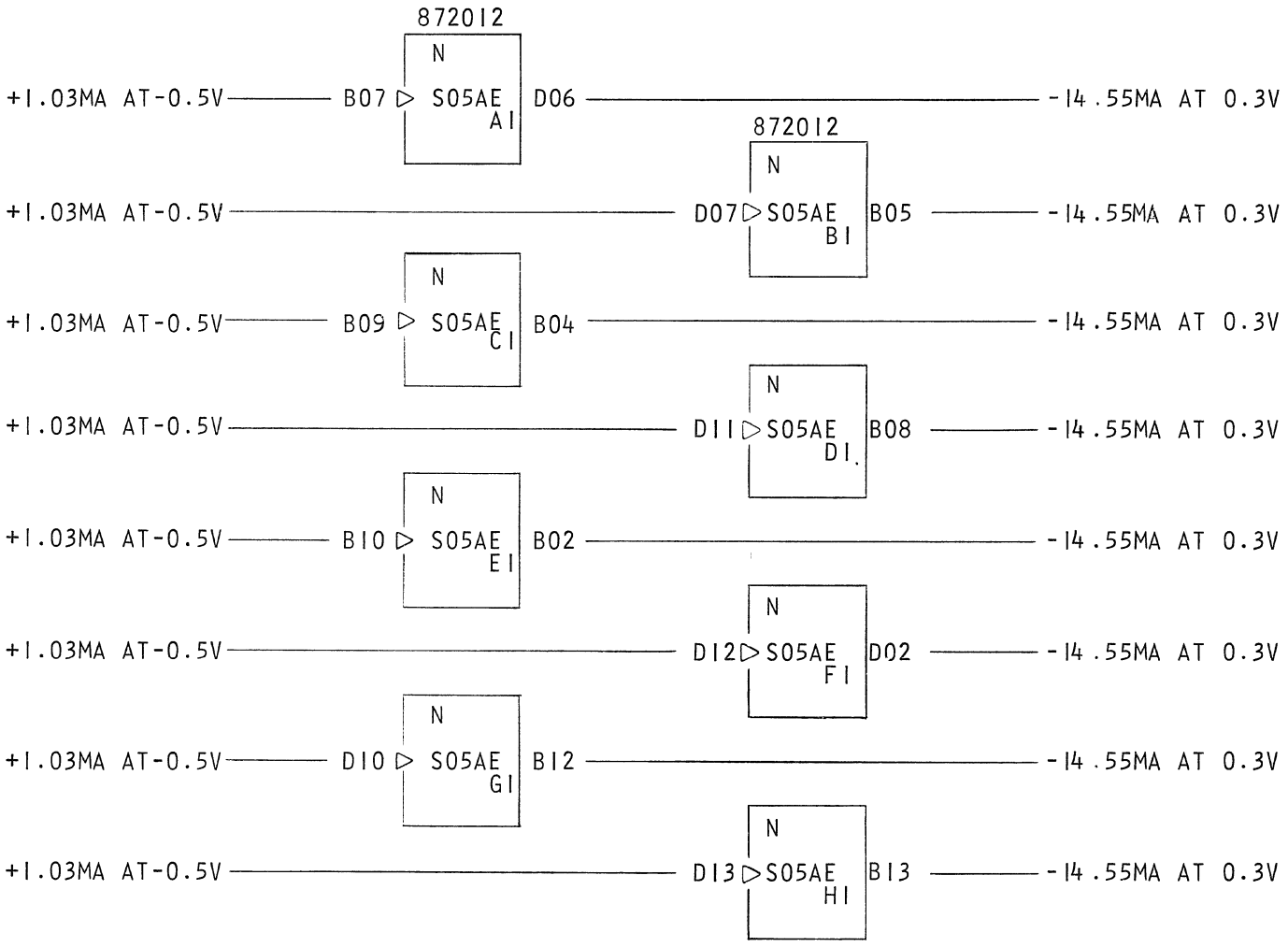
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
D08	GND

8-MULTIPLEX INTERFACE RECEIVERS

CATEGORY CODE

S05

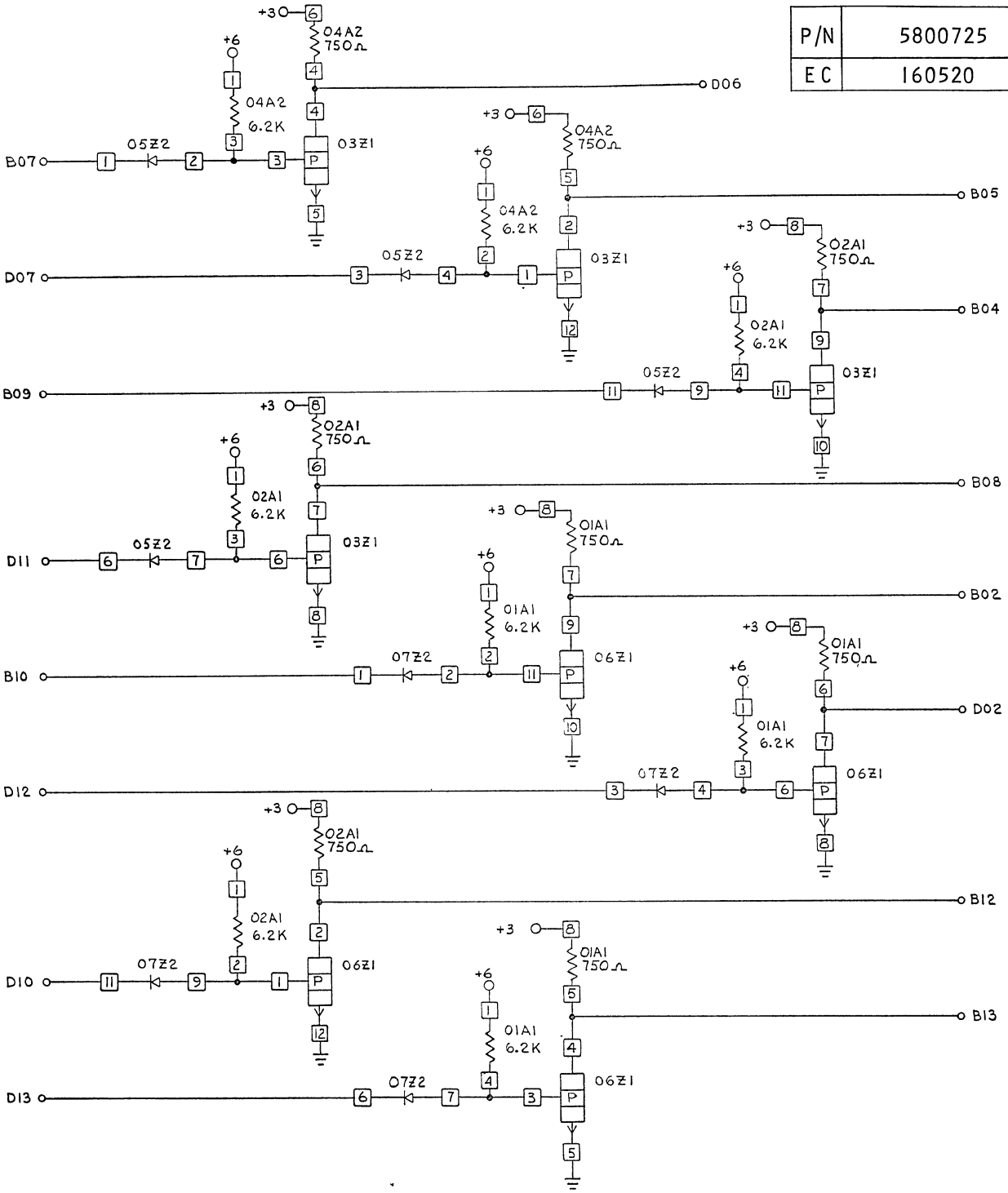
P/N	5800725
EC	160520
SPECIAL RESTRICTED	
CARD SIZE	1-6



LMH Cat.	O-2860 Subject	262 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
8-MULTIPLEX INTERFACE RECEIVERS

P/N	5800725
EC	160520



2 OF 2 Page	1-67 Date	

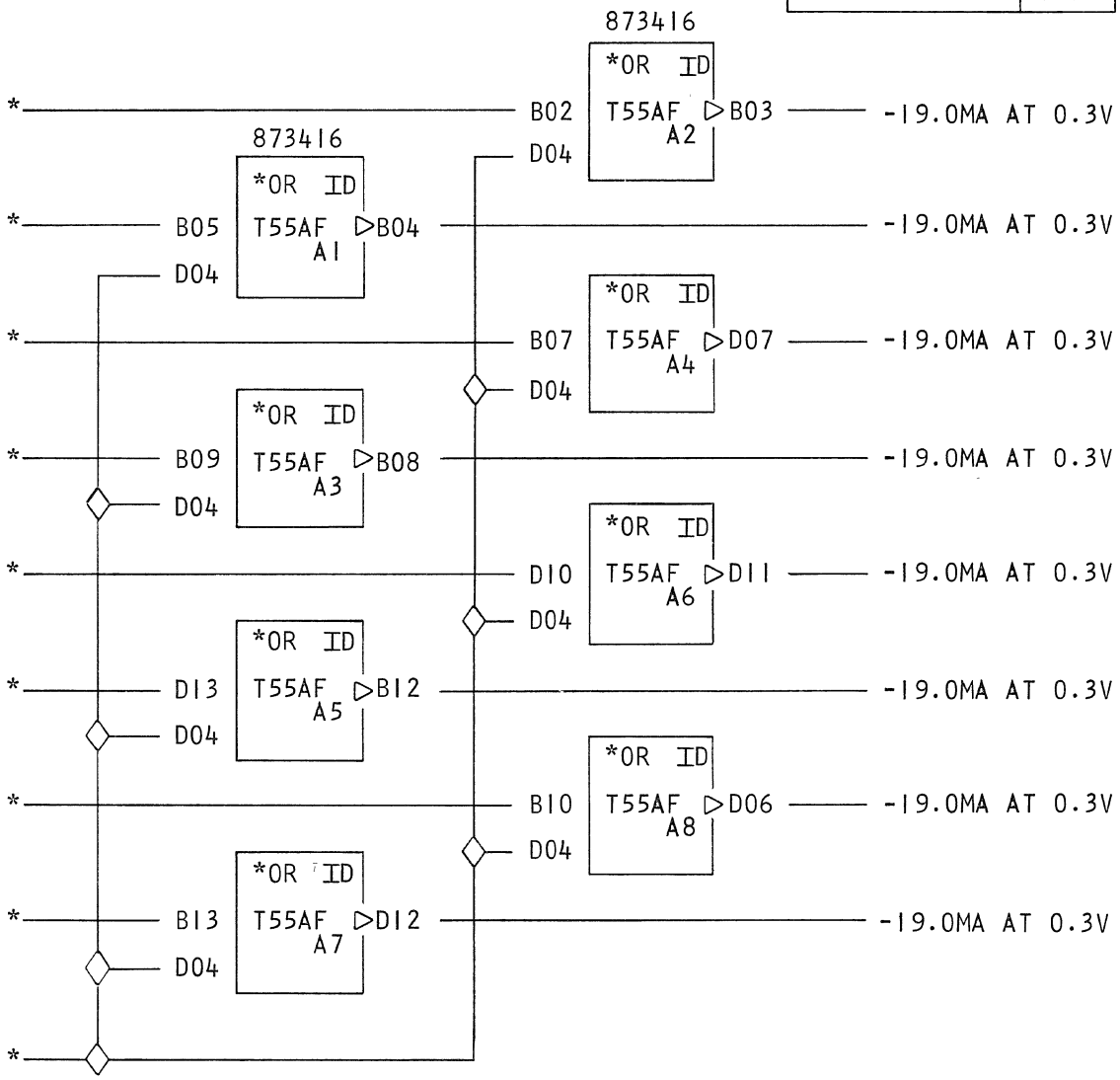
POWER REQUIRED	
PIN	VOLTS
D08	GND

ID 15MA

CATEGORY CODE

T55

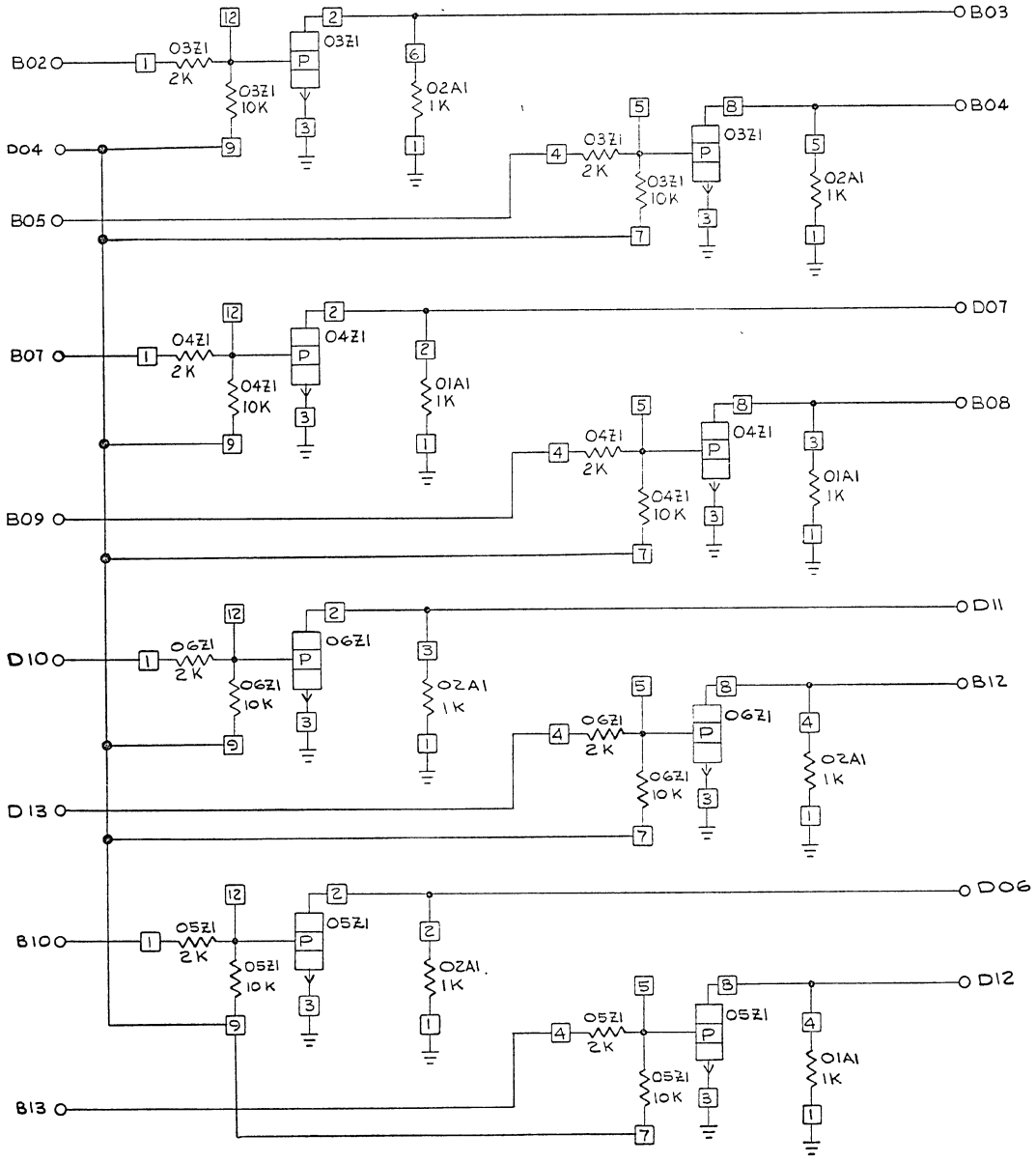
P/N	5800730
EC	160543
SPECIAL RESTRICTED	
CARD SIZE	1-6



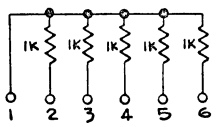
* SPECIAL DRIVE INSTRUCTION SEE CIRCUIT SPEC 873416

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
ID 15MA

P/N	5800730
EC	160543



A1
2390650



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
LINE TERMINATING NETWORK

LMH	0-2860	265
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

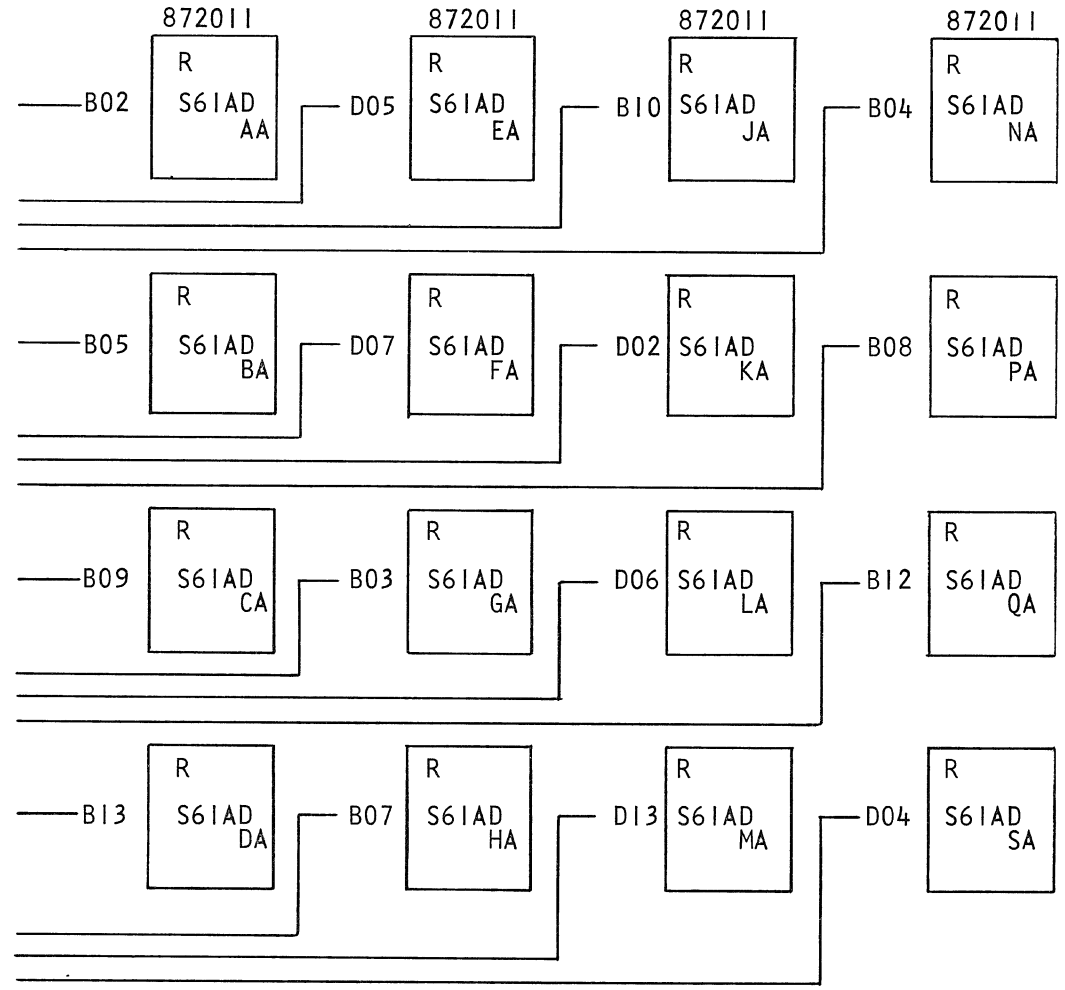
POWER REQUIRED	
PIN	VOLTS
D03	+3
D08	GND

LINE TERMINATING NETWORK

CATEGORY CODE

S06

P/N	5800736
EC	160544
SPECIAL RESTRICTED	
CARD SIZE	1-6



* MAXIMUM LOAD CURRENT
AT -1.88V = 35MA
AT -2.48V = 41.5MA

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		ENDICOTT Responsibility	1-67 Date	1 of 2 Page

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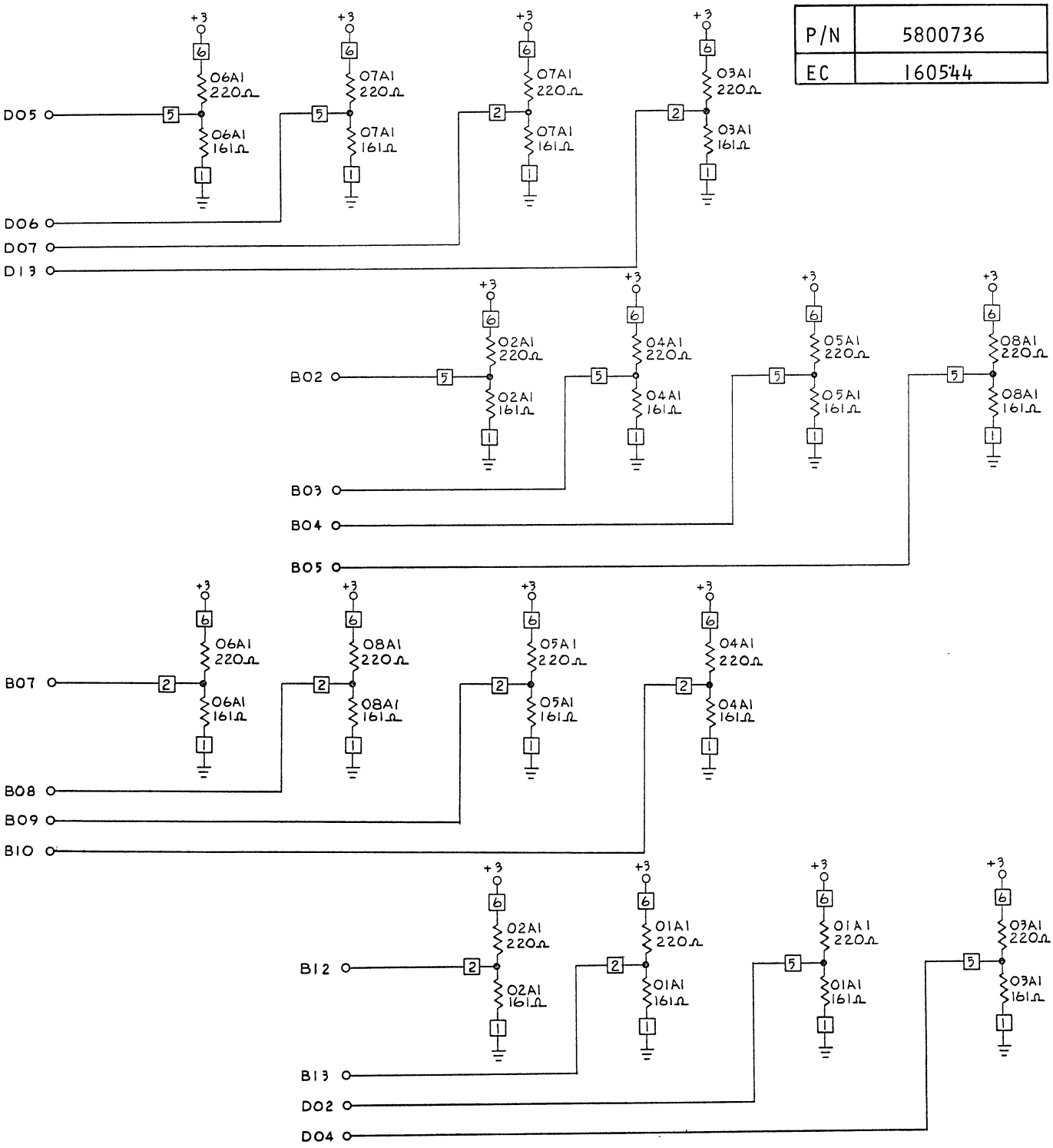
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
LINE TERMINATING NETWORK

P/N	5800736
EC	160544



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
5.0 MHZ X-TAL OSCILLATOR & SATURATING INVERTER

LMH	0-2860	266
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

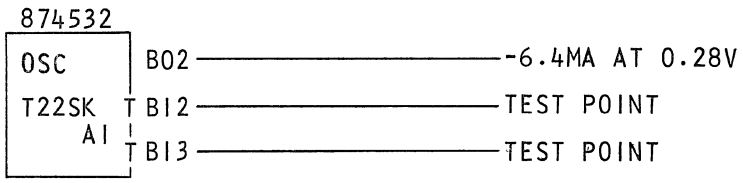
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
D08	GND

5.0 MHZ X-TAL OSCILLATOR & SATURATING INVERTER

CATEGORY CODE

T22

P/N	5800768
EC	164785A
SPECIAL RESTRICTED	
CARD SIZE	1-12



NOTE: FOR NORMAL USAGE CONNECT B12 AND B13

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		ENDICOTT Responsibility	1-67 Date	1 OF 2 Page

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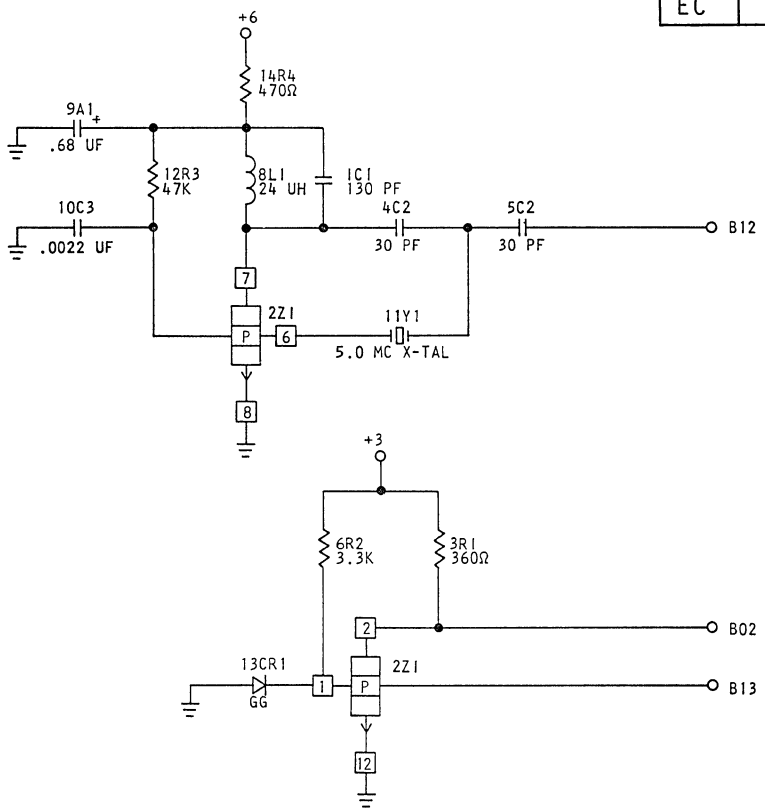
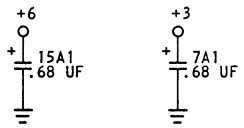
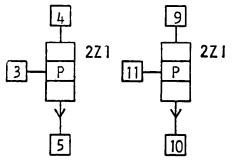
LMH Cat.	O-2860 Subject	266 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 5.0 MHZ X-TAL OSCILLATOR & SATURATING INVERTER

P/N	5800768
EC	164785A







2 OF 2 Page	1-67 Date	

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
AC TRIGGER

LMH	0-2860	267
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

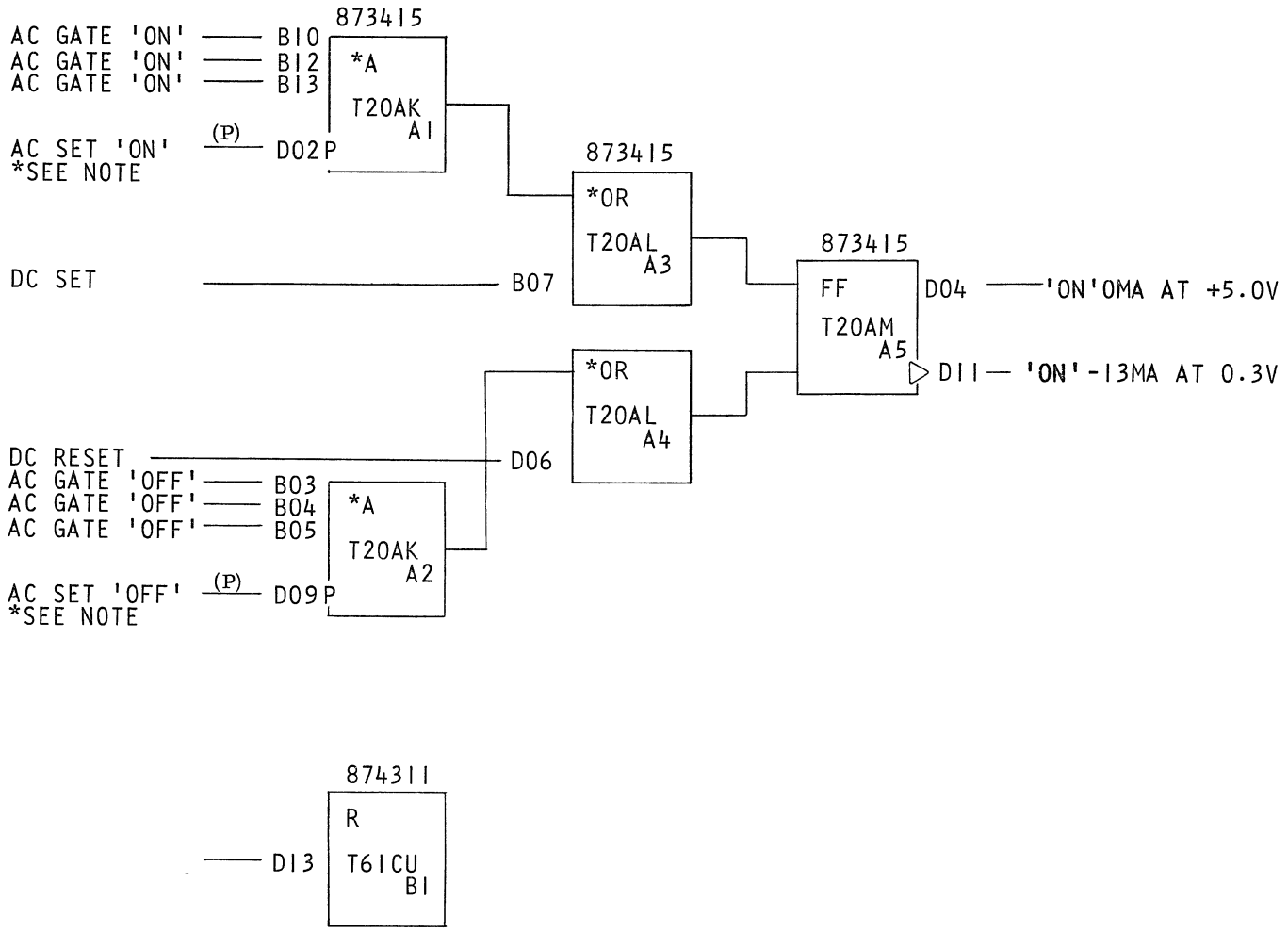
POWER REQUIRED	
PIN	VOLTS
B11	+6
D08	GND

AC TRIGGER

CATEGORY CODE

T20

P/N	5800800
EC	163460A
STANDARD RESTRICTED	
CARD SIZE	1-6



* SPECIAL DRIVE INSTRUCTIONS SEE CIRCUIT SPEC 873415

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
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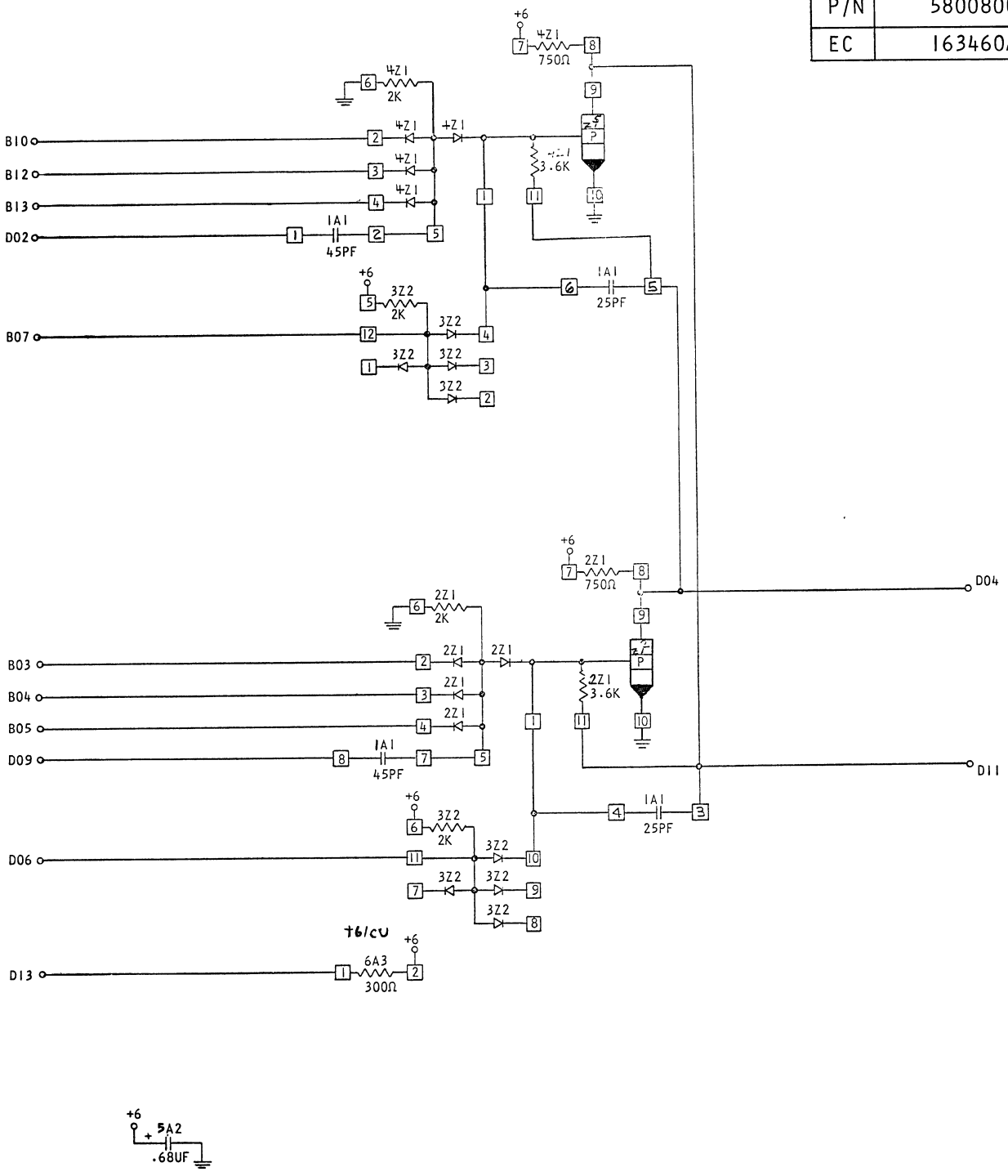
LMH Cat.	0-2860 Subject	267 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
AC TRIGGER

P/N	5800800
EC	163460A

T20AK, T20AL, T20AM



2 OF 2 Page	1-67 Date

IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

6-XOR LTH

CATEGORY CODE

T03

P/N	5800813
EC	161115
STANDARD RESTRICTED	
CARD SIZE	1-6

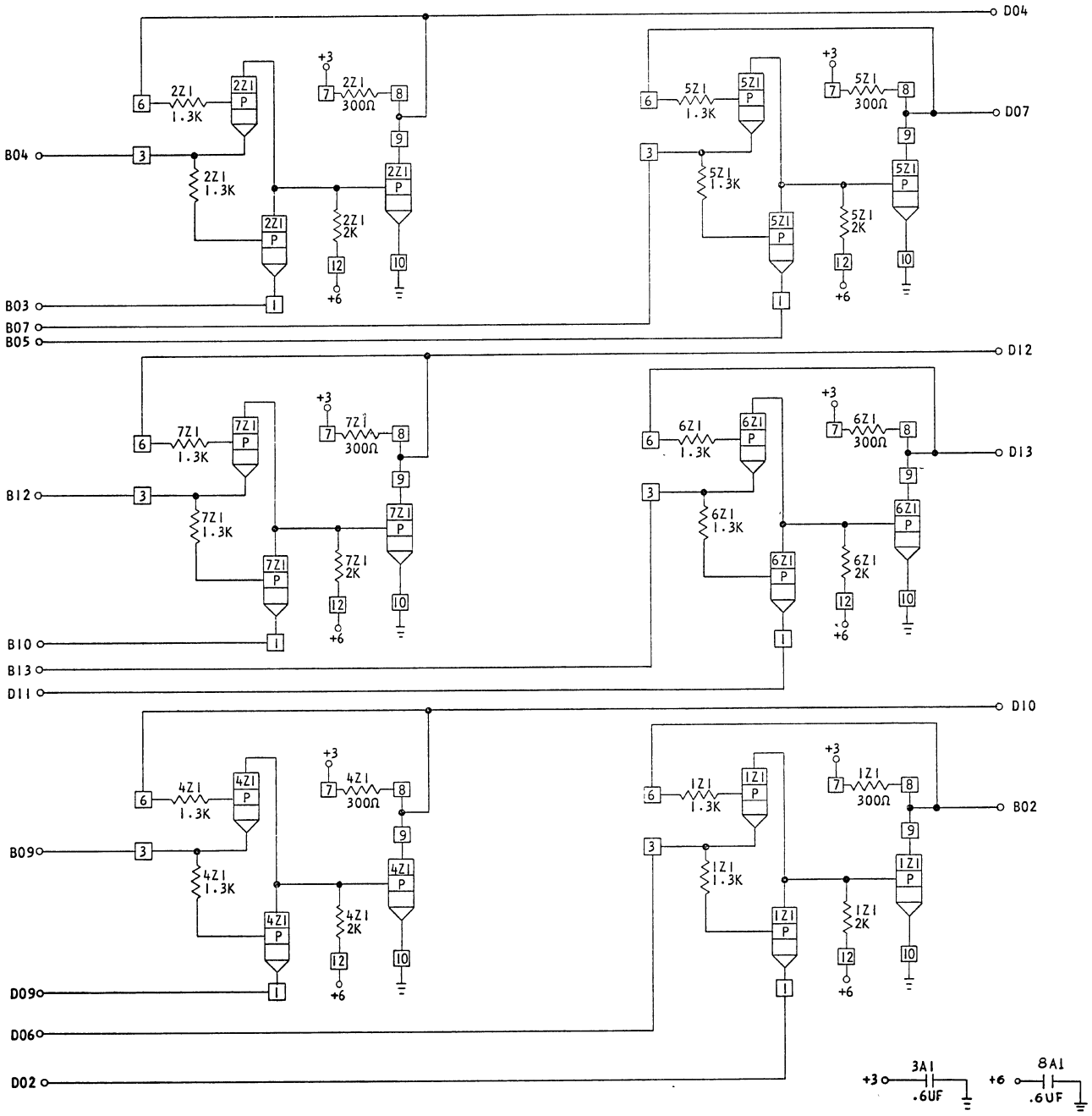
890985

DATA	*	B03 ▷ *PH	T03AK A1	▷ D04		
CONTROL	*	B04				-24.0MA AT 0.3V
DATA	*	B05 ▷ *PH	T03AK B1	▷ D07		
CONTROL	*	B07				-24.0MA AT 0.3V
DATA	*	B10 ▷ *PH	T03AK C1	▷ D12		
CONTROL	*	B12				-24.0MA AT 0.3V
DATA	*	D11 ▷ *PH	T03AK D1	▷ D13		
CONTROL	*	B13				-24.0MA AT 0.3V
DATA	*	D09 ▷ *PH	T03AK E1	▷ D10		
CONTROL	*	B09				-24.0MA AT 0.3V
DATA	*	D02 ▷ *PH	T03AK F1	▷ B02		
CONTROL	*	D06				-24.0MA AT 0.3V

* SPECIAL DRIVE RULES SEE CIRCUIT SPEC 890985

LMH Cat.	0-2860 Subject	268 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 6-XOR LTH

P/N	5800813
EC	161115



2 OF 2 Page	1-67 Date	

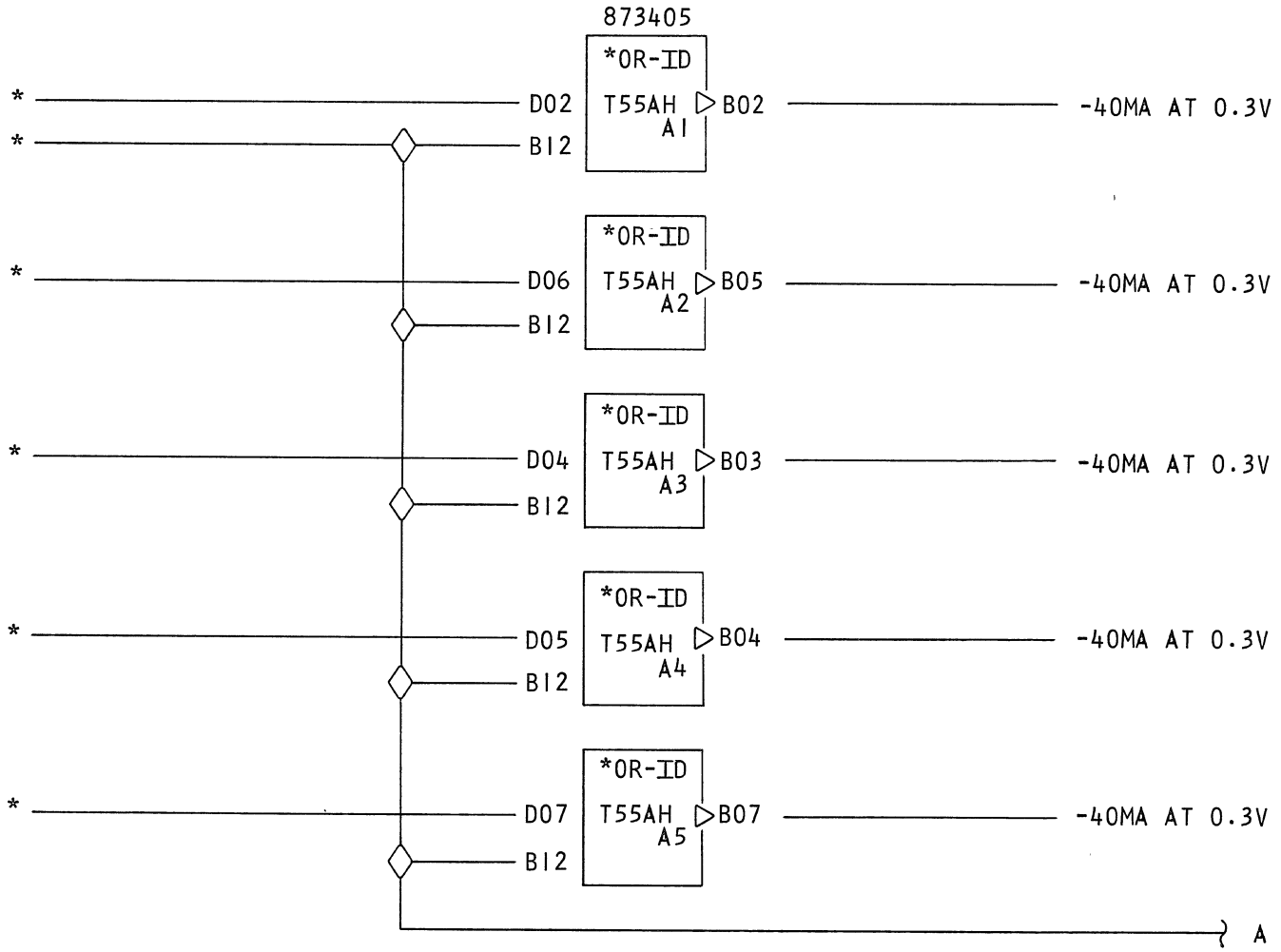
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

9-40MA ID

CATEGORY CODE

T55

P/N	5800822
EC	162045
STANDARD RESTRICTED	
CARD SIZE	1-6



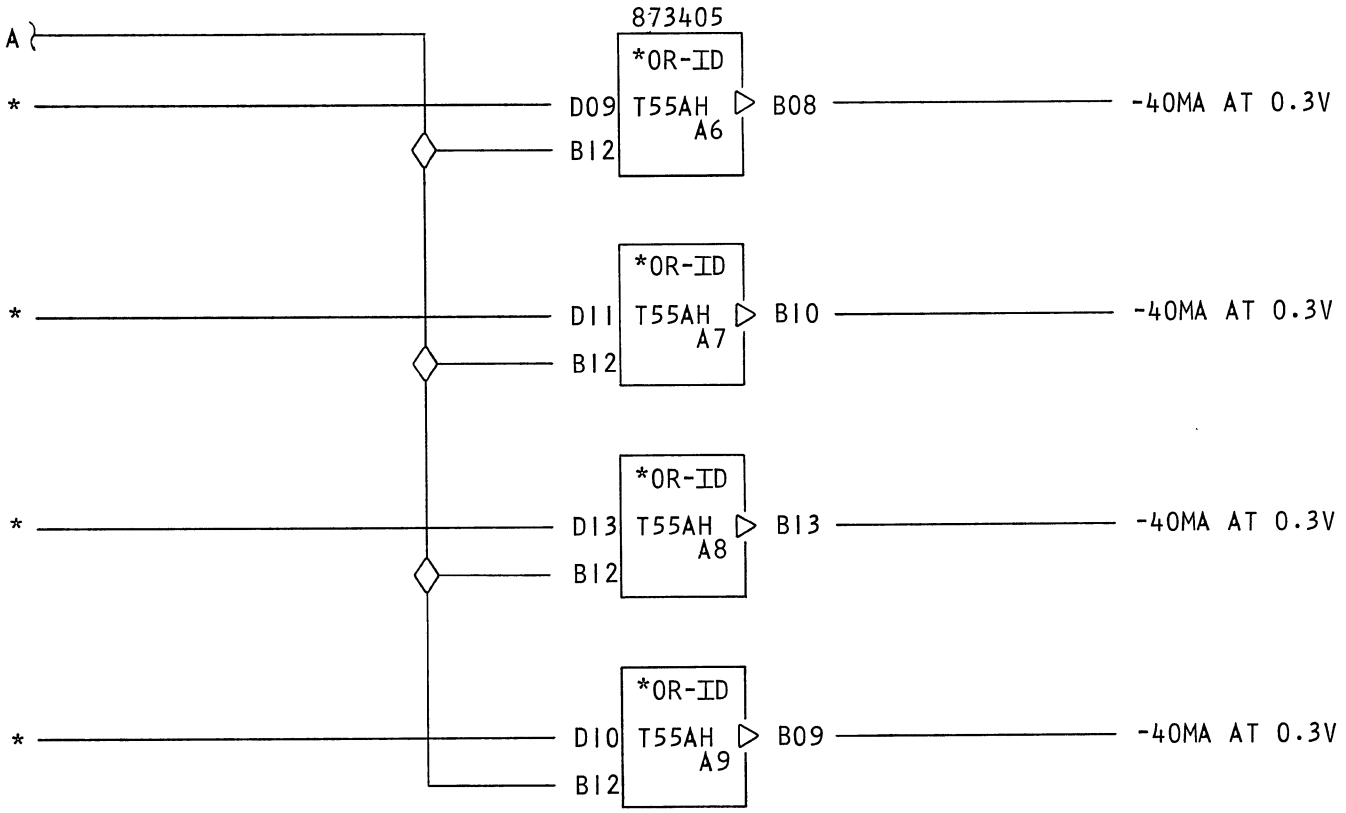
* SPECIAL DRIVE RULES SEE CIRCUIT SPEC 873405

9-40MA ID

CATEGORY CODE

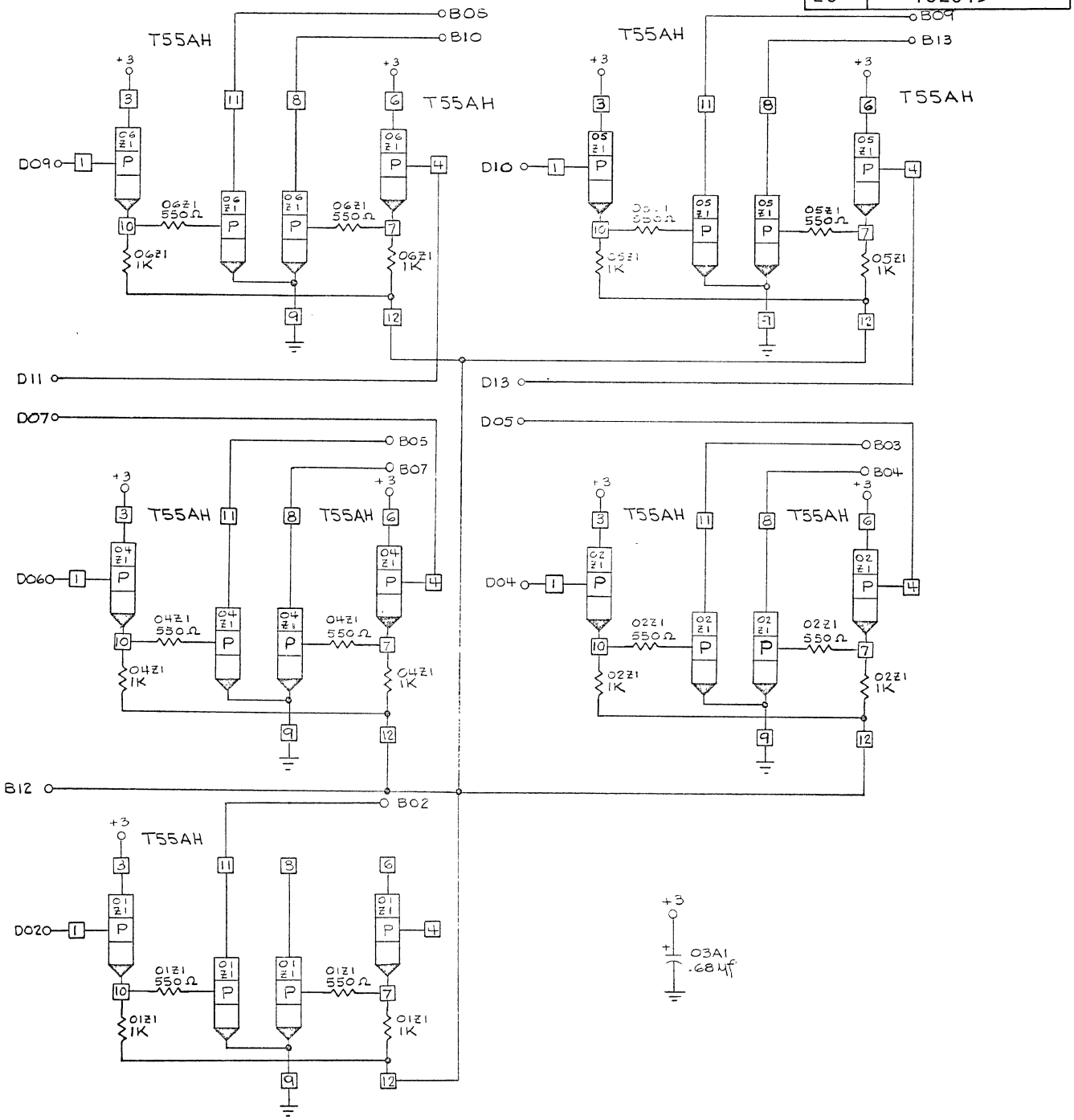
T55

P/N	5800822
EC	162045



* SPECIAL DRIVE RULES SEE CIRCUIT SPEC 873405

P/N	5800822
EC	162045



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-S.P. (N/O) 48 VOLT REED RELAYS

LMH	0-2860	274
Cat	Subject	Suffix

IBM

Location

Manufacturing Specification

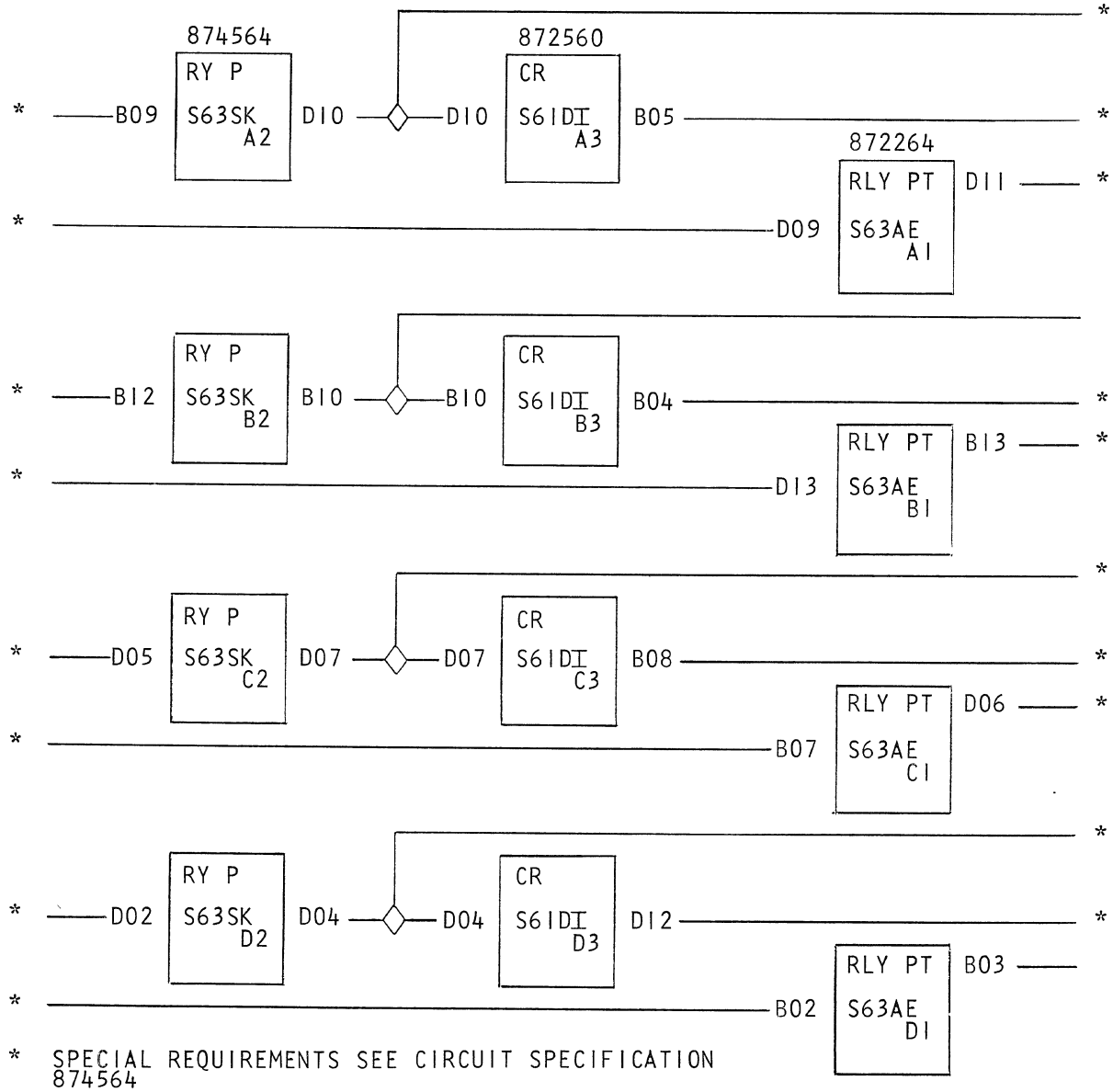
POWER REQUIRED
NONE*

4-S.P. (N/O) 48 VOLT REED RELAYS

CATEGORY CODE

S63

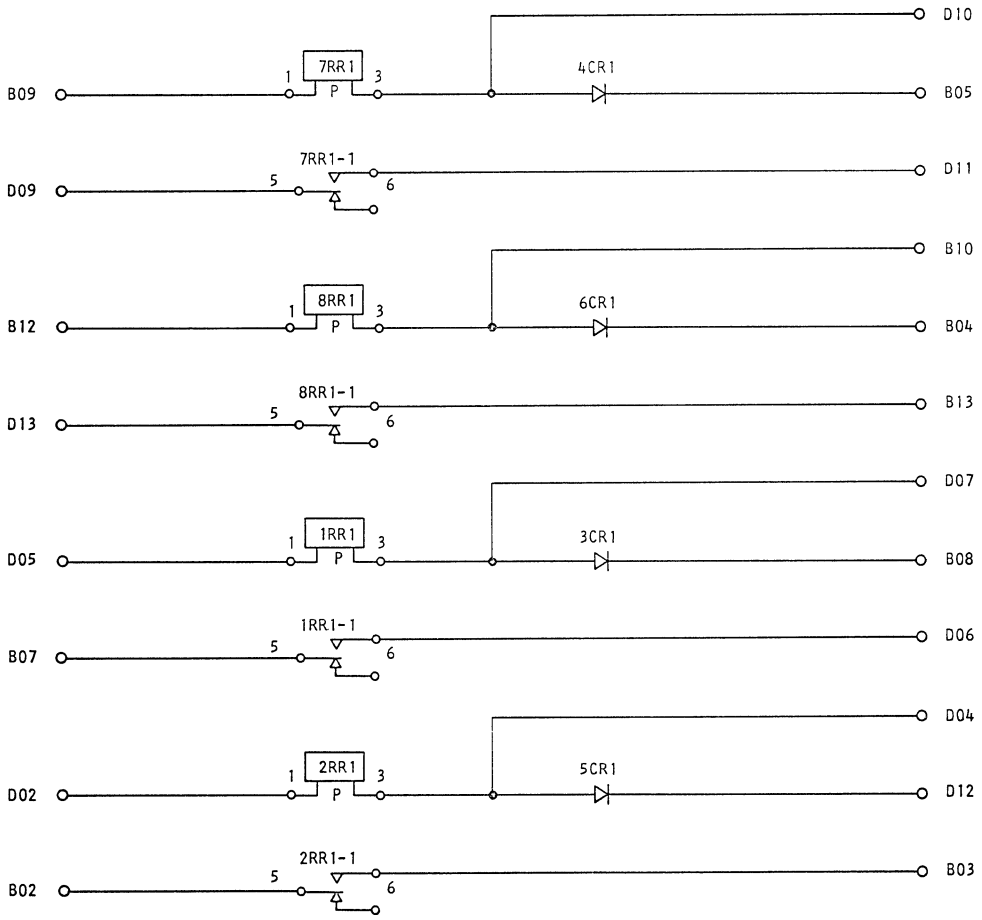
P/N	5800871
EC	164820A
SPECIAL RESTRICTED	
CARD SIZE	1-12



* SPECIAL REQUIREMENTS SEE CIRCUIT SPECIFICATION 874564

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-S.P. (N/O) 48 VOLT REED RELAYS

P/N	5800871
EC	164820A



IBM Location
Manufacturing Specification

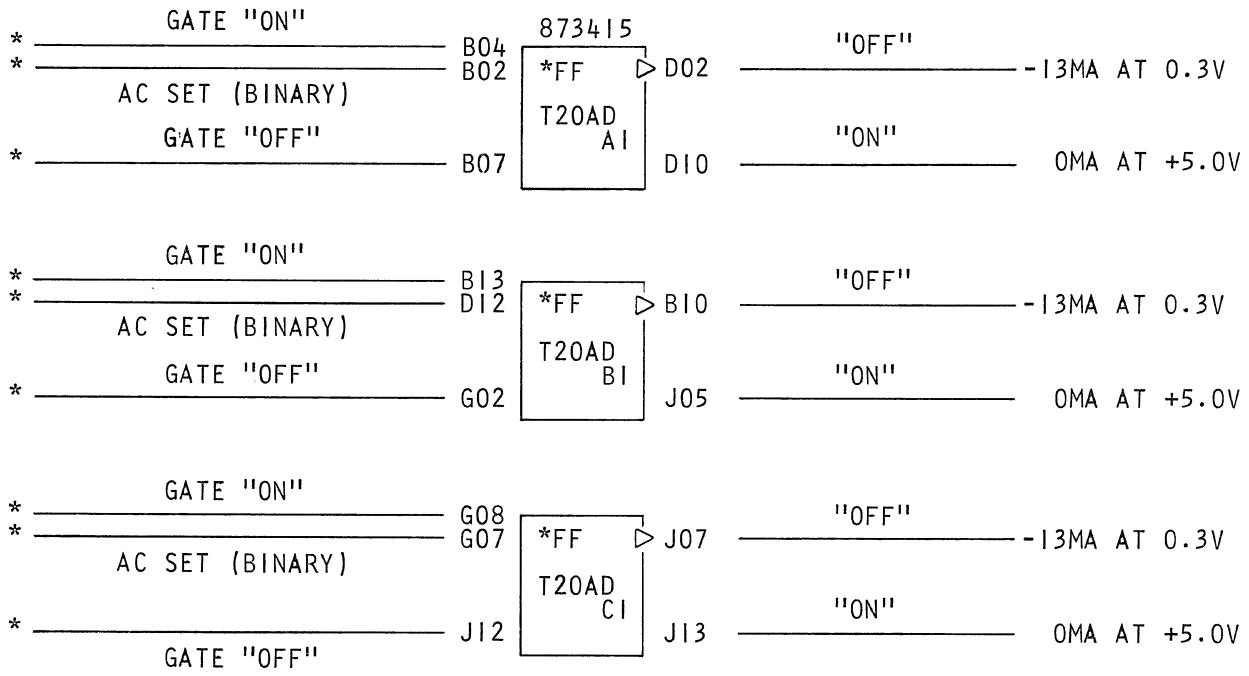
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

AC TRIGGER (BINARY)

CATEGORY CODE

T20

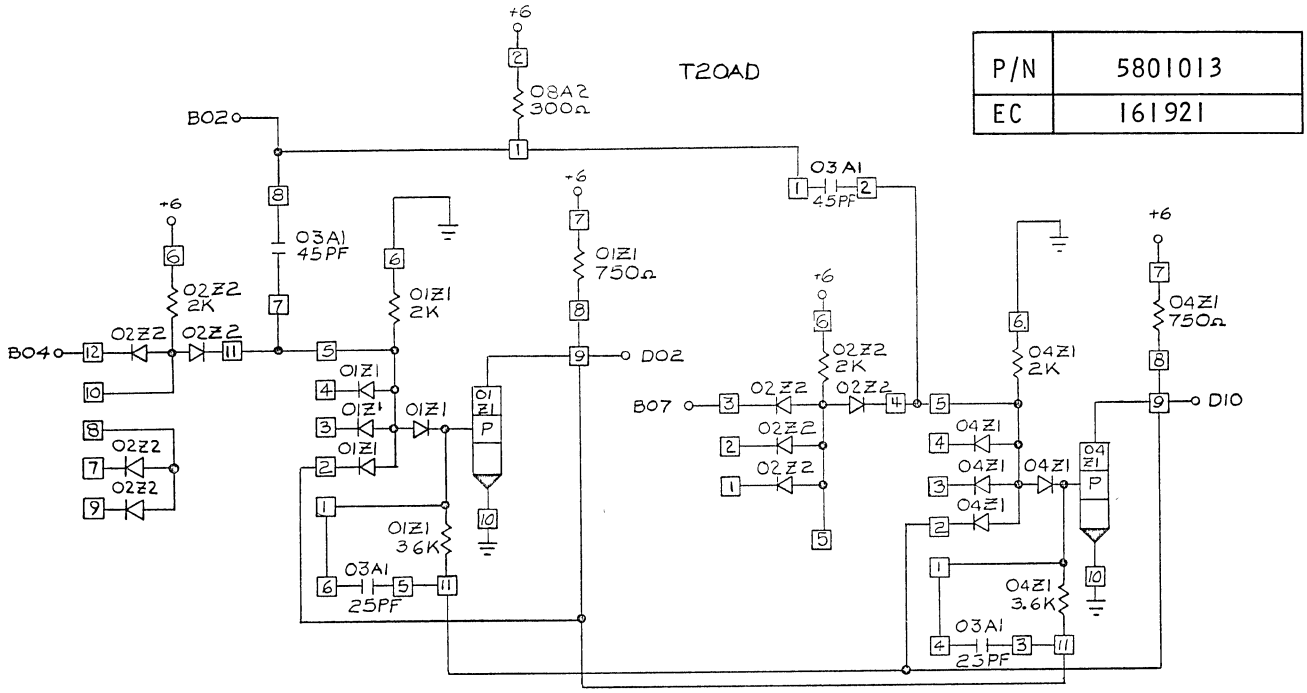
P/N	5801013
EC	161921
STANDARD RESTRICTED	
CARD SIZE	1-6

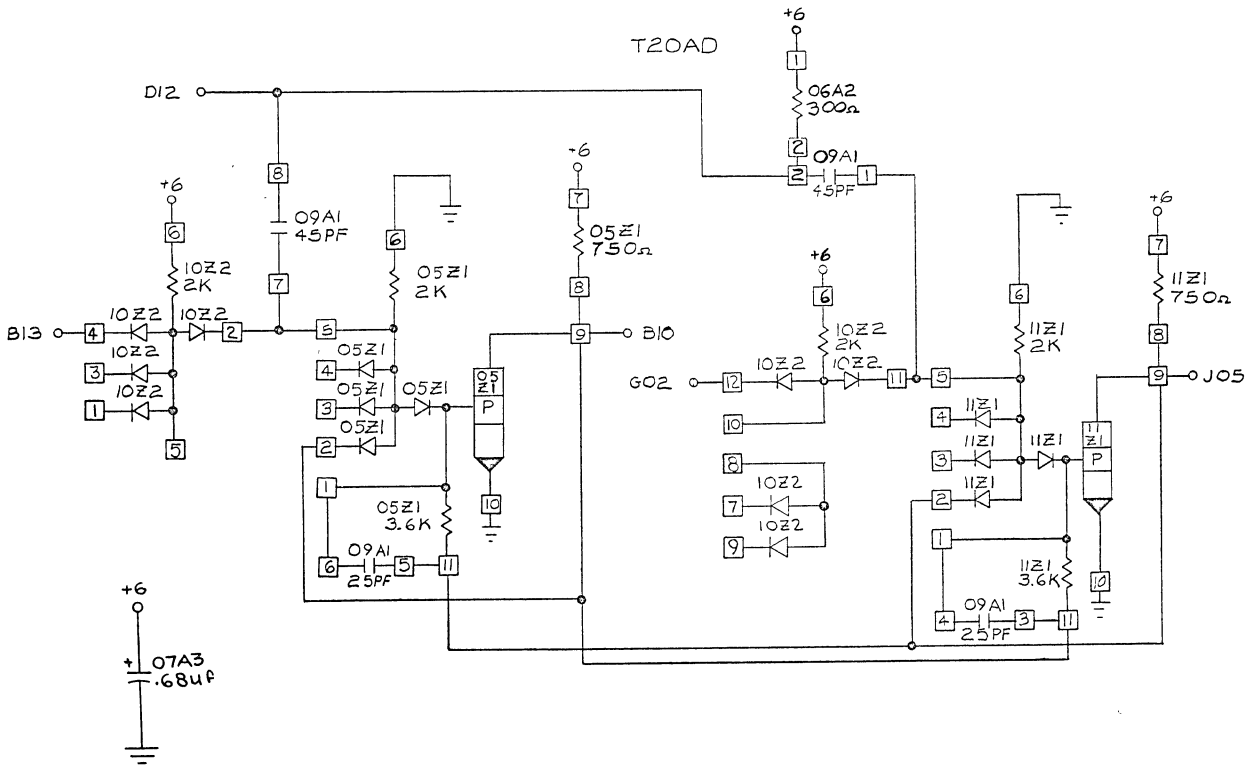


* SPECIAL DRIVE RULES SEE SPEC 873415

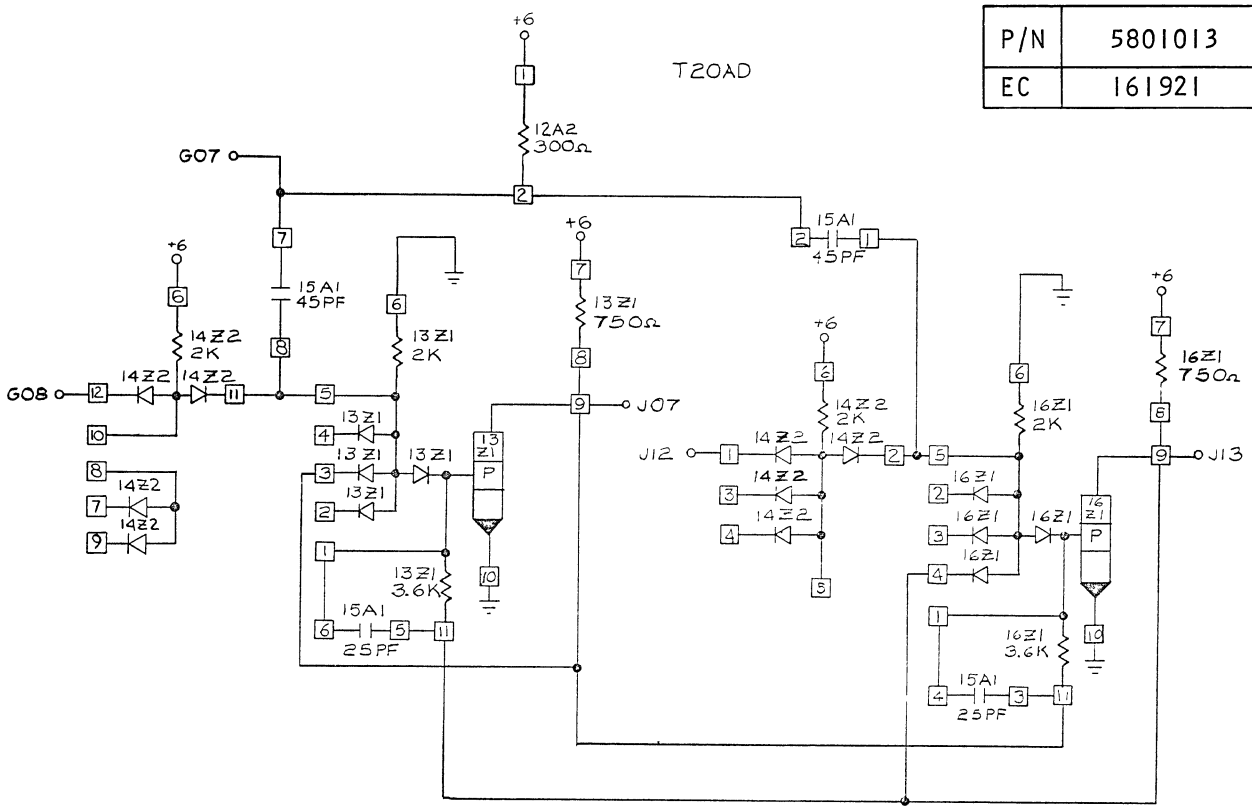
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
AC TRIGGER (BINARY)

P/N	5801013
EC	161921





P/N	5801013
EC	161921



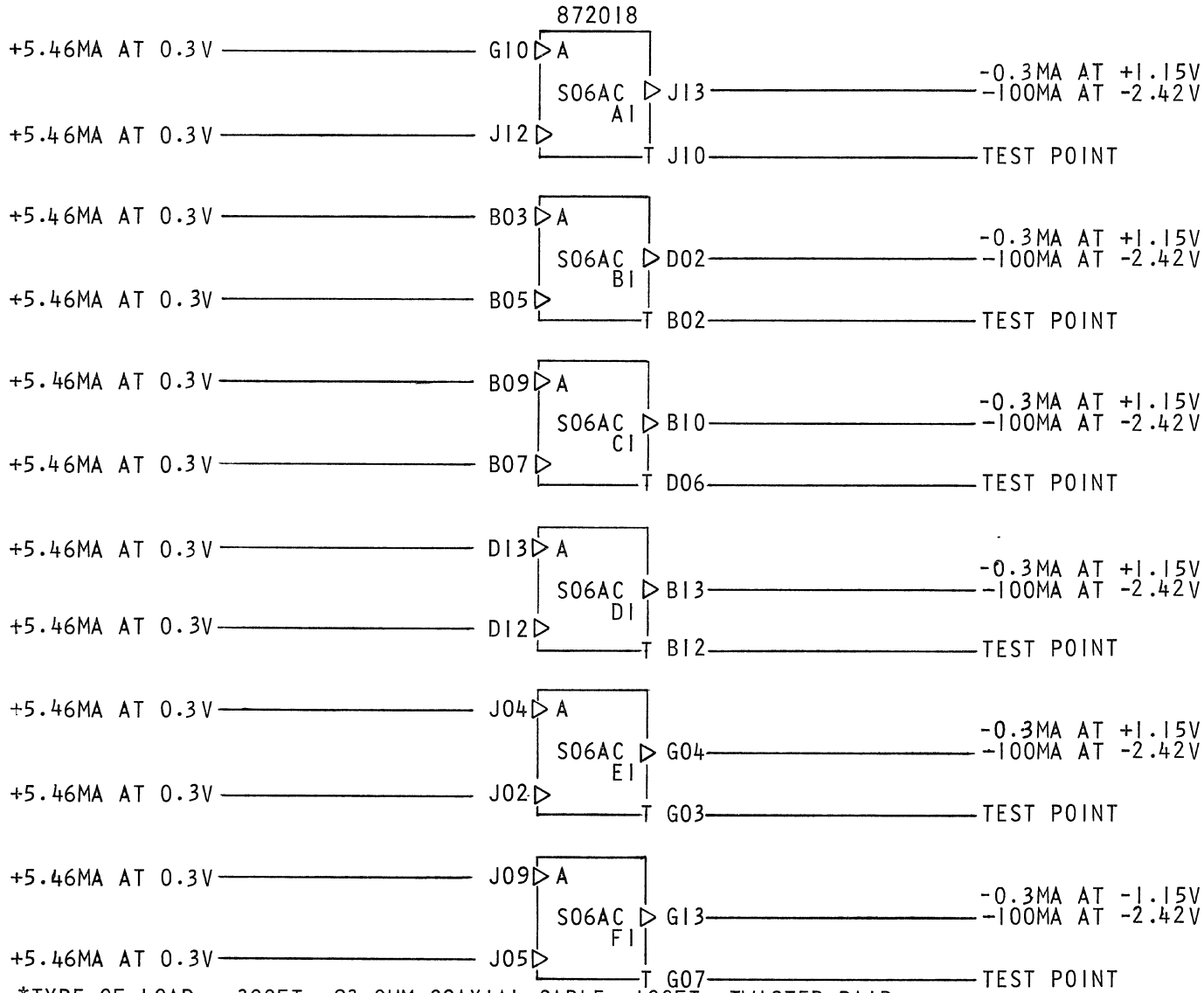
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D08	GND
J08	GND

MULTIPLEX INTERFACE DRIVER

CATEGORY CODE

S06

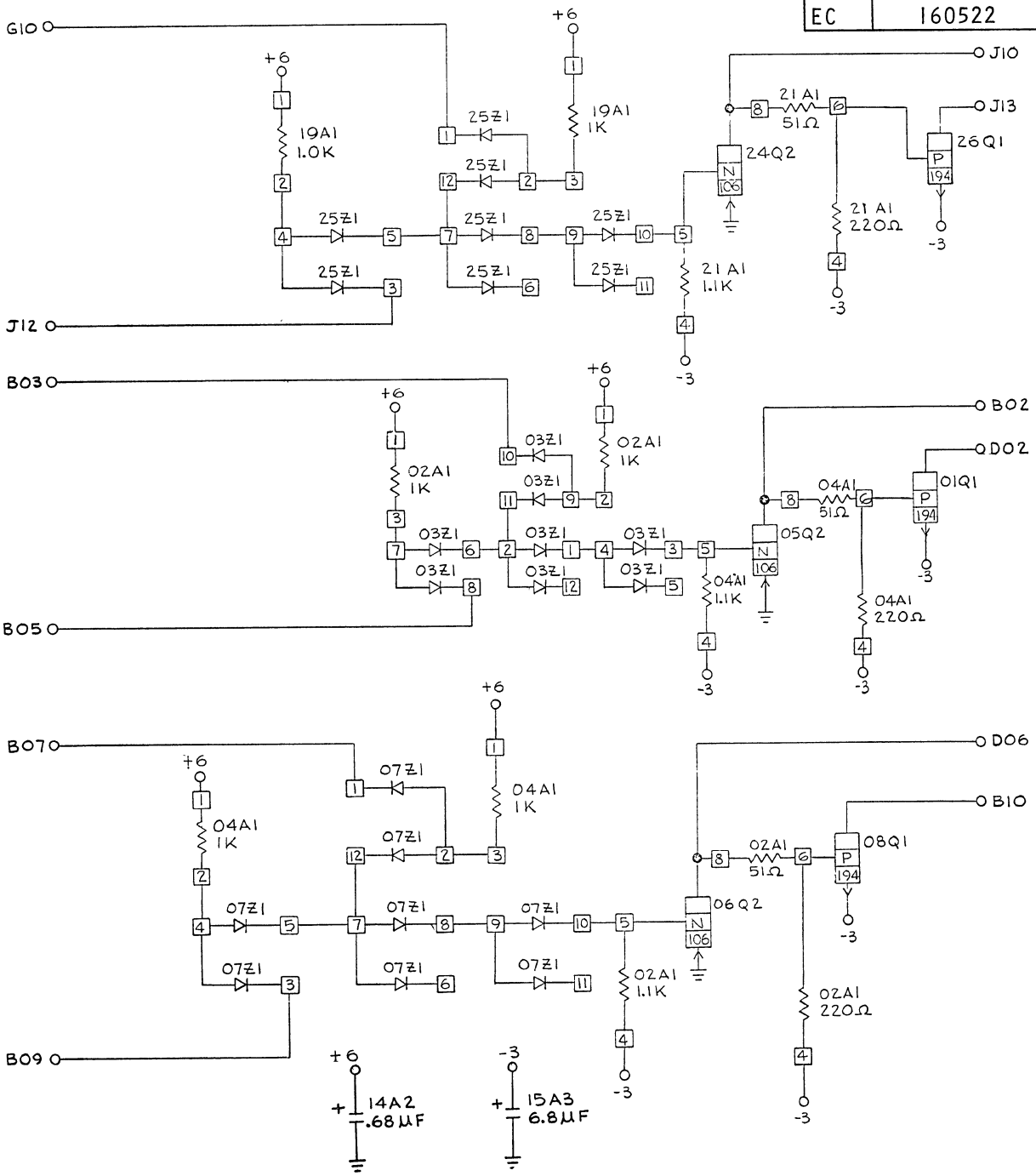
P/N	5801147
EC	160522
SPECIAL	RESTRICTED
CARD SIZE	2-12



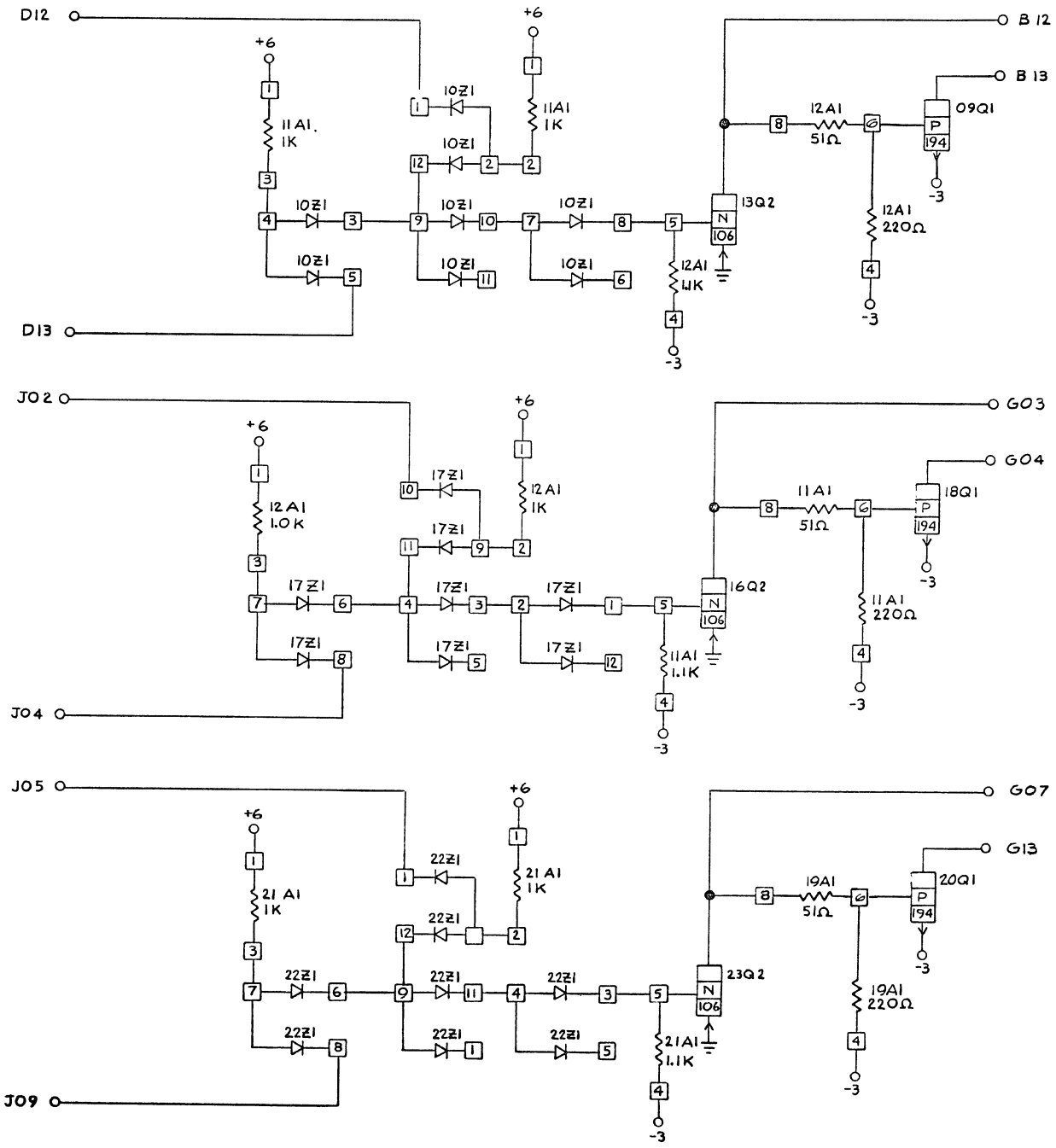
*TYPE OF LOAD: 300FT. 93 OHM COAXIAL CABLE 100FT. TWISTED PAIR
EACH END MUST BE TERMINATED IN ITS CHARACTERISTIC IMPEDANCE.

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
MULTIPLEX INTERFACE DRIVER

P/N	5801147
EC	160522



P/N	5801147
EC	160522



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
RES. CARD, CABLE TERMINATORS

LMH	0-2860	281
Cat.	Subject	Suffix

IBM **Location Manufacturing Specification**

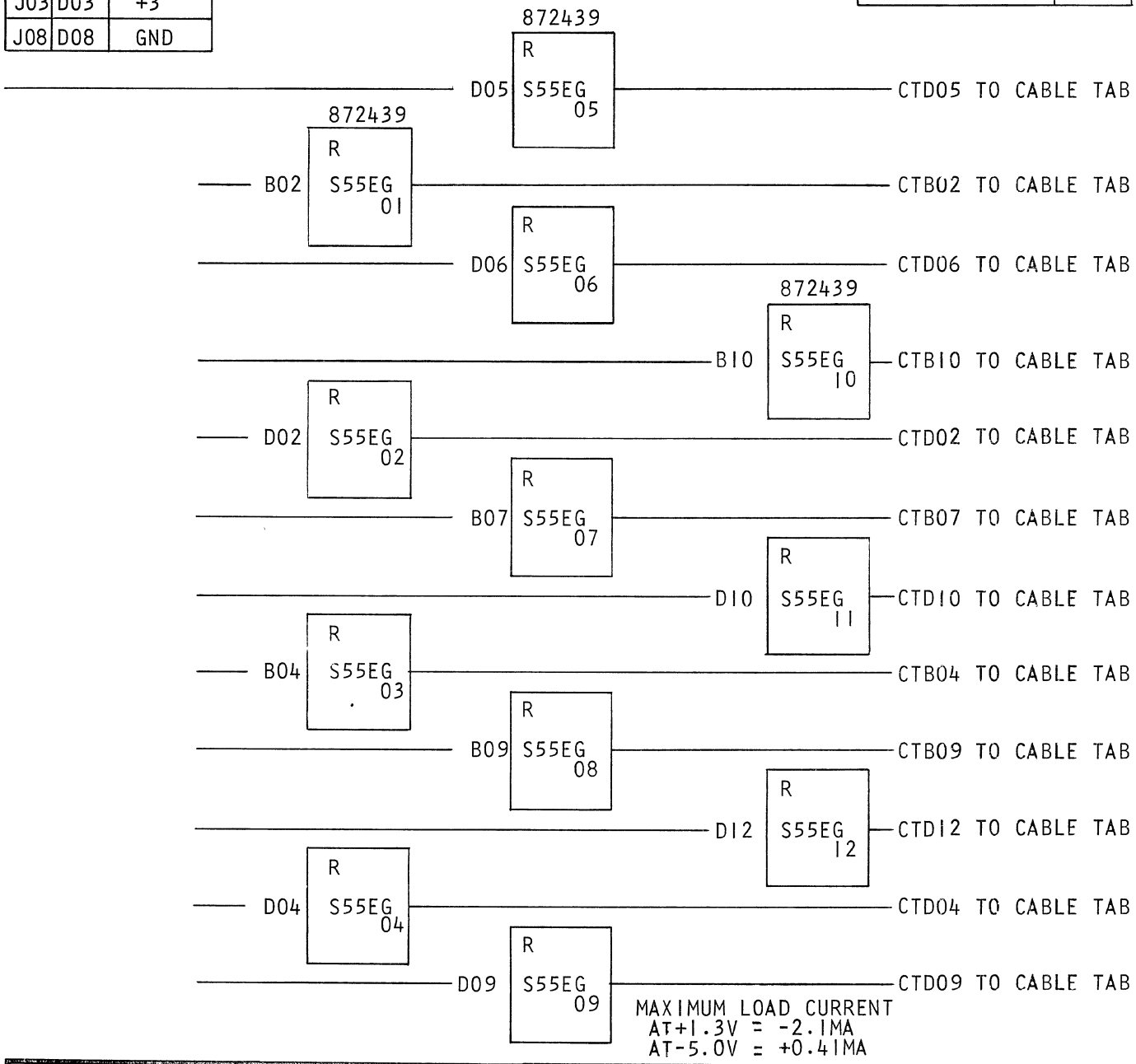
POWER REQUIRED		
PIN		VOLTS
G06	B06	-3
G11	B11	+6
J03	D03	+3
J08	D08	GND

RES. CARD, CABLE TERMINATORS

CATEGORY CODE

S55

P/N	5801246
EC	165508C
STANDARD RESTRICTED	
CARD SIZE	2-12



MAXIMUM LOAD CURRENT
AT+1.3V = -2.1MA
AT-5.0V = +0.41MA

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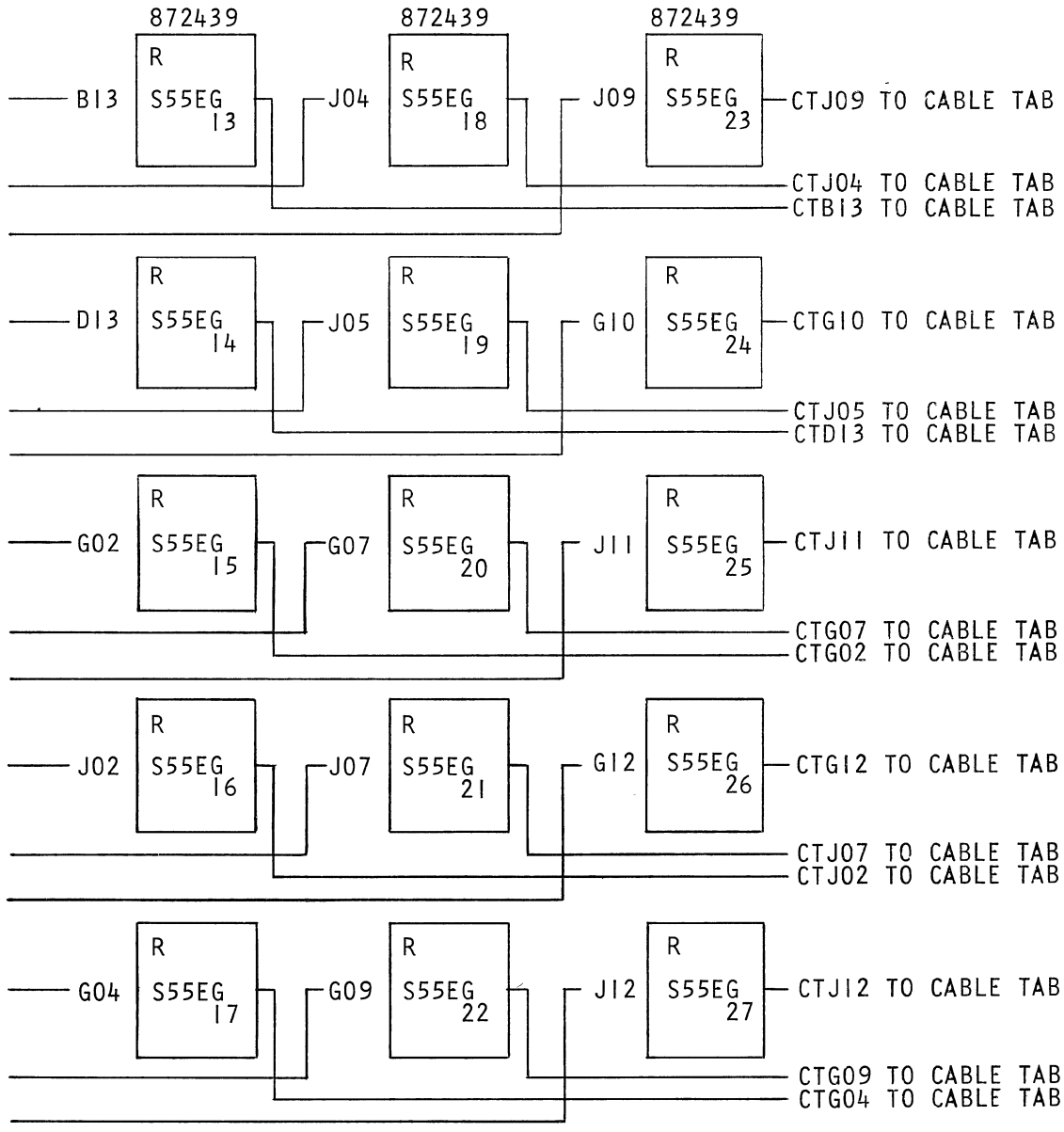
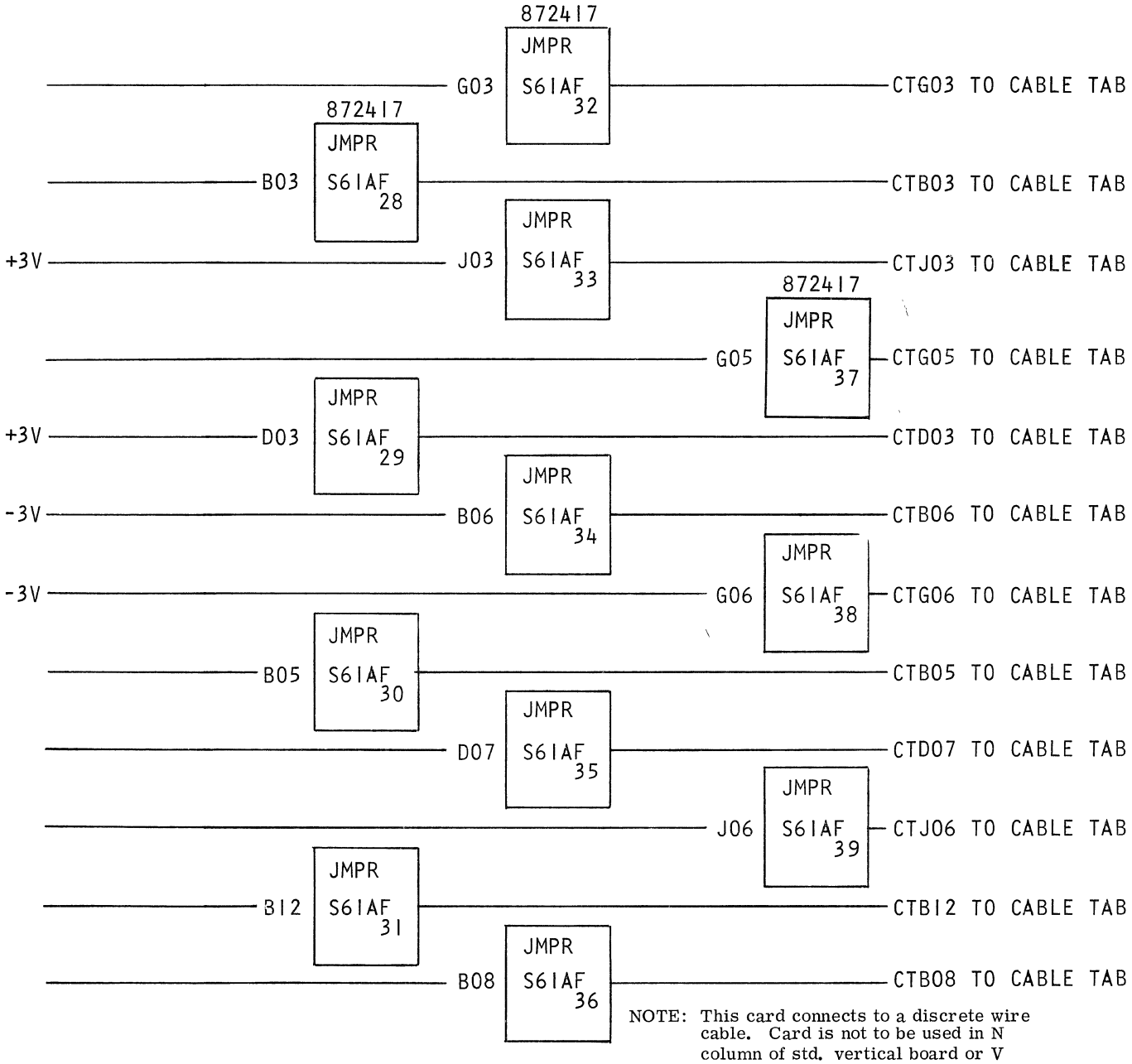
RES. CARD, CABLE TERMINATORS

P/N	5801246
EC	165508C



RES. CARD, CABLE TERMINATORS

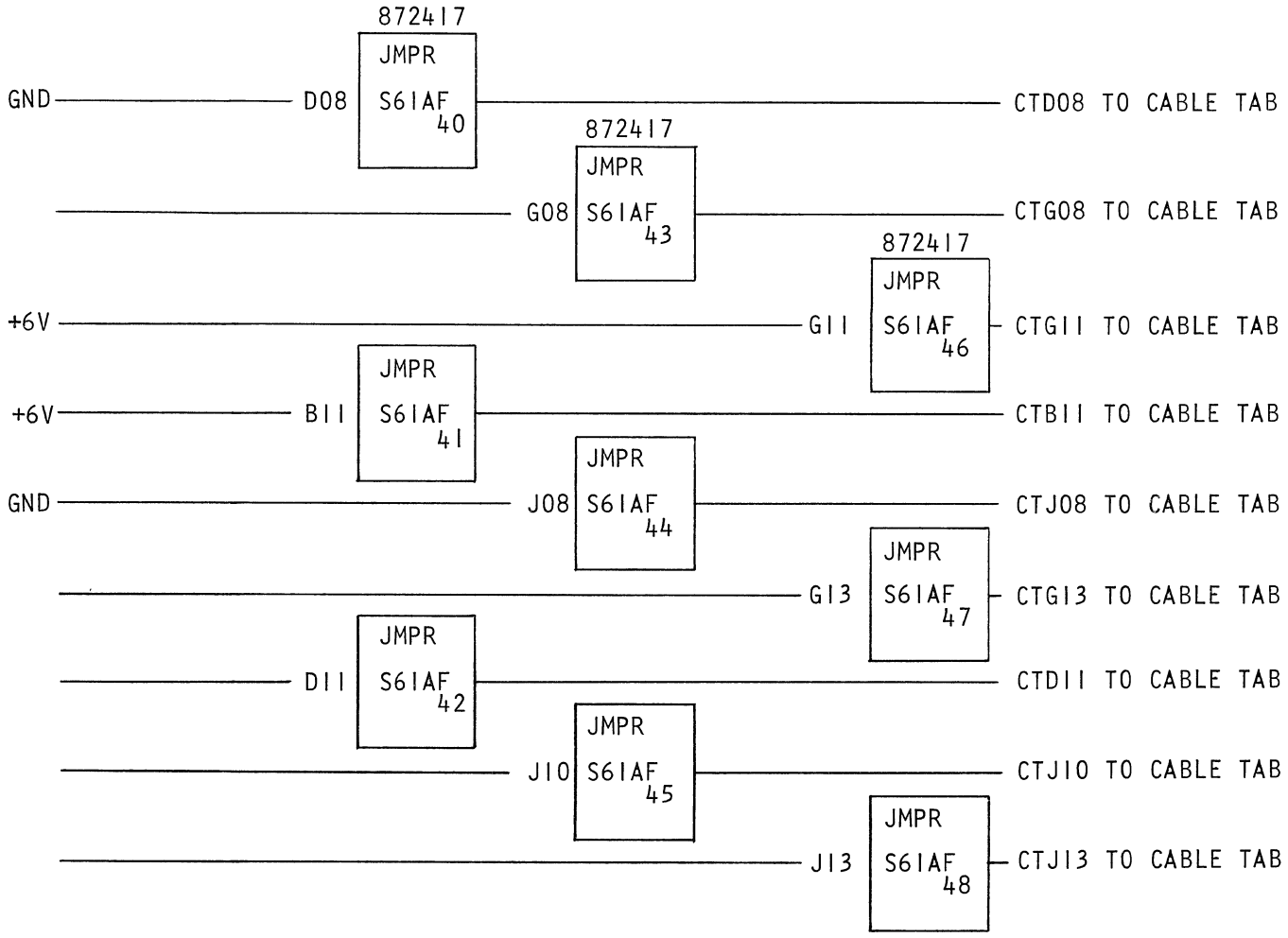
P/N	5801246
EC	165508C



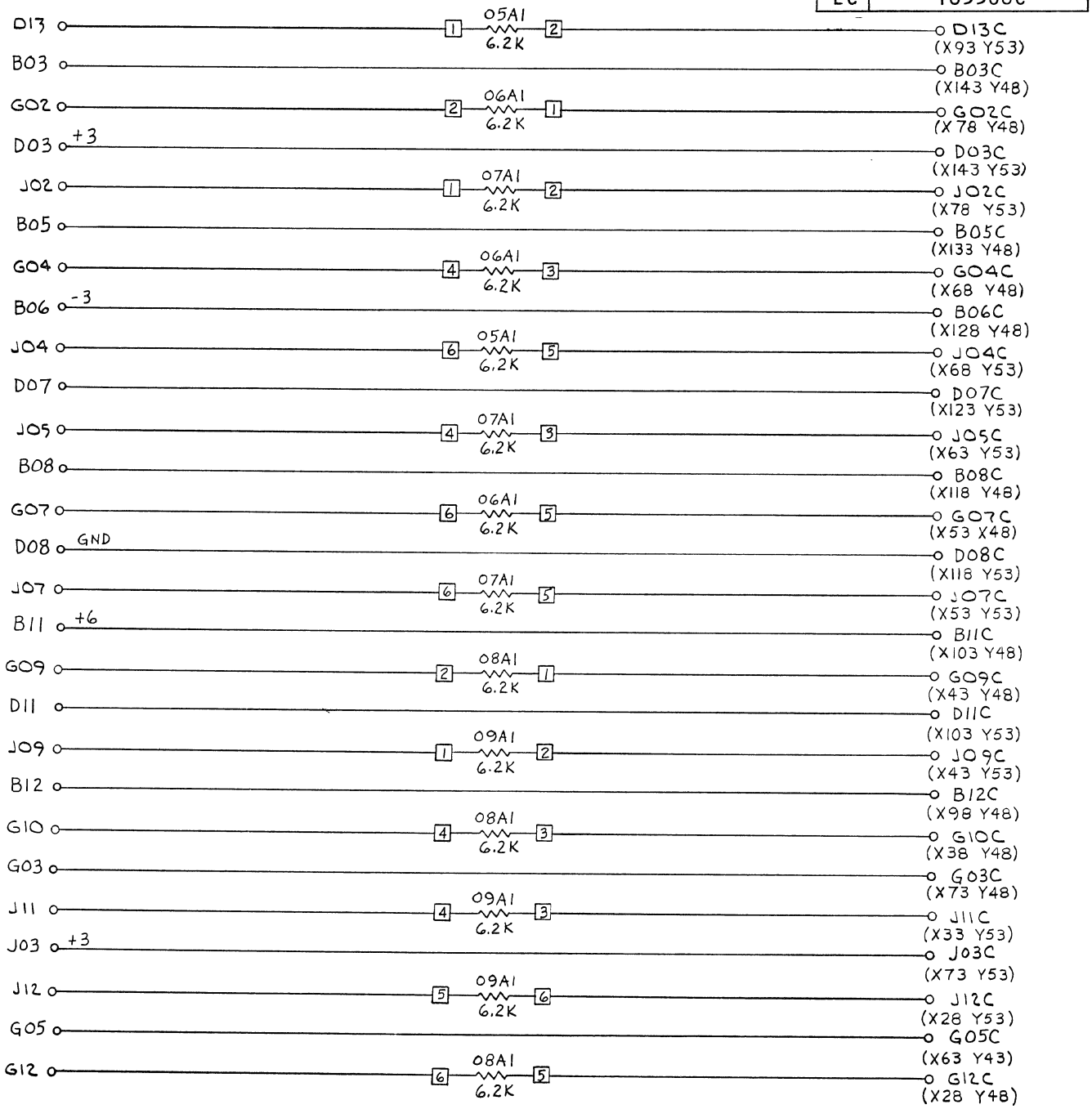
NOTE: This card connects to a discrete wire cable. Card is not to be used in N column of std. vertical board or V column of std. horizontal board.

RES. CARD, CABLE TERMINATORS

P/N	5801246
EC	165508C



P/N	5801246
EC	165508C



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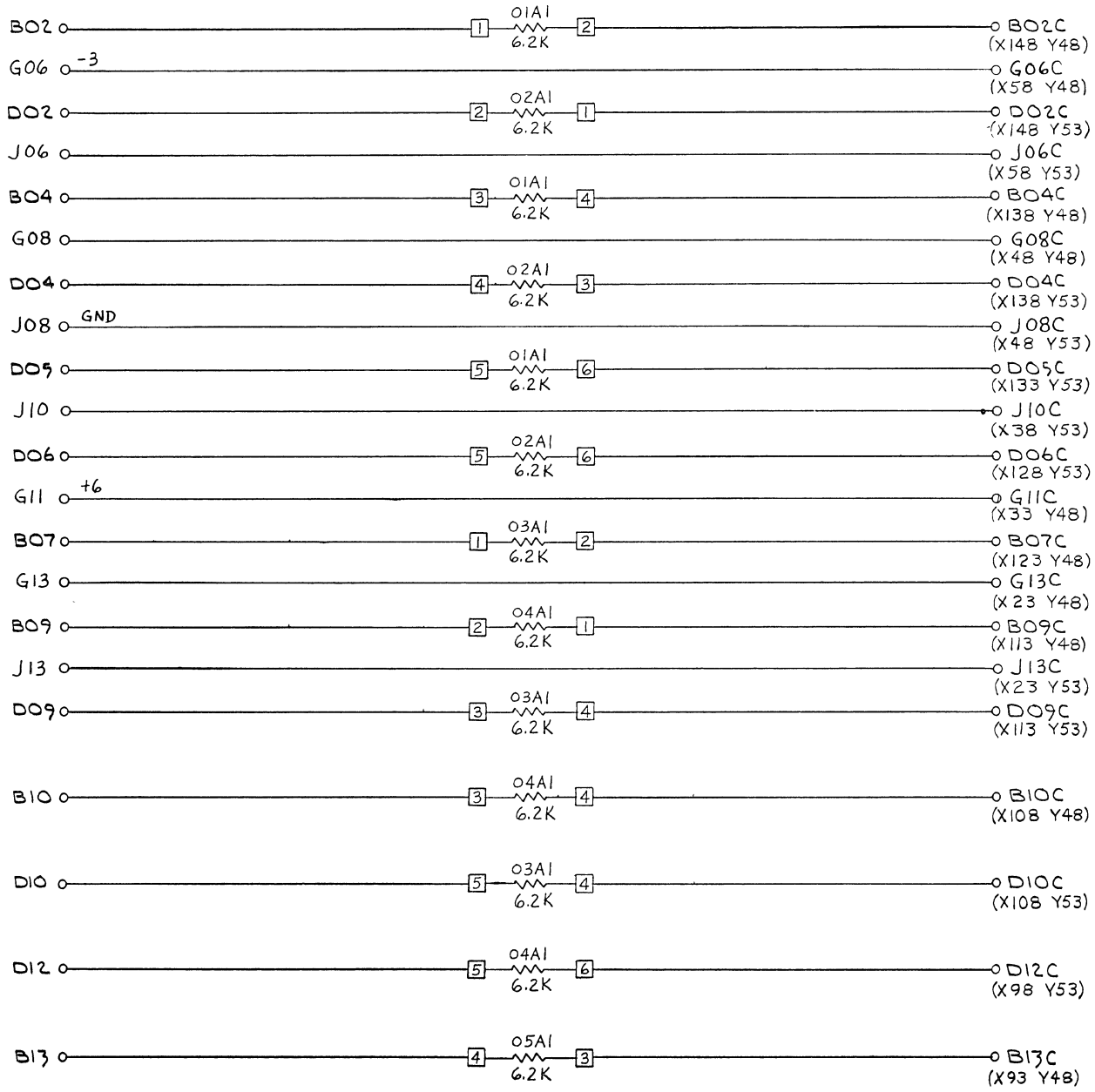
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
RES. CARD, CABLE TERMINATORS

P/N	5801246
EC	165508C



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6-AOI,II LATCH CARD

LMH (Cat.)	O-2860 (Subject)	283 (Suffix)

IBM Location Manufacturing Specification

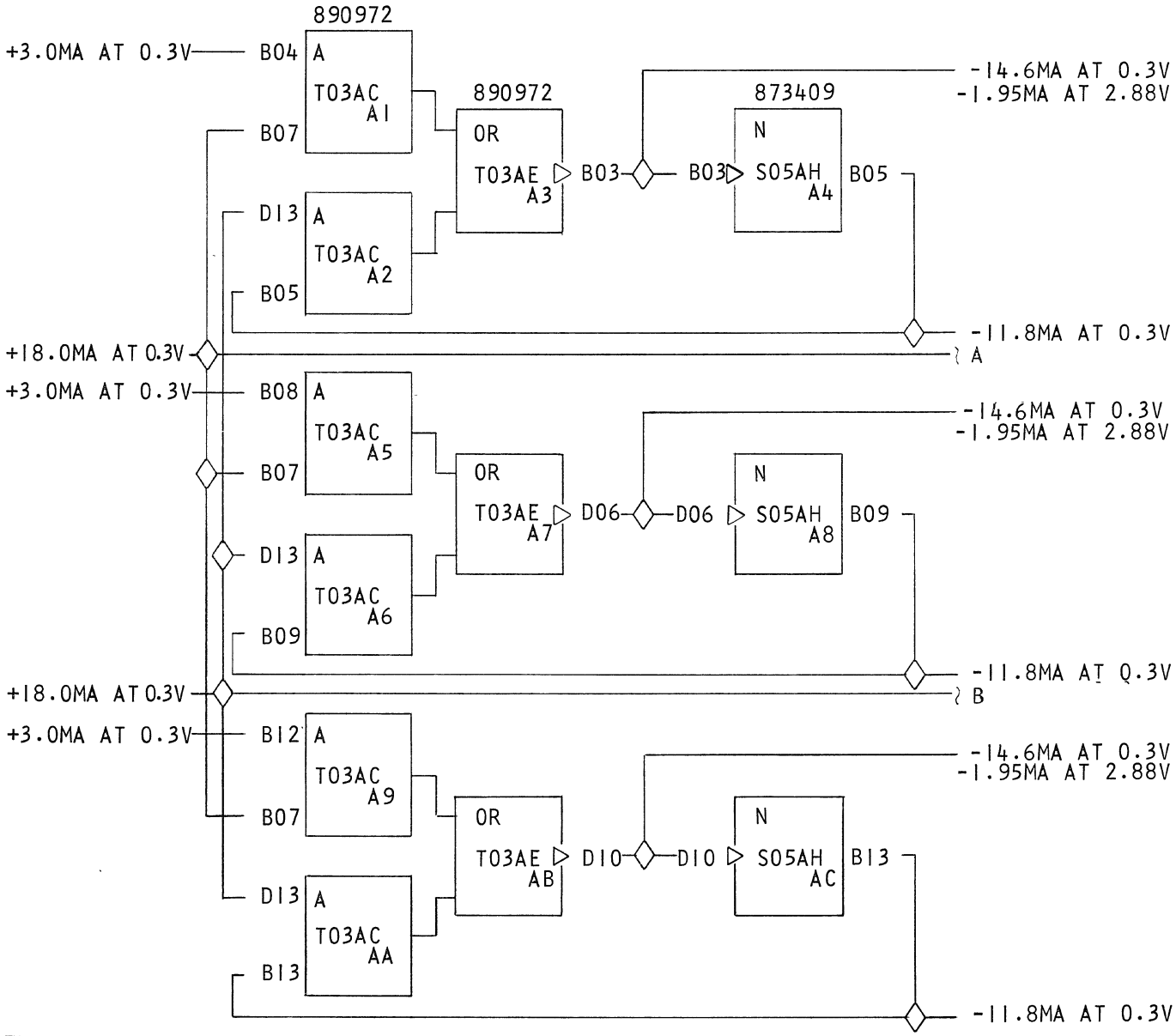
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

6-AOI,II LATCH CARD

CATEGORY CODE

T32

P/N	5801271
EC	162545A
STANDARD RESTRICTED	
CARD SIZE	1-12



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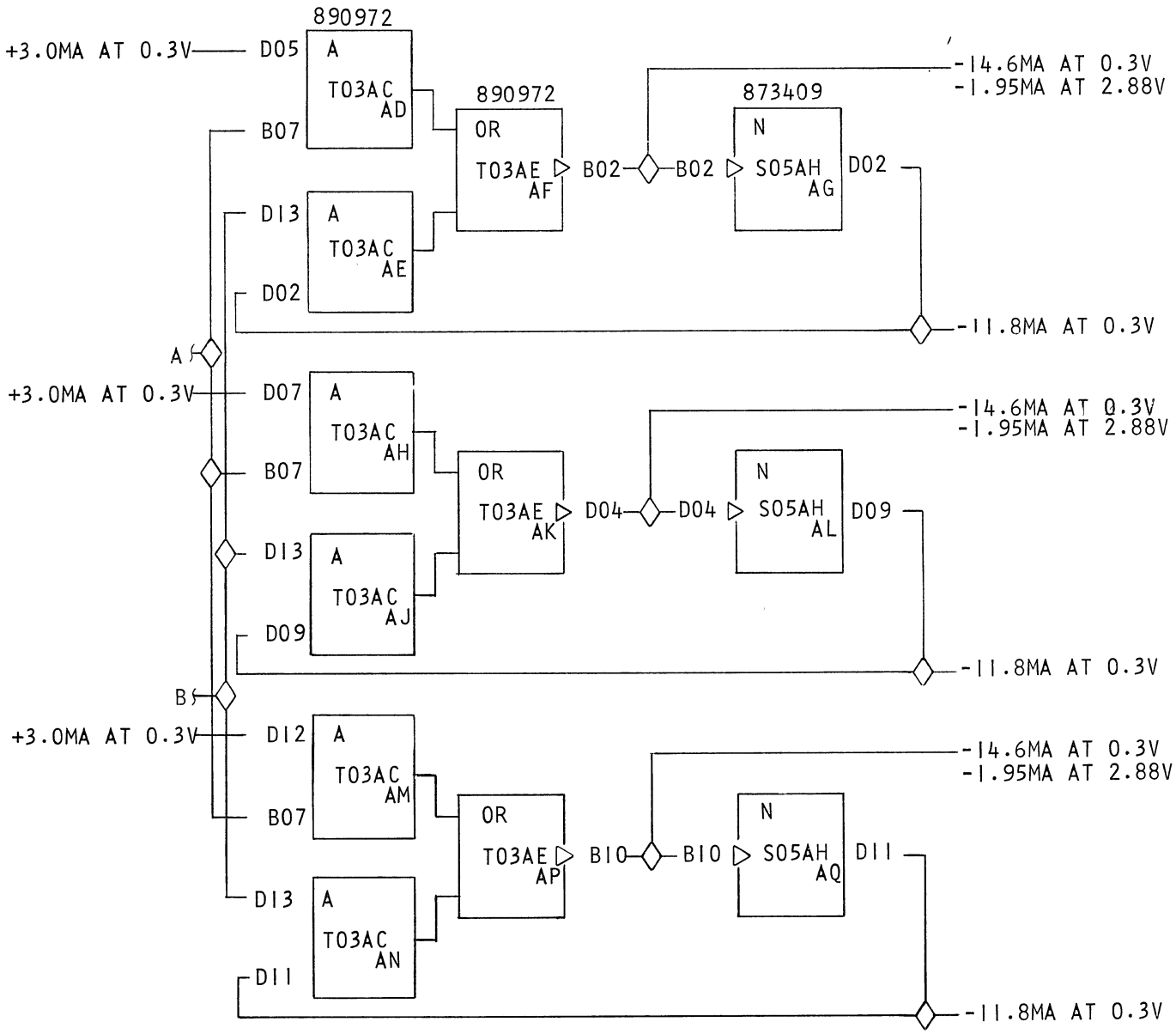
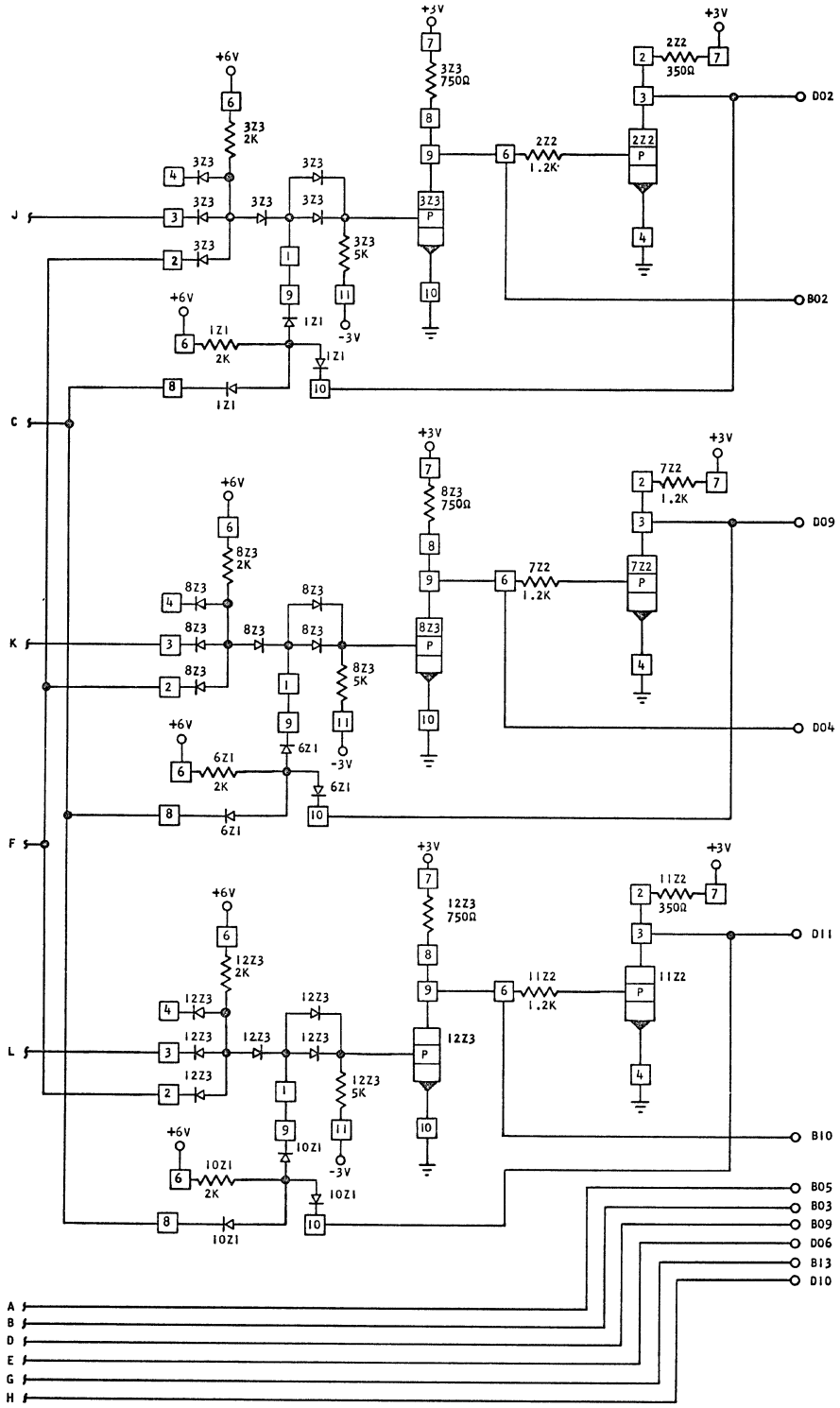
6-AOI,II LATCH CARD

T32

P/N	5801271
EC	162545A



P/N	5801271
EC	162545A

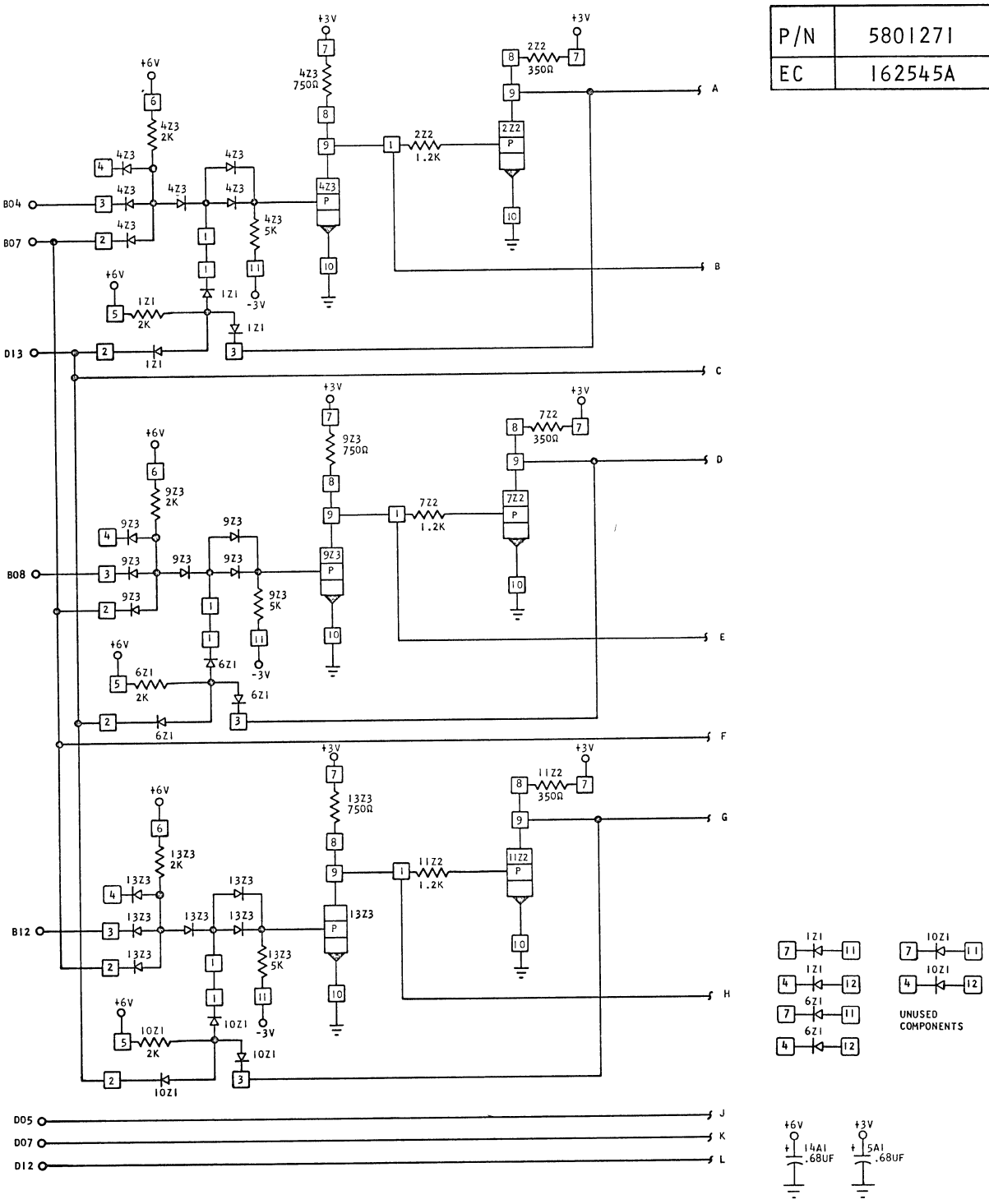


Printed in U.S.A.

LMH Cat.	0-2860 Subject	283 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6-AOI,II LATCH CARD

P/N	5801271
EC	162545A



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IBM Location Manufacturing Specification

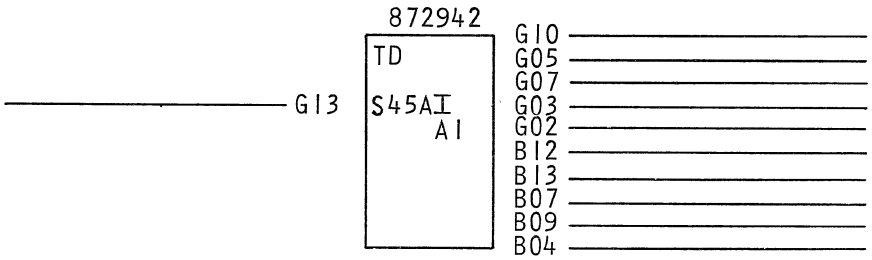
POWER REQUIRED	
PIN	VOLT
B06, G06	-3
B11, G11	+6
D03, J03	+3
D08, J08	GND

DELAY LINE (100 TO 1000NS)

CATEGORY CODE

S45

P/N	5801295
EC	163453
STANDARD	RESTRICTED
CARD SIZE	2-12

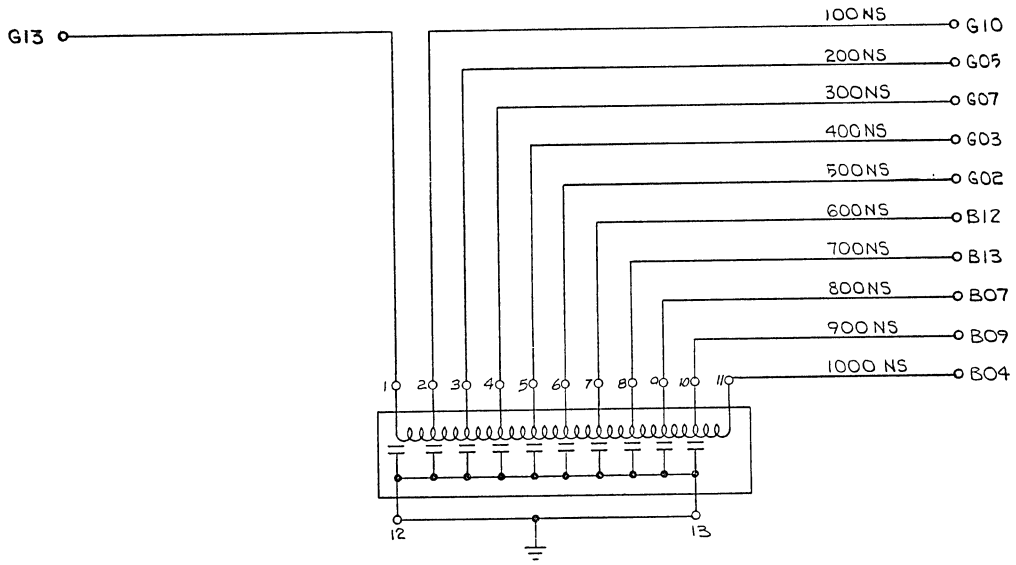


PIN	DELAY
G10	100NS
G05	200NS
G07	300NS
G03	400NS
G02	500NS
B12	600NS
B13	700NS
B07	800NS
B09	900NS
B04	1000NS

Note: The delay line should be terminated at the input and output with non-inductive resistors having a value equal to the lines nominal impedance.

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
DELAY LINE (100 TO 1000NS)

P/N	5801295
EC	163453



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1.0 AMP DRIVER

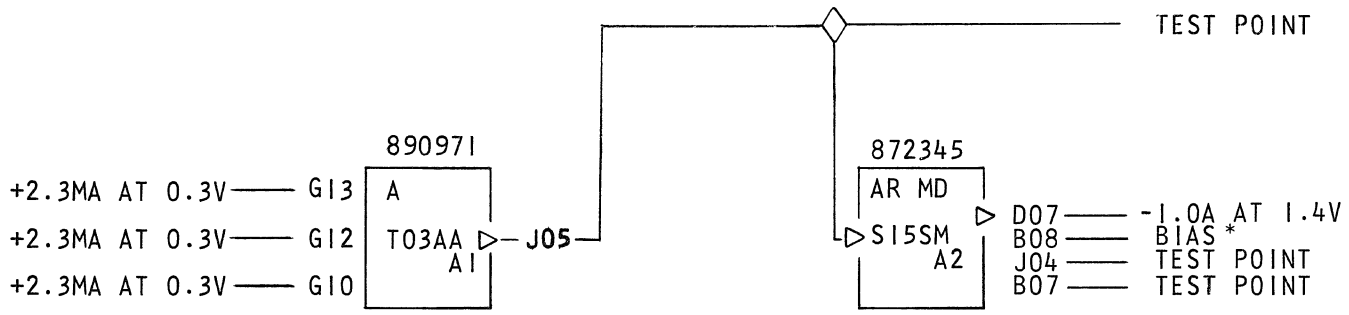
LMH (Cat.)	0-2860 (Subject)	286 (Suffix)

IBM **Location Manufacturing Specification**

POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1.0 AMP DRIVER	
CATEGORY CODE	
T03	S15

P/N	5801297
EC	162047A
SPECIAL RESTRICTED	
CARD SIZE	2-12



* Special ground connection to reduce noise rejection into logic circuits by separating the high current ground from the logic ground.

06-09 Primary Standards Manual	Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		ENDICOTT Responsibility	12-68 Date	1 OF 2 Page

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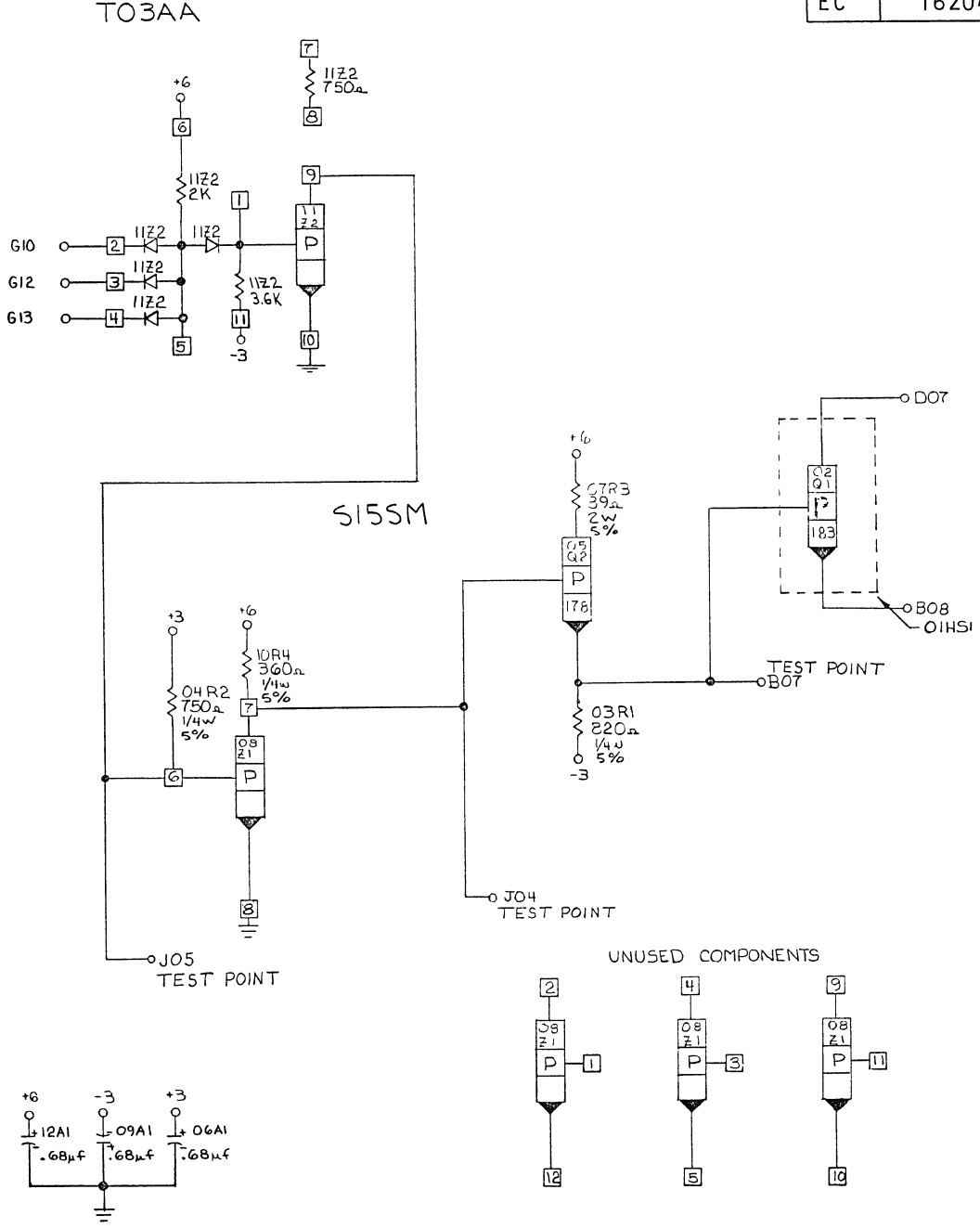
LMH Cat.	0-2860 Subject	286 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1.0 AMP DRIVER

P/N	5801297
EC	162047A



2 OF 2 Page	12-68 Date

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
3 MPLX INTF DRVS WO/L & 3-1W AOI & 5-95 OHM TRMNTRS

LMH	0-2860	292
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

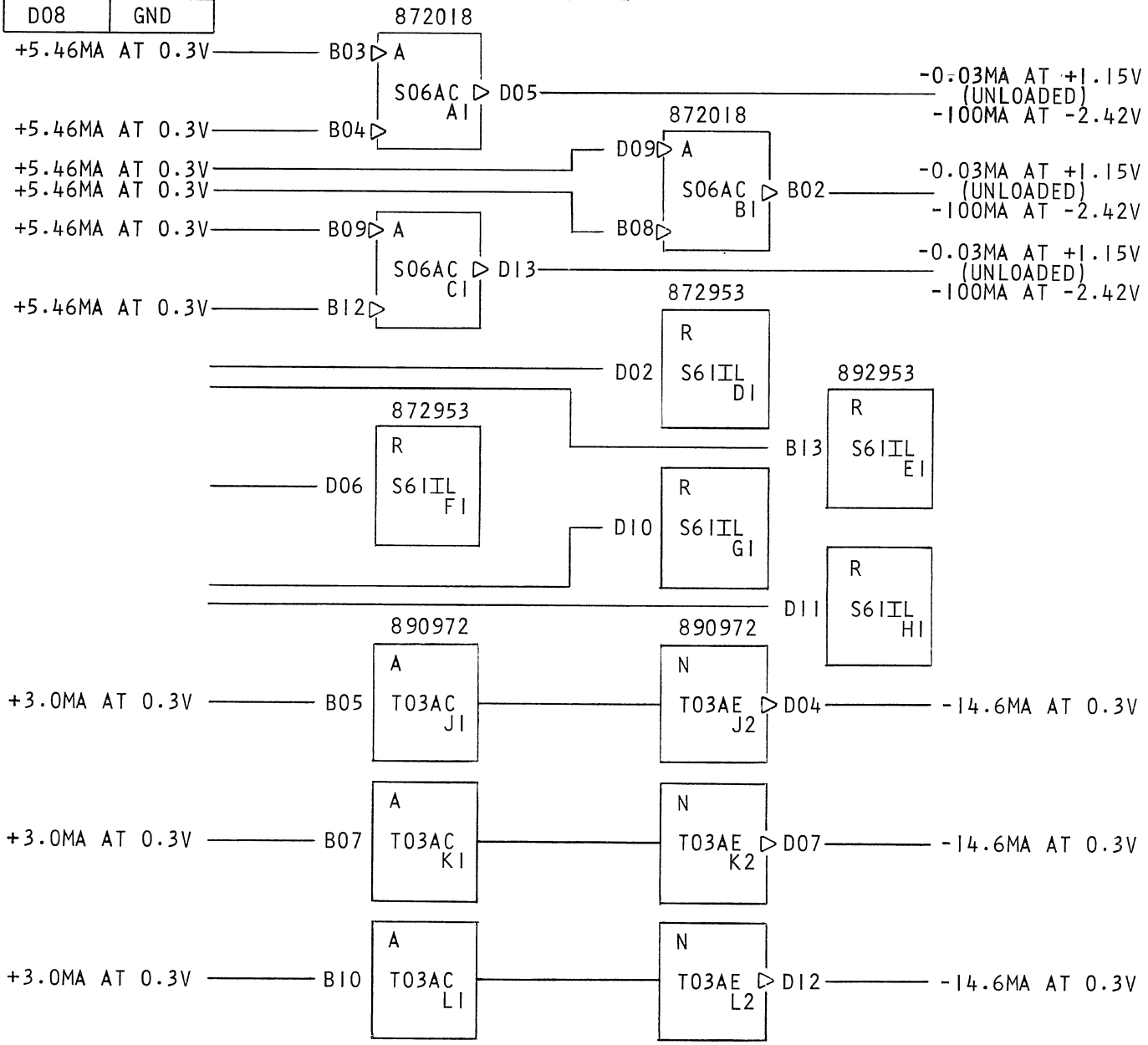
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

3 MPLX INTERFACE DRIVERS WO/L &
3-1W AOI & 5-95 OHM TERMINATORS

CATEGORY CODE

S06	T03

P/N	5801655
EC	165656
SPECIAL	RESTRICTED
CARD SIZE	1-12



06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		Responsibility: ENDICOTT	Date: 1-67	Page: 1 of 2

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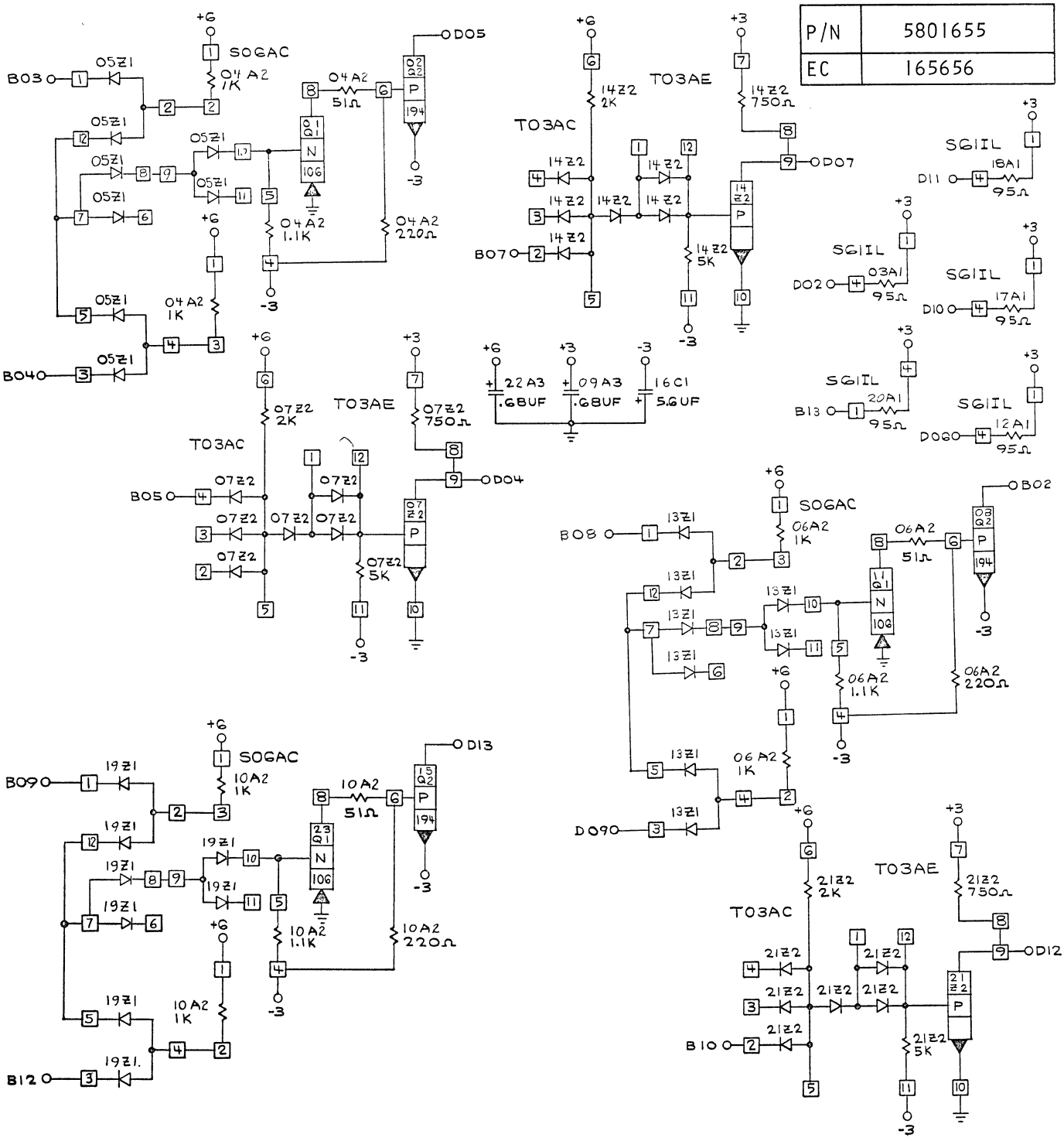
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
3 MPLX INTF DRVS W0/L & 3-1W AOI & 5-95 OHM TRMNTRS

P/N	5801655
EC	165656



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6 SEQUENCED MULTIPLEX LINE DRIVERS

LMH	0-2860	293
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

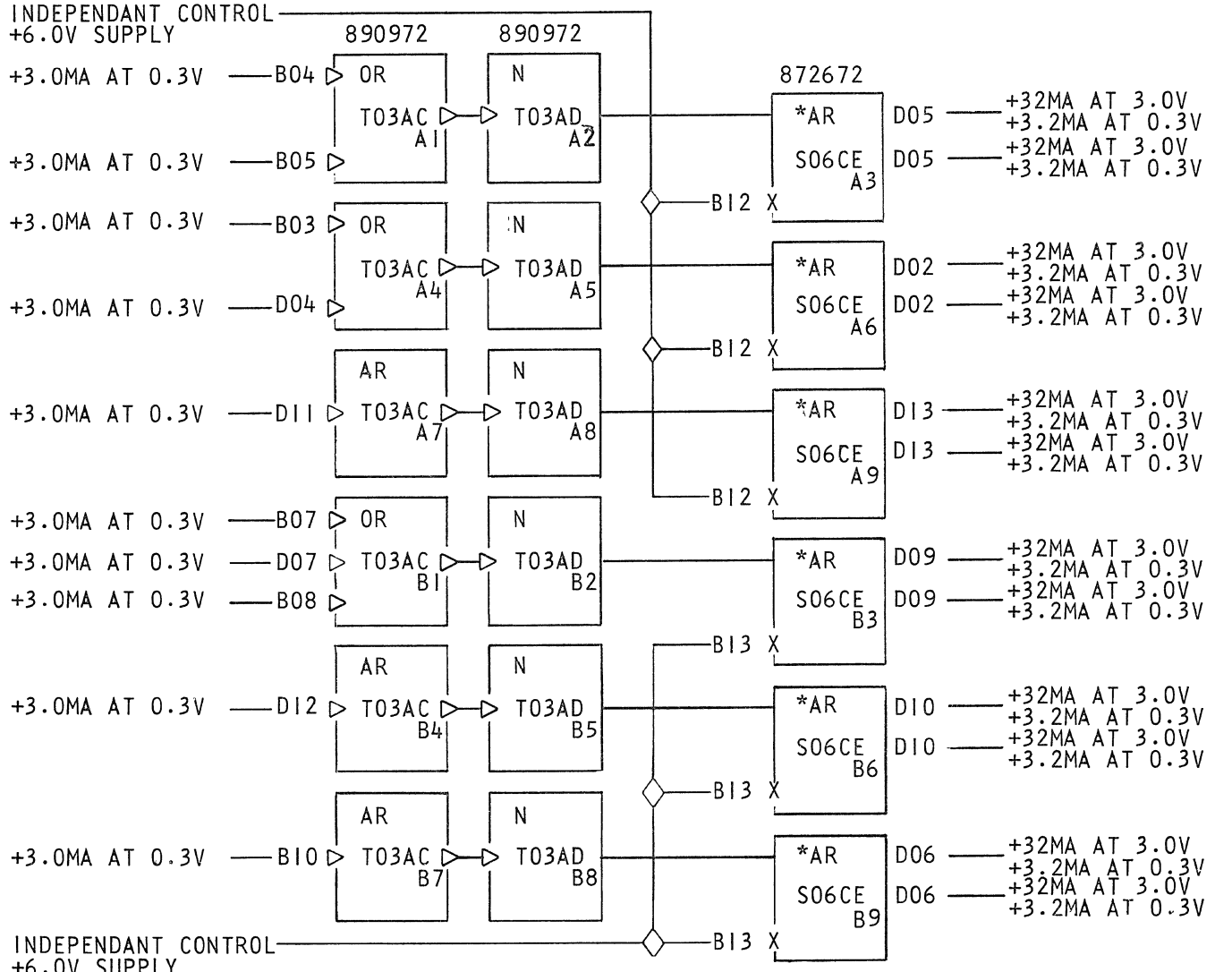
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

6 SEQUENCED MULTIPLEX LINE DRIVERS

CATEGORY CODE

S03

P/N	5801664
EC	165680C
SPECIAL	RESTRICTED
CARD SIZE	1-12



NOTE: A 95 OHM RESISTOR TO GND MUST BE CONNECTED TO THE OUTPUT AT EACH EXTREME END OF THE COAX CABLE.

A MAXIMUM OF 14 MULTIPLEX RECEIVERS CAN BE DRIVEN BY EACH DRIVER.

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
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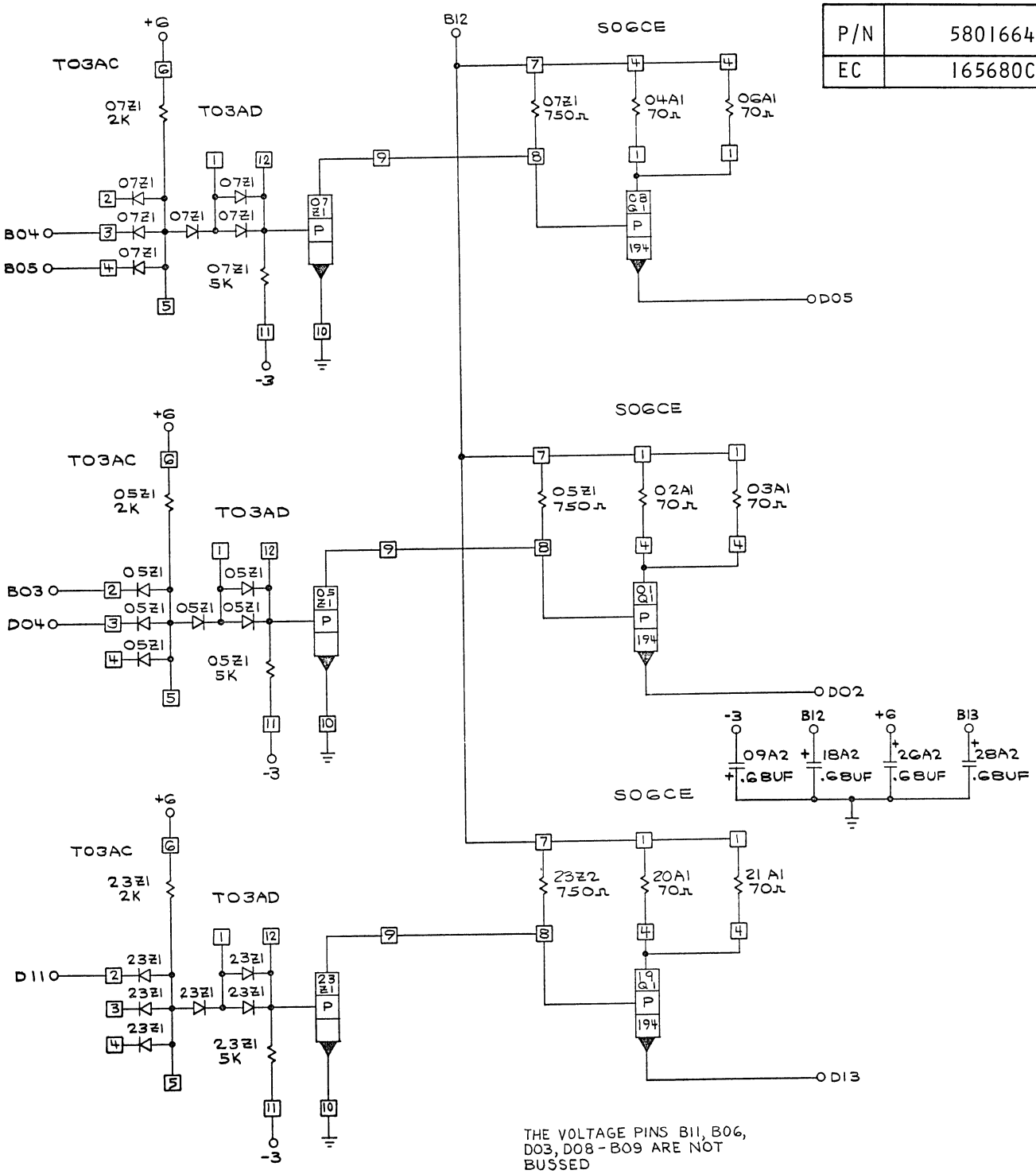
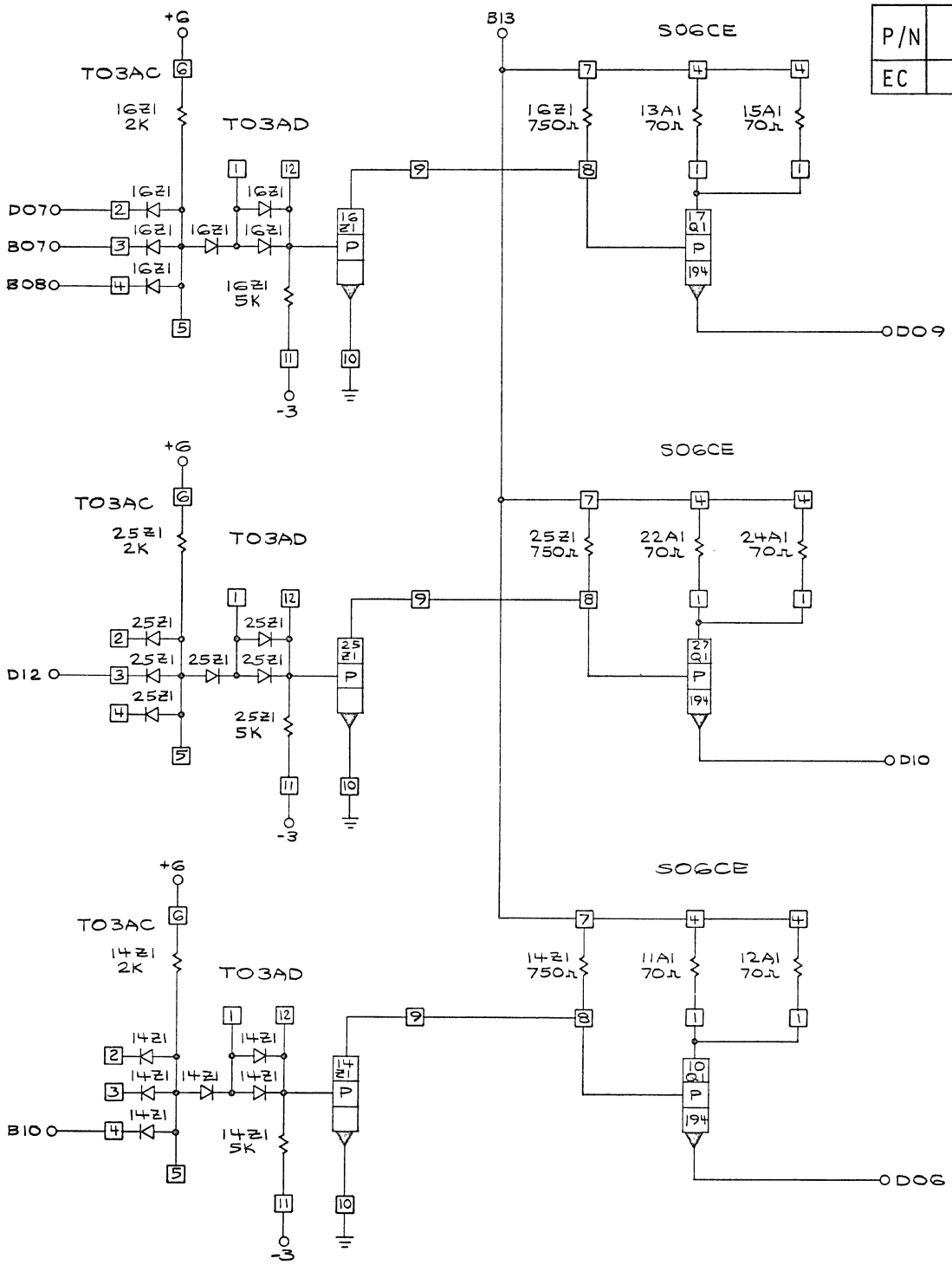
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6 SEQUENCED MULTIPLEX LINE DRIVERS

P/N	5801664
EC	165680C



THE VOLTAGE PINS B11, B06, D03, D08 - B09 ARE NOT BUSSED

P/N	5801664
EC	165680C



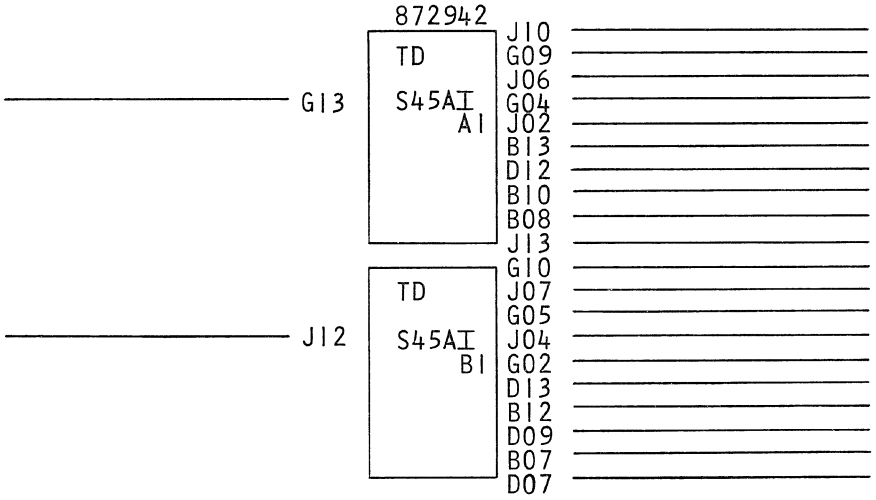
POWER REQUIRED	
PIN	VOLT
D08	GND
J08	GND

2-DELAY LINES (100 TO 1000 NS)

CATEGORY CODE

S45

P/N	5801671
EC	164252
STANDARD RESTRICTED	
CARD SIZE	2-24



INPUT PIN	OUTPUT PIN	DELAY
G13	J10	100NS
G13	G09	200NS
G13	J06	300NS
G13	G04	400NS
G13	J02	500NS
G13	B13	600NS
G13	D12	700NS
G13	B10	800NS
G13	B08	700NS
G13	J13	1000NS

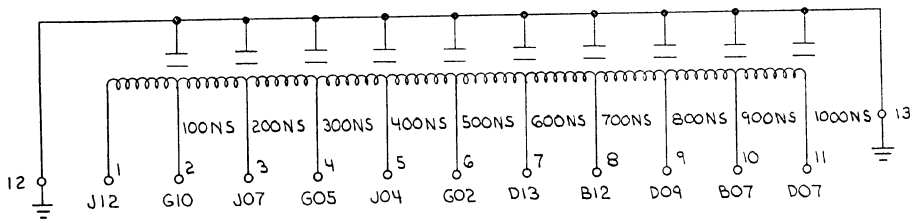
INPUT PIN	OUTPUT PIN	DELAY
J12	G10	100NS
J12	J07	200NS
J12	G05	300NS
J12	J04	400NS
J12	G02	500NS
J12	D13	600NS
J12	B12	700NS
J12	D09	800NS
J12	B07	900NS
J12	D07	1000NS

Note: The delay line should be terminated at the input and output with non-inductive resistors having a value equal to the lines nominal impedance.

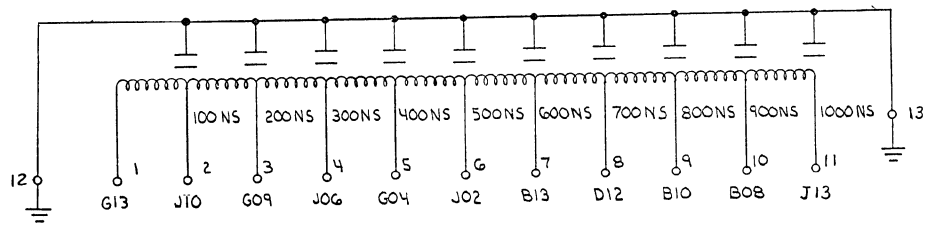
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-DELAY LINES (100 TO 1000 NS)

P/N	5801671
EC	164252

S45AI
1DL1



S45AI
2DL1



IBM

Location Manufacturing Specification

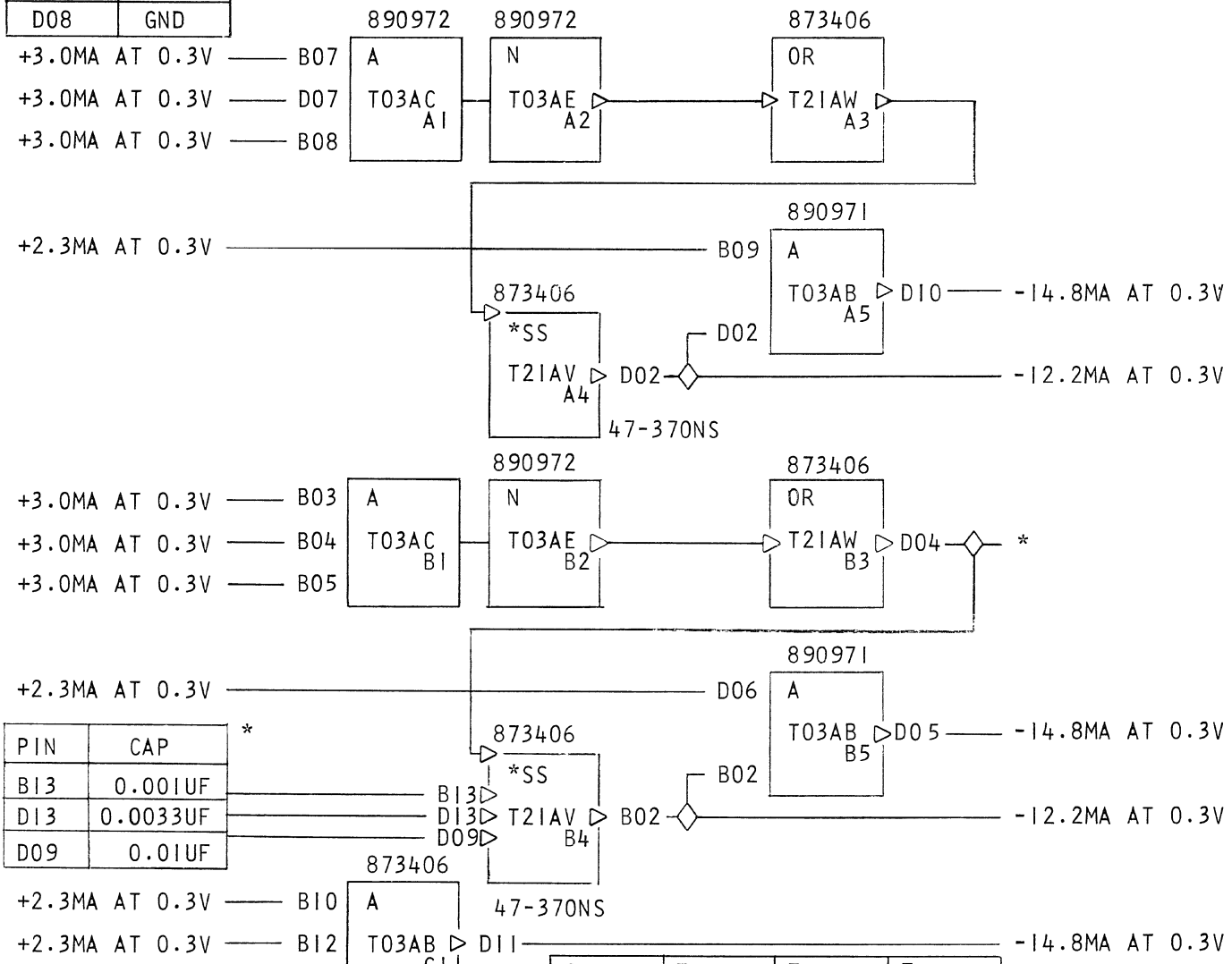
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

SSI 47-370NS & SS2 47NS-120US

CATEGORY CODE

T21

P/N	5801697
EC	164699
STANDARD RESTRICTED	
CARD SIZE	1-12



*

PIN	CAP
B13	0.001UF
D13	0.0033UF
D09	0.01UF

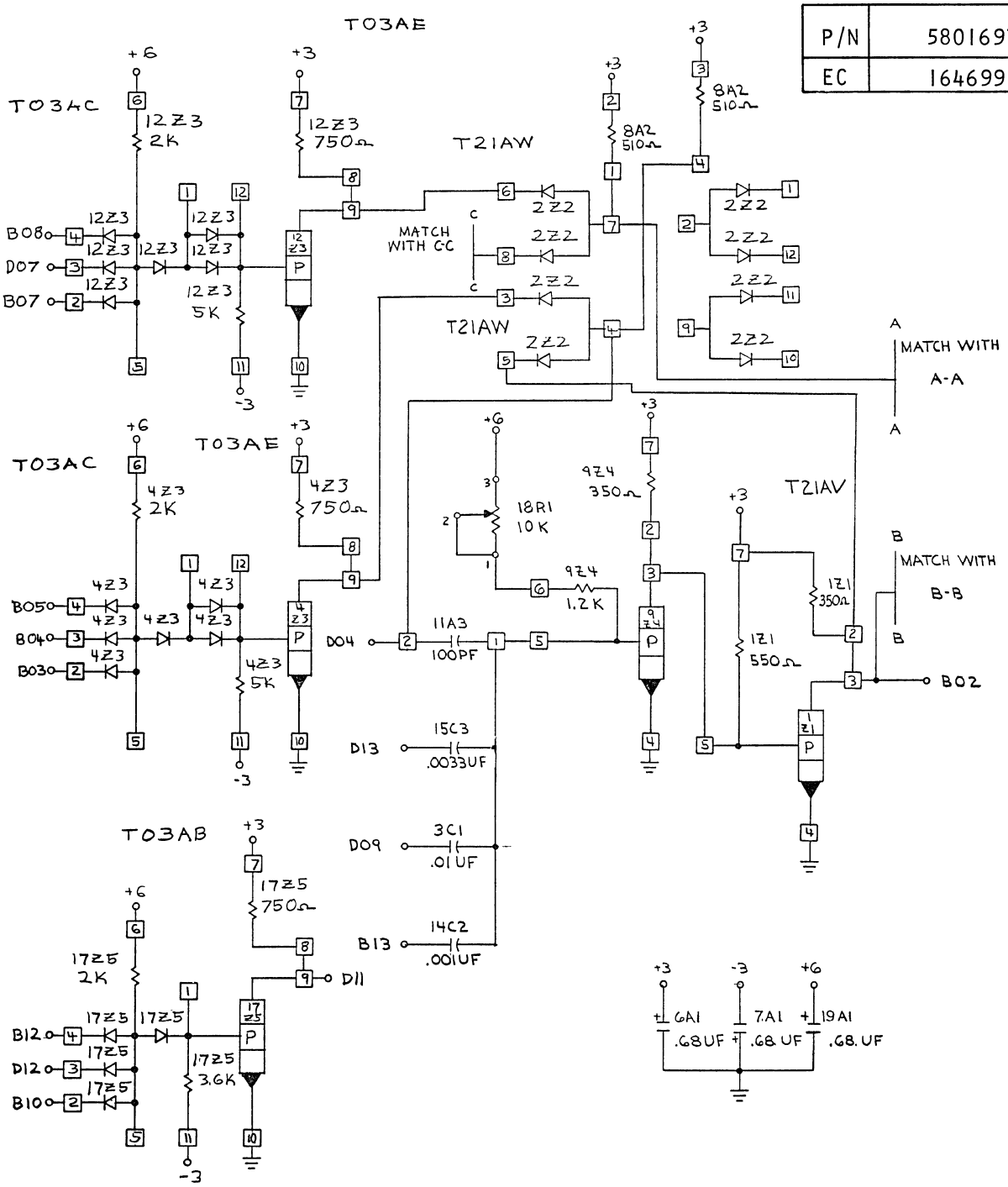
*TIE TO ADDITIONAL CAPACITORS IF REQUIRED

C_T	T_{MAX}	T_{MIN}	T_R MIN
100PF	370NS	47NS	190NS
.001UF	3.7US	470NS	1.9US
.0033UF	12US	1.45US	6.2US
.01UF	37US	4.6US	19US

TABLE OF OUTPUT PULSE WIDTHS AND RECOVERY TIMES

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
SS1 47-370NS & SS2 47NS-120US

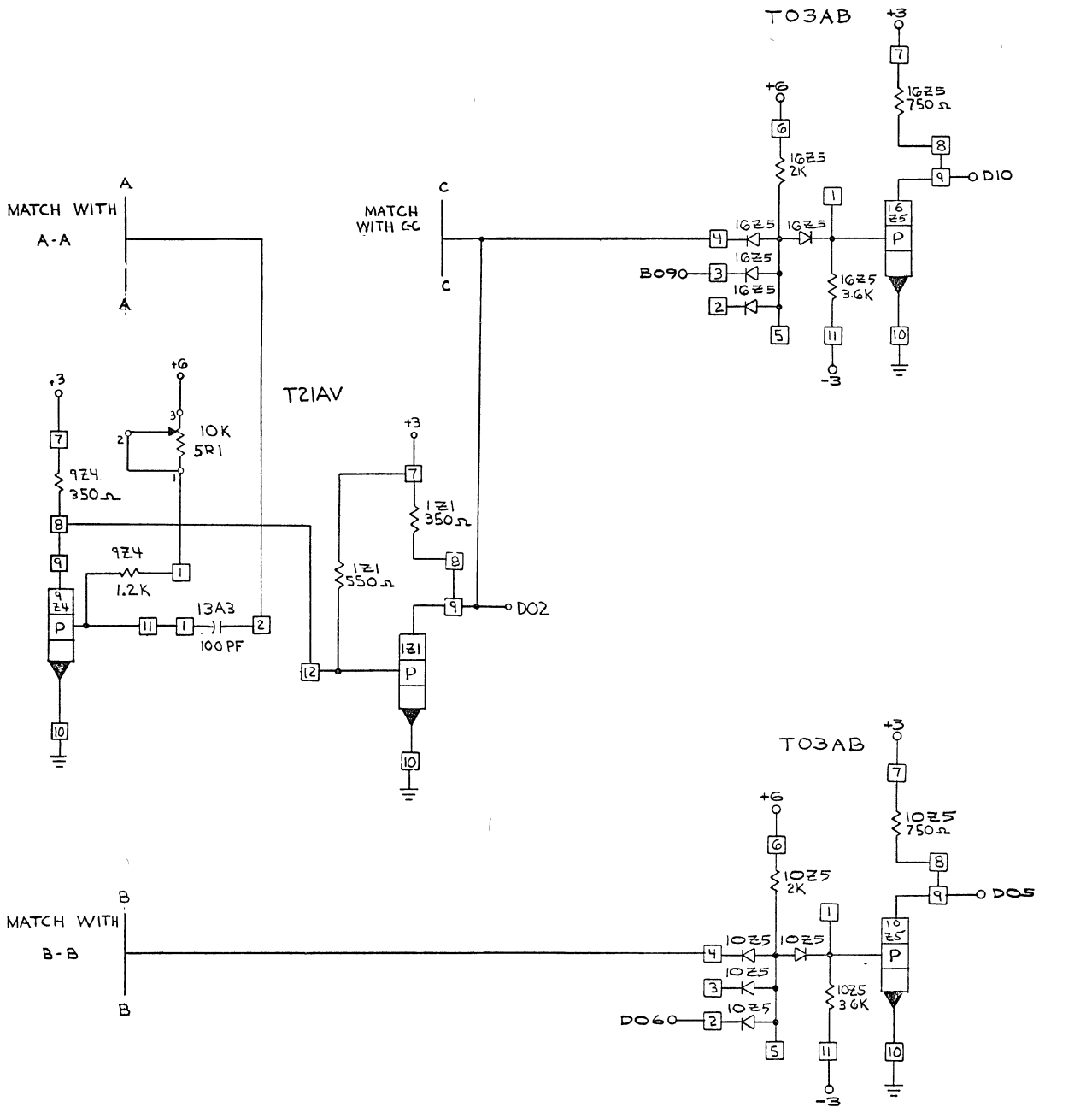
P/N	5801697
EC	164699



IBM

Location
Manufacturing Specification

P/N	5801697
EC	164699



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POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

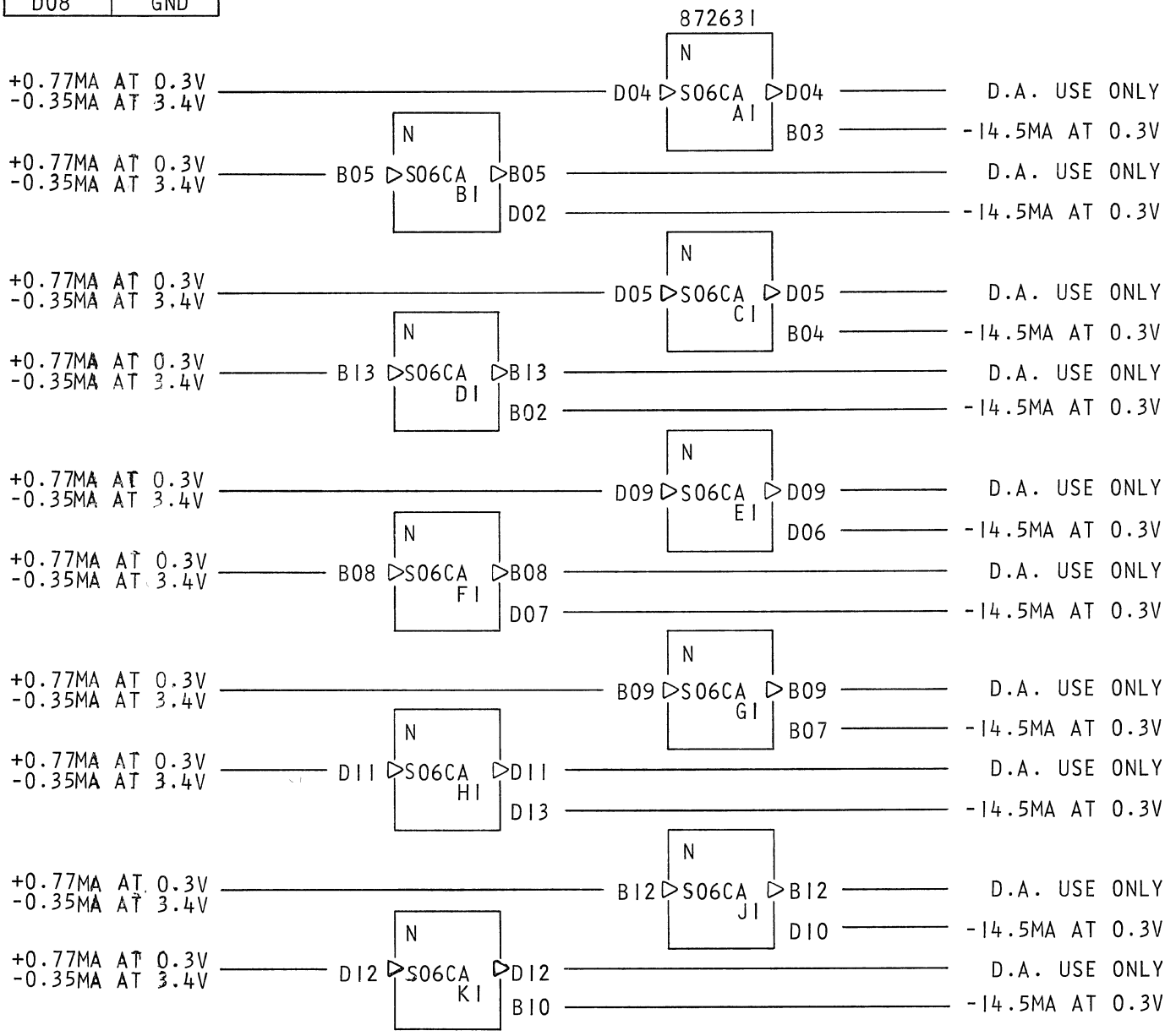
10 MULTIPLEX RECEIVERS

CATEGORY CODE

S06

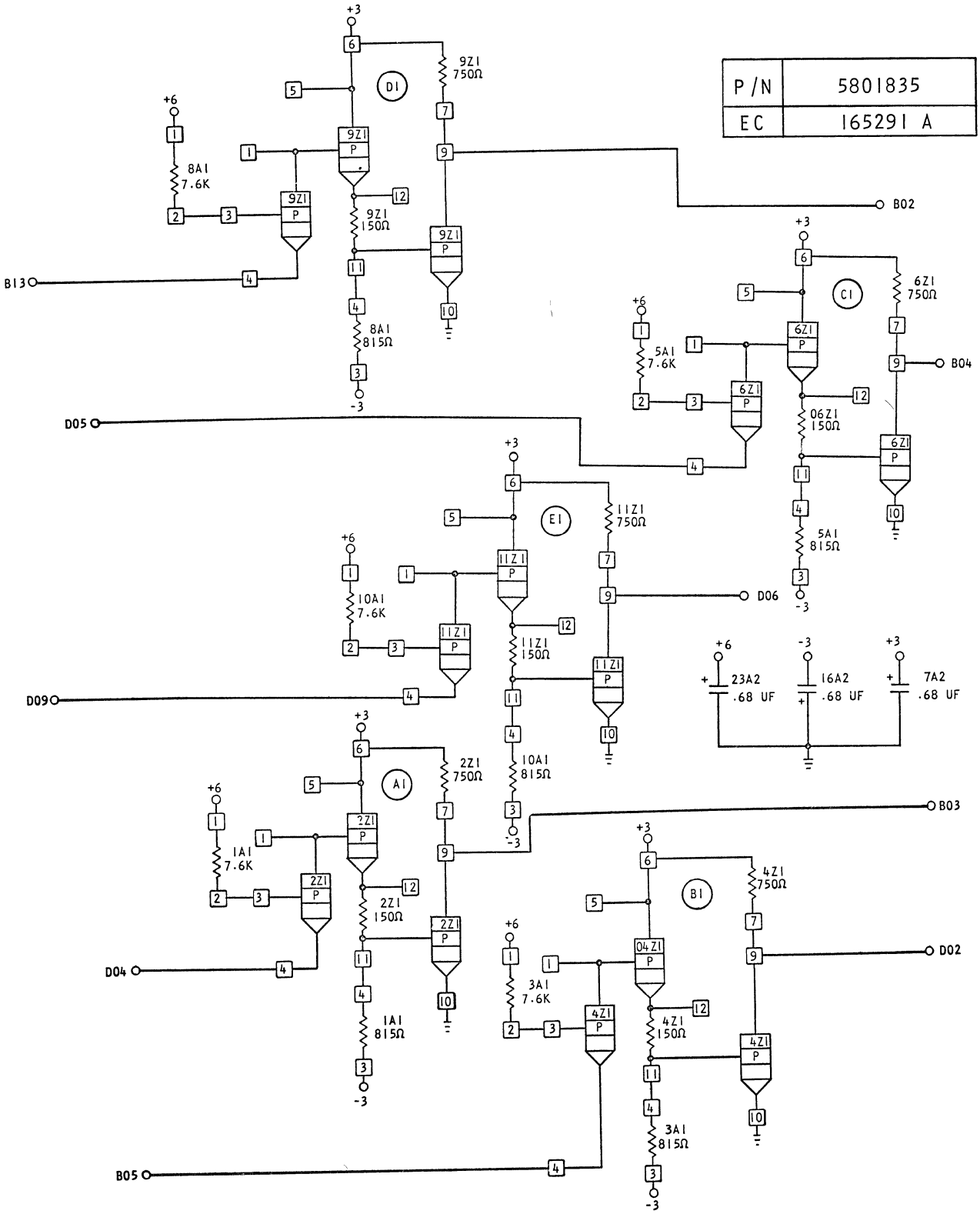
P/N	5801835
EC	165291A
SPECIAL RESTRICTED	
CARD SIZE	1-12

872631

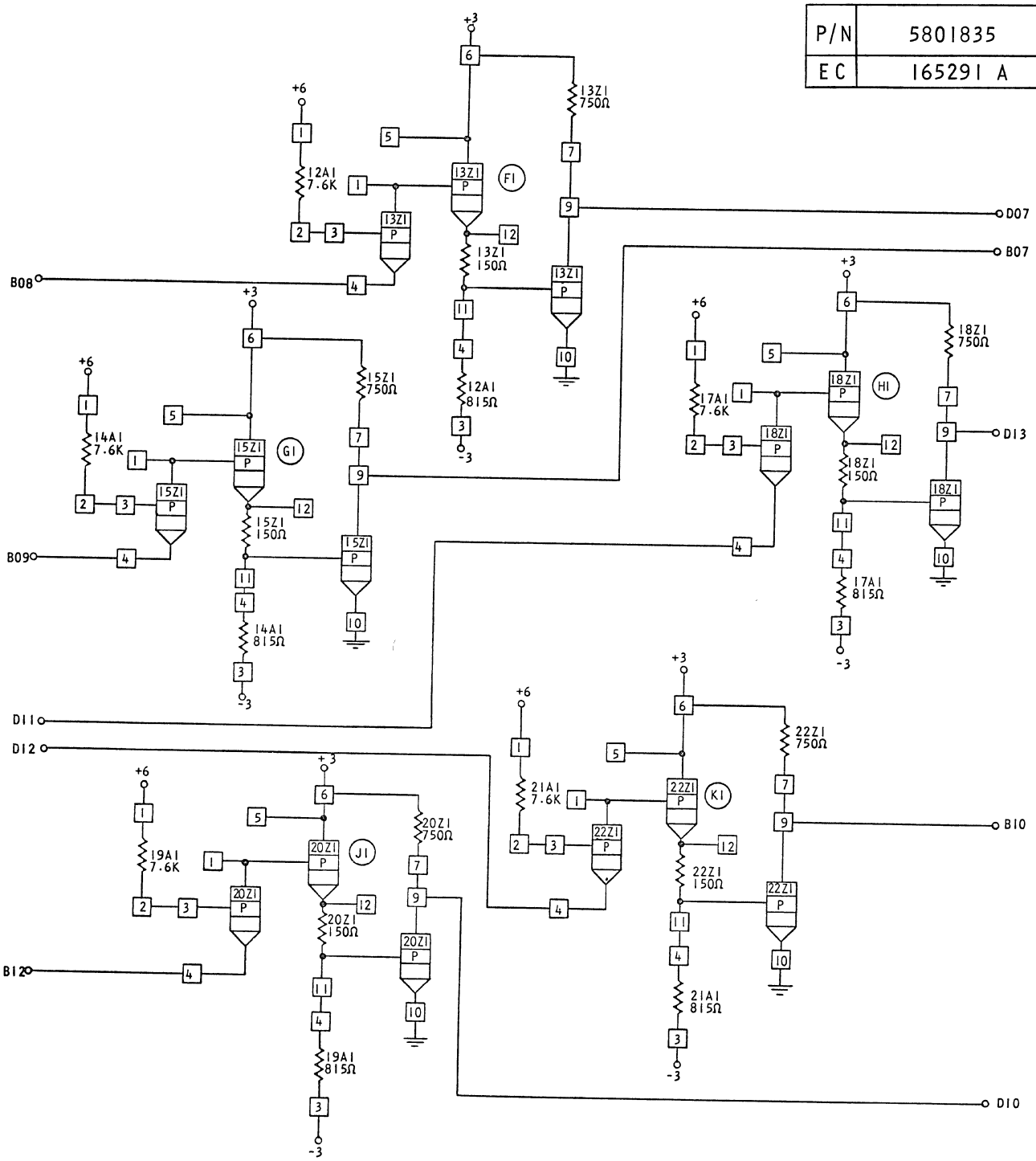


SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
10 MULTIPLEX RECEIVERS

P/N	5801835
EC	165291 A



P/N	5801835
EC	165291 A



SLT LOGIC DIAGRAM & SCHEMATIC -EQUIPMENT ENGINEERING
20-82 OHM RESISTOR TERMINATORS TO +3V

LMH Cat.	0-2860 Subject	300 Suffix

IBM **Location Manufacturing Specification**

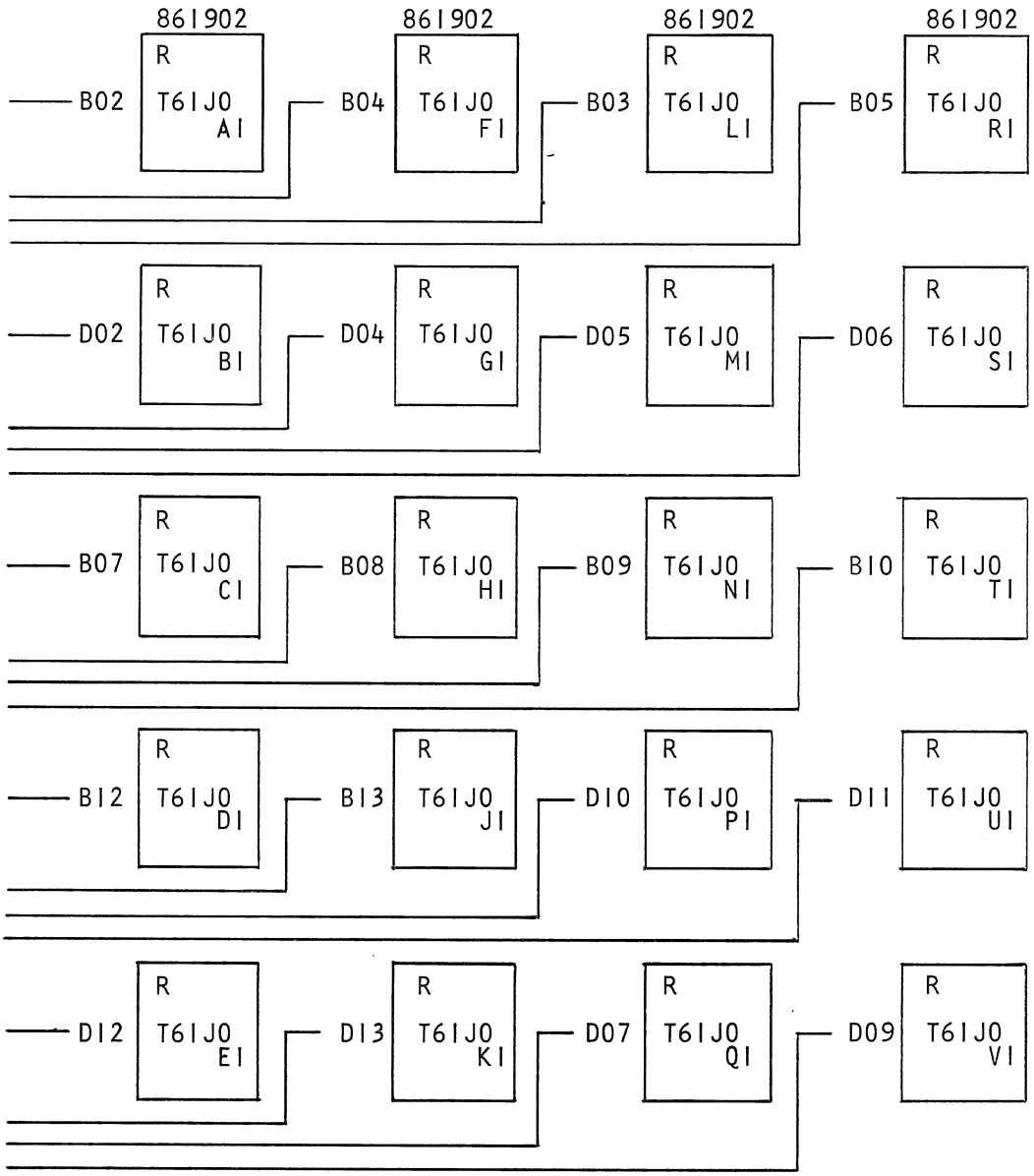
POWER REQUIRED	
PIN	VOLTS
D03	+3
D08	GND

20-82 OHM RESISTOR TERMINATORS TO +3V

CATEGORY CODE

T6I

P/N	5801883
EC	168029A
STANDARD ACTIVE	
CARD SIZE	I-12



* MAXIMUM LOAD CURRENT AT 0.3V = 36MA

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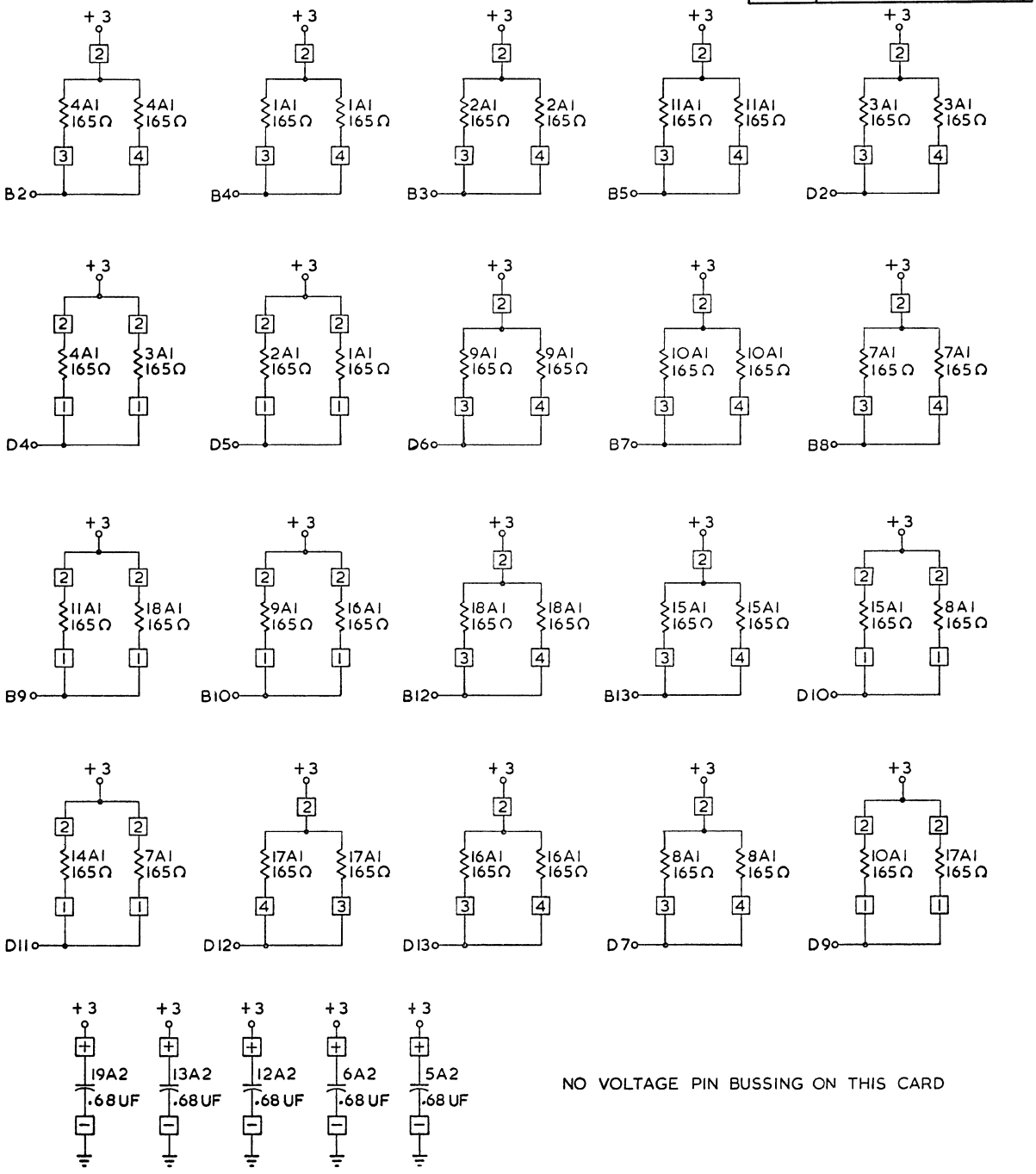
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
20--82 OHM RESISTOR TERMINATORS TO +3V

P/N	5801883
EC	168029A

T61JO



NO VOLTAGE PIN BUSSING ON THIS CARD

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
170 K HZ OSCILLATOR

LMH Cat.	0-2860 Subject	301 Suffix

IBM

Location

Manufacturing Specification

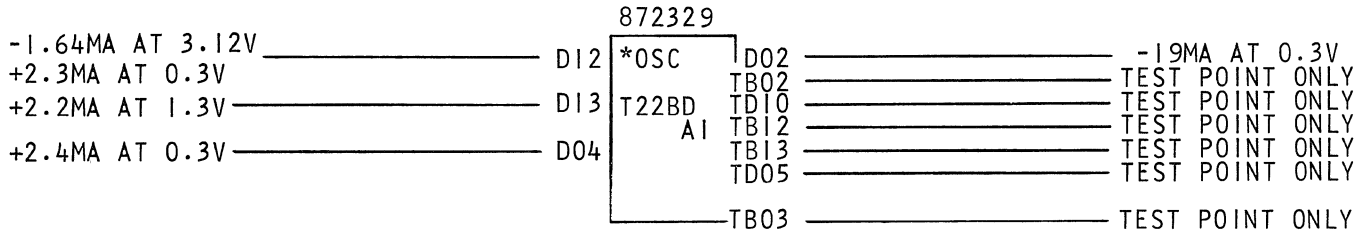
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

170 K HZ OSCILLATOR

CATEGORY CODE

T22

P/N	5803011
EC	162906
SPECIAL RESTRICTED	
CARD SIZE	1-12



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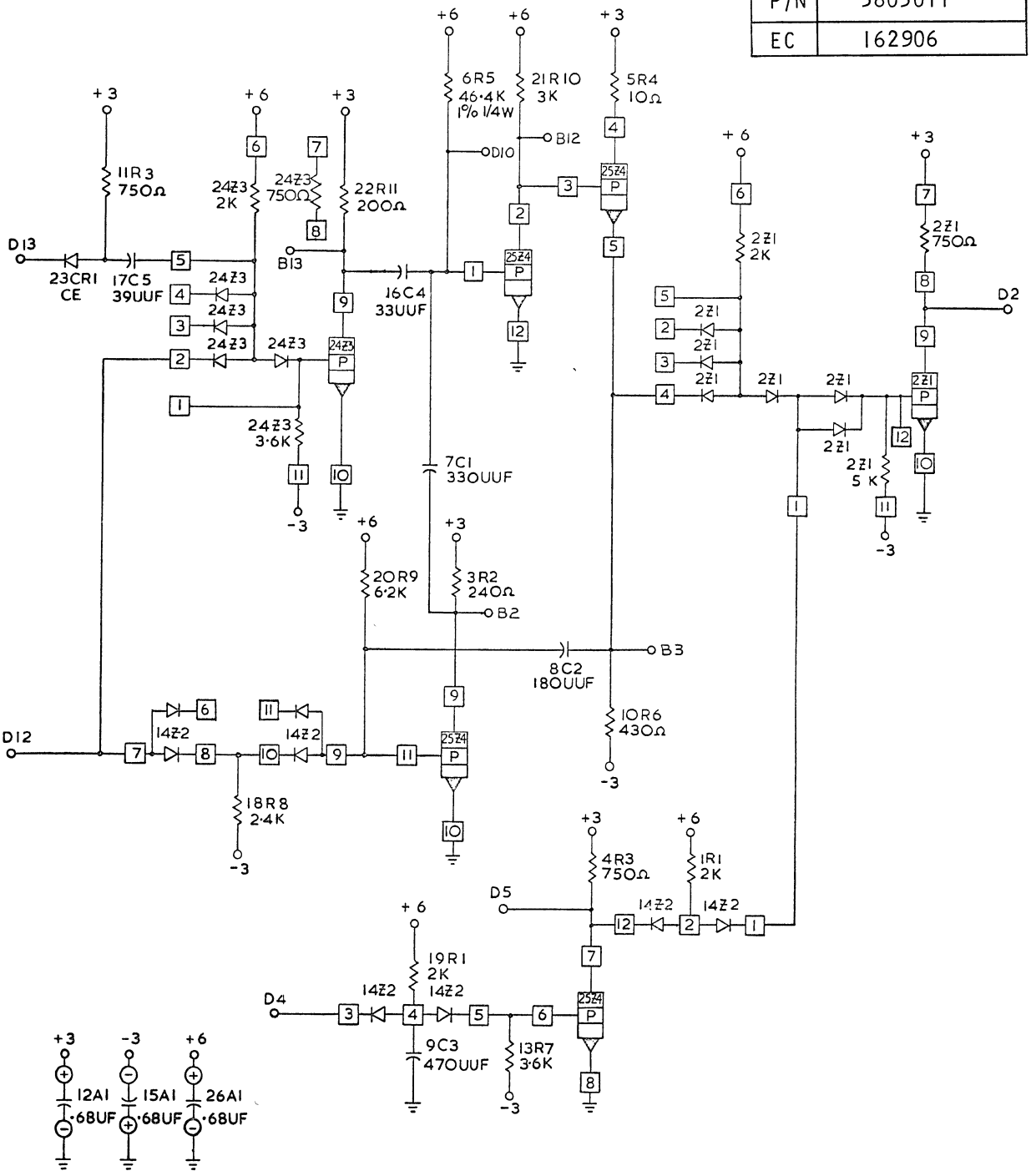
LMH Cat.	0-2860 Subject	301 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
170 K HZ OSCILLATOR

P/N	5803011
EC	162906



Page 2	Date Jan. 67

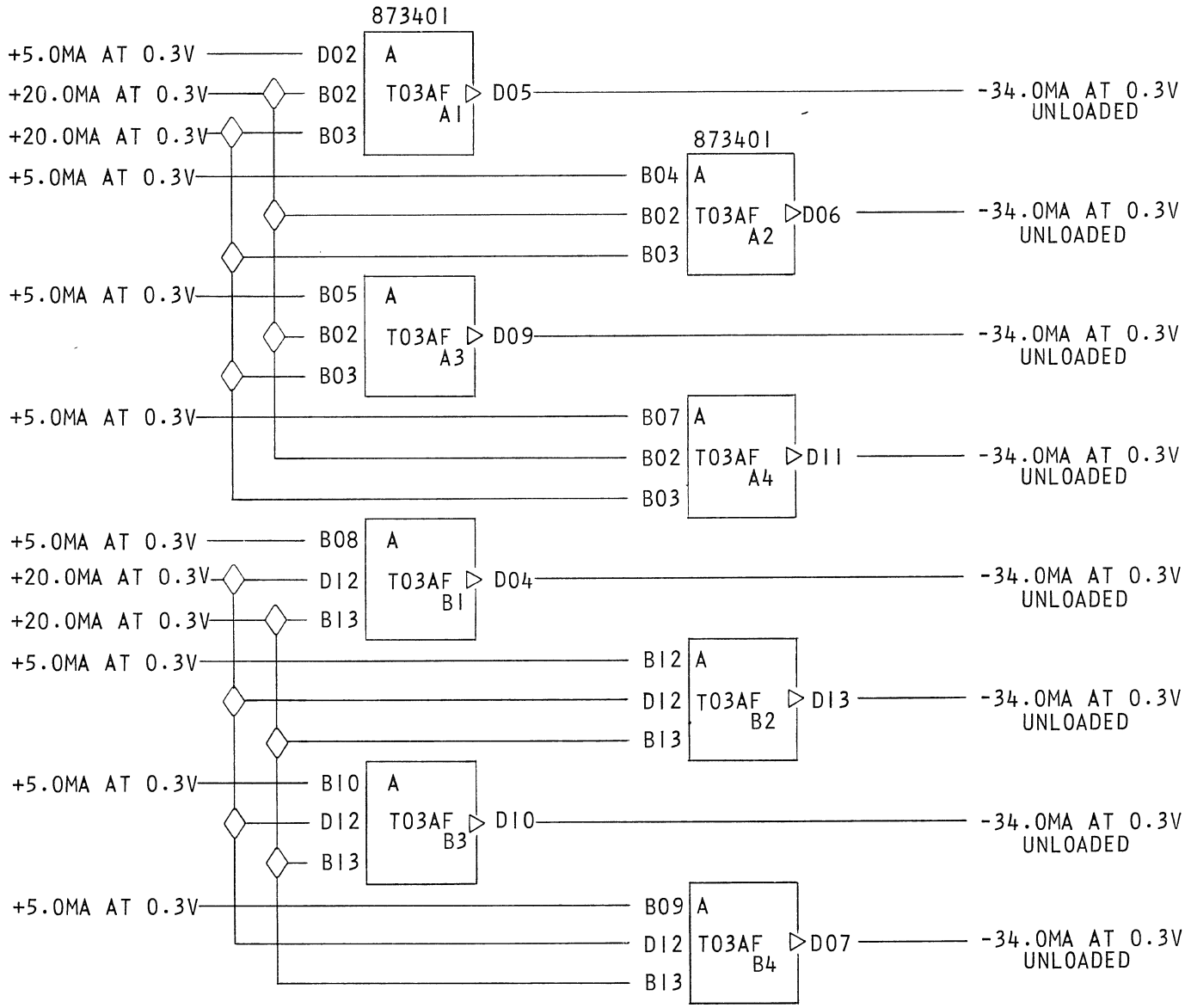
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

4-3W,4-3W GATED API WO/L

CATEGORY CODE

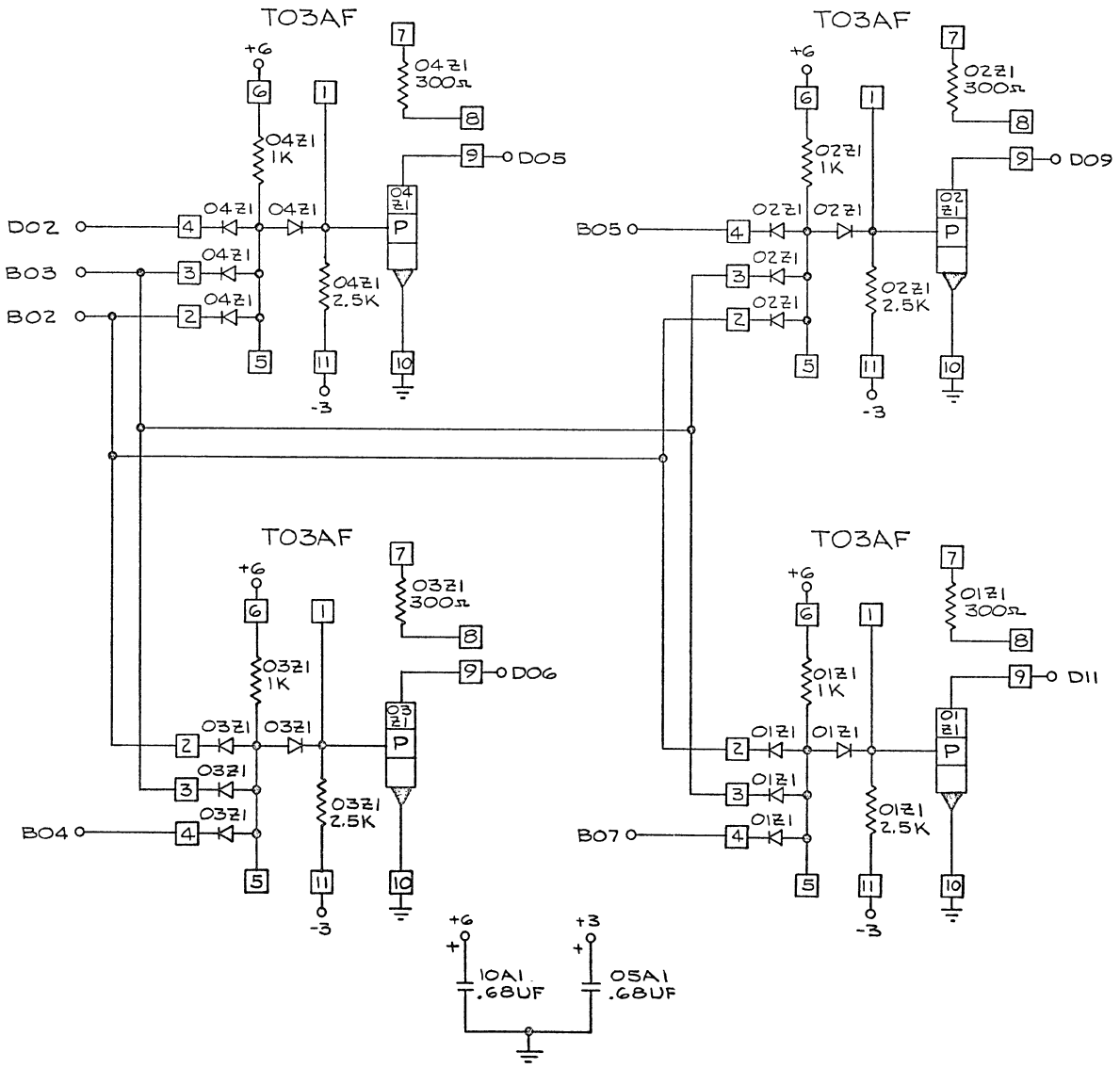
T03

P/N	5803024
EC	161933
STANDARD RESTRICTED	
CARD SIZE	1-12



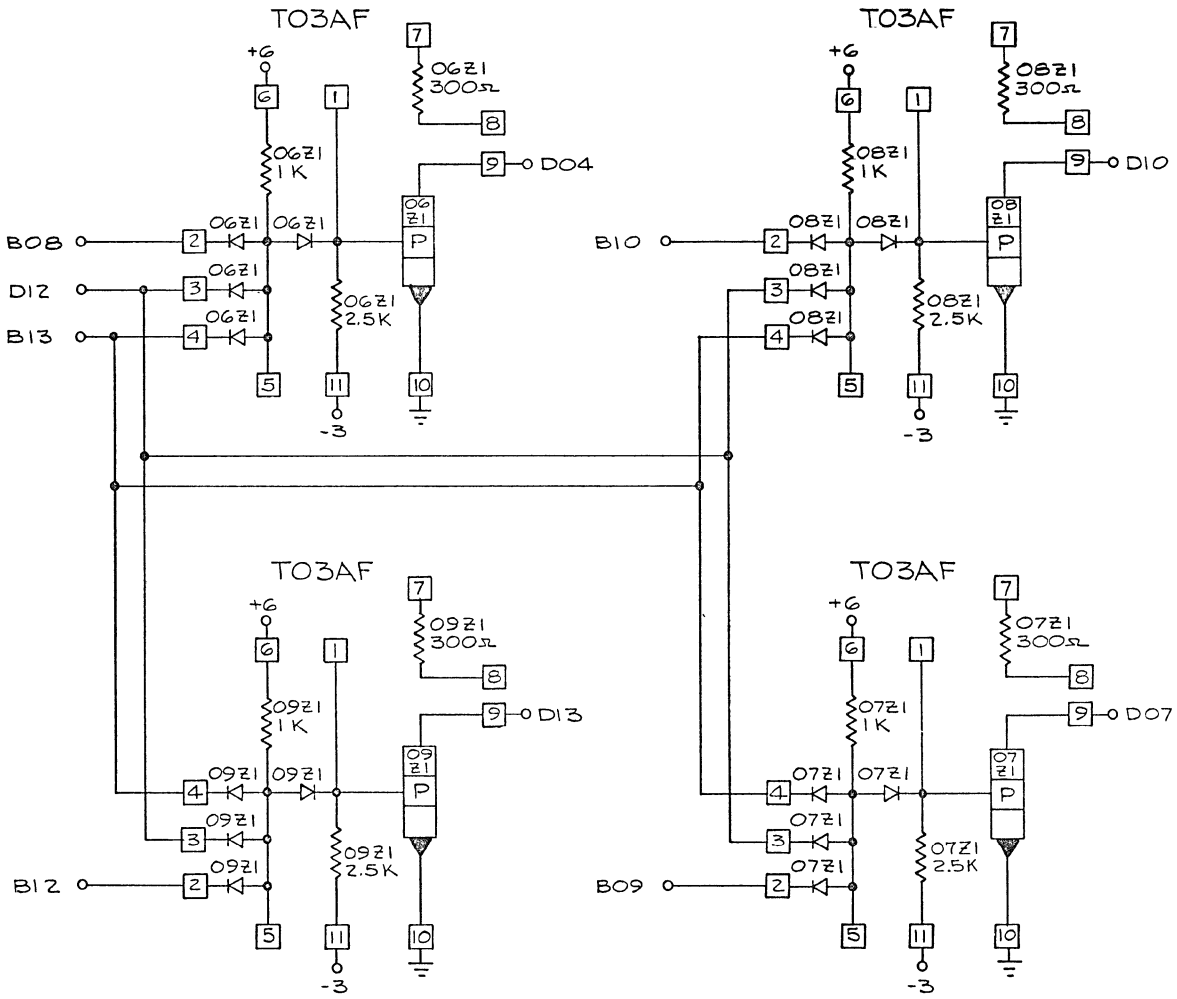
LMH	0-2860	304	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
Cat.	Subject	Suffix	4-3W,4-3W GATED API W0/L

P/N	5803024
EC	161933



2 OF 3	1-67	
Page	Date	

P/N	5803024
EC	161933



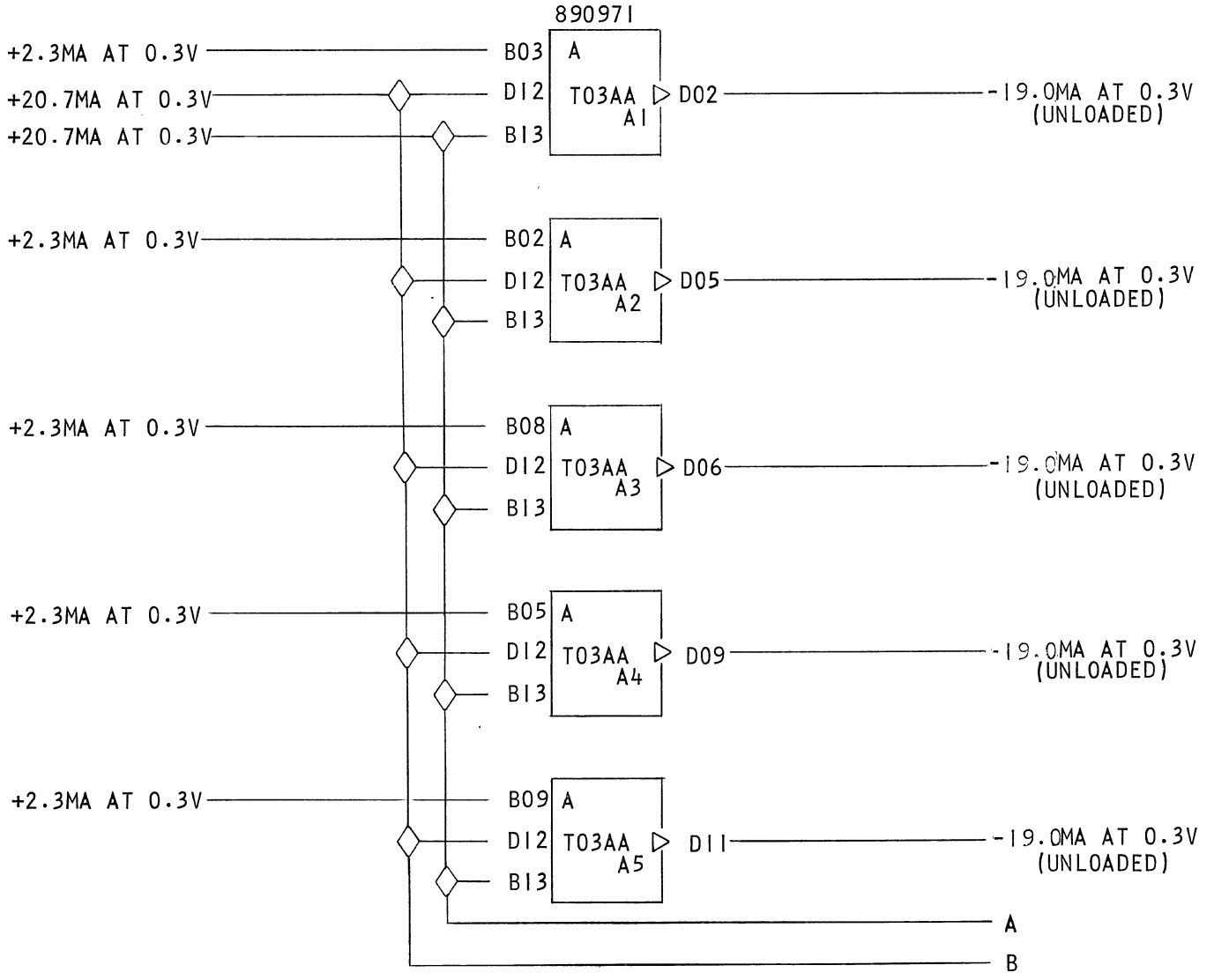
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

I-INPUT ASSEMBLER WO/L

CATEGORY CODE

T03

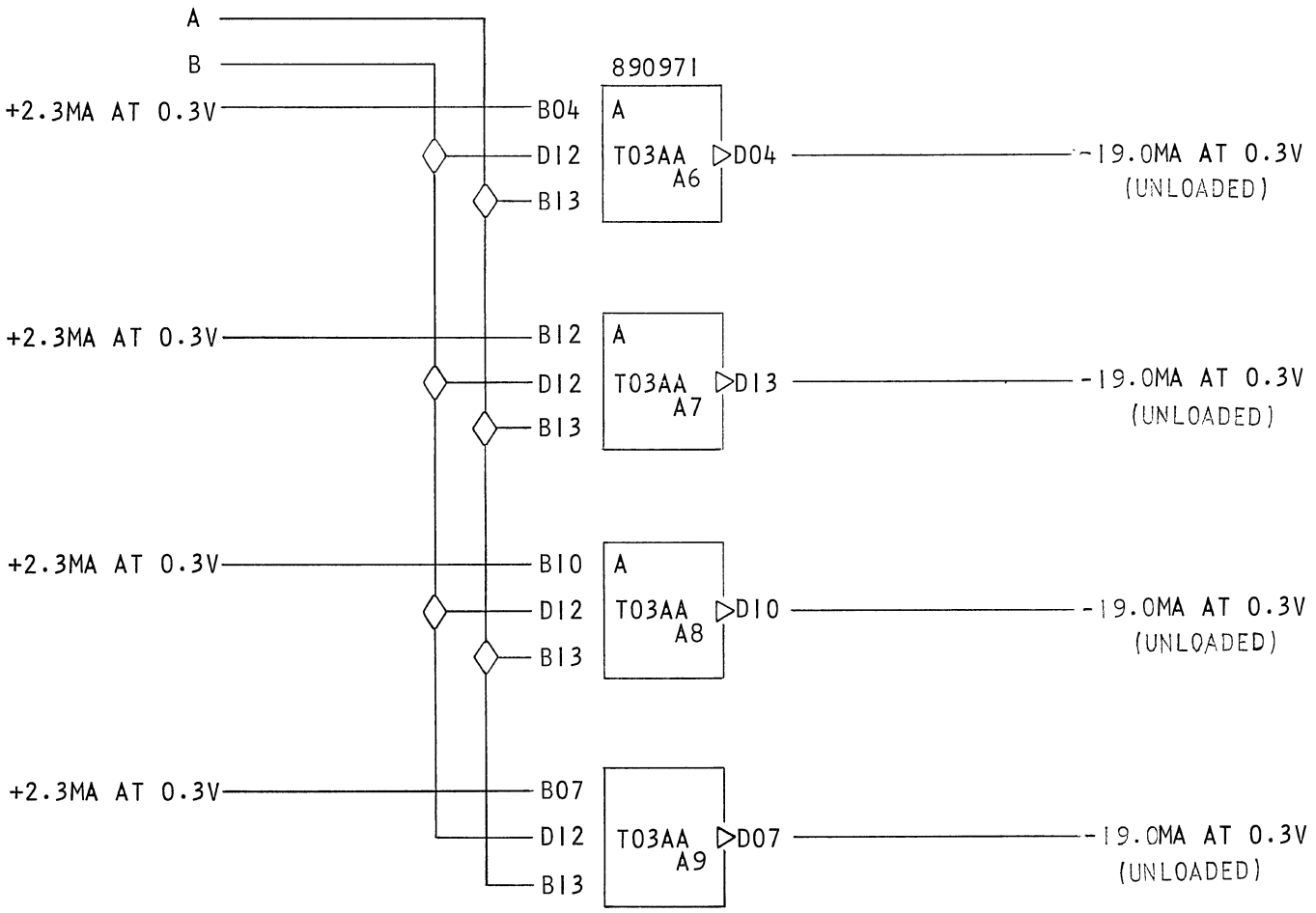
P/N	5803028
EC	165438
STANDARD RESTRICTED	
CARD SIZE	I-12



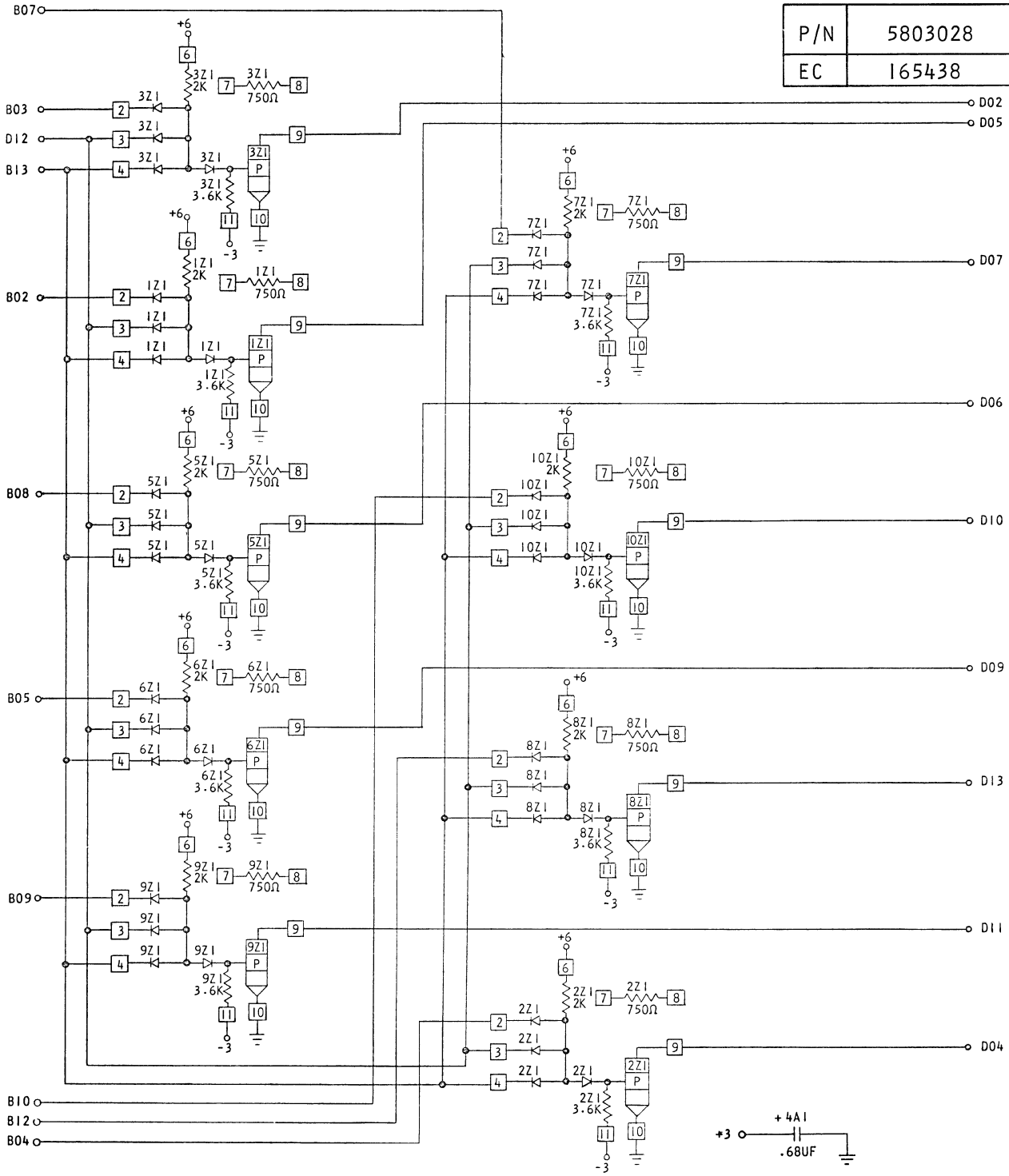
I-INPUT ASSEMBLER WO/L

T03

P/N	5803028
EC	165438



P/N	5803028
EC	165438



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-5W AI & 2-5W AI W0/L & 2 PROG RESISTORS

LMH	0-2860	306
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

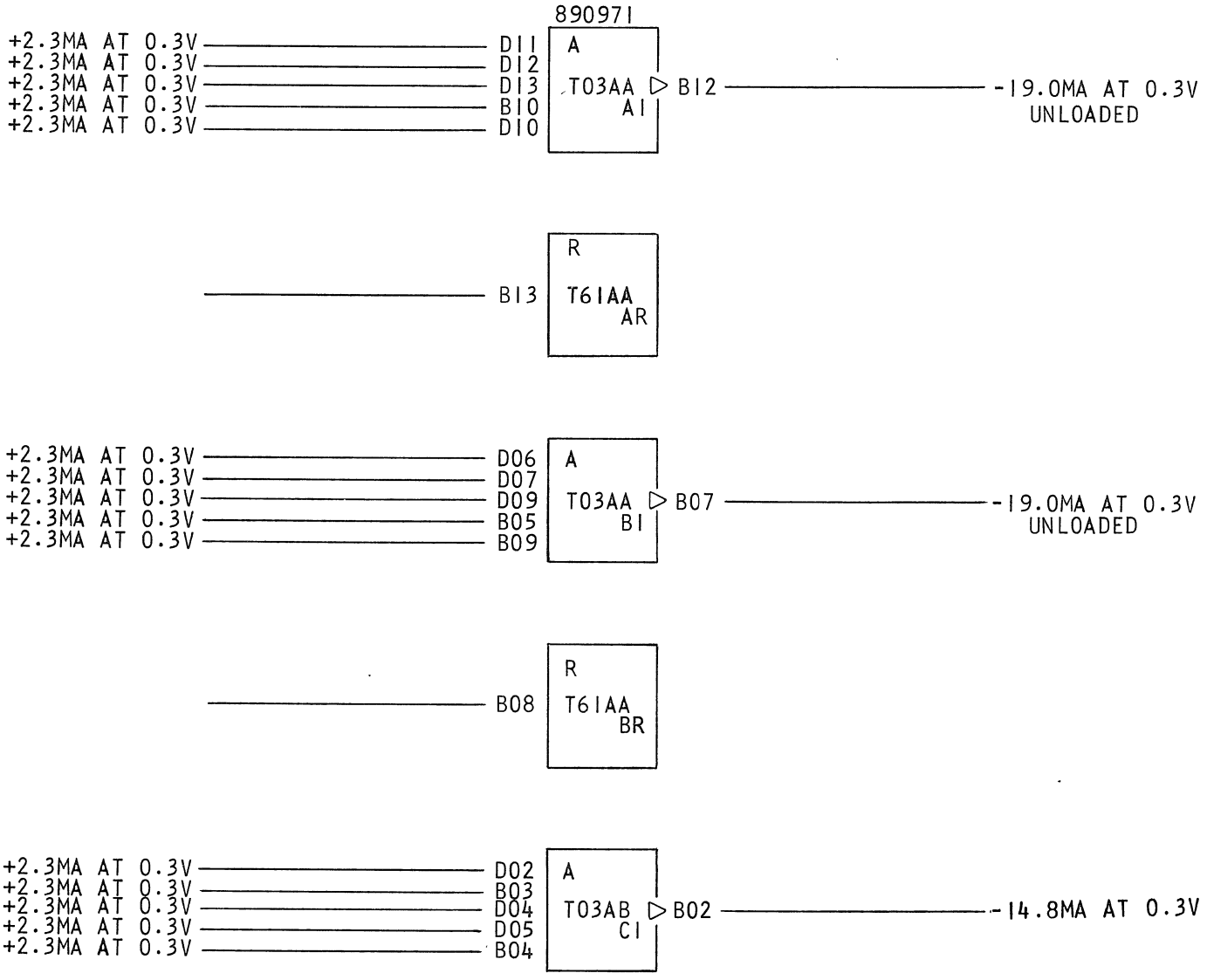
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

1-5W AI & 2-5W AI W0/L & 2 PROG RESISTOR

CATEGORY CODE

T03

P/N	5803031
EC	160039
STANDARD RESTRICTED	
CARD SIZE	1-6



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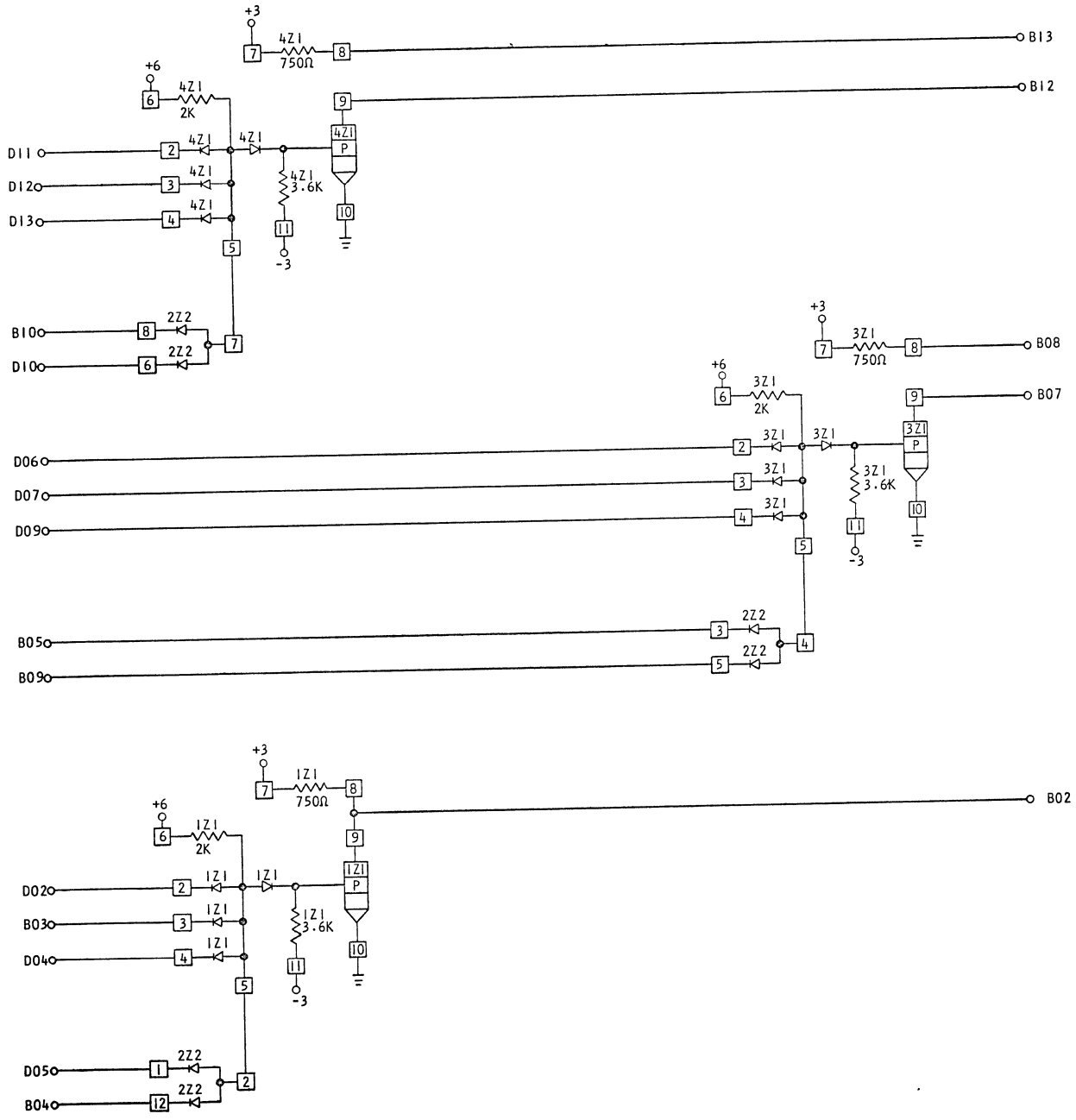
P/N	5803031
EC	160039



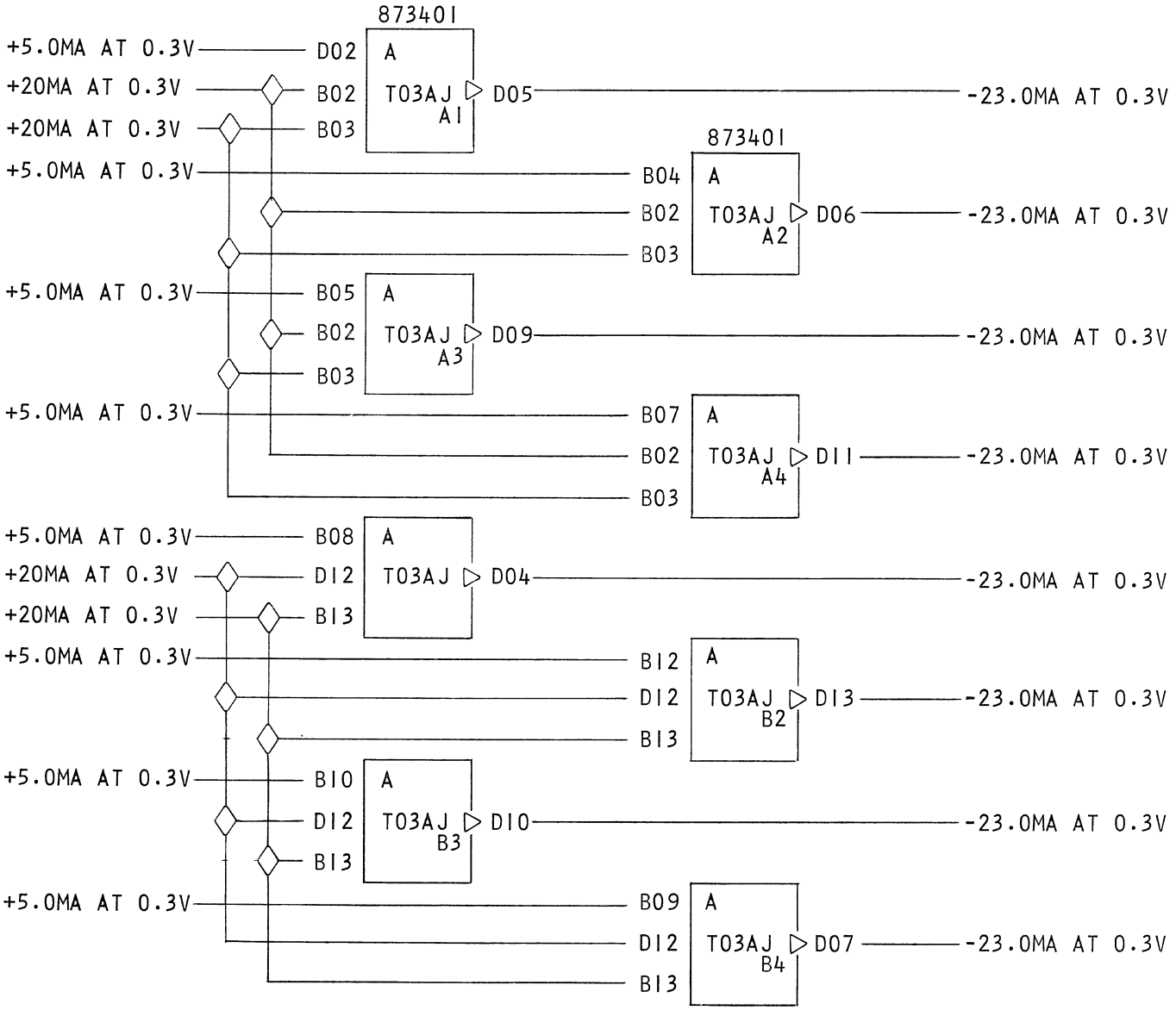
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

4-3W,4-3W GATED API

CATEGORY CODE

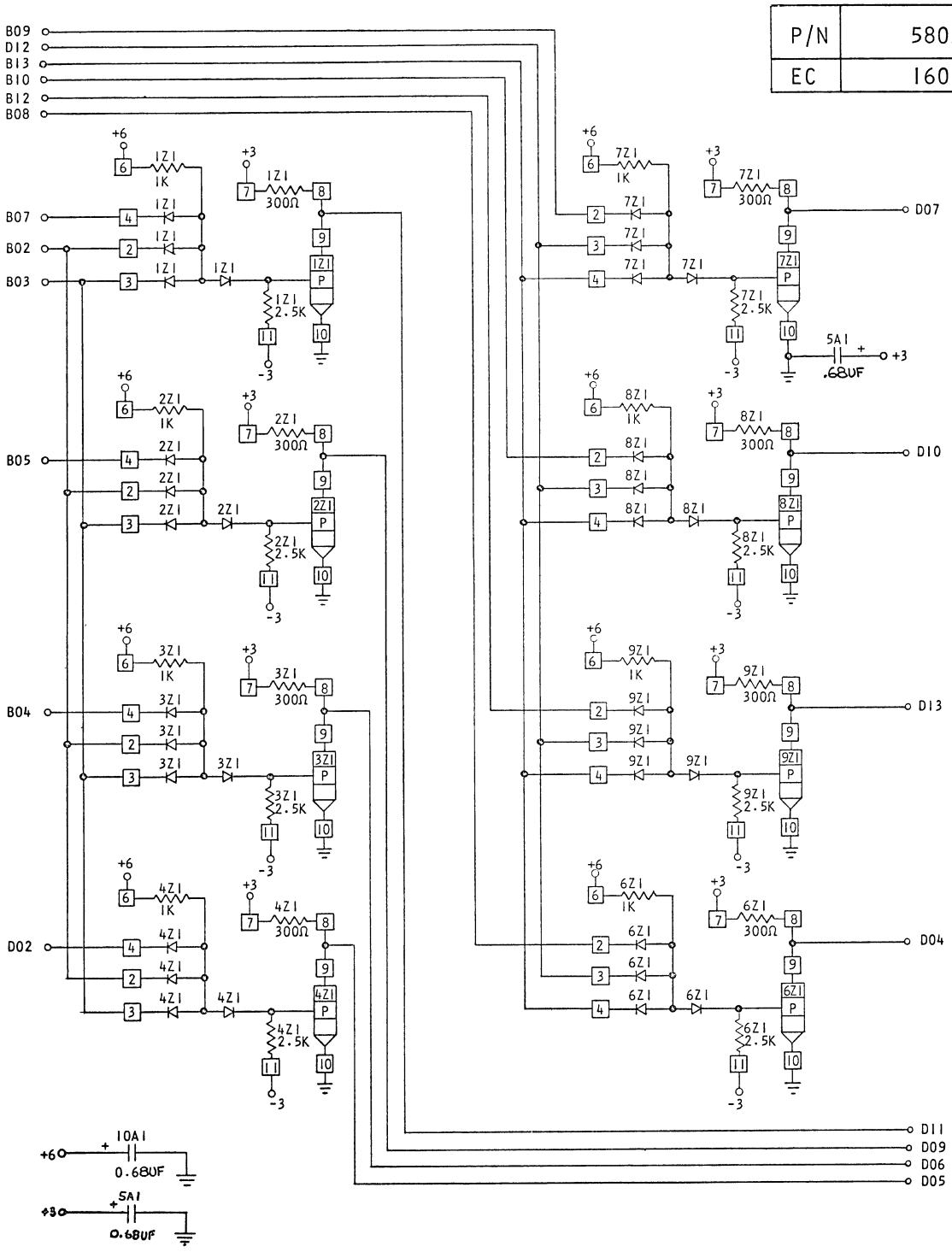
T03

P/N	5803036
EC	160034
STANDARD RESTRICTED	
CARD SIZE	1-12



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-3W,4-3W GATED API

P/N	5803036
EC	160034



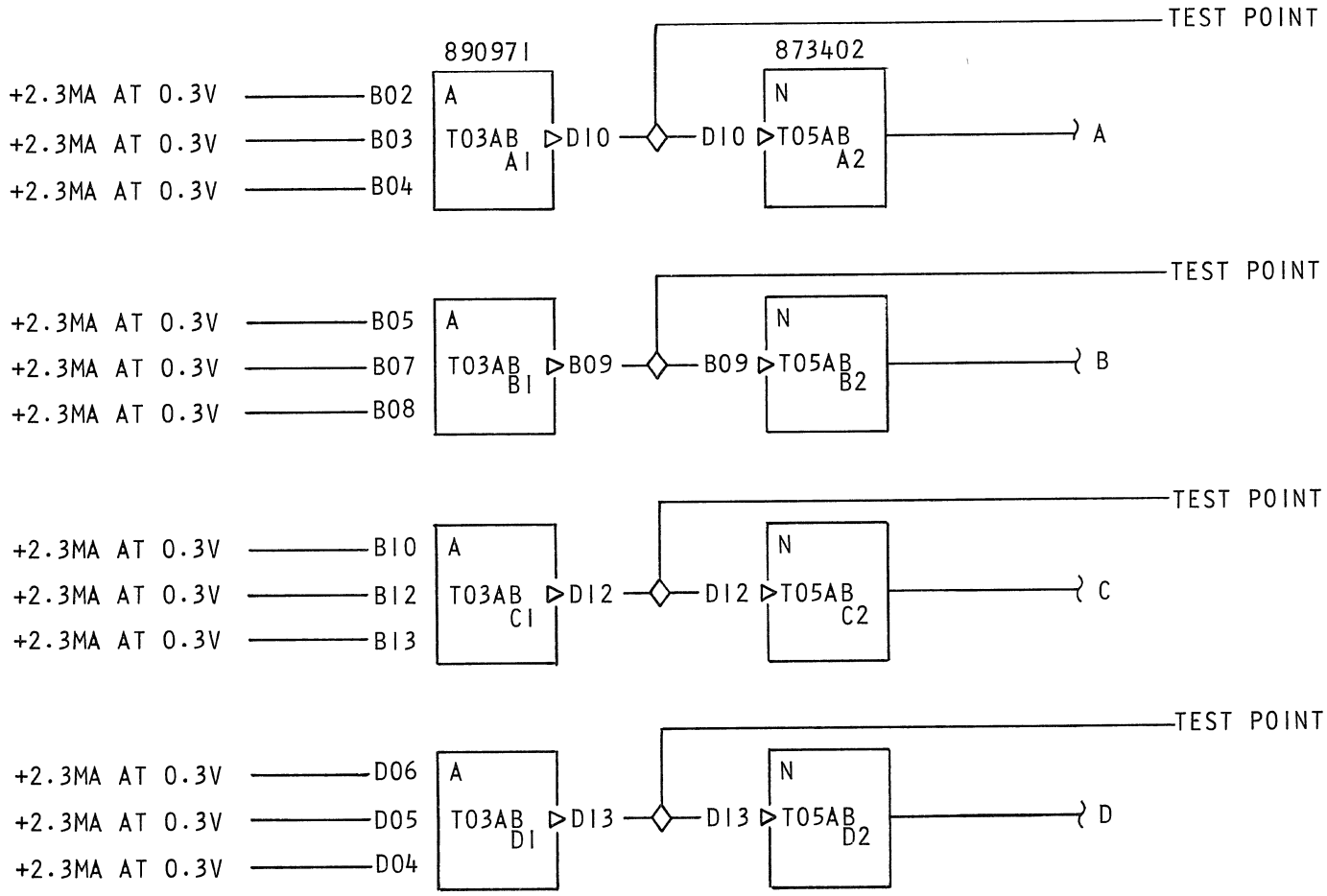
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

4-3WA MPLX LD TERMINATED

CATEGORY CODE

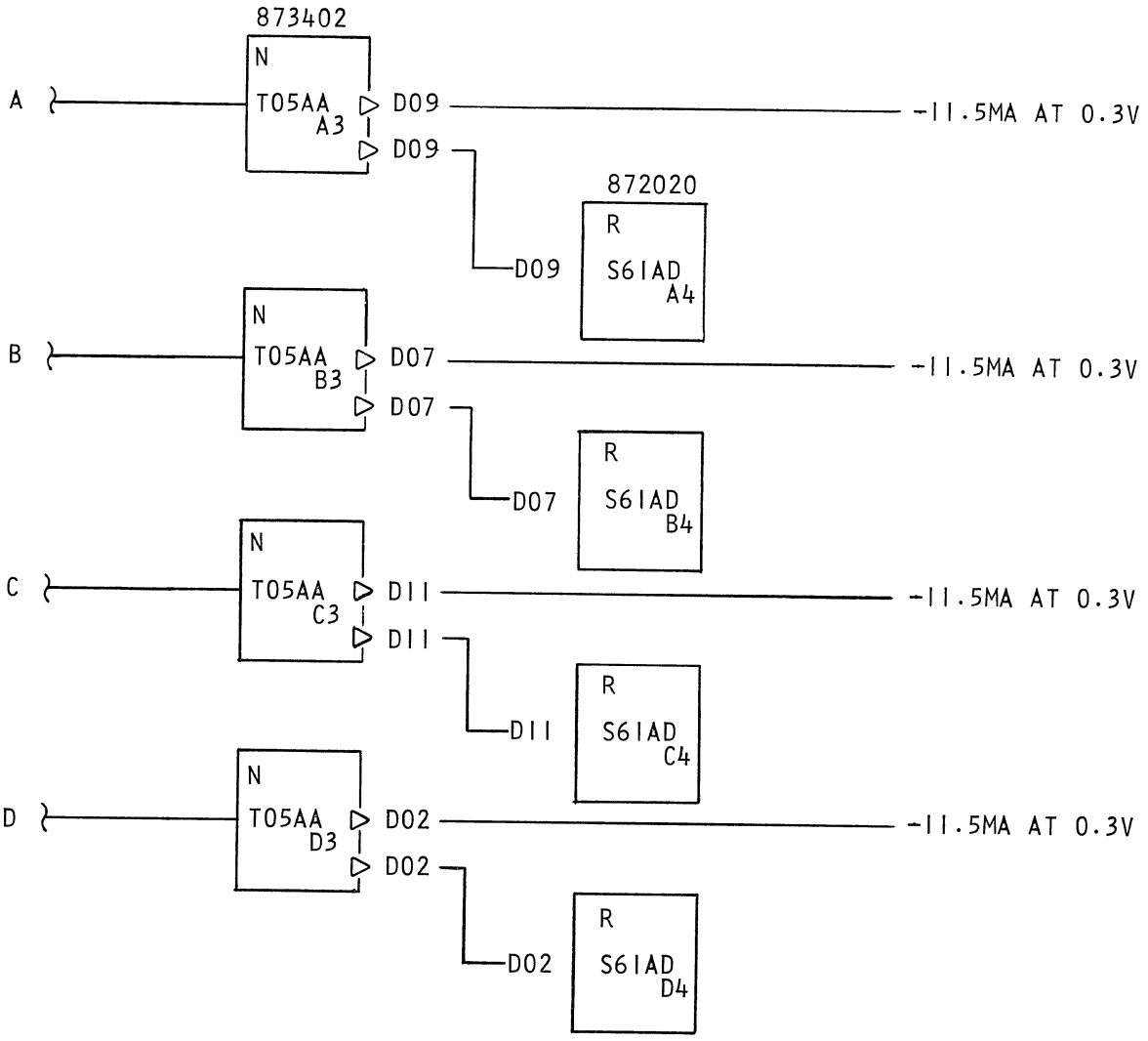
T06

P/N	5803039	
EC	1637218	
SPECIAL RESTRICTED		
CARD SIZE		1-12

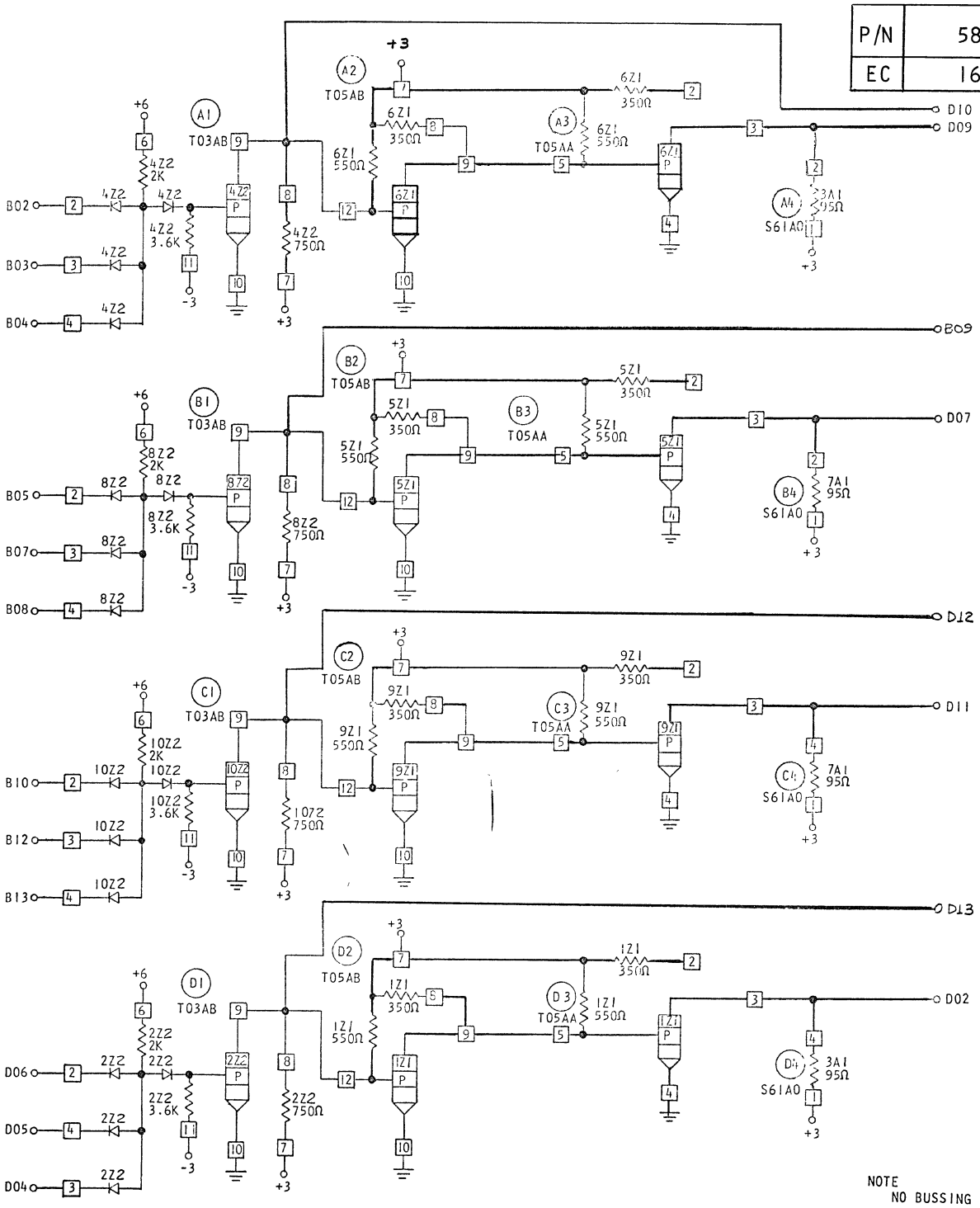


4-3WA MPLX LD TERMINATED

P/N	5803039
EC	163721B



P/N	5803039
EC	163721B



NOTE
NO BUSSING CONDITION

Printed in U.S.A.

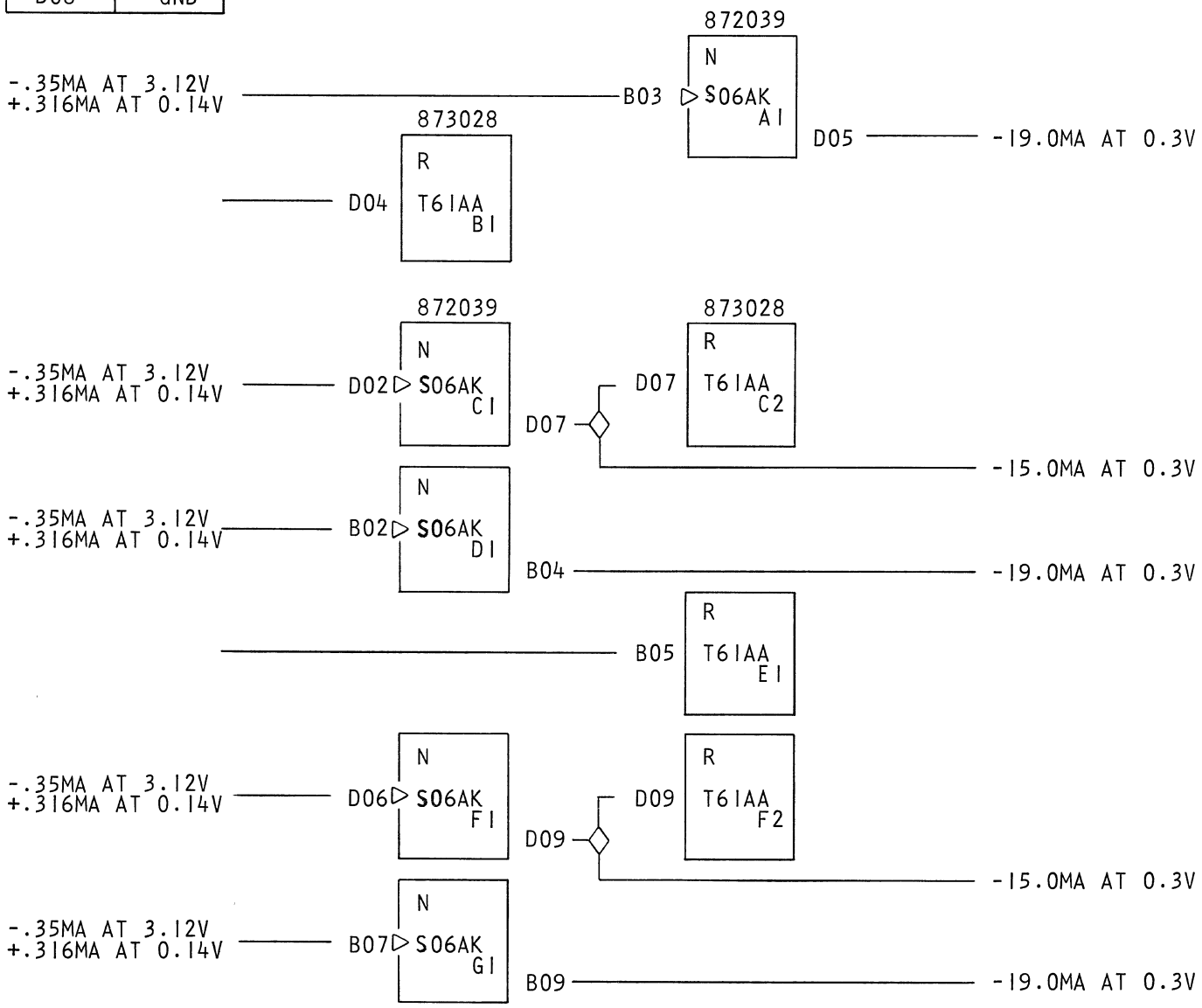
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

8-INTERFACE RECEIVERS

CATEGORY CODE

T66

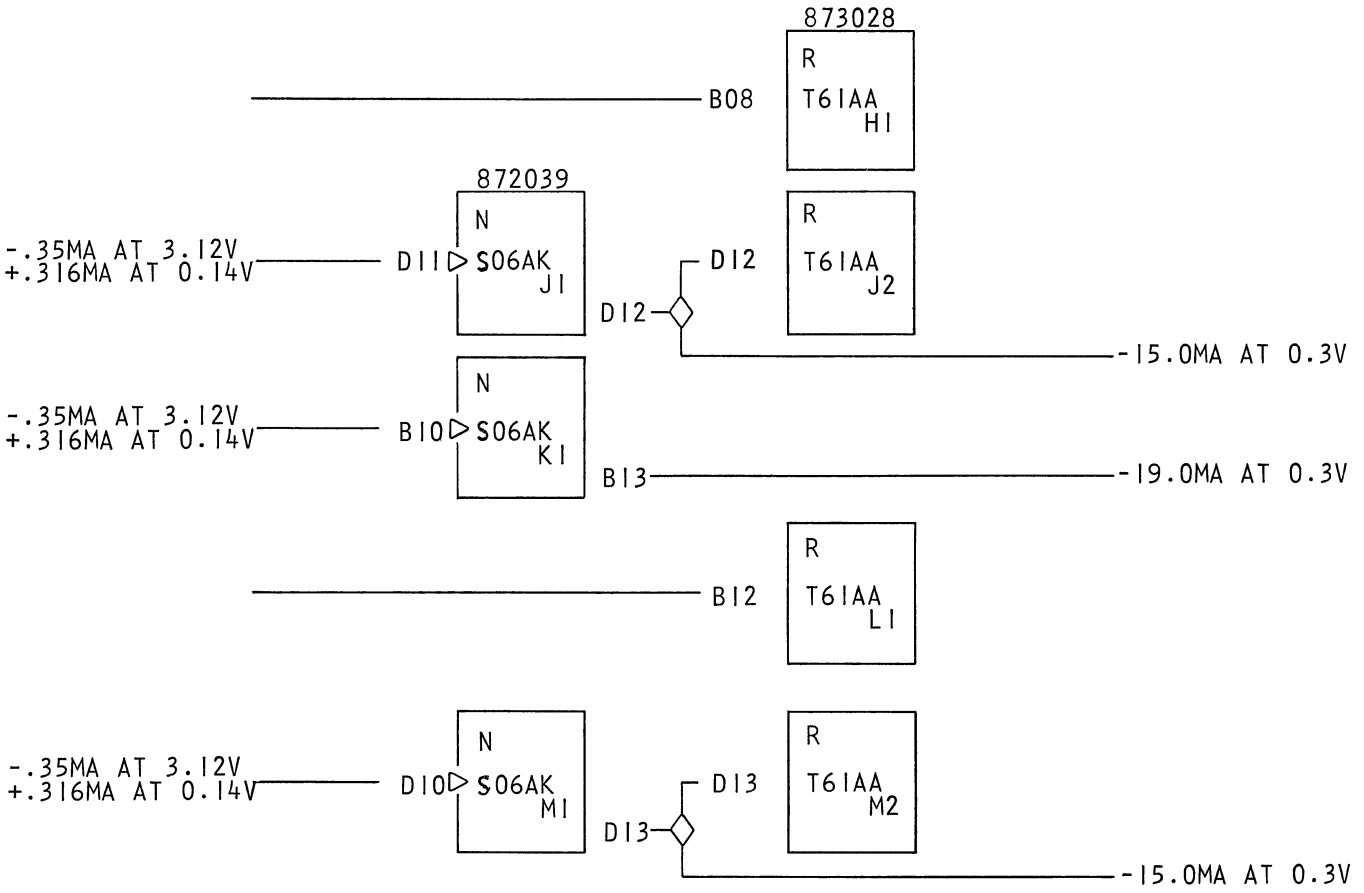
P/N	5803041
EC	161445
STANDARD RESTRICTED	
CARD SIZE	1-12



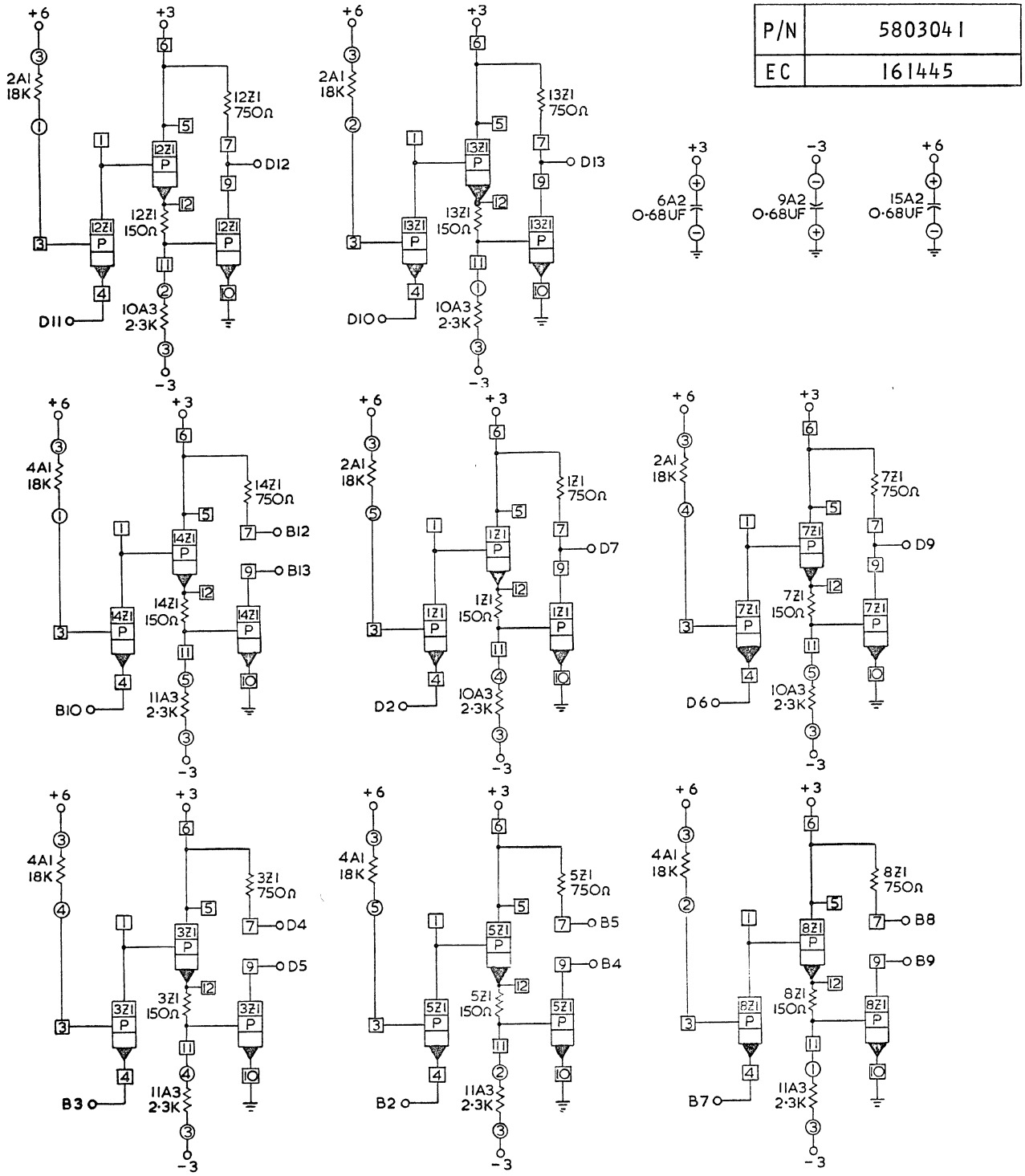
8-INTERFACE RECEIVERS

T66

P / N	5803041
E C	161445



P/N	5803041
EC	161445



Printed in U.S.A.

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
PARITY CHECKER

LMH Cat.	0-2860 Subject	313 Suffix

IBM Location Manufacturing Specification

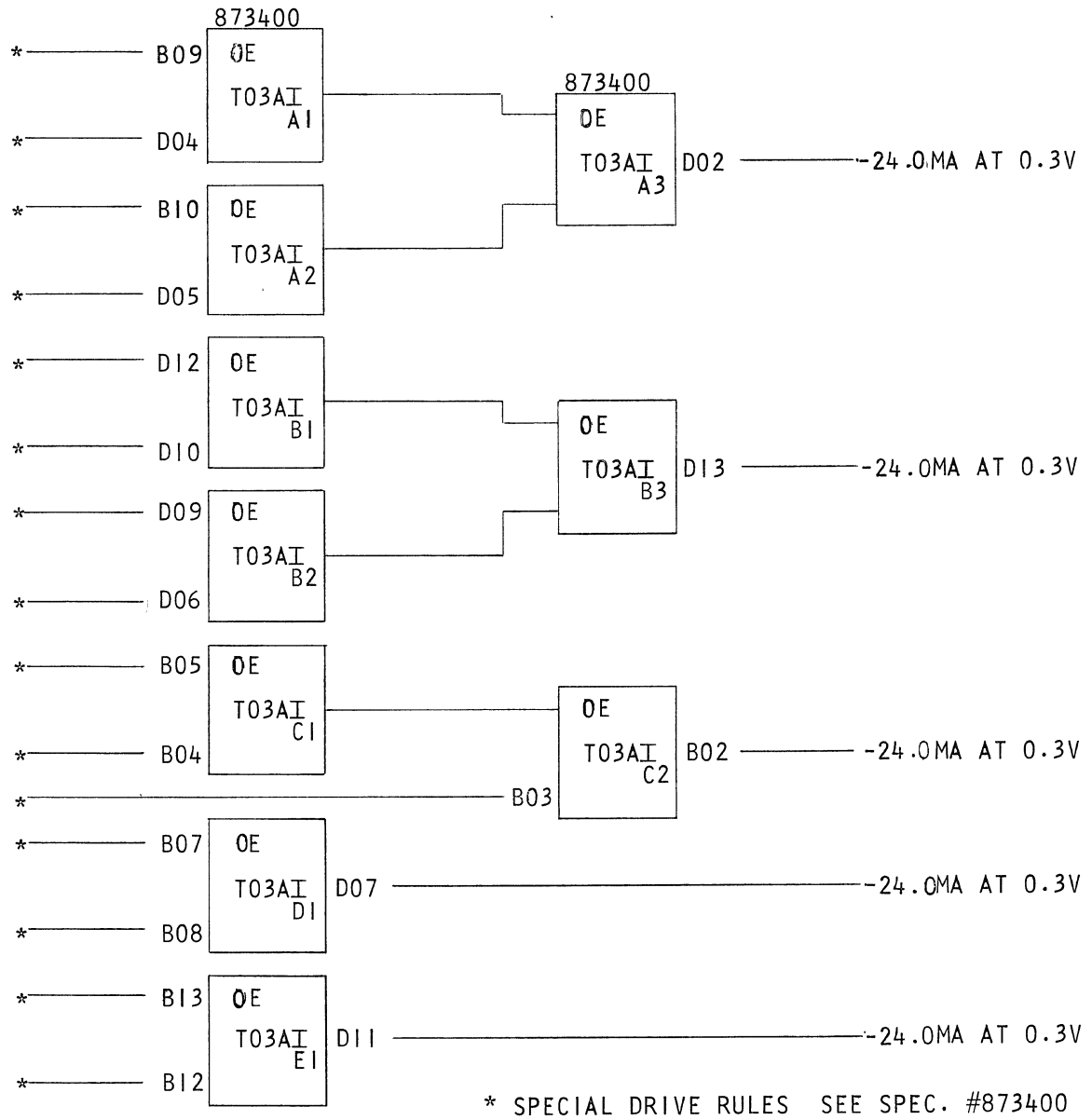
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

PARITY CHECKER

CATEGORY CODE

T03

P/N	5803051
EC	162195
STANDARD RESTRICTED	
CARD SIZE	1-12



06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.		
Applicability: ENDICOTT		Responsibility: ENDICOTT	Date: 1-67 / Page: 1 of 3

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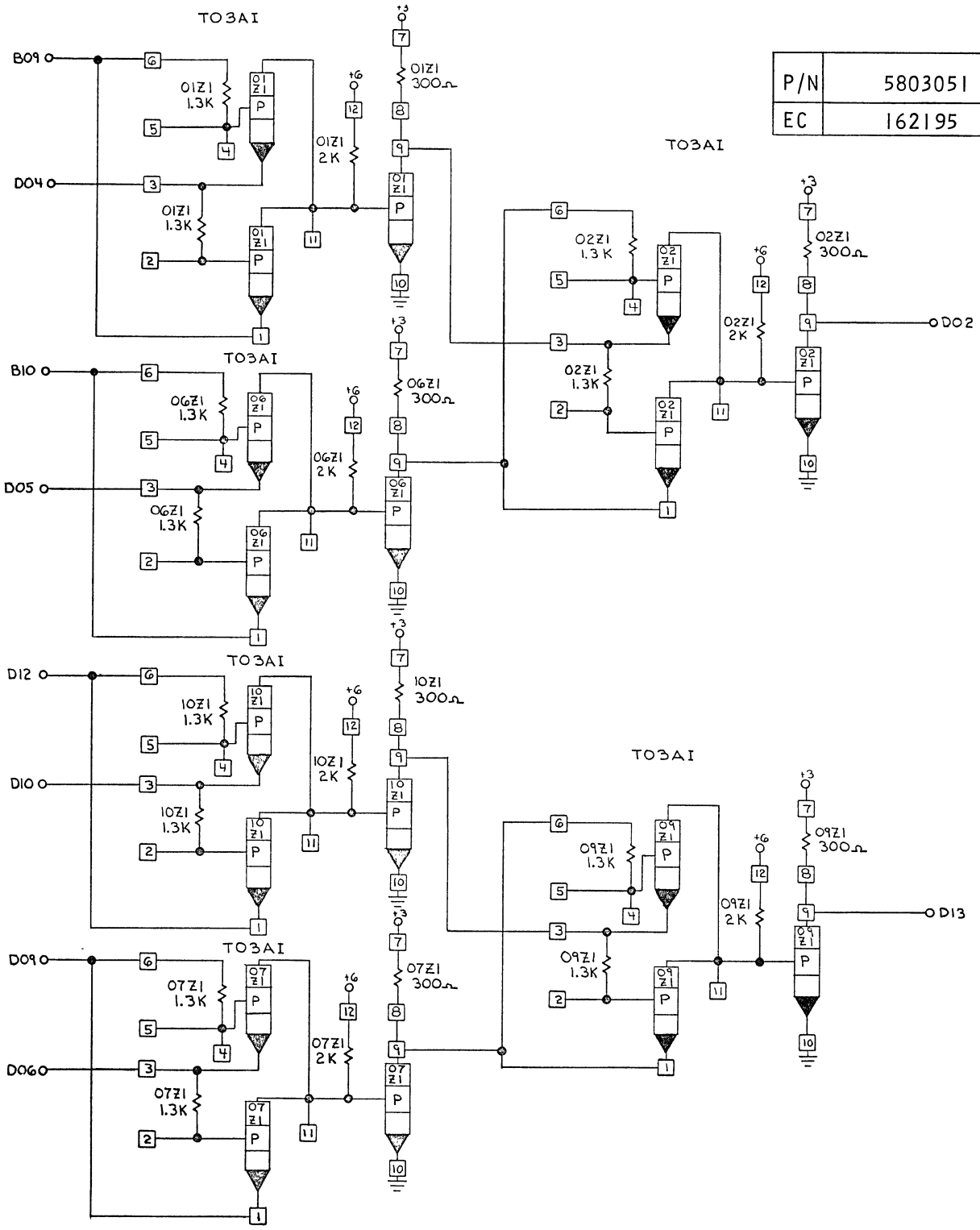
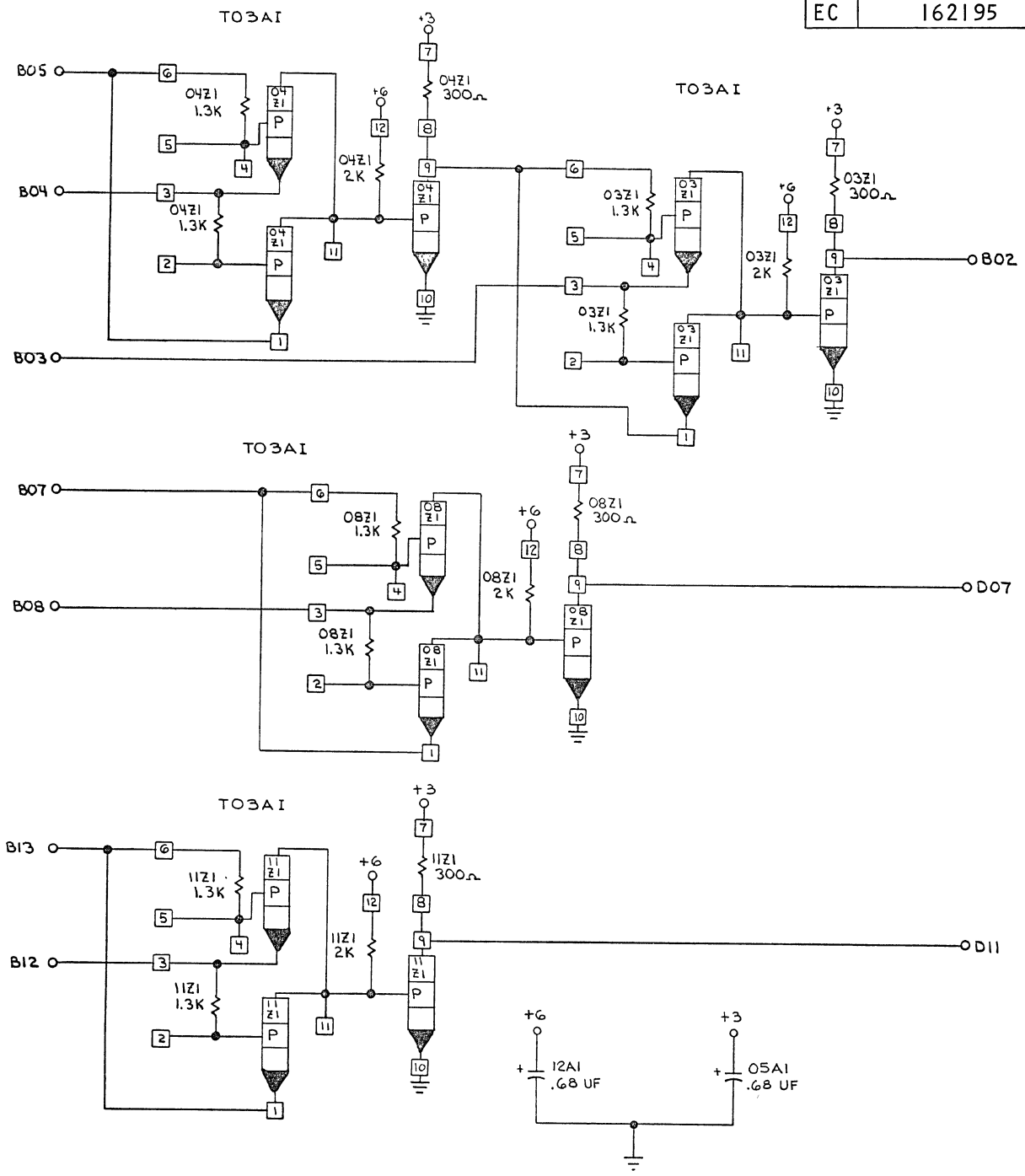
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
PARITY CHECKER

P/N	5803051
EC	162195



P/N	5803051
EC	162195



Printed in U.S.A.

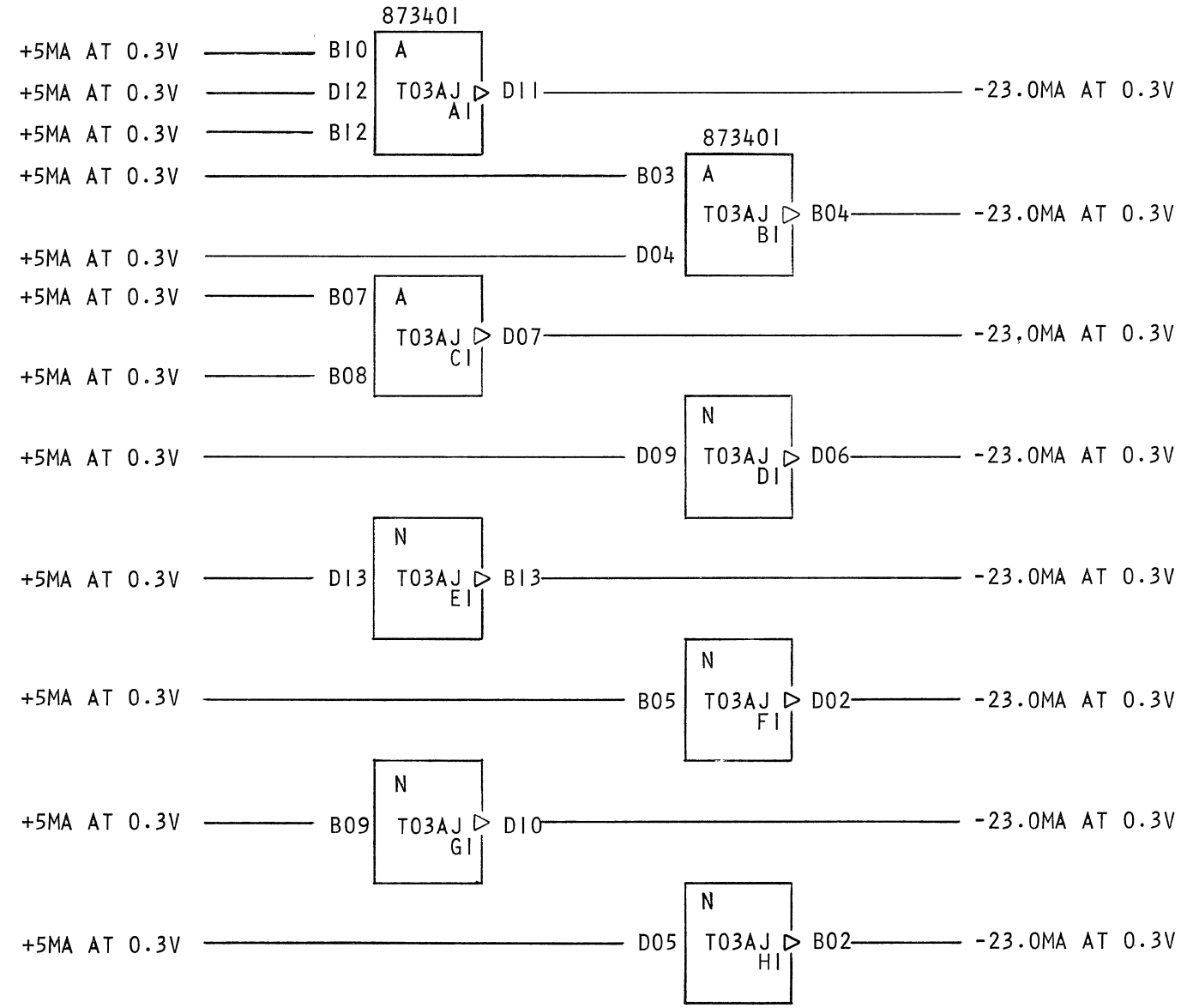
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

5-1W,2-2W,1-3W API

CATEGORY CODE

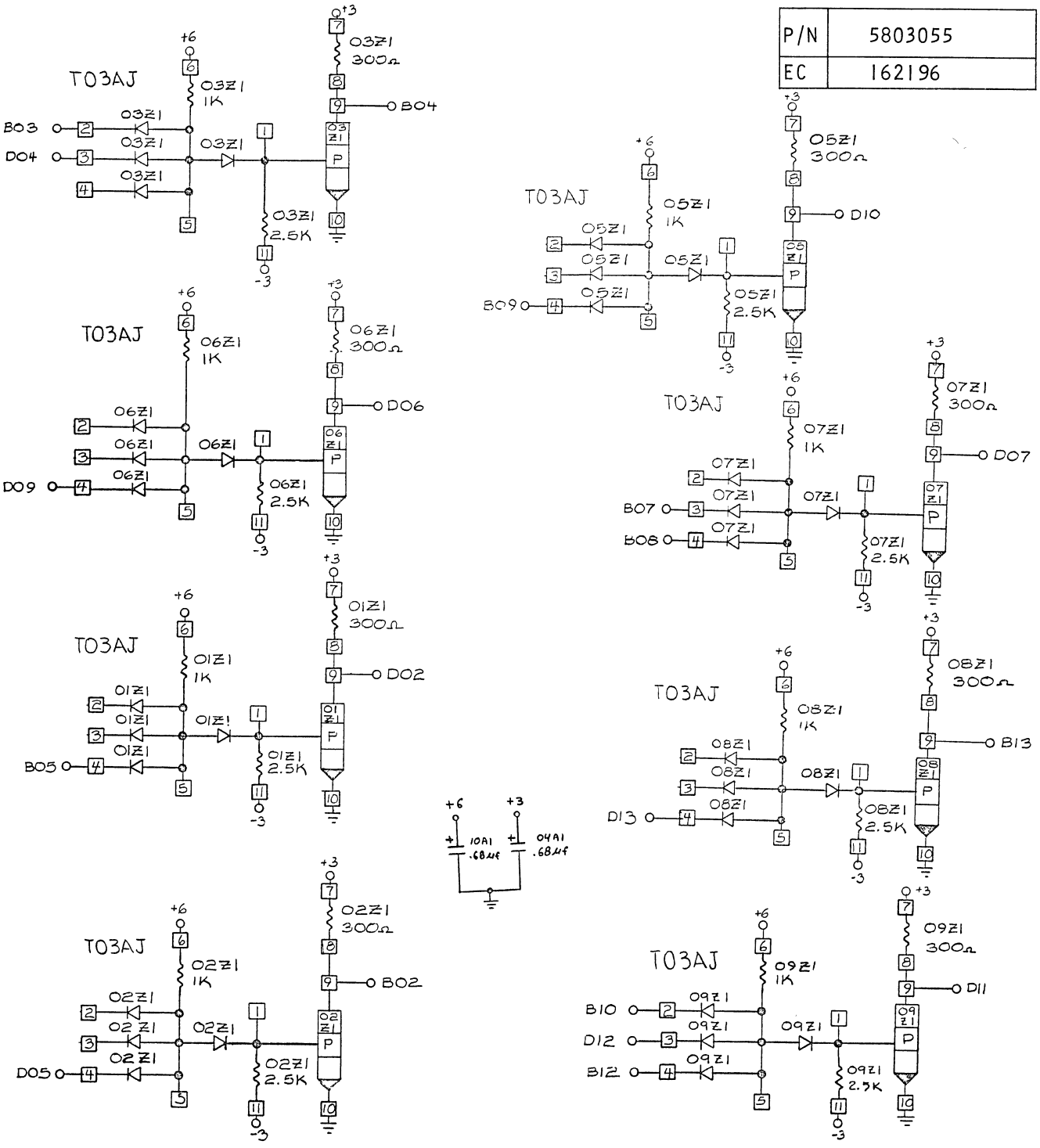
T03

P/N	5803055
EC	162196
STANDARD RESTRICTED	
CARD SIZE	1-12



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
5-1W, 2-2W, 1-3W API

P/N	5803055
EC	162196



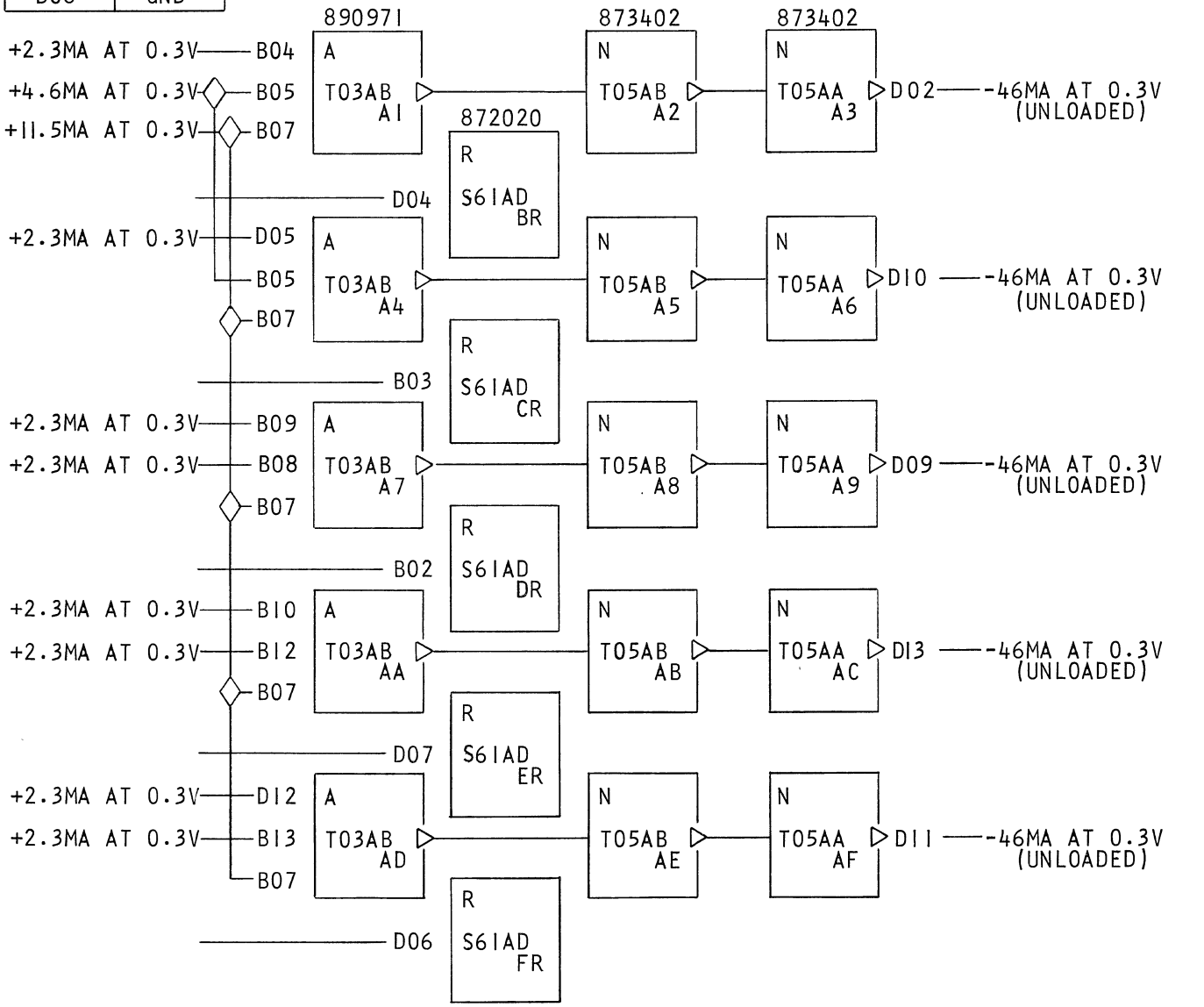
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

5-INTERFACE LINE DRIVERS

CATEGORY CODE

T03	T05

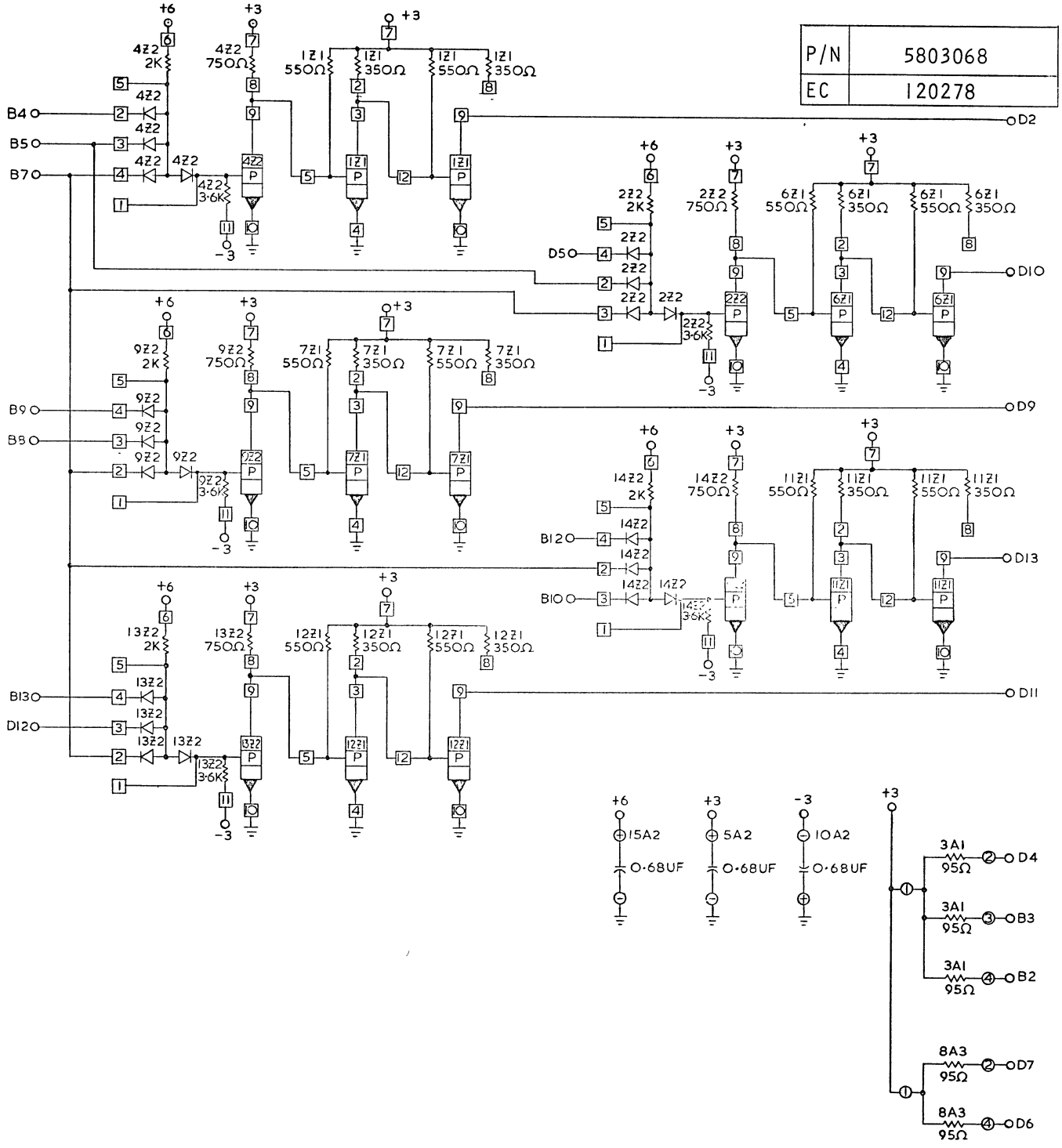
P/N	5803068
EC	120278
STANDARD RESTRICTED	
CARD SIZE	1-12



LMH Cat.	0-2860 Subject	316 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
5-INTERFACE LINE DRIVERS

P/N	5803068
EC	120278



2 of 2 Page	1-67 Date

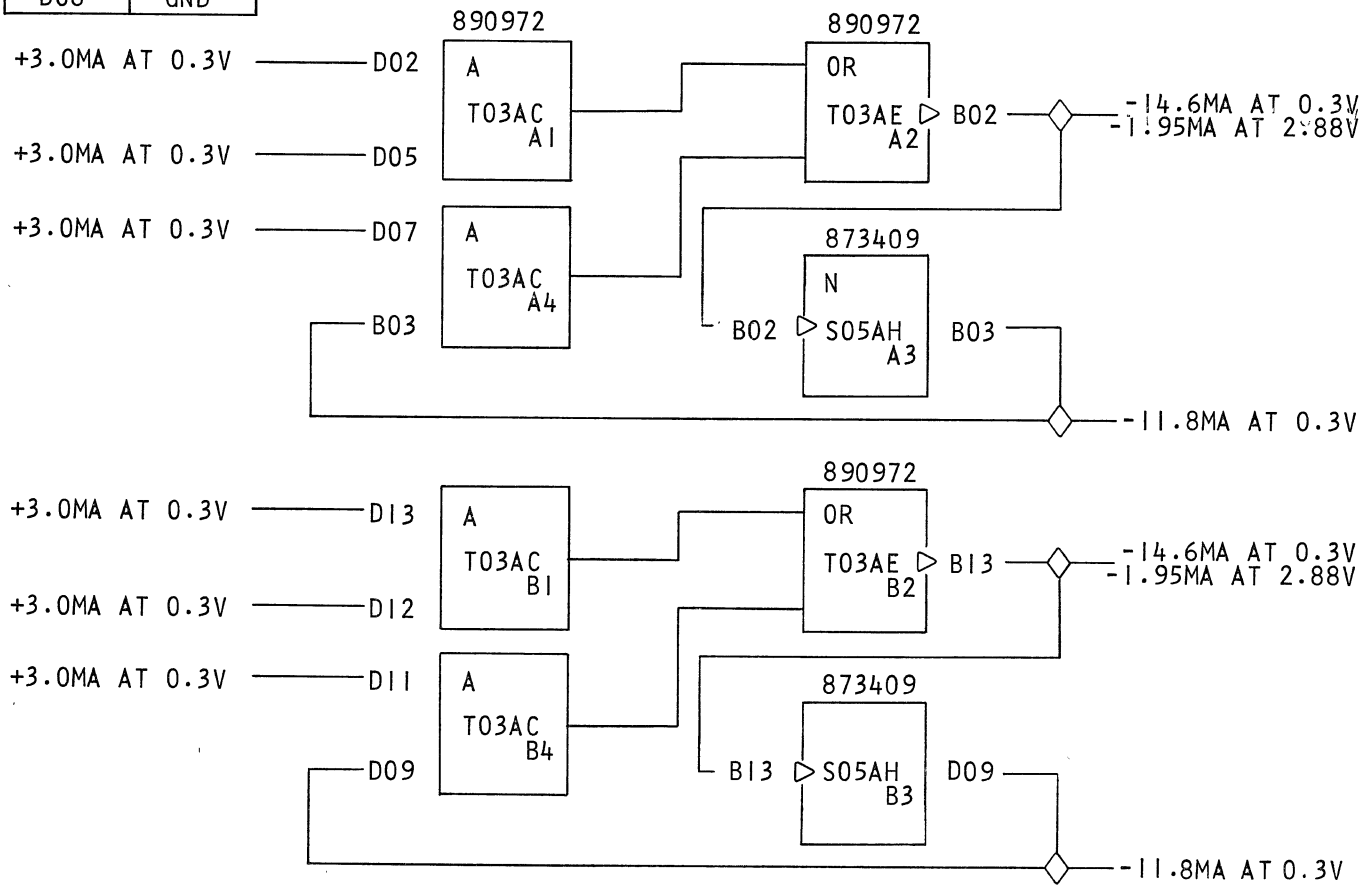
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

4-AOI,II LATCH CARD

CATEGORY CODE

T03

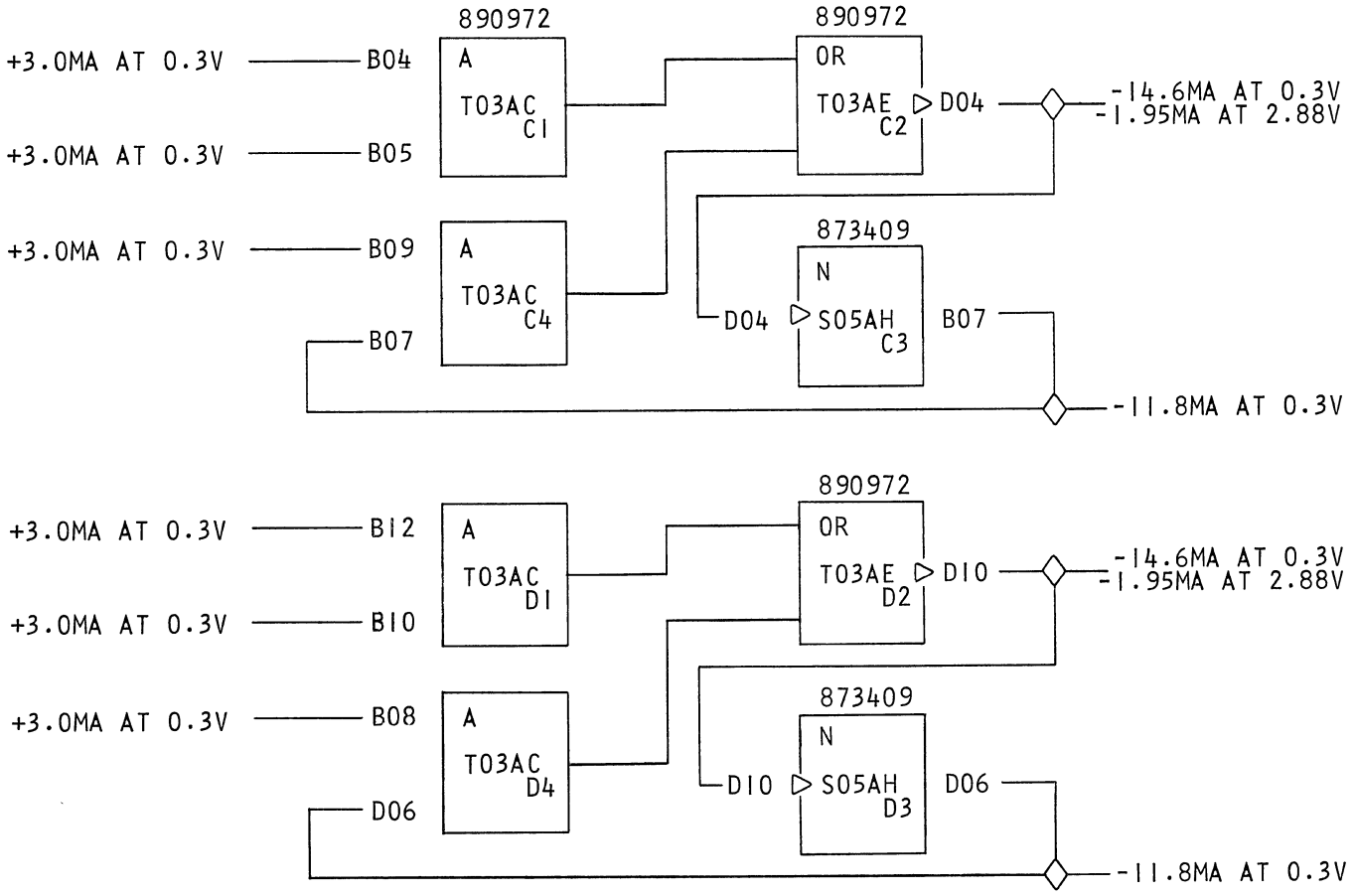
P/N	5803130
EC	161589
STANDARD RESTRICTED	
CARD SIZE	1-12



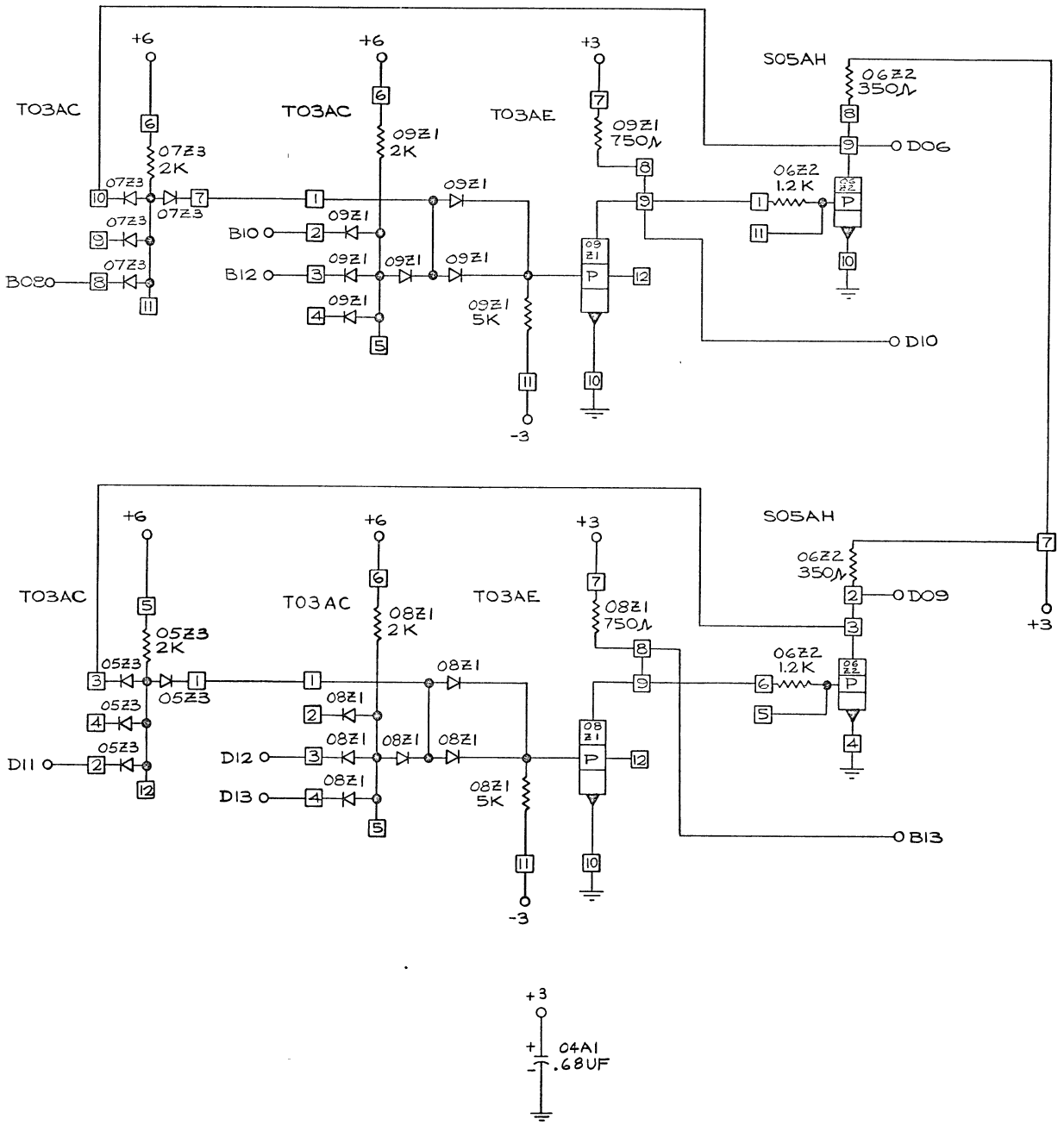
4-AOI,II LATCH CARD

T03

P/N	5803130
EC	161589

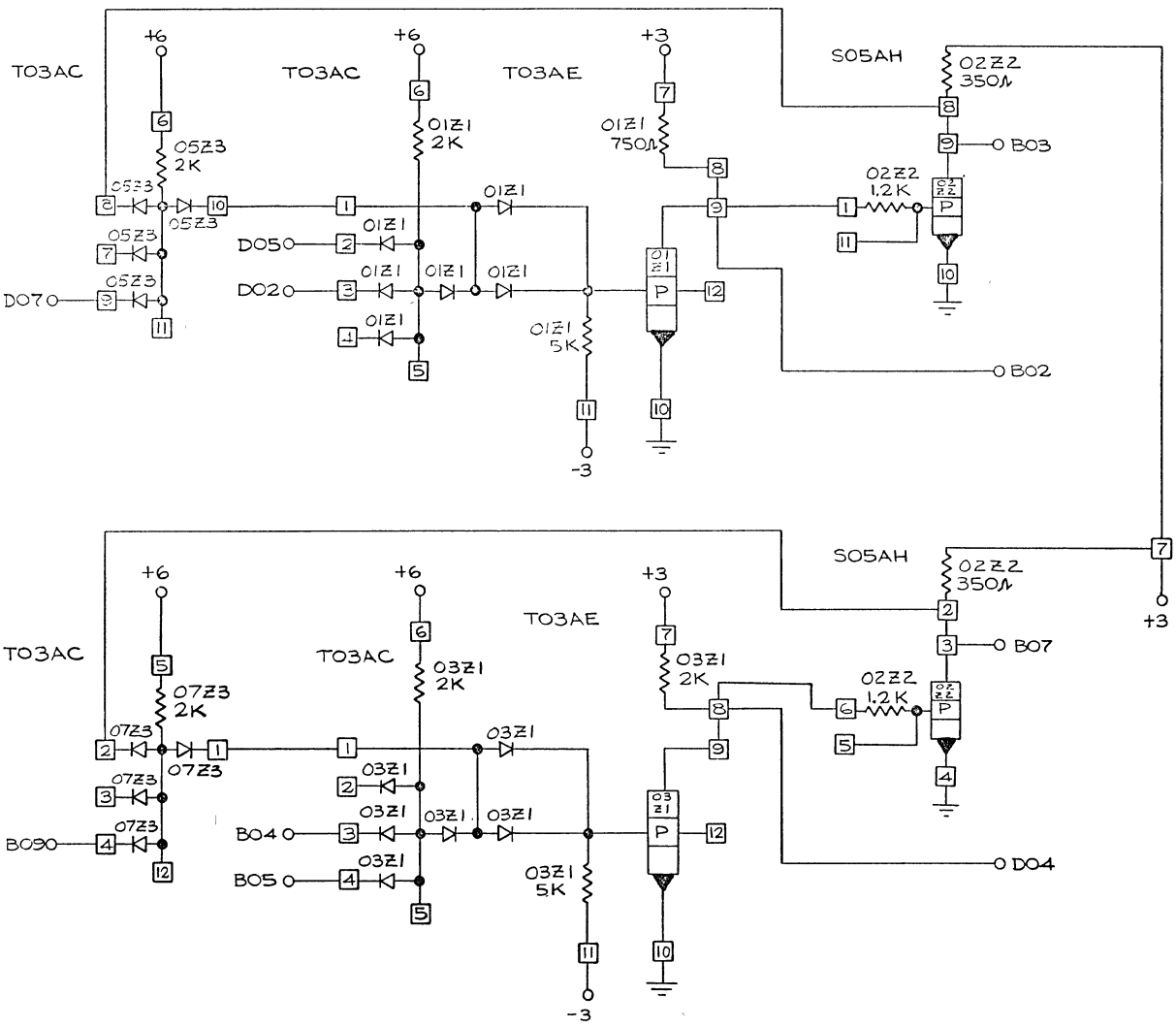


P/N	5803130
EC	161589



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-AOI,II LATCH CARD

P/N	5803130
EC	161589



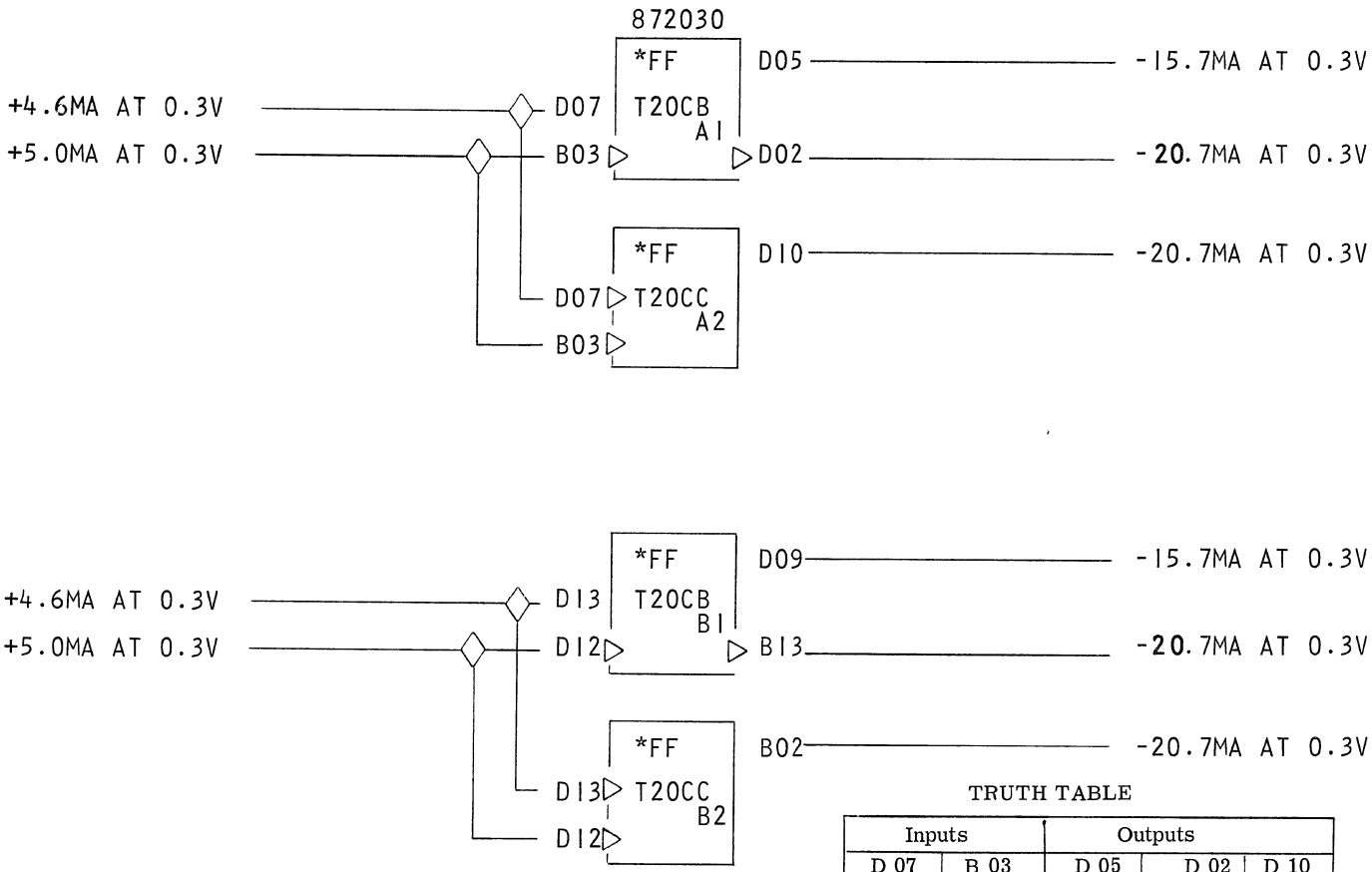
POWER REQUIRED	
PIN	VOLT
B06	-3
B11	+6
D03	+3
D08	GND

D.C. LOGIC TRIGGER

CATEGORY CODE

T20

P/N	5803165
EC	163566
SPECIAL ACTIVE	
CARD SIZE	1-12



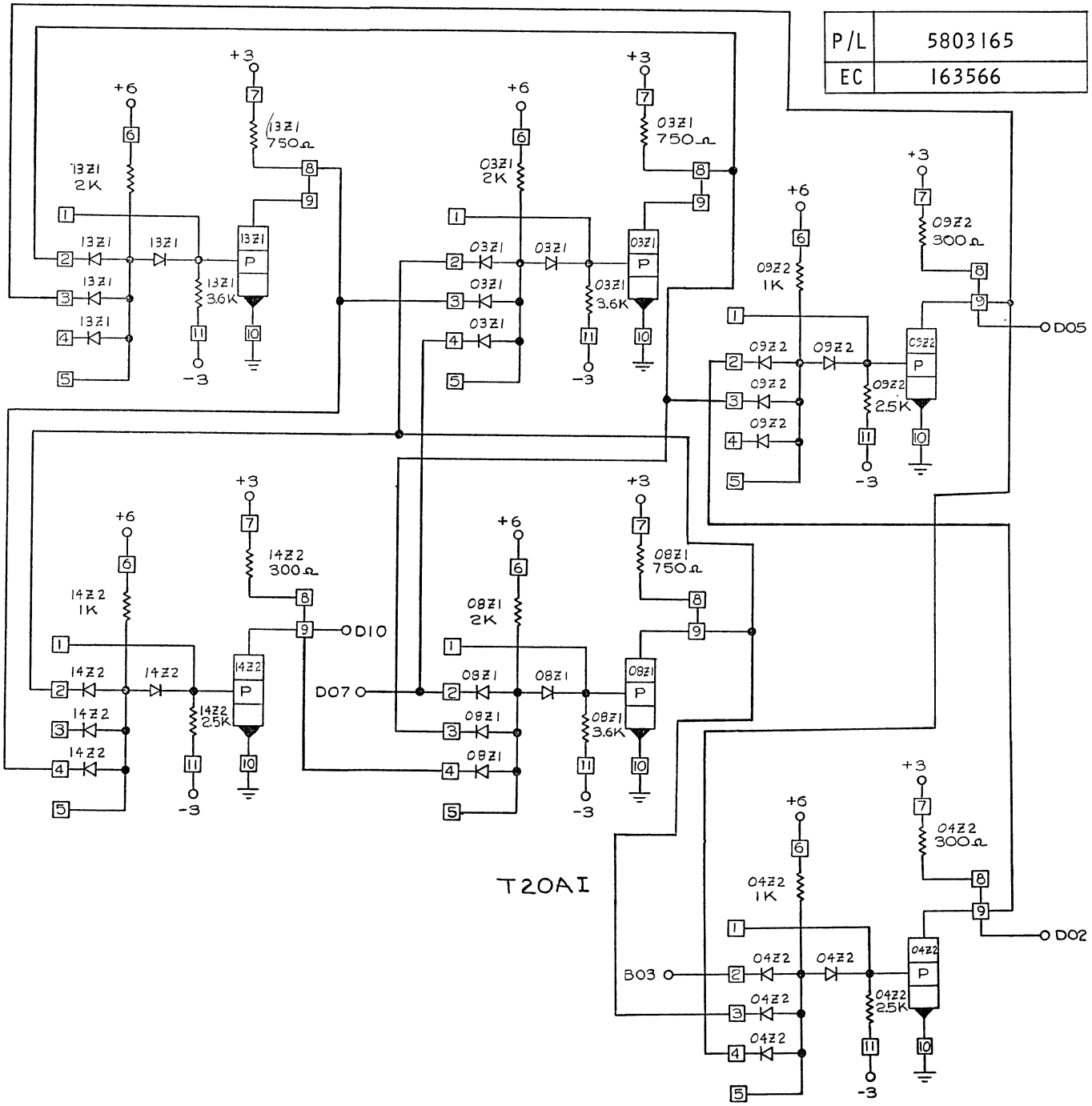
TRUTH TABLE

Inputs		Outputs		
D 07 D 13	B 03 D 12	D 05 D 09	D 02 B 13	D 10 B 02
0	0	0	1	0
1	0	1	1	0
1	1	1	0	0
0	1	1	0	1

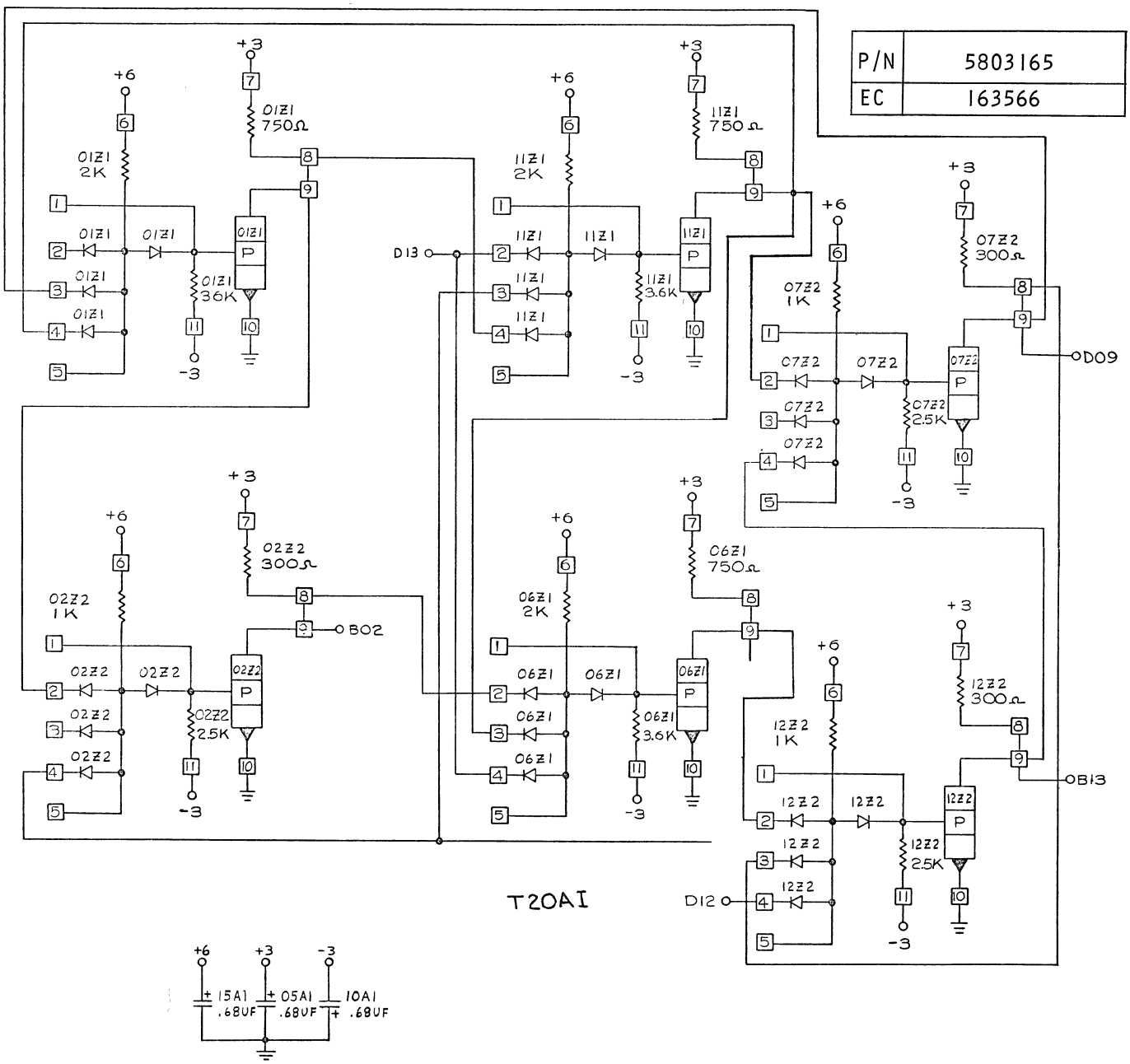
LMH Cat.	0-2860 Subject	318 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
D.C. LOGIC TRIGGER

P/L	5803165
EC	163566



P/N	5803165
EC	163566



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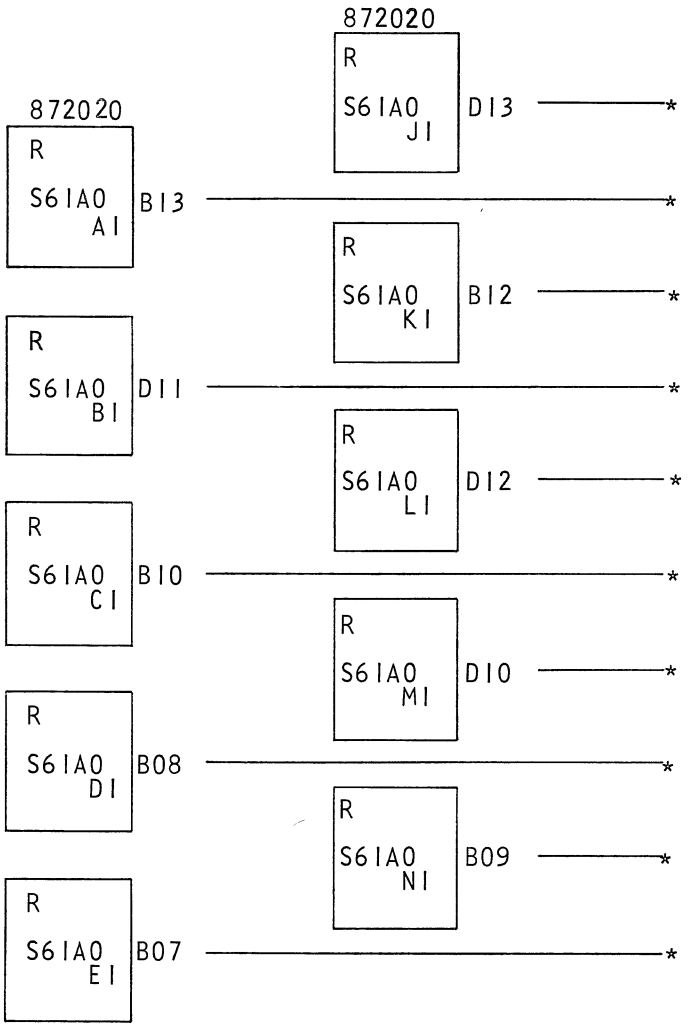
POWER REQUIRED	
PIN	VOLT
D03	+3
D08	GND

20-95 OHM MULTIPLEX TERMINATING RESISTORS TO +3V

CATEGORY CODE

S61

P/N	5803172
EC	160586
STANDARD RESTRICTED	
CARD SIZE	1-12

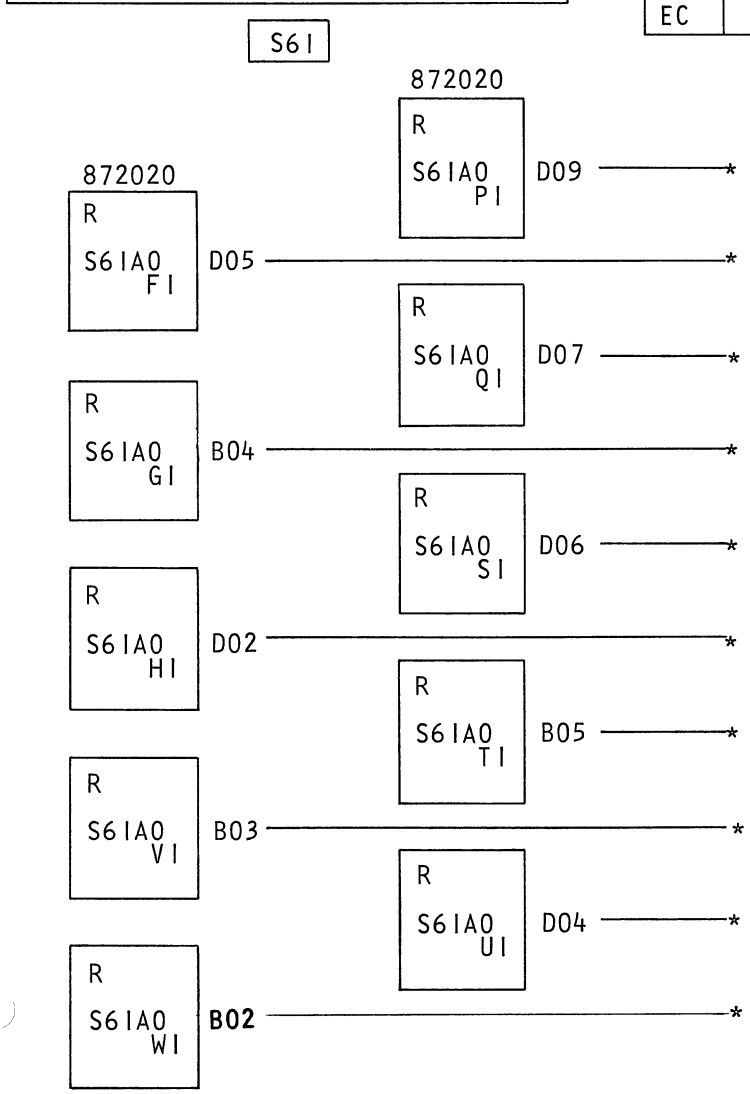


NOTE:

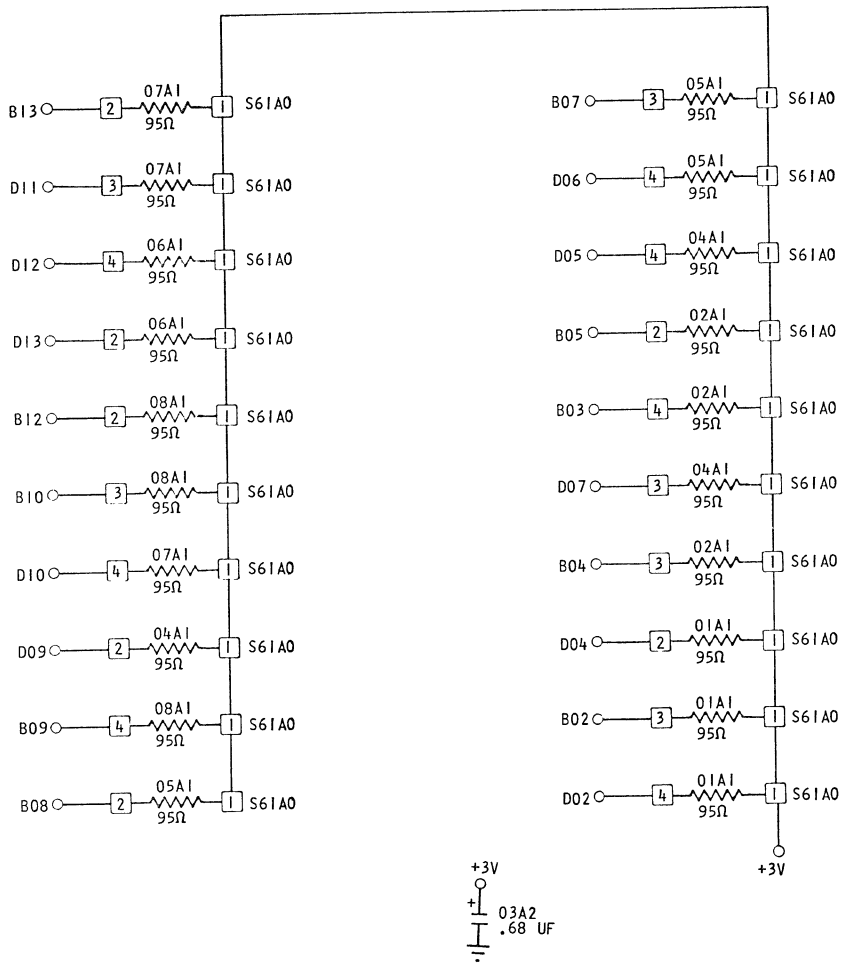
*MAXIMUM LOAD CURRENT 31.6MA AT 0.3V FOR ALL (±5%) RESISTORS.

20-95 OHM MULTIPLEX TERMINATING RESISTORS TO +3V

P/N	5803172
EC	160586



P/N	5803172
EC	160586



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2.0KHZ OSCILLATOR

LMH (Cat.)	0-2860 (Subject)	321 (Suffix)

IBM Location
Manufacturing Specification

POWER REQUIRED	
PIN	VOLT
B02	+12
B03	-12
B06	-3
D03	+3
D08	GND

2.0KHZ OSCILLATOR

CATEGORY CODE

T22

P/N	5803208
EC	163246A
SPECIAL RESTRICTED	
CARD SIZE	1-12

872656
OSC
T22AB
A1

D12 ——————————— -18.5MA AT 0.3V

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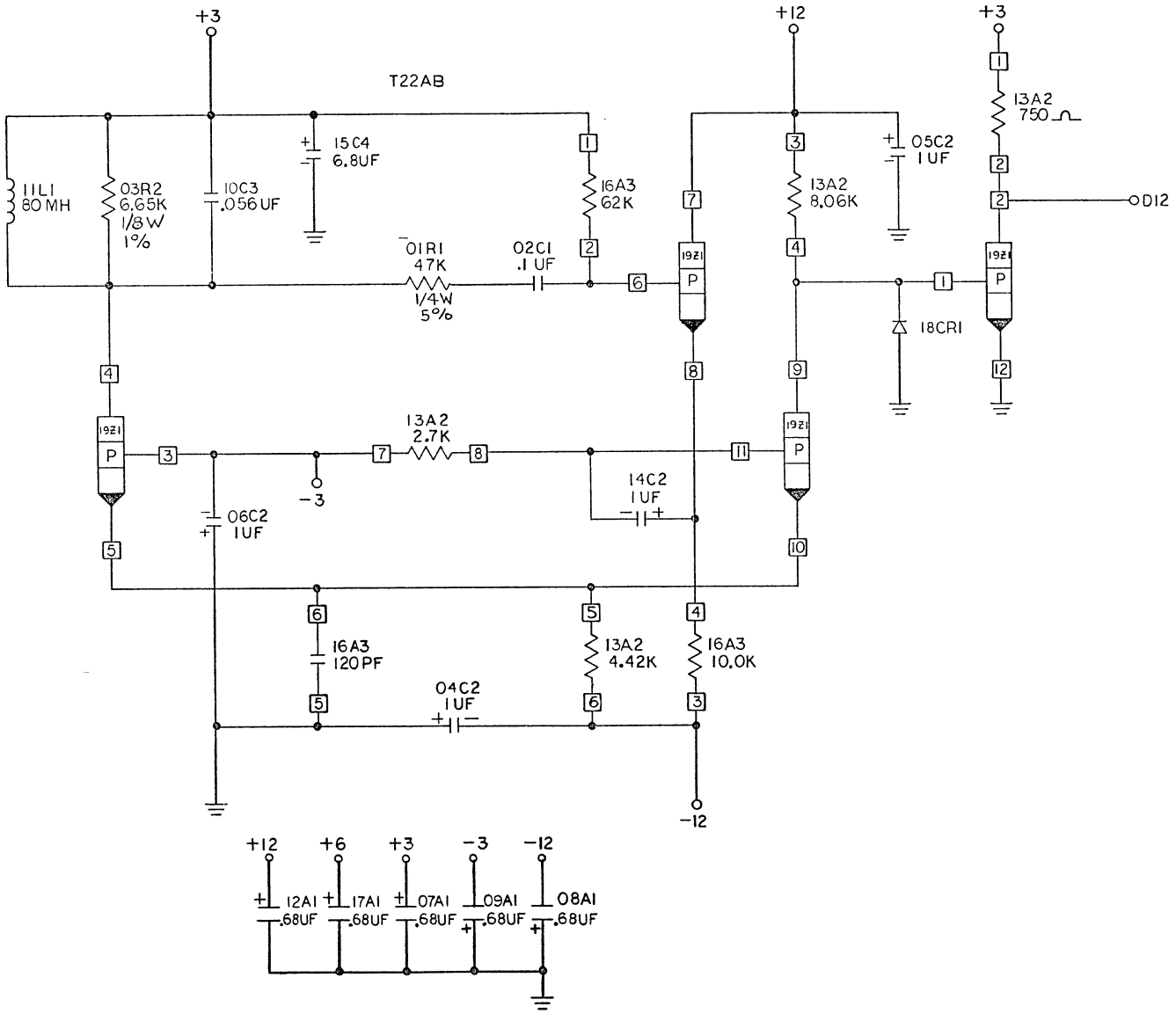
LMH Cat.	0-2860 Subject	321 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 2.0KHZ OSCILLATOR

P/N	5803208
E C	163246A



2 OF 2 Page	1-67 Date	

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
VARIABLE SSA (0.6 TO 450 U SEC)

LMH	0-2860	322
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

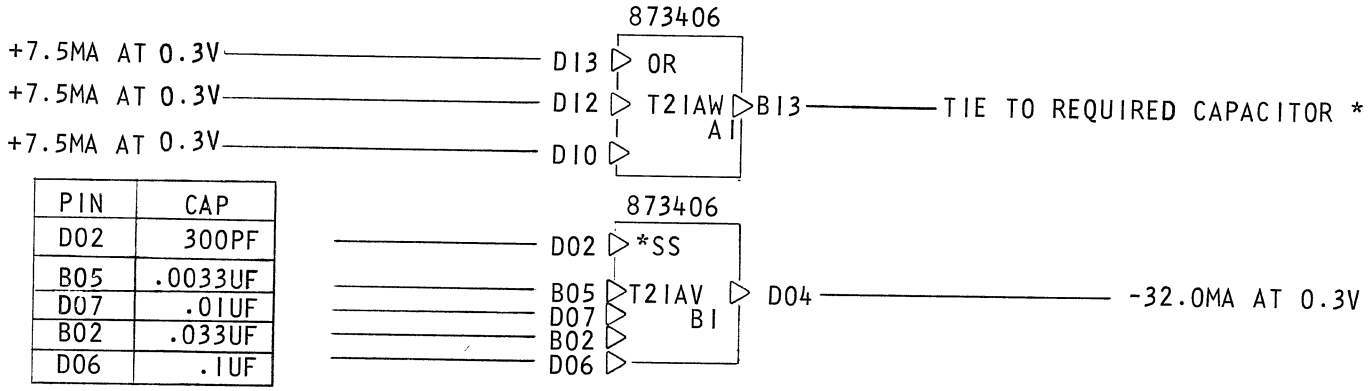
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

VARIABLE SSA (0.6 TO 450 U SEC)

CATEGORY CODE

T21

P/N	5803209
EC	162952
STANDARD RESTRICTED	
CARD SIZE	1 - 12



PIN	CAP
D02	300PF
B05	.0033UF
D07	.01UF
B02	.033UF
D06	.1UF

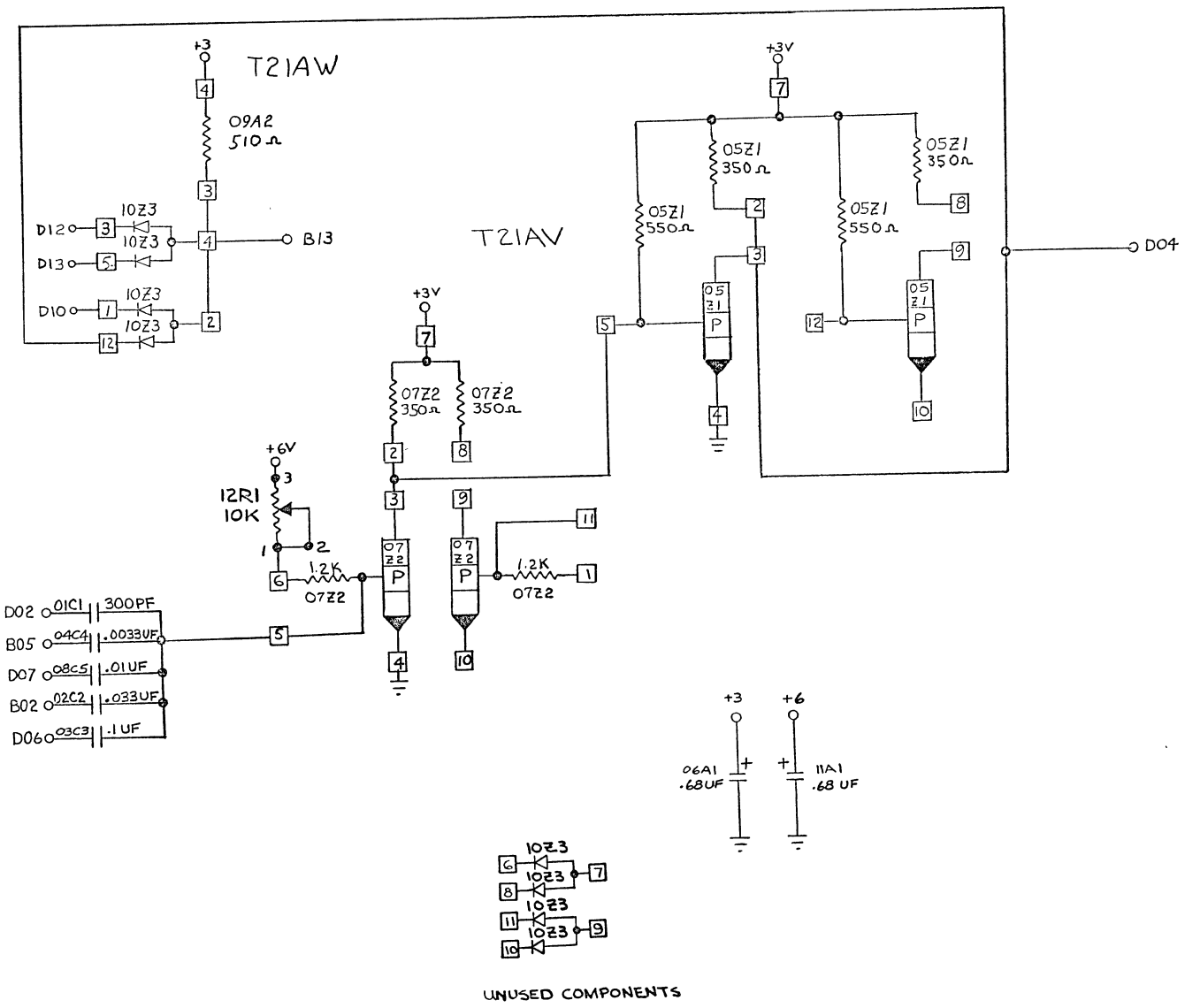
TABLE OF OUTPUT PULSE WIDTH AND RECOVERY TIME

CT	TMAX	TMIN	TRMIN
300PF	1.1US	135NS	600NS
.0033UF	12.0US	1.45US	6.2US
.01UF	37.0US	4.6US	19.0US
.033UF	120US	15.0US	64US
.1UF	370US	45US	190US

LMH Cat.	0-2860 Subject	322 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
VARIABLE SSA (0.6 TO 450 U SEC)

P/N	5803209
E C	162952



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6 GATED AI-DCI WO/L +6 RESISTORS

LMH	0-2860	324
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

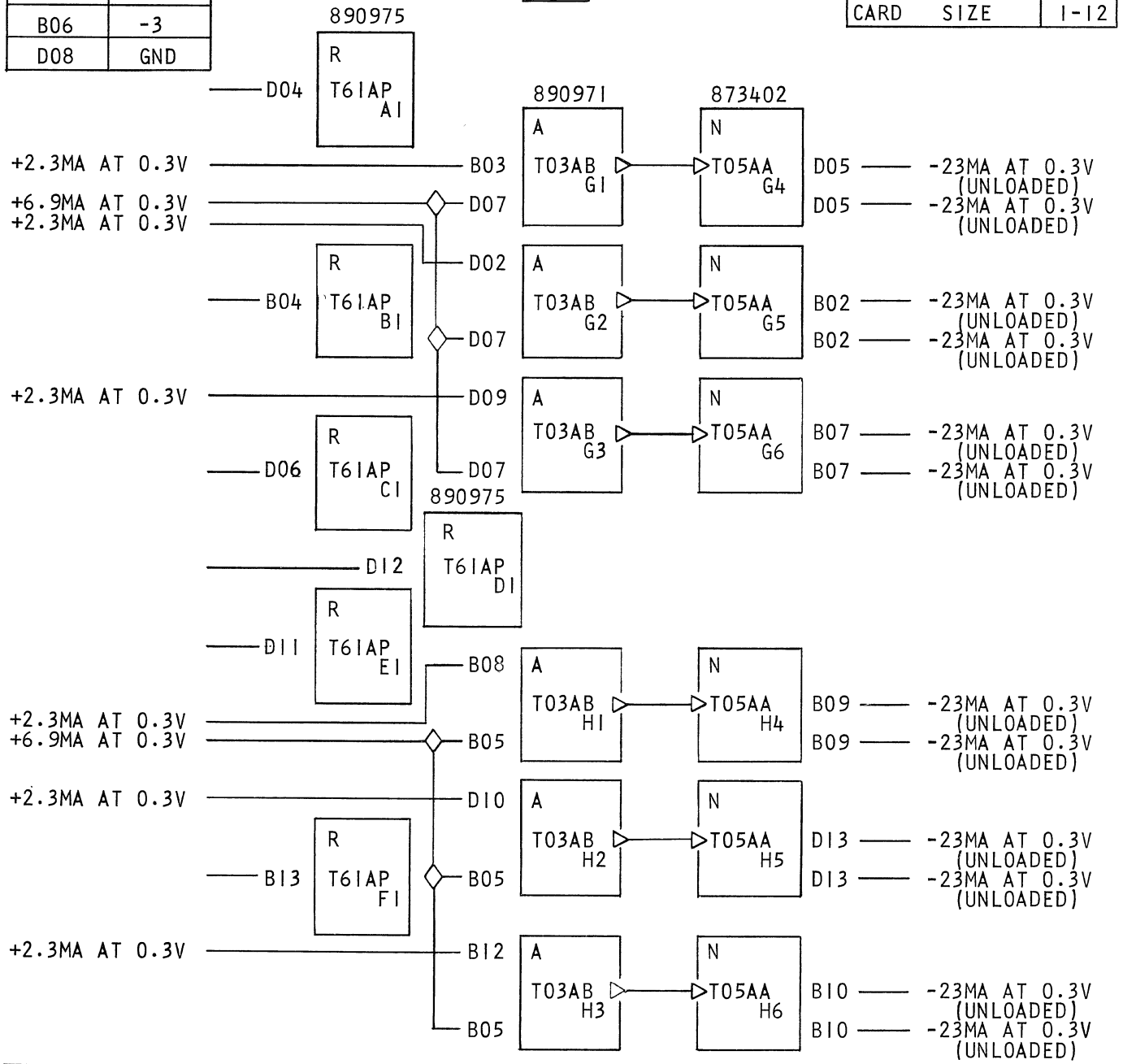
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

6 GATED AI-DCI WO/L +6 RESISTORS

CATEGORY CODE

T65

P/N	5803300	
EC	160485	
STANDARD RESTRICTED		
CARD	SIZE	1-12



06-09	00-00			
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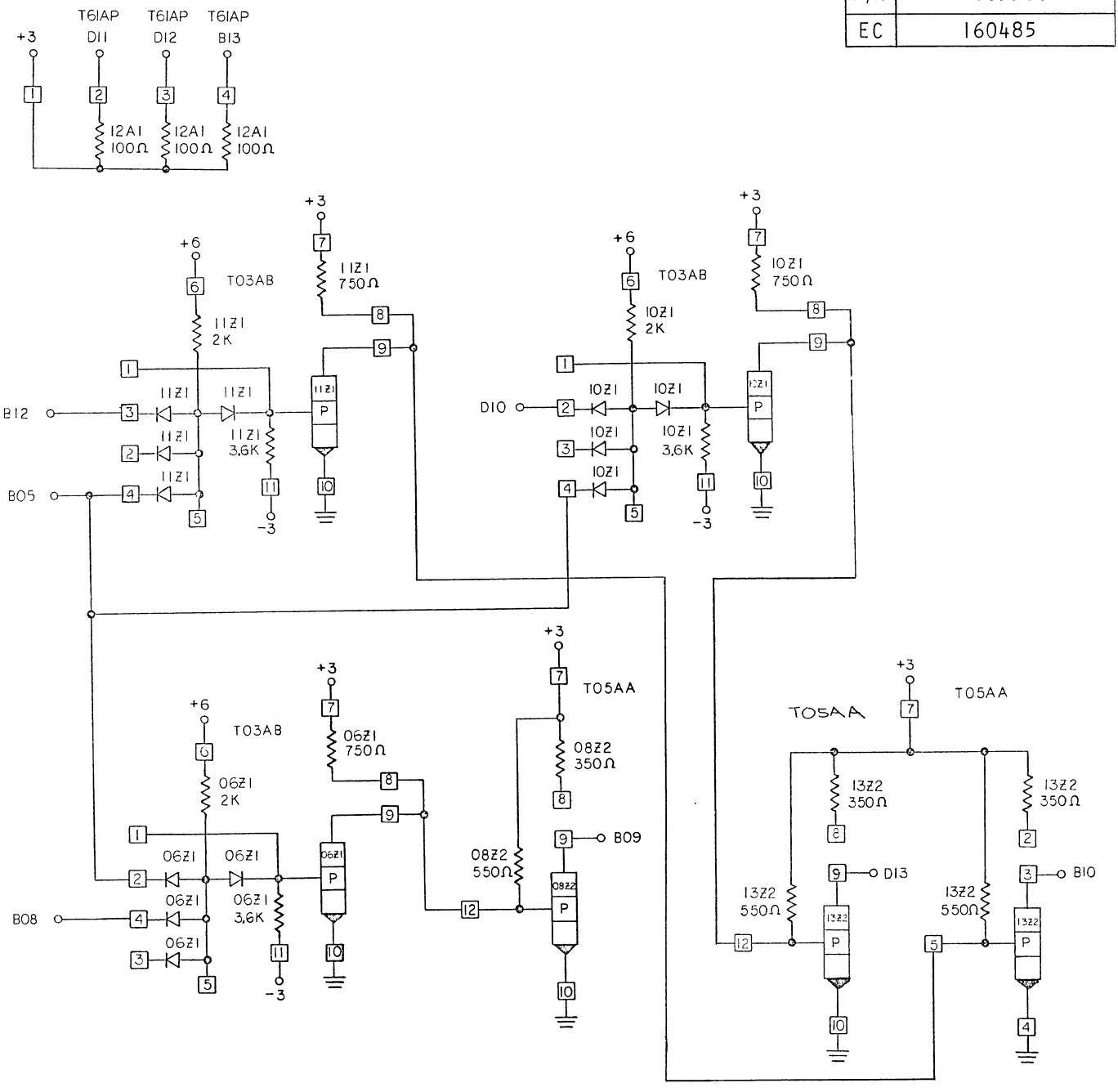
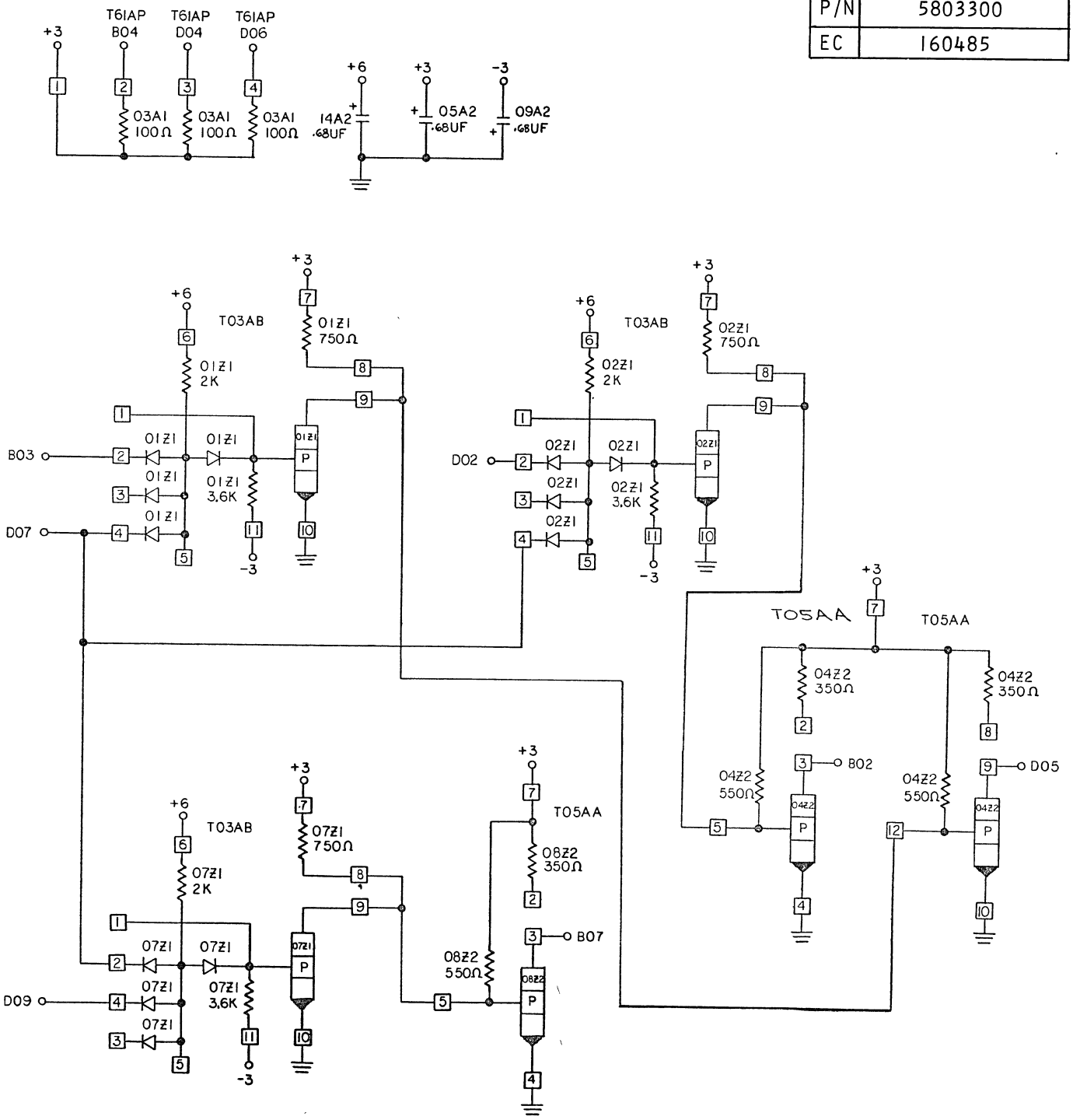
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6 GATED AI-DCI W0/L +6 RESISTORS

P/N	5803300
EC	160485



P/N	5803300
EC	160485



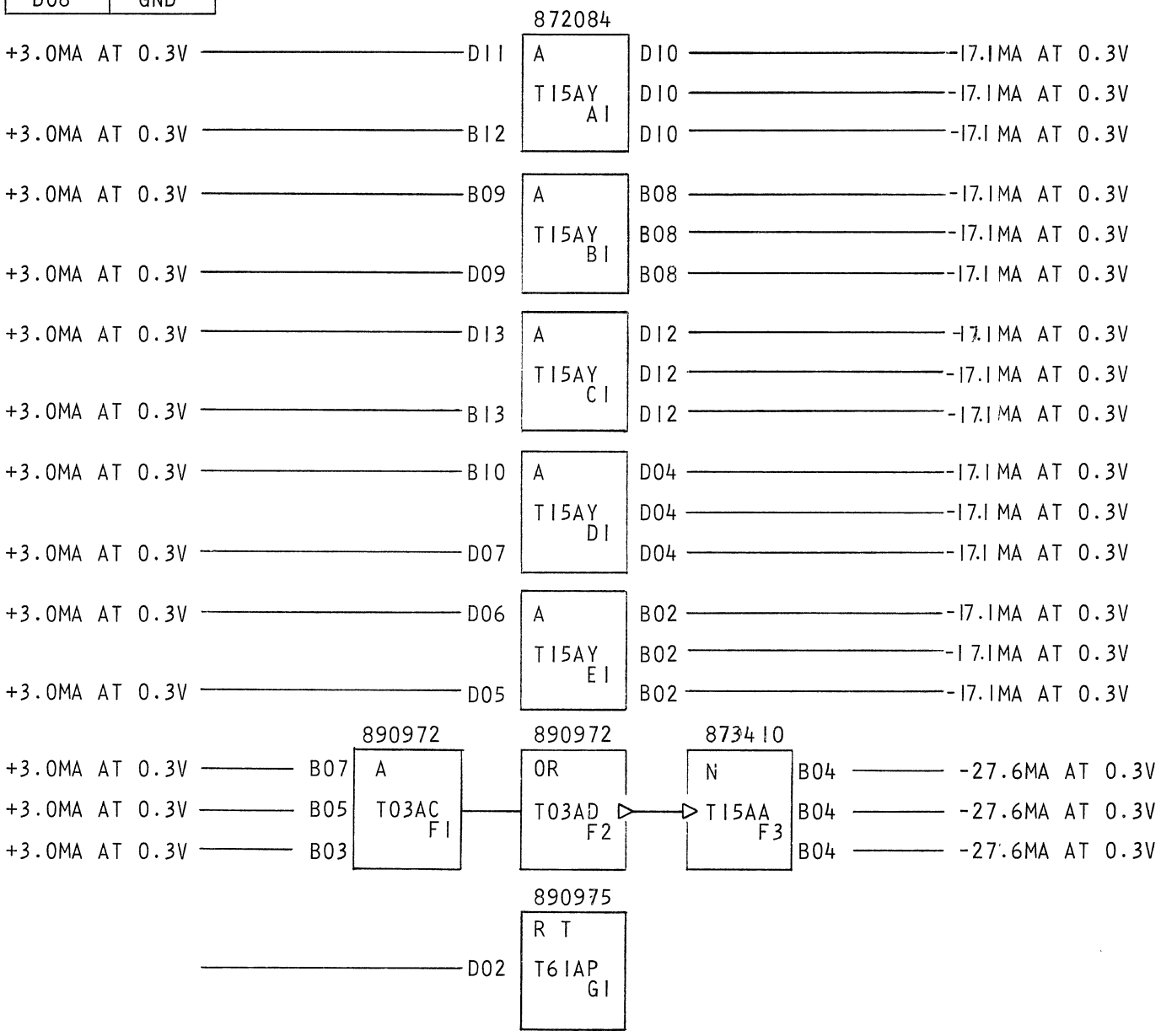
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

6 GATED HIGH POWER DRIVERS

CATEGORY CODE

T15

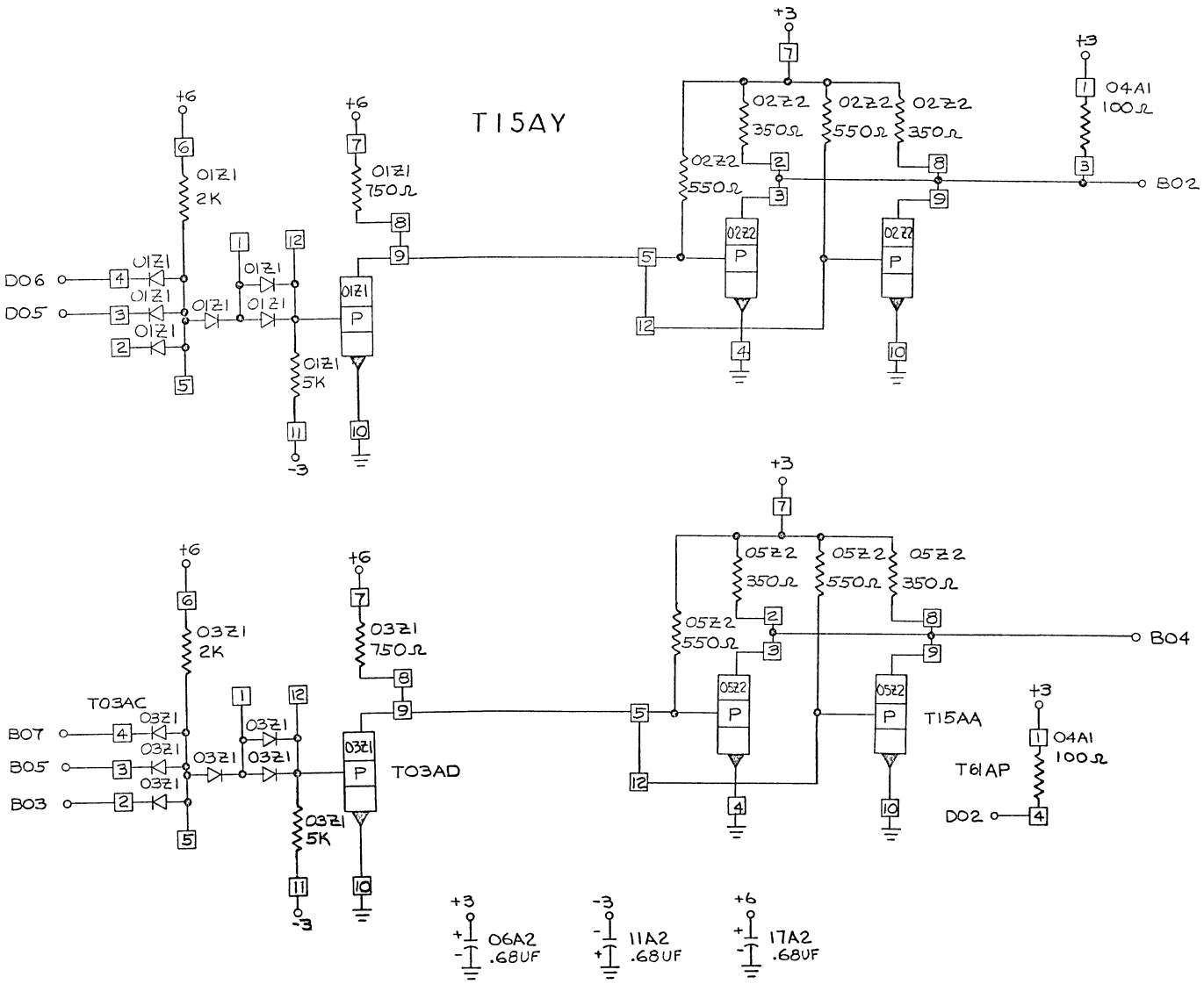
P/N	5803309
EC	161310
STANDARD RESTRICTED	
CARD SIZE	1-12



LMH Cat.	0-2860 Subject	325 Suffix

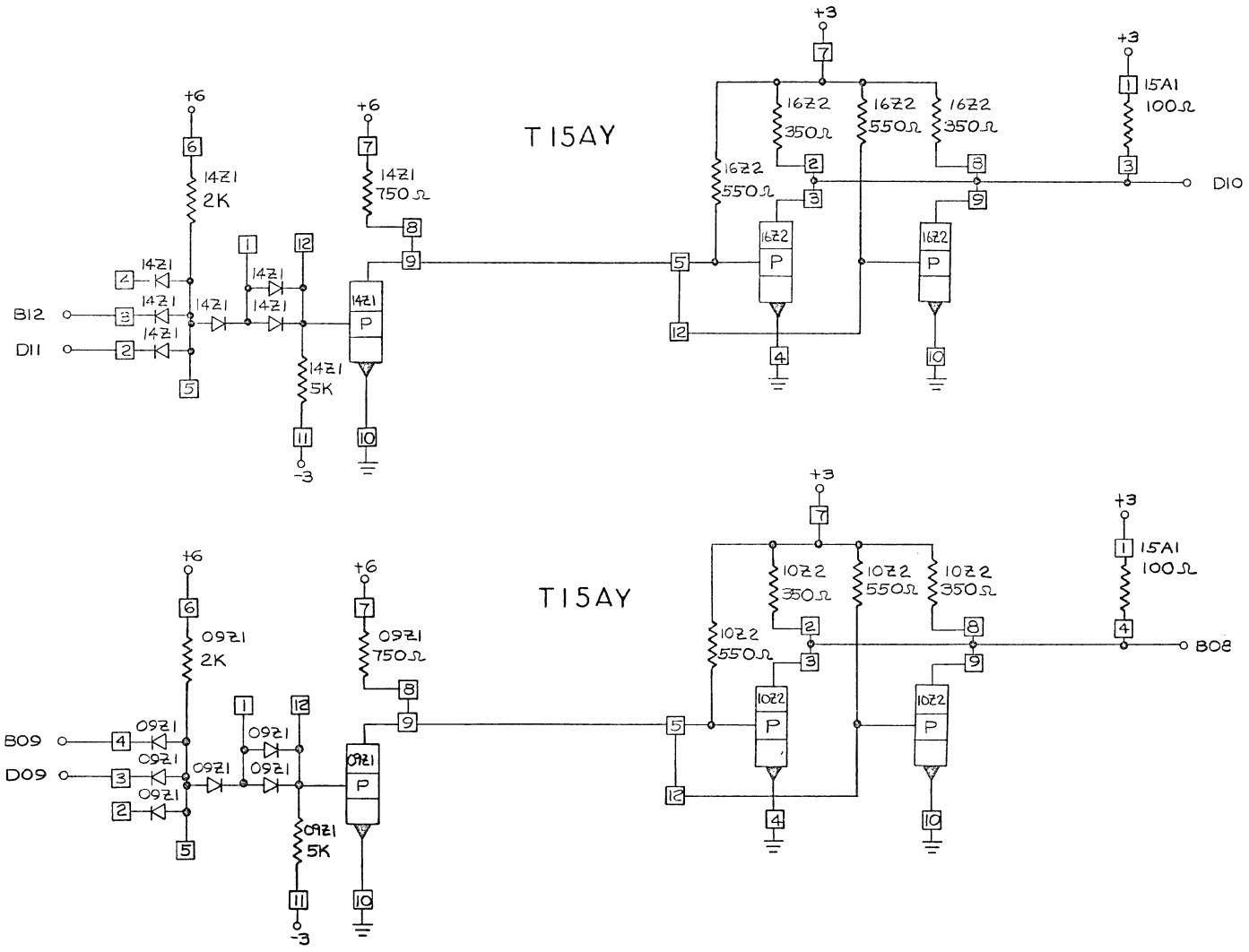
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6 GATED HIGH POWER DRIVERS

P/N	5803309
EC	161310



Page 2	Date Jan. 67

P/N	5803309
EC	161310



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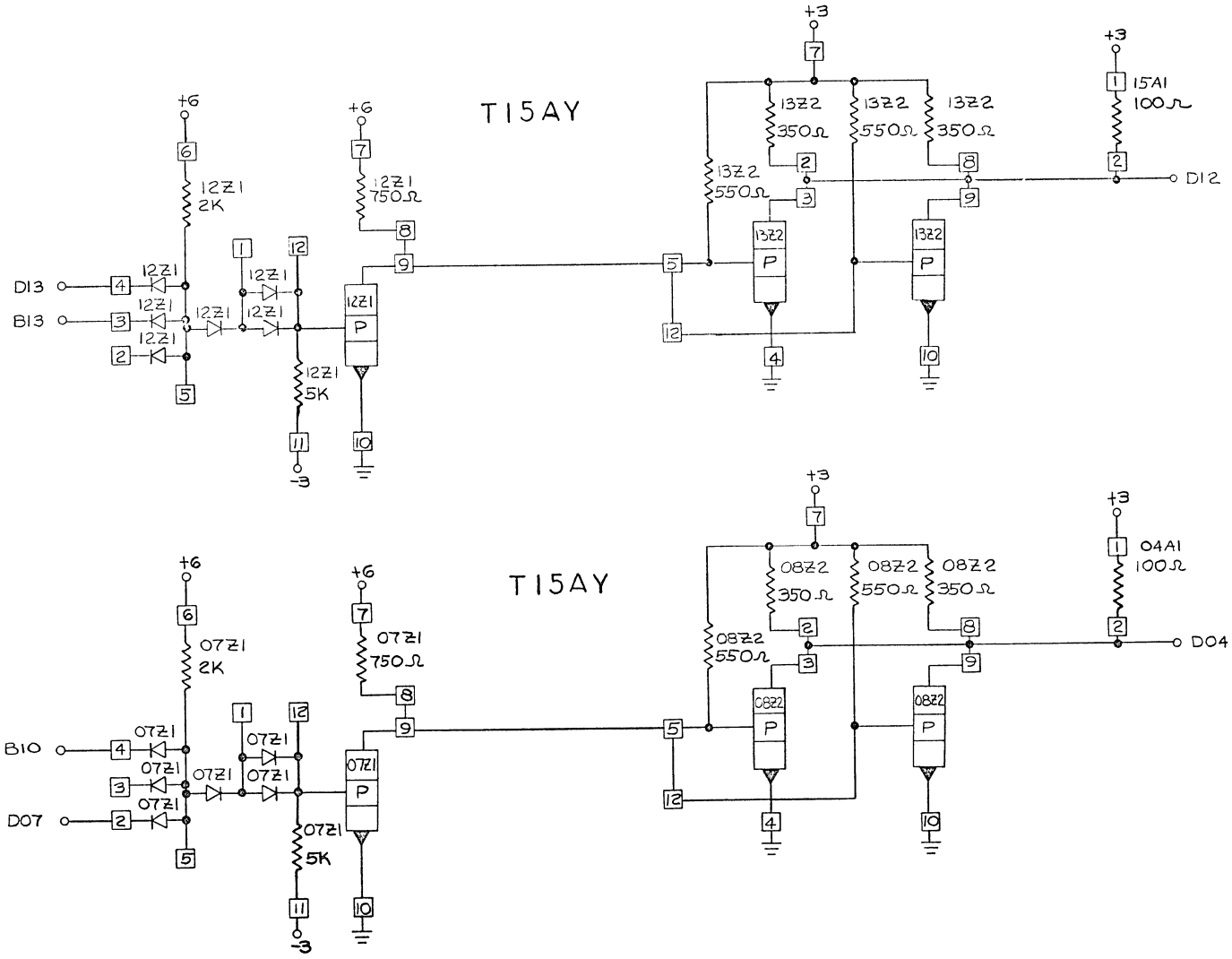
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6 GATED HIGH POWER DRIVERS

P/N	5803309
EC	161310



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
IO MULTIPLEX RECEIVERS

LMH	0-2860	326
Cat	Subject	Suffix

IBM Location Manufacturing Specifications

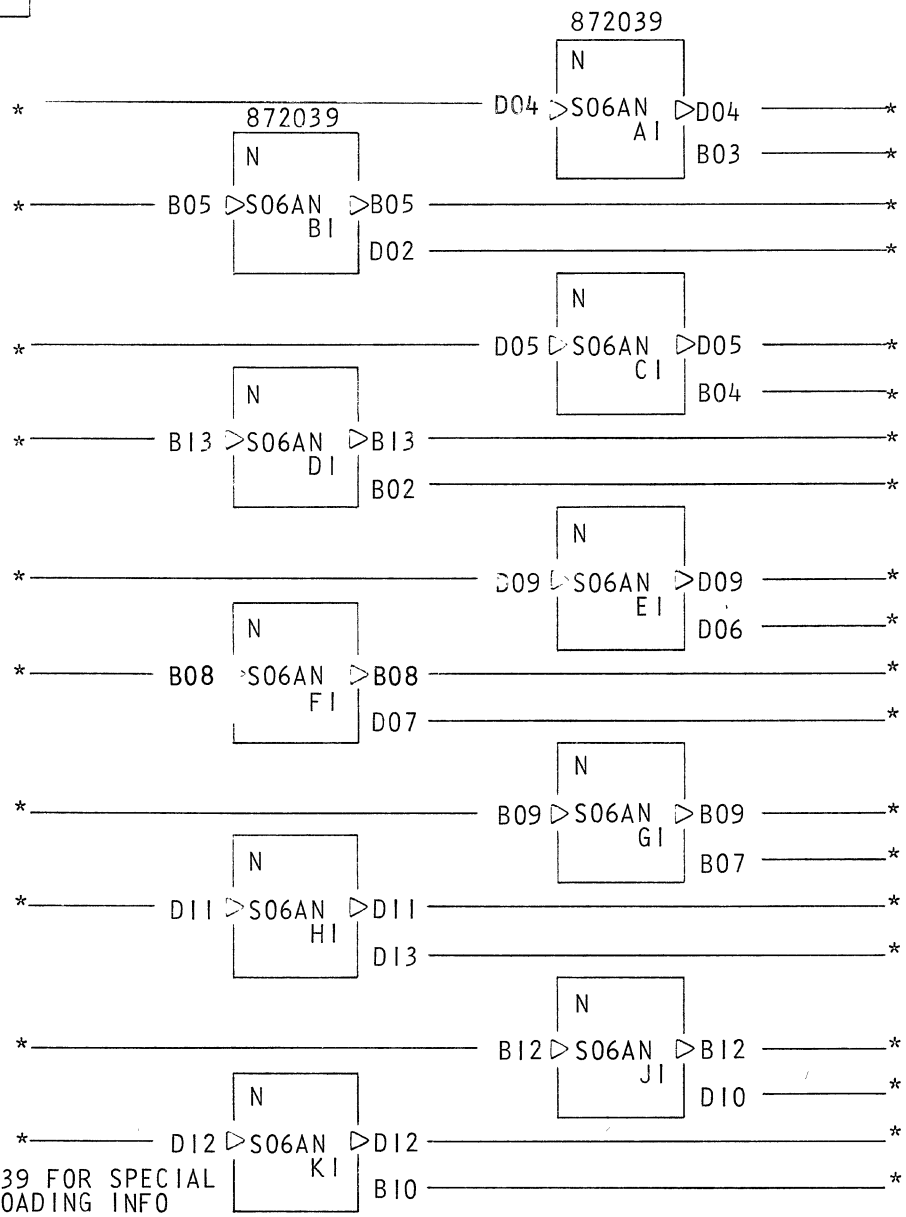
POWER REQUIRED	
PIN	VOLT
B06	-3
B11	+6
D03	+3
D08	GND

IO MULTIPLEX RECEIVERS

CATEGORY CODE

S06

P/N	5803325
EC	160180
SPECIAL RESTRICTED	
CARD SIZE	1-12



*SEE SPEC 872039 FOR SPECIAL DRIVING AND LOADING INFO

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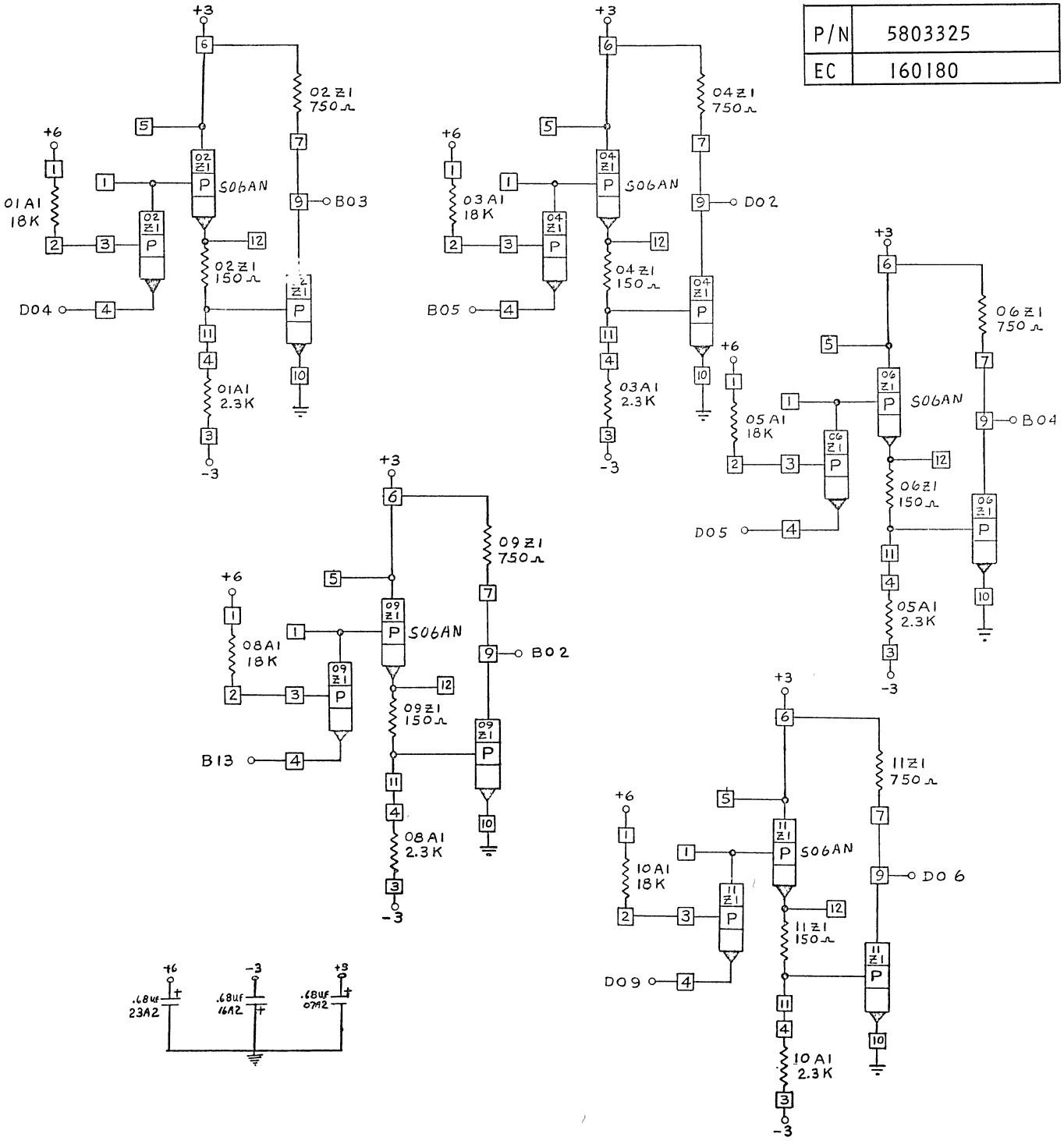
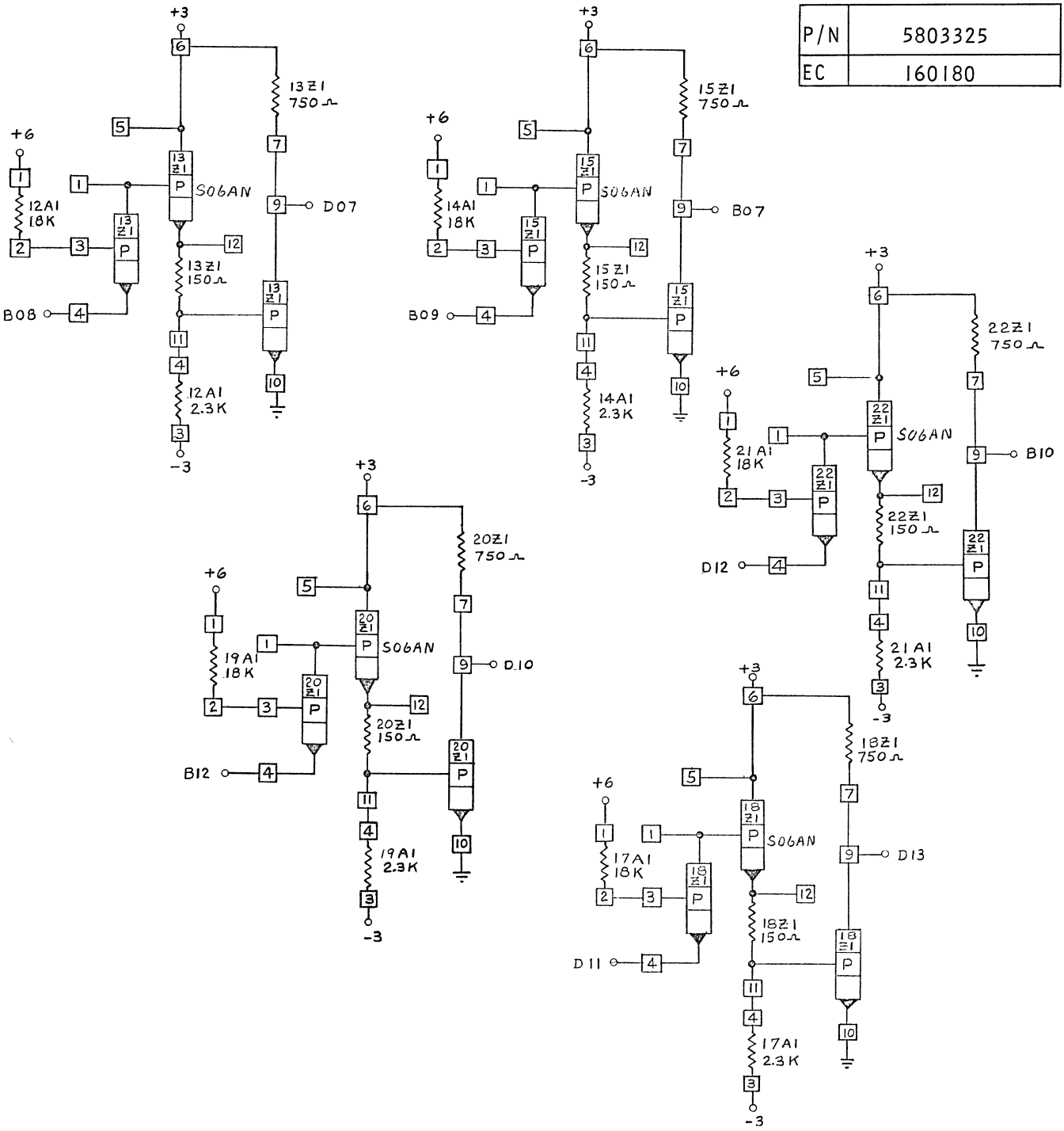
LMH Cat.	O-2860 Subject	326 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
10 MULTIPLEX RECEIVERS

P/N	5803325
EC	160180



P/N	5803325
EC	160180



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-300 MA DRIVERS

LMH	0-2860	329
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

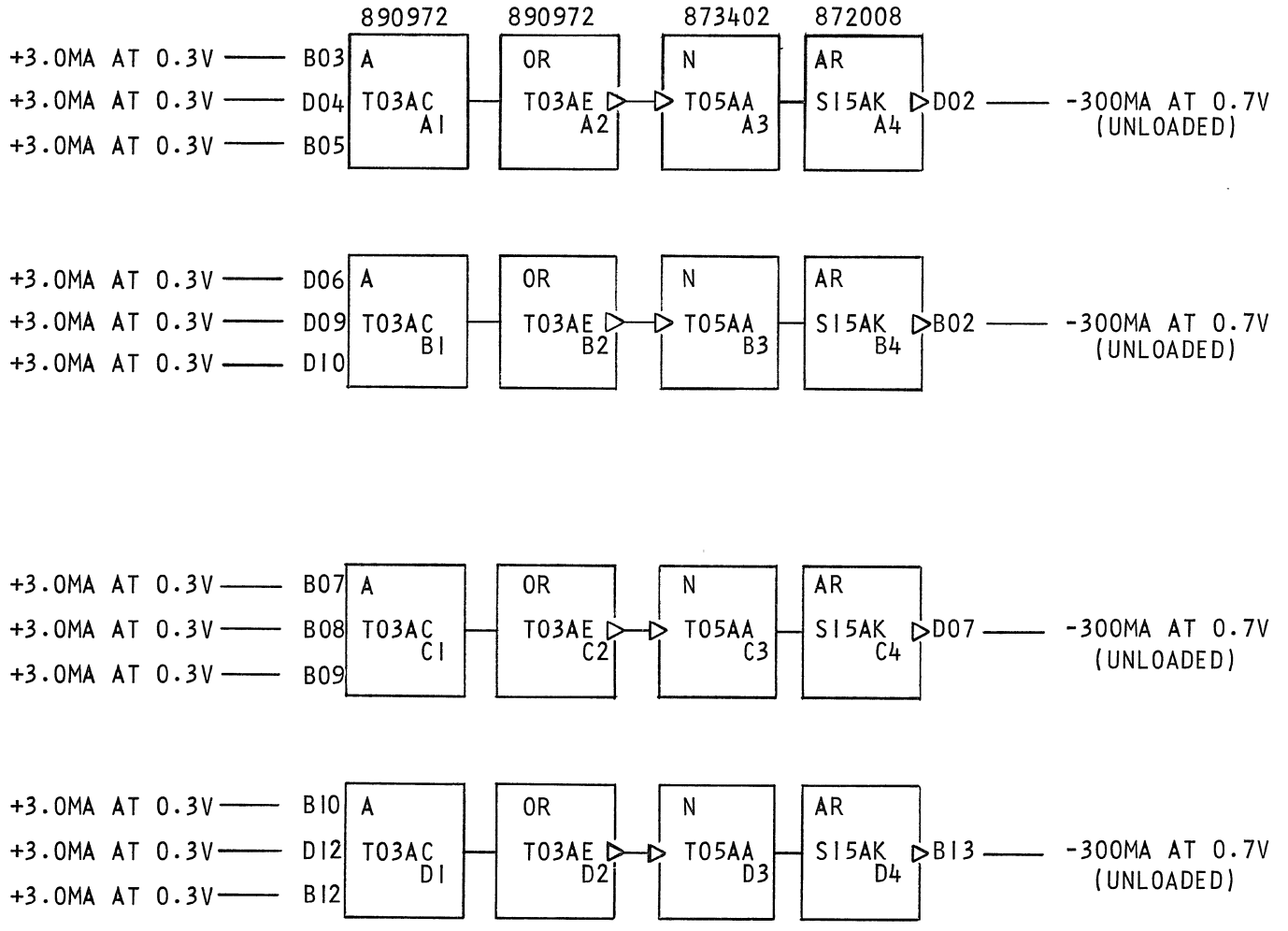
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

4-300 MA DRIVERS

CATEGORY CODE

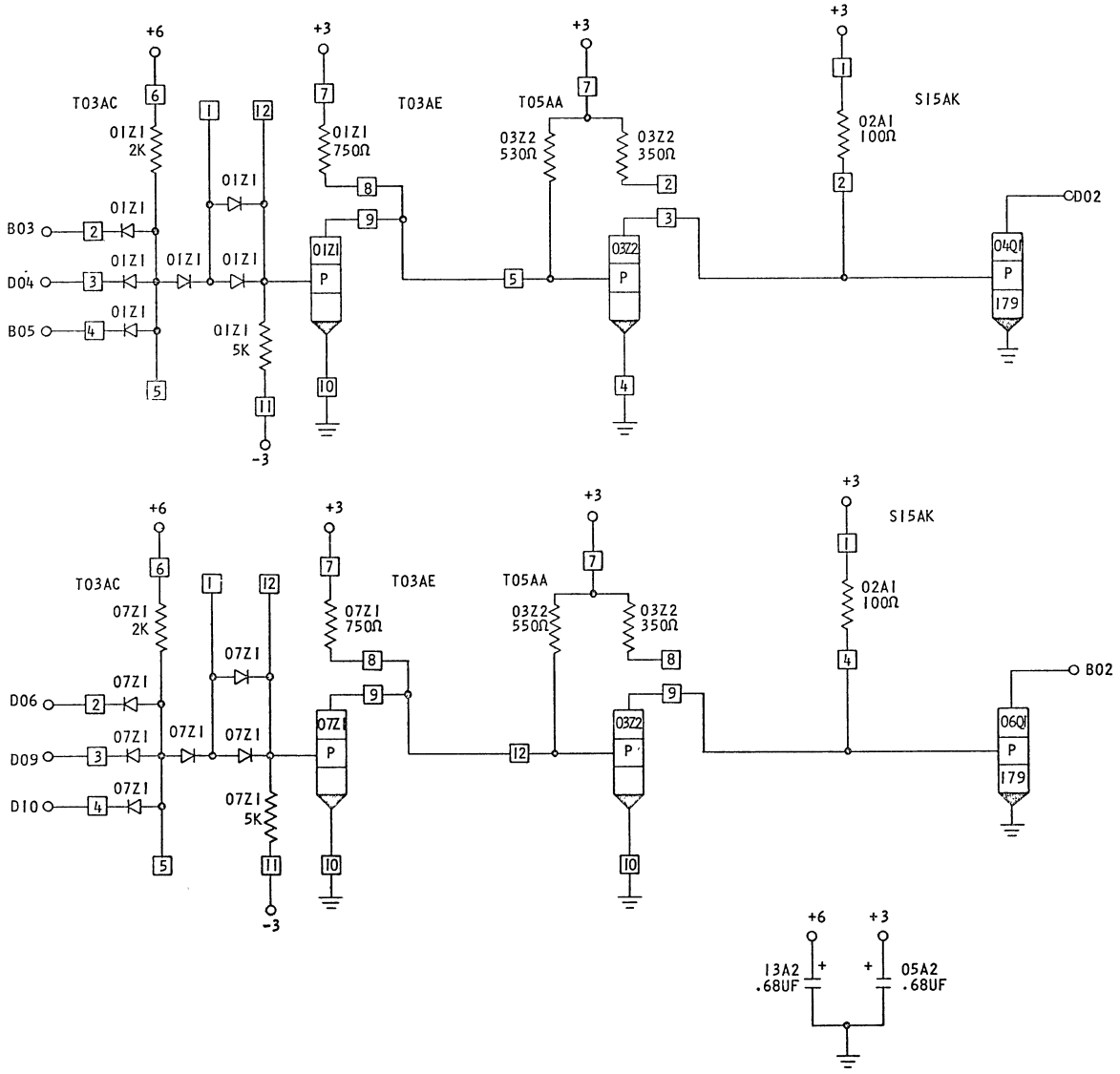
T03

P/N	5803332
EC	160172
SPECIAL	RESTRICTED
CARD SIZE	1-12

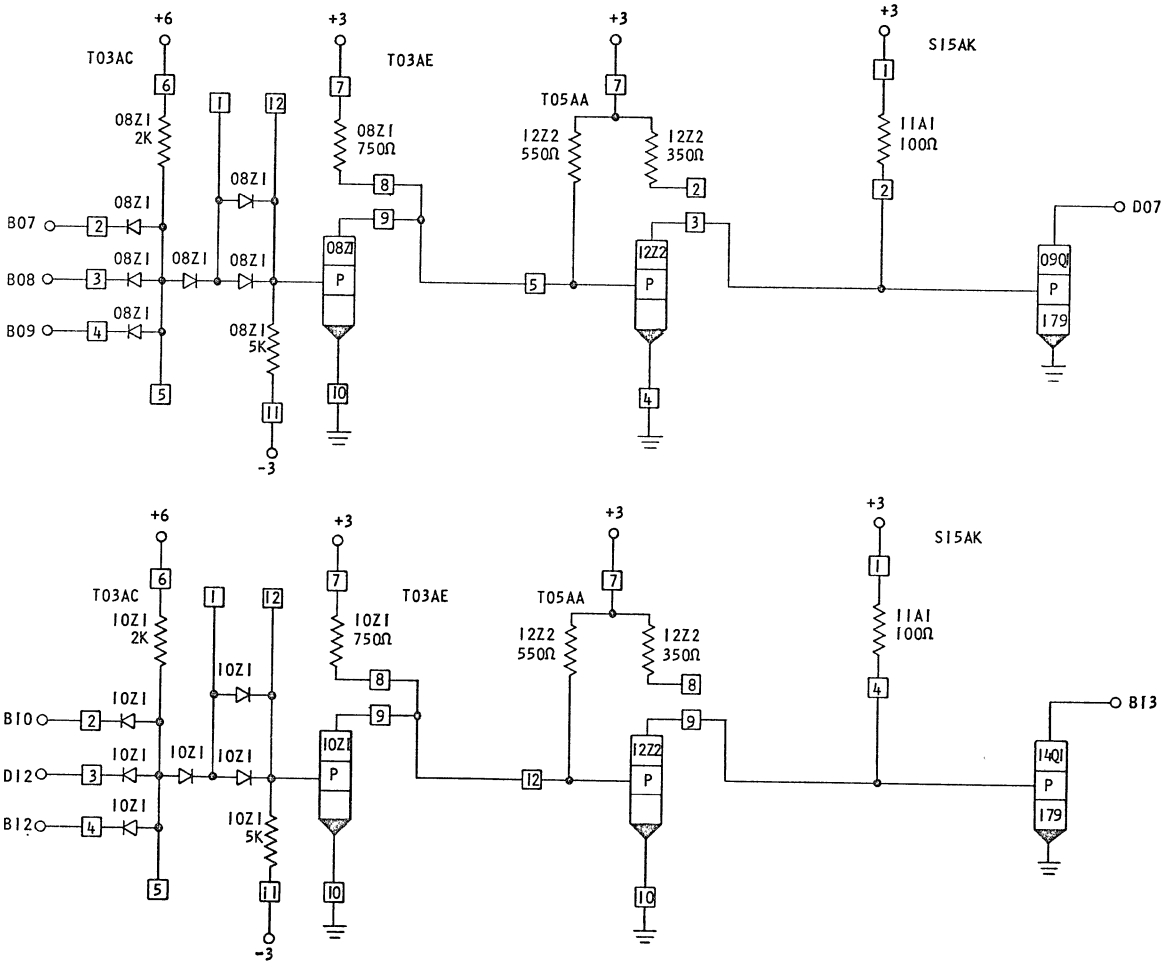


SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-300 MA DRIVERS

P/N	5803332
EC	160172



P/N	5803332
EC	160172



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-SSA, 1-3W AI

LMH (Cat.)	0-2860 (Subject)	330 (Suffix)

IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2-SSA, 1-3W AI

CATEGORY CODE

T03	T21

P/N	5800334 5803333
EC	163836
STANDARD	RESTRICTED
CARD SIZE	1-12

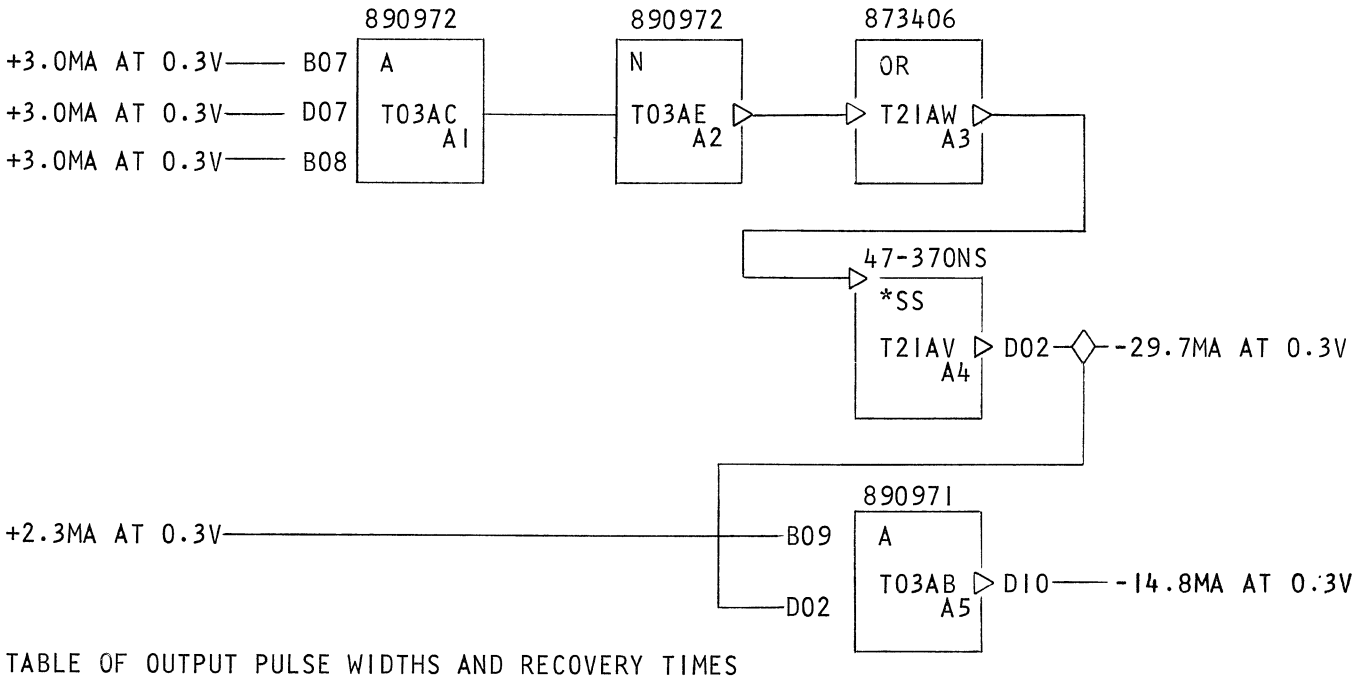


TABLE OF OUTPUT PULSE WIDTHS AND RECOVERY TIMES

CT	TMAX	TMIN	TR MIN
100PF	370NS	47NS	190NS
33UF	115MS	15.5MS	67MS
.01UF	37.0US	4.6US	19.0US
.0033UF	12.0US	1.45US	6.2US

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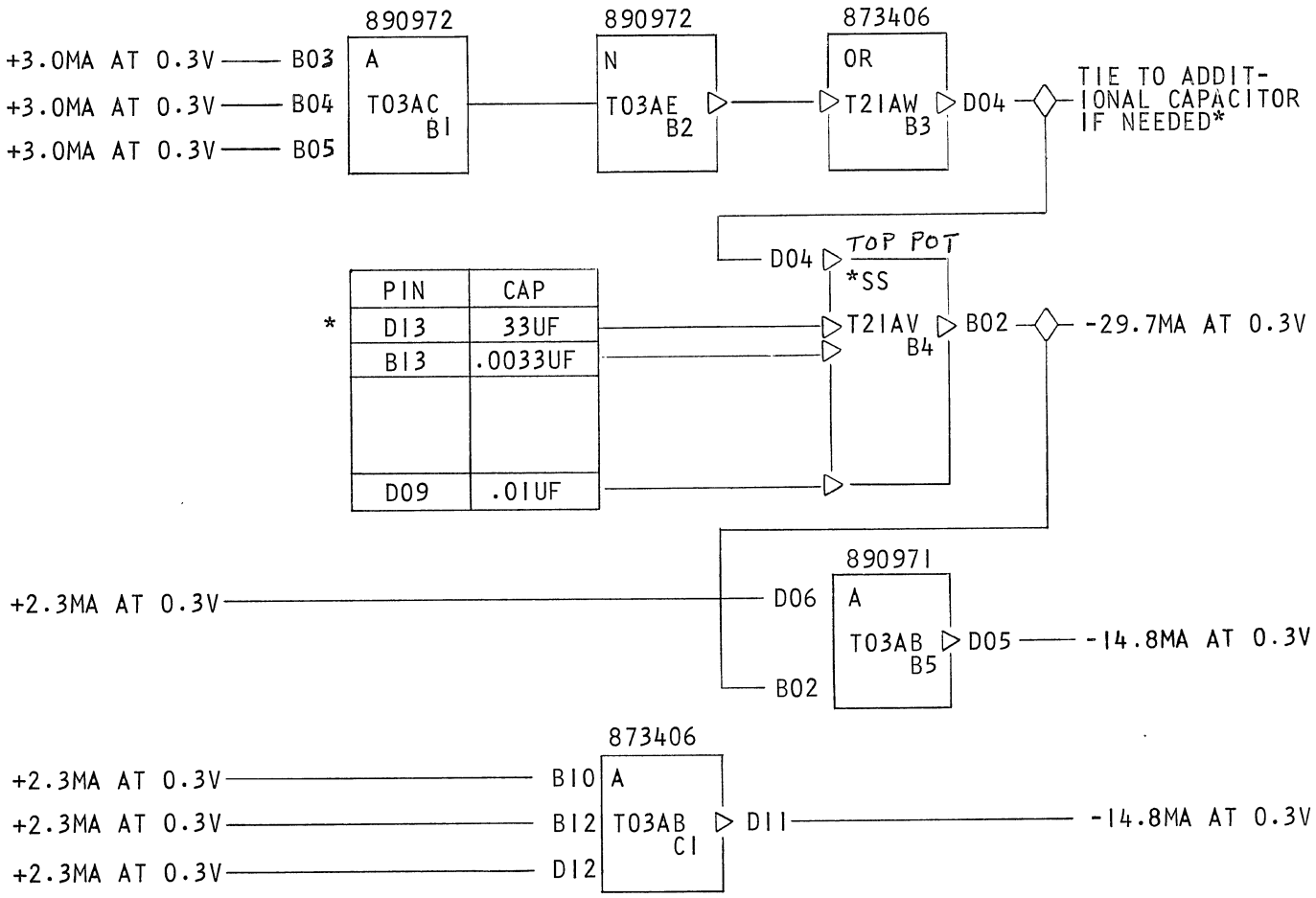
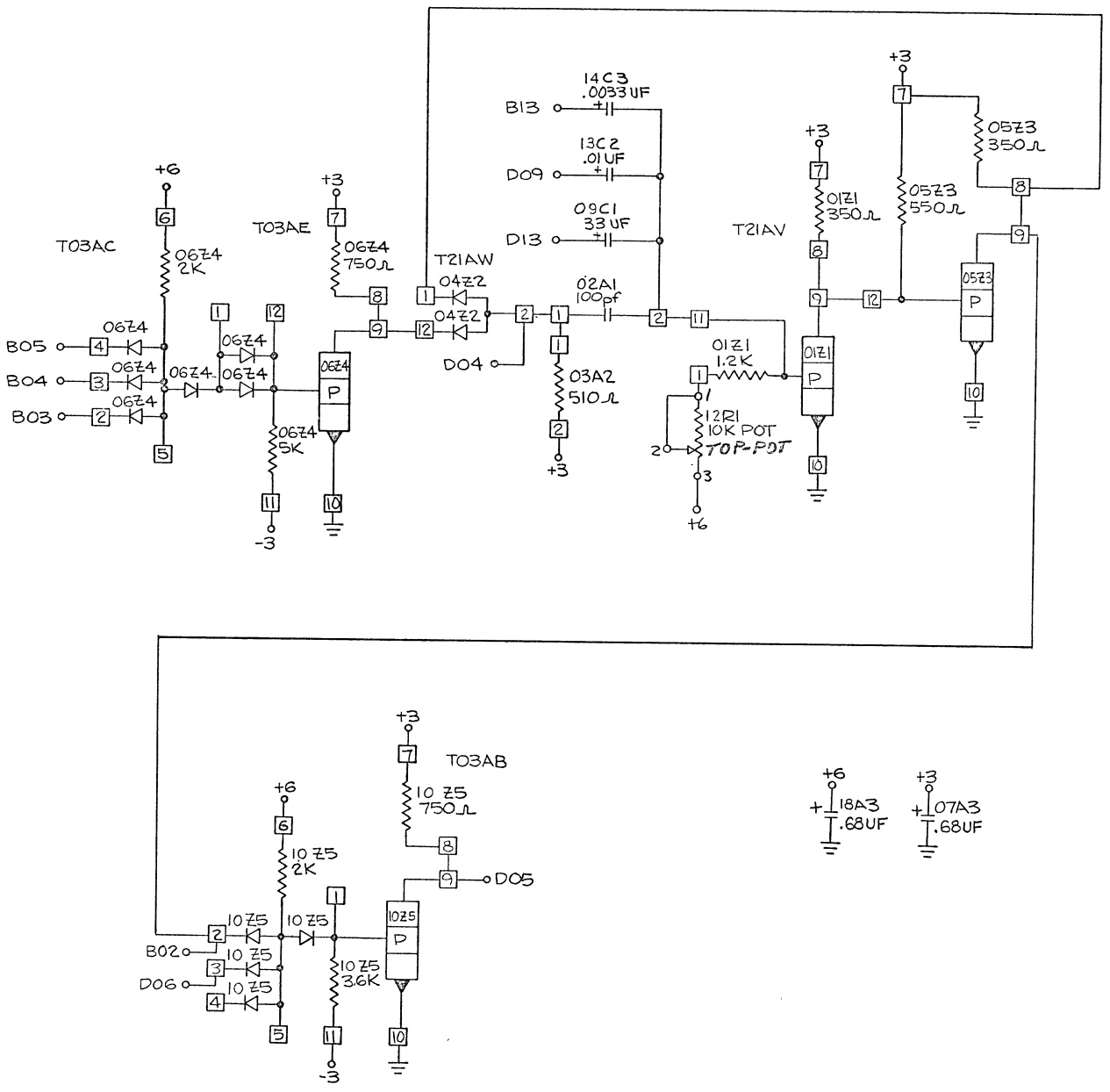
2-SSA, I-3W AI	
T03	T21

P/N	5803333
EC	163836

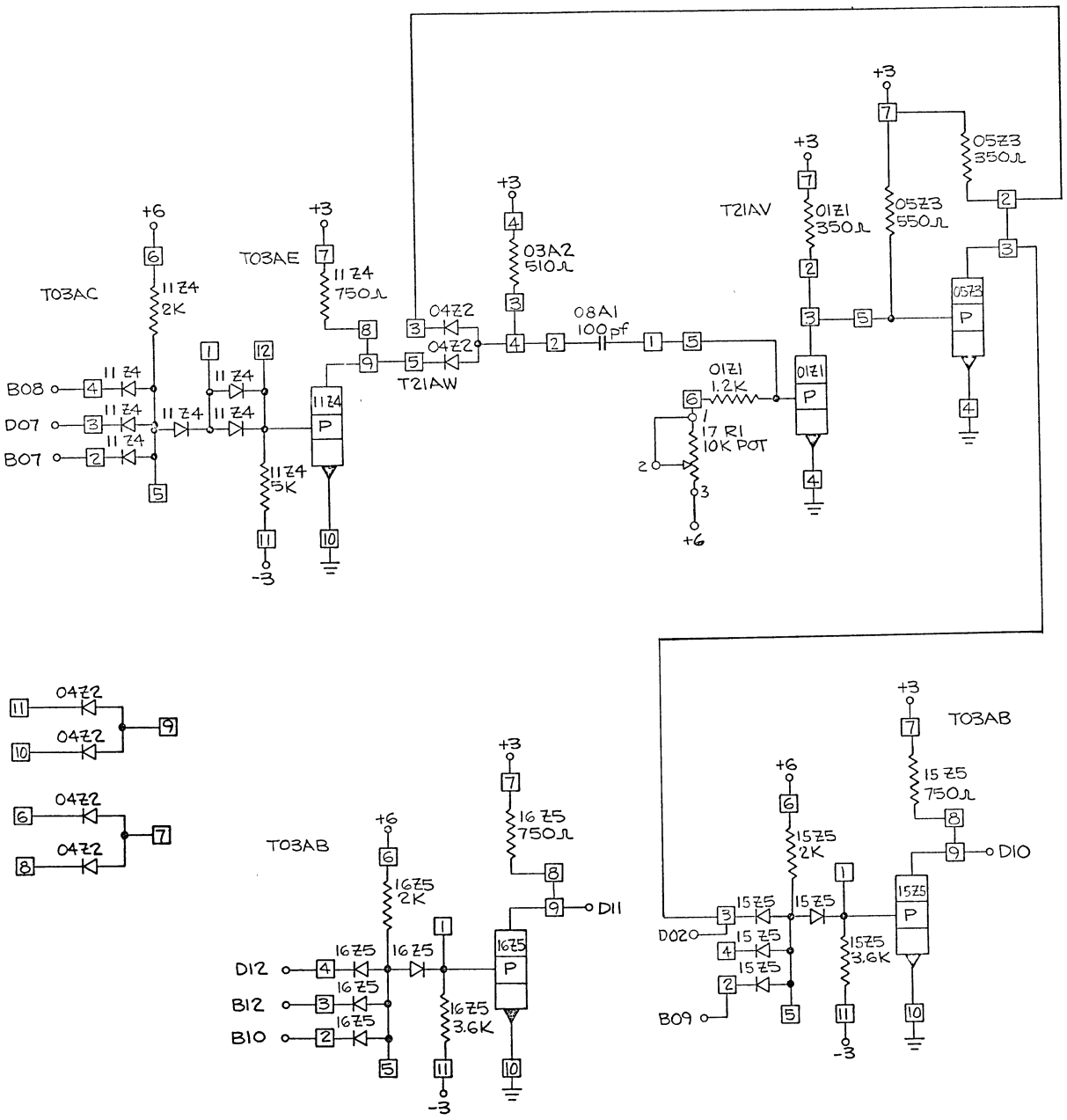


P/N	5803333
EC	163836



LMH Cat.	0-2860 Subject	330 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 2-SSA, 1-3W AI

P/N	5803333
EC	163836



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
LEADING EDGE TIME DELAY 12MS-2.9 SEC

LMH	0-2860	331
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

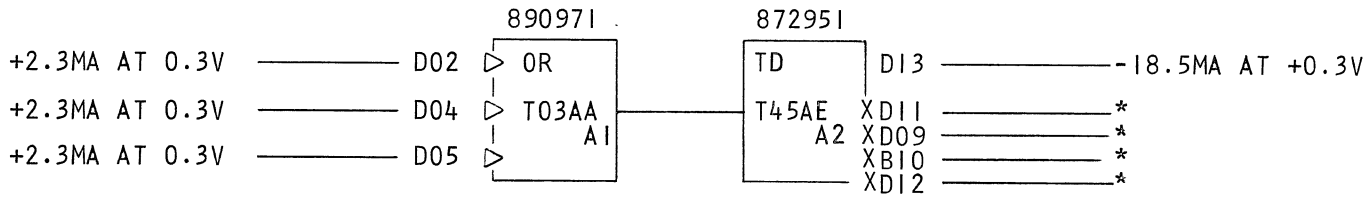
POWER REQUIRED	
PIN	VOLTS
D03	+3
B11	+6
B06	-3
D08	GND
B08	+12

LEADING EDGE TIME DELAY 12MS-2.9 SEC

CATEGORY CODE

T45

P/N	5803337
EC	163472
STANDARD RESTRICTED	
CARD SIZE	1-12

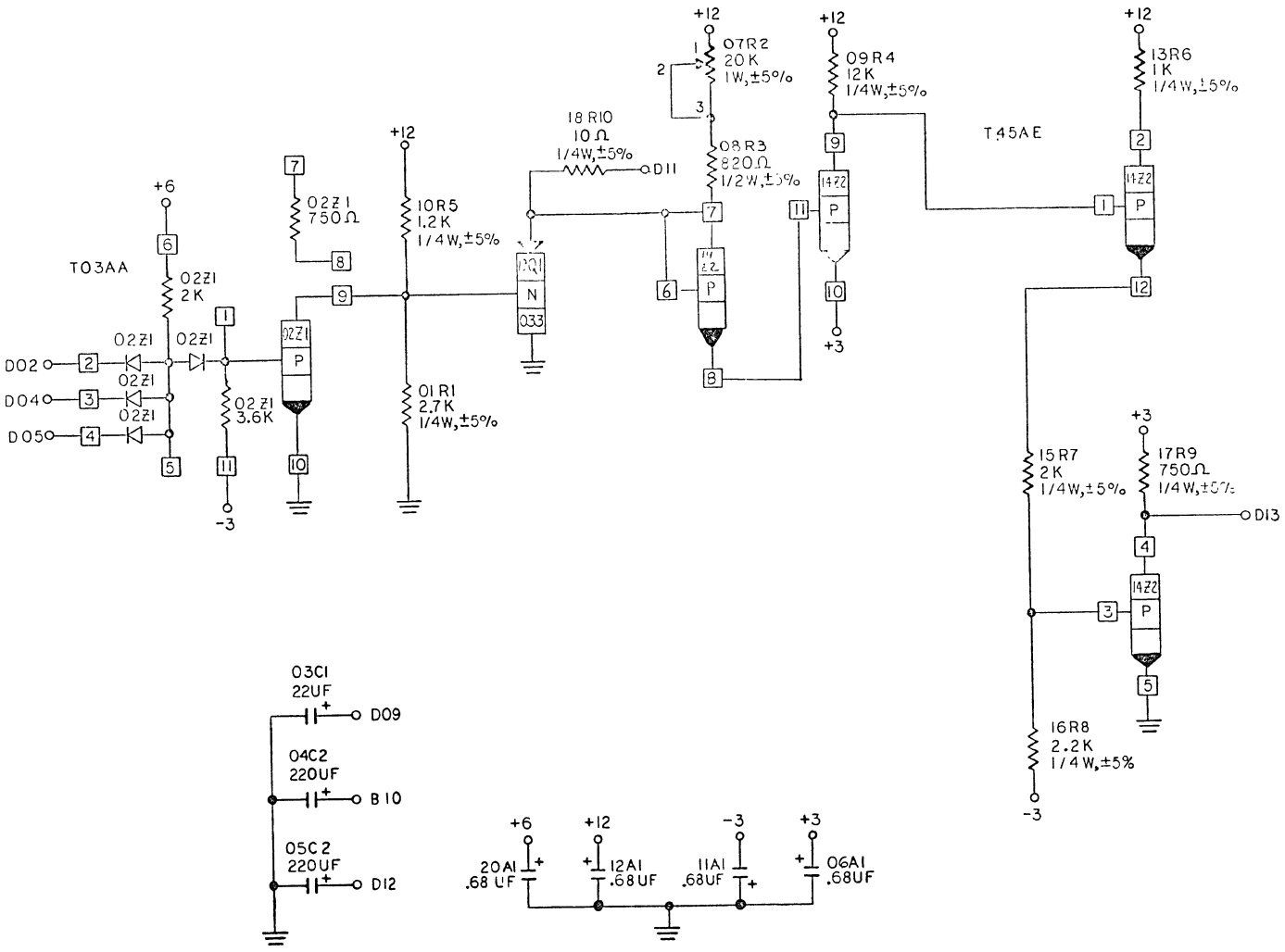


* SEE CIRCUIT SPEC 872951 FOR TIMING CONNECTION.

LMH Cat.	0-2860 Subject	331 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
LEADING EDGE TIME DELAY 12MS-2.9 SEC

P/N	5803337
EC	163472



2 OF 2 Page	1-67 Date	

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-VARIABLE SSA (15.5 TO 115M SEC)

LMH	0-2860	333
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

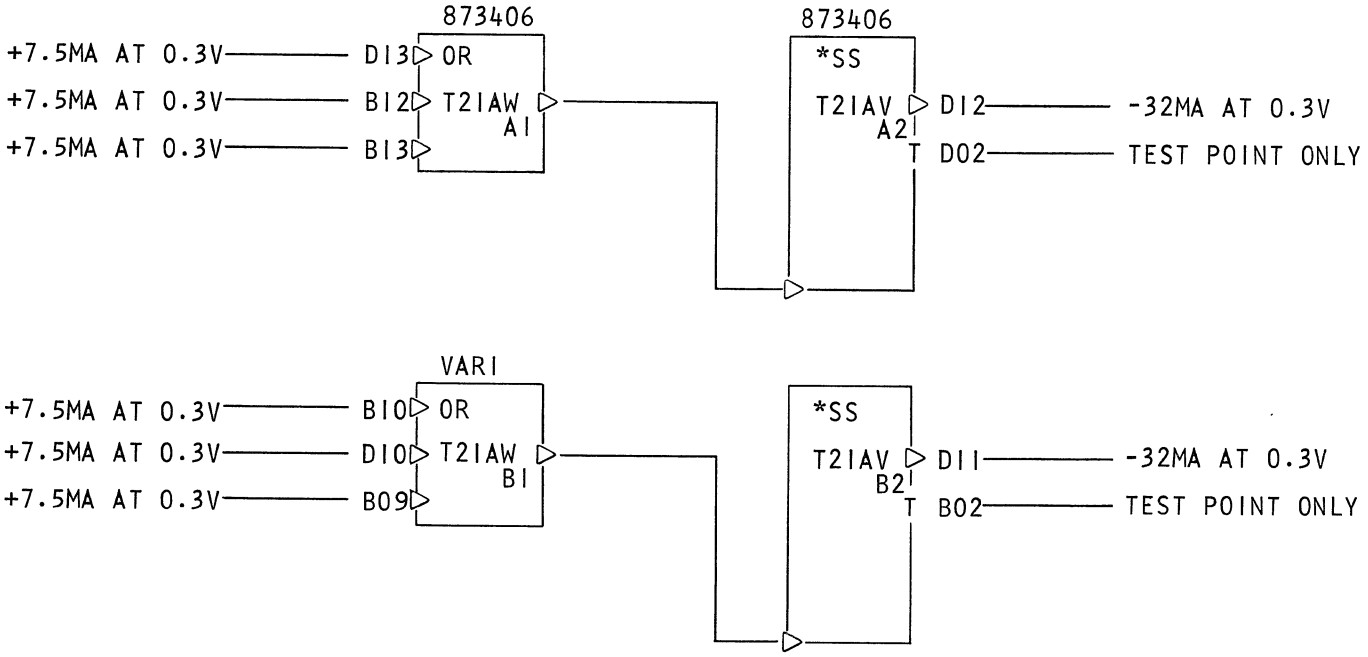
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
D08	GND

2-VARIABLE SSA (15.5 TO 115M SEC)

CATEGORY CODE

T21

P/N	5803340
EC	164574
STANDARD RESTRICTED	
CARD SIZE	1-12



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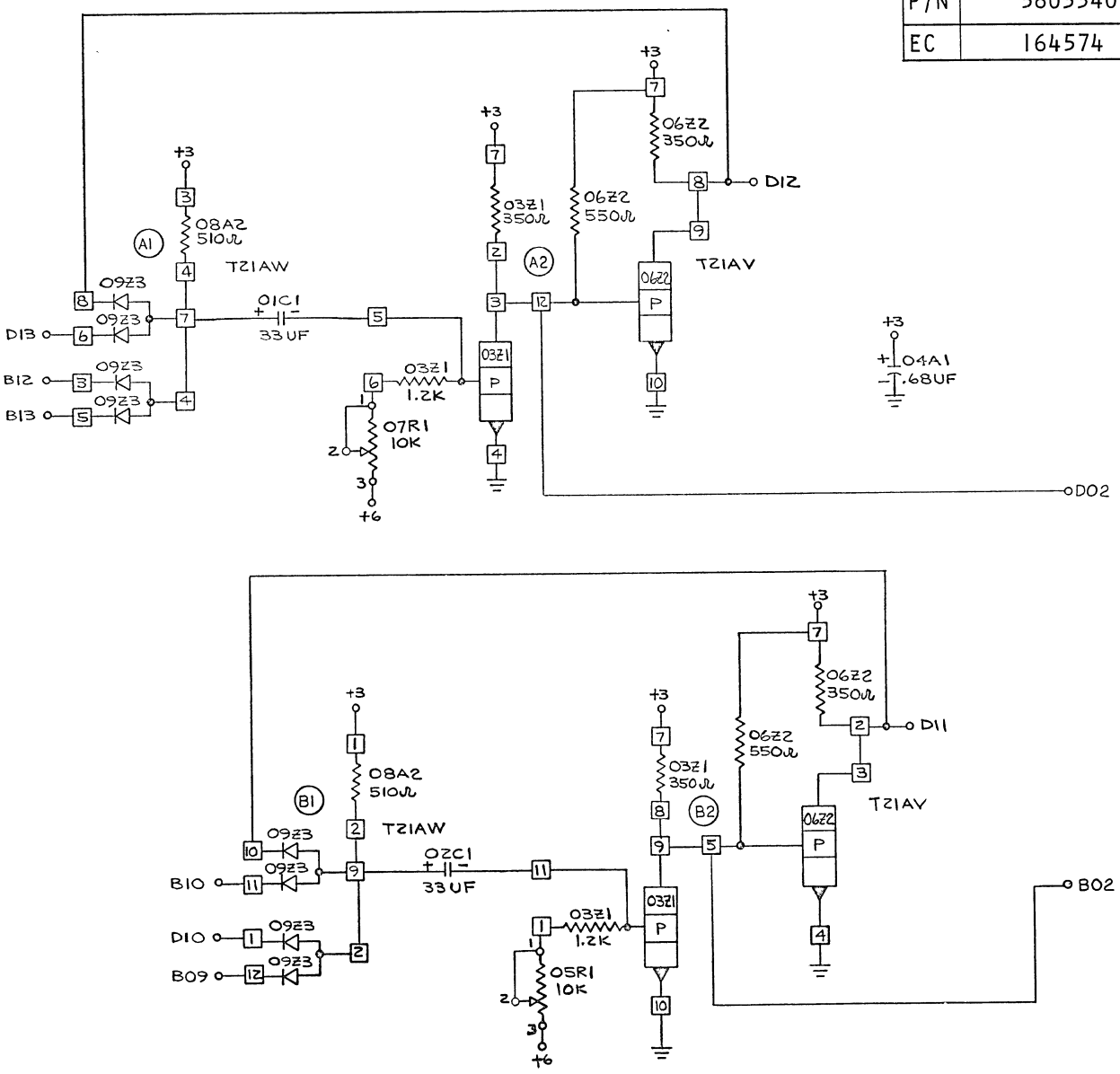
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-VARIABLE SSA (15.5 TO 115M SEC)

P/N	5803340
EC	164574



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-VARIABLE SSA (1.45 TO 12.0U SEC)

LMH	0-2860	334
Cat.	Subject	Suffix

IBM Location Manufacturing Specifications

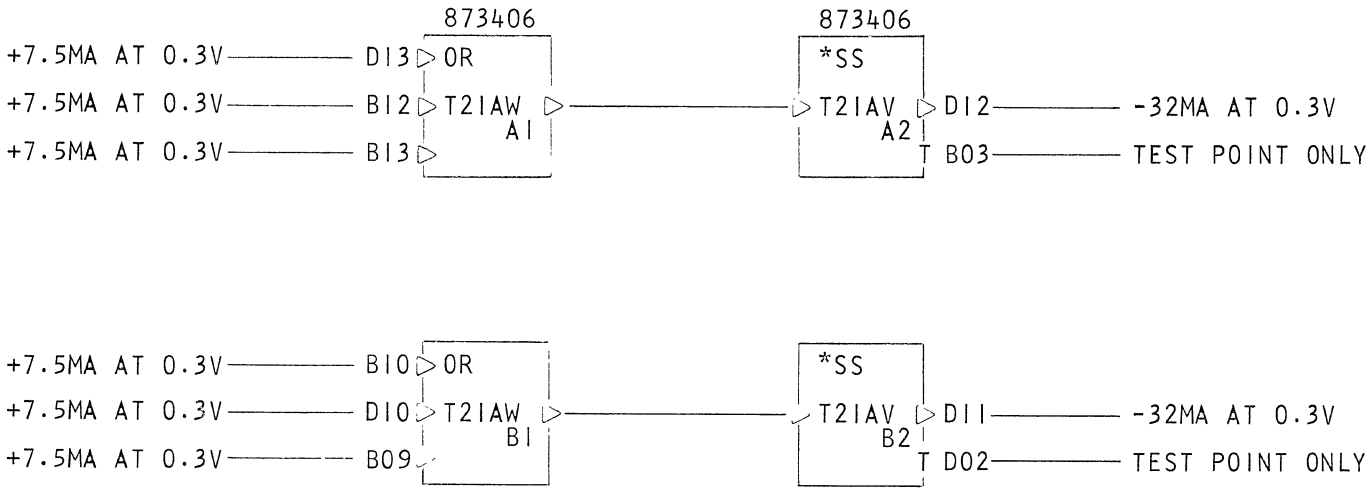
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
D08	GND

2-VARIABLE SSA (1.45 TO 12.0U SEC)

CATEGORY CODE

T21

P/N	5803341	
EC	167467	
STANDARD RESTRICTED		
CARD SIZE		1-12



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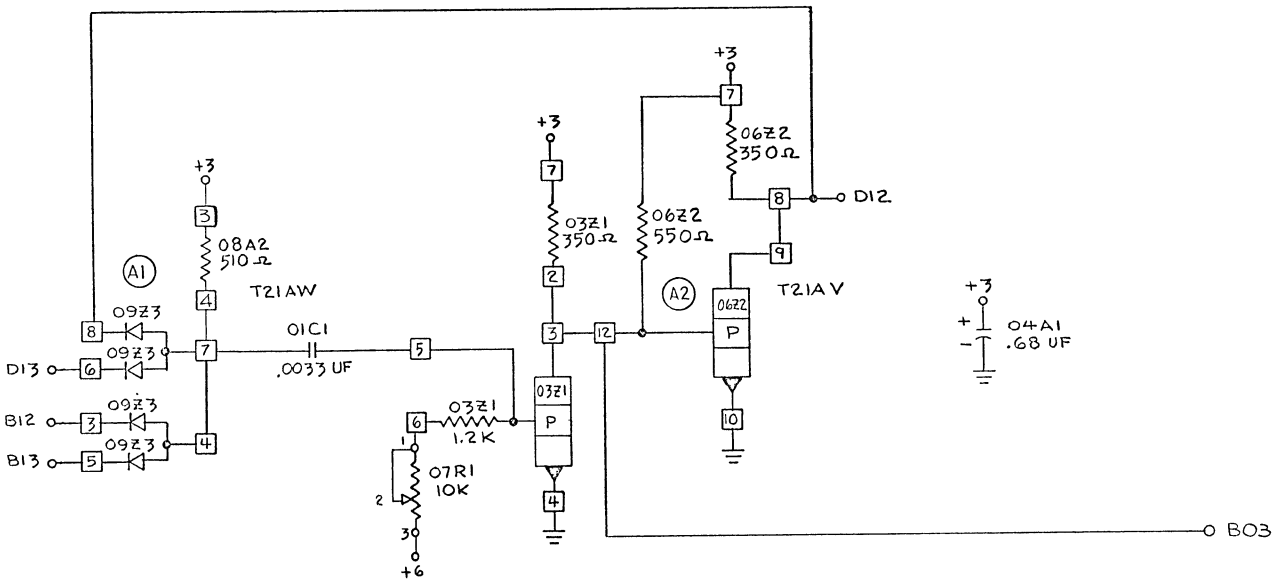
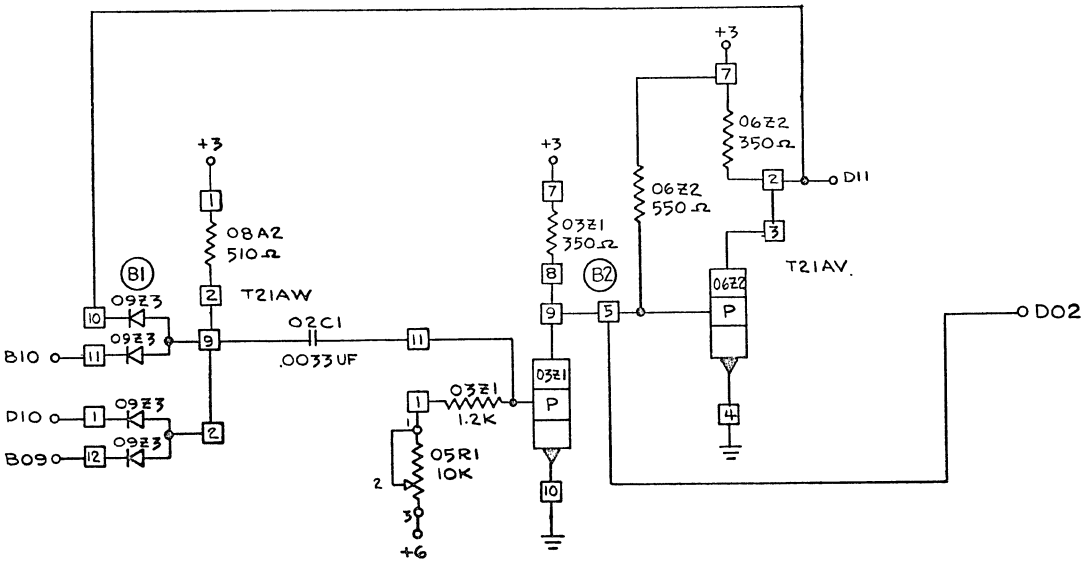
LMH Cat.	0-2860 Subject	334 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-VARIABLE SSA (1.45 TO 12.0U SEC)

P/N	5803341
EC	167467





SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
SS 53U SEC. TO 170M SEC.

LMH Cat.	0-2860 Subject	335 Suffix

IBM

Location

Manufacturing Specification

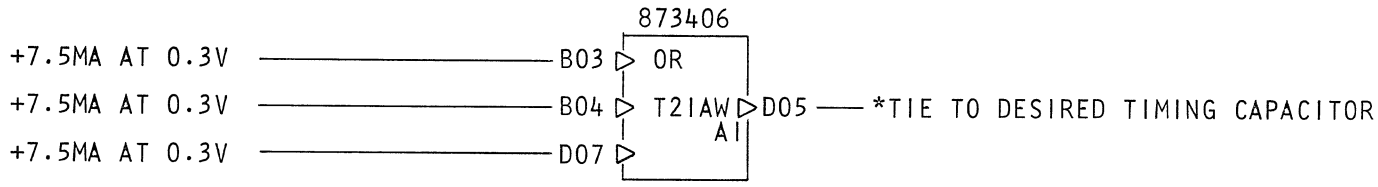
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
D08	GND

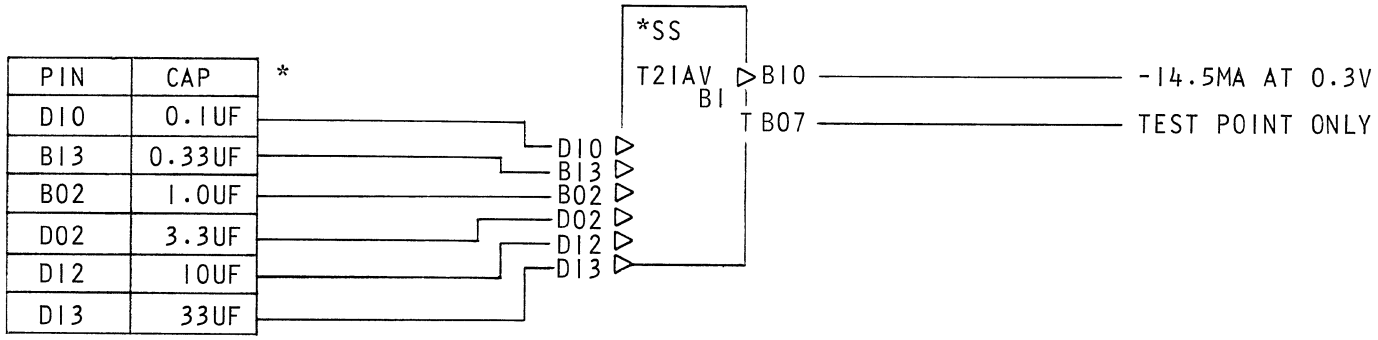
SS 53U SEC. TO 170M SEC

CATEGORY CODE

T21

P/N	5803345	
EC	164572	
STANDARD RESTRICTED		
CARD SIZE		1-12





PIN	CAP
D10	0.1UF
B13	0.33UF
B02	1.0UF
D02	3.3UF
D12	10UF
D13	33UF

*

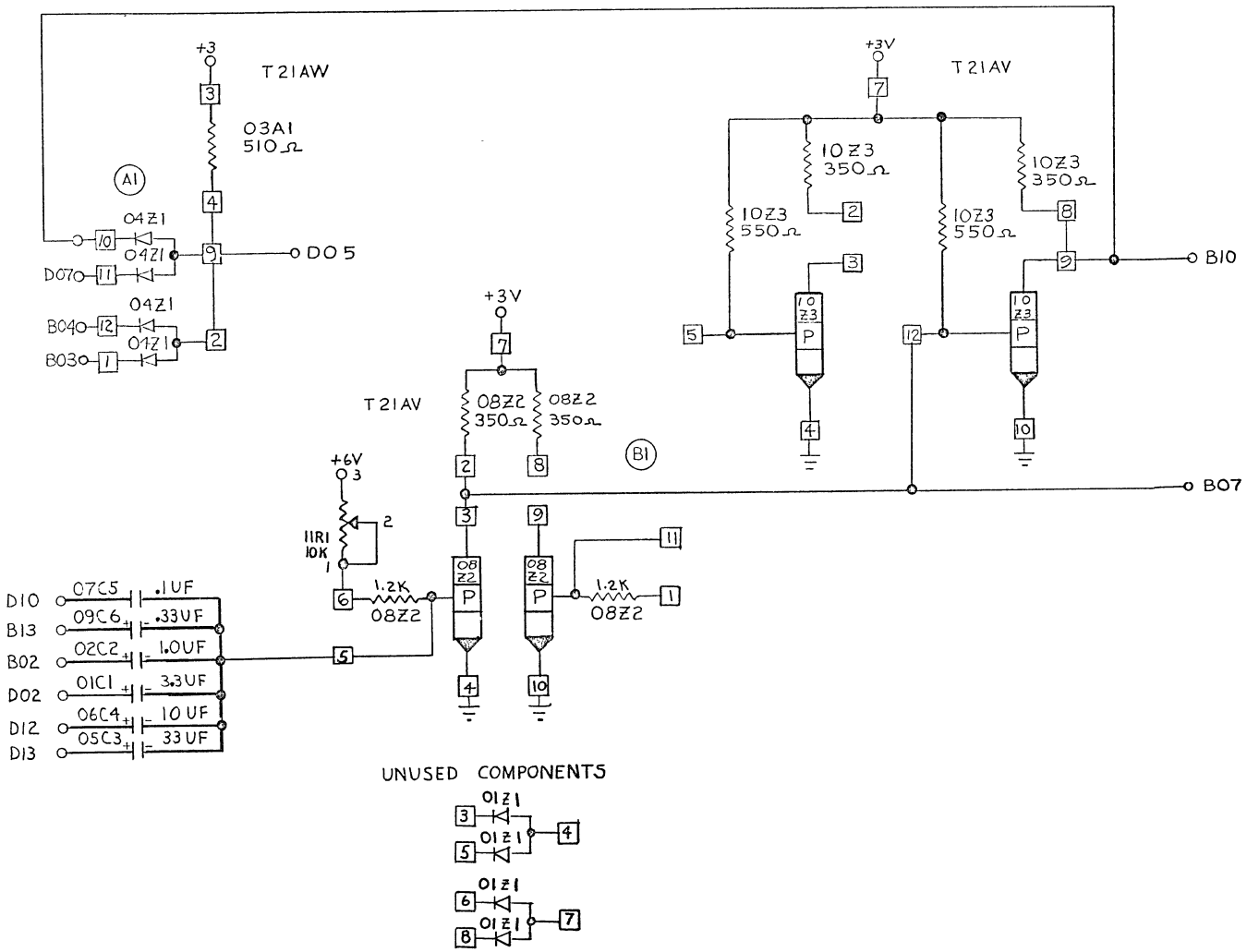
TABLE OF OUTPUT WIDTH AND RECOVERY TIMES

CAP	T_{MAX}	T_{MIN}	$T_{R\ MIN}$
0.1UF	370US	45US	190US
0.33UF	1.2MS	150US	650US
1.0UF	3.8MS	470US	2.0MS
3.3UF	11.4MS	1.55MS	6.6MS
10UF	36MS	4.6MS	20MS
33UF	115MS	15.5MS	67MS

LMH Cat.	0-2860 Subject	335 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
SS 53U SEC. TO 170M SEC.

P/N	5803345
EC	164572



IBM Location Manufacturing Specification

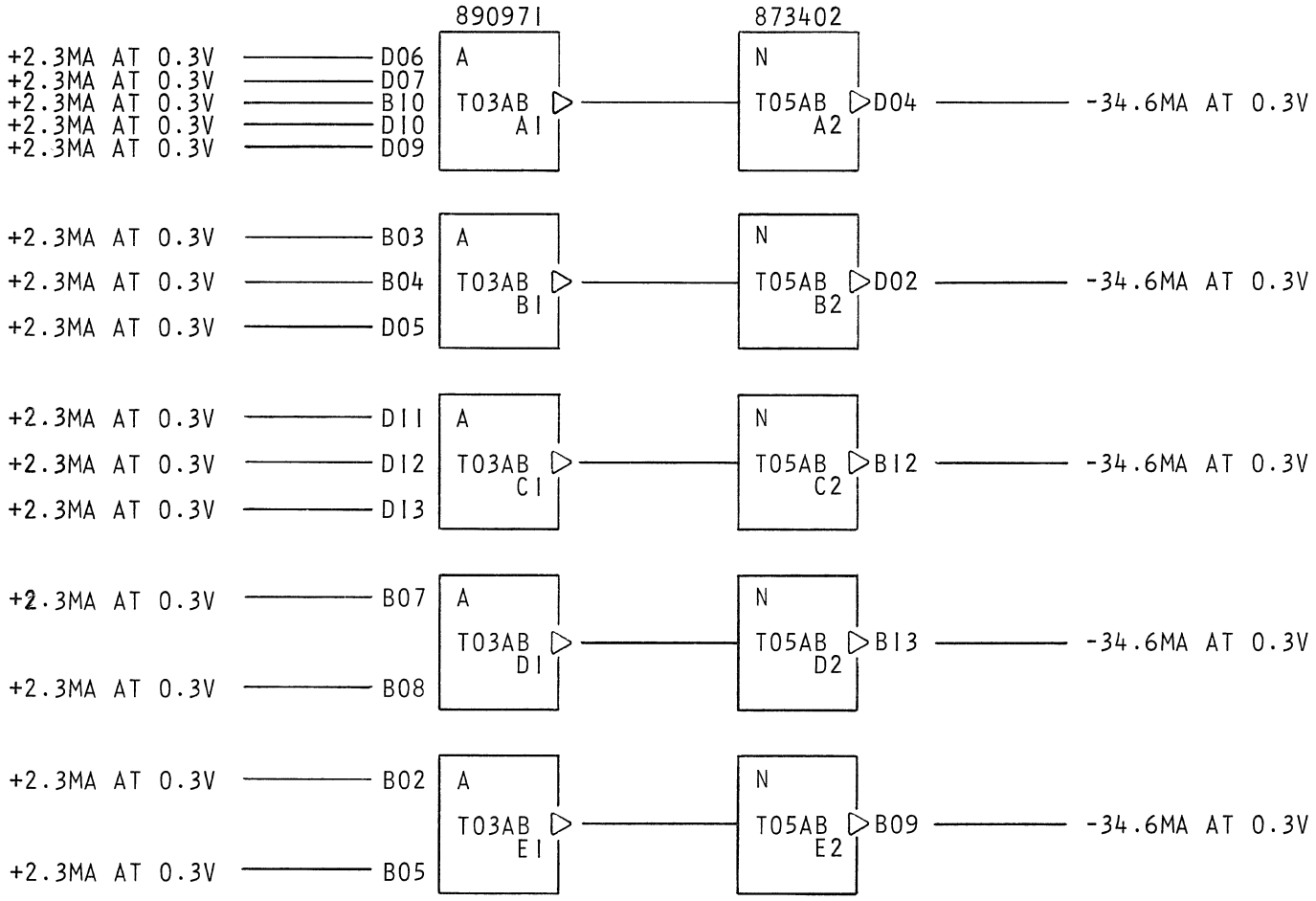
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

1-5W AI,DCI & 2-3W AI,DCI & 2-2W AI,DCI

CATEGORY CODE

T03

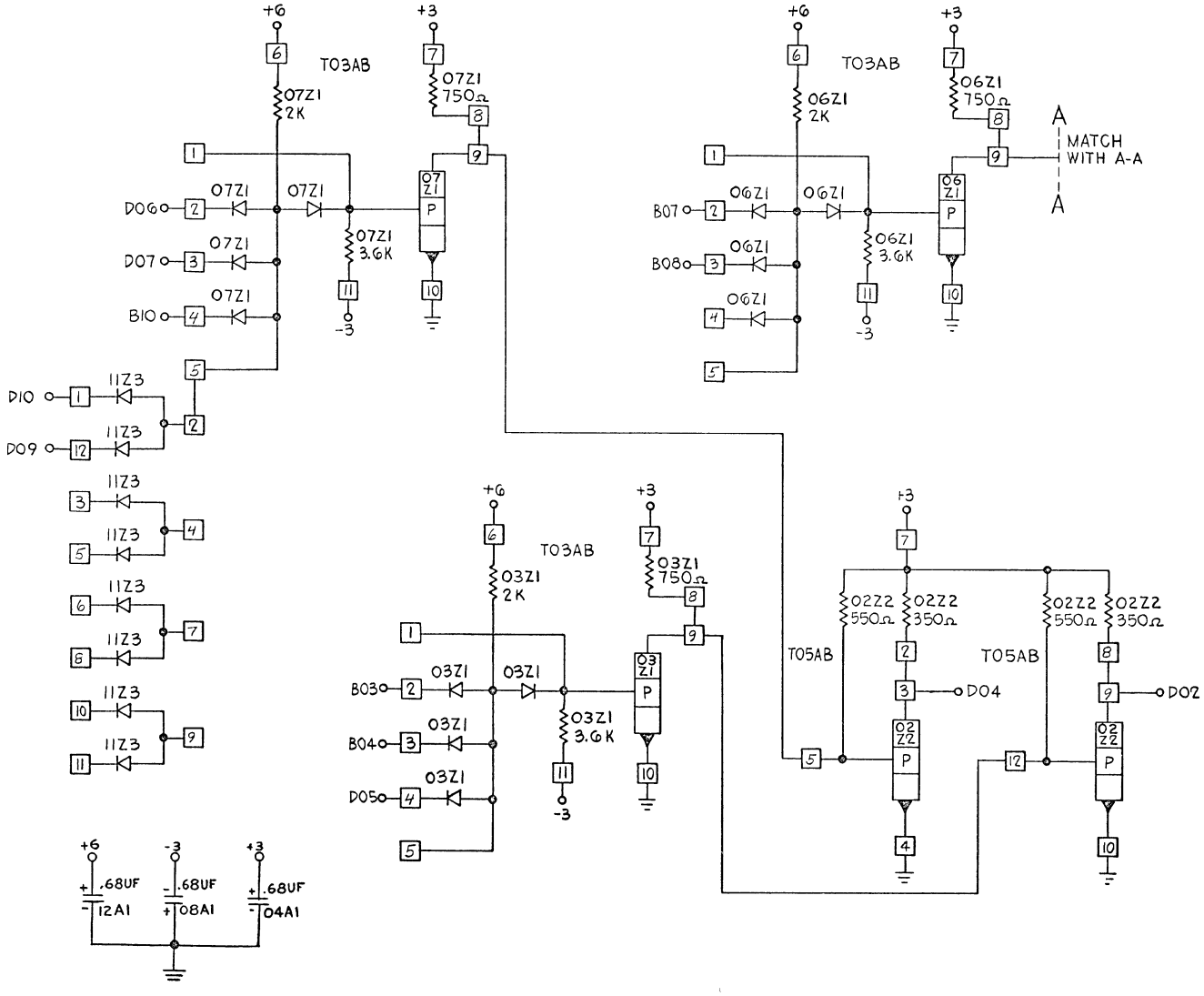
P/N	5803404
EC	162201
STANDARD RESTRICTED	
CARD SIZE	1-12



LMH Cat.	0-2860 Subject	337 Suffix

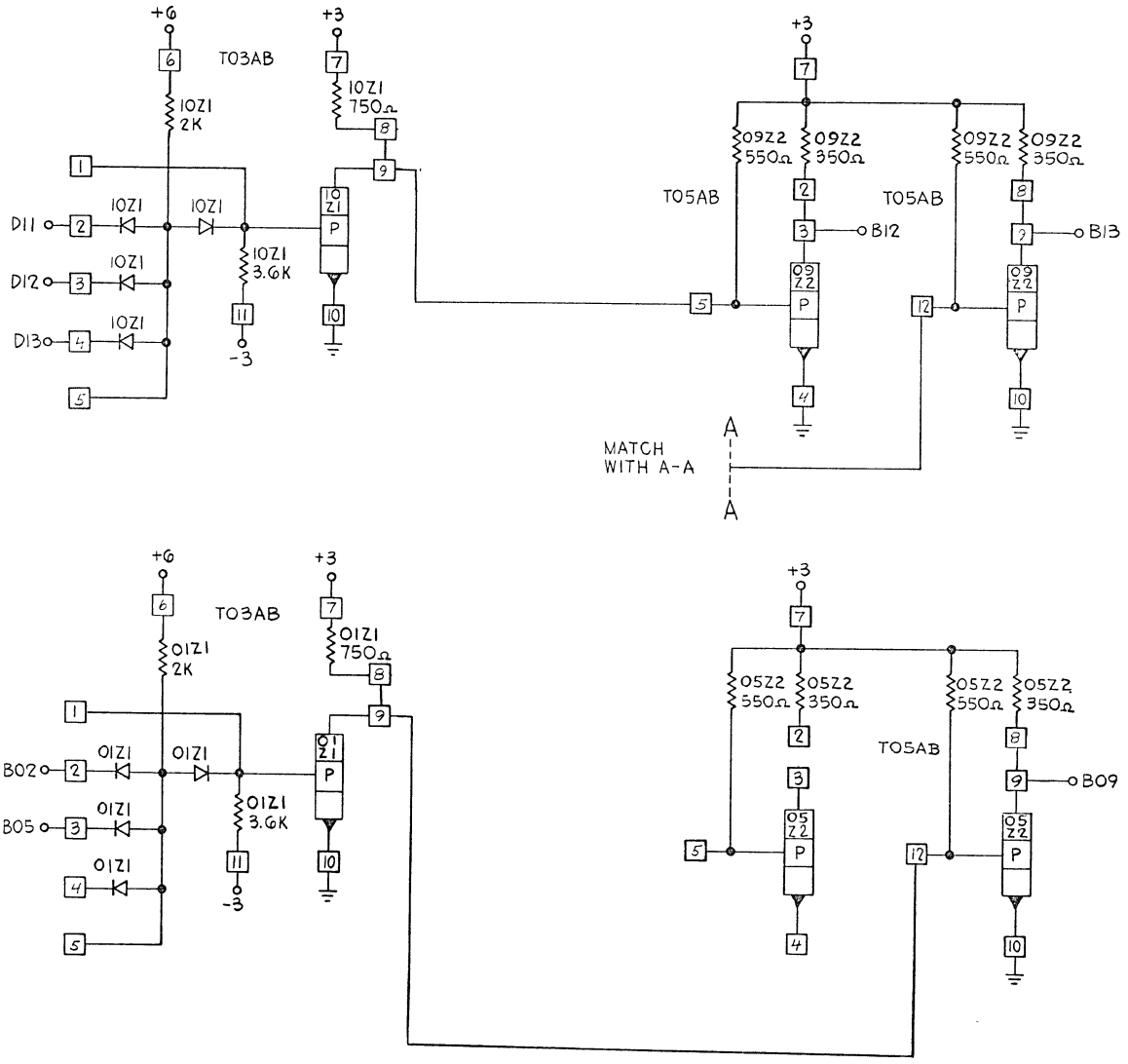
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-5W AI,DCI & 2-3W AI,DCI & 2-2W AI,DCI

P/N	5803404
EC	162201



2 OF 3 Page	1-67 Date	

P/N	5803404
EC	162201



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4 SINGLE LEG INPUT LATCHES, I-IW API

LMH	0-2860	338
Cat.	Subject	Suffix

IBM **Location Manufacturing Specification**

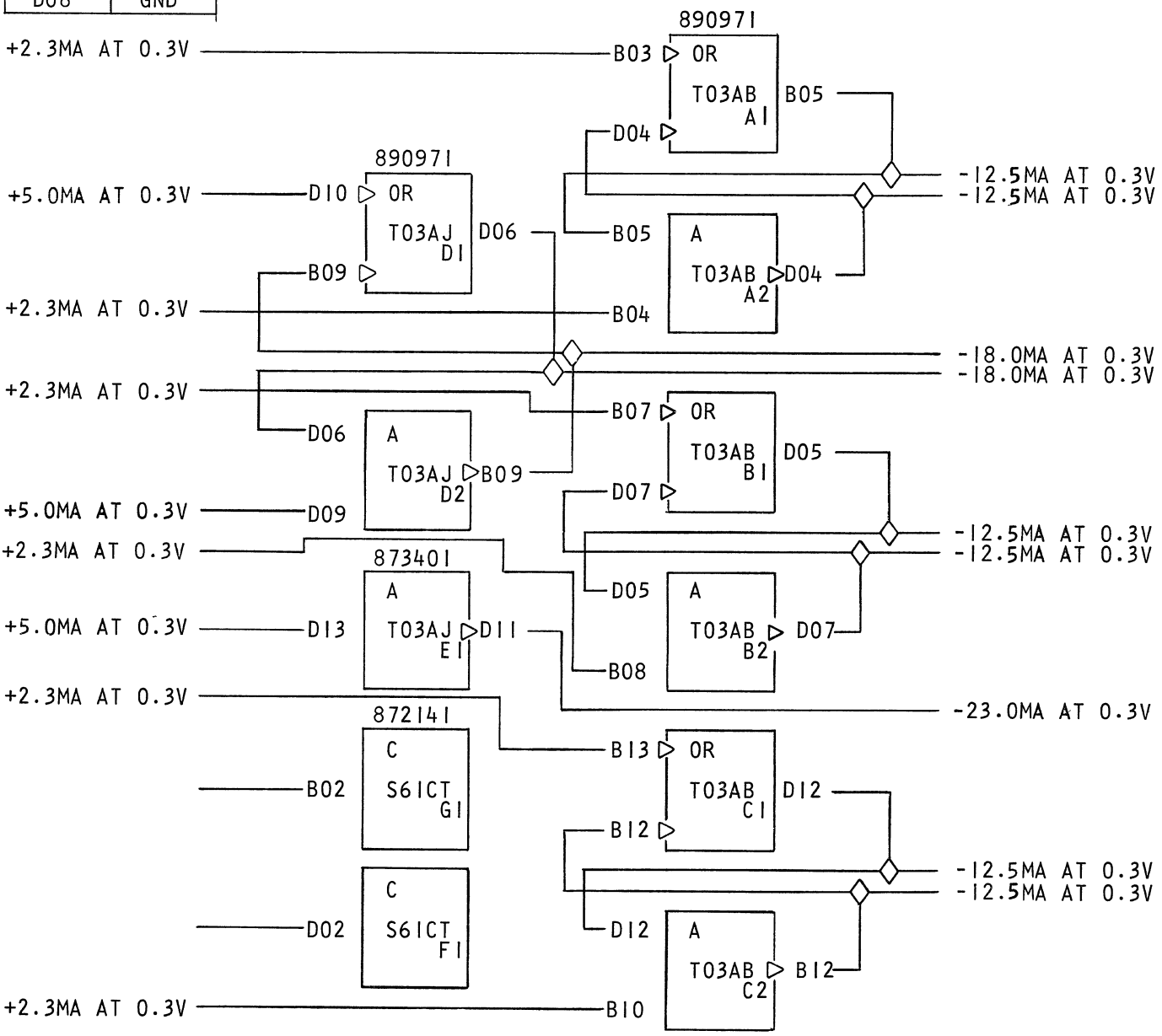
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

4 SINGLE LEG INPUT LATCHES, I-IW API

CATEGORY CODE

T03

P/N	5803405
EC	162204
STANDARD RESTRICTED	
CARD SIZE	I-12



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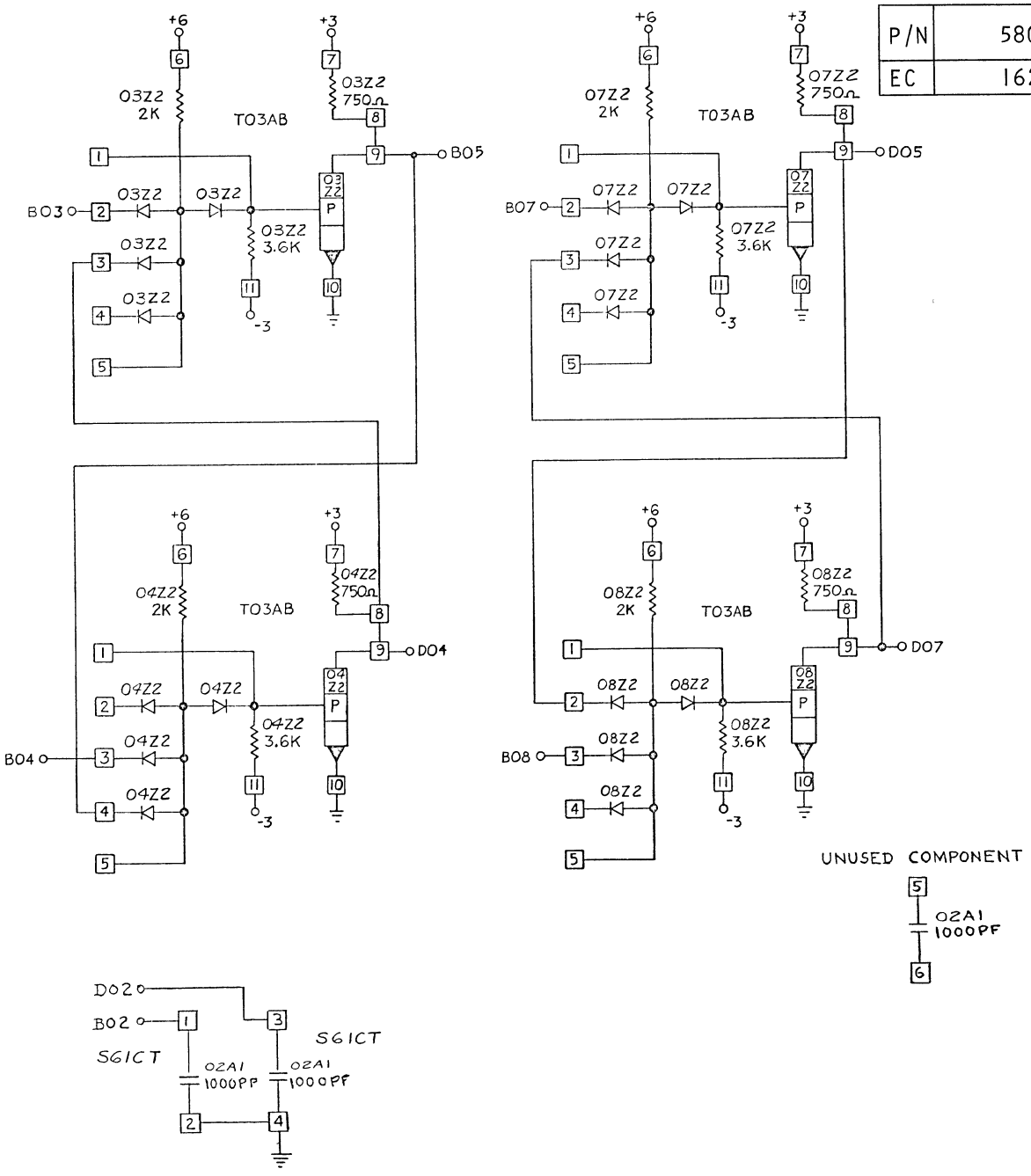
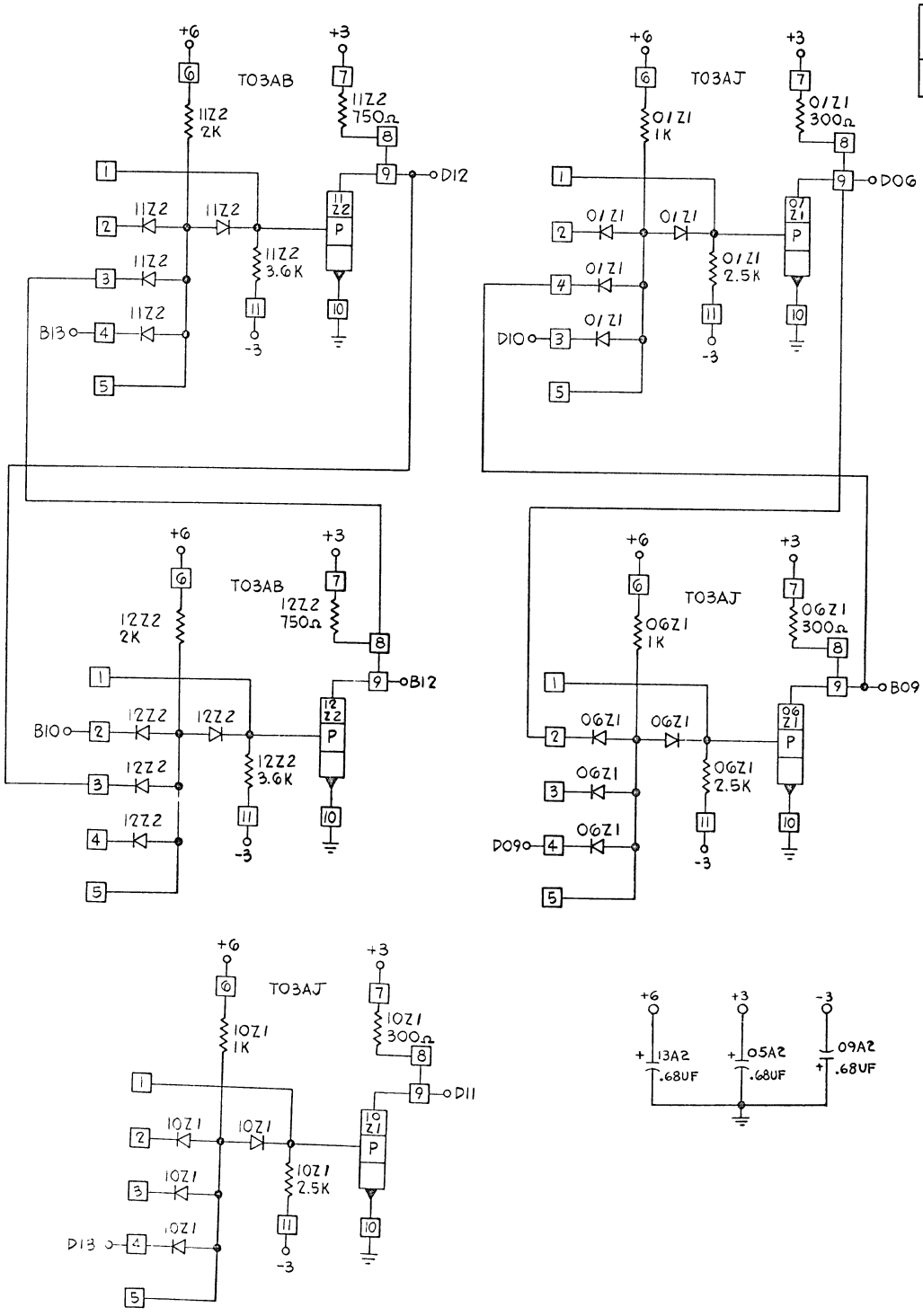
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4 SINGLE LEG INPUT LATCHES, I-IW API

P/N	5803405
EC	162204



P/N	5803405
EC	162204



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
3-3W HPD DRIVING API

LMH	O-2860	339
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

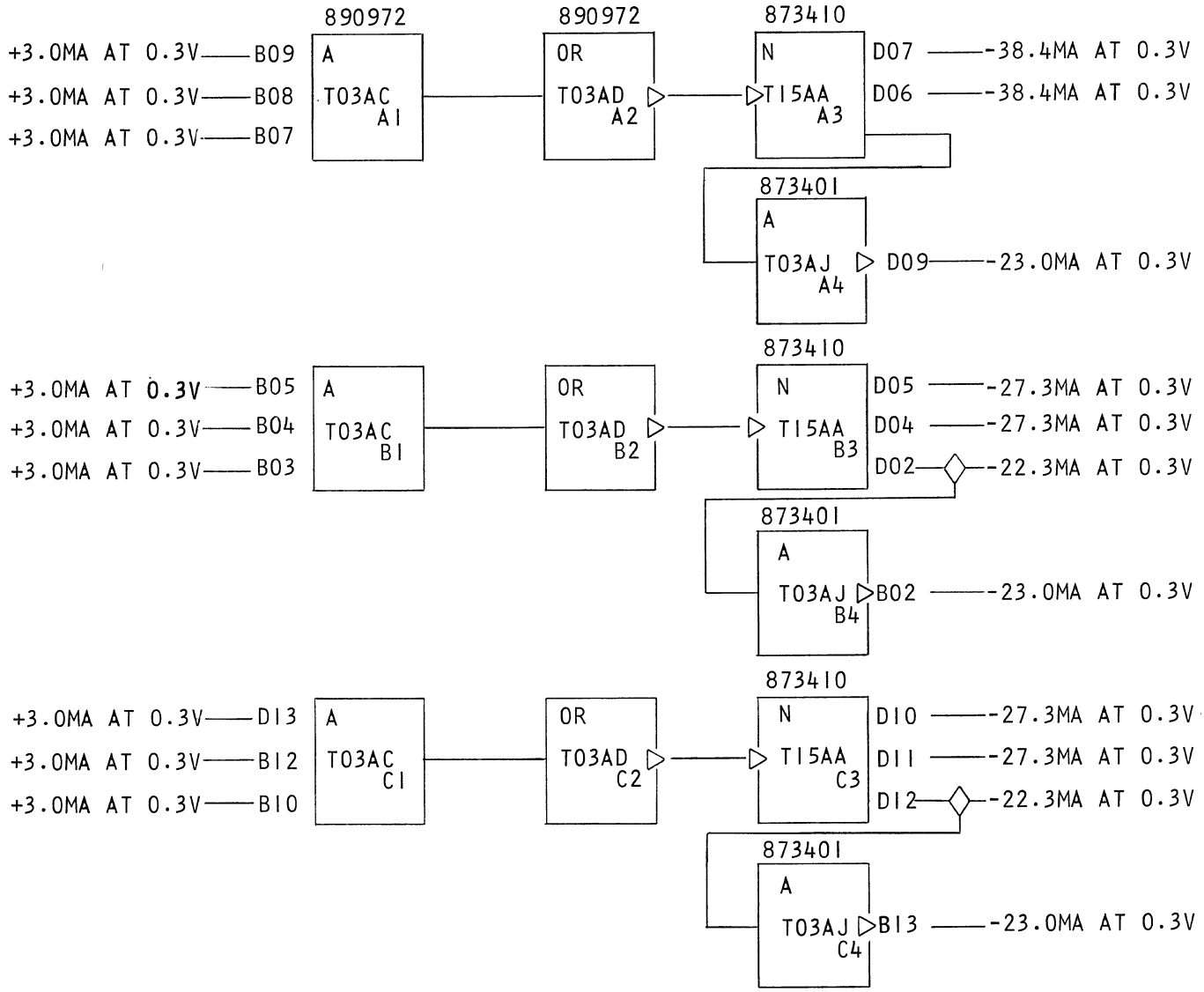
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

3-3W HPD DRIVING API

CATEGORY CODE

T03	T15

P/N	5803406
EC	164272
STANDARD RESTRICTED	
CARD SIZE	1-12



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Primary Standards Manual	Other standards manuals in which this document may be filed.			
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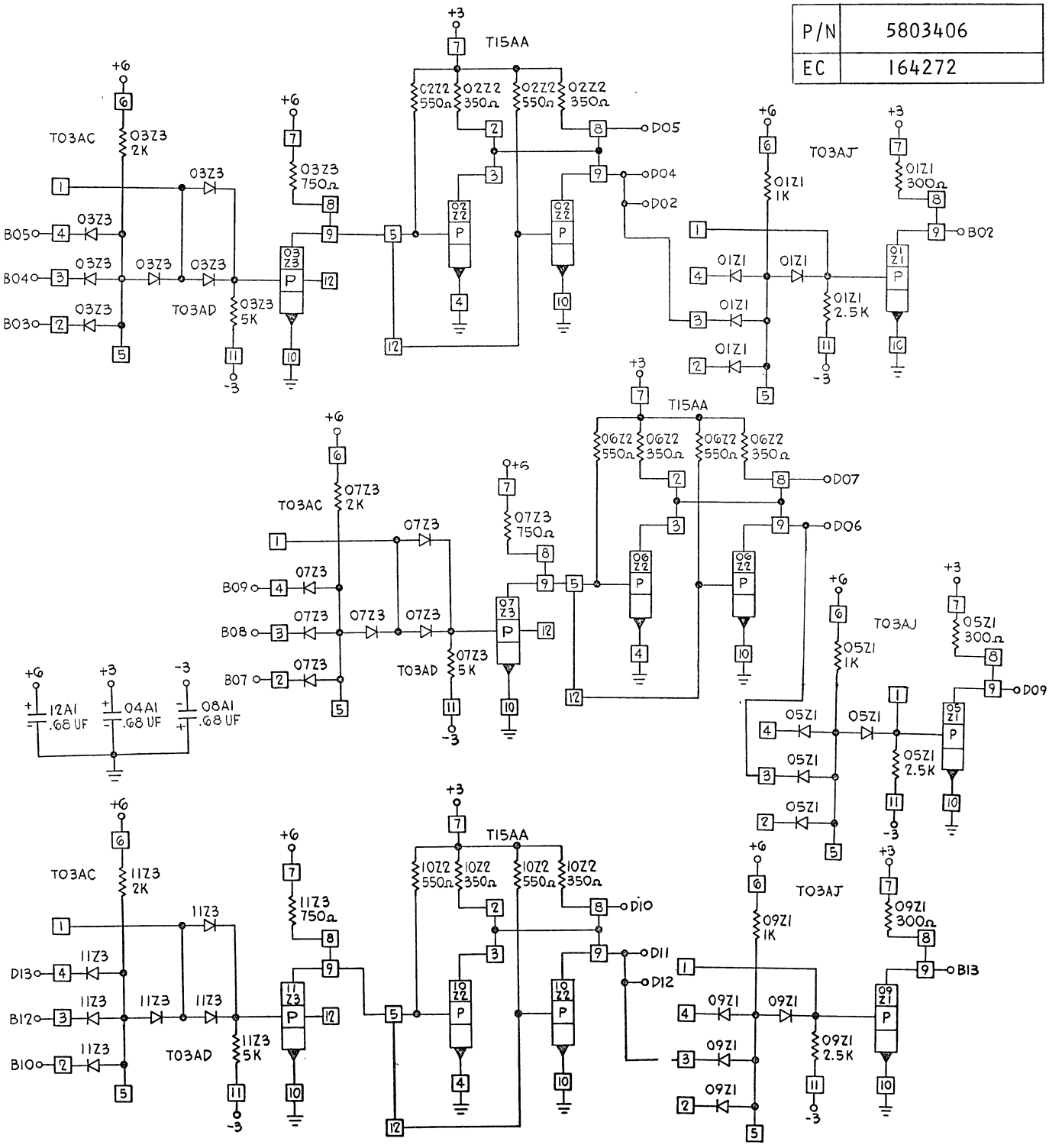
LMH Cat.	0-2860 Subject	339 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 3-3W HPD DRIVING API

P/N	5803406
EC	164272



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
8-3W A DCI (DOUBLEGATED)

LMH	0-2860	341
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

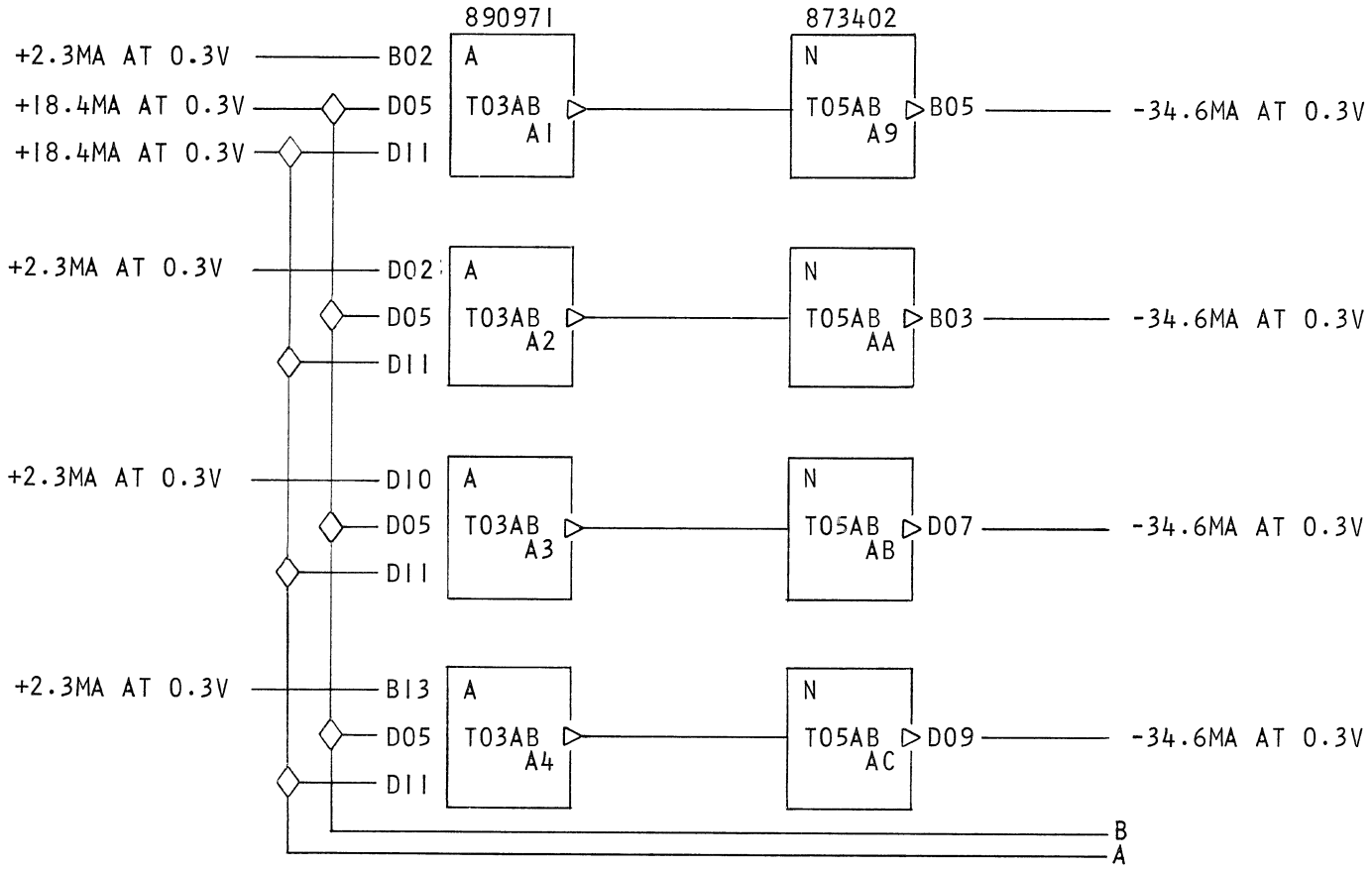
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

8-3W A DCI (DOUBLEGATED)

CATEGORY CODE

T03

P/N	5803411
EC	162029
STANDARD RESTRICTED	
CARD SIZE	1-12



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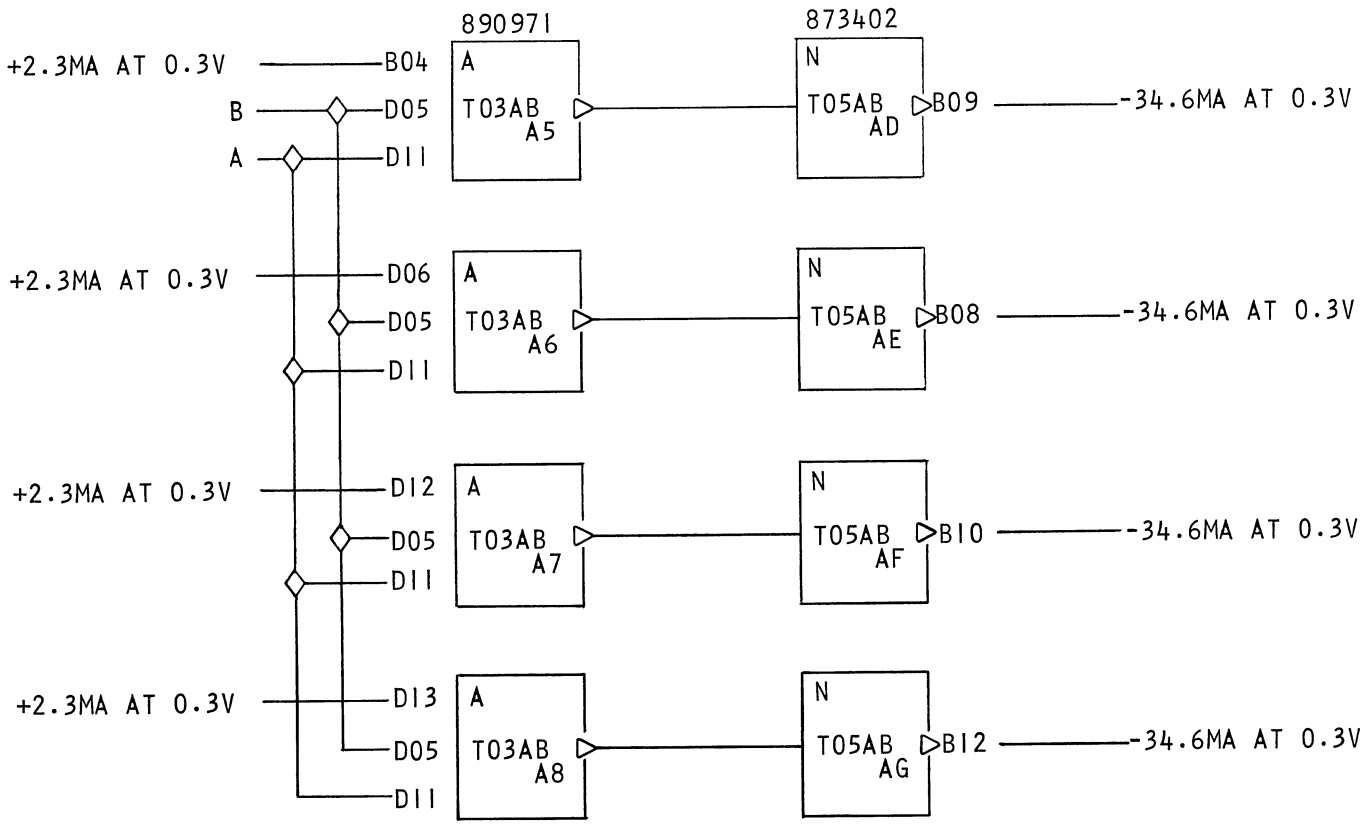
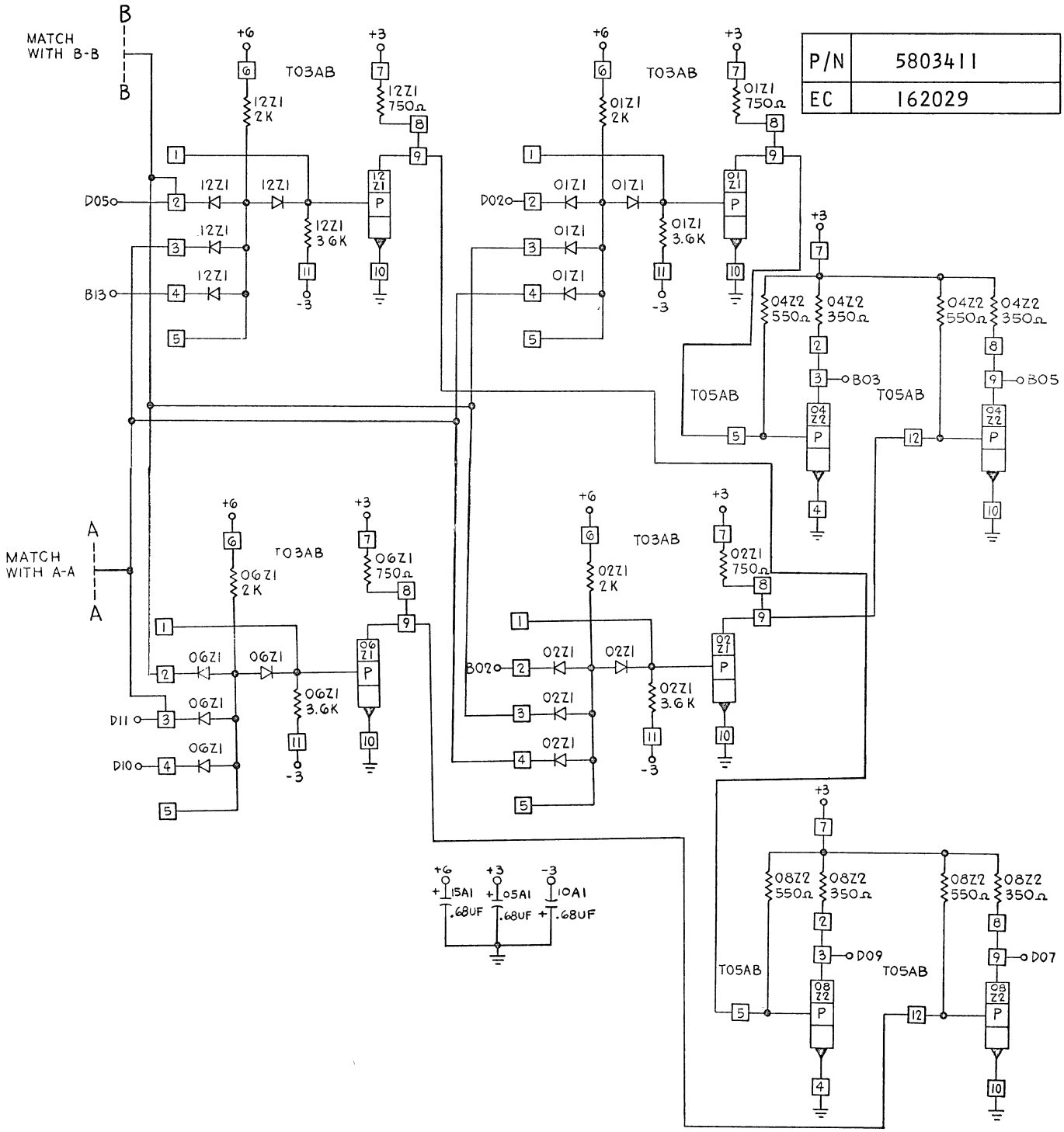
8-3W A DCI (DOUBLEGATED

P/N	5803411
EC	162029



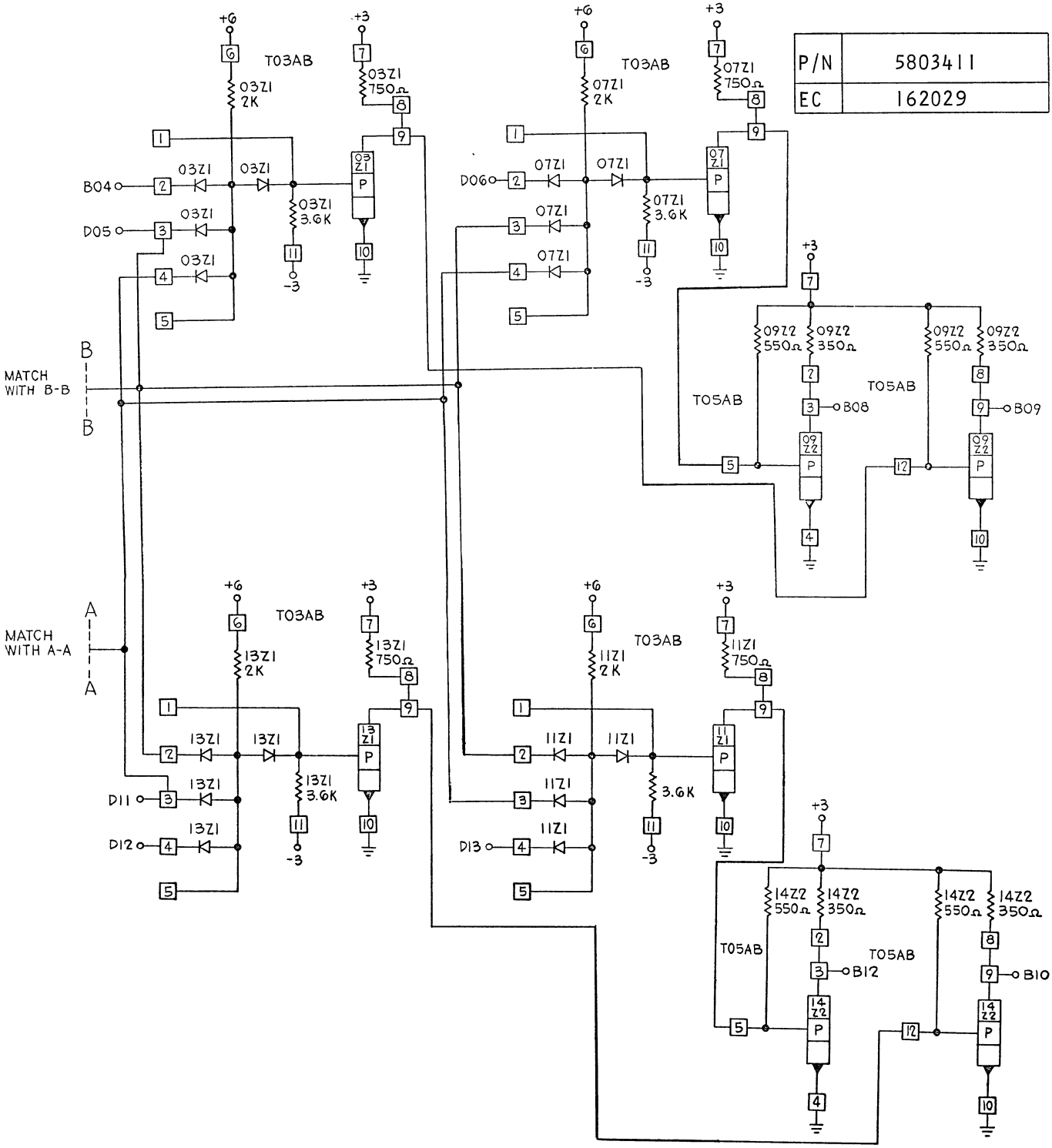
P/N	5803411
EC	162029



LMH Cat.	0-2860 Subject	341 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
8-3W A DCI (DOUBLEGATED)

P/N	5803411
EC	162029



Page	Date
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POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

10-1W AI

CATEGORY CODE

T03

P/N	5803421
EC	162215
STANDARD RESTRICTED	
CARD SIZE	1-12

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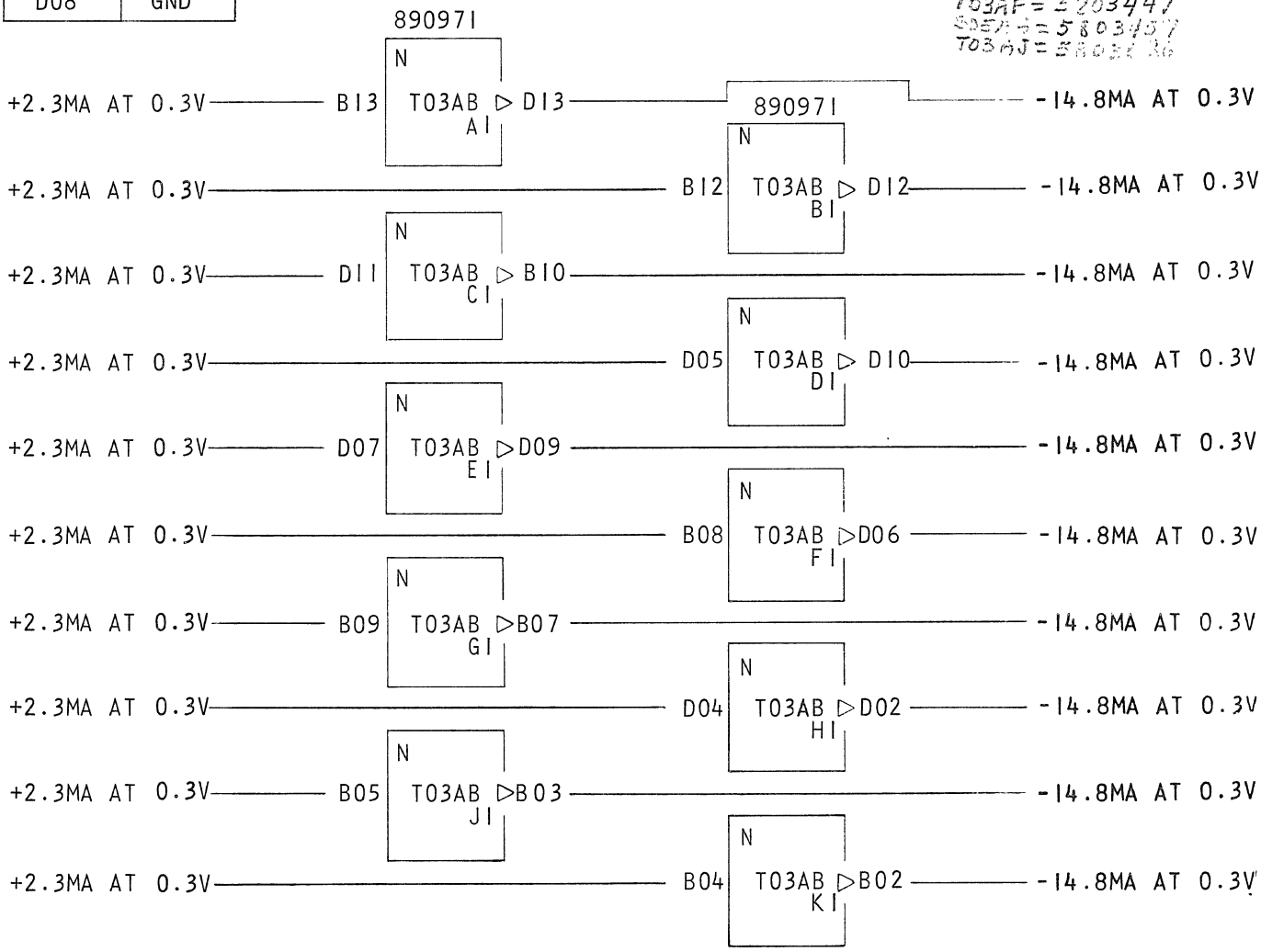
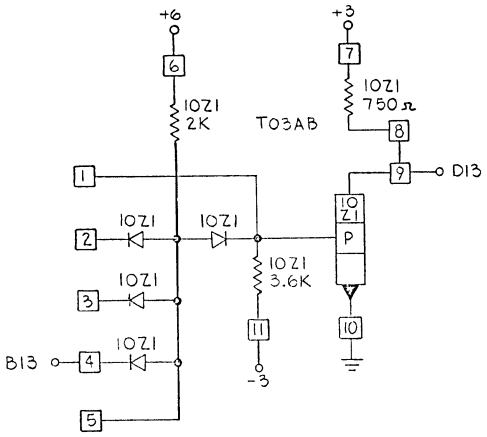
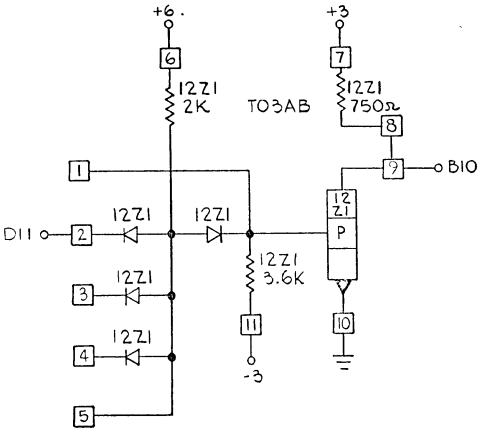
T03AF=5803447
S05AJ=5803457
T03AJ=5803516

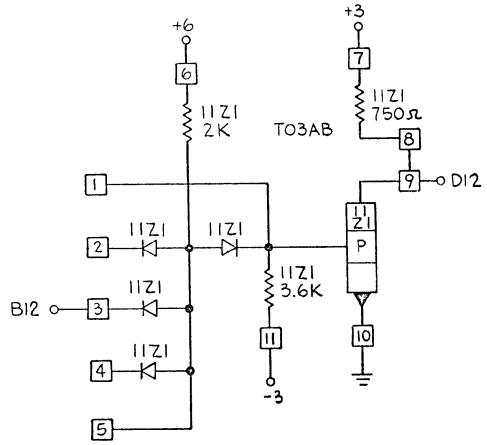


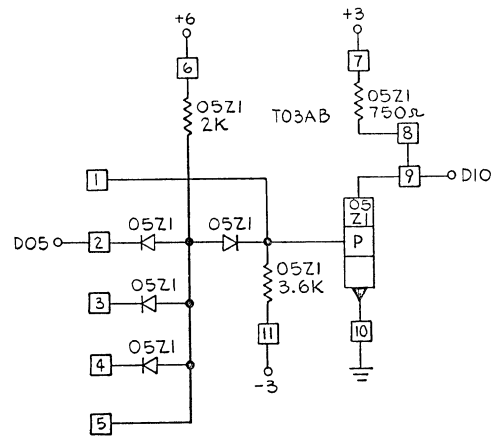
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
10-1W AI

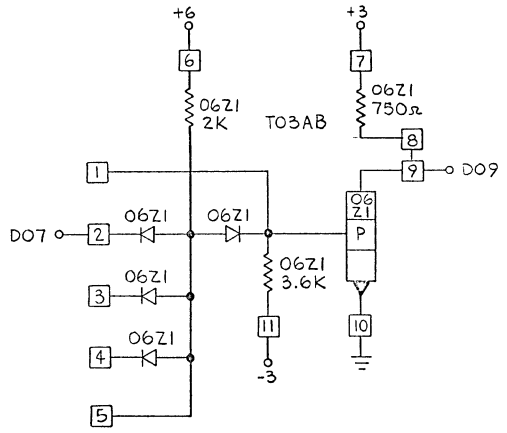
P/N	5803421
EC	162215



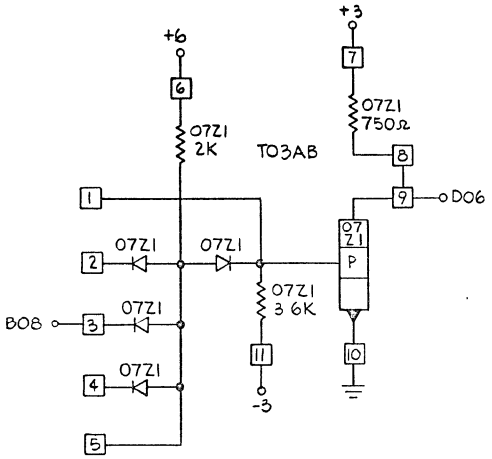


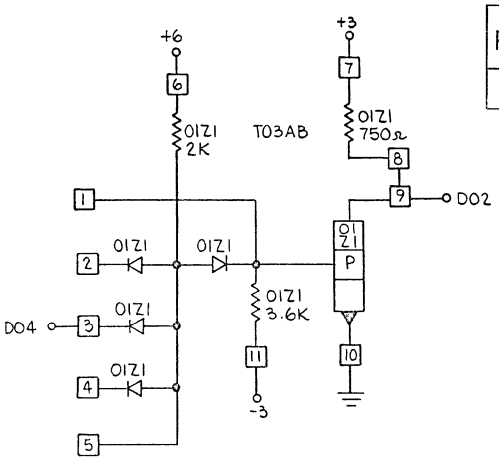


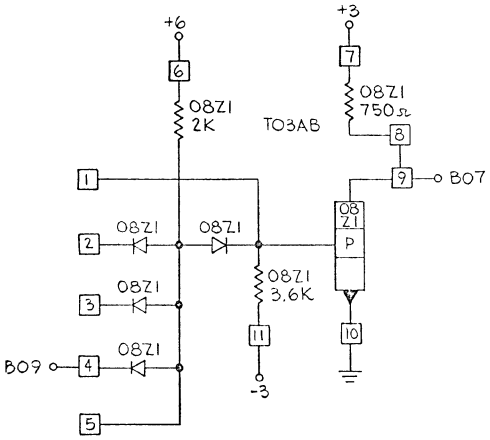


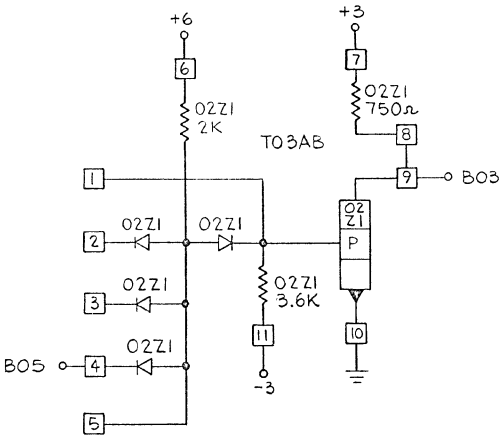


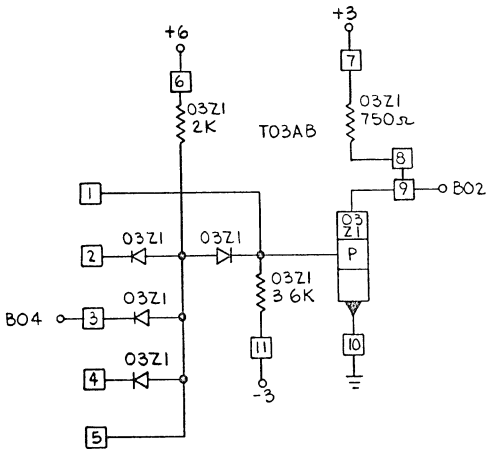
P/N	5803421
EC	162215

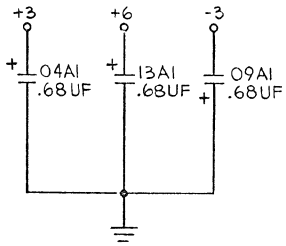












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POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

10-1W API-WO/L

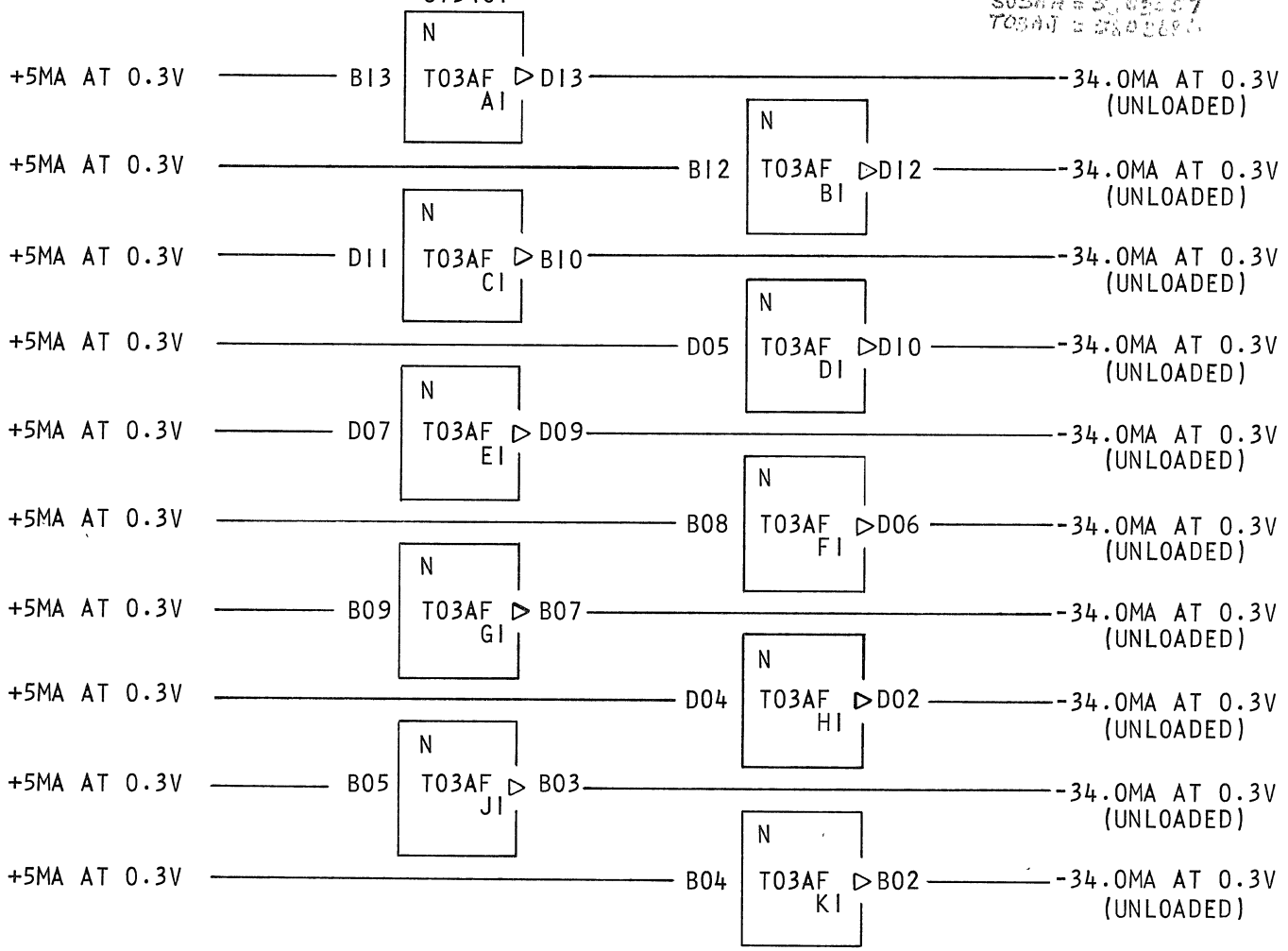
CATEGORY CODE

T03

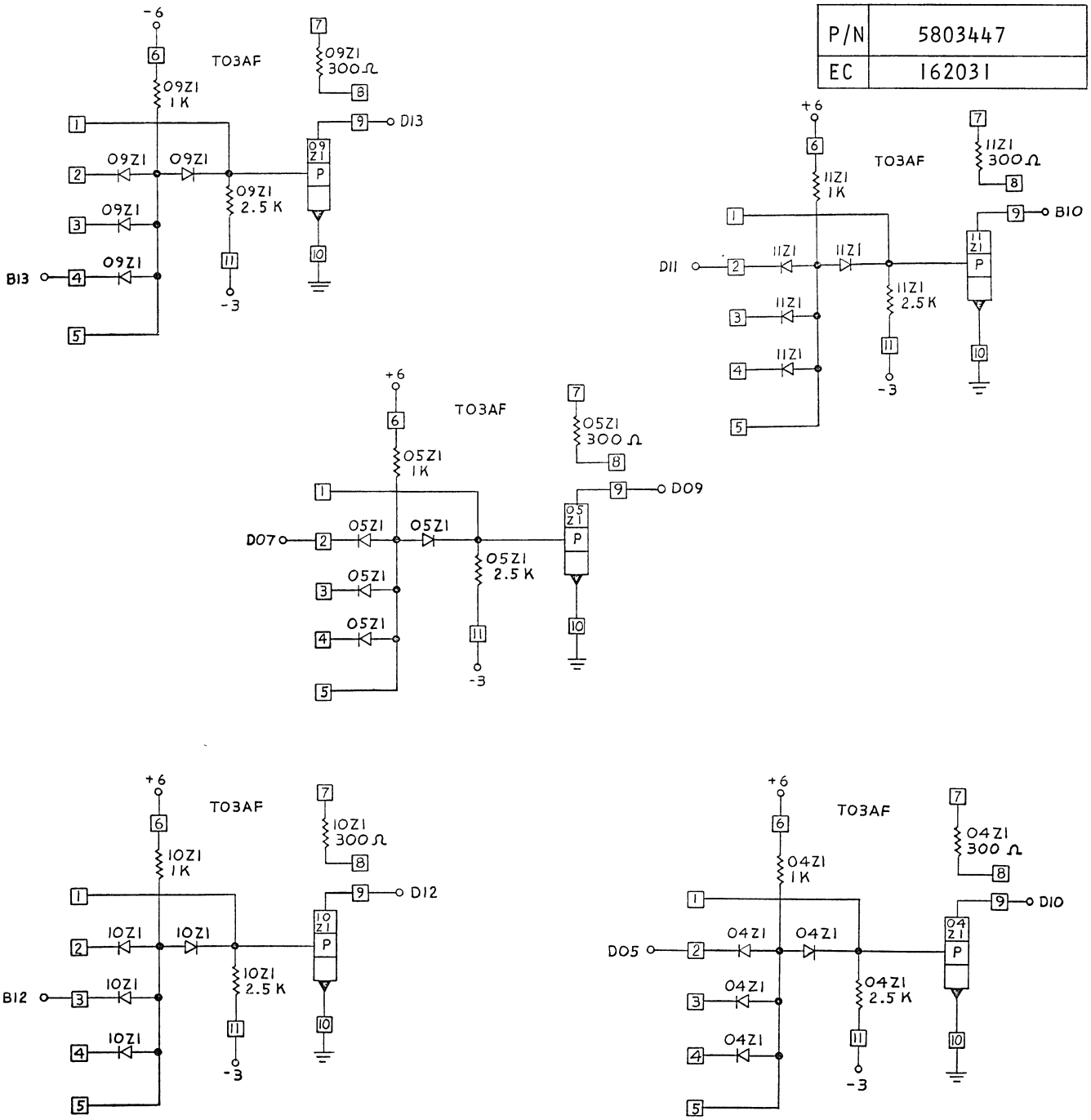
P/N	5803447	
EC	162031	
STANDARD RESTRICTED		
CARD SIZE		1-12

T03AB = 5803431
S03AH = 5800509
S03AH = 5803457
T03AJ = 5800511

873401



P/N	5803447
EC	162031



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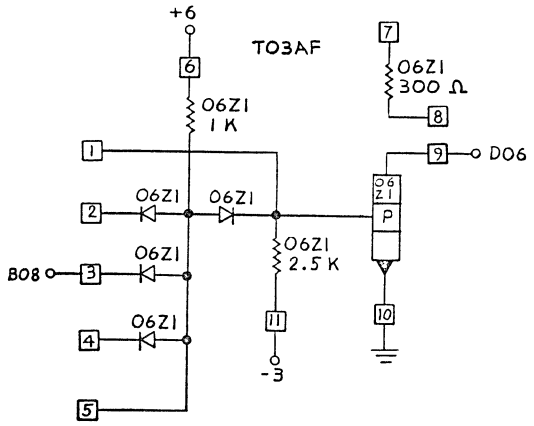
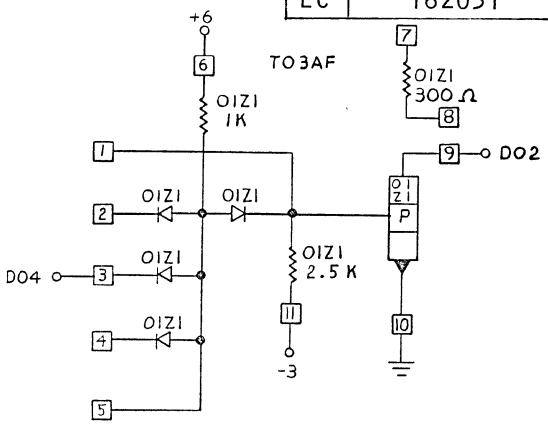
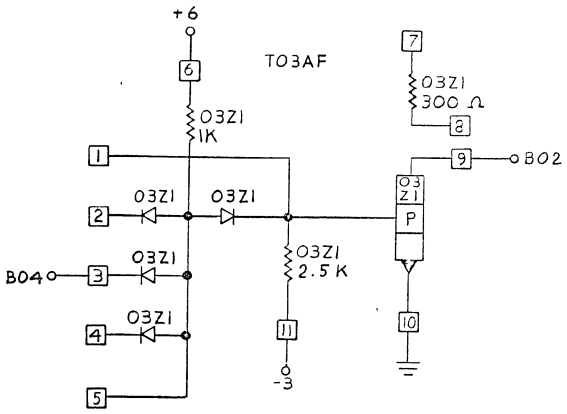
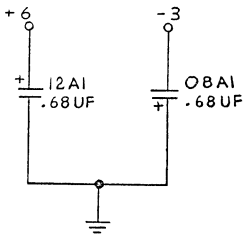
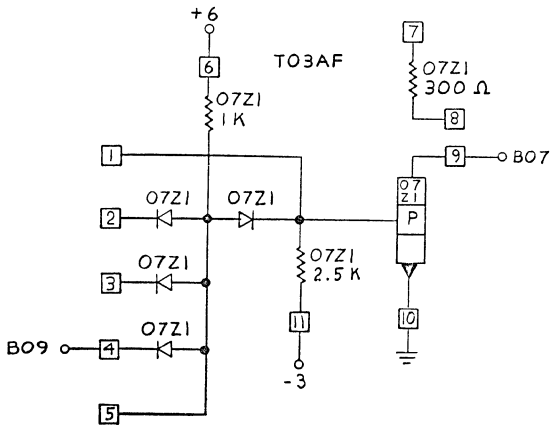
EC	162031

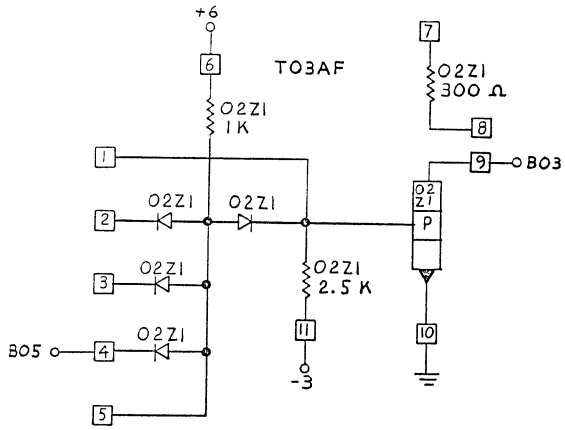












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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
IO INVERTERS

LMH	0-2860	345
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
D03	+3
D08	GND

IO INVERTERS

CATEGORY CODE

S05

P/N	5803457	
EC	160271	
SPECIAL RESTRICTED		
CARD SIZE		1-12

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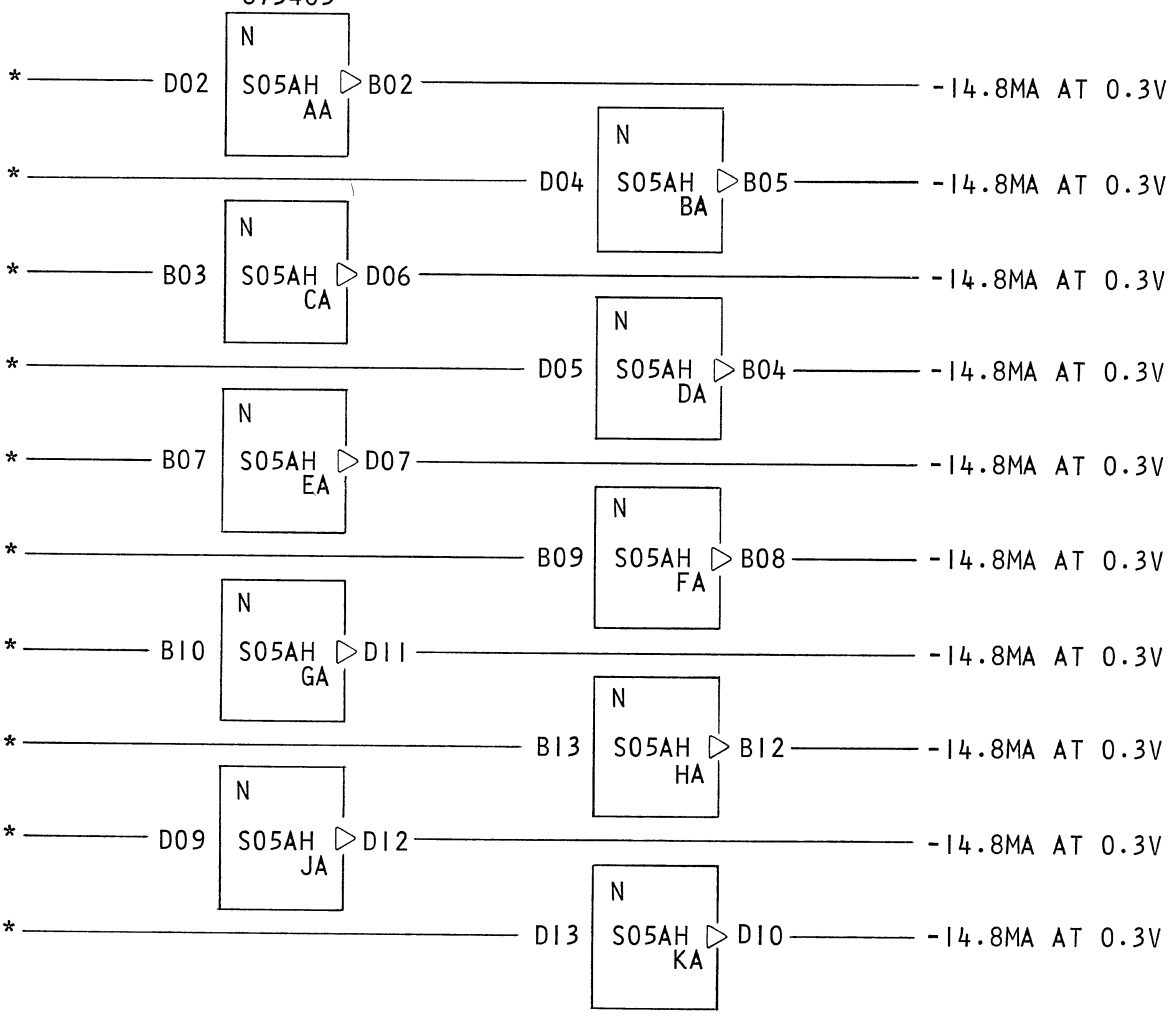
T05AB = 5803021
T05AF = 5803447
T05AJ = 5803616

873409



*SPECIAL DRIVE RULE SEE SPEC 873409

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Primary Standards Manual	Other standards manuals in which this document may be filed.			
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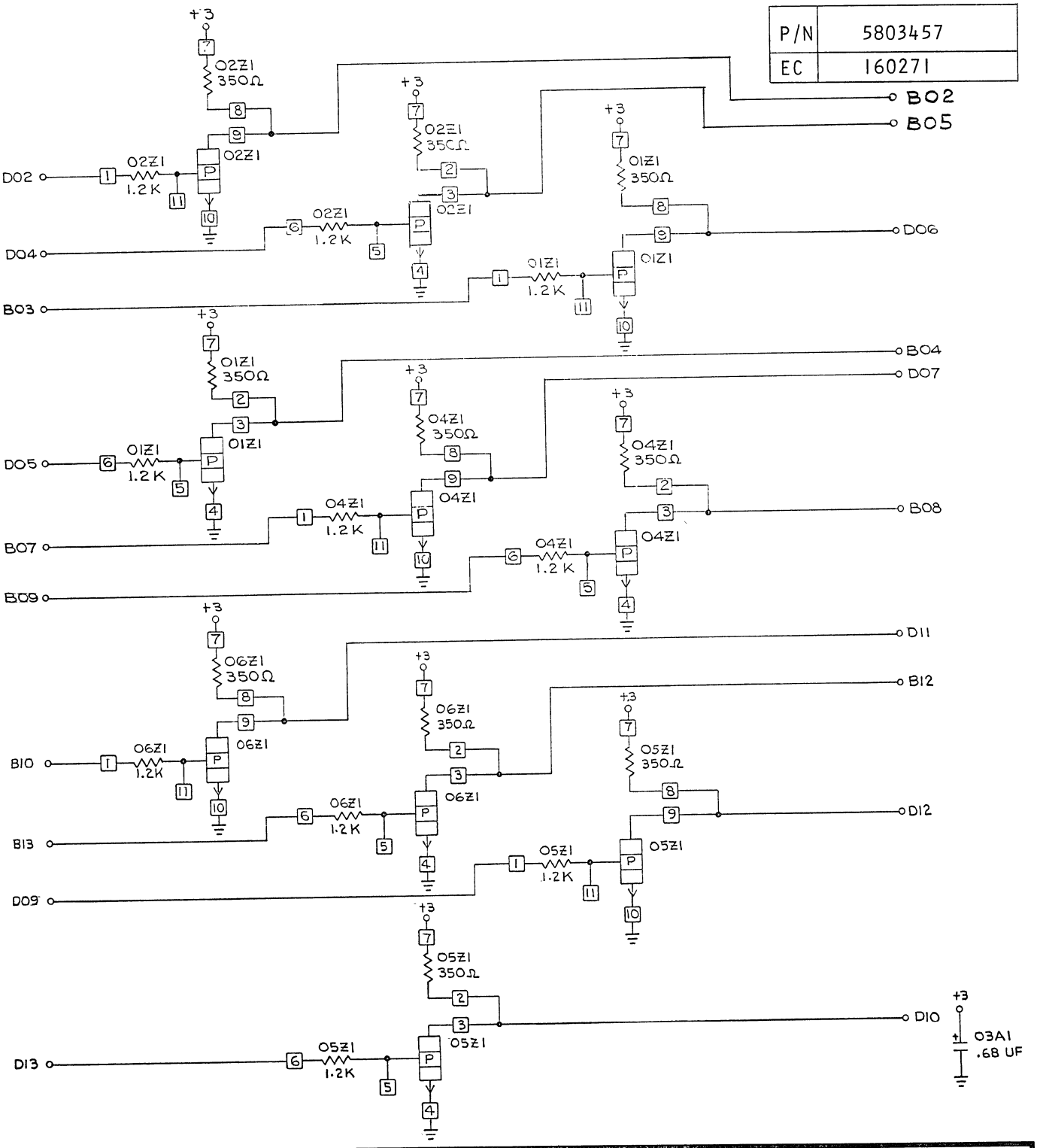
LMH Cat.	0-2860 Subject	345 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
10 INVERTERS

P/N	5803457
EC	160271



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
9 COMMON GATED 2W AI

LMH Cat.	0-2860 Subject	346 Suffix

IBM Location Manufacturing Specification

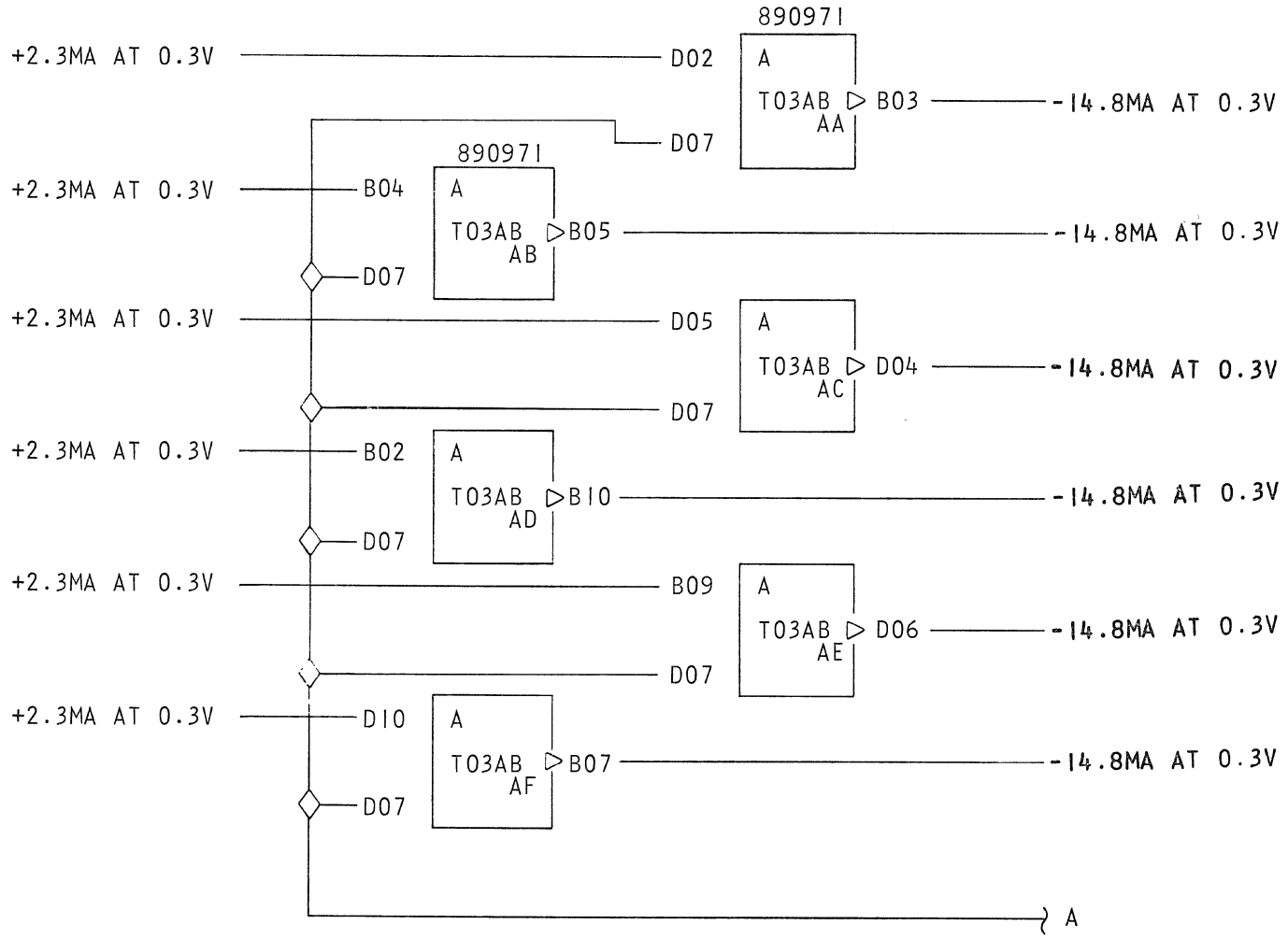
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

9 COMMON GATED 2W AI

CATEGORY CODE

T03

P/N	5803466
EC	162723
SPECIAL ACTIVE	
CARD SIZE	1-12

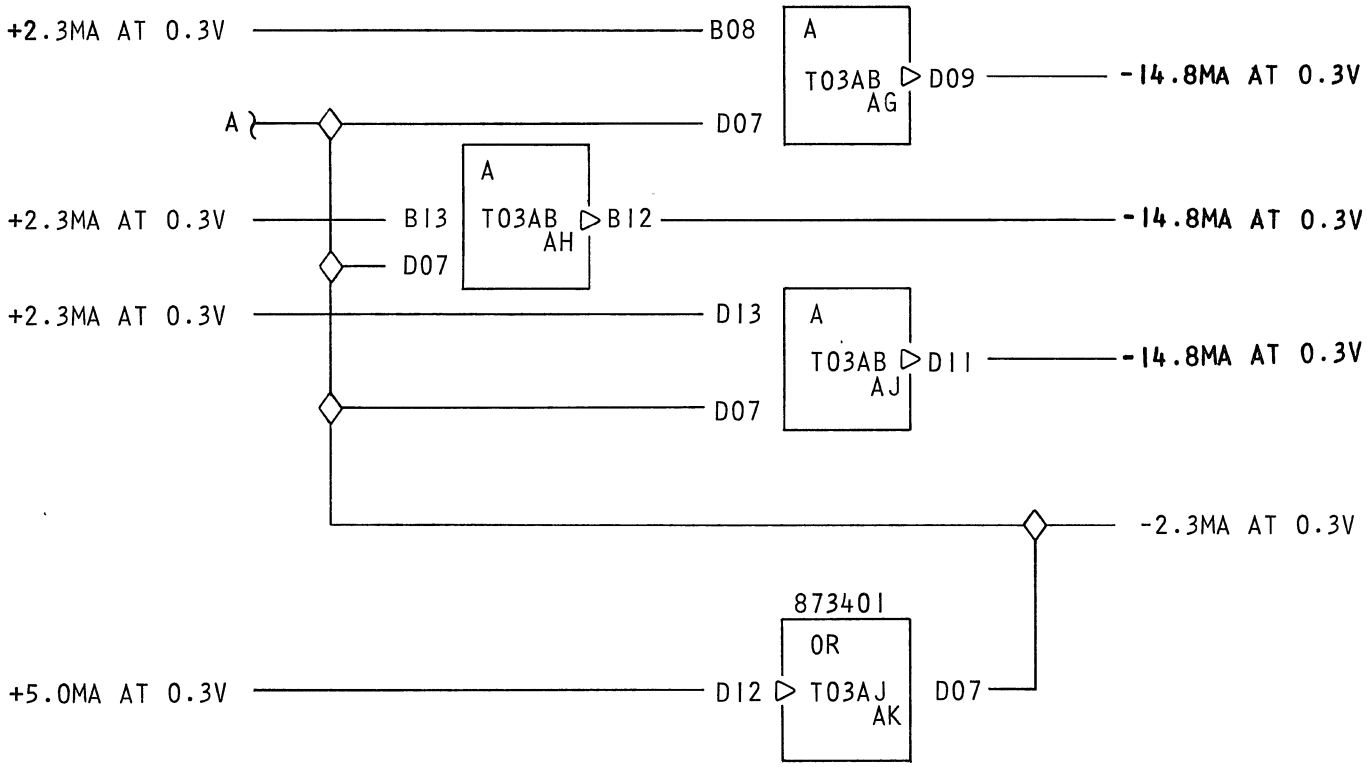


SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
9 COMMON GATED 2W AI

9 COMMON GATED 2W AI

T03

P/N	5803466
EC	162723

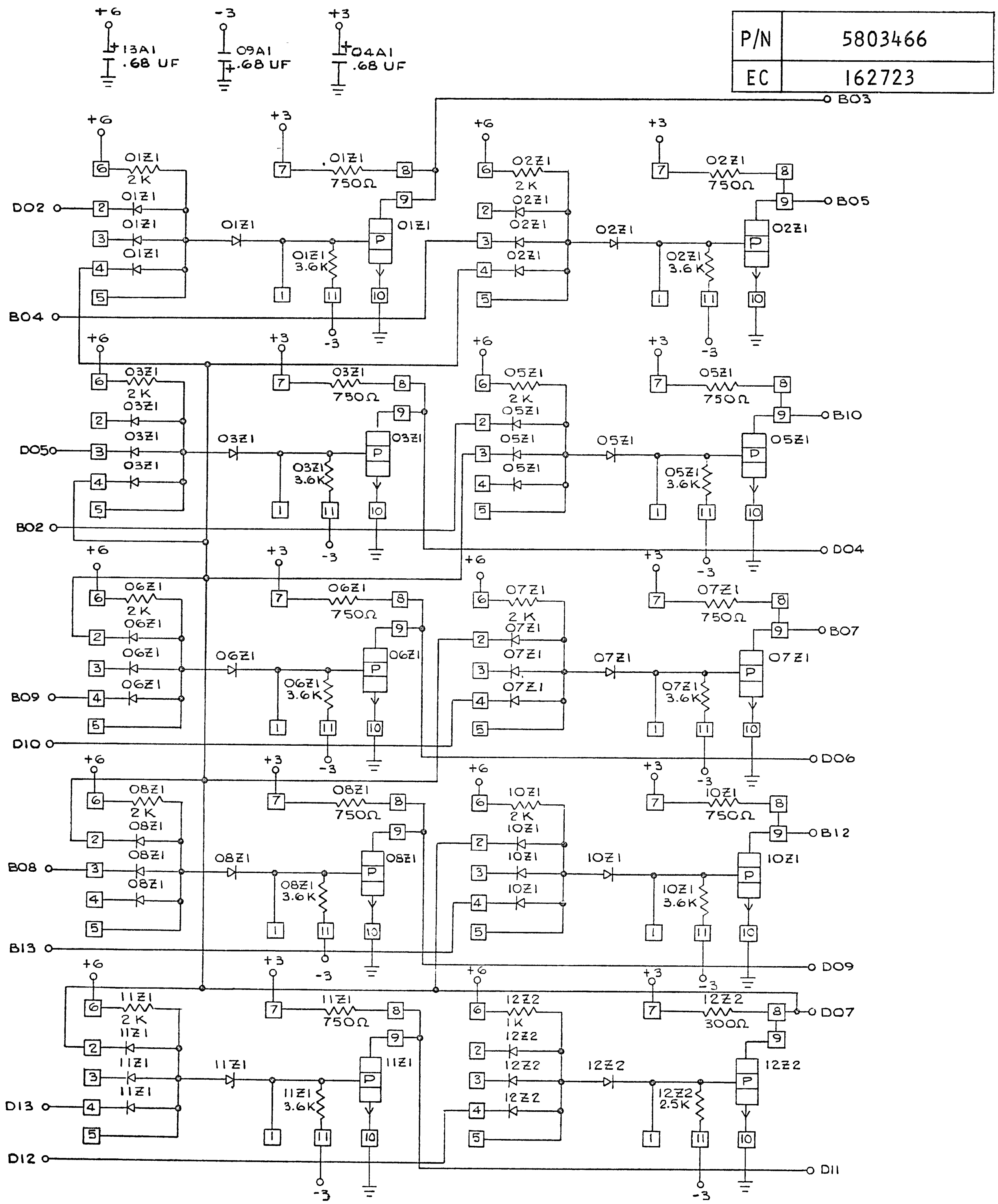


SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
9 COMMON GATED 2W AI

LMH	0-2860	346
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

P/N	5803466
EC	162723



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
LATCH CARD

LMH Cat.	0-2860 Subject	347 Suffix

IBM Location Manufacturing Specification

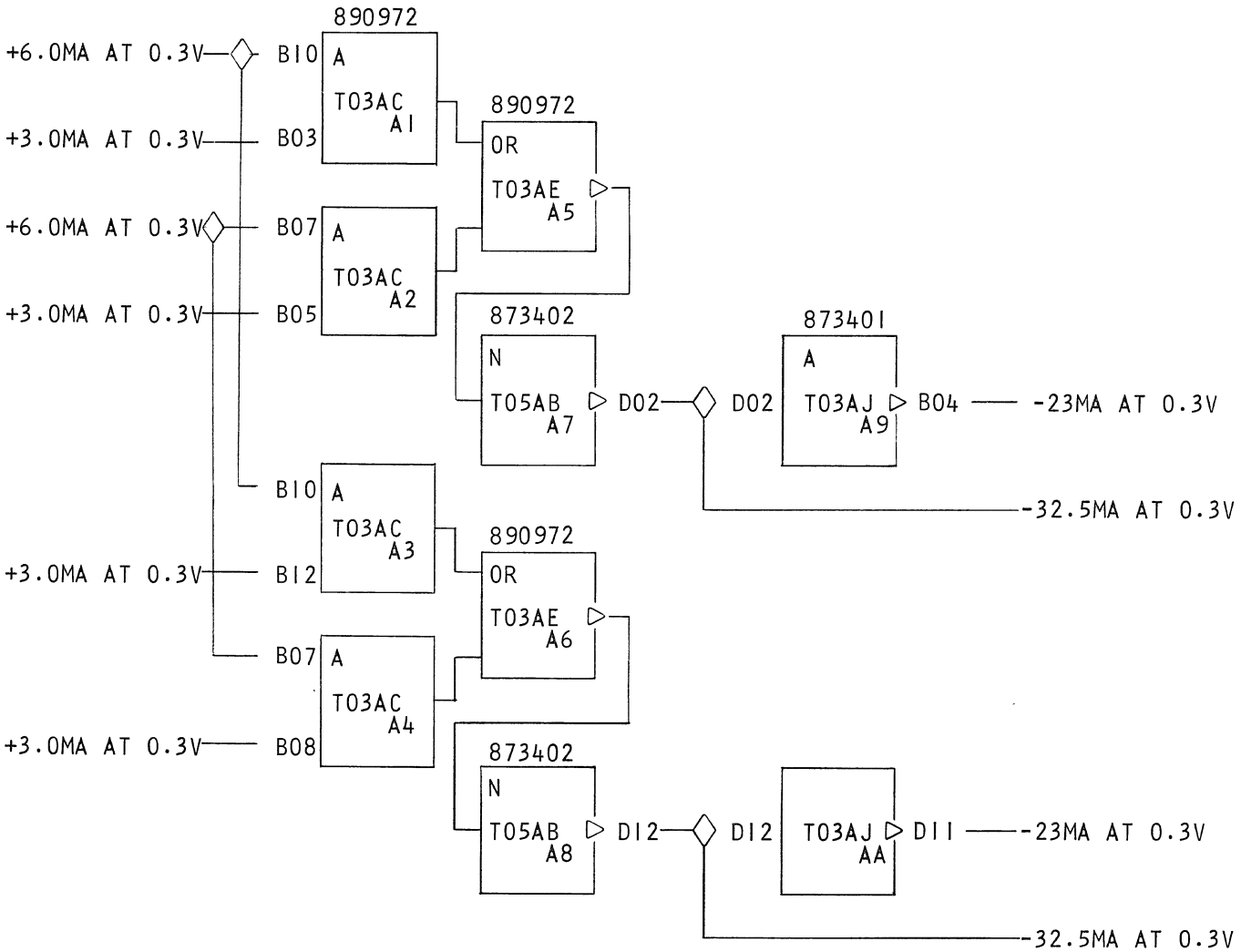
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

LATCH CARD

CATEGORY CODE

T65

P/N	5803474
EC	161274
STANDARD RESTRICTED	
CARD SIZE	1-12



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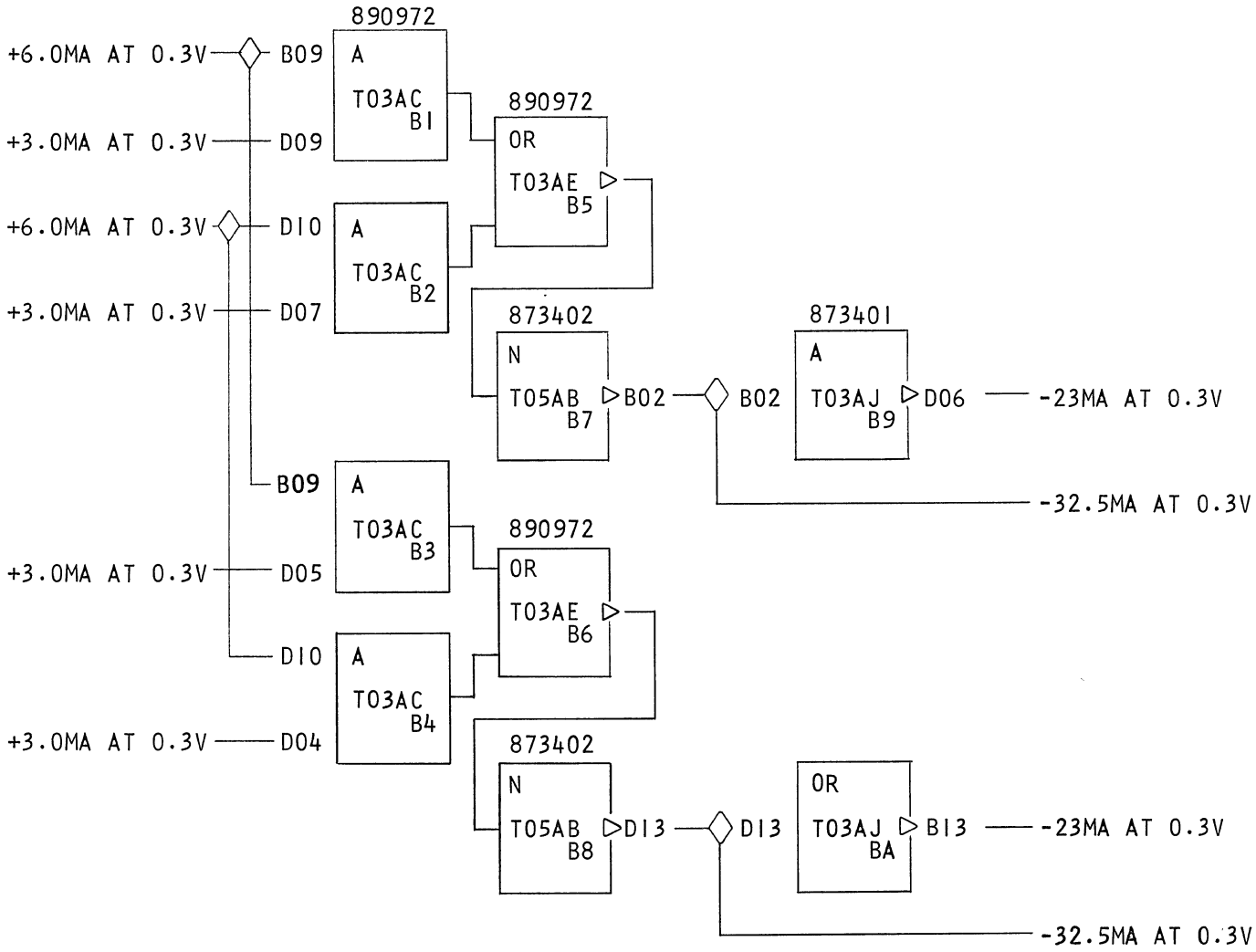
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
LATCH CARD

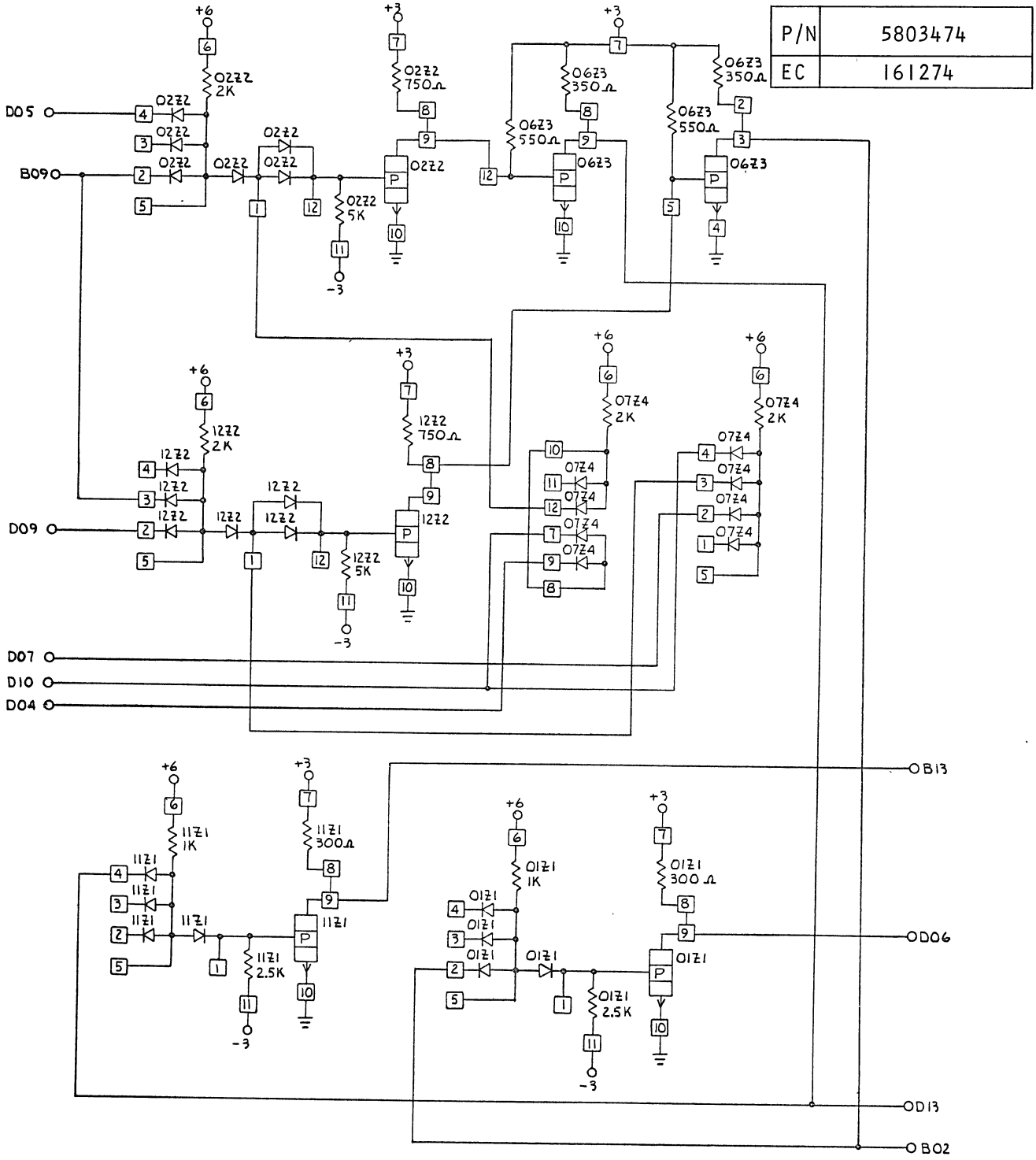
LATCH CARD

T65

P/N	5803474
EC	161274



P/N	5803474
EC	161274



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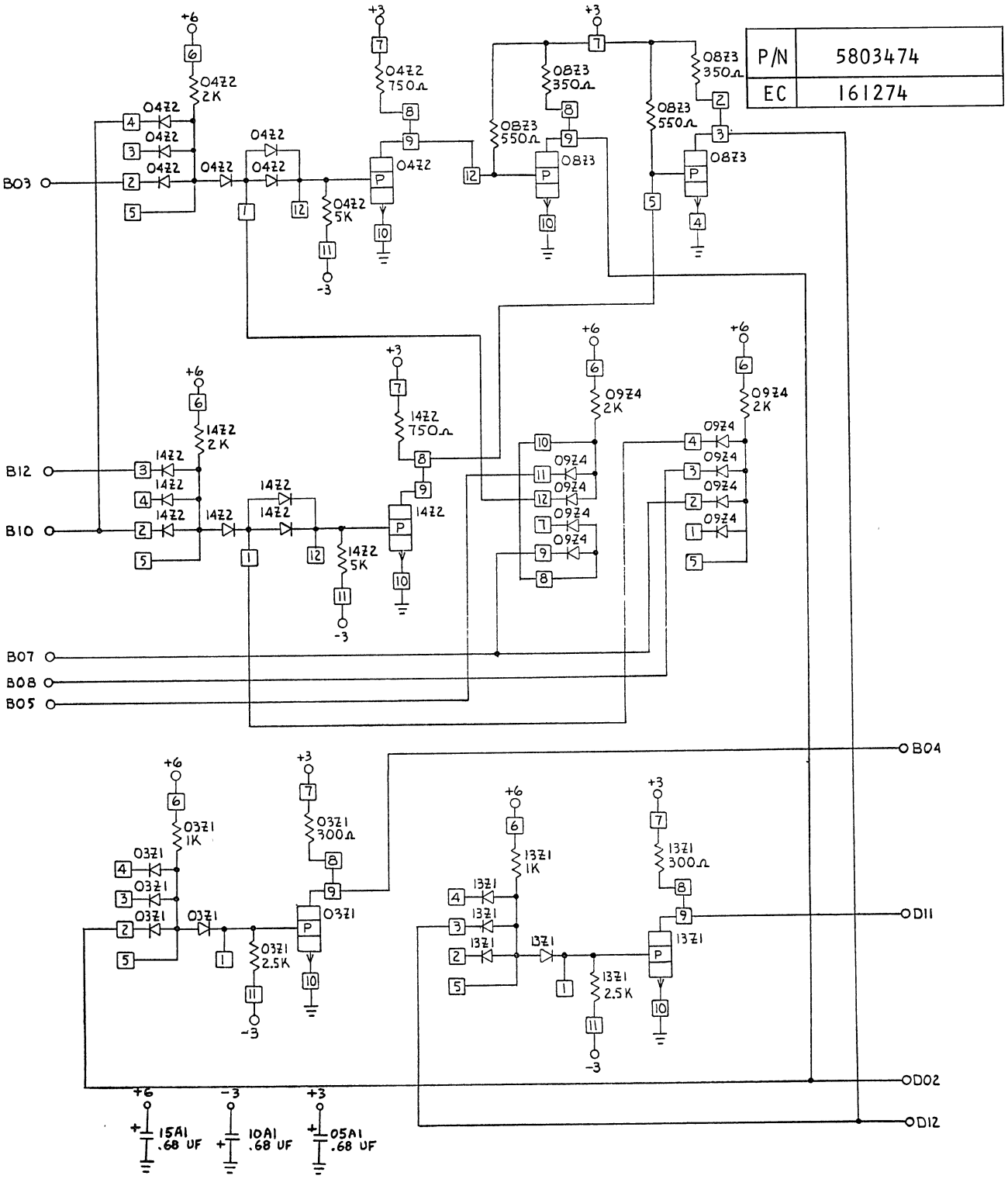
LMH Cat.	0-2860 Subject	347 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING LATCH CARD

P/N	5803474
EC	161274



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2.5M HZ X-TAL OSCILLATOR

LMH	0-2860	348
Cat.	Subject	Suffix

IBM **Location Manufacturing Specification**

POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
D08	GND

2.5M HZ X-TAL OSCILLATOR

CATEGORY CODE

T22

P/N	5803492
EC	161400
SPECIAL RESTRICTED	
CARD SIZE	1-12

872751

OSC	B02	-6.4MA AT 0.3V
T22SE A1	TB12	TEST POINT ONLY
	TB13	TEST POINT ONLY

NOTE: FOR NORMAL USAGE CONNECT PIN B12 TO PIN B13

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability	ENDICOTT	ENDICOTT Responsibility	1-67 Date	1 of 2 Page

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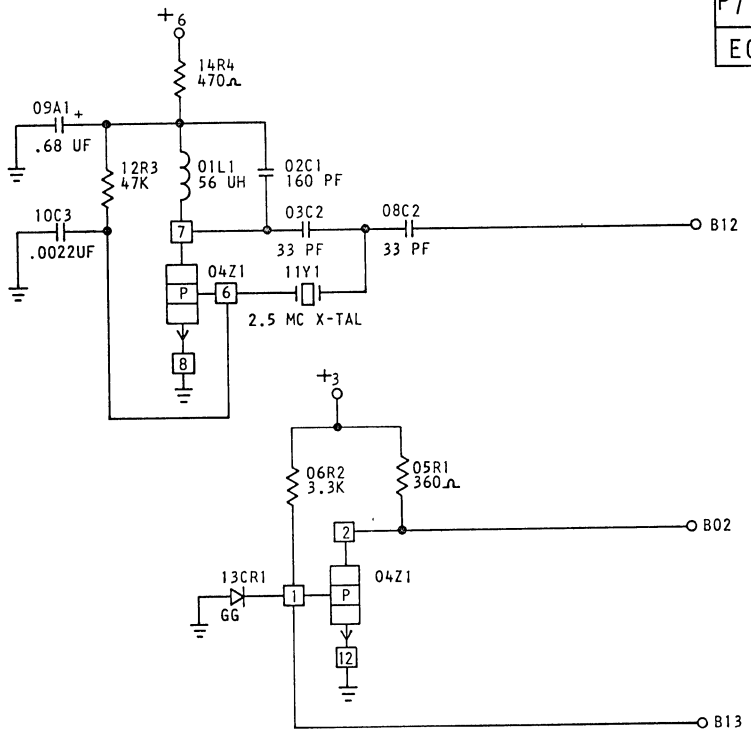
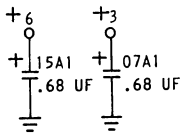
LMH Cat.	0-2860 Subject	348 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2.5M HZ X-TAL OSCILLATOR

P/N	5803492
EC	161400





SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4.0M HZ OSCILLATOR

LMH	0-2860	349
Cat	Subject	Suffix

IBM

Location

Manufacturing Specification

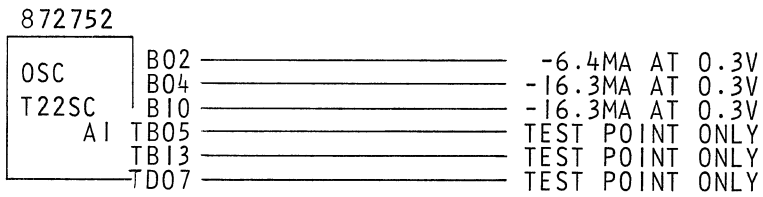
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

4.0M HZ OSCILLATOR

CATEGORY CODE

T22

P/N	5803493	
EC	165199	
SPECIAL RESTRICTED		
CARD SIZE		1-12



NOTE: FOR NORMAL USAGE CONNECT PIN B05 TO PIN B13

06-09	00-00			
Primary Standards Manual	Other standards manuals in which this document may be filed.			
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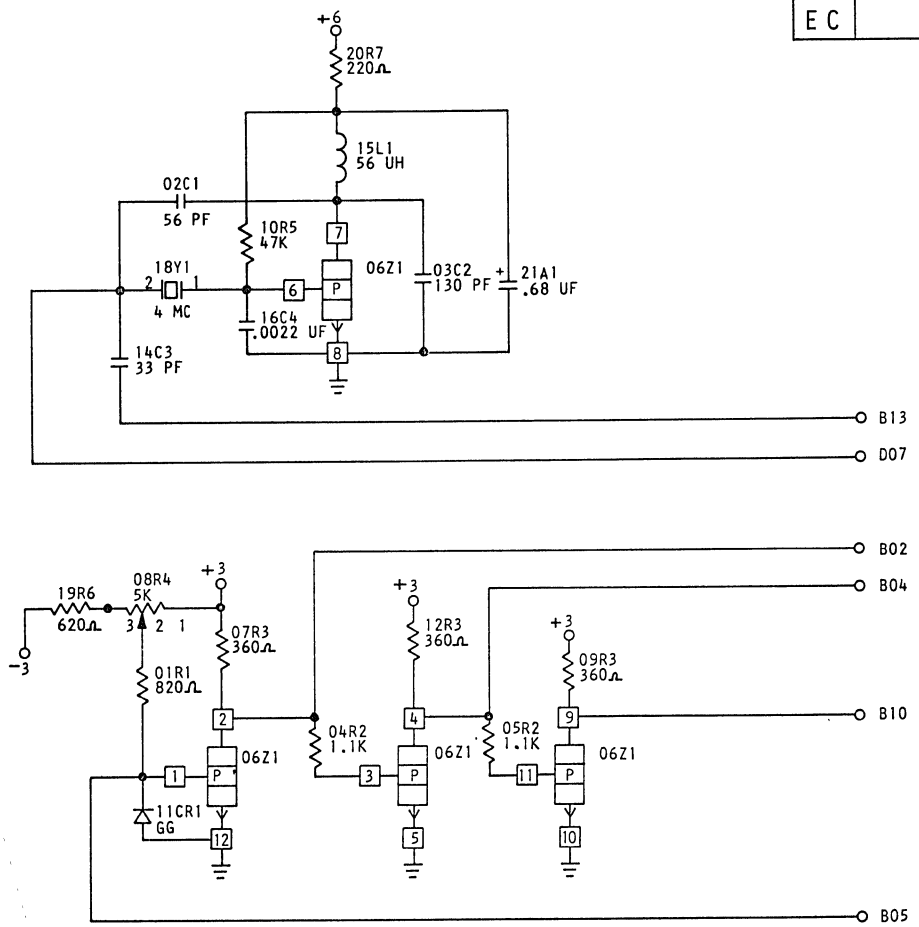
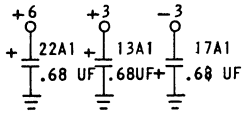
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4.0M HZ OSCILLATOR

P/N	5803493
E C	165199





SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-S.P. (N/O) 12 VOLT REED RELAYS

LMH	0-2860	350
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

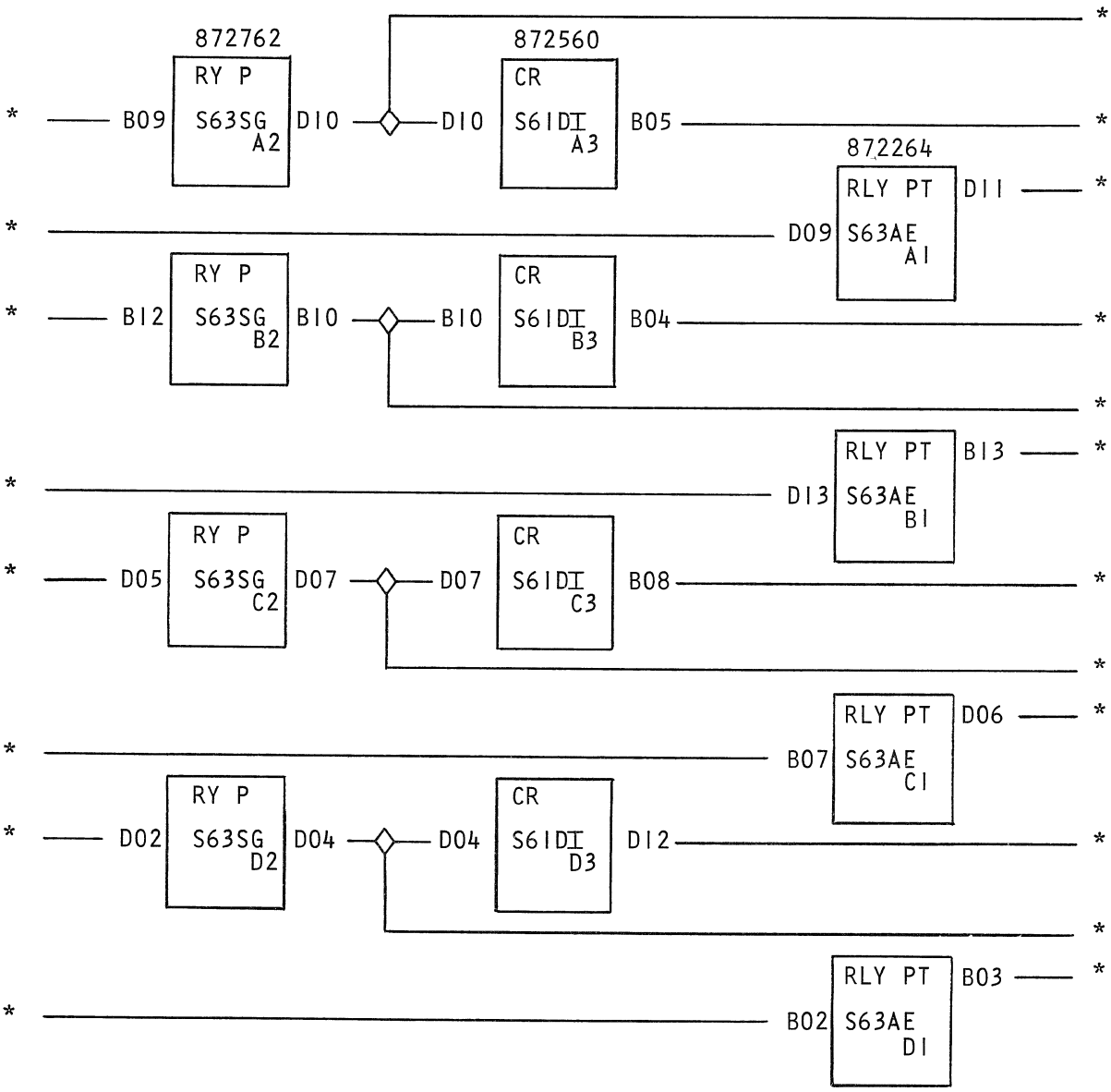
POWER REQUIRED
NONE *

4-S.P. (N/O) 12 VOLT REED RELAYS

CATEGORY CODE

S63

P/N	5803495	
EC	161426	
SPECIAL RESTRICTED		
CARD SIZE		1-12



* SPECIAL REQUIREMENTS SEE CIRCUIT SPECIFICATION 872762

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
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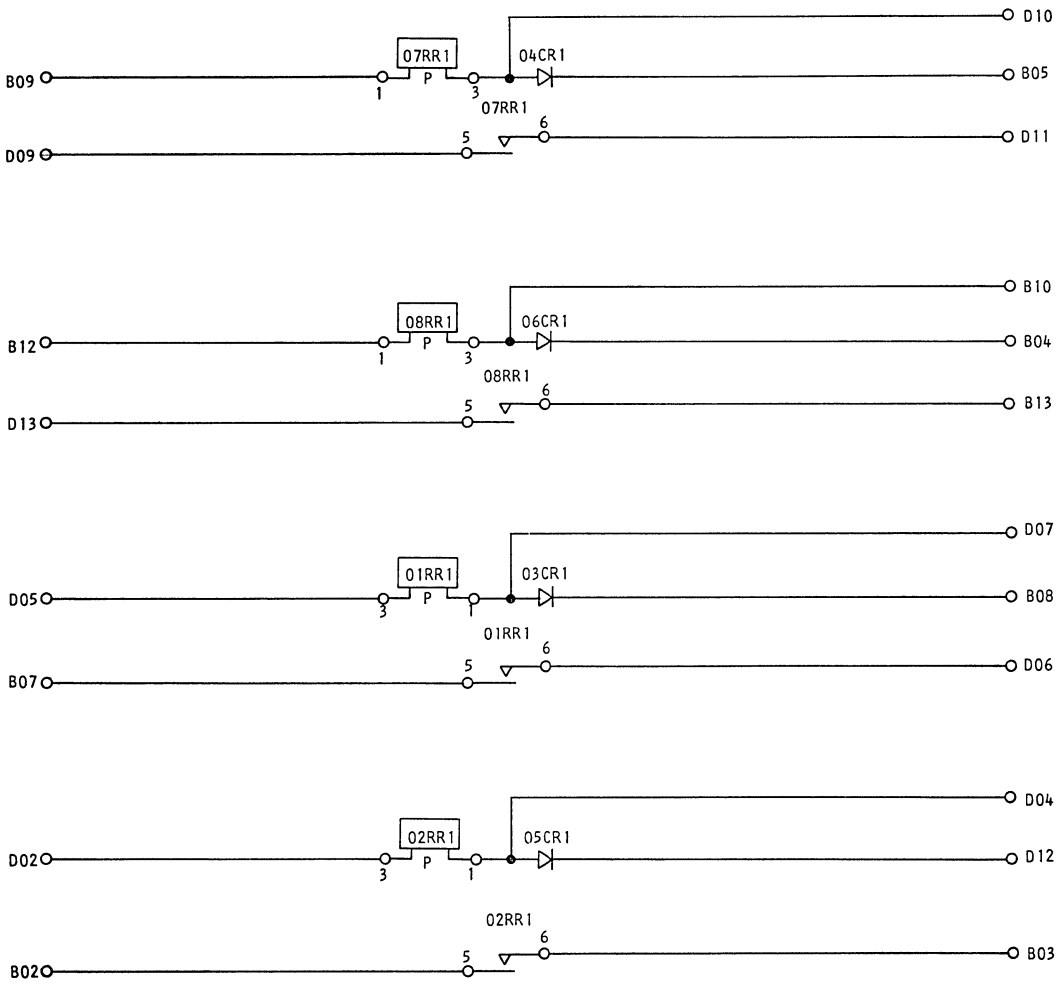
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-S.P. (N/O) 12 VOLT REED RELAYS

P/N	5803495
EC	161426



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2M HZ OSCILLATOR

LMH Cat.	0-2860 Subject	351 Suffix

IBM **Location Manufacturing Specification**

POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2M HZ OSCILLATOR

CATEGORY CODE

T22

P/N	5803499	
EC	167918	
SPECIAL RESTRICTED		
CARD SIZE		1-12

872775

OSC T22SB A1

B02	-6.4MA AT 0.3V
B04	-16.3MA AT 0.3V
B10	-16.3MA AT 0.3V
TB05	TEST POINT ONLY
TB13	TEST POINT ONLY
TD07	TEST POINT ONLY

NOTE: FOR NORMAL USAGE CONNECT PIN B05 TO PIN B13

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability ENDICOTT		ENDICOTT Responsibility	1-67 Date	1 OF 2 Page

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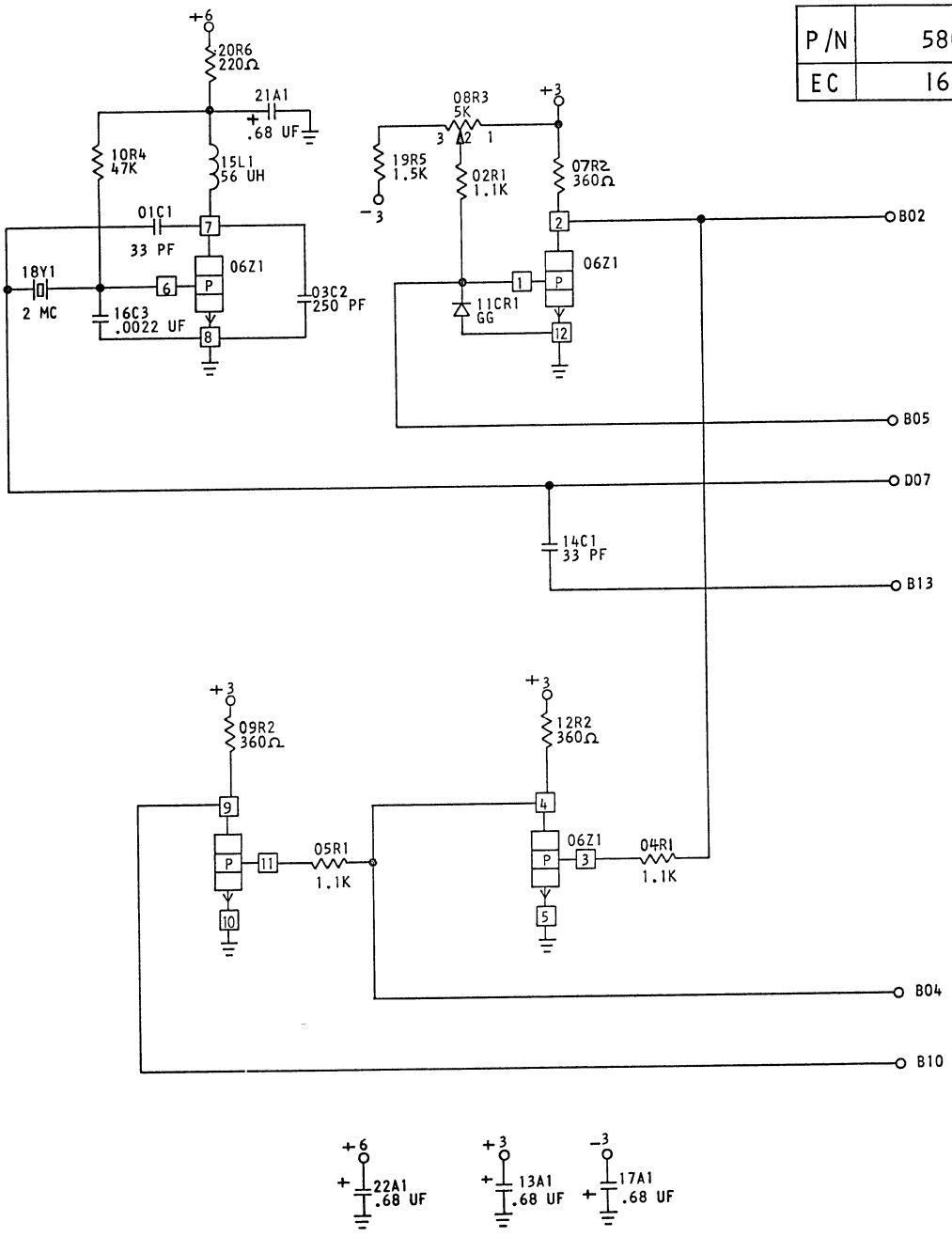
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2M HZ OSCILLATOR

P/N	5803499
EC	167918



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
5 POWER LATCHES

LMH	0-2860	352
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

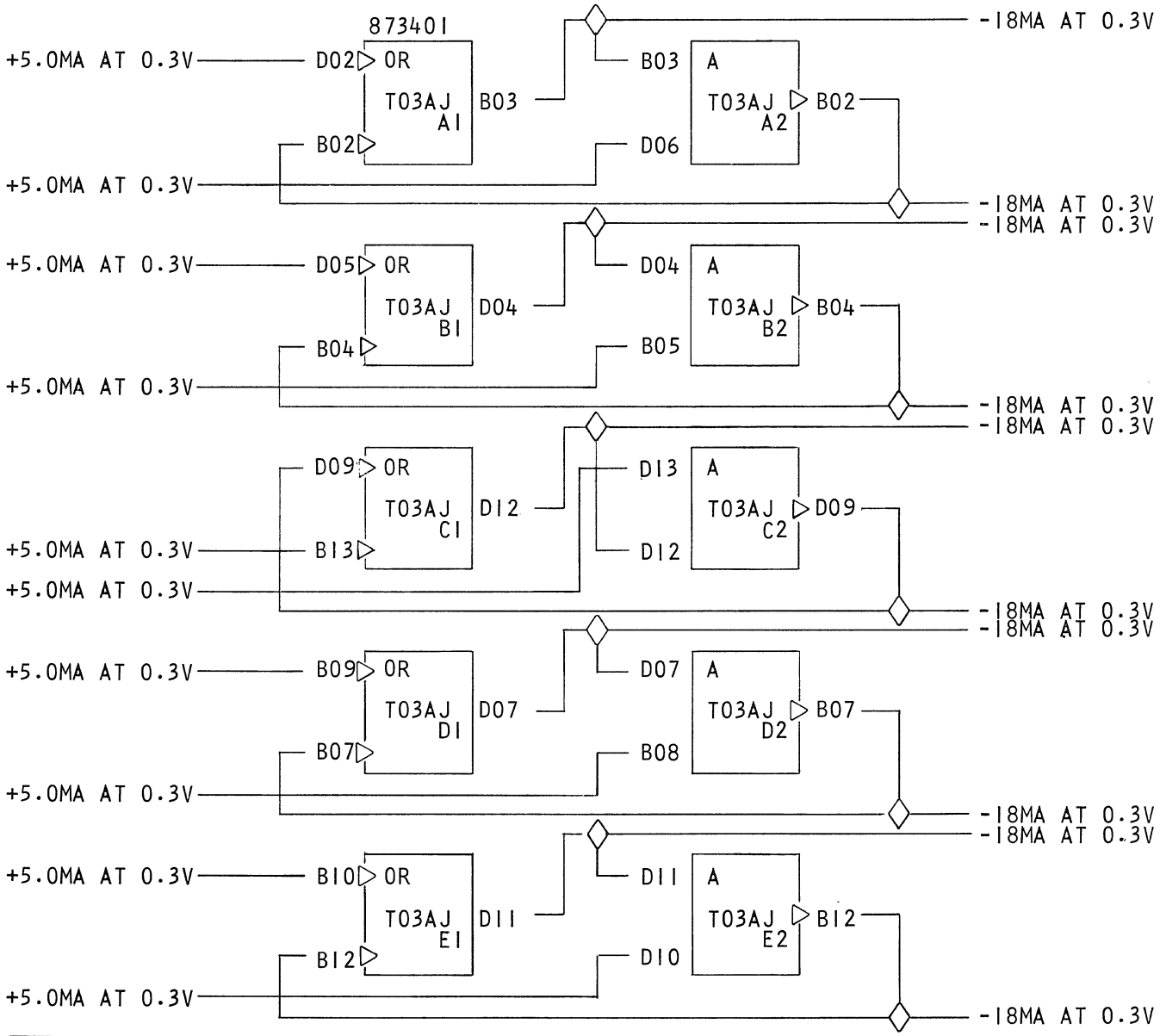
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

5 POWER LATCHES

CATEGORY CODE

T03

P/N	5803531	
EC	163180	
SPECIAL RESTRICTED		
CARD SIZE		1-12



06-09	00-00			
Primary Standards Manual	Other standards manuals in which this document may be filed.			
ENDICOTT		ENDICOTT	1-67	1 OF 3
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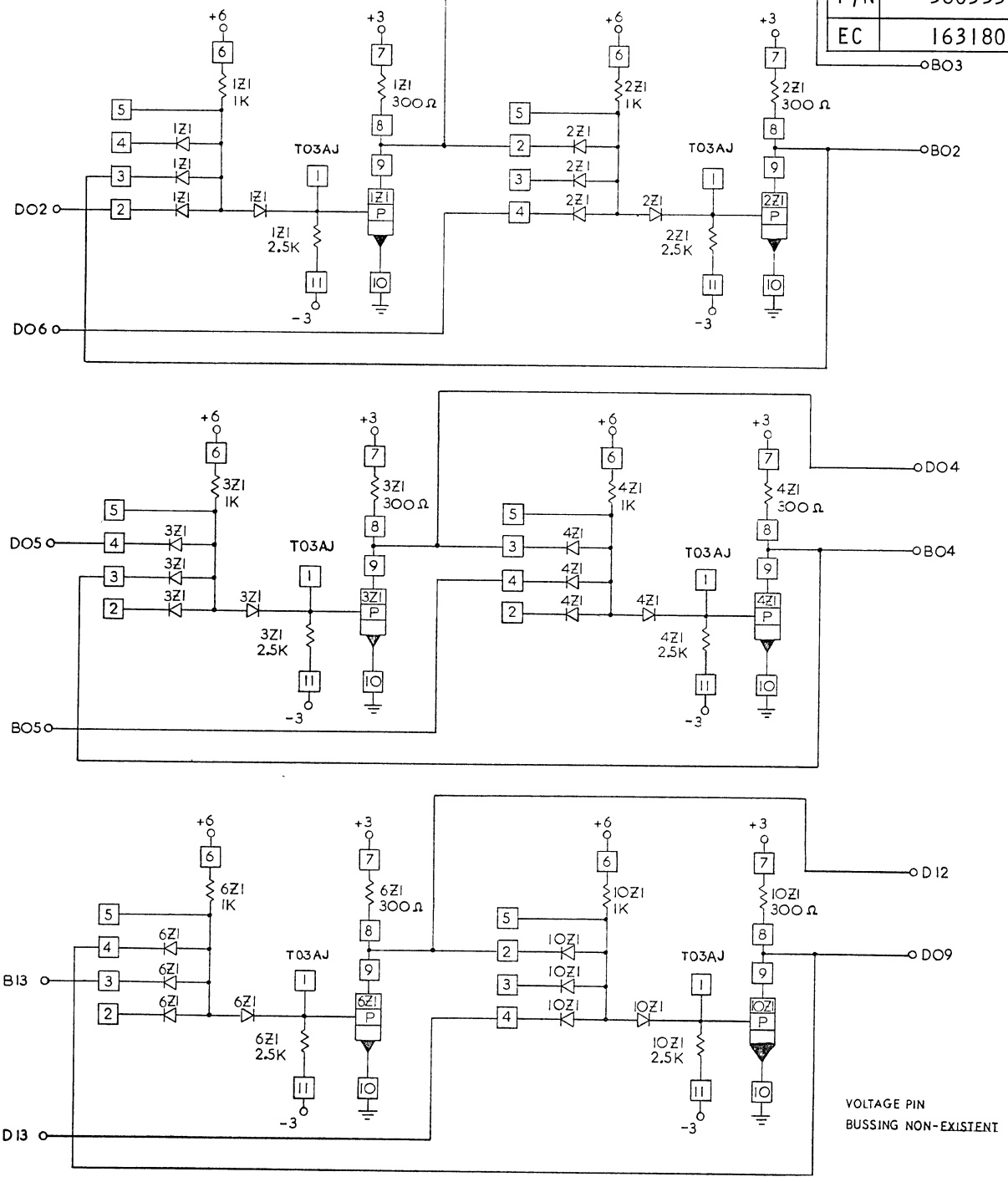
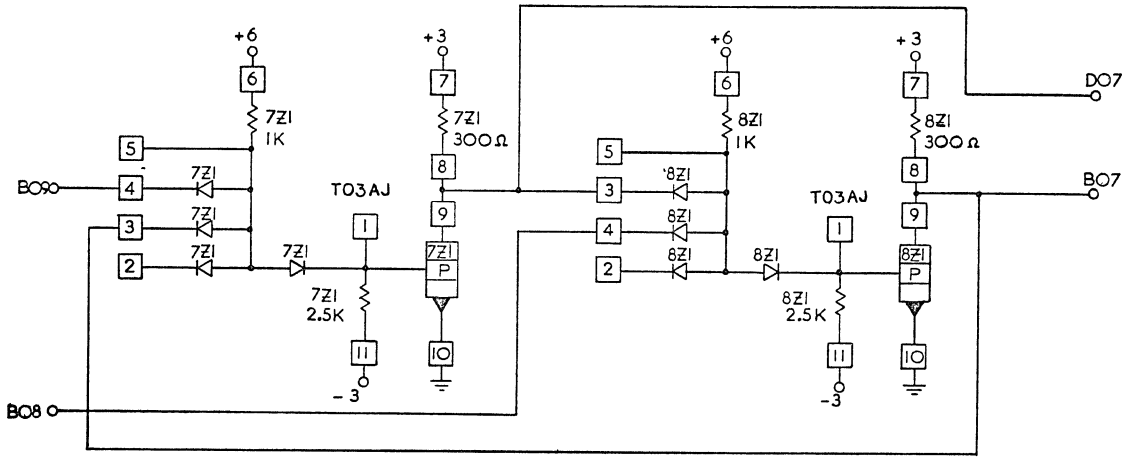
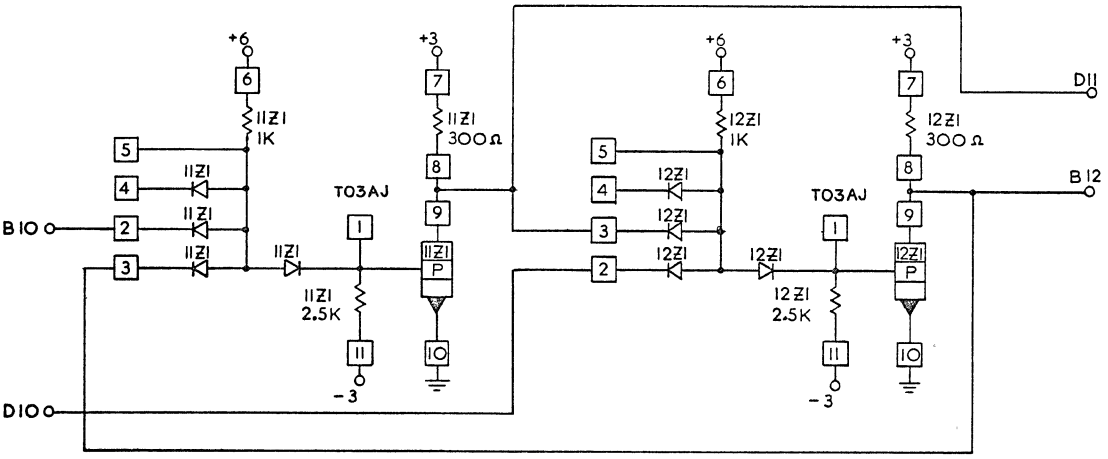
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
5 POWER LATCHES

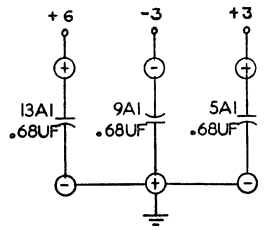
P/N	5803531
EC	163180



P/N	5803531
EC	163180







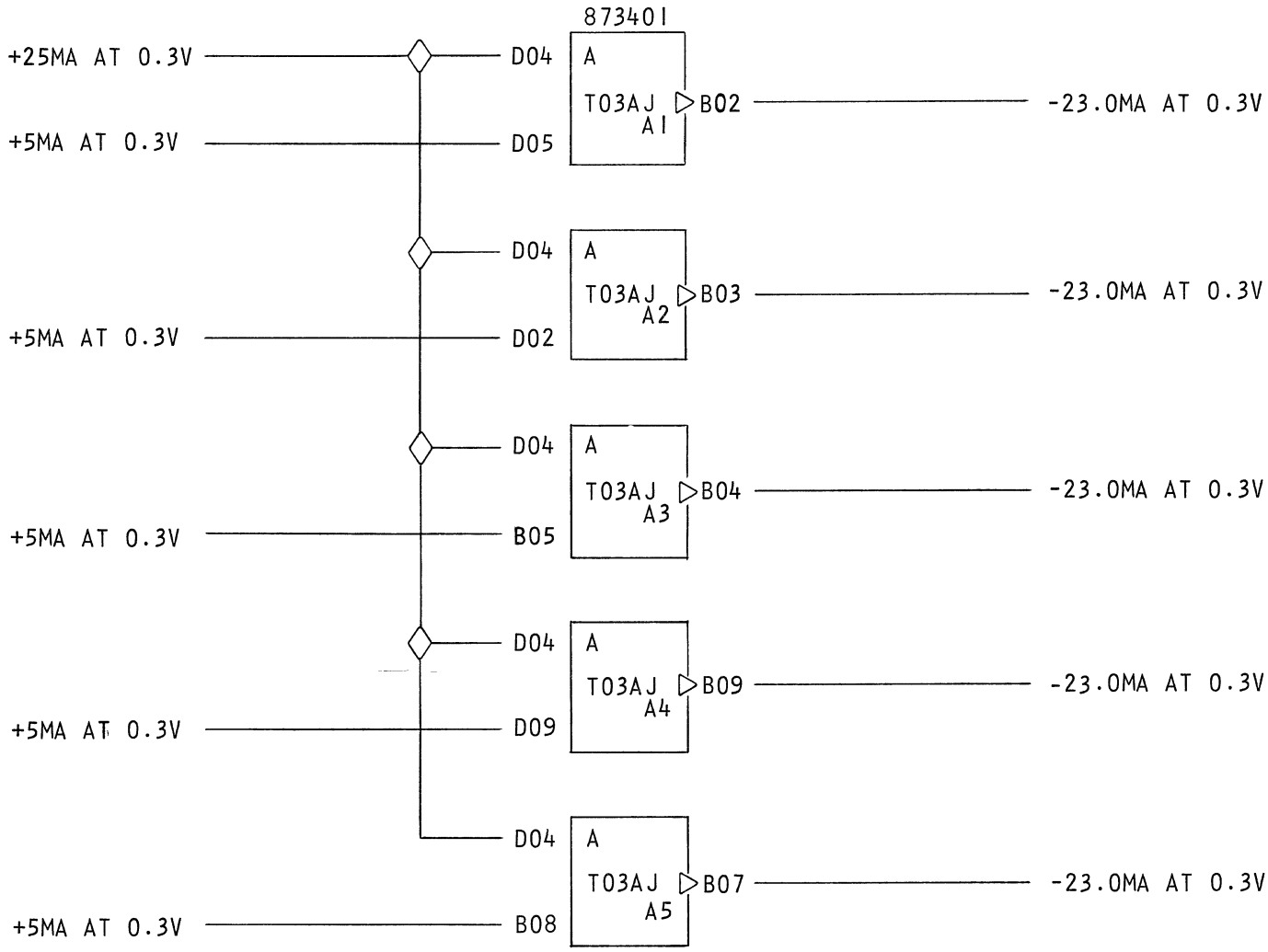
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

5-2W COMMON GATED API & 4-2W COMMON GATED API

CATEGORY CODE

T03

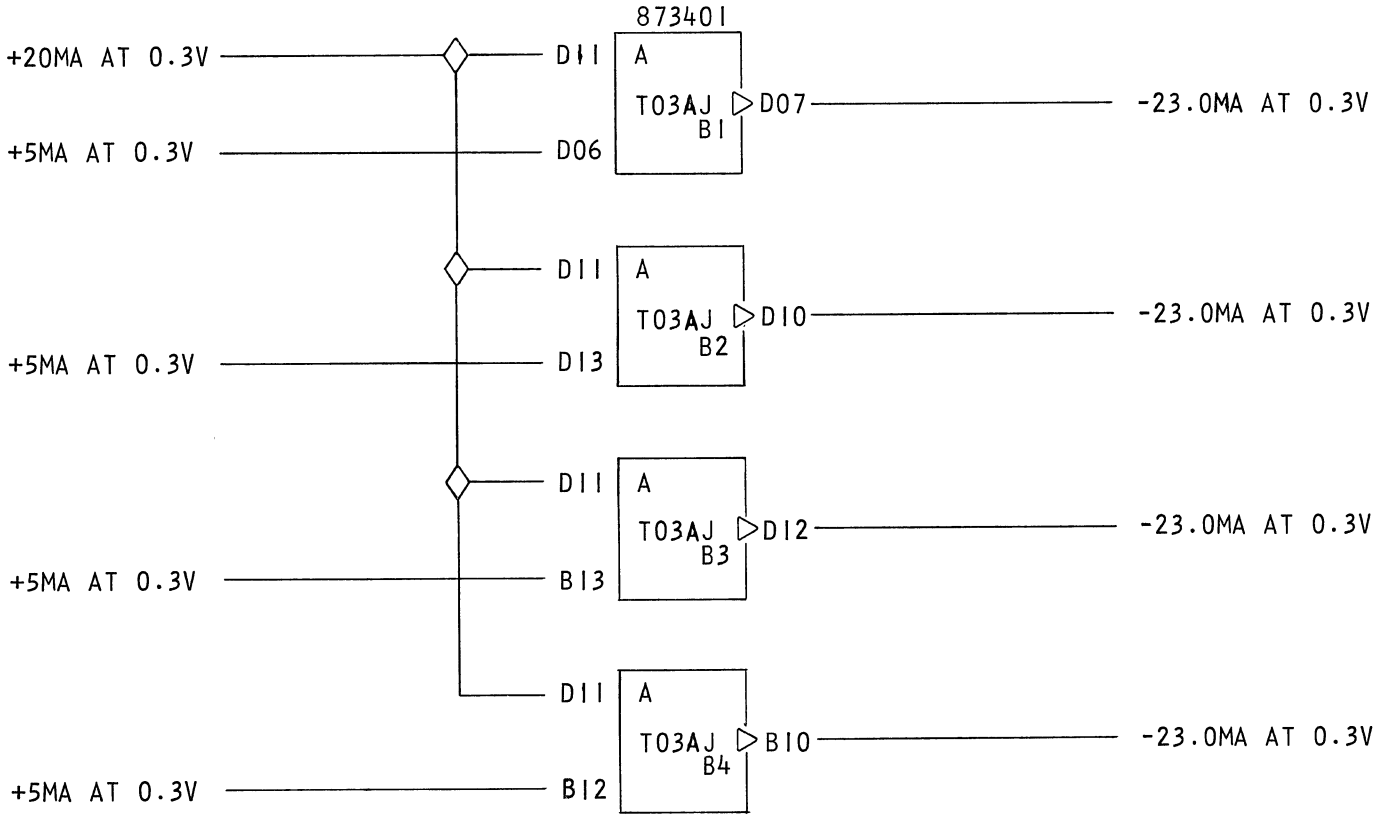
P/N	5803575
EC	160866
SPECIAL RESTRICTED	
CARD SIZE	1-12



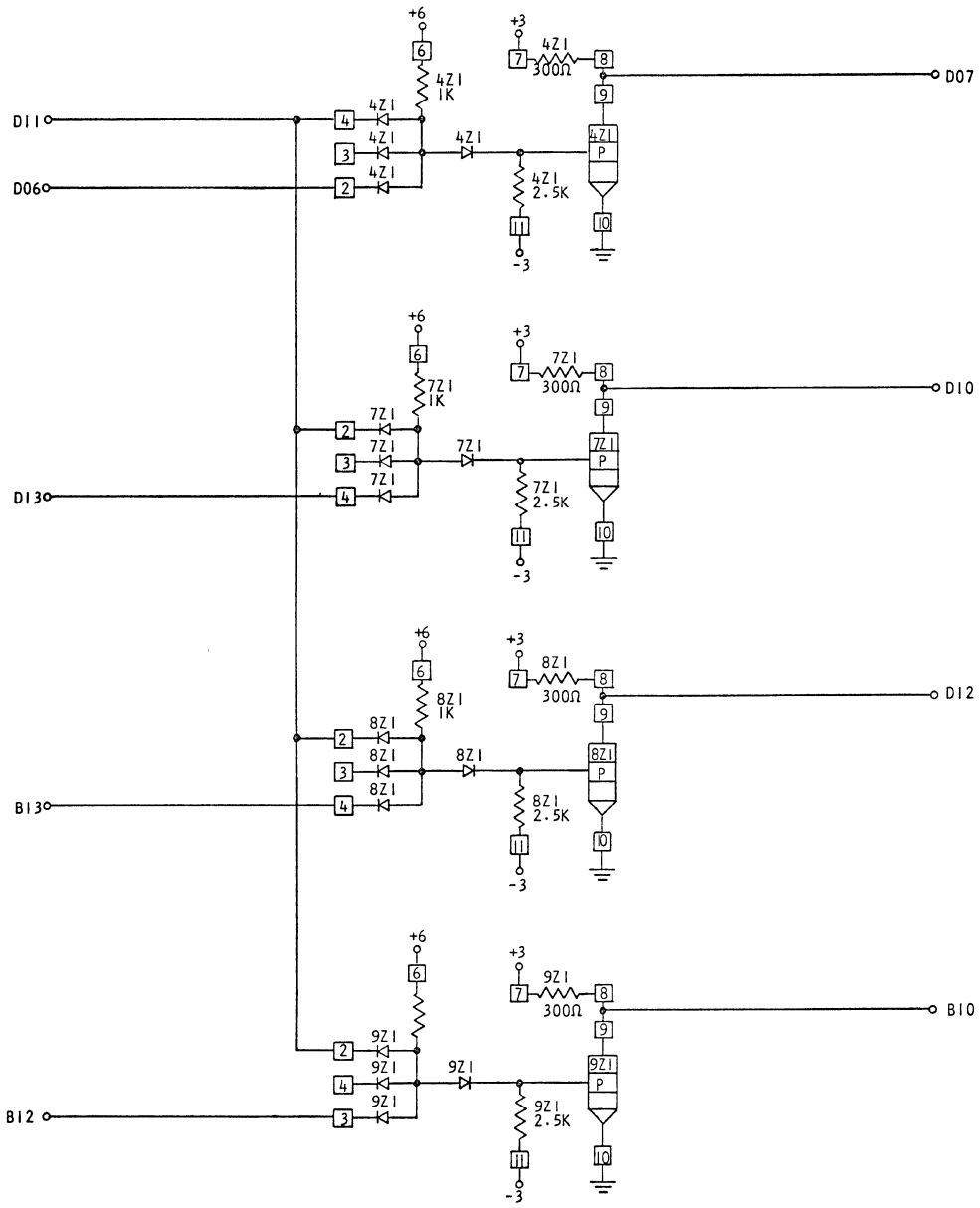
5-2W COMMON GATED API & 4-2W COMMON GATED API

T03

P/N	5803575
EC	160866



P/N	5803575
EC	160866



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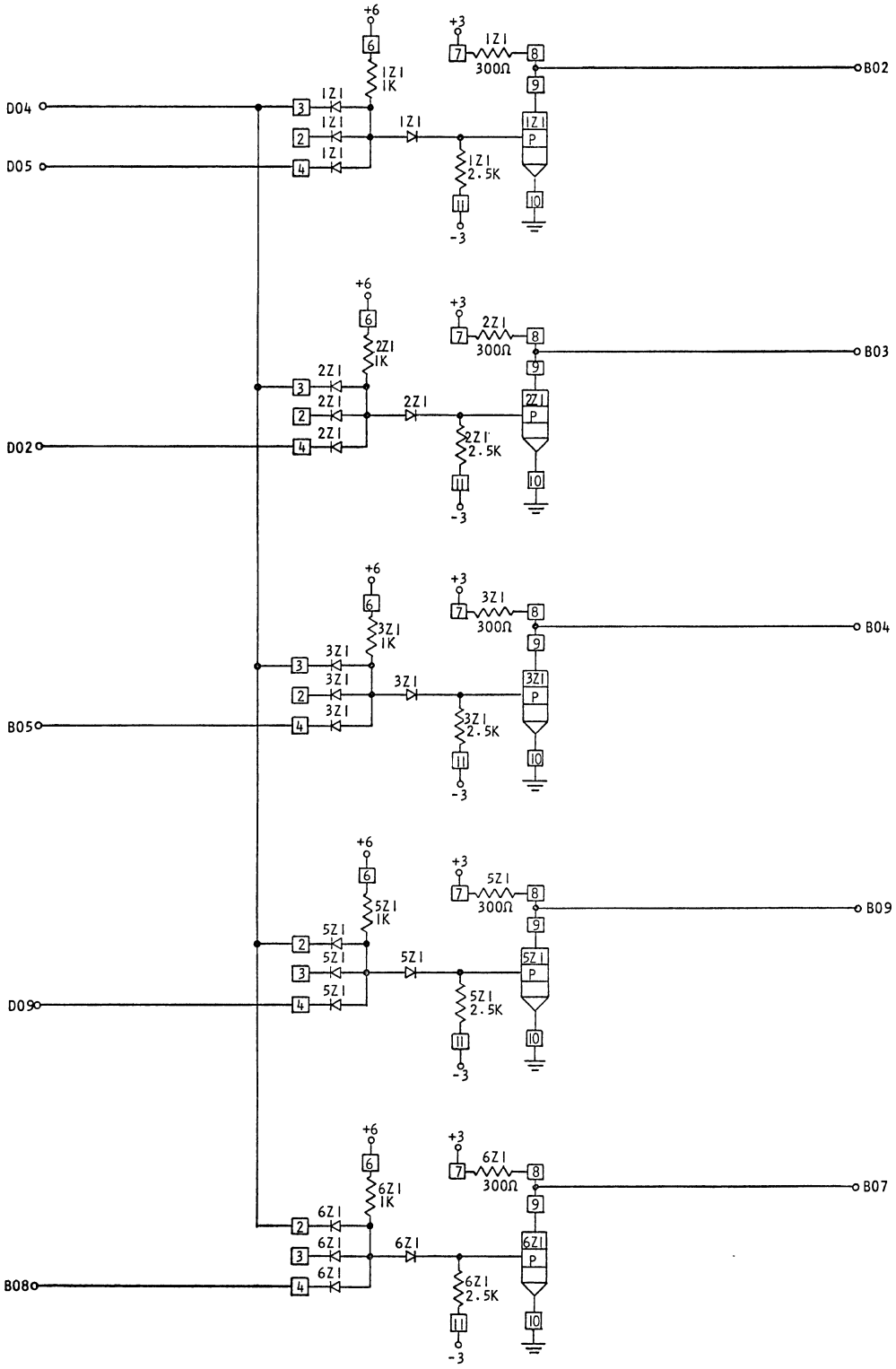
LMH Cat.	O-2860 Subject	354 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
5-2W COMMON GATED API & 4-2W COMMON GATED API

P/N	5803575
EC	160866



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-S.P. (N/O) 6 VOLT REED RELAYS

LMH	0-2860	355
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

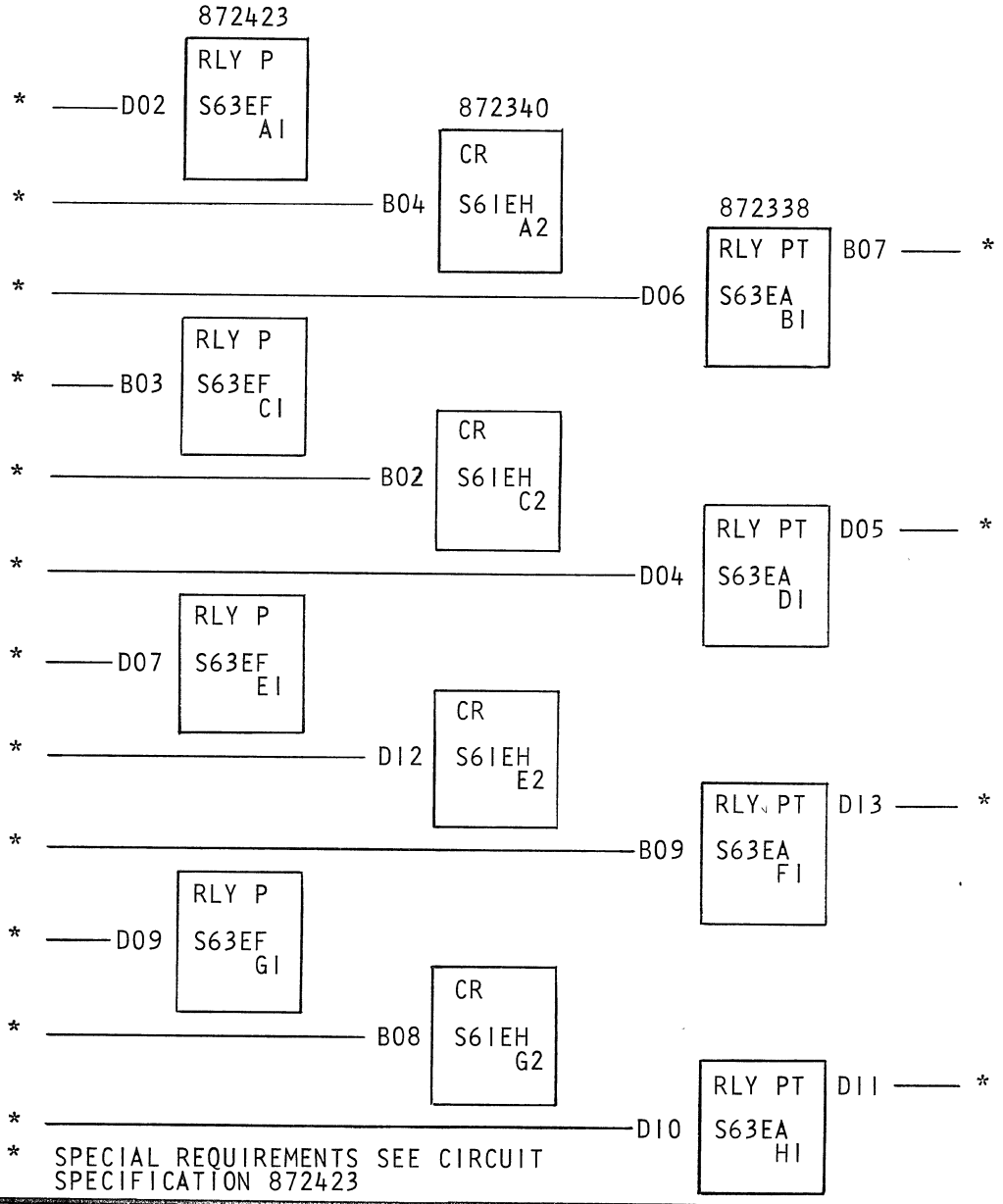
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

4-S.P. (N/O) 6 VOLT REED RELAYS

CATEGORY CODE

S63

P/N	5803576
EC	165714B
SPECIAL	RESTRICTED
CARD SIZE	1-12



* SPECIAL REQUIREMENTS SEE CIRCUIT SPECIFICATION 872423

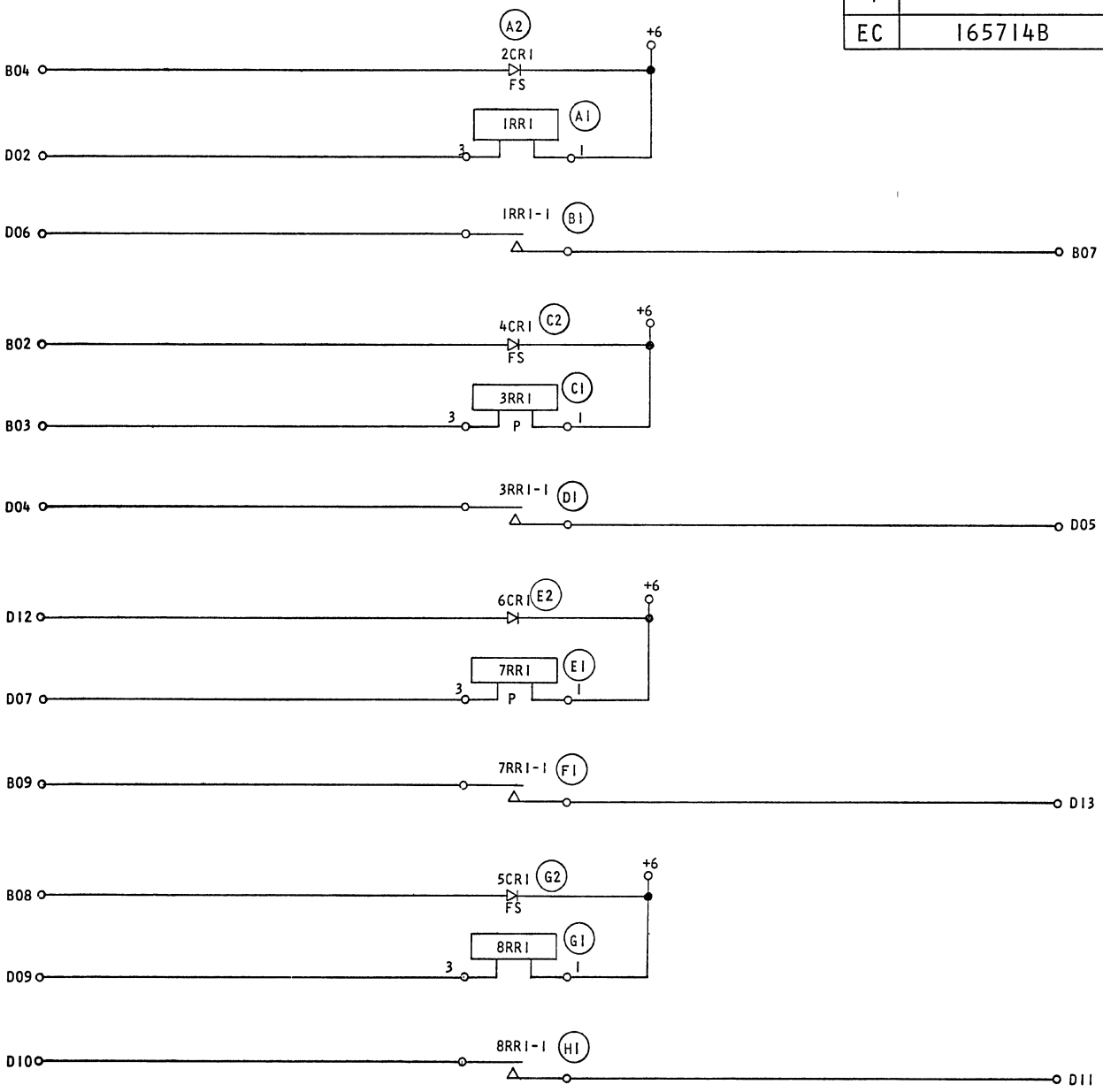
06-09	00-00			
Primary Standards Manual	Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		Responsibility: ENDICOTT	Jan. 67 Date	1 of 2 Page

PRINTED IN USA

LMH Cat.	0-2860 Subject	355 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-S.P. (N/O) 6 VOLT REED RELAYS

P/N	5803576
EC	165714B



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
20-300 OHM LOAD RESISTORS TO +3V

LMH	0-2860	356
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

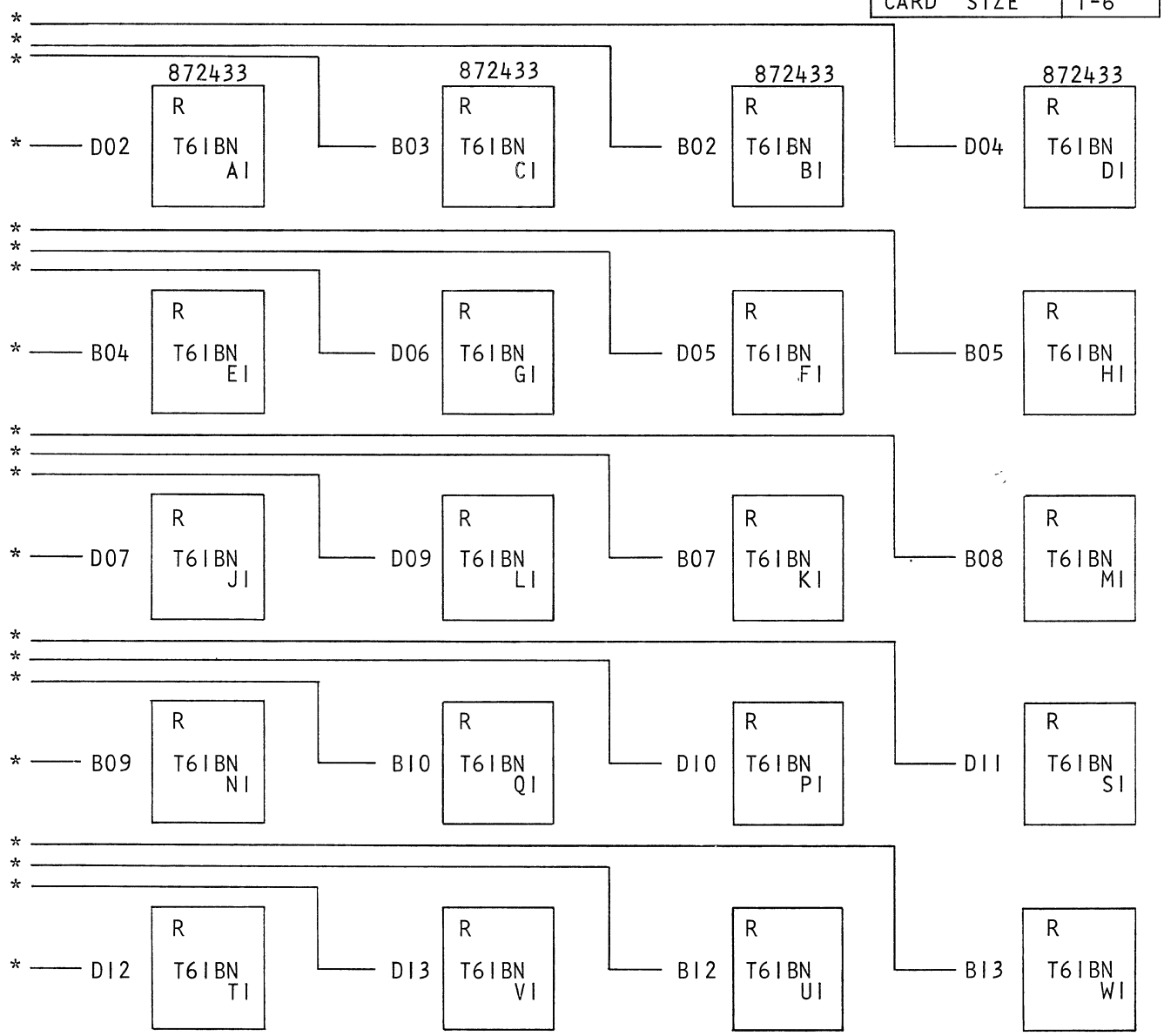
POWER REQUIRED	
PIN	VOLTS
D03	+3
D08	GND

20-300 OHM LOAD RESISTORS TO +3V

CATEGORY CODE

T61

P/N	5803577
EC	168025B
SPECIAL RESTRICTED	
CARD SIZE	1-6



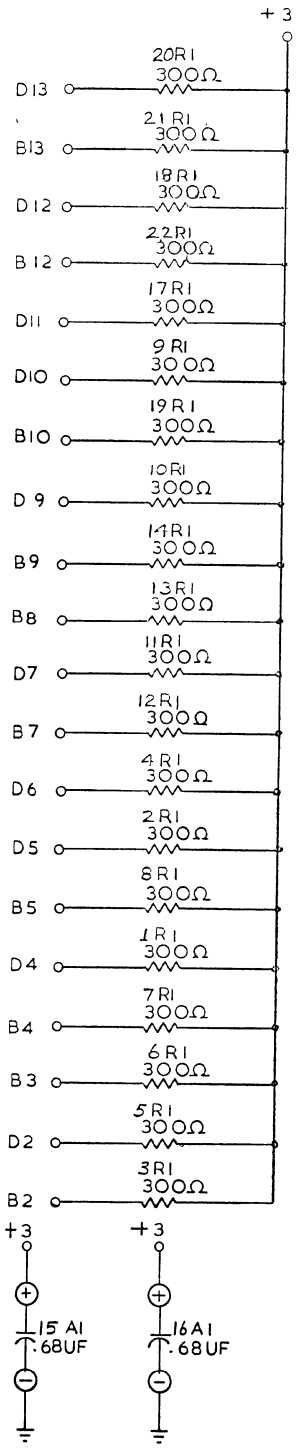
NOTE:
*MAXIMUM LOAD CURRENT 10.0MA AT 0.3V FOR ALL RESISTORS

06-09	00-00			
Primary Standards Manual	Other standards manuals in which this document may be filed.			
ENDICOTT		ENDICOTT	1-67	1 OF 2
Applicability		Responsibility	Date	Page

PRINTED IN USA

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
20-300 OHM LOAD RESISTORS TO +3V

P/N	5803577
EC	168025B



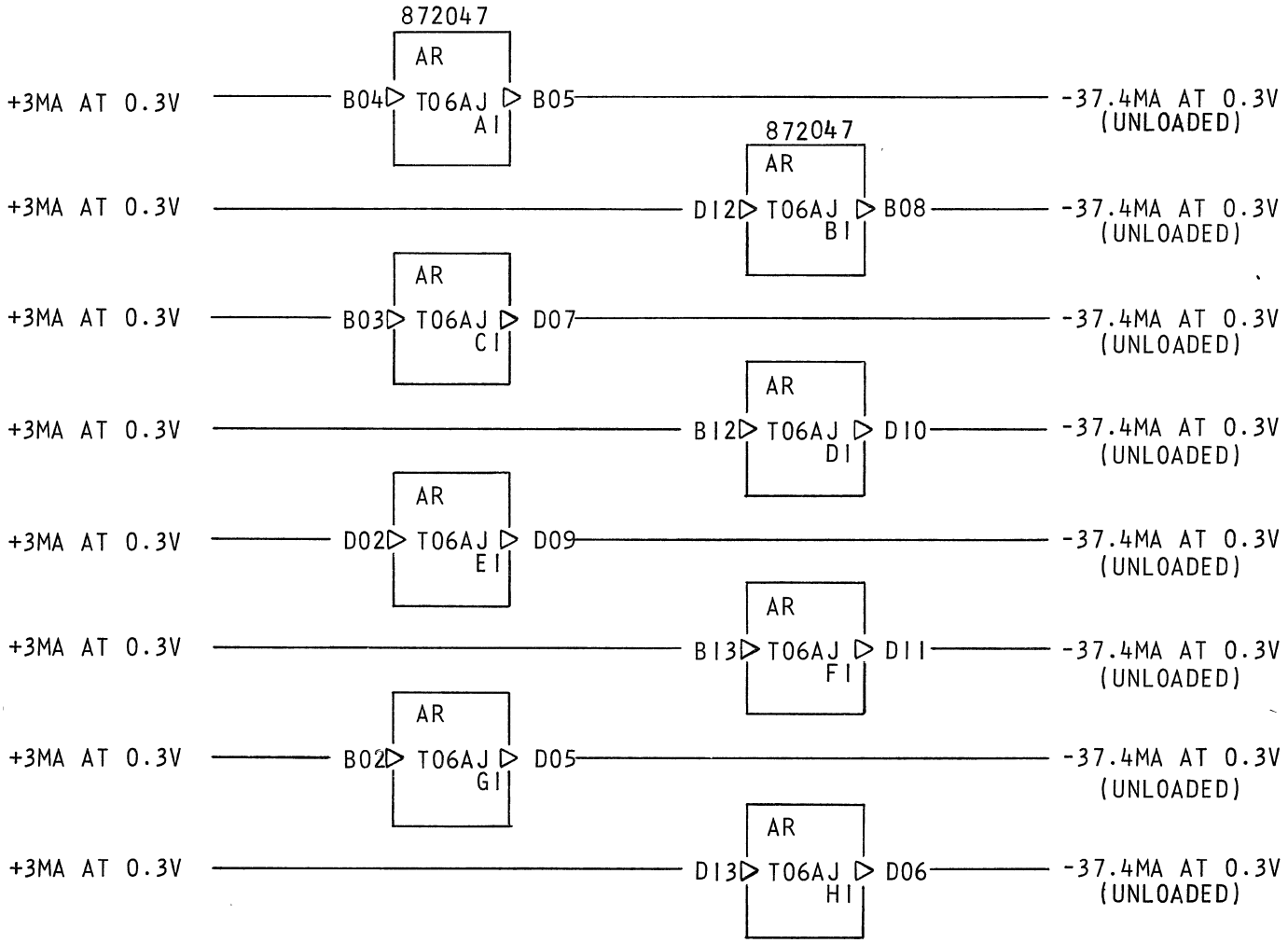
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

8-COUPLED INVERTER DRIVERS WO/L

CATEGORY CODE

T03

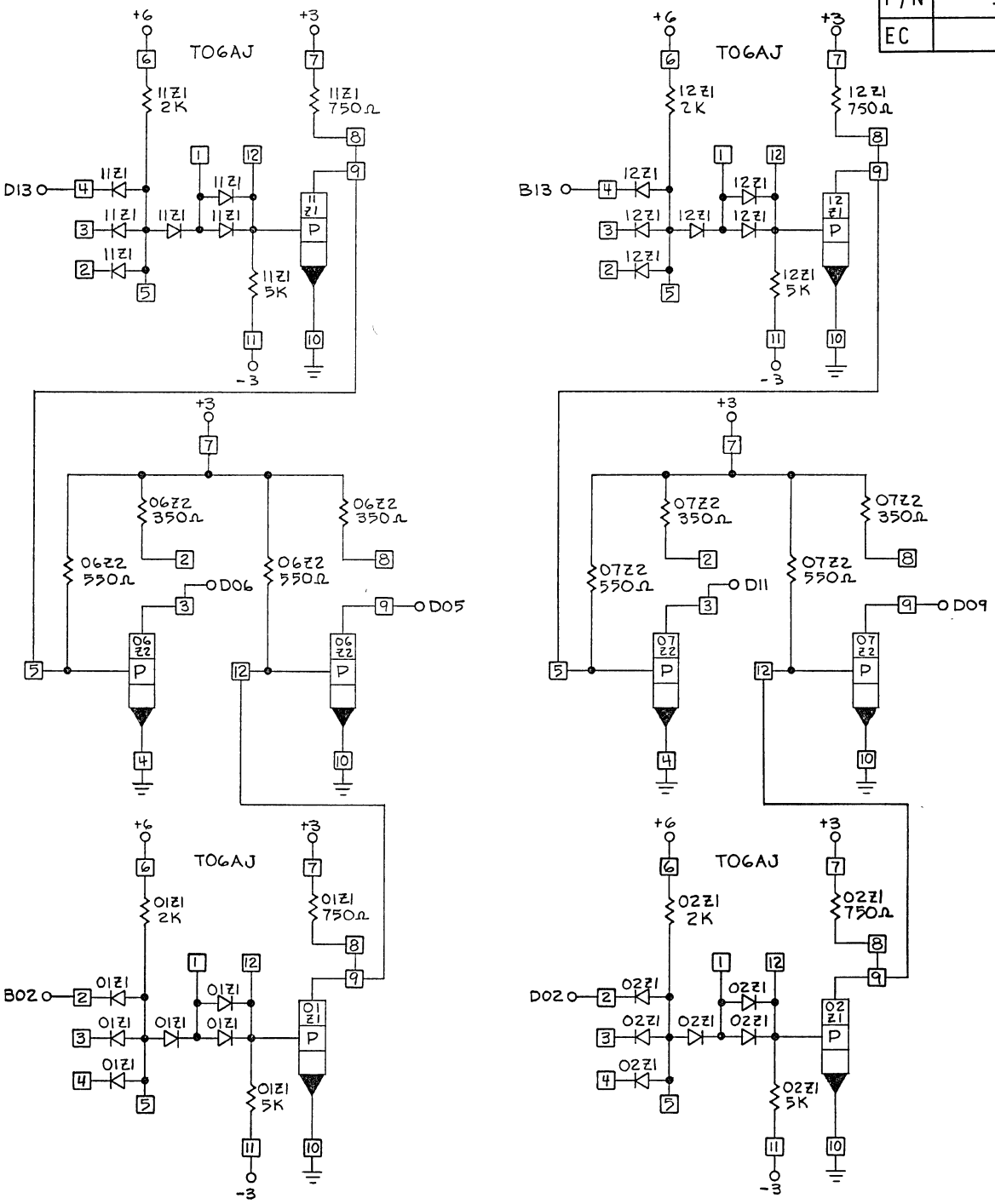
P/N	5803608
EC	163476 A
STANDARD RESTRICTED	
CARD SIZE	1-12



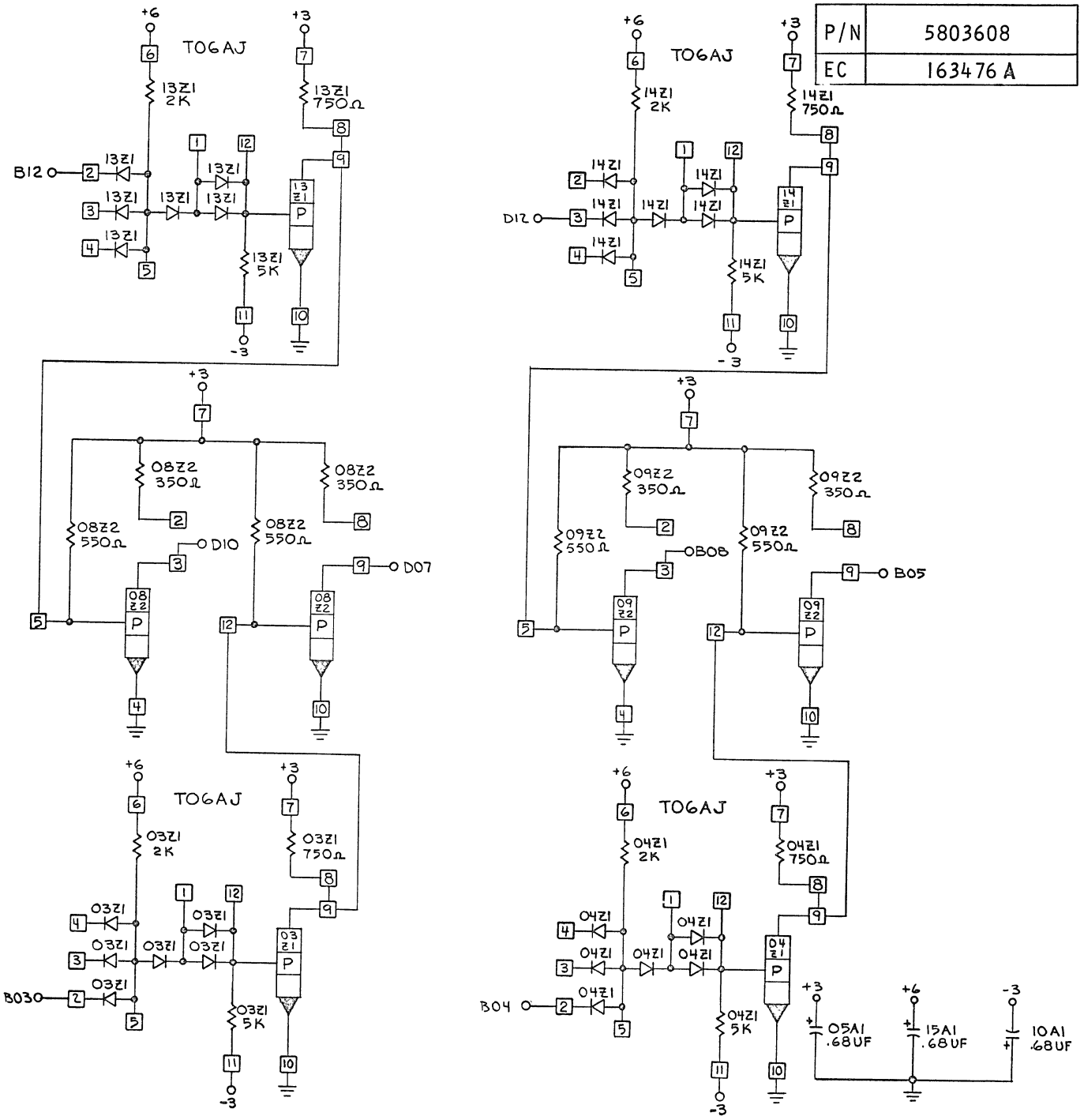
LMH Cat.	0-2860 Subject	358 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENIGNEERING
8-COUPLED INVERTER DRIVERS WO/L

P/N	5803608
EC	163476 A



P/N	5803608
EC	163476 A



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IBM **Location Manufacturing Specification**

POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

2-VARIABLE SSA

CATEGORY CODE

T03	T21

P/N	5803617
EC	182277
STANDARD RESTRICTED	
CARD SIZE	1-12

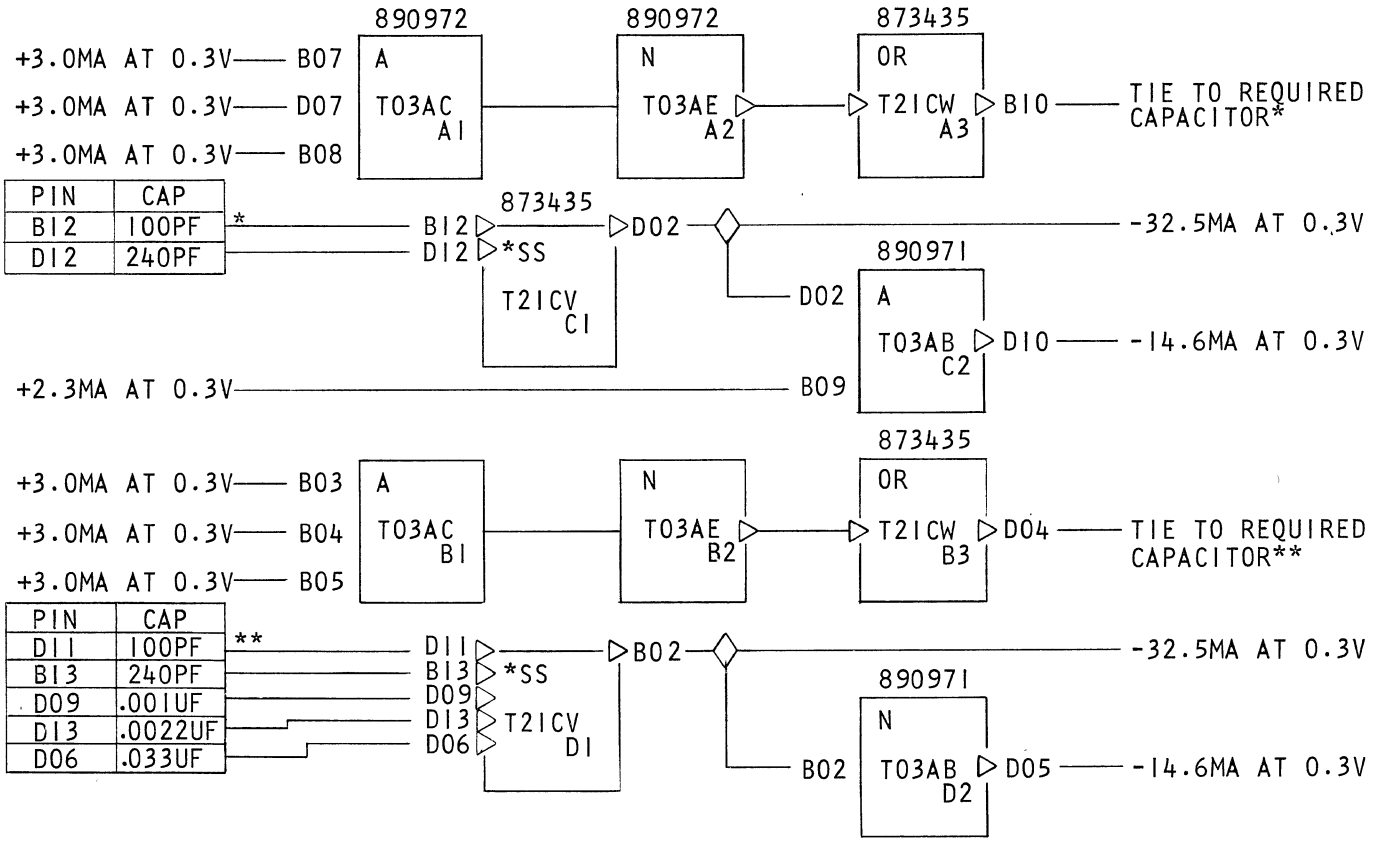


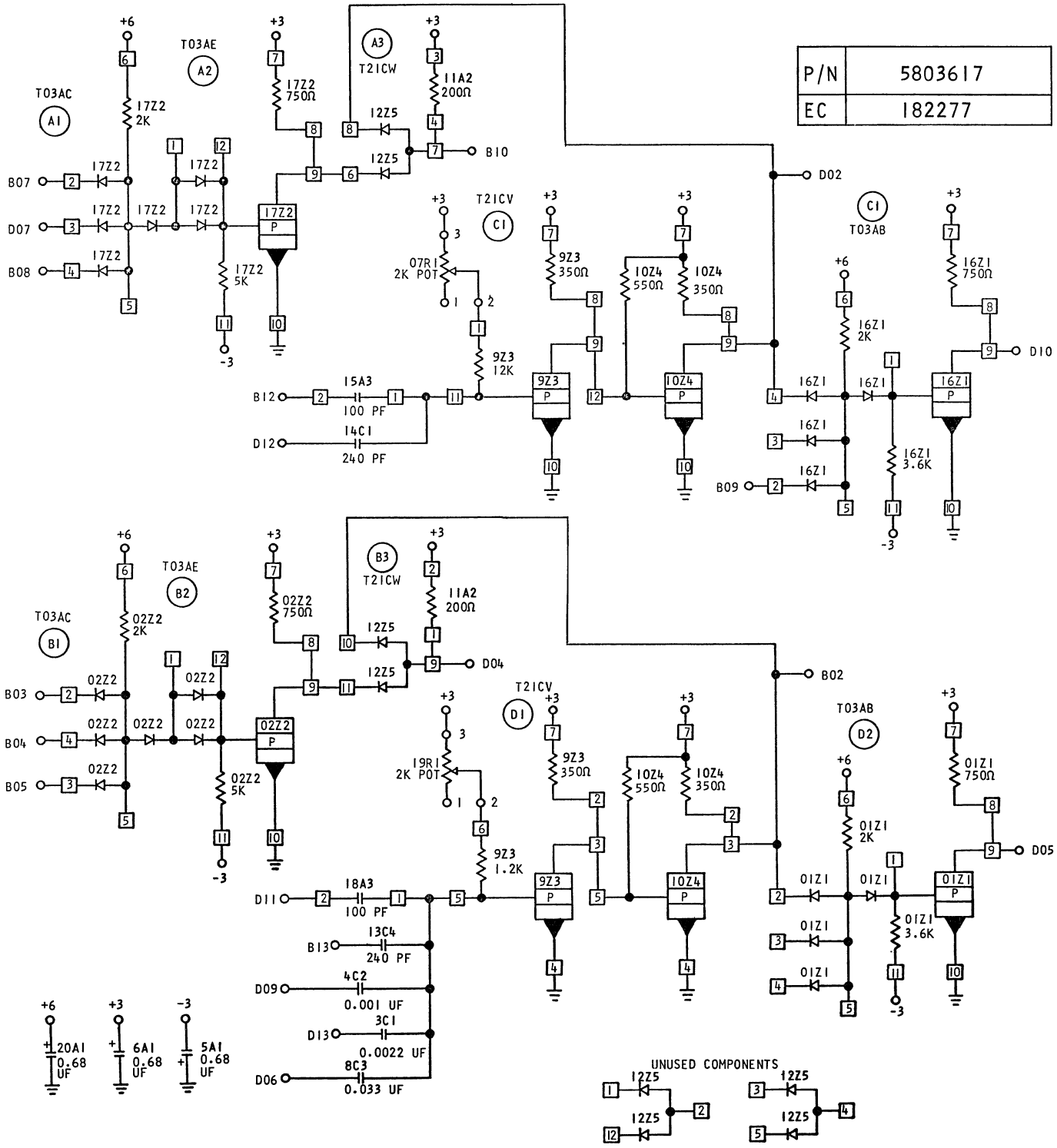
TABLE OF OUTPUT PULSEWIDTHS AND RECOVERY TIMES

CT	TMAX	TMIN	TR MIN
100PF	207NS	78NS	92NS
240PF	497NS	187NS	221NS
.001UF	2.07US	780NS	920NS
.0022UF	45.5US	17.2US	2.02US
.033UF	68.5US	25.7US	30.4US

LMH Cat.	0-2860 Subject	360 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-VARIABLE SSA

P/N	5803617
EC	182277



Page	Date
2 of 2	1-67

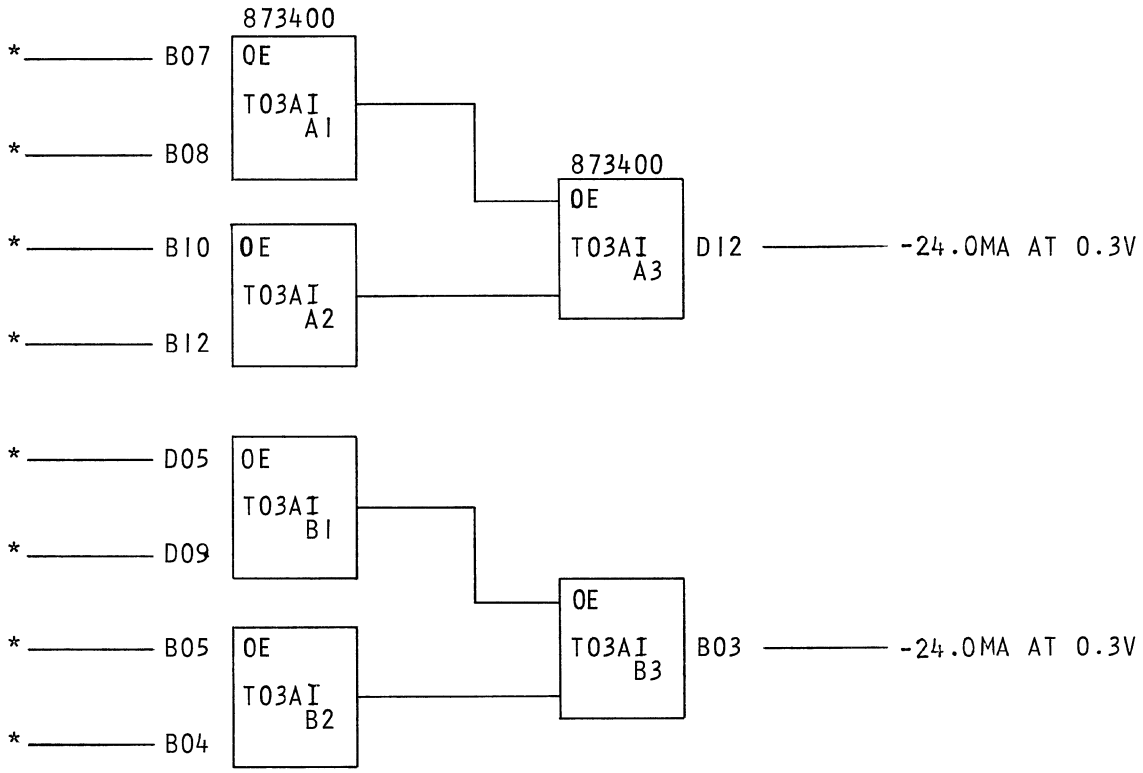
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

XOR CARD

CATEGORY CODE

T03

P/N	5803639
EC	160616
SPECIAL RESTRICTED	
CARD SIZE	1-12



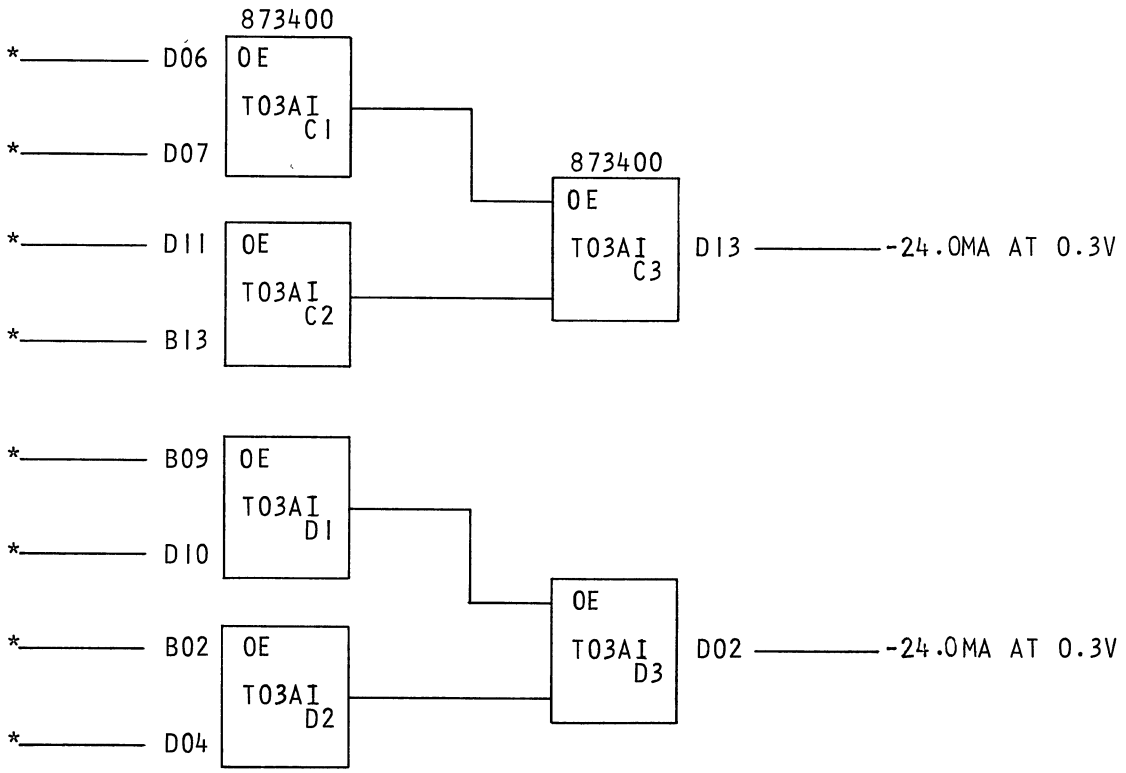
*SPECIAL DRIVE RULES- SEE CIRCUIT SPEC. 873400

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
XOR CARD

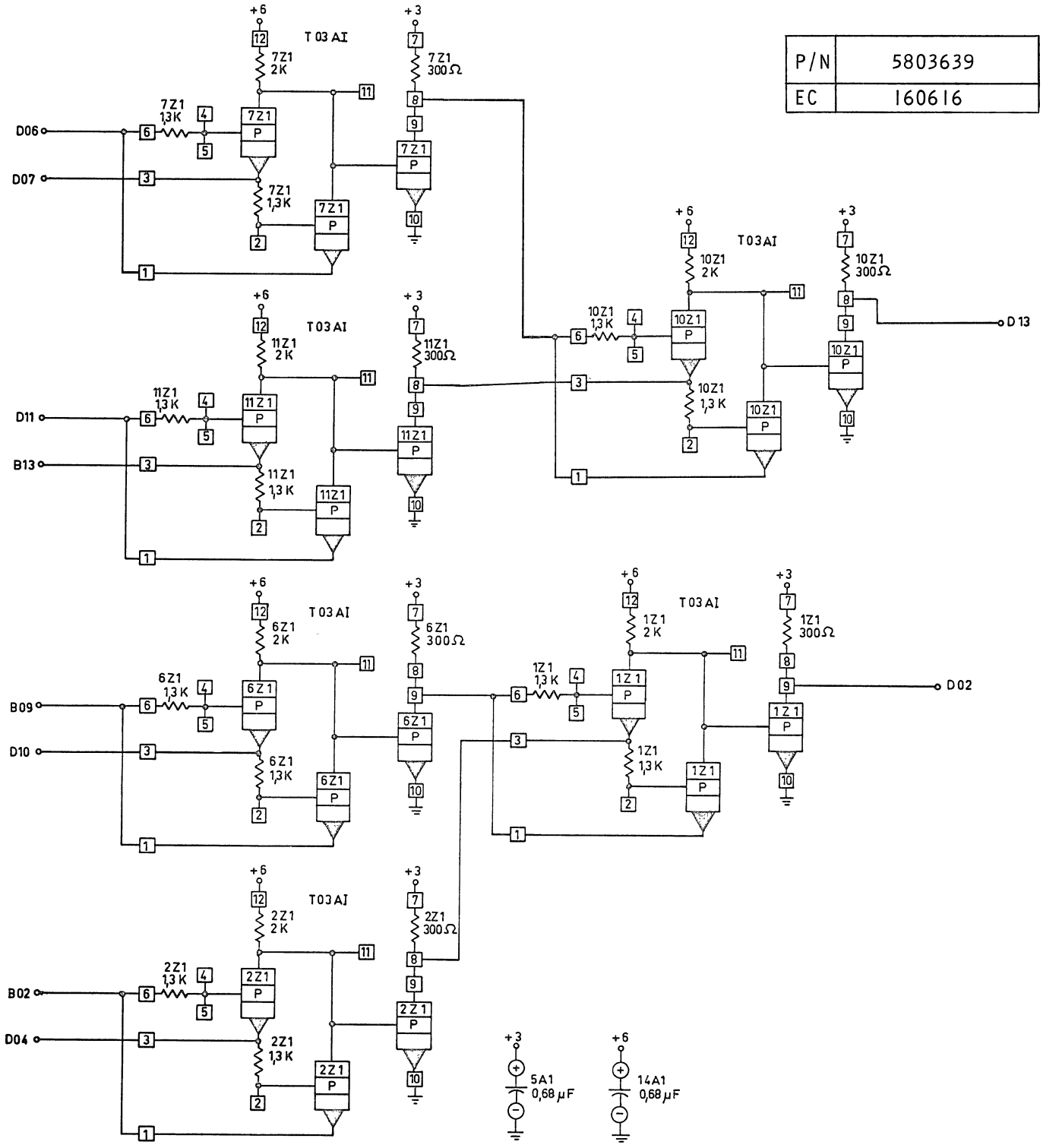
XOR CARD

T03

P/N	5803639
EC	160616



P/N	5803639
EC	160616



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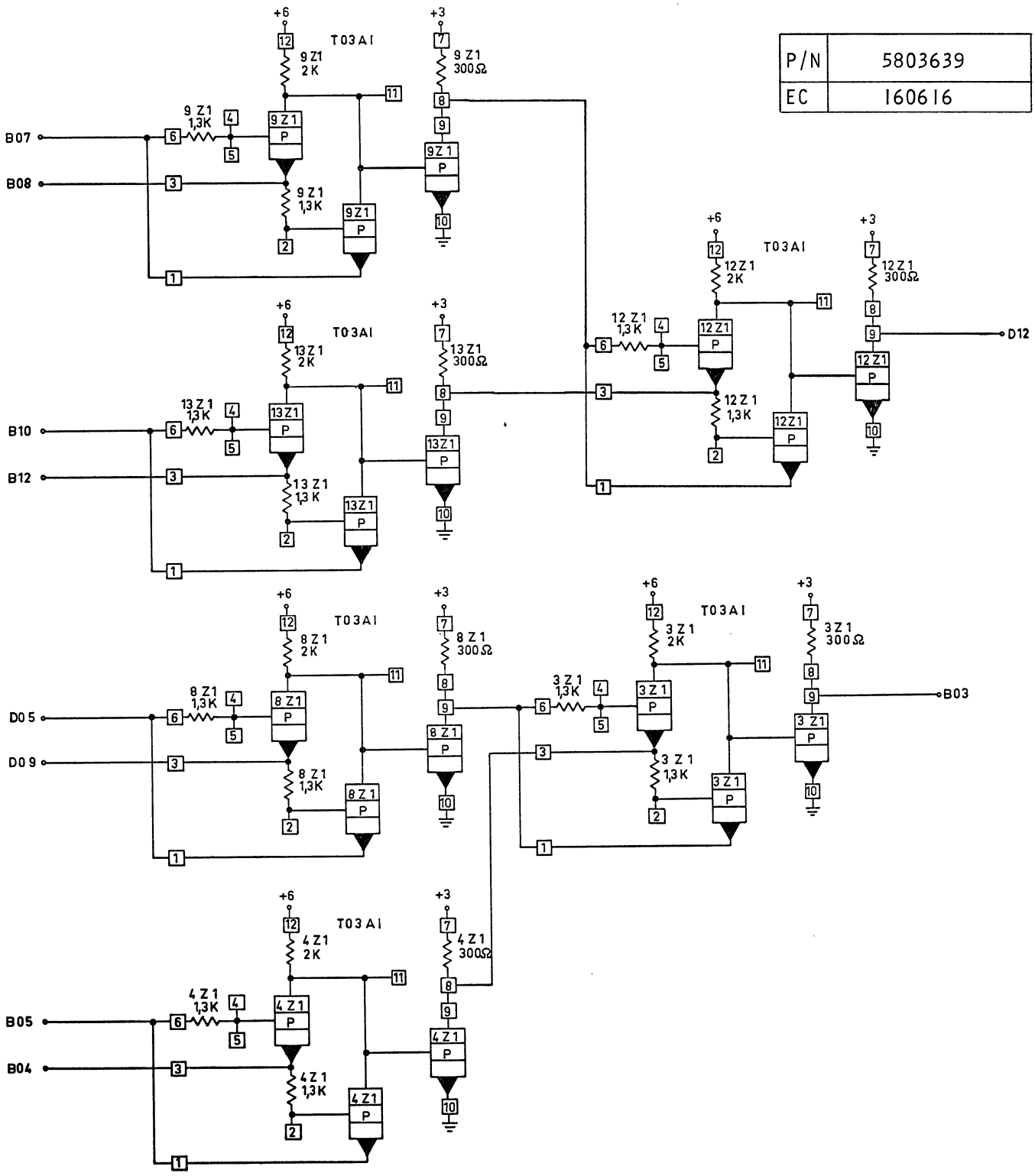
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
XOR CARD

P/N	5803639
EC	160616



POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

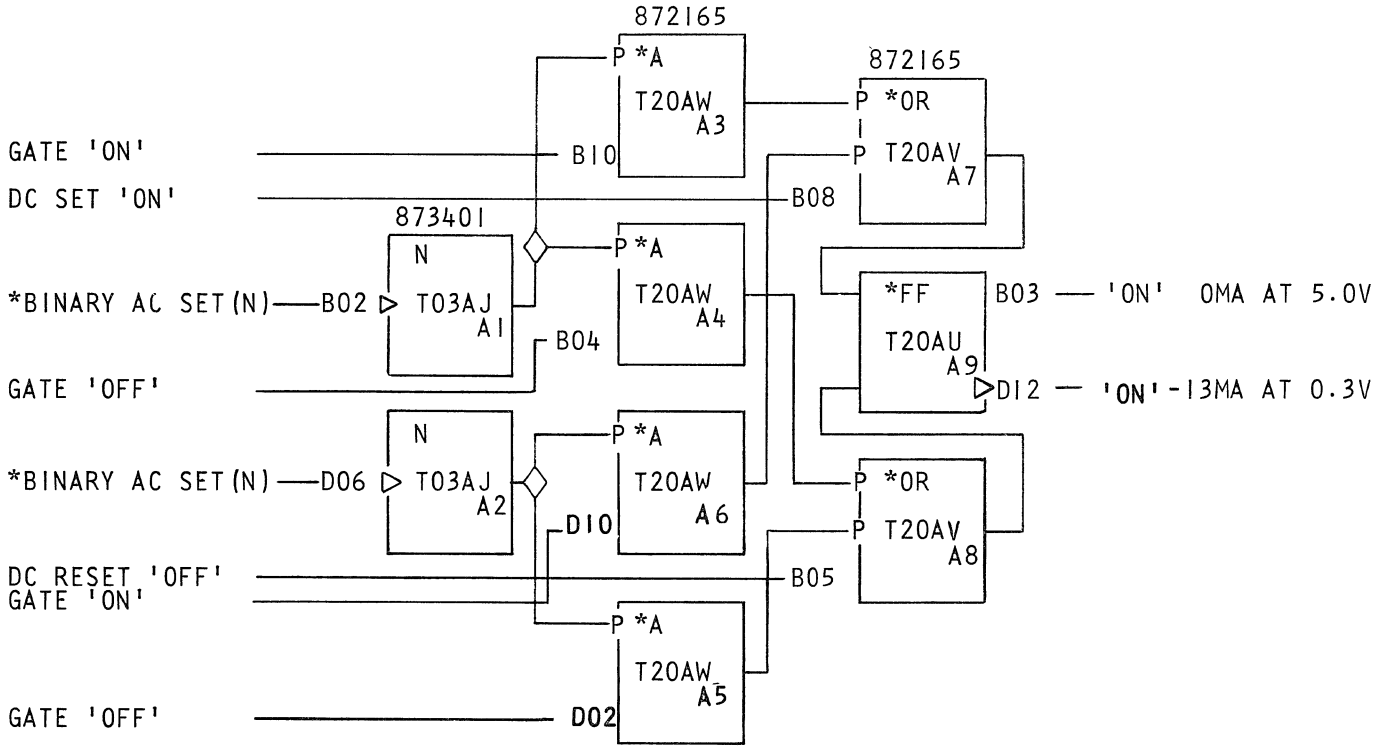
2-BINARY AC TRIGGERS

CATEGORY CODE

T20

P/N	5803683
EC	162051 *
STANDARD RESTRICTED	
CARD SIZE	1-12

(EC in process)



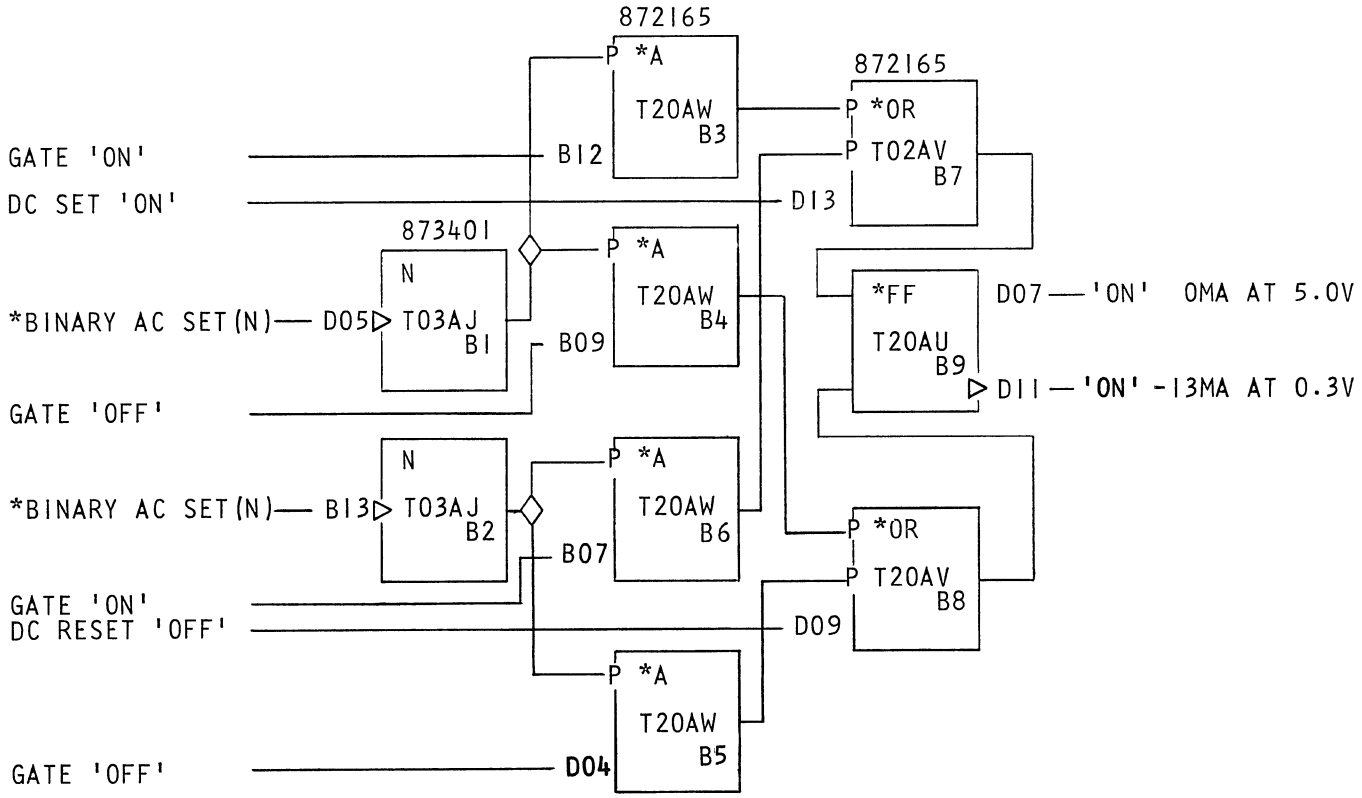
* DRIVE RULES SEE CIRCUIT SPECIFICATION 873415

NOTE: A C SETS AND RESETS ARE INTERNALLY GATED BY THE OUTPUTS OF THE TRIGGER.

2-BINARY AC TRIGGERS

P/N	5803683
EC	162051 *

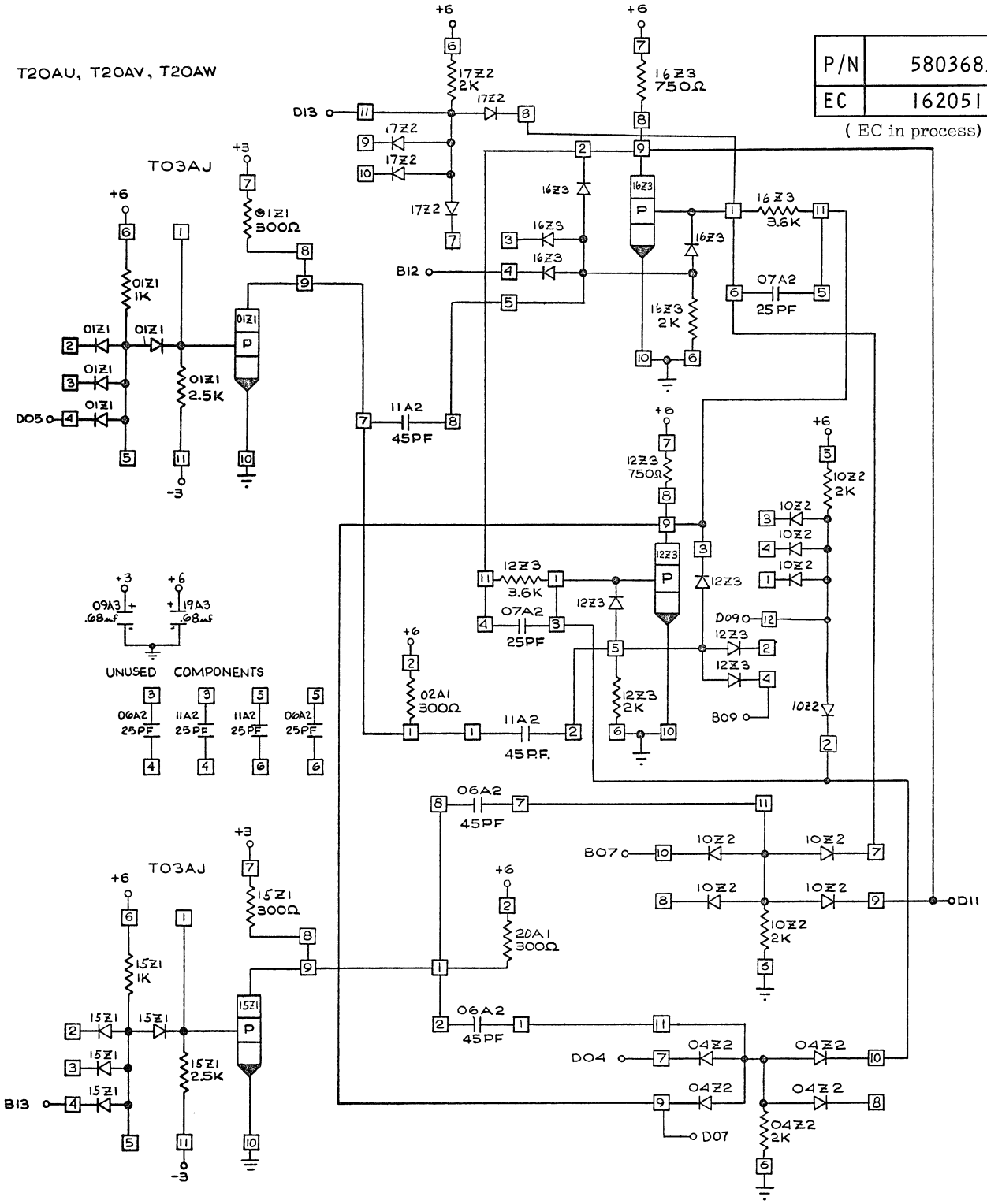
(EC in process)



NOTE: A C SETS AND RESETS ARE INTERNALLY GATED BY THE OUTPUT OF THE TRIGGER.

P/N	5803683
EC	162051 *

(EC in process)



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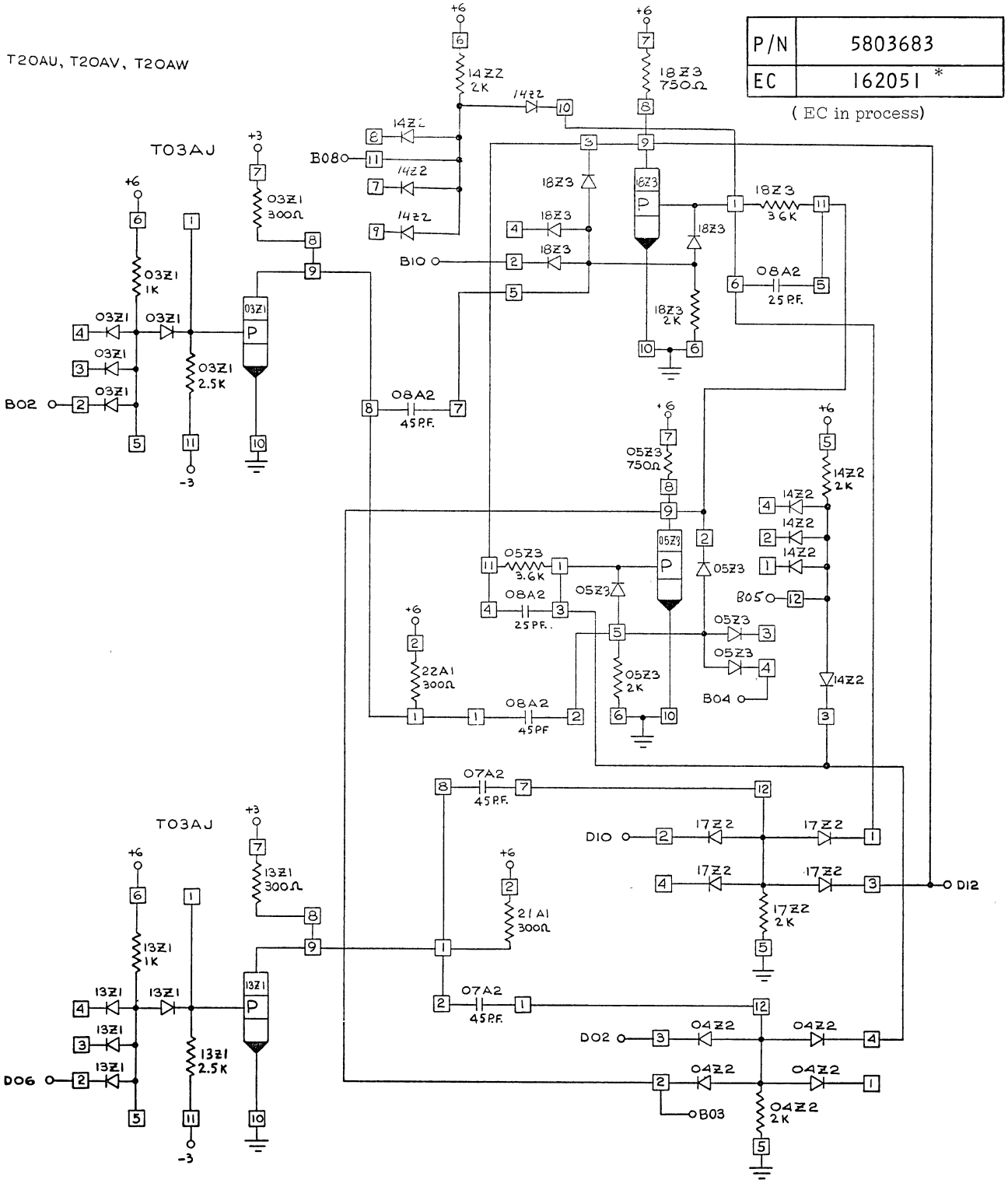
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-BINARY AC TRIGGERS

P/N	5803683
EC	162051 *

(EC in process)

T20AU, T20AV, T20AW



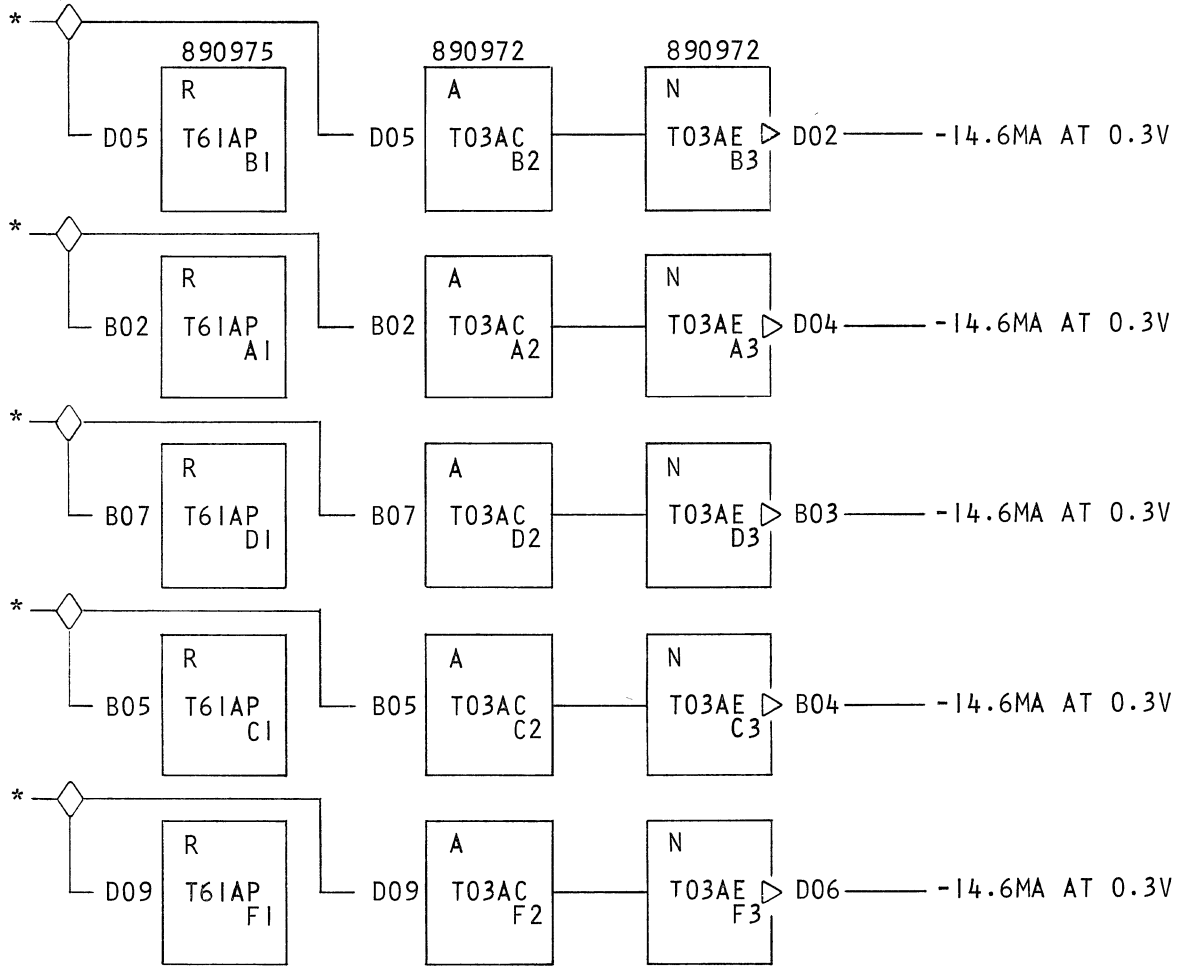
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

IO LINE TERMINATORS

CATEGORY CODE

T03	T61

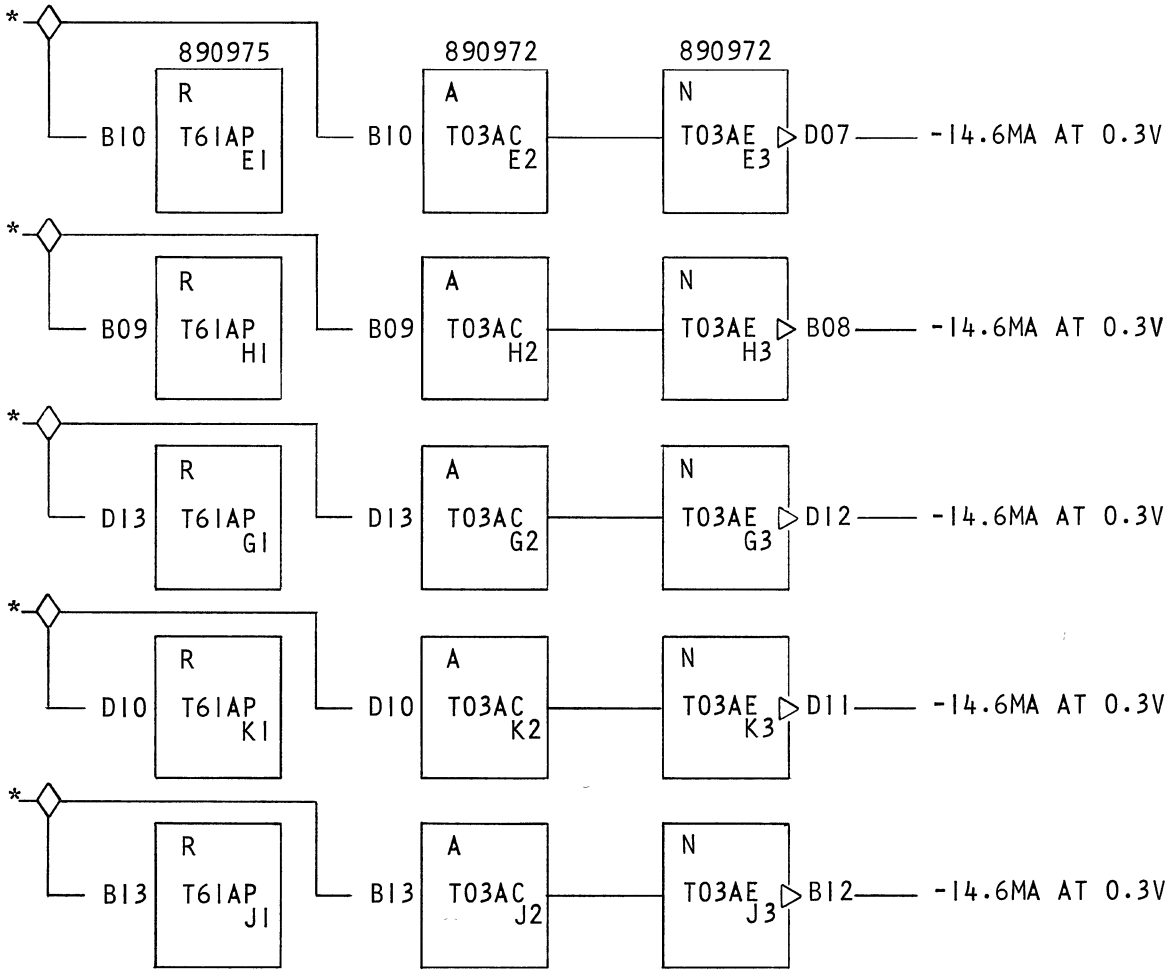
P/N	5803685
EC	162033
STANDARD RESTRICTED	
CARD SIZE	1-12



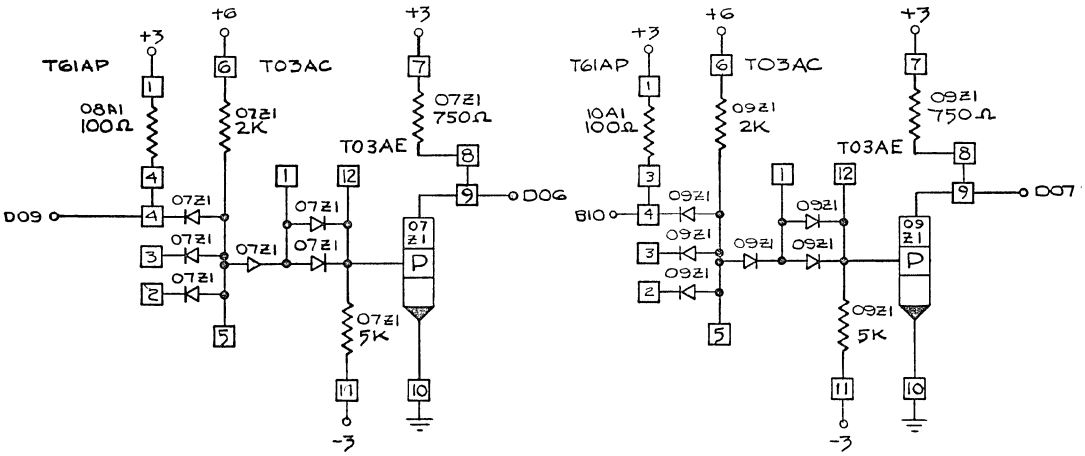
*SEE SPEC 890975 FOR SPECIAL INPUT CHARACTERISTICS

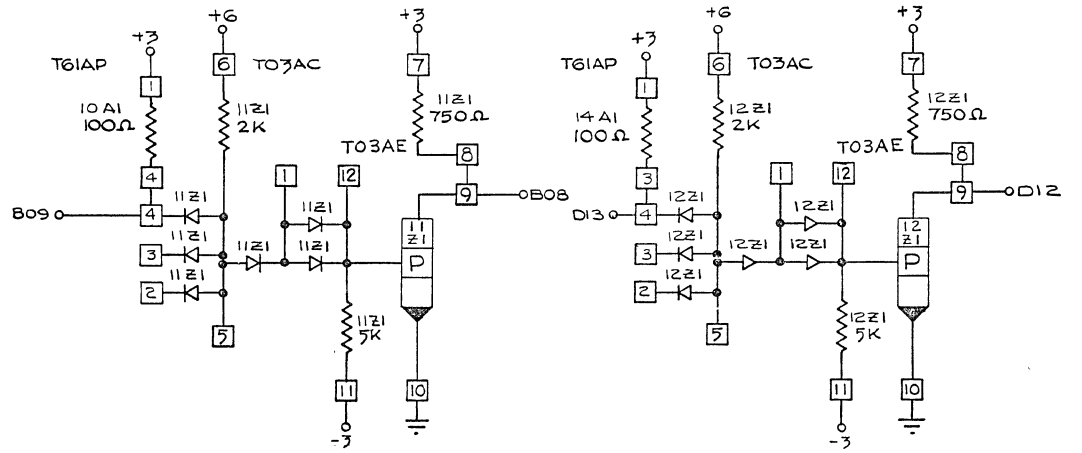
IO LINE TERMINATORS	
T03	T61

P/N	5803685
EC	162033



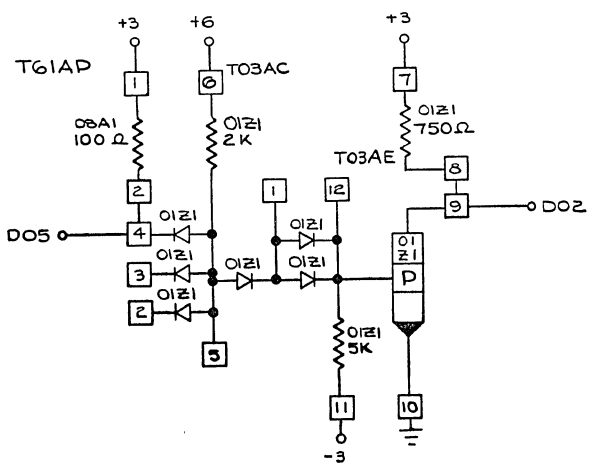
P/N	5803685
EC	162033

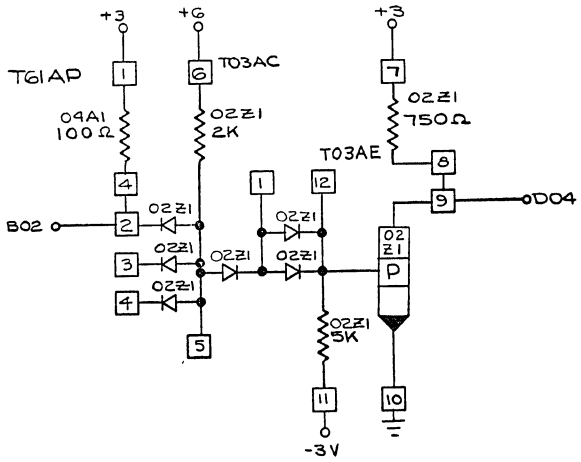


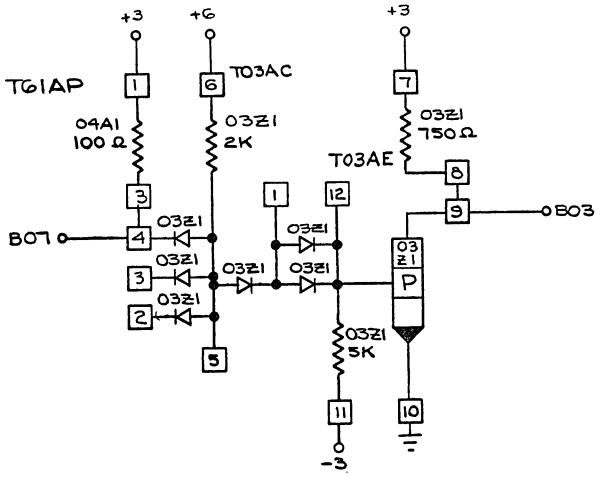


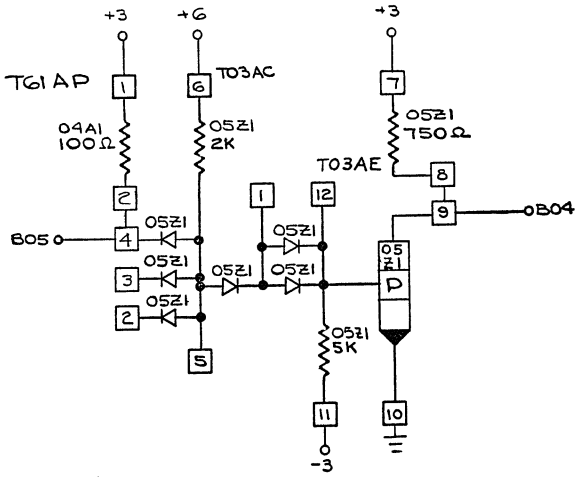
LMH Cat.	0-2860 Subject	364 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 10 LINE TERMINATORS

P/N	5803685
EC	162033



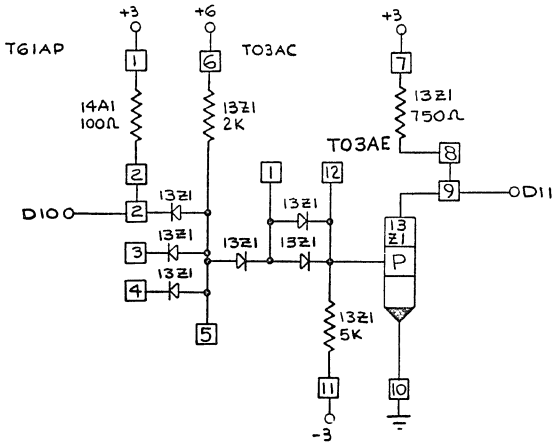


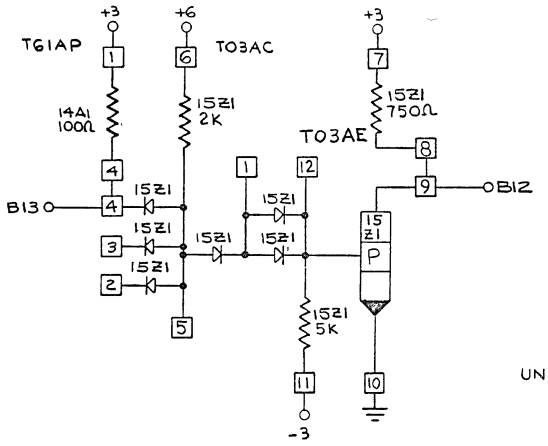


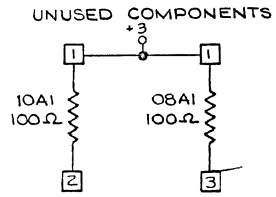


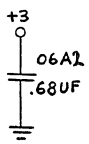
4 OF 5 Page	1-67 Date	

P/N	5803685
EC	162033









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POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

IO API'S

CATEGORY CODE

T03

P/N	5803686
EC	162034
STANDARD RESTRICTED	
CARD SIZE	1-12

873401

+5MA AT 0.3V — D04 — N T03AJ A1 — D02 — -23MA AT 0.3V

873401

+5MA AT 0.3V — B05 — N T03AJ B1 — B03 — -23MA AT 0.3V

+5MA AT 0.3V — B04 — N T03AJ C1 — B02 — -23MA AT 0.3V

+5MA AT 0.3V — D05 — N T03AJ D1 — D10 — -23MA AT 0.3V

+5MA AT 0.3V — D07 — N T03AJ E1 — D09 — -23MA AT 0.3V

+5MA AT 0.3V — B08 — N T03AJ F1 — D06 — -23MA AT 0.3V

+5MA AT 0.3V — B09 — N T03AJ G1 — B07 — -23MA AT 0.3V

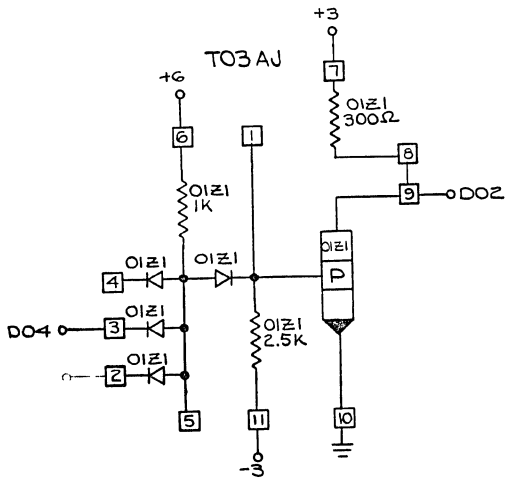
+5MA AT 0.3V — B13 — N T03AJ H1 — D13 — -23MA AT 0.3V

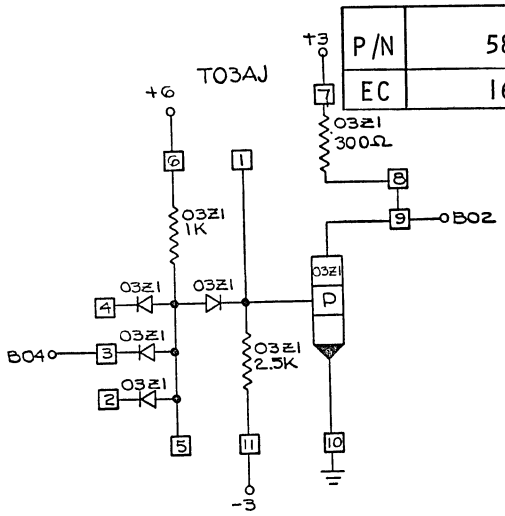
+5MA AT 0.3V — B12B — N T03AJ J1 — D12 — -23MA AT 0.3V

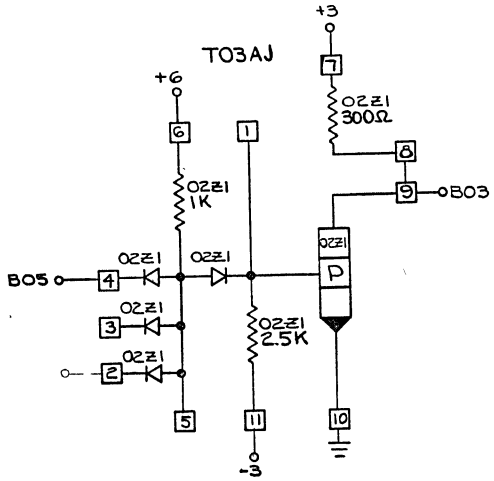
+5MA AT 0.3V — D11 — N T03AJ K1 — B10 — -23MA AT 0.3V

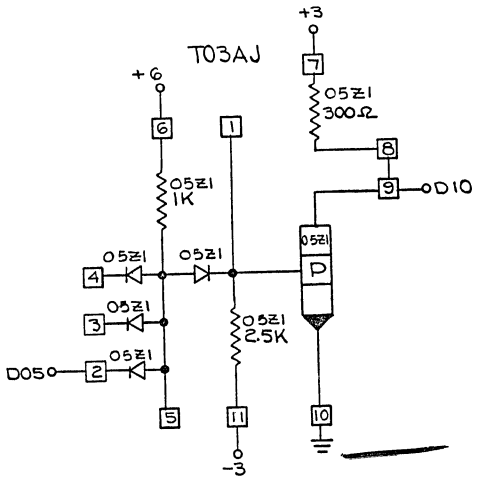
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
10 API'S

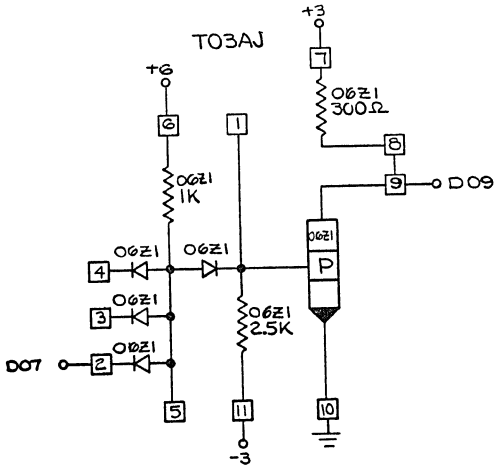
P/N	5803686
EC	162034



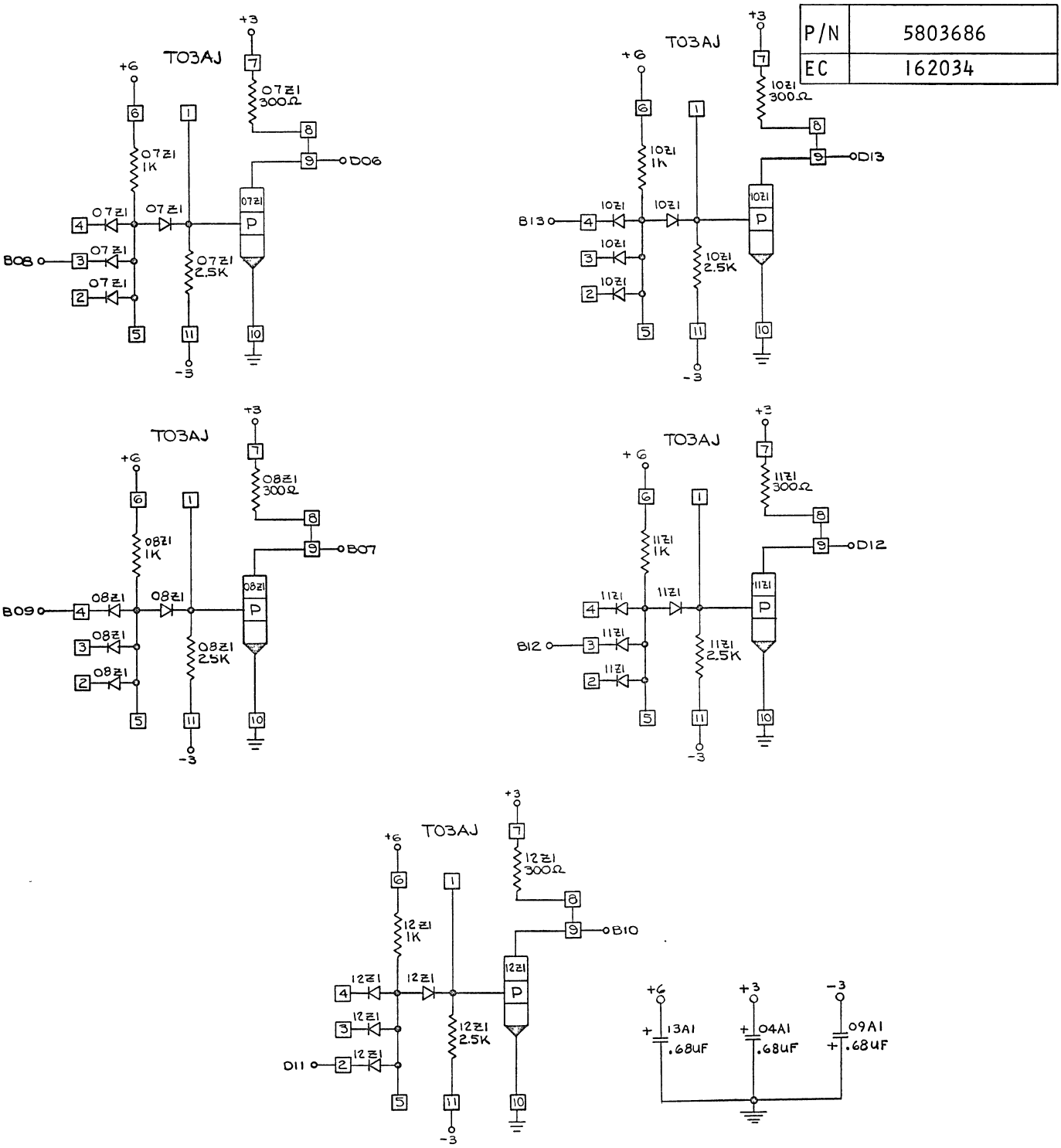








P/N	5803686
EC	162034



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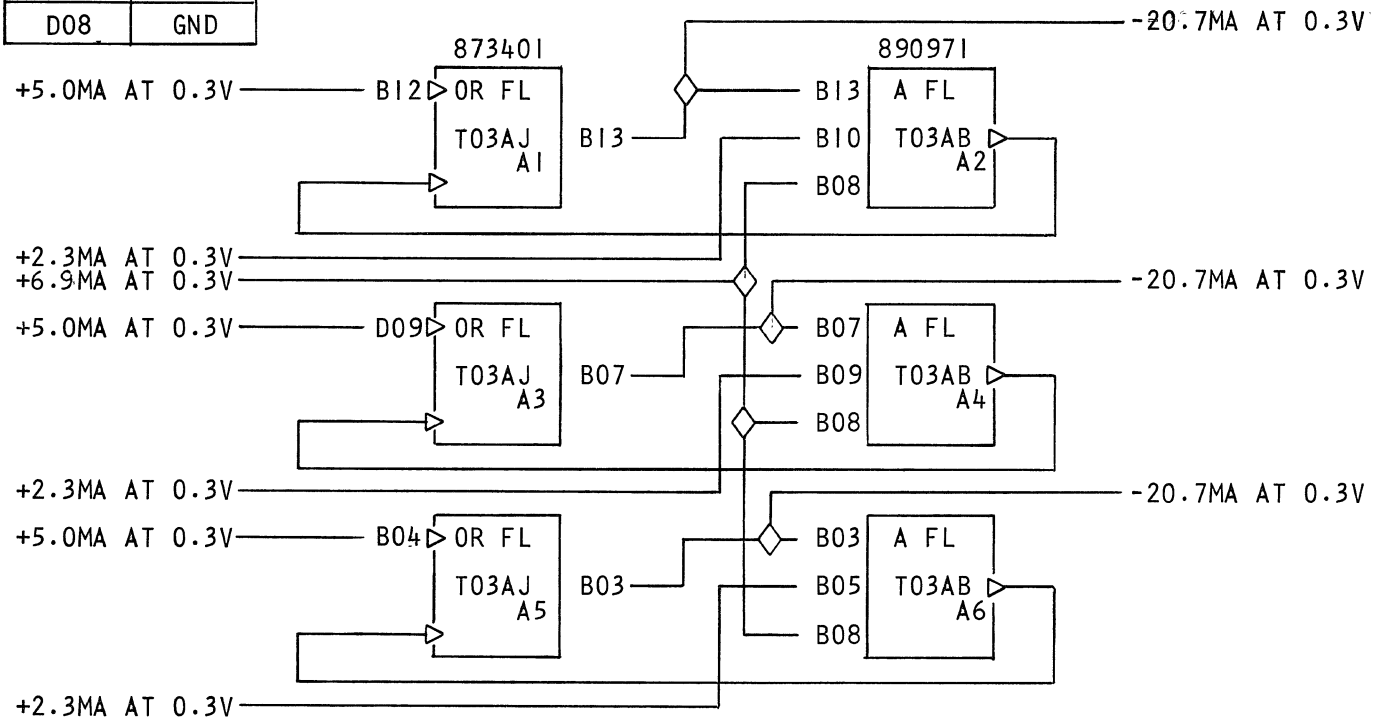
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

6 LATCHES W/API OUTPUT

CATEGORY CODE

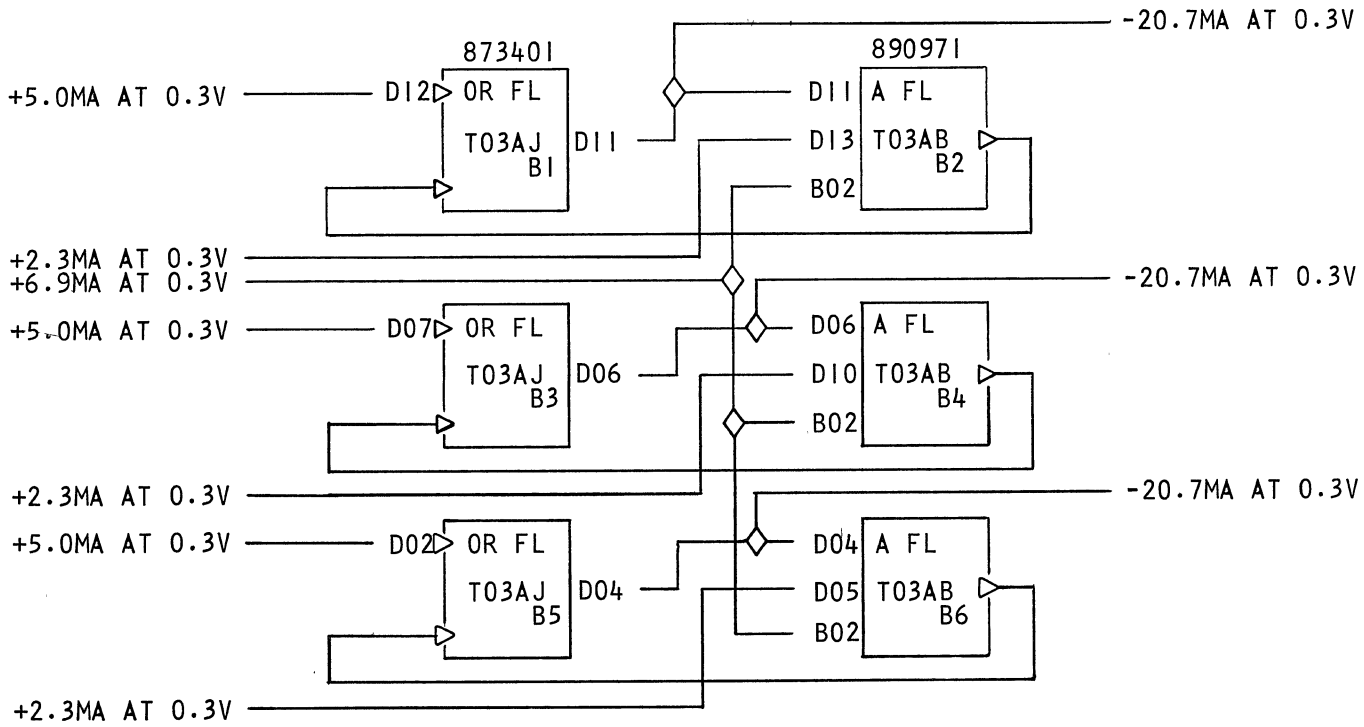
T03

P/N	5803712	
EC	162188	
STANDARD RESTRICTED		
CARD SIZE		1-12

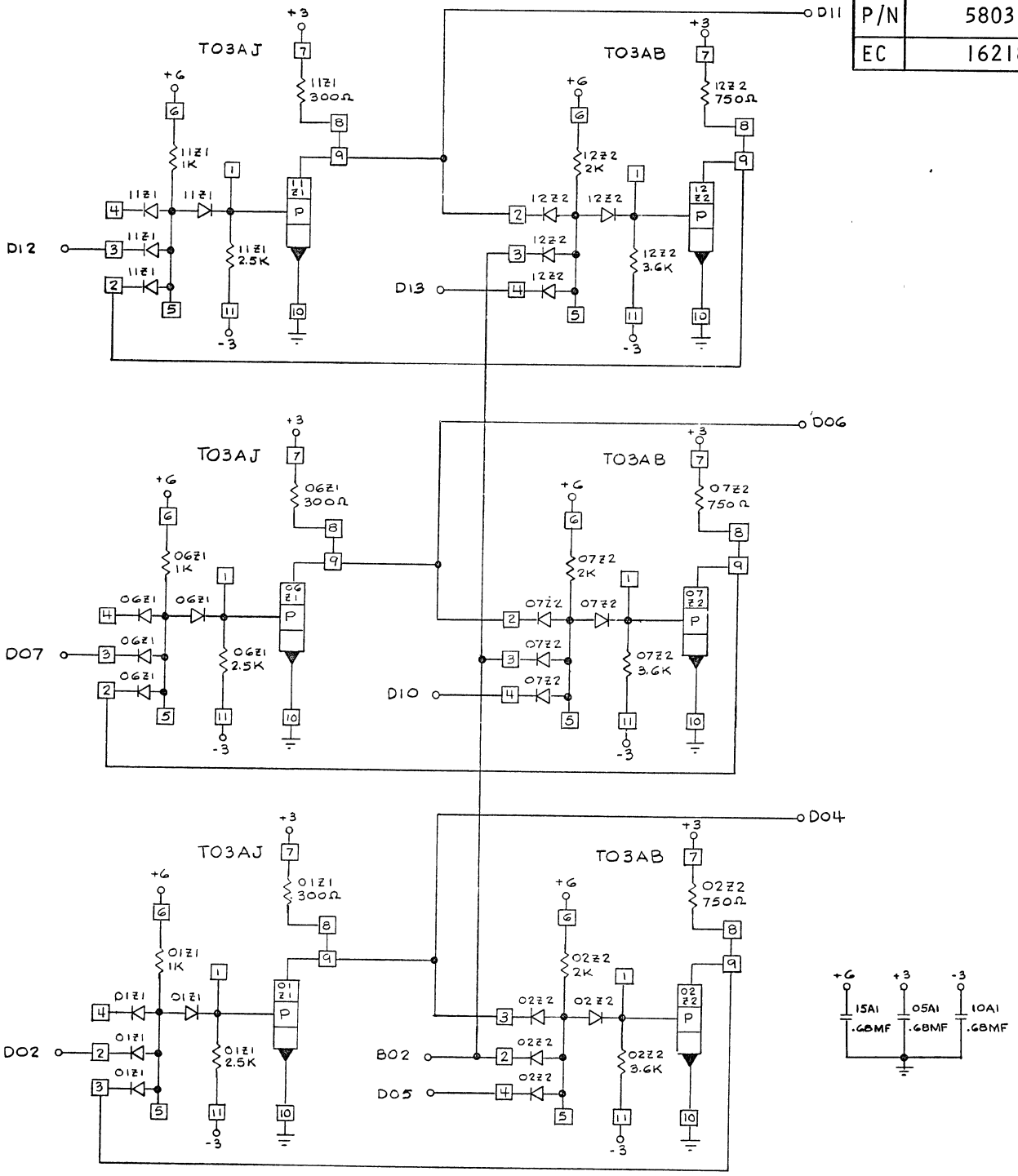


6 LATCHES W/API OUTPUT

P/N	5803712
EC	162188



P/N	5803712
EC	162188

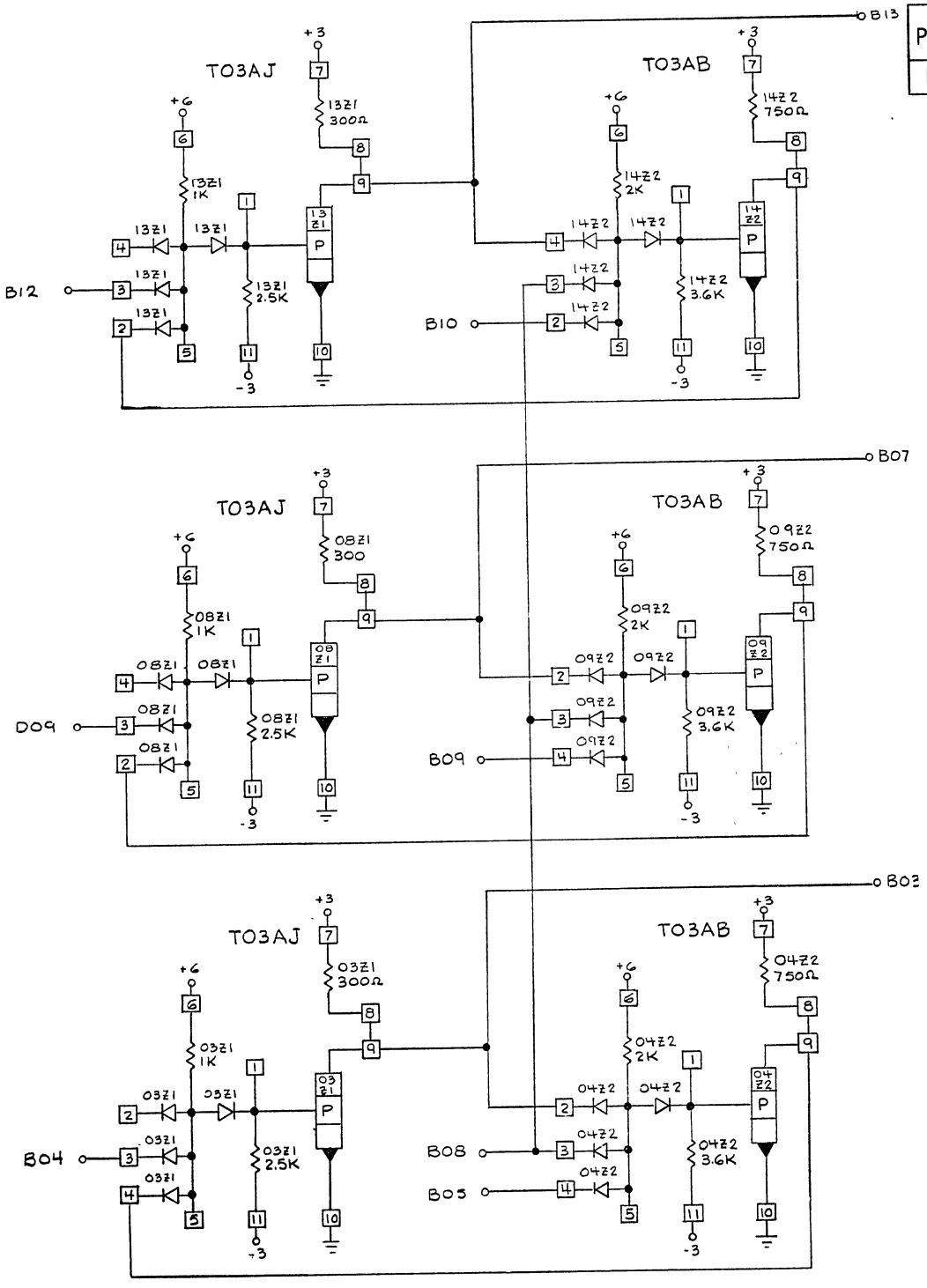


Printed in U.S.A.

LMH Cat.	0-2860 Subject	370 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6 LATCHES W/API OUTPUT

P/N	5803712
EC	162188



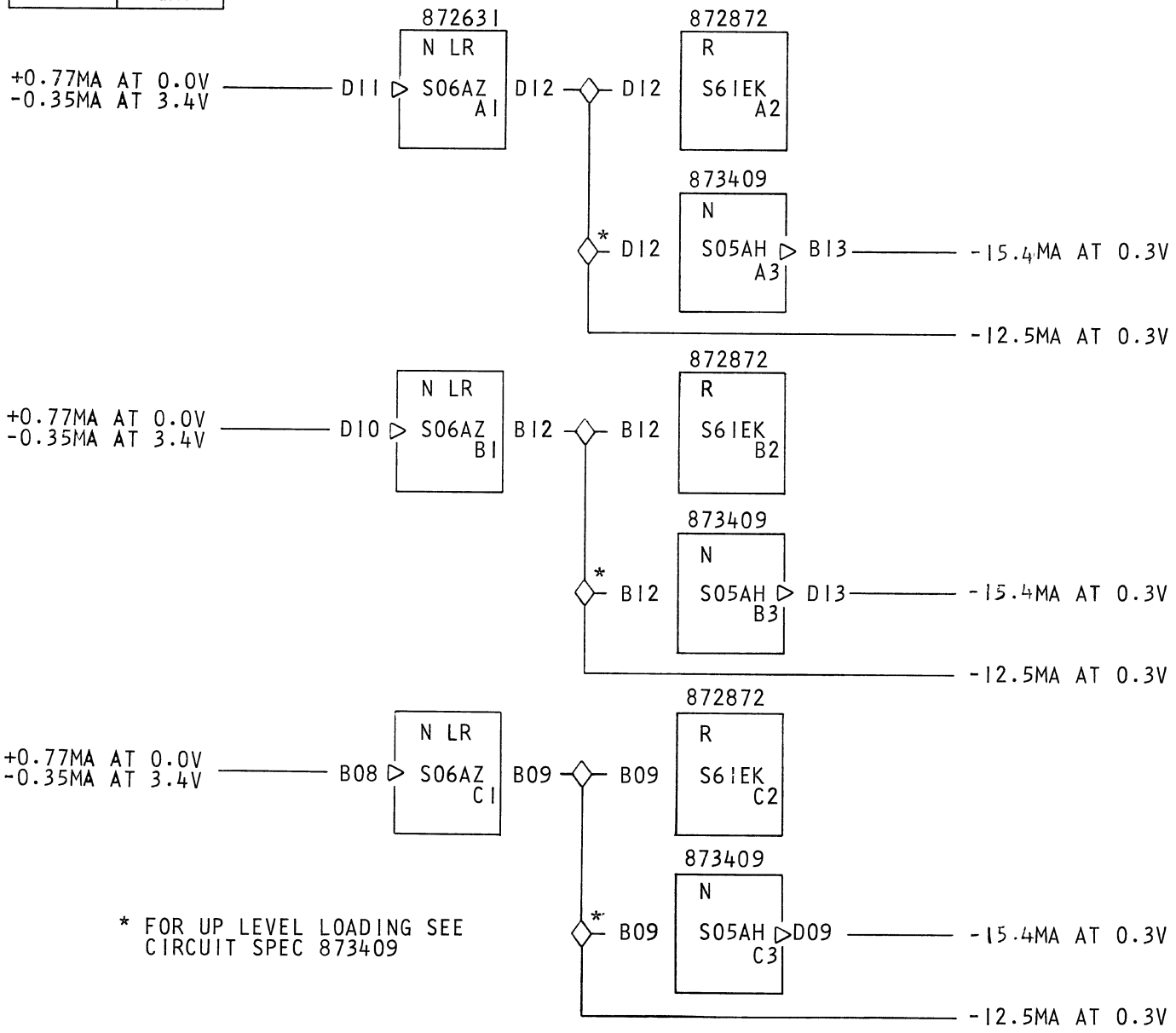
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

6-MULTIPLEX LINE RECEIVERS & INV.

CATEGORY CODE

S06

P/N	5803732
EC	165385B
STANDARD RESTRICTED	
CARD SIZE	1-12

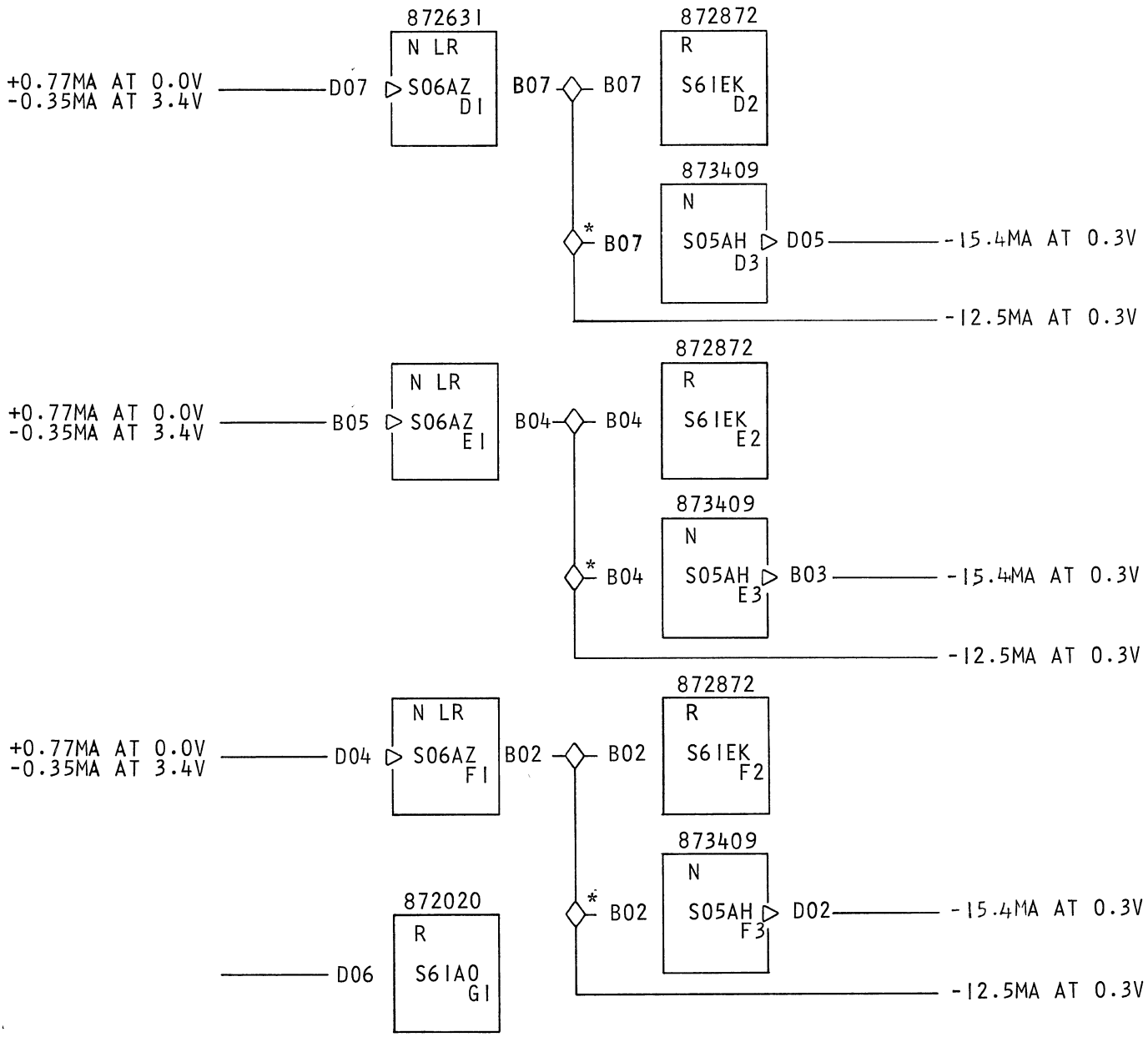


* FOR UP LEVEL LOADING SEE CIRCUIT SPEC 873409

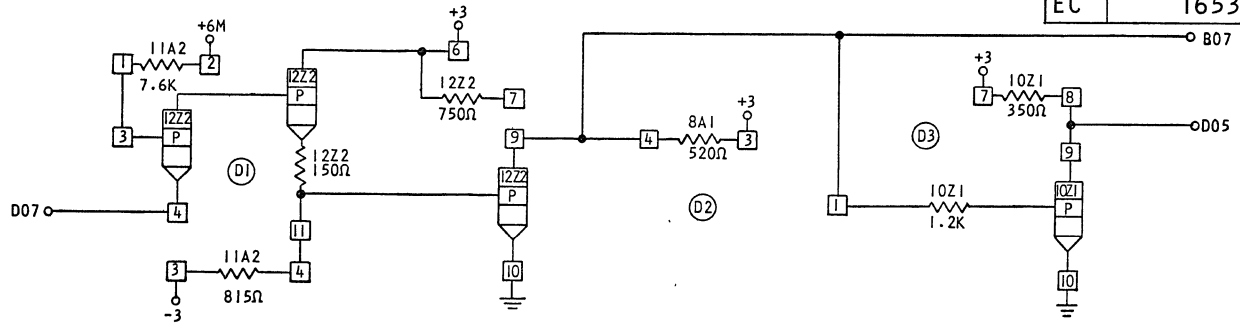
6-MULTIPLEX LINE RECEIVERS & INV.

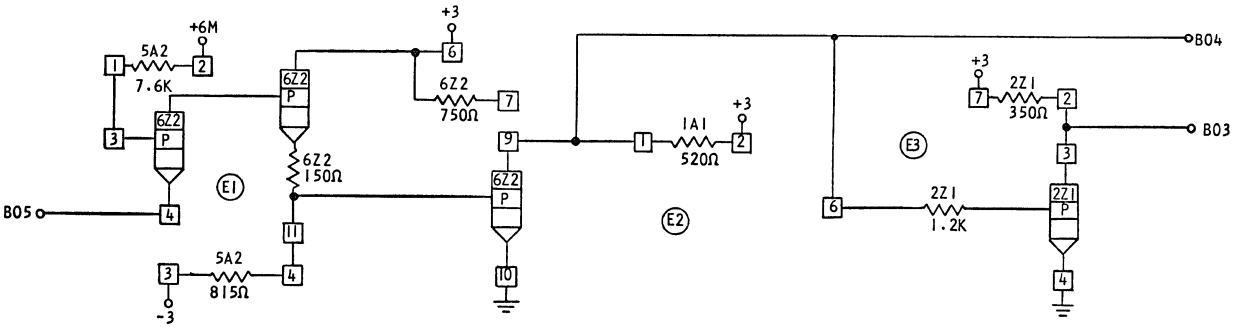
S06

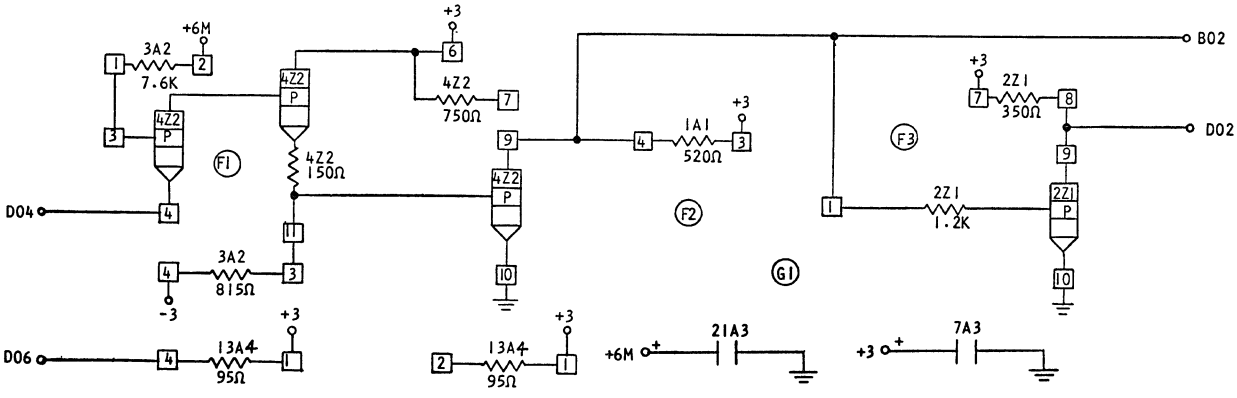
P/N	5803732
EC	165385B



P/N	5803732
EC	165385B

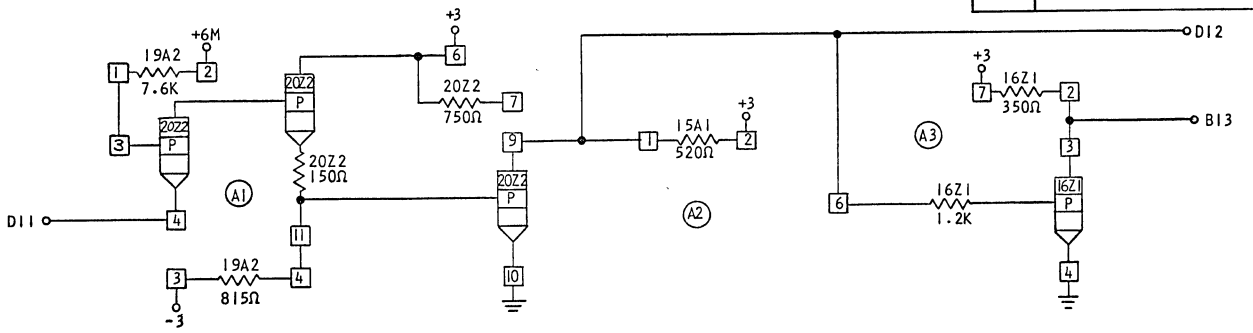


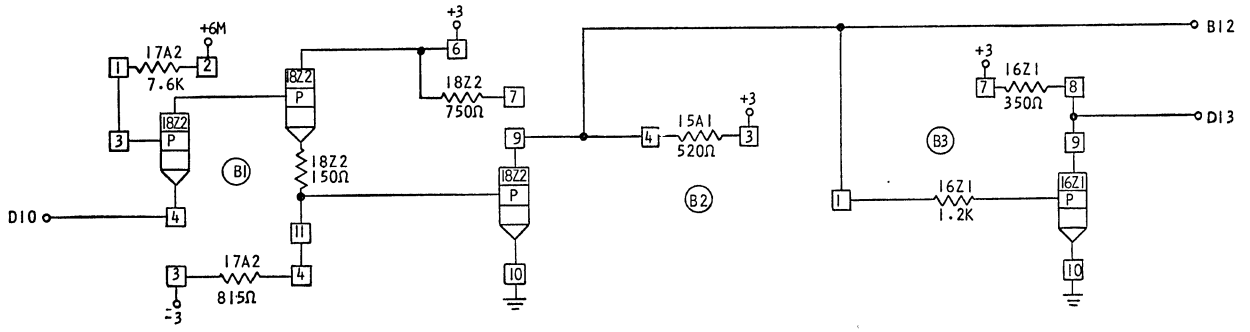


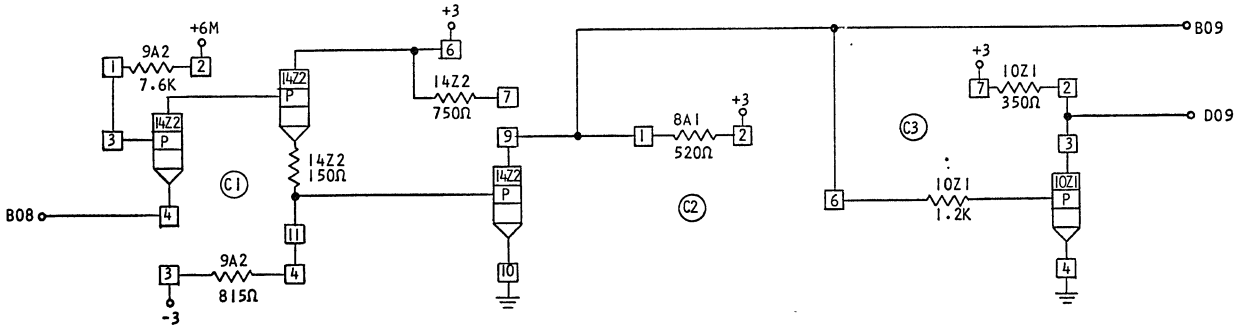


SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6-MULTIPLEX LINE RECEIVERS & INV.

P/N	5803732
EC	165385B







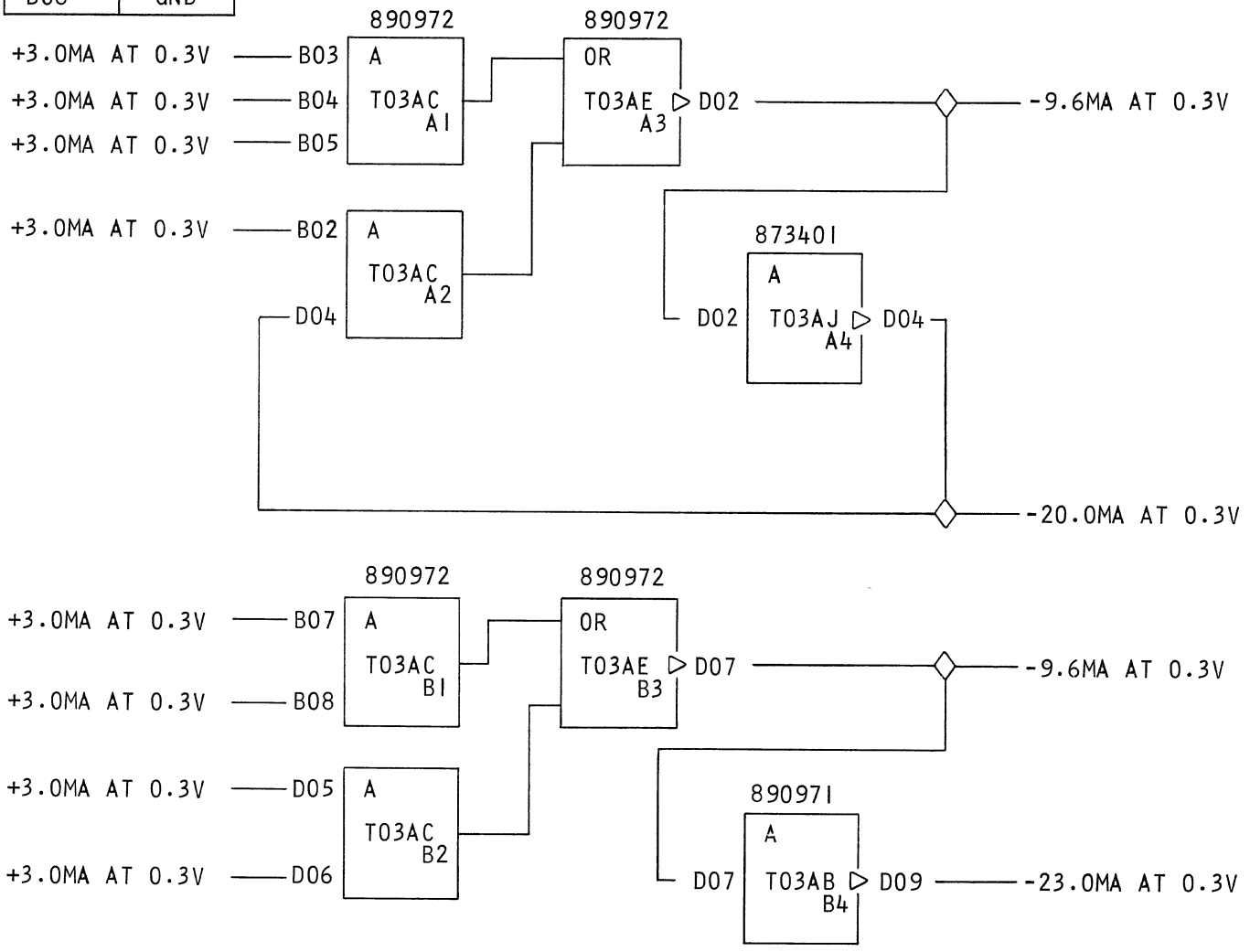
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

GENERAL PURPOSE LTH

CATEGORY CODE

T03

P/N	5803735
EC	161947
SPECIAL RESTRICTIVE	
CARD SIZE	1-12

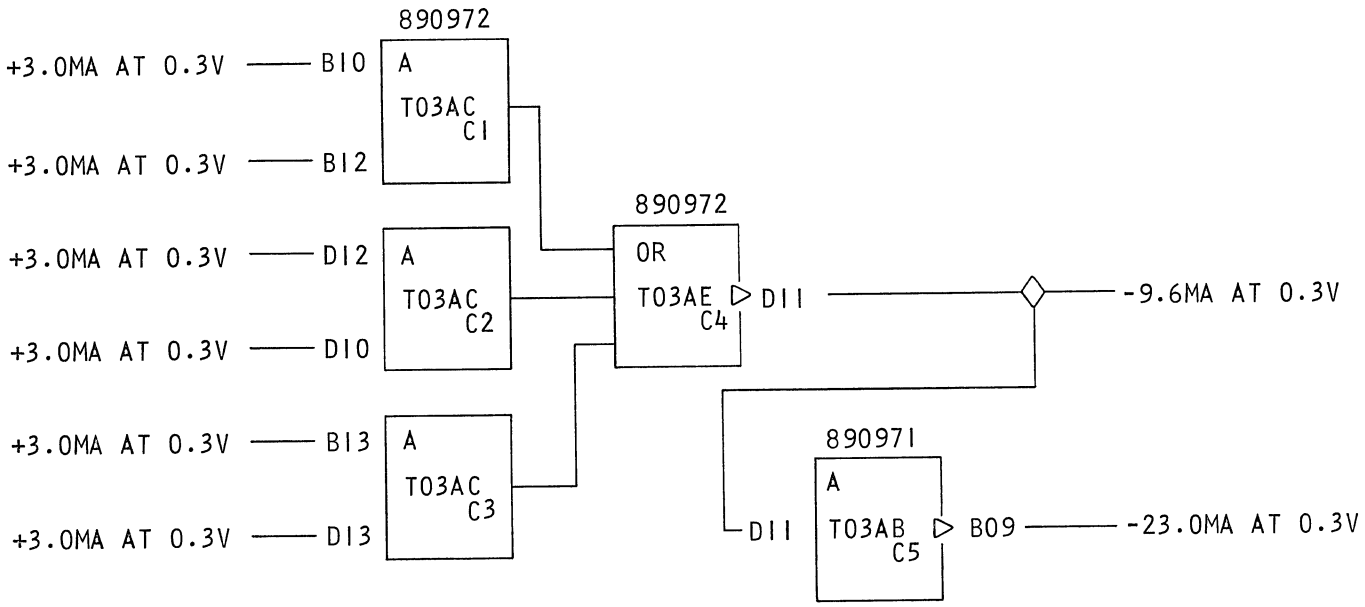


GENERAL PURPOSE LTH

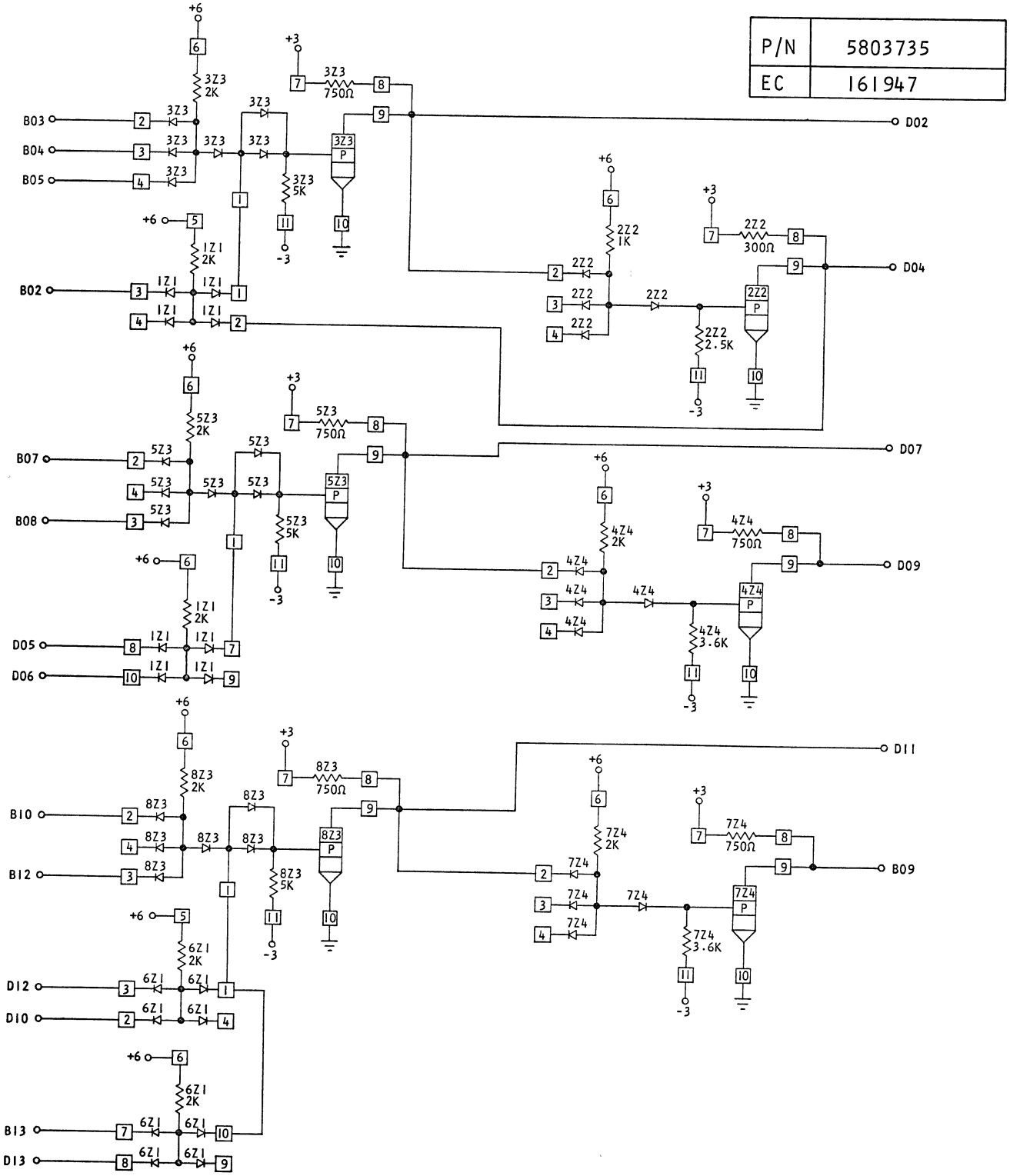
CATEGORY CODE

T03

P/N	5803735
EC	161947



P/N	5803735
EC	161947



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
5-2W COMMON GATED API W0/L,4-2W COMMON GATED API W0/L

LMH	0-2860	377
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

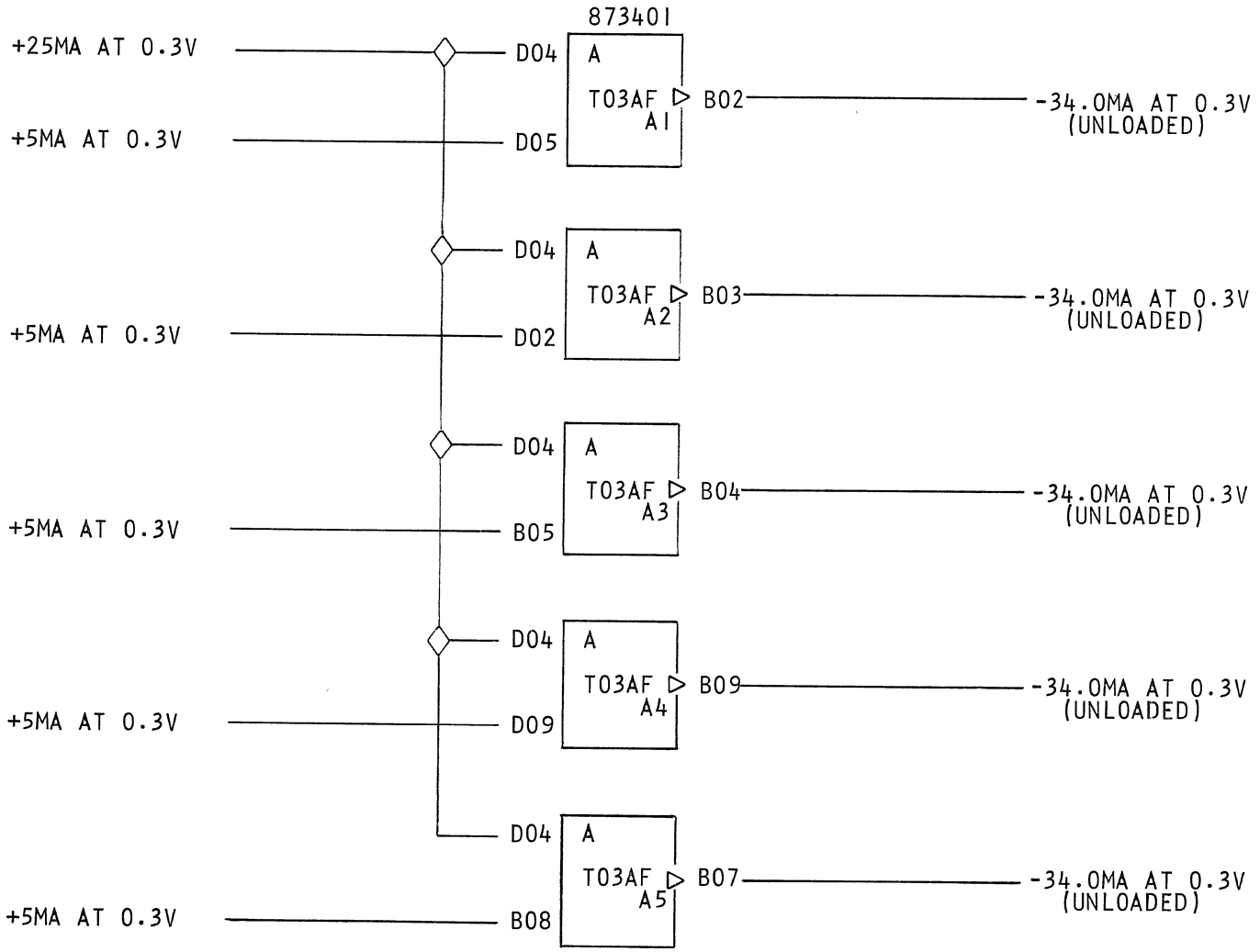
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

5-2W COMMON GATED API W0/L
4-2W COMMON GATED API W0/L

CATEGORY CODE

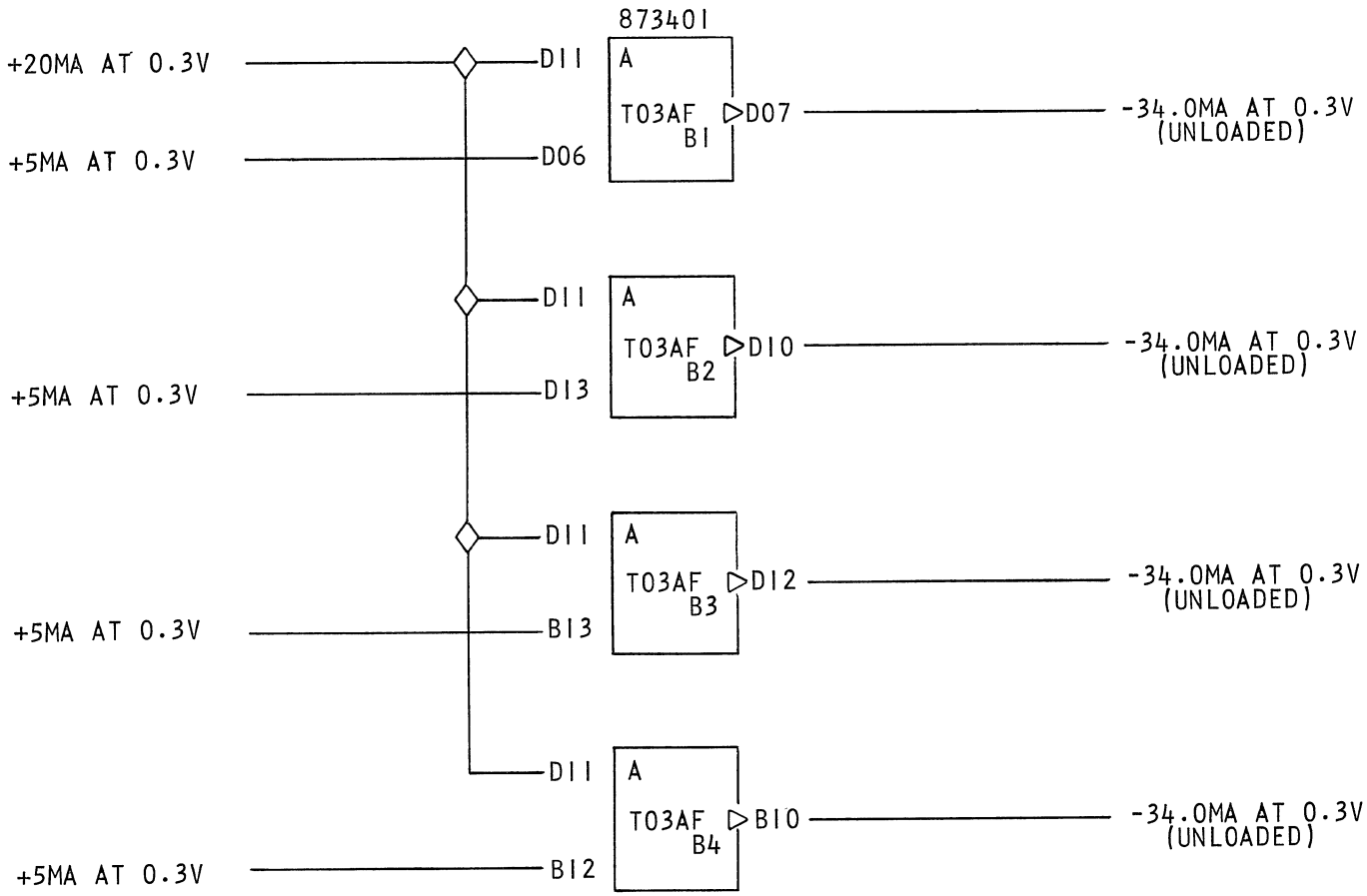
T03

P/N	5803737
EC	161224
SPECIAL	RESTRICTED
CARD SIZE	1-12

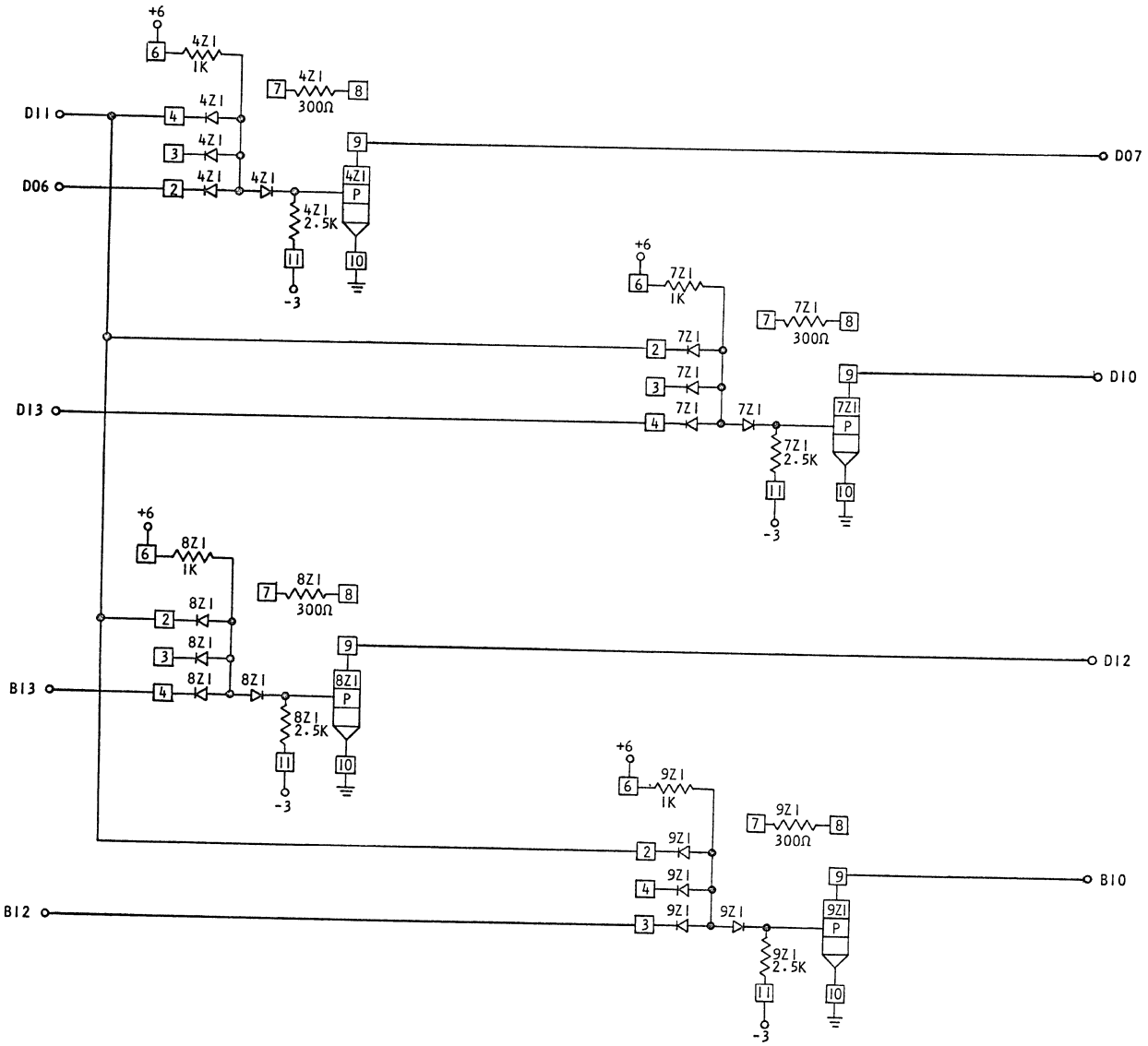


5-2W COMMON GATED API W0/L 4-2W COMMON GATED API W0/L

P/N	5803737
EC	161224

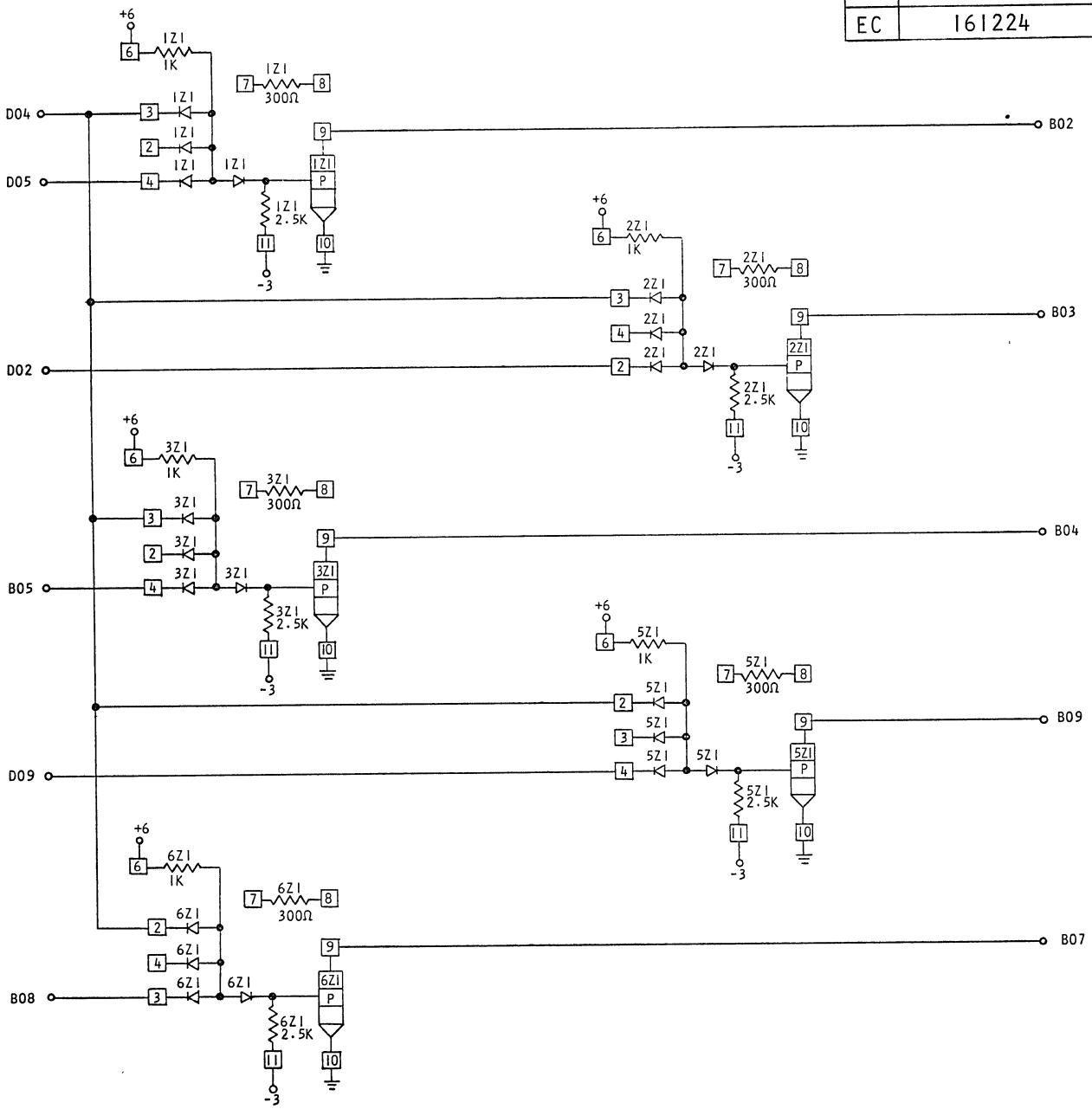


P/N	5803737
EC	161224



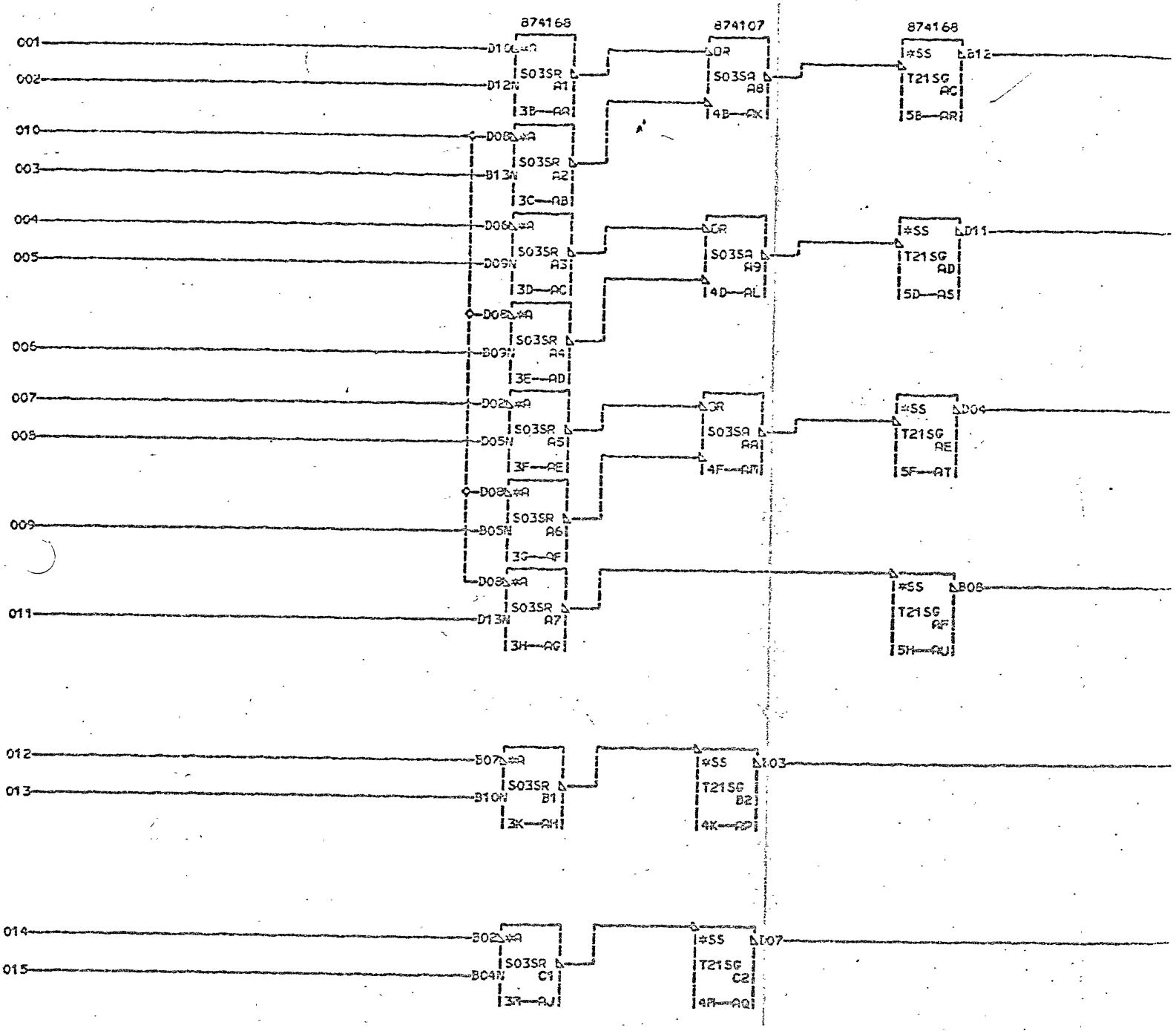
LMH Cat.	0-2860 Subject	377 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 5-2W COMMON GATED API W0/L, 4-2W COMMON GATED API W0/L

P/N	5803737
EC	161224



Page	Date
4	Jan. 67

3757


874168
874107
874168
001
002
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003
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008
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011
012
013
014
015
D10
D12N
D08
B13N
D06
D09N
D09
B09N
D02
D05N
D08
B05N
D08
D13N
B07
B10N
B02
B04N
S03SR
A1
3B
AA
OR
S03SA
A8
4B
AK
*SS
T21SG
AC
5B
AR
B12
A2
3C
AB
A3
3D
AC
A9
4D
AL
AD
5D
AS
D11
A4
3E
AD
A5
3F
AE
AA
4F
AM
AE
5F
AT
D04
A6
3G
AF
A7
3H
AG
AF
5H
AU
B08
B1
3K
AH
B2
4K
AP
B03
C1
3R
AJ
C2
4R
AQ
B07

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
300 MA DRIVER

LMH Cat.	0-2860 Subject	379 Suffix

IBM **Location Manufacturing Specification**

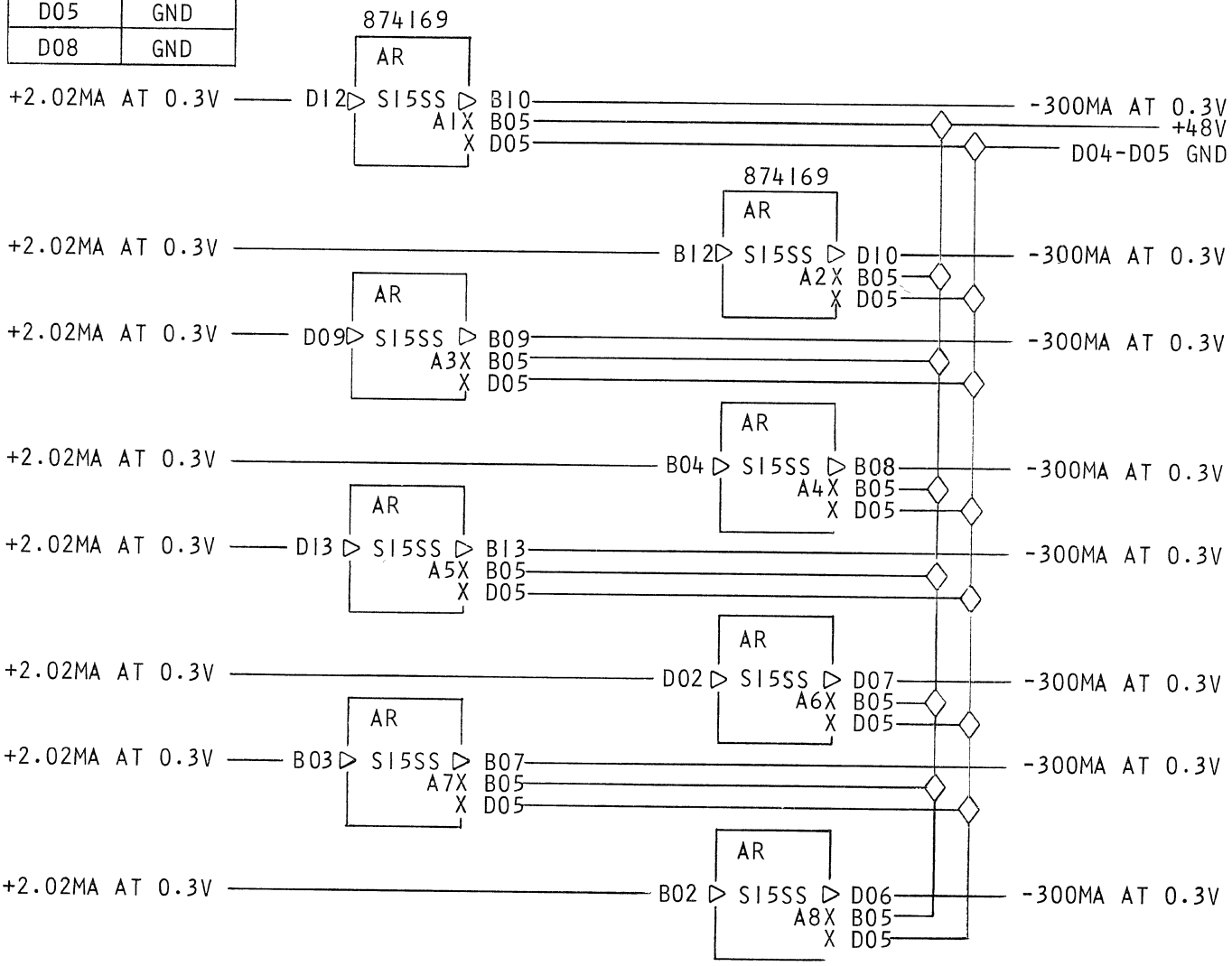
POWER REQUIRED	
PIN	VOLTS
B05	+48
B11	+6
D03	+3
D04	GND
D05	GND
D08	GND

300 MA DRIVER

CATEGORY CODE

SI5

P/N	5803819	
EC	163291A	
SPECIAL RESTRICTED		
CARD SIZE		1-12



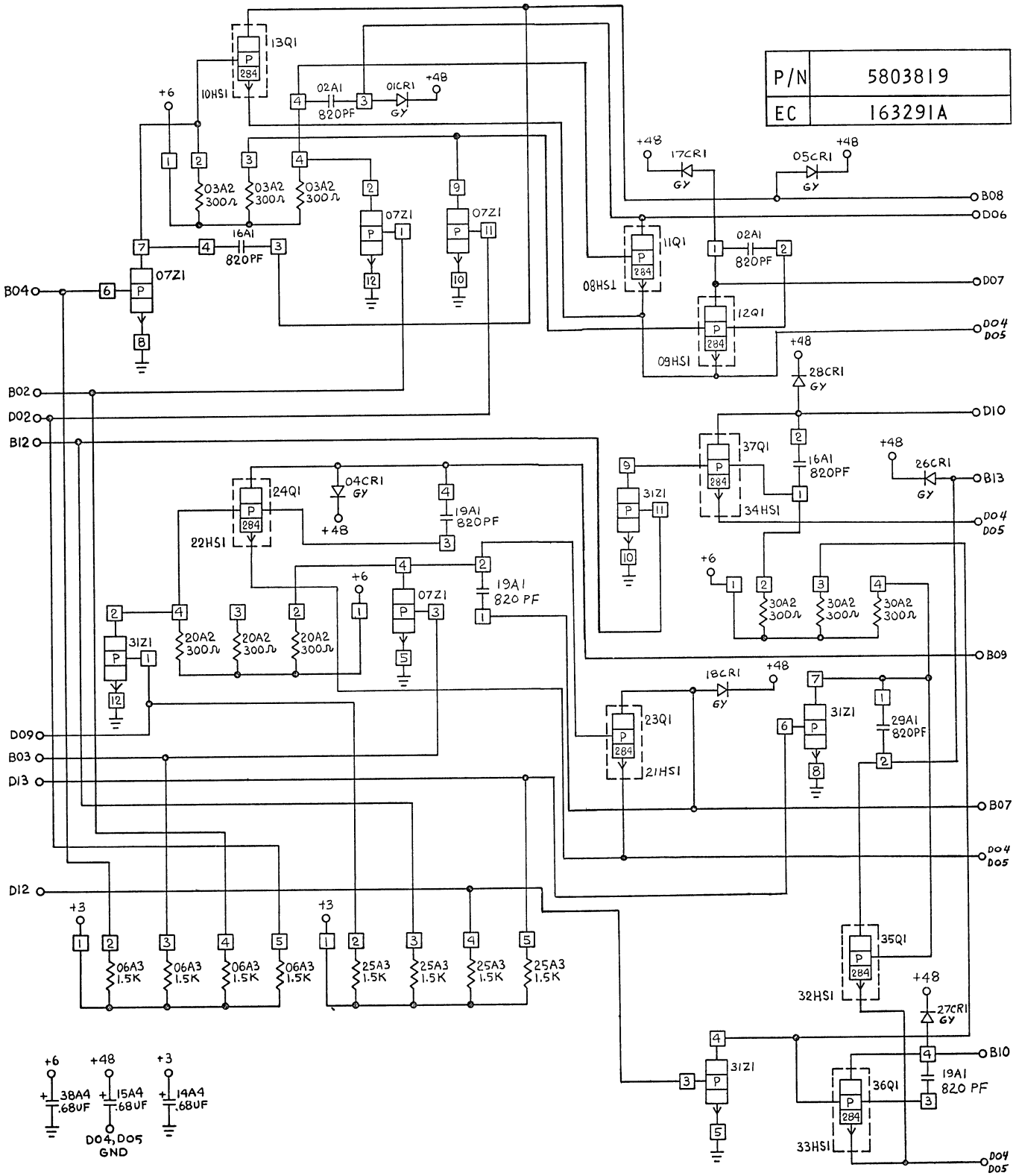
06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		Responsibility: ENDICOTT	Date: 1-67	Page: 1 OF 2

PRINTED IN USA

LMH Cat.	0-2860 Subject	379 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
300 MA DRIVER

P/N	5803819
EC	163291A



2 OF 2 Page	1-67 Date

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1.44MHZ OSCILLATOR

LMH	0-2860	380
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B02	+12
B03	-12
B06	-3
D03	+3
D08	GND

1.44MHZ OSCILLATOR

CATEGORY CODE

S22

P/N	5803835	
EC	162354A	
STANDARD ACTIVE		
CARD SIZE		1-12

872004

OSC

S22AL
A1

B05 ——— -18.5MA AT 0.3V

TD04 ——— TEST POINT ONLY

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		ENDICOTT Responsibility	1-67 Date	1 OF 2 Page

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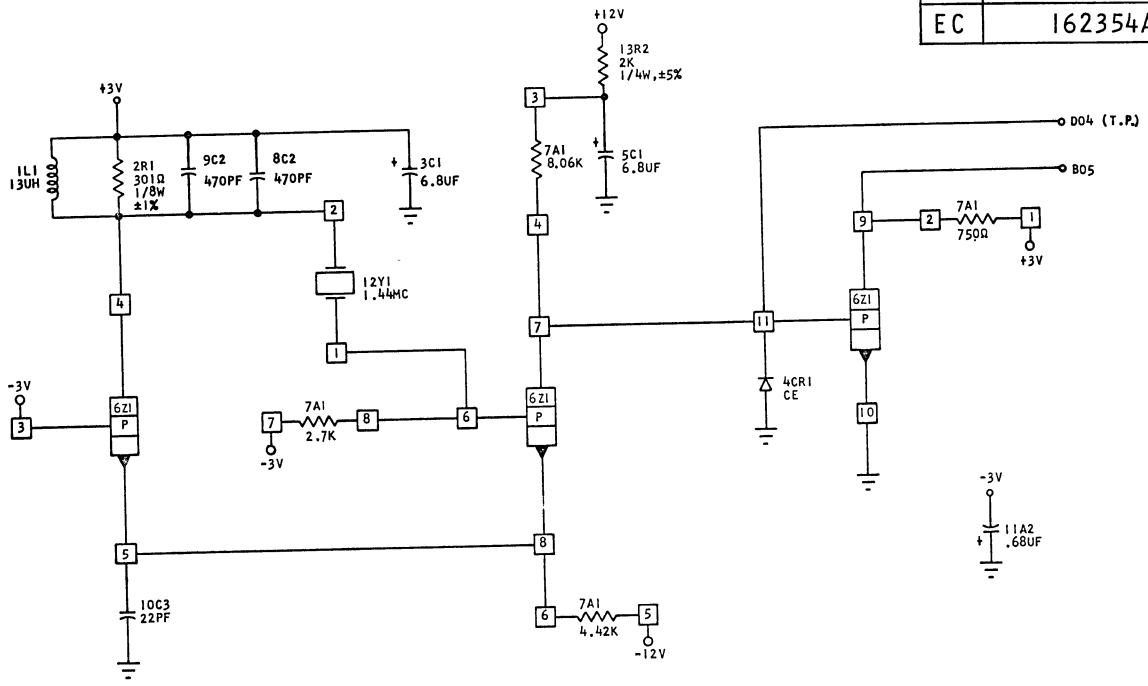
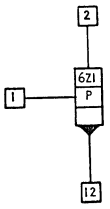
LMH Cat.	O-2860 Subject	380 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1.44MHZ OSCILLATOR

P/N	5803835
EC	162354A





UNUSED COMPONENT

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1.0MHZ OSCILLATOR

LMH	0-2860	381
Cat.	Subject	Suffix

IBM **Location**
Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B02	+12
B03	-12
B06	-3
D03	+3
D08	GND

1.0MHZ OSCILLATOR

CATEGORY CODE

S22

P/N	5803836
EC	162355A
STANDARD ACTIVE	
CARD SIZE	1-12

872003

OSC

S22AK
A1

B05 ——— -18.5MA AT 0.3V

TD04 ——— TEST POINT ONLY

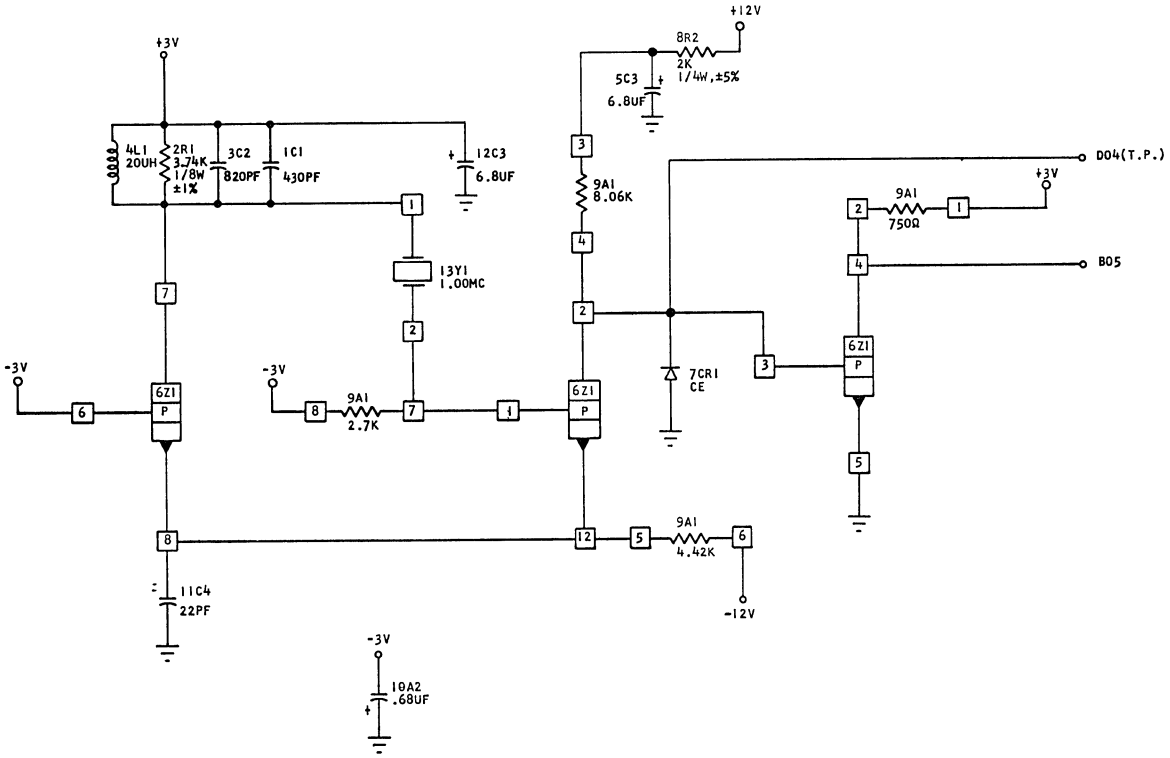
06-09	00-00			
Primary Standards Manual	Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		ENDICOTT Responsibility	1-67 Date	1 OF 2 Page

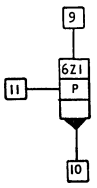
PRINTED IN USA

LMH Cat.	O-2860 Subject	381 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1.0MHZ OCILLATOR

P/N	5803836
EC	162355A





UNUSED COMPONENT

2 OF 2 Page	1-67 Date

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1.0 MHZ GATED OSCILLATOR

LMH	0-2860	382
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

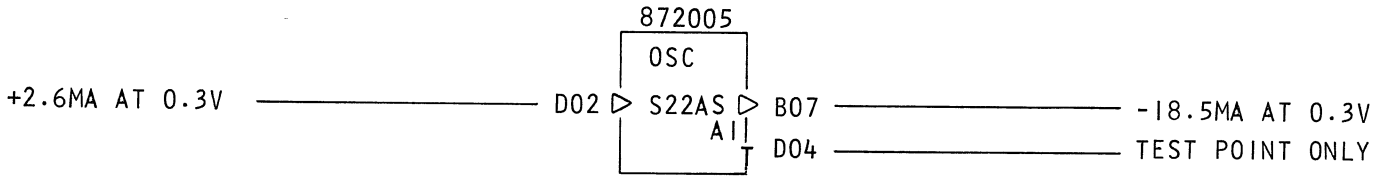
POWER REQUIRED	
PIN	VOLTS
B02	+12
B03	-12
B11	+6
D03	+3
D08	GND

1.0 MHZ GATED OSCILLATOR

CATEGORY CODE

S22

P/N	5803837
EC	162356
STANDARD RESTRICTED	
CARD SIZE	1-12



06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		ENDICOTT Responsibility	1-67 Date	1 OF 2 Page

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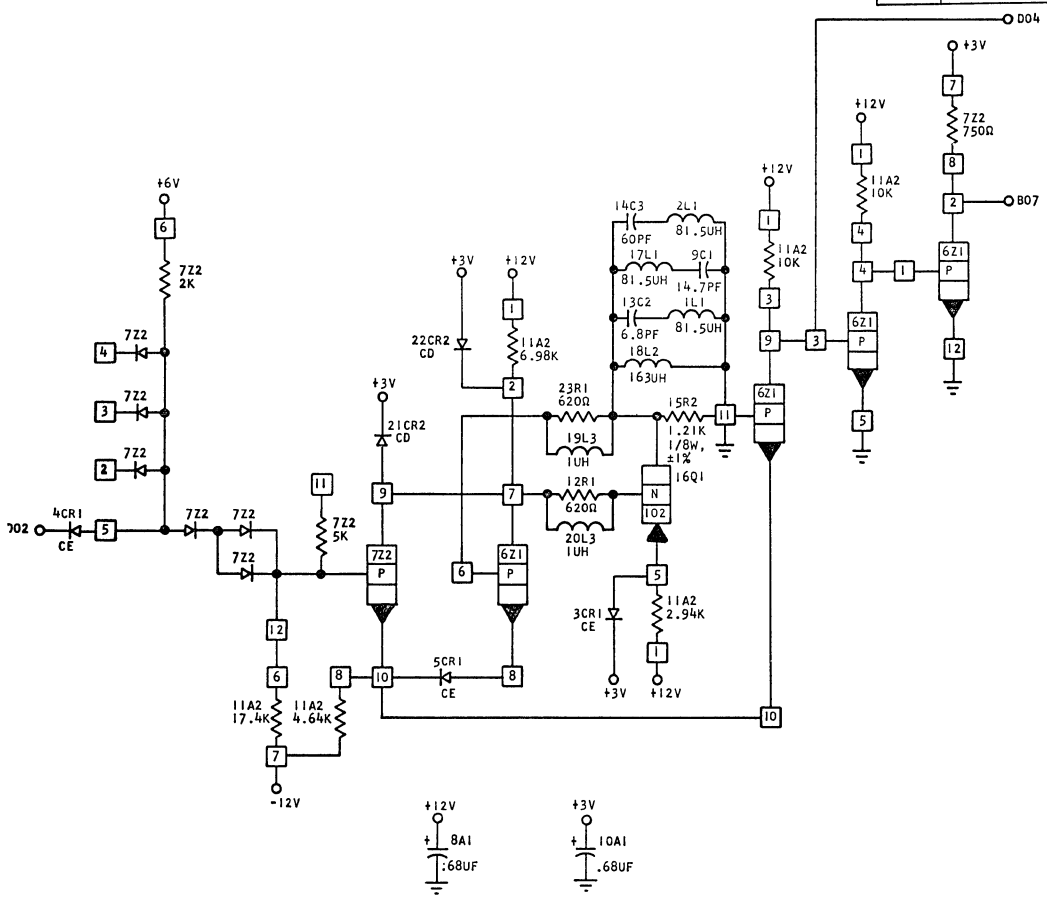
LMH Cat.	O-2860 Subject	382 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1.0 MHZ GATED OSCILLATOR

P/N	5803837
EC	162356



ALL RESISTORS ARE 1/4W ±5%
UNLESS OTHERWISE SPECIFIED

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
720 K HZ OSCILLATOR

LMH	0-2860	384
Cat.	Subject	Suffix

IBM

Location
Manufacturing Specification

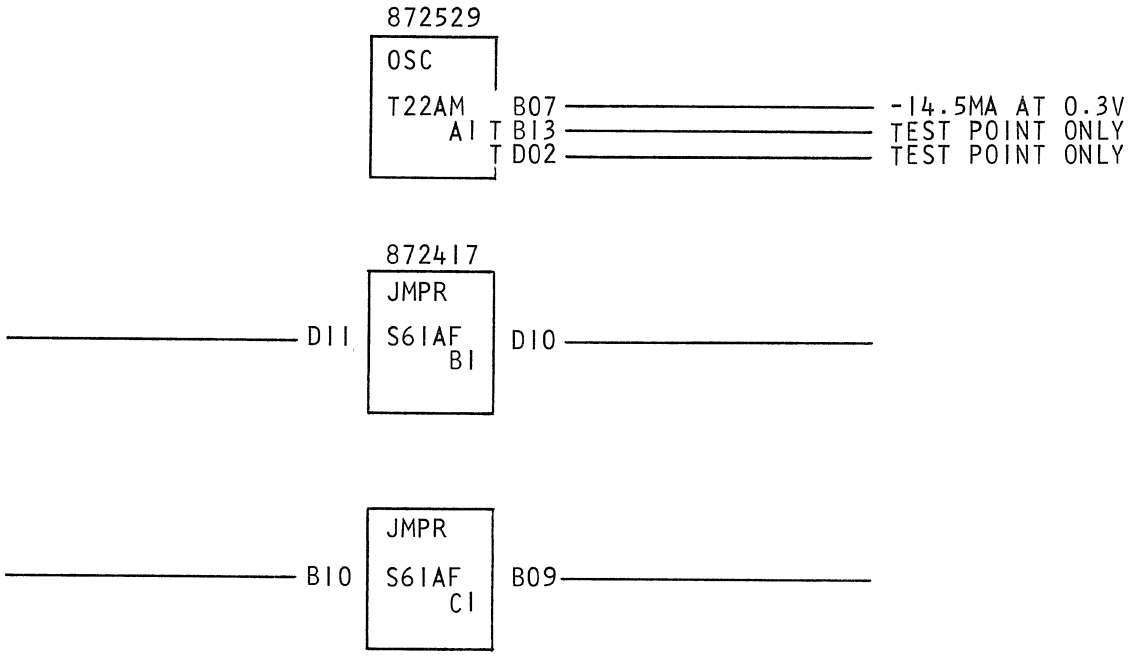
POWER REQUIRED	
PIN	VOLTS
B06	-3
D03	+3
D08	GND

720 K HZ OSCILLATOR

CATEGORY CODE

T22

P/N	5803938	
EC	160624	
SPECIAL	RESTRICTED	
CARD	SIZE	1-12



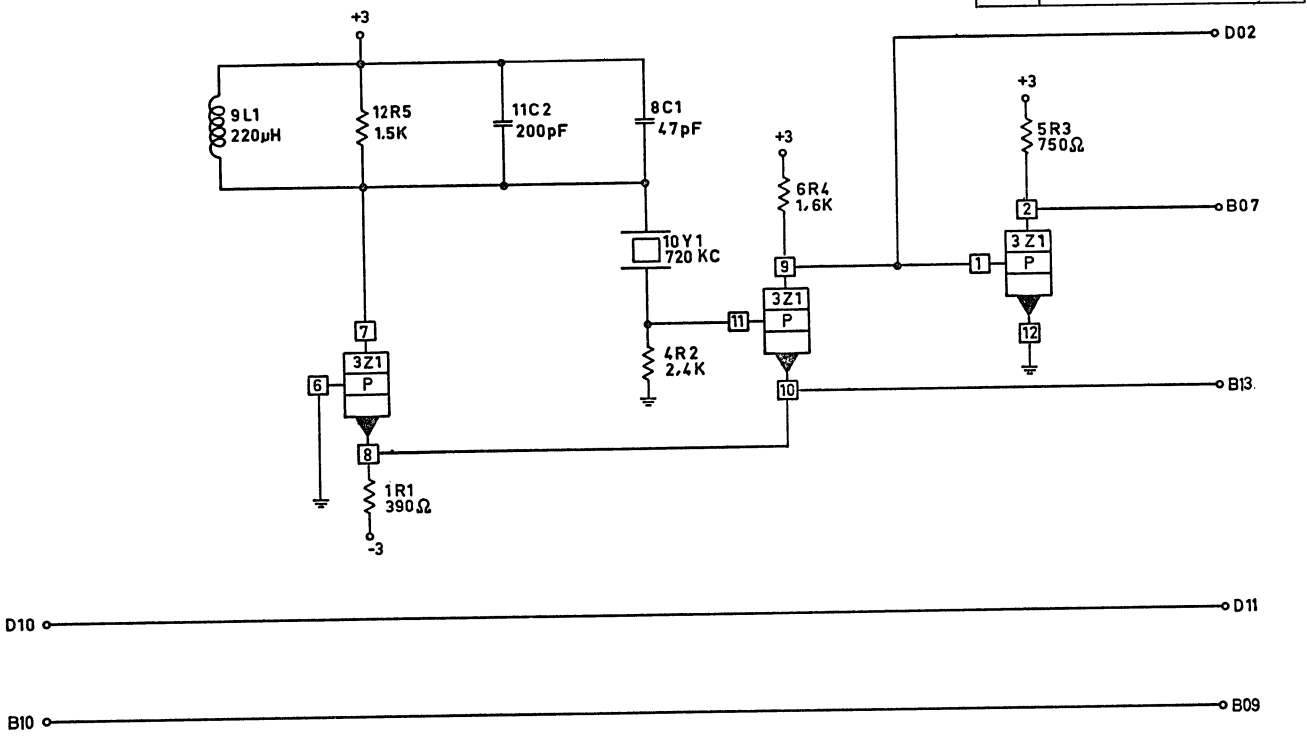
06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		ENDICOTT Responsibility	1-67 Date	1 of 2 Page

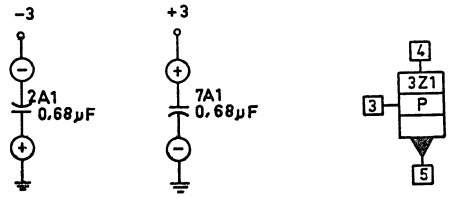
PRINTED IN USA

LMH Cat.	0-2860 Subject	384 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
720 K HZ OSCILLATOR

P/N	5803938
EC	160624





PIN BUSSING B10, B09 CONNECTED
D10, D11 CONNECTED

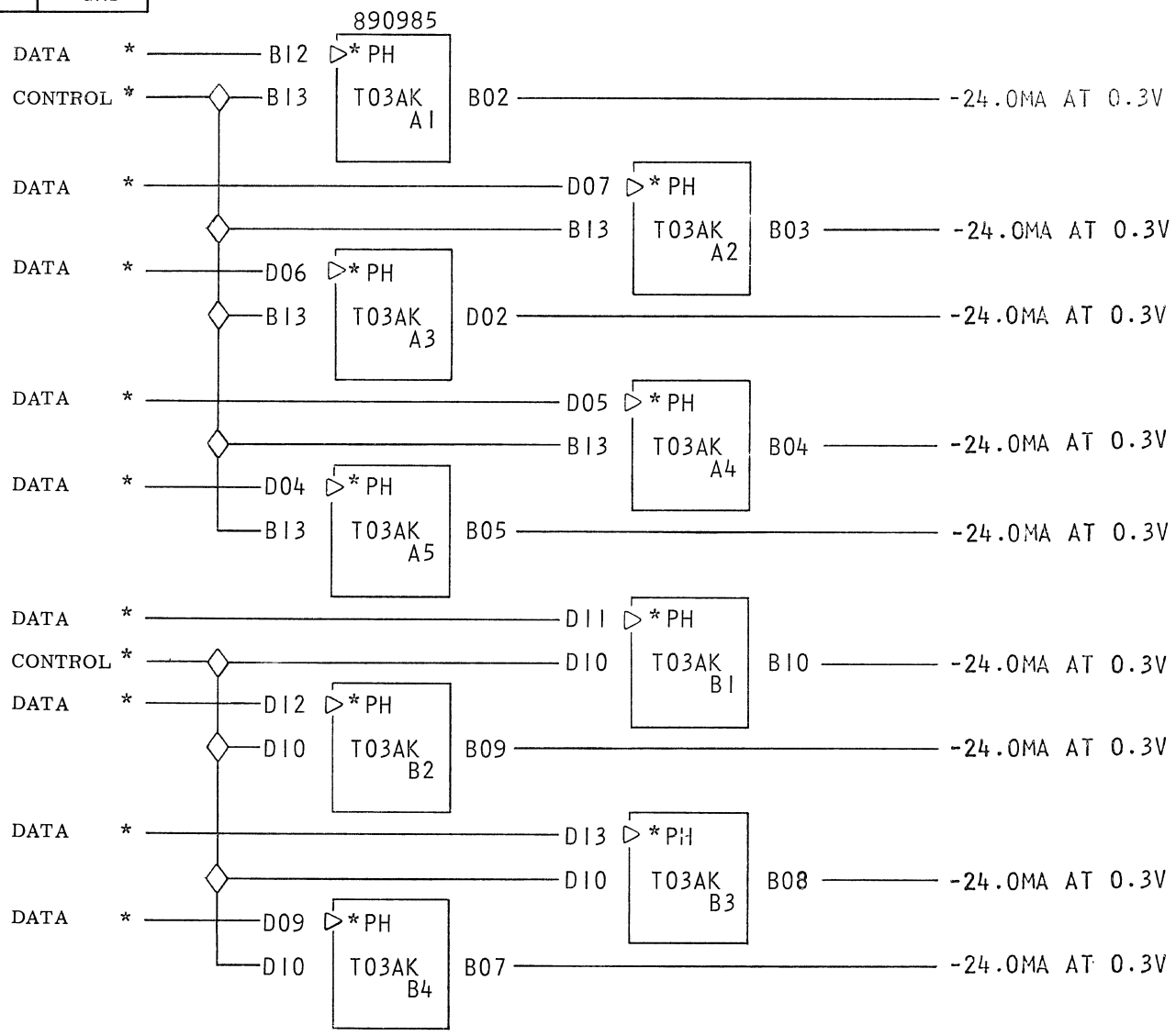
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND

9 BIT POSITION STORAGE

CATEGORY CODE

T03

P/N	5804007
EC	160811
STANDARD RESTRICTED	
CARD SIZE	1-12

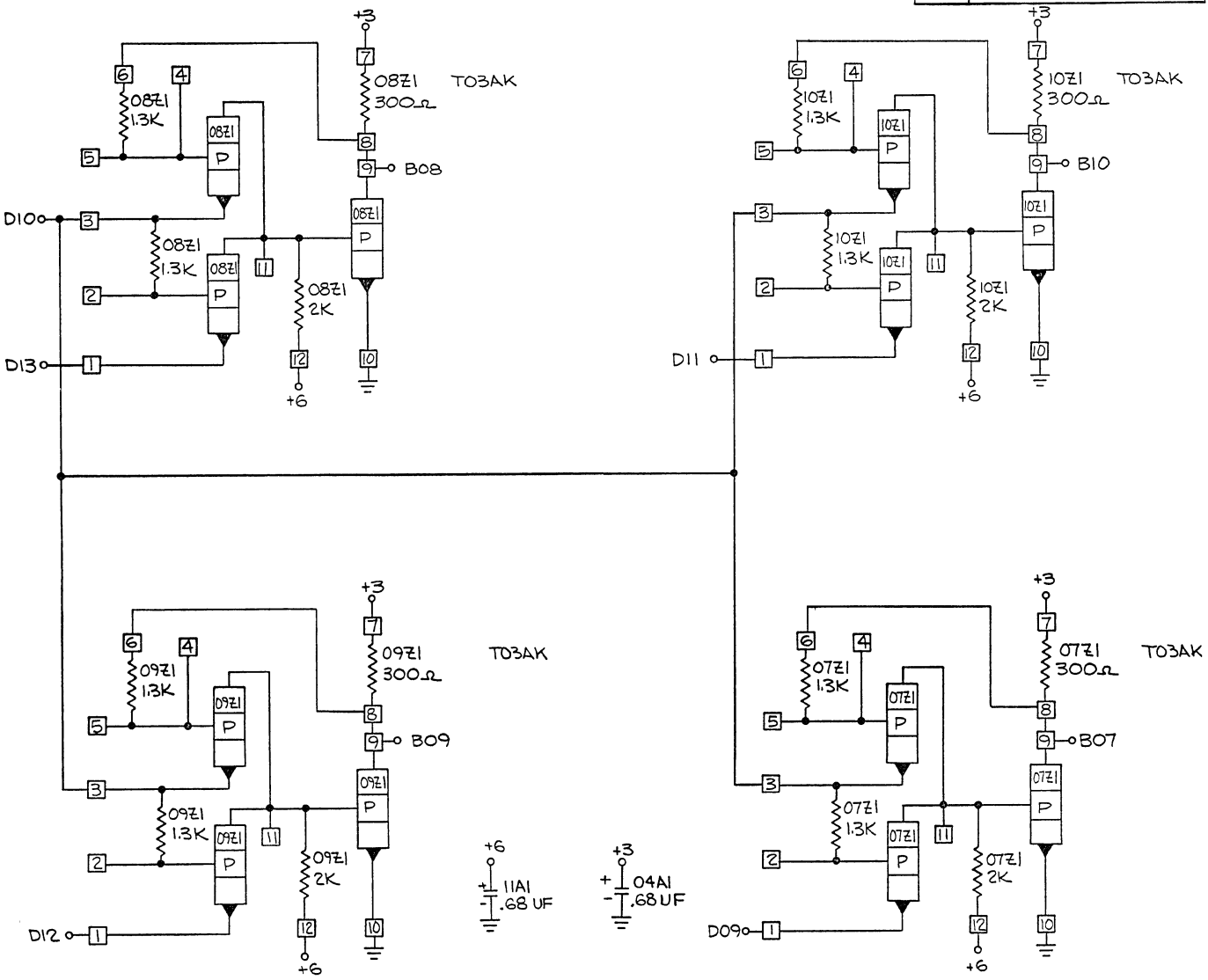


* SPECIAL DRIVING AND LOADING INFORMATION SEE CIRCUIT SPEC 890985

LMH Cat.	0-2860 Subject	385 Suffix

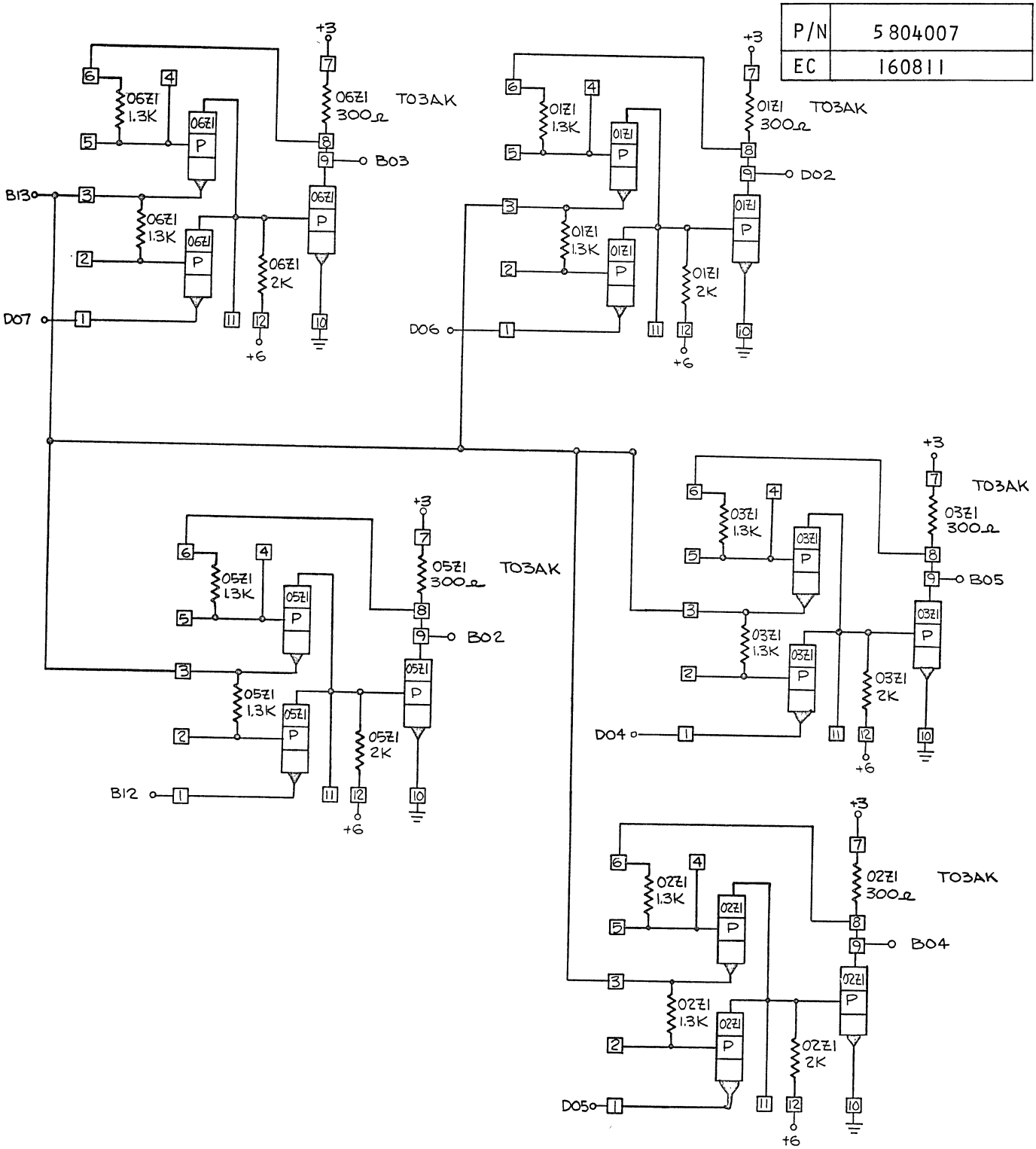
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
9 BIT POSITION STORAGE

P/N	5804007
EC	160811

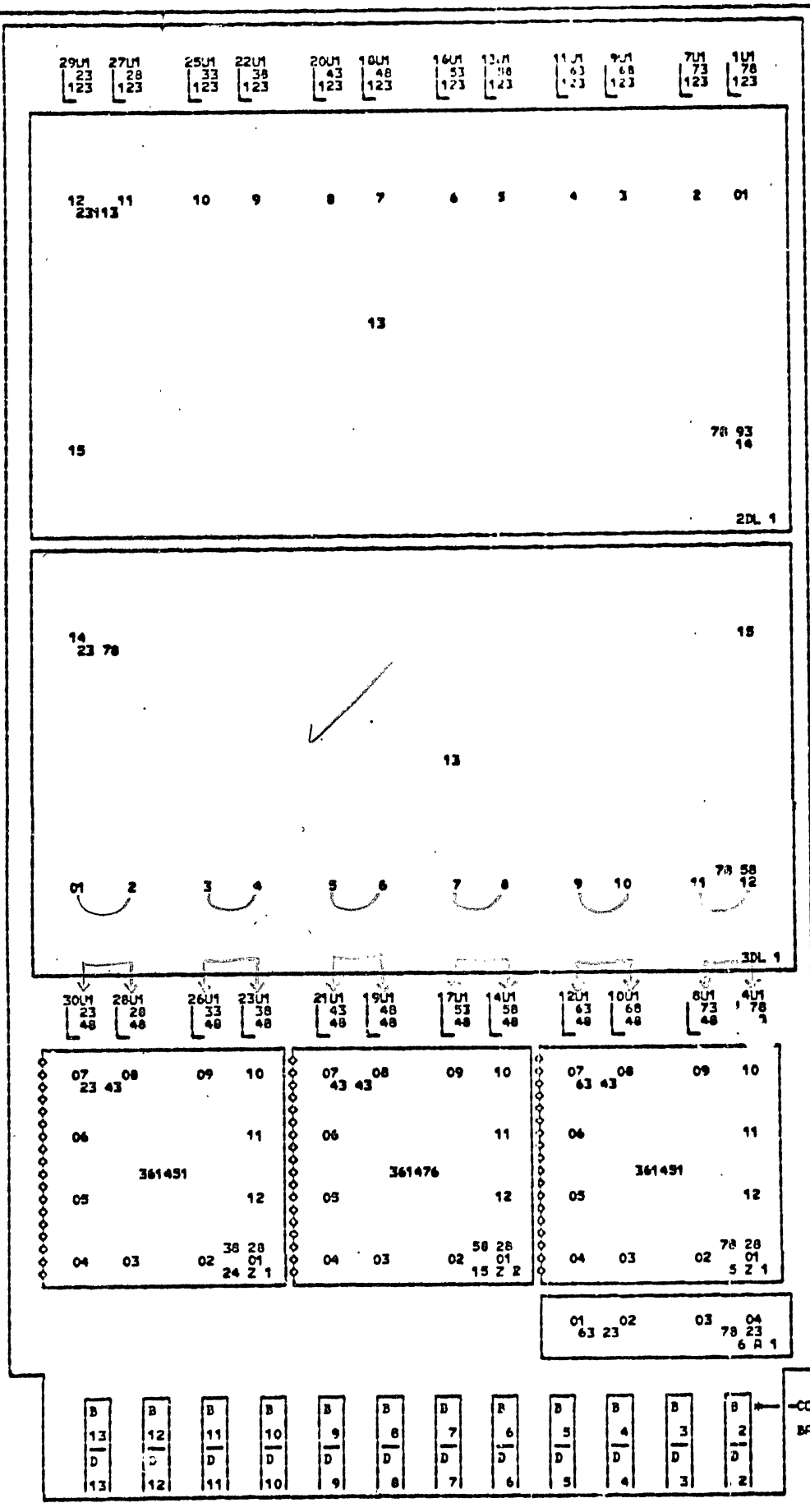


2 of 3 Page	1-67 Date

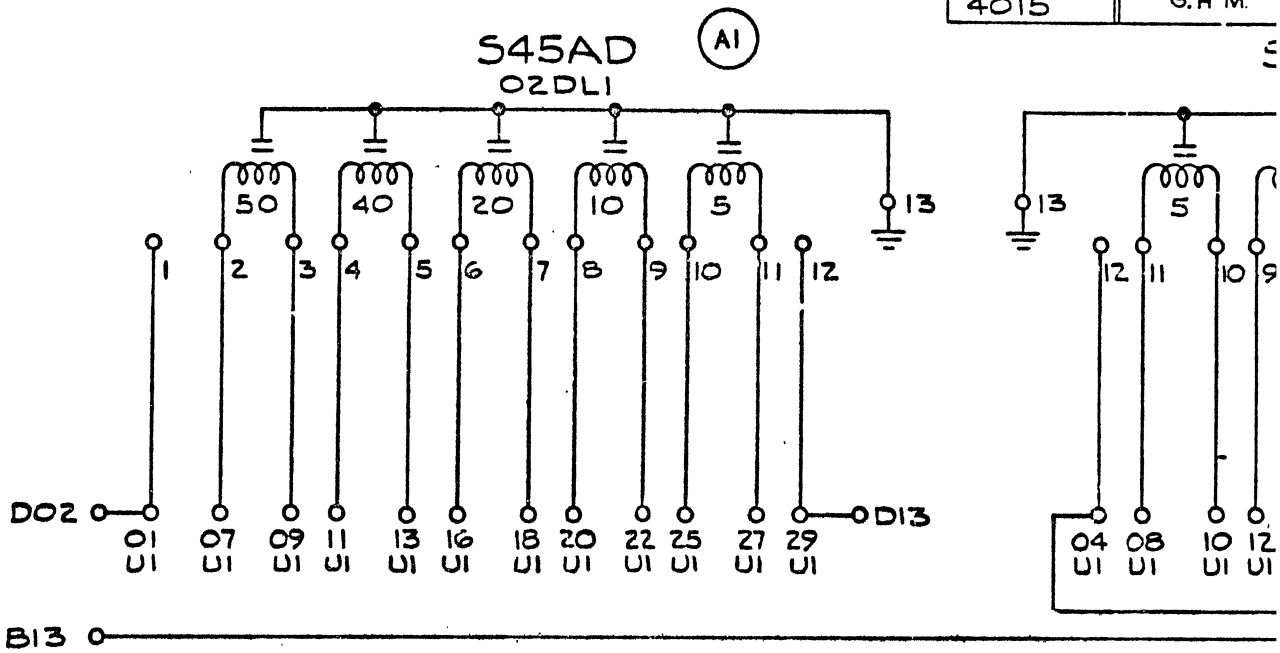
P/N	5804007
EC	160811

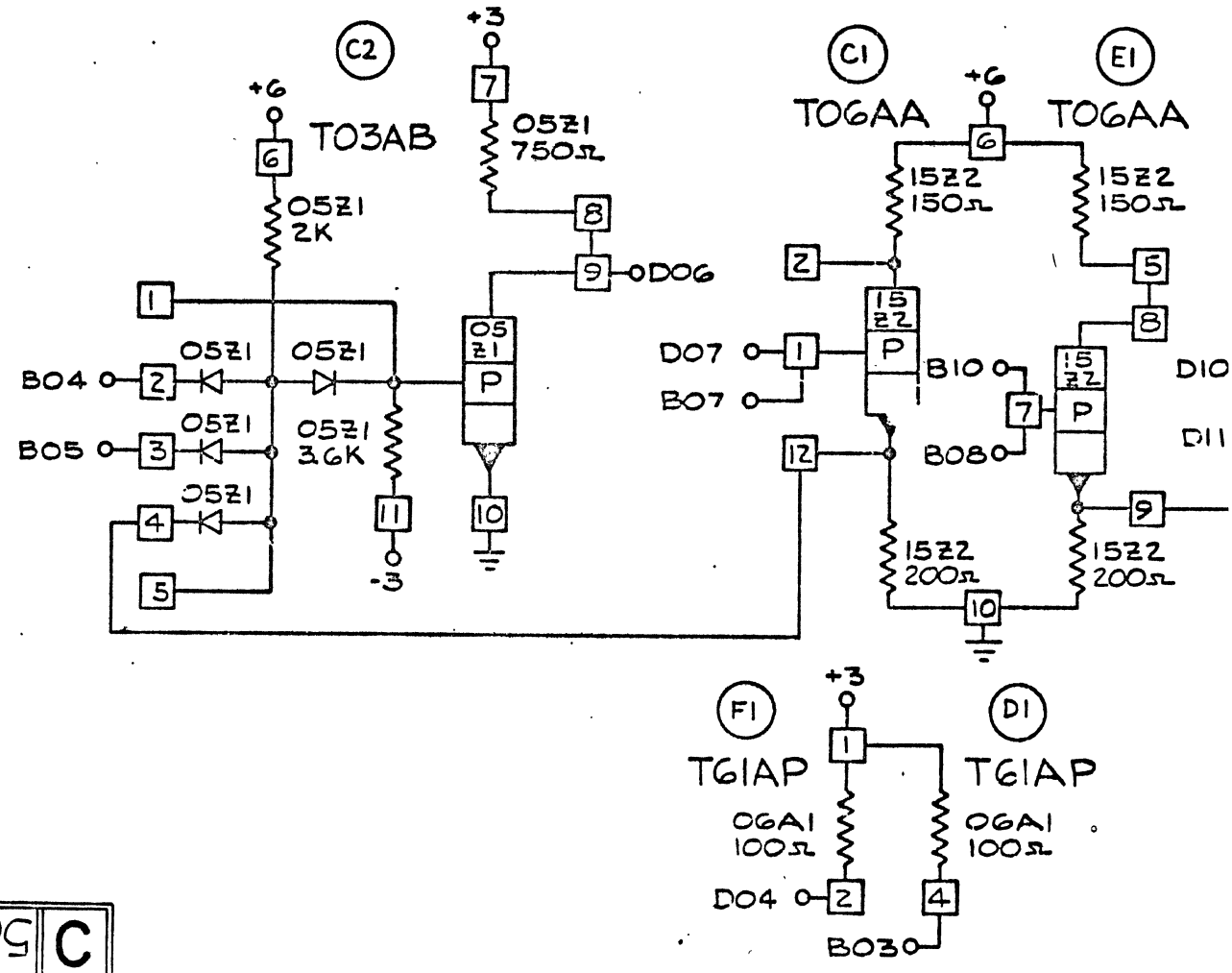


Printed in U S A.


29U1 23 123
27U1 28 123
25U1 33 123
22U1 38 123
20U1 43 123
18U1 48 123
16U1 53 123
13U1 58 123
11U1 63 123
9U1 68 123
7U1 73 123
1U1 78 123
2DL 1
3DL 1
30U1 23 48
28U1 28 48
26U1 33 48
23U1 38 48
21U1 43 48
19U1 48 48
17U1 53 48
14U1 58 48
12U1 63 48
10U1 68 48
8U1 73 48
4U1 78 1
361451
361476
361451
CONTACTS ON BACK OF CARD

STANDARDS CODE	CIRCUIT / PACKAGING S
2-7045	APPROVAL
CARD CODE	G.H M.
4015	





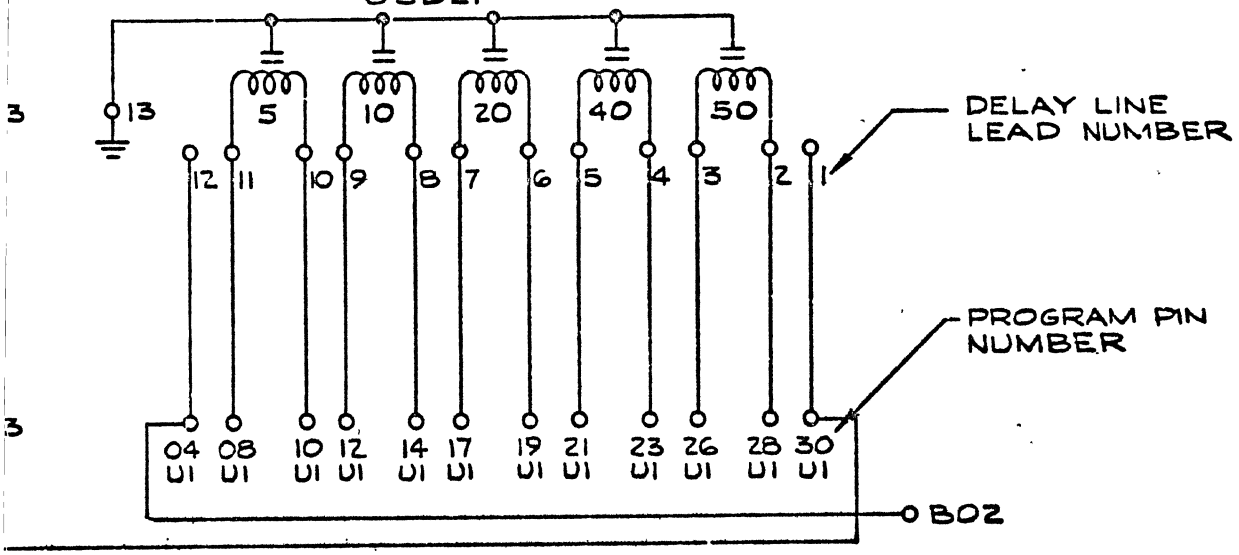
C 5804015

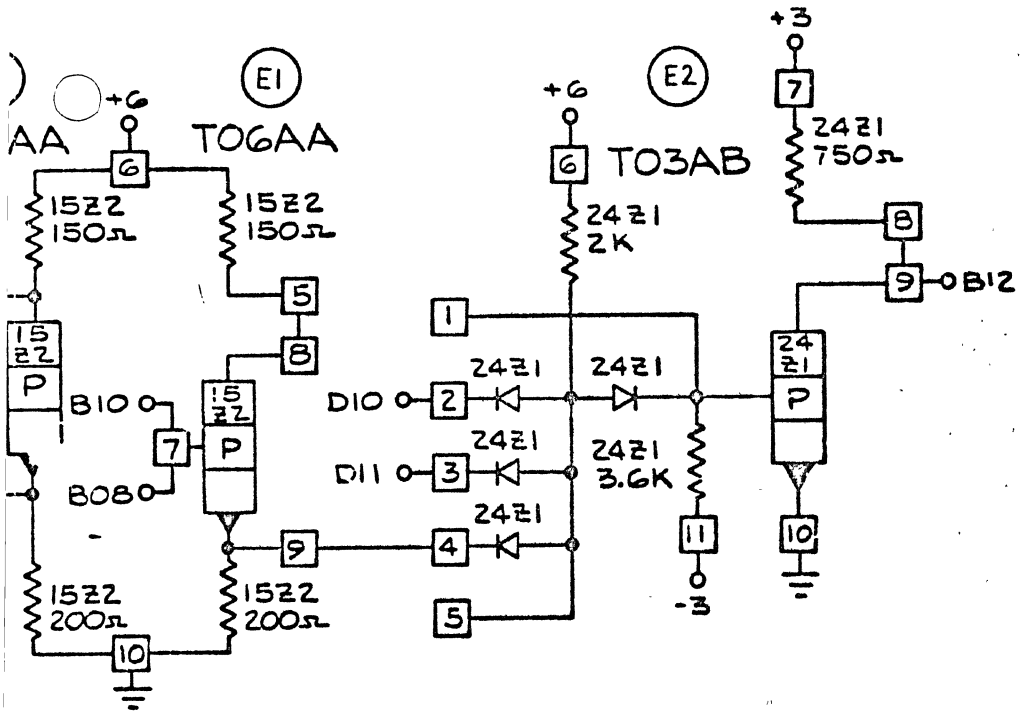
STANDARDS CODE	CIRCUIT AND PACKAGING STANDARD		SYM	DATE	CHANGE NO	TECH APPRO	SYM	DATE	CHANGE NO	TECH APPRO	DEVELOPMENT NO	Q/M
2-7045	APPROVAL	DATE		12-01-63	DEV. 1617							
CARD CODE	G. H. M.	26AUG66		8-13-64	160484						5804015	
4015				12SEP66	168746	B						

SHEET 3 OF 4

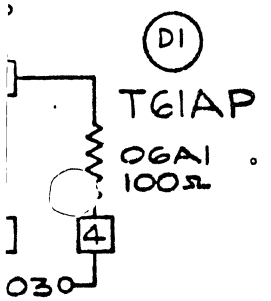
RESTRICTED

S45AD 03DL1 (B1)





NOTE
NO BUSSING CONDITIONS



INTERNATIONAL BUSINESS MACHINES CORP					
NAME	CARD ASM-DELAY LINE				
2-LSA-AJ'S & 2 LTN S					
DESIGN	TJZ	6-29-63	TYPE	2050	
DETAIL	TJZ	6-29-63	SCALE	NONE	
CHECK	DJL	7-1-63	DRAW	CDA	6-10-64
APPRO	WJR	7-17-63	CHECK	CDA	6-11-64

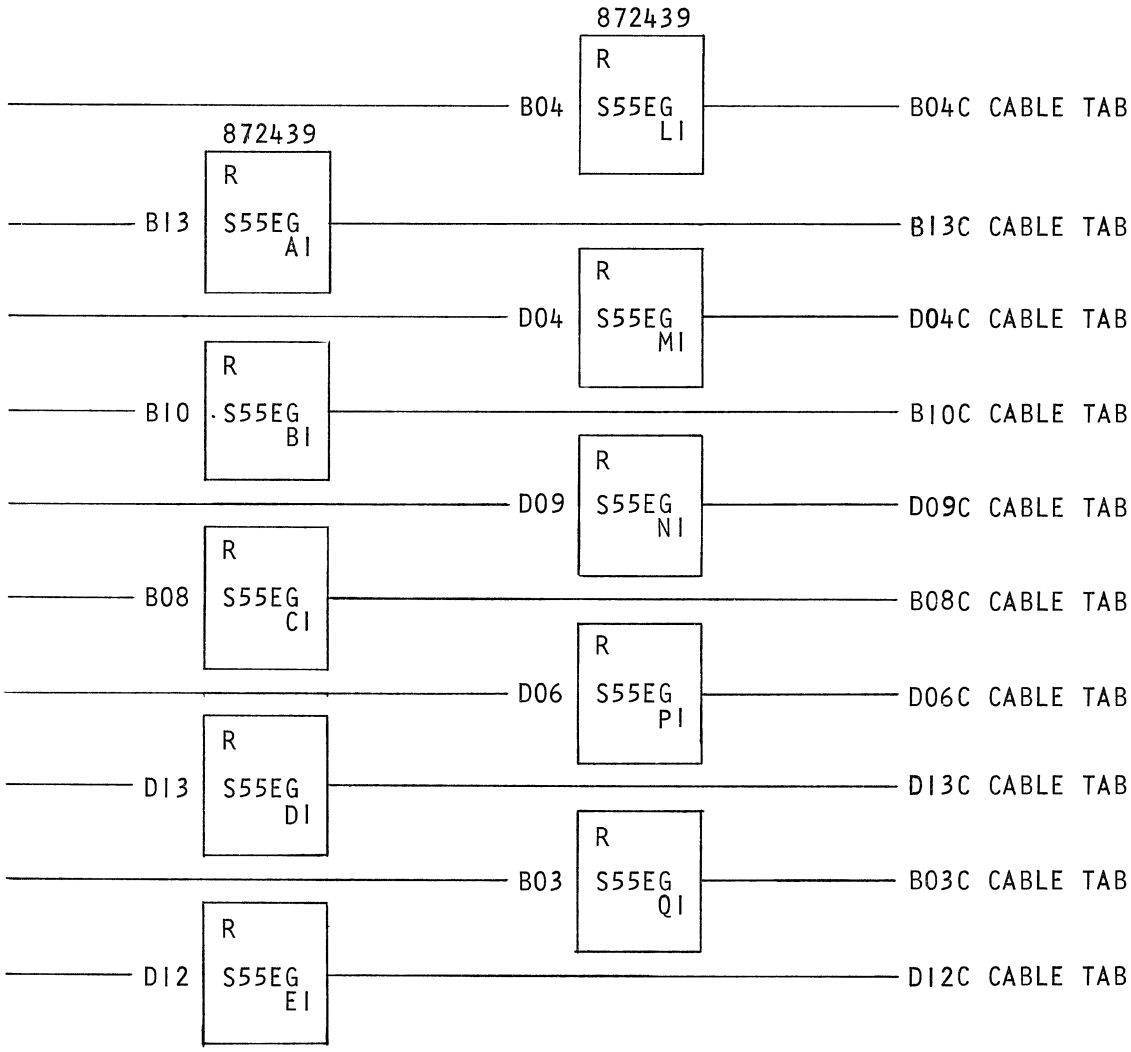
POWER REQUIRED	
PIN	VOLTS
D08	GND

20-6.2K OHM SCR SIGNAL ENTRY RESISTORS

CATEGORY CODE

S55

P/N	5805015
EC	168796
STANDARD RESTRICTED	
CARD SIZE	1-12



NOTE:

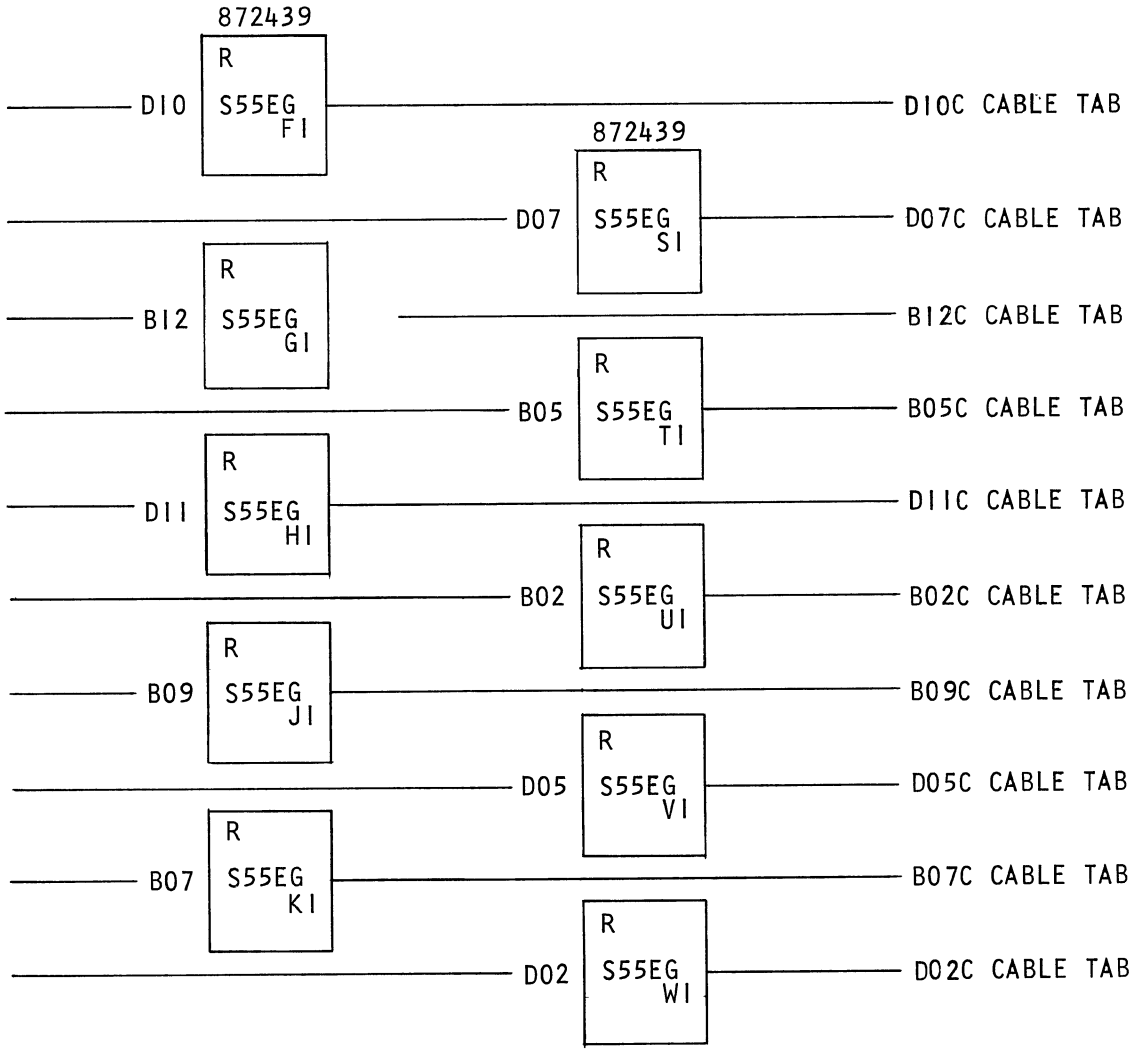
ALL RESISTORS ARE 50MW, ±5%

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
20-6.2K OHM SCR SIGNAL ENTRY RESISTORS

20-6.2K OHM SCR SIGNAL ENTRY RESISTORS

S55

P/N	5805015
EC	168796

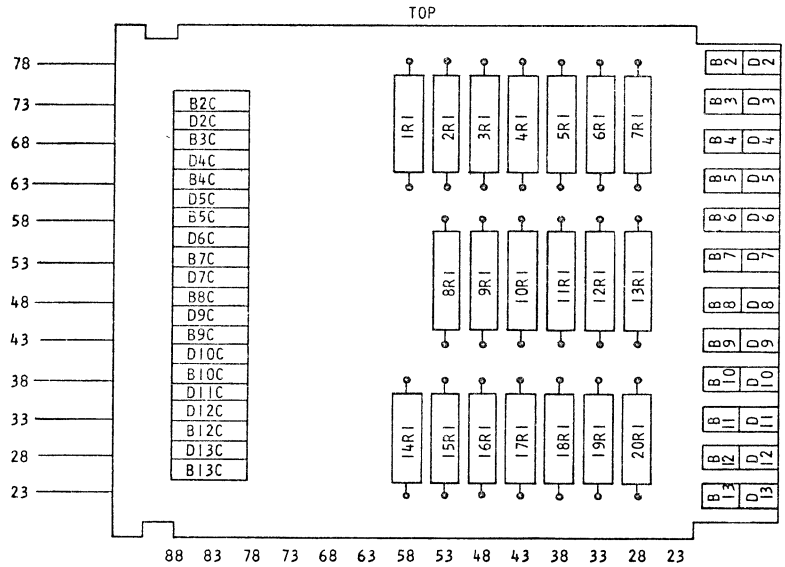


CODE	PART NO.	VALUE	QTY
	5819674	CARD	1
R1	216463	6.2K	20

P/N	5805015
EC	168796

VOLTAGE	PIN	VOLTAGE	PIN
GND	D08		

CKT. FAMILY	HOLE PAT.
	813818

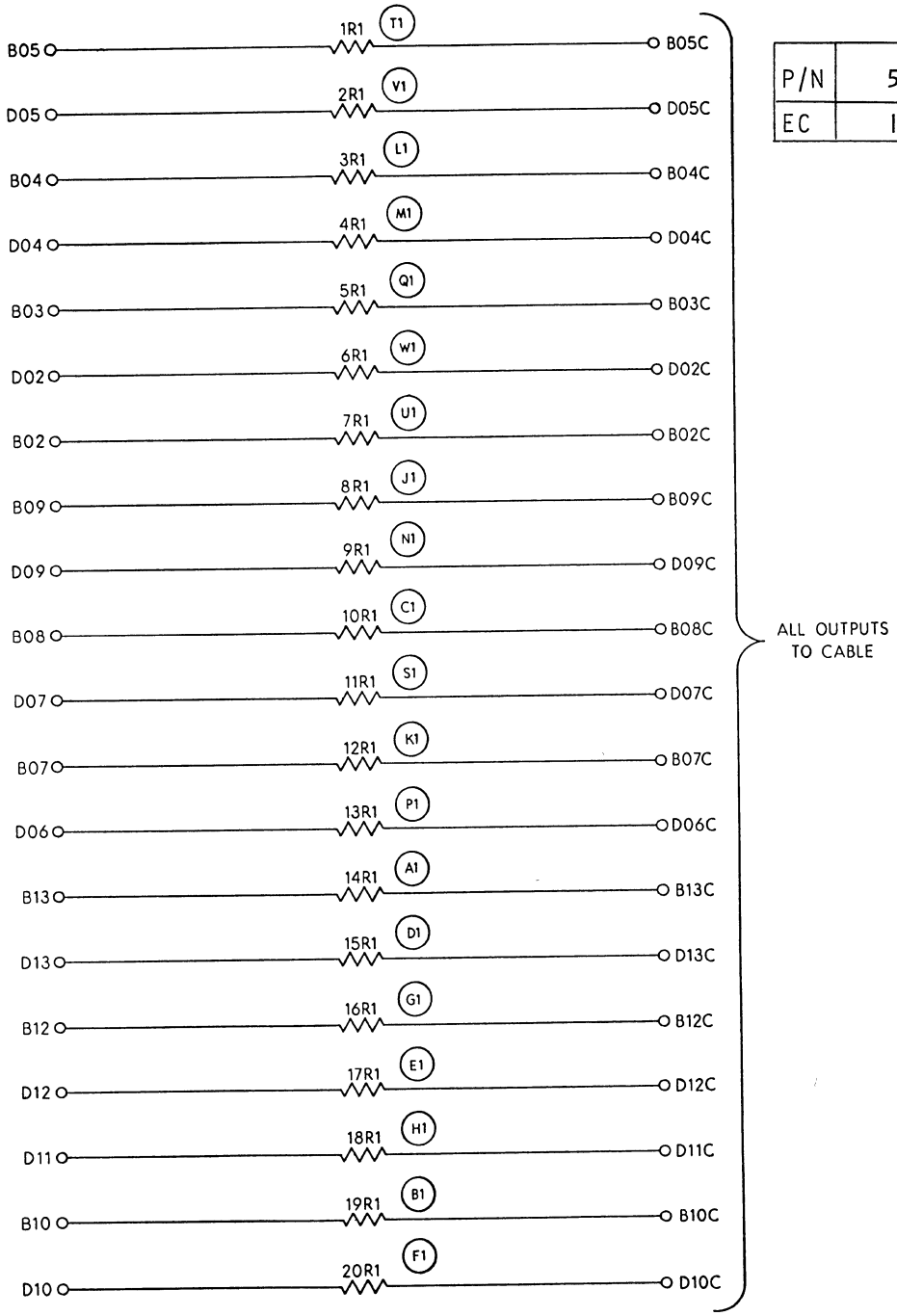


COMPONENT VIEW

Printed in U S A

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
20-6.2K OHM SCR SIGNAL ENTRY RESISTORS

P/N	5805015
EC	168796



NOTE:
ALL RESISTORS ARE 6.2K, 1/4W, 5%
ALL FLYERS S55EG

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
REED RELAY DRIVERS AND LATCHES

LMH	0-2860	396
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

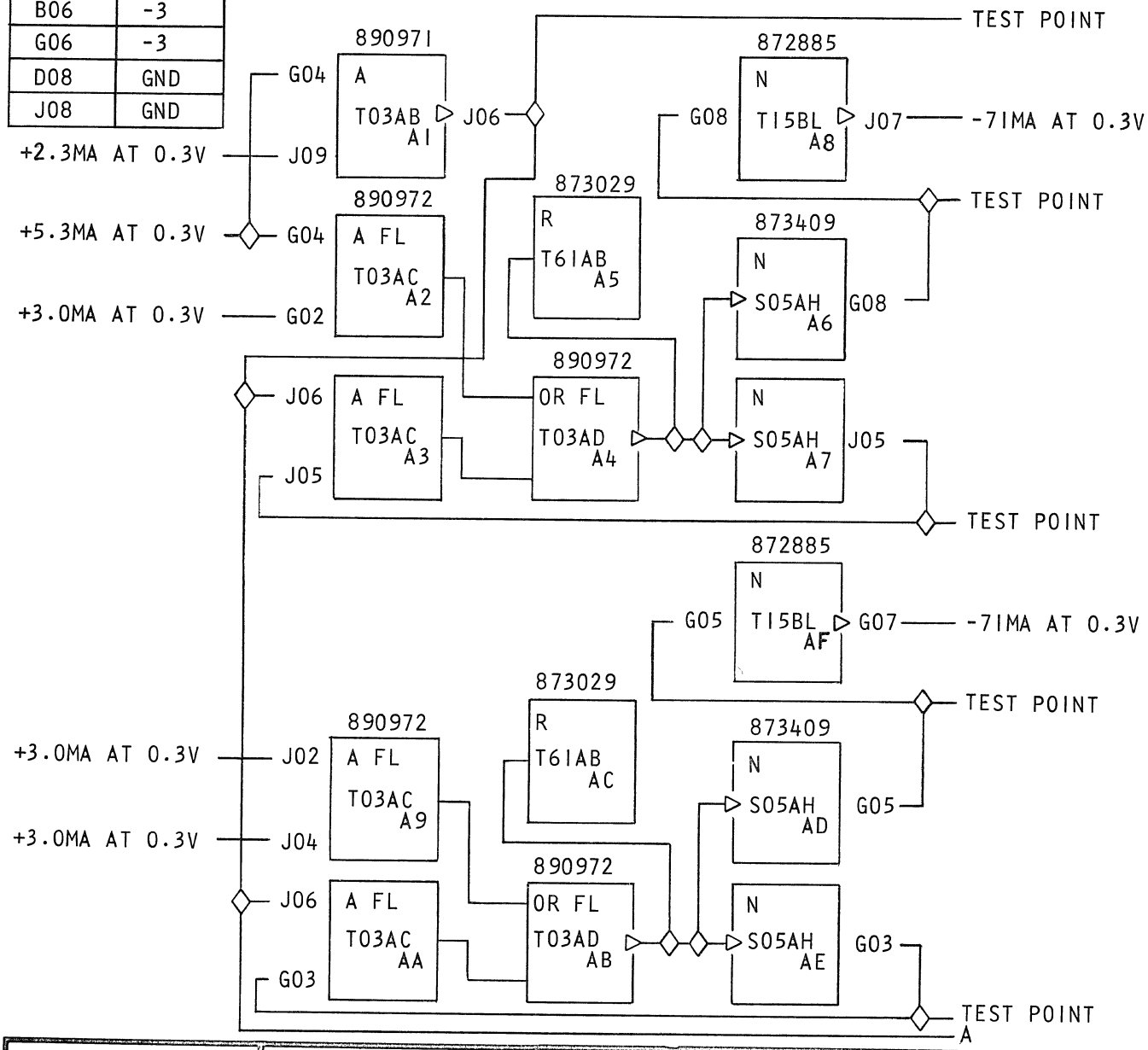
POWER REQUIRED	
PIN	VOLTS
B11	+6
G11	+6
D03	+3
J03	+3
B06	-3
G06	-3
D08	GND
J08	GND

REED RELAY DRIVERS AND LATCHES

CATEGORY CODE

T65

P/N	5806140
EC	164122B
STANDARD RESTRICTED	
CARD SIZE	2-24



06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.		
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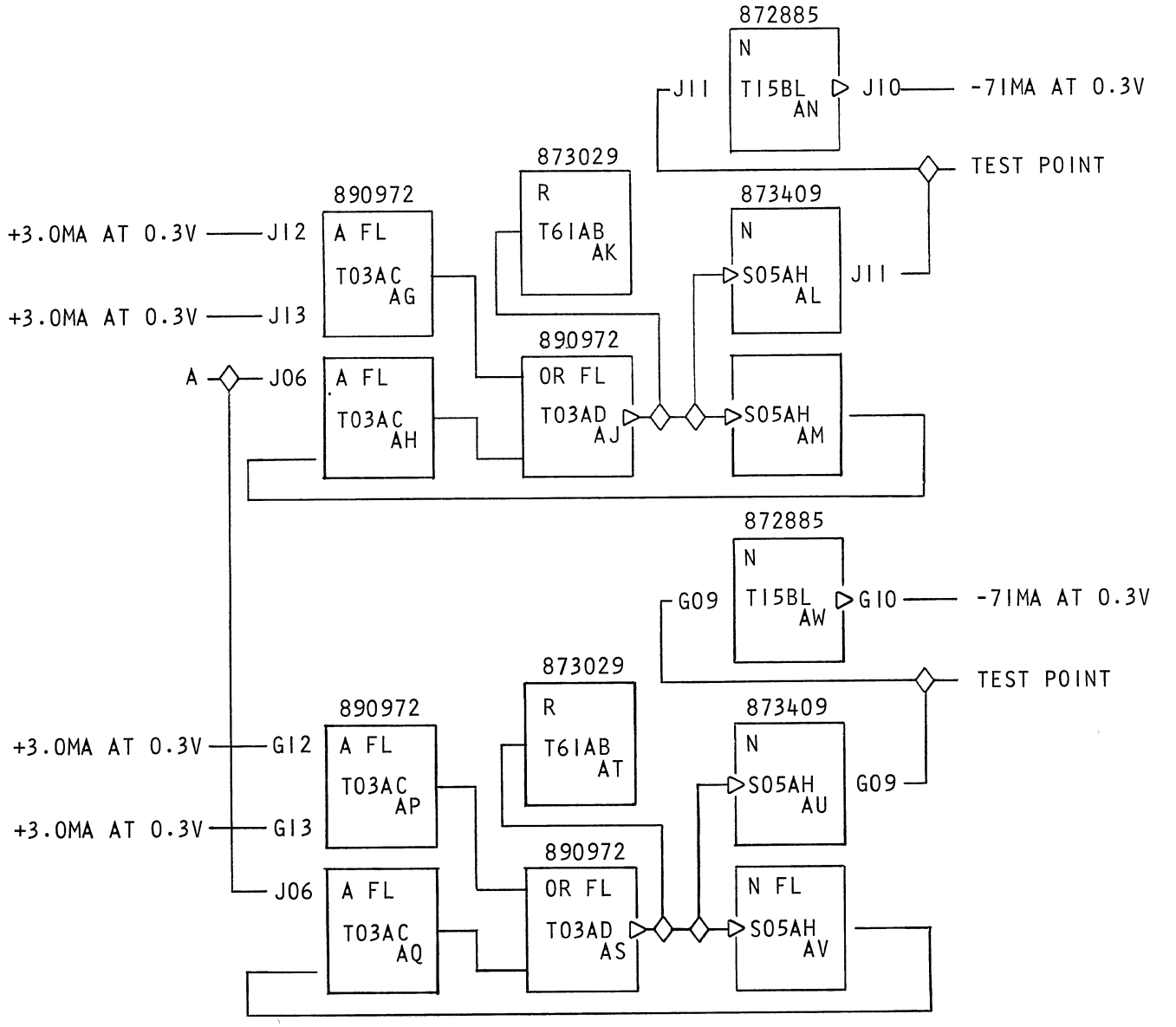
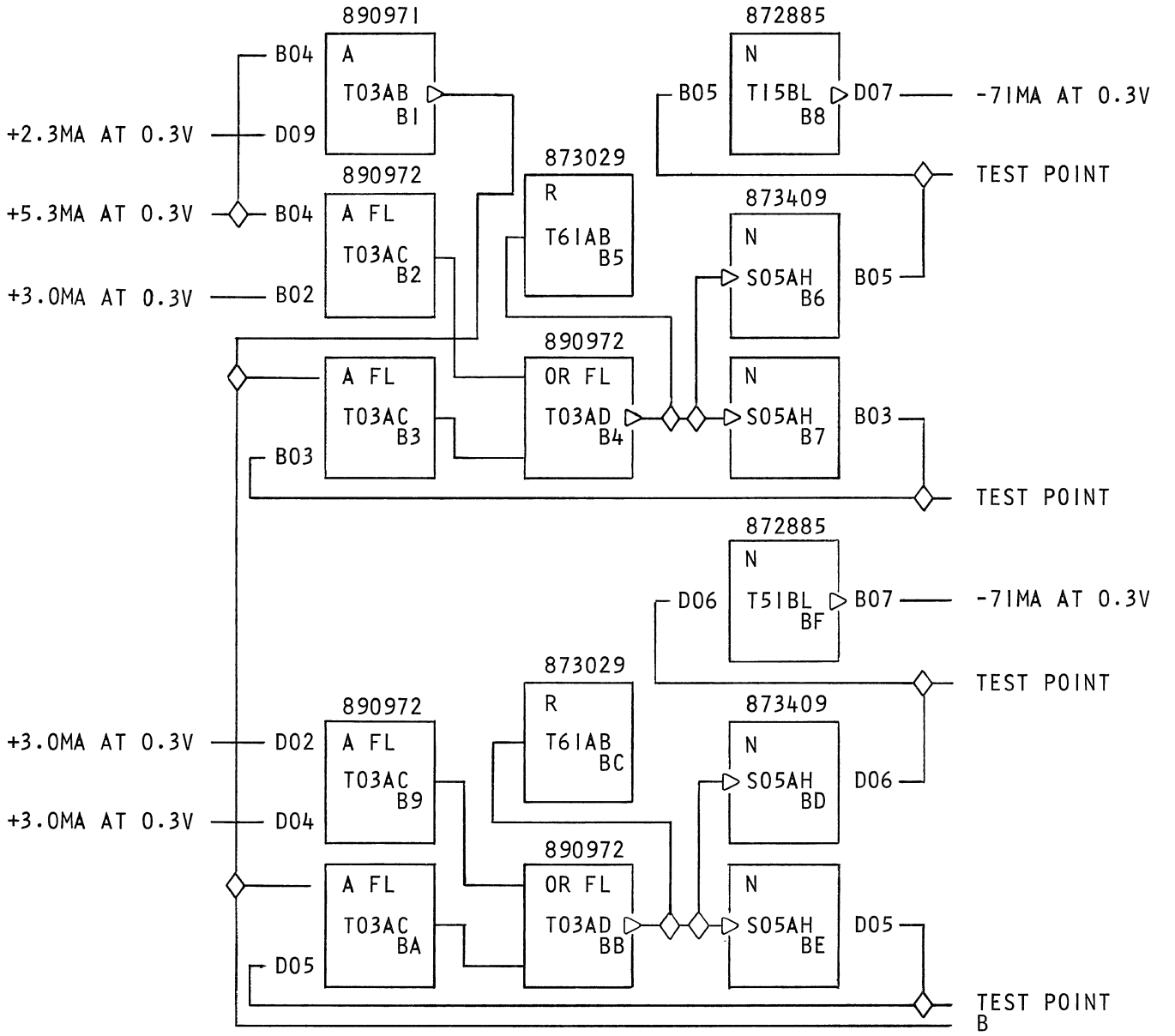
REED RELAY DRIVERS AND LATCHES

P/N	5806140
EC	164122B



REED RELAY DRIVERS AND LATCHES

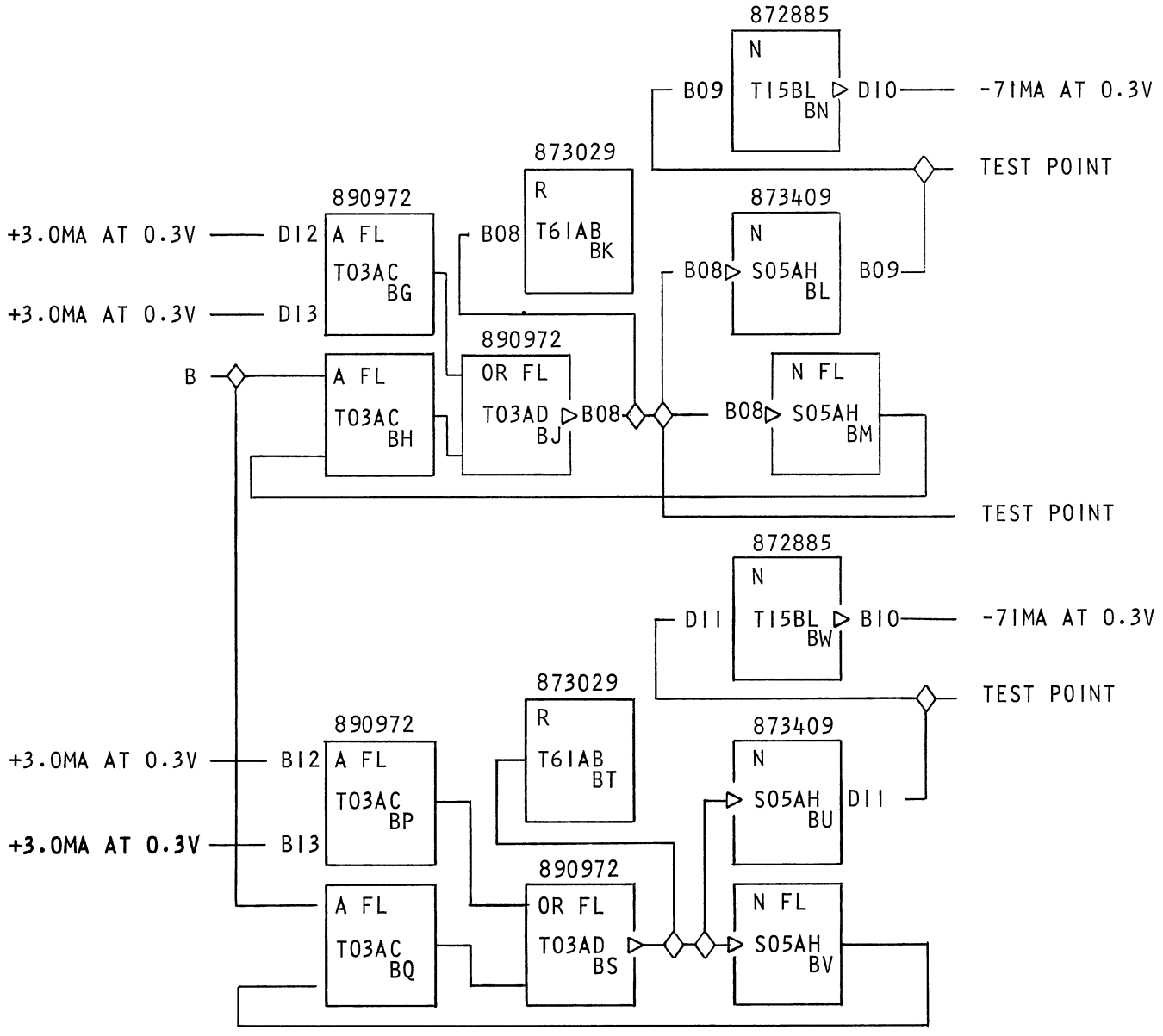
P/N	5806140
EC	164122B



Printed in U.S.A.

REED RELAY DRIVERS AND LATCHES

P/N	5806140
EC	164122B



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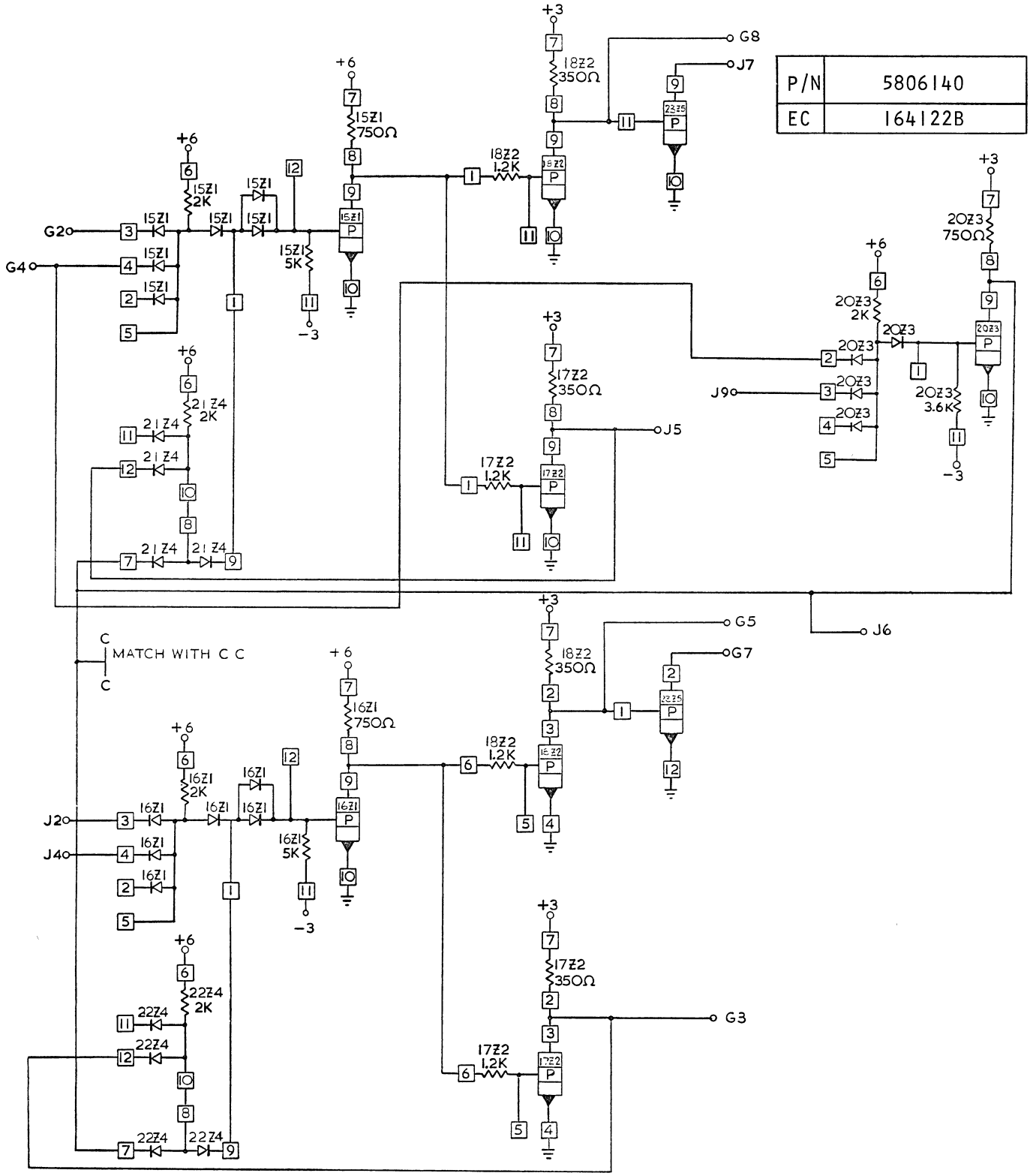
EC	164122B



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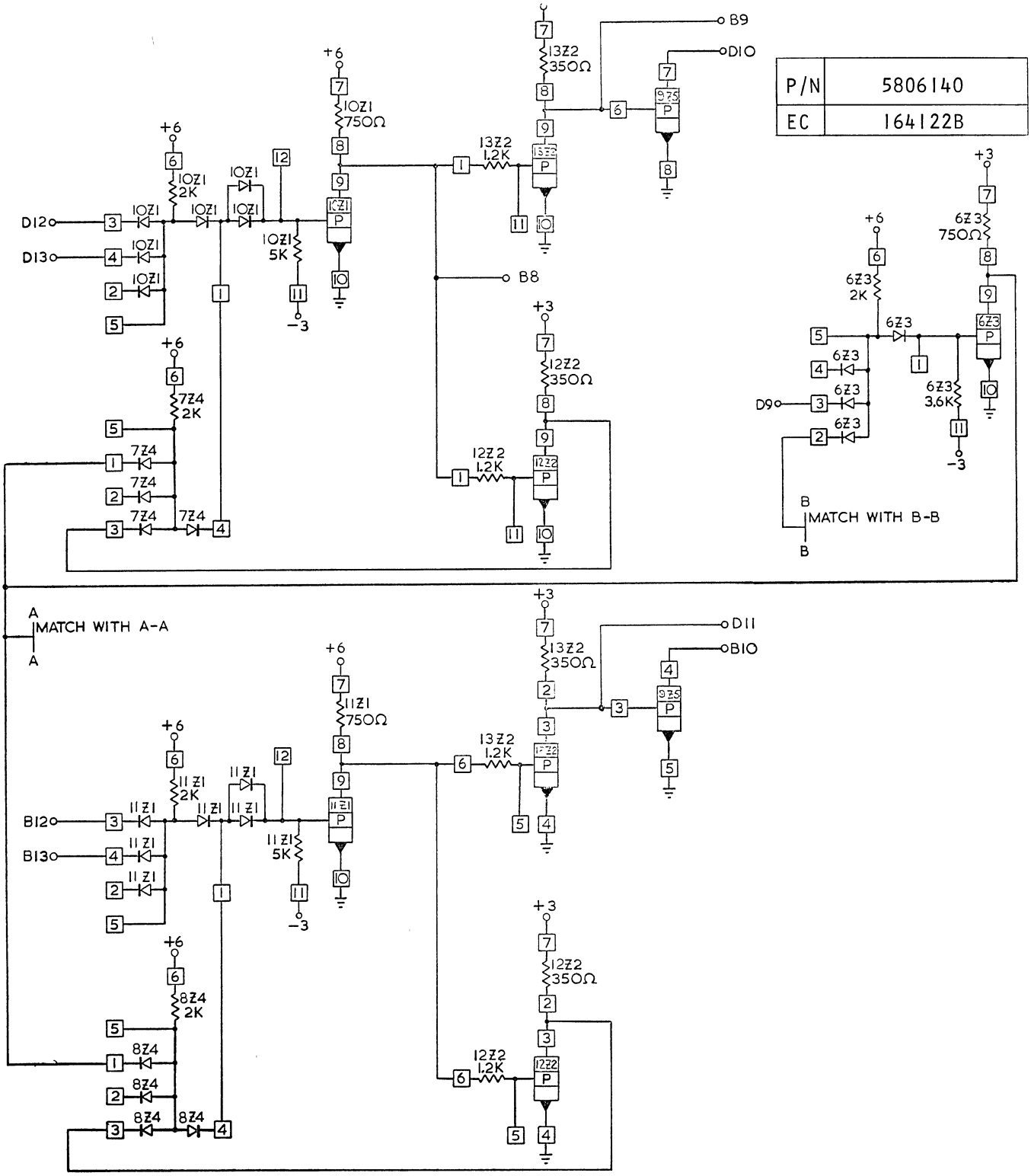
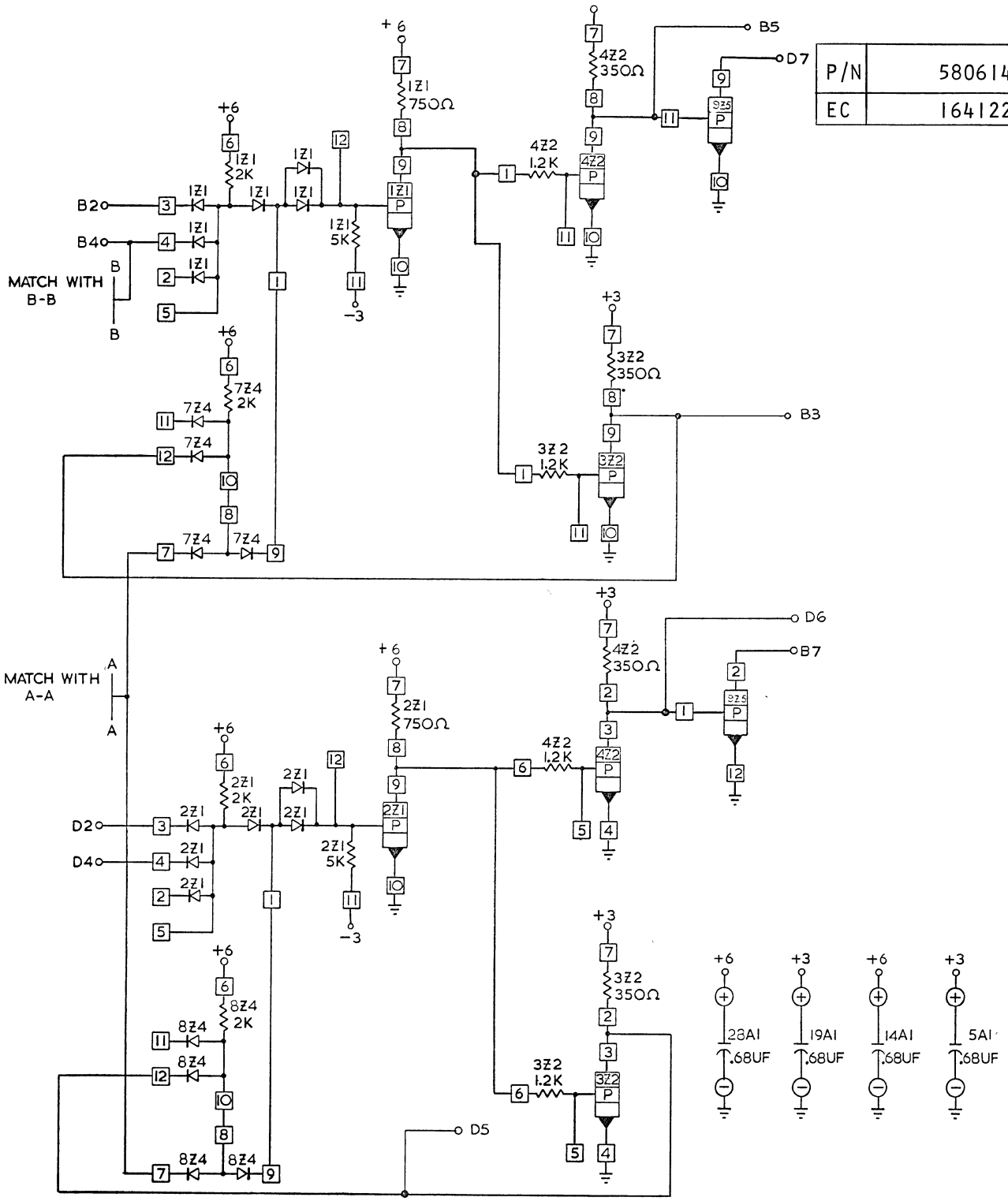
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
REED RELAY DRIVERS AND LATCHES

P/N	5806140
EC	164122B



P/N	5806140
EC	164122B

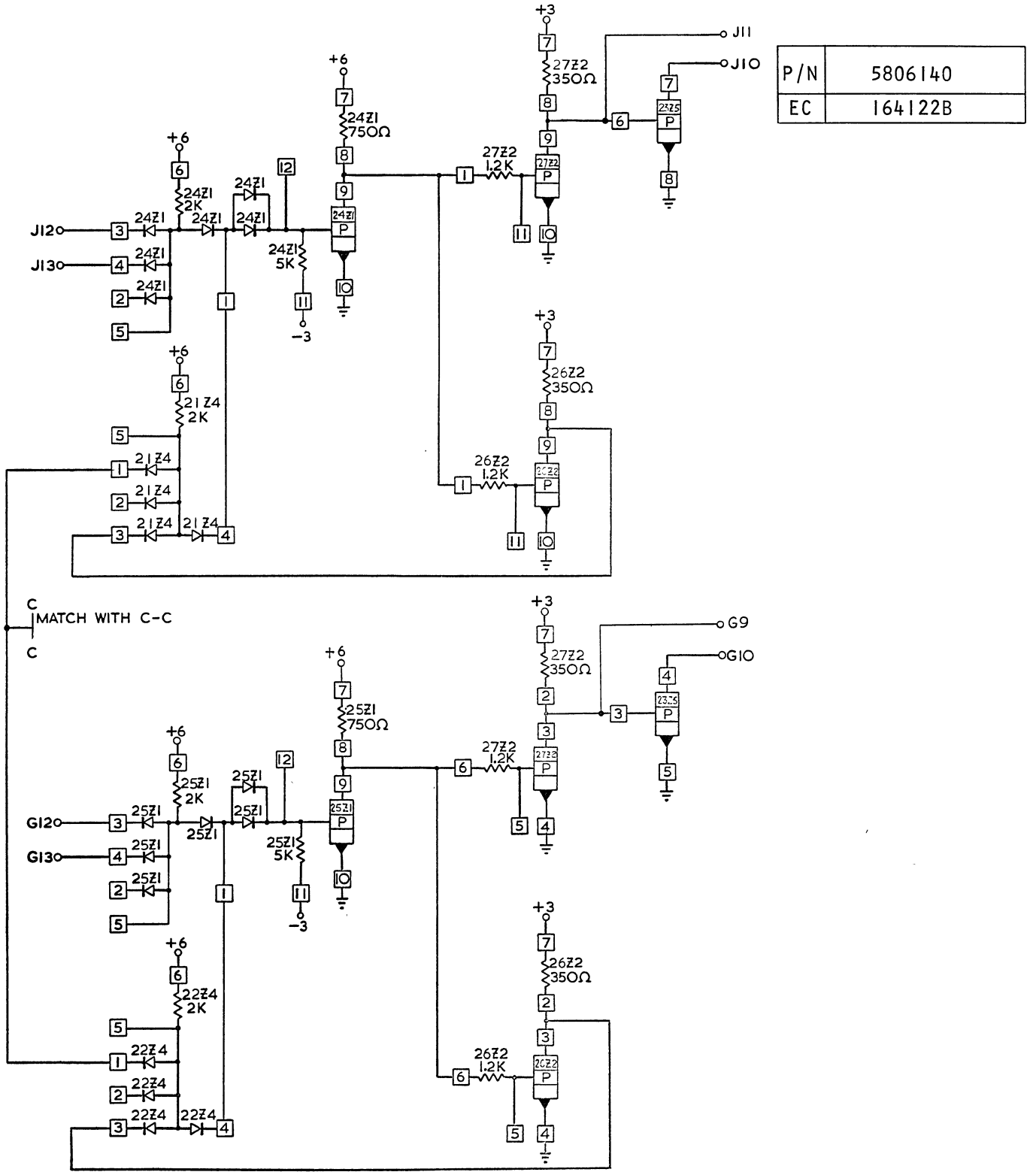


Printed in U.S.A.

LMH Cat.	0-2860 Subject	396 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
REED RELAY DRIVERS AND LATCHES

P/N	5806140
EC	164122B



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6-VARIABLE SS 780US TO 2.07MS

LMH	0-2860	397
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

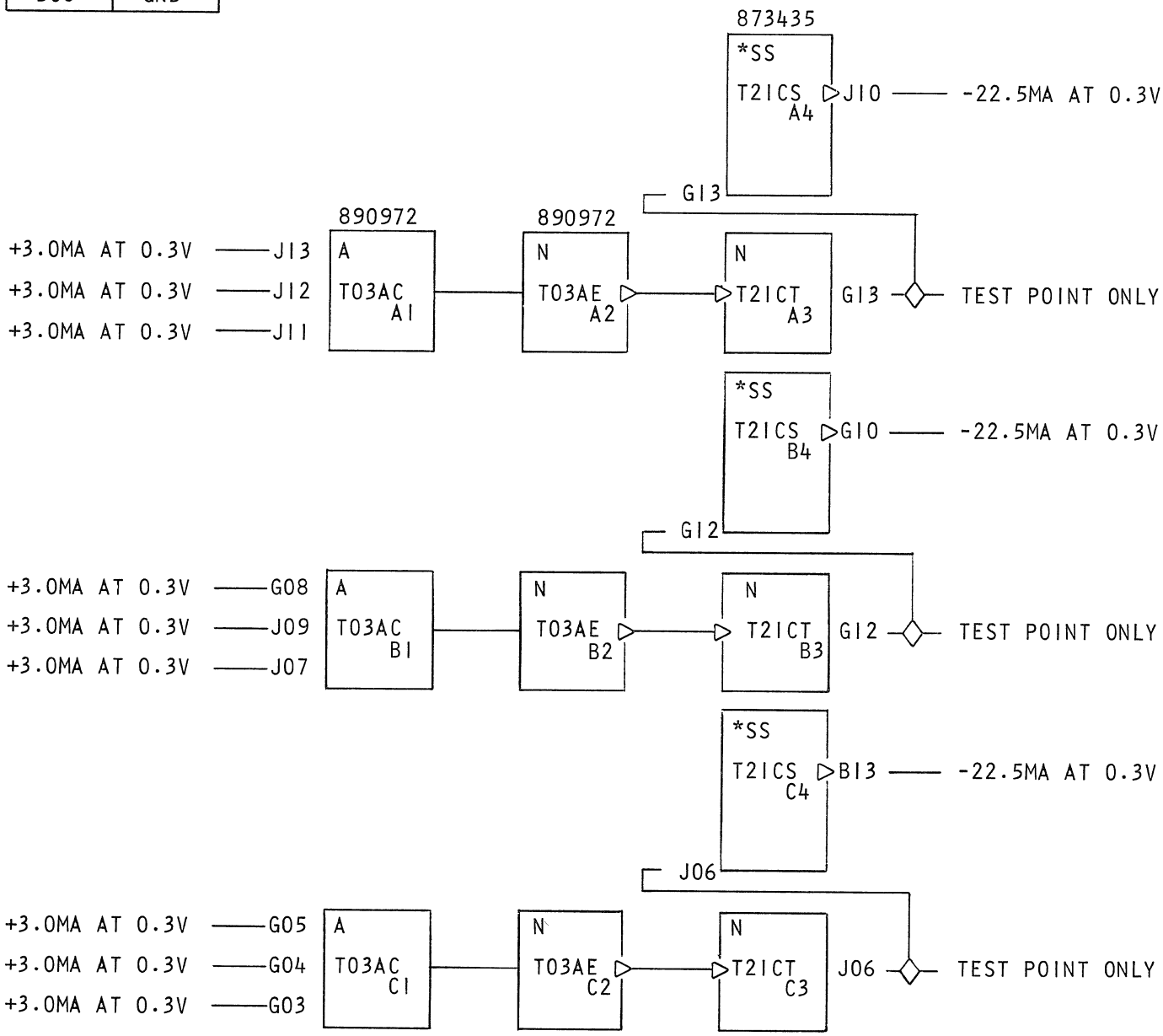
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

6-VARIABLE SS 780US TO 2.07MS

CATEGORY CODE

T03	T21

P/N	5806150
EC	168034
STANDARD RESTRICTED	
CARD SIZE	2-24



06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
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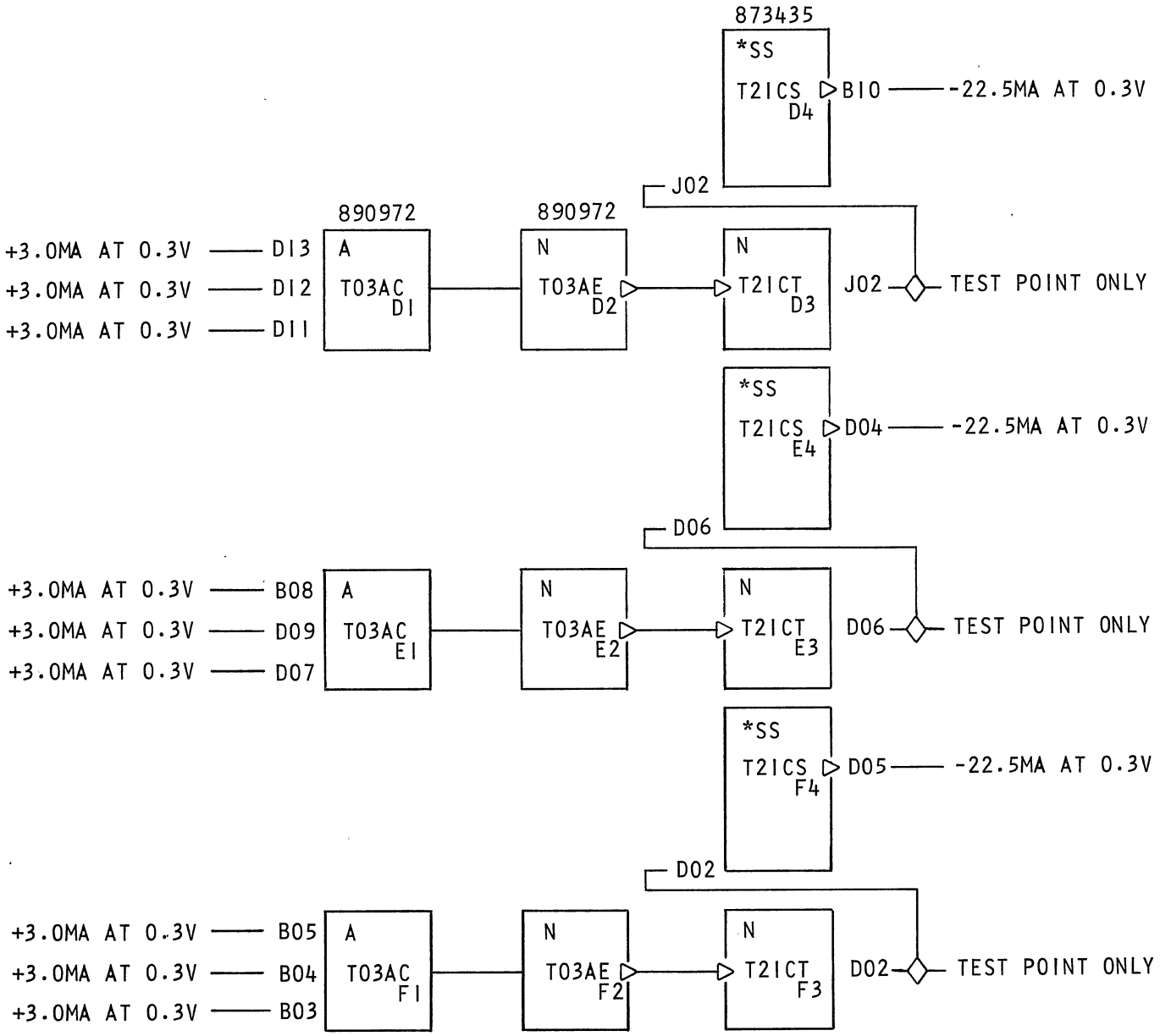
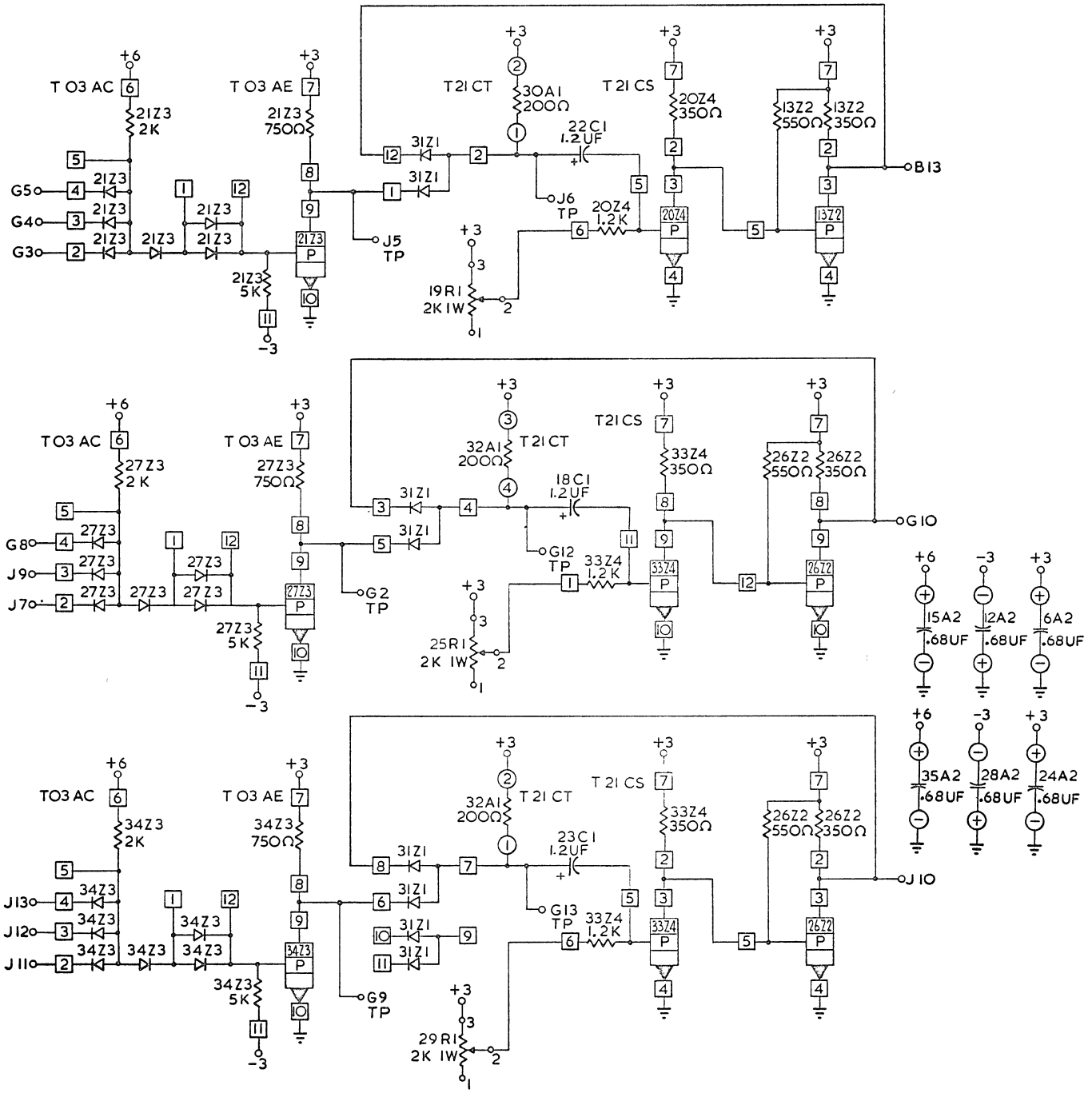
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6-VARIABLE SS 780US TO 2.07MS

6-VARIABLE SS 780US TO 2.07MS

P/N	5806150
EC	168034



P/N	5806150
EC	168034

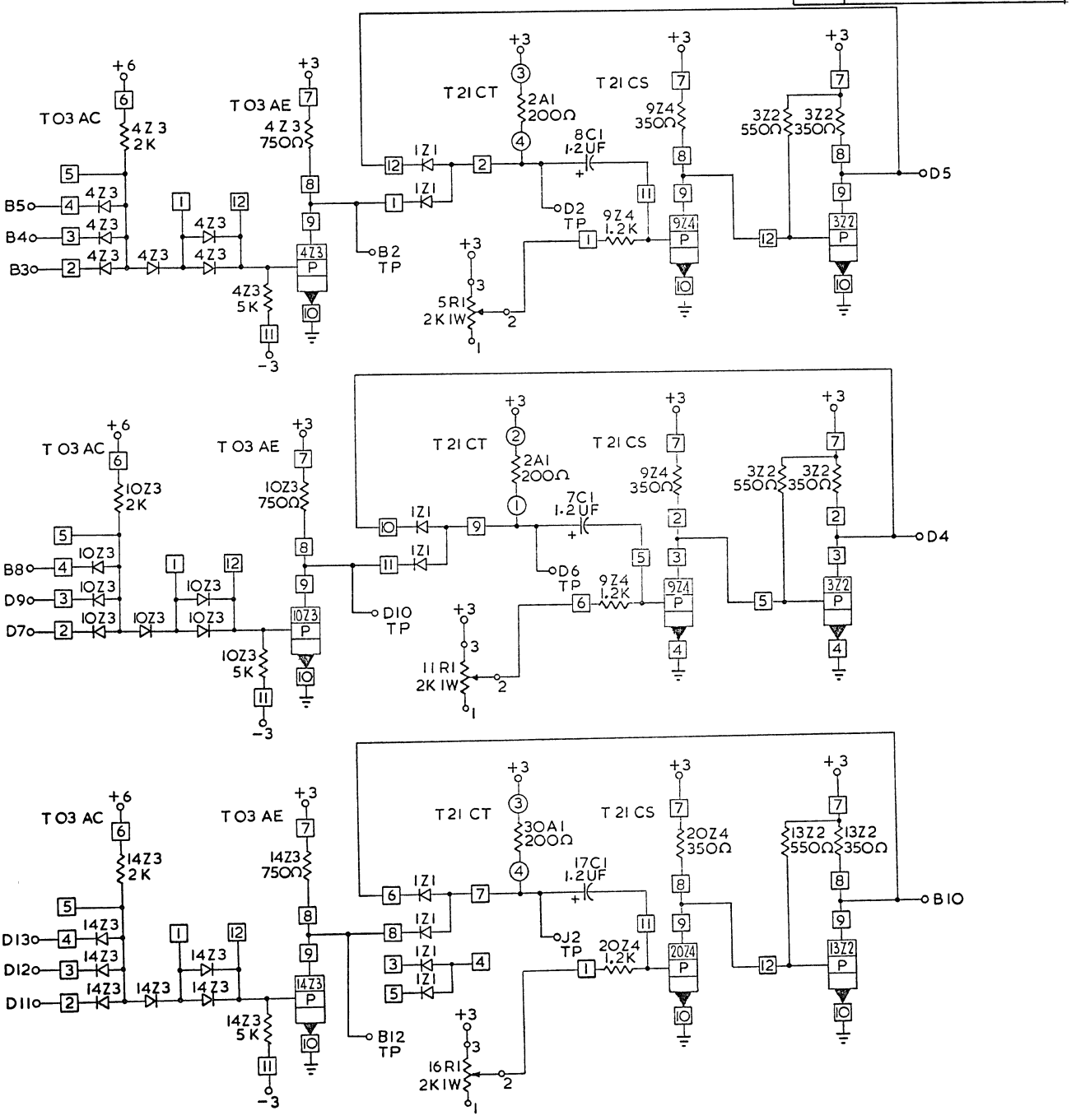


Printed in U.S.A.

LMH Cat.	0-2860 Subject	397 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
6-VARIABLE SS 780US TO 2.07MS

P/N	5806150
EC	168034



THE VOLTAGE PINS: B11-G11, B06-G06, D08-J08, D03-J03 ARE BUSSED.

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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-2W, 2W AOI HPD WO/L

LMH Cat.	0-2860 Subject	398 Suffix

IBM

Location

Manufacturing Specification

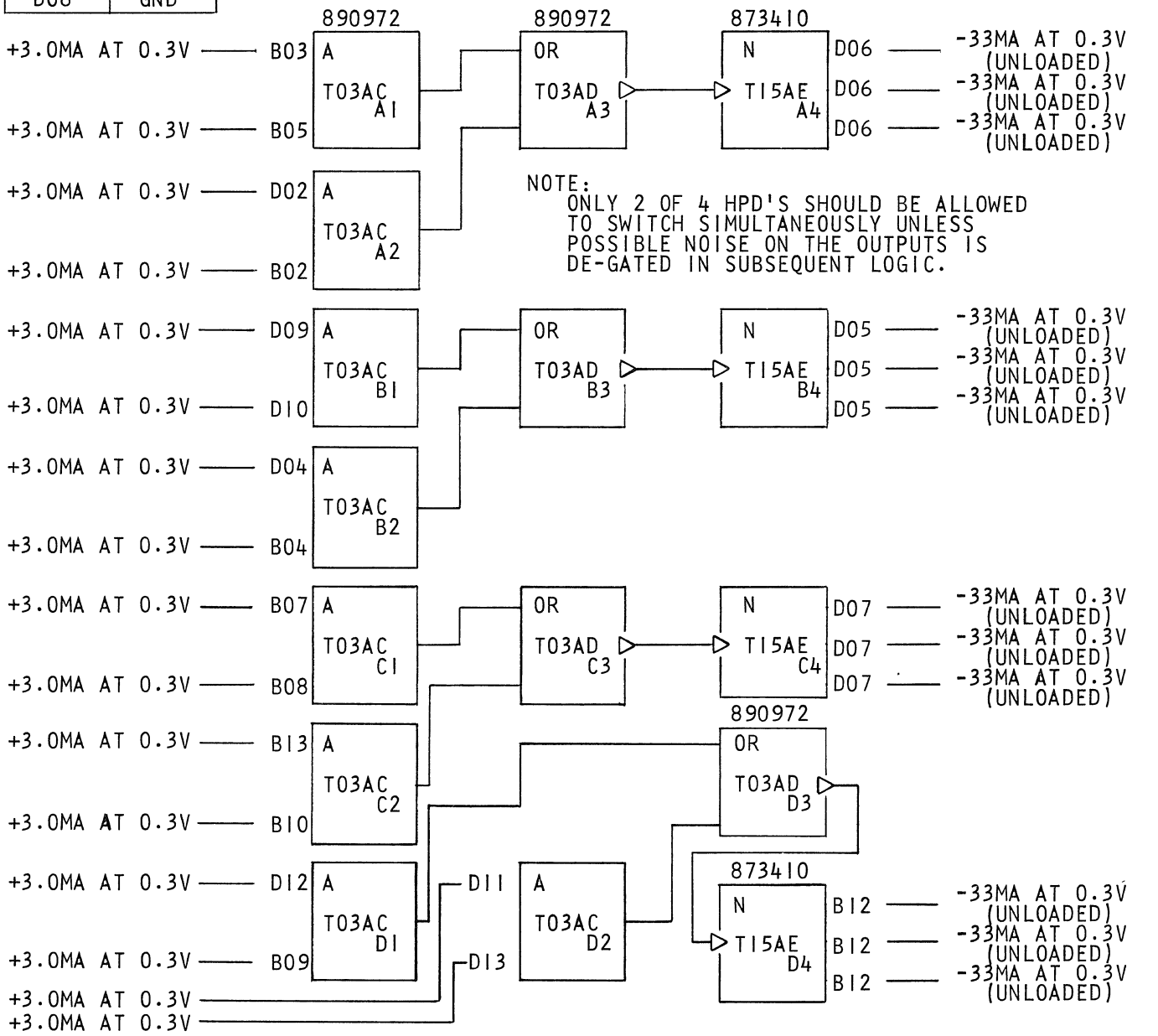
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

4-2W, 2W AOI HPD WO/L

CATEGORY CODE

T03, T15

P/N	5806194
EC	164996
STANDARD RESTRICTED	
CARD SIZE	1-12



06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
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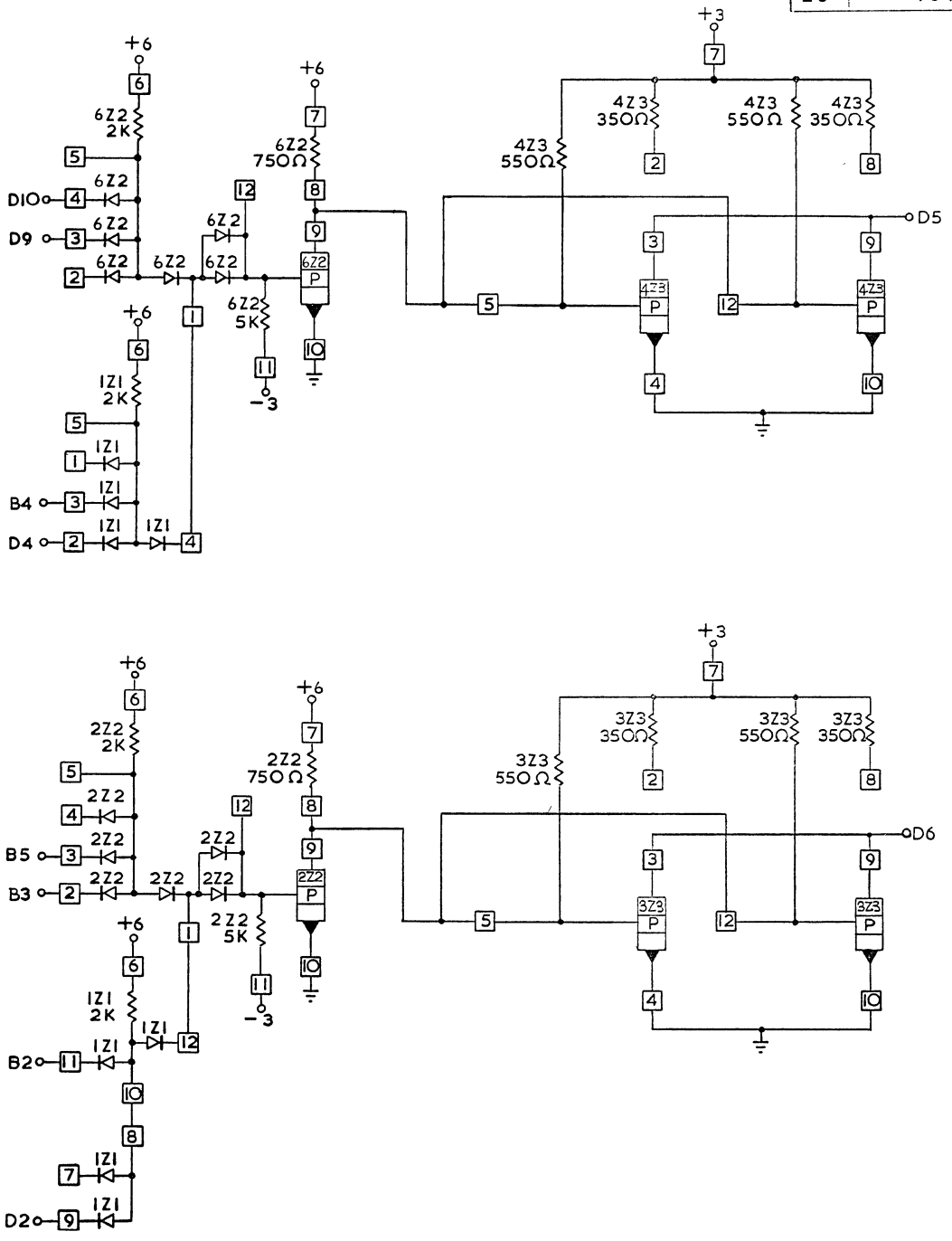
LMH Cat.	0-2860 Subject	398 Suffix

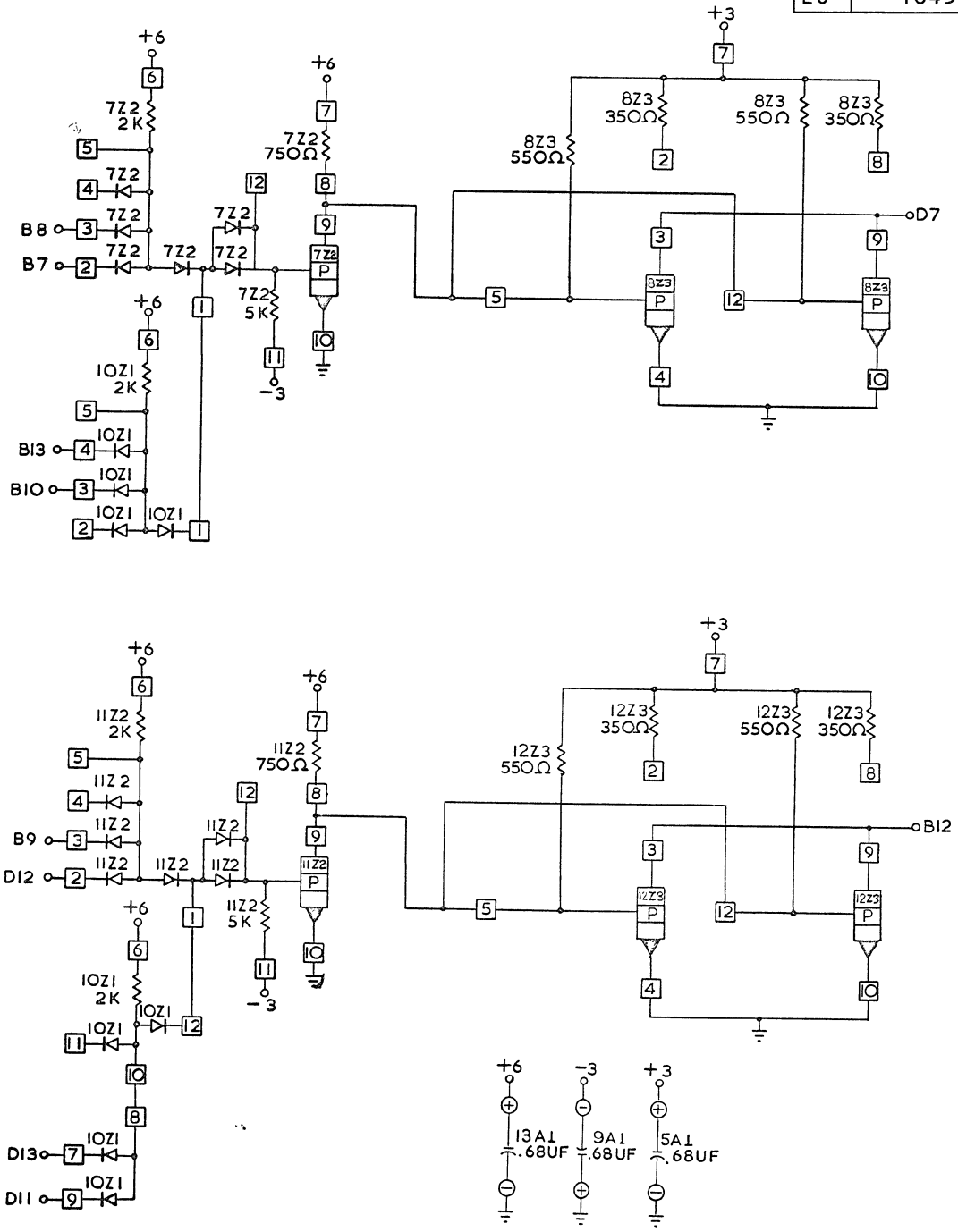
SLR LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
4-2W, 2W AOI HPD WO/L

P/N	5806194
EC	164996



Page 2	Date Jan. 67

P/N	5806194
EC	164996



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
PRE-DRIVER I AMP 48V SOLENOID DRIVER

LMH	0-2860	399
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D08	GND

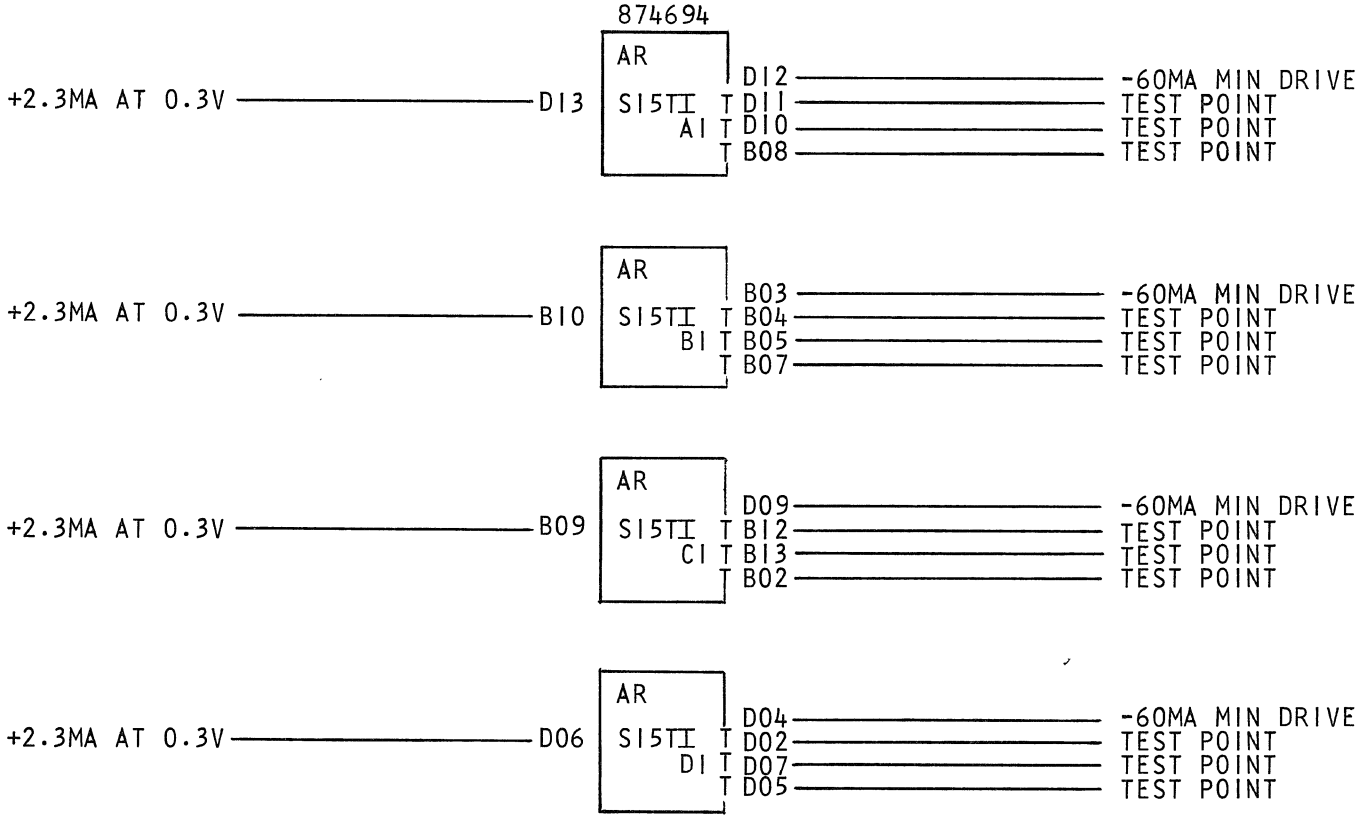
PRE-DRIVER I AMP 48V SOLENOID DRIVER

CATEGORY CODE

S15

P/N	5806287	
EC	167055A	
SPECIAL RESTRICTED		
CARD SIZE		1-12

874694



06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
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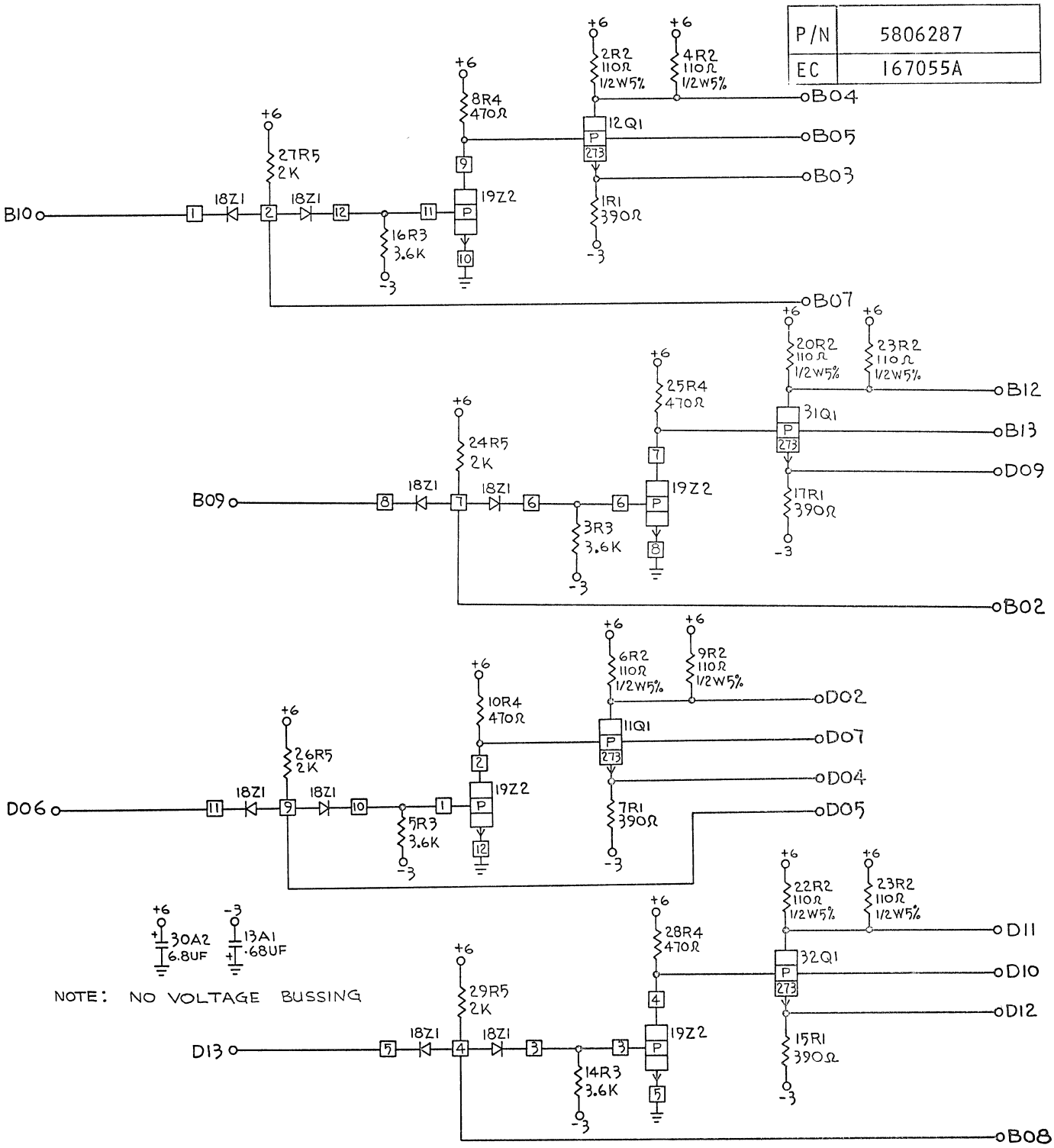
LMH Cat.	0-2860 Subject	399 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
PRE-DRIVER I AMP 48V SOLENOID DRIVER

P/N	5806287
EC	167055A



Page 2	Date 1-67

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
300 MA DRIVER

LMH	0-2860	400
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

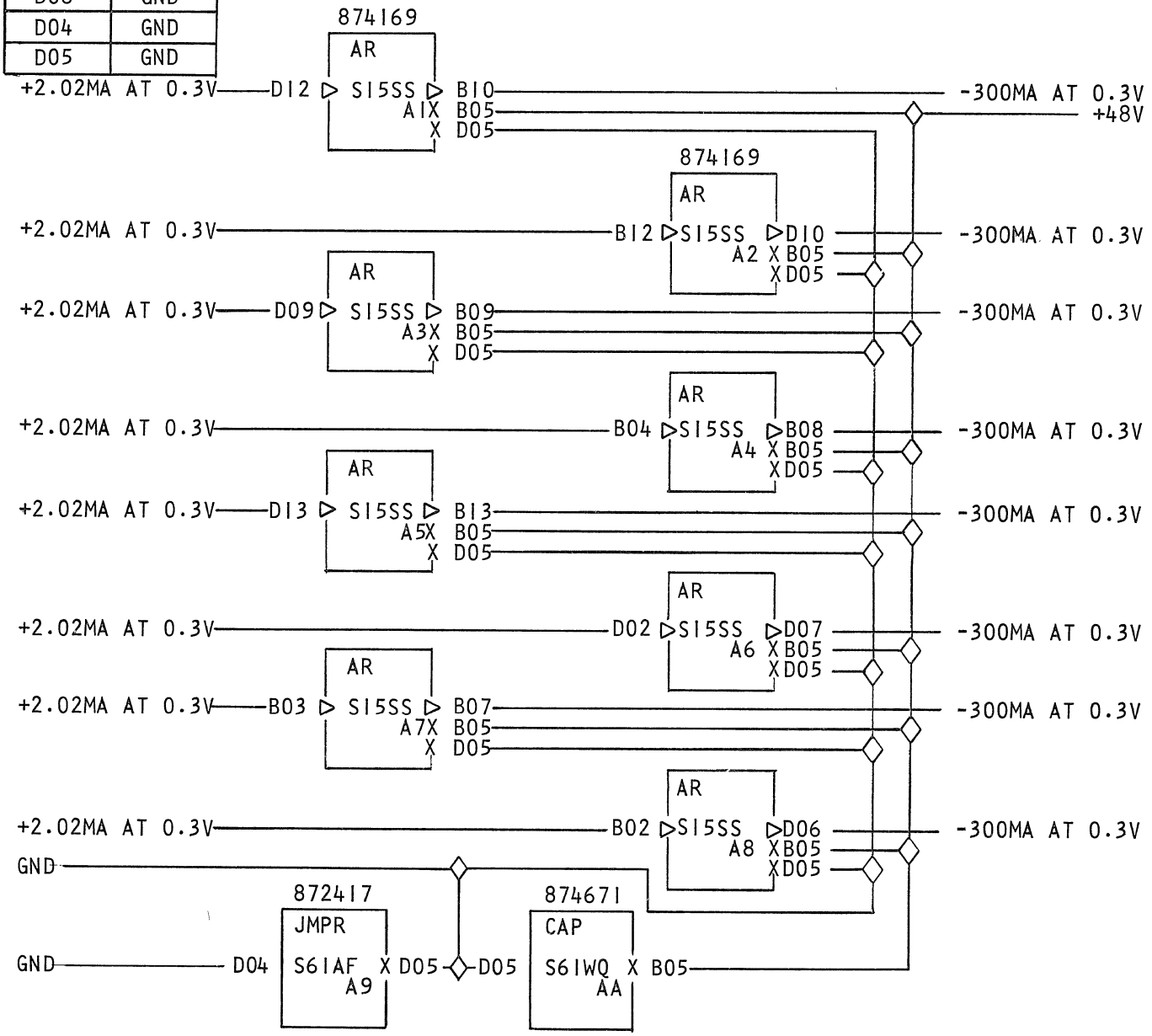
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B05	+48
D08	GND
D04	GND
D05	GND

300 MA DRIVER

CATEGORY CODE

S15

P/N	5806290
EC	167061A
SPECIAL RESTRICTED	
CARD SIZE	1-12



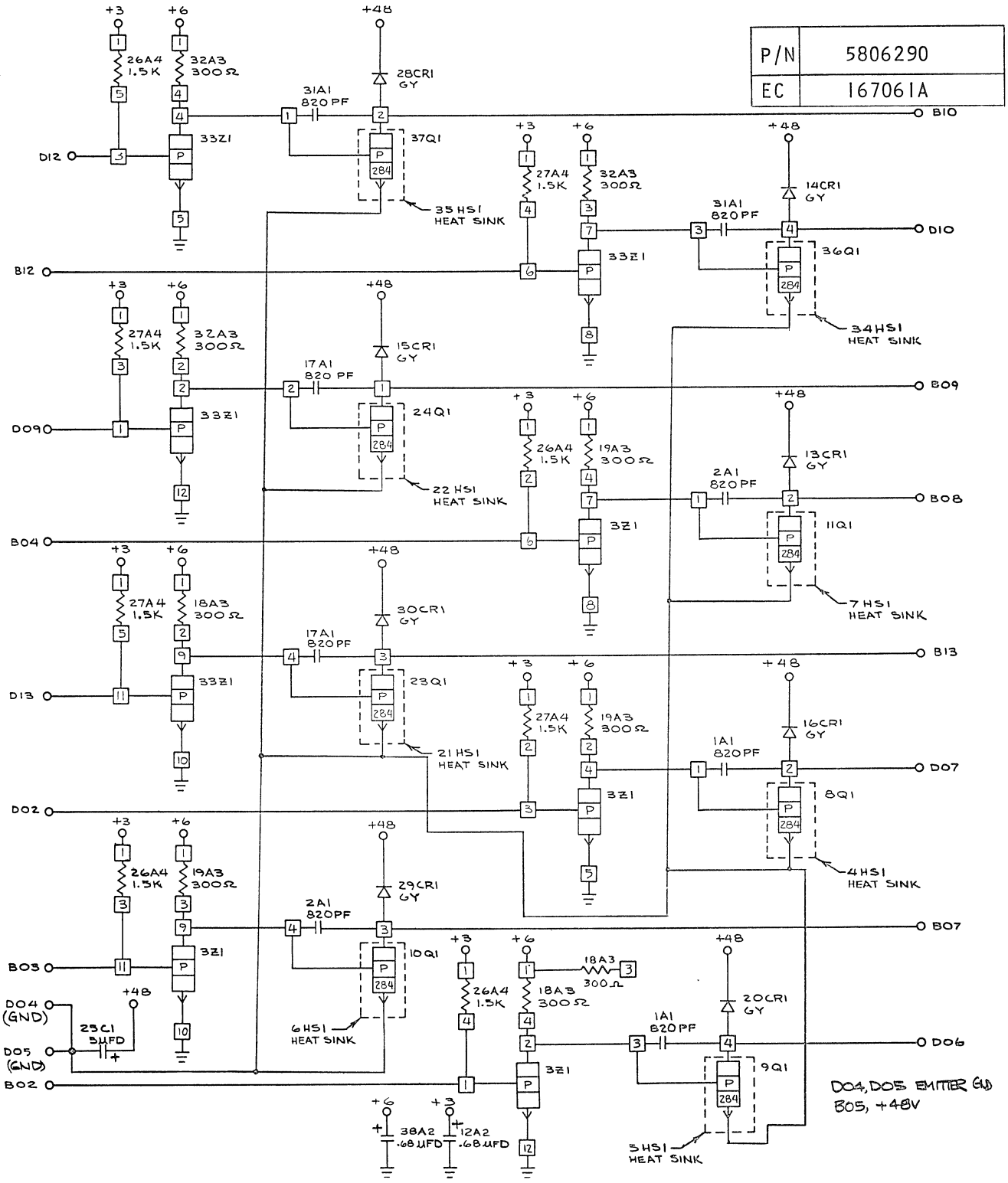
06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability: ENDICOTT		Responsibility: ENDICOTT	Date: 1-67	Page: 1 OF 2

PRINTED IN USA

LMH Cat.	0-2860 Subject	400 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
300 MA DRIVER

P/N	5806290
EC	167061A



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
11-100 OHM PADDLE CARD RESISTORS

LMH Cat.	0-2860 Subject	402 Suffix

IBM **Location**
Manufacturing Specification

POWER REQUIRED	
VOLTS	PIN
+3	B04, D03, D04
-3	B06, B07, D07
+6	B11, B12, B13
GND	D08, B08

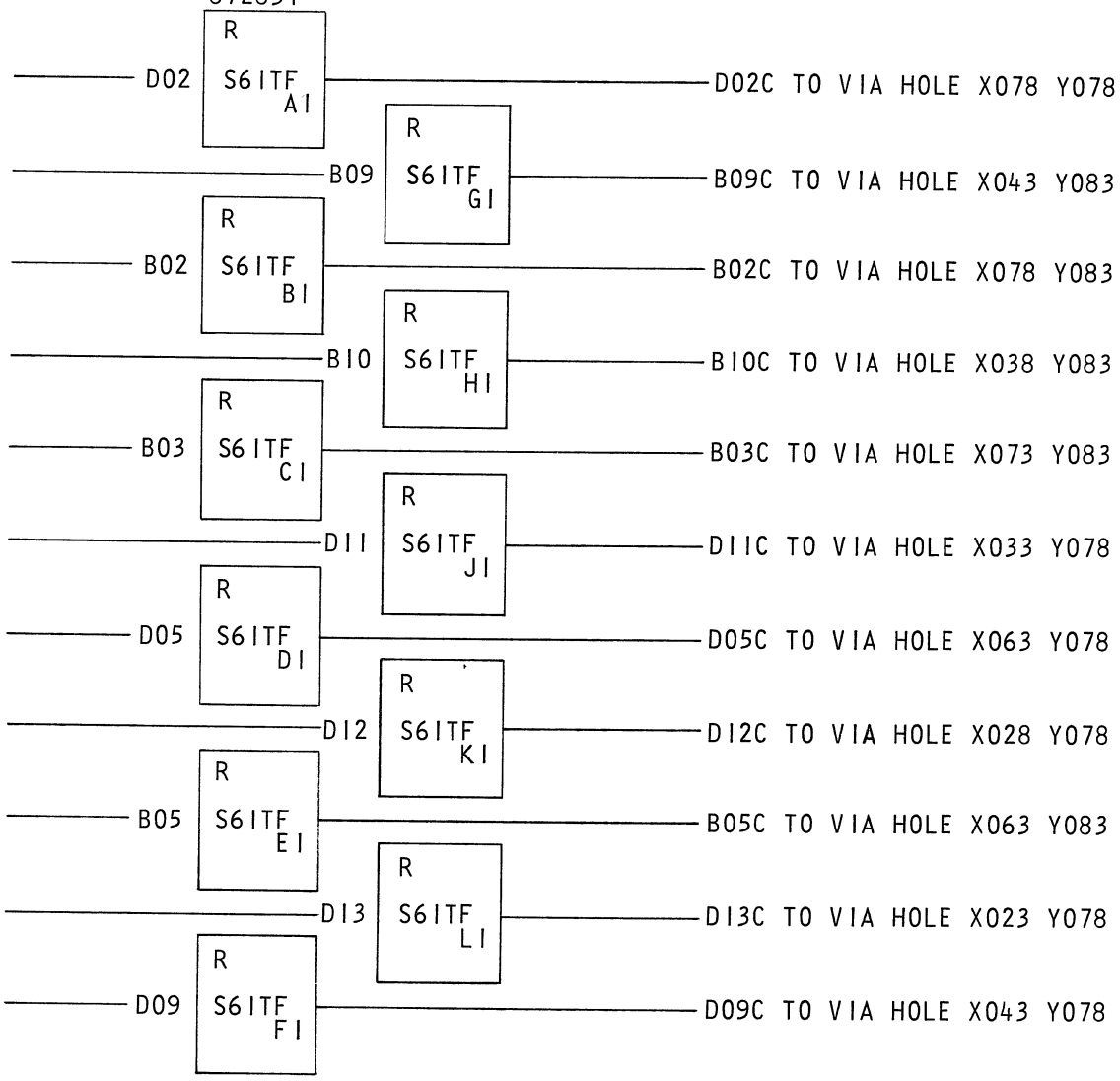
11-100 OHM PADDLE CARD RESISTORS

CATEGORY CODE

S61

P/N	5807027
EC	168410
STANDARD RESTRICTED	
CARD SIZE	1-12

872831

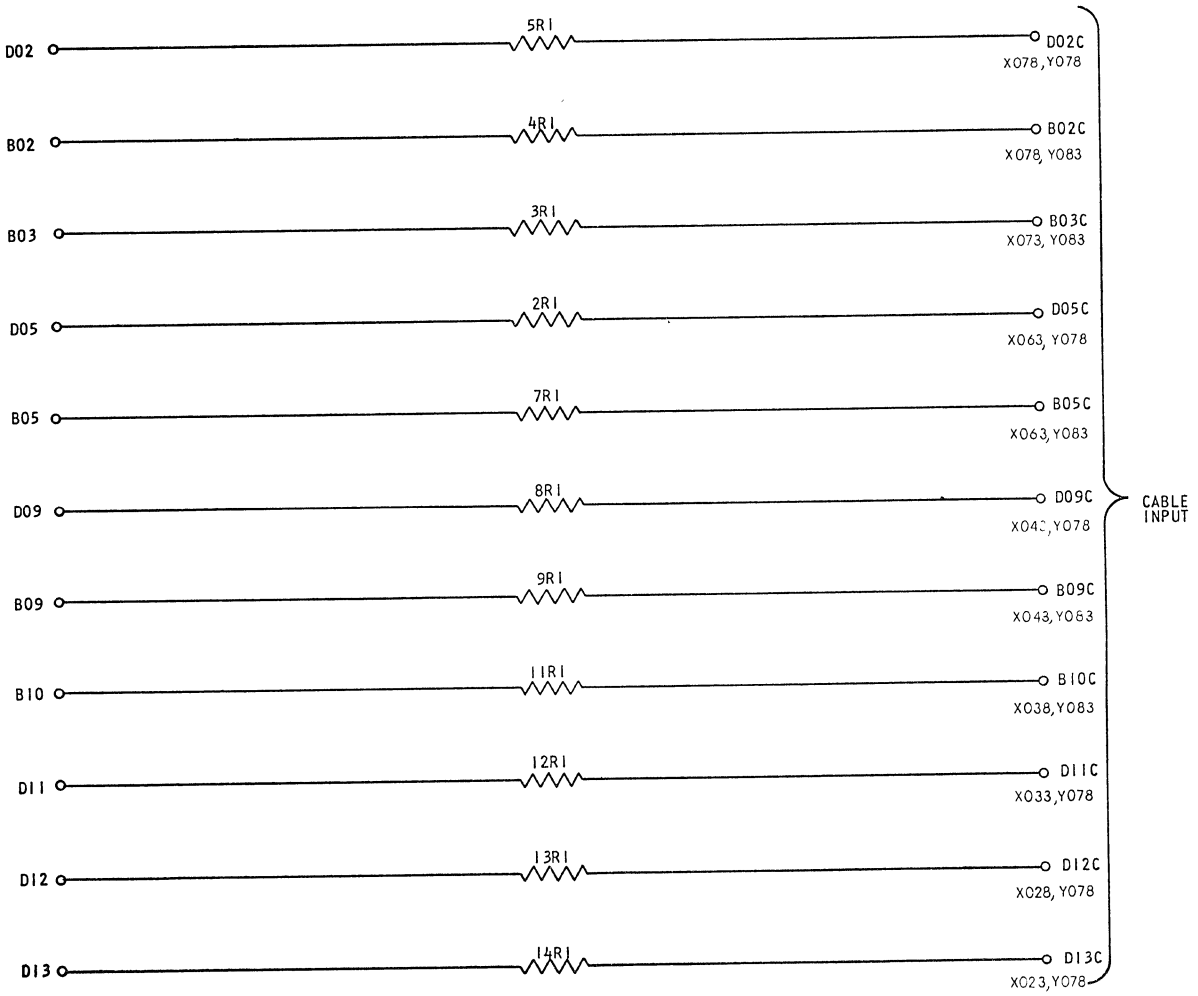


NOTE: ALL RESISTORS 1/4W, ± 5%

LMH Cat.	0-2860 Subject	402 Suffix

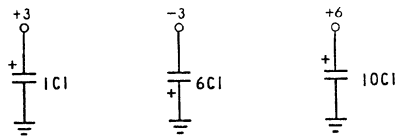
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
11-100 OHM PADDLE CARD RESISTORS

P/N	5807027
EC	168410



ALL RESISTORS
1/4W 5% 100Ω P/N 595359

ALL CAPACITORS
.33 UF ±20% P/N 222076



NOTE
+3-B04, D04, D03 BUSSED
-3-B06, B07, D07 BUSSED
+6-B11, B12, B13 BUSSED
GND-D08, B08 BUSSED

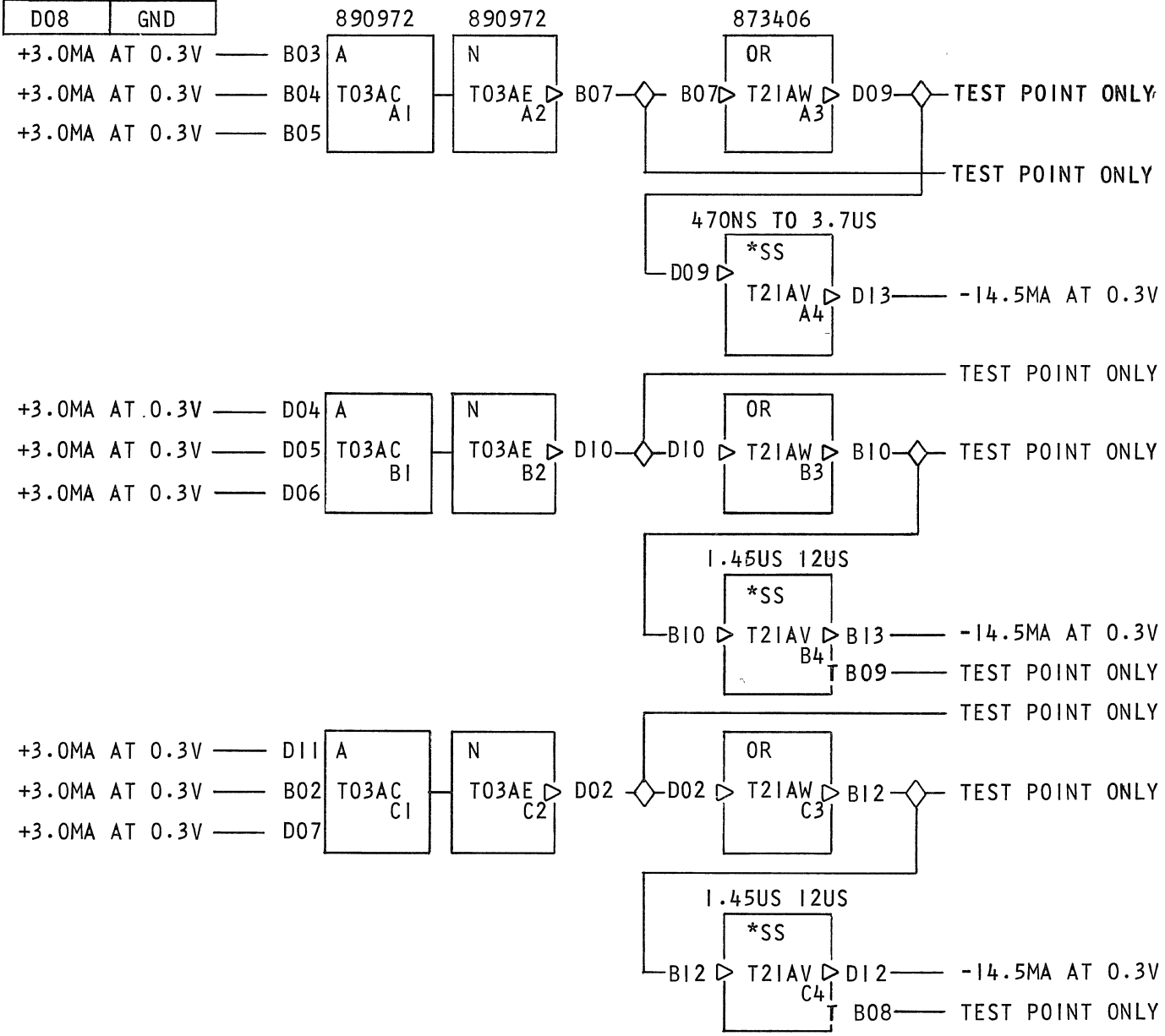
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

1-SS 470NS TO 3.7US 2-SS 1.45 TO 12US

CATEGORY CODE

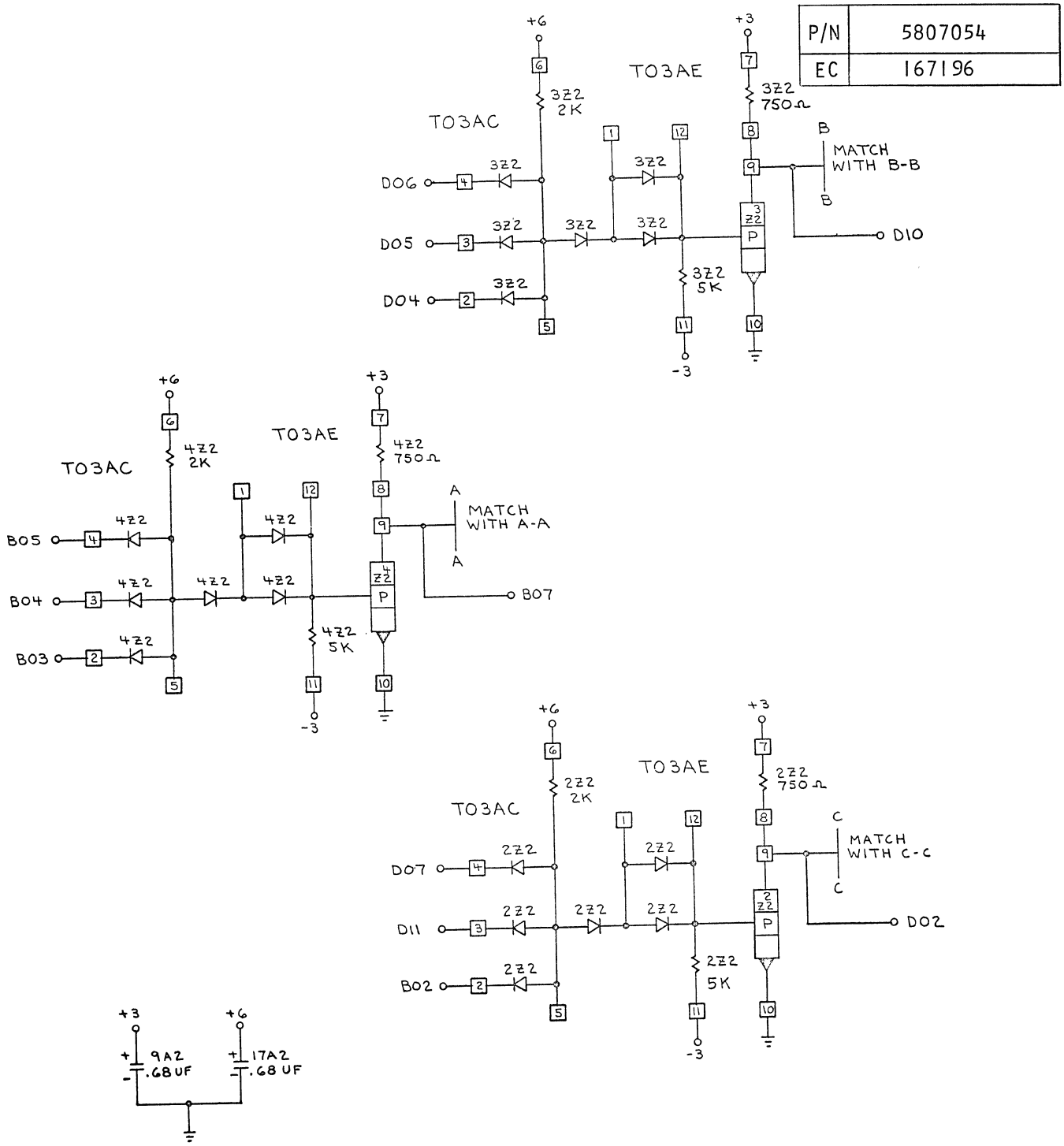
T03

P/N	5807054
EC	167196
STANDARD RESTRICTED	
CARD SIZE	1-12

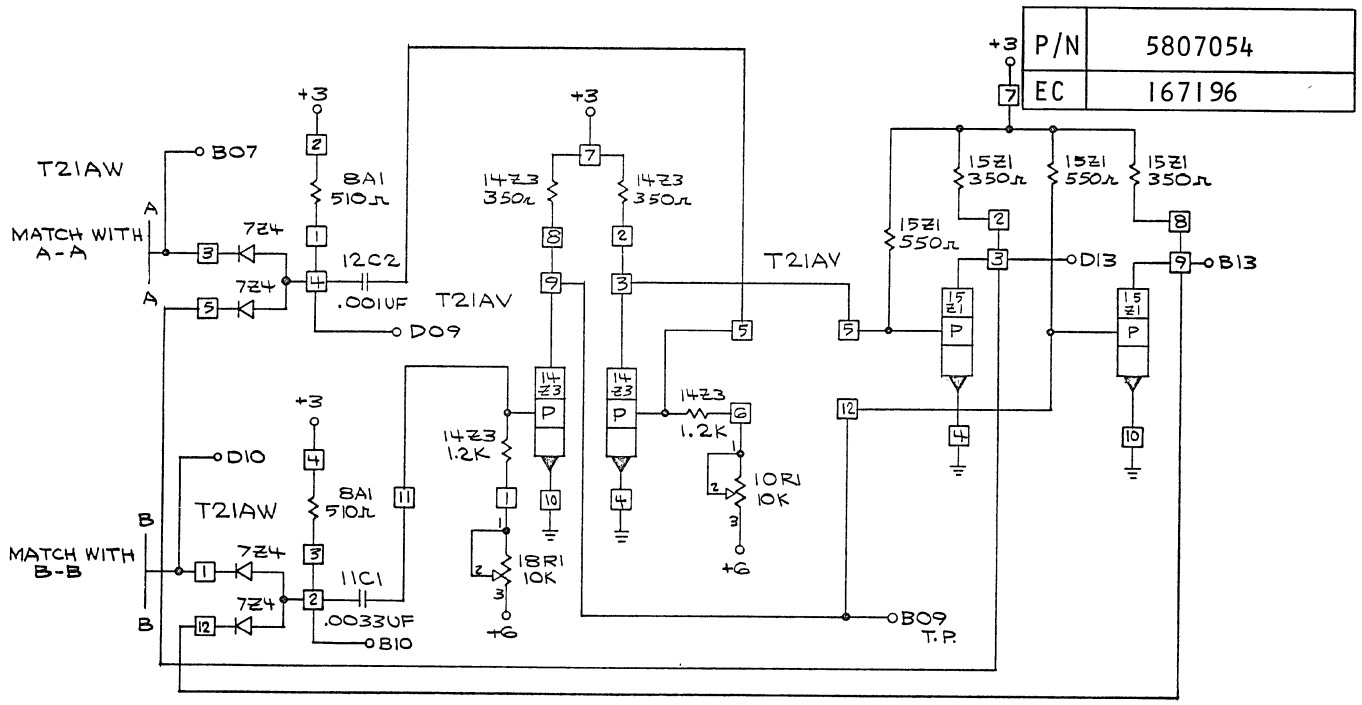


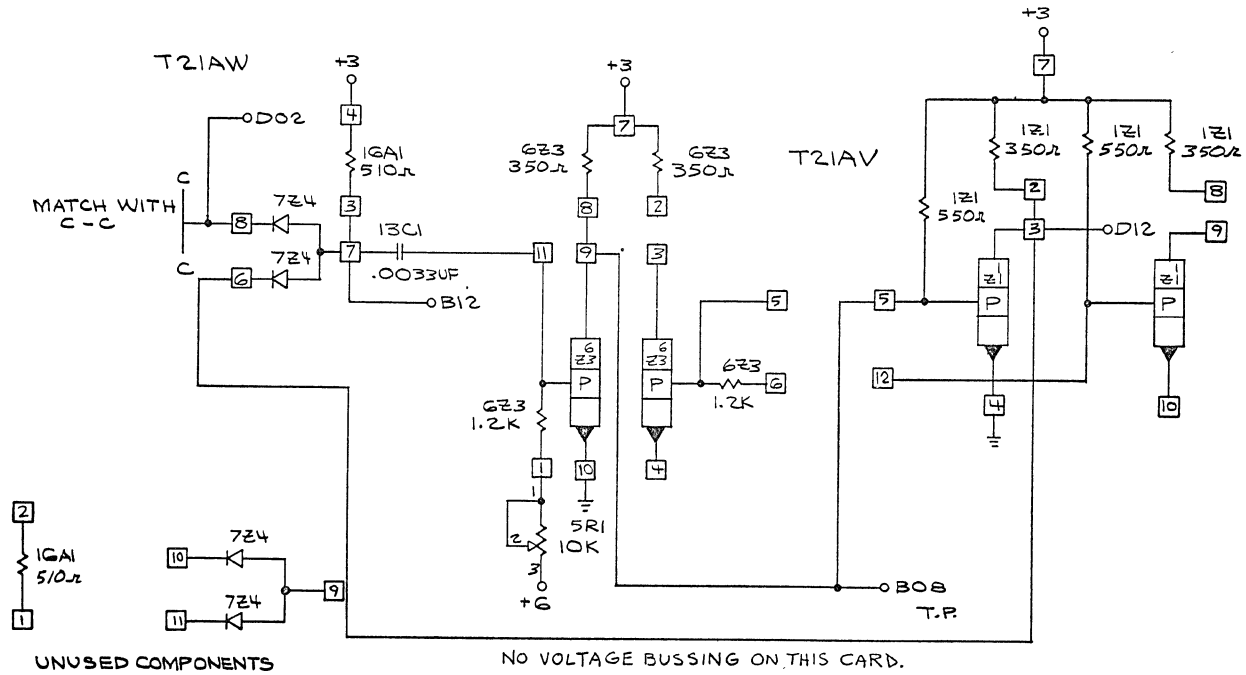
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1-SS 470NS TO 3.7US 2-SS 1.45 TO 12US

P/N	5807054
EC	167196



P/N	5807054
EC	167196



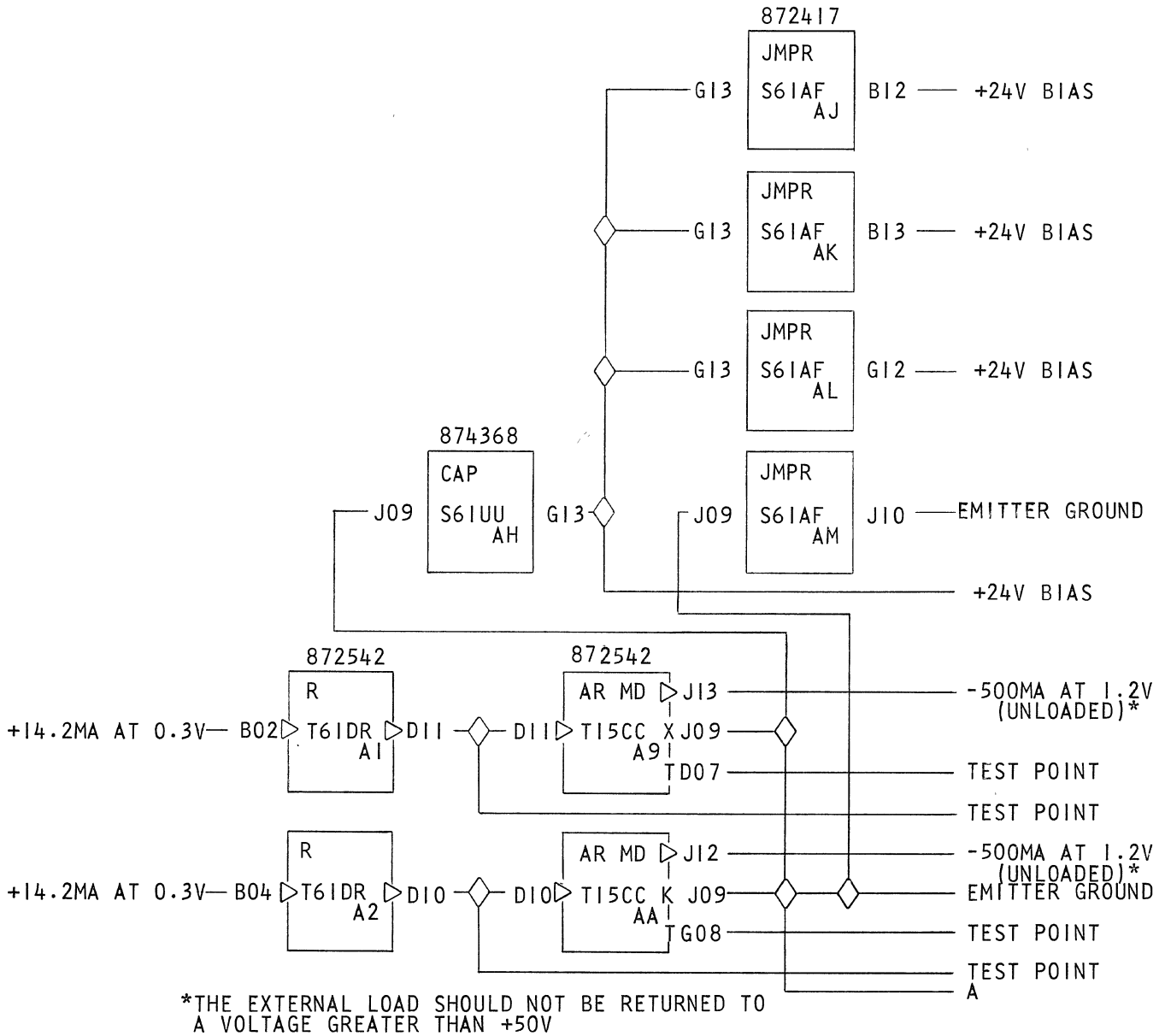


POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D08	GND

8-0.5 AMP DRIVER
CATEGORY CODE

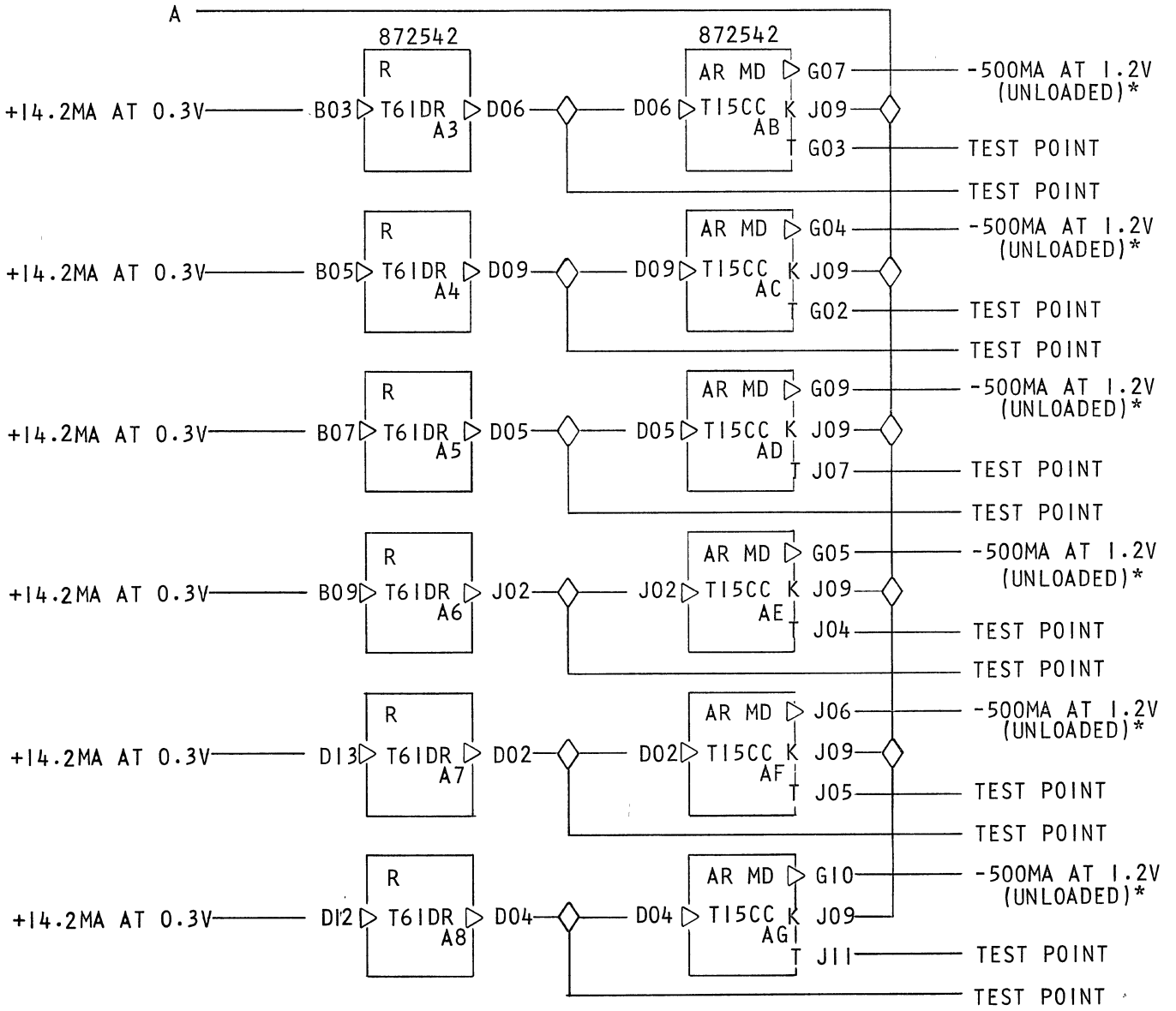
T61	T15

P/N	5807138
EC	165077
STANDARD	ACTIVE
CARD SIZE	2-24

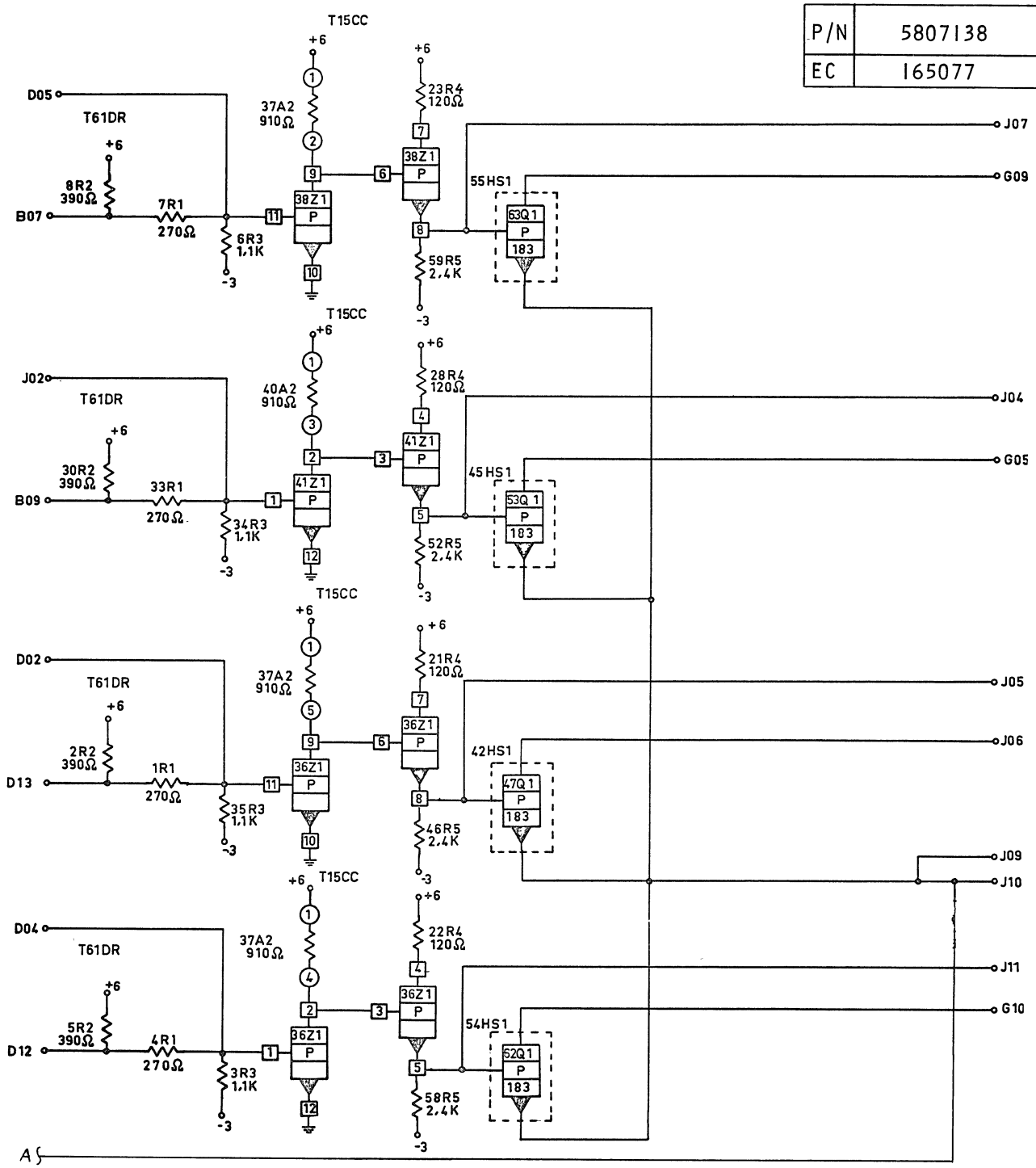


8-0.5 AMP DRIVER	
T61	T15

P/N	5807138
EC	165077

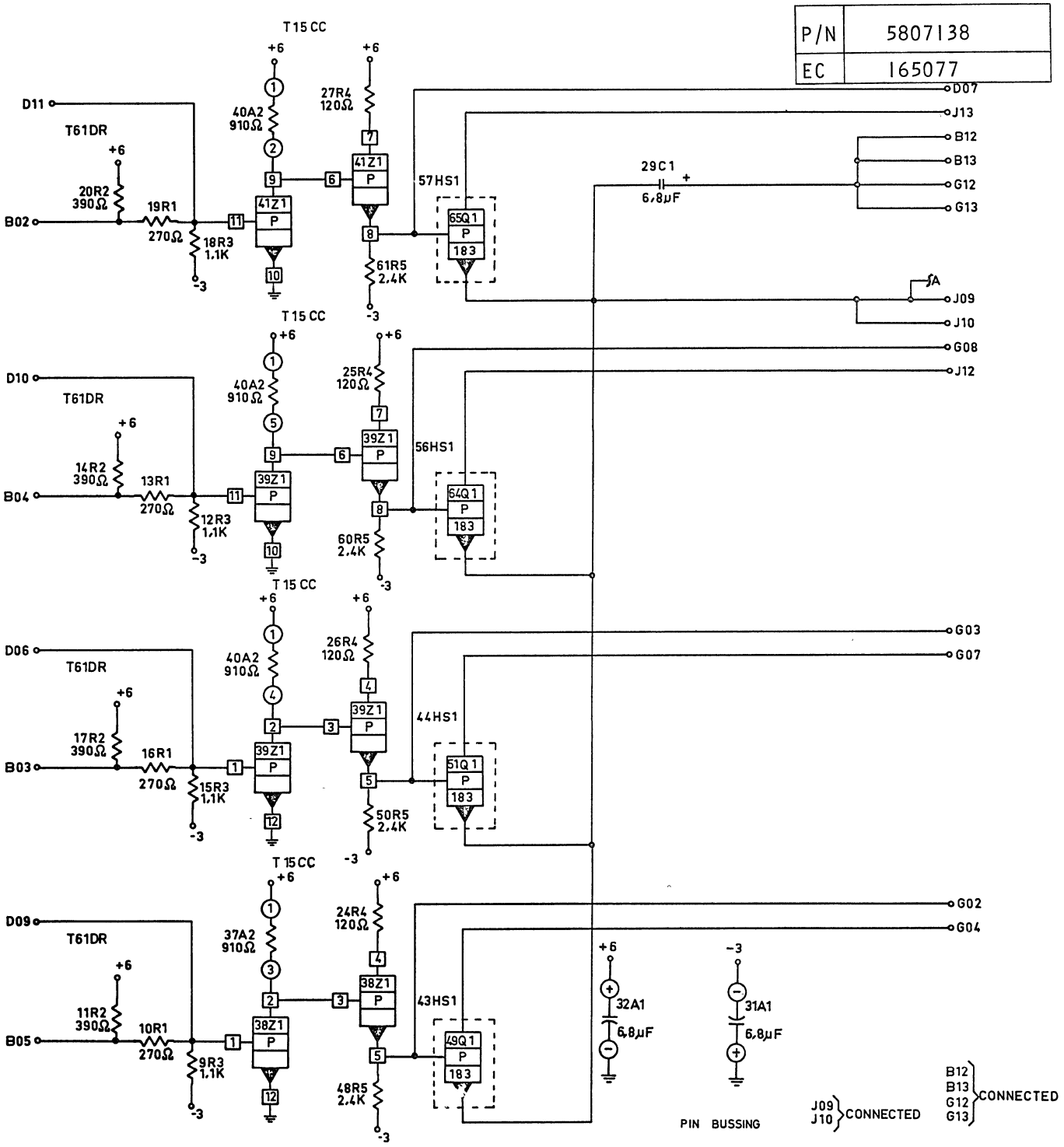


P/N	5807138
EC	165077



LMH Cat.	0-2860 Subject	404 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 8-0.5 AMP DRIVER

P/N	5807138
EC	165077



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2.5 AMP DRIVER

LMH Cat.	0-2860 Subject	405 Suffix

IBM Location Manufacturing Specification

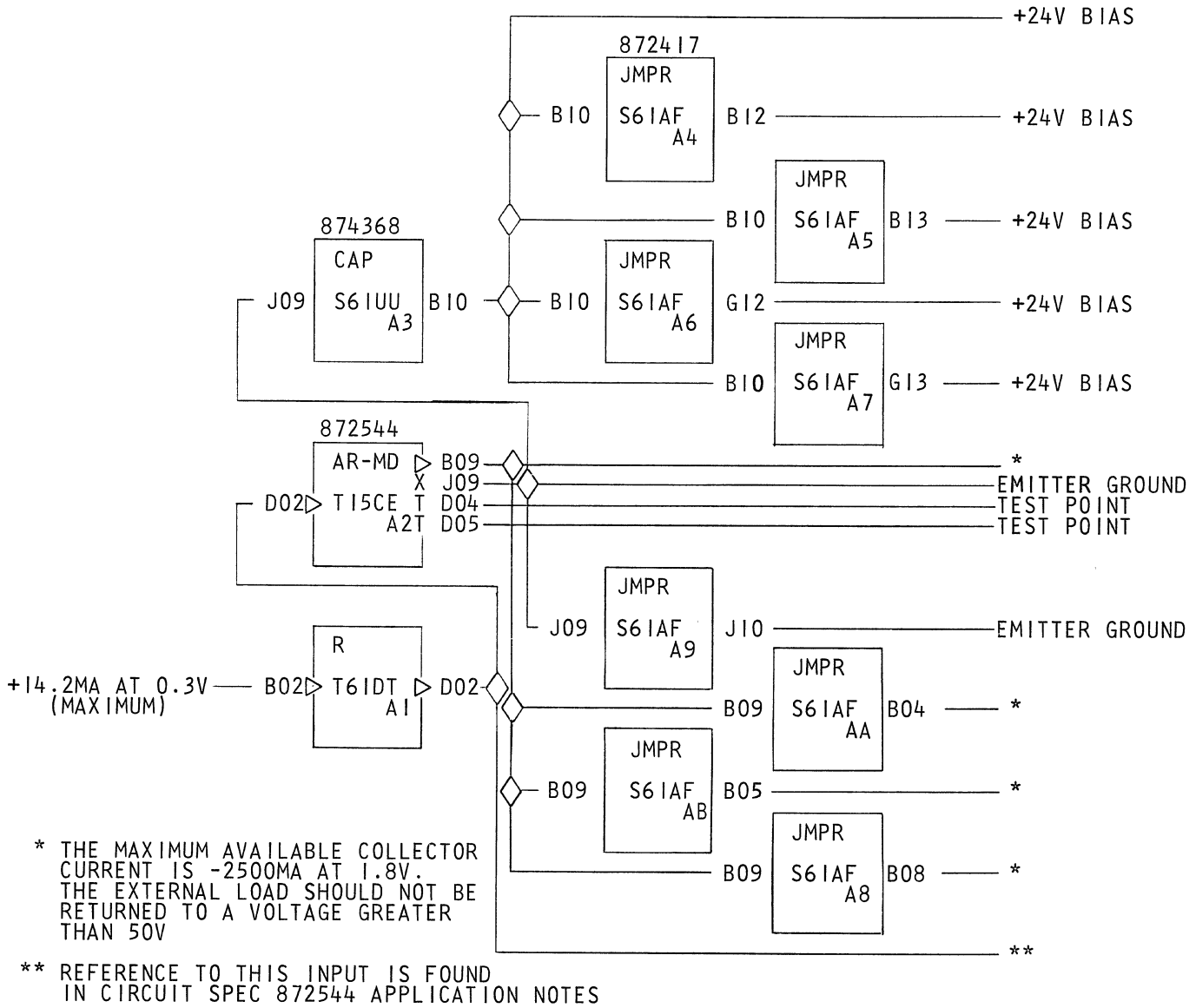
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D08	GND

2.5 AMP DRIVER

CATEGORY CODE

T61	T15

P/N	5807140
EC	167509
STANDARD RESTRICTED	
CARD SIZE	2-24



* THE MAXIMUM AVAILABLE COLLECTOR CURRENT IS -2500MA AT 1.8V. THE EXTERNAL LOAD SHOULD NOT BE RETURNED TO A VOLTAGE GREATER THAN 50V

** REFERENCE TO THIS INPUT IS FOUND IN CIRCUIT SPEC 872544 APPLICATION NOTES

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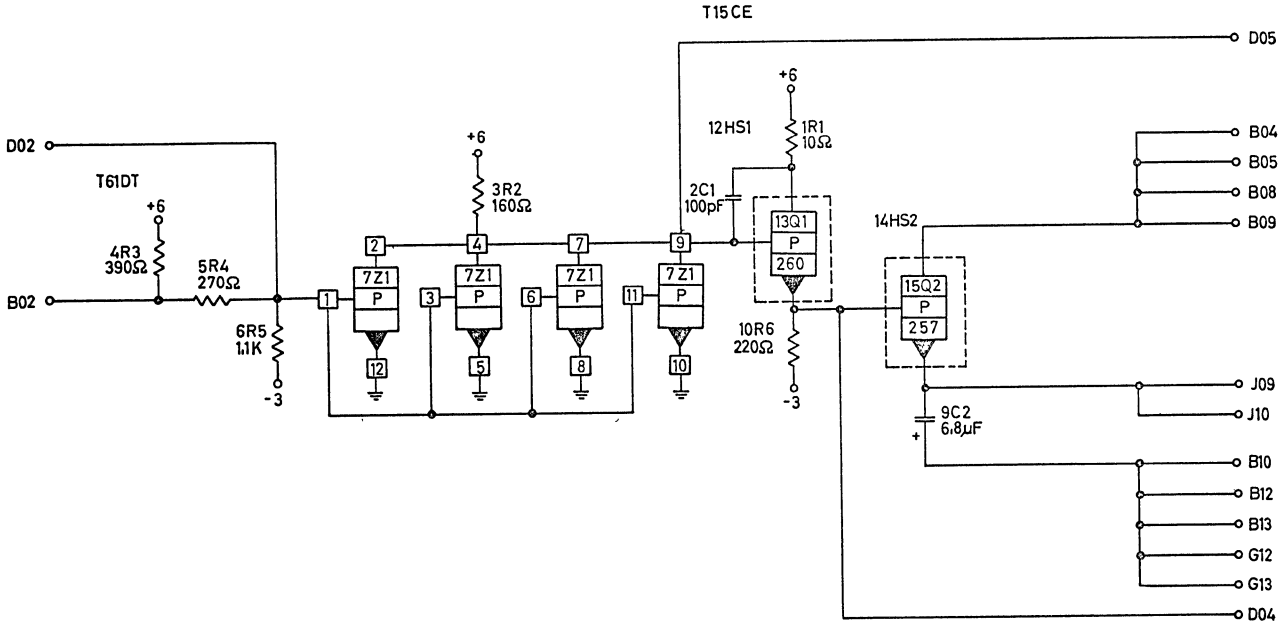
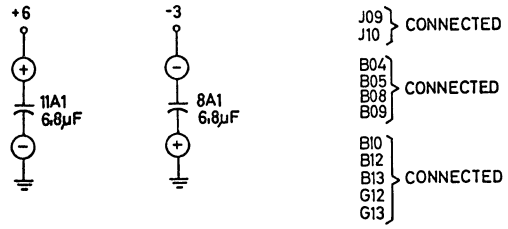
LMH Cat.	0-2860 Subject	405 Suffix	SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING 2.5 AMP DRIVER

P/N	5807140
EC	167509





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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1.0 AMP DRIVER

LMH Cat.	0-2860 Subject	406 Suffix

IBM Location Manufacturing Specification

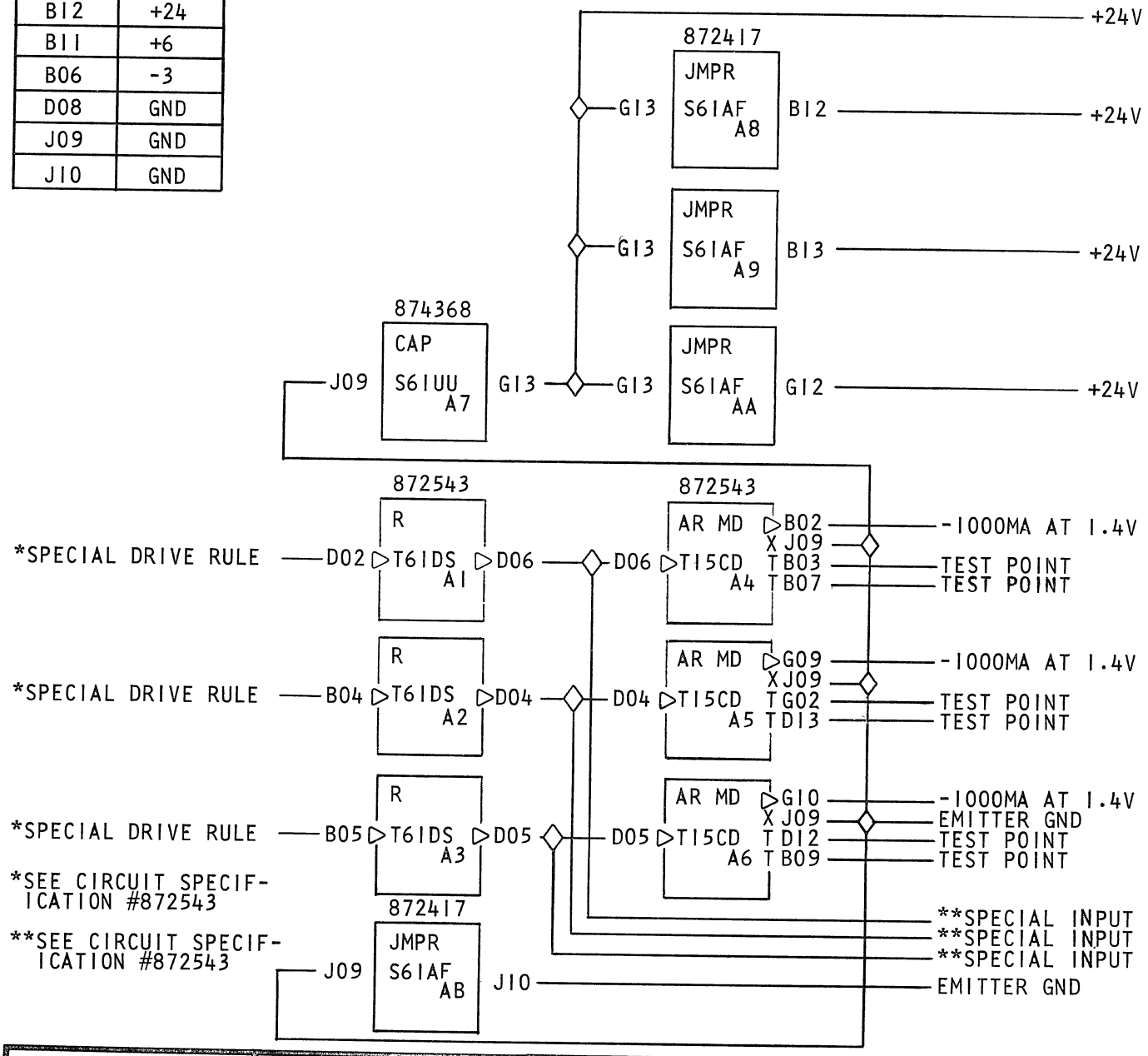
POWER REQUIRED	
PIN	VOLTS
G13	+24
B13	+24
G12	+24
B12	+24
B11	+6
B06	-3
D08	GND
J09	GND
J10	GND

1.0 AMP DRIVER

CATEGORY CODE

T15

P/N	5807141
EC	165080A
STANDARD	ACTIVE
CARD SIZE	2-24



06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
ENDICOTT Applicability		ENDICOTT Responsibility	1-67 Date	1 of 2 Page

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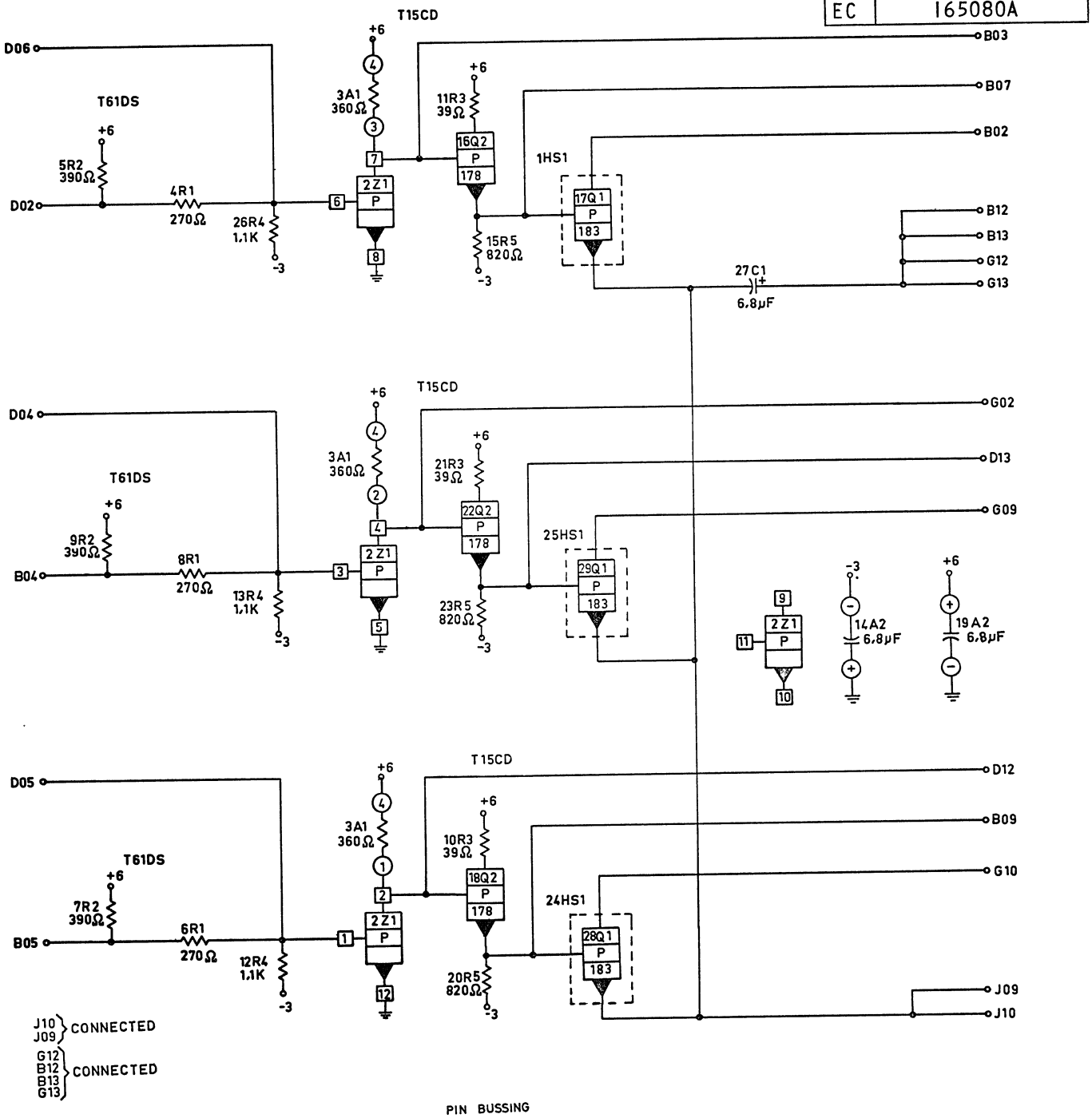
LMH Cat.	0-2860 Subject	406 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
1.0 AMP DRIVER

P/N	5807141
EC	165080A



PIN BUSSING

Page 2	Date 1-67

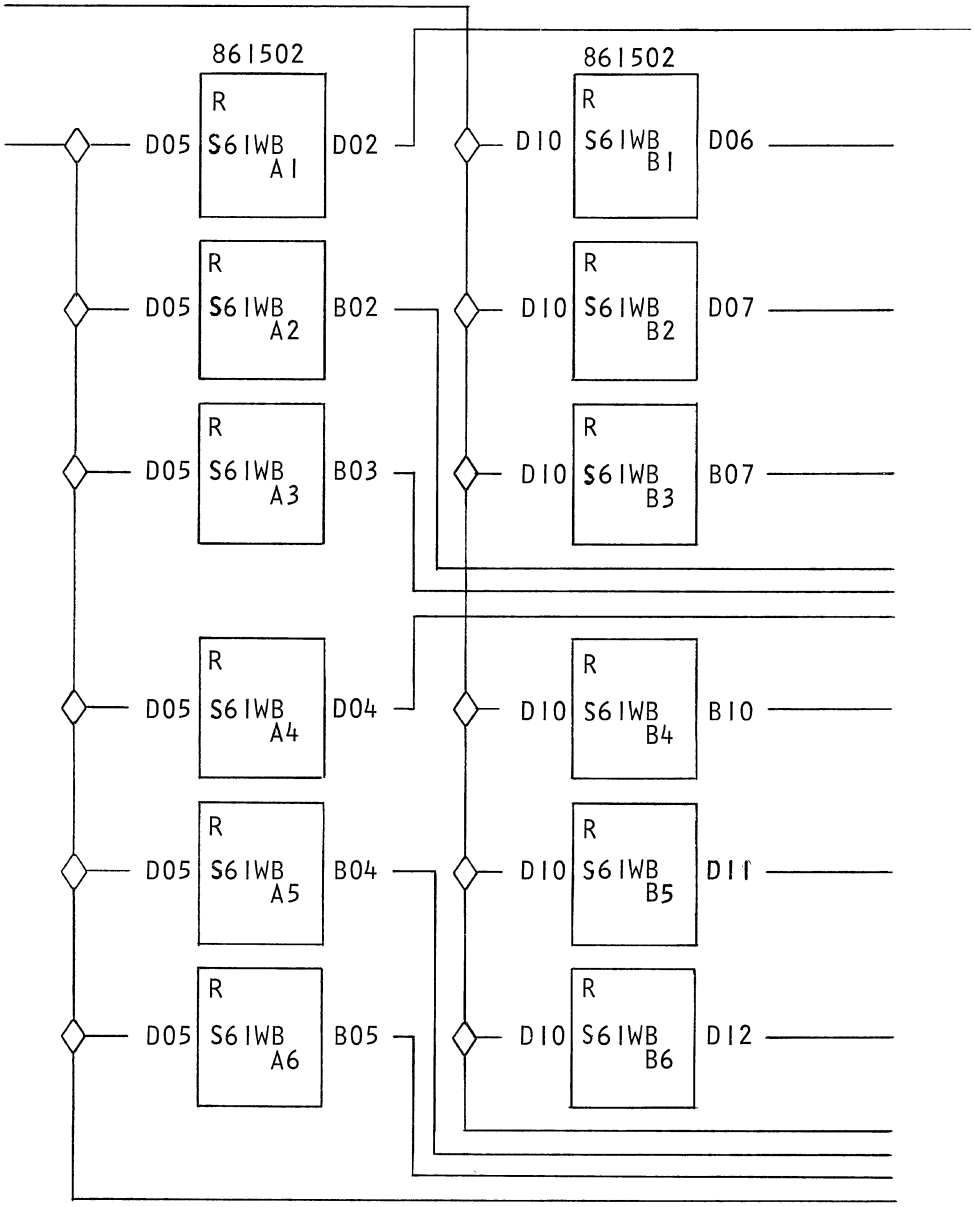
POWER REQUIRED
NONE

18-16K OHM RESISTORS

CATEGORY CODE

S61

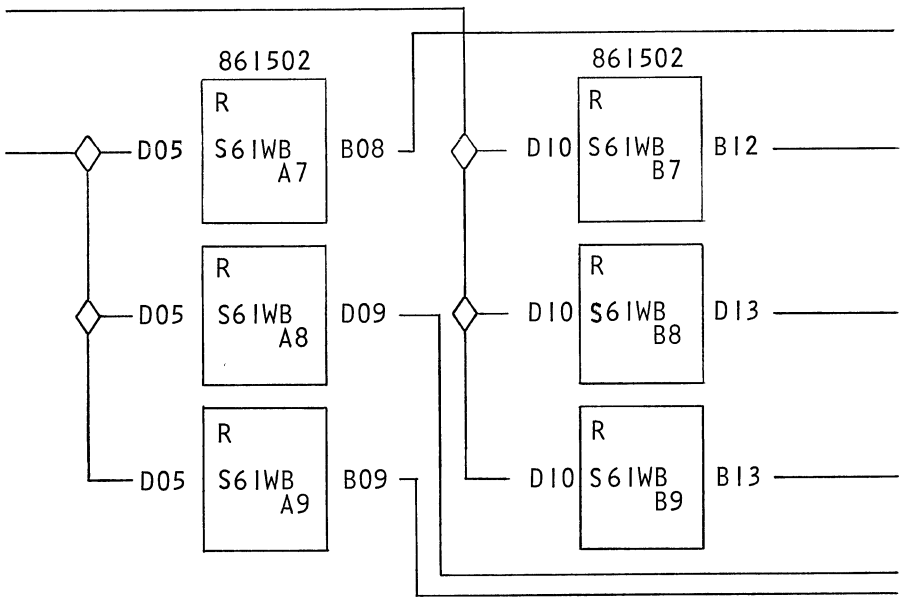
P/N	5807202	
EC	167417	
STANDARD ACTIVE		
CARD SIZE		1-6



18-16K OHM RESISTORS

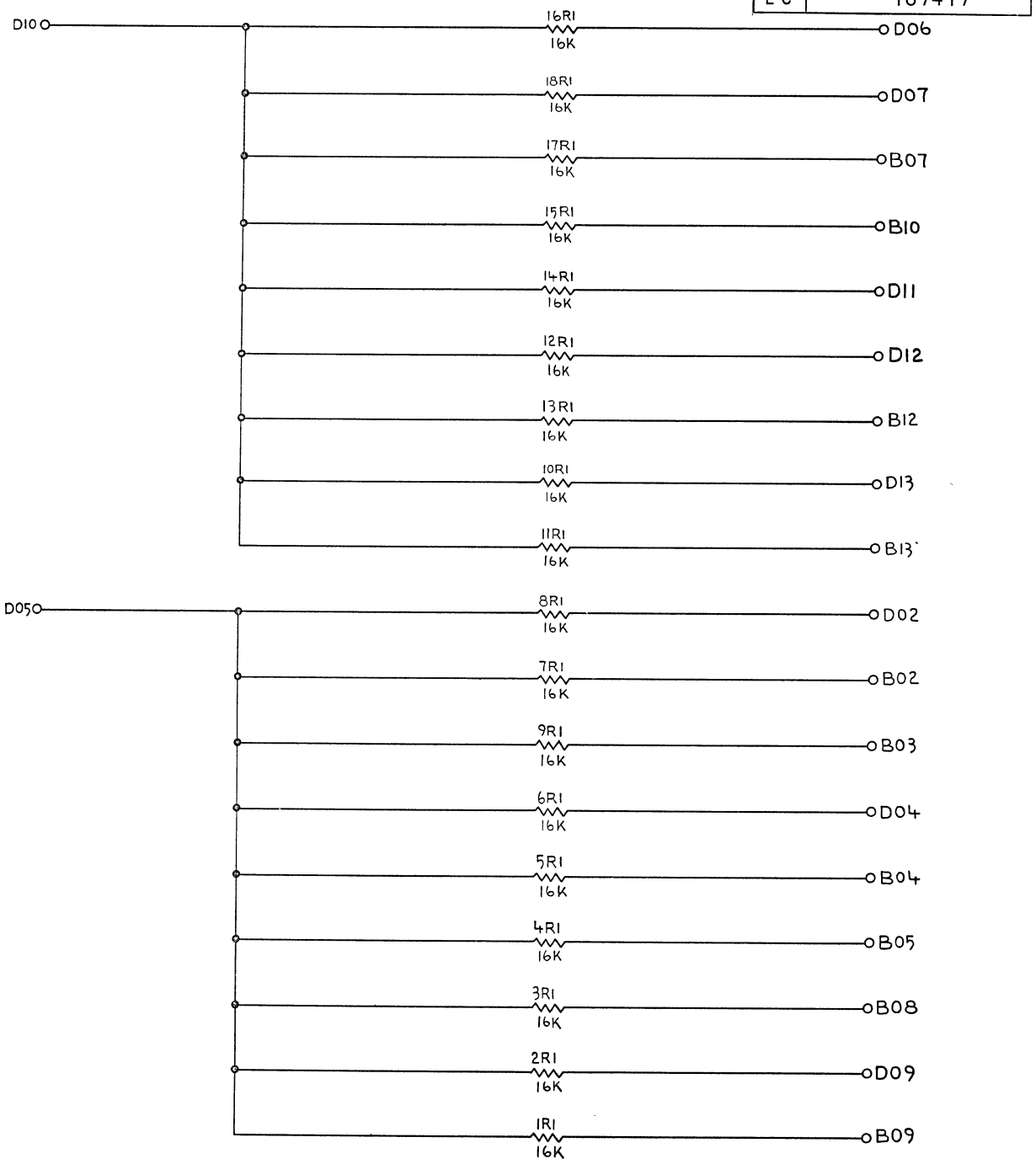
S61

P/N	5807202
EC	167417



NOTE: ALL RESISTORS ARE 1/4W, ±5%

P/N	5807202
EC	167417



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
SIX MPLX DRIVERS

LMH Cat.	0-2860 Subject	411 Suffix

IBM Location Manufacturing Specification

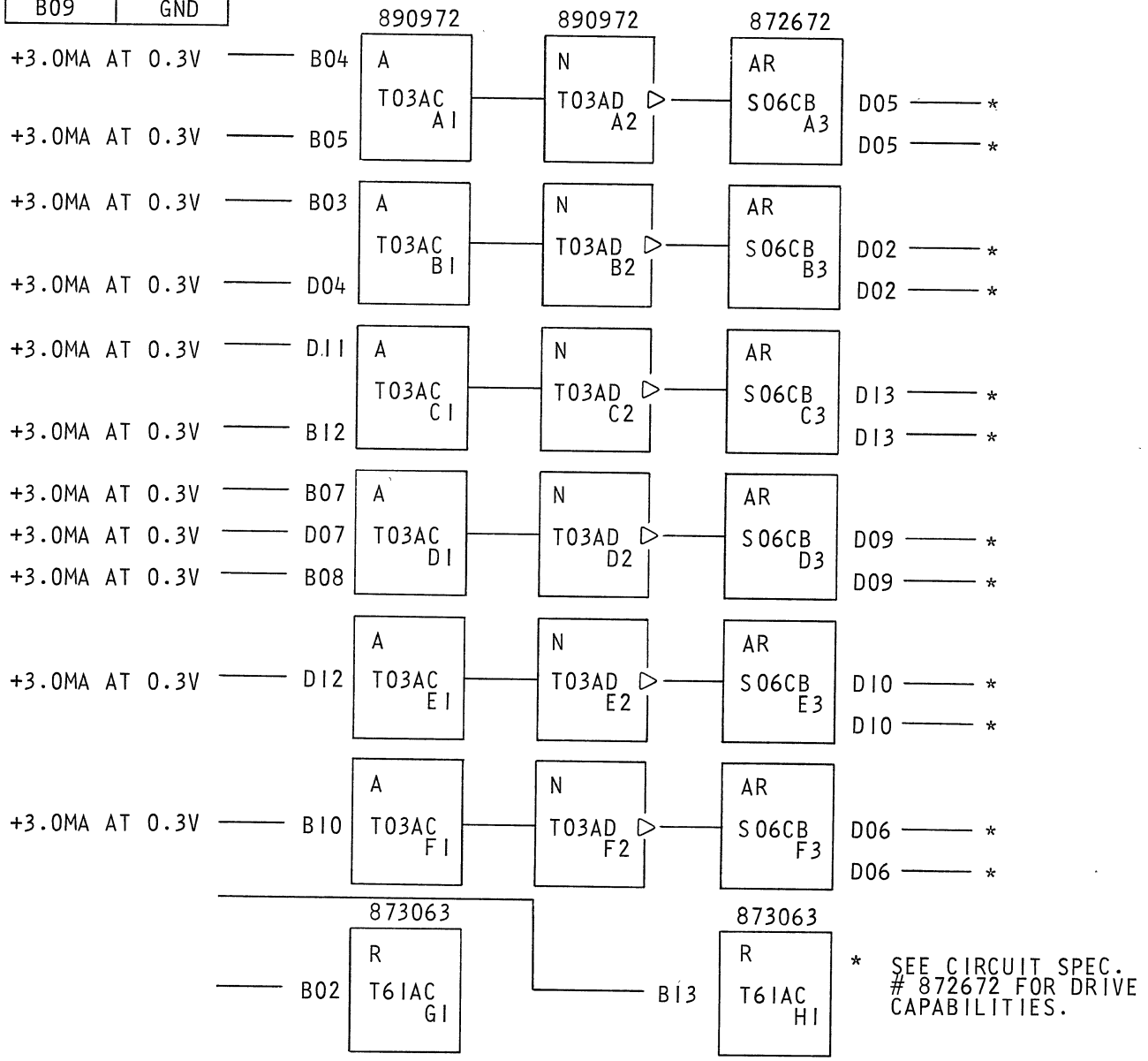
POWER REQUIRED	
PIN	VOLTS
B11	+6
D03	+3
B06	-3
D08	GND
B09	GND

SIX MPLX DRIVERS

CATEGORY CODE

T03

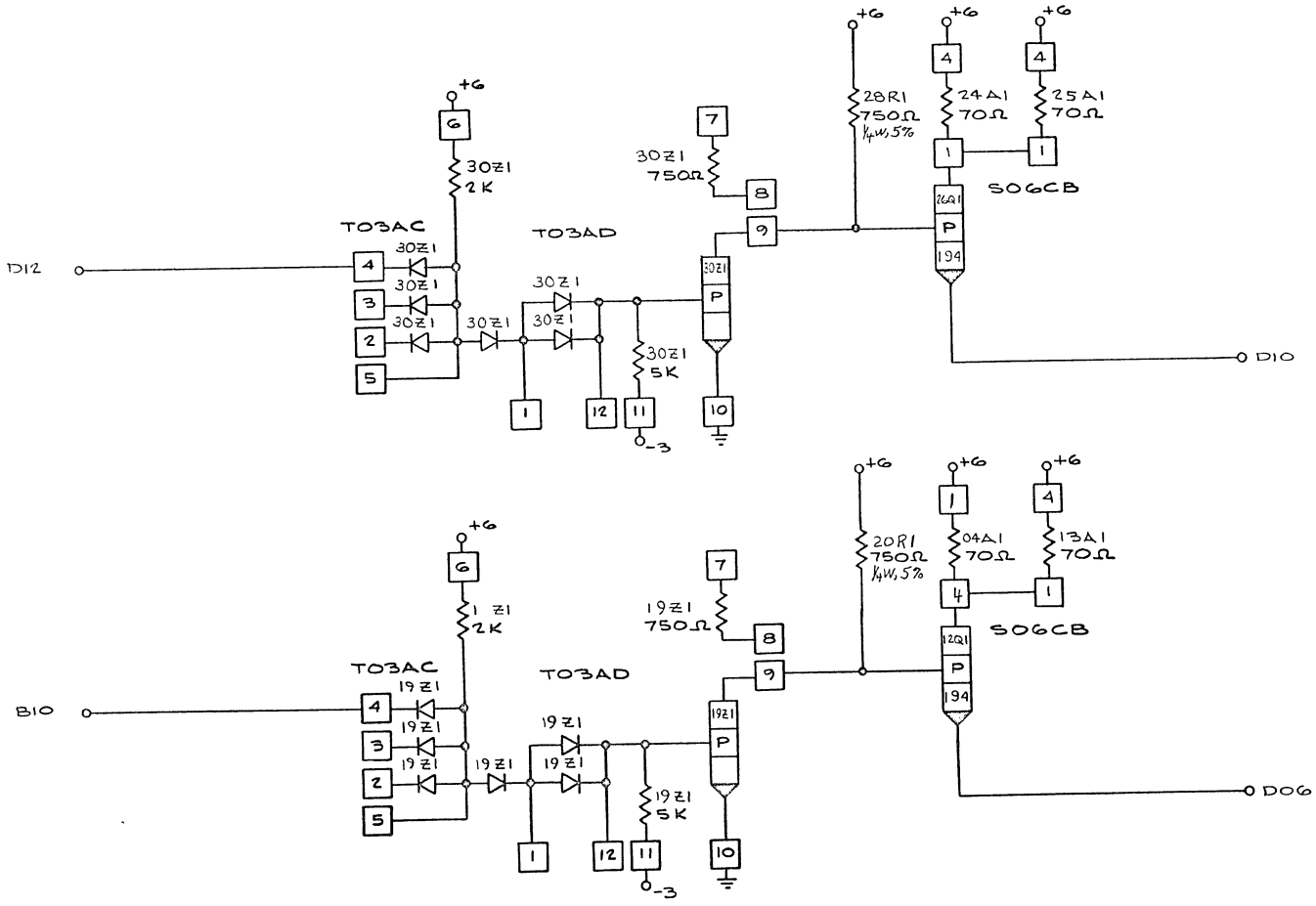
P/N	5808045
EC	164353 A
SPECIAL RESTRICTED	
CARD SIZE	1-12



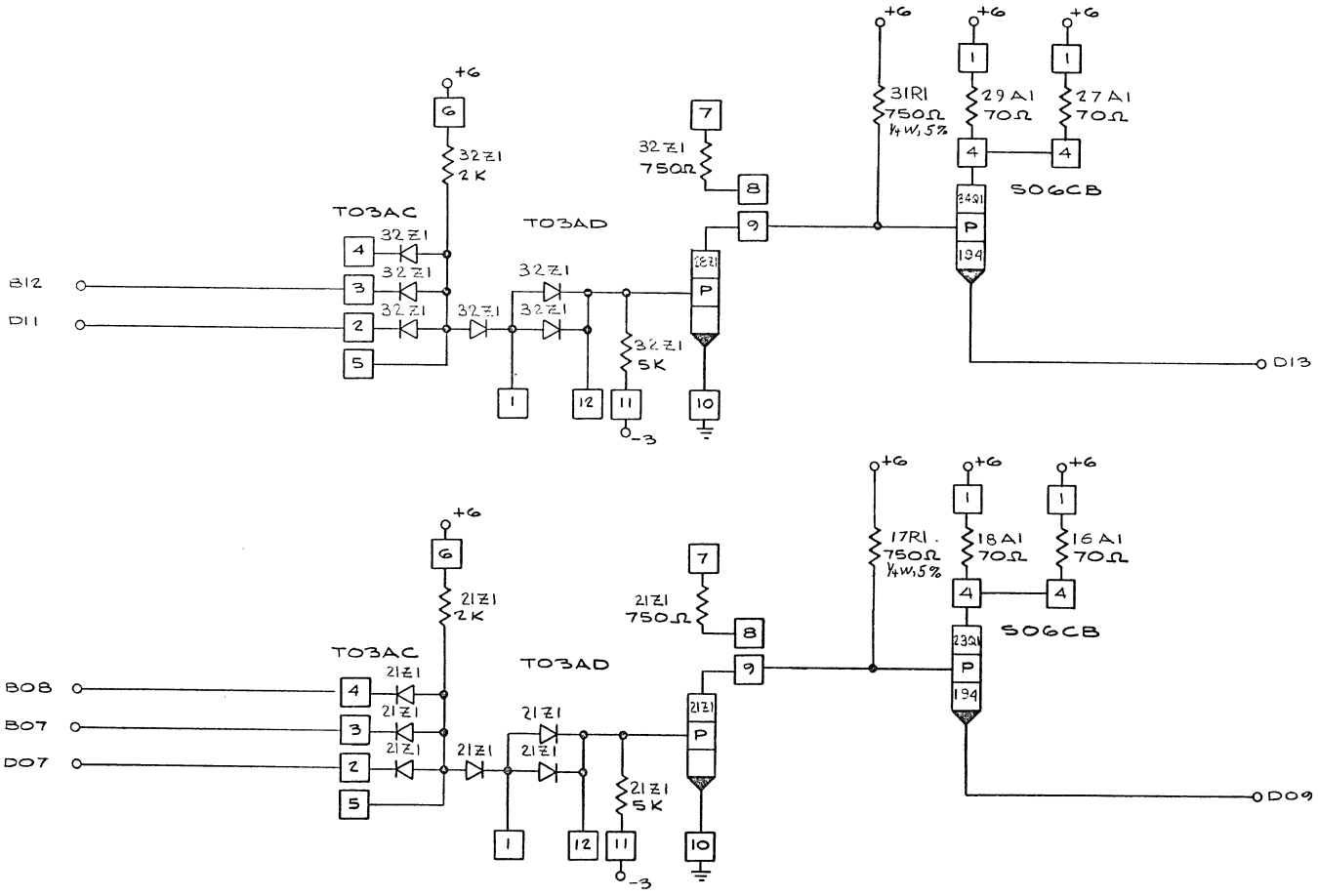
* SEE CIRCUIT SPEC. # 872672 FOR DRIVE CAPABILITIES.

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
SIX MPLX DRIVERS

P/N	5808045
EC	164353 A



P/N	5808045
EC	164353 A



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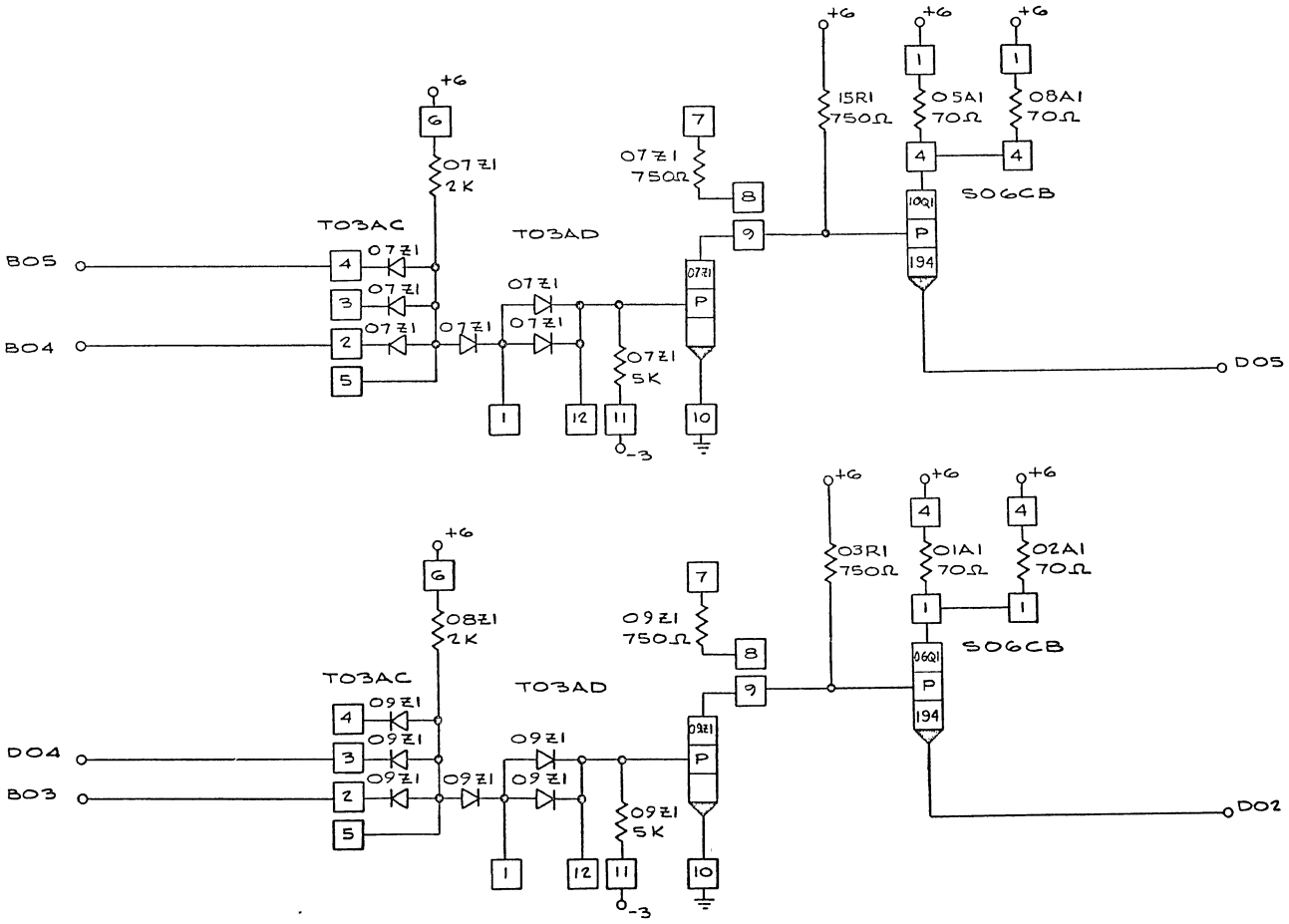
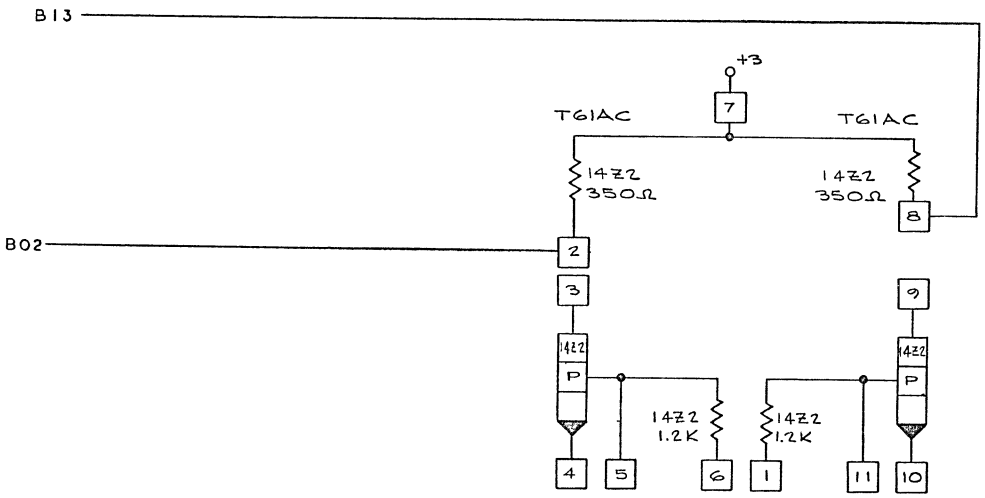
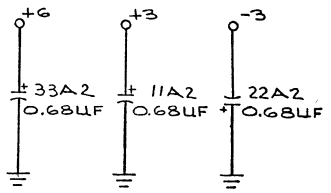
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
SIX MPLX DRIVERS

P/N	5808045
EC	164353 A



P/N	5808045
EC	164353 A





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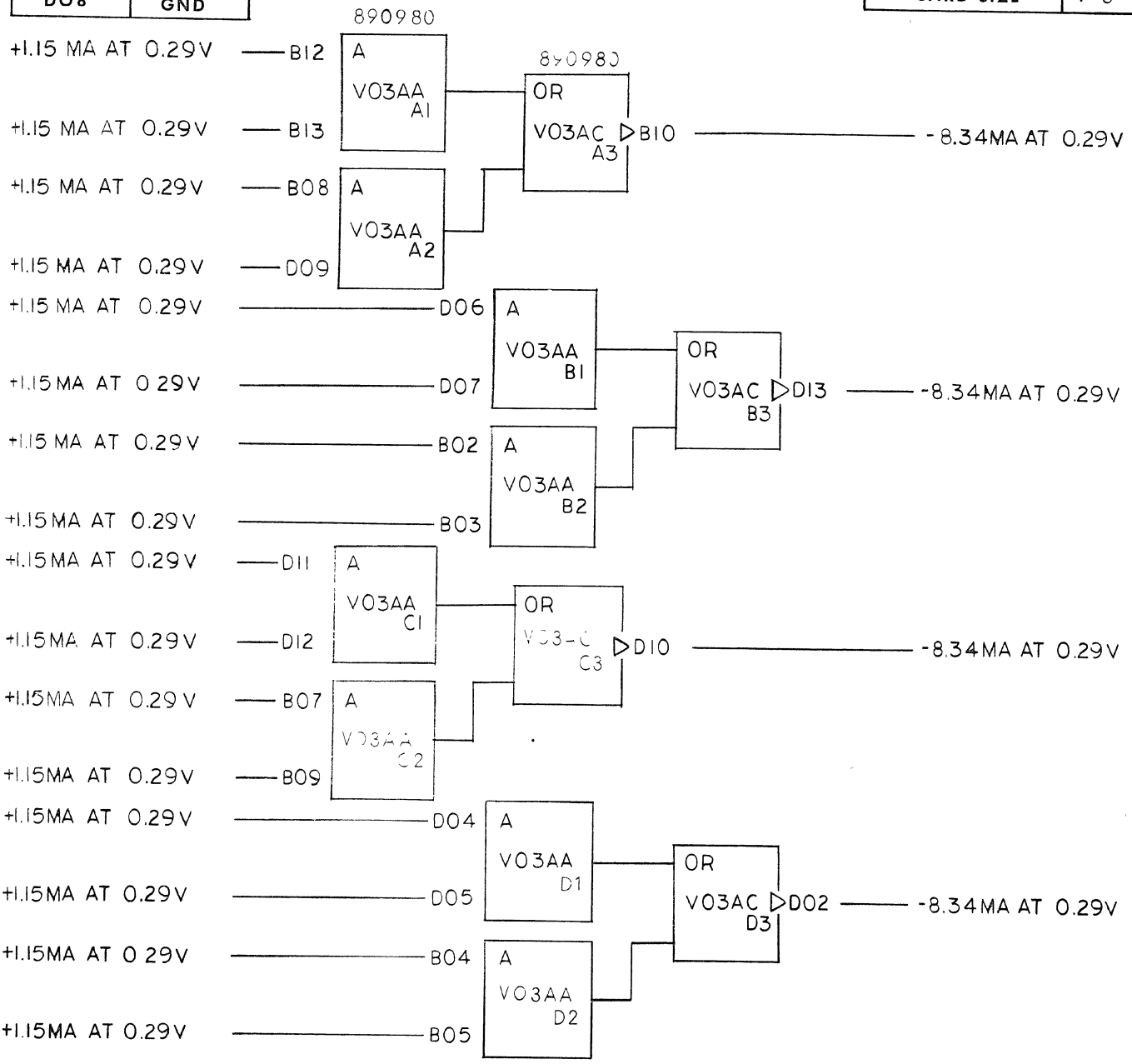
POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	12M
DO8	GND

4-2W 2W AOI

CATEGORY CODE

V03

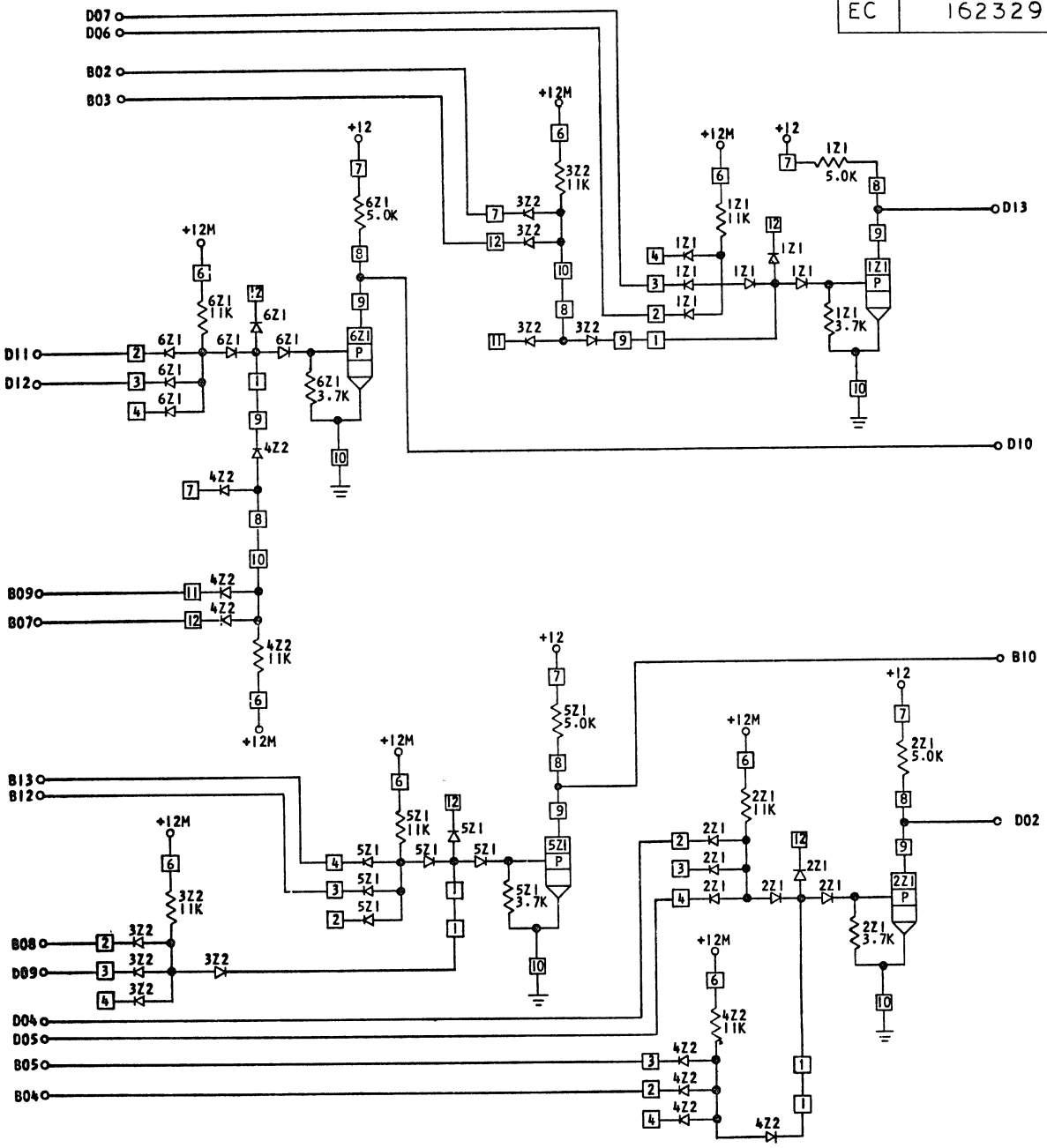
P/N	5800280
EC	162329
STANDARD	RESTRICTED
CARD SIZE	1-6



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

4-2W 2W AOI

P/N	5800280
EC	162329



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
2-5W AI & 1-7W AI

LMH	0-2860	507
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

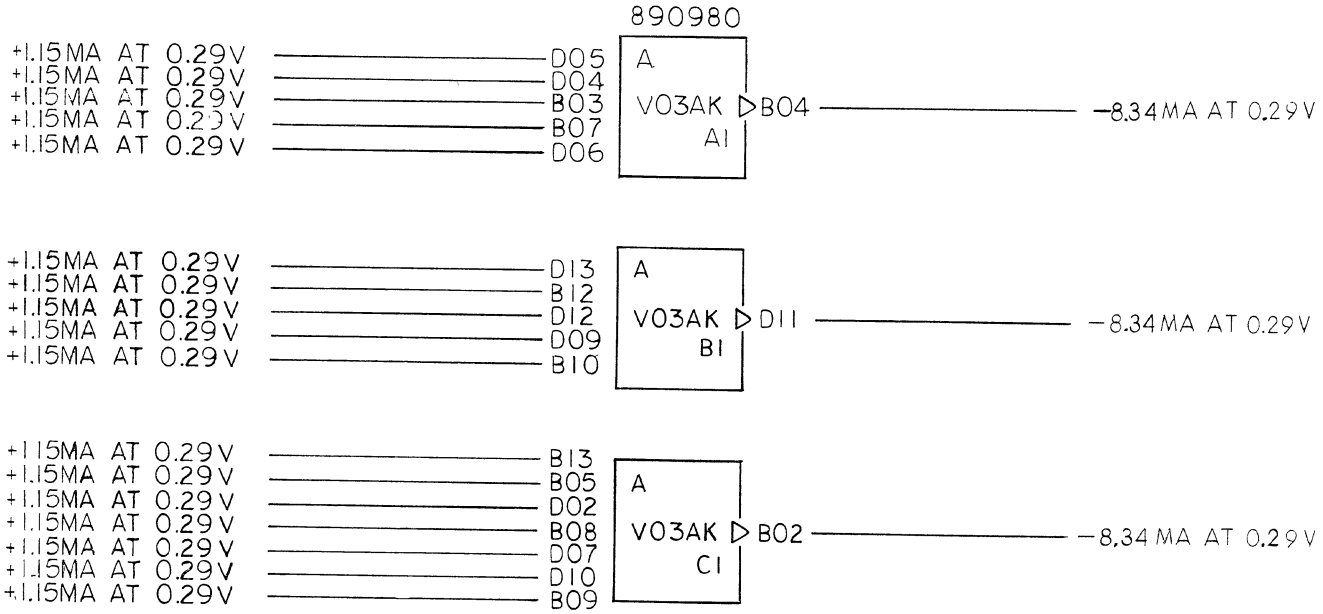
POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	12M
DO8	GND

2-5W AI & 1-7W AI

CATEGORY CODE

V03

P/N	5800286
EC	162333
STANDARD	RESTRICTED
CARD SIZE	1-6



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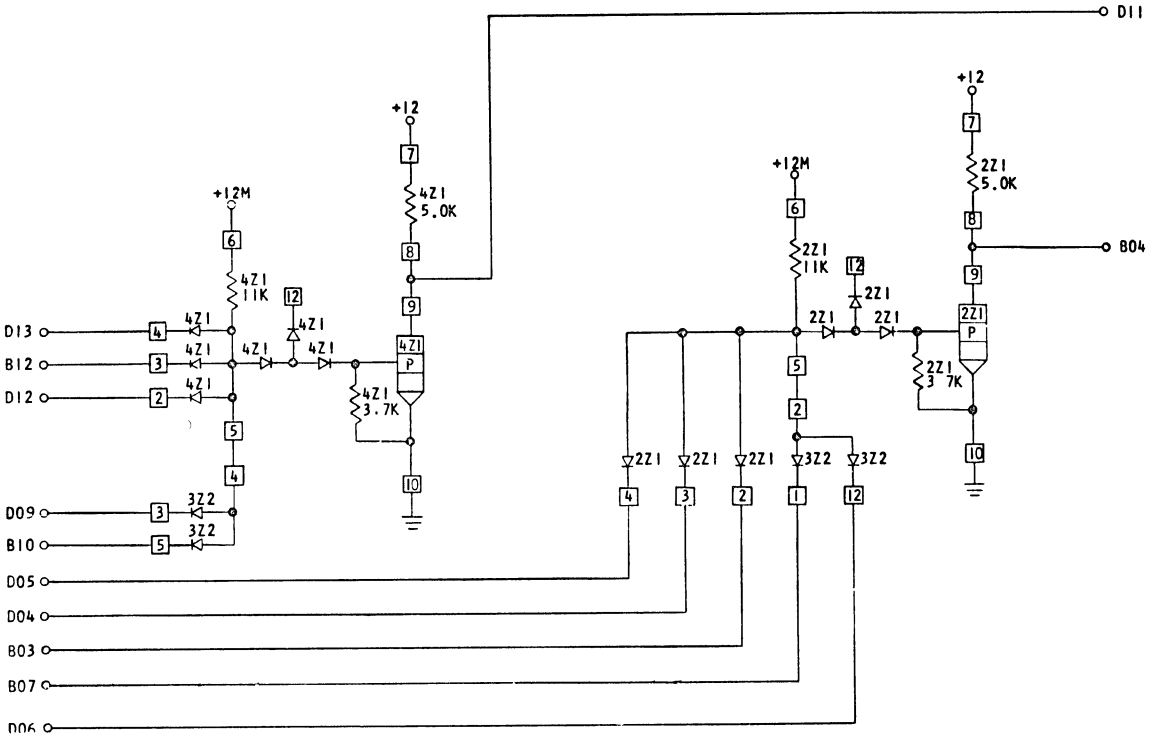
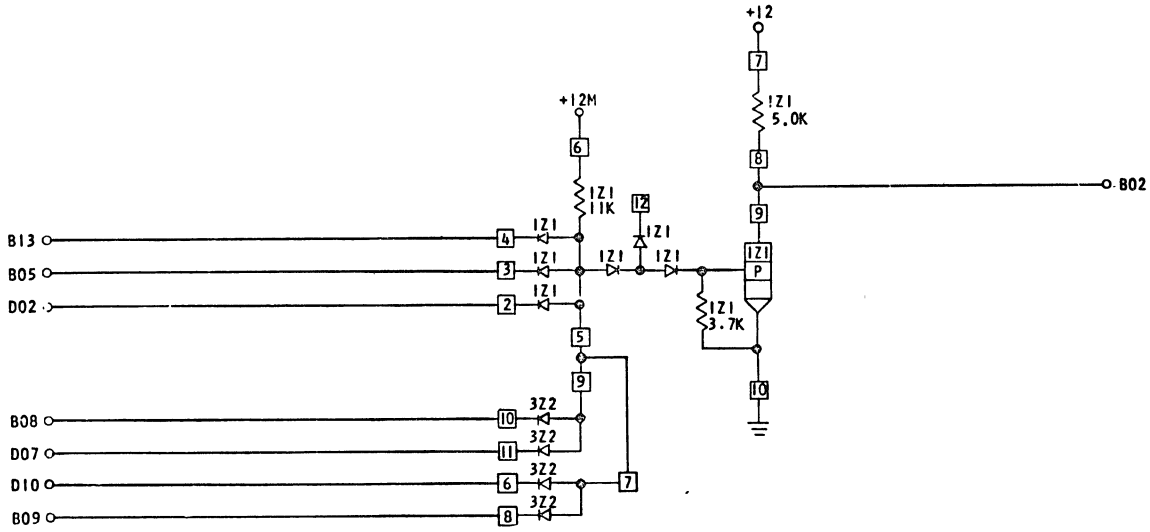
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

2-5W AI & 1-7W AI

P/N	5800286
EC	162333





SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

1-10W AI & 3-2W AI

LMH Cat.	0-2860 Subject	506 Suffix

IBM **Location Manufacturing Specification**

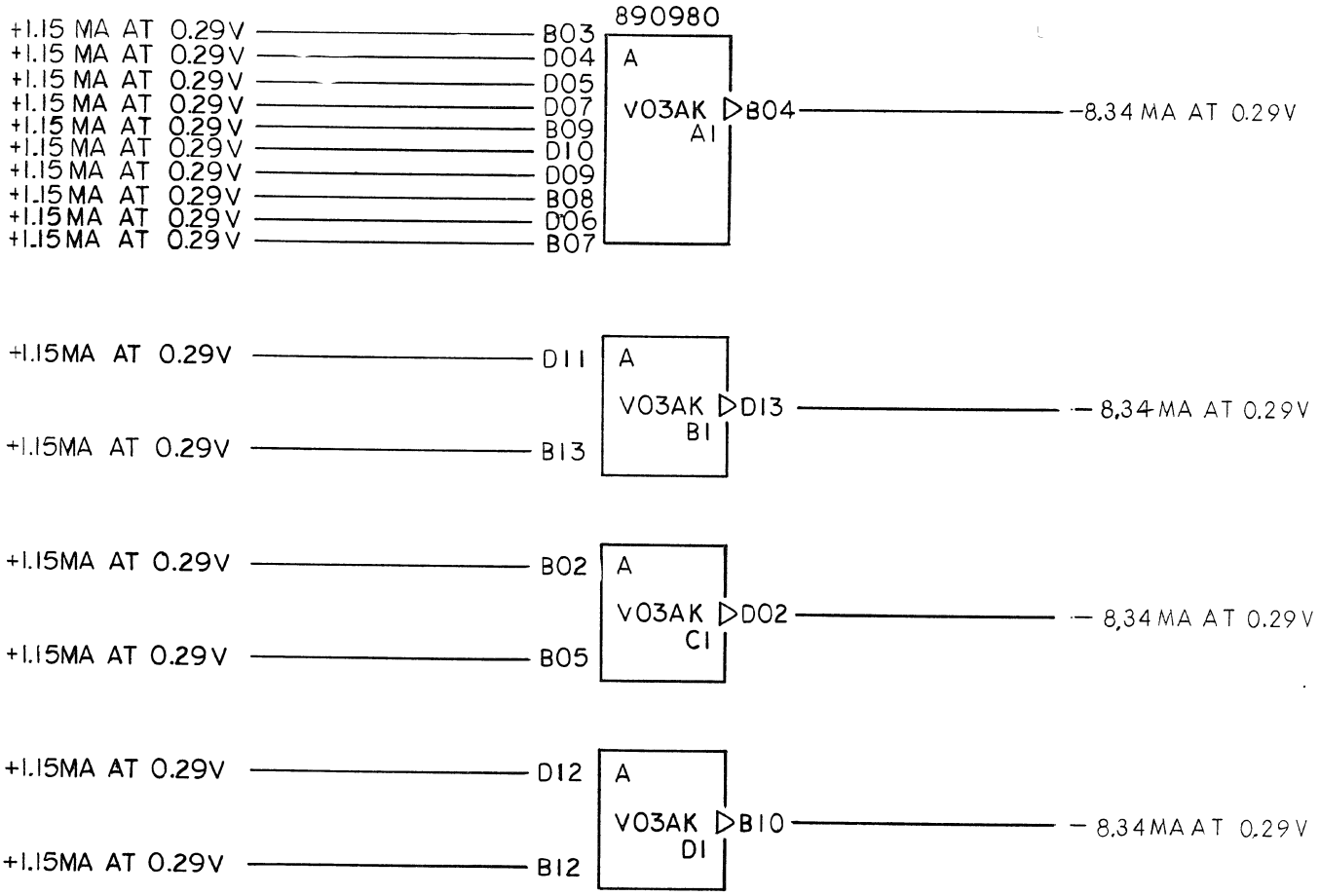
POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	12M
DO8	GND

1-10W AI & 3-2W AI

CATEGORY CODE

V03

P/N	5800287
EC	162334
STANDARD	RESTRICTED
CARD SIZE	1-6



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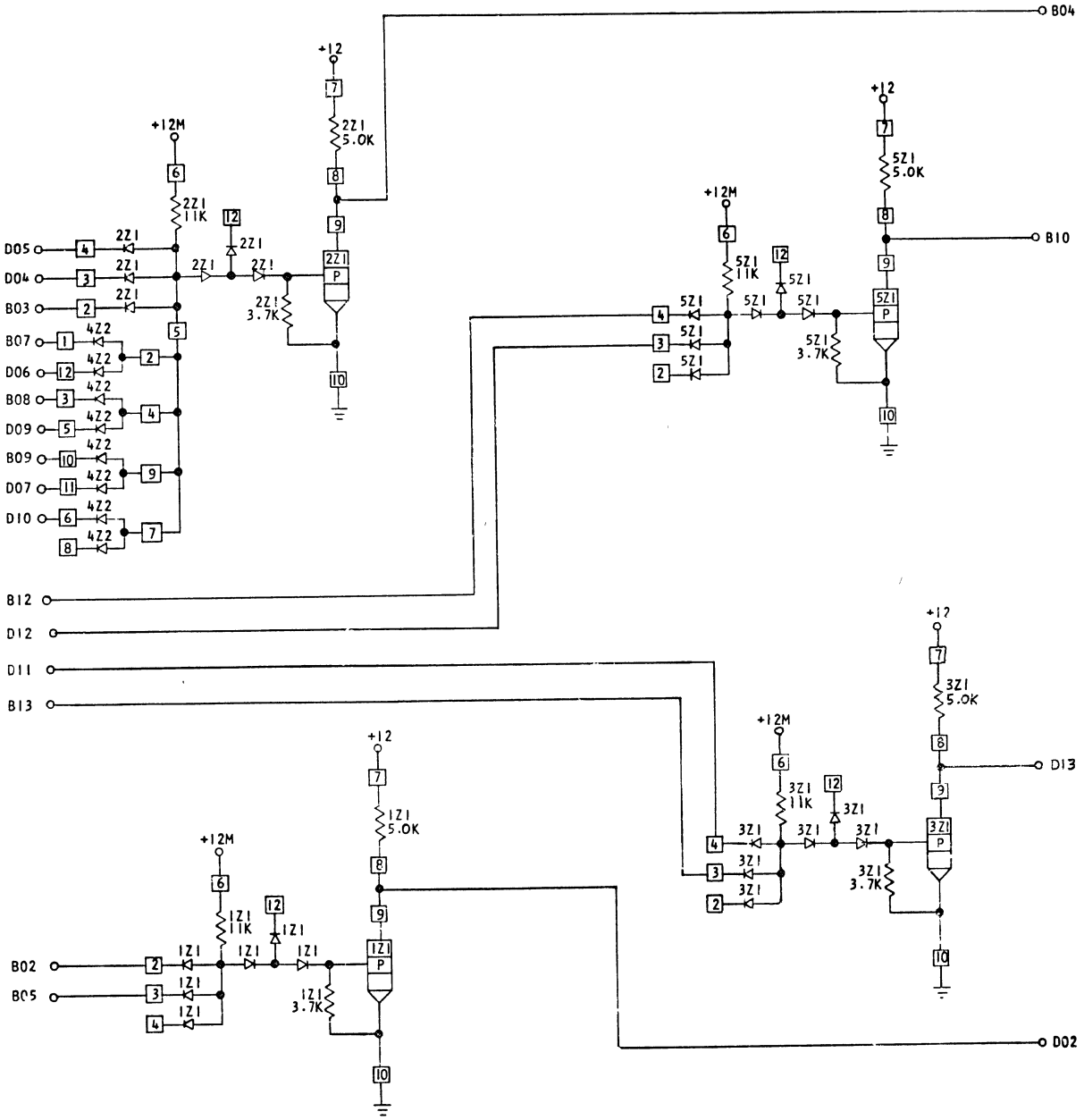
LMH Cat.	0-2860 Subject	506 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

1-10W AI & 3-2W AI

P/N	5800287
EC	162334



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

4-2W A I(NO LOAD)& 2-3W A I(NO LOAD) LC

LMH	0-2860	511
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
D03	+12
B11	12M
D08	GND

4-2W AI(NO LOAD) & 2-3W AI(NO LOAD) LC

CATEGORY CODE

V03

P/N	5800291
EC	160048
STANDARD	RESTRICTED
CARD SIZE	1- 6

890980

+1.15MA AT 0.29V — D12
+1.15MA AT 0.29V — D13
A
V03AJ A1 ▷D10 — −11MA AT 0.29V

+1.15MA AT 0.29V — D07
+1.15MA AT 0.29V — B09
A
V03AJ B1 ▷B07 — −11MA AT 0.29V

+1.15MA AT 0.29V — B08
+1.15MA AT 0.29V — D09
A
V03AJ C1 ▷D06 — −11MA AT 0.29V

+1.15MA AT 0.29V — B03
+1.15MA AT 0.29V — D05
A
V03AJ D1 ▷D04 — −11MA AT 0.29V

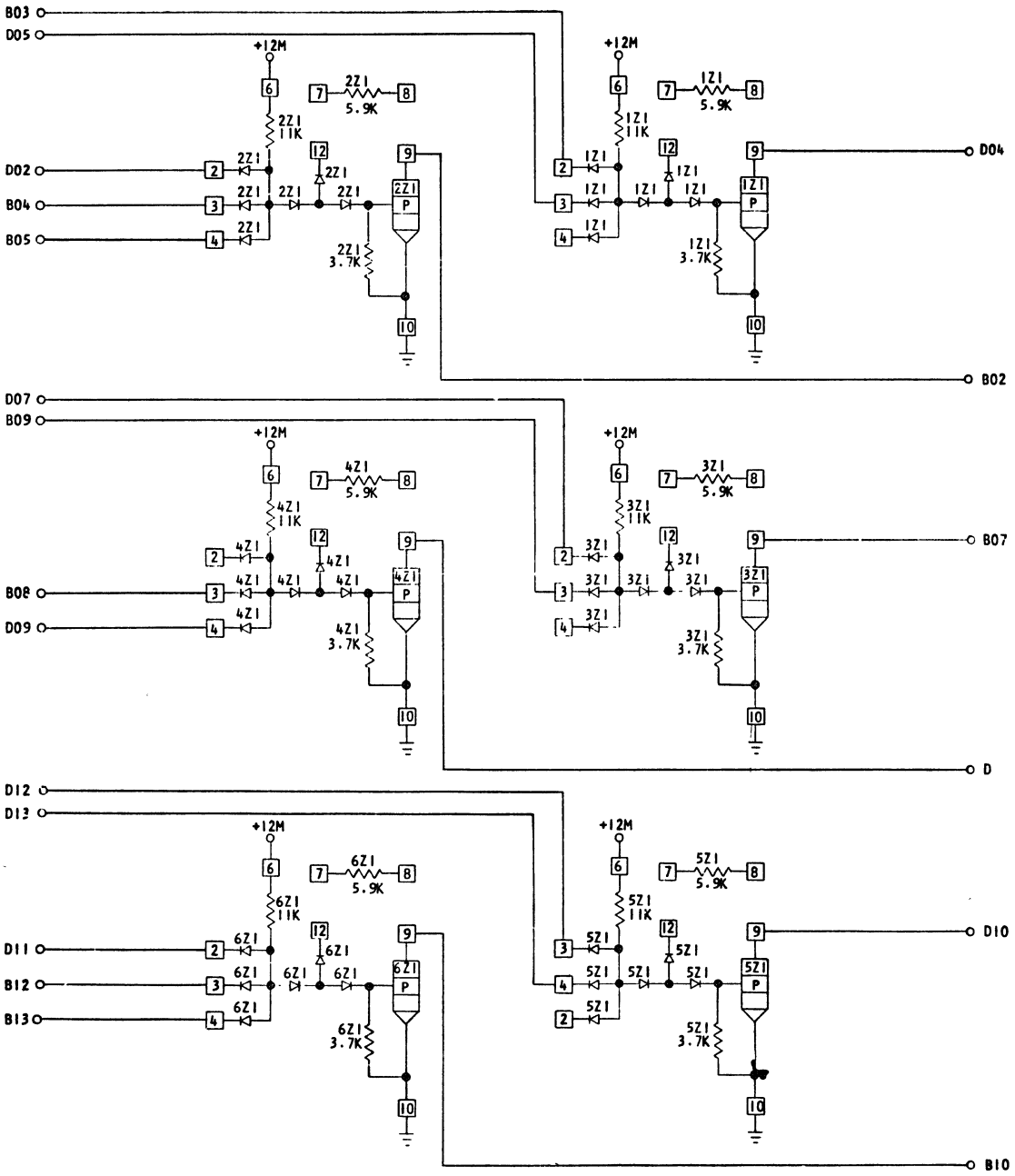
+1.15MA AT 0.29V — D02
+1.15MA AT 0.29V — B04
+1.15MA AT 0.29V — B05
A
V03AJ E1 ▷B02 — −11MA AT 0.29V

+1.15MA AT 0.29V — D11
+1.15MA AT 0.29V — B12
+1.15MA AT 0.29V — B13
A
V03AJ F1 ▷B10 — −11MA AT 0.29V

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

4-2W AI (NO LOAD) & 2-3W AI (NO LOAD) LC

P/N	5800291
EC	160048



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

5-3W API LC

LMH	0-2860	509
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

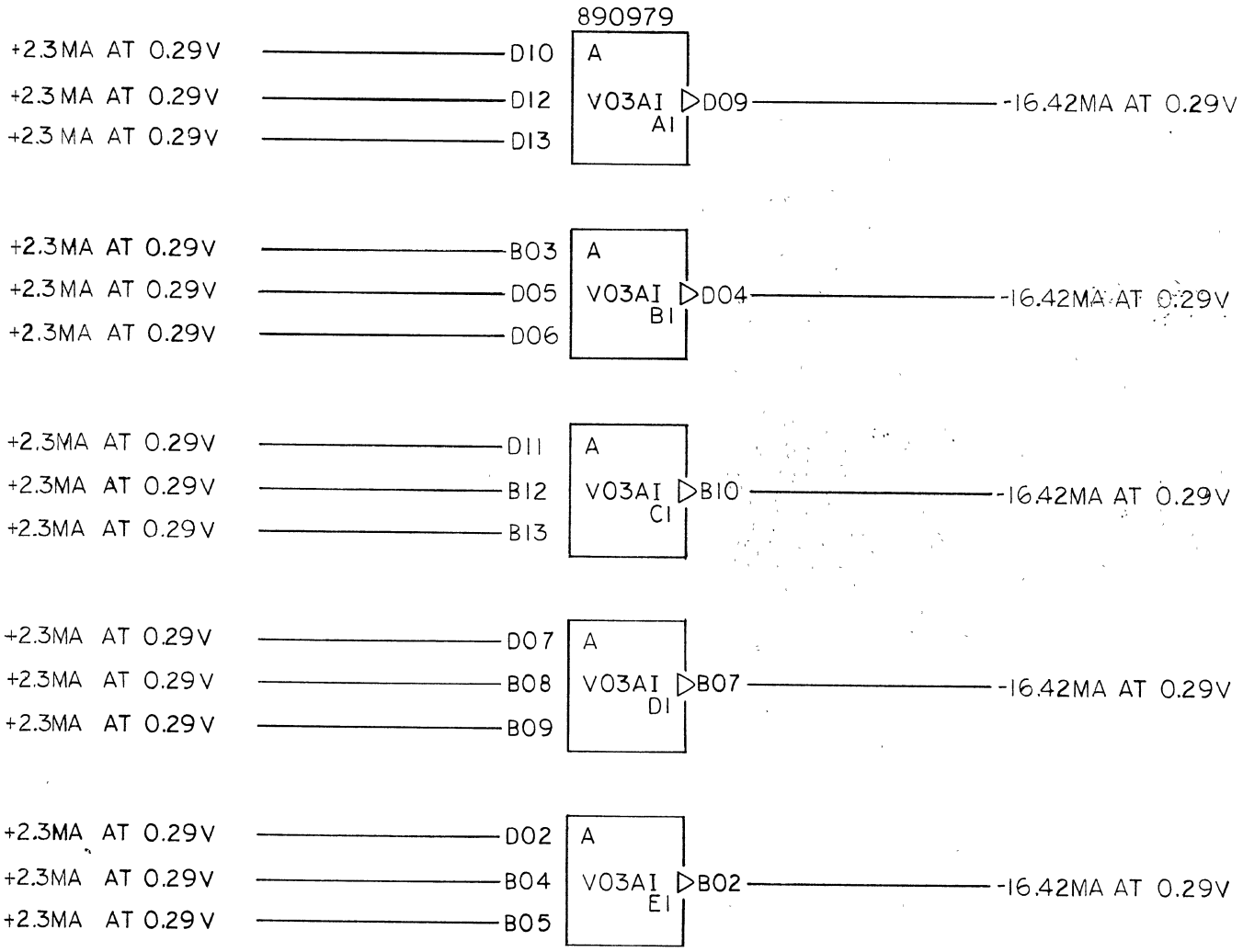
POWER REQUIRED	
PIN	VOLTS
DO3	12 M
B11	12M
DO8	GND

5-3W API LC

CATEGORY CODE

V03

P/N	5800294
EC	163700
STANDARD	RESTRICTED
CARD SIZE	1-6



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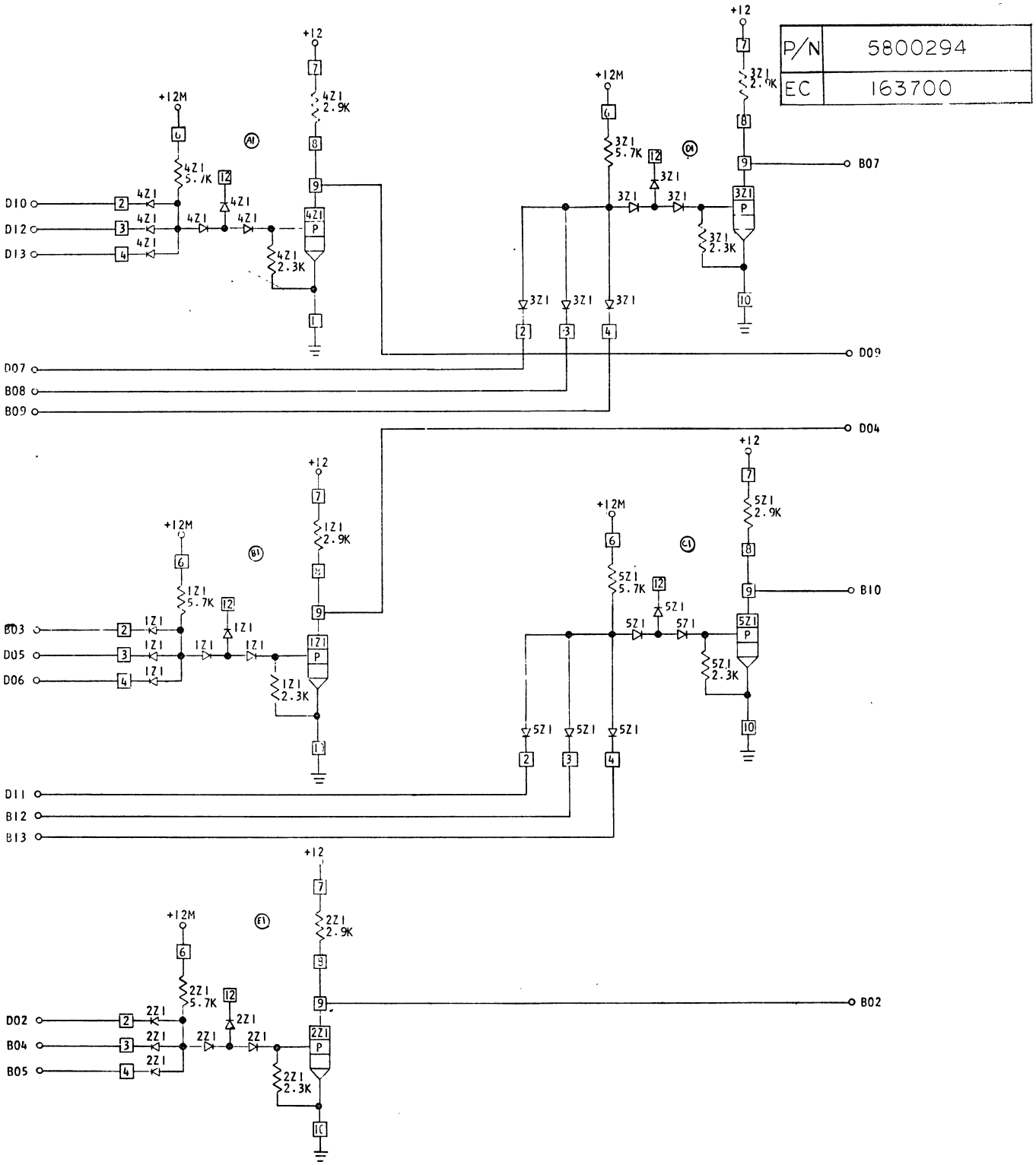
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

5-3W API LC

P/N	5800294
EC	163700



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

4-2W AI & 2-3W AI

LMH Cat.	0-2860 Subject	505 Suffix

IBM Location Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	12M
DO8	GND

4-2W AI & 2-3W AI

CATEGORY CODE

V03

P/N	5800297
EC	164429
STANDARD	RESTRICTED
CARD SIZE	1-6

890980

+1.15MA AT 0.29V — B08
+1.15MA AT 0.29V — D09
A
V03AK ▷ D06 — 8.34MA AT 0.29V
A1

+1.15MA AT 0.29V — B03
+1.15MA AT 0.29V — D05
A
V03AK ▷ D04 — 8.34MA AT 0.29V
B1

+1.15MA AT 0.29V — D07
+1.15MA AT 0.29V — B09
A
V03AK ▷ B07 — 8.34MA AT 0.29V
C1

+1.15MA AT 0.29V — D12
+1.15MA AT 0.29V — D13
A
V03AK ▷ D10 — 8.34MA AT 0.29V
D1

+1.15MA AT 0.29V — D02
+1.15MA AT 0.29V — B04
+1.15MA AT 0.29V — B05
A
V03AK ▷ B02 — 8.34MA AT 0.29V
E1

+1.15MA AT 0.29V — D11
+1.15MA AT 0.29V — B12
+1.15MA AT 0.29V — B13
A
V03AK ▷ B10 — 8.34MA AT 0.29V
F1

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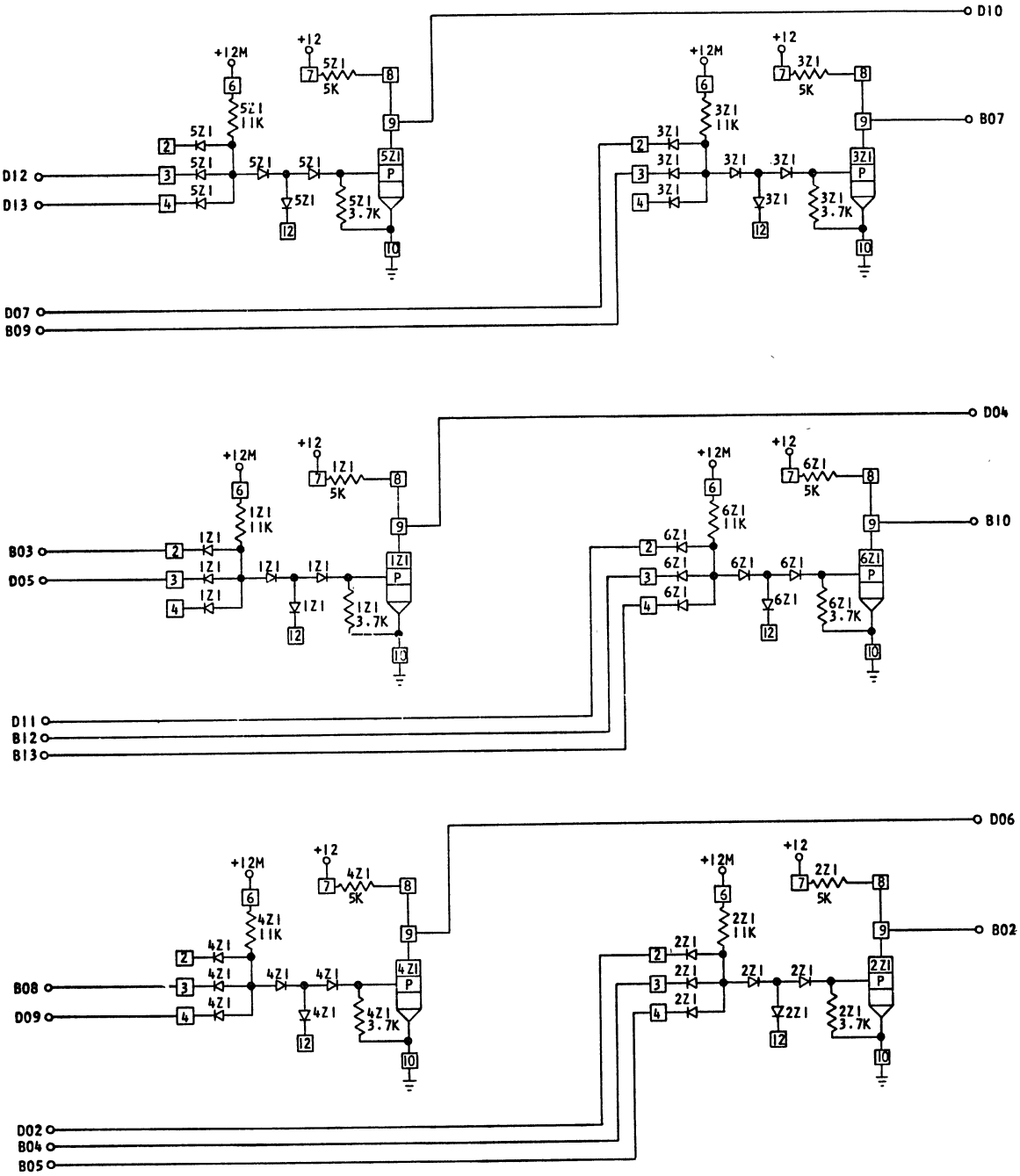
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

4-2W AI & 2-3W AI

P/N	5800297
EC	164429



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

TEN ISOLATING INVERTERS WITH LOADS

LMH	0-2860	512
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	12M
DO8	GND

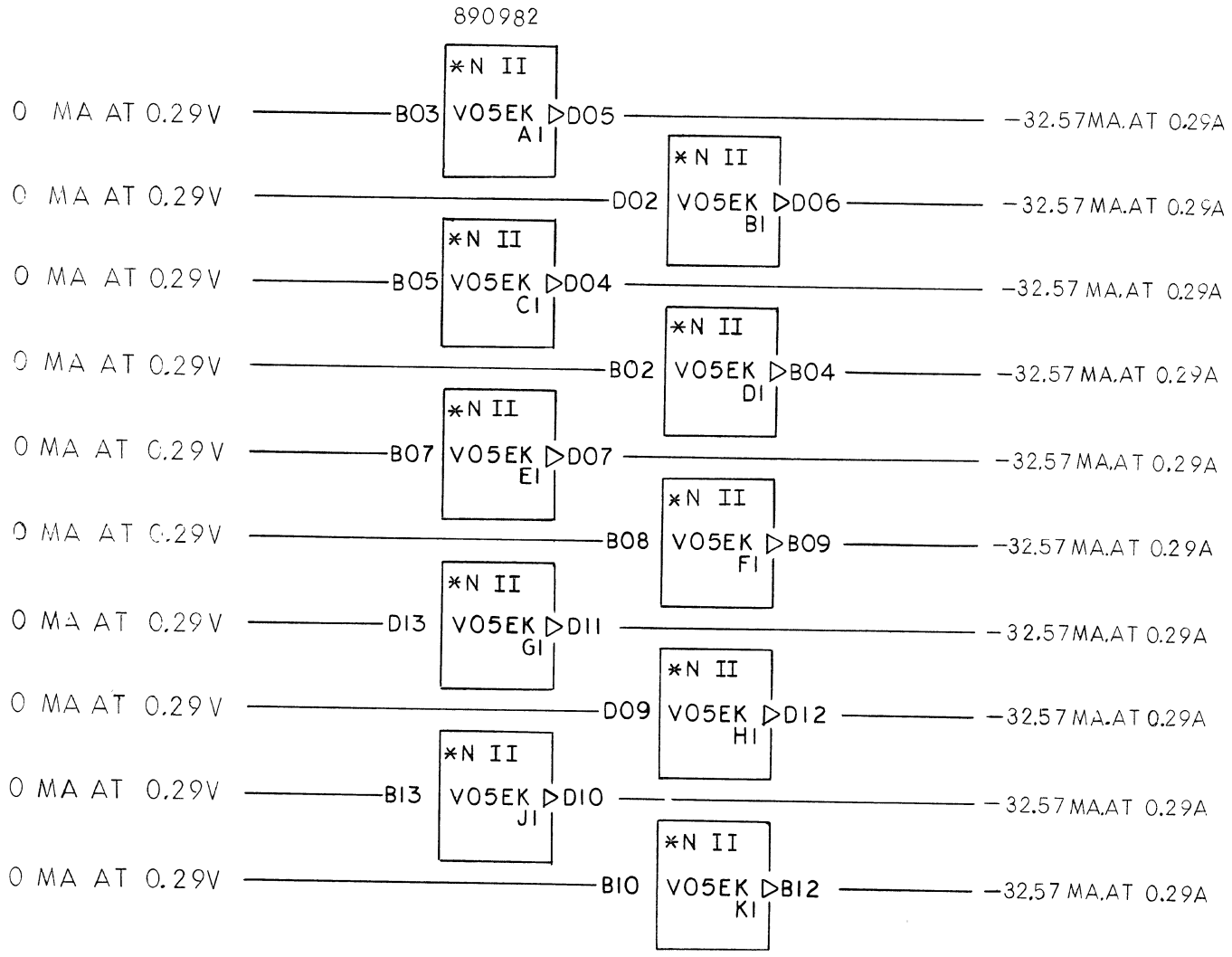
TEN ISOLATING INVERTERS WITH LOADS

CATEGORY CODE

V05

P/N	5800383
EC	160213
STANDARD	RESTRICTED
CARD SIZE	1-6

890982



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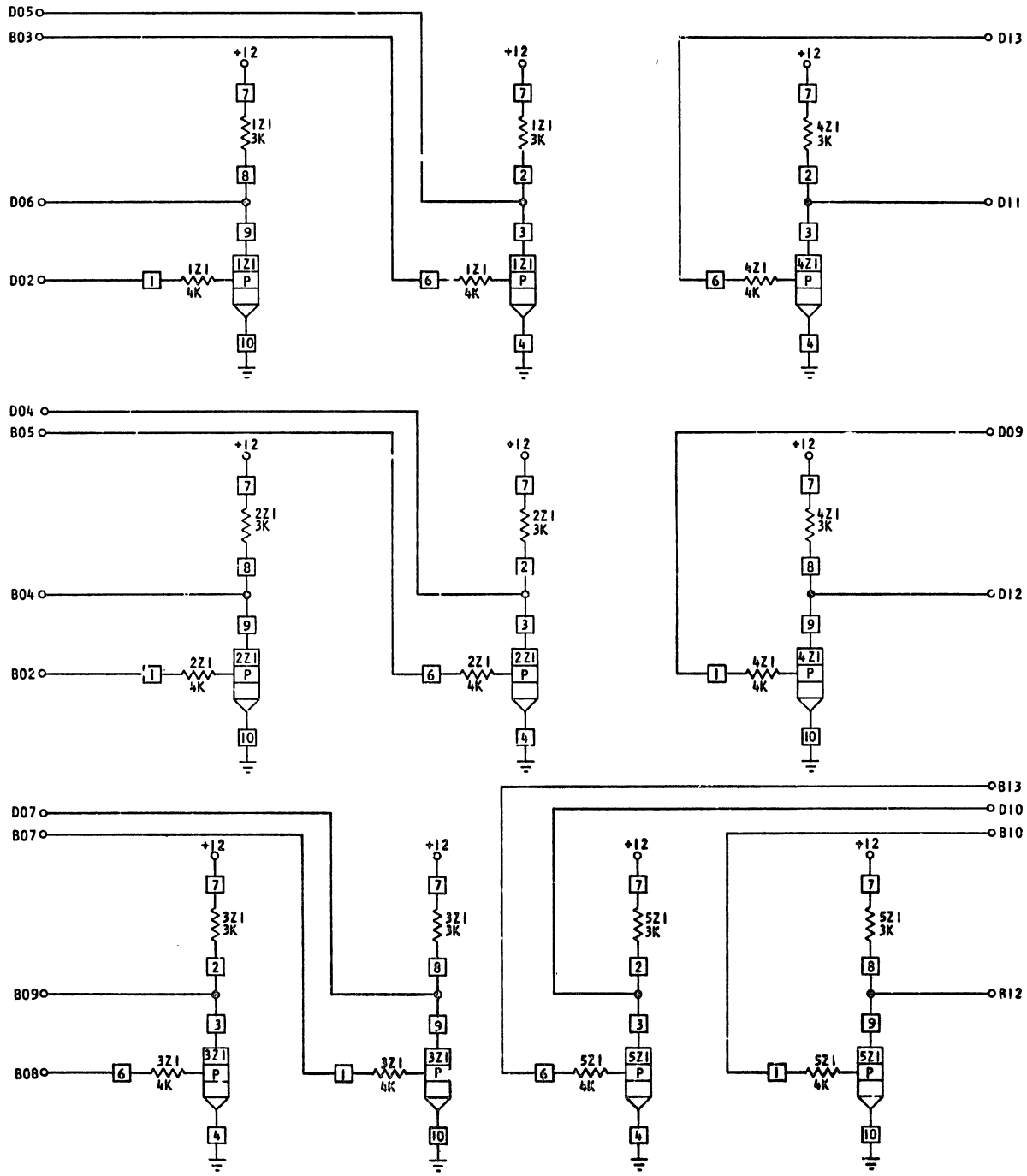
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

TEN ISOLATING INVERTERS WITH LOAD

P/N	5800383
EC	160213



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

8 INDICATOR DRIVERS FOR 10V 40 MA LAMP

LMH	0-2860	514
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

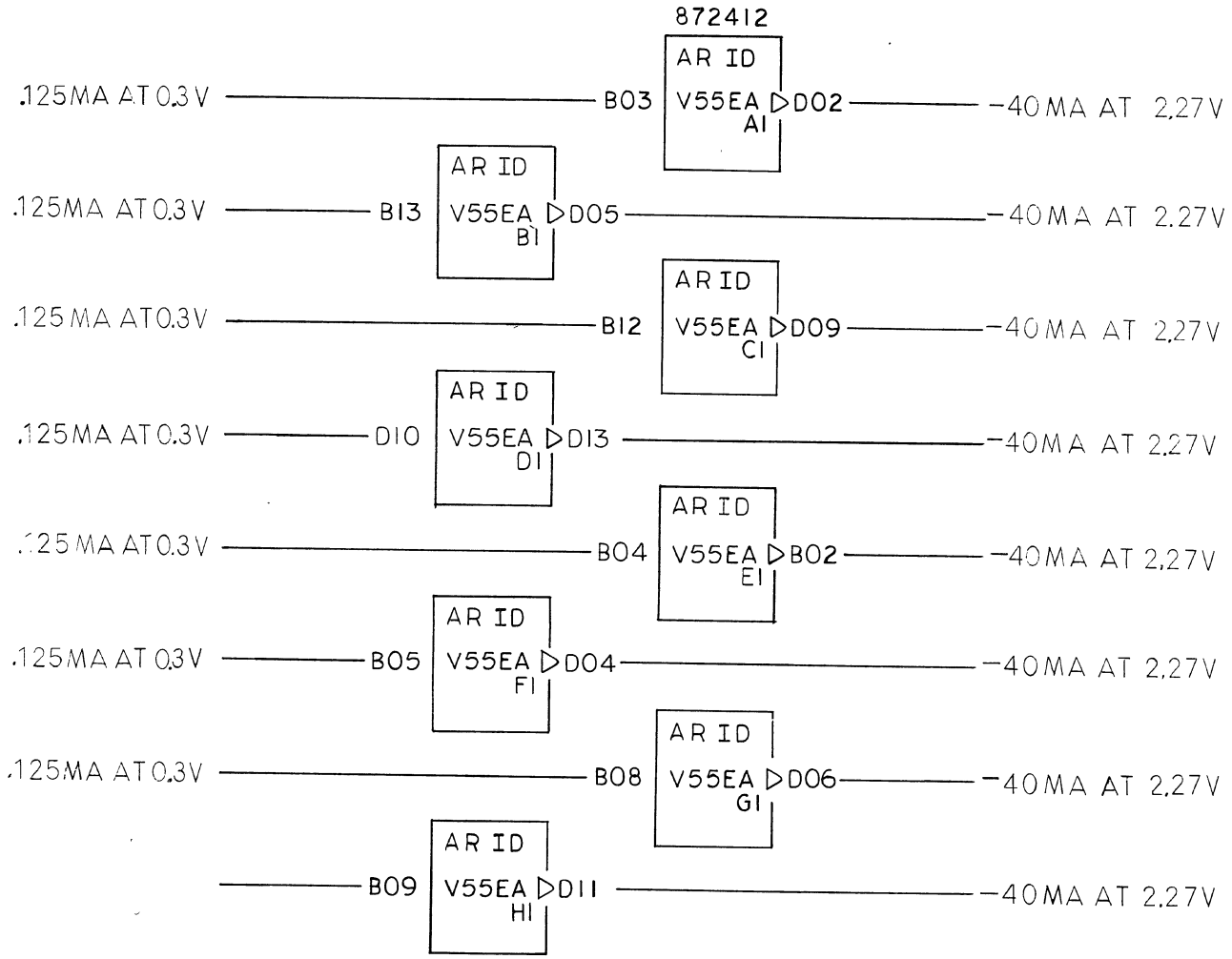
POWER REQUIRED	
PIN	VOLTS
DO3	+12
DO8	GND

8 INDICATOR DRIVERS FOR 10V 40 MA LAMP

CATEGORY CODE

V55

P/N	5800387
EC	160133
SPECIAL	RESTRICTED
CARD SIZE	1-6



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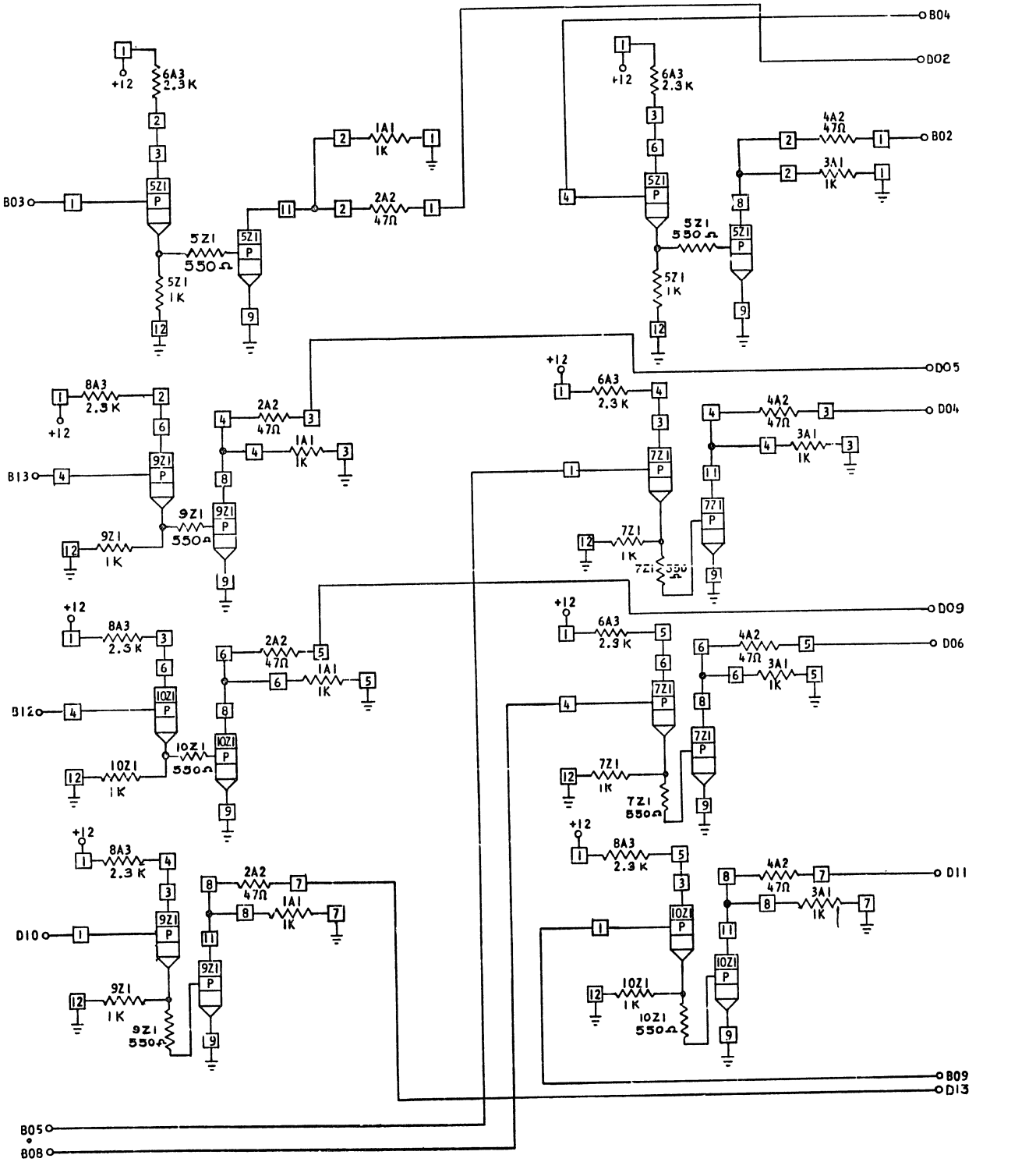
LMH Cat.	0-2860 Subject	514 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

8 INDICATOR DRIVERS FOR 10V 40MA LAMPS

P/N	5800387
EC	160133



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

10 TRANSMISSION LINE TERMINATORS

LMH	0-2860	510
Cat.	Subject	Suffix

IBM **Location Manufacturing Specification**

POWER REQUIRED	
PIN	VOLTS
B06	+12
D08	GND

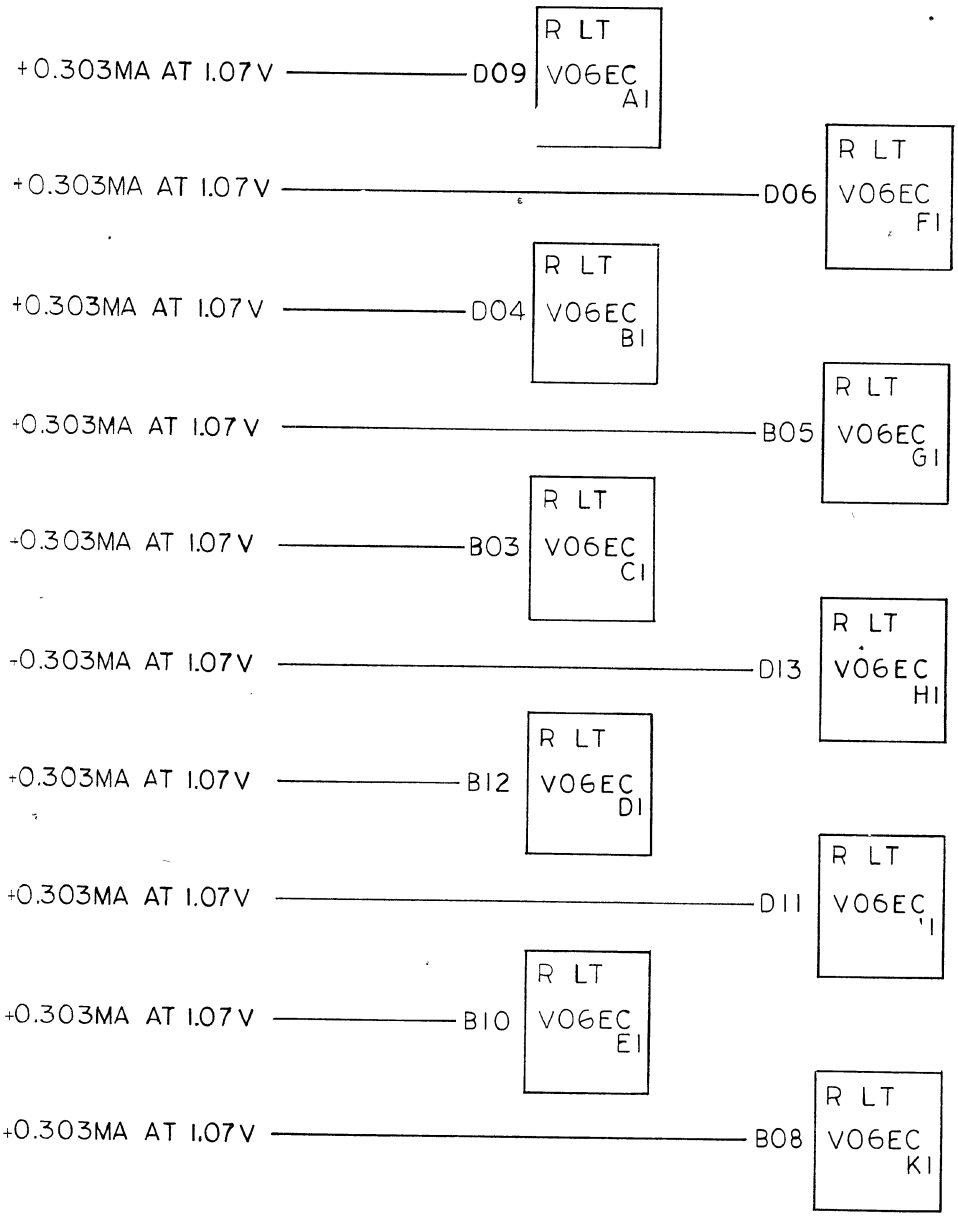
10 TRANSMISSION LINE TERMINATORS

CATEGORY CODE

V06

P/N	5800538
EC	161573
STANDARD	**RESTRICTED**
CARD SIZE	1-6

873404



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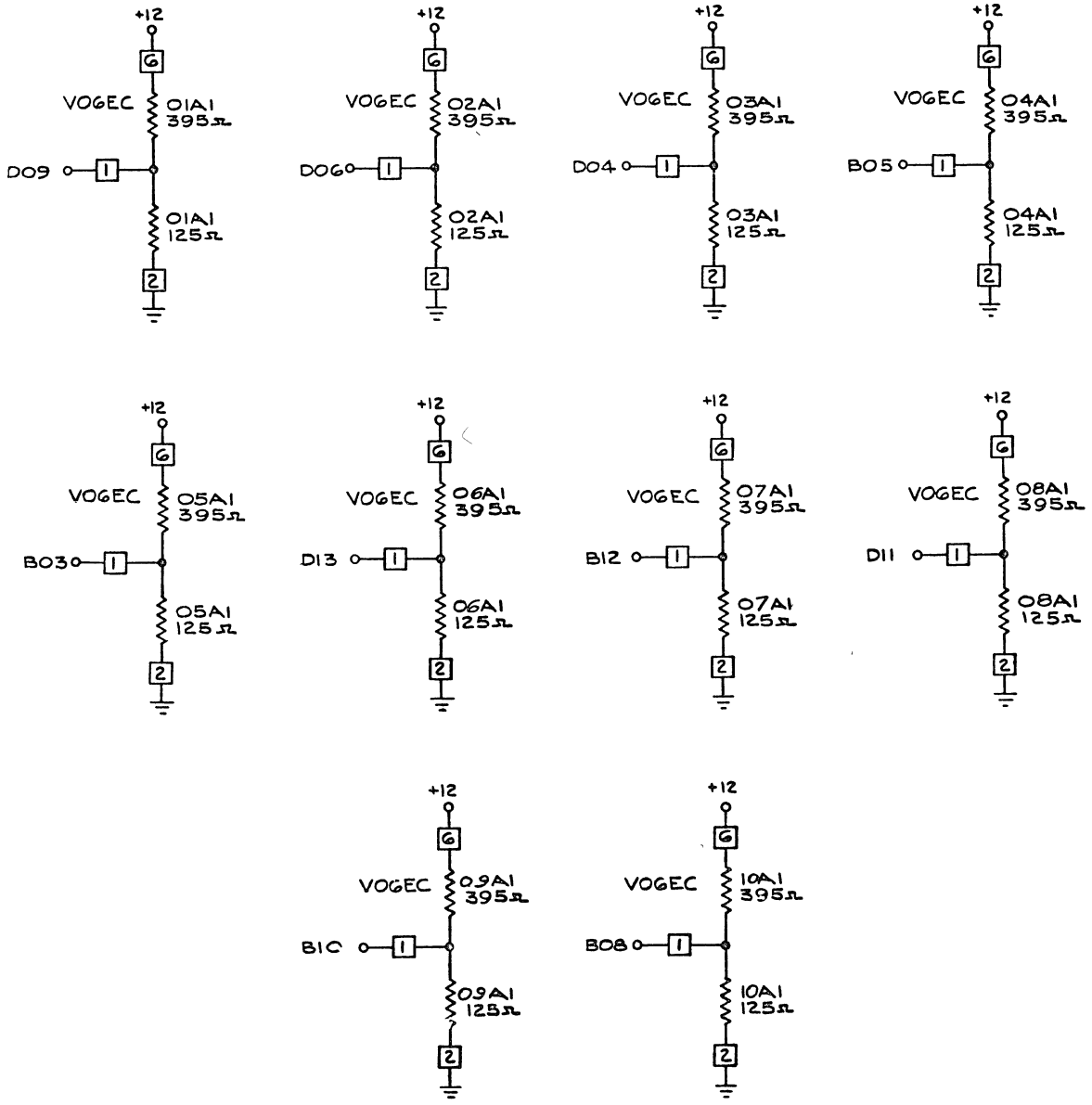
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

10 TRANSMISSION LINE TERMINATORS

P/N	5800538
E C	161573



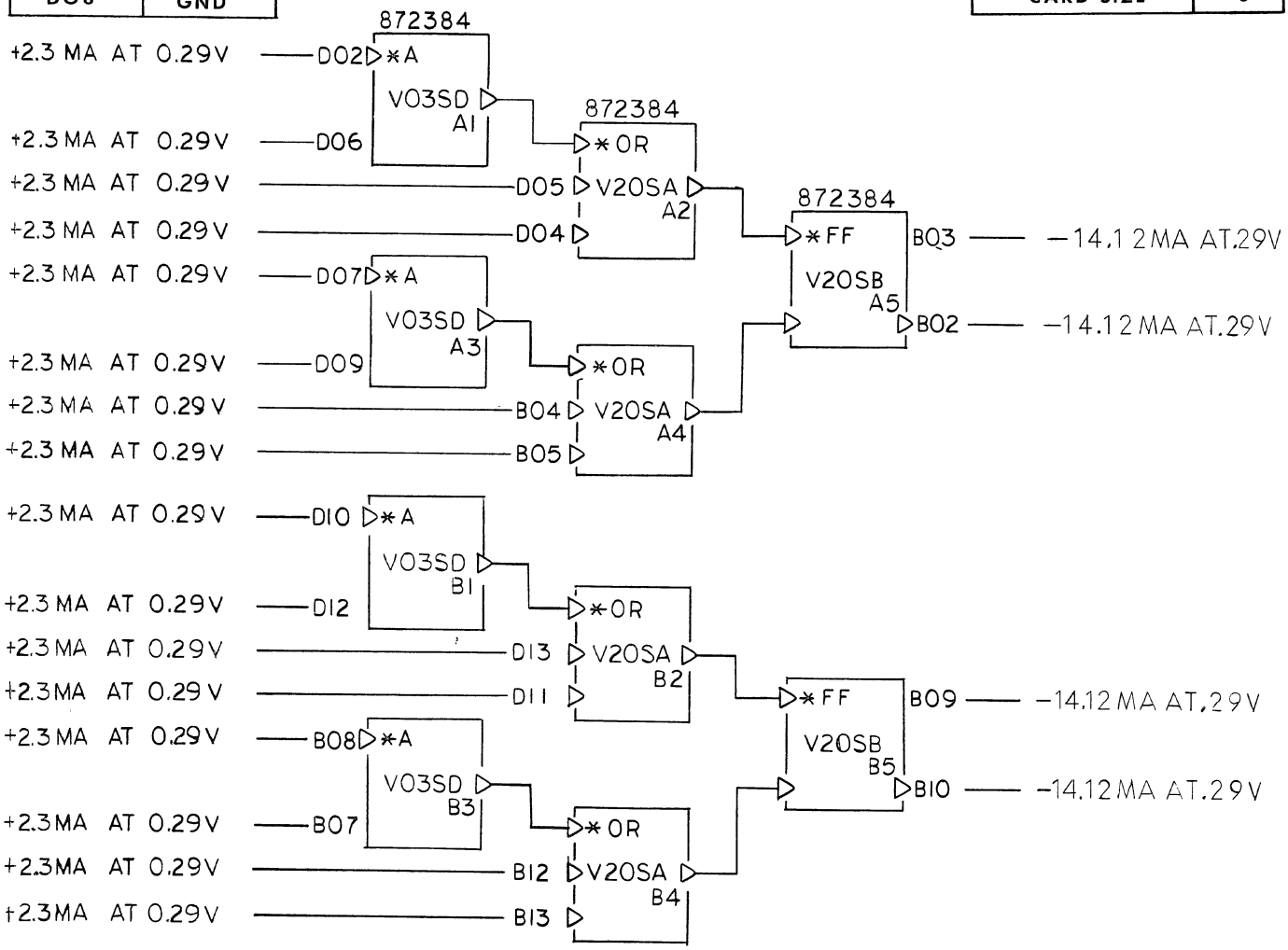
POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	+12M
DO8	GND

TRIGGER

CATEGORY CODE

V03	V20

P/N	5800733
EC	167840
SPECIAL	RESTRICTED
CARD SIZE	1-6

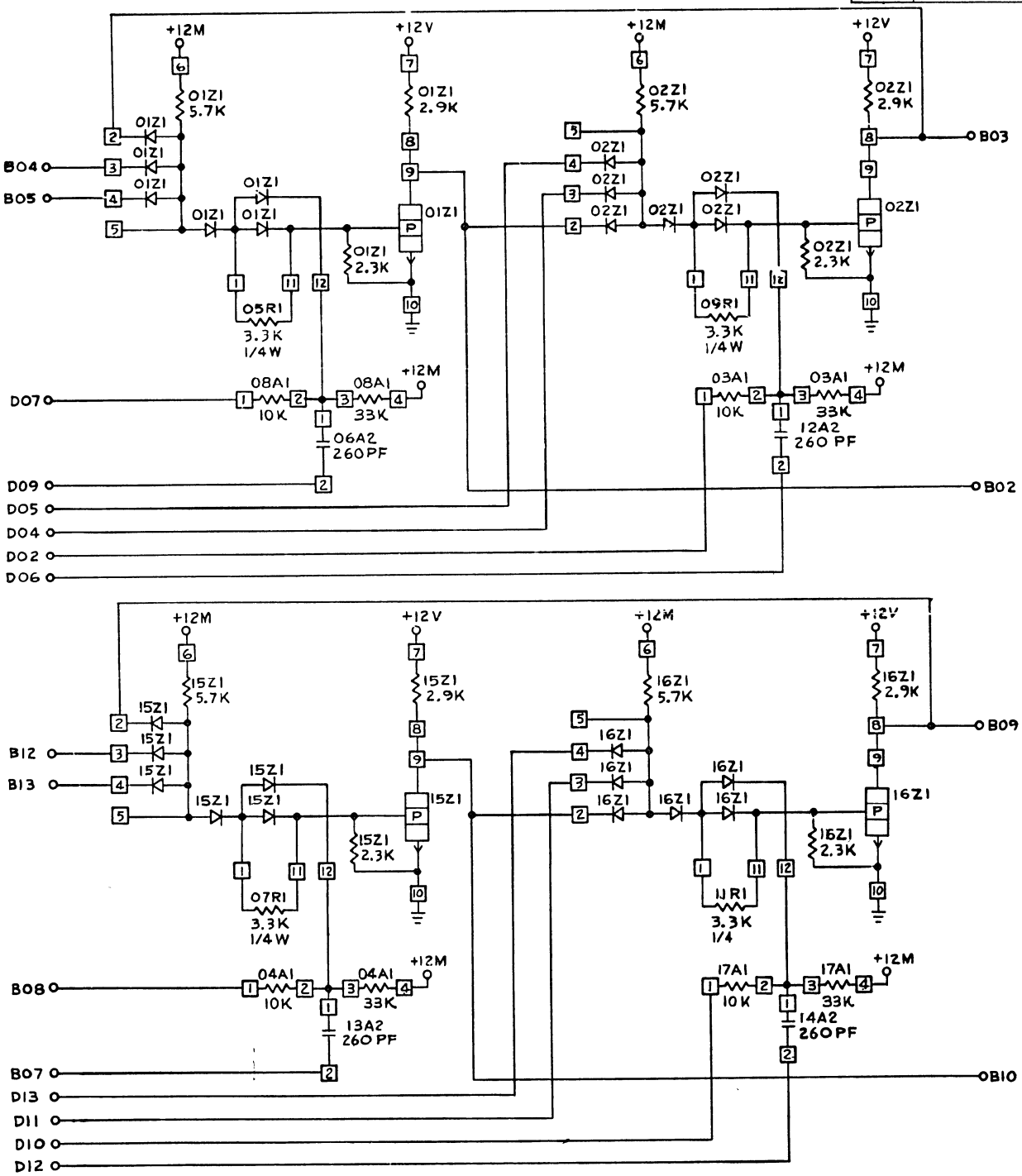


LMH Cat	0-2860 Subject	516 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

TRIGGER

P/N	5800733
E/C	167840



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

LATCH CARD

LMH Cat.	0-2860 Subject	508 Suffix

IBM Location Manufacturing Specification

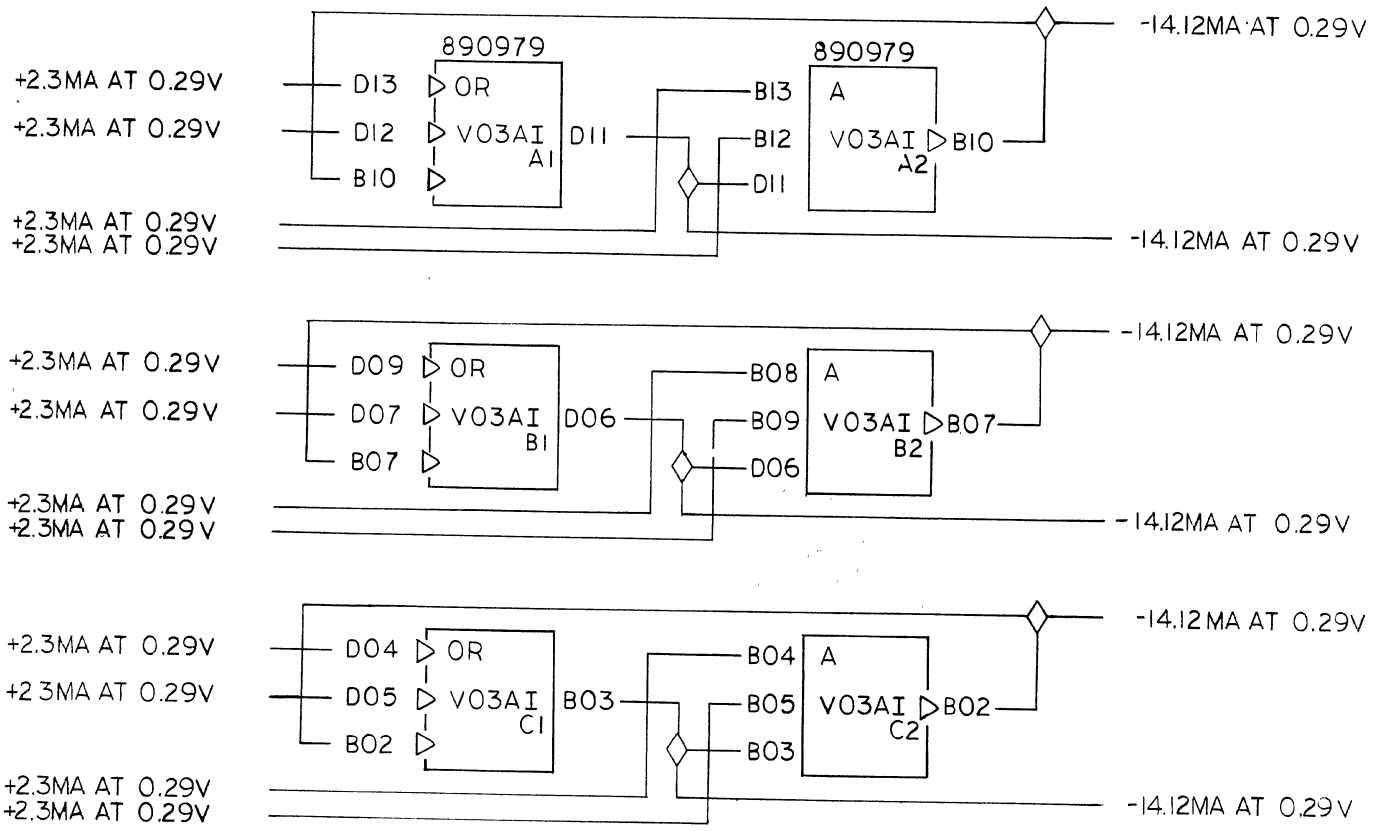
POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	12M
DO8	GND

LATCH CARD

CATEGORY CODE

V03

P/N	5800734
EC	160530
STANDARD RESTRICTED	
CARD SIZE	1-6



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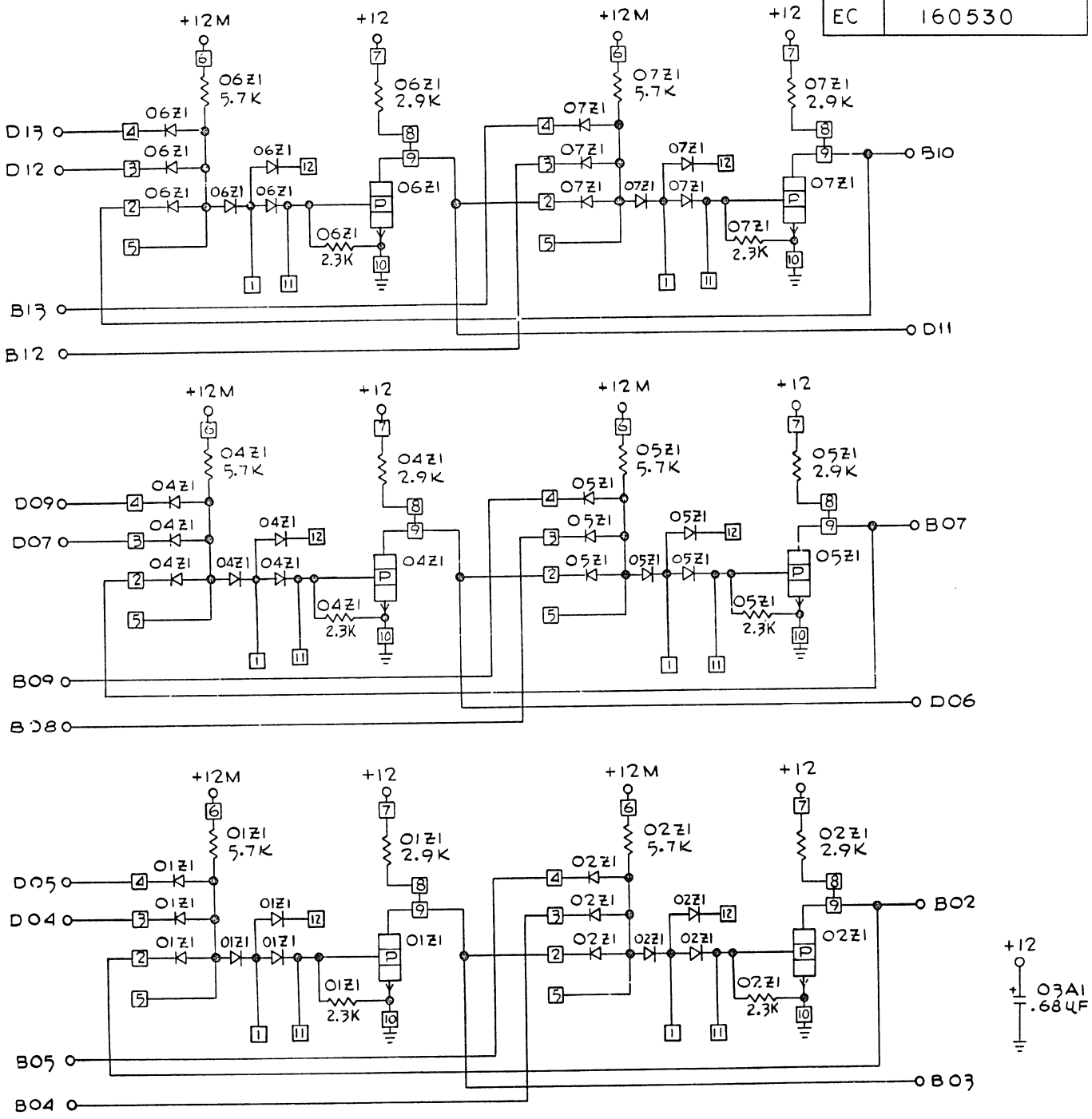
LMH Cat.	0-2860 Subject	508 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

LATCH CARD

P/N	5800734
EC	160530



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

RELAY DRIVER

LMH	0-2860	513
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

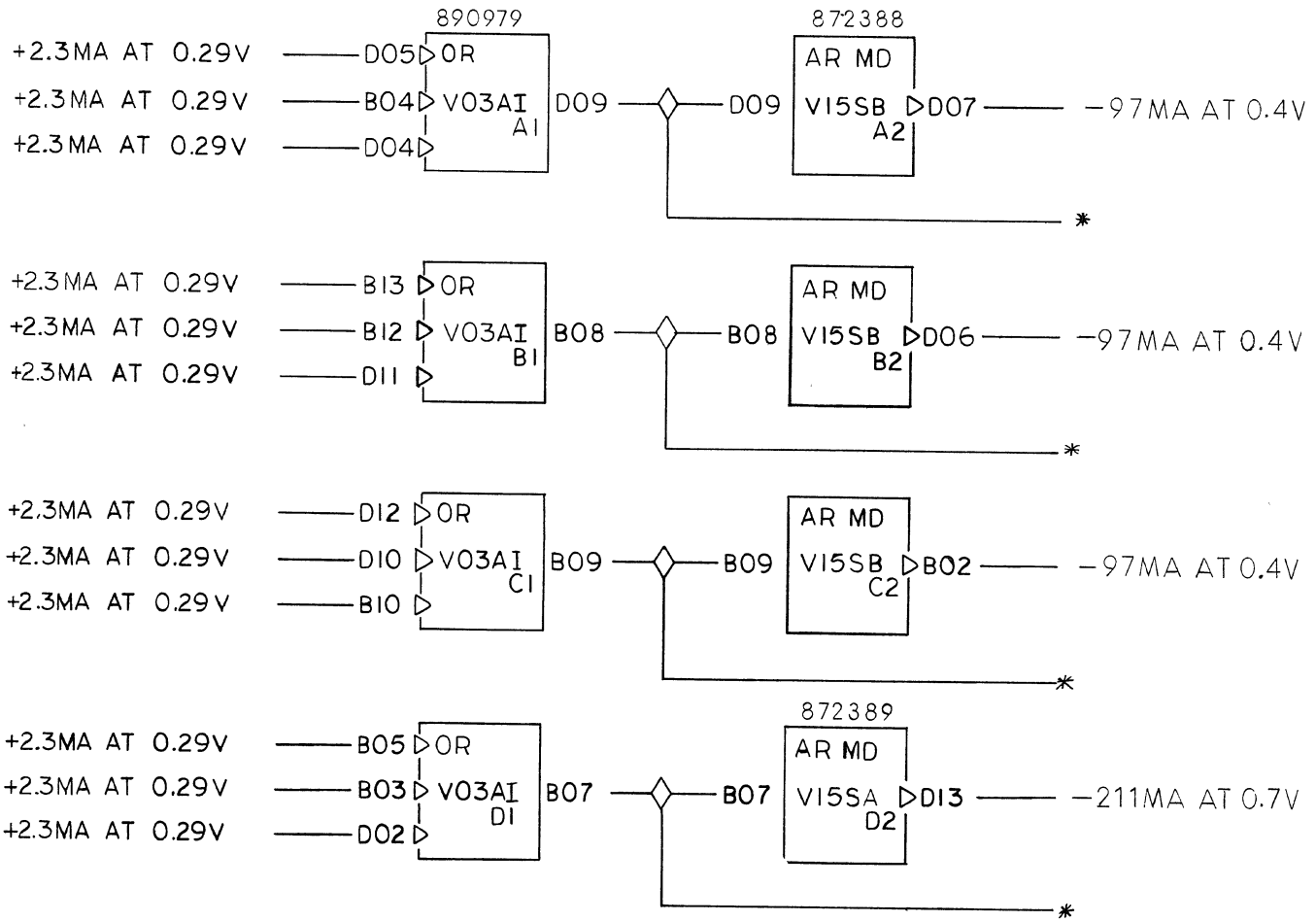
POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	12M
DO8	GND

RELAY DRIVER

CATEGORY CODE

V03	V15

P/N	5800735
EC	163085
SPECIAL	RESTRICTED
CARD SIZE	1-6



* SPECIAL REQ. SEE CIRCUIT SPEC. 872388

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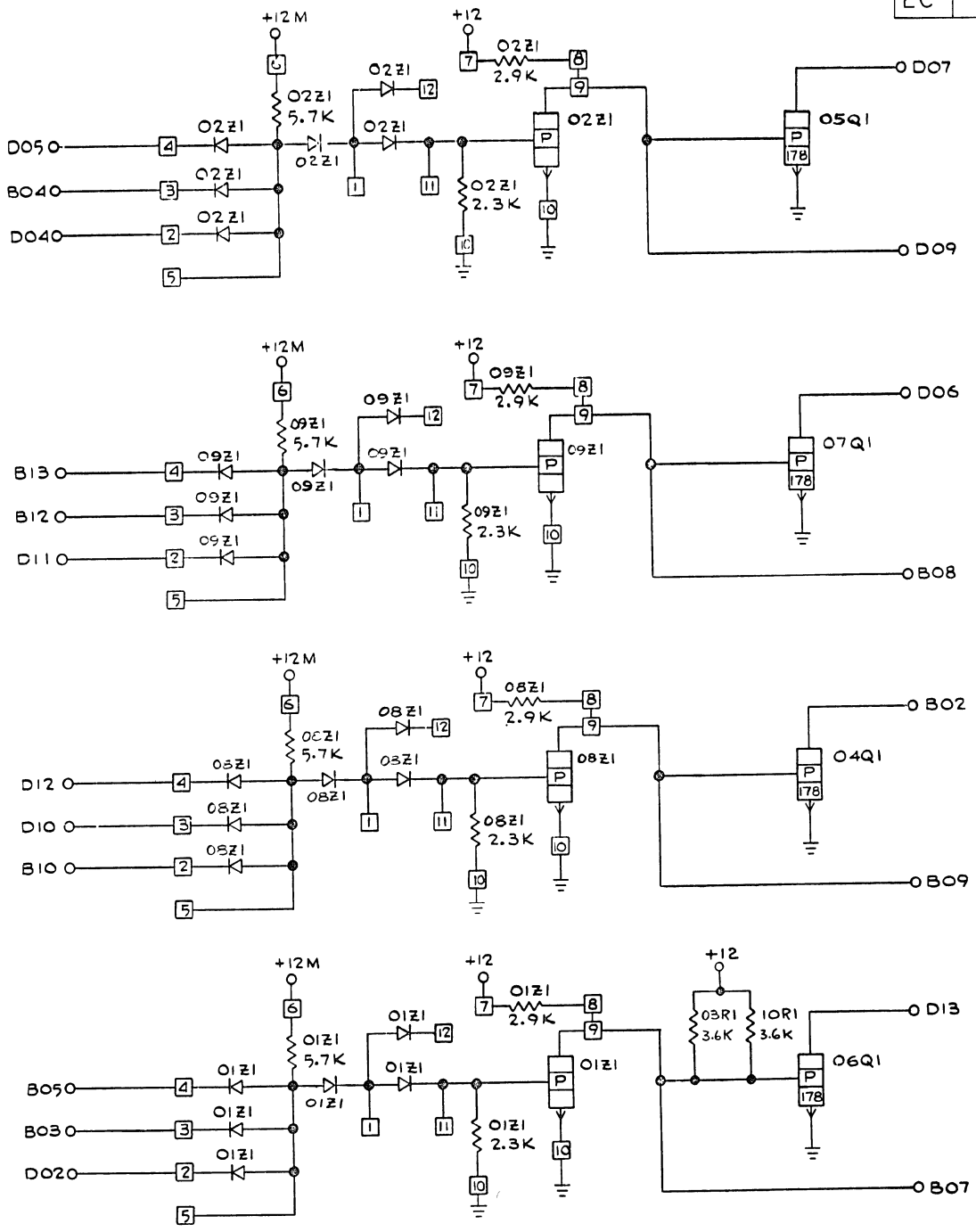
LMH Cat.	0-2860 Subject	513 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

RELAY DRIVER

P/N	5800735
EC	163085



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

VARIABLE SS .99 USEC TO 90 USEC

LMH Cat.	0-2860 Subject	504 Suffix

IBM Location Manufacturing Specification

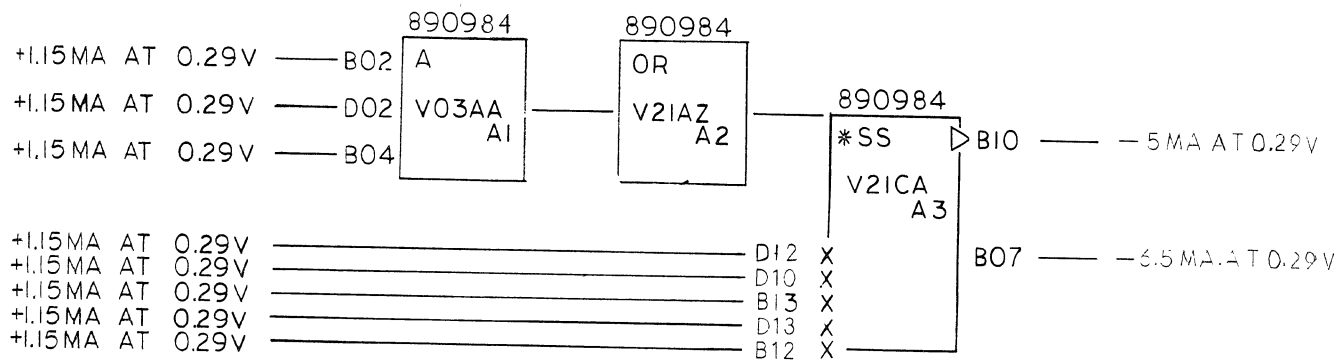
POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	12M
DO8	GND

VARIABLE SS .99 USEC TO 90 USEC

CATEGORY CODE

V03	V21

P/N	5800907
EC	162707
STANDARD	RESTRICTED
CARD SIZE	1-6



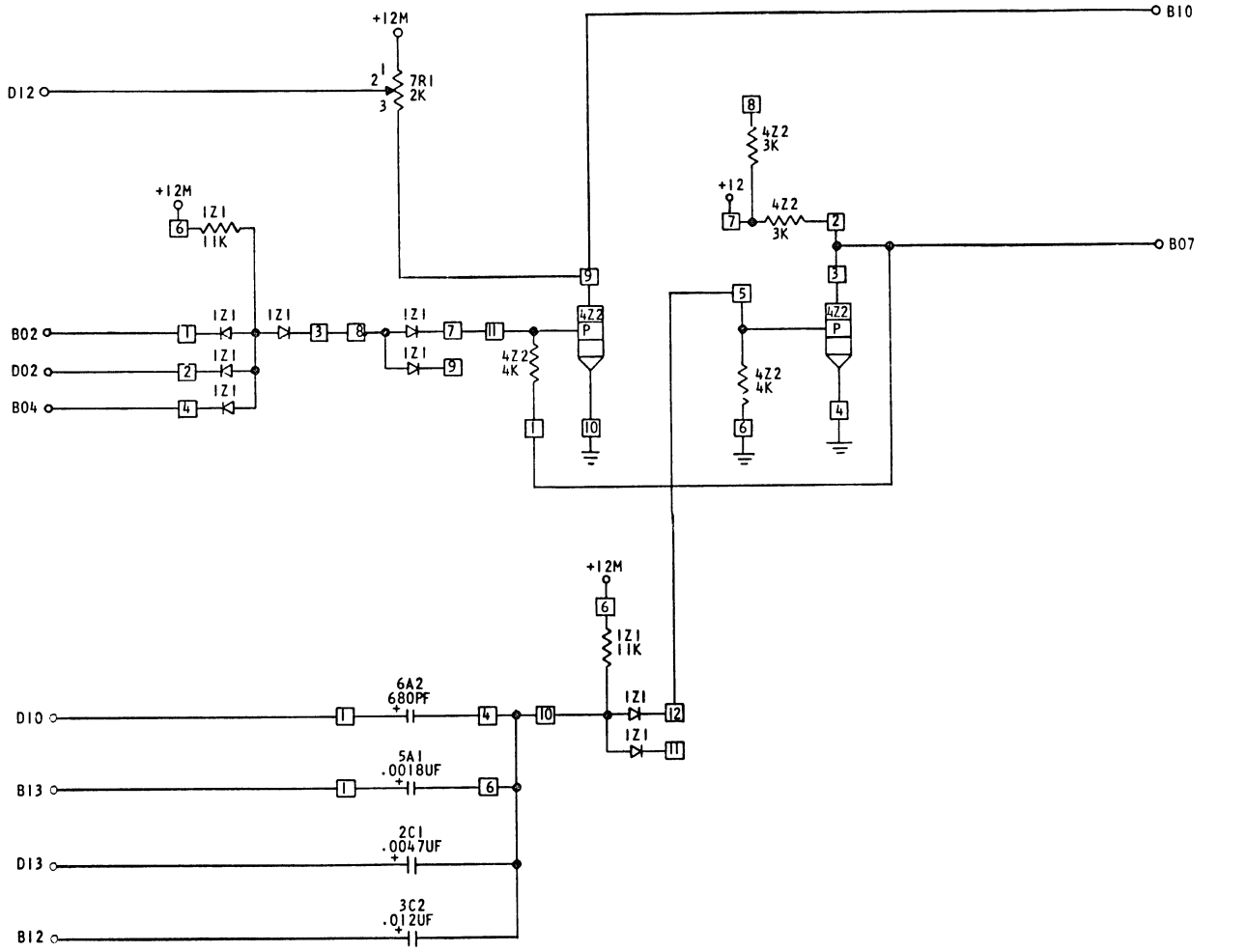
CONNECT PINS	DELAY RANGE
D10	0.99 TO 5.1 US
B13	3.4 TO 13.5 US
D13	9.0 TO 35.0 US
B12	23.0 TO 90.0 US
D12 MUST JOIN 1 LINE ABOVE	

LMH Cat.	0-2860 Subject	504 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

VARIABLE SS .99 USEC TO 90 USEC

P/N	5800907
EC	162707



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

VARIABLE SS 62 USEC TO 4.2 MSEC

LMH	0-2860	503
Cat.	Subject	Suffix

IBM

Location

Manufacturing Specification

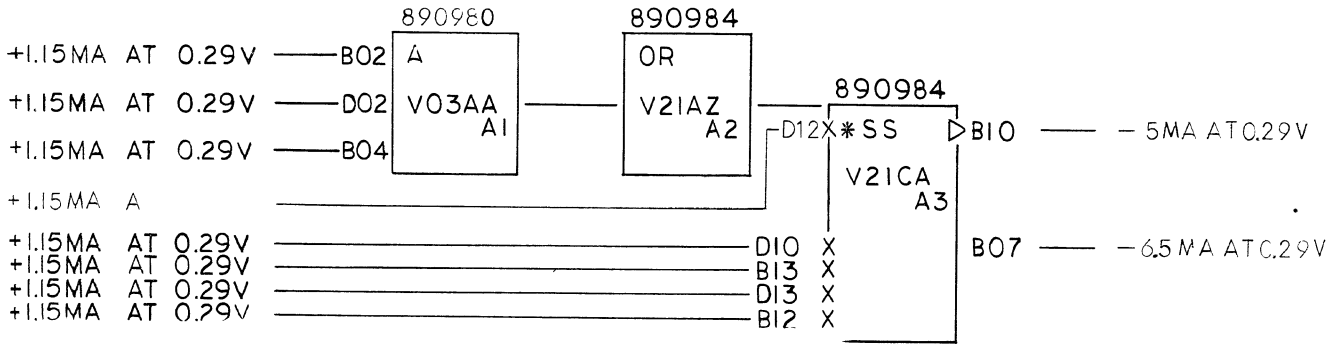
POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	12M
DO8	GND

VARIABLE SS 62 USEC TO 4.2 MSEC

CATEGORY CODE

V03 | V21

P/N	5800908
EC	162701
STANDARD	RESTRICTED
CARD SIZE	1-6



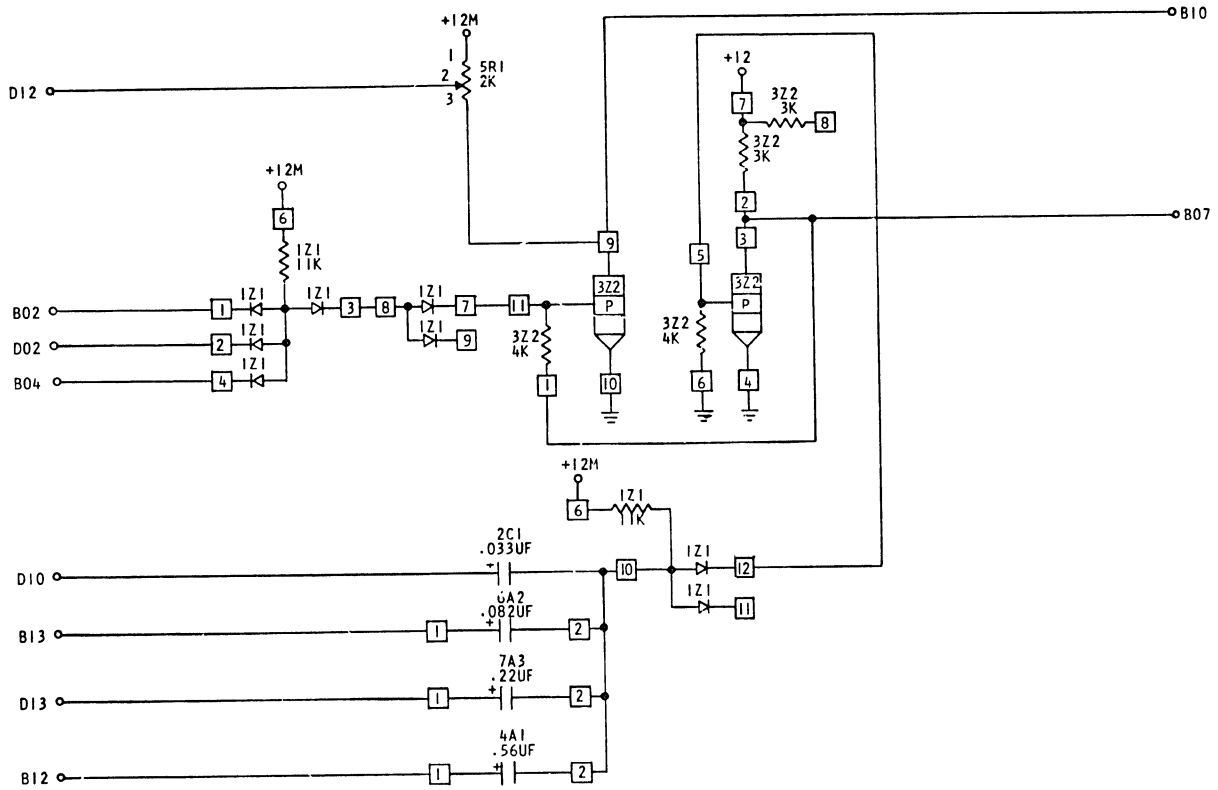
CONNECT PINS	DELAY RANGE
D10	62 TO 248US
B13	153 TO 615US
D13	.41 TO 1.65MS
B12	1.1 TO 4.2MS
D12 MUST JOIN I LINE ABOVE	

LMH Cat.	0-2860 Subject	503 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

VARIABLE SS 62 USEC TO 4.2 MSEC

P/N	5800908
EC	162701



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

VARIABLE SS 2 8MS TO 200MS

LMH	0-2860	501
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

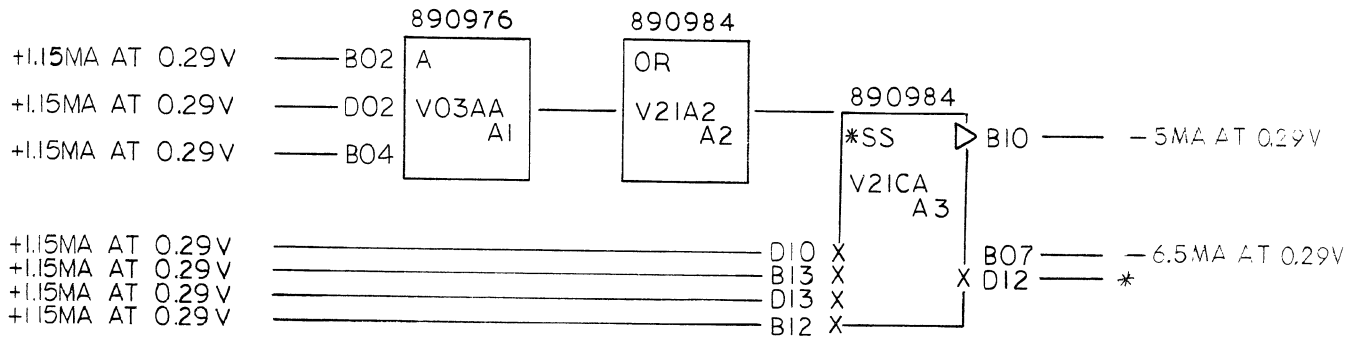
POWER REQUIRED	
PIN	VOLTS
DO3	+12
B11	12M
DO8	GND

VARIABLE SS 2.8MS TO 200MS

CATEGORY CODE

V03	V21

P/N	5800909
EC	171275
STANDARD	RESTRICTED
CARD SIZE	1-6



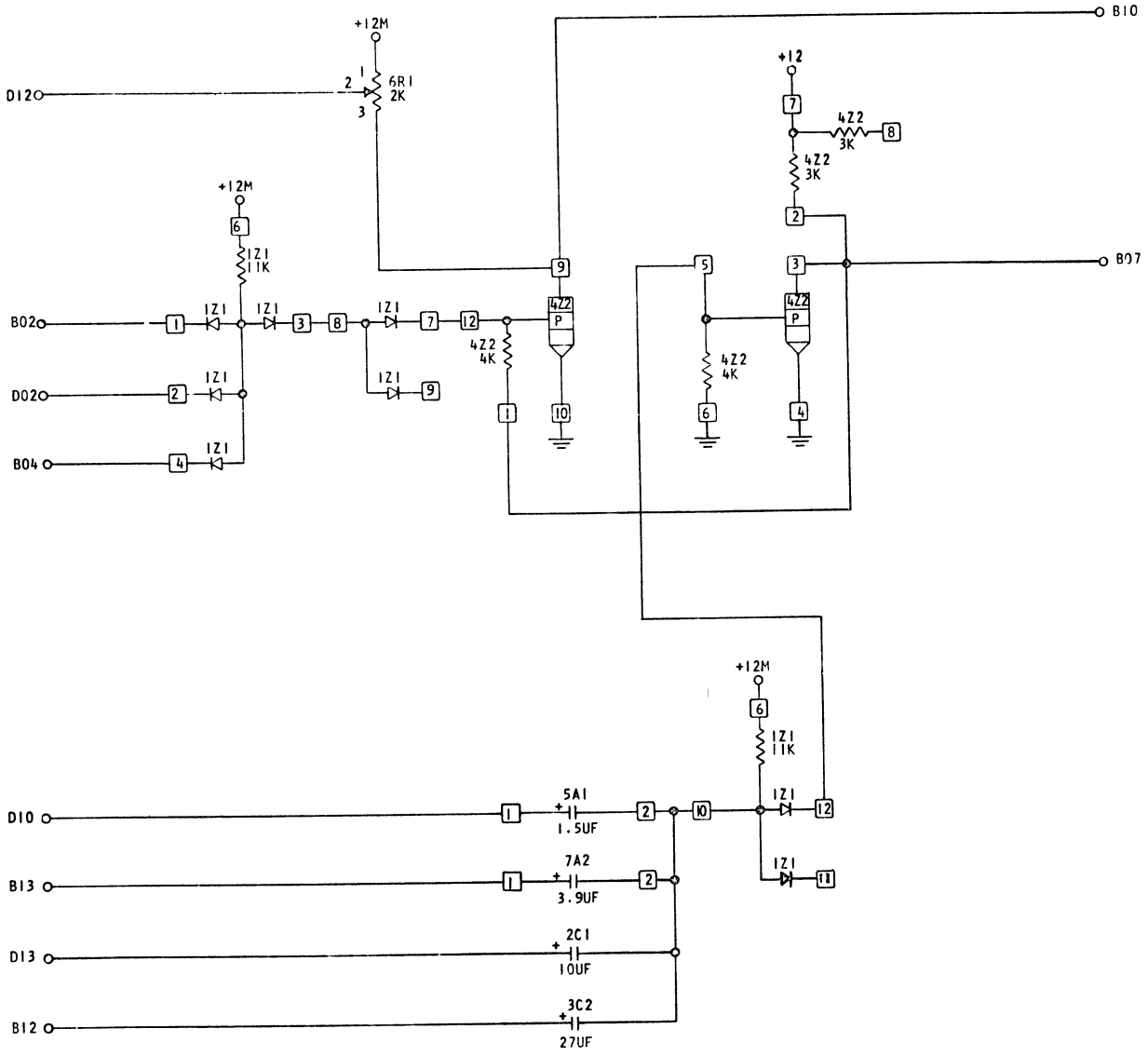
CONNECT PINS	DELAY RANGE
D10	2.8 TO 11MS
B13	7.3 TO 29MS
D13	19 TO 75MS
B12	50 TO 200MS
*	D12 MUST DRIVE 1 TIMING PIN

LMH Cat.	0-2860 Subject	501 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING

VARIABLE SS 2.8MS TO 200MS

P/N	5800909
EC	171275



SPEC. PART NO. 872003 1 M Hz Xtal Oscillator	LMH Cat.	0-2860 Subject	706 Suffix

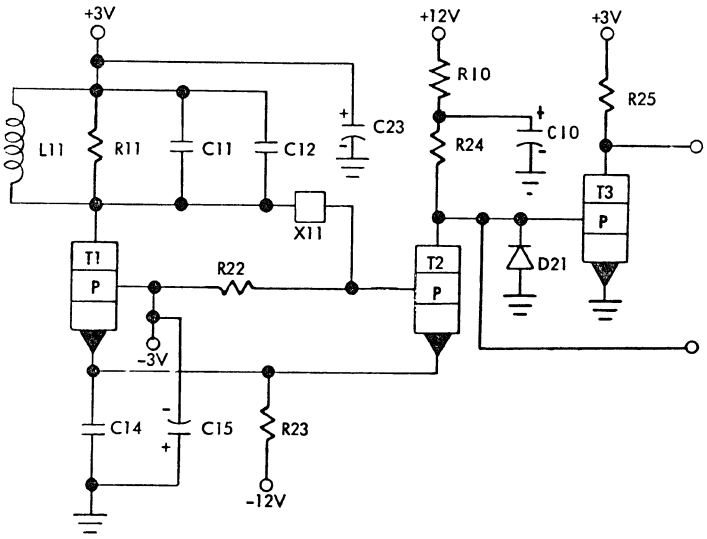
IBM

Location Manufacturing Specification

Referenced Circuit Flyer - S 22 AK.

EC Level-163026

Circuit Schematic - 1 M Hz Xtal Oscillator



X_{11} = 1.00 MC
L_{11} = 20 UH
C_{11} = 820 PF
C_{12} = 430 PF
C_{14} = 22 PF
C_{15} = 0.68 UF
C_{10}, C_{23} = 6.8 UF

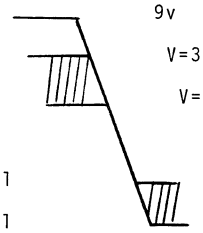
Circuit Description

The 1.00 M Hz free-running crystal oscillator generates standard SLT pulses with the drive capability of a standard SLT AI Block.

Input Requirements

Not Applicable

Output Specifications



Maximum Allowable 9v

Maximum Up Level V=3.12 I=0.0 ma

Minimum Up Level V=2.88 I=0.0 ma

Minimum Down Level V=0.3 I= -18.5 ma

Maximum Down Level V=0.0 I=-18.5 ma

Stray wiring discharge current $C \frac{dv}{dt}$ = 3.5 ma

Delay Parameters

Not Applicable

Power Requirements

VOLTAGE (VOLTS)	MAXIMUM ON CURRENT (ma)
+12	+1.7
-12	-2.7
+ 3	+5.6,-1.0
- 3	+1.2,-1.1

Total Power Dissipation

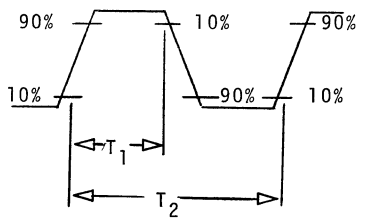
MAXIMUM (mw)
145

Noise Tolerance

Not Applicable

Application Notes

A. Symmetry



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At worst case $T_1 = 0.46\ T_2$ with no load, 3AI, or 5AI loads.

b. Fall time - measured form 10% to 90% in nanoseconds

LOADS	MAX FALL TIMES
Unloaded	24
3AI	30
5AI	34

c. Rise times - measured from 10% to 90% in nanoseconds

LOADS	MAX RISE TIME
Unloaded	80
3AI	130
5AI	150

d. Frequency Stability is 1.0 M Hz $\pm$ 500 Hz from 4°C to 60°C.

SPEC. PART NO. 872004 1.44 M Hz Xtal Oscillator	LMH Cat.	0-2860 Subject	707 Suffix

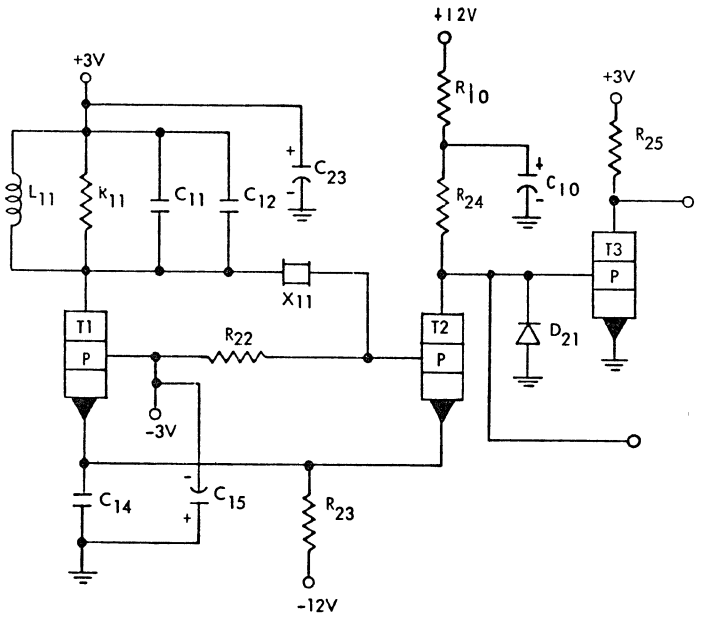
IBM

Location Manufacturing Specification

Referenced Circuit Flyers - S 22 AL

E. C. Level- 163026

Circuit Schematic - 1.44 M Hz Xtal Oscillator



X_{11} = 1.44MC
L_{11} = 13UH
C_{11} = 470PF
C_{12} = 470PF
C_{14} = 22PF
C_{15} = 0.68UF
C_{23}, C_{10} = 6.8UF
R_{10} = 2K
R_{11} = 301Ω
R_{22} = 2.7K
R_{23} = 4.42K
R_{24} = 8.06K
R_{25} = 0.75K
D_{21} = CE

Circuit Description

The 1.44 M Hz free-running crystal controlled oscillator generates standard SLT pulses for voltage mode operation with the drive capability of a standard SLT AI block.

Input Requirements

Not Applicable

Output Specifications

Maximum Allowable	9.0 V	
Maximum Up Level	V=3.12	I= 0.0ma
Minimum Up Level	V=2.88	I= 0.0ma
Minimum Down Level	V=0.3	I= -18.5ma
Maximum Down Level	V=0.0	I= -18.5ma

Delay Parameters

Not Applicable

Power Requirements

VOLTAGE (V)	MAXIMUM ON Current (ma)
+12V	+1.7
-12	-2.7
+3	+5.6 -1.0
-3	+1.2 -1.1

Total Power Dissipation

Maximum (mw)
144

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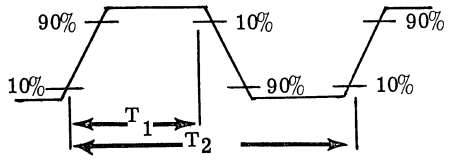
Noise Tolerance

Not Applicable

Application Notes

a. Symmetry



At worst case $T_1 = 0.46T_2$ with no load, 3 AI, or 5 AI loads.

b. Fall times - measured from 10% to 90% in nanoseconds.

Loads	Max Fall Times
Unloaded	20
3 AI	26
5 AI	28

c. Rise times - measured from 10% to 90% in nanoseconds.

Loads	Max Rise Times
Unloaded	70
3 AI	125
5 AI	150

d. Frequency Stability is 1.44 M Hz $\pm$ 720 Hz from 4°C to 60°C.

SPEC. PART NO. 872005 · 1 MHz Gated Oscillator	LMH Cat.	0-2860 Subject	708 Suffix

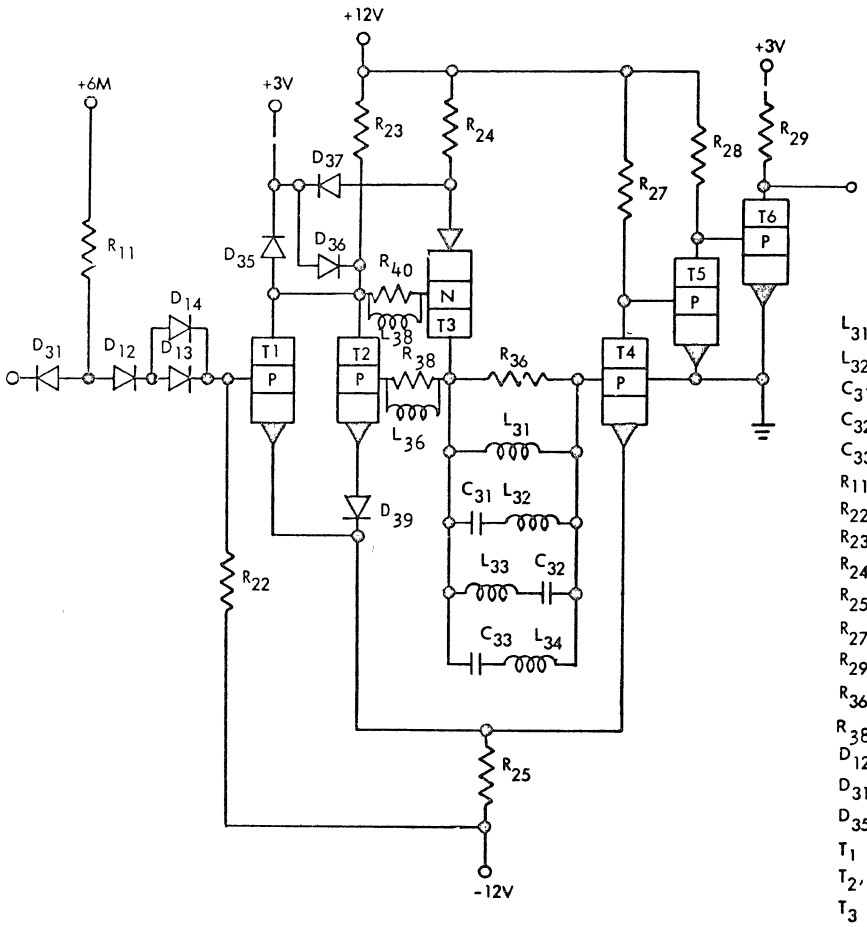
IBM

Location Manufacturing Specification

Referenced Circuit Flyer - S 22 AS.

EC Level-163028

Circuit Schematic - 1 M Hz Gated Oscillator

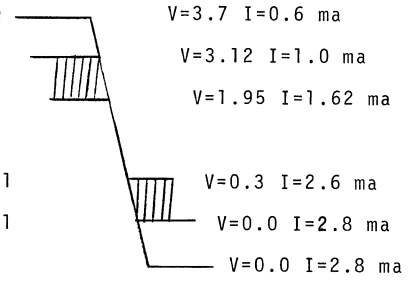


L_{31}	= 163UH
L_{32}, L_{33}, L_{34}	= 81.5UH
C_{31}	= 60PF
C_{32}	= 14.7PF
C_{33}	= 6.8PF
R_{11}	= 2.0K
R_{22}	= 17.4K
R_{23}	= 6.98K
R_{24}	= 2.94K
R_{25}	= 4.64K
R_{27}, R_{28}	= 10.0K
R_{29}	= 0.75K
R_{36}	= 0.75K
R_{38}, R_{40}	= 620Ω
D_{12}, D_{13}, D_{14}	= SLT
D_{31}, D_{37}, D_{39}	= CE
D_{35}, D_{36}	= CD
T_1	= SLT
T_2, T_4, T_5, T_6	= SLT
T_3	= 102
L_{36}, L_{38}	= 1UH

Circuit Description

The gated oscillator generates standard SLT pulses in response to a gate pulse for voltage mode operation with the drive capability of a standard SLT AI block.

Input Requirements



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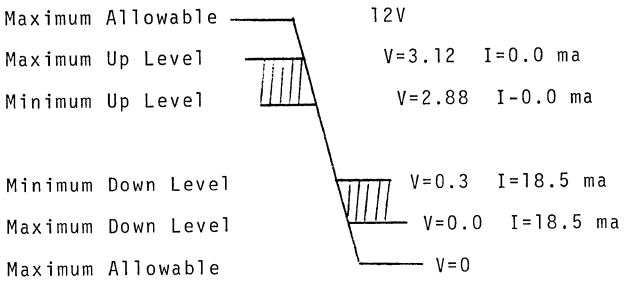
Input fall times must be less than 50 ns when measured from 10% to 90%. The turn-on delay becomes greater as the fall time becomes longer.

Output Specifications



Delay Parameters

Gate Oscillator On Maximum Delay 85 nsec

Gate Oscillator OFF Maximum Delay 60 nsec

Delays were measured with an output load of 5AI inputs.

Power Requirements

VOLTAGE Volts	MAXIMUM Current (ma) ON	OFF
+3	+6.3	0.0
+6M	+3.4	+1.0
+6M(±2v)	+4.3	+0.6
+12v	+7.9	+5.3
-12v	-4.2	-2.7

Total Power Dissipation

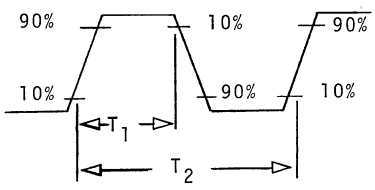
MAXIMUM (MW)
308

Noise Tolerance

Not Applicable

Application Notes

a. Symmetry



At worst case $T_1 = 0.46\ T_2$ with no load, 3AI, or 5AI loads

b. Fall time - measured from 10% to 90% in nanoseconds.

LOADS	MAX FALL TIMES
Unloaded	32
3AI	45
5AI	50

c. Rise time - measured from 10% to 90% in nanoseconds

LOADS	MAX RISE TIMES
Unloaded	37
3AI	45
5AI	50

d. Frequency Stability is 1 M Hz -5% to +7% o°C to 60°C

SPEC. PART NO. 872075 4.4 K Hz Xtal Oscillator	LMH Cat.	0-2860 Subject	717 Suffix

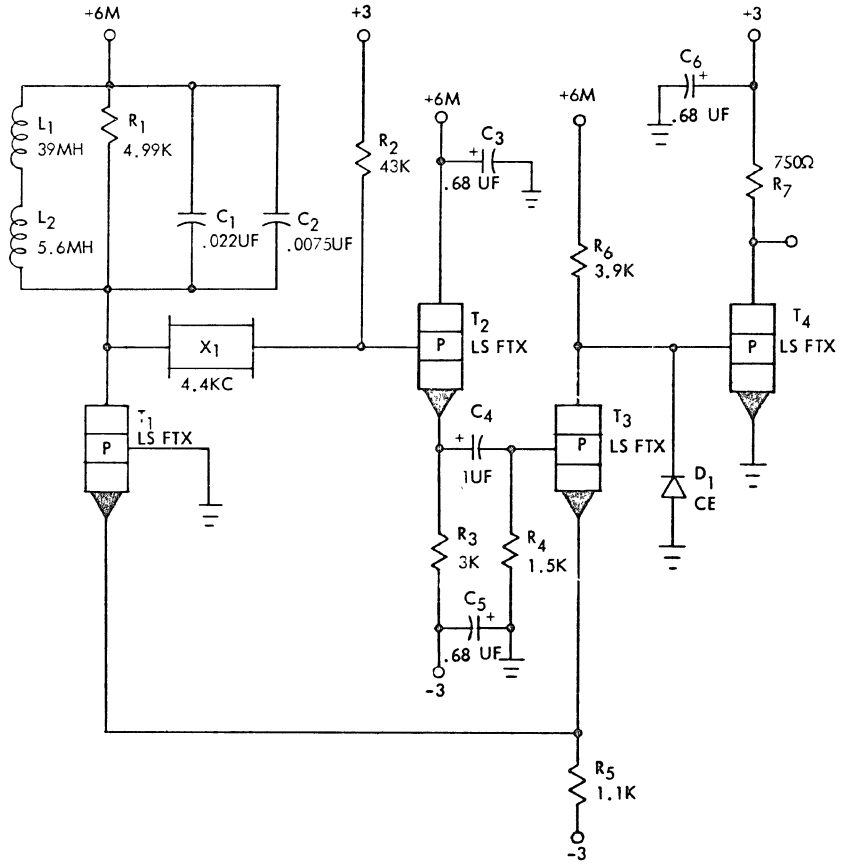
IBM

Location Manufacturing Specification

Referenced Circuit Flyer - S 22 CX .

EC Level 162295

Circuit Schematic - 4.4 K Hz Xtal Oscillator



Circuit Description

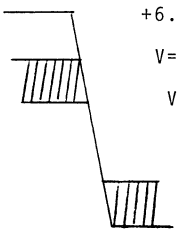
Oscillator generates standard SLT pulses.

Input Requirements

Not Applicable

Output Specifications

Maximum Allowable	+6.0v
Maximum Up Level	V=3.12 I=0.0 ma
Minimum Up Level	V=2.7 I=0.0 ma
Minimum Down Level	V=0.3 I=14.5 ma
Maximum Down Level	V=0.0 I=14.31 ma



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Delay Parameters

Not Applicable

Power Requirements

VOLTAGE (Volts)	MAXIMUM Current (ma)
+6M	+7.0
+3	+4.5
-3	-5.2

Total Power Dissipation

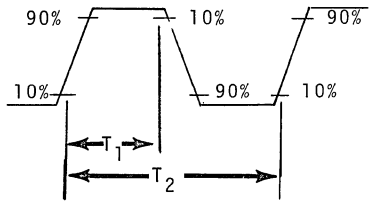
MAXIMUM (MW)
90.5

Noise Tolerance

Not Applicable

\pplication Notes

a. Symmetry



$$\% \text{ SYM} = \frac{T_1}{T_2} \times 100\%$$

Worst case % SYM = 41%

b. Fall time - measured from 10% to 90% in nanoseconds

LOADS	MAX FALL TIMES
2AI	72
4AI	240

c. Rise time - measured from 10% to 90% in nanoseconds

LOADS	MAX RISE TIMES
2AI	104
4AI	500

d. Frequency Stability is 4.4 k Hz $\pm$ .1% from 10°C to 55°C

SPEC. PART NO. 872656 2.0K Hz Oscillator	LMH Cat.	0-2860 Subject	744 Suffix

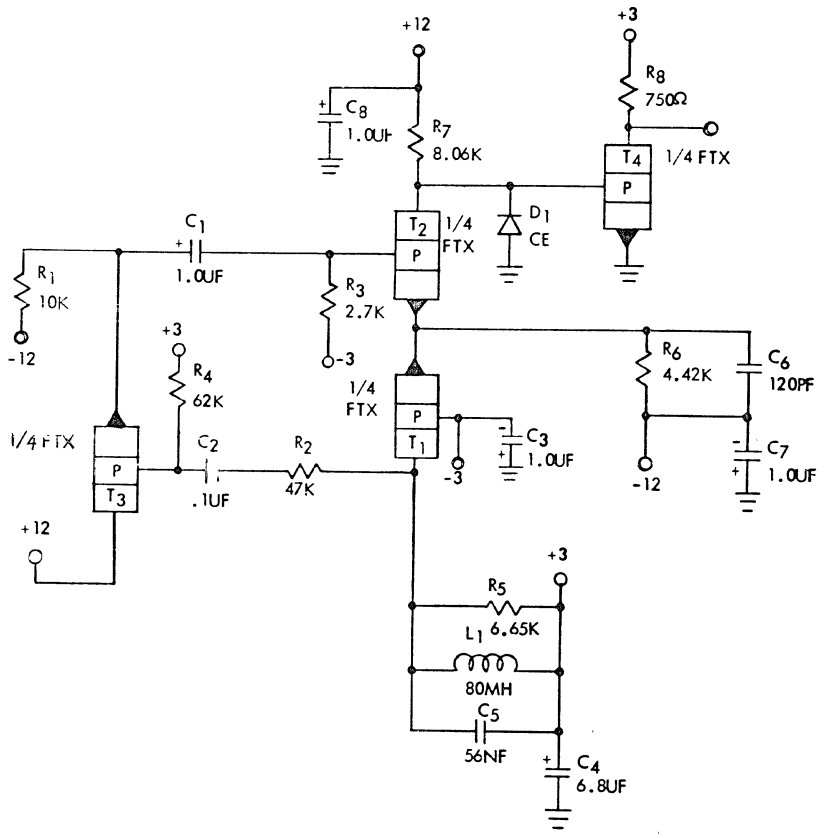
IBM

Location Manufacturing Specification

Referenced Circuit Flyer - T22AB

EC Level-163205

Circuit Schematic - 2.0K Hz Oscillator



Circuit Description

This circuit generates standard SLT pulses for voltage mode operation and has the drive capability of a standard SLT AI block.

Input Requirements

Not Applicable

Output Specifications

Maximum Allowable	V=12.0 I=0 ma
Maximum Up Level	V=3.12 I=0 ma
Minimum Up Level	V= 2.88 I=0 ma
Minimum Down Level	V=0.3 I= -14.31 ma
Maximum Down Level	V=0.14 I= -14.31 ma

Delay Parameters

Not Applicable

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SPEC. PART NO. 872656

2.0K Hz Oscillator

Power Requirements

VOLTAGE	Maximum Current(ma)
+12	+3.7
-12	-5.0
+3	+6.1
-3	+1.3

Total Power Dissipation

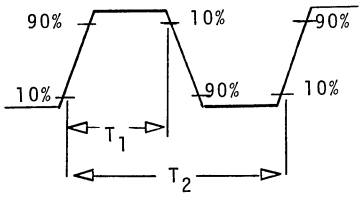
Maximum (MW)
235.6

Noise Tolerance

Not Applicable

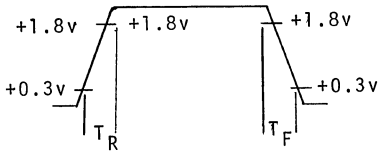
Application Notes

(a) Symmetry



At worst case T_1 = 0.46 T_2 with no load, 3AI or 5AI loads.

(b)



T_R = Rise Time T_F = Fall Time

	Max.
turn-on (tf) in nsec	1700
turn-off (tr) in nsec	1500

(c) Frequency stability is 2.0K Hz ± 200 Hz from 25°C to 50°C.

SPEC. PART NO. 872775 2M Hz Oscillator	LMH Cat.	0-2860 Subject	751 Suffix

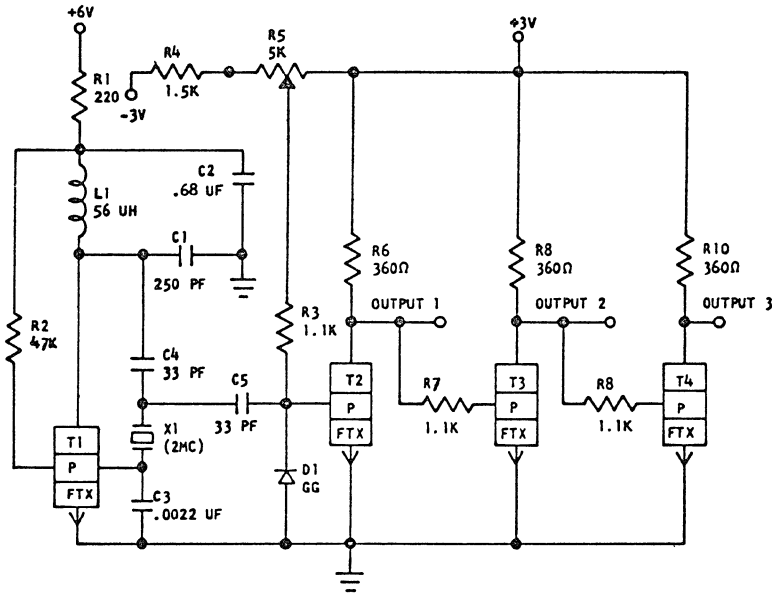
IBM

Location Manufacturing Specification

Referenced Circuit Flyer - T22SB

EC Level-168322

Circuit Schematic - 2M Hz Oscillator



Circuit Description

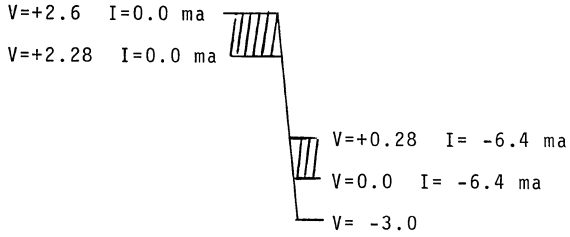
This circuit consists of a 2M Hz crystal oscillator and saturating inverters. Three pulse output waveforms are available, two that are inverted and nonsymmetrical, and one with a symmetry adjustment. The symmetrical output also allows a ± 20 nsec adjustment.

Input Requirements

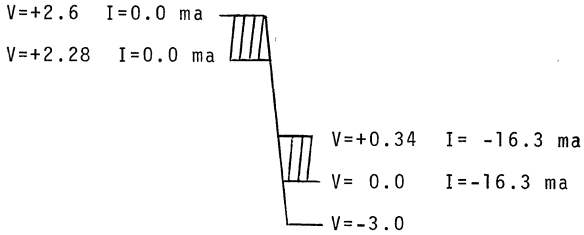
Not Applicable

Output Specifications

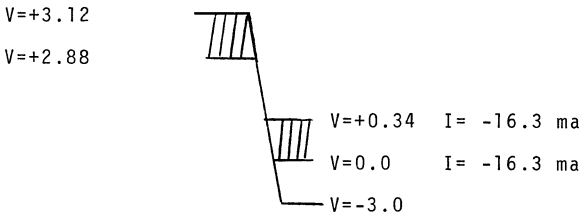
1. Output 1 Voltage Levels:



2. Output 2 Voltage Levels:



3. Output 3 Voltage Levels:



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SPEC. PART NO. 872775
2M Hz Oscillator

Delay Parameters

Not Applicable

Power Requirements

VOLTAGE (v)	Maximum ON Current (ma)
+6	+6.0 ma
+3	+25.0 ma
-3	-3.0 ma

Total Power Dissipation

Maximum (mw)
148.7

Noise Tolerance

Not Applicable

Application Notes

(a) Frequency Stability is 2M Hz ± .05%

(b) Output 1 can drive 2 medium speed AI's

(c) Output 2 and 3 can drive 5 medium speed AI's

SPEC. PART NO. 873400 Exclusive OR-XOR	LMH Cat.	0-2860 Subject	760 Suffix

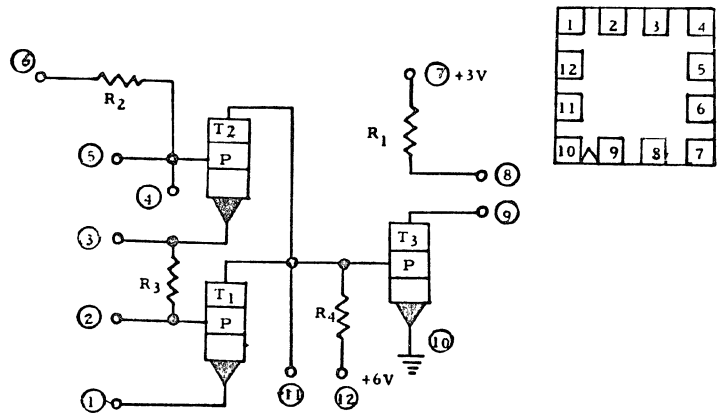
IBM

Location Manufacturing Specification

Referenced Circuit Flyers - T03AI, T03AP, T61AJ

EC Level-752349

Circuit Schematic - Exclusive OR - XOR



R_1 = 300 ohm
R_2 = R_3 = 1.3K ohm
R_4 = 2K ohm
Ref: Module P/N 361477

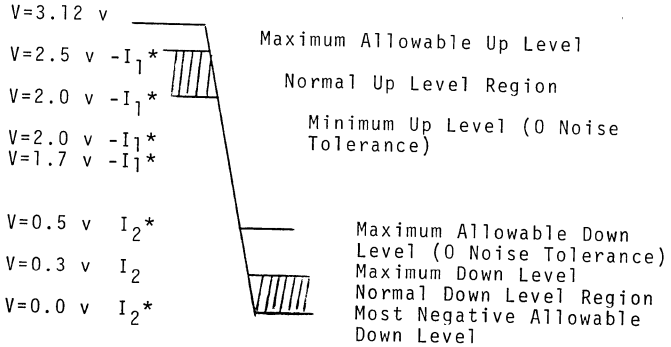
Circuit Description

This circuit performs the exclusive OR of the signals applied to pins 5 and 3, when pins 6 and 1 are tied together. When both inputs are up or both are down, the output will be at a potential of less than 0.3V.

When the inputs are not identical (i.e., one up and one down), the output will be up at a potential around 3.0V depending on the collector load.

Input Requirements

Voltage and current levels



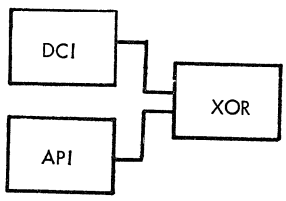
I_1* See Figure 1

In General, $I_2^* = 3.07 + \frac{2.84}{1.26K + .95R_C}$ ma.

R_C is the collector resistor returned to +3v of the circuit driving the opposite XOR input.

For R_C = 750Ω I_2* = 4.2 ma
375Ω 4.8 ma

USE OF FIGURE 1



Example:

To find the Up levels of the XOR inputs proceed as follows:

Collector Resistor of API = 300Ω = R_2

Collector Resistor of DCI = 350Ω = R_1

Assume V_1 = 2.0v
for R_2 = 300 (.95) = 285Ω I_1^* = 1.3 ma
then, $\frac{2.88-2.0}{105\ R_1} \geq 1.3$ ma
and 2.4 ma > 1.3 ma if $V_1 \geq 2.0$v

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SPEC. PART NO. 873400

Exclusive OR-XOR

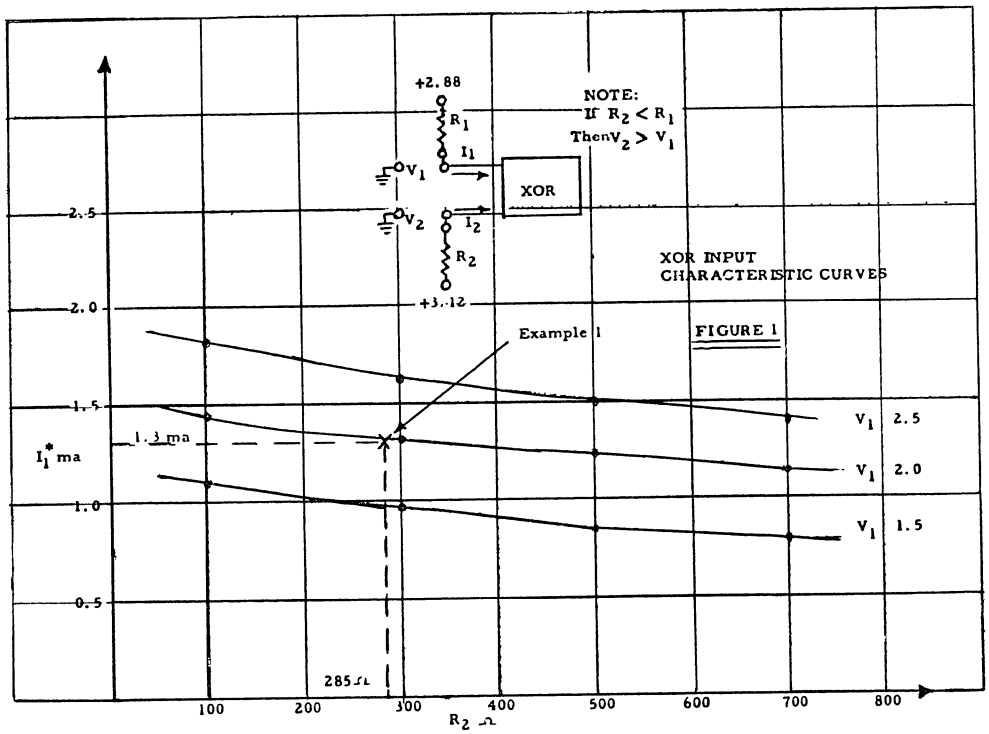


FIGURE 1

Output Specifications

V=9v I= -5ma — Maximum Allowable Up Level

V=+3v ±4% I=0ma — Normal Up Level Region

V=*I= -3ma — Minimum Up Level (0 Noise Tolerance)

V=0.3v I= -38ma — Maximum Saturated Down Level

V=0.0v I= 0ma — Normal Down Level Region / Most Negative Allowable Down Lev.

V* = Determined by collector load impedance.

Delay Parameters

Conditions:

1. 60 pf stray capacitance on the collector.
2. All components and Power Supplies at W.C.
3. W.C. ON delay was taken for a fan-out of 10 W.C. off AI's.
4. W.C. OFF delay was taken with a fan-out of one W.C. ON AI.
5. Taken at 25°C.

W.C. ON $\leq$ 40 nsec. W.C. OFF $\leq$ 55 nsec

Power Requirements

VOLTAGE (Volts)	Maximum Current (ma) ON	OFF
+6M	+04.6	+5.5
+3	+10.1	0
-3	-01.8	-1.5
GND	-35.3	0

Total Power Dissipation

MAXIMUM (mw)	
ON	OFF
59	24

Noise Tolerance

Input Pulse Width $\geq$ 20 nsec.

1. Positive Noise Tolerance: Greater than or equal to 200 mv above 0.3v reference.
2. Negative Noise Tolerance: Greater than or equal to -300 mv from 2.0v reference.
3. The input noise tolerance is decreased by 10 mv for each dot-ORed collector

Application Notes

Wiring Rules

a. Inputs

Since the input levels of the XOR are defined by the collector resistors tied to these inputs, the noise tolerance at this input can be very small. To insure proper operation, the entire net on any XOR input should be contained on the card adjacent to it.

b. Outputs--API Wiring Rules

c. The distance between dot-ORed blocks is limited when one of the dotted collectors must remain on when the other collectors are turned "off". The distance of the load to any one of the remaining "on" collectors is limited to a maximum of 10" of line.

d. Average delay per stage is 33 nsec.

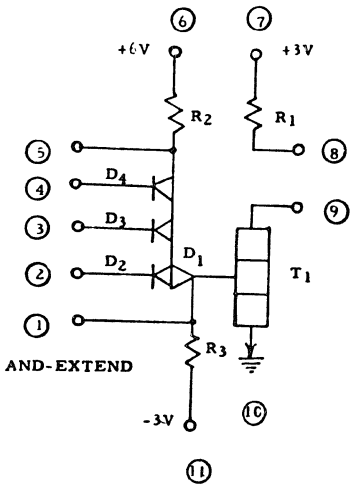
SPEC PART NO. 873401 AND Power Invert	LMH Cat.	0-2860 Subject	761 Suffix

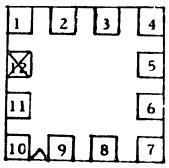
IBM Location Manufacturing Specification

Referenced Circuit Flyers - T03AF, T03AJ, T61AJ, T03AN, T03AO

EC Level-752349

Circuit Schematic - AND Power Invert





R_1 = 300 ohm

R_2 = 1K ohm

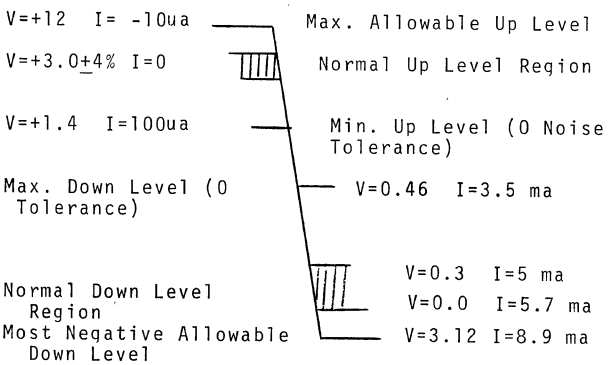
R_3 = 2.5K ohm

Reference: Module P/N 361473

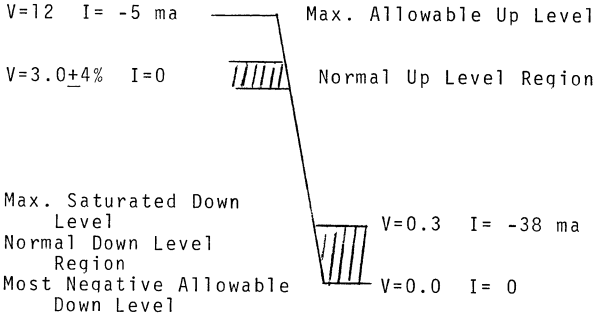
Circuit Description

The API module is used for a power inverter with logic capability at the input. The API serves the same logic function as an AI module, but has higher fan-out capabilities. The API module consists of a diode positive AND circuit followed by a saturating inverter.

Input Requirements



Output Specifications



$$C \frac{dv}{dt} = 4 \text{ ma}$$

Delay Parameters

	Delay Used By SLDA	8" Net		48" Net	
		BC	WC	BC	WC
Output Rising	27	5	32	10	42
Output Falling	13	5	15	10	22

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SPEC PART NO. 873401

AND Power Invert

Power Requirements

VOLTAGE	MAXIMUM Current (ma)	
	ON	OFF
+6	+04.6	+5.5
+3	+10.1	0
-3	-01.8	-1.5
GND	-35.3	0

Total Power Dissipation MW

MAXIMUM	
ON	OFF
73	38

Noise Tolerance

1. Positive Noise — Pulse width $\geq$ 20 nsec. Positive noise tolerance is 160 mv referenced to 0.3v (Down (Level). For DOT-ORing, the positive noise tolerance is decreased by 10 mv for each dotted collector.

2. Negative Noise — Pulse width $\geq$ 20 nsec Negative noise tolerance is 1.5v referenced to 2.88v (Up Level)

Application Notes

Wiring

a. The maximum net length at either the input or output must not exceed six feet of line.

b. The input line to an API must not exceed four feet if driven by an API or DCI (Single line in channel).

c. If there are two lines switching simultaneously, the maximum input line length is eighteen inches.

And Fan In Rules

a. Maximum of 5 AND diodes for quoted Worst Case Delays. (W.C. "on" $\leq$ 19 nsec., W.C. "off" $\leq$ 37 nsec.)

b. Maximum of 17 AND diodes allowable.

Dot-Oring Rules

The number of dot-ORed collectors is limited by the allowable noise tolerance reduction at the input of each of the dot-ORed blocks.

The distance between dot-ORed blocks is limited only when one of the dotted collectors must remain "on" when the others are turned "off".

The distance of API loads to any one remaining "on" collector is limited to a maximum 6" line.

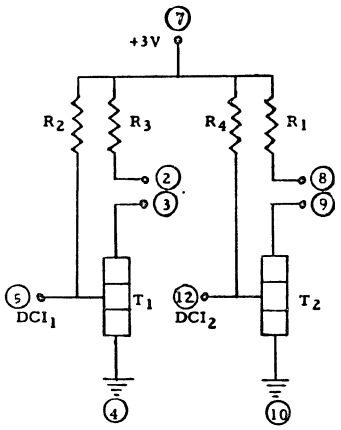
SPEC. PART NO. 873402 Direct Coupled Inverter - DCI	LMH Cat.	0-2860 Subject	762 Suffix

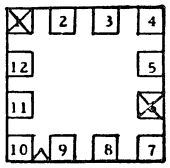
IBM Location Manufacturing Specification

Referenced Circuit Flyers - T05AA, T05AB, T61AC

EC Level 752349

Circuit Schematic - Direct Coupled Inverter - DCI





R_1, R_3 = 350 ohm

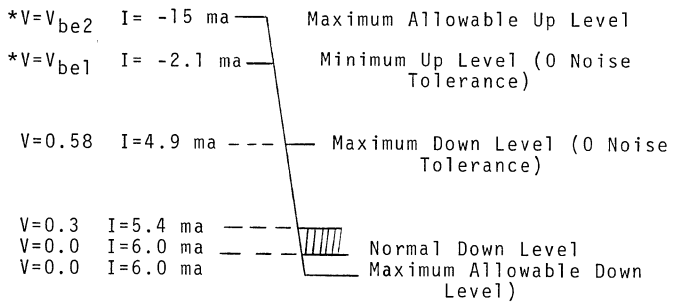
R_2, R_4 = 550 ohm

Reference: Module P/N 361454

Circuit Description

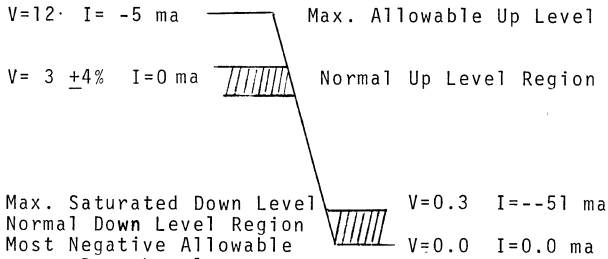
The DCI module contains two separate direct coupled inverters. These inverters extend the fan-out of an AI or an AOI module by a factor of 3.

Input Requirements



*Defined by the V_{be} - I_b characteristics.

Output Specifications



$$C \frac{dv}{dt} = 5 \text{ ma}$$

Delay Parameters

	Delay Used By SLDA	Delay Limits 8" net BC	Delay Limits 8" net WC	Delay Limits 48" net BC	Delay Limits 48" net WC
Output Rising	17	5	20	5	25
Output Falling	17	5	20	5	25

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SPEC. PART NO. 873402

Direct Coupled Inverter - DCI

Power Requirements

VOLTAGE (Volts)	MAXIMUM Current(ma) ON	OFF
+3	+13	+6
GND	-59	0

Total Power Dissipation In MW

Component	Maximum ON	OFF
Total Single DCI Power Dissipation	59	17
Total Module Power Dissipation	118	34

Noise Tolerance

Positive Noise -- For pulse widths $\geq$ 20 nsec. The noise tolerance is 280 mv referenced to 0.3 V saturated collector level.

Negative Noise -- For pulse widths of $\geq$ 20 nsec., the noise tolerance is 0V.

Application Notes

1. Wiring Rules

   a. The maximum net length at output should be less than 6 ft.

   b. The input line length is restricted to 6 inches because of coupled noise when adjacent lines are switching. The block driving the DCI cannot have additional fan-outs.

   c. The maximum single wire length in the output should be less than 1.5 ft.

Special Input Rules

Driving source (AI, AOI, API, II, DCI) can drive nothing else.

SPEC. PART NO. 873409 Isolating Inverter II	LMH Cat.	0-2860 Subject	764 Suffix

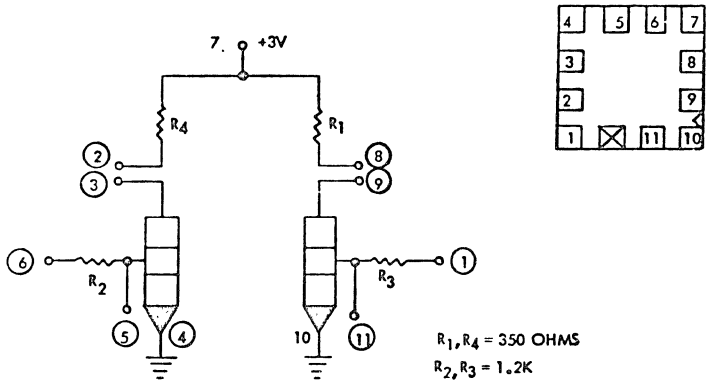
IBM

Location Manufacturing Specification

Referenced Circuit Flyer - SO5AS, SO5AH, T61AC

E.C. Level-752464

Circuit Schematic - Isolating Inverter, II



R_1, R_4 = 350 OHMS
R_2, R_3 = 1.2K

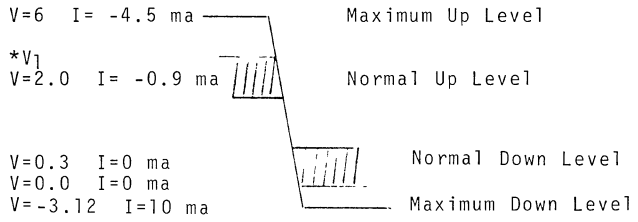
MODULE PART NO.: 361479

Circuit Description

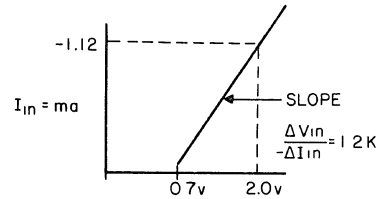
The II module contains two separate inverters. The inverter presents a 1.2 K series resistance when connected to the driving block.

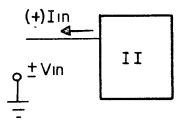
Input Requirements

Voltage and Current Levels:



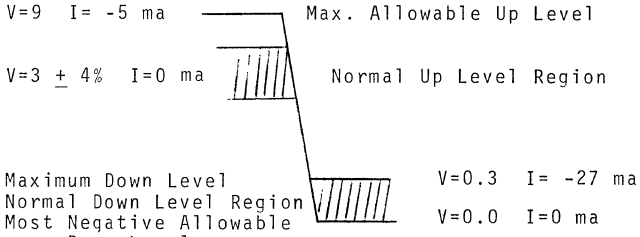
*V_1 is defined by the equivalent circuit and the collector load resistance.





V_{in} = volts
I_{DC} = Steady State Input Current = -0.9 ma (Up Level Load Only)

Output Specifications



$$C \frac{dv}{dt} = 3.5 \text{ ma}$$

Delay Parameters

Output Rising	40 ns
Output Falling	40 ns

Power Requirements

VOLTAGE (Volts)	Maximum Current (ma) ON	OFF
+6	--	--
+3	+8.8	0
-3	--	--
GND	+25.1	0

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Total Power Dissipation In MW

ON	OFF
35.3	0

Noise Tolerance

Positive Noise - Pulse Width $\geq$ 25 nsec. The DC noise tolerance is 280 mv from +0.3V level at 25°C.

Negative Noise - Pulse Width $\geq$ 25 nsec. The DC noise tolerance at input is V_1 - 2.0V at 25°C.

Wiring Rules

Maximum net length - The maximum net length at either input or output should not exceed 6 ft. of line.

Input Restrictions - The input line length should not exceed 9 inches to prevent excessive coupled noise.

Output Restrictions - The maximum single wire length should be less than 1.5 ft. to prevent large reflections and coupled noise.

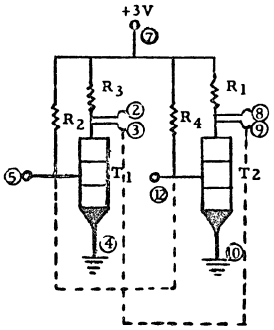
SPEC. PART NO. 873410	LMH Cat.	0-2860 Subject	765 Suffix
High Power Driver (HPD)			

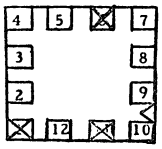
IBM Location Manufacturing Specification

Referenced Circuit Flyers - T15AA, T15AE, T06AR

EC Level-752349

Circuit Schematic - High Power Driver (HPD)





R_1, R_3 = 350 ohms

R_2, R_4 = 550 ohms

Reference Module Part No. 361475

Circuit Description

The HPD module is a specially selected DCI module with the two inverters wired in parallel. The driving block can be an AI or AOI but the collector resistor has to return to a +6v supply. The HPD has a fan-out capability of 36 AI's or equivalent load.

Input Requirements

*$V = V_{be2}$ I= -15 ma — Max. Allowable Up Level

*$V = V_{be1}$ I= -5.8 ma — Min. Up Level(0 noise tol.)

V=0.58 I=9.8 ma — Max.Down Level(0 noise Tol.)

Normal Down Level Region

V=0.3 I=10.8 ma
V=0.0 I=12.0 ma

Most Negative Allowable Down Level — V=0.0 I=12.0 ma

*Defined by the V_{be} vs I_b characteristic

Output Specifications

V=12 I= -10 ma — Max. Allowable Up Level

V=3.12 I=0 ma

V=2.88 I=0 ma — Normal Up Level Region

Normal Down Level Region — V=0.3 I= -111 ma

Min. Allowable Down Level — V=0.0 I=0 ma

V=0.0 I=0 ma

$C \frac{dv}{dt} = 10$ ma

Delay Parameters

	Delay Used By SLDA	Delay Limits 8" Net BC	8" Net WC	48" Net BC	48" Net WC
Output Rising	17	5	20	5	25
Output Falling	17	5	20	5	25

Power Requirements

VOLTAGE (Volts)	Maximum Current (ma) ON	OFF
+6m	---	---
+3	26	6
-3	---	---
GND	-126	0

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SPEC. PART NO. 873410
High Power Driver (HPD)

Total Power Dissipation

MAXIMUM (MW)	
ON	OFF
120	34

Noise Tolerance

Input Noise Sensitivity

1. Positive Noise - For pulse widths of 20 nsec or larger the noise tolerance is 280 mv referenced to 0.3v, staturated collector level of driver. T = 75°C

2. Negative Noise - For pulse widths of 20 nsec or larger, the noise tolerance is 0v. T = 75°C.

Application Notes

1. Wiring Rules

   A. Maximum single line length = six inches when only one load is being driven at the end of the line. No maximum load restriction.

   B. A minimum of at least three AI loads or equivalent must be at the end of the line if it is one foot long. The maximum load on each one foot lone is 12 AI or equivalent.

   C. For a single line length longer than one foot and extending to another board, the line must be terminated. The maximum single line length is four feet and the maximum loading is 6AI or equivalent per line.

   D. The maximum net length in this case can be as much as 24 feet, but to prevent excessively long circuit delays, a reasonable net length of six feet is tolerable.

SPEC. PART NO. 873416 15 ma Switch (ID)	LMH Cat.	0-2860 Subject	767 Suffix

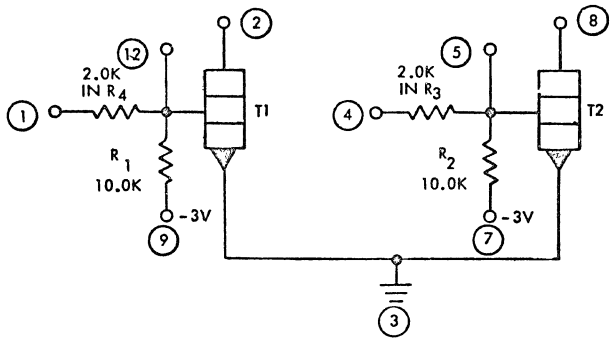
IBM

Location Manufacturing Specification

Referenced Circuit Flyers - T 55 AD, T 55 AF

EC Level - 725074

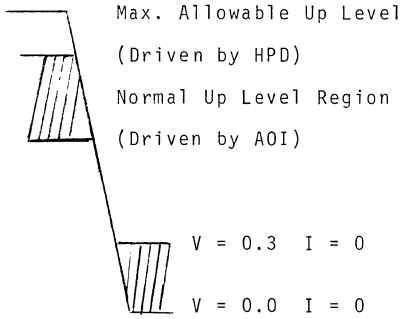
Circuit Schematic - 15 ma Switch (ID)



Circuit Description

This circuit is a simple current switch for application where speed is not essential such as for an indicator driver.

Input Requirements



Output Specifications

Collector Current Available

I_c max. = 19.0 ma at V_{ce} = 0.3v

Delay Parameters

Not Applicable

Power Requirements

(Power Supply Current Requirements in Milliamperes)

VOLTAGE (Volts)	Maximum Current (ma)	
	ON	OFF
-3	1.4	0.8
GND	21.3	--

Total Power Dissipation

Maximum (mw)	
ON	OFF
11.74	0

Noise Tolerance

Not Applicable

Application Notes

a. Medium Speed Application uses lamp number 2-456-016, and +3v Power Supply for collector of ID.

b. Wiring Rules -- The wire length from the output of the ID to the lamp can be 10 feet of board wiring or 50 feet of flat cable.

c. Lamp Test -- With 12 v ± 4% applied at the 10K input and with the 2K input held at 0.3v, the transistor will saturate and the lamp will turn on.

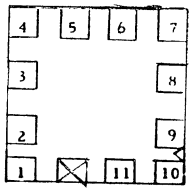
SPEC. PART NO 890971 AND INVERT	LMH Cat.	0-2860 Subject	789 Suffix

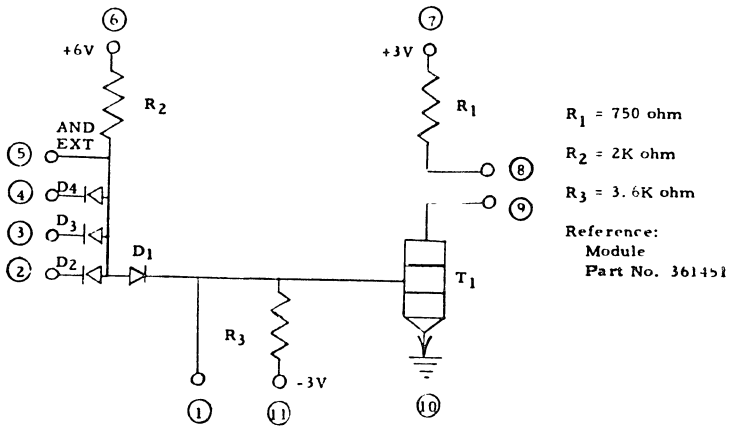
IBM Location Manufacturing Specification

Referenced Circuit Flyers - T03AA, T03AB, T61AA, T61AB

EC Level-752349

Circuit Schematic - AND INVERT

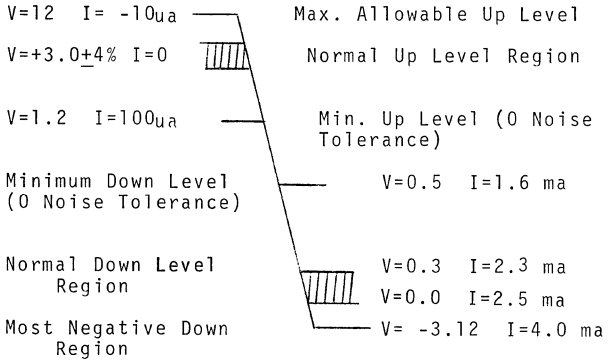




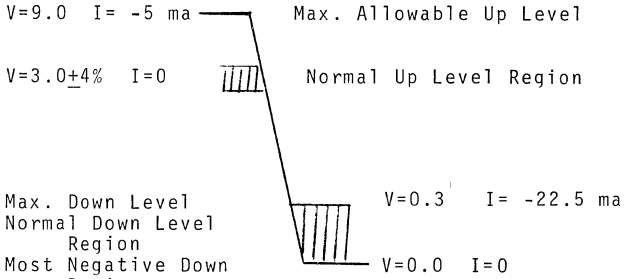
Circuit Description

The AI module consists of a diode positive AND circuit followed by a saturating inverter.

Input Requirements



Output Specifications



$$C \frac{dv}{dt} = 3.5 \text{ ma}$$

Delay Parameters

	Delay Used By SLDA	Delay Limits 8" Net BC	Delay Limits 8" Net WC	Delay Limits 48" Net BC	Delay Limits 48" Net WC
Output Rising	21	5	25	10	35
Output Falling	25	5	30	5	35

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Power Requirements

VOLTAGE	maximum Current (ma)	
	ON	OFF
+6	+02.50	+2.78
+3	+04.06	+0.00
-3	-01.16	-1.01
GND	-17.05	-0.00

Total Power Dissipation

Maximum (mw)	
ON	OFF
34.75	20.10

Noise Tolerance

1. Positive Noise
   Pulse width $\geq$ 20 ns
   Positive Noise tolerance $\geq$ 200 mv reference to 0.3v
   Positive Noise tolerance decreases 10 mv for each dotted collector

2. Negative Noise
   Pulse width $\geq$ 20 ns
   Negative Noise tolerance $\geq$ -1.7v reference to 2.88v

Application Notes

Wiring

a. The maximum net length at either input or output should not exceed six feet of line.

b. For a single line in a channel the input to an AI must not exceed three feet, if driven by an AI or AOI. It must not exceed two feet if driven by an API or one and a half feet if driven by a DCI. If there are two other lines in the channel switching simultaneously, the maximum length is eighteen inches.

DOT ORing Collectors

The number of dot ORed collectors is limited by the allowable noise tolerance reduction at the input of each of the dot ORed blocks.

The distance between dot ORed blocks is limited only when one of the dotted collectors must remain on when the other collectors are turned off.

The distance of AI loads to any one remaining "on" collector is limited to a maximum of 10" line.

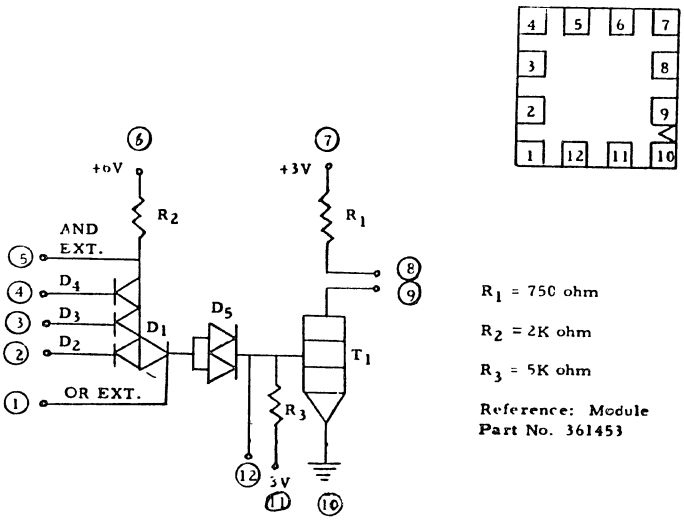
SPEC. PART NO. 890972 AND OR INVERT	LMH Cat.	0-2860 Subject	790 Suffix

IBM Location Manufacturing Specification

Referenced Circuit Flyers - TO3AC, TO3AD, TO3AE, T61AA, T61AB, TO3VA, TO3VB

EC Level-752349

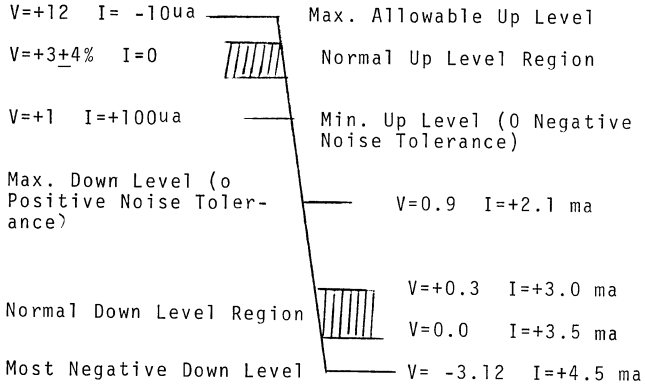
Circuit Schematic - AND OR INVERT



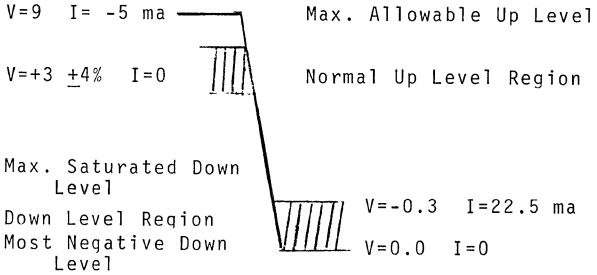
Circuit Description

The AOI module consists of a diode positive AND function and one diode for an OR function, followed by a saturating inverter.

Input Requirements



Output Specifications



$$C \frac{dv}{dt} = 3.5 \text{ ma}$$

Delay Parameters

	Delay Used By SLDA	Delay Limits 8" Net BC	8" Net WC	48" Net BC	48" Net WC
Output Rising	21	5	25	5	32
Output Falling	34	10	40	20	60

06-09 Primary Standards Manual	00-0- Other standards manuals in which this document may be filed.			
Applicability	ENDICOTT	ENDICOTT Responsibility	1-67 Date	1 of 2 Page

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Power Requirements

VOLTAGE (Volts)	Maximum Current (ma)	
	ON	OFF
+6M	+2.1	+2.8
+3	+4.1	+0.0
-3	-0.9	-0.7
GND	-25.0	0.0

Total Power Dissipation

Maximum (mw)	
ON	OFF
37.0	21.0

Noise Tolerance

1. Positive Noise Pulse widths $\geq$ 20 nsec.

The W.C. D.C. Noise Tolerande at the input.

	Noise Tolerance (MV)
1 way OR	610
2 way OR	570
3 way OR	540
4 way OR	520
5 way OR	510

All are referenced to 0.3v.

2. Negative Noise The W.C. D.C. noise tolerance at the input is $\geq$ 1.08v below the +2.88v for one way OR.

3. Decrease in positive noise tolerance is 10 mv for each dot-ORed collector.

Application Notes

Wiring

a. The maximum net length at either the input or the output should not exceed six feet of line.

b. With a single wire in a channel, the input to an AOI must not exceed five feet if driven by an AI or AOI. It must not exceed three feet if driven by an API or DCI. If there are two other lines switching simultaneously in the same channel, the maximum length is thirty inches.

AND Fan In Rules

a. Maximum of five AND diodes for W.C. delays specified. (W.D. "on" 39 nsec., W.C. "off" 28 nsec. at 25° C to 75° C.)

b. Maximum of 19 AND diodes may be switched simultaneously.

c. 64 maximum D.C. limit, where delays are not critical.

d. All extended AND diodes should be on the same small cards as the AOI module to minimize stray capacitance and difference in the junction temperatures between the translate and the extending AND diodes.

OR Fan In Rules

a. Maximum number of OR inputs is five.

b. All extended OR diodes should be on small car as the AOI module.

c. The W.C. Off delay increases approximately seven nsec. for each OR input greater than one.

SPEC. PART NO. 890985 Exclusive OR Latch XOR-L	LMH Cat.	0-2860 Subject	793 Suffix

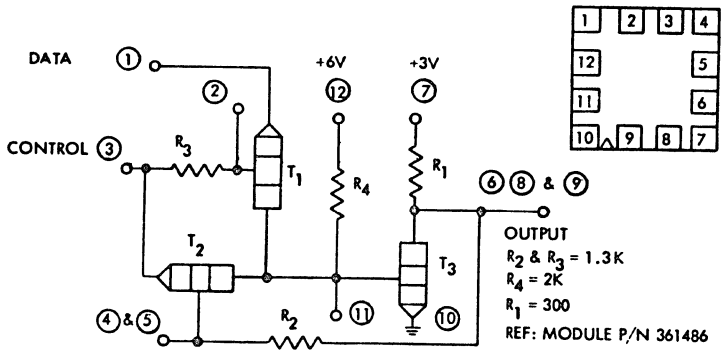
IBM

Location Manufacturing Specification

Referenced Circuit Flyers - T03AK

EC Level-752612

Circuit Schematic - Exclusive OR Latch XOR-L



Circuit Description

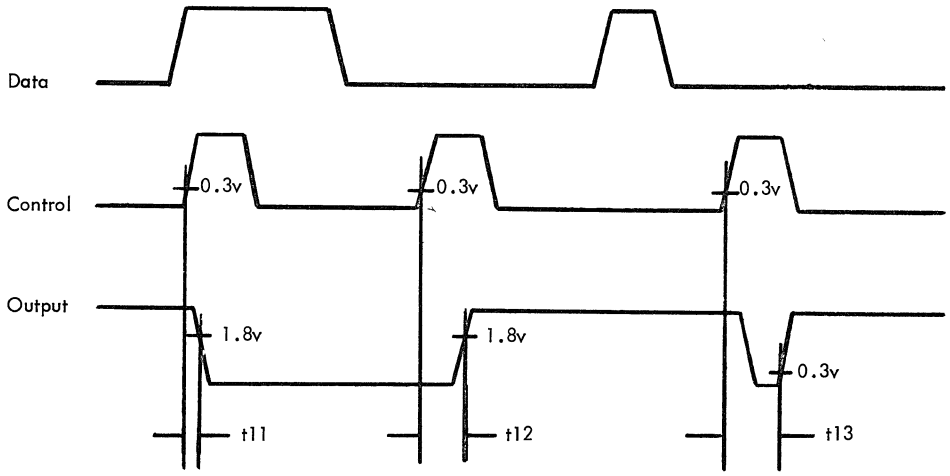
The XOR Latch has a single bistable output that can be changed by proper sequencing of the control and data inputs. The inputs can be used in either sequence (1) or (2).

Sequence Operation (1)

Control is normally down. The latch output will be set to the complement of the data input on the control rise.

a. Data line up. With the control rise the output will be set to (0) state. All further changes in the control line will not affect the state of the latch, if data line in unchanged.

b. Data Line down. With the control rise, the output will be set to the (1) state. All further changes in the control line will not affect the latch state, if data line in unchanged.



Worst Case Delays t_{11} = 20 ns max. t_{12} = 50 ns max. t_{13} = 50 ns max.

06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
Applicability	ENDICOTT	ENDICOTT Responsibility	1-67 Date	1 of 3 Page

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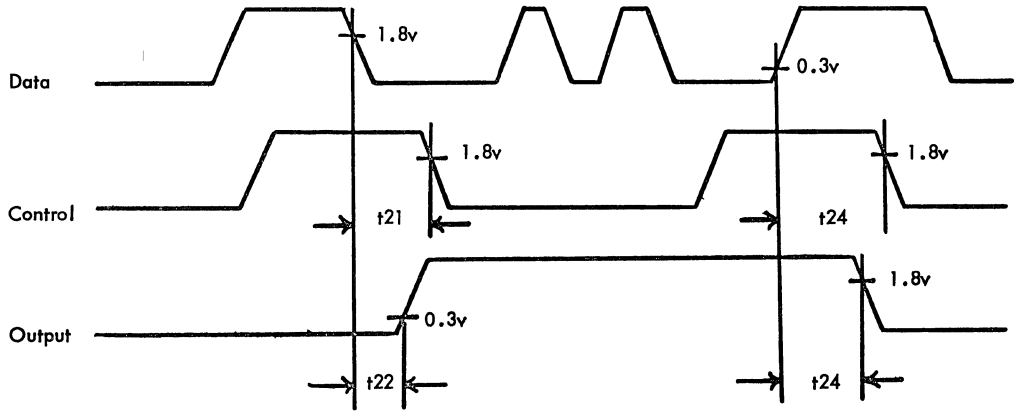
Sequence of Operation (2)

Control is normally up. The latch output will change with changes in the data line. Information is stored on the control fall. If the control line remains down after the control fall, changes in the data line will not affect the latch state.

a. Data line up. With the clock fall, the output will be held in (0) state.

b. Data line down. With the clock fall, the output will be held in (1) state.



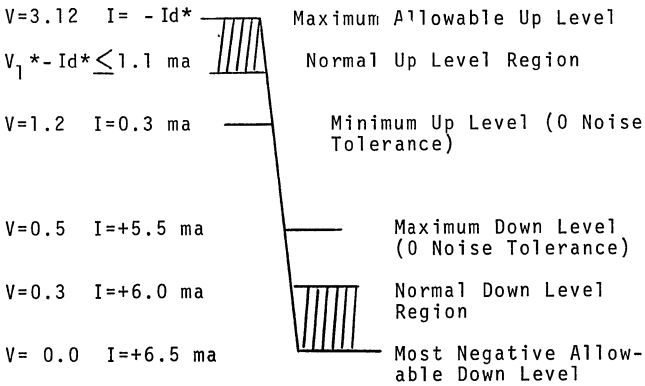
Worst Case Delays

* t_{21} = 50 ns min. t_{22} = 20 ns max. t_{23} = 40 ns min. t_{24} = 20 ns max.

* If HPD driver is used and $\leq$ 30 pf on the latch output t_{21} = 40 ns min.

Input Requirements

1. Voltage and Current Levels: DATA INPUT



*Note: Control Input Down.

I_d=0, V_1 defined by the remaining data inputs tied to this node and/or other loading connected to it.

$$I_d = (.7)\left[\frac{.085\,(P-1)\,R_d+2.6}{R_C[1.3+1.07(P-1)]+1.7}\right] \text{ ma} \leq 1.1 \text{ ma}$$

Where:

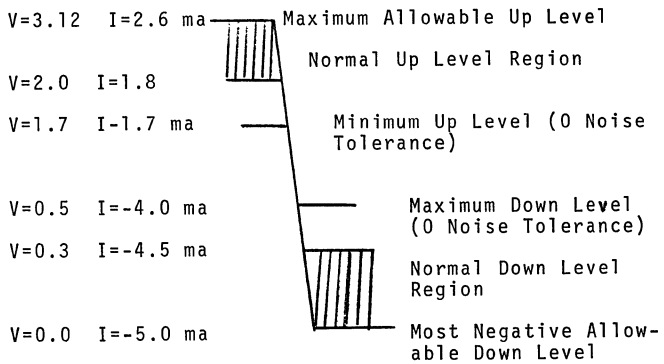
P = number of control inputs tied to a common node.

R_C = Resistance from the node to the +3v supply (in KΩ)

R_d = Resistance from the data node to the +3v

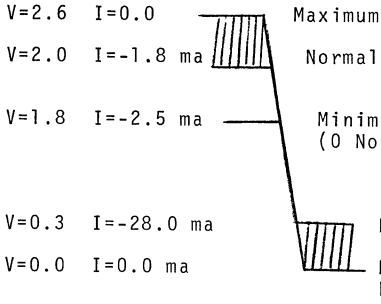
V_1 is defined by the other loading at this point including the values of I_d calculated for each Data input tied to this common node.

2. Voltage and Current Levels: CONTROL INPUT



Output Specification

Voltage and Current Levels (with collector resistor and feedback loop connected to the collector of the output transistor of the latch. These connections are not to be removed when using this module).



Delay Parameters included in Circuit Description

Power Requirements

VOLTAGE (Volts)	Maximum Current (ma)	
	ON	OFF
+6M	+02.8	+3.2
+3	+10.5	+3.9
GND	-39.0	0.0

Power Dissipation In MW)

Total Power dissipation

Maximum (MW)	
ON	OFF
66.0	-27.25

Input Noise Tolerance

Pulse Widths $\geq$ 20 nsec.

1. Data Input. Positive Noise Tolerance 200 mv referenced to 0.3v saturation level. Negative Noise Tolerance V_1 - 1.2v.
2. Control Input. Positive Noise Tolerance 200 mv referenced to 0.3v saturation level. Negative Noise Tolerance 300 mv referenced to 2.0v Up Level.

Output Noise Tolerance

Pulse Widths $\geq$ 20 ns.

1. Positive Noise $\geq$ 500 mv above 0.3v reference.
2. Negative Noise $\geq$ 200 mv below 2.0v reference.

Application Notes

Wiring Rules (Based on 30 ma switching in each active line)

A. Date Input

Maximum single line length = 18".
18" maximum for 1 adjacent line switching.
9" maximum for 2 adjacent line switching.
6" maximum line length without GND plane.

B. Control Input

Maximum single line length = 20"
20" maximum for 1 adjacent line switching.
9" maximum for 2 adjacent line switching.
6" maximum line length without GND plane.

C. Output

Restrictions due to loading
18" line, 12 ma current load maximum.
9" line, 23 ma current load maximum.
6" line no GND plane 12 ma current load maximum.

D. DOT-ORED Collectors

1. Dot-Oring of the outputs of two or more latches is not allowed.
2. When the latch output is Dot-Ored with the collectors of other circuits the collector resistors of the blocks to be dotted with the latch output, will not be used.
3. When collectors are dotted, the negative noise tolerance at the inputs of the dotted blocks decreases by 10 mv per dot-OR.
4. Care must be taken to insure that the output capacity of the latch output is $\leq$ 60 pf to guarantee latch operation.
5. The maximum distance of the source of load current from the remaining "on" collector when all other collectors are turned "off" is 10 inches.

IBM

Location Manufacturing Specification

INTRODUCTION

1.1 SCOPE. This specification describes the Manufacturing Project File and provides instructions for the preparation, maintenance and control of documentation required to implement the project file system. This document supplements and is in agreement with CMH 0-4010-001.

1.2 APPLICATION. This specification applies to the Endicott Components Division.

1.3 EXEMPTION. Programs involved in the design and manufacture of products under special government contracts are exempt from this specification.

1.4 SUPERSESSION. This specification supersedes LMH 0-4010-002 dated 11-67

DESCRIPTION

2. GENERAL

2.1 A Project File is a planning and control document used to record all aspects of a project from inception to completion. It shall be used for Technical communication, as a source document for technical investigations, to provide complete project history and as an aid toward reducing duplication of effort.

2.2 Project Files shall be maintained for each technical and operational project as deemed necessary by management. A Project File can be initiated by anyone whose project qualifies. All Project Files must be reviewed by the originator's manager.

2.2.1 A manager's decision to document an activity shall be determined by its significance. He should consider:

a. Technology
b. Management information
c. Impact on peripheral areas
d. Potential marketing effect
e. Budget, plan and cost estimate usage
f. Legal and patent implications
g. Financial significance
h. Cost reduction
i. New Product Release

3. PROJECT FILE SYSTEM

3.1 The Project File System consists of:

a. Authorized Documentation
b. Mandatory Distribution
c. Information Retrieval Capability

3.2 Authorized Documentation. Project Files shall be prepared using the following forms:

a. Index, Review and Transmittal (Form No. M08-0001-1)

b. Engineering-Management Abstract (Form No. M08-0009-0)

c. Multi-Purpose Sheet (Form No. M08-0002-1)

d. Summary Sheet (Form No. M08-0003-1)

e. Resource Plan (Form No. 924-5216-0)

3.2.1 Forms(a)(b)(c), and (d) are available from Mechanicsburg. Form (e) is a new one, available from stationery stores.

3.2.2 These forms comprise the project file "package", (see Figures 1 through 5). Each form contains blocks for project and file identification. Other blocks, (e.g. "Responsibility", "Project Status") are provided for information pertinent to the function of an individual form.

3.2.3 The type of information which must be recorded is defined by the file sections of the "Section Index" of the Index, Review and Transmittal. This index is the key to information required on the other forms.

3.2.4 General applications of forms

Index, Review and Transmittal (Fig. 2)	Cover sheet of file-must accompany individually distributed sections-used to update retrieval system.
Engineering-Management Abstract (Fig. 1)	Files Section 1, the only narrative section of the project file which is entered in the ITIRC (IBM Technical Information Retrieval Center.)
Multi-Purpose Sheet (Fig. 4)	Used for all sections of the file for which a special form does not exist.
Summary Sheet(Fig. 3)	Used for file sections 3 & 4. (Optional use for file section 12, as described in paragraph 3.6.10).
Resource Plan (Fig. 5)	Used for Section 5.
Distribution Sheet (Fig. 8)	Used for Section 6.

3.2.5 Project files shall be prepared for parent projects and sub-projects.

a. Sub-projects are related to the parent project by product type or technology and the objectives of both parent and sub-project will be complementary or supplementary.

4. FILLING OUT FORMS

4.1 Considerations applicable to all forms

4.1.1 Project Name. Enter a short, descriptive title. The wording must be the same on each form.

4.1.2 Origination Date. The date entered on the Index, Review and Transmittal form shall be the date of project origination and shall remain unchanged. The date entered on the other four forms shall be the date the individual sections are added to the file and will change as the sections are updated. A completed Project Identification block should appear as:

PROJECT IDENTIFICATION

PROJECT NAME	ORIGINATION DATE MO. DAY YEAR
Electronic Test Equipment for 2400 Series Tape Drives	06 23 66

4.1.3 File Identification. This block shall contain a two character alpha code for the division, the applicable alpha code for the location, a three digit number for the department, a four digit file number, and a two digit suffix. For example, a project being conducted in he Systems Manufacturing Division at Poughkeepsie, in Department 379, under file number 2400, and which is the parent project for several sub-projects, would be identified as follows:

FILE IDENTIFICATION

DIVISION	PLANT ALPHA CODE	DEPT.	FILE NUMBER	SUFFIX
SM	POK	379	2400	00

The originator should leave the file number blocks blank. This will be assigned by Dept. 204. The suffix is used when a project is divided into a parent project and several sub-projects, all charging the same number, the parent file shall be suffixed 00 and the sub-projects shall be suffixed 01 through 99.

a. Division. The following codes shall be used:

Division	Code
Components Division	CD
Federal Systems	FS
Information Records	IR
Office Products	OP
Systems Manufacturing	SM
World Trade Corporation	WT

b. Plant Alpha Code for Endicott is E N D.

c. Number of the department responsible for the project.

4.1.4 All sections shall use a decimal numbering system, like the one used in this specification, when subdivision becomes necessary.

4.2 Considerations Applicable to Specific Forms:

4.2.1 Approvals. This block shall contain the typewritten names of the engineer and/or the manager responsible for the project, their initials (signifying approval) and the dates. Approvals are required on all forms except the Multi-Purpose and Distribution sheets.

Example:

APPROVALS (BOTH REQUIRED)

ENGINEERING (TYPE NAME)	INITIALS	DATE
Jonathan Doe	JD	12-24-66
MANAGEMENT (TYPE NAME)	**INITIALS**	**DATE**
John Smith	JS	12/24/66

4.2.2 Responsibility. This block is found only on the Index, Review and Transmittal form. A reporting function is one which reports directly to the assistant general manager of a plant.

Example:

RESPONSIBILITY

REPORTING FUNCTION (EXAMPLE: MFG. ENG., IND ENG., QUAL. ENG., ETC.)
Manufacturing Engineering

4.2.3 File Type. This block appears only on the Index, Review and Transmittal form. Under certain circumstances, files will be prepared which contain management information only. An example of this type of file would be one which contains summaries of funding, scheduling and manpower; and excludes or minimizes engineering information. The appropriate box in the File Type block shall be checked.

4.2.4 Project Status. This block appears only on the Index, Review and Transmittal form. A completed block (illustrated below) should indicate the status of a project.

PROJECT STATUS (CHECK ONE)

☒ ACTIVE	LEVEL 03	☐ TERMINATED
☐ SUSPENDED	DATE	DATE

a. "Levels" of Project Files shall be designated numerically with the initial file as "Level 01". Thereafter, the updating of each file shall follow in numerical order: 02, 03, 04, etc. Existing files shall have the first update labeled as "Level 02".

b. When "Suspended" is checked the reason for, and the anticipated duration of suspension shall be entered in the "Remarks" block.

4.2.5 Remarks. This block appears only on the Index, Review and Transmittal form. It shall be used to provide any amplifying or limiting comments. It is especially of value for supplying information to the IBM Technical Information Retrieval Center (ITIRC). Any information entered in this block will be recorded on ITIRC's retrieval tapes.

4.2.6 Section. The section blocks appear on the Multi-Purpose Sheet and the Summary Sheet. Because the Multi-Purpose Sheet has wide application, it requires the section number and the section title be entered by the project file writer. For example, the number and name for Section 2 should appear as:

SECTION

NUMBER	NAME
2	Objectives

The section block which appears on the Summary Sheet contains the names and numbers of the three sections for which the form is used. Process Engineering will use this form for Section 3 only. Check the appropriate box. For example, a block completed for Section 3 should appear as:

SECTION (CHECK ONE)

☑ 3 SCHFDULE OF EVENTS (LINE-THRU PERIOD) ☐ 4 MANPOWER (ENTER MAN MONTHS) ☐ 5 COST (ENTER DOLLARS)

The parenthesized information which appears to the right of section title indicates the units or manner in which information should be entered in the grid area of the form. The method of entry is shown in Figure 6.

5. DESCRIPTION OF PROJECT FILE SECTIONS

5.1 Engineering-Management Abstract. A narrative section prepared on the form of the same name, this should briefly describe the purpose and broad objectives of the project including the reason for the file (e.g., Technology, Management Information, Cost Reduction, New Product Release, Budget Information, etc.). Any abbreviations or acronyms used must be defined. This abstract should also include the machine type and project number codes applicable to the project.

5.1.1 Within the body of the abstract or in the key word descriptors, the activity area performing the project shall be indicated. These areas are of the following: Manufacturing Research, Advanced Manufacturing Engineering, Industrial Engineering, Quality, Quality Engineering, Test Equipment Engineering, etc. The use of these descriptors will provide the Information Retrieval System with a facility for retrieving projects on an activity-related basis. Include as many key-word descriptors as possible to adequately describe the project file.

5.1.2 The Engineering-Management Abstract and the Index, Review and Transmittal forms are the only project file elements that enter the retrieval system. Therefore, it is very important that the abstract be prepared carefully. The abstract should contain salient information to help the reader gain insight into the project.

5.2 Objectives (File Section 2). Uses Multi-Purpose Sheet. The purpose, briefly described in the previous section, shall be expanded here. Include such items as:

a. Improve yield
b. Increase production efficiency
c. Reduction of scrap
d. Improve quality
e. Reduce labor or parts cost
f. More thorough testing
g. Improve reaction to changes
h. Improve process control
i. Fill information gap, etc.

The description should be specific, If, for example, the project involves building a machine with a definite capacity to product a given number of parts, say so.

5.3 Schedule of Events (File Section 3). Prepared on a Summary Sheet as illustrated by Figure 6, this section should provide a visual picture of the major events in the project and their inter-relationships. The event listed should be the major milestones only. It is not necessary to include a complete breakdown by every subsidiary task in the project.

5.4 Manpower Requirements (File Section 4). Formerly prepared on the Summary Sheet, this section is no longer required since the information is now included in the Resource Plan.

5.5 Cost (File Section 5). Prepared on the Resource Plan Form shown in Figure 5. Use a separate form for each year.

5.5.1 Fill out the project file heading information as previously described.

5.5.2 Fill out the project description information as follows:

Dept. - Engineering department
MT - Machine type code
Proj. - Project number

Project Description - A brief but accurate description of the project to be described below. Use abbreviations wherever possible.

Priority - This is a single digit, selected from the list below, which indicates the urgency of the project.

1. Essential - Necessary to meet production schedules or unabatable requirements.
2. Extremely desirable - alternatives are impractical and task must be accomplished.
3. Quite desirable - Involves a considerable increase in efficiency of an existing operation.
4. Desirable - slight increase in efficiency with possible benefit in future.
5. Vaguely desirable - slight increase in efficiency with no other benefits.

Project File - This includes the project file number (first four digits) and suffix number (last two digits).

BCC - Benefitting Process Center - If more than one Process Center benefits, use 111. If no existing Process Center benefits, use 777.

Yr. - The last two digits of the year being planned for.
Start - The month and year the project is to start.
Stop - The month and year the project will be completed.

NOTE
Start and stop dates should be carried over from first year of the project if it runs more than one year.

Carryover- Indicate the total 4th and n-4th carryover dollars included in the tasks listed below. Carryover dollars are those dollars that were committed or planned for, but not spent, in a previous year that will be spent.

5.5.3 Fill out the task description information as follows:

Task Description - A brief but accurate description of the task to be performed. This description must be limited to one (1) line; therefore, abbreviate as much as possible.

Quarter - The dollars required for the task must be entered by quarter in the quarters they will be spent.

Effort - The effort code describes the effort planned. Those to be used are listed at the bottom of the form.

Act - Activity code defines the type of activity. A list of these codes and their descriptions will be provided by the Functions Involved.

Build - Build code defines the type of build; see the listing at the bottom of the form.

Workload - Workload code defines types of build effort and identifies brass tag equipment; see the listing at the bottom of the form.

Item - Sequential numbering of tasks (01-99). Required for computer operations.

Yr - The last two digits of the year being planned, must be the same as the year in the project description.

5.6 Distribution (File Section 6). This is prepared on the Distribution form. Details are covered in Section 7 of this specification.

5.7 Project Status (File Section 7). This section is required in all Project Files and provides a "running account" of the project in relation to the scheduled objectives. When changes to the schedules, objectives or estimates are required, the reason for the alterations must be included here.

5.7.1 If a change results from a technical problem, a general description of the problem shall be given as the cause. Do not provide a detailed description here because File Section 9 is used for the details of the technical problems.

NOTE
File Sections 8-15 are optional but should be used when the project generates information which must be included.

5.8 Machine Design Objectives or Specifications (File Section 8). The design objectives and specifications for devices which will be produced as a result of this project should be referenced in this section. These specifications shall be prepared according to IBM Division Standard 0-0-2507-0 and/or P/T Procedure 104.

5.9 Key Technical Problems (File Section 9). Detailed descriptions of technical problems, their causes and possible solutions shall be included in this section of the file. When a solution is reached, the reasons for selecting the specific solution shall be noted.

NOTE
This file section does not replace the Engineer's Notebook. All significant technical information should be recorded in the notebook and referenced.

5.10 Complementary or Peripheral Projects (File Section 10). The effect that the subject has on other projects and the effects that other projects may have on the subject project shall be described in this section.

5.11 Reference Material (File Section 11). Related information such as technical reports, proposals, machine descriptions and Engineering Notebooks shall be listed and identified in this section. The listing shall include the title, author, source and serial number of each reference document. (DO NOT INCLUDE THE ACTUAL DOCUMENTS.)

NOTE
To avoid unnecessary bulk, the originator shall review and edit his material and refer to only that information which is pertinent to the purpose and objectives of the project. All other material should be retained by the originator.

5.12 Economic Evaluation (File Section 12). If alternative approaches to a project are developed, the relative economic merits of the alternatives shall be discussed.

5.13 Production Schedule (File Section 13). The production schedule shall be referred to in this section. Production schedule information may be transcribed from the original schedule to a Summary Sheet, but only if it is necessary.

5.14 Patent Status (File Section 14). If any Invention Disclosures have been filed, or if action has been started to file for a patent, this section shall include:

a. The name of the invention
b. Date disclosure was filed
c. Disposition
d. Name of inventor(s)

NOTE
Include in separate paragraphs, IBM inventions being used in the project that were not invented by members of the project team and inventions being used but not invented by IBM personnel.

5.15 Sub Project Status (File Section 15). If the completion of a project depends upon related sub-projects, this section shall contain a brief statement of the status of the sub-projects. For example:

Project 4567-89, Wet Process Conveyor Equipment;
On Schedule

Project 6543-21, Test Equipment for SLT Cards;
Two Weeks behind schedule

Project 4987-65, SLT Card Etching Equipment,
Project Suspended 012266

5.16 Additional File Sections. If a situation arises in which information cannot be logically included in the previously titled sections (a PERT network, for example) additional sections may be included. Generally, the Multi-Purpose Sheet is recommended for this purpose.

5.17 Sections 1 through 15 shall not be re-titled, nor shall they contain information irrelevant to a section title. Added sections shall start with number 16.

6. FILE MAINTENANCE

6.1 When adding or updating a section, prepare a completley new Index, Review and Transmittal sheet. All information entered on the new sheet shall be identical with the previous one except:

6.1.1 Section Origination Date - will be a new entry if a new section is being added to the file.

6.1.2 Updated Date - a new entry for each section being updated.

6.1.3 Asterisk - a new entry for each section being updated and which is an attachment to the new transmittal sheet. Do not enter asterisks for sections not included in the current updating.

6.2 When updating is required on the Engineering Management Abstract, prepare a new form and use the current date as the origination date.

6.3 When additions are made to sections that are written on the Multi-Purpose Sheet, they are to be entered on a new sheet and the Origination Date shall be the date of inclusion.

6.4 If the original information entered on the Summary Sheet changes, the existing sheet shall remain in the Library File and the updated information shall be entered on a new copy of this form. The origination date shall be the current date.

6.5 Information shall not be deleted from the library copy of any project file.

6.6 Project files should be updated as required by changing ground rules and/or technical progress, but the maximum allowable time between updates is three months. Even if no change to the file is necessary at the end of this time, the status should be noted as unchanged via File Section 7 (5.7).

6.7 Be sure to include any changes in the distribution in the update.

6.8 When an update includes changes to any narrative file section, be sure to reference the associated paragraph or item number under Remarks.

6.9 When transferring the responsibility of a project file from one department to another:

6.9.1 Notify the proper Financial personnel that a project will be assumed by another department.

6.9.2 The status of the project file shall remain active.

6.9.3 Indicate in Section 7, Project Status section, that the responsibility is being transferred, the name of the individual who will be assuming the responsibility, and the department number.

6.9.4 Update the Distribution List, Section 6, by adding the name of the individual who will be responsible for future updating of the project file.

6.10 When changing the name of a project file: To avoid confusion and to ensure that all records are current, it is important that Department 204 be notified when a change is made in the name of a project. This can be accomplished by completing an Index, Review and Transmittal form. Under "Remarks", indicate the new name of the project file.

7. DISTRIBUTION

7.1 Input to the system is prepared by the individual responsible for the project. All input documents shall be approved as specified on the forms.

7.2 All narrative sections and transmittal sheets shall be typewritten on the prescribed forms. Other sections may be handwritten, but must be clear and legible and written in black lettering on white paper to ensure good reproduction.

7.3 Project files may be distributed at the abstract level, the detailed file level, or as selected sections and may be entered in a Corporate or Local distribution as desired by the Manager responsible for the project. The only difference between these distributions, as shown in Fig. 7, is that no material is sent to ITIRC or Corporate Technical Services when the Local Distribution block on the Distribution Sheet is checked.

7.3.1 Abstract Level - requires the Index, Review and Transmittal and the Engineering-Management Abstract. When initially completed, or whenever either is changed, these are sent to the IBM Technical Information Retrieval Center (ITIRC), Department 777, Armonk, New York, Attention: Manufacturing Project Files; thus, although the abstract is part of the detailed project file, it has an an additional usage. It enters and maintains the status of the project in the Retrieval Systems's data bank.

7.3.2 Detail Level. Whenever a Project File is changed, or updated, the completed forms, together with a new Index, Review and Transmittal Sheet, are forwarded to Department 204 who will make distribution. Figure 7 shows the processing flow for the distributions and for information retrieval.

7.3.3 Selected sections. Indicate in the Distribution (Section 6) of the Project File, which sections are to be forwarded to the addressee (for example, Functional Staff-Section 5). When preparing the distribution list, the originator shall clearly specify the name, department, building, floor and any other information necessary to expedite distribution.

7.3.4 In addition to normal local distribution, the Project File Originator should include his copy requirements on the distribution list. The Project File Center in Department 204 is the only area authorized to make copies of project files.

NOTE

Because of the sensitive nature of the information recorded in the project file, classification of the document is IBM CONFIDENTIAL. Therefore, the manager of those who request project files information has the responsibility of providing assurance that the requestor has the "Need-To-Know".

7.4 At Endicott, Department 204 has been designated for project file coordination. All input shall be received by this area and the originals (typewritten vellum masters) of project files shall be retained by this area. The project file coordinator shall maintain the microfilm (aperture card) library. Local distribution shall also be the responsibility of the project file coordinator.

NOTE

Microfilm (aperture card) output to manufacturing locations will occur as soon as possible after the initial input or updating of files.

7.5 The Process Engineering and Test Engineering Manufacturing Project File Center is located in the CD Technical Library (Cafeteria Building). It will act as a clearing house for all inquiries concerning project files. The Center will store, distribute and maintain all Process Engineering and Test Engineering project files. It will also have an up-to-date aperture card file on all project files in the Corporate System. Abstract listings will be made available by the Center. All inquiries concerning the processing of local project files or the acquisitions of local or other IBM project file data should be directed to the librarian.

8. INFORMATION RETRIEVAL

8.1 The retrieval of project file information is also divided into two parts: The "Abstract Level" and the "Detail Level".

8.1.1 Abstract Level. This level is received from ITIRC and contains the abstract and status of the project and the date of the latest revision to the project file sections. To initiate a request for project file information, an individual must submit a Data Sheet* to ITIRC. The Data Sheet, when completed, will indicate requestor's "field-of-interest profile". A request from an individual to search the total project file data bank will produce a listing of project files, at the abstract level, from the Research, Development and Manufacturing organizations. This listing will match the individual's "field-of-interest profile". If an individual wishes to be informed continually of new project files or when additions have been made to existing manufacturing project files in his field of interest, he will submit a profile of ITIRC's CIS (Current Information Selection) program.

*Blank forms are available from the CD Technical Library, Dept. 204.

NOTE
Since ITIRC is the designated area to receive technical information on all types of projects throughout the IBM Corporation, Endicott management recommends that each engineer take advantage of this service by completing and submitting CIS Data Sheets appropriate to his field-of-interest. When preparing a Data Sheet for participation in the Current Information Selection (CIS) program, write in red pencil across the top of the sheet, "Manufacturing Project Files". This will enable ITIRC to quickly identify that project file abstract information being requested.

8.1.2 Detail Level. This level consists of microfilm files (aperture cards) of manufacturing project files. The index to the detail level file for an individual's field-of-interest will be the project file "abstract level" listing, which is obtained from ITIRC, as described above. The Project File Center will keep an up-to-date aperture card file containing detail information on each project file submitted to Corporate Technical Services from anywhere in IBM. This file is available for your review at any time.

8.2 Local abstract listings will be generated by CD Technical Library. This listing will be sent to all Project Managers in the Process Engineering and Test Engineering functions who should review this listing for possible projects of interest in Endicott. Additional information can be secured from the Project File Center.

8.3 As stated above, all project files shall have a minimum classification of IBM CONFIDENTIAL. Corporate Instruction C1-101, dated 12/1/65, provides information governing the control and classification of documents.

IBM

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(FILE SECTION 1)

Manufacturing Project File
Engineering Management Abstract

PROJECT IDENTIFICATION

PROJECT NAME

ORIGINATION DATE MO DAY YEAR

FILE IDENTIFICATION

DIVISION	PLANT ALPHA CODE	DEPT	FILE NUMBER	SUFFIX

ABSTRACT IN LESS THAN 250 WORDS.

KEYWORD DESCRIPTORS (INCLUDE AS FIRST DESCRIPTOR THE NAME OF REPORTING FUNCTION. EXAMPLE, IND. ENG , MFG. ENG , QUAL. ENG.)

ITEM	CAPITAL EXPENDITURES	+ EXPENSE EXPENDITURE (INCL LABOR & BURDEN)	= TOTAL FOR PERIOD	MANPOWER (MAN/MONTHS)
CURRENT CALENDAR YEAR ESTIMATES				
NEXT CALENDAR YEAR ESTIMATES				
REMAINING PERIOD ESTIMATES				
TOTALS FOR LIFE OF PROJECT	$	$	$	

PROJECT START DATE MO. DAY YR.

ESTIMATED COMPLETION DATE MO DAY YR.

APPROVALS (ONLY ONE REQUIRED)

ENGINEERING (TYPE NAME)	INITIALS	DATE
MANAGEMENT (TYPE NAME)	INITIALS	DATE

M08-0009-0

FIGURE 1

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Manufacturing Project File
Project Index, Review and Transmittal

PROJECT IDENTIFICATION

PROJECT NAME

ORIGINATION DATE MO DAY YEAR

FILE IDENTIFICATION

DIVISION	PLANT ALPHA CODE	DEPT.	FILE NUMBER	SUFFIX

RESPONSIBILITY

REPORTING FUNCTION (EXAMPLE MFG ENG, IND ENG, QUAL ENG, ETC)

FILE TYPE (CHECK ONE)

☐ MANAGEMENT ☐ ENGINEERING

INDEX, REVIEW and TRANSMITTAL

SECTION INDEX	SECTION ORIGINATION DATE	UPDATED	ASTERISK (*) ATTACHMENTS
1 ENGINEERING MANAGEMENT ABSTRACT			
2 OBJECTIVES			
3 SCHEDULE OF EVENTS			
4 MANPOWER REQUIREMENTS			
5 COST			
6 DISTRIBUTION			
OPTIONAL—USE THE FOLLOWING SECTIONS ONLY AS REQUIRED			
7 PROJECT STATUS			
8 MACHINE DESIGN OBJECTIVES OR SPECIFICATIONS			
9 KEY TECHNICAL PROBLEMS			
10 COMPLEMENTARY OR PERIPHERAL PROJECTS			
11 REFERENCE MATERIAL			
12 ECONOMIC EVALUATION			
13 PRODUCTION SCHEDULE			
14 PATENT STATUS			
15 SUB PROJECT STATUS REPORTS			
ADDITIONAL SECTIONS—ADD AS REQUIRED. NUMBER SEQUENTIALLY STARTING WITH SECTION 16			

REMARKS

PROJECT STATUS (CHECK ONE)

☐ ACTIVE LEVEL ___ ___ ☐ TERMINATED

☐ SUSPENDED DATE DATE

APPROVALS (BOTH REQUIRED)

ENGINEERING (TYPE NAME)	INITIALS	DATE
MANAGEMENT (TYPE NAME)	INITIALS	DATE

M08-0001-1

FIGURE 2

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(USE FOR SECTIONS 3 THROUGH 5)

Manufacturing Project File Summary Sheet

SHEET _____ OF _____

PROJECT IDENTIFICATION *FILE IDENTIFICATION*

PROJECT NAME	ORIGINATION DATE MO. DAY YEAR	DIVISION	PLANT ALPHA CODE	DEPT.	FILE NUMBER	SUFFIX

SECTION (CHECK ONE)

☐ 3. SCHEDULE OF EVENTS (LINE-THRU PERIOD) ☐ 4. MANPOWER (ENTER MAN MONTHS) ☐ 5. COST (ENTER DOLLARS)

ENTER NAMES OF EVENTS, MANPOWER SKILLS, OR COST ITEMS, BELOW		YEAR. QUARTERS 1	2	3	4	YEARLY TOTALS BY CATEGORY	YEAR QUARTERS 1	2	3	4	YEARLY TOTALS BY CATEGORY
	EST.										
	ACT.										
	EST										
	ACT.										
	EST.										
	ACT.										
	EST.										
	ACT.										
	EST.										
	ACT.										
	EST.										
	ACT.										
	EST.										
	ACT.										
	EST.										
	ACT.										
TOTALS FOR PERIOD	EST.										
	ACT.										

CONCURRENCE OF SUPPORTING AREAS (AS REQUIRED LOCALLY)						*APPROVALS (ONLY ONE REQUIRED)*		
INITIALS	DATE	INITIALS	DATE	INITIALS	DATE	ENGINEERING (TYPE NAME)	INITIALS	DATE
INITIALS	DATE	INITIALS	DATE	INITIALS	DATE	MANAGEMENT (TYPE NAME)	INITIALS	DATE

M08-0003-2

FIGURE 3

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(USE FOR SECTIONS 2, 6, 7 AND SUBSEQUENT SECTIONS)

Manufacturing Project File
Multi Purpose Sheet

SHEET _____ OF _____

PROJECT IDENTIFICATION | *FILE IDENTIFICATION*

PROJECT NAME	ORIGINATION DATE MO DAY YEAR	DIVISION	PLANT ALPHA CODE	DEPT	FILE NUMBER	SUFFIX

SECTION

NUMBER	NAME

ENTER NARRATIVE OR TABULAR INFORMATION HERE

M08 0002 1

FIGURE 4

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Manufacturing Project File
Resource Plan

924-5216-0

Project Name	Date-Month-Day-Year	Division	Plant Alpha Code	Dept.	File Number	Suffix

Dept. (1-3)	MT (4-5)	Proj (6-8)	Not Used (9-11)	Project Description (12-47)	PE	Proj. File No. & Suffix (49-54)	BCC (55-57)	Yr. (58-59)	Start Mo (60-63) Yr	Stop Mo (64-67) Yr	Carryover 4th (68-73)	Non 4th (74-79)	1

Duplicate on Detail	Effort	Activity	Build	Workload	Item	Task Description (16-57)	Year	Quarter 1 (60-64)	2 (65-69)	3 (70-74)	4 (75-79)	2

1 2 3 4 5 6 7 8 | 9 10 11 | 12 | 13 | 14 15 | 16 ... 57 | 58 59 | 60 ... 64 | 65 ... 69 | 70 ... 74 | 75 ... 79 | 80

Effort: 2=Eng. Effort, 4=Design, 5=Build, 7=L-Orders

Build Code: 0=4th Bld, 1=Month Bld, 2=Capital Bld

Workload Code: 0=PE type work, 1=Other IBM function type work, 2=Commercially purchased items-comp. and parts, 3=DT equip.-general, 4=DT equip.-mech. test & inspection, 5=DT equip.-elec. test & inspection

Approvals	Date
Engineer	
Management	

FIGURE 5

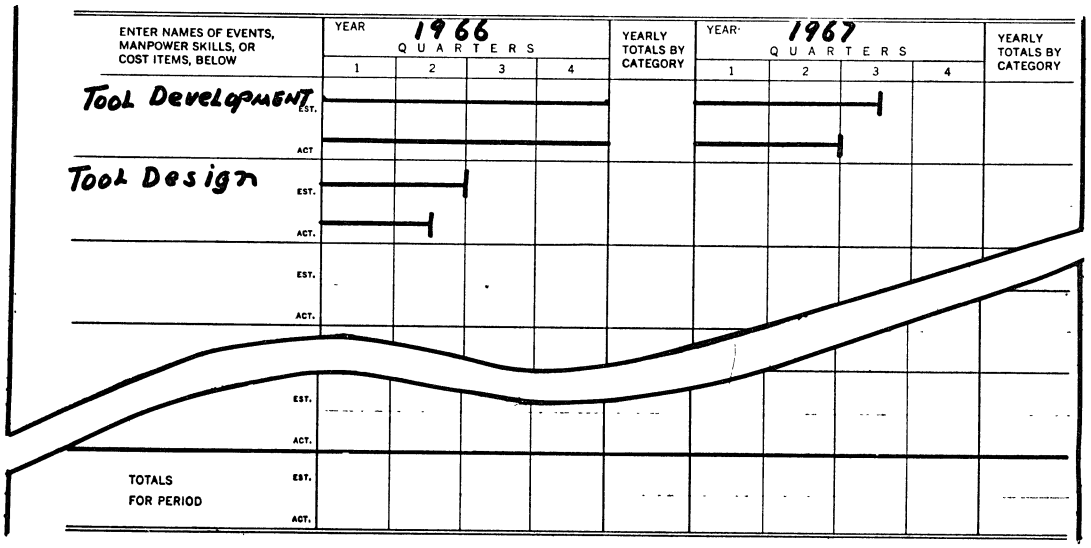

FIGURE 6

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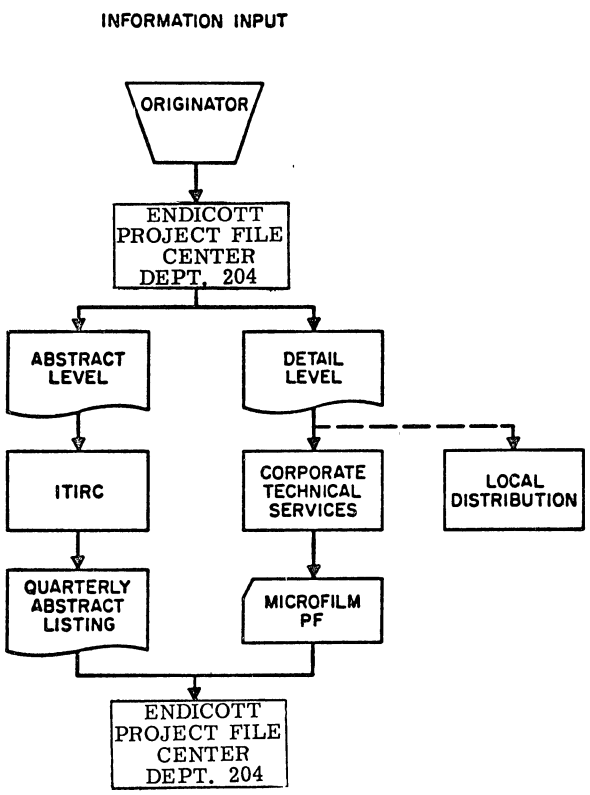

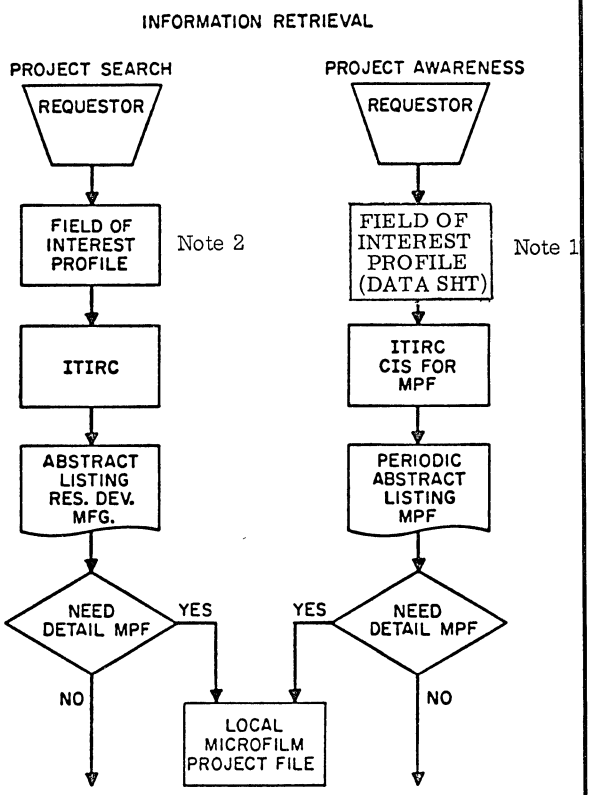

ITIRC - IBM Technical Information Retrieval Center
CIS - Current Information Selection Program for Manufacturing Project Files
MPF - Manufacturing Project Files

NOTE 1 - A data sheet must be submitted before requests for project searches will be honored by ITIRC.
NOTE 2 - Use information retrieval request #808-0100

FIGURE 7

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(USE FOR SECTIONS 2, 6, 7 AND SUBSEQUENT SECTIONS)

Manufacturing Project File
Multi Purpose Sheet

SHEET _____ OF _____

PROJECT IDENTIFICATION

PROJECT NAME

ORIGINATION DATE MO DAY YEAR

FILE IDENTIFICATION

DIVISION	PLANT ALPHA CODE	DEPT	FILE NUMBER	SUFFIX

SECTION NUMBER

NAME

FORM 924-5383-0

Type of File Distribution: Corporate ☐ Local Only ☐

Name	Dept.	Location	Section - Check (x) Applicable																		
			All	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			

FIGURE 8

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