IBM Standards Publication

PRINTED IN USA

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SLT DESIGNER'S HANDBOOK BOOK 06-09

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SLT DESIGNER'S HANDBOOK BOOK 06-09

IBM **Standards Publication**

INTRODUCTION

1.1 SCOPE. This manual is intended as a guide for equipment engineers and designers who design within the SLT (Solid Logic Technology) discipline. It includes data recommended or required for the design and build of equipment utilizing SLT.

This new circuit technology and hardware has necessitated the formation of a manual that will satisfy the requirements of equipment engineers.

Circuit descriptions are limited to the 30 and 700 nano-second family with some references to the 5 ns family. Hardware requirements peculiar to Equipment Engineering are discussed in the manual. Special forms required for design automation services are also included.

1.2 OBJECTIVE. This manual seeks to achieve a common understanding of the use of SLT concepts as they apply to Equipment Engineering functions. This common understanding will accomplish standardization where it is most desirable and practical.

1.3 AUTHORIZATION. The SLT designer's documents contained in this manual were approved by the task group assigned and authorized by a document of understanding on file in the Manufacturing Standards Department.

1.4 DEVIATION. The deviations from the requirements of the various documents within this volume are stated on each document.

1.5 PUBLICATION. Additional documents pertinent to Equipment Engineering will be published and distributed to 06-09 manual holders.

1.5.1 Manuals. This manual is issued and controlled by the Manufacturing Standards Department, Endicott.

1.5.2 Documents. Individual documents contained within this manual shall be developed by the organization most qualified in the subject or operation. Proposed new revisions documents shall be submitted to the Manufacturing Standards Department for authorization and inclusion in this manual. Documents are intended for Equipment Engineering use.

1.6 DEFINITION. Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Reserarch and/or their equivalents throughout the Manufacturing facilities.

2. DOCUMENTS

2.1 Classifications:

a. Standard. A description of any component, process or operation which has been identified as being of such significance to the company or a segment thereof from the standpoint of cost operations, maintainability, compatability, and/or safety that it should be implemented uniformly in its products or operations. The requirements section of a standard is a statement of the end result which must be achieved in order to conform to that standard.

b. Specification. A description of the physical, functional or other characteristics of parts, materials, functions, processes and/or procedures.

c. Practice. Procedures, actions, or design philosphies, which have been identified as being of overall value to the IBM Company or a segment thereof.

d. Techincal Bulletin. Bulletins contain Technical or procedural information that is released for "information purposes only" They are released to provide rapid dissemination of information. Each bulletin shall have a termination (void) date after which the document shall be withdrawn.

2.2 Applicability. This designation shall be based on the scope of authority of the document.

a. Corporate. Established by the concurrence of all divisions and subsidiaries.

b. Interdivisional. Established by the concurrence of two or more divisions.

c. Divisional. Established as applicable within one division or subsidiary.

d. Location. Established as applicable to an individual facility.

2.3 The combined classification and applicability will result in the following document categories (M designates Manufacturing):

Corporate	(C)	CMS	CMP	CMH	TMB
Interdivisional	(I)	IMS	IMP	IMH	TMB
Division	(D)	DMS	DMP	DMH	TMB
Location	(L)	LMS	LMP	LMH	TMB

3. DEVIATION PROCEDURE

3.1 Authorization required to deviate from a standard document must be obtained through the local standards function and shall be stated on the document.

a. Corporate Standards. Deviations must be requested by division or subsidiary President or General Manager an approved by the group Director of Standards or an authority designated by him.

b. Interdivisional Standards. Deviations require approval in accordance with local procedures, and the concurrence of the Division Director of Standards of each division or subsidiary committed to the standard.

c. Division and Location Standards. Deviations shall be in accordance with procedures of the division or location involved.

d. Specifications. Deviations shall be controlled by the procedure applicable to the document in which the specification is referenced.

e. Practice. Implementation of a practice is expected but does not require the formal control and deviation procedure of a standard.

4. FORMAT

4.1 Document format shall be the responsibility of Manufacturing Standards personnel and shall conform to Corporate Standards Instruction No. 10, dated November 5, 1963.

4.2 Document identification shall be by category, subject and suffix number.

a. Category. See Paragraph 2.3.

b. Subject. All standards documents are classified by subject matter in the IBM Data Classification System (DCS). See Corporate Practice 0-0106-0.

c. Suffix number. Identifies supplemental publications; major publications usually have a zero suffix.

Example: Case Hardened Sintered Metal Parts - CMH 6-3538-2

Category	Subject	Suffix
CMH	6-3538	2
Corporate Manufacturing Specification.	Hardening Processes	Second Document on subject.

4.3 Proprietary Information. Standards documents containing proprietary infromation shall be identified as "IBM CONFIDENTIAL". Requests for such documents by an outside source should be referred to the local standards function.

4.4 Applicability Block. Identifies divisions, subsidiaries or locations to which a document applies.

4.5 Responsibility Block. Identifies division and/or location responsible for document maintenance.

5. DISTRIBUTION

5.1 Published standards documents shall be assigned to those manual in which they have direct or indirect application.

5.2 Distribution of standards documents shall be to bookholders of applicable manuals.

5.3 Instructions received with the document shall indicate appropriate manual, add and remove and reason for revisions.

5.4 Standards manuals and individual documents should be requested through the local Manufacturing Standards function. Indicate the following:

a. Name and man number.

b. Department number, Plant Division

c. Book number and title.

5.5 Notify the local standards function of address changes.

5.6 Manuals no longer required should be returned to the local standards area.

6. BIBLIOGRAPHY

(1) Technical Engineering Bulletin "SLT Designer's Handbook" TEB2-7060-625

(2) Power and Signal Distribution "SLT Package Engineering Spec" 811800

(3) SLT Design Guide IEP2-7100-BKT

(4) Design Automation (DA) Physical Master Tape System CEPO-2815-6

(5) Solid Logic Design Automation "Logic Block Symbols" CES 1046-003

(6) Solid Logic Design Automation "Analog Block Symbols" CES 1046-005

IBM Location Manufacturing Practice

INTRODUCTION

1.1 SCOPE: This practice is presented for use as a composite list of the abbreviations for Solid Logic Technology (SLT) terms. A revision to this document will be required as sufficient number of additional terms are introduced to this discipline.

1.2 OBJECTIVE: This practice seeks to achieve uniformity in the abbreviated presentation of SLT terms.

1.3 DEVIATION APPROVAL: Adherence to the list as presented here is expected. Deviation is controlled in accordance with local procedures.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

RECOMMENDED PRACTICES

2. ABBREVIATIONS FOR SLT

A	AND	DVR	Driver
A-2, A-3	Threshold	E	Extender
ACT	AC Trigger	Entr	Entrance from machine type
AI	AND Invert	ESD	Eight Single Diodes
AIT	AND Invert Terminate	Even	Even Count
AOI	AND OR Invert	Excl	Exclusive
AOPI	AND OR Power Invert	Exit	Exit to machine type
AOPX	AND OR Power Extend	FDD	Four Dual Diodes
AOX	AND OR Extend	FF	Flip Flop
API	AND Power Invert	FFL	Flip Flop Latch
AR	Amplifier	FL	Flip Flop Latch or Flip Latch
C or CAP	Capacitor	FTX	Four Transistors
Chan	Channel	GEN	General Usage
Cl	Cell	HD	Magnetic Head Driver
CLK	Clock	HP	High Power
Cntl or Ctl	Control	HPD	High Power Driver
Cntr or Ctr	Counter	HS	High Speed
CR	Diode	I or Inv or N	Invert
CS	Current Switch	ICN	Indicator Coupling Network
CV	Converter	ID	Indicator Driver
D or Dvr	Driver	IDL	Indicator Driver Lamp
DCI	Direct Coupled Inverter	II	Isolating Inverter
DL	Delay line	Ind	Indicator
DLD	Delay Line Driver	Ja	Jack
DLY	Delay	Jmpr	Jumper

L	Inductor
Ld	Loaded
LD	Transmission Line Driver
Lim	Limiter
Lmp	Lamp
Lp	Loop
LS	Low Speed
LSA	Line Sensing Amplifier
LT	Transmission Line Terminate
LTN	Line Terminating Network
M	Millisecond
mach	machine
MD	Magnet Driver
Mem	Memory
Mplx	Multiplex
MS	Medium Speed
N	Nanosecond
NL	No Load
Odd	Odd Count
OE	Exclusive Or
OI or OR	OR Invert
OIT	OR Invert Terminate
OR	OR
OSC	Oscillator
PB	Push button
PH	Polarity Hold
Plgbl	Pluggable
Pwr	Power or Power Supply
R or Res	Resistor
Rcvr	Receiver
Rd	Read, Reed
Reg.	Register
Rly	Relay
RW	Read-Write
S	Second
SA	Sense Amplifier
SCRID	Silicon Controlled Rectifier Indicator Driver
Sel	Select
Ser	Serial
Serv	Service or Service Voltage
SLT	Solid Logic Technology
SPD	Sample Pulse Driver
Spec	Special
SRETL	Screened Resistor Epitaxial Transistor Logic
SS	Single Shot
SSL	Single Shot Low Speed
SSA	Single Shot Medium Speed
ST	Schmitt Trigger
SW	Switch
T	Terminate
TD	Time Delay
Tgr	Trigger
Ther	Thermal Switch
TLR	Transmission Line Resistor
TLT	Transmission Line Terminate
Tx	Transistor
U	Microsecond
V	Voltage Amplifier
Var	Variable
X	Extend
XOI	Exclusive OR Invert
XOR	Exclusive OR
XORL	Exclusive OR Latch
Xtl	Crystal
Z	Impedance

IBM **Location Manufacturing Practice**

INTRODUCTION

1.1 SCOPE. This practice is presented as a composite list of term definitions used in SLT. A revision to this list will be required as additional terms are introduced to this discipline.

1.2 OBJECTIVE. This practice seeks to establish uniformity in the understanding of SLT Terminology.

1.3 DEVIATION APPROVAL. Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION. This practices was approved by the the Equipment Engineering Task Group assigned and dated 1/67.

1.5 DEFINITION. Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing Facilities.

RECOMMENDED PRACTICES

2. GLOSSARY OF TERMS

Automated Logic Diagram (ALD) is a computer generated block diagram representation of machine function.

Basic refers to the standard design of the machine.

Calm Listing refers to the Card Listing Program which generates the Card Usage by Part Number Listing, Card Usage by Category Code, Circuit Flyer Where Used, and Card Duplication Listings.

Circuit Number consists of five alphameric characters of the form ANNAA, which uniquely define a particular basic ciruit.

Design Automation refers to the programs that prepare and print the ALD's. They consist of four major stages of processing: Logic Master Tape, Simulation, Packaging and Checking, and Physical Master Tape. The outputs consist of documents to aid Engineering in the development of computers, release documents (ALD's), and tapes for manufacturing.

Dot-Block is an ALD block used on ALD logic pages to show "DOT-AND" and "DOT-OR" functions which are physically accomplished by tying two signals together at a pin. Thus, one logical net on the ALD is combined with other logical nets by the DOT-block to produce one combined physical net.

NOTE: One DOT-block cannot connect to another DOT-block.

Flexible Integrated Tooling System "FITS" is automated notching and bending equipment used for the fabrication of gate and machine frames.

Grouping refers to the associating of certain circuit configurations prior to partioning. Circuits represented on the ALD's by more than one block but always found on the same card are said to be in the same group.

Logic Master Tape (LMT) is the machine language record in logic page order. Each time a portion of this machine record is altered, logic pages containing the changes are produced for the Engineer.

Modular Power Supply (MPS) is a self contained, modular unit that generates a regulated DC voltage designed to power solid state logic and control circuits.

Net is a complex of nodes, normally pins or connectors on the ALD, all common electrically.

Net Number consists of the source block page number, block serial number, and output line position of the source block. It consists of eight alphameric chacters of the form, AANNNAAB (A - alphabetic, N - numeric, B - either alphabetic or numeric).

Node is one circuit end point of a net (Such as a pin on a card or a connector on a board).

Packaging and Checking refers to a series of programs that aid the engineer in the physical packaging of the logic and check data that is manually inserted on the pages.

Partitioning refers to that part of the design automation program that breaks up logic into cards and assigns the cards to boards.

Physical Master Tape (PMT) is a machine language record of the physical aspects of the design. It is arranged in physical sequence. Its purpose is (1) to retain in convenient form the physical data from LMT, as well as the physical data from PMT (wiring data primarily), (2) to retain the physical design at a fixed level while the logical design is undergoing change, and (3) to extract information from the tapes at the request of the engineer or other users.

Pins are the male parts of the connection between card and board or between cable connector and board.

Portion refers to those circuits on a card that are connected together by printed wiring.

Signal Name is the title that gives meaning to a logical net, each net has only one signal name.

Simulation refers to programs that allow the engineer to dynamically exercise the logic before the machine is packaged.

Sink is the end or ends of a net to which signals flow.

Source is the beginning of a net from which signals flow.

Symbolic Package is two characters used by Design Automation in the partitioning and placement programs. Blocks with the same characters in the symbolic package field are placed on the same board by the card partitioning program.

NOTE: Blocks with different symbolic packages may be packaged on the same board.

Version is a term used by Design Automation that indicates the particular manner in which logic records are kept for certain features.

Via Hole is the plated-through-hole which may or may not contain a pin; it is used exclusively as a contact between conducting layers of the board. It is not considered a node.

IBM Location Manufacturing Practice

INTRODUCTION

1.1 SCOPE: This practice presents a basic description of the SLT semi-conductor. It includes a brief physical description, pictorial displays and some basic characteristics. Its use is intended for Equipment Engineering.

1.2 OBJECTIVES: The intent is to acquaint the concerned reader with the basics in nomenclature and description.

1.3 APPROVAL: This practice was approved by the Equipment Engineering Task Group assigned and dated Jan. 67.

1.4 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

1.5 DEVIATION: Adherence to the concepts of this practice is expected. Deviation is controlled in accordance with local procedures.

RECOMMENDED PRACTICE

2. THE SLT PACKAGE

2.1 General. Solid Logic Technology (SLT) is the technology of current IBM systems. Chip, module, card, board and gate are the physical building blocks. Circuit speeds demand computer use for figuring wire lengths. Microminiaturization techniques are used in the production of devices for high-speed computers.

2.1.1 The basic semiconductors are the dual diode and the transistor chip. The chips, along with screened resistors and interconnections, are packaged in 1/2 inch square modules. The modules may have 12 or 16 pins for connections to the card.

2.1.2 The module and other electronic components are designed into circuits that have three operating speeds: 700 nonoseconds (slow speed), 30 nanoseconds (medium speed), and 5-10 nanoseconds (high speed).

2.1.3 The modules and other electronic components are mounted on cards. The card plugs into an 8.375 x 12.50 inch board. The boards are cabled into gates. The gates are cabled together to form the machine or system.

2.1.4 Design automation has developed several programs for SLT. One of these programs, called ALD's (Automated Logic Diagrams), is the computer-generated logic of the machine or system. Another computer program designs the printed wiring of the boards for optimum operation.

2.1.5 As machines operate at faster speeds, wire lengths between components become a design problem. Electricity travels at about 186,300 miles a second, which equals 11.8 inches a nanosecond. Assuming one nanosecond of delay for approximately each foot (11.8 inches) of wiring, the wiring paths for circuits in the 5-10 nanosecond range of operation can become critical. The design automation program calculates wiring paths on the card and board so that wire lengths and circuit paths are a minimum distance.

2.2 Physical Description. The smallest physical component is the dual diode or transistor chip, which is 0.025 inch square. The chip is mounted on the substrate along with other chips screened resistors, and the printed wiring. The substrate and its components are encapsulated to form a module. The module is about 1/2 inch square. Modules and molded R/C components are mounted on pluggable cards. The cards have a printed circuit (wiring) pattern and, generally, a voltage-ground plane. Card sizes are such that 6, 12, 24, or 36 or more modules may be mounted on each card. The cards may plug into one or two sockets depending upon the particular type of card. (Figures 1 through 4).

2.2.1 The cards plug into an SLT board. The board has a printed circuit (wiring) pattern on both sides, a voltage plane, and a ground plane. The physical size of the board is 8.375 inches wide and 12.50 inches high. Boards are mounted on gates and interconnected by flat cables. The gates are interconnected and make up a machine or system.

2.2.2 In summary, physical size from the smallest to the largest is: chip to module to card to gate to frame to machine.

2.3 Physical Design of Circuits. The physical building blocks of SLT are the module, card, board, and gate. The physical building blocks of the electronic circuit (the function block as found on the ALD page), are the modules and the printed circuit pattern of the card. The modules are designed so that they may be used separately or in combination with other modules or separate components. Circuits are designed to use parts of modules in combination with other modules or parts of modules and/or components. For example, the medium speed singleshot consists of: one-half of an FDD, R-1 of an R-pack, one-half of an II module, one-half of a DCI module, a timing capacitor, and all the separate parts connected by the printed circuit pattern of the card.

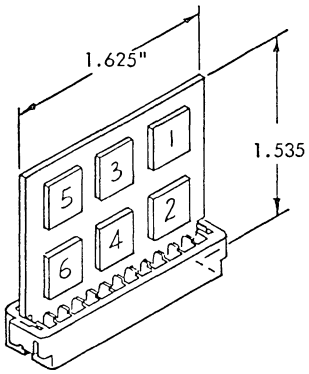
3. CARDS

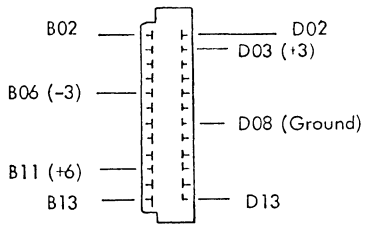
3.1 SLT cards accomodate SLT modules, R/C modules, and discrete components in various combinations. Model work with etch-it-yourself cards or wire-it-yourself cards requires ordering the raw cards, spring contacts, and contact housings individually. Artwork for the etched pattern may be taped up by local drafting or card layout groups. Design Automation requirements for creating an Engineering Description Tape (EDT) for card release are available at local DA groups or circuit packaging groups.

3.2 Nomenclature. Card types are identified by the number of board sockets required for plugging and the module capacity. (Ex: 1-12 refers to a one socket card with 12 module capacity; 2-12 refers to a two socket card with 12 module capacity; other types are 1-6, 2-24 and 2-36). See Figures 1, 2, 3 and 4. Table I lists etch-it-yourself cards, wire-it-yourself cards, and hole pattern reference drawings.

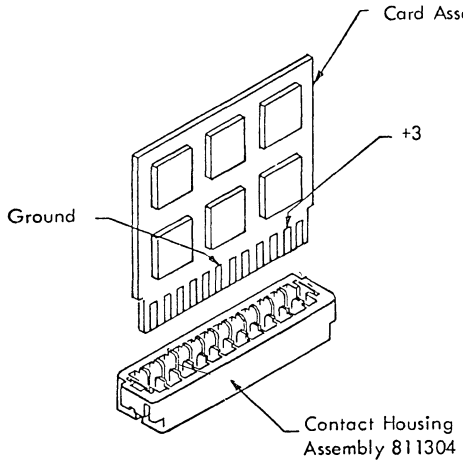
4. DISPLAYS

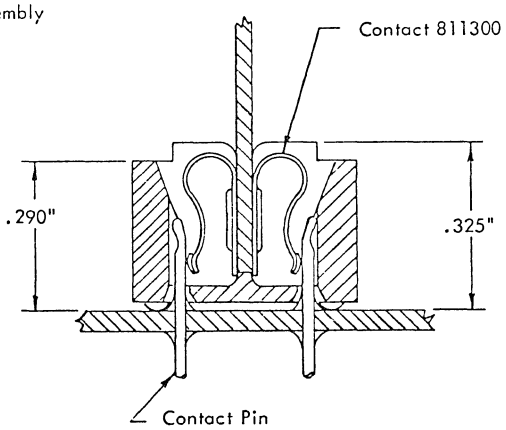
4.1 FIGURE 1. 1-6 PAC



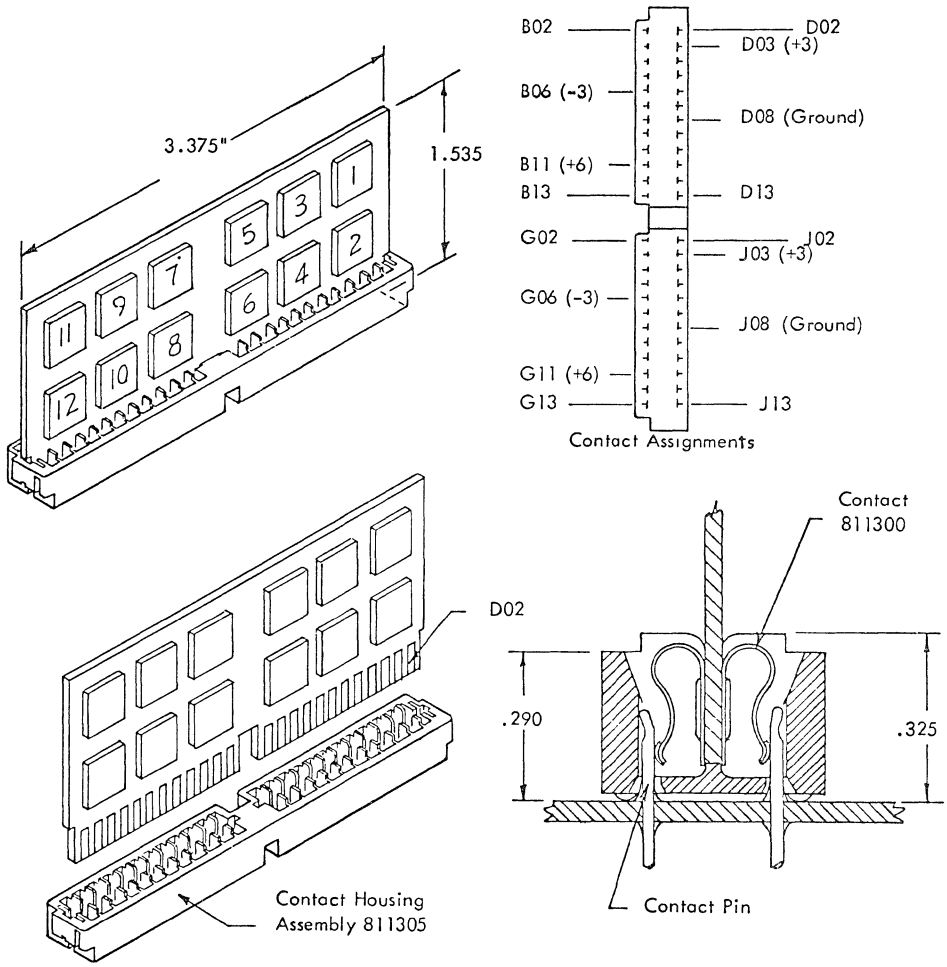


Contact Assignments

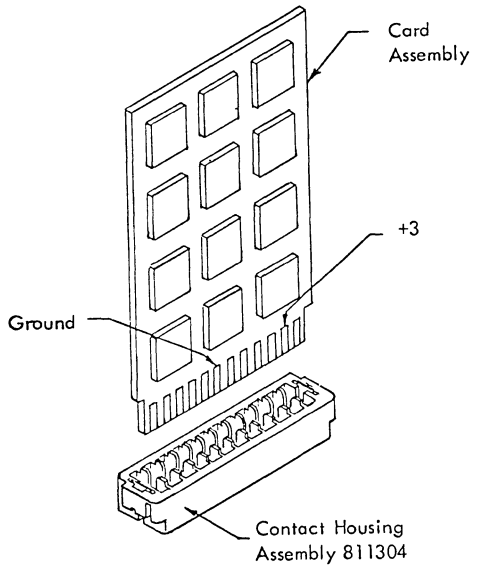




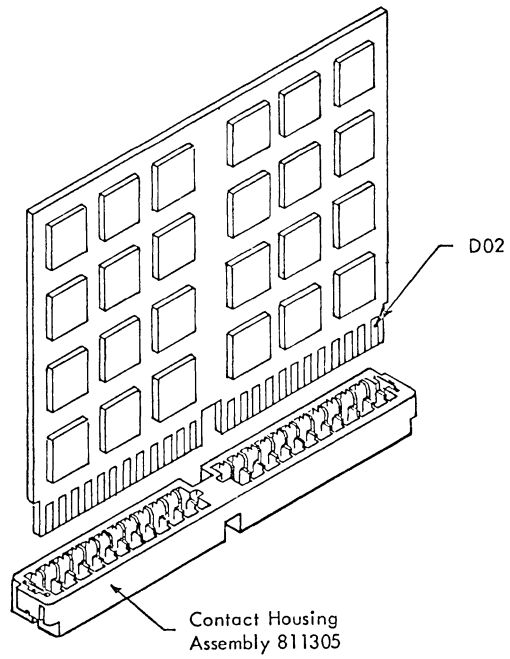
4.2 FIGURE 2. 2-12 PAC



4.3 FIGURE 3. 1-12 PAC



4.4 FIGURE 4. 2-24 PAC



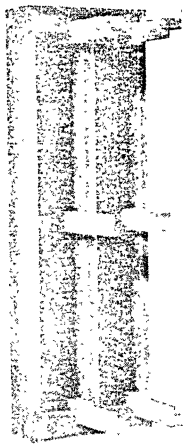
4.5 CARD TYPES

Card Type	Contact Contact	Assignment Voltage	Standard Hole Pattern Ref. Drawing	Etch-It-Yourself Cards Part No.	Etch-It-Yourself Cards Internal Planes	Wire-It-Yourself Cards Part No.	Wire-It-Yourself Cards Internal Planes
1-6	B06 D03 B11 D08	-3V +3V* +6M** Gnd.	811192	5812127	None	5800033 5800882	None None
1-12	B06 D03 B11	-3V +3V* +6M**	811370	581360 5813799 5813501	None Gnd. Gnd. & Voltage	None	None
2-12	B06 & G06 D03 & J03 B11 & G11 D08 & J08	-3V +3V* +6M** Gnd.	811193	5812130	None	5800034	None
2-24	B06 & G06 D03 & J03 B11 & G11 D08 & J08	-3V +3V* +6M** Gnd.	811371	5813632 5815525 5813504	None Gnd. Gnd. & Voltage	None	None
2-36	(Same as 2-12 and 2-24).		811229	5819007	None	None	None

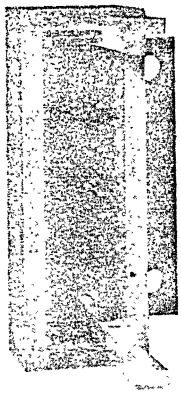
* 700 nsec circuit application +12V assigned.
**700 nsec circuit application +12M assigned.

TABLE I

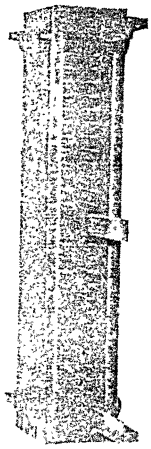
TYPE 1
DOUBLE SOCKET SQUARED PINS



TYPE 2
FOUR SOCKET SQUARED PINS



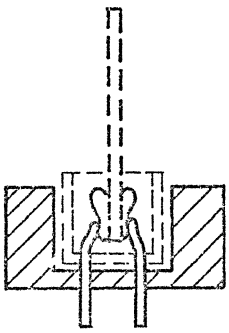
TYPE 3
SINGLE SOCKET SOLDER PINS



TYPE 4
DOUBLE SOCKET CARD SOCKET, BOTH SIDES

SPECIFICATIONS

CURRENT RATING:	-	CONTACT MATERIAL:	NICKEL
VOLTAGE RATING:	-	CONTACT PLATING:	GOLD
INSULATOR MATERIAL:	CARBAGLASS	CONTACT RESISTANCE:	5 MILLIOHMS
INSULATION RESISTANCE:	100 MEGOHMS	DIELECTRIC STRENGTH:	945V @ 60 HZ



TYPICAL CROSS SECTION
WITH CARD AND SOCKET INSERTED

PART NUMBER	TYPE	NO. OF SOCKET POSITIONS*	LAB OF CONTROL
813329	1	2	ENDICOTT
816696	2	4	ENDICOTT
818869	3	1	ENDICOTT
813392	4	2+2	ENDICOTT

* 24 PINS PER SOCKET

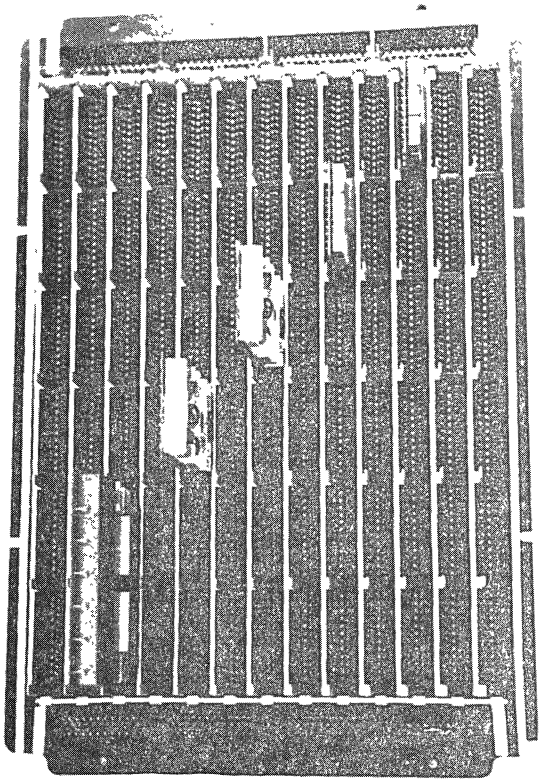
5. SLT BOARD

5.1 The SLT board (Figure 5) is the basic building block of SLT packaging. Its size is 8 3/8" by 12 1/2". The board itself is the main carrier for SLT cards as well as various connectors used to interconnect boards.

5.2 Material. Glass epoxy laminate, 1 oz./sq. ft. copper clad on both faces with optional internal copper planes for voltages and ground distribution.

5.3 Pin location. Pins are located on a .125 by .125 grid system to form socket patterns for accepting cards. The standard voltages for the SLT 5-30 NSEC hardware are -3, +3, +6 and ground. There are two types of boards which are vertical and horizontal and may be ordered in various sizes shown in Table II.

5.4 Customizing. In order to customize a board, the logic schematics must be processed through Design Automation, A Printed Circuit Generator (PCG) is used to expose land patterns on the board and then etched.



CARD SIDE OF AN SLT BOARD WITH CARD ALIGNING MOULDINGS INSTALLED

FIGURE 5

TABLE II BOARD TYPES

Board Size	Logic Card Pos.	X-Over Pos. Vert. Cable	Horiz. Cable	Basic Board For PCG	Hardware B/M	Group STFNR	Guide-post	Wire-It-Yourself Board Asm.	Inner Planes	Remarks
8.375x12.500	66	8	12	812110	5811100	811596	813621	5811536	G+V	Full size vertical;30-700 nsec.
8.375x12.500	66	8	12	812001	5811100	811596	813621	5811538	G+V	Full size vertical;5-12 nsec.
8.375x12.500	66	8	12	812002	5811100	811596	813621	5811590	None	Full size vertical
8.375x12.500	None	0	0	811066	None	None	None	811066	None	Full size Dummy Board
4.000x12.500	30	4	6	812103	5811101	811443	813621	5811560	G+V	1/2 Board
4.000x12.500	30	4	6	811226	5811101	811443	813621	5811280	G+G	1/2 Board;Ground Only
4.000x12.500	30	4	6	812274	5811101	811443	813621	5811586	None	1/2 Board
4.000x12.500	None	0	0	813768	None	None	None	813768	None	1/2 Dummy Board
5.500x 8.375	22	8	4	812054	5811103	813388	813615	5811420	G+V	1/3 Board
3.750x4.000	10	0	2	812085	812145	813586	813615	5811516	G+V	1/6 Board
2.75x4.00	8	0	0	812230	812150	-	-	5811580	None	1/9 Board
.800x3.920	2	0	0	812064	813329	813328	None	812064	None	Segment-Stiffener on one side
.800x3.920	2	0	0	812070	813392	813328	None	812070	None	Segment-Stiffener on both sides
8.500x12.250	72	12	8	812078	5811102	811780	811781	5811522	G+V	Horizontal 90° Board
8.500x12.750	72	12	8	812189	5811102	811780	811781	5811162	None	Horizontal 90° Board
8.375x12.500	77	0	0	812219	812220	815035	815037	5811588	G+V	7 x 13 Board

IBM

Location Manufacturing Practice

INTRODUCTION

1.1 SCOPE. This practice considers basic SLT circuits and circuit description relative to operating characteristics and functional application.

Circuit information is restricted to:

1. Relation of circuit inputs to circuit outputs.
2. How the circuit converts input signals to output signals.
3. Important input and output requirements.

This practice describes only those SLT circuits that are most widely used.

1.2 OBJECTIVE. This practice seeks to achieve a degree of unanimity in design of SLT circuits for use by Equipment Engineering.

1.3 DEVIATION APPROVAL: Adherence to the concepts of this practice is expected. Deviation is controlled in accordance with local procedures.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

RECOMMENDED PRACTICE

2. SLT CIRCUITS DESCRIPTION

2.1 Basic information

The basic SLT circuit is the AND-OR-Invert (AOI).

Logic may be diode, transistor, or a combination.

A logic block may use different circuits for each of the three speeds.

A transistor circuit can be approached and understood in terms of knowing the logic relation of the inputs to the outputs, or knowing the power dissipation of components and the relation of loading and input transition times to circuit delays.

2.2 Circuit Speeds

Presently there are three circuit speeds. The circuit speed is dependent upon the semiconductor and circuit configuration used. The circuit speeds are in the order of 5-10, 30, and 700 nanoseconds for each logical block.

2.3 Circuit Voltages

Approximate voltage levels for each of the three circuit speeds are:

5-10 nsec circuit:	+0.9v, most negative; +3.0v, most positive.
30 nsec circuit:	+0.0v, most negative; +3.0v, most positive.
700 nsec circuit:	+0.0v, most negative; +12.0v, most positive.

2.4 Transitions

2.4.1 Transition (Figure 1-A) is the time a transistor takes to switch. The transition points for the different families are:

Family	Transition Points
5-10 nsec high speed	+1.2v, 1.9v
30 nsec medium speed	+0.3v, 1.8v
700 nsec low speed	+0.29, 2.0v

The different transition times are turn-on-transition, turn-on-delay, turn-off transition, and turn-off delay. These values are basically the same for each of the circuit families. The major difference is that the transition points and voltage levels vary for each family.

2.4.2 Turn-on transition (Figure 1-B) is the switching time from an off state to an on state. Turn-on transition is measured on the output waveform from a specified value in the nonconducting state to a specified value in the conducting state.

2.4.3 Turn-off transition (Figure 1-C) is the switching time from an on state to an off state. Turn-off transition is measured on the output waveform from a specified value in the conducting state to a specified value in the nonconducting state.

2.4.4 Turn-on delay (Figure 1-D) is the switching time from an off state to an on state. Switching time is measured from a point where the input waveform has reached a specified value to a point where the output waveform has reached a specified value.

2.4.5 Turn-off delay (Figure 1-E) is the switching time from an on state to an off state. Switching time is measured from a point where the input waveform has reached a specified value to a point where the output waveform has reached a specified value.

3. BASIC CIRCUITS

3.1 The basic circuit of SLT is the AOI (AND-OR-Invert Figure 6). The AOI comprises an AND gate, an OR circuit, and an inverter.

3.2 The Diode AND Gate

The AND Gate is a diode AND circuit (Figure 2A). The AND circuit may be considered a plus AND, or a minus OR. The logical operation of these circuits requires:

+AND circuits: must have all plus inputs for a plus output.

-OR circuit: has a minus output if either input is minus.

The two circuits are identical; only the logical usage is different. The +AND circuit insures that both inputs are up before the output comes up; the -OR circuit has a minus output as long as any input is down. In this simplified description, the example specifies two diodes. The same description, however, applies to (n) diodes. If both inputs are minus, the polarities are correct for both diodes to conduct (Figure 2B). Because of the low forward resistance of the diodes, the output voltage will be approximately equal to the input voltage.

If input 1 changes instantaneously to a positive voltage, diode 1 is cut off because the cathode is more positive than the plate (Figure 2C). Diode 2, with 0v on its cathode, maintains conduction and the output voltage remains unchanged (0v).

When input 2 also changes to a positive voltage, diode 2 is cut off (Figure 2D). When output voltage reaches +3.0 volts, the diodes go back into conduction. The output remains at +3.0v. When input 1 falls to 0v, diode 1 conducts more heavily, and diode 2 is cut off (Figure 2E). The output follows input 1 down to 0v.

The following truth table applies to Figures 2A through 2E.

	IN		OUT
	1	2	
2B	0	0	0
2C	+3	0	0
2D	+3	+3	+3
2E	0	+3	0

This shows the AND function is satisfied at the +3v level.

The action of an AND circuit (Figure 2F) may be summarized as follows: The output voltage of a plus AND circuit approximately equals the most negative input voltage. This statement applies regardless of the number of inputs.

3.3 The Diode OR Circuit

Circuit configurations (Figure 3A) for the +OR and the -AND circuits are identical. Logical operation of these two circuits is as follows:

+OR circuit: gives a plus output, if either input is plus.

-AND circuit: requires all minus inputs for a minus output.

Therefore, the +OR circuit differs from the +AND circuit because the OR circuit needs only one input up to bring the output up. (In this simplified description, the example specifies two diodes but the description applies as well to (n) diodes.) The operation is as follows: If both inputs are at the most negative level, the polarities are correct for both diodes to conduct (Figure 3B). Thus, the input level determines the output level.

If either input diode rises to the most positive level, that diode conducts more heavily (Figure 3C). The other diode then cuts off and the output follows the input, rising to the most positive level of input voltage. Normally only one input to an OR circuit comes up at a time.

When the input that was up drops, the input diode is cut off (Figure 3D). The input diode conducts again when the output voltage reaches a point slightly more positive than the most negative input level.

The action of a plus OR circuit (Figure 3E) is summarized as follows: The output voltage of a plus OR circuit approximately equals the most positive input voltage.

3.4 The Inverter

In SLT circuits, the transistor provides inversion. The inverter used in SLT applications is the grounded emitter transistor of the NPN (P base) type.

The voltages applied to the elements of a transistor are the basis for controlling the transistor's conduction. Figure 4A relates the elements of the transistor and the tube. Transistor conduction, as defined here, is current which flows through the collector or emitter circuit.

3.4 Contd.

Bias is the term given to the control potential in both transistor and tube applications. Bias voltage is the dc voltage difference in potential between the base (grid) and the emitter (cathode). Bias voltage is the controlling factor in transistor conduction.

To determine conduction control, consider the emitter voltage to be held at a constant ground level, then apply the input voltage to the base (Figures 4B, C).

To control the conduction of the transistor, the base voltage must be capable of a level either above or below the emitter voltage.

The following rules cover conduction:

1. An NPN (P base) transistor will conduct if its base is more positive than its emitter.

2. A PNP (N base) transistor if its base is more negative than its emitter.

In tube theory, if the dynamic resistance between the cathode and plate is decreased by the grid voltage, current will flow in the plate circuit. This theory is also true in transistors; the bias potential changes the dynamic resistance between the emitter and collector, thereby controlling current flow through the transistor. A high dynamic resistance of the transistor results in little or no current flow. The direction of bias potential is called either "forward bias" (which causes conduction) or "reverse bias" (which cuts off conduction).

The property of displaying a large or a small dynamic resistance is the primary consideration in analyzing basic transistor circuits. The resistance parameter is also true in tube theory.

The following rules cover resistance:

1. A conducting (or "conditioned") transistor presents a small resistance to current flow.
2. A cut-off (or "deconditioned") transistor presents a large resistance to current flow.

Even though direction of current flow through a transistor is relatively unimportant in analyzing a circuit, two points should be remembered: (1) Current flows from emitter to collector in an NPN transistor; and (2) Current flows from collector to emitter in a PNP transistor. Remember also that even though current will flow against the direction of the arrowhead indicating the emitter (Figure 4C), current will always flow from negative to positive, so that:

1. The collector of an NPN must be returned to a more positive voltage than its emitter.
2. The collector of a PNP must be returned to a more negative voltage than its emitter.

3.5 Operating Characteristics. A conducting diode must have ground (0.6v) on the anode and +0.0v on the cathode. There is approximately a 0.6v drop across a conducting diode.

A transistor with a grounded emitter will be cut off with 0.3v at the base. An input voltage above 0.3v will start a transistor into conduction. With 0.8v at the base, the transistor will conduct to saturation.

The translate diode (Figure 6, Diode 5, i.e., the diode between the AND gate and the transistor acting as an OR diode) suppresses noise and provides uniform voltage at the base of the transistor. The voltages are 0.3v for cutoff and 0.8v for saturation.

4. CIRCUIT DESCRIPTIONS

4.1 The AND-OR-Invert circuit is used in many ways; the more common usages are included here.

4.2 AND-Invert (AI)

The AI (Figure 5) consists of a diode positive AND circuit followed by a saturating transistor inverter. Pins 2, 3, and 4 are the AND inputs. Pin 5 is available for extending the fan-in to the AND by connecting it to common anode diodes from an FDD or AOX module. Pins 8 and 9 are connected on the card for most applications. However, when collectors are dotted, only one collector resistor is needed for the common collector connection. If more collector resistors are connected, the fan-out is reduced accordingly.

The output, pin 9, fans out to a maximum of 5 AI loads for medium speed circuits, and to a maximum of 7 AI/AOI loads for slow speed circuits.

4.3 AND-OR Invert (AOI)

The AOI module (Figure 6) consists of a three-way diode positive AND function and one diode for an OR function, followed by a saturating transistor inverter, Pins 2, 3, and 4 are the AND inputs. Pin 5 will extend the fan-in to the AND by connecting it to the common anode diodes of the FDD module. Pin 1 can extend the OR fan-in from the OR diode of the AOX module. The maximum OR fan-in is 5.

The output pins, 8 and 9, are connected on the card for most applications. However, when collectors are dotted, only one collector resistor may be connected to retain the specified fan-out capability. The AOI can drive a maximum of 5 AOI circuits (low speed) or 7 AI/AOI circuits (medium speed).

4.4 AND-OR Extend (AOX)

The AOX module (Figures 7 and 8)has two identical extender circuits on one substrate. The extender circuits are used with the AI, AOI, API, and ACT to increase the input capabilities of these circuits. Each extender circuit can:

Increase the AND fan-in of the AI and AOI by four.

Increase the OR fan-in of the API by one while simultaneously increasing the AND fan-in by three.

Increase the number of AC gates on one side of one ACT by three.

Provide one DC set input for the ACT.

Increase the AND fan-in of the API by four; this requires two extender circuits.

4.5 AND Power Inverter (API)

The API module (Figure 9) is used as a power inverter with input logic capability. The API serves the same logic function as the AI module, and can drive more loads than the AI. The API module consists of a three-way diode positive AND circuit followed by a saturating transistor power inverter. Pins 2, 3, and 4 are the AND inputs. Pin 5 extends the AND fan-in by connecting to the common anode diodes of the FDD module.

Pins 8 and 9 are connected on the card for most applications. However, when the collectors are dotted, only one collector resistor can be connected (to retain the specified fan-out capability).

The API can drive a maximum of 14 AI/AOI, or equivalent, loads.

4.6 Direct-Coupled Invert (DCI)

The DCI Module (Figure 11) contains two separate direct-coupled inverters. These inverters are designed to provide a fast, economical way of extending the fan-out of an AI, or an AOI module by approximately a factor of 3. The lead between the AI or AOI output pin 9 and the DCI input pin 5 or 12 must be kept as short as possible for the full speed capability of this circuit to be realized.

The collector resistor must be connected on the driving AI or AOI to provide the necessary base current drive to the DCI. The DCI collector resistor has been left programmable, but must be connected on the card for the intended use of this module. Connect pin 2 to 3 and 8 to 9.

The circuit will not drive long transmission lines of fast output transitions.

4.7 Delay Line, Driver and Terminator (DLD)

The DLD (Figure 12) consists of (1) An API driver, (2) a programmable delay line, (3) A line Terminating Network (LTN), and (4) An AOI output stage. The output pulse width is the same as the input pulse width, but is delayed for a selected time interval.

The API line driver accepts the LTN current plus the AOI drive current, a total of 29 ma. Note that the API collector resistor is not used.

The programmable delay lines offer delays of 5-500 nsec maximum in 5 nsec increments, or four separate 5-125 nsec maximum delay lines used individually. The Line Terminating Network (LTN) with the ON input impedance of the AOI matches the characteristic impedance of the delay line (93 ohms). The AOI with the LTN acts as a terminator and as an output stage.

4.8 Delay Circuit (DLY)

4.8.1 Variable Delay Circuit. The delay circuit (Figure 13) consists of one $\overline{\text{AOX}}_1$ module, one II module, one potentiometer and one capacitor. It has a fan-in of 1 and fan-out of 5 AI's. The circuit functions as an inverter with worst case turn-off delay of 520 nsec and variable turn-on delay, ranging from 1.9 usec to 220 ms controlled by the 2K potentiomemter and the timing capacitor. For a given timing capacitor, the range of the turn-on delay is fixed (Figure 14). A continuous variation can be obtained by adjusting the potentiometer. After the circuit is turned off, a minimum time must be allowed for the timing capacitor to charge up fully before it can be turned on. Otherwise, incorrect turn-on delay will result.

4.8.2 Fixed Delay Circuit. An R/C module combines with one $\overline{\text{AOX}}_1$ module and one II module to form a delay circuit with a fixed turn-on delay of 2.8 usec or 5.6 usec $\pm$ 30 percent.

The module contains two resistors and one capacitor. The interconnections between modules remain as shown except that the R/C module is used to replace the 2K trim potentiometer and the timing capacitor.

4.9 Triggers

4.9.1 The AC Trigger (ACT) (Figure 15) consists of two AI modules, one AOX module and a four-capacitor C-pak. Additional components may be added to increase flexibility.

The cross-coupled inverters are fed at their respective bases either from the up level of a DC set pulse (at a DC set or DC reset input), or from the positive going edge of an AC set pulse (at the AC inputs).

4.9.1 (Continued)

The current from an AC set pulse is directed into the base of a transistor in the cross-coupled latch or is bypassed through a gate diode as determined by the voltage at the cathode of this diode. If the cathodes of the three gate diodes associated with a common AC input are at an "up level" (+3v), current from the AC input will start trigger switching by turning the transistor, connnected to this gate network, from off to on. If the cathode of any one gate diode is tied to a saturated collector (0.3v), the AC input current for the gate will be sent to the gate diode through the saturated collector to ground, preventing trigger switching.

The DC set and reset inputs (11) and (12) can be driven from any 30 nsec logic block. If is impossible to program collector resistors as in other 30 nsec circuits. The number of inputs for each side of the AC trigger is:

AC inputs--1.

Input Gates available for use with each AC input--3.

DC input--1.

4.9.2 Multi-Gated Trigger

Two sets of RC Networks provide for both triggering and binary operation (Figure 29). A negative going pulse, introduced at the "off" side, will cause the trigger to change state. Inputs, pins 1 and 2 provide for DC set. All inputs can be driven from any 30 ns logic block. The extender, pin 7, provides connection for additional diodes that may be used for DC resetting. Pins 3 and 8 are extenders for additional AC inputs.

4.10 High Power Driver (HPD)

NOTE: 1. This is not a standard application of the DCI Module. The HPD is a selected DCI that has closely matched transistors to allow parallel operation of the two inverters.

2. The collector current can become 80 ma for the most unbalanced transistor pair.

3. The HPD module may not be used as a DCI.

The HPD (Figure 16) is a high-current driver made by connecting the two inverters in parallel on a specially selected DCI module. The HPD can be driven by an AI or an AOI if the collector resistor on the driving block is returned to +6v. The HPD is mounted in the adjacent module position.

The API-3v can also drive the HPD with normal power supplies.

The HPD may be used to drive a large number of loads (36 AI or 28 AOI) or it may drive long transmission lines. The HPD may not be used to drive both LSA's and regular loads simultaneously. The HPD cannot drive long lines when it is driving a high fan-out of AI's, etc., because of the reflections on the unterminated transmission lines.

4.11 Indicator Coupling Network (ICN)

The indicator coupling network (Figure 17) is used in conjunction with a 3v, 9 ma incandescent lamp. One end of the lamp is returned to +6 volts and the other end to R_1 of the coupling network.

The lamp glows when the driving collector is down. Thus, the lamp will glow when all of the AND circuit inputs are up on the driving block. The coupling network draws the same current as two logic loads. Three logic blocks and one indicator may be driven from a logic block.

The lamp may be located remote from the coupling network.

4.12 40-ma Switch (Indicator Driver) (ID_2)

The 40-ma Switch (Figure 18) is a driver capable of accepting 40 ma at its output. It is used in slow speed applications such as an indicator driver.

The ID_2 may be driven by high, medium, or low-speed circuits. Its driver may drive the regular AND blocks and the ID_2 block. It cannot be driven from an LSA.

4.13 Indicator Driver (ID)

An II stage (a saturating transistor) (Figure 19) serves as a driver for both the up and down level indicators.

The bulb, when lit, indicates the state of the input level. The up level indicator requires a 1 and the down level indicator a 0 at the input to turn the light on.

Because of the high impedance of the II the driver can drive its full load plus the indicator driver (ID).

The indicator driver, besides driving either of the indicators (bulbs), can also drive an API/AOPI load for latch-back (transient noise indication).

Using one II/DCI module, two "R-Paks", and two bulbs, these combinations are possible:

1. Two up-level indicators.

2. Two down level indicators.

3. One up and one down level indicator.

4.13 (Continued)

The following special conditions apply for the ID:

1. The indicator driver(s) must not be used as a link in a logic chain.

2. II/DCI or XOI loads must not be driven by IDL's.

3. The indicator driver(s) can drive, besides the bulb and its network, an additional AI/AOI or API/AOPI load only for latch-back purposes.

4.14 Isolating Inverter (II)

The II module (Figure 20) consists of two isolating inverters. Because of the current-limiting resistor in the base, the II fan-out capability is only 7 AI/AOI, or equivalent, loads. Pins 1 and 6 are the input pins and pins 2, 3 and 8, 9 are the output pins. Pins 2, 3 and 8,9 may be connected on the card for most applications. When the collectors are dotted, only one collector load resistor is connected to retain the specified fan-out capability.

4.15 Sample Pulse Driver (SPD)

The SPD (Figure 21) consists of one-half of a DCI, one-half of an FDD, one-half of a TTX and a pulse transformer. The input to the SPD can be an AI, AOI, or API minus the collector resistor. When the input is at the up level, T_1 is turned on and current is built up in the primary inductance L_1 with a time constant of L_1/R_1. During the time that T_1 is on, T_2 remains off. When the input is at the down-level, T_1 switches off. The current in the primary inductance falls at a rate of di_1/dt, and T_2 is turned on by the mutual coupling in the transformer. When T_2 is turned on, a large current is delivered to the load.

The diodes at the collector of T_2 limit the voltage swing, while the diodes between the collector of T_1 and the emitter of T_2 are used for the off current from the AC inputs. The SPD must drive at least 16 AC inputs on two separate lines of no more than 10 inches each when the output of the SPD has no load resistor. When only two AC inputs are used, the output of the SPD must be terminated with a 50-ohm resistor. The SPD can drive 20 AC inputs when the output is not terminated. The output of the SPD is an emitter follower, and the impedance reflected back to the emitter decreases as the number of AC inputs increases.

4.16 Single-Shot Medium Speed (SSA)

The SSA (Figure 22) uses one AI module, one-half of a DCI module, one-half of an AOX module, a trim potentiometer, and a timing capacitor. However, the AI module is not used as an AND inverter: It is used solely to provide a transistor and two resistors. The AND diodes of the AI modules are not used, the translate diode is shorted and the 3.6K and the 2K resistors are paralleled. The output pulse is controlled by the 10K trim potentiometer and the timing capacitor, C_T. For a given C_T, the range of the output pulse width is fixed, and by means of the trim potentiometer, a continuous variation can be obtained.

4.17 Exclusive OR Latch (XORL)

The XOR Latch (Figure 23) has a single bi-stable output that can be changed by proper sequencing of the control and data inputs. The inputs can be used in either sequence 1 or sequence 2:

4.17.1 Sequence 1

a. Data Line Up - With the rise of the clock pulse the output will be set to the (0) state. All further changes in the control line will not affect the state of the latch.

b. Data Line Up - With the rise of the clock pulse the output will be set to the (1) state. All further changes in the control line will not affect the latch state.

4.17.2 Sequence 2

a. Data Line Up - With the fall of the clock pulse the output will be held in the (0) state.

b. Data Line Down - With the fall of the clock pulse the output will be held in the (1) state.

In either sequence 1 or 2, the control is normally down.

4.18 Exclusive-OR (XOR)

This circuit (Figure 24) performs the exclusive OR of the signals applied to pins 6 and 3 when pins 6 and 1 are tied together. When the inputs are both up or both down, the output will be at a potential of less than 0.30v. When the inputs are not identical (i.e., one up and one down) the output will be between 2.0v and 3.0v, depending on the loads.

The XOR module will not perform the exclusive OR latch function. The XORL module is the exclusive-OR-latch.

4.19 Crystal Oscillator (OSC)

The free-running cyrstal oscillator (Figure 25) serves as a pulse generator. The oscillator produces pulses or voltage variations of a definite frequency, e.g., 4.0 mc. The circuit consists of a basic switching circuit whose output is determined by the quartz crystal. The crystal vibrates at 4.0 mc and develops a sinusoidal voltage that is amplified and clipped to produce the square wave output of the oscillator. The inductively tuned tank circuit provides regenerative feedback to sustain the cyrstal oscillations.

4.20 Line Sensing Amplifier (LSA)

The LSA (Figure 10) line termination consists of a resistor network at the end of the line and one to ten LSA circuits placed at the end of the line or distributed along the line.

4.21 Extender (E) and DOT Functions

AND circuits and OR circuits may be connected together to produce a single output (Figure 26). When the circuit of the AND or OR block is diode logic, one logic block is connected to the other by an extender (E). The extender (E) is, in effect, a method of adding diodes to the input of a circuit. The extender symbol (E) is only used on the ALD's when the connection is made between two cards.

When the output of the AND or OR block comes from a transistor (vs a diode) the logic blocks are connected with the DOT block (Figure 27 and 28). The DOT block is simply wiring connecting the outputs of two or more transistors.

The function of the DOT block depends upon the desired logical use of the shared transistors. Generally, the AND DOT is a +A; the OR DOT is a -OR.

5. DISPLAYS

5.1 Transitions and Circuit Measurements

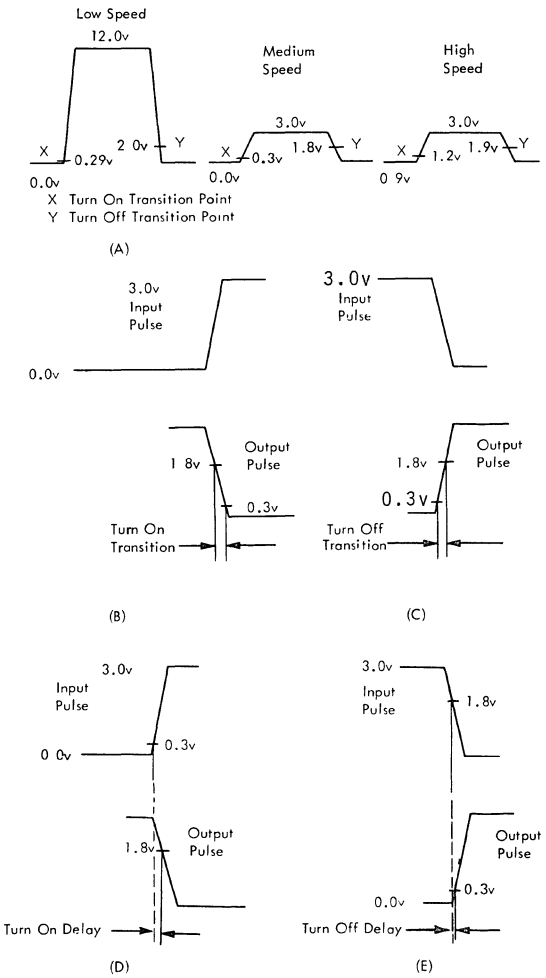


FIGURE 1

5.2 The AND Gate

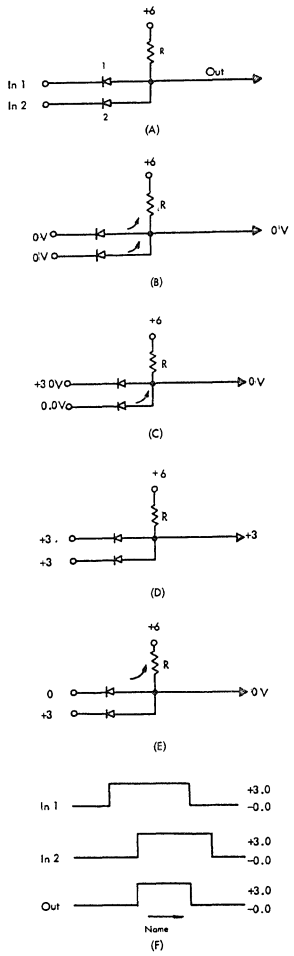


FIGURE 2

5.3 The OR Circuit

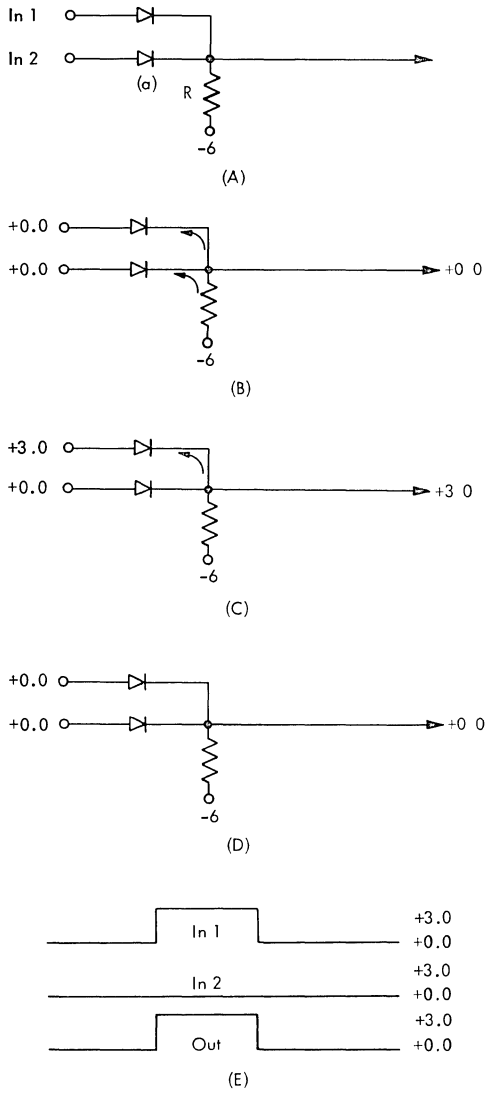


FIGURE 3

5.4 The Inverter

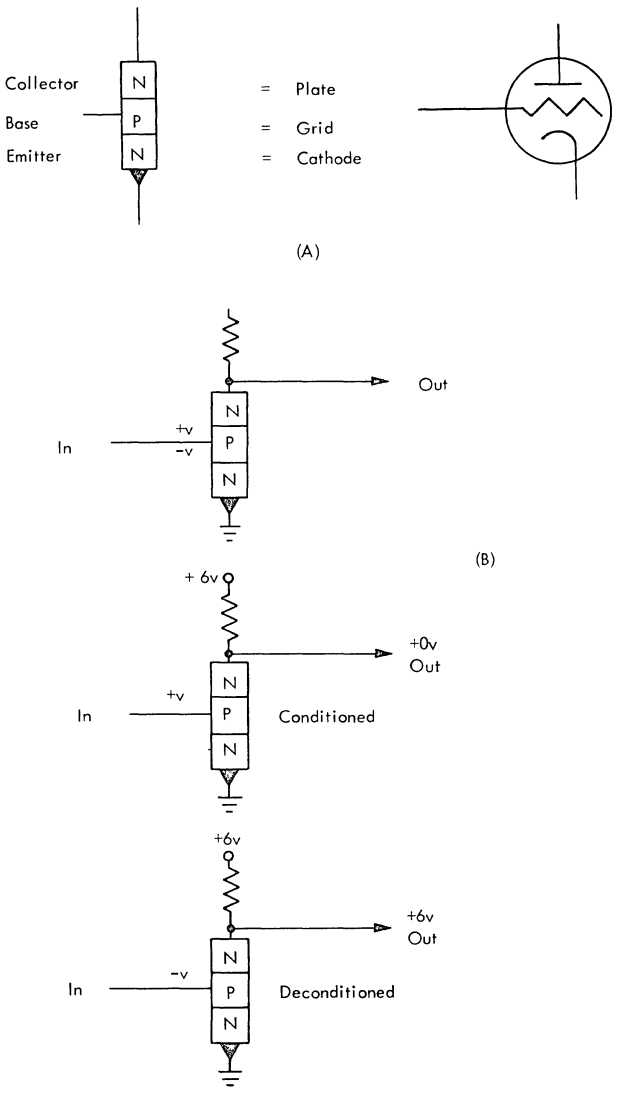


FIGURE 4

5.5 AND-Invert, Medium-Speed (AI)

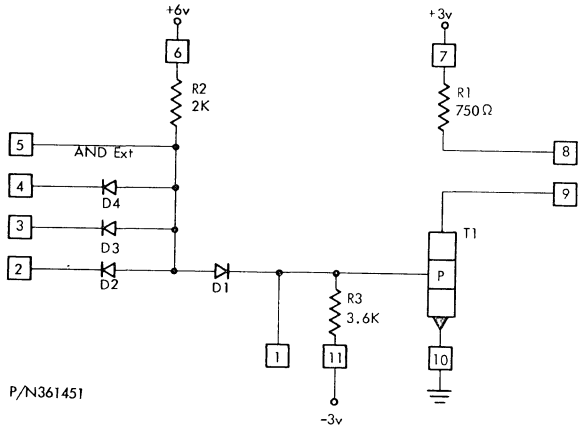


FIGURE 5

5.6 AND-OR-Invert, Medium-Speed (AOI)

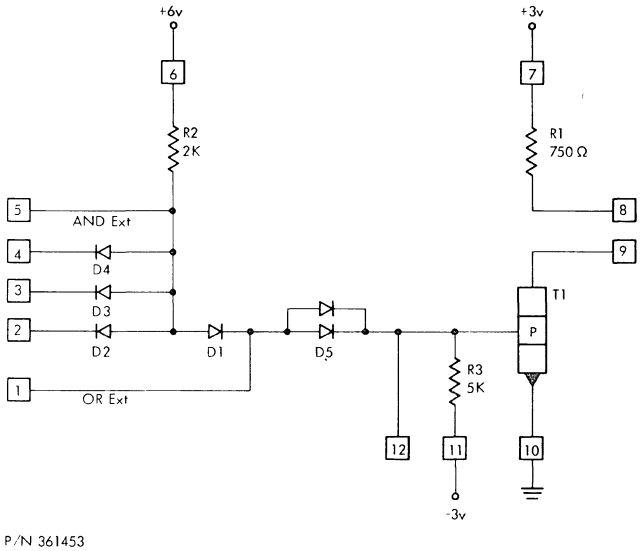


FIGURE 6

5.7 AND-OR-Extend, Medium-Speed (AOX)

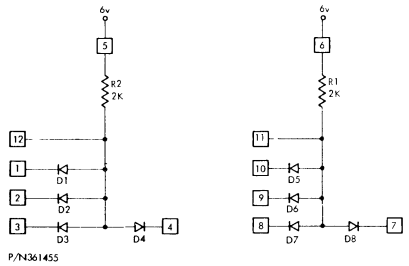


FIGURE 7

5.8 AND-OR-Extend, Medium-Speed (AOX_B)

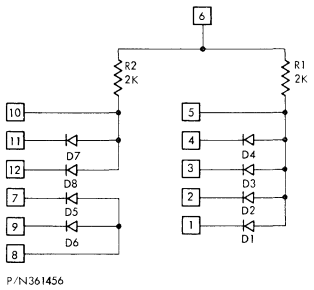


FIGURE 8

5.9 AND-OR-Power-Invert, Medium-Speed (AOPI)

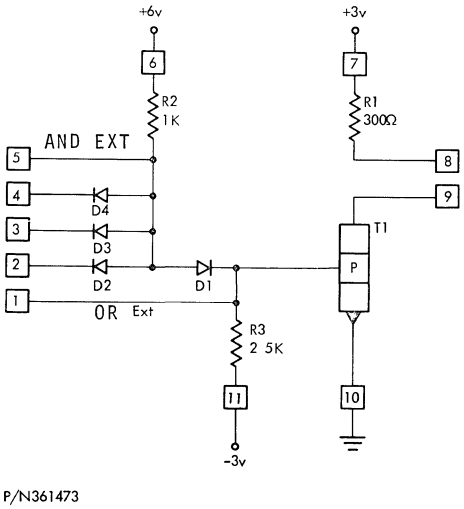
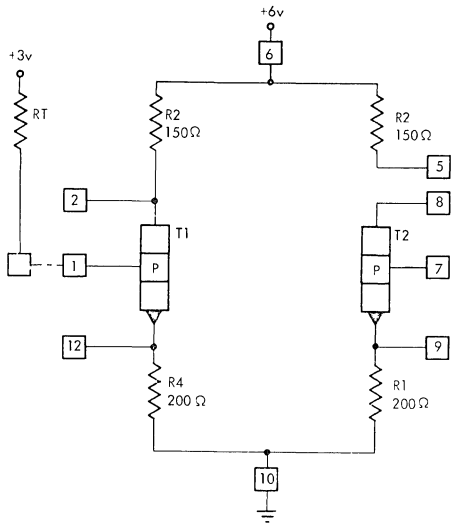


FIGURE 9

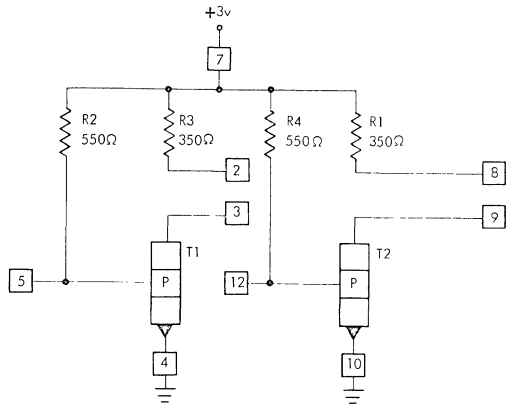
5.10 Line Sense Amplifier Medium-Speed (LSA)



P N 361476

FIGURE 10

5.11 Direct Coupled Invert, Medium-Speed (DCI)



P/N 361454

FIGURE 11

5.12 Delay Line Driver and Terminator (DLD)

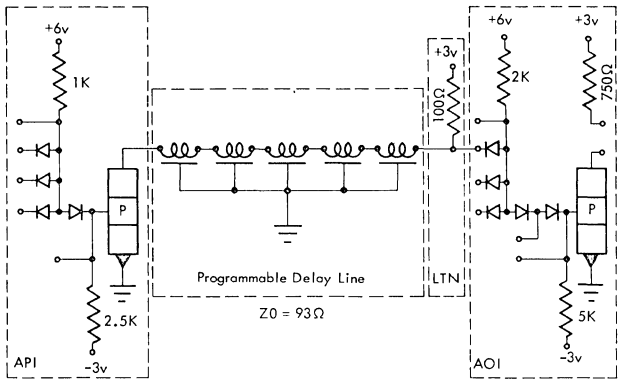


FIGURE 12

5.13 Delay Circuit (DLY)

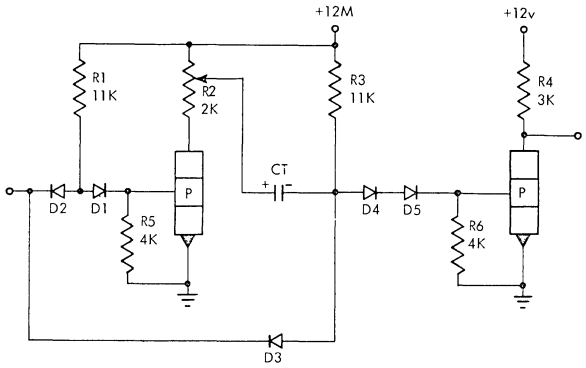


FIGURE 13

5.14 DLY Timing Capacitors

Capacitor		Turn-On Delay			
0.00068	uf	1.4	-	5.5	usec
0.0018	uf	4.5	-	14.6	usec
0.0047	uf	12	-	38	usec
0.012	uf	30	-	97	usec
0.033	uf	83	-	260	usec
0.082	uf	205	-	660	usec
0.22	uf	550	-	1,780	usec
0.56	uf	1.4	-	4.5	ms
1.5	uf	3.7	-	12	ms
3.9	uf	9.7	-	31	ms
10	uf	25	-	81	ms
27	uf	67	-	220	ms

FIGURE 14

5.15 AC Trigger (ACT)

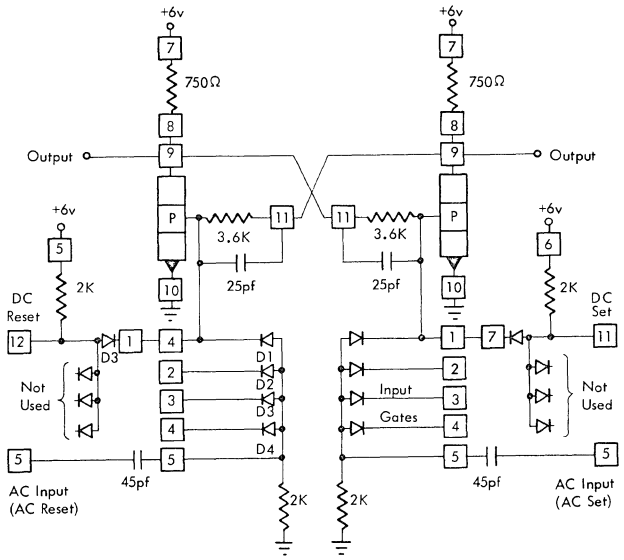
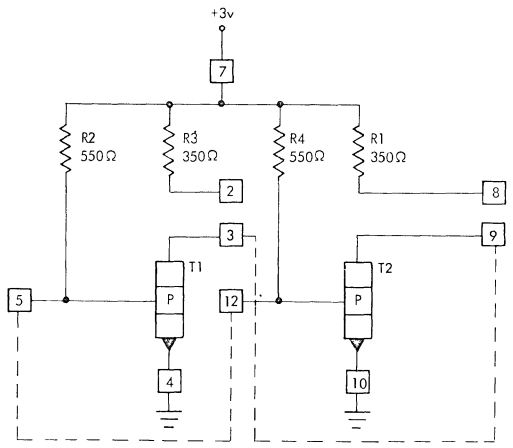


FIGURE 15

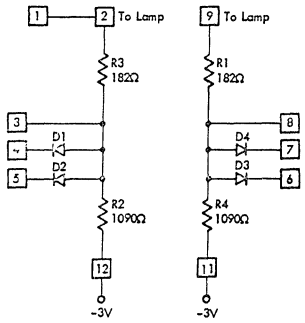
5.16 High Power Driver (HPD)



P/N 361475

FIGURE 16

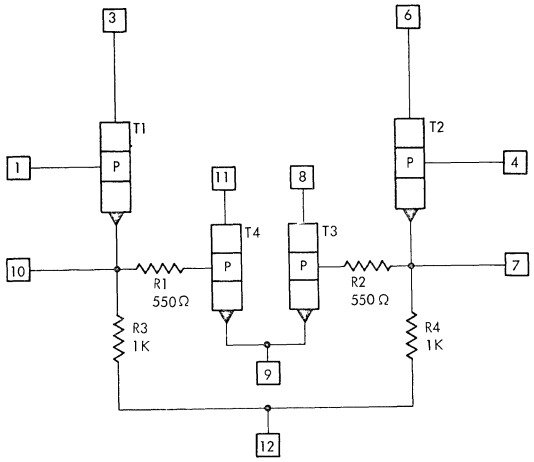
5.17 Indicator Coupling Network (ICN)



P/N 361471

FIGURE 17

5.18 Indicator Driver, 40 ma (ID)



P/N 361426

FIGURE 18

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5.19 Indicator Driver (ID)

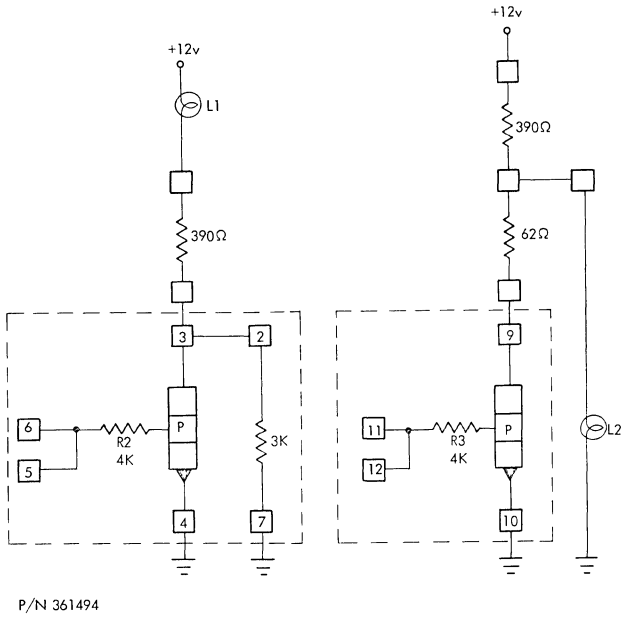


FIGURE 19

5.21 Sample Pulse Driver, Medium-Speed (SPD)

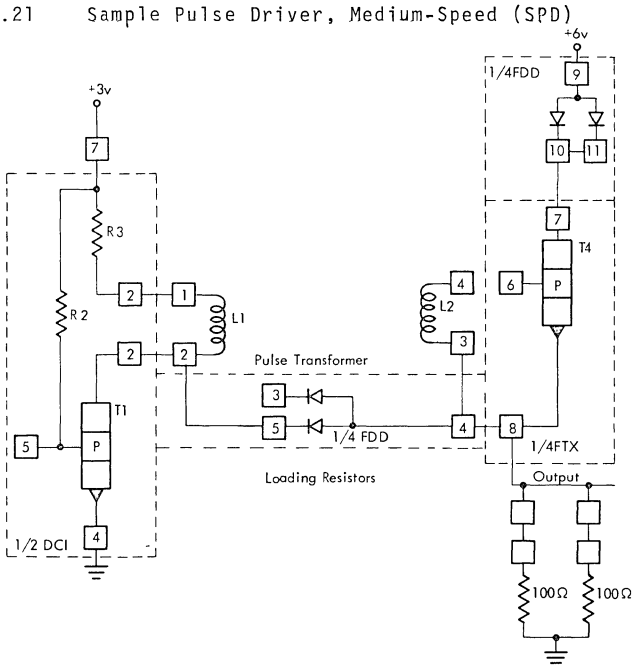


FIGURE 21

5.20 Isolating Inverter, Medium-Speed (II)

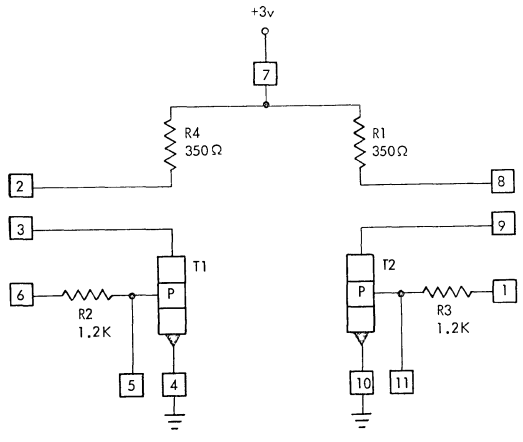


FIGURE 20

5.22 Singleshot, Medium-Speed (SSA)

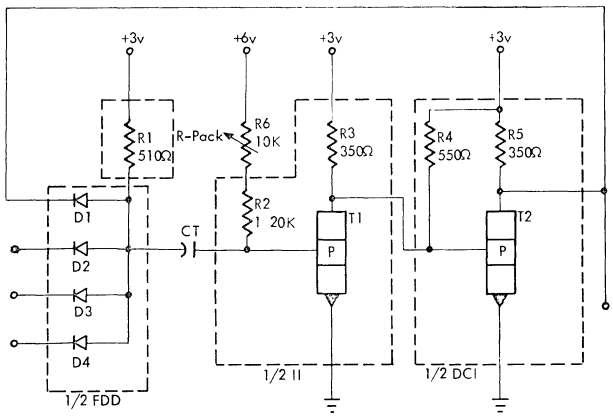


FIGURE 22

5.23 Exclusive OR Latch, Medium-Speed (XORL)

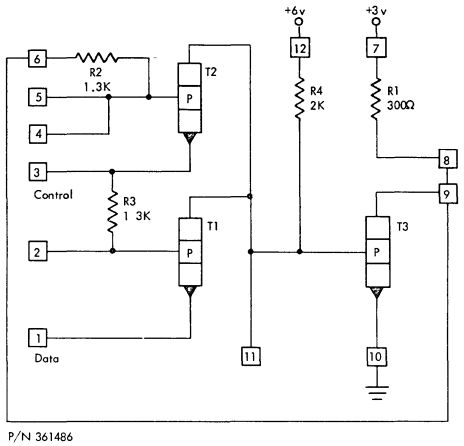


FIGURE 23

5.24 Exclusive OR, Medium-Speed (XOR)

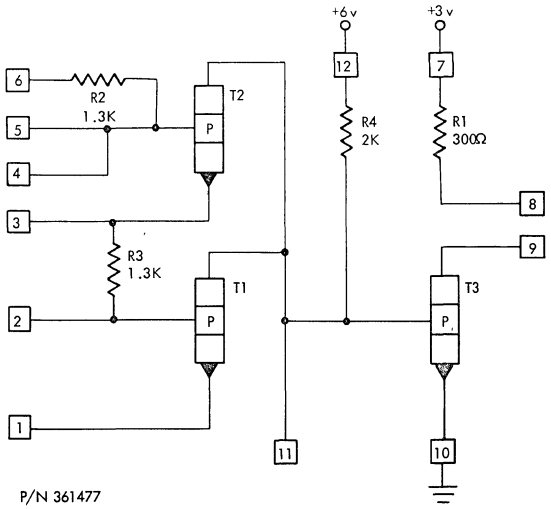


FIGURE 24

5.25 Crystal Oscillator

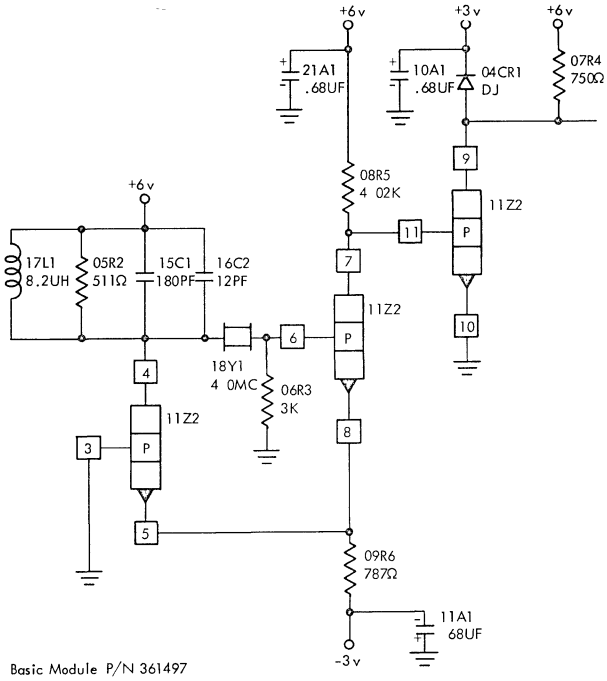


FIGURE 25

5.26 Typical Extender Circuit

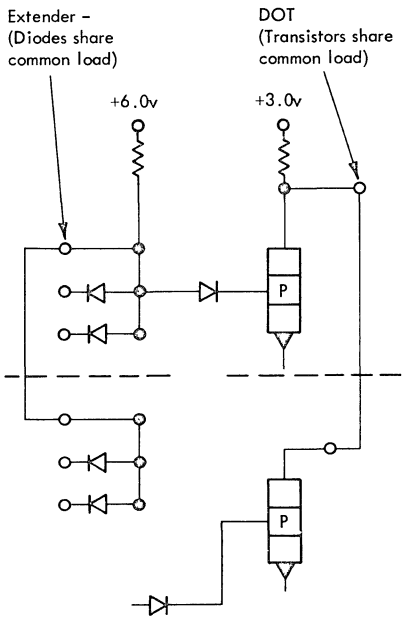
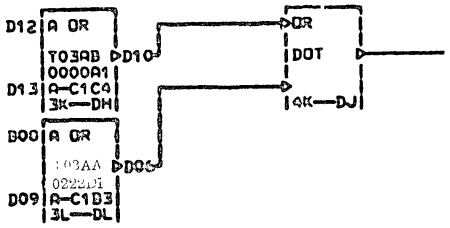
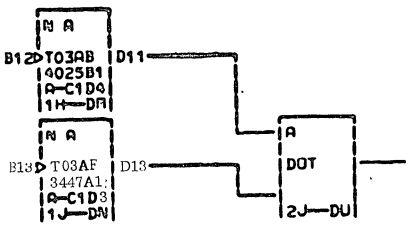


FIGURE 26

5.27 The OR DOT Block



5.28 The AND DOT Block



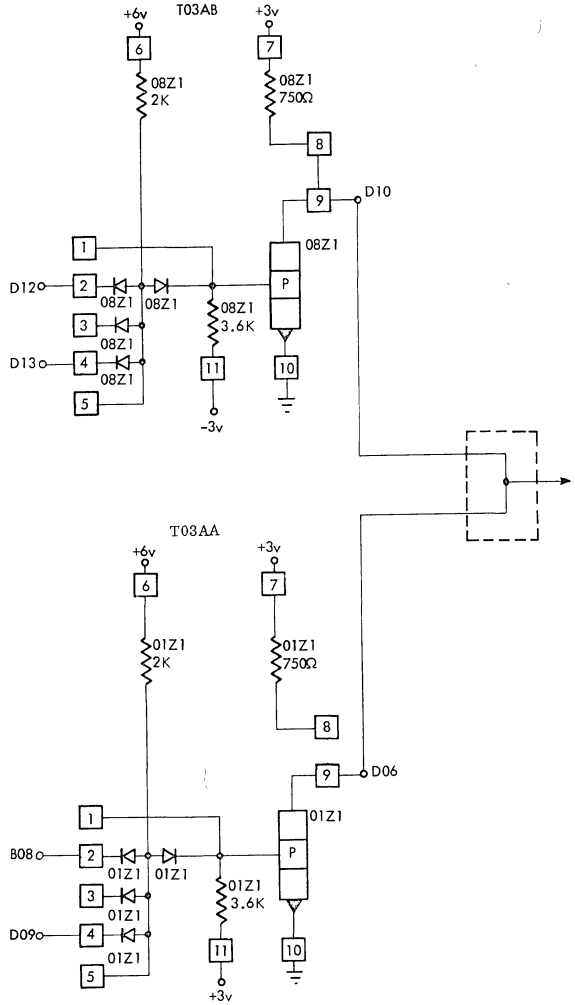


FIGURE 27

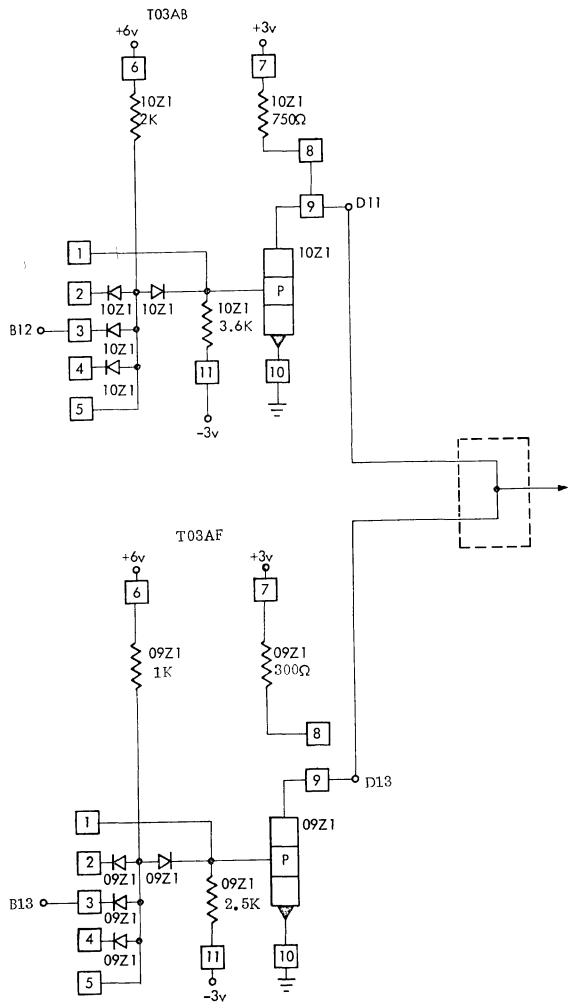


FIGURE 28

5.29 Multi-Gated Trigger

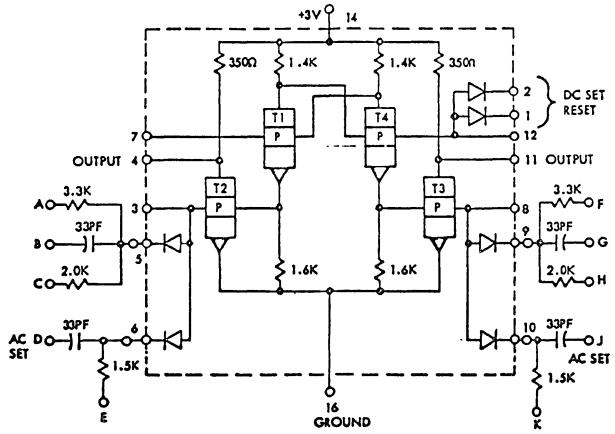


FIGURE 29

INTRODUCTION

1.1 SCOPE: This practice presents modules of the 30 NSEC circuit family.

1.2 OBJECTIVE: The objective of this practice is to aquaint the SLT designer with the wide range of module configurations available. Its use is intended for Equipment Engineering design effort.

1.3 DEVIATION APPROVAL: Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

RECOMMENDED PRACTICES

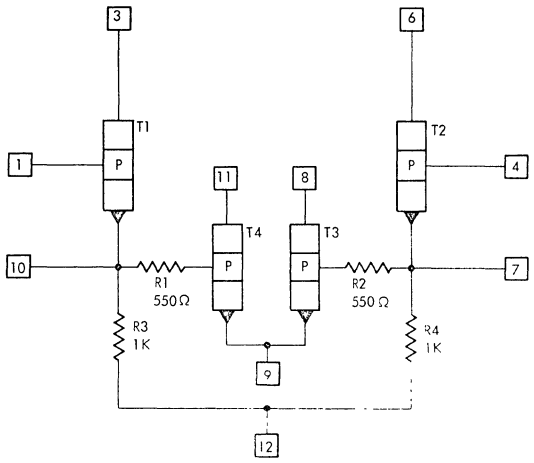
2. MODULE CONFIGURATIONS

2.1 For ease in cross-referencing, the modules are listed below by part number, name and by type.

Part Number	Name	Type	
361426	ID	GEN	(SEE FIGURE 1)
361427	TLR	MS	(" " 2)
361428	Mplx Rcvr	MS	(" " 3)
361429	FTX	MS	(" " 4)
361430	FTX	GEN	(" " 5)
361431	ESD	MS	(" " 6)
361433	FTX	MS	(" " 7)
361434	SA	GEN	(" " 8)
361435	FF	MS	(" " 9)
361437	FTX	MS	(" " 10)
361438	FTX	GEN	(" " 11)
361451	AI	MS	(" " 12)
361453	AOI	MS	(" " 13)
361454	DCI	MS	(" " 14)
361455	AOX	MS	(" " 15)
361456	AOX_B	MS	(" " 16)
361457	FTX	MS	(" " 17)
361459	FDD	MS	(" " 18)
361473	API-3V	MS	(" " 19)
361475	HPD	MS	(" " 20)
361476	LSA	MS	(" " 21)
361477	XOR	MS	(" " 22)
361479	II	MS	(" " 23)
361480	ID	MS	(" " 24)
361481	FDD	MS	(" " 25)
361485	FDD	GEN	(" " 26)
361486	XORL	MS	(" " 27)

3. DISPLAYS

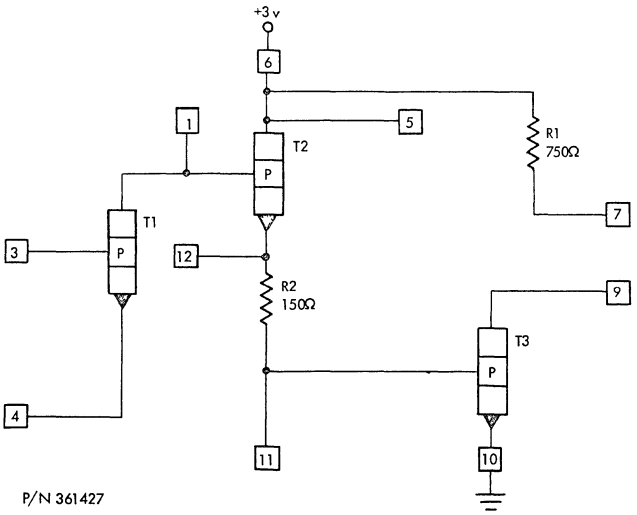
3.1 ID-40 MA Switch-General



P/N 361426

FIGURE 1

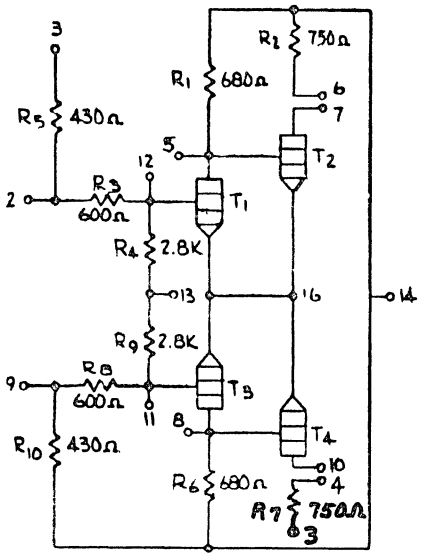
3.2 TLR-Transmission Line Receiver



P/N 361427

FIGURE 2

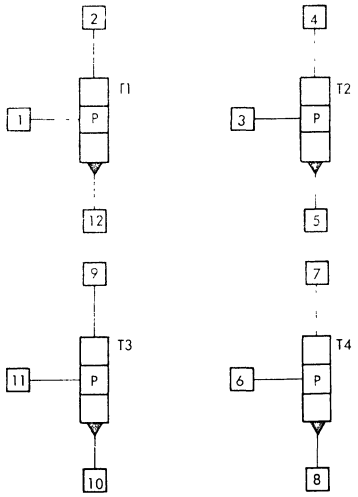
3.3 Multiplex Receiver



P/N 361428

FIGURE 3

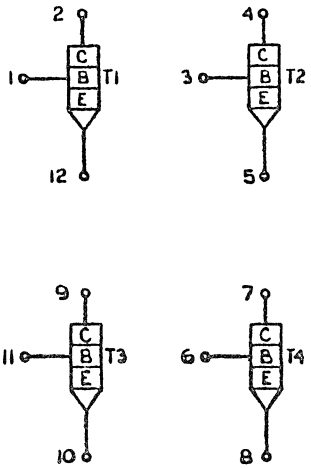
3.4 FTX-Four Transistors (12V)



P/N 361429

FIGURE 4

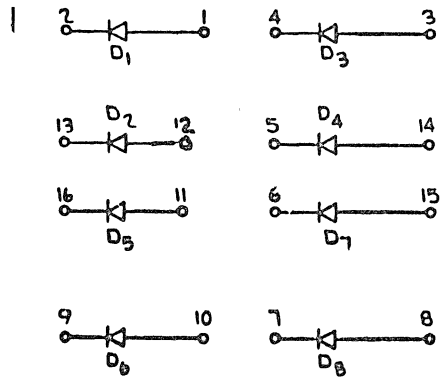
3.5 FTX-For Amplifier Application - General



P/N 361430

FIGURE 5

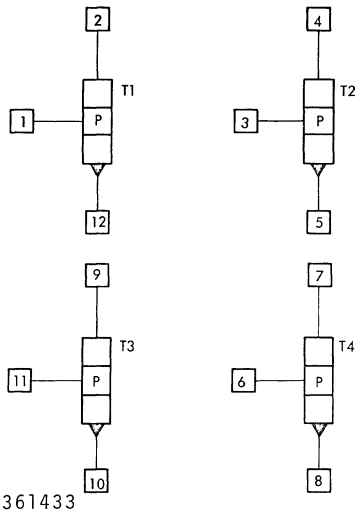
3.6 ESD - Eight Single Diodes



P/N 361431

FIGURE 6

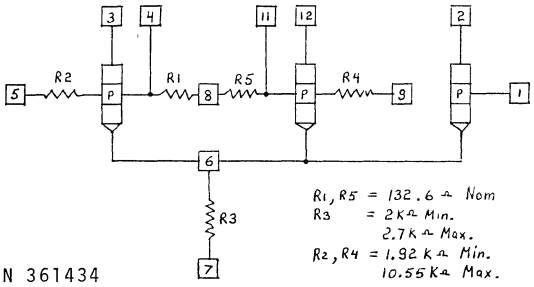
3.7 FTX-Four Transistors



P/N 361433

FIGURE 7

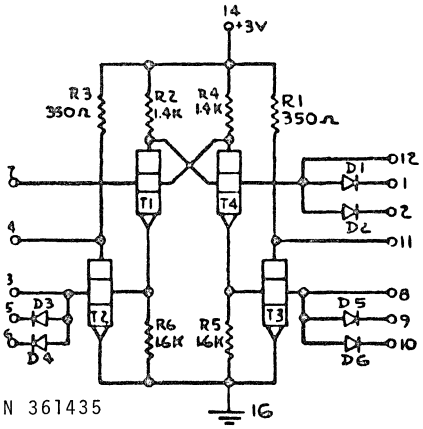
3.8 SA-Sense Amplifier - General



P/N 361434

FIGURE 8

3.9 Multi-Gated Trigger



P/N 361435

FIGURE 9

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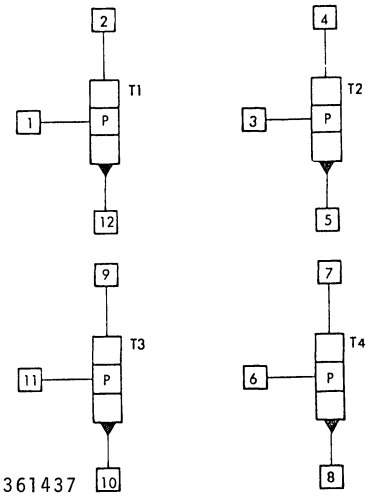
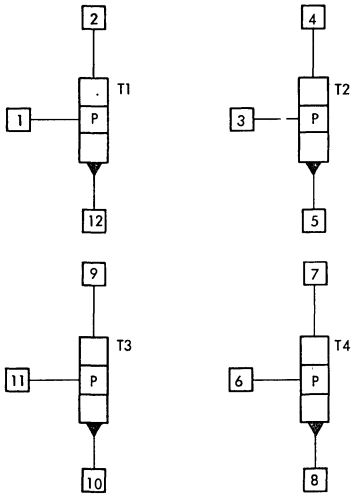
3.10 FTX - Four Transistors



P/N 361437

FIGURE 10

3.11 FTX - Four Transistors - General



P/N 361438

FIGURE 11

3.12 AI and Invert

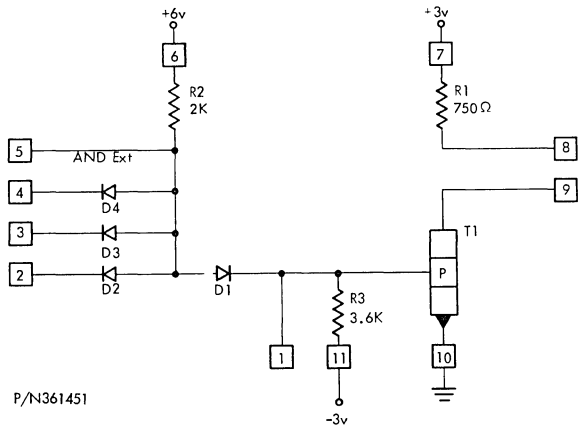
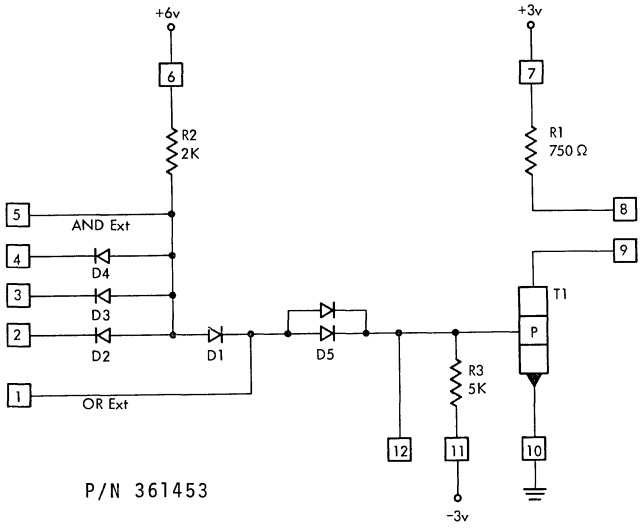


FIGURE 12

3.13 AOI AND-OR-Inverter



P/N 361453

FIGURE 13

3.14 DCI - Direct Coupled - Inverter

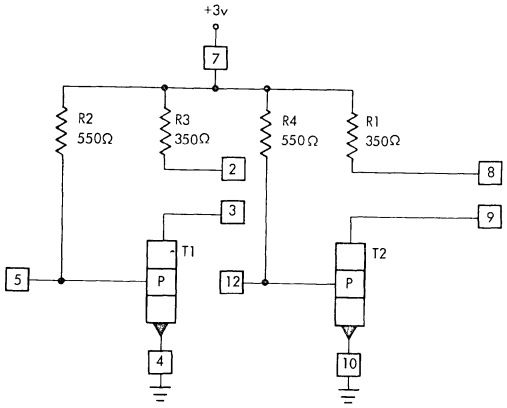


FIGURE 14

3.15 AOX - AND-OR-Inverter

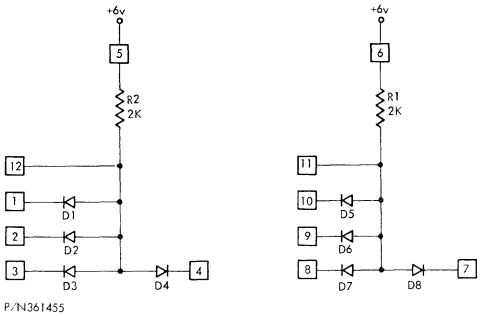


FIGURE 15

3.16 AOX_B - AND-OR-Extender

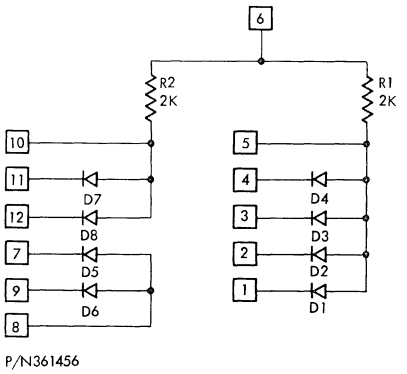


FIGURE 16

3.17 FTX - Four Transistors (9V)

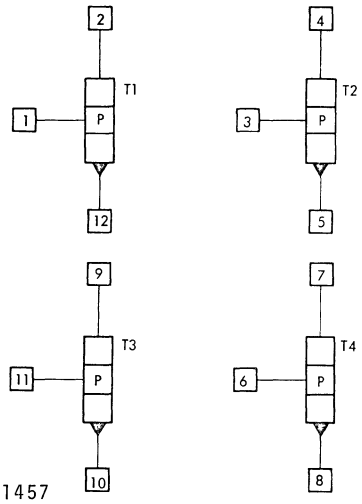


FIGURE 17

3.18 FDD - Four Double Diodes

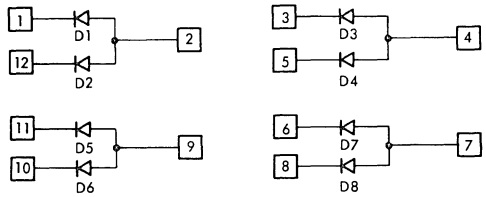


FIGURE 18

3.19 API - AND Power Invert (3V)

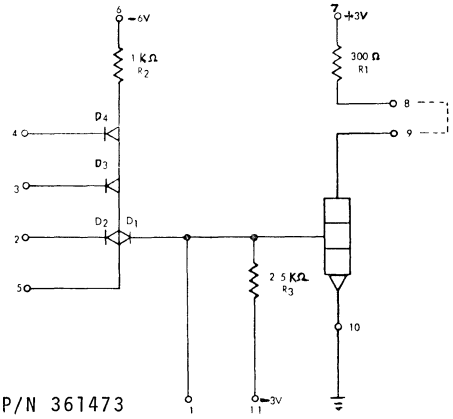


FIGURE 19

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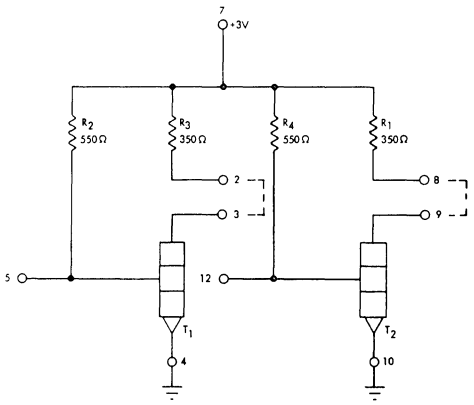
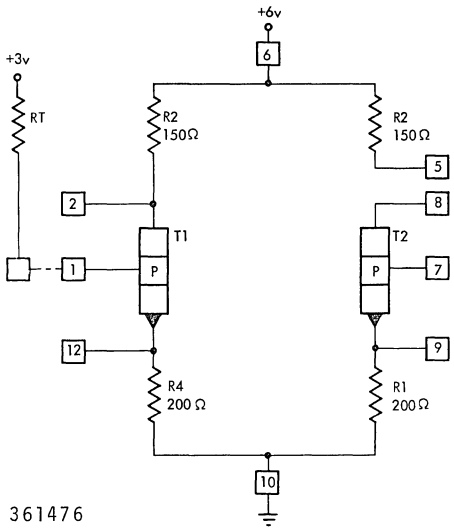
3.20 HPD - High Power Driver



P/N 361475

FIGURE 20

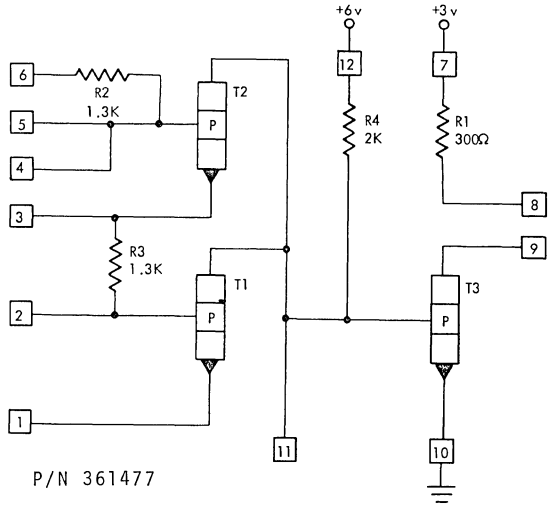
3.21 LSA - Line Sense Amplifier



P/N 361476

FIGURE 21

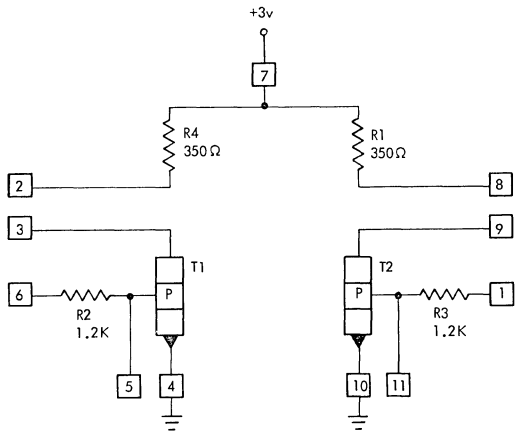
3.22 XOR - Exclusive OR



P/N 361477

FIGURE 22

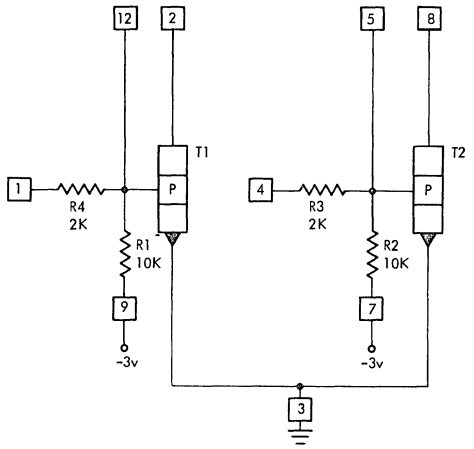
3.23 II - Isolating Inverter



P/N 361479

FIGURE 23

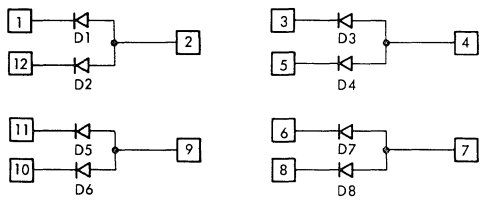
3.24 ID - Indicator Driver



P/N 361480

FIGURE 24

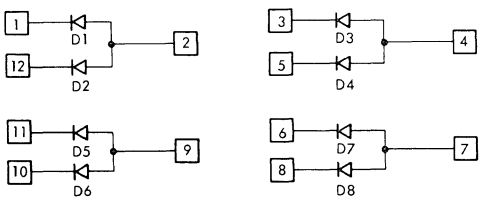
3.25 FDD - Four Double Diodes



P/N 361481

FIGURE 25

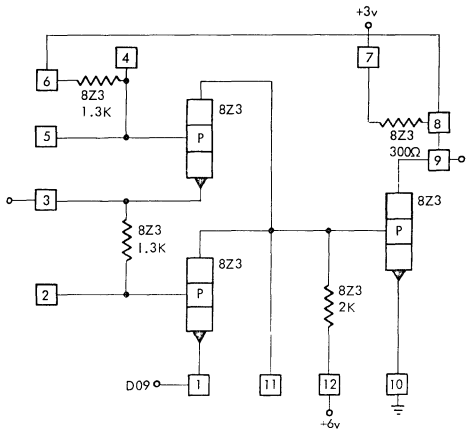
3.26 FDD - Four Double Diodes - General



P/N 361485

FIGURE 26

3.27 XORL - Exclusive OR Latch



P/N 361486

FIGURE 27

INTRODUCTION

1.1 SCOPE. The purpose of this practice is to provide the designer with the block identification number which is the code for a particular circuit.

1.2 OBJECTIVE. The objective is to provide uniformity in the presentation of block identification numbers and their related circuit name.

1.3 DEVIATION APPROVAL. Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION. This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION. Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

RECOMMENDED PRACTICE

2. CIRCUIT FLYER LISTING

2.1 The Block Identification Number or Circuit Number is the coded name given to a particular circuit. This number can be found in a cross-reference called the "Circuit Flyer Title and Specification" list. This list contains all circuit numbers in alphanumeric order and calls out all the circuit flyers associated with the block identification or circuit number. In the logic block configuration, this number will always be found inside the block on the third line.

2.1.1 Logic General Form - XYYZZ

X DEFINED

S - SRETL General
T - 30 ns
U - 5-10 ns
V - 700 ns
0 - Analog

YY DEFINED

03 - Logic Blocks
05 - Voltage Translate Circuits
06 - Transmission Line Drivers and Receivers
07 - Sense Amplifiers
10 - Inverting Drivers Less than 50 ma
11 - Non-Invert Driver Less Than 50 ma
15 - Power Driver More Than 50 ma
16 - Magnetic Head and Core Driver
20 - Triggers
21 - Singleshots
22 - Oscillators
25 - Regulators, Clamps, Clippers, and Limiters
32 - Gates
40 - Specials
45 - Delay Circuits
55 - Indicator Circuits
60 - Integrators and Filters
61 - Components
63 - Reed Relays
65 - Functional Card
66 - Field Replacement Card

ZZ DEFINED - THE UNIQUE CIRCUIT

2.2 The following list presents representative circuit groupings from the "Circuit Flyer Title and Specification" list.

Circuit Number	Title
S03AG	MULTIPLEX INTERFACE DRIVER-M4
S03AH	SELECT SAFETY
S03AI	AND-DOUBLE GATE
S03AJ	AND-HARPER GATE
S03AW	SPECIAL RECEIVER 750 OHM LOAD
S03SA	NEGATIVE OR DIODES
S03SC	CURRENT CONTROL AND EMITTER LOAD
S03SD	RESISTOR OR
S03SE	HIGH VOLTAGE AND
S03SF	AC AND
S03SG	AC AND
S03SJ	BINARY OUTPUT
S03SK	AC SET AND RESET
S03SL	MINUS AND
S03SM	NEGATIVE AND
S03SN	DUAL DIODE OR
S03SO	DUAL DIODE AND
S03SP	NON SYMETRICAL OR
S03SQ	AND-DOUBLE GATE
S05AB	U TO T CONVERTER
S05AC	L TO U CONVERTER
S05AE	MULTIPLEX INTERFACE RECEIVER
S05AG	SLT STANDARD INTERFACE DRIVER
S05AH	ISOLATING INVERTER
S05AJ	HI-GAIN AMPLIFIER
S05AK	UNITY GAIN AMPLIFIER
S05AM	FINAL AMPLIFIER
S05AO	DELAY LINE TERMINATOR
S05AR	MULTIPLEX INTERFACE DRIVER
S05AS	ISOLATING INVERTER NO LOAD
S05AT	U TO L CONVERTER
S05AU	T TO L CONVERTER
S05AW	5NS TO 30NS INTERFACE

Circuit Number	Title
S05AZ	INTERFACE TRANSMITTER
S05CA	INPUT AMPLIFIER DISC SPEED DETECT
S05CB	OUTPUT AMPLIFIER DISC SPEED DETECT
S05CD	50 OHM CABLE DRIVER CIRCUIT
S05CE	S TO SLT LEVEL CONVERTER
S05CF	CABLE TERMINATOR CIRCUIT
S05CH	CONVERTER
S05CI	CLAMPING TERMINATOR
S05CJ	TRANSMISSION LINE RECEIVER WITH GA
S05CM	SLT +3V TO +5V CONVERTER
S05EB	NAND SLT CONVERTER
S05EC	SLT NAND CONVERTER
S05SA	ISOLATING INVERTER WITH DELAY
S05SB	CONVERTER
S05SC	LEVEL CONVERTER
S06AB	INHIBIT TIMER
S06AC	MULTIPLEX INTERFACE DRIVER
S06AE	FIX STROBE EF
S06AK	TRANSMISSION LINE RECEIVER
S06AN	TRANSMISSION LINE RECEIVER W LD
S06AS	LOOP 2.0MC RD BUS TERM
S06AT	EMITTER FOLLOWER C13
S06AV	RESISTOR TERMINATORS 100 OHM
S06EA	NPL TERMINATION
S06SA	LINE DRIVER
S06SC	DATA LINE RECEIVER
S06SD	MULTIPLEX LINE DRIVER
S06SE	MULTIPLEX LINE DRIVER 3
S07AA	PREAMPLIFIER
S07AC	SENSE AMPLIFIER 1 PART A
S07AD	SENSE AMPLIFIER 1 PART B
S07AE	SENSE AMPLIFIER 2 PART A
S07AF	SENSE AMPLIFIER 2 PART B
S07AQ	PHOTOCELL AMPLIFIER
S07AS	SENSE AMPLIFIER
S07AT	SENSE AMP C13
S07CF	SYNC SENSE AMP
S07EA	PUNCH DETECTOR
S07ED	PREAMPLIFIER
S07EE	PREAMPLIFIER OUTPUT
S07LA	PHOTO TRANSISTOR SENSE AMPLIFIER
S07LB	PHOTO TRANSISTOR EF
S07SF	PREAMPLIFIER
S07SI	CYLINDER PULSE PRE-AMP
S07SJ	PREAMPLIFER
S07SK	LOW LEVEL SOLAR CELL AMP
S07SL	READ AMPLIFIER
S07SM	PUNCH CHECK AMPLIFIER
S07SN	WRITE ERASE CURRENT DETECT
S07SO	PREAMPLIFIER
S07SP	DIFF-LIN AMP
S07SQ	HEAD DE-SELECT CKT
S07SS	INDEX PRIMARY AMP
S07SU	CYLINDER PREAMP
S07SV	DETENT PREAMP

Circuit Number	Title
S07SW	INDEX PREAMP
S07SX	READ AMPLIFIER 2
S07SZ	CE TEST AMP.
S07TA	AMPLIFIER AND FILTER
S07TB	AMP-DIFFERENTIATOR
S07TE	PREAMPLIFIER
S07TF	TACH BUFFER AND FILTER
S07TG	POWER AMPLIFIER
S10AF	25MA RELAY DRIVER
S10AG	LOOP 2.0MC VFO CLAMP DRIVER
S10AH	37MA RELAY DRIVER
S10SB	GATE CONTROL
S10SC	INVERTER WITH LOAD
S10SE	AI WITH LOAD
S10SH	EMITTER AMPLIFER
S10SI	INVERTER WITH LOAD
S10SJ	INVERTER POWER
S10SK	INVERTER UNLOADED
S10SL	INVERTER
S10SM	INVERTER CLAMP
S10SN	INVERTER
S10SO	INVERTER
S10SP	POWER INVERTER
S10SQ	INVERTER
S11AE	EMITTER FOLLOWER
S11AG	DELAY LINE DRIVER
S11AL	DATA CONCENTRATOR RDU
S11AM	OSCILLATOR AMP
S11EA	DELAY LINE DRIVER
S11SA	EMITTER FOLLOWER - V.C.
S11SB	EMITTER FOLLOWER HEAD LOAD
S15AE	1.3 AMP DRIVER
S15AG	DRIVE FOR 1.3 AMP DRIVER
S15AH	100 MA HAMMER DRIVER
S15AI	Y-SELECT
S15AK	300MA DRIVER
S15AQ	PROLAY DRIVER
S15AR	RELAY DRIVER
S15AW	1.7A SOLENOID DRIVER
S15AZ	DATA CONCENTRATOR 2 RDM
S15CA	650 MA SOLENOID DRIVER
S15EB	400 MA DRIVER
S15EC	DRIVER FOR 2.2 A DRIVER
S15ED	DRIVER FOR 2.2 A DRIVER
S15EF	2.2 A DRIVER
S15EJ	R/W DRIVER
S15LA	CLUTCH DRIVER
S15LB	BRAKE DRIVER
S15LC	48V 0.1 AMP RELAY DRIVER
S15SA	INHIBIT DRIVER
S15SF	STROBE DRIVER
S15SG	DRIVER GATE CONTROL
S15SH	1 AMP 8MS SOLENOID DRIVER
S15SL	1 AMP PNP DRIVER
S15SM	1 AMP NPN DRIVER

Circuit Number	Title
S15SN	2.5 AMP DRIVER 1
S15SO	.5 AMP NPN DRIVER
S15SP	2.5 AMP DRIVER 2
S15SQ	HIGH CURRENT SWITCH 1
S15ST	INHIBIT DRIVER
S15SV	WRITE DRIVER INVERTER
S15SX	POWER TRANSISTOR
S15SY	POWER TRANSISTOR 257
S15SZ	POWER INVERTER HEAD LOAD
S16AE	Z DRIVER
S16AG	TITLE R/W DRIVER
S16AH	CORE DRIVER-INHIBIT
S16AI	X-Y CORE DRIVER
S16AJ	CURRENT SWITCH-CORE
S16AK	SWITCH DRIVER
S16AL	WRITE DRIVER
S16AT	DIFFERENTIATOR
S16AU	AC COUPLED AMPLIFIER
S16CH	READ AMP FILTER
S16CJ	STROBE DRIVER SP4
S16CK	SINGLE SHOT CONTROL
S16CL	ARRAY DRIVER C13
S16CM	WRITE DRIVER
S16EA	Z-DRIVER
S16EB	TERMINATOR GATE
S16EC	INHIBIT TIMER
S16SA	X-Y DRIVER
S16SB	X-Y DRIVER
S16SC	ERASE DRIVER
S16SD	WRITE DRIVER
S16SE	WRITE CURRENT SOURCE
S16SG	WRITE HEAD SELECT
S20SA	TRIGGER
S21AA	50-60 PULSE PER SECOND
S21AF	PULSE FORMER SINGLE SHOT
S21AI	VAR. FREQ. SINGLE SHOT
S21SB	MAGNETIC CB SHAPER
S21SC	PRECISION TIMER
S21SD	2 SECOND TIMER
S21SE	SINGLE SHOT 60NS
S21SF	SINGLE SHOT 165 USEC
S21SG	SINGLE SHOT 800 USEC
S22AA	4 MC OSCILLATOR
S22AE	5KC XTAL OSCILLATOR
S22AK	500 KC XTAL OSCILLATOR
S22AL	720KC XTAL OSCILLATOR
S22AS	500KC GATED OSCILLATOR
S22AT	700KC GATED OSCILLATOR
S22AZ	5 WAY PLO
S22CH	4 MC XTAL OSCILLATOR
S22CI	1.36 MC CRYSTAL OSC
S22CJ	1.496 MC CRYSTAL OSC
S22CK	3.2648KC XTAL OSCILLATOR
S22CL	4.004KC XTAL OSCILLATOR
S22CM	4.84KC XTAL OSCILLATOR

Circuit Number	Title
S22CN	5.0063KC XTAL OSCILLATOR
S22CO	SLT 5.9176KC XTAL OSCILLATOR
S22CP	1.460 MCS OSCILLATOR
S22CU	CYRSTAL OSCILLATOR
S22CV	4.0 MC CRYSTAL OSCILLATOR
S22CW	3.3KC XTAL OSCILLATOR
S22CX	4.4KC XTAL OSCILLATOR
S22DE	2.0KC CRYSTAL OSCILLATOR
S22LA	4.26KC XTAL OSCILLATOR
S22LB	5.824KC XTAL OSCILLATOR
S22LC	3.64KC XTAL OSCILLATOR
S22LE	6.4KC XTAL OSCILLATOR
S22LF	4.8KC XTAL OSCILLATOR
S22LG	7.04KC XTAL OSCILLATOR
S22LH	9.6KC XTAL OSCILLATOR
S22SA	185KC OSCILLATOR
S22SC	400 CPS OSCILLATOR
S25AA	Z CLAMP
S25AB	GATE CLAMP
S25AC	REFERENCE VOLTAGE
S25AD	REFERENCE VOLTAGE
S25AE	RW DRIVER CLAMP
S25AF	LOOP 2.0MC AMP-LIMITER
S25AH	9V REGULATOR
S25AI	REGULATOR 9V
S25AJ	13V CLAMP
S25AK	VOLTAGE REGULATOR C13
S25AL	VOLTAGE REGULATOR
S25AM	VOLTAGE CLAMP +0.125 V DC
S25AT	CLAMP DIODES +3V
S25CF	SINGLE SHOT REF
S25EA	VOLTAGE DIVIDER
S25EC	+12 CCROS DRIVER SUPPLY
S25EB	CAPACITOR COUPLING NETWORK
S25EE	DIODE
S25EF	R/W DRIVER CLAMP
S25LA	POSITIVE TRANSITION DETECTOR
S25SA	VOLTAGE SET FOR SAR
S25SB	REFERENCE TEMPERATURE LEVEL
S25SD	DRIVER CONTROL
S25SE	DIODE CLAMP
S25SF	CURRENT SOURCE
S25SG	POWER REGULATOR 20V
S25SH	VOLTAGE REFERENCE 50MV
S25SI	VOLTAGE REFERENCE 5V
S25SL	VOLTAGE REGULATOR
S25SM	POWER REGULATOR 60V
S25SN	LEVEL SETTER
S25SO	OVER DRIVEN AMPLIFIER
S25SP	VOLTAGE REGULATION 36 OHM
S25SQ	RECTIFIER
S32AB	GATE
S32AC	TERMINATOR GATE
S32AE	GATE
S32AF	LOOP 2.0MC LWR GATE

Circuit Number	Title
S32AG	LOOP 2.0MC LINEAR GATE
S32EB	GATE TRANSISTORS WITH CLAMP
S32EC	GATE TRANSISTORS WITH CLAMP
S40AB	SECTOR SWITCH
S40AC	SPEED DETECTOR
S40AD	INDEX GENERATOR
S40AG	LOOP 2.0MC REF CLOCK GEN
S40AJ	LOOP 2.0MC PEAK PULSER
S40AM	LOOP 2.0MC SQUELCH DRIVER
S40AO	FREQUENCY DETECTOR DISC SPEED DET
S40EA	SWITCH NETWORK
S40EB	TEMP SENSING NETWORK
S40SA	POWER SUPPLY 28V
S40SB	POWER SUPPLY 28V
S40SD	SENSE LEVEL VOLTAGE
S40SE	REF VOLTAGE
S40SF	+4V SPECIAL VOLTAGE
S40SH	LEVEL SETTING
S40SI	POWER SUPPLY SAFETY
S40SJ	NULL BIAS
S40SK	VARIABLE CURRENT SOURCE
S40SL	DC SAFETY
S40SM	AC SAFETY
S40SO	VOLTAGE TO FREQUENCY CONVERTER
S40SP	LEVEL INDICATOR MINUS
S40SQ	LEVEL INDICATOR PLUS
S40SR	DETECTOR AMPLIFIER
S40SS	SINGLE BRK FUNC GENERATOR
S40ST	FAIL SAFE BLOCKING VALVE DET
S40SV	REFERENCE VOLTAGE
S40SW	ZERO S DETECTOR
S40SX	GAP SENSOR
S40SY	DETECTOR
S40SZ	RAMP GENERATOR
S40TA	CAP SENSOR
S40TB	TEST REFERENCE CIRCUIT
S40TE	0.45 AMP DRIVER
S40TF	BALANCE NETWORK
S40TG	LEVEL DETECTOR
S40TH	VOICE COIL AMPLIFIER
S40TL	DETECTOR CIRCUIT
S40TM	WRITE SELECT
S40TN	A C UNSAFE
S40TO	VOLT TO HIGH FREQ CONV
S40TP	ZERO S DETECTOR (0.438 MBS)
S40TQ	GAP SENSOR (0.438 MBS)
S40TR	DETECTOR (0.438 MBS)
S40TS	RAMP GENERATOR (0.438 MBS)
S40TW	WRITE SAFETY LATCH
S40TX	SCHMIDT TRIGGER
S40TY	TRANSDUCER DETECTOR
S40TZ	LEVEL DETECTOR
S45AB	5 to 25 NS DELAY LINE
S45AC	TAPPED DELAY LINE
S45AD	5-125 NS DELAY LINE

Circuit Number	Title
S45AE	DELAY LINE TERMINATOR W/O-L
S45AH	ELAPSED TIME METER DISPLAY
S45AK	DELAY LINE 0-125
S45AN	VARIABLE DELAY .2 SEC TO 2.0 SEC
S45EA	350 NS DELAY LINE
S45EB	3 to 8.6 SECOND TIME OUT
S45EC	VARIABLE TIME DELAY 5-125NS
S45SB	500 NS DELAY LINE
S45SC	DELAY LINE IMS
S45SD	DELAY 90 SEC
S55AA	40 MA INDICATOR DRIVER
S55AD	15 MA INDICATOR NETWORK
S55AH	LAMP DRIVER-ID 2
S55EA	40 MA LAMP RESISTOR NETWORK
S55EB	40 MA INDICATOR DRIVER
S55EG	SCR SIGNAL ENTRY RESISTOR
S55EH	SCR INDICATOR DRIVER
S55SB	40 MA INDICATOR NETWORK
S55SC	250 MA DRIVER
S55SD	LAMP DRIVER
S60AB	CAM INTEGRATOR
S60AC	CAPACITOR NETWORK
S60AH	SINGLE SHOT FILTER
S60AR	INTEGRATOR
S60BA	JUMPER CARD
S60EA	FILTER 25KC
S60EC	TUNGSTEN CONTACT NETWORK
S60FE	DRIVER FILTER
S60SA	RESISTOR EMITTER LOAD
S60SB	COMPENSATION NETWORK
S60SC	DISK SPEED DETECTOR
S60SD	DECOUPLING CAPACITORS
S60SE	VELOCITY INTEGRATOR
S60SF	LINE FILTER
S60SG	FILTER
S60SH	INTEGRATOR 07 PERCENT SPEED
S60SI	INTEGRATOR LESS THAN 90 PERCENT SP
S61AD	MULTIPLEX TERMINATING NETWORK
S61AF	JUMPER
S61AJ	STANDARD INTERFACE TERMINATOR
S61AM	DISCRETE CAPACITOR
S61AN	2.7K RESISTOR 1/4 W
S61AO	TRANSMISSION LINE RECEIVER
S61AP	TYPE 6V DIODE
S61AR	TERMINATING RESISTOR-100 OHM
S61AU	INTEGRATOR
S61AX	39K RESISTOR
S61AY	PLUGGABLE SWITCH
S61AZ	REED RELAY SUPPRESSION
S61BE	JUMPER
S61BG	200 OHM RESISTOR TO +3V
S61CA	220 OHM RESISTOR
S61CC	TYPE DD DIODE CLAMP
S61CG	THERMISTOR
S61CH	POTENTIOMETER

Circuit Number	Title
S61CM	DEC CAPACITOR +3V
S61CN	DEC CAPACITOR -3V
S61CO	DEC CAPACITOR +66V
S61CP	DECOUPLING CAPACITOR TO +12V
S61CQ	DEC CAPACITOR -12V
S61CR	ISOLATING RESISTOR-1D2
S61CS	200 OHM RESISTOR TO +6V
S61CT	DELAY CAPCACITOR
S61CU	SPECIAL DN LVL IND RESISTOR
S61CW	TYPE AM DIODE TO -12V
S61CX	22 MEG OHM RESISTOR
S61CY	THERMOSWITCH
S61CZ	330 OHM RESISTOR
S61DA	AC INPUT
S61DB	36 OHM RESISTOR
S61DC	TERMINATOR C13
S61DD	5 UF CAPACITOR NP
S61DE	10 UF COUPLING CAPACITOR
S61DF	2.0 KC CRYSTAL
S61DG	DECOUPLING CAPACITOR TO GROUND
S61DH	1.0 UH CHOKE
S61DI	ALS DIODE
S61DJ	CAPACITOR 680PF 5 PERCENT
S61DK	3K RESISTOR
S61DL	MAGNETIC HEAD
S61DM	SOLAR CELL
S61DN	.1 UFD DELAY CAPACITOR
S61DQ	AM DIODE
S61DR	RESISTOR 200 OHM
S61DT	CAPACITOR .02 UF
S61DW	6.8 UFD DECOUPLING CAPACITOR
S61DX	LOAD RESISTOR 95 OHM
S61EA	CAPACITORS I
S61EB	CAPACITORS II
S61EE	PLUGGABLE JUMPERS
S61EK	LOAD RESISTOR -52 OHM
S61EM	100 OHM RESISTOR LOAD TO GND
S61EQ	1 K RESISTOR TO -3V
S61IG	95 OHM TERMINATING RESISTOR TO GRD
S61II	DEC CAPACITOR +12V
S61LA	1 K RESISTOR
S61SO	DIODE MATRIX
S61SA	VERNIER RESISTANCE
S61SC	RESISTOR 14.3 OHM
S61SE	5.1 OHM RESISTOR
S61SF	10 OHM RESISTOR
S61SG	POWER SEQUENCE BLOCK
S61SH	EMITTER LOAD
S61SI	DIODE SUPPRESSION
S61SJ	18 OHM RESISTOR
S61SK	COMMON BAR JUMPER
S61SL	READ-WRITE SELECTION MATRIX
S61SM	PROGRAM CAP HUB
S61SP	DIODE MATRIX
S61SQ	36 OHM 1 WATT RESISTOR

Circuit Number	Title
S61SR	DIODE SUPPRESSION
S61ST	RESISTOR 2.49 K
S61SU	TRACK DIVIDER 2
S61SW	RESISTOR SAFETY
S61SX	CURRENT FEEDING
S61SZ	RESISTOR 21 OHM
S61TA	AC TERMINATOR
S61TB	DECOUPLING CAPACITOR
S61TC	DIODE MATRIX
S61TD	VOLTAGE REGULATOR
S61TE	1.8 K RESISTOR
S61TF	RESISTOR-100 OHM
S61TG	2.4 K RESISTOR
S61TH	RESISTOR 1100 OHM 1/2W
S61TJ	RESISTOR - 1.5K 1/2W 5 PERCENT
S61TK	2K RESISTOR
S61TL	HEAD PLUG-13RK
S61TM	RESISTOR 220 OHM
S61TN	RESISTOR 62 OHM
S61TO	RESISTOR 130 OHM
S61TP	RESISTOR 2 OHM
S61TQ	DIODE CLAMP
S61TR	RESISTOR 25 OHM
S61TS	RESISTOR 1 OHM
S61TT	RESISTOR 825 OHM
S61TU	DIODE SUPPRESSION
S61TV	RESISTOR 1 K
S61UF	DIODE AAS
S63AA	4-POSITION REED RELAY
S63AB	6-POSITION REED RELAY
S63AC	COIL 1-POLE REED RELAY
S63AD	COIL 6-POLE REED RELAY
S63AE	RELAY POINT REED
S63AK	REED RELAY COIL OR 2N/0.2N/C ASSM
S63AL	REED RELAY 2N/0 2N/C
S63AM	REED RELAY HOLD WINDING
S63AN	REED RELAY PICK WINDING
S63AQ	6 N/O P AND H REED RELAY
S63AS	4 N/O P AND H REED RELAY
S63AU	1 POSITION REED RELAY
S63AW	TELEGRAPH RELAY - RECEIVE
S63AY	TELEGRAPH RELAY - TRANSMIT
S63EA	REED POINT-NORMALLY OPEN
S63EB	REED POINT-NORMALLY CLOSED
S63EC	REED RELAY ASSM 2N/0 2N/C
S63ED	REED RELAY ASSM 6V
S63EF	6V COIL FOR REED RELAY
S63EG	REED POINT-NORMALLY OPEN
S63EH	REED POINT-NORMALLY CLOSED
S63SA	COIL-2 POLE REED RELAY
S63SB	COIL 2-POLE REED RELAY
S63SC	COIL 2-POLE REED RELAY
S63SD	48V REED RELAY COIL
S63SE	2 POINT - REED - RELAY
S63SF	4 POINT - REED - RELAY

Circuit Number	Title
S63SG	1-POINT REED RELAY
S63SH	4 POINT RELAY
T03AA	AND INVERT NO LOAD
T03AB	AND INVERT-750 OHM LOAD
T03AC	AND
T03AD	OR INVERT-NO LOAD
T03AE	OR INVERT-750 OHM LOAD
T03AF	AND POWER INVERT NO LOAD
T03AI	EXCLUSIVE OR W/LOAD
T03AJ	AND-PWR INVERT 300 OHM LOAD
T03AK	EXCLUSIVE OR LATCH
T03AL	8 WAY EXCLUSIVE OR
T03AM	4 WAY EXCLUSIVE OR
T03AN	7 WAY API-NO LOAD
T03AO	7 WAY API-300 OHM LOAD
T03AP	EXCLUSIVE OR-NO LOAD
T03AQ	AND FOR MULTIPLEX INTERFACE DRIVE
T03AR	MULTIPLEX INTERFACE DRIVE
T03AS	AND-1K
T03AX	AND EXT MULTIPLEX INTERFACE DR
T03BF	MINUS OR INVERT UNLOADED
T03BN	GATE
T03BO	MINUS OR INVERT LOADED
T03BP	DECODER
T03BQ	SENSE LATCH AND
T03BR	SENSE STROBE AND
T03BS	SENSE AMPL AND
T03BT	EXTENDED API WITHOUT LOAD
T03BV	EXTENDED API
T03BW	EXTENDED API 270 OHM +6
T03BX	SELECTOR
T03BY	GATE DECODER
T03CC	Y-SELECT LOGIC
T03CD	Y-SELECT 2
T03CE	AND GATE
T03CG	AND FOR SENSE AMP LCM
T03CI	POSITIVE OR DIODES
T03CK	TITLE WRITE DRIVER
T03CO	MULTIPLEX RECEIVER
T03CP	OR-INVERT
T03EF	AND FOR API
T03EH	OR INVERT NO LOAD
T03EI	OR INVERT WITH LOAD COMBINED LOGIC
T03EL	AND-OR INVERT NO LOAD
T03EM	AND-OR INVERT WITH LOAD
T03EN	AND-FOR AI
T03JB	SENSE AMPLIFIER AND
T03JC	AND-LATCH CONTROL
T03JD	AND
T03JE	AND
T03JF	OR
T03SA	AND
T03SF	OR INVERTER
T03SG	AND INVERTER

Circuit Number	Title
T03SH	OR DIODES
T03SI	AND INVERTER WITH LOAD
T03SJ	API WITH LOAD
T03SK	SPECIAL OR CIRCUIT
T03SL	AND INVERT
T03SN	POSITIVE AND WITH DELAY
T03SV	REPLACED BY T03SI
T03TB	POSANDEL
T03TC	AOI WITH EXTEND
T03TD	MINUS AND
T03TE	AND EMITTER FOLLOWER
T03TG	DIODE OR
T03TH	STEP MODE OR
T03TI	STEP MODE AND
T03TJ	SEPARATE COMPONENT AI
T03TK	READ SELECT
T03TL	OR INVERTER
T03TM	INVERTER
T03VA	AOI-GROUPING-NO LOAD
T03VB	AOI-GROUPING-W/LOAD
T03VC	MULTIPLEX DRIVER GROUPING-NO LOAD
T05AA	INVERT DIRECT CPLD NO LOAD
T05AB	INVERTER DIRECT CPLD (350 OHM LOAD)
T05AF	NPL FINAL AMP HI + LO ACCEPT DRIVE
T05AJ	TERMINATING EIA TO SLT CONVERTER
T05AL	TRANSLATE BLOCK
T05AM	WRITE DRIVER CHECK
T05AO	45 MA TRANSMISSION LINE DRIVER
T05AP	INTERLOCK CIRCUIT TERMINATOR
T05AO	INVERTER
T05BG	DELAY LINE DRIVER
T05BI	DRIVER STROBE
T05BJ	LAMP TEST CCT FOR DOWN LEVEL ID
T05BK	GATE
T05BM	LATCH STAGE I
T05BN	INVERTER
T05BO	GATE INVERT
T05EA	FINAL AMPLIFIER
T05SA	FORMAT X-READ SELECT
T05SB	DATA X-READ SELECT
T05SC	DIRECT COUPLED INVERTER
T05SD	ISOLATING INVERTER DISCRETE
T05SE	CONVERTER
T05SG	MAGNETIC CB SHAPER
T06AA	LINE SENSE AMP LSA
T06AE	CORE-DRIVER
T06AG	MULTIPLEX LINE TERMINATOR
T06AH	MULTIPLEX INTERFACE DRIVER
T06AI	SLT TO EIA CONVERT LINE DRIVER
T06AJ	DIRECT COUPLED INVERTER DRIVER
T06AL	STD INTERFACE LINE DRIVER
T06AM	GATED LINE INTRFC TERM
T06AN	STD INTERFACE LINE TERMINATOR
T06AR	HIGH POWER DRIVER - 100 OHM LOAD
T06AY	PHASE DETECTOR

Circuit Number	Title
T06AZ	LINE TERMINATOR AND GATE
T06BC	LINE SENSING AMPLIFIER
T06BD	DELAY LINE SENSING AMPLIFIER
T06CE	SENSE AMP TERM C13
T06CF	EMITTER FOLLOWER C13
T06CG	LINE REPEATER
T06CH	LINE TERMINATOR AND GATE II
T06CI	MULTIPLEX LINE DRIVER
T06CJ	LINE DRIVER
T07AD	NPL FINAL AMP PEAK DETECTOR
T07AG	C9 SENSE LATCH 2
T07AH	C9 SENSE AMP 1
T07AI	SENSE AMPLIFIER
T07AJ	PREAMPLIFIER AND FILTER
T07AK	FILTER
T07AS	SENSE AMPLIFIER
T07AT	NPL FINAL AMP INPUT TERM
T07AZ	MAGNETIC HEAD SENSE AMPLIFIER
T07BB	PARAPHASE AMP
T07BC	SENSE AMPLIFIER
T07BD	CCROS RHO SENSE AMPLIFIER
T07BE	CR SENSE AMPLIFIER
T07CA	PROBE AMPLIFIER
T07CB	PROBE AMPLIFIER
T07CF	SENSE AMP
T07CH	SENSE AMPLIFIER
T07CK	SENSE AMPLIFIER
T07CM	MOTION INTEGRATOR II
T07CN	DETECTOR AMPLIFIER 2
T07SA	SUMMING AMP INPUT
T07SB	FUNCTION GENERATOR INPUT
T07SC	LOW LEVEL POSITION AMP
T07SD	LOW LEVEL VELOCITY AMP
T07SG	FUNCTION GENERATOR OUTPUT
T07SH	INNER FUNCTION GENERATOR
T07SI	VELOCITY ARRIVAL BUFFER
T07SJ	TACHOMETER BUFFER AND FILTER
T07SK	COMPLEX ZERO INPUT
T07SL	POSITION ARRIVAL BUFFER
T07SM	CLASS A POWER AMPLIFIER
T07SN	2 SECOND CIRCUIT INPUT
T07SP	SOLAR CELL AMPLIFIER
T07SQ	CYLINDER DETECTOR CIRCUIT
T07SR	INDEX DETECTOR CIRCUIT
T07SS	READ AMPLIFIER 1
T07ST	WRITE AMPLIFIER 1
T07SU	BLOCKING VALVE DET INPUT
T07SW	DETENT DETECTOR CIRCUIT
T07SX	PUNCHCHECK AMPLIFIER
T10BB	SENSE AMPLIFIER
T10BC	DRIVER SUPPLY
T10BE	FORCE CARD PRINT INVERTER
T10BF	LATCH RESET DRIVER 1
T10BG	INVERTER DRIVER
T10BH	GATED INVERTED DRIVER

Circuit Number	Title
T10BI	LATCH RESET DRIVER 2
T10EA	HARPER GATE DRIVER
T10SA	CURRENT CONTROL
T10SC	AMPLIFIER-STROBE DRIVER
T10SF	TRIGGER DRIVER
T10SI	INVERTER
T10SL	INVERTER
T10SN	INVERTER-CLAMPED
T10SP	INTEGRATOR SWITCH
TL0SQ	INVERTER SPEC
T10SR	ISOLATING INV WITH FILTER
T10SS	HIGH POWER INVERTER
T11AB	SA GATE DRIVER
T11BH	SENSE STROBE FOLLOWER
T11BI	EMITTER FOLLOWER
T11BJ	DRIVER
T11BK	RESET DRIVER
T11BL	GATE DRIVER
T11BO	SENSE AMP STROBE DRIVER
T11BP	EMITTER FOLLOWER
T11BQ	EMITTER FOLLOWER
T11BR	EMITTER FOLLOWER
T11BS	EMITTER FOLLOWER
T11BT	EMITTER FOLLOWER
T11BU	EMITTER FOLLOWER
T11BW	EMITTER FOLLOWER
T11EA	STROBE DRIVER
T11EC	CCROS DECODE DRIVER
T11ED	CCROS EMITTER GATE
T11EE	CCROSS GATED DRIVER
T11SA	AND EMITTER FOLLOWER
T15AA	HIGH POWER DRIVER - 175 OHM LOAD
T15AE	HIGH POWER DRIVER-NO LOAD
T15AJ	SOLENOID DRIVER, 1.5A
T15AM	1 POLE REED RELAY DR
T15AN	REED RELAY DRIVER
T15AO	STROBE DRIVER
T15AQ	XY GATE OR INHIBIT DRIVER
T15AT	4 AMP DRIVER NPL
T15AY	HIGH POWER DRIVE-COMBINED LOGIC
T15AZ	434 MA RELAY DRIVER
T15BC	GATE STROBE
T15BD	UP LEVEL INDICATOR DRIVER
T15BE	SENSE STROBE DRIVER
T15BF	DRIVER SUPPLY AMP
T15BG P	DRIVER SUPPLY OUTPUT
T15BH P	SENSE STROBE DRIVER 2
T15BI P	DRIVER SUPPLY AMP 2
T15BJ E	DRIVER DECODER
T15BK P	HIGH POWER INVERT
T15EF P	SONIC LINE DRIVER
T15SH P	BOOTSTRAP AMPLIFIER
T15SJ P	INVERTER
T15SK P	HIGH POWER
T15SL P	450 MA DRIVER

Circuit Number	Title
T15SN P	2.5 AMP DRIVER
T16AF P	S9-WRITE DRIVER
T16AH P	S9-READ DRIVER
T16AI P	A WORD GATE LCM
T16AJ P	SWITCH GATE
T16AK P	A GROUP AND DRIVER
T16AL P	WORD GATE
T16AM E	B SWITCH GATE-LCM
T16AN P	A B GROUP AND LCM
T16AO E	A WORD DRIVER
T16AP P	A GROUP AND CONVERTER LCM
T16AQ P	A GROUP PULSE GEN LCS
T16AT P	WRITE DRIVER
T16AU P	WRITE SAFETY
T16AY E	STROBE DRIVER LCM
T16BB T	DOWN LEVEL INDICATOR DRIVER
T16BC P	CLOCK LINE DRIVER
T16CA P	A GROUP DRIVER- LCS
T16CB E	A WD GATE DRIVER LOAD RESISTOR LCM
T16CC E	B WD GATE DRIVER LOAD RESISTOR LCM
T16CF P	A SWITCH GATE DRIVER- LCM
T16CG P	B SWITCH GATE DRIVER LCM
T16CH P	A WORD GATE DRIVER-LCS
T16CI P	B WORD GATE DRIVER-LCM
T16CJ P	STRIP HIGH DETECTOR
T16CK E	HEAD PRE-AMP
T16CL E	A SHUNT CLIPPER LCM
T16CN E	A COMPENSATION AMPLIFIER LCM
T16CO E	B COMPENSATION AMPLIFIER
T16CT P	BIT GATE CONVERTER LCM
T16CU P	B GROUP AND DRIVER- LCS
T16CW P	B GROUP DRIVER LCS
T16CX P	B GROUP AND CONVERTER LCM
T16CY E	BIT DRIVER
T16CZ P	BIT DRIVER LCM
T16DA P	A EMITTER CLAMP- LCM
T16DB P	B EMITTER CLAMP
T16DC P	A REFERENCE CLAMP LCM
T16DD E	B REFERENCE CLAMP
T16DE E	B WORD DRIVER LCM
T16DG P	S-9 BIT DRIVER
T16DK P	INVERTER FOR C E F
T16DL P	COMP EMITTER FOLLOWER
T16DN E	CURRENT DRIVER
T16DO E	TIMING SWITCH A
T16DP E	A CURRENT GATE
T16DQ E	B CURRENT GATE
T16DR E	VFC DENSITY SWITCHES
T16DS E	WRITE CURRENT CONTROL
T16DT P	SP4 BIT DRIVER
T16DU P	SP4 WRITE DRIVER
T16DW E	LCS BUFFER AND READ BIT RESISTOR
T16DY E	LCS DETECTOR
T16DZ E	LCS FINAL AMPLIFIER
T16IA E	LCS AMPLIFIER INVERTER

Circuit Number	Title
T16IB E	LCM BIT GATE PULL DOWN
T16IC E	TIMING SWITCH B
T16SA P	PHOTO TRANSISTOR AMPLIFIER
T20AB B	400 KC TRIGGER
T20AD T	AC TRIGGER NO. 2
T20AE	HARPER GATE
T20AF	HARPER GATE
T20AG	INTEGRATOR-STROBE
T20AH	S9-LATCH
T20AI	LOGIC TRIGGER
T20AM	AC TRIGGER
T20AR	GATED AC TRIGGER
T20AT	GATED AC TRIGGER
T20AW	GATED AC TRIGGER 2
T20BB	CCROS SENSE CATCH
T20BC	SPECIAL LATCH
T20BD	SPECIAL LATCH
T20EB	400 KC TRIGGER
T20SA	WRITE TRIGGER
T20SC	MULTIPLE INPUT TRIGGER
T20SD	WRITE TRIGGER
T20SE	TRIGGER 2.1
T21AH	NPL FINAL AMP PULSE SHAPER + DR
T21AN	LEADING EDGE TIME DELAY
T21AP	B GROUP PULSE GENERATION PNP-LCS
T21AR	HALF PERIOD GEN
T21AW	SINGLE SHOT-VARIABLE
T21AZ	VARIABLE SINGLE SHOT
T21CC	VARIABLE SINGLE SHOT
T21CF	VARIABLE SINGLE SHOT
T21CH	SINGLE SHOT-FIXED
T21CI	SINGLE SHOT 410 NS
T21CK	250 NS SINGLE SHOT
T21CM	FIXED SINGLE SHOT 1
T21CN	PRECISE SINGLE SHOT ADJ
T21CT	VARIABLE SINGLE SHOT
T21CU	HALF PERIOD GEN 2
T21CW	SINGLE SHOT SSB(VAR) 78NS-68.5US
T21SC	SINGLE SHOT 1400NS
T21SD	SINGLE SHOT 185 NS
T21SE	SINGLE SHOT WITH DELAY
T21SH	500NS SINGLE SHOT
T21SJ	7MS SINGLE SHOT
T21SK	SINGLE SHOT 600 MS
T21SL	300MS SINGLE SHOT
T21SS	SINGLE SHOT
T21ST	SINGLE SHOT 1
T21SU	SINGLE SHOT 2
T21SV	1060 NS SINGLE SHOT
T21SW	300 NS SINGLE SHOT
T21SX	1100 NS SINGLE SHOT
T21SY	VARIABLE SINGLE SHOT
T21TA	110 NS SINGLE SHOT
T21TB	VARIABLE SINGLE SHOT
T21TC	2 MS SINGLE SHOT

Circuit Number	Title
T21TD	10 MS SINGLE SHOT
T21TE	800NS SS
T21TG	15 MS SS
T21TJ	100 NS SINGLE SHOT
T21TK	500 NS SINGLE SHOT
T22AB	2KC OSCILLATOR
T22AC	20KC OSCILLATOR
T22AF	1.667 MC CRYSTAL OSCILLATOR
T22AH	2.4MC XTAL OSC
T22BC	CLOCK OSCILLATOR 3.2 MC
T22BD	170 KC OSCILLATOR
T22EA	2.0MC CRYSTAL OSCILLATOR
T22EB	3 PER CENT 117.2 CPS OSCILLATOR
T22SB	2 MC OSCILLATOR
T22SC	4 MC CRYSTAL OSCILLATOR
T22SD	CLOCK 1.44 MC
T22SE	2.5MC XTAL OSCILLATOR
T22SG	GATED MULTIVIBRATOR
T25AA	NPL FINAL AMP LOW ACCEPT CLIP
T25AB	NPL FINAL AMP HI ACCEPT CLIP
T25AD	REGULATOR 28.5V
T25AG	SENSE LEVEL SET
T25AH	VOLTAGE REFERENCE
T25AL	AB GROUND CLAMP- LCM
T25AM	BASE CLAMP C13
T25BB	SENSE CLAMP PWR AMPL
T25BC	SENSE CLAMP
T25BD	+3V CLAMP
T25BE	SENSE CLAMP PWR AMP
T25BF	SENSE CLAMP PWR AMP
T25BG	OVER VOLTAGE LIMITER
T25EE	SIGNAL DETECTOR
T25EF	GATE CLAMP
T25EH	DELAY LINE DETECTOR
T25SB	CURRENT CONTROL
T25SC	CURRENT VOLTAGE
T25SD	OFFSET VOLTAGE
T26AA	NPL FINAL AMP LO ACCEPT CLIP
T26AB	NPL FINAL AMP HI ACCEPT CLIP
T27BB	SENSE CLAMP POWER AMP
T27BC	SENSE CLAMP
T27BD	+3 V CLAMP
T30BC	PUNCH MAGNET DRIVER GROUPING
T31BC	CHANGE OVER SWITCH
T31BD	3-WAY CHANGE OVER
T31BE	LAMP TEST SWITCH
T32AF	NPL FINAL AMP GATE
T32AH	CORE-GATE
T32BA	LINE RECEIVER GROUPING
T32BD	THRESHOLD GATE
T32BE	LATCH STAGE II
T32BF	GATE
T32EB	TRIGGER GATE
T32SA	ARRIVAL DETECTOR

Circuit Number	Title
T32SC	ARRIVAL-CAPACITOR AND GATE
T32SF	HOME DRIVER AND
T32SG	INTEGRATOR RESET
T32SH	CE RUN
T32SI	DETENT DRIVER
T40AA	NPL FINAL AMP RECT + CHAN SEP
T40AB	NPL FINAL AMP .9V ZENER SUPPLY
T40AE	LIMIT AMPLIFIER
T40AF	INDEX PULSE AMPLIFIER
T40AG	FORMAT SELECT
T40AH	8 POSITION CLOCK
T40AI	6 POSITION COUNTER
T40AJ	DIFFERENTIAL AMP FOR SENSE AMP LCM
T40AK	VFC PULSER
T40AL	VARIABLE FREQUENCY CLOCK
T40AN	VARIABLE CURRENT SOURCE
T40AP	SA GATE GENERATOR
T40AR	VARIABLE FREQUENCY CLOCK 2
T40BB	BUFFERED SENSE LATCH
T40SA	CONSTANT CURRENT LAMP SUPPLY
T40SB	CURRENT SOURCE
T40SC	SUMMING AMP CURRENT SOURCE
T40SD	WRITE BYPASS
T40SE	DIFFERENTIATOR
T40SG	POWER SUPPLY SAFETY +6 V
T40SH	BLOCKING VALVE DET. OUTPUT
T40SI	SINGLE SHOT 750 USEC
T40SJ	CURRENT CONTROL
T40SK	SENSE LEVEL
T40SL	REFERENCE VOLTAGE
T45AC	125 NS DELAY LINE
T45AF	15 SECOND DELAY
T45AG	250 NSEC TAPPED DELAY LINE
T45AH	500 NSEC DELAY LINE TAPPED
T45AL	MOTOR DELAY CIRCUIT
T45BB	VARIABLE DELAY LINE
T45BC	CLOCK DELAY
T45EC	200 NS DELAY CIRCUIT
T45ED	350 NS DELAY LINE
T45LC	RC DELAY CIRCUIT 250 NS
T45LD	RC DELAY CIRCUIT 440 NS
T45LE	RC DELAY CIRCUIT 160 NS
T45LG	RC DELAY CIRCUIT 2.1 S
T45LH	RC DELAY CIRCUIT 500 MS
T45LI	RC DELAY CIRCUIT 176 MS
T45SA	DELAY FILE READY
T55AA	INDICATOR COUPLING NETWORK
T55AB	ICN-LAMP
T55AC	INDICATOR LAMP-3V
T55AD	15MA SWITCH ID NO LOAD
T55AH	40 MA IND DRIVER UNLOADED
T55AI	40 MA INDICATOR DRIVER
T55AM	15 MA INDICATOR DRIVER
T55AN	15 MA INDICATOR DRIVER WITH NETWORK
T55BB	INDICATOR

Circuit Number	Title
T60AA	50V DECOUPLING NETWORK
T60AB	20V DECOUPLING NETWORK
T60AI	+48V INTEGRATOR
T60AJ	20V INTEGRATOR
T60BF	SWITCH INTEGRATING NETWORK
T60SA	AC WRITE CURRENT INT
T60SE	INTERGRATOR
T61AA	750 OHM LOAD RESISTOR
T61AB	750 OHM LOAD RESISTOR
T61AC	350 OHM LOAD RESISTOR TO +3V
T61AD	LINE TERMINATOR NETWORK
T61AG	BIT GATE CONVERTER LOAD RESISTR LCM
T61AJ	300 OHM LOAD RESISTOR TO +3V
T61AK	750 OHM RESISTOR
T61AM	630 OHM LOAD RESISTOR
T61AN	LOAD RESISTOR-232 OHMS
T61AO	NPL FINAL AMP INPUT TERMINATOR
T61AP	100 OHM TERMINATING RESISTOR
T61AW	100UH INDUCTOR TO -3V
T61AX	160 OHM RESISTOR TO +3V
T61BD	DRIVER DAMPING NETWORK
T61BE	DRIVER COLLECTOR LOAD
T61BF	DRIVER EMITTER LOAD
T61BG	130 OHM TO + 3V
T61BI	RESISTOR COMB
T61BJ	DELAY LINE TERMINATOR
T61BK	RESISTOR 759 OHM TO -3V
T61BL	100 OHM TO +3V
T61BM	220 OHM TO +3V
T61BN	300 OHM TO +3V
T61BO	RESISTOR 300 OHM TO -3V
T61BP	RESISTOR 1.8K TO -3V
T61BR	180 OHM RESISTOR TO +3V
T61BS	SELECTOR DECOUPLING NETWORK
T61BT	DRIVER COLLECTOR LOAD
T61BU	DECOUPLING NETWORK A
T61BV	DECOUPLING NETWORK B
T61BW	+12V MARGINAL POWER SUPPLY
T61BX	110 OHM TO +3V
T61BY	180 OHM TO +3V

Circuit Number	Title
T61BZ	120 OHM TO +3V
T61CC	430 OHM TO +6M
T61CF	FDD
T61CG	TYPE DD DIODE
T61CH	TYPE DE DIODE
T61CK	RESISTOR-CHOKE
T61CL	175 OHM TO +3V
T61CN	BIASING NETWORK
T61CR	WRITE BIT RESISTOR-LCM
T61CS	TYPE DO DIODE SUPPRESSOR
T61CV	TYPE DE DIODE
T61CW	HPD LOAD RESISTOR
T61CY	1.175K LOAD RESISTOR
T61CZ	2K POTENTIOMETER
T61DA	750 OHM TO +3V
T61DC	100 OHM LINE TERMINATING TO +3V
T61DD	MAGNETIC HEAD DIFFERENTIATOR
T61DE	BIT GATE DIODE LCM
T61DF	RESISTOR 38.3 OHM
T61DG	BIT GATE CONVERTER LOAD RESISTOR
T61EA	600 OHM RESISTOR LOAD TO +6V
T61EE	164 OHMS TO -3V
T61EF	820 OHM RESISTOR TO +6V
T61JB	680 OHM TO +6V
T61JD	240 OHM TO -3V
T61JE	+ 6V DECOUPLING NETWORK
T61SB	DETENT LEVEL SETTER
T61SC	CYLINDER A.C. LEVEL SETTER
T61SD	INDEX LEVEL SETTER
T61SE	51 OHM RESISTOR TO -3V
T61SJ	R.C. FILTER
T61SN	130 OHM RESISTOR TO +6V
T61SQ	BIASING NETWORK
T61SS	SINGLE STEP DIFFERENTIATOR
T61ST	RESISTOR 2K
T63AA	COIL FOR 6 CONTACT REED RELAY
T63AB	POINTS FOR 6 CONTACT RR
T63AC	6 CONTACT REED RELAY
T66AA	NPL FINAL AMP PULSE SHAPE AND DR

IBM Location Manufacturing Practice

INTRODUCTION

1.1 SCOPE: This practice presents the Logic Block Symbols for Solid Logic Design Automation Systems.

1.2 OBJECTIVE: The intent of this document is to provide design output of a consistent uniform nature.

1.3 DEVIATION APPROVAL: Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

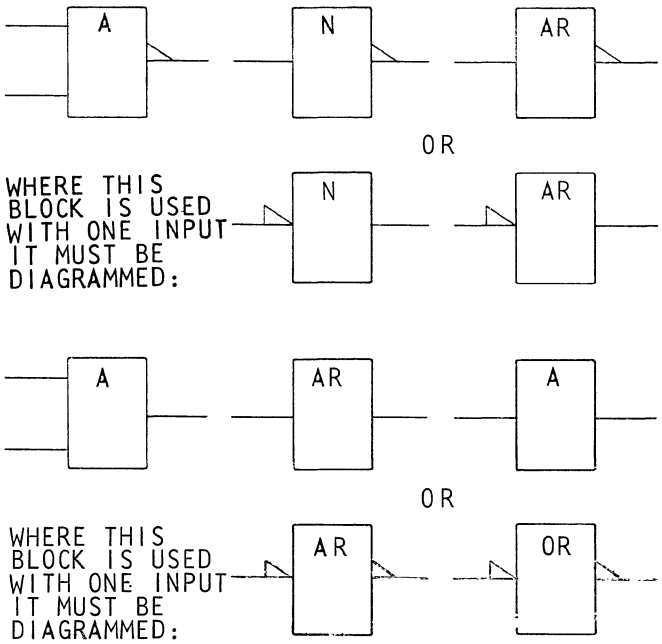
RECOMMENDED PRACTICES

2. INPUTS

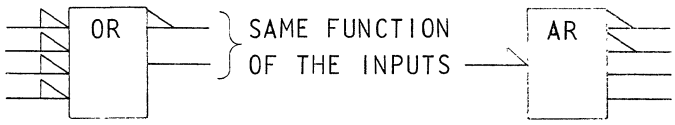
2.1 Entry To Symbol. No input shall enter a symbol in the vicinity of an output or on the output side of a symbol, except as provided in Paragraph 3.4.

2.2 AND or OR Block. An AND or OR block must have at least two inputs unless it is being used as one of the blocks in an EXTENDER arrangement. (See Paragraph 3.4.)

2.2.1 Exception. An exception shall be allowed in the ALD's for those cases where only one input of a multiple input device is used to gain entrance to the adjacent circuit within a standard unit, i.e., one diode of the AND device is used to gain entrance to the OR device with an AND, OR, INVERT configuration.



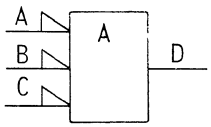
2.3 MULTIPLE OUTPUTS are allowed from logic blocks, provided that each of these (polarity as indicated) is the same function of the input(s) as specified by the block function label.



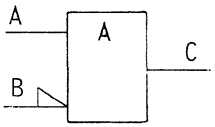
3. LINE SYMBOLS

3.1 1-STATE (ACTIVATED). A small, open, right triangle at the point where a signal line joins a logic symbol indicates that the line's 1-state (activating) is the less positive potential.

3.1.1 Omission of Symbol. Omission of the triangle indicates that the line's 1-state (activating) is the more positive potential.

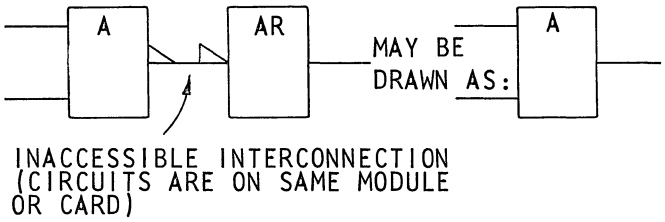


(A) AND (B) AND (C) MUST ALL BE IN THEIR LESS POSITIVE CONDITION FOR (D) TO BE IN ITS MORE POSITIVE CONDITION

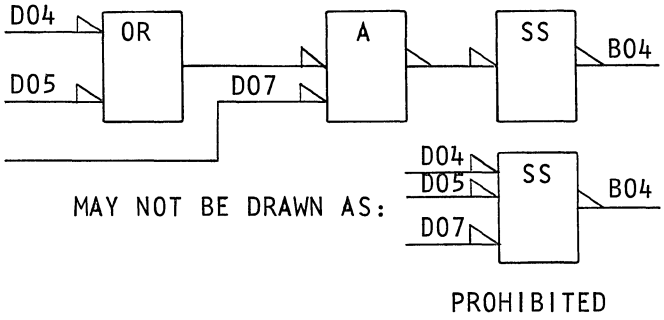


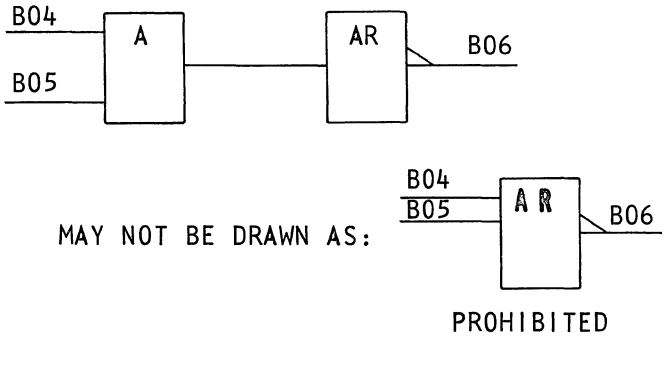
(A) MUST BE IN ITS MORE POSITIVE CONDITION AND (B) IN ITS LESS POSITIVE CONDITION FOR (C) TO BE IN ITS MORE POSITIVE CONDITION.

3.1.2 The A (AND) and AR (AMPLIFIER) symbols may, as packaging allows, be combined into the one (A) (AND) symbol.

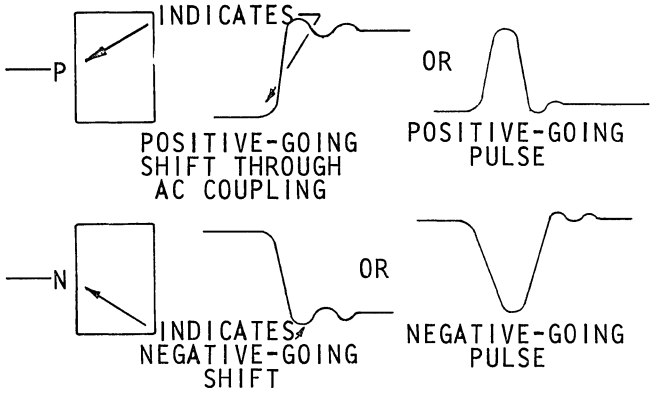


3.2 BLOCK LINE POSITION OR GROUPING shall not be used to denote any of the basic logic functions shown in this standard. (See Paragraph 4.1). Neither shall block line position be used to denote any parameter of the signal such as polarity, pulse length, shift, amplitude, timing, etc. It will be noted that the use of line position to identify a particular lead, such as on a FLIP FLOP, is not a violation of this paragraph.

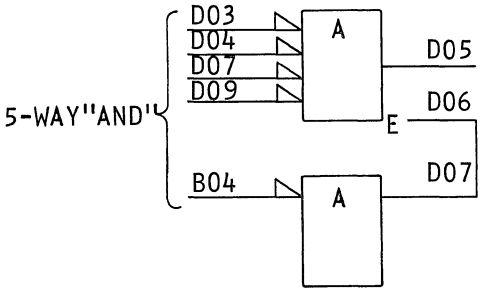




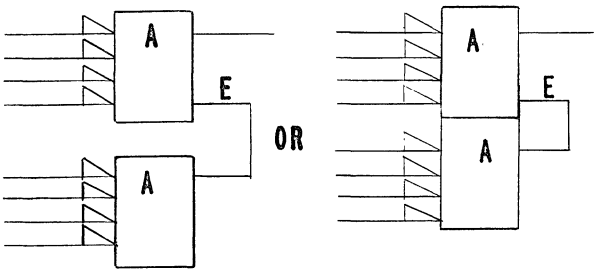
3.3 AC COUPLING at an input of a logic block shall be shown by a P or an N at the place normally occupied by the polarity indicator according to the conventions shown below.



3.4 USE OF EXTENDER. When a circuit is used to add inputs to another AND or OR circuit, and the connection from the second circuit to the first is made at other than a normal input or output of the first circuit, the connection shall be shown without polarity and labeled E (for EXTENDER). The "E" shall be placed at the block whose inputs are being extended.

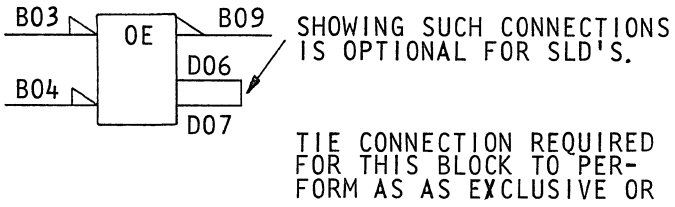


These blocks shall be vertically butted to conserve space.

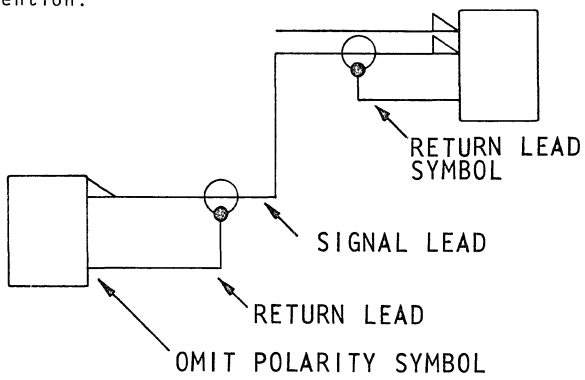


3.5 Handling of Tie-Downs and Return Leads

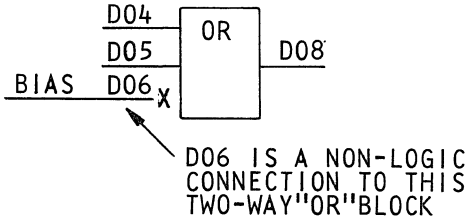
Certain pins of a block other than logic inputs and outputs must be tied together in order for the block to perform its function as indicated. The pins and connection shall be shown on other than an input side of the block.



A signal line that connects one block with another requires a separate return lead. This may shown by giving the pin number of the return lead directly under that of the signal line to which it pertains and omitting the line corresponding to the return lead itself. The relationship of these leads shall be further denoted by the following diagram convention:



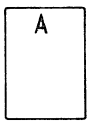
3.6 NON-LOGIC CONNECTIONS to a logic block shall be marked with an X at the place normally occupied by the polarity indicator. Examples of non-logic connections: voltage, bias, feed back, shield lines and other connections shown at the block but which do not affect the logic function of the block.



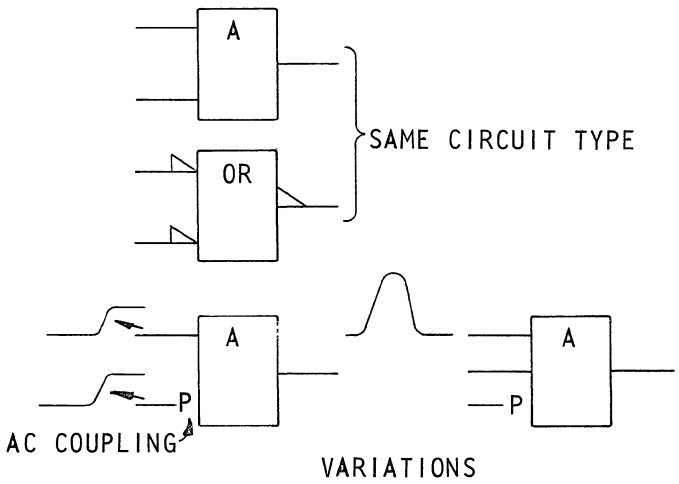
4. DEFINITIONS

4.1 A COMPLETE LISTING OF BASIC BLOCKS AND FUNCTION SYMBOL DEFINITIONS. A device may have more than one acceptable function symbol (possibly affecting line polarity indication). This is shown in the illustrations by identifying different blocks as "same circuit type." The number of inputs and outputs may vary in some of the devices. Blocks shown as variations are not intended to be inclusive.

4.1.1 AND. This is a device whose output will stand at its indicated polarity when and only when all of the inputs stand at their indicated polarities. Paragraphs 4.1.1.1 and 4.1.1.2 are the more common types.



4.1.1.1 Positive AND. The output of the Positive AND is in its more positive condition when and only when all of the inputs are in their more positive condition.



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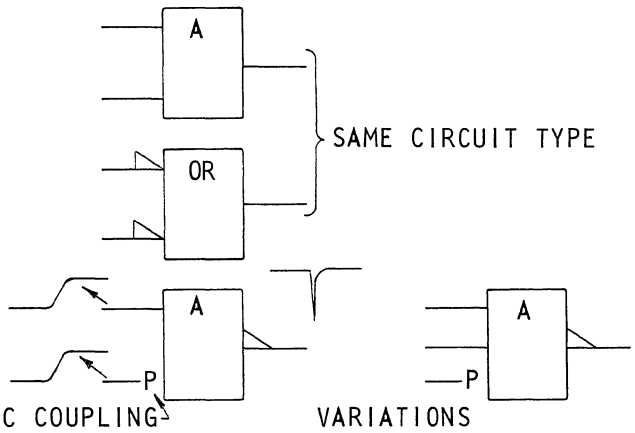
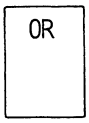
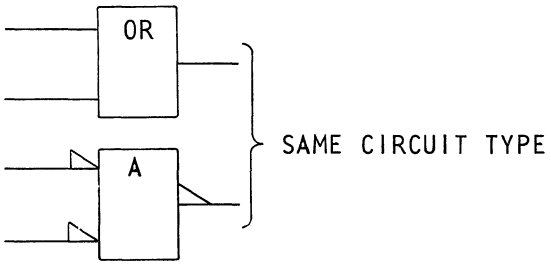
4.1.1.2 Positive AND INVERT. The output of the Positive AND INVERT is in its more negative condition when and only when all of the inputs are in their more positive condition.



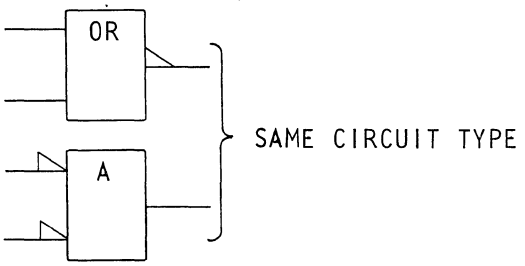
4.1.2 OR. This is a device whose output will stand at its indicated polarity when and only when one or more of its inputs stands at its indicated polarity. Paragraphs 4.1.2.1 and 4.1.2.2 are common types.



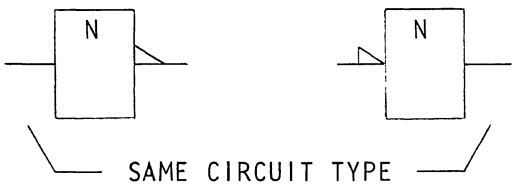
4.1.2.1 Positive OR. The output of the Positive OR is in its more positive condition when and ony when one or more of the inputs are in their more positive condition.



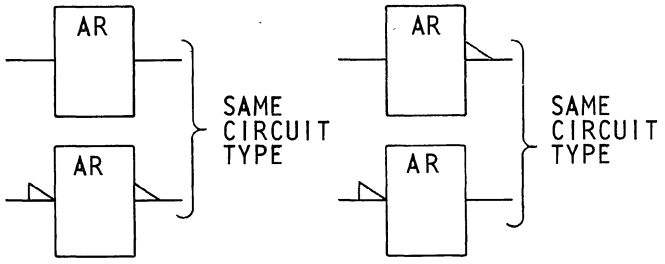
4.1.2.2 Positive OR INVERT. The output of the positive OR INVERT is in its more negative condition when and ony when one or more of the inputs are in their more positive condition.



4.1.3 INVERTER. This is a device whose input is in the more positive condition as a result of its input being in the more negative condition and vice-versa. It shall be drawn in one of two ways only: with negative polarity indicated at the input and positive at the output, or vice-versa. An inverter can have no more than one logic input (a return lead or shield connection is not considered a "logic" input).

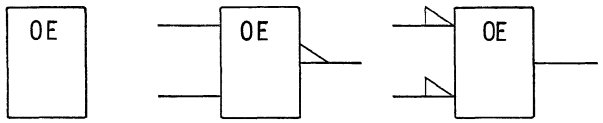


4.1.4 AMPLIFIER. This is a device whose fundamental purpose is to provide adequate driving energy and appropriate impedance matching to other devices. Its output will be at its indicated polarity when and only when its input is at its indicated polarity. An AMPLIFIER can have no more than one logic input. (More than one physical input may be necessary, for example a return lead or the other lead of a differential input).



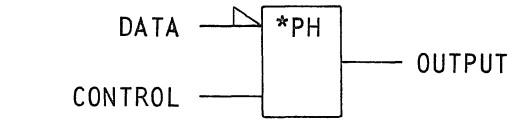
4.1.4.1 Non-Standard Logic Signal Voltage. An AMPLIFIER having input or output of other than standard logic signal voltage shall be made recognizable through labeling at the block.

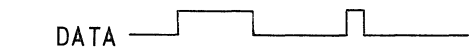
4.1.5 EXCLUSIVE OR. The output of an EXCLUSIVE OR will be at its indicated polarity when one and only one of its inputs is at its indicated polarity.

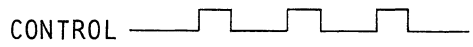


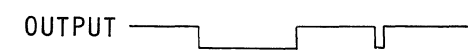
VARIATIONS

4.1.6 The Exclusive OR Latch has a single bistable output that can be changed by proper sequencing of the control and data inputs.









4.1.6.1 Sequence of Operation:

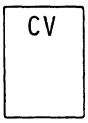
1. Control is normally down. The Latch output will be set to the compliment of the data input on the control rise.

   (a) Data line up - with the control rise, the output will be set to (0) state. All further changes in the control line will not affect the state of the latch, if the data line is unchanged.
   (b) Data line down - with the control rise, the output will be set to the (1) state. All further changes in the control line will not affect the latch state, if the data line is unchanged.

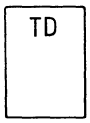
2. Control is normally up. The latch output will change with changes in the data line. Information is stored on the control fall. If the control line remains down after the control fall, changes in the data line will not affect the latch state.

   (a) Data line up - with the clock fall, the output will be held in (0) state.
   (b) Data line down - with the clock fall, the output will be held in (1) state.

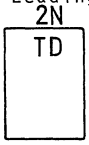
4.1.7 SIGNAL MODE CONVERTER. This is a device that provides the necessary conversion or translation between signal lines having different signal reference values - current mode to voltage mode, voltage mode to voltage mode, etc. Where these reference values are, in fact, current or voltage levels then a numeric indication of such values shall be given in the title area. (See Paragraph 4.9).



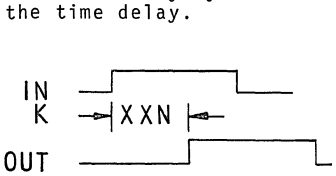
4.1.8 TIME DELAY. This is a device whose primary function is the time delay of a signal without intentional distortion of the signal. The TIME DELAY symbol must always be accompanied by its time delay, which is shown in the 14 character block title. (See Section 5).

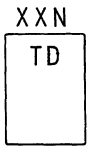


4.1.9 TIME DELAYS. The time duration is indicated in the 14 character title, followed by N, U, M, or S to denote nano, micro, milli seconds or seconds respectively. Leading blanks are permitted.



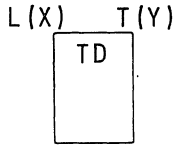
The time delay symbol must always be accompanied by the time delay.



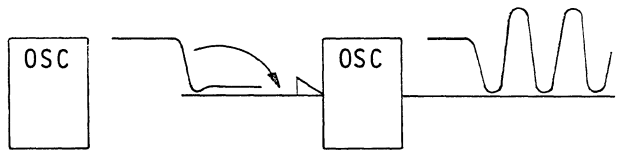


Time delays having a delay time for the leading edge of the output that is different from the time delay for the trailing edge shall be identified by the placement of an L for leading and a T for trailing immediately prior to the separate delay times in the block area. The input polarity at the block must be that associated with the "leading" edge of the output.

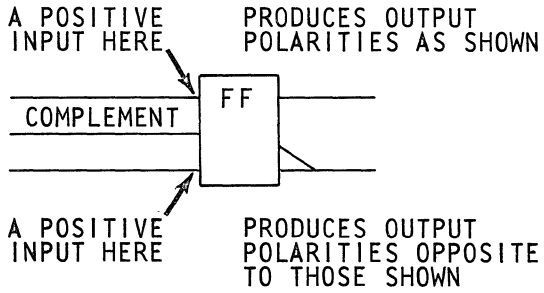
4.1.10 Unequal Leading and Trailing Delay. TIME DELAYS having a different delay time for the leading edge of the output than for the trailing edge shall be identified by the placement of a "L" for leading and a "T" for trailing immediately prior to the separate delay times in the block title area. The input polarity shown at the block must be that which is associated with the "leading" edge of the output.

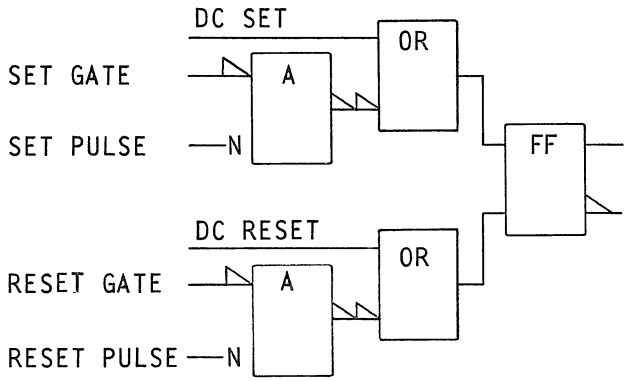


4.1.11 OSCILLATOR. This is a device which produces a uniform repetitive output either continuously or during the application of an input signal of the polarity indicated. It is desirable to show the frequency in the block title.



4.1.12 FLIP FLOP. This is a device which has two stable states. One of these is called the 1-state or set state, the other is the 0-state or clear state. The device normally has two outputs, a 1 output and a 0 output. In the ALD's a line from the upper part of the block will be assumed to be the 1 output and a line from the lower part of the block will be assumed to the 0 output. The FLIP FLOP is in the 1 state when its 1 output (the upper output on the ALD)is at its indicated polarity. Regardless of the condition of its inputs, the 1 output and 0 output of a FLIP FLOP in its stable state are always opposite in polarity. The polarities show at the inputs and outputs of a FLIP FLOP of a particualr circuit type are unchanging parts of the symbol itself.





FLIP FLOP WITH INPUT AND'S AND OR'S

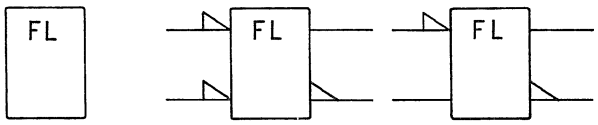
4.1.12.1 Operation.

(a) Application of a signal of indicated polarity to the line opposite the 1 output will cause the outputs of the block to assume their indicated polarities.

(b) Application of a signal of indicated polarity to the line opposite the 0 output will cause the outputs to assume polarities opposite to those indicated.

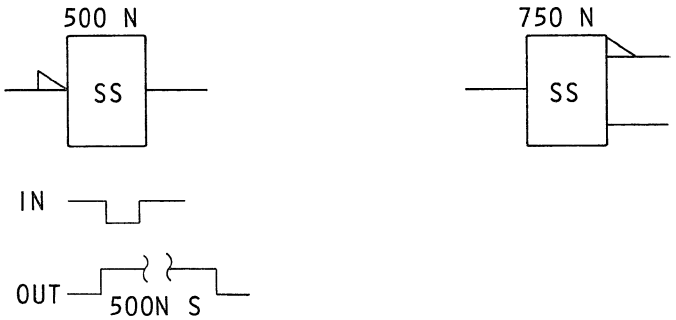
(c) Application of a signal of indicated polarity to a line centered between the two lines already mentioned, or to both the set and clear inputs simultaneously, will change the state of the FLIP FLOP (complement the FLIP FLOP).

4.1.13. FLIP FLOP LATCH OR FLIP LATCH. The definition of this device is the same as that given for FLIP FLOP except that simultaneous application of signals of indicated polarity at the 1 input and the 0 input will cause the 1 output and 0 output to both go to the negative polarity or both go to the positive polarity (depending upon the characteristics of the particular circuit type) for the duration of such simultaneous input application. Complement input is not applicable to this block.

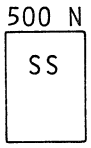


VARIATIONS

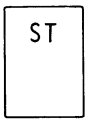
4.2 SINGLESHOT. The output of the singleshot changes temporarily to the indicated polarity when it reaches an input signal of the indicated polarity. The output remains in this quasi-stable state for a time characteristic of the particular block. The singleshot always has the time duration shown in the title area of the block. If a singleshot has more than one output not of the same duration, the block will be labeled or a reference note on the page will relate pin numbers to time durations.

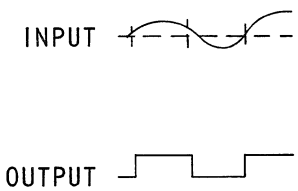


4.2.1 SINGLE SHOT. The time duration of the quasi-stable state is followed by N, U, M, or S to denote nano, micro, milli seconds, or seconds respectively. Leading blanks are permitted.

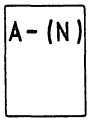


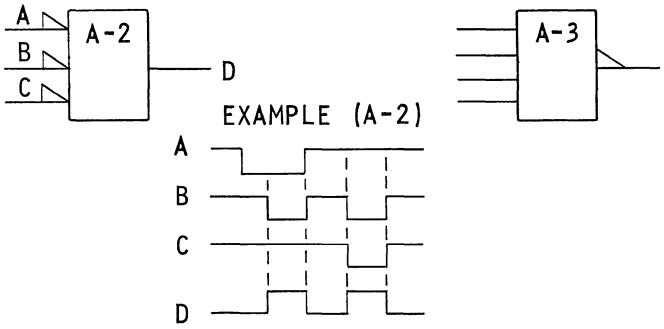
4.3 SCHMITT TRIGGER. The output of the Schmitt trigger goes to its indicated polarity whenever the input crosses the threshold in the direction of the indicated polarity. The output remains at this indicated polarity until the input signal crosses the threshold in the opposite direction.





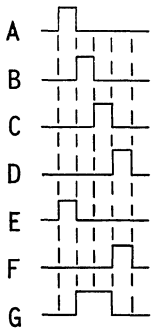
4.3.1 THRESHOLD. This a device whose output will be at its indicated polarity when and only when the number of its inputs which stand at their indicated polarity reaches or exceeds the number specified in the function symbol. This symbol shall also be used where an input may have greater weight than 1 in the determination of the threshold. In such case this input shall be suitably titled with a number which denotes the particular weighting factor. The number specified in the A-(n) symbol may not be 1 nor may it be equal to the total weighted value of the inputs.

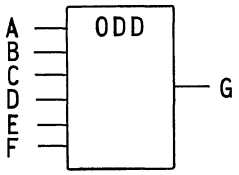




4.4 ODD Count. The output of odd count (ODD) is at its indicated polarity when, and only when, an odd number (1, 3, 5, 7, etc.) of inputs are at their indicated polarity.

NOTE: An ODD may be shown as an even count (EVEN) through proper change in polarity indication, and vice-versa. There is a simular relationship in the AND and OR circuits.



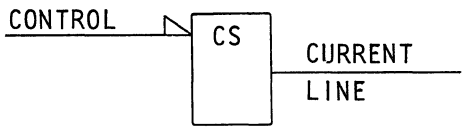


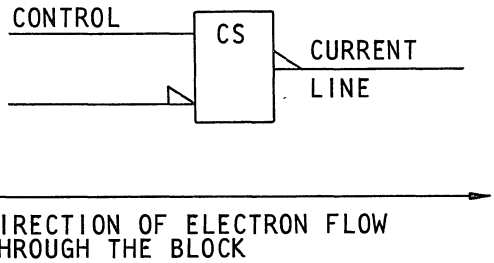
4.4.1 EVEN Count. The output of even count is at its indicated polarity when an only when an even number (0, 2, 4, 6, etc.) of inputs are at their indicated polarity.

As noted earlier an EVEN may be shown as an ODD through proper change in polarity indication, and vice versa. This change may be compared to the AND and OR circuit.

4.5 CURRENT SWITCH. Under some circumstances, it is difficult to describe the logic operations of AND'ing and OR'ing in the standard block symbols because of the use of series control of current flow, e.g., handling the drive currents in a magnetic core array. At times the purpose of a circuit is to allow a flow of current (either in or out) under logic voltage control. When this condition exists, the circuit cannot cause the current to flow solely through electrical action at its own logic input. Because of the series flow of this current through other controlling circuits, the circuit may be given the function label CS (current switch).

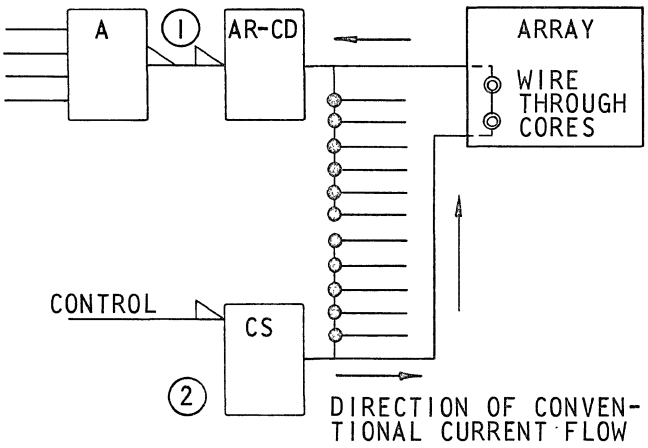
The control input of the CS is placed towards the top of the block. Sending a signal of indicated polarity to this input allows (not necessarily causes) the flow of current through the block in the direction indicated by the polarity symbol located at the output side of the block (on the current line). A negative polarity symbol, for example, indicates electron flow away from the output side. A line opposite the output line is assumed to be the same current line, separated by the circuitry of the CS. The polarity indication for this line is the same as that of the corresponding output line.





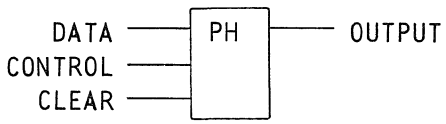
4.5 Contd.

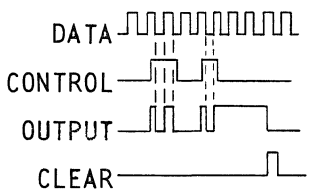
The accompanying illustration shows the use of the current switch in the control of a series flow of current through more than one circuit. A negative signal at (1) causes current to flow in the array, provided the control signal is negative at (2).



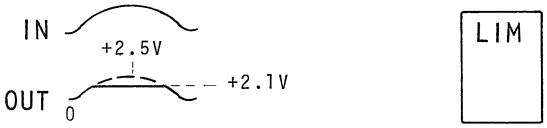
4.6 POLARITY HOLD. The output of this block is at the indicated polarity whenever the data line is at its indicated polarity and the control line is at its polarity. When, at a particular moment in time, the control input goes to the polarity opposite to that indicated, the output remains at whatever polarity it possesses at that moment. The PH block may have a clear input. If so, when the clear polarity is at its indicated polarity, the output will be opposite of its indicated polarity.

The output line is located towards the top of the block. The data line is opposite the output line. The control line is centered on the input side of the block. The clear line is located towards the bottom of the block.

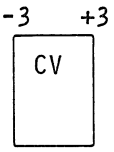




4.7 LIMITER. The limiter block sets one or both extremes of a wave-form to a predetermined level without intentional distortion of the remaining waveform.



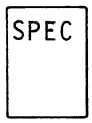
4.8 CONVERTER. The converter block provides the necessary conversion or translation between two types of logic, i.e., voltage mode to current mode, voltage to voltage, etc. An indication of input voltage levels, or line types, is shown in the block title area of the block.



4.9 SPECIAL BLOCKS. Two conditions must exist for a block to be designated as special:

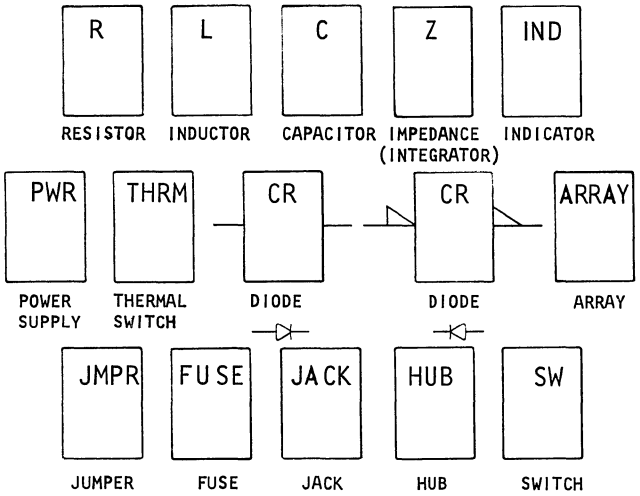
1. The function is not covered by any single block symbol.
2. The function cannot be expressed in terms of an interconnected set of individual block symbols.

The function of a special block is described by the wording on the ALD, located either at the block or in a comment area referenced by a note in the title area of the block.

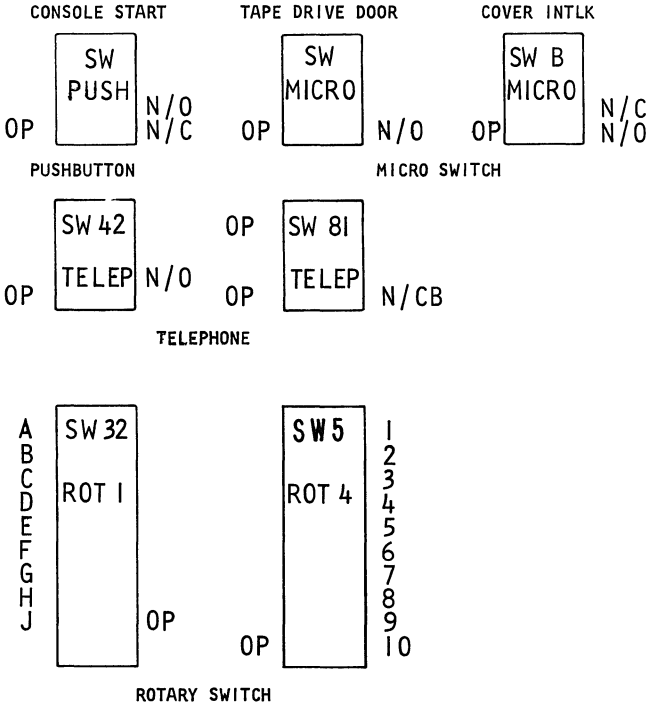


4.10 COMPONENT AND AUXILIARY BLOCKS. Many types of components may be mounted on an SLT card. The following examples are typical (but not all-inclusive) of these components.

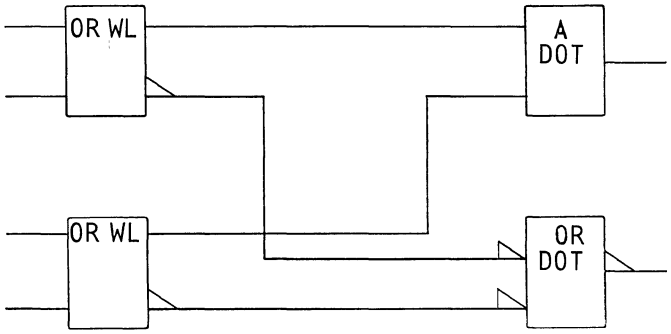
4.10.1 COMPONENT BLOCKS



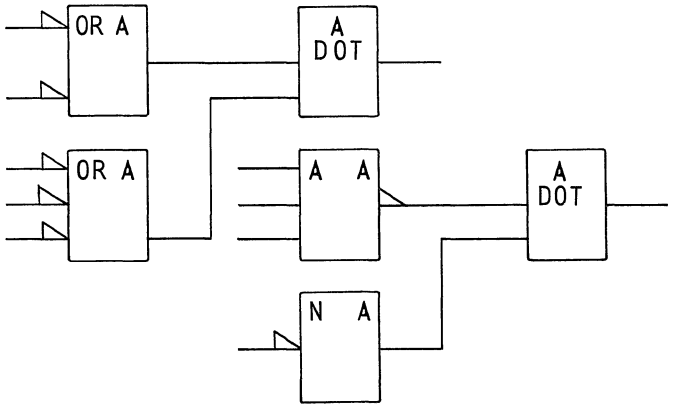
4.10.2 SWITCH BLOCKS



4.10.3 WIRED LOGIC. When the output of a block enters into both a DOT OR and a DOT AND operation the letters WL (for WIRED LOGIC) shall be placed to the right of the primary block function symbol.

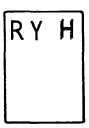


4.10.4 DOT OR and DOT AND. Basic function whose outputs are connected externally so that the connection performs an AND or OR operation (dot AND, dot OR) shall be identified by having an additional A or OR placed in the block to the right of the primary block function symbol. Suffix must match the logic function shown at the DOT block. In the ALD's a block labeled OR DOT or AND DOT will be used to form the junction of lines being joined in this manner. All input and output polarity indications at the DOT block must be identical and the function of the DOT A or DOT OR must agree with the AND and OR definitions as described in Paragraph 4.1.1 and Paragraph 4.1.2 respectively.

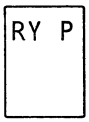


4.10.5 RELAY COIL AND CONTACTS. These representations pertain to relays. One set of contact points per block is preferred.

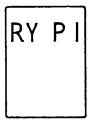
4.10.5.1 HOLD COIL



4.10.5.2 PICK COIL

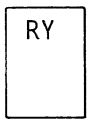


4.10.5.3 PICK 1 COIL

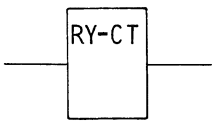


4.10.5.4 RELAY

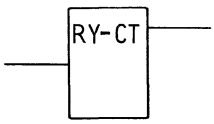
4.10 5.5 SINGLE COIL



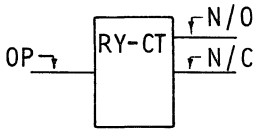
4.10.5.6 N/C POINT: OUTPUT LINE MUST BE OPPOSITE INPUT LINE.



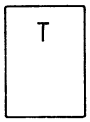
4.10.5.7 N/O POINT: OUTPUT LINE MUST BE ABOVE INPUT LINE



4.10.5.8 TRANSFER POINT

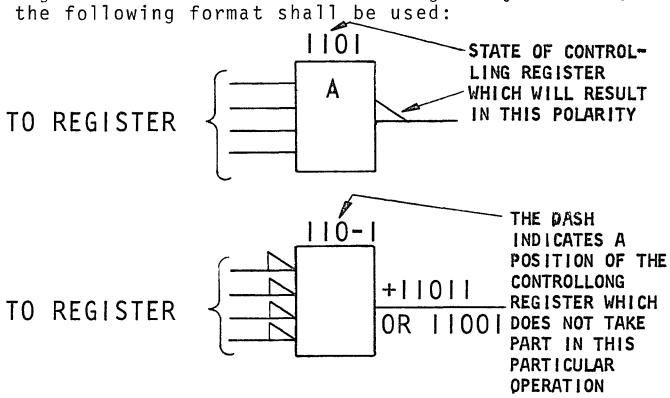


4.10.5.9 TRANSFORMER



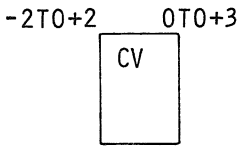
5. BLOCK TITLES

5.1 BLOCK TITLE = REGISTER STATUS. Where it is desired to have the title of a block pertain in terms of a binary number to the status of a particular register to which the block is logically related, the following format shall be used:



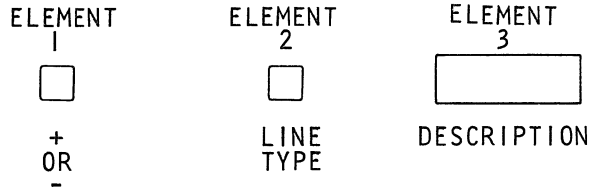
5.2 SPACE. If the block operation cannot be adequately described in the 14 character block title, use "NOTE" in the block title area and comment in the note section.

5.3 SIGNAL MODE CONVERTER. Input and output signal mode parameters shall be defined as in Paragraph 4.1.7.



6. LINE TITLES

6.1 GENERAL FORMAT FOR ALL LINES ENTERING OR LEAVING A DIAGRAM PAGE. All lines which enter or leave a diagram page shall conform to the following general format:



Printed in U.S.A.

6.1.1 Element 1. The + or - symbol in element 1 refers solely to the relative level of the signal line with respect to its title. For example, the + symbol indicates that for the title condition, the line will stand at the more positive of its two possible states. The + or - symbol should generally match the output polarity indication shown on the source block.

6.1.1.1 Element 1 Exceptions. An exception will be allowed for those machines in which active (1-state) polarity is predominately of one type which will be obvious from the line polarity symbols. In these cases element 1 shall be required on all lines which do not conform to the predominate polarity.

6.1.2 Element 2 refers to the physical characteristics of the signal line which control its logic state. Where this is in terms of voltage, numeric values shall be indicated.

6.1.2.1 Element 2 Exceptions. Where the line type within a machine is predominately the same, element 2 may be omitted for those line types. Its use will then denote the exceptional condition. When the unit of measurement of element 2 denotes voltage, the abbreviation for voltage may be ommitted. However, the unit of measurement for any other parameter must be shown. See Paragraph 6.1.2.2.

6.1.2.2 Indication of Line Type in Line Titles. Where a design group chooses to follow paragraph 6.1.2 without exception, the following line title format is recommended:

(a) For lines whose voltage swing is that of the predominate type within the machine:
Show element 1 (+ or - symbol) followed by the nominal voltage which corresponds to that polarity.

EXAMPLES:
(1) +3 L REG BIT 6
(2) -0 WRITE ERROR
(3) + -6 TRANSFER A TO B
(4) - -12 CLEAR B REG

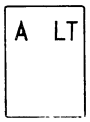
(b) For lines whose voltage swing does not conform to the predominate type:
Show element 1 (+ or - symbol) followed first by the nominal voltage which corresponds to that polarity, then by the voltage which corresponds to the other polarity. The latter voltage must be bracketed by "X's."

EXAMPLES:
(1) + -4 X-14X TEST INTERLOCKS
(2) -14 X-4X SET HOLD CONDITION

6.1.3 Suffixes.

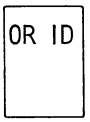
(a)	LT	transmission line terminator	
(b)	LD	transmission line driver	
(c)	ID	indicator driver	
(d)	CD	core driver	
(e)	HD	magnetic head driver	
(f)	MD	magnet driver - relay, clutch, solenoid, etc.	
(g)	V	voltage amplifier	
(h)	DF	differential amplifier	
(i)	FF	flip flop	used for emphasis of
(j)	FL	flip flop latch	storage elements whose
(k)	PH	polarity hold	elements must exist in multiple block form.
			used in the identification of blocks whose outputs are connected in the DOT AND or DOT OR arrangement. These suffixes take precedence over all others.
(l)	OR	or	Where a sufix which de-
(m)	A	and	notes DOT AND or DOT OR
(n)	WL	wired logic	supplants a suffix which would normally be separated from the primary function symbol by a dash (see above) the displaced suffix shall be placed above the block in the title area.
(o)	P	pick	used with the relay
(p)	H	hold	block (IRY) to denote
(q)	CT	contact	coil and contact.
(r)	LR	line receiver	

6.1.4 EXAMPLES: Some possible uses of the suffix are shown below:



"AND" CIRCUIT BEING USED AS A TRANSMISSION LINE TERMINATOR

RELAY DRIVER



"OR" CIRCUIT USED AS AN INDICATOR DRIVER

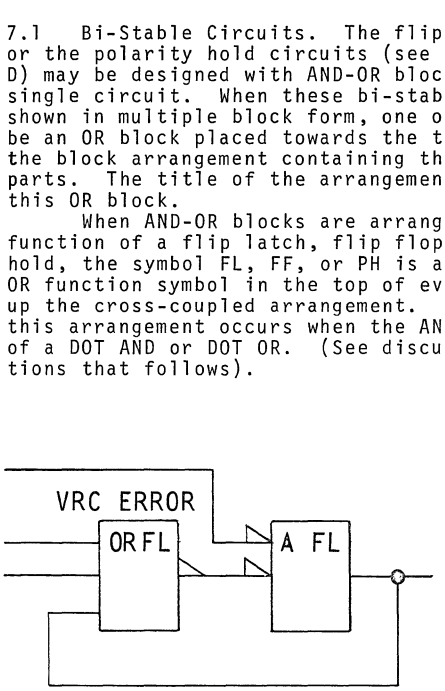
DIFFERENTIAL AMPLIFIER

CORE DRIVER

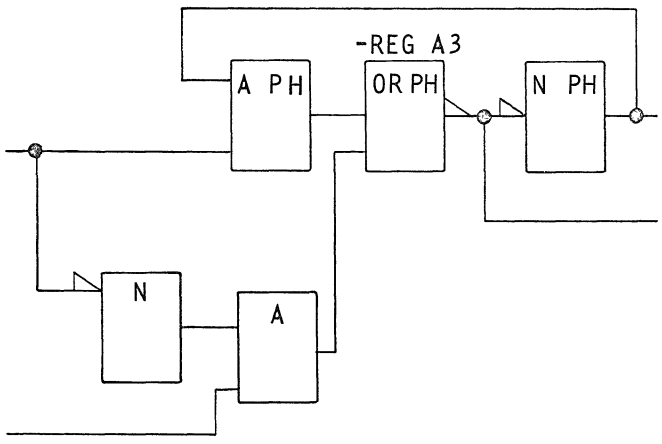
7. MULTIPLE BLOCK CONFIGURATIONS

7.1 Bi-Stable Circuits. The flip flop, flip latch, or the polarity hold circuits (see examples A, B, C, D) may be designed with AND-OR blocks instead of a single circuit. When these bi-stable circuits are shown in multiple block form, one of the blocks will be an OR block placed towards the top (or left) in the block arrangement containing the cross-coupled parts. The title of the arrangement is placed above this OR block.

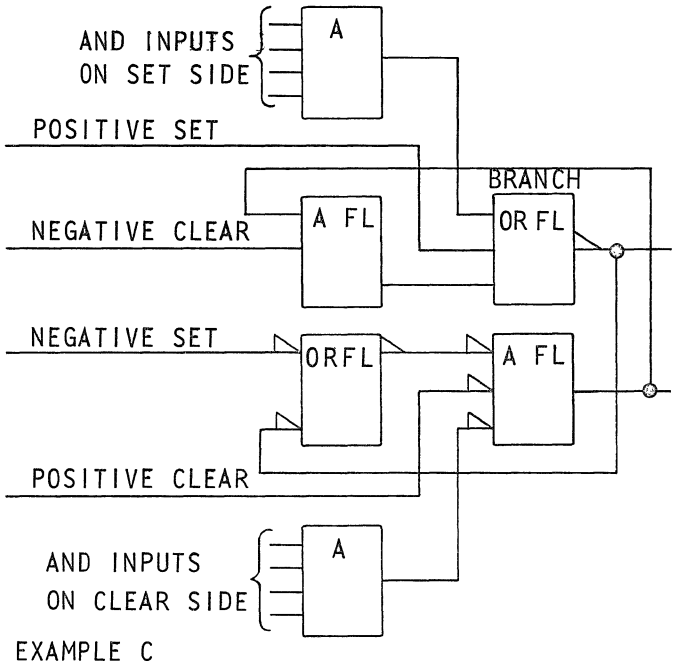
When AND-OR blocks are arranged to perform the function of a flip latch, flip flop, or polarity hold, the symbol FL, FF, or PH is added to the AND-OR function symbol in the top of every block making up the cross-coupled arrangement. An exception to this arrangement occurs when the AND-OR block is part of a DOT AND or DOT OR. (See discussion on DOT functions that follows).



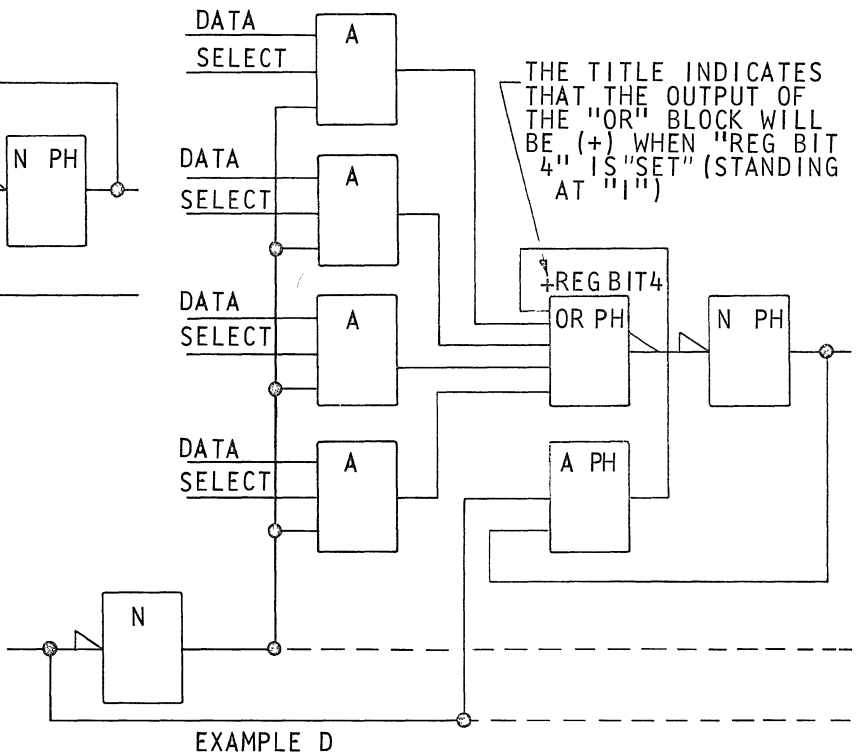
EXAMPLE A



EXAMPLE B



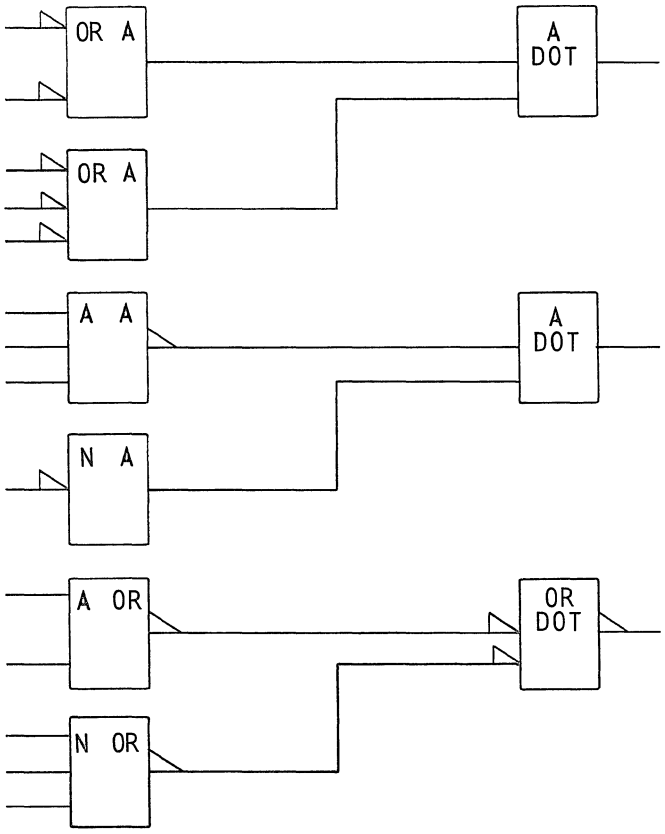
EXAMPLE C

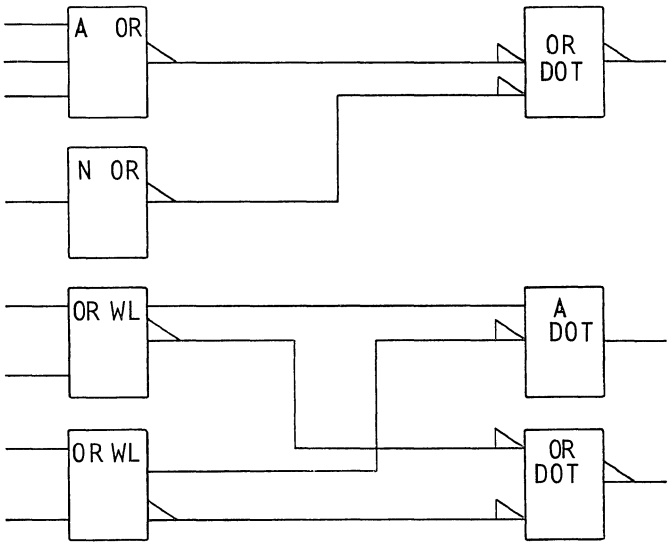


EXAMPLE D

7.2 DOT OR, DOT AND. Basic blocks whose outputs are connected externally to perform an AND or OR operation (DOT AND, DOT OR) are identified by an additional A or OR placed in the block to the right of the primary block function symbol. In the ALD's block labeled OR DOT or A DOT is used to form the junction of the lines being joined.

When the output of a block enters into both a DOT OR and a DOT AND, the letters WL (for wired logic) are placed to the right of the primary block function symbol.





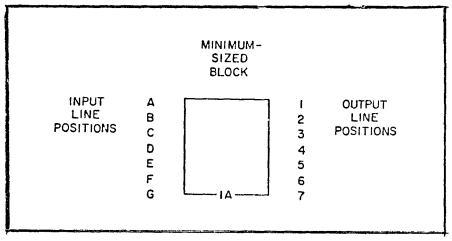
8. BLOCK INFORMATION

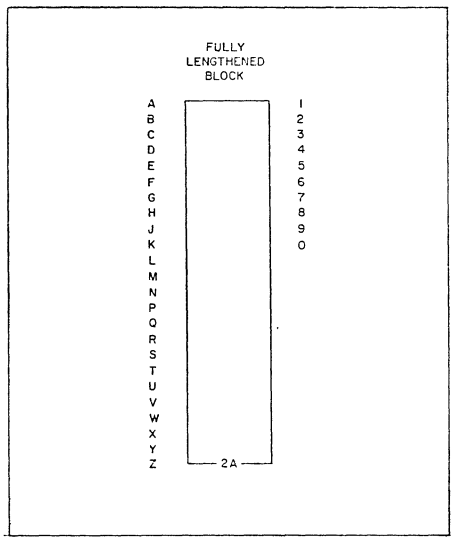
8.1 Logic Blocks. Logic blocks are positioned on the page in a matrix 7 columns wide and 13 rows high. The columns are numbered 1 - 7; the rows are lettered A - N, excluding I; the 91 block positions are labeled 1A through 7N. The need for routing lines across a page restricts the number of block positions which may be used to 49 under average conditions.

8.1.1 The individual logic block area is 14 characters wide; the interior of the block is 6 characters wide, two edge box positions (1 character each) and fields at either side of the block for 3 character pin designations. The logic block is a minimum of 7 lines high; 5 lines of information appear inside the block and one line on its bottom edge. There are 7 positions for input lines, lettered A - G, and 7 for output lines, numberd 1 - 7.

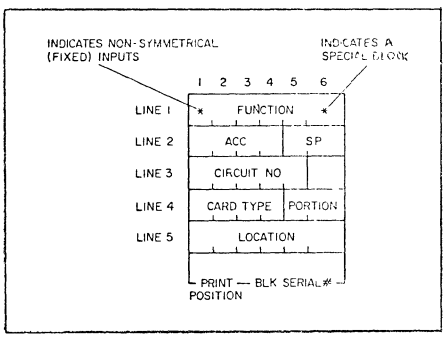
8.1.2 When necessary, the block may be lengthened downward to accommodate a maximum of 24 sinks, lettered A - Z, excluding I and O, and 10 sources numbered 1 - 9, 0. Blocks may not be lengthened below the bottom edge of minimum - sized blocks in row N. Lengthened blocks are assigned the block position of the uppermost part of the block.

8.1.3 On the Logic Sketch Sheet, all logic blocks must be outlined in order to reproduce. Thirteen blocks should not be drawn in one column, nor more than 49 on a page.





8.2 Information Inside Logic Block.



8.2.1 Line One, the logical function being performed by the circuit. Permissible logic function symbols for a given circuit appear on the circuit flyer. An asterisk in the first character position indicates that the input line positions must be positioned, as indicated on the circuit flyer.

NOTE: The Symbology to be used on the ALD's are governed by Corporate Engineering Standard CES 0-1046-3 (SLDA Logic Block Symbols).

8.2.2 Line Two.

(a) Characters 1 - 4. Additive Card Codes (ACC). Additive Card Codes indentify those logic blocks which pertain to a special class of machine features in which the feature can be installed by plugging only the feature cards.

(b) Characters 5 - 6. A symbolic package designation may appear here. See Partitioning Program of Packaging and Checking System - LMP 0-2860-081

8.2.3 Line Three.

(a) Characters 1 - 5. The circuit number of the circuit represented appears here. The circuit number must be present for certain SLDA programs to function. This circuit number is a means to specify the electrical circuit independently of the packaging. By specifying the circuit, the performance of the logical circuit is well-defined and simulation, load checking and logic partitioning can be carried out as an aid in packaging.

(b) Character 6; Unused.

8.2.4 Line Four.

(a) Characters 1 - 4. The card code which designates the type of card used to implement the logic function.

(b) Characters 5 - 6. The portion and sub-portion used on the card are indicated here. A portion represents an independent section of a card. The section may be represented by one or more logic blocks, each of which has a sub-portion number.

8.2.5 Line Five.

(a) Characters 1 - 6. The location of the card is identified here by gate (one alpha), a dash, board or panel, (one alpha, one numeric) socket location (one alpha, one numeric). The location given in the case of a 12-pac card (one occupying vertically adjacent card positions) is the upper location. The frame location is given in the title block. All the circuits represented on a page must be in one frame.

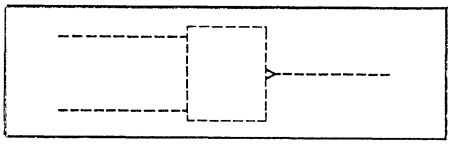
8.3 Information in the Edge of the Block.

8.3.1 Bottom Line.

(a) Characters 1 - 2. The block's print position is shown here. On the Logic sketch sheet, the block position of each block used must be traced over, in black pencil, if reproductions are to be made.

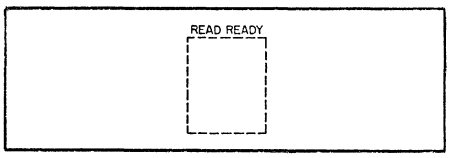
(b) Characters 5 - 6. The block serial number appears here. The block serial number is a two-letter unique designation of a block on a given page. The serial number of a block need not change as long as the block remains somewhere on the page. Block serial numbers are assigned for the blocks on each page in serial order beginning with AA. It is recommended that block serial numbers SA through ZZ are reserved for blocks added by a version.

8.3.2 Sides. A hollow wedge in the edge of a block in line with an input or output line, indicates that the more negative of two D.C. voltages may be expected at the indicated input or output line when the circuit represented is performing the indicated function. The absence of a wedge indicates that the more positive voltage may be expected.

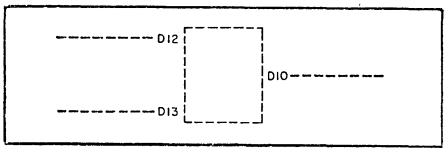


8.4 Information Outside the Block.

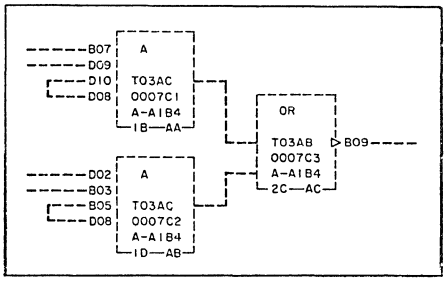
8.4.1 Block Title. Fourteen spaces are available in the line immediately above the block title. This space is not available if there is another block immediately above the first.



8.4.2 Card Pins. Card pins appear at the left and right of the block, in line with the input and output lines. Pins used for wiring are B02 through B13 and D02 through D13, or in the case of 12-pac cards, B02-B13, D02-D13, G02-G13, J02-J13.



When it becomes necessary to tie down unused input or output pins, the following rules must be used. The only voltages that may be used to tie down inputs or outputs will be ground and +3. The Physical Master Tape System (PMT) used for board wiring will accept the ground pins (D08, J08) and the +3 voltage pins (D03, J03) being in more than one net number.



IBM Location Manufacturing Practice

INTRODUCTION

1.1 SCOPE: This practice presents the approved documentation methods for both vertical and horizontal boards.

1.2 OBJECTIVE: The intent of this practice is to provide the designer with a document that can be released if the board is not processed through S.L.D.A.

1.3 DEVIATION APPROVAL: Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

1.6 SUPERSESSION: This practice supersedes LMP 0-2860-075 dated Jan. 67.

RECOMMENDED PRACTICES

2. PLUG IN CHARTS

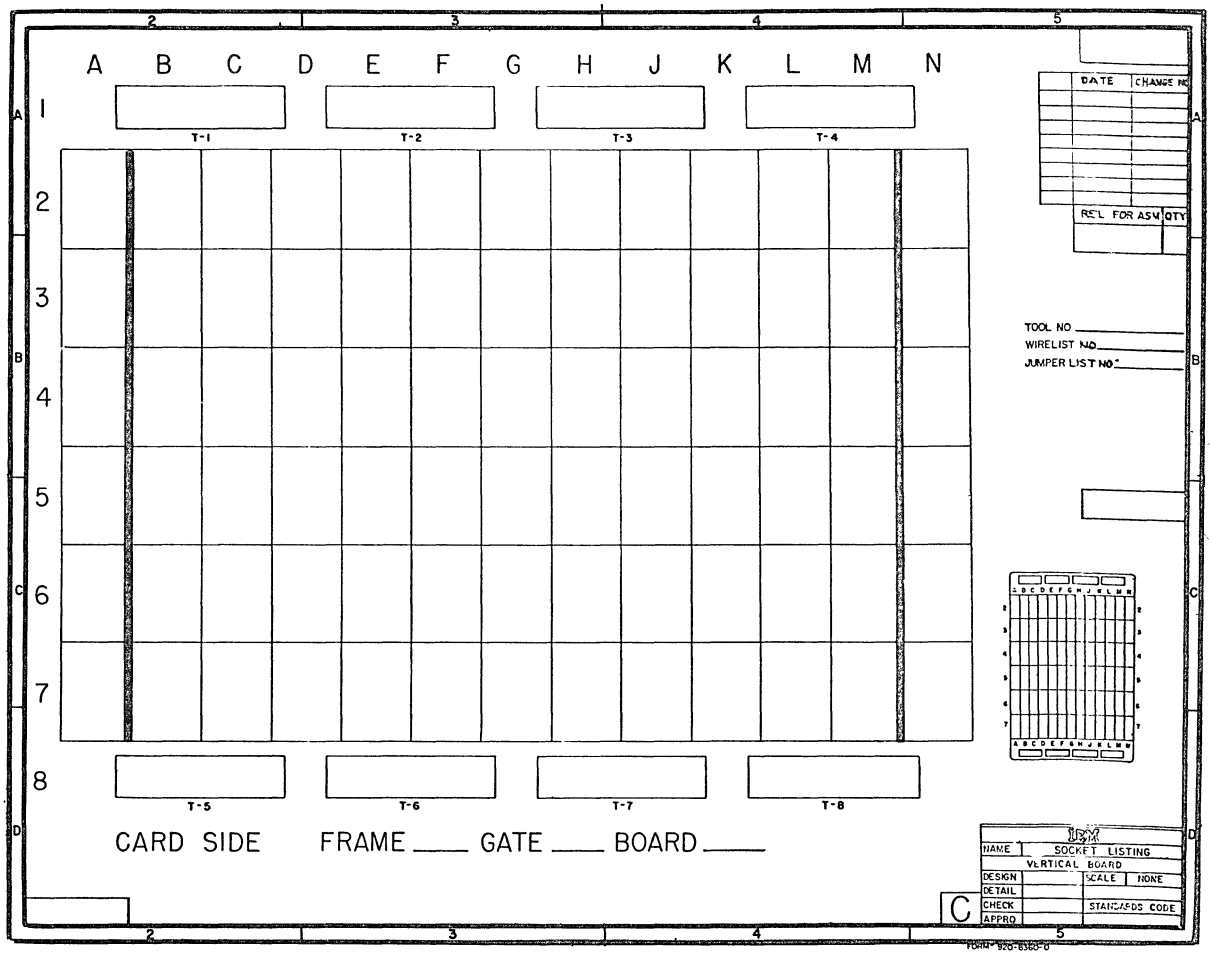


FIGURE 1

2.1 Vertical Board

2.1.1 Description. The chart (Figure 1) represents the actual board layout and addressing scheme.

Additional card sockets may be obtained by wiring voltage pins to edge connector sockets.

It should be noted that the plug-in-chart represents the board as viewed from the card side.

2.1.2 Requirements. The following information should be recorded on this chart:

At the bottom of the chart fill in Frame, Gate, Board sections.

For socket location the following is necessary: (see Fig.2)

2.1.3 Plug-in-Chart (Vertical Board) Form No. 920-8360

Purpose of chart:

a) To aid the designer in populating the board with cards by providing a record of used card locations and card portions.

b) To generate a document which can be released into Express if the board is not processed through D.A. See Figure 1.

2.2 Horizontal Board

2.2.1 Description. The chart (Figure3) represents the actual board layout and addressing scheme.

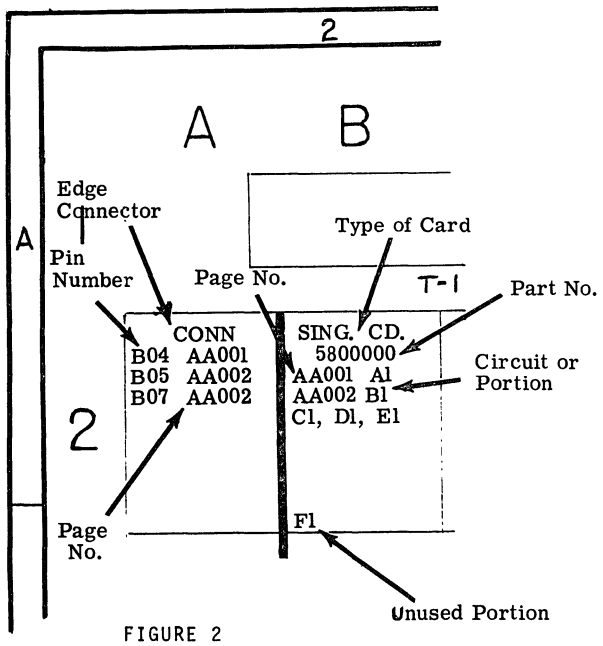


FIGURE 2

2.2.2 Plug-in-Chart (Horizontal
Form No. 920-8361

Purpose of Chart:

a) To aid designers in populating the board with cards by providing a record of used card locations and card portions.

b) To generate a document which can be released into Express if the board is not processed through Design Automation.

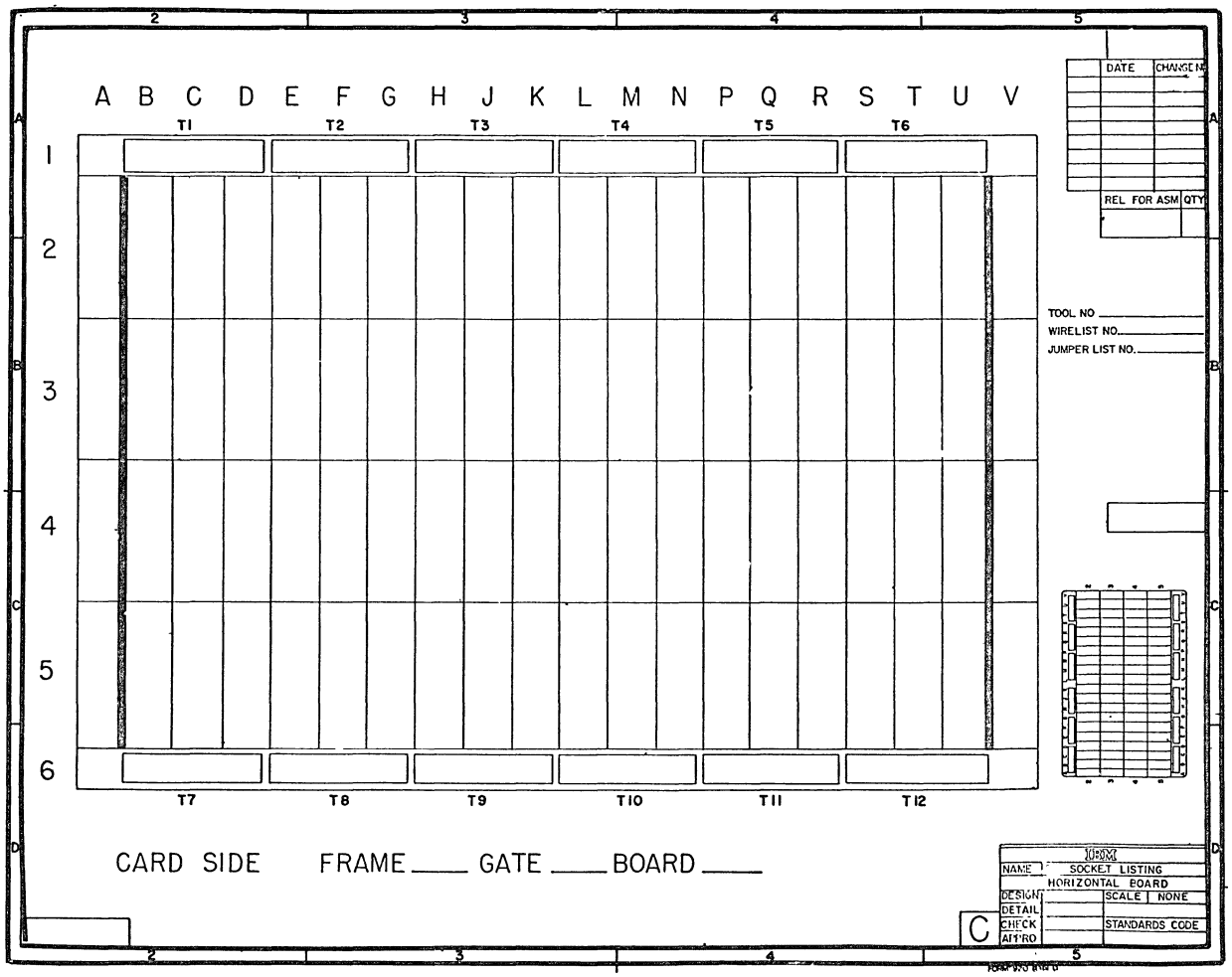


FIGURE 3

3. BOARD LAYOUT

3.1 Some holes and pins have permanent assignments for ground and voltage connections. Figure4 shows the board layout and includes pin and hole locations, permanent assignments, addressing scheme and location of connectors.

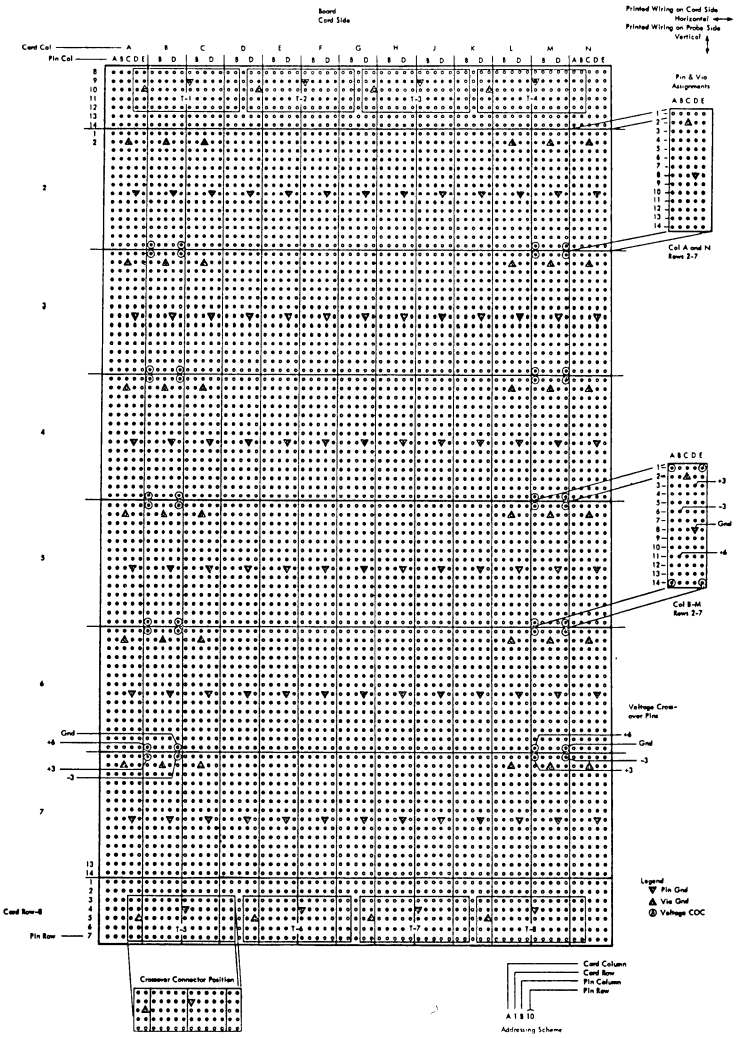


FIGURE 4

IBM Location Manufacturing Practice

INTRODUCTION

1.1 SCOPE. This practice will introduce the procedures and format necessary for input to a design group. It also introduces the various aspects of SLDA which are of interest to the design engineer.

1.2 OBJECTIVE. This practice is intended for use by the design engineer and logic designer. It will provide a method of uniform representation within SLT design.

1.3 DEVIATION APPROVAL: Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

RECOMMENDED PRACTICE

2. SECOND LEVEL DRAWINGS

2.1 Function: Second level drawings have two functions:

a. They are the source document for logic implementation.

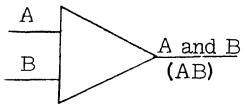
b. They are used by maintenance personnel for training and diagnostic analysis.

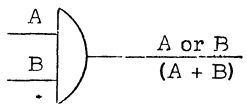
Because of this usage, arrangement and clarity of logic flow are essential. Logic flow should always be left to right.

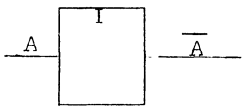
2.2 Logic Blocks respond to logical "1" inputs and do not invert.

2.3 The basic symbols used on second level drawings are:

2.3.1 AND, OR INVERTER

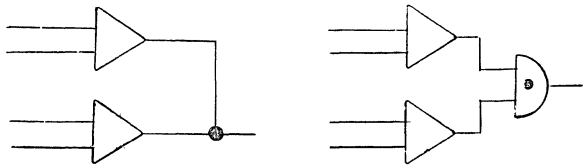
AND 

OR 

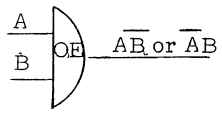
INVERTER 

The AND circuit with logical "1" signals on all inputs will have a logical "1" output. The OR circuit with a logical "1" on any input will have a logical "1" output. INVERTERS will be drawn for logic inversion only, never for proper line levels.

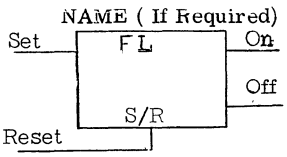
Dot OR's should appear as discrete OR symbols on second levels.



2.3.2 A special "OR" circuit is the exclusive "OR".

EXCLUSIVE "OR" 

2.3.3 Flip Latches will be represented by:



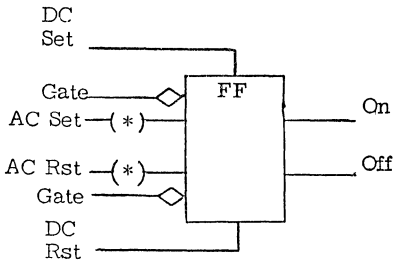
Do not draw a flip latch using discrete AND, OR symbols.

2.3.3 (Continued)

All Set inputs come into the left side of the block. All Resets enter the bottom of the block. A logical "1" on the Set initiates a logical "1" at the ON output.
The output of the top half of the block is always the ON output. The output of the lower half of the block is always the OFF output.

If the flip latch set and reset times overlap, the block must be labeled S/R (Set overrides reset) or R/S (Reset overrides set).

2.3.4 Flip Flops will be represented by:



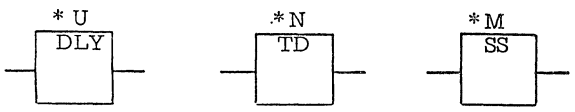
Upper half of block contains all ON inputs and outputs.

Lower half of block contains all OFF inputs and outputs.

All AC inputs and gates enter the left side of the block. The diamond ( ) in an input line represents the gate input. The input adjacent to the gate is the AC input associated with that gate. The DC set enters the top of the block. The DC reset enters the bottom of the block.

*P will represent a positive shift and N will represent a negative shift in the AC Set/Reset necessary to trigger the flip flop.

2.3.5 The symbols for delays and single shots are:



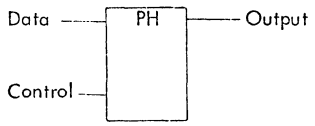
CARD	FUNCTION
DLY	Delays only the leading edge. A logical "1" input gives a delayed logical "1" output.
TD	Time Delays both the leading and trailing edge.
SS	A logical "1" input to single shot gives a logical "1" output pulse.

NOTE: *

M = millisecond
U = microsecond
N = nanosecond

Any other type of circuit block will be represented by the appropriate identity.

2.3.6 The polarity hold has a single Bl-stable output that can be changed by proper sequencing of the control and data inputs.



The upper half of the left side of the block will represent the data input, the lower half will represent the control input.

3. GENERAL

3.1 Special circuits required at the switch logic interface (such as integrators and resistors) must be specified.

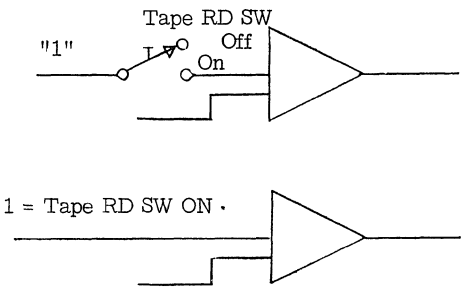
3.2 Implementation instructions:

a. The types of line drivers and terminators must also be specified.

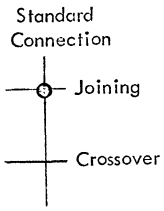
b. If special cards are used, (i.e. SMS cards or SLT cards) supply enough informations so they may be properly implemented. This may be on supplemental pages, not on the second level diagram.

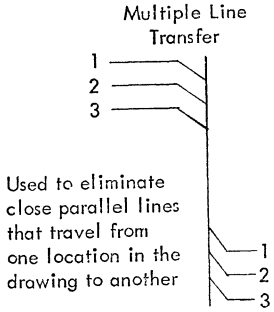
3.3 Lines derived from photo sensors should relate line polarity (i.e. logical "1" or "0") to the state of the light path (i.e. clear or blocked). Lines from electro-mechanical switches should relate line polarity to the position of the switch, i.e. ON or OFF.

(EXAMPLES)

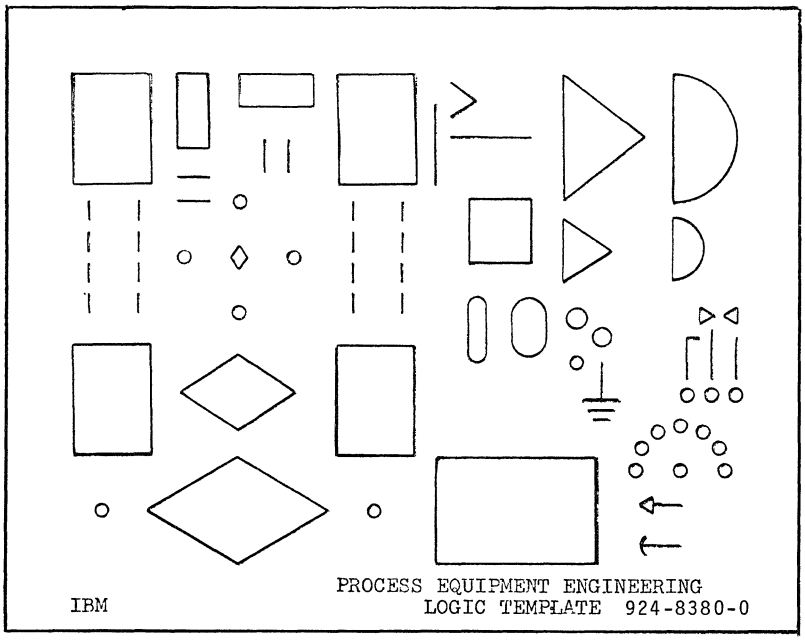


3.4 Solid junctions dots are used at all line junctions except with multiple-line transfers.





3.5 The following template should be utilized by the design engineer in the creation of second level schematics used as input to the SLT designer for implementation into first level logics necessary for SLDA. Deviation from the functions represented by the template should be infrequent as possible.



IBM Location Manufacturing Practice

INTRODUCTION

1.1 SCOPE. It is the purpose of this practice to assist the design engineer in understanding the over-all Solid Logic Design Automation System. A more comprehensive study of SLDA may be found in CEP 0-2815.

1.2 OBJECTIVES. The objective of the SLT program is to produce by highly mechanized processes those parts needed to build a new tool or system. It takes advantage of the use of computers to help in the engineering design, record keeping and release activities as well as the manufacturing processes and filed servicing aspects of the technology.

1.3 DEVIATION APPROVAL: Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

RECOMMENDED PRACTICES

2. GLOSSARY

2.1 BASIC. Refers to the standard design; includes optional features (MFI's) if drawn as part of the standard logic pages.

2.2 CIRCUIT NUMBER. The circuit number consists of five alphanumeric characters of the form ANNAA which uniquely defines a particular basic circuit.

2.3 CROSS-REFERENCING. When the signal name is shown on the source page the program will automatically insert the same signal name on the sink page providing the net number appears on both pages.

2.4 DELETION PROPERTY. Defined as obeying certain ground rules during the layout of the large card or back panel wiring so that any node can be eliminated from the net without disturbing the rest of the net.

2.5 DOT-BLOCK. The logic block which must be used on logic pages to show the dot-or, dot-and function which is physically accomplished by tying two signals together at a pin. Thus one logical net on several logic pages may be combined with other logical nets by means of a dot-block to produce one combined physical net.

NOTE: All fanout for such a net must be shown at the output of the dot-block; one dot-block may not feed another dot-block.

2.6 FUNCTION CHECK. Functional checking is performed to determine that the circuits shown by the logics do appear on manually assigned cards.

2.7 GROUPING. Prior to partitioning certain circuit configurations must be associated together. Circuits which are represented on logic pages by more than one block, but which, without exception, are always found on the same small card are said to be in the same group.

2.8 LOAD CHECKING. Check nets to see that the driven and driving circuits are compatible and that the D.C. loading requirements are met.

2.9 LOCATION CHECKING. Checks made to insure that: (1) One group is not assigned two different locations or two groups assigned the same location, (2) Two small cards are not assigned to the same location, (3) Too many cards are not assigned to one large card, (4) The same card portion has not been used more than once.

2.10 LOGICAL MASTER TAPE. Contains all logic page information which is obtained by manual input from logic pages designed by engineers or feedback from computer programs.

2.11 NET. A complex of nodes, normally pins or connectors on a logic page, all common electrically.

2.12 NET NUMBER. The net number consists of the source block page number, block serial number and output line position of the source block. It consists of eight alphanumeric characters of the form. AANNNAAB (A - alphabetic N - numeric B - either alphabetic or numeric).

2.13 NODE. One circuit termination point of a net such as a pin on a card or a connector on a board/panel.

2.14 PARTITIONING. Breaks logic up into cards and assigns the cards to boards.

2.15 PHYSICAL MASTER TAPE. Contains all physical location information for board/panel design and cable assignment.

2.16 PIN ASSIGNMENT. A program which accepts as input information from a rules tape and fills in the card pins for groups which have been assigned to card portions. These groups are checked to make sure that the card portion is legal for the group number.

2.17 PINS. Small parts mounted into a board or back panel which act as the male part for the card or tape cable connectors.

2.18 PLACEMENT. Takes cards assigned to actual boards and places them in locations on the boards.

2.19 PRIMARY PAGE. A logic page which is submitted as part of an Engineering Change to be processed by SLDA.

2.20 PORTION. Circuits on a card which are connected together via printed wiring are said to be in the same portion.

2.21 SECONDARY PAGES. Those logic pages which are updated as a result of a change to a primary page. Such as a line name being changed on the source page for an output net which causes the line name to be changed on all sink pages which will print out as secondary pages. The E.C. Level of the primary page will be reflected on the secondary page.

2.22 SELECTION. A program which takes requests from the engineer or the Control Center and selects the data necessary for processing a request. Logic may be selected by page and block and/or physical location.

2.23 SIGNAL NAME. The 30-character name which gives meaning to the logical net; each net has only one signal name which may be blank.

2.24 SINK. The end or ends of a net to wich signals flow. Example: Sink Page - same as "To" page in SMS technology.

2.25 SIMULATION. A program to enable the designer to exercise the logical circuit action before committing the design to hardware. Simulation means "pulse chasing" of individual electrical signals through the logical circuits.

2.26 SOURCE. The beginning of a net from which signals flow. Example: Source Page - same as "From" page in SMS technology.

2.27 SYMBOLIC PACKAGE. The symbolic package is composed of two characters to be used by the partitioning and placement programs. Blocks with the same characters in the symbolic package field will be placed on the same board by the card partitioning programs.

NOTE: Blocks with different symbolic packages may be packaged on the same board.

2.28 VERSION. The term used within SLDA to indicate the particular manner to which logic records are kept for certain features; that is, a feature is a version of its records on the Logic Master Tape which are kept as an add/delete (by block) to the basic records.

NOTE: This gives automatic or implied updating of the feature by the basic since an added basic block is thus effectively in the version.

2.29 VERSION PAGE. Page made up of all blocks on the basic page which appear unchanged in the version design plus the additional blocks (called version blocks) which are needed in order to change the basic page into the version page.

2.30 VIA HOLE. A plated-thru hole which may or may not contain a pin and used exclusively as a contact between conducting layers. Not considered as a node.

3. DESCRIPTION

3.1 A NETWORK OF DESIGN AUTOMATION PROGRAMS gives the Engineering logic designer powerful tools to aid him in simulation and packaging of logic. The programs aid manufacturing by feeding printed wiring information concerning boards to a process automation system in a relatively short time cycle from design changes. Field personnel will be aided by the fact that the SLDA (Solid Logic Design Automation) programs will be used corporate wide which will standardize outputs from all locations.

3.2 THE PHILOSOPHY OF SLDA is to reduce time between development and manufacture. Design Automation personnel from all divisions of IBM were called upon to contribute to the programming of the Design Automation system. Primarily a development tool, the SLDA programs assume that standards can be established for SLT, in terms of circuits and packages, as well as design procedures.

3.3 LOGIC DESIGNERS must gain a thorough understanding of the procedures, capabilities, and limitations of the SLDA program system. Only in this way can it become a worthwhile tool for the designer. Answers to detailed questions concerning the operational status of SLDA programs and about the contents of this practice may be obtained by consulting your local SLDA liason group.

4. DESIGN AUTOMATION PROCESSING

4.1 DESCRIPTION. The Solid Logic Design Automation System consists of four major stages of processing.

4.1.1 The Logic Master Tape (LMT). This tape is the machine language record in logic page order. It has a direct correspondence to the logic pages describing the unit being designed. Each time a portion of this machine record is altered, logic pages containing the changes are produced for the engineer.

4.1.2 Simulation. Simulation programs are designed to allow the engineer to dynamically exercise the logic before the machine is packaged.

4.1.3 Packaging and Checking. This is a series of programs designed to aid engineers in packaging logic into a physical environment or to check data which was manually inserted on pages.

4.1.4 Physical Master Tape (PMT). This is a machine language record of the physical aspects of the design. It is arranged in physical sequence. Its purpose is to:

4.1.4.1 Retain in a more convenient form that physical data inherent in the LMT as well as additional physical data not contained in the LMT (wiring data primarily).

4.1.4.2 Serve as a vehicle for retaining the physical design at a fixed level while the logical design is undergoing change or experimentation.

4.1.4.3 Retain records on magnetic tape as design evolves. Each stage is dependent on the logic master tape (LMT) or physical master tape (PMT) for the source data.

4.1.4.4 Selected programs extract information from the tapes under the direction of requests submitted by the users. There are several computer programs which make up the framework of each stage. Outputs consist of documents to aid engineering in the development of computers,release documents, and tapes for manufacturing.

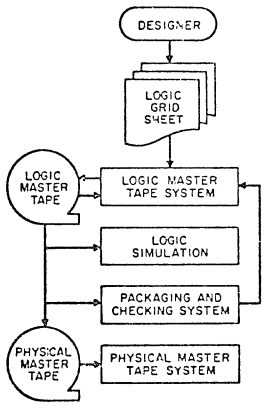


FIGURE 1

5. LOGIC MASTER TAPE SYSTEM

5.1 ORGANIZATION OF LMT.

5.1.1 One Magnetic Tape has on it the composite logic design of a machine type at one particular engineering level. This composite design includes the parent (basic) design plus all features. If required, the history of valid designs may therefore be accrued by saving tapes.

5.1.2 The Logic Design exists as a set of interconnected logical functions which are subdivided into pages. These logical functions are hereafter referred to as logic blocks and the interconnections are referred to as nets.

5.1.3 Logic Blocks are the basic units of information which are recorded on the LMT. Feature designs, which are referred to as versions, are recorded as logic block add and/or deletes to the basic set of logic blocks comprising the parent design. Each block is identified by:

(a) Logic page number
(b) Block serial number
(c) Version number

5.1.4 Nets are identified by the page number (5 characters) and the block serial number (2 characters) of the source block at which the net originates as well as the line position from which the net emerges from the block (1 character).

5.1.5 The Format of the net number is specific and must be adhered to throughout the system.

A A N N N A A A/N

Page Ser Pos

8 CHARACTERS

A = Alphabetic N = Numeric

5.1.6 A Net is a set of signal points (source and sinks) which have to be electrically interconnected. Generally, the source point refers to the output pin of the driving block and the sink points refer to the input pins at the driven blocks. The net identification is used to indicate which points (pins) belong to a given network.

5.1.7 The Following Figure summarizes the basic unit of data in the LMT system: The logic block surrounded by inputs and outputs with their net numbers.

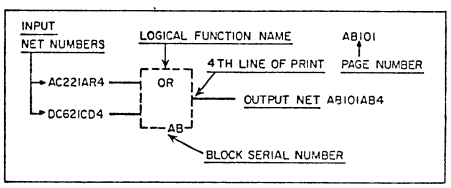


FIGURE 2

5.2 PREPARATION OF THE LOGIC MASTER TAPE

5.2.1 ORIGINAL DATA

5.2.1.1 The Original Logic Design Data for a machine is entered into SLDA through the use of a logic grid sheet. Information on the pages is keypunched, verified, and merged onto the LMT. Some checking of logic pages will be performed as updating of the LMT takes place. This will enable designers to make certain corrections immediately following the printing of logic pages.

5.2.2 ADDING DATA

5.2.2.1 As the Original Data is Expanded into a complete design, new data is added to the logic description on the LMT and printed on the appropriate pages. All such additional data may be entered manually by marking up the existing pages. However, there are many other programs in the system which can supply some of this data. It is up to the designer to make a choice as to which parts will be supplied manually and which will be supplied by programs.

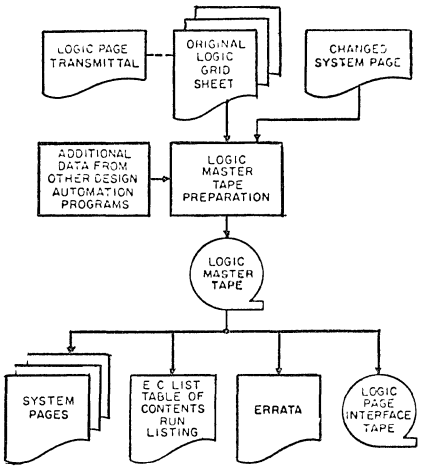


FIGURE 3

5.2.3 CLASSES OF DATA.

5.2.3.1 Minimum Data. These data are logic blocks with functions and circuit numbers plus indicated interconnections. This is the minimum information required to establish an LMT which could be processed by the remaining SLDA programs.

5.2.3.2 Additional Data. These data consists of card type, portion and terminal pins, card socket locations and connector descriptions. It is this information which can be added to the LMT either by use of the design assistance programs or by the manual entry on the system pages or by combination of both methods.

6. SELECTION SYSTEM

6.1 GENERAL. The logic master tape serves as the central data source for the simulation, packaging/checking, cabling and physical master tape systems. These systems are called upon to operate on the logical data for the entire LMT or in part. Certain programs require the data to be accumulated on a physical location basis; others require it on a logical location basis.

6.1.1 The Selection System provides the ability to select portions of the logic master tape by logic locations, by physical locations, by symbolic package, or by combinations of all three. These selections must be designated exclusively for either the basic design or for any one version number.

6.2 SELECTION MODES ARE:

6.2.1 Logical; Individual ALD(S) or a range of ALD's are selected. All logic blocks are actively selected.

6.2.2 Physical; The entire Logic Master Tape is searched to find all logic pages/blocks which satisfy the physical selection request.

6.2.3 Symbolic Package; Those logic blocks which have a symbolic packaging code designated in the last two positions of line two are selected. This selection type is requested if the symbolic package mode of partitioning is being used.

6.2.4 Environment; This is an additional mode of selections which apply to partitioning only. Select looks for physical locations, on the entire master tape, which partitioning is using as its packaging environment. Partitioning must know all physical locations or information about the boards which it will assign cards to in order to get the entire picture. This must be requested to run partitioning properly.

6.3 SELECTED DATA TYPES. All data which is selected from the LMT is categorized as either active or peripheral.

6.3.1 Active Blocks. Logic Blocks or connectors which are part of the primary logical or physical selection are active selections. Only the active data is operated on during a packaging assignment run and re-updated on the LMT.

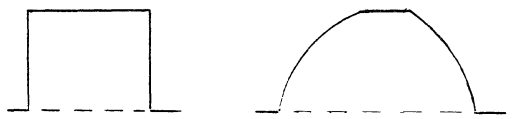
6.3.2 Peripheral. Logic blocks which feed an active block or blocks, are considered peripheral. Load Check uses peripheral blocks to get as complete a load check as possible on selected logic. Partitioning uses peripheral blocks to get a picture of lines leaving and entering the logic to be partitioned and give a count of nets leaving the board. Block check, normally does not give messages on peripheral blocks except if no circuit number is found.

7. SILMULATION SYSTEM

7.1 GENERAL

7.1.1 SLDA Simulation is a system of programs which take selected logic from the Solid Logic Design Automation Logic Master Tape (LMT) and perform a detailed logical simulation. Output of the program is a timing chart of the logic showing the on-off sequence of up to 100 nets. This can be thought of as similar to monitoring the logic on a multi-channel oscilloscope. However; simulation is not intended to replace model testing, simulation does not take into account variations in circuit components, physical placement of cards and boards, effects of wire lengths, etc. The designer will therefore get the most profit out of simulation by running it before packaging his logic.

7.1.1.1 The Simulation Program is primarily logical, that is, all nets are either "on" or "off". Each logic block represents a circuit which has a "switch-on" and a "switch-off" delay associated with it. The delays are extracted from the Corporate Circuit Flyer and used in the program. In graphic terms, all pulses are considered to be like (a) not like (b).



(a) (b)

FIGURE 4

7.1.1.2 The "ON" and "OFF" delays for simulation are the Nominal (Average) delay figures as determined by the circuit designers and included on the circuit flyers. These delays are to be considered as the time between the arrival of a signal (i.e., of the threshold voltage) at a block, and the time this signal reaches the next block (at threshold voltage).

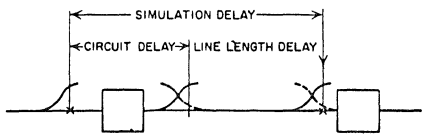


FIGURE 5

7.1.2 Simulation is composed of the elements listed below. Elements 1, 2, and 3 are the basic requirements, element 4, consists of optional features.

7.1.2.1 Element 1. A set of interconnected logic blocks (not exceeding 3500) with circuit numbers (extracted from the logic master tape).

7.1.2.2 Element 2. Circuit characteristics consisting of logic functions and delays (extracted from rules tapes-i.e., from circuit flyers).

7.1.2.3 Element 3. Controls (by use of a control language).

(a) Specification of initial conditions for lines with outside sources.

(b) Specification of changes to outside sources as they occur with time.

(c) Selection and definitions of output charts desired.

7.1.2.4 Element 4. Refinements (also by use of the control language)

(a) Monitoring of critical nets (tests) during simulation to alter the course of events.

(b) Conditional commands (obtained by use of indicators.

(c) Flexible time base (scales).

(d) Transfer for loops or for skipping of controls.

(e) Experimental Corrections to logic.

(f) Modification of circuit type delays.

7.1.3 The Capacity of the Program is determined by the size of the 7090 memory and the complexity of the logic. A maximum of four thousand nets can be simulated.

7.2 FLOW OF SIMULATION SUB-PROGRAMS. The following figures illustrate the simulation run sequence. It has four major programs -- the Select program, function translator, the Simulation Compiler, and Simulation itself.

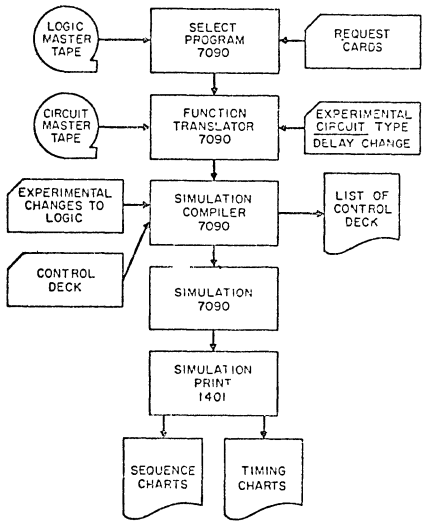


FIGURE 6

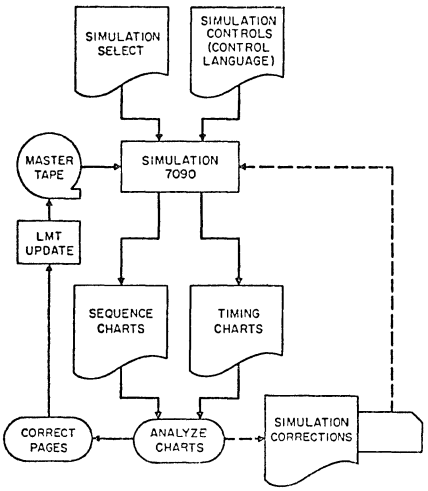


FIGURE 7

8. THE PACKAGING AND CHECKING SYSTEM

8.1 DESCRIPTION. The packaging and checking system consists of several programs to aid the engineer.

8.1.1 Block Checking. This program will compare the functional symbols and use of wedges, appearing in the logic block, against the circuit rules. It will generate error messages when deviations are found.

8.1.2 Load Check. This performs a D.C. network check on nets. Error messages are generated for nets which violate the circuit rules.

8.1.3 Partitioning. This program will select the cards to implement the engineer's design, and assign these cards to boards.

8.1.4 Pin assignments/Checking. This program will either assign pins to logic block or check the existing pins against the card rules.

8.1.5 Placement. This program places cards which have been assigned to boards in order to optimize board wiring.

8.1.6 Connector Check. This program checks each net for the proper number of connectors and produces several reference listings.

8.1.7 Connector, Checking and/or Assignment. This program will assist in the assignment of connectors to the signal networks. Accuracy of connectors/cables assigned manually will be checked.

8.1.8 Location Check. Selected physical locations are checked for duplicate and over-lapping card types by physical location. Charts are printed out which show the locations by card type for each board processed. Suitable errata messages print out whenever error conditions are encountered.

8.1.9 Cabling. Computes cabling for intra-frame requirements and provides a process automation interface tape.

8.2 BLOCK CHECK. The block check program compares the logic block information selected from the logic Master Tape to the circuit rules found on the Circuit Master Tape. These rules contain circuit block specifications from the corporate circuit flyers. The results of the comparison enables the program to perform the following functions:

8.2.1 Assign the Input/Output Numbers to the Logic Blocks. These numbers are recorded on the BET (block equivalence tape) to be used by the Grouping, Partitioning, Pin Check or Assignment, Load Check, and Simulation programs.

8.2.2 Check (or correct, when requested) the circuit functions (names) and edge - of - box characters for the blocks. The program also checks to see if any necessary input or output is missing. The line positions of the inputs and outputs are also checked against the rules.

8.2.2.1 In Block Check Processing, when a rules violation is detected, the program generates appropriate errata. Further functioning of the program is determined by (1) Whether "checking only" or "correct function and box character errors" has been requested, and (2) the nature of the violation.

8.2.2.2 If "Checking Only" is specified, the errata messages will be printed. If "correct" is specified, the program will correct, when possible, the function and box character errors on the block equivalence tape (BET), and will not Print a message.

8.2.2.3 If the Nature of an Error is such that block check cannot make a correction, then an errata message is generated whether or not correction of function and box character errors have been specified. Errors of this type (code 01) also prevent block check from properly assigning input-output numbers.

8.2.2.4 The Errata Messages and the causes of them are detailed in CEP 0-2815-12.

8.3 BLOCK CHECK ERRATA. The error conditions (except for function and box character errors) detected by block check, if not corrected, will usually cause problems in processing PCS programs or the simulation program. These conditions should, therefore, be corrected before these programs are run.

8.3.1 The Errata Messages are in two categories, Code 01 and Code 02. Any code 01 error condition may result in incomplete and/or improper input-output number assignment. Also Code 02 conditions "block has missing input", and "block has missing output" will cause incomplete input-output number assignment.

8.3.1.1 The effects of the code 01 error conditions on the other programs are as follows:

(a) Load Check - Incomplete nets and incomplete checking of all pins in the nets.

(b) Partitioning - Will not partition any block having code 01 errata.

(c) Pin Assignment - Cannot assign all pins, and can possible incorrectly assign pins.

(d) Simulation - The erroneous block is dropped in the "translate functions" phase, and the condition must be corrected before simulation can proceed.

8.4 Load Check. Load check will be used by logic designers to determine D.C. loading violations.

8.4.1 Current Direction. The IRE standard is followed. It states that current flowing into a node is positive and away from the node is negative. Thus, into a block is negative, out of a block is positive.

8.4.2 Available Source Current. The current that can be guaranteed from a source.

8.4.3 Minimum Source Current. The current required to be drawn from source by a load.

8.4.4 Maximum Load Current. The maximum current taken by a load.

8.4.5 Minimum Load Current. The minimum current taken by the load.

8.4.6 Checking Performed

(a) Are rules present for each pin in the net?

(b) Is the net coupled?

(c) Does the net contain source and load currents at each level (up and down voltage levels)?

(d) Does voltage compatibility exist at each level?

(e) Is the net overloaded at either the up or down voltage level?

(f) Is the net underloaded at either the up or down voltage level?

(g) Have too many blocks been dot-and/ored?

(h) Are special case rules satisfied?

(i) General rules to be satisfied by the Load Check Program:

	Class	Signal UP	Level DOWN
NPN Family	Output	L	S
	Input	L	L
	Resistors	S	L
PNP Family	Output	S	L
	Input	L	L
	Resistors	L	S

Where S = Source L = Load

A source and load are required at each signal level.

8.4.7 Method of Checking. The program performs its checking by examining a table built from the rules for each circuit in a net. The table is first scanned to insure at least one coupled or non-check pin is in net. The current types of each pin are then examined to insure a source and load at the up and down voltage levels. Next, the operating voltage levels of the net are established. This is accomplished by choosing the most positive minimum up level and the most negative minimum down level.

EXAMPLE 1: The operating voltage levels of a net containing two pins would be -.3 and -7.0.

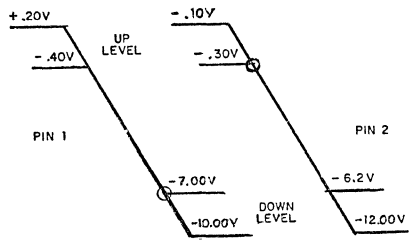


FIGURE 8

8.4.7.1 Currents and Voltage Levels. The two voltage levels (up and down) which are picked, must lie within the respective ranges of all other pins in the net in order to establish voltage level compatibility. The current at the up and down voltage levels for each point in the nets is determined by performing a linear interpolation between Vmin and Vmax for each point. In example 1, the operating up level was picked at -.3V. To find the current for pin 1 at this voltage an interpolation is performed between .2V and -.4V.

8.4.7.2 Overload Check. The available current in the net is determined by examining each current source. The weakest current or sum of all the source currents present in the net picked. The "current type" column on the circuit flyer determine this. The current picked must be greater than the sum of all the load currents for the overload check.

8.4.7.3 Underload Check. Some current sources require a minimum current to be drawn in order to guarantee proper operation of the circuit. This is called the underload check and is performed by taking the maximum of all minimum source currents. This current must be less than the sum of all minimum load currents.

8.4.7.4 Dot - Check. The dot-or check counts the total number of blocks that have been dotted and compares it to the dot-count figure appearing on the circuit flyers. If it exceeds the number an error is generated.

8.4.7.5 Special. Special cases are then checked, (of the form "X can drive only Y"). If the rule specifies to check the special case only, previous checking is bypassed. A special case overload check is also performed.

8.4.8 Options

8.4.8.1 List Suppression. Each of the lists produced by the program, the net list, the available currents and the incomplete net list, may be suppressed.

8.4.8.2 Different Rules. A special set of load check rules may be defined and used. This requires use of the CMT system to generate the special rules.

8.4.8.3 Net Reassignments. Several nets may be considered as one net for load checking purposes. Two nets are made into one if:

(a) Each net contains the same physical pin and these pins appear on the same block.

(b) Each net appears on the same "jumper" or "feed through" block.

8.5 PARTITIONING

8.5.1 DESCRIPTION. The partitioning program of the Solid Logic Design Automation System provides a means of assigning logic cards, and cards to boards. The objectives are to:

8.5.1.1 Package Logic on a minimum number of cards.

8.5.1.2 Package Logic on cards so that each card contains closely connected logic.

8.5.1.3 Assign Cards to boards in such a way as to minimize the number of boards required and the number of connectors required for each board.

8.5.2 GENERAL. SLDA logic pages with logic blocks containing the function symbol and standard five digit circuit code are the input to the partitioning program. The partitioning program will use the circuit code and card rules to assign a logic block (circuit) to a specific card and portion (card and portion code).

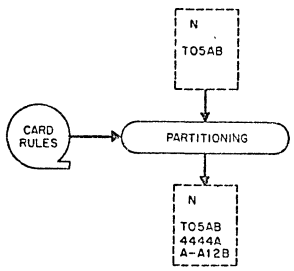


FIGURE 9

8.5.2.1 Partitioning Program. The card rules are generated from the card logic pages during the development and release of cards. The card rules will contain the circuit code, portion and sub-portion designations for each circuit on a card. All cards will be put on the rules.

8.5.2.2 Logic Selection For Partitioning. The Partitioning program is controlled by the selection of certain logic to be assigned to a particular physical environment. This selection is done via the SLDA "Logic Select" program.

8.5.2.3 Requesting Partitioning. When requesting a partitioning run, the following items have to be indicated on the "SLDA PCS" form.

A. Partitioning works on one gate at one time. The frame and gate designation must be given. In addition, boards within the gate may be given. Partitioning will assign cards to these boards. If no boards are given then only the frame and gate will be assigned to the cards.

B. For each board assigned, the engineer must give a limit on the total number of sockets available and the total number of nets which are allowed to leave the board. The program will not exceed these limits. The limits apply to all the logic on the board, whether pre-assigned or put there by the program.

Frame 01 Gate A	Board	Number of Sockets Available For Cards	Number of Nets Allowed To Leave Board
	A1	50	96
	A2	46	80
	A3	52	85

C. The designer may specify that the gate, board, socket, card and portion, and symbolic package fields are to be blanked. This option is specified by proper selection of the "Blanking Options" on the PCS transmittal under the block check/grouping program.

D. It must be specified whether the partitioning run is actual mode or symbolic mode. The partitioning modes are described later in this writing.

E. The cards that partitioning may select from the card rules and assign to the logic selected for the run must be specified.

There are four options available for the engineer to specify those cards which the partitioning program can use.

(a) CMT BY CLASS AND STATUS

(b) ATTACHED LIST ONLY

(c) ATTACHED LIST UNLESS OTHERS ARE NECESSARY

(d) ATTACHED LIST PREFERRED OVER CLASS AND STATUS

These options are treated as follows:

Option (a) The entire CMT (Circuit Master Tape) is examined to find cards which have the same class and status codes as the designer requested.

Option (b) The partitioning program will try to implement the logic using the card list, specified by the designer. A check is performed that all cards on the list are in the card rules and a message may be given "NOT IN RULES". The cards for the list are specified by listing the four character card code. If no card on the list will package a given circuit, the block will be left blank.

Option (c) The program uses both the attached list of cards and other cards selected from the CMT by using the Class and Status codes given by the designer. This option will always use the cards on the list to implement the engineer's logic if possible. If a circuit is encountered by the partitioning program that it cannot package using the cards on the attached list, then the program will go to the cards on the CMT to try and implement the logic.

Option (d) The program again uses both a specific list of cards selected from the CMT by class and status. Everything being equal the program will select a card on the list rather than a card selected by class and status.

F. An option is available to limit the choice of cards selected by class and status to only those with no functional postions.

G. If the Logic Master Tape is to be updated with the output of the partitioning run, the (Update LMT program) must be requested on the SLDA Program Request Form.

IBM

SLDA PACKAGING CHECKING TRANSMITTAL

☐ PARTITIONING FRAME ______ GATE ______ MODE ACTUAL ☐ SYMBOLIC __ __ ______

LIST ERRATA BY < LOGIC PAGE ☐ / ERROR CODE ☐

SELECT PARTITIONING CARDS FROM —[CHECK ONE ONLY]

1 ☐ CMT, BY CLASS AND STATUS
2 ☐ ATTACHED LIST ONLY
3 ☐ ATTACHED LIST, UNLESS OTHERS ARE NECESSARY
4 ☐ ATTACHED LIST PREFERRED OVER CLASS AND STATUS

CLASS AND STATUS
STA ☐ SPR ☐
STR ☐ EXA ☐
SPA ☐ EXR ☐

INDICATE THE CLASS & STATUS OF CARDS FOR OPTIONS 1,3,4
LIST ON BACK OF THIS SHEET CARD LIST NECESSARY FOR OPTIONS 2,3,4

☐ DO NOT SELECT NON-FUNCTIONAL PORTIONS OF FUNCTIONAL CARDS
(OVERRIDDEN IF CARD IS ON LIST FOR OPTIONS 2,3 AND 4.)

BOARD	NUMBER OF SOCKETS AVAILABLE FOR CARDS	NUMBER OF NETS ALLOWED TO LEAVE THE BOARD

☐ PLACEMENT

INDICATE BOARD(S) TO BE PLACED. CROSS OUT SOCKETS NOT AVAILABLE FOR PLACEMENT.
INDICATE WHETHER REPLACEMENT, ADDITIONAL, OR COMPLETE REPLACEMENT
INDICATE WHETHER ALGORITHM, INTERCHANGE, OR BOTH.

☐ COMP
☐ REPL
☐ ADD FR__ G__B__ ☐ ALOG ☐ INTR
2 A B C D E F G H J K L M N
3 A B C D E F G H J K L M N
4 A B C D E F G H J K L M N
5 A B C D E F G H J K L M N
6 A B C D E F G H J K L M N
7 A B C D E F G H J K L M N

☐ COMP
☐ REPL
☐ ADD FR__ G__B__ ☐ ALOG ☐ INTR
2 A B C D E F G H J K L M N
3 A B C D E F G H J K L M N
4 A B C D E F G H J K L M N
5 A B C D E F G H J K L M N
6 A B C D E F G H J K L M N
7 A B C D E F G H J K L M N

☐ COMP
☐ REPL
☐ ADD FR__ G__B__ ☐ ALOG ☐ INTR
2 A B C D E F G H J K L M N
3 A B C D E F G H J K L M N
4 A B C D E F G H J K L M N
5 A B C D E F G H J K L M N
6 A B C D E F G H J K L M N
7 A B C D E F G H J K L M N

☐ COMP
☐ REPL
☐ ADD FR__ G__B__ ☐ ALOG ☐ INTR
2 A B C D E F G H J K L M N
3 A B C D E F G H J K L M N
4 A B C D E F G H J K L M N
5 A B C D E F G H J K L M N
6 A B C D E F G H J K L M N
7 A B C D E F G H J K L M N

620-8200-4

FIGURE 10

8.5.3 PARTITIONING INPUT OPTIONS

8.5.3.1 Program Assignment. Complete program assignment of card portion, board and gate can be done by the partitioning program. The designer using this option leaves the packaging fields of his logic blocks blank and when requesting the partitioning program specifies the logic and physical environment for the run.

EXAMPLE:

BEFORE PARTITIONING	AFTER PARTITIONING
A T03AC	A T03AC 2222B A-A22B

A. In the partitioning example, the packaging fields of the logic block were left blank, the designer requested this logic to be partitioned on gate A, board A2. The partitioning program assigned the circuit to card code 2222, portion B. Also, gate A, board A2 was inserted in the logic block and the card was given pseudo-socket 2B.

B. A Pseudo-Socket is a two character designation given to each card selected by partitioning. This designation is not a legal socket on a board but serves only to uniquely identify the card. The card may be placed in a real socket location either by the engineer or the placement program. Pseudo-sockets are of the following form:

Numeric - alphabetic, or
Alphabetic - alphabetic

They are ordered as follows:

1A, 1B,...1Z, 2A,...9Z, AA,AB,...AZ, BA,...ZZ.

The program assigns pseudo-sockets starting from the highest one found in the data.

C. The Program will also accept certain partial assignments and complete them.

EXAMPLE:

BEFORE PARTITIONING	AFTER PARTITIONING
A T03AC A-A2	A T03AC 222B A-A22B

D. The above example is the same as the previous one except here the designer has assigned the block to the board before running the program.

8.5.3.2 Manual Assignment. Complete manual assignment of a circuit can be done by the designer.

N T05AB 4444A1 A-B2C2

A. This logic block (circuit) has been completely packaged. The partitioning program will not alter the packaging in any manner.

8.5.3.3 Additive Card Code. The Additive Card Code (ACC) for a card shall be indicated in the first four digits of line two of the logic block.

N ACC T05AB

A. The ACC may be either numeric or alphabetic ("000" is not allowed). ACC's are used to control optional cards (board wiring always exists) for a board. ACC cards are listed on individual card distribution lists separate from the distribution list for basic cards of a board. Basic cards or a board have no ACC (blank).

B. The Partitioning Program will not assign logic blocks with different ACC's to the same card. The partitioning program will not assign blocks with an ACC to basic (blank ACC) cards.

8.5.3.4 Summary. The logic blocks of the following figure illustrate a summary of the partitioning program input options. Any one option or combination of options may be used on logic pages for partitioning.

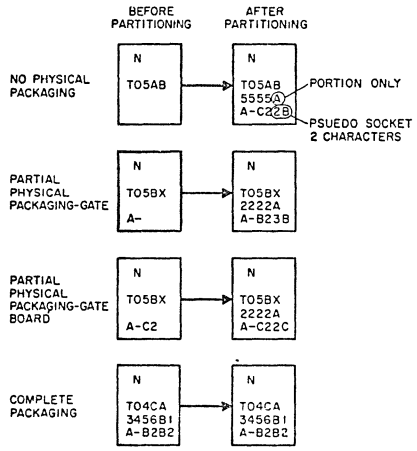


FIGURE 11

8.5.4 PARTITIONING MODES OF OPERATION. The partitioning program operates in one of two modes: Actual or Symbolic.

8.5.4.1 Actual Mode. In the actual mode selected logic is assigned to cards, boards and gates. Each card selected by the program is assigned to a Pseudo-socket in order to distinguish it from other cards. Care must be taken in the selection of data to insure that duplicate pseudo-sockets are not created. For example, if a card on the LMT is not assigned to a board and has pseudo-socket 3F and the highest pseudo-socket in the data selected is 3E then the possibility exists that the program will create a card, call it 3F and will not assign it to a board; either because no boards were given or they were full. If this information is then fed back to the LMT a conflict will exist.

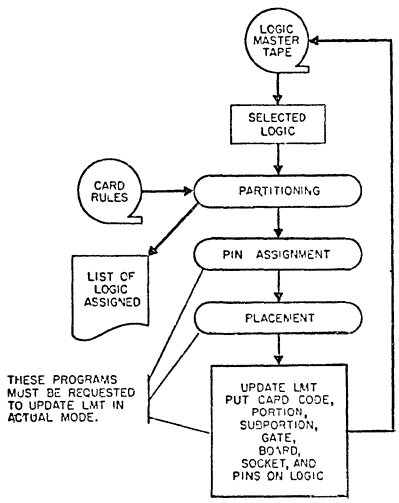


FIGURE 12

8.5.4.2 Symbolic Packaging Mode - Definition. Symbolic packaging is offered as a useful tool to aid in packaging experiments to determine the optimal arrangement. It does this since it furnishes a logical grouping tool which remains constant as various locations are assigned. It also offers a vehicle for holding together sections of logic which must be closely associated for circuit or other reasons in a manner such that the abilities of the partitioning and placement systems can be used.

A. If the engineer desires to package a section of logic that "goes together" he can have this logic packaged onto cards by itself and have all the cards thus created be members of a symbolic package (S.P.). This symbolic package can then, as a group, be assigned and reassigned to various boards by the engineer or by the programs without losing its identity.

B. Special Use of the last two characters of line two is necessary when using symbolic packaging.

```
 OR
    AA
TO4AA
2222A1
A-B2C3
```

SYMBOLIC PACKAGE-AA

C. A Symbolic Package Designation is any combination of alpha and/or numeric characters appearing in the symbolic package field of a logic block.

D. Symbolic Package designations, if used, will be printed and maintained on automated logic pages.

E. Creating a Symbolic Package. A symbolic package can be created by either, (1) manual entry on logic pages or (2) selecting logic with blank symbolic package fields and running partitioning in the symbolic mode. In the symbolic mode, the designer specifies the particular symbolic package on which he desires to have the partitioning program work. All selected logic with blank symbolic package fields will be filled in with the symbolic package specified by the designer.

F. Card and Board Assignment. In the symbolic mode, logic is packaged on cards so that each card contains logic belonging to the specified symbolic package and nothing else. A pseudo-socket is assigned to each card selected by the program. In this case, the pseudo-socket is assigned so that no two cards within the same symbolic package will have the same pseudo-socket.

EXAMPLE:

AFTER PARTITIONING

```
N
   CC
TO7AA
3333A
   1A
```

```
 A
   CC
TO3VV
4444B
   1B
```

G. The Partitioning Program will not assign logic blocks (circuits) to the unused circuits of a symbolic package card unless the symbolic package designation is the same.

H. Cards will be assigned to boards in symbolic mode in the same way as in actual mode.

I. Updating LMT - Symbolic Mode. The Pseudo-socket locations for cards assigned by partitioning are unique for each card of a particular symbolic package. The possibility of two different cards being assigned the same Pseudo-socket on the LMT does not exist in the symbolic mode.

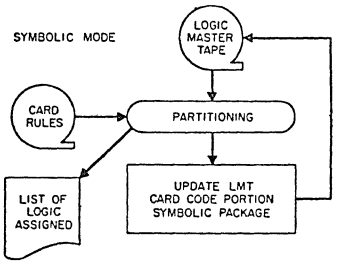
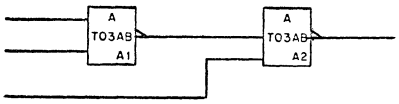


FIGURE 13

8.5.5 FUNCTIONAL PORTIONS

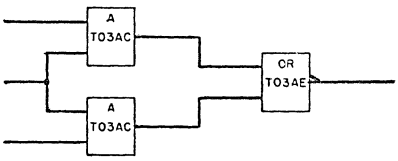
8.5.5.1 SLDA Definition. A functional portion of a card is a portion which either:

(a) Contains circuits which can appear in separate portions.



(b) Has internal bussing.

Example:



The program will never use such portions to package logic.

8.5.6 PROGRAM CAPACITY. Approximately fifteen boards worth of logic can be partitioned on one partitioning run. This amount includes both the selected logic and any other logic already assigned to the specified environment.

8.6 PIN ASSIGNMENT AND CHECKING

8.6.1 Purpose. This program compares logic block data (pins, card code, portion and sub-portion) appearing on systems pages, with the card code rules. It has two modes of operation.

8.6.1.1 The First Mode (assignment) will generate data to automatically update the Logic Master Tape.

8.6.1.2 The Second Mode (checking) will compare the data on systems pages to the card code rules and generate error messages when discrepancies occur.

8.6.2 ASSIGNMENT MODE. Partitioning program is not used.

8.6.2.1 The Following Logic Block Fields on systems pages should be filled in to ensure proper assignment.

(a) Circuit number
(b) Card Code
(c) Portion and sub-portion
(d) Physical location

A. Program has three options.

(a) Assign all pins - it will assign all pins and disregard all pin information that nay have already been filled in.

(b) Additional assignment - Pin assignment will check each portion to see if any pins for those blocks are filled in. If any pin on any sub-portion of a card is filled in, then pin assignment will not be done on any of the blocks within that portion. Instead checking will be done.

(c) Assignment of Pin Tie Downs - This feature provides the automatic tie-down of un-used input and output card pins. These assignments will occur provided that:

1. This option is requested.
2. Either option a. or b. above must also be requested.
3. Circuit rules must have been established which designate to what voltages the unused inputs or outputs must be tied to.

If pin errors occur for a card portion then no tie down assignemnts will be made.

The following figure reflects the workings of the program.

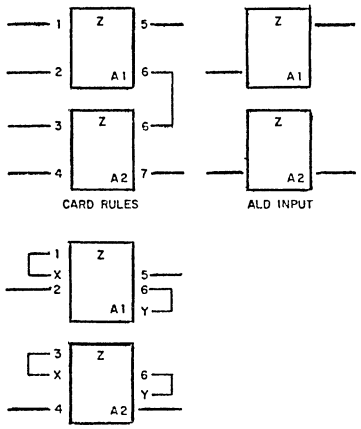


FIGURE 14

8.6.3 CHECKING MODE. The following fields should be filled in to check a logic block:

(a) Circuit number
(b) Card code
(c) Portion and sub-portion
(d) Physical location

1. Frame - gate - board - socket
2. Frame - symbolic package - pseudo-socket.

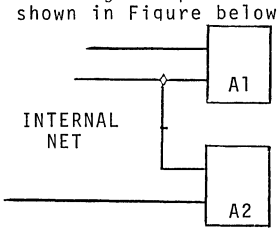
8.6.4 FUNCTIONAL CARDS - GENERAL. The Pin Assignment program will assign pins to complex functional cards. A functional card will usually consist of several internal nets bussing the inputs of various sub-portions; the first portion/ sub-portion is A1. Numbering proceeds from A1 to A9 then AA to AZ excluding I, O and R. If a card has more than 32 sub-portions, then the portions/sub-portions are assigned starting with an all numeric notation in the range of 01 to 99.

8.6.4.1 Limitations. If selecting logically, all pages that effect a portion of a card must be selected in order for pin assignment to assign pins correctly.

A. Whenever the Message, "The following internal nets have been omitted" is given, the possibility exists that the Pin Assignment program has not properly matched internal nets on both ALD's and card rules. The engineer must check his ALD's to insure that proper pin assignment has been accomplished. Several pins may have to be assigned manually by the engineer.

B. If a Functional Card is encountered by Pin Assignment that has an improper circuit number in a logic block with internal nets, the engineer should check his ALD's to see that proper pin assignment has been accomplished. A second pass on Pin Assignment may be necessary because of the circuit number change caused by Pin Assignment of the first pass.

C. When a Designer has omitted a sub-portion of a functional portion, Pin Assignment will make a note of this condition in an Errata message. However, if he chooses both sub-portions, he must show the internal net between the blocks, even if he is not using the pin involved in the net as shown in Figure below.



In the figure above, if the engineer chooses not to use sub-portion A1 he may omit it from his logic page. If he decides to draw A1 on his ALD, he must show the internal connectors between this block and all other blocks that have been drawn.

D. When Errata from Pin Assignment is printed by Logic Page, a misunderstanding may exist for internal net messages. Internal nets are only mentioned on the Errata for the first page encountered on which the portion appears. When sub-portions are scattered over several ALD's, the only message that may appear is "No Assignment on the following pins". The reason for the lack of assignment will appear on the Errata sheet for the fist ALD on which the portion was encountered.

8.7 PLACEMENT

8.7.1 INTRODUCTION. Placement is the SLDA program which assigns cards to specific board sockets. The sockets are chosen to achieve minimal wiring. This program is run after the logic has been partitioned and pins have been assigned. It is desirable to run Placement after connector assignment.

8.7.1.1 The Placement Program operates on one board at a time. The designer has the option to manually assign all or some of the cards to sockets by entering the information in the logic blocks on his logic pages. Placement can also change or reassign sockets for cards which have been previously placed. Placement can handle up to 100 cards and 2000 pins per board, including all connector pins and pins on card sockets to be left fixed.

8.7.2 PLACEMENT OUTPUT. The output from placement is a list showing the results of Placement and the wireability factor. If the engineer desires he can get the wireability factor of a board that he has placed manually by checking ADD and ALOG,(See CEP 0-2815). No cards are placed since there are no pseudo-sockets on the board. The results of placement are put on a tape that can be used to update the engineer's ALD's with the new assignments.

8.8 CONNECTOR PROCESSING

8.8.1 CONNECTOR CHECKING. Selected logic is checked for correct edge connector communication with other boards. The edge connectors are listed by net number to show all connectors from the logic pages and to show those nets which are connected to other boards but have no connector assignments. A check is made to see that the correct number of connectors is shown by following the formula, 2(N - 1), where N = number of boards in the net. If the formula is not satisfied, the message, "Improper number of connectors in the above net", is printed under the list of connectors for the net.

8.8.1.1 The Connector Checking Program will also perform a check to see that all nets in the selected logic have at least 2 pins per net per board. Any single pin will be listed with the following information.

(a) net number
(b) pin type - signal or connector
(c) physical location
(d) block and line for signal pins

8.8.1.2 All nets are checked for those that contain both a real pin and a pin with a designation. All pins in each net meeting this condition are listed in the errata.

8.8.1.3 Connectors that are being used, can be listed by physical location sequence. Associated with each connector listed is the net number and the remaining connectors in the string.

8.8.2 CABLE CONNECTOR ASSIGNMENT AND CHECKING This program requires that cables have been assigned and are recorded as cable blocks on the LMT, and that rules have been established which define cable assemblies and the frame-gate-board descriptions.

8.8.2.1 Functions performed by this program are:

(a) Insure that specified cable types may be used to connect the sockets designated.

(b) Check compatibility between connector pins and cables.

(c) Insure that a net has been completely connected without redundancies.

(d) Assign connector pins for a net when the appropriate cable blocks have been specified for the net, or when the net involves only two boards.

8.8.2.1.1 Outputs from the program are an updated BET (if connector assignment has been done), a listing of cable blocks specifying which connector pins are used and unused, and Errata. The updated BET is used to update the LMT with the connector data.

8.8.3 Connector Assignment. Connector pin assignment can be accomplished in the following ways.

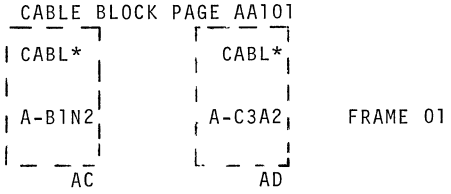
(a) The program can generate all connectors for nets which involve only two boards if a cable is available between the appropriate boards.

(b) The program can generate the second member of a connector pair when one member is already present.

(c) A pseudo-connector of the form 01*AA101AC* can be used to represent a pair of connector pins. This pseudo-connector refers to the page - serial of the "From" cable block involved, (between asterisks) and the frame involved. This pseudo-connector must be recorded on the network involved on the logic pages. They can be recorded in the same manner as regular connectors.

8.8.3.1 The program assigns a pair of actual connector pins from the cable block referred to and these replace the pseudo-connector on the ALD.

EXAMPLE:



ALD
Pg BB101

Connector pair before pin assignment
01*AA101AC*

Connector pair after pin assignment and feedback
01A-B1N2B06
01A-C3A3B06

(a) and (b) in para. 8.2.2 are optional while (c) is always done if a pseudo-connectors are present.

8.8.3.2 Operation. One frame of data can be processed at a time. It is recommended that at least a single gate be processed at a time. This is to insure that the entire set of cable blocks and preassigned connectors for the gate be processed as an entry because the only record of connectors assigned is contained on the ALD. If all pre-assigned connectors are not included in the run, the assignment program could assign duplicates.

A. If Pseudo-connectors are present, the program attempts to assign pins; otherwise the program checks those conditions mentioned above.

8.9 LOCATION CHECKING AND CHARTS

8.9.1 LOCATION CHECKING. Location checking is a program in the packaging and checking system that will check selected logic pages or physical locations for several error conditions.

8.9.1.1 Conditions Checked by Location Checking Are:

A. When the Cable Rules (CMT) are used, each socket will be checked to see if it is a legal card, connector, cable, or cross-over socket.

B. Two different Card Types in the same socket on a board.

C. A Card and a Connector in the same socket in a board.

D. A Card Type not mentioned on the rules tape (CMT).

E. A Blank Card Code in a socket.

F. Different Net Numbers having identical connector pins.

G. Portions used but not mentioned on the rules tape (CMT).

H. Portion and Sub-portions used with more than one logic block in the same socket.

I. Unused Portions.

J. A Pseudo-socket (i.e., Num-Alpha, 1A) in a logic block.

K. Missing Frame, Gate, Board or Socket designation on the selected logic blocks.

L. Two different ACC's (Additive Card Codes) associated with the same socket.

In addition to the checking, Location chart(s) will be printed showing the socket locations and card types used for each physical board. In each socket an S or ERR can also be printed. The "S" stands for space portions on the card type shown. The "ERR" stands for an error in the card socket, such as 2 different card types that were found by the program to be occupying the same socket. Any numeric or pseudo-sockets encountered will print out, in the form "1 A WONT FIT". In addition to the chart, a location listing will be printed out showing the logic page locations that make up each card socket or connector socket. A card count is given for each board that was selected. In the sequence of PCS programs, the Location Checking Program is the last program run. This allows an engineer to run Partitioning, Pin Assignment, Placement, and Location Checking, and come out with a location chart that shows the final results of the above sequence of programs.

M. In Addition to the listing shown, a list of each pin in a socket is printed out. This list gives the box character in the ACC field.

9. PHYSICAL MASTER TAPE SYSTEM

9.1 GENERAL DESCRIPTION OF SYSTEM. The printed circuit design of a board is accomplished by extracting logic net information from the logic master tape, updating the physical master tape, and processing this information through the board wiring programs.

9.1.1 A Single Physical Master Tape (PMT), will exist for each machine type in development. This PMT will be generated and subsequently updated from the Logic Page Master Tape (LMT) under the control of the machine development group. All physical information recorded on the LMT is transferred to the PMT, and recorded there in "raw" form. Detailed physical designs (such as wiring) are created from this "raw" data and are also recorded on the PMT.

9.1.2 The PMT Programs will:

9.1.2.1 Record Historic Physical Designs and generate "logical" add/deletes to more recent designs.

9.1.2.2 Check Basic to Version as well as version to version physical conflicts.

9.1.2.3 Design Printed Wiring

9.1.2.4 Prepare Manufacturing Release Interface Tapes - to enable rapid conversion by manufacturing "Process Automation" of this data to finished boards, and required manufacturing paperwork.

9.1.2.5 Prepare Secondary Documents for engineering reference such as wiring and location lists.

9.2 PMT CAPABILITIES. The PMT can retain the physical design while many experimental changes are carried on with the LMT. When the design is firm, it can be transferred to the PMT and implemented. In addition to the above, manual creation and updating of a PMT is provided so that test boards which are not supported by logic pages can be processed.

9.2.1 Updating from LMT - General Description. The transfer of the LMT data to the PMT should be attempted only after extensive use of the LMT and PCS systems has insured a sound design.

9.2.1.1 All of the Data for either the basic or version design being considered is transferred. The data is sequenced in physical location order and is kept as adds and and/or deletes to the previous level. It is recorded under a specific transfer level number (the most recent 7 character engineering change number found on the LMT plus a 1-character suffix).

9.2.1.2 Whenever a Transfer Level becomes a release level, the engineer should request that the LMT used be held until a logic page interface tape can be prepared for release.

9.2.1.3 Approximately 500 levels of design (history) can be handled within the PMT system.

9.2.1.4 Physical conflicts are detected at the time of PMT updating and are forwarded to the engineer in the form of ERRATA lists. Conflicting data will not be transferred to the PMT.

9.2.2 Types of Data Processed. All logic blocks which conform to the usual format, i.e., contain logic function, circuit number, card code, machine location, are processed and recorded on the PMT.

9.2.2.1 Generally all logic blocks which are referred to as special block representations and are identified by an asterisk (*) in the sixth position of line one within the block are not processed or recorded on the PMT. An exception, however, is the special wiring block which has a line one identifier (SERV*). The block is used for the purpose of submitting special service wiring requirements which supplement the regular board voltage plane distribution and are implemented as printed wires. The existence of these blocks will not cause conflicts to be noted if cards or connectors are plugged in the same location.

9.2.3 Program Limit.

(a) Board matrix cannot exceed 107 x 71 pins and holes.

(b) Number of nets on a board cannot exceed 1000.

(c) Number of pins used on a board cannot exceed 3000.

(d) Number of pins per net cannot exceed 100.

(e) Number of Pins/Card socket-300.

(f) Maximum manual brackets-2000.

(g) Reserved area-50.

(h) Maximum discrete Wires/Board-400.

(i) Number of transfer levels cannot exceed 500.

9.2.4 Board Interface Tape. An interface tape will be developed upon request of the engineer or engineering records. This request must contain:

(a) Machine type

(b) Board locations

(c) Transfer level(s) of Boards - Transfer level is the logical design level of the board at the time the data was transferred from the LMT and recorded on the PMT.

9.2.4.1 The data for an individual board is broken down into 10 different groups in the following sequence. This information is repeated for each board which is being processed by Design Automation.

(a) General Board Specifications
(b) Production Controls
(c) Wiring Image
(d) Card Data
(e) Discrete Wires
(f) Net List Data
(g) Unused Pins
(h) Service Voltage Pins
(i) Card Add/Delete
(j) Board Field Rework data

NOTE: For a detailed description of the Manufacturing Interface tape as to field lengths and actual tape formats refer to CEP 0-2815-8 "Processing Control Implementation Program."

9.2.5 Outputs from Updating. The outputs produced from each update are:

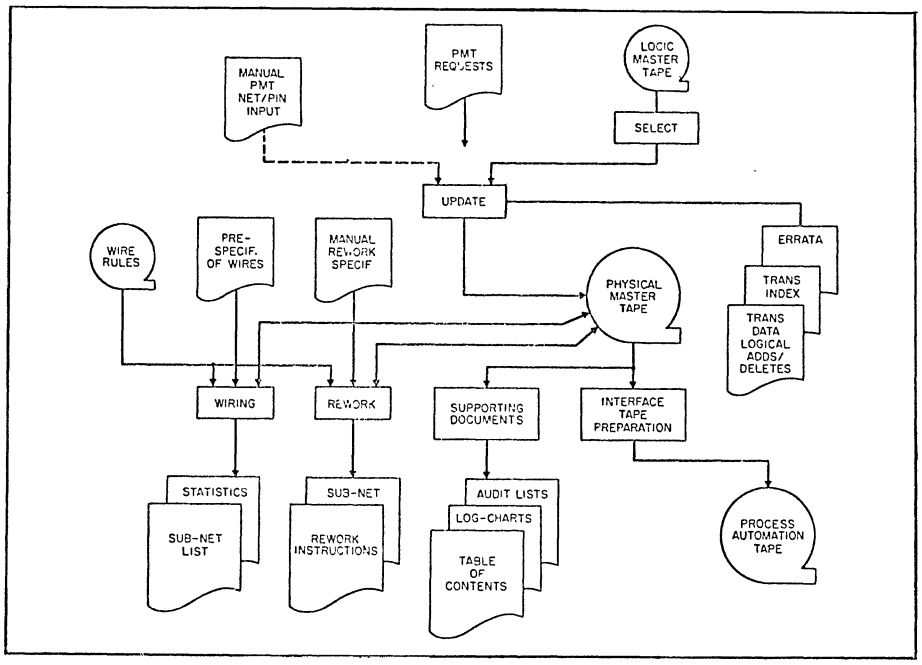
(a) Transfer level index. This is an index of the levels which are recorded on the PMT.

(b) Logical add/delete listing - this indicates the cards and pins affected in the update and indicates those items which were not transferred.

9.2.6 Manual Update of PMT. For the purpose of generating test boards which are not supported by logic pages, a PMT can be created and updated manually.

9.2.6.1 A manually created or updated PMT can be updated from logic pages. Once this is done, however, the PMT can no longer be updated manually. Further updating must be done through logic pages.

9.2.6.2 Output from the manually generated PMT is the same as if the conventional LMT input is used.



PHYSICAL MASTER TAPE SYSTEM

FIGURE 15

9.3 WIRE ROUTING

9.3.1 PRINTED WIRING DESIGN PROGRAM. This program designs the printed wiring for the two signal plane board(s) so that the pins within each network are electrically connected. Those pins between which printed paths weren't available are connected by yellow wire.

9.3.1.1 Two Modes of Wiring Are Available with many options within each. They are:

(a) Original wiring in which the entire set of pins for the board(s) are wired and;

(b) Rework wiring in which the changed pins are applied to some previous design level.

9.3.1.2 All Wiring Designs are Recorded on the PMT for the purpose of retaining it for future rework and for the subsequent requests for a process automation interface tape.

9.4 ORIGINAL WIRING

9.4.1 General Description. Board wiring designs must be classified into either of two categories with respect to characteristics of the interconnections made between the pins. They are:

(a) Point-to-point wiring. Each wiring segment connects only two pins. (Equivalent in characteristics to yellow wire connections.)

(b) Multi-ended wiring. Each wiring segment connects two or more pins.

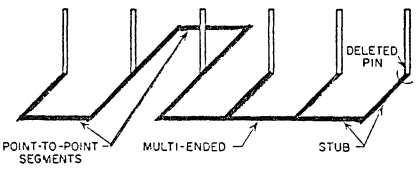


FIGURE 16

9.4.2 The type of design that should be chosen is determined from a consideration of the specifications for the circuits and card types used. The original wiring choice should also consider whether or not stubs can be allowed when the board is reworked.

(a) If stub wiring cannot remain on a board after rework, point-to-point wiring must be used. (Rework procedure provides the proper instructions to insure no stubs.)

(b) If stubs can remain on the board after rework then multi-ended wiring can be used.

9.4.3 The significant difference between point-to-point wiring and multi-ended wiring is that more yellow wires are required to complete the point-to-point wired boards.

9.4.4 Once designed, a board can be reclassified from the point-to-point type to the multi-ended type only.

9.4.5 On original wiring no more than two yellow wires will be connected to a pin and the absolute maximum number of printed connections is eight. Exceptions to the above is when certain nets are controlled by special wiring rules and manual input. Special wiring rules can force three yellow wire connections to a pin. Manual input can force any number of yellow wire connections to a pin. It is pointed out that the control of the number of yellow wire wraps on a pin specified via manual input remains with the designer.

9.4.6 Additional options which can be used by the engineer to govern the wiring design are:

(a) Quality Wiring - enables a trade-off between computer running time and success of printed wire designs.

(b) Pre-specified connections (printed and yellow) - enables the pre-routing of printed wires and the pre-specification of yellow wires.

(c) Reserved areas - the program inhibits routing printed wires through these designated areas

(d) Special wiring rules -dictates the configuration of wiring (branch or point-to-point)for critical circuits and also provides messages when critical wiring lengths are exceeded.

10. VERSION PROCESSING

10.1 GENERAL DESCRIPTION OF VERSION MODE OF OPERATION. The version process is intended to assist in the design of computer systems which are variations to original designs. All original designs are called "basic"designs. All modified designs are called "version" designs.

10.1.1 The SLDA System will provide the same facilities to the designer of a version machine as to the basic machine designer. There are two ways in which it can do this:

10.1.1.1 Version Consideration (New Design). The "Version" can be considered an entirely new design, assigned a new logical name (machine type #) and a separate set of pages and hardware used to define it. This is the same way in which separate basic designs are handled, and the word version is not used to describe such a process.

10.1.1.2 Version Consideration (Basic Design). The version can be considered as superimposed on the basic design, in which case only the differences between the basic and version design are recorded. Such a method of operation results in several advantages:

(a) New pages and hardware need be produced only in the areas where the basic design has been modified.

(b) Changes to the basic in those areas not impacted by the version can be automatically applied to the version.

(c) As design changes occur, conflicts between versions, or between basic and versions, can be readily detected.

(d) Correlation between the documentation of the basic and version designs is aided (i.e., "similar to" notes on logic pages, composite tables of contents, etc.).

10.1.2 Two types of versions are handled. (1) single version design and, (2) combination version design, which is the combination of two or more single versions. The redesign necessary to provide a combination is recorded as such and all unaffected basic or single version logic data remains intact.

IBM **Location Manufacturing Practice**

INTRODUCTION

1.1 SCOPE. This practice introduces the (MPS) Modular Power Supplies and their physical and electrical characteristics.

1.2 OBJECTIVE. This practice is published as an aid to the SLT Designer in the selection of power supplies.

1.3 DEVIATION APPROVAL. Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 6/68.

1.5 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

1.6 SUPERSESSION. This Practice supersedes LMP 0-2860-085, dated Jan. 67.

RECOMMENDED PRACTICES

2. POWER SUPPLIES

2.1 General. The (MPS) Modular Power Supplies were found to be most suitable for usage because they:

a. require no ferro-pac
b. use Line Voltage input
c. are similar in size to SMS Power Supply
d. mount on rails - same as SMS

2.2 Packaging & Cooling

2.2.1 It is recommended that the MPS power supplies be mounted in a chassis so that the heat sinks on opposing power supplies face each other, forming a chimney for air convection. (See Figure 1).

2.2.2 Two recommended methods of cooling the power supplies are:

1. Ducting air from the base blower in the cabinet to a plenum on the bottom of the chassis.

2. Mounting a fan to a plenum on the chassis, locating it under the heat sinks.

2.2.3 It is recommended that some sensing device be incorporated to protect the power supplies from overheating (maximum outlet temperature: 55°C). For unit lengths and rail mounting hole dimensions, See Table I.

2.3 Electrical Characteristics.

2.3.1 These supplies are self-contained, modular units that generate a regulated DC voltage designed to power solid state logic and control circuits. These supplies have floating outputs and may be used either as positive or negative supplies.

2.3.2 All inputs are single phase, 50 or 60 nz, and 115, 208, or 238 volts ±10% RMS sinusoidal input. Provision must be made by the user to provide input power protection by use of a circuit protective device.

Recommended Power Supply Mounting For Chimney Effect

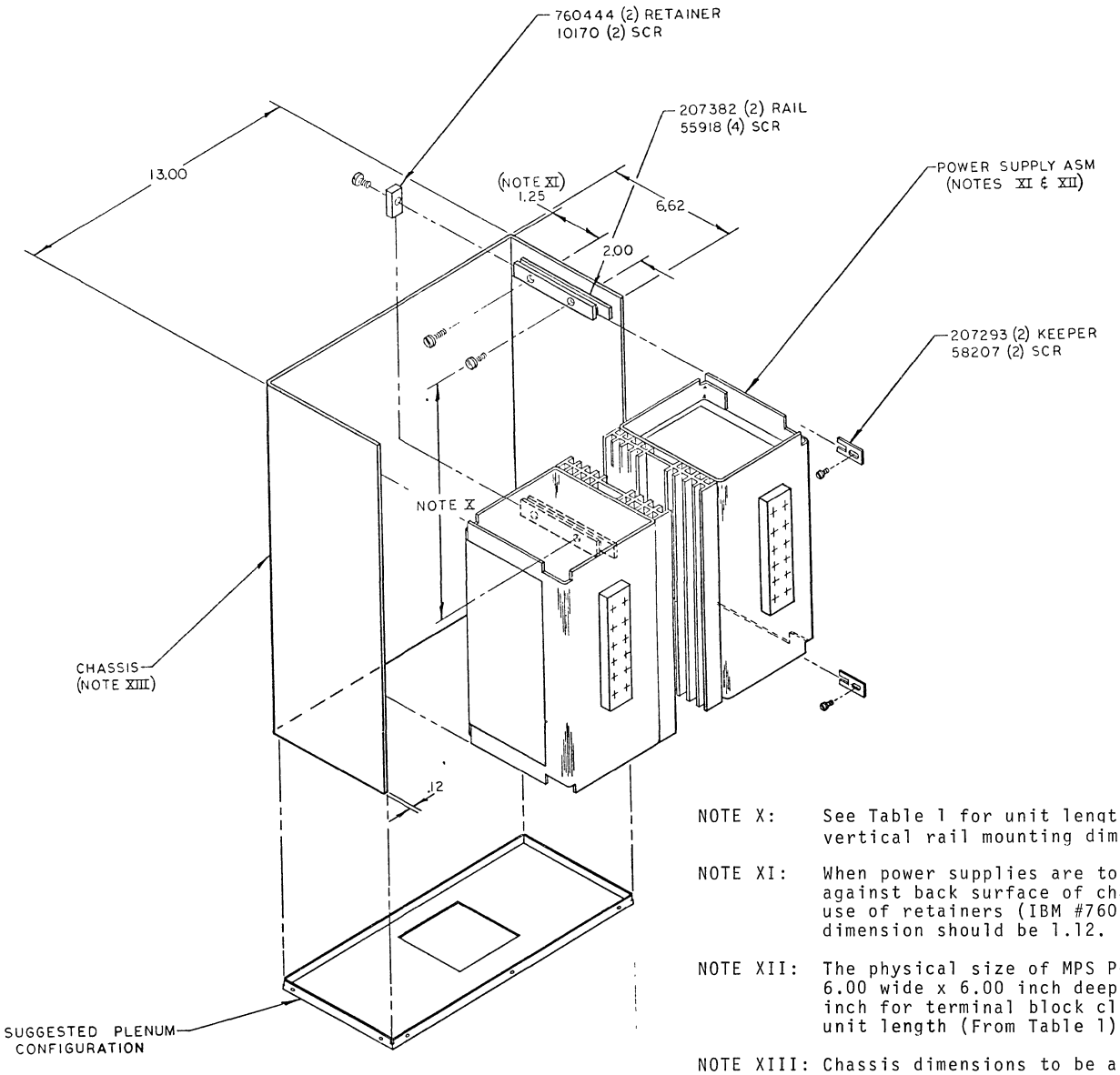


FIGURE 1

NOTE X: See Table 1 for unit lengths and vertical rail mounting dimensions.

NOTE XI: When power supplies are to be mounted against back surface of chassis without use of retainers (IBM #760444), this dimension should be 1.12.

NOTE XII: The physical size of MPS Power Supplies 6.00 wide x 6.00 inch deep (add 0.44 inch for terminal block clearance) x unit length (From Table 1).

NOTE XIII: Chassis dimensions to be as indicated - with height determined by physical requirements.

3. The following Table #1 lists the recommended modular power supplies available.

Supply Assembly	Freq. (HZ)	Output Volt(V)	Output Current(A)	Regulator Card Assembly	Regulation (%)	Overvolt. Protect. (Note 1)	Overcurrent Protect. (Note 1)	Remote Sense	Size In.xIn.xIn. (Note 2)	Performance Spec.	Wiring Diagram
5239400	60	3	4	375200	2	X	--	X	6x6x9	5261005 877196	5261001
5239418	50	3	4			X	X	--	6x6x9	5261605 877196	5261001
5239401	60	3	8			X	--	X	6x6x11	5261015 877196	5261011
5239419	50	3	8			X	--	X	6x6x11	5261615 877196	5261011
5239402	60	3	12			X	--	X	6x6x12	5261025 877196	5261021
5239420	50	3	12			X	--	X	6x6x12	5261625 877196	5261021
5239403	60	3	16			X	--	X	6x6x14	5261035 877196	5261031
5239421	50	3	16			X	--	X	6x6x14	5261635 877190	5261031
5239406	60	6	3	375203		X	--	X	6x6x9	5261195 877190	5261191
5239424	50	6	3			X	--	X	6x6x9	877119 877190	5261191
5239407	60	6	6			X	--	X	6x6x11	5261045 877190	5261041
5239425	50	6	6			X	--	X	6x6x11	5261645 877190	5261041
5239409	60	6	12			X	--	X	6x6x14	5261055 877190	5261051
5239427	50	6	12			X	X	X	6x6x12	5261655 877190	5261051
5239410	60	6	15			--	X	X	6x6x17	877176 877190	5253871
5239428	50	6	15			--	X	X	6x6x17	877177 877190	5253881
5760610	60	6	15	374621		--	X	X	6x6x14	876245 877190	5760611
5760690	50	6	15	374621		--	X	X	6x6x14	876243 877190	5760611
5239411	60	6	18	375203		X	--	X	6x6x20	5261065 877190	5261061
5239429	50	6	18	375203		X	--	X	6x6x20	5261665 877190	5261061
5738307	60	6	18	374621		--	X	X	6x6x20	876235 5261065	5738311
5239110	50	6	24	375203		--	--	X	6x6x23	876173	5239101
5239100	60	6	24	375203		--	--	X	6x6x23	876172	5239101
5709440	50	9	10	374922		--	X	X	6x6x14	876097 876174	5709441
5709480	50	9	10	374922		--	X	X	6x6x14	876098 876174	5709441

TABLE I

Supply Assembly	Freq. (HZ)	Output Volt(V)	Output Current(A)	Regulator Card Assembly	Regulation (%)	Overvolt. Protect. (Note 1)	Over-current Protect. (Note 1)	Remote Sense	Size In.xIn.xIn. (Note 2)	Performance Spec.	Wiring Diagram
5239412	60	12	2.5	375161	2	--	X	X	6x6x9	5261075 876174	5261071
5239430	50	12	2.5			--	X	X	6x6x9	5261675 876174	5261071
5239431	50	12	5			--	X	X	6x6x11	877118 876174	5261141
5239413	60	12	5			--	X	X	6x6x11	877117 876174	5261141
5253900	50	12	5			--	X	X	6x6x11	877177 876174	5253891
5253890	60	12	5			--	X	X	6x6x11	877117 876174	5261141
5239432	50	12	7.5			--	X	X	6x6x12	877115 876174	5261121
5239414	60	12	7.5			--	X	X	6x6x12	5261125 876174	5261121
5239433	50	12	10			--	X	X	6x6x14	5261685 876174	5261081
5239415	60	12	10			--	X	X	6x6x14	5261085 876174	5261081
5239416	60	12	12.5			--	X	X	6x6x17	377161 876174	5261171
5239434	50	12	12.5			--	X	X	6x6x17	877162 876174	5261171
5239417	60	12	15			--	X	X	6x6x20	5261135 876174	5261131
5239435	50	12	15			--	X	X	6x6x20	877116 876174	5261131
5738320	60	12	18			--	--	X	6x6x20	876238	5738321
5709430	60	15	2.5	374923		--	--	X	6x6x9	876093	5709431
5709470	50	15	2.5	374923		--	--	X	6x6x9	876094	5709431
5253930	60	15	13	375204	5	X	--	X	6x7x17	876162	5253931
5253940	50	15	13	375204	5	--	--	X	6x7x17	876163	5253931
5253950	50	18	4	374774	2	--	--	X	6x6x11	877140	5253951
5253850	60	18	4	374774		--	--	X	6x6x11	877139	5253851
5253960	50	20	8	375205		--	--	X	6x6x17	877135	5253961
5253860	60	20	8	375205		--	--	X	6x6x17	877134	5253861
5261090	60	30	2	375206		--	--	X	6x6x11	5261095	5261091
5261690	50	30	2	375206		--	--	X	6x6x11	877113	5261091
5261150	60	36	1	374568		--	--	X	6x6x9	5261155	5261151
5261750	30	36	1	374568		--	--	X	6x6x9	877175	5261151
5261100	60	36	2	375206		--	--	X	6x6x11	5261105	5261101
5261700	50	36	2	375206		--	--	X	6x6x11	877114	5261101
5261160	60	36	3	374568		--	--	X	6x6x12	876164	5261161

Supply Assembly	Freq. (HZ)	Output Volt(V)	Output Current(A)	Regulator Card Assembly	Regulation (%)	Overvolt. Protect. (Note 1)	Overcurrent Protect. (Note 1)	Remote Sense	Size In.xIn.xIn. (Note 2)	Performance Spec.	Wiring Diagram
5261760	50	36	3	374568	2	--	--	X	6x6x12	876165	5261161
5261180	60	36	4	374568	↓	--	--	X	6x6x14	876102	5261181
5261780	50	36	4	374568	↓	--	--	X	6x6x14	876103	5261181

TABLE I (CONTINUED)

NOTE 1: Overvoltage and overcurrent protective devices are included in the MPS final assembly if indicated by (X).
NOTE 2: Vertical rail mounting dimensions are obtained by adding 0.38 inches to the length given in the table, i.e., 6x6x9 becomes 6x6x9.38.

INTRODUCTION

1.1 SCOPE. This practice outlines the application limits of the various devices within the power distribution system which includes all conducting media from the point of entry at the laminar bus to the exit pins on the boards and establishes voltage decoupling requirements.

1.2 OBJECTIVE. This practice seeks to establish design criteria and basic ground rules for distributing power and signals within the SLT package.

1.3 REFERENCE. The majority of information contained herein may be found in Engineering Specification 811800.

1.4 AUTHORIZATION. This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION. Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

1.6 DEVIATION APPROVAL. Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

RECOMMENDED PRACTICE

2. VOLTAGE TOLERANCES

2.1 POWER SUPPLY TOLERANCES

2.1.1 Power supplies for the 30 nanosecond family must regulate to within ± 2% of the nominal value.

2.1.2 Power supplies for the 700 nanosecond circuit family must regulate to within ± 5% of the nominal value.

2.1.3 The power supply tolerances include dynamic line changes, dynamic load changes, ripple and thermal drift and are to be determined by measuring at the supply terminals.

2.1.4 When remote sensing is necessary, such remote sensing point will be defined at or near the lateral center of the distribution plane, which is that area at the logic gate or frame that is serviced by a group of power supplies supplying power to the same group of boards and sharing the same ground return path. Conductors assigned solely to the sense function should be routed from the supplies to the designated sense point.

2.1.5 Standard Voltages for SLT application are +3, -3, +6M, for the 30 nanosecond circuit family and +12, +12M for the 700 nanosecond circuit family.

2.2 DISTRIBUTION SYSTEM TOLERANCE

2.2.1 The distribution system shall be responsible for not more than 2% variation from the normal voltages. The tolerance is measured at the card socket. The d.c. ground shift is measured from the input to the laminar bus, to the card socket. Ground and voltage transients are held to specified values by card decoupling.

2.2.2 To establish a distribution system that will meet the requirements as set forth in this document, values of load current for a given supply voltage were determined from several representative machines. Each six-pack socket position was assigned the same value of load currents and a uniformly distributed load condition was assumed.

2.2.3 Power supply, distribution system, and transient noise tolerances for the various circuit families are given in Figure 1 and Table 1.

*Measured from a voltage pin to the ground pin on the board within the same six-pack socket location and shall not exceed the limits A_1 and t_1 or A_2 and t_2.

**Measured from a voltage pin of a module to the board ground pin within the same six-packet socket location and shall not exceed the limits A_1 and t_1 or A_2 and t_2.

NOTE
The exact d.c. level of the "nominal voltage" shown in Figure 1 must be established when making noise measurements. Noise is measured from this measured d.c. level. Positive or negative noise is determined as shown in Figure 1.

2.2.4 A combined a.c. and d.c. ground shift between any two points within a page or gate in any circuit family, shall not exceed 100 millivolts.

2.2.5 The combined a.c. and d.c. ground shift between the ground pin of any module and the board ground pin within the same six pack socket location shall not exceed:

a.	30 nsec family	100 mv
b.	700 nsec family	200 mv

2.2.6 Noise will be kept within the limits stated in Sections 2.2.3 and 2.2.4 if decoupling is applied as stated in Section 10.

TABLE 1

Family (Nanoseconds)	Voltage-to-Ground * (On Board)	Voltage-to-Ground ** (On Card)
30	a. A_1 = 100 mv; t_1 = 40 nsec b. A_2 = 200 mv; t_2 = 20 nsec	a. A_1 = 250 mv; t_1 = 40 nsec b. A_2 = 500 mv; t_2 = 20 nsec
700	a. A_1 = 250 mv; t_1 = 100 nsec b. A_2 = 500 mv; t_2 = 50 nsec	a. A_1 = 500 mv; t_1 = 100 nsec b. A_2 = 1 volt; t_2 = 50 nsec

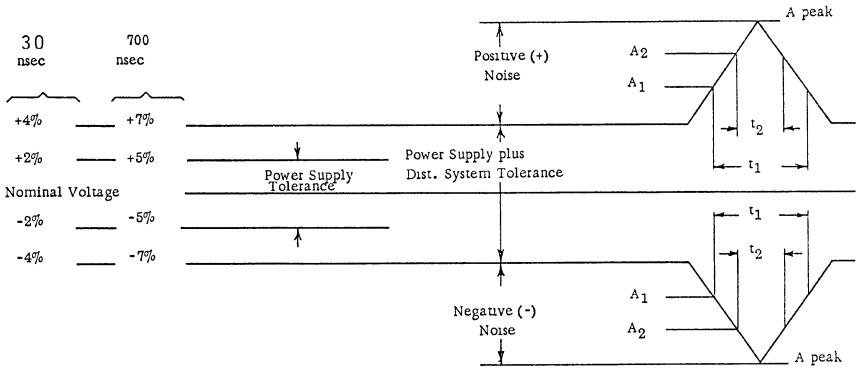


FIGURE 1

2.2.7 All voltage distribution media are rated for 90 volts d.c., capable of withstanding for one minute, without breakdown, 900 volts rms.

1. For applications of 0-90 volts d.c.: Ten times the rated voltage but not less than 100 volts rms.

2. For applications higher than 90 volts: The test voltage is three times the rated voltage but not less than 900 volts rms.

2.2.8 The voltage distribution system does not provide for the integration of 700 nanosecond family circuits with faster circuit families within the same board.

2.2.9 When 700 nanosecond family circuits are integrated with faster circuits within the same gate, the different families of circuits shall be located so that voltage distribution for both is practical.

3. LAMINAR BUS ASSEMBLY

3.1 GENERAL

3.1.1 The laminar bus assembly is made to the applicable drawings (See Figure 2). Characteristics are given in Section 11.

3.1.2 Six of the 12 conductors in the assembly are used to distribute standard voltages and ground in the 30 nanosecond application as follows:

(1) One conductor for each of +3, -3, +6 volts and each return.

3.1.3 Eight conductors are used to distribute standard voltages in the 30 nanosecond 2-Hi card application as follows:

1. One conductor for each of -3 volts and return.
2. One conductor for each of +6 volts and return.
3. Two conductors for each of +3 volts and return.

3.1.4 Four conductors are used to distribute standard voltages in the 700 nanosecond application as follows:

1. One conductor for each +12, +12M and each return.

3.1.5 All conductors not used for distribution of standard voltages may be used for distribution of special voltages, (See Figure 3).

3.1.6 The bus will be available with less than 12 conductors.

3.2 HORIZONTAL BUS ASSEMBLY

3.2.1 The horizontal assembly has 12 conducting layers and is designed for the distribution of d.c. power across the top and/or bottom of a gate or page in a machine.

3.2.2 The horizontal assembly is "L" shaped and has terminal tabs on the short leg which are connected to the power source. Terminal tabs along the major leg are provided for connecting to the vertical assemblies, (See Figure 4).

3.3 VERTICAL BUS ASSEMBLY

3.3.1 The vertical bus assembly has 12 conducting layers and is designed for distribution of d.c. power along the vertical boundaries of boards within a page or gate in a machine.

3.3.2 The vertical assembly is "L" shaped and has terminal tabs, on the short leg, which connect to the horizontal assembly. Power may be fed from the power supplies to the short leg by discrete wires. Tabs are provided along the major (vertical) leg for feeding d.c. power to the boards by means of voltage crossover connnectors.

3.3.3 In the 30 nanosecond, 1-Hi card application the vertical bus assembly shall not exceed three board lengths and shall feed a maximum of three board columns on each side (18 boards maximum per vertical bus).

3.3.4 In the 30 nanosecond, 2-Hi card application the bus assembly shall not exceed three board lengths and shall feed a maximum of two board columns on each side (12 boards maximum per vertical bus).

3.3.5 In the 700 nanosecond, 1-Hi card applications the vertical bus assembly shall not exceed 3 board lengths and shall feed a maximum of 3 board columns on each side (18 boards maximum per vertical bus assembly).

3.3.6 In the 700 nanosecond, 2-Hi card application the vertical bus assembly shall not exceed 3 board lengths and shall feed a maximum of 2 board columns on each side (12 boards maximum per vertical bus assembly).

4. MINI-BUS

4.1 DESCRIPTION

4.1.1 The mini-bus consists of two flat conductors separated by a thin strip of dielectric material. Tabs are formed on the conductors at various intervals as required.

4.1.2 Slip-On devices are connected to the tabs, thus making the assembly a pluggable device for use on the probe side of boards. Any number of slip-ons, up to eleven, may be installed on one assembly, (See Figure 5).

4.1.3 Characteristics of the mini-bus are given in Section 11.

4.2 APPLICATION.

4.2.1 The mini-bus may be used to distribute one special voltage and ground, or two special voltages.

4.2.2 Two or eleven slip-ons are located on the mini-bus assembly to satisfy the requirements of the application. Assemblies available by part number:

Pin	Description
813263	2 position
813264	3 position
813265	4 position
813266	5 position
813267	6 position
813268	7 position
813269	8 position
813270	9 position
813271	10 position
811065	11 position

4.2.3 The mini-bus assembly is installed horizontally on the probe side of the board, between any two rows of pins. Connection to the laminar bus is by discrete wire, (See Figure 3).

5. INTERNAL PLANES

5.1 DESCRIPTION

5.1.1 Internal conducting planes consist of one ounce (per square foot) copper sheets laminated within the board material.

5.1.2 Two internal planes are laminated within the board. One is voltage distribution plane: the other is a voltage return and ground plane, (See Figures 6 & 7).

5.1.3 Connection to the internal planes is by means of plated-through holes and/or pins.

5.1.4 Connection from plane to plane within a board is by means of plated-through holes.

5.1.5 Connection from the conducting planes to circuits not within the board are made through pins.

5.1.6 Internal planes may be modified or customized for special applications. In such case, the design and adherance to specified electrical tolerances are the responsibility of the user.

5.1.7 The voltage plane may be used to distribute special voltages when such use does not interfere with other assignments.

5.1.8 Point-to point resistances within the internal planes are shown in Table 2.

TABLE 2

From pin loc.	To pin loc.	Service		Resistance Milliohms
		30 n.s.	700 n.s.	
Voltage Plane				
B2A14	M2A14	+6	+12M	13.0
B3A01	M3A01	+3	+12	12.0
B3E01	M3E01	-3	Not used	36.0
Ground Plane				
B2E14	M2E14	GND	GND	6.0

6. VOLTAGE CROSSOVER CONNECTOR

6.1 DESCRIPTION

6.1.1 The voltage crossover connector is a short four conductor jumper cable used to feed d.c. power to the board in the SLT package.

6.1.2 There are two types of voltage crossover connector assemblies available to provide voltage and ground distribution from a vertical lamination bus assembly to adjacent boards. The two types are: Voltage Crossover With Decoupler, and Voltage Crossover Without Decoupler. The part numbers for the two types and their related use are as follows:

With Decoupler

P/N	Description
813077	Board to bus to board
813080	Bus to board, right
813081	Bus to board, left
813083	Board to board (30-700 nsec only)

Without Decoupler

P/N	Description
811621	Board to bus to board
811483	Bus to board (left or right)
811482	Board to board (30-700 nsec only)

In addition to the crossovers with decoupling, a Voltage Decoupler Assembly, P/N 813076, may be used in the unused voltage crossover board positions. The Decoupling Capacitor Assembly P/N 811600 is planned to be obsoleted if systems users do not indicate a continuing need for it.

6.2 BUS-TO-BOARD CONNECTION

6.2.1 Five connectors shall be used to carry d.c. power from the vertical laminar bus to each board served directly. The connectors engage pins on the probe side of the board in the areas of columns B and M, (See Figures 8 & 10).

6.2.2 The voltage crossover connector may be used to carry special voltages or voltages from the laminar bus to the board when one or more of the conductors are not assigned to other service.

6.3 BOARD-TO-BOARD CONNECTION

6.3.1 Five connectors shall be used to carry power laterally from a board to an adjacent board. The voltage crossover connectors are installed on the probe side of the board, in the areas of columns B and M, (See Figures 9 & 10).

6.3.2 The voltage crossover connector may be used to carry special voltage or voltages from board to board when one or more conductors are not assigned to other service.

6.4 ELECTRICAL CHARACTERISTICS

6.4.1 Electrical characteristics are given in Section 11.

7. DISCRETE WIRES

7.1 DESCRIPTION

7.1.1 Discrete wires are individual conductors used to interconnect two circuits. Connection may be by wire-wrap, solder, weld, or slip-on devices.

7.1.2 The following voltage and signal connectors are soldered or crimped to discrete wires and slip on the board pins:

P/N	Description
813198	Connector-Discrete Wire Slip-On Ref. Dwg.
813194	Connector-Discrete Wire Slip-On, 20-18 AWG
813195	Connector-Discrete Wire Slip-On, 26-24-22 AWG
813196	Connector-Discrete Wire Slip-On, 30-28 AWG
813197	Housing-Discrete Wire Connector (accommodates 2 connectors)
813810	Connector-Single Discrete Wires Slip-On, 26-24 AWG (uninsulated)
813444	Connector-Single Discrete Wire Slip-On, 30-28 AWG (uninsulated)

7.2 APPLICATION

7.2.1 Engineering changes and field repairs will be made with No. 30 AWG solid wire similar to Part No. 811425.

7.2.2 In the absence of voltage crossover connectors, the ground of horizontally adjacent boards will be interconnected by five discrete wires installed on the probe side.

7.2.3 The grounds of vertically adjacent boards will be interconnected by four discrete wires installed on the probe side.

7.2.4 Discrete wire will be used to make the connection from the laminar bus to the board pins.

7.2.5 (Ref. to Section 11 for characteristics).

8. PRINTED LINES

8.1 DESCRIPTION

8.1.1 Printed lines are located on the outer conducting planes of card and boards.

8.1.2 Printed lines on boards and cards are .0020 to .0028 inch in thickness. Minimum spacing between adjacent lines is .010 inches.

8.1.3 Line width is:

(a) $.008 \pm .002$ inches on boards

(b) $.013 \mp .000$ $.031 + .000$ inches
$- .005$ $- .005$ on Cards

8.1.4 Lines not specified in 8.1.3 cannot be programmed and will require special artwork.

8.1.5 Characteristics of printed lines are given in Section 11.

8.2 APPLICATION

8.2.1 Printed lines may be used to distribute standard d.c. voltages on boards to points not served by the pattern of the voltage plane, (See Figure 3).

8.2.2 Printed lines may be used to distribute special d.c. voltages.

9. VOLTAGE SENSING AND MEASUREMENT

9.1 VOLTAGE SENSING

9.1.1 Normally, the d.c. voltage will be sensed at the power supply and adjustment and regulation will be to such measured level.

9.1.2 When the feed lines from the supply to the circuits supplied are too long for acceptable regulation, voltage sensing will be by remote means and will occur at some point on the horizontal laminar bus as specified in 2.1.4.

9.1.3 Voltages will be sensed remotely over lines installed exclusively for this function.

9.2 MEASUREMENT OF D.C. VOLTAGE

9.2.1 Measurement will be made with a 1000 ohms per volt meter having a minimum accuracy of .5% at full scale.

9.2.2 Measurement of d.c. supply voltages shall be made during machine or system operation. Measurements are to be made at point or points designated for each application and such point or points shall be so marked.

9.3 MEASUREMENT OF A.C. VOLTAGE

9.3.1 The voltage to ground noise at the card socket shall be measured using an oscilloscope having response of d.c. to 50 megacycles and minimum sensitivity of 100 millivolts per major division (cm) of calibration. The minimum input impedance of the probe shall be 500 ohms (Tektronix 010-110 or equivalent). The ground lead on the probe shall not exceed 2 inches.

9.3.2 The voltage to ground noise at the module pins shall be measured using a sampling oscilloscope similar to Hewlett-Packard Model 187B. Measurements shall be made at points specified in Sections 2.2.3 and 2.2.4.

9.3.3 Ground to ground noise measurements shall be made across any two ground points on a card using an oscilloscope having a differential amplifier similar to 9.3.2.

9.3.4 Measurement of ground to ground points on a board or gate are to be specified.

10. DECOUPLING

10.1 GENERAL

10.1.1 This section outlines the voltage decoupling requirements for the various circuit families in SLT Packaging. Values given are for worst case conditions, and any lesser values for other than worst case conditions shall be determined by the user group for each individual application. In all cases, that amount of circuit decoupling shall be used which will assure that the power distribution system tolerances will not be exceeded.

10.1.2 Values of decoupling devices are given for 30 and 700 n.s. circuit families and one-high cards and two-high cards with and without internal service planes.

10.2 GROUND RULES COMMON TO ALL CIRCUIT FAMILIES

10.2.1 The decoupling requirements are stated for a six-pack card (and socket location). Each six-pack equivalent within a 12-pack must be considered separately.

10.2.2 All d.c. supply voltages shall be decoupled at the board by means of six (6) 0.68 mfd capacitors along each vertical edge of each board, thus providing 8.16 mfd for each voltage at each board.

10.2.3 Decoupling within cards, when required, shall be by use of a 0.68 mfd capacitor connnected to the circuit concerned and mounted in row 23.

10.3 ADDITIONAL GROUND RULES FOR 30 NANOSECOND FAMILY ONLY

10.3.1 The following rules apply to two-high cards with internal service planes, and one-high cards:

10.3.2 Voltage and ground lines on one-high cards shall have a nominal width of .031 inches. The ground leads shall fan out from the first via hole and not more than one circuit may be connected to each ground lead.

10.3.3 All cards with two or more line terminators (LTN) shall provide for decoupling of the +3 volts line in all cases. Cards requiring decoupling on the basis of the circuits within need no further decoupling if line terminators are provided.

10.3.4 Cards with four or more line sense amplifier (LSA) circuits shall provide for decoupling of the +6 volts line when all circuits driven by the LSA's are on the same card.

10.4 ADDITIONAL GROUND RULES FOR THE 700 NSEC FAMILY ONLY

10.4.1 These ground rules cover one and two-high cards without internal service planes. Exceptional cases may require use of an internal plane and are given special consideration in Section 10.6.2.2.

10.4.2 Voltage and ground lines on cards shall be nominally .031 wide. Ground lines shall fan out from the first via hole. Within limits described herein, up to four emitters may be connected to a single ground line originating from the first ground via hole.

10.4.3 Ground lines shall take the most direct route to the circuits served.

10.5 ASSIGNMENT OF DECOUPLING CAPACITORS

10.5.1 The decoupling requirements for cards are determined by type and number of modules used and the location of the modules. Two weight factors, "A" and "B", are used in determining the requirement.

10.5.2 A weight factor "A" is assigned to each module position on the card. This weight factor is derived from:

a. Characteristics of service plane (2-Hi cards).

b. Characteristics of fanned out ground lines (1-Hi cards).

10.5.3 The weight factor "A" for each module position in the various circuit families is given in Table 3.

TABLE 3

"A" FACTOR VALUES

30 nsec				700 nsec family		
7.5	7.5	7.5		60	60	60
7.0	7.0	7.0	2-hi	50	45	50
6.5	6.5	6.5		40	30	40
6.0	6.0	6.0	1-hi	25	15	25

10.5.4 A weight factor "B" is assigned to each circuit based on worst case loading and representative transition times for current changes. Weight factors "B" for all circuit families are shown below. For circuits not listed, "B" factors may be determined from the relation:

$$B = \frac{\text{Approximately (max ground current change in M.A.)}}{\text{(current transition time in n.s.)}}$$

TABLE 4

Circuit	30 n.s.	700 n.s.
LSA	2	
AI	2	1
AOI	3	1
API	5	1.5
DCI	10	4.5
II	3	1
AOPI		2
HPD	16	
XOR	6	
TLR	6	

10.6 DECOUPLING ANALYSIS

10.6.1 Decoupling Analysis for the 30 nanosecond family.

10.6.1.1 A decoupling factor, "C" is obtained by taking the summation of the products A B for each given module position n; however, it is possible to have two circuits in one module position, thus:

$$C = \Sigma NA_nB_n$$

where N = the number of occupied module positions.

The numerical value C determines how many voltages are decoupled.

10.6.1.2 The limits on C are specified such that the on-card noise tolerances specified in Section 2.2.3 are not exceeded.

	$C \leq 100$	No decoupling needed.
$100 \leq$	$C \leq 200$	+3 volts requires decoupling
$200 \leq$	$C \leq 300$	+3 and +6 volts require decoupling
$300 \leq$	C	30 nanoseconds family - see Section 10.6.1.3

10.6.1.3 Where $C \geq 300$ for the 30 nanosecond family, there is a high probability that the on-card noise tolerances in Section 2.2.3 may be exceeded. It is recommended that the card be re-laid out or restrictions be placed on the number of circuits that can be switched simultaneously.

10.6.2 DECOUPLING ANALYSIS FOR 700 NANOSECOND FAMILY

10.6.2.1 (a) The electrical noise at the ground via hole is referred to as "G" and is determined as follows:

$$G = 6 \Sigma NB$$

Where N = number of circuits on card, the figure derived represents the electrical noise environment with no decoupling.

(b) The electrical noise voltage (L) induced on each ground line fanning out from the ground via hole is:

$$L = \frac{(J-1)}{(J)} \Sigma JA_iB_i \qquad (1 \leq J \leq 4)$$

Where J = number of circuits connected to the ground line concerned.

i = one of the circuits connected to the ground line considered.

The values of G are specified such that the limits of on-card noise described in Section 2.2.3 are not exceeded.

(c) A card layout is acceptable with no decoupling only when:

$$G \leq 200$$

Cards requiring no decoupling shall be laid out so that for each ground line on the card:

$$L \leq (200\text{-}G)$$

(The factor (200-G) is the maximum allowable noise for a ground line such that the ground noise specification will not be exceeded).

(d) A card layout is acceptable when only the +12 volt collector supply is decoupled if:

$$G \leq 400$$

Cards with only the +12 volts collector supply decoupled shall be laid out so that for each ground line on the card:

$$L \leq (200 - 1/2G)$$

(The factor (1/2G) is a result of decoupling.)

(e) Cards are not recommended when:

$$G > 400$$

Such cards may be used under some conditions where only a limited number of circuits will switch simultaneously. Decoupling of +12M volts will help to minimize noise in this application.

10.6.2.2 Decoupling criteria only for cards with internal service plane if:

	G	$\leq$200	No decoupling
200 $\leq$	G	$\leq$400	+12 volts decoupled
400 $\leq$	G	$\leq$500	+12 and +12 M volts decoupled

(Decoupling devices mounted on row 23 of the card)

11. CHARACTERISTICS OF THE CONDUCTING MEDIA

	Specification Number	L/Inch	C/Inch	R_{dc}/Inch	I at 30°C	C_{w-w}/Inch	C_{w-g}/Inch	Short Circuit Current
Vertical Laminar Bus	890916	.606 nh	117.8 pf	.06 mohms	30 amps			
Horizontal Laminar Bus	890916	.736 nh	117.8 pf	.05 mohms	40 amps 50 amps			
Voltage Crossover Bus to Board	890921	24.9 to 101 nh		Pt. to Pt. 7 mohms	10 amps			20 amp/sec
Voltage Crossover Board to Board	890921	36 to 130 nh		Pt. to Pt. 12 mohms	10 amps			20 amp/sec
Minibus	890919	6.02 nh	33.9 pf	0.45 mohms	10 amps			20 amp/sec
Internal +3 Volt Bus ***	890909	1 nh	40.0 pf	Pt. to Pt. Res. 12 mohms	5 amps			60 amp/ 200 msec
Internal +6 Volt Bus ***	890909	1 nh	40.0 pf	Pt. to Pt. Res. 13 mohms	5 amps			60 amp/ 200 msec
Internal -3 Volt Bus ***	890909	3 nh	13.0 pf	Pt. to Pt. Res. 36 mohms	3 amps			40 amp/ 200 msec
Internal Ground Plane **	890909			Pt. to Pt. Res. 6.2 mohms	*See Note			
.010 Printed Line	890914	11.25 to 12.9 nh		29 mohms to 36 mohms	1.0 amp	.426 to .703 pf	1.96 to 2.23 pf	3.5 amps
.030 Printed Line		6.97 to 7.63 nh		7.5 mohms to 7.8 mohms	3.0 amps	.737 to 1.04 pf	3.3 to 3.61 pf	6.0 amps
Stranded Wire No. 18 AWG					8.0 amps			
Stranded Wire No. 20 AWG					6.0 amps			
Flat Cable	890917	10 to 11.7 nh		18.75 mohms	1.0 amp	.05 to .1 pf	1 to 1.4 pf	
Engineering Change Wire	890922							

Average Propagation Delay

Element	Delay
Board Printed Wiring	1.96 to 2.28 nsec/ft.
Card Printed Wiring (W/Internal Gnd.)	1.96 to 2.28 nsec/ft
Card Printed Wiring	0.106 nsec/inch
Spring (Card Contact)	0.120 nsec/inch
Board Discrete Wiring	1.300 to 1.500 nsec/ft.
Flat Cable	1.400 to 1.600 nsec/ft.

Contact Resistance

1. Crossover Connector (Voltage) - 5 mohms/contact
2. Card Socket - 10 mohms/contact

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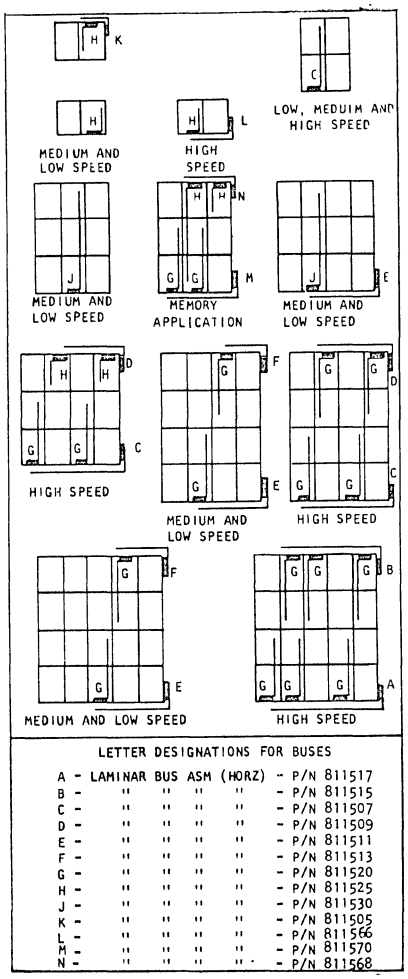
* Based on .010" spacing.
** Must carry return currents of ± 3 and 6 volts.
***Each leg of internal buss on voltage plane of board.

12. POWER SUPPLY TO GATE OR BOARD

12.1 Voltage Cabling. There are no specific ground rules established in regards to cabling from the Power Supplies to the Gate or Board for the SLT system. Basic design requirements for Power Supply cabling should be strictly adhered to with precautions in regard to shielding taken as required by equipment being designed.

13. DISPLAYS

13.1 Laminar Bus Arrangement



LETTER DESIGNATIONS FOR BUSES

A -	LAMINAR BUS ASM (HORZ)	- P/N 811517
B -	" " " "	- P/N 811515
C -	" " " "	- P/N 811507
D -	" " " "	- P/N 811509
E -	" " " "	- P/N 811511
F -	" " " "	- P/N 811513
G -	" " " "	- P/N 811520
H -	" " " "	- P/N 811525
J -	" " " "	- P/N 811530
K -	" " " "	- P/N 811505
L -	" " " "	- P/N 811566
M -	" " " "	- P/N 811570
N -	" " " "	- P/N 811568

FIGURE 2

13.2 Special Voltage Distribution

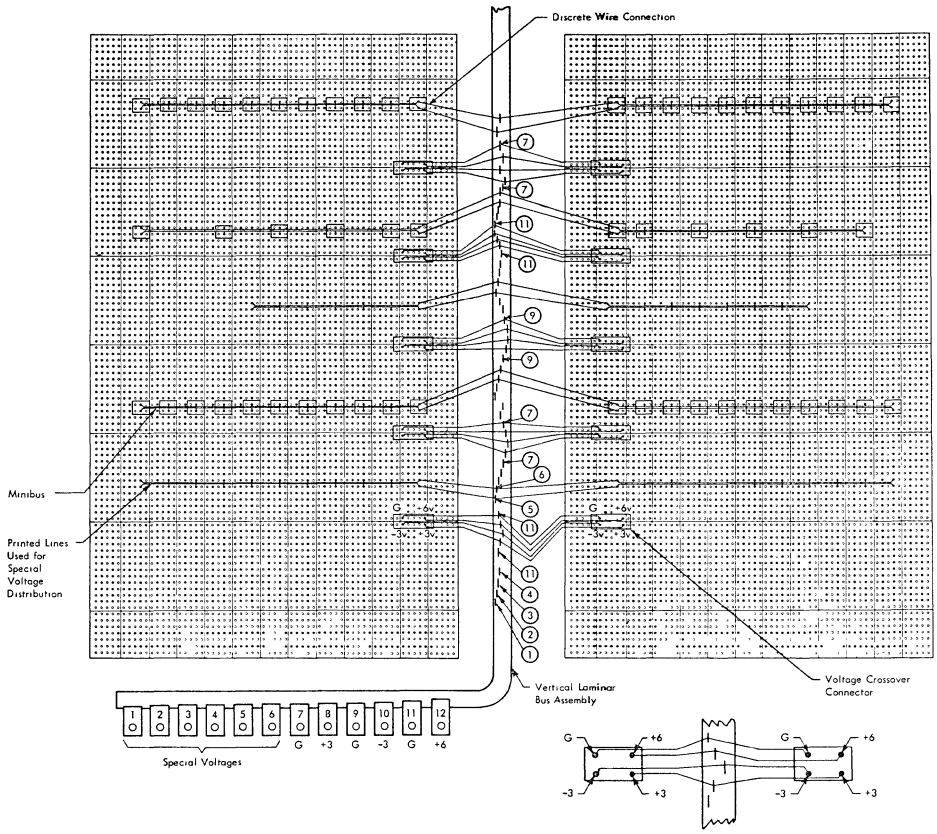


FIGURE 3

13.3 Board Assembly

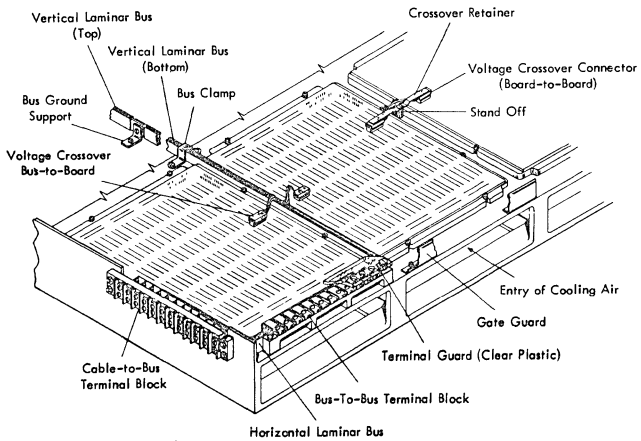


FIGURE 4

13.4 Mini-Bus

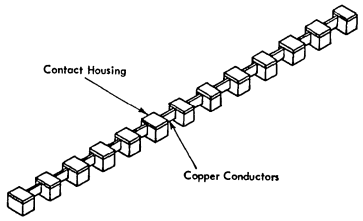
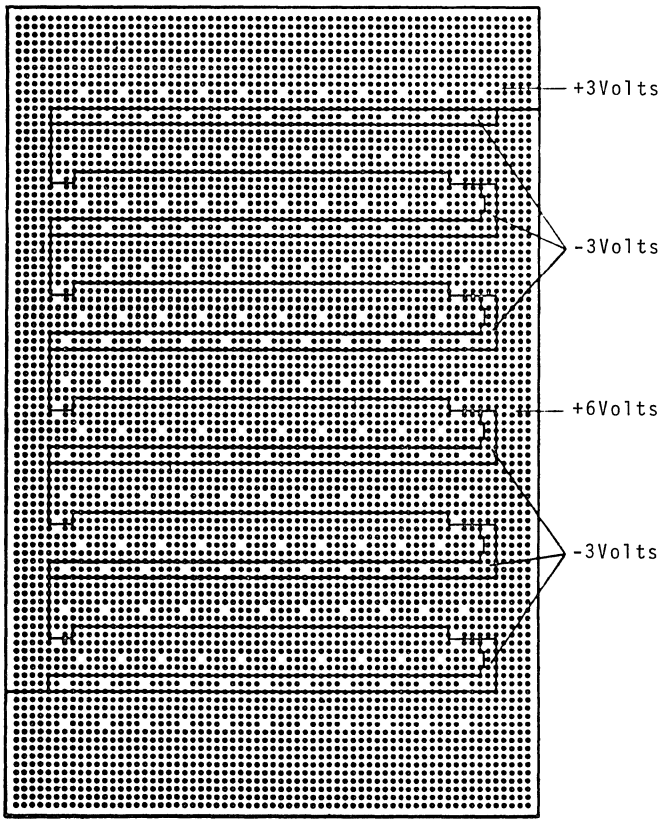


FIGURE 5

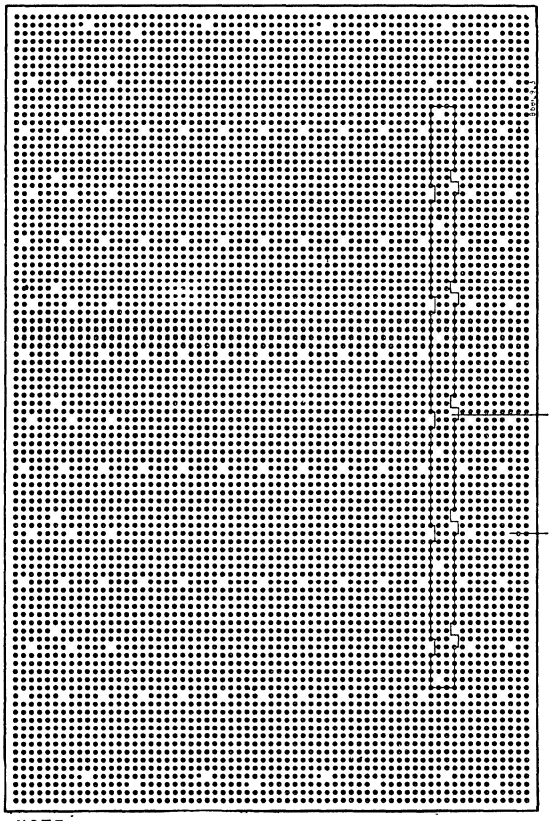
13.5 Voltage Plane - Card Side



NOTE: Conductive Surface Shown in White

FIGURE 6

13.6 Ground Plane - Pin Side



NOTE: Conductive Surface Shown in White

FIGURE 7

13.7 Voltage Crossover, Board to Board

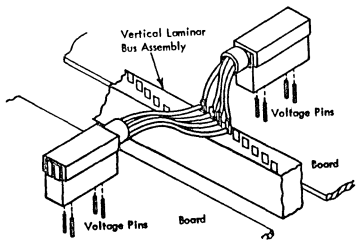


FIGURE 8

13.8 Voltage Crossover, Board to Board

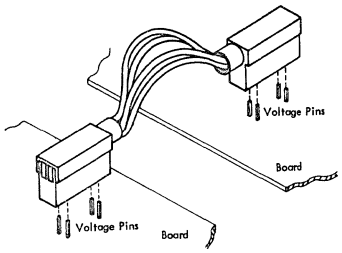


FIGURE 9

13.9 Eighteen Boards Fed by One Vertical Laminar Bus

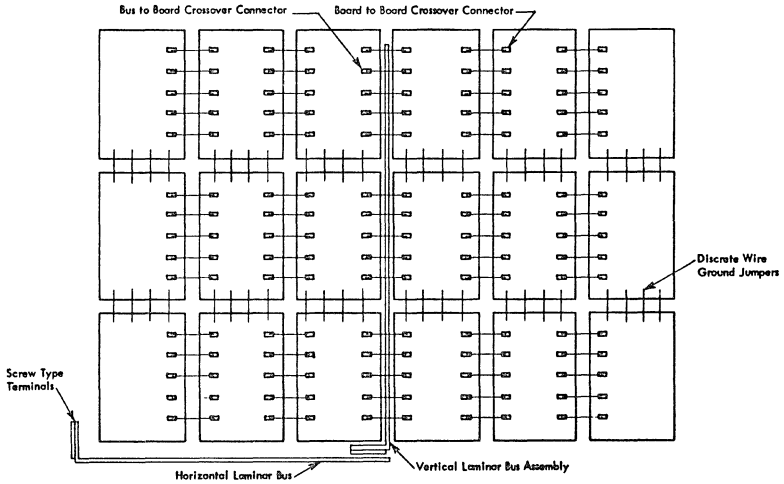


FIGURE 10

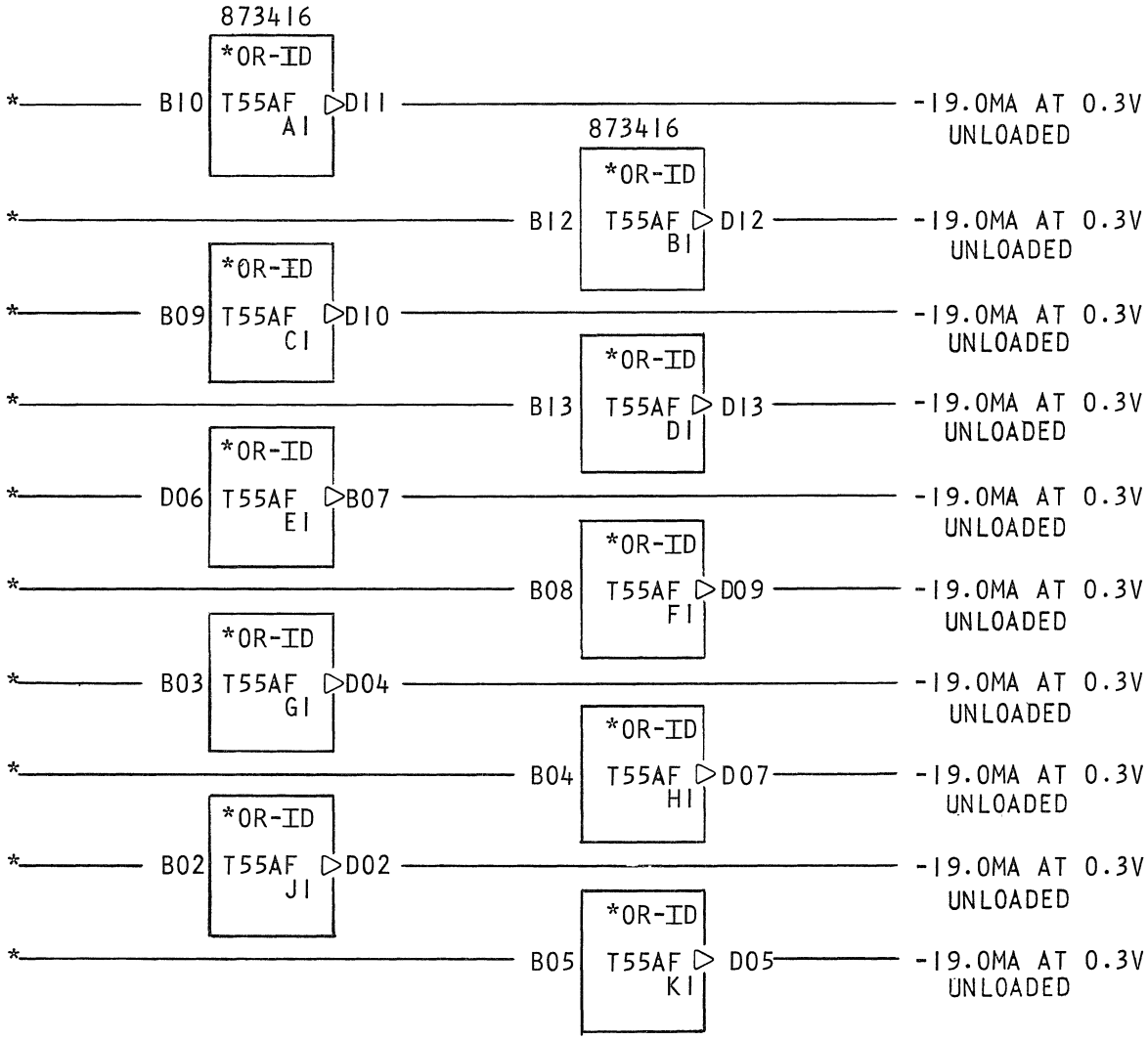
POWER REQUIRED	
PIN	VOLTS
B11	+6
B06	-3
D03	+3
D08	GND

10 INDICATOR DRIVERS WO/L

CATEGORY CODE

T55

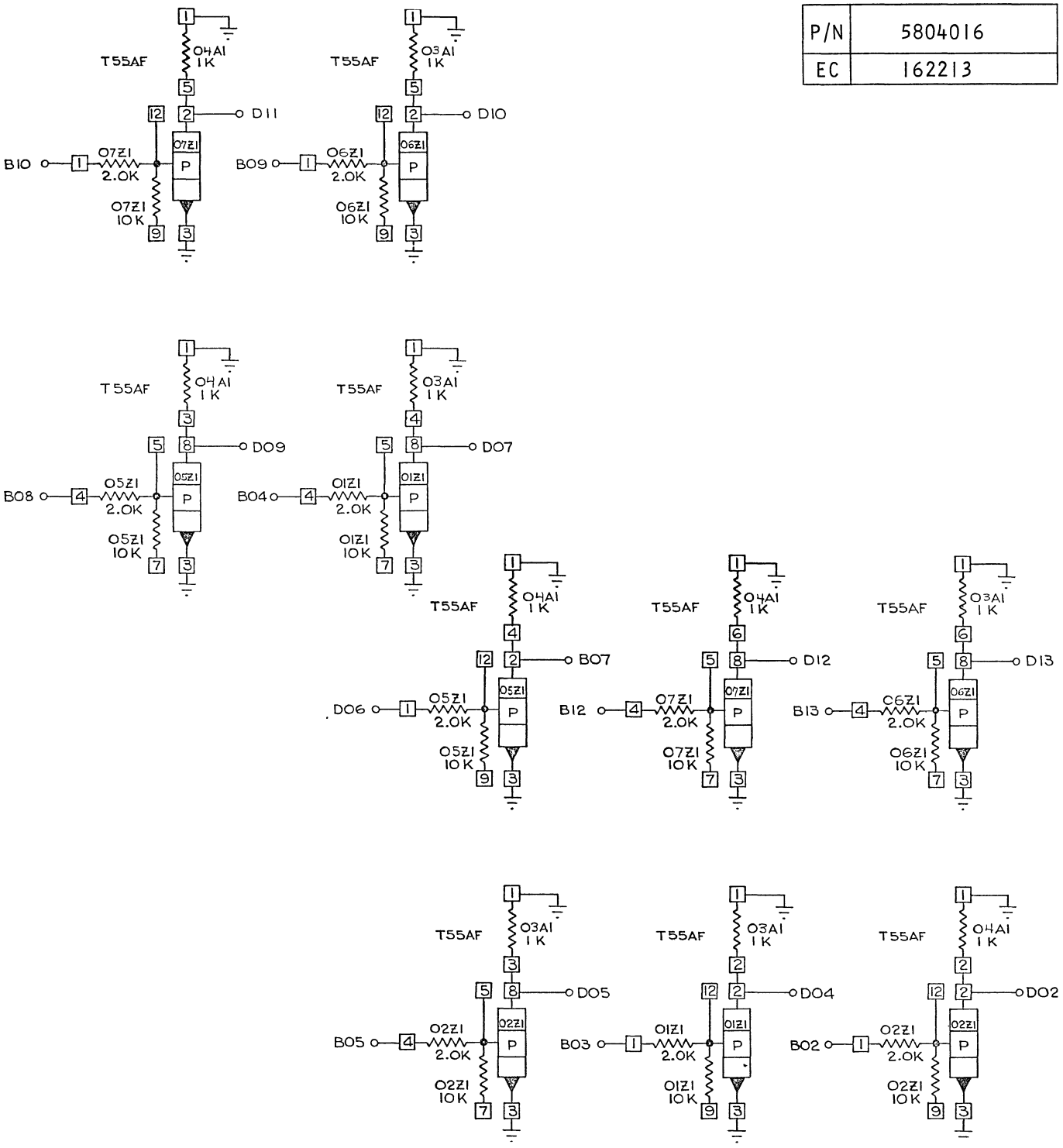
P/N	5804016	
EC	162213	
STANDARD RESTRICTED		
CARD SIZE		1-12



* SEE SPEC 873416 FOR SPECIAL DRIVE CONSIDERATION

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
IO INDICATOR DRIVERS WO/L

P/N	5804016
EC	162213



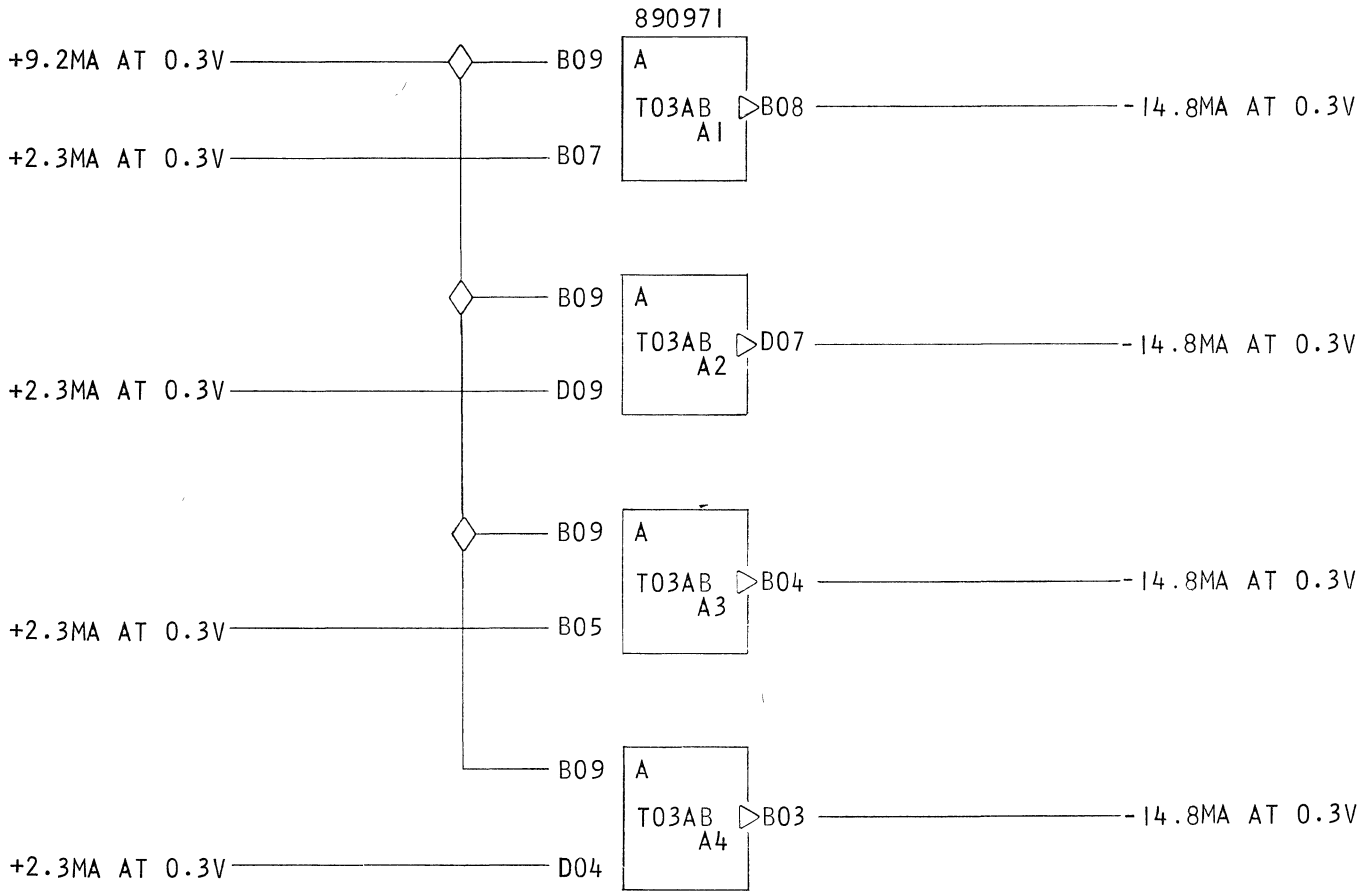
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

4-2W COMMON GATED AI & 5-2W COMMON GATED AI

CATEGORY CODE

T03

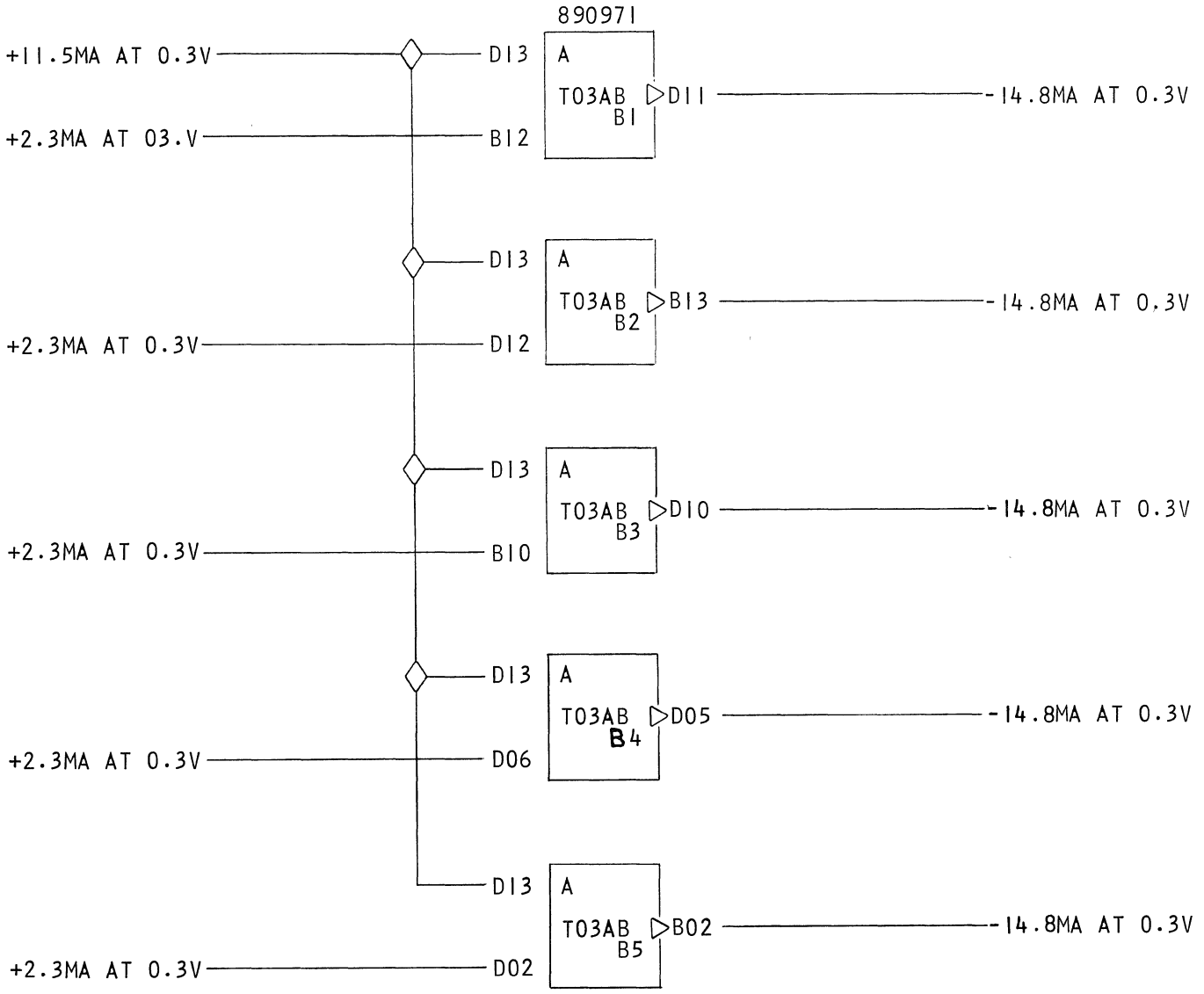
P/N	5804025	
EC	160160	
STANDARD RESTRICTED		
CARD SIZE		1-12



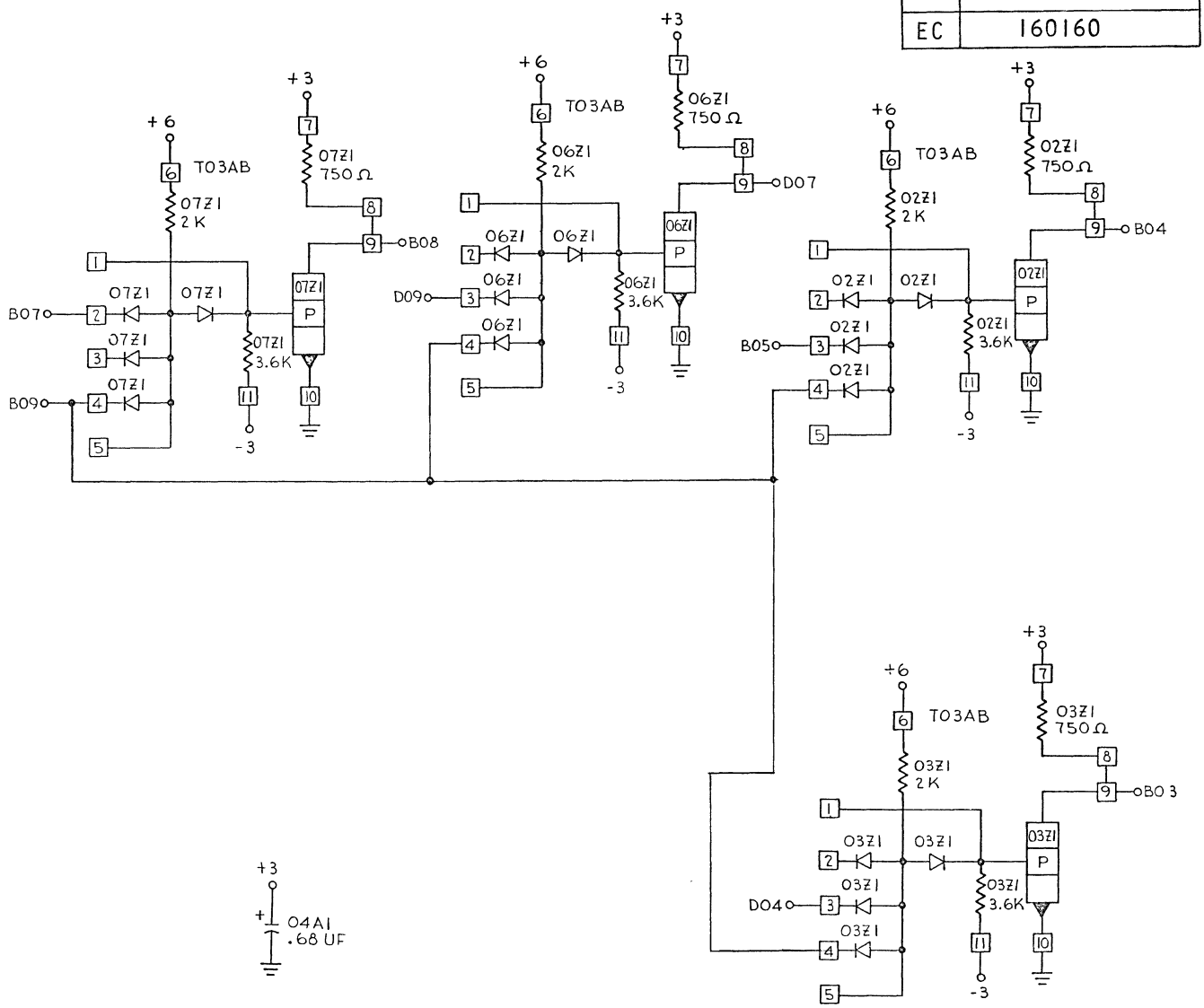
4-2W COMMON GATED AI & 5-2W COMMON GATED AI

T03

P/N	5804025
EC	160160



P/N	5804025
EC	160160



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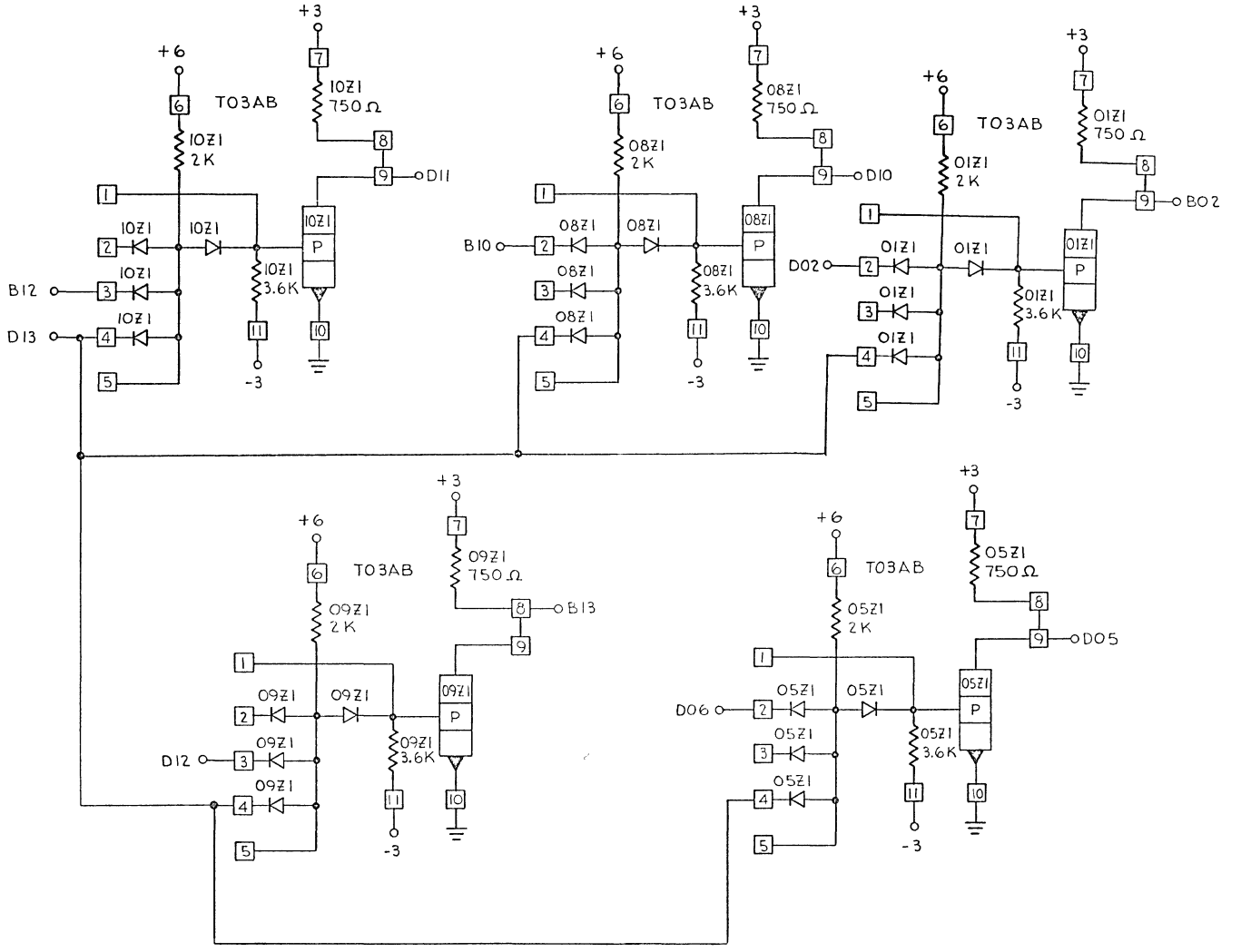
SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINGEERING
4-2W COMMON GATED AI & 5-2W COMMON GATED AI

P/N	5804025
EC	160160



SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
3-3W AI HPD WO/L

LMH Cat.	0-2860 Subject	390 Suffix

IBM **Location Manufacturing Specification**

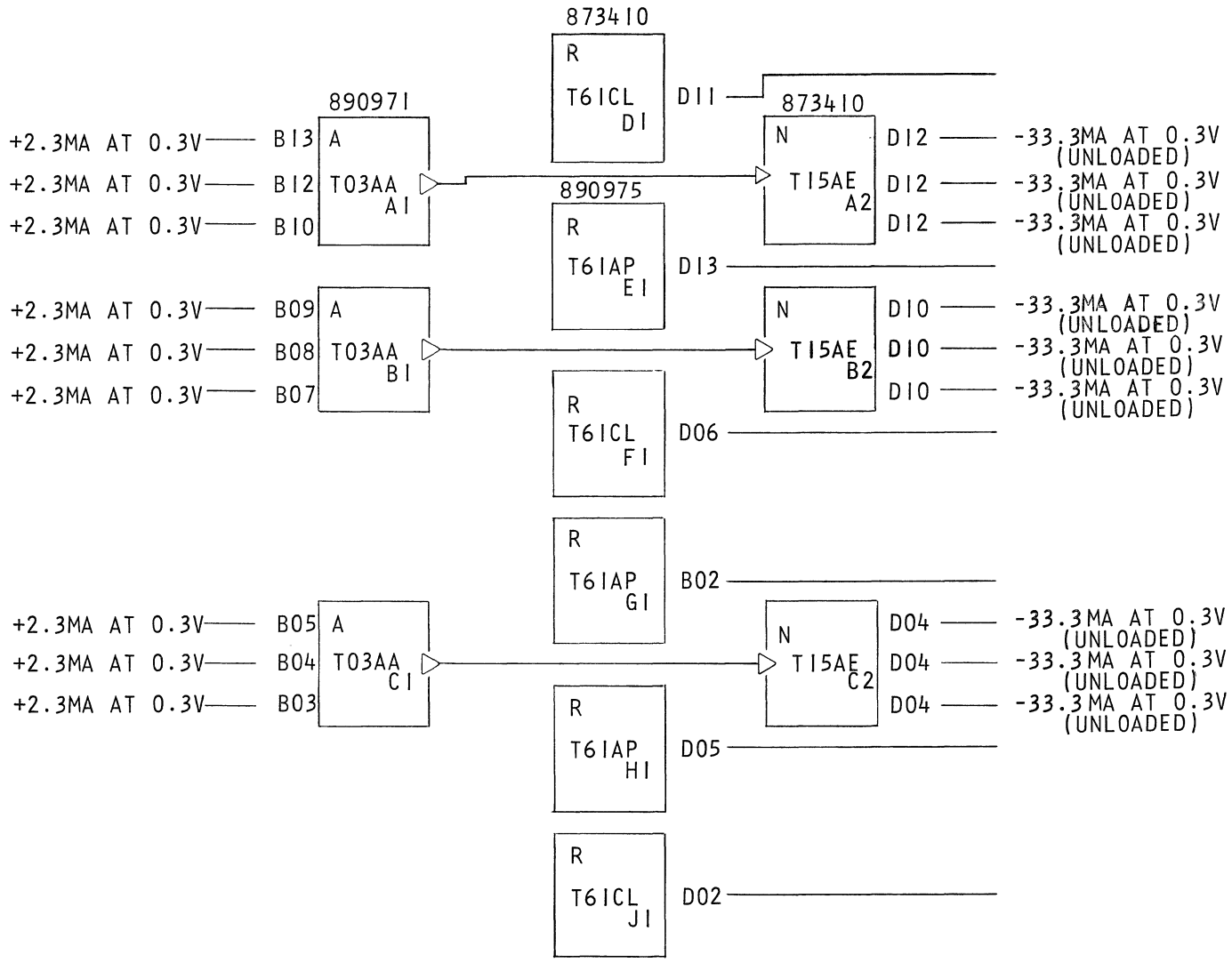
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

3-3W AI HPD WO/L

CATEGORY CODE

T03,T15

P/N	5804061
EC	160161
STANDARD RESTRICTED	
CARD SIZE	1-12



06-09 Primary Standards Manual	00-00 Other standards manuals in which this document may be filed.			
ENDICOTT Applicability		ENDICOTT Responsibility	1-67 Date	1 OF 2 Page

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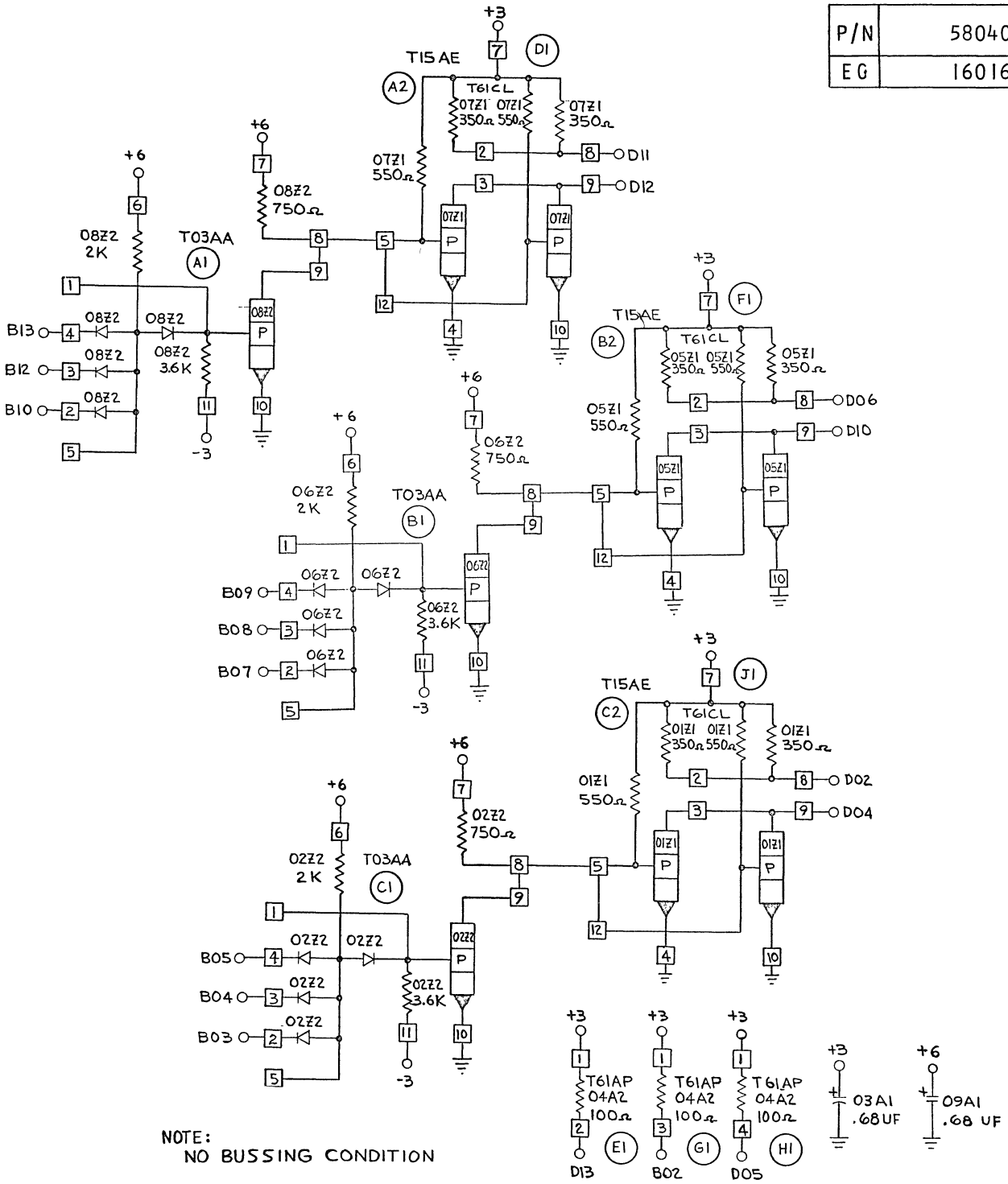
LMH Cat.	0-2860 Subject	390 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
3-3W A1 HPD WO/L

P/N	5804061
EG	160161



NOTE:
NO BUSSING CONDITION

Page	Date
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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
8-2 POINT (2 N/O) 48 VOLT REED RELAYS

LMH	0-2860	391
Cat.	Subject	Suffix

IBM

Location
Manufacturing Specification

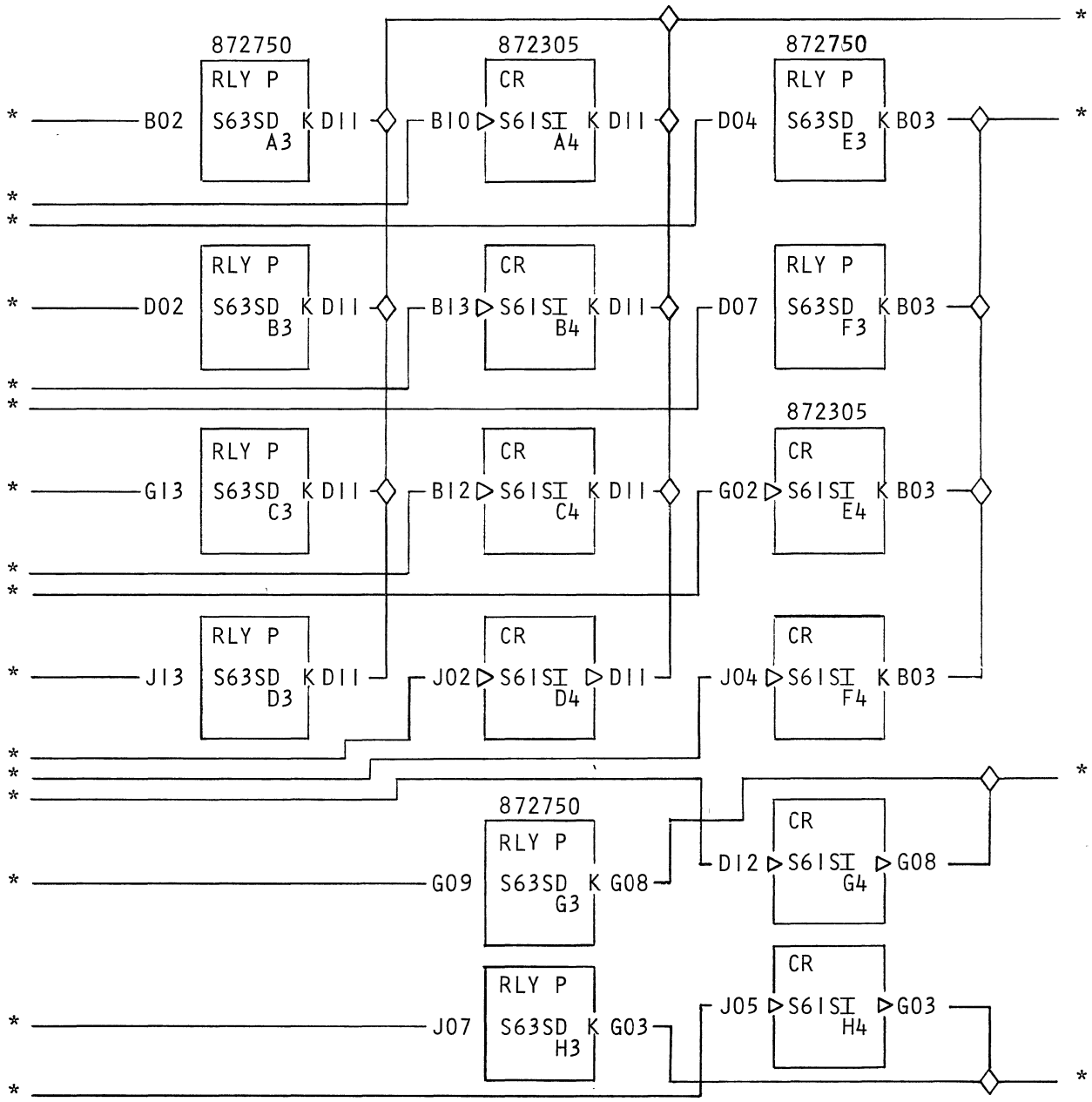
POWER REQUIRED
NONE*

8-2 POINT (2 N/O) 48 VOLT REED RELAYS

CATEGORY CODE

S63

P/N	5804611
EC	162880A
STANDARD ACTIVE	
CARD SIZE	2-24



06-09	00-00
Primary Standards Manual	Other standards manuals in which this document may be filed.

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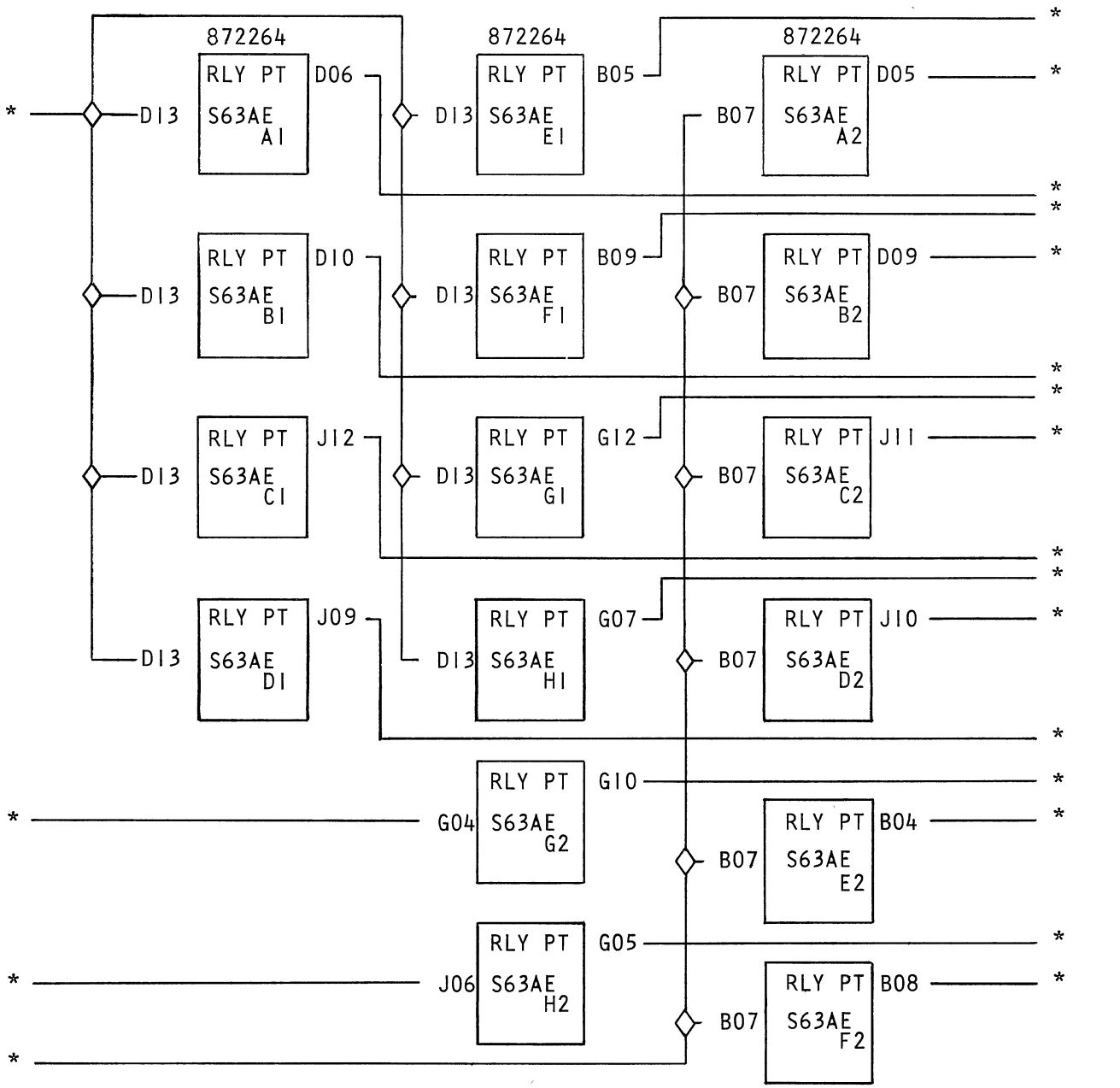
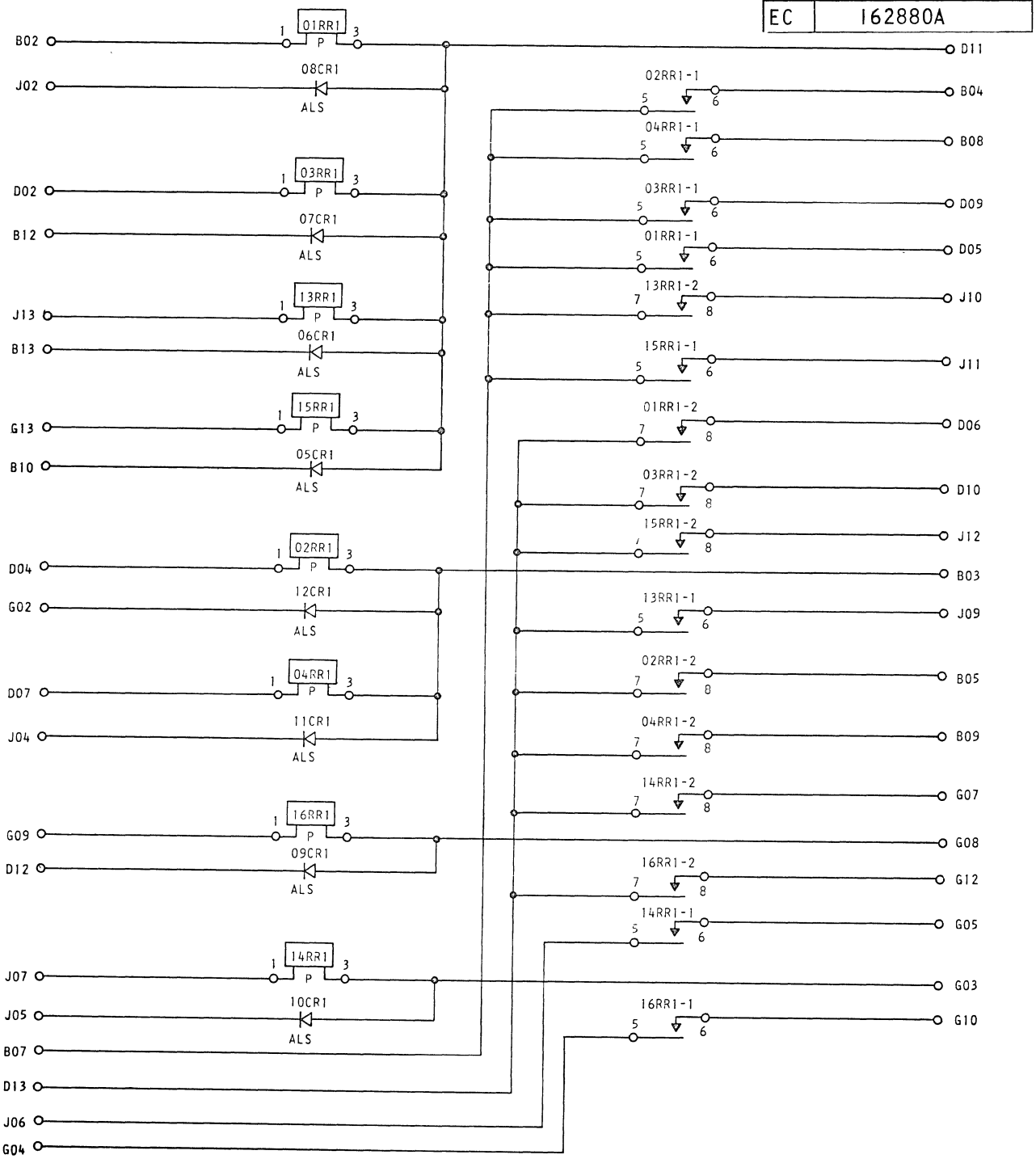
8-2 POINT (2 N/O) 48 VOLT REED RELAYS

P/N	5804611
EC	162880A



* SPECIAL REQUIREMENTS SEE CIRCUIT SPECIFICATION 872750

P/N	5804611
EC	162880A



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SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
VARIABLE TIME DELAY

LMH	0-2860	393
Cat.	Subject	Suffix

IBM Location Manufacturing Specification

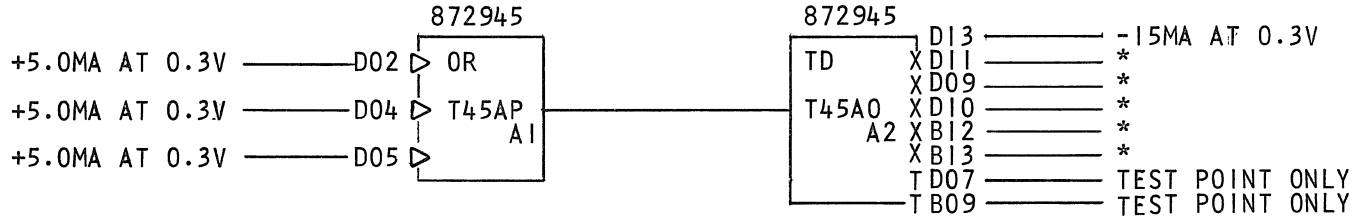
POWER REQUIRED	
PIN	VOLTS
B06	-3
B11	+6
D03	+3
D08	GND

VARIABLE TIME DELAY

CATEGORY CODE

T45

P/N	5804740
EC	164253
STANDARD RESTRICTED	
CARD SIZE	1-12



*ADJUSTABLE DELAY RANGES ARE OBTAINED BY CONNECTING DIFFERENT COMBINATIONS OF THESE OUTPUTS.

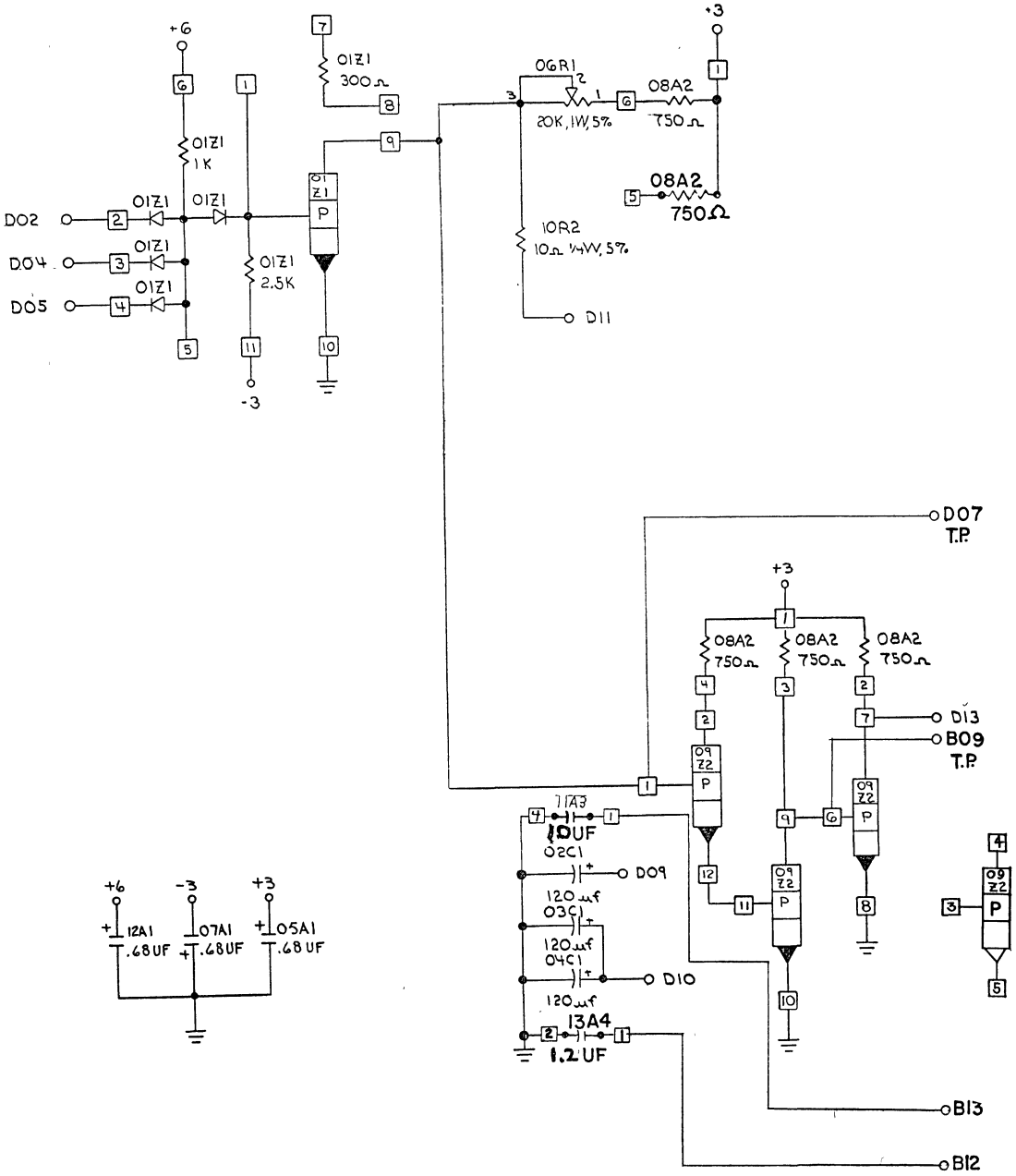
CONNECT PINS	DELAY RANGE
D11-D09-D10	2.5 TO 0.82 SEC
D11-D10	1.6 TO 0.52 SEC
D11-D09	0.82 TO 0.09 SEC
D11-B12-B13	96MSEC TO 9 MSEC
D11-B12	11MSEC TO 1 MSEC

LMH Cat.	0-2860 Subject	393 Suffix

SLT LOGIC DIAGRAM & SCHEMATIC - EQUIPMENT ENGINEERING
VARIABLE TIME DELAY

T45AØ, T45AP

P/N	5804740
EC	164253



Page 2	Date 12/69	

INTRODUCTION

1.1 SCOPE. Cooling demands relative to SLT packaging and the related hardware are discussed in this practice.

1.2 OBJECTIVE. Use of this practice is expected to eliminate air flow problems in the design of SLT packages.

1.3 DEVIATION APPROVAL. Implementation of the practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 SUPERSESSION. This practice supersedes LMP 0-2860-100 dated Jan. 67.

1.5 DEFINITION. Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

RECOMMENDED PRACTICE

2. GATE COOLING

2.1 General

2.1.1 The packaging of heat dissipating devices in any confined area imposes certain cooling requirements on the user. The mode and degree of cooling is dependent on several factors. The main considerations in the SLT program are component and device junction temperature, power dissipations, air velocities and pressure drops under various ambient temperature, humidity and altitude conditions.

2.1.2 Section 4 will give the designer a selection of fan units and header assemblies that meet the cooling requirements for SLT Board Gates.

3. GENERAL PACKAGING REQUIREMENTS

3.1 Air leakage should be minimized.

3.2 Air flow from card column to card column should be made as uniform as possible.

3.3 In the absence of cards (logic, cable, or horizontal crossover) in columns A or N of a board; dummy cards or other provisions must be made to avoid large air leakage or by-pass.

3.4 Recirculation of hot air should be avoided.

3.5 Isolate all heat from extraneous devices (motors, power supplies, etc.) from the cooling load if possible.

3.6 For high heat density special circuit components, adequate free-flow space (and heat sink if needed) should be provided in order to avoid hot spots.

3.7 Locate the most temperature-sensitive cards close to the bottom (air-inlet) of the gate frame as possible.

3.8 Locate the non-temperature sensitive high heat dissipating discrete components as high in the gate frame as possible.

3.9 Dummy cards shall be included in the design, as required, to compensate for any unbalance of card assignment.

3.10 Baffles shall be included in the design, as required, to compensate for the presence of unusual obstacles to air flow.

3.11 Warning indicators or devices shall signal when exhaust temperatures are in excess of their specified limit (131°F) and/or; signal the failure of the cooling system to maintain its specified minimum air flow.

Recommended Sensing Device

Thermal Switch Asm - P/N 5357070

3.12 The following is a list of dummy cards and card extenders used to promote even air flow:

2 Hi Dummy Cards	1 Hi to 2 Hi Card Extenders
2 Hi 6 Pac-P/N 811064	For 1-6 Card P/N 811363
1 Hi 6 Pac-P/N 811063	For 2-12 Card P/N 811364

4. COOLING ASSEMBLIES

4.1 General

4.1.1 The suggested cooling assemblies for Equipment Engineering's use are specifically designed for use with SLT board gates and the packaging concept allows the cooling unit and filter to be removed without the use of hand tools so as to minimize servicing time.

4.2 Description

4.2.1 The cooling hardware for a gate consists of two major assemblies; the Header Assembly and the Cooling Unit Assembly. A complete hardware B/M can be selected from the assemblies and the miscellaneous hardware parts as shown on the reference drawing P/N 5357101.

4.2.2 The Header Assembly is designed to distribute the air from the cooling unit to the gate, and to allow quick detachment of the cooling unit. A cable clamp, quick release mechanism, and sealing to the cooling unit, is provided in each Header.

4.2.3 The Cooling Unit assembly consists of the following major parts:

4.2.3.1 Housing. The housing contains one or more air moving devices, one or two filters and a cable harness if required. It clamps to the header with a tongue at one end and a quick release latch at the other end.

4.2.3.2 Air Moving Devices. Depending on the Cooling Unit Assembly selected from ref. drawing 5357101, you will get one of the following fan units:

4 inch fan assembly: 50-60 CFM

5 inch fan assembly: 100-120 CFM

Centrifugal Blower assembly: 150-200 CFM

4.3 Filter Assembly

4.3.1 The filter assembly contains a plastic foam type filter media and a supporting frame. It is held in place by a plunger type retainer.

4.4 Cable Assembly

4.4.1 A cable assembly is located in the housing when two or more moving devices are used in a cooling unit assembly.

5. PERFORMANCE

5.1 Complete performance, electrical, and maintenance specs on cooling assemblies can be obtained from Engineering Spec. 877224.

6. SUMMARY

6.1 For most applications Cooling Unit Assembly - P/N 5357052 and Header Assembly - P/N 5357055, are recommended for use by Equipment Engineering. This Cooling Assembly delivers from 100 to 120 CFM of air which is more than adequate under general packaging conditions. Any application that deviates from the basic package or exceeds its specified limits should be considered on an individual basis.

IBM Location Manufacturing Practice

INTRODUCTION

1.1 SCOPE. This practice discusses the limitations of the IBM frame for Equipment Engineering usage.

1.2 OBJECTIVE. This practice attempts to enlighten the Equipment Engineer in the selection of machine frames.

1.3 DEVIATION APPROVAL: Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

1.6 SUPERSESSION. This document supersedes LMP 0-2860-105, dated Jan. 67.

RECOMMENDED PRACTICES

2. SELECTION OF MACHINE FRAMES

2.1 General rules to follow when selecting a machine frame:

a. When the majority of assemblies being used are standard IBM parts, and they are all assembled to the same IBM product frame, then it is recommended that this IBM product frame be used.

b. When the assemblies being used are oriented towards the rack-mount frame and you are using a 2-wide gate frame, then it is recommended that a 30 inch rack-mount frame be used similar to that shown in Figure 1.

c. When more rigidity is required than that offered by IBM product frames and rack-mounting frames, then it is recommended that a square tubing framework be employed.

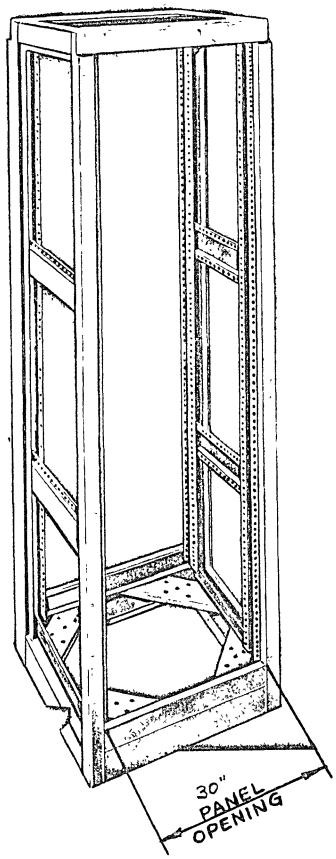


FIGURE 1

(NO SCALE)

INTRODUCTION

1.1 SCOPE. This practice presents components used in displaying control panel messages.

1.2 OBJECTIVE. The intent of this practice is to establish common display and control panel concepts.

1.3 DEVIATION APPROVAL: Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

RECOMMENDED PRACTICES

2. BACK PANEL LIGHTING COMPONENTS

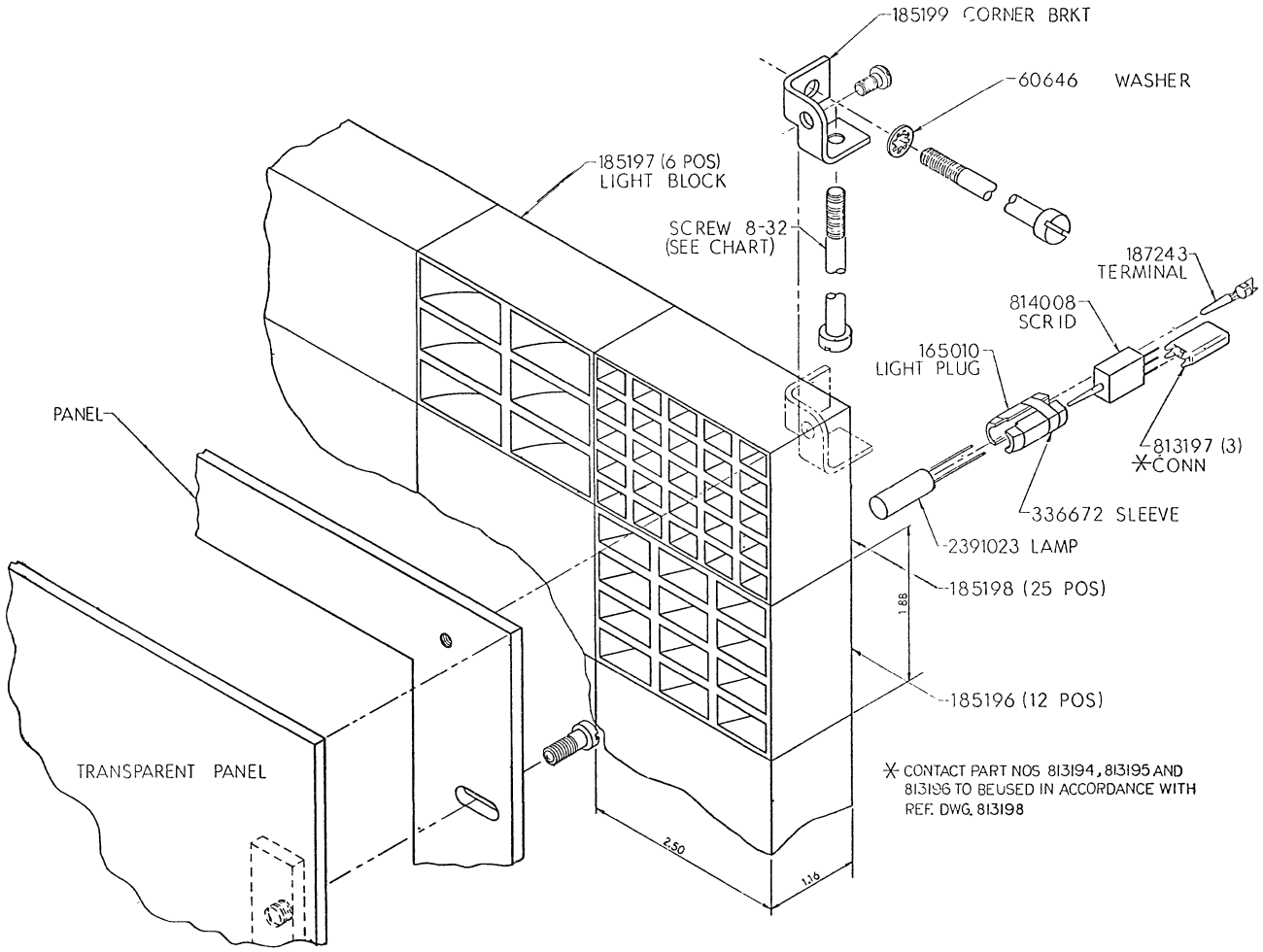


FIGURE 1

2.1 Descriptions and Applications (Figure 1)

2.1.1 TRANSPARENT PANEL. Messages are silk screened on a transparent plastic panel. Light blocks are held firmly against the panel. When a lamp is activated, the characters are illuminated and stand out against the dark and opaque panel.

No part numbers are given for the transparent panel, since the size, shape, and messages will vary with each application. The panel should be as thin as possible and consistent with mechanical strength. (Suggested material: 23-261).

2.1.2 INDICATOR ASSEMBLIES. Three different light blocks are available identical in outside dimensions, and keyed on the flats for firm nesting when multiple grouping of blocks is desired. The light blocks may be used individually and in groups of the same or mixed types. These blocks are identified as follows:

P/N	Description
185197	Six (6) lighted openings - each .500 by 1.125 inches.
185196	Twelve (12) lighted openings - each .344 by .708 inches.
185198	Twenty-five (25) lighted openings - each .268 by .393 inches.

2.1.3 LAMPS. Indicator lamp - P/N 2391023 is a 4.5 volt, 140 milliampere lamp, with an expected life of 25,000 hours. It has two wire leads coming from the rear which pass through the two contact holes in the light plug (P/N 165010) and are wedged into retaining slits on the side of the light plug.

2.1.4 LIGHT PLUG. The lampholder, P/N 165010 has a recess in one end for the lamp body, two holes lengthwise for the lamp leads to pass through, and a deep center slot lengthwise. Lamp leads pass through the longitudinal holes and are pulled into slots at the rear to retain the lamp in the light plug. Sleeve P/N 336672 is then assembled over the rear of the light plug to retain the lamp leads in the slots.

2.1.5 SCR INDICATOR DRIVER (Taper Contact). The Silicon Controlled Rectifier Indicator Driver - P/N 814008 is used as a switch to turn a lamp on and has an A.C. transformer as a lamp power source. The SCR and its associated circuitry is packaged into a module which plugs into one contact socket in the back of the light plug (P/N 165010).

2.1.6 LEAD TERMINAL. Taper pin terminal P/N 187243 must be assembled to the lead which plugs into the remaining contact socket of the light plug (P/N 165010). (See Figure 1).

2.1.7 CORNER BRACKETS. Light blocks are mounted individually or in groups by means of the 185199 corner bracket and connecting screws.

2.1.8 SCREWS. #8-32 screws connect the corner brackets, providing the tension to hold the light blocks together and the corner brackets in place. The length of the screws will vary, depending on the number of blocks being clamped. (See Table 1).

No. of Blocks Clamped on 1.875 Dim.	No. of Blocks Clamped on 2.500 Dim.	Length of Screw	Description	Part No.
1		1.500	FILL HEAD	52998
	1	2.250	FILL HEAD	438582
2		3.500	ROUND HEAD	304480
	2	4.750		*
3		5.250		*
	3	7.281	FILL HEAD	185210
4		7.281	FILL HEAD	185210
	4	9.781	FILL HEAD	761312
5		9.000		*
	5	12.250		*
6		11.000		*
	6	14.780	FILL HEAD	824475
7		12.750		*
	7	17.250		*
8		14.780	FILL HEAD	824475
	8	19.750		*
9		16.500		*
	9	22.500		*
10		18.500		*
	10	25.000		*

*Where a standard screw is not available, screw stock should be used with a jam nut on both ends. Add approximately .250 to length of screw to allow for the nuts. Please notify the Manufacturing Standard Function when a 9 million number is assigned to the screw stock, to update this table.

TABLE 1

3. FRONT PANEL LIGHTING COMPONENTS

3.1 Description. This method employs an indicator assembly and a plastic housing which are installed from the front of the panel and mates with two serpent connectors which are installed from the rear of the panel. (See Figure 2).

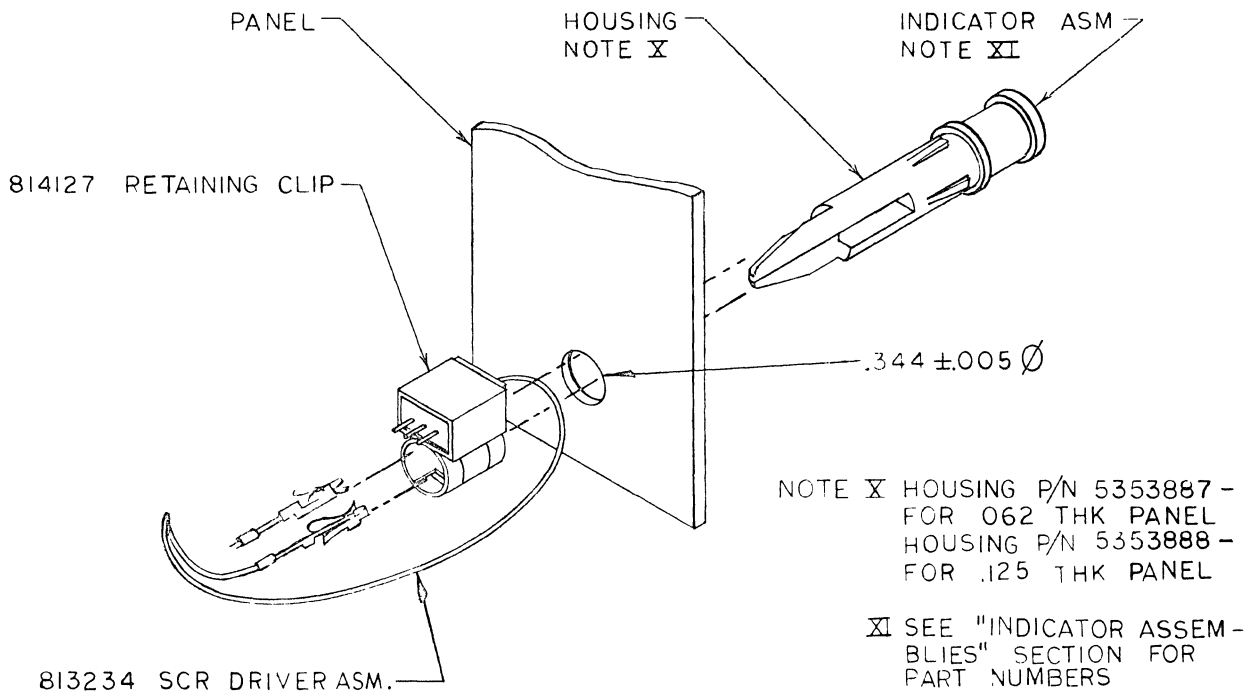


FIGURE 2

3.2 Application.

3.2.1 PANEL. For compatibility with the indicator housings available, the two panel thicknesses are .062 and .125 inches. A finished hole size of .344 ± .005 diameter should be provided for the plastic housing and indicator assembly.

3.2.2 INDICATOR ASSEMBLIES. The indicator assemblies recommended for front panel mounting are:

P/N 5372183 - Clear	uses lamp P/N 2391022
P/N 5372848 - Red	4.5 volt, 120 millampere
P/N 5372182 - Amber	(expected life - 25,000 hours)

3.2.3 HOUSINGS. There are two plastic housings for the indicator assemblies which are used for two different panel thicknesses. These are:

P/N 5353887 - .062 inch thick panel
P/N 5353888 - .125 inch thick panel

3.2.4 SCR INDICATOR DRIVER (Serpent Contact). The "Serpent Contact" indicator driver assembly, P/N 813234 is the same electrically as the "Taper Contact" indicator driver P/N 814008. The only physical difference is the mounting arrangement, as P/N 813234 mounts with a clip (P/N 814127) to the plastic housing of the indicator assembly and is connected electrically by the "Serpent Contact".

3.2.5 RETAINING CLIP. Retaining clip P/N 814127 is used to locate the indicator driver P/N 813234 on the indicator plastic housing.

4. ILLUMINATED INDICATORS & PUSHBUTTON SWITCHES

4.1 Description

a. Illuminated Indicators (Non-Operative). This method employs a plastic housing assembled with a pushbutton screen with information engraved on it and illuminated by a lamp behind the screen (See Figure 3).

b. Illuminated Pushbutton Switches (Operative) This method utilizes the same parts as the "non-operative" with the addition of a switch mounted on the back of the plastic housing (See Figure 4).

c. The plastic type illuminated indicators and pushbutton switches are designed for sub-panel mounting applications and are recommended for use because of low cost.

ILLUMINATED INDICATORS

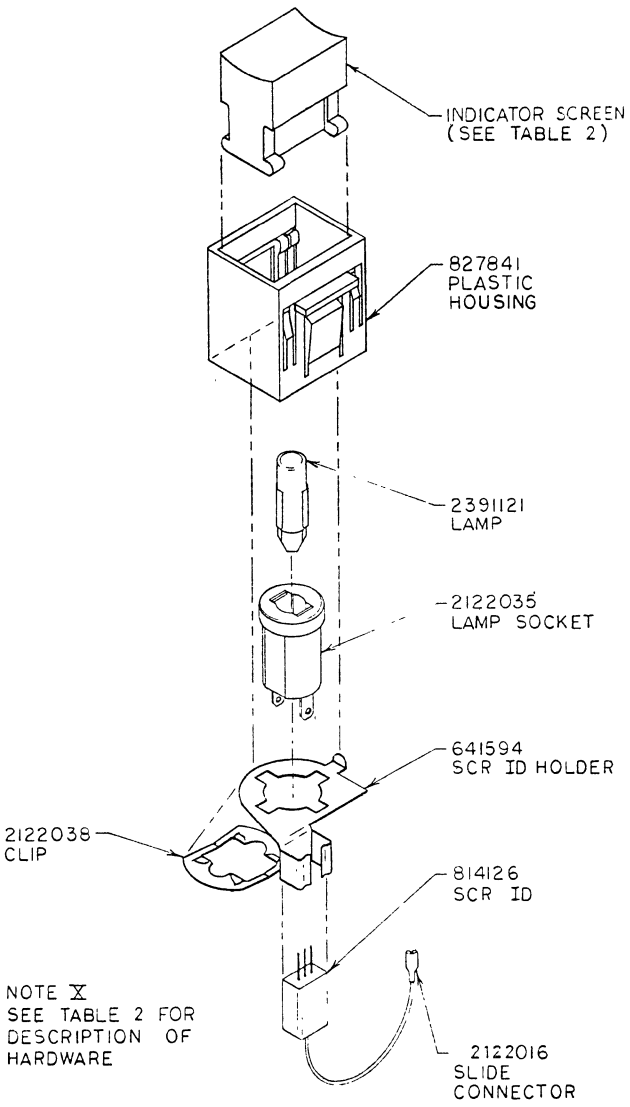


FIGURE 3

ILLUMINATED PUSHBUTTON SWITCHES

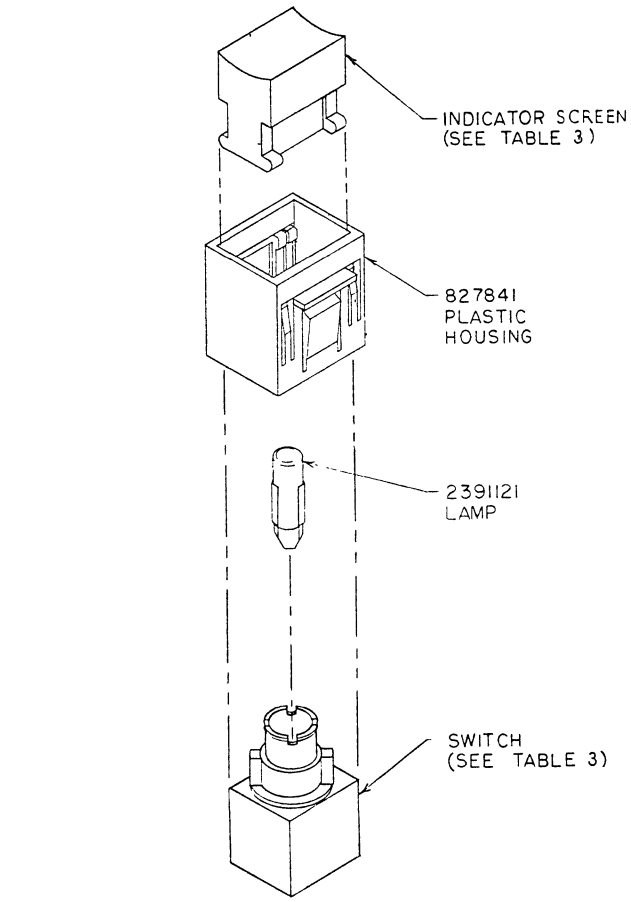


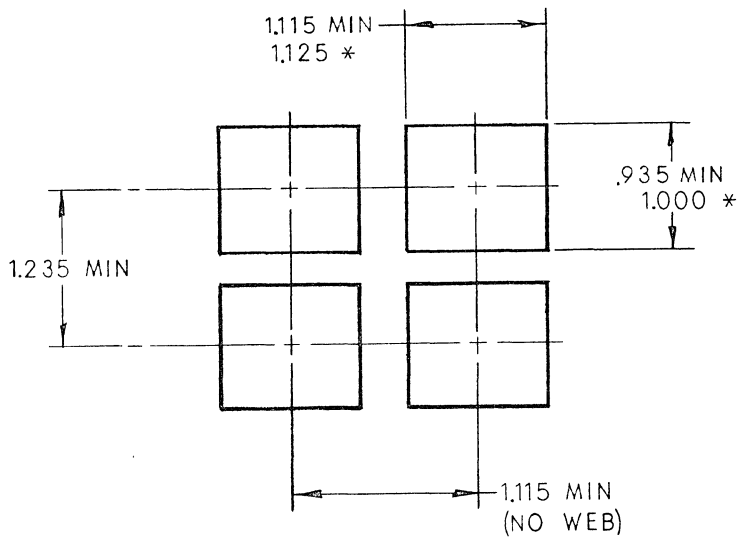
FIGURE 4

4.2 APPLICATION:

a. Illuminated Indicator Hardware (See Figure 3 and Table 2)

NAME	DESCRIPTION		Part Number
HOUSING	Basic plastic building block -- For mounting dimensions See Figure 5		827841
INDICATOR SCREEN	Illuminated by lamp to display information engraved on it - Has two lines engraved lengthwise on it to distinguish it from a pushbutton switch	White Red Green Yellow	827850 827851 827852 827853
LAMP	4.5 Volt, 200 milliamp - Telephone slide base. Expected life - 10,000 Hours minimum.		2391121
LAMP SOCKET	Assembled with lamp, positions in base of plastic housing - Has two push-on terminals for connector 2122016.		2122035
SCR INDICATOR DRIVER	Drives lamps - Is assembled to connector 2122016 for connection to lamp holder.		814126
SLIDE CONNECTOR	Assembles to lead of SCR Indicator Driver and connects to lamp holder.		2122016
SCR ID HOLDER	Positions SCR Indicator Driver on back of the plastic housing.		641594
CLIP	Retains SCR ID Holder on back of the plastic housing.		2122038

TABLE 2



* RECOMMENDED

FIGURE 5

b. Illuminated Pushbutton Switches

1. FEATURES

MOUNTING. Snap-in mounts to housing or panel. No adjustment required. Panel mounting holes must conform to outline dimensions on Figure 5. Panel thickness must be .062 inch.

Switch removal is accomplished by unlocking the tabs from the mounting surface with pliers or other suitable means. Reasonable care should be exercised in order not to damage plastic members in the process and allow reuse of the switch.

LAMP REPLACEMENT. When mounted to a plastic housing, the switch lamp is replaced by removing the pushbutton and grasping the plunger wall thickness with a long nose plier and pulling the plunger forward. The lamp ejects in the process and may be grasped with the plier or fingers after pushing the plunger back to its normal position. The plunger does not separate from the switch.

The replacement lamp is positioned in the plunger with the tip of the pliers, pencil, or finger. The lamp terminals should be oriented to the plunger terminals when inserting; however, improper orientation is prevented by the interference configuration of the switch lamp contact base.

2. Illuminated Pushbutton Switches (See Figure 4 and Table 3)

NAME	DESCRIPTION		PART NUMBER
HOUSING	Basic plastic building block - For mounting dimensions See Figure 5		827841
INDICATOR SCREEN	Illuminated by lamp to display information engraved on it - operates pushbutton switch mounted on back of plastic housing.	Red White Green Yellow	847920 847921 847922 847923
LAMP	4.5 Volts, 200 milliamp - Telephone Slide Base - Expected Life - 10,000 Hours Minimum.		2391121
PUSHBUTTON SWITCHES	See "Recommended Electrical Parts" - DCS Code 2-0102 for switch part numbers. (Engineering Standards Function in Glendale)		_____

TABLE 3

5. TRANSFORMER

5.1 A 7.25 volt transformer is suggested for driving all display panel lamps. A listing of suitable transformers is available below in Table 4.

POWER SUPPLY 7.25 V AC OUTPUT				
INPUT VOLTAGE (AC)	OUTPUT CURRENT	INPUT FREQ. (CPS)	FERRO NUMBER	ASSEMBLY NUMBER
112-235	25 amps	50	5708991	5708992
195-235	12.5 amps	50	5253828	
	25 amps	60	5708922	5708920
	25 amps	60	5708922	5708960
208-230	12.5 amps	60	5261395	
115	25 amps	60	5708993	
115-208	4 amps	60	634475	

TABLE 4

INTRODUCTION

1.1 SCOPE. This practice describes the silicon controlled Rectifier (SCR) indicator driver used for display and control panel lighting.

1.2 OBJECTIVE. The purpose of this practice is to provide the Equipment Engineer a circuit analysis of SCR indicator drivers.

1.3 DEVIATION APPROVAL: Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION: This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION: Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

RECOMMENDED PRACTICE

2. DISPLAY AND CONTROL PANEL ELECTRICAL SPECIFICATIONS

2.1 Silicon Controlled Rectifier (SCR) Indicator Driver

2.1.1 Functional Description. The SCR indicator driver was designed to provide power to incandescent lamps for plastic housing, display and control panel lighting, and can be used with any existing circuit family, regardless of power supplies available or signal type. See Section 8 for complete application information. Referring to Figure 1:

Entry point S(Signal) couples the logic net signal via an external resistor(R_S) to the gate of the SCR(1W8). An up-level (See Section 3.1) turns on the SCR and completes the connection between point G and the output pin causing the lamp to turn on. Dropping the logic net signal causes the SCR to extinguish (when negative excursion of voltage occurs at anode output), and causes an open circuit to exist between the output and point G, turning the lamp off. Point T, depending on the circuit family, is connected to either G or a negative voltage. It is brought positive to lamp test the circuit.

2.1.2 Circuit Diagram

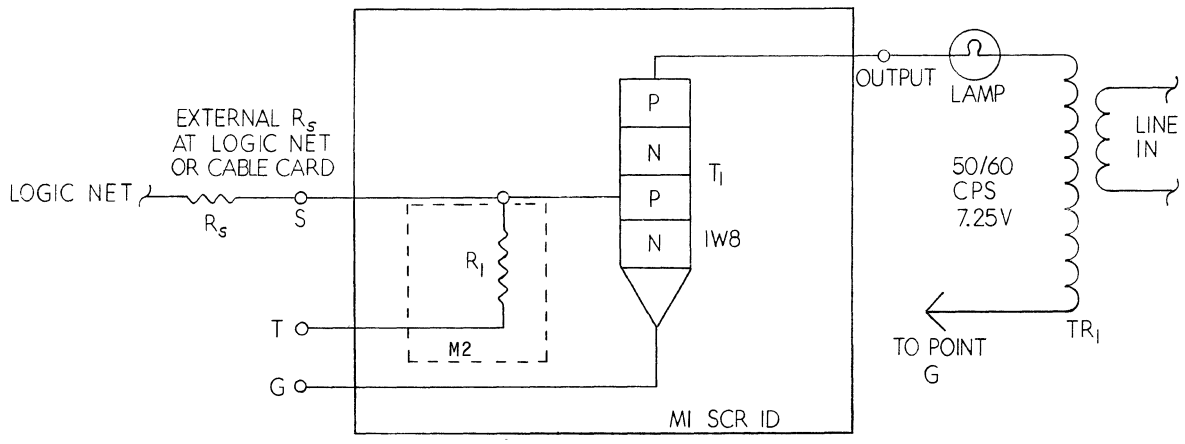
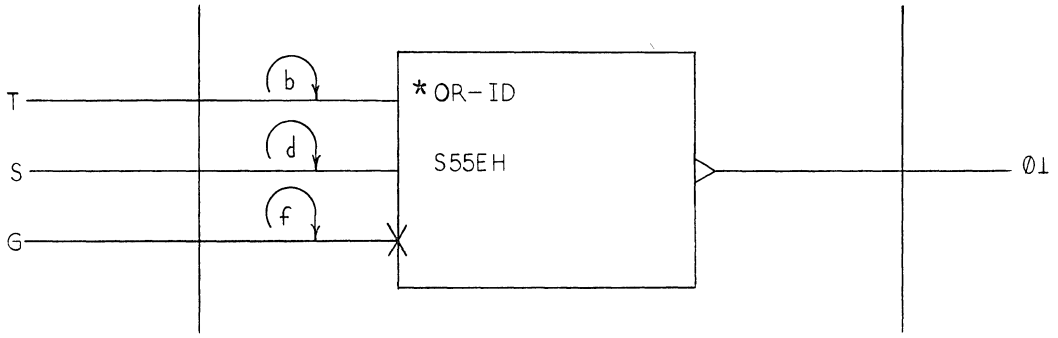


FIGURE 1

M2- optional R pac P/N 2390669 or discrete package P/N 216464, 6.8k
M1A- taper contact type 1 SCR module P/N 814008
M1B- serpent contact type 2 SCR module P/N 814126

R_S- See Section 3.1
T1- SCR type IW8, P/N 813228

2.1.3 Design Automation Block Representation



2.1.4 Special Driving Rules. Pin 'S' must be driven from a T55AL or S55EG source resistor. Pin G is normally grounded. The output must drive the indicator, (200 mA maximum).

	C P L	C T	MAXIMUM VOLTAGE (VOLTS)	MINIMUM VOLTAGE (VOLTS)	MAXIMUM LOAD CURRENT(MA)	MINIMUM LOAD CURRENT(MA)
UP LEVEL			20.0	2.2	-2.0 -0.22	-2.0 -0.22
DOWN LEVEL			-5.0	0.3	0.0 +0.4	0.0 +0.4

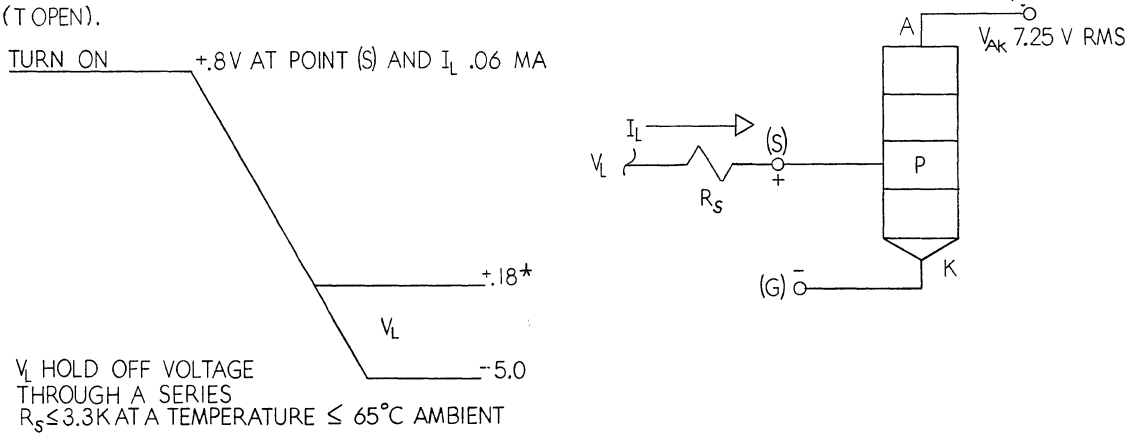
2.1.5 Referenced Circuit Flyers

S55EG - 6.2k Resistor (external)
S55EH - MT, SCRID

3. CIRCUIT SPECIFICATIONS: EC LEVEL 167662

3.1 Voltage levels (All voltages referenced to G)

TO EFFECT SWITCHING THE FOLLOWING VOLTAGES MUST BE OBSERVED WITH RESPECT TO POINT(G) (T OPEN).



* THIS MAY BE INCREASED TO +.3 VOLTS AND R_S MAY BE ≤ 7.2K FOR TEMPERATURE ≤ 55°C AMBIENT

FIGURE 2

3.1.1 The above switching requirement is guaranteed under the following application rules:

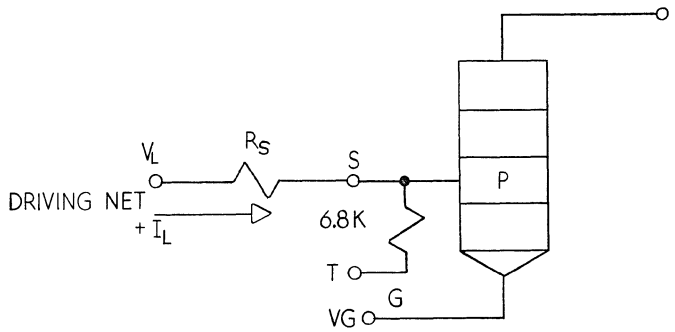


FIGURE 3

3.1.2 For T connected to G and V_L in down level equal to V_G (+.3 volts), then

V_L Up Level Required To Switch (Reference To V_G)	Maximum R_s Value	I_L Required From Driving Net (MA)
+1.8	5.0k	.234
+1.9	5.6k	.220
+2.0	6.2k	.220
+2.1	6.8k	.218
+2.25	7.5k	.217

Maximum Up-Level at V_L is limited only by power dissipated in R_S. For R_S = 6.2k, V_L Max. = 27 volts (for P = 125 MW)

3.1.3 For T connected to -3 volts and V_L in down level equal to V_G(+0.3 volts), then

V_L Up-Level Required To Switch (Referenced to V_G)	Maximum R_S Value	I_L Required From Driving Net (MA)
1	.270 K min.	1.16
1.33	.75 K	0.88
1.5	1k	0.84
1.93	1.6k	0.81
2.35	2.2k	0.79
3.83	4.3k	0.77
5.1	6.2k	0.75

Max. Up-Level at V_L is limited only by power dissipated in R_S.
For R_s = 6.2k V_L max = 27 Volts (P = 125 MW)
For R_s = 2.2k V_L max = 16 Volts (P = 125 MW)
For R_s = 1.6k V_L max = 14 Volts (P = 125 MW)

3.1.4 For T connected to -3 volts and V_L in down level equal to V_G (+1.06 Volts), then

V_L Up-Level Required To Switch(Referenced To V_G)	R_s Value	I_L Required From Driving Net (MA)
2.35	2.2k min	.79
3.83	4.3k	.77
5.1	6.2k	.75

Maximum Up-Level at V_L is limited only by power dissipated in R_s.

For R_s = 2.2k V_L max = 16 Volts (P = 125 MW)
For R_s = 5.1k V_L max = 25 Volts (P = 125 MW)

3.1.5 Minimum test entry voltage (Up-Level) is equal to $\frac{7.52}{R_S}$ (.8 - V_L Down Level) +1.44
Maximum test entry voltage should not exceed 20 volts.

3.2 Current Requirements:

3.2.1 Signal Entry: See Section 3.1 for Up-Level current requirement I_L. Down-Level current requirement is zero for T connected to G. For T connected to -3 volts, Down-Level current for S entry (current that flows into SCR circuit while V_L is at Down-Level) is equal to

$$\frac{V_L \text{ Down-Level } +2.88}{1.05\ R_s\ +7.15}$$

3.2.2 Test entry requirements (all voltages referenced to Point G)

Voltage At V_L	Value Of R_S	Minimum Required Test Entry Voltage (V)	Required Test Entry Current (MA)
0.0	.27k	23.4	3.4
0.0	1k	7.3	1.0
0.0	1.6k	5.0	.65
0.0	2.2k	4.0	.50
0.0	4.3k	2.6	.29
0.0	6.2k	2.2	.23

3.3 Equivalent Circuit Schematic Presented to Drive.

3.3.1 Signal Entry (S)

Logic net at Up-Level ($V_L > .7V$)

Logic Net at Down-Level ($V_L < .8V$)

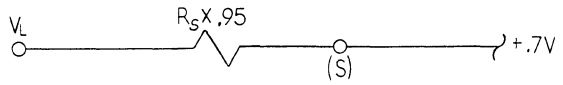


FIGURE 4

3.3.2 Test Entry (T)

Net at Up-Level ($V_T > .7V$)

Net at Down-Level ($V_T < .8V$)

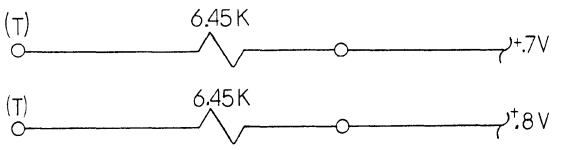


FIGURE 5

3.4 Pulse Width:

With R_S equal to 6.2k and T connected to G, a 20 US, 2 Volt pulse is necessary to turn on the SCR. Increasing the amplitude to 6 Volts decreases the required turn on pulse width to 1 USEC. To cause full lamp incandesence it is necessary to increase the pulse width to 100 ms.

3.5 Input Slope:

Not Applicable

4. OUTPUT SPECIFICATIONS

4.1 Anode Voltage: The SCR may be returned to 20 volts anode voltage and perform according to entry spec. listed in Section 3.1. The maximum voltage limit on the device is 40 volts (anode to cathode). The anode waveform under normal operation is:

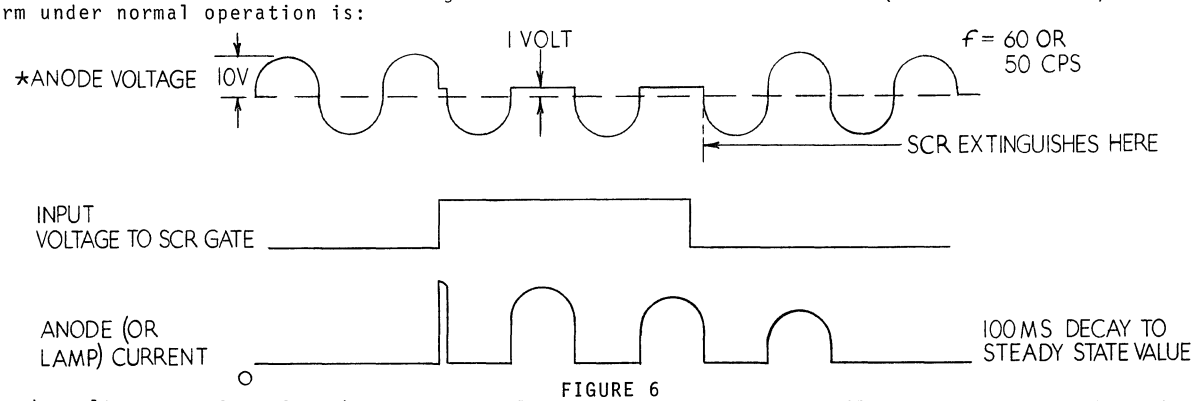


FIGURE 6

*The anode voltage waveform for the constant voltage transformer source will be more square than sinusoid for less than maximum load on transformer.

4.2 Anode Current: The indicator driver is specified to operate at 200 MA steady state anode current. Under normal operation (AC on anode) the following current waveform will be observed:

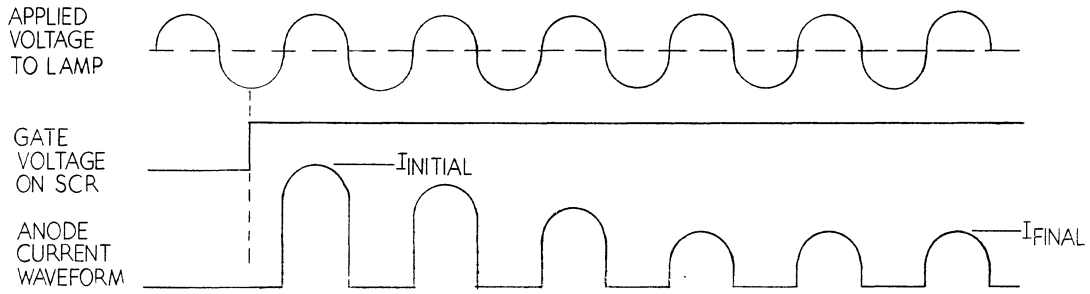


FIGURE 7

APPROXIMATELY 100 MS REQUIRED FOR FULL HEATING OF LAMP FILAMENT (f = 50 OR 60 CPS)

I Final = 170 MA for a 120 MA DC rated 4.5V bulb

I Final = 198 MA for a 140 MA DC rated 4.5V bulb

I Final = 280 MA for a 200 MA DC rated 4.5V bulb

I Initial for a cold bulb = approximately 8 times I final

The SCR is capable of supplying 3.0 amps peak for 10 consecutive cycles at a 60 CPS rate. The RMS value of current must then settle to 300 MA.

5. TRANSIENT BEHAVIOR

SEE SCR Device Specification #813228

6. POWER REQUIREMENTS

6.1 Power supply voltage tolerance at circuit.

6.1.1 A constant voltage transformer is specified for lamp power. This guarantees a specified lamp life at a required light output. See Section 8.1.

6.1.2 When point T is connected to -3 volts a 4% variation is permitted on this supply.

6.2 Power supply current requirements:

6.2.1 See Section 8.1 for current rating of transformer as a function of lamps driven.

6.2.2 The -3 volt supply must be capable of accepting .62 MA from each circuit when point T is connected to -3 volts.

6.3 Power dissipation:

6.3.1 SCR dissipation (Gate Up)

When Driving	SCR 1/2 Cycle Power	SCR Average Power	Lamp Average Power
120 MA Lamp	170 MW	85 MW	540 MW
140 MA Lamp	196 MW	98 MW	630 MW
200 MA Lamp	280 MW	140 MW	900 MW

6.3.2 Dissipation in R_T (6.8k)

Point T connected to Cathode (G) and Gate at -5 volts

Max Power = 4 MW

Point T connected to -3 volts and gate at +.8 volts

Max Power = 2.2 MW

Max Power in R_S (Refer to Fig. 3) is $\frac{(\overline{V}_L - .7)^2}{.95\ R_S}$

6.3.3 For maximum device performance (SCR), See Specification 813228.

6.4 Duty Cycle: With the specified loads there is no limitation on duty cycle.

6.5 The SCR ID module requires no forced air cooling in an ambient temperature not exceeding 65°C.

6.6 The anode to cathode voltage must not exceed 40 volts. The gate to cathode voltage must not exceed -5 volts.

6.7 No power supply sequencing is required.

7. MARGINAL CHECKING

Not Applicable

8. APPLICATIONS

8.1 Transformer Selection

8.1.1 The relationship between the number of lamps that may be powered by one transformer and the output current rating of the transformer is given by

$$N = \frac{7.25 \times I \text{ rated}}{PL \times F}$$

Where:
I rated is the 100% load current capability of the transformer.

PL is the power in watts required by each lamp position (driver plus lamp)

PL = .73 for 140 MA lamp; PL = .63 for the 120 MA lamps; PL = 1.05 for the 200 MA bulb.

F is the fractional number of lamps that may be on at any one time.

8.1.2 For lamp test, the maximum number of lights that may be wired into one transformer and all tested simultaneously is

$$N = \frac{7.25 \times I \text{ rated } X2}{PL}$$

MEDIUM AND LOW SPEED CIRCUIT APPLICATION

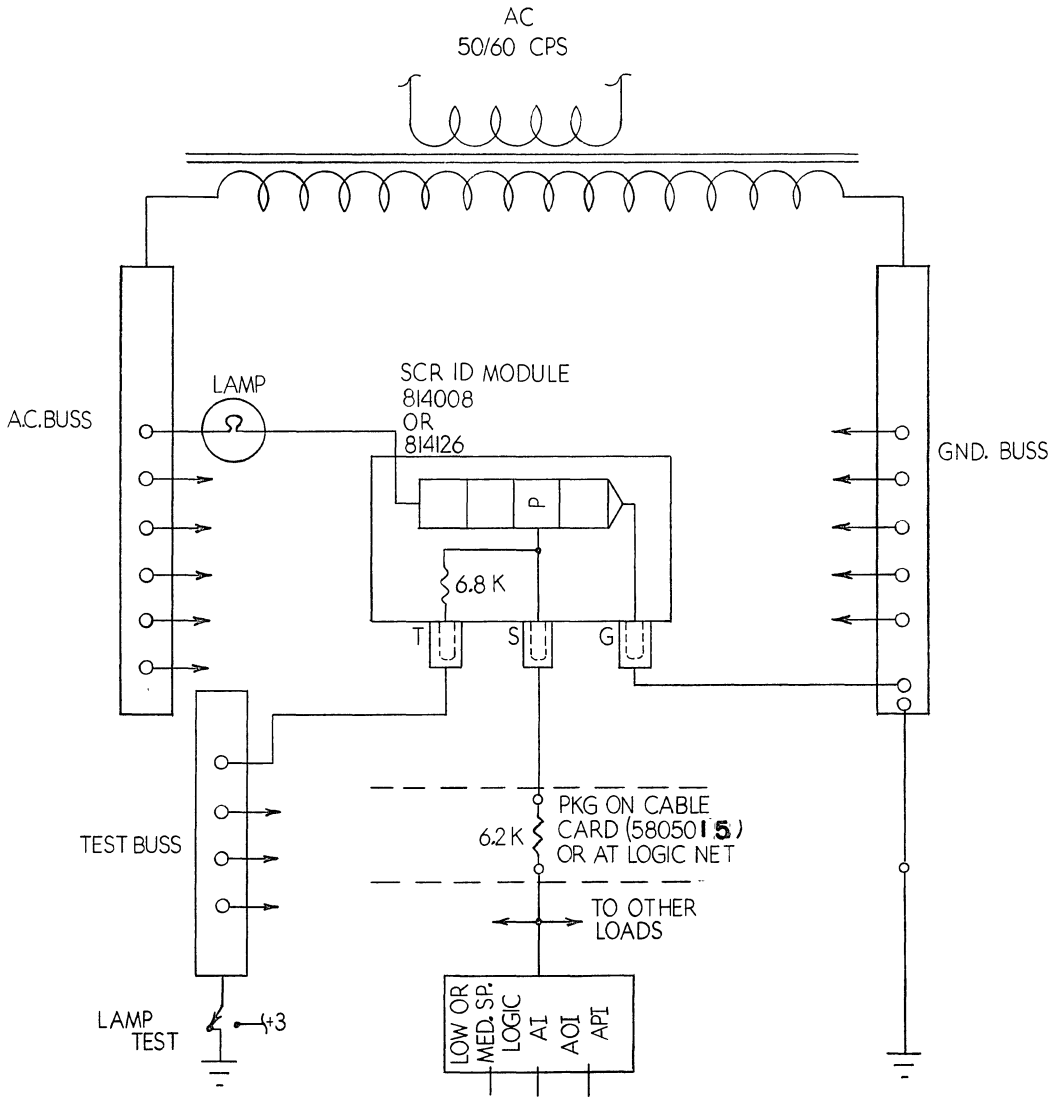


FIGURE 8

8.1.2 (Continued)

Under this condition, the transformer will not provide specified voltage and the lamps will be at less than full brilliance. If it is desired to test more lamps than the formula allows, it will be necessary to split the lamp test circuit into several parts and test each part independent of the other on a time share basis.

8.1.3 The lamp formula may also be used to determine the transformer rating.

$$I \text{ rated} = \frac{F \times N \times PL}{7.25}$$

8.1.4 Since all lamps required the same voltage (7.25 vac) mixed lamp combinations (behind panel, thru panel, and behind plastic) may exist on one transformer. The composite lamp loading equation then becomes $(F_1)(N_1)(PL_1) + F_2\ N_2\ PL_2 + F_3\ N_3\ PL_3 = 7.25\ I$ rated.

Where subscripts 1, 2, and 3 indicate the behind panel, thru panel and behind plastic lighting quantities as previously defined.

8.2 Circuit Application:

8.2.1 Low and medium speed SLT logic. (6.2k entry resistor) the overall schematic is shown in Figure 8. The SCR gate entry resistor is not mounted within the ID module but is available on a cable card. If desired, the resistor may be packaged functionally on the card that contains the logic net that will drive the indicator. If the lamp test feature is not desired, then the test and ground points must be jumpered together and grounded.

To permit the SCR to turn off, it is necessary to drop the voltage at the logic net to +.3 volts or more negative (not to exceed -5 volts). This enables the SCR to turn off (hence, extinguish the lamp) on the next negative excursion of voltage on the anode. Logic net loading at 0.3 volts is negligible. To turn the SCR on, it is necessary to increase the voltage at the logic net to +2.0 volts. The current required from the net at this voltage is .22MA and at +4 volts is .56 MA. The current required by the ID at input voltage VL is equal to $\frac{VL - .7}{.95\ R_S}$ MA

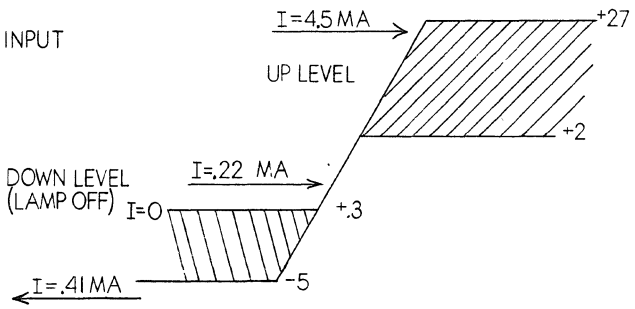
where R_S is the entry resistor.

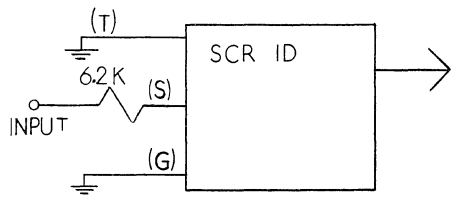
The voltage V_L necessary to turn on the ID is equal to $0.8 + R_S\left[\frac{0.8 - V_T + .063}{6.12}\right]$

with G grounded

For lamp test, it is necessary to disconnect point(T) from (G) and apply a voltage equal to or greater than +2.2 volts to pin(T). The current required into pin (T) at +2.2 volts is 0.23 MA. For any voltage V_T applied to the test entry pin(T) the current required is equal to $\frac{V_T - .7}{6.45}$ MA

Maximum test entry voltage should not exceed 20 volts. Figure 10 provides net load trade offs that exist under conditions shown in Figure 8. Figure 9 shows the voltage - current requirements for Figure 8. If it is desired to drive both isolating inverter loads and SCR ID loads from medium speed AI/AOI drivers then it will be necessary to increase the up level drive available on the AI/AOI output net. Two such existing schemes are shown in Fig. 11 and Fig. 12.





MEDIUM AND LOW SPEED INPUT REQUIREMENTS

FIGURE 9

UP LEVEL TRADE-OFF CHART

DRIVER	UP LEVEL VOLTAGE	NO. OF II LOADS	NO. OF SCR ID LOADS
Low Speed -	4	1	1
AI/AOPI -	2	0	7
Low Speed -	4	2	1
API/AOPI -	4	1	2
	2	0	13
Med Speed -	2	1	0
AI/AOI -	2	0	5
Med Speed -	2	2	3
API -	2	1	8
	2	0	12

FIGURE 10

SPECIAL MEDIUM SPEED CONFIGURATION

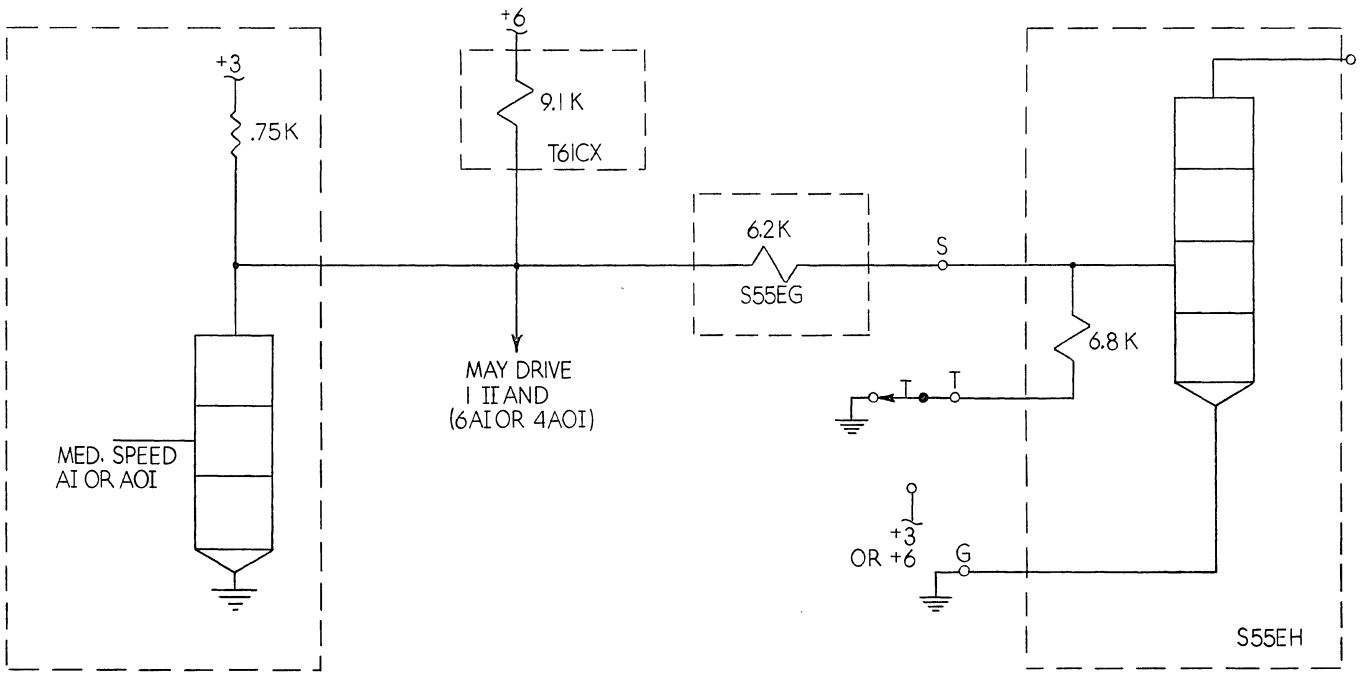


FIGURE 11

SPECIAL MEDIUM SPEED CONFIGURATIONS

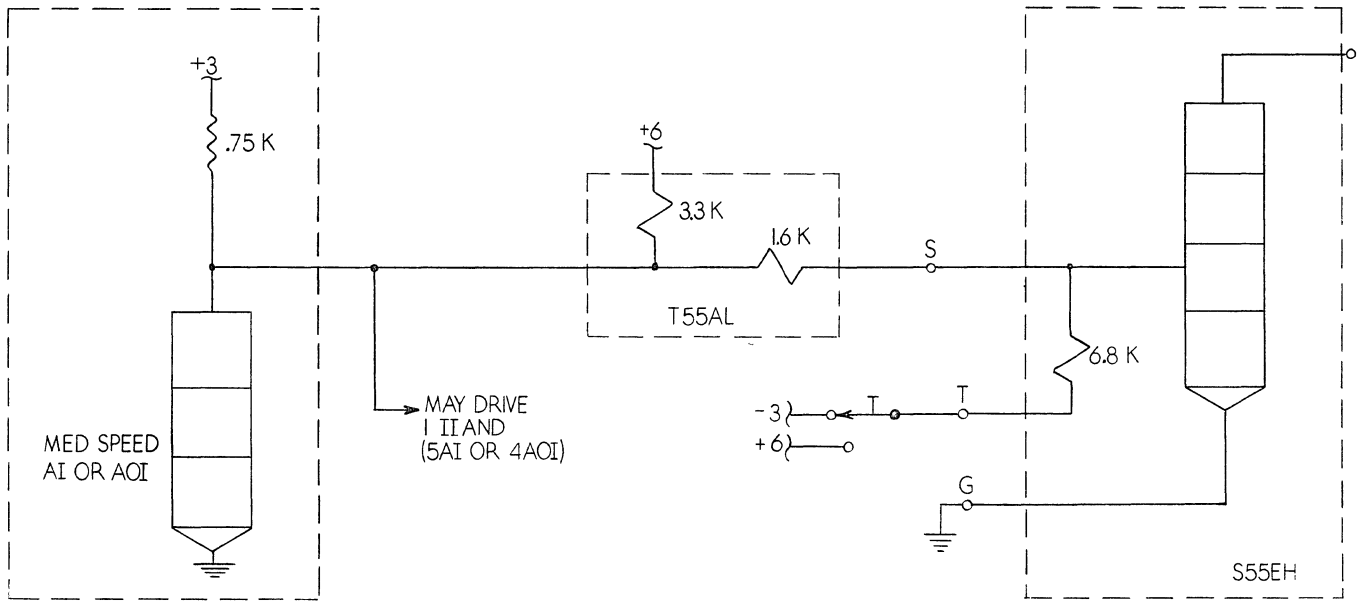


FIGURE 12

8.3 Bussing and Contact Schemes: There are two general methods of interconnecting arrays of SCR modules and lamps.

For bussing the test entry (T) #30 wire size or larger may be used. #30 wire size or larger may also be used to connect into the signal entry (S). No practical limit exists on these lengths. For bussing the ground entry #30 wire size may be used if the total length does not exceed 2 feet and carries current for 1 SCR ID only. If several modules are fed from one ground wire, the length must be reduced accordingly. These lengths are measured from the copper rail buss, which should be size 18 or larger; the lamp AC buss should be size 18 or larger.

Peak currents on bussing (at required voltages) per circuit.

Test entry	.22 MA	Total voltage bussing drop from AC power supply to any module should not exceed 0.2 volts. This includes summation of AC feeder plus ground return.
Signal Entry	.22 MA	
Ground Entry	200 MA	
Lamp AC Entry	200 MA	

Wire Size (Solid Copper)	Voltage Drop Per Foot - Per 200 MA
14	.0005
16	.0008
18	.0013
20	.002
22	.0032
30	.02

9. ADVANTAGES OF SCR INDICATOR DRIVERS

1. Lower servicing cost (higher current capacity of SCR allows use of heavier filament, hence more reliable lamp).
2. Lower product cost since (a) No indicator driver cards are required and (b) Simple AC transformer replaces regulated power supply.
3. More light output from higher current lamp makes its use in back panel lighting more reliable than the 10ESB in high ambient light conditions.
4. All lamp currents isolated from logic areas.
5. All lamps and their associated drivers may be tested simultaneously from the console.
6. DC net loading effect of an SCR indicator driver on a logic net will be under 0.5 ma (up level) at 2 volts.

Printed in U.S.A.

7. Down level loading will be zero (at .3 volts)

8. Because of inherent inductance of the transformer powering the lamps, the cold lamp surge currents will be reduced.

9. The SCR has the ability to provide 2.0 amps peak current and a DC current of .5 amps while remaining in saturation.

10. The replacement of the input base resistor can be at the logic net for isolation of cable capacitance from this net.

11. Only base drive current (under 1 ma) flows in the interconnecting cable.

12. Returning the SCR to a DC voltage provides a latch indicator driver useful in CE servicing.

13. The emitter of the SCR may be referenced to any voltage and hence the driver may be used with any referenced input line. (The transformer is always referenced to the SCR emitter).

14. A single noise shot may turn the SCR on; however, the next negative excursion of AC on the collector will extinguish the SCR. The bulb will not light in this time because of its long thermal time constant. (Over 15 ma).

15. No DC is required on the module, hence its use is independent of existing power supplies in the system.

16. The projected lamp price should be under 30 cents for a lamp three times as reliable as the present 40 ma 10ESB lamp. The lamp will be of the same mechanical dimensions as the 10ESB and will be rated DC at 150 ma and 4.5 volts.

17. The indicator driver will be packaged in a module and plugged directly into the bulb holder. A printed circuit buss under development will common all emitters and test points as desired. Approximate dimensions are:

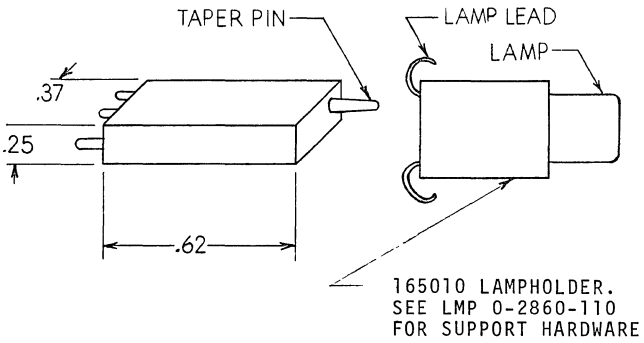


FIGURE 13

18. The indicator driver cost will be in the 50 cent range.

19. Schematic of indicator driver.

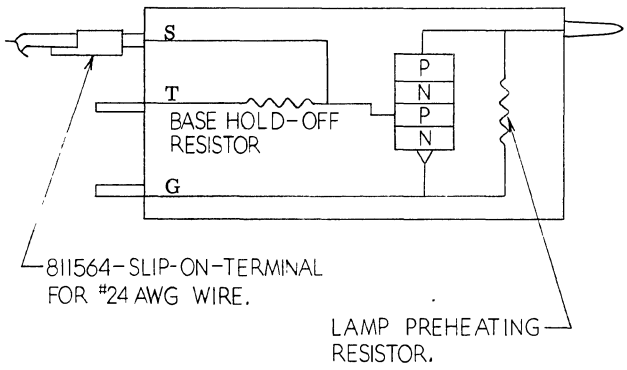


FIGURE 14

IBM **Location Manufacturing Practice**

INTRODUCTION

1.1 SCOPE. This practice describes internal and external signal cabling using SLT hardware and ground rules.

1.2 OBJECTIVE. The intent of the practice is to establish a common understanding of signal cabling and ground rules.

1.3 DEVIATION APPROVAL. Implementation of a practice is expected and deviation is controlled in accordance with the procedures of the concerned functions.

1.4 AUTHORIZATION. This practice was approved by the Equipment Engineering Task Group assigned and dated 1-67.

1.5 DEFINITION. Equipment Engineering is understood to include Test Equipment Engineering, Process Equipment Engineering, Manufacturing Research and/or their equivalents throughout the manufacturing facilities.

RECOMMENDED PRACTICE

2. SIGNAL CABLING

2.1 Inter-Board Cabling. Crossover connector assemblies provide board-to-board signal jumpering. The physical construction is similar to that of flat cable assemblies. Full width assemblies connect board sockets horizontally or vertically in a one-to-one pin relationship. Half-width connectors may be used horizontally to connect half the pins in one socket to the corresponding half in the other socket. (Example: T-T, top-to-top, and B-B, bottom-to-bottom). The half width connectors are used only for horizontal crossover.

Table 1 (below) lists the available crossover connector assemblies. These assembles may be ordered from Kingston.

P/N	Description	Speed (NS)
5802213	crossover asm-horiz. 9 sig (B-B) 1 gnd.	30 & 700
5802214	crossover asm - horiz. 9 sig (T-T) 1 gnd.	30 & 700
5803315	crossover asm - vert. 22 sig, 1 gnd.	30 & 700
5802216	crossover asm - horiz. 22 sig, 1 gnd.	30 & 700

2.2 Inter-Gate Cabling. Flat Cable assembles profide the most common means of gate-to-gate signal transfer. In special applications, twisted pair cables are used. The available cable assemblies are listed in Reference Drawing 811645. The ordering procedures are outlined in a memorandum to SLT users titled, "B/M Structure and Cable Ordering System for Production Systems", dated February 10, 1964. Cables must be ordered by assembly number, length, fold marks,etc. Limited quantities of selected cables may be obtained from Mechanicsburg by referring to the information included in memorandum to SLT users titled, "Temporary Repair Cables", dated August 26, 1965. Also, Central Model Shop-Printed Circuit Area, SDD Lab, Endicott, is equipped to manufacture limited quantities of special cables.

2.3 Gate to I/O Interface Cabling. The gate is I/O interface cabling to accomplished by flat cable assemblies terminated into 24 and 48 position serpent type contact connectors. The machine half of the connector mates with the I/O cable half which usually employs shielded coax for signal transmission. The I/O connectors and nomenclature are fully described in IEP 2-1521-001.

2.4 I/O Cabling. As stated above, the I/O cabling usually employs coax cable for signal transmission. The coax types, maximum lengths, etc. must be determined for each individual application depending on the speeds, delays, line driver and terminator types, and noise considerations involved. The "Signal Cabling" section of the "SLT Design Guide", IEP 2-7100-BKT provides additional information and a listing of reference material pertinent to all of the above areas. The Packaging Mechanical Design Department, SDD Lab, Endicott, is able to provide additional information on signal cabling.

3. DESCRIPTION

3.1 General

3.1.1 Signal cabling hardware includes flat cable assembles, crossover connectors, and ribbon cable with discrete terminating cards for manual assemblies. The ribbon cable and discrete cabling cards should only be considered for model or limited production machines. Flat cable is the basic means for signal cabling due to its automated design, assembly ordering, and routing procedures. There are two sources for ordering flat SLT cables.

1. "The Temporary Repair Cable List" from Mechanicsburg. To order a temporary repair cable, the I&E sheet should identify the following fields.

FIELDS	EXAMPLE
Basic Name =	Cable A
Description =	SLT Tempy Rpr
Part Number =	5800919
Quantity =	1

2. "Engineering Assembly Shop Services" Department in Glendale. This department is to be utilized when a particular length cable is required that is not on the Mechanicsburg listing. This method incorporates a cable "type" part number with the length or "Y" dimension inserted in the description field. To order such a cable, the I&E sheet should identify the following fields.

FIELDS	EXAMPLE
Basic Name =	Cable A
Description =	SLT 16.5 IN LG
Part Number =	5802200
Quantity =	1

Design information can be obtained from reference drawings:

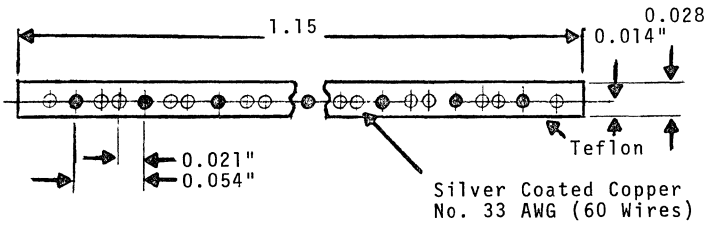
811344 - Cable Fold Types & Markings
811346 - SLT Cable Routing Form Drawing
811367 - Dimensioning Tables - Full and Half Width Cables

Additional information concerning flat cables is available from the SLT Packaging Development Department in Glendale.

3.1.2 Further investigation is required to determine feasibility of cable procurement specified in 3.1.1 for Equipment Engineering practices.

3.2 Flat Cable Assemblies

3.2.1 Material. IBM flat cable is constructed of one plane of #33 AWG signal and ground wires, two ground per signal, enclosed in homogenous or laminated Teflon, available in full and half widths. See Figure 1. Half width falt cable is constructed in the same manner as full width with 27 wires and 0.56 in. width.



● = Signal
○ = Ground

FIGURE 1

CROSS SECTION OF FULL WIDTH FLAT CABLE

3.2.2 Electrical Characteristics. See Engineering Specification 890917, Bulk Flat Cable.

3.2.3 Dimensions. Dimensions are given in Figure 1.

3.2.4 An index of flat cable assemblies for use in 360 Systems is given in Table 2 (taken from reference drawing 811645). Users should note that the following flat cable assembles must be ordered according to the procedures outlined in the above referenced memos, and not by part number only. A listing of "Temporary Repair Cables" is available from the SLT Packaging Development Department in Glendale. These cables can be ordered from Mechanicsburg by part number and may be utilized in special instances.

3.3 Table 2 - Flat Cable Assemblies

P/N	Description	Speed (NS)
5802200	cable asm-20 sig	30 & 700
5802202	cable asm-9 sig (T-B)	30 & 700
5802203	cable asm-9 sig (B-T)	30 & 700
5802204	cable asm-9 sig (B-B)	30 & 700
5802205	cable asm-8 sig (T-B)	30 & 700
5802206	cable asm-8 sig (B-T)	30 & 700
5802207	cable asm-8 sig (B-B)	30 & 700
5802208	cable asm-7 sig (T-T)	30 & 700
5802209	cable asm-7 sig (B-T)	30 & 700
5802210	cable asm-7 sig (T-B)	30 & 700
5802211	cable asm-6 sig (B-T)	30 & 700
5802212	cable asm-6 sig (B-T)	30 & 700
5802918	cable asm-20 sig (resistor terminated)	30
5802919	cable asm-20 sig 2 hi to 3 hi	30
5802923	cable asm-20 sig resistor terminated 1 hi to 2 hi	30
5802925	cable asm-20 sig special transfer	30
5802930	cable asm-20 sig resistor terminated	30
5802935	cable asm-20 sig resistor terminated	30
5802942	cable asm-20 sig resistor terminated	30

Reference Drawings for Manual Routing

P/N	Description
811645	Cable Index, Cable Assemblies, Crossover Assemblies
811344	Cable Fold Types and Markings
811346	Cable Routing Form, Six and Split Six
815071	Flat Cable Dimension Tables, Inter-Lattice
815130	90° Board Dimension Tables
815160	Cable Routing, 90° Board
811366	Six and Split Six Dimensioning Tables, 2 hi Gates

Spacer Drawings

813086	Spacer Application Reference Drawing
811236	Spacer, Horizontal, Full, Adhesive
811237	Spacer, Vertical, Full, Adhesive
811641	Spacer, Horizontal, Half, Adhesive
811642	Spacer, Vertical, Half, Adhesive
811223	Spacer, Bulk, Full, Non-Adhesive
811639	Spacer, Bulk, Half, Non-Adhesive

Tape Drawings (required on homogeneous coated cable)

811790	Tape Fold Application, Full
811791	Tape Fold Application, Half
811788	Tape, Bulk, Full (72 Yard Roll)
811789	Tape, Bulk, Half (72 Yard Roll)

Cable Retainers

Rubber straps for use on gate:

811427	straight
813519	cross

3.4 Table 3, taken from Gate and Mounting Hardware reference drawing 811446, lists the applicable clamp part numbers for typical uses as shown in Figure 2. (Select "Group 3" from Table 3.)

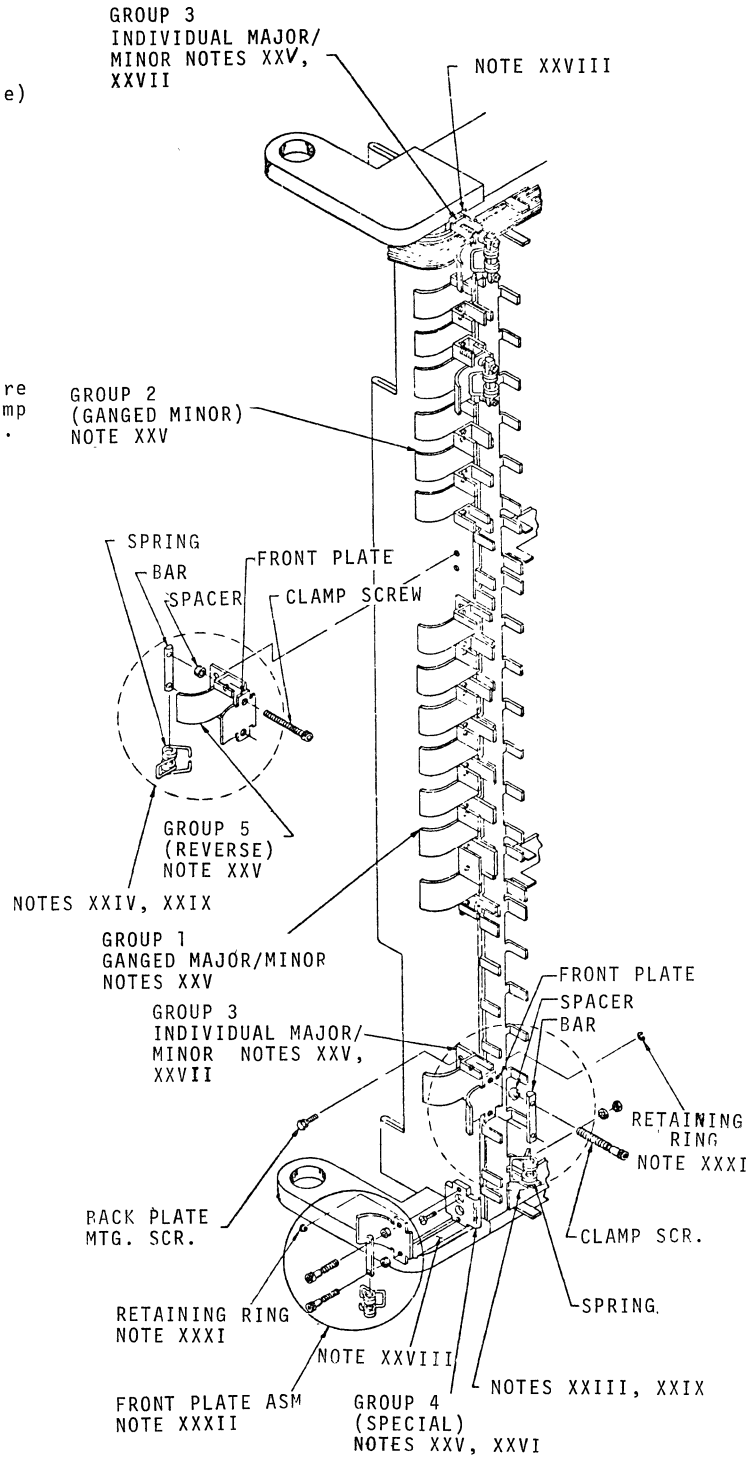


FIGURE 2
CABLE CLAMPS

3.4.1 Table 3 CABLE CLAMPS AND GROUPINGS

GROUPING CHART (NOTE XXV)											
Spring Mounting Type	Normal (Note XXIII)								Reverse (Note XXIV)	
Group	1		2		3 (Note XXVII)		4 (Note XXVI)		5	
Description	Part No.	Qty.	Part No.	Qty.	Part No.	Qty.	Part No.	Qty.	Part No.	Qty.
Back Plate 1/2" finger	815165	1	815166	1	815167	1	Available as cast part only		815168	1
Back Plate 1" finger	815169	1	815170	1	815171	1			815172	1
Back Plate 1-1/2" finger	815212	1	815213	1	815214	1	815215	1	815216	1
Back Plate Mtg. Scr.	813706	5	813706	4	813706	2	See chart 3	2	813706	2
Front Plate	S 815217	1	S 815217	1	815217	1	815217	1	815218	1
Spacer	E 815219	2	E 815219	2	815219	2	815219	2	815219	2
Bar	E 815220	1	E 815220	1	815220	1	815220	1	815220	1
Spring	* 813321	1	* 813321	1	813321	1	813321	1	813321	1
Clamp Screw	See Cht 1	2	* See Cht 1	2	See Cht 1	2	See Cht 1	2	See Cht 2	2
Retaining ring	815210	2	815210	2	815210	2	815210	2		
Back plate mtg. nut							11598			
Back plate mtg. lock washer							9092			

*
* Multiply each quantity by number of cable positions used up to 6 max.
* Multiply each quantity by number of cable positions used up to 7 max.

	CHART 1		CHART 2		CHART 3	
Channel Usage	Cable Build-Up	Screw Part No.	Cable Build-Up	Screw Part No.	Gate Construction	Screw Part No.
Minor		815173		149898	Channel	367
	0-.43	815173	0-.24	149898		
	.44-.94	815174	.25-.74	186931		
Major	.95-1.50	815175	.75-1.50	438582	Tubular	6286

NOTES:

XXII	Order of mounting clamp backplates as shown is not absolute, and will depend upon individual gate requirements. Pictorial representation should be used only for orientation purposes.
XXIII	Normal spring mounting.
XXIV	Reverse spring mounting -- if interface exists between normal spring mounting and adjacent gate, external machine cover, etc. use reverse spring mounting which utilizes short arc frontplate and transfers spring, spacers, and tapped bar into backplate.
XXV	Refer to grouping chart and select compatible parts grouping, Spring mounting and backplate are determinging factors for groups.
XXVI	If space limitation in the cable loop area of the machine frame is critical, special backplate may be used. In the area where this backplate is used, the gate holes must be enlarged to .213 diameter -- through both sides of tubing, if gate is of tubular construction; or through single thickness if channel construction.
XXVII	If gate cable population is such that the ganged major/minor or ganged minor backplate is unwarranted, individual major/minor backplates(s) may be used as required.
XXVIII	If interference exists between ear on backplate/frontplate and gate hinge, hinge must be grooved to accommodate.
XXIX	Tighten clamp screws only until bar initially contacts spacers. Do not overtighten as this may result in damage to cables and/or clamp.
XXX	Select applicable clamp mounting holes and indicate on gate form drawing by checking applicable holes in the option block.
XXXI	Use of retaining ring bar captive front plate assembly applies to all areas where normal spring mounting exists.
XXXII	Complete assembled front plate asm. available in three sizes: Part No. 815224 (for .0-.43 cable Build-up) Part No. 815225 (for .44-.94 cable Build-up) Part No. 815226 (for .95-1.50 cable build-up)

3.5 Serpent Contact Connectors

3.5.1 Serpent contacts are gold plated phosphor bronze; contact is made by dual mating on the surface. See below.

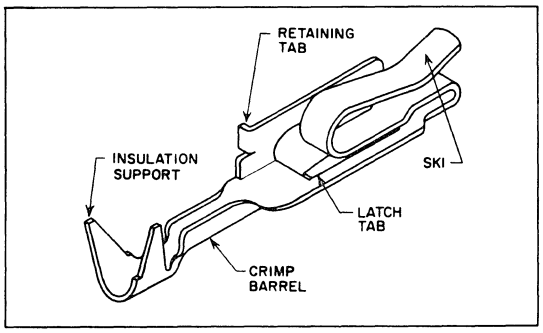
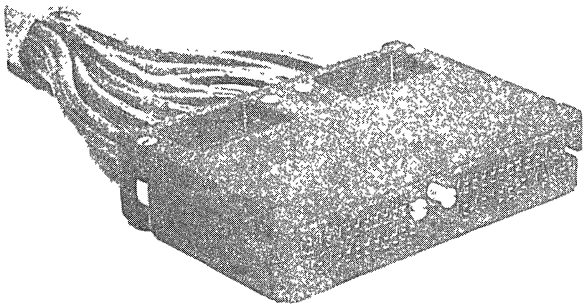


FIGURE 3

SERPENT CONTACT

3.5.2 Serpent contact connector assemblies can be used to terminate coaxial or discrete wires, and also as a transition block from coaxial wire to flat cable. See Figure 4. These connector assemblies use serpent contacts to make electrical connection. There are two basic block configurations: 48 position and 24 position (the 24 position block does not mate with the 48 position block). Reference drawings 5362310 (48 position serpent connector, separate shields) and 5362320 (48 position serpent connector, common shields), Engineering Specification 877223, and Standards Publication IEP 2-1521-1 in Book 4-1 describe and provide application information and part numbers for the various types of 48 position connector assemblies. IEP 2-1521-1 describes and lists the Connector Group bills of material, Wire Assembly Group bills of material, and External Cable Assemblies.



SERPENT CONTACT CONNECTOR

FIGURE 4

3.5.3 Description and part numbers for the 24 position serpent contact connectors are given in IBM Technology News, Volume 4, No. 5 dated 5/66. Reference drawings 5393113 (24 position serpent connector, common shields) and 5400508 (24 position serpent connector, separate shields) are available from Poughkeepsie Reproduction department.

3.5.4 The 48 and 24 position blocks both provide separate or common shielding. The 48 position block is normally used with a maximum of 20 signal wires, each with an individual shield connection; however, it is possible to terminate 24 signal lines with separate shield connections. The 48 position block can also terminate a maximum of 40 signal wires by connecting the shield drain wires to commoning boards, allowing eight individual grounds to be carried through the block.

The 24 position connector is normally used to terminate a maximum of 10 signal wires with separate shield terminations; however, it can also be used to terminate 12 signal lines with separate shield connectors. With the common shielding, the 24 position block can terminate 20 signal wires. When the transition half (that half of the connector block which accepts flat cable terminating cards) of a serpent connector block is used, the number of discrete or coax signal wires connected to the flat cable is limited by the signal capacity of the flat cable.

3.6 Discrete Cabling

3.6.1 "Discrete" cable assemblies consist of ribbon cable, cable cards, strain reliefs, and rivets. Discrete cabling involves a unique design and local manufacture, as opposed to selection of preferred flat cable assemblies and centralized manufacturing in Kingston. The following hardware is commonly used for discrete cabling:

Ribbon Cable (See Standards Manual 4-2, IEC 5-2062-L)

P/N	Conductors	AWG	Width	Thickness
587477	8TP	#24	1.06	.145
760243	16	#22	1.02	.063
5352957	20	#24	1.06	.053

Cable Cards, used for terminating above cables

5800610	20 signal, 1 ground
5800634	23 signal, 1 ground

Strain Reliefs

5352958	1 hi, clamp capacity .040
5352963	1 hi, clamp capacity .040
5352964	1 hi, clamp capacity .095
5352960	2 hi, clamp capacity .095
5352967	2 hi, clamp capacity .040
5353922	1 or 2 hi, clamp capacity .095 does not extend beyond card

(NOTE: P/N 595720 - rivet, used with above strain reliefs.)

3.7 Miscellaneous Cable Assemblies. The following cable assemblies are available from Kingston.

P/N	Description
5802934	cable asm-18 sig twisted pair
5802938	cable asm-18 sig network terminated
5802939	cable asm-20 sig flat ribbon
5802917	cable asm, triple twist, 3 hi term to end

4. TABLE OF HARDWARE CONSTANTS

Capitance	
Printed wiring	1.8 to 2.2 pf/inch (add 0.4 pf/ inch for each line
Flat cable	1.7 pf/inch
Paddle card	2.0 pf
Via hole	0.6 pf
Contact (small card)	3.0 pf
Transistor collector	6.0 pf
Diode	2.5 pf
Resistance	
Printed wiring	0.5 ohms/ft
Flat cable	0.233 ohms/ft
Coax cable 535912	0.5 ohms/ft
Coax cable 535914	0.098 ohms/ft
Coax cable 595712	0.12 ohms/ft
Coax cable 595997	0.048 ohms/ft
Discrete wire (#30)	0.111 ohms/ft
Serpent connector	0.4 ohms (Spec. 877223)
Delays	
Printed wiring (large board)	1.96 to 2.28 nsec/ft
Printed wiring (small card)	0.156 to 0.165 nsec/ft
Discrete wire (large board)	1.3 to 1.5 nsec/ft
Flat cable	1.4 to 1.6 nsec/ft
Contact (small card)	0.12 nsec average
Cable paddle cards (laminated)	0.22 to 0.33 nsec
Cable paddle cards (non-laminated)	0.15 to 0.2 nsec
Coax cable	1.27 nsec/ft