3–62–0

THEORY OF OPERATION

OF

DISPLAY SYSTEM

FOR

AN/FSQ-7 COMBAT DIRECTION CENTRAL

AND

AN/FSQ-8 COMBAT CONTROL CENTRAL

VOLUME I

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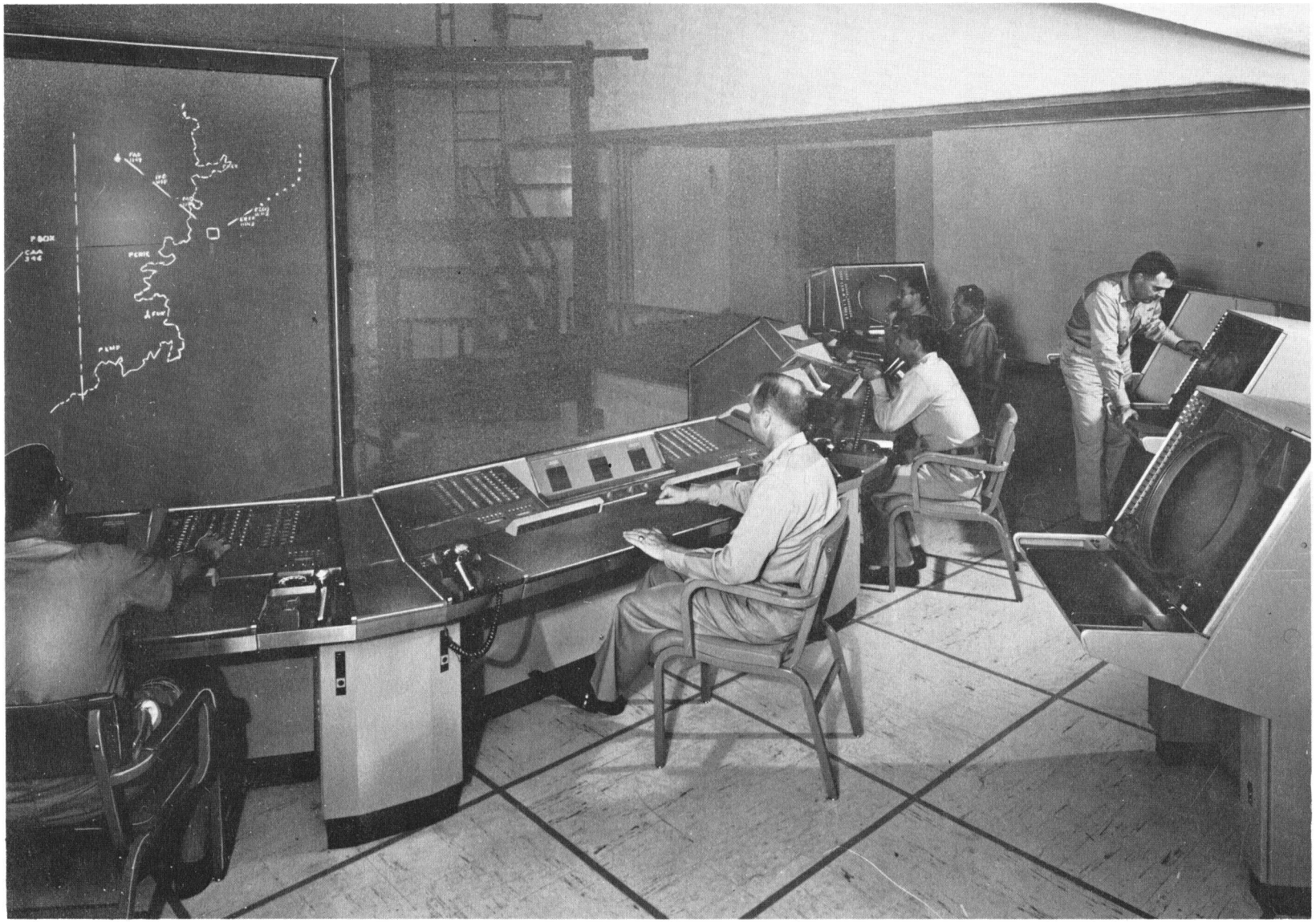


Frontispiece. Operating Personnel at Command Post of Display System

PART 1

INTRODUCTION

CHAPTER 1

PURPOSE AND SCOPE OF MANUAL

1.1 PURPOSE

This manual provides a theory of operation for the Display System in the AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central. Combat Direction and Combat Control Centrals in the SAGE System are complex mechanisms of highly developed electronic schemes. The proper operation and maintenance of such intricate equipment make it mandatory for operating personnel and field engineers to have available an organized compilation of the related theory.

1.2 SCOPE

The AN/FSQ-7 and AN/FSQ-8 are two separate systems but, with comparatively few exceptions, differ so little from each other that a combined manual could cover both systems if the exceptions were noted. This manual is the result of such an effort; the differences are listed in Part 7.

1.2.1 Scope of Equipment Differences

Basically, the differences in equipments result from tactical requirements. The AN/FSQ-8 processes track data (TD) only; the AN/FSQ-7 processes both radar data (RD) and track data. This manual, therefore, is essentially the theory of operation for the more comprehensive system, the AN/FSQ-7. Material, both text and illustrations, that would normally be excluded from the AN/FSQ-8 is set off with an asterisk or, in the case of the drawings, with a broken line. These devices are used as an example, and appear only in the beginning of the book.

1.2.2 Division of Contents

The contents of the manual is arranged in seven parts. Part 1 is an all-inclusive introduction of display units. A common description and the logic-function relationship of the units to the complete system are given. The sequence in which the units are introduced dictates the general order of their detailed discussion in the manual. Part 2 contains a general theory of cathode-ray tubes (CRT) and the specific theory of Display System CRT's. This organization of Parts 1 and 2 was designed to give the reader a broad working knowledge of the Display System and a reference to the detailed theory.

Part 3 is the detailed operation of the digital display (DD) elements. Part 4 presents the detailed operation of the situation display (SD) elements. Part 5, Associated Equipment, is separated into nine chapters with a complete chapter devoted to an individual element or to equipment associated with the Display System, such as the photographic recorder-reproducer, the display consoles, the display tester element, etc. Part 6 discusses the manual data input (MDI) element and its various input devices. Part 7, titled AN/FSQ-8 Combat Control Central Essentials, has Chapter 1 introduce the scope of the differences and Chapter 2 list the specific differences.

1.3 RELATIONSHIP TO OTHER MANUALS

The Display System is logically a part of all the systems within the AN/FSQ-7 and -8; thus, this Display System manual is related to every other theory of operation manual. This manual is directly related to 3-12-0, *Introduction to AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central, 3-3-0, Special Circuits for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central, and 3-252-0, Schematics for Display System of AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central.*

1.4 LIST OF NOMENCLATURE

Table 1–1 lists the major units and components of the Display System. The listing is by unit number, the official AN designation, and the common name for the unit.

TABLE 1–1. UNITS ASSOCIATED WITH DISPLAY SYSTEM, AN/FSQ-7

UNIT NO.	COMMON NAME	AN NOMENCLATURE	CLASS	QUANTITY	FIGURE NUMBER
1	Duplex maintenance console	Duplex Maintenance Console OA-1006/FSQ	Duplex	2	1–1
22	Main drum	Main Magnetic Drum Unit RD-158/FSQ	Duplex	2	1–2
23	MDI	Manual Data Input Unit SN-169/FSQ	Duplex	2	1–3
24	SDGE	Situation Display Generator CV-390/FSQ	Duplex	2	1–4
25	DDGE	Digital Display Generator CV-391/FSQ	Duplex	2	1–5
28	MI interconnecting unit	Manual Data Interconnecting Unit J-726/FSQ	Duplex	2	1–6
30	Warning light data storage unit	Warning Light Data Storage Unit RD-31/FSQ	Duplex	2	1–7
45	Duplex switching	Computer Switching Control C-2045/FSQ	Duplex	2	1–8
		Power Supply Set Control C-2046/FSQ	Duplex	1	1–8
47	Simplex maintenance console	Simplex Maintenance Console OA-1010/FSQ	Simplex	1	1–9
91	Warning light interconnecting unit	Warning Light Interconnecting Unit J-727/FSQ	Duplex	1	1–10
177, 178	Patching panel	Panel, Patching, Signal Data SB-602/FSQ	Duplex	4	1–11
250	Command Post	Command Post Console OA-1013/FSQ	Simplex	1	1–12
251, 252	PRR	Recorder-Reproducer, Photographic KD-6 (1)	Simplex	2	1–13
352, 353, 354	CEP	IBM 020 Computer Entry Punch	Simplex	3	1–14
	Area discriminator	Area Discriminator Pickup Unit F-298/FSQ	Simplex	2	1–15
	Aux console	Auxiliary Display Console OA-1287/FSQ	Simplex*	47	1–16
	DB	Signal Distribution Box	Duplex	18	1–17
	DD unit	Digital Display Unit (SD Console) IP-350/FSQ	Simplex	71	1–20
		Digital Display Unit (CP Console) IP-3841/FSQ	Simplex	11	1–12

TABLE 1-1. UNITS ASSOCIATED WITH DISPLAY SYSTEM, AN/FSQ-7 (cont'd)

UNIT NO.	COMMON NAME	AN NOMENCLATURE	CLASS	QUANTITY	FIGURE NUMBER
		Digital Display Unit (Type C and D Aux Console) IP-385/FSQ	Simplex	40	1-16
	Light gun	Light Gun, Data Selecting MX-1900/FSQ	Simplex	65	1-18
	Optical pointer	Lecture Pointer, Electrical MX-2090/FSQ	Simplex	11	1-19
	SD console	Situation Display Console OA-1008/FSQ	Simplex**	91	1-20
	Semiautomatic camera	Still Picture Camera KD-16A	Duplex	2	1-21
	Side wing	Control Panel, Input Data Selection C-1825/FSQ	Simplex	85	1-22
		Control Panel, Input Data Selection Special C-2020/FSQ	Simplex	20	1-23

**Auxiliary consoles: Units 45, 174, and 175 are duplex.*
***SD consoles: Units 167, 168, and 171 are duplex.*

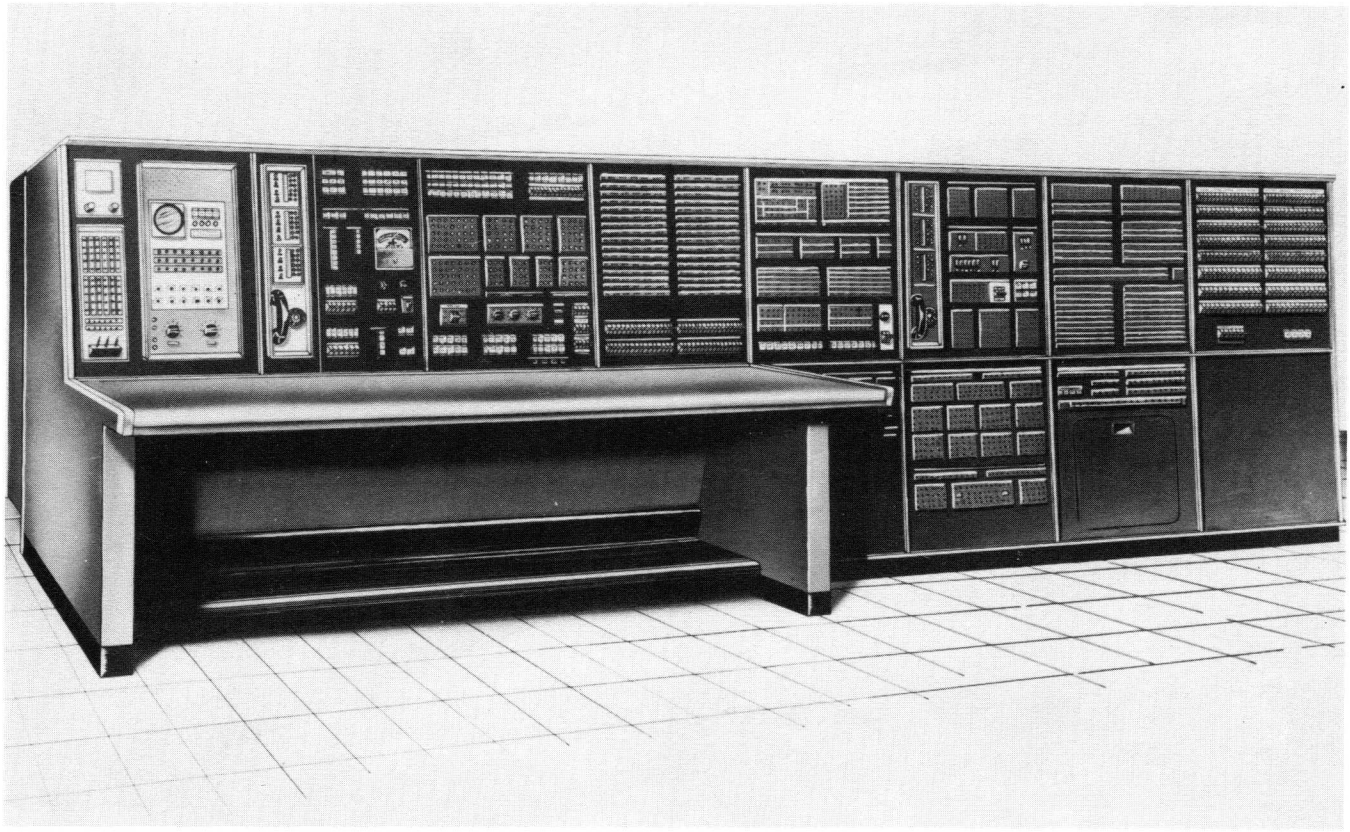


Figure 1-1. Controls for Display System, Duplex Maintenance Console, OA-1006/FSQ

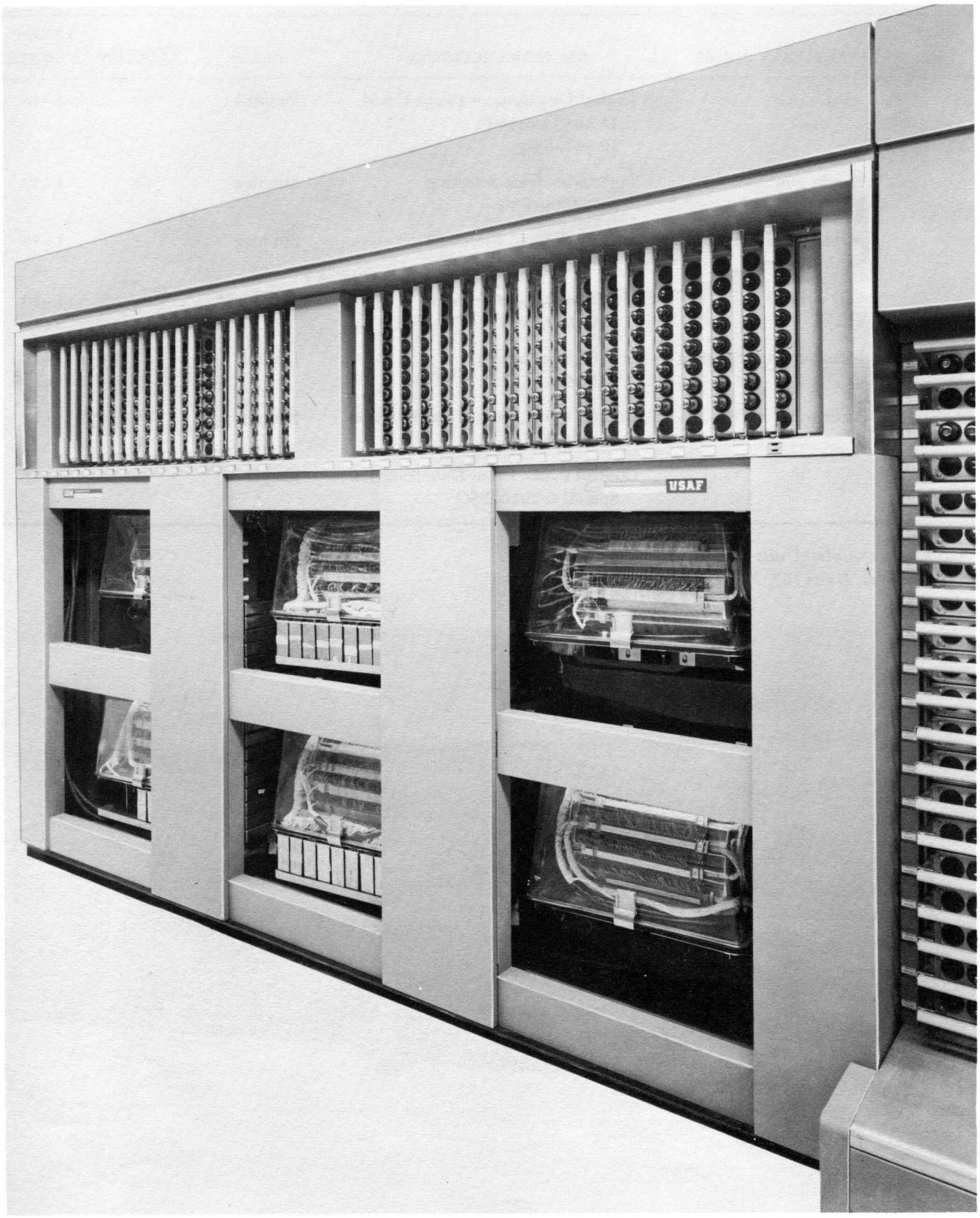


Figure 1–2. Main Magnetic Drum Unit, RD-158/FSQ

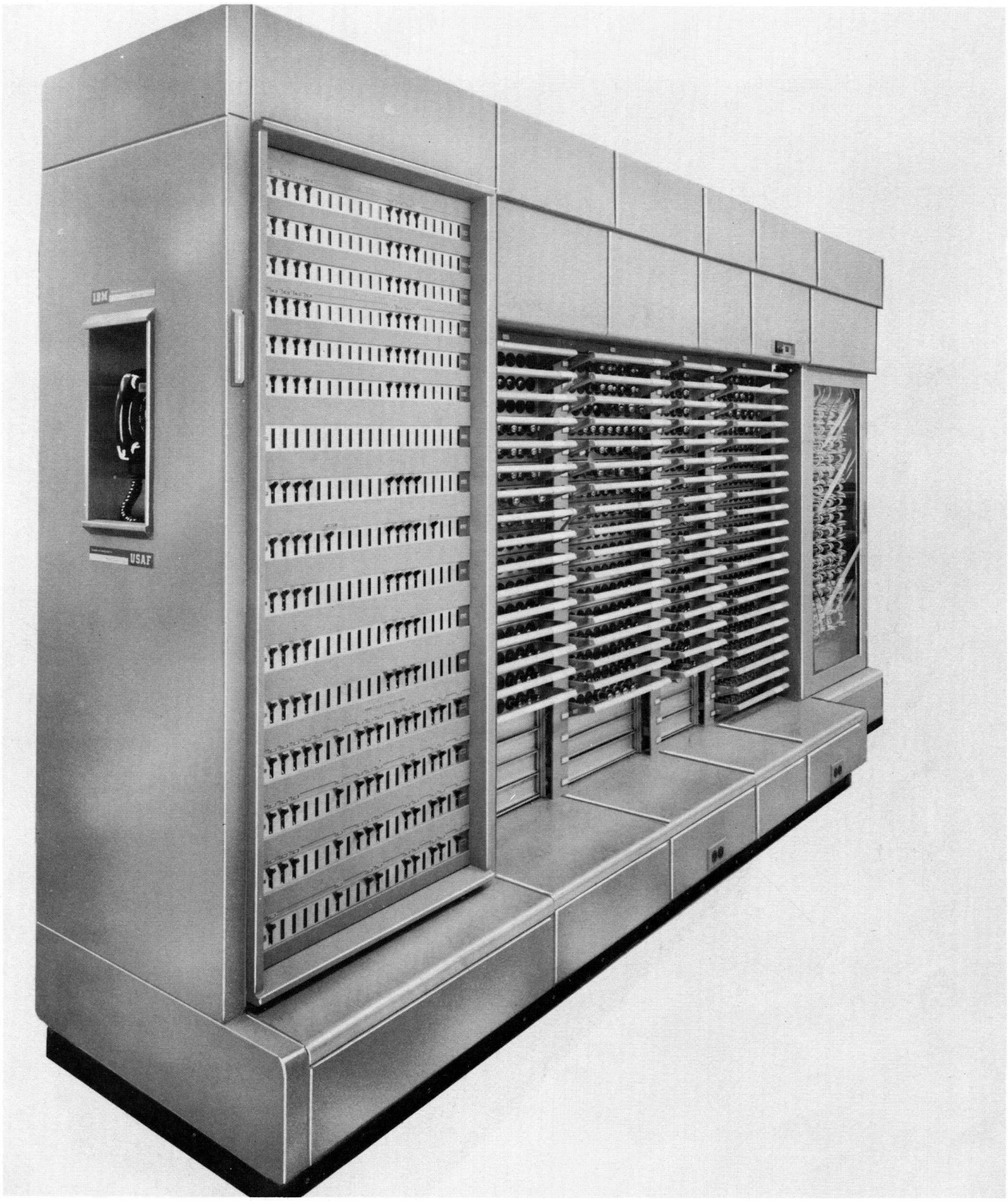


Figure 1-3. Manual Data Input Unit, SN-169/FSQ

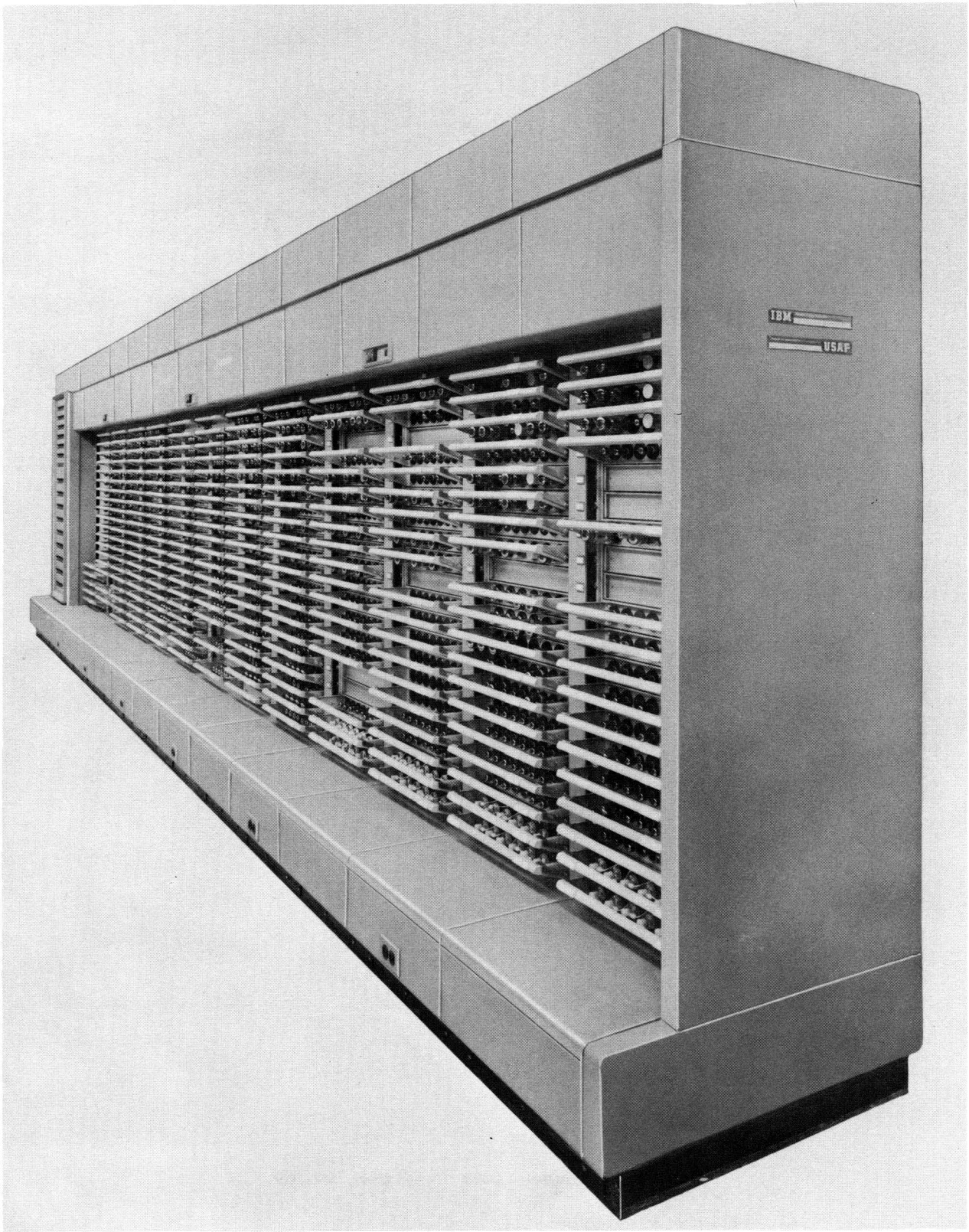


Figure 1–4. Situation Display Generator, CV-390/FSQ

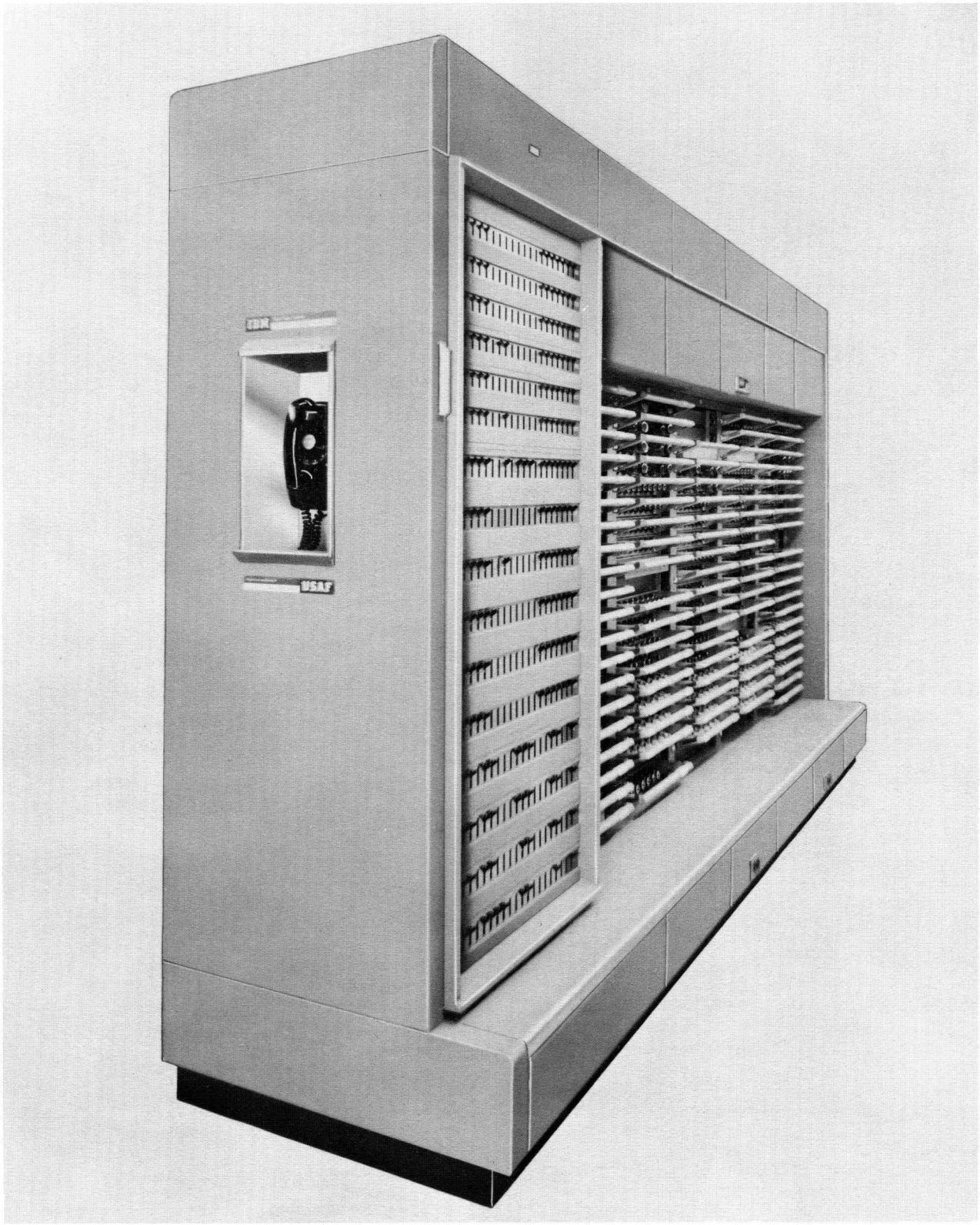


Figure 1–5. Digital Display Generator, CV-391/FSQ

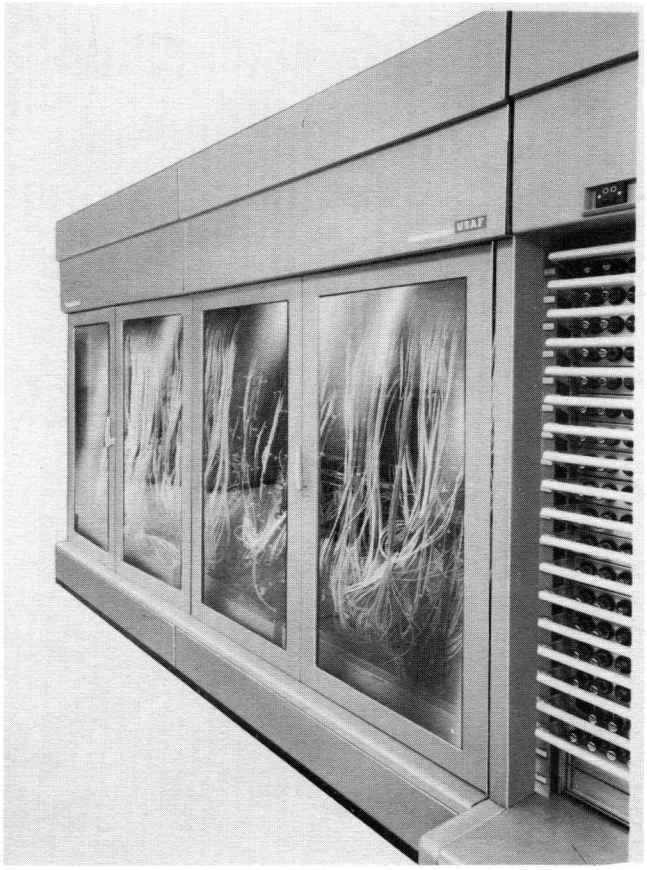


Figure 1–6. Manual Data Interconnecting Unit, J-726/FSQ

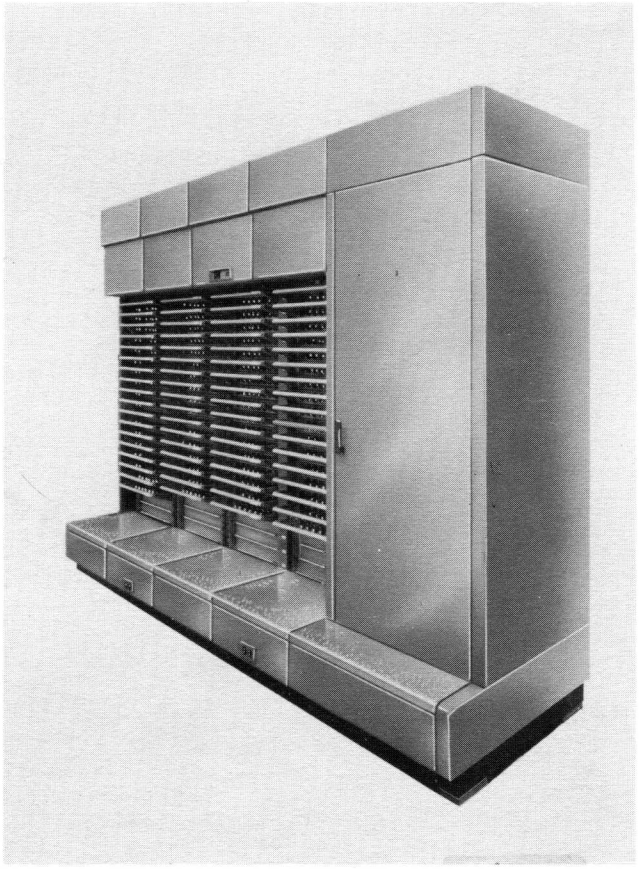


Figure 1–7. Warning Light Storage Unit, RD-31/FSQ

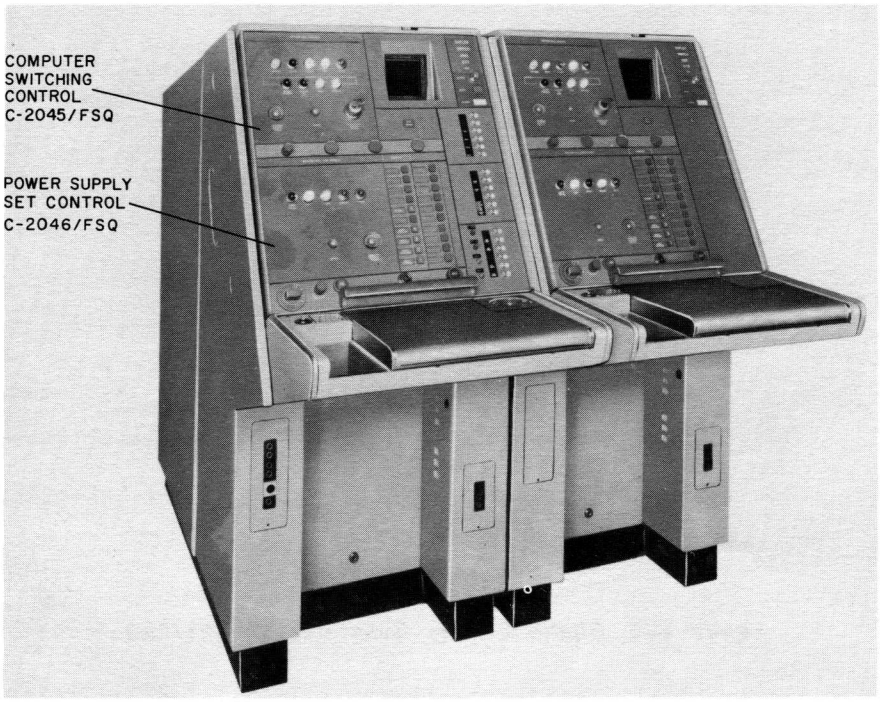


Figure 1–8. Duplex Switching Console

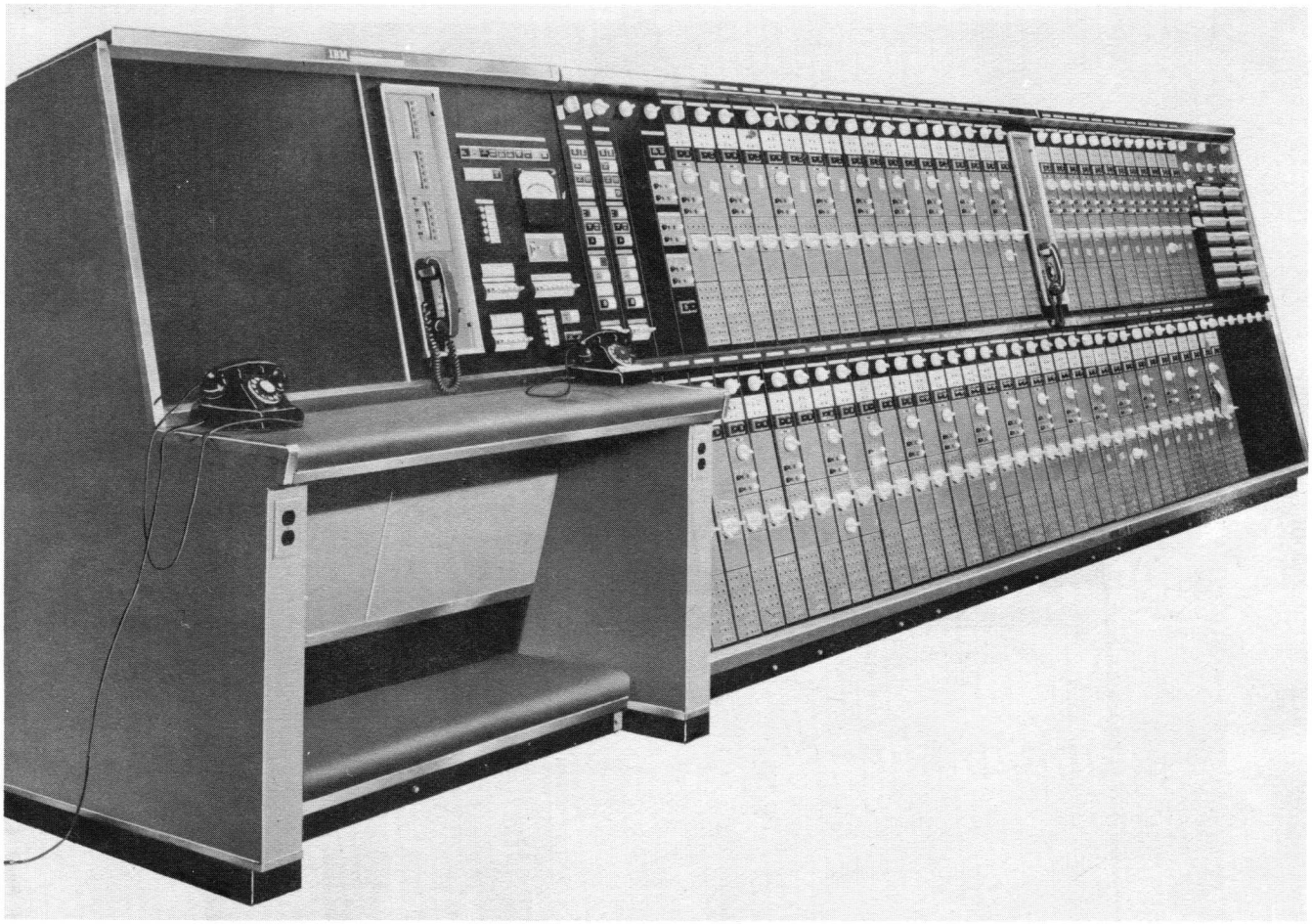


Figure 1–9. Simplex Maintenance Console, OA-1010/FSQ

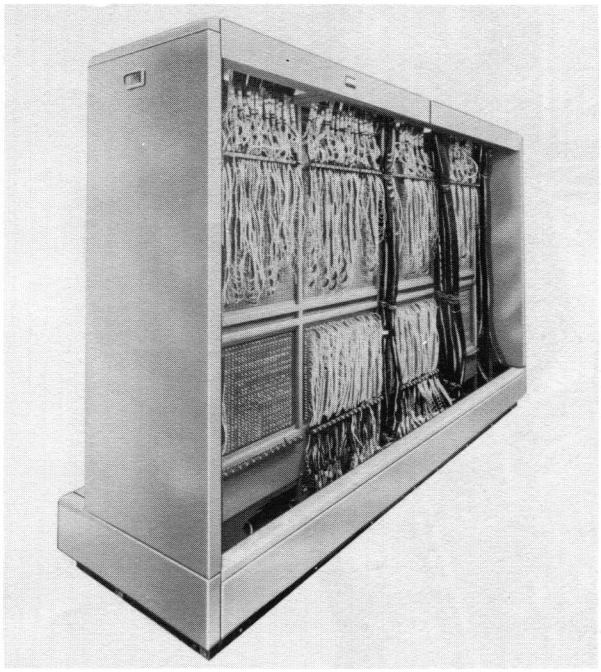


Figure 1–10. Warning Light Interconnecting Unit (Rear View), J-727/FSQ

Figure 1–11. Signal Data Patching Panel, SB-602/FSQ

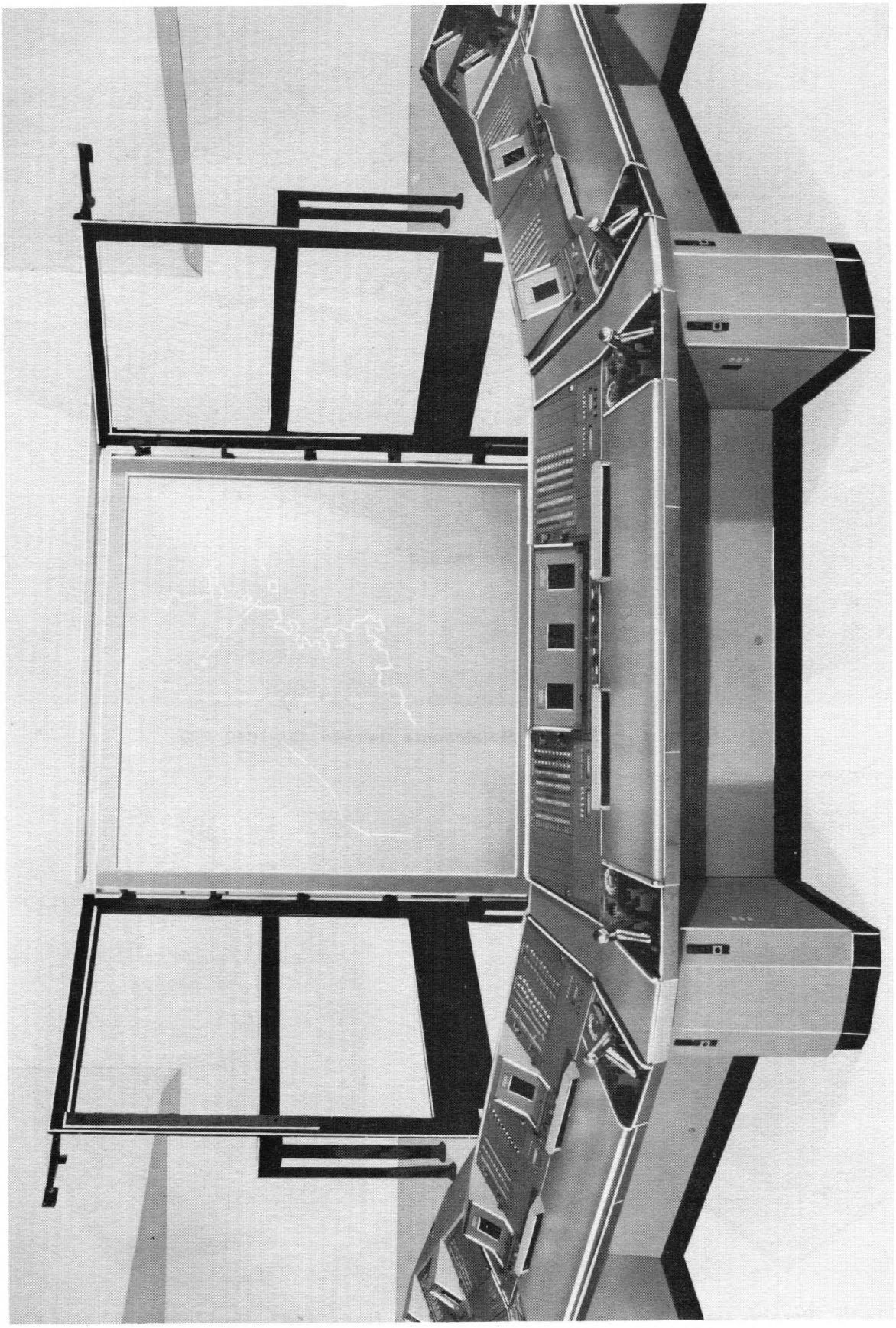


Figure 1–12. Command Post Console, OA-1013/FSQ

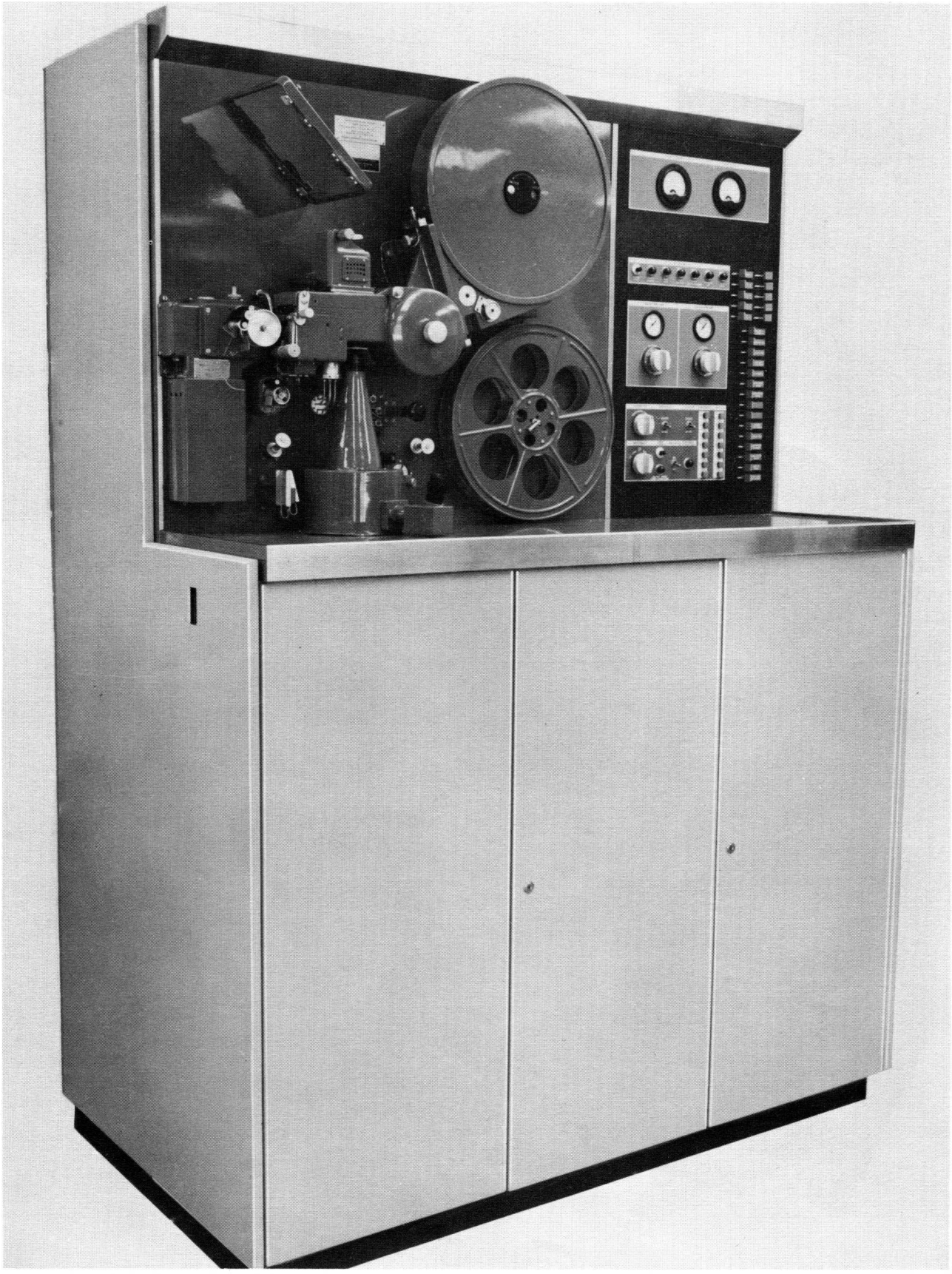


Figure 1–13. Photographic Recorder-Reproducer Unit, KD-6 (1)

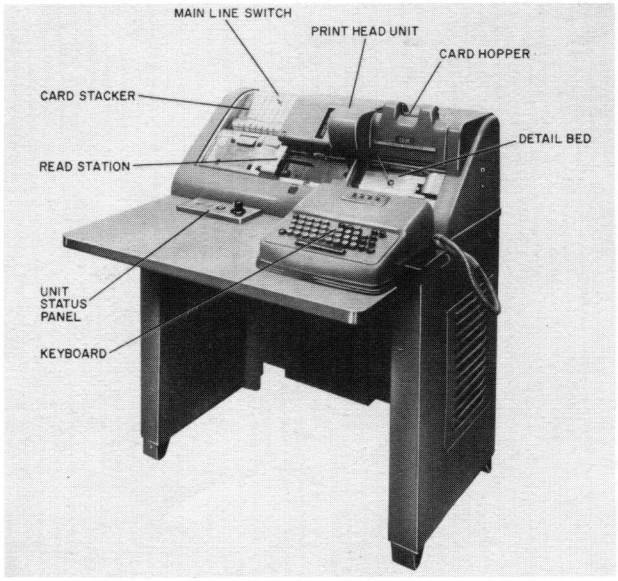


Figure 1–14. Computer Entry Punch, IBM 020

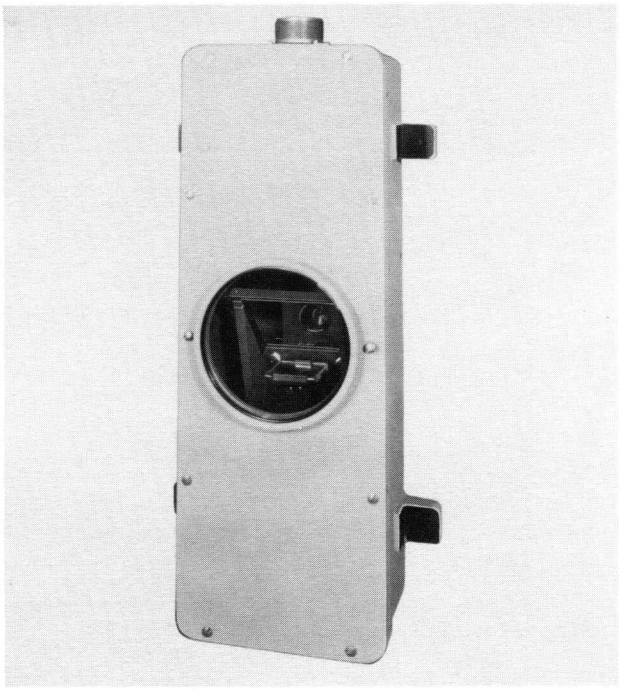


Figure 1–15. Area Discriminator Pickup Unit, F-298/FSQ

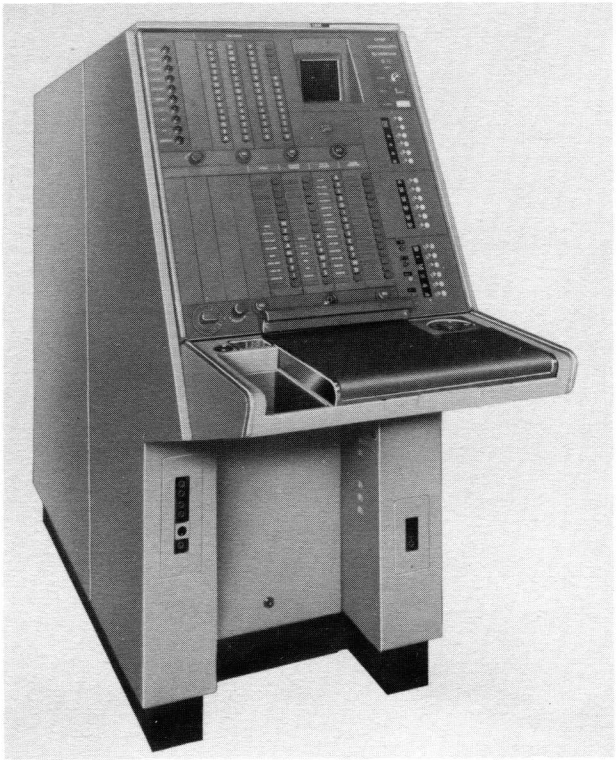


Figure 1–16. Auxiliary Display Console (with DD Unit), OA-1287/FSQ

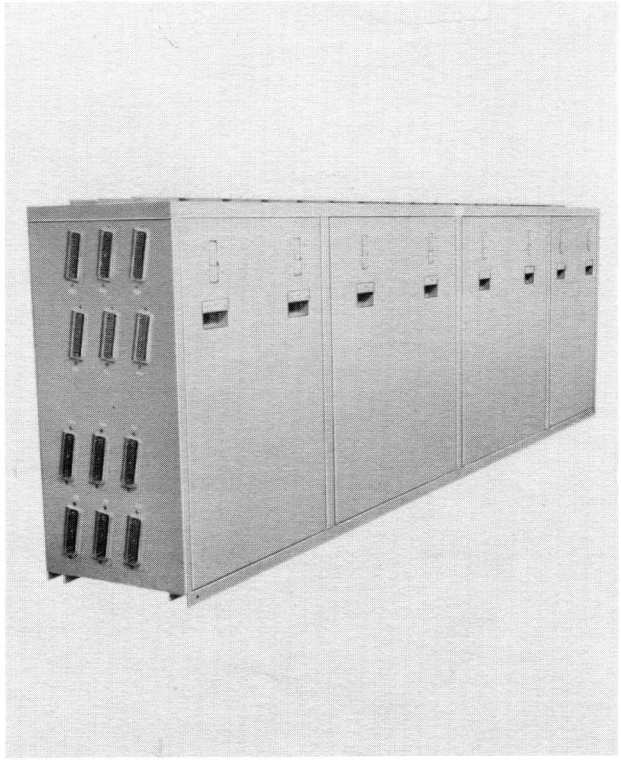


Figure 1–17. 10-1/2-Foot Signal Distribution Box

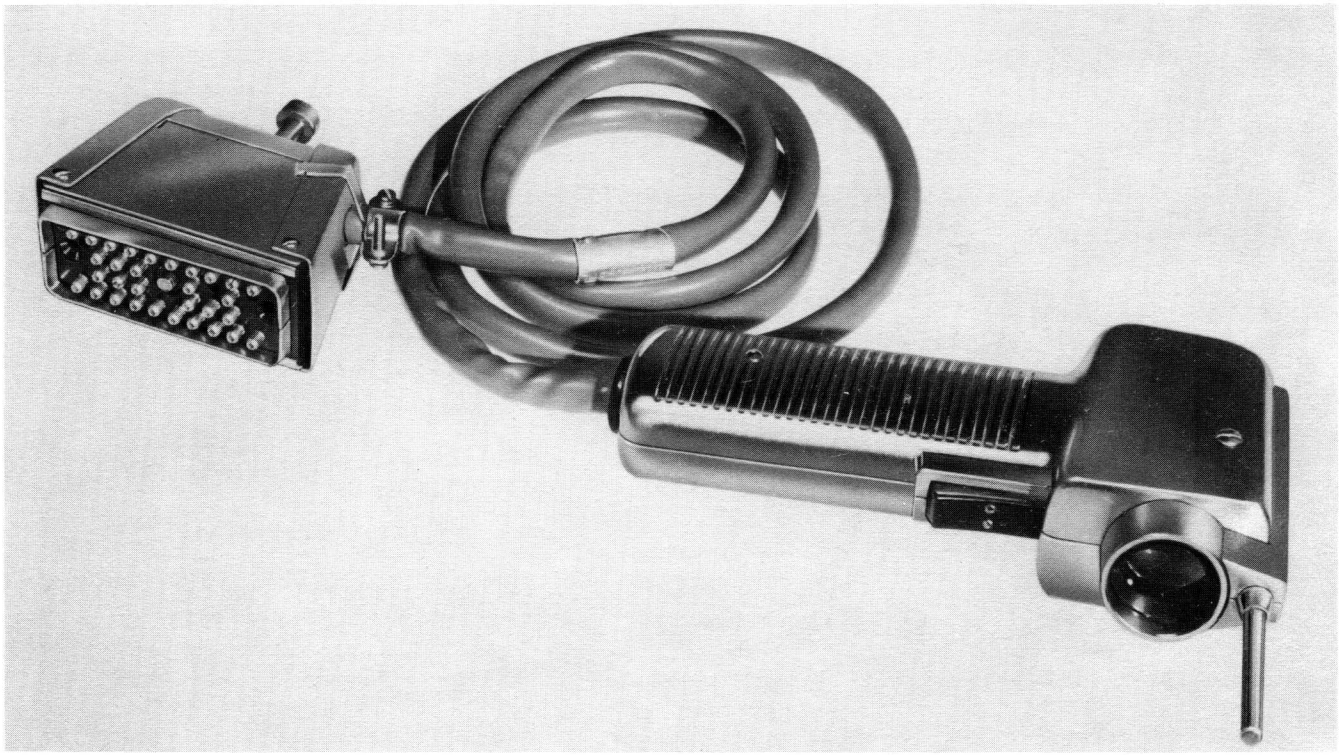


Figure 1–18. Light Gun, MX-1900/FSQ

Figure 1–19. Optical Pointer, MX-2090/FSQ

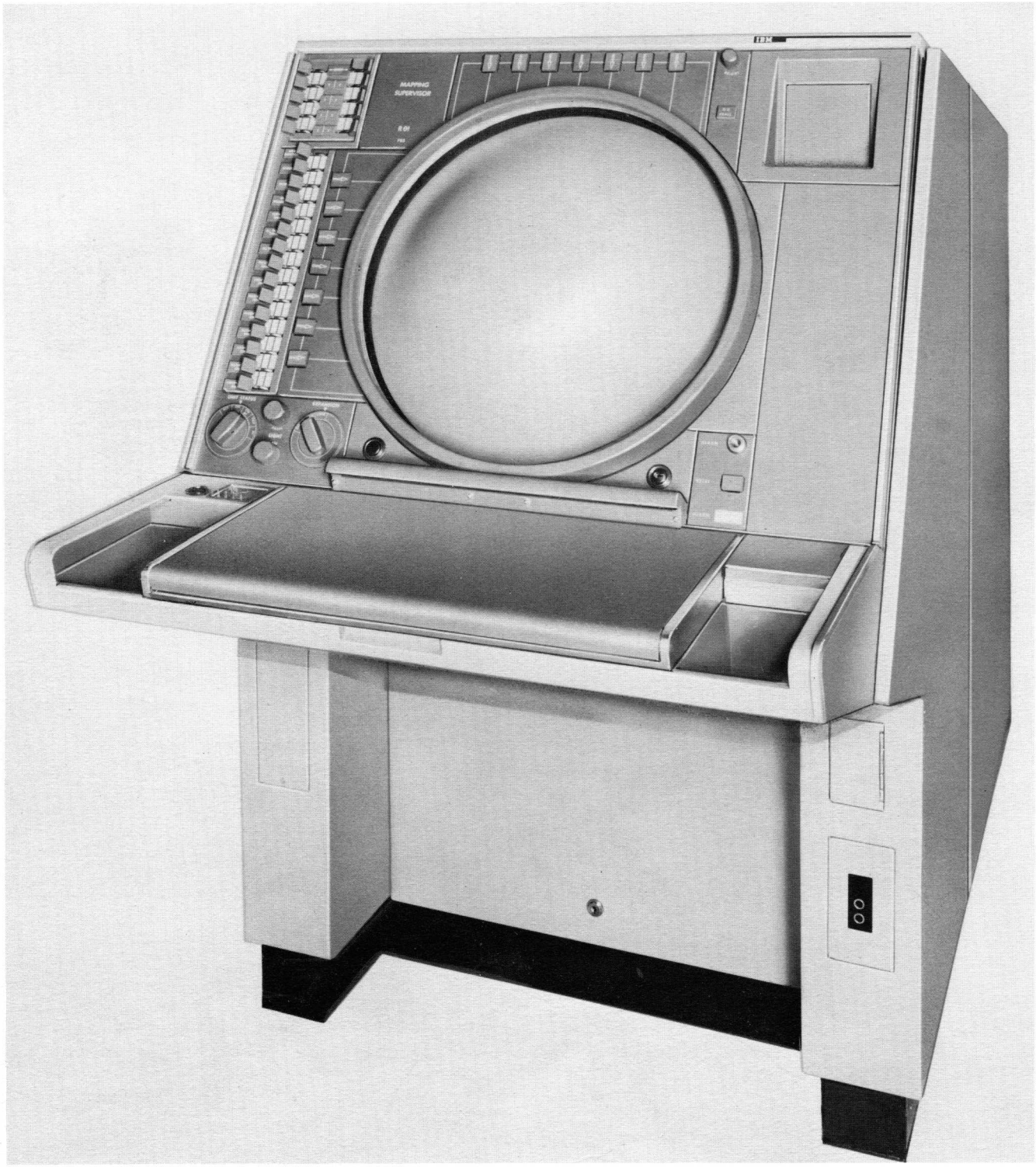


Figure 1–20. Situation Display Console, OA-1008/FSQ

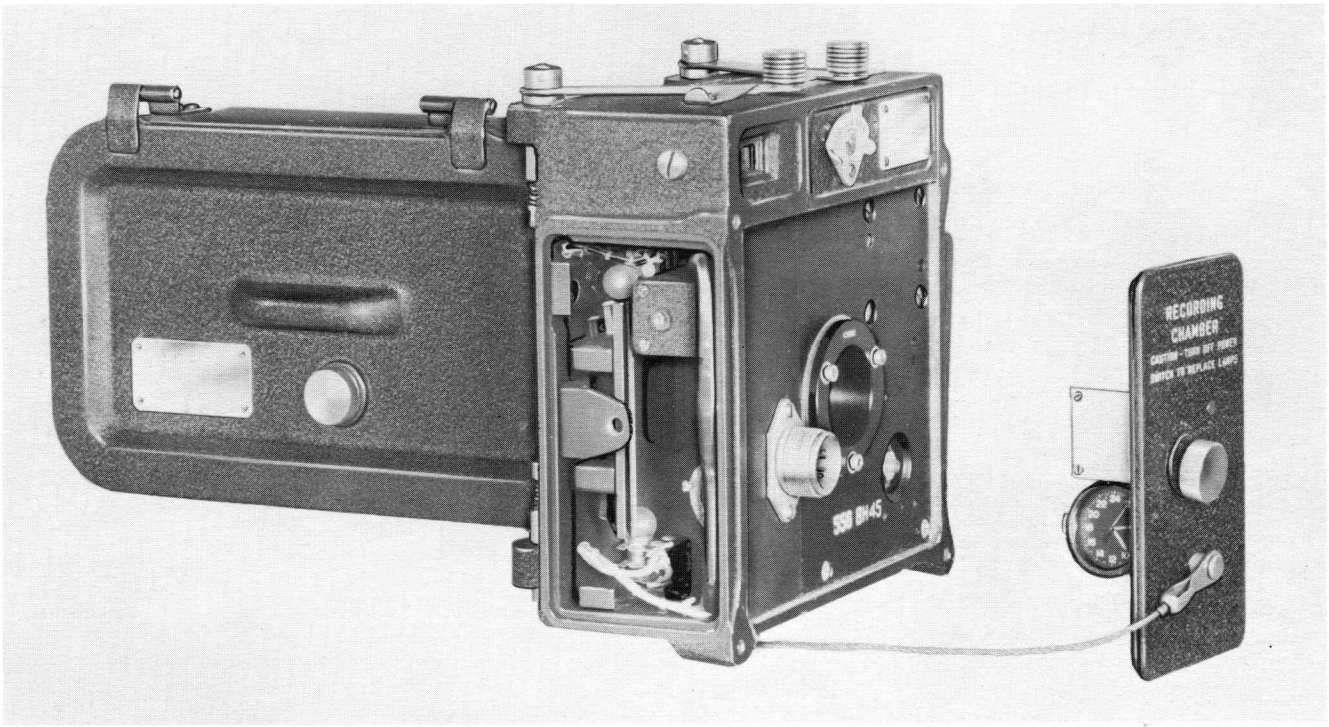


Figure 1–21. SD Camera (Unmounted), KD-16A

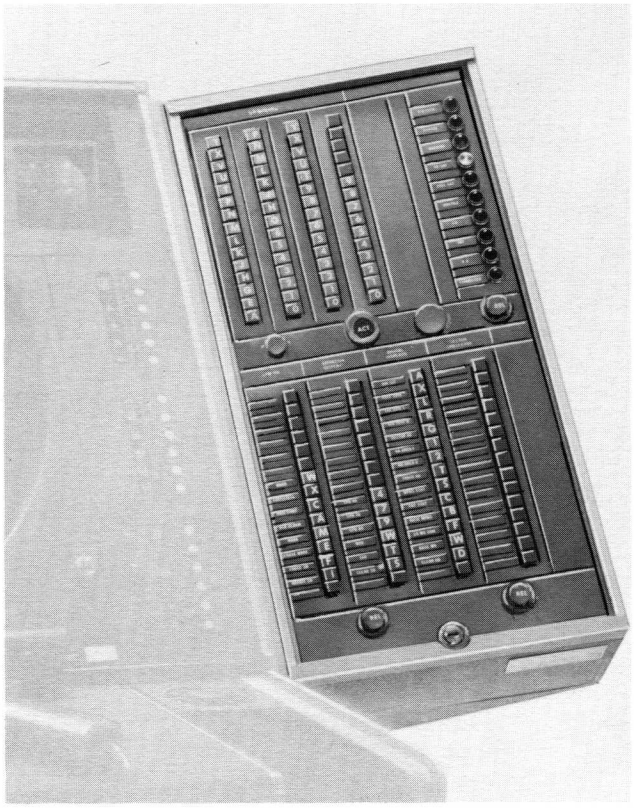


Figure 1–22. Typical Side Wing, C-1825/FSQ

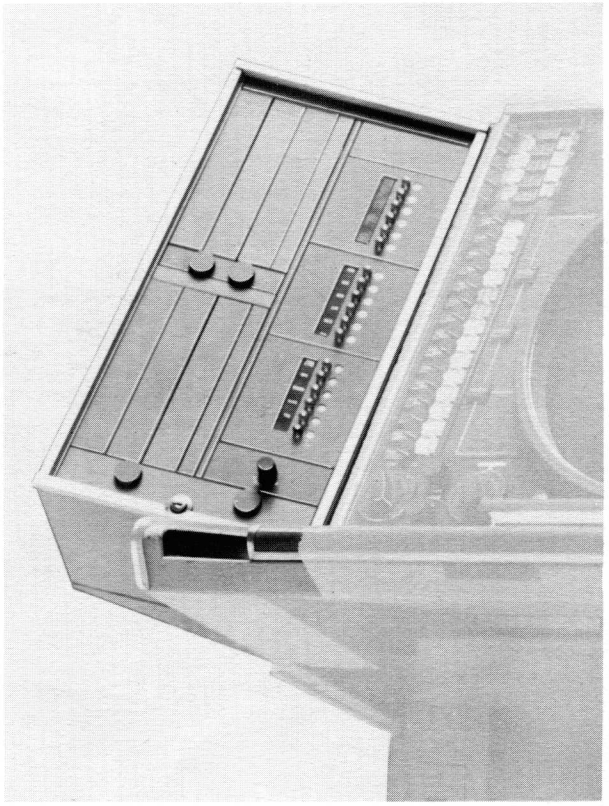


Figure 1–23. Special Side Wing, C-2020/FSQ

CHAPTER 2
DISPLAY SYSTEM IN THE AN/FSQ-7 AND AN/FSQ-8

SECTION 1
SCOPE

1.1 RELATION OF DISPLAY SYSTEM TO AN/FSQ-7 AND AN/FSQ-8

The AN/FSQ-7 and -8 Combat Direction Center accepts air defense intelligence from radar outposts and other data reception points and evaluates and summarizes this intelligence for presentation by the Display System.

The prime purpose of air defense is to provide flight-path instructions for interceptor air weapons. To accomplish this effectively, a clear picture of the compiled information must be available to personnel who are to act upon this data in directing retaliatory air defense.

The Display System provides this picture. It presents relevant air surveillance intelligence on the viewing screens of specially constructed CRT's in the form of bright or dimly illuminated symbols and characters. The directing staff may act on this information in various ways. It may, in fact, communicate with the same Central Computer System that processed and evaluated the information to be displayed. For example, an operator may feed back additional data in reply to a request from the computer device or he may ask the device a question. Similarly, he may instruct it to relay a message to some other operator. The latter statement stresses the fact that, aside from telephoning, the only way an operator can exchange data with another operator is by asking the Central Computer System to display an appropriate message on the viewing screen on the other operating position.

The major paths of communication flow through the Display System are shown in figure 1–24. Information is presented to the operating staff by three prime means:

a. Through audible alarms and warning lights (to alert operators to the presence of new information or to a rapidly developing or alarming situation)

b. Through digital displays (a display of detailed tabular information)

c. Through situation displays (a plan-position type of presentation of the current air situation)

The operating staff can communicate with the world outside the site by means of wire and radiotelephone circuits. The staff can also transmit information back to the computer by means of manual intervention switches and light guns. The switches are used to set up coded messages for delivery to the Central Computer System. The light gun enables an operator to aim the gun at a part of the display pertinent to the action and, in effect, say to the computer, "this is the message you are to act on." In addition, one function is carried out automatically by the area discriminator; it picks up information directly from one of the cathode-ray display tubes and asks the Central Computer System to take action without personal intervention from the operating staff.

The types of displays are described below. The warning lights and audible alarms are discussed in Section 2 of Chapter 8, Part 5.

1.2 TYPES OF DISPLAYS

As indicated in figure 1–24 two types of displays are made available to operating personnel; i.e., digital displays and situation displays. Each display has a CRT unique to its system. The plan-position maps of the air situation or portions of it are presented on special 19-inch tubes. Information pertaining to radar tracks, flight plans, geographical boundaries and locations, weapons sites, etc., are presented on the viewing screen of this tube in the form of letters, numbers, special symbols, and vectors. The letters and numbers are used to assemble short encoded messages that are posted adjacent to certain points and targets, giving identification and other descriptive data. One type of display position is shown in figure 1–25.

Information on selected tracks that is too detailed for the situation display is presented on a digital display which appears as a 2-column table of letters, numerals, and symbols on the face of a special 5-inch CRT.

The Display System makes use of two general types of console: SD and auxiliary. The SD console (fig. 1–20) contains both an SD and a DD tube. The auxiliary console (fig. 1–16) may be equipped with a DD CRT. The installation of the DD CRT in an auxiliary

console is optional, depending on the console type. An SD CRT is never employed in an auxiliary console. The two types of displays are not common to each other (with the exception of some power supplies) and are independently controlled.

Display controls enable operating personnel to select or reject certain types and categories of information according to the tactical requirements assigned to each operating position. This is in addition to the common facilities for expansion, offcentering, brightness, and communication controls.

A periodic display summarizing the tactical air situation is generated by the computer, presented on an SD CRT, specifically adapted for fine definition, photographed, and then projected on a large area screen at the Command Post. This display, brought up to date every 30 seconds, provides command personnel with a big-board summary of the current air situation (see the frontispiece).

1.2.1 Digital Display Elements

The digital display presents supplementary data that is either too slow-changing or does not warrant displaying its graphic information on a situation display. The data appears as a tabular array of characters only (letters, numerals, and special symbols, but no vectors) on the viewing screen of the 5-inch CRT. (See fig. 1–26.) These characters appear in two columns of rows with five characters to the row. There may be a possible maximum of 16 rows in a column.

A digital display changes only when the Central Computer System orders a new digital display. In the absence of instructions from the computer, the display will remain indefinitely. The computer may order a new display as a result of new information from routine data processing or as a result of instructions given to the computer by an operator.

Digital display information prepared by the Central Computer System is in binary digital form. This data form is not readily interpreted until it is changed to analog voltages (the CRT is in itself an analog device). The analog voltages, in turn, are changed to the visual display that is presented to the operator on the viewing screen of the DD CRT.

1.2.2 Situation Display Elements

The SD CRT viewing screen shows an ever changing plan-position graphic display of the changing air situation, with correct geographical relations between fixed points and moving targets. Additional descriptive data in the form of vectors and characters (letters, numerals, and special symbols) is posted adjacent to particular points and targets. The assemblage of this information on the viewing screen resembles a message pattern similar to the one shown in figure 1–27. This figure is not intended to represent an actual air situation;

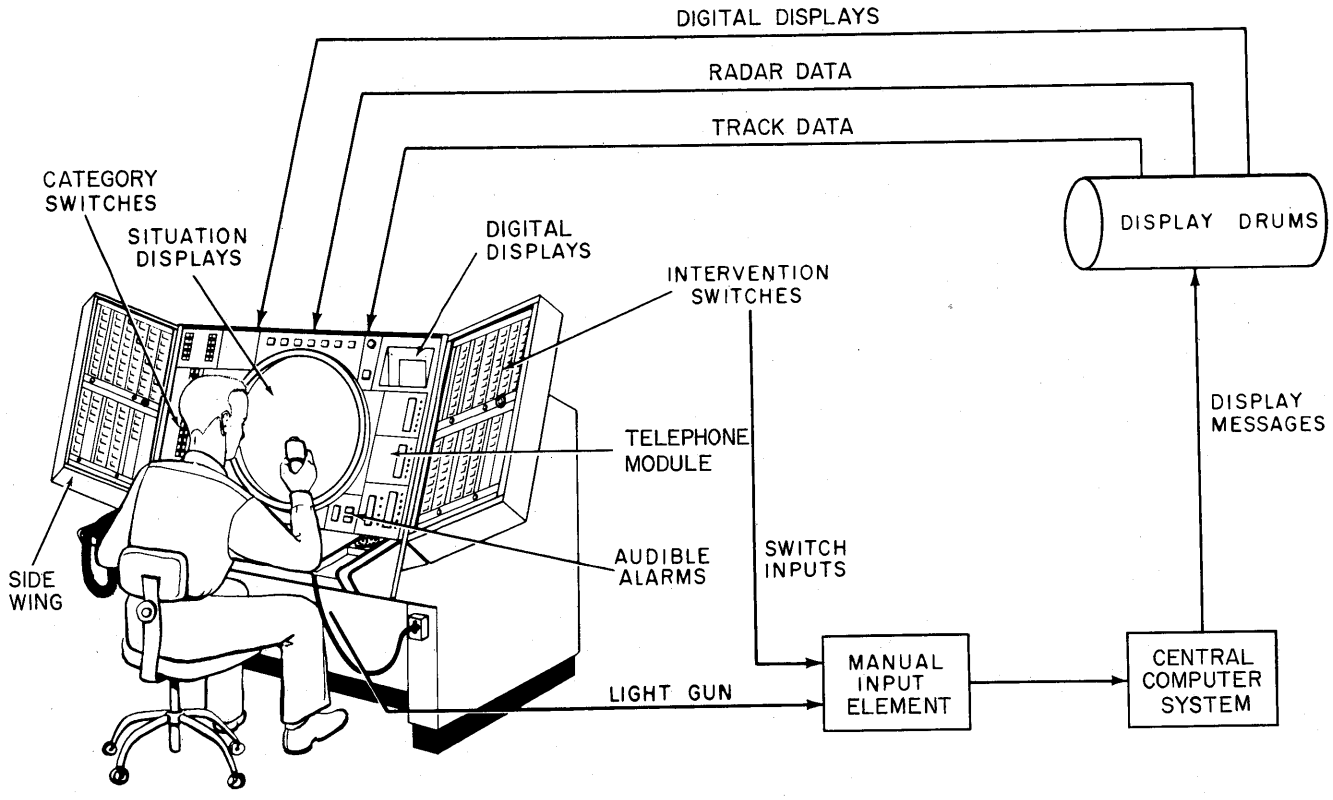


Figure 1–24. Communication Flow between Operating Personnel and Automatic Equipment

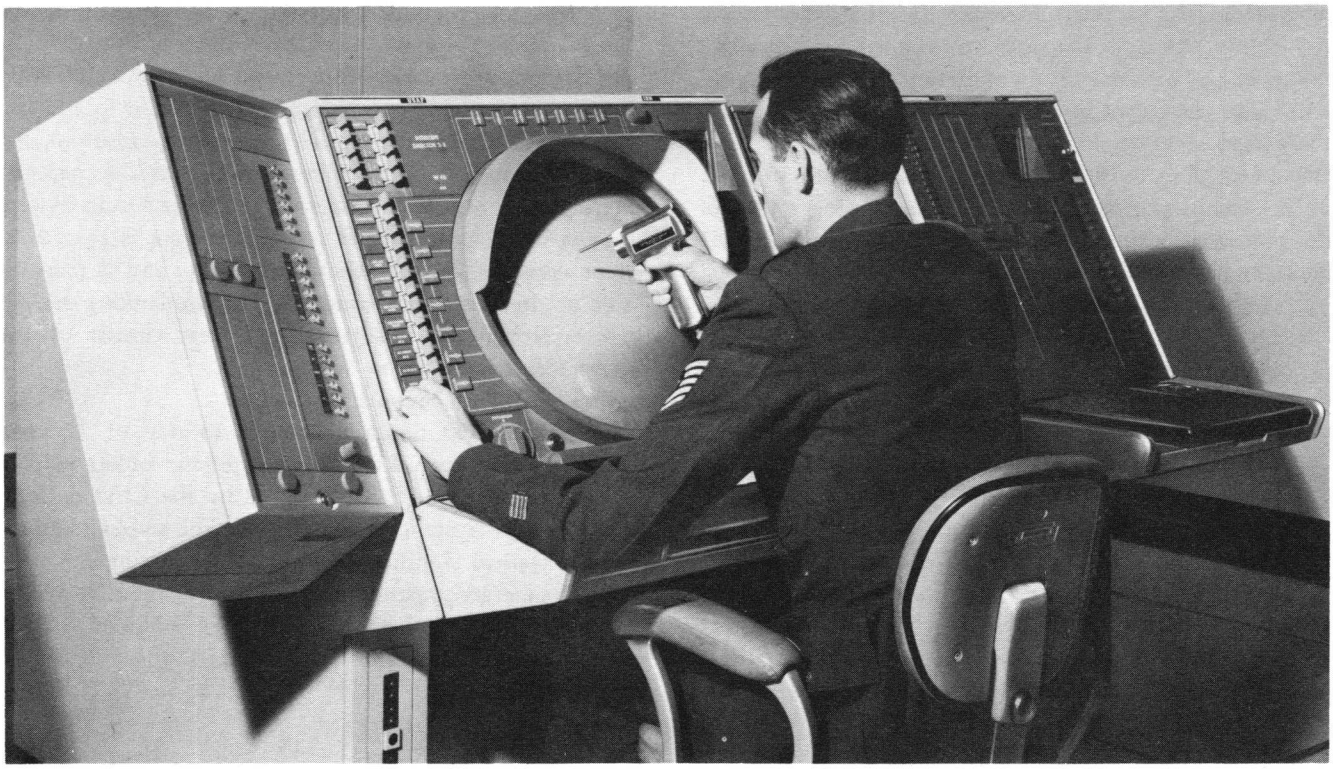


Figure 1–25. One Type of Operating Position

however, it does give a sampling of the tactical and geographical air situations that can appear. (The details of each type are explained in Ch. 1 of Part 4.)

A message may consist of a single symbol or a group of symbols relating to one point or target. For instance, one type (shown at right center of fig. 1–27) includes, for the target, a point designating the location, a vector describing the direction and speed, a group of characters specifying target identification, height and track number, and other information the Central Computer System has processed. Situation Display messages are rewritten on the viewing screen of the SD CRT every 2.62 seconds. If the underlying information has not changed or has been deleted, the message is repeated in the same location. However, if the information has changed, the next message is corrected and, if necessary, moved to a new location. In this manner, operating personnel are constantly aware of the existing tactical air situation.

1.2.2.1 The SD Message

The message on the viewing screen of an SD CRT and its methods of generation are explained in detail in Part 4. The CRT itself is covered in Part 2. However, it will be helpful to understand, in its broader aspects, how an SD message is made to appear on the viewing screen.

The tube differs from that of the customary CRT in many respects. It can also do many things the conventional tube is incapable of performing:

a. It generates complete alpha-numeric characters (as in typewriting) and character symbols (as shown in fig. 1–27).

b. It draws vector-line representations.

c. It assembles these characters, symbols, and vectors into a message pattern.

d. It positions the entire message pattern on discrete portions of the viewing screen.

The characters are formed by an extrusion (or stenciling) process; i.e., a diffuse beam of electrons is extruded through a selected aperture in the character-forming matrix. The character selection process uses a set of electrostatic deflection plates to direct the electron beam through the selected aperture.

Vector generation is accomplished by focusing the emitted beam and passing it through a nonrestricting aperture in the matrix to form a point. This point (or spot) is then swept as required by a second set of electrostatic deflection plates.

An electromagnetic deflection yoke is used to position the message on the viewing screen on the face of the tube.

Although messages on the SD CRT may appear to be presented simultaneously, each message is actually

generated and positioned one character at a time. Figure 4–7 shows the time sequence for the type of message shown at right center of the situation display of figure 1–27 and described in a preceding paragraph. Each phase represents an interval of approximately 50 μsec. The message in its entirety takes less than 1,050 μsec. On the completion of this message, succeeding messages are presented sequentially until all the available SD messages have appeared.

The message described, a TD tabular track message, is but one SD type. Others are TD tabular information, TD vector, and RD messages. (See figs. 4–3, 4–4, and 4–12.) There are up to 1,536 TD and 16,384 RD messages per SD cycle.

1.2.2.2 Individual Console Routing

Except for the signals which unblank (cause to conduct) the writing beams, all the signals required for the display of SD messages are available at each and all of the many SD CRT's. However, the full display of all SD messages would needlessly crowd the screens with messages that serve no immediate tactical purpose. The Combat Direction Center has been arranged in its distribution so that each console is forced to display only those classes or parts of messages determined by the tactical problem assigned to the operator. In addition, the operator can select for display certain classes or parts of messages. Thus, the information from the Drum System that is being processed at any given time is forced on some consoles, can be selected on some, and is unavailable at the remaining consoles. The unblanking signals which accomplish this routing process consist of the three following types:

a. Category Signals

Each TD message belongs to one of 32 categories; each RD message, to one of eight. The classification is determined by the Central Computer System on the basis of the source, subject, tactical significance, etc., of the message. A message accompanied by a category signal is available for display at the consoles assigned to that category, usually as a selected display.

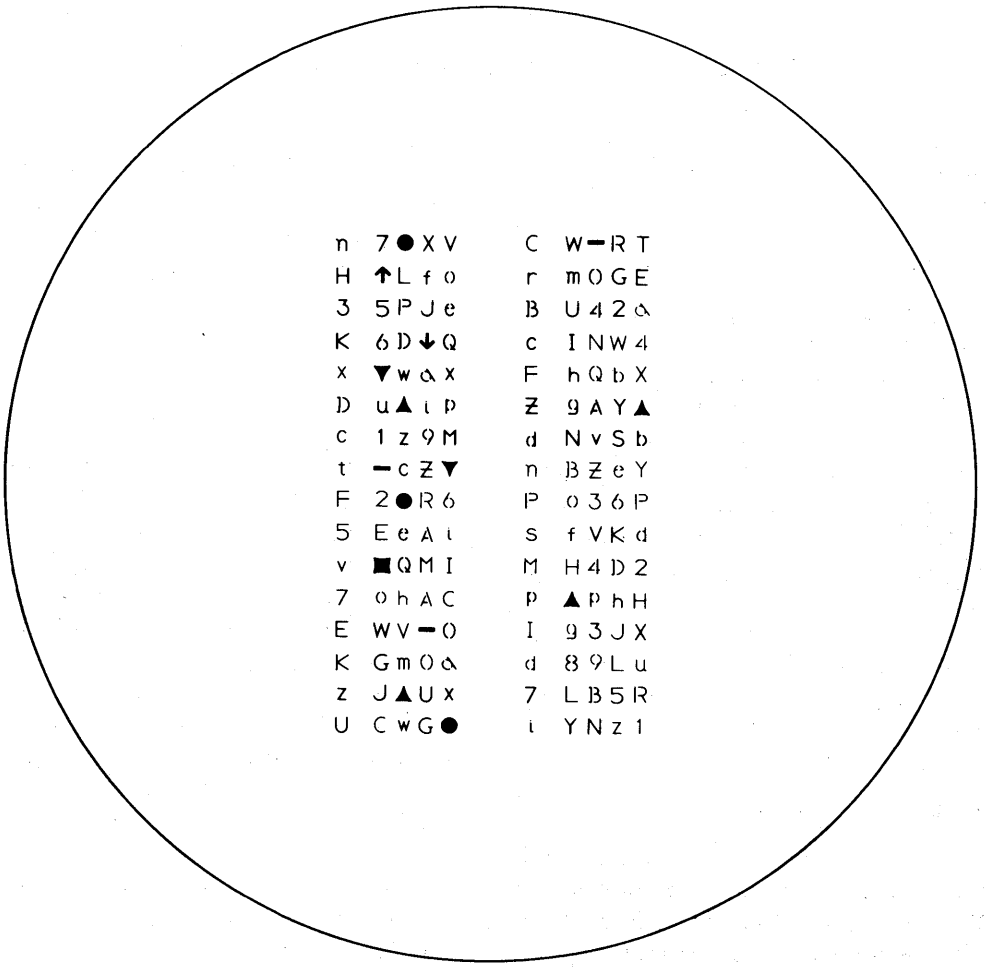
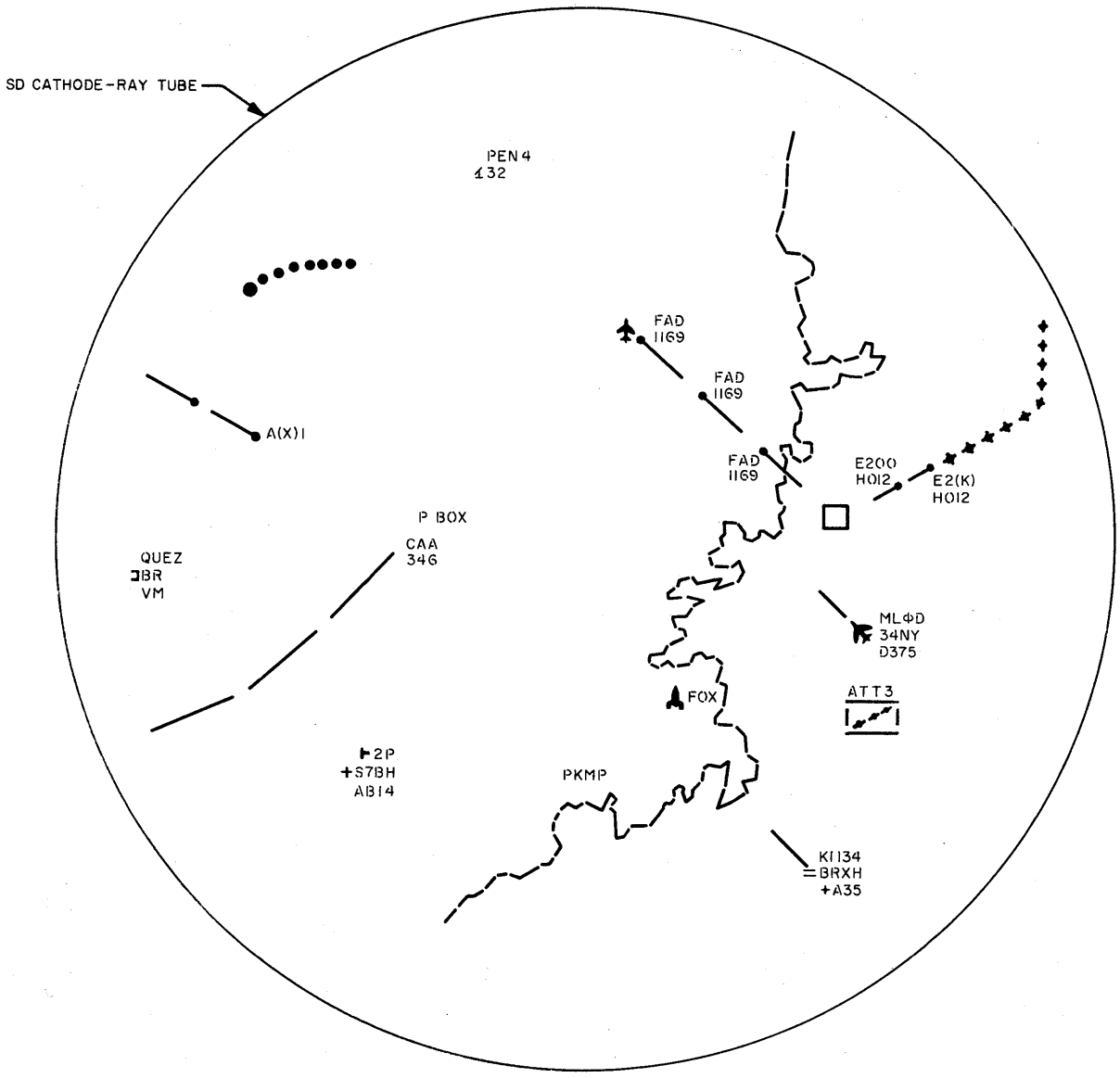


Figure 1–26. Digital Display Message



NOTE:
SYMBOLS IN RD MESSAGES WHICH APPEAR LARGER THAN NORMAL ARE SHOWN IN THIS MANNER TO INDICATE THAT THEY ARE DISPLAYED BRIGHTLY.

Figure 1–27. Representative Situation Display

b. Display Assignment Bit (DAB) Signals

Each console is assigned a DAB number (from 1 to 90). A TD message containing a DAB corresponding to a particular number is available for display at the console or consoles assigned to that number, usually as a forced display.

c. Feature Signals

Specific parts of TD messages (e.g., the target location point) are accompanied by a signal which allows a specific part of the message to be selected for display or which forces its display (bypass features).

At a console, the routing signals which permit display are applied to selection switches at the operator's console. The routing signals for a forced display bypass these switches. Messages displayed at a console can be intensified brightly or dimly.

1.3 DISPLAY INFORMATION SIGNALS

All of the information presented on either of the two displays is prepared by the Central Computer System. In the case of the situation displays (and, in a comparable manner, for the digital displays), the latest target information in the form of SD messages must first be calculated and composed by the Central Computer System in accordance with one or more of its automatic

data-processing programs. The information is brought up to date in each operating cycle to fulfill the high-speed requirements of the equipment. The information is generated at irregular intervals, the frequency of which is determined by the volume of traffic in new radar target messages. On the other hand, the information must be made available immediately, continuously, and at a slow enough rate to match the functional needs of the Display System.

To meet the requirements, three magnetic drums in the Drum System are employed as a time-buffer storage medium. The Central Computer System writes the information on the drums and the Display System reads it off independently. Thus, the Drum System acts as a secondary source of information that makes the time cycles of the Display System substantially independent of the time cycles of the Central Computer System. While this is not true in all cases, it is helpful to regard the display drums as an independent source of signals, making it unnecessary to go beyond the Drum System to understand how the Display System functions. The display drums generate the basic timing pulses that con-

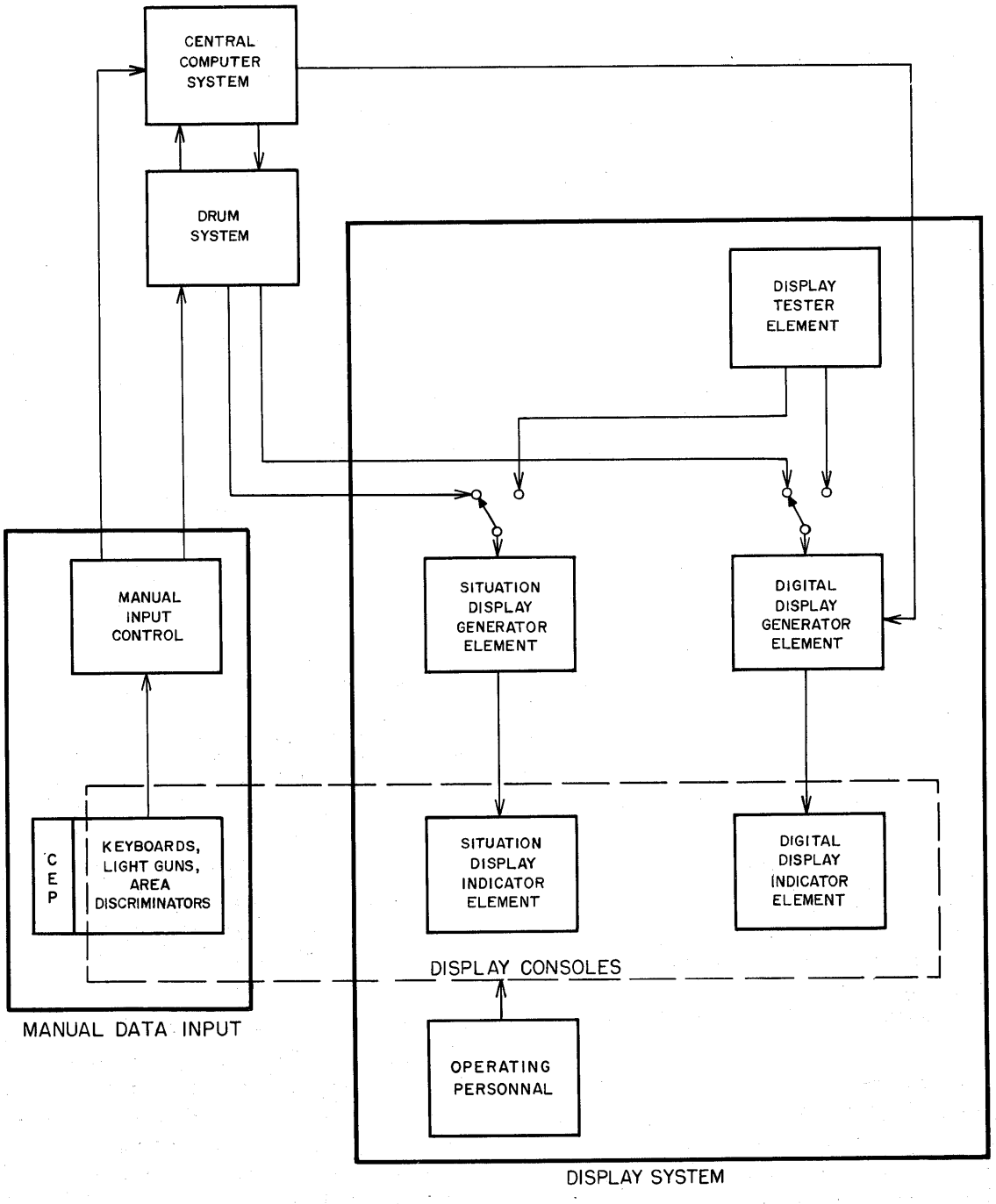


Figure 1–28. Display System and Interrelated Systems, Simplified Flow Diagram

trol the generation and ultimate presentation of the situation and digital displays. (An exception are the signals which initiate DD cycles; they are programmed by the Central Computer System.)

1.4 LOGICAL ORGANIZATION OF DISPLAY SYSTEM

The Display System deals separately with the preparation of situation digital displays. An SD generator and the SD indicator element (SDIE) receive and display situation information (see fig. 1–28). Similarly, a DD generator and the DD indicator element (DDIE) process information. Each generator element receives from the Drum System both timing signals and the binary-form information that has been prepared for display by the Central Computer System. The generator elements perform the necessary storage, timing, and signal conversion functions by means of which the signals for operating the cathode-ray display tubes are rearranged in time and otherwise processed. The SDIE contains all the CRT's and associated circuits that display situation data. Each SD CRT and its associated circuits is called an SD indicator section (SDIS). In the same way, the DDIE consists of all the DD indicator sections (DDIS), including those mounted in SD consoles.

The Display System contains other elements; namely, the signal distribution element and signal data patching panels. These additional elements distribute to the individual displays in the indicator elements the signals developed in the generator element. The display tester element (DTE) consists of circuits for making tests on the Display System independently of the Drum and Central Computer systems. Another unit is the SD camera element (SDCE) which contains a camera that makes photographic records of situation displays for review and training purposes. The Display System also contains the photographic recorder-reproducer element (PRRE), the Command Post (CP) console, and the communication equipment of telephone and maintenance lines.

It has been established that the Display System is logically related to the Drum and Central Computer Systems. In the same manner, the Display System is related to the Manual Input and Warning Light Systems. The SD and auxiliary consoles contain circuits which function logically as part of the Manual Input and Warning Light Systems.

1.5 EQUIPMENT RELIABILITY

Fundamental to air-defense equipment is that it have a 24-hour-a-day operating availability. It was with this goal in mind that the AN/FSQ-7 and -8 were engineered for the utmost reliability consistent with economic operation. Reliability in this context can be defined as maximum operating periods with minimum down-time. Some of the more important considerations in achieving this reliability include the duplex installation of critical equipment, marginal checking to anticipate component degeneration before failure occurs, carefully selected and engineered components to increase reliability, and programming for error detection.

Duplexing, the method we are concerned with at this time, involves the duplication of critical equipment. This method makes it possible for one unit (called the standby) to be maintained or serviced while a duplicate unit is in operation. Should a failure occur in the duplicate (active) unit, the standby takes over the operation, with the malfunctioning unit now designated as, and, in effect, being, the standby.

The next paragraph deals specifically with those units in the Display System that are affected.

1.6 DUPLEX OPERATION IN DISPLAY SYSTEM

As explained in the previous paragraph, duplexing dictates that all units whose failure would halt the operation of the Combat Direction Central be duplex (duplicated). The duplex units are organized in two groups (machines or units); one of these is active and the other is standby (ready to take over, but being used for maintenance).

The following units are duplex in the Display System:

a. The SDGE.

b. The DDGE.

c. The DTE. This equipment is duplex to assure continuous maintenance.

d. The signal distribution element.

e. The SDCE.

f. A few portions of the SDIE and DDIE (e.g., the camera console, the signal data patching panel, the SDIS and DDIS in maintenance consoles, etc.). This equipment is duplex to assure continuous operation and maintenance.

The following units are simplex (not duplicated):

a. The SDIE. The breakdown of any one SDIE does not affect the electrical operation of the other units. The tactical assignment of the console can be assumed by other consoles. In some cases, another console can be adapted to perform the functions of the inoperative console. (Exceptions are indicated in item f, above.)

b. The DDIE.

c. The Command Post element. The five desks are not duplexed. The flexibility of the DDIS in the Command Post (two or more per desk) can compensate for the breakdown of any one of the 11 DDIS's in the Command Post.

d. The PRRE. Although there are two PRR units in the system, they are not hooked in as duplexed, even though one unit can be considered to be on a standby basis.

The power supplies for all simplex equipment are duplicated (systems C and D). One system supplies all active simplex units; the other supplies all standby simplex units.

Each console can be operated at any time from active signal sources and, therefore, active power sources. If required for maintenance purposes, any one console can be switched individually to standby signals and therefore, to standby power.

1.7 CHECKING THE DISPLAY SYSTEM

The Display System, in the same manner as the computer and the rest of the equipment, is checked by means of a marginal checking (MC) method. Marginal checking is the method used for the detection of imminent circuit failure.

With the system using fool-proof devices, rigidly tested components, and with the best available circuit techniques, it is still necessary to devise methods of preventive maintenance, since even the best components deteriorate. Maintenance on the Display System, and on the AN/FSQ-7 and -8 generally, has two separate but related objectives: marginal checking and maintenance programming. The easiest approach to marginal checking, it was learned, was to vary one of the supply voltages servicing the unit, which subsequently varies the corresponding voltage on all like circuits at the same time. Use of a variable power supply for marginal checking applies the same voltage excursion to all circuit groups which use that voltage.

Failure of a circuit is defined in terms of its 1,0 signal characteristics. The circuits must be so engineered that one or more of their associated supply (power) voltages may be varied in prescribed quantities without causing circuit failure when the component parts are within their specified tolerances. Characteristic variations of components, outside of accepted tolerances, must be reflected in a reduction of the voltage variation sufficient to cause failure. The voltage variation which causes circuit failure is called the circuit margin. Marginal checking in itself is not a complete maintenance method unless used in conjunction with programs for the particular circuits to which the MC voltage excursion is applied.

The MC system varies the MC voltages, one at a time, over large sections of the system. For a more detailed reliability check, a breakdown of these large circuit groups is made on the expected circuit margins. A further breakdown is provided for the purpose of fault-isolation when MC procedures indicate a performance failure or drastic characteristic change in a circuit or component.

SECTION 2
FUNCTIONAL OPERATION OF DISPLAY SYSTEM

2.1 DISPLAY SYSTEM FUNCTION

The purpose of the Display System is to present air-defense information in a manner that will facilitate rapid tactical interpretation and use of the data. This data, such as radar returns and weapons and weather status, is presented on the viewing screens of the CRT's constructed for that purpose. Since the information from the Central Computer System is in binary units, the primary function of the Display System is to present such information in a form that can easily be interpreted by operating personnel. It does this by changing the binary information to visual intelligence that consists of letters, numerals, vectors, and special symbols in a prearranged format on the viewing screens of the CRT's.

That part of the Direction Central or Control Central which presents or displays this essential information is designated the Display System. As such, the system contains the equipment necessary to generate the display and the consoles which contain the CRT's that picture this defense data. These consoles also contain accessory equipment which is described in Part 5.

Figure 1–29 illustrates signal flow to the Display System. References to the display generator and display consoles are found in Parts 3 and 4.

2.2 DISPLAY SYSTEM BREAKDOWN

The Display System can logically be grouped into four divisions or parts: the DD elements, the SD elements, the associated equipment, and the MDI as shown in figure 1–28.

Each group of elements processes a different type of information. The associated equipment contains major components that are associated or connected with the SD and DD elements.

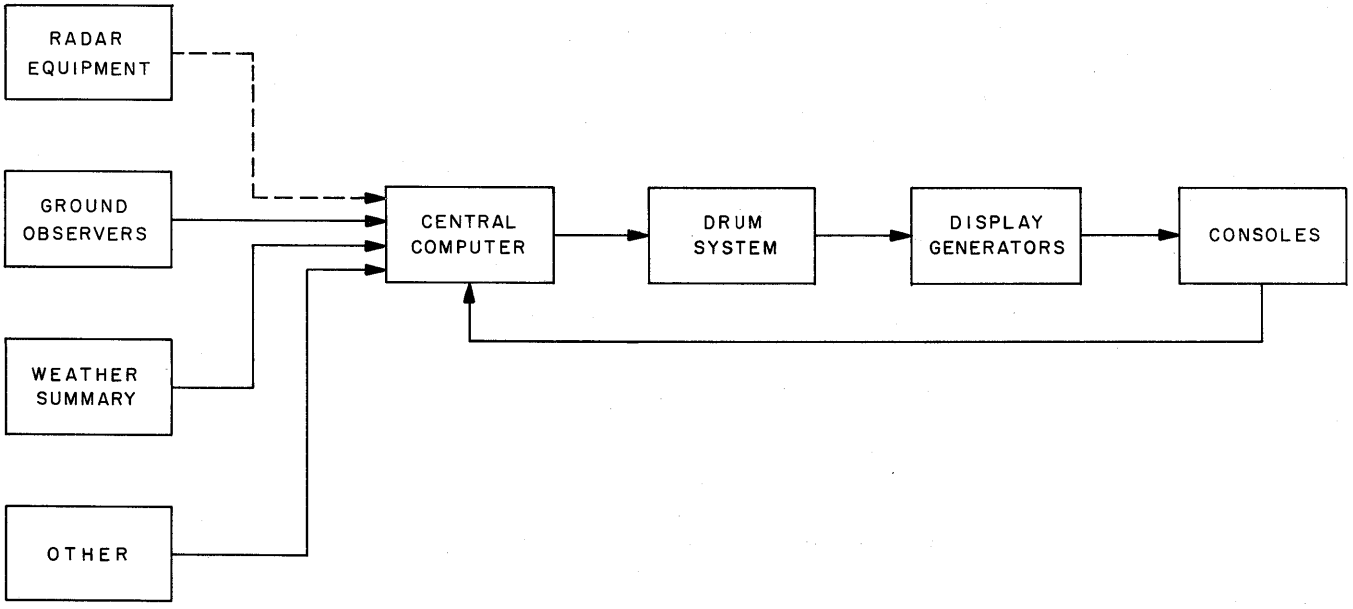


Figure 1–29. Signal Flow to Display System

SECTION 3
OVERALL FUNCTION OF DD ELEMENTS

3.1 SCOPE

The digital display presents information on selected tracks that is too detailed as well as too slow-changing to appear on the SD CRT. This information, shown on the DD CRT viewing screen, is in the form of a 2-column table of letters, numerals, and symbols. The display remains unchanged until such time as the Central Computer System establishes and directs a new display. In the absence of instructions from the computer, in ordering a new display, the existing display will remain on the viewing screen indefinitely. Figure 1–30 is a functional block diagram of the DD system.

3.2 DIGITAL DISPLAY INSTRUCTIONS

Digital instructions presented to operating personnel on DD CRT's are prepared in the Central Computer System for delivery to the DD elements through the DD drum field of the MIXD drum. This drum acts as a time buffer between the rapid operation of the Central Computer System and the relatively slow DD elements.

Two types of signals are delivered from the Drum System to the DD elements. One type is the information signal that contains the digital information needed to select the proper characters shown on the 5-inch DD CRT. The second type is the control signal. This signal controls the positioning of the characters that are selected for the tabular format and synchronizes the DD elements operation with the drum operation.

3.3 DIGITAL DISPLAY ELEMENTS

The DD elements contain the DDGE and the DDIE. The DDGE is a duplex element that receives digital signals from the Drum System and converts them to analog voltages and gates which are fed to the DDIE. The DDIE is an element that is made up of all the DDIS's. Each DDIS is simplex equipment that contains the 5-inch CRT and its associated circuits. The DDIS receives the analog voltages and gates from the DDGE and then writes the tabular arrangement of characters on the face of the CRT.

There are two types of signal flow from the DDGE

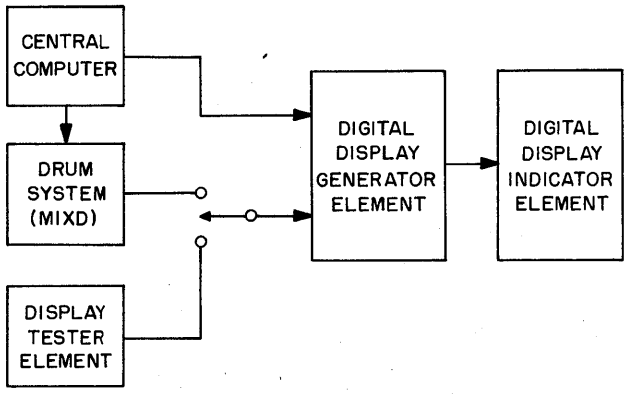


Figure 1–30. Digital Display, Functional Block Diagram

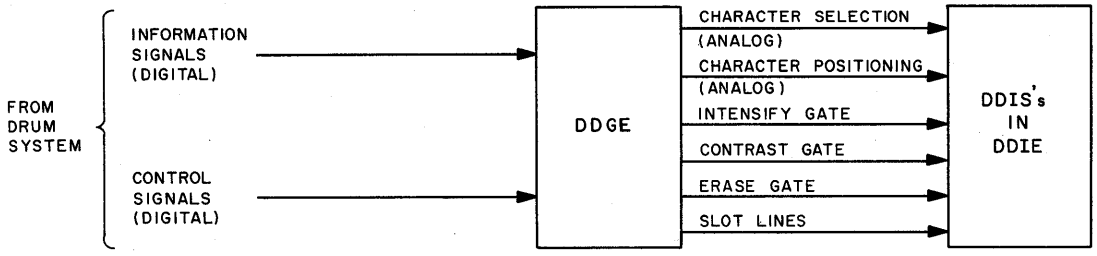


Figure 1–31. Digital Display Elements, Signal Flow

to the DDIE. One is used to select and position the characters that appear in the displayed outputs. The other signal flow consists of the gating signals used to control the operation of the DDIE. Figure 1–31 is a DD elements block diagram showing the DDGE, DDIE, and the signal flow.

3.4 TIMING OF A DD CYCLE

The sequence of operations in the DD cycle is controlled by signals and gates generated in the DD timing and control section. The duration of the initial period varies between approximately 205 and 225 ms. The actual time would depend on where the drum is, rotationally, when the Central Computer sends an initiate-DD signal to the generator element. Figure 3–16 shows the overall timing of a DD cycle.

Although the signals for the DDGE and the SDGE are separately generated, all signals are run to a common point and terminated for distribution by the distribution element.

SECTION 4
OVERALL FUNCTION OF SD ELEMENTS

4.1 SCOPE

The SD elements of the Display System present a rapidly changing picture of the present and past air-defense tactical situation. The presentation is made in the form of plan-position indicating maps of the air situation or selected portions of it. Information pertaining to radar tracks, flight plans, geographical boundaries and locations, weapons, sites, etc., appear on the viewing screen of special CRT's as letters, numbers, vectors, and special symbols. The letters and numerals are used to assemble short, encoded messages that are posted adjacent to particular points and targets in the form of vectors, giving identification, location, and other description information.

4.2 SD INFORMATION

The SD element receives its information in the form of binary words from the Central Computer System through the necessary buffer devices, specifically, the TD and RD drums. The drums act as a time buffer between the rapid operation of the Central Computer System and the relatively slow SD elements.

The TD (track data) drum is capable of storing 1,536 8-word messages whereas the RD (radar data) drum can store 18,432 messages at any given time. Both of these drums are read by the SDGE approximately every 2.6 seconds. (The TD drum is read repeatedly at a rate of 1.6 seconds by the SDGE in the AN/FSQ-8, since there is no RD drum in that system.)

4.3 SD MESSAGE PRESENTATION

The types of messages displayed by the SD element are separated into three main categories in the AN/FSQ-7, or two main types in the AN/FSQ-8. The first type, radar messages,* is used to indicate present and past radar returns. The second, vector messages, is used to indicate flight plans, geographical boundaries, and other instances where lines and/or designs are to be shown. The third type is the tabular message. This type of information presentation is used to indicate cities, aircraft, airports, and missile or antiaircraft bases.

* *Not applicable to AN/FSQ-8; part of AN/FSQ-7 only.*

4.4 SITUATION DISPLAY ELEMENTS

The SD elements contain the SDGE and the SDIE. The SDGE is a duplex element that receives digital information signals from the Drum System and converts them into voltages that can be used by the SDIE. This element also receives the timing and control signals from the Drum System.

The SDIE contains all the SDIS's. These sections all operate alike and are placed at various SD consoles for the assigned operators. Each SDIS is simplex equipment that contains the SD CRT and its associated circuits. They receive the signals from the SDGE and change them into the visual information displayed on the viewing screen.

There are two types of signal flow between the SDGE and the SDIE. One is used to select the characters in the pattern, place the characters in the proper pattern, and then orient the pattern in the correct position on the viewing screen. The second type is used to control the operation in the SDIE. Figure 1–32 is a block diagram of the SD elements showing the SDGE, the SDIE, and the accompanying signal flow.

4.5 SD SIGNAL FLOW AND TIMING

Figure 1–33 is a functional block diagram of the SD element, showing information flow from the drums to the SDIE. The drums send to the generator element the binary information to be displayed, along with timing pulses, WOW pulses, and other control signals.

The generator converts these binary signals into the necessary digital and analog voltages. These volt-

ages are distributed to the various consoles by the cables and distribution boxes of the distribution element. Although all signals are wired through all boxes, only those signals necessary to a specific console's tactical assignment are wired in to that console.

The signals thus generated by the generator elements are classified as variable signals and common signals. Common signals are applied to all consoles, whereas variable signals are only applied to selected consoles.

4.6 SDIS SELECTION

Each of the SD messages sent to the SD elements from the Central Computer is given a category (CAT) and a display assignment bit (DAB). These CAT's and DAB's select which SDIS's in the SD consoles will be intensified for the particular message. If each SDIS were intensified for each message, the resulting display would be an intermingling of many messages that would be hopelessly unintelligible. This chaotic condition would result because all messages are sent to each SDIS; therefore, some such device as that described above would be necessary to assure discrete displays on the viewing screen.

4.6.1 Message Category

Each SD message is assigned one of 32 CAT numbers on the basis of source, subject, tactical significance, etc. This assignment is made by the Central Computer when the message is made up, and the CAT is sent with the message to the SD elements.

Certain SDIS's only display messages with a particular CAT. When a message with the proper CAT arrives at the console, the SD CRT is intensified (unblanked), thus activating the phosphors so that the data can be viewed. When the message arrives at a console

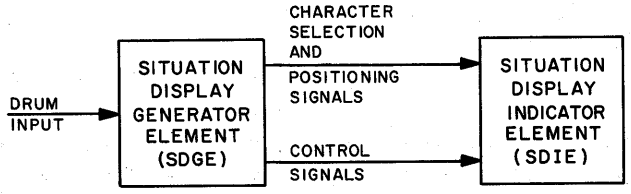
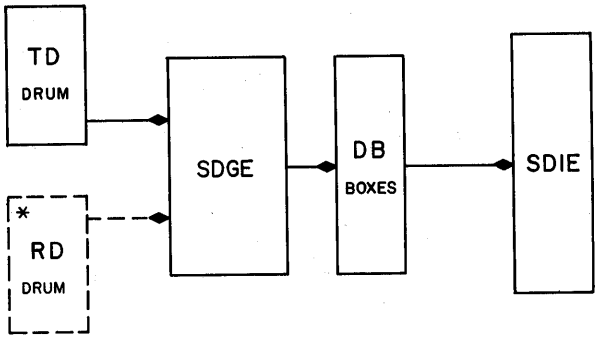


Figure 1–32. SD Elements, Block Diagram



* NOT APPLICABLE TO AN/FSQ-8, PART OF AN/FSQ-7 ONLY.

Figure 1–33. SD Element, Functional Block Diagram

with the improper CAT (and should not be displayed), the CRT is not intensified (blanked). When a console displays a message with a particular CAT, the console is said to be assigned that CAT.

4.6.2 Display Assignment Bit

The Central Computer assigns at least one of 90 DAB's to each message. The DAB accompanies the message throughout the system.

Certain SD consoles only display messages with a particular DAB. Like the CAT assignment, the messages are intensified at the console only when a message is received with the proper DAB.

4.6.3 Optional Message Display

Any message that has the same CAT or DAB as that assigned to an SDIS may be displayed. However because some of the CAT and DAB assignments are sent through switches at the SDIS, and if the switch for a particular CAT or DAB is moved to the off position, the messages given this CAT or DAB are not displayed. This is done to give the operator partial control over the messages that are displayed. On the other hand, some messages do not have the CAT or DAB sent through a switch, so that the operator has no control over their display. These are called forced messages and will always be displayed at the SDIS regardless of what action the operator takes at the controls.

SECTION 5
OVERALL FUNCTION OF ASSOCIATED EQUIPMENT

5.1 SCOPE

The DDIS and SDIS may display the results of the computer, but it would be of little value unless operating personnel could act upon it. The controls, indicators, and communicating devices that are part of the operating consoles provide the means of operator response. Other devices contributing to an even greater degree of display evaluation and flexibility are the PRRE, the SD camera, and the SD, auxiliary, and Command Post consoles. Supporting Components associated with the Display System, and so designated in Part 5, consist of the audible alarms, the communication equipment, manual inputs, the unit status switch, and warning lights. The DTE, another part of the associated equipment, is used to check the operation of the Display System by sending simulated drum signals into the system.

5.2 SUPPORTING COMPONENTS

The SD, auxiliary, and Command Post consoles, and the PRRE have some controls, indicators, and operating devices in common. Such devices as audible alarms, communication equipment, MI devices, unit status switches, and warning lights are located at more than one operating position. The operation of each is basically the same, no matter where it may be located in the system.

5.2.1 Audible Alarms and Warning Lights

By means of the Warning Light System, the Central Computer can light lamps or sound audible alarms at the display consoles to alert operators to a situation requiring their attention. With certain exceptions, there are provisions for as many as 20 warning lights at an auxiliary display console or 10 in each input data-selection control panel at an SD console.

5.2.2 SD Console

Most of the SD CRT's in the Display System are in SD consoles. (An illustration of a console is shown in fig. 1–20.) The consoles are simplex with the exception of certain consoles (as SEE ALLS and others) associated with maintenance monitoring. Most of the SD consoles include a DD CRT. In addition, the SD consoles are equipped with accessory devices, such as light guns and warning lights which are logically parts of the MI element and Warning Light System, respectively.

5.2.3 Auxiliary Console

The majority of the DD CRT's in the Display System are also in SD consoles, as stated previously. Most of the remaining DD CRT's are used in auxiliary consoles. There are four types of auxiliary consoles: A, B, C, and D. The A and B models do not contain CRT's. Models C and D do have DD CRT's. The location of an auxiliary console is determined by the work that has been assigned to it. Figure 1–16 illustrates the type C auxiliary console.

5.2.4 Command Post Console

The Command Post console provides operating positions for command personnel and staff. These personnel are continuously informed of the tactical situation in the air-defense sector by digital displays, warning lights, and a situation display that is projected on a large screen above and behind the Command Post console. As the information is evaluated, the personnel direct certain courses of action, using manual inputs located at the console.

5.2.5 Communication Equipment

Telephone and radio communication equipment is provided at many SD and AUX consoles as a part of the tactical telephone system. This enables operators to communicate with other defense personnel inside or outside the Direction Center or Control Center. The telephone-control panels are of plug-in modular construction to facilitate maintenance. The basic telephone/radio module consists of 18-circuit pushbuttons and 4 special function keys. When additional facilities are required, a special telephone module containing additional 6-circuit pushbuttons is employed. In addition to the telephone panels, consoles equipped for telephone or radio service are provided with an illuminated telephone dial and an operator's headset or handset.

5.2.6 Photographic Recorder-Reproducer Element

The PRRE receives the output of the SDGE, converts it for presentation on the 7-inch SD CRT, photographs the viewing screen, and then projects the processed image on a large beaded screen mounted ahead of the Command Post console.

The PRRE consists primarily of two sections, the SD section and the photographic recorder-reproducer. The SD section functions in much the same manner as

the SDIS. The photographic recorder-reproducer is essentially a camera which automatically records the situation display on 35-mm film, develops, reverses the image, and automatically projects this image for evaluation by command personnel. A new display is recorded and reproduced every 30 seconds.

5.2.7 Situation Display Camera Element

The SDCE makes a permanent 35-mm photographic record of situation displays. The records are used for tactical analysis and as training aids. Since records of both standby and active displays are required, the SDCE is duplexed. One of the two cameras, depending on which machine is on active status, records active displays; the other records standby displays.

The recording device itself is a semiautomatic (still picture) camera mounted over the face plate of the SD CRT installed in a modified SD console. This console is called the SD camera console because it has been specially modified to accommodate the camera and the control circuits.

In addition to making permanent records of displays generated by the active computer, the SDCE records the results of maintenance programs without interrupting the standby computer. Figure 2–5 shows an SD camera console with the camera, mounting frame, and shroud installed.

5.2.8 Display Tester Element

The DTE is employed in testing the digital and situation display generator and indicator elements independently of the Drum System. Figure 1–34 illustrates the interconnections of the elements with the DTE. The DTE has provisions for inserting a test message into the SDGE or DDGE for subsequent display on the SDIE or DDIE.

5.2.9 Distribution Element

The signal distribution element distributes outputs from the SDGE and DDGE to their respective indicators (SDIS and DDIS). In addition to distributing the outputs of the display generators, the signal distribution element also routes the light gun signals and warning light signals. The light gun and warning light signals are associated with the MI element and Warning Light System, respectively.

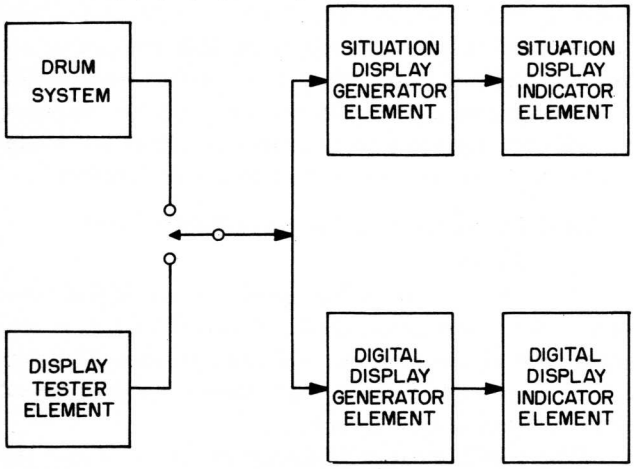


Figure 1–34. Display Tester and Drum System Relationship to Display System

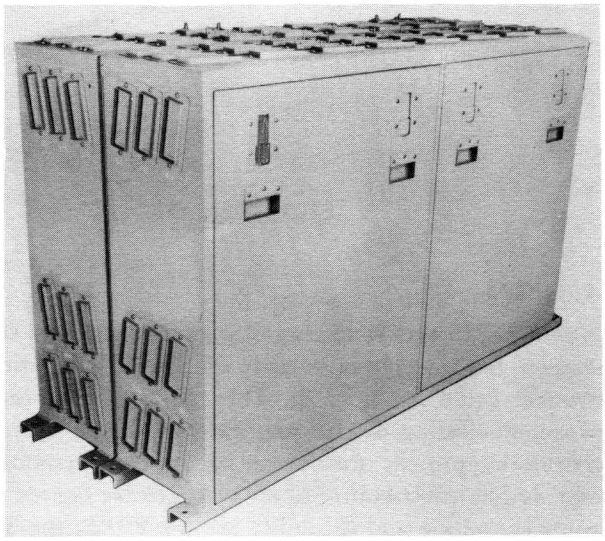


Figure 1–35. Typical Signal Distribution Box

5.2.9.1 Distribution Boxes

The distribution box serves the function of making signals generated by the display generator elements available to all SD, PRRE, and auxiliary consoles located throughout the AN/FSQ-7 and -8 equipment. The boxes have been engineered to minimize the length of cable runs and increase the flexibility of the signal distribution system.

Dimensionally, each distribution box is approximately 10.5 feet long, 1.5 feet wide, and 3 feet high. Two such boxes are secured and installed back-to-back (fig. 1–35). Each box is electrically independent of the other. One section receives and distributes signals from the A display generator elements; the other section receives and distributes signals from the B display generator elements.

5.2.9.2 Signal Data Patching Panel

The signal data patching panel enables the operator of an SD console to patch route or transfer signals, category assignment bits, and category lines from the SDGE so that they are available to each of the associated consoles. The patching panel is located next to the (SEE ALL) SD console, one for each computer. Figure 5–60 illustrates a patch panel and associated SD console.

The patching panels and associated consoles are basically maintenance devices and can be used to monitor the displays that should be present on any SD or DD CRT. The signal data patching panels are part of the signal distribution element.

SECTION 6
OVERALL FUNCTION OF MANUAL DATA INPUTS

6.1 SCOPE

The designation SAGE indicates that the design conception of the overall system was not to be fully automatic. Although the Combat Direction Central performs most of its functional operations automatically, the need for human intervention in tactical air-defense problems made necessary the MDI element.

The situation and digital display indicator elements of the Display System present information to the operating personnel. The MDI element makes it possible for personnel to act upon this information and make known to the Central Computer, by means of the direct entry or drum entry, the resulting decisions. The MDI also provides the machine with data which does not lend itself to automatic introduction. The MDI does this by devices such as CEP's, area discriminators, light guns, and the keyboard control panels on the auxiliary consoles and SD console side wings. Figure 1–36 is a simplified flow diagram of the manual data input.

6.2 MDI DEVICES

The information channeled to the MDI is the output of one or more of the devices listed in 6.1 and briefly described below.

6.2.1 Keyboard Control Panel

The keyboard control panel is made up of modules containing the neon warning lights, audible alarms, and MI information switches. The warning lights and audible alarms are visual and aural alerting devices. The MI switches arrange binary messages that are conveyed to the matrix in the MI element. There are various types of MI information modules containing from 5 to 15 pushbuttons.

6.2.2 Computer Entry Punch

The CEP is also used to channel information to the MI element. It may be used as a printing card punch and reader or as a prepunched card reader. This intelligence, either punched or read (or both) on modular IBM cards, usually consists of availability lists, weather data, and other, like information.

6.2.3 Light Gun

The data-selecting light gun is a pistol-shaped, trigger-actuated, photoelectric device. (See fig. 1–18.) It is used by the operating personnel to designate a particular target on the display when making a request for additional, specific information. The request is made by placing the protruding plunger of the gun adjacent to and aimed at a bright point of a specified character on the viewing screen of the SD CRT.

The spectral frequency response of the light gun has been limited to the bright blue light emitted from the viewing screen. It is unresponsive to ambient or incidental light.

6.2.4 Area Discriminator

The area discriminator, like the light gun, is a photoelectric transducer that converts blue light into electrical energy and, like the light gun, has an amplifier that shapes and amplifies these voltages for proper computer response. The significant difference between the two is that the light gun is a hand-held mechanism pointed at a discrete target and operated at will. The area discriminator, on the other hand, is an automatic device designed to be responsive to the entire viewing screen area of the SD CRT.

The area discriminator head is a fixed installation secured to the console by rigid elevation brackets (fig. 6–4).

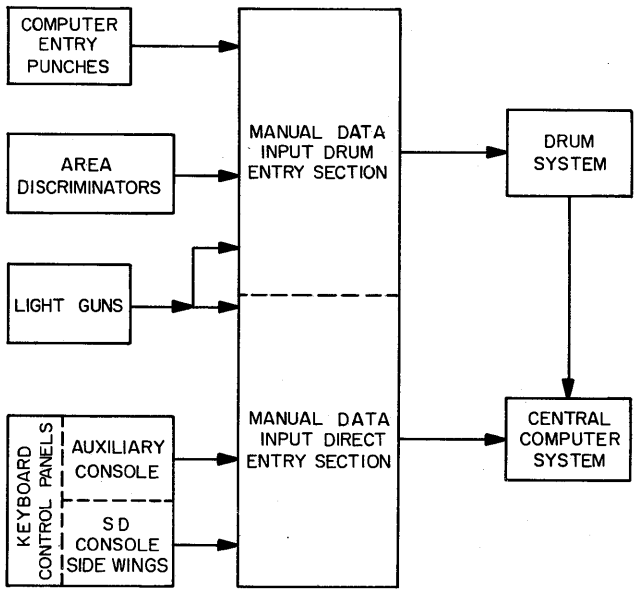


Figure 1–36. Manual Data Input Element, Simplified Flow Diagram

PART 2
CRT's IN DISPLAY SYSTEM

CHAPTER 1
GENERAL THEORY OF CRT's

1.1 INTRODUCTION TO CRT's

Since the end function of the Display System is to present the information output of the Central Computer System, the displaying element or CRT's can be considered the heart of this system.

Four types of CRT's, grouped into two functional classifications, are used for display: three SD CRT's and one DD CRT. The SD CRT's present situation information; the DD CRT presents digital information. The type of information (message) that each CRT can present is given in detail in Parts 3 and 4. Figure 2–1 illustrates the relative configuration of each type of CRT. Figure 2–2, in the form of a simplified flow block diagram, shows the relation of the CRT's to the major elements of the Display System. The display indicator section (DDIS and SDIS) represents, in each block, one of many replica units that are driven collectively, in each group, by a DDGE and SDGE. Comprehensive block diagrams are shown in those sections of this manual which discuss each CRT type in detail.

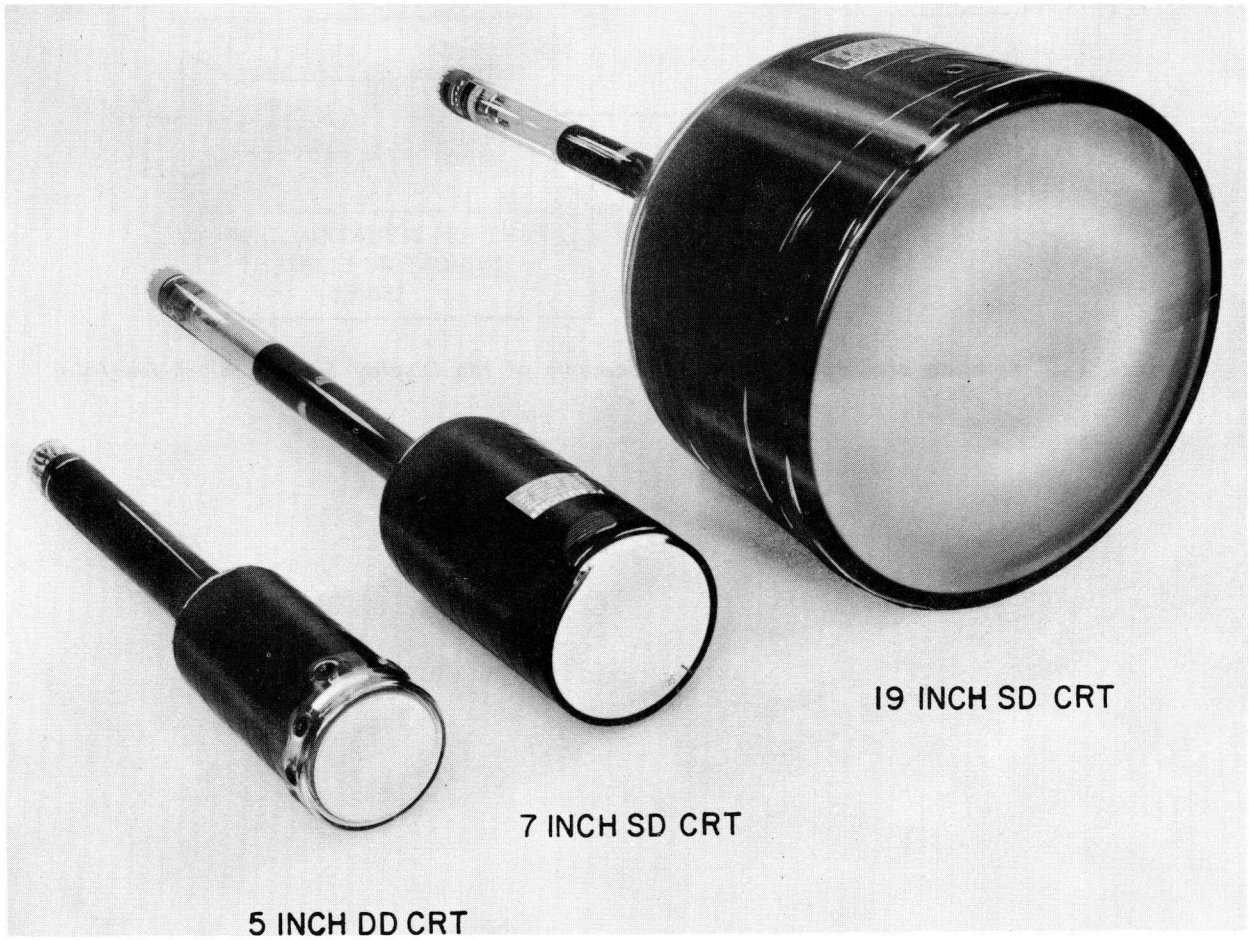


Figure 2–1. CRT Types Used in Display System

1.2 DISPLAY SYSTEM CRT's

The CRT types commonly known and used for oscillographic or picture displays contain four essential parts: an evacuated glass envelope, an electron gun that will generate and shoot a stream of electrons, a means of deflecting the electron stream and a screen which transforms the electrical energy of the electron stream into light. The CRT's used in the Display System operate on the same basic principles; only additional elements have been added to further control and direct the electron stream for character display.

1.2.1 Electron Gun

The electron gun consists of a separately heated cathode that acts as a source of electrons, a control grid that limits the number of electrons traveling toward the screen, a first (or focusing) anode, and a second (or accelerating) anode. Voltages applied to the first and second anodes accelerate the electrons and cause them to be focused into a narrow beam. The cathode, control grid, and first and second anodes physically have their axes coincident with the axis of the tube. Electrons leave the heated cathode in random directions, but most

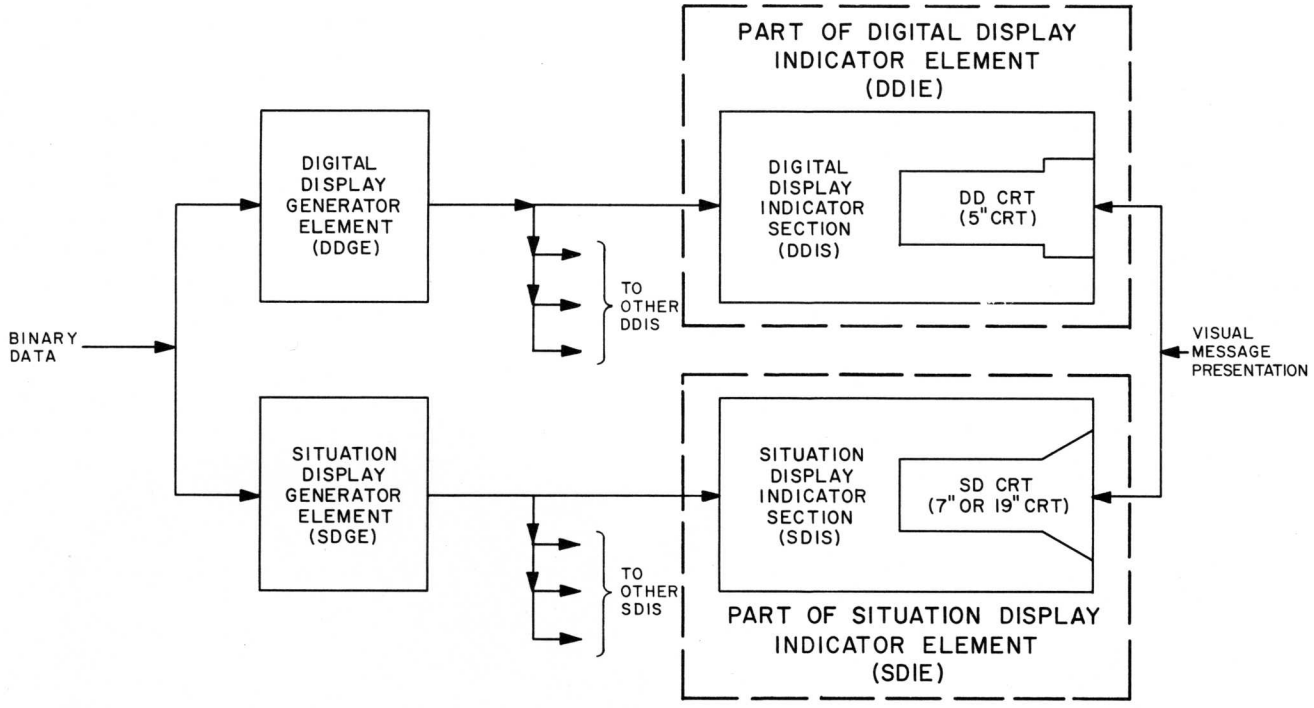


Figure 2–2. Relation of Display Tubes to Elements of the Display System, Block Diagram

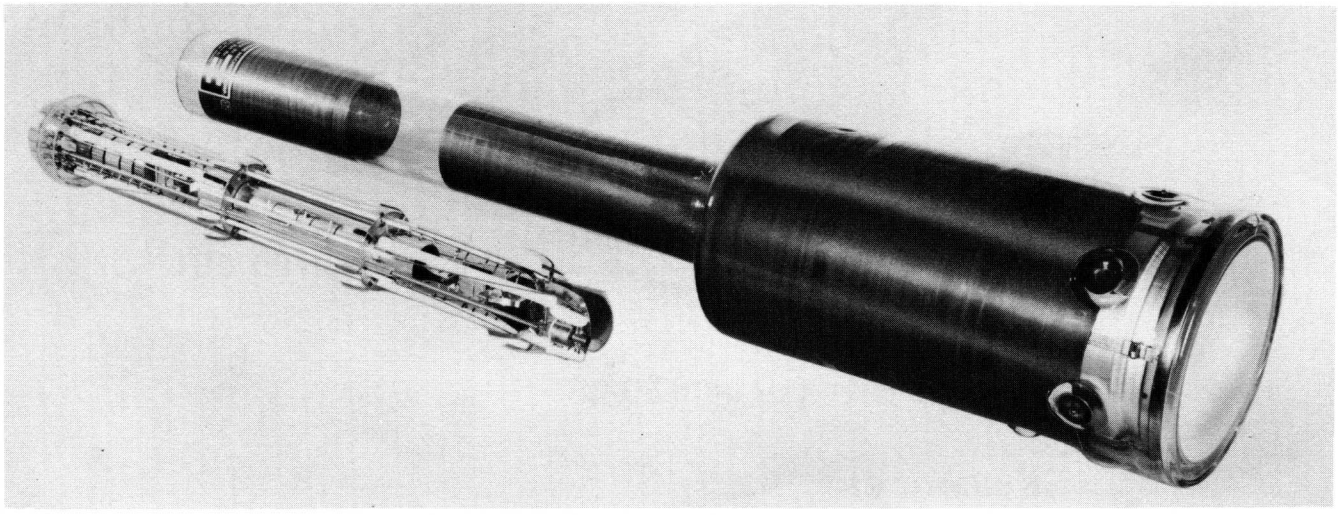


Figure 2–3. Electron Gun Removed from 5-Inch DD CRT

of them are converged toward the axis of the tube by the action of the electric field between the cathode and the control grid. Figure 2–3 shows the electron gun removed from the 5-inch DD CRT.

The electrons pass through a space within the first anode that is almost field-free and enter the space within the first and second anodes, creating an axial field. As the electrons leave this field, their paths become less rapidly convergent. However, they are still headed toward the axis and will meet at a point. If this point is at the screen, it is said to be in focus. The forces producing convergence of the beam depend on the ratio of the voltages applied to the first and second anodes. By adjusting either of these two voltages, the point of convergency may be changed. Focus is usually controlled by adjusting the first-anode voltage.

The beam may be focused on the screen either by an electrostatic field or by a magnetic field. Similarly, the beam may be deflected on the screen either by an electric or a magnetic field.

1.2.2 Screen Phosphors

To convert the energy of the electron beam into visible light, the area where the beam strikes is coated with a phosphor material which emits light when bombarded with electrons of sufficiently high velocities. This phenomenon is called fluorescence. The continuance of light output, for a short time after bombardment has ceased, is called phosphorescence. All fluorescent materials are associated with a characteristic relationship between the intensity of the emitted light and the colors contained in that light. Some emit a green light; others, yellow, blue, orange, etc., depending upon the phosphor or mixture of phosphors used.

All fluorescent materials have some afterglow or phosphorescence, but the duration of the afterglow (or persistence) varies with the material as well as with the energy in the beam.

1.2.3 Persistence of Phosphors

The persistence of the screen is generally designated by a "P number". In applications where a CRT is used for observing periodic phenomena, which occur at a low repetition rate, a screen material on which the image will linger is desirable. Such a tube is described as a "long persistence" tube. Where the image changes rapidly, a "short persistence" tube is employed. If the application is such that a tube display will be photographed, as well as observed directly, a phosphor having a spectral light output in the blue range is used.

Of the Display System CRT's, the 19-inch SD CRT used in the camera console and the 7-inch SD CRT used in the PRR have P11 phosphors. The other 19-inch SD CRT, although identical in every other respect, has a P14 phosphor, and is used in the SD consoles. The 5-inch DD CRT employs a P1 phosphor.

The characteristic features of the fluorescent screens used in the Display System CRT's are:

Phosphor-P1	Produces a brilliant spot having green fluorescence and medium persistence.
Phosphor-P11	Produces a brilliant actinic spot of bluish fluorescence of short persistence. This color is effective for photographic applications because of the sensitivity of the film emulsion to blue light.
Phosphor-P14	A medium-long persistence cascade (2-layer) screen. During excitation by the electron beam, the phosphor exhibits purple fluorescence of short persistence. After excitation, it exhibits an orange phosphorescence which persists a little over a minute.

To maintain uniform screen potential, increase light output, and improve contrast, metal-backed phosphors are used where practicable. It has been established that a major increase in light is obtained if a large fraction of the light from the bombarded side of the screen is reflected through the screen. The lighter elements such as aluminum or beryllium make a suitable reflecting film on the back of a phosphor screen. Aluminum is used almost exclusively because it is more easily adaptable for screen application.

1.2.4 Envelope Coating

Practically all CRT's are coated on the inside of the glass envelope or bulb with a conductive coating. The coating generally used is a trade-named preparation of graphite. The main function of this coating is to attract any secondary electrons emitted by the fluorescent screen. (Different methods of application may be used to achieve specific characteristics, as in the Display System CRT's.) If electrons were allowed to pile up on the screen, it would soon acquire a large negative voltage which would interfere with the normal operation of the CRT. However, when the beam strikes the screen, some of the energy is used to knock off electrons. Such electrons are known as secondary electrons and may be considered to have been emitted from the fluorescent screen. If the number of secondary electrons equals the number that originally strikes the screen, there will be no change in the screen voltage. The tube will thus continue to operate properly.

Another use of graphite coating is to provide shielding for the electron beam. In some CRT's there is no metallic accelerating anode; the dag coating is electrically connected to perform this function in addition to those previously explained.

CHAPTER 2
19-INCH SD CRT's

2.1 GENERAL

The SD CRT is a character-display type of CRT that was specifically designed to display characters in an SD message format. The message so presented is a function of analog voltages since the information represented on the discrete proportionment of the CRT is fundamentally that of an analog device.

The tube primarily contains an electron gun, character selection plates, matrix, convergence coil, character position and compensation plates, and a deflection coil. With the exception of the convergence and deflection coils, the elements are contained within the evacuated tube.

Figure 2–4 shows two distinct structural sizes of SD CRT's. The larger (19-inch) CRT is made in two types for the Display System. One type is installed in the SD console; the other is in the SD camera console. A still picture camera is mounted above the tube in the SD camera console, as illustrated in figure 2–5. Both these tubes are identical physically and electrically; the sole difference is in the screen phosphors. For the SD camera application, the phosphor is of the P11 type; so is the other CRT used for recording purposes, the 7-inch SD CRT. Figure 2–6 is a schematic representation of the 19-inch SD CRT symbol.

In the SD CRT tubes, the electron gun shoots a stream of electrons toward the screen. But this stream is intercepted by various elements that control, direct, and shape the beam to impinge a particular character and/or vector on a desired section of the screen. With the aid of the schematicized view shown in figure 2–6, the path of a hypothetical electron can be followed.

The electron stream from the gun is deflected both vertically and horizontally to direct the beam to the selected character in the matrix. The matrix (fig. 2–7), in the form of a supported metal disk, has 63 characters cut through the metal; the remaining area in the 8 x 8 row format is left untouched as a beam inhibitor for blank space representation. The electron flow directed to the selected character in the disk is formed or extruded through the character matrix in the shape of the character selected. Figure 2–8 is a greatly enlarged section of the character matrix. This extruded or stenciled beam of electrons now is headed toward the character position and compensation plates, but its path is affected by the magnetic field of the convergence coil.

2.1.1 Convergence Coil

The convergence coil is a 3-coil assembly externally mounted around the gun envelope. The entire assembly contains a deflection trim coil, the convergence coil proper, and a selection trim coil.

The effect of the convergence coil assembly on the electron beam is to simultaneously spiral the stenciled beam on its own axis and on the zero axis so that it is displaced by a rotational deflection through 90 degrees. Figure 2–9 shows the effect of the convergence coil on the character-formed electron beam.

2.1.2 Trim Coils

Current through the windings of the selection trim coil sets up a magnetic field which opposes the field of the convergence coil in the area of the selection plates. This neutralizes the convergence coil effect on the selection plates and, with the deflection trim coil, effectively isolates the convergence coil field from affecting the character selection, and character positioning and compensation plates. Similarly, the deflection trim coil individually neutralizes the field effect on the deflection plates and, with the selection trim coil, isolates the other elements from the convergence field effect.

2.1.3 Character Position and Compensation Plates

The beam now reaches the character positioning and compensation plates where the plates compensate for the original deflection imparted to the electron beam and simultaneously reorient the beam by deflection, to position the character properly in the message.

2.1.4 Deflection Coil

The electron beam, now a properly positioned character in a message format, is impinged on the selected portion of the screen by the deflection coil. The deflection coil field determines the area of the viewing screen in which the message is to be displayed. The de-

flection currents energizing the coil are held constant until all the characters in a message have been displayed.

2.1.5 Viewing Screen and Message Format

The electron beam, in striking the solid materials of the phosphors, causes the latter to become luminous in the characteristic shape of the beam. A message similar to the typical display shown in figure 4–1 can appear on the viewing side of the CRT face plate. The details of the formation of such a display is given in Part 4.

The character matrix, of which a single character has been illustrated as an example, has a total of 64 possible selections in a pattern of eight columns and eight rows. (One space in the pattern is left intact to permit empty space-blank presentation in a message format.) These characters are the elements of messages that can be displayed on the face of the SD CRT. Figure 2–8 shows the arrangement of the characters in the matrix. The binary addresses along the vertical and horizontal columns are references that are used and explained fully in Part 4. The selection of a column and row is initiated by three binary digits (3 bits) in each axis. The intersection of the selected column and row is the selected character.

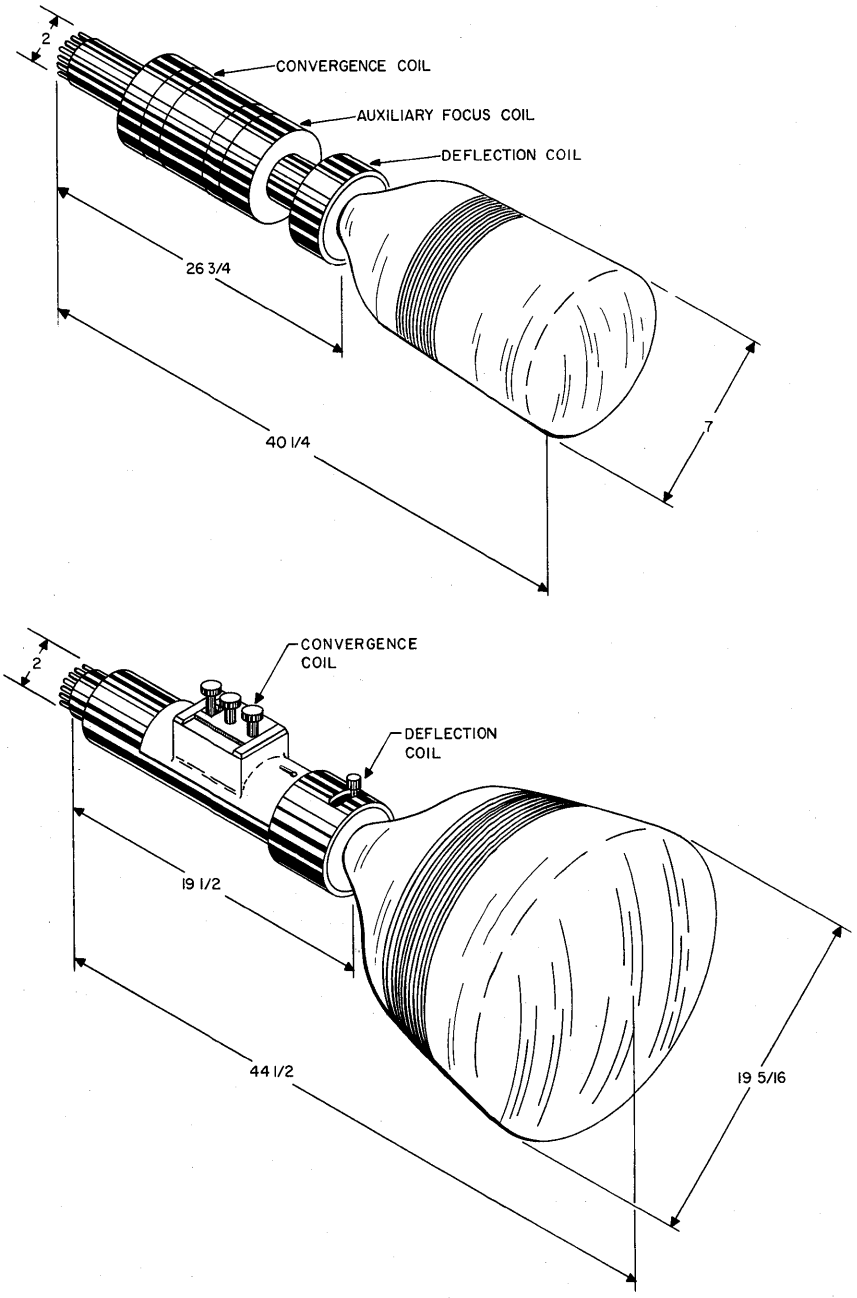


Figure 2–4. SD CRT Dimensions

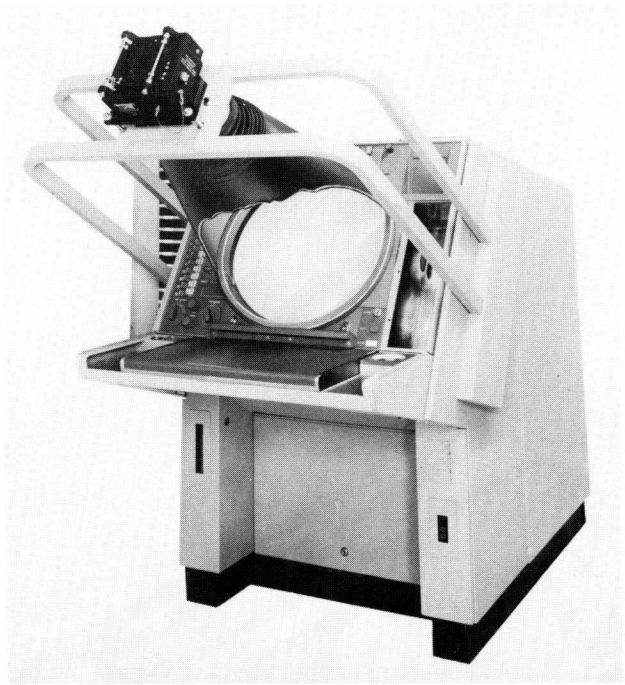


Figure 2–5. 19-Inch SD CRT Employed with Still Picture Camera

2.1.6 Post-Acceleration Coating

The unconventional shape of the SD CRT, for a round-face tube, is due to its unusual requirements. The need to display characters over the entire area of a 19-inch screen, and the necessary high intensity of illumination for their display, made this shape optically desirable. In order to realize the required amount of illumination, it was necessary to increase the energy of the beam. Because of the optical properties of the tube, beam energy had to be obtained by post acceleration. This post-acceleration potential is developed across the helical accelerator (often referred to as a dag coating). The helical accelerator is located in the portion of the envelope between the deflection coil and the screen. The accelerator is a continuous spiral of electrically resistive material, ruled on the inner surface of the bell portion of the envelope extending to nearly 7 inches. The conductive coating bands of the helix are about 0.050 inch in width, spaced 10 turns to the inch. The total length of the helix is approximately 375 feet; it has a total resistance of about 100 megohms.

This type of accelerator has several advantages over types consisting of one or more bands of material, particularly, less distortion of the character-shaped beam.

2.2 SD CRT FUNCTIONAL OPERATION

The display, which appears on the face plate of the SD CRT in the form of a message, may consist of characters and/or vectors. The character is electron-beam-shaped when the beam is intercepted in its path by the selected character cutout in the matrix. The vector, however, is formed by the electron having been first brought to a pinpoint focus and then directed through a non-restricting aperture in the matrix. The beam is then swept in a given direction for a given distance to produce the desired vector display. The type of presentation, as a display, can then be considered to be dependent upon the control and operation of the CRT elements.

Table 2–1 is a list of the controls and functions given each element to produce either a character or a vector in the display. This table, in the form of a summary, is given in greater detail in Part 4. The function of each element for a particular display is also given in detail in Part 4.

In making use of this table, and the subsequent text, it is assumed that the reader is familiar with the special circuits (see Special Circuits Manual, 3-3-0) that

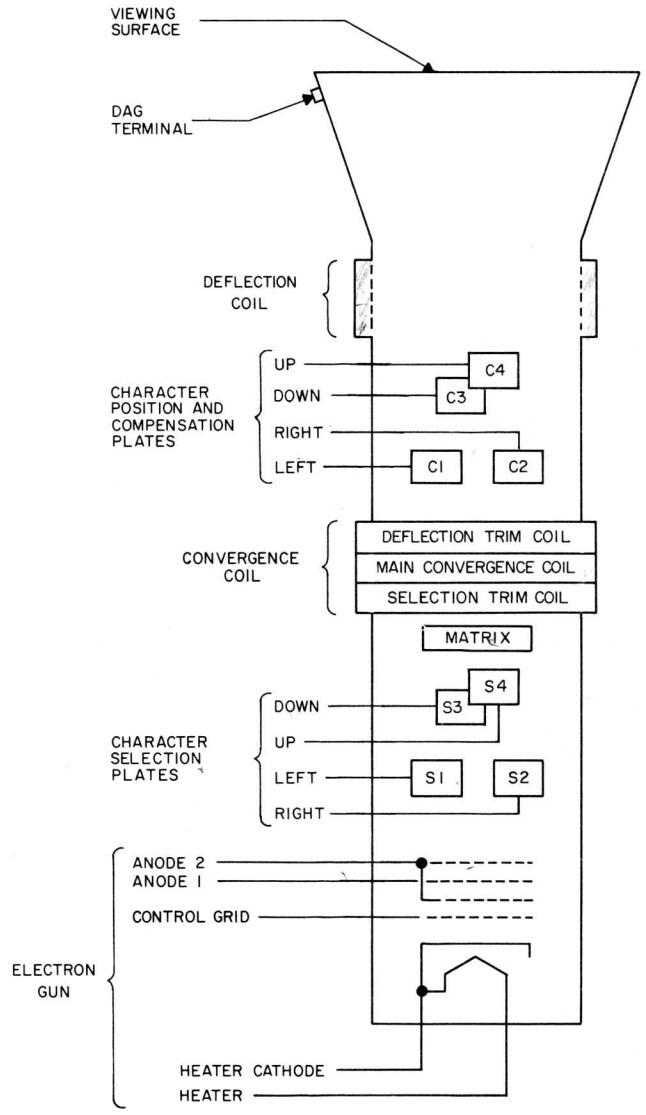


Figure 2–6. 19-inch SD CRT Symbol

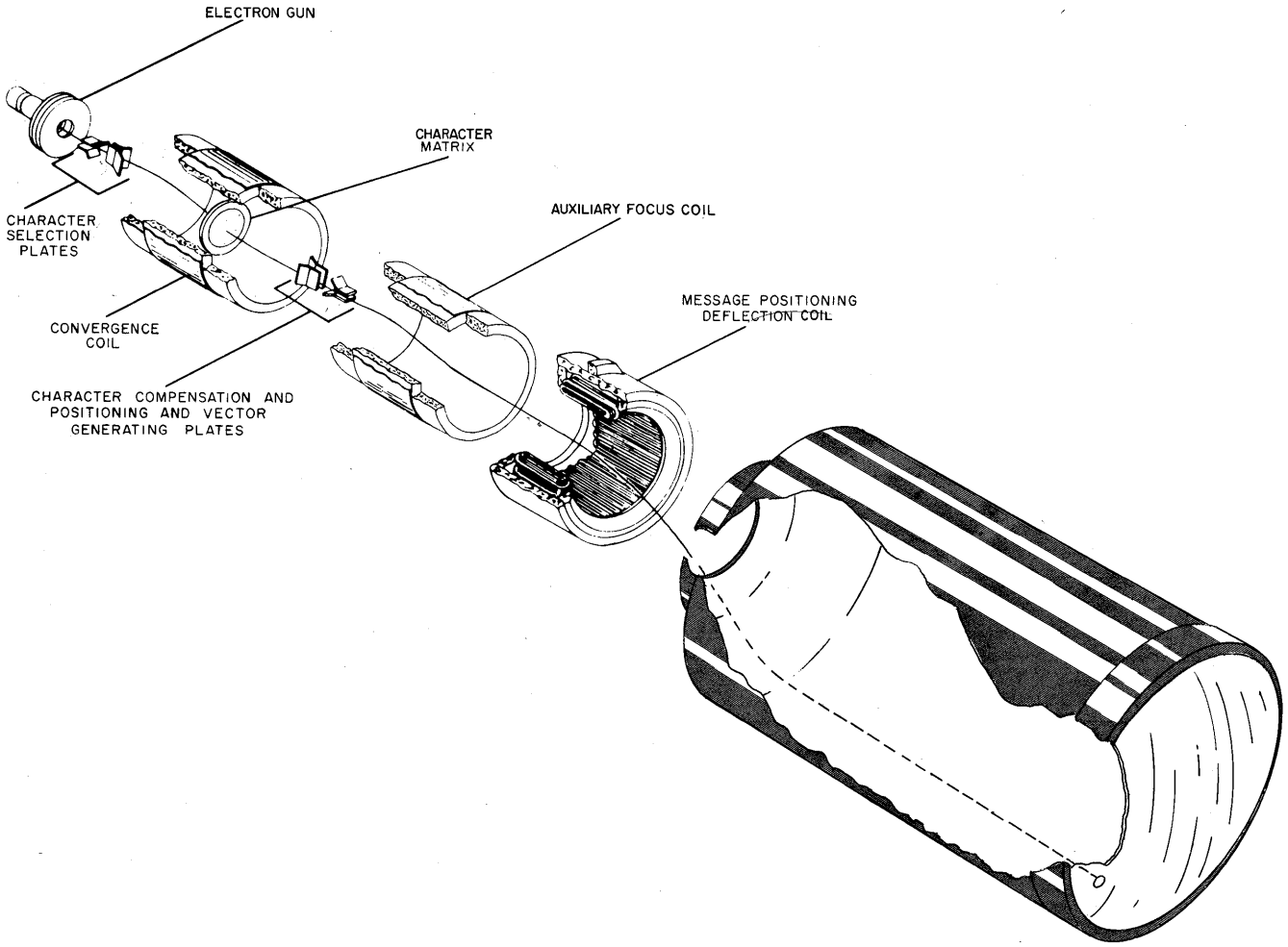


Figure 2–7. 7-Inch SD CRT, Cutaway View

power and control the Display System and therefore the CRT's.

Under functional requirement No. 2, the focus function ensures uniform passage of the electron beam through the matrix and a resultant pinpoint-dot image on the viewing screen of the SD CRT. The defocus function ensures complete inclusion of a selected character within the cross-sectional area of the electron beam. The differences in functional requirement No. 5 are in degree. For character display, the beam can be aimed at any one of 64 positions on the matrix-disk: 63 individual characters or the blank portion of the matrix. For vector display, the beam is directed at one symbol of the matrix. Figure 2–8 shows an illustration of the character-forming matrix with binary addresses. Projecting the X-axis binary address of 111 and the Y-axis binary address of 111, the intersection will be seen as a square cutout in the matrix. Requirement No. 6 is allied to No. 2. If a defocused beam (as it would be for a character) were directed at the vector aperture, the beam would be extruded through in the characteristic form of a square. The image on the screen would therefore be an enlarged filled-in square. The pinpoint-focused beam, because of its much smaller relative area, passes through the same aperture unchanged and is impinged on the screen as an electron spot. In that instant, function No. 10 takes over, and the spot is swept into a

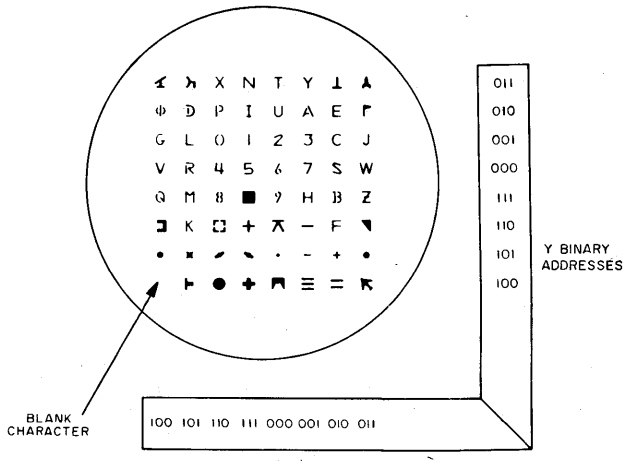


Figure 2–8. SD Matrix Array With Binary Addresses

line for a given direction and distance by the application of a sweep voltage. It is these two elements that determine the generation of either a character or a vector.

2.2.1 Character Display, Detailed Operation

The following text, which parallels the introduction to the basic operation of the CRT's, contains a detailed discussion of the generated electron beam and how it is affected on its way to the screen. Individual functional requirements and associated tube elements are dealt with in the sequence established in table 2–1.

2.2.1.1 Electron Beam Generation

The electron beam is generated by the electron gun element in the SD CRT. Figure 2–10 is a simplified schematic drawing of the electron gun and its relative location within the envelope of the SD CRT. Fig. 2–11 is a block diagram of the control and supply voltages required to generate the electron beam. The detailed discussion of Display System CRT operation is keyed to the referenced illustrations and text and should be consulted for ready analysis.

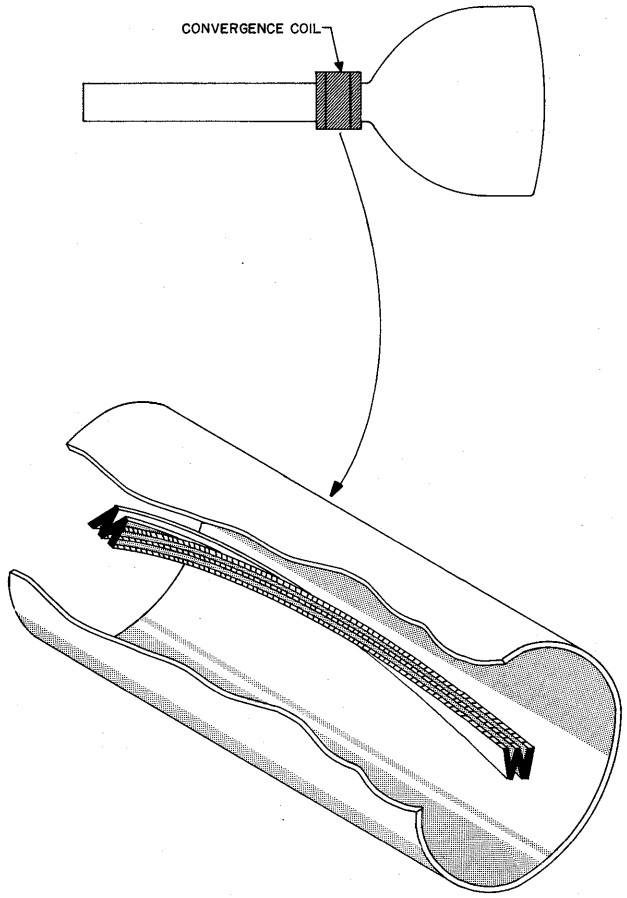


Figure 2–9. Convergent and Rotational Effect of Convergence Coil on Electron Beam

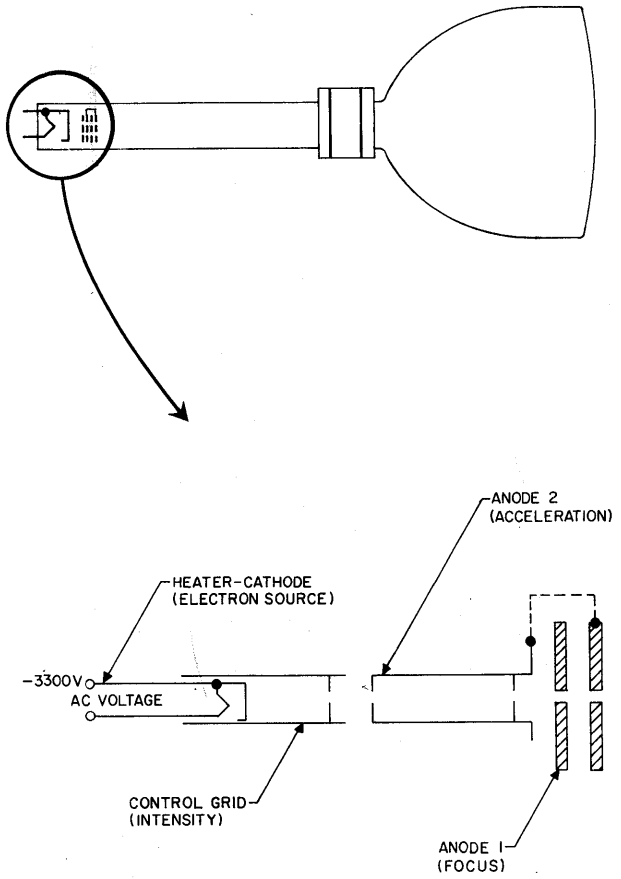


Figure 2–10. Electron Gun, Elements and Control Functions

The potentials applied to the elements of the electron gun determine the characteristics (blanked and unblanked, intensity, and cross-sectional area) of the electron beam. The SD CRT is blanked (electrons cannot pass through control grid aperture) by the fixed bias on the control grid. An intensity gate applied to the control grid unblanks the SD CRT. The magnitude of the gate controls the image intensity (the quantity of electrons passing through the aperture to the tube). The electrostatic field between the control grid and anode 2 is a fixed electron lens which focuses the electron beam on the aperture in anode 2. This anode and the accelerating potential applied to it produce a concentrated beam of high-velocity electrons coincident with the longitudinal axis of the tube. At this point, unimpeded progress of the beam would result in a circular image greater in cross-sectional area than the area originally at anode 2. To overcome this projecting increase in area, anode 1 (focusing anode) is physically located adjacent to anode 2. The electrostatic field between anode 1 and the two elements of anode 2 form a second electron lens which will overcome the dispersive effect of mutual repulsion between the electrons. A fixed-focus potential applied to anode 1 is adjustable and is set to produce a pinpoint image on the viewing screen of the SD CRT.

A defocus gate applied to anode 1 superimposes a positive voltage level on the fixed focus potential. This changes the focal effect of the electron lens to broaden the beam (increase its cross-sectional area).

The heater voltage is supplied from a transformer winding of the high-voltage unit, model A (AHVU). The cathode voltage is fixed at —3,300V, obtained from the high-voltage power supply, model C (CHVP). The cathode voltage return is tied to one side of the filament.

The control grid is biased by a voltage obtained from AHVU. This voltage is adjustable between fixed potentials (—3,450 and —3,300V by an intensity control in AHVU.) The bias on the control grid is sufficient to cut off the flow of electrons to the screen (blanked). The variable gate amplifier, model A (AVGA), output is fed to the control grid through AHVU and is the source of intensity gates (unblanking). The intensity gate signal will overcome the cutoff bias on the control grid and cause it to conduct electrons, illuminating the screen and therefore unblanking it. Anode 2 is maintained at +45V by AHVU. The voltage differential between the cathode and anode 2 (3,345V) is the accelerating potential for the electrons emitted by the cathode. The potential on anode 1 is adjusted to a fixed voltage (between —2,700 and —2,300V) by the setting of a focus control in AHVU. The resultant electrostatic field set up between anodes 1 and 2 determines the cross-sectional area of the electron beam. A defocus gate, supplied by the variable gate amplifier, model B (BVGA), is fed to anode 1 through AHVU. This defocus gate is used to vary the cross-sectional area of the electron beam.

The potentials applied to the elements of the electron gun determine the characteristics (blanked and unblanked, intensity, and cross-sectional area) of the electron beam.

2.2.1.2 Character Selection

The character selection plates of the SD CRT, in association with the matrix, select a specific character for display. The following theory of character selection operation explains the method of deflection and the origin of deflection voltage. Figure 2–12 is a simplified drawing of the character selection plates. The insert drawing shows the approximate location of the plates within the envelope of the SD CRT. Figure 2–13 is a block diagram of the circuits located in the SDGE and the model A high-voltage unit, which are associated with the SD CRT.

A significant feature should be noted before proceeding. In figure 2–13, the horizontal selection decoder feeds the vertical character selection plates. This would appear to be an obvious error, but the effect of the convergence coil (refer to 2.1.1) on the path of the electron beam makes this necessary. The electron beam rotates 90 degrees in passing through the convergence coil area of the magnetic field. To compensate for this effect, the matrix is reoriented 90 degrees in the counter direction. The 90-degree rotation has the effect of interchanging the X and Y axis. For this reason, X-axis selection voltages must be applied to the vertical selection

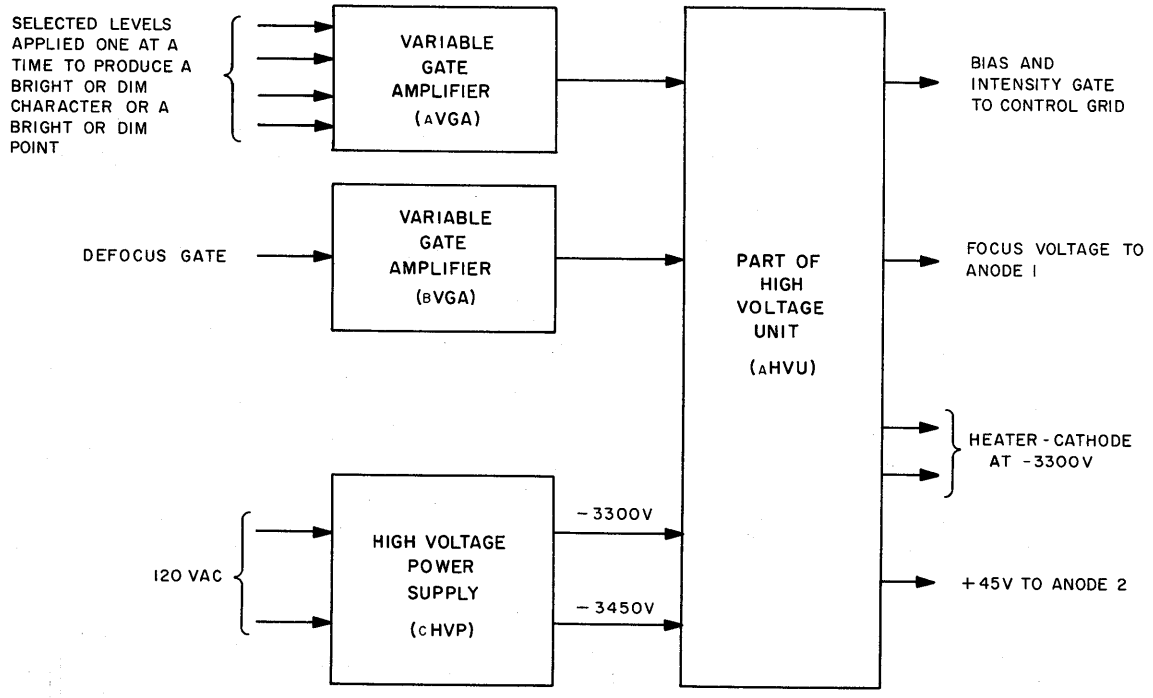


Figure 2–11. Electron Gun, Control and Supply Voltages, Block Diagram

TABLE 2–1. SD CRT FUNCTIONAL REQUIREMENTS AND ASSOCIATED TUBE ELEMENTS

FUNCTIONAL REQUIREMENTS			
NUMBER	CHARACTER DISPLAY	VECTOR DISPLAY	SD CRT ELEMENT
1.	Generate an electron beam.	Generate an electron beam.	Electron gun
2.	Defocus the beam.	Focus the beam.	Anode 1
3.	Intensify (bright or dim) the beam.	Intensify (bright or dim) the beam.	Control grid
4.	Accelerate the beam.	Accelerate the beam.	Anode 2
5.	Aim the beam at a character.	Aim the beam through the vector aperture.	Character selection plates
6.	Form the beam in the shape of the character.	Pass focused beam unchanged.	Matrix
7.	Spiral the beam through 90 (450) degrees and make it intersect the longitudinal axis of the SD CRT.	Spiral the beam through 90 (450) degrees and make it intersect the longitudinal axis of the SD CRT.	Convergence coil
8.	Cancel deflection applied in No. 5, above.	Cancel deflection applied in No. 5, above.	–
9.	Position character-formed beam in the required location in the message format.	Position the pinpoint-focused beam in the required location in the message format.	One set of character compensation, character position, and vector generation plates
10.	–	Sweep the beam in a given direction through a given distance.	–
11.	Position the message on the face of the SD CRT.	Position the message on the face of the SD CRT.	Deflection yoke

plates. Similarly, the Y-axis selection voltages must be applied to the horizontal selection plates.

The character selection plates generate electrostatic-deflecting fields as a function of analog voltages. An electron beam passing through such a field is deflected in the direction of the more positive plate. The beam deflection is proportional to the voltage differential applied to the plates (forward velocity is assumed constant). Figure 2–12 shows the path of an electron beam under three different conditions. Path A depicts an undeflected electron beam. The voltages on plates U and D are equal and the voltages on plates L and R are equal. Path B represents an electron beam deflected in the vertical position only. To produce this result, deflection plate U is positive with respect to plate D. Plates L and R still have an equal potential. Path C represents an electron beam deflected both vertically and horizontally. To achieve this effect, plates U and L are each more positive than plates D and R, respectively. By the application of appropriate voltages to the deflection plates, the electron beam is accurately directed to any selected point on the reference plane or, as is physically the case, the character matrix.

The character selection voltages are generated in the SDGE (fig. 2–13). Binary input levels are applied to two 3-bit decoders, one decoder for each axis (X-Y) of deflection. The two decoders are packaged as a single unit and designated as the 6-bit binary decoder. There are eight combinations of binary levels for each axis. As a result of these inputs, the binary decoder produces an analog voltage output at one of eight possible corresponding levels. Each level corresponds to a row (X-axis) or column (Y-axis) in the character matrix. These analog levels are fed to the analog driver which drives the corresponding selection-centering and amplitude-control circuits. The control circuits are tied to their respective character-selection plates as indicated in figure 2–13.

2.2.1.3 Electron Beam Shaping

As described in the introduction (par. 1.1 of this part), the electron beam is formed and shaped as an extrusion or stenciling of the particular character cutout in the matrix (fig. 2–14). There are 63 such characters in an equidistant format of eight columns and eight rows. There is a blank space for the missing 64th character to permit space-blank presentation in a message format. The size of the characters in the matrix is about 1/10 the size of that area presented on the screen by the projected numbers, letters, or symbols which are the characters in a typical display message.

Besides the character representation, another important factor in the formation of the beam is its cross-sectional area. The area of the beam must be greater than the cutout area in the matrix for full character extrusion.

For vector generation or point selection, the beam is first reduced to a focused point for unimpeded progress through the vector aperture in the matrix. Figure 2–15 illustrates the relative area requirements for the electron beam.

2.2.1.4 Electron Beam Convergence

The character selection plates divert the electron beam from its axial path in the SD CRT. To overcome this effect, the beam must be converged to nearly its original shape and course for further control. The convergence coil is used to counteract the effect of the

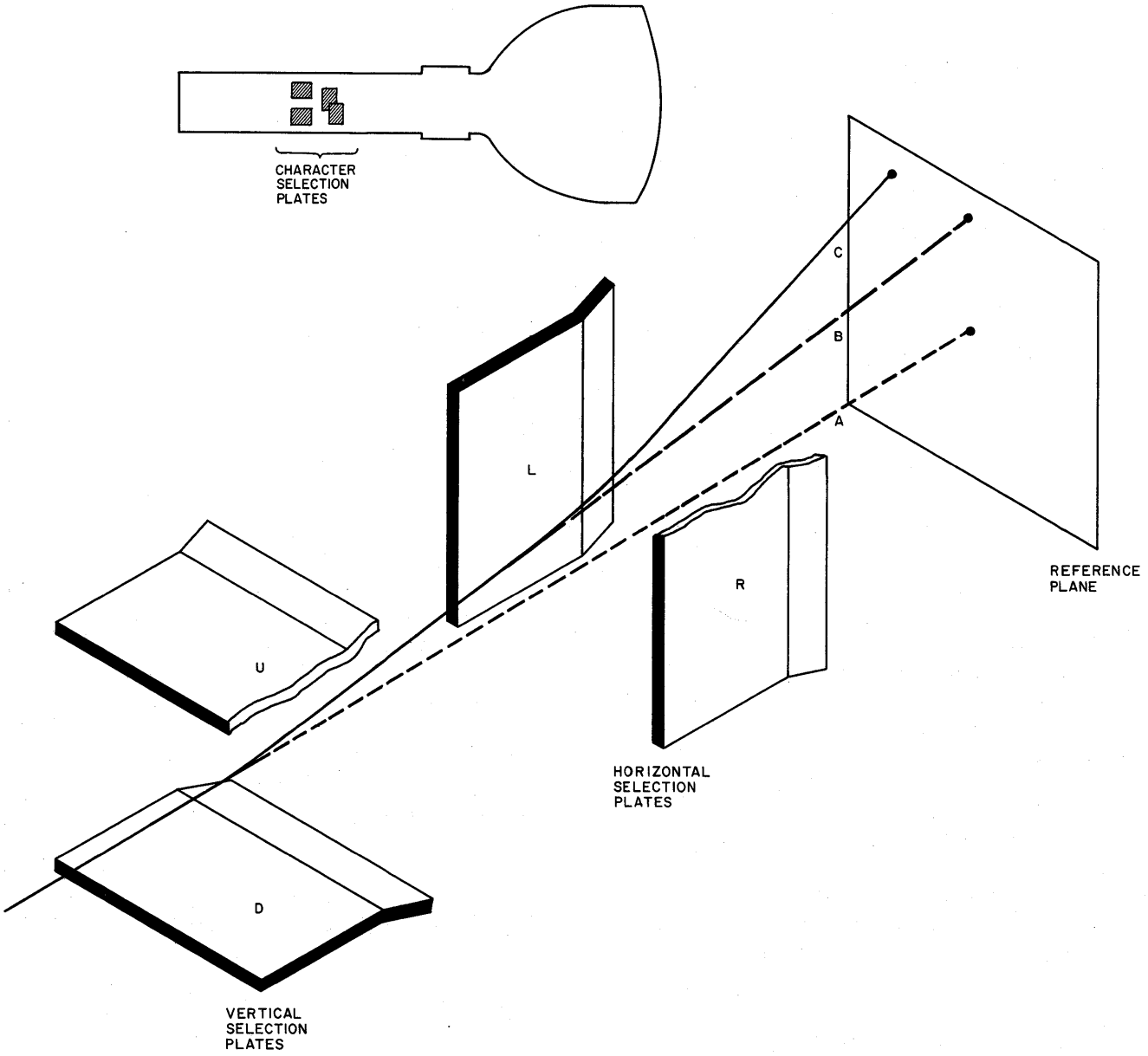


Figure 2–12. Character Selection Plates, Effect on Electron Beam

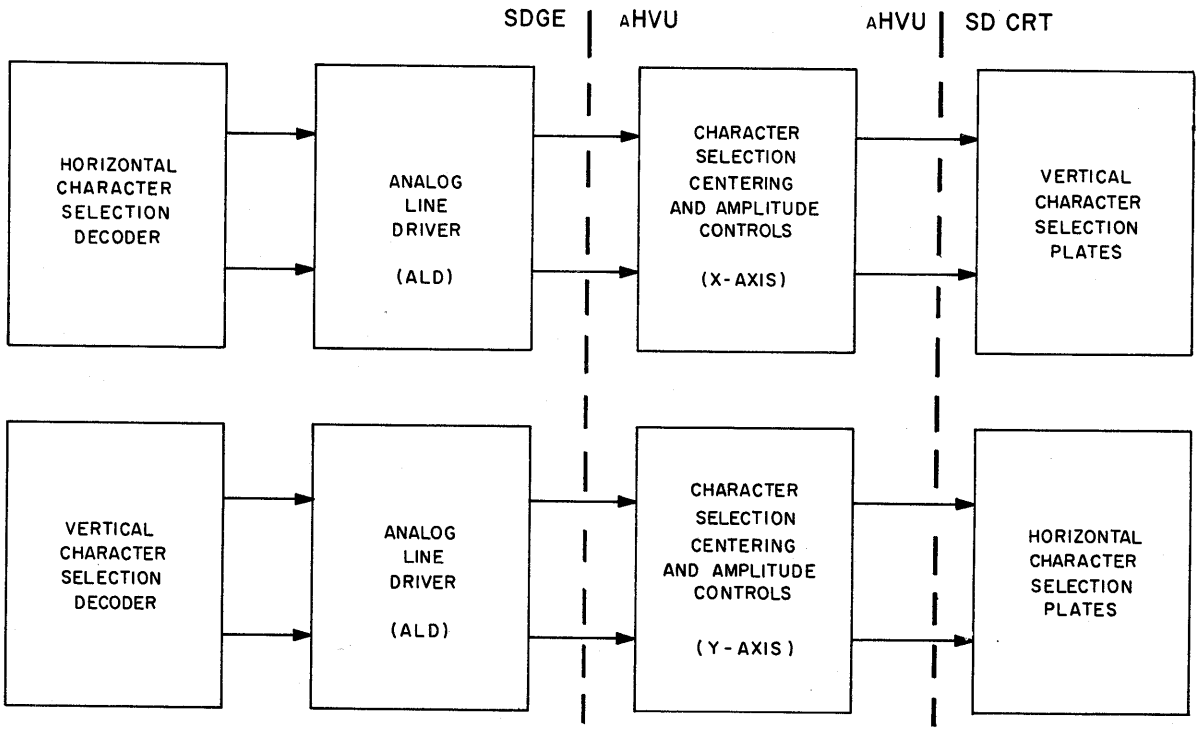


Figure 2–13. Character Selection Control Circuits, Block Diagram

character-selection plates on the beam. The deflection imparted to the beam by the selection plates is designed to intersect the matrix at the selected character. In figure 2–16, where this intersection is illustrated, the focusing effect of the convergence coil's magnetic field can be followed, from left to right.

As seen in figure 2–16, if the four electron beam paths are extended in a straight line from the point of emergence from the deflection plates to each of the four selected characters, the individual beam paths are obviously divergent. Before any one of the beams (the four beams represent four typical characters) can be further controlled, the beam must be returned to the same focal point on the longitudinal axis. This is effected by generating a uniform magnetic field whose lines of flux are parallel to the axis of convergence. This magnetic field is created by the SD CRT convergence coil.

Figure 2–17 shows the convergence effect of the magnetic field caused by the convergence coil. The heavy lines, running from left to right, represent the beam paths of four different respective characters. Each is initially deflected to a different point through the character matrix. The individual beams continue in straight lines to the convergence coil area, where each enters the magnetic field at a different angle. The convergence force of the field on the electron beam is proportional to the angle of deflection. Consequently, the outer beams are subjected to a greater bending force than the inner beams, with the result that all deflected beams ultimately intersect at one focal point on the longitudinal axis. In addition to the convergent effect of the magnetic field, a rotational or spiraling force is exerted on the electron beam.

The sum of the forces exerted on the electrons in the beam produces a resultant which imparts a sideward and inward (convergent) force on a beam. Figure 2–9 shows the combined effects of these forces on an electron beam stenciled by the character W. The angle formed by the electron beam and the longitudinal axis of the SD CRT (after the beam leaves the mag-

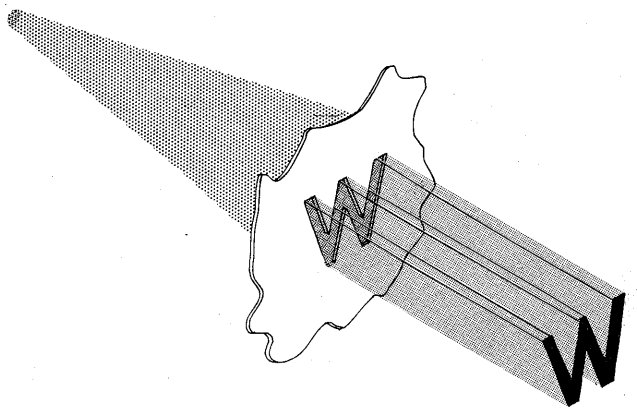


Figure 2–14. Character-Matrix Effect on Electron Beam

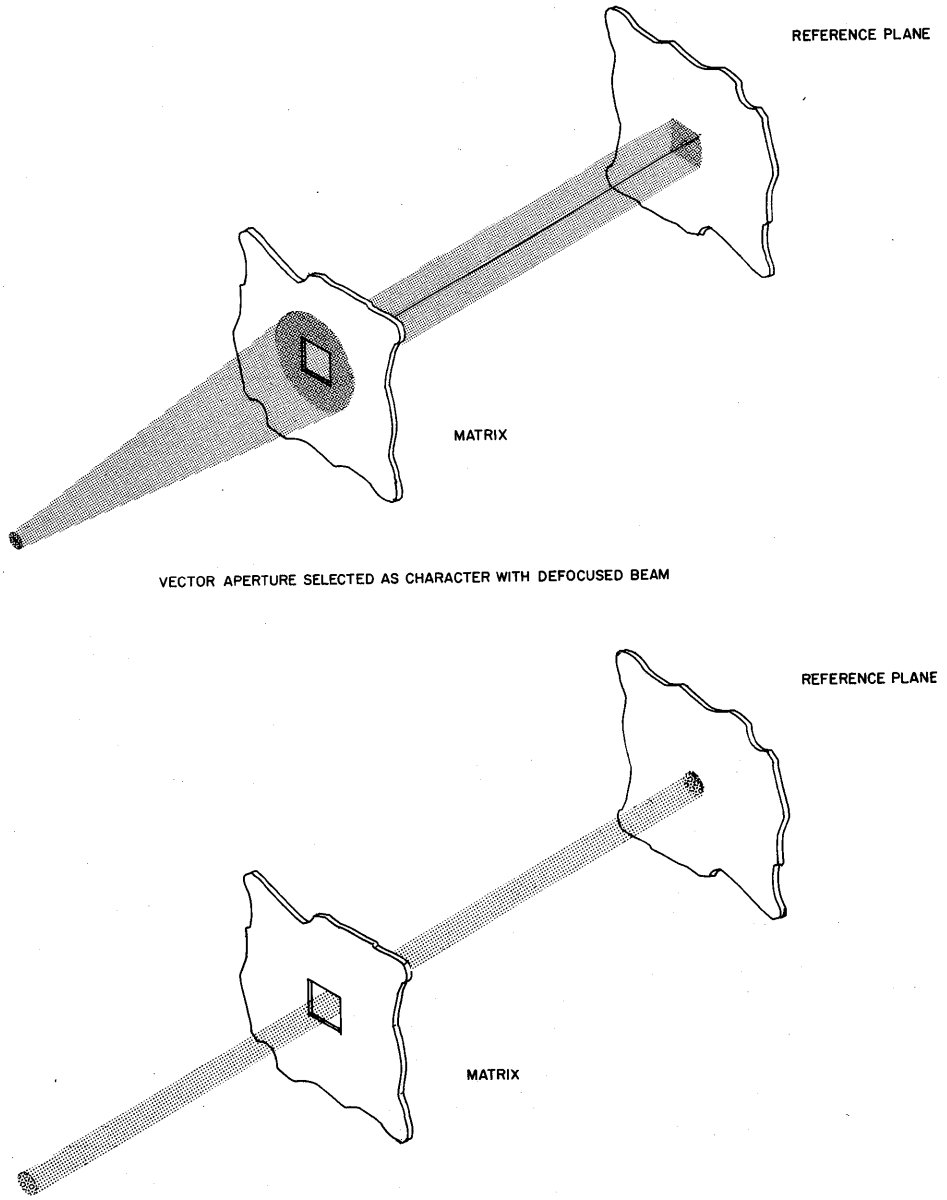


Figure 2–15. Relative Area of Defocused and Focused Beam through Square Aperture

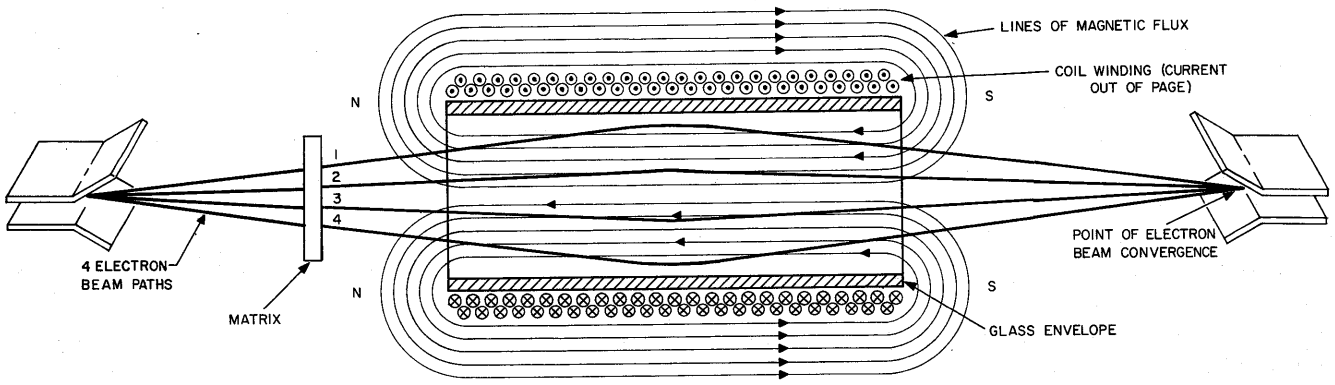


Figure 2–16. Focusing Effect of Convergence Coil Magnetic Field

netic field) is identical with the angle of deflection imparted by the character selection plates.

The circuits which control the extent of rotation and ensure a constant point of convergence of the electron beams are shown in block form in figure 2–18. This point of convergence and the degree of rotation are a function of magnetic field strength and electron beam velocity. Convergence coil current determines magnetic field strength; accelerating potential determines beam velocity. If either varies, the point of convergence and degree of rotation will vary, producing misalignment and tilting of characters in a message display. The model A convergence current regulator (ACCR) controls convergence coil current to prevent any variation.

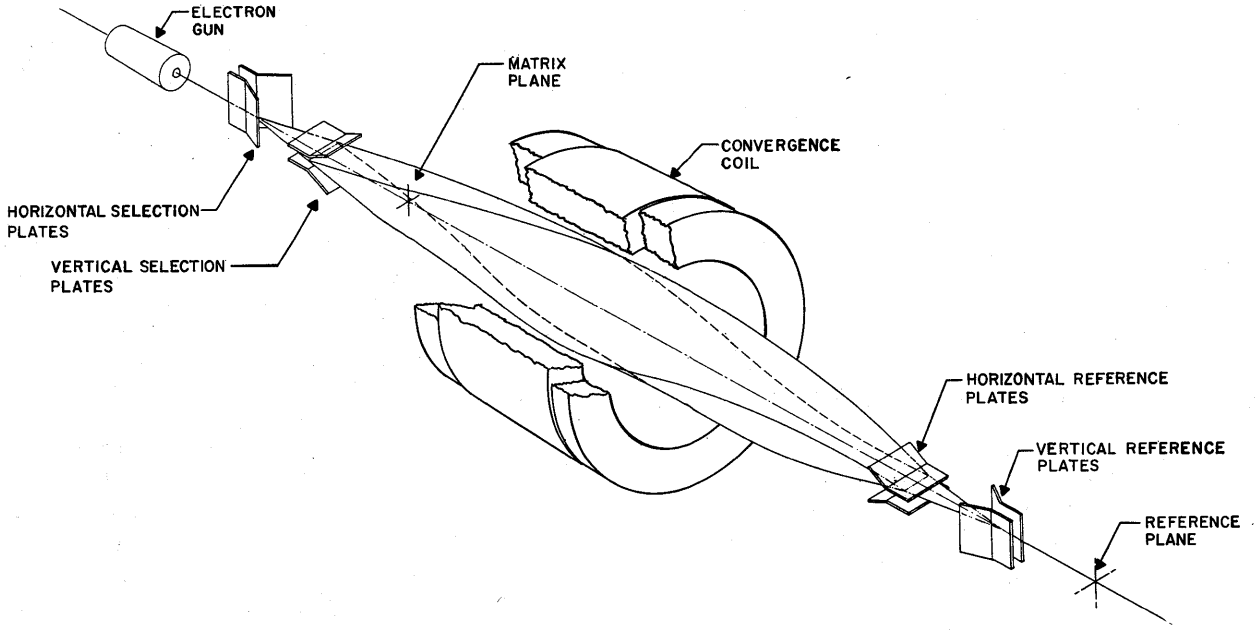


Figure 2–17. Effect of Convergence Coil in Returning All Beams to Reference Plane Axis

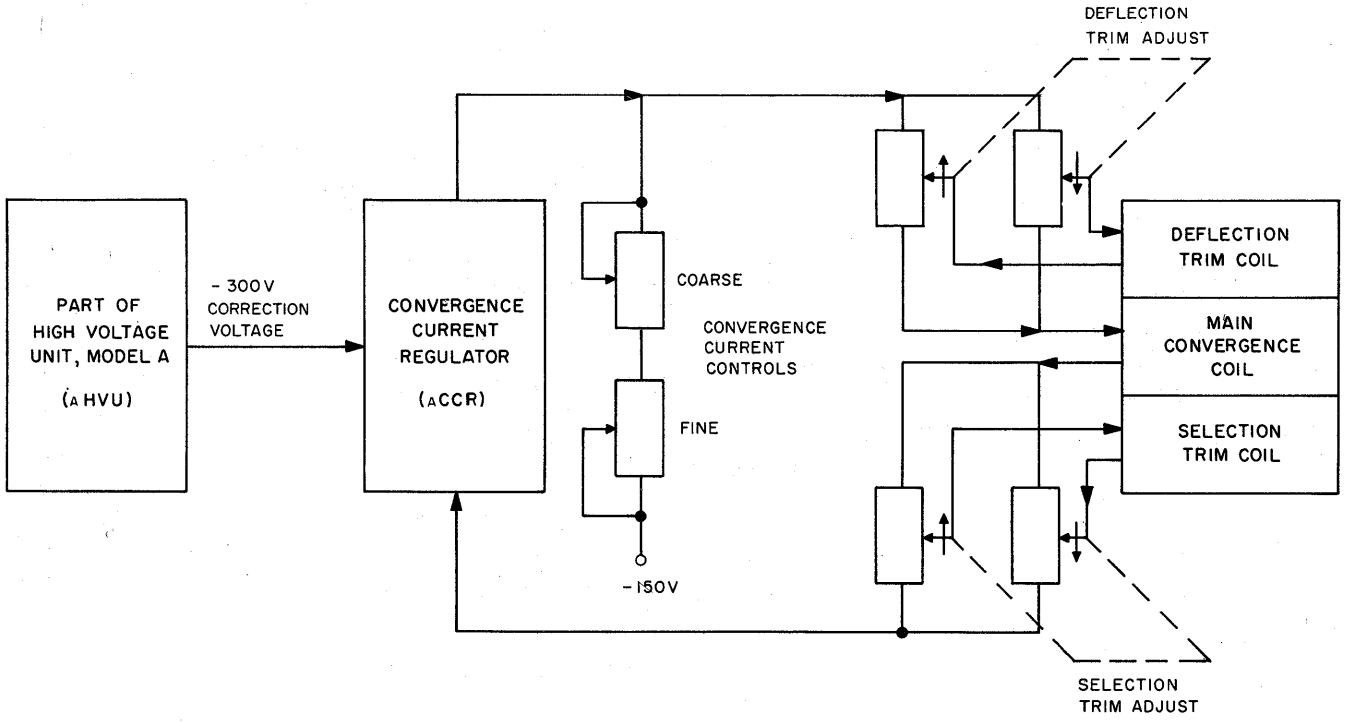


Figure 2–18. Convergence Coil Assembly and Associated Circuits, Block Diagram

The model A high-voltage unit provides a correction voltage which varies about a nominal voltage of —300V. This variation is proportional to accelerating voltage variations. The ACCR output current is a function of this correction voltage variation and compensates for electron beam velocity variations. Thus, if the beam speeds up, the magnetic field is strengthened. If the electron beam slows down, the magnetic field is weakened. Nominal magnetic field strength is set by means of the convergence current controls. These controls have the greatest influence on beam rotation and point of convergence. Final adjustments are made with the selection and deflection trim adjustments.

The selection trim coil serves two functions. It isolates the selection plates from the convergence coil magnetic field and permits precise adjustment of rotation within a range of approximately 4 degrees. The deflection trim coil also serves a dual purpose. It enables precise control of the point of convergence within the area of compensation and positioning plates, and isolates the convergence coil magnetic field from these plates.

2.2.1.5 Character Compensation and Positioning

After leaving the convergence coil area, the electron beam passes between the compensation and positioning deflection plates. The method of deflection is the same as that discussed in paragraph 2.2.1.2. Figure 2–19 shows the approximate location of the character compensation and positioning plates within the tube envelope.

The circuits providing the control voltages to the deflection plates are shown in block form in figure 2–20. Binary position and compensation-determining levels are converted into analog voltages by the respective decoder in the SDGE. The analog voltages are fed through the model A high-voltage unit AHVU to the deflection plates of the SD CRT by the respective analog line drivers (ALD). The compensation voltages are the character selection voltages with reversed polarity, which nullify the character selection deflection and make the electron beam coincident with the longitudinal axis of the SD CRT. Applied simultaneously, the positioning voltages impart a new deflection to the electron beam which positions the selected character in the required location within a message format. In effect, the compensation and position plates straighten out the beam and reposition it. The vector-generation function of these plates is discussed in paragraph 2.2.2.

2.2.1.6 Message Deflection

Each message unit, consisting of a vector and/or character, is deflected to a particular location on the viewing screen of the SD CRT by the deflection coil. Figure 2–21 shows the coil with one pair of deflection windings. The inset drawing shows the approximate location of the coil around the neck of the tube envelope. The coil is wound on a square form. There are two windings. The black winding on the top and bottom sides of the coil is a continuity between the power supply and the deflection driver (DEF); similarly, the white winding is continuous to the control circuits.

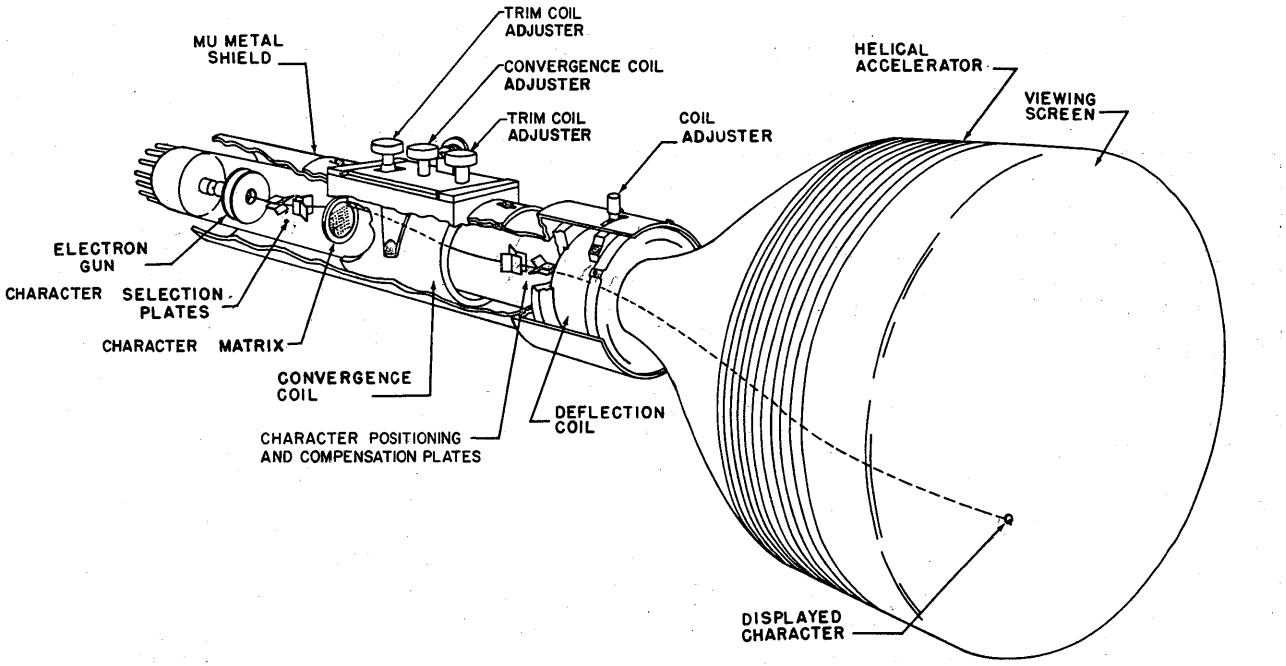


Figure 2–19. 19-Inch SD CRT, Cutaway View

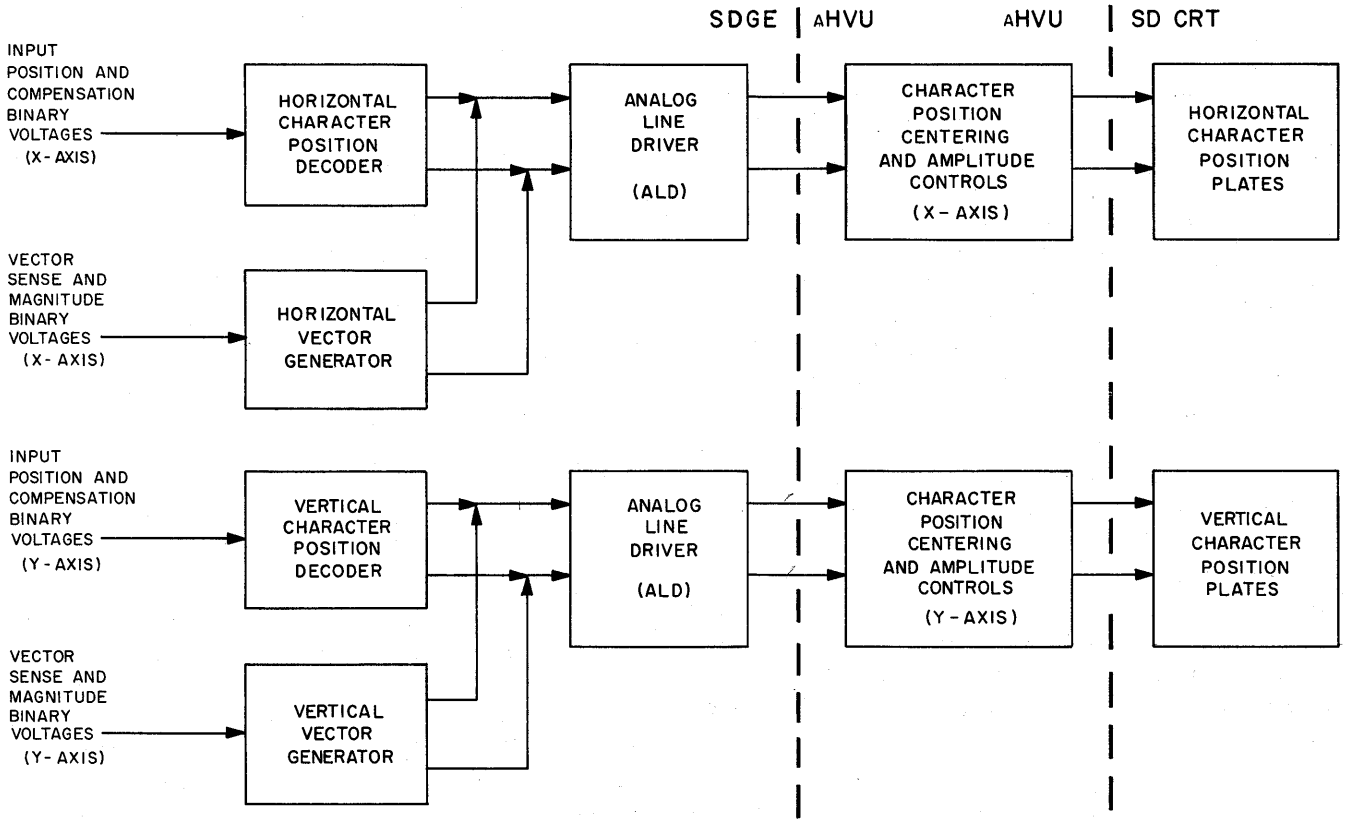


Figure 2–20. Character Position, Compensation, and Vector Generation Control Circuits, Block Diagram

Electron flow through the black winding generates a magnetic field of opposing polarity to that generated by the white winding. The vertical sides of the coil (not shown in figure) have the same type of windings. This results in a magnetic field of variable strength and reversible polarity that can be generated along each axis (horizontal and vertical) with the neck of the SD CRT. The magnetic field strength is a function of the magnitude of the electron flow. The polarity of the field is determined by the winding which carries the greater electron flow.

Figure 2–22 illustrates the field-generating properties of the windings on one vertical side of the coil. The discussion concerning these windings applies equally to the windings on each of the other three sides of the coil. Solid and dashed lines are used to distinguish between the two windings and their respective fields. As shown, electronic flow in the solid-line winding (I_2) is in a counterclockwise direction and produces a north pole at the top of both vertical coil members. Electron flow (I_1) in the dashed-line winding is in a clockwise direction and produces a north pole at the bottom of both vertical coil members. With I_2 greater than I_1, the solid-line magnetic field is the stronger. An electron beam directed into the page is deflected to the right. With I_1 greater than I_2, the dashed-line magnetic field is stronger, and an electron beam directed into the page is deflected to the left. With I_1 equal to I_2, the magnetic fields are completely neutralized, and the beam is not deflected. Thus, horizontal deflection is a function of the electron flow in the vertical coil windings. Similarly, vertical deflection is a function of the electron flow in the horizontal coil windings. The electron flow in the vertical windings is controlled by two tubes operating in push-pull. An increase in I_1 occurs simultaneously with a like decrease in I_2.

Figure 2–23 is a block diagram of the circuits which are utilized in message-positioning. The 10-bit binary decoder produces an analog voltage as a function of 10 binary levels. There is one decoder for each deflection axis. The decoder outputs are applied to the respective deflection amplifier and driver together with a reference level from the decoder simulator. The deflection drivers and amplifiers maintain a linear relationship between this analog voltage input and the currents supplied to the windings in the deflection coil. Thus, a direct relationship between digital-positioning information and message-deflecting currents is established to permit precise positioning (within 1/1024 increment of total deflection along either axis) of a message on the viewing screen of the SD CRT.

2.2.1.7 Character Display Summary

An intensity gate and a defocus gate applied to the appropriate elements in the electron gun provide an electron beam of a large cross-sectional area. The beam is accelerated toward the character selection plates. Analog voltages applied to these plates deflect the electron beam to a character on the character matrix. The electron beam, in passing through the matrix, is extruded into the shape representing the character and enters the magnetic field of the convergence coil. The magnetic field converges the beam to intersect the longitudinal axis of the SD CRT in the area of the character position and compensation plates.

Analog compensation voltages applied to the character-position plates bend the beam to coincide with the longitudinal axis of the SD CRT. Simultaneously, analog-positioning voltages applied to these plates deflect the electron beam to the required position in the message format. The electron beam next enters the deflection coil area. Analog currents in the deflection coil windings generate a magnetic field which deflects the electron beam to the required point on the viewing screen of the SD CRT.

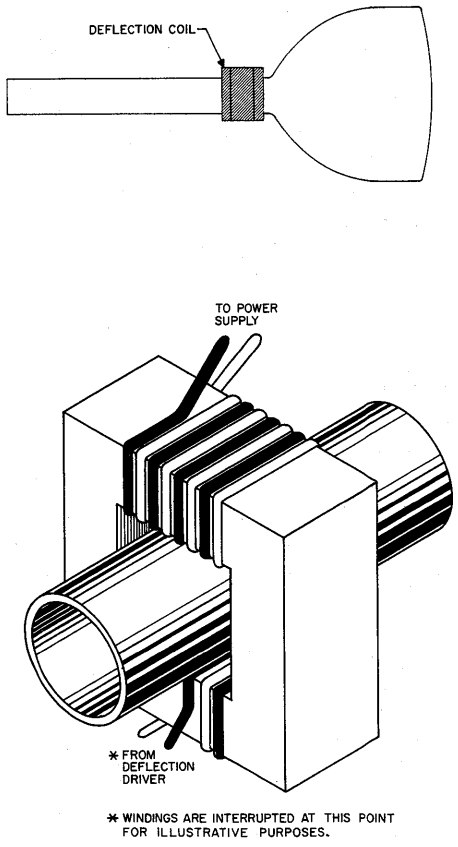


Figure 2–21. Deflection Coil, Horizontal Windings, Simplified Drawing

Note

During convergence, the magnetic field rotates the electron beam by 90 degrees in a counterclockwise direction (viewed from the face). The character matrix is oriented in a position (rotated 90 degrees from the vertical in a clockwise direction) to compensate for the rotation caused by the convergence coil.

2.2.2 Vector Display, Detailed Operation

The procedure for producing a vector is summarized in table 2–1. A discussion of the vector display operation follows.

The vector intensity gate unblanks the SD CRT. The gate width is 50 μsec, twice as long as the character intensity gate. Two factors determine the characteristics of the vector intensity gate. First, the vector is generated by a moving electron spot or point. The intensity of the point must be increased to produce a vector with an overall intensity equal to the intensity of the character. Second, all vectors are generated in the same length of time, irrespective of vector size. When a dim image of a vector is required, the intensity gate is correspondingly reduced in amplitude. Refer to the discussion of the model A variable gate amplifier for a more detailed discussion of the intensity gates.

The electron beam must have the smallest cross-sectional area possible. The focus adjustment in high-voltage unit model A determines this area. A focus gate can be considered the absence of a defocus gate. In the absence of the latter, the adjusted focus of the electron beam prevails. As shown in figure 2–15, this adjustment permits unchanged passage of the electron beam through the character matrix.

The character selection plates deflect the electron beam into and through the vector aperture in the character matrix. The convergence coil directs the beam at the point of convergence between the character position and compensation plates. Here, as in character display, the beam is returned to the longitudinal axis of the SD CRT by the application of analog voltages opposite in polarity to the character selection analog voltages. Simultaneous with the application of these correction voltages, analog vector-positioning voltages are applied, deflecting the electron beam to the vector point of origin in the message format. Immediately thereafter, sweep voltages are superimposed on these voltages at the character position plates. The electron beam is swept by the varying pairs of potential (X and Y), producing a straight-line image of the required direction and length.

The entire message presentation (or format), of which the vector is a part, is positioned on the face of the SD CRT by the deflection coil.

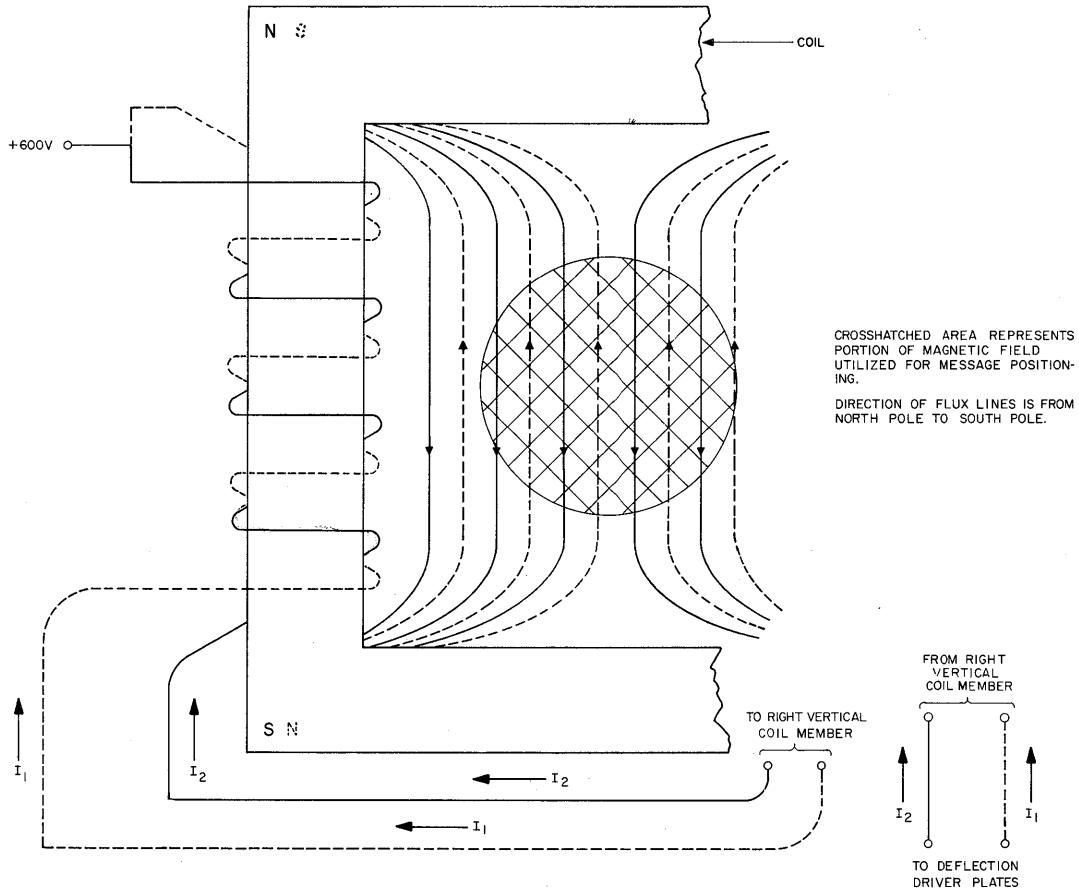


Figure 2-22. Deflection Coil, Magnetic Field Diagram

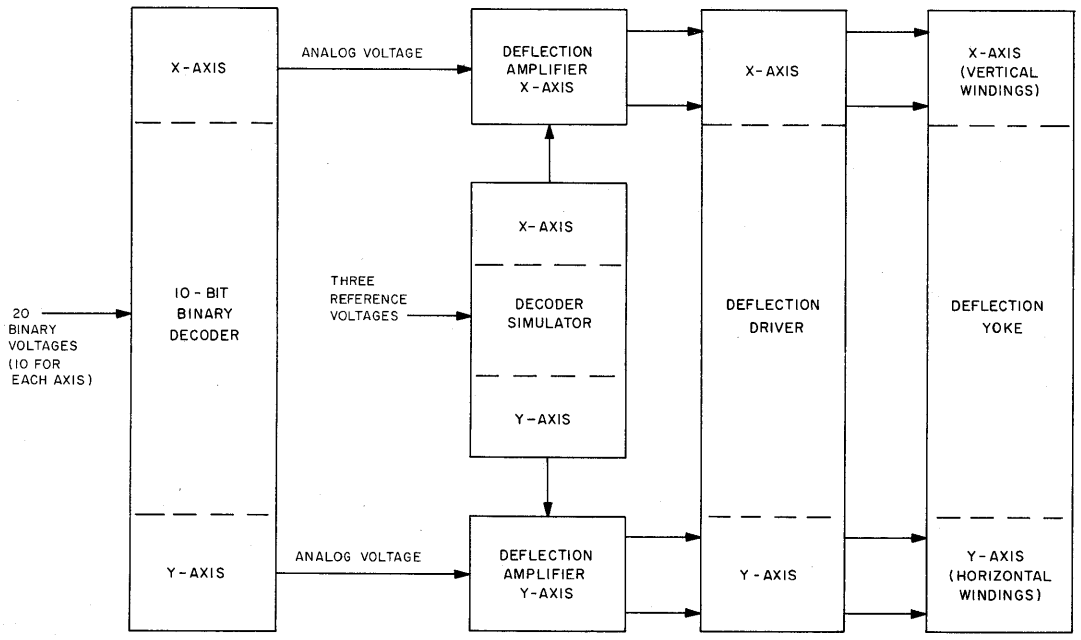


Figure 2-23. Message-Positioning Control Circuits, Block Diagram

CHAPTER 3
7-INCH SD CRT

3.1 GENERAL

The 7-inch SD CRT is similar, operationally, to the 19-inch SD CRT except with respect to the following: the location of the character matrix, flexible placement of the convergence coil, and the addition of an auxiliary focus coil. Figure 2–24 is a schematic representation of the 7-inch SD CRT symbol.

The character matrix in the 7-inch tube is located in the center of the convergence field. In the 19-inch tube, the matrix is fixed at the electron gun end of the convergence field. The convergence coil can be moved and set-positioned along the neck of the 7-inch CRT. The 19-inch SD CRT convergence coil, as such, is fixed. The auxiliary focus coil employed on the 7-inch tube is used to ensure maximum definition of display. This tube is used exclusively for photographic reproduction, thus making extreme definition essential for subsequent large-screen image projection. As a further aid to faithful photographic recording, the viewing screen phosphor emits a blue light to which photographic emulsions are sensitive. This P11 phosphor is also employed for the 19-inch SD CRT used in the camera console.

With the exception of the differences already enumerated, the 7-inch SD CRT is very much the same as the 19-inch SD CRT. Therefore, for detailed operation, reference should be made to the 19-inch tubes. The following discussions are limited to the differences only. Figure 2–7 is a cutaway view of the 7-inch SD CRT, showing the location of the character matrix and the focus coil.

3.1.1 Auxiliary Focus Coil

The object of this additional coil, as previously stated, is to ensure sharply defined displays necessary for reproduction. It does this by realigning the electrons diverging from the beam proper. These electrons would normally be projected as blurred, indistinct images. With the aid of the auxiliary focus coil, the projecting and deflected electrons are compelled to follow a path that will make them meet with the main body or beam of electrons that come into the focus coil field. See figure 2–25. The size of this path is such that electrons which are far off the longitudinal axis of the beam will come into the magnetic field almost parallel to the axis. All electrons will now be heading directly toward the crossover point with the same velocity and at the same time. If all the electrons now require the same

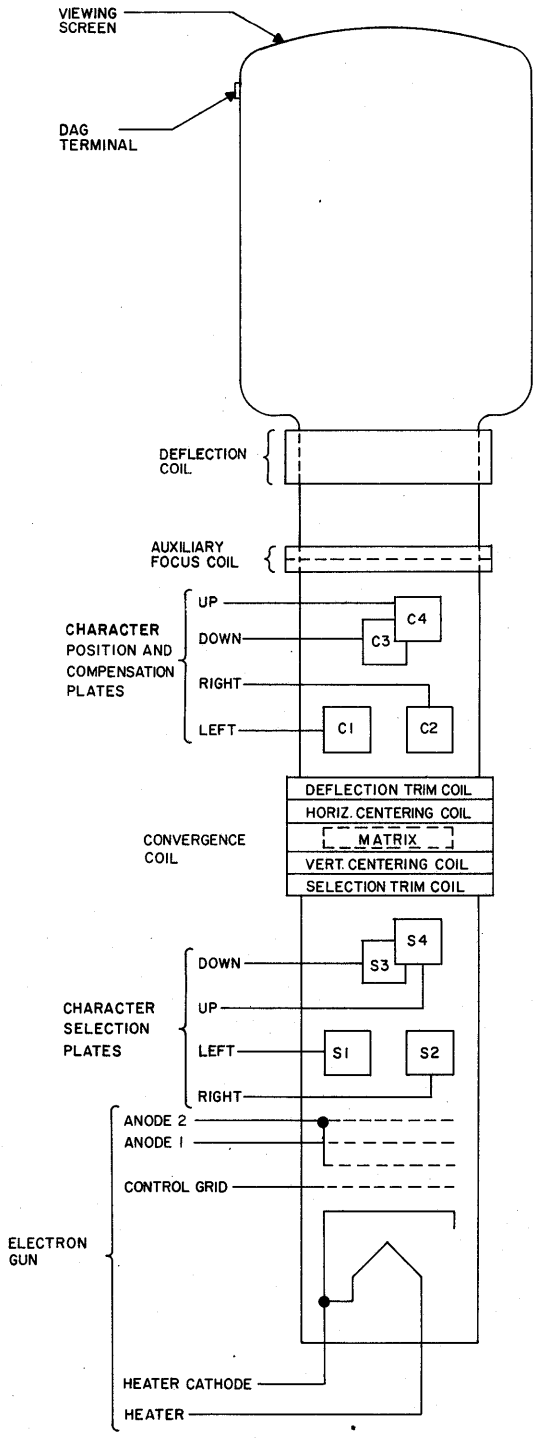


Figure 2–24. 7-inch SD CRT Symbol

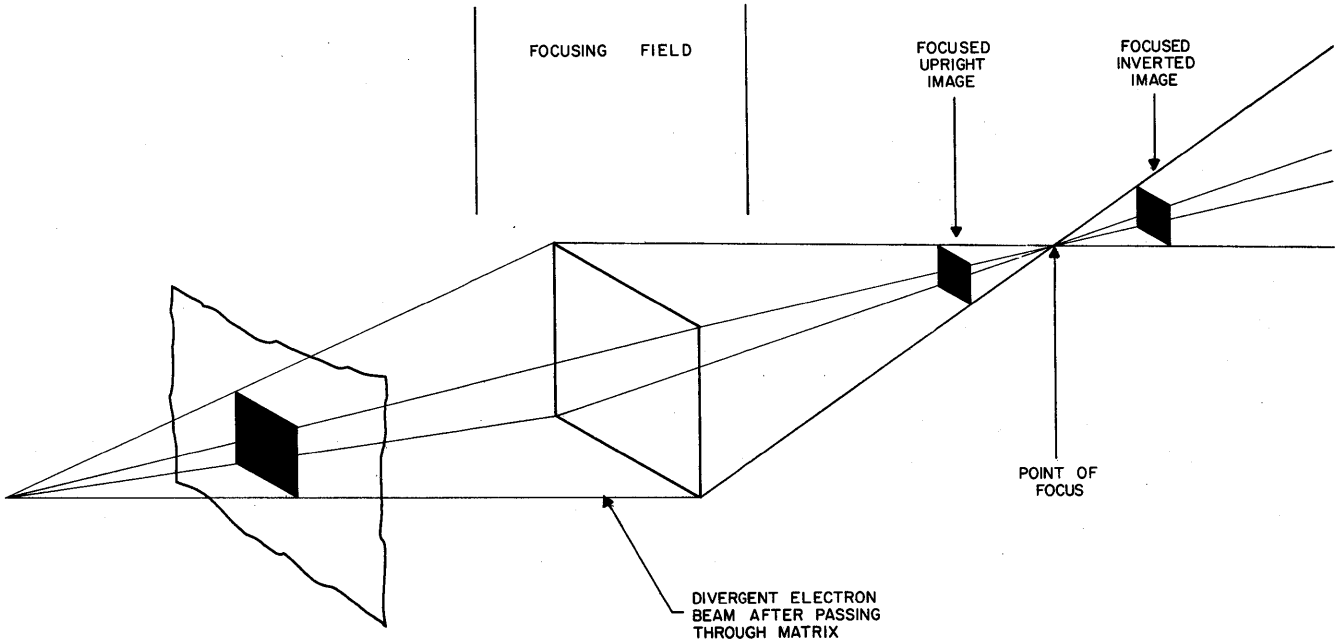


Figure 2–25. Focusing Coil Effect on Character-Formed Electron Beam

length of time to pass through the magnetic field, they will meet at a common point. If the strength of the magnetic field is adjusted so this common point is at the fluorescent screen of the tube, the beam will be sharply defined and capable of being recorded for large-screen projection.

As is the case with the convergence coil, or any device producing a magnetic field, a spiral rotation is imparted to the electron beam by the focus field. This is offset by an opposing field produced by a bucking winding of the dual-winding focus coil. Therefore, no additional compensation for rotation is necessary for the focus-coil field effect.

3.1.2 Character Matrix Location

The location of the character matrix is not the same as it is in the 19-inch SD CRT. The placement of the 7-inch matrix in the center of the convergence field was again an effort to obtain maximum display recording quality.

Ideal character-forming of the beam is accomplished if the electron beam enters the character matrix perpendicular to the plane of the matrix. This, of course, is the logical physical placement for electron-beam character-stenciling, with minimum distortion. As shown in figure 2–16, the electron beam enters the convergence field at a deflection angle. However, in the center of the field the angle of deflection becomes zero, and the electron beam is parallel to the axis of the tube. It is at this point in the field that the character matrix in the 7-inch SD CRT is located. The spiraling effect of the convergence field imparts a 90-degree rotation to the cross-sectional area of the electron beam. Since the character matrix is located in the center of this field, the beam is rotated 45 degrees before it reaches the focus coil field. It will be remembered that the 19-inch SD CRT matrix was placed before the convergence coil field, thus imparting a 90-degree rotation to the emanating beam. In the manufacture of the 7-inch tube, the matrix is physically counter-rotated to its normal axis to offset the rotation of the beam, so that the image is upright on the viewing screen.

3.1.3 Convergence Coil

The 7-inch convergence coil has the same function as the 19-inch convergence coil. They differ only in the adjustments and physical method of coil placement about the neck of the tube. The 7-inch tube coil is mounted to an inner mu-metal shield which rides along a slot in the main shield by means of a screw-thread device. See figure 5–6. The point of convergence and isolation of the convergence field are established by the manual-positioning of the convergence coil. The coil mount is designed to accomplish this with a minimum of adjustment.

In addition to the differences already mentioned, the convergence coil on the 7-inch CRT has an extra winding. This winding is a horizontal and vertical centering coil superimposed on the convergence coil. This coil, in the form of a quad pancake winding, is arranged so that the field of one pair of coils will affect the X axis of the electron beam; the field of the other pair, the Y axis. In this way, it is possible to control the yaw, pitch, and vertical and horizontal positioning of the electron beam. These controls bring the beam up into reference as required. The field strength adjustments of the vertical and horizontal centering coils are controlled from the operating position of the PRRE unit.

CHAPTER 4
5-INCH DD CRT

4.1 GENERAL

The DD CRT (performs the same basic operation as SD CRT's) displays characters (fig. 2–26) as a function of the analog voltages applied to its electrodes. Figure 2–27 is the symbol used to represent the DD CRT in schematic diagrams.

The two types of tubes can best be compared by referring to figures 2–28 and 2–29. It can be seen that the DD CRT employs electrostatic deflection by means of deflection plates. The SD CRT uses a deflection coil for magnetic deflection, to position the message on a predetermined portion of the screen. The DD tube employs a storage element to enable a continuous display, if so desired, on the viewing screen. This storage element consists of a flood gun (electron gun) and three grids between the flood gun and the phosphor of the viewing screeen. These grids or coatings are called storage mesh, collector mesh, and ion repeller mesh, in line from the phosphor to the flood gun.

The phosphor of the DD CRT viewing screen is of such short persistence that it enables the instantaneous erasure of a message. This is a functional requirement of the tube. For this reason, the methods of creating an image on the face plate of the DD CRT differ from those of the SD CRT. With the exception of these major differences, the other elements of the DD tube function in much the same manner as comparable elements in the SD CRT. The physical dimensions of the DD CRT are given in figure 2–28.

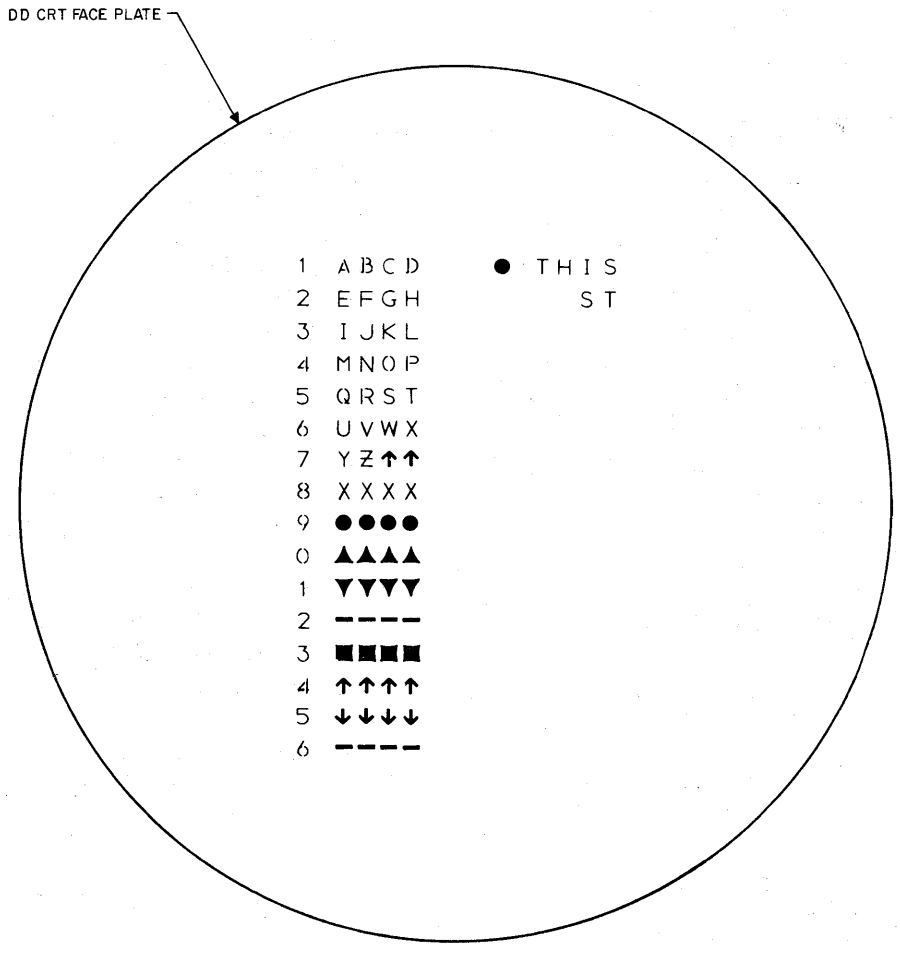


Figure 2–26. Typical Digital Display Characters

4.1.1 Basic Operation

The image displayed on the DD CRT is initiated in the same manner as that in the other CRT's described. The electron gun generates a beam of electrons each time the control grid is fed a positive-going voltage. The beam is then deflected through the desired character in the character matrix by the character selection plates. The resultant stenciled beam is shaped in the form of the selected character. The rotated beam is returned to the longitudinal axis of the tube by the convergence coil before it reaches the character compensation plates. The character deflection plates position the character-formed beam to the proper location in the message format. The beam continues to the storage mesh where it writes the character into the mesh.

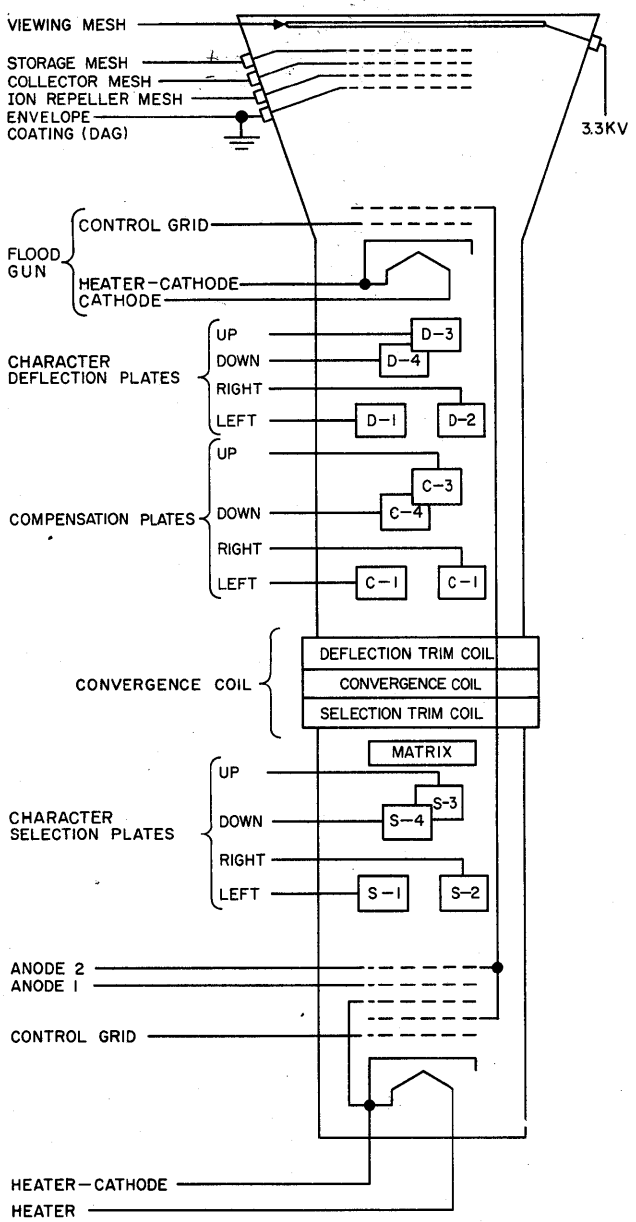


Figure 2–27. DD CRT Symbol

The flood gun is a constant source of low-velocity electrons. These electrons are sprayed out in the shape of a cone with the apex at the emitter of the flood gun and the base of the cone at the phosphors. The base covers the entire viewing surface of the tube. This spray of electrons passes through the electron-transparent portions of the storage mesh to impinge on the phosphors and produce a visual display of the character written on the storage mesh.

A negative erase gate is applied to the collector and storage mesh. This, as mentioned previously, will make the storage mesh opaque to flood-gun electrons prior to writing a new message. Provision is also made for the manual-controlled erasure of the DD message.

4.1.2 Detailed Operation

The detailed operation of the DD CRT is confined to those areas which are peculiar to or different from the elemental operation of those tubes already described. However, the control circuits for all the DD CRT elements are discussed briefly and in the sequence listed in table 2–2.

4.1.2.1 Electron Gun

The electron gun of the DD CRT provides a defocused beam each time an intensity (unblanking) gate is applied to the control grid. (Fig. 2–30 is a block diagram of the control and supply voltage circuits for the electron gun.) Since the DD message consists of characters only, a defocus gate is not required (as was employed with the SD CRT) because the beam is normally defocused. Anode 1 voltage is supplied directly from the focus control in the BHVU. This control is adjusted to give the beam a cross-sectional area which will encompass the largest character cutout in the matrix. Once the proper adjustment is made, the beam will remain constant. The heater is supplied with 6.3V, one side of which is the −3,150V cathode return from the CHVP. The bias on the control grid keeps the tube at cutoff until overcome by the positive pulse of the intensity gate. This intensity gate or unblanking signal is fed through the CVGA and BHVU to the control grid of the electron gun. The electron beam will pass through the DD CRT to the storage mesh only when the intensity gate is present.

The accelerating anode (or anode 2) is tied to the +45V tap of a voltage divider in BHVU. This +45V added to the −3,150 cathode voltage provides an accelerating potential of 3,195V.

4.1.2.2 Character Selection

The character selection plates of the DD CRT function in much the same manner operationally as their counterparts in the SD CRT. Refer to paragraph 2.2.1.2

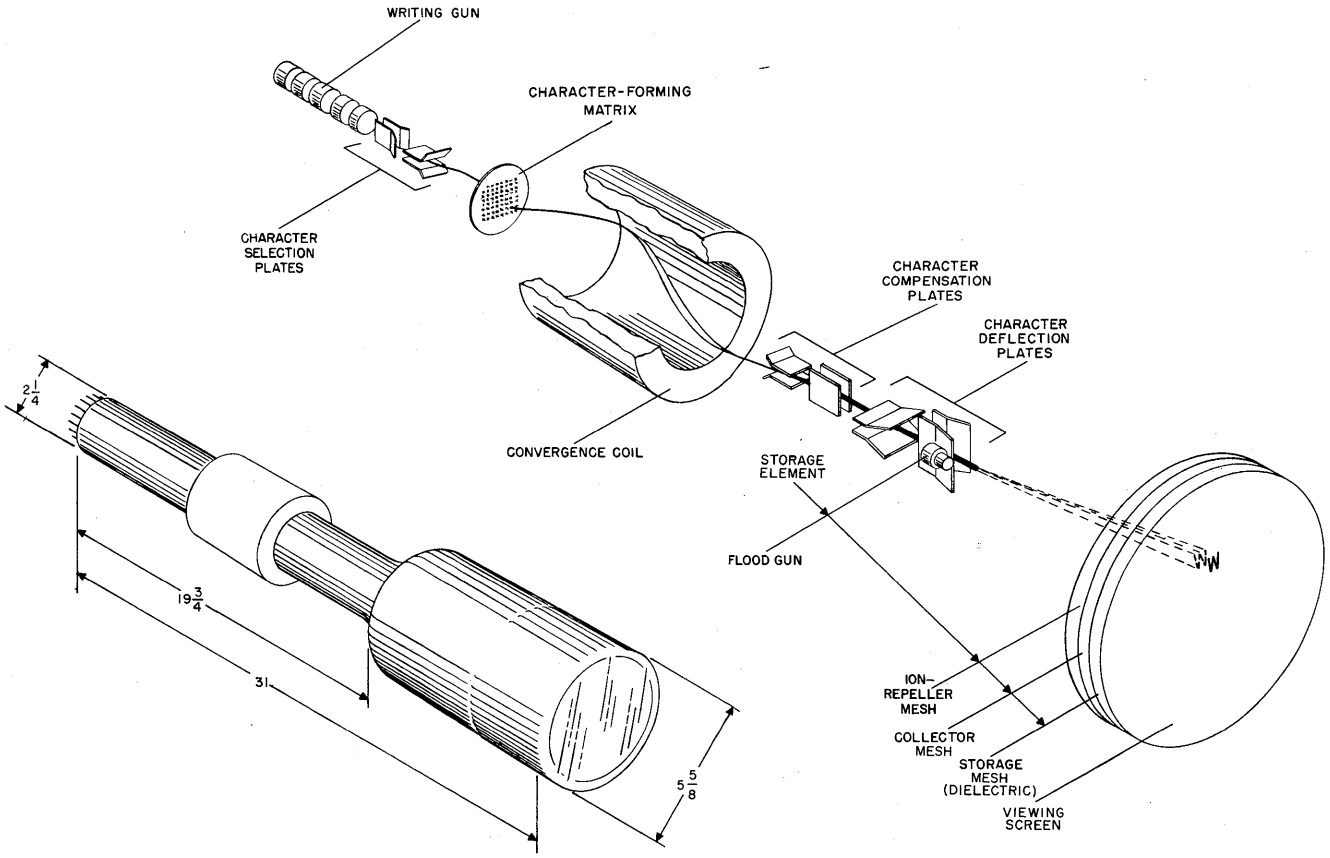


Figure 2–28. DD Cathode-Ray Tube

of Chapter 2 for a detailed explanation of the deflection necessary for character selection. Figure 2–31 is a block diagram of the control circuits for the character selection plates of the DD CRT. Binary levels applied to the character selection decoder are converted into corresponding analog voltages. These analog voltages are power-amplified by the analog line drivers and fed through the control networks to the selection plates. As with the SD CRT, the horizontal and vertical deflection voltages are applied to the vertical and horizontal plates, respectively. This is due to the mounting of the character-forming matrix (rotated 90 degrees clockwise viewed from the front) in a position to compensate for convergence coil rotation of the electron beam.

4.1.2.3 Electron Beam Convergence

The DD CRT convergence coil is identical in operation to the convergence coil in the SD CRT's. Refer to paragraph 2.2.1.4 of Chapter 2 for the detailed convergence coil function. Figure 2–32 is the block diagram of the DD CRT convergence coil control circuits. The trim coil current is controlled by a single potentiometer connected in parallel across the trim coil proper. This method of connection differs from the trim coil circuit in the SD CRT (fig. 2–18). However, the absence of vectors in DD messages permits this method of control. The point of convergence in the DD CRT corrects for selection beams of a relatively large cross-sectional area (compared to electron beams employed in vector generation) and is adjustable to the same precise limits as in the SD CRT. The trim coils, as well, have a degree of control precision of rotation and point of convergence comparable to the SD CRT's. The high-voltage units and convergence current regulators serve the same functions as their counterparts in the SD CRT control circuits.

4.1.2.4 Electron Beam Compensation

The character compensation plates electrostatically compensate for the deflection given the electron beam by the character selection plates. This compensation or neutralization of selection-plate effect results in the beam being made coincident with the longitudinal axis of the DD CRT.

Figure 2–33 is a block diagram of the character compensation circuits. Analog voltages derived from the character selection decoder are applied through the centering and amplitude controls to the compensation plates. The 180-degree reversal of selection voltages in each axis when applied to the selection makes the beam coincident with the tube axis.

4.1.2.5 Character Message Deflection

The DD CRT also employs electrostatic deflection for character positioning within the message format. A typical DD message is illustrated in figure 2–26. Counting circuits provide the necessary binary levels to shift the electron beam to each successive character position in a row and to each new line. The precise positioning of messages on a specific portion of the screen is not a requirement for digital display. Therefore, the complex magnetic deflection network of the SD CRT was not used.

Figure 2–34 is the block diagram of the special circuits which supply the analog control voltages to the character-deflection plates. Binary levels applied to the character position decoders are converted to corresponding centering and amplitude controls.

4.1.2.6 Flood Gun

The flood gun is essentially an electron gun specifically designed to supply the storage element with a consistent source of low-velocity electrons. This is necessary because ordinarily the short persistence time of the phosphors does not permit a character to be displayed for a prolonged period of time. The flood gun is a source for a continuous flood of electrons which maintains each successive selected character at uniform intensity during the complete DD message presentation. Without the flood gun, each character would be displayed for the duration of phosphor persistence only and then would quickly fade away.

Functionally, the flood gun is the same as the main electron gun of the DD CRT. The gun consists of a heater cathode control grid and an accelerating anode.

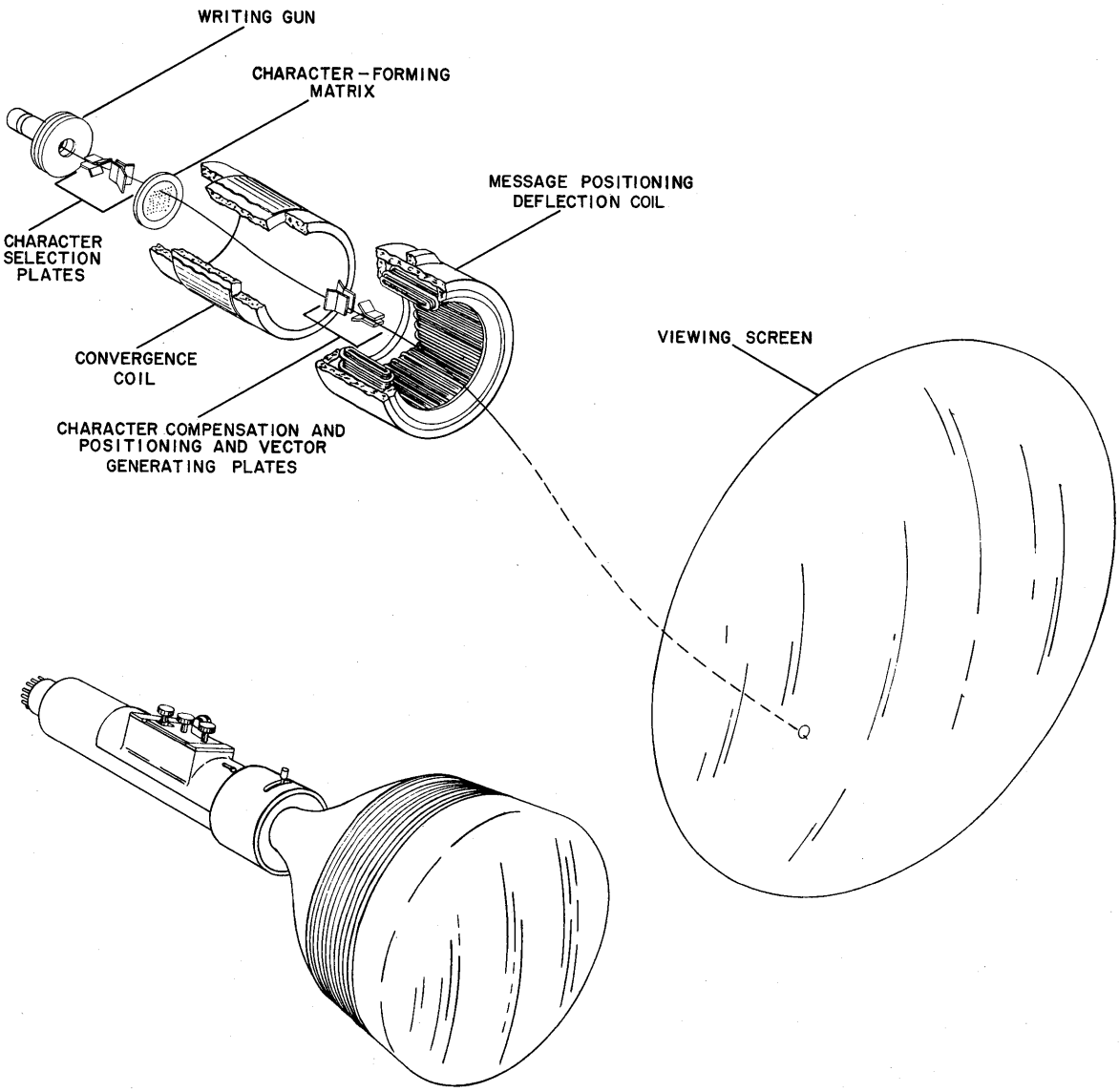


Figure 2–29. SD Cathode-Ray Tube

Figure 2–35 is a block diagram of the circuits associated with the storage element. The voltages for the flood gun are supplied by the model B high-voltage unit. The heater is supplied with 6.3Vac. The cathode voltage of —150V is returned to one side of the heater. The control grid is biased into conduction so that a continuous flow of electrons is supplied to and directed at the storage mesh. The accelerating anode is maintained at +45V. The total accelerating potential would thus be 200V. Compared with the 3,200V used to accelerate the main electron-gun beam, the flood gun can be considered a low-velocity electron emitter.

4.1.2.7 Collector Mesh

The collector mesh is a fine metallic screen which serves as the collector for secondary emission electrons from the storage mesh. The collector mesh potential is adjusted by the collector mesh level adjust potentiometer. This level is adjusted to provide the maximum collection of secondary emission electrons compatible with the passage of flood gun electrons. To increase this collection function, a positive contrast gate is applied to the collector mesh simultaneously with the impact of the high-velocity electron beam on the storage mesh. To erase the message, an erase gate (negative voltage) is applied to the collector and storage mesh. This gate places the collector at a lower potential than the flood gun anode. Low-velocity flood gun electrons are repelled by the collector mesh, interrupting the flood of electrons through the storage mesh to the phosphors. The short time of persistence of the phosphors causes the image to disappear instantaneously.

4.1.2.8 Storage Mesh

The storage mesh is fine metallic film-coated grid. This film has the property of high electron emission when bombarded by high-velocity electrons. Thus, when the high-velocity character-shaped beam impinges on the storage mesh, electrons are emitted by the film. As a result, the storage mesh acquires a positive charge at those points on the mesh where electrons have been emitted, producing a positive charged area in the shape of the character. Low-velocity electrons from the flood gun are attracted through this area to the phosphor, causing an image of the character to appear on the viewing screen. As long as this character-shaped area remains positively charged, flood gun-emitted electrons will maintain an image of the character on the face of the tube.

The storage mesh potential is set by the storage mesh level adjustment potentiometer (fig. 2–35). The mesh level control network holds the storage mesh at a more negative potential than the collector mesh to prevent the return of emitted electrons to the storage mesh. When the negative erase gate is applied to the collector and storage mesh, the positively charged areas attract electrons and become neutralized.

4.1.2.9 Ion Repeller Mesh

The ion repeller mesh deflects positively charged ions to the dag coating on the inner surface of the DD CRT. The bombardment of the phosphers by the high-velocity electrons generates these positively charged ions. The dag coating is maintained at ground potential and therefore attracts these positively charged particles.

TABLE 2–2. DD CRT FUNCTIONAL REQUIREMENTS AND ASSOCIATED TUBE ELEMENTS

FUNCTIONAL REQUIREMENTS	DD CRT ELEMENT
Generate electron beam. Blank or unblank the beam.	Electron gun
Aim beam at a character.	Character selection plates
Form beam in shape of character.	Matrix
Make electron beam intersect the tube axis. (Beam spirals through 90 degrees in transit.)	Convergence coil
Cancel deflection applied by selection plates. Make beam coincident with tube axis.	Character compensation plates
Position character-formed beam in the required position in message format.	Character deflection plates
Display or erase message:	Storage element
a. Generate cone of low velocity electrons.	a. Flood gun
b. Store character.	b. Storage mesh
c. Intensify message (contrast gate) erase.	c. Storage mesh
d. Erase message (erase gate or manual).	d. Storage mesh
Deflect positive ions.	Ion repeller mesh
Collect secondary emission electrons.	Collector mesh

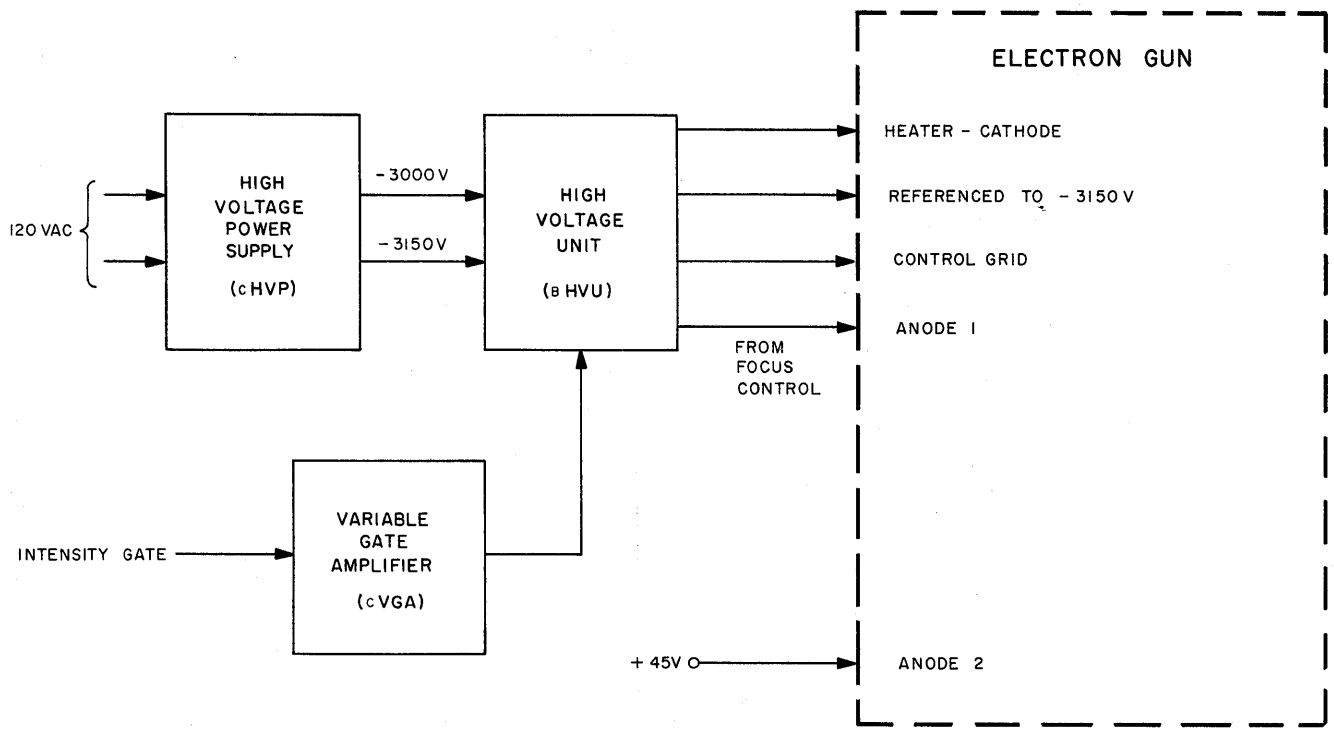


Figure 2–30. Electron Gun Control and Supply Circuits, Block Diagram

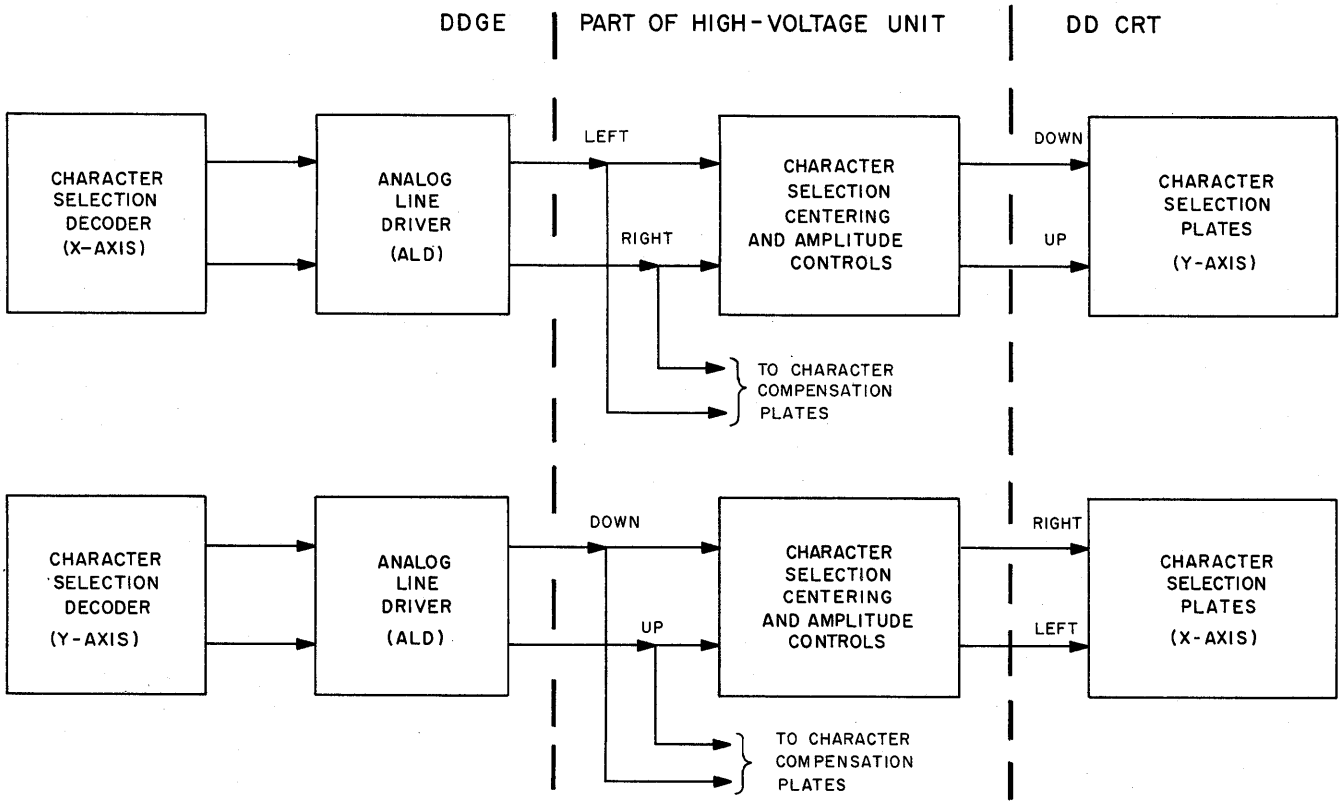


Figure 2–31. Character Selection Plates and Associated Circuits, Block Diagram

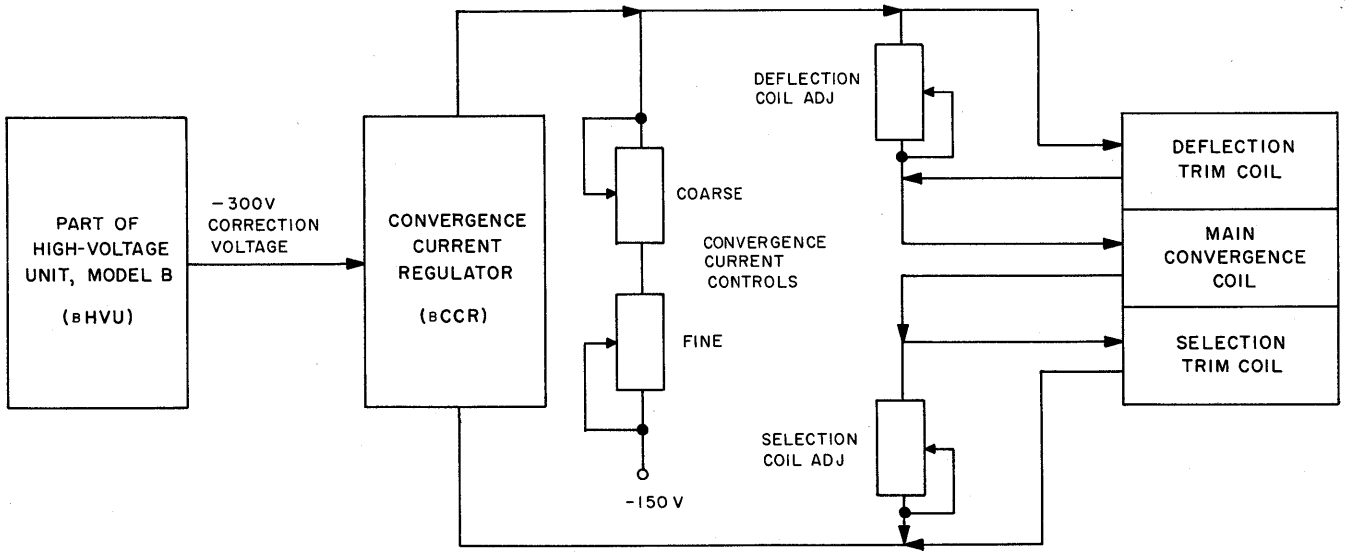


Figure 2–32. Convergence Coil Assembly and Associated Circuits, Block Diagram

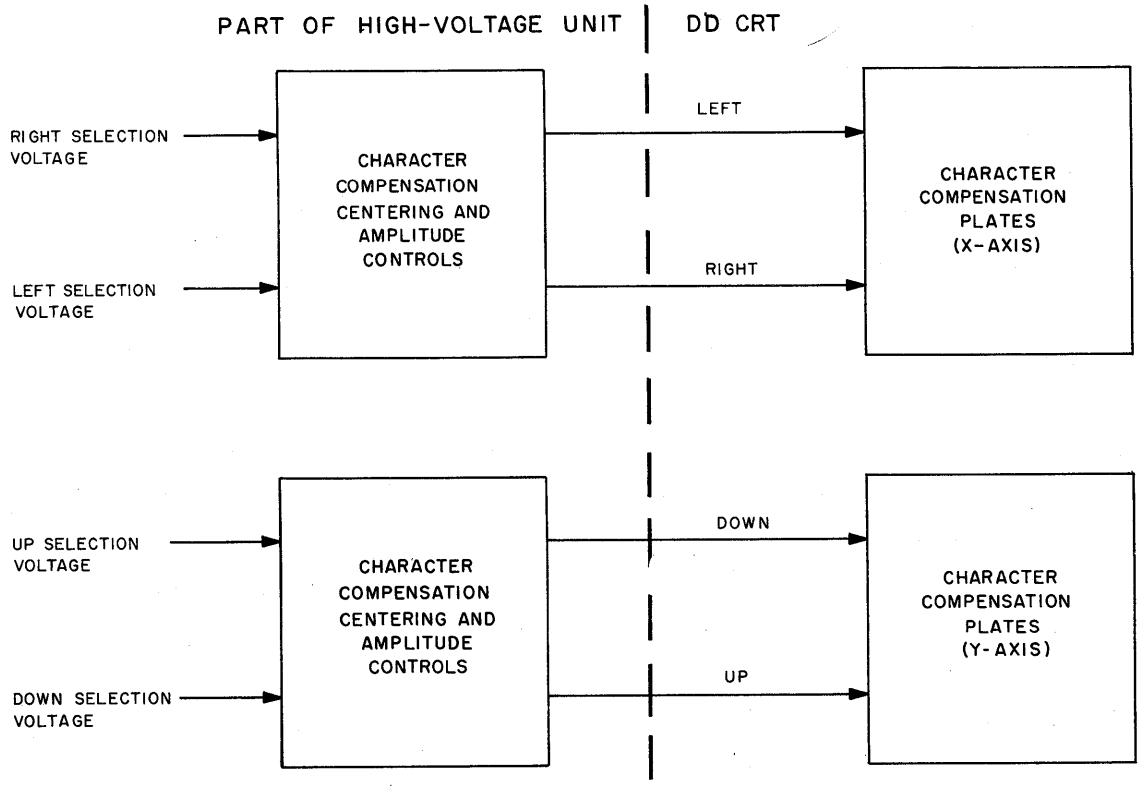


Figure 2–33. Character Compensation Plates and Associated Circuits, Block Diagram

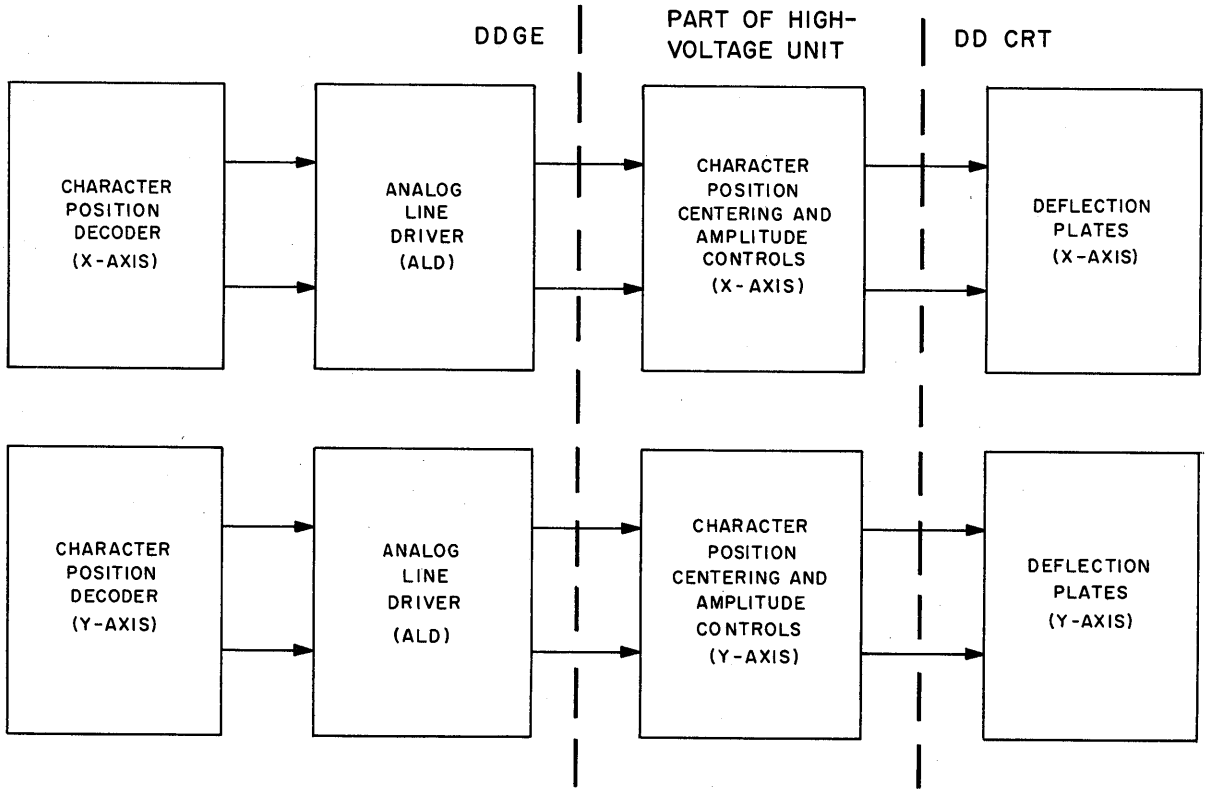


Figure 2–34. Character Deflection Plates and Associated Circuits, Block Diagram

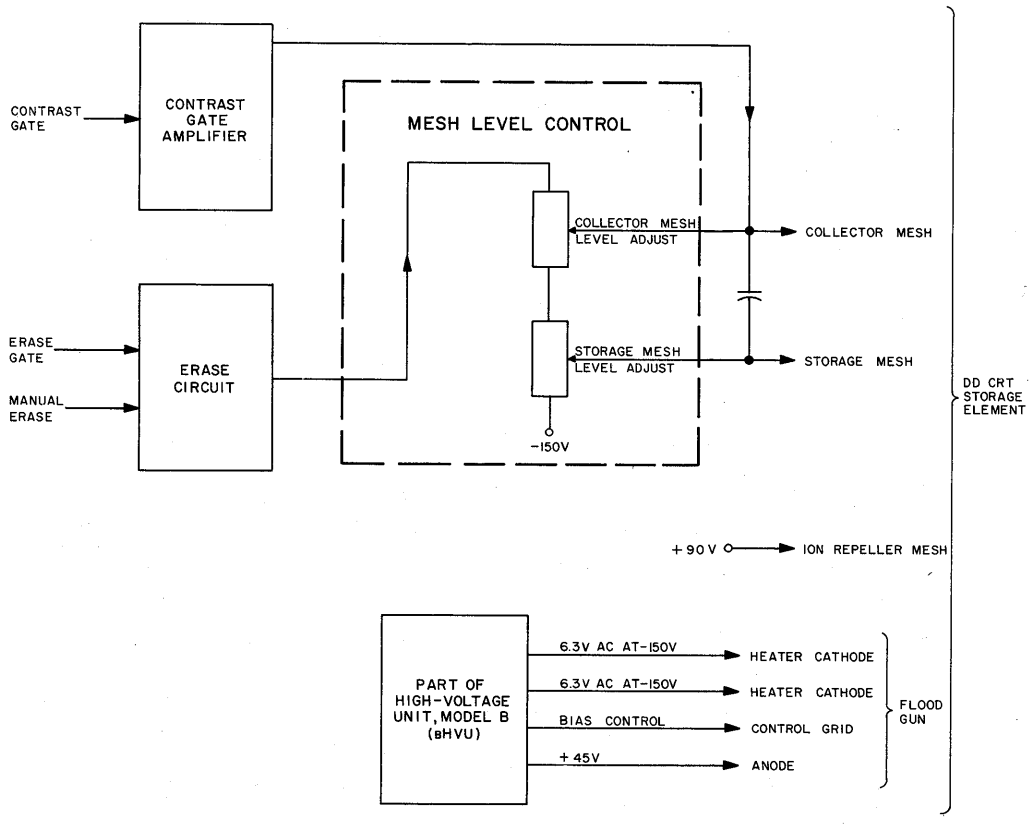


Figure 2–35. Storage Element and Associated Circuits, Block Diagram

PART 3
DIGITAL DISPLAY ELEMENTS

CHAPTER 1
INTRODUCTION TO DIGITAL DISPLAY ELEMENTS

1.1 GENERAL

Information compiled by the Central Computer System of AN/FSQ-7 and -8 Combat Direction and Combat Control Centrals for presentation by the Display System is divided into two main classifications: situation display (SD) data and digital display (DD) data. Part 4 of this manual describes the theory of operation of the SD elements, while this part describes the DD elements.

Digital display data, which is supplemental to SD data, is presented on the 5-inch CRT and appears in a tabular array of characters consisting of letters, numerals, and special symbols. Unlike the situation display, which is automatically renewed every 2-⅔ seconds, the digital display changes only when the Central Computer System initiates a new display. Therefore, in the absence of instructions from the Central Computer, information displayed on the DD CRT may be retained on the viewing screen indefinitely. The basic difference, then, between the situation display and the digital display is that the DD CRT stores messages until the display is deliberately erased.

1.2 PURPOSE OF DIGITAL DISPLAY ELEMENTS

The DD elements of the Display System are the digital display generator element (DDGE), the digital display indicator element (DDIE), and the equipment on the OD side of the DD field of the MIXD drum. The DDGE receives DD messages from the Drum System and the Central Computer System via the DD field of the MIXD drum. It processes these messages for visual display in the DDIE by converting the DD message bits into the analog voltages and control signals required by a DDIE console to display messages on the viewing screen.

The data displayed by the DDIE is of a type that is supplemental to the displays presented on the SD CRT and includes such information as the availability of defense groups, weather conditions, and similar slow-changing information.

1.3 TYPE OF DISPLAY

Digital information on the DD CRT is displayed as indicated in figure 3–1. Five characters per row in two columns (16 rows per column) can be represented in the format of a complete DD message. The characters, L, K, J, I, and H in each row are not physically displayed and are arbitrarily assigned for purposes of identification only. The subscript indicates the row in which the character is positioned. The character display sequence for the group at the left is right to left and top to bottom. When all the required characters have been written in the group at the left, the other group may be written. A DD message may consist of a minimum of four and a maximum of 32 words. Figure 3–2 illustrates a typical DD display.

Digital display units are divided functionally into two sections: DD 1 and DD 2. This division permits one section to display new information without affecting the original information in the other group. At the present time, all DDIE's are assigned to DD 1, with DD 2 unassigned. Display sections DD 1 and DD 2 are activated by the Central Computer *Operate* instructions *PER 35* and *PER 36,* respectively.

1.4 MIXD DRUM OPERATION

Information to be displayed by the DD elements of the Display System is sent from the Central Com-

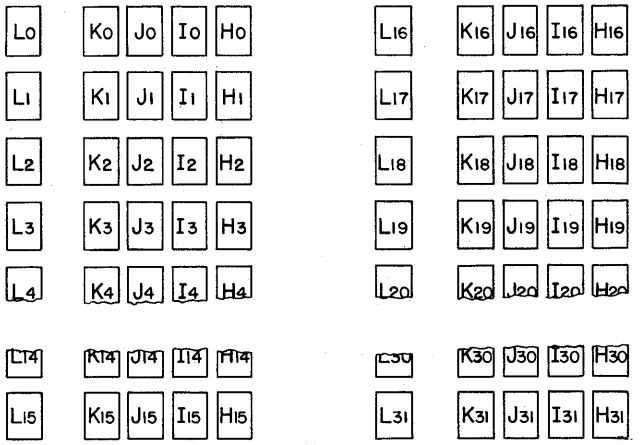


Figure 3–1. DD Message Format

puter to the DDGE via the DD field of the MIXD drum. Each 32-bit binary word from the computer is stored magnetically in one of the 2,048 registers of the DD field and is later transmitted to the DD elements to provide the information required in displaying the five characters of one row. Since the DD elements cannot accept information from the Central Computer at the frequency with which these words are stored (one every 10 μsec), the drum must also function as a buffer device; that is, slow down the readout of words to a rate acceptable to the DDGE (one word every 640 μsec). The pattern in which the messages are stored on the drum allows the DD elements to receive the words in their proper sequence, since the words are read by a process called interleaving. Interleaving is the skipping of a predetermined number of registers between each register or group of registers read. The DD field is read by an interleave pattern of 64; that is, the field is read in a pattern of skip 63 registers, read one. This method of reading the drum makes words available at a 640-μsec rate and requires 64 revolutions of the MIXD drum to completely read the DD field.

1.4.1 Timing and Control Signals

The signals produced by the MIXD drum to synchronize the operations of the drum and the DDGE are the timing and control signals. The OD pulses (so named because they are employed on the OD side of the drum) that appear at the DDGE are OD 1 and OD 3 pulses. These pulses are received alternately at 5-μsec intervals and recur every 10 μsec. For example,

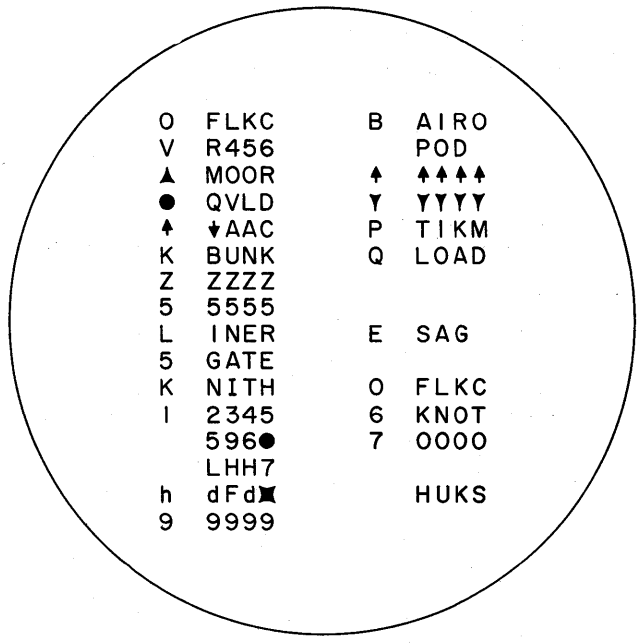


Figure 3–2. Typical Digital Display

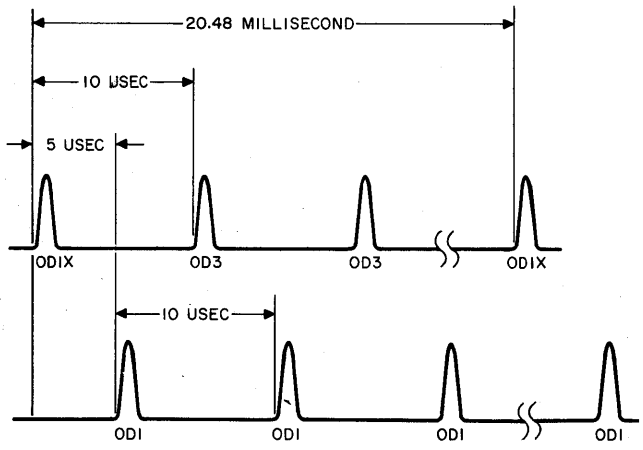


Figure 3–3. Drum Timing Pulses

an OD 3 pulse (fig. 3–3) follows the first OD 1 pulse by 5 μsec and, following the OD 3 pulse by 5 μsec is the second OD 1 pulse. Every 20.48 ms, or once every revolution of the drum, the DDGE receives an OD index (OD IX) pulse which is used both for reference and for timing. Also generated in the Drum System are read-sample pulses which occur simultaneously with the reading of every drum word.

1.4.2 Information Signals

Drum words received by the DDGE are 32-bit binary words previously stored on the DD field by the Central Computer. These words, received by the DDGE at intervals of 640 μsec, designate the characters to be displayed by the DD elements. In addition, the two sign bit positions in the drum word are used to control a portion of the operations in the generator elements. The coding and function of the sign bit positions are shown in figure 3–4.

1.5 MESSAGE FORMAT

Figure 3–4 also shows the message format of a digital data message. Each word controls the display of one row of five characters on a DD CRT. The x selection co-ordinates are contained in bits L1 through L15; the y selection co-ordinates are contained in bits R1 through R15. Six bits are used to select each character, three bits for x and three bits for y. The x and y co-ordinates vary the deflection voltages used in selecting a desired character from the DD tube character matrix.

1.6 DD SEQUENCE OF OPERATION

To better evaluate the nature and type of input information to the DD elements, an examination of a complete cycle of the digital display will be considered. A display cycle may be defined as the time interval between the start of one DD 1 or DD 2 cycles and the start of the next. The display cycle is divided into four periods: the

WORD	BIT POSITIONS																												
	LS	LI	L2	L3	L4	L5	L6	L7	L8	L9	LI0	LI1	LI2	LI3	LI4	LI5	RS	RI	R2	R3	R4	R5	R6	R7	R8	R9	RI0	RI1	RI2	RI3	RI4	RI5
0	*	L0			K0			J0			I0			H0			*	L0			K0			J0			I0			H0		
	①	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	②	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$
1	*	L1			K1			J1			I1			H1			*	L1			K1			J1			I1			H1		
	①	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	②	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$
2	*	L2			K2			J2			I2			H2			*	L2			K2			J2			I2			H2		
	①	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	②	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$
3	*	L3			K3			J3			I3			H3			*	L3			K3			J3			I3			H3		
	①	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	②	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$
4	*	L4			K4			J4			I4			H4			*	L4			K4			J4			I4			H4		
	①	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	②	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$
30	*	L30			K30			J30			I30			H30			*	L30			K30			J30			I30			H30		
	①	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	②	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$
31	*	L31			K31			J31			I31			H31			*	L31			K31			J31			I31			H31		
	①	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	②	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$

NOTE:
*INDICATES CONTROL BIT, AS FOLLOWS:

NAME	POSITION AND CONTENT		MEANING
	① LS	② RS	
CONTINUE	0	0	DISPLAY WORD ON FOLLOWING LINE OF SAME COLUMN
NEW SLOT	0	1	DISPLAY WORD ON TOP LINE OF LEFT COLUMN. INCREASE SLOT COUNTER BY ONE
OTHER HALF	1	0	DISPLAY WORD ON TOP LINE OF OPPOSITE COLUMN
SKIP LINE	1	1	DISPLAY WORD TWO LINES BELOW IN SAME COLUMN

Figure 3–4. DD Message, Drum Format

initial period, the display period, the retention period, and the erase period.

1.6.1 Initial Period

During the initial period, the DDGE synchronizes with drum operation, erases some of the previously written information within the digital display indicator sections (DDIS's), and clears and/or presets some of the DDGE circuits. The initial period of a DD cycle is further subdivided into three phases: the synchronization, the delay, and the display phases.

1.6.1.1 Synchronization Phase

When a new display cycle has been programmed by the Central Computer, an initiate-DD pulse, which readies the DDGE to accept information from the DD field, is fed from the CC to the DDGE.

1.6.1.2 Delay Phase

During the delay phase, an initial erase gate is generated which erases the digital display assigned to the first 14 indicator sections (slots). After the messages from the previous cycle have been erased, the DDIE is ready to accept new messages from the Drum System through the DDGE. The remaining DDIS's are erased successively, but not always in single sequence; two or more may be selected, and the other is determined by the slot counter.

1.6.1.3 Display Phase

A start-DD-read signal is sent from the generator element to the Drum System to indicate that the DDGE is ready to accept display information. This marks the beginning of the display phase. The display phase ends when the first word is received from the DD field.

1.6.2 Display Period

The display period of the cycle begins with the receipt of a read-sample pulse from the Drum System. The read-sample pulse is received at the same time as the first 32-bit information signals. Within the DDGE, the read-sample pulse is called a load-DD signal, since its function is to indicate to the element that a word of digital data is being received. Each word contains first, the control and information bits necessary to select the proper character and second, the positioning bits required to position the word in the message format. A word requires 640 μsec to be displayed. The maximum time necessary to display a complete message (or slot) is, therefore, 640 μsec/word x 32 words/message or 20.48 ms. After the last slot has been displayed, the DDGE remains inactive until the next initiate-DD pulse readies the DDGE to receive new information from the Drum System.

1.6.3 Retention Period

All messages remain displayed during the retention period until erasure takes place during the succeeding cycle. Since DD 1 and DD 2 cycles function independently, retention in one section is possible while messages are displayed in the other section. During the retention period, new information can be written on the DD field to be displayed at a later time.

1.6.4 Erase Period

Before writing a new display on the DD CRT, the old information must be destroyed. This destruction is accomplished with the erase gate generated by the timing and control circuitry. The DDIS's to be erased are selected by the slot lines in a manner similar to that in which they are selected for intensification.

CHAPTER 2
DIGITAL DISPLAY INDICATOR ELEMENT

2.1 GENERAL

The DDIE is part of the AN/FSQ-7 & -8 and, along with the situation display indicator element (SDIE), presents information from the Central Computer System to the operators responsible for its disposition. The information to be displayed is, as is also the case with the situation display, integrated and processed by the Central Computer as programmed by operator personnel. The resulting information is conducted to the display generating element for further processing and is then written on specially designed cathode-ray tubes for the digital display.

The DDIS's comprise the DDIE. (See fig. 3–5.) Each DDIS contains a 5-inch CRT with its associated circuits and is designated as variable simplex equipment. This breakdown makes the DDIS provisional equipment which may be assigned to auxiliary, situation display, Command Post, and duplex switching consoles.

2.2 INFORMATION FLOW TO DDIE

Signal voltages required by the DDIE are supplied by the DDGE through the distribution element. Junction boxes are used to make all information signals available to all consoles. Specific indicator selection signals are distributed only to the consoles that require them. The signals required by each DDIS are given below:

a. Four lines — analog character selection voltage (also used in the DDIS for character compensation).

b. Four lines — analog character-positioning (deflection) voltage.

c. Three lines — an erase gate and two erase-selection signals which precede the message to be displayed by 200 ms. The two selection signals are slot lines corresponding to the erase slot number assigned to the DDIS.

d. Three lines — an intensity gate and two intensification-selection signals which accompany each character being displayed. The two selection signals are slot lines corresponding to the display slot number assigned to the DDIS.

e. One line — a contrast gate which occurs periodically about once each word to improve the legibility of characters displayed previously.

f. Four lines — two test-erase and two test-intensity-selection signals which are used to display the DD test pattern.

2.3 DIGITAL DISPLAY INDICATOR SECTION

Because the DDIS units, with minor exceptions, are all alike, the theory of operation given here is applicable to all models of the DDIS. Figure 3–6 is a simplified flow diagram of the DDIS and shows six major blocks: the unit status switch, DD signal switching relays, the DD intensification and erasure unit, the high-voltage unit, the high-voltage power supply, and the 5-inch DD CRT.

Each DDIS is supplied with two complete sets of information and control signals from the duplexed

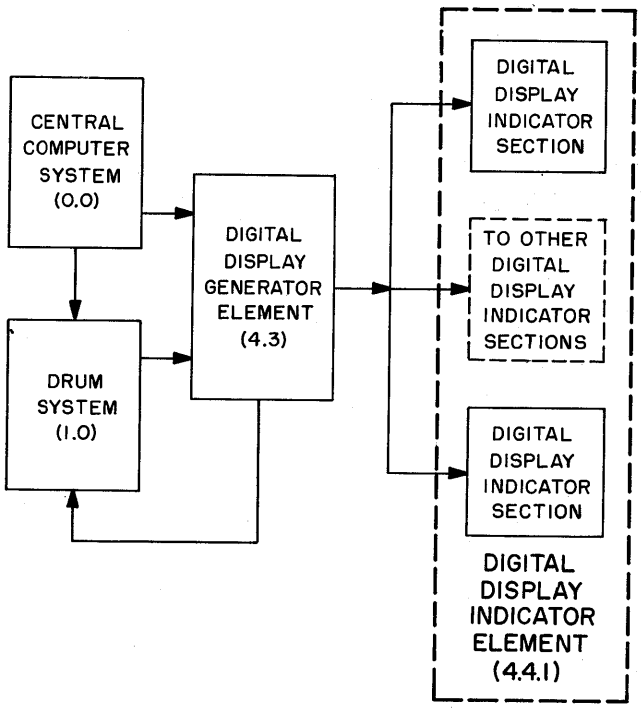


Figure 3–5. DDIS Relationship to Display System Elements

DDGE, where the signals are generated. At any given instant, one of the two DDGE's is in active status and the other is in standby status. A pair of corresponding signals, one from the active DDGE and one from the standby DDGE, is applied to two pairs of switching relays (see fig. 3–7, sheet 1, foldout). The relays are operated by the UNIT STATUS switch, which determines whether computer A signals or computer B signals are to be displayed. From the switching relays, the analog voltages for character selection and deflection are applied to the high-voltage unit. All other selected signals are applied to the DD intensification and erasure circuit (see fig. 3–7, sheet 2, foldout). Note that the switching relays provide a dummy load resistor for each pair of push-pull analog voltages that are not being used in the DDIS. For example, signals DD ± y are applied across resistor R111 when they are not required for display. The function of each circuit is discussed in this section. For a more complete analysis of the circuits used in the Display System, refer to manual 3-3-0, *Special Circuits for AN/FSQ-7 Combat Direction Central and AN/FSQ-8, Combat Control Central.*

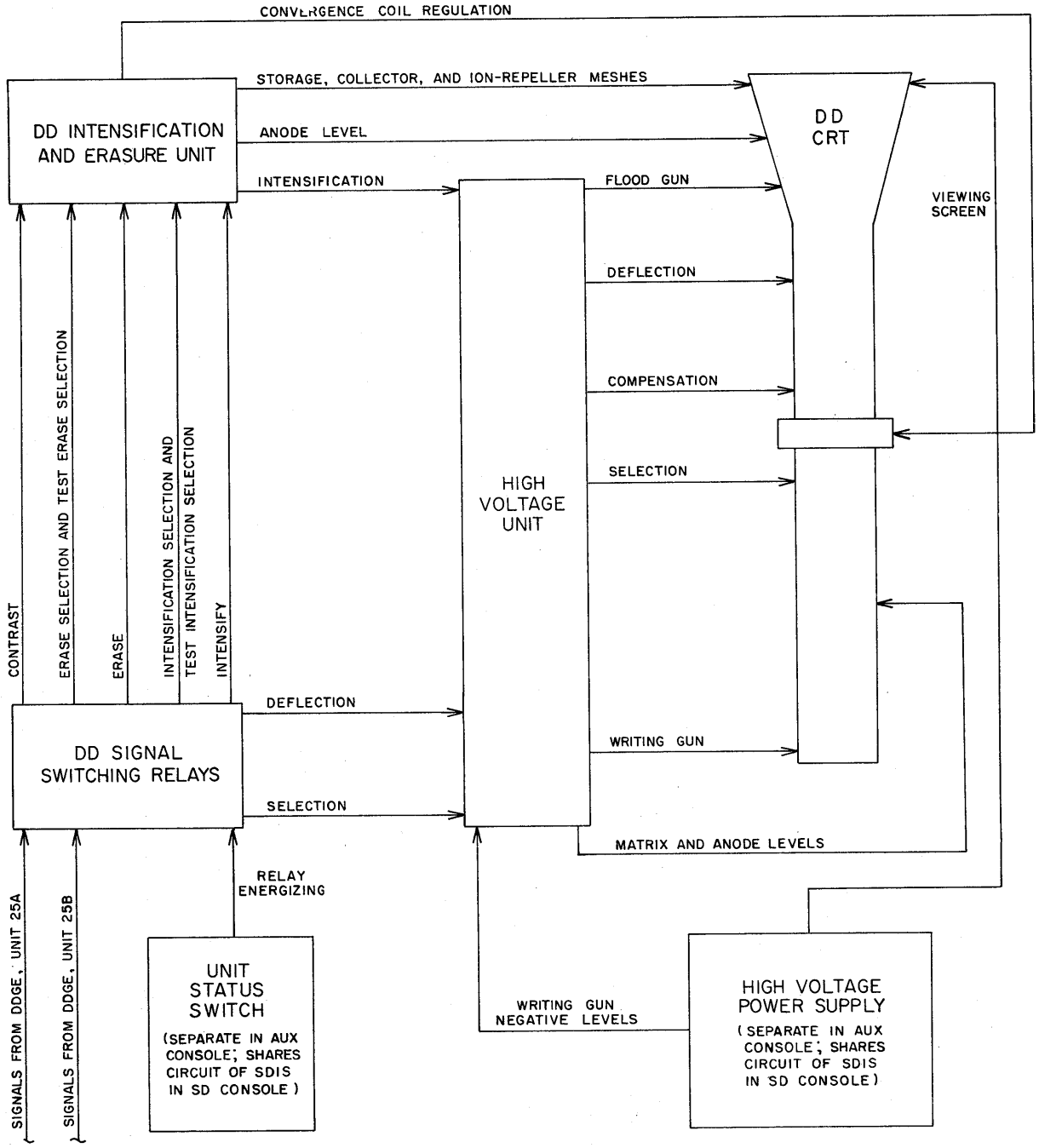


Figure 3–6. DD Indicator Section, Simplified Flow Diagram

2.3.1 Unit Status Switch and Signal Switching Relays

The position of the UNIT STATUS switch determines whether signals from the active DDGE or the standby DDGE are to be used in the DDIS. For active or standby operation, the UNIT STATUS switch energizes switching relays which admit signals from the designated machine. For example, if the switch is set to ACT, signals from the active machine (whether A or B) are admitted to the console. Since active and standby signals are available to all simplex consoles at all times, the selection of signals to be displayed is at the discretion of the console operator.

All active simplex units receive power from either power supply C or power supply D, whichever is designated active at the duplex switching console. The standby simplex units (which receive power, but no signals) are supplied by the power supply designated standby. The UNIT STATUS switch, therefore, also controls the relays which switch in power from the appropriate (C or D) power supply. For a more detailed discussion of the UNIT STATUS switch, refer to Part 5, Chapter 8, Section 1.

2.3.2 Intensification and Erasure Circuit

In order to display the character selected by the character-selection signals, the DD CRT must first be unblanked. The tube is unblanked (made to conduct) when sufficient voltage has been applied to the control grid to permit electron flow. Upon receipt of intensity-gate and intensity-selection signals, the intensification and erasure unit generates the proper intensification level to the high-voltage unit. The high-voltage unit then applies an unblanking pulse to the writing gun.

The intensification signal, which usually recurs every 120 μsec, is generated by the timing and control section of the DDGE. Two leads from the slot counter are wired to each DDIS to control intensification, and two leads are wired to each DDIS for erasure.

The erase operation occurs approximately 200 ms before a new message is written. This is accomplished by applying simultaneously an erase signal and voltages from the slot counter to the intensification and erasure unit. The process is identical to the selection of a console for intensification. When the three signals occur simultaneously at the erase circuit, a negative voltage is applied to the collector grid of the DD CRT and the viewing screen is erased.

2.3.2.1 Normal Intensification Selection

Normal selection of a DDIS for intensification requires the coincidence of the proper slot counter output and the intensity-gate signal. Since an intensity gate is provided for each character of every message, the DDIS to be intensified is determined mainly by the slot counter. Coincidence takes place in an AND circuit when the DD TEST PATTERN switch (S49) is in the NORMAL position. The output of the AND is applied to the variable-gate amplifier; hence, through the high-voltage unit to the control grid of the DD CRT.

In each DDIS, the slot-line signals that correspond to the assigned slot are the intensification-selection-A and the intensification-selection-B signals. The correlation between A and B slot-line assignments for intensification and erasure is shown in table 3–1.

2.3.2.2 Intensification in Test 1

When the DD TEST PATTERN switch (S49) is placed in the TEST 1 position, the A and B slot-line signals are replaced by corresponding test slot-line signals. Coincident gating of these test signals intensifies the DDIS's selected to receive the test slot. The test pattern display is used primarily for maintenance.

2.3.2.3 Intensification in Test 2

Placing the DD TEST PATTERN switch in the TEST 2 position allows all DD messages to be intensified. Both the A and B slot-line signals are replaced by +10V levels. The intensification AND, therefore, permits unblanking of the DD CRT upon receipt of the intensity gate.

2.3.2.4 Normal Erase Selection

The coincidence of two erase-selection signals with the erase gate from the DDGE produces erasure. (This condition exists at the same time that another DDIS is being intensified.) For example, when the slot counter number is equal to 12 (table 3–1) and the DDIS assigned to this slot is being intensified, erase-selection signals are being routed from the slot counter to another DDIS. The DDIS being erased, in this case, would be the one assigned to slot 25.

When the DD TEST PATTERN switch is placed in the NORMAL position, erase-selection signals from the appropriate slot lines are fed to the mesh level control and erasure unit. Each DDIS is assigned a pair of slot lines for erase selection on the basis of:

a. The assigned display slot.
b. The duration of the slot immediately preceding the display slot, depending upon the number of registers assigned to each slot.

2.3.2.5 Erasure in Test 1

Placing the DD TEST PATTERN switch in the TEST 1 position replaces the erase-selection-A and erase-selection-B signals with the test signals dictated by the test slot. Erasure of the CRT occurs approximately 200 ms before the test pattern is displayed.

2.3.2.6 Erasure in Test 2

With the DD TEST PATTERN switch in the TEST 2 position, the erase-selection-A and erase-selection-B signals are replaced by +10V levels. As a result, erasure

takes place every time the erase gate is received from the DDGE.

2.3.3 High-Voltage Unit

The high-voltage (HV) unit receives information signals (character selection and positioning analog voltages), the intensification gate (from the intensification and erasure circuit), and high d-c voltages (from the high-voltage power supply). The unit derives compensation analog voltages from the character selection voltages. It contains amplitude and centering controls for the three groups of analog voltages and a limiting circuit for the intensification gate. The HV unit also generates and adjusts d-c levels which are applied to the matrix and to anode 1. For a more detailed analysis of the HV unit, refer to the special circuits manual, 3-3-0.

2.3.4 High-Voltage Power Supply

The high-voltage power supply (HVP) is a nonlogic circuit that provides accelerating potentials for the DD and SD CRT's. In an SD console, the voltages for the DD CRT are supplied by the power supply of the SDIS. For a more detailed discussion of the various types of HVP's, refer to the special circuits manual, 3-3-0.

TABLE 3–1. SLOT LINES FOR INTENSIFICATION AND ERASE SELECTION, AN/FSQ-7

SLOT LINES		SLOT NUMBER	
A	B	INTENSIFICATION	ERASURE
0	000	0	1–14
1	000	1	15
2	000	2	16
3	000	3	17
4	000	4	
5	000	5	18
6	000	6	19
7	000	7	20
8	000	8	21
9	000	9	22
10	000	10	23
11	000	11	24
12	000	12	25
13	000	13	26
14	000	14	27

TABLE 3–1. SLOT LINES FOR INTENSIFICATION AND ERASE SELECTION, AN/FSQ-7 (cont'd)

SLOT LINES		SLOT NUMBER	
A	B	INTENSIFICATION	ERASURE
15	000	15	28
0	100	16	29
1	100	17	30
2	100	18	31
3	100	19	32
4	100	20	33
5	100	21	34
6	100	22	35
7	100	23	36
8	100	24	37
9	100	25	38
10	100	26	39
11	100	27	40
12	100	28	41
13	100	29	42
14	100	30	43
15	100	31	44
0	200	32	45, 46
1	200	33	47, 48, 49
2	200	34	50, 51, 52
3	200	35	53, 54
4	200	36	55, 56
5	200	37	57, 58
6	200	38	59, 60
7	200	39	61, 62
8	200	40	63, 64, 65
9	200	41	66, 67
10	200	42	68, 69
11	200	43	70, 71
12	200	44	
13	200	45	72
14	200	46	73, 74

TABLE 3–1. SLOT LINES FOR INTENSIFICATION AND ERASE SELECTION, AN/FSQ-7 (cont'd)

SLOT LINES		SLOT NUMBER	
A	B	INTENSI-FICATION	ERASURE
15	200	47	75
0	300	48	76
1	300	49	77
2	300	50	
3	300	51	
4	300	52	78
5	300	53	
6	300	54	79
7	300	55	
8	300	56	
9	300	57	80
10	300	58	
11	300	59	81
12	300	60	
13	300	61	82
14	300	62	
15	300	63	83
0	400	64	
1	400	65	84
2	400	66	
3	400	67	85
4	400	68	
5	400	69	
6	400	70	86
7	400	71	87
8	400	72	
9	400	73	88
10	400	74	
11	400	75	
12	400	76	
13	400	77	89, 90
14	400	78	91

TABLE 3–1. SLOT LINES FOR INTENSIFICATION AND ERASE SELECTION, AN/FSQ-7 (cont'd)

SLOT LINES		SLOT NUMBER	
A	B	INTENSI-FICATION	ERASURE
15	400	79	92
0	500	80	93
1	500	81	94
2	500	82	95
3	500	83	96
4	500	84	97
5	500	85	98
6	500	86	99, 100
7	500	87	101, 102, 103
8	500	88	104, 105
9	500	89	
10	500	90	
11	500	91	
12	500	92	
13	500	93	
14	500	94	
15	500	95	
0	600	96	
1	600	97	
2	600	98	
3	600	99	
4	600	100	
5	600	101	
6	600	102	
7	600	103	
8	600	104	
9	600	105	
10	600	106	
Used for DDGE timing and initial erase of group 2		107	
Group DD 2 not assigned		108–127	

2.3.5 DD Cathode-Ray Tube

The 5-inch DD CRT displays the information processed by the DD elements. Since the visual presentation on the viewing screen is a function of analog voltages, the DD CRT serves as a transducing readout element. The DD CRT has a character-forming matrix that shapes the diffused electron beam into the form of the characters stenciled in the matrix. A flood gun is used in the storage element to maintain a continuous display. The console operator has the option of erasing the DD presentation on the viewing screen by depressing the ERASE pushbutton located on the front panel on the DD unit. A more detailed discussion of this tube has already been given in Part 2.

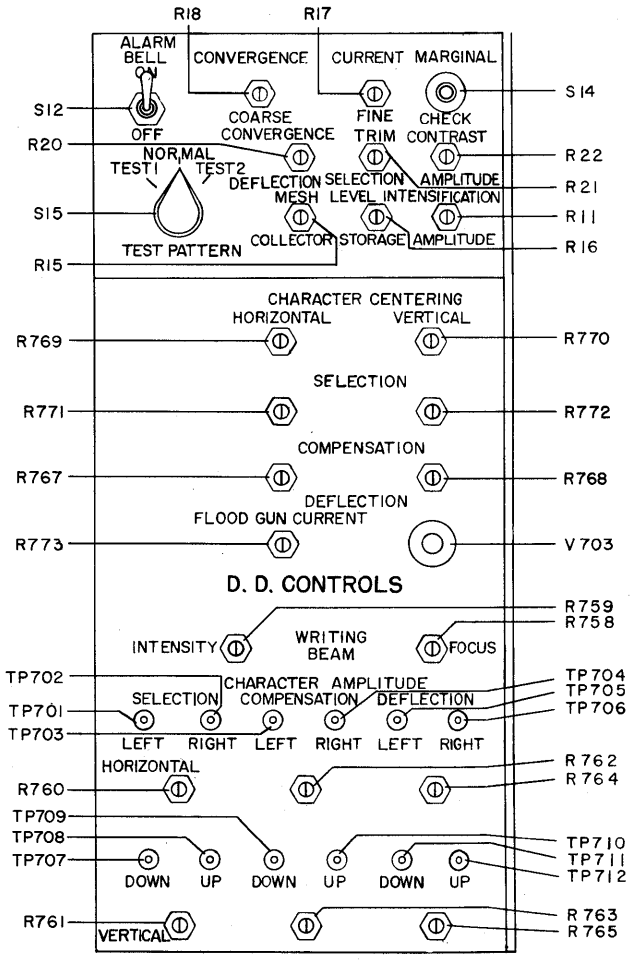


Figure 3–8. Auxiliary Console, Subpanel Controls

2.3.6 Convergence Current Regulator

The convergence current regulator, Model B (BCCR), is used to supply and regulate current to the convergence coil of the DD CRT. The magnetic field generated by the convergence coil is a magnetic lens that causes the character-shaped electron beam to converge along the longitudinal axis of the CRT at a common point. The convergence current regulator must automatically change the current amplitude through the convergence coil for changes in the —3,300-volt HV unit; hence, an increase in the accelerating voltage develops a proportional increase in the convergence coil current.

For a more detailed analysis of this current as well as other circuits used in the Display System, refer to the special circuits manual, 3-3-0.

2.3.7 Contrast Gate

The contrast gate is amplified in the intensification and erasure unit. The gate is superimposed on the d-c levels established by the unit for the collector and storage meshes. This contrast gate is provided to increase the image contrast ratio for improved perception. A more detailed analysis of this circuit, including its adjustments, is described in the special circuits manual, 3-3-0.

2.4 DDIS MARGINAL CHECKING

A DDIS has only one provision for marginal checking. Depressing the DD MARGINAL CHECK pushbutton (S55) decreases the plate voltage of the erasure unit and, therefore, indicates the marginal or lower limit of the circuit. Failure to erase properly with the marginal voltage applied is a notification to maintenance personnel to replace the erasure unit.

2.5 DDIS CONTROLS

The DDIS in an auxiliary console is similar to the DDIS in an SD console. In both consoles, only two controls (the ERASE pushbutton and the UNIT STATUS switch) are located on the front panel. The remaining DD controls are located on the console subpanel. Figure 3–8 shows the subpanel controls for the auxiliary console. Refer to figure 4–31 for the DDIS SD console subpanel controls. Table 3–2 lists all the controls for auxiliary and SD DDIS's with their function and logic circuit components.

TABLE 3–2. DIGITAL DISPLAY INDICATOR SECTION CONTROLS

CONTROL	FUNCTION	LOGIC CIRCUIT COMPONENT	
		SD CONSOLE	AUXILIARY CONSOLE
Front Panel Controls			
DD ERASE	Erase CRT display at any time	S26	S2
UNIT STATUS	Five positions:		
	AC: a-c power only	S29	S6
	PWR: a-c and d-c power only		
	STDBY: signals and power from standby system		
	OFF: no signals and power		
	ACT: signals and power from active system		
Subpanel Controls			
TEST PATTERN	Three positions:	S49	S15
	NORMAL: the message (slot) assigned to the DDIS is displayed		
	TEST 1: the DD test pattern is displayed		
	TEST 2: all slots are intensified and erased		
CONVERGENCE CURRENT			
COARSE	Orients writing beam	R18	R18
FINE	Adjusted to give upright characters	R21	R17
CONVERGENCE TRIM			
DEFLECTION	Fine adjustment of character registration	R19	R20
SELECTION	Used in conjunction with character deflection and character selection controls	R20	R21
MESH LEVEL			
COLLECTOR	Adjusts mesh levels for optimum (stable) storage of display	R22	R15
STORAGE	Adjusts mesh levels	R23	R16
MARGINAL CHECK	Used for marginal check of mesh level control and erasure unit	S55	S14
CONTRAST AMPLITUDE	Adjusts contrast gate amplitude	R24	R22
INTENSIFICATION AMPLITUDE	Adjusts signal level of intensification gate	R25	R11
CHARACTER CENTERING			
SELECTION			
HORIZONTAL	Adjusts the writing beam horizontally on matrix	R769	R769

TABLE 3–2. DIGITAL DISPLAY INDICATOR SECTION CONTROLS (cont'd)

CONTROL	FUNCTION	LOGIC CIRCUIT COMPONENT	
		SD CONSOLE	AUXILIARY CONSOLE
VERTICAL	Adjusts the writing beam vertically on matrix	R770	R770
COMPENSATION			
HORIZONTAL	Adjusts the writing beam horizontally on the viewing screen	R771	R771
VERTICAL	Adjusts the writing beam vertically on the viewing screen	R772	R772
DEFLECTION			
HORIZONTAL	Adjusts the writing beam horizontally on the viewing screen	R767	R767
VERTICAL	Adjusts the writing beam vertically on the viewing screen	R768	R768
FLOOD GUN CURRENT	Varies quantity of electrons to the storage mesh from flood gun	R773	R773
WRITING BEAM			
INTENSITY	Adjusts d-c (bias) level of intensification signal to determine the writing beam intensity	R759	R759
FOCUS	Adjusts focus of the writing beam	R758	R758
CHARACTER AMPLITUDE			
SELECTION			
HORIZONTAL	Adjusts amplitude of selection signal for proper character selection	R760	R760
VERTICAL	Adjusts amplitude of selection signal for proper character selection	R761	R761
COMPENSATION			
HORIZONTAL	Adjusts amplitude of compensation signals for optimum character registration	R762	R762
VERTICAL	Adjusts amplitude of compensation signals for optimum character registration	R763	R763
DEFLECTION			
HORIZONTAL	Adjusts amplitude of deflection signals for proper character deflection	R764	R764
VERTICAL	Adjusts amplitude of deflection signals for proper character deflection	R765	R765
Convergence Coil Mount Controls (Mechanical Adjustments of Coil Position)			

TABLE 3–2. DIGITAL DISPLAY INDICATOR SECTION CONTROLS (cont'd)

CONTROL	FUNCTION	LOGIC CIRCUIT COMPONENT	
		SD CONSOLE	AUXILIARY CONSOLE
YAW 	Controls beam movement on the viewing screen in the directions indicated		
VERTICAL			
PITCH 			
HORIZONTAL 			
LONGITUDINAL	Focus control for the writing beam		

CHAPTER 3
DIGITAL DISPLAY GENERATOR ELEMENT

SECTION 1
FUNCTIONAL OPERATION OF DD GENERATOR ELEMENT

1.1 PURPOSE OF DIGITAL DISPLAY GENERATOR ELEMENT

The DDGE contains the equipment necessary to take digital data messages from the Drum System or display tester element (DTE) of the Display System and present these messages for visual display to the DDIE. (See figs. 3–9 and 3–10.) In general, the DDGE accepts digital information from the Drum System, times the operation, converts the information to forms usable by the indicator, and distributes the messages to the correct sections of the DDIE. Specifically, the DDGE performs the following functions:

a. Converts the character selection co-ordinates, which are received in digital form, into character selection analog voltages.

b. Generates character-positioning analog voltages as determined by the desired position of a word within a message.

c. Produces erase and intensification gates together with indicator selection signals. The combination of these signals erases the previous messages from the appropriate CRT's, then writes and displays the new messages received from the Drum System.

d. Produces contrast signals to improve the quality of displayed messages.

1.2 DDGE LOGIC-BLOCK FUNCTION

The DDGE consists basically of five sections: the input switch, indicator selection, character selection, character-positioning, and timing and control sections. These sections are shown in figure 3–11 with their interconnecting signals.

1.2.1 DD Input Switch Section

The DD input switch section consists of a group of relays which function as a switching device. With the relays in the normal position (de-energized), signals are provided by the Central Computer and Drum System. When the relays are actuated for test operation, the normal inputs from the Central Computer and Drum System are replaced by simulated signals generated by the DTE.

All timing and control signals are fed through the input switch to the timing and control section, and the thirty information bits (L1-L15, R1-R15) are applied through the input switch to the character selection section.

1.2.2 DD Indicator Selection Section

Each DD message is recorded in one slot of the MIXD drum and is displayed only on consoles assigned to that slot. The indicator selection section generates signals which correspond to the slot number of the message being processed. These signals, generated by the slot-counter circuit, permit the proper DD CRT to be intensified and, thus, to display the message.

A DD CRT display must be erased about 200 ms before it receives a new message. While one DDIS is being erased, another is being intensified. The slot-counter signals which select one DDIS for display can, therefore, be used to select another for erasure.

The slot number of the message is not contained in the message itself, but is established in a counter (fig. 3–12). This counter is preset to the initial slot of a DD group at the start of a cycle and is stepped by a new-slot (add-1) signal from the DD timing and control section each time a new message (slot) is to be displayed. Slot counter outputs corresponding to the last slots (slot 106 or 126) in each DD group are used to generate the end-slot signal, which establishes the end of a display cycle. All outputs applied to the DDIE are also fed to dummy loads when the DDGE is in test status. The dummy loads provide loading for the driving circuits and are physically located in the SDGE (unit 24).

1.2.3 DD Character Selection Section

The character selection section stores the information bits received in binary form and decodes the bits one character at a time. Since the DDIE requires analog voltages to effect a visual presentation, the binary information bits received from the input switch must be converted to analog voltages (see fig. 3–13).

The selection bits for the H character are applied to a register circuit where they are decoded and then fed to the indicator element. After the H character has

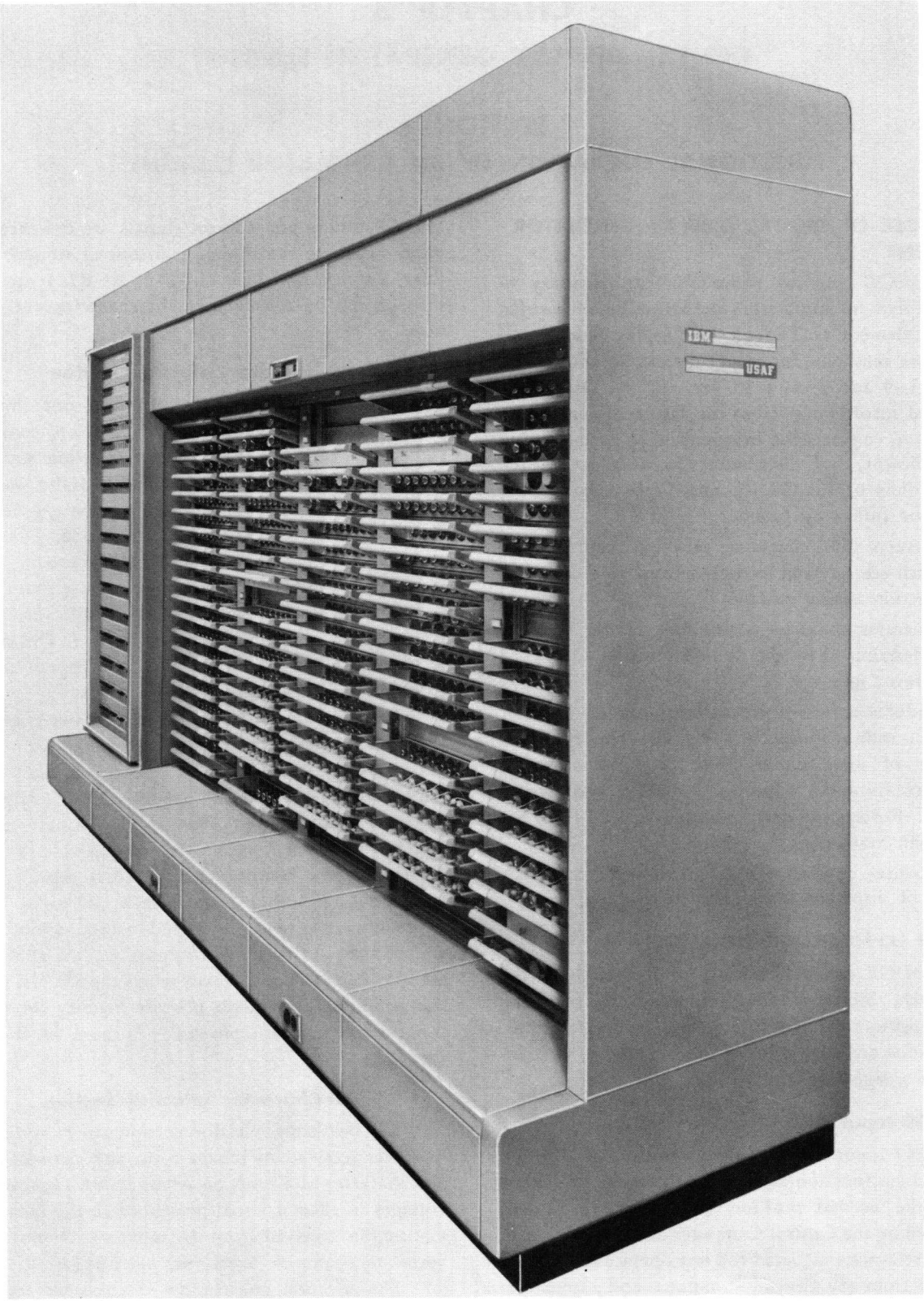


Figure 3–9. Digital Display Generator Element

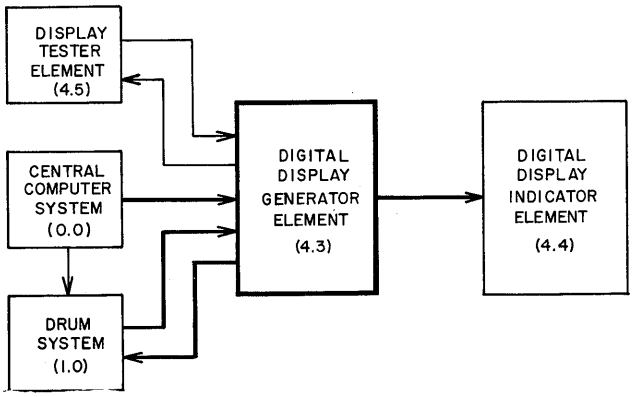


Figure 3–10. DDGE, Logic Flow Diagram

been displayed and the character register has been cleared, the I character bits which have been in storage are shifted to the register, are decoded, and then displayed. The processing of the J, K, and L characters is similar.

1.2.4 DD Character Positioning Section

The function of the character positioning section (fig. 3–14) is to produce four analog voltages which are used to position the character selected from the DD tube character-forming matrix. Two counters in the section generate binary voltages whose outputs condition two decoding circuits. The outputs of the decoding and driver circuits are analog signals which are fed to the indicator as positioning voltages.

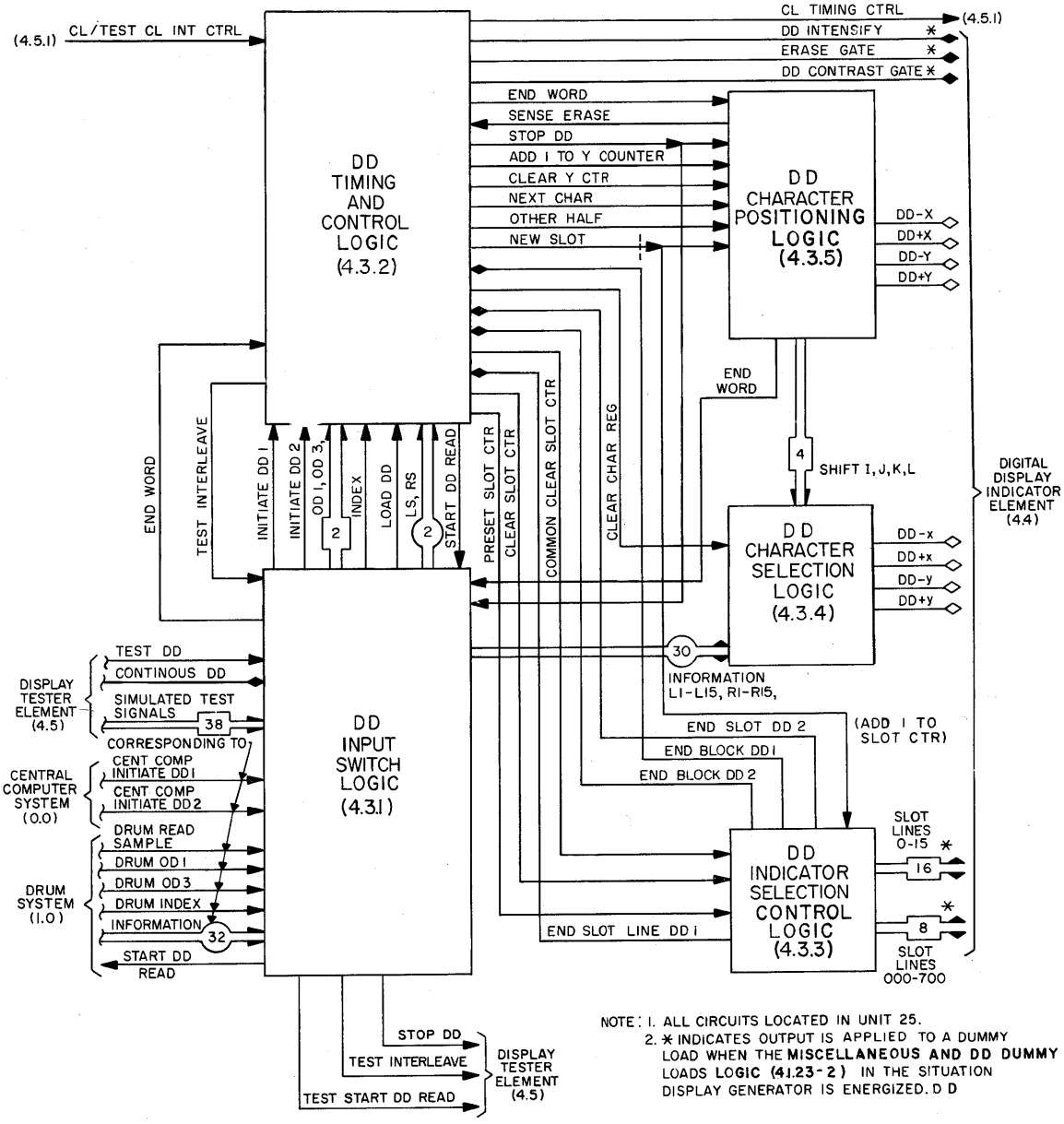


Figure 3–11. DDGE, Functional Block Diagram

The two counters determine the horizontal and vertical position of a given character. The next-character and add-1-to-Y-counter signals are used to step the X and Y counters, respectively. A word is positioned on the left side of the CRT viewing screen by the left-half signal from the timing and control section. The other-half signal positions the word on either the left or the right side of the viewing screen, depending upon the side in use when the other-half signal is received.

The X counter circuit also produces shift control signals which are fed to the character selection section. The shift signals are timed by the next-character signal from the timing and control section. End-word and sense-erase signals are also generated by the character positioning section and are used by the timing circuit to establish the erase gate.

1.2.4.1 X-Position Counter and Shift Control

The X-position counter is a basic binary counter which controls both the generation of shift signals and X positioning voltages. Each next-character signal applied to the counter steps the counter to a new combination and, at the same time, produces a character-shift signal. The left-half and other-half signals are generated by the bits sensed in the control bit sensing circuit. The left-half signal sets the counter to a predetermined combination which positions the characters on the left side of the viewing screen. The other-half signal sets the counter so that the remainder of the message is displayed on the opposite side of the viewing screen. The sense-erase signal is a branch of the shift-L signal. End-word signals are generated by the X-position counter and shift control circuit as an indication that the word has been shifted from storage to the character decoder. These signals occur 120 μsec after each shift-L signal.

1.2.4.2 Y-Position Counter

The Y-position counter is a 4-stage counter capable of producing 16 different output combinations. Each of these combinations is used to define a particular Y position on the viewing screen. The add-1-to-Y-counter signal is a branch of the end-word signal developed by the X-position counter. Therefore, each time an end-word signal is generated, the Y-position counter is advanced to the next binary combination. The counter is cleared by the new-slot combination of sign bits produced when a new message is received. The preset-Y-counter signal is the stop-DD signal generated at the end of the display cycle.

1.2.4.3 Character Position Decoder and Line Drivers

The function of this circuit is to convert binary voltages received from the X- and Y-position counters to the analog voltages required by the indicator element.

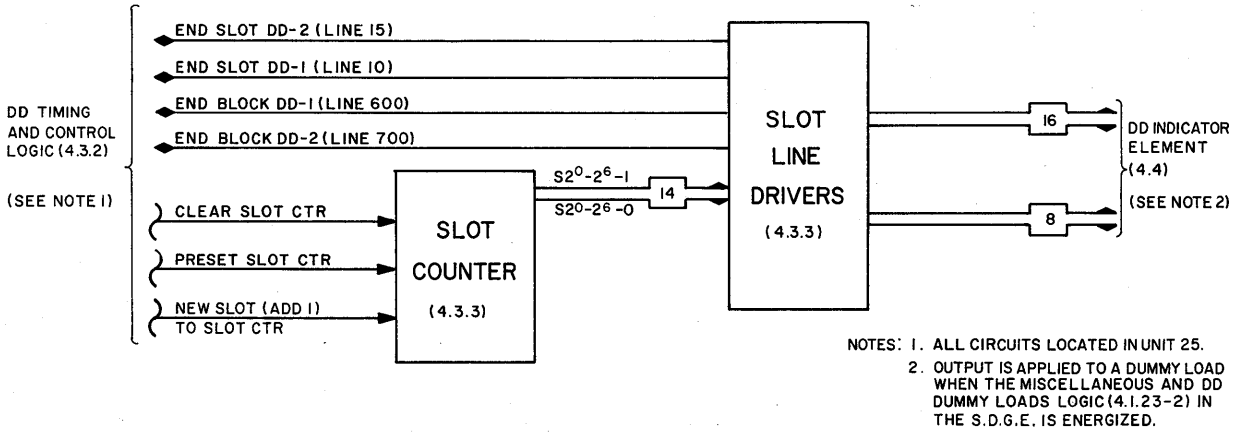


Figure 3–12. DD Indicator Selection Section, Functional Block Diagram

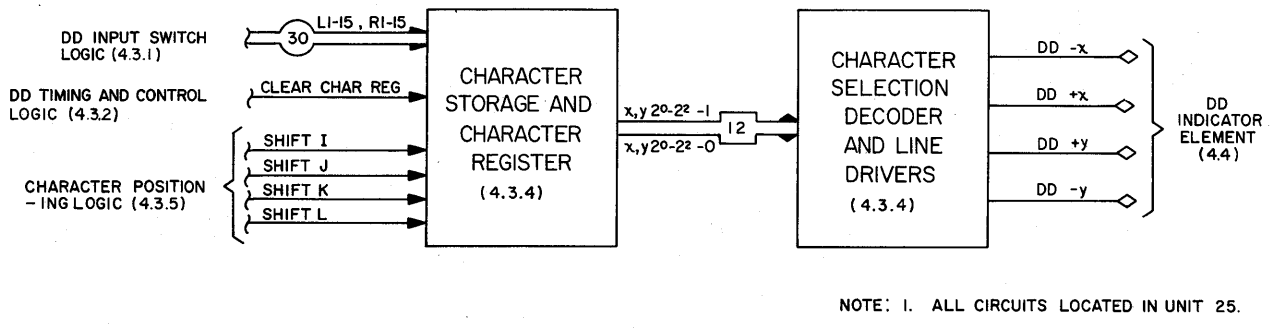


Figure 3–13. DD Character Selection Section, Functional Block Diagram

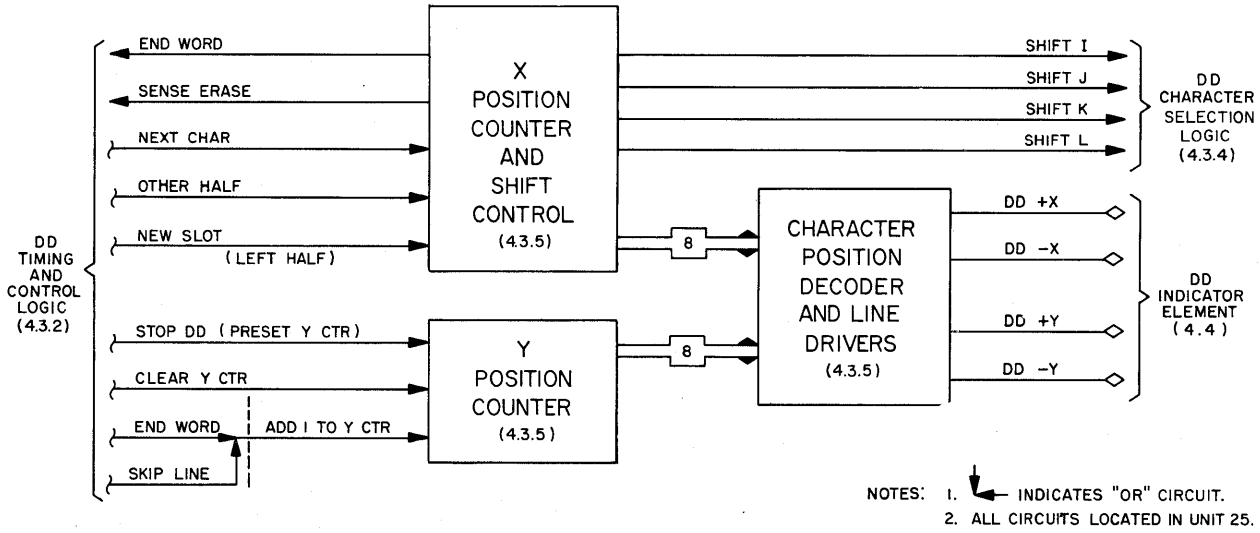


Figure 3–14. DD Character Positioning Section, Functional Block Diagram

Eight input lines from each of the counters are fed to the character position decoder, which transfers the contents of the counters at any given count. The decoding circuit converts these signals to four analog voltages ($\pm X$, $\pm Y$), which are used by the indicator element to position the characters both vertically and horizontally on the viewing screen.

1.2.5 DD Timing and Control Section

The DD timing and control section consists of five circuits: the master control, character timing and intensity, control bit sensing, contrast gate, and erase gate circuits (see fig. 3–15). The master control circuit performs the major portion of the control functions of the section. Character timing and intensity circuits establish a time base against which intensification and erase gates are generated. The control bit sensing circuit performs programmed functions on the basis of the content of the left and right sign bits. A sensing circuit also controls the generation of erase gates. The contrast gate circuit provides a gated signal to improve the relative contrast between the display and nondisplay areas on the face of the DD CRT.

1.2.5.1 Overall Timing and Control Functions

The sequence of operations performed by the DDGE to effect the visual presentation on the DD CRT is controlled by signals generated in the DD timing and control section. Figure 3–16 illustrates the overall timing of both a DD 1 and a DD 2 cycle. A DD cycle begins with an initial period followed by a series of continuous read and display operations which comprise the display period and the retention period. The duration of the initial period varies between 205 and 255 ms and depends upon the receipt of the first MIXD OD IX pulse in relation to the time the initiate-DD signal is received by the DDGE.

Once the initial period has ended, the DDGE receives digital data from the Drum System. The first word read from the drum is stored, processed, and fed to a selected indicator section of the DDIE. A 640-μsec interval exists between readings.

The drum skips 63 registers of its field and then reads the 64th register out to the DD generator. A read time interval of 630 μsec exists when the drum is precessed. The drum is precessed at index time, which occurs once every revolution.

The duration of the display period is 1.34 seconds for DD 1. The period ends 640 μsec after the last word is received by the generator element. The DDGE must receive another initiate-DD signal from the Central Computer before it will begin another display cycle.

1.2.5.2 Master Control Circuit

The master control circuit synchronizes Display System and Drum System operations. A phase counter and delay counter are utilized to achieve this synchronism. The delay counter is used to assure the complete erasure of DD tubes in the initial erase. Upon receipt of an initiate-DD signal, OD 1 and drum-index pulses condition these counters to produce a start-DD signal. This signal is sent to the Drum System as an indication that the DDGE is ready to receive information signals.

The display period of the DD cycle begins with the arrival of the first load-DD signal and continues until the master control circuit receives end-block and end-slot levels with an end-word signal. The stop-DD display signal generated at this time is fed to the Y-position counter to preset the counter in preparation for the next DD cycle. During the display period, add-1 signals are fed to the Y-position counter when an end-word or skip-line signal is received by the master control circuit. When an initiate-DD 1 signal is received,

common-clear-slot-counter and clear-slot-counter signals are sent to the slot counter. When an initiate-DD 2 signal is received, common-clear-slot-counter and preset-slot-counter signals are sent to the slot counter to preset it for the display of group DD 2.

The add-1 signals to the character timing and intensity circuit are gated OD 1 signals which recur every 10 μsec. The load-DD signal is fed to the character timing and instensity circuit as a clear signal.

Initial-erase, end-word, and stop-DD signals are applied to the erase gate circuit to control the erase gate.

OD 3 signals are gated through the master control circuit to the control bit and character timing and intensity circuits to function as control-bit-sensing and clear-character-register signals.

1.2.5.3 Character Timing and Intensity Circuit

The basic component of the character timing and intensity circuit is a modified 6-stage counter which is stepped by add-1 signals. During the display period of a DD cycle, this counter produces an 80-μsec intensification gate which intensifies the DD tube selected for display. The intensification gates are synchronized with the word being displayed by the clear-timing-control signal from the master control circuit.

During the delay period, no intensification gates are generated, because the slot counter is cleared and no DDIS's are assigned to slot 0; however, the signal which normally initiates intensification is present. The clear-character-register and next-character signals are developed at this time. The next-character signal is used by the generator element to time the initial erase gate and the character register.

1.2.5.4 Control Bit Sensing Circuit

The control bit sensing circuit is a decoding matrix which controls the positioning of a display word on the selected DD tube. Three AND circuits are utilized to sense the value of the two control bits (LS and RS) that are present in each of the words received by the generator element. One of four combinations of left and right sign bit levels (00, 01, 10, or 11) are avail-

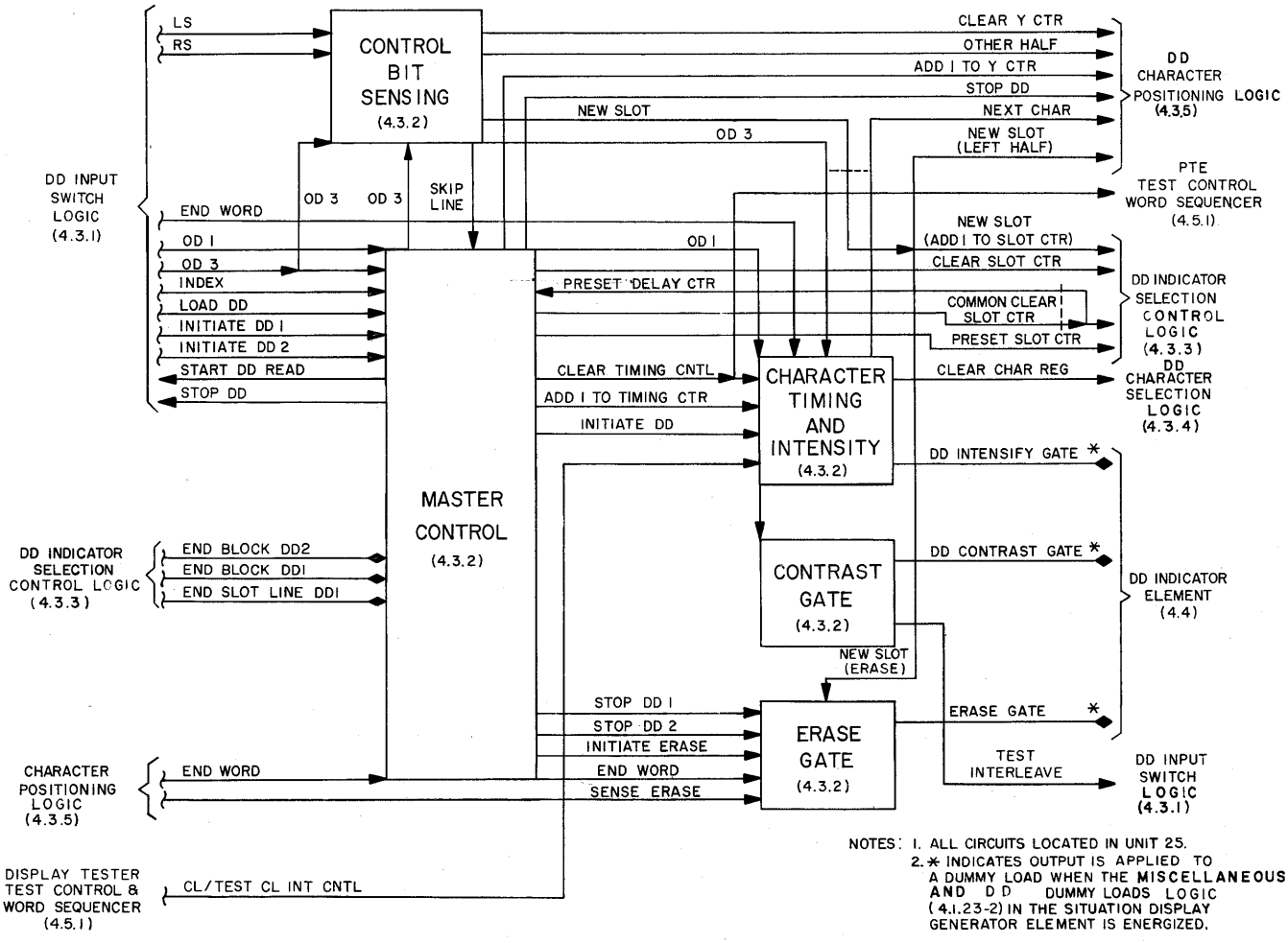


Figure 3–15. DD Timing and Control Section, Functional Block Diagram

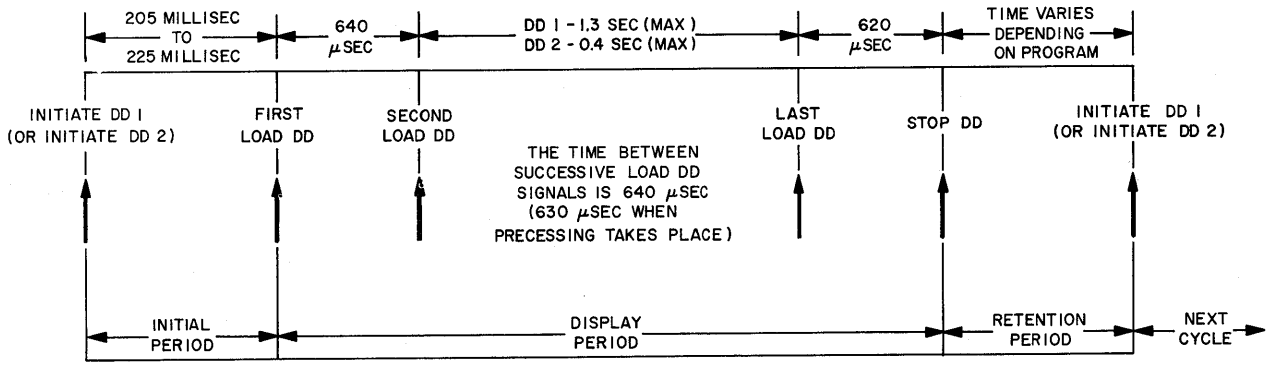


Figure 3–16. Overall Timing of DD Cycle

able. A 0 in the LS bit and a 1 in the RS bit produces the combination 01, which clears the Y-position counter and generates a new-slot signal, advancing the slot counter. This last action selects another indicator section for display. The new-slot signal is also applied as a left-half signal to the X-position counter and shift control circuit. As a result, the word is displayed at the upper left of the newly selected DD CRT.

When the LS bit is 1 and the RS bit is 0, the Y-position counter is cleared and the other-half signal is applied to the X-position counter. As a result, the remainder of the message is displayed on the other half of the display tube. A 1 in both sign bit positions generates a skip-line signal which steps the Y-position counter and causes the word to be displayed two lines below the previous word displayed. If both sign bit positions contain a 0, the display continues with the word placed directly beneath the previous word displayed.

OD 3 timing pulses are used to sense each of the gate tubes conditioned by the control bit sensing circuit. The erase signal is actually the new-slot signal produced by the 01 combination of the left and right sign bits, respectively.

1.2.5.5 Erase Gate Circuit

Normally, once a message is displayed on the viewing screen, it is displayed continuously until erased by a signal developed by the generator element. The function of the erase gate circuit is to produce this erase signal for distribution to the DDIE. The first erase gate produced occurs during the initial period of the DD cycle and is 2,280 μsec in duration. At this time, the initial-erase and sense-erase signals generated by the master control and character positioning circuits are used to produce the erase gate. During the display period of the cycle, the erase gate circuit utilizes both the new-slot (erase) signal generated by the control bit sensing circuit and the sense-erase signal. The duration of the erase gate is controlled by a counter which is pulsed by end-word signals from the character-positioning section. The time duration of each erase gate is 2,400 μsec. No erase gates are generated after a stop-DD signal is received from the master control circuit, until the following cycle.

1.2.5.6 Contrast Gate Circuit

The function of the contrast gate circuit is to generate a gate that can be used by the DDIE to improve the contrast between the used and unused portions of the display. As shown in figure 3–15, OD 1 timing pulses are used to generate this gate. Each OD 1 pulse applied to the circuit steps a 7-stage counter which produces a 10-μsec gate after 64 pulses have been received. The gate is then applied to all display tubes of the element to improve contrast. Test-interleave signals generated by this circuit are used by the DTE during test operations.

1.2.6 DD Timing and Control Inputs

The DD timing and control section receives most of its input signals through the input switch. During test operations, all signals are replaced by simulated signals from the DTE. The input signals are enumerated below by type:

a. To initiate display cycles, the initiate-DD signals from the Central Computer.

b. To sequence events within a display cycle, the OD 1, OD 3, MIXD OD IX, and load-DD signals generated by the Drum System and the end-word and sense-erase signals from the character-positioning section.

c. To end display cycles, the end-slot-DD and end-block-DD signals generated in the indicator selection section.

d. To control word position and slot count, the LS and RS signals (the control bits from the Drum System).

1.2.7 DD Timing and Control Outputs

The DD timing and control section applies a start-DD-read signal to the Drum System to indicate that

the DDGE is ready to process messages. The timing and control circuitry also generates signals which are used within the DDGE. These signals clear, set, and/or step circuits in the indicator selection, character selection, and character-positioning sections. Three signals are supplied to the DDIE, as follows:

a. DD intensity gate – accompanies each character to permit its display.
b. Erase gate – generated with each slot (message) to permit erasure of the DD CRT assigned to display some later message.
c. Contrast gate – generated every 640 μsec to increase the contrast ratio.

The three outputs to the DDIE are also routed to dummy loads when the DDGE is in test status. The dummy loads are physically located in the SDGE.

SECTION 2
LOGIC OPERATION OF DD GENERATOR ELEMENT

2.1 DD INPUT SWITCH

Figure 3–17 is a simplified diagram of the DD input switch section, showing inputs from the Central Computer System, Drum System, and the DTE. The relays used to control switch action are maintained in the de-energized condition during a display cycle and are energized only when the DTE is performing DD test operations. Thus, during a display cycle, all signals applied to the input switch from the Central Computer and Drum System are passed to the components of the generator element.

Nine of these signals are fed to the DD timing and control section, and 30 signals (L1-L15, R1-R15) are passed to the character selection section. The OD 1 and OD 3 pulses are drum timing signals which are separated by 5 μsec and which recur at 10-μsec intervals. Drum-index pulses recur at a rate established by the speed of the MIXD drum. One index pulse is generated at OD 3 time each time the drum makes one revolution. Once the display cycle begins, this pulse recurs every 20.48 ms.

The read-sample pulse is applied to the input switch at the same time as the 30 information bits. The read-sample pulse is called a load-DD signal when it leaves the switch and indicates that a word transfer has been effected from the Drum System. The initiate-DD signals are generated by circuits in the Central Computer System. Generation time is a function of the Central Computer program. End-word signals are applied through the switch for transfer to the master control section.

Four signals produced by the DDGE are applied to the switch for transfer to the Drum System, to the DTE, and to other sections in the generator. These signals are the start-DD-read, stop-DD, end-word, and test-interleave signals. The start-DD-read signal is generated by the master control circuit and informs the Drum System that the initial period of the display cycle has ended.

A stop-DD signal is passed by the switch to the master control circuit as an end-control signal and is used by this circuit to end the display cycle. End-word signals, when received, indicate that the previous word has been displayed and that the character-positioning section is now ready to receive the next word. Test-interleave signals are used by the DTE during test operations.

Other signals fed through the input switch with the input switch relays energized are the simulated signals generated by the DTE for test operations.

2.2 DD INDICATOR SELECTION SECTION

Selection of an indicator section (or slot) for display or erasure is controlled by the slot-counter and slot-line driver circuits. The slot counter circuit is pulsed by a new-slot signal from the control bit sensing circuit. This signal is generated when a 01 combination exists in the sign bits of the DD word. Each add-1 signal applied to the counter establishes a new count to provide selected output levels. These output levels condition two matrices in the slot-line driver circuit. Twenty-four lines from the slot-line driver circuit are connected to the display tubes of the indicator element in such a manner that each add-1 signal applied to the counting circuit selects a new slot for display or erase.

2.2.1 Slot Counter Circuit

The slot counter is a 7-stage counter used to select DDIS's, in sequence, for intensification and erasure. (See fig. 3–18.) By means of the common-clear-slot-counter and clear-slot-counter signals, the slot counter is cleared upon arrival of the initiate-DD signal. The counter is stepped when a word read from the Drum System is the first word of a slot. The 1 side of each flip-flop conditions an associated gate tube. Thus, the first add-1-to-slot-counter signal inspects gate tube (GT) 1 and sets flip-flop (FF) 1. The second signal passes GT 1 and

complements FF's 1 and 2. With each successive signal, a new binary combination is established in the flip-flops.

Slot counter operation during the DD 2 cycle is the same as for the DD 1 cycle, except that the initiate-DD-2 signal presets the slot counter to 107 instead of clearing it to 0. The initiate-DD-2 signal pulses the common-clear-slot-counter and preset-slot-counter lines and establishes the number 1101011 in the 7-stage counter.

The seven stages of the slot counter are used in two groups, with four flip-flops in the first group and three flip-flops in the second group. The first group of four flip-flops has a total count of 16; the second group of three flip-flops has a total count of 8. A total of 128 (16 x 8) different combinations can be established by the counter. Combinations (slots) 0 through 106 are assigned to DDIS's in the DD 1 cycle; slots 107 through 127 are assigned to DDIS's in the DD 2 cycle.

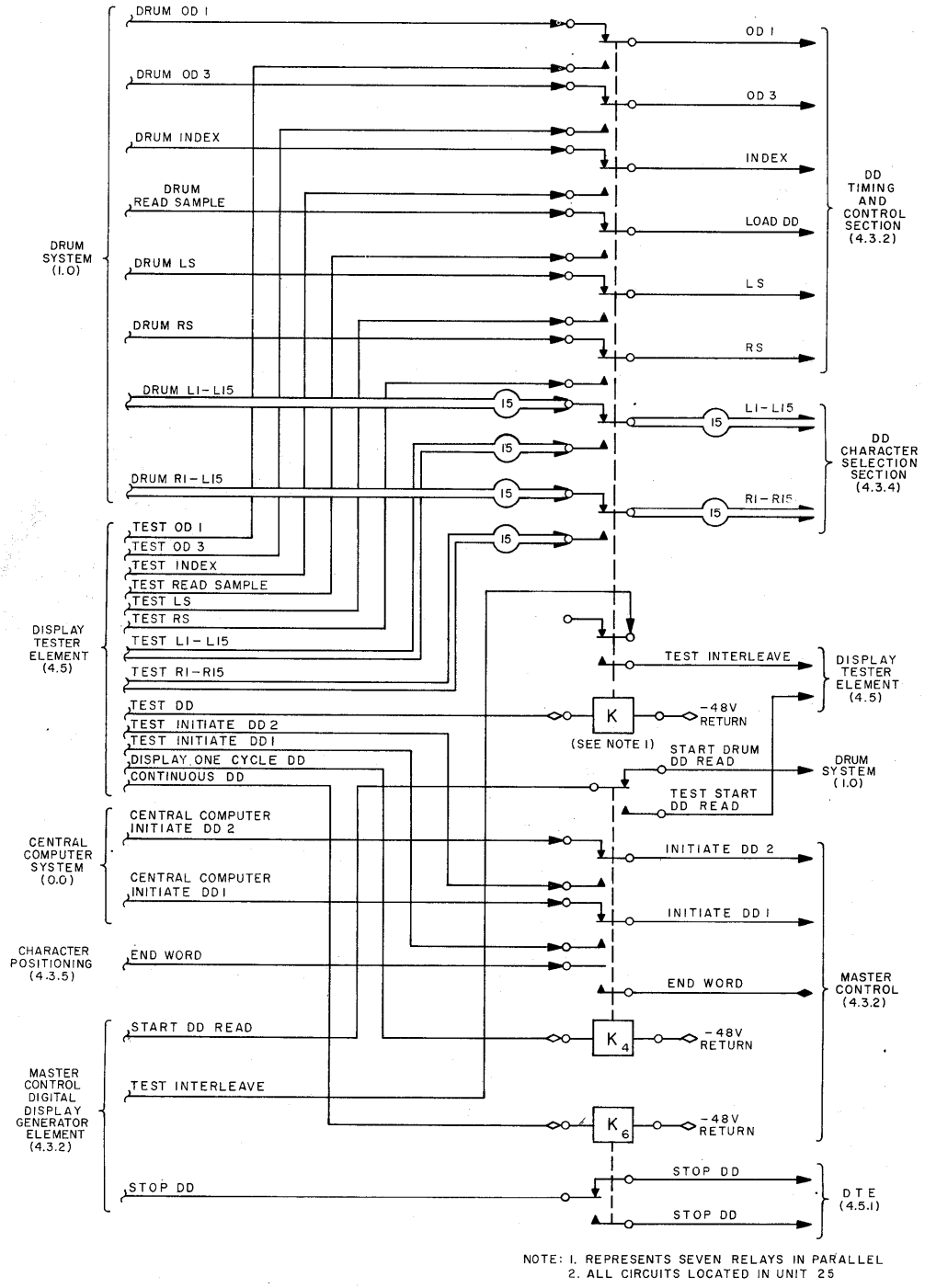
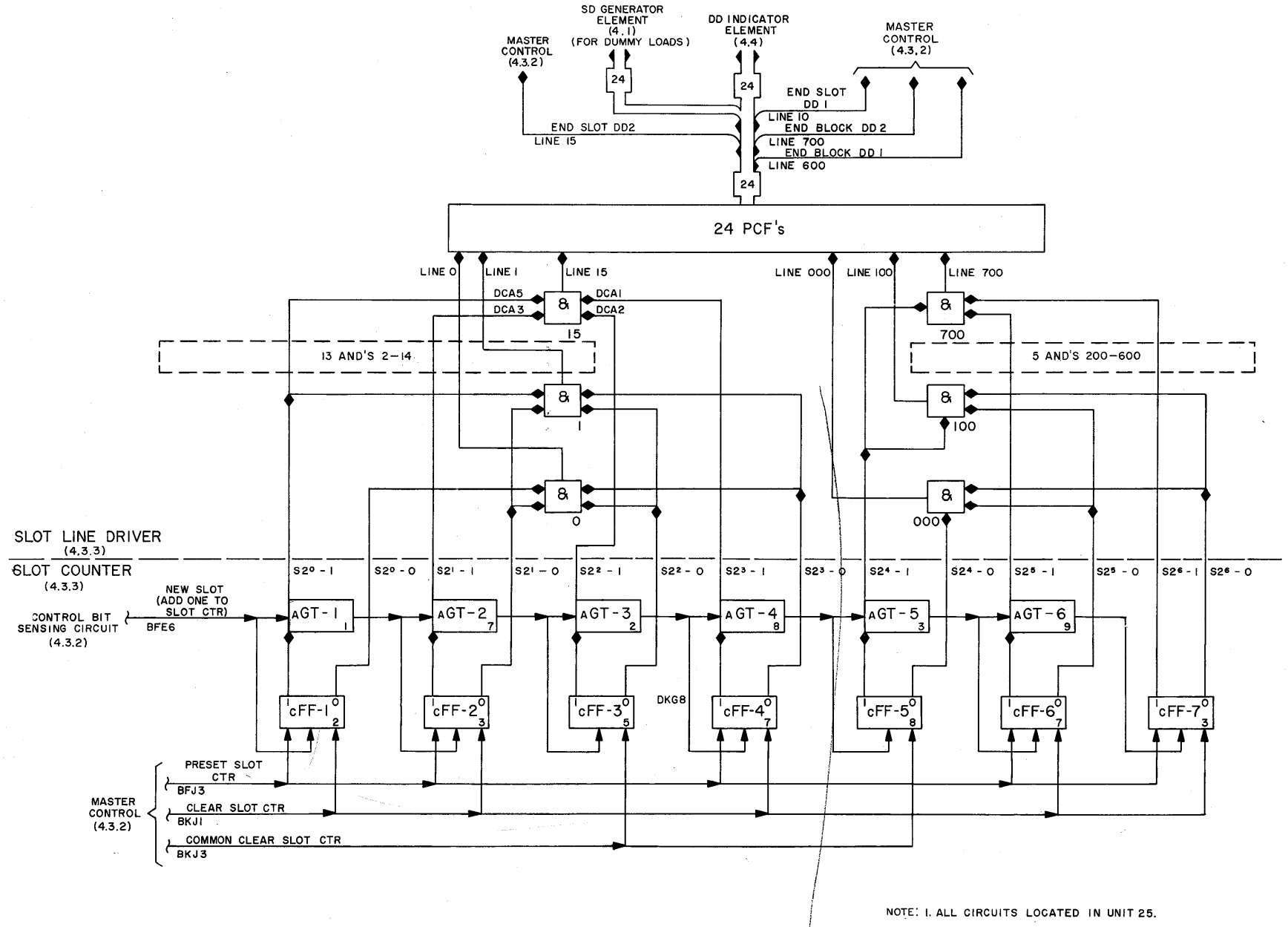


Figure 3–17. DD Input Switch Section, Simplified Diagram



NOTE: 1. ALL CIRCUITS LOCATED IN UNIT 25.

Figure 3—18. Slot Counter and Slot Line Drivers Circuit, Logic Diagram

The theory of operation of the slot counter used in the AN/FSQ-8 is similar. For a more detailed analysis of the slot counter used in the AN/FSQ-8, refer to Part 7.

2.2.2 Slot Line Driver Circuit

The function of the slot line driver circuit is to sense the slot count in the slot counter and to provide the indicator element with signals on two of the 24 slot lines which relate the condition of the counter at any given time. Two matrices are utilized to perform these functions. One matrix is associated with the first four flip-flops and is designated the A slot line. The other matrix is associated with the remaining three flip-flops and is designated the B slot line. Any binary combination present in the first four flip-flops conditions one of 16 AND circuits in the driver (see fig. 3–18). The output of the conditioned AND is fed to its corresponding power cathode follower (PCF) and is supplied on the A slot line to the DDIE. At the same time, the voltage combination present in the remaining three flip-flops conditions one of eight AND circuits. The output of the conditioned AND is fed to its associated PCF and is supplied on the B slot line to the DDIE. In this manner, any combination contained in the slot counter produces two conditioning voltages which are applied simultaneously to the slot line driver. The A slot line levels are labeled 0 through 15, and the B slot line levels are labeled 000, 100, 200, ... 700. The slot line driver circuit passes the two signals to two preassigned slots in the indicator element. One of the slots is intensified while the other is erased.

When the common-clear-slot-counter and clear-slot-counter signals are applied to the slot counter, a 0000000 combination is established in FF's 1 through 7. This combination conditions AND's 0 and 000 in the matrices. The outputs of these AND's are fed through the PCF's to select the first slot (slot 0) in the indicator element. The first add-1-to-slot-counter signal steps the slot counter by one and produces the combination 0000001. At this time, AND's 1 and 000 are conditioned, selecting the next slot in the indicator element. The combination in the slot counter at the time of the 15th add-1 signal conditions AND's 15 and 000; the combination resulting from the 16th signal conditions AND's 0 and 100.

This process of conditioning and sensing for indicator selection is continuous during a display cycle. The outputs of AND's 10 and 15 are taken to the master control circuit as end-slot-DD-1 and end-slot-DD-2 signals. The output of AND's 600 and 700 are fed to the master control circuit as end-block DD-1 and end-block-DD-2 signals. In the master control circuit, the end-slot-DD-1 and end-block-DD-1 signals are combined with an end-word signal to end the display period. A similar combination is used to end the DD 2 cycle.

All 24 slot lines are routed to dummy loads when the DDGE is in test. The dummy loads are located in the SDGE.

2.2.3 Intensification and Erase Gate Distribution

Once generated, the intensification and erase gates are applied to all tubes simultaneously. The combination of these gates and the two outputs from the slot line drivers control the display intensification and erase operations. The two signals from the slot line driver are applied to the indicator element in such a manner that one indicator section (slot) is erased while another slot is intensified. A display on the DD CRT must be erased before new information is displayed. The erase operation, therefore, is performed on the slot that will be intensified at some later count of the slot counter.

2.3 DD CHARACTER SELECTION SECTION

The character selection section is used to store each display word received from the Drum System and to furnish the indicator element with analog signals representing, successively, the five characters of the word. When the word is received from the drum field, the I, J, K, and L characters are stored in the character storage circuit. As the H character is the first character displayed, the H character bits (L13-L15, R13-R15) are transferred directly to the character register for processing. Once the H character is displayed, the I, J, K, and L characters are shifted sequentially into the character register.

The character decoders generate four analog voltages for each character, two for x selection and two for y selection. The x- and y-character selection voltages are used to deflect the electron beam to the selected character in the character-forming matrix. The character selected is a function of the binary value of the character bits presented to the decoding circuit.

2.3.1 Character Storage and Character Register Circuit

Each character of a DD word is represented by six binary bits. These bits are assigned specific positions in the word. The value of the bits which comprise the left half of the word are used to condition the horizontal section and are called x selection bits. Bits assigned to the right half-word are used to condition the vertical section and are termed y selection bits. The content of each bit position is fed to the 1 side of its associated flip-flop in the character storage and character register circuit. (See fig. 3–19.) The H character is transferred directly to the character register and the remaining characters are transferred to assigned storage registers.

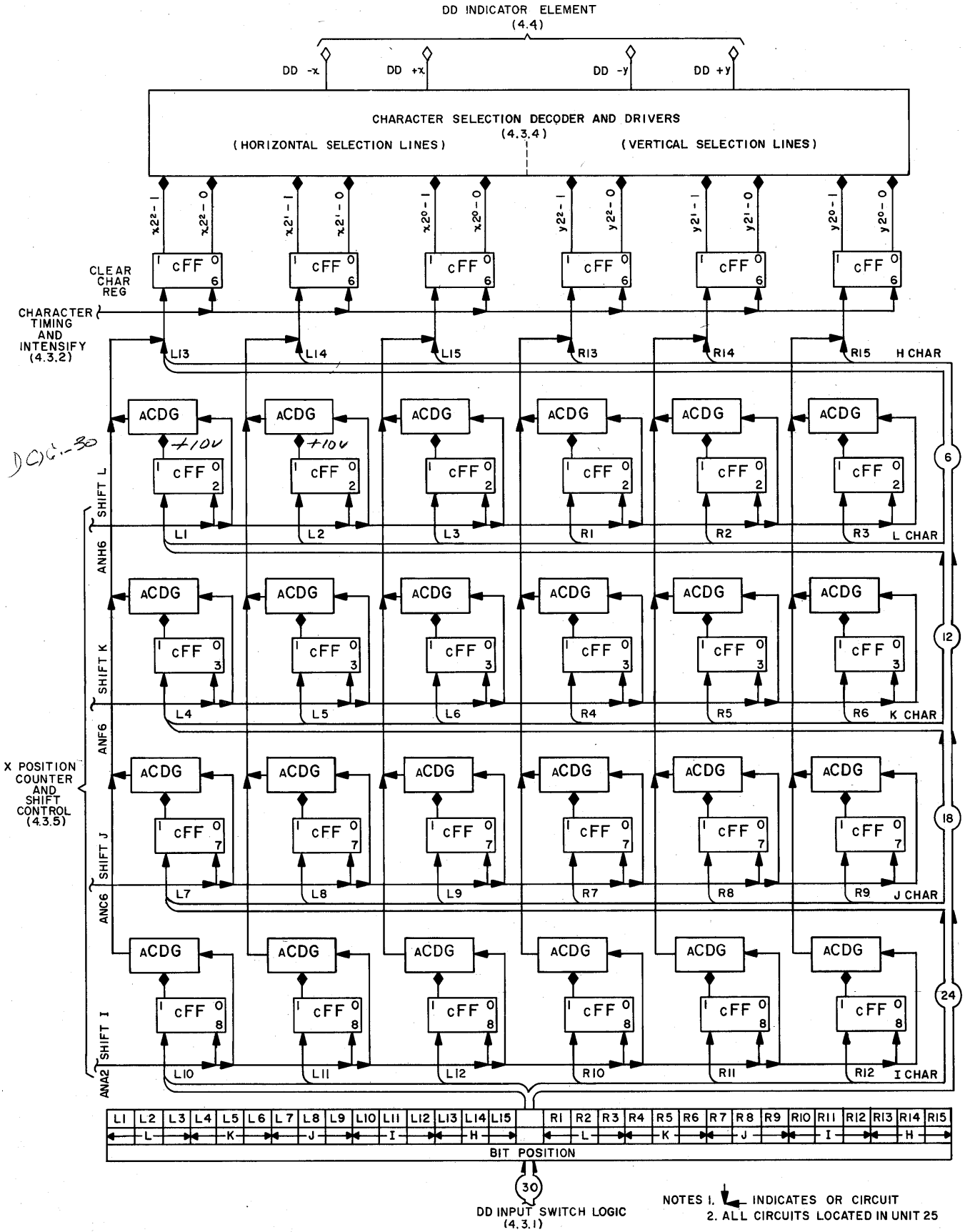


Figure 3–19. Character Storage and Character Register Circuit, Logic Diagram

Initially, all flip-flops are cleared, and upon receipt of a word from the drum field only those bits representing a 1 will set the related flip-flops. The remaining flip-flops retain their 0 levels. The I, J, K, and L characters are fed to flip-flops which are associated with gate circuits. If these storage flip-flops have been set, the gate circuits will be conditioned. Shift signals from the X-position counter sense the gates, pass the contents to the character register, and clear the storage flip-flops.

The shift I signal is received 140 μsec after the word is received from the drum. During the 140-μsec interval, the H character is applied to the decoders and the character register is cleared by the clear-character-register signal. The shift-I signal transfers the contents of the I storage flip-flops to the character register and clears the I storage flip-flops. Thus, the first shift-character signal places the I character in the character register and clears the storage register initially used to store this character.

The remaining characters (J, K, and L) are shifted at 120-μsec intervals in the manner described previously. Five μsec prior to each shift signal, the character register is cleared by a clear-character-register signal. During a continuous read operation, the end-word signal is generated by the X-position counter and shift control circuit 120 μsec after the shift-L signal. Five μsec prior to the end-word signal, a clear-character-register signal is applied to the character register. All registers having been cleared, the next word is read 20 μsec after the end-word signal (10 μsec if precessing takes place). The character storage and character register circuit, therefore, receives the next word 140 μsec after the L character is shifted from storage to the register. At this time, the H character of the following word is applied to the decoders.

2.3.2 Character Selection Decoder and Drivers Circuit

The character selection decoder and drivers circuit receives six binary voltages from the character register. These binary voltages represent the x and y selection voltages which must be converted to analog form for use by the DD tubes. The six binary outputs from each half of the character register are fed to three current gate tubes in the decoder. It is the function of the decoder to convert each group of six binary voltages into two groups of analog voltages (x and y) 180 degrees out of phase. The two DD x-character-selection and two DD y-character-selection analog voltages are then fed to the DD tubes, where they are used to deflect the electron beam to the selected character in the character-forming matrix.

2.4 CHARACTER POSITIONING SECTION

The circuits of the character positioning section are used to generate the voltages required by the indicator element to position the character selected from the character-forming matrix on the viewing screen. Two counting circuits, the X-position counter and the Y-position counter, are utilized to produce the necessary binary voltages which are applied to the decoding circuits. The character position decoder and line driver circuit generates four analog voltages which are fed to the DD CRT to deflect the selected character to the desired position on the viewing screen. The specific position occupied by the character is a function of the voltages applied to the decoder circuits. The decoders generate two voltages for horizontal or X positioning and two voltages for vertical or Y positioning.

The X-position counter and shift control circuit also controls the shift operation of transferring characters from storage to the character register.

2.4.1 X-Position Counter and Shift Control Circuit

The X-position counter and shift control circuit (fig. 3–20) conditions the decoder circuits with the voltages required for the X positioning of the selected character, and performs the shifting operations necessary to transfer characters from storage into the character register.

2.4.1.1 Counting and Shift Control

The next-character signal generated by the character timing and intensity circuit is used to step the X-position counter. After the H character has been processed, the first next-character signal is applied to GT 1, figure 3–20. The next-character signal is passed through GT 1 as a shift-I signal, since GT 1 is conditioned by the 00 AND. The shift-I signal is fed to the character storage and register circuit as a sense-erase signal to the erase gate circuit, and it also sets FF 2^0 in the X-position counter. The shift-I signal shifts the I character from storage into the character register. The sense-erase signal is used with a new-slot pulse by the erase gate circuit to develop an erase gate. The shift-I signal and sense-erase signal are both generated 140 μsec after the first word of the slot is received by the generator element. The sense-erase signal establishes an erase gate only when the word sent from the Drum System represents the beginning of a new slot.

The setting of FF 2^0 by the first next-character signal establishes a 001 combination in FF's L, 2^1, and 2^0, respectively. When the second next-character signal is generated 120 μsec later, it is gated by GT 2. The output of GT 2 sets FF 2^1, clears FF 2^0, and is also fed to the character storage and register circuit as a shift-J signal. The shift-J signal transfers the J character from storage into the character register. The flip-flop combination at this time is 010. The third and fourth next-character signals initiate the shift-K and shift-L signals in the same manner.

When the fifth next-character signal is applied to the parallel bank of gate tubes, it is gated by GT 5, which was conditioned by the fourth signal. The output pulse is called an end-word signal. It is fed to the master control circuit and also clears FF's L and 2^0 in the counter. The end-word signal fed to the master control circuit clears the on-off FF, cutting off add-1-to-timing-counter signals to the character timing and intensity circuit. The total time required to process one word from storage to the character decoders is 620 μsec. The process described is continuous and recurs at the time a new word is read into the generator element.

As shown in figure 3–20, the flip-flop levels are applied to the X half of the decoding and driving circuits as well as to the AND's used in generating the shift signals. Each combination present in FF's L, 2^1, and 2^0 positions a character along the X (horizontal) axis of a display line. Since five characters are assigned to each display line, five different combinations must be generated by the counter for each word received from the

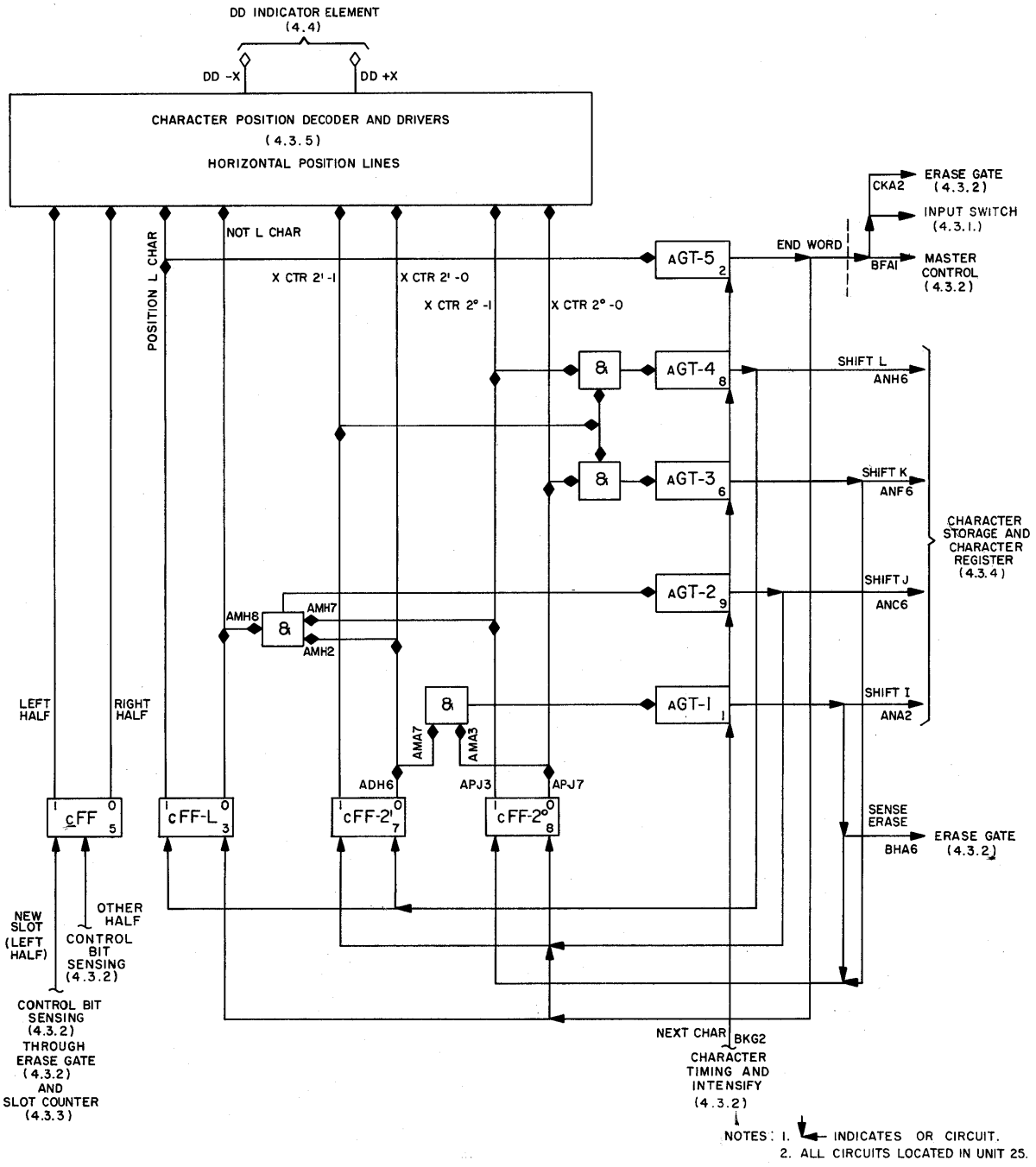


Figure 3–20. X-Position Counter and Shift Control Circuit, Logic Diagram

Drum System. The H character is positioned by the 000 combination when the counter is at 0 (cleared). The I, J, and K characters are positioned by the 001, 010, and 011 combinations, respectively. The L character is positioned by the 101 combination produced when the next-character signal is gated by GT 4.

The decimal values of the five binary combinations generated by the counter are 0, 1, 2, 3, 5, successively. This arrangement of the X positioning voltages accounts for the increased horizontal spacing between the L and K characters, since the positioning voltage for 100 (or 4_{10}) is not used.

2.4.1.2 Left-Half or Other-Half Flip-Flop

The left-half or other-half flip-flop shown in figure 3–20 is used to condition the character decoding circuits so that words will be displayed on either the left side or the right side of the viewing screen. The condition of the flip-flop is determined by signals sent from the control bit sensing circuit. Each new-slot signal generated by the control bit sensing circuit is applied as a left-half signal to this flip-flop. The other-half signal is generated when the words of the slot are to be displayed on the other side of the viewing screen.

2.4.2 Y-Position Counter

The Y-position counter is a 4-stage counting circuit which provides the Y section of the character position decoders and line driver circuit with the signals required to position the word vertically on the viewing screen. Sixteen different output combinations are available, each of which may be used to define a particular Y position on the DD CRT. Since the display has been divided into left and right sides, a maximum of 32 lines may be used for the display of a message. In this manner, a DD tube can display two groupings of 16 words. The full complement of words that can be displayed on a DD tube are contained in 32 drum registers. Figure 3–21 is a logic diagram of the Y-position counter.

2.4.2.1 Y-Counter Operation

The clear-Y-counter signal from the control bit sensing circuit is applied to the 0 side of the flip-flops of the counter. This action clears the counter so that four 0 levels are fed to the Y half of the decoders and

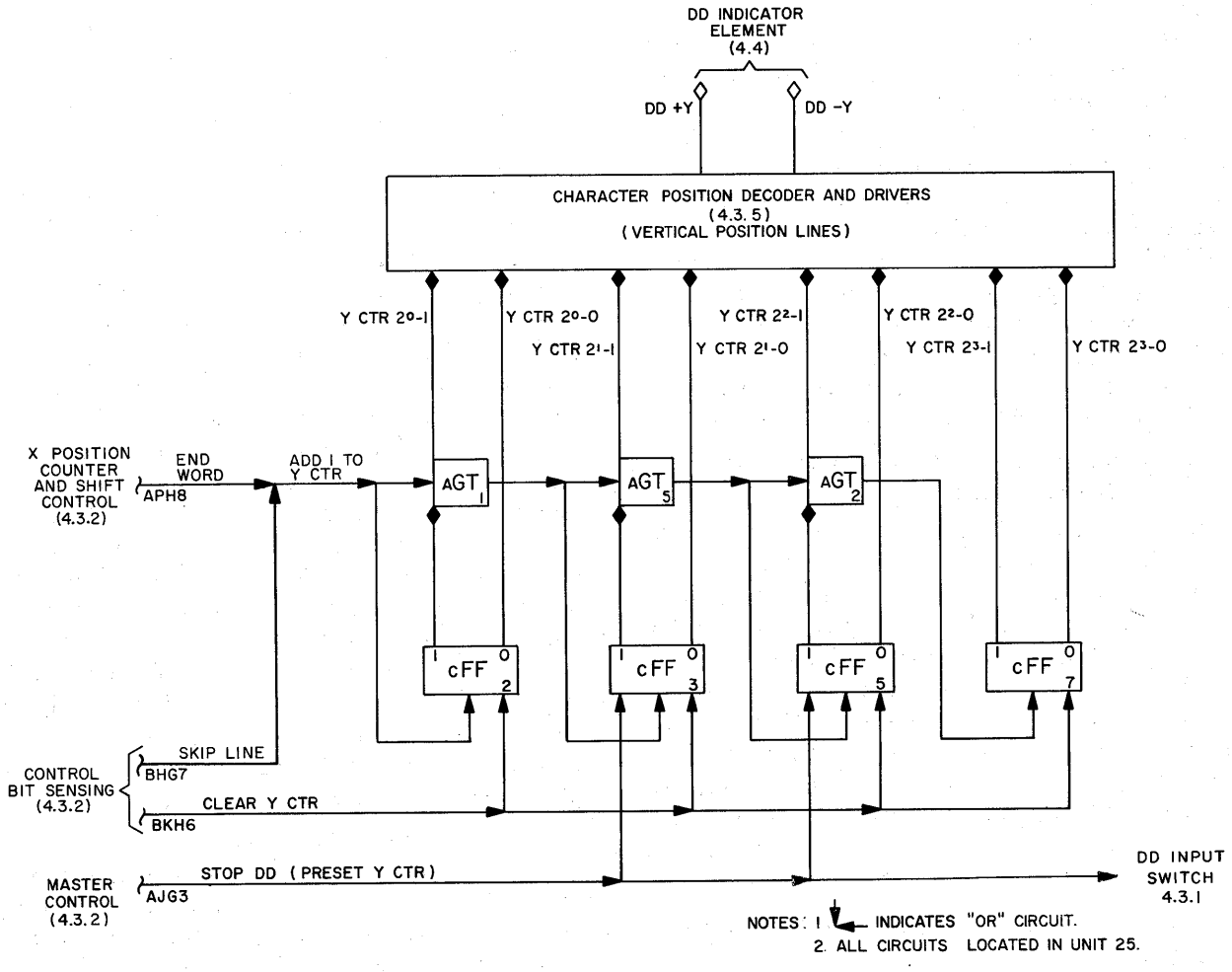


Figure 3–21. Y-Position Counter Circuit, Logic Diagram

drivers. A clear-Y-counter signal is generated when the sign bits of a word indicate that a new slot is being read into the generator element or that the other half of the DD tube is to be used to display the remainder of the message. Both conditions require that the word received from the drum be displayed on the top row of each grouping on the viewing screen. The clear-Y-counter signal is a gated OD 3 signal generated 5 μsec after the word is received from the Drum System.

An add-1-to-Y-counter signal is applied to the Y-position counter each time an end-word signal is generated by the X-position counter and shift control circuit. This add-1 signal is used to step the counter to establish new combinations in the flip-flops. The first signal produces a 1000 combination, the second a 0100, the third a 1100, etc. Unless the sign bits of the incoming words produce a clear-Y signal, the counter will count 15 add-1 signals and then clear itself at the 16th signal. Each combination produced by the add-1 signal is used to define a specific Y position on the viewing screen.

The successive application of add-1 signals to the counting circuit positions each word one line below the word previously displayed. The only exception to this occurs when the Central Computer program requires that the display skip one line. Since each output of the counter determines the word position, passing over a count eliminates that word position. A skipped count is accomplished by the skip-line pulse, which is fed into the add-1-to-Y-counter line, double pulsing the Y counter and providing the skip line required.

At the end of the display period of a DD cycle, a stop-DD signal is generated in the master control circuit to prepare the Y-position counter for the next DD cycle. Flip-flops 2 and 3 are set by the stop-DD signal. This resting position of the Y counter (0110) facilitates the positioning of the first word of the succeeding slot.

2.4.2.2 Character Position Decoder and Line Driver Circuit

The binary signals from the Y-position counter represent the desired vertical position for the DD words. The signals, however, must be converted to analog form for use by the DD tubes. Eight binary outputs from the counter are applied to the current gate tubes (as in the X-position counter) in the character position decoder and driver circuit. Each group of eight binary signals is converted into two analog voltages 180 degrees out of phase with each other. The two Y positioning voltages (+Y, −Y) are applied to the character positioning plates which position the selected character on the viewing screen.

2.5 DIGITAL DISPLAY TIMING AND CONTROL SECTION

The DD timing and control section synchronizes the generator element with Drum System operations and also controls the remaining components of the generator. The master control and character timing and intensity circuits establish a time base with which the generator element performs its timing functions. The control bit sensing circuit performs control functions in accordance with sign bit values programmed by the Central Computer System. The erase gate and contrast gate circuits generate gates which are used to erase messages previously displayed and to improve the contrast of the message currently displayed.

2.5.1 Master Control Circuit

The master control circuit defines the duration of both the delay and display periods of a DD cycle. Two counters, a phase counter and a delay counter, establish the conditions which control these intervals. The phase counter synchronizes master control circuit operation with Drum System operation and determines the time when the delay counter begins to function. When the phase counter is in its delay phase, the delay counter begins to count drum index pulses. The delay counter counts 10 drum index pulses before it produces a start-DD-read signal. The total time required to generate the start-DD-read signal varies between 205 and 225 milliseconds. The precise time is dependent upon the position of the drum when an initiate-DD signal is received from the Central Computer System.

2.5.1.1 Phase Counter

The phase counter uses three AND circuits to sense the value of two flip-flops in order to establish three separate operating phases: synchronization, delay, and display. Prior to the arrival of an initiate-DD signal, a 00 combination exists in FF's 1 and 2. (See fig. 3–22.) The initiate-DD signal sets FF 2, producing a 01 combination in the counter. This 01 output conditions the sync AND, which in turn provides an up level to GT 1. The next OD 1 pulse passes GT 1 and sets FF 1, resulting in an 11 combination in the flip-flops. This combination defines the delay phase of the phase counter.

The 11 combination is applied to the delay AND, which conditions GT 2. This situation enables drum index pulses to step the delay counter and initiates the initial erase signal. A 10 combination is established in the phase counter when the 11th drum index pulse is gated through the delay counter. This condition initiates the display phase of the phase counter. The phase counter is cleared (00) when a stop-DD signal is applied to the 0 side of FF 1.

2.5.1.2 On-Off Flip-Flop

In addition to their function in the phase counter, initiate-DD signals are also used to generate an initial-erase pulse. As shown in figure 3–22, the initiate-DD signal is applied to the 0 side of the on-off FF. This action conditions GT 5, which is pulsed by the output of

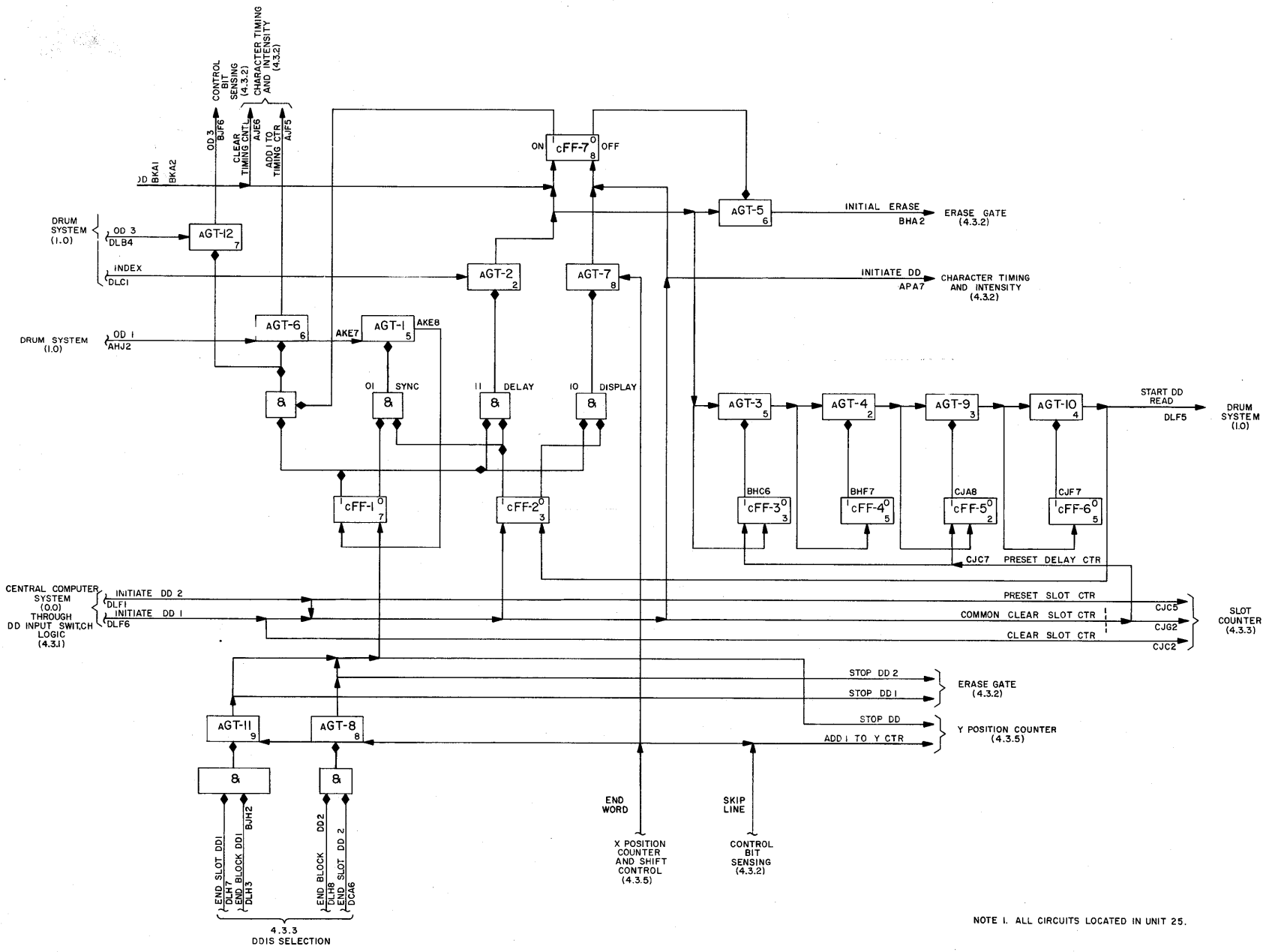


Figure 3—22. Master Control Circuit, Logic Diagram

GT 2. The output of GT 5 is fed to the erase gate circuit as an initial-erase signal. The output of GT 2 is a gated drum index pulse which is applied simultaneously to the 1 side of the on-off flip-flop and to GT 5. This pulse is passed by GT 5 before the on-off flip-flop changes its state.

When the on-off flip-flop and FF 1 are set, GT 6 is conditioned. OD 1 pulses are then gated through GT 6 and are sent to the character timing and intensity circuit as add-1-to timing-counter signals. Thus, an add-1-to-timing-counter pulse is developed for every OD 1 pulse occurring after the first drum index pulse is applied to the master control circuit. When the phase counter is in the display phase and the DD word has been displayed, an end-word signal is gated through GT 7 to clear the on-off FF. As a result, GT 6 is deconditioned and no add-1-to-timing-counter signals are generated until the next load-DD signal is applied to the on-off flip-flop.

2.5.1.3 Delay Counter

The master control circuit uses a 4-stage binary counter to time the delay phase. The preset-delay-counter signal presets the counter to five, consisting of a 1010 combination in FF's 3, 4, 5, and 6. This signal is a branch of the common-clear-slot-counter signal which is generated by either an initiate-DD-1 or initiate-DD-2 signal. Upon receipt of the preset signal, FF's 3 and 5 are set, establishing the 1010 combination in the delay counter. The first index pulse is passed by GT's 2 and 3, setting FF 4 and complementing FF 3. The count is advanced by successive index pulses. The 11th index pulse establishes a 0000 combination in the delay counter, clears FF 2 in the phase counter, and is also fed to the Drum System as a start-DD-read signal. When FF 2 is cleared, a 10 combination is produced in the phase counter which conditions the display AND circuit. Gate tube 2, which was conditioned by the 11 combination of the phase counter, is now deconditioned, preventing drum index pulses from being applied to the delay counter during the display period of the cycle.

2.5.1.4 Display Period Operation

The generator element receives display information from the Drum System 630 μsec after the delay counter generates the start-DD-read signal. The load-DD signal is received by the master control circuit at the same time that the display word is received, and is applied simultaneously to the 1 side of the on-off FF and to the 0 side of the flip-flops in the timing counter. The master control circuit remains in this condition until an end-word signal is received from the X-position counter, indicating that the display word has been applied to the selected DDIS. Since the phase counter is in the display phase, the add-1-to-timing-counter signals are gated through GT 6 to the character timing and intensity circuit to control character timing and intensity. After the last character of the word has been displayed, the end-word signal is fed to the Y-position counter as an add-1 to-Y-counter signal. This action advances the Y-counter to position the next word on the viewing screen. When the next word is sent from the drum, a second load-DD pulse sets a 1 in the on-off FF and clears the timing counter in the character timing and intensity circuit.

2.5.1.5 End Display

The Drum System continues the read operation to the DDGE until the words of all slots of the DD group have been read and displayed. The display period will be stopped by slot 106 for the DD 1 cycle and by slot 127 for the DD 2 cycle. When the slot counter in the DD indicator selection section indicates slot number 106 or 127, two conditioning signals are generated and sent to the master control circuit. These are the end-slot DD and end-block DD signals. The combination of these two signals gates an end-word signal from the X-position counter through GT 8 or GT 11. The stop-DD signal thus produced ends the display period by presetting the Y-position counter and by clearing the phase counter in preparation for the next DD cycle.

2.5.2 Character Timing and Intensity Circuit

The character timing and intensity circuit is basically a timing device used by the generator element to produce an 80-μsec intensification gate and to control character timing sequence. The basic component of the circuit is a 6-stage counter whose output combinations perform specific functions.

As shown in figure 3–23, seven input signals are applied to the timing counter: clear-timing-counter, add-1-to-timing-counter, initiate-DD, end-word, clear- or test-clear-intensity-control, OD 1, and OD 3 signals. The clear-timing-counter signal is the load-DD input to the master control circuit and is sent to the timing counter at the same time that a word is sent to the character storage and character register sections. The add-1-to-timing-counter signals are the gated OD 1 pulses from the master control circuit. Since OD 1 pulses recur every 10 μsec, add-1-to-timing-counter signals step the timer every 10 μsec. A stop-DD signal terminates the generation of intensification signals at the end of the display period by cutting off add-1 signals to the counter.

2.5.2.1 Intensification Gate Generation

A 0 time of operation for the character timing and intensity circuit is established by the clear-timing-counter input. (See fig. 3–23.) The first clear signal is generated by the load-DD signal which begins the display period of the DD cycle. Each clear-timing-counter signal clears FF's 1, 2, 3, 4, and 5. Flip-flop 8 is cleared by the clear- or test-clear-intensity-control signal which is a

branch of the clear-timing-counter signal. The timer-equal-3 AND circuit is used to control the generation of the intensification gate. This AND is conditioned by an 1100 combination in FF's 2, 3, 4, and 5. When the AND is conditioned by this combination, GT 4 passes the add-1-to-timing-counter signal gated by GT 1.

The first add-1-to timing-counter signal sets a 1 in FF 1. This flip-flop remains set until the counter has completed its cycle and a second clear-timing-counter signal is received. The second add-1-to-timing counter signal passes GT 1 and sets FF 2 to the 1 side. The third signal passes GT's 1 and 2, sets a 1 in FF 3, and clears FF 2. Four successive add-1 pulses produce an 1100 combination in FF's 2, 3, 4, and 5 to condition GT 4. The fifth add-1-to-timing-counter signal passes gate tubes 1 and 4.

Gate tube 10 is conditioned by the 0 output of FF 8. The first clear-timing-counter (load-DD) signal in a DD cycle which initiates the display period, clears FF 8. An initiate-DD signal at the beginning of the next cycle sets FF 8 and deconditions GT 10. When GT 10 is conditioned, the pulse from GT 4 passes GT 10 to the 1 side of FF 6. The 1 side of FF 6 is used to produce the intensification gate and is fed to all DDIS's. This intensification gate, combined with slot counter outputs A and B (see fig. 3–7, sheet 2, foldout), determines the DDIS to be intensified. The DDIS's are selected in sequential order for intensification.

2.5.2.2 Intensification Gate Cutoff

The intensification gate has a time duration of 80 μsec. Since the gate is established when the fifth add-1-

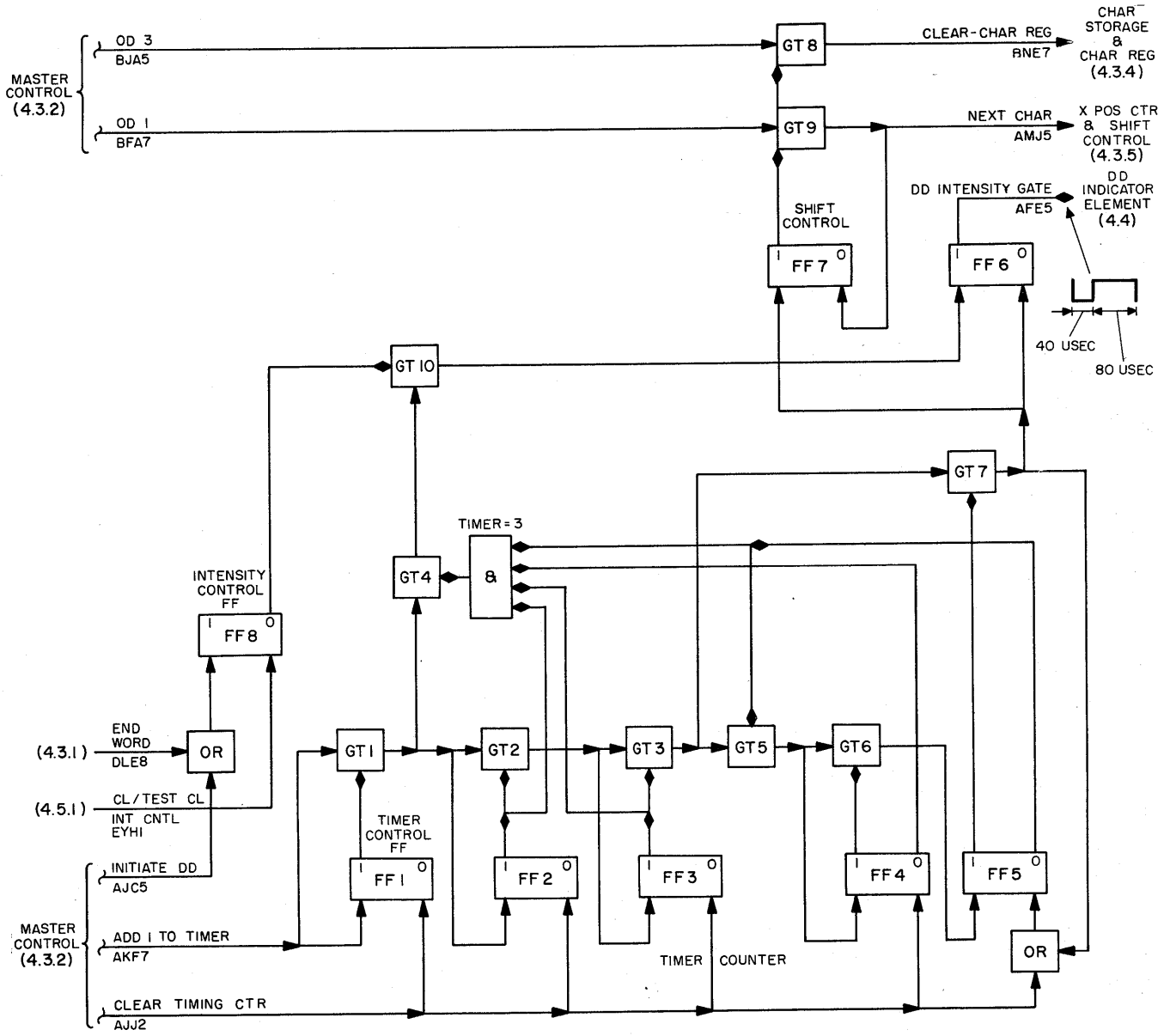


Figure 3–23. Character Timing and Intensity Circuit, Logic Diagram

to-timing-counter signal is received, the gate must be cut off at the 13th signal. This situation will provide an 80-μsec interval. Table 3–3 describes the condition of FF's 1, 2, 3, 4, 5, and 6 for the complete period.

At time 90, a 1 is set into FF 5, deconditioning GT 7. The 10th, 11th, and 12th add-1 signals complement FF's 2 and 3 so that, at the 12th pulse, the flip-flops contain a 111011 combination. The 13th pulse cannot pass GT 5, but does pass GT 7. One output of GT 7 is applied to the 0 side of FF 6, cutting off the intensification gate. Other outputs of GT 7 clear FF 5 and set FF 7. The combination of the flip-flops at this time is 100000. The 16th add-1 signal produces another 111000 voltage combination in the flip-flops of the counter, conditioning the circuit for a second intensification gate. The intensification gate is repetitive every 120 μsec. Each gate corresponds to one character of the word being displayed.

During the display period of the DD cycle, the end-word signal is generated by the X-position counter and shift control circuit at time 620 (coincident with the fifth next-character signal described in 2.4.1.1 of this chapter). Generation of the end-word signal restricts add-1-to-timing-counter signals from the master control circuit. The timing counter remains unchanged until the next clear-timing-counter signal is received. This occurs at time 640 (at time 630 if precessing takes place), when a new word is received from the Drum System.

The intensification-gate cutoff signal, generated at time 130, is also used to time the display of the characters that make up a word. Gate tubes 8 and 9 (fig. 3–23) and FF 7 generate a clear character-register signal and a next-character signal. The clear-character-register signal is applied to the character storage and character register circuit, and the next-character signal is sent to the X-position counter and shift control circuit.

2.5.3 Control Bit Sensing Circuit

The control bit sensing circuit makes use of three AND's and two flip-flops to decode the value of the sign bits in each DD word. Depending upon the values of these sign bits, one of three possible control conditions is established in the sensing circuit. A 01 combination of the left sign bit and right sign bit produces a new slot condition which effects the selection of a DDIS and displays the word in the upper left of the viewing screen. A 10 combination of these bits causes the display word to be positioned at the top line of the opposite side of the viewing screen. When both sign bits are 1, the word is displayed two lines beneath the word previously displayed. The control bit sensing circuit has no control of the display when the sign bits are both 0, and the cycle continues. An OD 3 signal clears the sensing circuit flip-flops after the control function has been exercised. Figure 3–24 is a logic diagram of the control bit sensing circuit.

2.5.3.1 New-Slot Operation

When the left and right sign bits of a word contain a 0 and a 1, respectively, a 01 combination is established in FF's 1 and 2. This combination indicates that a new message is being read into the generator element. The function of the new-slot AND is to sense this 01 combination and to condition GT 1 so that signals may be sent to the remote generator components which prepare the indicator element for the receipt of a new message. Since a word is sent from the Drum System at OD 1 time, GT 1 passes the first OD 3 signal applied to the gate. The output of GT 1 is the new-slot signal and is distributed as an erase signal, a left-half signal, an add-1-to-slot-counter signal, and a clear-Y-counter signal. The add-1-to-slot-counter signal is applied to the slot counter circuit, stepping the counter to a new count, and selecting another slot to display information. The erase signal is fed to the erase gate circuit to establish the erase gate. The left-half signal is applied to the X-position counter; and the clear-Y-counter signal is applied to the Y-position counter. The combined execution of

TABLE 3–3. CONDITION OF CHARACTER TIMING AND INTENSITY FLIP-FLOPS, DISPLAY PERIOD

TIME (in μsec)	FF 1	FF 2	FF 3	FF 4	FF 5	FF 6
0	0	0	0	0	0	0
10	1	0	0	0	0	0
20	1	1	0	0	0	0
30	1	0	1	0	0	0
40	1	1	1	0	0	0
50	1	0	0	1	0	1
60	1	1	0	1	0	1
70	1	0	1	1	0	1
80	1	1	1	1	0	1
90	1	0	0	0	1	1
100	1	1	0	0	1	1
110	1	0	1	0	1	1
120	1	1	1	0	1	1
130	1	0	0	0	0	0
140	1	1	0	0	0	0
150	1	0	1	0	0	0

these signals positions the first word of a new message in the upper left of the selected slot.

2.5.3.2 Other-Half Operation

A 10 combination in the sign bits of a word positions the word, as well as the remaining words of the slot, on the other side of the selected indicator slot. The 10 combination in FF's 1 and 2 is sensed by the other-half AND. This circuit conditions GT 2, which gates the next OD 3 pulse applied to GT 2 after the word is received from the Drum System.

The output of GT 2 is applied to a flip-flop in the X-position counter and shift control circuit. This signal is called an other-half signal, and its function is to condition the X-position counter and shift control circuit so that the remainder of the message will be displayed on the other half of the display tube viewing screen. Hence, the other-half signal, together with the clear-Y-counter signal, causes the word to be displayed on the top line of the other column of the selected display tube.

2.5.3.3 Skip-Line Operation

A 1 in both the left and right sign bits of a word causes the selected display tube to display the next word two lines below the word previously displayed. The skip-line AND is used to sense the 11 combination in FF's 1 and 2. Gate tube 3 is conditioned by this AND and passes an OD 3 pulse as a skip-line signal. This signal is applied through the master control circuit to the Y-position counter, stepping the counter by one count. Since the counter had previously been set by the end-word signal generated during the processing of the previous word, the display skips one line.

2.5.4 Erase Gate Circuit

The function of the erase gate circuit is to generate an erase gate which may be used with the DDIE selection signals to erase messages previously displayed. The circuit consists of two basic parts: one part establishes the erase gate, and the other determines the termination of the erase gate. The initial erase gate produced by the

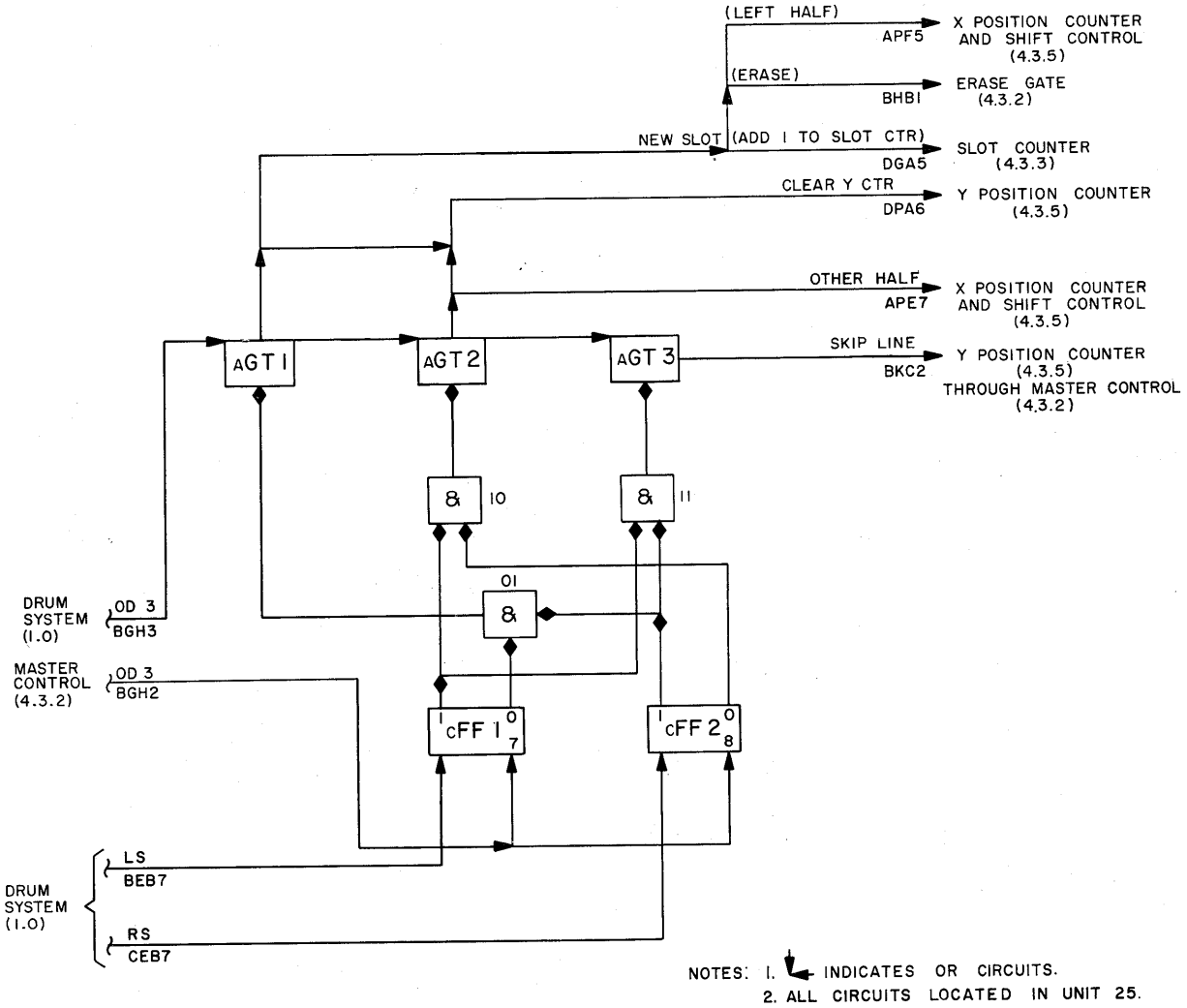


Figure 3–24. Control Bit Sensing Circuit, Logic Diagram

generator element occurs during the delay period of the DD cycle. This gate has a duration of 2,280 μsec. Each gate generated during the display period of the cycle is 2,400 μsec in length. Timing of the erase gate is dependent upon the next-character signal generated by the character timing and intensity circuit. Figure 3–25 is a logic diagram of the erase gate circuit.

2.5.4.1 Erase Gate Generation

The first erase gate is generated during the delay phase of the initial period. The initial-erase signal generated in the master control circuit sets FF 1 in the erase gate circuit, thereby conditioning GT 1. After the initial-erase signal, the first next-character signal is generated. The next-character signal, occurring 120 μsec after the initial-erase signal, is applied to the X-position counter and shift control circuit to produce a sense-erase signal which is applied to GT 1 and to the 0 side of FF 1. This sense-erase signal passes GT 1, sets FF 2, and also clears FF's 3 and 4. When FF 2 is set, the erase gate is initiated. (See fig. 3–25.)

During the display period of the DD cycle, the new-slot signal from the control bit sensing circuit sets FF 1. The next-character signal, which shifts the I character of the first word of a slot, also generates a sense-erase signal. This occurs 140 μsec after the clear-timing-counter (load-DD) signal is received by the character timing and intensity circuit. The sense-erase signal is applied to conditioned GT 2 and to the 0 side of FF 1. The output of GT 1 sets FF 2, establishing the erase gate during the display period.

2.5.4.2 Erase Gate Cutoff

A 2-stage counter in the erase gate circuit is used to cut off the erase gate. This counter is cleared by the sense-erase signal, gated through GT 1, and is stepped by the end-word signal produced by the X-position counter and shift control circuit. End-word signals occur at a time coincident with every fifth next-character signal. The first end-word signal is applied to the counter 480 μsec after the erase gate is established.

During the delay phase of a DD cycle, the timing counter in the character timing and intensity circuit is not cleared while it is being recycled. As a result, the three remaining end-word signals required to clear the erase gate counter and cut off the erase gate occur at

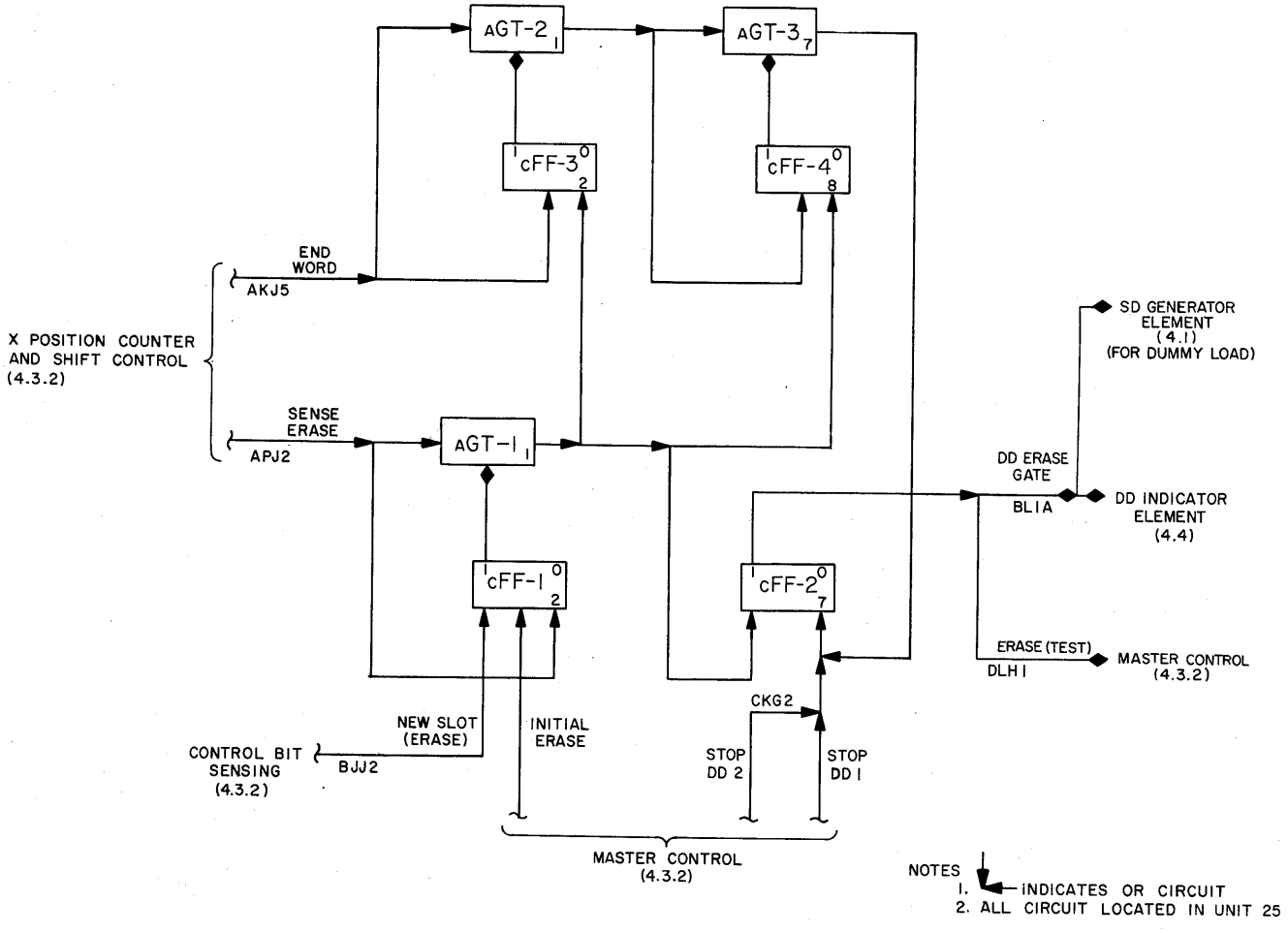


Figure 3–25. Erase Gate Circuit, Logic Diagram

600-μsec intervals. The fourth end-word signal applied to the counter is gated by GT's 2 and 3 to the 0 side of FF 2, cutting off the erase gate. The duration of the initial erase gate is, therefore, 2,280 μsec.

Operation of the erase gate counter during the display period is the same as that described for the delay phase, except that the timing of the end-word signals is altered. The first end-word signal is received 480 μsec after the sense-erase signal, as in the delay phase. There is a delay of 20 μsec before the next word begins. Therefore, the second end-word signal is received 640 μsec after the first. Similarly, 640-μsec intervals elapse before the third and fourth end-word signals are received. The fourth end-word signal clears FF 2, cutting off the erase gate 2,400 μsec after the gate is established.

At the end of the display period, a stop-DD signal from the master control circuit clears FF 2. This action prepares the erase gate circuit for the next DD cycle. Note that the last sense-erase signal of the display period clears FF 1. Flip-flop 1 is set by the initial-erase signal of the next DD cycle. Figure 3–26 shows the time duration of the erase gate for the initial period and display period.

2.5.5 Contrast Gate Circuit

The contrast gate circuit is a 6-stage binary counter with a seventh flip-flop which produces a 10-μsec gate

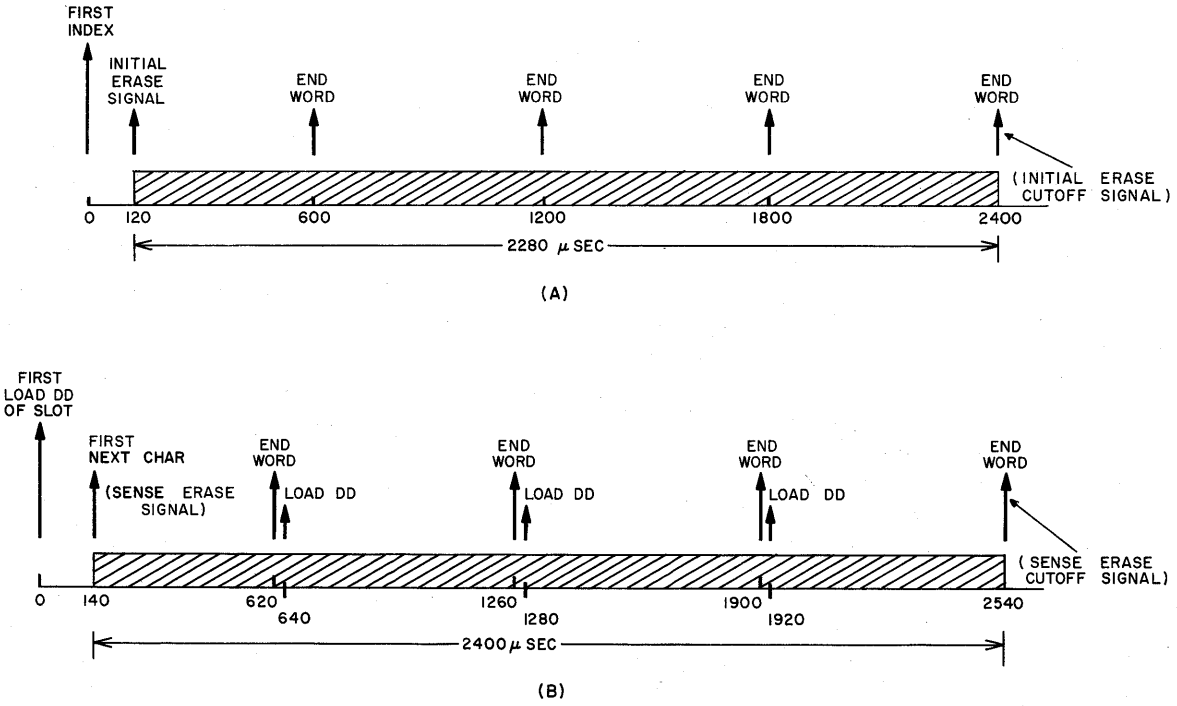


Figure 3–26. Erase Gate Timing

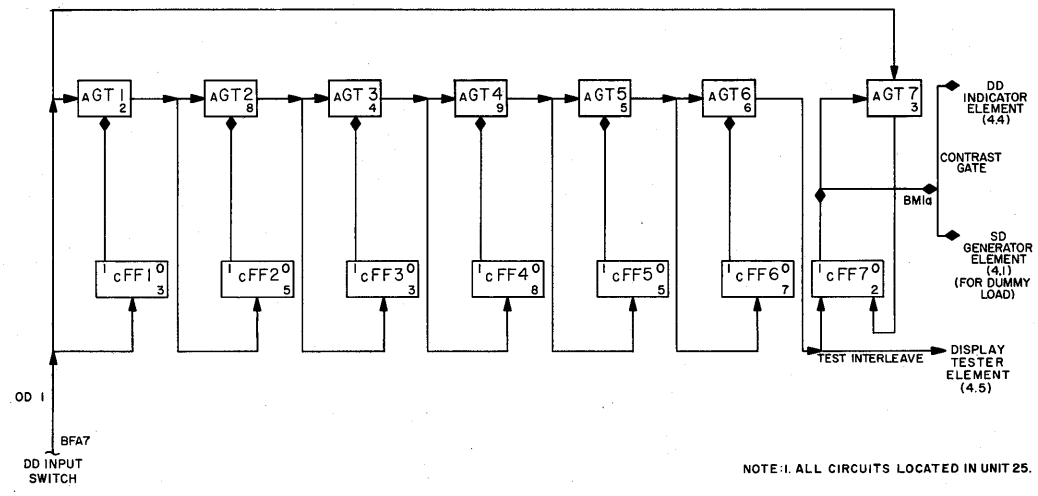


Figure 3–27. Contrast Counter, Logic Diagram

once every 640 μsec of generator element operation. This gate is applied simultaneously to all of the display tubes of the indicator element, resulting in an improvement of the contrast between the used and unused portions of the viewing screen. OD 1 pulses are used to generate the contrast gate.

As shown in figure 3–27, the contrast counter operates as a conventional binary counter. Sixty-three OD 1 pulses are required to establish a 111111 combination in the six flip-flops of the counter. The 64th pulse sets FF 7 and clears the first six flip-flops. This action conditions GT 7 at the same time that it establishes the contrast gate. The 65th OD 1 signal sets FF 1 at the same time that it is gated to the 0 side of FF 7, cutting off the gate. Since OD 1 pulses occur every 10 μsec, the time duration of the contrast gate is 10 μsec, with a recurrence rate of 640 μsec of element operation. The output of GT 6 is applied to the DD input switch as a test-interleave signal. This signal is utilized by the DTE during test operations.

SECTION 3
OVERALL TIMING OF DD ELEMENTS

3.1 TIMING AND CONTROL OF DD ELEMENTS

Timing of the DDE's is dependent upon the timing and control signals received from the Drum System. A brief summary of timing and control signals follows. Index pulses are received from the Drum System every time the MIXD drum completes a revolution. The index recurs at 20,480-μsec intervals. Other basic timing pulses generated by the Drum System are the OD 1 and OD 3 pulses, which recur at 10-μsec intervals.

The first OD 1 pulse after index time follows the index pulse by 5 μsec. The OD 3 pulses are generated 5 μsec after the OD 1 pulses. Reading of a DD word from the Drum System is initiated every 640 μsec, and the drum contains a maximum of 2,048 words.

In essence, the operational timing and control signals for the DDE's are the signals from the Drum System. It is these basic signals which initiate the functional operations necessary during the initial and display periods of the DD cycle.

3.2 CHARACTER PROCESSING

At OD 1 time, the Drum System sends a load-DD signal, gated by the master control circuit, to the character timing and intensity circuit in the DDGE. This signal is known as the clear-timing-counter signal and clears the timing counter. The H character in the DDGE is processed differently from the rest of the characters. Binary selection bits for the first character of the word (character H) are sent directly to the character register from the drum. The binary values are converted into analog voltages, selecting the desired character at the DD CRT. When the H character has been intensified, it is cleared out of the character register. The binary selection bits for characters I, J, K, and L are sent to character storage when they are received from the Drum System. They are shifted into the character register sequentially by the appropriate character-shift signals. While each character is in the register, the character selected at the DD CRT is intensified. After the intensification of one character, the register is cleared in preparation for the next character.

3.2.1 Character Timing, Display Period

The intensification-gate cutoff signal generated at time 130 is used to time the display of characters of the word. (See fig. 3–28.) The cutoff signal sets FF 7 (fig. 3–23), thereby conditioning GT's 8 and 9. Since the cutoff signal is in essence an OD 1 pulse, the OD 3 input will pass GT 8 before the OD 1 pulse is applied to GT 9. Thus, a clear-character-register signal is developed at approximately time 135; i.e., 135 μsec after the word is received from the Drum System. When the OD 1 pulse passes GT 9, FF 7 is cleared and the X-position counter and shift control circuit receives a next-character signal. This signal is generated at time 140. A clear-character-register signal is generated 135, 255, 375, 495, and 615 μsec after each display word is received by the generator element. The next-character signal is produced 140, 260, 380, 500, and 620 μsec after the word is received.

The condition of FF's 1 through 6 (fig. 3–23, table 3–3) at time 620 is the same as at time 140; i.e., 110000. Since the end of the display period coincides with an end-word signal, the combination existing at the end of a display period is 110000.

3.2.2 Character Timing, Initial Period

No add-1-to-timing-counter signals are generated after a display period ends. Beginning with the next DD cycle, the flip-flop combination, as explained above, is 110000. The first add-1 signal of the new cycle is generated by the OD 1 signal that follows the first drum

index pulse received. The 11th add-1 pulse is generated 110 μsec after the drum index pulse is received. As a result of the eleven add-1 pulses, the flip-flop combination is 100000. This combination conditions GT 9 (fig. 3–23) which gates the next OD 1 signal as a next-character signal. Because no clear-timing-counter signals occur during the initial period, next-character signals are generated at 120-μsec intervals as long as add-1 signals are received. Every fifth next-character signal produces an end-word signal; the end-word signals are generated at 600-μsec intervals during the delay phase. The intensity gate is generated because the intensity circuit is operating; however, since the slot counter is set at 0 and there is no DDIS assigned to slot 0, no DDIS is intensified.

3.3 WORD PROCESSING

All characters processed in the DDGE are put into words. The processing of the word begins with the load-DD signal from the Drum System. The end of a word is signified by an end-word signal received from the X-position counter. At the end of a word, the Y-position counter is advanced and the character storage and character register flip-flops are cleared in preparation for the next word. Since the time required to process the H character is 140 μsec and the time required to process the other four characters is 120 μsec each, the time from the start of a word to the end of a word is 620 μsec. When a DD cycle is initiated, words are read out consecutively, one every 640 μsec. The 20-μsec delay between words is used for precessing the drum at index time.

3.4 SLOT PROCESSING

The words processed are displayed in slots. A new slot is started by the first word in the slot. The 01 combination in the LS and RS bit positions of this word causes the control bit sensing circuit to send a signal to advance the slot counter by 1. This action selects another DDIS (or slot) to display the next DD message on its viewing screen. Simultaneously, an erase gate is generated to erase still another DDIS, making this second DDIS ready to receive data when

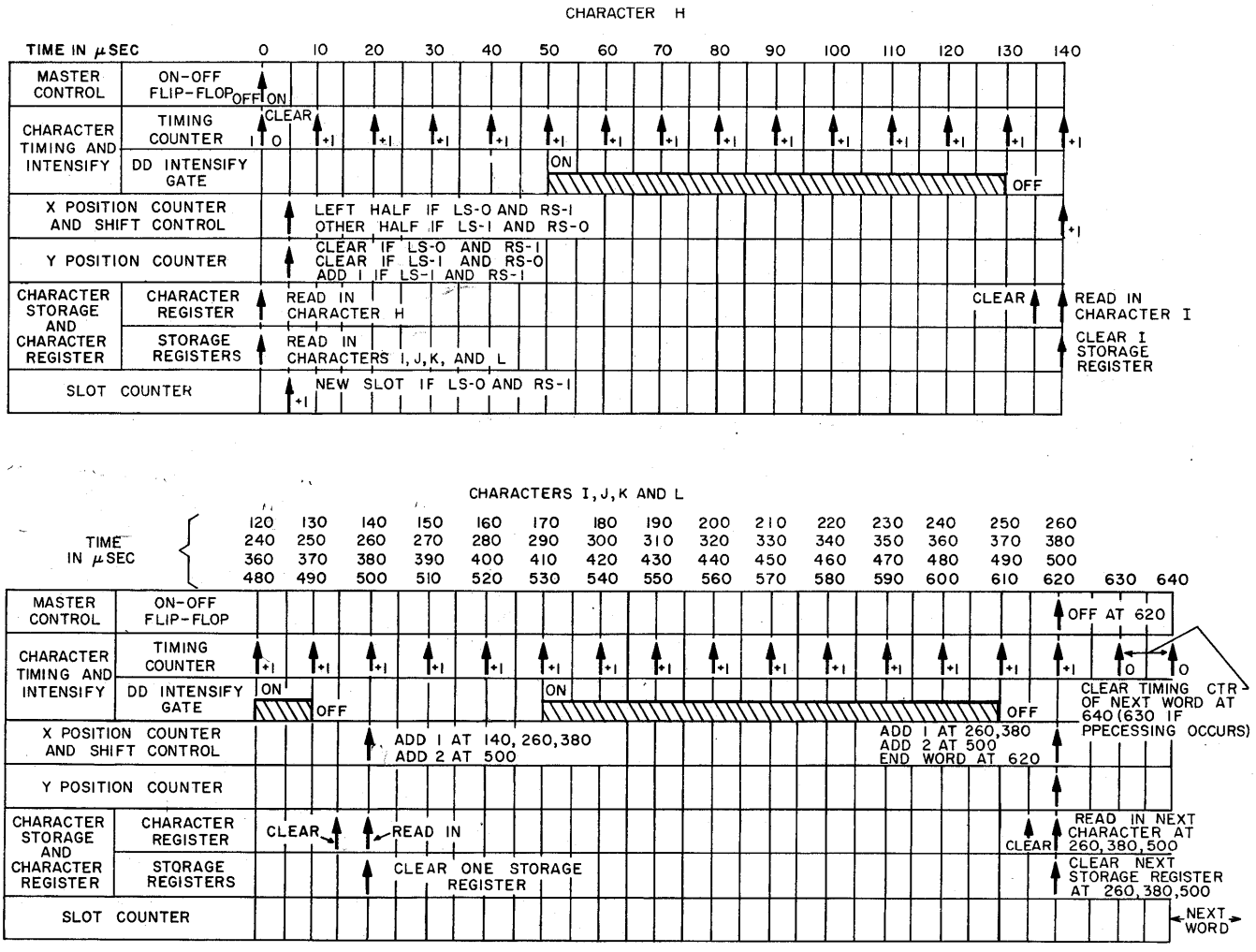


Figure 3–28. DD Timing for All Words

it is selected for display. The length of a slot is determined by the number of words assigned. This may be any number of words from 4 to 32. The minimum word assignment is dictated by the time required to generate the erase gate; the maximum is established by the capacity of the DD CRT word storage.

3.5 CYCLE PROCESSING

The slots processed are either in the DD 1 or the DD 2 cycle. Both cycles are initiated by the Central Computer in a similar manner. When a cycle is started, the master control section distributes the control signals necessary for DDGE operation: the slot counter is set for DD 1 or DD 2, and the initial erase gate is generated. Each slot of the appropriate cycle is then selected sequentially to display its assigned information. When it is time for the cycle to stop, the master control is set so that the DDGE will not operate until the next cycle is started, the erase gate is cut off, and the Y-position counter is preset. The cycle of operation is stopped by the last slot. Only one word is used for this slot; it is not displayed, but is used only for stopping the cycle. This word contains the control bits required to advance the slot counter (LS-0 and RS-1). This makes the end-block signal coincide with the end-slot signal. These two signals are combined in the master control circuit to produce the stop-DD signal.

3.5.1 Timing of Initial Period

Figure 3–29 presents a graphic illustration of the initial period of the display cycle. The function of this portion of the cycle is to synchronize generator element operation with Drum System operation and to erase the DD tubes which are selected when the slot counter is 0. To erase the CRT's, an initial erase gate of 2,280 μsec is generated (refer to 2.5.4 of this chapter). Drum reading is delayed after the erase gate for a period exceeding the 200 ms required for complete erasure of the previous display. The phase counter in the master control circuit remains in a delay condition until the 11th drum index pulse is received from the Drum System. During this interval, the generator element produces all the gates and timing signals required for operation except the intensification gate to the indicator element.

The initial erase gate is established 120 μsec after the first drum index signal is received. At this time, the first next-character signal is generated by the char-

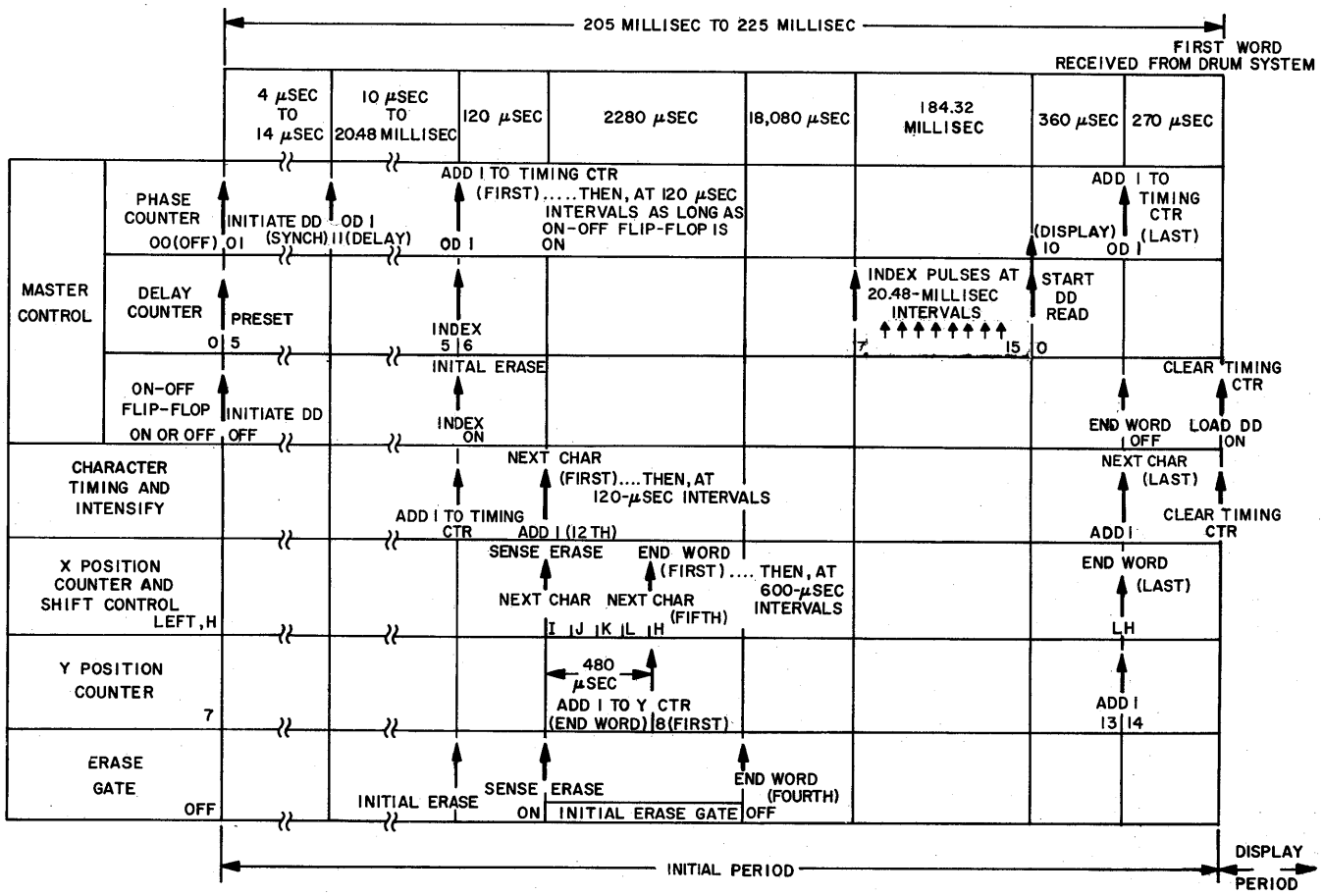


Figure 3–29. Initial Period of DD Cycle, Timing Chart

acter timing and intensity circuit. These shift signals recur at 120-μsec intervals during the delay phase. An add-1 signal is fed to the Y-position counter 480 μsec after the first shift signal is developed and at every fifth shift signal thereafter.

When the 11th drum index pulse is received by the generator, the delay counter in the master control circuit sends a start-DD-read signal to the Drum System. After 63 drum registers are skipped, the 64th register is read out to the DDGE. At the same time that the 64th register is read, the Drum System sends a read-sample (load-DD) signal which clears the timing counter in the character timing and intensity circuit and sets the on-off flip-flop in the master control circuit. A period of 270 μsec before this signal is received, the last end-word pulse produced during the delay period steps the counter in the erase gate circuit at the same time that it steps the Y-position counter. No further shift (next-character) signals are generated by the character timing and intensity circuit.

3.5.2 Timing of Display Period

The display period of the DD cycle begins 630 μsec after the phase counter has been set to the display phase. At this time, the read-sample (load-DD) signal, as well as the 32 information signals which comprise the word, are received from the Drum System. Figure 3–29 illustrates the condition of the generator. The word is read into storage, the on-off flip-flop is set to on, and the flip-flops which comprise the timing counter in the character timing and intensity circuit are cleared. This is shown as time 0 in the timing chart. Five μsec later, at OD 3 time, the slot counter and the X-position counter and shaft control circuits are stepped by the LS and RS combination of the display word. The Y-position counter is cleared by this action.

The character timing and intensity circuit generates an 80-μsec intensification gate at time 50. Five μsec after this gate is cut off (at time 135), a clear-character-register signal clears the character register in preparation for the shift operation that will shift the I character from storage into the register. During this first 135-μsec period, the H character has been applied to the character decoder and displayed on the selected indicator slot. The shift-I signal is generated at time 140, and initiates the transfer of the I character. The remaining characters (J, K, and L) are shifted from character storage to the register at 120-μsec intervals. A period of 620 μsec is required to read one word from the Drum System and apply the word, in analog form, to the selected slot in the indicator element. The end-word signal generated by the fifth next-character pulse is fed to the Y-position counter as an add-1 signal, which prepares the indicator element for the position of the next word.

When the last slot in the DD group has been displayed, end-block and end-slot signals are combined in the master control circuit with the end-word signal. As a result, a stop-DD signal is produced which ends the display period. At this time, the various counters in the timing and control section are prepared for the next DD cycle.

PART 4
SITUATION DISPLAY ELEMENTS

CHAPTER 1
SITUATION DISPLAY PRESENTATION

1.1 GENERAL

The situation display (SD) elements in the Display System provide a visual presentation of the information communicated to it by the Central Computer System. This information is rapidly changing air-attack intelligence and is presented on a display tube in the form of a plan-position display. The display shows primarily the correct locations of moving targets and their geographical relationship to fixed points and/or other moving targets.

1.2 TYPES OF MESSAGES

The output, or the graphic representation on the viewing screen of the SD CRT, appears as a message in the form of individual characters or vectors. The message may consist of a single symbol or of a group of symbols relating to one point or target; it may be a single vector describing location or a combined group of vectors and other characters designating the direction and speed of a target, its height, track number and identification.

The air situation thus shown is interpreted and reduced by operator personnel. The display reflects existing and changing air-tactical conditions.

The illustration in figure 4–1 shows a typical SD CRT with the four basic types of messages that may be displayed. These are designated radar data (RD), track data (TD), TD tabular information, and TD vector messages.

Figure 4–2 shows a typical TD tabular track message. This type of message contains a vector and up to 13 characters. Referring back to figure 4–1, it will be seen that this type of message has a point which shows the present position of an aircraft, with the vector indicating the speed and heading of the aircraft. The letters and characters in this message provide identification and other data about the aircraft.

Figure 4–3 depicts a typical TD tabular information message. Messages of this type contain up to 13 characters. In figure 4–1, this type of message uses a symbol and letters to indicate the location of airfields and other geographical locations.

Figure 4–4 shows typical displays of TD vector messages. This type of display consists of four vectors (V1 through V4), with four characters adjacent to the origin of the last vector. In figure 4–1, this type of display is used to indicate an aircraft flight plan and also to form an attention-getting box.

Figure 4–12 shows a typical radar message with each of the 8 categories. Each display consists of eight radar returns. Of the eight returns, seven are "history" and are dimly displayed. The eighth return is the present return and is brightly displayed.

1.3 TD TABULAR TRACK MESSAGE DISPLAY FORMAT

The complete format pattern of a TD tabular track message when displayed on the SD CRT is shown in figure 4–5. Each box of the format represents one character of the message. Each character is identified by a letter with a numerical subscript to identify its position in the message.

In this tabular track message format, each group of characters bearing the same letter designation is referred to as a feature. There are A, B, C, D, and E features, each of which contains information. In addition, the point shown in the E feature is referred to as the point feature. The vector is an additional source of information, but is not considered a feature.

The feature is significant in that it represents a particular type of air-defense information. The E (point) feature represents the present location of an aircraft. The A, B, C, and D features represent the present location of an aircraft. The A, B, C, and D features represent other computer-resolved information about the aircraft, such as track number, velocity, and altitude. Although the vector is not a feature, its direction indicates the direction of the aircraft and its length indicates the speed of the aircraft.

Particular features and characters may be omitted from a displayed track message at the discretion of the console operator. This is possible because the features are wired through selection switches at the SD consoles. With these selection switches, the operator can display

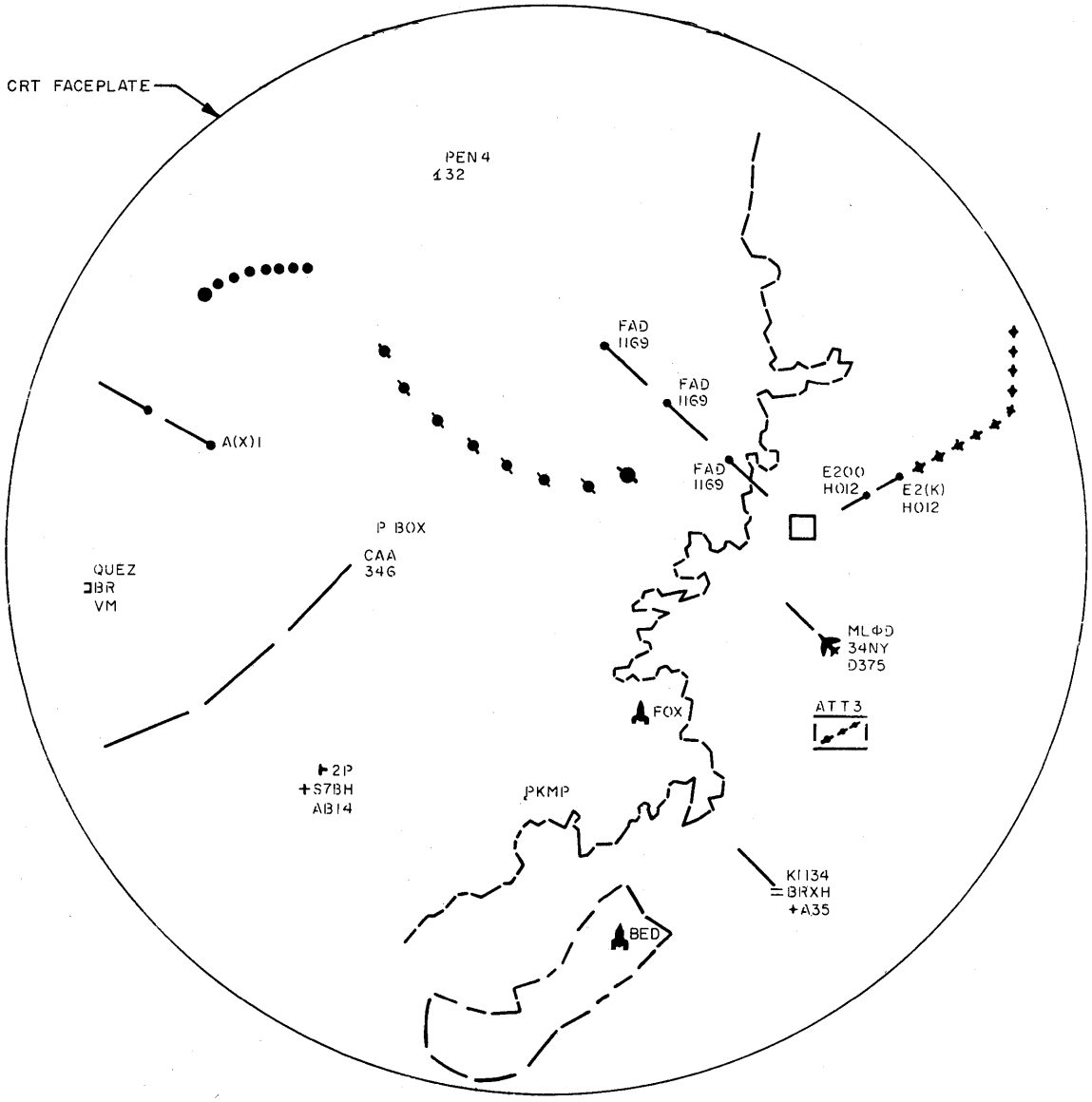


Figure 4–1. Typical Situation Display

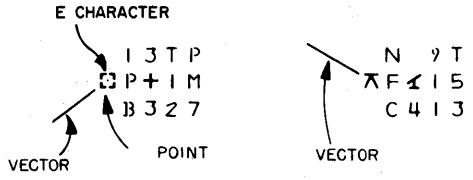


Figure 4–2. Typical TD Tabular Track Message Displays

or suppress any of the five features (A, B, C, D, and E) supplied to his console, with the exception that both the A and B features cannot be displayed simultaneously.

A vector is started with its origin at the point feature and is swept some distance in a direction determined by the $\dot{X}$ and $\dot{Y}$ values of the vector. The direction that the vector is swept from the E feature (central point) partly determines whether the other features will be located left of, right of, above, or below the E feature. Message positioning in relation to the vector is also determined by a position bit generated by the computer. If this position bit is 0, the E feature is positioned left or right of the other features. Whether the

Figure 4–3. Typical TD Tabular Information Message Displays

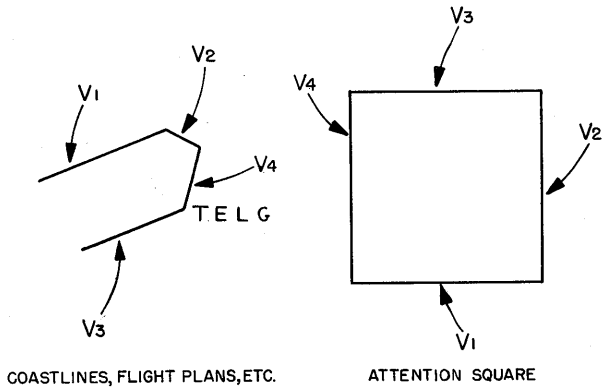


Figure 4–4. Typical TD Vector Message Displays

E feature is positioned on the left or right, then, depends on whether the $\dot{X}$ value of the vector is positive or negative. If the $\dot{X}$ value is negative, the E feature is positioned on the left; if the $\dot{X}$ value is positive, the E feature is positioned on the right (see top portion of fig. 4–6). If the position bit is 1, the E feature is placed either above or below the rest of the features. The $\dot{Y}$ value of the vector determines this. If the $\dot{Y}$ value is negative, the E feature falls below; if the $\dot{Y}$ value is positive, the E feature is placed above the rest of the features (see bottom portion of figure 4–6). The sequence in which the parts of the TD tabular track message are generated is shown in figure 4–7.

1.4 TD TABULAR INFORMATION MESSAGE DISPLAY FORMAT

As indicated in figure 4–8, the TD tabular information format is similar to that of the TD tabular track message. There are, however, two distinct and important differences. First, this format is different because there is no vector generated. Second, the character groups are not called features, they are not selected by the operator, and there are only four groups (A, C, D, and E). Otherwise, the TD tabular information message is similar to the TD tabular track message.

1.5 TD VECTOR MESSAGE DISPLAY FORMAT

Figure 4–9 illustrates the format for the TD vector message display. It shows the four vectors and the G character group. The four vectors are generated, and then the character group is positioned in relation to the fourth vector.

Each vector is swept from a point of origin (central point) designated by X and Y, in a direction and for the distance determined by the $\dot{X}$ and $\dot{Y}$ values. The subscripts indicate the sequence in which the vectors are generated. Subscript 1 designates the first vector, subscript 2 designates the second vector, etc.

After the fourth vector has been generated, the four G characters are positioned adjacent to the point of origin (central point X4, Y4) of the fourth vector.

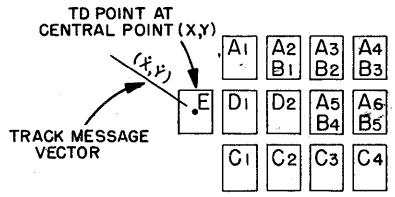


Figure 4–5. TD Tabular Track Message Format

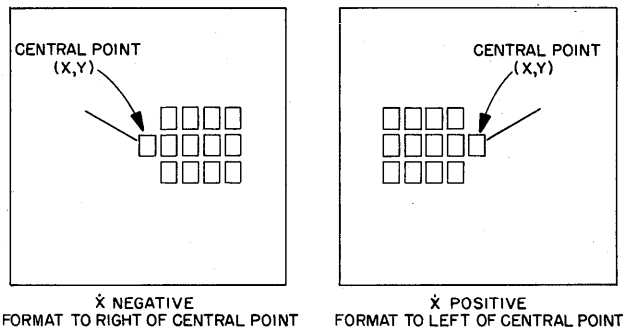


Figure 4–6. Format Positioning of TD Tabular Track Message

Relative positioning of the G characters in respect to the central point of vector 4 is determined by the values of X4 and Y4. Figure 4–10 shows the four possible positions of the G characters and lists the corresponding X4 and Y4 values needed for each position.

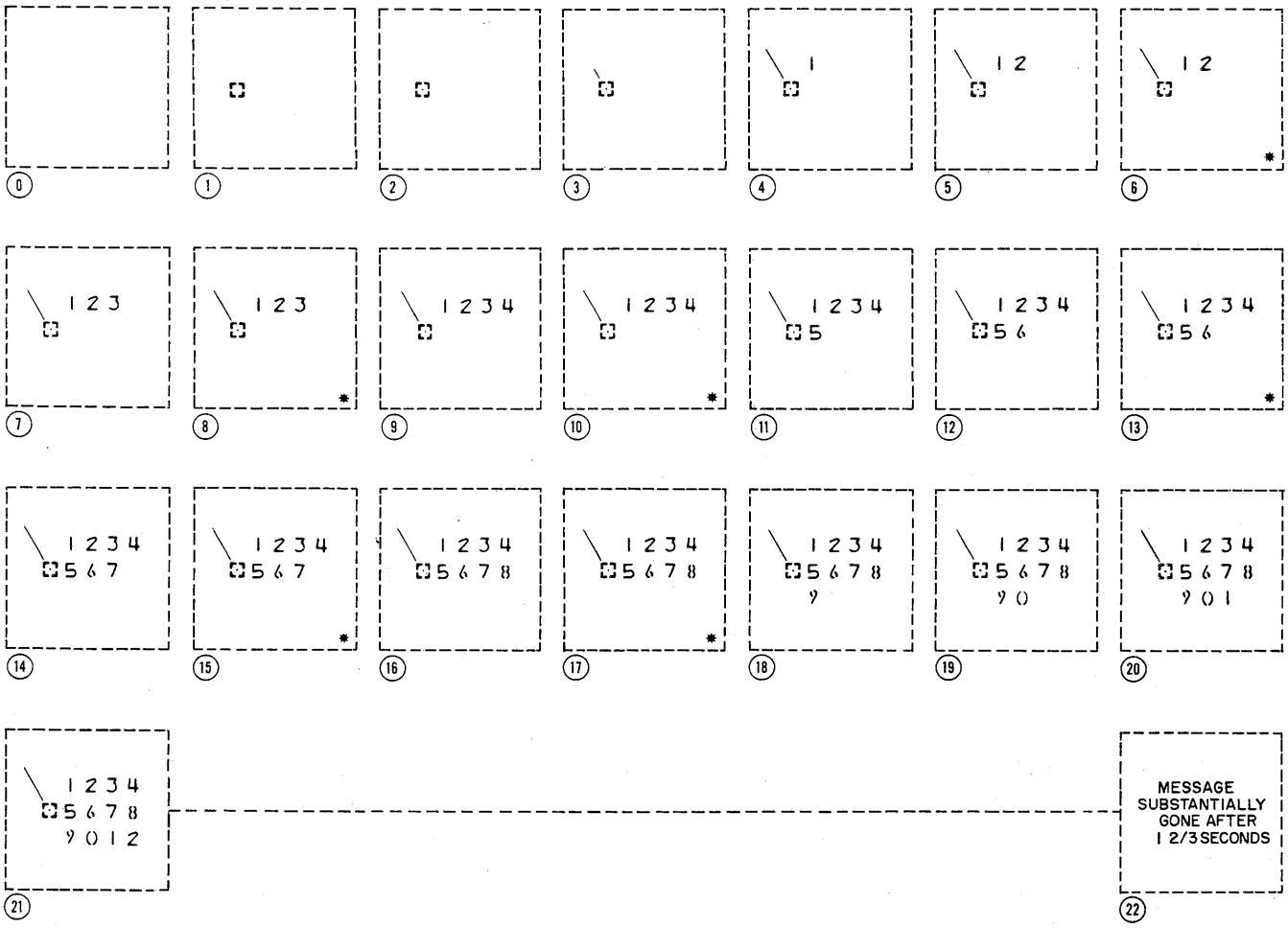
1.6 RADAR DATA MESSAGE DISPLAY

Each radar target return reported to a Combat Direction Central is prepared in the Central Computer System for presentation by the Display System to observer personnel.

When a given target report is entered into the Central Computer, the target co-ordinates are converted to rectangular co-ordinates. (Radar polar co-ordinates must first be converted to rectangular co-ordinates with respect to the sector reference point.) The rectangular co-ordinates are then placed on one of the nine fields of the RD drum as an RD message. Note that each such set of data is considered to be a single message; i.e., a 1-word message.

1.6.1 RD Message Contents

The RD message received by the Display System is converted into analog voltages and displayed on the SD CRT. The message is displaced from the center of the viewing screen by horizontal and vertical distances determined by the X and Y co-ordinates, respectively. This displacement is proportional to the displacement of the target from the sector reference point along a parallel and a meridian. For targets to the west or to the south of the sector reference point, the X or Y co-ordinates would be negative. In effect, the message is displayed in the same manner that a point is plotted on a 4-quadrant graph. The RD message data on the RD drum must, therefore, contain the X and Y co-ordinate of the target.



* NOTE: NO CHANGE IN THIS INTERVAL. (ALLOCATED TO DISPLAY OF ONE CHARACTER IN ALTERNATE (B) FEATURE GROUP).

Figure 4–7. Time Sequence of Character and Vector Generation for a Typical TD Tabular Track Message

The method used in writing and reading the RD drum provides an age classification of RD messages into present radar data and history radar data. Of the nine fields on the RD drum, only eight are read by the Display System during one of the 2.6-second display cycles. The ninth is held for writing new messages from the Central Computer System. The fields, numbering from one to nine, are written on in numerical order. Thus, field 1 usually contains older information than field 2, field 2 usually contains older information than field 3, etc. When field 9 has been written on, writing is again initiated on field 1, replacing the oldest history information on the drum with the newest (present) information. RD drum reading by the Drum System starts with the field following the one being written on by the Central Computer and continues with the other seven fields in numerical sequence. Thus, field 1 is read after field 9, and so on. RD data messages are displayed in the order of their age, the oldest first, and the most recent last. To indicate the age of the messages as they are being displayed, the last field (most recent) supplies a display-bright signal, making the present message display bright on the viewing screen. The seven preceding messages (containing older history) always appear comparatively dim.

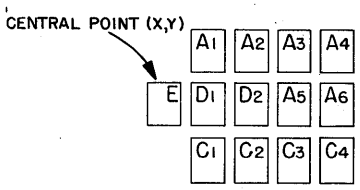
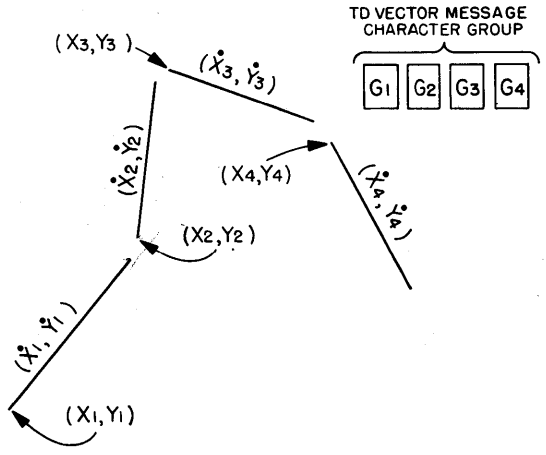
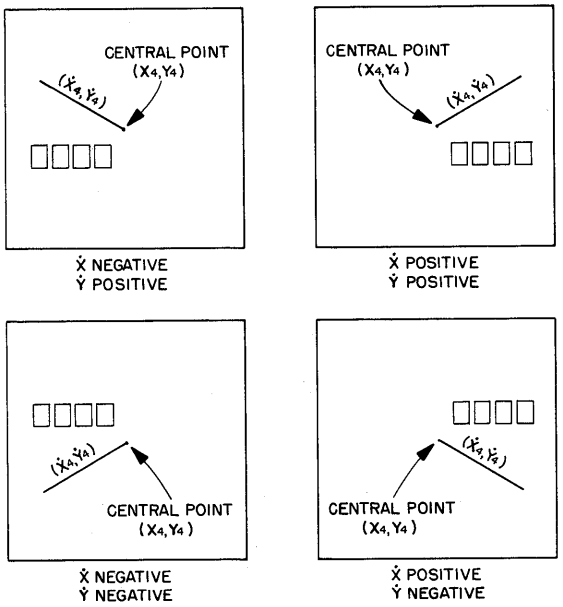


Figure 4–8. TD Tabular Information Message Format



EACH OF THE FOUR VECTOR MESSAGE VECTORS CAN APPEAR WITH ANY ORIENTATION AT ANY CENTRAL POINT; MAXIMUM LENGTH APPROXIMATELY 2.1 INCHES. THE G CHARACTER GROUP OCCUPIES A DEFINITE POSITION WITH RESPECT TO THE CENTRAL POINT OF VECTOR 4 (X4, Y4).

Figure 4–9. TD Vector Message Display Format



POSITIONS DEPEND ON SIGNS OF $\dot{X}_4$ AND $\dot{Y}_4$ (COMPONENTS OF VECTOR 4)

Figure 4–10. Format Positioning of TD Vector Messages

As a result of the writing and reading operations described above, the SD CRT presents for any one target a rapid sequence of RD messages that report the position of the target during each of eight, successive writing intervals. The evolution of a typical pattern is shown in figure 4–11 in which the positions of successive readings of the eight RD fields are illustrated. The intervals between successive additions to the display average 1/8 second, which is the approximate reading time for one field.

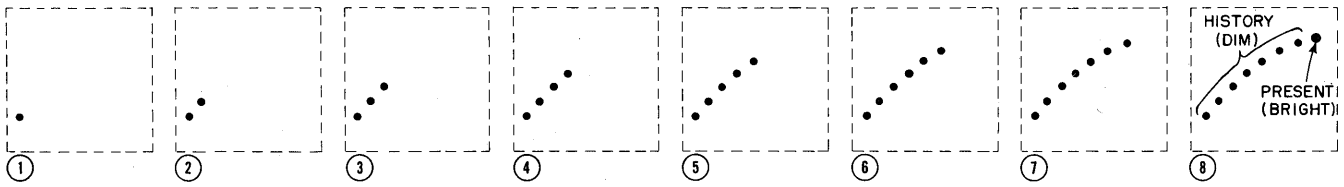
1.6.2 RD Message Categories

There are eight special classes or categories of RD messages, each containing X and Y co-ordinates and distinguished in the Display System by their source, status, and age. Each RD message belongs to only one of the eight categories, and each category has a distinctive display. A symbol represents the source and status of a message; the symbol brightness indicates the age of the message (see fig. 4–12). The categories to be displayed by a given SD CRT are under the control of the operator at that display console. The operator may

choose certain categories for display and suppress all others. The latter statement is subject to two restrictions:

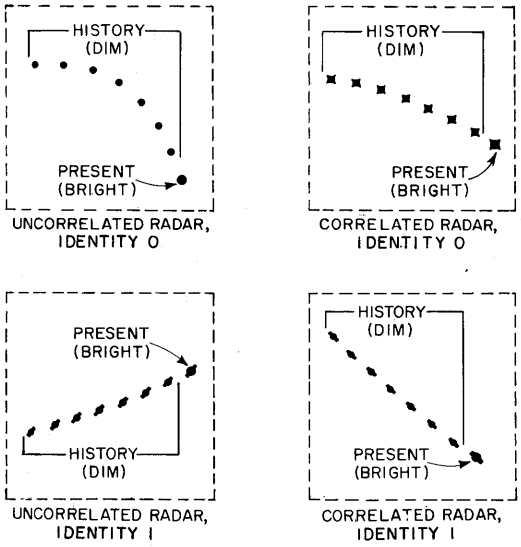
a. The operator cannot choose a particular RD category unless his operating position is wired to receive and display that category. (RD messages are not supplied to the console of an operator whose duties do not require them.)

b. Some SDIS's are wired so that certain categories bypass the selection switches and are forced to display.



NOTE:
1. PRESENT RD-MESSAGE SYMBOLS ARE DISPLAYED BRIGHTER BUT NOT LARGER THAN HISTORY RD-MESSAGE SYMBOLS.
2. SYMBOLS APPEAR EVERY 1/8 SECOND ON THE AVERAGE. DISPLAY OF NEXT PATTERN STARTS AFTER APPROXIMATELY 2-2/3 SECONDS; EITHER REPEATING PREVIOUS PATTERN OR REPORTING A NEW PRESENT POSITION.

Figure 4–11. Evolution of a Pattern of RD Messages



NOTE:
PRESENT RD-MESSAGE SYMBOLS ARE DISPLAYED BRIGHTER BUT NOT LARGER THAN HISTORY RD-MESSAGE SYMBOLS.

Figure 4–12. RD Message Displays, Showing Samples of the Eight RD Categories

CHAPTER 2
SITUATION DISPLAY INDICATOR ELEMENT

2.1 INTRODUCTION

The situation display indicator element (SDIE) is made up of all the situation display indicator sections (SDIS's). The SDIS is primarily the SD CRT, with its associated circuits and controls. Information from the SDGE is displayed on the face of the cathode-ray tubes so that the operators can interpret the prevailing air defense area for interceptor flight-path instructions. Each SDIS is located conveniently for the operators at an SD console.

2.1.1 SDIS Inputs

All the inputs to the SDIE come from the SDGE, either as information signals or control signals.

The information signals consist of 34 signal lines of X, Y digital voltages (d-c levels of +10 or −30V) for use in positioning the SD messages on the SD CRT. Also included as information signals are the eight lines of analog voltages, four for positioning of characters and four for vector deflection.

Control signals are distributed as d-c levels for use in generation and selection of displays.

The following three signals are provided to enable the SD CRT to display the SD message:

a. One line – An intensify signal during character or vector display.

b. One line – A defocus signal during character generation (except for point and vector generation).

c. One line – A defocus signal during character generation (except for point and vector generation).

The following types of signals (also d-c levels) are distributed to the consoles to enable the selection of the various types of situation displays:

a. Seven lines – Features (to all consoles)

b. Thirty-one lines – Track categories (including one test category)

c. Ninety lines – DAB's

d. Up to 45 lines – Mixed TD category of DAB's (supplementary drivers)

e. Two lines – Mix all categories; mix all DAB's

Of the possible 188 DAB and CAT lines, a maximum of 27 may be brought into any signal console. All remaining signals to the SD console are concerned with the generation and positioning of the individual message.

2.1.2 SDIS Outputs

The outputs from the SDIS are the same as the displays explained in Chapter 2 of this part.

2.1.3 Situation Display CRT

The SD CRT is capable of displaying a number of different types of information. It can generate vectors to indicate aircraft direction and speed, aircraft flight plans, and geographical borders. It can also generate characters to indicate information about an aircraft, intercept point, geographical object, etc. The information supplied is constantly redisplayed in a cyclic manner to keep the SD CRT up to date with the latest information being received by the SD subsystem.

The complete operation of the SD CRT is explained in Part 2.

2.2 THEORY OF OPERATION

This chapter discusses the SDIE as it is broken down into its logical functions. These functions are illustrated in figure 4–13. A more detailed discussion of each functional unit in the block diagram will be found in paragraph 2.3 of this chapter.

The messages received from the Drum System by the SDGE consist of eight digital words (TD message), or one digital word (radar track message). When the message goes to the SD console, it is composed of both digital and analog signals. Of these, a certain number are information signals, and a certain number are control signals. The information signals are of two kinds, digital and analog. For instance, the character selection and position signals are analog, while the message positioning signals are digital. The control signals are all digital signals consisting of feature, and CAT and DAB gates which determine whether the message can be displayed at a particular console. Thus, the control signals within a message determine whether the information signals within the message can be displayed.

2.2.1 Character Selection

The character-forming matrix is a metal disk containing the 63 cut-out characters shown in figure 2–8. These characters have been etched through the metal

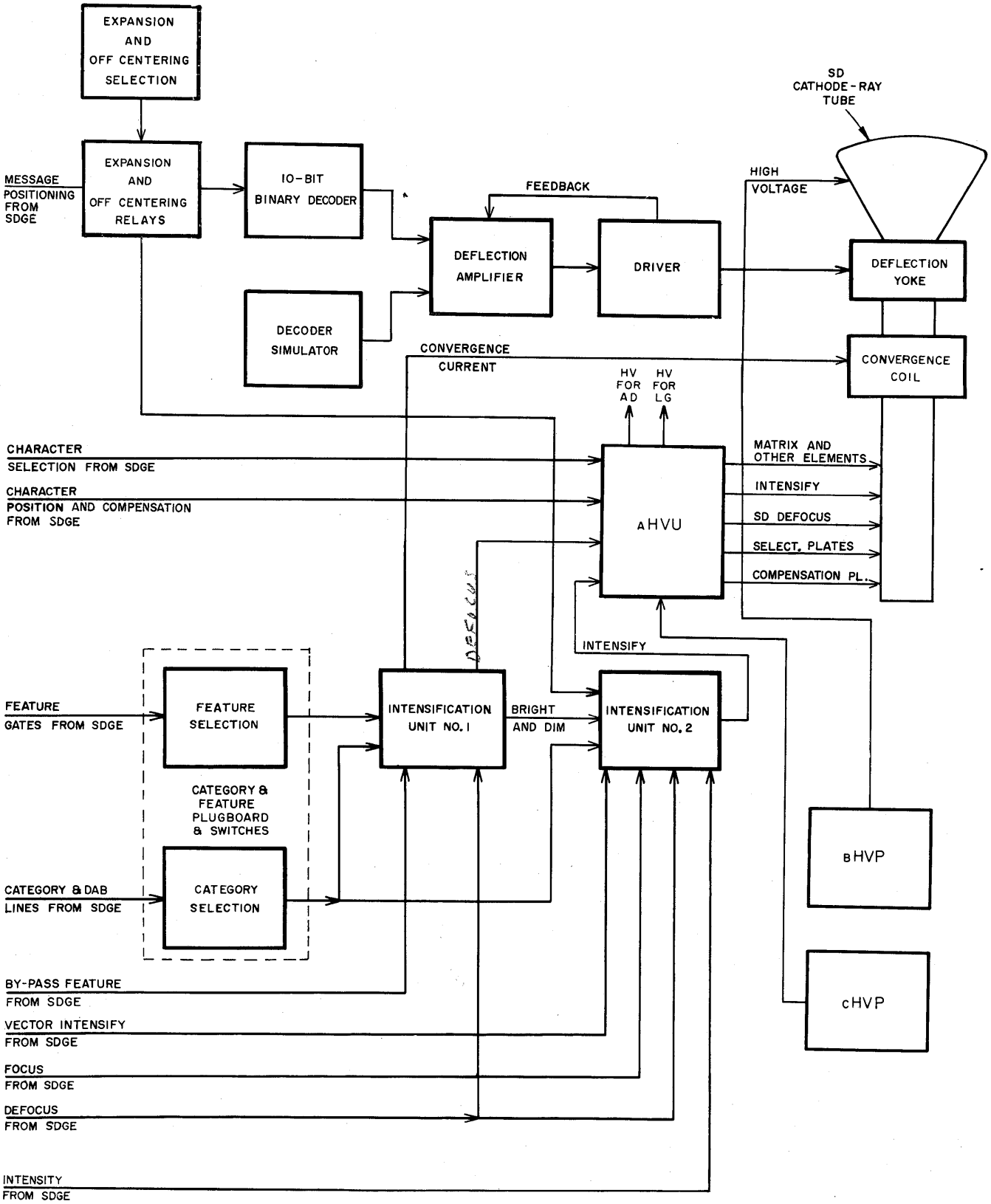


Figure 4–13. Situation Display Indicator Element, Simplified Flow Diagram

disk. The disk is located in the front end of the electron gun, as indicated in figures 2–6 and 2–7. The electron beam from the gun is directed through one of the character cut-outs selected by the message bits. The emanating beam is thus extruded into the shape of the selected character and appears as an enlarged replica of the character on the viewing screen.

The bits of a message that select a character are decoded (changed from digital to analog voltages) in the SDGE. The resulting analog voltages are applied to potentiometers within the high-voltage unit of the SD console. The voltages from potentiometers in a push-pull arrangement are applied to the selection plates of the SD CRT. The voltages on the selection plates deflect the electron beam to the proper place on the character matrix. The portion of the beam passing through the matrix is shaped in the form of the desired character. That portion of the beam which does not pass through the matrix is attracted by the potential on the matrix and passes off as a matrix current.

2.2.2 Character Positioning and Compensation

The second set of deflection plates in the SD CRT places the character-shaped electron beam in a specific position with respect to the message being displayed. If a vector is to be displayed, this second set of plates sweeps the electron beam (in this case, a focused beam) the desired length and direction. These plates also compensate for any off-centering of the character-shaped electron beam caused by the character selection described above. The character-positioning analog voltages for the second set of deflection plates come from two sets of potentiometers which are set up in a push-pull arrangement similar to that used for the character selection plates. These potentiometers are also located within the high-voltage unit. The character-positioning voltages are obtained from decoders within the SDGE.

2.2.3 Message Positioning

Because of the great variety and quantity of information which will be displayed on the SD CRT, the individual console operator requires different expansion scales so that he may observe enlarged displays of particular areas of interest. For this purpose, OFF-CENTERING pushbuttons and an EXPANSION control are provided on the front panel of the console.

2.2.3.1 Expansion Scales

The basic scale of expansion is designated as X1 (times 1). This is also called the frame of reference or unexpanded display. The X1 display can be expanded into X2, X4, and X8 displays.

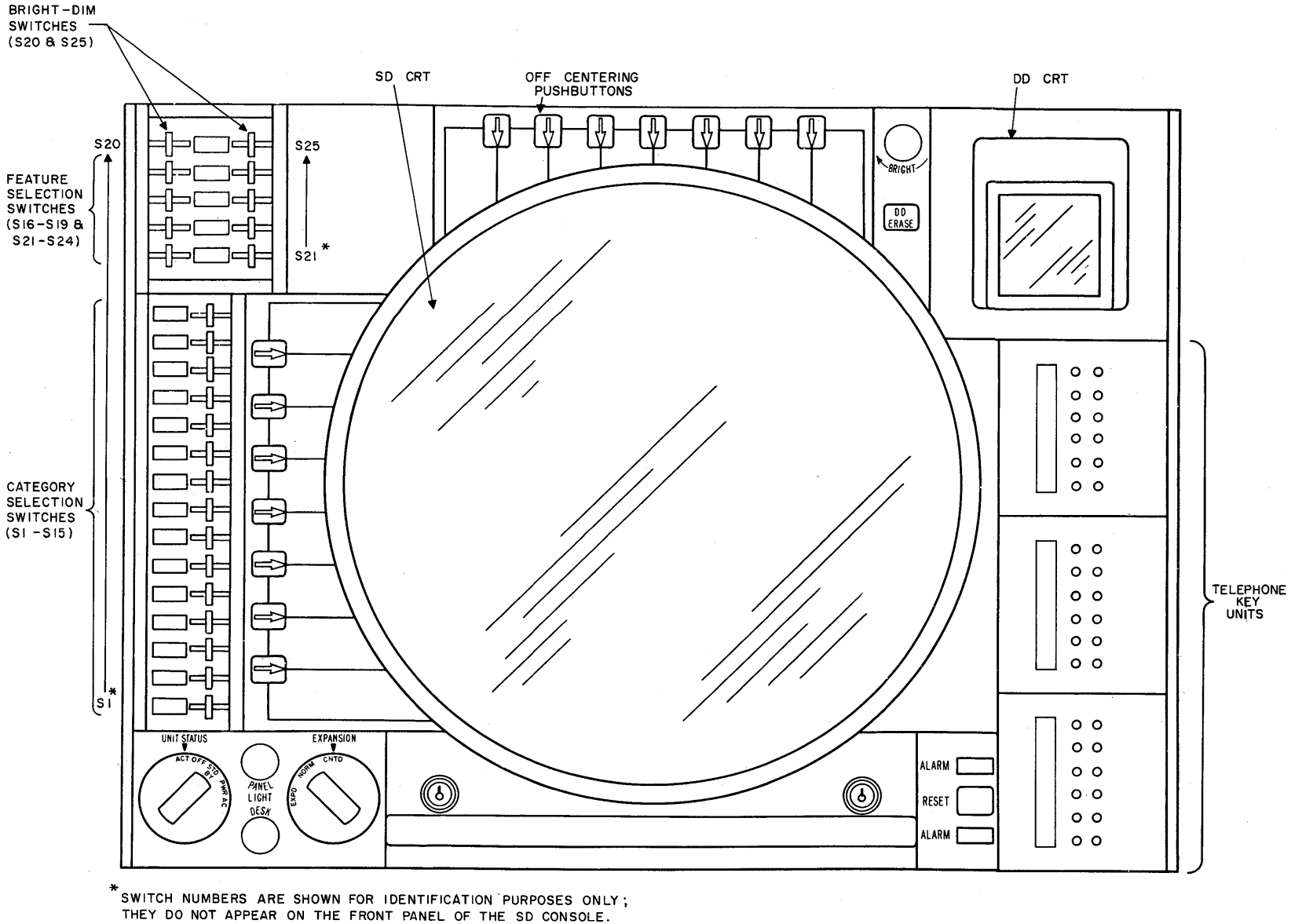
If the X1 display is visualized with X and Y axes superimposed on the face of the SD CRT, all messages will be positioned with respect to the intersection of the two axes. This positioning information is contained within each message in the form of X- and Y-positioning bits. When an X2 expansion is being observed, the same SD CRT area is used to display ½ the X-axis distance and ½ the Y-axis distance that is represented by the X1 display. Thus, only ¼ of the original geographic area can be seen, so that the messages appearing in that particular area will be further apart and can be interpreted more easily. In a similar manner, the X4 expansion presents only 1/16 of the original area for display or ¼ of the X2 display. The X8 expansion displays only 1/64th of the original X1 display.

Of the four scales described, only three can be selected at any one SD console. The three scales selected are determined by how the expansion and off-centering rotary switches (S71, S72, S73, and S74), at the rear of each console, are positioned. The 3-position EXPANSION switch (S28) is used to select contracted (CNTD), normal (NORM) or expanded (EXPD) displays. In most cases, each switch position will select a scale not used on another switch position, the CNTD display will usually be a lower expansion scale than NORM, and NORM will usually be a lower expansion scale than EXPD. CONTRACT AREA switch (S71) allows for expansion scales X1 or X2 in the CNTD position. SCALE switch (S72) makes possible X1, X2, or X4 in the NORM position and X2, X4, or X8 in the EXPD position. Provision for X1 is not made in the EXPD position since off-centering is not possible in the X1 expansion. Therefore, the CNTD scale will never be X4 or X8, the NORM scale will never be X8, and the EXPD scale will never be X1, since no off-centering would be possible under these circumstances.

Expansion and off-centering do not affect the character size or spacing between the characters of a message because the digital voltages of word 1 (which are used to position the entire message on the face of the SD CRT) are processed for expansion separately from the bits that are used for positioning each character within the message. The latter are actually decoded in the SDGE and arrive at the SD console as analog voltages. In the case of a TD vector message, however, the spaces between the vectors will vary with the expansion, although the size of the vectors will not be altered by the particular expansion level.

2.2.3.2 Off-Centering

Expansion and off-centering rotary switches (S71, S73, and S74) determine the off-centering positions for CNTD and NORM displays. If, for instance, the CNTD display is an X2 expansion, the segment of the X1 display which will be viewed when in the CNTD position will be independent of operator control. The X1 segment will have been selected by maintenance personnel by setting CONTRACT AREA switch S71.



* SWITCH NUMBERS ARE SHOWN FOR IDENTIFICATION PURPOSES ONLY; THEY DO NOT APPEAR ON THE FRONT PANEL OF THE SD CONSOLE.

Figure 4–14. Situation Display Console, Operating Controls

The operator will, however, be able to select a particular segment of the NORM display for expanded viewing on the EXPD display. A maximum of 14 OFF-CENTERING buttons is provided on the front panel of the console for this selection, seven along the top of the SD CRT, and seven along the left side of the SD CRT. These controls are shown in figure 4–14.

If the EXPD scale is four times that of the NORM scale, only three of each set of seven pushbuttons will be available to the operator. The other four will not be available. Figure 4–15,A, shows a display wired so that X2 expansion appears with the EXPANSION control switch at NORM. If we divide this area into sixteenths (four of which can be picked for display when the EXPANSION control is set to EXPD), it can be seen that there are nine areas that can be expanded to twice the NORM size: ABEF, CDGH, IJMN, KLOP, BCFG, JKNO, EFIJ, GHKL, and FGJK. Note that this allows a 50 percent overlap between sections. Observe, also, that the intersection of a vertical line drawn from the top OFF-CENTERING pushbutton on the side would intersect at the center of the selected area.

To select the shaded area of figure 4–15,A, for expansion, pushbuttons Xc and Y_1 are depressed, and the EXPANSION control is turned to EXPD. In this case, the EXPD position displays a geographical area 1/4 the size of the area of the normal display. In B, of fig. 4–15, however, the NORMAL display is an X4 scale of the frame of reference; the EXPD display is covering an area 1/16 that of the frame of reference.

A maximum of seven pushbuttons along the X-axis of the display and seven along the Y-axis provide a maximum of 49 possible areas of expansion (figs. 4–14 and 4–15), when turning from a NORMAL display to an EXPD display.

The rotary switches (or plugboard, where these are still used) are located in the rear of the console (fig. 4–16). These switches or plugboards also control the level of expansion to which a particular console has access. A further description of these controls is given in 2.6 of this chapter. The situation display console operating controls are shown in figure 4–14.

2.2.3.3 Expansion Relays

The message-positioning bits go first to the expansion relays which are controlled by the EXPANSION switch (S28), CONTRACTED AREA switch (S71), SCALE switch (S72), NORMAL AREA switches (S73 and S74), and OFF-CENTERING buttons. Of the 26 positioning bits that come in, 13 are for X-axis positioning and 13 are for Y-axis positioning. For any particular expansion, 10 of the X bits and 10 of the Y bits are selected. A different set of 20 bits is used for each individual expansion. The relays which select the 20 bits direct these bits to the 10-bit binary decoder (which accepts 10 bits for X and 10 bits for Y positioning), where the digital voltages are converted into analog voltages for use in the SD CRT. In addition, the intensification signal is gated into intensification unit 2. The gating of this signal in the intensification unit is determined by the operation of the expansion and off-centering relays in order to produce intensification on the face of the SD CRT for only those messages that fall within the expanded area. All other messages are not intensified.

2.2.3.4 Ten-Bit Binary Decoder

The function of the decoder is to convert the digital voltages (the voltages are the positioning bits) into analog voltages for positioning the messages on the viewing screen of the SD CRT. The decoder consists of two identical sections, one for X positioning and one for Y positioning. Each half accepts 10 input digital voltages and combines them to form one analog output voltage. For instance, if all the input bits to the X section are 1, the analog output will be +150V, corresponding to a message position on the extreme right side of the tube. If all the output bits are 0, the analog output will be +100V, corresponding to the extreme left side of the tube. Various combinations of input bits will produce analog outputs between these two values; +125V would then be the center of the tube in the reference plane. A net change (differential output) of 50V is therefore required to produce deflection from one end of the SD CRT to the other.

The decoder is also connected to the decoder simulator which is a circuit similar to the decoder but which has no signal input. The decoder simulator is located in a pluggable unit directly beneath the decoder. Both decoder and decoder simulator are powered from the same B+ supply; any variation in the B+ voltage will be reflected equally in the outputs of the decoder and decoder simulator. Both of these outputs are fed to the deflection amplifier (described below in 2.2.3.5). The deflection amplifier has been designed so that it will not be sensitive to signals appearing on both inputs (from decoder and decoder simulator). Thus, any variation appearing on the decoder output due to B+ variation will also appear on the decoder simulator output, and the deflection amplifier will not respond to this variation. Message-positioning will therefore be independent of supply voltage variations.

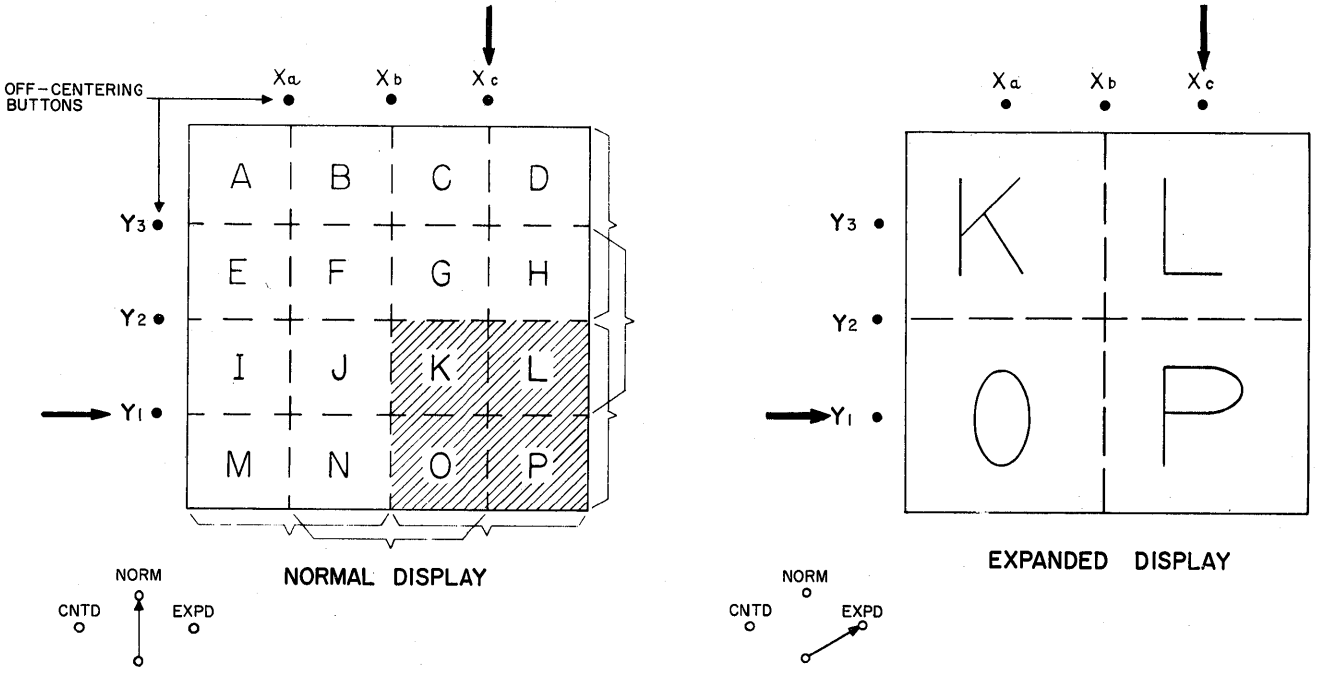
2.2.3.5 Deflection Amplifiers and Deflection Drivers

The deflection amplifiers amplify the X, Y outputs of the binary decoder. The amplified outputs are fed to a deflection driver unit which contains cathode follower power amplifiers. The resultant output, in turn, drives the deflection yoke (located around the neck of the SD CRT), and positions the SD message on the viewing

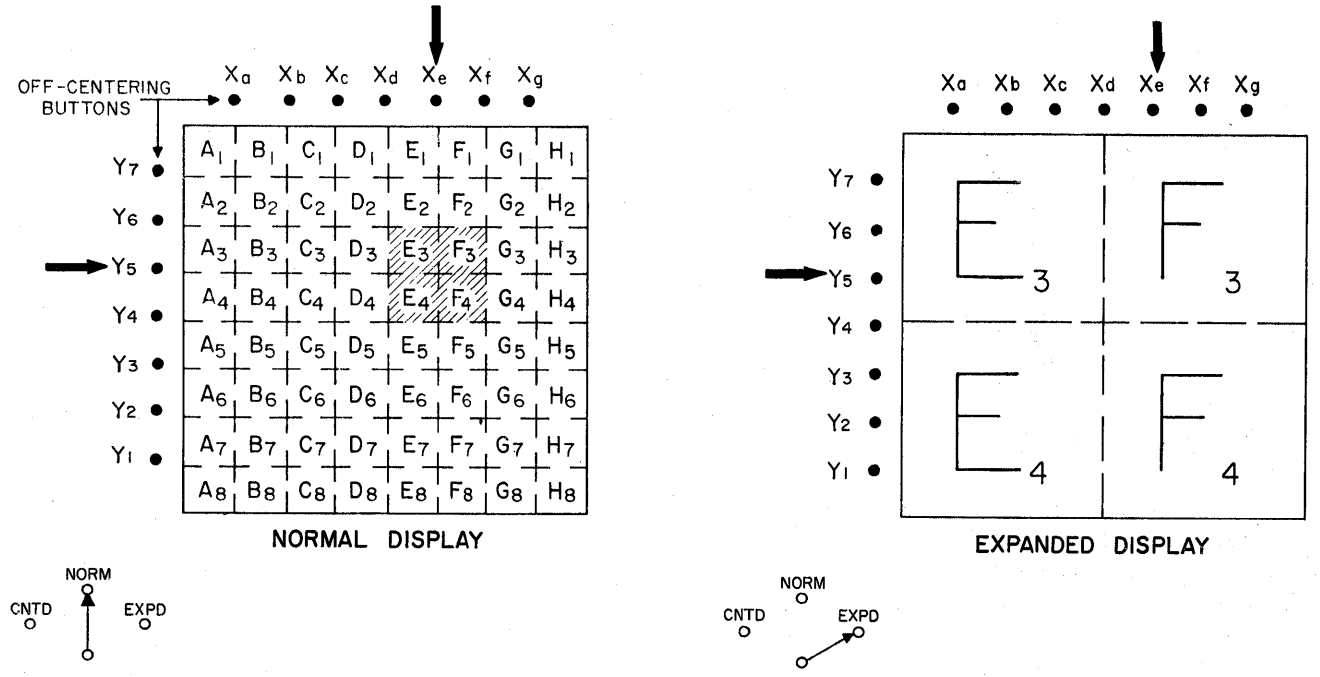
screen of the CRT. One deflection amplifier and one channel of the driver constitute a feedback system which is used to maintain accuracy and stability of amplification.

2.2.4 SDIS Selection

There are great quantities of messages on the air defense situation of the geographical area covered by the AN/FSQ-7 and -8. These messages would be too many in number to be usefully displayed on the viewing screen of any one SD CRT. For this reason, all SD messages are classified in many ways so that a given console receives only those messages for which it has a tactical use.



a. X2 EXPANSION



b. X4 EXPANSION

Figure 4–15. Off-Centering and Expansion Areas (X2 and X4)

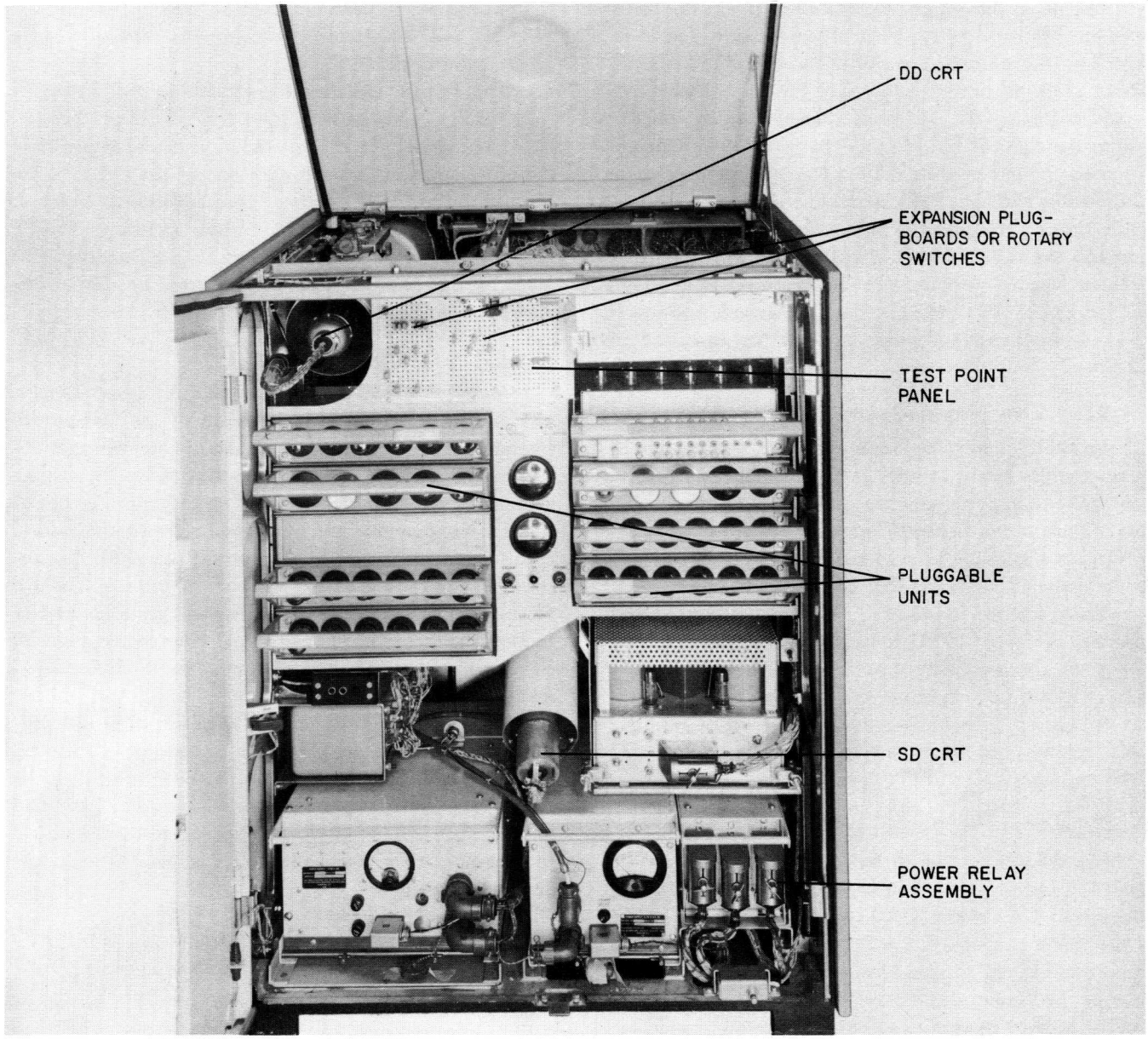


Figure 4–16. SD Console, Access Doors Open

2.2.4.1 Categories

One method used by the Central Computer in differentiating between messages involves placing each SD message in one of a possible 40 (32 TD and 8 RD) basic categories. Each console is assigned a certain number of categories, receiving only those categories which are required by the operator for performing his tactical duties.

Those categories that are assigned are routed through CAT switches on the front panel of the SD console so that the operator has control over whether the messages in a particular category will be displayed or not displayed. Only category 1 (test category) cannot be selected at the front panel of the SD consoles.

Bits LS through L4 of word 2 of a tabular or vector message are used to identify the category of the message. These five bits can be used to count 32 since there are 32 combinations of 1's and 0's possible with the five bits. Category 0, containing 0's in all five bit positions, is referred to as a null category. This category is used only when a display assignment bit (DAB) is assigned to a message.

There are also eight radar categories, identified by bits L14 and L15 of an RD message and an RD-dim-RD-bright signal.

Although all the information signals (character selection, character position, etc.) of a particular TD or RD message arrive at every SD console, the message

will not be displayed on the SD CRT unless the category bits of that message form a combination that is assigned to the particular console. In addition, the CAT switch must be turned to its ON position. Each CAT switch has two ON positions, immediately to the left and to the right of center (OFF position). The ON position on the left permits the CAT switch to function in conjunction with one bank of feature selection switches, while turning the category switch to its other ON position (on the right) allows it to function with the other bank of feature switches. (In the case of RD messages and geography TD messages, the CAT switch position is of no consequence.) Feature switches are discussed in 2.2.4.5.

2.2.4.2 Display Assignment Bits

In addition to selection by category, a message can be selected by means of a DAB. Each DAB has a permanent relationship or assignment to one or more consoles. Thus, if the Central Computer System is impelled to display a message at a specific console, it places a 1 in the assigned DAB for that console in the message.

There are two types of DAB messages: forced and selected. A forced DAB message is automatically displayed at the assigned console; a selected DAB message is routed to a specific console where the operator has the option of switching the message on or off. The CAT selection switches are used to control selected DAB messages.

2.2.4.3 Mixed DAB's and CAT's

In addition to the 40 basic categories and the 90 DAB's, up to 45 supplementary drivers (CAT's, DAB's, and mixed CAT's and DAB's) may be created in the SDGE. The mixing of CAT's and DAB's can be accomplished either at the SDGE or at the consoles, although the 45 supplementary drivers, referred to here, are obtained by mixing in the SDGE.

2.2.4.4 DAB and CAT Inputs to Consoles

There are 27 input lines to each console which may be used to bring DAB's and CAT's to the console. The assignment of these lines differs from console to console and is a function of the tactical requirements of each individual console.

2.2.4.5 Feature Selection

Feature selection (applicable only to TD tabular track messages) enables the operator to select portions of the messages selected at the CAT switches. Five input lines to the consoles carry features A through E to the feature switches. These switches govern which of the features (in the messages selected by the CAT switches) will be intensified on the SD CRT. When a feature is selected by a feature switch, the feature gate is transmitted to the intensification circuits so that the SD CRT will be intensified during the time of display of the feature.

The feature switches are located in two banks of four switches each at the upper left corner of the console front panel. Each bank functions independently of the other and is associated with one of the two ON positions of the CAT switches. One additional switch is located above each bank of feature switches. This is the BRIGHT-DIM switch; it controls the intensification level of the features that are selected by the associated bank of feature switches.

2.2.5 Intensification

Message selection by means of CAT's and DAB's, and feature selection and expansion of the display are implemented by the intensify circuits. Those messages (or features of messages) which are not intended for display at a particular console are sent to the console, nevertheless; but they are not intensified. Should the tactical requirements of a particular console change so that the console requires a different category of message (or different feature assignments), it becomes a simple matter to alter the incoming control signal lines to the intensify circuits so as to produce illumination of the desired messages.

In the case of expanded displays, the messages which fall in the geographical areas outside the expanded area being viewed are still brought to the console. However, the geographical information produced in the expansion circuits is sent to intensification unit 2 so that only those messages in the expanded area will be intensified.

2.2.5.1 Intensification Unit 1

The functions of this unit are as follows:

a. Intensification of selected features (with intensification unit 2).

b. Application of regulated current to the SD CRT convergence coil for optical focusing of the electron beam so that the characters will not appear blurred.

c. Intensification of bypass feature (with intensification unit 2).

d. Application of a defocus gate to the first anode of the SD CRT to defocus the electron beam before it reaches the character-forming matrix, for all characters except point and vector.

2.2.5.2 Intensification Unit 2

This unit functions with intensification unit 1 and four input gates to the SD console to produce intensification of all points and characters scheduled for display on the particular console.

2.2.6 High-Voltage Power Supplies

There are two high-voltage power supplies in the SD console: HV power supply B and HV power supply C. The model B supply produces high voltage for the second anode of the SD CRT. The model C supply produces the supply voltages for the cathode and control grid of the CRT. The filament voltage for the CRT is obtained from the high-voltage unit. The operation of these units is explained in the Special Circuits Manual, 3-3-0.

2.2.7 High-Voltage Units

High-voltage unit, model A, supplies the SD CRT circuits with most power requirements. Both major signal and power needs are routed through this unit. A complete circuit analysis is given in the Special Circuits Manual, 3-3-0.

The functions of the model A high-voltage unit are as follows:

a. Provides taps on the high-voltage supply bleeder for the light-gun and area-discriminator high-voltage requirements.

b. Provides the input network for a convergence current regulator that generates a voltage proportional to SD CRT accelerating voltage, by means of which the convergence coil current is regulated.

c. Contains the amplitude adjustment for horizontal and vertical centering controls for character compensation and selection.

The unit is mounted so that the controls are located on the subpanel of the console.

2.3 DETAILED OPERATION

This chapter discusses the SDIE from a detailed functional operation. The block diagram in figure 4–13 shows the logic functions in the overall operation of the SDIE.

2.3.1 Character Selection

Characters are selected at the matrix by feeding appropriate x and y voltages to the character selection plates. These are obtained in the SDGE where digital voltages from the Drum System are changed into analog voltages. The analog voltages are fed to the character selection plates through potentiometers in the high-voltage unit. The potentiometers, labeled CHARACTER SELECTION CENTERING and CHARACTER AMPLITUDE, are used to adjust the voltages to the individual SD CRT characteristics.

In a quiescent condition (no signal input from the SDGE), the input voltage and the voltage at each of the selection plates is nominally +45V. The CHARACTER CENTERING potentiometers are adjusted, in practice, until the electron beam is centered on the matrix. The center position is indicated when a corner of each of the four centrally located characters appears on the viewing screen.

Character selection is a function of two pairs of voltages, one for horizontal and one for vertical selection. The pairs are fed push-pull to the horizontal and vertical character selection plates where they deflect the electron beam to the desired point on the matrix.

A potential of approximately 50V between plates (+25V fed to one plate and −25V fed to the other) is required for full horizontal selection. The actual voltages on the plates in this instance are +70V and +20V (+45V plus 25V on one plate; 45V minus 25V on the other). Intermediate deflections are linear with a nominal 14.5V difference in potential being required to deflect the electron beam horizontally for one character space.

Similarly, an approximate 90V potential between plates is required for full vertical selection. The actual voltages on these plates are, for full deflection, +90V (+45V and +45V) and 0V (+45V and −45V). Intermediate vertical deflections are also linear and require nominal 25V differences in potential to deflect the electron beam vertically for one character space.

2.3.2 Character Compensation

The electron beam must be recentered in order to compensate for the off-centering caused by character selection. This is done by feeding in character-spacing analog voltages and character compensation analog voltages from the SDGE. (The compensating voltages are opposite in phase to the character selection voltages.) The compensation voltages are fed to the compensation plates through potentiometers in the high voltage unit which are similar to the CHARACTER SELECTION potentiometers. These are labeled CHARACTER COMPENSATION AMPLITUDE and CHARACTER COMPENSATION CENTERING and are used to adjust the compensation voltages so that, with no character-positioning signals, the character appears on the center of the SD CRT.

2.3.3 SDIS Selection

The SDIS selection is the method used to channel the assigned messages to a specific console. A greater quantity of messages is processed and transmitted to the Display System than can readily be shown on every console CRT. Therefore, a selection method is necessary. The various consoles are assigned definite tactical duties so that a need exists only for certain messages for each console. These messages are placed in separate categories and assigned one or more DAB's that establish the category to be displayed on a particular console.

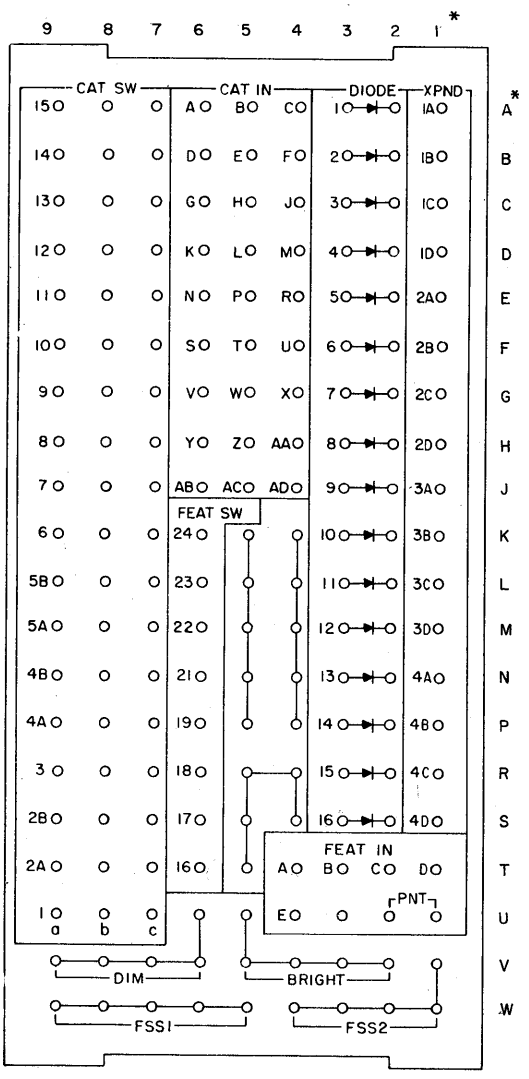
2.3.4 CAT and DAB Switches

Each SD console has 15 lever switches that are used for CAT and DAB control. They are referred to

as the CAT switches and are located in a single column to the left of the SD CRT (fig. 4–14). All the CAT switches have three positions: left, center, and right. The center position is OFF. For TD categories, the left position is generally connected to FEATURE SELECTION group I and the right to group II. Provision has been made on the console for inserting a label with the name of the assignment along the side of each CAT switch. The inputs assigned to these switches are TD categories and supplementary drivers. Some of the latter signals may be DAB's that are used for display selection rather than forced display.

2.3.5 RD CAT Switches

The switches used for radar data also have three positions: ON, OFF, and ON. Recent radar data is displayed by both of the ON positions as a bright symbol. Past or history radar data is displayed dimly. Double-pole, double-throw switches are provided for three of the CAT switches. If no RD categories are assigned to a particular console, these switches can be used for the TD categories and supplementary drivers.



* THE LOCATION NUMBERS AND LETTERS ARE SHOWN FOR IDENTIFICATION PURPOSES ONLY; THEY DO NOT APPEAR ON THE PLUGBOARD

Figure 4–17. Category Control Panel (Plugboard)

2.3.6 Feature Selection Switches

There are eight feature selection switches of the lever type located above the 15 category switches (fig. 4–14). The feature selection switches are located in two groups of four each. Each switch has two positions, labeled ON and OFF. The feature switches can control combinations of the five features: A, B, C, D, and E. There is an associated BRIGHT-DIM switch located above both feature selection switch groups, causing all categories in each group to be displayed at the bright or dim level of CRT intensification. There is no off position for the BRIGHT-DIM switches.

2.3.7 Interaction of Feature and CAT Switches

The CAT switches are the primary message-selecting device available to the operator. Each message has been placed in a category by the Central Computer System so that the operator may select the messages in all categories available to him. In addition, TD tabular track messages consist of features that can be selected. The operator need observe only those features of TD tabular track messages which are necessary for his tactical duties. His feature requirements, however, will not be the same for all messages. He will wish, for example, to see the A, C, and D features of some categories of messages while desiring to see the A, C, D, and E features of other categories. This is made possible by providing two independent sets of feature selection switches, groups I and II. All CAT switches, for example, that control categories for which the A, C, and D features are desired can be set to one of the feature selection groups, while the remainder are set to the other feature selection group. For further differentiation in display, one of the groups can be displayed with dim illumination and the other with bright intensification.

2.3.8 Category Control Panel

It has been established in the preceding paragraphs that each SD console is located at a different tactical station and that each has its own specific category and feature assignments. In order to provide a flexible means for connecting the switches to the necessary signal lines, a control panel (plugboard) has been provided at the top of each console underneath the access door. When this control panel has been properly patched in, the console acquires the unique signal-handling properties that distinguish it from the other consoles in the Display System. This method also makes it

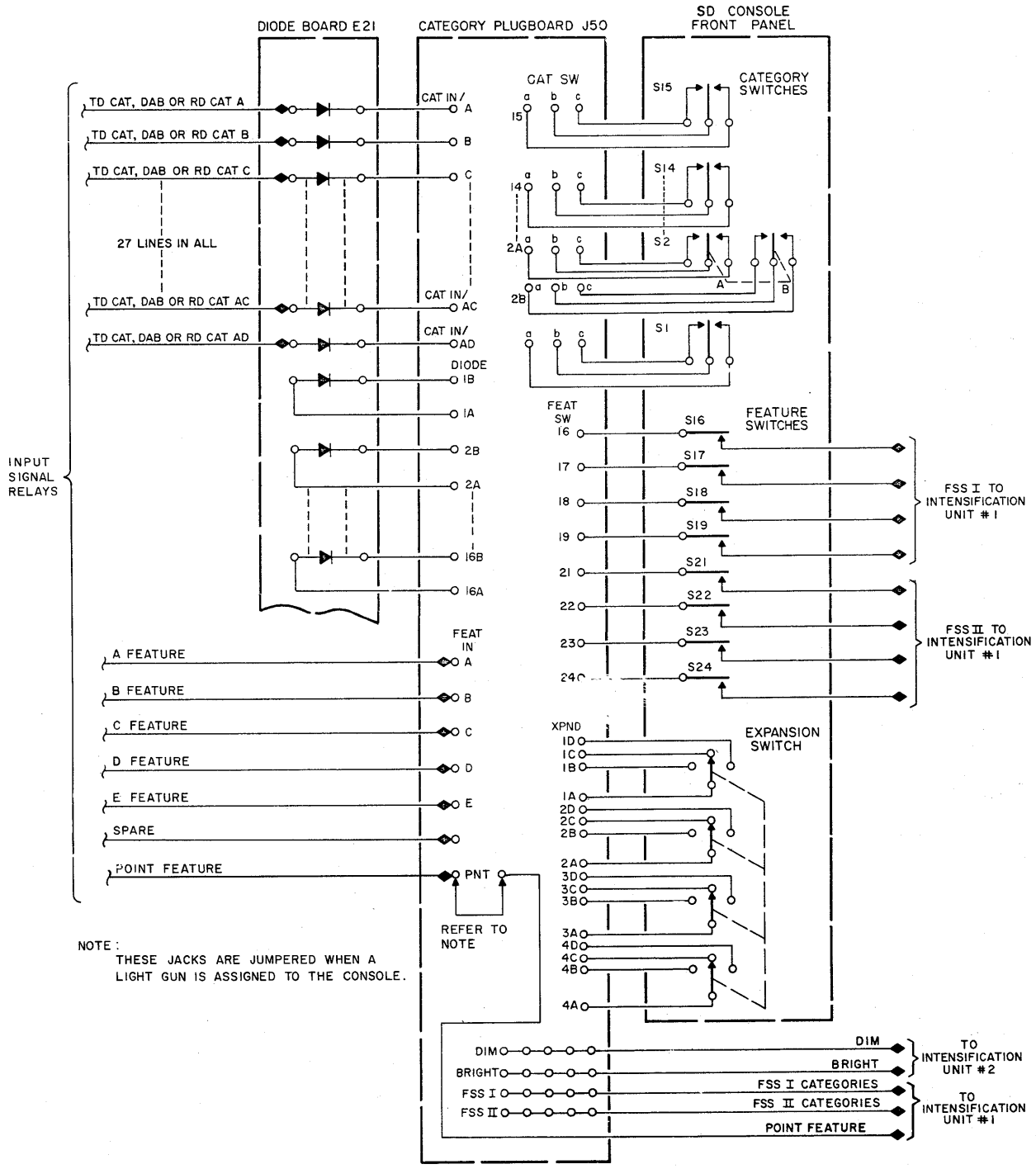


Figure 4–18. Category Control Panel (Plugboard), Schematic Diagram

relatively easy to change the switch assignments of a particular console, should the need arise.

The category control panel is shown in figure 4–17. The schematic of the control panel is shown in figure 4–18 and the logic is discussed in 4.2.1. All the jacks shown on figure 4–17 are grouped into eight separate areas. With the exception of the group of spares, all areas are labeled. Each individual jack is identified by a number and a letter which do not appear on the actual control panel. In figure 4–17 there are nine columns, starting with column 1 on the right side. The rows of jacks are identified by letters, starting with A for the first row at the top.

2.3.8.1 CAT IN

There are 27 jacks under the CAT IN label, corresponding to the 27 CAT and DAB lines available at

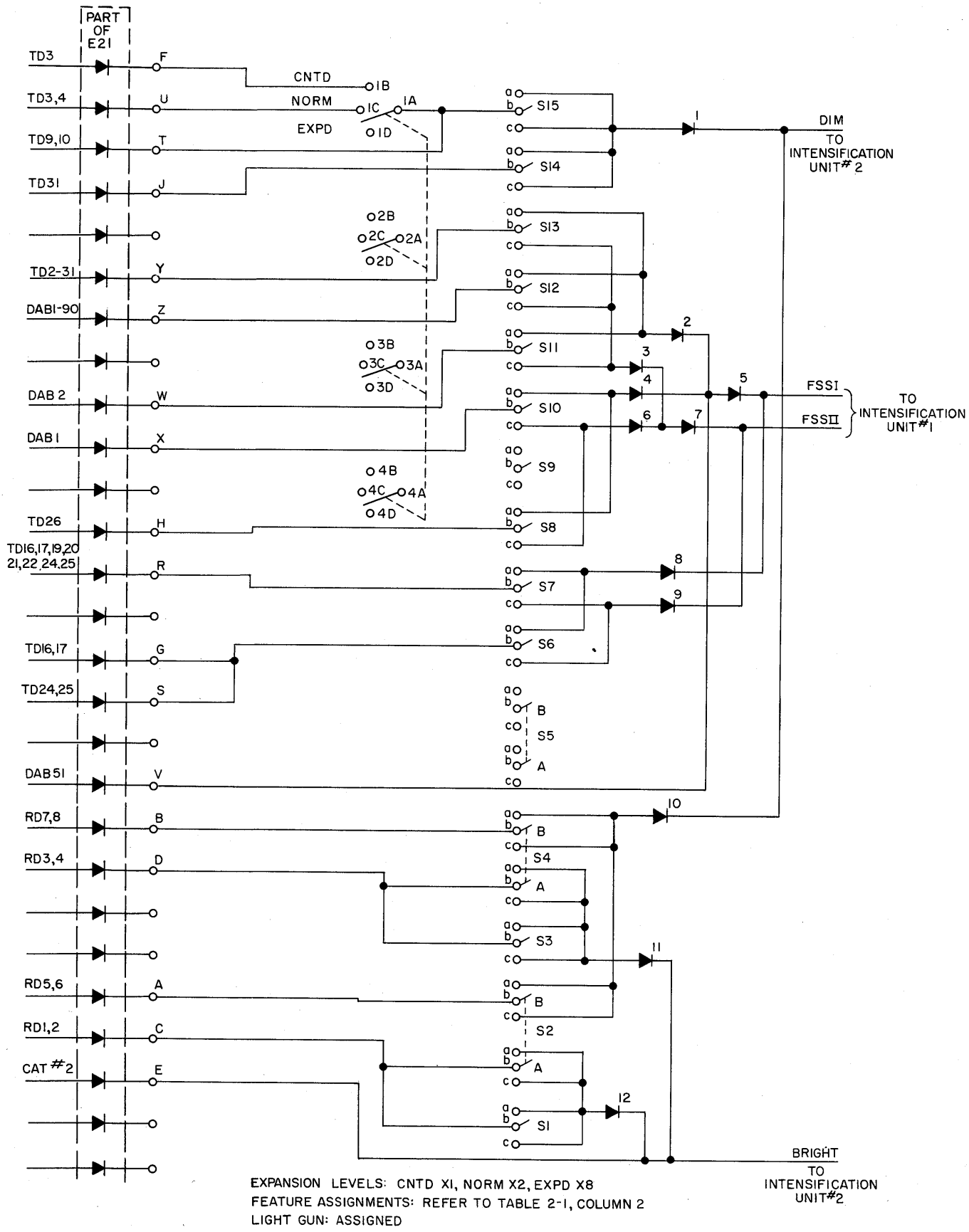


Figure 4–19. Typical CAT/DAB Plugboard, Wiring Diagram

each console. They are located in columns 4, 5, and 6. Some consoles will not have all 27 lines assigned to them; the maximum number (27) will appear only on those consoles with a full complement of lines.

The category gates that appear at each of these jacks have already passed the diode board (E21). A list of CAT and DAB assignments will accompany each console so that the categories can be wired to the jacks under the CAT SW label.

2.3.8.2 CAT SW

The two fixed contacts of each CAT switch are connected to jacks marked a and c in columns 9 and 7, respectively. The movable contact is connected to jack b in column 8. Six jacks, arranged in two rows of three jacks each, are provided for each of the double-pole CAT switches (S2, S4, and S5). These rows are labeled 2A, 2B, 4A, 4B, 5A, and 5B; the A's and B's designate the two poles of the associated CAT switches.

2.3.8.3 DIODE

Columns 2 and 3 contain jacks for 16 diodes that are located on diode board E21. These diodes are not employed as input diodes but are utilized as isolation diodes when patching the plugboard for the particular CAT and DAB assignments of the associated SD console.

2.3.8.4 EXPD

These jacks (column 1) are connected to contacts on four of the sections of the EXPANSION switch. In each group of four jacks, the A jack is connected to an arm of the EXPANSION switch, while the B, C, and D jacks go to the three fixed contacts (CNTD, NORM, and EXPD, respectively) of that section.

The expansion levels of the three positions of the EXPANSION switch are determined by the wiring of the expansion switches located in the rear of the console.

2.3.8.5 FEAT IN

Five of the FEAT IN jacks receive the feature gates from the signal relay contacts. The sixth jack is connected to the point feature gate (jack U2); if the particular console has a light gun assigned to it, U2 is jumped to U1, thereby connecting the point feature to the intensification circuits. Jack U3 is connected to the spare feature line.

2.3.8.6 FEAT SW

The eight jacks in this group are used for connecting the features at the input to the plugboard to the feature switches located on the front panel of the console.

2.3.8.7 Output Jacks

The jacks at the bottom of the control panel are the four main outputs of the plugboards. These are the intensity lines: bright, dim, FSS I, and FSS II. The remaining (unlabeled) jacks are for convenience in patching.

2.3.9 Intensity Levels

There are two different levels of illumination for messages appearing on the viewing screen of the SD CRT: dim and bright. Some messages will always appear dimly illuminated and some will be relatively bright. The remainder can be made dim or bright, according to the needs of the operator. In general, two types of messages will always appear at the bright level of intensification: present radar and TD CAT 2 messages.

All other messages will be placed in one of two groups: FSS I or FSS II. The intensity level of these two groups will be determined by the setting of the corresponding BRIGHT-DIM switches on the front panel.

The forced CAT and DAB signals will always be connected to the FSS I group and, therefore will always have the same level of intensification as messages placed in the group.

2.3.10 Patching Procedure

Figure 4–19 is a typical CAT/DAB plugboard wiring diagram for an SD console and illustrates the patching procedure. The CAT and DAB assignments appear on the lines feeding diode board E21. Only 18 of the 27 available input lines to the plugboard are utilized. The outputs of the diode board are wired to the CAT IN jacks of the plugboard. The purpose of the patching procedure is to channel these inputs through the EXPANSION and CATEGORY switches onto one of the four intensification lines (bright, dim, FSS 1, and FSS II). Jumpers with 2, 3, 4, and 5 heads are available for patching the plugboard as directed in the wiring diagram.

The inputs to CAT IN jacks, F, U, and T (T, D geography categories), are assigned to CAT switch S15. However, inputs F and U are functions of expansion and are therefore patched to contacts 1b and 1c of section 1 of the EXPANSION switch, before feeding S15. The expansion levels for the three positions of the expansion switch are noted at the bottom of the wiring diagram. Input T is independent of the expansion levels and is patched directly to S15. Similarly, input J is patched directly to S14. The outputs of CAT switches S14 and S15 are connected to the dim output line through isolation diode 1.

The inputs at CAT IN jacks, Y, Z, W, X, H, R, G, and S are individually patched directly to CAT switches S13 through S6, respectively. (S9 is not utilized.) The outputs of these switches in the FSS I position (contact a) are fed to the FSS I output line by means of isolation diodes 2, 4, 5, and 8. In a similar manner, the outputs of

each of the FSS II positions (contact c) are applied to the FSS II output line through isolation diodes 3, 6, 7, and 9.

The inputs at jacks B, C, A, and C (radar categories) are patched to CAT switches S4 through S1, respectively. The CAT switches S4 and S2 are double-pole switches; the outputs of one pole (section B of these switches) are connected to the dim output line by means of diode 10. The outputs of CAT switch S3 and section A of S4 are fed to diode 11; S1 and section A of S2 are connected to diode 12. The outputs of diodes 11 and 12 are applied to the bright output line.

DAB 51 (CAT IN jack V) is a forced display and is patched to the FSS I output line through diode 5. The CAT 2 (all categories) is also a forced display and is connected to the bright line.

The patching information for the feature assignments is not included in the CAT/DAB plugboard wiring diagram. The necessary information is provided with each console; i.e., FEAT IN A is patched to FEAT SW 21; B, to 15; C, to 17 and 22; D, to 18 and 23; and E, to 19 and 24, for the typical plugboard used in this discussion.

In this manner, all SD selection signals have been placed on one of the four lines which go to the intensification circuits. All CAT and DAB signals which have been routed to the dim line will produce dim intensification for the messages they control; this also holds true for the signals on the bright line. In addition, category switches that are turned to FSS I will receive the intensification determined by the setting of the FSS I BRIGHT-DIM switch. The same is true for FSS II. However, an exception occurs in the case of RD and geography TD categories whose brightness is independent of the feature switches.

2.4 INTENSIFICATION

The position and character information for all SD messages in the Display System are sent to all SD consoles. The messages which will appear on the SD CRT are those for which an intensity gate has been applied to the grid of the CRT. The application of the intensity gate to the CRT is dependent upon a number of factors, all of which enter into the operational variations of the intensification circuits. Paragraph 2.2.4 of this chapter covers certain of these requirements. For example, a message must be in an assigned and selected category if it is to be displayed. Or, the message can be in one of the assigned and forced categories. It may also contain an assigned and selected or forced DAB. Any one of these cases could satisfy one of the requirements for message intensification; that is, message selection. Another factor is the geographical location or object represented by the message. Different consoles are assigned different segments of the overall area covered by the Direction Central. Consoles assigned the X1 expansion, however, can view the entire area covered by the Direction Central.

The settings of the EXPANSION switch and OFF-CENTERING buttons also determine the particular geographical area being observed. Thus, for a message to be intensified, it must correspond geographically with the area being observed on the SD CRT at the time the message arrives at the console. In addition, there must also be a coincidence of feature and category gates for the message to be seen. In the case of a TD tabular track message, at least one of the feature switches must pass a feature gate; otherwise, the point and/or vector will have no associated characters. For TD tabular information messages and TD vector messages, a bypass feature gate is always present.

The intensify circuits perform several other important functions which will be described in the subsequent paragraphs.

2.4.1 Intensification Unit 1

This unit is illustrated in figure 4–20 and discussed in logic 4.2.3. Reference to this figure will show that the feature gates are applied to OR 1 and OR 2, the lines from FS II switches going to OR 2. The bypass feature gate goes to both OR circuits along with a gate that is present when the point feature is to be displayed. Either OR circuit will produce an output gate when a feature gate occurs at its input. In this way, AND circuits 1 and 2 are conditioned. The other signals entering the AND circuits are the FSS 1 and FSS 2 category lines from the category control panel (via the test switch).

If there are any gates on either of the category lines, the corresponding AND circuit (if it has been conditioned by a feature gate) will permit the gate to pass, signifying that the message is in one of the assigned and selected CAT's (or DAB's) and that it contains one or more features that require display. Note that the feature gate occurs only during the time of display of the particular feature concerned, so that the output of AND 1 or AND 2 is not always a continuous gate but can be a series of gates that occur during the display times of the individual features. In the case of a vector message, the bypass feature gate will last for the display of the entire message.

The output of the two AND circuits goes to S20 and S25, the BRIGHT-DIM switches. These two switches feed into the remaining four diodes of the E21 diode board. The latter are connected to the bright and dim lines, as shown. Thus, the four intensify lines are now reduced to two, a bright line and a dim line, on which appear all assigned category gates. These two lines are inputs for intensification unit 2 where the intensity gate for the SD CRT grid is produced.

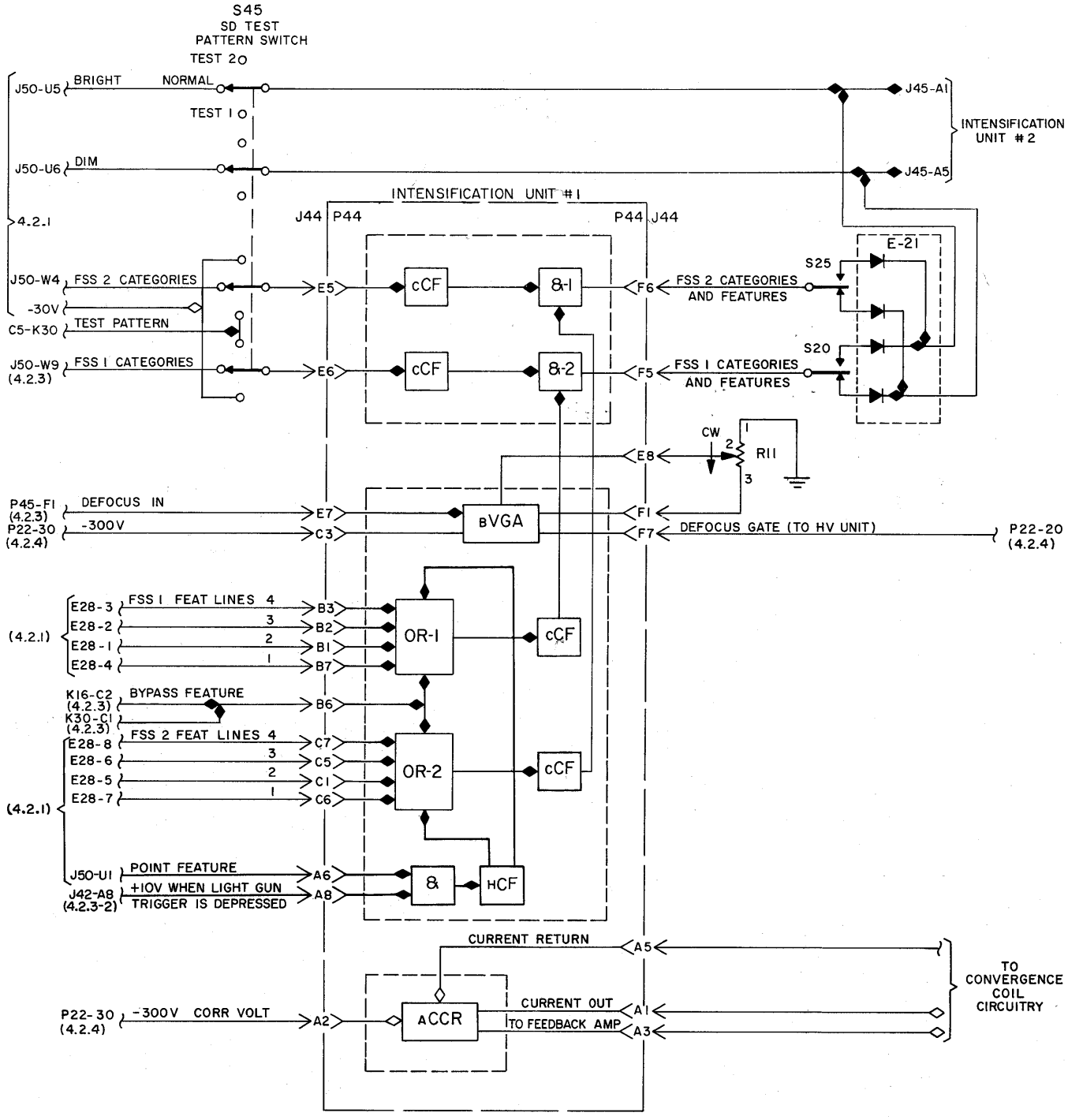


Figure 4–20. Intensification Unit 1

Contained in intensification unit 1 is a variable gate amplifier (VGA) model B to which is applied the defocus gate. The VGA provides a positive gate, at its output, which is fed to anode 1 of the SD CRT via the high-voltage unit. This gate occurs at the time a character or symbol is selected from the SD CRT matrix by the character selection voltages. As a result, the electron beam is defocused so that it spreads out and completely covers the entire area occupied by the character, thus providing a beam wide enough for extrusion through the character cutout.

In addition, intensification unit 1 contains a model A convergence current regulator which supplies the convergence coil of the SD CRT with a regulated current. The regulator enables the selected character to be in sharp focus, compensating for variations in the accelerating high-voltage.

2.4.2 Intensification Unit 2

Intensification unit 2 (fig. 4–21) receives all the information governing the actual intensification of the SD CRT. The sequence of AND circuits, consisting of AND's 6 through 9, determines when the intensity gate from the SDGE (which accompanies every character, symbol, vector, and point) will be passed through the AND circuits to the grid of the SD CRT via the variable gate amplifier.

The functioning of AND 5 is dependent on message position, which is discussed in the next paragraph. For the present, it is sufficient to know that if a particular message falls within the geographical area being observed on the SD CRT, AND 5 will be conditioned by one of the two OR circuits so that the intensity gate will be passed through to AND's 6 through 9. The other input to these AND circuits comprises the dim and bright signals. The dim signal is applied to AND's 8

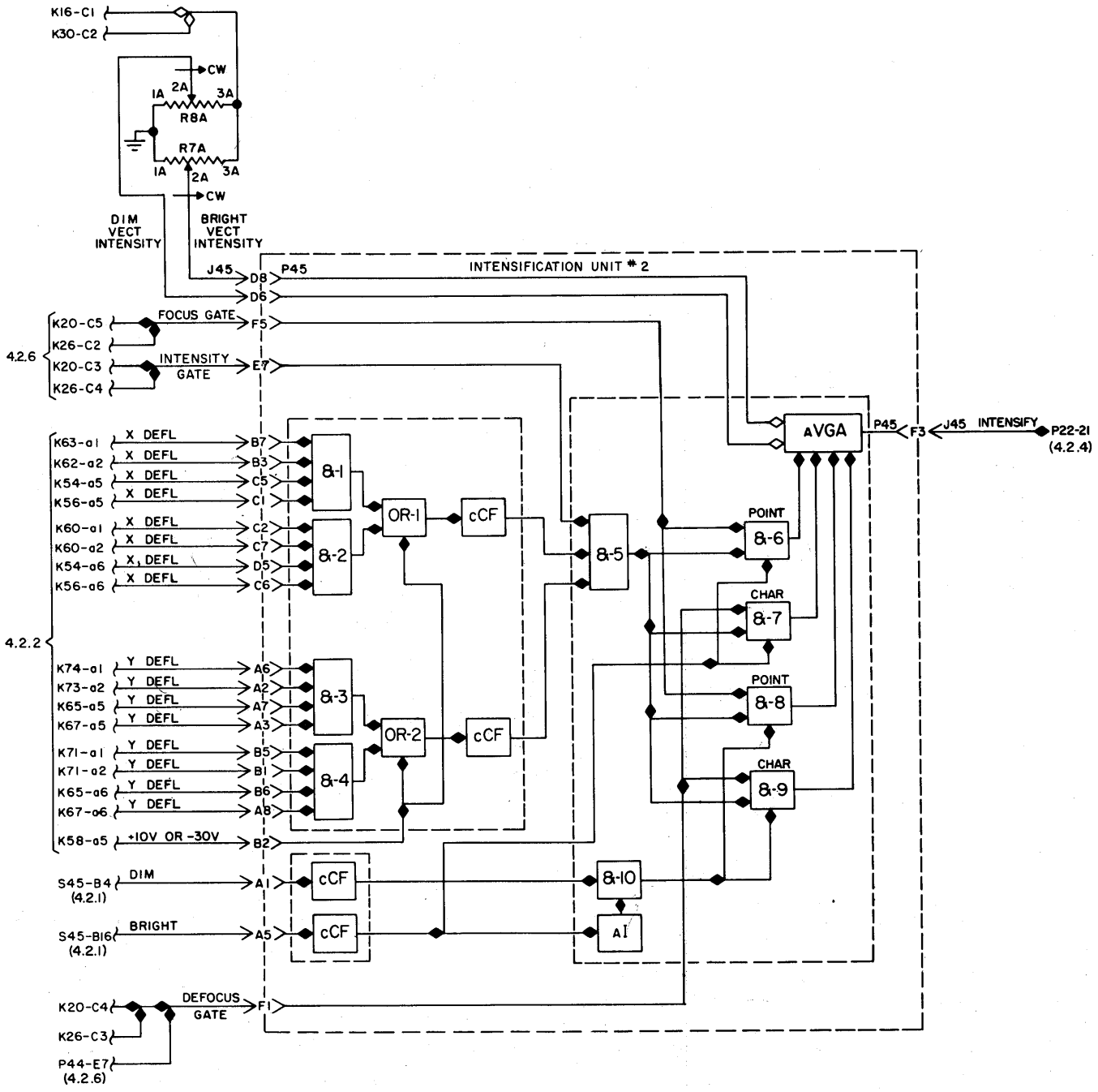


Figure 4–21. Intensification Unit 2

and 9, and the bright signal to AND's 6 and 7. Thus, the combination of signals necessary to completely condition any of these AND circuits then is as follows:

AND 6 – Focus, bright, intensity

AND 7 – Defocus, bright, intensity

AND 8 – Focus, dim, intensity

AND 9 – Defocus, dim, intensity

Notice that the intensity gate is required for the conditioning of all AND circuits.

AND's 6 and 8 require a focus signal, which means that they will be conditioned only during the display of a point or vector (a swept point), because all characters and symbols require a defocused electron beam and are accompanied by a defocus gate. AND 6 will be conditioned when the category signal of the particular message occurs on the bright intensification line, and thus controls the intensification of dim points and vectors.

AND's 7 and 9 require a defocus signal for conditioning, which means they will be conditioned only for characters and symbols. AND 7 governs bright character display. AND 9 controls dim character display. The outputs of the four AND circuits are fed to the model AVGA which produces the positive intensity gate that is fed to the SD CRT grid.

The bright intensity line, in addition to conditioning gates 6 and 7, goes to an inverter, model A, the output of which conditions an AND circuit in the dim intensity line. The purpose of this arrangement is to avoid the simultaneous dim and bright intensification of the same point, symbol or character, which would result in an extremely bright display. This can occur when a message arriving at the console is both force-displayed (FSS I intensify line) and is selected for display on the FSS II line. When there is no bright signal present at its input, the inverter produces a conditioning voltage at its output so that the dim signal will pass into the AND circuits. When a bright signal is present, the inverter produces a negative voltage, at its output, which prevents the passage of any signals that may be present on the dim intensify line.

The VGA is a multichannel amplifier that produces a positive gate at its output when it receives a signal at any one of its four inputs. Each channel has a separate gain control so that the output gate can be set up for bright or dim intensification of the SD CRT, according to the function of the particular channel.

The reason that the bright and dim point channels are kept separate from the bright and dim character and symbol channels is that the point is generated by a focused beam, whereas the symbol or character is generated by a defocused beam. If both received the same intensification gate level, the point would seem brighter. Therefore, the point is assigned to two of the four input channels of the VGA. The gain of these channels is adjusted to a somewhat lower point than the gain for the character channels, and an even intensification of all points and characters (dim or bright) is secured.

The remaining two inputs to the VGA are the dim-vector-intensity and bright-vector-intensity lines which originate from a common vector-intensity-control signal that is applied to potentiometers R7 and R8. This is a compensation signal applied to the intensity circuits in order to maintain an even intensification level for all vectors of all lengths.

The duration of the waveform which sweeps the point to produce the vector is 50 μsec long. Therefore, each vector is intensified for a period of 50 μsec, regardless of the physical length of the vector. Thus, short vectors would appear brighter than long vectors. To compensate for this effect, an analog signal is sent to the VGA at the time of the display of all vectors so that the gain of the particular channel through which the intensity gate for the vector passes is altered to ensure even intensification of all vectors. For long vectors, the gain is increased; for short vectors, it is decreased.

2.5 MESSAGE-POSITIONING

A total of 26 bits is brought to the console for message-positioning, 13 for X and 13 for Y. These bits come from storage flip-flops in the registers of the SDGE. In the case of the first four bits in each group of 13 (LS-L3 and RS-R3), both outputs of the flip-flops are brought into the console. That is, both the 0 and 1 sides of eight of the register flip-flops are connected to the console circuits. Of the remaining message-positioning flip-flops, only the 1 side output is brought to the console.

All the positioning bits are sent to the expansion and off-centering relays, where they are channeled to the 10-bit binary decoder, and to the intensification circuits as required for the particular expansion, and/or off-centering. The 10 bits which are sent to each half (X and Y) of the decoder, in each case, determine the message position on the face of the SD CRT.

The binary address scheme used in the AN/FSQ-7 & -8 is shown in figure 4–22. This diagram represents the complete area assigned to a Direction Central and a Control Central. The representation can be thought of as an X1 display with a set of axes superimposed on it. The center of the co-ordinate axes (origin) is identified by the binary address of all 0's (only the X-axis is shown) and, therefore, conforms to the normal co-ordinate system in which the origin is identified as the zero point of both axes. This is done so that the Central Computer can treat the positioning of messages

by conventional computer methods. The need for describing the center of the X1 display as having an address of all 0's, however, results in a complication of console circuits which will become evident in the following analysis.

Sending a 1 bit to the binary decoder increases its analog output and causes deflection toward the right. A 0 bit at one of the decoder inputs reduces the decoder analog output and, therefore, tends to cause deflection to the left. An all-1-bit input produces maximum analog output voltage; an all-0-input produces minimum analog output voltage. A message address to all 0's, then, instead of producing deflection to the center of the tube, positions the message at the extreme left side. In this case, in order to ensure that a message ends up at the desired position on the viewing screen, the bit, entering the decoder as the most significant bit (LS), must be reversed. Instead of a 0 (−30V), a 1 (+10V) must be applied. Since both the 1 and 0 outputs of the LS bit register flip-flops are available in the console, this application of the 1 (+10V) can be done by switching via relay contacts. In the case of X2, X4, and X8 displays, a similar switching of the most significant bit may occur, but for a different reason.

To summarize, bits LS through L9, used for positioning a message on the X1 display, will all be 0 for a message that is located at the center of the tube. Bit LS, the sign bit, is still spoken of as a 0 bit, although the complement (1) has actually been sent to the decoder. If any of the magnitude bits are changed to 1, the decoder output will increase and deflection will be to the right. Thus, as long as the sign bit is a 0, the message will be located on the right half of the viewing screen. If the sign bit were at 1, a 0 would be sent to the decoder as the most significant bit. If all the remaining bits were also 0, the message would be positioned to the extreme left side of the tube, point A in figure 4–22. If any of the magnitude bits were then changed to 1's, the message would be deflected to the right but would never be deflected beyond the center of the tube. The LS bit, when a 1, signifies that the message will be on the left side of the tube.

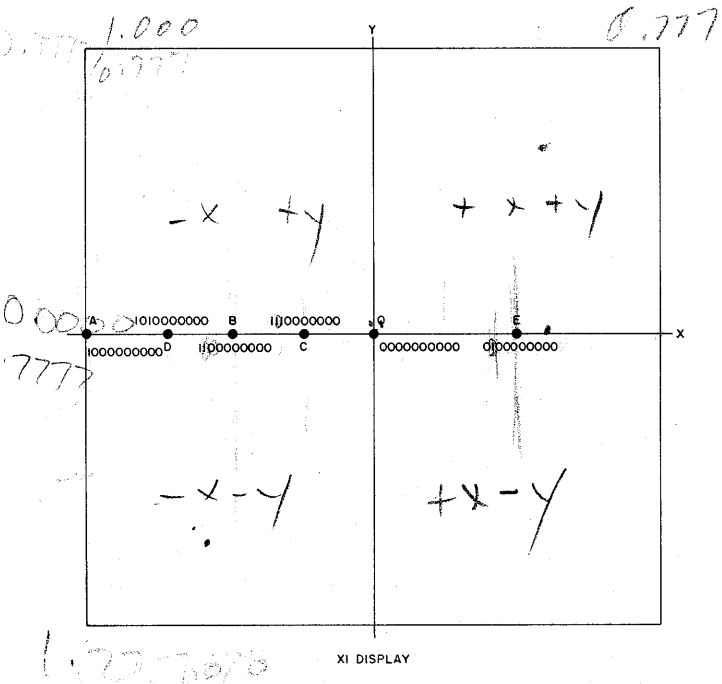


Figure 4–22. Co-ordinate System

The fact that message-positioning can never occur on the right side of X1 display (once the sign bit is 1) is explained by the relative significance of the bits and the corresponding weighting which the bits receive in the binary decoder. Each bit is half as significant as the previous bit in a message-positioning address; that is, each bit exerts one-half the effect on the message position that the previous bit did. The sign bit, we have seen, can exert the maximum influence on the message position, since it can select that half of the tube to which the message will be deflected. The next bit is weighted only half as much in the binary decoder so that the net change in decoder analog output voltage for the second bit is only half that obtained by the sign bit. Therefore, the L1 bit can cause deflection over one quarter of the viewing screen. It can be seen then that, if the message address describing point A in figure 4–22 is altered so that L1 is a 1, the message will be deflected to the right across one-quarter of the viewing screen to point B. Bit L2 is weighted half this much so that, if L2 is changed to a 1 bit, the message will be deflected across an additional one-eighth of the viewing screen to point C. Changing each of the remaining magnitude bits to 1 will move the message to the right, but by smaller and smaller decrements. The limit of the geometric series thus produced is the center of the viewing screen.

Note that the significance of each bit is independent of the stage of each previous bit. In the example given above, for instance, assume that the address describing point A is altered so that bit L2 is changed to a 1 but bit L1 is left at 0. Then the message will move across 1/8 of the tube to point D. If L3-L9 are then changed to 1's, the message will approach point B as a limit, rather than the center of the viewing screen. It will never, however, reach point B. When L3-L9 are all 1's, the message will be to the left of point B by the amount of the least significant digit, or will assume a position approximately several thousandths of an inch from point B.

In general, each point on the tube has two of the approximate addresses. The reason for this becomes apparent when the relative significance of the bits is con-

sidered. Since each bit is half as significant as the previous bit, the significance of any one bit is slightly greater than that of all subsequent bits, taken together. (A simple addition of fractions will verify this.) Thus, it is apparent that binary addresses 1100000000 and 1011111111 are approximately equivalent, differing only by the distance determined for the last digit.

An address of all 0's is considered to be the center of the tube, as shown in figure 4–22. Actually, this address produces deflection to a point slightly to the left of center of the screen. An address of all 1's describes a point slightly to the right of the geometrical center of the screen. The differences between the addresses are minute and are significant only in that the all-0 address will appear in an expansion of the left half of the screen, while the all-1 address will appear in an expansion of the right half of the viewing screen.

2.6 ROTARY SWITCH AND PLUGBOARD CONTROL

Each console, as a rule, will have different tactical requirements that necessitate specific expansion and off-centering. To enable each console to be patched (or switch-connected) to the various circuits providing these voltage gradients, a control panel is provided for each console. This panel may contain a rotary switch or a plugboard (some of the older consoles may still have plugboards), as an interconnection device.

Both the rotary switch and the plugboard are discussed here. To ensure sufficient coverage for each type, some overlapping or repetition may occur in describing each method. For example, the PRRE has always made use of rotary switches, and their description in Part 5, Chapter 2, was thought necessary (although somewhat analogous to that given here) to eliminate excessive cross-referencing.

2.6.1 Expansion and Off-Centering Rotary Switches

At any one time, the SD console can have, at the most, three different levels of expansion assigned to it. These three levels correspond to the three positions of the EXPANSION switch. In addition, if CNTD is X1 and NORM is X2, or if CNTD is X2 and NORM X4, the automatic off-centering that occurs when switching from CNTD to NORM can, at any one time, select only one of a possible nine different areas; if CNTD is X1 and NORM X4, there are 49 different area selections.

In order to simplify the changing of these assignments, a set of four rotary switches (shown in fig. 4–23) is provided at the rear of the console. The switches perform the following functions in the indicated areas:

S71-CONTRACT AREA: Perform expansion level and off-centering area assignments for CNTD position.

S72-SCALE: Perform expansion level assignments for NORM and EXPD positions.

S73-NORMAL AREA X: Perform X axis off-centering assignments in NORM position.

S74-NORMAL AREA Y: Perform Y axis off-centering assignments in NORM position.

A schematic of the circuits involved is shown in figure 4–24, foldout. The switches are connected to actuate the relays located at the top of the illustration. The relays consist of two groups: the expansion level relays at the upper right and the off-centering relays at the upper left. All of the relays are identified by a K number on the illustration, as well as an arbitrarily assigned letter designation. The latter will be used in the following subparagraphs. The expansion relays consist of Ex, Ey, Fx, Fy, Gx, Gy. Operation of relay Ex, for instance, means that both K58 and K59 are energized. In the case of the expansion relays, both x and y axis relays operate simultaneously in order that both axes display the same expansion level. The off-centering relays are referred to as Ax through Dx and Ay through Dy.

Figure 4–24 does not show the expansion relay contacts; it shows only the coils and circuitry which provide the energizing voltages. Later, it will be shown how operation of these relays produces the various expansion levels and off-centering selections. For the present, it is sufficient to know that relays Ex and Ey must be energized to produce an X1 display; Gx and Gy to obtain X4; and both the F and G relays to obtain X8. Expansion level X2 is obtained with all expansion relays de-energized.

The various off-centering selections are obtained by energizing the A, B, C, and D relays in various combinations. Figure 4–25 shows how the X1 display is divided into 15 overlapping segments in each axis. These basic segments are numbered 1-15. For X2 expansion, each axis is divided into 3 segments, as shown for the X axis. The first section includes segments 1-7, the second 5-11 and the third 9-15. The y axis is divided in the same manner. The result of this division is to provide the nine overlapping areas, any of which will fill the entire usable portion of the SD CRT in expansion level X2.

For X4 expansion, the X1 display has been divided into seven sections along each axis; this is also shown in figure 4–25 for the x axis. Each section consists of three of the basic segments with 50 percent overlap between each set of three. There are thus 49 divisions of the X1 display, any one of which will fill the SD CRT face in X4 expansion. In expansion level X8, one of the basic segments of the X1 display is expanded to fill the SD CRT face; there are, therefore, 225 possible X8 expansion segments.

2.6.1.1 Contracted Expansion Level and Area Assignment

CONTRACT AREA switch (S71) is used for setting the expansion level and off-centering for the CNTD position of the EXPANSION switch. As shown in figure 4–24, this switch has three sections: A, B, and C. The arms of all three sections are connected to ground through a contact of the EXPANSION switch, when the latter is in the CNTD position. Since one terminal of all the relay coils is connected to a —48V source, the other terminal need only be connected to ground to energize the relay. The three sections of S71 can only supply this ground when the EXPANSION switch is in the CNTD position.

Terminal 12 (position 1-15) of section C is connected to the E relays so that the Ex and Ey relays operate in the energized position and thus obtain an X1 display. There are no connections made to sections A and B in this position. Relays A-D are not energized, and, hence, there is no off-centering selection. This is to be expected since the X1 display is the frame of reference or unexpanded display. In positions 3 through 11, the E relays are not energized. The F and G relays are also not energized, and, hence, an X2 expansion is obtained. Each of these positions, in addition to selecting an X2 display, selects a different combination of segments in the x and y axes.

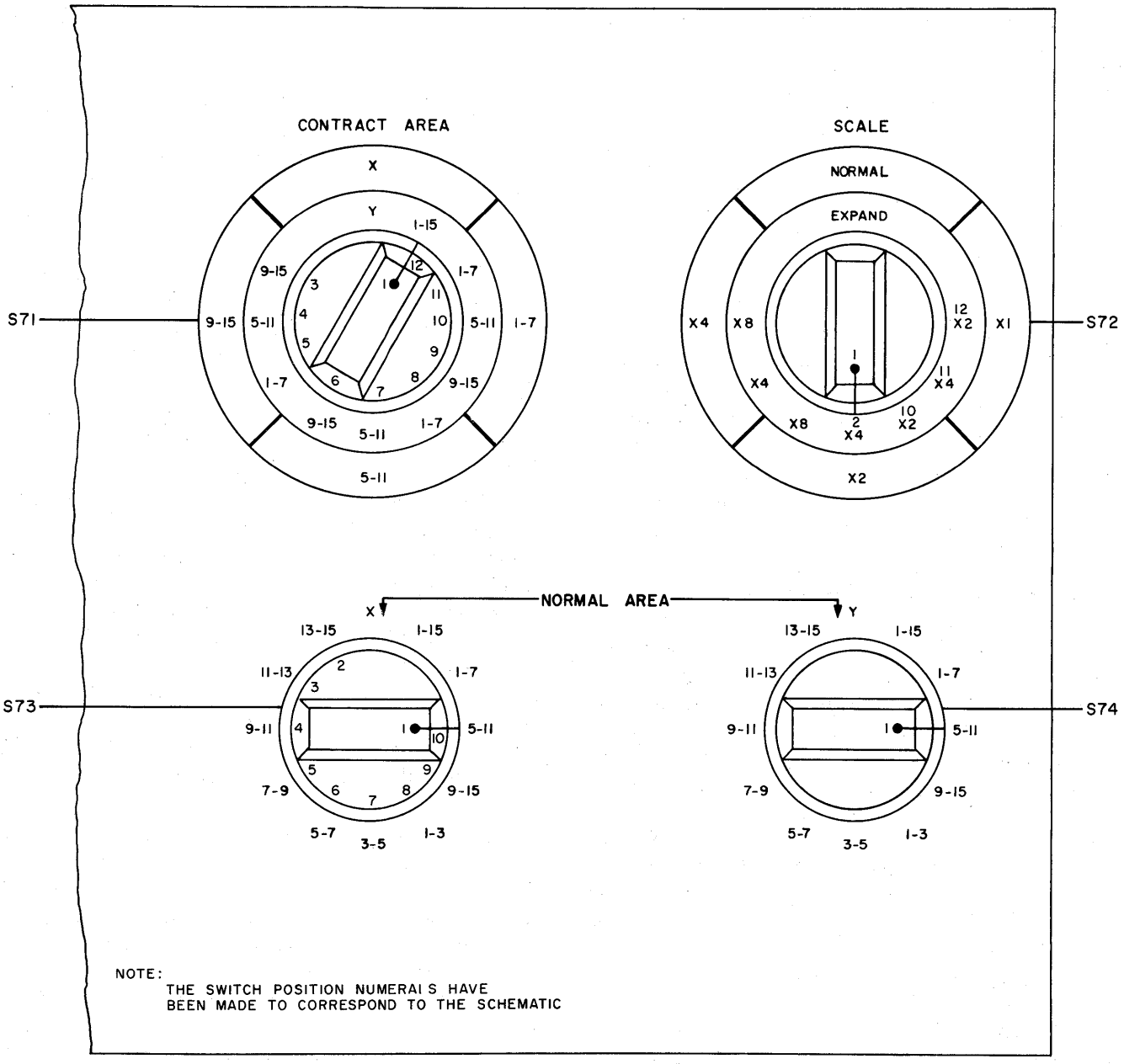


Figure 4–23. Expansion and Off-Centering Rotary Switches

Reference to table 4–1 shows that all three possible segment selections (1-7, 5-11, 9-15) require that relays C and D be energized for both x and y. This is accomplished by terminals 3-11 of section C. Sections A and B are used to energize the A and B relays, depending upon which segment is selected. For example, terminal 3 (position 9-15 in X and position 9-15 in Y) of section A energizes relay Ay; and, similarly, section B energizes relay Ax. The operation of relays A, B, and C selects, according to table 4–1, segments 9-15. In this case, segments are selected in each axis.

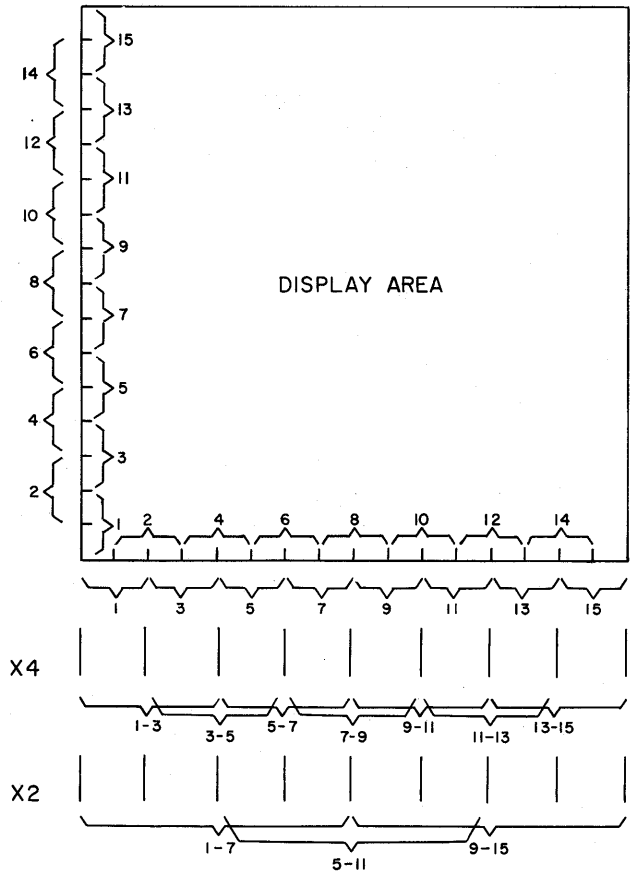


Figure 4–25. Division of X1 Display

2.6.1.2 Normal and Expanded Expansion Level Selections

The SCALE switch (S72), a 6-pole rotary switch, selects the expansion level for the NORM and EXPD positions of the EXPANSION switch (S28) by providing ground returns for the expansion relays through EXPANSION switch (S28) for section A in the NORM position, and for sections B and D in the EXPD position. Ground returns for the off-centering relays are provided through section C and through S28 in the NORM position. Sections E and F provide ground returns for off-centering relays Dx and Dy through S28 in the EXPD position.

As an example of how the switch functions, assume that S28 is in the NORM position and that S72 is at terminal 12 (NORMAL X1, EXPAND X2). Of the six switch sections, only A, E, and F will be in the circuit at this time. The arm of section A will receive a ground through S28 and will apply it to the E relays. Since sections E and F receive a ground through the EXPD position of S28, they are ineffective now. Thus, the switch has only accomplished the operation of the E relays and produced an X1 expansion level. If the EXPANSION switch (S28) is now turned to the EXPD

TABLE 4–1. CONTRACT AREA SWITCH (S71), OFF-CENTERING ASSIGNMENTS VERSUS RELAY OPERATION

SWITCH POSITION		TERMINAL	RELAYS	OPERATED
X	Y	See figs. 4–23 and 4–24	X	Y
–	1–15	12	–	–
1–7	1–7	11	CD	CD
1–7	5–11	10	CD	BCD
1–7	9–15	9	CD	ACD
5–11	1–7	8	BCD	CD
5–11	5–11	7	BCD	BCD
5–11	9–15	6	BCD	ACD
9–15	1–7	5	ACD	CD
9–15	5–11	4	ACD	BCD
9–15	9–15	3	ACD	ACD

position without turning S72, relays E will no longer operate. None of the expansion relays will now operate since terminal 12 of sections B and D is not wired, thereby producing an X2 expansion level. Sections E and F will operate the D relays since these relays are always energized in X2 and X4 expansions. Table 4–2 lists the expansion levels selected by the S72 for both NORM and EXPD.

2.6.1.3 Normal Area Off-Centering Selections

Sections E and F of the NORMAL AREA X and Y switches (S73 and S74) perform the function of off-centering area selection in the NORM position of S28. The arms of sections E and F and the Dx and Dy relays are returned to ground through terminals 6-10 (X2 and X4 expansion levels) of section C of S72 and the NORM position of S28, thus making operative combinations of the off-centering relays. Table 4–3 lists the selections made by switches S73 and S74 for NORM operation.

As shown in table 4–3, no relays are operated in position 1-15 (terminal 12) of switches S73 and S72, and, hence, no area selection occurs. In the other 10 positions of switches S72 and S73, reference to table 4–3 shows the NORMAL expansion level used with each position and the off-centering relays energized in each position.

2.6.1.4 Expanded Area Off-Centering Selections

Since the area that will be selected in the EXPD position of S28 will be a portion of the area selected in the NORM position, there is some necessary relation between NORM and EXPD. Sections A, B, C, and D of the NORMAL AREA X and Y switches (S73 and S74) perform this function. A similiar relationship between NORM and CNTD is not required since AN/FSQ-7 programming does not require that the NORM display necessarily be part of the CNTD display. (This, of course, is in cases where the CNTD off-center area displayed is on the X2 level of expansion.)

Off-centering selection for expanded operation is accomplished by the console operator by depressing one X axis and one Y axis pushbutton. One contact of each of the pushbuttons is grounded through the EXPD position of EXPANSION switch (S28), and one or more of the other contacts are wired through sections A, B, C, and D of switches S73 and S74 to the off-centering relays. As an example of operation, assume pushbutton Y4 (see fig. 4–24) is depressed and that S74 is on terminal 11. (This means the normal display was an X2 expansion level showing segments 1-7.) Assume also that an X8 expansion level is selected on the EXPAND scale of S72 (terminal 8). Since one contact of each pushbutton is grounded, depressing button Y4 grounds three leads. The first of these goes to S74, B12, and C11. Since S74 is on terminal 11, grounding of B12 is ineffective, but C11 provides a ground for relay Cy which is therefore energized. The second of the three leads goes to S74, B4, B10, C3, C5, and C7 and is therefore ineffective. Operation of pushbutton Y4 has therefore energized relays Cy and Dy. Reference to table 4–4 indicates that segment 4 is selected for display.

A comparison of table 4–4 with figure 4–24 indicates that the switches are wired so that each of the pushbuttons selects one of the segments that was displayed in the NORM position.

2.6.1.5 Incorrect Combinations

There are many ways to set up the expansion and off-centering switches incorrectly. For instance, seven pushbuttons are required for off-centering selection when NORM is X2 and EXPD is X8. This number is

TABLE 4–2. SCALE SWITCH (S72), EXPANSION LEVEL SELECTIONS

SWITCH POSITION		TERMINAL	RELAYS	OPERATED
NORMAL	EXPAND	(See figs. 4–23 & 4–24)	NORM	EXPD
X1	X2	12	E	–
X1	X4	11	E	G
X2	X2	10	–	–
X2	X4	9	–	G
X2	X8	8	–	F & G
X4	X4	7	G	G
X4	X8	6	G	F & G

TABLE 4–3. NORMAL AREA X AND Y SWITCHES (S73 AND S74), OFF-CENTERING ASSIGNMENTS VERSUS RELAY OPERATION

SWITCH POSITION	EXPANSION LEVEL (S72)	TERMINAL (See figs. 4–23 and 4–24)	RELAYS OPERATED
1–15	X1	12	–
1–7	X2	11	CD
5–11	X2	10	BCD
9–15	X2	9	ACD
1–3	X4	8	D
3–5	X4	7	CD
5–7	X4	6	BD
7–9	X4	5	BCD
9–11	X4	4	AD
11–13	X4	3	ACD
13–15	X4	2	ABD

necessary because each X2 display encompasses seven segments (1-7, 5-11, 9-15). Since only one segment is displayed in X8, there must be a choice provided for each of the seven. If NORM is X4, only three segments are displayed (1-3, 3-5, 5-7, etc.), and, hence, if EXPD were X8, only three pushbuttons (2, 4, 6) are required. In this case, under normal circumstances, four of the pushbuttons are masked off. There exists the possibility, however, that the SD console is assigned X2 in NORM and X8 in EXPD (requiring seven pushbuttons), and, yet, SCALE switch (S72) is mis-set to select X4 (terminal 6 instead of terminal 8) for the NORM display. The four unneeded pushbuttons are now unmasked and can be used to select meaningless combinations of relay operation by the console operator. There are a number of other ways in which meaningless relay combinations can be obtained, so great care on the part of the technician is required when he changes the expansion and off-centering requirements of the console. One rule that can be followed is that seven buttons are required if the EXPD level is four times the NORM level (X4 and X1, or X8 and X2). If the EXPD level is only twice the NORM level (X2 and X1, X4 and X2, or X8 and X4), only three pushbuttons are required.

2.6.2 Plugboard

The plugboard (or control panel) is shown in figure 4–26, and its associated circuits are shown in figure 4–27, foldout, and are discussed in logic 4.2.2. It has been divided into three sections, as shown for ease of understanding. This division does not correspond to the actual physical layout of the plugboard.

TABLE 4–4. OFF-CENTERING ASSIGNMENTS VERSUS RELAY OPERATION, X8 EXPANSION

SEGMENT SELECTION	RELAYS OPERATED
1	–
2	D
3	C
4	CD
5	B
6	BD
7	BC
8	BCD
9	A
10	AD
11	AC
12	ACD
13	AB
14	ABD
15	ABC

Connections are made in the control panel by the insertion of bottle plugs. The bottle plug is a 2-pronged plug which fits into two adjacent jacks on the board. For

ease of illustration, the two jacks which receive the bottle plug are shown on the diagram as one jack (an open circle). The two lines which intersect at each jack are not connected to each other until a plug is inserted. Without the plug, both lines bypass the jacks. For example in the lower section (marked section 3 on the drawing), any of the horizontal lines, marked 1x-16x, can be connected by means of plugs to any of the four lines running up to the four X off-centering relays.

The relays concerned here are identified by a K number on the illustration. For ease of discussion, however, the relays will be identified by means of a letter designation also shown on the diagram. Thus, the expansion relays consist of Ex, Ey, Fx, Fy, Gx, and Gy. Operation of relay Ex, for instance, means that both K58 and K59 have operated. Similarly, the off-centering relays are referred to as relays Ax-Dx and Ay-Dy.

2.6.2.1 Plugboard Section 1

The jacks in this section are used for connecting the expansion relays to the EXPANSION switch in such a manner that the three positions of the EXPANSION switch will correspond to the type of displays assigned to the particular console. There is a specific relay assignment for each level of expansion. Once it is known which expansion levels are to be assigned to each of the three positions of the EXPANSION switch, the corresponding part of the control panel can be patched up.

For instance, to produce an X1 expansion, relays Ex and Ey must be operated. (In all cases, X and Y expansion relays are operated at the same time to avoid the possibility of having one expansion in the X direction and another in the Y direction. The above arrangement is wired into the console, and the operator need not concern himself with it.) Four poles of the EXPANSION switch are shown, connected to the first section of the control panel. For example, if the CNTD position is to produce an X1 display, the Cs line going to the relay line is plugged so that relay operation will be secured at this position of the switch. By plugging the Ns 1 or Ns 2 on the E relay line, an X1 display can be obtained in the NORMAL position of the switch.

For an X2 display, none of the expansion relays should operate; hence, no plugs are used on whatever switch position is devoted to the X2 display. For an X4 display, relay G must operate. An X8 display may be assigned to either the NORMAL or EXPANDED posi-

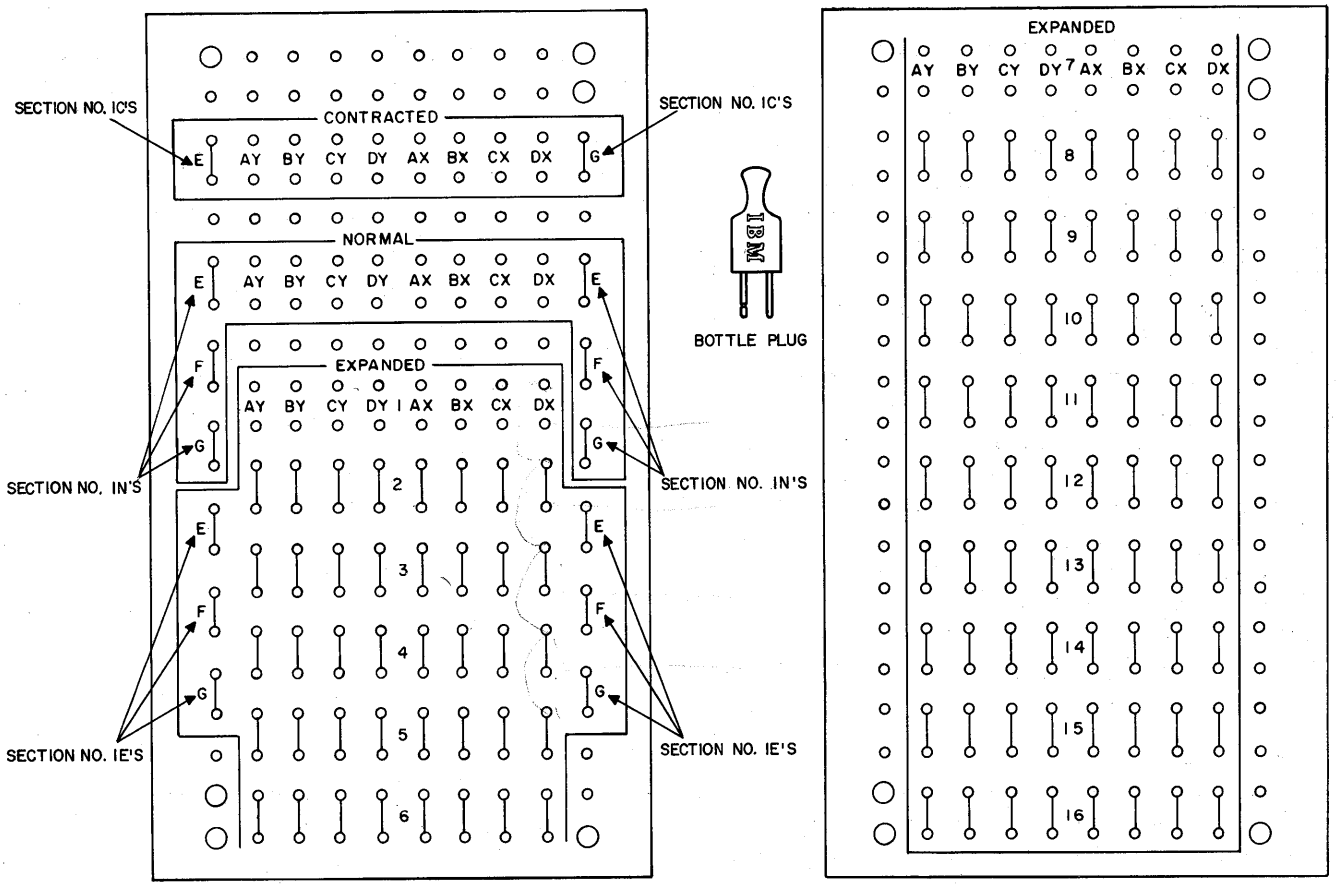


Figure 4–26. Expansion and Off-Centering Plugboards (Control Panel)

tions of the EXPANSION switch. Regardless of which position the X8 display is to assume, however, the two relays are not patched to the same pole of the EXPANSION switch. If relays F and G are to be patched up to the EXPANDED position, one of them should be plugged to the ES 1 line and the other to the ES 2 line. If they were both plugged to the same line, two relays would remain interconnected permanently by means of the horizontal line between jacks so that, if relay G remained connected for the NORMAL position, relays F and G would also operate in the NORMAL position. Therefore, whenever two of the EXPANSION relays are to be connected to a particular EXPANSION switch position, they should always be connected to different sections of the switch.

2.6.2.2 Plugboard Section 2

As stated previously, the console operator has no control over the segment of the CONTRACTED display that he sees when the EXPANSION switch is turned to NORMAL. This segment is assigned to the console on a tactical basis. Likewise, if the CONTRACTED display is anything but an X1 display, the particular segment that will be seen in CONTRACTED is assigned.

This assignment of off-centering position is accomplished through the use of control panel section 2. The off-centering relays, Ax through Dx and Ay through Dy, are connected to control panel section 2 through eight poles of the EXPANSION switch. In the CONTRACTED position, any of the eight relays can be connected by means of a plug to the Cs line. In the NORMAL position, they can be connected to the Ns 1 line. In this way, the —48V return for any of the relays can be completed through the switch, thus achieving operation.

Figure 4–25 shows how the X1 display is divided into 15 overlapping segments in each axis. For an X2 expansion, each axis is divided into three sections, as shown in the figure. The first section consists of segments 1-7, the second section consists of segments 5-11, and the third section consists of segments 9-15. The Y-axis is divided up in the same way. The result of this division is to provide nine overlapping areas, any one of which will fill the entire usable portion of the SD CRT when an X2 expansion is being displayed.

For an X4 expansion, the X1 display has been divided up into seven sections along each axis. This is also shown in figure 4–25. Each section is seen to consist of three of the basic segments with 50-percent overlap between each set of three. There are, thus, 49 divisions of the X1 display, any one of which will fill the SD CRT face when an X4 expansion is displayed.

The remaining level of expansion is the X8 display. In this expansion, one of the basic segments of the X1 display is expanded to fill the SD CRT face; there are, thus, 225 possible X8 expansions.

To produce display of any particular segment of the X1 display in an X2, X4, or X8 expansion requires a different combination of relays. Table 4–5, part A, summarizes the relay connections that must be made to assign any particular segment to the CNTD position of the EXPD switch. For instance, if the X2 expansion is assigned to the CNTD position, there will be three possible assignments of sector in each axis. Inserting plugs on the Cs line for relays Cx and Dx will produce, in the x axis, the display of segments 5-11. For an X4 expansion, there are seven choices in each axis, as shown.

Table 4–5, part B, provides the same information for the NORM position of the switch. Note that this position can be assigned an X8 expansion and, therefore, has 225 possibilities for that display.

2.6.2.3 Plugboard Section 3

This section of the plugboard is devoted to the OFF-CENTERING switches and contains the jacks that are connected to the off-centering relays through the EXPD position of the EXPANSION switch. Table 4–5, part C, summarizes the connections that must be made for each OFF-CENTERING button for each level of expansion.

Column 1 of table 4–5, part C, describes those connections that are needed for producing an X2 display in the EXPD position. As stated earlier, none of the expansion relays is to be operated for this level of expansion, and, hence, control panel section 1 is not plugged. Since the EXPD display is to be X2, the largest number of OFF-CENTERING buttons needed will be three. (NORMAL is X1 and, therefore, an X2 expansion can provide only nine segments to choose from. This can be seen from figure 4–25. If NORM is X2, then no expansion is possible between the NORM and EXPD positions.) Thus three buttons are required for each axis. Examination of table 4–5, part C, will reveal that, for the EXPD position of the switch, the OFF-CENTERING buttons accomplish precisely what is performed by the patching done on control panel section 2. In the example used in plugboard section 2, segments 5 through 11 were selected for the X-axis by energizing relays Bx, Cx, and Dx. To wire up OFF-CENTERING button IV to accomplish the same thing requires that leads 6x, 7x, and 8x (see fig. 4–27, fold-out) be connected to relays Bx, Cx, and Dx, respectively. In this manner, identical relay operation is achieved, although the return for the relays is now picked up through the first contact of OFF-CENTERING button IV.

For an X4 display in the EXPD position, there are two possibilities, depending on whether the NORM display is X2 or X1. In the case of the X1 NORM DISPLAY, there will be 49 possible sectors to select from for an X4 EXPD display, and hence seven buttons in

each axis are required. (See fig. 4–25.) Column 5 of table 4–5 is applicable here. If the NORM display is an X2 expansion, however, there will be only three sectors to choose from in each axis, and, hence, only three OFF-CENTERING buttons in each will be required since the X2 expansion will have already selected a particular area from the X1 display. Information is provided in the table for the three possibilities in each axis. Thus, if the X2 expansion had selected segments 1-7, the OFF-CENTERING buttons would be wired up as shown in column 2. Columns 3 and 4 provide the information needed for the other two possibilities.

There are again the two major possibilities for the X8 display in the EXPD position. If the NORM position is an X2 expansion, segments 1-7, for example, there will be 49 possible EXPD displays, and all OFF-CENTERING buttons will be required. In this case, columns 13, 14, and 15 are applicable. If the NORM display is an X4 expansion, only three pushbuttons are required in each axis, and columns 6-12 are applicable. In any case, the X8 expansion will produce display of only one of the basic segments of the X1 display.

2.6.2.4 Situation Display Test Pattern Switch

The —48V return for the expansion and off-centering relays in the CNTD, NORM, and EXPD positions of the EXPANSION switch is obtained through one section of the SD test pattern switch. When this switch is in either of the TEST positions, only the E expansion relays are operated, thereby ensuring an X1 display for the test pattern.

2.6.2.5 Control Panel Layout

The actual expansion control panel consists of two separate boards located in the rear of the console and shown in figure 4–26. The board shown at the left contains three labeled areas: CNTD, NORM, and EXPD. The board shown on the right is devoted entirely to EXPD. In each labeled area, both the expansion and off-centering relays are brought out to jacks.

The 2-pronged bottle plugs are made to fit into adjacent horizontal rows (see fig. 4–26). In the CNTD area, pairs of jacks, labeled E and G, are shown with a vertical line between the two jacks of a pair. The vertical line shows the way in which the plug is to be inserted. A number of these vertical lines are drawn on both boards. They do not, as in the case of the category board, indicate an electrical connection. Their sole purpose is to indicate which jacks are paired together so

TABLE 4–5. EXPANSION AND OFF-CENTERING PLUGBOARD CONNECTIONS

A

S28, EXPANSION-SWITCH POSITION	OFF-CENTERING ASSIGNMENTS, CONTRACTED											
EXPANSION SCALE	X1	X2			X4							
PLUGBOARD SECTION I Cs TO (SEE NOTE 1)	E	OPEN			G							
OFF-CENTER POSITION, X AXIS (SEE NOTE 2)	1-15	1-7	5-11	9-15	1-3	3-5	5-7	7-9	9-11	11-13	13-15	
CONTRACTED SECTION OF PLUGBOARD (SEE NOTE 3)	OPEN	$C_X D_X$	$B_X C_X D_X$	$A_X C_X D_X$	D_X	$C_X D_X$	$B_X D_X$	$B_X C_X D_X$	$A_X D_X$	$A_X C_X D_X$	$A_X B_X D_X$	
OFF-CENTER POSITION, Y AXIS (SEE NOTE 2)	1-15	1-7	5-11	9-15	1-3	3-5	5-7	7-9	9-11	11-13	13-15	
CONTRACTED SECTION OF PLUGBOARD (SEE NOTE 3)	OPEN	$C_Y D_Y$	$B_Y C_Y D_Y$	$A_Y C_Y D_Y$	D_Y	$C_Y D_Y$	$B_Y D_Y$	$B_Y C_Y D_Y$	$A_Y D_Y$	$A_Y C_Y D_Y$	$A_Y B_Y D_Y$	

NOTE:
1. REFER TO FIGURE 3-8 FOR PLUGBOARD SECTION LOCATION.
2. REFER TO FIGURE 3-10 FOR SECTOR LOCATIONS.
3. REFER TO FIGURE 3-8 FOR LOCATION OF TERMINALS TO BE SHORTED.

B

S28, EXPANSION-SWITCH POSITION	OFF-CENTERING ASSIGNMENTS, NORMAL											
EXPANSION SCALE	X1	X2			X4							
PLUGBOARD SECTION I Ns TO (SEE NOTE 1)	E	OPEN			G							
OFF-CENTER POSITION, X AXIS (SEE NOTE 2)	1-15	1-7	5-11	9-15	1-3	3-5	5-7	7-9	9-11	11-13	13-15	
NORMAL SECTION OF PLUGBOARD (SEE NOTE 3)	OPEN	$C_X D_X$	$B_X C_X D_X$	$A_X C_X D_X$	D_X	$C_X D_X$	$B_X D_X$	$B_X C_X D_X$	$A_X D_X$	$A_X C_X D_X$	$A_X B_X D_X$	
OFF-CENTER POSITION, Y AXIS (SEE NOTE 2)	1-15	1-7	5-11	9-15	1-3	3-5	5-7	7-9	9-11	11-13	13-15	
NORMAL SECTION OF PLUGBOARD (SEE NOTE 3)	OPEN	$C_Y D_Y$	$B_Y C_Y D_Y$	$A_Y C_Y D_Y$	D_Y	$C_Y D_Y$	$B_Y D_Y$	$B_Y C_Y D_Y$	$A_Y D_Y$	$A_Y C_Y D_Y$	$A_Y B_Y D_Y$	

B (CONT'D)

S28, EXPANSION-SWITCH POSITION	OFF-CENTERING ASSIGNMENTS, NORMAL (CONT'D)														
EXPANSION SCALE	X8														
PLUGBOARD SECTION I N_S TO	G AND F (ON OPPOSITE SIDES)														
OFF-CENTER POSITION, X AXIS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
NORMAL SECTION OF PLUGBOARD	OPEN	D_X	C_X	$C_X D_X$	B_X	$B_X D_X$	$B_X C_X$	$B_X C_X D_X$	A_X	$A_X D_X$	$A_X C_X$	$A_X C_X D_X$	$A_X B_X$	$A_X B_X D_X$	$A_X B_X C_X$
OFF-CENTER POSITION, Y AXIS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
NORMAL SECTION OF PLUGBOARD	OPEN	D_Y	C_Y	$C_Y D_Y$	B_Y	$B_Y D_Y$	$B_Y C_Y$	$B_Y C_Y D_Y$	A_Y	$A_Y D_Y$	$A_Y C_Y$	$A_Y C_Y D_Y$	$A_Y B_Y$	$A_Y B_Y D_Y$	$A_Y B_Y C_Y$

TABLE 4–5. EXPANSION AND OFF-CENTERING PLUGBOARD CONNECTIONS (cont'd)

C

S28, EXPANSION-SWITCH POSITION		OFF-CENTERING ASSIGNMENTS, EXPANDED				
EXPANSION SCALE		X2	X4			
PLUGBOARD SECTION I E_s TO (SEE NOTE 1)		OPEN	G			
NUMBER OF PUSHBUTTONS		3	3			7
NORMAL PLUGBOARD SECTION SET FOR EXPANSION RATIO		X1	X2			X1
PUSHBUTTON NUMBER		II / IV / VI	II / IV / VI	II / IV / VI	II / IV / VI	I / II / III / IV / V / VI / VII
OFF-CENTER POSITION OF PUSHBUTTON (SEE NOTE 2)		1-7 / 5-11 / 9-15	1-3 / 3-5 / 5-7	5-7 / 7-9 / 9-11	9-11 / 11-13 / 13-15	1-3 / 3-5 / 5-7 / 7-9 / 9-11 / 11-13 / 13-15
EXPANDED PORTION OF PLUGBOARDS J35 & J36 (SEE NOTE 3)	ROW #1	*	*	*	*	D_x
	2	C_x	D_x	B_x	A_x	C_x
	3	D_x	OPEN	D_x	D_x	D_x
	4	*	*	*	*	B_x
	5	*	*	*	*	D_x
	6	B_x	C_x	B_x	A_x	B_x
	7	C_x	D_x	C_x	C_x	C_x
	8	D_x	OPEN	D_x	D_x	D_x
	9	*	*	*	*	A_x
	10	*	*	*	*	D_x
	11	A_x	B_x	A_x	A_x	A_x
	12	C_x	D_x	D_x	B_x	C_x
	13	D_x	OPEN	OPEN	D_x	D_x
	14	*	*	*	*	A_x
	15	*	*	*	*	B_x
	16	*	*	*	*	D_x

C (CONT'D)

S28 EXPANSION SWITCH POSITION		OFF CENTERING ASSIGNMENTS-EXPANDED (CONT'D)									
EXPANSION SCALE		X8									
PLUGBOARD SECTION I E_s TO		G AND F (ON OPPOSITE SIDES)									
NUMBER OF PUSHBUTTONS		3							7		
NORMAL PLUGBOARD SECTION SET FOR EXPANSION RATIO		X4							X2		
PUSHBUTTON NUMBER		II / IV / VI	II / IV / VI	II / IV / VI	II / IV / VI	II / IV / VI	II / IV / VI	II / IV / VI	I / II / III / IV / V / VI / VII	I / II / III / IV / V / VI / VII	I / II / III / IV / V / VI / VII
OFF-CENTER POSITION OF PUSH BUTTON		1 / 2 / 3	3 / 4 / 5	5 / 6 / 7	7 / 8 / 9	9 / 10 / 11	11 / 12 / 13	13 / 14 / 15	1 / 2 / 3 / 4 / 5 / 6 / 7	5 / 6 / 7 / 8 / 9 / 10 / 11	9 / 10 / 11 / 12 / 13 / 14 / 15
EXPANDED PORTION OF PLUGBOARDS J35 & J36 (SEE NOTE 3)	ROW #1	*	*	*	*	*	*	*	OPEN	B_x	A_x
	2	OPEN	C_x	B_x	B_x	A_x	A_x	A_x	D_x	B_x	A_x
	3	OPEN	OPEN	OPEN	C_x	OPEN	C_x	B_x	OPEN	D_x	D_x
	4	*	*	*	*	*	*	*	C_x	B_x	A_x
	5	*	*	*	*	*	*	*	OPEN	C_x	C_x
	6	D_x	C_x	B_x	B_x	A_x	A_x	A_x	C_x	B_x	A_x
	7	OPEN	D_x	D_x	C_x	D_x	C_x	B_x	D_x	C_x	C_x
	8	OPEN	OPEN	OPEN	D_x	OPEN	D_x	D_x	OPEN	D_x	D_x
	9	*	*	*	*	*	*	*	B_x	A_x	A_x
	10	*	*	*	*	*	*	*	OPEN	OPEN	B_x
	11	C_x	B_x	B_x	A_x	A_x	A_x	A_x	B_x	A_x	A_x
	12	OPEN	OPEN	C_x	OPEN	C_x	B_x	B_x	D_x	D_x	B_x
	13	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	C_x	OPEN	OPEN	B_x
	14	*	*	*	*	*	*	*	B_x	A_x	A_x
	15	*	*	*	*	*	*	*	C_x	C_x	B_x
	16	*	*	*	*	*	*	*	OPEN	OPEN	C_x

* ROW NOT IN CIRCUIT

NOTE: ROWS 1–16 SHOWN FOR X COLUMNS ONLY, DUPLICATE FOR Y COLUMNS.

that there will be no doubt in which two jacks a particular bottle plug is to be inserted.

To obtain operation of any of the labeled relays, the bottle plug is inserted in the pair of jacks corresponding to that relay. To produce an X4 expansion in the NORM position, a plug is inserted in either of the two pairs of G jacks shown in the NORM area. Any particular off-centering can then be selected by plugging in the off-centering relays, according to the information given in table 4–5, part B.

The EXPANDED area of the control panel is treated in the same manner as the other two areas. Each line of jacks is numbered to correspond with the numbering given in table 4–5, part C, shown on the schematic diagram, figure 4–27. In this area, as in the NORM area, there are two pairs of jacks for each of the expansion relays. Each pair corresponds to a different section of the EXPANSION switch. As explained in plugboard section 1, whenever two expansion relays are to be operated in a particular position of the switch, they are never operated from the same section of the switch. Expansion relay jacks on the same side of the control panel correspond to the same section of the EXPANSION switch. Thus, when plugging the control panel for an X8 expansion (relays F and G), the F jacks that are used must be on the opposite side of the board from the G jacks.

2.6.3 Magnitude Bit Selection

Figure 4–28 and logic 4.2.2 show the contacts of the expansion relays that are used for positioning the selection, exclusive of the most significant bit. Nine of the ten inputs to the binary decoder are shown at the right of the illustration. The tenth decoder input, corresponding to the most significant bit, is discussed in 2.6.4.

A number of relay contacts for the three expansion relays are shown. In each group of contacts that feed one of the binary decoder inputs, there is one armature and two contacts from each of the three expansion relays. Only the X-positioning circuits are shown, since the Y section is identical except for nomenclature.

Considering the case of the X1 expansion, assume that only the E relay is operated. The only bit of the first four that can be on the digit 1 line will be L1. An open circuit will be present for each of the other three bits. If each group of contacts is traced, it will be found that for the X1 display, positioning bits L1-L9 will be admitted to the binary decoder on the digit 1-9 lines, respectively.

For the X2 expansion, when no relays are operated, bits L2-L10 will be admitted to the decoder. For an X4 expansion, when relay G is operated, bits L3-L11 will go to the decoder. For an X8 expansion, bits L4-L12 will get through the contacts to the decoder. Note that the selection of inputs 1-9 to the decoder is dependent only on the expansion level selected by the EXPANSION switch. Off-centering does not play a part in it.

2.6.4 Digit 0 Selection, X2 Expansion

Figure 4–29 illustrates the X-axis contacts which are used for message intensification and digit 0 selection. It is to this part of the message-positioning circuitry that both the 1 and 0 sides of the LS-L3 bits are connected.

The expansion relay contacts involved in the selection of digit 0 are at the bottom of the illustration. Each of the three expansion relays is involved in a relay tree which is connected into various points in the network of off-centering relay contacts. The number of possible signals that could go out as digit 0 are seven, two sides of each of the three bits and the 0 side of the LS bit. The bit that is selected will depend both on the expansion and the off-centering of the display.

If an X1 expansion is being displayed, only relay E of the expansion relays will be operated, and, hence, only one of the seven bits can get through as digit 0; namely, that from the 0 side of the LS register flip-flop through the normally open Ex-1 contact. If a message had arrived at the console with all of its positioning bits 0, nine bits would go to the decoder as digits 1-9, but the most significant bit, LS, would go to the decoder on the digit 0 line as a 1. (The output of the 0 side of a flip-flop will be a 1 if the output of the 1 side is a 0.) Thus, an address which consisted of all 0's has been converted (as far as the binary decoder is concerned) into an address containing a 1 followed by nine 0's. The resultant message position will be at the ~~extreme left~~ center of the viewing screen. If the LS bit had not been reversed in the manner described, the message would have been positioned at the ~~center~~ left of the tube, since putting all 0's into the decoder produces a minimum output analog voltage. If the input address had been a 1 followed by all 0's, the LS bit would still be reversed so that the message address going into the decoder would be all 0's, producing deflection to the extreme left side of the tube. In this manner, the most significant bit is used to select which half of the tube the message will appear on. At the same time, this bit (the sign bit) is treated by the decoder in the same way it treats each of the magnitude bits. In other words, the decoder does not know that the LS bit is the sign bit. (It apparently is only another magnitude bit.) Thus, it is the relays which give the sign bit its ability to select the correct side of the tube for a given message display.

If an X2 expansion is being displayed, none of the expansion relays will be operated, and the only way for a bit to go out on the digit 0 line is for it to go through normally closed contacts Ex-1 and Gx-1. This means that the most significant bit going to the binary decoder will be either the 1 or 0 side of the L1 bit, depending

on the operation of the off-centering relays Bx, Cx, and Dx.

Reference to table 4–5, part A, will show that there are three combinations of off-centering relay operations during the display of an X2 expansion. The three combinations are Cx and Dx for segments 1-7; Bx, Cx, and Dx for segments 5-11; and Ax, Cx, and Dx for segments 9-15.

When Cx and Dx are operated, the 1 side of the L1 bit goes through normally closed contact Bx-3 and normally open contacts Cx-2 and Dx-2. Thus, when selecting segments 1-7, no sign bit reversal takes place. The reason for not reversing the most significant bit in this case becomes apparent when it is considered how the SD console produces an expanded display. By turning to an X2 expansion, the 10 bits going to the binary decoder are switched from LS-L9 to L1-L10. The ability to select the half of the screen on which the message appears is now apparently lost since the LS bit, which formerly accomplished this, is no longer sent to the decoder. The L1 bit is now sent in its place as the most significant bit. This results in an uncertainty of message positioning since messages on both sides of the tube in an X1 expansion could have the same L1 bit. For instance, in figure 4–22, points B and E both have a 1 for the L1 bit, and, yet, they are on opposite sides of

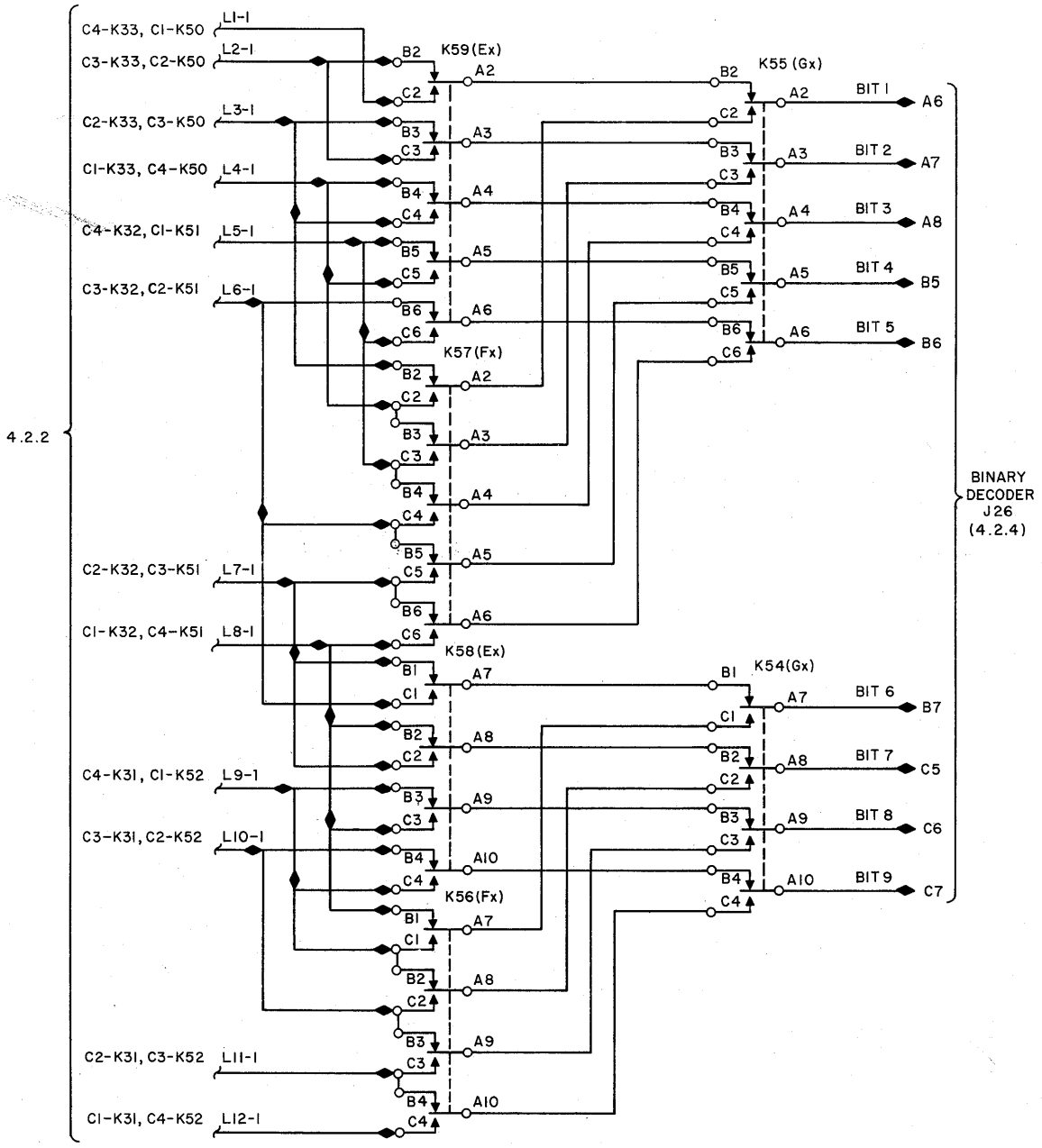


Figure 4–28. Magnitude Bit Selection Relay Contact

the viewing screen. Obviously, the L1 bit cannot perform the task of selecting the half of the screen on which to display the message.

What has happened (when switching to an X2 expansion) can be visualized by stretching what was formerly on the left side of the X1 display over the entire face of the tube so that what was formerly the center of the display is now on the extreme right side of the tube. At the same time, the right side of the X1 display has similarly been spread over the entire surface of the tube so that there are actually two superimposed areas, one corresponding to segments 1-7 and the other corresponding to segments 9-15. Message locations which were formerly on the left side of segments 1-7 (first quarter of the tube) are now located in the entire left side of the tube. Message locations formerly occupying the right side of segments 1-7 are now spread out through the entire right side of the tube. Similarly, the right and left sides of segments 9-15 now occupy the entire right and left sides of the tube. This is what constitutes the X2 expansion; it will be explained later how the expansion circuits send a gate to the intensify circuits so that messages in only one of these two superimposed areas became intensified. But it can now be seen why the L1 bit is not reversed in the X2 expansion, as the LS bit is in the X1 display. There is no longer any need for selecting half of the tube for display purposes; this job is now performed by the intensify circuits.

It can also be seen now how the spacing between messages in the X1 display is doubled in the X2 display. Since the LS bit is not used now for positioning, the L1 bit is twice as significant as it formerly was. Thus, two messages having a 1 and a 0 for the L1 bit will be twice as far apart as formerly because the bits produce twice as much differential output in the binary decoder. This

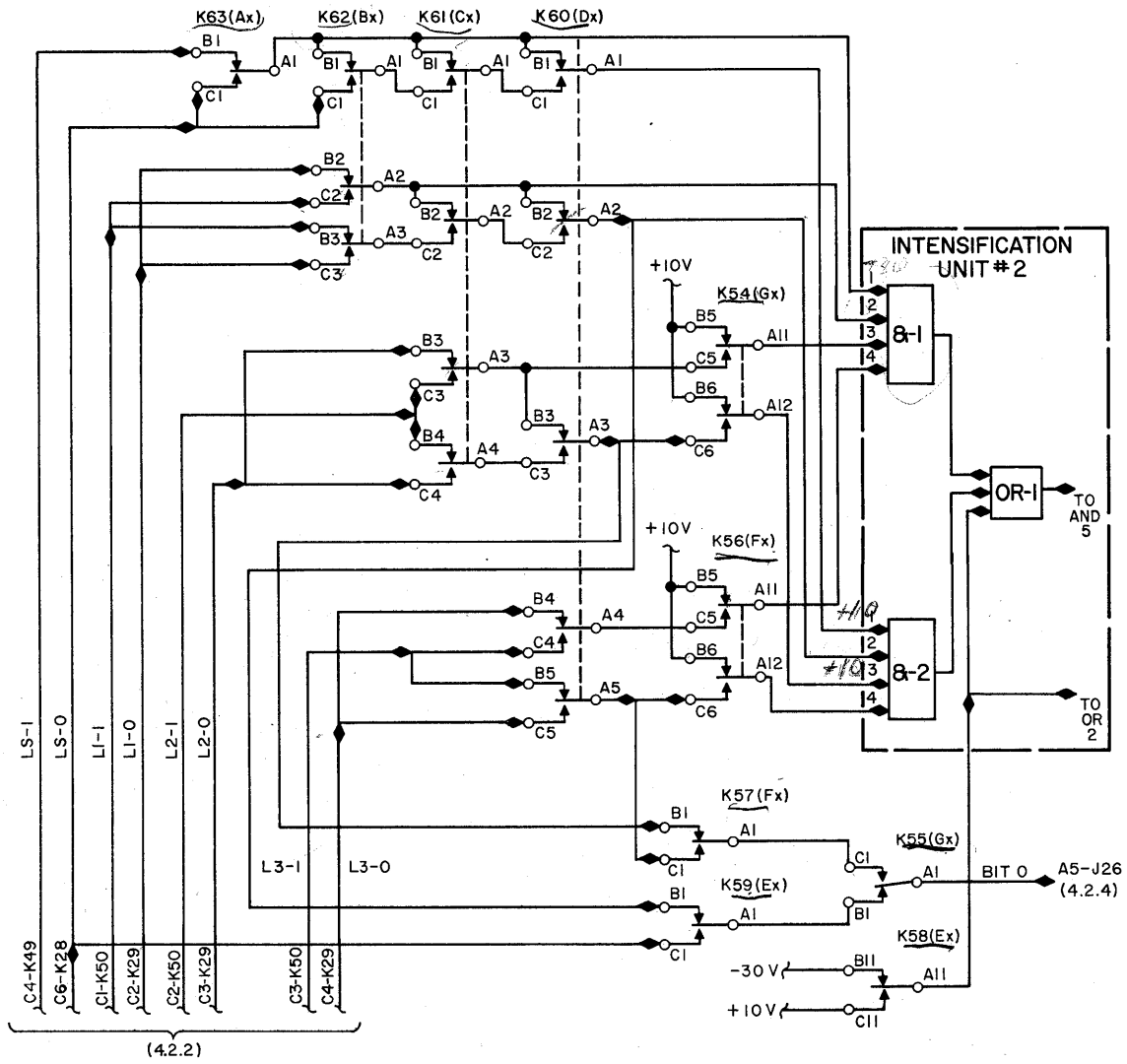


Figure 4–29. Digit 0 Selection and Intensification Selection

follows from the fact that they are going in on the digit 0 line, instead of the digit 1 line. Two messages which have the same L1 bits, but different L2 bits, will similarly be spaced twice as far apart as before because the L2 bits now go into the decoder on the digit 1 line instead of the digit 2 line and are, therefore, twice as influential as formerly in affecting message position. The same discussion applies to all of the bits of the address. Segments 9-15 are selected for an X2 expansion by relays Ax, Cx, and Dx. The Ax relay does not enter into the selection of the digit 0. However, as far as positioning bits are concerned, this will be the same situation as that for the selection of segments 1-7; that is, the 1 side of the L1 bit is selected as the digit 0 and there is no reversal of the sign bit. The difference in circuit operation occurs in the intensify circuitry where, because of the operation of relay Ax, only the messages that were formerly in segments 9-15 (right half of the X1 display) will be displayed.

To select the center section of the X1 display for the X2 expansion (segments 5-11), relays Bx, Cx, and Dx must operate. Tracing out the circuitry associated with the L1 bit will reveal that only the 0 side of the L1 bit can get through to the decoder by means of operated contacts Bx-3, Cx-2, and Dx-2. This means that, as in the X1 display, there is a reversal of the most significant bit.

The reversal is necessary, here, because of the way in which the center segments of the X1 display are selected for an X2 expansion. As explained in connection with the X2 expansions discussed above, areas of the X1 display are selected for expanded viewing by altering the set of position bits sent to the binary decoder and by not intensifying messages that belong in segments other than the ones desired for display. In expanding segments 1-7, segments 9-15 were not intensified. There are, however, two areas capable of being displayed simultaneously on the SD CRT; the areas are an expansion of segments 1-7 and an expansion of segments 9-15. Only the first was intensified. In the second case (discussed above), only segments 9-15 were intensified. Now, however, there arises the problem of intensifying the right half of segments 1-7 and the left half of segments 9-15; these constitute segments 5-11 as shown in figure 4–30.

But the right half of expanded segments 1-7 is now on the right half of the tube and the left half of segments 9-15 is now on the left of the tube. Both are in the wrong half of the tube as far as an X2 expansion of the 5-11 segments is concerned. That is, the right half of segments 1-7, which comprise the left half of segments 5-11, is on the right half of the tube although intensification of the 5-11 segments would require it to be on the left half. Therefore, when selecting these segments, the most significant bit is reversed so that the right half of the 1-7 segments falls on the right half the tube. The intensifying circuitry at the same time illuminates only those messages falling in the selected segments, 5-11.

2.6.5 Digit 0 Selection, X4 Expansion

When an X4 expansion is being displayed, expansion relay G is operated so that the bit which becomes digit 0 in the decoder can only come from the circuits associated with the L2 bit by passing through normally closed contact Fx-1 and normally open contact GX-1. Inspection of table 4–5 shows that there are seven areas along the x axis that can be selected and there are seven combinations of off-centering relays with which to obtain the selection.

As before, the message-positioning circuitry selects the desired display by intensification, thus allowing the positioning bits of all messages to get to the binary decoder but intensifying only those messages in the desired area. Therefore, in the X4 expansion, there are, in effect, four superimposed areas consisting of segments 1-3 expanded to cover the entire tube; segments 5-7 expanded in the same way, etc. Only messages in the selected segments are intensified. For purposes of message-positioning, there is still the problem of ensuring that the messages end up on the correct half of the tube. For instance, with segments 1-3, no sign bit reversal is necessary since messages in the left half of X1, segments 1-3, will fall on the left half of the X4 display. Messages on the right half of X1, segments 1-3, will fall on the right half of the X4 display. The same situation exists with selected segments 5-7, 9-11, or 13-15.

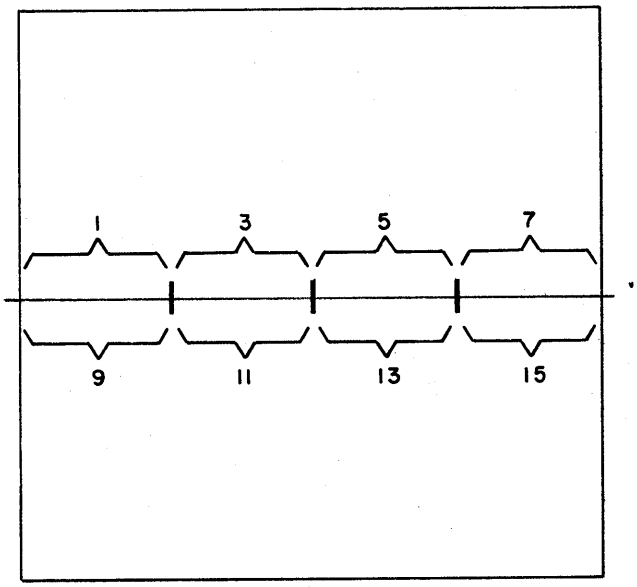


Figure 4–30. Overlapping of Off-Center Areas

The selection of segments 3-5, 7-9, or 11-13, however, requires the sign bit reversal since, in each of these cases, the desired segments would be on the wrong side of the tube (as explained for the 5-11 selection of the X2 expansion). For instance, segment 3 falls on the right side of the tube as part of the display of segments 1-3. When segments 3-5 are to be selected, however, segment 3 must be on the left half of the tube.

2.6.6 Digit 0 Selection, X8 Expansion

In an X8 expansion, relays F and G are operated so that digit 0 must come from the circuitry associated with the L3 positioning bit through normally open contacts of X-1 and Gx-1. Table 4–5 lists the segments which can be selected (in this case, any of the basic 15) and the relays which must operate. Since only D relay contacts of the off-centering relays are involved in the selection of the digit 0 bit, a quick generalization can be made. When the relay is not operated, the 0 side of the L3 bit is selected by the normally open contact of Dx-5. This is in agreement with what has been discussed previously since the D relay is operated only when selecting segments 2, 4, 6, 8, 10, 12, and 14. These are the segments that make up half of each adjoining segment, as shown in figure 4–25. The areas capable of being displayed simultaneously consist of segments 1, 3, 5, 7, 9, 11, 13, and 15. To select segment 2, for example, requires the right half of segment 1 and the left half of segment 3, both of which must be reversed to achieve a correctly oriented display of segment 2.

2.6.7 Intensification Selection

The process of producing an expanded display in the SD console involves the selection of 10 positioning bits for all messages received at the console. In addition, only those messages in the selected areas must be intensified, since, regardless of area selection, all messages are presented to the SD CRT circuitry. The remainder of the circuits (fig. 4–29) are used for this purpose.

As explained, to achieve intensification of any message, AND 5 in intensification unit 2 must be conditioned by three gates (fig. 4–21), one of which is the intensify gate. Assuming then that an intensify gate is present, signifying that a message or part of a message is ready for display, it falls to the expansion and off-centering relays to decide whether the message qualifies for display by determining whether it is in the area being viewed. If the message is in the correct area, gates will appear on the two other inputs to AND, signifying that the position of the message in both x and y co-ordinates is satisfactory and the message is intensified. In order to provide these two additional inputs to AND 5, OR circuits 1 and 2 must be conditioned, either by 10V which is fed to both OR's or by AND's 1, 2, 3, and 4, as shown in the illustration. The four bits necessary to condition each of these four AND circuits are selected by the contacts of the expansion and off-centering relays. Only the X-contacts will be discussed since operation of both sets is identical.

2.6.7.1 Intensification of X1 Displays

Reference to figure 4–29 shows that +10V is applied to the normally open contact of Ex-11. The normally closed contact of Ex-11 is connected to −30V. The armature is connected to OR circuits 1 and 2. Therefore, whenever there is an X1 display, relay E will operate, and a conditioning voltage is applied to both the X and Y OR circuits so that all messages will be intensified. This is necessary, of course, since there is no selection of area in the X1 display. When relay E is not operated (X2, X4, and X8 expansions), −30V is applied to both OR circuits.

2.6.7.2 Intensification of X2, X4, and X8 Displays

In order to illuminate messages for an X2 display, either AND 1 or AND 2 must be completely conditioned (for the x co-ordinate) so that OR 1 will condition AND 5 in intensification unit 2.

Each of the four inputs to AND 1 comes from the relay contact circuitry associated with each of the first positioning bits. By analyzing each of the three possible conditions of relay operation in an X2 expansion, it can be seen how conditioning of one of the AND circuits is obtained for messages that fall in the correct areas.

Assume, for instance, that a message having a binary address shown below arrives at the console circuitry.

LS	L1	L2	L3	L4	L5	L6	L7	L8	L9
1	0	1	0	0	0	0	0	0	0

There will be three additional bits (L10-L12) in the address, but they will not be discussed, as yet, since they do not play a part in the deflection or intensification.

Consider first where this message would occur on the X1 display. Since the sign bit (LS) is a 1, the message must appear on the left-hand side of the SD CRT. The L1 bit is a 0 and, hence, does not produce deflection to the right. The L2 bit is a 1 and, as the third most significant bit, is weighted in the binary decoder to produce deflection across $\frac{1}{8}$ of the tube face. The message is thus positioned $\frac{1}{4}$ of the way across the left half of the tube on the x axis. This is point D of figure 4–22.

If this message is to be seen on an X2 expanded display, segments 1-7 must be selected. Relays C and D are operated to obtain this off-centering selection, and, therefore, the 1 side of the L1 bit will go out as the digit 0 bit to the binary decoder.

Line 1 to AND 1 is connected to the 1 side of the LS bit through the normally closed Ax-1 contact. Since the LS bit is a 1, this line will be up; that is, at +10V. (Note that, although a different set of 10 bits is used for each expansion level, the unused and more significant bits are not discarded; they are still used for intensification purposes.) Line 2 of AND 1 is connected to the L1 circuitry and goes to the 0 side since relay B is not operated. Since L1 is a 0, this line will contain a 1, and, hence, line 2 will also be up. Line 3 of AND 1 goes to both the circuitry associated with the L2 bit and to a source of +10V through the normally closed contact of Gx-11; hence, this line is also up. Similarly, line 4 not only goes to the circuits of L3 but also goes to +10V through the normally closed contact of Fx-11. Thus, all four lines are up and AND 1 is conditioned, thus conditioning OR 1 and AND 5 and allowing display of the message.

Tables 4–6, 4–7, and 4–8 summarize the conditions under which each of the lines going to AND circuits 1 and 2 is energized. Each table covers a different expansion level. Reference to table 4–6 reveals all the conditions which must be met by the positioning bits of an incoming message in order for the message to be intensified on the SD CRT during an X2 expansion. For instance, if segments 1-7 are being observed (having been selected by the OFF-CENTERING buttons or the plugboard patching), there are two combinations of the LS and L1 bits that will produce intensification of the message. If both bits are 1, AND 2 will be energized. This follows from the fact that a 1 bit for LS selects the left half of the X1 display and a 1 bit for L1 selects the right half of the left half, or the second quarter of the axis which corresponds to the 5-7 segments, and which, therefore, merits display. If the LS bit is 1 and the L1 bit is 0, the message will appear to the left of the tube, an area that corresponds to segments 1-3 of an X1 display.

If L1 is 0, intensification will still be achieved (through AND 1), because, once the LS bit has selected the left half of the X1 display, either condition of the L1 bit will still result in message-positioning in the area covered by the 1-7 segments.

Notice that table 4–6 lists bit combinations for the 5-11 column that are duplicated in the other two columns. This follows from the fact that the areas covered by the different groups of segments overlap and

TABLE 4–6. CONDITIONS FOR INTENSIFICATION, X2 EXPANSION

	1–7	5–11	9–15
AND 1			
Line 1	LS=1	LS=1	LS=0
Line 2	L1=0	L1=1	L1=0
Line 3	+10v	+10v	+10v
Line 4	+10v	+10v	+10v
AND 2			
Line 1	LS=1	LS=0	LS=0
Line 2	L1=1	L1=0	L1=1
Line 3	+10v	+10v	+10v
Line 4	+10v	+10v	+10v

TABLE 4–7. CONDITIONS FOR INTENSIFICATION, X4 EXPANSION

	1–3	3–5	5–7	7–9	9–11	11–13	13–15
AND 1							
Line 1	LS=1	LS=1	LS=1	LS=1	LS=0	LS=0	LS=0
Line 2	L1=0	L1=0	L1=1	L1=1	L1=0	L1=0	L1=1
Line 3	L2=0	L2=1	L2=0	L2=1	L2=0	L2=1	L2=0
Line 4	+10v	+10v	+10v	+10v	+10v	+10v	+10v
AND 2							
Line 1	LS=1	LS=1	LS=1	LS=0	LS=0	LS=0	LS=0
Line 2	L1=0	L1=2	L1=1	L1=0	L1=0	L1=1	L1=1
Line 3	L2=1	L2=0	L2=1	L2=0	L2=1	L2=0	L2=1
Line 4	+10v	+10v	+10v	+10v	+10v	+10v	+10v

TABLE 4–8. CONDITIONS FOR INTENSIFICATION, X8 EXPANSION

AND 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Line 1	LS=1	LS=1	LS=1	LS=1	LS=1	LS=1	LS=1	LS=1	LS=0	LS=0	LS=0	LS=0	LS=0	LS=0	LS=0
Line 2	L1=0	L1=0	L1=0	L1=0	L1=1	L1=1	L1=1	L1=1	L1=0	L1=0	L1=0	L1=0	L1=1	L1=1	L1=1
Line 3	L2=0	L2=0	L2=1	L2=1	L2=0	L2=0	L2=1	L2=1	L2=0	L2=0	L2=1	L2=1	L2=0	L2=0	L2=1
Line 4	L3=0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

AND 2

Line 1	LS=1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Line 2	L1=0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Line 3	L2=0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
Line 4	L3=1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

that a message occurring in the overlapping areas will be intensified if either of the two groups of segments has been selected for expanded viewing.

In a like manner, tables 4–7 and 4–8 list all the conditions that must be met for message intensification in the X4 and X8 levels of expansion.

2.7 SD CONSOLE SUBPANEL CONTROLS

Figure 4–31 shows an SD indicator subpanel and the adjustment controls located on it. Those which are used in the SDIS are colored green and are indicated on the illustration by shading. Those which are used for the light gun and which are part of the audible alarm are colored black and are indicated by pairs of diagonal lines. The DD controls are red (diagonal dashed lines on the illustration) and are discussed in Part 3, Chapter 2. The camera control section is shown drawn to the left of the DDIS controls. Situation display consoles that have cameras attached do not contain a DDIS; this section replaces the DDIS controls.

2.7.1 Situation Display Controls

The following SD controls are on the subpanel of the console. They are listed from left to right and from top to bottom:

a. SD TEST PATTERN. This 3-position switch allows normal console operation in the NORMAL position. When in either TEST position, only

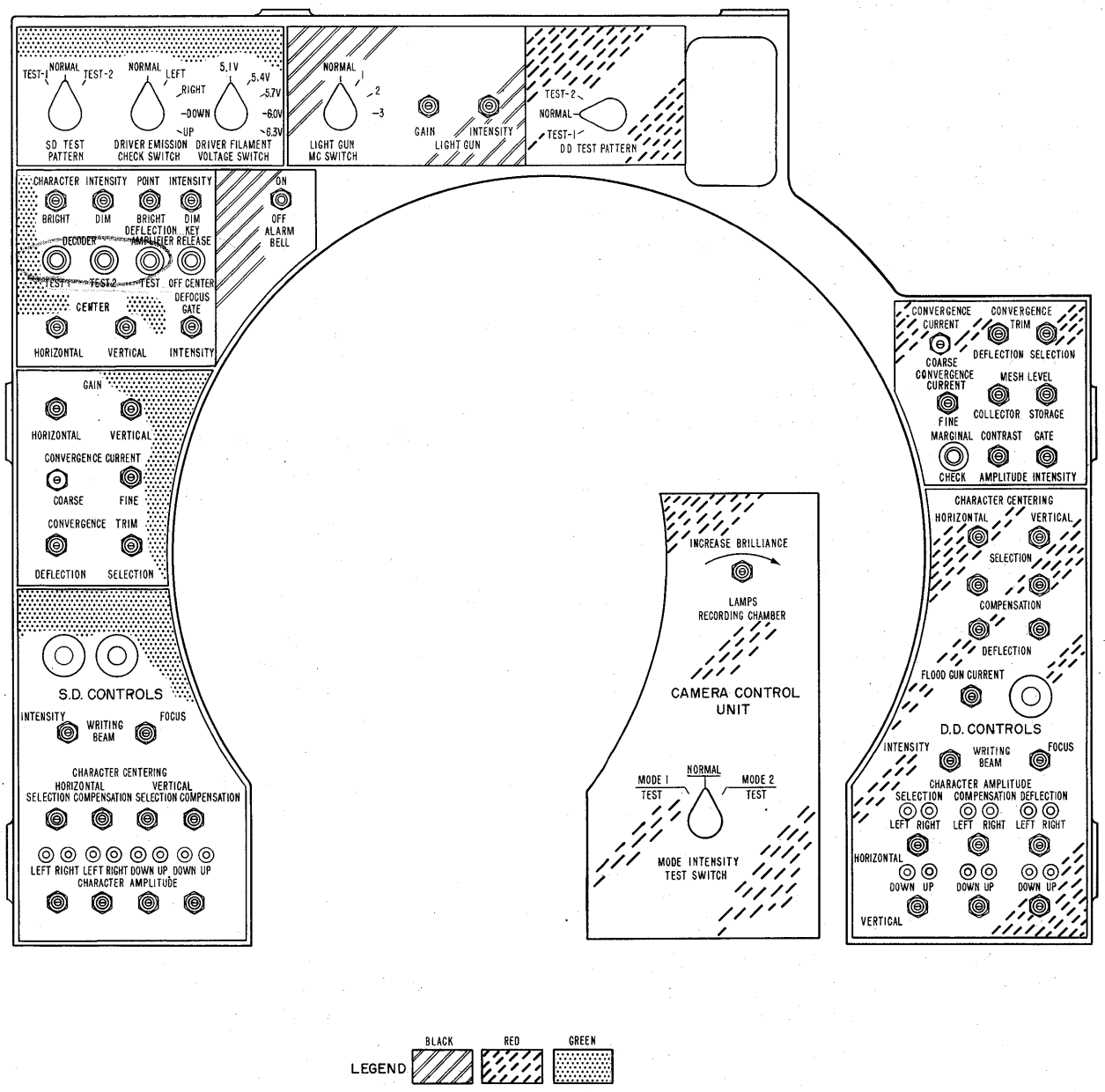


Figure 4–31. Situation Display Console Subpanel

the test category is displayed while all other categories are disconnected. In addition, the times 1 expansion is selected for display. When in TEST 1 position, the feature selection switches in group 1 are operative; when in TEST 2 position, the feature selection switches in group 2 are operative.

b. DRIVER EMISSION CHECK-SWITCH. This 5-position rotary switch allows checking of the operation of the driver unit. In NORMAL position, the driver unit operates normally. In any of the other four positions (LEFT, RIGHT, DOWN, UP), only one of the four driver tubes is allowed to operate.

c. DRIVER FILAMENT VOLTAGE-SWITCH. This switch reduces the filament voltage applied to all four driver unit tubes, allowing a stringent test for low-emission tubes.

d. BRIGHT and DIM CHARACTER INTENSITY. These controls vary the intensity of bright characters and dim characters, respectively.

e. BRIGHT and DIM POINT INTENSITY. These controls adjust the intensification levels for bright and dim points, respectively.

f. DECODER TEST 1 and TEST 2. These switches are used in marginal checking of the 10-bit decoders.

g. DEFLECTION AMPLIFIER TEST. This switch provides a means for marginal checking the deflection amplifier.

h. OFF CENTER KEY RELEASE. If the off-centering keys on the front panel are all accidentally depressed, this switch will energize a solenoid which will release them.

i. HORIZONTAL-VERTICAL CENTERING. These controls adjust the horizontal and vertical centering of the yoke deflection system.

j. DEFOCUS GATE INTENSITY. This control adjusts the evenness of illumination of bright characters during adjustments using a test pattern.

k. HORIZONTAL-VERTICAL GAIN. These controls vary the width and height of the display area on the SD CRT to fit within the inscribed square on the face of the tube by varying the gain of the deflection amplifier unit.

l. COARSE-FINE CONVERGENCE CURRENT. These controls are adjusted for sharpest character registration as viewed on the SD CRT.

m. CONVERGENCE DEFLECTION AND TRIM SELECTION. These controls provide fine adjustments for character registration and character format. They are used in conjunction with the CHARACTER COMPENSATION and SELECTION controls respectively.

n. WRITING BEAM INTENSITY. This control adjusts the overall brightness of the SD display.

o. WRITING BEAM FOCUS. This control adjusts the size of a point display. The adjustment is made by reducing a bright point to optimum size.

p. HORIZONTAL and VERTICAL CHARACTER COMPENSATION CENTERING. These controls adjust horizontal and vertical character registration. They are adjusted while viewing a test pattern to reduce the variation in position of different characters displayed sequentially in the same location.

q. HORIZONTAL and VERTICAL CHARACTER SELECTION CENTERING. These controls adjust for proper selection of columns and rows of characters on the character-forming matrix so that the defocused writing beam is centered on the selected character aperture.

r. HORIZONTAL and VERTICAL CHARACTER COMPENSATION AMPLITUDE. These controls help adjust for the best format registration of characters. They control the amplitude of correction signals applied to compensate for the beam deflection introduced by character selection.

s. HORIZONTAL and VERTICAL CHARACTER SELECTION AMPLITUDE. These controls also adjust the best format registration of characters by controlling the amplitude of the character selection signals applied to the selection plates of the SD CRT.

2.7.2 Light Gun Controls

The following controls on the subpanel of the console are used in conjunction with the light gun:

a. LIGHT GUN MC SWITCH. This 4-position rotary switch allows normal light gun operation when in NORMAL. Position 1 is used for testing the thyratron within the light gun, position 2 is used for testing the light gun amplifier, and position 3 is used when adjusting the LIGHT GUN GAIN.

b. LIGHT GUN GAIN. This control adjusts the level of the input signals to the light gun amplifier.

c. LIGHT GUN INTENSITY. This control varies the intensity of the red light within the light gun proper.

2.7.3 Alarm Bell Control

This control is used to quiet the bell section of the audible alarm for maintenance or similar purposes.

CHAPTER 3

DRUM INPUTS TO SITUATION DISPLAY ELEMENTS

3.1 GENERAL

The AN/FSQ-7 and AN/FSQ-8 utilize the Drum System as a storage buffer device. Information, which is to be used by the Display System, is written on the drums by the Central Computer. The drums, associated with the Display System, continually send data to the situation display elements. The two types of signals needed to generate a display are timing and control signals, and display information signals.

3.2 TIMING AND CONTROL SIGNALS

Three timing and control signals are sent to the situation display elements from the Drum System. The drum timing pulses (OD 1 through OD 4) are sent for timing. Also, just before a TD or RD cycle begins, the Drum System sends a start TD or start RD to put the generator in the correct mode of operation. Before a message is sent, a word-on-way (WOW) signal (OD 4 pulse which occurs 2.5 μsec before OD 1) is sent to SDGE in order to prepare the generator for incoming messages.

3.3 DISPLAY INFORMATION SIGNALS

Signals used to generate the display are read from the drum which has the needed information stored in a certain layout. The drum layout and the message layout for the TD displays are the same. They contain an 8-word layout with 32 bit positions for each word. The bit positions in a word are divided into left half (L) and right half (R). The positions in each half have a sign bit position followed by 15 numbered positions. This gives each word 32 bit positions labeled LS, L1 through L15 and RS, R1 through R15. (See fig. 4–32.)

There are six different classes of information stored in the layout. Part of the layout indicates what kind of message is present. Another part indicates where the message will appear on the face of the CRT. Whether a light gun may be used on the message and whether the message is to be displayed or suppressed is also indicated in the layout. The CAT's and DAB's for a message are also indicated in the layout. Finally, the information needed to generate the display is also stored in the drum layout.

Each of the three TD message types has different layouts because all the messages are different.

Note

Lower-case x and y represent character selection. Upper-case X and Y represent character positioning. Upper-case $\dot{X}$ and $\dot{Y}$ represent vector generating voltages.

3.3.1 TD Tabular Track Message Drum Layout

The drum layout for the TD tabular track message is shown in figure 4–32. Bits LS and RS of word 0 are both 0 to indicate that this layout contains the information needed for a TD tabular track message.

Positioning of the message on the CRT is determined by the X and Y co-ordinates of the central point. For positioning the central point, word 1 bits LS through L12 determine X and RS through R12 determine Y.

The CAT's and DAB's accompanying the message are located in words 2, 3, and 4. The category is located in word 2 bits LS through L4. The display assignment bit is located in word 2 bits L6 through L15 and RS through R15 and all of words 3 and 4.

If added information is necessary along with the SD display, a 0 must be in LS of word 6 so the light gun can be operated. If that condition does not exist, the light gun is inoperative because the point on the SD display is not intensified. Without intensification, there would be insufficient illumination to actuate the photo-electric cell in the light gun.

If L5 of word 2 is a 0, the message sent to the SDGE will be suppressed. However, if it is 1, the message may be displayed.

For the generation of the display, the information within the layout is needed to generate the vector, select the characters, and position the characters in respect to the central point.

The vector is generated from the central point, already established, in a direction and for a distance indicated by $\dot{X}$, $\dot{Y}$ located in word 5 bits LS through L6 and RS through R6, respectively. If the most significant bit (LS) of either $\dot{X}$ or $\dot{Y}$ is a 0, the sign is positive. If the bit is 1, the sign is negative.

Each of the characters in the display is selected by two signals, x and y. Each of these signals is represented by the binary bits. The x used to select the A character is stored in word 0, bits L1 through L3; the y is found in bits R1 through R3. All of the other

characters A through E are stored and selected in a similar manner, as indicated in the layout.

Word 7, bit LS is the format position bit. This bit with the sign of $\dot{X}$ or $\dot{Y}$ determines the positioning of the characters with respect to the central point, as explained in the display message format (refer to 1.3, Part 4, Chapter 1).

3.3.2 TD Tabular Information Message Drum Layout

This message layout is also shown in figure 4–32. In word 0, LS is 1 and RS is 0 to indicate a TD tabular information message.

Message-positioning, CAT and DAB, light-gun, and display-suppress information is the same for the TD tabular track message. Since there is no vector or B character in the TD tabular information message, these portions of the drum layout are left blank.

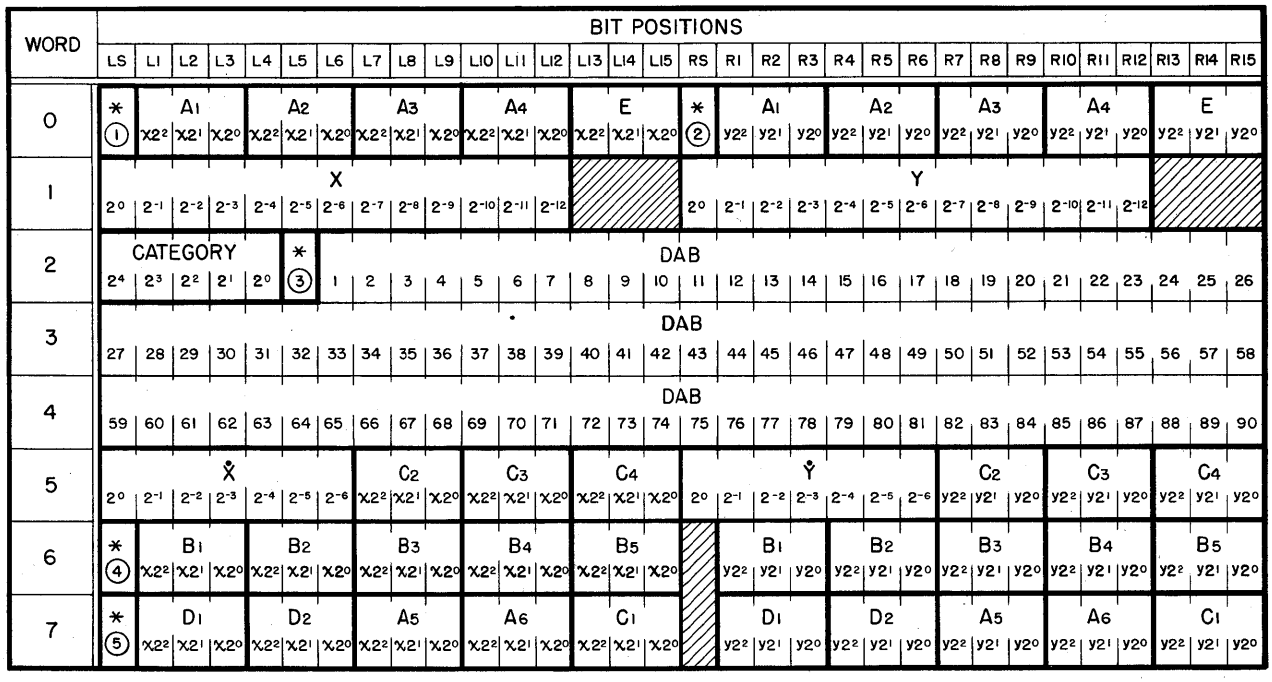
3.3.3 TD Vector Message Drum Layout

The TD vector message drum layout is shown in figure 4–33. A 1, located in bit RS or word 0, indicates that the information located in this layout is a vector message. Central points for the four vectors in this layout are designated by the X's and Y's (LS-L9, RS-R9) with the subscripts 1 through 4 in words 1, 5, 6, and 7. Words 2 through 4 contain all the CAT and DAB information as indicated. Since light guns are never used on a vector message, the control bit is not needed. L5 of word 2 is still applicable, and, if it is a 1, the message may be displayed.

Each vector is generated from the central point established by the X and Y positioning bits. The vector is swept in a direction indicated by the sense and magnitude bits ($\dot{X}$, $\dot{Y}$). The subscripts associate each central point with its magnitude and sense bit for a correct vector generation.

3.3.4 RD Message Drum Layout

An RD message is contained in 24 bits; the RD drum is divided into nine fields of 24-bit registers. The



NOTE:
* INDICATES CONTROL BIT, AS FOLLOWS:

NAME	WORD	POSITION	CONTENT	MEANING
① TRACK/INFO BIT	0	LS	0 1	TD TABULAR TRACK MESSAGE TD TABULAR INFORMATION MESSAGE
② TABULAR/VECTOR BIT	0	RS	0	TD TABULAR MESSAGE (COMPARE WITH TD VECTOR MESSAGE)
③ DISPLAY BIT	2	L5	0 1	SUPPRESS DISPLAY OF MESSAGE DISPLAY MESSAGE
④ LIGHT GUN BIT	6	LS	0 1	PERMIT USE OF LIGHT GUN PROHIBIT USE OF LIGHT GUN
⑤ POSITION BIT	7	LS	0 1	FORMAT LEFT OR RIGHT OF CENTRAL POINT FORMAT ABOVE OR BELOW CENTRAL POINT

Figure 4–32. TD Tabular Message Drum Layout

WORD	BIT POSITIONS																													
	LS	LI	L2	L3	L4	L5	L6	L7	L8	L9	LI0	LI1	LI2	LI3	LI4	LI5	RS	RI	R2	R3	R4	R5	R6	R7	R8	R9	RI0	RI1	RI2	RI3	RI4	RI5
0		G1			G2			G3			G4						*	G1			G2			G3			G4					
		$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$	$x2^2$	$x2^1$	$x2^0$				①	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$	$y2^2$	$y2^1$	$y2^0$			
1		X1									$\dot{X}1$							Y1									$\dot{Y}1$					
		2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}
2		CATEGORY					*	DAB																								
		2^4	2^3	2^2	2^1	2^0	②	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
3		DAB																														
		27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58
4		DAB																														
		59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90
5		X2									$\dot{X}2$							Y2									$\dot{Y}2$					
		2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}
6		X3									$\dot{X}3$							Y3									$\dot{Y}3$					
		2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}
7		X4									$\dot{X}4$							Y4									$\dot{Y}4$					
		2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}

NOTE:
*INDICATES CONTROL BIT, AS FOLLOWS:

NAME	WORD	POSITION	CONTENT	MEANING
① TABULAR/VECTOR BIT	0	RS	1	TD VECTOR MESSAGE (COMPARE WITH TD TABULAR MESSAGE)
② DISPLAY BIT	2	L5	0 1	SUPPRESS MESSAGE DISPLAY MESSAGE

Figure 4–33. TD Vector Message Drum Layout

BIT POSITIONS																						
LS	LI	L2	L3	L4	L5	L6	L7	L8	L9	LI0	LI4	LI5	RS	RI	R2	R3	R4	R5	R6	R7	R8	R9	RI0
X											*	*		Y									
2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	①	②	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

NOTE:
*INDICATES CONTROL BIT, AS FOLLOWS:

NAME	POSITION	CONTENT	MEANING
① SOURCE BIT	L14	0 1	IDENTITY 0 IDENTITY 1
② STATUS BIT	L15	1 0	CORRELATED DATA UNCORRELATED DATA

THESE CONTROL BITS PROVIDE FOUR CLASSIFICATIONS OF RD MESSAGES. FURTHER CLASSIFICATION INTO THE EIGHT RD CATEGORIES IS ACCOMPLISHED BY THE RD-BRIGHT AND RD-DIM SIGNALS.

Figure 4–34. RD Message Drum Layout

24 bits of an RD message are laid out in a register as shown in figure 4–34. The first 11 bits contain the message's X co-ordinates. The next bit is the source bit. If it is a 1, the source is identity-1 type radar; if it is a 0, the source is the identity-0 type radar. The status bit follows the source bit, and contains a 1 if the message is correlated, or a 0 if the message is uncorrelated with the other radar data. The final 11 bits contain the Y co-ordinate. Those radar returns coincident with the radar scans are displayed brightly in illumination. Previous radar scans are dimly displayed. These signals are controlled by the intensification signal sent by the Drum System from the field containing the message. The intensification signal, in turn, is determined by the position of that field with respect to the field being written on by the Central Computer System.

Empty registers containing no X, Y bits correspond to a message with 0, 0 co-ordinates. If the CRT were intensified for empty registers, the center phosphors of the viewing screen would burn out. To prevent this, should the X co-ordinate of any message be 0, the message would not be displayed.

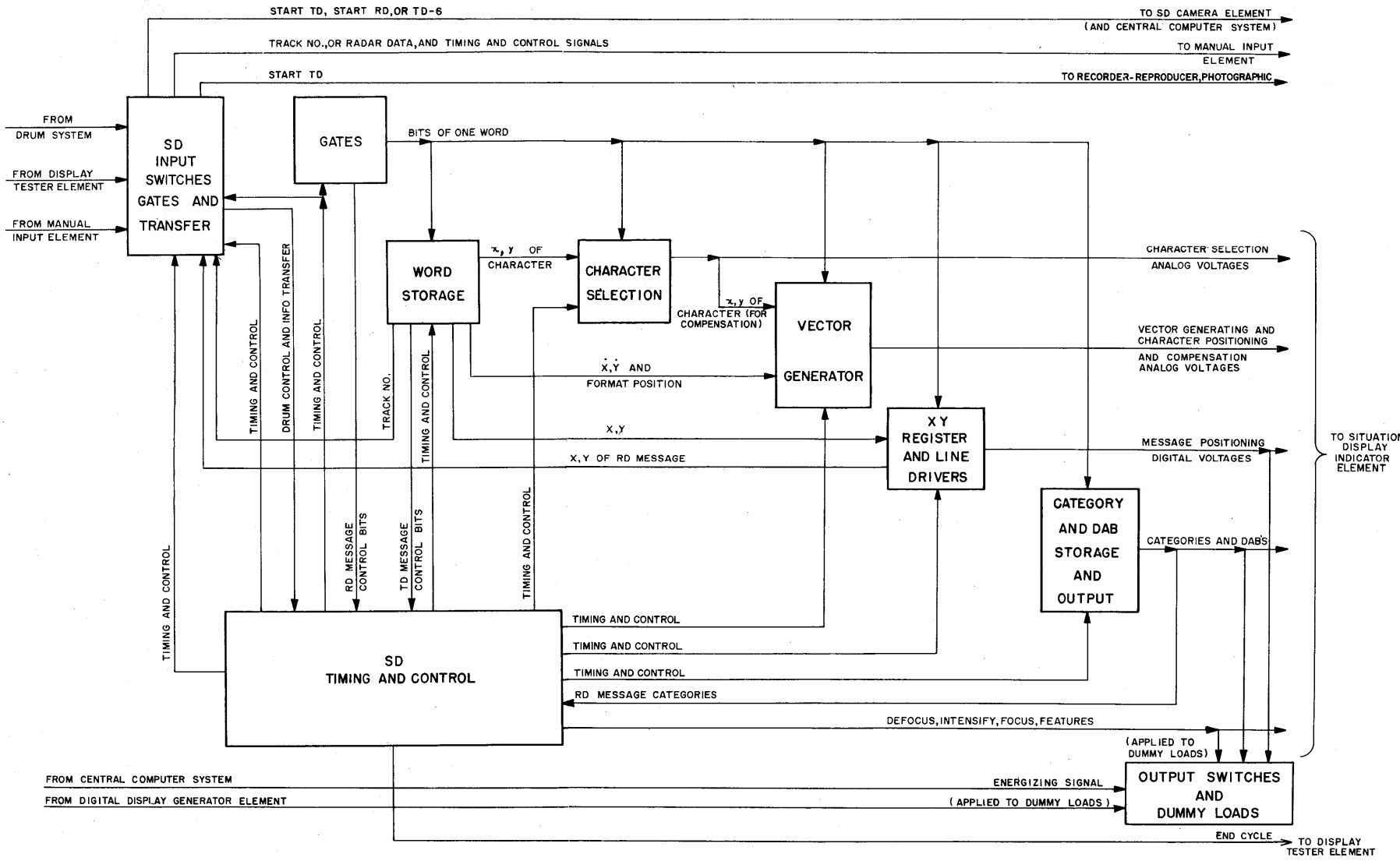


Figure 4–36. Situation Display Generator Element, Simplified Flow Diagram

CHAPTER 4
SITUATION DISPLAY GENERATOR ELEMENT

SECTION 1
SCOPE

1.1 OBJECTIVE

The SDGE contains the necessary circuits to accept messages from the Drum System or during required tests from the DTE and present these messages for personnel observation on the SDIE. The SDGE presents the messages on the SDIE's by routing timing and control signals which originated in the system. The messages contain information which has to be routed to separate sections so proper sequencing can take place. The SDGE also supplies the target co-ordinates for light gun and area discriminator inquiries directed to the Central Computer.

1.2 INPUTS TO THE SDGE

The major inputs to the SDGE are from the Drum System. These are the information and control signals from the drum and the timing and control signals from the drum control circuits. In addition to inputs from the Drum System, the SDGE receives inputs to a minor degree from the MI element, the duplex maintenance console of the Central Computer System, and the DTE during test.

1.2.1 Information and Control Signals from the Drum

The messages, which are to be presented by the SDGE, are stored on the drum as 1 or 0 bits. The number of bits, which make up a register, are different for TD and RD messages. Track data messages are stored on six fields of the TD drum. Each TD message is stored on eight consecutive 32-bit drum registers. Each register is referred to as a word of the message. A group of eight registers that contains a TD message is referred to as a slot. On a drum field there are 2,048 registers or 256 slots, and since there are six fields (256 x 6), 1,536 slots or possible messages can be stored on the TD drum. In the RD message there is one word per 24-bit drum register. Each field contains 2,048 registers, and eight fields out of nine are read (because the Central Computer is writing on the ninth field). The total number of messages available on the RD drum is 16,384.

1.2.2 Drum Message Arrangement

The Central Computer writes on the drum in consecutive registers and arranges the messages on the drum so that each message can be read out, for the slower access time of the Display System. Figure 4–35, foldout, is a functional block diagram of the SDGE.

1.3 OUTPUTS FROM THE SDGE

The major outputs from the SDGE are sent to the SDIE. The outputs are routed through the signal distribution boxes to the SDIS's. Message-positioning (XL, YR), vector-generating, character-compensation and character-positioning (SD $\pm$X, Y), and character-selection (SD x, y) signals are sent to the SDIS display circuits. These signals, with the exception of the XL, YR signals, are sent in analog form. The XL, YR signals are sent as digital voltages to the deflection circuits of the SDIS's. The CAT and DAB signals are sent to certain SDIS's for selection of particular messages.

Besides the major outputs to the SDIE, signals are sent to the MI element and, during test, to the DTE. The track number of a tabular track message and the X and Y co-ordinates of a radar message (for transfer to the Central Computer) are sent to the MI element. Control signals accompany the transferred information. During test operation, the timing and control section of the SDGE sends end-cycle pulses to the DTE. A start-TD signal from the SDGE is sent to the PRRE to synchronize its operation with the TD cycle, and to the SDCE to synchronize camera operation with the SD display cycle. Refer to Chapter 2 of Part 5 for a detailed discussion of the PRR and to Chapter 4 of Part 5 for a discussion of the SDCE.

1.4 SDGE FUNCTIONAL OPERATION

The SDGE is divided into functional blocks, as shown in figure 4–36, that operate to present the display. The signals, which are developed in these blocks, are sent to the SD CRT's for display of the SD message. The sections are described briefly below.

1.4.1 SD Input Switch Section

The function of the SD input switch section, during normal operation, is to provide input paths from

the Drum System to various sections of the SDGE and input and output paths of information to the MI element. The SD input switch relays, which are energized during test, are controlled by the duplex maintenance console. During test, input paths are provided from the DTE instead of the drums. Also, the input and output paths to the MI element are opened. A block diagram is shown in figure 4–37.

The information-transfer signal from the MI element is interrupted when the SD input switch relays are in test. The 24 information lines, which route information from the SDGE to the MI element, are also prohibited.

1.4.2 Input Gates and Word Storage Section

All information drum bits pass to the input gates section from the input switch section. These gates are conditioned by a 2.5-μsec level, originated in the SDGE by the WOW pulse, which allows the message to be received by the SDGE. Since the WOW pulse originated the 2.5-μsec gate, each message must contain a WOW pulse 2.5-μsec prior to the admittance of a message from the drum. Specifically, each of the eight registers of a tabular message must be preceded by a WOW pulse. Each radar message (each register constituting a message) is also preceded by a WOW pulse.

The input gate section performs an additional function in preventing spurious drum noise signals from actuating the SDGE. Figure 4–38 is a functional block diagram of the input gates, showing inputs and outputs.

Information is read from the drum faster than it can be displayed. Storage circuits are provided to hold information from words 0, 5, 6, and 7 that cannot be applied directly to control circuits or registers. Information from all words is applied to each storage circuit but must be gated into the appropriate circuits by read-word signals from the SD timing and control section. The word storage section also generates signals corresponding to the control bits contained in the stored words for use as control signals in the SDGE. A functional block diagram of the word storage section is shown in figure 4–39.

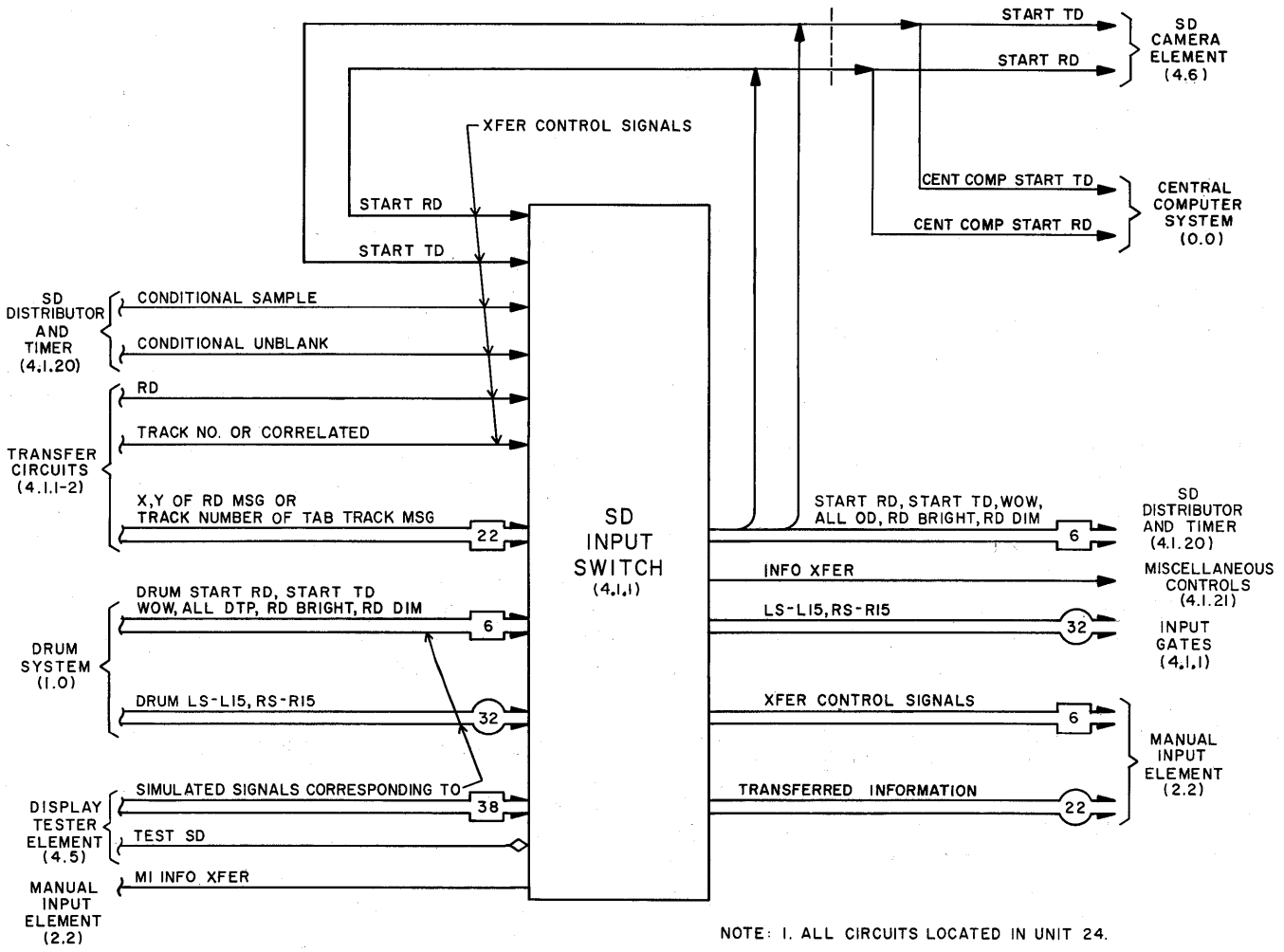


Figure 4–37. Situation Display Input Switch Section, Functional Block Diagram

1.4.3 Character Selection Section

The character selection section generates analog voltages which are used by the SDIE to select the characters required for the message. A block diagram of the SD character selection section is shown in figure 4–40.

For TD messages, the voltages are obtained by decoding the character selection address bits in the messages. The point character (produced by focusing the CRT beam and passing it through the vector aperture in the character-forming matrix) is required for the display of the vectors in a TD vector message, and the point and vector in a TD tubular track message. The character selection circuit is used to select the point character by application of the set-point signal from the SD timing and control section. The RD category of an RD message is decoded in other sections of the SDGE and sets up the character register section to select the character required for the message display. In any message, the digital character selection signals are not gated into the register selection section until the character is scheduled for display. Gating into the character register is controlled by transfer signals generated in the SD timing and control section. Storage for the signals of TD messages is provided by the word storage section. Signals for the E characters are an exception. They are gated directly into the character register from the input gates by a read-word-0 signal from the SD timing and control section. (Since the E character is the first part of a TD tabular message to be displayed, its character selection bits are gated into the character register without previous storage.)

The digital voltages which generate the character selection voltages are also applied to the vector and character positioning section. They are used as character compensation voltages in order to compensate for beam deflection created by the character selection voltages. These voltages are combined with the character positioning voltages at the same time the signals are being set up for positioning the characters.

1.4.4 Character Compensation and Positioning, and Vector Generation

The SD CRT contains a set of character compensation and positioning and vector generating plates. The voltages that perform these three functions must be combined with the SDGE, since only one set of analog voltages is applied to the SDIE at one time. Figure 4–41 is a diagram of the character positioning and vector generation section.

Digital voltages are decoded in the character selection section to select the characters by deflecting the beam off its axis. The same digital voltages are used to compensate for the deflection of the beam. They are applied to the character position decoders. Character compensation is identical for TD vector, TD tabular, and RD messages.

To produce a vector, the electron beam is first focused and passed through the vector aperture in the character-forming matrix (by the selection plates). Then the pinpoint beam on the viewing screen is swept (by the voltages impressed on the compensation plates) in

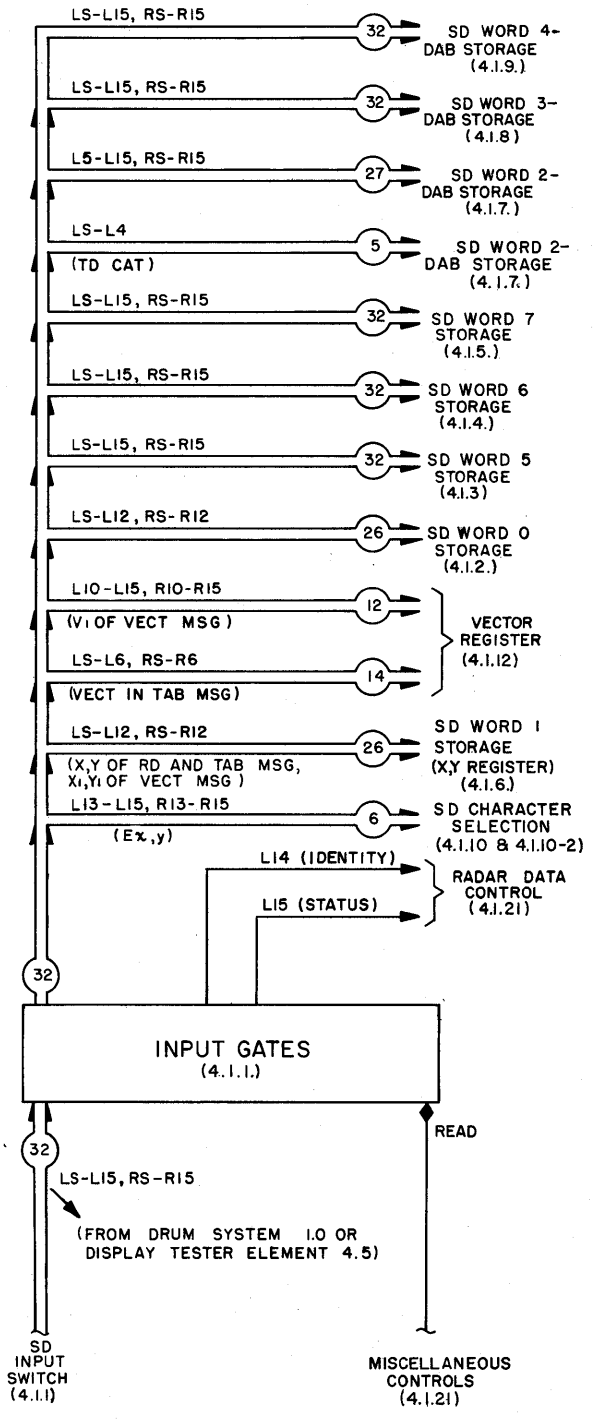


Figure 4–38. Input Gates Section, Functional Block Diagram

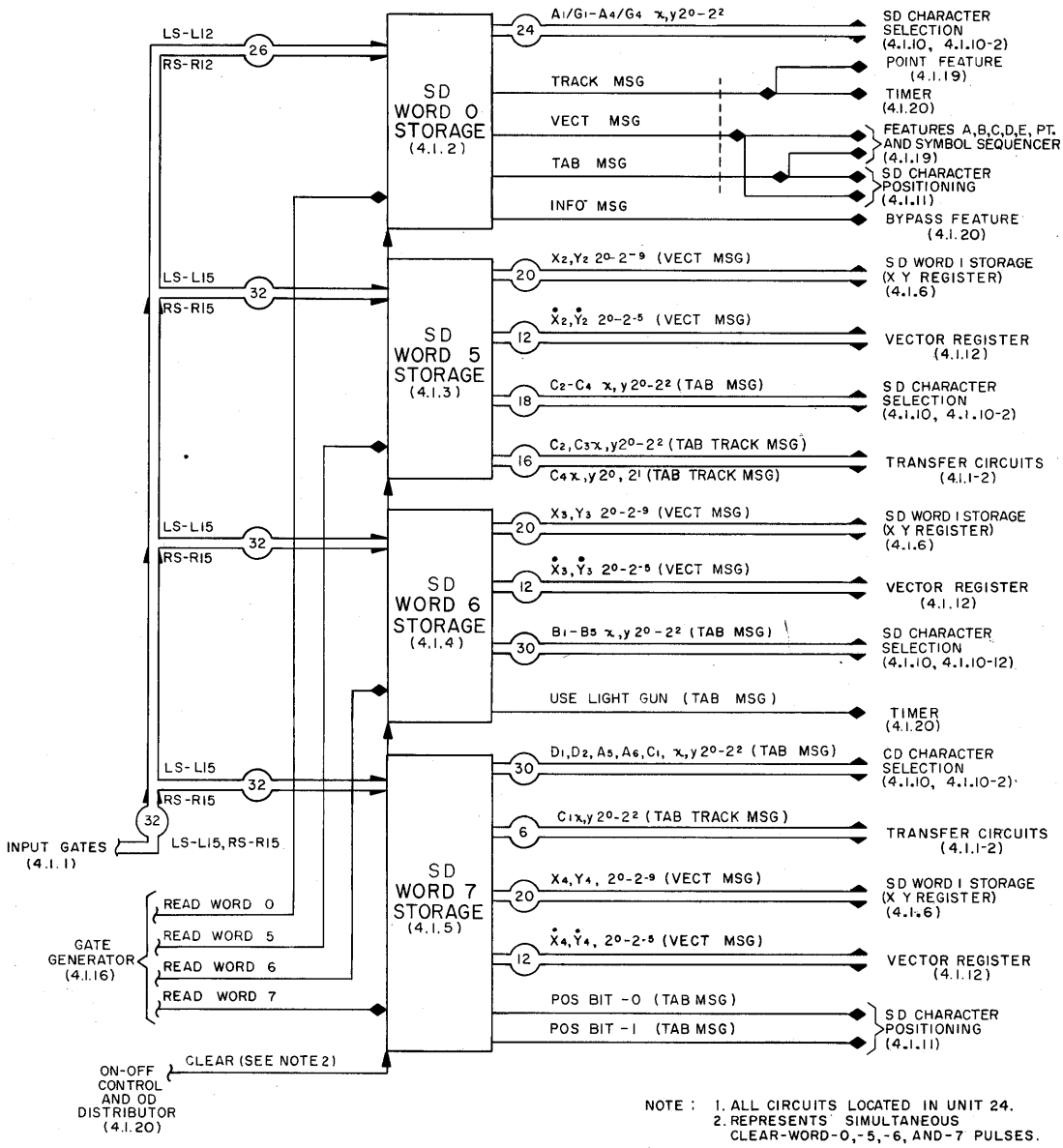


Figure 4–39. Situation Display Word 0, 5, 6, and 7 Storage Section, Functional Block Diagram

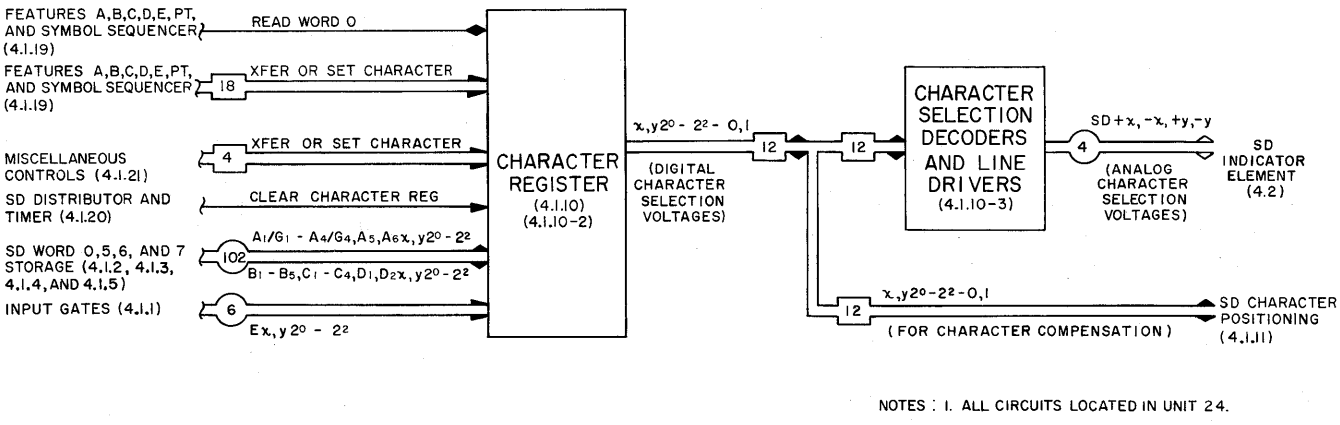


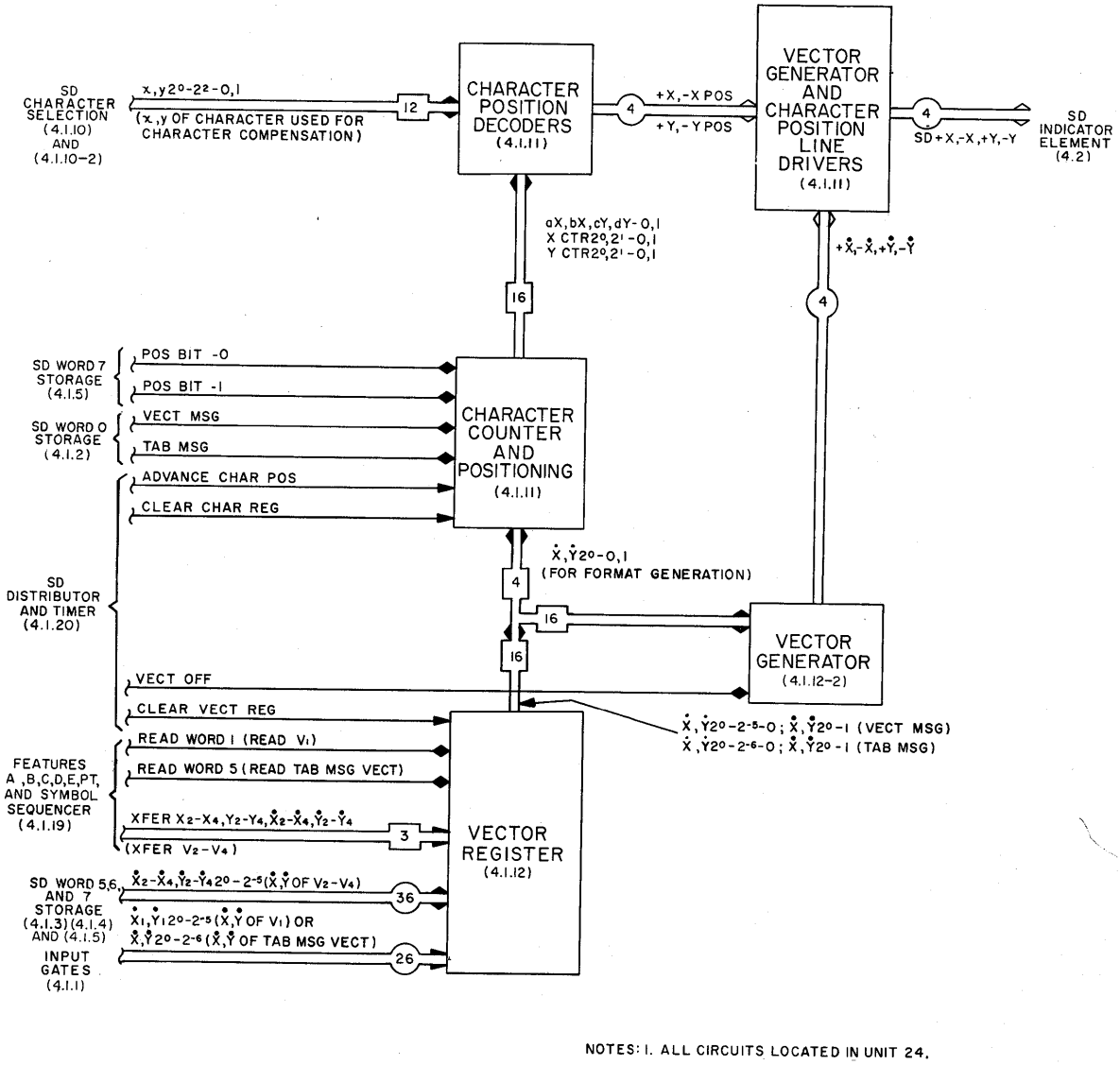
Figure 4–40. Situation Display Character Selection Section, Functional Block Diagram

the direction determined by the sense and magnitude bits of the vector contained in the message. These bits ($\dot{X}$ and $\dot{Y}$) are decoded in the vector generation section. The $\dot{X}$ and $\dot{Y}$ bits are stored in the word storage section and are transferred to the vector generation section at the time the vector is to be displayed. (The $\dot{X}$ and $\dot{Y}$ bits of the TD tabular message vector and the first vector in a TD vector message are exceptions. They are applied to the vector register without prior storage.) The transfer signals are generated in the SD timing and control section.

1.4.5 Message Positioning (XY Register and Drivers Section)

Message positioning on the viewing screen of the SD CRT is controlled by the positioning bits. Positioning bits are contained in each message to determine the location of the message on the SD CRT. (Each vector of a TD vector message is positioned independently.) The positioning bits generate digital voltages which are decoded in the SDIE to provide analog voltages for the deflection coil to position the message on each SD CRT.

The digital voltages, which correspond to the positioning bits in a message, are generated in the SD word-1 XY register storage and drivers section. The bits in word-1 storage are gated through the input gates section. Figure 4–42 is a diagram of the SD word-1 XY register storage and X and Y line drivers section. Vectors $V_2 - V_4$ of a TD vector message are not displayed at the start of the message because their positioning bits are stored in the word storage section until needed.



NOTES: 1. ALL CIRCUITS LOCATED IN UNIT 24.

Figure 4–41. Situation Display Character Positioning Section and Vector Generation Section, Functional Block Diagram

Each RD message contains 11 message positioning bits for each co-ordinate. These bits are applied through the input gates section to the XY register and drivers section. A path to the SD timing and control section is provided for each 1-bit of the X co-ordinate. If all 11 signals are absent, the display is suppressed.

1.4.6 Category and DAB Storage and Output Section

Every message falls into one of 40 (32 TD and 8 RD) SD categories. The message category received by the SDGE from the drum is in five bits (LS-L4 of word 2). The SDGE generates a level corresponding to the category bits of the message and routes the message to the assigned consoles. The mix-all-DAB's level, which enables the display of all DAB's at a single console, is used for monitoring or maintenance purposes. If a category level corresponding to a selected category is received with the message, the message can be selected for display. Also DAB's determine whether a message can be displayed on a specific console. The DAB for each message, contained in the message layout, is used to determine on what console the message may be displayed. Not every console needs a DAB to display the message because the category bits may also enable a console to intensify the message. The DAB's of certain messages are sent to CAT and DAB switches on the front of the SD console to enable the operator to have control of the messages, while other DAB's bypass the switches to force the message to be displayed on certain SD CRT's.

Mixed category and mixed DAB signals are also provided. A mixed category signal permits two or more message categories to be chosen by a single switch on the console. A mixed DAB signal forces the display on a single console of messages normally assigned to two or more consoles. This may be done for monitoring purposes. Figure 4–43 is a diagram of the CAT and DAB storage and output section. Table 4–9 shows the various TD CAT signals that are mixed to provide mixed CAT signals (on the supplementary drivers line).

The eight categories used in radar are also mixed to provide mixed radar categories. There are 12 mixed

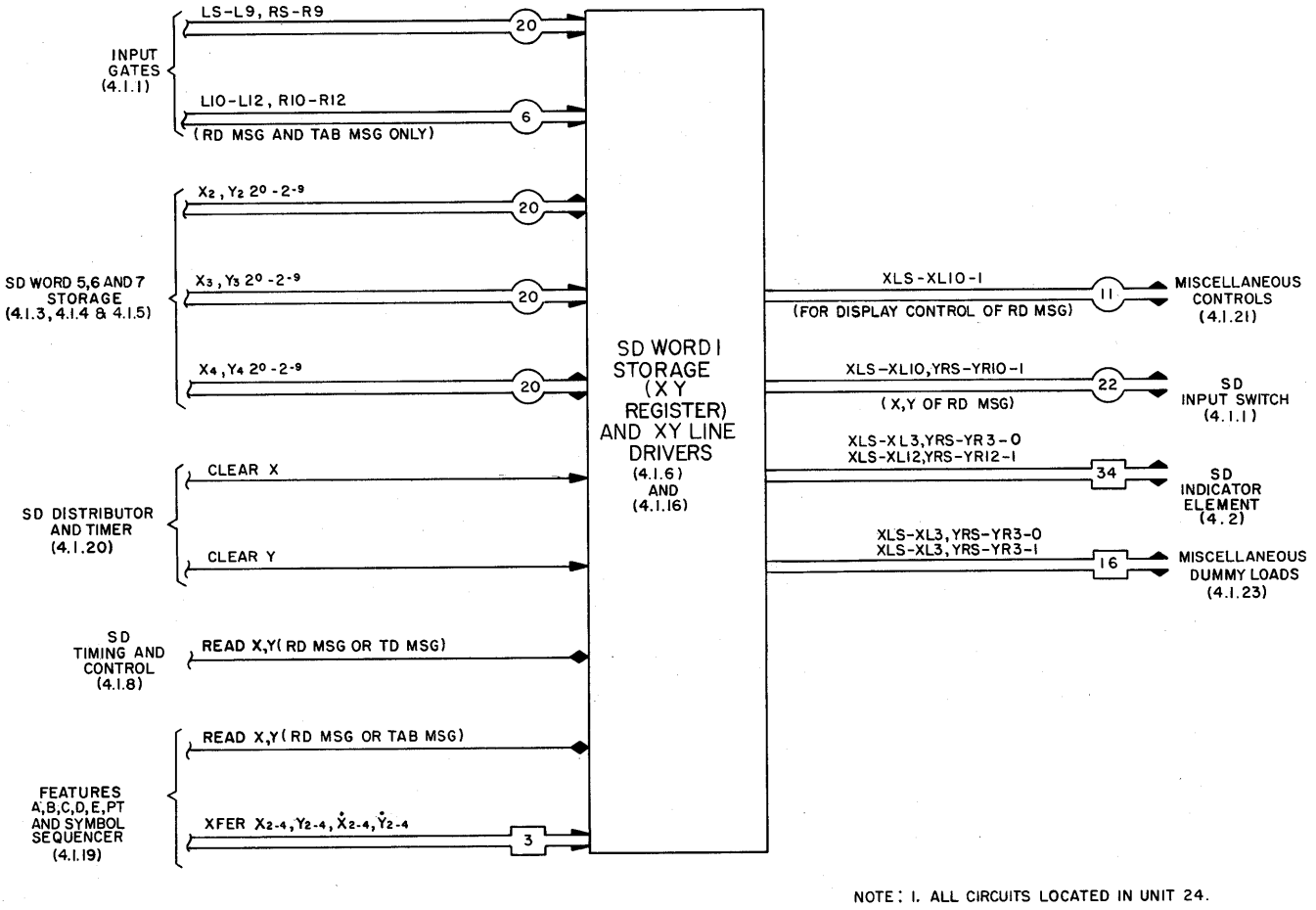


Figure 4–42. Situation Display Word 1 Storage (XY Register) and XY Line Drivers Section, Functional Block Diagram

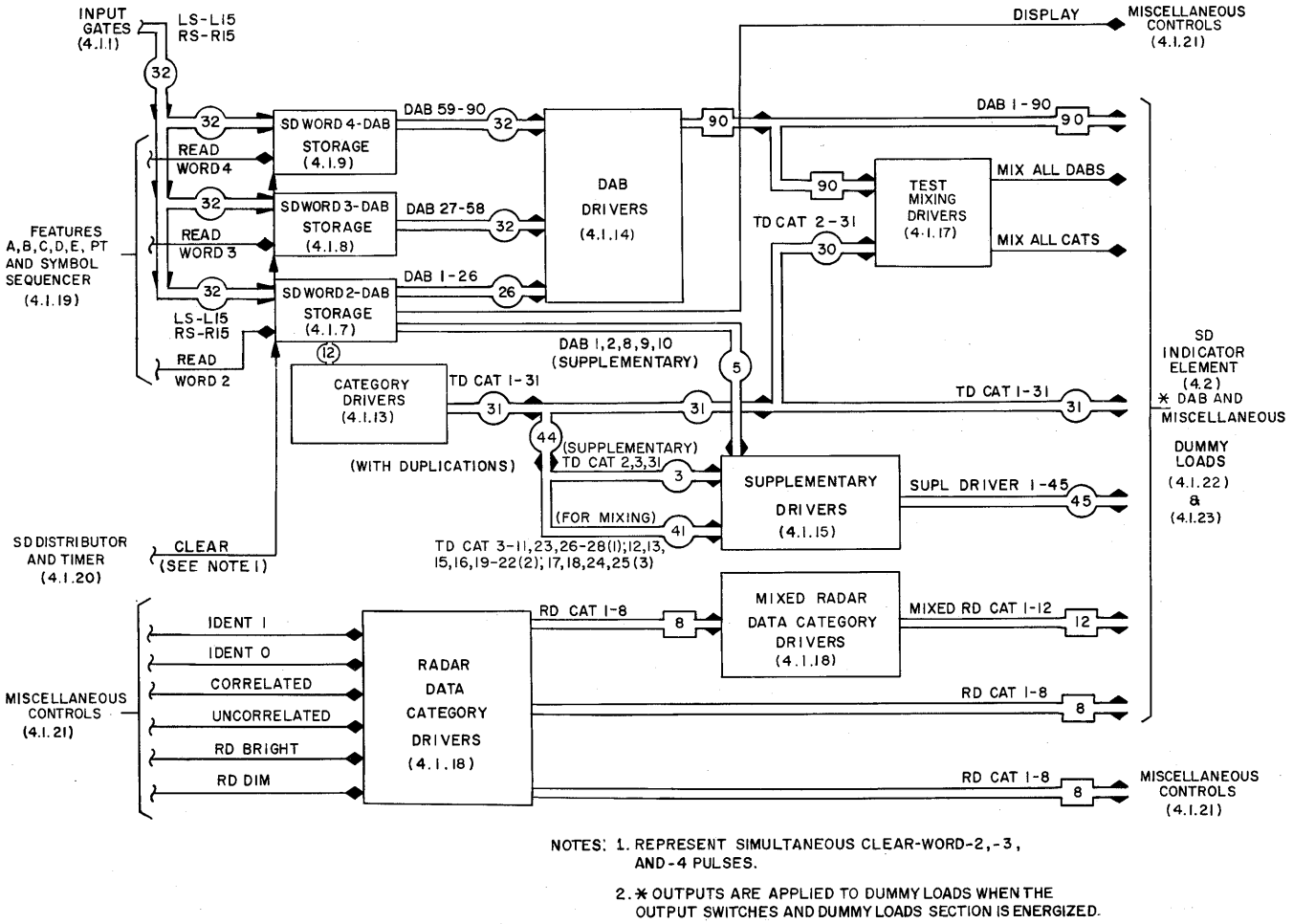


Figure 4–43. Category and DAB Storage and Output Section, Functional Block Diagram

radar categories generated by the eight basic categories being OR'ed. Table 4–10 shows the mixed radar categories.

1.4.7 Transfer Circuits Section

The track number (C1-C4 characters) of a TD tabular track message or the X and Y co-ordinates of a radar message can be transferred to the MI element. The transfer of information can occur only after the SD timing and control section generates a conditional-unblank signal. The conditional-unblank signal is transmitted to the MI element where it initiates a pass-light-gun signal. This signal is transmitted to consoles in the SDIE which have light guns. If a light gun produces an output signal coincident with the pass-light-gun signal, the light gun output is transmitted to the MI element. If a light-gun-output signal has been received by the MI element, the latter sends the SDGE an information-transfer signal. This signal generates a transfer X, Y or transfer-track-number signal in the SD timing and control section. These signals are applied to the transfer circuits section to permit the transfer of the information. A start-RD or start-TD signal (from the Drum System) is also transferred to the MI element. The transferred information is accompanied by identifying signals generated in the transfer circuits section (fig. 4–44).

The XLS-XL10, YRS-YR10 signals, which represent the position of the RD message, are generated in the SD word-1 XY register storage section and X and Y drivers section. These signals are applied to the transfer circuits section and are gated through the section by a transfer X, Y signal. The information is applied to the MI element through the SD input switch section.

1.4.8 Dummy Load Section

The SDGE contains amplifying circuits which amplify many of the outputs before they are applied to the SDIE. It may be desired to operate the SDGE for testing purposes without applying the outputs to the SDIE. To test the SDGE correctly, dummy loads must be provided for the SDGE circuit outputs.

Dummy loads are contained in the dummy loads section as shown in figure 4–45. The SDGE outputs are switched from the SDIE to the dummy loads when

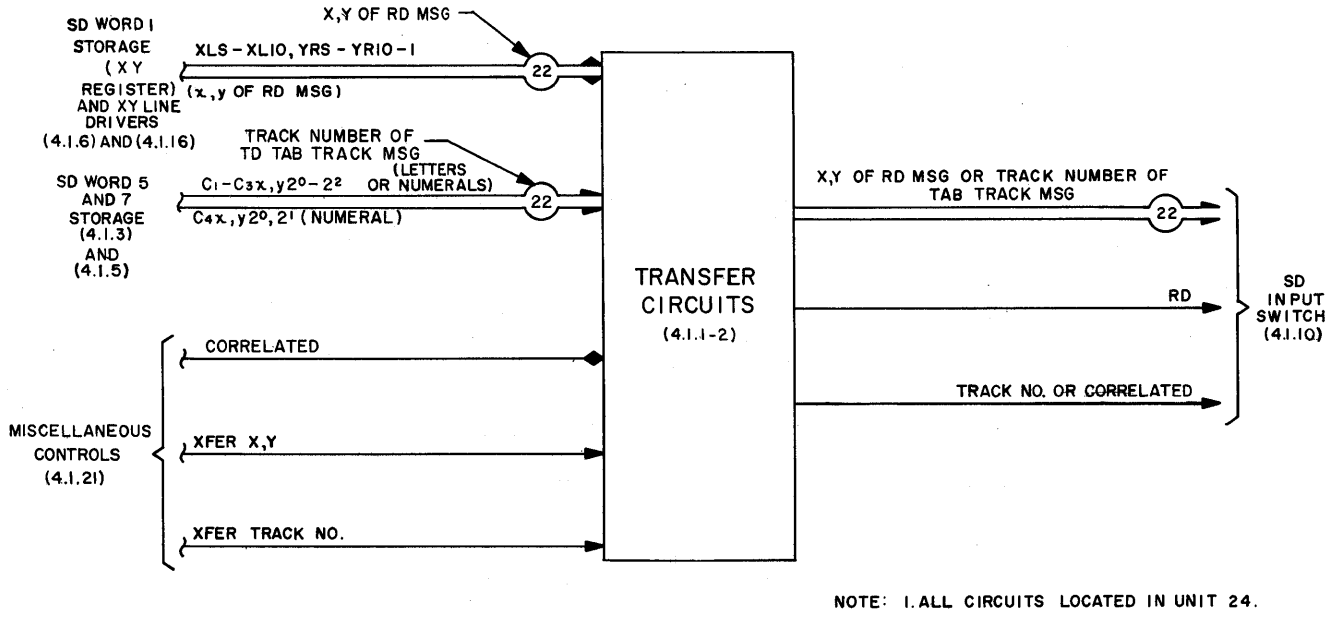


Figure 4–44. Transfer Circuits Section, Functional Block Diagram

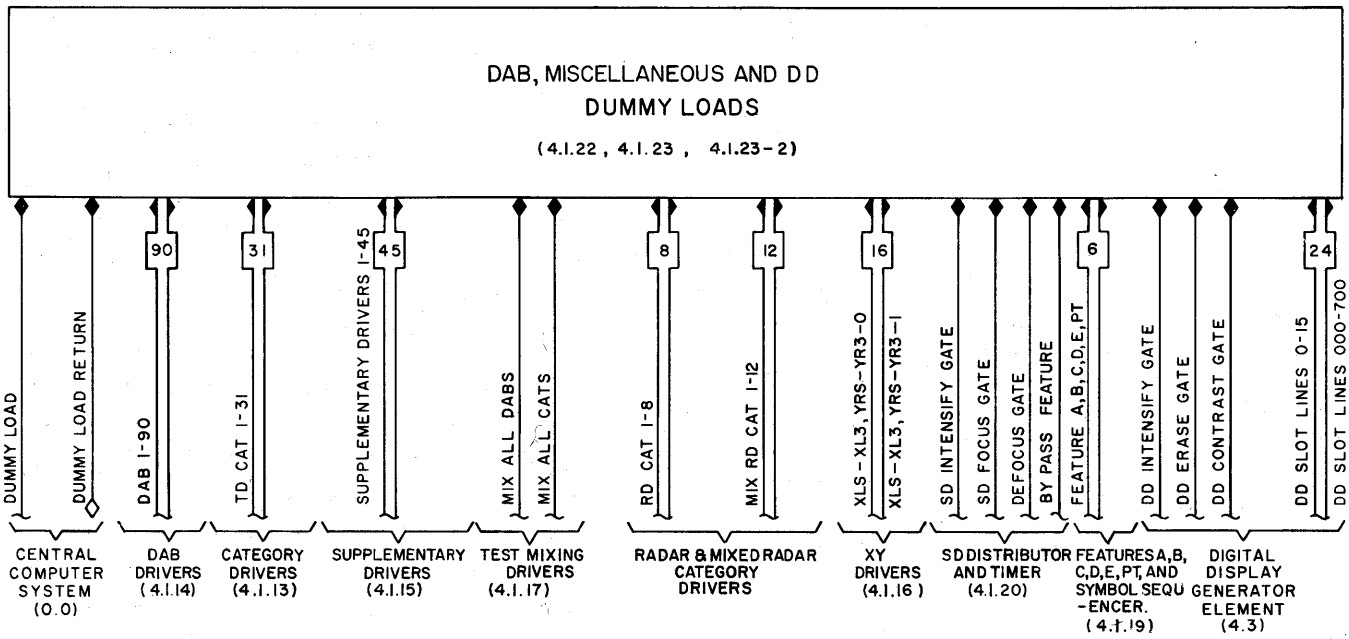


Figure 4–45. DAB Miscellaneous and DD Dummy Loads Section, Functional Block Diagram

the dummy load section is energized by a dummy-load signal from the Central Computer System. All DDGE outputs to the DDIE are also handled by the output switch and dummy load section of the SDGE.

TABLE 4–9. GENERATION OF SUPPLEMENTARY DRIVER SIGNALS, AN/FSQ-7

SUPPLEMENTARY DRIVER	GENERATED BY
1–21	Not used
22	TD CAT's 19, 20, 21, 22
23	TD CAT's 18, 23
24	SUPL DRIVER 22 (TD CAT's 19, 20, 21, 22) TD CAT's 16, 17, 24, 25
25	TD CAT's 19, 21
26	TD CAT's 20, 22
27	TD CAT's 19, 20, 23
28	TD CAT's 16, 18
29	TD CAT's 16, 17
30	TD CAT's 21, 22
31	TD CAT's 24, 25
32	DAB 10 (SUPL)
33	DAB 9 (SUPL)
34	TD CAT's 3, 4, 5
35	TD CAT's 3, 4, 5
36	TD CAT's 9, 10
37	DAB 2 (SUPL)
38	DAB 8 (SUPL)
39	DAB 1 (SUPL)
40	TD CAT's 3, 4
41	TD CAT's 3, 4
42	TD CAT's 12, 13
43	TD CAT 31
44	TD CAT 3
45	TD CAT 2
——	——
——	——

1.4.9 SD Timing and Control Section

The functions of the SD timing and control section fall into four categories:

a. Beam focusing, beam defocusing, and intensification of control signals at the SDIE (these include the feature and bypass feature signals).
b. Transfer control signals to the MI element.
c. An end cycle (control signal) to the DTE.
d. Internal timing and control signals to the other circuits of the SDGE.

Timing and control signals are received from the Drum System through the SD input switch section. Figure 4–46, foldout, is a logical diagram of the SD timing and control section. The applications made of the timing and control signals depend on the type of message being presented for display. This type is determined by the control information contained in the message. (For RD messages, the control information is gated into the timing and control section without storage.) In the case of TD vector and tabular messages, the control bits are applied through the word storage section. Signal voltages corresponding to the control bits are generated in the word storage section.

The SD CRT is adjusted upon installation to provide a pinpoint beam. Whenever a character is to be displayed, a defocus gate is applied to the focus anode of the CRT. When a point feature is to be displayed, the defocus gate is suppressed.

TABLE 4–10. GENERATION OF MIXED RADAR CATEGORIES

MIXED CAT	GENERATED BY RD CAT's
1	5 and 6
2	5 and 7
3	6 and 8
4	7 and 8
5	5, 6, 7, and 8
6	7
7	1 and 2
8	2 and 4
9	1, 2, 3, and 4
10	3 and 4
11	1 and 3
12	1

The beam is intensified only during the time that the SD intensity gate coincides with a category signal (from the CAT and DAB storage and output section) and a feature signal (from the SD timing and control section). The category and feature signals are applied through switches on the console which permits the selection of messages (categories) or parts of messages (features) for display. Those messages which are forced displays bypass the selection switches at the console. Similarly, those features within a message which must be displayed are accompanied by a bypass feature. The bypass-feature signal functions as a feature signal (i.e., AND'ed with the SD intensity gate and the category signal to intensify the beam) but does not go through the selection switches on the console. (Consoles are connected so that a feature signal is not required if the category signal is a radar category.)

The sequence of a message and characters within one SD cycle is discussed in the next chapter. The SD timing and control section generates two signals (conditional-sample and conditional-unblank) which are sent to the MI element. The transfer X, Y or transfer-track-number signal causes the transfer of information from the transfer circuits section to the MI element. An end-cycle signal, which is generated and used internally by the SD timing and control section, is sent to the DTE to trigger it when the SDGE is switched from the drum input to the DTE input.

The SD timing and control section generates six types of signals for use within the SDGE:

a. Clear signals to clear registers and storage circuits before information is gate into them.
b. Read signals which gate signals from the Drum System into registers or storage circuits.
c. Transfer signals which transfer signals from a storage circuit to a register.
d. Advance-character-position and vector-off signals, which are applied to the vector and character positioning section, determine the position of a character within a message and the presence or absence of a vector.
e. Set signals to the character selection section, which supply the selection voltages for the required character of an RD message or for the point character required for the point and vector in TD messages.
f. Signals involved in the transfer of information through the MI element to the Central Computer System.

1.4.9.1 RD Message

During an RD message, the SD focus, defocus, and intensify gates are produced. Since an RD message consists of one word only, no storage is required, and transfer signals (from storage) are not generated. Figure 4–47, foldout, is a functional block diagram of tne RD message.

Radar category control voltages are generated in the SD timing and control section and are decoded in the CAT and DAB storage and output section. The voltages correspond to the RD control bits (L14 identity and L15 status) and to the RD-bright or RD-dim signal from the control circuits of the Drum System. RD category information received from the CAT and DAB storage and output section is used to generate set signals which select the single character of the RD message. (No advance character-position signal is required.)

1.4.9.2 TD Vector Message

The X, Y (positioning) and $\dot{X}$, $\dot{Y}$ (sense and magnitude) information of the first vector of a vector message is routed into the XY and vector registers, respectively, by read X, Y (TD message) and read-vector (vector message) signals. Similar information for V2-V4 is stored in the word storage section, then transferred by transfer X, $\dot{Y}$,$\dot{X}$, Y signals from the SD timing and control section. During the vector display, the set-point signal selects the point-character and the start-vector signal; then the vector-off signal (a negative 50-μsec gate is generated to activate the sweep circuit of the vector generator) is applied. Figure 4–48, foldout, is a functional block diagram of the TD vector message.

The character selection information for the four characters (G1-G4) is transferred to the character register preceding the display of each character. Advance-character-position signals are generated for the positioning of the four characters in a horizontal row.

The TD vector message must be displayed in its entirety. Therefore, during the whole message, the bypass-feature signal is generated by the SD timing and control section and sent to the SDIE.

The start-TD signal sent to the PRRE is amplified in the SD timing and control section. This signal synchronizes SDGE operations with the PRR operations.

1.4.9.3 TD Tabular Messages

For TD tabular messages, the X, Y (position) information, the X, Y information for the single vector, and the selection information for the E character are gated into registers without previous storage. The registers are the X, Y vector and character registers, and gating is accomplished by read word signals from the SD timing and control sections.

Selection of the point character for generating the point and vector is accomplished by the set-point signal from the SD timing and control section. Selection information for the remaining characters of the message is gated into the word storage section by read-word signals. The information for each character is transferred, in turn, to the character register by transfer signals.

Each time a character is transferred, advance-character-position signals are generated.

For the TD tabular track message, the vector and the characters are correctly positioned by the SD timing and control section. Figure 4–49, foldout, is a functional block diagram of the TD tabular message.

During a TD tabular information message, the negative-vector-off gate is not applied to the vector generator because no vector is necessary. Also, the point-feature signal is not generated.

While the A, C, D, and E features are being processed, the bypass-feature signal is generated. This forces the character of those features to be displayed. The SD intensity gate is not generated during the periods corresponding to the B feature. This is done to prevent a conflict between the forced A feature and the B feature because they share the same location on the viewing screen of the SD CRT.

SECTION 2
SDGE, DETAILED THEORY OF OPERATION

2.1 INTRODUCTION

In the detailed theory of operation, this chapter is concerned with the following:

a. TD tabular message operation

b. TD vector message operation

c. Radar message operation

Reference should be made to the individual foldouts and illustrations for each section. The discussions are keyed to the block diagrams. In these diagrams, every circuit involved with the particular type of message concerned is shown as a block with all input and output signals so designated (figs. 4–49, 4–48, 4–47).

2.2 SD INPUT SWITCH AND DRUM SIGNALS

The main function of the SD input switch section is to provide a means of switching from drum signals, which are applied to the SDGE during normal operation, to simulated drum signals, which are applied to the SDGE during a test operation. Switching is accomplished by three relays controlled by the test-SD signal from the DTE. Figure 4–50 is a logical diagram of the SD input switch section.

Normally, relays K1, K2, and K3 are de-energized. In this position of the relays, signal paths are completed for all signals that are sent to the SDGE by the Drum System and the MI element and for those sent through the SDGE to external circuits. An output path is also closed for the signals from the SDGE to the MI element.

2.2.1 Drum System Signals

Thirty-eight signal lines are connected from the Drum System to the generator. Thirty-two of these lines are used to carry information signals for the bits of one word of an SD message and six carry drum control pulses. From the SD input switch section, the bits of one word are sent to the input gates section, and the drum control pulses are sent to the SD timing and control section.

2.2.2 RD Messages

For radar messages, only 24 bits per word are sent from the Drum System: drum LS-L10, L-14, L15, and RS-R10. L14 and L15 are the identity and correlate bits, respectively. Five drum control signals are used: all drum-DTP(OD 1-4 signals on one line), drum-start-RD, drum-WOW, drum-RD dim, and RD-bright.

2.2.3 TD Messages

For vector and tabular messages, 32 information bits are received (drum LS-L15, RS-15). Three drum control signals are used: all-drum-DTP, drum-start-TD, and drum-WOW.

2.3 INFORMATION TRANSFER TO THE MI ELEMENT AND TEST OPERATION

In addition to the signals from the Drum System, a single pulse from the MI element (the MI information-transfer signal) passes through the SD input section into the generator. This pulse causes the transfer of message-identifying information back to the Central Computer System through the MI element. Twenty-eight lines carry this information from the transfer circuit section to the MI element.

2.3.1 RD Message

For radar messages, 22 lines carry the X, Y positioning voltages (XL0-XL10, YR0-YR10). Five other signals sent to the MI element are MI-start-RD, RD, correlated, conditional-sample, and conditional unblank.

2.3.2 TD Vector Message

No signals are sent to the MI element for vector messages.

2.3.3 TD Tabular Track Message

For TD tabular track messages, 22 lines carry track information. Lines C_1–C_3 X 2^0–2^2, Y 2^0–2^2 give the complete character selection address of the first three characters (positions C1 and C3 which may be letters)

of the track number. The last character position (C_4) is always a decimal number and only the two least-significant bits for each axis of the character selection address are required. They are transferred by lines C_4 X 2^0, $X2^1$, $Y2^0$, and $Y2^1$.

MI-start-TD, track-number, conditional-sample, and conditional-unblank signals are also transferred to the MI element.

2.3.4 TD Tabular Information Message

For tabular information messages, no signals are sent to the MI element.

2.3.5 Test Operation

To test the SDGE, the TEST DD-TEST SD switch on the display tester console is thrown to the TEST SD position. This action applies a test signal to energize relays K1, K2, and K3. The contacts of the energized relays break the connection of the SDGE to the Drum System and MI element and connect simulated drum signals from the DTE instead of the normal inputs from the Drum System.

2.4 INPUT GATES SECTION

The input gates section of the SDGE performs two functions. The gate circuits in the section allow the setting of the flip-flops when words are read into the generator element from the Drum System and also act as buffer amplifiers to supply the signals with driving power. At all other times, the gate circuits prevent signal and noise pulses from the Drum System from setting any flip-flops.

The input gates section passes the bits of each word in an SD message being read from the display drums. The bits are received from the Drum System through the SD input switch section. From the input gates section, the words are distributed into specific storage flip-flops in various sections of the generator element. Each bit in a word is permanently associated with one of the gate tubes in the input gates section. The bits may be considered to be coming directly from the drums, since the input switch section performs no logical function dur-

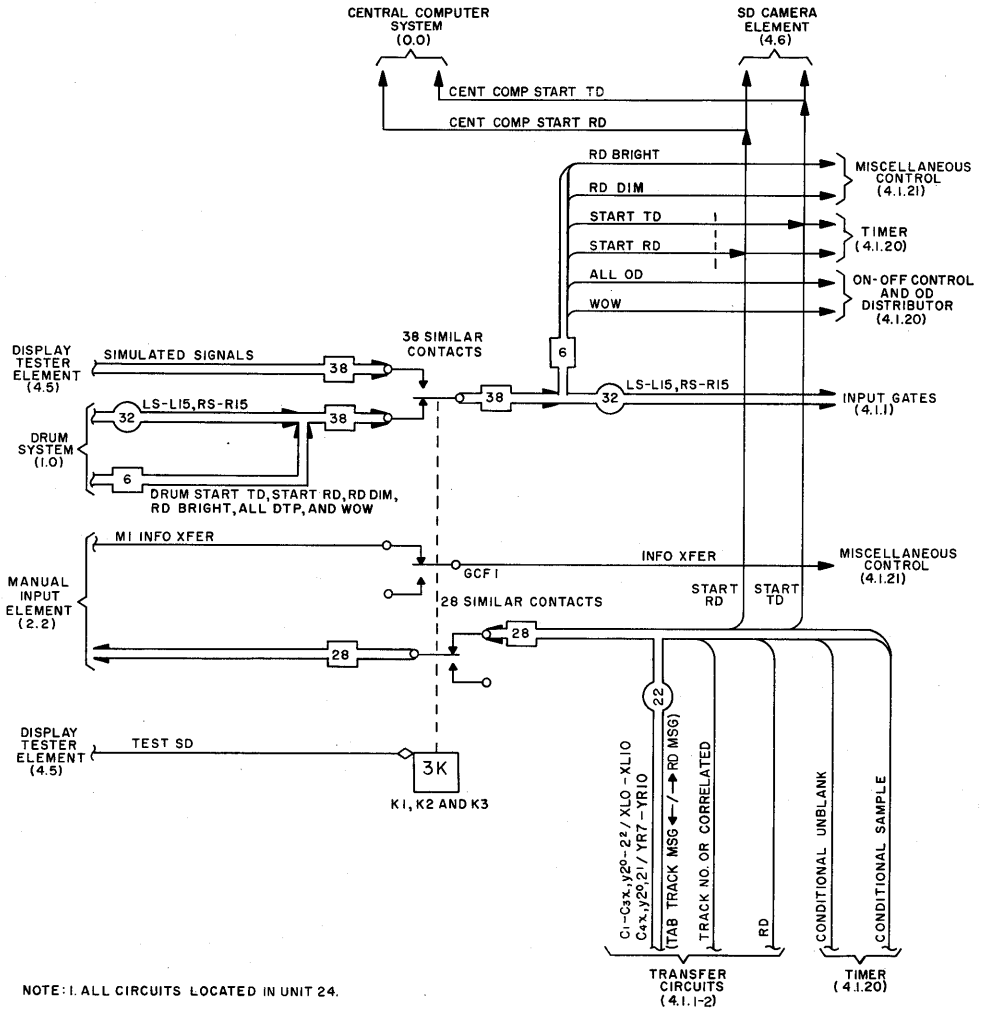


Figure 4–50. SD Input Switch Circuit, Logic Diagram

ing normal operation. Figure 4–51 is a logic diagram of the input gates circuit.

Each word on the SD drums is delivered to the gate circuits at OD 1 time. A WOW signal, which occurs at the preceding OD 4 time, initiates a read signal from the miscellaneous control circuit. The signal is applied simultaneously to all 32 gate tubes and conditions the gates to admit the bits of a word for distribution in the generator.

Each of the 32 gates admits one specific bit to the distribution lines of the generator. Regardless of the type of message being gated in, every input gate is conditioned. Those which are sensed by a bit containing a 1 will pass that pulse to the distribution gates in the subsections of the following sections of the generator element SD word 1: word storage, character selection, vector and format generation, character positioning, XY register storage, X and Y drivers, and CAT and DAB storage and output. The bits are then selectively gated within the subsections of the sections. This gating is accomplished by signals from the SD timing and control section and is dependent upon the particular word and type of message being admitted by the input gates section.

2.4.1 RD Message

For radar messages, the LS-L10, RS-R10 are gated into the SD word 1 XY register message and line drivers, and bits L14 and L15 are applied to the RD control circuit.

2.4.2 TD Messages

The gating of bits for TD vector messages is discussed in paragraphs 2.4.2.1 and 2.4.2.2; and that for TD tabular messages, in 2.4.2.3.

2.4.2.1 TD Vector and Tabular Messages

For both vector and tabular messages, bits L1-L12 and R1-R12 of word 0 (character-selection bits) are gated to word 0 storage. Bit RS of word 0 (vector or tabular message bit) is also gated to word 0 storage. Bits LS-L4 of word 2 (the category bits) are gated into the category storage, matrix, and driver circuit. Bit L5 of word 2 (the display bit) is gated to word 2 storage. Bits L6-L15 and RS-R15 of word 2 and bits LS-L15 and RS-R15 of words 3 and 4 (DAB's) are gated into DAB storage.

2.4.2.2 TD Vector Messages

For vector messages, bits LS-L9 and RS-R9 of words 1, 5, 6, and 7 (positioning bits of the four vector origins) are gated to the XY register. The word-1 bits are gated to the register and held until it is time to gate in the word-5 bits. The same procedure is followed for the word-5 bits, word-6 bits, and then the word-7 bits.

Bits L10-L15 and R10-R15 of words 1, 5, 6, and 7 (sense and magnitude bits of the four vectors) are gated directly into the vector register. The same procedure is followed as that described above for the positioning bits of the vectors.

2.4.2.3 TD Tabular Messages

For tabular messages, bit LS of word 0 (information or track message bit) is gated to word 0 storage. Bits L13-L15 and R13-R15 of word 0 (E character selection bits) are gated into the character register. Bits LS-L12 and RS-R12 of word 1 (message-positioning bits) are gated to the XY register and held until the final-

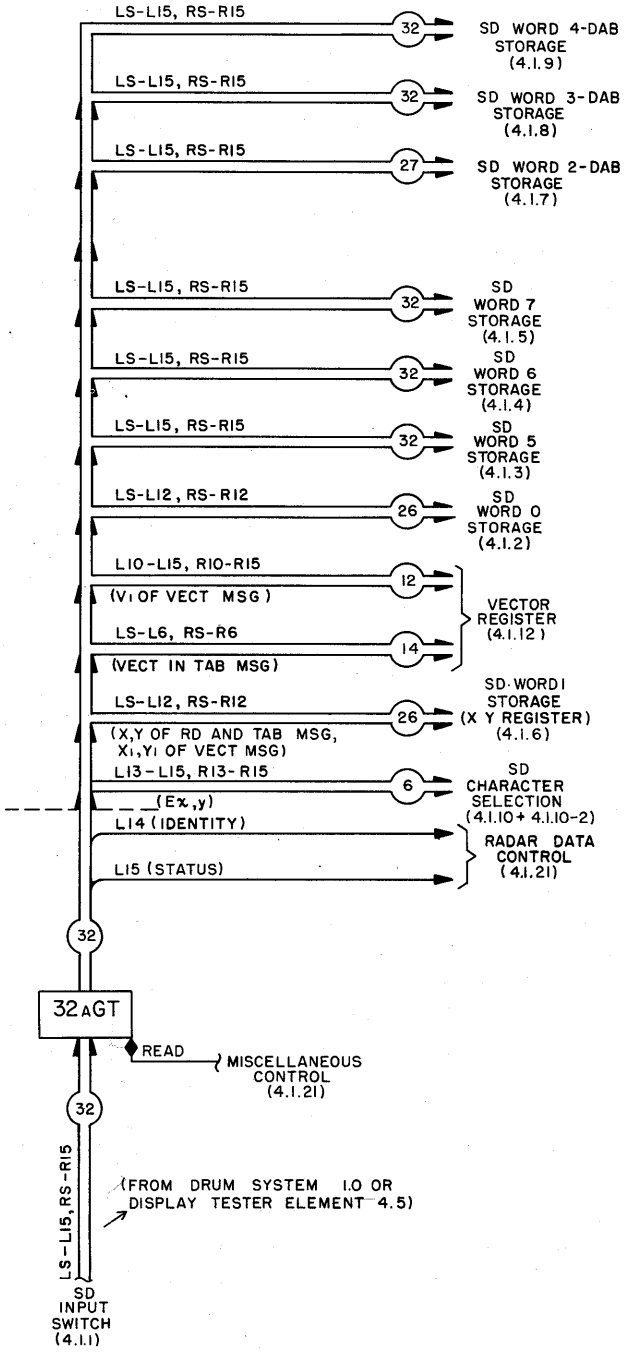


Figure 4–51. Input Gates Circuit, Logic Diagram

message-clear signal. Bits LS-L6 and RS-R6 of word 5 (sense and magnitude bits of the single vector of a track message) are gated directly into the vector register. Bits L7-L15 and R7-R15 of word 5 and bits L1-L15 and R1-R15 of words 6 and 7 (character selection bits) are gated to words 5, 6, and 7 storage, respectively. Bit LS of word 6 (the light gun bit) is gated to word 6 storage, and bit LS of word 7 (format-positioning bit) is gated to word 7 storage.

2.5 WORD STORAGE

Approximately 40 μsec are required to set up current in the deflection yoke to deflect any TD message on its XY position on an SD CRT. Twenty μsec are required for the selection and positioning of any character by means of the character selection plates and positioning plates. Twenty-five μsec are required for the intensification of each character on the viewing screen, and 5 μsec are required to switch from the generation of one character or vector to another. The eight words of a vector message contain bits for selecting four characters and four vectors; the eight words of a tabular message contain bits for selecting up to 18 characters and a vector. The words are read into the generator at 10-μsec intervals. The time requirements, therefore, for the total display of a TD message, exceed the time during which the message is read from the drum. Storage flip-flops are employed in the generator to hold the bits of the words until it is time for each separate display of a character or vector.

The word storage section contains the flip-flops for storing words 0, 5, 6, and 7 of a TD message being read from the drum until the proper time occurs for generating the displays represented by the bits in the words. Prior to the receipt of the first word of a TD message from the TD drum, all the storage flip-flops in word 0, 5, 6, and 7 storage circuits are cleared by clear pulses from the on-off control and OD distributor.

The 32 bits of all eight words in a TD message (LS-L15 and RS-R15) are applied to the word storage section from the input gates section. Bits LS-L12 and RS-R12 sense 26 capacitor-diode gates in word-0 storage; bits LS-L15 and RS-R15 sense capacitor-diode gates in word-5, word-6, and word-7 storage. (Bits L13-L15 and R13-R15 of word 0 are the E feature character selection bits and they sense the character selection section.) These same bits sense the word-distribution (admittance) gates in all of the word storage circuits regardless of which word is being gated into the SDGE by the input gates section. However, for the bits of a word to be admitted to the appropriate storage circuit (e.g., word 0 bits to word 0 storage), a conditioning level peculiar to that storage circuit must be applied to its word-admittance gates.

The conditioning voltages for the word 0, 5, 6, and 7 storage circuits are the read-word-0, -5, -6, and -7 signals developed in the gate generator. Each read-word signal is a result of a specific symbol-sequencer count; read-word-0 is applied when the symbol sequencer is 5, read-word-6 when the symbol sequencer is 6, and read-word-7 when the symbol sequencer is 7. Word storage of the 1-word RD message is not required.

2.5.1 Word 0 Storage

Twenty-four of the 26 bits stored in word 0 storage contain information which, after decoding, selects the characters to be displayed in positions A_1, A_2, A_3, and A_4 of a tabular message or positions G_1, G_2, G_3, and G_4 of the vector message. This character selection information is sent to admittance gates in the character register where it is sensed at specific times by character-transfer signals from the SD timing and control sections. Four signals from two control bits are also developed in word 0 storage and indicate to other circuits within the generator what type of message is being gated in. The control bit signals are tabular-message, vector-message, information-message, and track-message. All the signals are used in the SD timing and control section, and the tabular- and vector-message signals are used as well in the character counting and positioning circuit.

2.5.1.1 TD Tabular Message

Word 0 storage consists of 26 flip-flops and their associated input (distribution) gates. This circuit converts the word 0 character selection bit pulses received from the drum into digital d-c levels that are normally +10 and −30V. These pulses select characters A_1-A_4. Bits L13-L15 and R13-R15 of word 0, the x, y bits of the E character, bypass 0 storage and pass immediately into the character register. The bits are then stored for the duration of the TD message display cycle.

Figure 4–52 is a diagram of word 0 storage. Flip-flops 1 through 26 are cleared by clear pulses from the on-off control and OD distributor before a TD message is read from the drum.

Twenty-six bits (LS-L12 and RS-R12) from the input gates section are applied to capacitor-diode gates 1 through 26. Coincident with the appearance of word 0, a read-word-0 signal from the gate generator is applied to gates 1 through 26. This signal conditions the gates, thereby admitting bit LS to FF 1, RS to FF 2, and bits L1-L2 and R1-R12 to FF's 3 through 26. The outputs of the flip-flops are connected to capacitor-diode gates in the character register and are passed into the register by transfer signals from the timing and control section at the proper time.

Word 0 contains two control bits, LS and RS. Each of the bits causes one or two d-c level signals to be sent out of word storage. Signals indicate to circuits in the timing and control section whether the message being

read in from the TD drum is tabular or vector; if it is tabular, they indicate whether it is information or track. The 0 and 1 side outputs of FF 1 are used in a tabular message to indicate, respectively, track and information types of tabular messages. When control bit LS is a 1, it sets FF 1. The 1 side (information-message-side) of the flip-flop is then up. When bit LS is a 0, the flip-flop remains in its cleared state with the 0 side (track message side) up. Control bit RS develops either a tabular- or a vector-message signal in FF 2; in much the same way, the 0 side of the flip-flops develops a tabular-message signal; the 1 side, a vector-message signal. The control-bit signals are connected from the flip-flops to the SD timing and control section and the character position counter.

2.5.1.2 TD Vector Message

Word 0 storage for vector messages is similar to that for TD tabular messages. The stored character selection bits are for character G1-G4.

2.5.2 Word 5 Storage

Word 5 storage consists of 32 flip-flops and their associated input (distribution) gates. This circuit transforms the 32 bits of word 5 from pulse signals to d-c level signals and stores them for the duration of the message display cycle. Figure 4–53 is a logic diagram of word 5 storage.

Flip-flops 1 through 32 are cleared, before drum reading of a TD message begins, by clear pulses from the on-off control and OD distributor.

Bits LS-L15 and RS-R15 from the input gates section are applied to capacitor-diode gates 1 through 32. Coincident with the arrival of word 5 from the input gates section, a read-word-5 signal from the gate generator is also applied to the 32-word admittance gates. This signal conditions the capacitor-diode gates which then admit bits LS-L15 and RS-R15 to the 1 side of FF's 1 through 32.

2.5.2.1 TD Tabular Message

All of word 5 of a tabular message is gated into word 5 storage. However, only information from the 1 side of the flip-flops pulsed by bits L7-L15 and R7-R15 is used. These bits form character selection addresses and are connected to the capacitor-diode gates of the character register. Bits LS-L6 and RS-R6 of a TD tabular message are the sense and magnitude of the vector in the message, and are passed directly through the in-

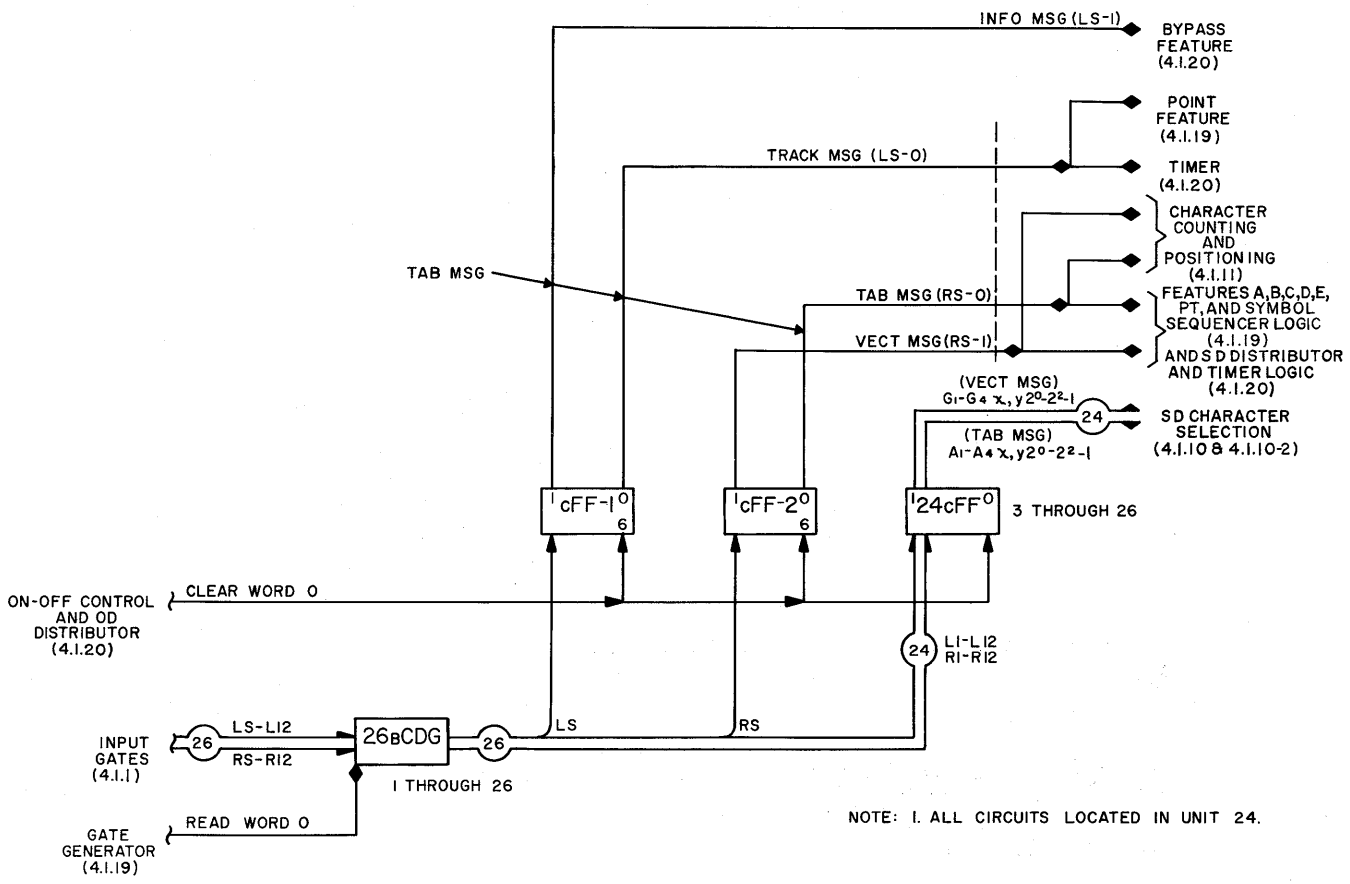


Figure 4–52. SD Word 0 Storage Circuit, Logic Diagram

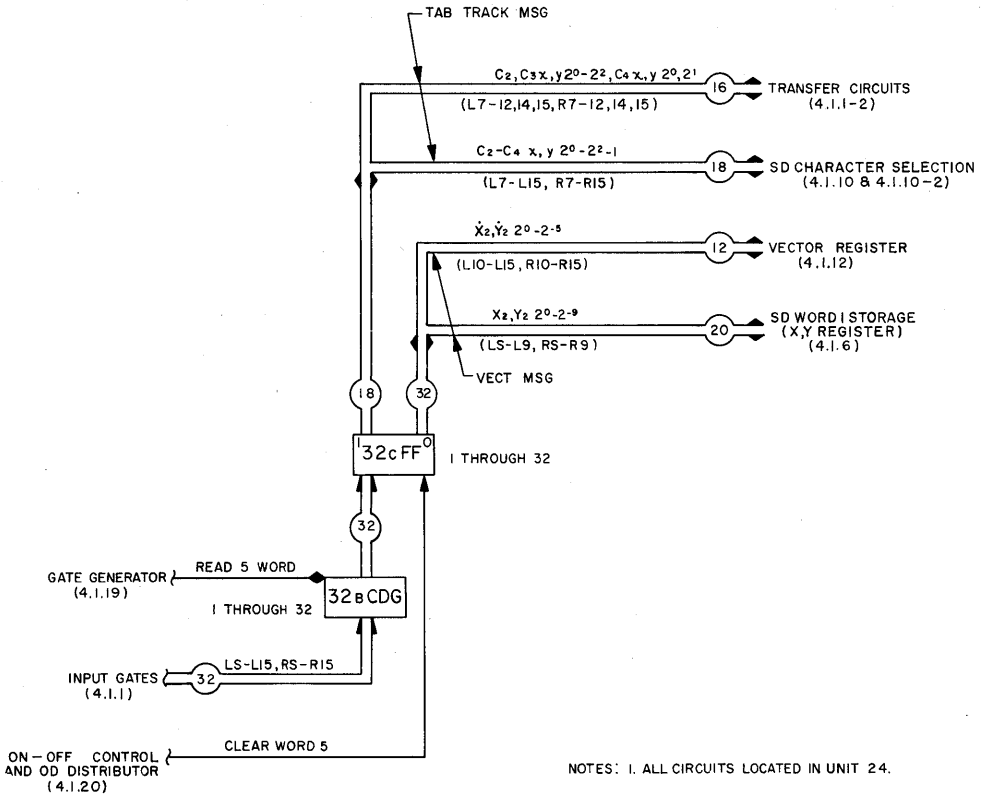


Figure 4–53. SD Word 5 Storage Circuit, Logic Diagram

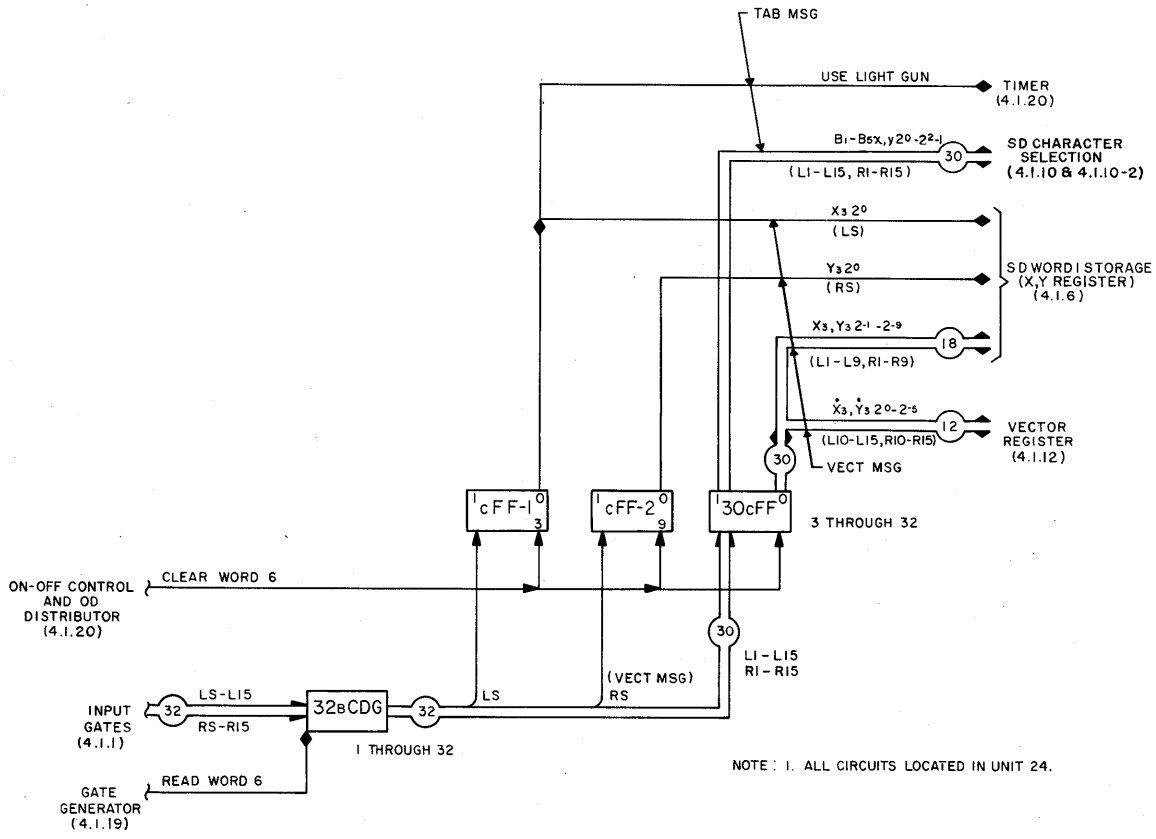


Figure 4–54. SD Word 6 Storage Circuit, Logic Diagram

put gates section into the vector register. The word 5 character selection bits of a TD tabular message specify characters in the track number of the message; they are therefore also connected to the transfer circuits section for re-entry into the Central Computer System through the MI element. (Only the two most significant bits in each address co-ordinate of C_4, a numeral, are used for this purpose.)

2.5.2.2 TD Vector Message

Word 5 of a TD vector message contains the bits that determine the origin, sense, and magnitude of the second vector message. The positioning (point of origin) information for the second vector is contained in 20 of these 0-side outputs ($X_2 2^0$–$X_2 2$–9, $Y_2 2^0$–$Y_2 2$–9) which are derived from bits LS-L9 and RS-R9. These 20 X_2, Y_2 signals are sent to the XY register and drivers section. The remaining 12 0-side outputs contain X_2, Y_2 information (sense and magnitude of the second vector) and are derived from bits L10-L15 and R10-R15. These 12 $\dot{X}_2$, $\dot{Y}_2$ signals ($\dot{X}_2 2^0$–$\dot{X}_2 2$–5, $\dot{Y}_2 2^0$–$\dot{Y}_2 2$–5) are sent to gates in the vector register and passed into the register by a transfer $-X_2$, Y_2, $\dot{X}_2$, $\dot{Y}_2$ pulse from the SD timing and control section. The original number in word storage is therefore placed in the register, since the 0 side of the storage flip-flop output is used (outputs to the transfer circuits are not used in the TD vector messages).

2.5.3 Word 6 Storage

Word 6 storage comprises 32 flip-flops and their associated admittance (distribution) gates. This register of flip-flops transforms the bits of word 6 into d-c levels and stores the data until it can be decoded from binary to analog form, and displayed. Figure 4–54 is a logic diagram of word 6 storage.

Prior to the arrival of a message, clear pulses from the on-off control and OD distributor are applied to the 0 side of FF's 1 through 32. Bits LS-L15 and RS-R15 of word 6 are passed from the input gates section into the 1 side of FF's 1 through 32 when a read-word-6 signal from the gate generator is applied to capacitor-diode gates 1 through 32.

2.5.3.1 TD Tabular Message

Word 6 of a TD tabular message contains character selection bits which are connected to the character register. Word 6 also contains a single bit, LS, which develops a use-light-gun signal. The bit is applied to FF 1. When this bit is a 0, the 0 side of the flip-flop remains up. This level is applied to the timer as a use-light-gun signal.

2.5.3.2 TD Vector Message

Word 6 of a vector message contains the origin, sense, and magnitude bits of the third vector in a vector message. The point of origin information ($X_3 2^0$–$X_3 2$–9, $Y_3 2^0$–$Y_3 2$–9) is taken from the 0 side of the flip-flops, which store bits LS-L9 and RS-R9, and is sent to the XY register and drivers. The sense and magnitude information of the third vector ($\dot{X}_3 2^0$–$\dot{X}_3 2$–5, $\dot{Y}_3 2^0$–$\dot{Y}_3 2$–5) is taken from the 0 side of the flip-flops, which store bits L10-L15 and R10-R15, and is sent to the vector register. In both registers, the information conditions gates which are sensed at the proper time by transfer signals from the SD timing and control section. The gates in the register are of the diode-capacitor, or inverting, type. The original number in the word storage is therefore placed in the registers, since the 0 side of the storage flip-flop output is used.

2.5.4 Word 7 Storage

Word 7 storage, like word storages 5 and 6, consists of 32 flip-flops and their associated gates. The circuit converts the pulse information of word 7 into d-c level signals. Figure 4–55 is a logic diagram of word 7 storage.

Prior to the arrival of a message, FF's 1 through 32 are cleared by clear pulses from the on-off control and OD distributor.

Bits LS-L15 and RS-R15 are applied from the input gates section to the 32-word admittance gates regardless of which word is being read from the drums. However, they will be admitted to the seven storage flip-flops only when a read-word-7 signal from the gate generator conditions capacitor-diode gates 1 through 32.

2.5.4.1 TD Tabular Message

Word 7 of a TD tabular message contains character selection bits. After entering storage, the bits are transferred to the character register in the same manner as the character selection bits in word storages 5 and 6. Bit LS is a position control bit for tabular messages. The bit is stored in FF 1. When the position bit is 0, the 0 output of the flip-flop places the character format to the left or right of the vector origin. When the bit is 1, the 1 output of the flip-flop places the format above or below the vector origin. The flip-flop outputs are used in the character counter and positioning circuit. The character selection bits of character C, in word 7 of a tabular message, are those of the letter part of the track number of the message. They are also connected into the transfer circuits section for re-entry into the Central Computer System through the MI element.

2.5.4.2 TD Vector Message

Word 7 of a vector message contains the origin (X4, Y4) and sense and magnitude ($\dot{X}4$, $\dot{Y}4$) bits of the fourth vector in the message. After entering storage, the bits are transferred to the XY and vector registers in the same manner as the vector information in words 5 and 6. (The outputs obtained from the position control bit, LS, are not used for vector messages.)

2.6 CHARACTER SELECTION REGISTER

The character register and the character selection decoders and line drivers compose the character selection section. Together, these circuits store digital voltages and decode them into analog voltages to select one character at a time from the character-forming matrix in the display tubes.

2.6.1 Character Register

A single register of six flip-flops, together with OR circuits and 18 logical groups of six capacitor-diode gates each, compose the character register. (See fig. 4–56, foldout.) The contents of the six flip-flops vary in accordance with the character selection addresses received from the word storage section, E feature circuit (set-point signal), or the input gates section (E character) during a TD message display cycle, and with the addresses received from the RD control circuit during an RD message display cycle.

Applied to the character register are 102 d-c levels from the word storage section. Six of these levels are required to select each character. The levels carry the bit information for selecting the following characters in a TD tabular message: A_1–A_6, B_1–B_5, C_1–C_4, D_1, and D_2. Twenty-four of the levels carry the bit information for selecting the G_1–G_4 characters in a TD vector message. The six character selection bits of each character are transferred into the character register in the proper sequence and at the proper time by 17 character-transfer

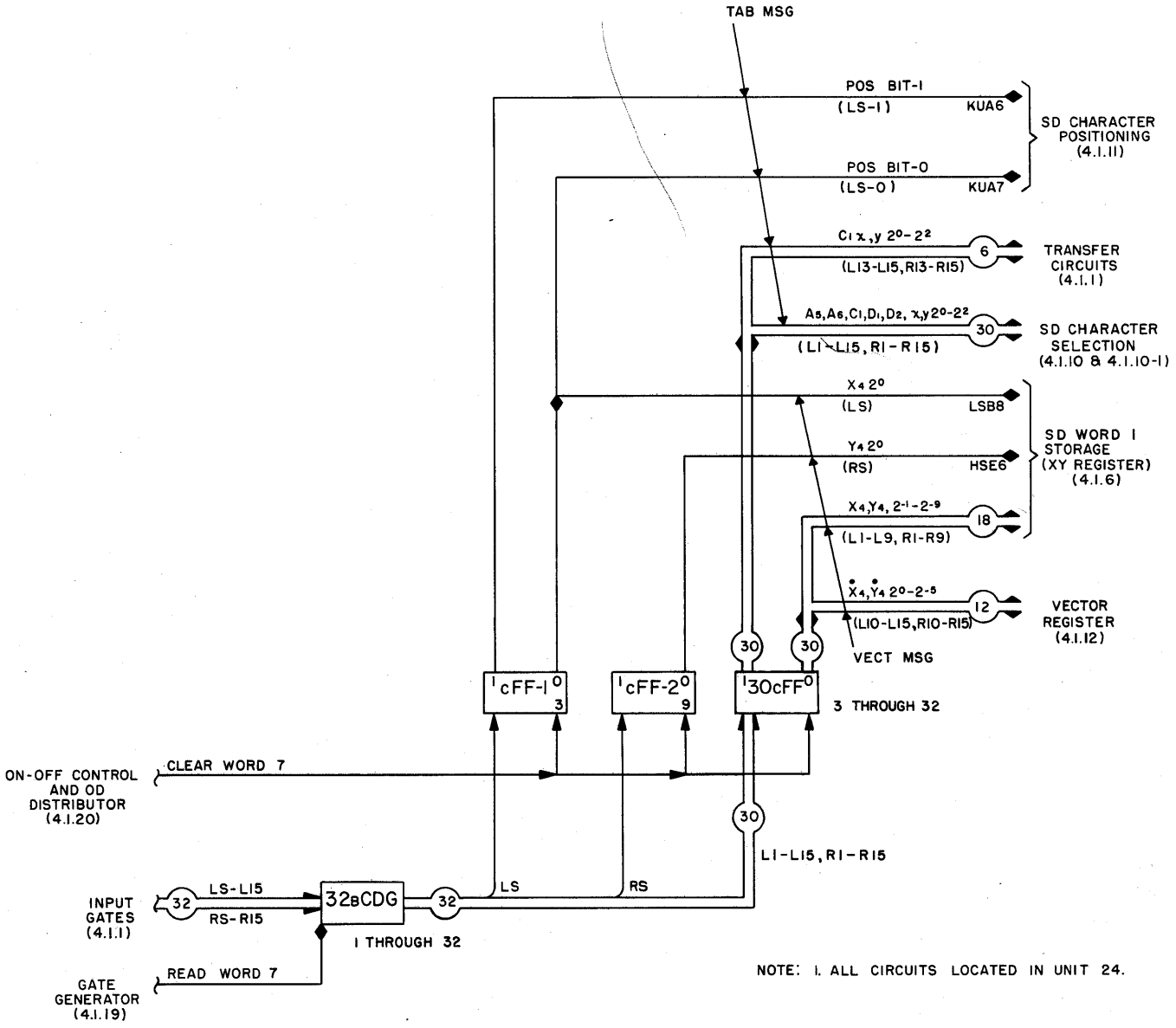


Figure 4–55. SD Word 7 Storage Circuit, Logic Diagram

signals from the SD timing and control section. Provision is also made for the selection of the E and point characters of a TD tabular message, of the point character for vector generation, and of the single character (out of a possible four) of an RD message.

Before the selection of a new character or point, clear-character-register pulses from the SD timing and control section clear the six character register flip-flops. The flip-flops retain the digital character selection bits for each character or point from the time the character selection information is transferred into them until they are cleared by the clear-character-register pulse.

2.6.1.1 TD Tabular Message

Twenty-four d-c levels, connected from the 1 sides of the flip-flops in word 0 storage, are applied to four separate groups of six capacitor-diode gates. The 24 signals contain the information which, after decoding, will select from the character-forming matrix characters A_1–A_4 of a TD tabular message. Each character is represented by three signals ($x2^2$–$x2^0$) for the horizontal axis address and three signals ($y2^2$–$y2^0$) for the vertical axis address.

The six x and y signals for A_1 of a tabular message are applied to the six capacitor-diode gates that are pulsed simultaneously by the transfer-A_1–G_1 pulse. The six gated outputs are applied to the 1 sides of FF's 1 through 6. Because the gates are conditioned by the 1 outputs of the storage flip-flops, the same number is made to appear in the register as in word 0 storage. The x and y addresses for each of the other characters selected for TD tabular messages (A_2–A_6, B_1–B_5, C_1–C_4, D_1–D_2) are brought into the register flip-flops from the word storage section by character-transfer signals in the same manner as character A_1. The address signals are shown as inputs to the register in figure 4–56.

The E character is the first to be displayed in a TD tabular message. Therefore, the information required to select the E character is gated directly from the input gates section into the character register. The gates which admit these pulses are conditioned at the proper time by a read-word-0 signal from the SD timing and control section. The character selection information for the single E character is applied directly from the track display drum through the SD input switch and input gates sections to the character register. Bits L13-L15 and R13-R15 of word 0, which contain the E character selection address, sense the six gates. A read-word-0 signal from the gate generator is applied to the gates at the same time that word 0 appears from the TD drum. The outputs of the gates are applied through OR's to the 1 sides of FF's 1 through 6. (Bits L13-L15 and R13 and R15 are not used in a TD vector message; therefore, no information can be transferred to the flip-flops by the read-word-0 signal.)

The selection of the point, which is also swept to produce the single vector of a TD tabular message, is carried out in a manner similar to the selection of a character. The aperture through which the focused beam is passed to produce the point is at the x = 111, y = 111 binary address in the character matrix. Therefore, the same combination of outputs from FF's 1 through 6 is always required. This combination is 111 in FF's 1-3 and in FF's 4-6. The six flip-flops are set by the set-point signal from the E-feature circuit.

2.6.1.2 TD Vector Message

Each vector of a TD vector message requires the selection of a point from the character-forming matrix. The point is then swept to produce the vector.

Character selection bits for G_1, G_2, G_3, and G_4 enter the character register on the same lines as those for A_1, A_2, A_3, and A_4. The six x and y signals ($x2^2$–$x2^0$, $y2^2$–$y2^0$) for G_1 of the vector message are applied to the six capacitor-diode gates that are pulsed simultaneously by the transfer $-A_1/G_1$ pulse during a TD vector message. The G_2, G_3, and G_4 bits are gated in by appropriate transfer pulses. The gated outputs for the G characters are then placed in the character register flip-flops in the same manner as the A character of a TD tabular message.

2.6.1.3 Radar Message

The address of the character to be displayed for an RD message is placed in the character register by set signals from the RD control circuit in the SD timing and control section. The character to be displayed depends on the category of the message.

Four possible set pulses from the RD control are applied to the character register during each RD message display cycle. The pulses are a set $y2^2$, $y2^0$ signal and a combination of set $x2^2$, set $x2^1$, and set $-x2^0$ signals. The last three signals are applied to the 1 side of FF's 1, 2, and 3, respectively. The set $-y2^2 + y2^0$ signal occurs for every RD message and places 1's in FF's 4 and 6. Flip-flop 5 ($y2^1$) always remains cleared. The result is that the combination of FF's 4, 5, and 6 is always binary 101 during an RD message; binary 101 is the vertical axis address for all the characters displayed in RD messages. The set $-x2^2$, set $-x2^1$, and set $-x2^0$ signals occur in a specific combination for each RD message and place the horizontal character address in FF's 1-3 for the character to be displayed for the message.

2.6.2 Character Selection Decoders and Line Drivers

The 1 and 0 side outputs of the six character register flip-flops are sent to the character selection decoders and line drivers and to the character position decoders. The character selection decoders decode the 12 digital voltages into four push-pull analog character selection

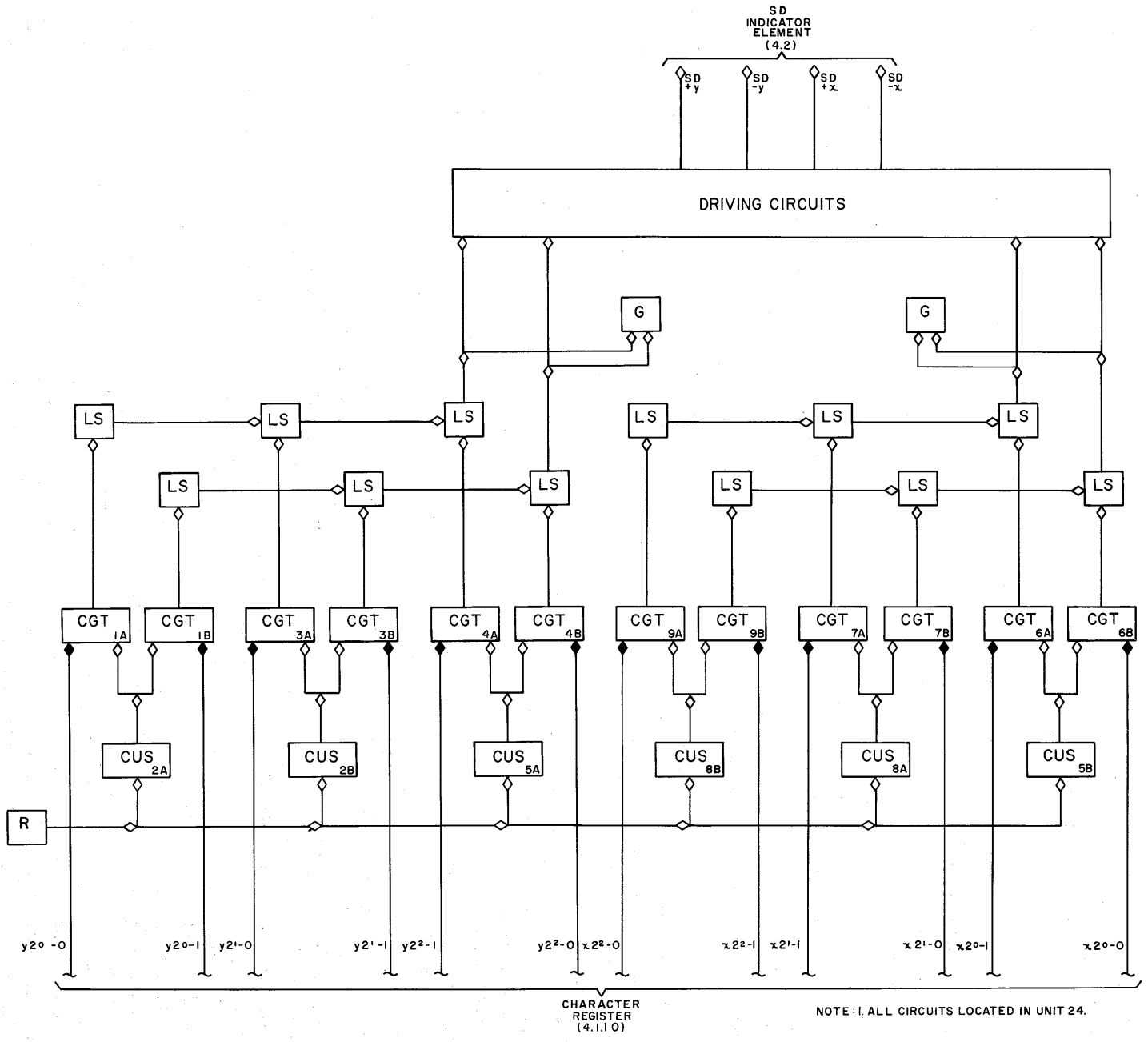


Figure 4–57. SD Character Selection Decoders and Line Drivers Circuit, Logic Diagram

voltages; the analog voltages are sent to the character selection plates in each SD CRT. The character register outputs are sent to the character position decoders to compensate for the off-axis displacement of the electron beam caused by deflecting the beam to a particular address on the character-forming matrix.

Binary numbers representing specific vertical and horizontal character-matrix addresses are supplied by the character register to the character selection decoders. The decoders transform the numbers into push-pull analog voltages which direct a display tube electron beam to a particular character, decimal number, or symbol in the character-forming matrix of the tube. The analog line drivers amplify the analog voltages and supply the necessary power to carry these voltages to the SD CRT's in the SDIE. Figure 4–57, foldout, is a logic diagram of the character selection decoders and line drivers.

The 0 and 1 outputs of the $y2^2$, $y2^1$, and $y2^0$ flip-flops in the character register are connected to current gate tubes (CGT) 4, 3, and 1, respectively. The 0 and 1 outputs of the $x2^2$, $x2^1$, and $x2^0$ flip-flops in the character register are connected to current GT's 6, 7, and 9, respectively. Each tube has two sections (A and B); one section is connected to the 0 side of the register flip-flop; the other section is connected to the 1 side. Both sections of one tube are supplied by the same current source tube. The signal inputs to a current gate tube will be the 1 or 0 held in the register flip-flop. One input will then be +10V; the other input will be −30V. The current gate tube section receiving the +10V signal will conduct current from the source tube through the ladder section (LS) associated with the current gate tube section; the current gate tube section receiving the −30V signal will not conduct current through its ladder section. In this manner, one bit of a character selection number will be converted through paired decoder stages (current gate tube sections and ladder sections) into a push-pull analog voltage.

Following the pattern of operation of all decoder circuits, the decoder stage for the bit is designed so that the analog voltage developed by the bit is proportional to the position of the bit in the binary number. All bits of the x and y character selection numbers from the character register are decoded in the same manner as the single bit just described. The positive and negative x and y analog character selection voltages from the ladder sections are delivered through line drivers to the character selection plates of all SD tubes. The symbol R on figure 4–57 represents a voltage regulator tube that keeps the currents drawn from the current source tubes at constant values. The symbol G represents an adjustable gain control.

2.7 CHARACTER COMPENSATION AND POSITIONING AND VECTOR GENERATION

The character positioning and vector generation section of the SDGE contains circuits that generate the vectors and provide for compensation and positioning of the characters in the display of TD messages. The output of the section consists of analog voltages which are applied to the vector generating and character compensating and positioning electrostatic deflection plates of the SD CRT's in the consoles of the indicator element. RD messages involve character compensation only.

2.7.1 Character Compensation

Character compensation is required for all messages to compensate for the deflection of the CRT beam necessary to select the required characters. Character compensation is accomplished in the character position decoders; this is covered in 2.7.2.3 of this section.

2.7.2 Character Positioning

The display of a TD tabular message and a TD vector message is shown in figures 4–2, 4–3, and 4–4. The spacing of the characters in the display is determined by the character counter and positioning circuit. The counter acts on available information (sense bits of vector, type of message, and positioning bit) to generate digital voltages for placing the characters in a specific position with respect to the central position and for placing the individual characters in their proper positions relative to one another. The latter grouping is called the character format of a message.

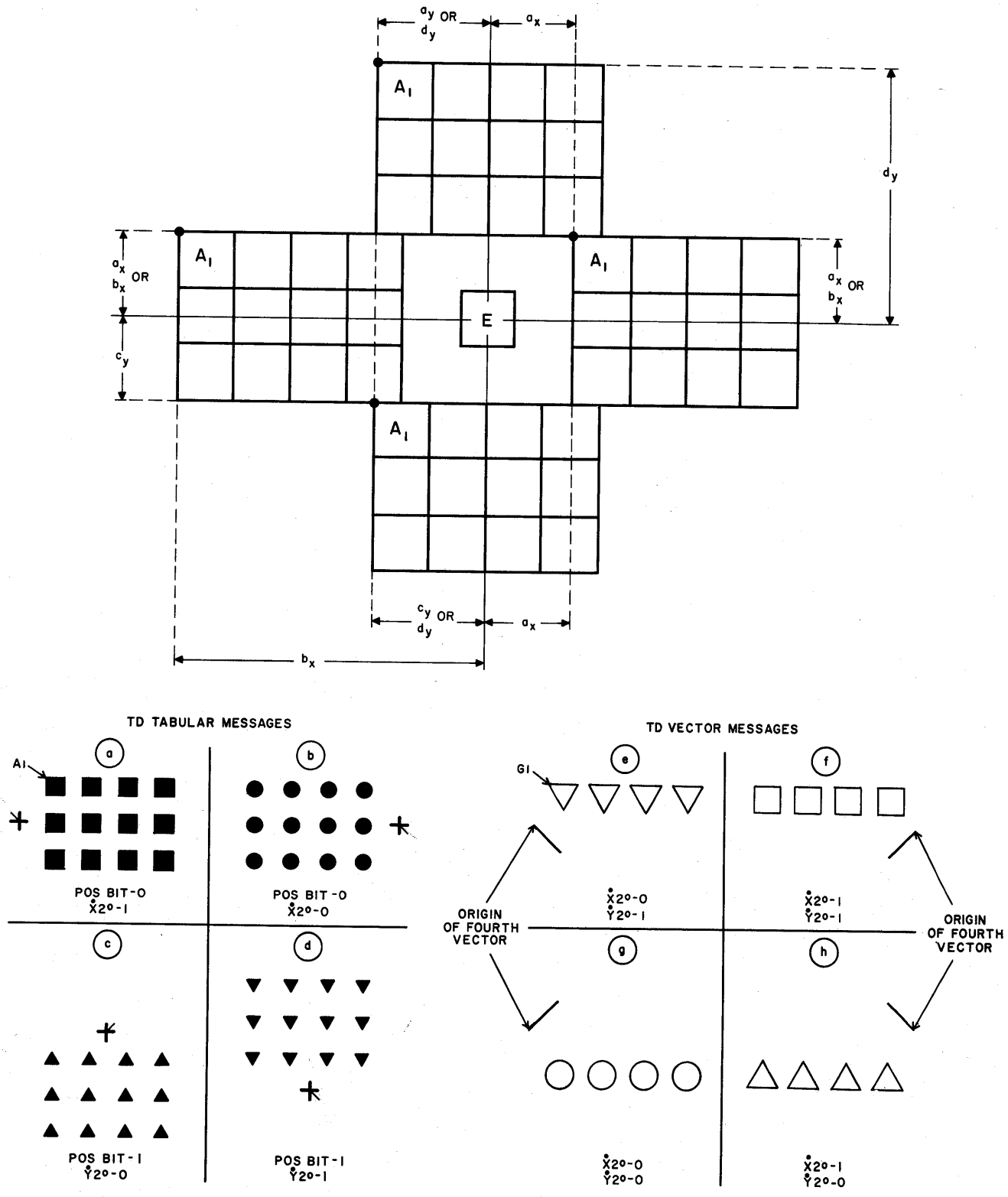
The basic position in TD tabular messages is the XY position (E character, point, and vector origin). The basic position in TD vector messages is the origin of the fourth vector (X4, Y4). Figure 4–58 shows the possible character format positions with respect to the central position (represented by the cross).

There are eight positions of the character formats with respect to the central position, as shown in figure 4–58. Four positions pertain to TD tabular messages and four to TD vector messages. The positioning bits (LS of word 7) pertain only to TD tabular messages.

The digital voltages produced by the character counting and positioning circuit are decoded by the character position decoder.

2.7.2.1 Character Counting and Positioning Circuit (TD Tabular Message)

Two control signals are applied to the character counter and positioning circuit by the SD timing and control section: an advance-character-position signal that steps the counter and a clear signal that restores the counter flip-flops to 0 outputs. The word storage section supplies a tabular message signal and two for-



NOTES: 1. + POSITION OF THE E CHARACTER, POINT AND VECTOR ORIGIN IN TD TABULAR MESSAGE; POSITION OF FOURTH VECTOR ORIGIN IN TD VECTOR MESSAGE.
2. E,W,N, AND S ARE ARBITRARY COORDINATES WITH RESPECT TO +.

Figure 4–58. Relative Positions of Character Formats

mat-positioning signals to the character counter and positioning circuit. Four format-positioning signals originate from a positioning control bit and from the vector sense bits in a TD tabular message. If the positioning bit is 0, the characters in a tabular message are positioned to the right or left of the vector. If the positioning bit is 1, the characters are positioned above or below the vector. The vector sense bits (the first $\dot{X}$, $\dot{Y}$ bits of the vector), which are also connected to the character counter and positioning circuit from the vector register, give the final determination of the position on the horizontal and vertical axes (TD tabular information messages, although containing no vector, do contain the vector sense bits which are required for format positioning).

In the above-below direction, the format appears opposite to the $\dot{X}$ $\dot{Y}$ (vertical) direction of the vector In the right-left direction, the format appears opposite to the horizontal direction of the vector. Boxes shown in figure 4–8 which outline the position of the characters in the format do not appear on the screen. Neither do the letters in the boxes appear in the actual display, but simply represent the classification of character positions in the format. All of the A characters constitute the A feature; all of the B characters constitute the B feature, etc.

The character counting and positioning circuit produces outputs in digital form, which are then translated into analog voltages by the character position decoders. These analog voltages are applied (through the vector generator and character position line drivers) to the vector generating and character compensating and positioning plates of all the SD CRT's. During a TD tabular message display cycle, the counter outputs are all 0 until vector generation is completed. Then the character counter and positioning circuits generate voltages which position the first character in the format (A_1).

The counter is then stepped successively to produce the positions for the display of each remaining character in the format. The character counting and positioning circuit (fig. 4–59) consists of flip-flops that supply the digital positioning voltages. The AND circuits are used to set FF's 2, 4, 6, and 8 which determine the initial or set condition for positioning the first character of the character format. The flip-flops produce aX, bX, cY, and dY outputs, respectively. The lower case letters a, b, c, and d, which prefix the output designations, refer to the four possible positions of the character format with respect to the central position, as shown in figure 4–58. Flip-flops 1 and 3 compose the X counter; FF's 5 and 7, the Y counter. A change in the condition of the eight flip-flops results in an equivalent change in the analog-positioning voltage.

Assume that the positioning bit of a TD tabular message is a 0 and the $X2^0$ (sense) bit is a 1 (fig. 4–58, part a). When a previous message ends, all the flip-flops are cleared, setting the 0 state. This meets the conditions under which AND 1 can apply a d-c level to GT 1. For the message under consideration, AND 2 is also conditioned to apply a d-c level, via OR 2, to capacitor-diode gate 1. The three inputs to AND 2 are the position-bit-0 signal originating in the word 7 storage circuit, the sense bit signal ($X2^0$-1) coming from the vector register, and the signal indicating that the message is tabular, which comes from the word 0 storage circuit. After the vector of the message is displayed, the first advance-character-position pulse is received from the timer. This pulse is gated through GT 1 and capacitor-diode gate 1, setting FF 2. The result is the application of a voltage (via the decoders and line drivers) to the positioning plates, deflecting the A_1 character to its proper position.

Once FF 2 has been set to 1 by the first advance-character-position pulse, AND 1 no longer applies a d-c level to GT 1. However, OR 1 applies a d-c level to GT 2, for the remainder of the message, and the X and Y counters (FF's 1, 3, and 5, 7) can now function. After the A_1 character has been displayed, another advance-character-position pulse is received. This pulse is gated through GT 2, complementing FF 1. The new condition of the flip-flops results in a new deflection voltage, placing the A_2 character in the proper position. The B_1 character is displayed in the same position on the screen, but feature selection switches at the consoles are used to prevent superposition of the two characters. The third advance-character-position pulse, which occurs after the display time of the B_1 character, complements FF's 1 and 3. The complementing pulse resets FF 1 to the 0 state and sets FF 3 to the 1 state, resulting once again in a new positioning voltage. The fourth advance-character-position pulse occurs after the display time of the B_2 character and complements FF 1, setting it to the 1 state. The fifth advance-character-position pulse occurs after the display time of the B_3 character. This pulse is gated through GT's 2, 3, and 4, complementing FF's 1, 3, and 5, respectively. This complementing causes FF's 1 and 3 (X flip-flops) to be reset to 0 and FF 5 (Y flip-flops) to be set to 1. Viewed from the display tube, this means that the first row of characters has been positioned and displayed and the second row is about to be displayed. Each additional advance-character-position pulse steps the counter in a similar manner until the remaining two rows of characters are positioned. After the last (C_4) character has been displayed, a clear pulse (from the on-off control and OD distributor) resets all the flip-flops to 0, readying the character position counter for the next message.

The tabular message discussed above is shown in figure 4–60. The E character, the point, and the origin of the vector are represented by the cross, and the

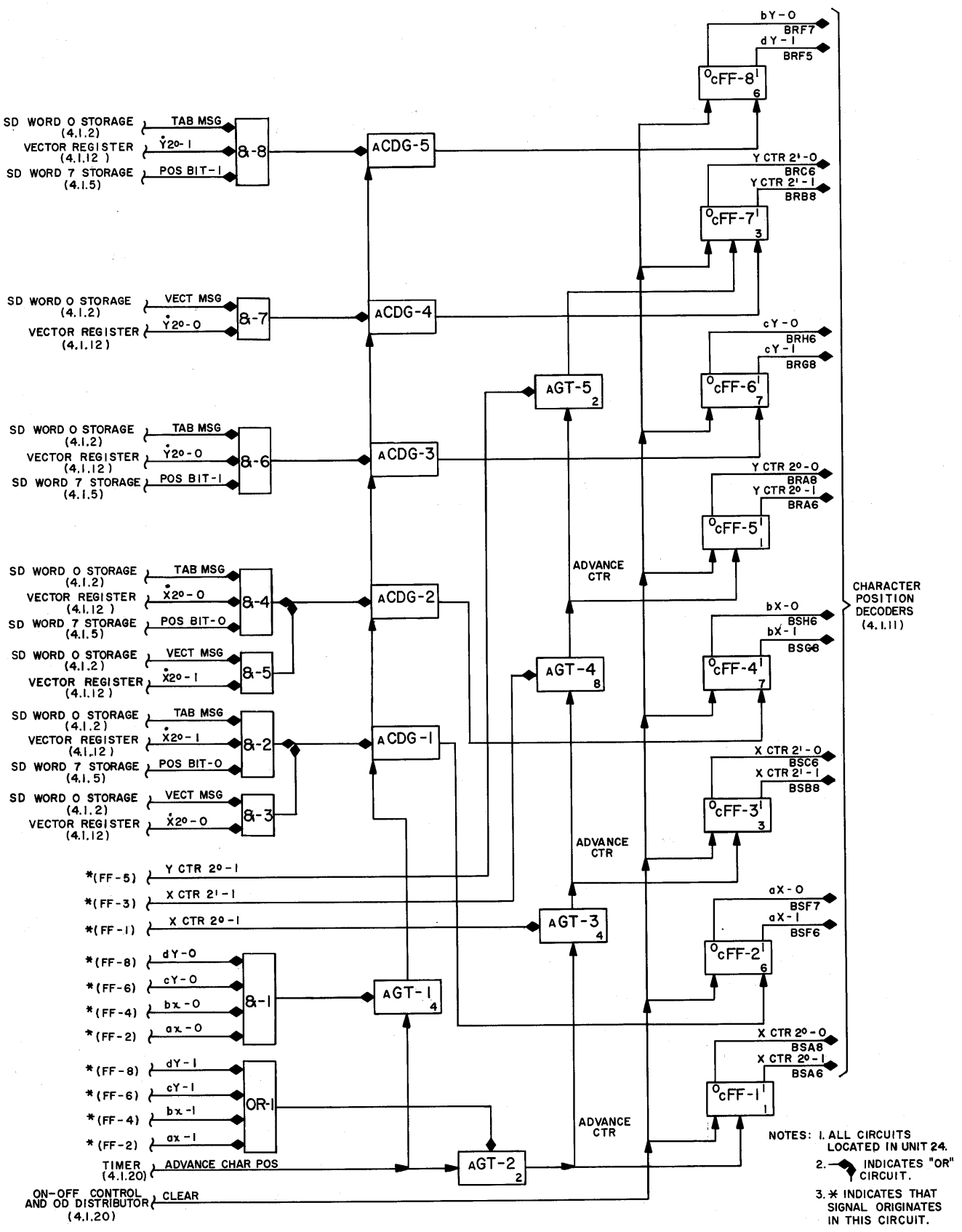


Figure 4–59. SD Character Counting and Positioning Circuit, Logic Diagram

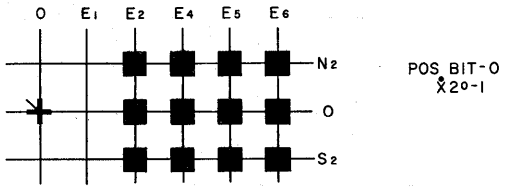
shaded squares indicate the positions of the characters in the message. The co-ordinate positions of the displayed characters are listed in the first horizontal row of the tabulated information. The columns should be read in the following manner: the fourth advance-character-position pulse is applied after the display of B_2 (seventh column of tabulated information). The condition of the flip-flops is such that FF's 1 through 3 are in the 1 state and FF's 4 through 8 are in the 0 state. This condition enables the positioning plates to place either the A_4 or B_3 characters at the E6 N2 co-ordinates.

2.7.2.2 Character Counting and Positioning Circuit (TD Vector Message)

Format positioning in TD vector messages (fig. 4–61) depends only on the two sense bits of the fourth vector. For example, assume that the fourth vector of a TD vector message is in the upper left ($\dot{X}2^0$—1, $\dot{Y}2^0$—0) direction (fig. 4–58, part h). The clear pulse (fig. 4–59) following the preceding message cleared all the flip-flops. AND 1 applies a d-c level to gate 1. For the message under consideration, AND's 5 and 7 apply d-c levels to capacitor-diode gates 2 and 4, respectively. The first advance-character-position pulse from the timer is received after the fourth vector is displayed. This pulse is gated through GT 1 and capacitor-diode gates 2 and 4, setting FF's 4 and 7, respectively. The resultant output voltage positions the G_1 character to the appropriate position in the format. (Note that in fig. 4–61 the G characters can occupy only one of two vertical co-ordinates. The vertical position depends entirely on whether FF 7 is set through AND 7 and capacitor-diode gate 4. Gates 4 and 5 and capacitor-diode gates 4 and 5 are never conditioned during a TD vector message. Flip-flops 5, 6, and 8 therefore remain in the 0 state.) Once FF 4 is set to the 1 state, OR 1 applies a d-c level to GT 2. After the G_1 character is displayed, the second advance-character-position pulse is received. This pulse is gated through GT 2, complementing FF 1. The result is a positioning voltage applied to the positioning plates for the next (G_2) character. The third and fourth advance-character-position pulses similarly advance the counter for the G_3 and G_4 characters so that the appropriate positioning voltages are applied to the positioning plates. After the G_4 character is displayed, ending the TD vector message display cycle, a clear pulse resets all the flip-flops to the 0 state. This readies the character position counter for the next message. The conditions for all the flip-flops, after each advance-character-counter pulse, are tabulated in figure 4–61, which is similar to figure 4–60 for the TD tabular messages.

2.7.2.3 Character Position and Compensation Decoder and Line Drivers

The function of the character position decoders is to change digital voltages into equivalent analog voltages for use on the character-positioning plates of the SD CRT's. The decoder circuits consist of current source tubes, current gate tubes, and ladder sections. (See fig. 4–62, foldout.) The inputs to the current gate tubes are composed of flip-flop outputs from the character counter and positioning circuits. Position-correction voltages are applied to other current gate tubes in the



COORDINATES		+	E_2,N_2	E_4,N_2	E_5,N_2	E_6,N_2	$E_2,0$	$E_4,0$	$E_5,0$	$E_6,0$	E_2,S_2	E_4,S_2	E_5,S_2	E_6,S_2	
CHARACTER DISPLAYED		VECTOR	A_1	A_2 OR B_1	A_3 OR B_2	A_4 OR B_3	D_1	D_2	A_5 OR B_4	A_6 OR B_5	C_1	C_2	C_3	C_4	
FF'S	OUTPUTS		AFTER VECTOR (SET)	AFTER A_1	AFTER B_1	AFTER B_2	AFTER B_3	AFTER D_1	AFTER D_2	AFTER B_4	AFTER B_5	AFTER C_1	AFTER C_2	AFTER C_3	AFTER C_4 (CLEAR)	
1	$X2^0$	0	0	1	0	1	0	1	0	1	0	1	0	1	0
2	aX	0	1	1	1	1	1	1	1	1	1	1	1	1	0
3	$X2^1$	0	0	0	1	1	0	0	1	1	0	0	1	1	0
4	bX	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	$Y2^0$	0	0	0	0	0	1	1	1	1	0	0	0	0	0
6	cY	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	$Y2^1$	0	0	0	0	0	0	0	0	0	1	1	1	1	0
8	dY	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 4–60. Character Counting and Positioning Circuit, Conditions for a Sample TD Tabular Message

positioning decoders. These voltages originate in the character register and are the same digital voltages that are used to select a character from a display tube character-forming matrix. The voltages compensate for the off-axis displacement of the electron beam caused by character selection.

The current gate tubes are arranged to act as switching devices to produce push-pull outputs. An input to one tube results in an increase of current flow in the tube. The output current of the gate tubes is applied to ladder sections, resulting in the generation of ±X-position and ±Y-position analog voltages. The voltages are applied to the CRT positioning plates via the vector generator and character position line drivers.

2.7.2.4 Vector Generator and Character Position Line Drivers

The vector generating voltages (see 2.8.1 of this section) and the character positioning and compensating voltages are supplied to the same sets of plates in over 70 display tubes. These voltages are combined in line drivers which provide the required power amplification needed for the deflection sensitivity of the SD tubes. Vector generator and character position line drivers are used for the analog output voltage of the vector generator and the character position decoders.

2.8 VECTOR GENERATION

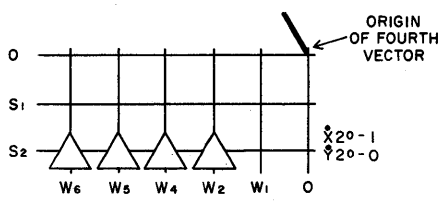
The vectors in TD vector messages and in TD tabular messages are generated by the vector register and vector generator circuits. The vector register consists of flip-flops, with associated input gates, which hold the digital values representing the direction (sense) and magnitude of the $\dot{X}$ and $\dot{Y}$ components of one vector. The output of the register is connected to the vector generator. The output of the vector generator is applied to the deflection plates of the SD CRT's (through the vector generator and character position line drivers discussed in paragraph 2.7.2.4). The following discussion pertains to the vector register $\dot{X}$ flip-flops (fig. 4–63) and the vector register $\dot{Y}$ flip-flops (fig. 4–64). The figures are similar.

2.8.1 Vector Register (TD Tabular Track Message)

The $\dot{X}$, $\dot{Y}$ digital information for the single vector in a TD tabular message is applied to the vector register by 14 lines from the input gates section. The vector register is conditioned to receive the information by a read-vector (tabular message) signal from the gate generator in the SD timing and control section. A clear pulse from the SD timing and control section is applied to the vector register after the vector is displayed.

The $\dot{X}$ and $\dot{Y}$ digital voltages for the vector in a TD tabular message are connected from the input gates section to capacitor-diode gates 7 through 13. The information is received by the capacitor-diode gates as pulses.

The LS and RS bits in word 5 ($\dot{X}2^0$, $\dot{Y}2^0$) are the vector sense bits. They determine the quadrant of the



COORDINATE POINTS			W_6,S_2	W_5,S_2	W_4,S_2	W_2,S_2	
CHARACTER DISPLAYED		4TH VECTOR	G_1	G_2	G_3	G_4	
FF'S	OUTPUTS		AFTER 4TH VECTOR (SET)	AFTER G_1	AFTER G_2	AFTER G_3	AFTER G_4 (CLEAR)
1	$X2^0$	0	0	1	0	1	0
2	aX	0	0	0	0	0	0
3	$X2^1$	0	0	0	1	1	0
4	bX	0	1	1	1	1	0
5	$Y2^0$	0	0	0	0	0	0
6	cY	0	0	0	0	0	0
7	$Y2^1$	0	1	1	1	1	0
8	dY	0	0	0	0	0	0

Figure 4–61. Character Counting and Positioning Circuit, Conditions for a Sample TD Vector Message

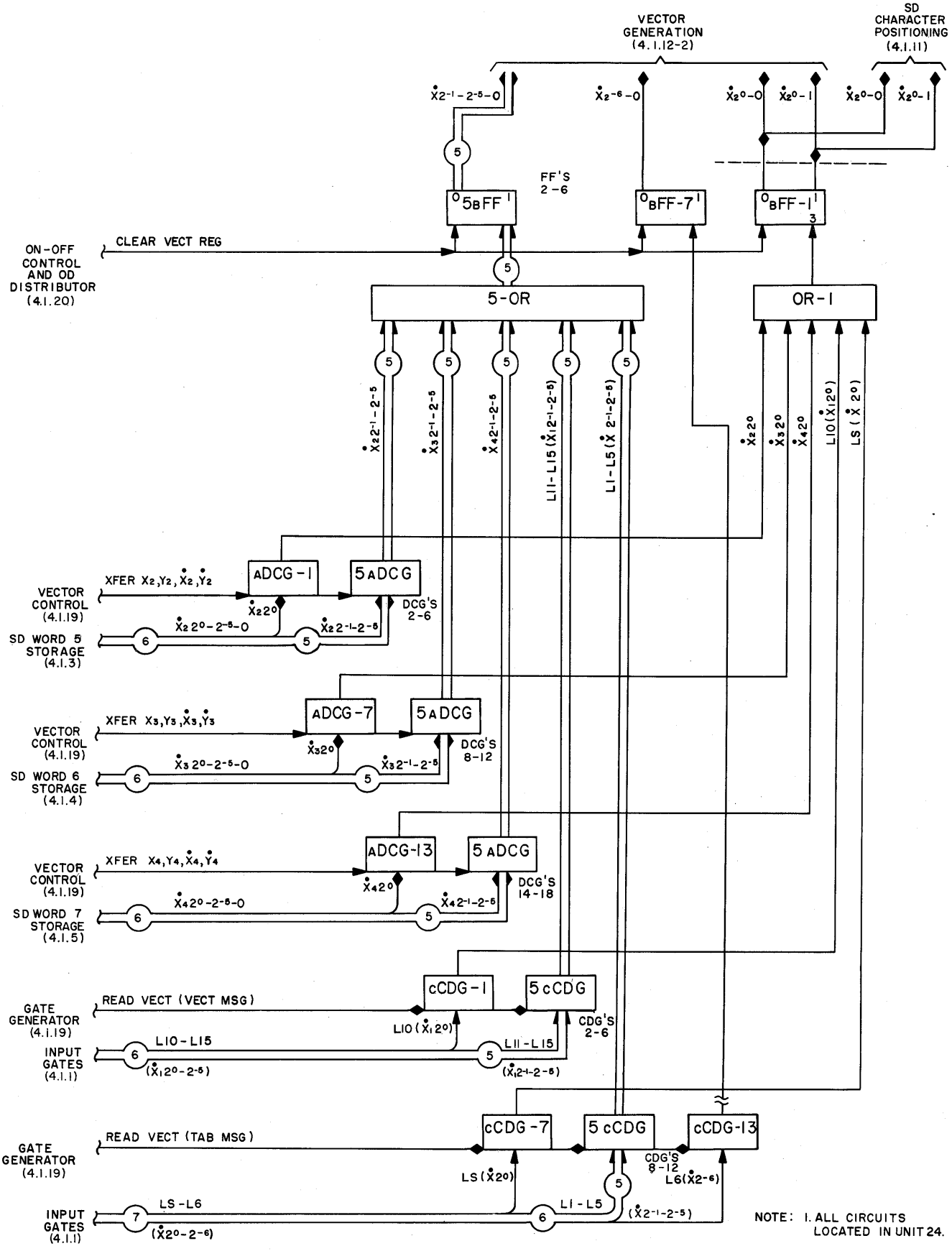


Figure 4-63. Vector Register X Flip-Flops Circuit, Logic Diagram

vector direction. The four possible combinations of $\dot{X}2^0$ and $\dot{Y}2^0$ bits for a vector are 00, 01, 11, and 10. Each combination selects a different quadrant. The northeast quadrant is represented by 00, southeast by 01, southwest by 11, and northwest by 10. The $\dot{X}2^0$ and $\dot{Y}2^0$ combinations are OR'ed to FF 1 and then applied to the character counter and positioning circuit (for character positioning purposes) and to the vector generator. The remaining $\dot{X}$ and $\dot{Y}$ bits of the vector determine the vector magnitude in the selected quadrant. The digital voltage values are OR'ed and applied to the 1 sides of FF's 2 through 7. The outputs of these flip-flops are applied to the vector generator.

2.8.2 Vector Register (TD Vector Message)

The $\dot{X}$, $\dot{Y}$ digital information for the first vector in a TD vector message (word 1) is applied to the vector register by 12 lines from the input gates section to capacitor-diode gates 1 through 6. The vector register is conditioned to receive this information by a read-vector (vector message) signal from the gate generator in the SD timing and control section. The $\dot{X}$, $\dot{Y}$ information for the second, third, and fourth vectors is transferred to the vector register from the word storage section by three transfer pulses that originate in the vector control circuit of the SD timing and control section. A clear pulse from the latter section is applied to the vector register after each vector is displayed.

The $\dot{X}$ and $\dot{Y}$ components of the vectors in a TD vector message each contain only six bits ($\dot{X}2^{-6}$, $\dot{Y}2^{-6}$ outputs always 0) compared to the seven bits for the single vector of a TD message. This is done because the four vectors, being used for geographical descriptions, etc., require less precision than the single vector of a TD tabular message (which might represent aircraft speed).

The $\dot{X}$ and $\dot{Y}$ voltages for the second vector in a vector message are received by capacitor-diode gates 1 through 6 from word 5 storage. The $\dot{X}$ and $\dot{Y}$ voltages for the third vector are received by capacitor-diode gates 7 through 12 from word 6 storage. For the fourth vector in a vector message, the $\dot{X}$ and $\dot{Y}$ voltages are received by capacitor-diode gates 13 through 18 from word 7 storage. The $\dot{X}$ and $\dot{Y}$ voltages for the second, third, and fourth vectors in a vector message are received by the capacitor-diode gates as voltage levels, and are gated by transfer -X, Y, $\dot{X}$, $\dot{Y}$ pulses (the same pulses simultaneously transfer the corresponding XY information into the vector register) from the vector control.

The information for the second, third, and fourth vectors of a vector message is taken from the 0 side of the flip-flops in the word storage section. The diode-capacitor gates invert all signals from the word storage. In this manner, the 1 levels of the word storage flip-flops are simulated for the vector register, and the number in the register will be the same as the number in storage.

2.8.3 Vector Generator

The vector generator receives the digital information from the vector register on 16 lines. The magnitude information of each vector component is applied to the vector generator on 12 of the 16 lines. The 12 lines carry the $\dot{X}2^{-1}$—2^{-6} and $\dot{Y}2^{-1}$—2^{-6} information. The flip-flops in the register containing sense bits $X2^0 = 0$ or $\dot{X}2^0 = 1$, and $\dot{Y}2^0 = 0$ or $\dot{Y}2^0 = 1$ for each vector are connected to the vector generator by four of the 16 lines. In the vector generator, the 1 and 0 combinations of the $X2^0$ and $Y2^0$ flip-flops determine the quadrant direction of the vector. The analog output voltage of the generator is applied to the positioning plates of the display tube through the vector generator and character position line drivers.

The vector-off signal from the timer must be suppressed to permit vector generation. This occurs for each vector of a TD vector message and for the vector in a TD tabular track message.

The vector generator develops the analog voltage for determining the direction and length of each vector by decoding the $\dot{X}$ and $\dot{Y}$ digital information received from the vector register. The analog output voltage is then applied to the display tube positioning plates through the vector generator and character position line drivers.

Figure 4–65, foldout, is a logic diagram of the vector generator. The $\dot{X}$ and $\dot{Y}$ digital information is applied to decoder stages. Each stage consists of three current gate tubes supplied by a single current source tube. Two of the current gate tubes in a decoder stage work in ladder sections, which are portions of register ladder networks. The third current gate tube regulates the amount of current available from the common current source tube to the current gate tubes feeding the ladder sections. The G symbols in the figure denote the final ladder sections, which are adjustable gain controls. The analog output voltage of the decoders is developed across the resistors in the ladder sections and is proportional to the digital value of input voltages. A voltage regulator (R) maintains a constant supply of current from the current source tubes. Current is supplied to the current gate tubes only during the time that a sweep signal is raised in the sweep generator. This requires the suppression of the vector-off signal connected from the timer in the SD timing and control section.

The $\dot{X}2^0$ and $\dot{Y}2^0$ bits of a vector determine the quadrant in which the vector is to appear. The bits perform this action by biasing the current gate tubes feeding the ladder sections. A $\dot{Y}2^0$—1 signal is connected from the vector register to the current gate tubes producing

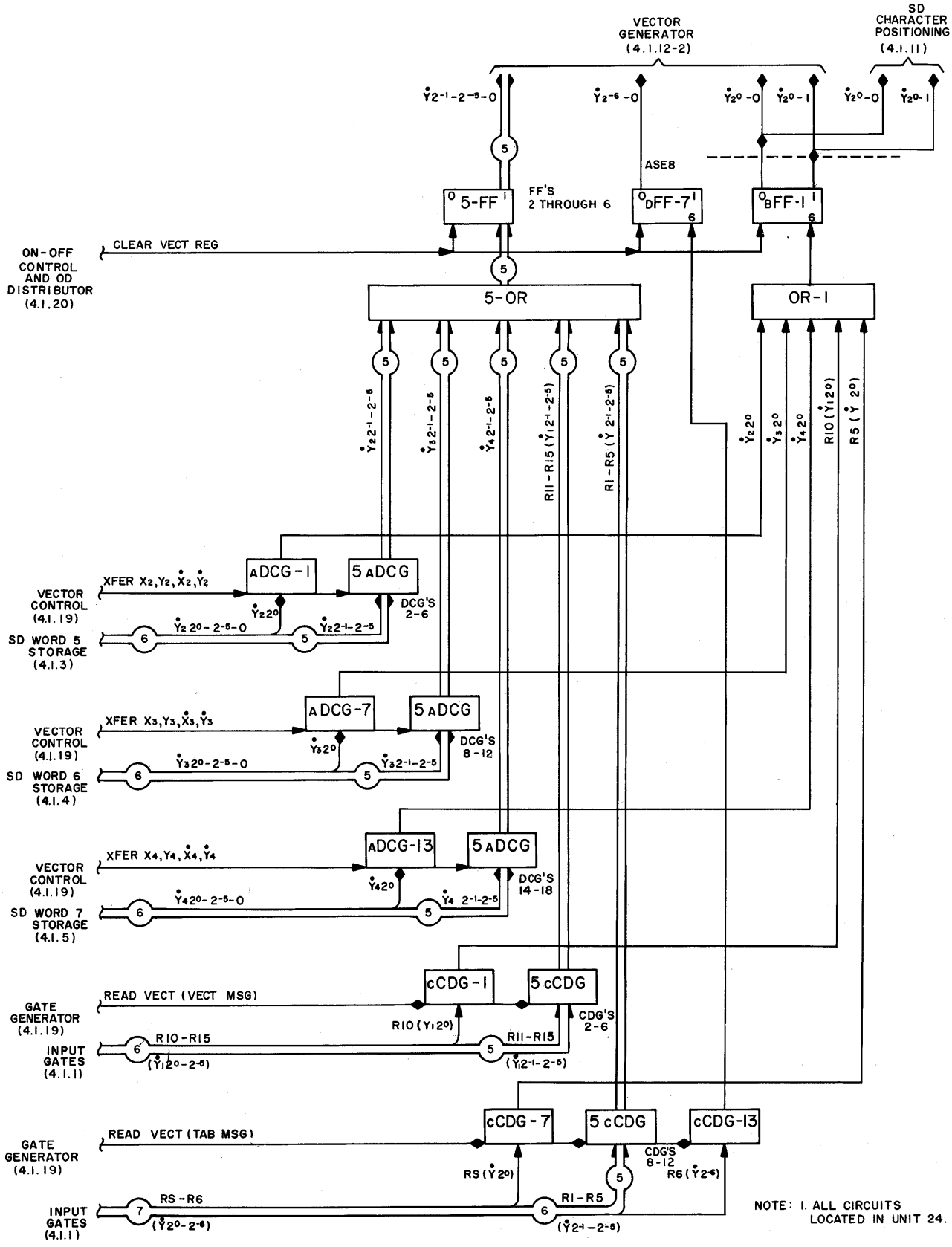


Figure 4–64. Vector Register Y Flip-Flops Circuit, Logic Diagram

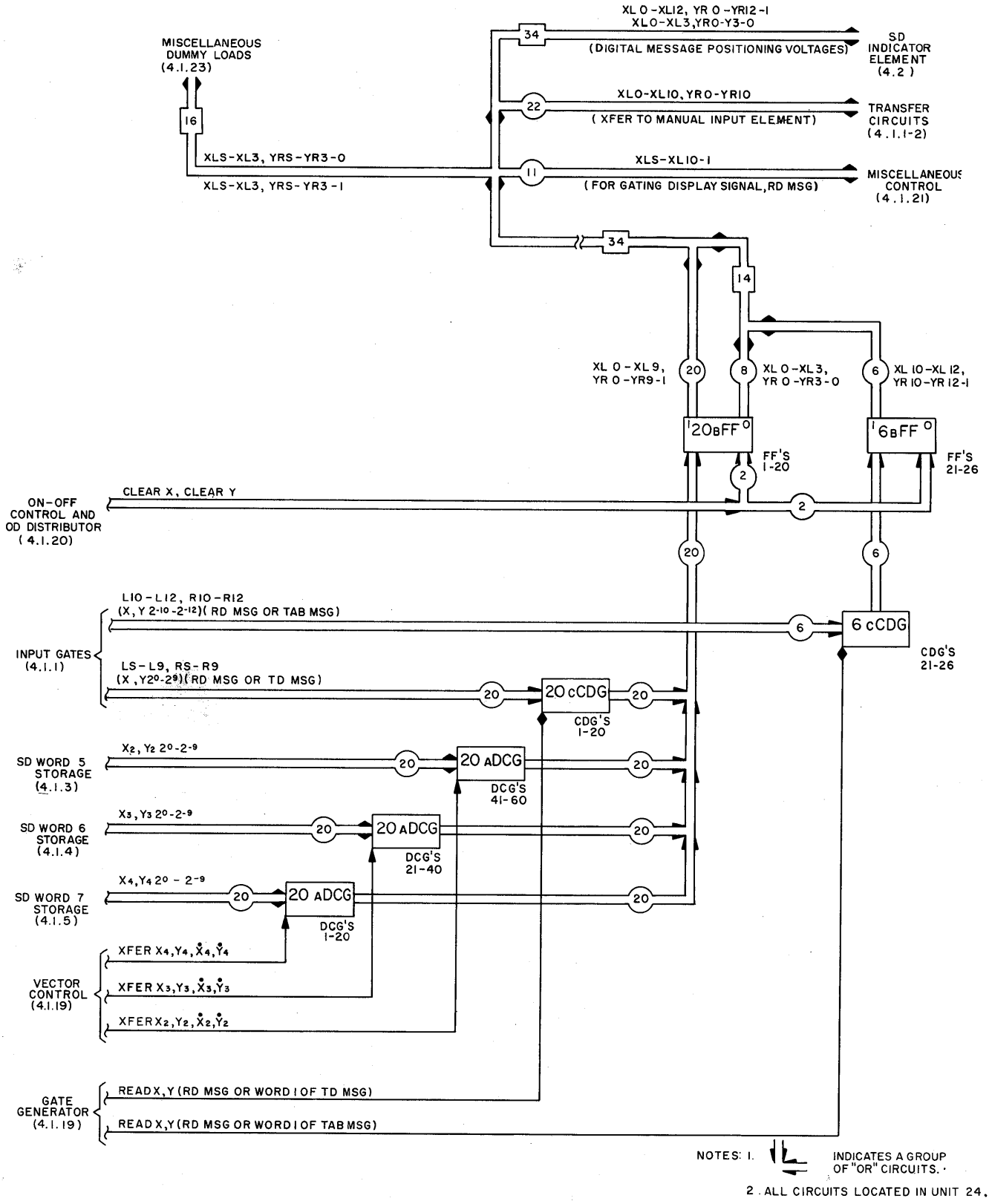


Figure 4–66. SD Word 1 Storage (XY Register) and XY Line Drivers Circuit, Logic Diagram

the +Y analog output voltage; a $Y2^0$—0 signal is connected to the current gate tubes producing the —Y analog output voltage. In a similar manner, the 1 and 0 values of $X2^0$ are connected to the current gate tubes producing the +X and —X analog output voltages. Either the current gate tubes delivering the +Y analog output or the current gate tubes delivering —Y analog output will be biased, depending on whether $Y2^0$ is a 0 or a 1. Bit $X2^0$ biases the X current gate tubes similarly.

Bits $X2^{-1}$—$X2^{-6}$ and $Y2^{-1}$—$Y2^{-6}$ determine the magnitude and sense of the vector within a quadrant and are applied from the vector register to the current gate tubes not biased by the sense bits (the control gate tubes). The magnitude of X, Y analog outputs is determined by the biasing action of the X and Y magnitude bits when the bits are 1's. This permits more current to pass from the common current source to the current gate tubes allowed to conduct by the $Y2^0$ and $X2^0$ bits.

The operation of the vector generator can be understood more clearly by the use of an example. Consider only the Y half of the generator. If the $Y2^0$ bit of the number in the vector register is a 1, the 1 side of the $Y2^0$ flip-flop in the register (fig. 4–64) is up and +10V is applied to the current gate tubes producing the +Y analog output. The 0 side of the flip-flop applies a bias of —30V to the current gate tubes producing the —Y analog output. Under the conditions described, the tubes producing the +Y analog output will conduct much more of the current from the current source tubes than the tubes producing the —Y analog output. The negative shift of the +Y analog voltage output will therefore be greater than the negative shift of the —Y analog voltage output. Bits $Y2^{-1}$ to $Y2^{-6}$ are connected from the 0 side of the register flip-flops to the central current gate tubes and act as bias voltages to these stages. Assuming that the register flip-flops have just cleared, positive voltages are applied to the central gate tubes. This allows them to conduct heavily and reduce the amount available to the tubes producing the +Y analog output. As bits $Y1^{-1}$ to $Y2^{-6}$ set various flip-flops in the register to 1, the $Y2^{-1}$ to $Y2^{-6}$ lines apply negative voltages to the corresponding central current gate tubes, causing them to draw less current. As a result, the tubes producing the +Y analog output will conduct more and will cause greater +Y analog voltage in the negative direction to appear on the deflection plates of the display tubes.

The X half of the vector generator operates in the same manner as the Y half just described. The X analog voltages affect the horizontal positioning of the electron beam, whereas the Y voltages have a vertical influence on the beam. The vectorial resultant of the X and Y voltages on the deflection plates determines the sense and magnitude of the vector. The vector is actually produced on the face of a display tube by the action of the X and Y analog voltages in deflecting the point character from the X and Y position determined by the deflection yoke. The deflection of the point character leaves a trace of light on the screen presenting the vector.

2.9 MESSAGE POSITIONING (XY REGISTER SD WORD 1 AND STORAGE XY LINE DRIVERS LOGIC)

The XY register and line drivers circuit is a register of 26 flip-flops that hold digital X, Y information of SD messages while the information is decoded to analog voltages in the SDIE. The X, Y analog voltages are used by the deflection yokes of the SD CRT's for message positioning. The X and Y information locates the E character and point positions and the point of vector origin in TD tabular messages, the origin of the four vectors in vector messages, and the position of RD messages. Figure 4–66 is a logic diagram of the XY register and line drivers circuit.

The 26 flip-flops of the XY register are cleared by the clear -X and clear -Y signals at the end of every RD and TD tabular message and at the end of the first three vectors of a TD vector message. This action prepares the flip-flops to receive new X, Y information.

2.9.1 TD Tabular Message

The X, Y bits of word 1 in a tabular message (LS-L12, RS-R12) contain the central position (E character and point positions and vector origin) in the display of the message. The bits are applied directly from the input gates section to the XY register. Bits LS-L9, RS-R9 sense capacitor-diode gates 1 through 20 which are conditioned by a read -X, Y (TD message) signal from the gate generator. The other six X, Y bits of word 1 in a tabular message (L10-L12, R10-R12) sense capacitor-diode gates 21 through 26, which are conditioned by a read X,Y (tabular message) signal, also from the gate generator. The two conditioning signals required for the admittance of tabular message digital X,Y information are applied simultaneously (when the symbol sequencer is 1) to the capacitor-diode gates, thereby admitting bits LS-L9 and RS-R9 to the 1 sides of FF's 1 through 20, and bits L10-L12 and R10-R12 to the 1 sides of FF's 21 through 26.

The 1 and 0 outputs of the flip-flops for bits LS-L3 and RS-R3 (XLS-XL3, YRS-YR3) are connected through individual cathode followers (16 in all) to the decoder and/or expansion circuits of the SD consoles. The outputs of these cathode followers are also connected, through relay contacts, to dummy loads when the SDGE is being used as a standby generator.

Only the 1 side output of the flip-flops for bits L4-L12 and R4-R12 (XL4-XL12, YR4-YR12) are connected through individual cathode followers (18 in all) to the decoder circuit in the SD consoles.

2.9.2 TD Vector Message

The X and Y (vector origin) information for the first, second, third and fourth vectors of a TD vector message is contained in bits LS-L9, RS-R9 of words 1, 5, 6, and 7. The information in words 5, 6, and 7 is consecutively gated from word storage into the XY register at the appropriate times.

The X, Y information for vector 1 (bits LS-L9, RS-R9 of word 1) is applied directly from the input gates section to capacitor-diode gates 1 through 20. These gates are conditioned, at the time that word 1 is read from the TD drum, by the read -X, Y (TD messages) signal from the gate generator. The gated output is applied to the 1 sides of FF's 1 through 20. Bits L10-L12 and R10-R12 of word 1 of a vector message are also applied to capacitor-diode gates 21 through 26, but a conditioning read X,Y signal is not applied to these gates for a TD vector message. After the first vector is displayed, the register is cleared by the clear-X and clear-Y signals.

The X, Y information for vectors 2, 3, and 4 of a vector message is contained in words 5, 6, and 7, bits LS-L9 and RS-R9. These bits are initially stored in word storages 5, 6, and 7. The X, Y signals are applied to capacitor-diode gates, groups 1 through 20, 21 through 40, and 41 through 60, in the XY register. The X, Y signals for the vectors of words 5, 6, and 7 are gated into the register. The register is cleared after the first, second, and third vectors are displayed; the final message will clear the register of the fourth vector. When transferring one of the X, Y bits from a word storage section flip-flop, the corresponding X or Y flip-flop in the XY register must become a 1 if the storage flip-flop is a 1 or a 0 if the storage flip-flop is a 0. However, the 0 side of the word storage section flip-flops are connected (through capacitor-diode gates) into the 1 sides of the register flip-flops. The correct correspondence between the number in storage and in the register is restored in the following manner. Assume that bit LS of word 5 ($X_2 2^0$) is a 1. The flip-flop holding the bit in word 5 storage has an output of —30V from its 0 side. This output conditions a capacitor-diode gate in the XY register; when the gate is sensed by the transfer X_2, Y_2, $\dot{X}_2$, $\dot{Y}_2$ signal, the 1 side of the register flip-flop connected to bit LS in storage is raised. The 1 in the storage flip-flop is thus successfully reproduced in the register flip-flop. All other 0 side flip-flop outputs through capacitor-diode gates operate in the same manner.

The same outputs from the X,Y register flip-flops to the display consoles occur for TD vector messages as for TD tabular messages.

2.9.3 RD Message

Radar data message bits LS-L10 and RS-R10 contain X and Y position information of a radar return. Bits LS-L10 and RS-R10 are carried from the input gates section on the same lines as the corresponding bits of a TD message. Bits LS-L9 and RS-R9 sense capacitor-diode gates 1 through 20; bits L10 and R10 sense two of the groups of six capacitor-diodes gates, 21 through 26. Both of these gate groups are conditioned by read X, Y (RD message) signals from the gate generator which allow the passage of the bits from the input gates section to the XY register. In addition to being sent to the consoles and dummy loads section in the same manner as TD tabular and TD vector message XL and YR signals, the XLS-XL10-1 signals are sent to the miscellaneous control circuit. They control the suppression of intensification for blank registers. The XLS-XL10-1 and YRS-YR10-1 signals are also sent to the transfer circuits section for re-entry into the Central Computer System through the MI element. (Bits L14 and L15, the remaining bits in an RD message, are the category control bits. These bits are connected directly from the input gates section to the SD timing and control section.)

2.10 CATEGORY AND DAB STORAGE AND OUTPUT

Figure 4–43 is a diagram of the CAT and DAB storage and output section, in which CAT and DAB signals are developed. The following logical analysis was written in terms of the diagram. For the purposes of this section, it is not necessary to consider TD tabular and TD vector messages separately. RD messages are handled by two circuits within the section independently of TD messages (2.10.10 and 2.10.11 of this section). Contained within this section of the SDGE are the following circuits: category storage, matrix, and drivers; DAB word 2 storage; DAB word 3 storage; DAB word 4 storage; DAB drivers; supplementary drivers; RD category drivers and mixed RD category drivers.

All of the flip-flops in the storage registers are cleared, before the start of each message display cycle, by clear pulses from the on-off control and OD distributor.

Words 2, 3, and 4 are admitted at 10-μsec intervals, along the same 32 lines, to the CAT and DAB storage and output section. Bits LS-L4 of word 2 sense gates in the category storage circuit; bits L5-L15 and RS-R15 sense gates in DAB word 2 storage; and bits LS-L15 of word 2 and RS-R15 of words 3 and 4 sense gates in DAB word 3 and DAB word 4 storage. The sensing of admittance gates in all these storage circuits for each word is admitted to the SDGE by the input gates section. However, each storage circuit requires a condi-

tioning level for the bits to be gated. These conditioning levels, called read-word 2, read-word 3, and read-word 4 signals, originate in the gate generator. Each level is coincident with the appearance of only one word from the input gates section. For example, at the time that word 2 appears, a read-word 2 signal is applied only to the category storage and DAB word 2 storage distribution gates. In the same manner, when word 3 appears, a read-word 3 signal is applied only to distribution gates for DAB word 3 storage, and when word 4 appears, the read-word 4 signal is applied only to DAB word 4 storage.

The category storage, matrix, and drivers circuit produces the 31 TD category signals. Only one of these signals can be developed for each TD message, and each is a result of a different binary combination of 1's and 0's contained in bits LS-L4 of word 2. TD category signals are applied directly to the consoles of the SDIE, which have been wired for those categories. Some are applied as well to the supplementary drivers for mixing or amplification. All TD categories (except TD category 1, the test category) are mixed in the mix-all-CAT's and mix-all-DAB's subsection circuit to provide the mix-all-cat's signal.

The remainder of word 2 (L5 through L15 and RS through R15) is gated into DAB word 2 storage. The gates in DAB word 2 storage which admit these bits are conditioned by the read-word 2 signal. Bit L5, when it is a 1, produces a display signal which is sent to the miscellaneous control. If this signal is not present, the message of which it is a part cannot be displayed. Bits L6-L15 and RS-R15 are display assignment bits. Any bit that contains a 1 will develop a DAB signal. The DAB lines, which are generally up, indicate to the consoles with which they are permanently associated that the message being generated in the SDGE must be displayed on those consoles.

All 32 bits of word 3 are gated into DAB word 3 storage at the time the read-word 3 signal is applied; the 32 bits of word 4 are gated into DAB word 4 storage coincident with the application of the read-word 4 signal. Each of the bits in these words that contain a 1 develops a DAB signal.

The 90 DAB signals are amplified in the DAB drivers circuit and applied to the SDIE and to the mix-all-CAT's and mix-all-DAB's subsection. In the latter they are mixed to provide the mix-all-DAB's signal.

The outputs of the CAT and DAB storage and output section are applied to the SDIE. These outputs are switched to dummy loads when the dummy load section is energized.

2.10.1 Category Storage, Matrix and Drivers (TD Messages Only)

Word 2 of a TD message contains five coded category bits (LS through L4) which identify the type of tactical information contained in words 0, 1, 5, 6, and 7 of the same message. The category storage and matrix decodes these five bits into one of 32 category signals. Figure 4–67 is a diagram of this circuit.

Flip-flops 1 through 5 are cleared by a clear pulse from the on-off control and OD distributor. The clear pulse is applied at the conclusion of the previous message.

Bits LS-L4 from the input gates section are each applied to one of the capacitor-diode gates associated with FF's 1 through 5. Coincident with the receipt of these bits when they are part of word 2, a read-word 2 conditioning signal from the gate generator is applied to the five gates. The bits which contain 1's (contain a pulse) are gated to the 1 side of the flip-flops with which they are permanently associated (FF's 1 through 5).

2.10.2 TD Category Generation

There are 32 possible combinations of the five category bits. The combinations range, in binary value, from 00000 to 11111. (A message is assigned to the 00000 category only if it is to be routed to SDIS's by means of DAB's.) A signal voltage level is generated for each category and is connected to category selection switches on various consoles. TD category 1 is assigned to the drum test pattern for the SD tubes, and its signal level, therefore, is connected to the TEST-OPERATE switch on the consoles.

The decimal equivalent of the binary value assigned to a message by the Central Computer System is shown in figure 4–67 as the decoded output of one of the AND 13 through 43 circuits. For example, when the contents of bits LS through L4 are 00001, the TD-category 1 signal is developed as the output of AND 27; when the contents of the category bits are 00010, the TD-category 2 signal is developed as the output of AND 26. The AND circuits develop outputs in the following manner.

Bits LS-L4 represent binary magnitudes 2^4-2^0. Bit 2^4 is stored in FF 1; 2^3, in FF 2; 2^2, in FF 3; 2^1, in FF 4; and 2^0, in FF 5.

All possible combinations of 2^1 and 2^0 (00, 01, 10, and 11) are AND'ed in AND circuits 9 through 12. Each of the four AND circuits develops an output for only one of these combinations. The binary numbers next to AND circuits 9 through 12 (fig. 4–67) indicate what the contents of bits L3 and L4 (and thus the status of FF's 4 and 5) must be for each AND circuit to develop an output.

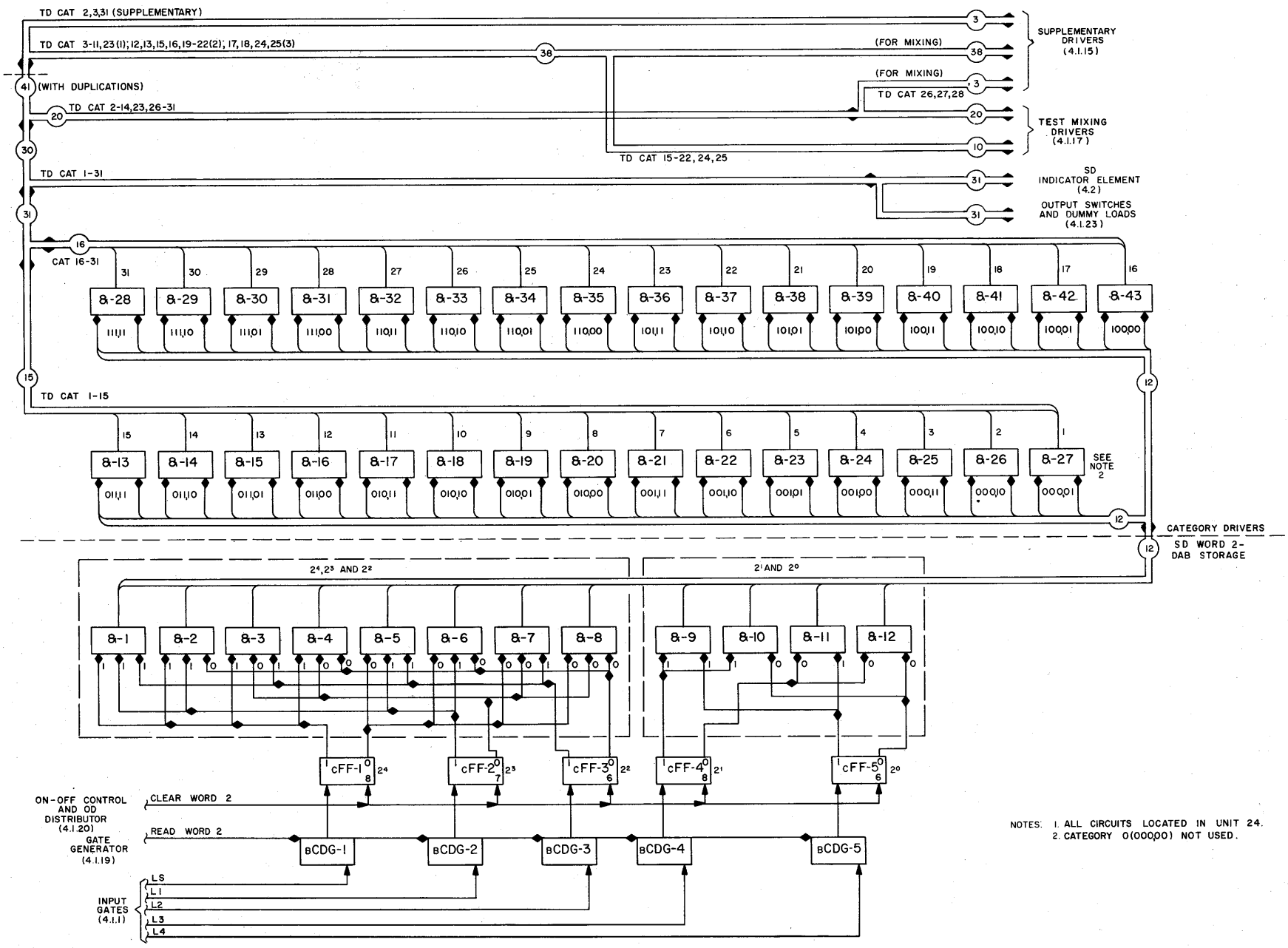


Figure 4–67. SD Word 2 DAB Storage and Drivers Circuit, Logic Diagram

All possible combinations of 2^4, 2^3, and 2^2 (000, 001, 010, 011, 100, 101, 110, and 111) are AND'ed in AND circuits 1 through 8. Each of these AND circuits develops a signal representative of only one combination of bits LS, L1, and L2. The binary numbers next to AND circuits 1 through 8 indicate what the contents of these three bits (and thus the status of FF's 1 through 3) must be for each AND circuit to develop an output.

Each TD message causes a single d-c level signal to be developed from one of AND circuits 1 through 8 (representing the binary value of 2^4, 2^3, and 2^2), and a single d-c level from one of AND circuits 9 through 12 (representing the binary value of 2^1 and 2^0). The two signals (representing the binary value of 2^0 through 2^4) are applied to one of AND circuits 13 through 43; the AND circuit output then corresponds uniquely to the binary category number in a TD message.

As an example of TD category signal formation, consider the development of the category 1 signal. Bits LS through L4 of a message in TD category 1 are 00001. They are gated to the 1 side of FF's 1 through 5. Bit L4 is the only bit which contains a pulse; therefore, FF 5 is the only one that is set. Thus, the overall contents of FF's 1 through 3 are 000; and flip-flops 4 and 5, 01. The three 0 side outputs of FF's 1 through 3 are AND'ed in AND circuit 8 to develop a d-c level output, and the 0 side output of FF 4 with the 1 side output of FF 5 are AND'ed in AND circuit 11 to develop another d-c level output. These two d-c level signals, representing a 00001 combination of bits LS-L4, are applied to AND circuit 27, which produces a single output. This output is the TD category 1 signal. TD category signals 2 through 31 are produced in a similar manner by ANDing the outputs of the five storage flip-flops in various other combinations. Table 4–11 lists the 32 possible input combinations of the five category bits, the AND circuits in which their outputs are combined, and the TD category signal (in decimal notation) produced by each input combination of bits.

2.10.3 TD Category Output Signals

The 31 TD category signals are applied to the SDIE and are also routed to dummy loads when the SDGE is a standby. TD category signals 2, 3, and 31 are applied to the supplementary drivers circuit for amplification, and 19 category signals are applied to the same circuit for mixing. TD category signals 2 through 31 are also applied to the mix-all-CAT's and mix-all-DAB's circuit.

2.10.4 DAB Word 2 Storage Circuit (TD Messages Only)

This circuit converts the 26 DAB's of word 2 from pulse form to d-c level DAB signals. It also develops the display signal required for each TD message from one of the bits in word 2. These signals are stored by this circuit for the duration of a TD message. Figure 4–68 is a diagram of DAB word 2 storage.

Flip-flops 1 through 27 are cleared before the start of each TD message display cycle by clear pulses from the on-off control and OD distributor. Bits L5-L15 and RS-R15 are admitted, by the input gates section, to 27 capacitor-diode gates. They are applied to these gates for every word that is read into the SDGE. However, the bits are gated to the 1 side of flip-flops only when a read-word 2 conditioning signal from the gate generator is applied.

Bit L5 pulses the 1 side of the display-bit flip-flop. When the bit is a 1, a display signal is developed on the 1 side of that flip-flop and sent to the miscellaneous control.

DAB signals are developed by the 1 bits of bits L6-L15 and RS-R15. The 26 0-side outputs of the flip-flops pulsed by these bits are the word 2 DAB signals. The DAB 1 through 26 signals are applied to the DAB drivers where they are inverted. DAB 1, 2, 8, 9, and 10 signals from the 1 side of the corresponding flip-flops are also applied to the supplementary drivers.

2.10.5 DAB Word 3 Storage Circuit (TD Messages Only)

The 32 DAB's of word 3 are converted from pulses to d-c levels from DAB signals by this circuit and are

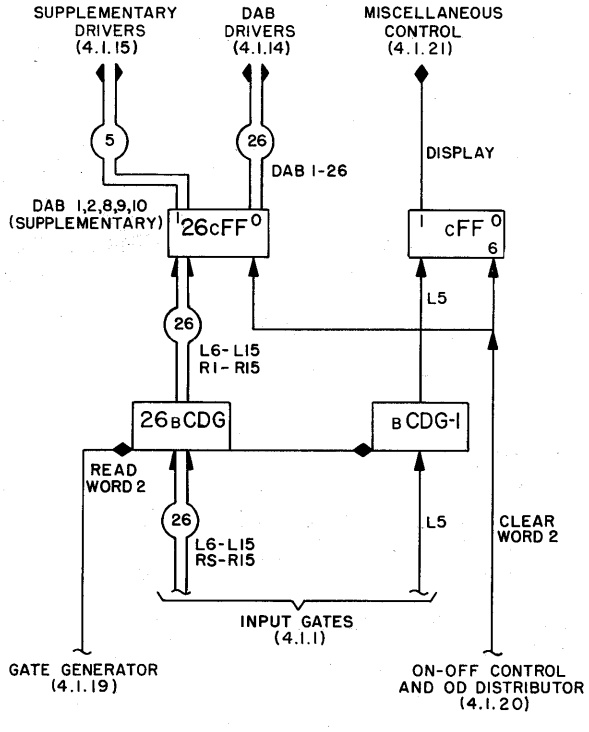


Figure 4–68. SD Word 2 DAB Storage Circuit, Logic Diagram

stored in 32 flip-flops for the duration of a TD message. Figure 4–69 is a diagram of DAB word 3 storage.

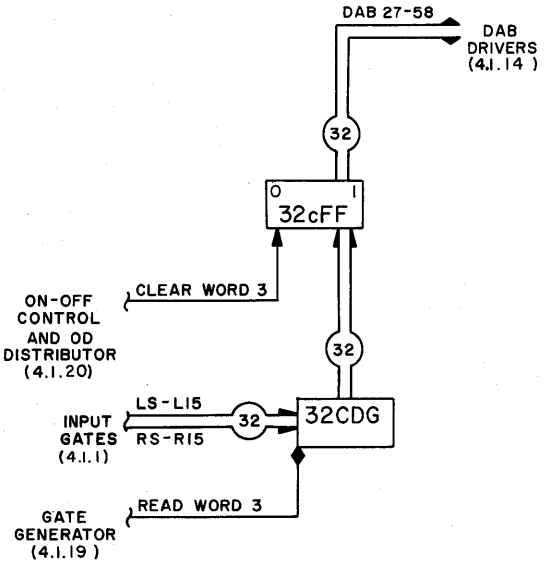
All flip-flops are cleared before the start of each TD message display cycle by clear pulses from the on-off control and OD distributor. Word 3, consisting of bits LS-L15 and RS-R15, is applied to DAB word 3 storage through the input gates. The 32 capacitor-diode gates are sensed by the bits of word 3 as well as those of the other seven words of a TD message. However, the gate generator provides the conditioning signal (read-word 3) for these gates only with the occurrence of word 3 from the Drum System. At that time, the 32 bits are gated to the 1 sides of the flip-flops.

DAB signals are developed on the 0 side of the flip-flops into which a 1 (indicated by the presence of a pulse in those bit positions) is gated. Display assignment bit signals 27-58 are developed by the 32 flip-flops. They are applied to the DAB drivers where they are inverted.

2.10.6 DAB Word 4 Storage Circuit (TD Messages Only)

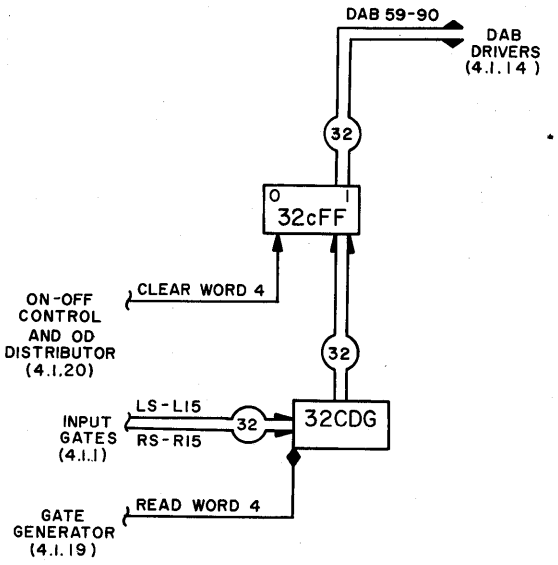
Word 4 consists of 32 DAB's. These DAB's are converted to d-c levels (DAB signals) and are stored for the duration of a TD message in DAB word 4 storage. Figure 4–70 is a diagram of this circuit.

Clear pulses from the on-off control and OD distributor clear the 32 flip-flops before a TD message cycle begins. Bits LS-L15 and RS-R15 of all words are applied to 32 capacitor-diode gates from the input gates



NOTE: ALL CIRCUITS LOCATED IN UNIT 24

Figure 4–69. SD Word 3 DAB Storage Circuit, Logic Diagram



NOTE: ALL CIRCUITS LOCATED IN UNIT 24

Figure 4–70. SD Word 4 DAB Storage Circuit, Logic Diagram

section. When these bits of word 4 occur, a read-word 4 conditioning signal from the gate generator conditions the 32 capacitor-diode gates, thereby gating the 32 bits to the 1 sides of the flip-flops.

The flip-flops into which 1's are gated are down on the 0 side. The DAB 59-90 signals which are thus produced are applied to the DAB drivers where they are inverted.

2.10.7 DAB Drivers

The DAB drivers, one for each DAB 1-90 signal, amplify and invert the signals and apply them to the SDIE and to the mix-all-CAT's and mix-all-DAB's circuit (fig. 4–71).

2.10.8 Supplementary Drivers

The supplementary drivers circuit contains mixing (OR) and amplifying circuits. DAB 1, 2, 8, 9, and 10 signals from DAB word 2 storage are amplified without mixing (supplementary drivers 32, 33, 37, 38, and 39). TD category 2, 3, and 31 signals from the category storage matrix and drivers are also amplified without mixing (supplementary drivers 43, 44, and 45). As indicated in table 4–9, various TD category signals are mixed in OR circuits. (Note that the inputs for supplementary driver signals 15 and 24 include mixed category signals.) The 10 remaining supplementary drivers are spares. Figure 4–72 is a diagram of the supplementary drivers circuit. The outputs of the supplementary drivers are applied to the SDIE.

TABLE 4–11. GENERATION OF TD CATEGORY SIGNALS

CONTENTS OF BITS LS-L2	CONTENTS OF BITS L3, L4	AND CIRCUITS DEVELOPING OUTPUTS	TD CATEGORY SIGNAL PRODUCED
000	00	8 and 12	None
000	01	8, 11, and 27	1
000	10	8, 10, and 26	2
000	11	8, 9, and 25	3
001	00	7, 12, and 24	4
001	01	7, 11, and 23	5
001	10	7, 10, and 22	6
001	11	7, 9, and 21	7
010	00	6, 12, and 20	8
010	01	6, 11, and 19	9
010	10	6, 10, and 18	10
010	11	6, 9, and 17	11
011	00	5, 12, and 16	12
011	01	5, 11, and 15	13
011	10	5, 10, and 14	14
011	11	5, 9, and 13	15
100	00	4, 12, and 43	16
100	01	4, 11, and 42	17
100	10	4, 10, and 41	18
100	11	4, 9, and 40	19
101	00	3, 12, and 39	20
101	01	3, 11, and 38	21
101	10	3, 10, and 37	22
101	11	3, 9, and 36	23
110	00	2, 12, and 35	24
110	01	2, 11, and 34	25
110	10	2, 10, and 33	26
110	11	2, 9, and 32	27
111	00	1, 12, and 31	28
111	01	1, 11, and 30	29
111	10	1, 10, and 29	30
111	11	1, 9, and 28	31

2.10.9 Mix All CAT's and Mix All DAB's

The mix-all-CAT's and mix-all-DAB's circuit (fig. 4–73) provides two output signals to the SDIE.

The 90 DAB signals from the DAB drivers circuit are mixed in OR and power cathode follower circuits. The single resulting signal is the mix-all DAB's signal. TD categories 2-31, from the category storage, matrix, and drivers, are mixed in a similar fashion. The mix-all-CAT signal is the result.

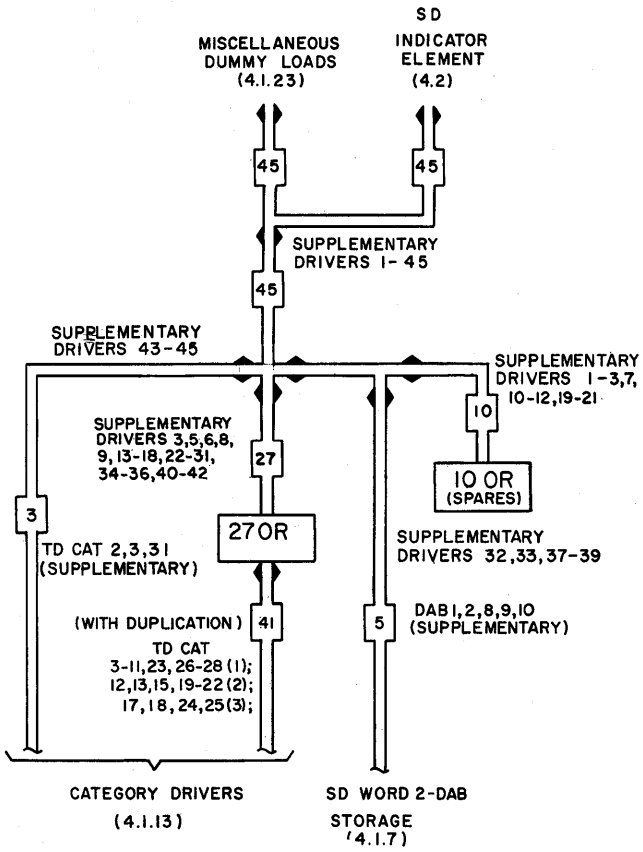
2.10.10 Radar Data Category Drivers (RD Messages Only)

Radar data messages belong to one of eight categories, according to the type of information contained in the message. Each type of message is displayed only on the consoles which require the display of the type of information contained in it. This is effected by generating one of eight RD category signals for every RD message. The signal is then used to gate the intensification circuits only in the desired consoles. The RD category drivers develop these RD category signals by adding various combinations of three of the six d-c level control signals from the RD control. Power amplification is provided for the category signals by power cathode followers within this circuit. Figure 4–74 is a diagram of the RD category drivers.

As shown in the figure, some combination of three of the six d-c level signals from the RD control circuit is applied to each of the AND circuits in the radar category matrix (AND circuits 1 through 8). They are identity 0 or identity 1, correlated or uncorrelated, and RD bright or RD dim. Only one signal from each pair is up for a given RD message.

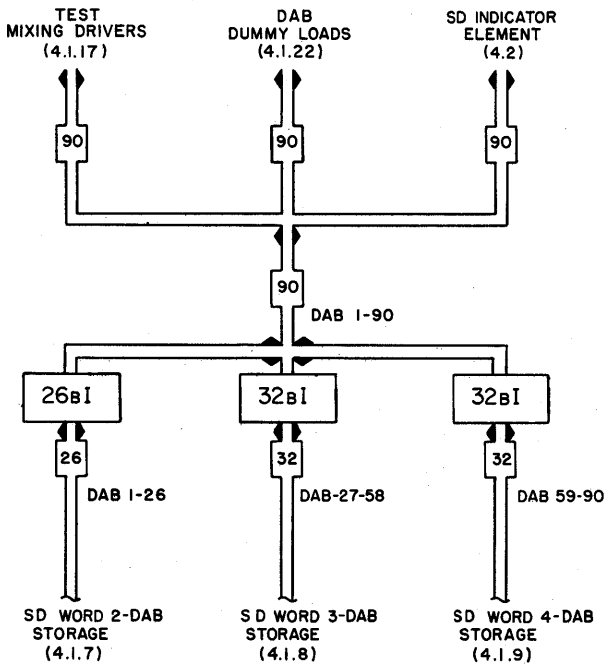
A possible combination of inputs from the RD control might be identity 1, correlated, and RD bright. The only AND circuit to which all three of these signals are applied is AND 1. Thus, the RD category 1 signal is developed. RD category signals 2 through 8 are developed in a similar manner by AND circuits 2 through 8. The three signals from RD control which are required to produce each of the eight RD category signals are indicated in figure 4–74.

RD category signals 1 through 8 (one of which is up for each RD message) are applied to eight drivers, which are power cathode followers. The eight driver outputs are sent to the RD control (to generate character selection set signals) and to display consoles of the SDIE. The RD category signals are also fed to the mixed RD category drivers.



NOTES: ALL CIRCUITS LOCATED IN UNIT 24.

Figure 4–72. Supplementary Drivers Circuit, Logic Diagram



NOTE: 1. ALL CIRCUITS LOCATED IN UNIT 24.

Figure 4–71. DAB Drivers Circuit, Logic Diagram

2.10.11 Mixed RD Category Drivers (RD Messages Only)

The mixed RD category drivers provide facilities for mixing RD categories. The RD category 1-8 signals

are received from the RD category drivers and channeled through 12 OR circuits to produce 12 mixed category signals (see fig. 4–75). The mixed signals are connected to the RD category selection switches on various consoles in the SDIE.

2.11 TRANSFER CIRCUITS SECTION

The track number of a TD tabular track message and the XY co-ordinates of an RD message may be sent to the Central Computer System through the MI element from the SDGE. (No TD tabular information or TD vector message information is transferred.) The transfer circuits section channels this information to the MI element. The circuits also deliver signals to the MI element to control the operation of the latter. Figure 4–76 is a diagram of the transfer circuit section. Other signals sent back to the Central Computer System in conjunction with transfer circuit section outputs are conditional unblank, conditional-sample, start-TD, and start-RD signals.

The transfer of information (track number or XY) is described in 2.11.1 and 2.11.2. The generation of the message-identifying signals is discussed in 2.11.3.

2.11.1 Transfer of Track Number (TD Tabular Track Message)

A track number consists of four characters which appear in a TD tabular message. They occupy format positions C1, C2, C3, and C4. C1 is a letter; C2 and C3 can be letters or decimal numerals; C4 is a numeral. Selection addresses for C1 through C3 are made up of six bits, which are stored in word 5 and 7 storage. The address for C4 also consists of six bits which are stored in word 5 storage. Only four bits, the two less significant bits of the X and Y components of the character selection address, are required for identifying the address of C4 (which is always a numeral).

Four bits, therefore, for the numeral of the track number (C4, $X2^1$, $X2^0$, $Y2^1$, $Y2^0$), and all six bits of the other characters (C_1–C_3, $X2^2$–$X2^0$, $Y2^0$–2^2), a total of 22 bits, are applied to capacitor-diode gates 26 through 47. The 22 gates are sensed by a transfer-track-number pulse from the miscellaneous control. The pulse is produced in the miscellaneous control by the coincidence of a TD signal and an information-transfer signal, the latter originating in the MI element. The track-number output of the gates is passed to the MI element through the SD input switch section.

2.11.2 Transfer of X, Y Information (RD Message)

All 22 X,Y co-ordinates of an RD message (XLS-XL10, YRS-YR10) are applied from the XY register to gates 4 through 25. The 22 gates are sensed by a transfer X,Y pulse from the miscellaneous control. The pulse results when an information-transfer signal from the MI element coincides with the RD signal in the miscellaneous control. The X, Y output of the gates is passed to the MI element through the SD input switch section.

2.11.3 Generation of Message-Identifying Signals

Capacitor-diode gates 1, 2, and 3 in the transfer circuits section generate a 2-bit code which enables the MI element to control the transfer of information from there to the Central Computer System. The output of capacitor-diode gate 1 (RD signal) produces one bit of the code (the left-hand bit), and the combined output of gates 2 and 3 (track-number or correlated signal) produces the other bit of the code (right-hand bit). Note that gates 1 and 2 are permanently conditioned by

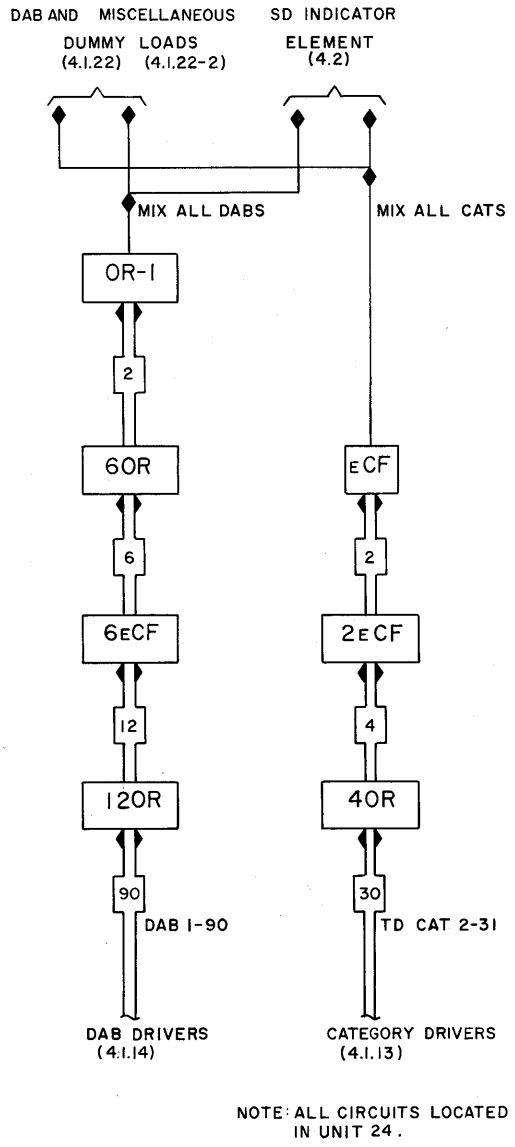


Figure 4–73. MIX-ALL-CAT's and MIX-ALL DAB's Circuit, Logic Diagram

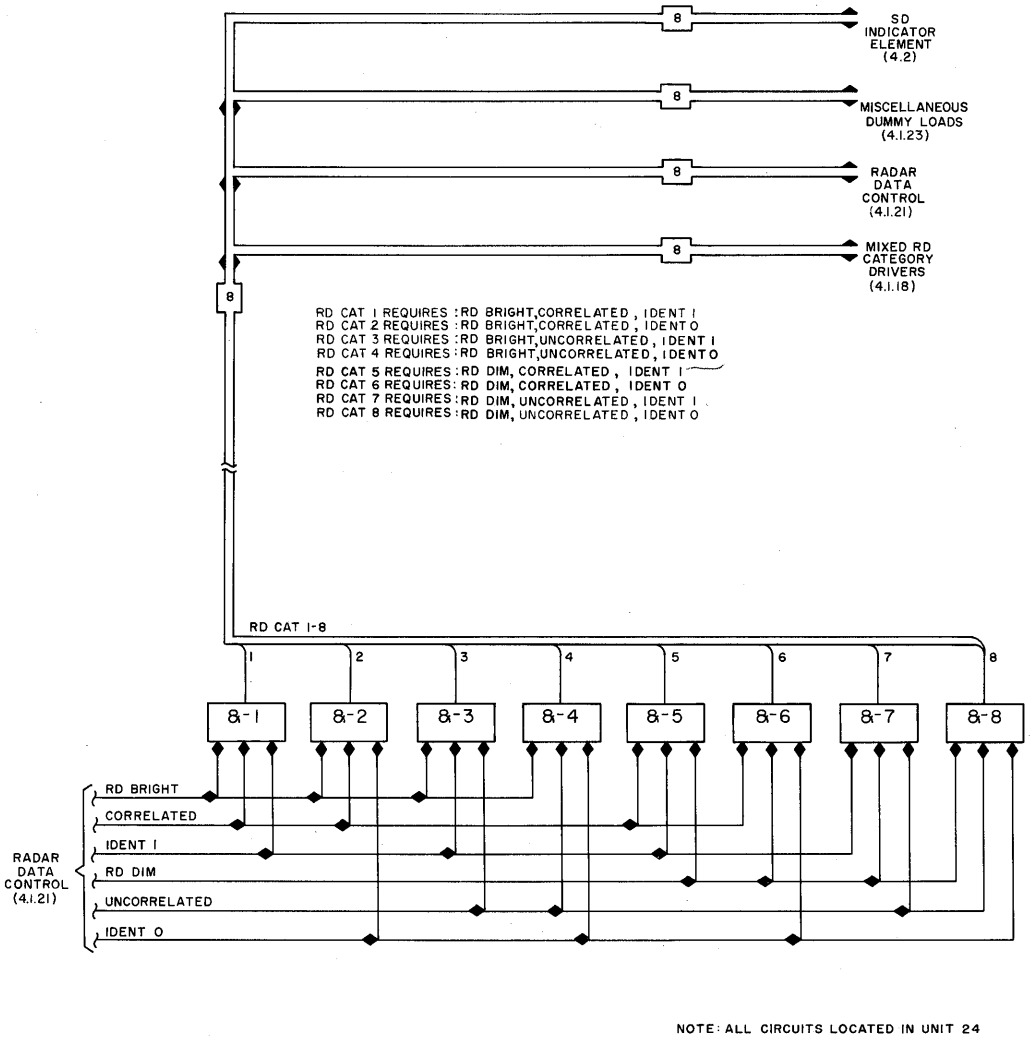
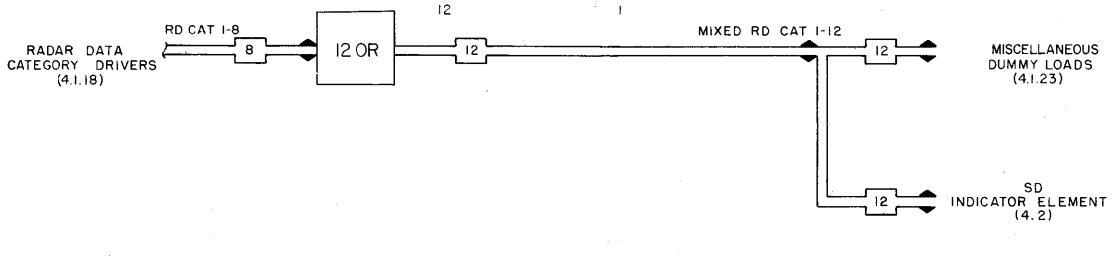


Figure 4–74. Radar Data Category Drivers Circuit, Logic Diagram

MIXED RD CAT NUMBER	IS GENERATED BY UNMIXED RD CAT NUMBER
1	5 OR 6
2	1 OR 5
3	6 OR 8
4	7 OR 8
5	5,6,7 OR 8
6	7
7	1 OR 2
8	2 OR 4
9	1,3 OR 4
10	3 OR 4
11	1 OR 3
12	1



NOTES: 1. ALL CIRCUITS LOCATED IN UNIT 24.

Figure 4–75. Mixed Radar Category Drivers Circuit, Logic Diagram

+10V levels to pass sensing pulses. Four 2-bit coded outputs are possible: 00 (during the time of no transfer to the MI element), 01 (track data), 11 (correlated radar data), and 10 (uncorrelated radar data).

2.11.3.1 TD Tabular Track Message

The 01 code indicates that track data, specifically the track number of a TD tabular track message, is being transferred to the MI element. Capacitor-diode gate 1 remains unpulsed, maintaining its 0 output. Gate 2 is pulsed to produce a 1 by a transfer-track-number pulse, which arises in the miscellaneous control as a result of an information-transfer signal from the MI element.

2.11.3.2 RD Message

The binary 10 code indicates that the X,Y position of an uncorrelated radar return is being transferred to the MI element. Capacitor-diode gate 1 is pulsed to produce a 1 by a transfer X,Y pulse, which arises in the miscellaneous control as a result of an information-transfer signal from the MI element. With uncorrelated data, the correlated signal is missing, and gate 3 is not conditioned to pass the transfer pulse and maintains its 0 output.

The binary 11 output indicates that the X,Y position of a correlated radar return is being transferred to the MI element. Capacitor-diode gates 1 and 3 are both pulsed by a transfer X,Y pulse to produce a 1 output. Gate 3 is conditioned to pass the transfer pulse by the correlated signal that arises in the RD control circuits.

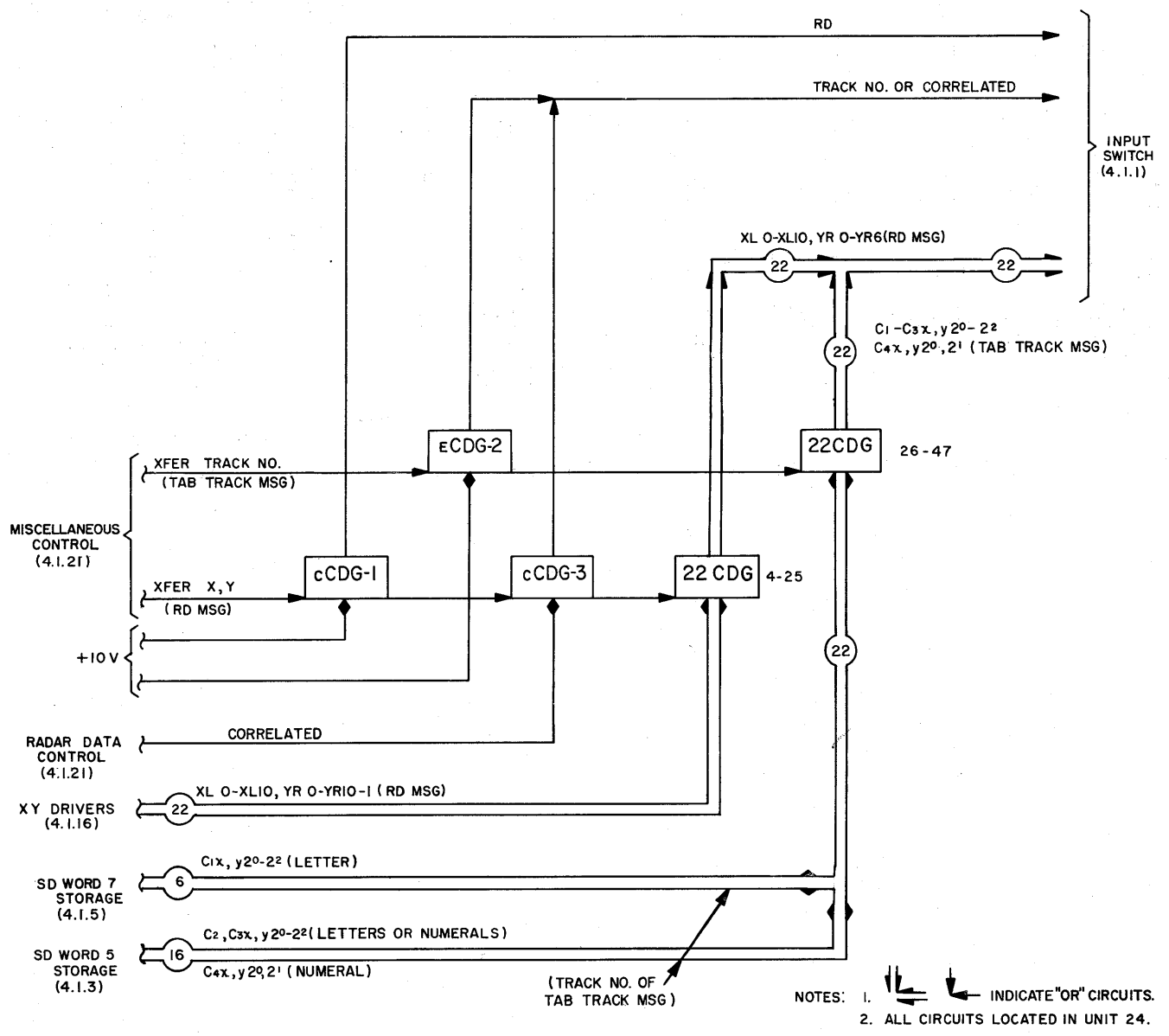
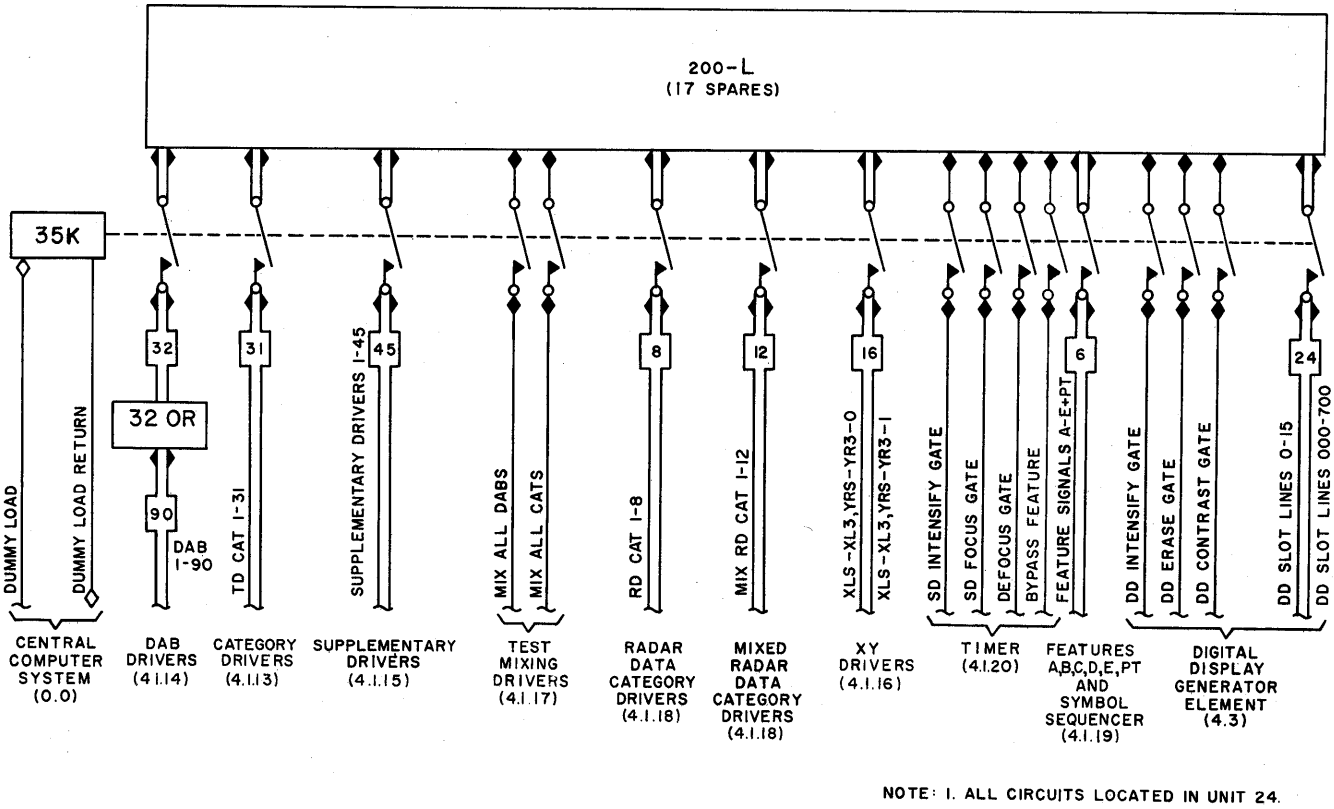


Figure 4-76. Transfer Circuits, Logic Diagram

2.12 DUMMY LOAD SECTION

The dummy load circuit provides dummy loads for outputs of the situation and digital display generator elements. (See fig. 4–77.) These outputs, normally applied to the SD or DD indicator elements, are also routed to dummy loads by the operation of 35 parallel relays. The relays are energized by the dummy-load signal from the duplex maintenance console of the Central Computer System.

Each of the inputs, with a few exceptions, is directly connected through a single pair of relay contacts to a dummy load. The DAB 1 through 90 signals are mixed in 32 OR circuits and applied to 32 dummy loads.



NOTE: 1. ALL CIRCUITS LOCATED IN UNIT 24.

Figure 4–77. DAB, Miscellaneous and DD Dummy Loads Circuit, Logic Diagram

SECTION 3
SD TIMING AND CONTROL

3.1 INTRODUCTION

The SD timing and control regulates the operation of SDGE display cycles. Each cycle produces situation displays for observation on the CRT's of the SDIE. Drum control pulses and information signals are sent to the timing and control section of the SDGE to operate counters and other circuits of pertinent importance. The outputs of the section control the reading of an SD message from the drums and the separate display of each character or vector in the display cycle of the message. Each time a cycle is completed, an end-cycle pulse is generated to turn off the SDGE. This pulse is also sent to the display tester element to control its operation.

3.2 TIMING, CONTROL, CIRCUITS, AND SIGNALS

Figure 4–46 is a diagram of the SD timing and control section, showing the 14 circuits in block form. The figures referenced in paragraphs 3.2.14.1 and 3.2.14.24 are detailed timing charts of TD and RD display cycles, respectively.

Six types of drum control pulses synchronize the operation of the SD timing and control section with the reading operation in the Drum System.
These signals are:

a. All-OD's (timing pulses OD 1, 2, 3, and 4 on one line; one OD pulse is received from the output side of the drum every 2.5 μsec)

b. WOW pulse (word-on-way pulse; one WOW pulse is received 2.5 μsec (OD 4 time) before word is read at OD 1 time)

c. Start-TD (start-track-data pulse; this pulse is an RD drum index signal, received in order to prepare the SD timing and control section for TD messages)

d. Start-RD (start-radar-data pulse; this pulse is a TD drum index signal, received in order to prepare the SD timing and control section for RD messages)

e. RD-bright (radar-data-bright pulse, which accompanies an RD message from the last RD drum field previously written on by the Central Computer System)

f. RD-dim (radar-data-dim pulse, which accompanies each RD message from an RD drum field other than the last field written on by the Central Computer System and the field currently being written on it)

Additional controls for the generation of situation displays are taken from bits in the SD messages. TD message control bits are connected from the word storage section to the timing and control section where the following signals are developed:

a. Tabular message

b. Vector message

c. Track message

d. Information message

e. Display

f. Use-light-gun

The RD message control bits indicate the identity (L14) and the status, correlated or uncorrelated (L15), of the RD source. These control bits are applied through the input gates to the SD timing and control section.

Three counting circuits in the SD timing and control section provide the major internal regulation of the SDGE. These circuits are the OD distributors, the symbol sequencer, and the timer counter.

The OD distributor counts OD pulses which arrive at the SDGE on a common "all OD" line. These pulses occur at 2.5-μsec intervals. The counter divides these pulses so that there are four individual pulses; namely, OD 1, 2, 3, and 4.

The timer counter develops command signals, during the generation of an SD message display cycle, in order to operate the various circuits required to produce an individual display. Examples of such commands from the timer are the SD intensity, focus, and defocus gates (which are directly connected to the consoles of the SDIE), the vector-off signal (which is connected to the vector generator), the advance-character-position signal (which is connected to the character counter and positioning circuit), and the conditional-unblank, conditional-blank, and conditional-sample signals (which are used for transferring information into the MI element).

At the end of the generation of a character or vector display in a display message cycle, the timer sends out a transfer signal to the vector control and feature circuits in order to display the next character or vector.

The counter in the symbol sequencer serves two purposes during the display cycle of a TD message. During the drum-reading period, at the beginning of a TD

message display cycle, the symbol sequencer counter controls the generation of read-word signals. These signals determine the distribution of the words of the message into the generator. The symbol sequencer also divides the total time of a TD message display cycle. This time, being divided into segments, allows for the proper display of different vectors and characters in the message.

In addition to the OD distributor already described, the ON-OFF control and OD distributor section contains a flip-flop (a bistable multivibrator circuit) that serves as the on-off control to the generator. This con-

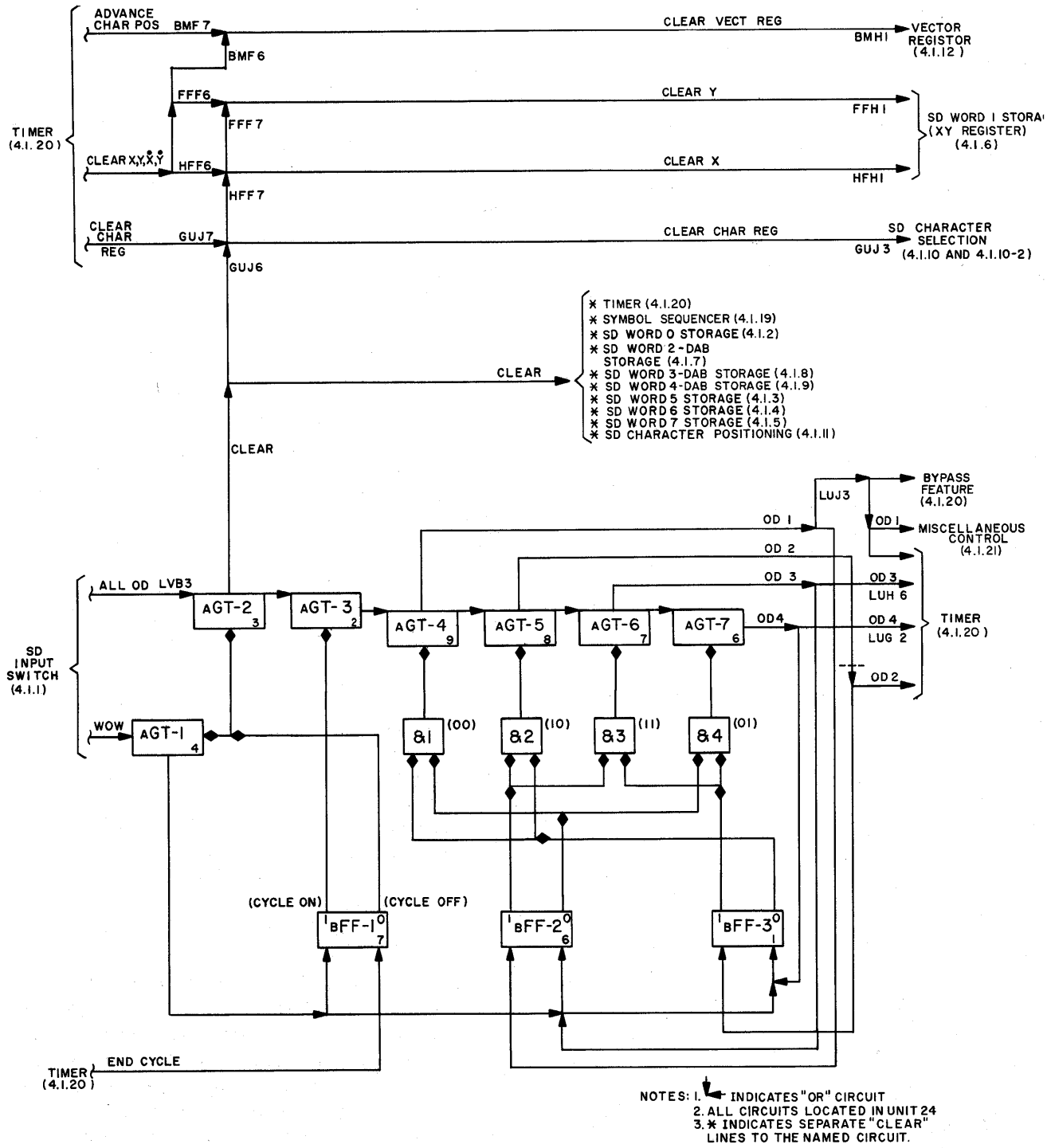


Figure 4–78. On-Off Control and OD Distributor Circuit, Logic Diagram

trol must be on before the OD pulses will activate the OD distributor. The on-off flip-flop is turned on by the WOW pulse preceding the first word of an SD message read from the drum. This flip-flop is turned off at the end of the display cycle, and then the OD's produce clear pulses for the entire SDGE. These pulses keep the SDGE cleared until receipt of the next message.

The miscellaneous control (besides generating the add-1 pulses to the symbol sequencer and channeling the RD-bright and -dim signals to the RD control) receives a start-TD signal or a start-RD signal from the Drum System to identify the message being read into the SDGE. The miscellaneous control also develops the read signal which conditions the input gates section to pass bits of words being read into the generator. Furthermore, the miscellaneous control regulates the transfer of information from the SDGE through the MI element into the Central Computer System.

Additional circuits in the SD timing and control section are the gate generator (which produces read-word signals), the seven feature circuits (that produce control signals for the display of individual characters in a TD message), and the vector and RD control circuits.

Outputs from the SD timing and control section which are normally connected to the SDIE are the feature signals and the SD intensify, focus, and defocus gates. These outputs can be switched to dummy loads when the SDGE is to be marginal checked. The controlling relays are energized by the Central Computer System.

3.2.1 On-Off Control and OD Distributor

The on-off control and OD distributor contains circuits for turning the SDGE on for a message display cycle, for distributing OD pulses throughout the generator when the SDGE is on, and for clearing flip-flops in the generator after a message display cycle has been completed. A logic diagram of the on-off control and OD distributor is shown in figure 4–78.

3.2.1.1 On-Off Control

The on-off control is a flip-flop (FF 1) which is set by the WOW pulse preceding the first word sent from the Drum System. This pulse occurs 2.5 μsec before the first word of an SD message is read. The WOW pulse passes through gate 1, which is conditioned by the 0 side of FF 1, and sets the on-off flip-flop and clears the OD distributor. When the message display cycle is completed, an end-cycle signal is generated. This signal clears the on-off flip-flop (flip-flop to 0 state) which prevents all OD's from being distributed as OD 1, 2, 3, and 4's. However, succeeding OD pulses pass gate 2 as clear signals to circuits in the SDGE.

3.2.1.2 OD Distributor

The SDGE receives a drum OD pulse (OD 1, 2, 3, and 4) every 2.5 μsec on one input line. The pulses are then sorted onto four different lines by OD distributor FF's 2 and 3 and are delivered to the circuits in the SD timing and control section.

In sorting the OD's, the OD distributor flip-flops operate as a counter in the following manner. After the initial WOW pulse (at OD 4) has turned on the generator and set the OD flip-flops to 0, the OD 1 that follows 2.5 μsec later is able to pass gate 3 (which is now conditioned by the on state of the on-off flip-flop) and gate 4 (which is now conditioned by a 00 output of the OD flip-flops through AND 1). The OD 1 output of gate 4 is connected to the timer, bypass feature, and miscellaneous control circuits. At the same time, it is connected back to the 1 side of OD FF 2 to bring up that side for the next step in the operation of the distributor circuit. The two OD flip-flops now have a 10 output which produces an output from AND 2. The 10 output of AND 2 conditions gate 5, which is now ready to pass pulse OD 2, the next OD pulse to arrive from the drum. After passing gate 5, the OD 2 pulse is connected back to the 1 side of OD FF 3 to bring up the 1 side of that flip-flop for the next step in the operation of the distributor circuit. The OD 2 pulse is also applied to the timer. The two OD flip-flops now have an output of 11 which produces an output from AND 3.

The 11 output of AND 3 conditions gate 6, which is now ready to pass pulse OD 3, the next pulse to arrive from the drum. After passing gate 6, the OD 3 pulse is connected to the timer for general use. At the same time, it is connected back to the 0 side of FF 2, bringing up that side for the next step in the operation of the distributor circuit. The two flip-flops now have an 01 output which produces an output from AND 4. The 01 output of AND 4 conditions gate 7, which is now ready to pass pulse OD 4, the next OD pulse to arrive from the drum. After passing gate 7, the OD 4 pulse is connected to the timer for general use. At the same time, it is connected back to the 0 side of FF 3, bringing that side up for the next step in the operation of the distributor circuit. The two OD flip-flops now have a 00 output, which produces an output from AND 1. This output conditions gate 4, which is now ready to pass pulse OD 1, the next OD pulse to arrive from the drum. The OD 1 pulse passes gate 4 in the same manner as the previous OD 1 pulse. The action of the OD distributor circuit then repeats itself for all succeeding OD pulses until the on-off flip-flop is turned off at the end of a display cycle. This removes the conditioning voltage from GT 3 through which all OD pulses enter the distributor. At the beginning of a new message display cycle, the first WOW (at OD 4) clears FF's 2 and 3, ensuring that the first OD pulse will be an OD 1.

3.2.1.3 Clear Signals

Clear signals are generated to keep the SDGE free from transients on the lines and previous data from affecting the display of a new cycle. Overall clear signals for the flip-flop circuits of the generator are developed by the on-off control and OD distributor section after the completion of a message display cycle. The signals are initially developed by the arrival of the end-cycle signal from the timer. This signal drives FF 1 to off (0 output) which deconditions gate 3 and conditions gate 2. This action prevents succeeding OD pulses from entering the OD distributor through gate 3; instead, it passes the succeeding OD pulses through gate 2 to clear (0 input) the storage, register, and counter flip-flop in the generator. Since the end-cycle signal occurs at the timer count of 7, OD 3 (an OD 3 steps the timer-counter), the first overall clear signal after a cycle has been completed occurs at the timer count of 3, OD 4. This is 2.5 μsec after the end of the cycle.

The overall clear pulse for the XY, character, and vector registers is connected separately from the on-off control and OD distributor section through OR circuits which also pass clear pulses. The pulses occur after the generation of each separate character or vector display in a TD message display cycle; the pulses are produced in the timer.

3.2.2 Miscellaneous Control Circuit

The miscellaneous control circuit develops the required signals for regulating the generation of SD messages. It develops a read (drum) signal for conditioning the input gates section of the SDGE when messages are being read into the generator from the drums. The miscellaneous control circuit amplifies the start-TD signal sent to the PRRE. It also generates the add-1 pulse to the symbol sequencer and a TD signal for reading

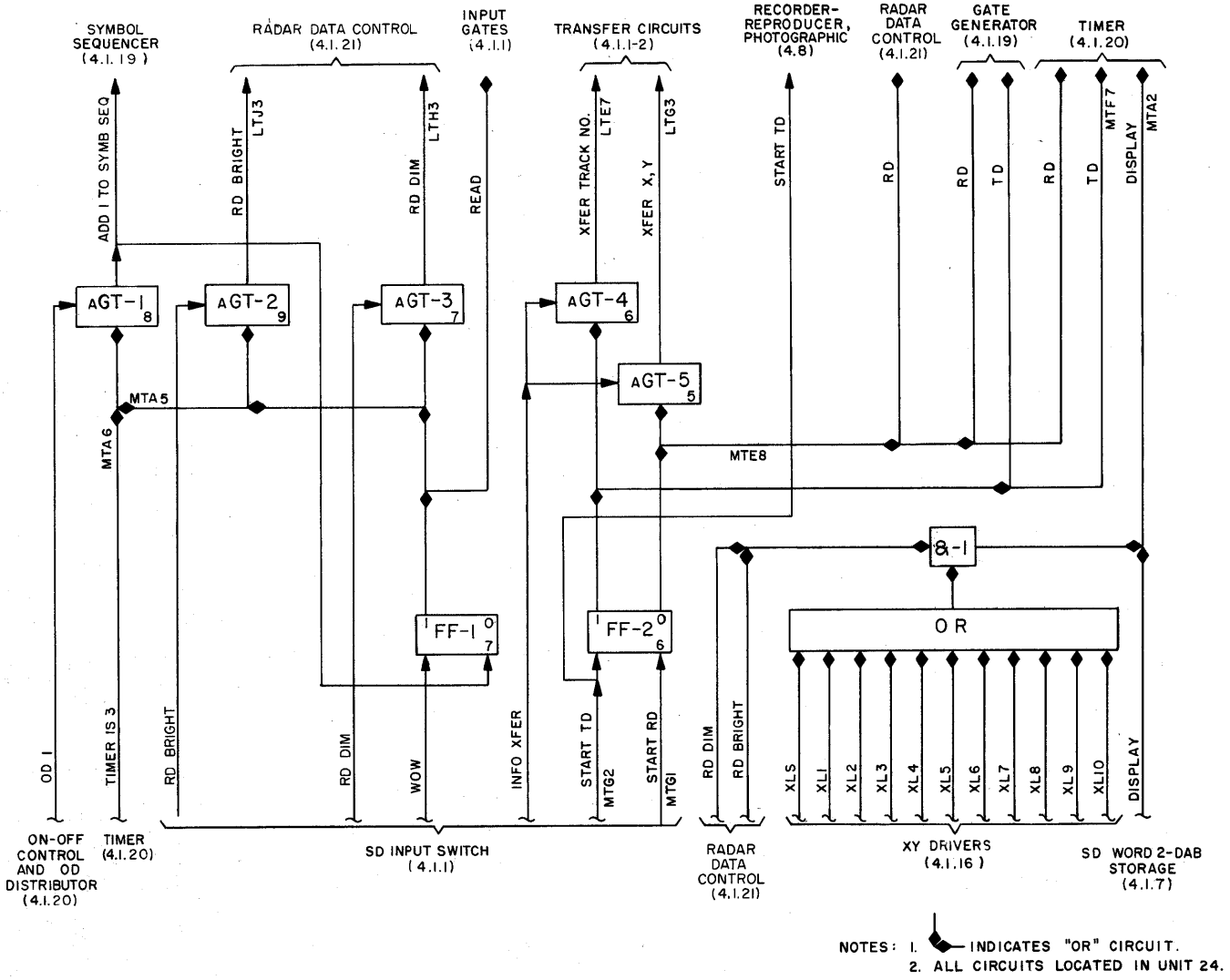


Figure 4–79. Miscellaneous Control Circuit, Logic Diagram

all words out of storage. Since one word is read in an RD message, it is necessary only to obtain a read-word 1 level. This is achieved by inhibiting the TD signal and allowing the RD signal to condition the reading of the one word. Figure 4–79 is a logic diagram of the miscellaneous control section.

3.2.2.1 TD Tabular Message

The TD-RD flip-flop in the miscellaneous control circuit establishes control signals to enable the SDGE circuits to distinguish between TD and RD messages. The TD output of this flip-flop conditions GT 4 whose output is the transfer-track-number signal. This signal permits the transfer of the track number of a TD tabular track message to the MI element. The miscellaneous control routes a display signal to the timer during the generation of all messages. This permits intensification only for those slots on the drum that are filled with messages.

A read signal is developed when FF 1 is set by a WOW pulse which occurs 2.5 μsec (at OD 4) before a word is read from the drum (at OD 1). This signal is then connected to the input gates section where it conditions the gates, allowing them to pass the bits of data being read from the drums into the SDGE.

The read (drum) signal has a duration of 2.5 μsec. This is due to the read signal conditioning GT 1 which will pass an OD 1 pulse (2.5 μsec after the WOW pulse raised the level of the read signal) to clear FF 1 and lower the level of the read signal. This same OD 1 time corresponds to the time that the message bits of a word on the drum are being read through the input gates section. Therefore, the time that elapses before the conditioning level is removed from the input gates section is sufficient to permit the message bits to pass into the SDGE.

The add-1 pulses for the symbol sequencer, during the generation of a TD tabular message, are generated in the miscellaneous control circuit. During the time that words of the message are actually being read into the SDGE through the input gates section, the add-1-to-symbol-sequencer signal is produced. This add-1 signal is generated eight times during the reading in of a TD message; the WOW signal and the OD 1 pulse, 2.5 μsec after the WOW, produce the add-1 signal through GT 1.

After the eight words have been read into the generator, in a TD tabular message display cycle, the symbol sequencer is stepped at 50-μsec intervals to divide the display cycle into intervals for the separate generation of each vector and character. During this time, OD 1 pulses also step the symbol sequencer through gate 1 in the miscellaneous control circuit. These OD 1 pulses also pass through gate 1 because the gate is conditioned by the timer-is-3 level. This level occurs after the timer has counted through its cycle of 3 to 7 and has finished commanding the signals necessary for generating an individual display in a tabular message display cycle. (When the timer stepped to 3 from 7, the commanding signals for the previous individual display were completed.)

The TD and RD control signals enable the generator to distinguish between TD and RD messages. The signals are produced by the outputs of FF 2. The TD signal is raised due to FF 2 being set on the 1 side by a start-TD pulse from the Drum System. This pulse is the RD drum-index pulse which is sent from the Drum System after the display of the 1-word message read from the RD drum.

The TD signal is connected into the timer and gate generator circuits. The TD signal also conditions GT 4 in the miscellaneous control circuit, which passes an information-transfer pulse that originated in the MI element. This signal is applied to the transfer circuits section as a transfer-track-number signal. It permits the character selection bits for the track number of a TD tabular message to pass through the transfer circuits section to the MI element and then to the Central Computer System.

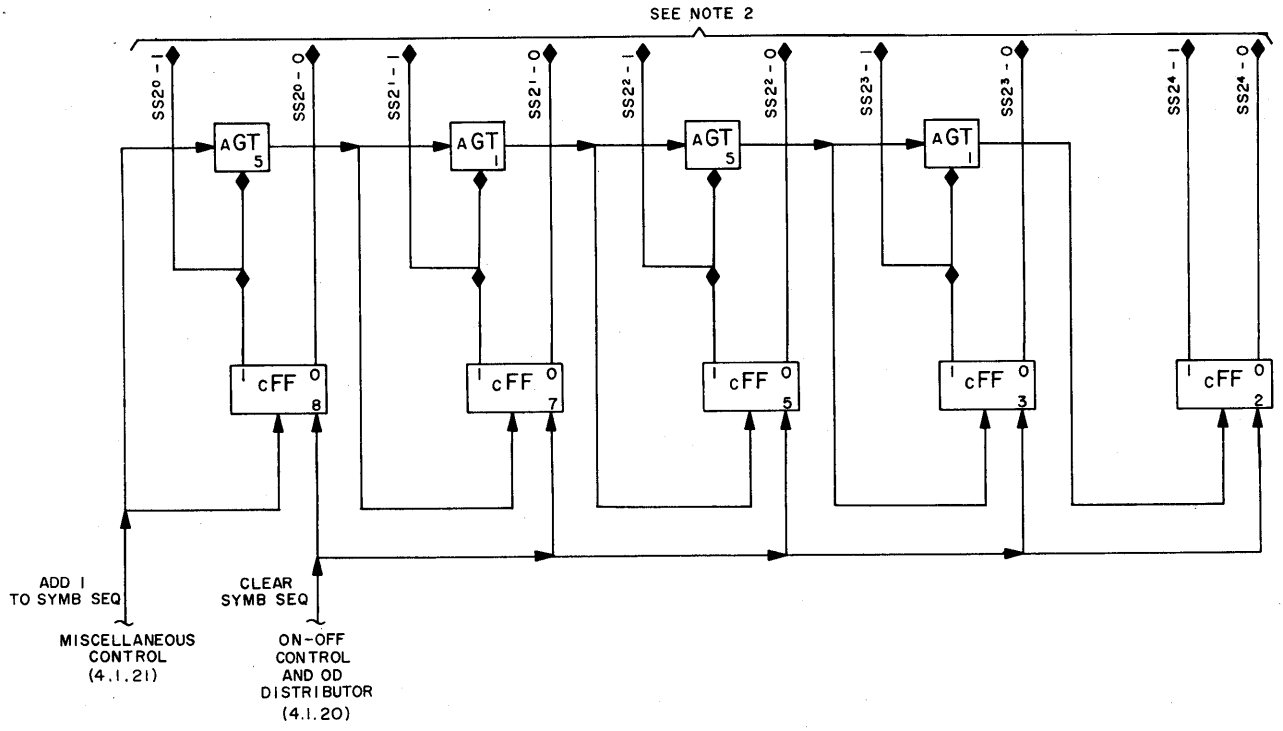
The miscellaneous control contains the circuits necessary for routing the display signal to the timer. This signal is contained in a control bit of the SD message. The display bit allows the intensification of the message received from the drums. However, the display bit is inhibited to prevent intensification of the co-ordinates corresponding to the empty slots of the drum. In the case of a TD message, the display signal originates in the storage of word 2, L5. The display signal is passed through an OR circuit in the miscellaneous control to the timer circuit.

3.2.2.2 TD Vector Message

Since the miscellaneous control section functions similarly for TD vector messages and TD tabular messages, the discussion in 3.2.2.1, TD Tabular Message, is used. The transfer-track-number signal is not required for a TD vector message.

3.2.2.3 RD Message

The TD-RD flip-flop in the miscellaneous control circuit establishes TD and RD signals which enable the SDGE to distinguish between TD and RD messages. The RD signal is developed when a start-RD pulse clears FF 2 to raise the 0 output. The start-RD pulse is a TD drum-index pulse which is sent from the Drum System after the display of the last message from the TD drum. The RD output of FF 2 conditions gate 5 in the miscellaneous control circuit. (See fig. 4–79.) Gate 5 passes the information-transfer signal to the transfer circuit as the transfer X, Y signal. This permits the



	$SS2^4$-0	$SS2^4$-1	$SS2^3$-0	$SS2^3$-1	$SS2^2$-0	$SS2^2$-1	$SS2^1$-0	$SS2^1$-1	$SS2^0$-0	$SS2^0$-1
TIMER (4.1.20)		*		*						
GATE GENERATOR (4.1.19)					*	*	*	*	*	*
VECTOR CONTROL (4.1.19)	*	*	*	*	*	*	*	*	*	*
A FEATURE (4.1.19)	*	*	*	*	*	*	*	*	*	*
B FEATURE (4.1.19)	*	*	*	*	*	*	*	*	*	*
C FEATURE (4.1.19)		*		*	*		*	*	*	*
D FEATURE (4.1.19)		*	*		*			*	*	*
E FEATURE (4.1.19)	*		*	*	*	*	*		*	
POINT FEATURE (4.1.19)	*			*	*		*			*

NOTES: 1. ALL CIRCUITS LOCATED IN UNIT 24.
2. * APPEARING UNDER AN OUTPUT SIGNAL IN THE TABLE INDICATES THAT THE SIGNAL IS APPLIED TO THE CIRCUIT OPPOSITE WHICH THE * IS PLACED.

Figure 4–80. Symbol Sequencer Circuit, Logic Diagram

transfer of the X, Y position of the RD message through the MI element to the Central Computer System. The RD signal is also connected to the timer, the gate generator, and the RD control where specific control functions are performed.

A read (drum) signal is generated when FF 1 receives a WOW pulse 2.5 μsec (OD 4) before a word is read from the drum (OD 1). This signal is connected to the input gates section where it conditions the gates to allow RD message information bits to pass from the drums at reading time (OD 1) into the generator. The read (drum) signal is also connected in the miscellaneous control to gates 2 and 3, which are the input gates of the RD-bright and RD-dim signals from the drum. A radar-bright or radar-dim signal accompanies each (one word) message read into the generator from the RD drum.

A display signal is produced for RD messages by the coincidence in AND 1 of any X-position-information -1 bit in the XY register and an RD-bright or RD-dim signal, which is present during the generation of an RD message. (An RD-bright or RD-dim signal is not present for an RD message when the Central Computer System chooses to write on a field while the Display System is reading the field.) The presence of the X-position information is indicated as an input to AND 1 through an 11-input OR circuit. This OR has an output if one of the XLS-1 to XL10-1 signals is applied to it. Therefore, when blank slots are being read, the OR is deconditioned, thus inhibiting the display bit. This prevents the intensification of the CRT from burning a portion of the viewing screen with X = 0, Y = 0 co-ordinates. The display signal is sent to the timer, during RD messages, to permit intensification of the message.

3.2.3 Symbol Sequencer (TD Messages)

The symbol sequencer is a 5-stage counter whose outputs are used for two major purposes in the SDGE. During drum-reading time, at the beginning of a TD message display cycle, the symbol sequencer outputs are applied to the gate generator. They generate signals which condition the distribution gates of storage and register flip-flops. Throughout an entire TD message display cycle, the symbol sequencer outputs divide the cycle into intervals in which the separate display of each vector and character in the message can occur. Figure 4–80 is a circuit diagram of the symbol sequence; the associated circuits of the symbol sequencer are listed in the table.

The symbol sequencer counts continuously from 0 to 27 before it is cleared at the end of a message cycle. During the time the drum is being read into a display cycle, eight stepping pulses (add-1 signals) for the counter are generated in the miscellaneous control circuit OD 1 pulses following the WOW signal preceding each word from the drum. These add-1 signals occur at 10 μsec intervals and advance the counter to 8. During the remainder of the display cycle, the stepping pulse is the OD 1 coincident with the timer count of 3, which occurs at 50-μsec intervals. In both cases, the add-1 signals are channeled to the symbol sequencer through the miscellaneous control circuit.

The outputs of the flip-flop counter are AND'ed to produce control levels, at specific counts, to the SD timing and control section. At the counts of 0 to 7, the gate generator produces read-word signals as words are being read (via the input gates section) from the drum. Each read-word signal is applied to the admittance (distribution) gates of the specific storage and register flip-flops corresponding to the particular word being read. Beginning with the count of 9, each count is used in the A through D and point feature circuits, and in the vector control circuit as the generation control for one character or vector of the TD message. The E feature circuit uses the interval between the symbol sequencer counts of 4 and 9 as timing for its generation control. The $SS2^4$-1 and $SS2^3$-1 outputs are also applied to the timer and through it to the bypass feature circuit. The symbol sequencer outputs are not required for RD messages.

3.2.4 Gate Generator

The gate generator develops read-word signals during the time that drum reading occurs at the beginning of TD and RD message display cycles. The read-word signals condition admittance (distribution) gates in word storage and register logic in such a manner as to deposit the different words coming from the drum (via the SD input switch and gates sections) into the proper storage or register for each word. Figure 4–81 shows a detailed gate generator circuit.

3.2.4.1 TD Messages

Read-word signals for TD messages are developed by outputs from the symbol sequencer, and tabular and vector message control signals from word 0 storage. The symbol sequencer counts used for this purpose are 0 to 7 (000 to 111); the 0 count is used for word 0; the 1 count, for word 1, etc., until the count of 7, which is used for reading word 7. The 0 and 1 levels from the three flip-flops ($SS2^2$, $SS2^1$, $SS2^0$) which count up to seven in the symbol sequencer are connected into the gate generator and AND'ed to produce a voltage level for each of the read-word counts 0 to 7. The resulting read-word signals are applied to the word category and DAB storage circuits. At the symbol sequencer count of 1, two read X, Y signals are produced which admit bits LS-L9 and RS-R9 into the XY register.

AND's 1 to 11 produce the read-word signals for TD messages. It is possible for tabular and vector mes-

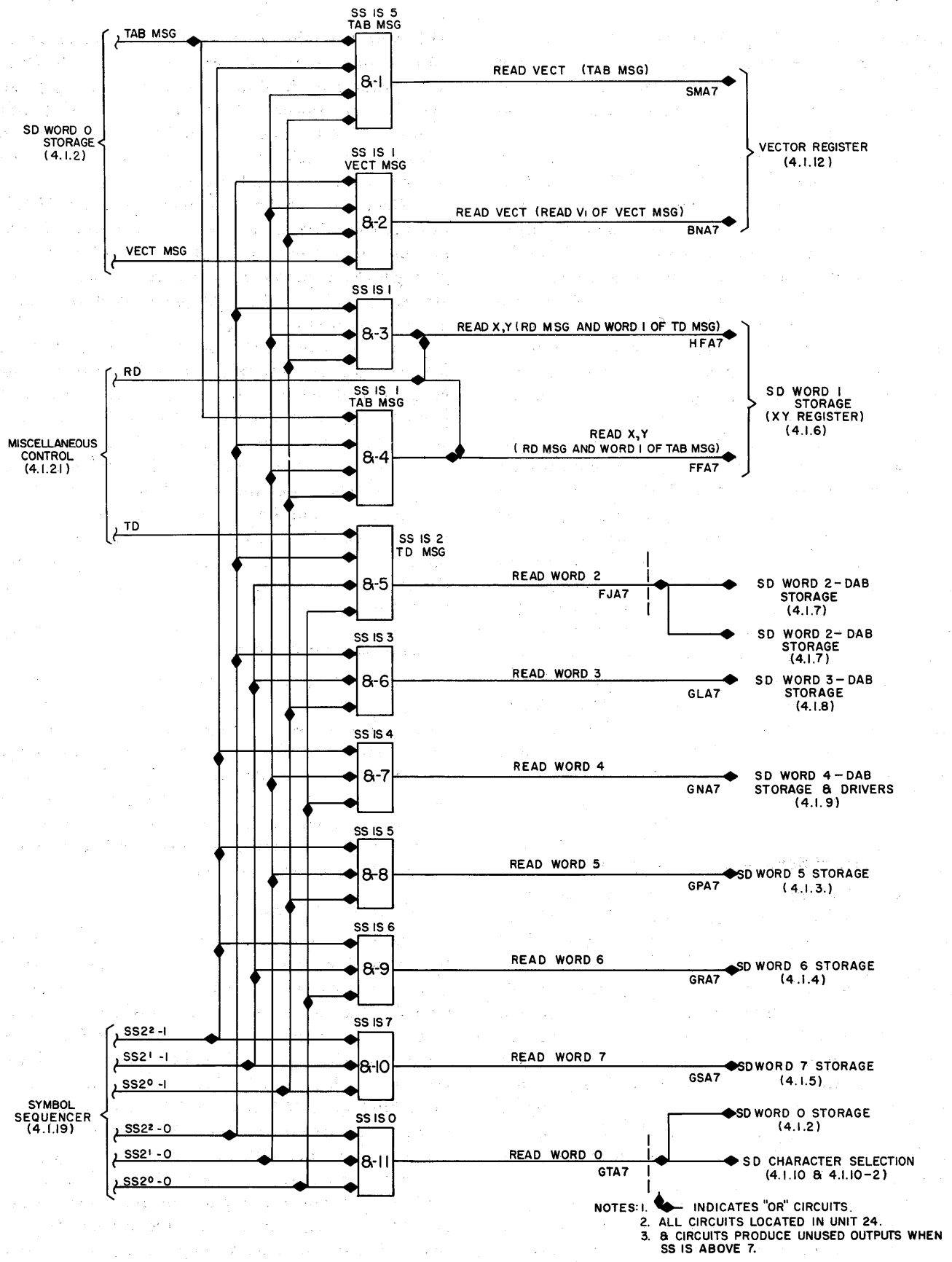


Figure 4–81. Gate Generator Circuit, Logic Diagram

sage control bit signals, connected from word 0 storage, to regulate drum reading into storage and registers, since the reading of word 0, the first word read in a TD message, does not need the regulation of either signal. For the following words, which need regulation by one of the signals, the controls are already stored and available for use. Note that the read-word 2 level requires the coincidence of a TD signal with the symbol sequencer levels. This TD level guarantees that no read-word 2 signal is generated during RD message time. If the read-word 2 signal is generated at RD time, erroneous CAT and DAB signals would be generated.

3.2.4.2 TD Tabular Message

The read-word 0 signal is also applied to the character register where it admits the selection bits for the E character of a TD tabular message. The symbol sequencer outputs at counts 1 and 5 are AND'ed with the tabular-message signal to produce read X, Y and read-vector signals, respectively. These signals admit XY bits LS-L12 and RS-R12 (word 1) and the $\dot{X}$, $\dot{Y}$ bits of the vector (word 5) into the XY and vector registers, respectively.

3.2.4.3 TD Vector Message

The count of 1 in the symbol sequencer is AND'ed with a vector-message signal in AND 2. This produces a read-vector signal which admits the $\dot{X}$, $\dot{Y}$ of the first vector into the vector register. The read-XY signal (AND 3) is also produced at this time, and LS-L9 and RS-R9, the central point for the first vector, are transferred to the X and Y drivers section.

3.2.4.4 RD Message

The read signals for RD messages are not developed by counts from the symbol sequencer but rather by the RD signal which is continuously generated by the miscellaneous control circuit when the RD drum is being read. The RD signal is connected to the admittance (distribution) gates of the flip-flops in the XY register through two OR circuits. OR 1 passes the RD signals as a read-XY signal to the gates that pass LS-L9 and RS-R9 into the register flip-flops. OR 2 channels the RD signal as a read-XY signal to the gates that pass bits L10-L12 and R10-R12 into the register. However, L11, L12 and R11, R12 are not utilized in an RD message.

3.2.5 A Feature Circuit

The A feature circuit generates control signals for the display of the A_1-A_6 characters in a TD tabular message and the G_1-G_4 characters in a TD vector message. Character-transfer signals are also generated with the aid of the A-feature signal.

3.2.5.1 TD Tabular Message

The A feature circuit operates under control of the symbol sequencer to produce the signals required to generate the six characters of the A feature (A_1 through A_6) in a TD tabular message display cycle. The signals consist of the A-feature signal connected to the consoles of the SDIE; the A_1 to A_6 character generation control (as the A-feature signal) connected to the timer through the bypass feature; an A_1 character signal connected to the timer; and the character-transfer signals which transfer the bits of the next character to be displayed from word storage into the character register. Figure 4–82 is a logic diagram of the A feature circuit.

AND circuits 1 through 6 combine the symbol sequencer outputs ($SS2^0 = 0$, $SS2^0 = 1$, etc.) with a tabular-message signal in order to produce an A-feature signal. This signal is produced at the time in a TD tabular message display cycle when any of the A characters are generated. The A-feature signal is also used as the overall generation control signal for the A_1 to A_6 characters.

The A-feature signal is connected to the feature selection switches on the consoles of the SDIE for display according to the operator's wishes. The A-features signal is connected through the bypass feature circuit to the timer to produce defocus, focus, intensity, and other signals necessary for the display of A characters.

An A_1 signal is produced in AND 6 at the symbol sequencer count of 11 in a TD tabular message. This signal is sent to the timer where it receives the proper timer count to develop the advance character-position signal for positioning the display of the A_2, B_1 characters after the A_1 character has been generated.

Character-transfer signals are developed in the A feature at the end of the display of each A character in a TD tabular message display cycle. Each character-transfer signal causes the transfer of the character selection bits for one character from the word storage section to the character register. The characters which are transferred to the character register immediately after the display of the A1 character are A_2, B_1, A_3, B_2, A_4, B_3, A_5, B_4, A_6, and B_5.

The transfer signals for the characters that follow A characters are passed through capacitor-diode gates 1 through 6. The gates are conditioned by the appropriate contents of the symbol sequencer, as developed in AND's 1 to 6. The transfer (from storage into register) signal that senses each gate occurs at the timer counter of 3, OD 1, which is the time when the display of an individual character ends.

3.2.5.2 TD Tabular Track Message

The A-feature signal is connected to the feature selection on the consoles of the SDIE. This permits display of the A characters if desired by the operator.

3.2.5.3 TD Tabular Information Message

In the case of TD tabular information messages, the

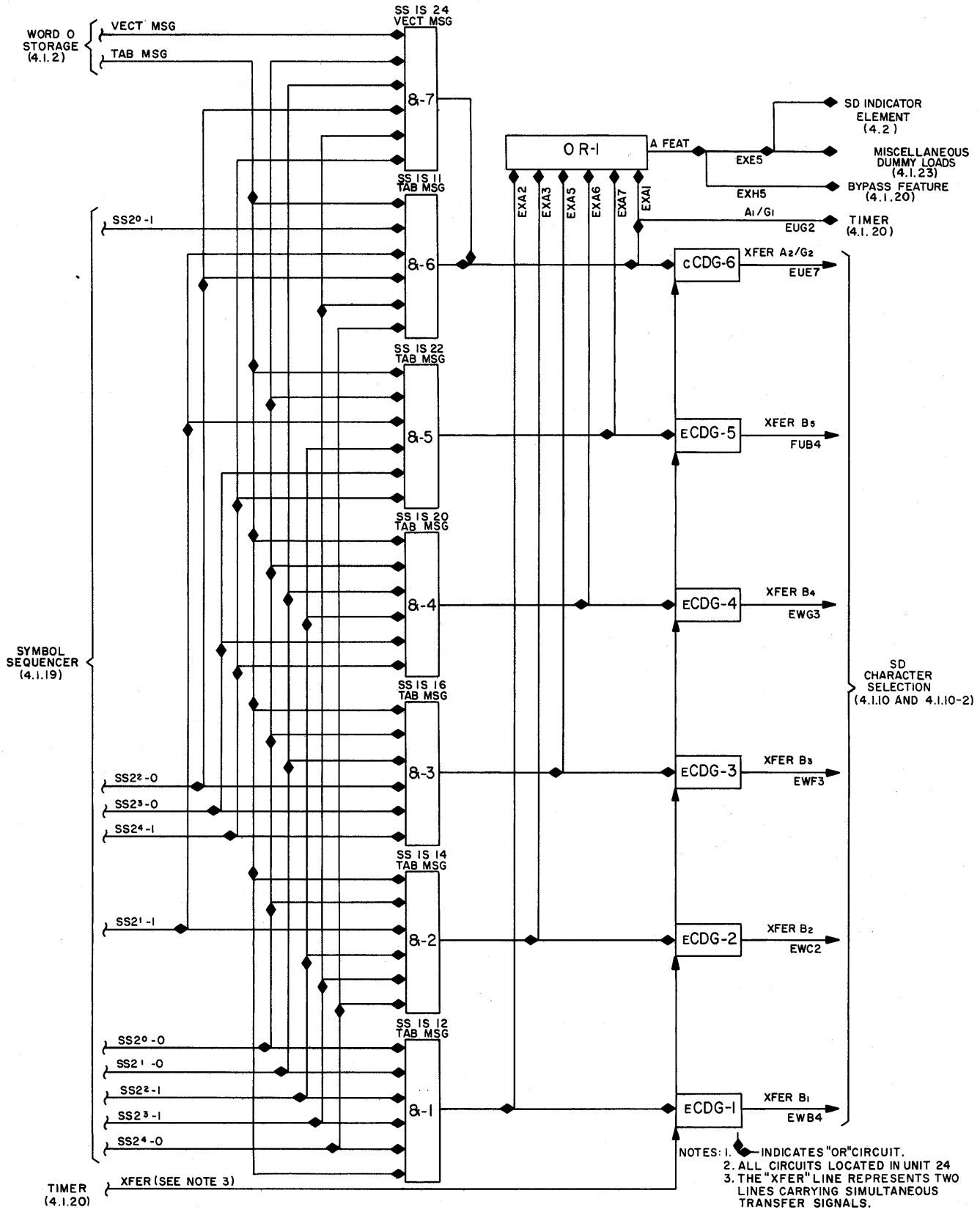


Figure 4–82. A Feature Circuit, Logic Diagram

A characters are forced. To accomplish this, the A-feature signal is applied to the bypass feature circuit where it generates the bypass-feature signal.

3.2.5.4 TD Vector Message

The A feature also produces the signal required for the generation of the G_1 character in a TD vector message display cycle. The operation is the same as that for TD tabular messages except that AND 7 is conditioned by the symbol sequencer to produce the generation control signal for the G_1 character.

The G_1 signal is connected (on the same line as the A_1 signals) through feature circuits to the timer to produce the signals necessary for the generation of a G_1 character. The G characters have no display control at the feature selection switches because the vector message generates a bypass-feature signal during the whole message.

A character-transfer signal is developed in the A feature at the end of the display of the G_1 character. G_2 is then transferred to the character register.

CDG 6 is used to pass the character-transfer signal for G_2 (as well as A_2). This common output circuit can be used for G_2 and A_2 since the character selection bits for both come from the same flip-flops in word 0 storage.

3.2.6 B Feature Circuit

The B feature circuit produces control signals for the display of the B_1 through B_5 characters in a TD tabular message and of the G_2 and G_3 characters in a TD vector message. Character-transfer signals are also generated.

3.2.6.1 TD Tabular Message

The B feature operates under control of the symbol sequencer to produce the signals required to generate the B characters (B_1 through B_5) in a tabular track message display cycle. The output signals of the symbol sequencer consist of the B-feature signal (connected to the consoles of the SDIE and to the bypass feature) and the character-transfer signal which transfers the character selection bits for the A_3, A_4, A_6, C_1, and D_1 characters from word storage into the character register in a TD tabular message display cycle. Figure 4–83 is a logical diagram of the B-feature.

AND circuits 1, 3, 5, 6, and 7 combine the outputs of the symbol sequencer with a tabular message signal to produce a B-feature signal (through OR_1) at the time when a B character is to be displayed. The same signal is used as a generation control signal for the characters.

The B-feature signal is connected to the timer in order to produce defocus, focus, intensity, and other signals necessary for the generation of a B character.

Character-transfer signals are developed (in the B feature) at the end of the generation of each B character, in a TD tabular message display cycle, in order to replace the bits in the character register with those of the next character to be generated. The bits are transferred from the word 0 storage section. The characters which are displayed immediately after the B_1 character are A_3 (which follows B_1), A_4 (which follows B_2), D_1 which follows B_3), A_6 (which follows B_4), and C_1 (which follows B_5).

The transfer signals for the characters that follow the B character are passed through capacitor-diode gates 1 through 5. The gates are conditioned by the symbol sequence counts (developed in AND's 1, 3, 5, 6, and 7) that establish the overall generation control for the B character at the proper time in the display cycle. The transfer (from-storage-into-register) signal that senses each gate occurs at the timer count of 3, OD 1, which is when the generation of an individual character ends and when those flip-flops in the character register are ready for the bits of the next character to be generated.

3.2.6.2 TD Tabular Track Message

For track messages, the B feature is connected to the SDIE. It permits the selection of the B characters if desired by the operator for display.

3.2.6.3 TD Tabular Information Message

During a tabular information message, the B characters must be suppressed to prevent superposition with A characters (the A characters are forced). The B-feature signal is generated during this message, but it does not receive intensify gates except when a track message is being displayed.

3.2.6.4 TD Vector Message

The B feature also produces the signals required for the generation of the G_2 and G_3 characters and character-transfer signals for the character selection bits of G_3 and G_4.

AND's 2 and 4 combine symbol sequencer outputs with a vector-message signal in order to produce a G_2 or G_3 character-generation-control signal when the contents of the symbol sequencer are appropriate for generating G_2 and G_3 characters in a vector message. The G_2 or G_3 character-generation-control signals are passed through OR 1 (as the B-feature signal) and through the bypass feature to the timer to develop generation signals. The G characters have no display control at the feature selection switches; the G characters appear as forced displays on the consoles by the action (in the bypass feature) of the vector-message signal, which is connected into the bypass line throughout vector message display cycles.

Character-transfer signals are developed in the B feature at the end of the generation of G_2 and G_3. The bits are transferred from the word 0 storage section. The characters which are displayed immediately after the B

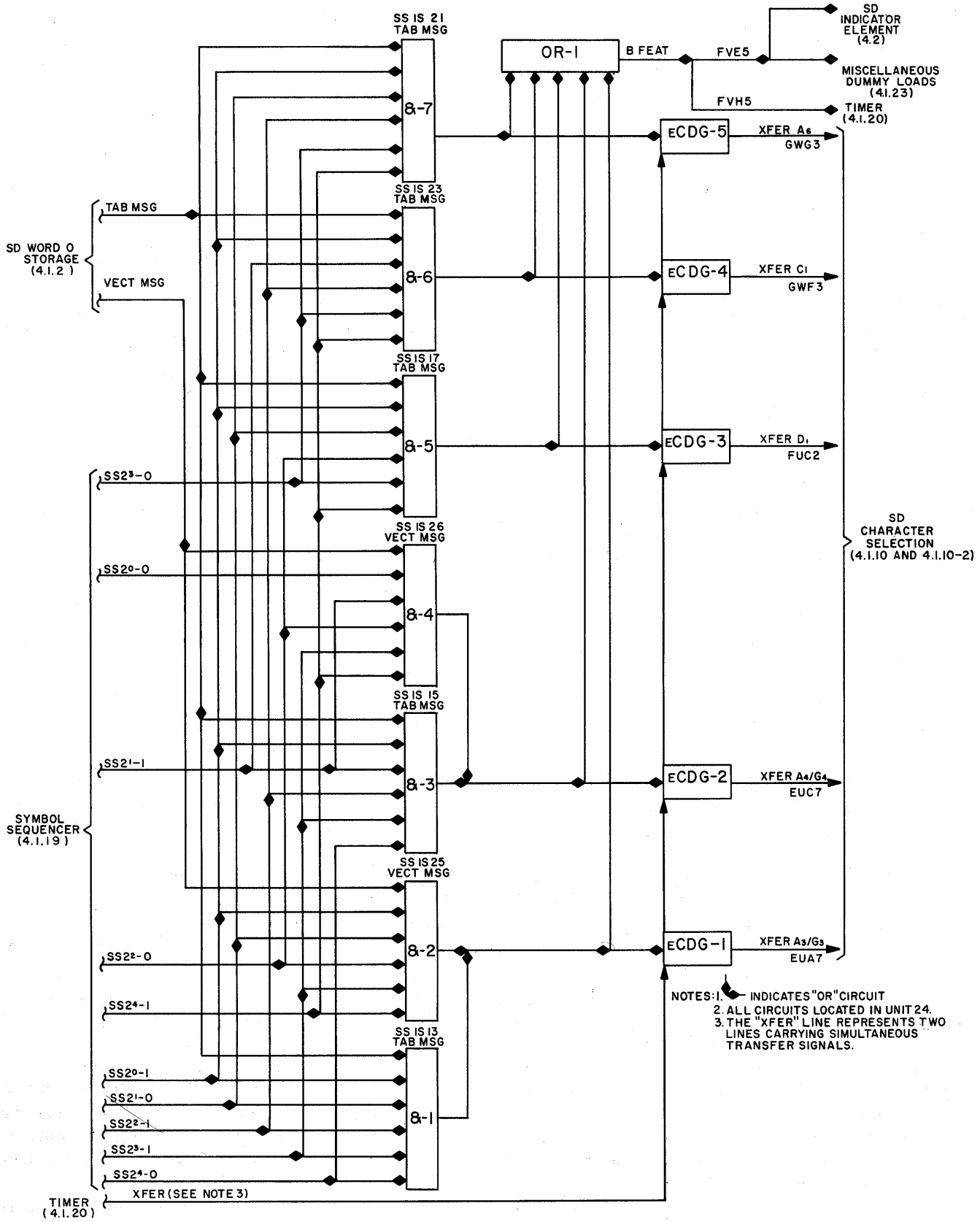


Figure 4–83. B Feature Circuit, Logic Diagram

characters are G_3 (which follows G_2) and G_4 (which follows G_3).

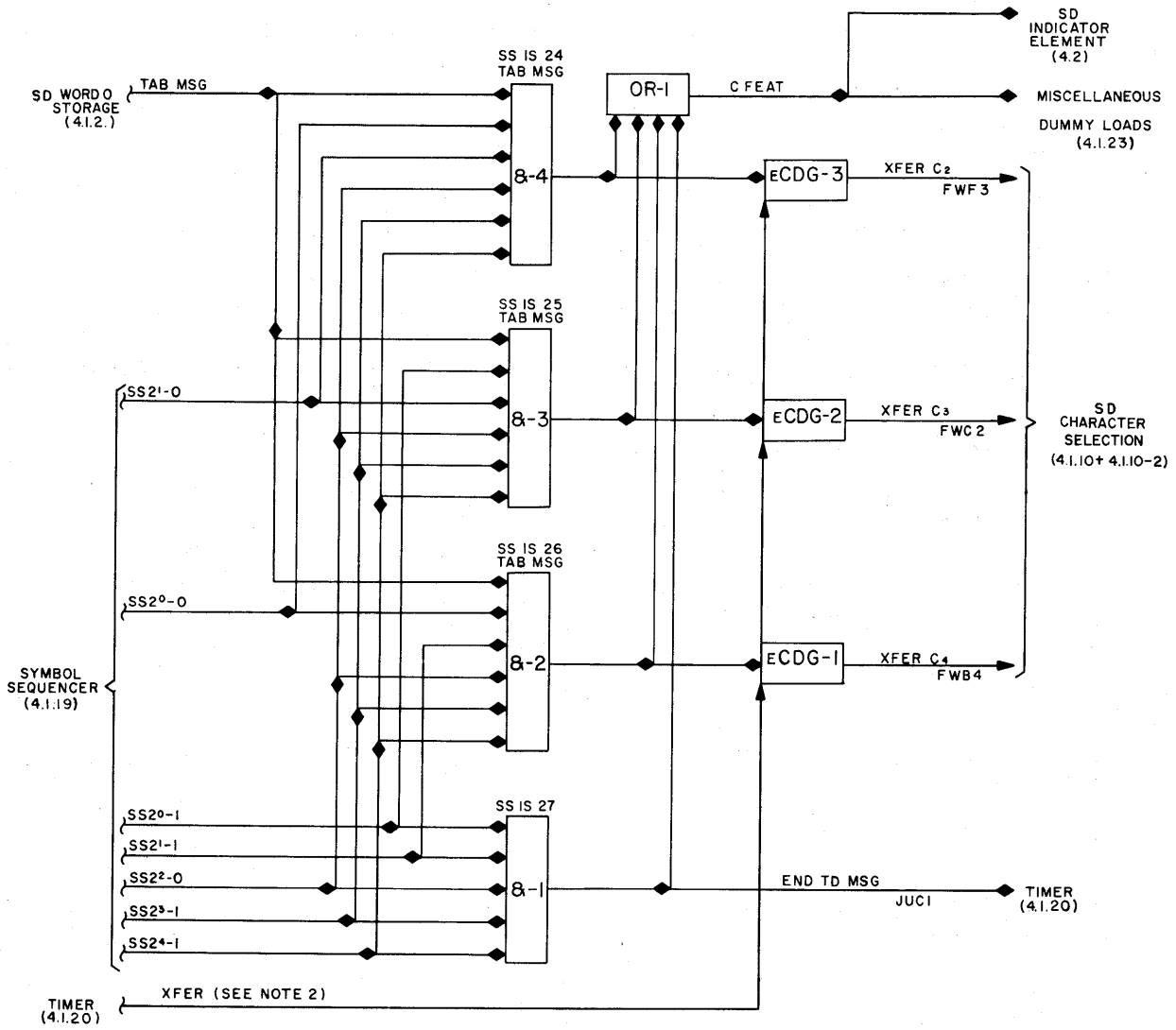
Capacitor-diode gate (CDG) 1 is used to pass the character-transfer signals for both A_3 and G_3; CDG 2 is used to pass the character-transfer signals for both A_4 and G_4. These common output circuits can be used since the bits selecting the A_3 and A_4 characters in a tabular message are stored in the same flip-flops (in word 0 storage) that store the G_3 and G_4 characters of a vector message.

3.2.7 C Feature Circuit

The C feature circuit generates control signals for the display of the C characters of a TD tabular message and the G_4 character of a TD vector message. Character-transfer signals required for the TD tabular message are also produced along with an end-TD-message signal.

3.2.7.1 TD Tabular Message

The C feature operates under control of the symbol sequencer to produce the signals required to generate the C characters (C_1 through C_4) in a TD tabular message display cycle. The signals are the C-feature signal (connected to the consoles of the SDIE) and character-transfer signals which occur at the end of the generation of the C characters in order to place bits in the character register for the next character to be displayed. The C feature also produces the end-TD-message signal for the termination of the TD display cycle. Figure 4–84 is a logic diagram of the C feature circuit.



NOTES: 1. ALL CIRCUITS LOCATED IN UNIT 24.
2. THE "XFER" LINE REPRESENTS TWO LINES CARRYING SIMULTANEOUS TRANSFER SIGNALS.

Figure 4–84. C Feature Circuit, Logic Diagram

AND circuits 2 to 4 combine the outputs of the counter flip-flops in the symbol sequencer with a tabular message signal in order to produce a C-feature signal (through OR 1) at the symbol sequencer counts in a tabular message display cycle when characters C_1 to C_3 are to be generated. AND 1 combines the symbol sequencer outputs at the count of 27 ($SS2^4 = 1$, $SS^3 = 1$, $SS2^2 - 0$, $SS2^1 = SS2^0 = 1$) to produce (through OR 1) a C-feature signal during a tabular message display cycle for the generation of C4.

The C-feature signal is not connected through the bypass feature to the timer in order to produce the signals necessary for the generation of the C_1 to C_4 characters. Instead, symbol-sequencer signals $SS2^4$–1 and $SS2^3$–1 are AND'ed (in the timer) and applied through the bypass feature circuit for C generation control. The two signals coincide only for SS counts 24 through 27 (11000 through 11001), at which time the C_1 to C_4 characters are displayed.

Character-transfer signals are developed in the C feature at the end of the generation of characters C_1 to C_3 in a tabular message display cycle. This is done to replace the bits in the character register with those of the next character to be generated. The bits are transferred from the word storage section. The characters which are displayed immediately after characters C_1 to C_3 are C_2 (which follows C_1), C_3 (which follows C_2), and C_4 (which follows C_3). The character-transfer signals for C_2, C_3, and C_4 are passed through capacitor-diode gates 1 to 3. The gates are conditioned by the counts from the symbol sequencer (developed in AND's 2, 3, and 4) that establish the feature signal for C_1, C_2, and C_3. The transfer (from-storage-into-register) signal that senses each gate occurs at the timer count of 3, OD 1, which is the time when the generation of an individual character ends and when the flip-flops in the character register are ready for the bits of the next character to be displayed.

The end-TD-message signal provides the conditioning level for producing the end-cycle signal in the timer after the last character of a TD message has been generated. The end-track-data signal corresponds to the generation control for the C_4 character and is raised by AND 1 at the count of 27 from the symbol sequencer.

3.2.7.2 TD Tabular Track Message

During a TD tabular track message display cycle, the C characters may be selected for display at the console. The C-feature signal is connected to the SDIE for this purpose.

3.2.7.3 TD Tabular Information Message

During the display of a TD tabular information message, the display of the C characters is forced by the bypass-feature signal generated from $SS2^4$–1 and $SS2^3$–1. (Refer to 3.2.7.1.)

3.2.7.4 TD Vector Message

Generation control for the G characters (which are displayed during SS counts of 24 through 27) is accomplished in the same manner as for C characters. (Refer

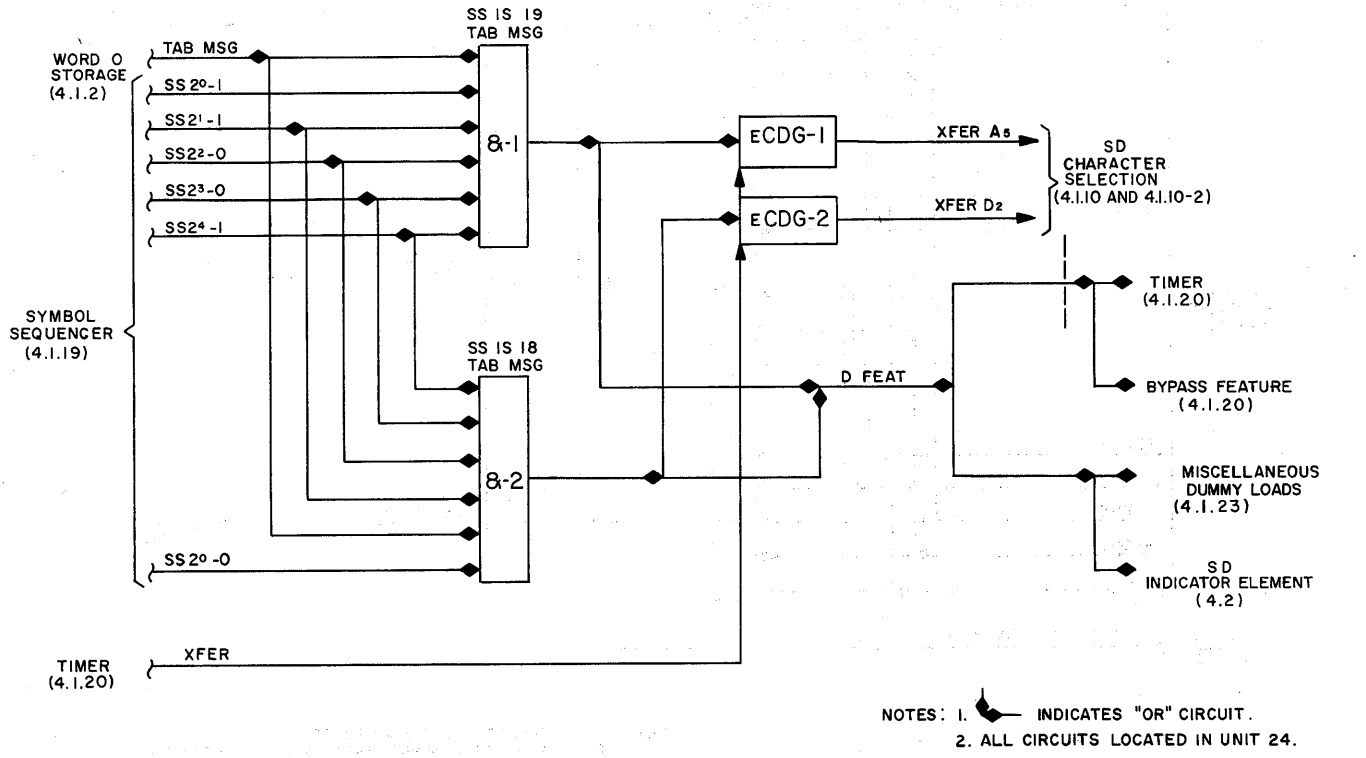


Figure 4–85. D Feature Circuit, Logic Diagram

to 3.2.7.1.) No feature signal is required since the whole message is forced.

The end-TD-message signal corresponds to the generation control for the G_4 character and is raised by AND 1 at the symbol sequencer count of 27. This signal is applied to the timer where it produces the end-cycle signal.

3.2.8 D Feature Circuit (TD Tabular Message)

The D feature operates under control of the symbol sequencer to produce the signals necessary to generate characters D_1 and D_2 in a TD tabular message display cycle. The signals consist of the D-feature signal (connected to the consoles of the SDIE through the bypass feature to the timer) and character-transfer signals which occur at the end of the generation of characters D_1 and D_2. This transfer signal enables bits to be placed in the character register for the next character to be displayed. Figure 4–85 is a logic diagram of the D feature circuit.

AND circuits 1 and 2 combine the symbol sequencer outputs with a tabular message signal in order to produce a D-feature signal (through OR 1) when characters D_1 and D_2 are to be displayed. The D-feature signal is also connected through the bypass feature to the timer in order to produce the defocus, intensity, and other signals necessary for the generation of a character.

3.2.8.1 TD Tabular Track Message

The D-feature signal is connected to the feature selection switches on the consoles of the SDIE. This permits the operator to control the D characters. These may either be displayed or suppressed, depending on the position of the switch.

3.2.8.2 TD Tabular Information Message

The D characters are forced during the display of a tabular information message. The D feature is used in the bypass feature circuit to generate the bypass-feature signal which forces the display.

3.2.9 E Feature Circuit

The E feature circuit generates the E feature which controls the display of the E character in a TD tabular message. The set-point signal generated by the circuit is used to select the point. The point is displayed in the TD tabular track message. It is also used to generate the vector in a TD tabular track message and the vectors in a TD vector message.

3.2.9.1 TD Tabular Message

The E feature operates under control of the symbol sequencer to produce the signals required to generate the E character (usually a symbol) in TD tabular message display cycles. The signals consist of the E-feature signal (connected to the consoles in the SDIE and to the bypass feature) and the set-point signal. The set-point signal sets digital voltages in the character register for selecting the point. The point is then displayed and swept to display the single vector in a TD tabular track message. Figure 4–86 is a logic diagram of the E feature. The counts of 4 through 7 from the symbol sequencer raise the E-feature signal in AND 1, and the count of 8 raises the signal in AND 2. The feature

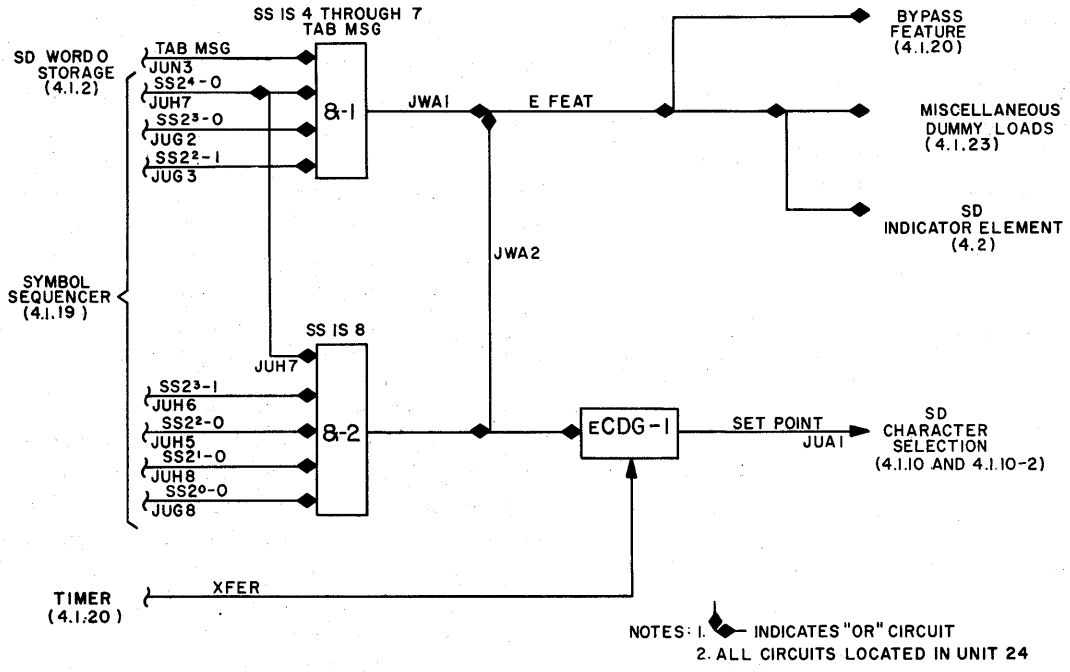


Figure 4–86. E Feature Circuit, Logic Diagram

signal produced during these counts (4-7) corresponds to the 50-μsec period required for the generation of a feature.

The E-feature signal is connected through the bypass feature to the timer in order to produce the defocus, intensity, and other signals necessary for the generation of the E character. During the generation of tabular information messages, the E character generation control is also connected into the bypass line in the bypass features to force the display of the E character.

3.2.9.2 TD Tabular Track Message

The E-feature signal is connected to the SDIE. It permits the selection of the E character for display.

The set-point signal places the bits in the character register to indicate prominently the point of origin of the vector in a TD tabular track message (the latest position of a target being tracked). The same character is swept to produce the single vector in a TD tabular track message. The voltages for the point are placed in the character register when the symbol sequencer is at 8 and the timer is at 3, OD 1. AND 2 in the E feature delivers the symbol-sequencer count to capacitor-diode gate 1; the gate is pulsed by the transfer (from-storage-into-register) signal from the timer, which occurs at the timer count of 3, OD 1. The output of CDG 1 is then connected to the 1 side of all flip-flops in the character register. (The binary address of the aperture in the character-forming matrix through which the beam is passed is 111 on the x axis and 111 on the y axis.)

3.2.9.3 TD Tabular Information Message

The E-feature signal is generated during a TD tabular information message. It is used in the bypass feature circuit to generate the bypass-feature signal which forces the display of the E character.

The set-point signal is generated during a TD tabular message. However, intensification of the point or vector does not occur because the required point-feature signal is not generated during a TD tabular information message.

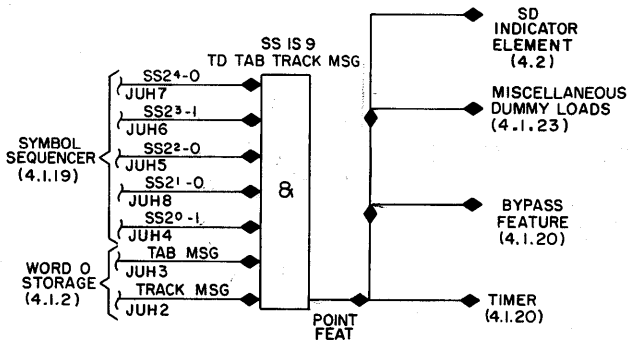


Figure 4–87. Point Feature Circuit, Logic Diagram

3.2.9.4 TD Vector Message

The set-point signal produced by the E feature is also used to place the digital voltages in the character register. The point signal is swept to display the four vectors of a TD vector message.

3.2.10 Point Feature Circuit (TD Tabular Message)

The point feature operates under control of the symbol sequencer to produce the signal required to generate the point and vector in a tabular track message display cycle. The circuit consists of one AND circuit. This circuit combines the symbol sequence outputs at the count of 9 and the tabular-and-track-message signals. These produce the point-feature signal for a generation control for both the point and vector of a TD tabular track message. (See fig. 4–87.) The output of the AND circuit is connected to the timer where the signal controls the intensity, vector-off, conditional-sample, and blank and unblank (for light gun use) signals in the generation of the point and vector. The output of the AND circuit is also connected (the point-feature signal) to the bypass feature which is connected to the consoles of the SDIE. In the bypass feature, the point-feature signal sets a flip-flop which establishes a level on the bypass line to the console feature selection switches for the entire period of generation of the point and vector. (See 3.2.14.1 and accompanying figure.)

The connection of the point-feature signal directly to the consoles permits a selection to be made of the bright point at the origin of the vector in the following manner. The point-feature signal is raised by the symbol sequence count of 9. The point-feature signal, however, does not raise the bypass-feature signal until the succeeding timer count of 7 is reached. During the interval preceding the bypass-feature signal, the display of the bright point at the origin of the vector may be selected by AND'ing the point-feature signal in the console with the trigger voltage of the light gun. When the bypass-feature signal does occur, it produces a forced display of the vector, which is generated after the point in a TD tabular track message cycle.

3.2.11 Bypass Feature Circuit

The bypass feature channels the generation-control (feature) signals of the characters in TD tabular messages to the timer. There, the signals are combined with timer counts to produce the specific signals (defocus, intensity, etc.) required for the display of a character. The bypass feature also produces the bypass-feature signal by connecting the character-generation-control signals into the bypass wire that forces the display around the feature selection switches on the consoles

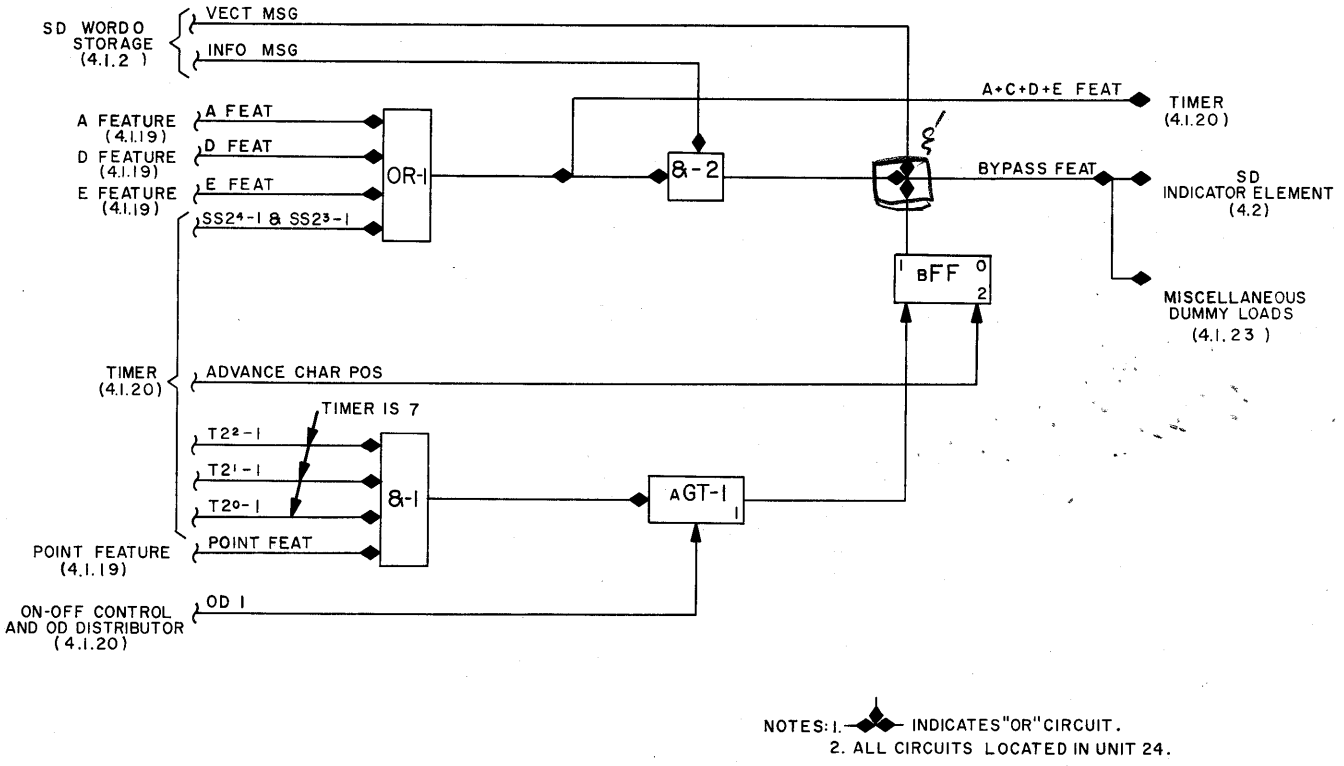


Figure 4–88. Bypass Feature Circuit, Logic Diagram

of the SDIE. Figure 4–88 is a logic diagram of the bypass feature circuit.

3.2.11.1 TD Tabular Message

The generation control signals for the A(G), C, D, and E characters are connected to the timer through OR 1. These are the A-, D-, and E-feature signals and the $SS2^4$-1 and $SS2^3$-1 signal (equivalent to the C-feature signal (par. 3.2.7.1).

The bypass-feature signal is required for the tabular messages, or parts of TD tabular messages, over which the console operators are to have no selective control. In such cases, the bypass-feature signal forces the displays on the consoles by effectively short-circuiting the feature selection switches.

3.2.11.2 TD Tabular Track Message

Only the display of the vector of a TD tabular track message is forced. A flip-flop is driven to its 1 output by the point-feature signal (which arises at the symbol sequencer count of 9) coincident with the timer count of 7, OD 1 (AND 1 and gate 1). The bypass-feature signal persists until the flip-flop is driven to its 0 output by the first advance-character-position signal in a TD tabular message. The advance-character-position signal occurs after the completion of the generation of the vector. (See fig. 4–93, foldout.)

3.2.11.3 TD Tabular Information Message

The display of the A, C, D, and E characters of a TD tabular information message is forced. The A-,C-,D-, or E-feature signals are applied through OR 1 to AND 2. When the information-message signal is also applied to AND 2, the bypass-feature signal is generated.

3.2.11.4 TD Vector Message

The A-, B-, C-, and E-feature signals are applied to the timer for generation control of the G characters. The vector-message signal is passed through an OR circuit as the bypass-feature signal. It forces the display of the whole TD vector message.

3.2.12 Vector Control Circuit

The vector control operates under the regulation of the symbol sequencer to produce signals required to generate the vectors of TD messages. The signals consist of the starting and stopping signals for the four vectors in a vector message, the stopping signal for the single vector in a tabular message, and transfer signals. The transfer signals occur at the end of the vectors in order to transfer (from storage) the bits of the next vector or character to be generated into the registers of the generator in a TD message display cycle. Figure 4–89 is a logic diagram of the vector control circuit. Vector control circuit outputs are not

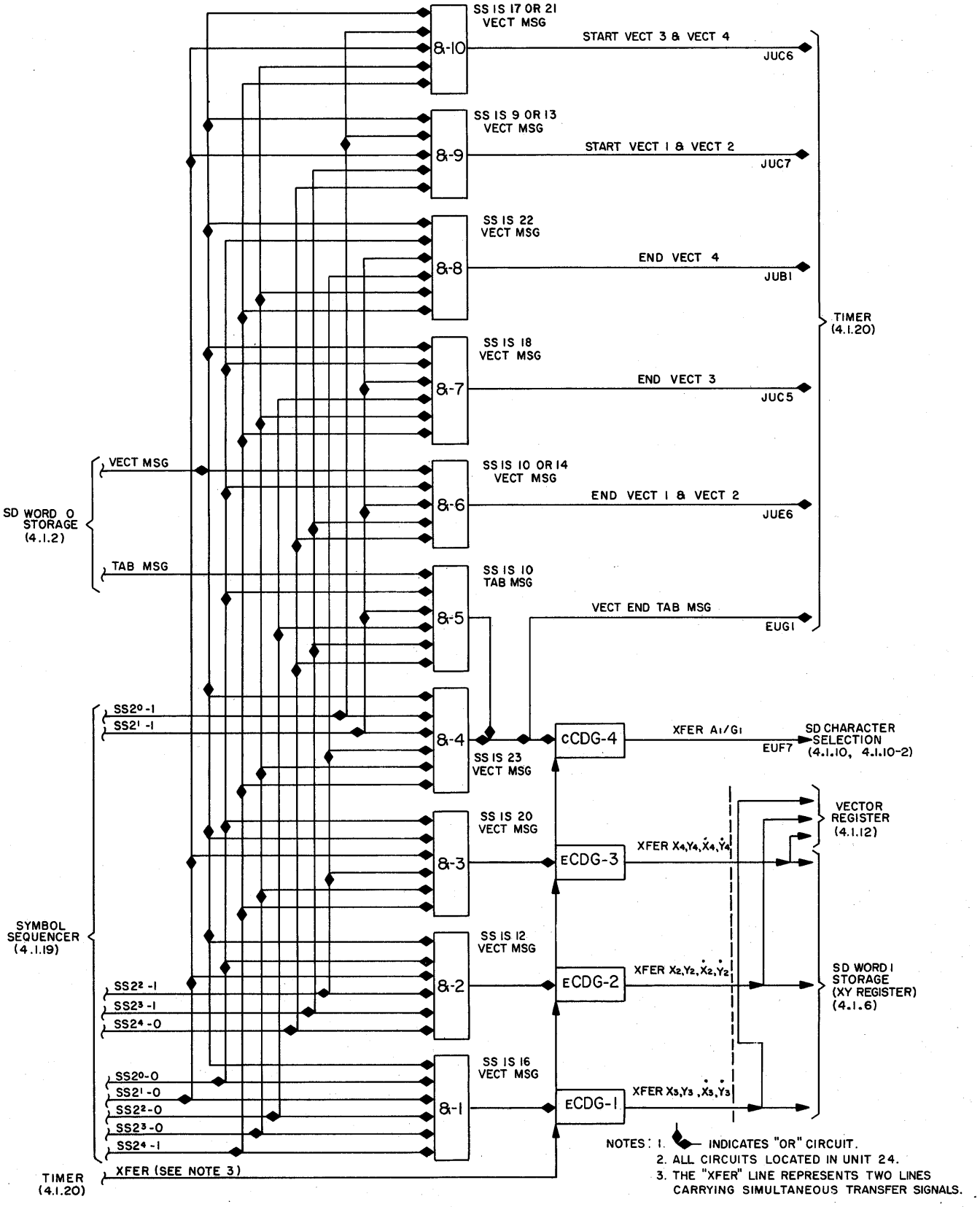


Figure 4–89. Vector Control, Logic Diagram

required for RD messages. For TD tabular information messages, only the transfer-A signal is used.

3.2.12.1 TD Tabular Message

The start-vector signal for the single vector in a tabular track message is developed in the timer by the point-feature signal from the point feature circuit.

The end-vector signal is raised by the output of AND 5 which combines the symbol sequencer outputs at the count 10 during a TD tabular message display cycle. The signals are connected to the timer to raise the vector-off signal, remove the intensity signal, and develop other signals at the proper timer count.

The vector appears as a forced display on the consoles of the SDIE and requires raising of a signal level in the bypass feature circuit to bypass the feature selection switches of the consoles. For the single vector in a tabular message, the bypass-feature signal is developed in the bypass feature circuit from the point-feature signal (from the point feature circuit).

A transfer signal occurs at the end of vector generation in order to transfer (from storage) the bits of the A_1 character into the registers of the generator. (The X, Y and $\dot{X}$, $\dot{Y}$ voltages for the vector are placed directly in the XY and vector registers as the message is read from the drum under control of the gate generator.) The bits which select the point that is swept to produce the vectors are placed in the character register at the symbol sequencer count of 8 by the set-point signal from the E feature circuit.

AND 5 combines the outputs of the symbol sequencer to develop the A_1 character-transfer signal after vector generation is completed in TD tabular message display cycles. At this time, the character register is ready for the digital voltages for the first character to be generated (A_1) after the vector. AND 5 produces an output at the symbol sequencer count of 10, which is then passed through CDG 4 by the transfer (from storage into register) signal at the timer count of 3, OD 1. The symbol sequencer count of 10, timer count of 3, and OD 1 time correspond to the time in a tabular track message display cycle when the generation of the single vector in a message has been completed and the generation of the A_1 character is to begin. (See 3.2.14.1 of this section and fig. 4–93.)

The transfer A_1 output from CDG 4 is connected to the gates in the character register that admit the bits for the A_1 character. The transfer-A signal is also used for TD tabular information messages.

3.2.12.2 TD Vector Message

The start-vector signals for the four vectors of a vector message are raised by the outputs of AND's 9 and 10 which combine the symbol sequencer outputs at the counts during a TD vector message display cycle when the vectors are to begin. The start-vector signals are connected to the timer where they serve as generation controls in removing the vector-off signal and in raising the intensify signals at the proper timer counts.

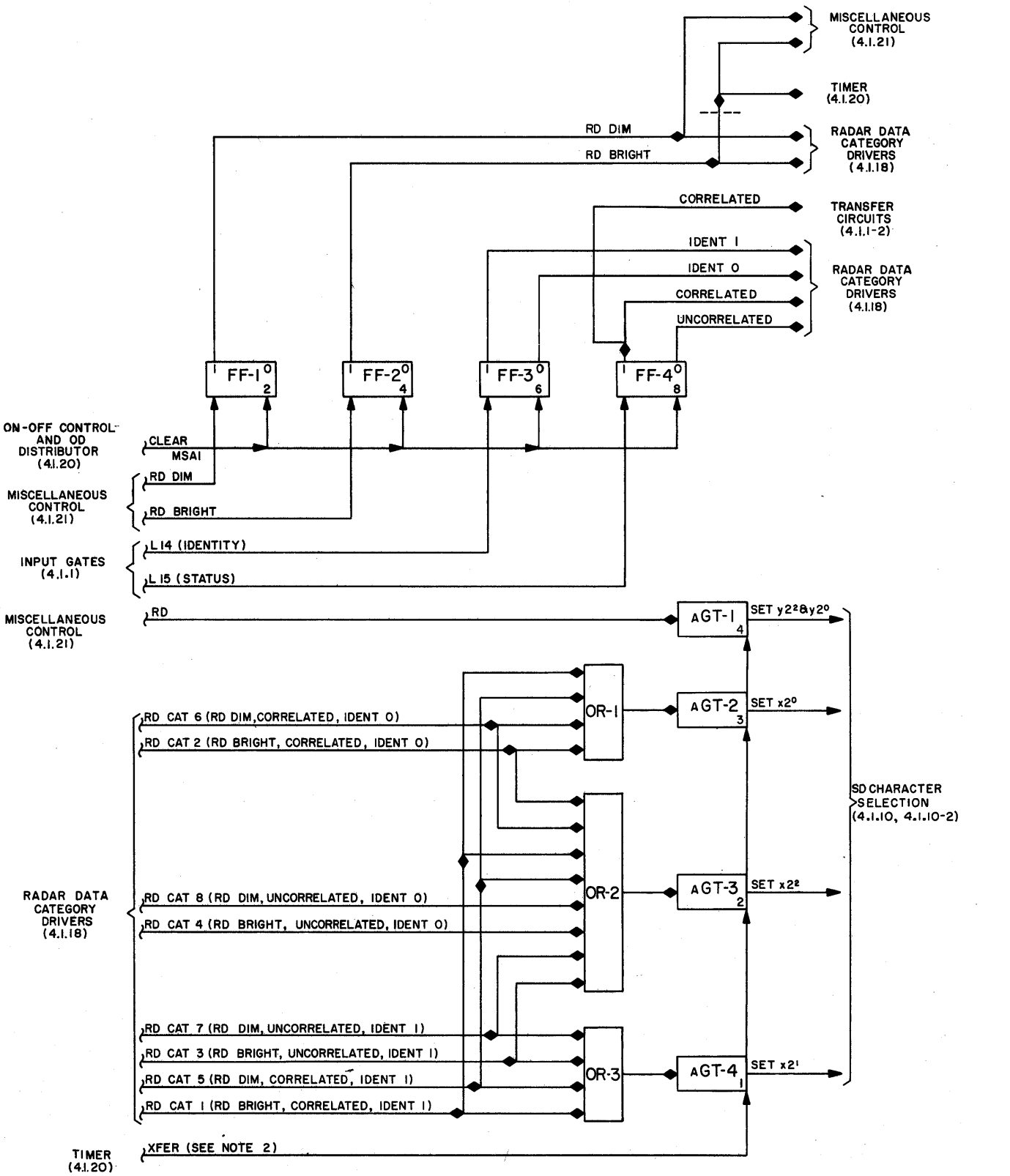
The end-vector signals are raised by the outputs of AND's 6 to 8 which combine the symbol sequencer outputs at the counts during a TD vector message display cycle when the vectors are to end. The start-and-end-vector signals are connected to the timer.

AND circuits 1 to 3 combine the outputs of the counter flip-flops in the symbol sequencer, at the counts in a vector message display cycle, when the X, Y and $\dot{X}$, $\dot{Y}$ voltages of the second, third, and fourth vectors are to be placed in the XY and vector registers. The outputs of the AND circuits are pulsed through capacitor-diode gates 1 to 3 by the transfer (from-storage-to-register) signal and then connected to the admittance gates in the registers that pass the voltages of each vector. (The X, Y and $\dot{X}$, $\dot{Y}$ voltages for the first vector of vector messages are placed directly in the registers as the messages are read from the drum under control of the gate generator.) The bits which select the point that is swept to produce the vectors are placed in the character register at the symbol sequencer count of 8 by the set-point signal from the E feature.

After all vector generation is completed, AND 4 combines the outputs of the counter flip-flops in the symbol sequencer to develop the transfer-G_1 signal. AND 4 and capacitor-diode gate 4 produce an output at the symbol sequencer-count of 23, timer count of 3, OD 1, which is the time in a TD vector message display cycle when the generation of the fourth vector in the message has been completed and the generation of the G_1 character is to begin. The G_1 character bit admission gates are connected to capacitor-diode gate 4, in common with the A_1 character gates. This is possible because both characters share the same word 0 storage flip-flops.

3.2.13 RD Control Circuit

The RD control contains flip-flops that develop the following six signals for regulating the generation of RD messages: RD-bright or RD-dim signal, corresponding to the most recent or to an earlier return on a target; correlated or uncorrelated signal, corresponding to the correlated or uncorrelated condition of the target return in the air defense situation; and identity 1 or identity 0 signal, which identifies the source of the radar data. The RD control also contains circuits for developing the bits which select characters to be displayed for the eight categories of RD messages. The categories themselves are developed by AND'ing combinations (RD-bright or -dim, correlated or uncorrelated, and identity 1 or 0) of RD message control signals in the RD category drivers section. Figure 4–90 is a logic diagram of the RD control circuit.



NOTES: 1. ALL CIRCUITS LOCATED IN UNIT 24.
2. THE "XFER" LINE REPRESENTS TWO LINES CARRYING SIMULTANEOUS TRANSFER SIGNALS.

Figure 4–90. Radar Data Control Circuit, Logic Diagram

3.2.13.1 Radar Data Message Control Signals

The six RD message control signals are developed by the RD control circuit. The RD-bright (or RD-dim) level is raised by the RD-bright (or RD-dim) pulse which is connected from the RD drum through the miscellaneous control to the 1 side of FF 2 (or 1) in the RD control. An RD-bright pulse is sent along with each RD message being read from the RD drum field which was last written on by the Central Computer System. An RD-dim pulse is sent along with each RD message being read from the seven fields of the RD drum which were written on previous to the field last written on by the Central Computer System. Neither an RD-dim nor an RD-bright pulse accompanies an RD message from a field chosen by the Central Computer System for writing upon while the Display System is reading the field. The correlated or uncorrelated signal of an RD message is developed by the information in control bit L15 of the message. The bit is connected from the RD drum through the input gates section to the 1 side of FF 4. A 1 in the bit will raise the 1 side of the flip-flop, establishing the fact that the target described in the RD message has been correlated in the air defense problem. When the bit is a 0, the 0 side of the flip-flop remains up, which is the condition to which it was driven by the clear pulse at the end of the last RD message display cycle. The 0 output of the flip-flop indicates that the target described in the RD message remains uncorrelated in the problem.

The identity 1 or 0 signal of an RD message is developed by the information in control bit L14 of the message. The bit is connected from the RD drum through the input gates section to the 1 side of FF 3. A 1 bit will raise the 1 side of the flip-flop, indicating that the answer to the query of the radar return is of the identity 1 type. When the bit is a 0, the 0 side of the flip-flop remains up, which is the condition established by the clear pulse at the end of the last RD message display cycle. The 0 output of FF 3 signifies that no answer to the query was received from the radar return, indicating that the target is of the identity 0 type.

The six RD message control signals occur in three pairs of mutually exclusive signals; that is, only one signal of each pair is present for each RD message read into the SDGE. (Neither signal, however, accompanies an RD message from a field chosen by the Central Computer System for writing upon while the Display System is reading the field.) The eight different combinations of the three signals present for an RD message are given in table 4–12.

These eight combinations are known as RD message categories. The actual combining of the control signals to make up the categories occurs in the RD category drivers to which the control signals from the RD control circuits are connected. A total of 20 lines, 8 categories and 12 mixed categories, are connected to the SDIE. The RD category signal is also connected back to the RD control circuit where the signal is encoded into the character selection bits corresponding to the RD category.

3.2.13.2 RD Message Character Selection Signals

The signals that select the character to be displayed for an RD message are developed in the RD control circuit. Four characters are used to represent the eight categories. One character represents both the bright and dim category for the same identity and correlation of two categories. For example, the same character is used in the display of an RD-bright, correlated, and

TABLE 4–12. SD CHARACTER-FORMING MATRIX ADDRESSES OF RD MESSAGE CHARACTERS

RADAR DATA CATEGORY		HORIZONTAL MATRIX ADDRESS	VERTICAL MATRIX ADDRESS
1	RD bright, correlated, and identity 1	111	101
2	RD bright, correlated, and identity 0	101	101
3	RD bright, uncorrelated, and identity 1	110	101
4	RD bright, uncorrelated, and identity 0	100	101
5	RD dim, correlated, and identity 1	111	101
6	RD dim, correlated, and identity 0	101	101
7	RD dim, uncorrelated, and identity 1	110	101
8	RD dim, uncorrelated, and identity 0	100	101

identity 1 category and RD-dim, correlated, and identity 1 category (RD categories 1 and 5, respectively). The bright or dim characteristic of a category is reintroduced at the console by the radar category selection switches.

The bits for selecting the four characters that display RD message categories are encoded in the radar control circuit. The four characters are located in the horizontal row with the y binary address 101 of the character-forming matrix in an SD CRT. Therefore, for the vertical selection of radar categories, it is necessary only to place the address 101 in the flip-flops of the character register whenever a radar message is being generated. The setting of binary 101 in the flip-flops is accomplished by gating the transfer (from-storage-into-register) signal passing through gate 1. The gate tube is conditioned by the RD signal which is the generation control for RD messages and is present during the display of all RD messages. The resulting output pulse from gate 1 places a 1 in the $y2^2$ and $y2^0$ flip-flops of the character register. Flip-flop $y2^1$ maintains the 0 output which was developed by the clear pulse at the end of the previous message display cycle. Therefore, the complete y selection address in the register is 101, which is then converted into analog voltages in the character selection decoder and line drivers and applied to the vertical character selection plates of the SD CRT's.

The horizontal selection addresses for RD message category characters are binary 100, 101, 110, and 111. To obtain any one of these addresses, an RD message category signal is connected to the encoding network consisting of OR's 1, 2, and 3. The network develops digital voltages corresponding to the specific RD message category signal connected to the network. The digital voltages from the network condition gates 2, 3, and 4 which permits the digital voltages to be transferred to the character selection register upon receipt of the transfer pulse from the timer. The digital voltages are then converted into analog voltages in the character selection decoder and line drivers and applied to horizontal character selection plates in the SD CRT's. Note that only 1's are placed in the flip-flops because 0's are already present as a result of the previous clearing. (See table 4–12.)

The x and y addresses (to select the character to be displayed for an RD message category) are applied to the character selection at the same time. The transfer pulse which gates the x address also gates the y address to the x and y character selection decoders and line drivers.

3.2.13.3 Other Outputs

Other outputs from the RD control are the correlated signal to the transfer circuits section, the RD-bright signal to the timer, and the RD-bright and RD-dim level signals to the miscellaneous control.

The transfer circuits section and the timer use the signals from the RD control in sending radar data from the SDGE to the Central Computer System through the MI element. The miscellaneous control uses the signals from the RD control to develop the overall display signal for RD messages.

3.2.14 Timer Circuit

The timer contains one of the three major counting control circuits in the SD timing and control section. The other two major counting control circuits are contained in the on-off control and OD distributor and in the symbol sequencer. The counter in the OD distributor separates and channels the OD pulses (OD 1, 2, 3, and 4) received at 2.5-μsec intervals on one wire from the Drum System. The OD 1, 3, and 4 pulses are used in the timer to synchronize the sensing of various output gates. The counter in the symbol sequencer divides the time of a TD message display cycle in order to generate separate displays of the different vectors and characters in the message. The counter in the timer develops command signals during the generation of each of the separate displays in a TD message display cycle and the single display in an RD message display cycle. This is done in order to operate the circuits required to generate an individual display. Examples of such command signals are the transfer (from-storage-into-register) signal and the SD defocus, intensify, and focus.

The description of the timer, which follows, covers TD tabular, TD vector, and the RD messages separately. It deals first with the counting circuit itself and then with the development of each command signal. Figure 4–91 shows the basic overall timing of the SD cycle; figure 4–92, foldout, is a logic diagram of the timer. The command signals produced by the timer are listed below and are described in that order:

a. Vector off
b. SD intensity
c. Clear XY register and vector register
d. Advance character position
e. Transfer (from storage into register)
f. SD focus and defocus
g. Clear character register
h. Timer is 3
i. Conditional blank, unblank, and conditional sample
j. End cycle

3.2.14.1 TD Tabular Message

The timing of the display cycle of the TD tabular message is shown in figure 4–93, foldout. The counter and command signals produced during such messages are discussed in 3.2.14.2 through 3.2.14.12.

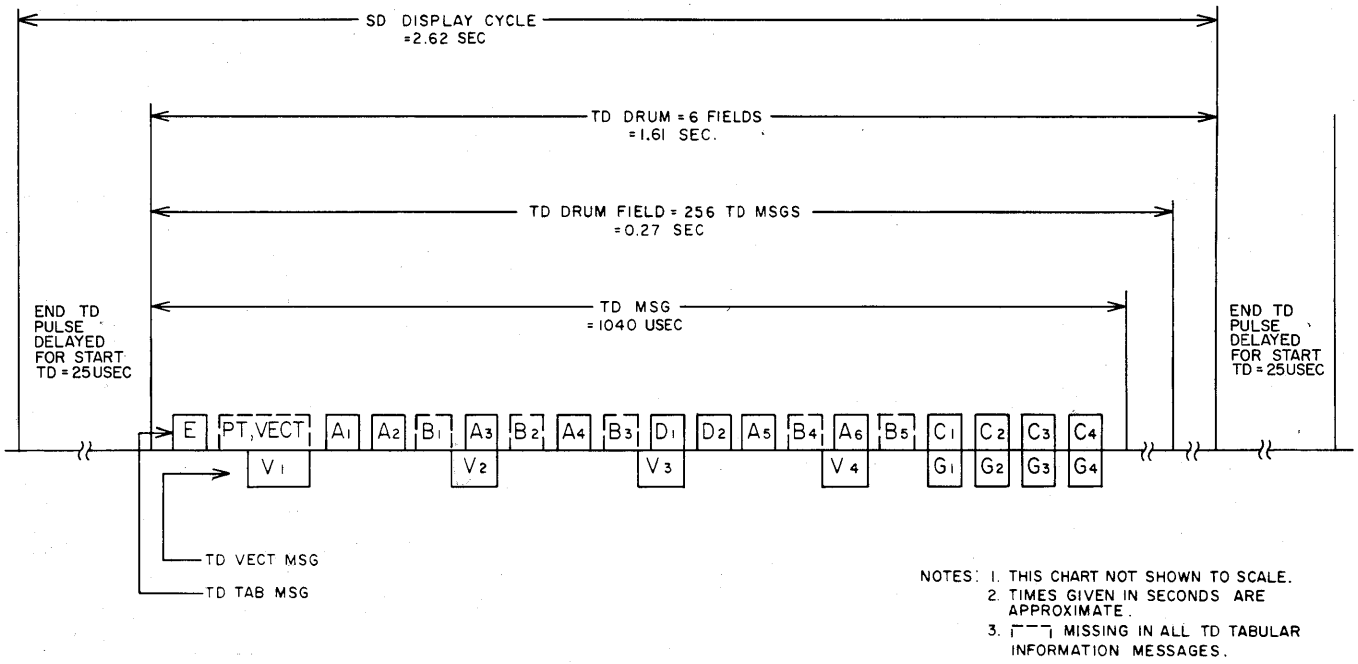


Figure 4–91. SD Cycle

3.2.14.2 Timer Counter, TD Tabular Message

The counting circuit in the timer consists of flip-flops, gates, and OR circuits. The timer is cleared when the SDGE is not receiving information from drums or during test from the DTE.

The actual counting occurs in FF's 1, 2, and 3 and GT's 5 and 6. The counter is stepped by OD 3 pulses from the drum. During a TD tabular message display cycle (1,040 μsec in duration, as shown in fig. 4–93), the timer counter counts from 0 to 7 at the beginning of the cycle and then from 3 to 7 repeatedly until the cycle ends at the count of 3.

The OD 3 stepping pulse to the counting flip-flops normally is applied as a complementing signal to FF 1, which is the $T2^0$ flip-flop. The symbol $T2^0$ represents the 2^0 digit from the timer counter. (In discussing the timer, symbols of this type will also be used for the other digits of the counter.) The stepping pulse is gated by a timer-is-not-7 signal (from OR 1) in order to permit continuous counting until 7 is reached. When this occurs, the OD 3 stepping pulse is applied through gate 3 (which is conditioned by a timer-is-7 signal from AND 1) to the 0 side of the $T2^2$ flip-flop (FF 3). Since the counter is 7 at this time and each flip-flop is producing a 1 output ($T2^2$–1, $T2^1$–1, $T2^0$–1), placing a 0 in flip-flop $T2^2$ sets the counter to 3 ($T2^2$–0, $T2^1$–1, $T2^0$–1). Succeeding OD 3 pulses then step the counter again from the count of 3 to the count of 7 through gate 1, which has been reconditioned by the timer-is-not-7 signal. The counting from 3 to 7 repeats until the message display cycle ends and clear pulses arrive from the on-off control and OD distributor circuits section.

The digital voltage outputs representing the counts from the flip-flops ($T2^2$–0 or $T2^2$–1, $T2^1$–0 or $T2^1$–1, $T2^0$–0 or $T2^0$–1) are AND'ed in the timer with other control signals from the SD timing and control section to produce the command signals for the specific displays of characters and vector in a message display cycle. The signals which coincide with timer count 7 are also applied to the bypass feature circuit.

At the beginning of a message display cycle, the counter is set to different levels to introduce the proper count into the circuit for the generation of TD or RD messages.

To allow for the arrival of each message from the Drum System with the proper sequence of timing, the timer counter is first set to 0. The setting of the counter to 0 is accomplished in two ways. The first method is accomplished by the start-TD signal (the RD drum-index pulse). The second is accomplished by a clear signal generated after each message display cycle.

The start-TD pulse is fed through OR circuits 3, 4, and 5 to clear the timer. The clear pulse, after the first TD message display cycle, is connected from the on-off control and OD distributor circuit to the 0 side of the $T2^0$ and $T2^1$ flip-flops through OR circuits 3 and 4. The clear pulse occurs at the end of the preceding TD message display cycle. Setting only these two flip-flops to 0 is sufficient to return the complete counter output to 0. (When the clear pulse is produced, the flip-flops are at the count

of 3: $T2^2$–0, $T2^1$–1, $T2^0$–1.) The clear pulse passes ungated through OR 3 to the $T2^0$ flip-flop. However, the clear pulse to $T2^1$ flip-flop is gated through gate 2 (and OR 4) which is conditioned by a TD signal. The TD signal is always present during the generation of a TD message. The purpose of the $T2^1$ flip-flop being gated is related to the clearing of the counter after RD message display cycles. The counter is set to 2 rather than 0, which is necessary for the beginning of RD message display cycles.

3.2.14.3 Vector-Off Signal (TD Tabular Message)

The vector-off signal is generated for the single vector in a TD tabular track message. This signal specifies the start and duration of the sweep signal to the vector generator.

Flip-flop 4, the vector control flip-flop, conditions the sweep generator in the vector generation circuit when the 1 output is down. Therefore, the start-vector signal clears FF 4 and generates a negative level to the sweep generator. The start-vector signal is produced in gate 7, which is pulsed by OD 3, and conditioned by AND 7. AND 7 is conditioned by the timer counter circuit containing 7 and a ready-to-start-vector signal from OR 6. The ready-to-start-vector signal is produced in OR 6 by the point-feature signal which originates in the point feature circuit.

The vector-off signal is raised (deconditioning the sweep generator) when FF 4 is driven to its 1 output state by the stop vector pulse from gate 8 at OD 3. Gate tube 8 is conditioned by the coincidence of the count of 7 from the timer counter ($T2^2$–1, $T2^1$–1, $T2^0$–1) and the ready-to-blank-and-stop-vector signal in AND 8. The ready-to-blank-and-stop-vector signal is produced in OR 7 which is conditioned by the vector end tabular message from the symbol sequencer. This signal also operates at every count of 7 to turn off the intensify signal after each separate display in the display cycle of all messages.

3.2.14.4 SD Intensify Gate (TD Tabular Message)

The SD intensify gate signal is a voltage level developed in the timer as an unblanking signal for the intensification circuits of the SD CRT's. The signal occurs independently of each of the characters, vectors, or symbols of an SD message as it appears on the viewing screen of the SD CRT's.

The intensify signal is produced in FF 5 when the 1 side is raised through OR 14 by the gated output signals from AND's 9, 10, and 11. The gating of the output signals from AND's 9, 10, and 11 occurs through gates 9, 10 (both pulsed by OD 1's), and 11 (pulsed by OD 4), respectively.

AND 9 routes the intensify signal for the A through E characters of TD messages to set the intensify flip-flop. This circuit produces its output signal when the count of 5 ($T2^2$–1, $T2^1$–0, $T2^0$–1) coincides with the message display signal and one of the following signals passed through OR 8:

a. A-, C-, D-, or E-feature signal. This signal is present whenever one of the characters indicated is to be generated in a TD message display cycle; the signal then serves as the overall generation control for the character.

b. B-feature signal coincident with a track-message signal in AND 2. These signals are present whenever one of the B characters is to be generated in a TD tabular track message display cycle. It also serves as the overall generation control for the character. Due to the required coincidence in AND 2, the SD intensify gate can arise only when control bit LS in word 0 of a tabular message is a 0 (indicating a track message).

AND 10 routes the intensify signal for the point and vector in a TD tabular message. The circuit produces an output signal when the timer count of 5 coincides with the display signal and point-feature signal. The point-feature signal provides intensification first for the point (from count of 5, OD 1, to the count of 7, OD 3), which is coincident with the origin of the vector, and then for the vector itself (which begins sweeping at the count of 7, OD 3). (Refer to fig. 4–93.)

The intensify signal is turned off after each of the characters or vectors of a TD tabular message has been individually displayed. This blanking occurs after 25 μsec for all characters and after 50 μsec for the vector. This is shown in figure 4–93. For all characters and vectors, the intensify signal is turned off at the count of 7, OD 3. The blanking actually arises when the 0 side of FF 5 is raised. The 0 side is raised by the output of AND 8 passing through gate 8 at OD 3. AND 8 produces its output signal when the count of 7 ($T2^2$–1, $T2^1$–1, $T2^0$–1) coincides with a ready-to-blank-and-stop-vector signal. The stop-vector portion of the ready-to-blank-and-stop vector signal takes effect through the parallel connection from gate 8 to the 0 side of vector-controlling FF 4.

The ready-to-blank-and-stop-vector signals are delivered to AND 8 through OR 7 as a result of one of the following input signals:

a. Vector-end in a tabular message, which originates in the vector control circuit, operates to end the sweep and blank the intensification of the vector in a tabular message.

b. A-, C-, D-, or E-feature signal. This signal is present as the overall generation control for all the characters indicated in its name.

c. B-feature signal. This signal is present as the overall generation control for all the B characters.

3.2.14.5 Clear-XY-Register-and-Vector-Register Signal (TD Tabular Message)

The clear-XY-register-and-vector-register signal is not required for TD tabular messages. The vector register is cleared by the first advance-character-position pulse at the end of the single vector. The XY register is cleared by the overall-clear pulse at the end of the display cycle.

3.2.14.6 Advance-Character-Position Signal (TD Tabular Message)

The advance-character-position signal is generated in the timer in order to step the X and Y position character in the character counter and positioning circuit. The counters provide the digital positioning voltages for the individual characters in the display format of tabular messages. The advance-character-position signals are sent to the counters each time a character is to be displayed in a different position of the format. The same signal is also applied to the on-off control and OD distributor, and bypass feature circuits. The relationship between the advance-character-position signals and the display timing of characters in TD tabular messages is shown in figure 4–93.

The pulse which originates in gate 16, when the timer count of 3 and OD 1 coincide, is applied to gate 15. When the pulse passes through gate 15, it is then the advance-character-position signal. Gate 15 is conditioned through OR 13 by one of the following signals:

a. Vector-end in a TD tabular message. This signal enables the advance-character-position signal to be sent to the character counter and positioning circuit. The circuit applies to the character positioning plates of the SD CRT's the necessary voltages for the first character position in a tabular message format (A_1).

b. The A_1 signal, which is generated in the A feature circuit, is the overall generation control of the A_1 character in a TD tabular message. The signal generates an advance-character-position signal which is sent to the character counter and positioning circuit. This circuit applies to the character positioning plates of the SD CRT'S the necessary voltages for positioning the A_2 and B_1 characters. One repositioning signal is used to place two characters in the character format. However, this does not result in their superposition on the viewing screen of an SD CRT. The proper wiring of the category plugboard prevents any such superposition.

c. The B-feature signal, which is the overall generation control for the B characters. This signal enables advance-character-position signals to be sent to the character counter and positioning circuit. This circuit applies to character position plates of the SD CRT's the necessary voltages for positioning A_3 or B_2 (two characters sharing the same format position), A_4 or B_3, D_1 or A_6, or B_5, and C_1.

d. The D-feature signal, which originates in the D feature circuit, is the overall generation control for the D_1 and D_2 characters. The D signal enables advance-character-position signals to be sent to the character counter and positioning circuit. This circuit applies to the character positioning plates of the SD CRT the necessary voltages for positioning D_2 and A_5 (or B_4) characters.

e. The $SS2^4$—1 and $SS2^3$—1 signal, coincident in AND 6, originates when the 1 side of 2^4 and 2^3 flip-flops in the symbol sequencer are present from the counts of 24 to 27 (11000 to 11011). The coincidence of $SS2^4$—1 and $SS2^3$—1 in AND 6 permits advance-character-position signals to be sent to the character counter and positioning circuit. This circuit applies to the character positioning plates of the SD CRT's the necessary voltages for positioning the C_2, C_3, and C_4 characters of a tabular message.

Advance-character-position signals are also used to clear the vector register after the display of the single vector in a TD tabular track message.

3.2.14.7 Transfer (from-Storage-into-Register) Signal (TD Tabular Message)

The transfer-from-storage-into-register signal is a constantly repeating pulse from the timer. This timer transfers the bits representing individual characters (x and y) (character-forming matrix selection voltage) from word storage into the character register. From the register, the information about one character is connected through a binary-to-analog decoder into the proper deflection system of the display tubes in the SDIE.

The transfer (from-storage-into-register) signal is used for the bits of all characters of a TD tabular message with the exception of the E character. The information bits for the E character are deposited into their character register as they are read from the drum without any intervening storage. A read-word-0 signal

from the gate generator controls the initial depositing of the character register.

The transfer signal is produced as the output of gate 16 at OD 1; gate 16 is conditioned by the timer count of 3. This signal is connected to the feature circuits where it passes through gates conditioned at the proper time in the display cycle by the symbol sequencer. From these gates the transfer pulses, which occur at the appropriate time, are connected to the character register input gates. These input gates are conditioned by the bits in word storage. From there, the bits are transferred to the character register. (However, the set-point signal is applied directly to the register flip-flops.)

3.2.14.8 SD Focus and Defocus Gates (TD Tabular Message)

Focusing is accomplished when the electron beam is converged to form a pinpoint beam on the viewing screen of the SD CRT. Defocusing causes the electron beam to be diverged in order for the cross-sectional area of the beam to cover the single character on the character matrix. The electron beam is normally focused in the SD CRT's of the SDIE. However, the beam is defocused for the display of any character. The one exception arises in the selection of the point that is used as the central point (point of origin) of a message and the area from which the vector is swept. This point is selected by a focused beam.

A defocus gate is sent to the SD CRT's 10 μsec before the intensification of a character is to start. (See fig. 4–93.) From the time the intensification begins, the defocus gate is maintained 25 μsec longer, while the character is being displayed. The defocus gate is then removed 2.5 μsec after the intensification ends, thus allowing 37.5 μsec for the defocus gate. The defocus gate is produced, which removes the focus gate, to permit the SD CRT's to maintain a defocused condition. The focus and defocus signals are also used in the circuits of the SD CRT's to control the amount of intensification voltage to be applied to the grids of SD CRT's during point and character displays.

The defocus gate is produced by the 1 side of FF 6 when that side of the flip-flop is raised by the output of gate 13 at OD 1. Gate 13 is conditioned by the coincidence in AND 13 of the count of 3 from the timer counter and the output of OR 8. OR 8 produces a signal whenever a character (A through E) of a TD message is to be displayed.

The focus gate is produced by the 0 side of FF 6 when that side of the flip-flop is raised by the output of gate 14, OD 4, or by the overall-clear pulse at the end of the display cycle. OR 15 channels these two alternative signals to the 0 side of FF 6. The overall-clear pulse produces the focus signal after the intensification of the last character in a message display cycle. The focus signal after the intensification of each of the other characters results from the signal passed through gate 14, at OD 4. Gate 14 is conditioned by the coincidence in AND 14 of the timer count of 3 and the ready-to-clear-character-register-and-focus signal from OR 11. As the title of the last signal indicates, the focus signal is identical with the clear-character-register signal.

3.2.14.9 Clear-Character-Register Signal (TD Tabular Message)

The clear-character-register signal is produced to remove the bits from the character register after each character of a TD tabular message has been displayed in a message display cycle. At the end of a message display cycle, the signal coincides with the overall-clear pulse.

The clear-character-register signal is passed through gate 14 at OD 4. Gate 14 is conditioned by the coincidence in AND 14 of the timer count of 3 with a ready-to-clear-character-register-and-focus signal from OR 11. The ready-to-clear-character-register-and-focus signal, as its name indicates, is produced to remove the character bits and to focus the electron beams of the SD CRT's after each character has been displayed in a message display cycle. The ready-to-clear-character-register-and-focus signal is produced in OR 11 whenever one of the following signals is present:

a. A-, C-, D-, or E-feature signals. This signal is the overall generation control of each of the features indicated in the name of the signal. The final action of the signal after the display of a character in a message display cycle is to remove the defocus signal from the SD CRT's and to clear the character register of the character selection bits whose generation the A-, C-, D-, or E-feature signal controlled.

b. B-feature signal. This signal is the overall generation control for the B characters. The final action of the signal after the display of a character in a message display cycle is to remove the defocus signal from the SD CRT's and to clear the character register of the character selection bits whose generation the B-feature signal controlled.

c. Vector-end-tabular-message signal. This signal, which is used to stop the sweep and intensification of the vector in a TD tabular message, is also channeled through OR 11. It clears the bits in the character register which were used to select the point that was swept to produce the vector. Once the bits selecting the point have been removed, the character register is ready to receive from storage the bits of the A_1 character.

3.2.14.10 Timer-is-3 Signal (TD Tabular Message)

The timer-is-3 signal is used to generate the add 1 signal to the symbol sequencer at OD 1 time. The signal is produced in AND 5 when the timer counter output is 3 ($T2^2$–0, $T2^1$–1, $T2^0$–1). The gating circuit to produce the coincidence of the timer count and the OD 1 pulse is located in the miscellaneous control circuit. This timer-is-3 signal is also applied to AND circuits in the timer to allow for proper sequencing of a TD message display cycle.

3.2.14.11 Conditional-Unblank, Conditional-Blank, and Conditional-Sample Signals (TD Tabular Message)

The conditional-unblank, conditional-blank, and conditional-sample signals are passed from the SDGE to the MI element during the display of TD tabular messages that are programmed for the use of the light gun unit. In the MI element, the unblank and blank signals condition circuits for the pickup of information from the viewing screen of the SD CRT by a light gun unit. The conditional-sample signal, which follows the conditional blank, transfers the information to the MI element. The conditional unblank occurs at the timer count of 6, OD 3; the conditional blank occurs at the timer count of 7, OD 3; the conditional sample occurs at the timer count of 7, OD 3. The required coincidence in AND 3 of a use-light gun signal and a point-feature signal permits the use of the light gun unit only with TD tabular track messages having a light gun bit programmed in the message. (The point-feature signal is not generated during a TD tabular information message.)

The conditional-unblank signal is passed through gate 18, at OD 3. Gate 18 is conditioned by AND 16 when the timer count is 6, the display signal is present, and an output from OR 12 is generated. OR 12 will have an output when either AND 3 or AND 4 produces an output. In this case, AND 3 will produce an output.

The conditional-blank signal is passed through gate 19, at OD 2. Gate 19 is conditioned by AND 15 when the timer count is 7, the display signal is present, and an output from OR 12 is generated. OR 12 will have an output when either AND 3 or AND 4 produces an output. In this case, AND 3 will produce an output.

The conditional-sample signal is passed through gate 17 at OD 3. Gate 17 is conditioned by the coincidence in AND 15 of the timer count is 7, the display signal, and the output from OR 12. The same signals, except the timer count, are present for AND 15 and AND 16.

In later manufactured systems the conditional sample circuits will be replaced by conditional reset circuits.

3.2.14.12 End-Cycle Signal (TD Tabular Message)

The end-cycle signal halts the display cycle of a TD tabular message by turning off the on-off flip-flop in the on-off control and OD distributor section. This circuit then develops the overall-clear pulse for removing all the bits in the register and storage flip-flops of the SDGE. The end-cycle signal is also sent to the DTE where, during test, it controls the operations of the tester.

The end-cycle signal occurs when an end-track-data-message signal, from the C feature circuit at the symbol sequencer count of 27, passes through gate 4 at the timer count of 7, OD 3. The timer count of 7, OD 3, is the end of the individual display of a character; in this case, the C4 character is the last of the message display cycle.

3.2.14.13 TD Vector Message

The timing of the display of a TD vector message is shown in figure 4–93. The counter and command signals required for the message are discussed in 3.2.14.14 through 3.2.14.23.

3.2.14.14 Timer Counter (TD Vector Message)

Timer counter operation is the same for a vector message as for a tabular message. (See 3.2.14.2 of this section.)

3.2.14.15 Vector-Off Signal (TD Vector Message)

Vector-off signal operation is similar to that described in 3.2.14.3 of this section for TD tabular messages, with the following exceptions. The ready-to-start-vector signal is produced in OR 6 by one of the following signals:

a. Start-V_1 and V_2 (start the first or second vector of a TD vector message), which originates in the vector control circuit.

b. Start-V_3 and V_4 (start the third and fourth vector message), which originates in the vector control circuit.

3.2.14.16 SD Intensify Gate (TD Vector Message)

The SD intensify gate for G_1–G_4 characters is produced in a way that is similar to a tabular message operation. (Refer to 3.2.14.4 of this section.) AND 9 produces an output whenever a G_1 or G_4 character-generation-control (A, C, D, or E) signal passes through OR 8. The G_2 or G_3 character-generation-control (B-feature) signal must coincide with a track-message signal in AND 2 to produce intensification of the G_2 and G_3 characters. This signal from AND 2 passes through OR 8 and is applied to AND 9. At the timer count of 5, AND 9 will condition gate 9, allowing the next OD 1 to set FF 5 through OR

14. (The coincidence occurs in AND 2 during a TD vector message because LS of word 0 is not used. With the track-message signal not connected to AND 11, the AND circuit is effectively a 1-legged OR circuit.)

The intensify signal, which is produced for all the vectors in a TD vector message, is channeled from AND 11. This circuit produces an output signal when a timer-is-3 signal (from AND 5) coincides with a display signal and a start-V_1 and V_2 signal, or a start-V_3 and V_4 signal is also applied to AND 7 through OR 6. At the timer count of 7, OD 3, gate 7 will pass a start-vector signal to clear FF 4 and start the sweeping of the vector. The intensify signal, which sets FF 5, occurs 2.5 μsec (timer-is-3, OD 4) after the sweep of the vector. (See fig. 4–93.) Therefore, no distinguishing intensification of the point of origin of any vector in a vector message will occur.

The intensify signal is turned off by the ready-to-blank-and-stop-vector signal after each of the characters or vectors of a TD vector message have been displayed. The ready-to-blank-and-stop-vector signal occurs after 25 μsec of intensification for all characters and after 47.5 μsec for vectors.

The ready-to-blank-and-stop-vector signal is delivered to AND 8 through OR 7 as a result of any of the following signals:

a. End-vector-1-and-vector-2 originates in the vector control. This signal operates to end the sweep and blank the intensification of the first or second vectors in a TD vector message.

b. End-vector-3 originates in the vector control. This signal operates to end the sweep and blank the intensification of the third vector in a vector message.

c. End-vector-4 originates in the vector control. This signal operates to end the sweep and blank the intensification of the fourth vector in a vector message.

d. $G_1 - G_4$ character-generation control (A, B, C, D, or E feature).

3.2.14.17 Clear XY-Register-and-Vector-Register Signal (TD Vector Message)

The clear-XY-register-and-vector-register signal is developed in the timer at different times during the display cycle of a TD vector message. This is done to remove the bits representing the points of origins of vectors (X, Y voltages) from the XY register and sense and magnitude bits of vectors ($\dot{X}$, $\dot{Y}$ voltages) from the vector register. Specifically, the signal clears the XY register and vector register after each of the first three vectors of a TD vector message have been displayed.

Clearing of the vector register after the fourth vector of a TD vector message is brought about by the first advance-character-position signal in the display cycle. The characters may thus be positioned in the required format without vector voltage interference (the display tube deflection plates that position characters also generate the vectors). Clearing of the XY register after the fourth vector of a TD vector message does not occur until the end of the messages with the arrival of the overall-clear pulse. In this manner, the point of origin of the fourth vector is maintained by the deflection coil of the display tubes while the character format is developed by the character-positioning plates.

The clear-XY-register-and-vector-register signal is pulsed at OD 4 through gate 12. Gate 12 is conditioned by the coincidence in AND 12 of a timer-is-3 signal (developed in AND 5) with an end-V_1 and V_2 signal or end-V_3 signal (through OR 10) from the vector control.

The clear-XY-register-and-vector-register signal is connected from the timer to the XY register and to the vector register through OR circuits in the on-off control and OD distributor. These OR circuits make it possible for both the overall-clear pulse at the end of the message display cycle and the clear-XY-register-and-vector register signal during a display cycle to enter the XY register and the vector register through the same connecting lines.

3.2.14.18 Advance-Character-Position Signal (TD Vector Message)

The advance-character-position signal is developed for TD vector messages in order to step the X and Y position counters in the character counter and positioning circuit. The stepping of the counter allows the G_1–G_4 characters to be positioned correctly. This is similar to TD tabular message operations described in 3.2.14.6 of this section.

Gate 15 is sensed by the output of gate 16 at OD 1 time of timer count 3. Gate 15 is conditioned through OR 13 by one of two signals:

a. End–V_4. This signal permits an advance-character-position signal to be sent to the character counter and positioning circuit to enable the necessary voltages to be applied to the character positioning plates. These voltages on the character positioning plates of the SD CRT's allow the first character (G_1) of a TD vector message to be displayed in its previously determined position.

b. $SS2^4$–1 and $SS2^3$–1 coincident in AND 6. This condition exists when the symbol sequencer count is 24 through 27 (digital 11000 through 11111). The G characters are displayed during this period.

3.2.14.19 Transfer (from-Storage-into-Register) Signal (TD Vector Message)

The transfer (from-storage-into-register) signal transfers the $\dot{X}$ and $\dot{Y}$ bits of the last three vectors into the vector register and also transfers the G character bits into the character register in a TD vector message. The transfer signal is used the same way in TD vector messages as it is used for TD tabular messages. (See 3.2.14.7 of this section.) However, the X, Y and $\dot{X}$, $\dot{Y}$ bits for the first vector of a TD vector message are fed directly into the X, Y and vector registers, respectively (without previous storage), while being read from the drum.

3.2.14.20 SD Focus and Defocus Gates (TD Vector Message)

The SD focus and defocus signals are produced for all of the characters and vectors of a TD vector message in a manner identical with their generation for the characters and vectors of a TD tabular message.

In a TD vector message, the ready-to-clear-character-register-and-focus signal is produced in OR 11 when any one of the following signals occurs:

a. End-vector-4. This signal (channeled through OR 11) removes the bits in the character register which were used to select the point that was swept to produce the four vectors. The character register is now ready to receive from storage the bits of the G_1 character which is the first character to be displayed in a TD vector message. This signal is also channeled through OR 7 to stop the sweep and intensification of the fourth vector of a vector message.

b. The G_1–G_4 character generation control signals (A-, B-, and C-feature) are also channeled through OR 11 to produce the same effects as those mentioned in a, above.

3.2.14.21 Clear-Character-Register Signal (TD Vector Message)

The purpose of the clear-character-register signal in a TD vector message is to clear the character register after the fourth vector and after each character is displayed.

This signal is generated by an OD 4 pulse which passes through gate 14. Gate 14 is conditioned by the coincidence in AND 14 of the timer-is-3 signal and the ready-to-clear-character-register-and-focus-signal. (See 3.2.14.20 of this section.)

3.2.14.22 Conditional-Unblank, Conditional-Blank, and Conditional-Sample Signals (TD Vector Message)

No information is transferred to the MI element during a TD vector message. Thus the conditional-unblank, conditional-blank, and conditional-sample signals are not required and, therefore, are not generated.

3.2.14.23 Timer-is-3 and End-Cycle Signals (TD Vector Message)

During a TD vector message, the timer-is-3 and end-cycle signals are generated as described for TD tabular message operation. (See 3.2.14.10 and 3.2.14.12 of this section.)

3.2.14.24 RD Message

The timing of an RD message display cycle is shown in figure 4–94. The timer counter and command signal for the message are discussed in 3.2.14.25 through 3.2.14.30. The vector-off, clear-XY-register-and-vector-register, and advance-character-position signals are not required for RD messages.

3.2.14.25 Timer Counter (RD Message)

The timer counter operation is similar to that for a TD tabular message (par. 3.2.14.2) with the exception that FF's 1, 2, and 3 count from 2 through 7 (instead of 3 through 7) and, after 7, the timer counter returns to 3, at which time the RD display cycle ends.

The message display cycle for an RD message requires that the timer counter begin at 2 instead of 0 as in a TD tabular message (fig. 4–93). For the first RD message display cycle after TD displays, a clear signal (through GT 19 conditioned by the RD control level) sets FF T 2^1 to 1 to produce a 2 in the timer counter. However, for the succeeding RD message display cycles, the timer counter is set to 2 by the clear pulse, which occurs at the end of each RD message display cycle when the timer counter is 3 ($T2^2$–0, $T2^1$–1, $T2^0$–1). This clear pulse will clear the $T2^0$ flip-flop to 0 in order for the timer counter to be at 2 for the ensuing cycle.

3.2.14.26 SD Intensity Gate (RD Message)

The intensification signal generation for an RD message is basically similar to that for TD messages. AND 9 (fig. 4–92) channels the intensify signals for all RD messages to FF 5 to raise the intensify gate. AND 9 is conditioned by the RD control bit, the display bit, and timer counter at 5. The RD control bit is routed through OR 8.

The intensify gate is dropped when the ready-to-blank-and-stop-vector signal (generated in OR 7 by the RD control bit) is applied to AND 8. AND 8 is conditioned by this signal and the timer counter at 7.

3.2.14.27 Transfer (from-Storage-into-Register) Signal (RD Message)

The transfer (from-storage-into-register) signal is applied to the RD control circuit. It is used to generate the digital signal voltages which select the character to be displayed in an RD message display cycle.

The transfer signal is produced as the output of

gate 16 (OD 1) which is conditioned by the timer-is-3 signal. The signal passes through gates in the RD control circuit which are conditioned by the category signals of the message. The pulses that are emitted from the gates are transferred to the character register where they set flip-flops for the selection of a specific character.

3.2.14.28 SD Focus and Defocus Gates and Clear-Character-Register Signals

The focus and defocus signal is produced for all the characters of a radar message in a manner identical with the generation for the characters of a tabular message. (See 3.2.14.8 of this section.)

The clear-character-register signal is produced to remove the bits from the character register after the symbol has been displayed. This occurs 2.5 μsec before the new character selection bits are transferred from the RD control circuit into the character register.

The ready-to-clear-character-register-and-focus signal is produced in OR 11 whenever an RD signal is present. The RD signal is the overall generation control for RD messages. Its action through OR 11 permits a clear-character-register-and-focus signal to arise 2.5 μsec before the bits for the RD message category are transferred to the character register. The overall-clear pulse at the end of an RD message display cycle also permits the character register and display tube circuits to be cleared and focused.

3.2.14.29 Conditional-Unblank, Conditional-Blank, and Conditional-Sample Signals (RD Message)

The conditional-unblank, conditional-blank, and conditional-sample signals are sent from the SDGE to the MI element during the display of the most recent (bright) RD message. The purpose of these signals is the same for TD tabular message operation (3.2.14.11) with the exception that the X and Y co-ordinates are transferred from the SDGE to the MI element.

AND circuit 4 is conditioned when the RD bright and RD control bit are coincident. This coincidence allows AND 15 and 16 (through OR 12) at the timer count of 6 and 7, respectively, to be conditioned. The coincidence of an RD signal and an RD-bright-signal makes it possible for the light gun to be used; i.e., with RD messages from the RD drum field most recently written on by the Central Computer System.

3.2.14.30 Timer-Is-3 End-Cycle Signals (RD Message)

The end-cycle signal stops the RD display cycle. This occurs when an RD signal (through OR 2) conditions gate 4 to pass an OD 3 pulse from gate 3 at the timer count of 7. This same pulse (OD 3, at timer count of 7) steps the timer counter to 3.

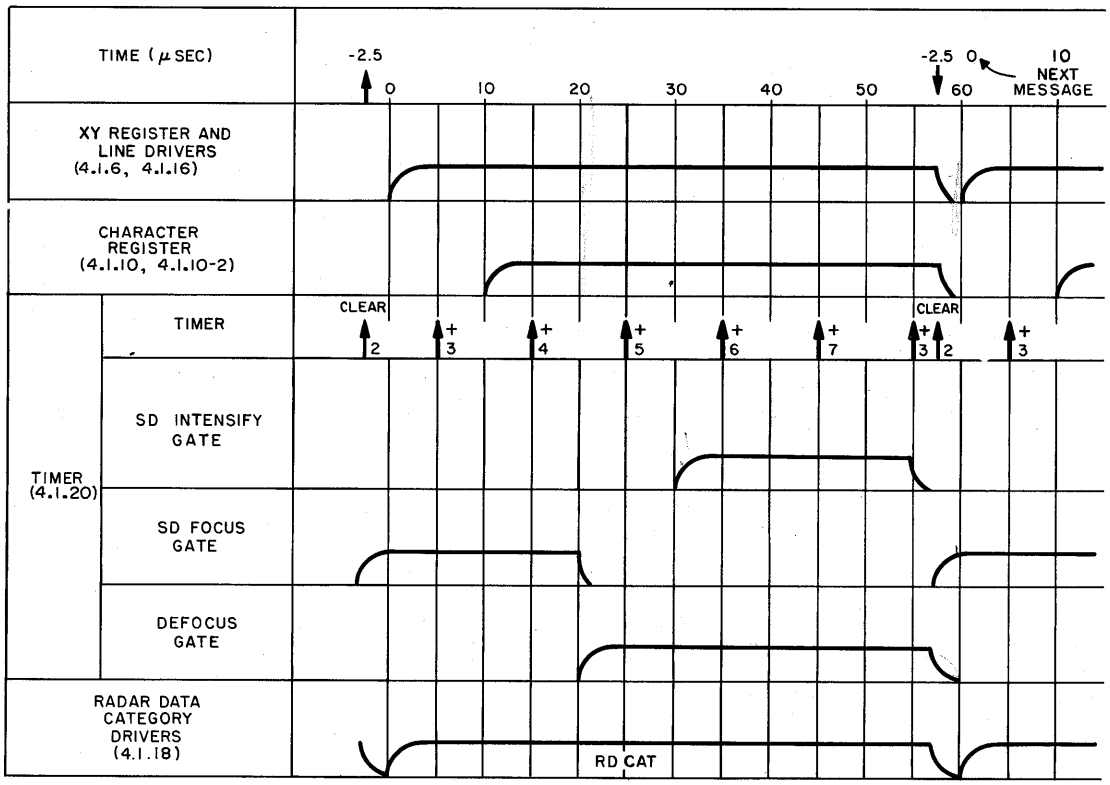


Figure 4–94. RD Messages Display Cycles, Timing Chart

3.3 OVERALL TIMING OF SD CYCLE

An SD cycle for the AN/FSQ-7 consists of the following:

a. Reading, processing, and displaying all RD messages (1 second, approximately).

b. Switching (by the Drum System) to the track data drum (0.01 second average).

c. Reading, processing, and displaying all TD messages (1.6 seconds, approximately).

d. Switching to the radar data drum (0.01 second average).

Figure 4–91 is a timing chart of the SD cycle. The SD cycle of approximately 2.62 seconds is repeated without interruption.

3.3.1 RD Messages

Each RD message, consisting of a single character, requires 60 μsec. The 2,048 RD messages contained on each field require approximately 0.12 second (2,048 times 60 μsec). Since only eight of the nine fields of the RD drum are read, the reading of the RD drum takes about 1 second.

3.3.2 TD Messages

Each TD message, whether vector or tabular, is read, processed, and displayed in 1,040 μsec. Each of the six fields of the TD drum contains 2,048 registers (words) or 256 slots (8-word message). Therefore, a field is displayed in approximately 0.27 second (256 times 1,040 μsec). The six fields of the drum are then read in 1.6 seconds.

3.3.2.1 TD Vector Message

The sequence in which the parts of a TD vector message are displayed is shown in figure 4–91. Exact time relationships within the 1,040-μsec period required for the display of the whole message are referred to in figure 4–93.

3.3.2.2 TD Tabular Message

The sequence in which the parts of a TD tabular message are displayed is shown in figure 4–91. Exact time relationships within the 1,040-μsec period required for the display of the whole message are referred to in figure 4–93. Although a TD tabular information message contains no point or vector, its overall timing is the same as that of a TD tabular track message.

3.4 DETAILED TIMING OF SD CYCLE

A detailed timing diagram of the operations of circuits in the SDGE during the display cycle of one TD message is shown in figure 4–93. A detailed timing diagram for an RD message is shown in figure 4–94 and is discussed in 3.5.3, below.

3.5 TD MESSAGES

The eight different horizontal rows in figure 4–93 illustrate the outputs related to the counter circuits in the SD timing and control section during one TD message display cycle. The outputs represent the presence of bits in registers and the occurrence of output signals to the SD CRT intensification units. With the presence of signals in the circuits of the SDGE, the SD CRT's may be intensified for the display of a TD message. The vertical lines across the horizontal rows indicate the time corresponding to the arrival of OD 1 timing control pulses from the Drum System. The interval between two vertical lines, or two OD 1 pulses, is 10 μsec, during which time OD 2, OD 3, and OD 4 pulses arrive 2.5 μsec apart.

A TD tabular or TD vector message display cycle is 1,040 μsec in duration. The cycle begins with a WOW signal, at OD 4 time, 2.5 μsec before the first word (word 0) of the message is read from the drum, at OD 1 time. At 1,027.5 μsec after the first word is read, a clear pulse ends the generation of the message. An elapsed time of 12.5 μsec occurs before the WOW signal for word 0 of the next message arrives to repeat the timing cycle.

3.5.1 TD Tabular Message

The following is an explanation of the circuit conditions indicated above the line in each row of figure 4–93. This pertains to TD tabular messages.

Row 1 on the diagram indicates the different read-word signals from the gate generator. The signals distribute the different words of a TD tabular message into the proper storage and register flip-flops while the words are passed through the input gates section. The input gates section passes information only when conditioned by a read (drum) signal from the miscellaneous control circuit. To accomplish the distribution, the read-word signals condition admittance (distribution) gates of the flip-flops that are to store the word being read at each of the first eight OD 1 times in the tabular message display cycle. The signals are developed by the first three stages ($S2^2$, $S2^1$, $S2^0$) of the 5-stage symbol sequencer (row 6 on the diagram) during the count of 0 through 7. Throughout the remainder of the display cycle, the signals are also developed but do not admit words into storage and register flip-flops. During this latter period, the drum is not being read; therefore, the input gates section remains deconditioned.

Row 2 on the diagram illustrates the presence in the XY register and drivers section of the X and Y bits of the TD tabular message. The $\dot{X}$ and $\dot{Y}$ bits position the E character and the point and provide the point of origin of the single vector in the display of the message. This location is the central position for the

display of the character format of the message. The bits enter the register as soon as word 1 is read from the drum at time 10 μsec and remain until the generation of the message is completed.

Row 3 on the diagram illustrates the presence of character selection bits in the character register during one SD message cycle. For a tabular message, which has 19 characters (point and A through E characters), the bits for the characters are allotted the different intervals shown in row 3 during the display cycle of the message. The E character bits are read into the register as word 0 is read from the drum at time 0; the bits of the A through D characters are transferred into the register from the word storage section at the times they are to appear in the display cycle. The character bits of the point feature are not written into a tabular message but are set into the register by a set-point signal from the E feature circuit. As a result, the normally focused beam is passed through the point character in the character-forming matrix and forms the point. The point is displayed in the same position as the E character and is swept to produce the vector.

Row 4 on the diagram illustrates the presence of the vector sense and magnitude ($\dot{X}$,$\dot{Y}$) bits in the vector register during a TD tabular message display cycle. For a tabular message, the bits enter the register as they are read (in word 5) from the drum. The interval, as shown in the diagram, for the sense and magnitude bits suppresses the vector-off signal in the timer to the vector generator. During this time, the sense and magnitude bits generate the voltages to sweep the point, thus producing a vector.

Row 5 on the diagram illustrates the times when advance-character-position signals enter the character counter and positioning circuit. The first signal sets the circuit and positions the A_1 character. Subsequent signals step the counter in order to advance from position to position in the character format. The positions determined by the counting circuit are all relative to the central X,Y position of the TD tabular message display (E character, point, and vector origin).

Row 6 on the diagram illustrates the symbol sequencer counts during a TD tabular message display cycle. The symbol sequencer is a counter of 27 that divides the entire display cycle into the 50-μsec intervals during which the individual displays of the vector and the character occur. At the beginning of a cycle, however, the words of the message are being read into the SDGE. During this period, the counter is stepped at 10-μsec intervals and produces the read-word signals for conditioning specific admittance (distribution) gates of the storage and register flip-flops in the generator.

Row 7 on the diagram illustrates the counts of the timer counter in the timer circuit. The timer counter is a counter of 7, stepped every 10 μsec (at OD 3). In a tabular message display cycle, the counter goes through an initial count of 0 to 7; successive counts are from 3 to 7 (50 μsec in duration, corresponding to one symbol sequencer cycle-dividing count). The counts of 3 to 7 are used to command output signals (row 8 on the diagram) from the timer to the console intensification units for each individual display in a tabular message display cycle.

Row 8 on the diagram illustrates the SD intensify gate (raised by the intensify signal) and the SD focus and defocus gates from the timer. For each character to be displayed (other than a point or vector), the defocus signal is sent to defocus the normally focused electron beam of each SD CRT at OD 1 time of timer count 4. This is 10 μsec before intensification is to begin at OD 1 time to timer count 5. The intensification persists for 25 μsec until the timer counter is stepped back to 3 (OD 3 time). The focus signal permits the electron beams to return to the normal focus state at OD 4 time of timer count 3. The generation of one individual display ends, and another begins, at OD 1 time of timer count 3.

The electron beam is not defocused prior to the display of the point or of the vector which is produced by sweeping the point. Instead, a sharper, more defined display is obtained by passing the focused beam through the vector aperture in the character-forming matrix. A single SD intensify gate is produced for both the point and vector. The point is displayed only if the point feature is selected at the SD display console.

3.5.1.1 Display of a TD Tabular Track Message

All sections of a TD tabular message are available for display during a TD tabular track message. In some instances, two characters (e.g., A_2 and B_1) occur after only one advance-character-position signal. These characters share the same format position in a final display; superposition is prevented by proper wiring of the category plugboards in the SD consoles. Regardless of what is displayed, the timing discussed in 3.5.1 is applicable.

3.5.1.2 Display of a TD Tabular Information Message

During a TD tabular information message, no point or vector is displayed. The A, C, D, and E features are forced. Superposition of the A and B feature characters is prevented by suppressing the intensification signals for the B characters. The timing discussed in 3.5.1 applies.

3.5.2 TD Vector Message

The circuit conditions below the line in each row of figure 4–93 pertain to TD vector messages. In the following discussion, references to the timing of a TD

tabular message (par. 3.5.1) will be made frequently to avoid unnecessary repetition.

The explanation of row 1 on the timing diagram is the same for TD tabular and TD vector messages. Row 2 illustrates the presence in the XY register and drivers section of the X and Y bits of a TD vector message. The X and Y bits generate the points of origin for the four vectors in the message. The bits for the first vector are read into the register immediately as they arrive in word 1 from the drum (at time 10-μsec). The X and Y bits for the second, third, and fourth vector are transferred to the register from the word storage section at the times in the display cycle allotted for their generation. However, the X and Y bits for the fourth vector remain in the XY register section after the vector has been generated because they determine the central position for the display of the character format (G_1–G_4 characters).

Row 3 on the diagram illustrates the presence of character selection bits in the character register during one message display cycle. In a TD vector message, the bits for selecting a pinpoint electron beam on the viewing screen of an SD CRT are set into the format to position the G_2, G_3, and G_4 characters. The positions determined by the counting circuit are all relative to the point of origin of the fourth vector in the TD vector message display.

The explanation for rows 6 and 7 of the timing diagram is the same as that given for a TD tabular message. The discussion for row 8 is also the same as that for a TD tabular message, with one exception. The intensification of the vector display persists for 47.5 μsec and begins 2.5 μsec after the sweep of the vector commences. Therefore, no intensification of the point at the start of the sweep (point of origin) can occur.

3.5.3 RD Message

A detailed timing diagram of an RD message display cycle is illustrated in figure 4–94. An RD message cycle lasts 60 μsec. The cycle begins with a WOW signal, at OD 4 time. At time 57.5 μsec, a clear pulse ends the display cycle. The WOW signal for the next RD message may be received at the same time, repeating the cycle.

The read-word signals for the single word of an RD message (not shown in the diagram) coincide with the RD signal which is present in the SDGE throughout all reading from the RD drum. The signals admit the word into the flip-flops of the XY register and line drivers section only when the input gates section is conditioned at the beginning of the display cycle by a read (drum) signal.

Row 1 on the diagram illustrates the presence in the XY register and line drivers section of the X and Y bits of radar data. For an RD message, the bits determine the position where the single character in an RD message is to appear on the viewing screen of the SD CRT's. The bits enter the register as soon as the 1-word RD message is read at time 0. The bits remain in the register until the generation of the message is completed.

Row 2 on the diagram illustrates the presence of character selection bits in the character register during one message cycle. For an RD message which has only one character (corresponding to the category of the message), the bits for the character enter the register at time 10-μsec and remain until the display cycle of the message is complete.

Row 3 on the timing diagram illustrates the stepping of the timer counter in the timer circuit. The timer counter is a counter of 7 and is stepped every 10 μsec (at OD 3). For an RD message, the timer counter provides the same type of output signal commands as for a TD tabular or TD vector message (SD intensify, focus, and defocus gates). However, the timer counter proceeds in a different manner for an RD message display cycle. The counter starts at 2, proceeds to 7, and steps back to 3. The counter is then cleared, in conjunction with the ending of the display cycle, and is again set to 2 for the beginning of the next RD message display cycle.

Rows 4, 5, and 6 illustrate that the electron beam is defocused 10 μsec before the 25-μsec intensification period begins. This enables the electron beam to be defocused when the single character formed by the character-forming matrix is displayed on the viewing screen of the SD console.

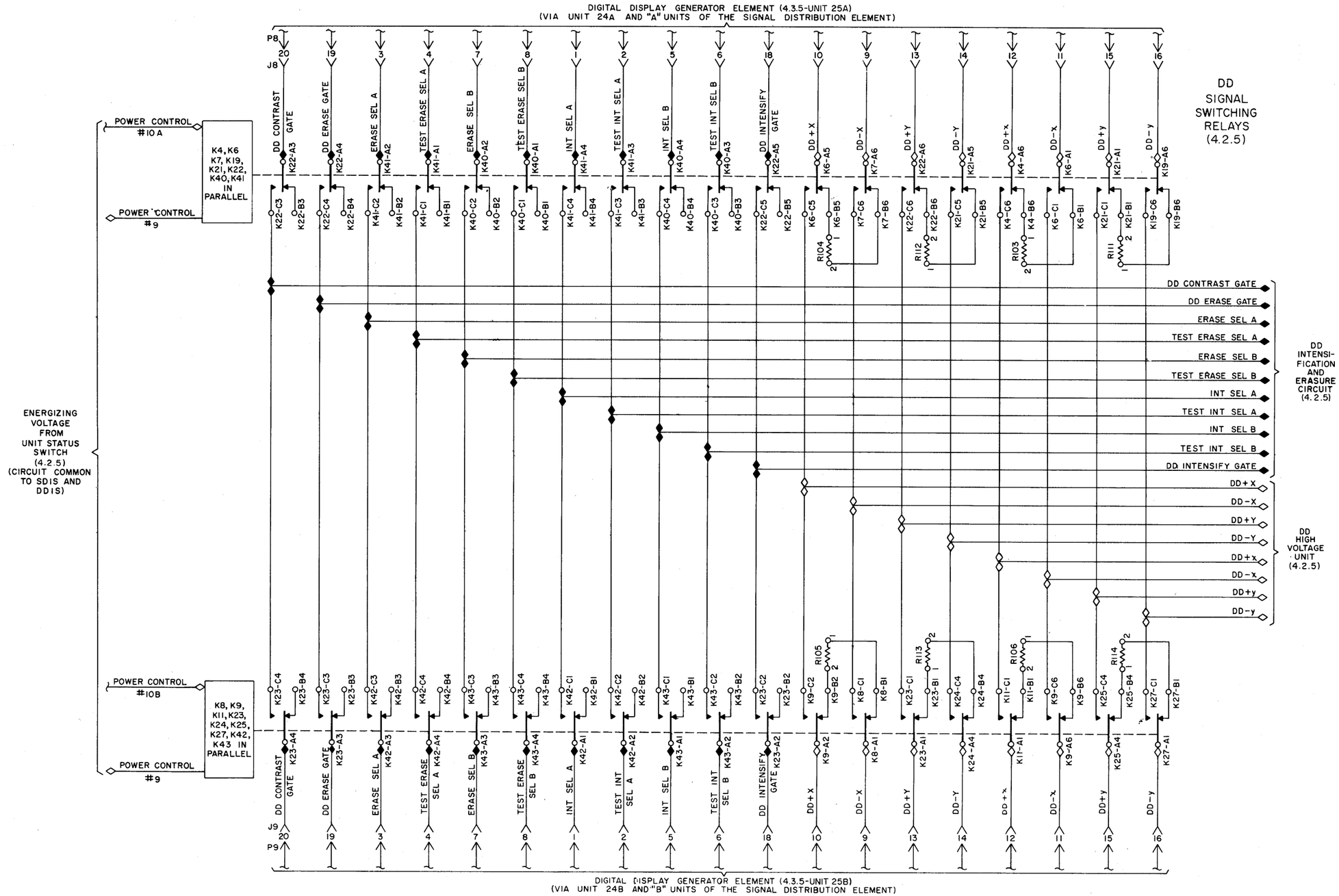
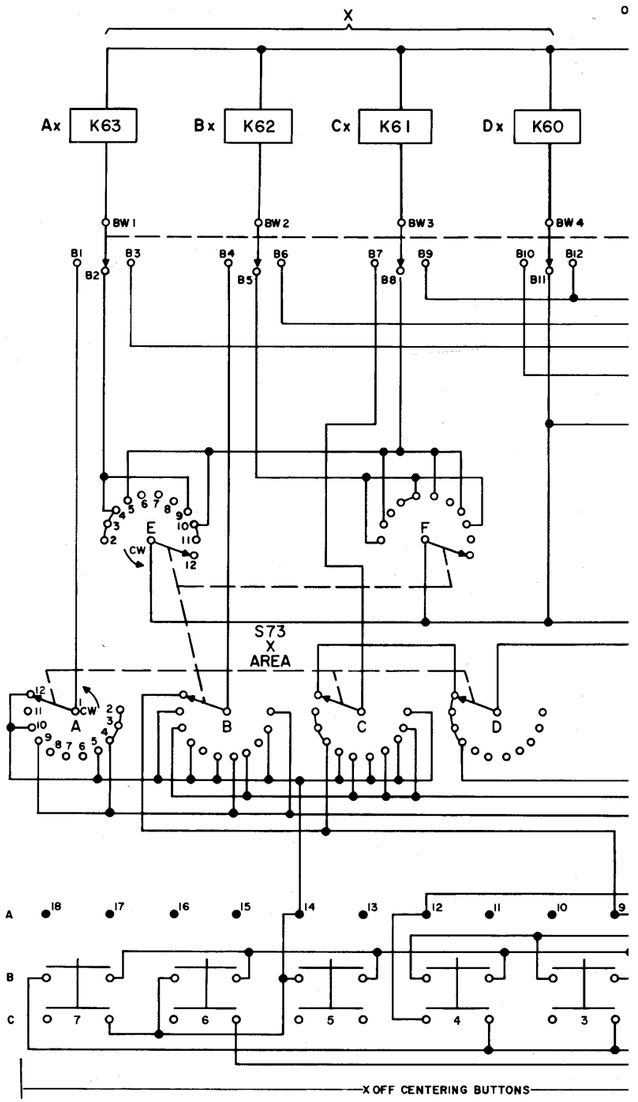
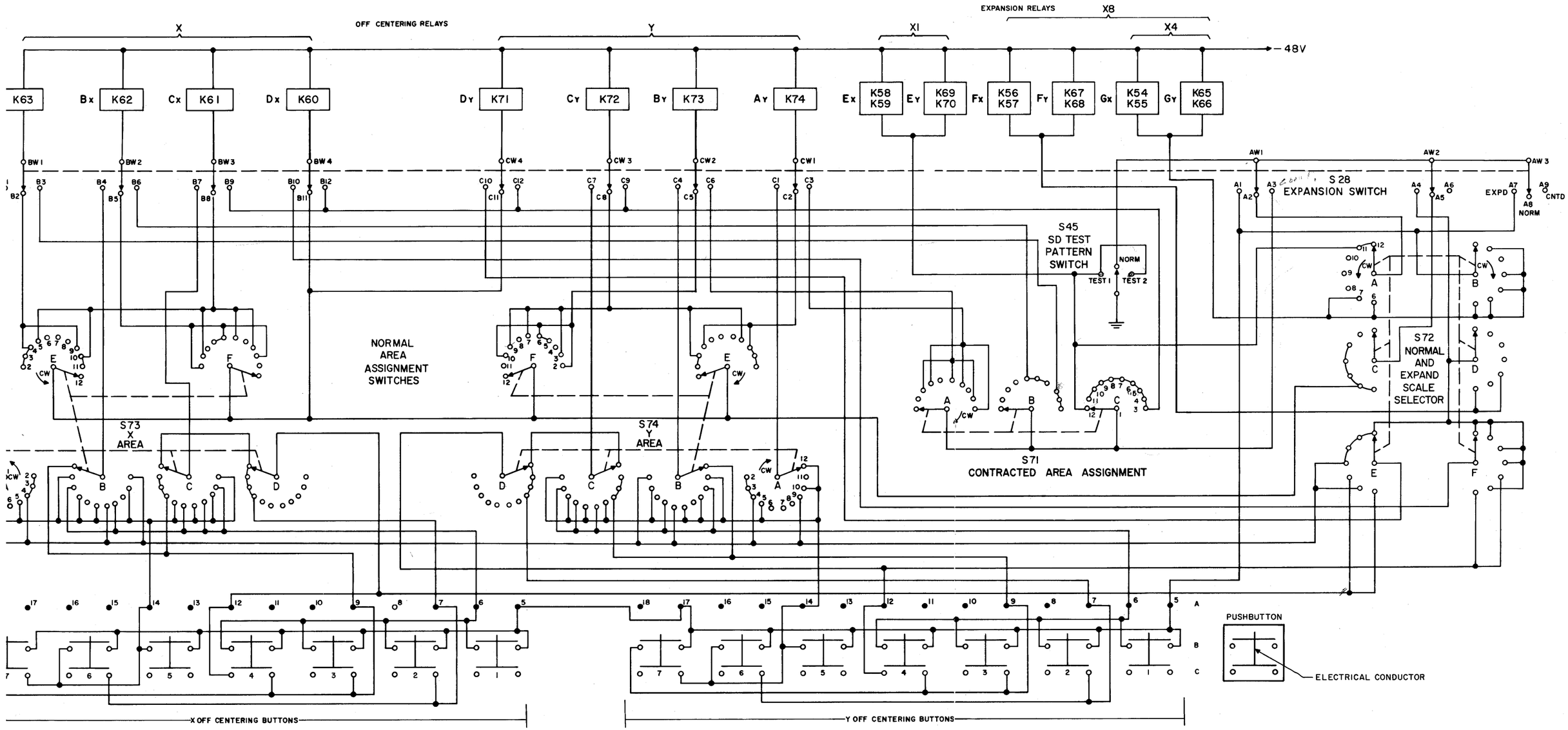


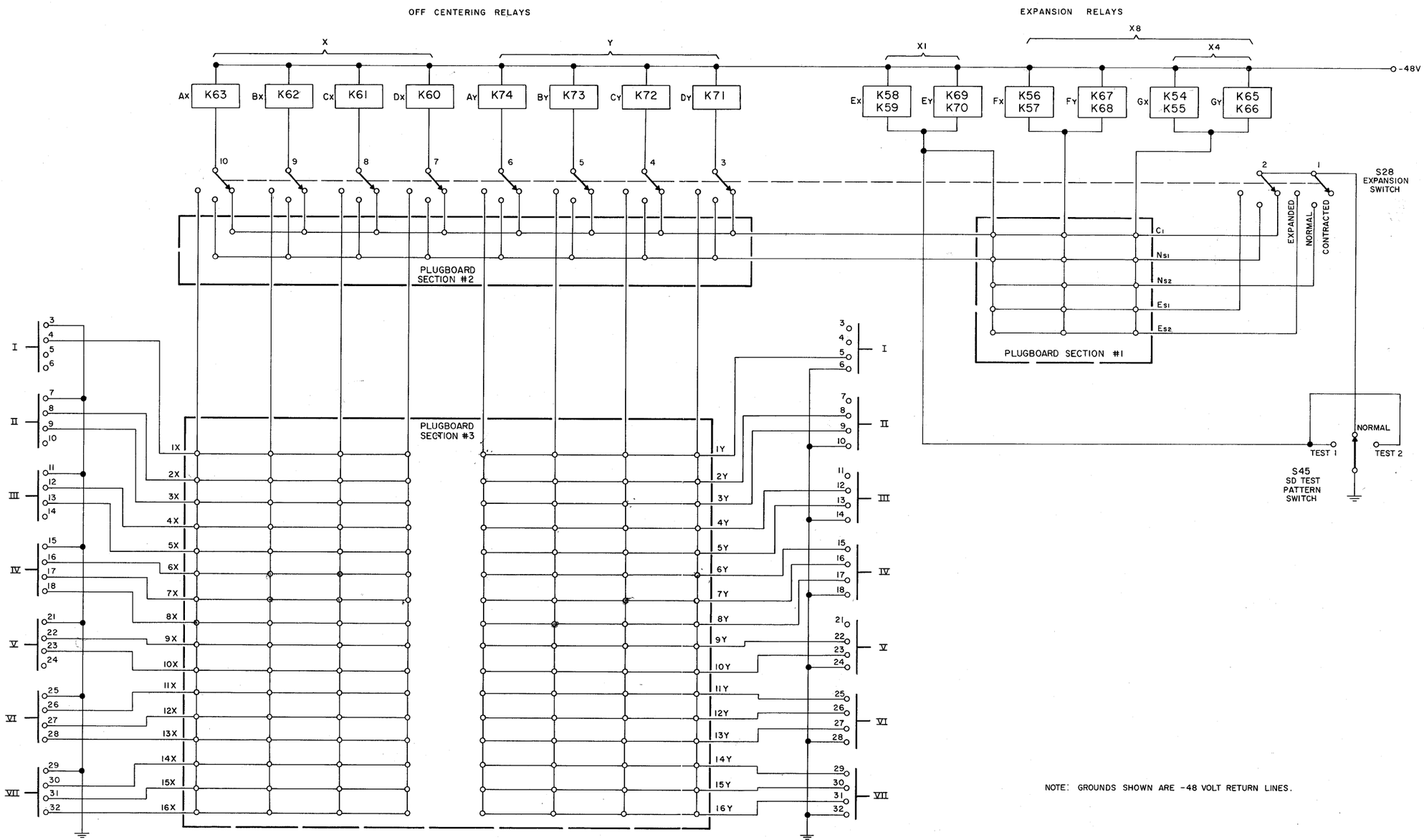
Figure 3-7. DD Indicator Section (in a Situation Display Console), Schematic Diagram (Sheet 1 of 2)


X
Ax
K63
Bx
K62
Cx
K61
Dx
K60
BW1
BW2
BW3
BW4
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
E
F
CW
S73
X
AREA
A
B
C
D
XOFF CENTERING BUTTONS



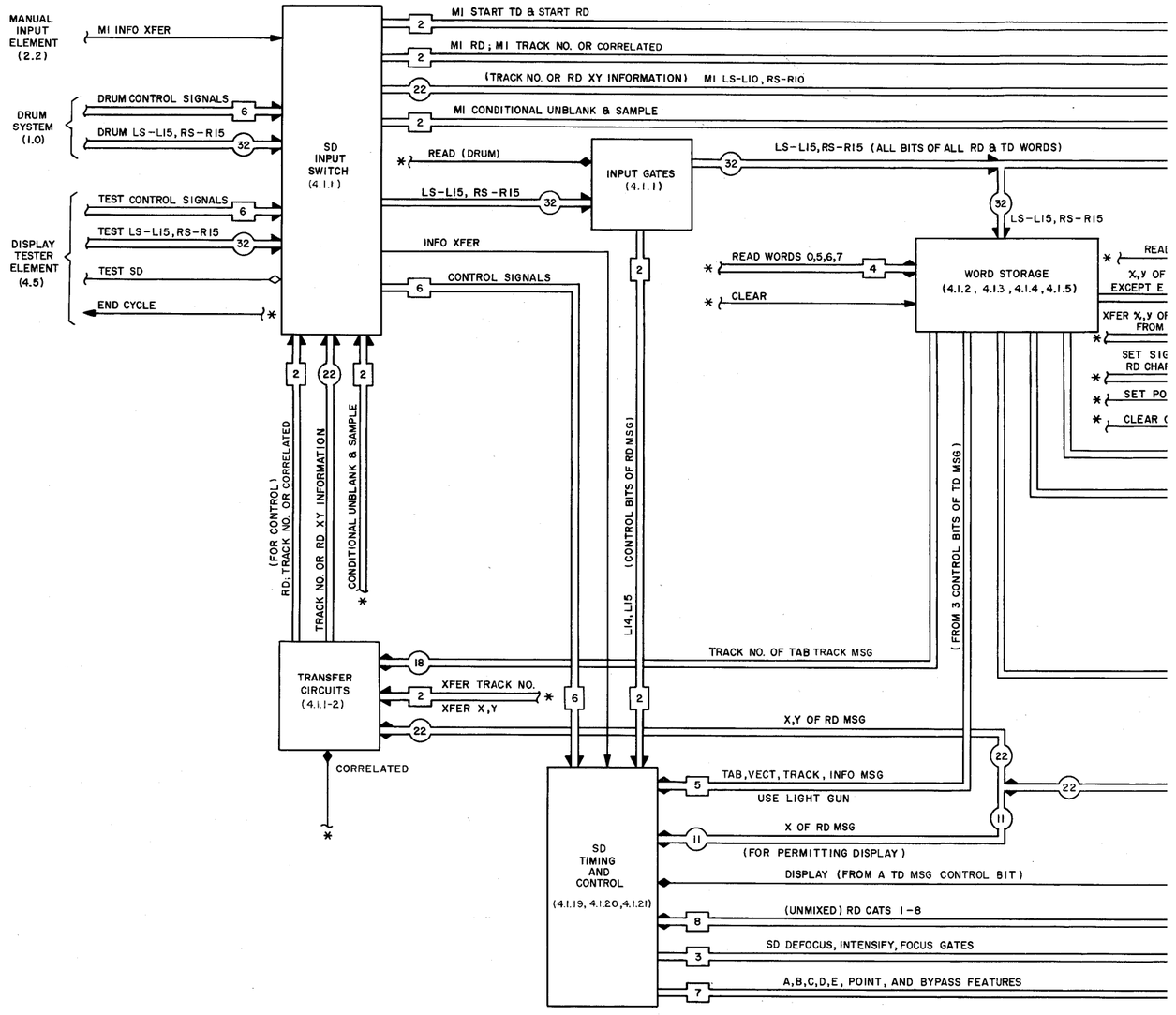
785 4-43

Figure 4-24. Expansion and Off-Centering Rotary Switches, Schematic



NOTE: GROUNDS SHOWN ARE -48 VOLT RETURN LINES.

Figure 4-27. Expansion and Off-Centering Plugboards, Schematic


MANUAL INPUT ELEMENT (2.2)
MI INFO XFER
DRUM SYSTEM (1.0)
DRUM CONTROL SIGNALS
DRUM LS-L15, RS-R15
DISPLAY TESTER ELEMENT (4.5)
TEST CONTROL SIGNALS
TEST LS-L15, RS-R15
TEST SD
END CYCLE
SD INPUT SWITCH (4.1.1)
MI START TD & START RD
MI RD ; MI TRACK NO. OR CORRELATED
(TRACK NO. OR RD XY INFORMATION) MI LS-L10, RS-R10
MI CONDITIONAL UNBLANK & SAMPLE
READ (DRUM)
LS-L15, RS-R15
INFO XFER
CONTROL SIGNALS
INPUT GATES (4.1.1)
LS-L15, RS-R15 (ALL BITS OF ALL RD & TD WORDS)
LS-L15, RS-R15
READ WORDS 0,5,6,7
CLEAR
WORD STORAGE (4.1.2, 4.1.3, 4.1.4, 4.1.5)
(FOR CONTROL) RD, TRACK NO. OR CORRELATED
TRACK NO. OR RD XY INFORMATION
CONDITIONAL UNBLANK & SAMPLE
L14, L15 (CONTROL BITS OF RD MSG)
(FROM 3 CONTROL BITS OF TD MSG)
TRACK NO. OF TAB TRACK MSG
TRANSFER CIRCUITS (4.1.1-2)
XFER TRACK NO.
XFER X,Y
CORRELATED
X,Y OF RD MSG
TAB, VECT, TRACK, INFO MSG
USE LIGHT GUN
X OF RD MSG
(FOR PERMITTING DISPLAY)
DISPLAY (FROM A TD MSG CONTROL BIT)
SD TIMING AND CONTROL (4.1.19, 4.1.20, 4.1.21)
(UNMIXED) RD CATS 1-8
SD DEFOCUS, INTENSIFY, FOCUS GATES
A,B,C,D,E, POINT, AND BYPASS FEATURES

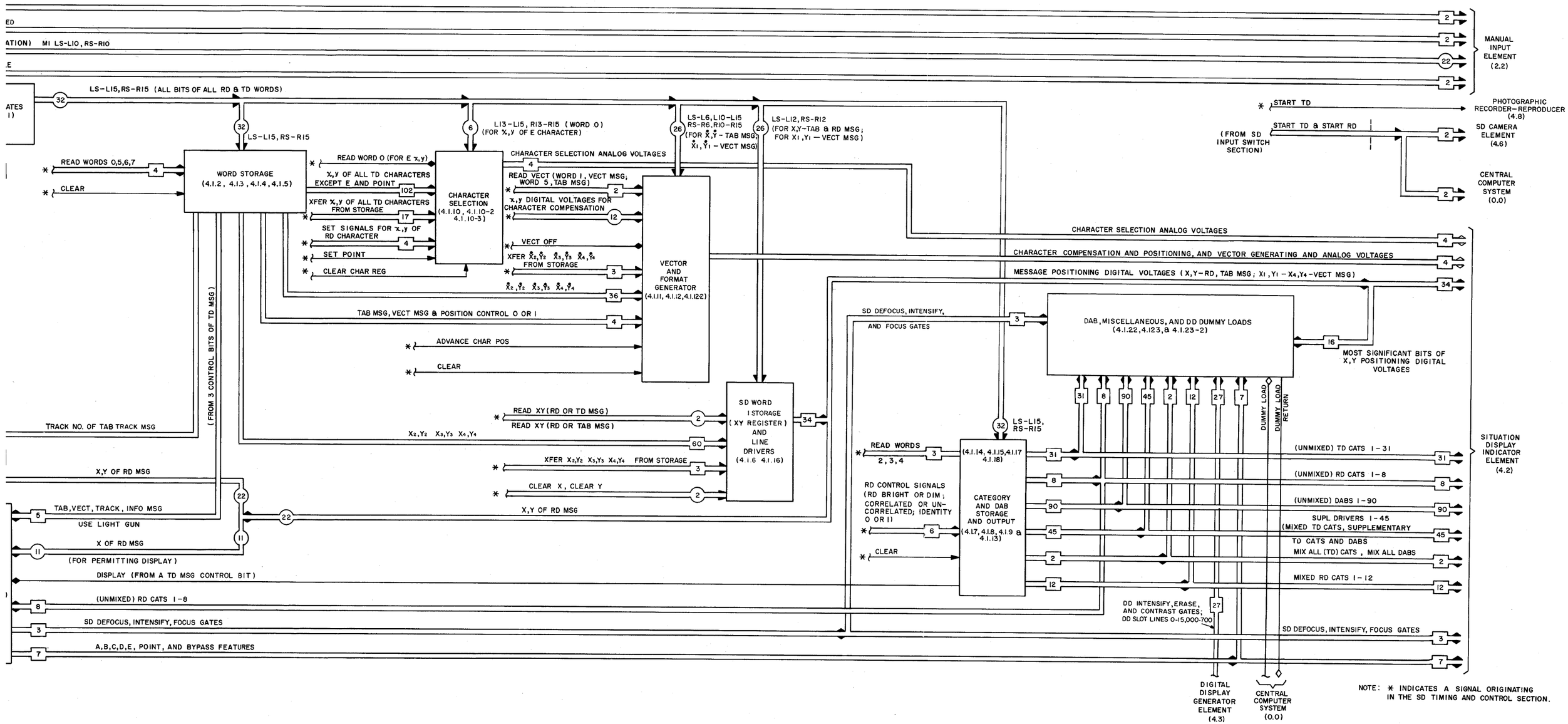


Figure 4-35. Situation Display Generator Element, Functional Block Diagram

SD CHARACTER SELECTION (4.1.10 AND 4.1.10-2)
SD INPUT SWITCH (4.1.1)
DISPLAY TESTER ELEMENT (4.5)
SD WORD I STORAGE (XY REGISTER) (4.1.6)
VECTOR GENERATION (4.1.12)
SD CHARACTER POSITIONING (4.1.11)
SD INDICATOR ELEMENT (4.2)
CLEAR CHAR REG
CONDITIONAL SAMPLE
CONDITIONAL UNBLANK
END CYCLE
CLEAR X
CLEAR Y
XFER X4,Y4,X̄4,Ȳ4
XFER X3,Y3,X̄3,Ȳ3
XFER X2,Y2,X̄2,Ȳ2
XFER X1,Y1,X̄1,Ȳ1
CLEAR VECT REG
ADVANCE CHAR POS
SD INTENSIFY GATE
SD FOCUS GATE
DEFOCUS GATE
BYPASS FEAT
A FEAT
B FEAT
C FEAT
D FEAT
E FEAT
POINT FEAT
BYPASS FEATURE (4.1.20)
OD 1
SS24-1*
SS23-1
T22-1
T21-1
T20-1
VECT MSG
VECTOR CONTROL (4.1.19)
SYMBOL SEQUENCER (4.1.19)
START VECT 1&2
START VECT 3&4
END VECT 1&2
END VECT 3
END VECT 4
VECT END TAB MSG
16
XFER
A+C+D+E FEAT
A1/G1
POINT FEAT
D FEAT
END TD MSG
B FEAT
CLEAR
SS24-1
SS23-1
TRACK MSG
RD
RD BRIGHT
CLEAR
TIMER (4.1.20)
ADVANCE CHAR POS
CLEAR
CLEAR X,Y,X̄,Ȳ
CLEAR CHAR REG
OD 4
OD 3
OD 2
OD 1
START TD
DISPLAY
TD
TIMER IS 3
OD 1
ADVANCE SYMB SEQ
START TD
RD BRIGHT
RD DIM
RD BRIGHT
RD DIM
XFER TRA
XFER X,Y
READ
DISPLAY
ON-OFF CONTROL AND OD DISTRIBUTOR (4.1.20)
MISCELLANEOUS CONTROL (4.1.21)
WOW
INFO MSG
USE LIGHT GUN
WOW
ALL OD
START RD
START TD
INFO XFER
RD BRIGHT
RD DIM
11
XLS-XL10-1
SD WORD O STORAGE (4.1.2)
SD WORD 6 STORAGE (4.1.4)
SD INPUT SWITCH (4.1.1)
XY DRIVERS (4.1.16)

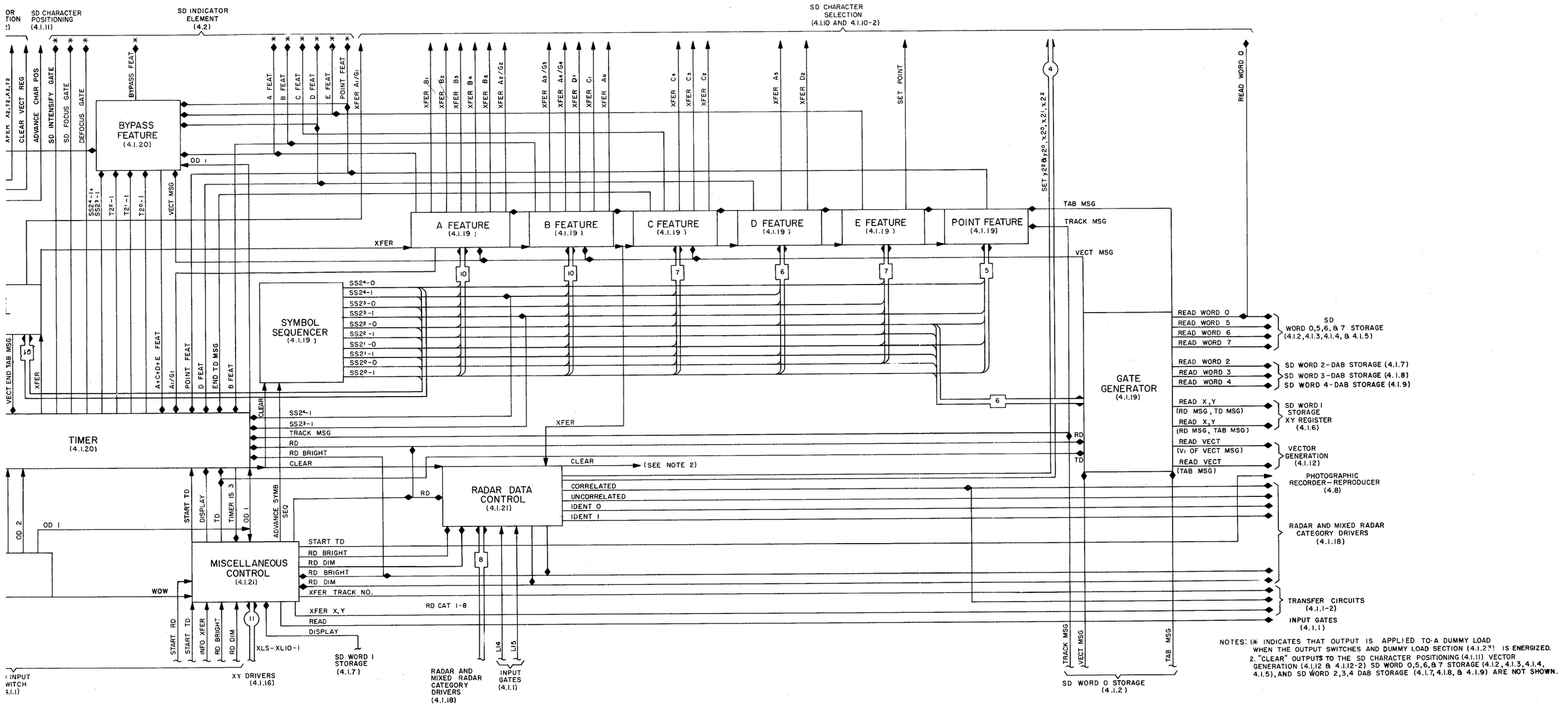
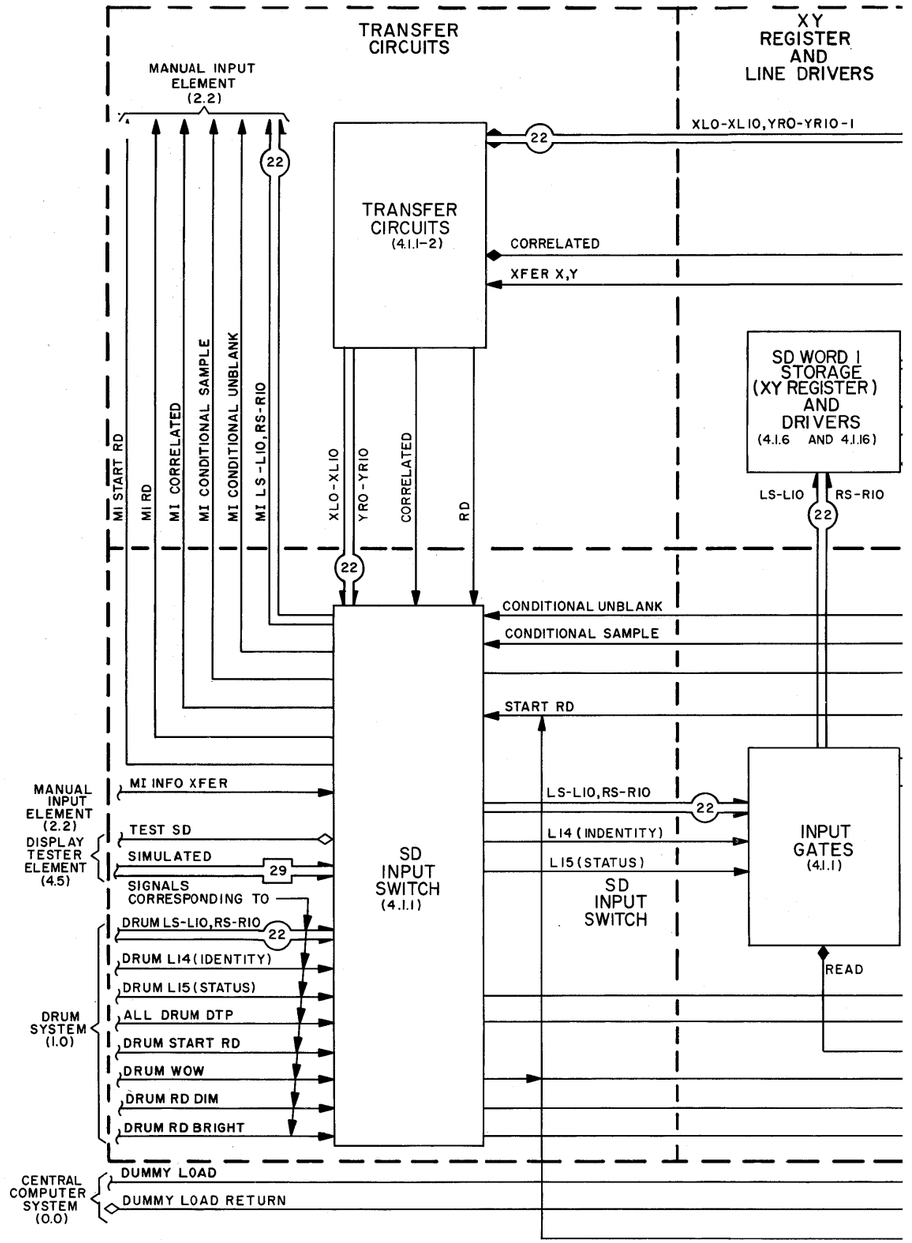


Figure 4–46. Situation Display Timing and Controls, Functional Block Diagram


TRANSFER CIRCUITS
XY REGISTER AND LINE DRIVERS
MANUAL INPUT ELEMENT (2.2)
22
XLO-XL10, YRO-YR10-1
TRANSFER CIRCUITS (4.1.1-2)
CORRELATED
XFER X,Y
SD WORD 1 STORAGE (XY REGISTER) AND DRIVERS (4.1.16 AND 4.1.16)
LS-L10
RS-R10
MI START RD
MI RD
MI CORRELATED
MI CONDITIONAL SAMPLE
MI CONDITIONAL UNBLANK
MI LS-L10, RS-R10
XLO-XL10
YRO-YR10
CORRELATED
RD
CONDITIONAL UNBLANK
CONDITIONAL SAMPLE
START RD
MANUAL INPUT ELEMENT (2.2)
MI INFO XFER
DISPLAY TESTER ELEMENT (4.5)
TEST SD
SIMULATED
29
SIGNALS CORRESPONDING TO
DRUM LS-L10, RS-R10
DRUM L14 (IDENTITY)
DRUM L15 (STATUS)
ALL DRUM DTP
DRUM START RD
DRUM WOW
DRUM RD DIM
DRUM RD BRIGHT
DRUM SYSTEM (1.0)
SD INPUT SWITCH (4.1.1)
LS-L10, RS-R10
L14 (INDENTITY)
L15 (STATUS)
SD INPUT SWITCH
INPUT GATES (4.1.1)
READ
DUMMY LOAD
DUMMY LOAD RETURN
CENTRAL COMPUTER SYSTEM (0.0)

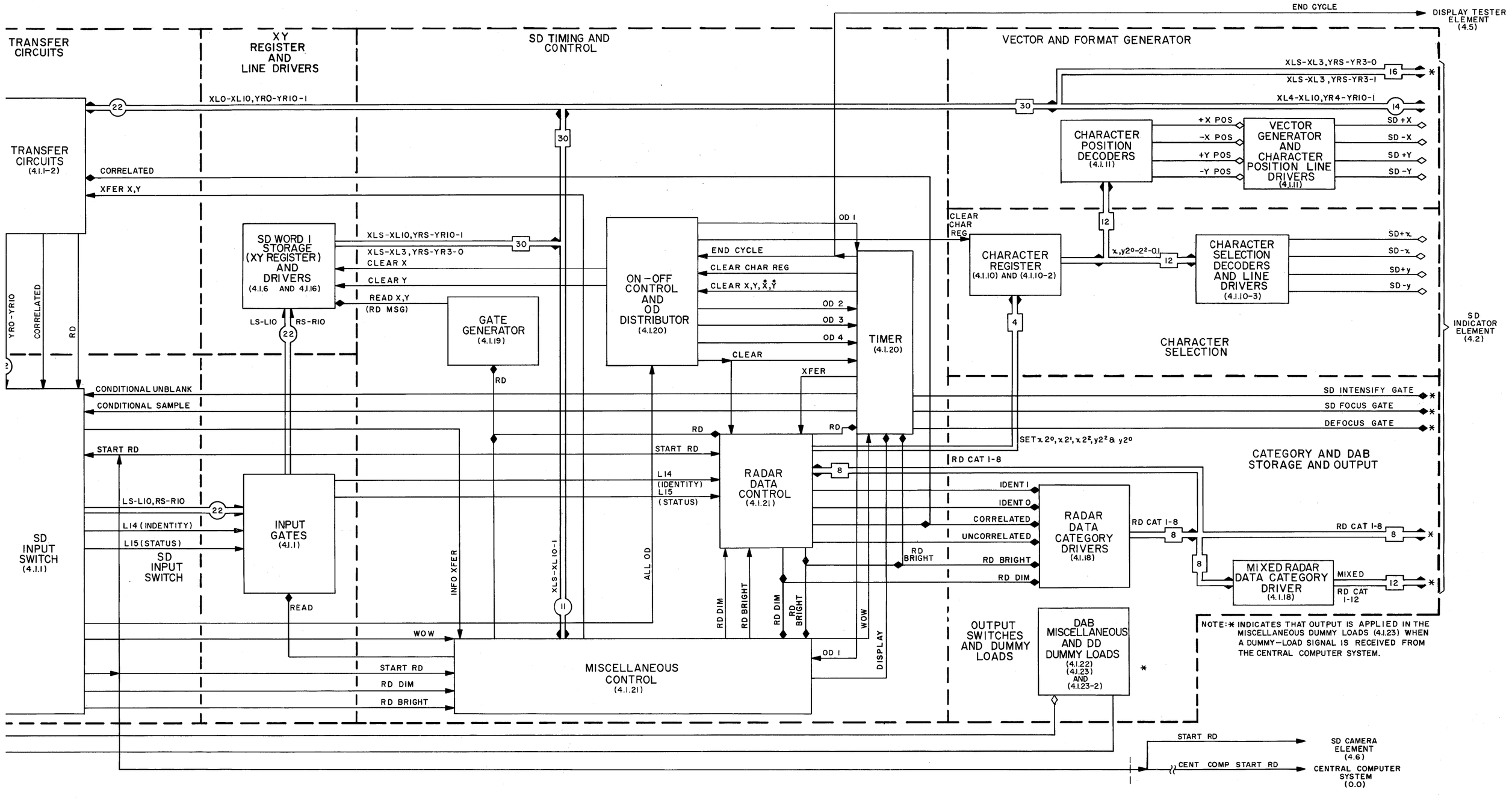
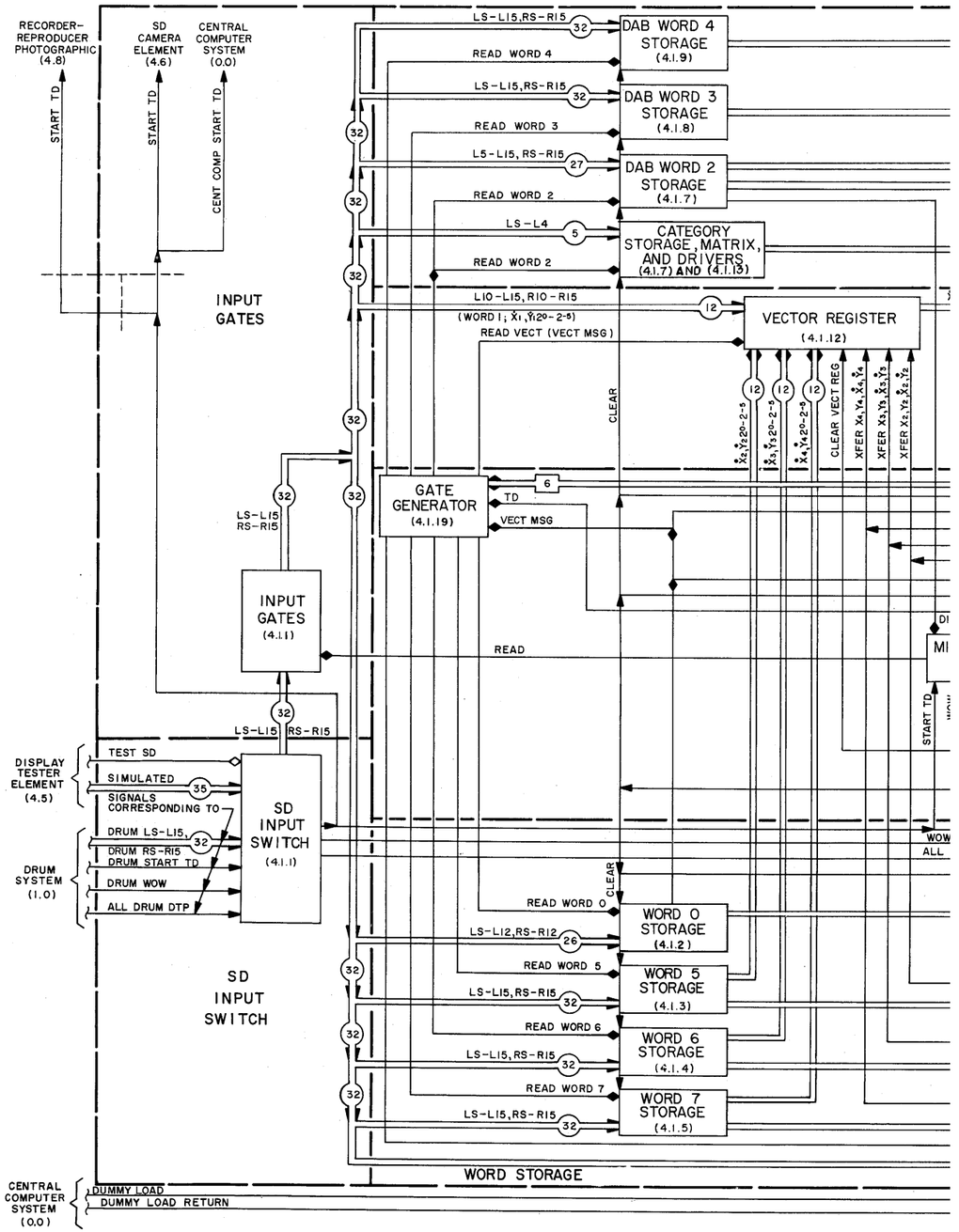


Figure 4-47. Situation Display Generator Element, Functional Block Diagram, Radar Data Message


RECORDER-REPRODUCER PHOTOGRAPHIC (4.8)
START TD
SD CAMERA ELEMENT (4.6)
START TD
CENTRAL COMPUTER SYSTEM (0.0)
CENT COMP START TD
INPUT GATES
LS-L15, RS-R15
DAB WORD 4 STORAGE (4.1.9)
READ WORD 4
DAB WORD 3 STORAGE (4.1.8)
READ WORD 3
L5-L15, RS-R15
DAB WORD 2 STORAGE (4.1.7)
READ WORD 2
LS-L4
CATEGORY STORAGE, MATRIX, AND DRIVERS (4.1.7) AND (4.1.13)
READ WORD 2
L10-L15, R10-R15
(WORD 1; X̄1, Ȳ120-2-5)
VECTOR REGISTER (4.1.12)
READ VECT (VECT MSG)
CLEAR
CLEAR VECT REG
XFER X4, Y4, X̄4, Ȳ4
XFER X3, Y3, X̄3, Ȳ3
XFER X2, Y2, X̄2, Ȳ2
GATE GENERATOR (4.1.19)
TD
VECT MSG
LS-L15 RS-R15
INPUT GATES (4.1.1)
READ
START TD
LS-L15 RS-R15
DISPLAY TESTER ELEMENT (4.5)
TEST SD
SIMULATED SIGNALS CORRESPONDING TO
DRUM LS-L15, DRUM RS-R15 DRUM START TD
DRUM WOW
ALL DRUM DTP
DRUM SYSTEM (1.0)
SD INPUT SWITCH (4.1.1)
SD INPUT SWITCH
CLEAR
READ WORD 0
WORD 0 STORAGE (4.1.2)
LS-L12, RS-R12
READ WORD 5
WORD 5 STORAGE (4.1.3)
LS-L15, RS-R15
READ WORD 6
WORD 6 STORAGE (4.1.4)
LS-L15, RS-R15
READ WORD 7
WORD 7 STORAGE (4.1.5)
LS-L15, RS-R15
WORD STORAGE
CENTRAL COMPUTER SYSTEM (0.0)
DUMMY LOAD
DUMMY LOAD RETURN

CATEGORY AND DAB STORAGE AND OUTPUT

VECTOR AND FORMAT GENERATOR

SD TIMING AND CONTROL

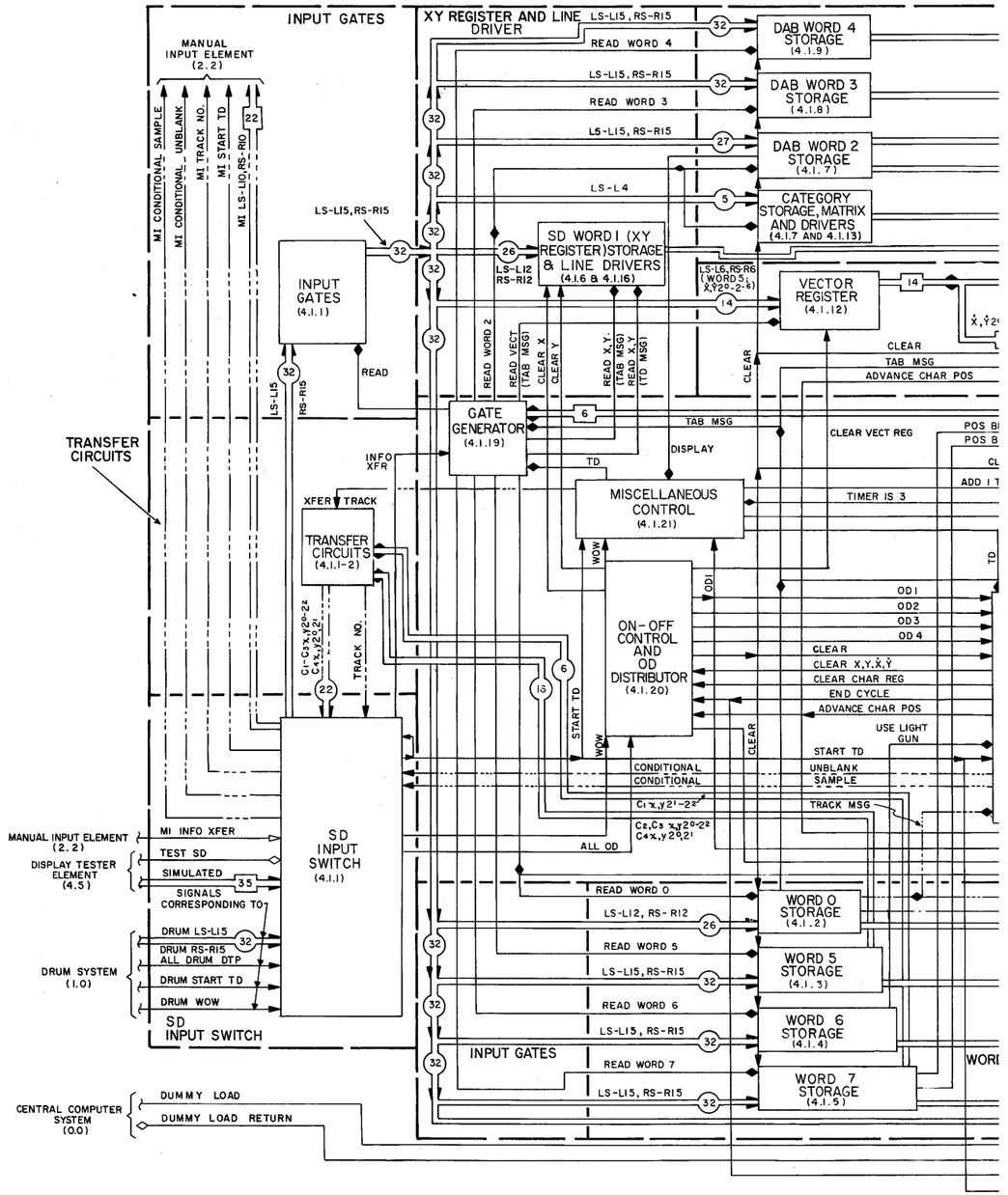
XY REGISTER AND LINE DRIVERS

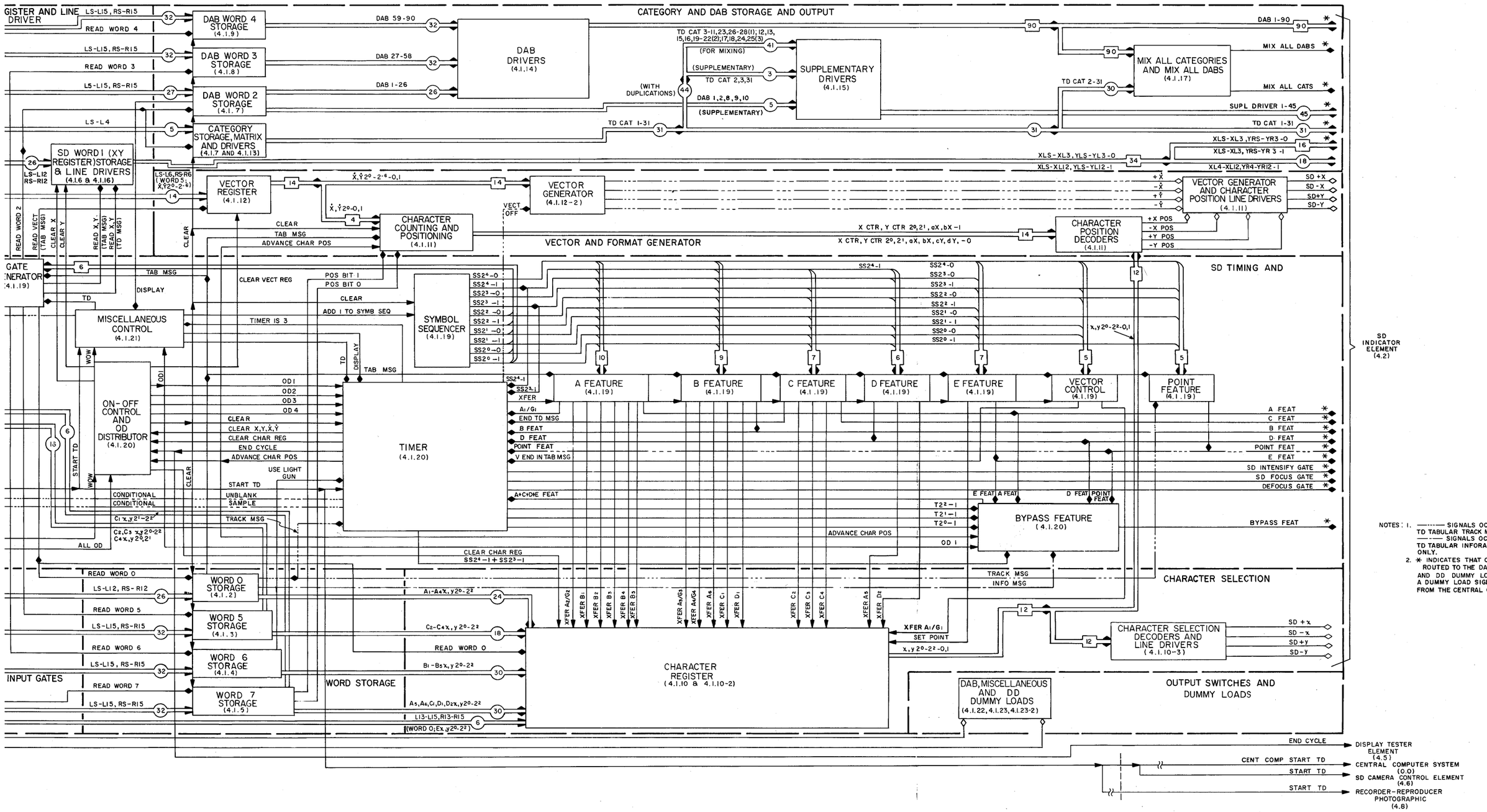
CHARACTER SELECTION

OUTPUT SWITCHES AND DUMMY LOADS

WORD STORAGE

Figure 4–48. Situation Display Generator Element, Functional Block Diagram, TD Vector Message


INPUT GATES
XY REGISTER AND LINE DRIVER
MANUAL INPUT ELEMENT (2.2)
MI CONDITIONAL SAMPLE
MI CONDITIONAL UNBLANK
MI TRACK NO.
MI START TD
MI LS-LIO, RS-RIO
TRANSFER CIRCUITS
INPUT GATES (4.1.1)
LS-LI5, RS-RI5
READ
LS-LI5
RS-RI0
XFER TRACK
TRANSFER CIRCUITS (4.1.1-2)
C1-C3 X,Y20-22 C1 X,Y21
TRACK NO.
SD INPUT SWITCH (4.1.1)
MANUAL INPUT ELEMENT (2.2)
MI INFO XFER
DISPLAY TESTER ELEMENT (4.5)
TEST SD
SIMULATED
SIGNALS CORRESPONDING TO
DRUM SYSTEM (1.0)
DRUM LS-LI5
DRUM RS-RI5
ALL DRUM DTP
DRUM START TD
DRUM WOW
SD INPUT SWITCH
CENTRAL COMPUTER SYSTEM (0.0)
DUMMY LOAD
DUMMY LOAD RETURN
DAB WORD 4 STORAGE (4.1.9)
READ WORD 4
DAB WORD 3 STORAGE (4.1.8)
READ WORD 3
DAB WORD 2 STORAGE (4.1.7)
LS-L4
CATEGORY STORAGE, MATRIX AND DRIVERS (4.1.7 AND 4.1.13)
SD WORD 1 (XY REGISTER) STORAGE & LINE DRIVERS (4.1.6 & 4.1.16)
LS-L12 RS-R12
LS-L6, RS-R6 (WORD 5, X,Y20,21)
VECTOR REGISTER (4.1.12)
READ WORD 2
READ VECT (TAB MSG)
CLEAR X
CLEAR Y
READ X,Y (TAB MSG)
READ X,Y (TD MSG)
CLEAR
TAB MSG
ADVANCE CHAR POS
GATE GENERATOR (4.1.19)
TAB MSG
DISPLAY
INFO XFR
TD
MISCELLANEOUS CONTROL (4.1.21)
CLEAR VECT REG
TIMER IS 3
WOW
ON-OFF CONTROL AND OD DISTRIBUTOR (4.1.20)
OD1
OD2
OD3
OD4
CLEAR
CLEAR X,Y,Ẋ,Ẏ
CLEAR CHAR REG
END CYCLE
ADVANCE CHAR POS
USE LIGHT GUN
START TD
UNBLANK
SAMPLE
TRACK MSG
CONDITIONAL
CONDITIONAL
C1 X,Y21-22
C2,C3 X,Y20-22 C4 X,Y20,21
ALL OD
START TD
WOW
CLEAR
READ WORD 0
LS-L12, RS-R12
WORD 0 STORAGE (4.1.2)
READ WORD 5
LS-LI5, RS-RI5
WORD 5 STORAGE (4.1.3)
READ WORD 6
LS-LI5, RS-RI5
WORD 6 STORAGE (4.1.4)
READ WORD 7
LS-LI5, RS-RI5
WORD 7 STORAGE (4.1.5)
INPUT GATES



NOTES: 1. ——— SIGNALS OCCURING IN TD TABULAR TRACK MESSAGES ONLY.
– – – – SIGNALS OCCURING IN TD TABULAR INFORATION MESSAGES ONLY.
2. * INDICATES THAT OUTPUT IS ROUTED TO THE DAB, MISCELLANEOUS AND DD DUMMY LOADS WHEN A DUMMY LOAD SIGNAL IS RECEIVED FROM THE CENTRAL COMPUTER SYSTEM.

Figure 4–49. Situation Display Generator Element, Functional Block Diagram, TD Tabular Message

6
6 CDG
A4/G4
A3/G3
A2/G2
A1/G1
C4
C3
C2
L13-L15, R13-R15
(E x, y 2⁰-2²)
INPUT GATES (4.1.1)
READ WORD 0
GATE GENERATOR (4.1.19)
24
A1/G1-A4/G4
x, y 20-2²-1
SD WORD 0 STORAGE (4.1.2)
XFER A4/G4
XFER A3/G3
B FEATURE (4.1.19)
XFER A2/G2
A FEATURE (4.1.19)
XFER A1/G1
VECTOR CONTROL (4.1.19)
18
C2-C4
x, y 20-2²-1
SD WORD 5 STORAGE (4.1.3)
XFER C4
XFER C3
XFER C2
C FEATURE (4.1.19)

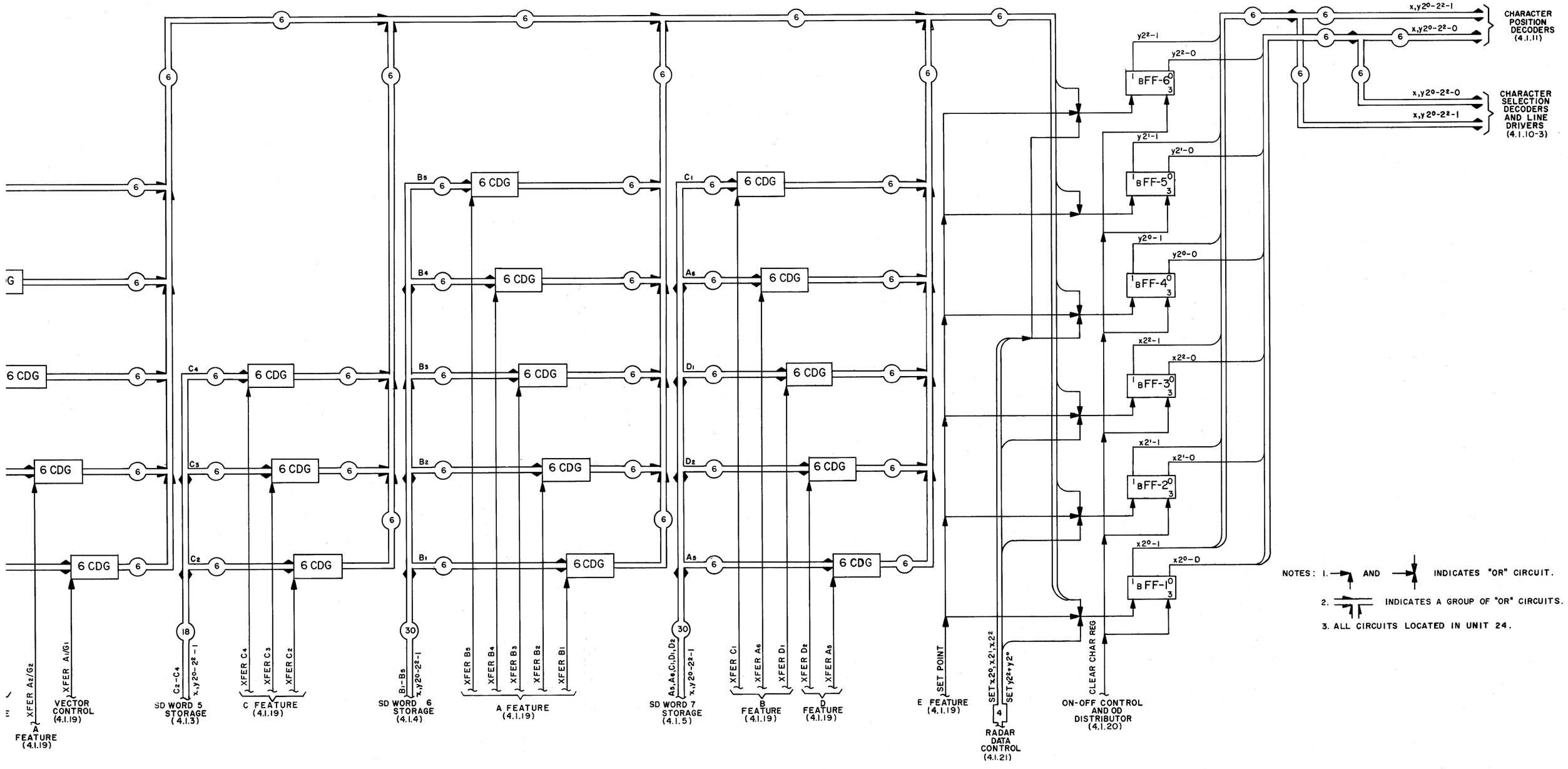
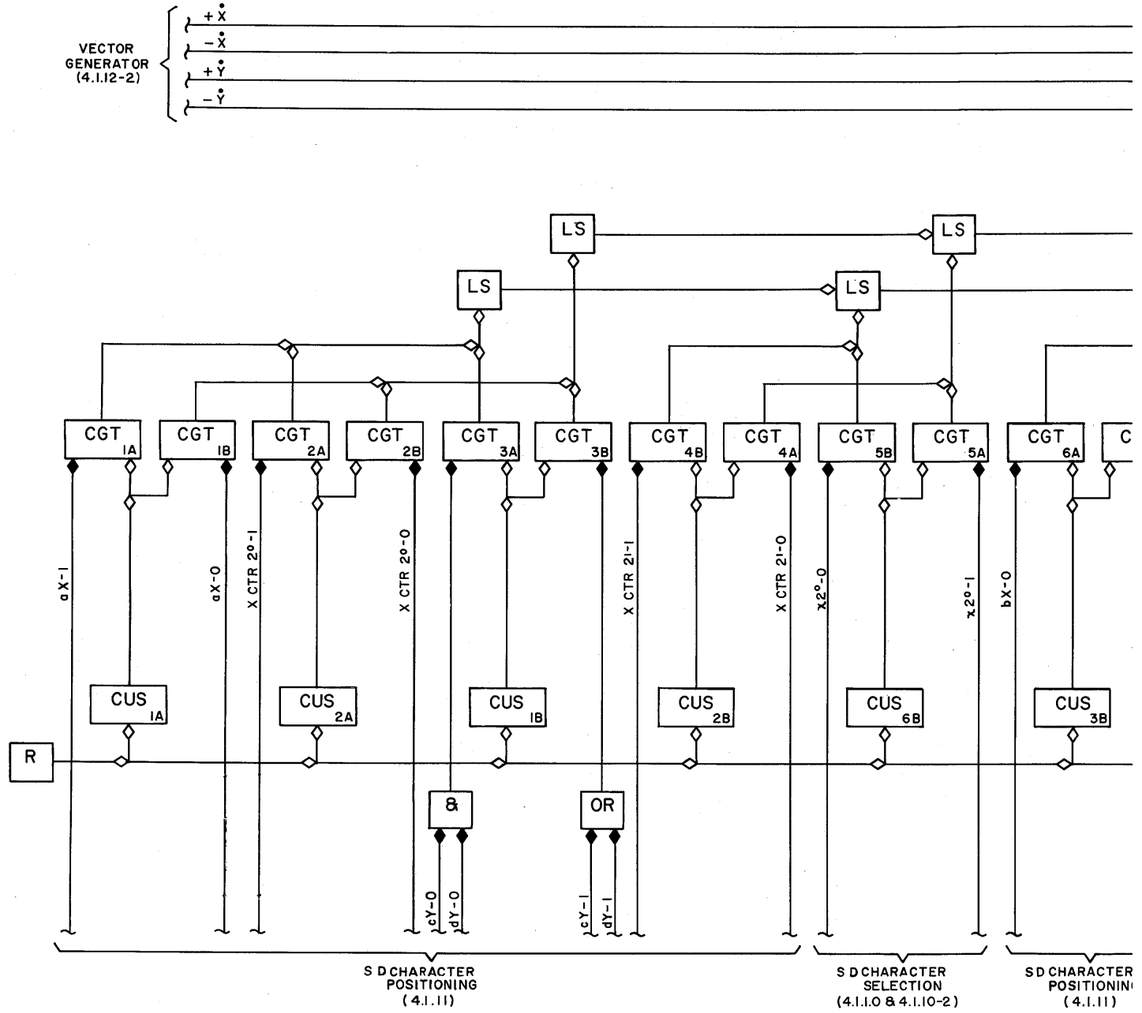
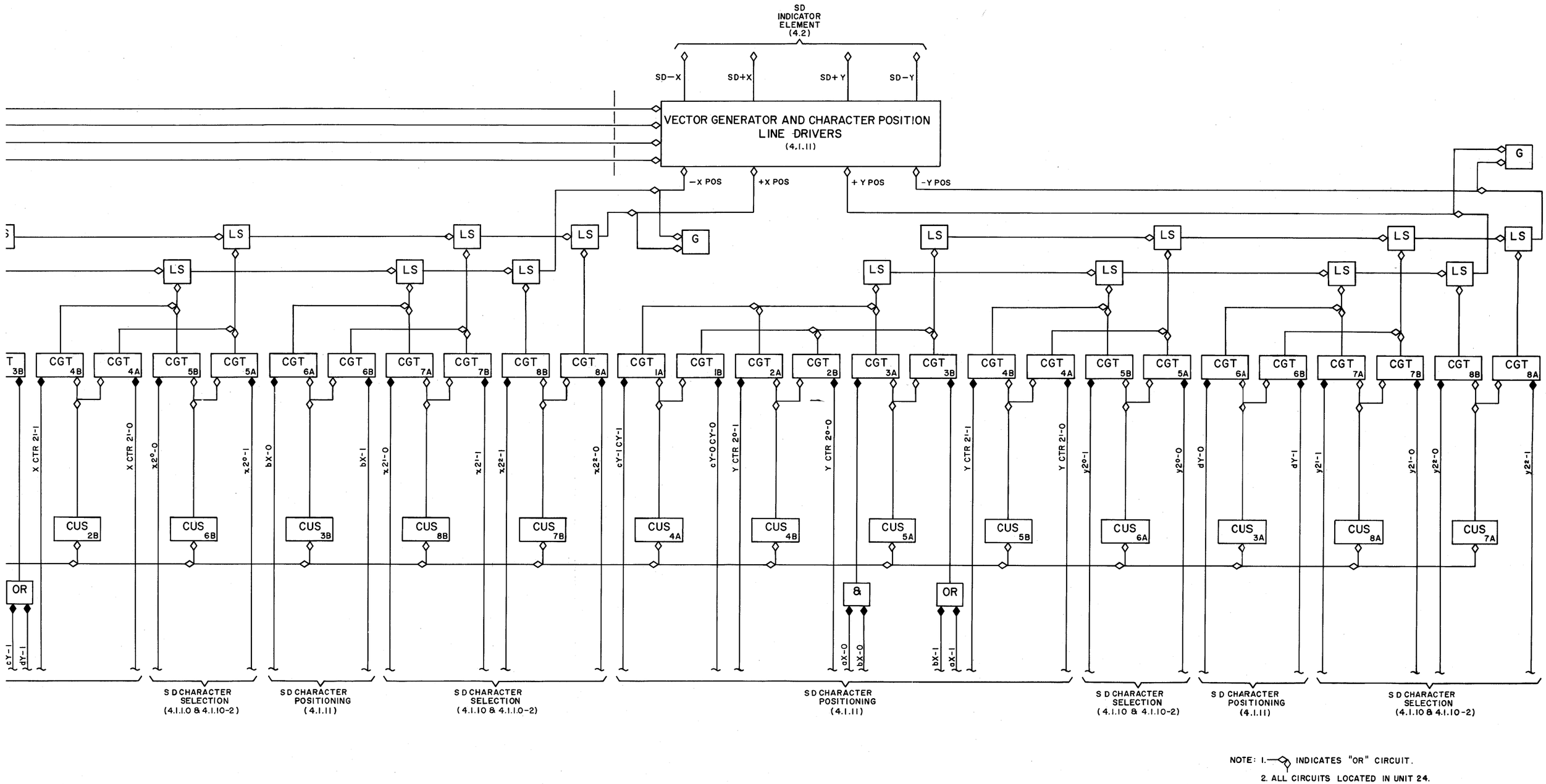


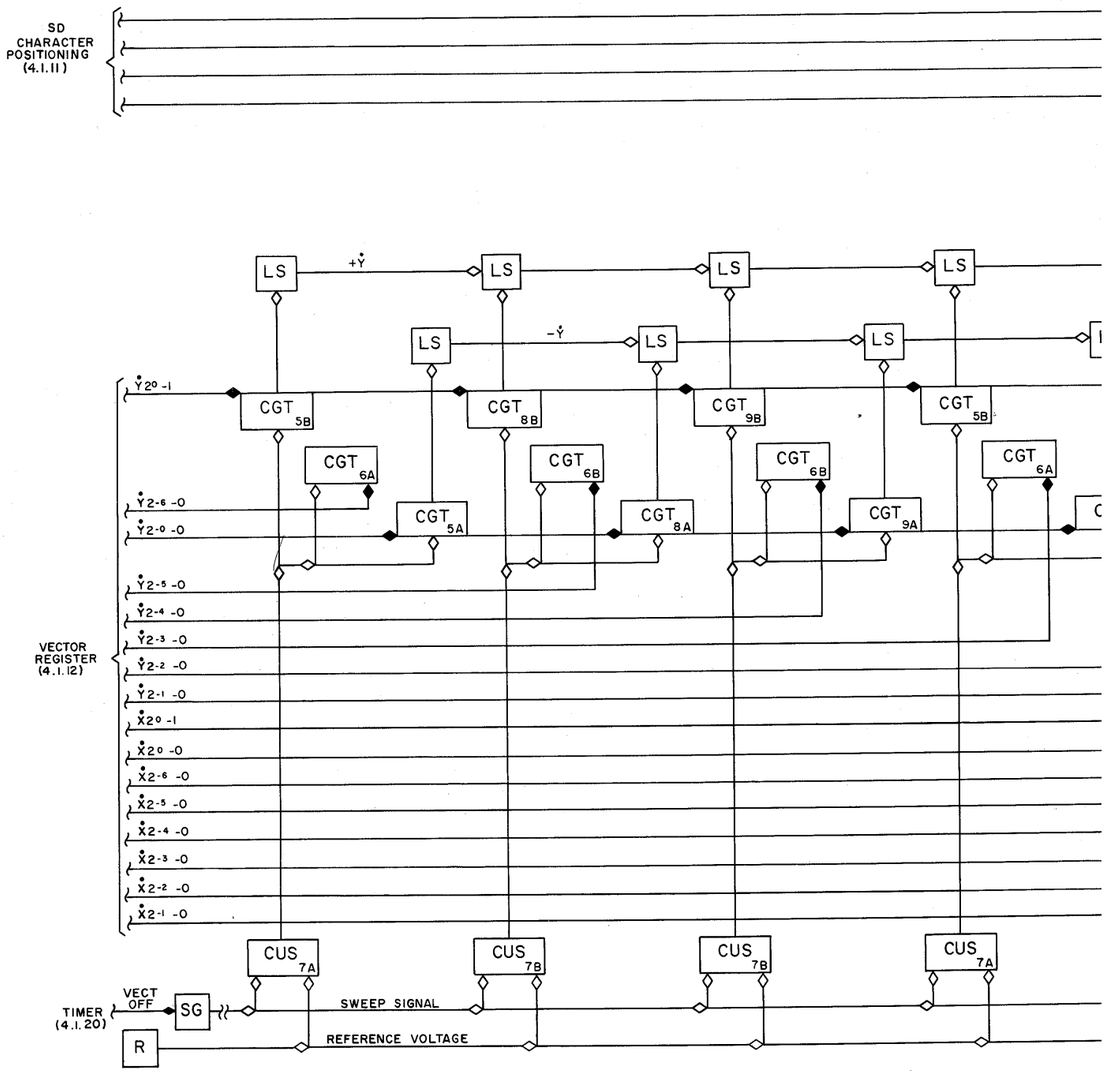
Figure 4-56. SD Character Selection Register Circuit, Logic Diagram

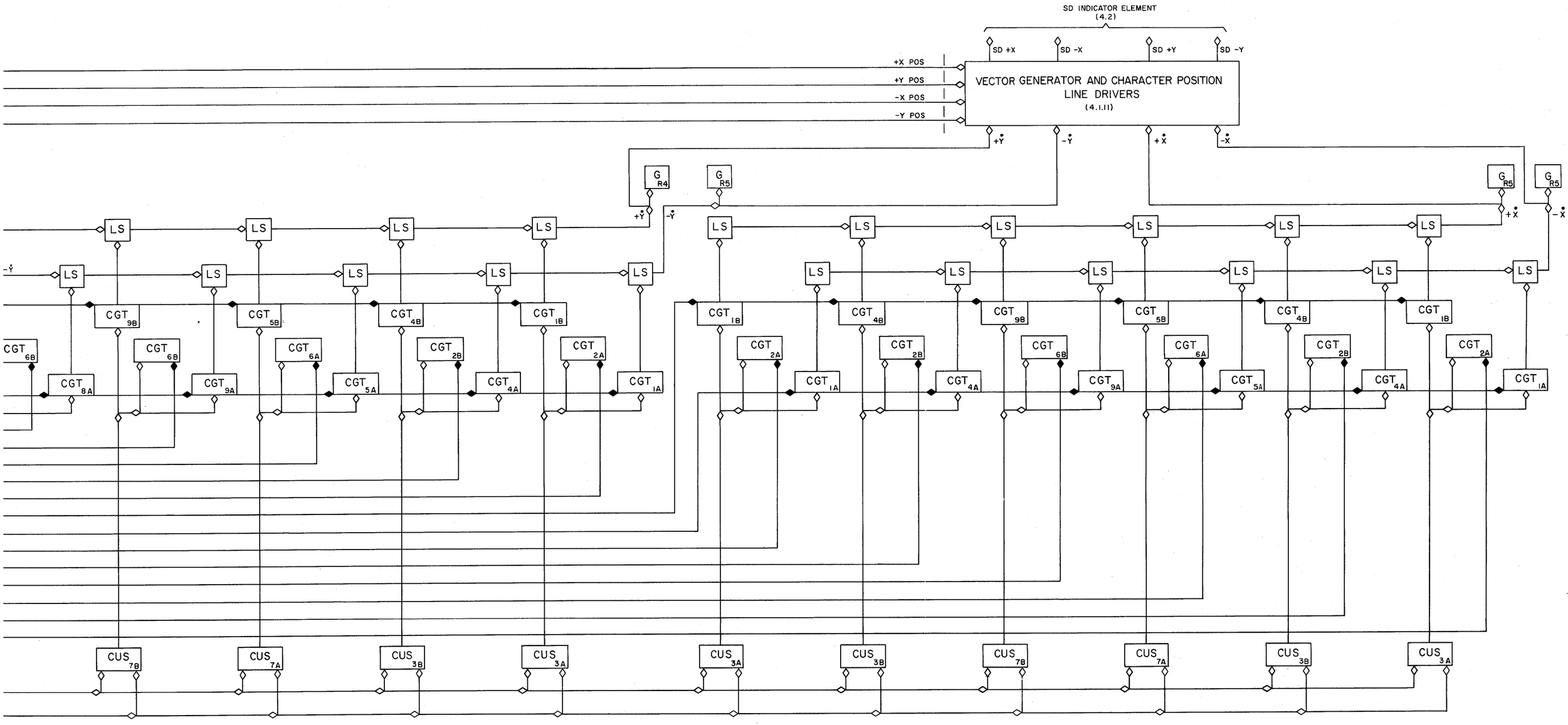

VECTOR GENERATOR (4.1.12-2)
+ẋ
−ẋ
+ẏ
−ẏ
LS
CGT 1A
CGT 1B
CGT 2A
CGT 2B
CGT 3A
CGT 3B
CGT 4B
CGT 4A
CGT 5B
CGT 5A
CGT 6A
aX-1
aX-0
X CTR 2⁰-1
X CTR 2⁰-0
X CTR 2¹-1
X CTR 2¹-0
x2⁰-0
x2⁰-1
bX-0
CUS 1A
CUS 2A
CUS 1B
CUS 2B
CUS 6B
CUS 3B
R
&
OR
cY-0
dY-0
cY-1
dY-1
S D CHARACTER POSITIONING (4.1.11)
S D CHARACTER SELECTION (4.1.10 & 4.1.10-2)
SD CHARACTER POSITIONIN (4.1.11)



NOTE: 1. ◇ INDICATES "OR" CIRCUIT.
2. ALL CIRCUITS LOCATED IN UNIT 24.

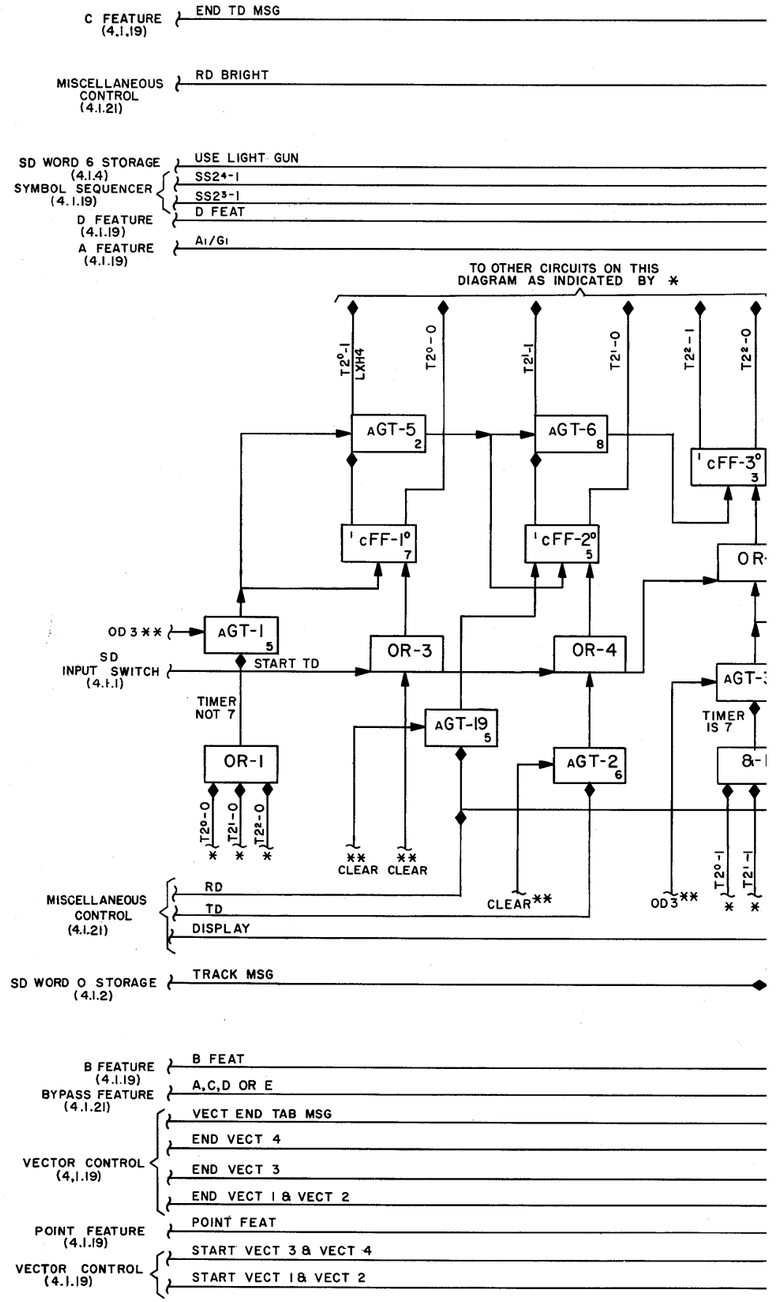
Figure 4–62. SD Character Positioning Decoder and Line Drivers Circuit, Logic Diagram


SD
CHARACTER
POSITIONING
(4.1.11)
LS
+Ẏ
-Ẏ
CGT 5B
CGT 8B
CGT 9B
CGT 5B
CGT 6A
CGT 6B
CGT 6B
CGT 6A
CGT 5A
CGT 8A
CGT 9A
VECTOR
REGISTER
(4.1.12)
Ẏ2⁰ -1
Ẏ2-6 -0
Ẏ2-0 -0
Ẏ2-5 -0
Ẏ2-4 -0
Ẏ2-3 -0
Ẏ2-2 -0
Ẏ2-1 -0
Ẋ2⁰ -1
Ẋ2⁰ -0
Ẋ2-6 -0
Ẋ2-5 -0
Ẋ2-4 -0
Ẋ2-3 -0
Ẋ2-2 -0
Ẋ2-1 -0
CUS 7A
CUS 7B
CUS 7B
CUS 7A
TIMER
(4.1.20)
VECT
OFF
SG
R
SWEEP SIGNAL
REFERENCE VOLTAGE



NOTE : 1. ALL CIRCUITS LOCATED IN UNIT 24.

Figure 4–65. Vector Generator Circuit, Logic Diagram


C FEATURE (4.1.19)
END TD MSG
MISCELLANEOUS CONTROL (4.1.21)
RD BRIGHT
SD WORD 6 STORAGE (4.1.4)
SYMBOL SEQUENCER (4.1.19)
D FEATURE (4.1.19)
A FEATURE (4.1.19)
USE LIGHT GUN
SS24-1
SS23-1
D FEAT
A1/G1
TO OTHER CIRCUITS ON THIS DIAGRAM AS INDICATED BY *
T20-1 LXH4
T20-0
T21-1
T21-0
T22-1
T22-0
AGT-5 2
AGT-6 8
1cFF-3 3
1cFF-1 7
1cFF-2 5
OR-
OD3**
AGT-1 5
SD INPUT SWITCH (4.1.1)
START TD
OR-3
OR-4
AGT-
TIMER NOT 7
TIMER IS 7
AGT-19 5
AGT-2 6
OR-1
8-
T20-0 *
T21-0 *
T22-0 *
** CLEAR
** CLEAR
CLEAR**
OD3**
T20-1 *
T21-1 *
MISCELLANEOUS CONTROL (4.1.21)
RD
TD
DISPLAY
SD WORD 0 STORAGE (4.1.2)
TRACK MSG
B FEATURE (4.1.19)
B FEAT
BYPASS FEATURE (4.1.21)
A,C,D OR E
VECTOR CONTROL (4,1.19)
VECT END TAB MSG
END VECT 4
END VECT 3
END VECT 1 & VECT 2
POINT FEATURE (4.1.19)
POINT FEAT
VECTOR CONTROL (4.1.19)
START VECT 3 & VECT 4
START VECT 1 & VECT 2

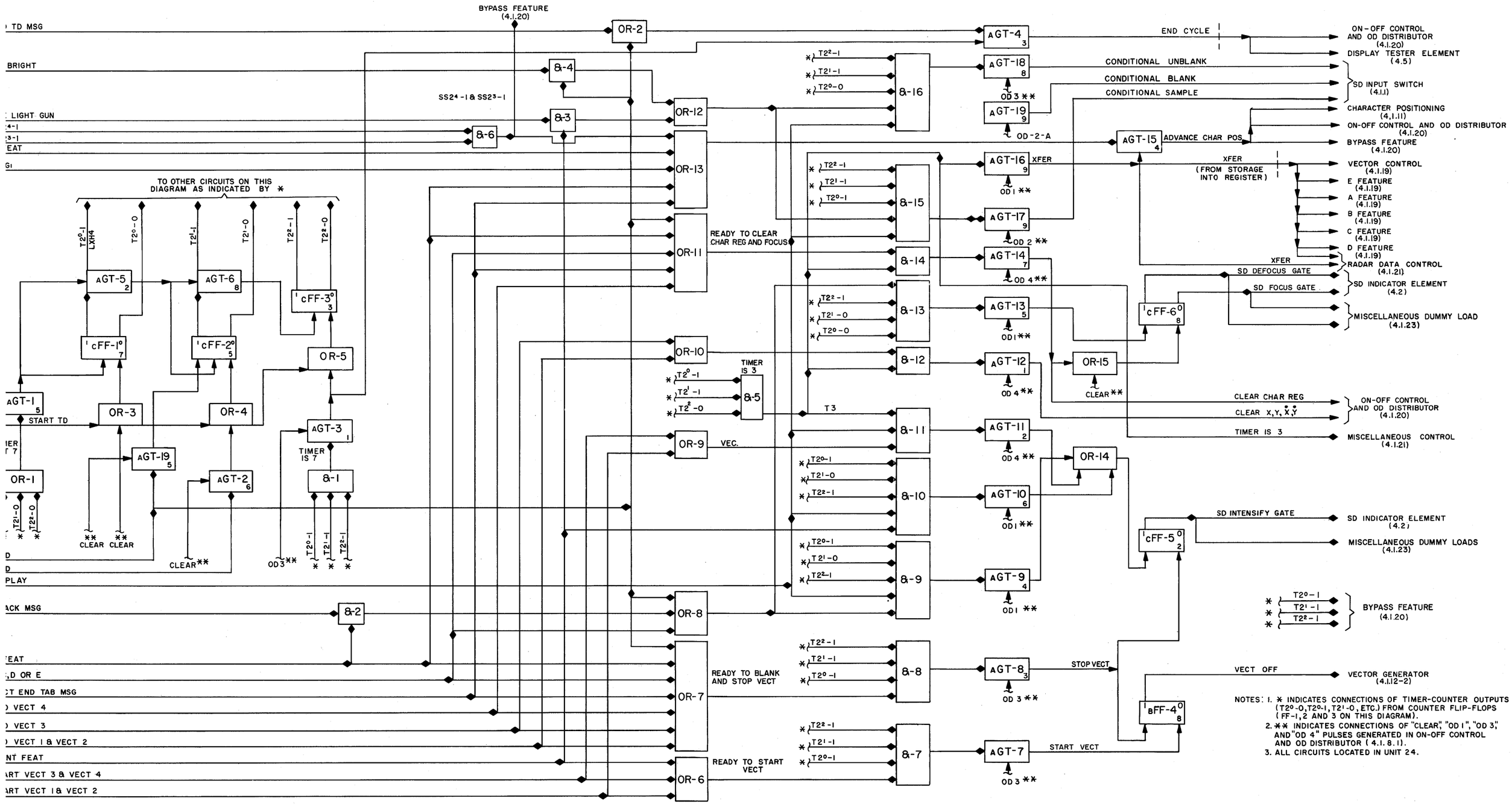
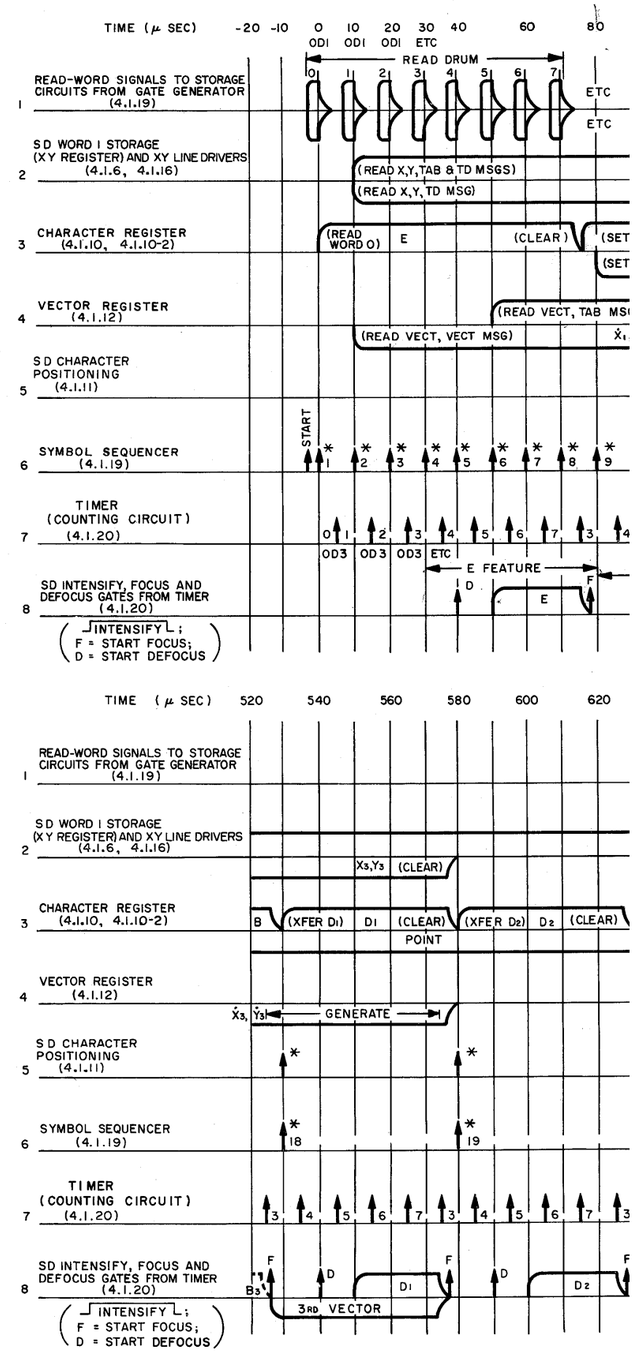
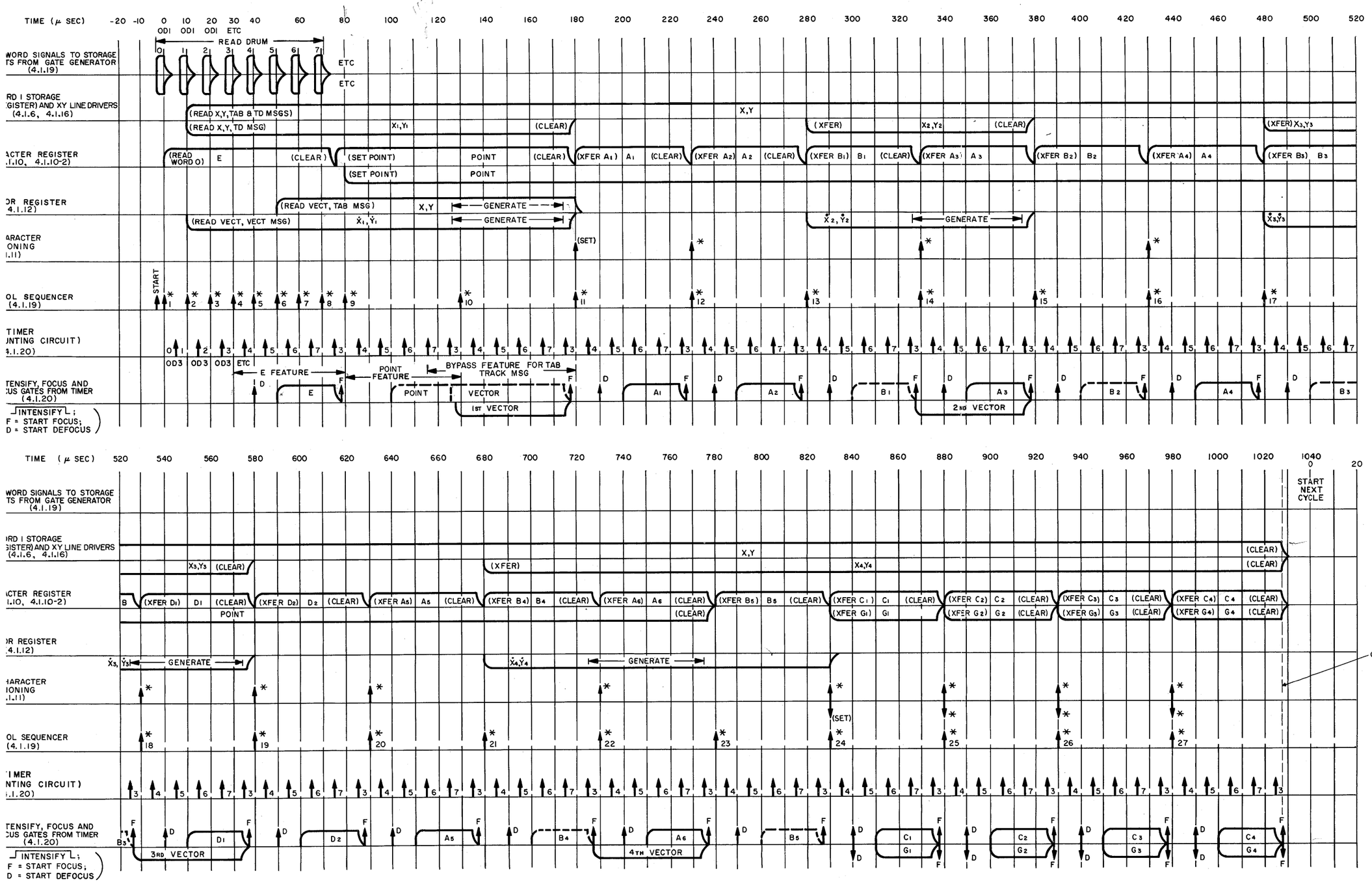


Figure 4-92. Timer Circuit, Logic Diagram


TIME (μ SEC)
-20 -10 0 10 20 30 40 60 80
ODI ODI ODI ETC
READ DRUM
1 READ-WORD SIGNALS TO STORAGE CIRCUITS FROM GATE GENERATOR (4.1.19)
ETC
ETC
2 SD WORD I STORAGE (XY REGISTER) AND XY LINE DRIVERS (4.1.6, 4.1.16)
(READ X,Y,TAB & TD MSGS)
(READ X,Y,TD MSG)
3 CHARACTER REGISTER (4.1.10, 4.1.10-2)
(READ WORD 0)
E
(CLEAR)
(SET
(SET
4 VECTOR REGISTER (4.1.12)
(READ VECT, TAB MS
(READ VECT, VECT MSG)
Ẋ1
5 SD CHARACTER POSITIONING (4.1.11)
START
6 SYMBOL SEQUENCER (4.1.19)
1 2 3 4 5 6 7 8 9
7 TIMER (COUNTING CIRCUIT) (4.1.20)
0 1 2 3 4 5 6 7 3 4
OD3 OD3 OD3 ETC
E FEATURE
8 SD INTENSIFY, FOCUS AND DEFOCUS GATES FROM TIMER (4.1.20)
D
E
F
(INTENSIFY; F = START FOCUS; D = START DEFOCUS)
TIME (μ SEC)
520 540 560 580 600 620
1 READ-WORD SIGNALS TO STORAGE CIRCUITS FROM GATE GENERATOR (4.1.19)
2 SD WORD I STORAGE (XY REGISTER) AND XY LINE DRIVERS (4.1.6, 4.1.16)
Xs,Ys
(CLEAR)
3 CHARACTER REGISTER (4.1.10, 4.1.10-2)
B
(XFER D1)
D1
(CLEAR)
(XFER D2)
D2
(CLEAR)
POINT
4 VECTOR REGISTER (4.1.12)
Ẋs, Ẏs1
GENERATE
5 SD CHARACTER POSITIONING (4.1.11)
6 SYMBOL SEQUENCER (4.1.19)
18
19
7 TIMER (COUNTING CIRCUIT) (4.1.20)
3 4 5 6 7 3 4 5 6 7 3
8 SD INTENSIFY, FOCUS AND DEFOCUS GATES FROM TIMER (4.1.20)
F
D
B3
D1
D2
3RD VECTOR
(INTENSIFY; F = START FOCUS; D = START DEFOCUS)



NOTES:
1. ITEMS BELOW LINES REFER TO TD VECTOR MESSAGES.
2. ITEMS ABOVE LINES REFER TO TD TABULAR MESSAGES.
3. ——— INDICATES ITEMS MISSING IN ALL TD TABULAR INFORMATION MESSAGES.
4. * INDICATES A STEPPING PULSE.
5. BYPASS FEATURE IS GENERATED DURING ENTIRE TD VECTOR MESSAGE.
6. BYPASS FEATURE FOR TD TABULAR INFORMATION MESSAGE – A, C, D, AND E CHARACTERS.

Figure 4–93. TD Message Display Cycles, Timing Chart