C654-416L-CD

AIR TRAINING COMMAND

COMPUTER SYSTEMS DEPARTMENT

AN/FSQ-7 DRUM SYSTEM

CHARTS & DIAGRAMS

5 JANUARY 1965

Course Nr. ABR30533-1

KEESLER AFB, MISS

This Schematics and Logic Diagrams Book provides student study material in support of Type II and Type III computer maintenance courses relating to WS416L.

SCHEMATICS

FOR

DRUM SYSTEM

OF

AN/FSQ-7
COMBAT DIRECTION CENTRAL

TRAINING MANUAL

1, September 1961

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KINGSTON, NEW YORK

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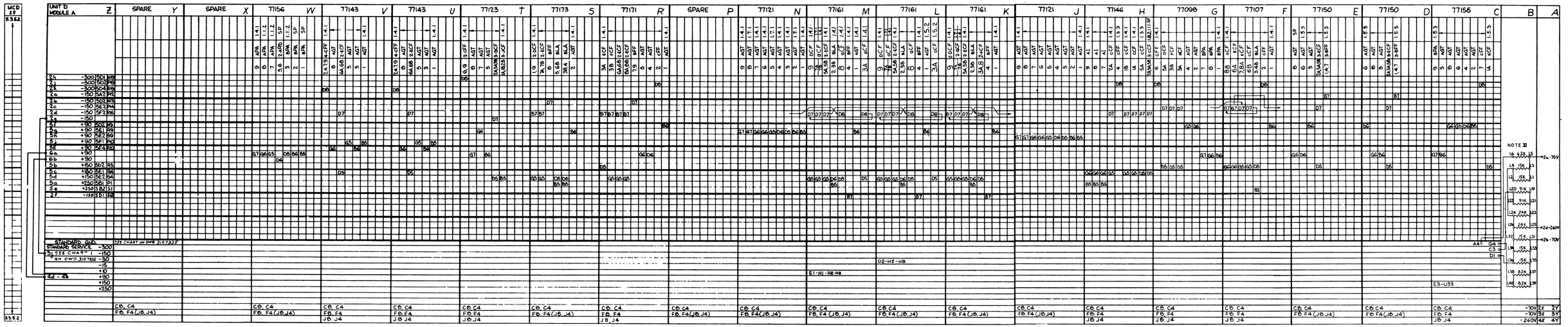
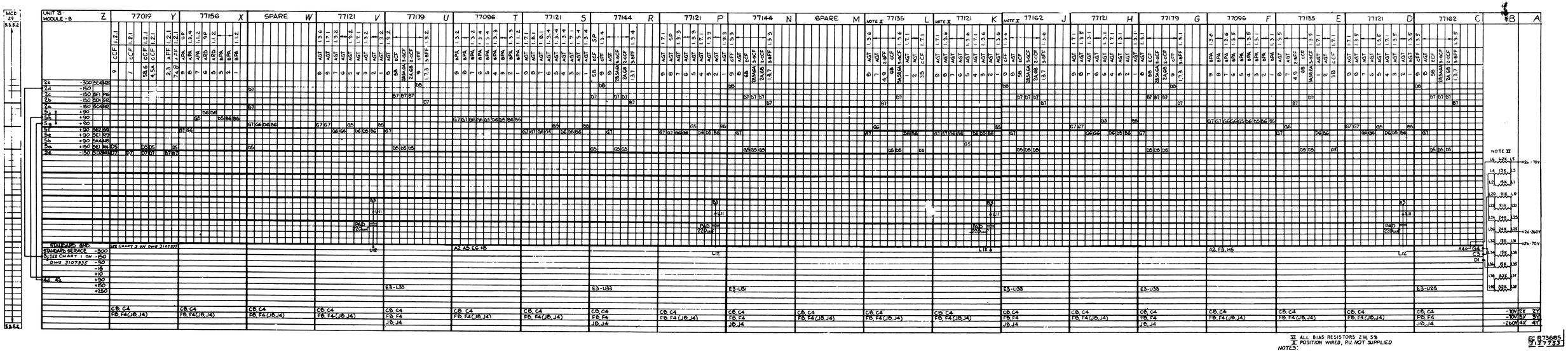
92-1879

L I S T O F C O N T E N T S

LOGIC	DESCRIPTION
1. 0. 1	MODULE 21 A&B
1. 1. 1	7AIN DRUM SELECTION & DIODE SWITCH
1. 1. 1- 2	RD DRUM CD SELECTION & SWITCHING
1. 1. 2	MAIN DRUM TIMING & DISTRIBUTION
1. 2. 1	MAIN DRUM ADDRESSABLE CONTROL CIRCUIT
1. 2. 2	MAIN DRUMS CD READ CIRCUITS & READ BUS.
1. 2. 3	MAIN DRUMS APC & ALARM CIRCUITS
1. 3. 1	MANUAL INPUT STATUS CONTROLS
1. 3. 3	LONG RANGE RADAR INPUT NO. 1-OPERATE CIRCUITRY
1. 3. 4	LONG RANGE RADAR INPUT NO. 2-OPERATE CIRCUITRY
1. 3. 5	CROSSTELL OPERATE CIRCUITRY
1. 3. 6	SPARE CROSSTELL OPERATE CIRCUITRY
1. 4. 1	MAIN DRUM OUTPUT BUFFER STATUS OPERATE
1. 5. 1	SITUATION DISPLAY RD & TD OPERATE CIRCUITRY
1. 5. 2	SITUATION DISPLAY OD FIELD SWITCHING & READ CIRCUITRY
1. 5. 3	DIGITAL DISPLAY OD CONTROLS & READ CIRCUITS
S1. 6. 1	OD IC FIELD COMP. A&B
1. 7. 1	MAIN DRUMS MANUAL CONTROLS
1. 7. 1- 2	MAIN DRUMS TEST PANEL NEON WIRING
1. 7. 2	MAIN DRUM MANUAL READ-WRITE CONTROLS
1. 7. 3	MAIN DRUM ERASE & WRITE INDEX & TIMING CHANNELS
1. 7. 3- 2	COMMON & SPECIAL SERVICE WIRING
1. 8. 1	MAIN DRUM LOOP TEST WRITE
1. 8. 2	MAIN DRUM LOOP TEST READ
1. 8. 3	INTERCOMMUNICATION TEST CONTROLS
1- 2. 1. 1	AXD DRUM SELECTION & DIODE SWITCHING
1- 2. 1. 2	AXD TIMING & DISTRIBUTION
1- 2. 2. 1	AXD DRUMS CONTROL & WRITE CIRCUITS
1- 2. 2. 2	AXD READ CIRCUITS
1. 2. 2. 3	AXD APC & ALARM CIRCUITS
1- 2. 3. 1	AUXILIARY DRUM UNIT MANUAL CONTROLS
1- 2. 3. 1- 2	AXD DRUMS TEST PANEL NEON WIRING
1- 2. 3. 2	AXD MANUAL TEST READ-WRITE CONTROLS
1- 2. 3. 3	AUXILIARY DRUMS ERASE & WRITE TIMING & INDEX CHANNELS





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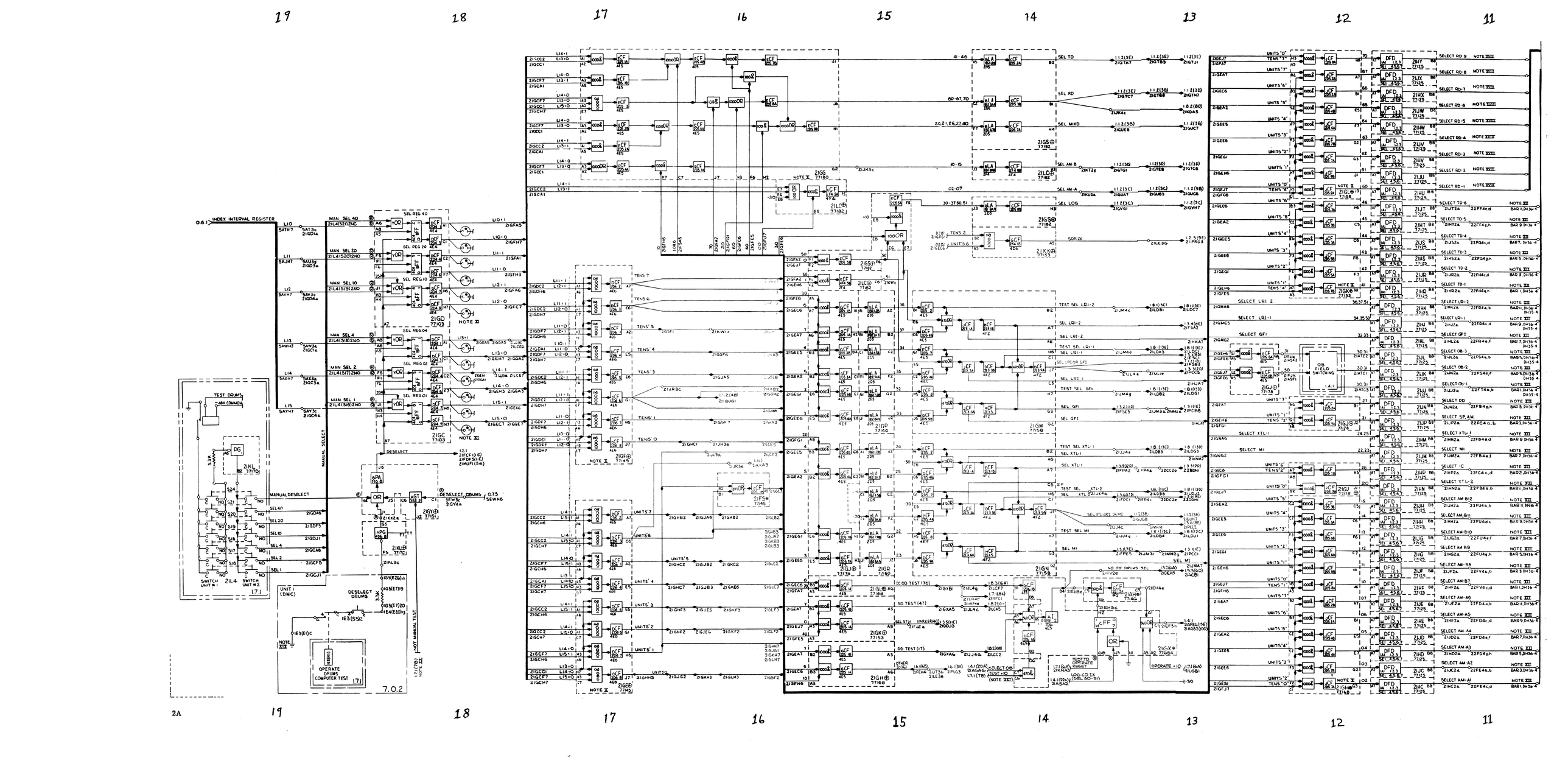
3107335


19
18
17
16
15
14
13
12
11
INDEX INTERVAL REGISTER
MANUAL SELECT
SEL REG 40
SEL REG 20
SEL REG 10
SEL REG 4
SEL REG 2
SEL REG 1
MAN. SEL 40
MAN. SEL 20
MAN. SEL 10
MAN. SEL 4
MAN. SEL 2
MAN. SEL 1
TEST DRUMS
ABV COMMON
SWITCH UNIT #1
SWITCH UNIT #2
MANUAL DESELECT
DESELECT DRUMS
UNIT 1 (DMC)
OPERATE DRUMS COMPUTER TEST
NOT MANUAL TEST
TENS 7
TENS 6
TENS 5
TENS 4
TENS 3
TENS 2
TENS 1
TENS 0
UNITS 7
UNITS 6
UNITS 5
UNITS 4
UNITS 3
UNITS 2
UNITS 1
UNITS 0
TEST SEL LRI-2
SEL LRI-2
TEST SEL LRI-1
SEL LRI-1
TEST SEL GF1
SEL GF1
TEST SEL XTL-1
SEL XTL-1
TEST SEL XTL-2
SEL XTL-2
TEST SEL MI
SEL MI
SEL TD
SEL RD
SEL MIXED
SEL AM-B
SEL AM-A
SEL LOG
SELECT LRI 2
SELECT LRI-1
SELECT GF1
SELECT OB-1
SELECT OB-2
SELECT SP, AM
SELECT XTL-1
SELECT XTL-2
SELECT MI
SELECT IC
SELECT AM-B12
SELECT AM-B11
SELECT AM-B10
SELECT AM-B9
SELECT AM-B8
SELECT AM-B7
SELECT AM-A6
SELECT AM-A5
SELECT AM-A4
SELECT AM-A3
SELECT AM-A2
SELECT AM-A1
SELECT RD-9
SELECT RD-8
SELECT RD-7
SELECT RD-6
SELECT RD-5
SELECT RD-4
SELECT RD-3
SELECT RD-2
SELECT RD-1
SELECT TD-6
SELECT TD-5
SELECT TD-4
SELECT TD-3
SELECT TD-2
SELECT TD-1
OB FIELD SWITCHING
DESELECT DRUMS
OPERATE +10
NO DD DRUMS SEL
IC DD TEST (76)
SD TEST (47)
DD TEST (17)
7.0.2
2A

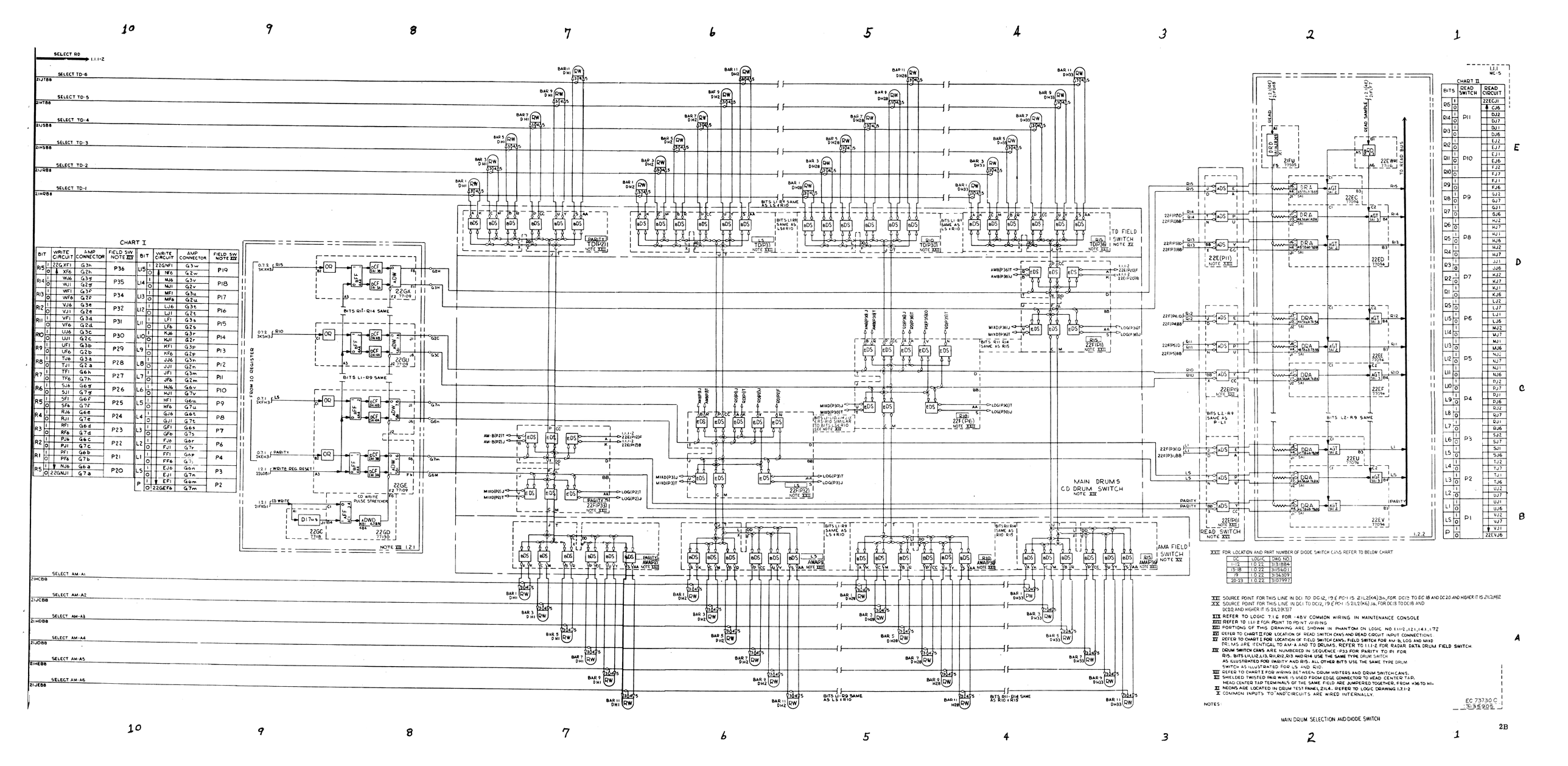

SELECT RD
SELECT TD-6
SELECT TD-5
SELECT TD-4
SELECT TD-3
SELECT TD-2
SELECT TD-1
SELECT AM-A1
SELECT AM-A2
SELECT AM-A3
SELECT AM-A4
SELECT AM-A5
SELECT AM-A6
CHART I
CHART II
MAIN DRUMS C.D. DRUM SWITCH NOTE XIV
TD FIELD SWITCH NOTE XX
AMA FIELD SWITCH NOTE XX
READ SWITCH NOTE XXI
MAIN DRUM SELECTION AND DIODE SWITCH
NOTES:
XXII FOR LOCATION AND PART NUMBER OF DIODE SWITCH CANS REFER TO BELOW CHART
XII SOURCE POINT FOR THIS LINE IN DC1 TO DC12, 19 E PC-1 IS 21L2(K4)3a, FOR DC13 TO DC18 AND DC20 AND HIGHER IT IS 21L2(K8)2
XX SOURCE POINT FOR THIS LINE IN DC1 TO DC12, 19 E PC-1 IS 21L2(K6)3a, FOR DC13 TO DC18 AND DC20 AND HIGHER IT IS 21L2(K3)7
XIII REFER TO LOGIC 7.1 G FOR -48V COMMON WIRING IN MAINTENANCE CONSOLE
XIII REFER TO 1.1-2 FOR POINT TO POINT WIRING
XXII PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM ON LOGIC NO. 1.1-2, 1.2.1, 1.4.1, 1.7.2
XII REFER TO CHART II FOR LOCATION OF READ SWITCH CANS AND READ CIRCUIT INPUT CONNECTIONS
XV REFER TO CHART I FOR LOCATION OF FIELD SWITCH CANS. FIELD SWITCH FOR AM-B, LOG AND MIXD DRUMS ARE IDENTICAL TO AM-A AND TD DRUMS. REFER TO 1.1-2 FOR RADAR DATA DRUM FIELD SWITCH.
XIII DRUM SWITCH CANS ARE NUMBERED IN SEQUENCE - P33 FOR PARITY, TO P1 FOR R15. BITS L11, L12, L13, R11, R12, R13 AND R14 USE THE SAME TYPE DRUM SWITCH AS ILLUSTRATED FOR PARITY AND R15. ALL OTHER BITS USE THE SAME TYPE DRUM SWITCH AS ILLUSTRATED FOR L5 AND R10
XIII SHIELDED TWISTED PAIR WIRE IS USED FROM EDGE CONNECTOR TO HEAD CENTER TAP. HEAD CENTER TAP TERMINALS OF THE SAME FIELD ARE JUMPERED TOGETHER, FROM #36 TO #1.
XI NEONS ARE LOCATED IN DRUM TEST PANEL 21L4. REFER TO LOGIC DRAWING 1.7.1-2
X COMMON INPUTS TO "AND" CIRCUITS ARE WIRED INTERNALLY.
EC 73730 C
3195905
MAIN DRUM SELECTION AND DIODE SWITCH
2B

CHART I

RADAR DISPLAY DRUM

BIT		WRITE CIRCUIT	AMP CONN	FIELD SWITCH	DUMMY LOAD
R15	I	22GXF1	G3h		P20
	O	22GXF6	G2h		
R14	I	22GWJ6	G3g		P19
	O	22GWJ1	G2g		
R13	I	22GWF1	G3f		P18
	O	22GWF6	G2f		
R12	I	22GVJ6	G3e		P17
	O	22GVJ1	G2e		
R11	I	22GVF1	G3d		P16
	O	22GVF6	G2d		
R10	I	22GUJ6	G3c	P36,P35	*
	O	22GUJ1	G2c		
R9	I	22GUF1	G3b	P34,P35	*
	O	22GUF6	G2b		
R8	I	22GTJ6	G3a	P33,P29	*
	O	22GTJ1	G2a		
R7	I	22GTF1	G6h	P30,P29	*
	O	22GTF6	G7h		
R6	I	22GSJ6	G6g	P31,P32	*
	O	22GSJ1	G7g		
R5	I	22GSF1	G6f	P28,P32	*
	O	22GSF6	G7f		
R4	I	22GRJ6	G6e	P27,P26	*
	O	22GRJ1	G7e		
R3	I	22GRF1	G6d	P25,P26	*
	O	22GRF6	G7d		
R2	I	22GPJ6	G6c	P21,P22	*
	O	22GPJ1	G7c		
R1	I	22GPF1	G6b	P23,P22	*
	O	22GPF6	G7b		
R5	I	22GNJ6	G6a	P24,P20	*
	O	22GNJ1	G7a		
L15	I	22GNF1	G3w	P19,P20	*
	O	22GNF6	G2w		
L14	I	22GMJ6	G3v	P18,P17	*
	O	22GMJ1	G2v		
L13	I	22GMF1	G3u		P15
	O	22GMF6	G2u		
L12	I	22GLJ6	G3t		P14
	O	22GLJ1	G2t		
L11	I	22GLF1	G3s		P13
	O	22GLF6	G2s		
L10	I	22GKJ6	G3r	P13,P17	*
	O	22GKJ1	G2r		
L9	I	22GKF1	G3p	P14,P15	*
	O	22GKF6	G2p		
L8	I	22GJJ6	G3n	P16,P15	*
	O	22GJJ1	G2n		
L7	I	22GJF1	G3m	P12,P11	*
	O	22GJF6	G2m		
L6	I	22GHJ6	G6v	P10,P11	*
	O	22GHJ1	G7v		
L5	I	22GHF1	G6u	P9,P5	*
	O	22GHF6	G7u		
L4	I	22GGJ6	G6t	P6,P5	*
	O	22GGJ1	G7t		
L3	I	22GGF1	G6s	P7,P8	*
	O	22GGF6	G7s		
L2	I	22GFJ6	G6r	P4,P8	*
	O	22GFJ1	G7r		
L1	I	22GFF1	G6p	P3,P2	*
	O	22GFF6	G7p		
L5	I	22GEJ6	G6n	P1,P2	*
	O	22GEJ1	G7n		
P	I	22GEF1	G6m		P12
	O	22GEF6	G7m		

*THIS BIT USES ONLY HALF OF THIS CAN

CHART II

RD FIELD SELECTION

SELECT FIELD 1 — 22E(P12)M — B1, DH1-4 — B1, DH2-4
SELECT FIELD 2 — 22E(P21R — B3, DH1-4 — B3, DH2-4
SELECT FIELD 3 — 22E(P21Y — B5, DH1-4 — B5, DH2-4
SELECT FIELD 4 — 22E(P12)W — B7, DH1-4 — B7, DH2-4
SELECT FIELD 5 — 22E(P12)Z — B9, DH2-4 — B9, DH1-4
SELECT FIELD 6 — 22E(P12)X — B11, DH1-4 — B11, DH2-4
SELECT FIELD 7 — 22E(P12)A — B3, DH36-4 — B3, DH36-4
SELECT FIELD 8 — 22E(P12)C — B7, DH36-4 — B5, DH36-4
SELECT FIELD 9 — 22F(P12)P — B11, DH34-4 — B9, DH38-4

SELECT RD-9 NOTE X 21HYB8
SELECT RD-8 NOTE X 21JXB8
SELECT RD-7 NOTE X 21HXB8
SELECT RD-6 NOTE X 21JWB8
SELECT RD-5 NOTE X 21HWB8
SELECT RD-4 NOTE X 21JVB8
SELECT RD-3 NOTE X 21HVB8
SELECT RD-2 NOTE X 21JUB8
SELECT RD-1 NOTE X 21HUB8

DDS — PARITY 22E(P12) B 3107960
DDS — 22E(P13) B 3107960
DDS — 22E(P14) B 3107960

RD(P1) 3107964
RD(P2) 3107964
RD(P19) 3107964
RD(P17) 3107964

BITS L1-L9 SAME AS LS NOTE XIII

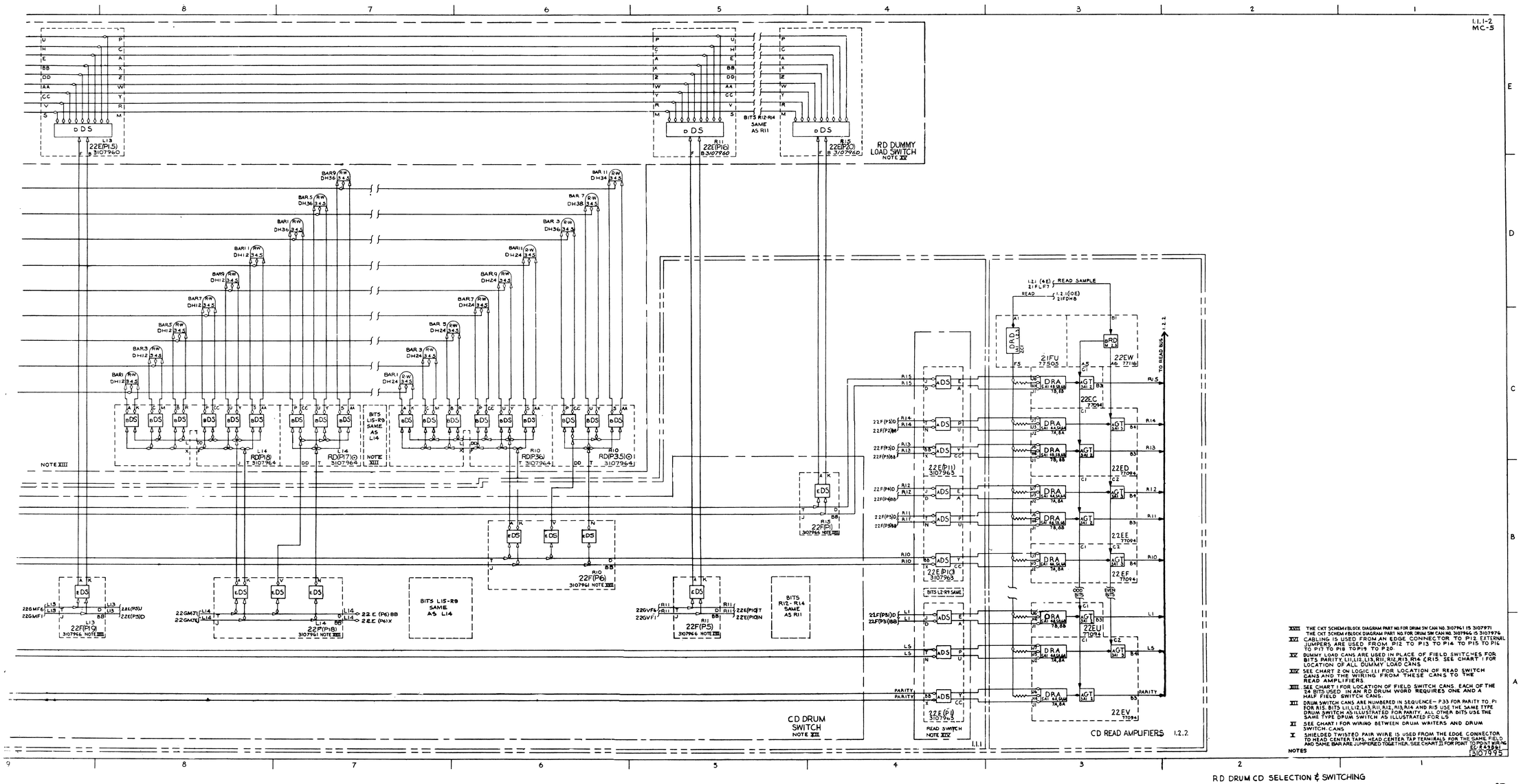
22F(P22) 3107961 NOTE XIII
22F(P21) 3107966 NOTE XIII
22F(P20) 3107966 NOTE XIII
22F(P32) 3107961 NOTE XIII
22F(P33) 3107966 NOTE XIII

RD CD FIELD SWITCH

CD DRUM WRITERS

22GX 77109 — R15 — BITS R11-R14 SAME AS P & LS
22GU 77109 — R10 — BITS L1-R9 SAME AS P & LS
22GE 77109 — LS
22GC 77118 — D 1.7μs
22GD 77130 — PARITY — FROM JD REG — WRITE REG RESET — CD WRITE

NOTE XI 1.2.1



XXII THE CKT SCHEM 4 BLOCK DIAGRAM PART NO FOR DRUM SW CAN NO. 3107961 IS 3107971
THE CKT SCHEM 4 BLOCK DIAGRAM PART NO FOR DRUM SW CAN NO. 3107964 IS 3107976

XVI CABLING IS USED FROM AN EDGE CONNECTOR TO P12, EXTERNAL JUMPERS ARE USED FROM P12 TO P13 TO P14 TO P15 TO P16 TO P17 TO P18 TO P19 TO P20.

XV DUMMY LOAD CANS ARE USED IN PLACE OF FIELD SWITCHES FOR BITS PARITY, L11, L12, L13, R11, R12, R13, R14 & R15. SEE CHART 1 FOR LOCATION OF ALL DUMMY LOAD CANS.

XIV SEE CHART 2 ON LOGIC 1.1.1 FOR LOCATION OF READ SWITCH CANS AND THE WIRING FROM THESE CANS TO THE READ AMPLIFIERS.

XIII SEE CHART 1 FOR LOCATION OF FIELD SWITCH CANS. EACH OF THE 24 BITS USED IN AN RD DRUM WORD REQUIRES ONE AND A HALF FIELD SWITCH CANS.

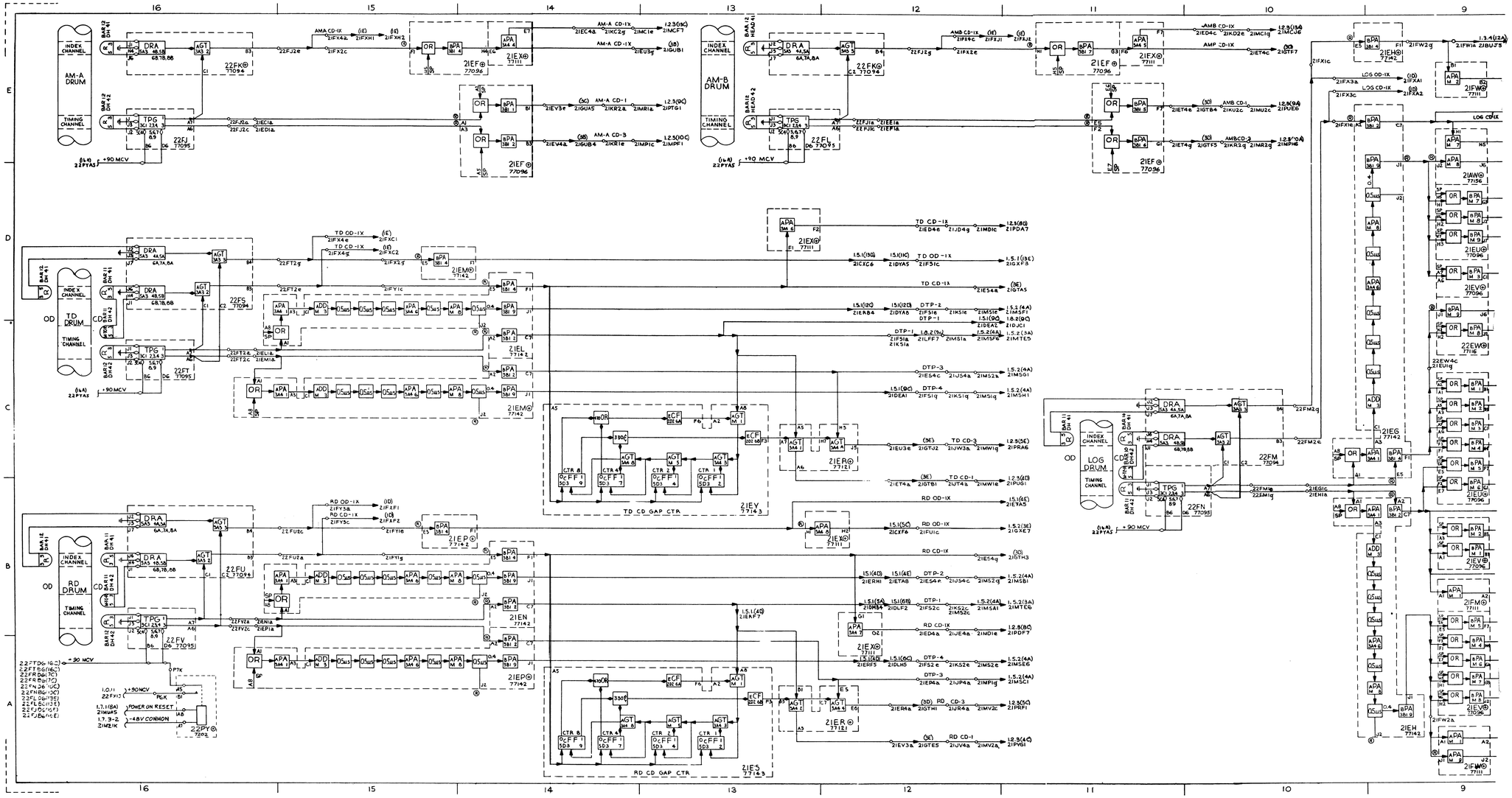
XII DRUM SWITCH CANS ARE NUMBERED IN SEQUENCE - P33 FOR PARITY TO P1 FOR R15. BITS L11, L12, L13, R11, R12, R13, R14 AND R15 USE THE SAME TYPE DRUM SWITCH AS ILLUSTRATED FOR PARITY. ALL OTHER BITS USE THE SAME TYPE DRUM SWITCH AS ILLUSTRATED FOR L15.

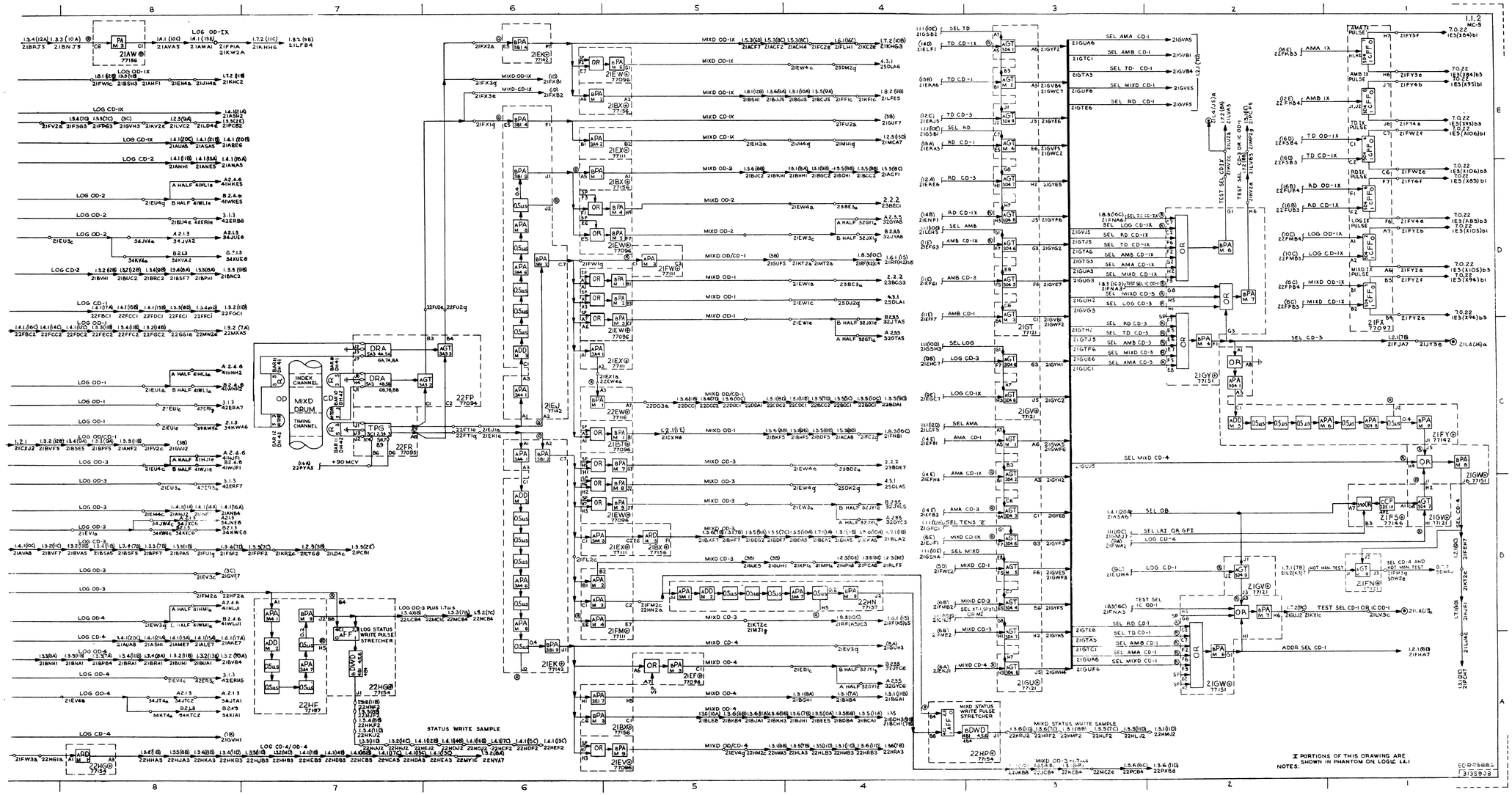
XI SEE CHART 1 FOR WIRING BETWEEN DRUM WRITERS AND DRUM SWITCH CANS.

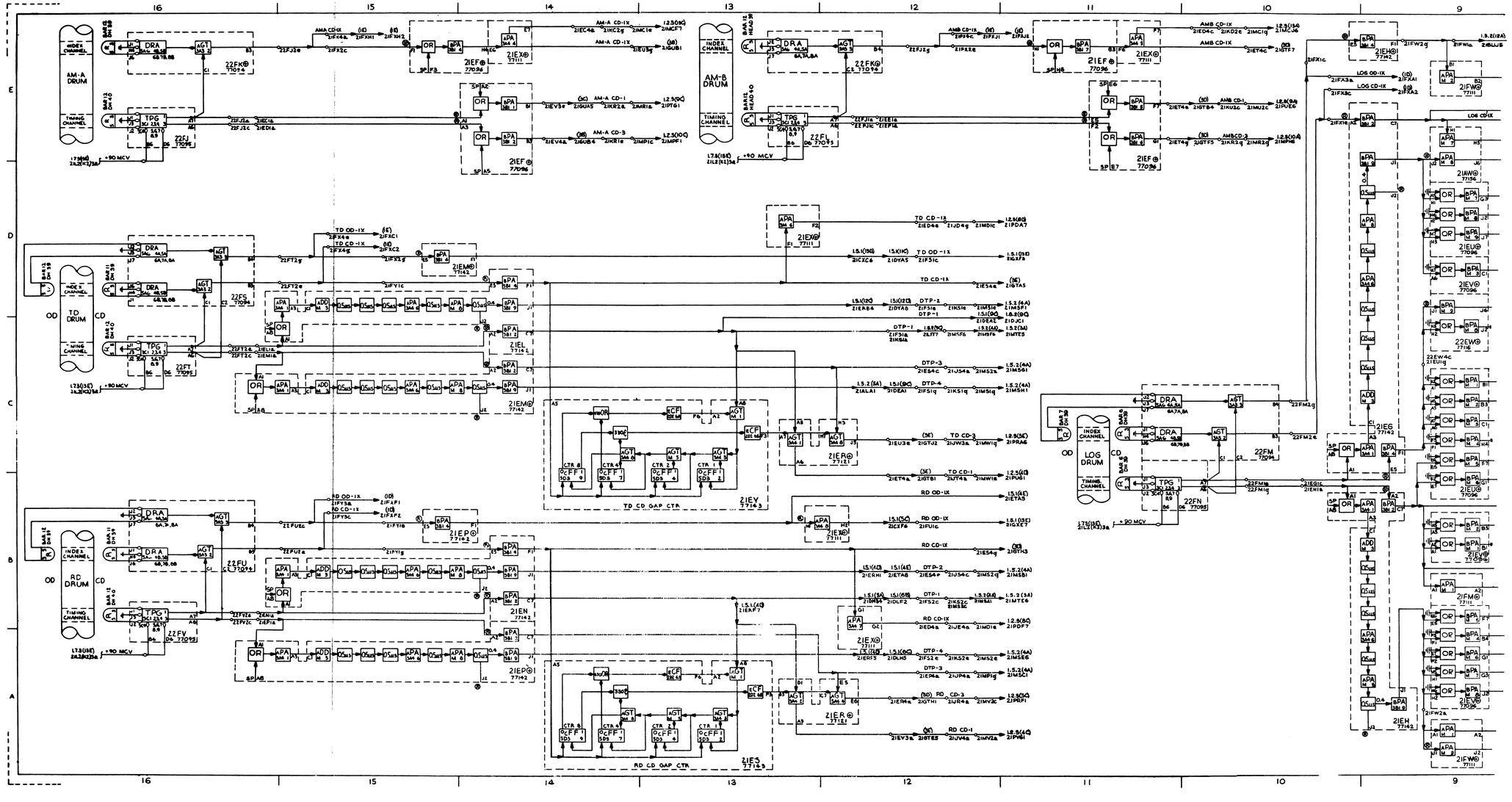
X SHIELDED TWISTED PAIR WIRE IS USED FROM THE EDGE CONNECTOR TO HEAD CENTER TAPS. HEAD CENTER TAP TERMINALS FOR THE SAME FIELD AND SAME BAR ARE JUMPERED TOGETHER. SEE CHART II FOR POINT TO POINT WIRING.

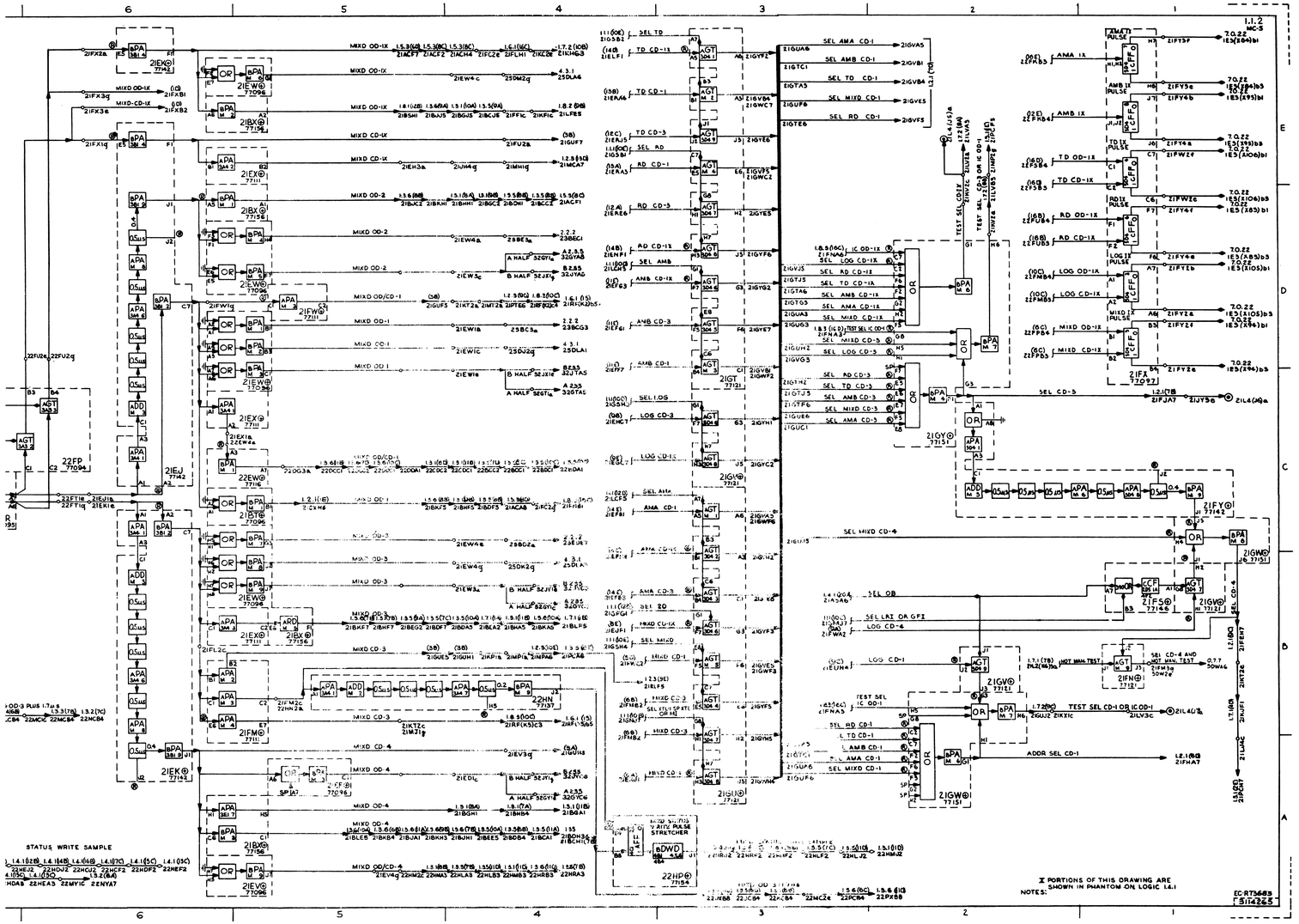
NOTES

EC #45861
3107975

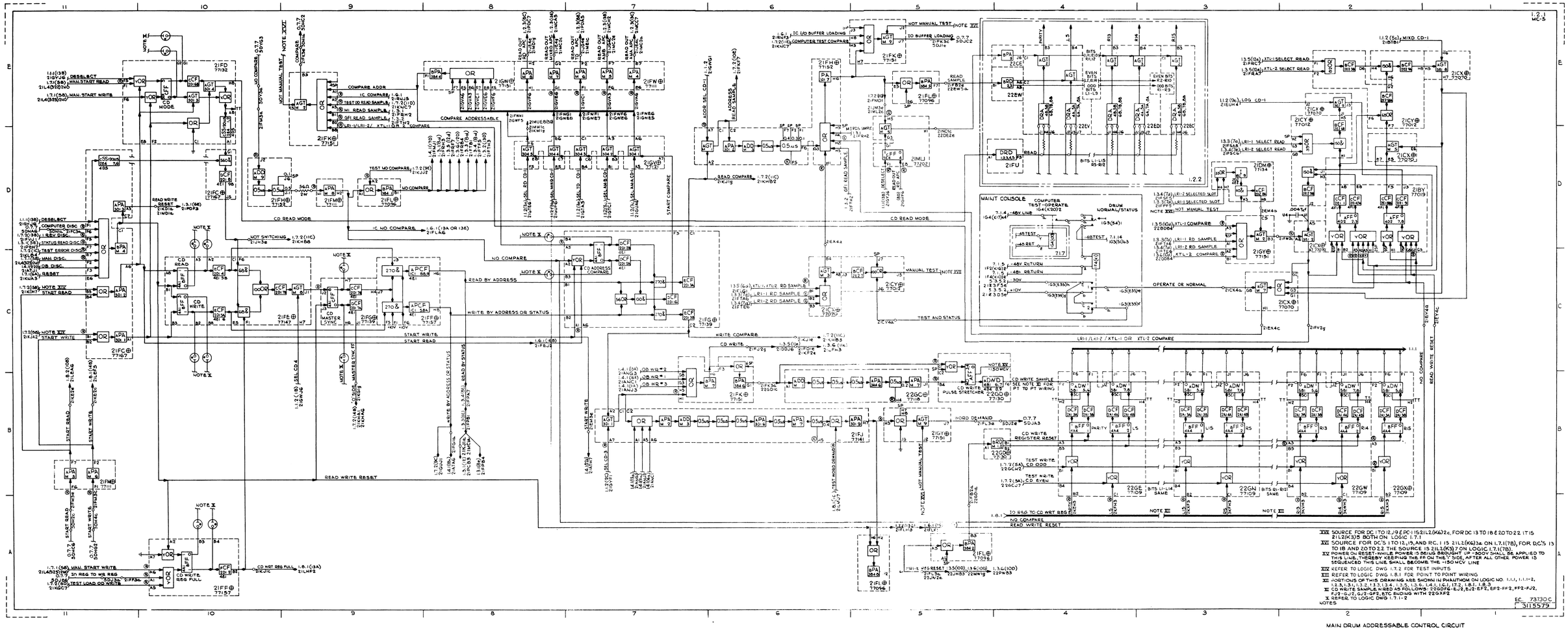

AM-A DRUM
AM-B DRUM
TD DRUM
RD DRUM
LOG DRUM
INDEX CHANNEL
TIMING CHANNEL
OD
DRA
AGT
TPG
OR
APA
ADD
22FK
22FJ
22FS
22FT
22FU
22FV
22FN
22FM
21EF
21EX
21EM
21EL
21EV
21EP
21ES
21ER
21EO
21EG
21EU
21EH
21EW
21EN
22PY
+90 MCV
-48V COMMON
POWER ON RESET
TD CD-1X
TD CD-2X
TD CD-3X
RD CD-1X
RD CD-2X
RD CD-3X
AM-A CD-1X
AM-A CD-2X
AM-A CD-3X
AMB CD-1X
AMB CD-2X
AMB CD-3X
LOG CD-1X
LOG CD-2X
LOG CD-3X
AMP CD-1X
AMP CD-2X
TD CD GAP CTR
RD CD GAP CTR


MAIN DRUM TIMING AND DISTRIBUTION
INDEX CHANNEL
MIXD DRUM
TIMING CHANNEL
OD
STATUS WRITE SAMPLE
MIXD STATUS WRITE SAMPLE
LOG STATUS WRITE PULSE STRETCHER
MIXD STATUS WRITE PULSE STRETCHER
SEL TD
SEL AMA CD-1
SEL AMB CD-1
SEL TD CD-1
SEL MIXD CD-1
SEL RD CD-1
SEL LOG CD-1X
SEL LOG CD-3
SEL MIXD CD-4
SEL OB
SEL LRI OR GFI
SEL CD-4 AND NOT MAN TEST
ADDR SEL CD-1
TEST SEL IC CD-1
TEST SEL CD-1X OR IC CD-1
NOTES:
X PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM ON LOGIC 14.1
EC-R7368.5
3135938
4B


AM-A DRUM
AM-B DRUM
TD DRUM
RD DRUM
LOG DRUM
INDEX CHANNEL
TIMING CHANNEL
DRA
TPG
AGT
OR
APA
ADD
NOR
NCF
OFF
TD CD GAP CTR
RD CD GAP CTR
+90 MCV
AM-A CD-1X
AM-A CD-1
AM-A CD-3
AMB CD-1X
AMB CD-1
TD OD-1X
TD CD-1X
TD CD-1
RD OD-1X
RD CD-1X
RD CD-1
LOG OD-1X
LOG CD-1X
DTP-1
DTP-2
DTP-3
DTP-4
RD CD-3
22FJ 77095
22FK 77094
22FS 77094
22FT 77095
22FU 77095
22FV 77095
22FM 77095
22FN 77095
21EF 77096
21EX 77111
21EM 77142
21EL 77162
21EP 77162
21EN 77142
21EV 77163
21ER 77161
21ES 77163
21EW 77156
21EU 77096
21EG 77142
21FM 77111
21FW 77111
21EH 77142


STATUS WRITE SAMPLE
MAIN DRUM TIMING AND DISTRIBUTION
X PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM ON LOGIC L4.1
NOTES:
EC-RT3685
51L4265

5B



XVI SOURCE FOR DC 1 TO 12, J9 & PC 1 15 21L2(KG)2c, FOR DC 13 TO 18 & 20 TO 22, IT IS 21L2(KG)3 BOTH ON LOGIC 1.7.1

XVII SOURCE FOR DC'S 1 TO 12, 19, AND PC, 1 IS 21L2(KG)3a ON 1.7.1(7B), FOR DC'S 13 TO 18 AND 20 TO 22 THE SOURCE IS 21L2(KG)3 7 ON LOGIC 1.7.1(7B).

XV POWER ON RESET-WHILE POWER IS BEING BROUGHT UP -300V SHALL BE APPLIED TO THIS LINE, THEREBY KEEPING THE FF ON THEY SIDE. AFTER ALL OTHER POWER IS SEQUENCED. THIS LINE SHALL BECOME THE +150MCV LINE

XIV REFER TO LOGIC DWG 1.7.2 FOR TEST INPUTS

XIII REFER TO LOGIC DWG 1.8.1 FOR POINT TO POINT

XII ADDITIONS OF THIS DRAWING ARE SHOWN IN PHAUTHOM ON LOGIC NO. 1.1.1, 1.1.1-2, 1.2.1, 1.3.1, 1.3.2, 1.3.3, 1.3.4, 1.3.5, 1.3.6, 1.4.1, 1.6.1, 1.7.2, 1.8.1, 1.8.3

XI CD WRITE SAMPLE WORD AS FOLLOWS: 22GDF6-EJ2, EJ2-EF2, EF2-FF2, FF2-FJ2, FJ9-GJ2, GJ2-GF2, ETC ENDING WITH 22GXF2

X REFER TO LOGIC DWG 1.7.1-2

NOTES

EC 73730C

31T5579

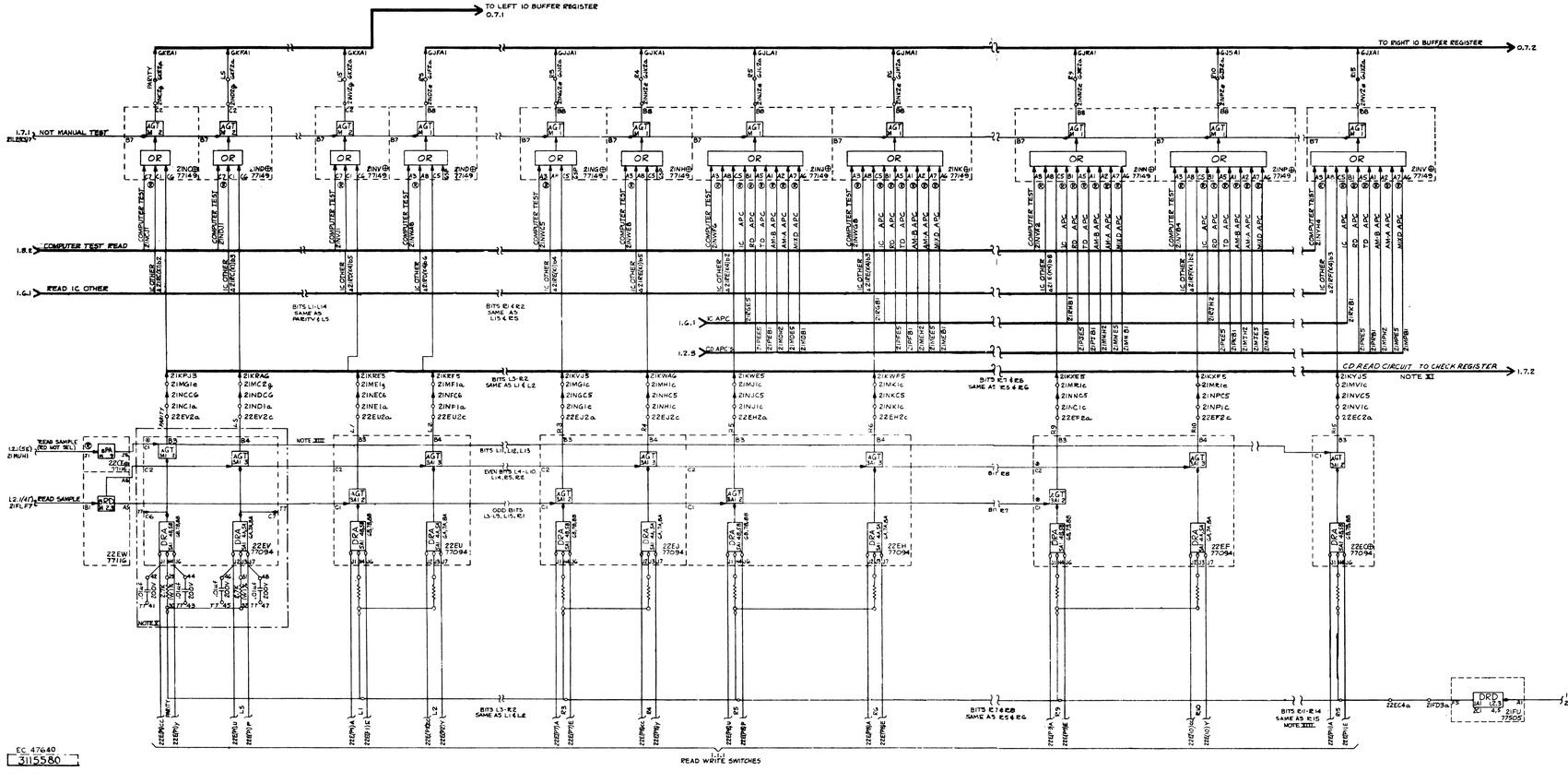


CHART II
(CARD SAMPLE TEST (DO NOT SEL))

BIT	PU PIN
	22EC12c
	22EC22c
E15	22ECC1
E13	22EDC1
E14	22EDC2
E16	22EEC2
E11	22EEC1
L13	22EWC1
L11	22EWC2
L12	22EVC2
P	22EVC1

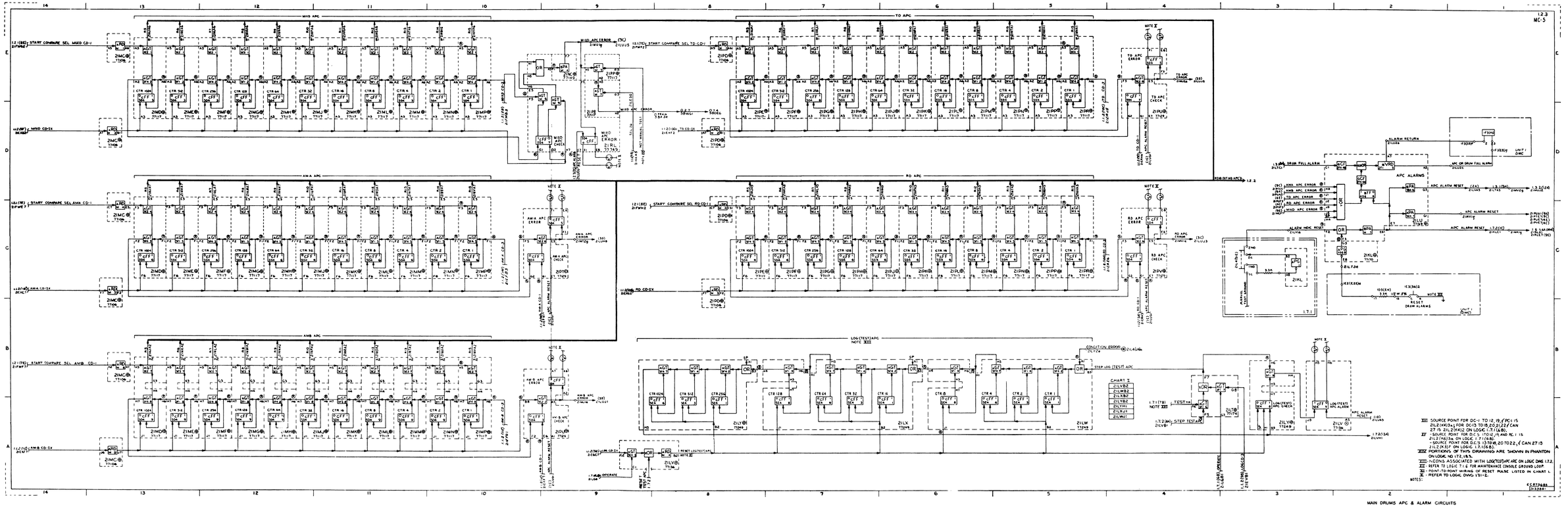
CHART I

BIT	LOGIC 1.2.2 D R A READ GATE		EDGE CONNECTOR	EDGE CONNECTOR	LOGIC 1.2.2 CD READ BUS	EDGE CONNECTOR	LOGIC 1.7.2 CHECK REGISTER
P	22EVB3	22EV2a	2INC1a		2INCC6	2IMG1e	2IKPJ3
L5	Y84	V2C	B1a		DC6	C5g	RAG
L1	U83	U2a	E1a		EC6	E1g	RES
L2	U84	U2c	F1a		FC6	F1a	RFS
L3	T83	T2a	G1a		GC6	G1a	RJS
L4	T84	T2c	H1a		HC6	H1a	SAG
L5	S83	S2a	J1a		JC6	J1a	SES
L6	S84	S2c	K1a		KC6	K1a	SFS
L7	R83	R2a	L1a		LC6	L1a	SJS
L8	K84	R2c	M1a		MC6	M1e	TAG
L9	P83	P2a	N1a		NC6	N1g	TES
L10	P84	P2c	P1a		PC6	P1e	TFS
L11	N83	N2a	R1a		RC6	R2c	TJS
L12	N84	N2c	S1a		SC6	R2a	UAG
L13	M83	M2a	T1a		TC6	T2c	UES
L14	M84	M2c	U1a		UC6	U2e	UFS
L15	L83	L2a	V1a		VC6	V1a	UJS
R5	L84	L2c	D1a		DC5	F1e	VAG
R1	K83	K2a	E1a		EC5	F1g	VES
R2	K84	K2c	F1a		FC5	F1c	VFS
R3	J83	J2a	G1a		GC5	G1c	VJS
R4	J84	J2c	H1a		HC5	H1c	WAG
R5	H83	H2a	J1a		JC5	J1c	WES
R6	H84	H2c	K1a		KC5	K1c	WFS
R7	G83	G2a	L1a		LC5	L1c	WJS
R8	G84	G2c	M1a		MC5	M1g	XAG
R9	F83	F2a	N1a		NC5	R1c	XES
R10	Y86	F2c	P1a		PC5	R1e	XFS
R11	E83	E2a	R1a		RC5	R1g	XJS
R12	E84	E2c	S1a		SC5	R2e	YAG
R13	D83	D2a	T1a		TC5	T2e	YES
R14	Y85	D2E	U1a		UC5	U2g	YFS
R15	22EC83	22EC2a	2INV1c		2INVC5	2IMV1c	2IKPJ5

III REFER TO CHART II FOR POINT TO POINT WIRING.
XII PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM ON LOGIC NO. 1.1.1, 1.1.1-2, 1.2.1, 1.3.1, 1.3.2, 1.3.3, 1.3.4, 1.3.5, 1.3.6, 1.6.1, 1.7.2, 1.8.2, 1.8.3.
XI REFER TO CHART I FOR WIRING SEQUENCE OF DRA OUTPUTS. COMPONENTS & TEST TERMINALS SHOWN IN PU 22EV ARE THE SAME FOR ALL DRA'S.

NOTES:

MAIN DRUMS CD READ CIRCUITS AND READ BUS


MIXD APC
TD APC
AMA APC
RD APC
AMB APC
LOG(TEST)APC
NOTE XIII
APC ALARMS
CHART I
21LV82
21LW82
21LX82
21LY82
21LZ11
21LW21
21LW22
NOTES:
XII SOURCE POINT FOR DC-1 TO 12.19,(PC-15 21LZ(4X)3x) FOR DC-13, TO 18,20,21,22,(CAN 27-15 21L27412) ON LOGIC 1.7.1 (G8).
XIV -SOURCE POINT FOR D.C.S. 17 TO 12.19 AND PC-1 15 21LZ(4X)3x ON LOGIC 1.7.1 (A8).
21LZ(4X)2 ON LOGIC 1.7.1 (A8) AND 18,20 TO 22,(CAN 27-15 21LZ(4X)1 ON LOGIC 1.7.1 (A8).
XIII PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM ON LOGIC NO 1.7.2, (8).
XIII -NODES ASSOCIATED WITH LOG(TEST)APC ARE ON LOGIC DWG 1.7.2.
III REFER TO LOGIC 7.1.2 FOR MAINTENANCE CONSOLE GROUND LOOP.
X - POINT-TO-POINT WIRING OF RESET PHASE LISTED IN CHART I.
REFER TO LOGIC DWG 1.3.1-2.
MAIN DRUMS APC & ALARM CIRCUITS

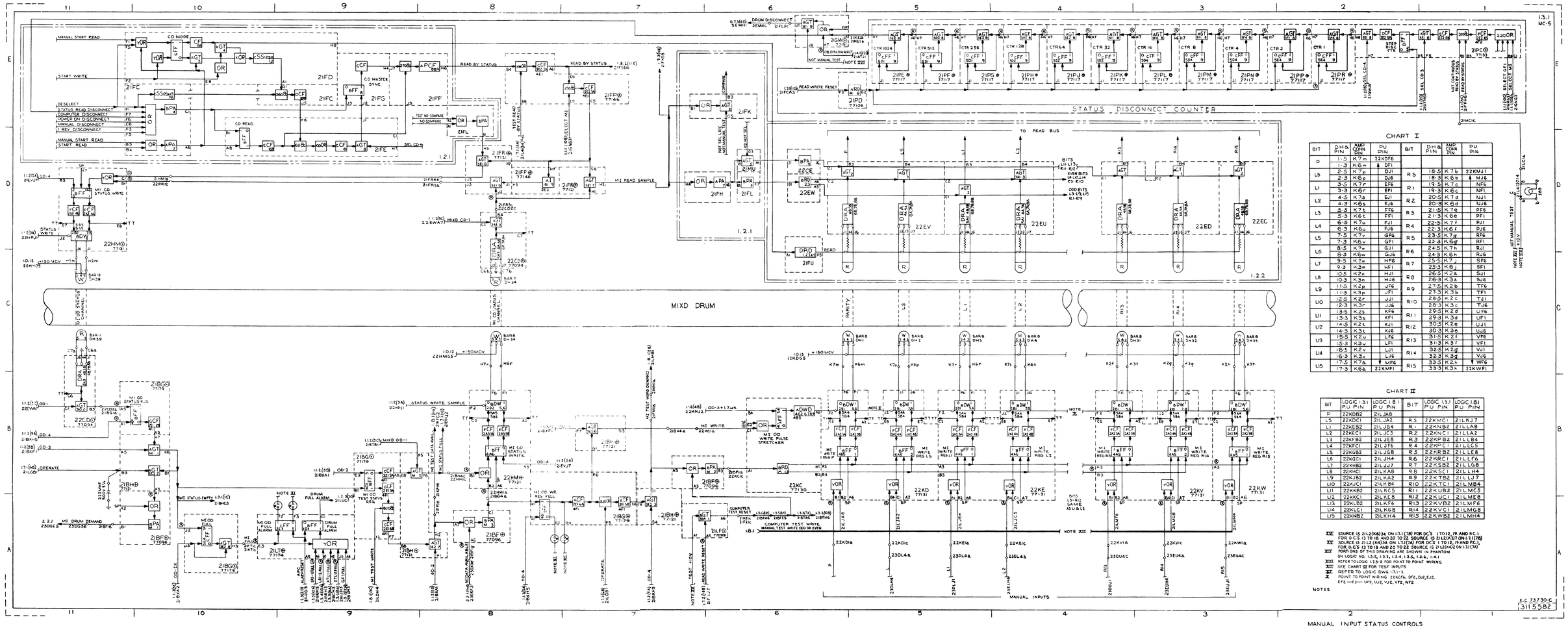


CHART I

BIT	DH& PIN	AUD CONN PIN	PU PIN	BIT	DH& PIN	AUD CONN PIN	PU PIN
P	1-5	K7m	22KDF6				
	1-3	K6m	DF1				
L5	2-5	K7p	DJ1	R5	18-5	K7b	22KMJ1
	2-3	K6p	DJ6		18-3	K6b	MJ6
L1	3-5	K7r	EF6	R1	19-5	K7c	NF6
	3-3	K6r	EF1		19-3	K6c	NF1
L2	4-5	K7s	EJ1	R2	20-5	K7d	NJ1
	4-3	K6s	EJ6		20-3	K6d	NJ6
L3	5-5	K7t	FF6	R3	21-5	K7e	PF6
	5-3	K6t	FF1		21-3	K6e	PF1
L4	6-5	K7u	FJ1	R4	22-5	K7f	PJ1
	6-3	K6u	FJ6		22-3	K6f	PJ6
L5	7-5	K7v	GF6	R5	23-5	K7g	RF6
	7-3	K6v	GF1		23-3	K6g	RF1
L6	8-5	K7w	GJ1	R6	24-5	K7h	RJ1
	8-3	K6w	GJ6		24-3	K6h	RJ6
L7	9-5	K3m	HF6	R7	25-5	K7j	SF6
	9-3	K3m	HF1		25-3	K6j	SF1
L8	10-5	K2n	HJ1	R8	26-5	K2a	SJ1
	10-3	K3n	HJ6		26-3	K3a	SJ6
L9	11-5	K2p	JF6	R9	27-5	K2b	TF6
	11-3	K3p	JF1		27-3	K3b	TF1
L10	12-5	K2r	JJ1	R10	28-5	K2c	TJ1
	12-3	K3r	JJ6		28-3	K3c	TJ6
L11	13-5	K2s	KF6	R11	29-5	K2d	UF6
	13-3	K3s	KF1		29-3	K3d	UF1
L12	14-5	K2t	KJ1	R12	30-5	K2e	UJ1
	14-3	K3t	KJ6		30-3	K3e	UJ6
L13	15-5	K2u	LF6	R13	31-5	K2f	VF6
	15-3	K3u	LF1		31-3	K3f	VF1
L14	16-5	K2v	LJ1	R14	32-5	K2g	VJ1
	16-3	K3v	LJ6		32-3	K3g	VJ6
L15	17-5	K2a	WF6	R15	33-5	K2h	WF6
	17-3	K6a	22KWF1		33-3	K3h	22KWF1

CHART II

BIT	LOGIC 1.3.1 PU PIN	LOGIC 1.8.1 PU PIN	BIT	LOGIC 1.3.1 PU PIN	LOGIC 1.8.1 PU PIN
P	22KDB2	21LJA5			
L5	22KDC1	21LJA2	R5	22KMC1	21LKJ7
L1	22KEB2	21LJB4	R1	22KNB2	21LLA8
L2	22KEC1	21LJC3	R2	22KNC1	21LLA2
L3	22KFB2	21LJE8	R3	22KPB2	21LLB4
L4	22KFC1	21LJF6	R4	22KPC1	21LLC5
L5	22KGB2	21LJG8	R5	22KRB2	21LLE8
L6	22KGC1	21LJH6	R6	22KRC1	21LLF6
L7	22KHB2	21LJJ7	R7	22KSB2	21LLG8
L8	22KHC1	21LKA8	R8	22KSC1	21LLH4
L9	22KJB2	21LKA2	R9	22KTB2	21LLJ7
L10	22KJC1	21LKB4	R10	22KTC1	21LMB4
L11	22KKB2	21LKC5	R11	22KUB2	21LMC5
L12	22KKC1	21LKE8	R12	22KUC1	21LME8
L13	22KLB2	21LKF6	R13	22KVB2	21LMF6
L14	22KLC1	21LKG8	R14	22KVC1	21LMG8
L15	22KMB2	21LKH4	R15	22KWB2	21LMH4

XII SOURCE IS 21L2(KA3)A ON 1.3.1(7B) FOR DCS 1TO12, 19 AND RC-1. FOR D.C.S 13 TO 18 AND 20 TO 22 SOURCE IS 21L2(K3)T ON 1.3.1(7B)
XI SOURCE IS 21L2(KA1)A ON 1.3.1(7A) FOR DCS 1 TO 12, 19 AND RC-1. FOR D.C.S 13 TO 18 AND 20 TO 22 SOURCE IS 21L2(K4)Z ON 1.3.1(7A)
XIII PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM
ON LOGIC NO. 1.3.5, 1.3.3, 1.3.4, 1.3.8, 1.3.6, 1.4.1
XIII REFER TO LOGIC DWG 1.7.1-1
SEE CHART II FOR TEST INPUTS
REFER TO LOGIC DWG 1.7.1-1
POINT TO POINT WIRING 22KDF6, DF2, DJ2, EJ2, EF2 —|— UF2, UJ2, VJ2, VF2, WF2

NOTES

E.C. 73730-C
13115582

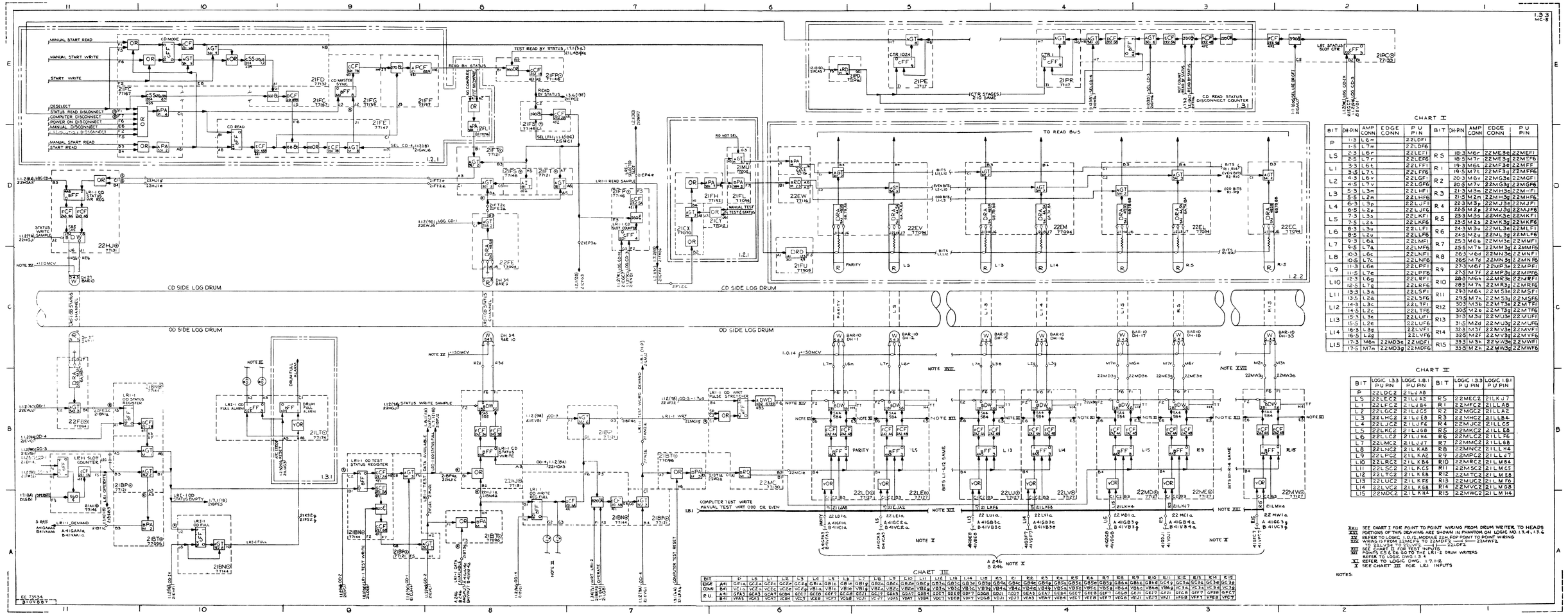


CHART I

BIT	DH-PIN	AMP CONN	EDGE CONN	P U PIN	BIT	DH-PIN	AMP CONN	EDGE CONN	P U PIN
P	1-3	L6m		22LDF1					
	1-5	L7m		22LDF6					
LS	2-3	L6r		22LEF1	R5	18-3	M6r	22ME3e	22MEF1
	2-5	L7r		22LEF6		18-5	M7r	22ME3d	22MEF6
L1	3-3	L6t		22LFF1	R1	19-3	M6t	22MF3e	22MFF
	3-5	L7t		22LFF6		19-5	M7t	22MF3d	22MFF6
L2	4-3	L6v		22LGF1	R2	20-3	M6v	22MG3e	22MGF1
	4-5	L7v		22LGF6		20-5	M7v	22MG3d	22MGF6
L3	5-3	L3m		22LHF1	R3	21-3	M3m	22MH3e	22M-F1
	5-5	L2m		22LHF6		21-5	M2m	22MH3d	22MHF6
L4	6-3	L3p		22LJF1	R4	22-3	M3p	22MJ3e	22MJF1
	6-5	L2p		22LJF6		22-5	M2p	22MJ3d	22MJF6
L5	7-3	L3s		22LKF1	R5	23-3	M3s	22MK3e	22MKF1
	7-5	L2s		22LKF6		23-5	M2s	22MK3d	22MKF6
L6	8-3	L3v		22LLF1	R6	24-3	M3v	22ML3e	22MLF1
	8-5	L2v		22LLF6		24-5	M2v	22ML3d	22MLF6
L7	9-3	L6a		22LMF1	R7	25-3	M6a	22MM3e	22MMF1
	9-5	L7a		22LMF6		25-5	M7a	22MM3d	22MMF6
L8	10-3	L6c		22LNF1	R8	26-3	M6d	22MN3e	22MNF1
	10-5	L7c		22LNF6		26-5	M7d	22MN3d	22MNF6
L9	11-3	L6e		22LPF1	R9	27-3	M6f	22MP3e	22MPF1
	11-5	L7e		22LPF6		27-5	M7f	22MP3d	22MPF6
L10	12-3	L6g		22LRF1	R10	28-3	M6h	22MR3e	22MRF1
	12-5	L7g		22LRF6		28-5	M7h	22MR3d	22MRF6
L11	13-3	L3a		22LSF1	R11	29-3	M6k	22M53e	22MSF1
	13-5	L2a		22LSF6		29-5	M7k	22M53d	22MSF6
L12	14-3	L3c		22LTF1	R12	30-3	M3k	22MT3e	22MTF1
	14-5	L2c		22LTF6		30-5	M2k	22MT3d	22MTF6
L13	15-3	L3e		22LUF1	R13	31-3	M3d	22MU3e	22MUF1
	15-5	L2e		22LUF6		31-5	M2d	22MU3d	22MUF6
L14	16-3	L3g		22LVF1	R14	32-3	M3f	22MV3e	22MVF1
	16-5	L2g		22LVF6		32-5	M2f	22MV3d	22MVF6
L15	17-3	M6n	22MD3e	22MDF1	R15	33-3	M3h	22MW3e	22MWF1
	17-5	M7m	22MD3g	22MDF6		33-5	M2h	22MW3d	22MWF6

CHART II

BIT	LOGIC 1.33 P U PIN	LOGIC 1.81 P U PIN	BIT	LOGIC 1.33 P U PIN	LOGIC 1.81 P U PIN
P	22LDC2	21LJA8			
LS	22LEC2	21LJA2	R5	22MEC2	21LKJ7
L1	22LFC2	21LJB4	R1	22MFC2	21LLA8
L2	22LGC2	21LJC5	R2	22MGC2	21LLA2
L3	22LHC2	21LJE8	R3	22MHC2	21LLB4
L4	22LJC2	21LJF6	R4	22MJC2	21LLC5
L5	22LKC2	21LJG8	R5	22MKC2	21LLE8
L6	22LLC2	21LJH4	R6	22MLC2	21LLF6
L7	22LMC2	21LJJ7	R7	22MMC2	21LLG8
L8	22LNC2	21LKA8	R8	22MNC2	21LLH4
L9	22LPC2	21LKA2	R9	22MPC2	21LLJ7
L10	22LRC2	21LKB4	R10	22MRC2	21LLM8
L11	22LSC2	21LKC5	R11	22MSC2	21LMC5
L12	22LTC2	21LKE8	R12	22MTC2	21LME8
L13	22LUC2	21LKF6	R13	22MUC2	21LMF6
L14	22LVC2	21LKG8	R14	22MVC2	21LMG8
L15	22MDC2	21LKH4	R15	22MWC2	21LMH4

CHART III

BIT	P	L5	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15
EDGE CONN	A41	GF1a	GC2a	GC2c	GC2e	GC2g	GB1a	GB1c	GB1e	GB1g	GB2a	GB2c	GB2e	GB2g	GB1a	GB1c	GB3e	GB3g	GB4a	GB4c	GB4e	GB4g	GB5a	GB5c	GB5e	GB5g	GB6a	GB6c	GB6e	GC4g	GC3a	GC3c	GC3e	GC3g
CONN	B41	VC1a	VC2a	VC2c	VC2e	VC2g	VB1a	VB1c	VB1e	VB1g	VB2a	VB2c	VB2e	VB2g	VB3a	VB3c	VB3e	VB3g	VB4a	VB4c	VB4e	VB4g	VB5a	VB5c	VB5e	VB5g	VB6a	VB6c	VB6e	VC4g	VC3a	VC3c	VC3e	VC3g
P.U.	A41	VFA3	GCA3	GCA1	GCA7	GCB4	GCC1	GCE8	GCF1	GCG8	GCJ1	GCL1	GCM1	GCP1	GDA1	GDC1	GDE8	GDF1	GDG8	GDJ1	GDL1	GDM1	GEA1	GEA7	GEB4	GEC1	GEE8	GEF1	VJE1	GEG8	GEJ1	GEL1	GEM1	GEP1
	B41	VFA5	VGA3	VCA1	VCB4	VCC1	VCE8	VCF1	VCG8	VCJ1	VCL1	VCM1	VCP1	VDA3	VDA1	VDB4	VDC1	VDE8	VDF1	VDG8	VDJ1	VDL1	VEA3	VEA7	VEB4	VEC1	VEE8	VEF1	VEG8	VEJ1	VEL1	VEM1	VEP1	VFC1

XXI SEE CHART I FOR POINT TO POINT WIRING FROM DRUM WRITER TO HEADS
XXII PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM ON LOGIC NO. 1.3.4, 1.3.6
XXIII REFER TO LOGIC 1.0.12, MODULE 22H, FOP POINT TO POINT WIRING
XXIV WIRING IS FROM 22MCF3 TO 22MDF2 ——— 22MWF2.
TO 22LV3B TO 22LVF2 ——— 22LDF2.
XXV SEE CHART II FOR TEST INPUTS.
POINTS E5 & E6 GO TO THE LR1-2 DRUM WRITERS
XXVI REFER TO LOGIC DWG. 1.3.4
X SEE CHART III FOR LR1 INPUTS

NOTES:

LONG RANGE RADAR INPUT NO 1-OPERATE CIRCUITRY

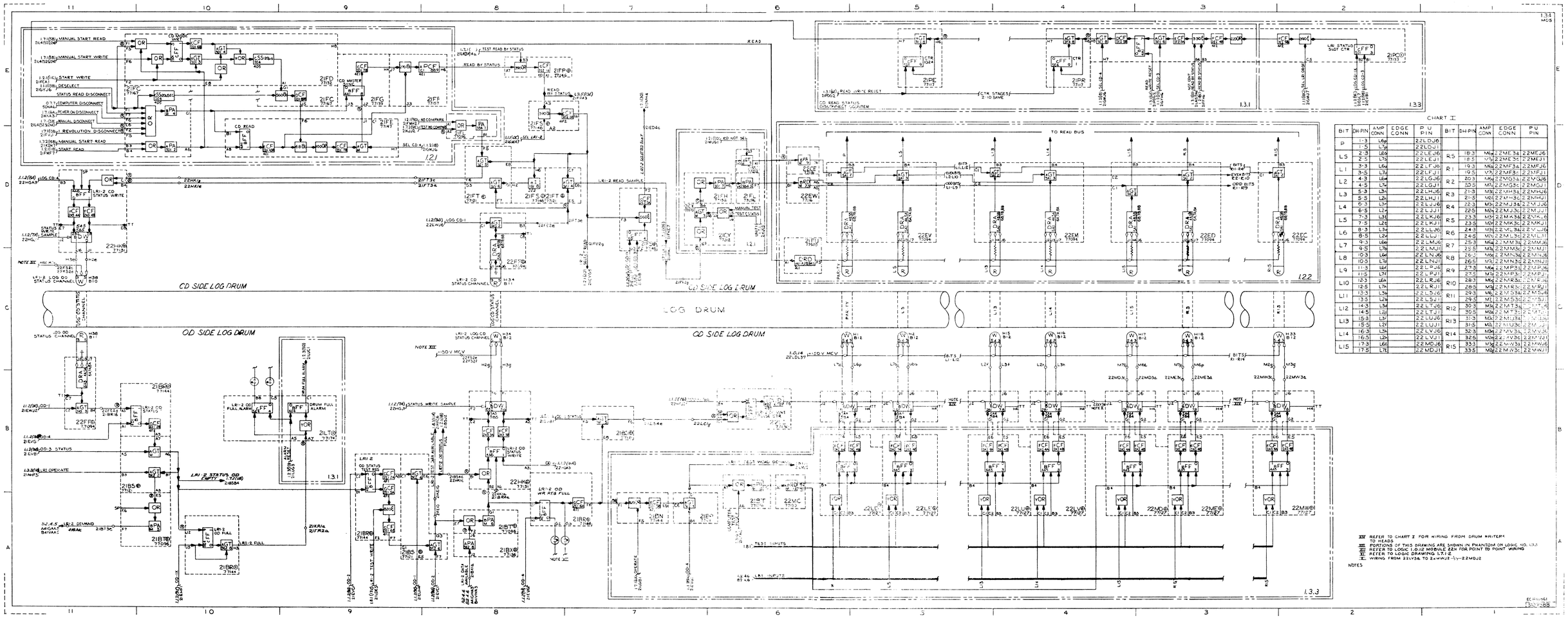
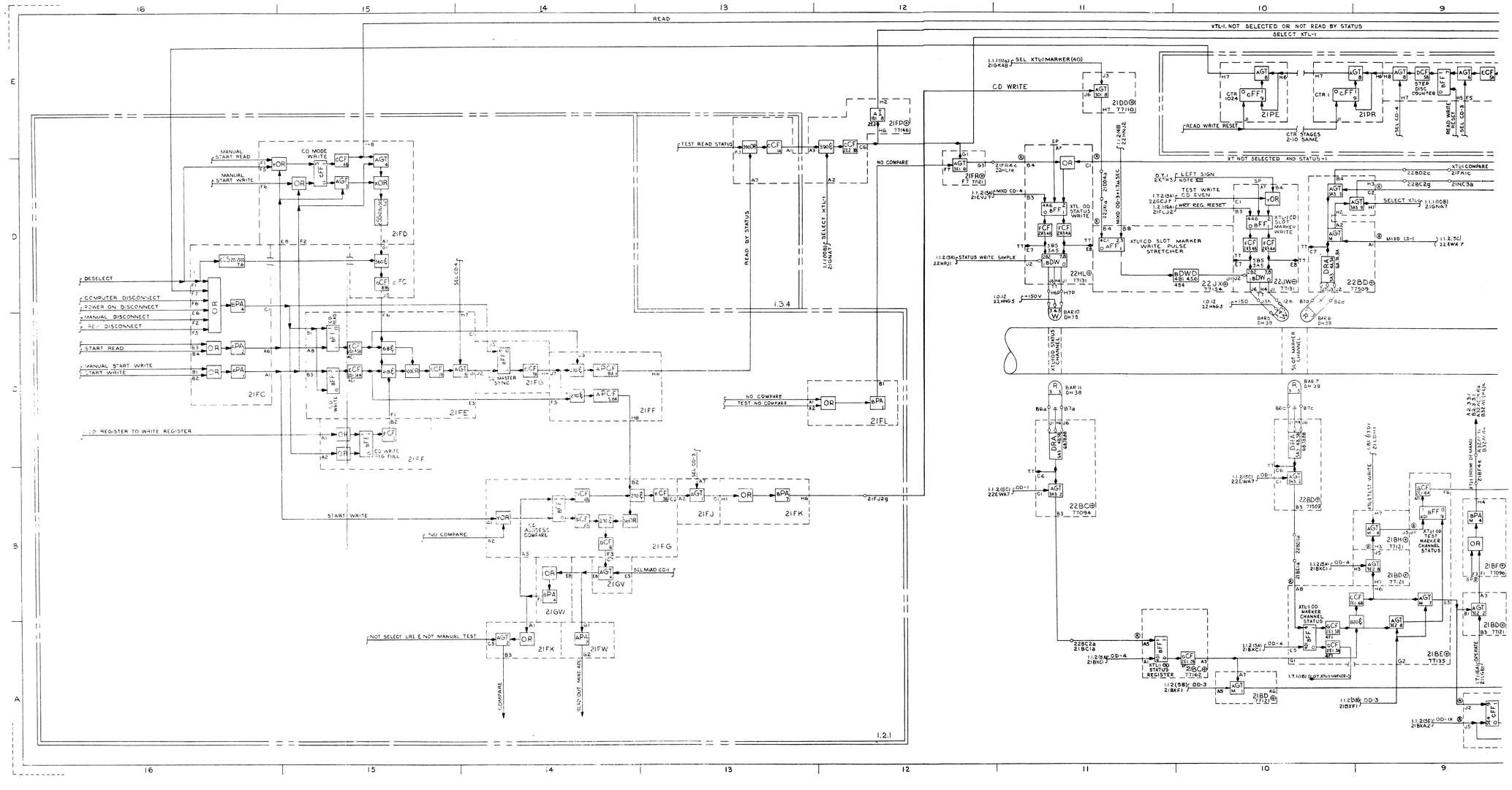


CHART I

BIT	DH-PIN	AMP CONN	EDGE CONN	PU PIN	BIT	DH-PIN	AMP CONN	EDGE CONN	PU PIN
P	1-3	L6p		22LDJ6					
	1-5	L7p		22LDJ1					
LS	2-3	L6s		22LEJ6	R5	18-3	M6s	22ME36	22MEJ6
	2-5	L7s		22LEJ1		18-5	M7s	22ME35	22MEJ1
L1	3-3	L6t		22LFJ6	R1	19-3	M6t	22MF36	22MFJ6
	3-5	L7t		22LFJ1		19-5	M7t	22MF35	22MFJ1
L2	4-3	L6u		22LGJ6	R2	20-3	M6u	22MG36	22MGJ6
	4-5	L7u		22LGJ1		20-5	M7u	22MG35	22MGJ1
L3	5-3	L3n		22LHJ6	R3	21-3	M3n	22MH36	22MHJ6
	5-5	L2n		22LHJ1		21-5	M2n	22MH35	22MHJ1
L4	6-3	L3m		22LJJ6	R4	22-3	M3m	22MJ36	22MJJ6
	6-5	L2m		22LJJ1		22-5	M2m	22MJ35	22MJJ1
L5	7-3	L3l		22LKJ6	R5	23-3	M3l	22MK36	22MKJ6
	7-5	L2l		22LKJ1		23-5	M2l	22MK35	22MKJ1
L6	8-3	L3k		22LLJ6	R6	24-3	M3k	22ML36	22MLJ6
	8-5	L2k		22LLJ1		24-5	M2k	22ML35	22MLJ1
L7	9-3	L6d		22LMJ6	R7	25-3	M6d	22MM36	22MMJ6
	9-5	L7d		22LMJ1		25-5	M7d	22MM35	22MMJ1
L8	10-3	L6e		22LNJ6	R8	26-3	M6e	22MN36	22MNJ6
	10-5	L7e		22LNJ1		26-5	M7e	22MN35	22MNJ1
L9	11-3	L6f		22LPJ6	R9	27-3	M6f	22MP36	22MPJ6
	11-5	L7f		22LPJ1		27-5	M7f	22MP35	22MPJ1
L10	12-3	L6h		22LRJ6	R10	28-3	M6g	22MR36	22MRJ6
	12-5	L7h		22LRJ1		28-5	M7g	22MR35	22MRJ1
L11	13-3	L3w		22LSJ6	R11	29-3	M6j	22MS36	22MSJ6
	13-5	L2w		22LSJ1		29-5	M5j	22MS35	22MSJ1
L12	14-3	L3d		22LTJ6	R12	30-3	M6k	22MT36	22MTJ6
	14-5	L2d		22LTJ1		30-5	M5k	22MT35	22MTJ1
L13	15-3	L3f		22LUJ6	R13	31-3	M6l	22MU36	22MUJ6
	15-5	L2f		22LUJ1		31-5	M5l	22MU35	22MUJ1
L14	16-3	L3h		22LVJ6	R14	32-3	M6m	22MV36	22MVJ6
	16-5	L2h		22LVJ1		32-5	M5m	22MV35	22MVJ1
L15	17-3	L6t		22MDJ6	R15	33-3	M3d	22MW36	22MWJ6
	17-5	L7t		22MDJ1		33-5	M2d	22MW35	22MWJ1

LONG RANGE RADAR INPUT NO 2 OPERATE CIRCUITRY


READ
XTL-1 NOT SELECTED OR NOT READ BY STATUS
SELECT XTL-1
CD WRITE
XT NOT SELECTED AND STATUS=1
MANUAL START READ
MANUAL START WRITE
CD MODE WRITE
DESELECT
COMPUTER DISCONNECT
POWER ON DISCONNECT
MANUAL DISCONNECT
REV DISCONNECT
START READ
MANUAL START WRITE
START WRITE
21FC
21FD
21FE
21FF
21FG
21FJ
21FK
21FL
21FW
21GV
21GW
21IPE
21IPR
21DD
21FP
21FR
21HL
22JX
22JW
22BD
22BC
21BH
21BD
21BF
21BE
21BC
21BA
21FU2g
TEST READ STATUS
NO COMPARE
TEST NO COMPARE
READ BY STATUS
SELECT XTL-1
CD REGISTER TO WRITE REGISTER
CD WRITE REG FULL
CD ADDRESS COMPARE
NOT SELECT LRI & NOT MANUAL TEST
SEL MIXD CD-4
SEL CD-3
SEL CD-4
MASTER SYNC
COMPARE
READ OUT MAST. ADR.
SEL XTL-1 MARKER (40)
XTL CD STATUS CHANNEL
XTL-1 CD SLOT MARKER CHANNEL
XTL-1 CD SLOT MARKER WRITE PULSE STRETCHER
TEST WRITE CD EVEN
WET REG RESET
STATUS WRITE SAMPLE
MIXED CD-1
MIXED CD-4
LEFT SIGN
XTL-1 COMPARE
SELECT XTL-1
XTL-1 CD SLOT MARKER WRITE
XTL-1 CD MARKER CHANNEL STATUS
XTL-1 TEST WRITE
XTL-1 CD TEST MARKER CHANNEL STATUS
XTL-1 CD STATUS REGISTER
READ WRITE RESET
CTR STAGES 2-10 SAME
STEP DISC COUNTER
1.2.1
1.3.4

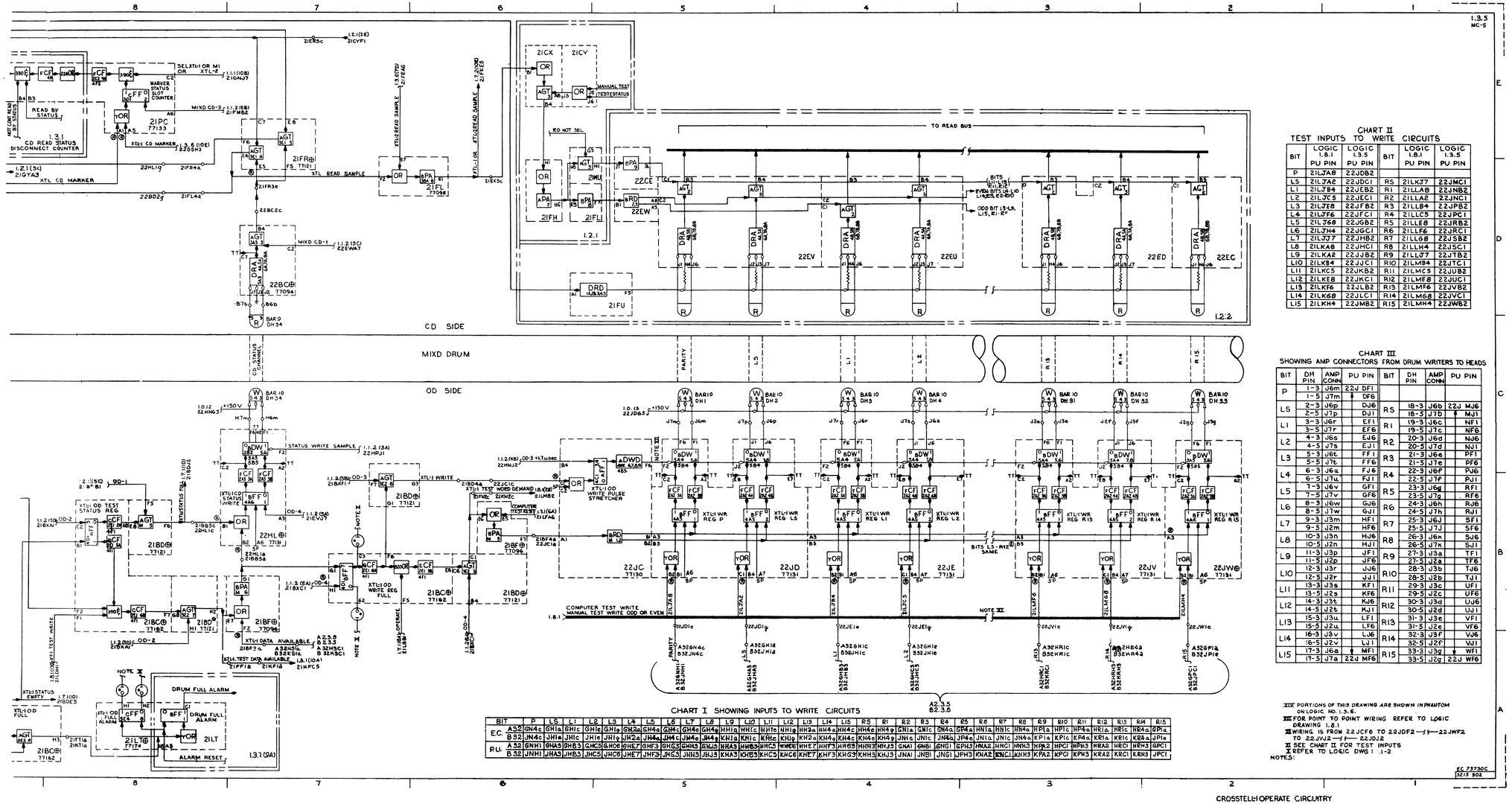


CHART I SHOWING INPUTS TO WRITE CIRCUITS

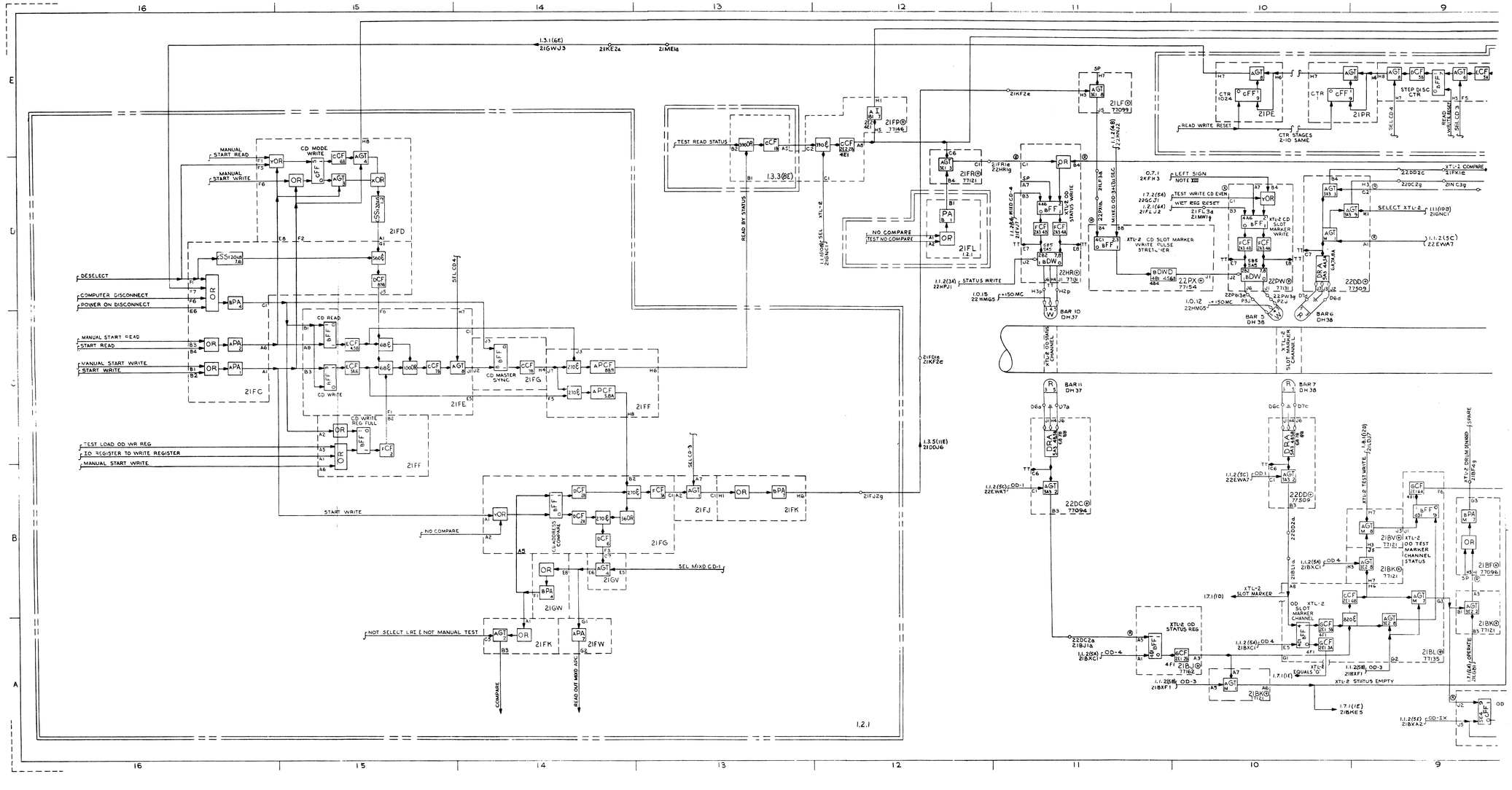
BIT	P	L5	L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	R5	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15
E.C.	A32	GN4c	GH1a	GH1c	GH1e	GH1g	GH2a	GH4a	GH4c	GH4e	GH4g	HH1a	HH1c	HH1e	HH1g	HH2a	HH4a	HH4c	HH4e	HH4g	GN1a	GN1c	GN4a	GP4a	HN1a	HN1c	HN4a	HP1a	HP1c	KP4a	KR1a	KR1c	KR4a	GP1a
	B32	JN4c	JH1a	JH1c	JH1e	JH1g	JH2a	JH4a	JH4c	JH4e	JH4g	KH1a	KH1c	KR1c	KH1g	KH2a	KH4a	KH4c	KH4e	KH4g	JN1a	JN1c	JN4a	JP4a	JN1a	JN1c	JN4a	KP1a	KP1c	KP4a	KR1a	KR1c	KR4a	JP1a
P.U.	A32	GN41	GH45	JH83	GJC5	GJC6	GJE7	GJF3	GJG5	GJH3	GJJ5	KHA3	KH85	KHC5	KHC6	KHE7	KHF3	KHG5	KHH3	KHJ5	GNA1	GNB1	GNG1	GPH3	KNA2	KNC1	KNH3	KPA2	KPC1	KPH3	KRA2	KRC1	KRH3	GPC1
	B32	JN41	JH45	JH83	JHC5	JHC6	JHE7	JHF3	JHG5	JHH3	JHJ5	KHA5	KH85	KHC5	KHC6	KHE7	KHF3	KHG5	KHH3	KHJ5	JNA1	JNB1	JNG1	JPH3	KNA2	KNC1	KNH3	KPA2	KPC1	KPH3	KRA2	KRC1	KRH3	JPC1

CHART II
TEST INPUTS TO WRITE CIRCUITS

BIT	LOGIC 1.8.1 PU PIN	LOGIC 1.3.5 PU PIN	BIT	LOGIC 1.8.1 PU PIN	LOGIC 1.3.5 PU PIN
P	21LJA8	22JDB2			
L5	21LJA2	22JDC1	R5	21LKJ7	22JMC1
L1	21LJB4	22JEB2	R1	21LLA8	22JNB2
L2	21LJC5	22JEC1	R2	21LLA2	22JNC1
L3	21LJE8	22JFB2	R3	21LLB4	22JPB2
L4	21LJF6	22JFC1	R4	21LLC5	22JPC1
L5	21LJ68	22JGB2	R5	21LLE8	22JRB2
L6	21LJH4	22JGC1	R6	21LLF6	22JRC1
L7	21LJJ7	22JHB2	R7	21LLG8	22JSB2
L8	21LKA6	22JHC1	R8	21LLH4	22JSC1
L9	21LKA2	22JJB2	R9	21LLJ7	22JTB2
L10	21LKB4	22JJC1	R10	21LMB4	22JTC1
L11	21LKC5	22JKB2	R11	21LMC5	22JUB2
L12	21LKE8	22JKC1	R12	21LME8	22JUC1
L13	21LKF6	22JLB2	R13	21LMF6	22JVB2
L14	21LKG8	22JLC1	R14	21LMG8	22JVC1
L15	21LKH4	22JMB2	R15	21LMH4	22JWB2

CHART III
SHOWING AMP CONNECTORS FROM DRUM WRITERS TO HEADS

BIT	DH PIN	AMP CONN	PU PIN	BIT	DH PIN	AMP CONN	PU PIN
P	1-3	J6m	22J DF1				
	1-5	J7m	DF6				
L5	2-3	J6p	DJ6	R5	18-3	J6b	22J MJ6
	2-5	J7p	DJ1		18-5	J7b	MJ1
L1	3-3	J6r	EJ1	R1	19-3	J6c	NF1
	3-5	J7r	EF6		19-5	J7c	NF6
L2	4-3	J6s	EJ6	R2	20-3	J6d	NJ6
	4-5	J7s	EJ1		20-5	J7d	NJ1
L3	5-3	J6t	FF1	R3	21-3	J6e	PF1
	5-5	J7t	FF6		21-5	J7e	PF6
L4	6-3	J6u	FJ6	R4	22-3	J6P	PJ6
	6-5	J7u	FJ1		22-5	J7F	PJ1
L5	7-3	J6v	GF1	R5	23-3	J6g	RF1
	7-5	J7v	GF6		23-5	J7g	RF6
L6	8-3	J6w	GJ6	R6	24-3	J6h	RJ6
	8-5	J7w	GJ1		24-5	J7h	RJ1
L7	9-3	J6m	HF1	R7	25-3	J6J	SF1
	9-5	J2m	HF6		25-5	J7J	SF6
L8	10-3	J6n	HJ6	R8	26-3	J6k	SJ6
	10-5	J2n	HJ1		26-5	J7k	SJ1
L9	11-3	J6p	JF1	R9	27-3	J6a	TF1
	11-5	J2p	JF6		27-5	J2a	TF6
L10	12-3	J6r	JJ6	R10	28-3	J6b	TJ6
	12-5	J2r	JJ1		28-5	J2b	TJ1
L11	13-3	J6s	KF1	R11	29-3	J6c	UF1
	13-5	J2s	KF6		29-5	J2c	UF6
L12	14-3	J6t	KJ6	R12	30-3	J6d	UJ6
	14-5	J2k	KJ1		30-5	J2d	UJ1
L13	15-3	J6u	LF1	R13	31-3	J6e	VF1
	15-5	J2u	LF6		31-5	J2e	VF6
L14	16-3	J6v	LJ6	R14	32-3	J6F	VJ6
	16-5	J2v	LJ1		32-5	J2F	VJ1
L15	17-3	J6a	MF1	R15	33-3	J6g	WF1
	17-5	J7a	22J MF6		33-5	J2g	22J WF6


MANUAL START READ
MANUAL START WRITE
CD MODE WRITE
21FD
DESELECT
COMPUTER DISCONNECT
POWER ON DISCONNECT
21FC
MANUAL START READ
START READ
MANUAL START WRITE
START WRITE
CD READ
CD WRITE
CD MASTER SYNC
21FG
21FE
21FF
CD WRITE REG FULL
TEST LOAD OD WR REG
IO REGISTER TO WRITE REGISTER
MANUAL START WRITE
START WRITE
NO COMPARE
21FG
21FJ
21FK
SEL MIXED CD-1
21GV
21GW
NOT SELECT LRE & NOT MANUAL TEST
21FK
21FW
COMPARE
READ OUT MIXED ADR
1.2.1
1.3.1(6E)
21GWJ3
21KE24
21ME18
TEST READ STATUS
1.3.3(8E)
READ BY STATUS
21FP
21LF
21KF2e
NO COMPARE
TEST NO COMPARE
21FL
21FR
21HR
1.1.2(3A)
22HPJ1
STATUS WRITE
1.0.15
22HMG5
+150MC
1.0.12
22HMG5
+150MC
BAR 10 DH37
BAR 5 DH38
BAR 6 DH38
BAR 11 DH37
BAR 7 DH38
XTL-2 OD SLOT MARKER CHANNEL
XTL-2 CD SLOT MARKER CHANNEL
1.3.5(11E)
21DD6
21KF2f
21KF2g
21KF2c
22DC
77094
22DD
77509
22DC2g
22DC2c
21BJ1a
1.1.2(6A)
21BAC1
CD-4
1.1.2(5A)
21BAC1
OD-4
1.1.2(5C)
22EWA7
CD-1
1.1.2(5C)
22EWA7
OD-1
1.1.2(5B)
21BXF1
OD-3
1.1.2(6B)
21BXF1
OD-3
1.7.1(10)
XTL-2 SLOT MARKER
1.7.1(10)
EQUALS "0"
XTL-2 STATUS EMPTY
1.7.1(1E)
21BKE5
1.1.2(5E)
21BXA2
CD-1X
1.7.1(6A)
21BKA2
OPERATE
1.7.1(10)
21BKA2
SPARE
XTL-2 CD STATUS REG
XTL-2 OD STATUS REG
XTL-2 CD SLOT MARKER WRITE PULSE STRETCHER
XTL-2 OD SLOT MARKER CHANNEL
XTL-2 OD TEST MARKER CHANNEL STATUS
XTL-2 TEST WRITE
XTL-2 DRUM REMIND
XTL-2 COMPARE
21FK1e
22DD2c
22DC2g
21N C3g
SELECT XTL-2
1.1.1.2(5C)
(22EWA7
STEP DISC CTR
CTR STAGES 2-10 SAME
READ WRITE RESET
SEL CD-4
SEL CD-3
21PE
21PR
21BV
21BK
21BF
21BL
21BJ
22PW
22PX
22DD
22DC
22PWA
22PWB
22PWC
22PWD
22PWE
22PWF
22PWG
22PWH
22PWJ
22PWK
22PWL
22PWM
22PWN
22PWP
22PWR
22PWS
22PWT
22PWU
22PWV
22PWW
22PWX
22PWY
22PWZ
22PWa
22PWb
22PWc
22PWd
22PWe
22PWf
22PWg
22PWh
22PWj
22PWk
22PWm
22PWn
22PWp
22PWr
22PWs
22PWt
22PWu
22PWv
22PWw
22PWx
22PWy
22PWz
22PWA
22PWB
22PWC
22PWD
22PWE
22PWF
22PWG
22PWH
22PWJ
22PWK
22PWL
22PWM
22PWN
22PWP
22PWR
22PWS
22PWT
22PWU
22PWV
22PWW
22PWX
22PWY
22PWZ
22PWa
22PWb
22PWc
22PWd
22PWe
22PWf
22PWg
22PWh
22PWj
22PWk
22PWm
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22PWr
22PWs
22PWt
22PWu
22PWv
22PWw
22PWx
22PWy
22PWz

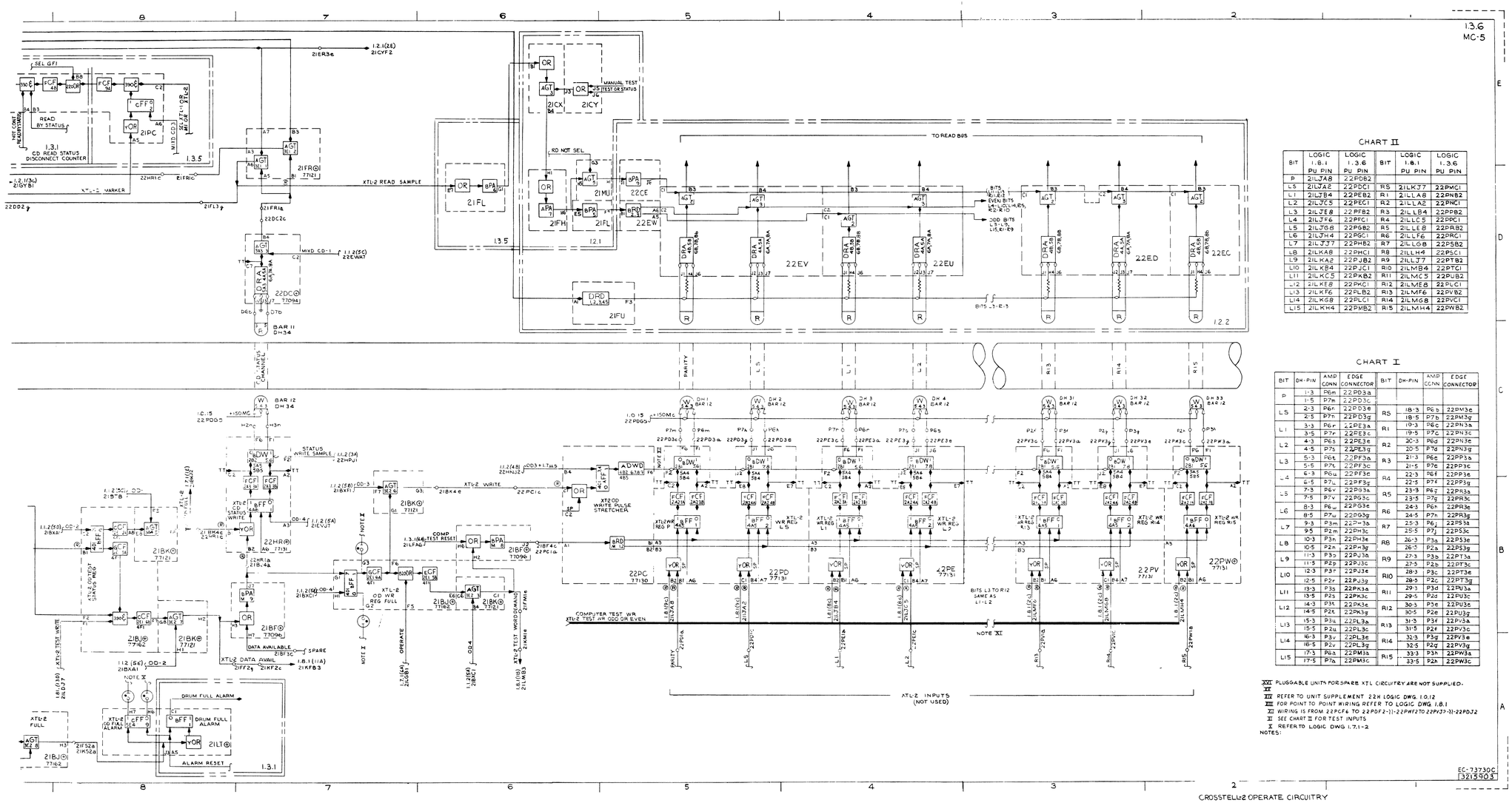


CHART II

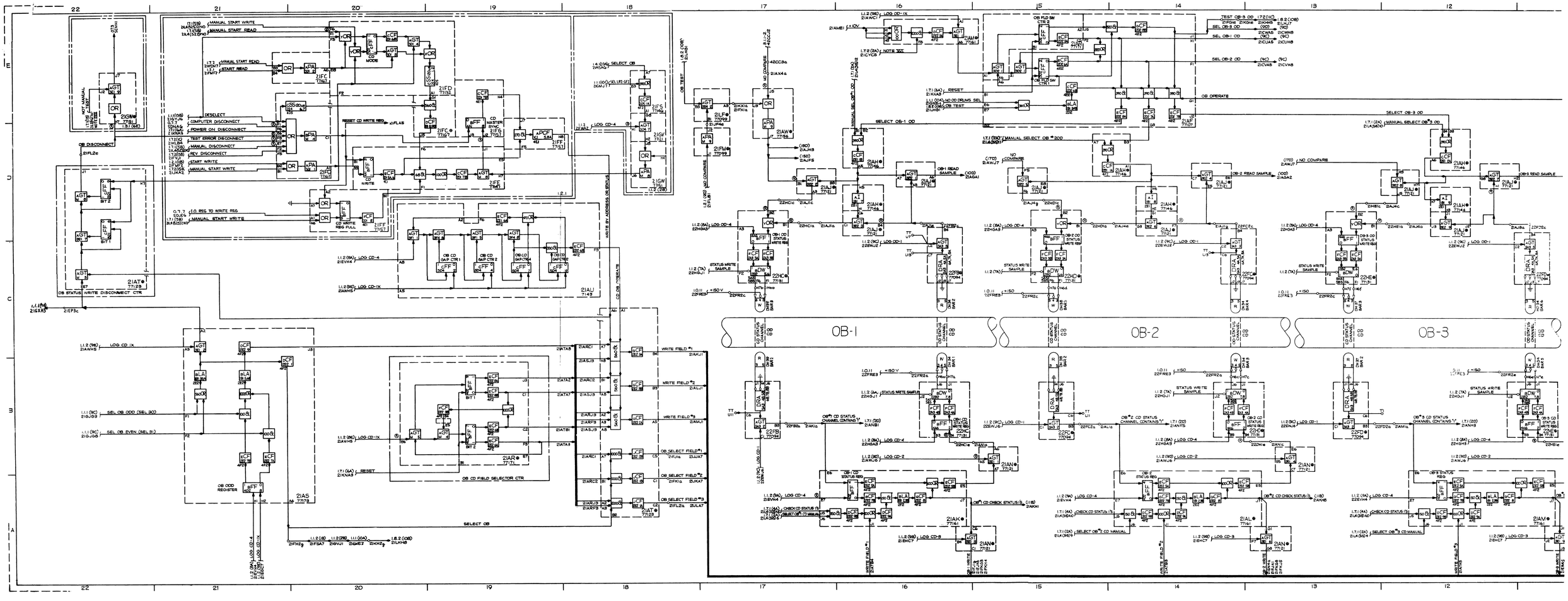
BIT	LOGIC 1.8.1 PU PIN	LOGIC 1.3.6 PU PIN	BIT	LOGIC 1.8.1 PU PIN	LOGIC 1.3.6 PU PIN
P	21LJA8	22PDB2			
L5	21LJA2	22PDC1	R5	21LKJ7	22PMC1
L1	21LJB4	22PEB2	R1	21LLA8	22PNB2
L2	21LJC5	22PEC1	R2	21LLA2	22PNC1
L3	21LJE8	22PFB2	R3	21LLB4	22PPB2
L4	21LJF6	22PFC1	R4	21LLC5	22PPC1
L5	21LJG8	22PGB2	R5	21LLE8	22PRB2
L6	21LJH4	22PGC1	R6	21LLF6	22PRC1
L7	21LJJ7	22PHB2	R7	21LLG8	22PSB2
L8	21LKA8	22PHC1	R8	21LLH4	22PSC1
L9	21LKA2	22PJB2	R9	21LLJ7	22PTB2
L10	21LKB4	22PJC1	R10	21LMB4	22PTC1
L11	21LKC5	22PKB2	R11	21LMC5	22PUB2
L12	21LKE8	22PKC1	R12	21LME8	22PUC1
L13	21LKF6	22PLB2	R13	21LMF6	22PVB2
L14	21LKG8	22PLC1	R14	21LMG8	22PVC1
L15	21LKH4	22PMB2	R15	21LMH4	22PWB2

CHART I

BIT	DH-PIN	AMP CONN	EDGE CONNECTOR	BIT	DH-PIN	AMP CONN	EDGE CONNECTOR
P	1-3	P6m	22PD3a				
	1-5	P7m	22PD3c				
L5	2-3	P6r	22PD3e	R5	18-3	P6b	22PM3e
	2-5	P7n	22PD3g		18-5	P7b	22PM3g
L1	3-3	P6r	22PE3a	R1	19-3	P6c	22PN3a
	3-5	P7p	22PE3c		19-5	P7c	22PN3c
L2	4-3	P6s	22PE3e	R2	20-3	P6d	22PN3e
	4-5	P7s	22PE3g		20-5	P7d	22PN3g
L3	5-3	P6t	22PF3a	R3	21-3	P6e	22PP3a
	5-5	P7t	22PF3c		21-5	P7e	22PP3c
L4	6-3	P6u	22PF3e	R4	22-3	P6f	22PP3e
	6-5	P7u	22PF3g		22-5	P7f	22PP3g
L5	7-3	P6v	22PG3a	R5	23-3	P6g	22PR3a
	7-5	P7v	22PG3c		23-5	P7g	22PR3c
L6	8-3	P6w	22PG3e	R6	24-3	P6h	22PR3e
	8-5	P7w	22PG3g		24-5	P7h	22PR3g
L7	9-3	P3m	22P-3b	R7	25-3	P6j	22PS3a
	9-5	P2m	22PH3c		25-5	P7j	22PS3c
L8	10-3	P3n	22PH3e	R8	26-3	P3a	22PS3e
	10-5	P2n	22P-3g		26-5	P2a	22PS3g
L9	11-3	P3b	22PJ3a	R9	27-3	P3b	22PT3a
	11-5	P2p	22PJ3c		27-5	P2b	22PT3c
L10	12-3	P3r	22PJ3e	R10	28-3	P3c	22PT3e
	12-5	P2r	22PJ3g		28-5	P2c	22PT3g
L11	13-3	P3s	22PK3a	R11	29-3	P3d	22PU3a
	13-5	P2s	22PK3c		29-5	P2d	22PU3c
L12	14-3	P3t	22PK3e	R12	30-3	P3e	22PU3e
	14-5	P2t	22PK3g		30-5	P2e	22PU3g
L13	15-3	P3u	22PL3a	R13	31-3	P3f	22PV3a
	15-5	P2u	22PL3c		31-5	P2f	22PV3c
L14	16-3	P3v	22PL3e	R14	32-3	P3g	22PV3e
	16-5	P2v	22PL3g		32-5	P2g	22PV3g
L15	17-3	P6a	22PM3a	R15	33-3	P3h	22PW3a
	17-5	P7a	22PM3c		33-5	P2h	22PW3c

XXI PLUGGABLE UNITS FOR SPARE XTL CIRCUITRY ARE NOT SUPPLIED.
XI
III REFER TO UNIT SUPPLEMENT 22K LOGIC DWG. 1.0.12
III FOR POINT TO POINT WIRING REFER TO LOGIC DWG. 1.8.1
II WIRING IS FROM 22PCF6 TO 22PDF2-1)-22PWF2TO 22PW37-7)-22PDJ2
II SEE CHART II FOR TEST INPUTS
X REFER TO LOGIC DWG. 1.7.1-2
NOTES:

CROSSTELL-2 OPERATE CIRCUITRY


OB-1
OB-2
OB-3
OB DISCONNECT
OB STATUS WRITE DISCONNECT CTR
OB CD FIELD SELECTOR CTR
OB CDD REGISTER
OB CD STATUS CHANNEL CONTAINS
SELECT OB
SELECT OB-1 OD
SELECT OB-2 OD
SELECT OB-3 OD
OB OPERATE
NO COMPARE
OB-1 READ SAMPLE
OB-2 READ SAMPLE
OB-3 READ SAMPLE
STATUS WRITE SAMPLE
WRITE FIELD *1
WRITE FIELD *2
WRITE FIELD *3
OB SELECT FIELD *1
OB SELECT FIELD *2
OB SELECT FIELD *3
MANUAL START WRITE
MANUAL START READ
COMPUTER DISCONNECT
POWER ON DISCONNECT
TEST ERROR DISCONNECT
MANUAL DISCONNECT
REV DISCONNECT
START WRITE
MANUAL START WRITE
RESET
LOG CD-1
LOG CD-2
LOG CD-3
LOG CD-4
LOG CD-IX
SEL OB ODD (SEL 30)
SEL OB EVEN (SEL 31)

1.4.1
MC-5

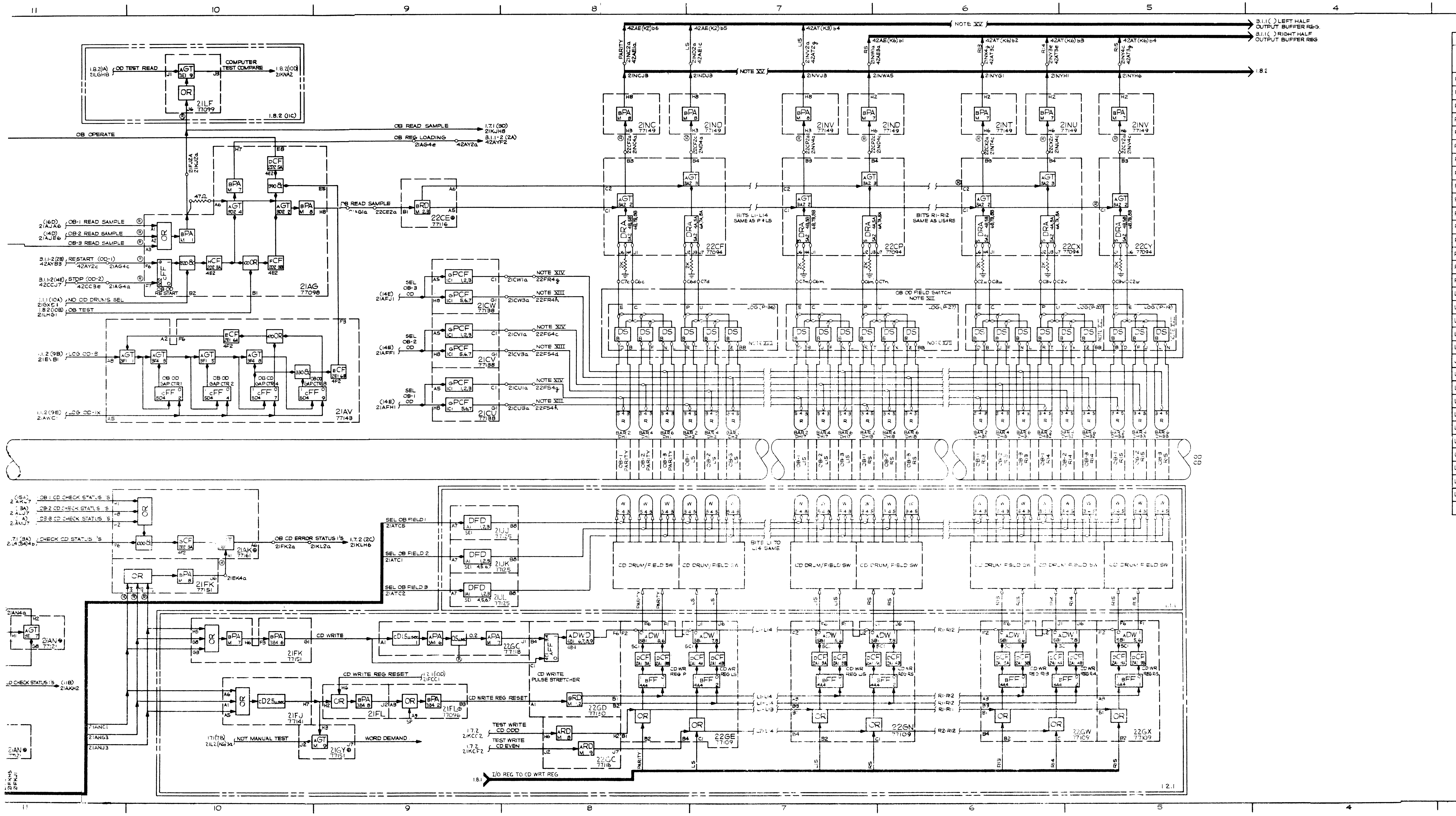


CHART 1					CHART 2				
BIT		FIELD SWITCH CAN	FIELD SWITCH PIN	AMP CONN	READ CIRCUIT OUTPUT PIN	TEST READ GATE INPUT PIN	EDGE CONNECTOR	EDGE CONNECTOR	OUTPUT BUFFER REGISTER INPUT PIN
R15	1 / 0	P19	C / E	C3w / C2w	21NVH2	21NYH6	21NY4c	42AT3g	42AT(K6)b4
R14	1 / 0	P20	P / U	C3v / C2v	21NUH2	21NYH1	21NY3e	42AT3e	42AT(K6)b3
R13	1 / 0		C / E	C3u / C2u	21NTH2	21NYG1	21NX4g	42AT3c	42AT(K6)b2
R12	1 / 0	P17	P / U	C3t / C2t	21NSH2	21NYF1	21NX4a	42AT3a	42AT(K6)b1
R11	1 / 0		C / E	C3s / C2s	21NRH2	21NYE5	21NX3c	42AN3g	42AN(K6)b4
R10	1 / 0	P22	P / U	C3r / C2r	21NPH2	21NYC7	21NX3a	42AN3e	42AN(K6)b3
R9	1 / 0		C / E	C3p / C2p	21NNH2	21NYB1	21NY1g	42AN3c	42AN(K6)b2
R8	1 / 0	P23	P / U	C3n / C2n	21NMH2	21NYA5	21NY1a	42AN3a	42AN(K6)b1
R7	1 / 0		C / E	C3m / C2m	21NLH2	21NWH6	21NW4c	42AJ3g	42AJ(K6)b4
R6	1 / 0	P24	P / U	C6v / C7v	21NKH2	21NWH1	21NW3e	42AJ3e	42AJ(K6)b3
R5	1 / 0		C / E	C6u / C7u	21NJH2	21NWG1	21NX2g	42AJ3c	42AJ(K6)b2
R4	1 / 0	P25	P / U	C6t / C7t	21NHH2	21NWF1	21NX2a	42AJ3a	42AJ(K6)b1
R3	1 / 0		C / E	C6s / C7s	21NGH2	21NWE5	21NX1c	42AE3g	42AE(K6)b4
R2	1 / 0	P26	P / U	C6r / C7r	21NFH2	21NWC7	21NX1a	42AE3e	42AE(K6)b3
R1	1 / 0		C / E	C6p / C7p	21NEH2	21NWB1	21NW1g	42AE3c	42AE(K6)b2
RS	1 / 0	P27	P / U	C6n / C7n	21NDH2	21NWA5	21NW1a	42AE3a	42AE(K6)b1
L15	1 / 0		C / E	C6m / C7m	21NVH8	21NVJ3	21NV2a	42AT2g	42AT(K3)b4
L14	1 / 0	P28	P / U	C3r / C2r	21NUH8	21NUJ3	21NU2a	42AT2e	42AT(K3)b3
L13	1 / 0		C / E	C3h / C2h	21NTH8	21NTJ3	21NT2a	42AT2c	42AT(K3)b2
L12	1 / 0	P29	P / U	C3g / C2g	21NSH8	21NSJ3	21NS2a	42AT2a	42AT(K3)b1
L11	1 / 0		C / E	C3f / C2f	21NRH8	21NRJ3	21NR2a	42AN2g	42AN(K3)b4
L10	1 / 0	P30	P / U	C3e / C2e	21NPH8	21NPJ3	21NP2a	42AN2e	42AN(K3)b3
L9	1 / 0		C / E	C3d / C2d	21NNH8	21NNJ3	21NN2a	42AN2c	42AN(K3)b2
L8	1 / 0	P31	P / U	C3c / C2c	21NMH8	21NMJ3	21NM2a	42AN2a	42AN(K3)b1
L7	1 / 0		C / E	C3b / C2b	21NLH8	21NLJ3	21NL2a	42AJ2g	42AJ(K3)b4
L6	1 / 0	P32	P / U	C3a / C2a	21NKH8	21NKJ3	21NK2a	42AJ2e	42AJ(K3)b3
L5	1 / 0		C / E	C6r / C7r	21NJH8	21NJJ3	21NJ2a	42AJ2c	42AJ(K3)b2
L4	1 / 0	P34	P / U	C6h / C7h	21NHH8	21NHJ3	21NH2a	42AJ2a	42AJ(K3)b1
L3	1 / 0		C / E	C6g / C7g	21NGH8	21NGJ3	21NG2a	42AE2e	42AE(K2)b2
L2	1 / 0	P35	P / U	C6f / C7f	21NFH8	21NFJ3	21NF2a	42AE2c	42AE(K2)b3
L1	1 / 0		C / E	C6e / C7e	21NEH8	21NEJ3	21NE2a	42AE2a	42AE(K2)b4
LS	1 / 0	P36	P / U	C6d / C7d	21NDH8	21NDJ3	21ND2a	42AE1c	42AE(K2)b5
P	1 / 0		C / E	C6c / C7c	21NCH8	21NCJ3	21NC2a	42AE1a	42AE(K2)b6

NOTES:

XVIII RELAY LOCATION IS FOR SYS 1-16 & 23 ONLY FOR SYS 17-22, 24 AND HIGHER, COMPARABLE POINT WOULD BE 21L2(K3)7

XVII FOR LOCATION AND PART NUMBER OF DIODE SWITCH CANS REFER TO THE FOLLOWING

SYS	LOGIC	DWG NO
DC-1,2,3-8,9-11,12	1.0.22	3131884
CC-1,2,+3	1.0.22	3131882
DC-13-18	1.0.22	3115601
DC-19	1.0.22	3136309
DC-20-22	1.0.22	3107997

XVI NOT MANUAL TEST OR NOT ERROR OR NOT STOP ON ERROR

XV SEE CHART 2 FOR WIRING FROM UNIT 21 READ CIRCUIT TO UNIT 42 OUTPUT BUFFER REGISTER

XIV THIS LINE CONNECTS TO PARITY AND ALL OTHER ODD BITS

XIII THIS LINE CONNECTS TO LS AND ALL OTHER EVEN BITS

XII SEE CHART 1 FOR LOCATION OF ALL FIELD SWITCH CANS AND WIRING FROM CANS TO AMP CONNECTORS

EC R-49861
3107999

MAIN DRUM OUTPUT BUFFER STATUS OPERATE

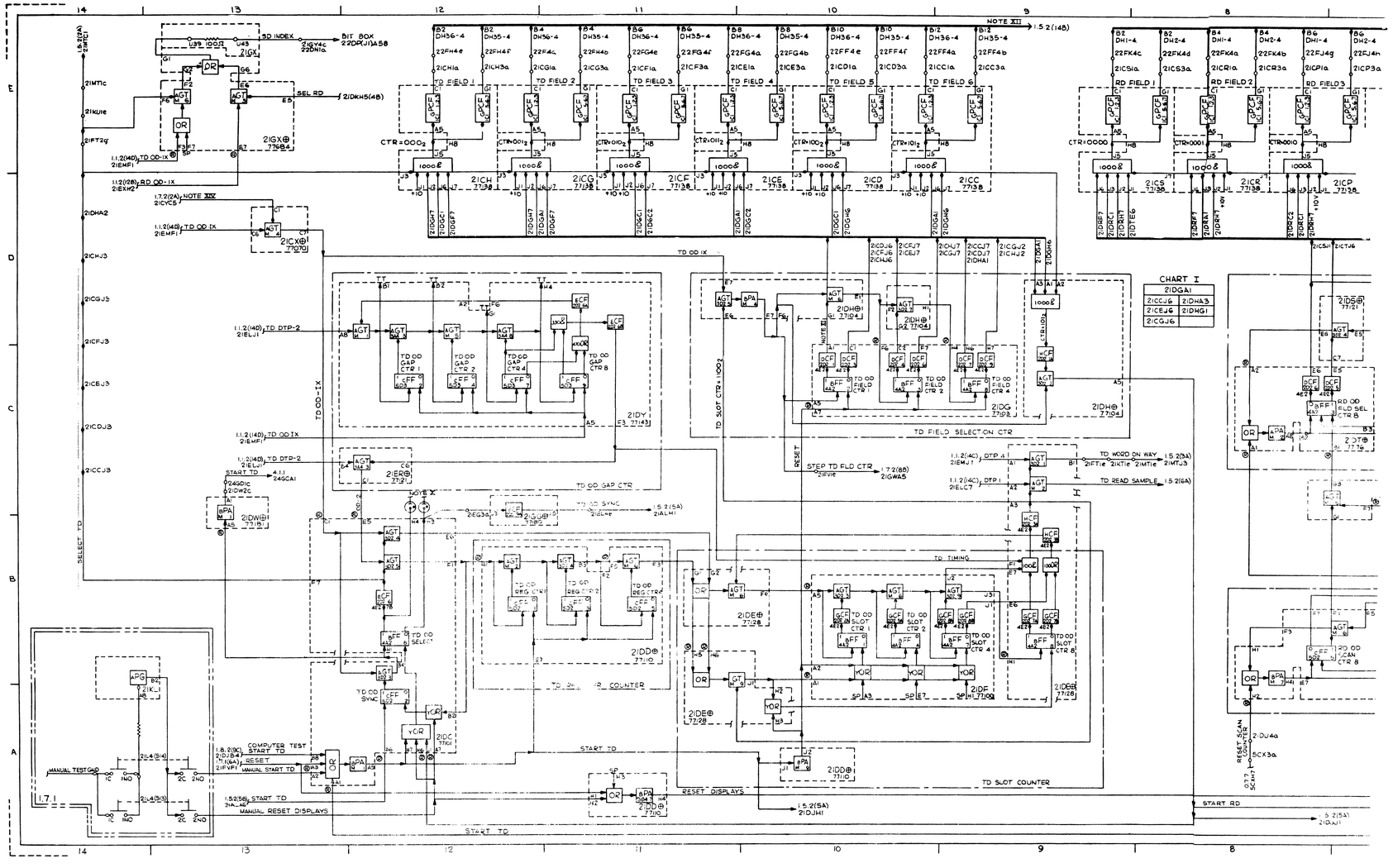
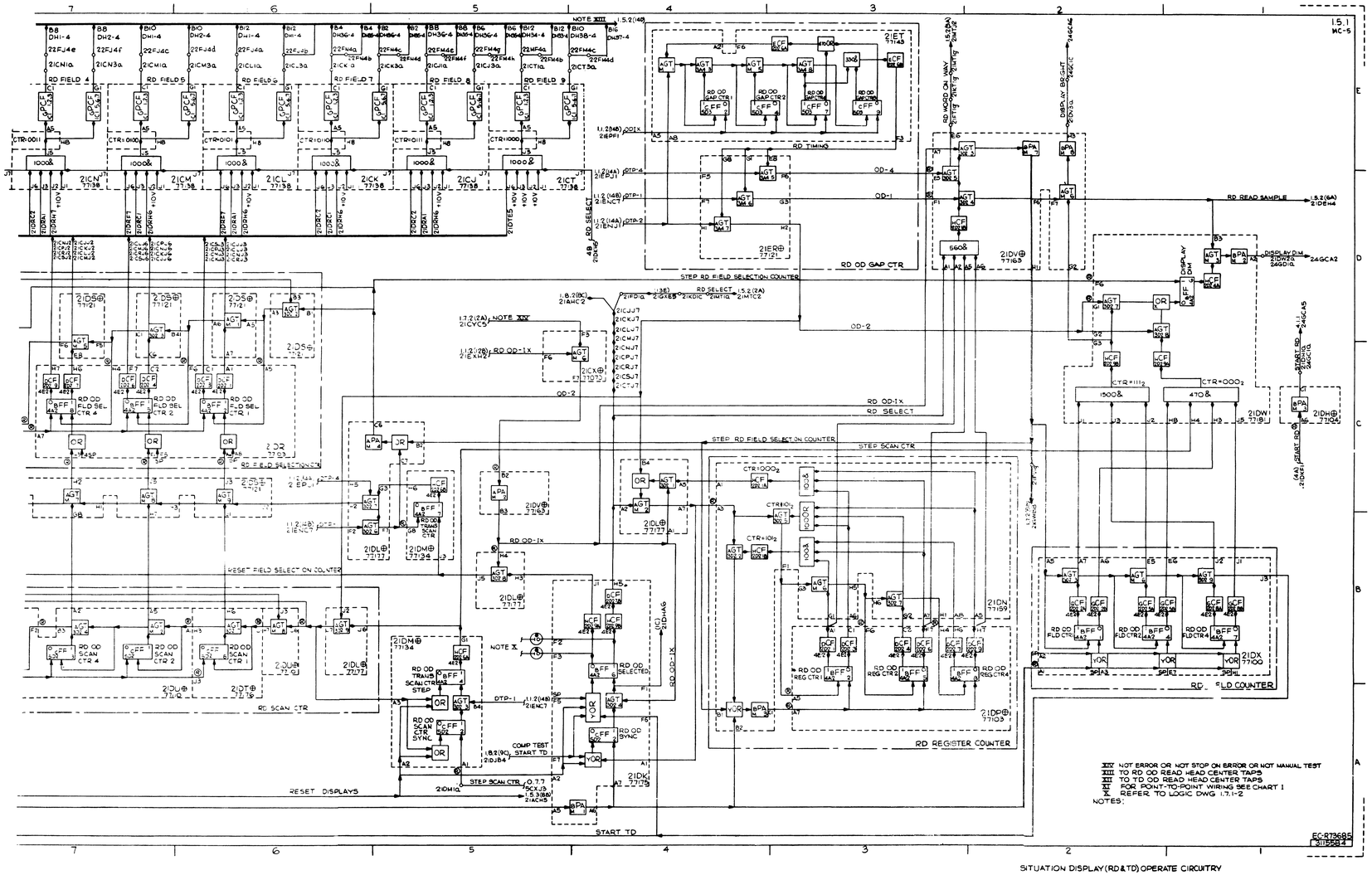
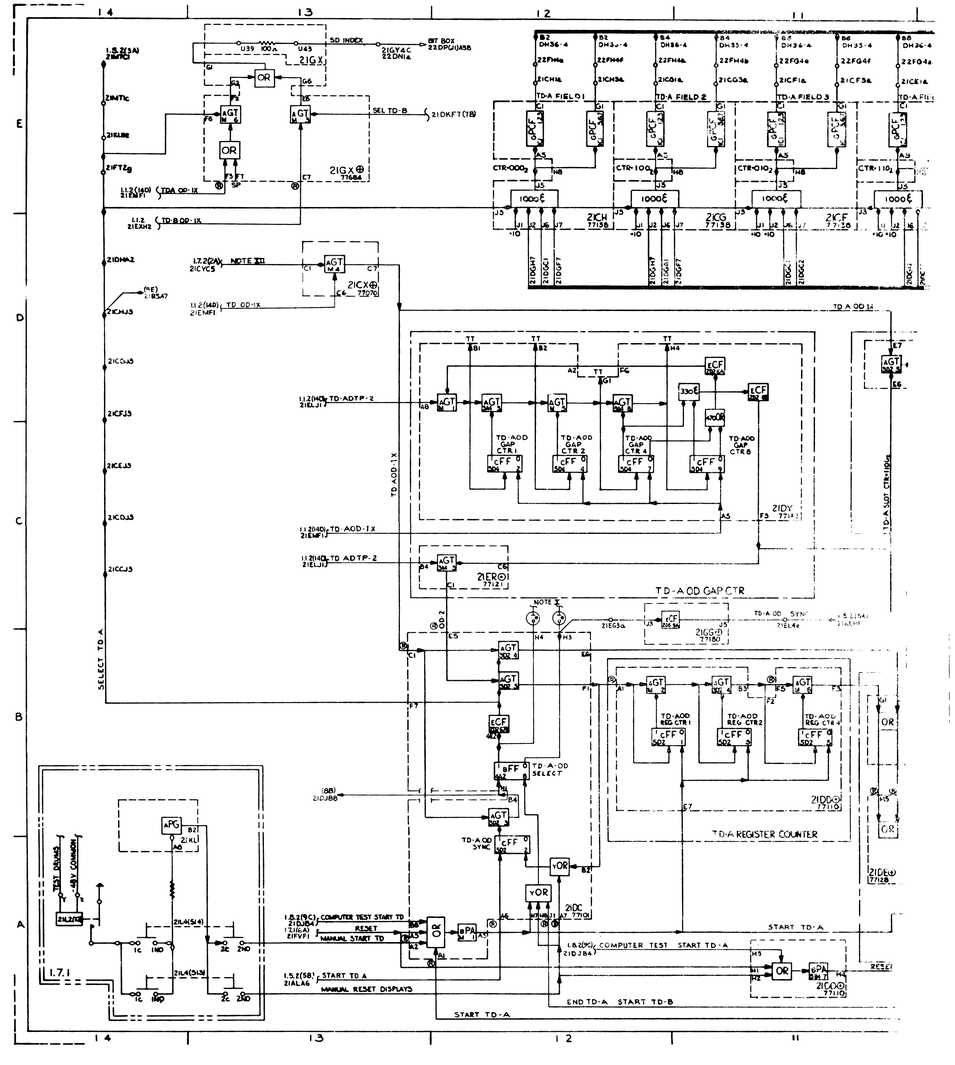
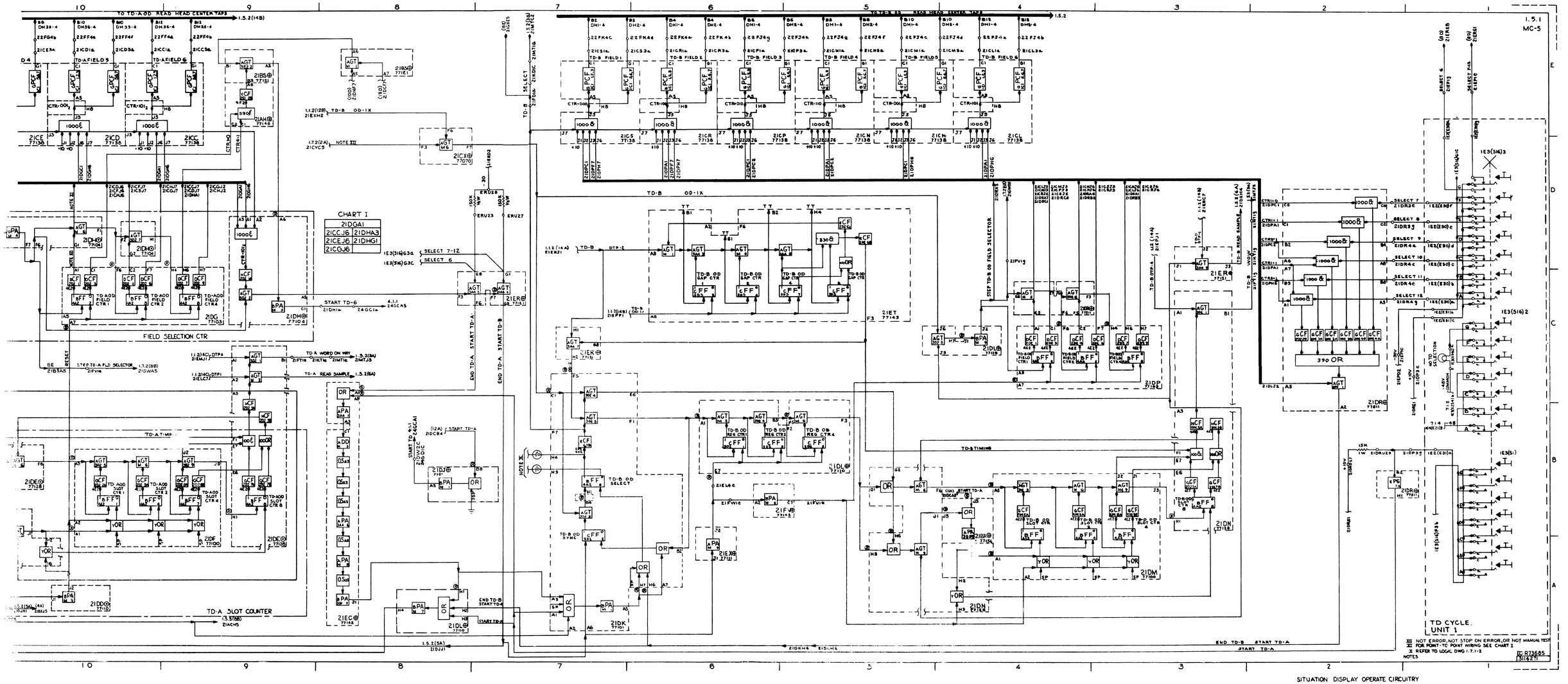


CHART I
2IDGA1
2ICGJ6 2IDHA3
2ICEJ6 2IDHG1
2ICGJ6
TD FIELD SELECTION CTR
TD SLOT CTR = 1002
TD SLOT COUNTER
TD TIMING
TD FIELD 1
TD FIELD 2
TD FIELD 3
TD FIELD 4
TD FIELD 5
TD FIELD 6
RD FIELD 1
RD FIELD 2
RD FIELD 3
TD OD-1X
SELECT TD
START TD
RESET DISPLAYS
MANUAL RESET DISPLAYS
MANUAL TEST GO
COMPUTER TEST START TD
MANUAL START TD
RESET
STEP TD FLD CTR
TD WORD ON WAY
TD READ SAMPLE
START RD
RESET SCAN
TD OD GAP CTR
TD OD SYNC
TD OD SELECT
TD OD SLOT CTR 1
TD OD SLOT CTR 2
TD OD SLOT CTR 4
TD OD SLOT CTR 8
RD OD FLD SEL CTR 8
RD OD SCAN CTR 8
NOTE XII
BIT BOX 22DP(J1)A58
SD INDEX



SITUATION DISPLAY (RD & TD) OPERATE CIRCUITRY


TD-A FIELD 1
TD-A FIELD 2
TD-A FIELD 3
TD A OD 1X
TD A OD 2X
TD-A OD GAP CTR
TD-A REGISTER COUNTER
TD-A OD SELECT
SELECT TD-A
START TD-A
END TD-A START TD-B
RESET
MANUAL START TD
MANUAL RESET DISPLAYS
TEST LAMPS
-48V COMMON


TD CYCLE, UNIT 1
SITUATION DISPLAY OPERATE CIRCUITRY
TD-A 3LOT COUNTER
FIELD SELECTION CTR
TD-A TIMING
TD-B TIMING
TD-B OD SELECT
CHART I
21DGA1
21CCJ6 21DHA3
21CEJ6 21DHG1
21CGJ6
NOTES
MC-5

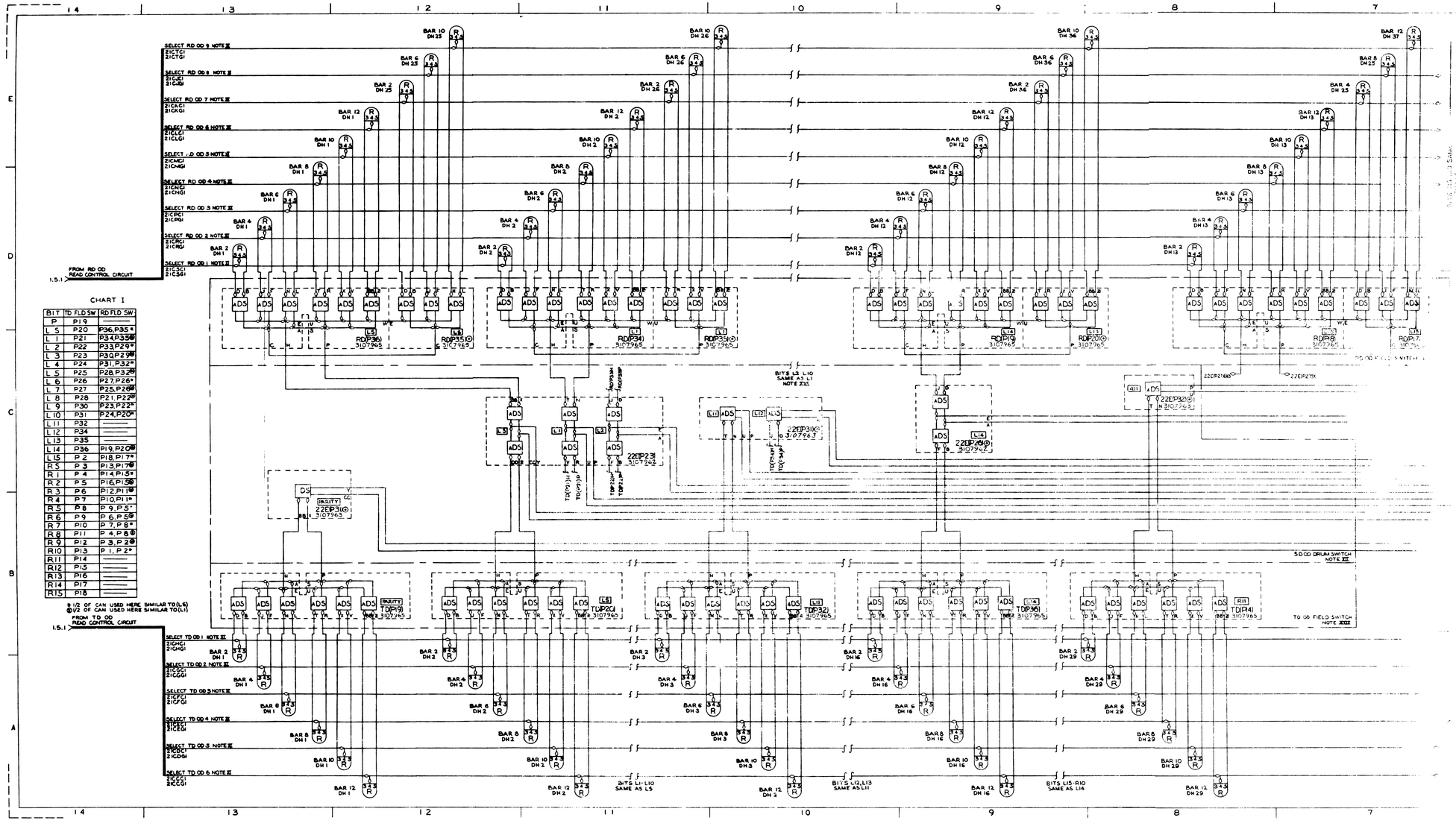


CHART I

BIT	TD FLD SW	RD FLD SW
P	P19	——
L 5	P20	P36, P35 *
L 1	P21	P34, P35 ⊗
L 2	P22	P33, P29 *
L 3	P23	P30, P29 ⊗
L 4	P24	P31, P32 *
L 5	P25	P28, P32 ⊗
L 6	P26	P27, P26 *
L 7	P27	P25, P26 ⊗
L 8	P28	P21, P22 ⊗
L 9	P30	P23, P22 *
L 10	P31	P24, P20 *
L 11	P32	——
L 12	P34	——
L 13	P35	——
L 14	P36	P19, P20 ⊗
L 15	P 2	P18, P17 *
R 5	P 3	P13, P17 ⊗
R 1	P 4	P14, P15 *
R 2	P 5	P16, P15 ⊗
R 3	P 6	P12, P11 ⊗
R 4	P 7	P10, P11 *
R 5	P 8	P 9, P 5 *
R 6	P 9	P 6, P 5 ⊗
R 7	P10	P 7, P 8 *
R 8	P11	P 4, P 8 ⊗
R 9	P12	P 3, P 2 ⊗
R10	P13	P 1, P 2 *
R11	P14	——
R12	P15	——
R13	P16	——
R14	P17	——
R15	P18	——

⊗1/2 OF CAN USED HERE SIMILAR TO (L6)
⊗1/2 OF CAN USED HERE SIMILAR TO (L1)

SD READ INFO TO COMPUTER TEST READ GATES → 1.8.2

TO SD ELEMENT

BITS R13-R14 SAME

BITS R1-R8 SAME

BITS L3-L10 SAME

NOTE XIV

22DY 77094 · 22DW 77094 · 22DV 77094 · 22DP 77094 · 22DN 77094 · 22DM 77094 · 22DG 77094 · 22DF 77094 · 22DE 77116 · 21DJ 77101 · 21DE 77128 · 21AL 77161 · 21MS 77111 · 21MT 77148

2INV 77149 · 2INS 77149 · 2INR 77149 · 2INP 77149 · 2INN 77149 · 2IND 77149 · 2INV 77149 · 2INU 77149 · 2INT 77149 · 2INS 77149 · 2INR 77149 · 2INF 77149 · 2INE 77149 · 2IND 77149 · 2INC 77149

SD RDS SAMPLE TO BIT BOX → 22 DP (J) A54

START TD → 1.5.1 (12A) 21DCA6

1.5.1 (9C) TD READ SAMPLE
1.5.1 (2D) RD READ SAMPLE Ⓚ
21DVFG

1.1.1 (10B) NO OD DRUMS SEL 21GXB4

1.8.2 (20C) SD TEST 21LHC7

1.5.1 (12C) START TD 21DAA3 · 1.7.1 (15B) MAN. RESET DISP 21DJH7 · 1.5.1 (9C) START RD 21DHA3

1.1.2 (14C) DTP-4 21EWJ1 · 1.5.1 (11B) TD OD SYNC 21661S

1.1.2 21ENC7 · 21EWJ1 · 21EPC7 · 21EPJ1 · 21ELC7 · 21ELJ1 · 21EMC7 · 21EMJ1 · 1.1.2 21ELC7 · 1.1.2 21ENC7 · 1.5.1 (13B) 21DCE8 · 1.5.1 (13C) 21DKH5 · 1.5.1 (11B) 21DCE7 · 1.5.1 (12B) 21DKH5

CHART II

BIT	OUTPUT	COMP TEST	EDGE CONN.	EDGE CONN.	S-D ELEMENT
P	2INCE7	2INCJ7	2INC4e	———	———
LS	DE7	DJ7	D4e	24JY2a	24JYA1
L1	EE7	EJ7	E4e	Y2c	YA5
L2	FE7	FJ7	F4e	Y2e	YD5
L3	GE7	GJ7	G4e	Y3a	YJ6
L4	HE7	HJ7	H4e	X2a	YA2
L5	JE7	JJ7	J4e	X2c	YD6
L6	KE7	KJ7	K4e	Y3c	YJ7
L7	LE7	LJ7	L4e	X2e	YA6
L8	ME7	MJ7	M4e	W2a	YD7
L9	NE7	NJ7	N4e	Y3e	YG2
L10	PE7	PJ7	P4e	W2c	YA3
L11	RE7	RJ7	R4e	W2e	YD8
L12	SE7	SJ7	S4e	24JX3a	YG6
L13	TE7	TJ7	T4e	24HY3a	YA7
L14	UE7	UJ7	U4e	24JX3c	YJ3
L15	VE7	VJ7	V4e	24JX3e	24JYG3
RS	DF7	WA6	W1c	24FY1a	24FYA1
R1	EF7	WB2	W2a	Y1c	YA5
R2	FF7	WC1	W2e	Y1e	YD5
R3	GF7	WE6	X1e	Y4a	YJ6
R4	HF7	WF2	X2c	X1a	YA2
R5	JF7	WG2	W3a	X1c	YD6
R6	KF7	WH2	W3g	Y4c	YJ7
R7	LF7	WH7	W4e	X1e	YA6
R8	MF7	YA6	Y1c	W1a	YD7
R9	NF7	YB2	Y2a	Y4e	YG2
R10	PF7	YC1	Y2e	W1c	YA3
R11	RF7	YE6	X3e	W1e	YD8
R12	SF7	YF2	X4c	24FX4a	YG6
R13	TF7	YG2	Y3a	24EW4a	YA7
R14	UF7	YH2	Y3g	24FX4c	YJ3
R15	2INVF7	2INYH7	2INY4e	24FX4e	24FYG3

BIT	SD DRUM SWITCH	AMP CONN	DRA 22D	BIT	SD DRUM SWITCH	AMP CONN	DRA 22D
P	P31-Y	D6c	RJ1				
	P31-CC	D7c	RJ6				
LS	P23-Y	D6f	RJ2	RS	P27-P	D6r	RJ2
	P23-CC	D7f	RJ7		P27-U	D7r	RJ7
L1	P23-P	D6g	GJ1	R1	P27-E	D6s	RJ1
	P23-U	D7g	GJ6		P27-A	D7s	RJ6
L2	P23-E	D6h	GJ2	R2	P28-Y	D6t	RJ2
	P23-A	D7h	GJ7		P28-CC	D7t	RJ7
L3	P24-Y	D6j	HJ1	R3	P28-P	D6u	SJ1
	P24-CC	D7j	HJ6		P28-U	D7u	SJ6
L4	P24-P	D3a	HJ2	R4	P28-E	D6v	SJ2
	P24-U	D7j	HJ7		P28-A	D7v	SJ7
L5	P24-E	D3b	JJ1	R5	P29-Y	D6w	TJ1
	P24-A	D2b	JJ6		P29-CC	D7w	TJ6
L6	P25-Y	D3c	JJ2	R6	P29-P	D3 l	TJ2
	P25-CC	D2c	JJ7		P29-U	D2 l	TJ7
L7	P25-P	D3d	KJ1	R7	P29-E	D3m	UJ1
	P25-U	D2d	KJ6		P29-A	D2m	UJ6
L8	P25-E	D3e	KJ2	R8	P30-Y	D3n	UJ2
	P25-A	D2e	KJ7		P30-CC	D2n	UJ7
L9	P26-Y	D3f	LJ1	R9	P30-P	D3p	VJ1
	P26-CC	D2f	LJ6		P30-U	D2p	VJ6
L10	P26-P	D3g	LJ2	R10	P30-E	D3r	VJ2
	P26-U	D2g	LJ7		P30-A	D2r	VJ7
L11	P31-P	D3L	MJ1	R11	P32-P	D3s	WJ1
	P31-U	D2h	MJ6		P32-U	D2s	WJ6
L12	P31-E	D3j	MJ2	R12	P32-E	D3t	WJ2
	P31-A	D2j	MJ7		P32-A	D2t	WJ7
L13	P32-Y	D6m	NJ1	R13	P33-Y	D3u	XJ1
	P32-CC	D7m	NJ6		P33-CC	D2u	XJ6
L14	P26-E	D6n	NJ2	R14	P33-P	D3v	XJ2
	P26-A	D7m	NJ7		P33-U	D2v	XJ7
L15	P27-Y	D6p	PJ1	R15	P33-E	D3w	YJ1
	P27-CC	D7p	PJ6		P33-A	D2w	YJ6

XIV WIRING SHOWN IS NOT POINT TO POINT
XIV SEE CHART II FOR WIRING FROM THE READ CIRCUIT OUTPUT TO THE SITUATION DISPLAY ELEMENT AND COMPUTER TEST READ CKTS
XIII SEE CHART I FOR LOCATION OF FIELD SWITCH CANS. EACH BIT IN A RADAR DISPLAY WORD REQUIRES ONE AND A HALF FIELD SWITCH CANS. BITS P, LII, LI2, LI3, RII, RI2, RI3, RI4 AND RI5 ARE NOT USED ON R.D. DRUM.
XII SEE CHART III FOR LOCATION OF DRUM SWITCH CANS. BITS L13, RII, RI2, RI3, RI4, RI5 USE THE SAME TYPE DRUM SWITCH CAN (3107963) AS ILLUSTRATED FOR P, LII AND LI2 (P31). ALL OTHER BITS USE THE SAME TYPE DRUM SWITCH CAN (3107962) ILLUSTRATED FOR LS, LI AND L2 (P23).
XI SHIELDED TWISTED PAIR WIRE IS USED FROM EDGE CONNECTOR TO HEAD CENTER TOPS. ALL EVEN (ALSO ALL ODD) HEAD CENTER TAP TERMINALS OF THE SAME FIELD AND BAR ARE JUMPERED TOGETHER. (EACH FIELD ON RD USES ONLY HEADS LS THRU L10, L14 THRU R10)
X INPUTS INDICATED ARE USED ONLY FOR TEST PURPOSES. REFER TO LOGIC DRAWING.

NOTES

EER-73685
3107993

SITUATION DISPLAY OD FIELD SWITCHING & READ CIRCUITRY

CHART 2

DIGITAL DISPLAY INFORMATION PULSE OUTPUT WIRING

BIT	UNIT 21 EDGE CONN	UNIT 25 EDGE CONN	UNIT 25 PU PIN	BIT	UNIT 21 TESTRUN	UNIT 21 EDGE CONN	UNIT 25 EDGE CONN	UNIT 25 PU PIN
L 1	21NE 3c	25BC 1g	25BEA5	R 1	21NWB3	21NW 2c	25CC 1g	25CEA5
L 2	↓ F 3c	↓ D 1e	25BED5	R 2	↓ C2	↓ W 2g	↓ D 1e	↓ D5
L 3	G 3c	D 1g	25BEJ6	R 3	E7	X 1g	D 1g	J6
L 4	H 3c	E 1e	25BEA2	R 4	F3	X 2e	E 1e	A2
L 5	J 3c	E 1g	↓ D6	R 5	G3	W 3c	E 1g	D6
L 6	K 3c	F 1e	J7	R 6	↓ H3	W 4a	F 1e	J7
L 7	L 3c	F 1g	A6	R 7	21NWH8	W 4g	F 1g	A6
L 8	M 3c	G 1e	D7	R 8	21NYA7	Y 1e	G 1e	D7
L 9	N 3c	↓ G 1g	G2	R 9	B3	Y 2c	G 1g	G2
L 10	P 3c	25BC 1a	A3	R 10	C2	Y 2g	G 2e	A3
L 11	R 3c	25AE 4a	D8	R 11	↓ E7	↓ X 3g	↓ E 3g	↓ D8
L 12	S 3c	25BE 3e	G6	R 12	21NYF 3	21NX 4e	25CC 4a	25CEG6
L 13	↓ T 3c	25BF 1a	↓ A7					
L 14	21NU 3c	25BC 4a	25BEJ3					

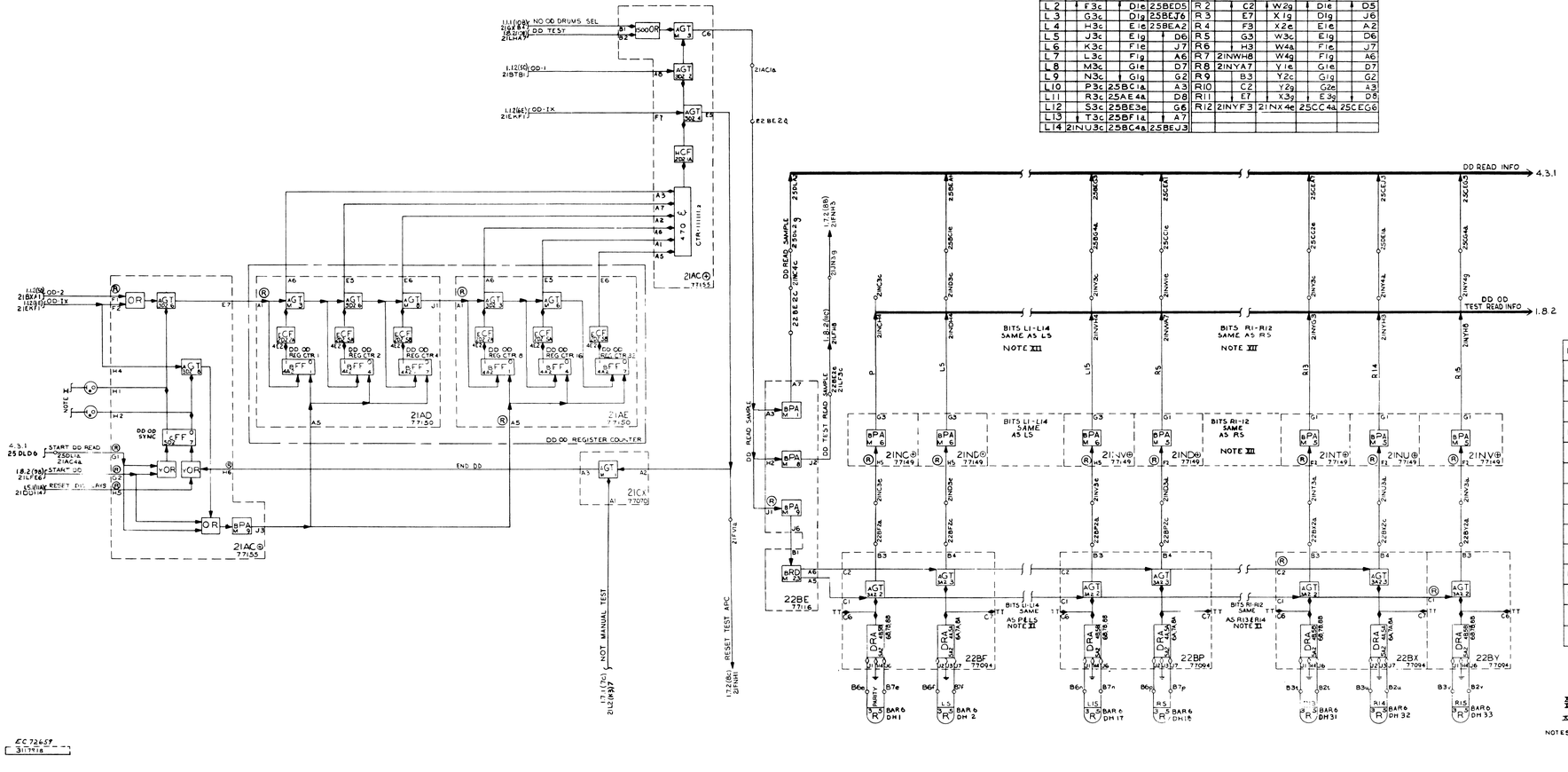


CHART 1

DIGITAL DISPLAY READ CIRCUIT WIRING

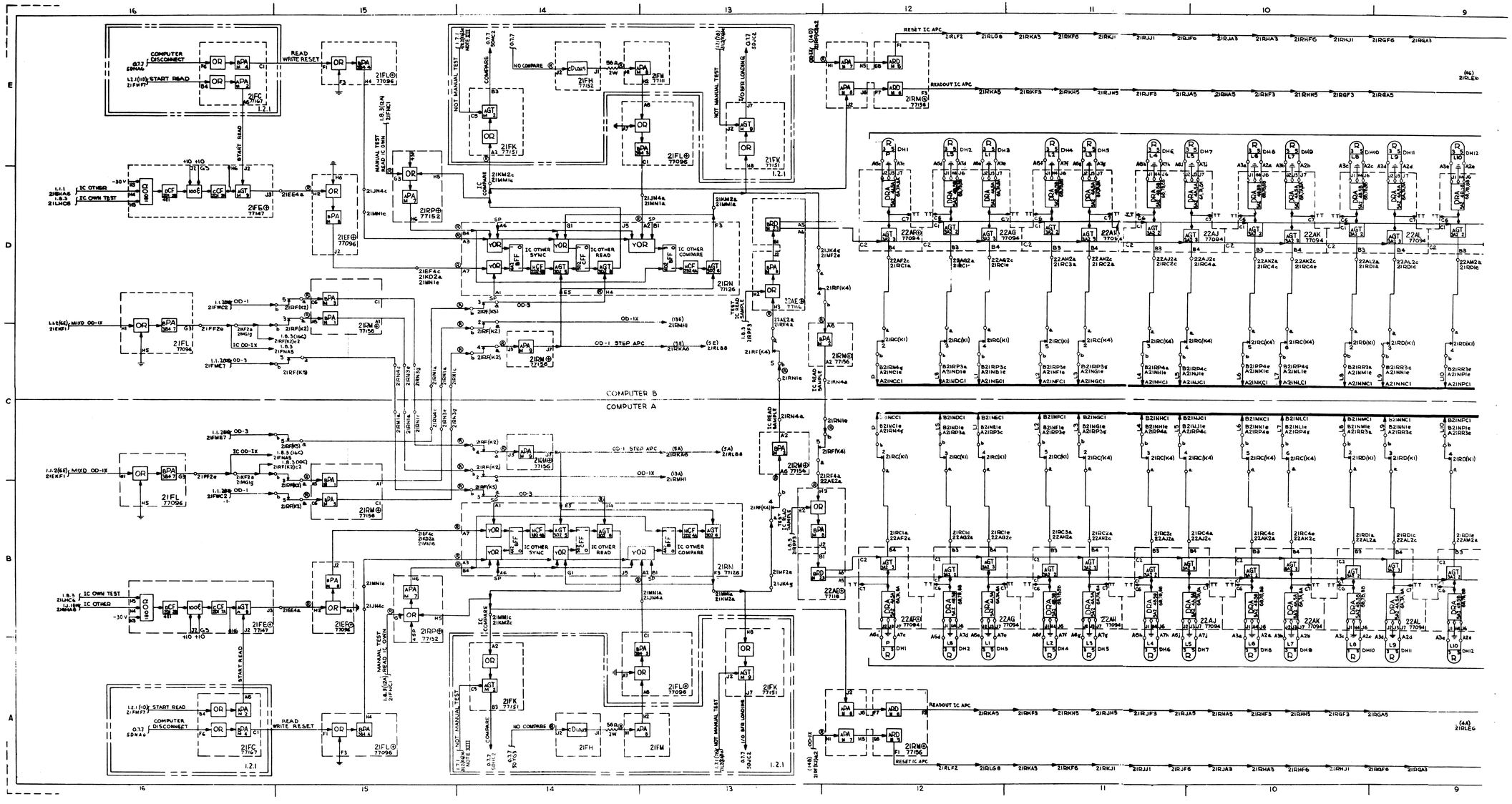
BIT	HEAD & PIN	AMP CONN	P U PIN	BIT	HEAD & PIN	AMP CONN	P U PIN
L 1	DH3-3	B6g	22BGJ1	R 1	DH19-3	B6r	22BRJ1
	DH3-5	B7g	↓ GJ6		DH19-5	B7r	↓ RJ6
L 2	DH4-3	B6h	GJ2	R 2	DH20-3	B6s	RJ2
	DH4-5	B7h	GJ7		DH20-5	B7s	RJ7
L 3	DH5-3	B6j	HJ1	R 3	DH21-3	B6t	SJ1
	DH5-5	B7j	HJ6		DH21-5	B7t	SJ6
L 4	DH6-3	B6k	HJ2	R 4	DH22-3	B6u	SJ2
	DH6-5	B7k	HJ7		DH22-5	B7u	SJ7
L 5	DH7-3	B3a	JJ1	R 5	DH23-3	B6v	TJ1
	DH7-5	B2a	JJ6		DH23-5	B7v	TJ6
L 6	DH8-3	B3b	JJ2	R 6	DH24-3	B6w	TJ2
	DH8-5	B2b	JJ7		DH24-5	B7w	TJ7
L 7	DH9-3	B3c	KJ1	R 7	DH25-3	B3t	UJ1
	DH9-5	B2c	KJ6		DH25-5	B2t	UJ6
L 8	DH10-3	B3d	KJ2	R 8	DH26-3	B3m	UJ2
	DH10-5	B2d	KJ7		DH26-5	B2m	UJ7
L 9	DH11-3	B3e	LJ1	R 9	DH27-3	B3n	VJ1
	DH11-5	B2e	LJ6		DH27-5	B2n	VJ6
L 10	DH12-3	B3f	LJ2	R 10	DH28-3	B3p	VJ2
	DH12-5	B2f	LJ7		DH28-5	B2p	VJ7
L 11	DH13-3	B3g	MJ1	R 11	DH29-3	B3r	WJ1
	DH13-5	B2g	MJ6		DH29-5	B2r	WJ6
L 12	DH14-3	B3h	MJ2	R 12	DH30-3	B3s	WJ2
	DH14-5	B2h	MJ7		DH30-5	B2s	22BWJ7
L 13	DH15-3	B6l	NJ1				
	DH15-5	B7l	NJ6				
L 14	DH16-3	B6m	NJ2				
	DH16-5	B7m	22BNJ7				

NOTES:

[II] SEE CHART II FOR OUTPUT WIRING.
[III] SEE CHART I FOR WIRING FROM DRUM HEADS TO READ CIRCUIT PLUGGABLE UNIT PINS.
M REFER TO LOGIC DWG 1.7.1-2.

DIGITAL DISPLAY OD CONTROLS & READ CIRCUITS

EC 72659
3117918


COMPUTER B
COMPUTER A
READ WRITE RESET
COMPUTER DISCONNECT
START READ
IC OTHER
IC OWN TEST
IC OTHER SYNC
IC OTHER READ
IC OTHER COMPARE
OD-1 STEP APC
OD-1X
OD-3
READOUT IC APC
RESET IC APC
MANUAL TEST READ IC OWN
NOT MANUAL TEST
NO COMPARE
COMPARE
21FL 77096
21FC 77167
21FE 77147
21FK 77151
21FM 77111
21IRN 77126
21IRM 77156
21IRP 77152
22AE 77116
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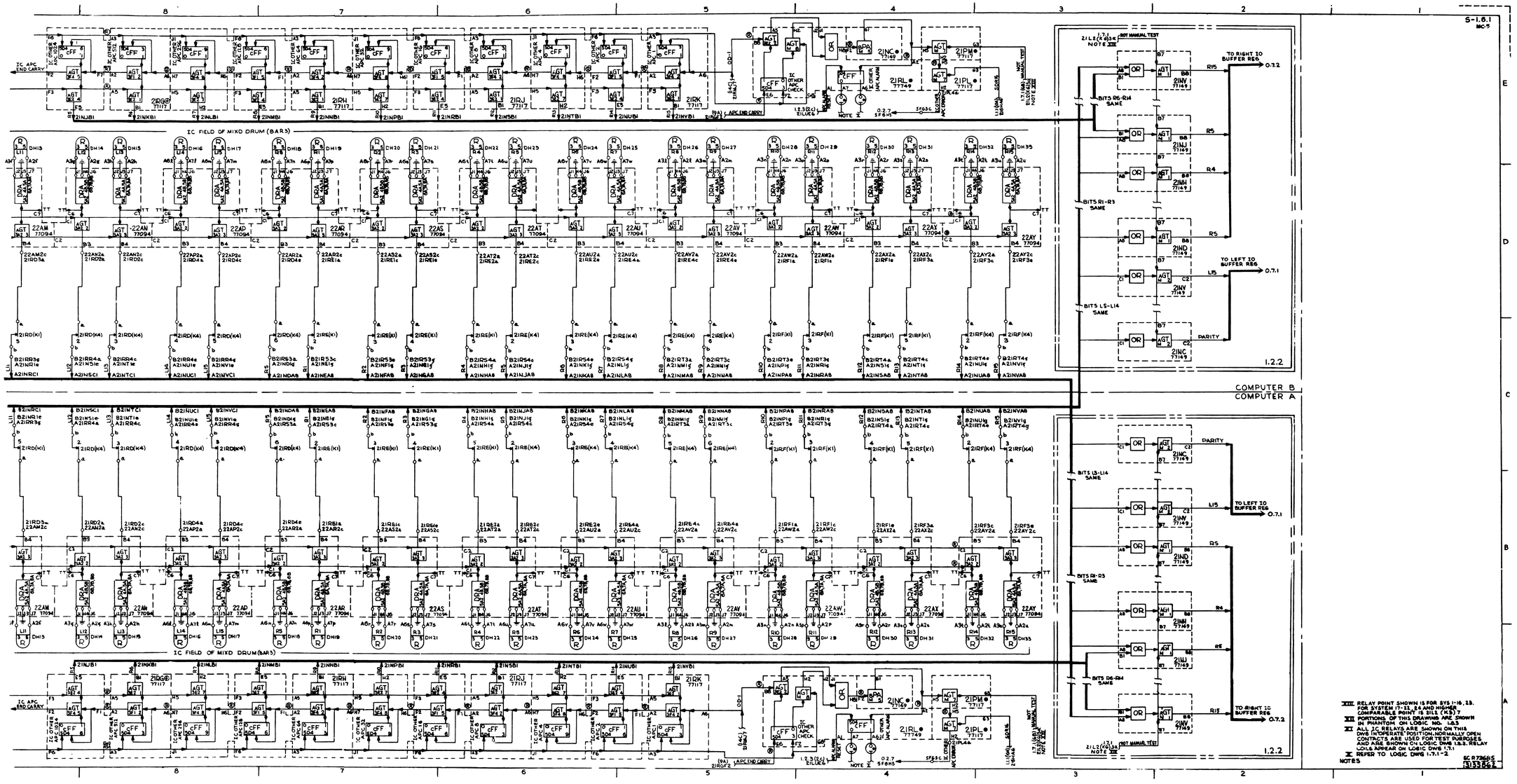
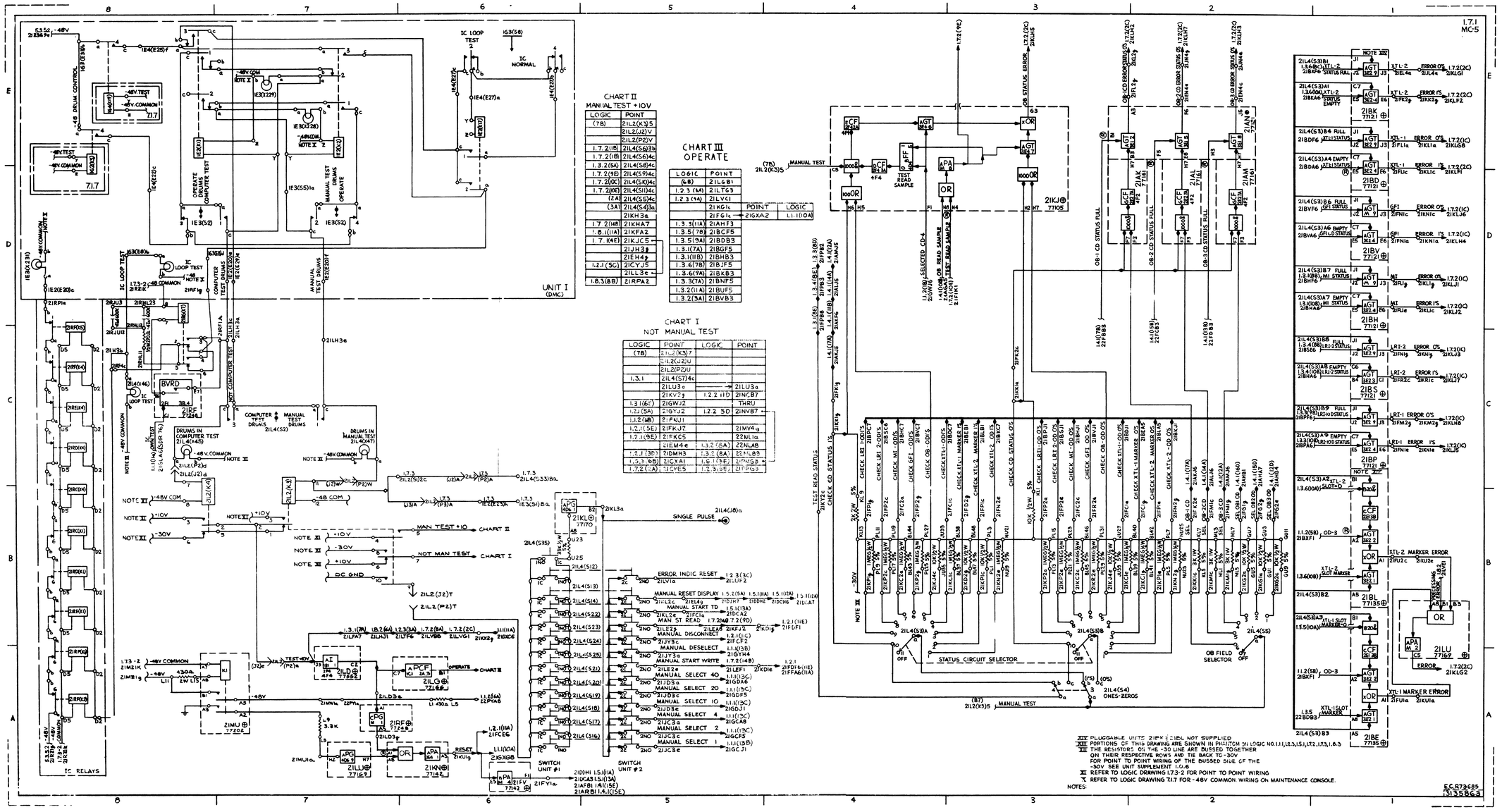
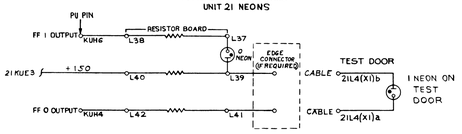
22AJ 77094
22AK 77094
22AL 77094
22AM 77094



OD IC FIELD COMP A&B


UNIT I (DMC)
CHART II MANUAL TEST +10V
CHART III OPERATE
CHART I NOT MANUAL TEST
IC RELAYS
SWITCH UNIT #1
SWITCH UNIT #2
STATUS CIRCUIT SELECTOR
OB FIELD SELECTOR
MAIN DRUMS MANUAL CONTROLS
NOTES:
XXX PLUGGABLE UNITS 21PK & 21DL NOT SUPPLIED
XXX PORTIONS OF THIS DRAWING ARE SHOWN IN PAIRTOM 21 LOGIC NO.1.11,1.13,1.15,1.17.2,1.17.3,1.8.3
III THE RESISTORS ON THE -30 LINE ARE BUSSED TOGETHER ON THEIR RESPECTIVE ROWS AND TIE BACK TO -30V FOR POINT TO POINT WIRING OF THE BUSSED SIDE OF THE -30V SEE UNIT SUPPLEMENT 1.0.6
REFER TO LOGIC DRAWING 1.73-2 FOR POINT TO POINT WIRING
REFER TO LOGIC DRAWING 7.1.7 FOR -48V COMMON WIRING ON MAINTENANCE CONSOLE.
EC R73685
1335863

TYPICAL WIRING DRAWING
UNIT 21 NEONS



FF OUT	PU TERM	RES BOARD TERM RESISTOR	RES BOARD TERM O NEON	LOGIC & E.C.	NEON & TITLE
1	ACH1	U39	U37	U35	1.5.3	DD OD SYNC
+150	ACE3	U33	U35	EC4c	JC4c	21L4 (X88) b
0	ACH2	U43	U45	EC4f	JC4a	21L4 (X85) a
1	BCG3	U31	U29	U29	U27	1.3.5	XTL-1 OD WRITE REG FULL
+150	BCE3	U25	U27	EC3a	JC3g	21L4(X64) b
0	BCG2	U33	U35	EC3b	JC3h	21L4(X64) a
1	BGG3	U39	U37	U37	U35	1.3.1	MOD WRITE REG FULL
+150	BGE3	U33	U35	EG3c	JG3c	21L4(X65) b
0	BGG2	U41	U43	EG3f	JG3d	21L4(X65) a
1	BJG3	U39	U37	U37	U35	1.3.4	XTL-2 OD WRITE REG FULL
+150	BJE3	U33	U35	EJ3a	JJ3A	21L4(X63) b
0	BJG2	U43	U45	EJ3b	JJ3b	21L4(X63) a
1	BNG3	U37	U35	U35	U33	1.3.3	LRH OD WRITE REG FULL
+150	BNE3	U31	U33	EN3a	JN3a	21L4(X68) b
0	BNG2	U41	U43	EN3b	JN3b	21L4(X68) a
1	BRG3	U39	U37	U37	U35	1.3.4	LRH-2OD WRITE REG FULL
+150	BRE3	U33	U35	ER3a	JR3A	21L4(X67) b
0	BRG2	U41	U43	ER3b	JR3b	21L4(X67) a
1	BUG3	L39	L37	L37	L35	1.3.2	GFI OD WRITE REG FULL
+150	BUE3	L33	L35	ET3a	JU3A	21L4(X66) b
0	BUG2	L41	L43	ET3f	JU3b	21L4(X66) a
1	DCH4	U39	U37	U37	U35	1.5.1	TD OD SELECTED
+150	DCE3	U33	U35	EC4a	JC4a	21L4(X87) b
0	DCH3	U41	U43	EC4g	JC4b	21L4(X87) a
1	DKF2	L37	L39	L39	L41	1.5.1	RD OD SELECTED
+150	DKE3	L43	L41	EK3a	JK3A	21L4(X86) b
0	DKF3	L45	L47	EK3b	JK3b	21L4(X86) a
1	FDG1	L39	L37	L37	L35	1.2.1	CD MODE
+150	FDE3	L33	L35	JD3g	21L4(X80) b
0	FDG2	L41	L43	JD3h	21L4(X80) a
1	FEA2	U5	U7	U7	U9	1.2.1	CD READ
+150	FEE3	U11	U9	JE3a	21L4(X102) b
0	FEA3	U1	U3	JE3b	21L4(X102) a
1	FEB2	U17	U19	U19	U21	1.2.1	CD WRITE
+150	FEE3	U23	U21	JE3c	21L4(X103) b
0	FEB3	U13	U15	JE3d	21L4(X103) a
1	FFB4	L15	L17	L17	L19	1.2.1	CD WRITE REG FULL
+150	FFE3	L21	L19	JF3a	21L4(X62) b
0	FFB3	L7	L9	JF3b	21L4(X62) a
1	FGB4	U13	U15	U15	U17	1.2.1	CD ADDRESS COMPARE
+150	FGE3	U19	U17	JF3e	21L4(X81) b
0	FGB3	U9	U11	JF3f	21L4(X81) a
1	FGH7	U39	U37	U37	U35	1.2.1	CD MASTER SYNC
+150	FGE3	U33	U35	JG3A	21L4(X79) b
0	FGH6	U43	U41	JG3b	21L4(X79) a
1	GCA1	U10	U9	U9	U7	1.1.1	SELECTION REG 04
+150	GCE3	U8	U7	JC4e	21L4(X98) b
0	GCC1	U6	U5	JC4f	21L4(X98) a
1	GCC2	U30	U29	U29	U27	1.1.1	SELECTION REG 02
+150	GCE3	U28	U27	JC4g	21L4(X97) b
0	GCF7	U26	U25	JC4h	21L4(X97) a
1	GCH6	U46	U45	U45	U43	1.1.1	SELECTION REG 01
+150	GCE3	U44	U43	JE3e	21L4(X96) b
0	GCH7	U42	U41	JE3f	21L4(X96) a
1	GDA1	L10	L9	L9	L7	1.1.1	SELECTION REG 40
+150	GDE3	L8	L7	JD4a	21L4(X101) b
0	GDC1	L6	L5	JD4b	21L4(X101) a
1	GDC2	L30	L29	L29	L27	1.1.1	SELECTION REG 20
+150	GDE3	L28	L27	JD4c	21L4(X100) b
0	GDF7	L26	L25	JD4d	21L4(X100) a
1	GDH6	L46	L45	L45	L43	1.1.1	SELECTION REG 10
+150	GDE3	L44	L43	JD4e	21L4(X99) b
0	GDH7	L42	L41	JD4f	21L4(X99) a

FF OUT	PU TERM	RES BOARD TERM RESISTOR	RES BOARD TERM O NEON	LOGIC & E.C.	NEON & TITLE
1	KLB8	U3	U9	U9	U11	1.7.2	MANUAL TEST ERROR
+150	KLE3	U13	U11			21L4(X94) b
0	KLC2	U7	U5			21L4(X94) a
1	KPH6	L39	L37	L37	L35	1.7.2	PARITY
+150	KPE3	L33	L35			21L4(X17) b
0	KPH7	L43	L41			21L4(X17) a
1	KRA2	U14	U13	U13	U11	1.7.2	L5
+150	KRE3	U12	U11			21L4(X16) b
0	KRB1	U10	U9			21L4(X16) a
1	KRC1	U20	U19	U19	U17	1.7.2	L1
+150	KRE3	U18	U17			21L4(X15) b
0	KRB3	U16	U15			21L4(X15) a
1	KRH5	U30	U29	U29	U31	1.7.2	L2
+150	KRE3	U32	U31			21L4(X14) b
0	KRG2	U34	U33			21L4(X14) a
1	KRH6	U38	U37	U37	U39	1.7.2	L3
+150	KRE3	U40	U39			21L4(X13) b
0	KRH4	U42	U41			21L4(X13) a
1	KSA2	L14	L13	L13	L11	1.7.2	L4
+150	KSE3	L12	L11			21L4(X12) b
0	KSB1	L10	L9			21L4(X12) a
1	KSC1	L20	L19	L19	L17	1.7.2	L5
+150	KSE3	L18	L17			21L4(X11) b
0	KSB3	L16	L15			21L4(X11) a
1	KSH5	L30	L29	L29	L31	1.7.2	L6
+150	KSE3	L32	L31			21L4(X10) b
0	KSG2	L34	L33			21L4(X10) a
1	KSH6	L38	L37	L37	L39	1.7.2	L7
+150	KSE3	L40	L39			21L4(X9) b
0	KSH4	L42	L41			21L4(X9) a
1	KTA2	U12	U11	U11	U9	1.7.2	L8
+150	KTE3	U10	U9			21L4(X8) b
0	KTB1	U8	U7			21L4(X8) a
1	KTC1	U18	U17	U17	U15	1.7.2	L9
+150	KTE3	U16	U15			21L4(X7) b
0	KTB3	U14	U13			21L4(X7) a
1	KTH5	U30	U29	U29	U31	1.7.2	L10
+150	KTE3	U32	U31			21L4(X6) b
0	KTG2	U34	U33			21L4(X6) a
1	KTH6	U38	U37	U37	U39	1.7.2	L11
+150	KTE3	U40	U39			21L4(X5) b
0	KTH4	U42	U41			21L4(X5) a
1	KUA2	L14	L13	L13	L11	1.7.2	L12
+150	KUE3	L12	L11			21L4(X4) b
0	KUB1	L10	L9			21L4(X4) a
1	KUC1	L20	L19	L19	L17	1.7.2	L13
+150	KUE3	L18	L17			21L4(X3) b
0	KUB3	L16	L15			21L4(X3) a
1	KUH5	L30	L29	L29	L31	1.7.2	L14
+150	KUE3	L32	L31			21L4(X2) b
0	KUG2	L34	L33			21L4(X2) a
1	KUH6	L38	L37	L37	L39	1.7.2	L15
+150	KUE3	L40	L39			21L4(X1) b
0	KUH4	L42	L41			21L4(X1) a
1	KVA2	U14	U13	U13	U11	1.7.2	R5
+150	KVE3	U12	U11			21L4(X33) b
0	KVB1	U10	U9			21L4(X33) a
1	KVC1	U20	U19	U19	U17	1.7.2	R1
+150	KVE3	U18	U17			21L4(X32) b
0	KVB3	U16	U15			21L4(X32) a
1	KVH5	U30	U29	U29	U31	1.7.2	R2
+150	KVE3	U32	U31			21L4(X31) b
0	KVG2	U34	U33			21L4(X31) a

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1	KVH6	U38	U37	U37	U39	1.7.2	R3
+150	KVE3	U40	U39			21L4(X30) b
0	KVH4	U42	U41			21L4(X30) a
1	KWA2	L14	L13	L13	L11	1.7.2	R4
+150	KWE3	L12	L11			21L4(X29) b
0	KWB1	L10	L9			21L4(X29) a
1	KWC1	L20	L19	L19	L17	1.7.2	R5
+150	KWE3	L18	L17			21L4(X28) b
0	KWB3	L16	L15			21L4(X28) a
1	KWH5	L30	L29	L29	L31	1.7.2	R6
+150	KWE3	L32	L31			21L4(X27) b
0	KWG2	L34	L33			21L4(X27) a
1	KWH6	L38	L37	L37	L39	1.7.2	R7
+150	KWE3	L40	L39			21L4(X26) b
0	KWH4	L42	L41			21L4(X26) a
1	KXA2	U12	U11	U11	U9	1.7.2	R8
+150	KXE3	U10	U9			21L4(X25) b
0	KXB1	U8	U7			21L4(X25) a
1	KXC1	U18	U17	U17	U15	1.7.2	R9
+150	KXE3	U16	U15			21L4(X24) b
0	KXB3	U14	U13			21L4(X24) a
1	KXH5	U30	U29	U29	U31	1.7.2	R10
+150	KXE3	U32	U31			21L4(X23) b
0	KXG2	U34	U33			21L4(X23) a
1	KXH6	U38	U37	U37	U39	1.7.2	R11
+150	KXE3	U40	U39			21L4(X22) b
0	KXH4	U42	U41			21L4(X22) a
1	KYA2	L14	L13	L13	L11	1.7.2	R12
+150	KYE3	L12	L11			21L4(X21) b
0	KYB1	L10	L9			21L4(X21) a
1	KYC1	L20	L19	L19	L17	1.7.2	R13
+150	KYE3	L18	L17			21L4(X20) b
0	KYB3	L16	L15			21L4(X20) a
1	KYH5	L30	L29	L29	L31	1.7.2	R14
+150	KYE3	L32	L31			21L4(X19) b
0	KYG2	L34	L33			21L4(X19) a
1	KYH6	L38	L37	L37	L39	1.7.2	R15
+150	KYE3	L40	L39			21L4(X18) b
0	KYH4	L42	L41			21L4(X18) a
1	LEA1	U8	U7	U7	U5	1.7.2	COMP. TEST READ
+150	LEE3	U6	U5			21L4(X77) b
0	LEC1	U4	U3			21L4(X77) a
1	LEC2	U16	U15	U15	U13	1.7.2	COMP. TEST WRITE
+150	LEE3	U14	U13			21L4(X78) b
0	LEF7	U12	U11			21L4(X78) a
1	LEH6	U38	U37	U37	U35	1.8.1	COMP. TEST SYNC
+150	LEF3	U36	U35			21L4(X76) b
0	LEH7	U34	U33			21L4(X76) a
1	LTA2	B2	U1	U1	U3	1.3.3	LRH OD FULL ALARM
+150	LTE3	U4	U3			21L4(X61) b
0	LTA3	U6	U5			21L4(X61) a
1	LTB8	U12	U11	U11	U13	1.3.4	LRI 2OD FULL ALARM
+150	LTE3	U14	U13			21L4(X60) b
0	LTC5	U16	U15			21L4(X60) a
1	LTF2	U20	U19	U19	U21	1.3.1	MOD FULL ALARM
+150	LTE3	U22	U21			21L4(X58) b
0	LTF3	U24	U23			21L4(X58) a
1	LTH1	U28	U27	U27	U29	1.3.5	XTL-1 OD FULL ALARM
+150	LTE3	U30	U29			21L4(X57) b
0	LTH2	U32	U31			21L4(X57) a
1	LTH7	U42	U41	U41	U39	1.3.6	XTL-2 OD FULL ALARM
+150	LTE3	U40	U39			21L4(X56) b
0	LTH6	U38	U37			21L4(X56) a

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1	LVH5	U43	U41	U41	U39	1.2.3	LOG/TEST APC ALARM
+150	LVE3	U37	U39			21L4(X48) b
0	LVH6	U47	U45			21L4(X48) a
1	LWA6	L10	L9	L9	L7	1.7.2	TEST APC 1
+150	LWE3	L8	L7			21L4(X34) b
0	LWA5	L6	L5			21L4(X34) a
1	LWC5	L18	L17	L17	L15	1.7.2	TEST APC 2
+150	LWE3	L16	L15			21L4(X35) b
0	LWB4	L14	L13			21L4(X35) a
1	LWF3	L30	L29	L29	L27	1.7.2	TEST APC 4
+150	LWE3	L28	L27			21L4(X36) b
0	LWF2	L26	L25			21L4(X36) a
1	LWH7	L32	L31	L31	L33	1.7.2	TEST APC 8
+150	LWE3	L34	L33			21L4(X37) b
0	LWG2	L36	L35			21L4(X37) a
1	LXA6	U10	U9	U9	U7	1.7.2	TEST APC 16
+150	LXE3	U8	U7			21L4(X38) b
0	LXA5	U6	U5			21L4(X38) a
1	LXC5	U18	U17	U17	U15	1.7.2	TEST APC 32
+150	LXE3	U16	U15			21L4(X39) b
0	LXB4	U14	U13			21L4(X39) a
1	LXF3	U30	U29	U29	U27	1.7.2	TEST APC 64
+150	LXE3	U28	U27			21L4(X40) b
0	LXF2	U26	U25			21L4(X40) a
1	LXH7	U32	U31	U31	U33	1.7.2	TEST APC 128
+150	LXE3	U34	U33			21L4(X41) b,
0	LXG2	U36	U35			21L4(X41) a
1	LYA6	L10	L9	L9	L7	1.7.2	TEST APC 256
+150	LYE3	L8	L7			21L4(X42) b
0	LYA5	L6	L5			21L4(X42) a
1	LYC5	L18	L17	L17	L15	1.7.2	TEST APC 512
+150	LYE3	L16	L15			21L4(X43) b
0	LYB4	L14	L13			21L4(X43) a
1	LYF3	L24	L23	L23	L21	1.7.2	TEST APC 1024
+150	LYE3	L22	L21			21L4(X44) b
0	LYF2	L20	L19			21L4(X44) a
1	MUH4	L39	L37	L37	L35	1.3.2	GFI OD FULL ALARM
+150	MUE3	L33	L35			MX1a	21L4(X59) b
0	MUJ5	L43	L45			MX1b	21L4(X59) a
1	RLE8	U23	U21	U21	U19	1.2.3	MXD APC ERROR
+150	RLE3	U17	U19			MP2e	21L4(X52) b
0	RLF1	U27	U25			MP2f	21L4(X52) a
1	PTE8	U23	U21	U21	U19	1.2.3	AM-A APC ERROR
+150	PTE3	U17	U19			MW2a	21L4(X53) b
0	PTF1	U27	U25			MW2b	21L4(X53) a
1	PUA6	L5	L7	L7	L9	1.2.3	AM-B APC ERROR
+150	PUE3	L11	L9			MW2c	21L4(X49) b
0	PUA7	L1	L3			MW2d	21L4(X49) a
1	PUE8	L27	L25	L25	L23	1.2.3	TD APC ERROR
+150	PUE3	L21	L23			MW2e	21L4(X50) b
0	PUF1	L31	L29			MW2f	21L4(X50) a
1	PVE8	U21	U19	U19	U17	1.2.3	RD APC ERROR
+150	PVE3	U15	U17			MW2g	21L4(X51) b
0	PVF1	U27	U25			MW2h	21L4(X51) a
1	RLA6	U7	U9	U9	U11	1.6.1	IC OTHER APC ALARM
+150	RLE3	U13	U11			ML2a	21L4(X54) b
0	RLA7	U3	U5			ML2b	21L4(X54) a

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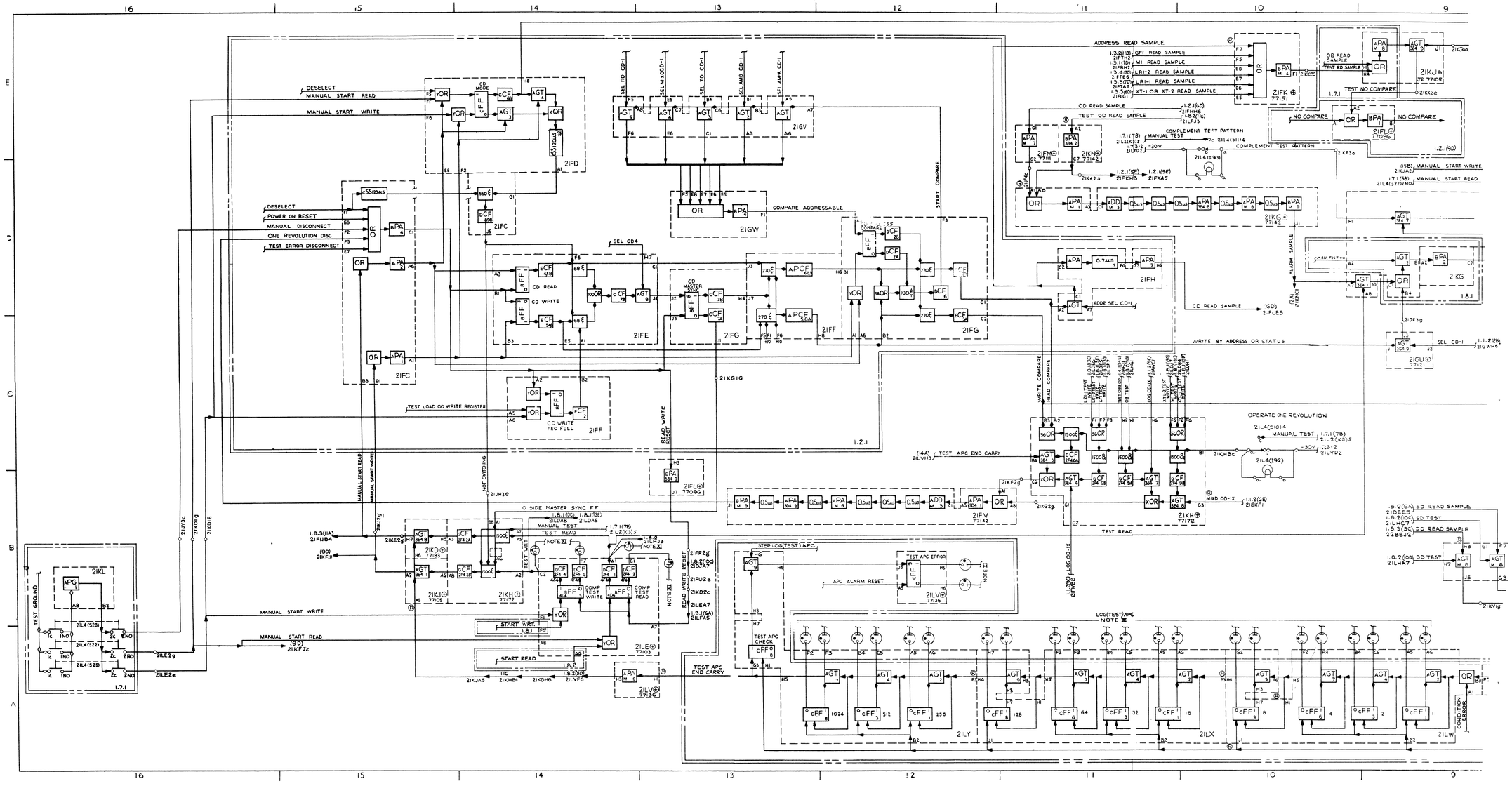
MAIN DRUMS TEST PANEL NEON WIRING


DESELECT
MANUAL START READ
MANUAL START WRITE
DESELECT
POWER ON RESET
MANUAL DISCONNECT
ONE REVOLUTION DISC
TEST ERROR DISCONNECT
21IFD
21IFC
21IGW
21IGV
21IFE
21IFG
21IFF
21IKG1G
TEST LOAD OD WRITE REGISTER
CD WRITE REG FULL
READ WRITE RESET
START COMPARE
COMPARE ADDRESSABLE
SEL RD CD-1
SEL MIX(OD)-1
SEL TD CD-1
SEL AMB CD-1
SEL AMA CD-1
SEL CD4
CD READ
CD WRITE
CD MODE
ADDRESS READ SAMPLE
GFI READ SAMPLE
MI READ SAMPLE
LRI-2 READ SAMPLE
LRI-1 READ SAMPLE
XT-1 OR XT-2 READ SAMPLE
21IFK
CD READ SAMPLE
TEST OD READ SAMPLE
21IKN
21IFM
21IFH
ADDR SEL CD-1
OB READ SAMPLE
TEST RD SAMPLE
TEST NO COMPARE
NO COMPARE
21IFL
21IKJ
21IKK
COMPLEMENT TEST PATTERN
MANUAL TEST
21L4(193)
21L4(51)14
21IKH
21IKG
21IGU
WRITE BY ADDRESS OR STATUS
SEL CD-1
ALARM SAMPLE
MAN TEST RD
2 KG
OPERATE ONE REVOLUTION
MANUAL TEST
21L4(192)
TEST APC END CARRY
MIXED OD-IX
TEST READ
WRITE COMPARE
READ COMPARE
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21MZ
21N
21N1
21N2
21N3
21N4
21N5
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21NA
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21NE
21NF
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21NM
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21NR
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21RC
21RD
21RE
21RF
21RG
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21RJ
21RK
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21RM
21RN
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21RR
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21SE
21SF
21SG
21SH
21SJ
21SK
21SL
21SM
21SN
21SP
21SR
21SS
21ST
21SU
21SV
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21TC
21TD
21TE
21TF
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21TJ
21TK
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21TR
21TS
21TT
21TU
21TV
21TW
21TX
21TY
21TZ
21U
21U1
21U2
21U3
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21U5
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21U9
21UA
21UB
21UC
21UD
21UE
21UF
21UG
21UH
21UJ
21UK
21UL
21UM
21UN
21UP
21UR
21US
21UT
21UU
21UV
21UW
21UX
21UY
21UZ
21V
21V1
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21XN
21XP
21XR
21XS
21XT
21XU
21XV
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21XY
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21Y1
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21YA
21YB
21YC
21YD
21YE
21YF
21YG
21YH
21YJ
21YK
21YL
21YM
21YN
21YP
21YR
21YS
21YT
21YU
21YV
21YW
21YX
21YY
21YZ
21Z
21Z1
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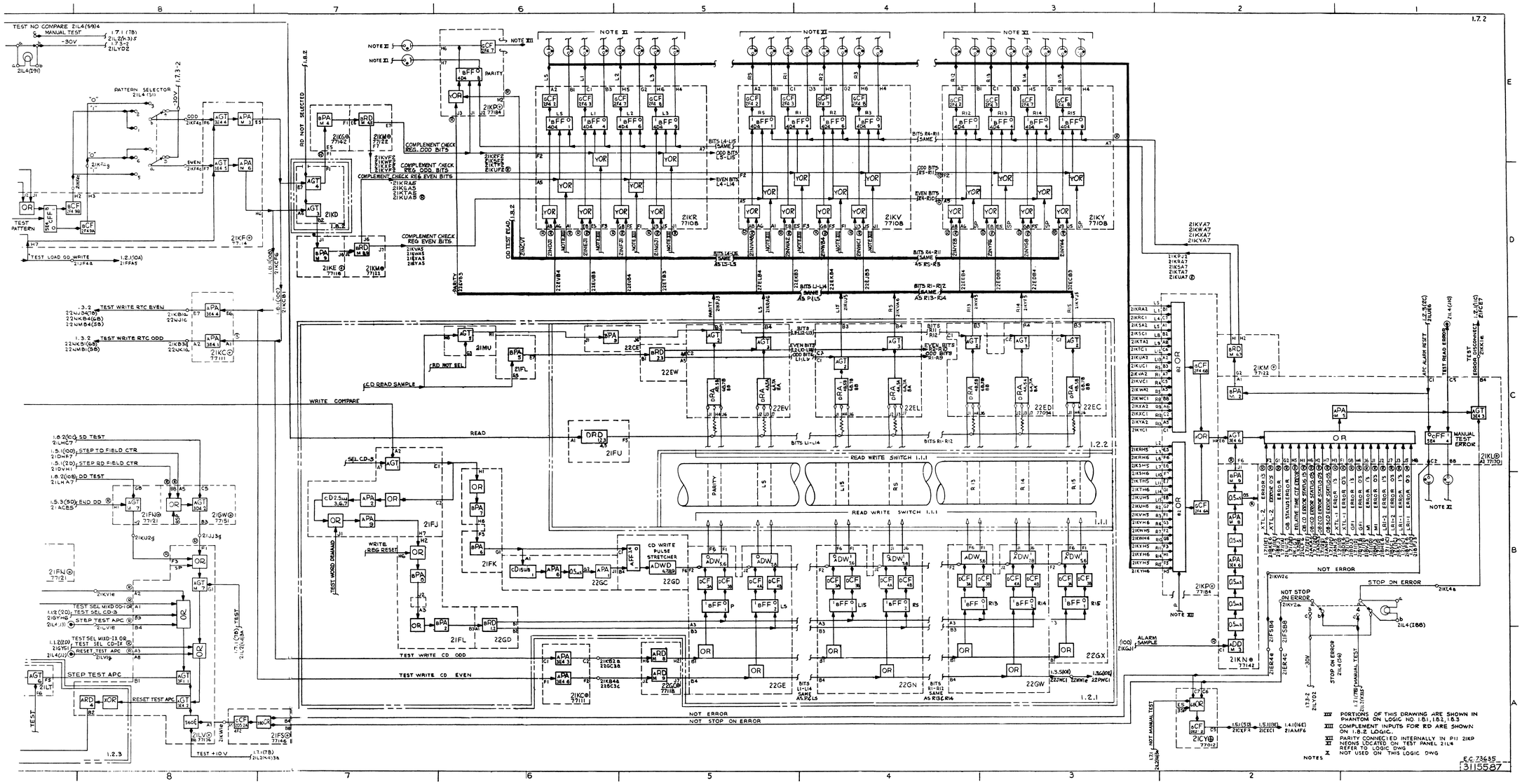
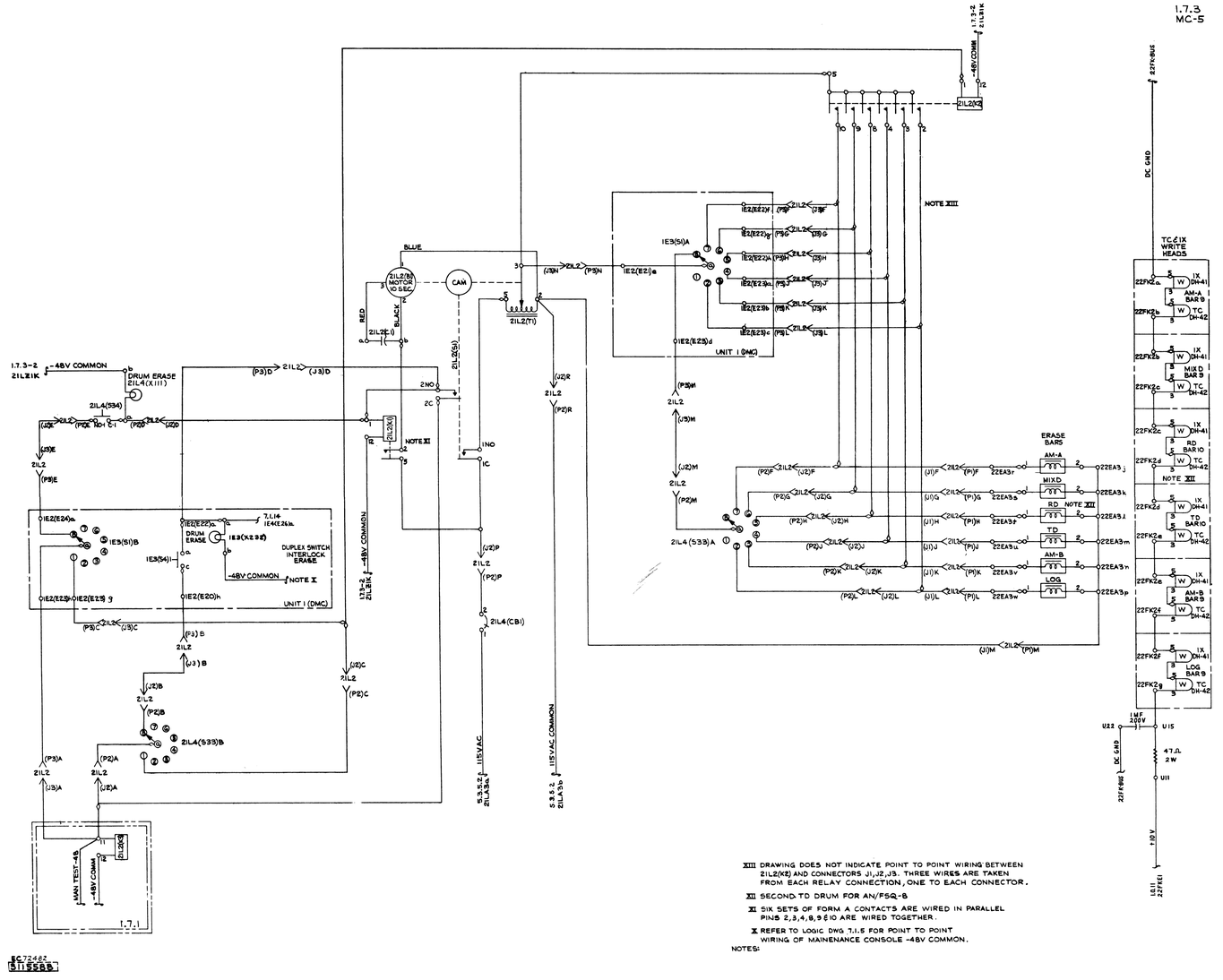
21Z3
21Z4
21Z5
21Z6
21Z7
21Z8
21Z9
21ZA
21ZB
21ZC
21ZD
21ZE
21ZF
21ZG
21ZH
21ZJ
21ZK
21ZL
21ZM
21ZN
21ZP
21ZR
21ZS
21ZT
21ZU
21ZV
21ZW
21ZX
21ZY
21ZZ
TEST GROUND
MANUAL START READ
MANUAL START WRITE
START WRT.
START READ
TEST APC ERROR
APC ALARM RESET
TEST APC CHECK
STEP LOG(TEST) APC
LOG(TEST)APC
NOTE XI
CONDITION ERROR
8.2(GA) SD READ SAMPLE
21DBES
8.2(GC) SD TEST
21LHC7
5.3(SC) DD READ SAMPLE
22BEJ2
8.2(GB) DD TEST
21LHA7
21KVIg


TEST NO COMPARE 21L4(59)4
MANUAL TEST
-30V
21L4(39)
PATTERN SELECTOR 21L4(51)
"0"
"1"
ODD 21KF4(6)
EVEN 21KF4(8)
TEST PATTERN
TEST LOAD OD WRITE
21JFA4
21FFA5
TEST WRITE RTC EVEN
22NJB4(6B)
22NKB4(6B)
22NMB4(5B)
TEST WRITE RTC ODD
22NKB1(6B)
22NJB1(6B)
22NMB1(5B)
21KB1a
21KB1d
21KC
77111
21KE
77116
21KM
77122
21KP
77184
21KN
77142
21KL
77170
21KY
77102
21IMU
21IFL
21IFJ
21IFK
21IFN
77121
21IFS
77146
21IFU
22CE
22EW
22EV
22EL
22ED
22EC
22GC
22GD
22GE
22GN
22GW
22GX
22GG
22GH
22GJ
22GK
22GL
22GM
21KR
77108
21KV
77108
21KY
77108
21KD
77122
21KF
77114
21KE
77116
21KM
77122
21KP
77184
21KN
77142
21KL
77170
21KY
77102
READ NOT SELECTED
COMPLEMENT CHECK REG. ODD BITS
COMPLEMENT CHECK REG. EVEN BITS
CD TEST READ
CD READ SAMPLE
WRITE COMPARE
READ
SEL CD-9
WRITE REG RESET
TEST WORD DEMAND
TEST WRITE CD ODD
TEST WRITE CD EVEN
CD WRITE PULSE STRETCHER
READ WRITE SWITCH 1.1.1
READ WRITE SWITCH 1.1.1
NOT ERROR
NOT STOP ON ERROR
STOP ON ERROR
ALARM SAMPLE
TEST MANUAL TEST
STEP TEST APC
RESET TEST APC
TEST SEL MIXED OD-10
TEST SEL CD-9
TEST SEL MIXED-IX OR
TEST SEL CD-IX
TEST +10 V
-30V
MAIN DRUM MANUAL READ-WRITE CONTROLS
NOTES
XIII PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM ON LOGIC NO. 1.8.1, 1.8.2, 1.8.3
XIII COMPLEMENT INPUTS FOR RD ARE SHOWN ON 1.8.2 LOGIC.
XII PARITY CONNECTED INTERNALLY IN P11 21KP NEONS LOCATED ON TEST PANEL 21L4
REFER TO LOGIC DWG
X NOT USED ON THIS LOGIC DWG
E.C. 73685
3115587

23B



XIII DRAWING DOES NOT INDICATE POINT TO POINT WIRING BETWEEN 21L2(K2) AND CONNECTORS J1, J2, J3. THREE WIRES ARE TAKEN FROM EACH RELAY CONNECTION, ONE TO EACH CONNECTOR.

XII SECOND TD DRUM FOR AN/FSQ-8

XI SIX SETS OF FORM A CONTACTS ARE WIRED IN PARALLEL PINS 2,3,4,8,9 & 10 ARE WIRED TOGETHER.

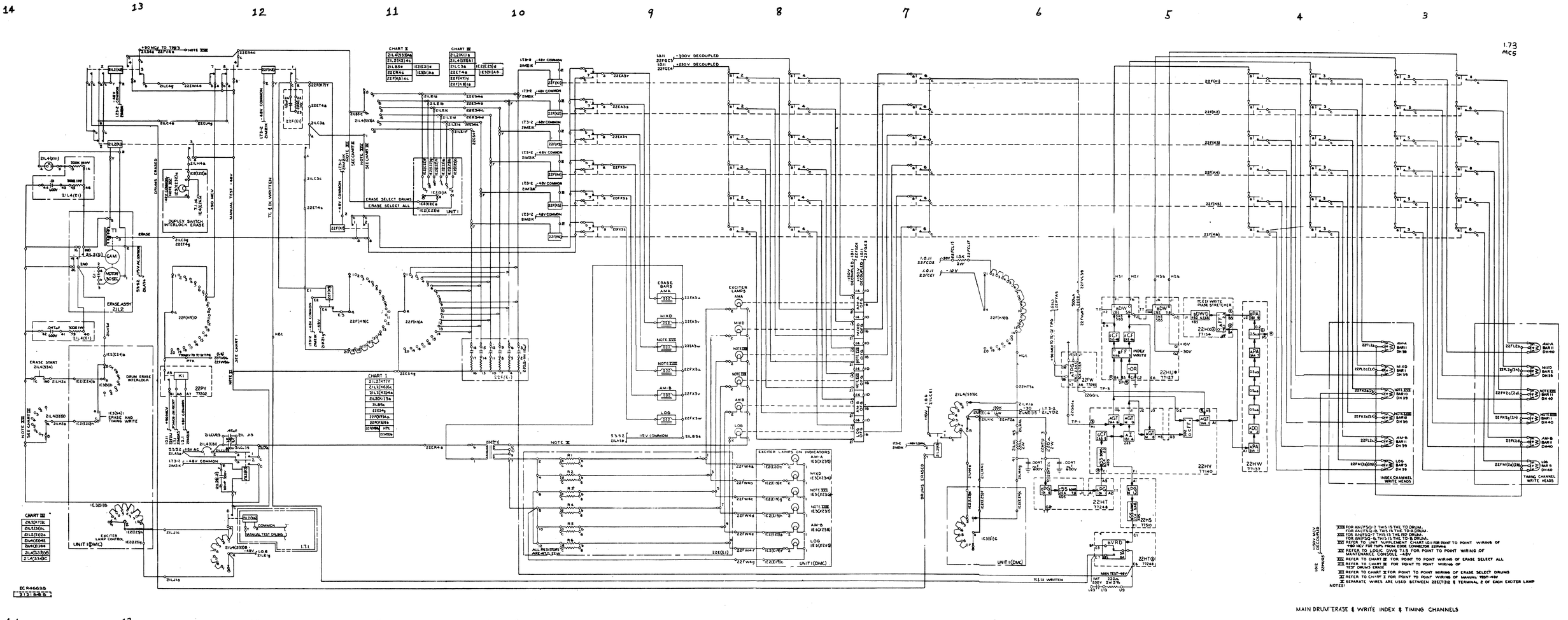
X REFER TO LOGIC DWG 7.1.5 FOR POINT TO POINT WIRING OF MAINENANCE CONSOLE -48V COMMON.

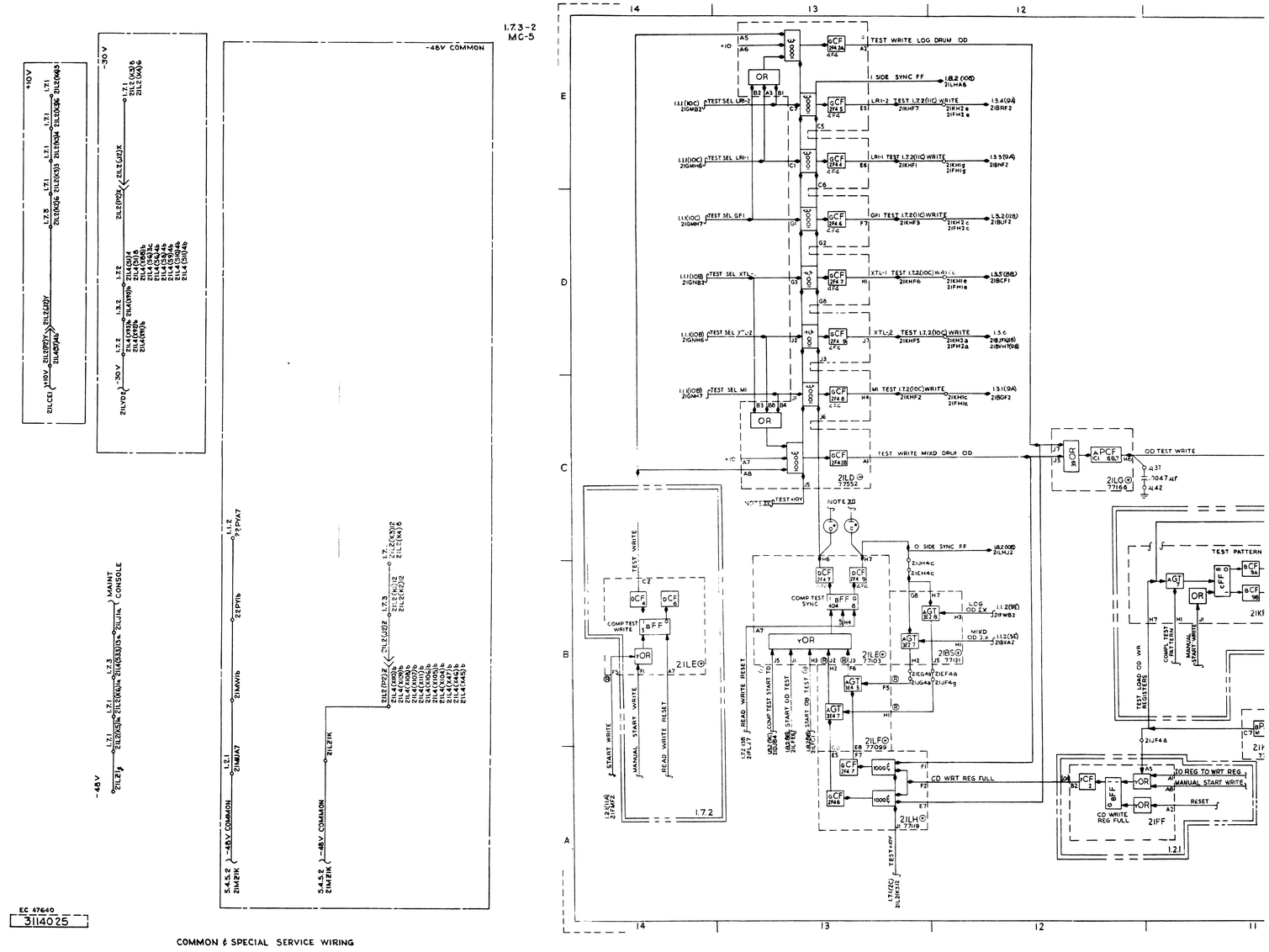
NOTES:

SC 72462
5115585

4 3 2 1

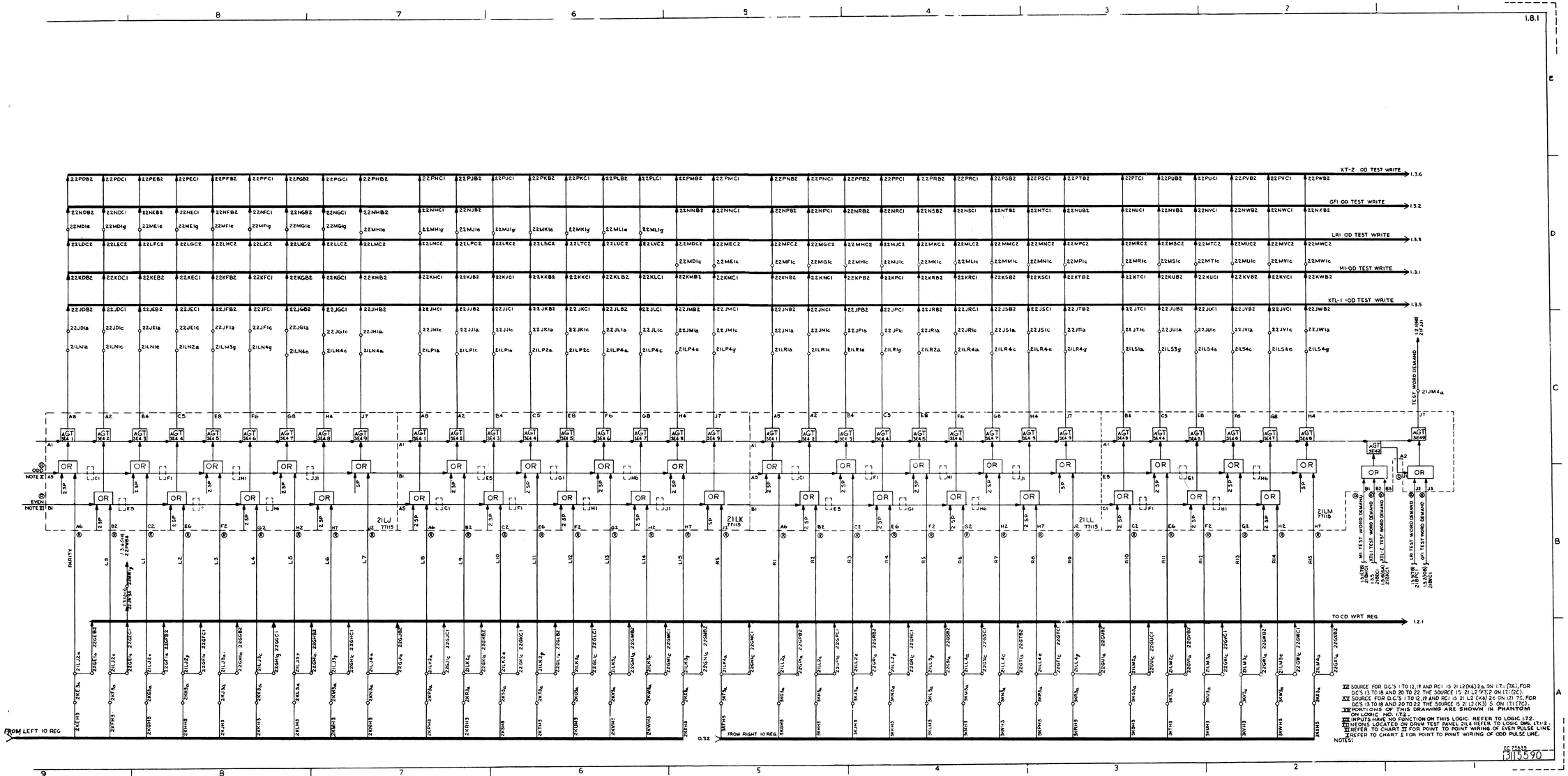
E D C B A

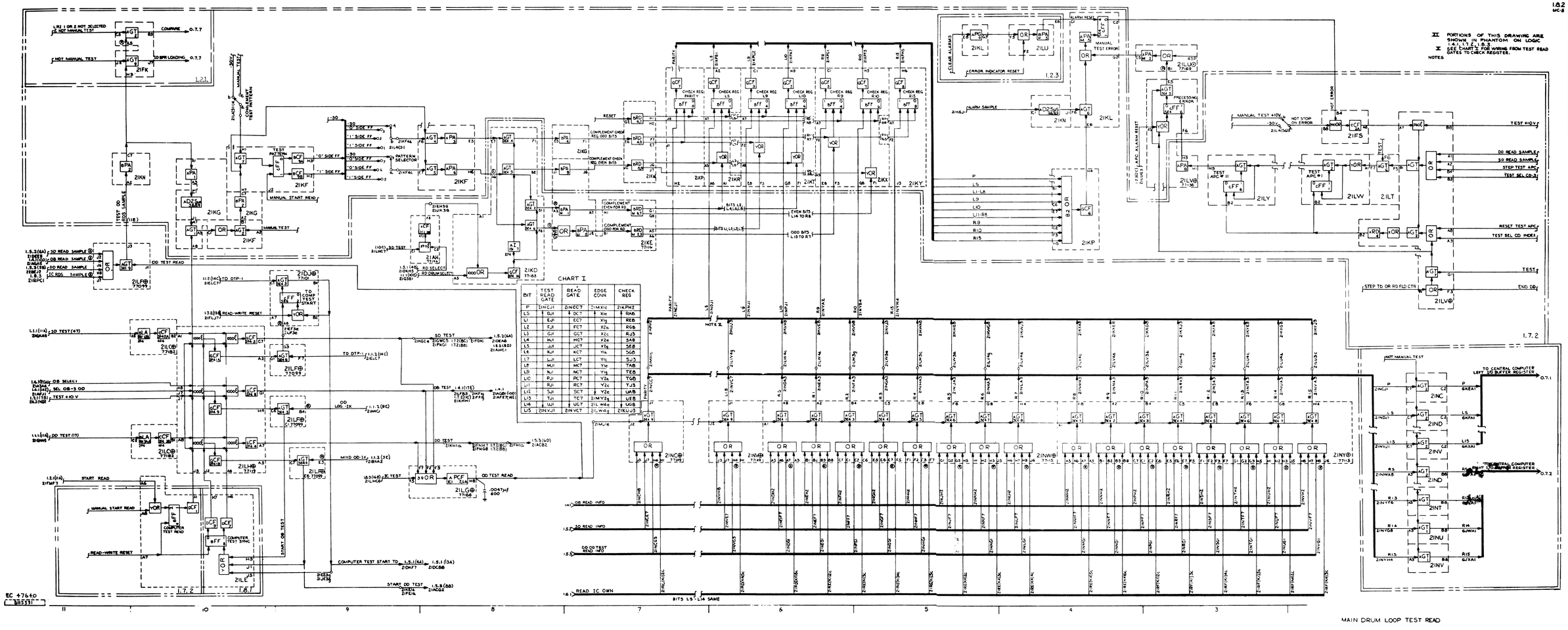

14 13 12 11 10 9 8 7 6 5 4 3
1.73 MC6
+90 MCV TO TB13
+48V COMMON
DRUMS ERASED
MANUAL TEST -48V
TC E.W. WRITTEN
ERASE
DUPLEX SWITCH INTERLOCK ERASE
ERASE ASSY 21L2
ERASE START 21L4(334)
DRUM ERASE INTERLOCK
ERASE AND TIMING WRITE
EXCITER LAMP CONTROL
UNIT I(DMC)
ERASE SELECT DRUMS
ERASE SELECT ALL
UNIT I
CHART I
CHART II
CHART III
NOTE X
ERASE BARS
MIXED
NOTE XXX
NOTE XXX
AM-B
LOG
EXCITER LAMPS
EXCITER LAMPS ON INDICATORS
AM-A IE3(X29)
MIXED IE3(X34)
NOT XXX IE3(X33)
NOT XXX IE3(X32)
AM-B IE3(X28)
LOG IE3(X25)
+300V DECOUPLED
+250V DECOUPLED
I.O.II 22FCE1
+10V
+30V
INDEX WRITE
22HU
22HV
22HW
22HX
22HT
22H5
22HT@
TC E.W. WRITE PULSE STRETCHER
MAIN TEST -48V
INDEX CHANNEL WRITE HEADS
TIMING CHANNEL WRITE HEADS
XXX FOR AN/FSQ-7 THIS IS THE TD DRUM. FOR AN/FSQ-8 THIS IS THE TD-A DRUM.
XXX FOR AN/FSQ-7 THIS IS THE RD DRUM. FOR AN/FSQ-8 THIS IS THE TD-B DRUM.
XXX REFER TO UNIT SUPPLEMENT CHART I.O.II FOR POINT TO POINT WIRING OF +90 MCV TO 1.7.5 FROM CONNECTOR E57M-S
XX REFER TO LOGIC DWG 1.7.5 FOR POINT TO POINT WIRING OF ERASE CONTROL -48V
XXX REFER TO CHART II FOR POINT TO POINT WIRING OF ERASE SELECT ALL
XXX REFER TO CHART III FOR POINT TO POINT WIRING OF TEST DRUM ERASE
XXX REFER TO CHART II FOR POINT TO POINT WIRING OF ERASE SELECT DRUMS
XX REFER TO CHART I FOR POINT TO POINT WIRING OF MANUAL TEST -48V
X SEPARATE WIRES ARE USED BETWEEN 22E(T10)& TERMINAL 2 OF EACH EXCITER LAMP
NOTES:
MAIN DRUM ERASE & WRITE INDEX & TIMING CHANNELS
25

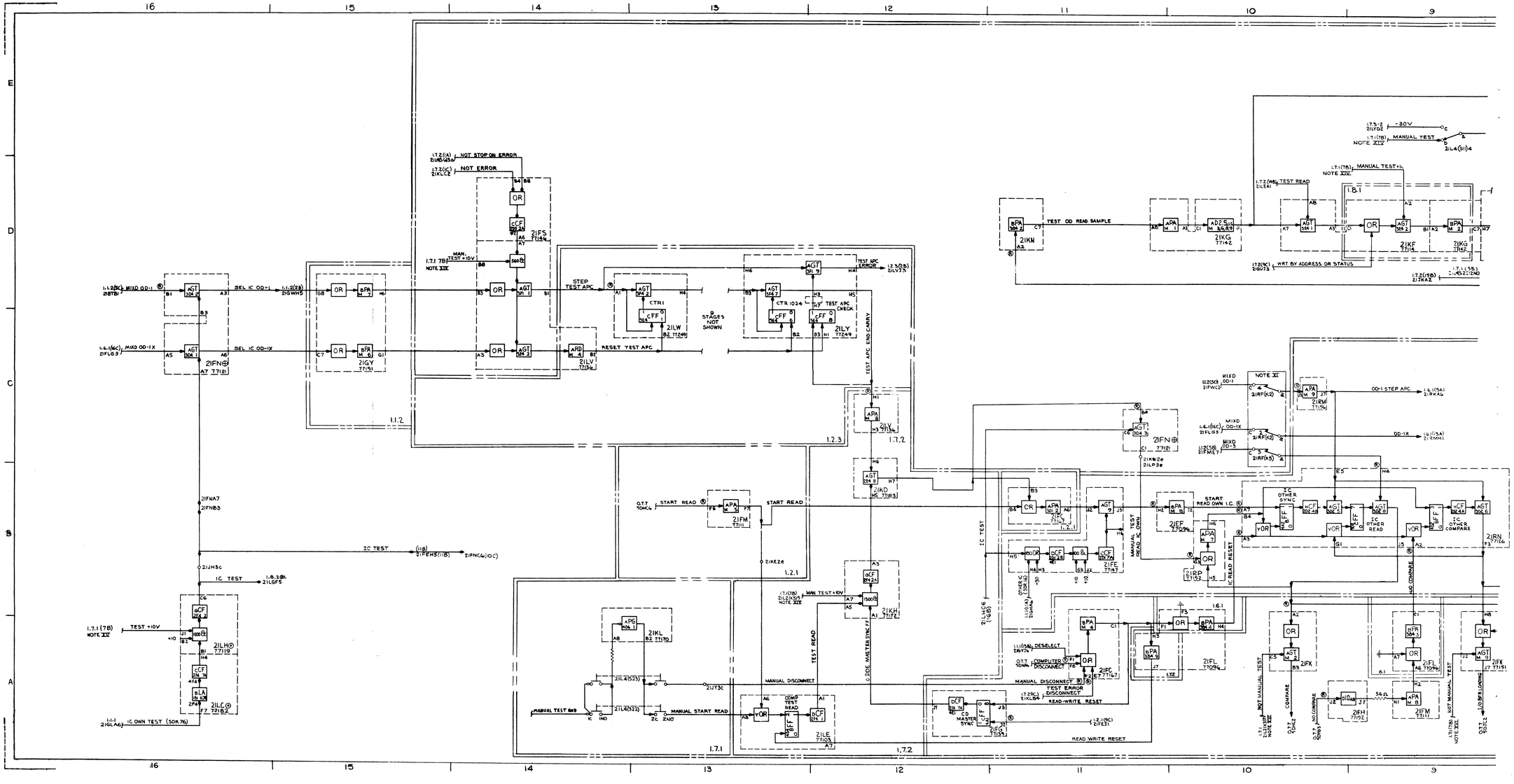


EC 67640
3114025

COMMON & SPECIAL SERVICE WIRING


XT-2 OD TEST WRITE
GFI OD TEST WRITE
LRI OD TEST WRITE
MI-OD TEST WRITE
XTL-1 -OD TEST WRITE
TEST WORD DEMAND
TO CD WRT REG.
FROM LEFT IO REG
FROM RIGHT IO REG.
21LJ 77115
21LK 77115
21LL 77115
21LM 77115
ODD
EVEN
PARITY
XI SOURCE FOR DCS 1 TO 12, 19 AND PCI 15 21 L2 (K6) 2a ON 171 (7A). FOR DCS 13 TO 18 AND 20 TO 22 THE SOURCE IS 21 L2 (K3) 2 ON 171 (2C).
XX SOURCE FOR DCS 1 TO 12, 19 AND PCI 15 21 L2 (K6) 2C ON 171 7C, FOR DCS 13 TO 18 AND 20 TO 22 THE SOURCE IS 21 L2 (K3) 3 ON 171 (7C).
XXI PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM ON LOGIC NO. 172.
XXII INPUTS HAVE NO FUNCTION ON THIS LOGIC. REFER TO LOGIC 172.
XXIII NEONS LOCATED ON DRUM TEST PANEL 21L4 REFER TO LOGIC DWG. 171-2.
XXIV REFER TO CHART II FOR POINT TO POINT WIRING OF EVEN PULSE LINE.
XXV REFER TO CHART I FOR POINT TO POINT WIRING OF ODD PULSE LINE.
NOTES:
EC 77633
3115590
MAIN DRUM LOOP TEST WRITE
1.8.1
26B


NOTES
I PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM ON LOGIC 1.4.1, 1.7.2, 1.8.3
II SEE CHART I FOR WIRING FROM TEST READ GATES TO CHECK REGISTER.
CHART I
BIT | TEST READ GATE | READ GATE | EDGE CONN | CHECK REG
P | 2INCJ1 | 2INCC7 | 2IMXIC | 2IKPH2
L5 | DJ1 | DC7 | X1E | RA8
L7 | EJ1 | EC7 | X1G | RE8
L2 | FJ1 | FC7 | X2A | RG8
L3 | GJ1 | GC7 | X2C | RJ8
L4 | HJ1 | HC7 | X2E | SA8
L5 | JJ1 | JC7 | X2A | SE8
L6 | KJ1 | KC7 | Y1A | SG8
L7 | LJ1 | LC7 | Y1C | SJ8
L8 | MJ1 | MC7 | Y1E | TA8
L9 | NJ1 | NC7 | Y1G | TE8
L10 | PJ1 | PC7 | Y2A | TG8
L11 | RJ1 | RC7 | Y2C | TJ8
L12 | SJ1 | SC7 | Y2E | UA8
L13 | TJ1 | TC7 | 2IMY2G | UE8
L14 | UJ1 | UC7 | 2IL M46 | UG8
L15 | 2INVJ1 | 2INVC7 | 2ILM46 | 2IKVJ5
BITS L5 - L14 SAME
MAIN DRUM LOOP TEST READ
EC 47640
MC-8
27


16
15
14
13
12
11
10
9
E
D
C
B
A
NOT STOP ON ERROR
NOT ERROR
MAN. TEST +10V
NOTE XIV
MIXED OD-1
MIXED OD-1X
SEL IC OD-1
SEL IC OD-1X
STEP TEST APC
RESET TEST APC
CTR1
CTR 1024
TEST APC CHECK
TEST APC ERROR
TEST APC END CARRY
8 STAGES NOT SHOWN
START READ
IC TEST
TEST +10V
IC OWN TEST (SDR76)
MANUAL START READ
MANUAL DISCONNECT
TEST READ
COMP TEST READ
TEST OD READ SAMPLE
MANUAL TEST
MANUAL TEST +10
NOTE XIV
TEST READ
WRT BY ADDRESS OR STATUS
-30V
MANUAL TEST
NOTE XIV
OD-1 STEP APC
OD-1X
START READ OWN I.C.
IC OTHER SYNC
IC OTHER READ
IC OTHER COMPARE
OTHER IC
COMPUTER DISCONNECT
TEST ERROR DISCONNECT
READ-WRITE RESET
CD MASTER SYNC
NOT MANUAL TEST
COMPARE
NOT COMPARE
I/O BPA LOADING
NOT MANUAL TEST
NOTE XIII
21IKN
21IKG 77142
21IKF 77114
21IKG 77142
21IFN 77121
21IFM 77111
21ILV 77134
21IKD 77103
21IKH 77172
21IKL 77170
21ILH 77119
21ILC 77182
21IFS 77134
21ILW 77249
21ILY 77249
21IGY 77151
21IRM 77156
21IRN 77126
21IFE 77147
21IEF 77096
21IRD 77152
21IFC 77147
21IFL 77096
21IFX
21IFL 77096
21IFH 77192
21IFM 77111
21IFK 77151
1.8.1
1.7.2
1.2.3
1.2.1
1.7.1
1.6.1
1.1.2
1.7.2
1.2.1
1.7.1
1.8.2
1.6.1
1.7.1

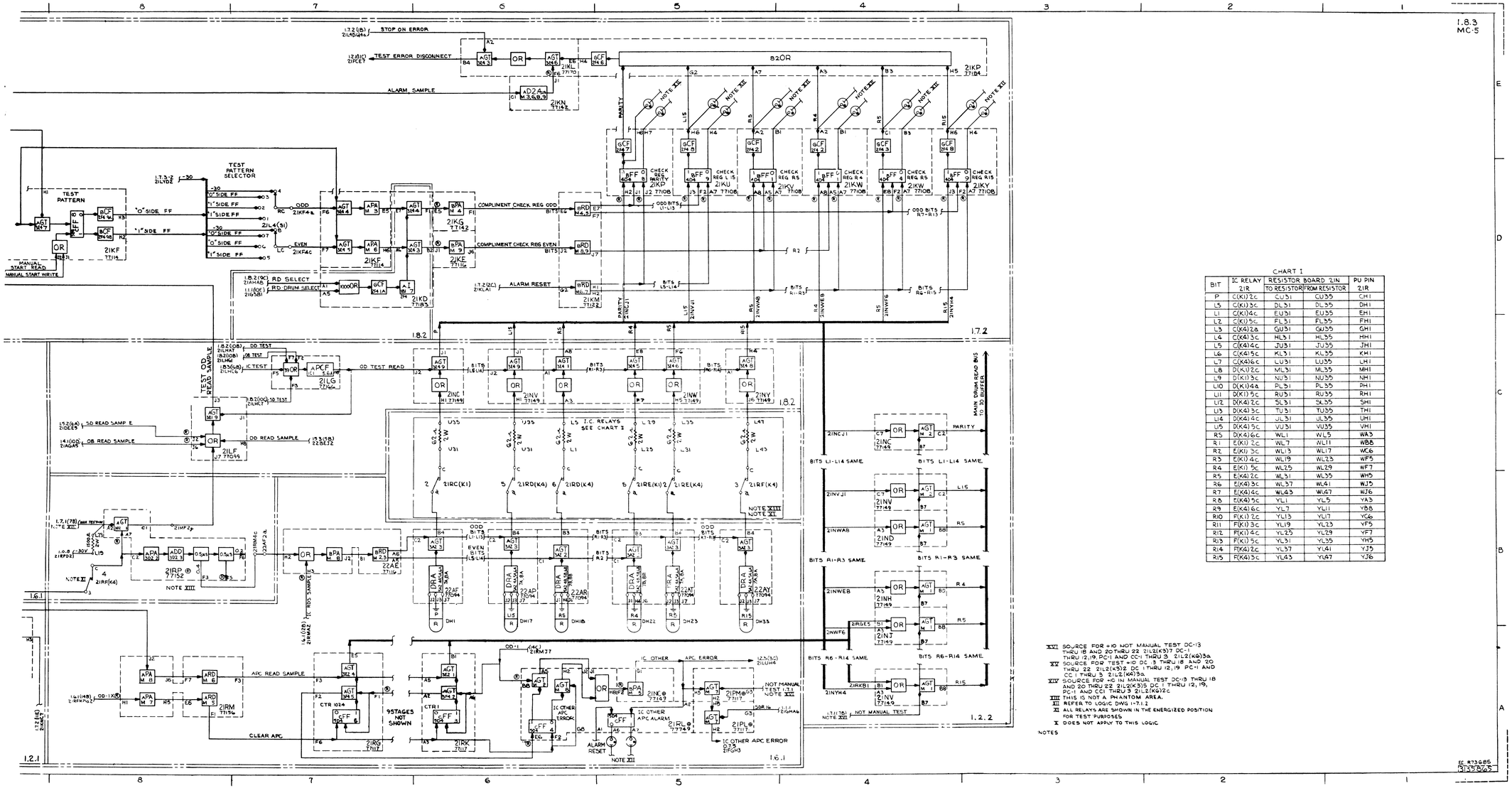


CHART I

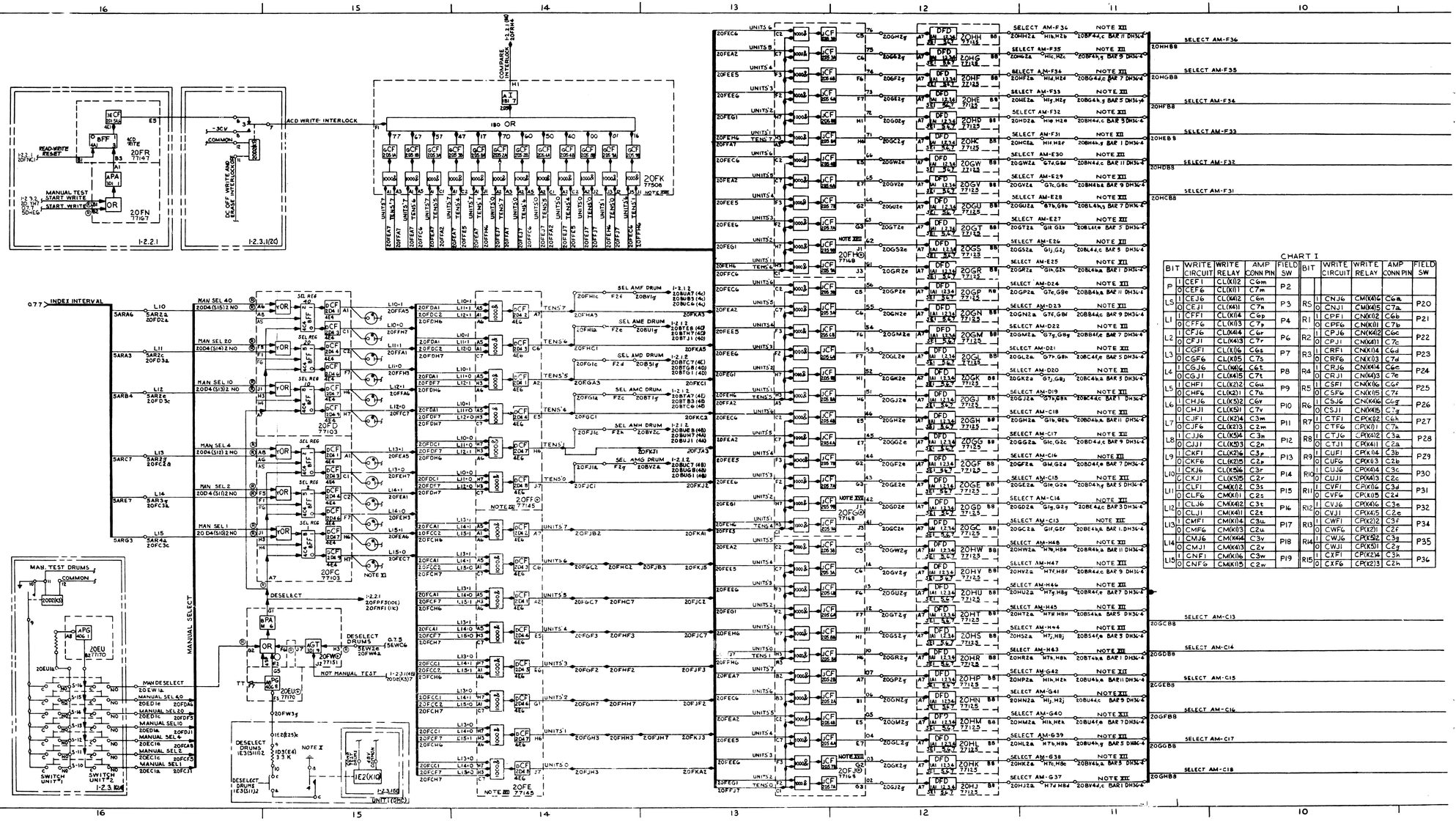
BIT	IC RELAY 2IR	RESISTOR BOARD 2IN TO RESISTOR	RESISTOR BOARD 2IN FROM RESISTOR	PU PIN 2IR
P	C(KI)2C	CU31	CU35	CH1
L5	C(KI)3C	DL31	DL35	DH1
L1	C(KI)4C	EU31	EU35	EH1
L2	C(KI)5C	FL31	FL35	FH1
L3	C(K4)2A	GU31	GU35	GH1
L4	C(K4)3C	HL31	HL35	HH1
L5	C(K4)4C	JU31	JU35	JH1
L6	C(K4)5C	KL31	KL35	KH1
L7	C(K4)6C	LU31	LU35	LH1
L8	D(KI)2C	ML31	ML35	MH1
L9	D(KI)3C	NU31	NU35	NH1
L10	D(K)4A	PL31	PL35	PH1
L11	D(KI)5C	RU31	RU35	RH1
L12	D(K4)2C	SL31	SL35	SH1
L13	D(K4)3C	TU31	TU35	TH1
L14	D(K4)4C	UL31	UL35	UH1
L15	D(K4)5C	VU31	VU35	VH1
R5	D(K4)6C	WL1	WL5	WA3
R1	E(KI)2C	WL7	WL11	WB8
R2	E(KI)3C	WL13	WL17	WC6
R3	E(KI)4C	WL19	WL23	WF5
R4	E(KI)5C	WL25	WL29	WF7
R5	E(K4)2C	WL31	WL35	WH5
R6	E(K4)3C	WL37	WL41	WJ5
R7	E(K4)4C	WL43	WL47	WJ6
R8	E(K4)5C	YL1	YL5	YA3
R9	E(K4)6C	YL7	YL11	YB8
R10	F(KI)2C	YL13	YL17	YC6
R11	F(KI)3C	YL19	YL23	YF5
R12	F(KI)4C	YL25	YL29	YF7
R13	F(KI)5C	YL31	YL35	YH5
R14	F(K4)2C	YL37	YL41	YJ5
R15	F(K4)3C	YL43	YL47	YJ6

XXI SOURCE FOR +10 NOT MANUAL TEST DC-13 THRU 18 AND 20 THRU 22 2IL2(K3)7 DC-1 THRU 2, 19, PC-1 AND CC-1 THRU 3. 2IL2(K6)3a.
XXII SOURCE FOR TEST +10 DC-3 THRU 18 AND 20 THRU 22. 2IL2(K3)2 DC-1 THRU 12, 19 PC-1 AND CC-1 THRU 3. 2IL2(K6)3a.
XIV SOURCE FOR +10 IN MANUAL TEST DC-13 THRU 18 AND 20 THRU 22. 2IL2(K3)5 DC-1 THRU 12, 19, PC-1 AND CC-1 THRU 3. 2IL2(K6)2c.
XIII THIS IS NOT A PHANTOM AREA.
XII REFER TO LOGIC DWG 1-7.1.2
XI ALL RELAYS ARE SHOWN IN THE ENERGIZED POSITION FOR TEST PURPOSES.
X DOES NOT APPLY TO THIS LOGIC

NOTES

EC R73685
3135065

INTERCOMMUNICATION OD TEST CONTROLS



BIT	WRITE CIRCUIT	WRITE RELAY	AMP CONN PIN	FIELD SW
P 1	CEF1	CL(K)02	C6m	P2
P 0	CEF6	CL(K)11	C7m	
L5 1	CEJ6	CL(K)12	C6n	P3
L5 0	CEJ1	CL(K)41	C7n	
L1 1	CFF1	CL(K)14	C6p	P4
L1 0	CFF6	CL(K)13	C7p	
L2 1	CFJ6	CL(K)44	C6r	P6
L2 0	CFJ1	CL(K)43	C7r	
L3 1	CGF1	CL(K)16	C6s	P7
L3 0	CGF6	CL(K)15	C7s	
L4 1	CGJ6	CL(K)46	C6t	P8
L4 0	CGJ1	CL(K)45	C7t	
L5 1	CHF1	CL(K)17	C6u	P9
L5 0	CHF6	CL(K)21	C7u	
L6 1	CHJ6	CL(K)52	C6v	P10
L6 0	CHJ1	CL(K)51	C7v	
L7 1	CJF1	CL(K)24	C3m	P11
L7 0	CJF6	CL(K)23	C2m	
L8 1	CJJ6	CL(K)54	C3n	P12
L8 0	CJJ1	CL(K)53	C2n	
L9 1	CKF1	CL(K)26	C3p	P13
L9 0	CKF6	CL(K)25	C2p	
L10 1	CKJ6	CL(K)56	C3r	P14
L10 0	CKJ1	CL(K)55	C2r	
L11 1	CLF1	CM(K)12	C3s	P15
L11 0	CLF6	CM(K)11	C2s	
L12 1	CLJ6	CM(K)42	C3t	P16
L12 0	CLJ1	CM(K)41	C2t	
L13 1	CMF1	CM(K)14	C3u	P17
L13 0	CMF6	CM(K)13	C2u	
L14 1	CMJ6	CM(K)44	C3v	P18
L14 0	CMJ1	CM(K)43	C2v	
L15 1	CNF1	CM(K)16	C3w	P19
L15 0	CNF6	CM(K)15	C2w	

BIT	WRITE CIRCUIT	WRITE RELAY	AMP CONN PIN	FIELD SW
R5 1	CNJ6	CM(K)46	C6a	P20
R5 0	CNJ1	CM(K)45	C7a	
R1 1	CPF1	CN(K)12	C6b	P21
R1 0	CPF6	CN(K)11	C7b	
R2 1	CPJ6	CN(K)42	C6c	P22
R2 0	CPJ1	CN(K)41	C7c	
R3 1	CRF1	CN(K)14	C6d	P23
R3 0	CRF6	CN(K)13	C7d	
R4 1	CRJ6	CN(K)44	C6e	P24
R4 0	CRJ1	CN(K)43	C7e	
R5 1	CSF1	CN(K)16	C6f	P25
R5 0	CSF6	CN(K)15	C7f	
R6 1	CSJ6	CN(K)46	C6g	P26
R6 0	CSJ1	CN(K)45	C7g	
R7 1	CTF1	CP(K)02	C6h	P27
R7 0	CTF6	CP(K)01	C7h	
R8 1	CTJ6	CP(K)42	C3a	P28
R8 0	CTJ1	CP(K)41	C2a	
R9 1	CUF1	CP(K)04	C3b	P29
R9 0	CUF6	CP(K)03	C2b	
R10 1	CUJ6	CP(K)04	C3c	P30
R10 0	CUJ1	CP(K)03	C2c	
R11 1	CVF1	CP(K)06	C3d	P31
R11 0	CVF6	CP(K)05	C2d	
R12 1	CVJ6	CP(K)46	C3e	P32
R12 0	CVJ1	CP(K)45	C2e	
R13 1	CWF1	CP(K)12	C3f	P34
R13 0	CWF6	CP(K)11	C2f	
R14 1	CWJ6	CP(K)52	C3g	P35
R14 0	CWJ1	CP(K)51	C2g	
R15 1	CXF1	CP(K)24	C3h	P36
R15 0	CXF6	CP(K)23	C2h	

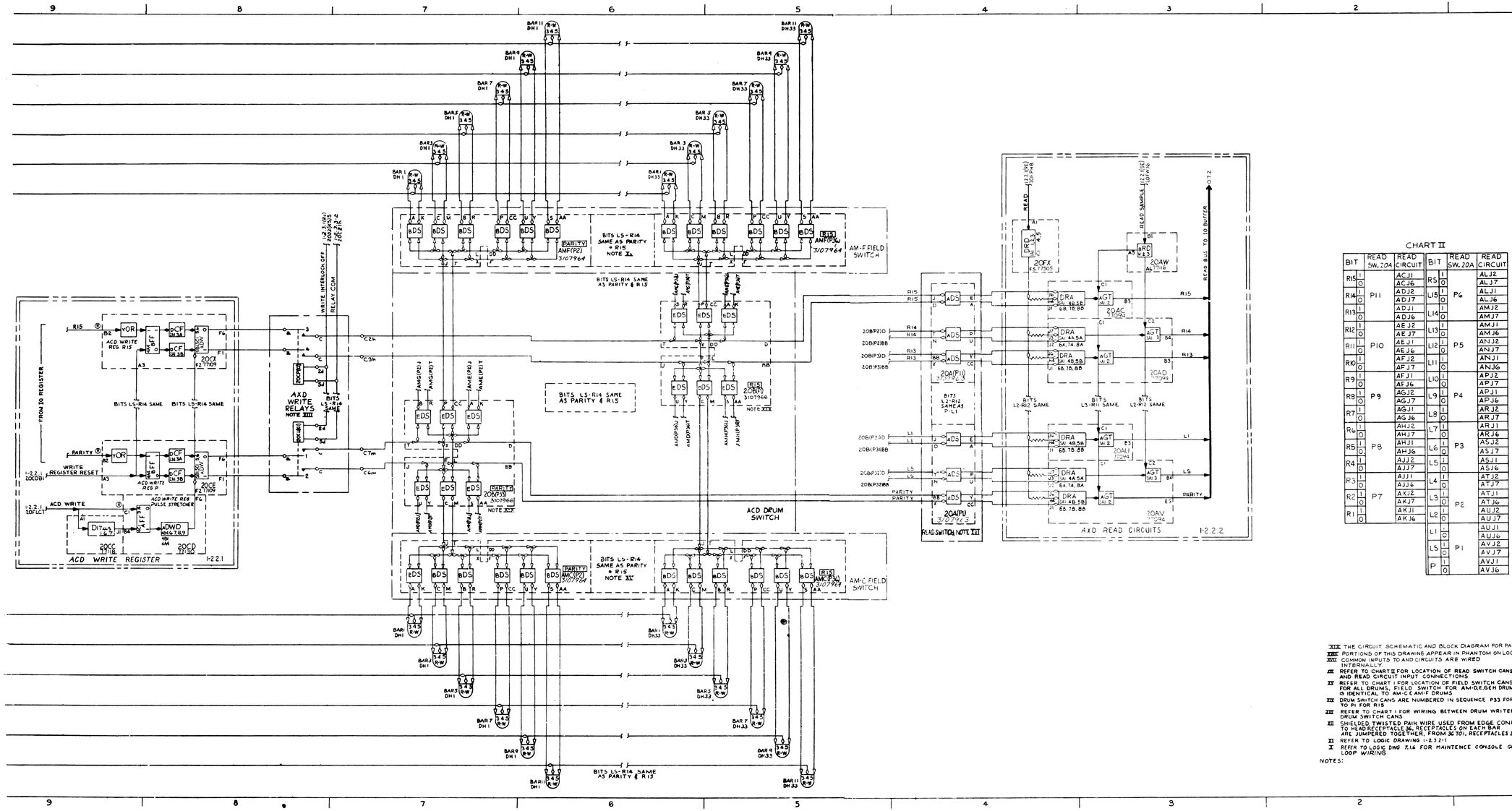


CHART II

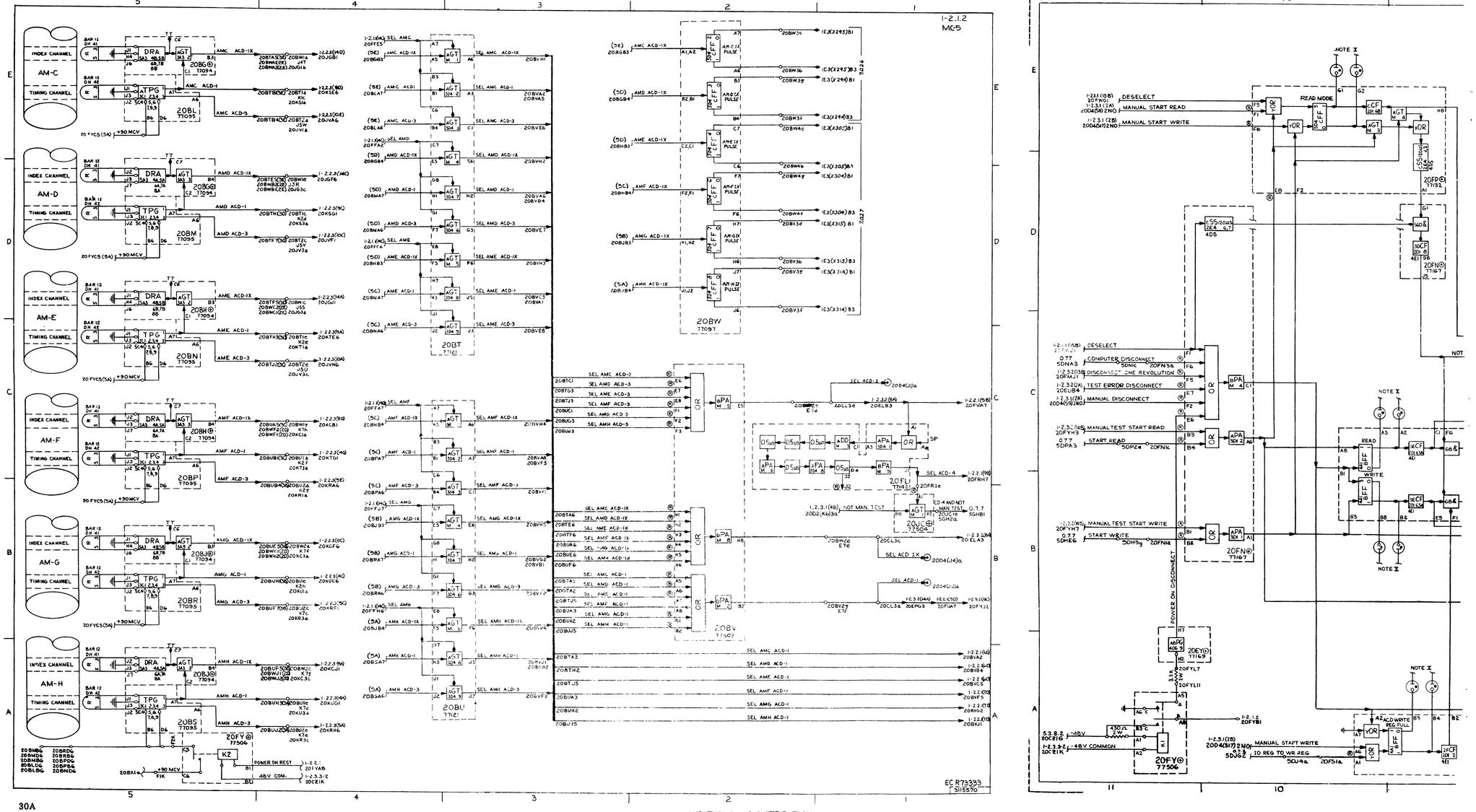
BIT	READ SW. 20A	READ CIRCUIT	BIT	READ SW. 20A	READ CIRCUIT
R15 L	P11	ACJ1	R5 I	P6	AMJ2
R15 O		ACJ6	R5 O		AMJ7
R14 L		ADJ2	L15 L		AMJ1
R14 O		ADJ7	L15 O		AMJ6
R13 L		ADJ1	L14 O		AMJ7
R13 O		ADJ6	L14 I		AMJ7
R12 I	P10	AEJ2	L13 I	P5	AMJ1
R12 O		AEJ7	L13 O		AMJ6
R11 I		AEJ1	L12 I		ANJ2
R11 O		AEJ6	L12 O		ANJ7
R10 I		AFJ2	L11 O		ANJ1
R10 O		AFJ7	L11 O		ANJ6
R9 I	P9	AFJ1	L10 I	P4	APJ2
R9 O		AFJ6	L10 O		APJ7
R8 I		AGJ2	L9 I		APJ1
R8 O		AGJ7	L9 O		APJ6
R7 I		AGJ1	L8 O		ARJ2
R7 O		AGJ6	L8 O		ARJ7
R6 I	P8	AHJ2	L7 I	P3	ARJ1
R6 O		AHJ7	L7 O		ARJ6
R5 I		AHJ1	L6 I		A5J2
R5 O		AHJ6	L6 O		A5J7
R4 I		AJJ2	L5 O		A5J1
R4 O		AJJ7	L5 I		A5J6
R3 I	P7	AJJ1	L4 I	P2	ATJ2
R3 O		AJJ6	L4 O		ATJ7
R2 I		AKJ2	L3 O		ATJ1
R2 O		AKJ7	L3 O		ATJ6
R1 I		AKJ1	L2 O		AUJ2
R1 O		AKJ6	L2 O		AUJ7
			L1 O	P1	AUJ1
			L1 O		AUJ6
			L5 I		AVJ2
			L5 O		AVJ7
			P I		AVJ1
			P O		AVJ6

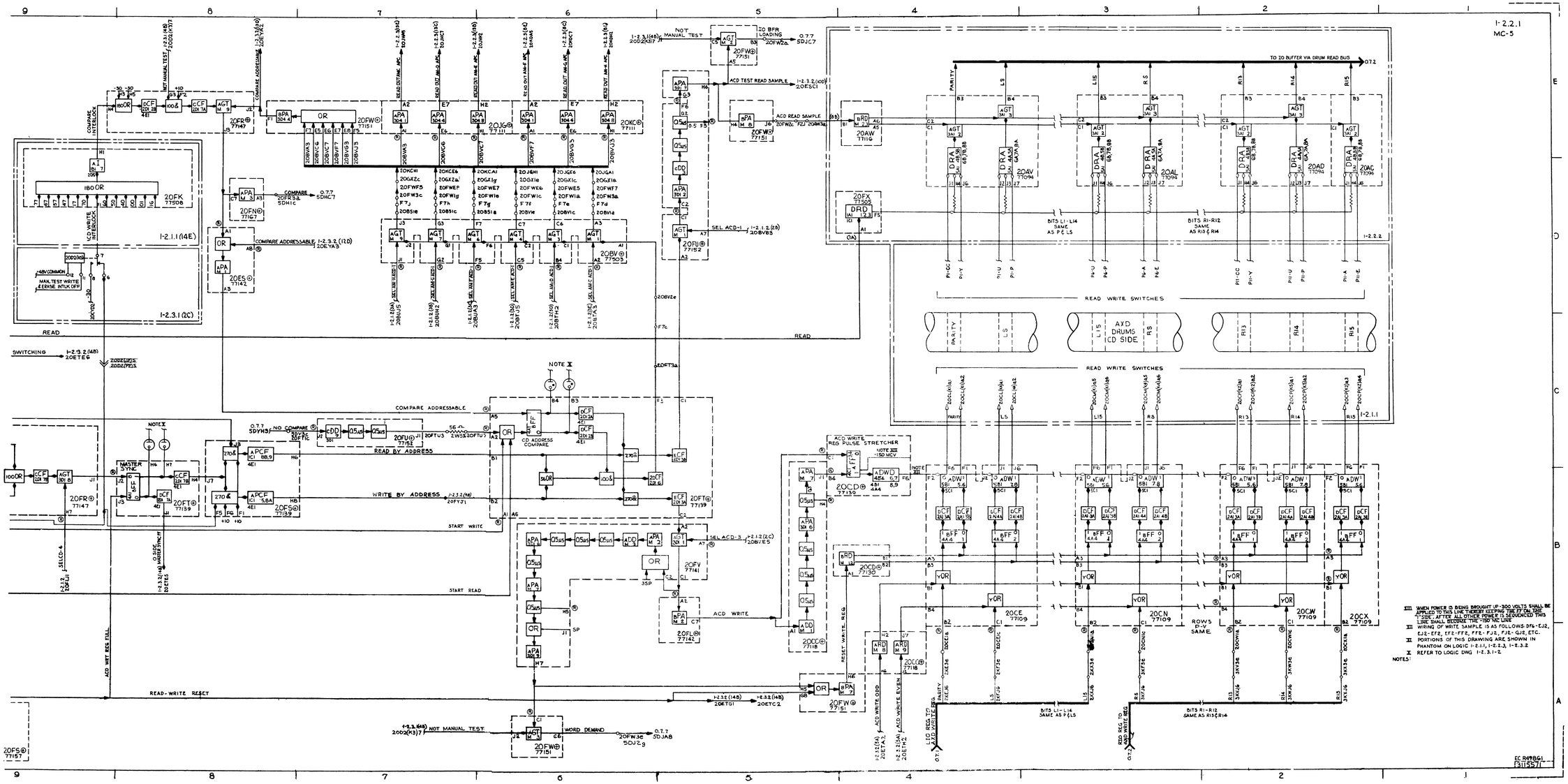
NOTES:

XIX THE CIRCUIT SCHEMATIC AND BLOCK DIAGRAM FOR PART NO. 3107966 IS 3107976.
XVIII PORTIONS OF THIS DRAWING APPEAR IN PHANTOM ON LOGIC 1-2.2.1
XVII COMMON INPUTS TO AND CIRCUITS ARE WIRED INTERNALLY.
IX REFER TO CHART II FOR LOCATION OF READ SWITCH CANS AND READ CIRCUIT INPUT CONNECTIONS
V REFER TO CHART I FOR LOCATION OF FIELD SWITCH CANS FOR ALL DRUMS. FIELD SWITCH FOR AM-D,E,G&H DRUMS IS IDENTICAL TO AM-C AM-F DRUMS
III DRUM SWITCH CANS ARE NUMBERED IN SEQUENCE P33 FOR PARITY TO P1 FOR R15
II REFER TO CHART I FOR WIRING BETWEEN DRUM WRITERS AND DRUM SWITCH CANS
III SHIELDED TWISTED PAIR WIRE USED FROM EDGE CONNECTOR TO HEAD RECEPTACLE 36. RECEPTACLES ON EACH BAR ARE JUMPERED TOGETHER. FROM 3G701, RECEPTACLES 34 TO 36 ARE SPARE.
II REFER TO LOGIC DRAWING 1-2.3.2-1
I REFER TO LOGIC DWG 7.1.6 FOR MAINTENCE CONSOLE GROUND LOOP WIRING

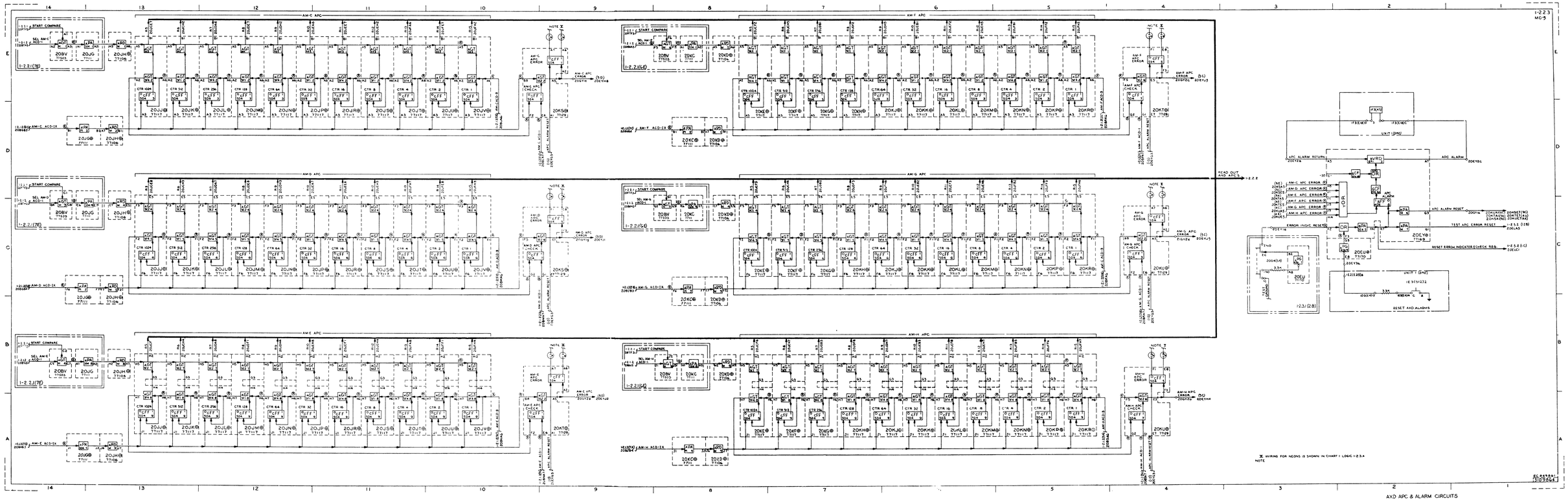
ECP-69861
3107940

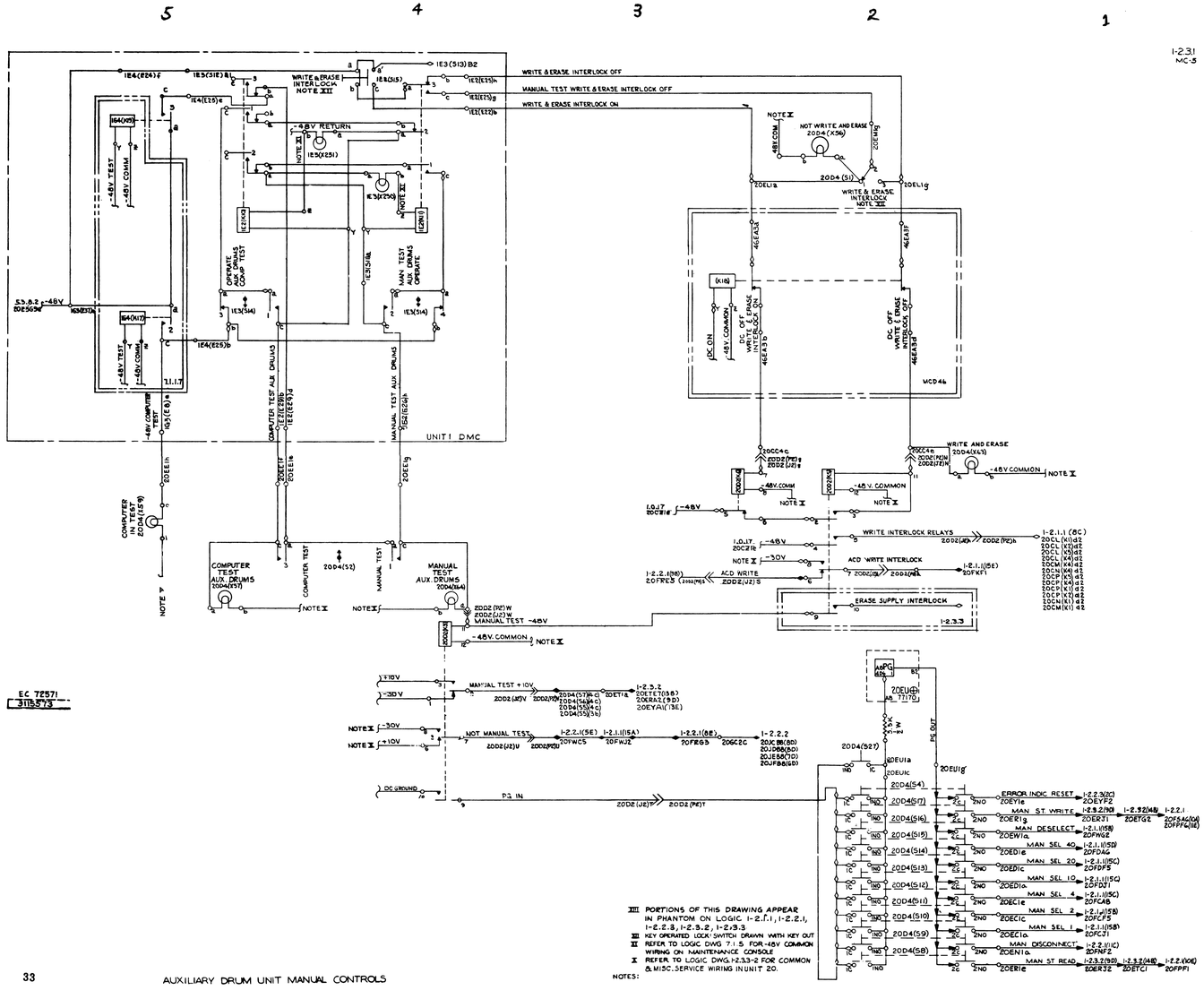
AXD DRUM SELECTION AND DIODE SWITCHING


1-2.1.2
MC-5
INDEX CHANNEL
AM-C
TIMING CHANNEL
AM-D
AM-E
AM-F
AM-G
AM-H
DRA
TPG
AGT
20BG
20BM
20BH
20BN
20BP
20BJ
20BR
20BS
20BL
20BT
20BU
20BW
20FV
20FY
AMC ACD-1X
AMC ACD-1
AMC ACD-3
AMD ACD-1X
AMD ACD-1
AMD ACD-3
AME ACD-1X
AME ACD-1
AME ACD-3
AMF ACD-1X
AMF ACD-1
AMF ACD-3
AMG ACD-1X
AMG ACD-1
AMG ACD-3
AMH ACD-1X
AMH ACD-1
AMH ACD-3
SEL AMC ACD-1X
SEL AMC ACD-1
SEL AMC ACD-3
SEL AMD ACD-1X
SEL AMD ACD-1
SEL AMD ACD-3
SEL AME ACD-1X
SEL AME ACD-1
SEL AME ACD-3
SEL AMF ACD-1X
SEL AMF ACD-1
SEL AMF ACD-3
SEL AMG ACD-1X
SEL AMG ACD-1
SEL AMG ACD-3
SEL AMH ACD-1X
SEL AMH ACD-1
SEL AMH ACD-3
20FYC5(5A)
+90MCV
20BXI
FIK
KZ
POWER ON RESET
48V COM.
20FV@ 77506
20BW 77097
20BT 77161
20BU 77161
EC R73393
5115570
AXD TIMING AND DISTRIBUTION
30A
NOTE I
READ MODE
DESELECT
MANUAL START READ
MANUAL START WRITE
COMPUTER DISCONNECT
DISCONNECT SMC REVOLUTION
TEST ERROR DISCONNECT
MANUAL DISCONNECT
MANUAL TEST START READ
START READ
MANUAL TEST START WRITE
START WRITE
POWER ON DISCONNECT
READ
WRITE
20FN@ 77167
20EY@ 77162
20FP@ 77132
20FQ@ 77167
-48V
48V COMMON
MANUAL STAPT WRITE
IO REG TO WR REG


I-2.2.1
MC-5
TO IO BUFFER VIA DRUM READ BUS
READ WRITE SWITCHES
AXD DRUMS CD SIDE
PARITY
LS
L15
RS
R13
R14
R15
READ
WRITE
COMPARE ADDRESSABLE
NO COMPARE
CD ADDRESS COMPARE
READ BY ADDRESS
WRITE BY ADDRESS
START WRITE
START READ
ACD WRITE
ACD WRT REG FULL
READ-WRITE RESET
RESET WRITE REG
ACD WRITE REG PULSE STRETCHER
ACD WRITE ODD
ACD WRITE EVEN
ACD TEST READ SAMPLE
ACD READ SAMPLE
SEL ACD-1
SEL ACD-2
SEL ACD-3
WORD DEMAND
NOT MANUAL TEST
IO BFR LOADING
SWITCHING
MASTER SYNC
MAN. TEST WRITE ERASE INTLK OFF
LCD WRITE INTERLOCK
COMPARE INTERLOCK
BITS L1-L14 SAME AS P'S LS
BITS R1-R12 SAME AS R13 & R14
ROWS E-Y SAME.
LCD REG TO AXD WRITE REG
RDD REG TO AXD WRITE REG
NOTE XIII
NOTES:
WHEN POWER IS BEING BROUGHT UP 300 VOLTS SHALL BE APPLIED TO THIS LINE THEREBY KEEPING THE FF ON. THE +150C AFTER ALL OTHER POWER IS DERANGED THIS LINE SHALL BECOME THE -150 MC LINE
WIRING OF WRITE SAMPLE IS AS FOLLOWS: DF6-EJ2, EJ2-EF2, EF2-FF2, FF2-FJ2, FJ2-GJ2, ETC.
PORTIONS OF THIS DRAWING ARE SHOWN IN PHANTOM ON LOGIC I-E.1.1, I-2.2.3, I-E.3.2
REFER TO LOGIC DWG I-2.3.1-2.
EC R498GL
5311557L
AXD DRUMS CONTROL AND WRITE CIRCUITS
30B

AXD READ CIRCUITS


AM-C APC
AM-F APC
AM-D APC
AM-G APC
AM-E APC
AM-H APC
START COMPARE
SEL AM-C ACD-1
SEL AM-F ACD-1
SEL AM-D ACD-1
SEL AM-G ACD-1
SEL AM-E ACD-1
SEL AM-H ACD-1
AM-C APC ERROR
AM-F APC ERROR
AM-D APC ERROR
AM-G APC ERROR
AM-E APC ERROR
AM-H APC ERROR
AM-C APC CHECK
AM-F APC CHECK
AM-D APC CHECK
AM-G APC CHECK
AM-E APC CHECK
AM-H APC CHECK
CTR 1024
CTR 512
CTR 256
CTR 128
CTR 64
CTR 32
CTR 16
CTR 8
CTR 4
CTR 2
CTR 1
NOTE X
READ OUT AXD APC'S
I-2.2.2
APC ALARM RETURN
APC ALARM
APC ALARM RESET
TEST APC ERROR RESET
ERROR IN SYNC RESET
RESET ERROR INDICATOR (CHECK REG.
RESET AXD ALARMS
UNIT 1 (PM2)
UNIT 7 (PM7)
I-2.3 (2B)
X WIRING FOR NEONS IS SHOWN IN CHART I LOGIC I-2.3.4
NOTE
I-2.2.3
MC-5
AXD APC & ALARM CIRCUITS



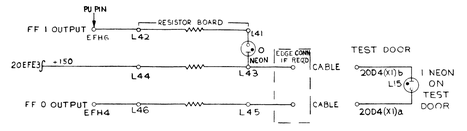
EC 72571
3115573

AUXILIARY DRUM UNIT MANUAL CONTROLS

ADVANCE

1-2.3.1-2

TYPICAL WIRING DRAWING
UNIT 20 - NEONS

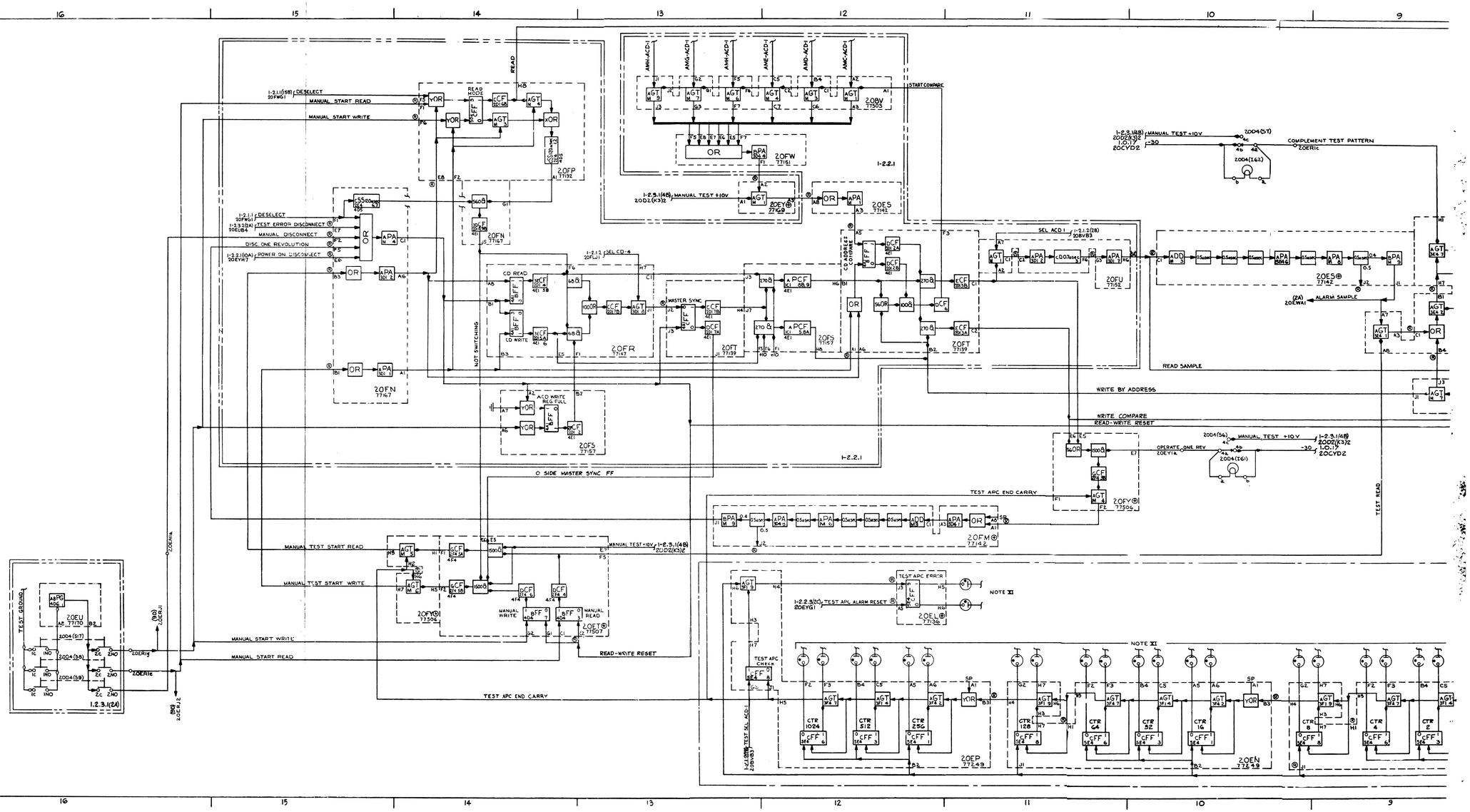


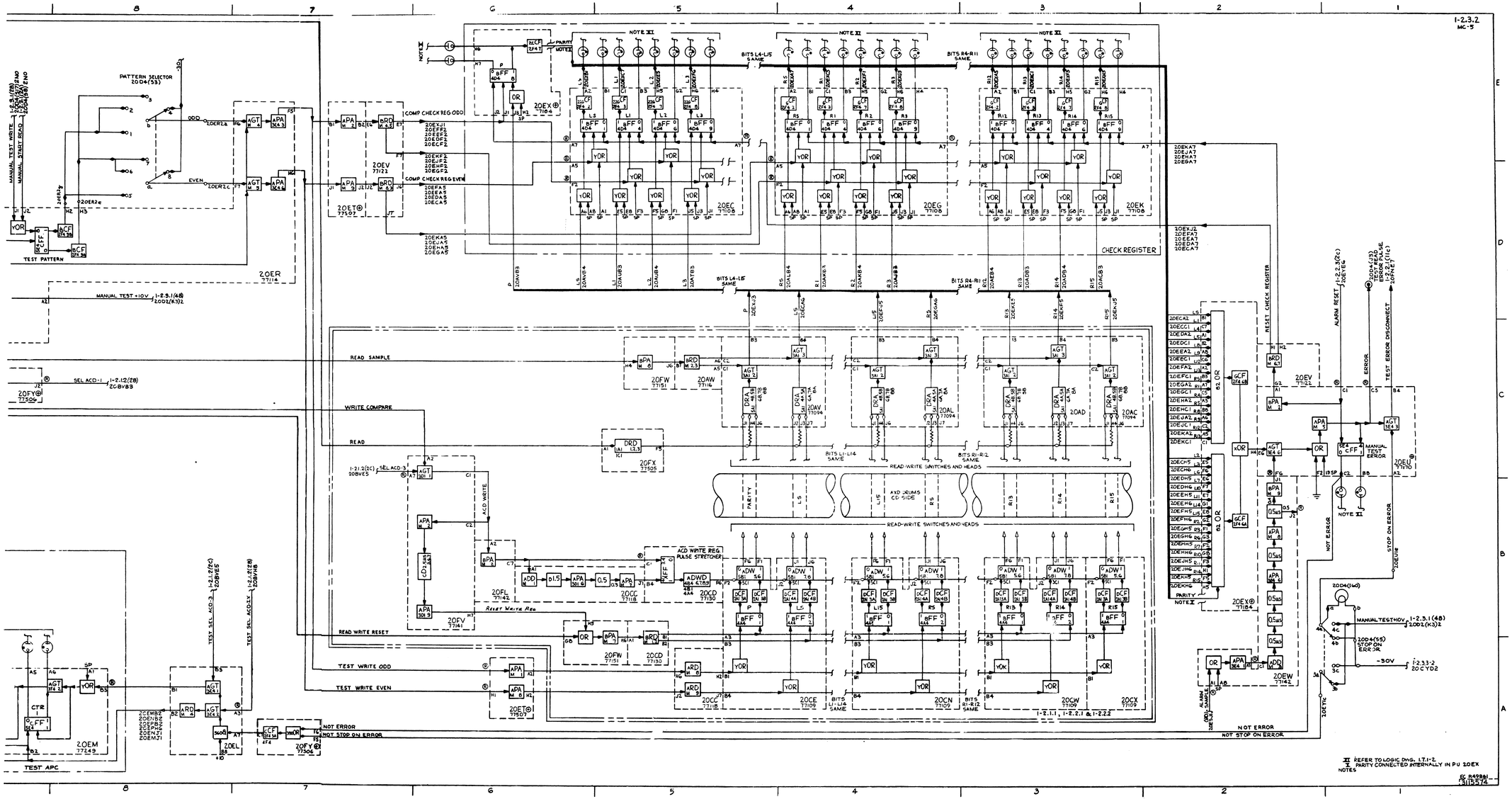
FF OUT	PU TERM	RES RESISTOR	BOARD TERM 0 NEON			LOGIC & E.C.	NEON & TITLE
1	ECA2	U18	U17	U17	U9	1-2.3.2	L5
+150	ECE3	U10	U9				20D4(X16)b
0	ECB1	U12	U11				20D4(X16)a
1	ECC1	U16	U15	U15	U17	1-2.3.2	L1
+150	ECE3	U18	U17				20D4(X15)b
0	ECB3	U20	U19				20D4(X15)a
1	ECH1	U34	U33	U33	U35	1-2.3.2	L2
+150	ECE3	U36	U35				20D4(X14)b
0	ECG2	U38	U37				20D4(X14)a
1	ELH6	U42	U41	U41	U43	1-2.3.2	L3
+150	ECE3	U44	U43				20D4(X13)b
0	ECH4	U46	U45				20D4(X13)a
1	EDA1	L8	L7	L7	L9	1-2.3.2	L4
+150	EDE3	L10	L9				20D4(X12)b
0	EDB1	L12	L11				20D4(X12)a
1	EDC1	L16	L15	L15	L17	1-2.3.2	L5
+150	EDE3	L18	L17				20D4(X11)b
0	EDB3	L20	L19				20D4(X11)a
1	EDH5	L34	L33	L33	L35	1-2.3.2	L6
+150	EDE3	L36	L35				20D4(X10)b
0	EDG2	L38	L37				20D4(X10)a
1	EDH1	L42	L41	L41	L43	1-2.3.2	L7
+150	EDE3	L44	L43				20D4(X9)b
0	EDH4	L46	L45				20D4(X9)a
1	EEA2	U8	U7	U7	U9	1-2.3.2	L8
+150	EEE3	U10	U9				20D4(X8)b
0	EEB1	U12	U11				20D4(X8)a
1	EEC1	U16	U15	U15	U17	1-2.3.2	L9
+150	EEE3	U18	U17				20D4(X7)b
0	EEB3	U20	U19				20D4(X7)a
1	EEH5	U34	U33	U33	U35	1-2.3.2	L10
+150	EEE3	U36	U35				20D4(X6)b
0	EEG2	U38	U37				20D4(X6)a
1	EEH1	U42	U41	U41	U43	1-2.3.2	L11
+150	EEE3	U44	U43				20D4(X5)b
0	EEH4	U46	U45				20D4(X5)a
1	EFA2	L8	L7	L7	L9	1-2.3.2	L12
+150	EFE3	L10	L9				20D4(X4)b
0	EFB1	L12	L11				20D4(X4)a
1	EFC1	L16	L15	L15	L17	1-2.3.2	L13
+150	EFE3	L18	L17				20D4(X3)b
0	EFB3	L20	L19				20D4(X3)a
1	EFH5	L34	L33	L33	L35	1-2.3.2	L14
+150	EFE3	L36	L35				20D4(X2)b
0	EFG2	L38	L37				20D4(X2)a
1	EFH1	L42	L41	L41	L43	1-2.3.2	L15
+150	EFE3	L44	L43				20D4(X1)b
0	EFH4	L46	L45				20D4(X1)a
1	EGA2	U8	U7	U7	U9	1-2.3.2	R5
+150	EGE3	U10	U9				20D4(X33)b
0	EGB1	U12	U11				20D4(X33)a
1	EGC1	U16	U15	U15	U17	1-2.3.2	R1
+150	EGE3	U18	U17				20D4(X32)b
0	EGB3	U20	U19				20D4(X32)a
1	EGH5	U34	U33	U33	U35	1-2.3.2	R2
+150	EGE3	U36	U35				20D4(X31)b
0	EGG2	U38	U37				20D4(X31)a
1	EGH1	U42	U41	U41	U43	1-2.3.2	R3
+150	EGE3	U44	U43				20D4(X30)b
0	EGH4	U46	U45				20D4(X30)a
1	EHA2	L8	L7	L7	L9	1-2.3.2	R4
+150	EHE3	L10	L9				20D4(X29)b
0	EHB1	L12	L11				20D4(X29)a

FFOUT	PU TERM	RES RESISTOR	BOARD TERM 0 NEON			LOGIC & E.C.	NEON & TITLE
1	EHC1	L16	L15	L15	L17	1-2.3.2	R5
+150	EHE3	L18	L17				20D4(X28)b
0	EHB3	L20	L19				20D4(X28)a
1	EHH5	L34	L33	L33	L35	1-2.3.2	R6
+150	EHE3	L36	L35				20D4(X27)b
0	EHG2	L38	L37				20D4(X27)a
1	EHH1	L42	L41	L41	L43	1-2.3.2	R7
+150	LHE3	L44	L43				20D4(X26)b
0	EHH4	L46	L45				20D4(X26)a
1	EJA2	U8	U7	U7	U9	1-2.3.2	R8
+150	EJE3	U10	U9				20D4(X25)b
0	EJB1	U12	U11				20D4(X25)a
1	EJC1	U16	U15	U15	U17	1-2.3.2	R9
+150	EJE3	U18	U17				20D4(X24)b
0	EJB3	U20	U19				20D4(X24)a
1	EJH5	U34	U33	U33	U35	1-2.3.2	R10
+150	EJE3	U36	U35				20D4(X23)b
0	EJG2	U38	U37				20D4(X23)a
1	EJH1	U42	U41	U41	U43	1-2.3.2	R11
+150	EJE3	U44	U43				20D4(X22)b
0	EJH4	U46	U45				20D4(X22)a
1	LKA2	L8	L7	L7	L9	1-2.3.2	P12
+150	EKE3	L10	L9				20D4(X21)b
0	LKB1	L12	L11				20D4(X21)a
1	EKC1	L16	L15	L15	L17	1-2.3.2	R13
+150	EKE3	L18	L17				20D4(X20)b
0	EKB3	L20	L19				20D4(X20)a
1	EKH5	L34	L33	L33	L35	1-2.3.2	R14
+150	EKE3	L36	L35				20D4(X19)b
0	EKG2	L38	L37				20D4(X19)a
1	EKH6	L42	L41	L41	L43	1-2.3.2	R15
+150	EKE3	L44	L43				20D4(X18)b
0	EKH4	L46	L45				20D4(X18)a
1	ELH5	U40	L39	U39	U41	1-2.3.2	TEST APC ERROR
+150	ELE3	U42	U41				20D4(X48)b
0	ELH6	U44	U43				20D4(X48)a
1	EMA6	L4	L3	L3	L5	1-2.2.2	TEST APC 1
+150	EME3	L6	L5				20D4(X34)b
0	EMA5	L8	L7				20D4(X34)a
1	EMC5	L14	L13	L13	L15	1-2.3.2	TEST APC 2
+150	EME3	L16	L15				20D4(X35)b
0	EMB4	L18	L17				20D4(X35)a
1	EMF3	L26	L25	L25	L27	1-2.3.2	TEST APC 4
+150	EME3	L28	L27				20D4(X36)b
0	EMF2	L30	L29				20D4(X36)a
1	EMH7	L34	L33	L33	L35	1-2.3.2	TEST APC 8
+150	EME3	L36	L35				20D4(X37)b
0	EMG2	L38	L37				20D4(X37)a
1	ENA6	U2	U1	U1	U3	1-2.3.2	TEST APC 16
+150	ENE3	U4	U3				20D4(X38)b
0	ENA5	U6	U5				20D4(X38)a
1	ENC5	U16	U15	U15	U17	1-2.3.2	TEST APC 32
+150	ENE3	U18	U17				20D4(X39)b
0	ENB4	U20	U19				20D4(X39)a
1	ENF3	U26	U25	U25	U27	1-2.3.2	TEST APC 64
+150	ENE3	U28	U27				20D4(X40)b
0	ENF2	U30	U29				20D4(X40)a
1	ENH7	U34	U33	U33	U35	1-2.3.2	TEST APC 128
+150	ENE3	U36	U35				20D4(X41)b
0	ENG2	U38	U37				20D4(X41)a
1	EPA6	L2	L1	L1	L3	1-2.3.2	TEST APC 256
+150	EPE3	L4	L3				20D4(X42)b
0	EPA5	L6	L5				20D4(X42)a
1	EPC5	L16	L15	L15	L17	1-2.3.2	TEST APC 512
+150	EPE3	L18	L17				20D4(X43)b
0	EPB4	L20	L19				20D4(X43)a

FF OUT	PU TERM	RES RESISTOR	BOARD TERM 0 NEON			LOGIC & EDGE CONN	NEON & TITLE
1	EPF3	L26	L25	L25	L27	1-2.3.2	TEST APC 1024
+150	EPE3	L28	L27				20D4(X44)b
0	EPF2	L30	L29				20D4(X44)a
1	EUB8	L2	L1	L1	L3	1-2.3.2	NOT ERROR
+150	EUE3	L4	L3				20D4(X58)b
0	EUC2	L6	L5				20D4(X58)a
1	EXH6	U39	U37	U37	U35	1-2.3.2	PARITY
+150	EXE3	U33	U35				20D4(X17)b
0	EXH7	U41	U43				20D4(X17)a
1	FCA1	U10	U9	U9	U11	1-2.1.1	SEL REG 4
+150	FCE3	U12	U11				20D4(X68)b
0	FCL1	U14	U13				20D4(X68)a
1	FCC1	U32	U31	U31	U33	1-2.1.1	SEL REG 2
+150	FCE3	U34	U33				20D4(X67)b
0	FCF1	U36	U35				20D4(X67)a
1	FCH6	U44	U43	U43	U45	1-2.1.1	SEL REG 1
+150	FCE3	U46	U45				20D4(X66)b
0	FCH7	U48	U47				20D4(X66)a
1	FD11	L10	L9	L9	L11	1-2.1.1	SEL REG 40
+150	FDE3	L12	L11				20D4(X71)b
0	FDC1	L14	L13				20D4(X71)a
1	FDC2	L32	L31	L31	L33	1-2.1.1	SEL REG 20
+150	FDE3	L34	L33				20D4(X70)b
0	FDF7	L36	L35				20D4(X70)a
1	FDH6	L44	L43	L43	L45	1-2.1.1	SEL REG 10
+150	FDE3	L46	L45				20D4(X69)b
0	FDH7	L48	L47				20D4(X69)a
1	FPG1	L31	L33	L33	L35	1-2.2.1	READ MODE
+150	FPE3	L37	L35				20D4(X46)b
0	FPG2	L41	L39				20D4(X46)a
1	FRA2	U4	U3	U3	U5	1-2.2.1	READ FF
+150	FRE3	U6	U5				20D4(X65)b
0	FRA3	U8	U7				20D4(X65)a
1	FRB2	U12	U11	U11	U13	1-2.2.1	WRITE FF
+150	FRE3	U14	U13				20D4(X72)b
0	FRB8	U16	U15				20D4(X72)a
1	FSB4	L8	L7	L7	L9	1-2.2.1	ADWRITE REGFULL
+150	FSE3	L10	L9				20D4(X55)b
0	FSB3	L12	L11				20D4(X55)a
1	FTB4	U40	U39	U39	U41	1-2.2.1	CD PROCESS COMPARE
+150	FTE3	U42	U41				20D4(X47)b
0	FTB3	U44	U43				20D4(X47)a
1	FTH7	U10	U9	U9	U11	1-2.2.1	MASTER SYNC
+150	FTE3	U12	U11				20D4(X45)b
0	FTH6	U14	U13				20D4(X45)a
1	KSA6	L11	L13	L13	L15	1-2.2.3	AM-C APC ERROR
+150	KSE3	L17	L15				G51b 20D4(X54)b
0	KSA7	L21	L19				G51a 20D4(X54)a
1	KSE8	L37	L39	L39	L41	1-2.2.3	AM-D APC ERROR
+150	KSE3	L43	L41				G51d 20D4(X53)b
0	KSF1	L47	L45				G51c 20D4(X53)a
1	KTA6	U11	U13	U13	U15	1-2.2.3	AM-E APC ERROR
+150	KTE3	U17	U15				GT1b 20D4(X52)b
0	KTA7	U21	U19				GT1a 20D4(X52)a
1	KTE8	U37	U39	U39	U41	1-2.2.3	AM-F APC ERROR
+150	KTE3	U43	U41				GT1d 20D4(X51)b
0	KTF1	U47	U45				GT1c 20D4(X51)a
1	KUA6	L11	L13	L13	L15	1-2.2.3	AM-G APC ERROR
+150	KUE3	L17	L15				GU1b 20D4(X50)b
0	KUA7	L21	L19				GU1a 20D4(X50)a
1	KUE8	L37	L39	L39	L41	1-2.2.3	AM-H APC ERROR
+150	KUE3	L43	L41				GU1d 20D4(X49)b
0	KUF1	L47	L45				GU1c 20D4(X49)a

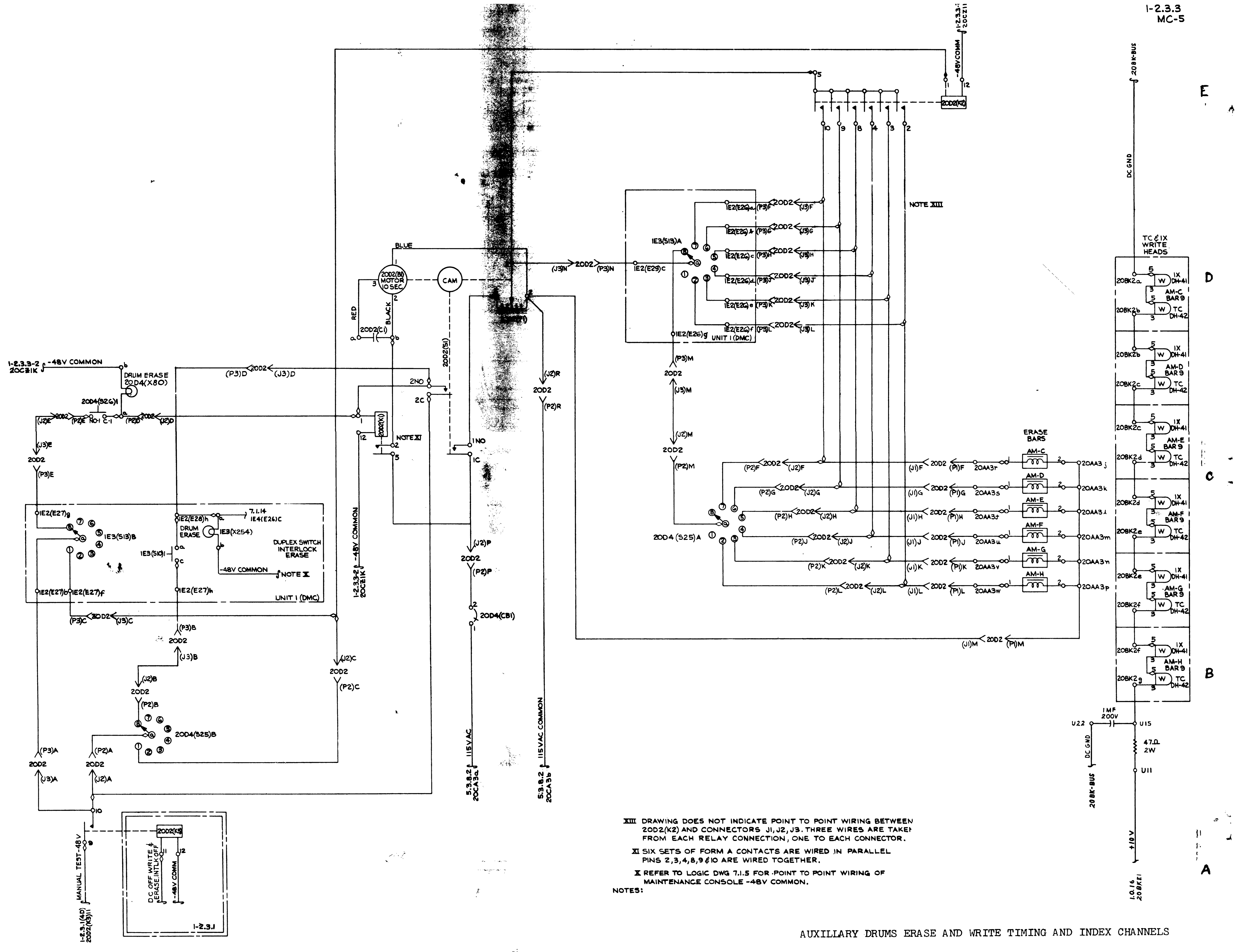
AND DRUMS TEST PANEL NEON WIRING


READ
READ MODE
20FP
A1 77132
20FN
77167
20FR
77147
20FT
J1 77139
20FS
77167
20FW
77161
20BV
77503
20ES
77142
20FU
77152
20EY
77149
20EN
77149
20FV
77506
20FM
77142
20EL
77136
20EU
A5 77170
20EP
77149
I-2.2.1
I-2.3.1(24)
0 SIDE MASTER SYNC FF
READ SAMPLE
WRITE BY ADDRESS
WRITE COMPARE
READ-WRITE RESET
TEST APC END CARRY
TEST READ
COMPLEMENT TEST PATTERN
ALARM SAMPLE
NOTE XI
MANUAL START READ
MANUAL START WRITE
MANUAL TEST START READ
MANUAL TEST START WRITE
DISC ONE REVOLUTION
MANUAL DISCONNECT
TEST APC ERROR
TEST GROUND
CTR 1024
CTR 512
CTR 256
CTR 128
CTR 64
CTR 32
CTR 16
CTR 8
CTR 4
CTR 2



XI REFER TO LOGIC DWG. L7.1-2.
I PARITY CONNECTED INTERNALLY IN PU 20EX

AXD MANUAL TEST READ-WRITE CONTROLS



NOTES:

X REFER TO LOGIC DWG 7.1.5 FOR POINT TO POINT WIRING OF MAINTENANCE CONSOLE -48V COMMON.

XI SIX SETS OF FORM A CONTACTS ARE WIRED IN PARALLEL PINS 2,3,4,8,9 & 10 ARE WIRED TOGETHER.

XIII DRAWING DOES NOT INDICATE POINT TO POINT WIRING BETWEEN 2002(K2) AND CONNECTORS J1, J2, J3. THREE WIRES ARE TAKEN FROM EACH RELAY CONNECTION, ONE TO EACH CONNECTOR.

AUXILLARY DRUMS ERASE AND WRITE TIMING AND INDEX CHANNELS

ATC Keesler 7-3157