REV	EO	DESCRIPTION	DWN	CHKD	APPD	DATE
A	3880	NEW RELEASE	JHH	—	—	6/26/75
B	4572	INCORP. E. O.	EKM	RTL	—	5/10/76
C	6786	INCORP. E.O.	RDP	9/22	RTL	3/16/77

CURRENT REV.	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET NO.	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
CURRENT REV.	C	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET NO.	27	28	29	30	31	32	33	34	35	36	37	38	39		
CURRENT REV	B	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET NO.	14	15	16	17	18	19	20	21	22	23	24	25	26		
CURRENT REV.	C	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET NO.	1	2	3	4	5	6	7	8	9	10	11	12	13		

UNINCORPORATED ENGINEERING ORDERS	

PREPARED J.H.Hookum	DATE 6/20/75	TITLE
CHECKER L. Scarsdale	6/20/75	2602 BINARY SYNCHRONOUS COMMUNICATIONS CONTROLLER
ENGINEER Bob Stewart	6/20/75	
APPD D Sawtt	6/26/75	
APPD	6/23/75	
APPD	6-24-75	
RECORDS		IDENT CODE 52936

Microdata™ IRVINE, CALIFORNIA

A	PS20002602	C
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Form 3-132-1

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1.0 INTRODUCTION

The Bisynchronous Modem Interface is a single card controller for those users who wish to employ Binary Synchronous Communications (BSC) procedures and equipment for data link communications. The Bisync Modem Interface is an I/O controller plug-in card option designed for all versions of the Micro 1600 processor and the REALITY Transaction Processor. The card provides the processor with the capability to communicate over full- and half-duplex data links, employing a half-duplex mode of operation, and interfacing with synchronous modems at all rates from 2000 to 20,000 Baud. It is assumed that clocking will be provided by the modems.

The controller is a single-channel version which utilizes an 8-bit character encoded in EBCDIC (transparent or non-transparent) character code assignments.

All data is transmitted as a serial bit stream and employs exclusively the Binary Synchronous Communications (BSC) procedures for data link discipline. The modem interface control procedures conform to the requirements of EIA RS-232-C.

2.0 CONTROLLER SUMMARY

Modem Rates

All rates to 20 kilobits per second will be supported. Data clocking shall be provided by the modem.

Modem Interface

EIA Standard RS-232-C, Half- and Full-Duplex.

Transmission Codes

EBCDIC
Transparent EBCDIC

Data Link Discipline

IBM Binary Synchronous Communications per IBM Document GA27-3004-2.

Synchronization

Modem supplied clock.

Error Checking

CRC-16
CRC-CCITT (Europe)

Data Transfer Modes

Byte I/O
Concurrent I/O

Card Addressing

Device and interrupt addresses. Strap selectable.
Range 00 thru 1F.

User Addressing

Line bidding and multilink addressing which employ user addresses will be supported in software.

Time Outs

Transmit – Nominal 1 second

Continue – Nominal 2 seconds

Receive – Nominal 3 seconds

Disconnect – Nominal 20 seconds.

3.0 FEATURES

3.1 Modem Rates, Interface and Quality

All modem rates from 2 kilobits per second to 20 kilobits per second can be accommodated. Modems which provide clock signals must be used. The modem interface discipline which the controller shall provide meets the requirements of EIA Standard RS-232-C, Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange. Modem and controller signal quality shall meet the requirements of EIA Standard RS-334, Signal Quality at Interface Between Data Processing Terminal Equipment and Synchronous Data Communication Equipment for Serial Data Transmission.

3.2 Transmission Codes

The transmission codes employed by the 2602 Bisynchronous Controller are Extended Binary Coded Decimal Interchange Code, EBCDIC, and the transparent code set. The EBCDIC code set consists of numeric, alphabetic (both upper and lower case), symbolic and special graphic characters. Certain symbols of the code are set aside for data link control requirements.

Figure 3.2.1 shows a standard EBCDIC Character Assignment Chart as presented in IBM document GA27-3004-2, General Information - BSC. Alternate and additional code chart assignments are encountered in specific IBM machine environments. However, the data link control subset remains primarily the same and is fully supported by the 2602 (Ref. Sec. 3.8).

3.3 Synchronization and Time-Outs

Primary bit symbol synchronization is assumed to be accomplished by the modem employed in the data link. Specifically, it is necessary that RS-232-C signals DB, Transmitted Signal Element Timing, and DD, Receiver Signal Element Timing, be provided by the synchronous modem to effect proper 2602 bit clocking operation. For the special case of diagnostic turn-around, the bit clock is provided by the card.

		S/360 Main Storage Bit Positions 0, 1, 2, 3															
Bit Positions 4, 5, 6, 7		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
	Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NUL	DLE	DS		SP	&	-						{	}	\	0
0001	1	SOH	DC1	SOS						a	j	~		A	J		1
0010	2	STX	DC2	FS	SYN					b	k	s		B	K	S	2
0011	3	ETX	DC3							c	l	t		C	L	T	3
0100	4	PF	RES	BYP	PN					d	m	u		D	M	U	4
0101	5	HT	NL	LF	RS					e	n	v		E	N	V	5
0110	6	LC	BS	ECB / ETB	UC					f	o	w		F	O	W	6
0111	7	DEL	IL	PRE / ESC	EOT					g	p	x		G	P	X	7
1000	8		CAN							h	q	y		H	Q	Y	8
1001	9	RLF	EM						\	i	r	z		I	R	Z	9
1010	A	SMM	CC	SM		¢	!	|	:							
1011	B	VT				.	$	,	#						.		
1100	C	FF	IFS		DC4	<	*	%	@								
1101	D	CR	IGS	ENQ	NAK	(	)	_	'								
1110	E	SO	IRS	ACK		+	;	>	=								
1111	F	SI	IUS	BEL	SUB	|	¬	?	"								

Duplicate Assignment

Fig. 3.2.1 EBCDIC Character Assignments

To effect word sync, the received bits are collected into 8-bit groupings, called characters, and each new character is tested for the hexadecimal code word 32, termed SYN; the synchronization code for message transmissions. Once SYN establishes the proper character grouping, further character sync on receive is not required until the data link is terminated or turned around. During transmit mode, two SYN characters are inserted at the beginning of all message blocks, including intermediate transmission blocks. All messages are terminated with a single trailing pad character 'FF' prior to data link turnaround or terminations.

Four timeouts are provided by the 2602 system through the use of a software programmable counter on the card. These are as follows:

Transmit Timeout - A one-second timeout that establishes the rate at which sync-idle characters (SYN SYN) are inserted into the transmitted message after the initial sync characters are transmitted. The 2602 software ensures that the two-character sequence SYN SYN (or DLE SYN in transparent mode) is present in the transmitted message at nominal one-second intervals for combinations of block lengths and baud rates which allow block transmission times greater than one second.

Continue Timeout - A two-second timeout which becomes applicable in data link turnaround situations where a delay in transmitting or receiving data must be indicated before the time-out occurs. Specifically, for the transmit case, a transmitting station must transmit TTD, after receiving an acknowledgment for a previous block, if it cannot send the next block prior to the two-second time-out. In the receive case, a receiving station must transmit WACK as an acknowledgment if it is unable to receive further data in the two-second period. Continue time-out and error recovery procedures associated with it are provided by the 2602 software.

Receive Timeout - A three-second timeout associated with link turnaround reply and receive procedures. A transmitting station, on reverting to receive mode, will wait up to three seconds without the reception of sync-idle characters (SYN SYN) before error recovery procedures are initiated. If a station is receiving a message, it will wait up to three seconds without receiving SYN SYN (or DLE SYN in transparent mode) before the 2602 controller notifies the system software of the error. Error recovery procedures are performed by the 2602 software.

Disconnect Timeout - A nominal 20 second timeout optionally used on switched networks to prevent a station from holding a connection for prolonged periods of inactivity. The 2602 software will provide this timeout capability by tallying integer (6 to 7) counts of the three-second timeout. The normal control link procedure, after the 20 second period, is to transmit the disconnect sequence DLE EOT and then, optionally, set Data Terminal Ready (CD) false. The 20 second timeout is primarily used with switched networks which are supported with the Automatic Answer feature. In this case, disconnect occurs when Data Terminal Ready (CD) is set false.

3.4 Bit Error Detection, Format Errors

Bisync data link discipline employs an error checking feature termed cyclic redundancy checking (CRC). The CRC is a binary accumulation of bits which is the remainder of the modulo-two division of applicable message bits by a generating polynomial. The transmitter sends the resultant check bits and the receiver compares them with a similar division it has performed on the received message. Non-comparison indicates that a single, double, or odd-bit error has occured in the received message.

The 2602 provides a hardware generation and checking of the CRC which uses IBM's BSC CRC-16 and alternately, for the European user, the CCITT-CRC. The polynomials are shown below:

CRC-16 : $X^{16} + X^{15} + X^2 + 1$

CRC-CCITT : $X^{16} + X^{12} + X^5 + 1$

The resultant CRC is a two-character check word termed the BCC. The BCC is transmitted following the control characters ETB, ETX, or ITB and compared against the accumulated BCC. A detected BCC error is indicated to the 2602 software by an interrupt and the setting of a status bit. Error-recovery procedures are performed by the software. In the event a control link or format error occurred simultaneously with a detected BCC error, the error-recovery procedures associated with the former would take precedence.

Format errors occur when the received control characters do not constitute a legitimate sequence. Typical examples are shown in Section 3.12.

When a format error is detected by the 2602 hardware, the format error status bit is set and an interrupt is sent to the processor. The software will initiate error recovery procedures.

3.5 Addressing

Controller addressing is provided on each card by strap connections to meet the following address requirements:

a. Card device address.

b. Concurrent I/O address.

c. Interrupt I/O address.

The range provided by the straps is from 00 to 1F. The preferred device addresses, however, will be constrained to the range 10-13 hex. User addressing, such as encountered in multilink operation, will be provided by the 2602 software.

3.6 Diagnostic Provisions

Turn-around diagnostic procedures will be primarily employed to verify proper operation of the 2602 hardware. Turn-around may be instituted by replacement of the modem cable with a specially provided cable designed to affect the data and control signal turn-around. Diagnostic testing with the special cable installed requires a cooperative removal of the terminal from the transmission link; however, it does provide a complete verification of the 2602 electronics, including interface electronics. Another A20002602 board is required for this test.

The 2602 diagnostic supports the turn-around modes and verifies that the 2602 electronics:

a. transmits and receives error-free data,

b. emits proper modem control signals and senses the return modem status signals,

c. generates and checks the BCC characters and initiates an error condition on reception of an erroneous BCC.

3.7 Automatic Answer (AA)

Automatic answer is a standard feature provided by the 2602 controller. In Auto Answer, the signal Data Terminal is normally set true. The modem, on receiving a Ring indication, answers the incoming call by establishing the switched network connection prior to issuing the signal Data Set Ready. If the 2602 software ascertains that no switched network connection was made within 20 seconds, the call is terminated and error recovery procedures are initiated.

3.8 Data Link Control

The 2602 will recognize and act on the following data link single-byte control characters:

EBCDIC Character	Hex
SYN	32
SOH	01
STX	02
ITB	1F
ETB	26
ETX	03
EOT	37
ENQ	2D
NAK	3D
DLE	10
BEL*	2F

*BEL is not a BSC data link control character; however, in 2780 and 3780 emulation environments the character may appear as a legitimate single-byte message. As such, the 2602 will recognize and pass BEL to the software.

6. Set a status bit and an error interrupt if the time-out timer runs out.

7. Set a status bit and an error interrupt if a format error is encountered in a control sequence, or a data overrun occurs.

3.9 Data Transfer Modes

The controller transfers all non-data bytes and control codes by employing the byte I/O interface. All data and link-control character transfers are accomplished using the concurrent I/O mode and interface.

In the byte I/O mode, function bytes, control codes, mask bytes and time-out timer settings are transferred to the controller during byte I/O output mode. During byte I/O input mode, status bytes are transferred to the processor. In both cases, transfer is initiated by the processor.

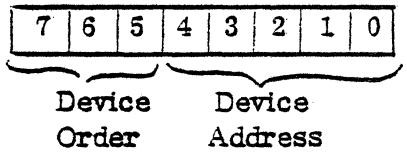
In concurrent I/O mode, data transfer is initiated by the 2602 controller and completion of the transfer is signalled by activating the external interrupt input.

In transmit mode, data is transferred one byte at a time from the processor to the output buffer register and from there to the transmit register. This double buffering feature allows a full character time for the next byte to be transferred to the output register.

In receive mode, similar double-buffering considerations hold, allowing up to a character time for transfer of the receive byte to the processor.

3.10 Device Order Codes

To set the primary control mode of the 2602 controller, the processor transfers a device order to the controller in byte I/O mode. The device order is the second byte of an I/O instruction and contains a three-bit device order and a five-bit device address:



Additionally, the following double-byte link control characters will be recognized by the 2602:

EBCDIC Character	Hex
ACK 0	10 70
ACK 1	10 61
WACK	10 6B
RVI	10 7C
TTD	02 2D
DLE EOT	10 37
SOH ENQ	01 2D
DLE ENQ	10 2D

The primary message control features performed by the 2602 are as follows:

1. Recognize and pass to the software, proper message sequences devoid of sync, transparent sync, pad and BCC characters.

2. Recognize specific control link characters in both transmit and receive message to effect the proper computation of the BCC characters. In receive mode, compare the computed BCC characters against the received BCC characters and set a status bit and error interrupt if they do not match. In transmit mode, compute the BCC and insert it into those messages that require them.

3. End each message with a trailing pad character ('FF').

4. Insert in the transmit message, where data transfer delays are encountered, SYN SYN characters (or DLE SYN in transparent mode) to hold the data link.

5. Set a status bit and an interrupt if a message termination occurs.

NOTE:

The software routine should insert two sync characters (SYN SYN) in the beginning of a message stream.

The 2602 Controller examines the device address portion and if it is the same as the device address of the card, the device order is accepted. Acceptable device addresses for the 2602 must lie in the range hex 10-13.

The device order definitions as they apply to the 2602 are shown in the table in Section 3.10.1. If a transfer is implied by the order code, the direction is established by the I/O control lines.

3.10.1 2602 Device Orders

Device Order	Operation	Description
0	Timeout Timer	Sets and releases to count a timeout timer whose range is from zero to three seconds. Causes Timeout Timer status bit to be cleared.
1	Status/Function	Causes a status byte to be transferred from the controller (on I/O input) or a function byte to be transferred to the controller (on I/O output).
2	Concurrent Input With Interrupt	Causes controller to enter receive (sync search) mode, arms the interrupt logic, and sets alternate status bit 0 true. Valid receive characters are transferred to memory. An interrupt will occur only if disconnect order code (Hex 4) is issued or an interrupt condition is encountered (see paragraph 3.11.3 Interrupts).
3	Arm Interrupt and Set Mask	Arms the interrupt logic, transfers an interrupt mask byte allowing the controller to interrupt if the mask conditions are satisfied and sets alternate status bit 2 true.

Device Order	Operation	Description
4	Disconnect	Clears Concurrent I/O In and Concurrent I/O Out states, sets alternate status bit 4 true, causes controller to enter idle mode (no operations performed), and generates an interrupt if interrupt logic is armed.
5	Disarm Interrupt	Inhibits controller from executing any interrupt and releases priority to lower devices. Order is sent on I/O output.
6	Concurrent Output With Interrupt	Causes controller to enter transmit mode, arms the interrupt logic, and sets alternate status bit 1 true. Valid characters are transferred from memory to the transmitter register. An interrupt will occur only if disconnect order code (Hex 4) is issued or an interrupt condition is encountered (see paragraph 3.11.3 Interrupts).
7	Alternate Status/ Function	Causes controller to transfer alternate status byte to the processor. Order causes an I/O input, or a function byte to be transferred to the controller.

In the table shown in Section 3.10.2, a summary of Micro 1600 instructions which effect the 2602 controller is presented. Device address Hex 10 is assumed.

3.10.2 Instruction List Summary

STATUS TRANSFER

Hex	Mnemonic	Instruction
3130	IBA	Input Status Byte to A Register
3230	IBB	Input Status Byte to B Register
3330	IBM	Input Status Byte to Memory

ALTERNATE STATUS TRANSFER

31F0	IBA	Input Alternate Status Byte to A Register
32F0	IBB	Input Alternate Status Byte to B Register
33F0	IBM	Input Alternate Status Byte to Memory

FUNCTION TRANSFER

3930	OBA	Output Function Byte from A Register
3A30	OBB	Output Function Byte from B Register.
3B30	OBM	Output Function Byte from Memory

ARM INTERRUPT & SET MASK

3970	OBA	Arm interrupt and output mask from A Register.
3A70	OBB	Arm interrupt and output mask from B Register.
3B70	OBM	Arm interrupt and output mask from Memory.

DEVICE ORDERS

3X10	OBZ	Output Timer Byte
3X50	OBZ	Enable Block Input Mode
3XD0	OBZ	Enable Block Output Mode
3X90	OBZ	Disconnect
3XB0	OBZ	Disarm Interrupt
3XF0	OBZ	Software Master Reset

(X = 9 or A or B) (Z = A or B or M)

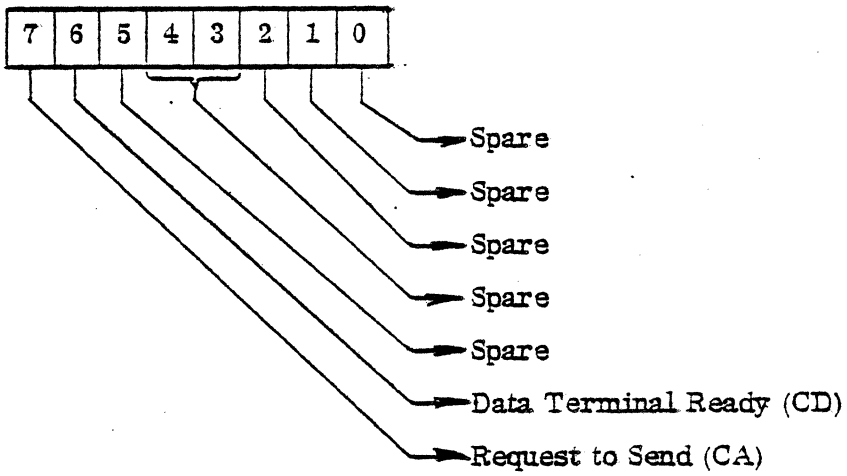
3.11 Functions, Status and Interrupts

3.11.1 Function Byte

A byte of data, termed a function byte, is transferred to the 2602 controller in Byte I/O mode by the device order Hex 1.

The function byte specifies the modem control signals and the controller I/O mode.

Function Byte



Data Terminal Ready (CD) - Modem control signal.

Request to Send (CA) - Modem control signal.

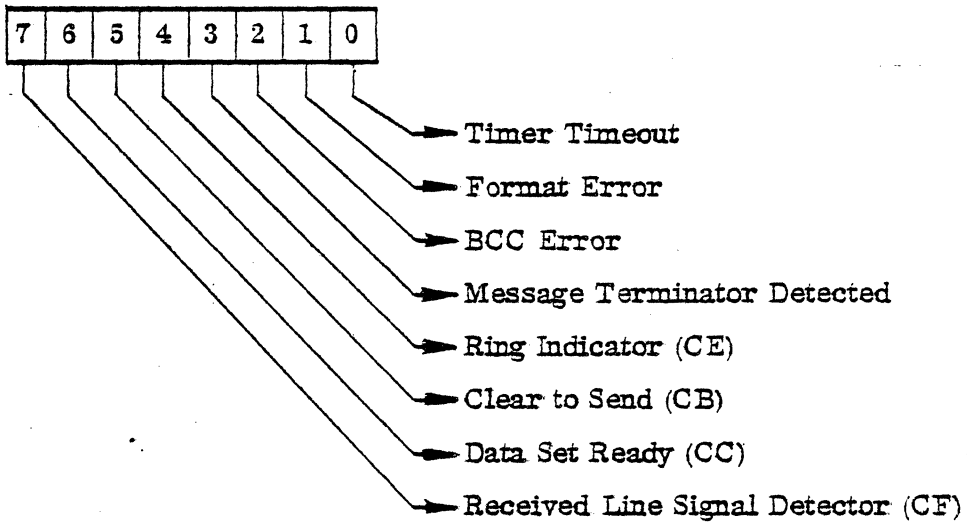
Alternate Function Byte

The alternate function byte is used as a Software Master Reset to the controller board. Modem terms CA and CD are not affected.

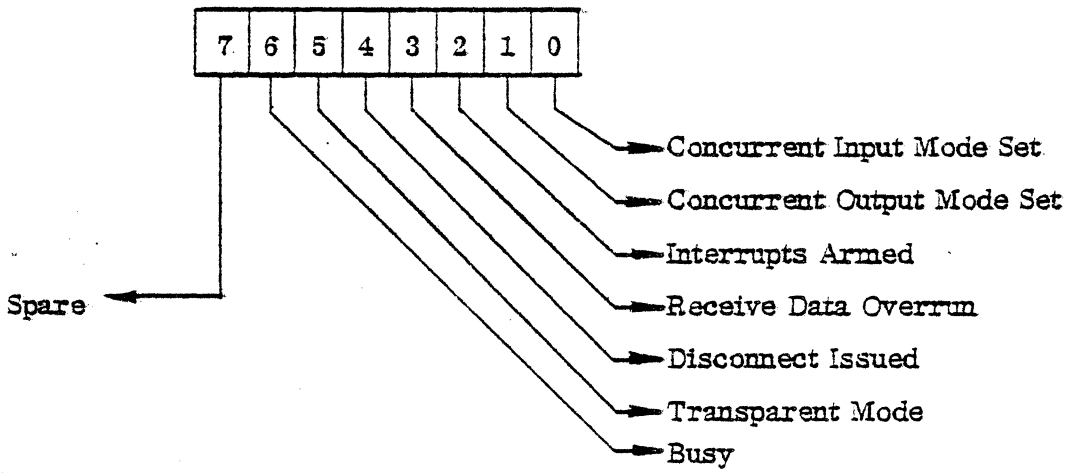
3.11.2 Status Bytes

Two status bytes are maintained by the 2602 controller. The main status byte is transferred from the controller to the processor whenever device order Hex 1 is issued. The alternate status byte is transferred with device order Hex 7.

Status Byte



Alternate Status Byte



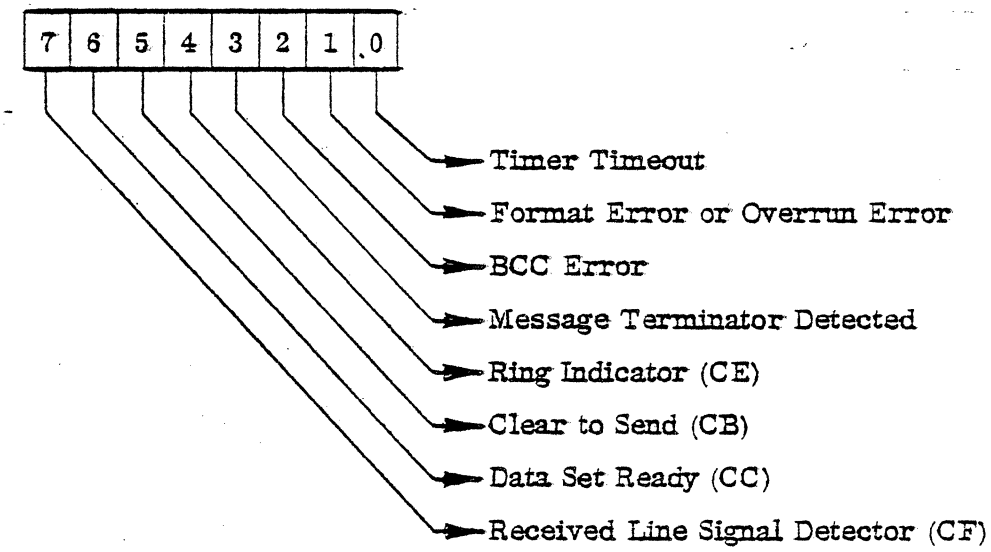
Reception of a message terminator will cause status bit 3 to set, Concurrent I/O out and Concurrent I/O in to reset, and an interrupt to be generated if armed and the mask bit is set. The order code Disconnect (hex 4) causes the Concurrent Input mode (hex 2) and Concurrent Output mode (hex 6) to reset and alternate status bits 0 and 1, to reset. Restarting the timeout timer (order code zero) will cause status bit 0 to go false. Accessing the status bytes will cause those modem sense bits to be set false whose signal is false, and clears the remaining status (or alternate status) bits. Transparent mode is solely controlled by the 2602 hardware and cannot be cleared by the software.

3.11.3 Interrupts

The processor can be interrupted on byte I/O operations or at the end of concurrent I/O operations if the interrupt has been armed.

All interrupt conditions, not concerned with concurrent I/O, are maskable. The mask byte is transferred to the controller on order code 3.

Interrupt Mask Byte

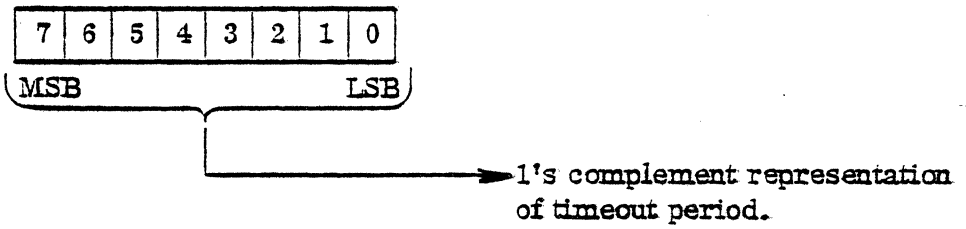


For interrupt mask bits 7 thru 4, any change in the signal will cause an interrupt if the associated mask bit is set. Interrupt bit 2 specifies that a BCC Error will be sensed as an interrupt. The runout of the timeout timer is specified by bit 0. Format error, bit 1, implies the reception of an improper control character sequence, or that a receive character was not transferred in time to prevent overflow. Message terminator Detected indicates that a control character (or characters) was received which would cause message termination or link turn-around; e.g., EOT, ENQ, DLE ENQ, DLE EOT, ETB, ETX, etc. Interrupt mask is reset by issuing an alternate function Reset command.

3.11.4 Timeout Timer Byte

The order code zero, when executed, transfers a byte to the timeout timer and releases it to count. For hardware purposes, the actual byte transferred is the binary 1's complement of the timeout period desired. Clock period is 12.3 milliseconds.

Timeout Timer Byte



Desired Timeout Period	Timeout Byte (Hex) Transferred
3 seconds	ØØ
2 seconds	4D
1 second	9E
12 milliseconds (min.)	EF

3.12 Functional Description

Two PROMS store a control program of 256 eight-bit words (decodable micro-instructions). The microprocessor is a three instruction machine executing most of the subroutines in a linear fashion. The basic clock period is 1.6 microseconds which is rapid enough for subsequencing inside the 9600 Baud rate (104 microseconds between characters), yet slow enough for the MOS devices.

Figure 1 shows a basic block diagram of the state sequencer and subsequencer section of the bisync controller. The eight-bit character word, sourced either from the MOS receiver register or the transmit buffer register, is decoded to one of 16 four-bit words in the state decoder PROM and applied as input to the state sequencer PROM. The other four inputs to the state sequencer are supplied by the subsequencer from a previous subroutine that has finished. The resulting four-bit word out of the state sequencer along with the signal CCOT (Concurrent Transmit Output) specifies one of 32 eight-bit starting locations of a subroutine in the 256-word control program.

Figure 2 shows a flow diagram, transmit or receive, of the control program. Each circle represents a subroutine, and the flow from one subroutine to another is dependent on the next word received and processed by the state sequencer. Flow diagrams are provided for each of the subroutines in Section 3.13.

Figure 3 shows specific flow of the state sequencer. The eight-bit control instruction performs specific operations depending on the state of bits six and seven which specify the instruction. Figure 4 lists the fields associated with them and a description follows.

The test and wait instruction looks at one-of-eight input to a MUX. If the input signal is false the address counter is prevented from being incremented causing the subsequencer to wait until the signal is true, then it will continue down the subroutine. Primarily the signals which enter into the test and wait MUX are concerned with the condition (full or empty) of interface registers.

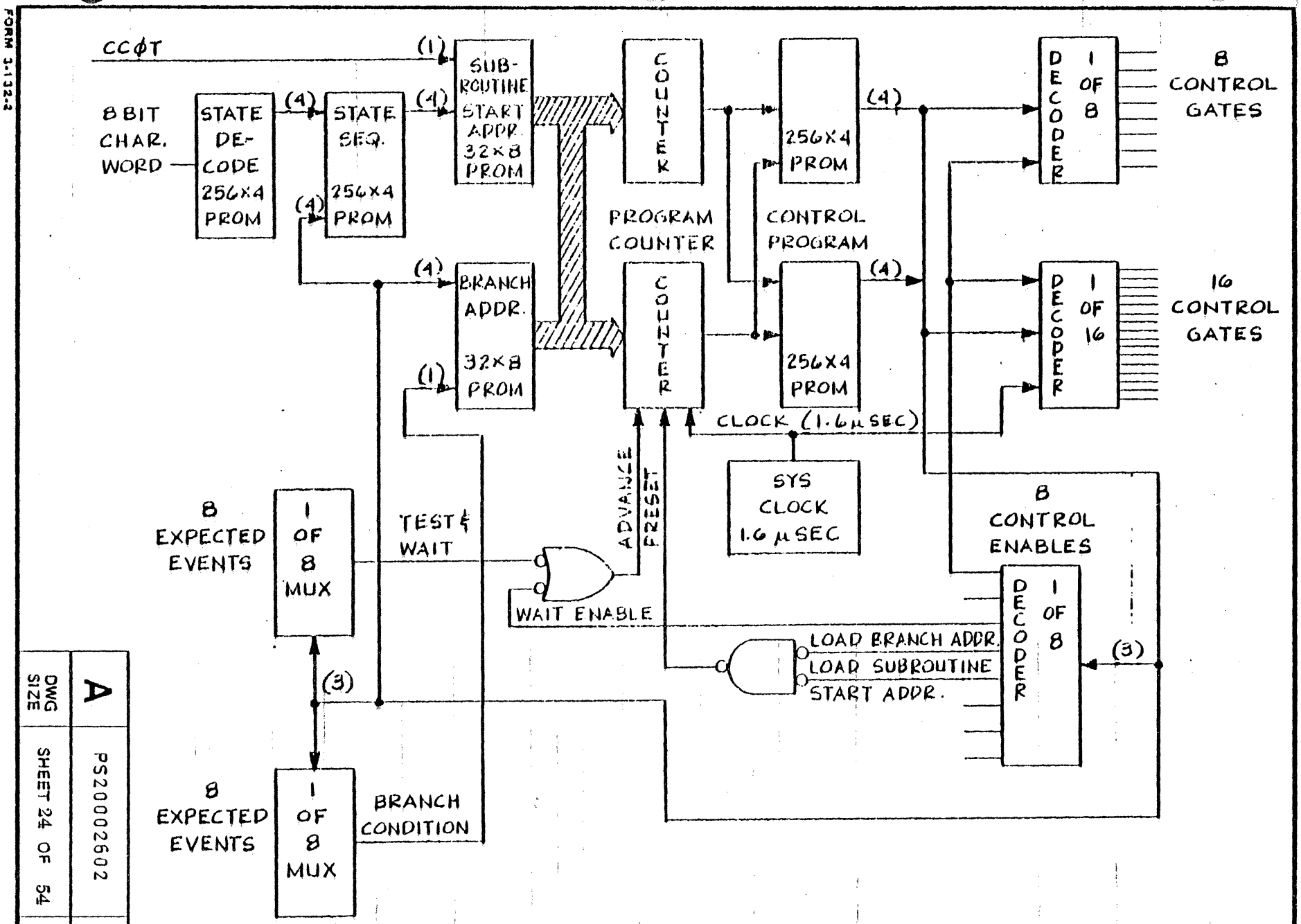


Figure 1. State Machine

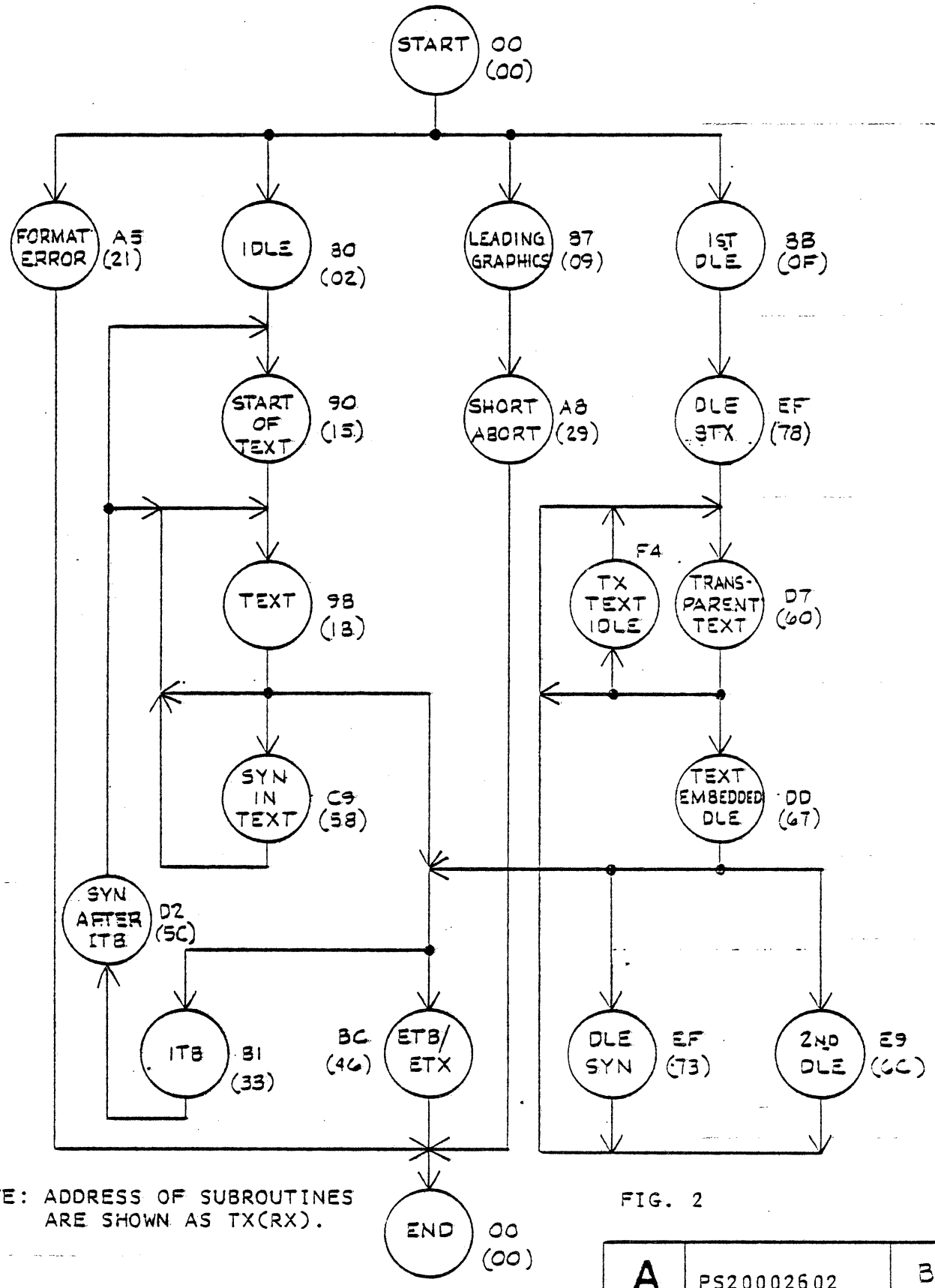
DWG SIZE	A
SHEET 24 OF 54	PS20002602
REV	B

The test and branch instruction looks at one-of-eight signals on which a branch within the subroutine or between subroutines may be taken. For each branch condition, one of two addresses may be specified, depending upon whether the tested signal is true or false. Bits MP0, 1, 2 and 3 specify the location in the branch address PROM along with BCND which contains the new address for the subsequencer.

The emit instruction provides fields which are encoded and supplies inputs to decoders used as control gates or control clocks. Field 'A' specifies the inputs to a three-to-eight decoder which has eight control gate outputs used primarily to control the MOS transmitter chip. Decode seven of this field, however, is used to perform a branch between subroutines, and Field 'B' at this time is used to input the four-bits to the state sequencer PROM. Field 'B' normally specifies the inputs to a four-to-sixteen decoder which is used to generate 16 separate control clocks. These control clocks are primarily used for loading registers, initiate transfers, keep house on CRC generator and MOS receiver chips.

Figure 5 shows a flow diagram of the overall data path. Output data from the computer is strobed into a latch. The data then goes through a MUX which selects this data or a check code, and then to the MOS transmit chip where it is broken down and transmitted serially. The word from the latch is also presented to the BCC generator and the state decoder. Input data is received by the MOS chip and strobed into a receiver buffer. The data from the receive buffer is presented to the BCC generator. Data from the MOS receive chip is presented to the state decoder.

The BCC generator starts accumulating on the first word after the start of text character and finishes on the end of text character. The accumulation is then added as two eight-bit words on to the end of the message or in the input mode, the last two words (BCC) are put into the generator and the result should be zero for a good received message.



NOTE: ADDRESS OF SUBROUTINES ARE SHOWN AS TX(RX).

FIG. 2

SUBSEQUENCER FLOW DIAGRAM OF SUBROUTINE LEVEL.

A	PS20002602	B
DWG SIZE	SHEET 26 OF 54	REV

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Test Input / Emit State	CHAR F	32 SYN 0	10 DLE 1	01 SOH 2	02 STX 3	1F ITB 4	26 ETB 5	03 ETX 6	37 EOT 7	2F BEL 8	2D ENQ 9	3D NAK A	70 ACK-1 B	6B WACK C	61 ACK-0 D	RUI E	Sub-Routine Addr. Tx	Sub-Routine Addr. Rx	Tx or Rx
0	1	0	2	3	3	1	1	1	6	6	6	6	1	1	1	1	80	02	Idle
1	1	1	2	3	3	1	1	1	1	1	6	6	1	1	1	1	87	09	Leading Graphics
2	5	5	5	5	F	5	5	5	6	5	6	5	6	6	6	6	8B	0F	1st DLE
3	4	9	4	4	4	7	8	8	4	4	6	4	4	4	4	4	90	15	STX/SOH
4	4	9	4	4	4	7	8	8	4	4	6	4	4	4	4	4	9B	1B	Normal Text
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A5	21	Format Error
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	A8	29	Short Abort
7	4	A	5	5	5	5	5	5	5	5	5	5	5	5	5	5	B1	33	ITB
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BC	46	ETB/ETX
9	4	9	4	4	4	7	8	8	6	4	4	4	4	4	4	4	C9	58	Normal Text embedded SYN
A	4	A	B	4	4	5	5	5	6	5	6	5	6	6	6	6	D2	5C	SYN after ITB
B	B	B	C	B	B	B	B	B	B	B	B	B	B	B	B	B	07	60	Transparent Text
C	D	E	D	D	D	7	8	8	6	D	6	D	D	D	D	D	DD	67	Embedded DLE
D	B	B	C	B	B	B	B	B	B	B	B	B	B	B	B	B	E9	6C	2nd DLE
E	B	B	C	B	B	B	B	B	B	B	B	B	B	B	B	B	EF	73	DLE SYN
F	B	B	C	B	B	B	B	B	B	B	B	B	B	B	B	B	EF	78	DLE STX

Figure 3. State Sequence Flow Diagram

TEST AND WAIT

7	6	5	4	3	2	1	0
0	0	0	0	0	A		

Word (Hex)	A	
00	0 - (DR)	New Character
01	1 - (RBE)	Receive Buffer Empty
02	2 - (TBF)	Transmit Buffer Full
03	3 - (THRE)	Transmit Buffer Empty
04	4 - (EOTC)	Last Bit of T_{x1} Character Time
05	5 - (MDET)	Match Detect
06	6 - (EOTC/)	Last Bit of T_x Character Time False
07	7 - (MDET/)	Match Detect False

Figure 4. Description of Subsequencer Instructions

TEST AND BRANCH

7	6	5	4	3	2	1	0
0	1	1	1	A			

Word (Hex)	A	
70	0 - (CCOT)	Concurrent Output
71	1 - (TBF)	Transmit Buffer Full
72	2 - (TBF)	
73	3 - (TBF)	
74	4 - (TBF)	
75	5 - (TRMD)	Transparent Mode
76	6 - (TRMD)	
77	7 - (TRMD)	
78	8 - (CCOT)	
79	9 - (TBF)	
7A	A - (TBF)	
7B	B - (TBF)	
7C	C - (TBF)	
7D	D - (TRMD)	
7E	E - (TRMD)	
7F	F - (TRMD)	

Figure 4 (Cont'd)

EMIT

7	6	5	4	3	2	1	0
1	B				A		

Word (Hex)	A	
80	0 - NO OPERATION	
81	1 - (LPAD/ DRR/)	Load Pad/Data Ready Reset
82	2 - (SYN/)	Load SYNC Character
83	3 - (LDLE/)	Load DLE Character
84	4 - (LTXC/)	Transfer Character to T_X Register
85	5 - (LCR1/)	Transfer BCC1 to T_X Register
86	6 - (LCR2/)	Transfer BCC2 to T_X Register
87	7 - (LDSS/)	Load Subroutine Branch Address

Word (Hex)	B	
80	0 - NO OPERATION	
88	1 - (LRBR/)	Transfer Character to R_X Buffer
90	2 - (ICHI/)	Initiate Character Transfer to Memory
98	3 - (ICHO/)	Initiate Character Transfer from Memory
A0	4 - (CCIOR/)	Reset Concurrent I/O Request
A8	5 - (CBCC/)	Clear BCC Generator
B0	6 - (GBCC/)	Generate BCC Check Code
B8	7 - NO OPERATION	
C0	8 - (MTDP/)	Set Message Terminator Detected
C8	9 - (FMEP/)	Set Format Error
D0	A - (SRCH/)	Initiate SYNC Search
D8	B - (BCEP/)	Check for BCC Error
E0	C - (TRMP/)	Set Transparent Mode
E8	D - (RTRM/)	Reset Transparent Mode
F0	E - (RTOT/)	Restart Timeout Timer
F8	F - (RTBF)	Reset Transmit Buffer Full

Figure 4. (Cont'd)

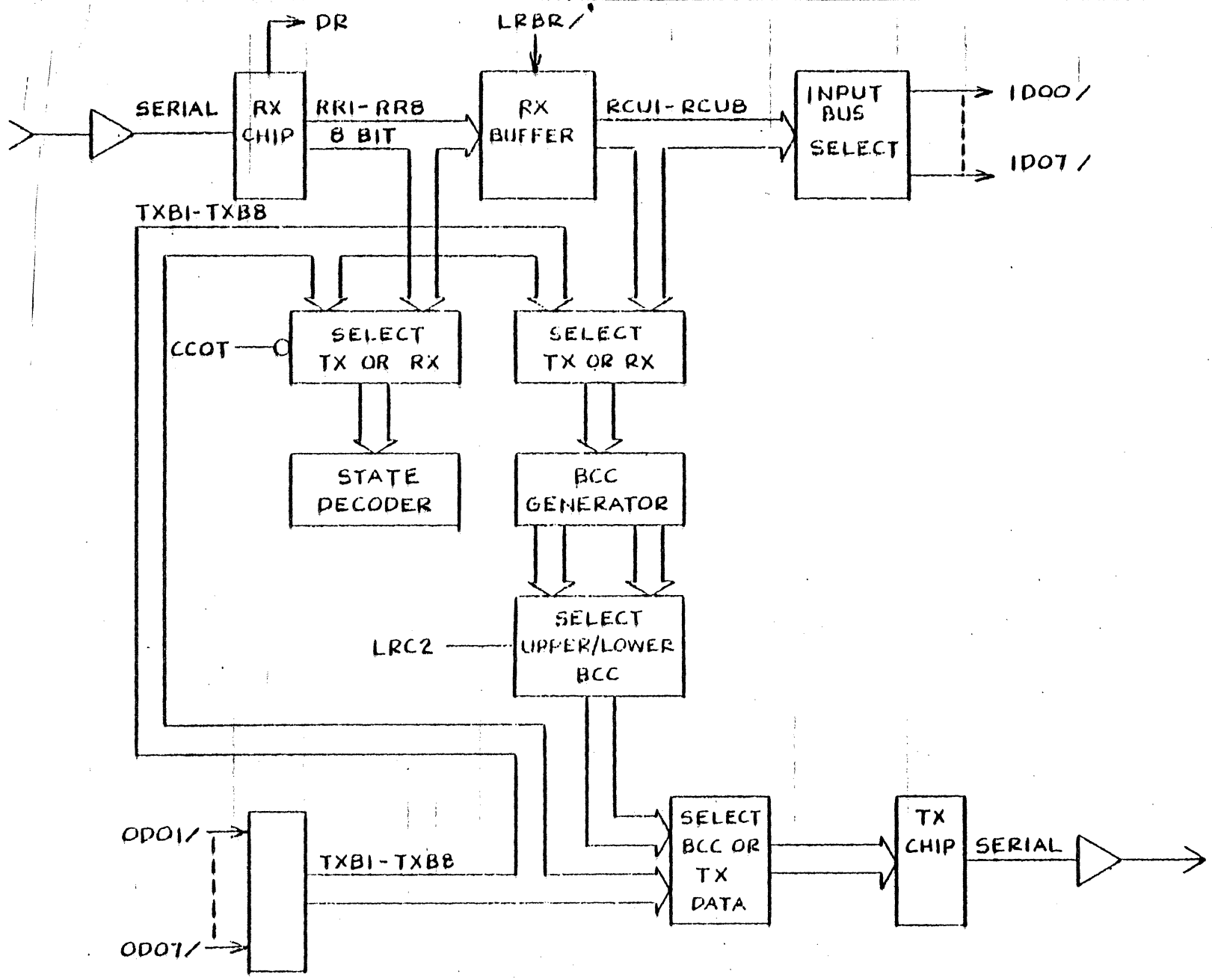
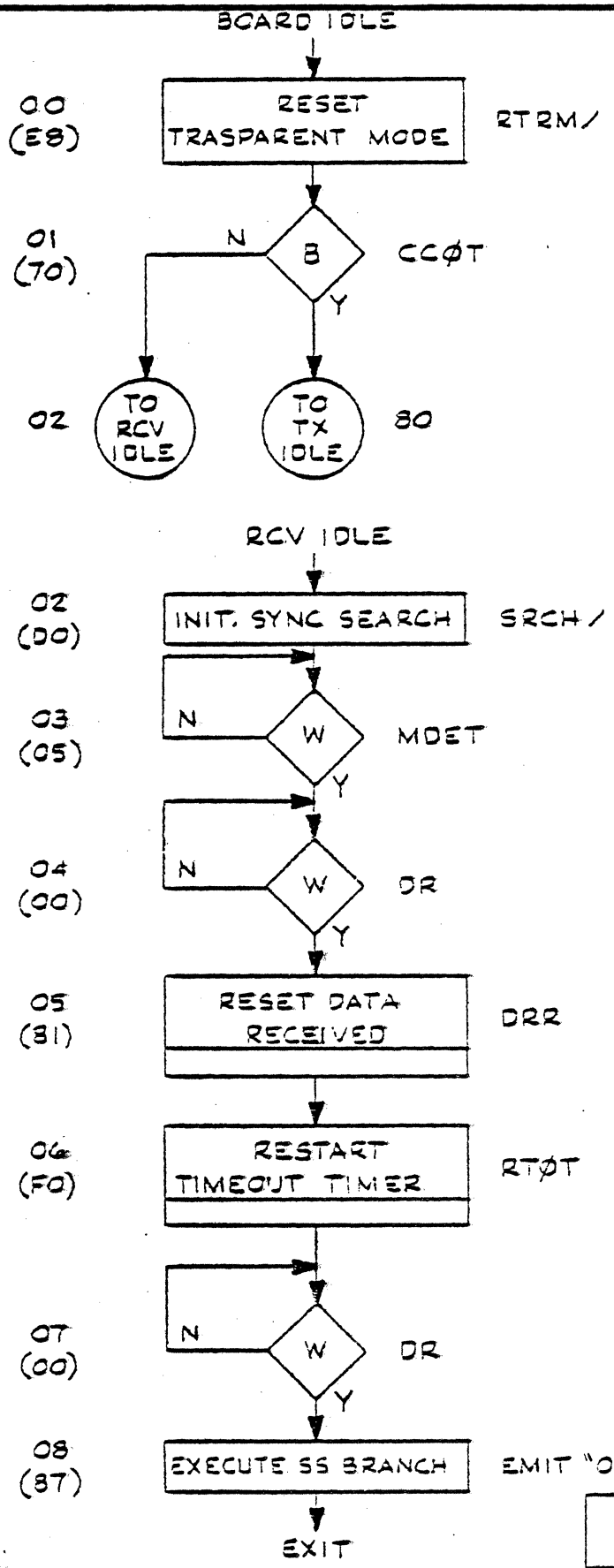


Figure 6. Data Flow Diagram

DWG SIZE	A	PS20002602	B
SHEET 31 OF 54			
REV			

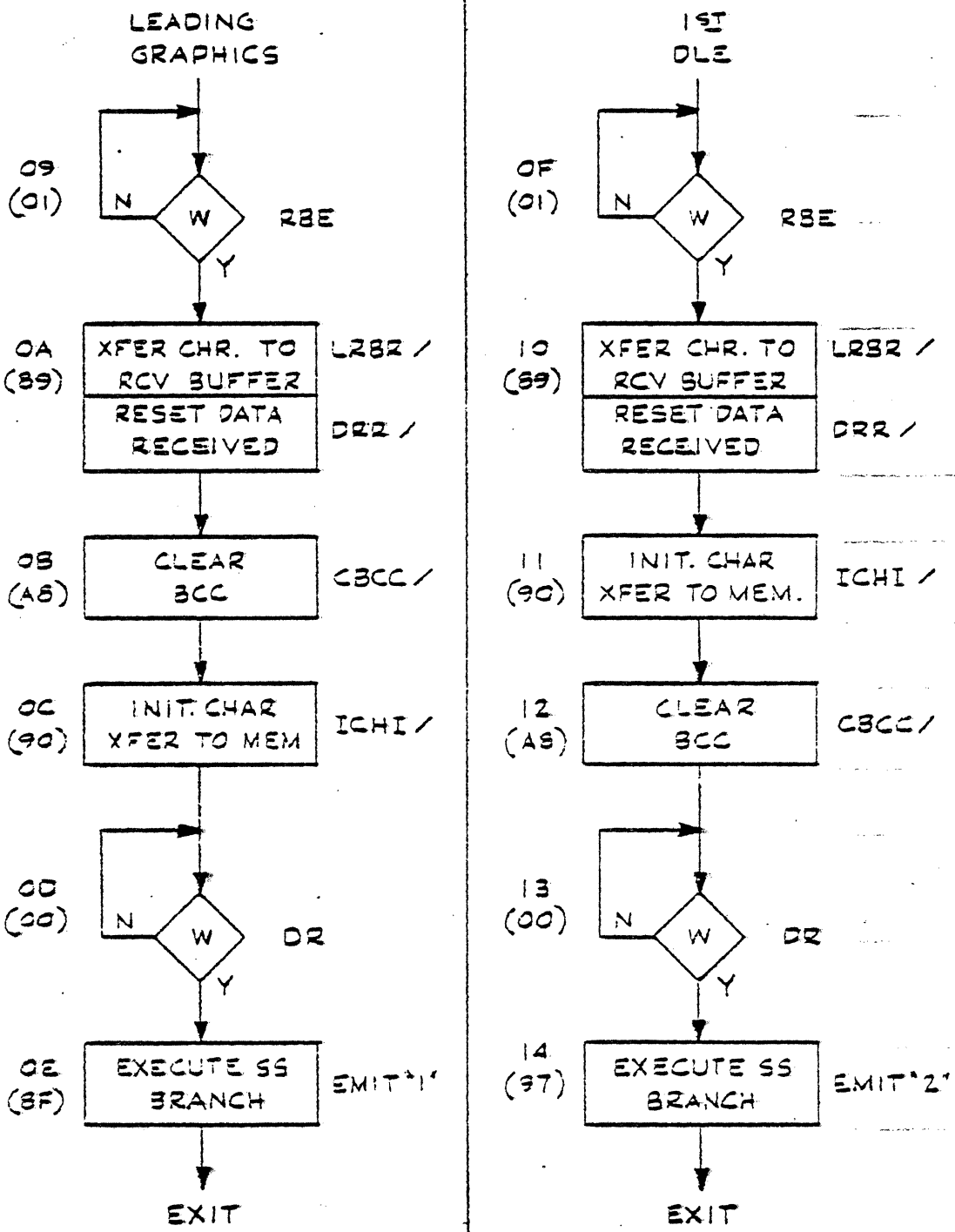
3.13 Sequencer Flow Diagrams

Note address is shown beside each instruction with the Hex value of the instruction in parenthesis.

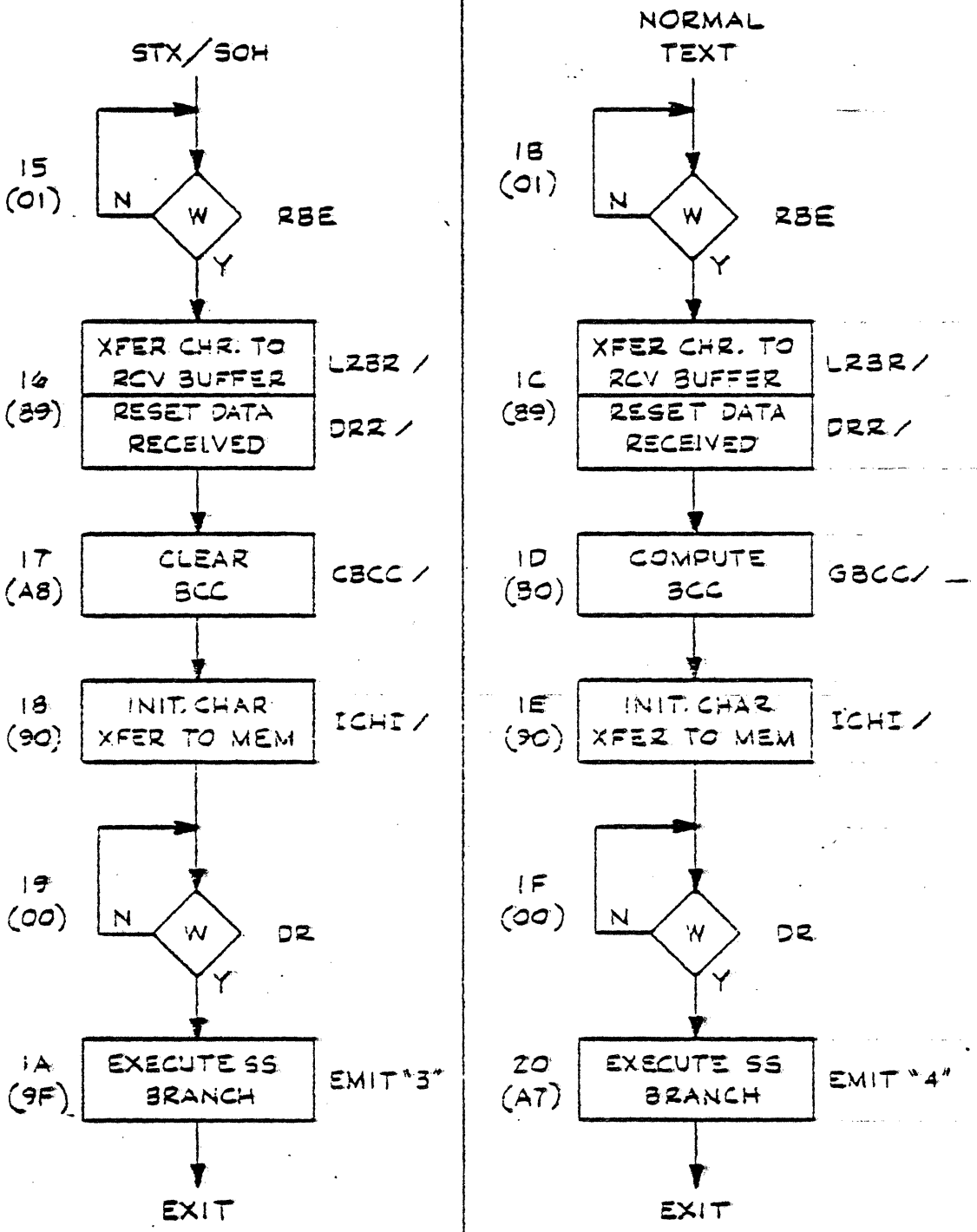


A	PS20002602	B
DWG SIZE	SHEET 33 OF 54	REV

FORM 3-132-2

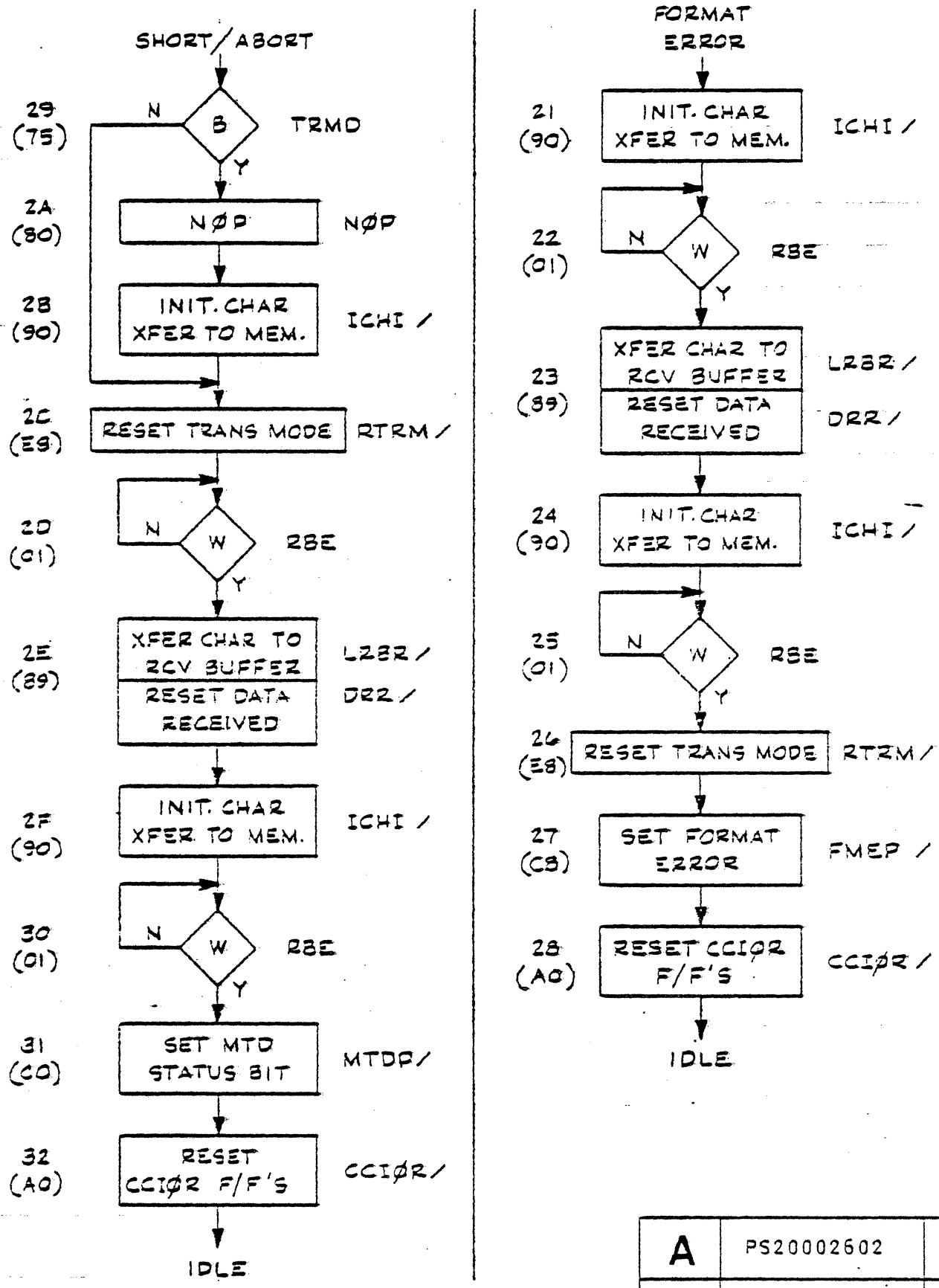


A	PS20002602	B
DWG SIZE	SHEET 34 OF 54	REV



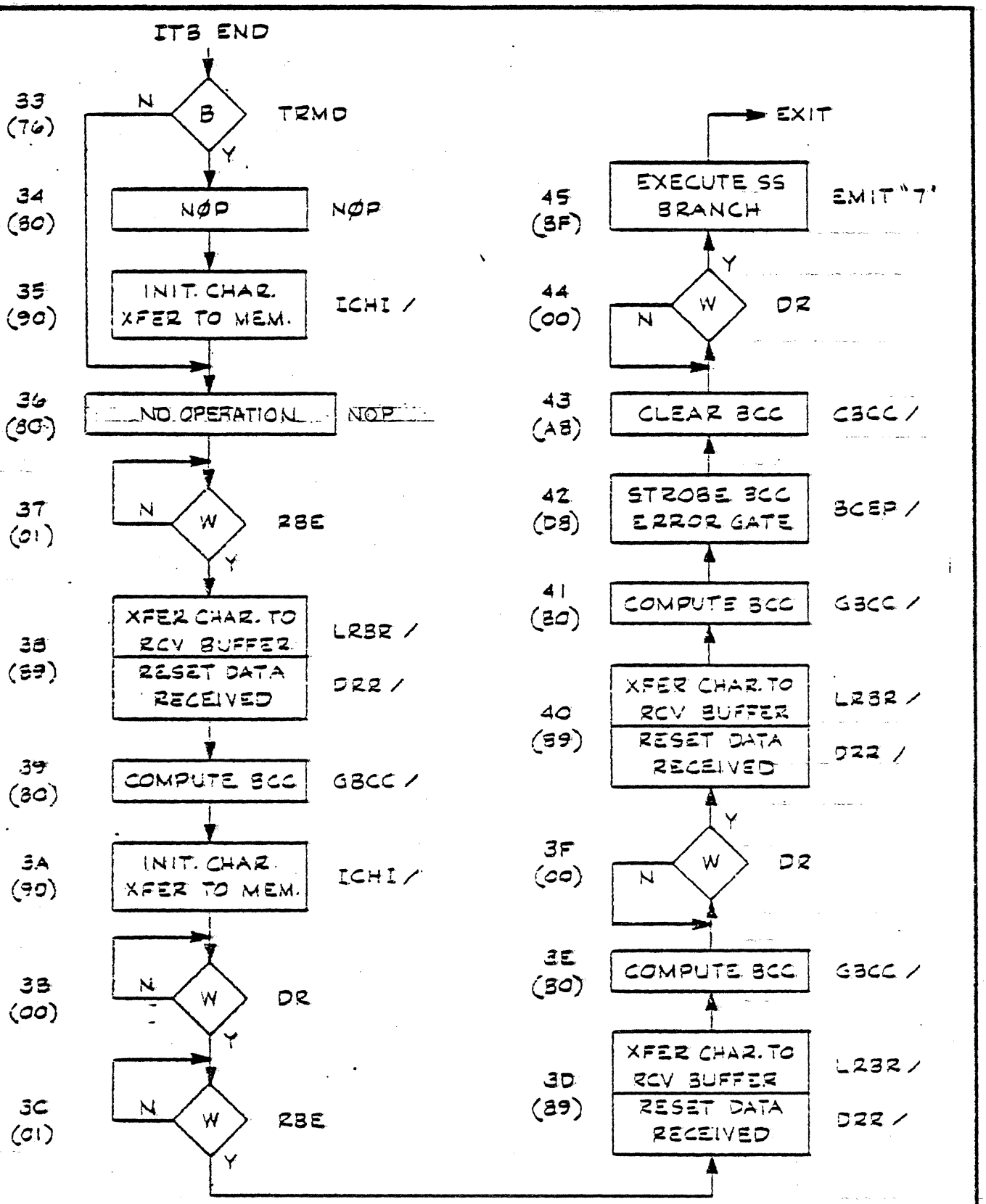
A	PS20002602	B
DWG SIZE	SHEET 35 OF 54	REV

FORM 3-132-2



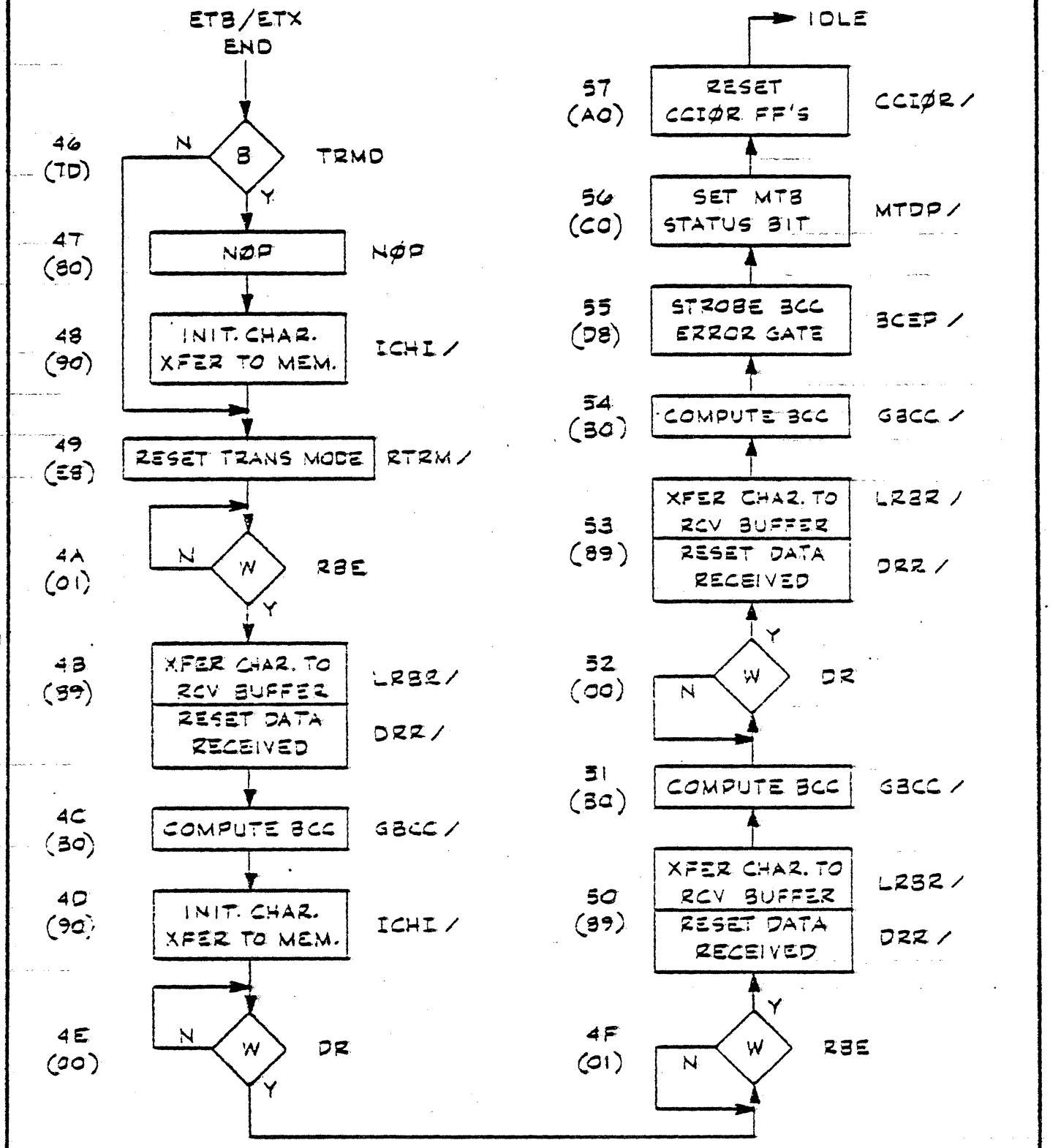
A	PS20002602	B
DWG SIZE	SHEET36 OF 54	REV

FORM 3-132-2



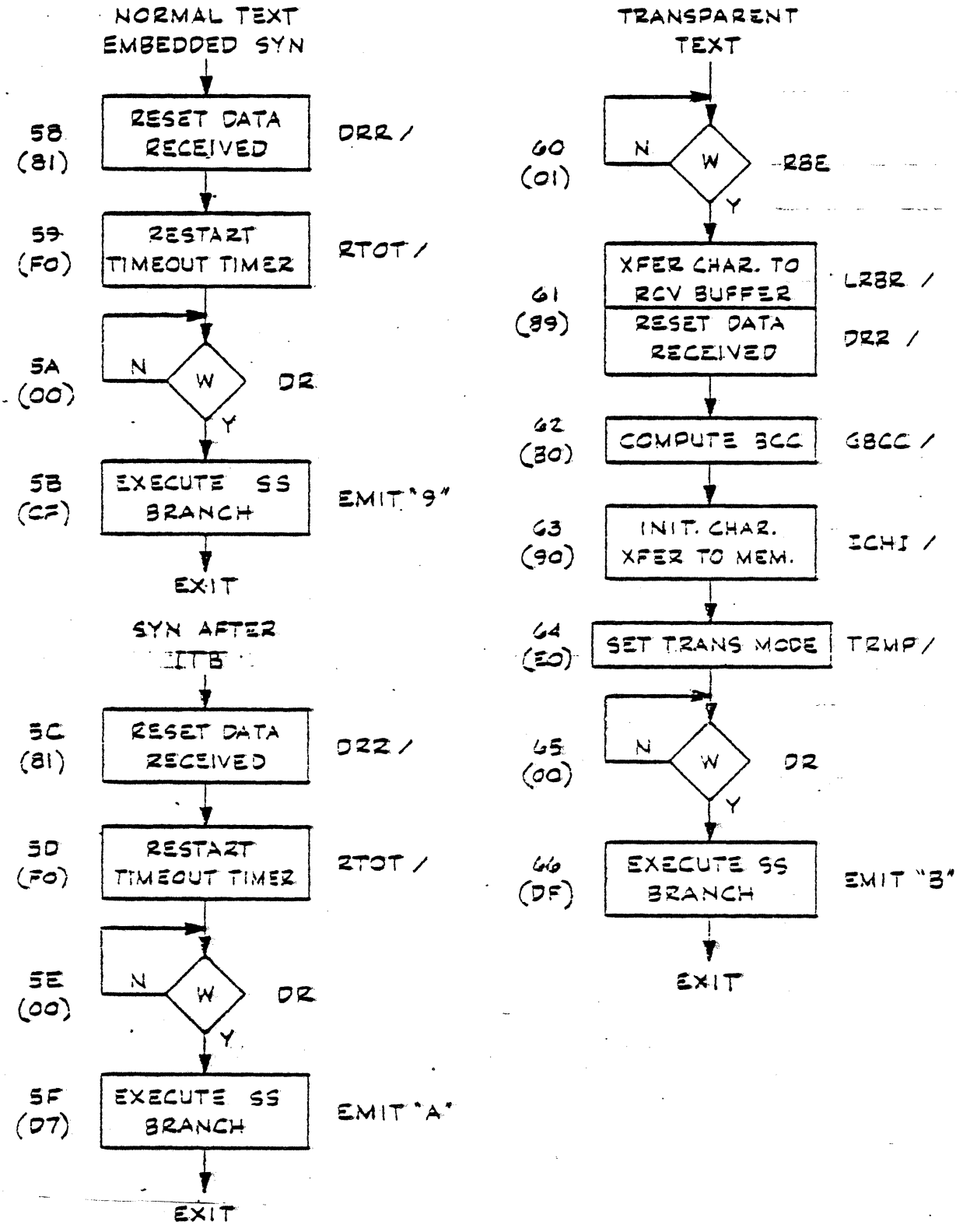
A	PS20002602	B
DWG SIZE	SHEET 37 OF 54	REV

FORM 3-132-2



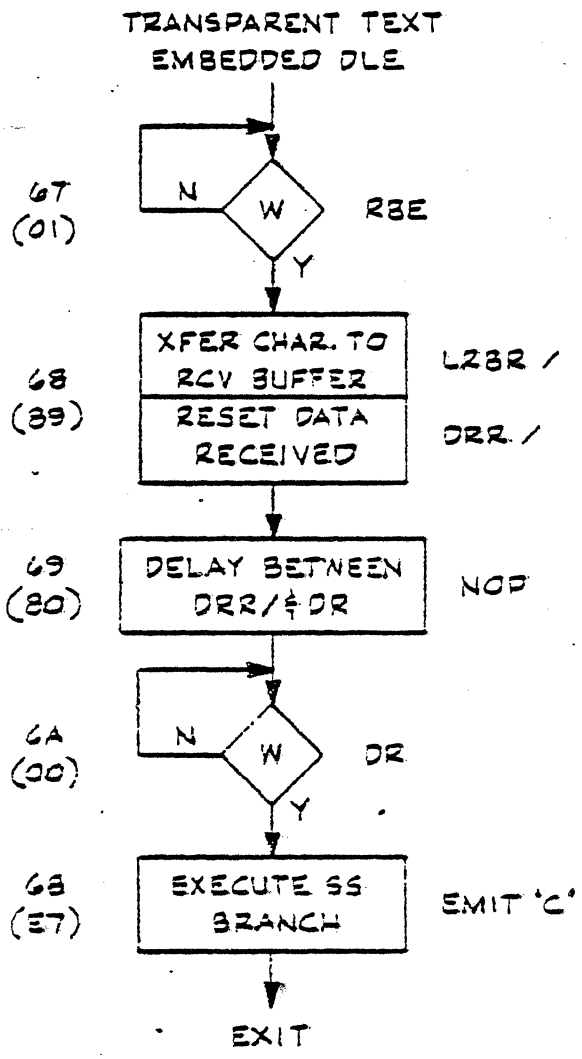
A	PS20002602	3
DWG SIZE	SHEET 38 OF 54	REV

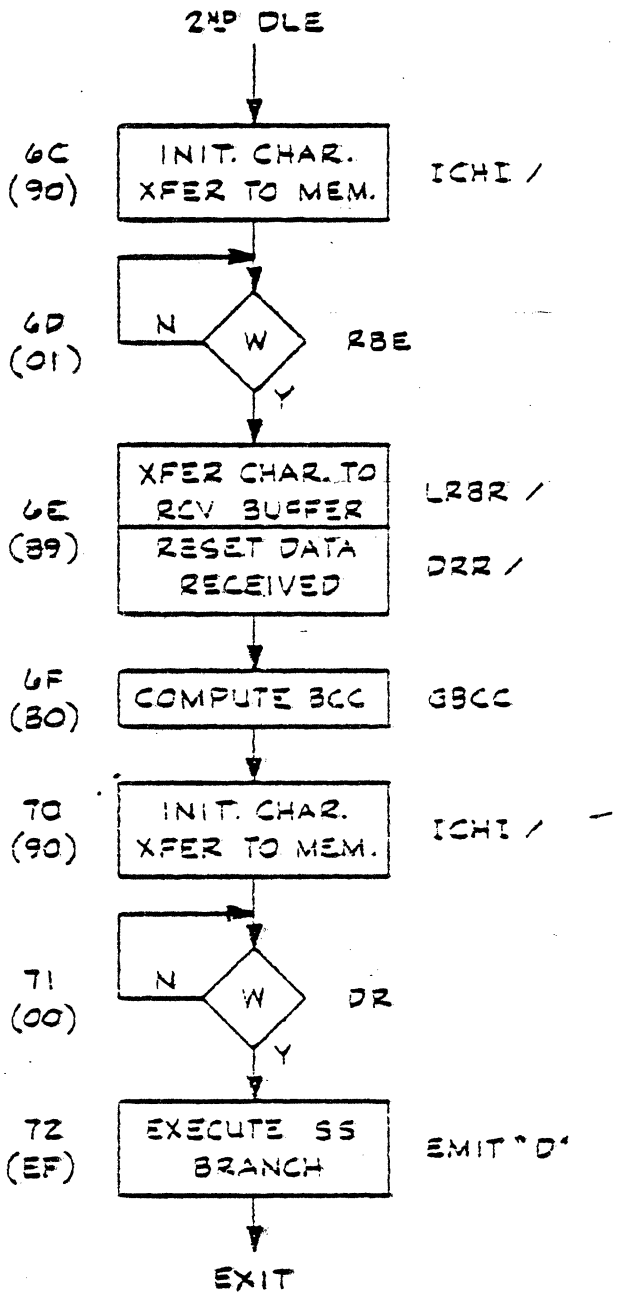
FORM 3-132-2



A	PS20002602	B
DWG SIZE	SHEET 39 OF 54	REV

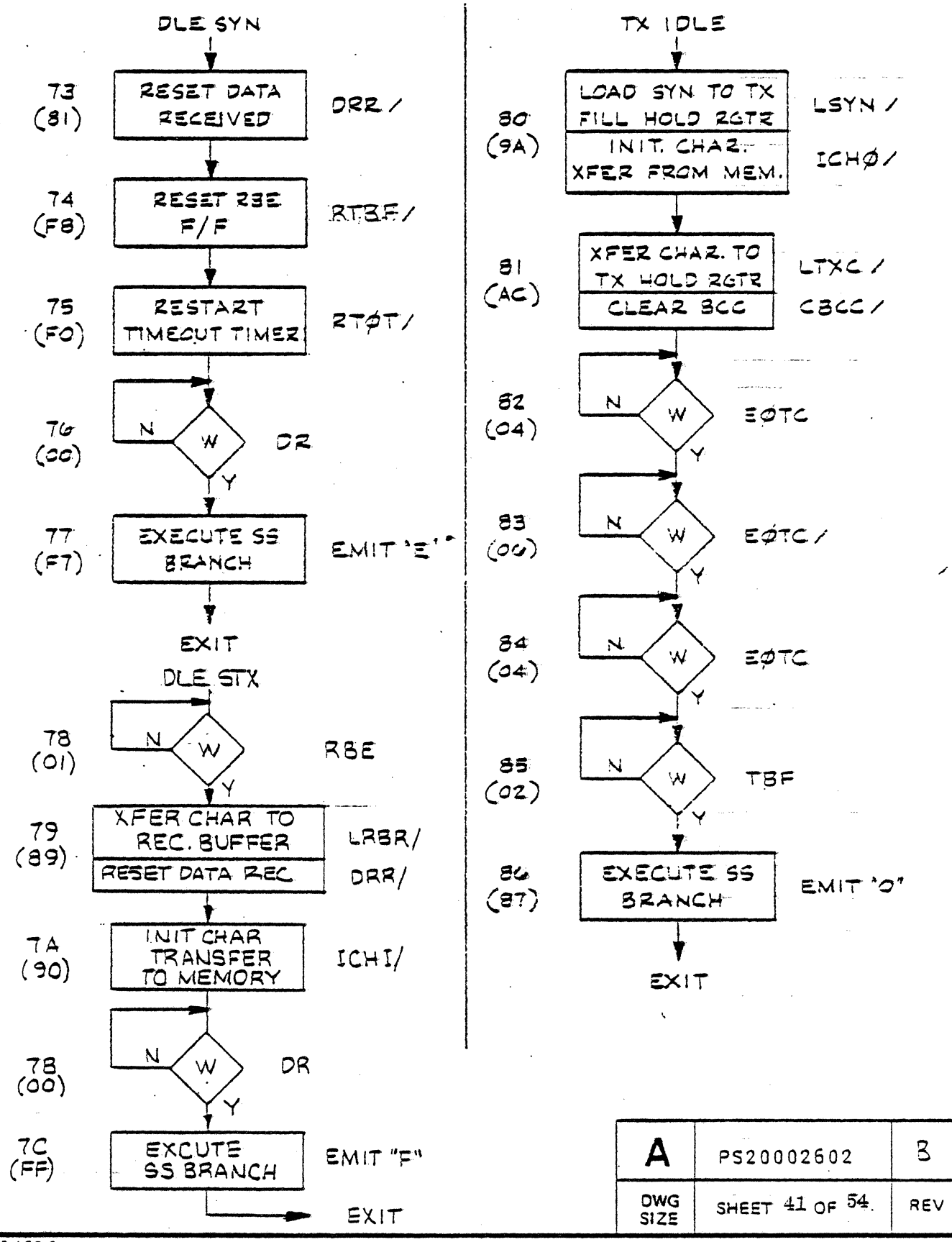
FORM 3-132-2





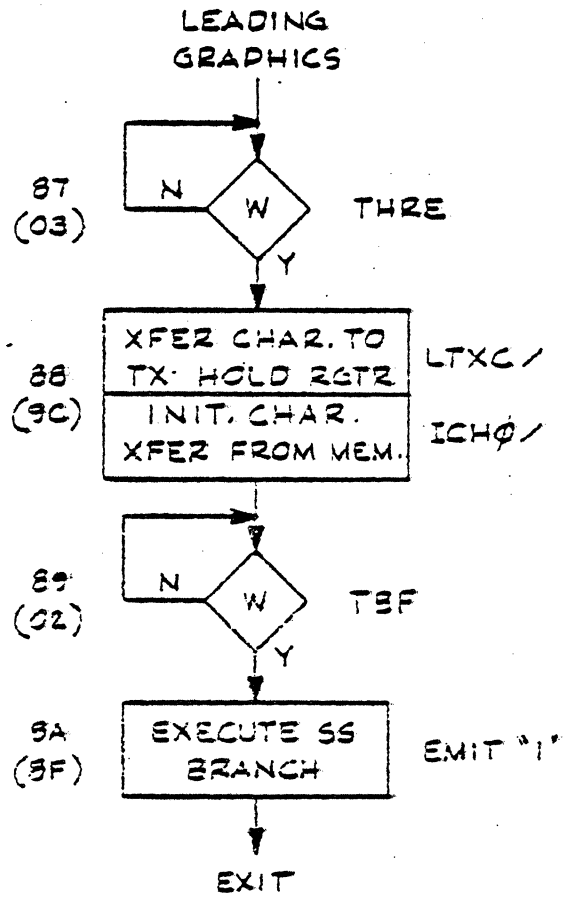
A	PS20002602	B
DWG SIZE	SHEET 40 OF 54	REV

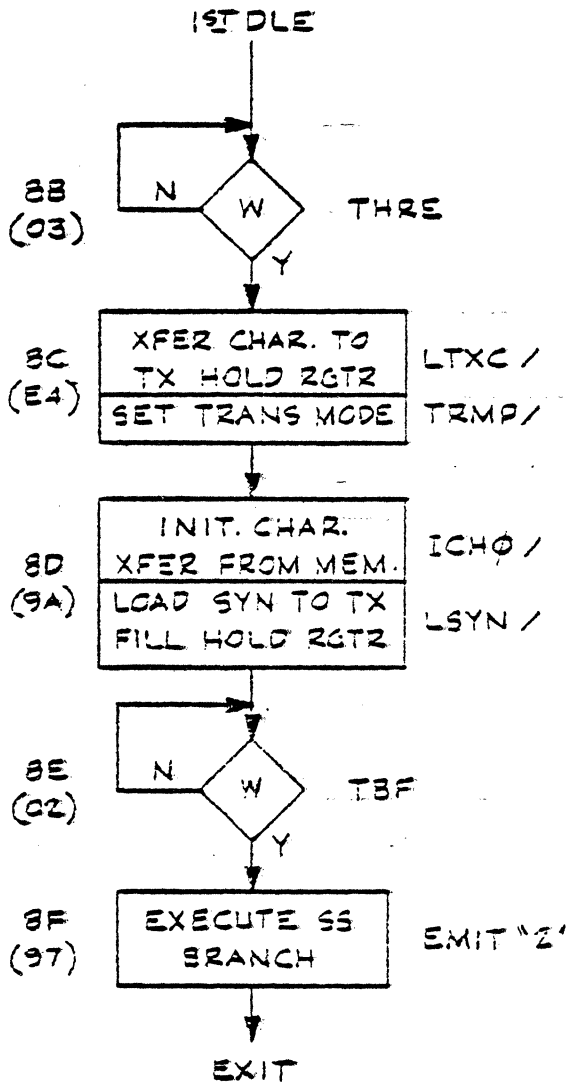
FORM 3-132-2



A	PS20002602	B
DWG SIZE	SHEET 41 OF 54.	REV

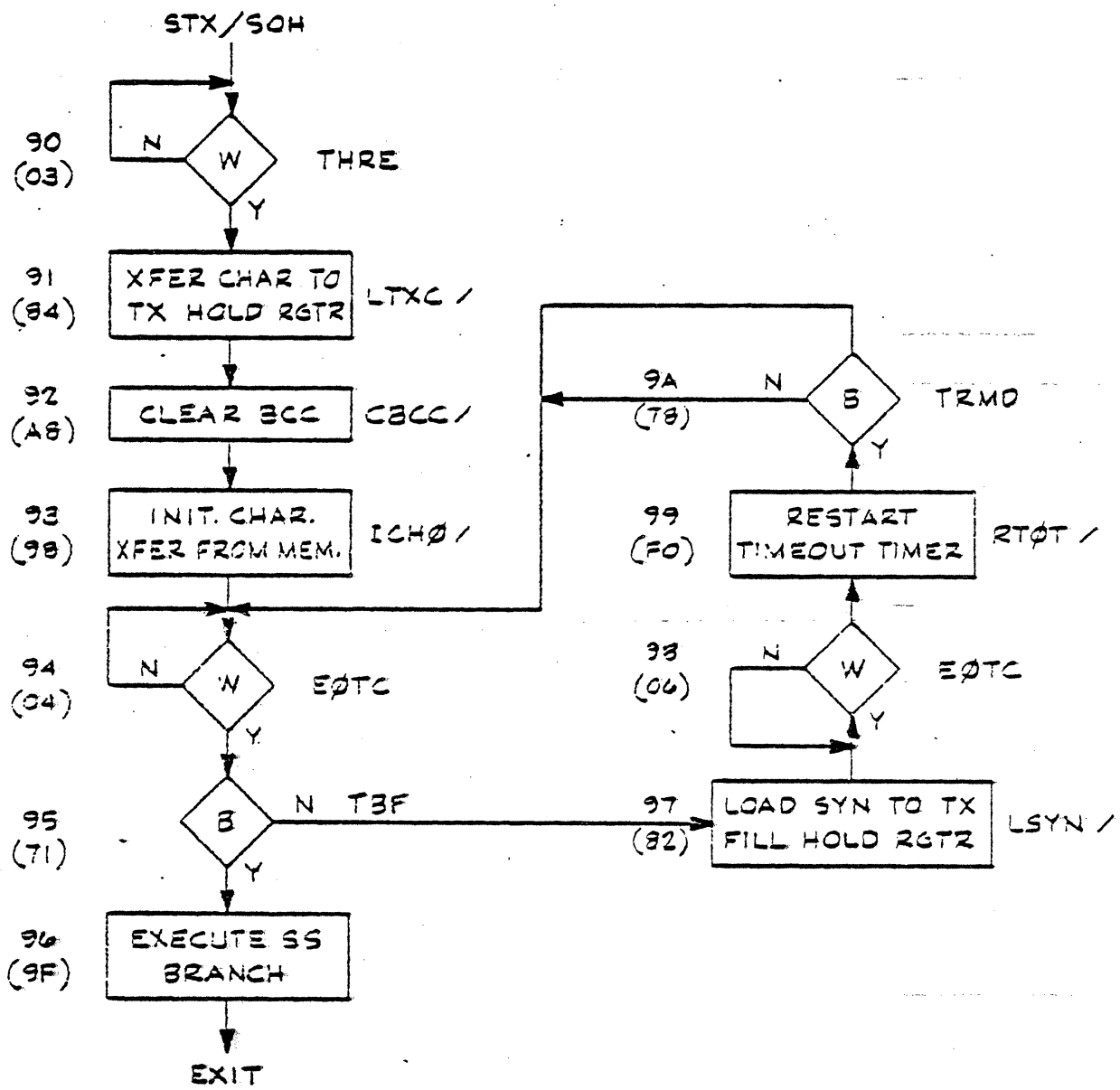
FORM 3-132-2





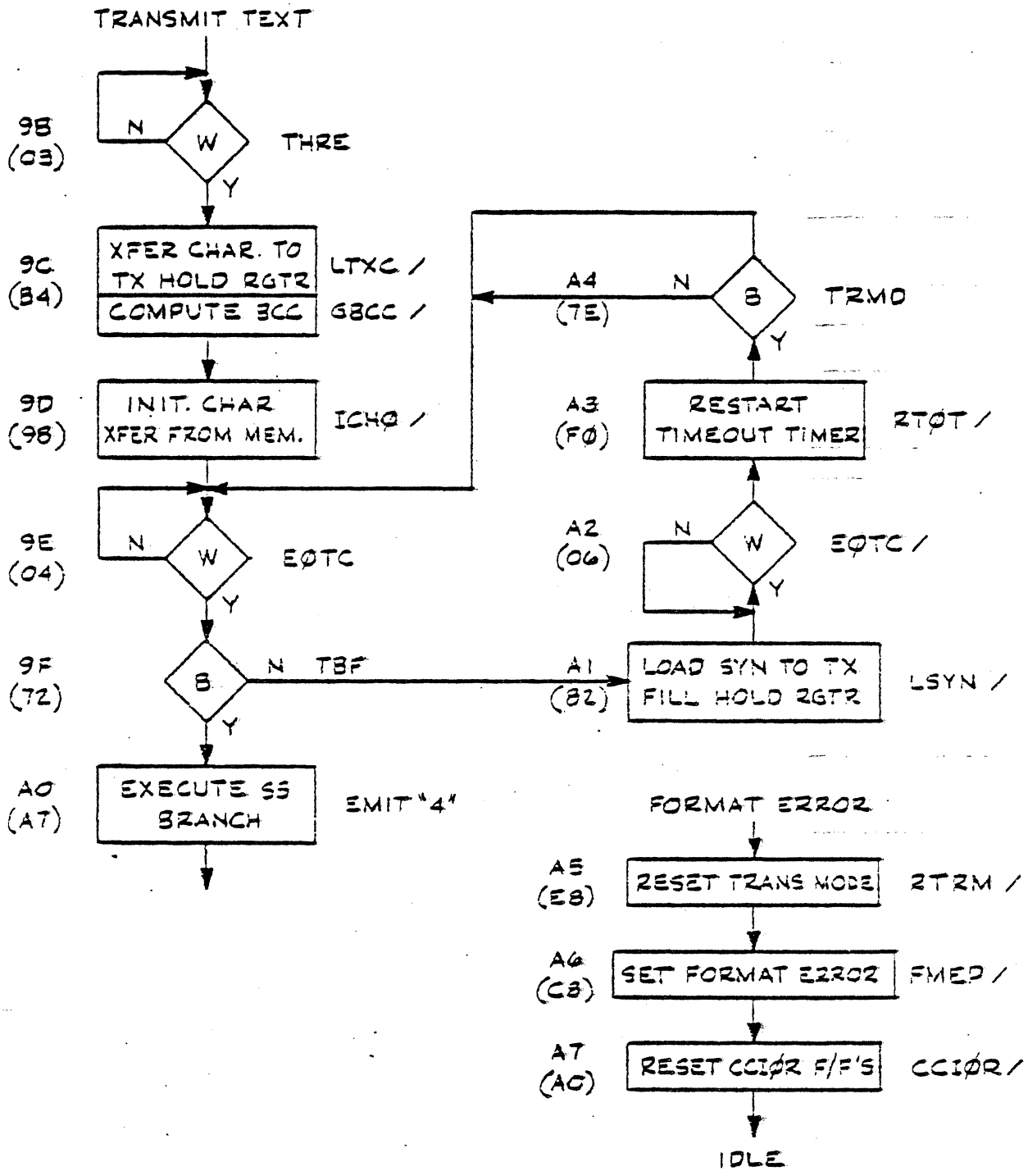
A	PS20002602	B
DWG SIZE	SHEET 42 OF 54	REV

FORM 3-132-2



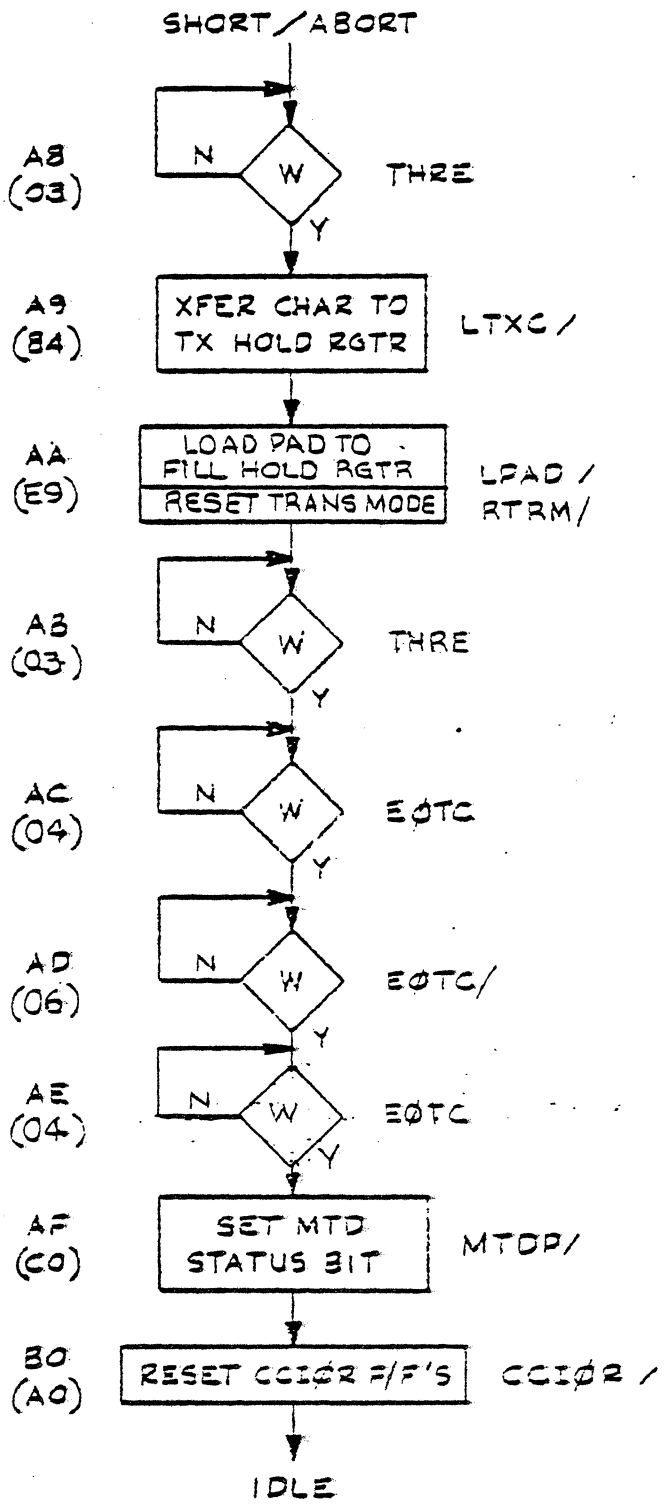
A	PS20002602	B
DWG SIZE	SHEET 43 OF 54	REV

FORM 3-132-2

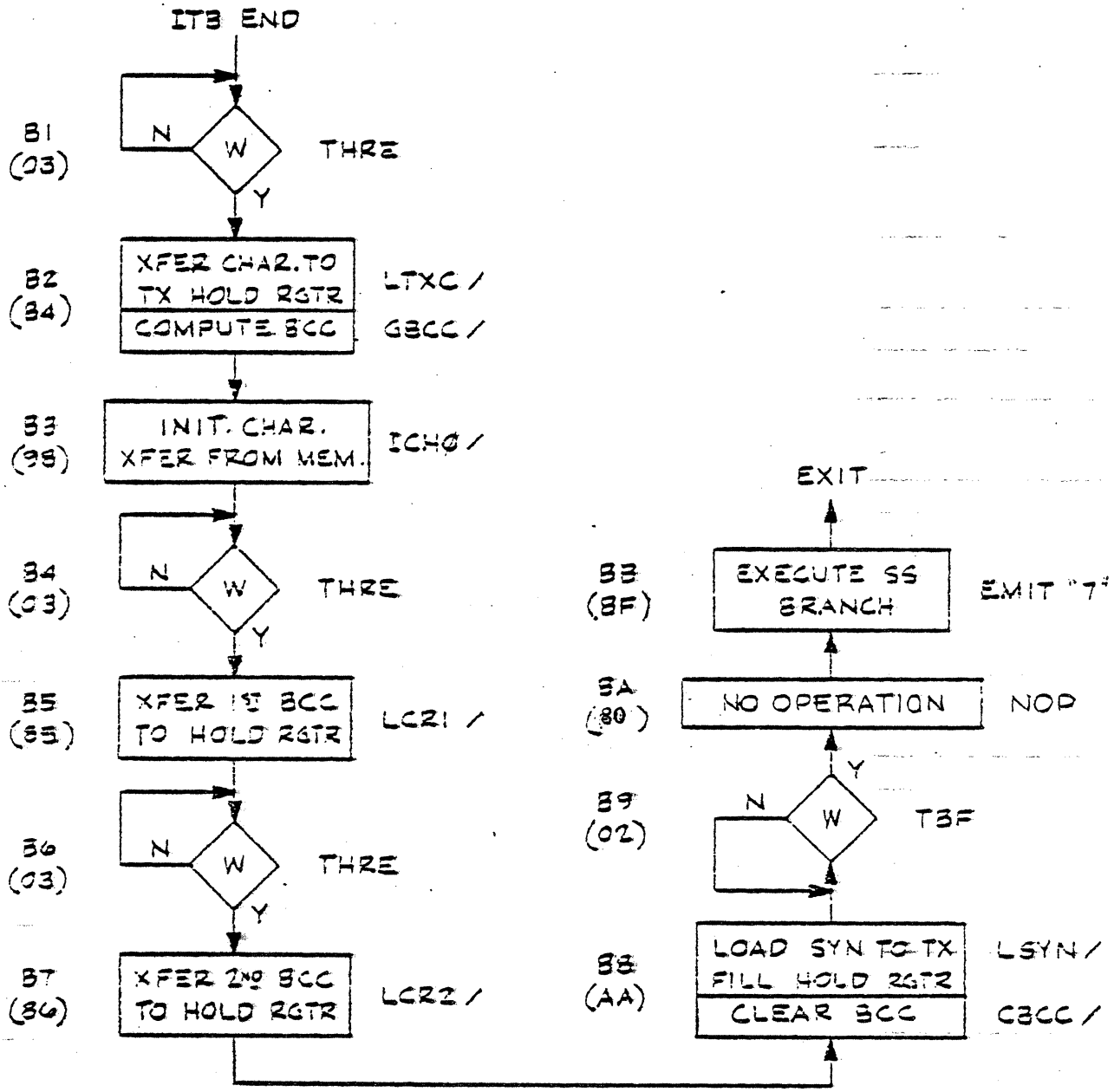


A	PS20002602	B
DWG SIZE	SHEET 44 OF 54	REV

FORM 3-132-2

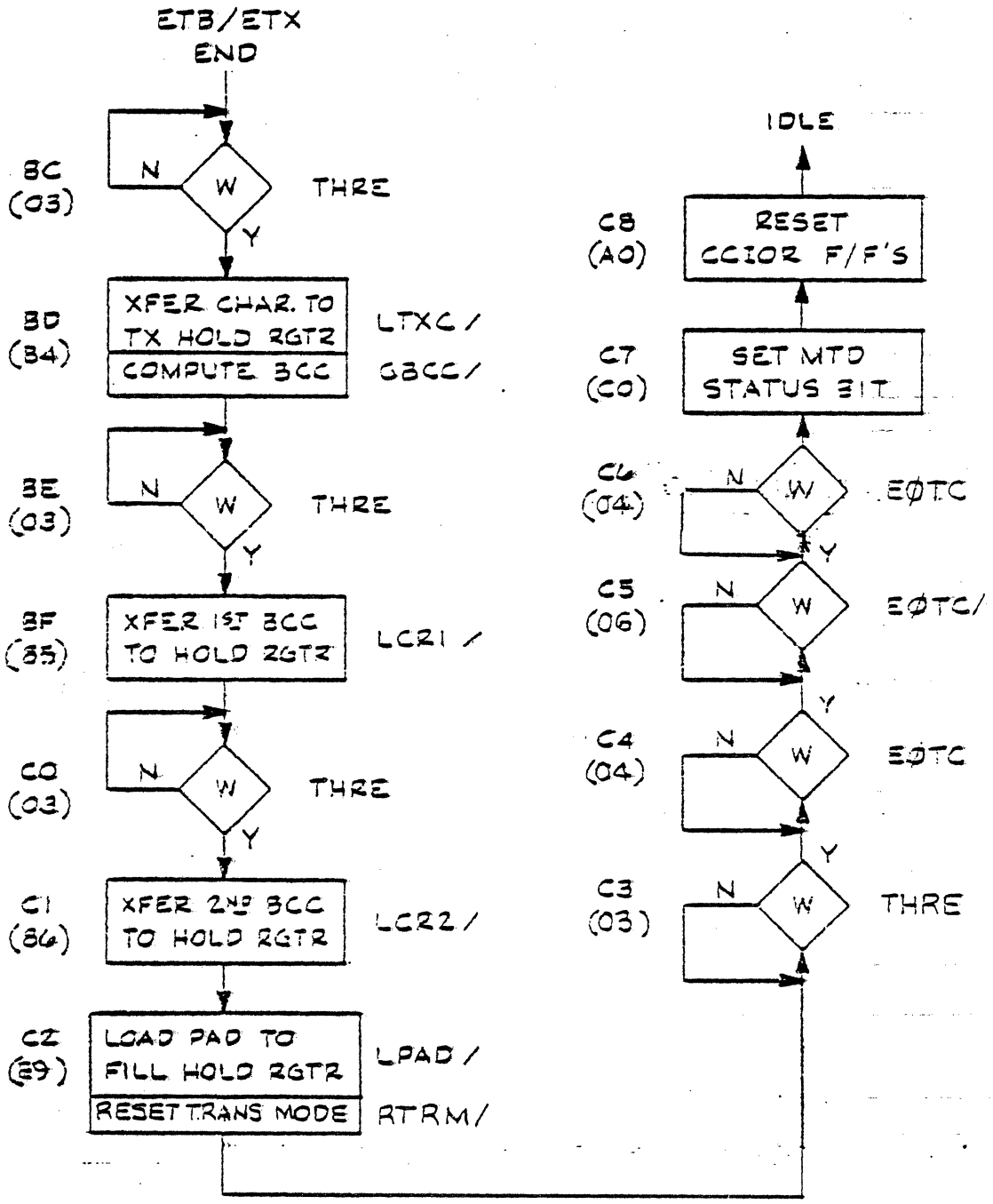


A	PS20002602	B
DWG SIZE	SHEET 45 OF 54	REV



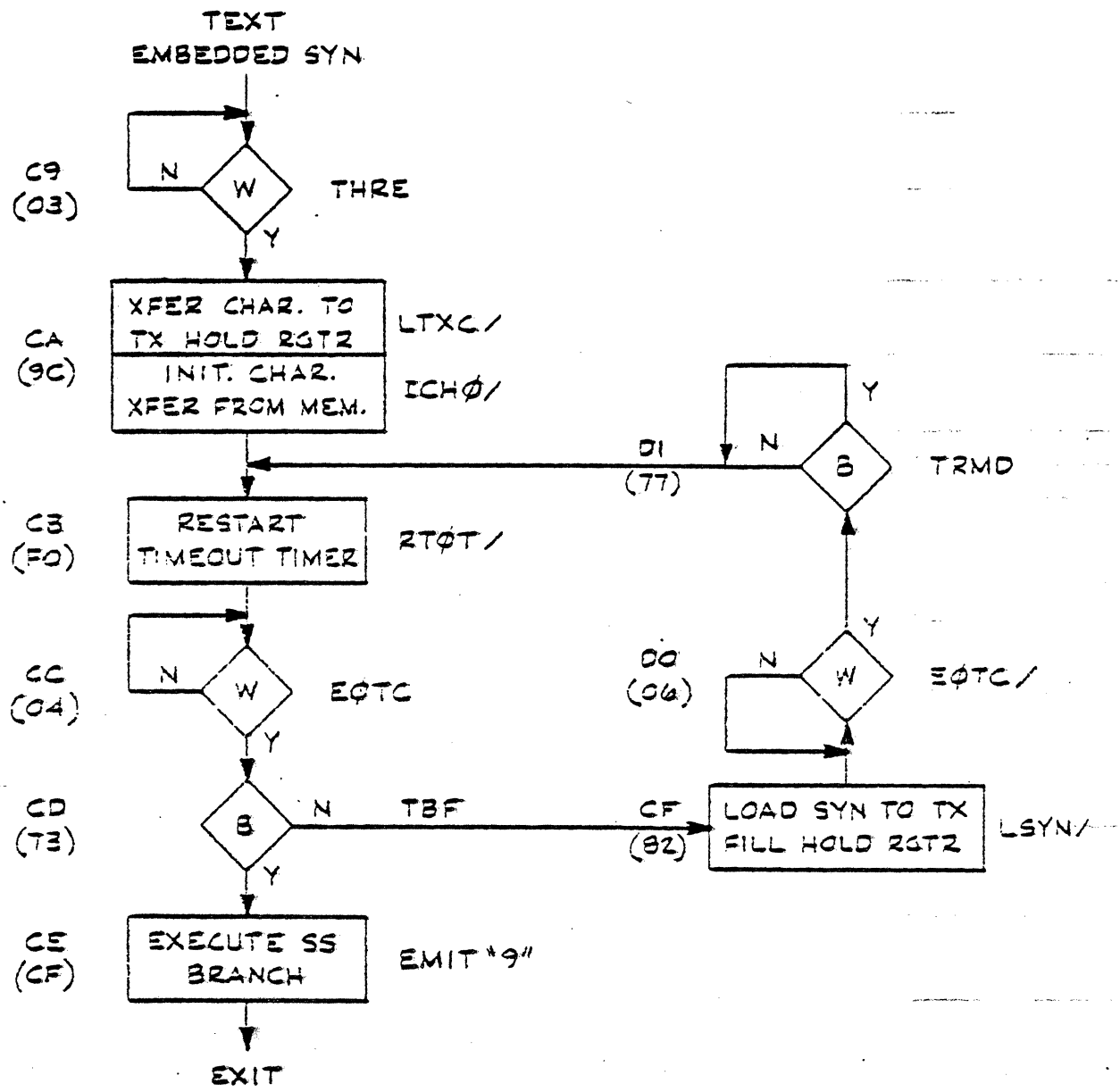
A	PS20002602	B
DWG SIZE	SHEET 46 OF 54	REV

FORM 3-132-2



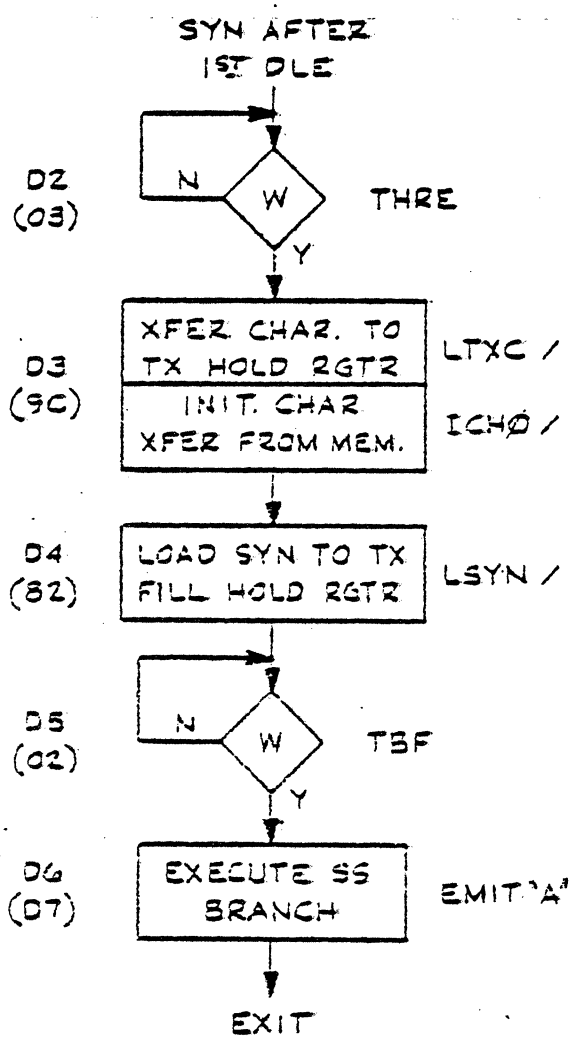
A	PS20002602	B
DWG SIZE	SHEET 47 OF 54	REV

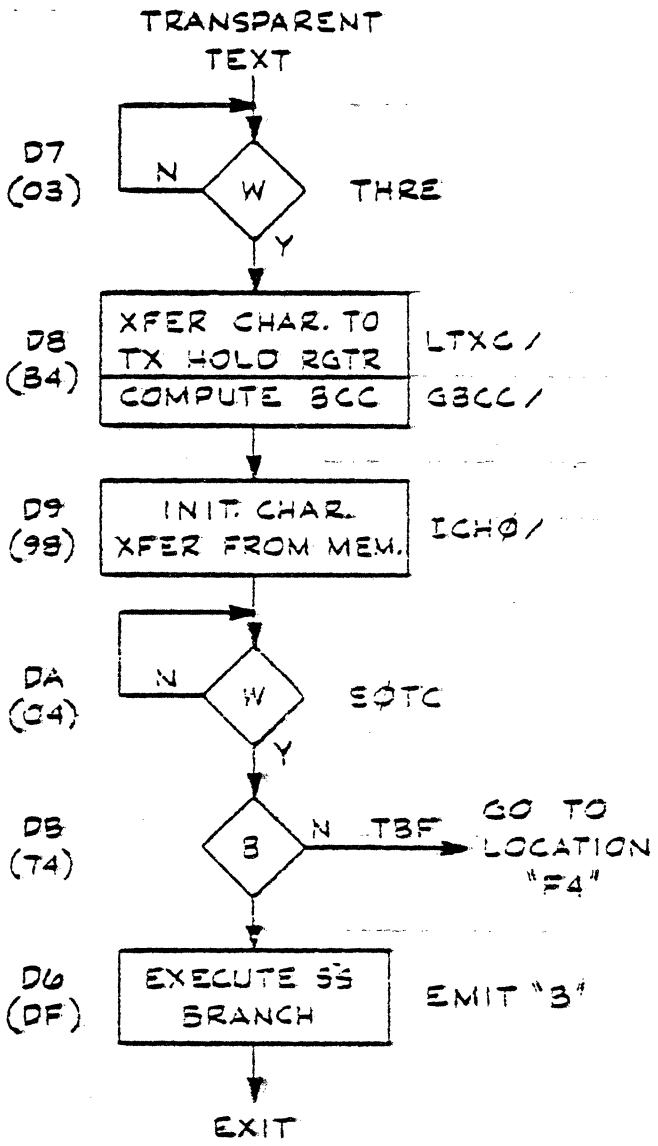
FORM 3-132-2



A	PS20002602	B
DWG SIZE	SHEET 48 OF 54	REV

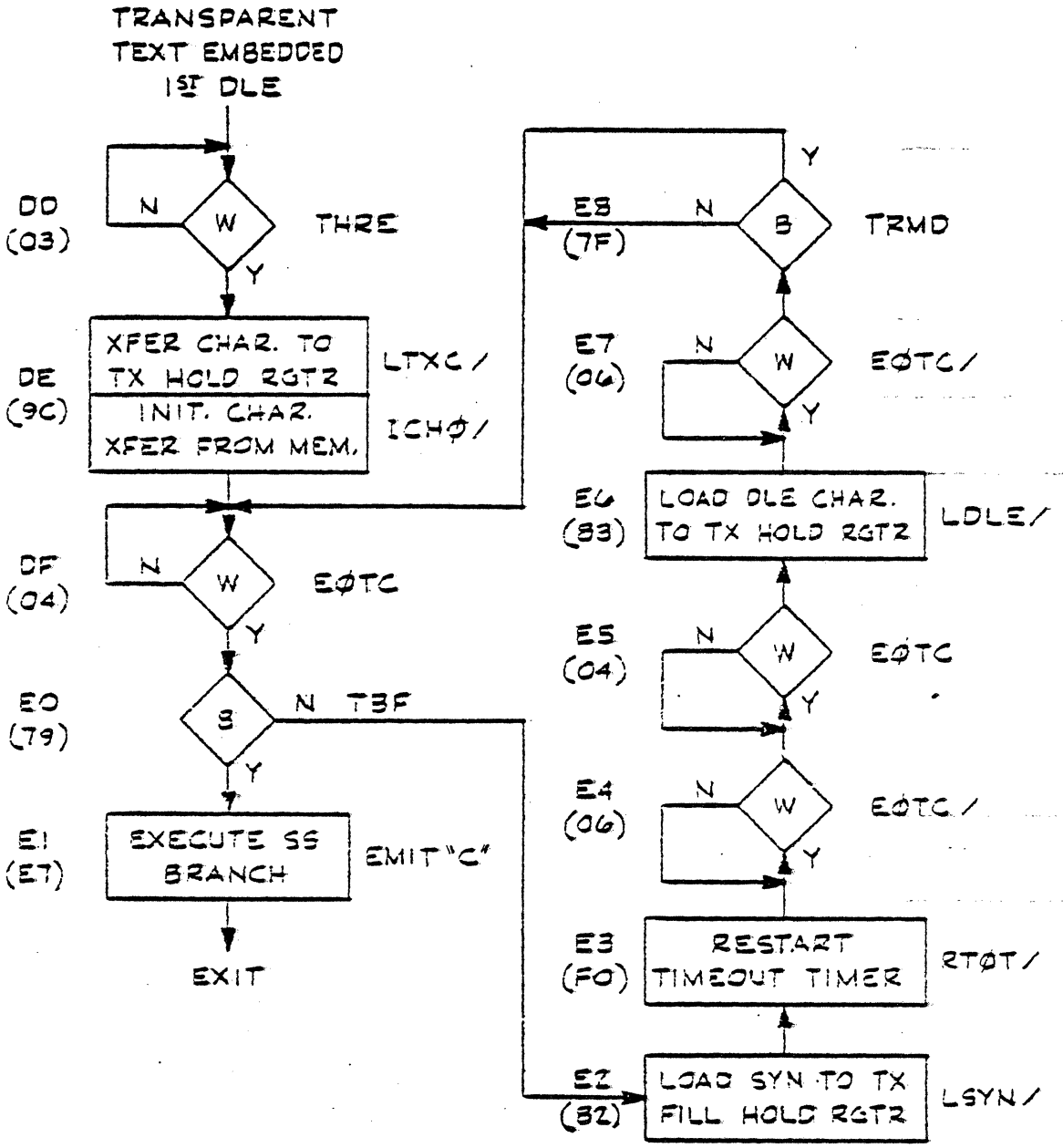
FORM 3-1132-2



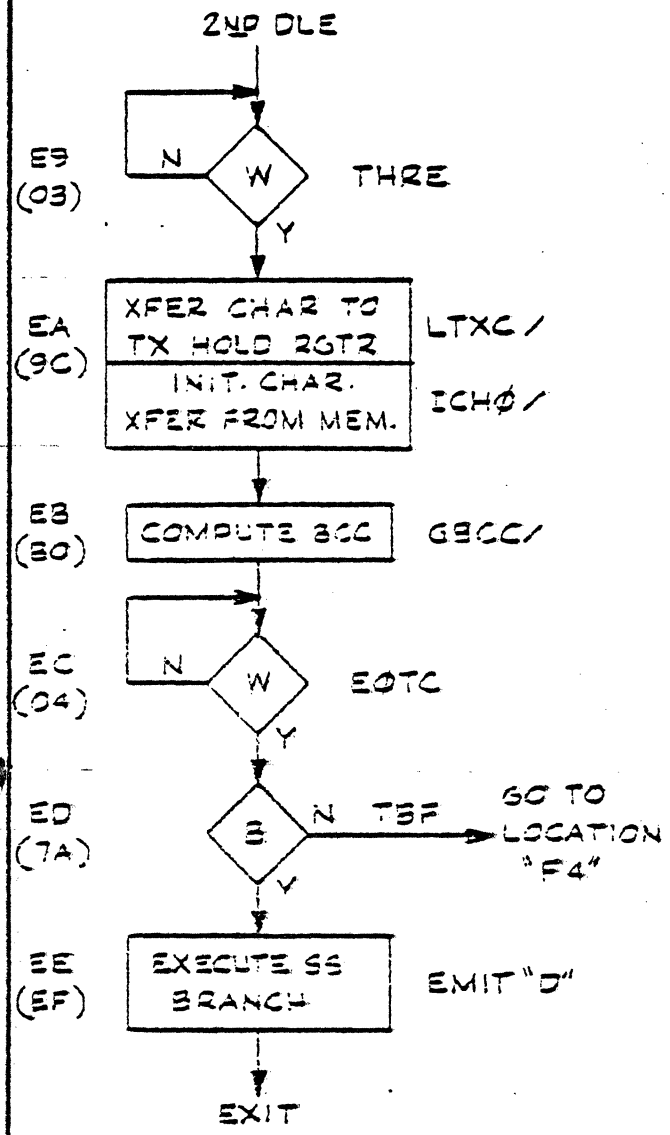


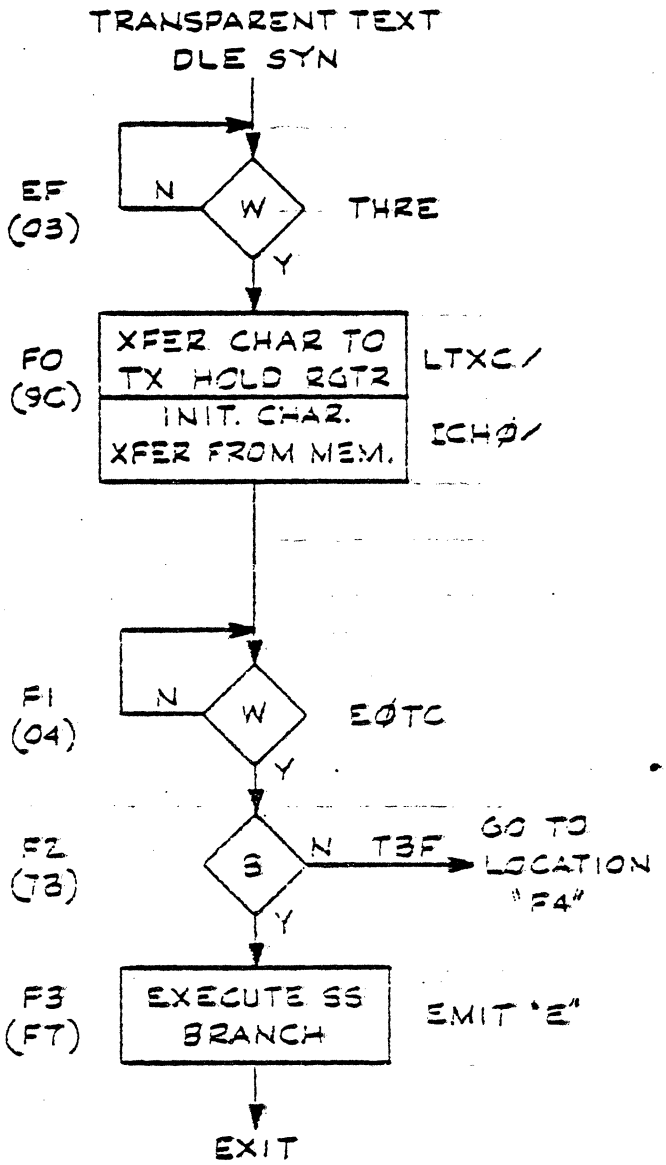
A	PS20002602	B
DWG SIZE	SHEET 49 OF 54	REV

FORM 3-132-2



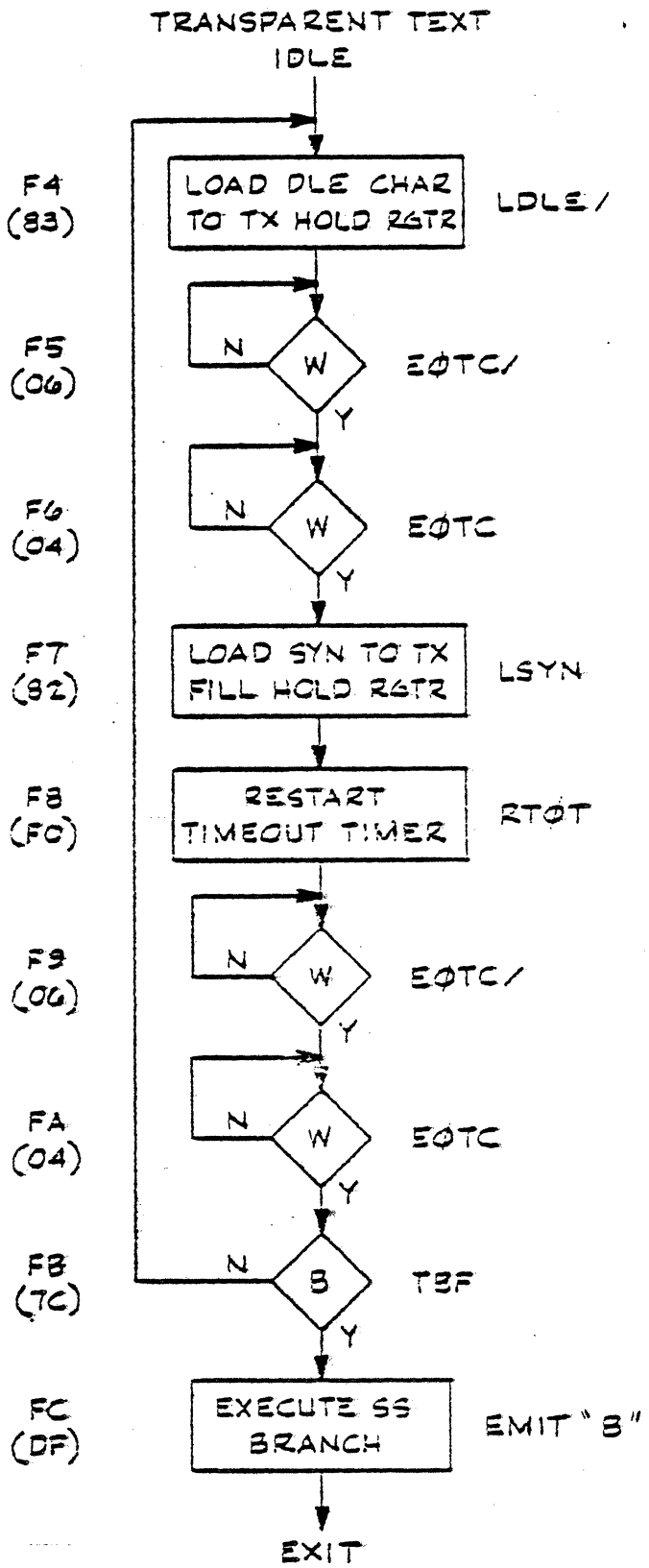
A	PS20002602	3
DWG SIZE	SHEET 50 OF 54	REV





A	PS20002602	B
DWG SIZE	SHEET 51 OF 54	REV

FORM 3-132-2



A	PS20002602	B
DWG SIZE	SHEET 52 OF 54	REV

FORM 3-132-2

4.0 ENVIRONMENT & POWER REQUIREMENTS

The controller requires 3 Amps at +5V, 60 mA at 12V, and 100 mA at 16.75V. It is designed to operate at temperatures between 0°C and 50°C and up to 90% relative humidity without condensation.

5.0 APPLICABLE DOCUMENTS

Product Specification	PS20002602
Artwork	AW20002602
Detail	D20002602
Assembly	A20002602-1 A20002602-2
Schematic	SC20002602
List of Materials	LM20002602-1 LM20002602-2

6.0 APPENDIX A

6.1 Diagnostic Information

a.	P/N 11192	DIA 2602 diagnostic for 16XX firmware systems.
b.	P/N11181	RD01-2602 diagnostic for REALITY System.

6.2 Device Address Jumpering

Table 1 contains the address jumpering for all ranges of address from 0 to 1F.

TABLE 1. DEVICE ADDRESS JUMPERING

HEX ADDRESS	JUMPER EYELET NUMBERS									
	E13 to		E4 to		E1 to		E7 to		E10 to	
	E2	E3	E11	E12	E14	E15	E8	E9	E5	E6
	E16 to		E19 to		E22 to		E25 to		E28 to	
	E29	E30	E27	E26	E24	E23	E21	E20	E18	E17
0		X		X		X		X		X
1		X		X		X		X	X	X
2		X		X		X	X			X
3		X		X		X	X		X	
4		X		X	X			X		X
5		X		X	X			X	X	
6		X		X	X		X		X	
7		X		X	X		X		X	
8		X	X			X		X		X
9		X	X			X		X	X	
A		X	X			X	X			X
B		X	X			X	X		X	
C		X	X		X			X		X
D		X	X		X			X	X	
E		X	X		X		X			X
F		X	X		X		X		X	
10*	X			X		X		X		X
11	X			X		X		X	X	
12	X			X		X	X			X
13	X			X		X	X		X	
14	X			X	X			X		X
15	X			X	X			X	X	
16	X			X	X		X			X
17	X			X	X		X		X	
18	X		X			X		X		X
19	X		X			X		X	X	
1A	X		X			X	X			X
1B	X		X			X	X		X	
1C	X		X		X			X		X
1D	X		X		X			X	X	
1E	X		X		X		X			X
1F	X		X		X		X		X	

*NOTE: Address "10" is normally assumed and is jumpered by etch. If another address is used, the etch between the eyelets that are changed must be cut.

TO: DEAN LIVINGSTON

FROM: DICK KEMPER 835-8853

SUBJECT: SYNCHRONOUS COMMUNICATIONS BOARD RECOMMENDATIONS

TRANSMISSION CODES

1. SIX-BIT TRANSCODE - NOT REQUIRED
2. EBCDIC (NORMAL AND TRANSPARENT) - REQUIRED
3. USASCII - NOT RECOMMENDED - USACII IS RARELY USED IN THE IBM WORLD OF REMOTE BATCH COMMUNICATIONS

DATA LINK CONTROL CHARACTERS

THE BOARD MUST BE ABLE TO RECOGNIZE THE FOLLOWING DATA LINK CONTROL CHARACTERS:

SYN -	X'32'
SOH -	X'01'
STX -	X'02'
ITB -	X'1F'
ETB -	X'26'
ETX	X'03'
EOT	X'37'
ENQ	X'2D'
NAK	X'3D'
DLE	X'10'
BEL	X'2F' *
PAD	X'FF' — strip

* BEL IS NOT A BSC DATA LINK CONTROL CHARACTER, HOWEVER A 2780 OR 3780 WILL TRANSMIT AND RECEIVE BLOCKS OF THE FORM:

"FF"

X	BEL	FAD

BEL on RCV. - Means 2 single byte messages. No RCC. BEL should be passed to software and treated as a legitimate starting character

CONTROL SEQUENCES

THE BOARD MUST BE ABLE TO TRANSMIT OR RECEIVE THE FOLLOWING TWO-CHARACTER CONTROL SEQUENCES;

DLE ENQ	X'102D'	DLE ENQ
ACK-Ø	X'1Ø7Ø'	DLE '70'
ACK-1	X'1Ø61'	DLE /
WACK	X'1Ø6B'	DLE ,
RVI	X'1Ø7C'	DLE @
TTD	X'022D'	STX ENQ
DLE-EOT	X'1Ø37'	DLE EOT
SOH-ENQ	X'012D'	* TRANSMIT ONLY - to S/360 from H/SP W.S. only. [illegible]

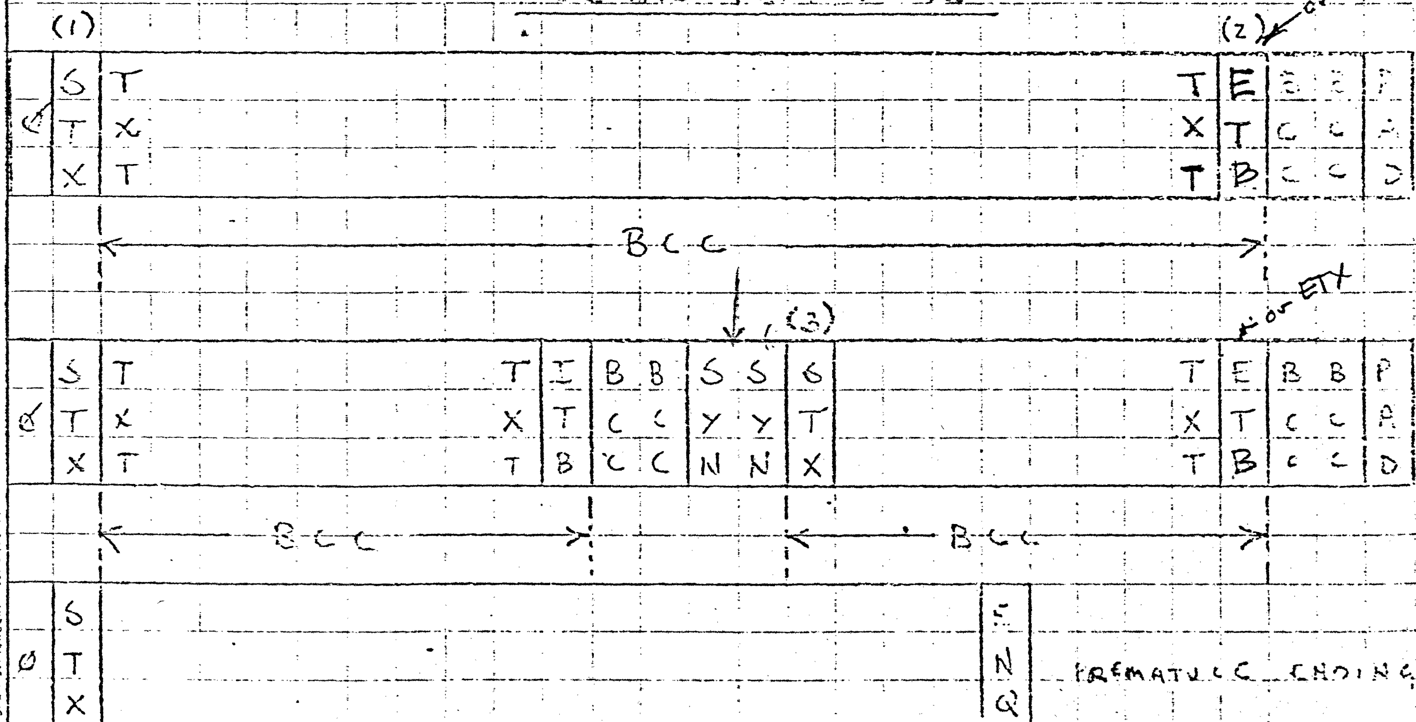
not in - FCV (separate [illegible])

ALL OF THE ABOVE SEQUENCES WILL BE PRECEDED BY AT LEAST TWO SYN CHARACTERS, AND FOLLOWED BY A PAD CHARACTER. NO BLOCK CHECK IS REQUIRED.

MESSAGE BLOCK FORMATS

THE BOARD MUST BE ABLE TO TRANSMIT AND RECEIVE MESSAGE BLOCKS HAVING THE FOLLOWING FORMATS;

NORMAL TEXT MODE



(1) EITHER AN SOH OR STX CHARACTER MAY INITIATE A MESSAGE BLOCK.

(2) THE LAST BLOCK IN A MESSAGE WILL BE TERMINATED BY AN ETX CHARACTER.

(3) THE STX FOLLOWING AN ITB IS OPTIONAL AND THEREFORE MAY NOT BE PRESENT.

Ø REPRESENTS TWO CONSECUTIVE SYN CHARACTERS.

TRANSPARENT TEXT MODE

exclude DLE SYN & first DLE & DLE DLE sequence from BCC.

(4)(3)

Ø	DLE	STX	TXT		TXT	DLE	ETB	BCC	BCC	PAD

← BCC →

insert fill characters but must be DLE SYN

Terminate transparent mode

Ø	DLE	STX	TXT		TXT	DLE	ITB	BCC	BCC	SYN	SYN	DLE	STX	TXT		TXT	DLE	ETB	BCC	BCC	PAD

← BCC → ← BCC →

Ø	DLE	STX		DLE	ENQ

(4) A CONTROL DLE, I.E., A DLE PRECEDING A DATA LINK CONTROL CHARACTER OR A DLE PRECEDING A TEXT DLE, IS NOT INCLUDED IN THE BLOCK CHECK. Note: Leave DLE's in Message to software. Delete DLE SYN's only.

IN THE ABOVE EXAMPLES, I WOULD RECOMMEND THE BOARD PERFORM THE FOLLOWING FUNCTIONS:

1. INSERT TWO CONSECUTIVE SYN CHARACTERS (Ø), BEFORE EVERY TRANSMISSION, AND IMMEDIATELY FOLLOWING THE BCC OF AN INTERMEDIATE BLOCK.

2. APPEND A PAD CHARACTER AT THE END OF EACH TRANSMISSION.

3. PERFORM THE ACCUMULATION AND CHECKING OF BLOCK ENDING CHARACTERS ON BOTH TRANSMIT AND RECEIVE BLOCKS BASED ON THE DATA LINK CONTROL CHARACTERS THAT DEFINE A BLOCK STRUCTURE. THE BCC SHOULD BE INSERTED ON TRANSMIT AND STRIPPED ON RECEIVE.

4. STRIP ALL RECEIVE SYN CHARACTERS OR DLE SYN SEQUENCES.

MODEM CONTROL SIGNALS

THE BOARD SHOULD BE ABLE TO REPORT THE PRESENT STATUS OF THE FOLLOWING MODEM CONTROL SIGNALS WITHOUT CHANGING ANY CONDITIONS ON THE BOARD, MODEM, OR LINE; ie inputting Tx or Rcv operations.

CARRIER DETECTOR

CLEAR TO SEND

SIGNAL QUALITY * - OPTIONAL

RING INDICATOR - OPTIONAL

DATA SET READY

DATA TERMINAL READY

INTERRUPT CONDITIONS Note: Disable to mask interrupt conditions.

THE FOLLOWING CONDITIONS SHOULD CAUSE THE BOARD TO INTERRUPT THE CPU:

1. COMPLETION OF A TRANSMIT OR RECEIVE MESSAGE BLOCK. Line
Note: Identify in Status on the Tx or Rcv.

2. DATA SET READY LINE FROM THE MODEM HAS CHANGED STATE.

3. CARRIER DETECTOR, CLEAR TO SEND, OR SIGNAL QUALITY LINES FROM THE MODEM HAVE CHANGED STATE WHILE DATA TERMINAL READY AND DATA SET READY ARE TRUE.

4. RING INDICATOR LINE FROM THE MODEM HAS CHANGED FROM FALSE TO TRUE WITH DATA Set READY FROM THE MODEM FALSE.

5. After receive mode is estab, set 3 second timer and restart with every SYN SYN (or DLE SYN in Transptext). Set status bit on runout.

MISCELLANEOUS

1. THE BOARD SHOULD OPERATE IN EITHER THE HALF DUPLEX OR FULL DUPLEX MODE AT SPEEDS FROM 2000 TO 50,000 BITS PER SECOND. Clocks from Modem.

1a. Test for SYN SYN (or DLE SYN) every 3 seconds and set a status bit.

2. IT ~~SHOULD BE~~ SHOULD PROVIDE AN EIA VERSION FOR UP TO 20,000 BPS USES AN RS 232-C AND CCITT/V.24 COMPATIBLE INTERFACE, AND A WIDEBAND VERSION FOR DATA RATES FROM 19.2 TO 50KBPS USING AN AT&T 303 COMPATIBLE INTERFACE.

3. A TEST CONNECTOR SHOULD BE PROVIDED FOR EXTERNAL LOOPING OF DATA FOR TEST PURPOSES.

TRANSMIT DATA → RECEIVE DATA

DATA TERMINAL READY → DATA SET READY AND CARRIER DETECT

REQUEST TO SEND → CLEAR TO SEND

ETC.

4. LEADING GRAPHICS SHOULD BE SUPPORTED — throw away 1-7 characters preceding ACK0, ACK1, NAK,