COPY NO. 307

Technical Manual

Reflex® II

Microdata
Customer Service Training

Technical Manual

Reflex® II

PUBLICATION NUMBER 81 1091B

PROPRIETARY INFORMATION

FOR INTERNAL USE ONLY

Microdata Corporation
2361 McGaw Avenue,
Irvine, California 92714
Telephone: 714/540-6730
Customer Service Training

CONTENTS

Section		Page
1	GENERAL DESCRIPTION	
	Introduction	1-1
	Features, Options, and Accessories	1-3
	Features	1-3
	Options	1-3
	Accessories	1-3
	General	1-4
	Functional Description	1-4
	Input	1-5
	Address Select	1-6
	Bus and Tag Lines	1-6
	Configuration Request	1-6
	Write Data and Write Clock	1-6
	Output	1-6
	Positioning	1-7
	Read/Write	1-8
	Physical Description	1-10
	Safety Features	1-11
	Operator	1-11
	Drive	1-11
	Data	1-11
	Nameplate identification	1-11

CONTENTS (Cont'd)

Section		Page
2	PHYSICAL PLANNING AND INTERFACE REQUIREMENTS	
	Introduction	2-1
	Environmental Conditions	2-1
	Stabilization	2-1
	Temperature	2-1
	Humidity	2-1
	Altitude	2-1
	Air Flow	2-2
	Noise Level	2-2
	Storage	2-2
	Space Requirements	2-2
	Power Requirements	2-2
	Input AC Voltage Fluctuations	2-4
	Power Cable Configurations	2-4
	AC Power With Optional Internal Power Supply	2-5
	AC Power Without Optional Internal Power Supply	2-5
	DC Voltage Without Optional Internal Power Supply	2-6
	Grounding	2-7
	Interface Requirements	2-8
	Logic Interface	2-8
	Cabling	2-8
	Data Cable	2-8
	Signal Cable	2-8
	Frame Ground Cable	2-10

CONTENTS (Cont'd)

Section		Page
	Available Cables	2-10
	Connector Jacks	2-11
	Connector Orientation	2-11
	Signal Cable Descriptions	2-11
	Pin Assignments	2-11
	Signal Cable Definitions	2-11
	Data Cable	2-22
	Pin Assignments	2-22
	Definitions	2-23
	Transmitters, Receivers, and Terminators	2-24
	Transmitters and Receivers	2-24
	Terminators	2-24
	Data Format	2-27
	Format Considerations	2-27
	Head Select	2-27
	Write Amplifier	2-27
	Read To Write	2-27
	Read VCO	2-27
	Splice	2-27
	Preamble	2-28
	Postamble	2-28
	Synch Pattern	2-29

CONTENTS (Cont'd)

Section		Page
	Method	2-29
	Write Initialization	2-29
	Write Record Data	2-30
	Read	2-31
	Format Summary	2-32
	Fixed Head Per Track	2-33
	Data Security	2-33
3	INSTALLATION AND OPERATION	
	Introduction	3-1
	Installation Check List	3-1
	Unpacking	3-3
	Physical Inspection	3-4
	Reflex II Units Without Internal Power Supply	3-5
	Grounding	3-6
	AC Power Cable	3-7
	Signal, Data, and Exerciser Cables	3-8
	Initial Checkout Procedure	3-10
	System Installation	3-11
	Power Verification	3-13
	60 Hz Verification	3-13
	50 Hz Verification	3-14
	Power Conversion	3-14
	60 Hz to 50 Hz	3-14
	50 Hz to 60 Hz	3-15

CONTENTS (Cont'd)

Section		Page
	Operation	
	Operator Indicator Panel	3-15
	Maintenance Controls	3-16
	Unit Address Selection	3-19
	Illegal Head Address Selection	3-19
	Sector Selection	3-20
4	THEORY OF OPERATION	
	Introduction	4-1
	Physical Description	4-1
	Power Components	4-1
	Transformer Assembly	4-1
	Sealed Module and Motor Assembly	4-1
	Printed Circuit Boards	4-2
	General	4-2
	Input/Output Interface	4-3
	Positioning System	4-3
	Cooling and Clean Air System	4-3
	Read/Write System	4-3
	Spindle Motor System	4-4
	Functional Description	4-4
	General	4-4
	Power Supplies and Distribution	
	Standard Power Configuration	4-8
	Optional Power Configuration	4-10

CONTENTS (Cont'd)

Section		Page
	Power Supply/Amplifier PCB	
	Voltage Filtration and Generation	4-11
	+5 Volt Overvoltage Protection	4-11
	Under Voltage Monitor (DCSAFE)	4-12
	DC Voltage Distribution	4-14
	Input Interface	4-15
	Drive Selection	4-17
	Sequencing	4-22
	Sequence Enable	4-22
	Sequence Control	4-24
	DCSAFE	4-24
	PWRINI	4-27
	SEQENBL	4-28
	Energizing the Spindle Motor	4-28
	Spindle Brake Released (SPINBRKRLSD)	4-28
	Solenoid Activated (Released)	4-28
	25-Second Timer	4-32
	Start AC Motor (STACMTR/)	4-33
	Up-To-Speed	4-33
	Disable Retract Heads (RETHDS/)	4-36
	Servo Control Logic (Sequence Up)	4-36
	Sequence Summary	4-40
	Sequence Down	4-40
	Function Decode	4-40

CONTENTS (Cont'd)

Section	Page
Positioning System	4-47
Recorded Servo Surface	4-47
Servo System Control	4-52
Initial Seek	4-52
Program Control Seek	4-55
Restore Operation	4-58
Servo Data Processing Into Clocks and Position Info	4-58
Clock Processing	4-58
Pattern Detection	4-63
Position Signal Generation	4-65
Servo Motor Control	4-66
Retract Heads	4-67
Velocity Mode	4-68
Track Following Mode	4-72
Servo Motor Current Amplifier	4-73
Positioning System Summary	4-73
Sector Generation	4-76
Read/Write System	4-78
Recording Format	4-78
Head Selection	4-80
Illegal Head	4-80
Head Decode	4-81
Write Circuit	4-82
Enabling R/W Head Write Driver	4-87

CONTENTS (Cont'd)

Section		Page
	Writing Data	4-89
	Read Circuit	4-90
	Read/Write Head Assembly	4-98
	Error Detection	4-98
	Fault	4-98
	DC Voltage Unsafe	4-99
	R/W Head Circuit Unsafe	4-99
	Illegal Head Selected	4-99
	Invalid Write Operations	4-100
	Reset Fault	4-100
	Seek Error	4-100
	Attempted Seek While Not Ready	4-101
	Illegal Cylinder Address	4-101
	Seek Time-Out (1.5 Second Time Out)	4-101
	Open Cable Active While Drive Is On-Line	4-102
	Resetting Seek Error	4-102
	Retract Control (Emergency Retract)	4-102
	Seek Time-Out Seek Error	4-102
	Open Cable	4-102
	Status	4-105
	Output Interface	4-105
5	MAINTENANCE	
	Introduction	5-1
	Preventive Maintenance	5-1

CONTENTS (Cont'd)

Section	Page
Corrective Maintenance	5-1
Troubleshooting	5-1
Fault Isolation	5-2
Maintenance Checks	5-2
Power Supply Check	5-2
DC Voltage Distribution	5-5
Sequence Up	5-8
Ground Brush Assembly	5-11
Servo Balance (Offset) Verification	5-12
Velocity Verification	5-12
Damper Verification	5-12
Pulse Gate Verification	5-12
Separated Pulse Verification	5-12
Phase Detector Offset Verification	5-13
Read/Write Pulse Width Verification	5-13
Brake Verification	5-13
Adjustments	5-14
Servo PCB Adjustments	5-14
Speed Adjustment	5-15
Separated Pulse Adjustment	5-16
Pulse Gate Adjustment	5-16
Balance (offset) Adjustments	5-16
Velocity Adjustment	5-17
Damper Adjustment	5-18

CONTENTS (Cont'd)

Section		Page
	Read Write Adjustment	5-18
	Phase Detector Offset Adjustment	5-18
	Pulse Width (Detector Window) Adjustment	5-21
	Brake Adjustment	5-21
	Removal and Replacement	5-22
	Printed Circuit Boards	5-23
	Read/Write Boards	5-23
	Servo PCB	5-23
	Logic/Interface PCB	5-24
	Power Supply/Amplifier PCB	5-24
	LED/Switch PCB (Operator Indicator Panel)	5-25
	Electromechanical Assemblies	
	Sealed Module and Motor Assembly	5-26
	Cooling Fan(s)	5-28
	Transformer Assembly (DC Voltage Supply)	5-28
	AC Motor Pulley	5-30
	AC Spindle Motor	5-31
	AC Motor Plate	5-31
	Ground Brush Assembly	5-32
	Brake Assembly	5-32
	Line Filter Assembly	5-33
	Test Equipment and Tools	5-34
6	PARTS LIST, ASSEMBLY DRAWINGS AND SCHEMATICS	
	Introduction	6-1

CONTENTS (Cont'd)

Section		Page
Parts List		6-1
Appendix A:	Number Conversions	A-1
Appendix B:	Glossary	B-1

ILLUSTRATIONS

Figure		Page
1-1	Reflex®II Disc Drive	1-1
1-2	Reflex II Without Covers	1-2
1-3	Reflex II Modular Component Accessibility	1-2
1-4	Reflex II General Block Diagram	1-5
1-5	Positioner Mechanism	1-7
1-6	Reflex II Cylinder Concept	1-9
1-7	Nameplate	1-14
2-1	Physical Dimension Considerations	2-3
2-2	Standard AC Power Outlet Configuration	2-4
2-3	Typical Current Characteristics With Internal Power Supply	2-5
2-4	Typical Current Characteristics Without Internal Power Supply	2-5
2-5	DC Voltage Supply Cable Pin Assignments	2-6
2-6	Cable Connections and Ground Tie Points	2-7
2-7	Daisy Chain and Star Configuration (OEM USE)	2-9
2-7A	Daisy Chain Configuration (REALITY USE)	2-10
2-8	Connector Pin Orientation	2-11
2-9	Signal Cable Pin Assignments	2-12
2-10	Drive Selection	2-13
2-11	Set Cylinder Timing	2-14
2-12	Set Head Timing	2-15
2-13	Set Cylinder and Set Head Timing Relationship	2-16
2-14	Write Command Timing	2-17
2-15	Read Command Timing	2-17
2-16	Offset Command Timing	2-18

ILLUSTRATIONS (Cont'd)

Figure		Page
2-17	Reset Fault Command Timing.	2-18
2-18	Restore Command Timing.	2-19
2-19	Data Cable Pin Assignments.	2-22
2-20	Read/Write Signal Relationships	2-23
2-21	Typical Signal Cable Transmission Line	2-25
2-22	Typical Data (Read/Write) Transmission Line	2-26
2-23	I OPNCBLDET Termination	2-26
2-24	Splice Location	2-28
2-25	Format Summary	2-32
2-26	Fixed Head Selection	2-33
3-1	Cover Removal	3-3
3-2	DC Voltage Connector	3-5
3-3	DC Voltage Connection	3-6
3-4	Ground Connection	3-7
3-5	AC Power Cable Convention	3-7
3-6	Cable Connections	3-9
3-7	Operator Indicator Panel	3-17
3-8	Power On/Off Switch	3-18
3-9	Logic/Interface Switches	3-18
3-10	Sector Length	3-25
4-1	Reflex II System Block Diagram	4-5
4-2	Typical Read/Write Head	4-7
4-3	Standard Power Configuration and AC Distribution	4-9
4-4	Optional Power Configuration and AC Distribution	4-10

ILLUSTRATIONS (Cont'd)

Figure		Page
4-5	Power Supply Filtering and Voltage Generation. . .	4-12
4-6	+5V Over Voltage Protection	4-12
4-7	Under Voltage Monitor	4-13
4-8	DC Voltage Distribution	4-15
4-9	Input Interface Cable Connection	4-16
4-10	Input Interface Logic	4-18
4-11	Drive Selection Logic	4-21
4-12	Sequence Enable	4-23
4-13	Sequence Control General Block Diagram	4-25
4-14	Sequence Control Initialization	4-26
4-15	Logic Initialization	4-27
4-16	Spindle Motor Flip-Flop Active	4-29
4-17	Spindle Brake Released	4-30
4-18	Solenoid Drive	4-31
4-19	Spindle Motor Control	4-34
4-20	Disc Speed Safe/Carriage Unlocked	4-35
4-21	RETHDS/Control of Servo Motor	4-37
4-22	Servo Control Logic (Sequencing)	4-38
4-23	Ready Logic	4-39
4-24	Function Decode Logic	4-41
4-25	Positioning System Block Diagram	4-45
4-26	Servo Disc Layout	4-48
4-27	Servo Track Frame Pattern	4-49
4-28	Frame Arrangement	4-50

ILLUSTRATIONS (Cont'd)

Figure		Page
4-29	Frame Patterns	4-51
4-30	Servo System Control	4-53
4-31	Servo Data Processing	4-59
4-32	Servo Data Timing	4-61
4-33	Index Pattern Detection	4-64
4-34	Up-To-Speed Detection	4-64
4-35	Outer Guard Band Detection	4-65
4-36	Position Signal	4-67
4-37	Servo Motor Control Circuit	4-69
4-38	Threshold and On Track Generation	4-72
4-39	Sector Counter	4-77
4-40	Simplified Block Diagram, Read/Write System	4-79
4-41	REFLEX II R/W Head Arrangement	4-81
4-42	Head Selection Circuitry	4-83
4-43	Write Circuitry	4-85
4-44	Timing Diagram	4-88
4-45	Read Circuit	4-91
4-46	Data Separator Timing Diagram	4-93
4-47	MFM Low and High Recording Frequencies	4-93
4-48	Differentiator Peak to "0" Crossing	4-94
4-49	Eliminate Extra Crossovers From Head Response	4-95
4-50	Read Phase Detection Settling Time	4-97
4-51	Fault Logic	4-103
4-52	Primary/Alternate Status	4-105

ILLUSTRATIONS (Cont'd)

Figure		Page
4-53	Output Interface	4-107
5-1	Power Supply/Amplifier Assembly	5-3
5-2	Power Supply/Amplifier PCB	5-5
5-3	Servo DC Voltages	5-6
5-4	Read/Write DC Voltages	5-8
5-5	DC Voltage Distribution	5-9
5-6	Sequence Up	5-10
5-7	Servo Adjustments	5-14
5-8	DELETED	
5-9	DELETED	
5-10	Velocity Adjustment	5-19
5-11	Read/Write Adjustments	5-19
5-12	Phase Detector Offset Adjustment	5-20
5-13	Pulse Width Adjustment	5-22
5-14	REFLEX II Front/Side View	5-25
5-15	REFLEX II Top View, Maintenance	5-27
5-16	REFLEX II Rear View	5-29
5-17	REFLEX II Bottom View	5-30
5-18	Motor Plate Hardware	5-32
5-19	Line Filter Assembly	5-34

TABLES

Table		Page
1-1	REFLEX II Specifications.	1-12
2-1	Input AC Voltage Fluctuations	2-4
2-2	DC Voltage Requirements	2-6
2-3	Operation Signals	2-14
2-4	I Configuration Status	2-20
3-1	Installation and Operation	3-1
3-2	Cable Connector Assignments	3-8
3-3	System Connection Information	3-12
3-4	Operator Indicator Panel	3-16
3-5	Maintenance Controls	3-17
3-6	Unit Address Switch Settings	3-19
3-7	Head Selection Switch Settings	3-20
3-8	Sector Selection	3-22
4-1	Drive Selection Switch Settings	4-19
4-2	Bus and Tag Decode	4-43
4-3	Movable Head Selection Decode	4-82
5-1	Voltage and Test Points for Power Supply/Amp PCB	5-4
5-2	Voltage and Test Points for Logic/Interface PCB .	5-5
5-3	Voltage and Test Points for Servo PCB	5-6
5-4	Voltage and Test Points for Read/Write PCB . . .	5-7
6-1	REFLEX II Part Numbers and Descriptions	6-1
6-2	REFLEX II Options	6-3
6-3	REFLEX II Accessories	6-3
6-4	REFLEX II Schematics	6-3

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

This section includes a general description of the Microdata Reflex® II disc drive. Figure 1-1 presents the Reflex II with all covers intact and all available options. Figure 1-2 shows the Reflex II with all covers removed. The accessibility of the modular components is shown in Figure 1-3.

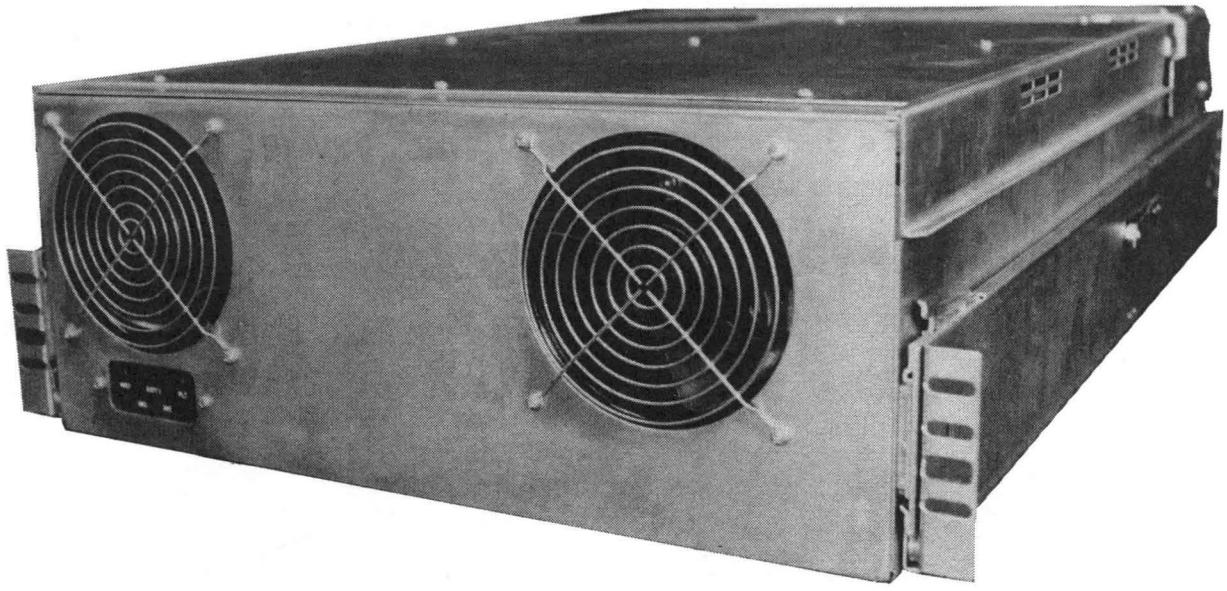


Figure 1-1. Reflex II Disc Drive

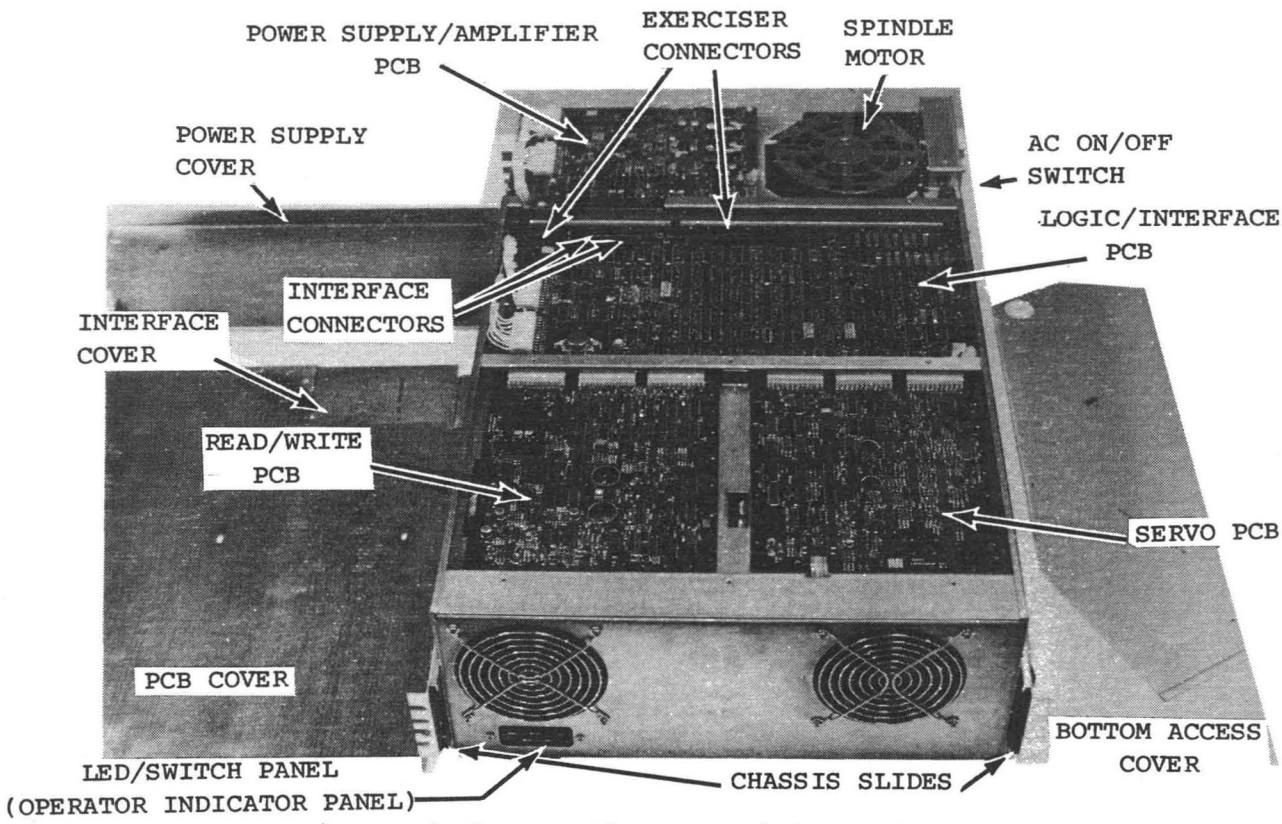


Figure 1-2. Reflex II Without Covers

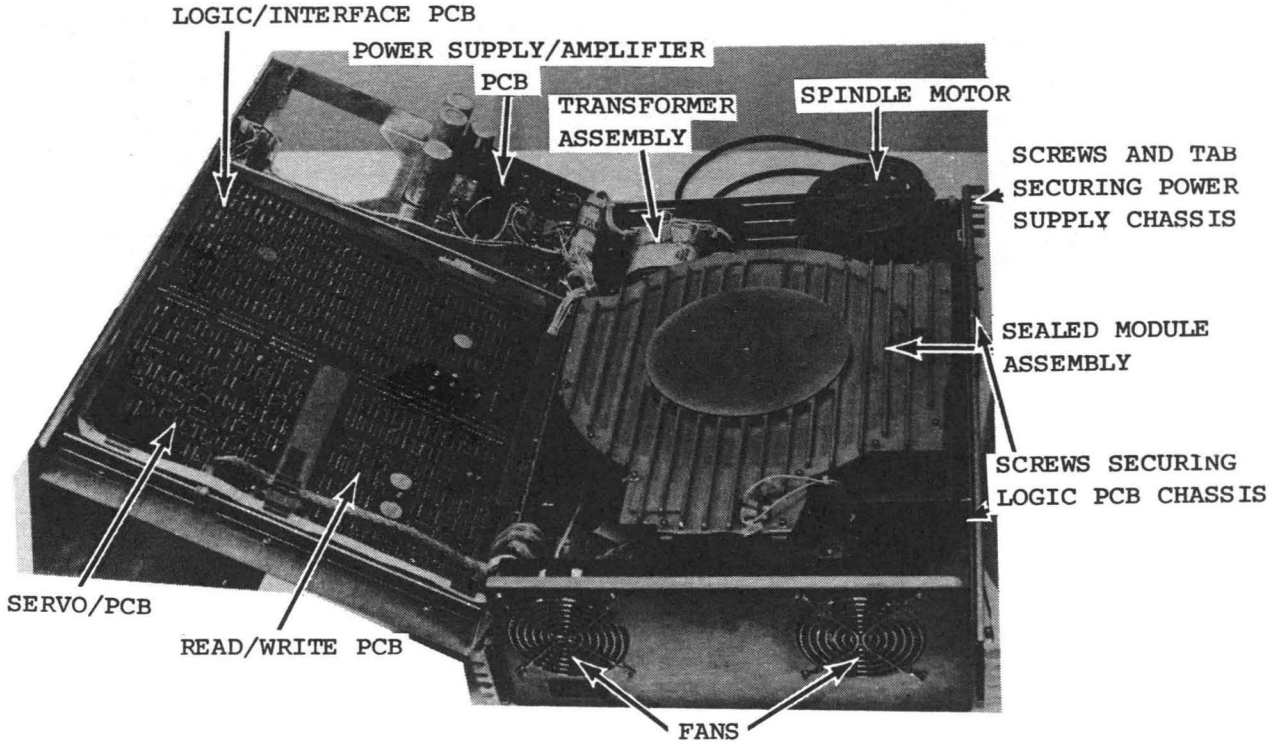


Figure 1-3. Reflex II Modular Component Accessibility

REFLEX II FEATURES, OPTIONS, AND ACCESSORIES

Features

Reflex II features include the following:

- Winchester technology
- Choice of four models (22.6, 67.8, 113.1, and 158.3 megabyte capacities)
- Fixed disc media
- High transfer rate
- Fast access time
- U.L. recognized component
- Sealed disc and positioning unit
- Modular construction
- Lifetime filters
- Quiet operation
- No scheduled maintenance
- Low temperature rise
- High reliability
- Closed recirculating clean air system
- Daisy chain or star (radial) configuration
- Selectable sector length
- Selectable unit address
- Built-in data separator for modified frequency modulation (MFM) recording
- Non-return to zero (NRZ) data at interface

Options

Reflex II optional items include the following:

- Operator indicator panel
- Chassis slides for Radio Electronics Television Manufacturers Association (RETMA) cabinet mounting
- Internal power supply with provision to select voltage combinations and supply all required DC power
- 50 Hz voltage frequency

Accessories

Reflex II accessories include the following:

- Data interface cable
- Signal interface cable
- Cable terminator assembly
- Exerciser Mod III

GENERAL

The Microdata Reflex II series disc drives are high performance, random-access memory devices designed to meet the fixed media storage requirements for minicomputers and small- and medium-sized general purpose computers. Reflex II units are immune to many external environmental conditions, making them exceptionally reliable devices. The unit is designed to be operated in the upright position.

Reflex II is available in four basic versions. Models A, B, C, and D utilize one, two, three or four discs, respectively, on the spindle. Models A, B, C, and D have unformatted storage capacities of 22.6 megabytes, 67.8 megabytes, 113.1 megabytes and 158.3 megabytes of data, respectively. Head positioning time is 6 milliseconds (track to track) and 30 milliseconds (average). Average rotational latency is 8.50 milliseconds. Up to sixteen disc drive units can be daisy-chained from a single controller, providing up to 2532.8 megabytes of unformatted, on-line storage.

Reflex II maintenance requirements are minimal. The need for periodic maintenance, including head alignments, is eliminated due to the integration of the rotating disc, recording heads, and the head positioning mechanism into a single replaceable assembly. A closed loop air circulation and filtration system, combined with positive internal pressure, provides maximum air purity within the assembly.

FUNCTIONAL DESCRIPTION

The Reflex II disc drive is a fixed media unit with fast access times, high data transfer rates, and medium capacity storage. The functional areas are shown and described in Figure 1-4. The disc drive can be divided into the following basic functional areas.

- Input/Output
- Positioning
- Read/Write

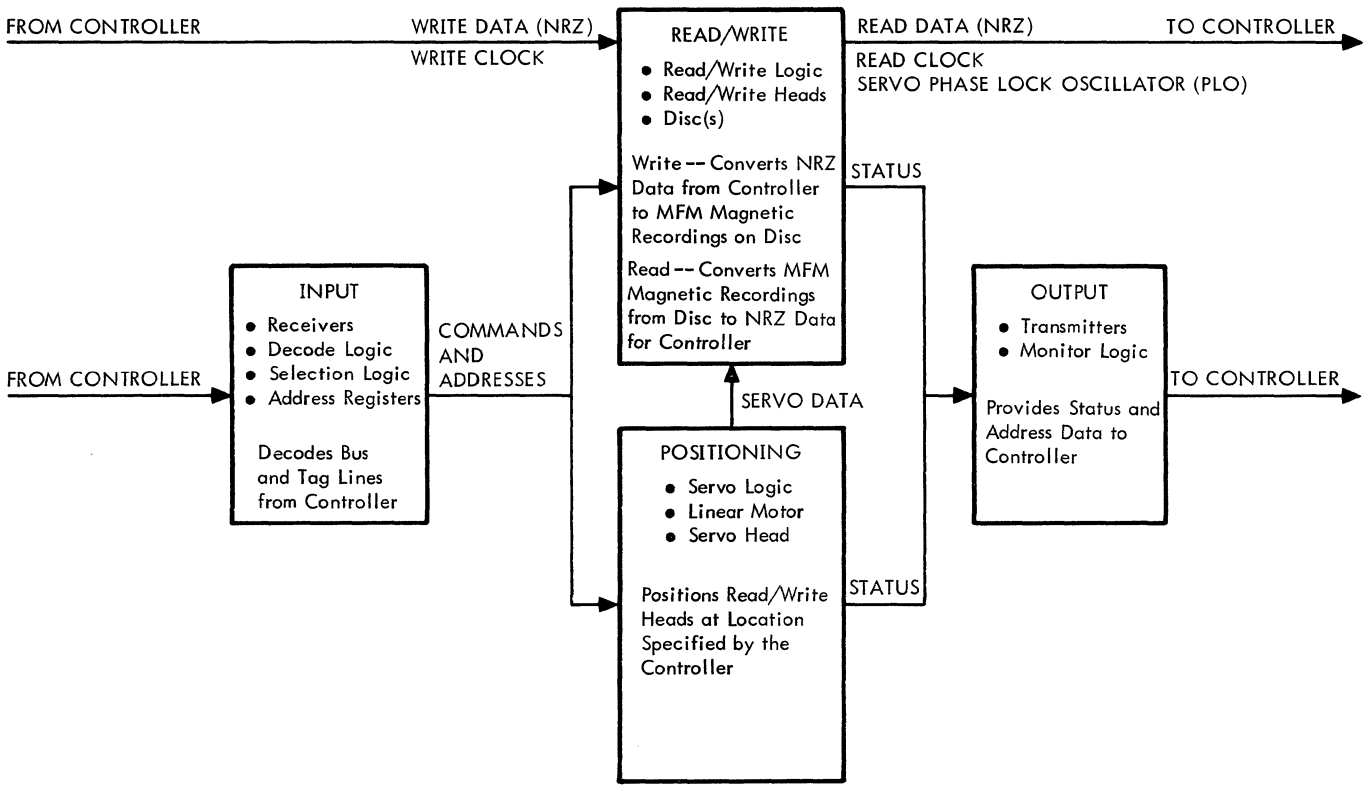


Figure 1-4. Reflex II General Block Diagram

Input

The controller provides the following input interface signals to the drive:

- Address select lines
- Bus and tag lines
- Configuration request
- Write data and write clock lines

1. Address Select

There are four select bus lines and one select tag line. They are connected in parallel to each drive. When the controller activates the select tag line, the drive's address comparison logic looks at the address bus lines and if there is a comparison, the disc drive becomes selected. Selection enables the input and output interface logic of the disc drive.

2. Bus and Tag Lines

There are ten bus lines and three tag lines that are used to provide information to the disc drive. The three tag lines define the information on the bus lines as either addresses or control commands.

3. Configuration Request

The configuration request line is used to differentiate status information from either the moving head disc or the fixed head disc. It is also used to define model type.

4. Write Data and Write Clock

A bidirectional cable is used to present write data and write clock to the drive. It also presents read data, read clock and data from the servo phase lock oscillator (PLO) to the controller. Write data is not directly controlled by the interface logic. The write enable lines are decoded from the bus and tag lines and control the write mode of the drive.

Output

Upon selection, the output interface is enabled and the following information is made available to the controller, when queried:

- Selection status
- Operational status
- Error condition status
- Read data and read clock
- Servo PLO (continuously transmitted, regardless of selection)

Seek end (interrupt) is made available to the controller with or without selection.

Positioning

Positioning is accomplished by the servo logic. The servo logic receives its input from the controller via the input interface. The input interface decodes the input from the controller and determines the necessary position of the read/write heads. This information is then passed to the servo logic, which drives and controls the position of the read/write heads. The read/write heads are moved into their proper position by a linear motor. This motor consists of a stationary permanent magnet surrounding a movable, servo-driven voice coil armature (bobbin) (see Figure 1-5).

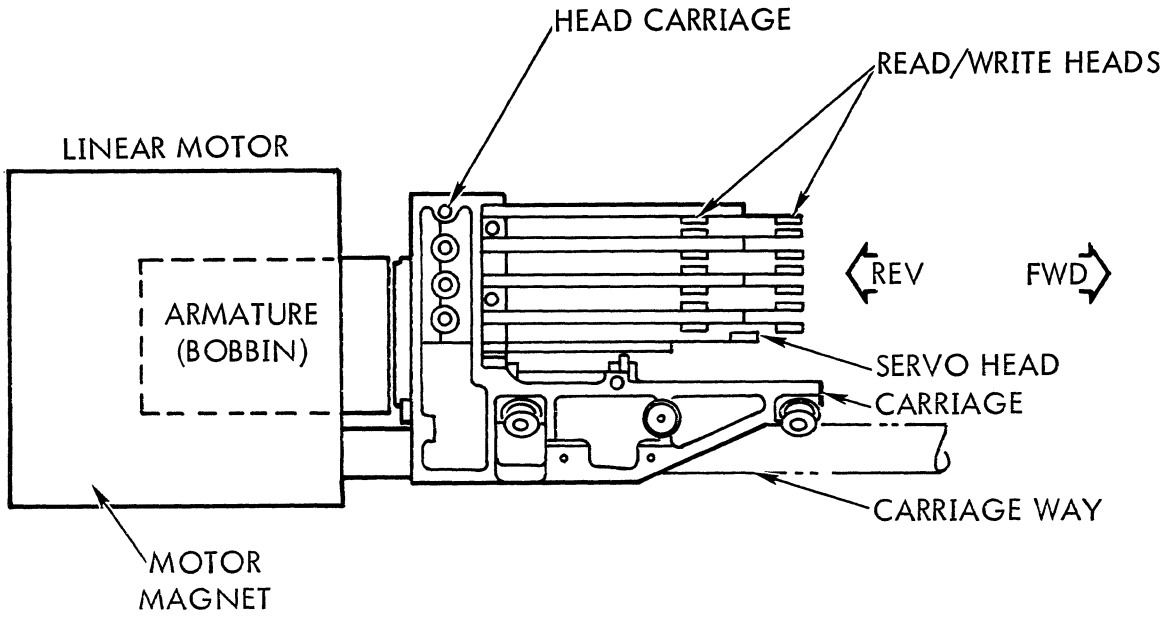


Figure 1-5. Positioner Mechanism

Power for the linear motor is provided from the servo logic by a direct current, which flows through the bobbin. The magnetic field built up around the bobbin by this current causes a reaction with the permanent magnetic field, and the reaction either forces the bobbin away from the permanent magnet or pulls it into the field of the permanent magnet. The direction of movement depends on the polarity of the current flow. Speed depends on the amplitude of the current.

Fastened to the bobbin is a head carriage which holds the read/write and servo heads. The carriage moves freely on ball-bearing rollers. Movement of the bobbin in and out of the permanent magnet moves the carriage backward and forward. This linear travel positions the read/write heads over their respective disc surfaces.

The servo has two modes of operation--a velocity mode and a track follow mode. The velocity mode is evoked when the controller commands the read/write heads to move from their current position (cylinder) to another cylinder. The track follow mode is active whenever the velocity mode is not active. The track follow mode works to maintain the present position of the read/write heads.

During either mode of operation, the servo receives information from the servo head. This information is derived from prerecorded data on the servo disc and is monitored by the read only servo head. The information provided during the velocity mode includes velocity information which allows the servo logic to control the speed of movement. It also includes cylinder boundary information to allow the servo logic to position the read/write heads to the commanded cylinder. The information provided during track follow mode allows the servo logic to maintain the position of the read/write heads.

In addition to the servo control information, the servo data provide information that is used to generate index location, sector pulses, and write clock frequency.

Read/Write

The read/write system includes the read/write logic, read/write heads, and discs. The system consists of the elements necessary to convert NRZ data input to MFM data, record the data, retrieve the data and convert it to NRZ data as output data.

Reflex II employs Winchester technology. This technology uses low mass, high compliance recording heads which fly much closer to the disc surface than permitted by previous technologies. Because of this close proximity to the disc surface, reading and recording may be performed at higher data and track densities, with greater reliability than was possible with the older technologies.

Reflex II uses the cylinder concept with up to four discs providing up to seven read/write data surfaces and one servo data surface. Information is recorded or retrieved from the discs by up to fourteen read/write heads. There are two heads for each recording surface. The read/write heads are mounted in a vertical stack on a single carriage and therefore are positioned together over their respective surfaces.

The discs are evenly spaced and stacked on a central hub. Each disc surface is an aluminum substrate with an oxide coating and a lubricant overcoat. The bottom side of the bottom disc contains the prerecorded servo data.

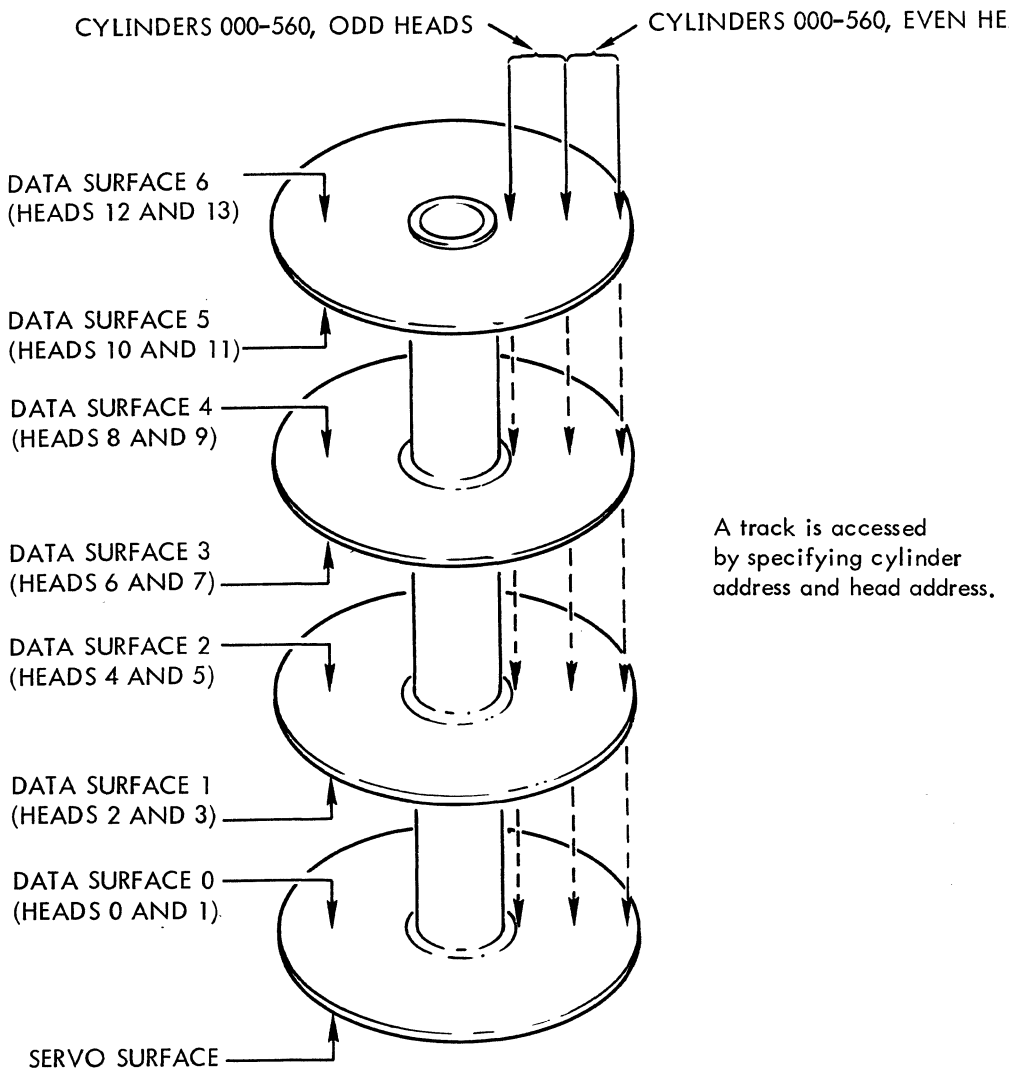


Figure 1-6. Reflex II Cylinder Concept

Data is recorded by magnetizing digital bit patterns in concentric circles (cylinders) on the recording surfaces. With two heads per surface, there is an inner and outer cylinder. The inner cylinder is comprised of the odd numbered heads while the outer cylinder is comprised of the even number heads. As shown in Figure 1-6, each surface contains 561 cylinders. Since each surface has two heads, there are 1122 tracks per surface. The cylinders are numbered 000 through 560. The cylinder nearest the outer edge of the disc is the beginning of the even numbered heads and the odd numbered heads begin with the cylinder nearest the center of the recording surface.

When the head carriage is moved to a given cylinder position, each read/write head is positioned over a corresponding track on its recording surface. For example, when the head

carriage is moved to cylinder 100, head 0 is positioned over track 100 on surface 0 in the outer cylinder boundary. Head 1 will be located over track 100 on surface 0 in the inner cylinder boundary and head 2 will be positioned over track 100 on surface 1 in the outer cylinder boundary.

To select a particular track for recording or retrieval of data, the following is performed:

(1) The head carriage is moved to the cylinder containing the track to be accessed.

(2) The appropriate read/write head for the desired track is selected.

Therefore, a complete track address requires both a cylinder address and a read/write head address.

When writing data, the read/write head is essentially an electromagnet that can concentrate a high magnetizing force over a very small area of the adjacent recording surface. The flux field is alternated to magnetize the disc with the desired bit pattern.

When reading data, the read/write head operates as a sensor. A flux reversal on the recorded surface induces a voltage across the electromagnetic coil. This voltage is amplified and conditioned to allow recovery of the recorded data.

PHYSICAL DESCRIPTION

Reflex II is a family of fixed disc units, enclosed with removable top covers. Reflex II has a front air intake panel to channel air from the front to the rear and to keep out dust and dirt.

The disc drive consists of a sealed module assembly, cables, panel, frame, power supply, printed circuit boards and covers. The unit will accommodate chassis slides for standard RETMA cabinet mounting, with locks to maintain the drive position in the cabinet.

The sealed module assembly is a field replaceable assembly. It is comprised essentially of the spindle, discs, carriage lock, heads, carriage, way, positioning motor, crash stops, air filters, and metal structure.

Attached to the sealed module are the brake, ground brush, spring-loaded spindle drive motor, and drive belt. These items are field replaceable along with the power supply and printed circuit boards.

The discs spin counterclockwise as viewed down from the top of the assembly.

The panel contains a write protect switch and indicators for ready, write protect status, and fault conditions.

The disc spindle is mounted in the sealed module assembly and is driven by a 115 VAC drive motor. The motor and spindle are coupled by a pulley and belt system designed to provide a disc rotational speed of 3530 rpm.

Cooling air is provided by two front mounted fans with 120 CFM flow capability. Air flow is into the front, through the unit and out the rear. Care must be taken not to block the air flow path either at the front or at the rear.

The clean air system is contained within the sealed module assembly and consists of two absolute filters, an air pump and seals. It is implemented to control pressure levels within the module.

SAFETY FEATURES

Operator

All exposed metal parts are at earth-ground potential. All moving parts and potentially hazardous voltages are covered, except when being serviced.

Drive

The linear positioning motor is protected against potential burnout by removing servo power to the motor if a motion command (seek, restore, head load) is not completed within 1-1/2 seconds. Additionally, if the motor is continuously driven against the mechanical stops, protective fuses will blow before either motor or amplifier damage can occur.

The spindle motor is protected against excessive heating by a thermo-cutoff in the motor. (Excessive heating may be caused by repeated start-stop cycles at a rate greater than three consecutive start-stop cycles).

Data

There is a write enable/disable switch to disable (prevent) writing when not desired. Extensive safety circuits are present to detect abnormal conditions within the drive and disable write operations if any abnormal condition is detected (see Section 2).

Reflex II specifications are listed in Table 1-1.

TABLE 1-1

REFLEX II SPECIFICATIONS

Operational	Model A	Model B	Model C	Model D
Track density (TPI)	478	478	478	478
Number of discs	1	2	3	4
Number of data surfaces	1	3	5	7
Number of data cylinders	561	561	561	561
Data heads per cylinder	2	6	10	14
Data tracks per surface	1122	1122	1122	1122
Data bytes per track	20160	20160	20160	20160
Data bytes per surface (MEGA)	22.62	22.62	22.62	22.62
Data byte capacity (MEGA)	22.62	67.86	113.1	158.3
Disc rotation speed (RPM)	$3530^{+3}_{-7}\%$	3530	3530	3530
Data byte transfer rate (MHz)	1.186	1.186	1.186	1.186
Data bit transfer rate (MHz)	9.489	9.489	9.489	9.489
Data bit cell time (nanosecond)	105.4	105.4	105.4	105.4
Bit density, inside track (BPI)	6427	6427	6427	6427
Optional fixed head per track data byte capacity (MEGA)	1.2	1.2	1.2	1.2

Recording Technology	
Write data input	NRZ at the interface, MFM at the disc
Read data output	MFM at the disc, NRZ at the interface
Read/write heads	
Number	Two (2) per disc surface
Type	IBM 3350 style
Format	Fixed or variable length, user determined

Accessing	
Head positioning	High efficiency voice coil linear motor with electronic velocity transducer is used for cylinder positioning of read/write heads.
Head positioning time	6 milliseconds track-to-track, 30 milliseconds average, 55 milliseconds maximum

Start time	50 seconds maximum (drive ready)
Stop time	10 seconds maximum
Rotational latency	8.50 milliseconds average 17 milliseconds nominal 18.19 milliseconds maximum
Error rates	
Head positioning	Less than one error in 10^6 motion commands
Recoverable	Less than one error in 10^{10} bits
Nonrecoverable	Less than one error in 10^{13} bits
Mean time between failure (MTBF)	Greater than 5000 hours
Mean time to repair (MTTR)	Less than one hour
Dimensions	
Width	17.5 inches (44.5 cm)
Height	7 inches (17.8 cm)
Depth	28 inches (71.1 cm)
Weight	100 pounds (45 kg)
Input Power Requirements	
AC voltage	100, 115, 120, 200, 208, 220, 240
	AC $^{+10}_{-15}$%
	Single phase
Amperes	
Start	20A rms at 115 VAC, first 10 seconds
Operating	4A rms at 115 VAC, typical
Power consumption	350 watts
Line frequency	60 Hz or 50 Hz ($\pm$1 Hz)
DC voltage	+9V @ 3 amperes
	-9V @ 2 amperes
	$\pm$18V @ 3 amperes
	NOTE: DC voltage input is not required for drives equipped with optional internal DC power supply.

TABLE 1-1, REFLEX II SPECIFICATIONS (Cont'd)

Environmental	
Temperature	
Operational	15°C to 55°C (59°F to 131°F) maximum rate of change 10°C (18°F) per hour. Inlet air must be within 15°C to 41°C (59°F to 106°F)
Storage	-50°C to +80°C (-58°F to +176°F) maximum rate of change 40°C (72°F) per hour.
Relative humidity	
Operational	10 percent to 80 percent noncondensing
Storage	10 percent to 80 percent noncondensing
Airflow	120 CFM minimum, unrestricted
Altitude	
Operational	-100 ft. to +6000 ft. (-30m to +1800m)
Storage	21 inches to 32 inches mercury (53 cm to 81 cm)

NAMEPLATE IDENTIFICATION

Figure 1-7 shows the nameplate which is affixed to the top left rear of the unit. The information provided includes the model name, top assembly part number, model ID, serial number, and power requirements as to VAC, ampheres, and Hz. A listing of the top assembly part numbers is provided in Appendix A.

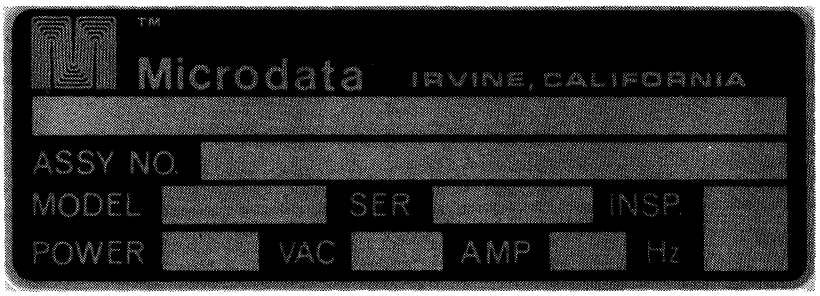


Figure 1-7. Nameplate

SECTION 2

PHYSICAL PLANNING AND INTERFACE REQUIREMENTS

INTRODUCTION

This section provides information for site considerations, including space, power, configuration and interface requirements.

ENVIRONMENTAL CONDITIONS

The typical environment for the Reflex II is an air-conditioned office or data processing center. However, this type of environment is not necessary. The Reflex II disc drive should not be directly exposed to outside weather or to unusual chemical or atmospheric gas conditions. The total sum of the environment is the major consideration that will affect the life of the product. While scheduled maintenance is not normally required, conditions of the environment may give rise to periodic maintenance such as vacuuming or removing dust accumulation. Care should be exercised not to exceed the environmental specifications listed in Section 1 and those noted in this section.

Stabilization

The Reflex II disc drive is subject to a stabilization period of four hours minimum, only when introduced to an in-specification environment from an out-of-specification environment.

Temperature

The drive may be bathed or placed in air with a temperature range of 15°C to 55°C (59°F to 131°F). However, the front panel air inlet temperature must be within 15°C to 41°C (59°F to 106°F). The operating temperature rate of change is limited to 10°C (18°F) per hour.

Humidity

The operational humidity range is 10 percent to 80 percent, noncondensing, with a wet-bulb temperature of less than 25.6°C (78°F).

Altitude

The altitude range is the sum of the temperature, humidity, and barometric pressure limits. The operational barometric pressure range is -100 to +6000 feet (-30 to +1800 m).

Air Flow

Uninhibited air flow must be allowed through the disc drive. The direction of the air flow is from front to back. The openings at the front and rear must be unrestricted to allow for 120 CFM of air flow.

Noise Level

The Reflex II disc drive has been designed not to exceed the noise criteria (NC55) standard for noise pollution.

Storage

For environmental limits during storage, see the specifications listed in Section 1.

SPACE REQUIREMENTS

Reflex II fits within box dimensions of 7 inches (17.78 cm) high, 28 inches (71.12 cm) deep, and 17.5 inches (44.45 cm) wide. The weight of the unit is less than 100 pounds (45 kg). See Figure 2-1 for an outline of physical dimensions.

Optional chassis slides are available for standard RETMA cabinet mounting. The slides allow for the performance of all maintenance activities through frontal access. The slides also allow for the drive to be locked in position when retracted in the cabinet.

POWER REQUIREMENTS

Power requirements are different depending on whether the optional internal power supply (transformer assembly) is installed. In either case, Reflex II has been designed to be tolerant of AC line voltage fluctuations. The only requirement is that the AC input power and ground must be consistent to, or common with, the other computer peripheral equipment at the same installation.

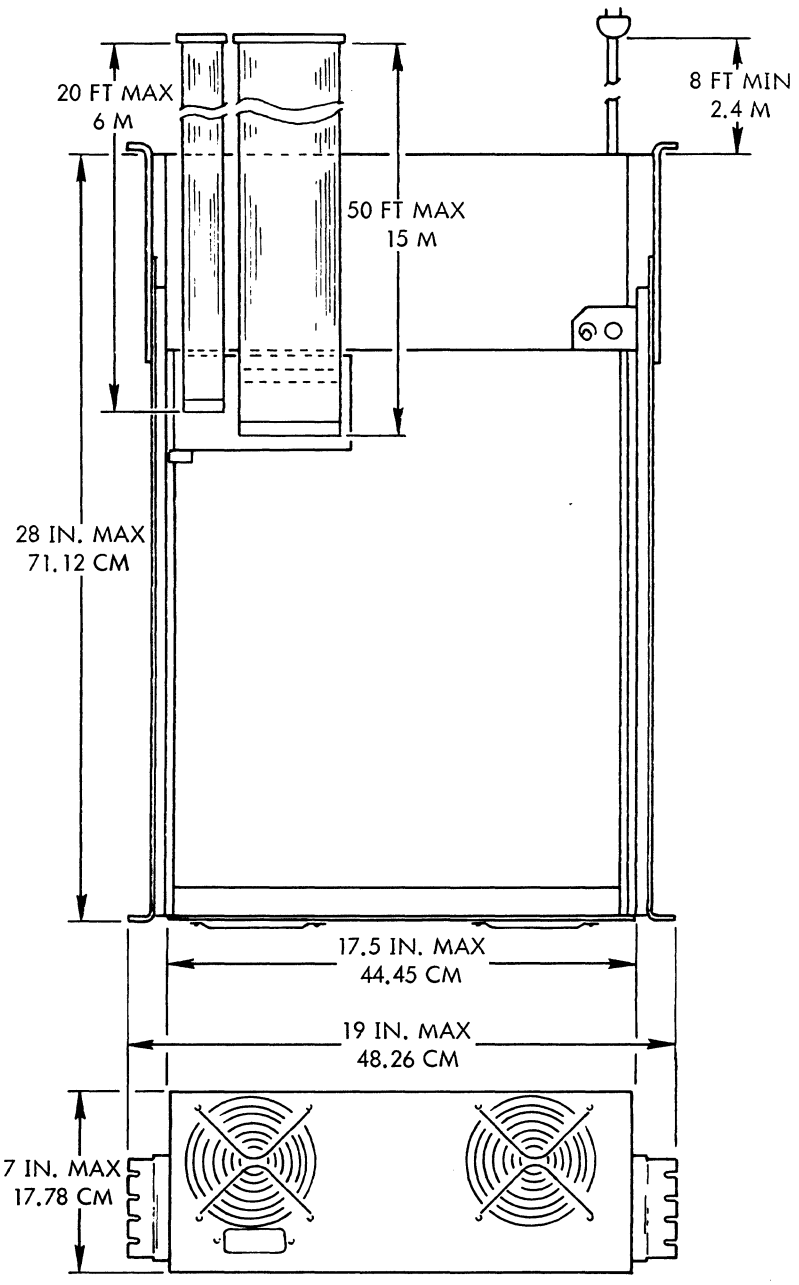


Figure 2-1. Physical Dimension Considerations

Input AC Voltage Fluctuations

The AC voltage should not vary from its nominal value longer or more frequently than the limits shown in Table 2-1. All occurrences must be noncoincident with each other.

TABLE 2-1

INPUT AC VOLTAGE FLUCTUATIONS

Input Voltage (Percent of nominal)	Duration (milliseconds)	Occurrence
0	10	1 per 600 seconds
50	10	1 per 10 seconds
130	60	1 per 30 seconds
200	10	1 per 240 seconds

Power Cable Configurations

The standard Reflex II configuration is for 115V 60 Hz. For this, a 9 foot (2.7 m) nominal, 8 foot (2.4 m) minimum power cable and connector is furnished to plug into a standard NEMA outlet as shown in Figure 2-2.

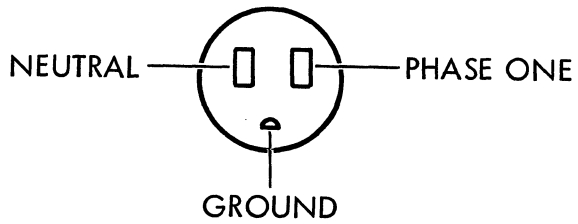


Figure 2-2. Standard AC Power Outlet Configuration

For voltage and frequency combinations other than 115V 60Hz, a connector is not provided at the end of the power cable. The user may connect his own connector per the power cable wire assignments listed as follows:

Power	Wire Color
Phase one	Black or brown
Neutral	White or blue
Ground	Green or green yellow

AC Power With Optional Internal Power Supply

Reflex II has internal taps to accommodate any one of the following single phase voltages: 100, 115, 120, 220, and 240. The voltage tolerances are +10 and -15 percent. The frequency of each voltage may be either 50 ±1 or 60 ±1Hz.

The run current is 4 amperes AC root mean squared (RMS) typical for 115 VAC, at a 70 percent power factor. However, there is a start current surge of 20 amperes. The typical current characteristics for 115 VAC are shown in Figure 2-3.

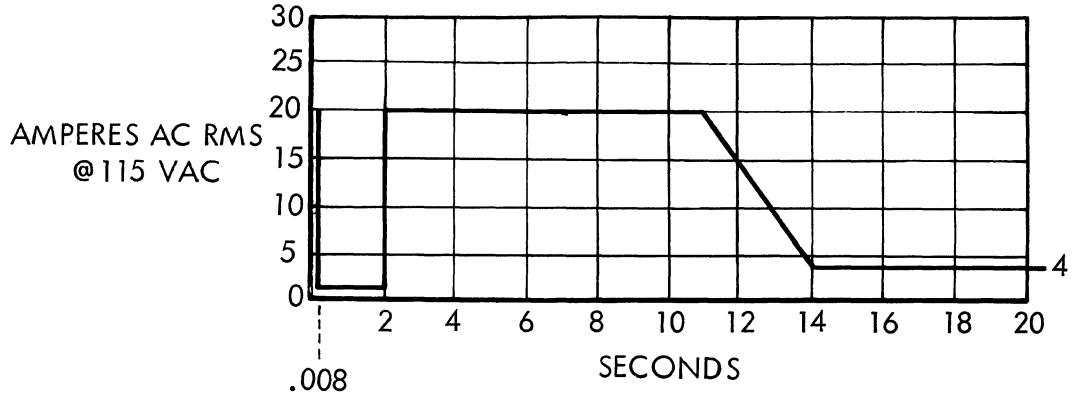


Figure 2-3. Typical Current Characteristics With Internal Power Supply

AC Power Without Optional Internal Power Supply

The input power requirement is 115 VAC +10 -15 percent, single phase with a frequency of either 50 ±1 or 60 ±1Hz.

The current requirement is 2.5 amperes RMS, nominal, at 115 VAC (considering a 70 percent power factor) with a start current surge of 20 amperes. The typical current characteristics are shown in Figure 2-4.

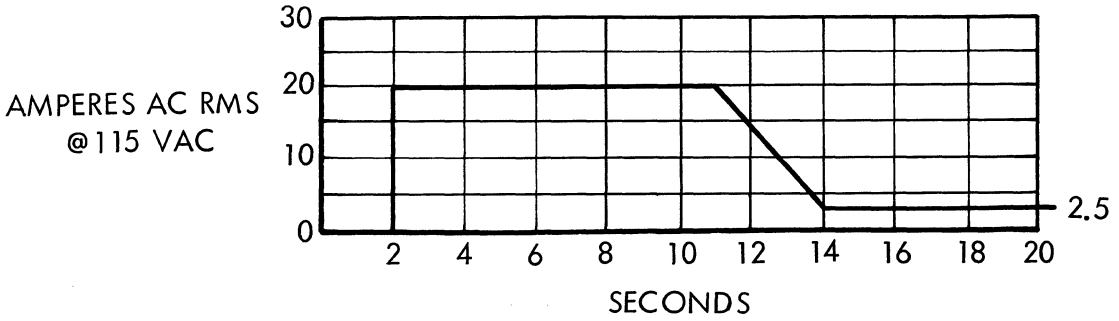


Figure 2-4. Typical Current Characteristics Without Internal Power Supply

DC Voltage Without Optional Internal Power Supply

Table 2-2 lists the required DC voltages with their appropriate load current characteristics. Each voltage is independently fused to protect the drive. External fuses may be necessary to protect the source cable or DC sources. Each voltage is filtered in the drive with a 15,000 microfarad (minimum) electrolytic capacitor. The incoming DC voltages must attain specified stable levels within 200 milliseconds of each other.

TABLE 2-2

DC VOLTAGE REQUIREMENTS

Voltage			RMS Ampere		500 KHz Impedance	Maximum Transient
Min.	Nom.	Max.	Min.	Max.	Max. Ohms	Current Ampheres
+ 8.0	+ 9.0	+10.0	1	3	0.05	1
-10.0	- 9.0	- 8.0	0.5	2	0.05	1
+16.5	+18.0	+19.5	1	3	0.10	5
-19.5	-18.0	-16.5	1	3	0.10	5

The voltages are conected to Reflex II connector J26 with pin assignments as shown in Figure 2-5. The mating connector that must be supplied to J26 is a MOLEX connector (part number 19-10-1091), with pins (part number 02-09-1103 or equivalent) for wire gauges of 14 to 20.

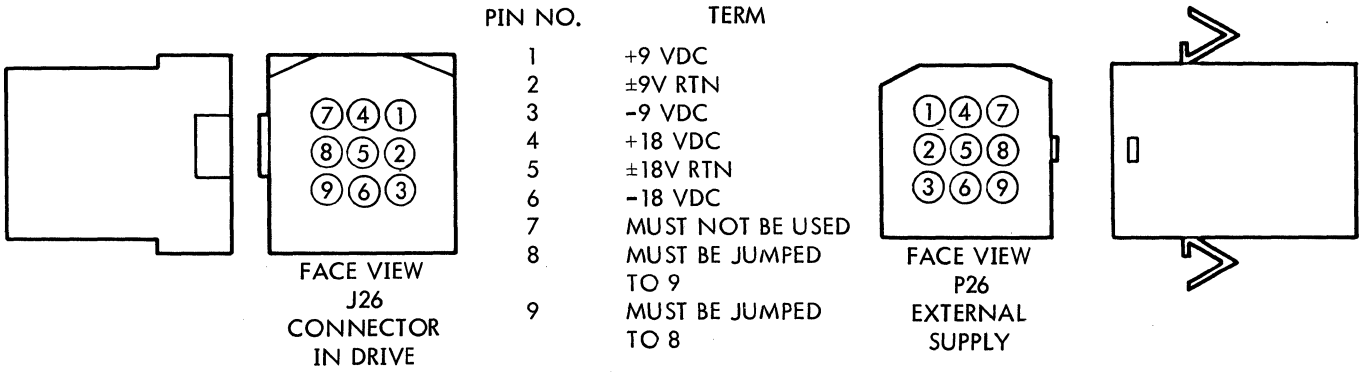


Figure 2-5. DC Voltage Supply Cable Pin Assignments

Grounding

REFLEX II grounding is of the distributed grounding scheme and the terms "frame ground" and "signal ground" become one and the same. A jumper between E2 and E4 on the power supply amplifier PCB is one of the points of commonality of frame and signal ground. An external frame (earth) ground must be connected to the power supply/amplifier PCB at E1 (Figure 2-6). This external GND may be via a system's cabinet frame, but must ultimately connect to earth ground. A 0.25-inch male terminal tab is provided for this connection.

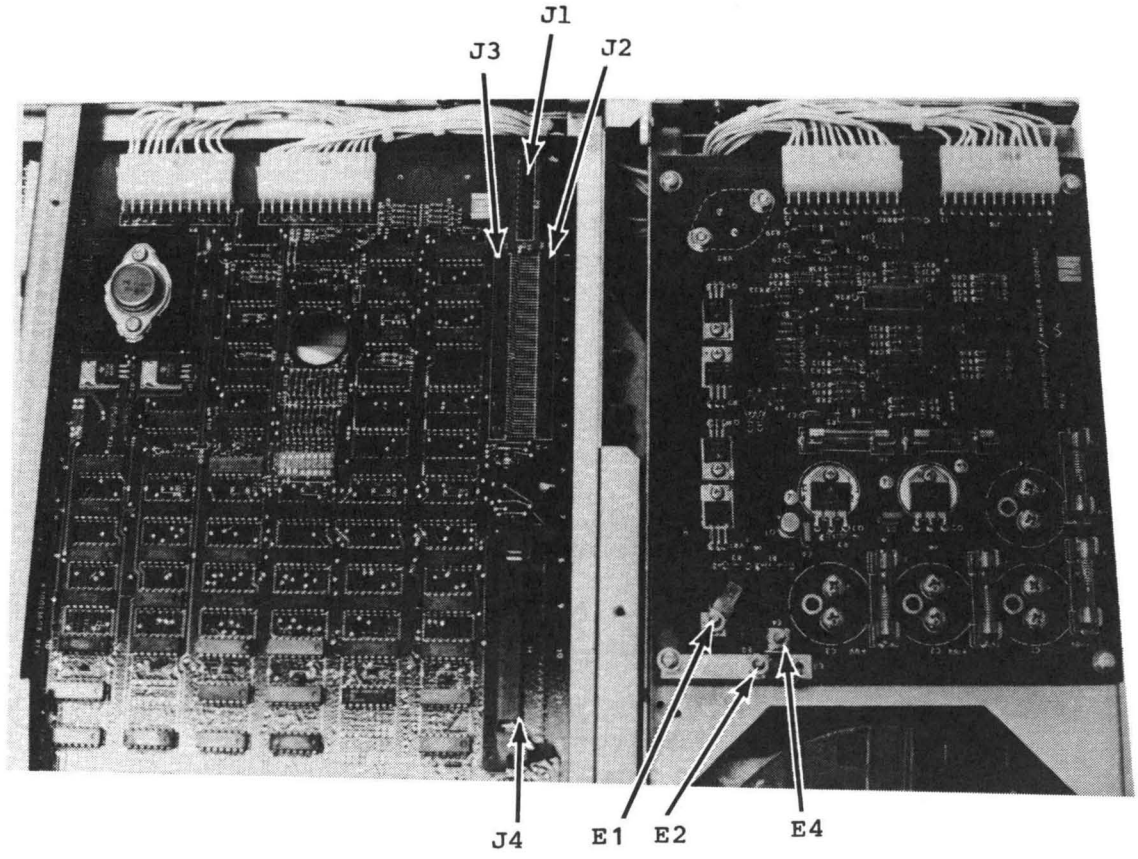


Figure 2-6. Cable Connections and Ground Tie Point

INTERFACE REQUIREMENTS

Logic Interface

All input and output signals are digital and are received and transmitted differentially through the data and signal cables. Industry standard 75110 transmitters are required. Differential receivers with at least 100MV sensitivity and ±3V common mode capability are to be used (±25MV for I OPNCBLDET signal).

Signal polarity convention for differential signals is defined so that if "SIGNAL" is more positive than "SIGNAL/", the line is considered to be active unless otherwise specified.

Cabling

Three cables are required: the AC power cable, the data cable, and the signal cable. The AC power cable is supplied as part of the drive.

1. Data Cable

The data cable is a 26-conductor shielded, flat cable and must be connected directly to the controller. The maximum permissible length for the data cable is 20 feet (6 m). The cable's characteristics are;

Impedance:	130 ± 15 ohm, conductor to adjacent conductor
	65 ohms nominal, conductor to ground.
Propagation:	1.7 nanoseconds per foot, nominal
Capacitance:	29 pfd per foot, conductor to ground, nominal

2. Signal Cable

The signal cable is a 60-conductor, 30-twisted pair, flat cable. This cable may connect either directly to the controller or as a daisy-chain configuration to the controller (see Figure 2-7). The configurations shown in Figure 2-7 are for possible OEM use only. Figure 2-7A shows the only acceptable configuration for

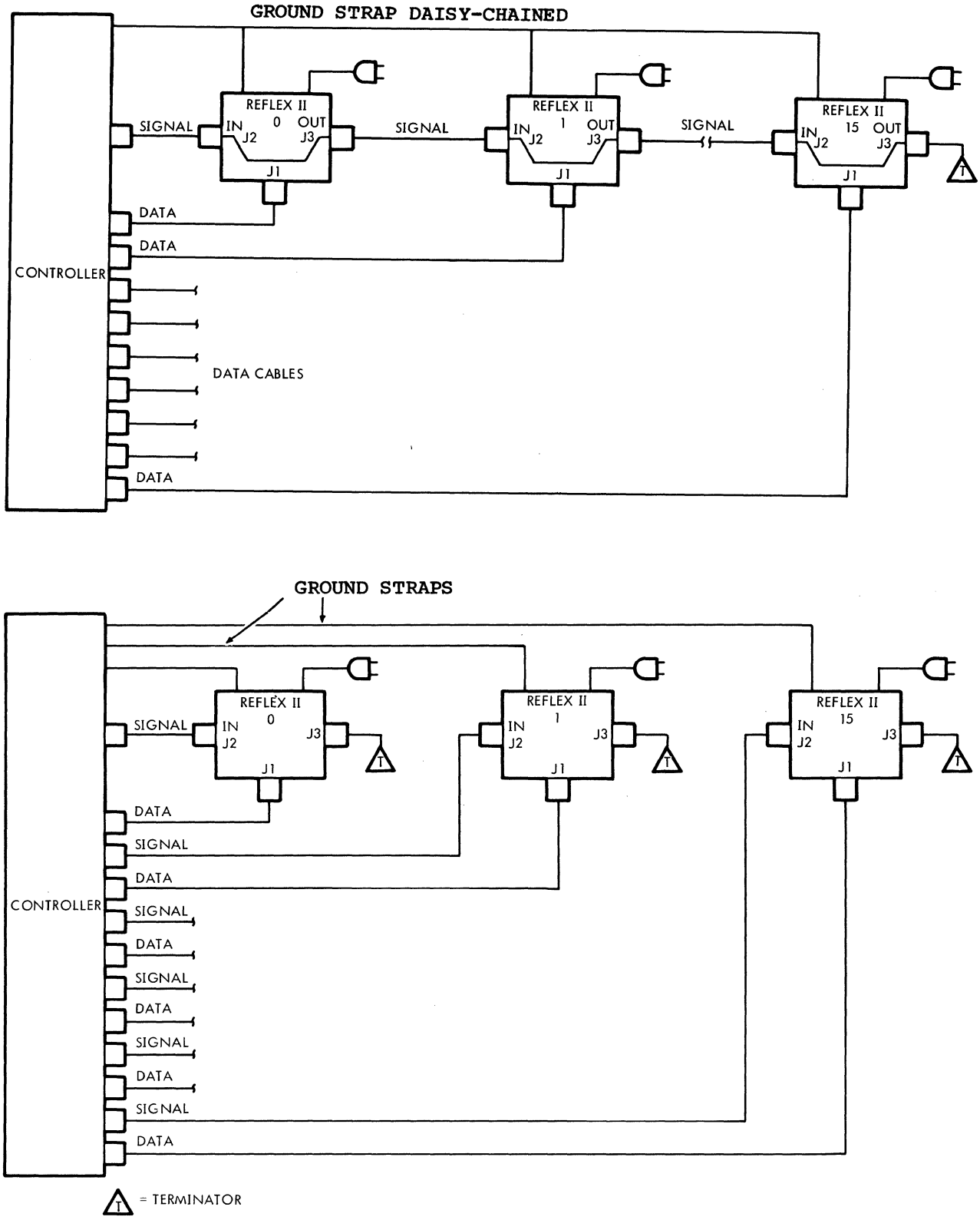


Figure 2-7. Daisy-Chain (top) and Star Configuration (bottom), For possible OEM use ONLY.

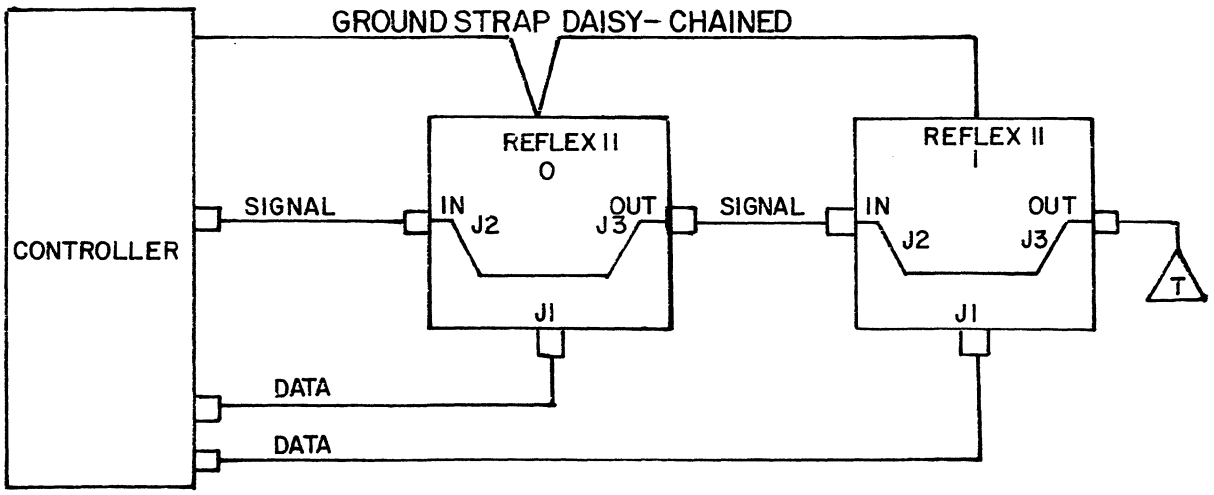


Figure 2-7A. Reality System Daisy-Chain Configuration

use in a Reality System. For a daisy-chain configuration, there is a requirement for the controller to have on driver (transmitter) for each four drives for the I OPNCBLDET line. In either configuration, the signal cable may not exceed 50 feet total aggregated length from controller to terminator. The cable's characteristics are:

Impedance:	100 ±10 ohm between conductors of same pair
Propagation:	1.7 nanoseconds per foot, nominal
Capacitance:	22 pfd per foot between conductors of same pair, nominal

3. Frame Ground Cable

A ground cable must be connected to the drive for connecting frame ground to earth ground.

4. Available Cables

Cables available for cabling purposes are as follows:

Signal Cable - 60 Conductor	
Controller to Drive...	A20013307-xxx *
Drive to Drive...	A20013339-xxx *
Data Cable - 26 Conductor...	A20000979-xxx *

* The dash number controls cable length, -001 is standard.

5. Connector Jacks

For available lengths, see the drawing for the applicable cable in Section 6. Connector jacks for cabling are as follows:

Connector	Reference
Signal J2, J3	AMP 3-87227-0 or equivalent
Data J1	AMP 1-87227-3 or equivalent

6. Connector Orientation

The connector pin orientation in the drive is shown in Figure 2-8. The connector locations are shown in Figure 2-6.

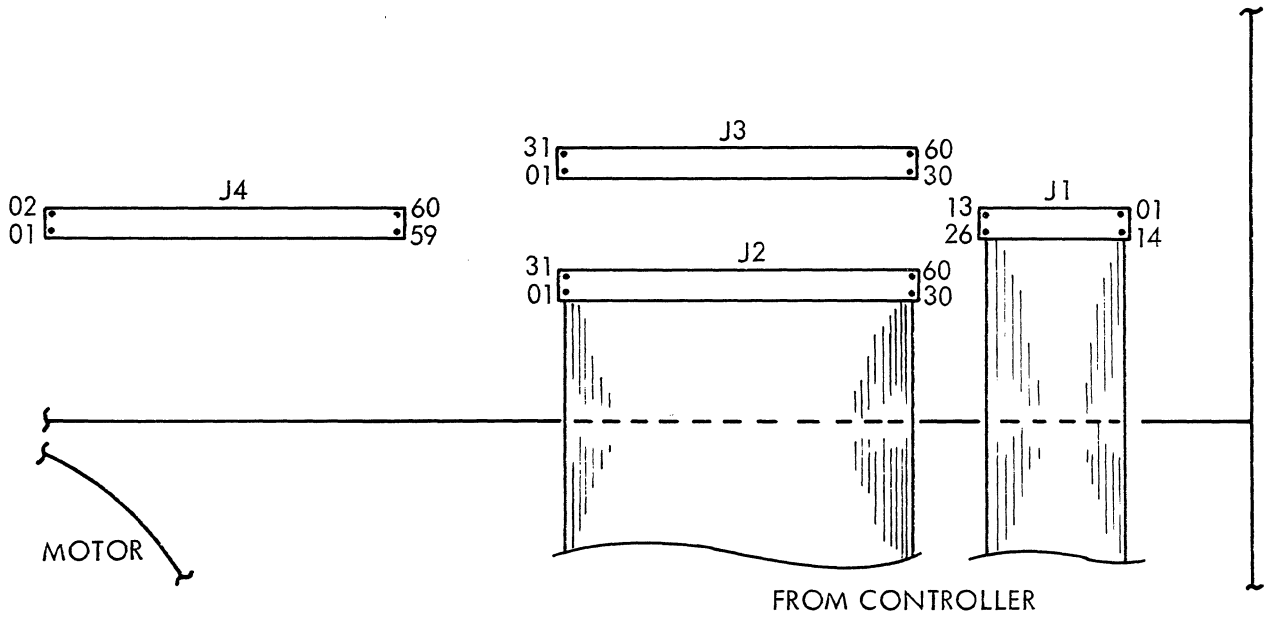


Figure 2-8. Connector Pin Orientation

Signal Cable Descriptions

The signal cable consists of 27 signals. Each signal is made up of two wires. For installations using more than one Reflex II drive, the signal cables may be daisy-chained or star-cabled (see Figure 2-7).

1. Pin Assignments

The signal cable signal listing and pin assignments are shown in Figure 2-9. The arrow indicates the transmitted direction. The pin number assignments are shown for the signal pair with the "/" used to describe polarity convention. The prefix "I" is used to indicate that the signal is at the interface.

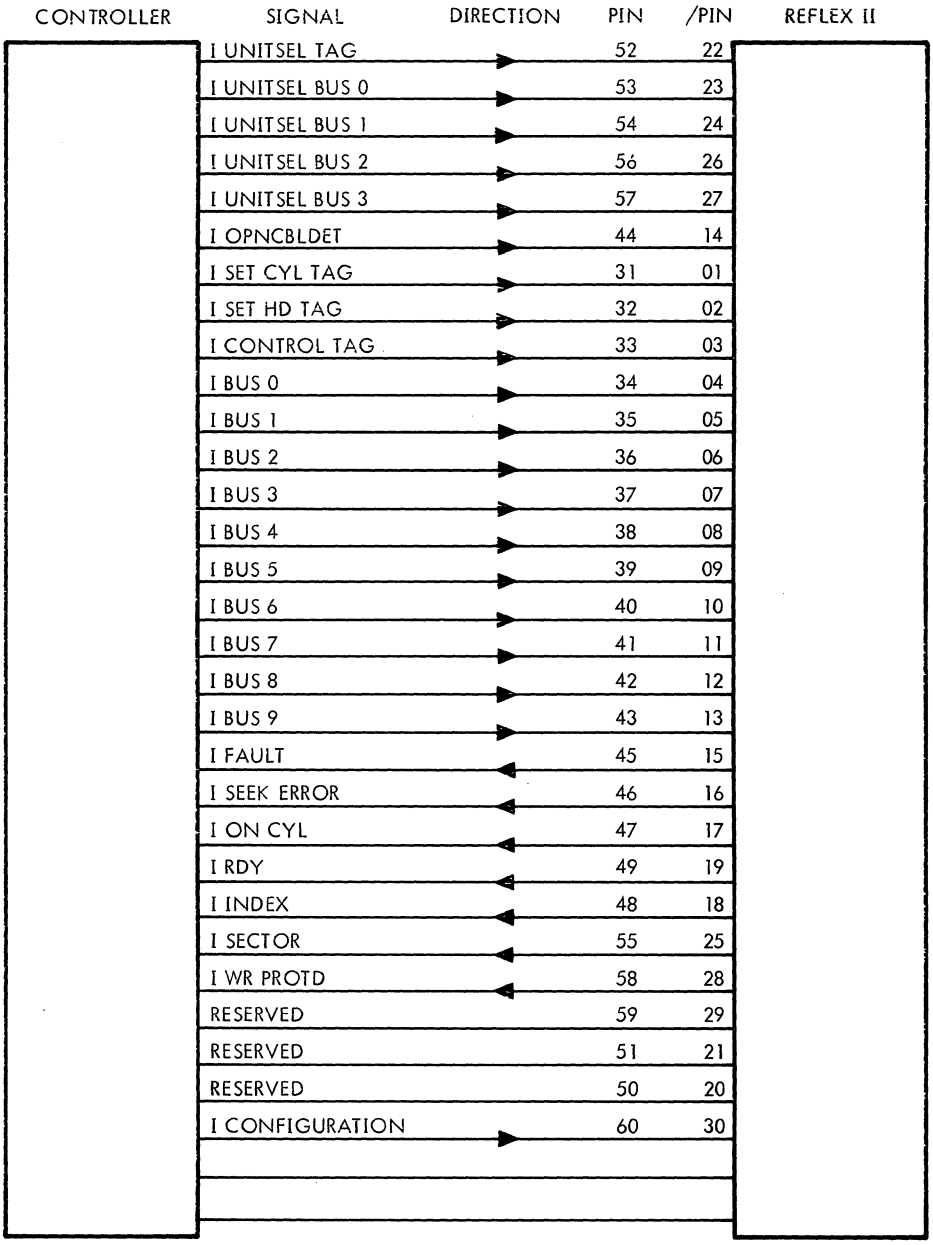


Figure 2-9. Signal Cable Pin Assignments

2. Signal Cable Definitions

The signal cable signals break into three groups. These groups provide selection, operation, and status, with operation breaking into address and control functions.

a. Open Cable

The first signal necessary is I OPNCBLDET. This signal must be inactive (cable connected) to allow selection, which in turn allows the other functions to work.

I OPNCBLDET active indicates the signal cable is not connected or a controller power failure. This signal is active when its "/" term is more positive than its other side. This term active will retract the heads, inhibit writing, and disable all signal cable functions.

b. Drive Selection

With I OPNCBLDET inactive, selection is allowed. Selection is accomplished by four bus lines (I UNITSEL BUS 0-3) and one tag line (I UNITSEL TAG). Selection occurs when the unit select bus lines are equal to the unit select switches, when the unit select tag line becomes active. The unit select bus lines are weighed so that bus 0 is the least significant bit and bus 3 is the most significant bit. The unit select switches are located on the logic/interface board, in the dip switch package S1.

The unit select bus lines must be active at least 200 nanoseconds before the unit select tag line becomes active. If the binary address agrees with the unit select switches, UNIT SELECTED will become active 400 nanoseconds later. It will remain active for 200 nanoseconds beyond the unit select tag remaining active. I UNITSEL TAG must remain active for the duration of selection (see Figure 2-10).

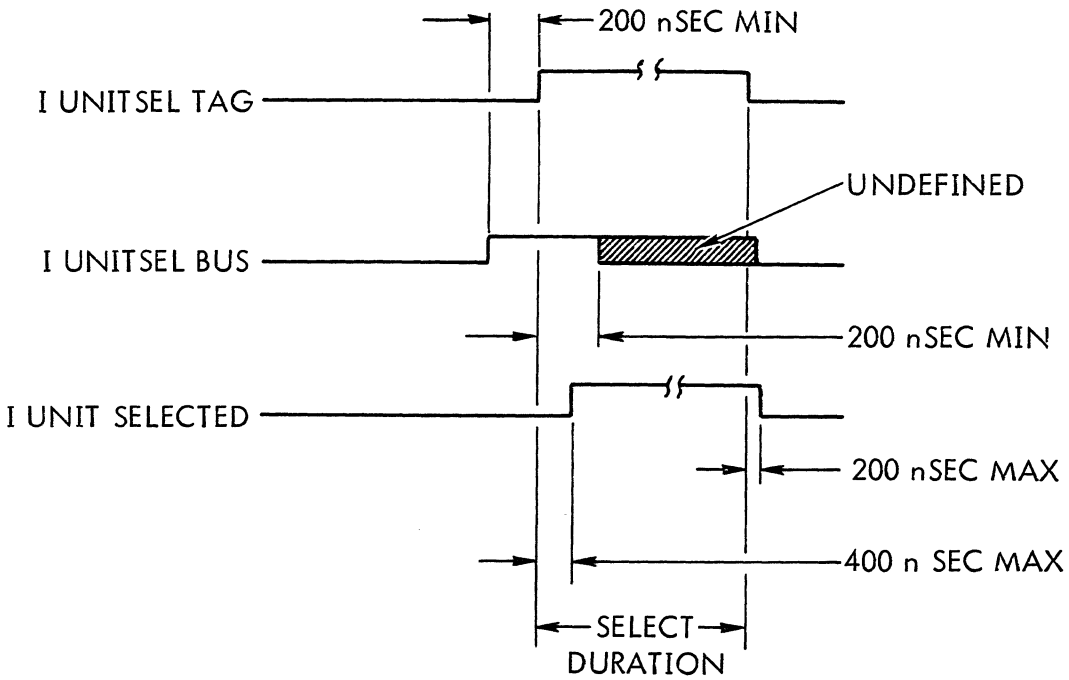


Figure 2-10. Drive Selection

c. Operation Commands

The operation group of signals breaks into address and control functions which are transferred on 10 bus lines and decoded with 3 tag lines as shown in Table 2-3.

TABLE 2-3

OPERATION SIGNALS

	I SET CYL TAG	I SET HD TAG	I CONTROL TAG
I BUS 0	CAR 1	HAR 1	WRT
I BUS 1	CAR 2	HAR 2	READ
I BUS 2	CAR 4	HAR 4	OFFSET FWD
I BUS 3	CAR 8	HAR 8	OFFSET REV
I BUS 4	CAR 16	*HAR 16	R/FAULT
I BUS 5	CAR 32	*HAR 32	--
I BUS 6	CAR 64	--	RESTORE
I BUS 7	CAR 128	*FXHDSEL	DSERLY
I BUS 8	CAR 256	--	DSLATE
I BUS 9	CAR 512	--	--

*Required for fixed head per track option

CAR = Cylinder Address Register
HAR = Head Address Register

I SET CYL TAG -- When active, the bus lines are decoded as the next cylinder the servo is to seek. The trailing edge of the signal starts the seek. If I SET CYL TAG is issued while ON CYL or RDY are not active, a seek error will occur. The seek error may be cleared by doing a restore command. The timing requirements are shown in Figure 2-11.

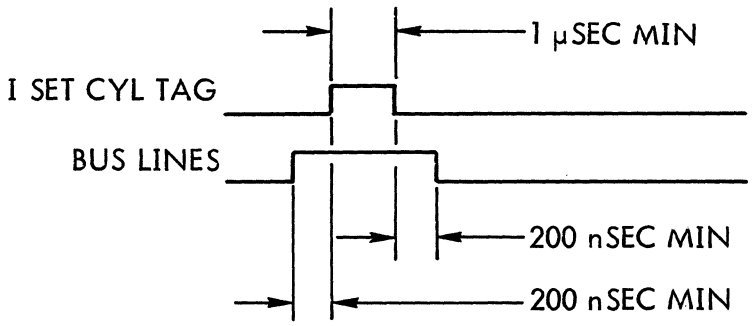


Figure 2-11. Set Cylinder Timing

I SET HD TAG -- When active, bus lines 0-3 are decoded as the next moving head to be selected. With the fixed head-per-track option present and with the fixed head select signal active, bus lines 0-5 are decoded as the next fixed head to be selected. The timing requirements are shown in Figure 2-12.

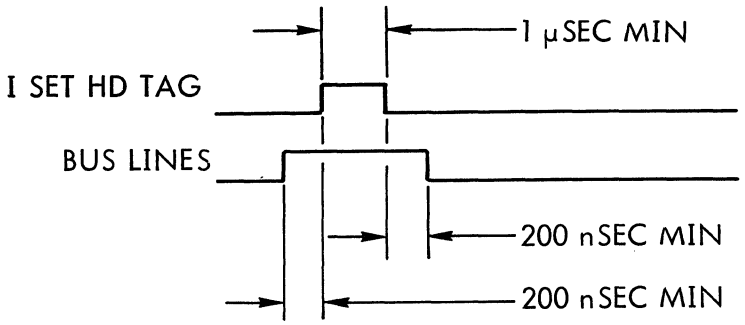


Figure 2-12. Set Head Timing

I SET HD TAG must not become active earlier than 1 μsecond after the I SET CYL TAG becomes inactive. The head selection register is reset by issuing a restore command, or cycling power on-off-on, or by issuing I SET HD TAG with the buses not active.

Typical timing for the I SET CYL TAG and I SET HD TAG lines are shown in Figure 2-13, where the next cylinder address is 85 and the next head address is 9.

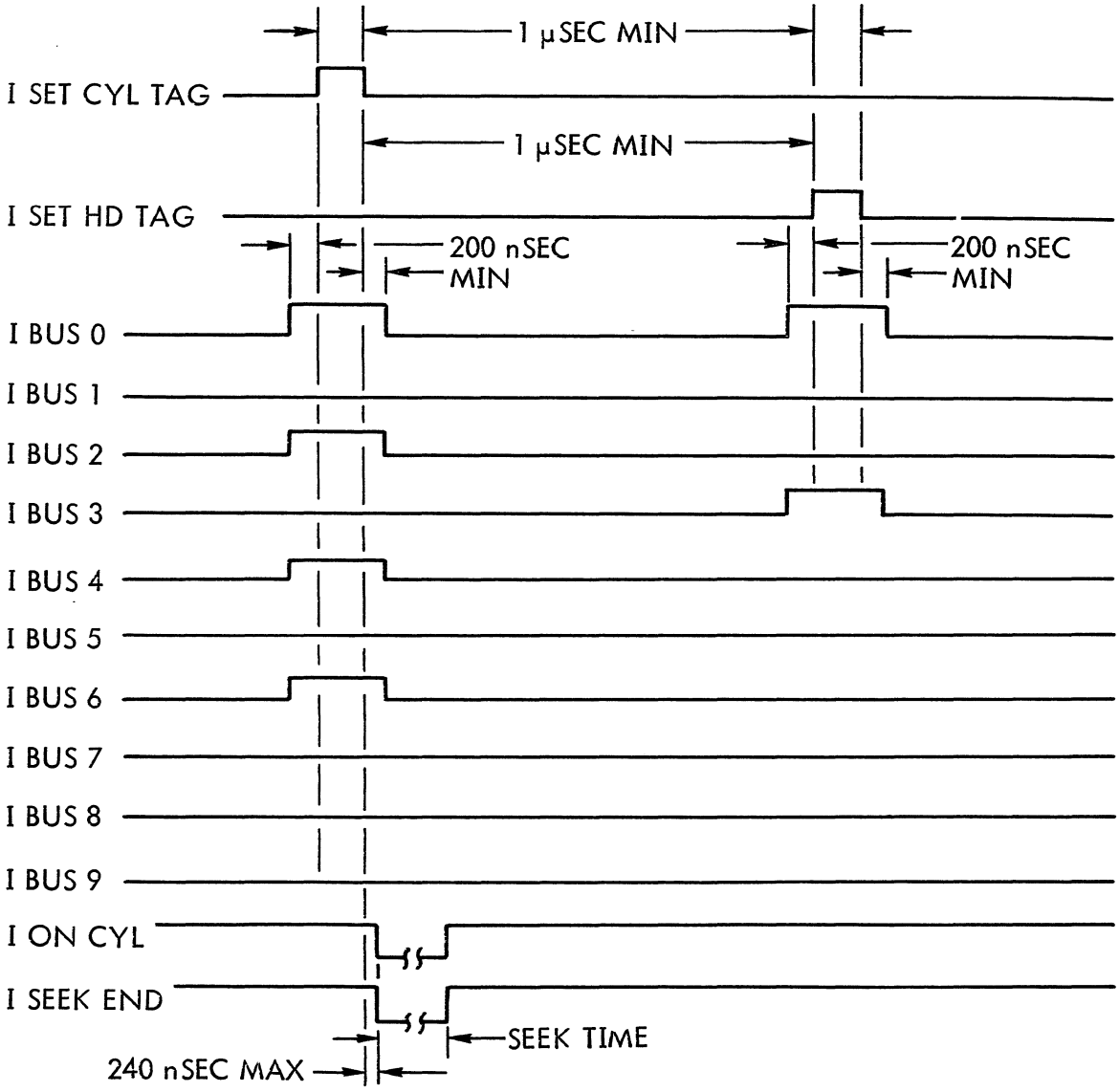


Figure 2-13. Set Cylinder and Set Head Timing Relationship

I CONTROL TAG -- When active, the bus lines are decoded as commands. The bus lines are decoded by this tag line as follows:

I BUS 0 = Write.

The WRT command enables the writing function for the time that I CONTROL TAG and I BUS 0 are active (see Figure 2-14).

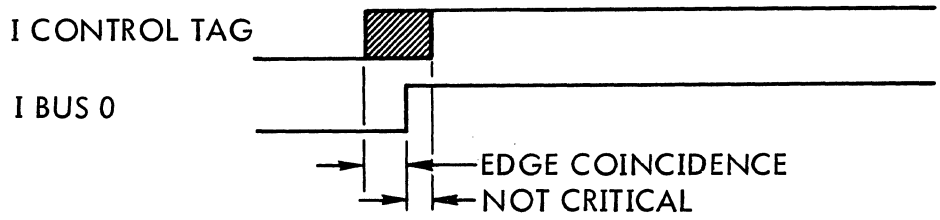


Figure 2-14. Write Command Timing

I BUS 1 = Read.

The READ command enables the read function for the time that I CONTROL TAG and I BUS 1 are each active (see Figure 2-15).

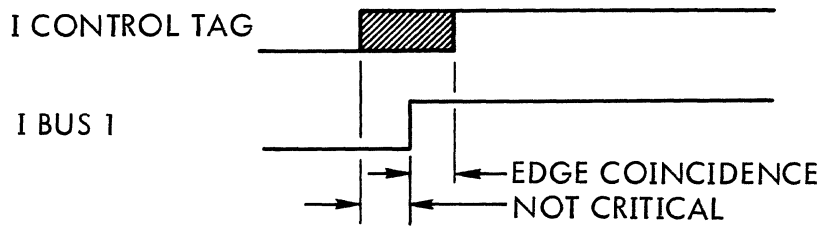


Figure 2-15. Read Command Timing

I BUS 2 = Offset forward
I BUS 3 = Offset reverse

The OFFSET FWD and OFFSET REV commands enable track offset for the duration of time that I CONTROL TAG and either I BUS 2 for forward offset or I BUS 3 for reverse offset are active. Forward is toward the spindle with respect to its normal track position. These signals are an aid in recovering marginal data and offset the track position ±200 microinches.

The time for the servo to move will not exceed 2.5 milliseconds for:

Normal track location to offset
Offset to normal track location
Offset forward to offset reverse
Offset reverse to offset forward

When either OFFSET FWD or OFFSET REV are issued, both I ON CYL and I SEEK END shall become inactive for 3.1 ±0.6 milliseconds. The I ON CYL and I SEEK END signals will become inactive within 245 nanoseconds of either the OFFSET FWD or OFFSET REV commands becoming active (see Figure 2-16 for timing).

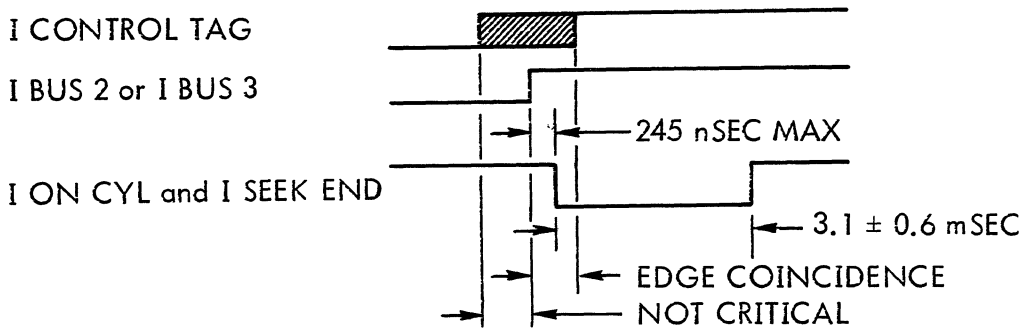


Figure 2-16. Offset Command Timing

I BUS 4 = Fault reset.

The R/FAULT command clears all fault conditions that do not have active inputs. If there are no existing faults, the I FAULT signal will become inactive. While CONTROL TAG must be active for at least 1 μsecond, BUS 4 only needs to be active for a minimum of 100 nanoseconds (see Figure 2-17).

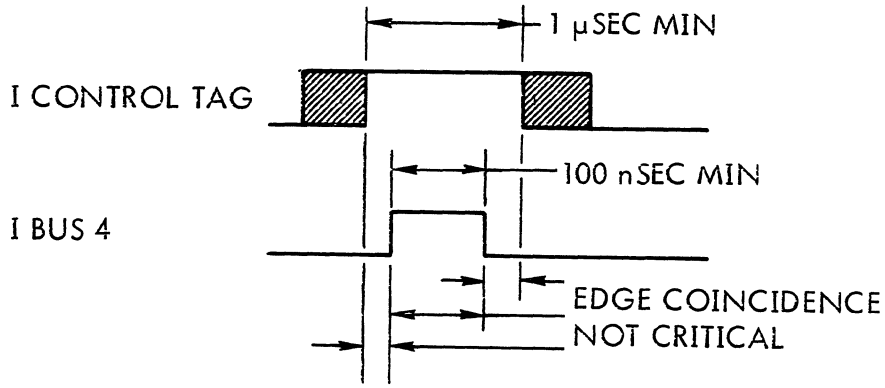


Figure 2-17. Reset Fault Command Timing

I BUS 6 = Restore

The RESTORE command causes the drive servo to seek to cylinder 000, resets the head address register to 00 and resets any seek error conditions. I BUS 6 shall be active at least 250 nanoseconds, but not more than 1 millisecond (see Figure 2-18).

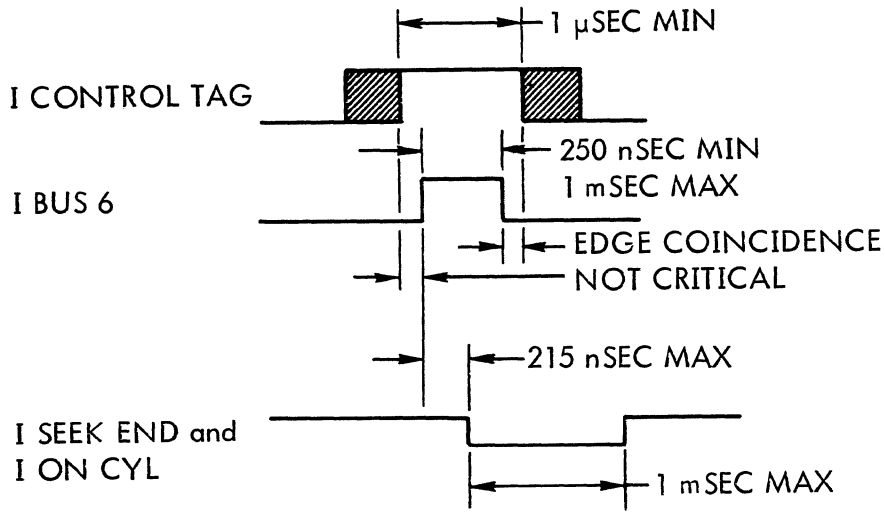


Figure 2-18. Restore Command Timing

The RESTORE seek time is less than 1 second.

I BUS 7 = Data Strobe Early

I BUS 8 = Data Strobe Late

The DSERLY and DSLATE commands enable the data strobe to shift in time from nominal. Early shifts the strobe 5 nanoseconds earlier than normal and late shifts the strobe 5 nanoseconds later than normal. These functions remain active for the duration of I CONTROL TAG and either I BUS 7 or I BUS 8 being active. The data strobe returns to nominal when neither of these functions are active. These signals are an aid in recovering marginal data that has become marginal due to peak shifting.

d. Status Lines

There are eight status signals; however, four of the status signals (FAULT, SEEK ERROR, ON CYL, and RDY) have alternate definitions, depending on the state of I CONFIGURATION.

I CONFIGURATION = Request Status Alternate Definitions

The I CONFIGURATION command enables the I SEEK ERROR and I FAULT signals to transmit the Reflex II Model configuration. It also enables the IRDY and IONCYCL signals to transmit the Reflex II fixed head configuration to the controller as determined by the indicated Reflex II switch settings on the logic/interface board. Table 2-4 presents the switch settings and definitions.

TABLE 2-4

I CONFIGURATION STATUS

Switch S1-6	Switch S1-7	Reflex Model	I SEEK ERROR	I FAULT
0	0	A	inactive	inactive
0	1	B	inactive	active
1	0	C	active	inactive
1	1	D	active	active

Switch S1-8	Number of Fixed Heads	I RDY	I ON CYL
1	0	inactive	inactive
0	60	active	inactive

Switch setting 1 = switch open (off)
Switch setting 0 = switch closed (on)

I CONFIGURATION is disabled when switch S1-5 is closed (on).

I FAULT -- This signal indicates that at least one of the following error conditions in the drive is active:

(1) Data head circuit unsafe monitor active due to any one or more of the following faults:

(a) Write command active and head coil open or shortened.

(b) Write command active and no head selected.

(c) Write command active and write current level not correct.

(d) Write command inactive and write current present.

(e) Write command active and write current transitions missing.

(f) Multiple heads selected.

(2) DC voltage unsafe.

(3) Illegal head selected.

(4) Write command active and read command active.

(5) Write command active and either offset forward or offset reverse commands active.

(6) Write command active and seek RDY not active.

(7) Write command active and write protect active.

The I FAULT signal is reset by issuing the R/FAULT command or by removing power and then reapplying power to initiate a sequence up routine.

The I FAULT signal transmits model number information when I CONFIGURATION is active (see I CONFIGURATION).

I SEEK ERROR -- This signal indicates that a seek error has occurred. A seek error is defined as one or more of the following:

(1) Motion command (Seek, Load, Restore) not completed within a 1 1/2 second time period.

(2) Illegal cylinder address commanded.

(3) I SET CYL TAG active and seek not done or drive not ready.

The I SEEK ERROR signal is reset by issuing a RESTORE command. The I SEEK ERROR signal becomes active within 800 nanoseconds of the I SET CYL TAG becoming active when an illegal cylinder address is commanded. The I SEEK ERROR signal transmits model number information when I CONFIGURATION is active (see I CONFIGURATION).

I ON CYL -- This signal indicates that the heads are positioned over a track.

The signal becomes inactive within 240 nanoseconds of the trailing edge of the I SET CYL TAG signal. It remains inactive for the duration of a motion seek and for a nonmotion seek, it remains inactive for 3.1 $\pm$ 0.6 milliseconds.

I ON CYL becomes inactive within 245 nanoseconds of the trailing edge of the I SET CYL TAG signal when an offset command is issued. It remains inactive for 3.1 $\pm$ 0.6 milliseconds. I ON CYL transmits the fixed head configuration when I CONFIGURATION is active (see I CONFIGURATION).

I RDY -- This signal indicates that when active the heads are loaded on a legal cylinder, and there is no detected drive fault.

I RDY transmits the fixed head configuration when I CONFIGURATION is active (see I CONFIGURATION).

I INDEX -- This signal is a pulse 3.0 $\pm$ 0.6 μseconds wide. Its leading edge is used to indicate the start of a track and the start of Sector 00. The INDEX signal characteristics are maintained during seek operations.

I SECTOR -- This signal is a pulse 840 ± 60 nanoseconds wide. Its leading edge is used to indicate the start of a sector. Sector marks are derived from the phase lock oscillator which produces one count for each data byte. The signal characteristics are maintained during seek operations. The number of sectors per track is selectable by switches on the drive's logic/interface board.

I WR PROTD -- This signal is commanded by the write inhibit switch on the optional operator indicator panel. The signal is permitted to change state only when I CONTROL TAG is inactive. The signal is active when the drive write inhibit switch is active.

Data Cable Descriptions

The data cable consists of 9 signals. Each signal is made up of two wires. The data cable signal lines are unique to each drive (see Figure 2-7).

1. Data Cable Pin Assignments

The data cable signal listing and pin assignments are shown in Figure 2-19. The arrow indicates the transmitted direction. The pin number assignments are shown for the signal pair with the "/" used to describe polarity convention. The prefix "I" is used to indicate that the signal is at the interface.

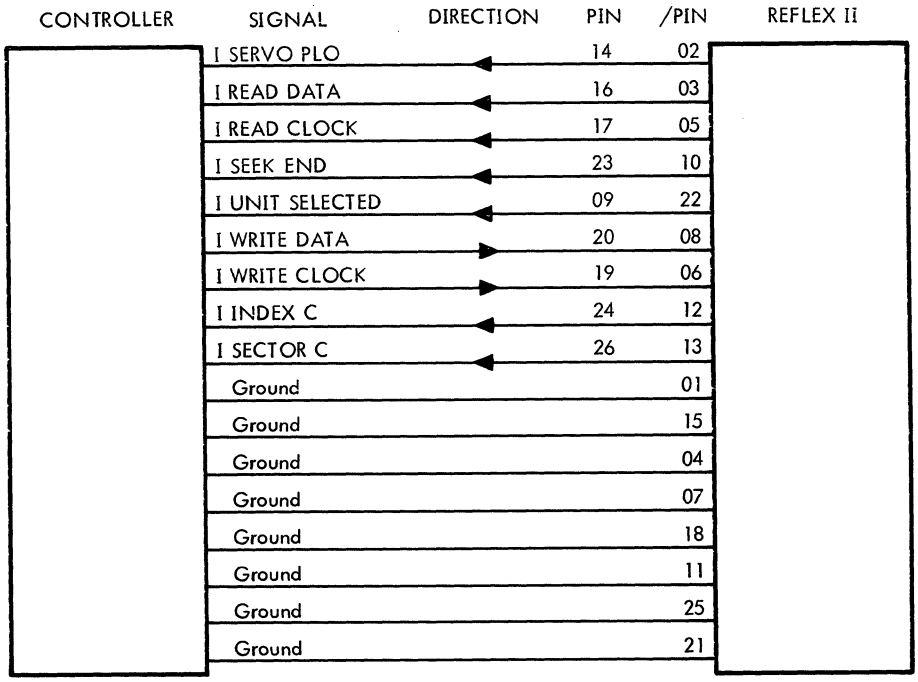


Figure 2-19. Data Cable Pin Assignments

2. Data Cable Signal Definitions

The data cable signals break down into two groups of signals, status and read/write.

a. Status

I UNIT SELECTED -- This signal becomes active within 400 nanoseconds of the I UNIT SELECT signal, if I OPNCBLDET is inactive. The signal indicates that the drive is selected. It becomes inactive when I OPNCBLDET is active or within 200 nanoseconds of I UNIT SELECT becoming inactive (see Figure 2-10).

I SEEK END -- This signal is active when a seek operation has terminated. Termination may be from either seek done or seek error.

I INDEX C and I SECTOR C -- These signals have the same definitions as index and sector in the signal cable. The difference is that these signals are transmitted without the drive being selected as long as I OPNCBLDET is inactive.

b. Read/Write

The I SERVO PLO, I READ DATA, I READ CLOCK, I WRITE DATA and I WRITE CLOCK signal relationships are illustrated in Figure 2-20.

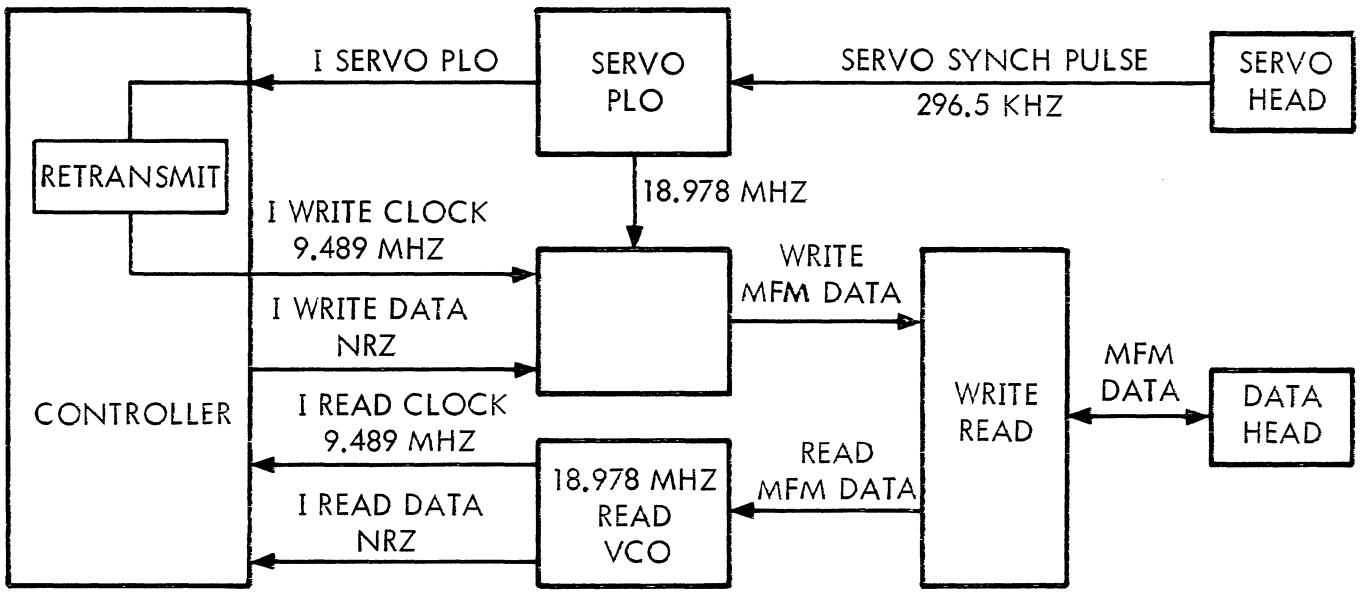


Figure 2-20. Read/Write Signal Relationships

I SERVO PLO -- This signal is the output of the servo phase locked oscillator (PLO), which is referenced to the servo surface. It is continuously transmitted. The I SERVO PLO frequency varies with the disc speed. It is 9.489 MHZ $^{+3}_{-7}$%.

I WRITE CLOCK -- This signal is the retransmitted I SERVO PLO signal. It is used to synchronize the I WRITE DATA signal. The I WRITE CLOCK signal must be transmitted at least 250 nanoseconds prior to enabling the WRT command.

I WRITE DATA -- This signal is the data that is to be recorded. It is presented in NRZ form.

I READ CLOCK -- This signal defines the data cell beginning; it is used to synchronize the I READ DATA. I READ CLOCK is continuously transmitted and will become phase synchronized with the I READ DATA SIGNAL within 10 μseconds after the READ command has been issued.

I READ DATA -- This signal is the data read by the drive. It is presented in NRZ form.

Transmitters, Receivers, and Terminators

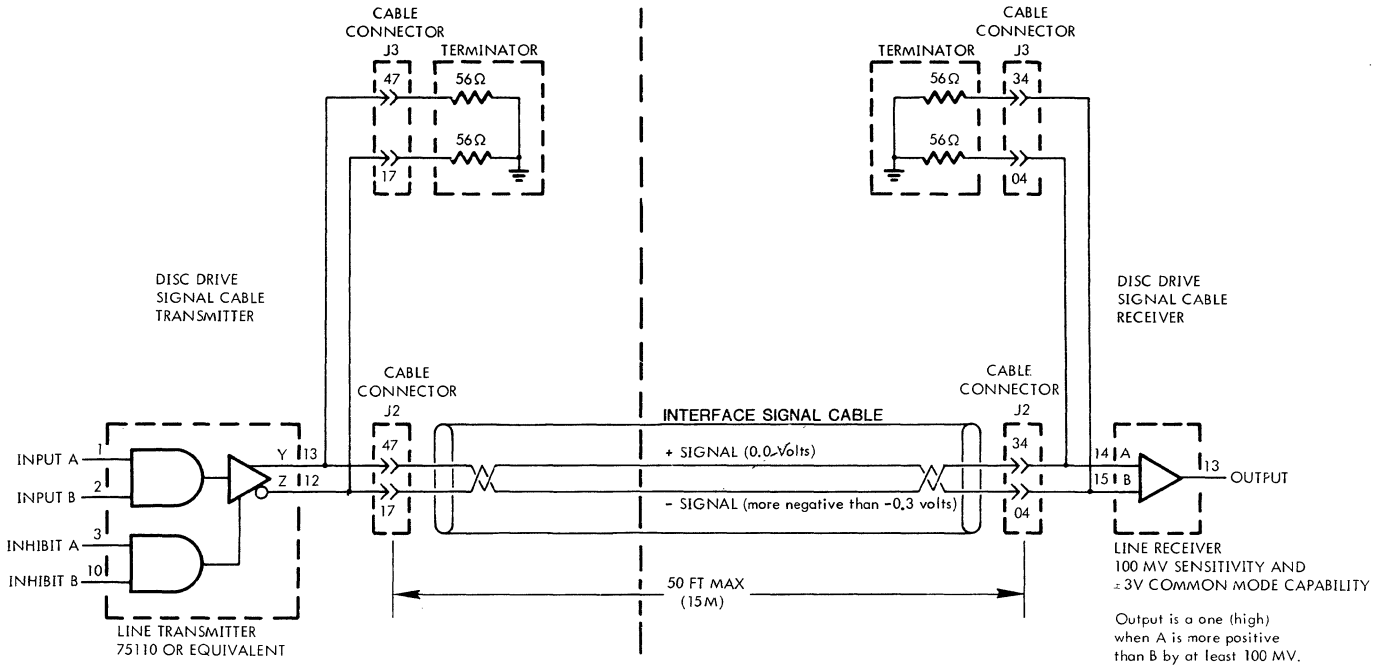
1. Transmitters and Receivers

All input and output signals are digital and are received and transmitted differentially through the data and signal cables. Industry standard 75110 transmitters are to be used. Differential receivers with at least 100MV sensitivity and ± 3V common mode capability are to be used. The I OPNCBLDET receiver has at least 25MV sensitivity. There is also a special requirement for the controller when a daisy chain configuration is used. The controller must have at least one driver (transmitter) for each four drives connected to the I OPNCBLDET signal. A typical signal cable transmission line is shown in Figure 2-21. Figure 2-22 presents a typical data cable transmission line while Figure 2-23 shows the special termination for the I OPNCBLDET line. Logic states are referred to as 1 or 0, don't care as X, and + (plus) as the signal voltage more positive then - (minus) as measured differentially.

2. Terminators

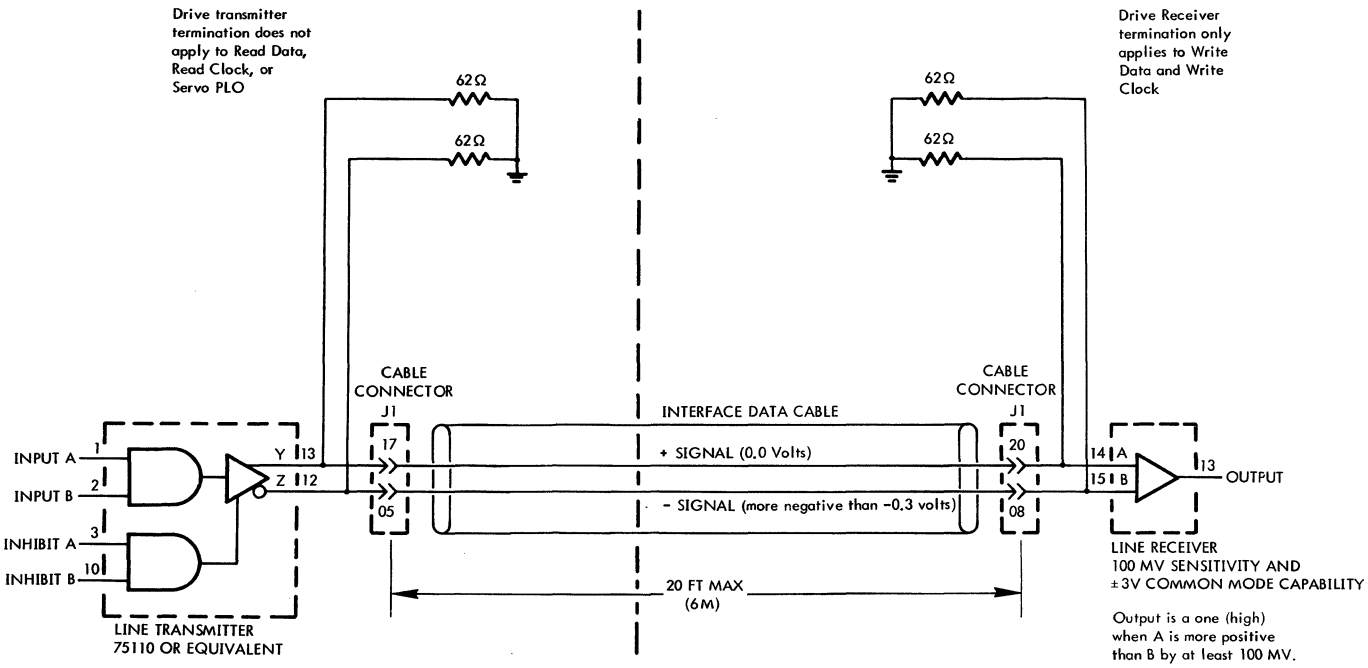
The signal cable termination consists of a 56 ohm resistor connected from each signal line to ground, (see Figure 2-21). All signal cable lines are terminated in the drive regardless of whether they are received or transmitted.

The data cable termination consists of a 62 ohm resistor connected from each signal line to ground (see Figure 2-22). The signals I SERVO PLO, I READ DATA, and I READ CLOCK are not terminated in the drive. All lines not terminated by the terminator assembly are terminated at their respective circuit board. All signals (received or transmitted) terminated in the drive should not be terminated in the controller.



INPUT	INHIBIT	OUTPUT	
A-B	A-B	Y	Z
X	0	+	+
0	1	-	+
1	1	+	-

Figure 2-21. Typical Signal Cable Transmission Line



INPUT A-B	INHIBIT A-B	OUTPUT Y	OUTPUT Z
X	0	+	+
0	1	-	+
1	1	+	-

Figure 2-22. Typical Data Cable (Read/Write) Transmission Line

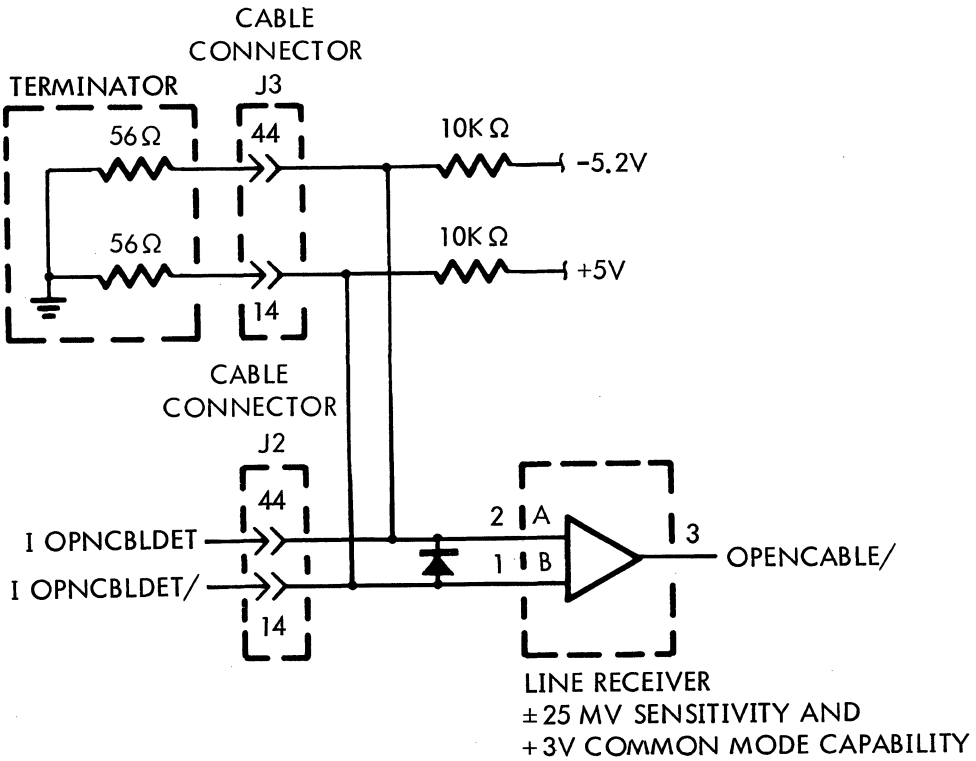


Figure 2-23. I OPNCBLDET Termination

Data Format

The format is determined by the controller; however, the format must conform to the drive timing and tolerance considerations noted below under Format Considerations.

1. Format Considerations

a. Head Select

The head requires 5.0 μseconds to stablize after it is selected before valid read or write data is assured.

b. Write Amplifier

The write amplifier requires 0.8 μseconds after the WRT command is enabled prior to valid written data being assured.

c. Read to Write

Prior to enabling the WRT command, there is a 0.3 μsecond delay required after disabling the READ command. This will ensure that there is no overlap due to signal propagation time. This time is absorbed in the time considerations for write amplifier stabilization.

d. Read Amplifier

The read amplifier requires 10 μseconds to stabilize prior to valid read data being assured for each of the following conditions:

After selecting a head
After writing with a selected head
Selecting another head after terminating a write function

e. Read VCO

The read VCO requires 10 μseconds to acquire synchronization to data. The synchronization field will consist of a string of 0's. The read VCO is commanded to begin acquiring synchronization at the leading edge of the READ command.

f. Splice

A splice is created at the start and end of every write function. There may be a splice located at the beginning and end of every header and record. It must be assumed that the data has not been properly written at the splice; therefore, at this location the READ command should not be enabled.

The location of the splice will vary with the method of enabling head select and write command. Assuming that the timing considerations of the disc drive are being honored and that the method of writing is per the recommended method noted elsewhere in this section, (head select $\geq$ 5 μseconds prior to write command) the location of the splice will be as follows (see Figure 2-24):

(1) In front of a header, splice will be in pre-amble byte.

(2) Header update only, splice will be in pre-amble byte for beginning of header and in the byte after the post-amble byte of the header.

(3) Record update only, splice will be in post-amble byte of header for beginning of record and in pre-amble byte of the next sector or index.

However, if the method of writing is to enable head select and the write command at the same time, the splice will move into the head select stability bytes.

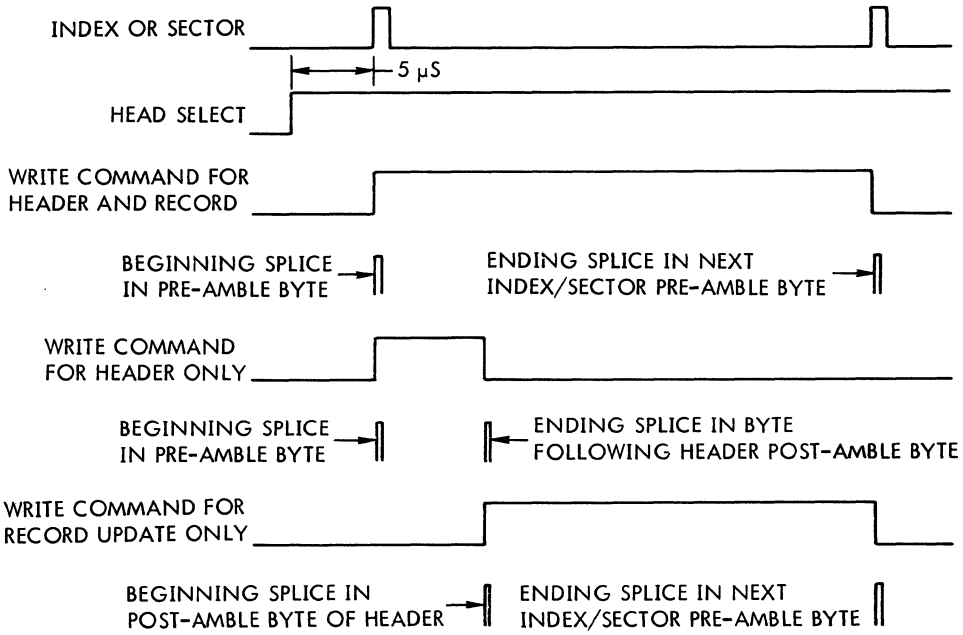


Figure 2-24. Splice Location

g. Preamble

A one-byte string of 0's is required at the start of each header to act as a pad. If the head stabilization time has been accounted for, this byte may be used for the write amplifier stabilization time.

h. Postamble

A one byte string of 0's is to be written at the end of each header and each record to act as a pad. This is to ensure that the last bit(s) of the checkword is not destroyed or distorted.

i. Synch Pattern

A synch pattern is written after the head VCO synchronization field to indicate the start of a header address or the start of record data. It usually is written as a byte of 1's.

j. Method

Consecutive or interlaced sector format may be utilized. The overhead for head select and read amplifier stabilization times will depend upon how head select, write command, and read command are utilized.

2. Write Initialization

The recommended initialization format is listed below. Byte counting is recommended for timing to eliminate disc speed tolerances (1 byte $\triangleq$ 843 nanoseconds).

(1) Command the appropriate unit cylinder, head and sector addresses.

(2) Enable head select at least 6 bytes prior to enabling the write command to allow for head select stabilization.

(3) Detect the appropriate I IDX or I SECTOR pulse and enable the WRT command.

(4) Write the pre-amble (1 byte of 0's). This time will include the allowance for the write amplifier stabilization.

(5) If the reading method requires an allowance for head select stablization, write 6 bytes of 0's.

(6) If the reading method requires an allowance for read amplifier stabilization, write 12 bytes of 0's.

(7) Write 12 bytes of 0's to allow for the read VCO synchronization time.

(8) Write the synch pattern for the header address (1 byte of 1's).

(9) Write the header address.

(10) Write a checkwork, either a cyclic redundancy character (CRC) or error correction code (ECC).

(11) Write the post-amble (1 byte of 0's).

(12) If a record field is to be written, proceed to (13) through (17). Otherwise, skip to (18).

(13) Write 12 bytes of 0's for read VCO synchronization time.

(14) Write a synch pattern for the record data (1 byte of 1's).

(15) Write the data field. For initialization purposes, a string of 1's is sufficient or a particular pattern may be written for diagnostic testing. Recommended test patterns are:

Repeated 155555

Repeated 125252

Repeated 6DB

(16) Write the error correction characters.

(17) Write the post-amble (1 byte of 0's).

(18) To avoid erased areas in the gap between the ending post-amble and the next sector pre-amble, it is best to continue writing the string of 0's from the post-amble until the next I IDX or I SECTOR pulse is detected. At this time the 0's are continued as necessary to initialize that sector's header.

(19) Remove the WRT command 100 nanoseconds minimum prior to removing the head select command.

3. Write Record Data

To be consistent with prior written data and to avoid the effects of disc speed tolerances, write timing should be accomplished by counting bytes. When writing the record, it is assumed that the head has been selected to read and locate the correct header, and that the head remains selected to write the record. The following steps outline the procedures for writing the record:

(1) Locate and identify the appropriate sector.

(2) After completing the read header function (end of post-amble), disable the READ command.

(3) Provide the read to write gap delay of 0.3 μseconds and then enable the WRT command.

(4) Write 12 bytes of 0's for read VCO synchronization time.

(5) Write the synch pattern (1 byte of 1's).

(6) Write the record data.

(7) Write the checkword ECC.

(8) Write the post-amble (1 byte of 0's).

(9) To avoid erased areas in the gap between the ending post-amble and the next sector's pre-amble, it is best to continue writing the string of 0's from the post-amble until the next I IDX or I SECTOR pulse is detected. At this time the 0's may be continued as necessary to initialize that sector's header.

(10) Remove the WRT command 100 nanoseconds (minimum) prior to removing the head select command.

4. Read

Reading is enabled by the READ command; the read command must not be enabled over splice areas. For splice areas, disable the read command and then enable it. As the read command is enabled, it causes the READ VCO to acquire synchronization. The synchronization field must be a string of 0's.

Read timing should be accomplished by counting bytes to be consistent with the written data and to avoid disc speed tolerance effects. The following steps outline the procedures required to accomplish read timing:

(1) Identify the correct I IDX or I SECTOR pulse.

(2) Activate the appropriate head select and the read command.

(3) Head select and read command must be utilized consistently with the written format. Considerations include the head select and read amplifier stabilization times, and the READ VCO synchronization time.

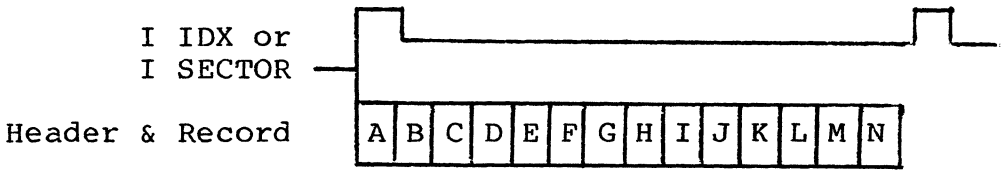
(4) Depending on the format used, the head select stabilization time may be included in the read amplifier stabilization time.

(5) The leading edge of the read command causes the read VCO to acquire synchronization. This must occur within a string of recorded 0's in the time alloted for VCO synchronization.

(6) The synch pattern search may begin 11 bytes after read becomes active, since at this time the read VCO will have acquired synchronization and the I READ DATA will be valid.

5. Format Summary

The formatted disc summary is shown in Figure 2-25.



		Minimum Length
Header	A = Pre-Amble	1 byte (0's)
	B = Head Select Stability	6 bytes (0's)
	C = Read Amplifier Stability	12 bytes (0's)
	D = Read VCO Synchronization	12 bytes (0's)
	E = Synch Pattern	1 byte (1's)
	F = Header Address	Variable
	G = Checkword	Variable
	H = Post-Amble	1 byte (0's)
Record	I = Read VCO Synchronization	12 bytes (0's)
	J = Synch Pattern	1 byte (1's)
	K = Record Data Field	Variable
	L = Error Correction Characters	Variable
	M = Post-Amble	1 byte (0's)
	N = End of Record Gap	Variable (0's)

Figure 2-25. Format Summary

The B and C fields are optional depending on utilization of head select, write command, and read command.

The F, G, K, and L lengths are set by the user. The N length is dependent upon the sector length chosen versus the sum of the header and record lengths. The minimum overhead is 29 bytes plus checkword and/or error correction code(ECC).

DATA SECURITY

Data is written by the drive in direct response to the interface commands presented by the controller. The drive will inhibit writing in the case of a fault condition (see fault definition under signal descriptions in this section).

In addition to inhibiting writing, the drive will retract the heads if one or more of the following conditions occur:

(1) DC voltage unsafe; this term also monitors AC power when the optional internal power supply is present.

(2) Carriage lock unsafe.

(3) Interface signal cable open (I OPNCBLDET is active).

(4) Motion command (seek, restore, head load) not completed within 1.5 seconds.

(5) Loss of spindle motor drive due to one or more of the following:

DC voltage unsafe
Spin brake unsafe
Disc speed unsafe

SECTION 3

INSTALLATION AND OPERATION

INTRODUCTION

This section provides installation and operation information for the Reflex II disc drive. Operation information includes optional operator's indicator panel and all switches that are internal in the drive (i.e., unit selection, sector selection, etc.).

INSTALLATION CHECK LIST

The installation check list (Table 3-1) is designed for trained service personnel to use as a guide in performing installation checks. If more detailed information is desired, refer to the appropriate paragraphs in this section.

TABLE 3-1

INSTALLATION CHECK LIST

Remove all packing material.

Check for:

- ☐ Shipping damage
- ☐ Electrical short circuits
- ☐ Loose or shorted connections
- ☐ Signs of possible trouble areas; listen for any audible indication.
- ☐ Resistance between ground and each DC voltage to ensure no electrical shorts.

Examine:

- ☐ Disc drive interior and exterior; clean as required.
- ☐ Major components and assemblies for tightness.
- ☐ All latches, covers, and hinges for proper operation.
- ☐ Spindle drive belt and tension spring.

Table 3-1. Installation Check List (Cont'd)

- ☐ All cables and receptacles for bent, loose, or recessed pins.
- ☐ All cables for proper length.
- ☐ Power rating on ID plate for volts and frequency to ensure compliance with site power.
- ☐ All DC voltages (+5, -5.2, -4, +6, +6RW, ±6.2, ±9, ±12, ±18).
- ☐ Servo alignment
- ☐ Servo operation
- ☐ Read/write alignment
- ☐ Read/write operation

Test:

- ☐ Power to the disc drive; cooling fans should operate.
- ☐ Sequence up operation.
- ☐ Spindle brush resistance for less than one ohm to ground.
- ☐ Brake time.

Select:

- ☐ Unit address
- ☐ Number of sectors
- ☐ Desired position of remaining switches on logic/interface PCB.

Run diagnostic routines.

Verify that customer jobs are properly executed.

UNPACKING

The recommended installation procedures listed in this section presume that the drive is correctly wired and configured for the site power source. However, after unpacking the drive, steps should be taken to ascertain the power configuration.

Detailed information for power verification is provided under separate headings in this section.

To unpack the drive, proceed as follows:

(1) Inspect the shipping container for evidence of damage. Contact the carrier and Microdata if damage is evident.

(2) Remove the contents from the shipping containers(s). Check the items removed against the shipping invoice to verify the contents. Contact Microdata in the event of a shortage.

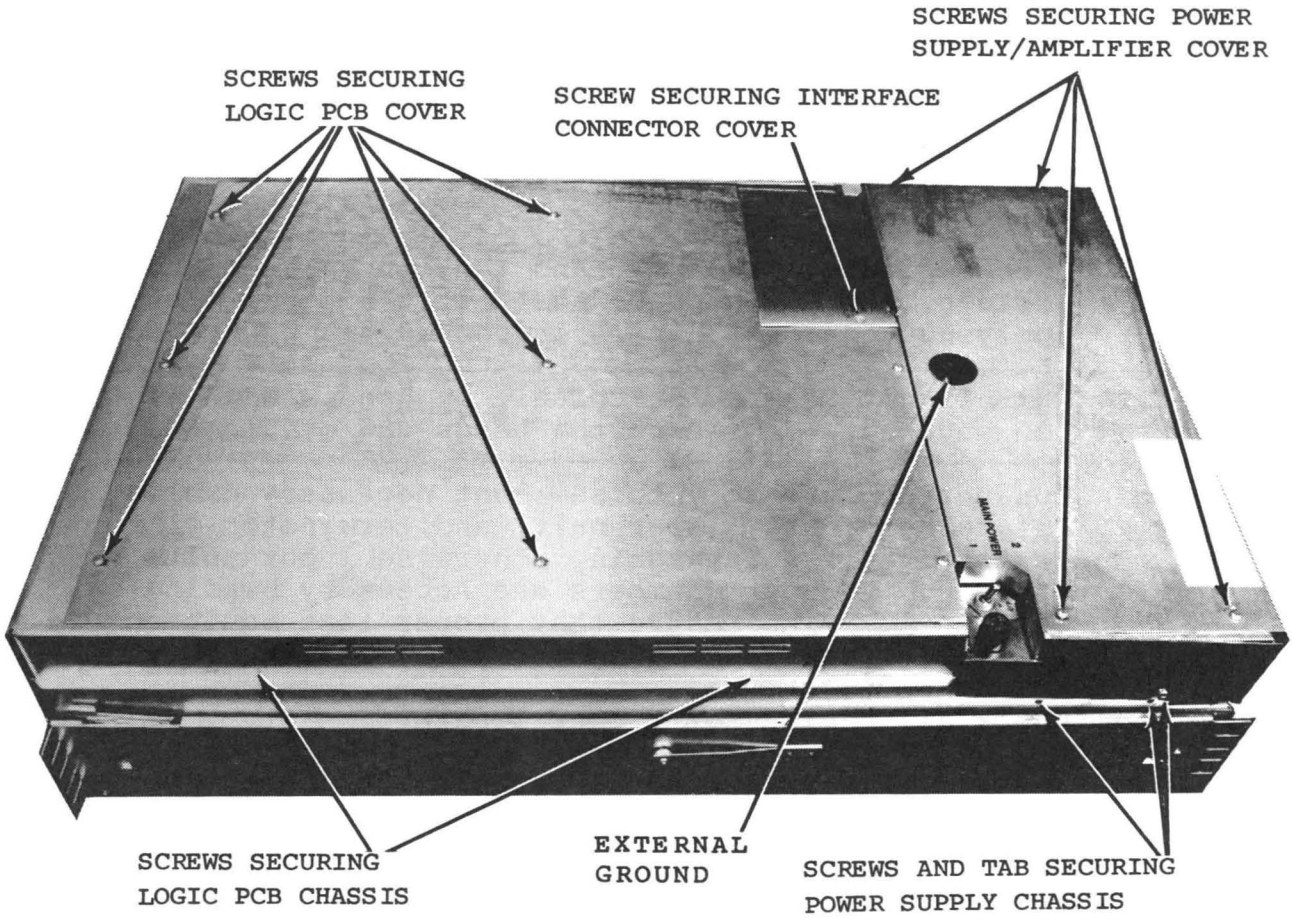


Figure 3-1. Cover Removal

(3) Verify that the serial number of each unit corresponds to the serial numbers shown on the shipping records. The serial number is found on the indentification nameplate.

(4) Visually inspect the exterior of the disc drive for evidence of damage that may have occurred in transit. If damage is found, notify appropriate personnel.

(5) Remove the covers from the Reflex II drive (see Figure 3-1).

(6) Remove the screws securing the PCB chassis and the power supply/amplifier chassis (see Figure 3-1).

PHYSICAL INSPECTION

(1) Check for loose or shorted connections.

(2) Check the major components and assemblies to determine if any assemblies or hardware have loosened. Correct as required.

(3) Check all latches, covers, and hinges for proper operation.

(4) Check spindle drive belt and tension spring; make certain belt is in place and that the tension spring is applying tension (this is inspected via bottom access).

CAUTION: Do not rotate the spindle by hand. Hand rotation may cause damage to the heads and/or disc(s).

(5) Conduct an inventory to see that necessary cables (signal and data, 1 per unit) and terminator (1 for last drive if daisy-chain, otherwise 1 per unit) are present. For part numbers see Accessory heading in Section 6. Also ensure that proper test equipment is available (see Test Equipment paragraph in Section 5).

(6) Check all cables for proper length.

(7) Inspect all cables and receptacles for bent, loose, or recessed pins.

(8) Check the power rating on the identification nameplate for line voltage and frequency requirements. The nameplate is located on the upper left rear portion of the drive. If the drive does not have the optional transformer assembly installed, DO NOT PROCEED WITH INSTALLATION IF POWER RATING DOES NOT MATCH AVAILABLE POWER SOURCE. If there is a problem, proceed to Power Verification/Configuration paragraphs in this section.

(9) Check to ensure that the power ON/OFF switch on the Reflex II drive is in the OFF position.

(10) If the disc drive does <u>not</u> contain an internal power supply, proceed to the next heading; otherwise, skip to Grounding Cable Connections in this section.

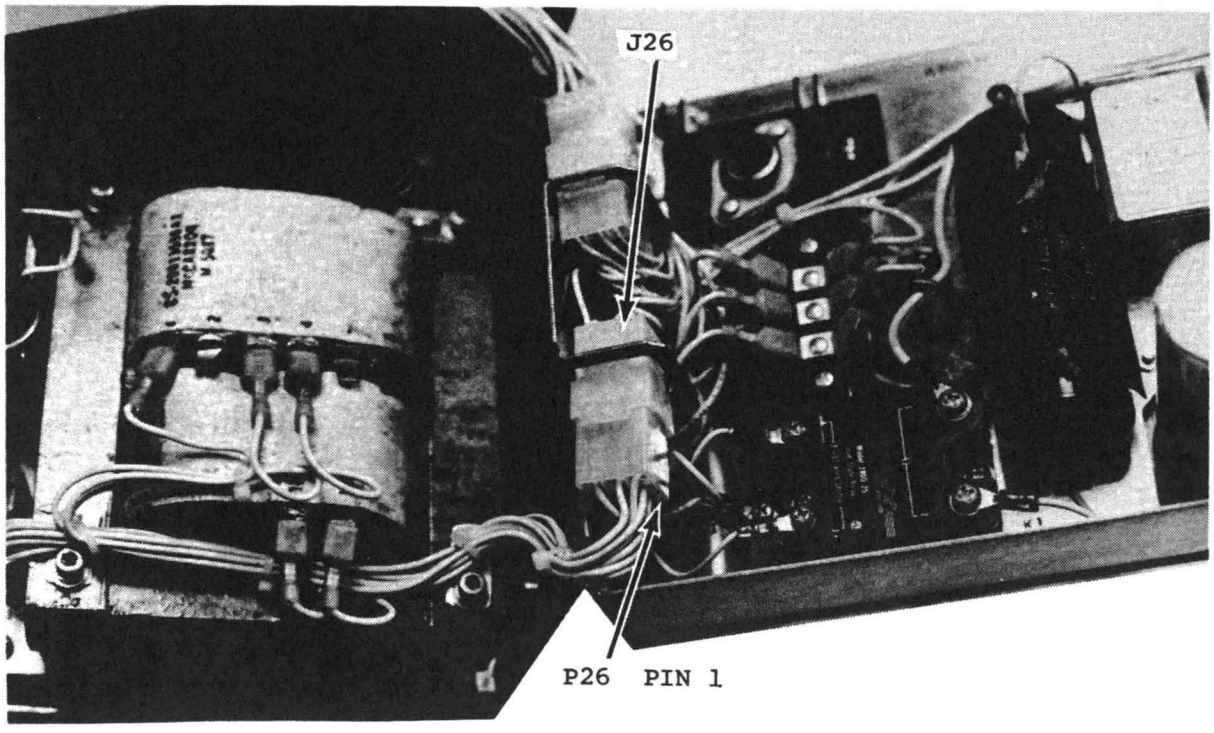


Figure 3-2. DC Voltage Connector

Reflex II Units Without Internal Power Supply

These units must receive DC power from an external source. External DC rectified power may be supplied to Reflex II via the power connector (J26) shown in Figure 3-2. See Section 2 for DC voltage requirements. Connect external DC voltage source to J26. The connection must satisfy what is shown in Figure 3-3.

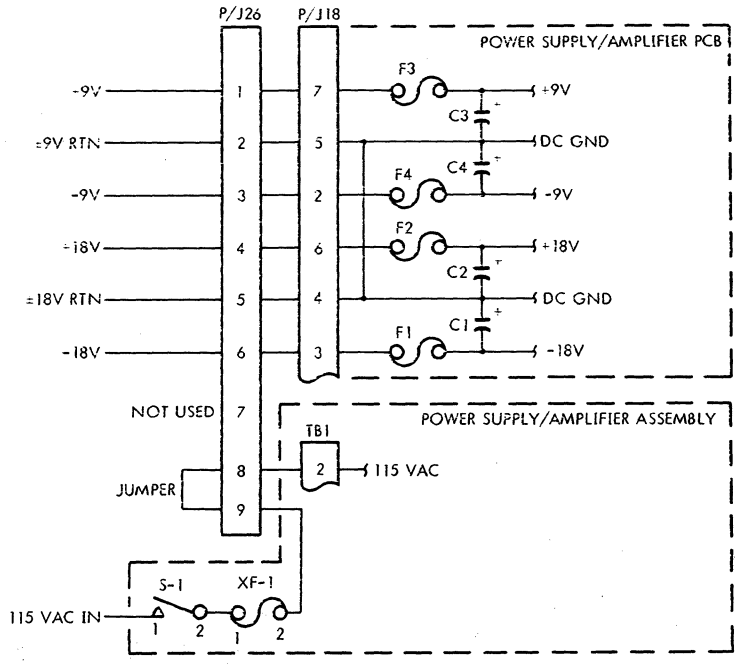


Figure 3-3. DC Voltage Connection

Grounding

The REFLEX II uses a single point ground system. One single point connects frame ground (AC ground) and signal ground (DC ground) together. The two grounds must be tied together, either locally (in drive) or remotely (in controller, or CPU, etc.). Do not apply power to the drive without the grounds being tied together.

The disc drive is delivered with the two grounds tied together on the power supply/amplifier PCB. This is done with a strap between terminals E2 and E4. (See Figure 3-4.)

(1) Determine the user system design for ground isolation.

(2) If the system design calls for single point grounds to be made at a point other than in the individual units, proceed with the succeeding steps; otherwise, skip to the next heading.

(3) Connect the braided wire ground strap between E1 of the power supply/amplifier PCB, and the common tie point called out by the system design (usually a point in the controller or CPU). This provides the frame (AC) ground. Signal (DC) ground is provided through the signal cable.

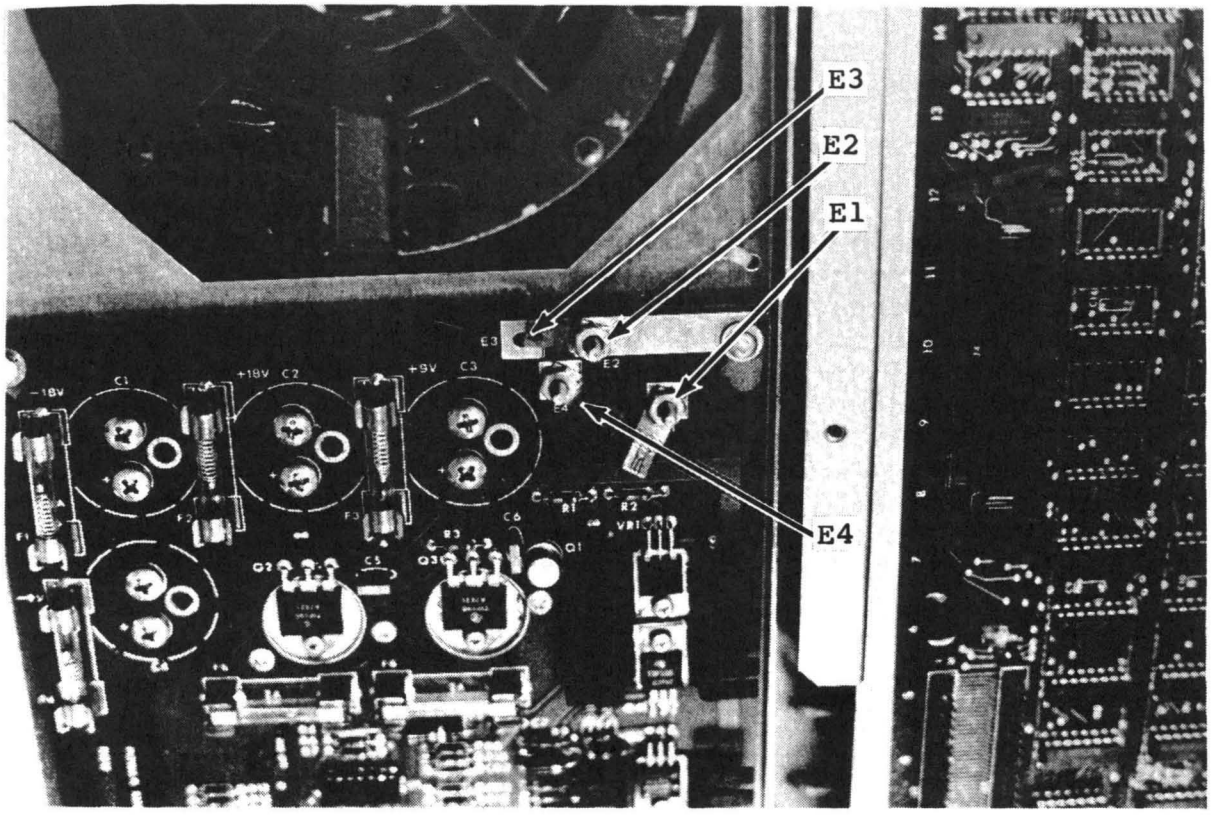


Figure 3-4. Ground Connection

AC Power Cable

The 115 VAC, 60 Hz disc drive is delivered with a power cord and plug. Other voltage and frequency combinations are delivered with a power cord, but no plug.

(1) If applicable, install plug on end of power cord. The convention to be followed is shown in Figure 3-5.

(2) Plug the AC cable into the power outlet.

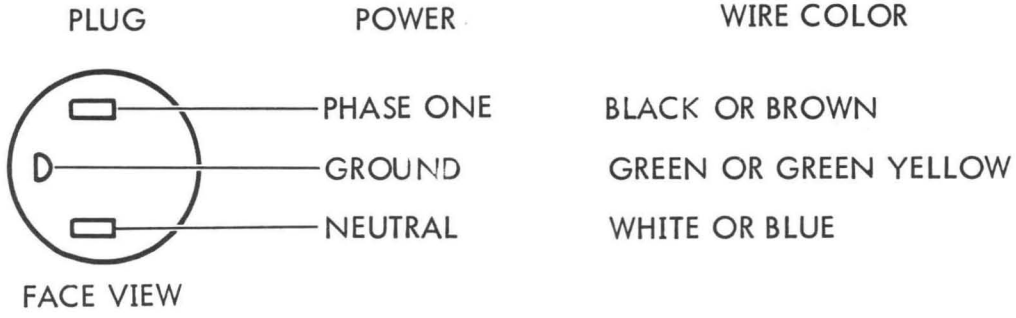


Figure 3-5. AC Power Cable Convention

Signal, Data, and Exerciser Cables

The logic/interface PCB houses the jacks for the signal, data, and exerciser cables. The signal cable may be cabled in a daisy-chain or star (radial) configuration as determined by the controller (see Cable Configuration in Section 2). The signal and data cables provide the system interface, while the exerciser provides a local connection for maintenance or diagnostic purposes. The exerciser can be cabled into the drive concurrent with the signal and data cables for all but read/write functions. The data cable must be removed for the exerciser to perform read/write functions. Table 3-2 presents the connector assignments and Figure 3-6 presents the cable connections. The maximum length for the data cable is 20 feet. The maximum length for signal cable is 50 feet from the controller to the terminator.

TABLE 3-2

CABLE CONNECTOR ASSIGNMENTS

Logic/Interface Connector Number	Function
J1 (26 pin)	Data cable--either to controller (system operation) or exerciser (local operation).
J2 (60 pin)	Signal cable--either to controller (1st drive or star configuration) or to previous drive (daisy-chain).
J3 (60 pin)	Terminator (last drive for daisy-chain or every drive for star configuration) Signal cable (to next drive if daisy-chain).
J4 (60 pin)	Exerciser (control/monitor cable).

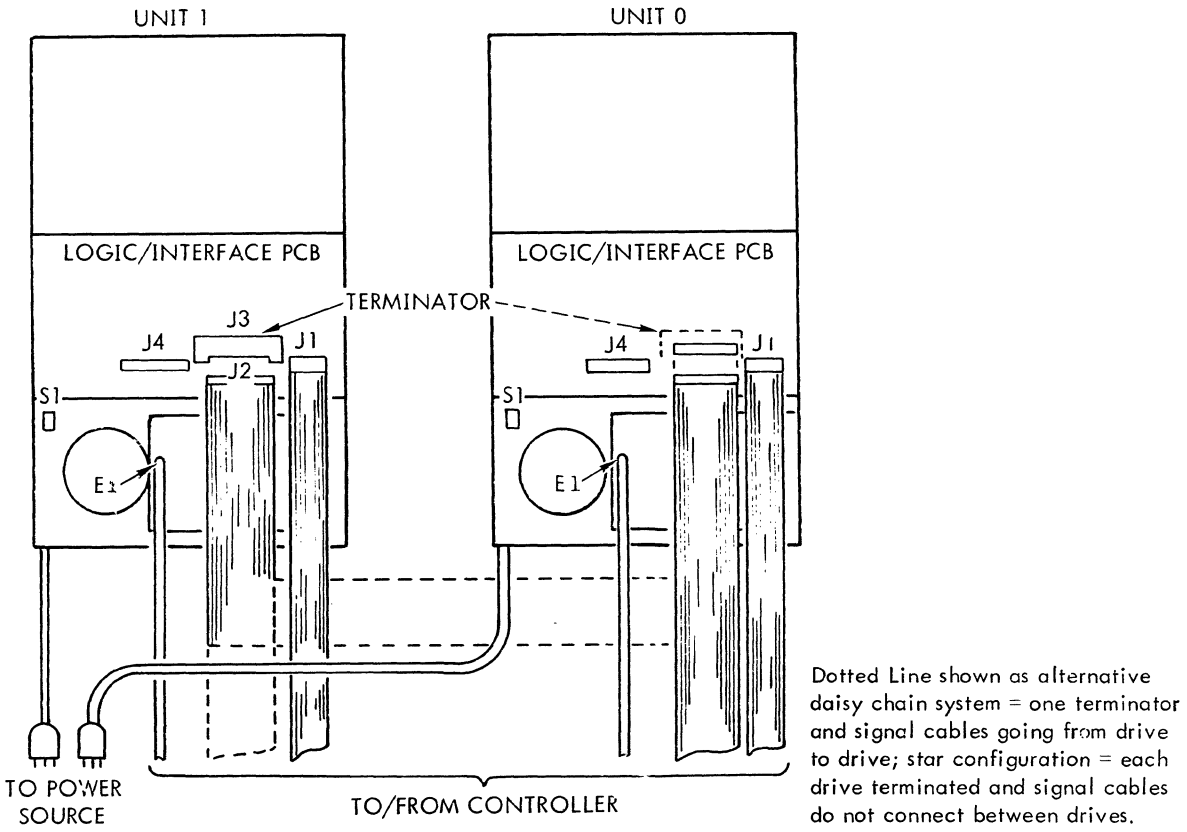


Figure 3-6. Cable Connections

(1) Connect the signal cable to J2 on the logic/interface PCB. This provides the signal (DC) ground connection to the disc drive.

(2) Install the terminator in J3 on the logic/interface PCB. This is applicable if this is the only drive, a star configuration, or the last drive in a daisy-chain string. Connect the ground lug on the terminator connector to E1 and E2, next to J3. Otherwise, install the signal cable that goes to the next drive into J3.

(3) The data cable connects into J1 on the logic/interface PCB, but will not be installed until after the initial checkout procedure.

INITIAL CHECKOUT PROCEDURE

(1) Connect the Reflex MOD III exerciser cable (60-pin cable) to the Reflex II drive at J4 on the logic/interface board.

(2) Plug the drive's AC cable into the power outlet.

(3) Set the exerciser control switch to SK-R (seek random position).

(4) Set the Reflex II switch in its "up" position.

(5) Set the SK ERR INHIBIT switch in its "down" position.

(6) Set the exerciser monitor switch to "B" position.

(7) Set the ACT and RESTORE switches to their OFF (center) positions.

(8) Set drive ON/OFF switch to ON position.

(9) A power-up sequence is now underway; the indicators on the exerciser should record the following events as they occur:

- ST0 indicator will light; all other indicators will be off.
- Within 5 seconds, DCSAFE, BRKSF and SMTR will become active (indicators will light). Also an audible click will be heard (brake solenoid releases).
- Spindle drive motor will start.
- Speed light will illuminate and another audible click (carriage lock releases) will be heard.
- HDLD indicator will light, heads will be permitted to load. (This is driven by carriage lock released signal.)
- Disc(s) will attain full operating speed and a first seek will occur.

(10) Verify all DC voltages (reference Maintenance Section).

This completes the power-up sequence. If a malfunction occurs, refer to the Maintenance Section; otherwise proceed to the next step.

(11) Verify servo alignment ([velocity, offset, damper, speed monitor, pulse gate and separated pulse] reference Maintenance Section).

(12) Using the exerciser, initiate several restores, then execute random seeks for several minutes.

(13) Connect the 26-pin exerciser cable to the drive at J1 of the logic/interface board.

(14) Verify read/write alignment ([pulse width, phase detector offset] reference Maintenance Section).

(15) Using the exerciser, execute read and write functions on each head. Monitor the exerciser display indicators for fault conditions; if a fault occurs, refer to the Maintenance Section.

(16) Turn off the AC power.

(17) Disconnect the exerciser cables from J1 and J4 of the logic/interface PCB.

SYSTEM INSTALLATION

When the disc drive has been satisfactorily checked out offline, all system connections should be completed. If all the installation steps have been completed to this point, the only cable to be installed should be the data cable into J1 on the logic/interface PCB. Table 3-3 presents the connections that should be made. For a listing and description of the signal lines in each cable, see Interface Requirements in Section 2.

(1) Make certain all necessary cable connections have been made.

(2) Set switches on logic/interface PCB as necessary (reference Table 3-5 for functions).

- Unit address (example; address 05, S1-1 and -3 closed [on], S1-2 and -4 open [off]).
- I CONFIGURATION disable, S1-5.
- Illegal head address, S1-6, -7, -8.
- Sector count, S2-1, -2, -3, -4, -5, -6, -7, -8, S3-1, -2, -3, and -4.
- Sequence enable, S3-6.

(3) Set drive ON/OFF switch to ON.

TABLE 3-3

SYSTEM CONNECTION INFORMATION

Connection	From	To
Ground (frame)		
External	E1 of power supply/ amplifier PCB	System tie point (controller, CPU, etc.)
Power		
AC	Disc drive (cord attached)	Site power source
DC (optional)	J26 of power supply/ amplifier assembly	External source
Signal cable	Controller	J2 on disc drive
	J3 on disc drive (daisy-chain)	J2 on next disc drive
Data cable	Controller	J1 on disc drive
Terminator		
Daisy-chain	J3 of last drive and E1 and E2 next to J3	
Star (radial)	J3 of each drive and E1 and E2 next to J3	

(4) Upon completion of first seek (RDY), run all available diagnostic routines. The routines must run error free. If trouble is encountered during testing, refer to the Maintenance Section of this manual.

(5) Replace the screws securing the PCB chassis and the power supply/amplifier chassis.

(6) Install the covers (top and bottom) on the Reflex II drive. Make certain there is no interference such as power supply cover touching fuse holders or bottom access cover not interfering with or touching belt, pulley, etc.

(7) If applicable, install the optional chassis slides on the sides of the disc drive. Use the hardware provided and install the disc drive into its cabinet space.

(8) The final check is the proper execution of all user programs (jobs). If the disc system is new and the user jobs have not been completely debugged, there is a possibility of software problems.

POWER VERIFICATION

Drives are shipped from the factory wired for the power source specified at the time of order. Before performing the drive installation, answer any questions that exist as to whether the drive matches the power source. The actual available line voltage must be measured and the drive power wiring must be verified. This verification relates to drives with the internal transformer assembly (power supply). If the internal transformer assembly is not present, the AC power source must be 115 VAC for the spindle motor. If the internal transformer assembly is present and the power source does not equal the drive wiring, refer to the Power Conversion paragraph in this section.

60 Hz Verification

(1) Verify that the nameplate on upper left rear of the unit indicates 60 Hz.

(2) Verify that the part number on top of power transformer ends with a -001.

(3) Verify that the part number on the motor pulley ends with a -002.

(4) Verify that the part number on the spindle belt ends with a -002.

(5) Verify the tab selection on power transformer. It must agree with measured input power. Tap selection is as follows:

1 = Common (neutral)
2 = 100 VAC
3 = 115 VAC
4 = 120 VAC
5 = 200 VAC
6 = 208 VAC
7 = 220 VAC
8 = 240 VAC

(6) Move input (wire from P26 pin 9) to correspond with proper tab.

50 Hz Verification

(1) Verify that the nameplate on upper left rear of the unit indicates 50 Hz.

(2) Verify that the part number on the top of power transformer ends with a -002.

(3) Verify that the part number on the motor pulley ends with a -003.

(4) Verify that the part number on the spindle belt ends with a -003.

(5) Verify the tab selection on power transformer. It must agree with measured input power. Tab selection is as follows:

1 = Common (neutral)
2 = 100 VAC
3 = 115 VAC
4 = 120 VAC
5 = 200 VAC
6 = 208 VAC
7 = 220 VAC
8 = 240 VAC

(6) Move input (wire from P26 pin 9) to correspond with proper tab.

POWER CONVERSION

60 Hz to 50 Hz

(1) Verify availability of the following parts before proceeding:

Transformer Assembly	A20013597-002
Pulley, Motor	D20013083-003
Belt, Drive	D20013085-003

(2) Position drive so that there is access to the power supply chassis and the bottom of the drive.

(3) Remove the top covers and the rear access (louvered) cover.

(4) Remove screws holding power supply chassis in place.

(5) Swing open the power supply chassis.

(6) Remove P26 from the power supply/amplifier assembly.

(7) Remove the bottom access cover to gain access to the spindle belt and pulley.

(8) While squeezing the spindle drive belt tension spring together, remove the drive belt.

CAUTION: Do not rotate the spindle by hand; damage to the heads and/or disc(s) is possible.

(9) Replace the pulley on the drive motor with the new one (reference Maintenance Section).

(10) While squeezing the spindle drive belt tension spring together, install new belt.

(11) Replace transformer assembly with new part.

(12) Select input tab on transformer, per Power Verification procedure.

(13) Reverse steps (7) through (3).

(14) Verify DC voltages.

50 Hz to 60 Hz

(1) Verify availability of the following parts before proceeding.

Transformer Assembly	A20013597-001
Pulley, Motor	D20013083-002
Belt, Drive	D20013085-002

(2) Perform steps (2) through (14) of 60 Hz to 50 Hz conversion steps.

OPERATION

Operator Indicator Panel

The optional panel is mounted in the lower left corner of the drive front panel (see Figure 3-7). The panel connects to connector J21 on the logic/interface PCB. The functions provided by the panel are presented in Table 3-4.

TABLE 3-4

OPERATOR INDICATOR PANEL

Term	Type	Function
WD and WE	Alternate Action switch	Write disable/write enable switch. When the switch is in the WD position, the drive will be write protected (write not allowed). Conversely, when the switch is in the WE position, writing is allowed.
WEI	Light Emitting diode (LED)	Write enable indicator. Indicates the status of the WD/WE switch. Off = Write disable (write protected) On = Write enable (write permitted)
RDYI	LED	Ready indicator. Off = Drive is not ready On = Disc(s) at full rotation speed, heads are loaded, and unit is ready to communicate with controller.
FLT	LED	Fault, Off = no faults, On = drive has one or more fault condition active. For a description of faults, see paragraph Interface Requirements, Status Lines, I FAULT in Section 2.

Maintenance Controls

A brief description of the maintenance controls is given in Table 3-5. Those controls that require a more detailed explanation are discussed under separate headings (unit address, illegal head detection and number of sectors).

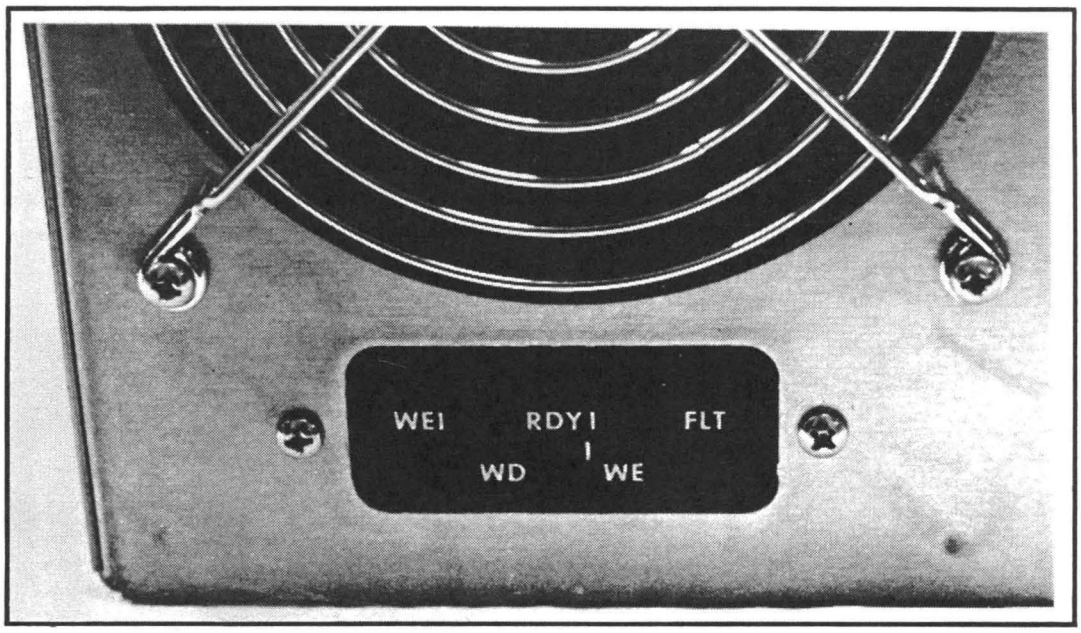


Figure 3-7. Operator Indicator Panel

TABLE 3-5

MAINTENANCE CONTROLS

Term	Type	Nomenclature	Location	Function
Power On/Off	Alternate action switch	S1	Power supply/ Amplifier assy. (Figure 3-8)	Controls source power to the drive unit.
Unit address selection	Alternate action switches	S1-1, -2, -3, -4	Logic/interface PCB (Figure 3-9)	Used to set the unit address. Addresses available are 0-15 decimal (0-F hexadecimal). See Unit Address Selection in this section for more detail.
Disable I CONFIGURATION	Alternate action switch	S1-5	Logic/interface PCB (Figure 3-9)	When closed (active), the switch disables the alternate status reporting provided by I CONFIGURATION.
Illegal head address	Alternate action switches	S1-6, -7, -8	Logic/interface PCB (Figure 3-9)	These switches are set to allow illegal head address detection. The settings depend upon the model (number of heads) and whether it is fixed head or not. See Illegal Head Address Selection headings in this section.
Sector selection	Alternate action switches	S2-1, -2, -3, -4, -5, -6, -7, -8, S3-1, -2 -3, -4	Logic/interface PCB (Figure 3-9)	Select the number of desired sectors per track. See Sector Selection heading in this section.
Sequence Enable switch	Alternate action switch	S3-6	Logic/interface PCB (Figure 3-9)	When closed, allows the drive to sequence up regardless of exerciser or controller connection. When open, sequence enable only becomes active if an exerciser is plugged in or the controller allows sequence enable.

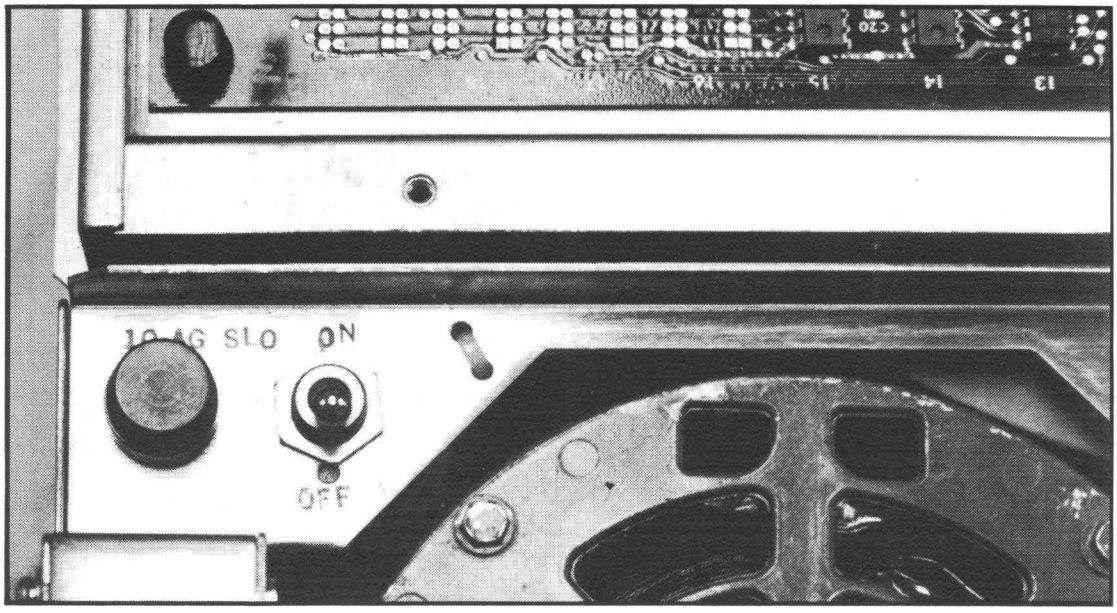
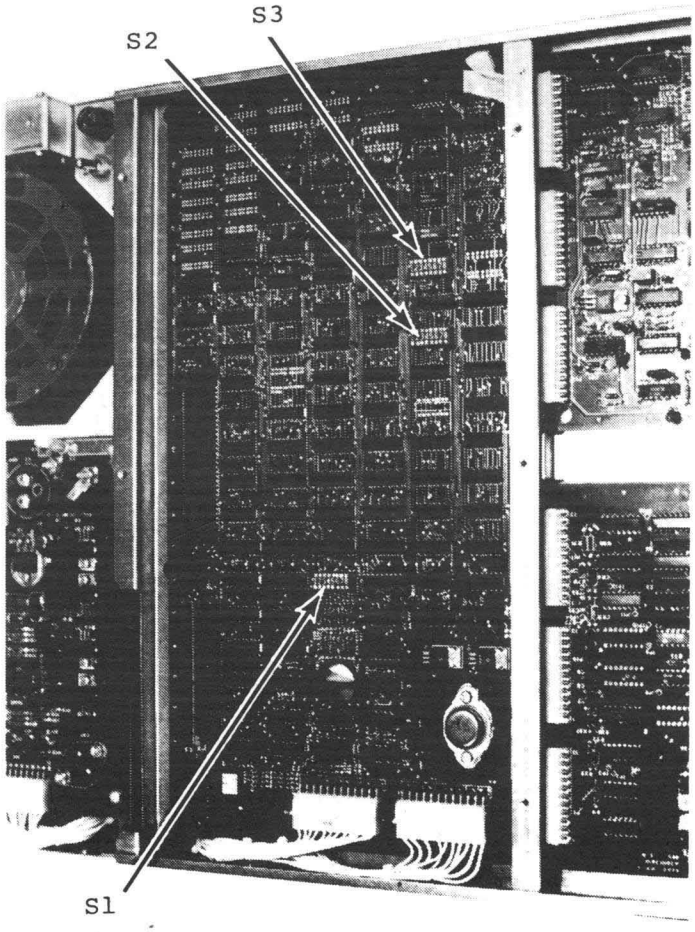
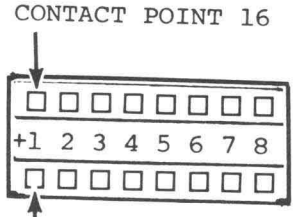


Figure 3-8. Power On/Off Switch



DIP SWITCHES HAVE THEIR POINTS COUNTED LIKE AN IC



REFERENCE TO SI-1 IS A REFERENCE TO DIP SWITCH SI CONTACTS 1 AND 16 WITH THE SWITCH CONTACTS BEING CLOSED WHEN THE ACTUATOR IS UP ON THE REFERENCE SIDE (-1)

Figure 3-9. Logic/Interface Switches

1. Unit Address Selection

The drive contains internal switches that are used to set the unit address. Four switches (S1-1, -2, -3, -4) allow for addresses 0 through 15 decimal (0 through F hexadecimal). Figur 3-9 shows the location of the switches. The switch settings are listed in Table 3-6.

TABLE 3-6

UNIT ADDRESS SWITCH SETTINGS

	SWITCH S1				I UNIT SEL BUS			
	-1	-2	-3	-4	3	2	1	0
Unit 0	0	0	0	0	0	0	0	0
Unit 1	0	0	0	1	0	0	0	1
Unit 2	0	0	1	0	0	0	1	0
Unit 3	0	0	1	1	0	0	1	1
Unit 4	0	1	0	0	0	1	0	0
Unit 5	0	1	0	1	0	1	0	1
Unit 6	0	1	1	0	0	1	1	0
Unit 7	0	1	1	1	0	1	1	1
Unit 8	1	0	0	0	1	0	0	0
Unit 9	1	0	0	1	1	0	0	1
Unit 10	1	0	1	0	1	0	1	0
Unit 11	1	0	1	1	1	0	1	1
Unit 12	1	1	0	0	1	1	0	0
Unit 13	1	1	0	1	1	1	0	1
Unit 14	1	1	1	0	1	1	1	0
Unit 15	1	1	1	1	1	1	1	1

Switch setting 1 = Switch open (off, inactive)

Switch setting 0 = Switch closed (on, active)

I UNIT SEL BUS = 1 indicates active condition.

2. Illegal Head Address Selection

The drive contains internal switches that are set to correspond to the number of heads in the unit. In essence, this sets the extent limit. Any attempt to select a head address beyond the extent will generate an illegal head signal. Three switches (S1-6, -7, -8) are used. S1-6 and -7 provide the selection for the standard moving head. S1-8 is used for the fixed head option. Figure 3-9 shows the location of the

switches. Table 3-7 is a chart presenting the appropriate settings.

TABLE 3-7

HEAD SELECTION SWITCH SETTINGS

		SWITCH S1 -6	-7	-8	
Reflex II Models	A	0	0	X	0 = Switch closed/on
	B	0	1	X	
	C	1	0	X	1 = Switch open/off
	D	1	1	X	
60 Track Fix Hd		X	X	0	X = Doesn't matter
No Fix Hd		X	X	1	

3. Sector Selection

The drive contains internal switches that are used to set the number of sectors per track. The maximum count available is 4095. Each count is equal to one data byte. Therefore, the maximum number of bytes between sector pulses is 4096 (0-4095) and the minimum number is one byte. Twelve switches are used for this function. The switches are S2-1, -2, -3, -4, -5, -6, -7, -8 (all sections) and S3-1, -2, -3, -4. Figure 3-9 shows the location of the switches. Table 3-8 presents the number of sectors with their length and possible remainder for the different switch settings. Figure 3-10 graphically presents sector pulses and length with regard to index.

To determine the switch settings, first select the desired number of sectors (S) per track. Divide the number represented by S into the constant 20,160 (number of bytes per track). The result (quotient) is the number of bytes (B) per sector. If the result includes a remainder, take the whole number as bytes (B) per sector, multiply B times S and subtract that result from 20,160. The result is the number of bytes to be added to the last sector (remainder).

When the number represented by B is available, subtract B from 4096 (the count that produces a sector). The result is the decimal number that must be converted to a binary number and then loaded into the switches. The weights of the switches are (for number conversions see Appendix B):

Switch	S3-4	S3-3	S3-2	S3-1	S2-8	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1
Binary Weight	2048	1024	512	256	128	64	32	16	8	4	2	1

Example: Number of sectors (S) per track = 44

$$\frac{20,160}{44} = 458.18$$

458 = number of bytes (B) per sector

```
   458 (B)
    44 (S)
------
20,152 number of bytes consumed in 44 sectors

20,160 number of bytes per track
- 20,152 number of bytes consumed in 44 sectors
------
     8 remaining bytes (remainder)
```

The last sector will be 8 bytes longer than all other sectors.

```
  4096 count which produces a sector pulse
- 458 (B)
------
 3638 decimal count to be loaded in switches
```

3638 converts to a binary number of 1110 0011 0110; set switches S3-1, S2-8, S2-7, S2-4, S2-1 on (closed), all other switches to be off (open).

TABLE 3-8

SECTOR SELECTION

NUMBER OF SECTORS	BYTES (NO.) NOMINAL - LAST	DIFF*	DURATION (µsec) NOMINAL - LAST	DIFF*	SWITCH SETTING S3-4	S3-3	S3-2	S3-1	S2-8	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1
4	4096 - 7872	3776	3453.26 - 6636.74	3183.48	0	0	0	0	0	0	0	0	0	0	0	0
5	4032 - 4032	0	3399.30 - 3399.30	0	0	0	0	0	0	1	0	0	0	0	0	0
6	3360 - 3360	0	2832.75 - 2832.75	0	0	0	1	0	1	1	1	0	0	0	0	0
7	2880 - 2880	0	2428.07 - 2428.07	0	0	1	0	0	1	1	0	0	0	0	0	0
8	2520 - 2520	0	2124.57 - 2124.57	0	0	1	1	0	0	0	1	0	1	0	0	0
9	2240 - 2240	0	1888.50 - 1888.50	0	0	1	1	1	0	1	0	0	0	0	0	0
10	2016 - 2016	0	1699.65 - 1699.65	0	1	0	0	0	0	0	1	0	0	0	0	0
11	1832 - 1840	8	1544.53 - 1551.27	6.74	1	0	0	0	1	1	0	1	0	0	0	0
12	1680 - 1680	0	1416.38 - 1416.38	0	1	0	0	1	0	1	1	1	0	0	0	0
13	1550 - 1560	10	1306.78 - 1315.21	8.43	1	0	0	1	1	1	1	0	1	0	0	0
14	1440 - 1440	0	1214.04 - 1214.04	0	1	0	1	0	0	1	1	0	0	0	0	0
15	1344 - 1344	0	1133.10 - 1133.10	0	1	0	1	0	1	1	0	0	0	0	0	0
16	1260 - 1260	0	1062.28 - 1062.28	0	1	0	1	1	0	0	0	1	0	1	0	0
17	1185 - 1200	15	999.05 - 1011.70	12.65	1	0	1	1	0	1	0	1	1	1	1	1
18	1120 - 1120	0	944.25 - 944.25	0	1	0	1	1	1	0	1	0	0	0	0	0
19	1061 - 1062	1	894.51 - 895.35	0.84	1	0	1	1	1	1	0	1	1	0	1	1
20	1008 - 1008	0	849.83 - 849.83	0	1	1	0	0	0	0	0	1	0	0	0	0
21	960 - 960	0	809.36 - 809.36	0	1	1	0	0	0	1	0	0	0	0	0	0
22	916 - 924	8	772.26 - 779.01	6.74	1	1	0	0	0	1	1	0	1	1	0	0
23	876 - 888	12	738.54 - 748.66	10.12	1	1	0	0	1	0	0	1	0	1	0	0
24	840 - 840	0	708.19 - 708.19	0	1	1	0	0	1	0	1	1	1	0	0	0
25	806 - 816	10	679.52 - 687.95	8.43	1	1	0	0	1	1	0	1	1	0	1	0
26	775 - 785	10	653.39 - 661.82	8.43	1	1	0	0	1	1	1	1	1	0	0	1
27	746 - 764	18	628.94 - 644.11	15.18	1	1	0	1	0	0	0	1	0	1	1	0
28	720 - 720	0	607.02 - 607.02	0	1	1	0	1	0	0	1	1	0	0	0	0
29	695 - 700	5	585.94 - 590.16	4.22	1	1	0	1	0	1	0	0	1	0	0	1
30	672 - 672	0	566.55 - 566.55	0	1	1	0	1	0	1	1	0	0	0	0	0
31	650 - 660	10	548.00 - 556.43	8.43	1	1	0	1	0	1	1	1	0	1	1	0
32	630 - 630	0	531.14 - 531.14	0	1	1	0	1	1	0	0	0	1	0	1	0
33	610 - 640	30	514.28 - 539.57	25.29	1	1	0	1	1	0	0	1	1	1	1	0
34	592 - 624	32	499.10 - 526.08	26.98	1	1	0	1	1	0	1	1	0	0	0	0
35	576 - 576	0	485.61 - 485.61	0	1	1	0	1	1	1	0	0	0	0	0	0
36	560 - 560	0	472.13 - 472.13	0	1	1	0	1	1	1	0	1	0	0	0	0
37	544 - 576	32	458.64 - 485.61	26.98	1	1	0	1	1	1	1	0	0	0	0	0
38	530 - 550	20	446.83 - 463.69	16.86	1	1	0	1	1	1	1	0	1	1	1	0

TABLE 3-8, SECTOR SELECTION (Cont'd)

NUMBER OF SECTORS	BYTES (NO.) NOMINAL - LAST	DIFF*	DURATION (μsec) NOMINAL - LAST	DIFF*	SWITCH SETTING S3-4	S3-3	S3-2	S3-1	S2-8	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1
39	516 - 552	36	435.03 - 465.38	30.35	1	1	0	1	1	1	1	1	1	1	0	0
40	504 - 504	0	424.91 - 424.91	0	1	1	1	0	0	0	0	0	1	0	0	0
41	491 - 520	29	413.95 - 438.40	24.45	1	1	1	0	0	0	0	1	0	1	0	1
42	480 - 480	0	404.70 - 404.70	0	1	1	1	0	0	0	1	0	0	0	0	0
43	468 - 504	36	394.56 - 424.91	30.35	1	1	1	0	0	0	1	0	1	1	0	0
44	458 - 466	8	386.13 - 392.88	6.74	1	1	1	0	0	0	1	1	0	1	1	0
45	448 - 448	0	377.70 - 377.70	0	1	1	1	0	0	1	0	0	0	0	0	0
46	438 - 450	12	369.27 - 379.39	10.12	1	1	1	0	0	1	0	0	1	0	1	0
47	428 - 472	44	360.84 - 397.93	37.10	1	1	1	0	0	1	0	1	0	1	0	0
48	420 - 420	0	354.09 - 354.09	0	1	1	1	0	0	1	0	1	1	1	0	0
49	411 - 432	21	346.51 - 364.21	17.70	1	1	1	0	0	1	1	0	0	1	0	1
50	403 - 413	10	339.76 - 348.19	8.43	1	1	1	0	0	1	1	0	1	1	0	1
51	395 - 410	15	333.02 - 345.66	12.65	1	1	1	0	0	1	1	1	0	1	0	1
52	387 - 423	36	326.27 - 356.62	30.35	1	1	1	0	0	1	1	1	1	1	0	1
53	380 - 400	20	320.37 - 337.23	16.86	1	1	1	0	1	0	0	0	0	1	0	0
54	373 - 391	18	314.47 - 329.64	15.18	1	1	1	0	1	0	0	0	1	0	1	1
55	366 - 396	30	308.57 - 333.86	25.29	1	1	1	0	1	0	0	1	0	0	1	0
56	360 - 360	0	303.51 - 303.51	0	1	1	1	0	1	0	0	1	1	0	0	0
57	353 - 392	39	297.61 - 330.49	32.88	1	1	1	0	1	0	0	1	1	1	1	1
58	347 - 381	34	292.55 - 321.21	28.66	1	1	1	0	1	0	1	0	0	1	0	1
59	341 - 382	41	287.49 - 322.06	34.57	1	1	1	0	1	0	1	0	1	0	1	1
60	336 - 336	0	283.28 - 283.28	0	1	1	1	0	1	0	1	1	0	0	0	0
61	330 - 360	30	278.22 - 303.51	25.29	1	1	1	0	1	0	1	1	0	1	1	0
62	325 - 335	10	274.00 - 282.43	8.43	1	1	1	0	1	0	1	1	1	0	1	1
63	320 - 320	0	269.79 - 269.79	0	1	1	1	0	1	1	0	0	0	0	0	0
64	315 - 315	0	265.57 - 265.57	0	1	1	1	0	1	1	0	0	0	1	0	1
65	310 - 320	10	261.36 - 269.79	8.43	1	1	1	0	1	1	0	0	1	0	1	0
66	305 - 335	30	257.14 - 282.43	25.29	1	1	1	0	1	1	0	0	1	1	1	1
67	300 - 360	60	252.92 - 303.51	50.58	1	1	1	0	1	1	0	1	0	1	0	0
68	296 - 328	32	249.55 - 276.53	26.98	1	1	1	0	1	1	0	1	1	0	0	0
69	292 - 304	12	246.18 - 256.30	10.12	1	1	1	0	1	1	0	1	1	1	0	0
70	288 - 288	0	242.81 - 242.81	0	1	1	1	0	1	1	1	0	0	0	0	0
71	283 - 350	67	238.59 - 295.08	56.49	1	1	1	0	1	1	1	0	0	1	0	1
72	280 - 280	0	236.06 - 236.06	0	1	1	1	0	1	1	1	0	1	0	0	0
73	276 - 288	12	232.69 - 242.81	10.12	1	1	1	0	1	1	1	0	1	1	0	0

TABLE 3-8, SECTOR SELECTION (Cont'd)

NUMBER OF SECTORS	BYTES (NO.) NOMINAL - LAST	DIFF*	DURATION (μsec) NOMINAL - LAST	DIFF*	SWITCH SETTING S3-4	S3-3	S3-2	S3-1	S2-8	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1
74	272 - 304	32	229.32 - 256.30	26.98	1	1	1	0	1	1	1	1	0	0	0	0
75	268 - 328	60	225.95 - 276.53	50.58	1	1	1	0	1	1	1	1	0	1	0	0
76	265 - 285	20	223.42 - 240.28	16.86	1	1	1	0	1	1	1	1	0	1	1	1
77	261 - 324	63	220.04 - 273.16	53.11	1	1	1	0	1	1	1	1	1	0	1	1
78	258 - 294	36	217.52 - 247.87	30.35	1	1	1	0	1	1	1	1	1	1	1	0
79	255 - 270	15	214.99 - 227.63	12.65	1	1	1	1	0	0	0	0	0	0	0	1
80	252 - 252	0	212.46 - 212.46	0	1	1	1	1	0	0	0	0	0	1	0	0
81	248 - 320	72	209.08 - 269.79	60.70	1	1	1	1	0	0	0	0	1	0	0	0
82	245 - 315	70	206.55 - 265.57	59.02	1	1	1	1	0	0	0	0	1	0	1	1
83	242 - 316	74	204.03 - 266.41	62.39	1	1	1	1	0	0	0	0	1	1	1	0
84	240 - 240	0	202.34 - 202.34	0	1	1	1	1	0	0	0	1	0	0	0	0
85	237 - 252	15	199.81 - 212.46	12.65	1	1	1	1	0	0	0	1	0	0	1	1
86	234 - 270	36	197.28 - 227.63	30.35	1	1	1	1	0	0	0	1	0	1	1	0
87	231 - 294	63	194.75 - 247.87	53.11	1	1	1	1	0	0	0	1	1	0	0	1
88	229 - 237	8	193.07 - 199.81	6.74	1	1	1	1	0	0	0	1	1	0	1	1
89	226 - 272	46	190.54 - 229.32	38.78	1	1	1	1	0	0	0	1	1	1	1	0
90	224 - 224	0	188.85 - 188.85	0	1	1	1	1	0	0	1	0	0	0	0	0
91	221 - 270	49	186.32 - 227.63	41.31	1	1	1	1	0	0	1	0	0	0	1	1
92	219 - 231	12	184.63 - 194.75	10.12	1	1	1	1	0	0	1	0	0	1	0	1
93	216 - 288	72	182.11 - 242.81	60.70	1	1	1	1	0	0	1	0	1	0	0	0
94	214 - 258	44	180.42 - 217.52	37.10	1	1	1	1	0	0	1	0	1	0	1	0
95	212 - 232	20	178.73 - 195.59	16.86	1	1	1	1	0	0	1	0	1	1	0	0
96	210 - 210	0	177.05 - 177.05	0	1	1	1	1	0	0	1	0	1	1	1	0
97	207 - 288	81	174.52 - 242.81	68.29	1	1	1	1	0	0	1	1	0	0	0	1
98	205 - 275	70	172.83 - 231.85	59.02	1	1	1	1	0	0	1	1	0	0	1	1
99	203 - 266	63	171.15 - 224.26	53.11	1	1	1	1	0	0	1	1	0	1	0	1
100	201 - 261	60	169.46 - 220.04	50.58	1	1	1	1	0	0	1	1	0	1	1	1
101	199 - 260	61	167.77 - 219.20	51.43	1	1	1	1	0	0	1	1	1	0	0	1
102	197 - 263	66	166.09 - 221.73	55.64	1	1	1	1	0	0	1	1	1	0	1	1
103	195 - 270	75	164.40 - 227.63	63.23	1	1	1	1	0	0	1	1	1	1	0	1
104	193 - 281	88	162.71 - 236.91	74.19	1	1	1	1	0	0	1	1	1	1	1	1
105	192 - 192	0	161.87 - 161.87	0	1	1	1	1	0	1	0	0	0	0	0	0
106	190 - 210	20	160.19 - 177.05	16.86	1	1	1	1	0	1	0	0	0	0	1	0
107	188 - 232	44	158.50 - 195.59	37.10	1	1	1	1	0	1	0	0	0	1	0	0
108	186 - 258	72	156.81 - 217.52	60.70	1	1	1	1	0	1	0	0	0	1	1	0

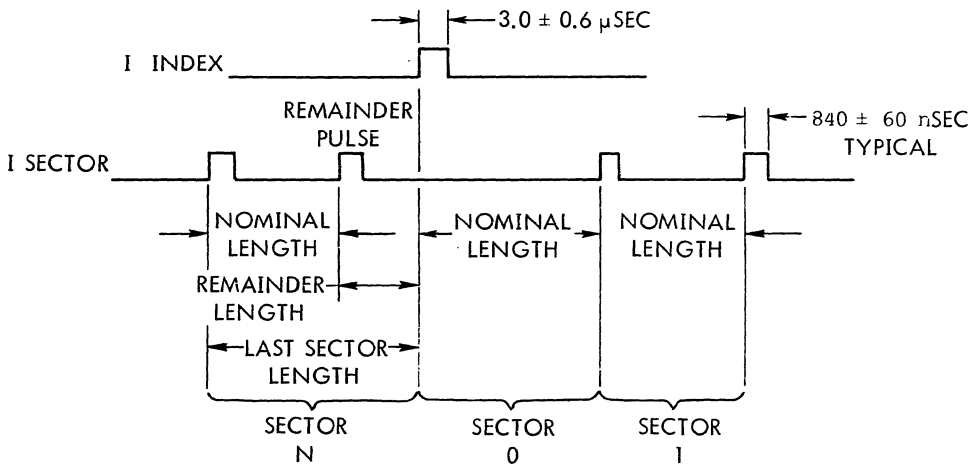
TABLE 3-8 SECTOR SELECTION (Cont'd)

NUMBER OF SECTORS	BYTES (NO.) NOMINAL - LAST	DIFF*	DURATION (μsec) NOMINAL - LAST	DIFF*	SWITCH SETTING S3-4	S3-3	S3-2	S3-1	S2-8	S2-7	S2-6	S2-5	S2-4	S2-3	S2-2	S2-1
109	184 - 288	104	155.13 - 242.81	87.68	1	1	1	1	0	1	0	0	1	0	0	0
110	183 - 213	30	154.28 - 179.58	25.29	1	1	1	1	0	1	0	0	1	0	0	1
111	181 - 250	69	152.60 - 210.77	58.17	1	1	1	1	0	1	0	0	1	0	1	1
112	180 - 180	0	151.75 - 151.75	0	1	1	1	1	0	1	0	0	1	1	0	0
113	178 - 224	46	150.07 - 188.85	38.78	1	1	1	1	0	1	0	0	1	1	1	0
114	176 - 272	96	148.38 - 229.32	80.94	1	1	1	1	0	1	0	1	0	0	0	0
115	175 - 210	35	147.54 - 177.05	29.51	1	1	1	1	0	1	0	1	0	0	0	1
116	173 - 265	92	145.85 - 223.42	77.56	1	1	1	1	0	1	0	1	0	0	1	1
117	172 - 208	36	145.01 - 175.36	30.35	1	1	1	1	0	1	0	1	0	1	0	0
118	170 - 270	100	143.32 - 227.63	84.31	1	1	1	1	0	1	0	1	0	1	1	0
119	169 - 218	49	142.48 - 183.79	41.31	1	1	1	1	0	1	0	1	0	1	1	1
120	168 - 168	0	141.64 - 141.64	0	1	1	1	1	0	1	0	1	1	0	0	0
121	166 - 240	74	139.95 - 202.34	62.39	1	1	1	1	0	1	0	1	1	0	1	0
122	165 - 195	30	139.11 - 164.40	25.29	1	1	1	1	0	1	0	1	1	0	1	1
123	163 - 274	111	137.42 - 231.00	93.58	1	1	1	1	0	1	0	1	1	1	0	1
124	162 - 234	72	136.58 - 197.28	60.70	1	1	1	1	0	1	0	1	1	1	1	0
125	161 - 196	35	135.74 - 165.24	29.51	1	1	1	1	0	1	0	1	1	1	1	1
126	160 - 160	0	134.89 - 134.89	0	1	1	1	1	0	1	1	0	0	0	0	0
127	158 - 252	94	133.21 - 212.46	79.25	1	1	1	1	0	1	1	0	0	0	1	0
128	157 - 221	64	132.36 - 186.32	53.96	1	1	1	1	0	1	1	0	0	0	1	1

* A remainder that causes the last sector to be longer than the nominal sector length. During this remainder there will be an additional sector pulse (see Figure 3-10).

Switch setting 1 = switch open (off, inactive)

Switch setting 0 = switch closed (on, active)



SECTION 4

THEORY OF OPERATION

INTRODUCTION

This section contains information describing circuitry and overall operation of the disc drive. The information is provided to give maintenance personnel an understanding of the disc drive functions.

PHYSICAL DESCRIPTION

The Reflex II disc drive is a high performance dual-head-per-surface device that enables the central processing unit (CPU) of a data processing system to store and retrieve blocks (records) of data on the rotating disc(s). The drive functions as an input/output (I/O) device to the CPU. It can operate in a star (radial) configuration or a daisy-chain configuration with up to 15 similar disc drives.

The elements of the Reflex II are power components, transformer assembly (optional), cooling fans, sealed module and motor assembly, printed circuit boards (PCB's), and LED/switch panel (optional indicator panel).

Power Components

The power components are as follows: line cord, line filter assembly, switch, fuse, relay, solid state switch, and a capacitor. These components are necessary to get AC power from the source to the spindle motor and, if applicable, to the optional transformer assembly.

Transformer Assembly (optional)

This assembly supplies the necessary DC voltages to the power supply/amplifier PCB, and 115 VAC to the spindle motor and fans.

The power components, transformer assembly, and power supply/amplifier PCB are located on or within the power supply/amplifier chassis.

Sealed Module and Motor Assembly

This assembly is comprised of the spindle, disc(s), carriage lock, heads, carriage, way, linear motor, crash stops, air filters, clean air system, metal structure, and head connector PCB. The fixed head-per-track module is also included if that option is present. Attached to the sealed module are the brake, ground brush, spring loaded spindle motor, and drive belt.

Printed Circuit Boards

The standard unit has four PCB's. The power supply/amplifier PCB is mounted on the power supply/amplifier chassis. The logic/interface PCB, the servo PCB, and the read/write PCB are mounted on the PCB chassis. In addition, a fifth PCB (the LED/switch) is present if the optional indicator panel is installed. The LED/switch PCB is mounted to the front panel of the frame.

General

Operation of the drive requires an associated control unit that will provide the necessary control and buffering between the CPU and the disc drive. Several operations must be performed by the control unit when data is to be recorded by a disc drive. The disc drive must be selected, its status must be checked to be normal, its heads must be positioned to the proper cylinder, and one of the read/write heads must be selected. The control unit then arranges the data from the CPU into the proper recording format, and transmits it to the drive in a serial NRZ form. This NRZ data is converted by the drive into MFM data, which is then recorded on the specified track via the selected read/write head.

To retrieve stored data, the control unit selects the drive, checks the status lines, sends the appropriate commands to position the heads to the desired cylinder, selects the desired read/write head, and enables the read circuitry. The drive responds by reading the data in a serial form, amplifies and shapes the data, converts it from MFM to NRZ and then sends it to the control unit. The control unit assembles the data and transfers it to the CPU.

To accomplish its task as an I/O unit, the physical elements of the disc drive are divided into several groups consisting of the following:

- Input/output interface
- Positioning system
- Cooling and clean air system
- Read/write system
- Spindle motor system

1. Input/Output Interface

The input/output interface contains the logic necessary to allow communications between the control unit and the positioning and read/write systems. It is physically contained on the logic/interface PCB.

2. Positioning System

The positioning system consists of the servo control logic on the logic/interface PCB, the servo logic on the servo PCB, and the power amplifier on the power supply/amplifier PCB. Also included are the linear motor, carriage, ways and servo head, all contained within the sealed module assembly.

The positioning system provides for the positioning of the heads as commanded from the control unit via the input interface.

3. Cooling and Clean Air System

Two cooling fans are mounted at the front of the frame. They provide an airflow through the unit to help dissipate heat generated within the unit. The fans are capable of an unrestricted airflow of 120 CFM. This airflow keeps the temperature rise within the unit less than 8°C (14°F) higher than the outside air temperature. The airflow keeps the temperature rise within the sealed module to less than 17° (30°F) higher than the surrounding air temperature.

The clean air system is contained within the sealed module assembly and consists of two absolute filters, an air pump, and seals. The two filters are a breather filter and a recirculation filter. The system is implemented to control pressure levels within the module so that the breather filter need pass only 0.01 CFM maximum.

The air pump is the spinning discs which causes frequent air exchange through the filter. The breather filter allows a transfer of air in or out of the assembly as temperatures change, or replenishes air that has escaped through minor leaks in the system. The recirculation filter is located so that the movement of air caused by the disc rotation forces air through the filter. This recirculation of air through the filter eliminates any contaminants that might enter the module.

4. Read/Write System

The read/write system consists of the following; the read/write control logic on the logic/interface PCB, the read/write electronics on the read/write PCB, and the discs and read/write heads contained within the sealed module assembly.

Also included is the servo PLO signal , which is spread across the read/write PCB, servo PCB, servo head and the servo surface on the bottom disc.

The read/write system provides for storage and retrival of data as commanded by the control unit via the input/output interface.

5. Spindle Motor System

This system consists of the spindle motor, pulley, belt, spring, and spindle. The spindle motor system provides for rotation of the discs at the proper speed.

FUNCTIONAL DESCRIPTION

The system block diagram of the Reflex II is presented in Figure 4-1. This diagram presents the major elements of the drive which include:

- Power supplies and distribution
- Input interface
- Drive selection
- Sequence control
- Function decode
- Positioning system
- Sector generation
- Read/write system
- Error detection
- Status
- Output interface

General

The Reflex II disc drive utilizes IBM 3350 style read/write heads and discs. The recording medium is from one to four 14-inch discs. Each disc consists of an aluminum substrate with an oxide coating and a lubricant overcoat. This coating is burnished to a flatness on the order of 12 microinches to allow the heads to fly in proximity to the surface without actual physical contact.

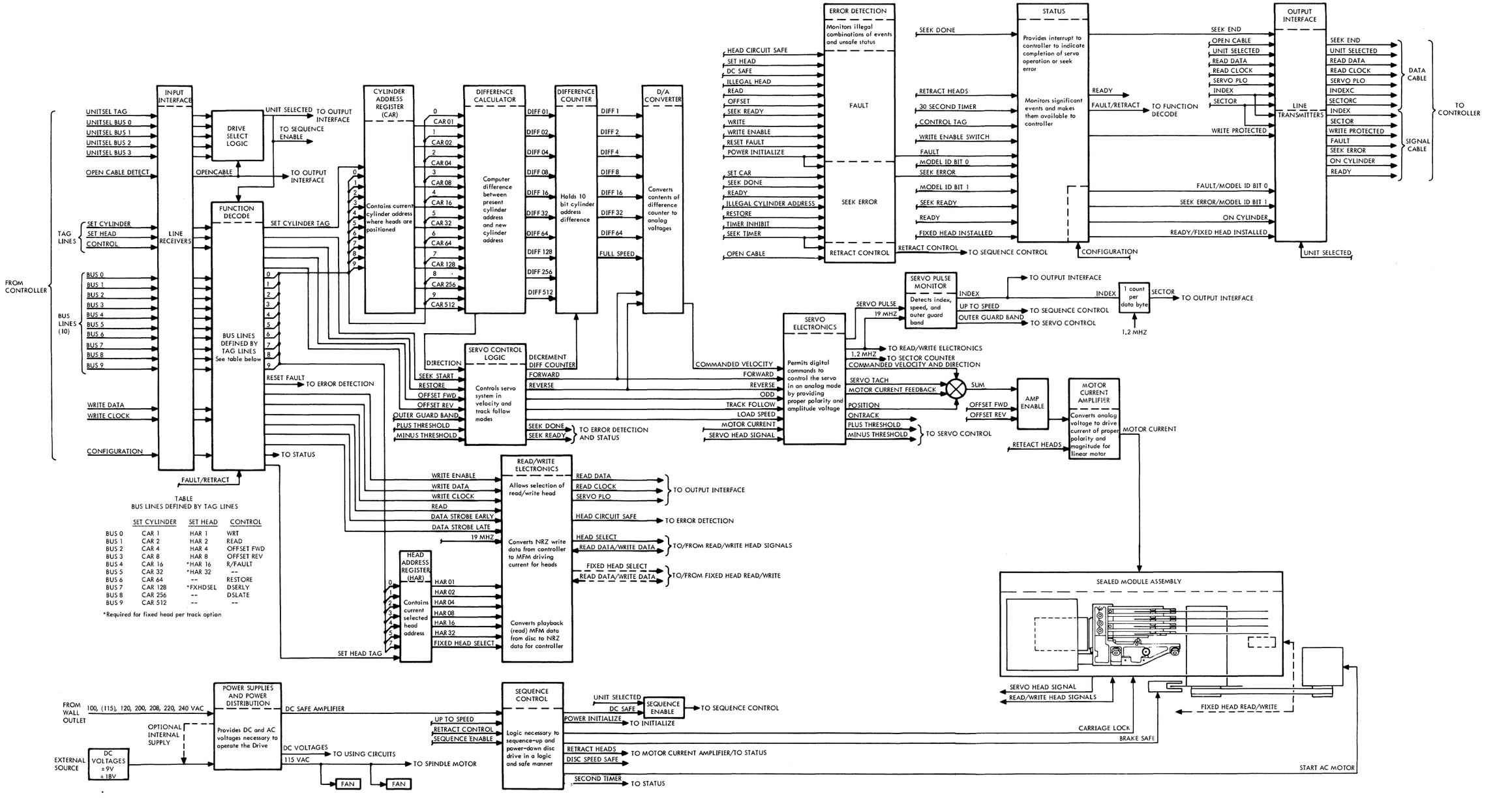


Figure 4-1. REFLEX II System Block Diagram

Data is recorded in serial fashion in concentric rings on each disc surface by holding the head in a fixed position over the rotating disc(s). These rings are referred to as tracks. The postioning system locates the heads precisely over the tracks. Corresponding track positions, both upper and lower on each disc, are referred to as one cylinder of data. The disc drive has 561 cylinders with two heads per surface, except for the servo surface, which has one head. This provides for an inner and outer cylinder with a total of 1122 tracks per surface. The odd-numbered heads comprise the inner cylinder and the even-numbered heads comprise the outer cylinder.

A center-tapped coil is mounted on the core of the read/write head to perform the read/write function. The recording flux direction is controlled by energizing the center-tap connection. This causes current to flow through the winding from the center tap to either one end or the other. When reading, the ends of the coil are switched to the input of the read amplifier and the center tap is grounded. Data is erased by overwriting with new data.

The head coil is mounted in a ferrite slider as shown in Figure 4-2. The sliders are spring loaded. This spring loading action forces them into contact with the lubricated disc surface when the unit is powered down. The lubricant overcoat permits head contact without damage. As the disc(s) rotates, it pulls a film of air around its surface. This air moves under the slider and exerts an upward force on the slider. The air pressure from this film of air grows to a value that counteracts the spring loading of the slider, so that at operating speed the heads fly at approximately 20 microinches above the disc surface. The flying height is influenced in part by the film of air and the spring force.

The head slider is mounted to the head arm assembly via a gimballed spring mount. This allows the slider to vary its flying altitude so that it can follow minor surface variations without contacting the disc surface.

The head assemblies are mounted to a carriage which is supported by bearings and ways. The carriage moves the heads as one unit, radially across the disc(s) surface to the different track locations. All heads are positioned to the same cylinder at any given time. The servo disc provides the positioning (servo) system with information that allows it to position precisely the head gaps over any of the tracks on a disc surface.

The carriage has a travel of approximately 1.2 inches with crash stops at either end to cushion the shock in case of a drive malfunction. There is a fail-safe solenoid operated carriage latch that locks the carriage in the reverse position when the drive is not operating.

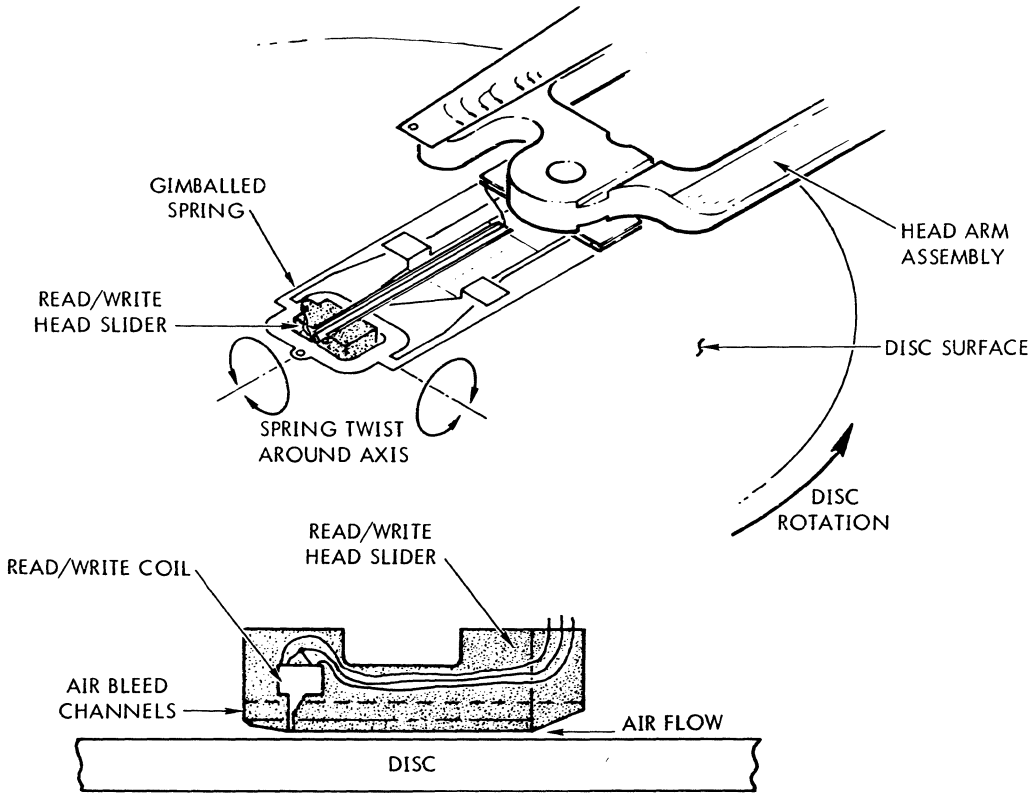


Figure 4-2. Typical Read/Write Head

The carriage is attached to the coil (bobbin) part of the linear motor assembly. The linear motor provides the force of motion and is controlled by the positioning system.

The discs(s) are rotated by the spindle drive system, which consists of an AC motor, pulleys, belt, disc brake, spindle, and associated power circuitry. The motor and brake are sized for proper acceleration and deceleration rates corresponding to the 3350 contact start/stop head requirements.

The spindle motor is a 2-pole, capacitor-start motor that generates high start torque relative to running torque. During the start cycle, the start winding and series capacitor are energized by a relay that is dependent upon the amount of current going through the run winding. During start conditions, the current in the run winding is high and the relay energizes the start circuit. As the monitor accelerates to speed, the run winding current decreases and the relay drops out at a predetermined speed, leaving the run winding to bring the spindle up to operating speed.

The motor is thermally protected to prevent damage during unusual overload conditions. There is a thermostatic switch device built into the motor that will open and turn off the solid state relay powering the motor when the motor temperature exceeds a predetermined level.

The disc brake is a solenoid-operated, fail-safe device. It consists of a disc mounted to the spindle pulley, a caliper assembly with friction material pads, a spring that forces the pads against the disc, and a solenoid that overcomes the spring force to allow the spindle to rotate freely. Thus, with no power applied to the brake system, the brake pads are forced against the brake disc by the spring force, and the spindle is inhibited from rotating. When the drive has power applied, the solenoid is energized and held on, overcoming the spring force that releases the brake pads from the brake disc. This allows the spindle to rotate freely.

The spindle motor torque is transmitted to the spindle through pulleys and a belt. The system is spring-loaded at the motor mounting plate, which creates the proper amount of belt tension to keep the belt from slipping. The belt is sufficiently conductive to prevent static charge accumulation. The motor pulley is hard-anodized to provide an electrical insulation to keep AC and DC ground systems isolated.

Power Supplies and Distribution

1. Standard Power Configuration

The Reflex II disc drive, in its basic configuration, requires +18 VDC, +9 VDC, and 115 VAC to be supplied by the user. The 115 VAC is used to power the spindle motor and the cooling fans. The +18 VDC and +9 VDC are routed to the power supply/amplifier PCB (see Figure 4-3).

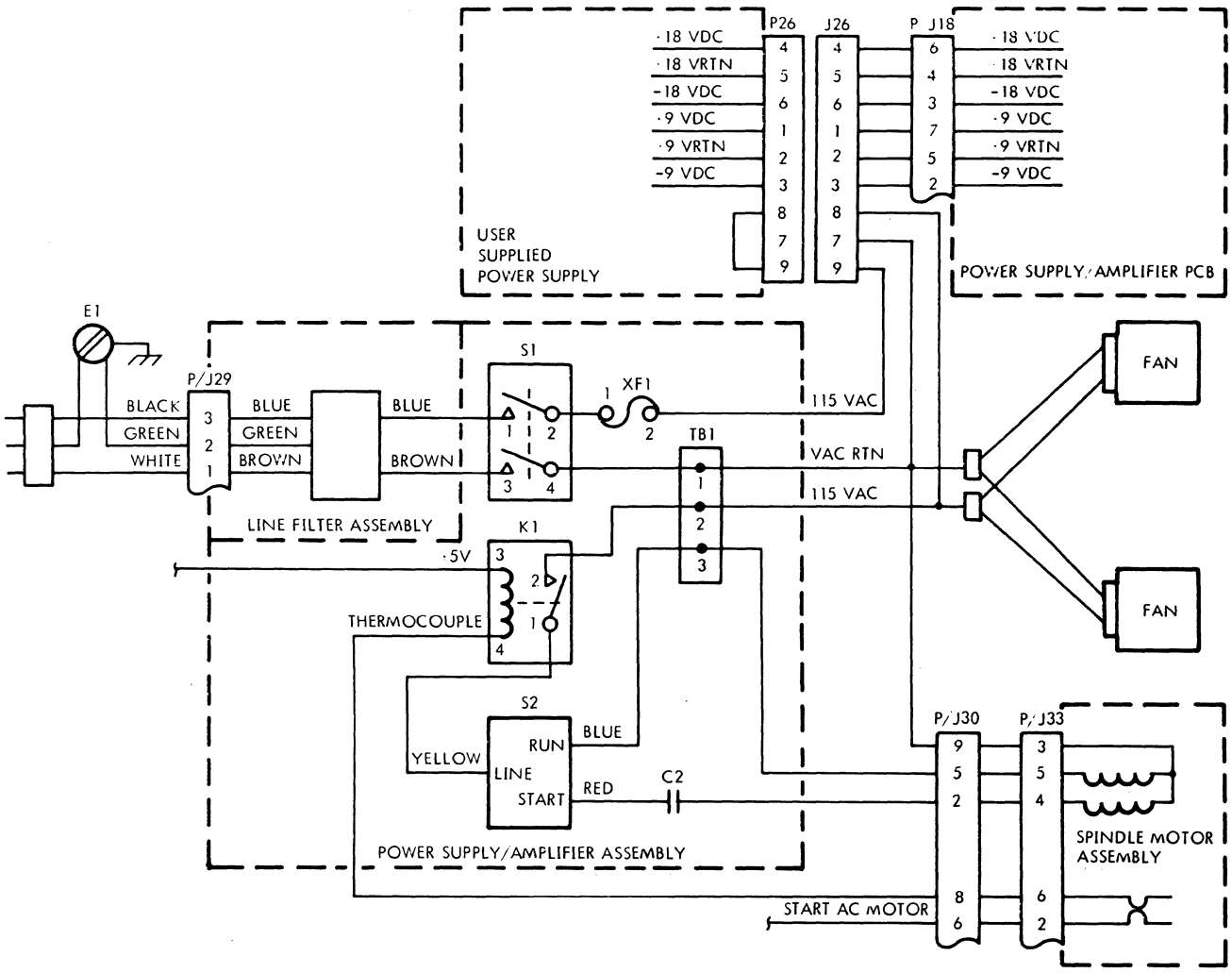


Figure 4-3. Standard Power Configuration and AC Distribution

2. Optional Power Configuration

The optional power supply configuration provides a transformer assembly. This constant voltage transformer assembly allows input voltages of 100, 115, 120, 200, 208, 220, and 240 VAC. All of these must be supplied by the user. The primary has tap selection for the applicable input voltage to provide 115 VAC power to the spindle motor and the cooling fans. The secondaries are center tapped and bridge rectified to provide ± 18 VDC and ± 9 VDC, and are routed to the power supply/amplifier PCB (see Figure 4-4).

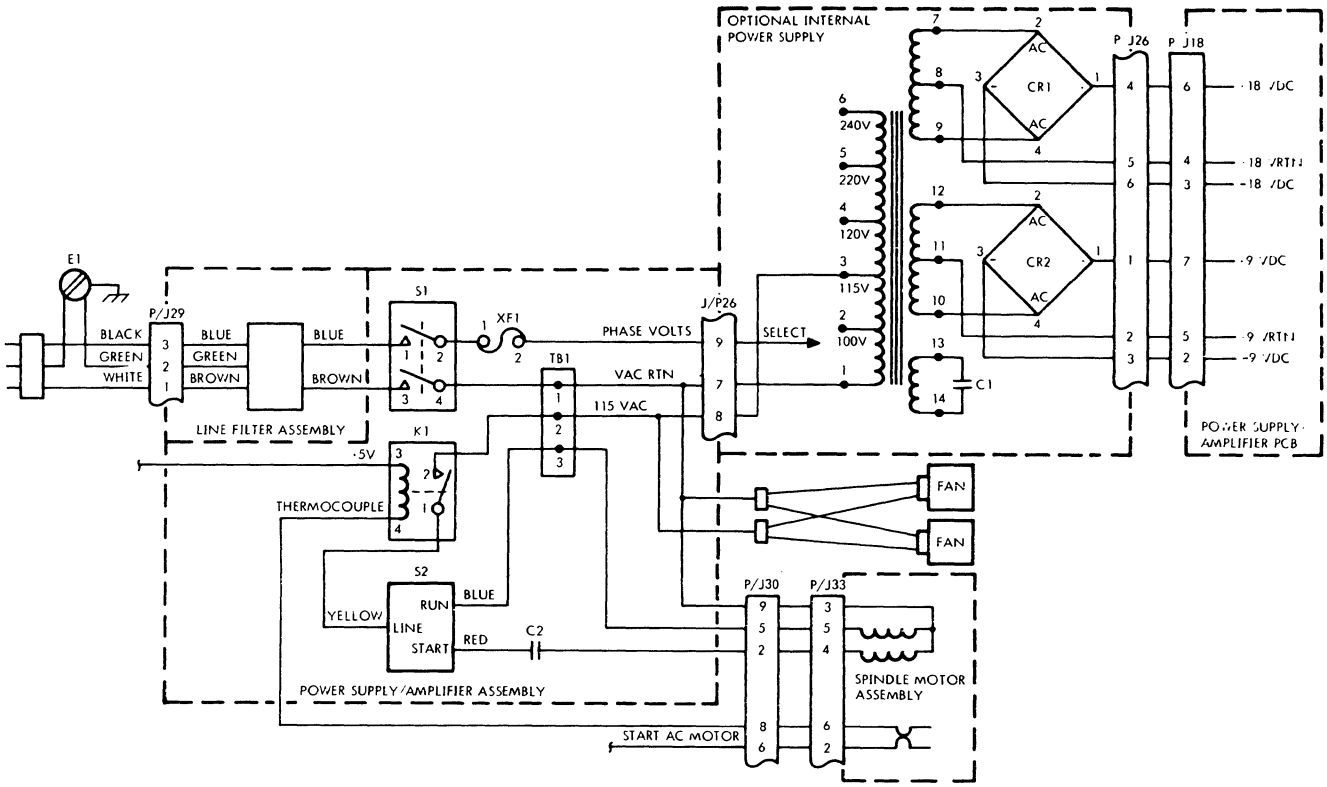


Figure 4-4. Optional Power Configuration and AC Distribution

3. Power Supply/Amplifier PCB

a. Voltage Filtration and Generation

On this PCB the ±18 and ±9 voltages are individually fused and filtered. Each voltage has a minimum filter capacitance of 15,000 microfarad. Thereafter ±18V produce ±12V, while +9V produces +5V. +5 and ±12V are regulated to within ±5 percent. Additionaly, this PCB provides the DC ground reference tie point (E1) for the entire disc drive along with the frame ground tie point (E2) (see Figure 4-5).

b. +5 Volt Overvoltage Protection

In addition to being regulated, the +5V has over-voltage protection. If the emiter of Q7 becomes more positive than its base as controlled by R34, R39, and CR7, then Q7 will turn on and enable the gate to Q5, causing Q5 to turn on. This will clamp +5V to less than +1.5V (see Figure 4-6).

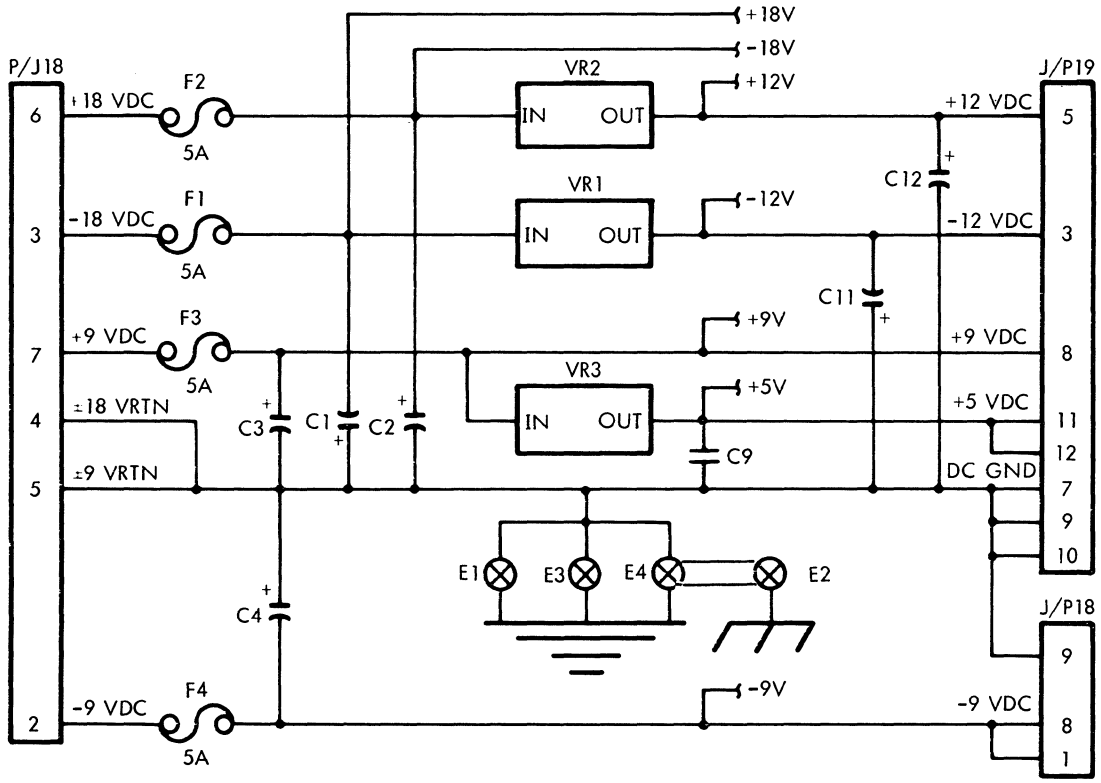


Figure 4-5. Power Supply Filtering and Voltage Generation

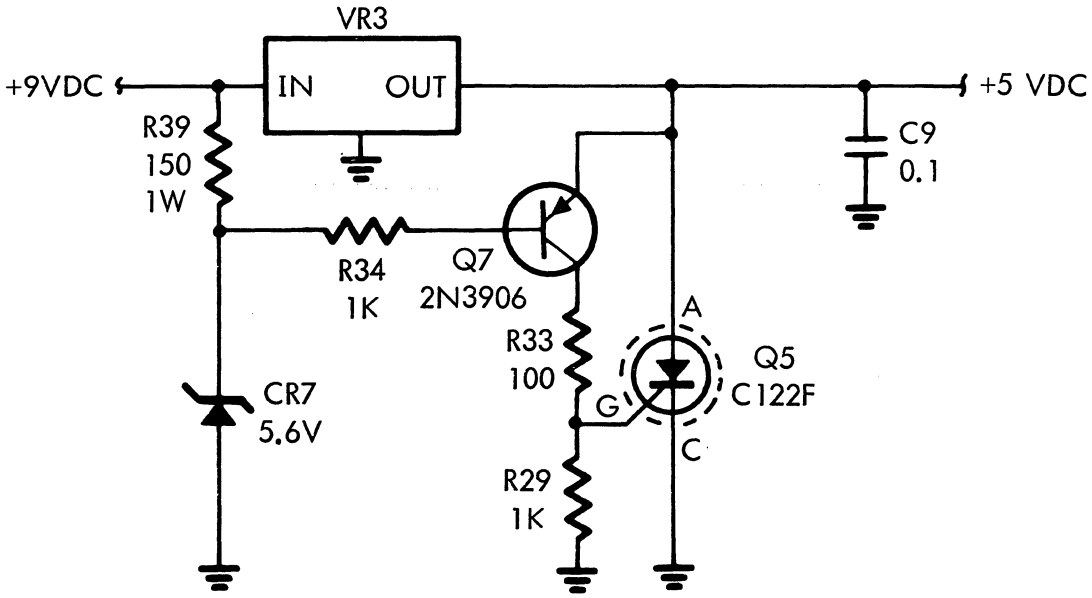


Figure 4-6. +5V Over Voltage Protection

c. Under Voltage Monitor (DCSAFE)

A DC voltage monitor circuit is located on the power supply/amplifier PCB. This circuit monitors the +5, ±9, ±12, and ±18 voltages. If any of these DC voltages fall below a predetermined level, the output of that comparator (U2, U3) goes

low, turning off Q6. This causes the signal DCSAFEAMP/ to go inactive (high), which then turns off the spindle motor, activates the brake, retracts the carriage, and makes the signal FAULT become active.

The under voltage detection level is set at approximately 70-80 percent of the nominal voltage. This is accomplished by establishing a reference voltage supplied by ±9V with dividers R12, R10, and CR2 (+9), and R30 and CR6 (-9). See Figure 4-7.

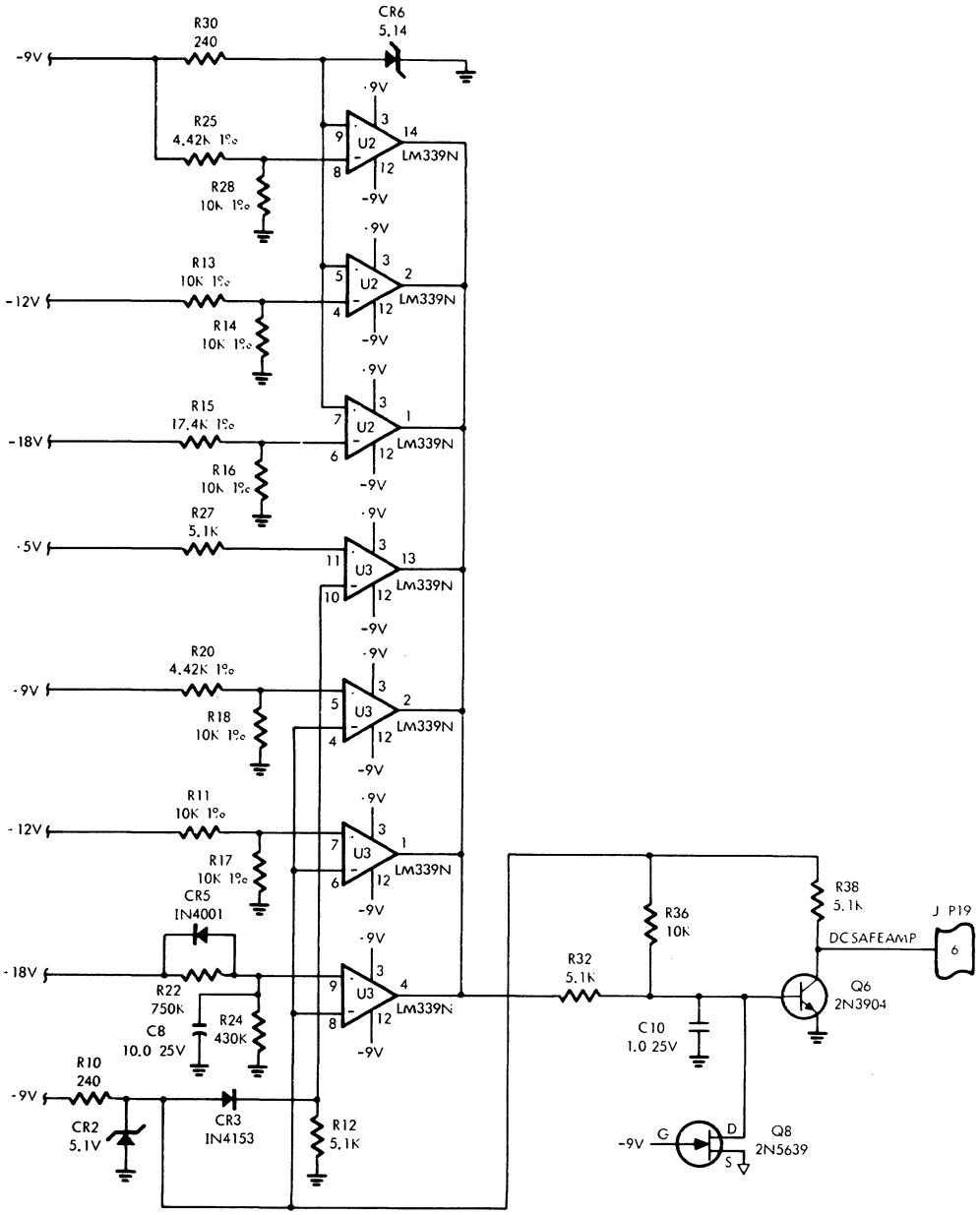


Figure 4-7. Under Voltage Monitor

The input voltages are then attenuated at the input of the comparators so that they are approximately 120 to 130 percent of the reference voltage. The R-C network of C10 and R32 provides a transient noise spike suppresor. This R-C network requires a low output from one or more of the comparators (input voltage is less than reference voltage) for at least 45 μseconds to turn off Q6. Q8 will detect the absence of -9V upon initial power-on.

d. DC Voltage Distribution

The DC voltages are distributed to the using circuits from the power supply/amplifier PCB. There are additional DC voltages generated on the logic/interface, servo, and read/write PCB's. These additional DC voltages are not monitored; therefore, there can be an active DCSAFE signal while missing a required voltage. The voltage distribution is from the power supply/amplifier PCB to the logic/interface PCB. From the logic/interface PCB the voltages are split and distributed to the read/write PCB, the servo PCB, the exerciser, and the LED/switch assembly (operator indicator panel). See Figure 4-8 for voltage distribution. The additional DC voltages are a regulated -5.2V generated from -9V on the logic/interface PCB, a regulated -4V generated from -9V, a regulated -5.2V generated from -9V, regulated +6V generated from +9V, an unregulated +6 VRW generated from +6V, an unregulated $\pm$6.2V generated from $\pm$12V on the read/write PCB, a regulated $\bar{-}$5.2V generated from $\bar{-}$9V, an unregulated $\pm$6.2V generated from $\pm$12V, and an unregulated -8.2V generated from -12V on the servo $\bar{P}$CB.

The user circuits for the voltages are as follows:

+18V	Servo motor current amplifier, brake solenoid pull-in, and carriage lock solenoid pull-in
-18V	Servo motor current amplifier
+12V	Read/write electronics, servo electronics
-12V	Read/write electronics, servo electronics
+9V	Power supply/amplifier PCB, sequence control, generate +6V on read/write PCB, solenoid holding power
-9V	Power supply/amplifier PCB, generate -5.2V on logic/interface PCB, generate -4V on read/write PCB, generate -5.2V on read/write PCB, generate -5.2V on servo PCB
-8.2V	Sealed module
+6.2V	Read/write electronics, servo electronics

-6.2V	Read/write electronics, servo electronics
+6V	Read/write electronics
+6VRW	Sealed module
-5.2V	Input/output interface, read/write electronics, servo electronics, exercisor
+5V	Throughout logic/interface, read/write, and servo PCB's, exercisor, operator indicator panel
-4V	Read/write electronics, sealed module

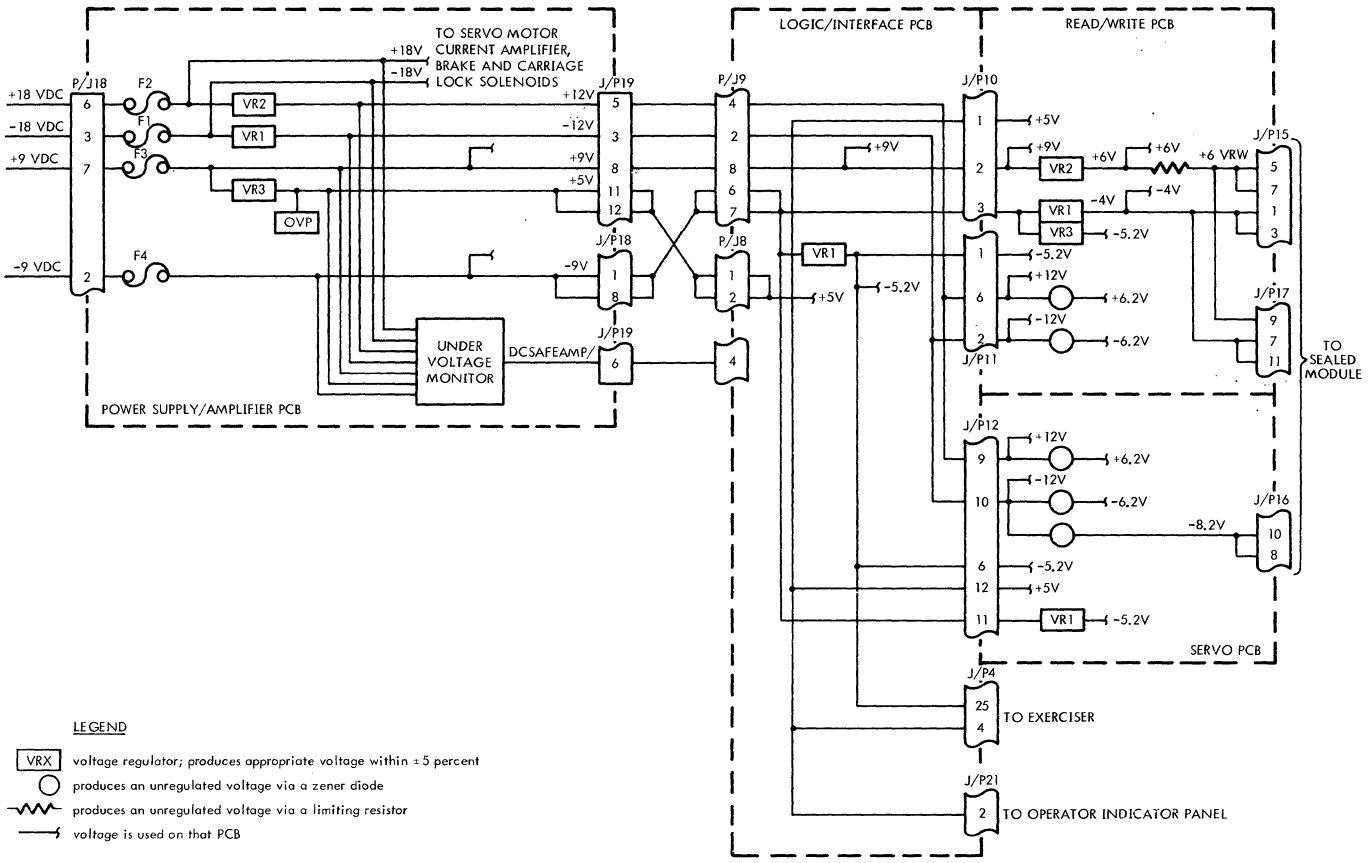


Figure 4-8. DC Voltage Distribution

Input Interface

For the disc drive to function within the data processing system, it is necessary to communicate with the central processing unit (CPU). This communication link is accomplished by a controller communicating with the disc drive (see Figure 4-9).

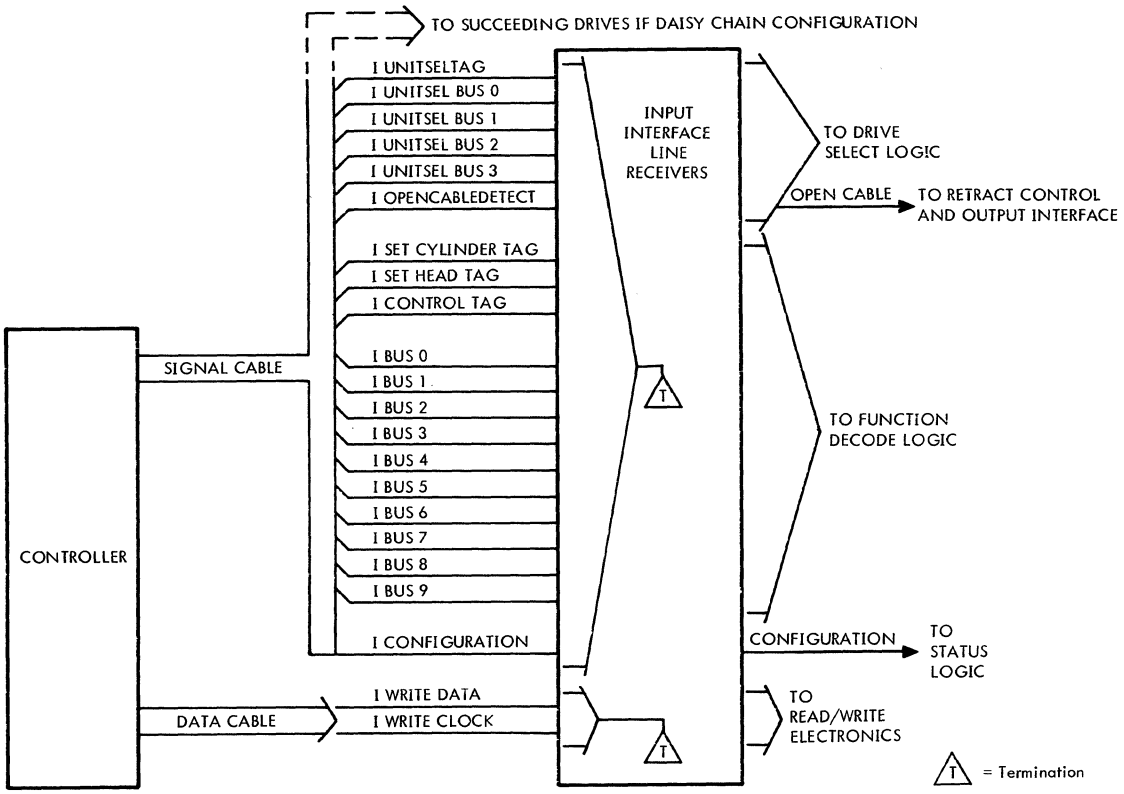


Figure 4-9. Input Interface Cable Connection

Communications between the controller and the disc drive take place in two cables, the signal cable and the data cable. In a daisy-chain configuration, a signal cable is connected from the controller to the first drive and then jumpered (daisy-chained) to succeeding drives in a serial-parallel fashion. The last drive in the daisy-chain string terminates the transmitted signals. In a star configuration, a signal cable is connected directly between each drive and the controller, with each drive terminating the transmitted signals. For the input interface the signal cable carries information that allows a drive to be selected, defines the function it is to perform, and identifies an alternate status request line.

In either configuration (daisy-chain or star) a data cable is connected between each drive and the controller. The data cable carries information for the input interface that is to be stored within the disc drive.

When the controller communicates with a disc drive in a daisy-chain configuration, information is presented to all drives simultaneously. However, in either configuration (daisy-chain or star) the drive will not respond to any information until it becomes selected.

Communication with the disc drive begins when the controller sends information in the signal cable to allow the unit to become selected. These signals are I OPNCBLDET, I UNITSELTAG, and 4 I UNITSEL BUS lines (0-3). The signals are received and sent to the drive select logic. The open cable line also goes to the retract control logic.

Once the unit has been selected, the drive will respond to the three tag signals (I SET CYLINDER TAG, I SET HEAD TAG, and I CONTROL TAG), the ten bus signals (I BUS 0-9) and the I CONFIGURATION signal. These signals are sent to the function decode logic to determine what the drive is supposed to do. The configuration signal is sent to the status logic to allow the drive to transmit alternate status.

The signals in the data cable (I WRITE DATA and I WRITE CLOCK) are responded to only after the drive has been selected and the function decode logic has decided that the drive is to perform a write function. These signals are sent to the read/write electronics.

The input interface (Figure 4-10) is comprised of the input line receivers. These are differential receivers with at least ±100mV sensitivity and ±3V common mode rejection. Attached to the front of the receivers is a termination of 56 ohms to ground for each line within the signal cable. The input signals in the data cable are terminated with 62 ohms to ground for each line.

There is a unique exception to the above in that the receiver for I OPNCBLDET has at least ±25mV sensitivity and a special termination (see Section 2).

The receiver outputs are such that when the + input is more positive than the - input, the output will be greater than 2.7V. With + input more negative than the - input, the output will be less than 0.4V.

Drive Selection

To communicate with the disc drive, it is necessary for the controller to select the drive. Selection is accomplished by the signal OPENCABLE/ being inactive and the controller sending the appropriate unit select information to the drive via the signal cable.

OPENCABLE/ is made inactive when a signal cable is connected between the drive and the controller, and the drive's line receiver receives the proper polarity signals (/IOPNCBLDET and /IOPNCBLDET/) from the controller.

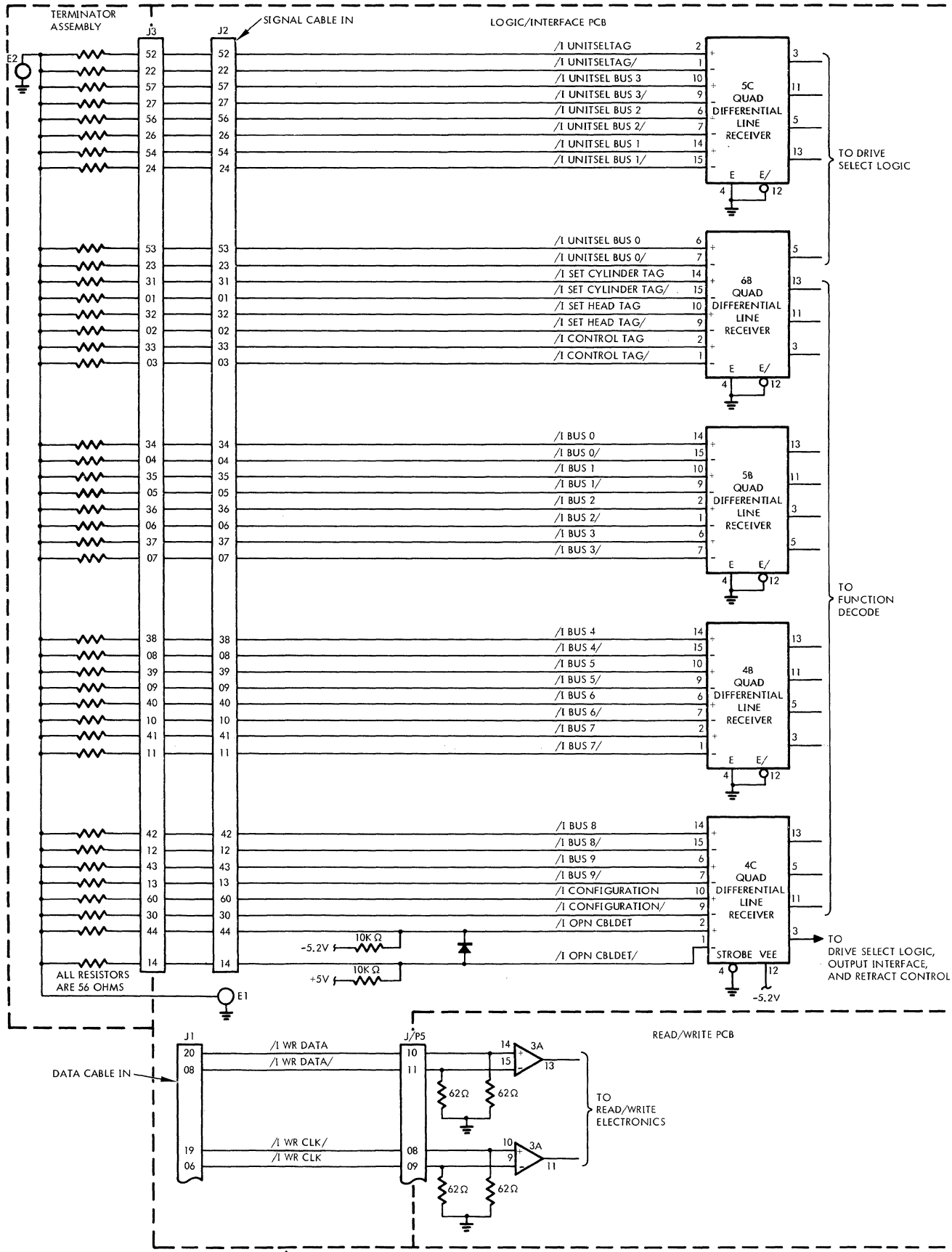


Figure 4-10. Input Interface Logic

The unit select information are binary coded signals (I UNITSEL BUS 0-3) and a strobe signal (I UNITSELTAG). The binary coded information, transmitted by the controller, is compared with the unit select switches in the drive. When there is a comparison, the drive generates a unit selected signal.

The unit select switches are located in dip switch S1 on the logic/interface PCB. There is a total of four switches (S1-1, -2, -3, -4) which allow for addresses 0 through 15 decimal (0 through F hexadecimal). The switch settings and unit select bus states are shown in Table 4-1 for selection of a given unit address.

TABLE 4-1

DRIVE SELECTION SWITCH SETTINGS

	SWITCH S1				I UNIT SEL BUS			
	-1	-2	-3	-4	3	2	1	0
Unit 0	0	0	0	0	0	0	0	0
Unit 1	0	0	0	1	0	0	0	1
Unit 2	0	0	1	0	0	0	1	0
Unit 3	0	0	1	1	0	0	1	1
Unit 4	0	1	0	0	0	1	0	0
Unit 5	0	1	0	1	0	1	0	1
Unit 6	0	1	1	0	0	1	1	0
Unit 7	0	1	1	1	0	1	1	1
Unit 9	1	0	0	0	1	0	0	0
Unit 9	1	0	0	1	1	0	0	1
Unit 10	1	0	1	0	1	0	1	0
Unit 11	1	0	1	1	1	0	1	1
Unit 12	1	1	0	0	1	1	0	0
Unit 13	1	1	0	1	1	1	0	1
Unit 14	1	1	1	0	1	1	1	0
Unit 15	1	1	1	1	1	1	1	1

Switch setting 1 = Switch open (off, inactive)

Switch setting 0 = Switch closed (on, active)

I UNIT SEL BUS = 1 indicates active condition.

To accomplish selection it is necessary for the unit select buses (/I UNITSEL BUS 0-3) to be active 200 nanoseconds prior to the strobe (/I UNITSELTAG). This is to allow the unit select buses to be compared with the unit select switches and produce a stable comparison signal to the unit selected flip-flop prior to the arrival of the strobe.

The comparison takes place in a 4-bit comparator that has to have its "A" inputs equal to its "B" inputs in order to produce an active output for unit selection purposes. The "A" inputs are the unit select bus bits from the drive's line receivers. The "B" inputs are the unit select switches. The "B" inputs are pulled up by pull-up resistors when the switches are off, and are grounded when the switches are closed.

Once the unit has been selected (UNITSELD active), the unit select buses can go inactive (different state than the switches). However, UNITSELTAG must remain active during the entire time that communication with the drive is desired.

The unit selected flip-flop produces outputs UNITSELD, UNITSELDB, and UNITSELD/. UNITSELD/ creates the signal multiplexer enable (MUXENBL/) that enables the function decode logic to allow further communication between the disc drive and the controller. UNITSELDB is for the disc drive exerciser. UNITSELD enables the following:

(1) /I UNITSELECTED is transmitted to the controller.

(2) Transmit enable (XMITENBL) is generated to enable the output interface for the signal cable.

(3) Sequence enable (SEQENBL) is generated.

As shown in Figure 4-11, the unit select bus bits (UNITSEL BUS 0-3) come into the "A" inputs of a 4-bit comparator (6C). The unit select switch lines are presented to the "B" inputs of the comparator. When there is a comparison of the "A" and "B" inputs, the A=B ouput becomes active (high). The A=B line provides the data input to the "D" flip-flop (13D). When the UNITSEL TAG becomes active it will clock the data input to the Q output, provided OPENCABLE/ is not active. Assuming there was an address match, the "D" flip-flop will now have active outputs. This will allow the drive to sequence up, decode the appropriate functions as commanded from the controller, send a unit selected (/UNITSELECTED) signal to the controller via the data cable, and enable the line drivers for the signal cable, permitting the drive to transmit status to the controller.

Once selected, the drive will remain selected until either OPENCABLE/ becomes active (14C) or UNITSEL TAG becomes inactive (15B, 14D, and 14C).

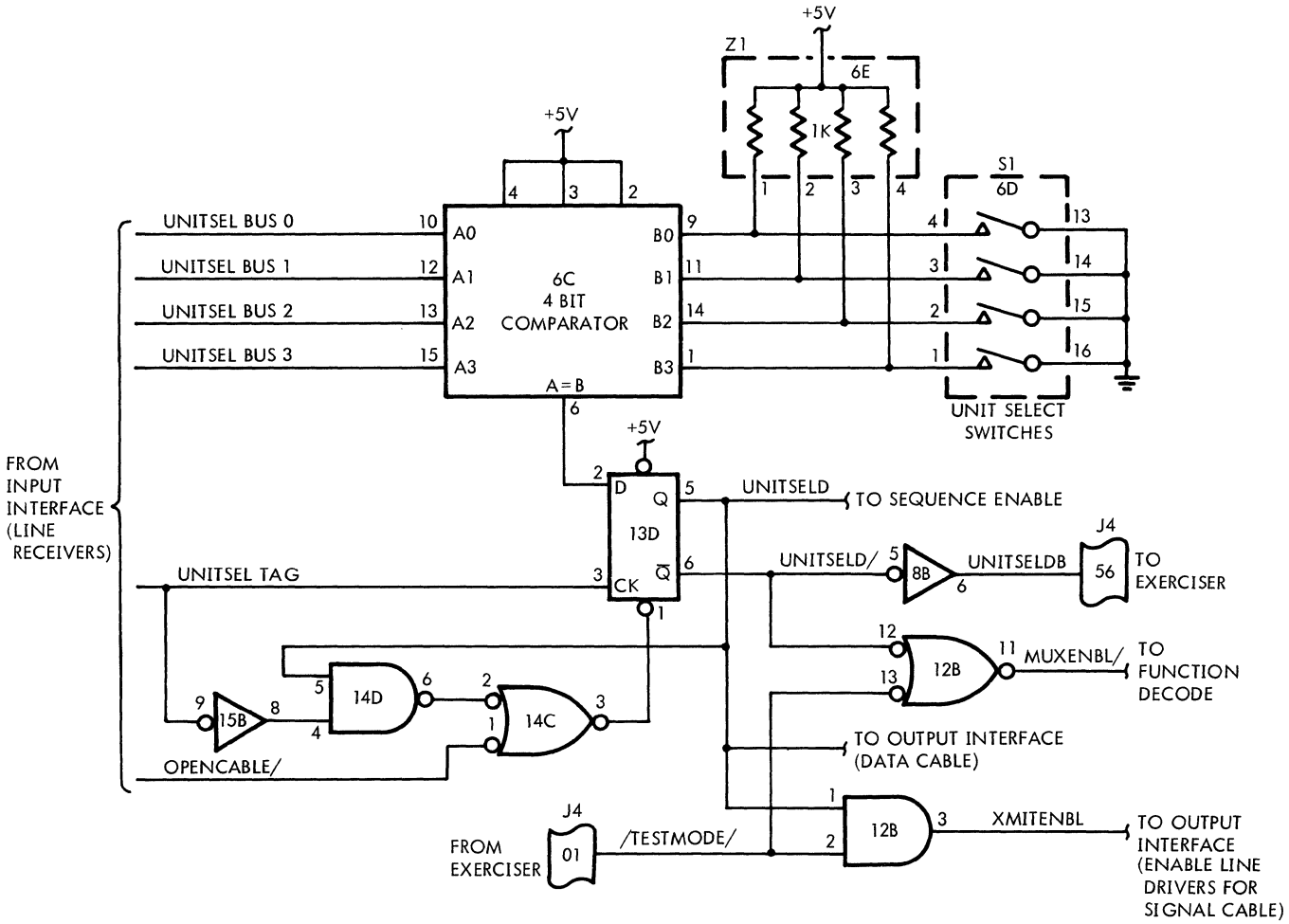


Figure 4-11. Drive Selection Logic

Sequencing

The sequencing circuits provide the means of sequentially controlling the power-up and power-down functions. The main objectives of the sequencing circuits are to:

- Establish and monitor conditions during a power-up cycle to allow the discs to spin and the heads to load, ending with a READY status.
- Unload the heads from the data recording area, lock the carriage in place, and stop the discs from spinning.

The sequencing circuits control power application to the spindle motor, the brake assembly solenoid, and the carriage lock solenoid. Circuits are provided to:

- Initialize certain logic functions.
- Deactivate/activate the spindle brake solenoid.
- Start and maintain the spindle motor rotation.
- Monitor the disc rotational speed.
- Deactivate/activate the carriage lock solenoid.
- Load/unload the heads.
- Ensure a timely sequence up via a 30-second monitor.
- Establish conditions for positioning system to position the heads at cylinder 0 and allow the status logic to report READY status.

The sequencing circuits have two major elements; sequence enable and sequence control.

1. Sequence Enable

As shown in Figure 4-12, sequence enable (SEQENBL) can be made active by three different methods. However, regardless of the method activating sequence enable, DC SAFE must be active to maintain sequence enable. The three methods are:

S3-6 closed, providing a direct set (14E) to the sequence enable flip-flop (15C). This allows sequence enable when the drive is a stand-alone unit.

The exerciser connected to the drive (14E) and the exerciser turned on.

Unit selection from the controller (15C).

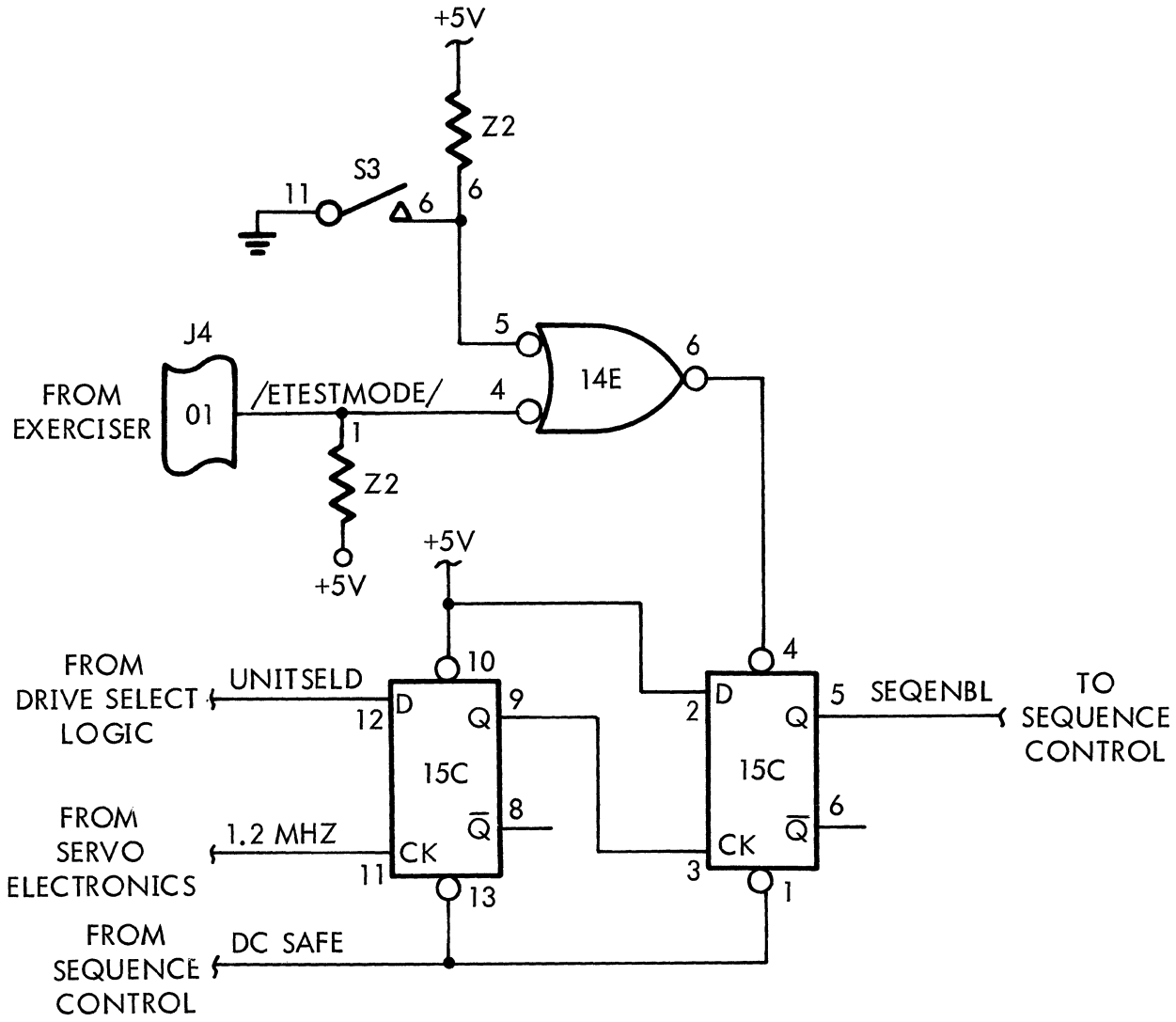


Figure 4-12. Sequence Enable

Switch S3-6 should be used only when the drive is in a stand alone unit configuration. S3-6 open will allow the selection method from the controller, thereby having the controller enable sequence up. Once sequence enable has been established, it will remain active until DC SAFE becomes inactive. Sequence enable goes to the sequence control circuit to allow a sequence up operation.

2. Sequence Control

Figure 4-13 presents a general block diagram of sequence control. The sequence control circuits enable the spindle motor, the spindle brake solenoid, the carriage lock solenoid, and whether or not the servo motor current is controlled by the servo electronics. Upon power-on, these control circuits initialize the drive's logic. Besides controlling the flow for a sequence up operation, the control circuits also contain the necessary monitor logic to sequence down the drive. Once the drive has sequenced up properly, the circuits monitor for an unsafe voltage, unsafe speed, or an active spindle brake. If the monitor detects any such condition, the spindle motor is turned off, the heads are retracted, the spindle brake is activated, and the carriage lock is activated.

A sequence up operation begins when power is applied to the disc drive. When all of the DC voltages on the power supply/amplifier PCB are above the tolerance level of the under-voltage monitor, the monitor produces the signal DCSAFEAMP/. This signal is then applied to the sequence control circuits on the logic/interface PCB where the signals DCSAFE, DCSAFE/, and DCSAFEDLYD are produced.

a. DCSAFE

As shown in Figure 4-14, DCSAFEAMP/ being active turns off transistor Q3. This disables the leg to the dot OR function for retract heads (RETHDS/) and allows gate 7F-12 to control the signal RETHDS/. DCSAFEAMP/ also produces DCSAFE through gate 1D2.

DCSAFE becoming active removes the direct set from the power initialize flip-flop (PWRINI). It provides one leg (2D1) of input to the monitor for resetting the start motor flip-flop (STRMTR F/F) if DCSAFE becomes inactive. DCSAFE goes to the sequence enable logic to allow sequence enable (SEQENBL) to become active and provide the signal DCSAFE to the exerciser (J4-14). It also produces the signal DCSAFE/ through gate 1D4.

DCSAFE/ is an input to the fault logic, which will produce a FAULT signal if DCSAFE/ becomes inactive. This signal also provides the input to the R-C network C3 and R12, which produces the signal DC safe delayed (DCSAFEDLYD). The R-C network provides a delay of 8 $\pm$3 microseconds.

DCSAFEDLYD active provides one leg of input to AND gate 3E3 to be ANDed with SEQENBL to clock the start motor flip-flop.

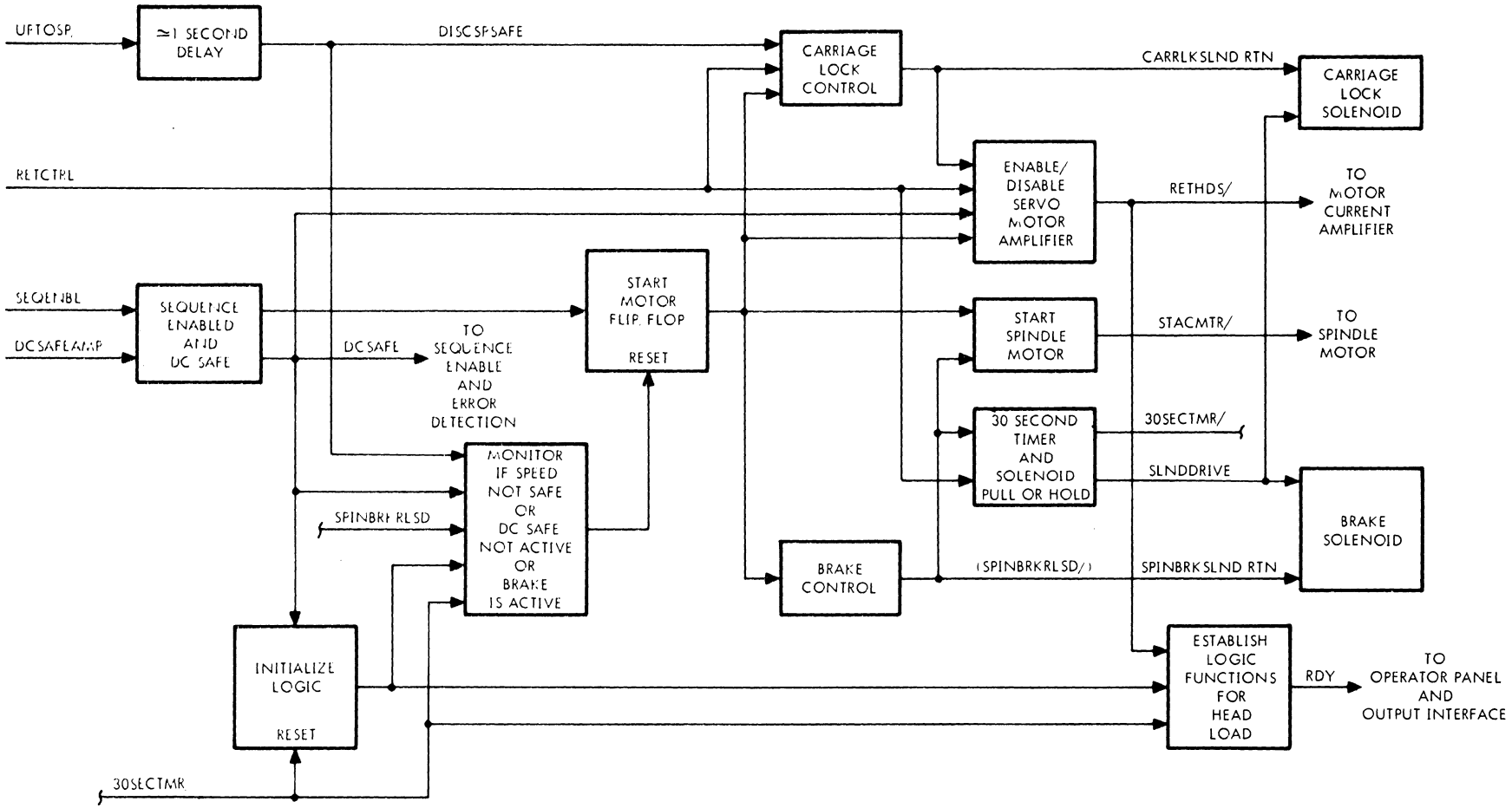


Figure 4-13. Sequence Control General Block Diagram

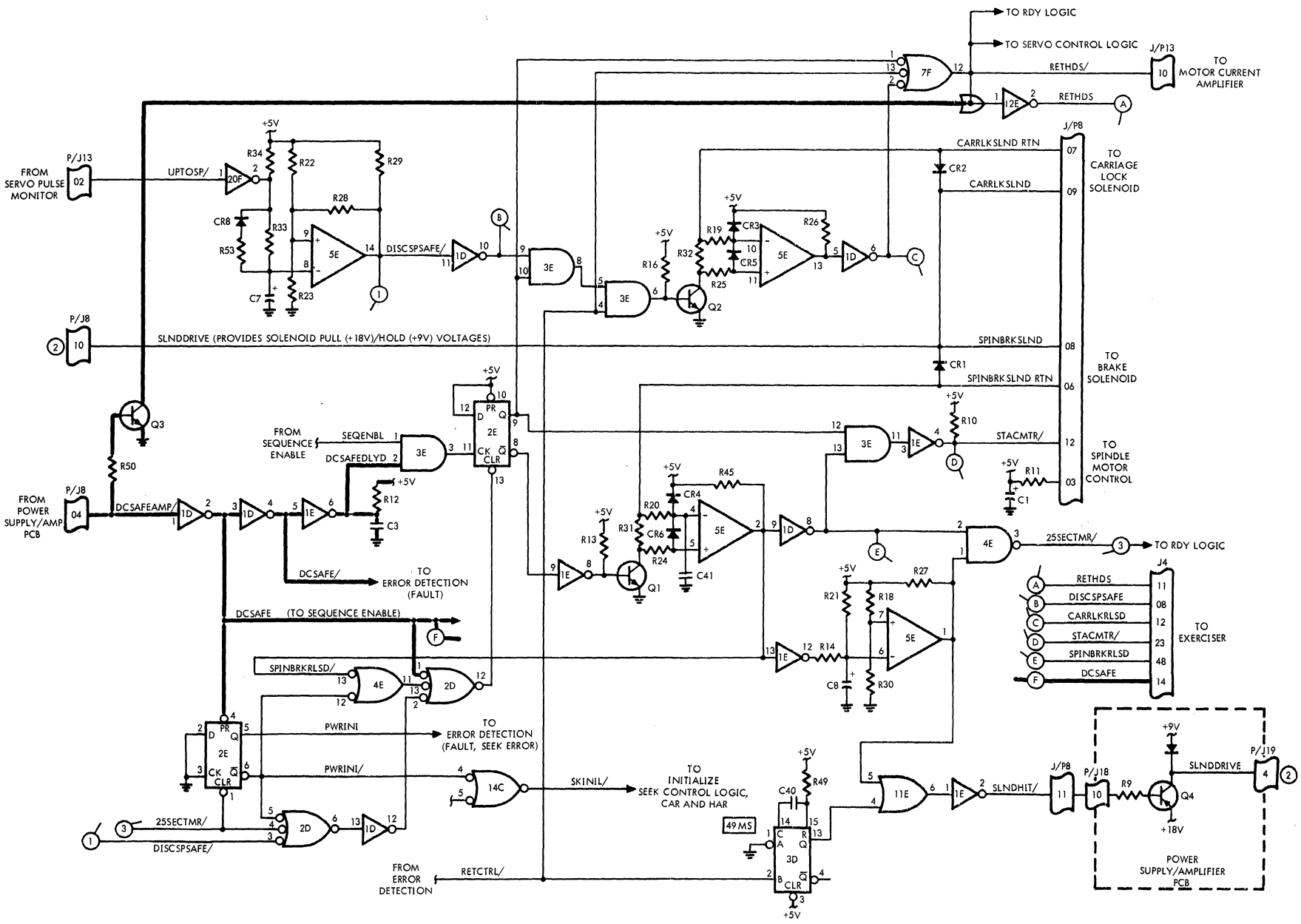


Figure 4-14. Sequence Control Initialization

b. PWRINI

The logic initialization signal is power initialize (PWRINI, PWRINI/). These signals are generated from one D flip-flop (2E) on the logic/interface PCB. As soon as +5V becomes stable, the flip-flop will set, since DCSAFE requires all DC voltages to be stable for at least two seconds before it becomes active. The flip-flop being set generates the active signals PWRINI and PWRINI/. These signals will remain active until the signal 25-second timer (25SECTMR/) becomes active.

While active, PWRINI causes a reset to the FAULT and SEEK ERROR Logic. PWRINI/ goes to gate 14C4 and produces the signal seek initialize (SKINIL/), which in turn resets CAR, HAR and initializes the seek control logic (no SETDIF, no SETCAR, no SKSTRT, ODD reset, direction reset, ST0 active, and ST1, ST2, ST3 inactive).

In addition, PWRINI/ disables two legs of the STACMTR F/F monitor. This disable remains active until 25 SECTMR/ becomes active, which resets the PWRINI F/F. At the time the spindle is released (SPINBRKRLSD/), the 25 SECTMR/ is generated (see Figure 4-15).

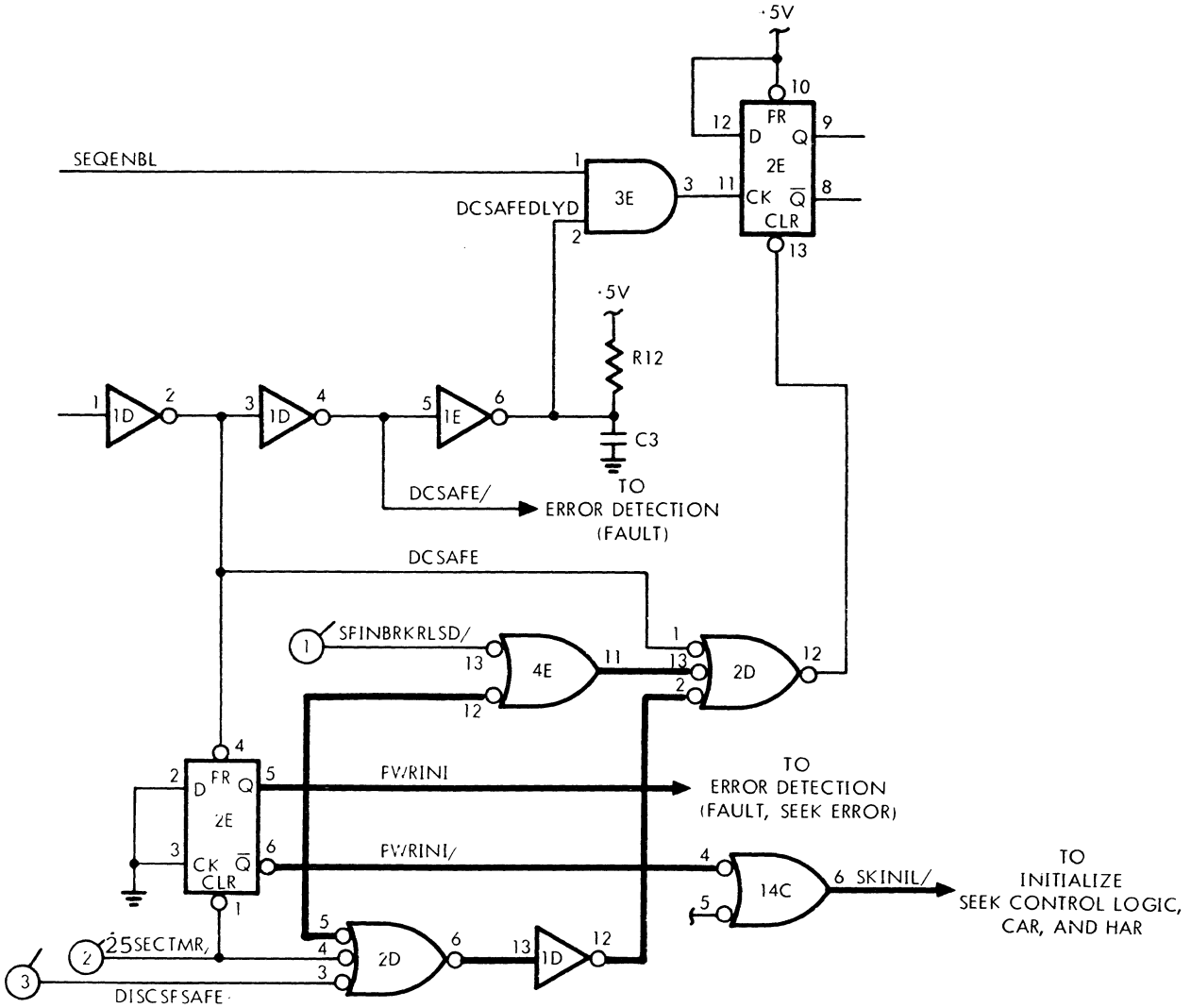


Figure 4-15. Logic Initialization

c. SEQENBL

Now that the logic is initialized and DCSAFE is active, DCSAFEDYLD is ANDed with sequence enable (SEQENBL) through AND gate 3E3 to clock the STR MTR F/F active.

d. Energizing the Spindle Motor

With the STR MTR F/F active, the spindle brake will be released (SPINBRKRLSD), the spindle motor started (STACMTR/), a 30-second timer (25 SECTMR/) will be activated to monitor the disc speed becoming safe (DISCSPSAFE) in the appropriate time. This will change the voltage to the brake and carriage lock solenoids. Figure 4-16 shows the start motor flip-flop outputs going to (1) transistor Q1 to release the spindle brake, (2) to one leg of AND gate 3E11 to start the spindle motor when the spindle brake is released (SPINBRKRLSD active), (3) to disable one leg of OR gate 7F16, (4) to disable retract heads (RETHDS/) when the carriage lock is released, and (5) to one leg of AND gate 3E8 to release the carriage lock when the disc speed is safe (DISCSPSAFE active) and retract control (RETCTRL/) is inactive.

Once the spindle motor flip-flop is set, it remains set until one of four possible things happen: (1) DCSAFE goes inactive (2D1), (2) SPINBRKRLSD/ goes inactive after PWRINI/ has gone inactive (2D13), (3) the disc speed does not become safe within the 25 second timer or (4) DISCSPSAFE/ has become active, then goes inactive (2D2).

3. Spindle Brake Released (SPINBRKRLSD)

As shown in Figure 4-17, transistor Q1 turning on will cause a voltage drop across R31 so that comparator 5E4 input will have a more positive voltage than input 5E5. The comparator will output a low indicating spindle brake released (SPINBRKRLSD/) which starts a 25-second timer. The spindle brake return line being activated by Q1 will energize the brake solenoid with the voltage side of the solenoid having +18V as long as solenoid hit (SLNDHIT/) is active. The +18V is used to pull the solenoid and when SLNDHIT/ goes inactive the solenoid drive voltage (SLNDRIVE) goes to +9V to hold the solenoid. When the solenoid is activated, it releases the brake disc, which will allow the spindle to turn. SPINBRKRLSD ANDed with the STR MTR F/F through gate 3E11 will now start the spindle motor. As long as SPINBRKRLSD/ remains active, it will disable one leg of monitor input to the STRMTR F/F.

f. Solenoid Activated (Released)

The disc brake assembly is of a fail safe type, in that it requires some positive affirmative action to energize the solenoid to release the brake. The solenoid is energized and held on by a dual voltage level circuit as shown in Figure 4-18.

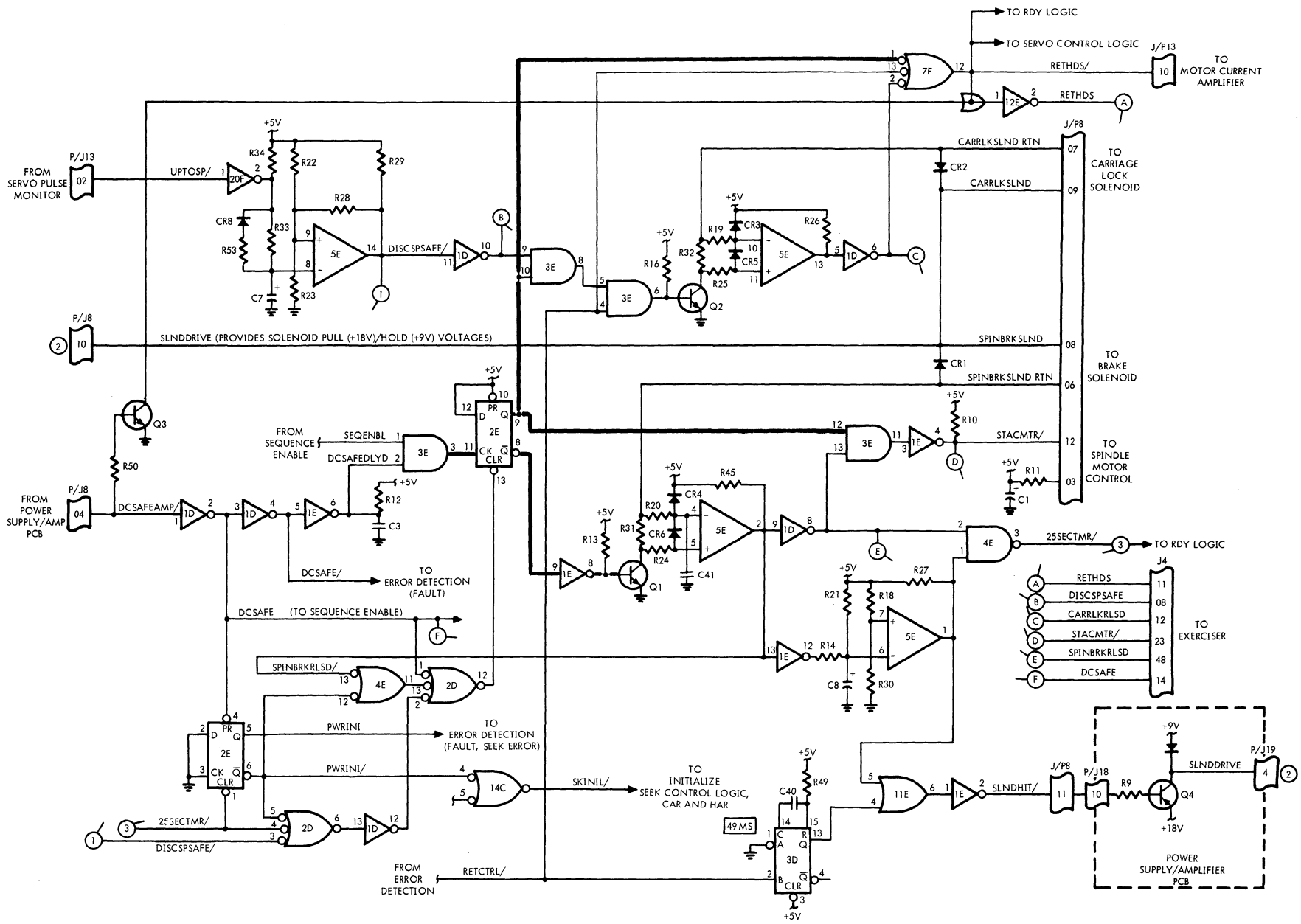


Figure 4-16. Spindle Motor Flip-Flop Active

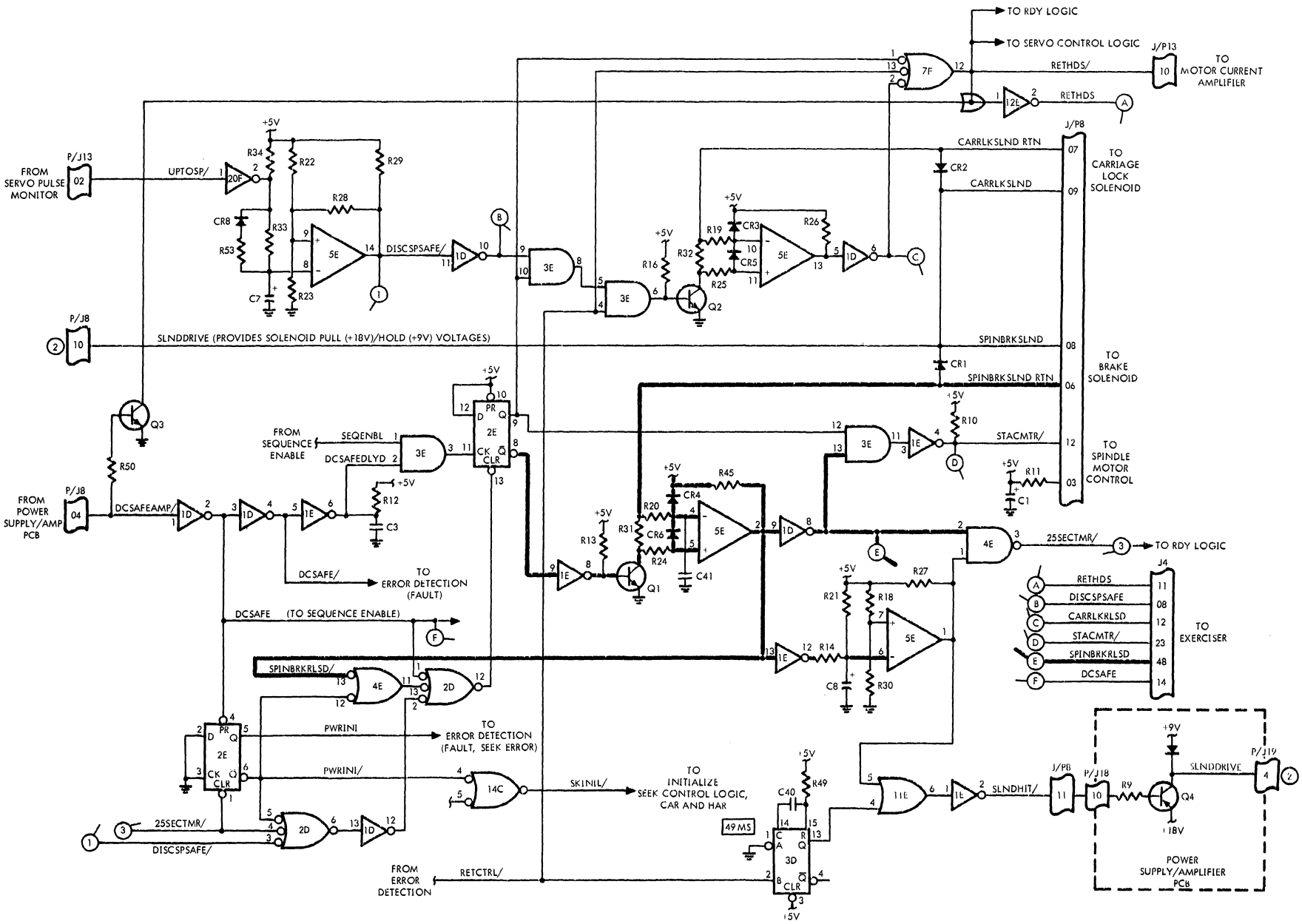


Figure 4-17. Spindle Brake Released

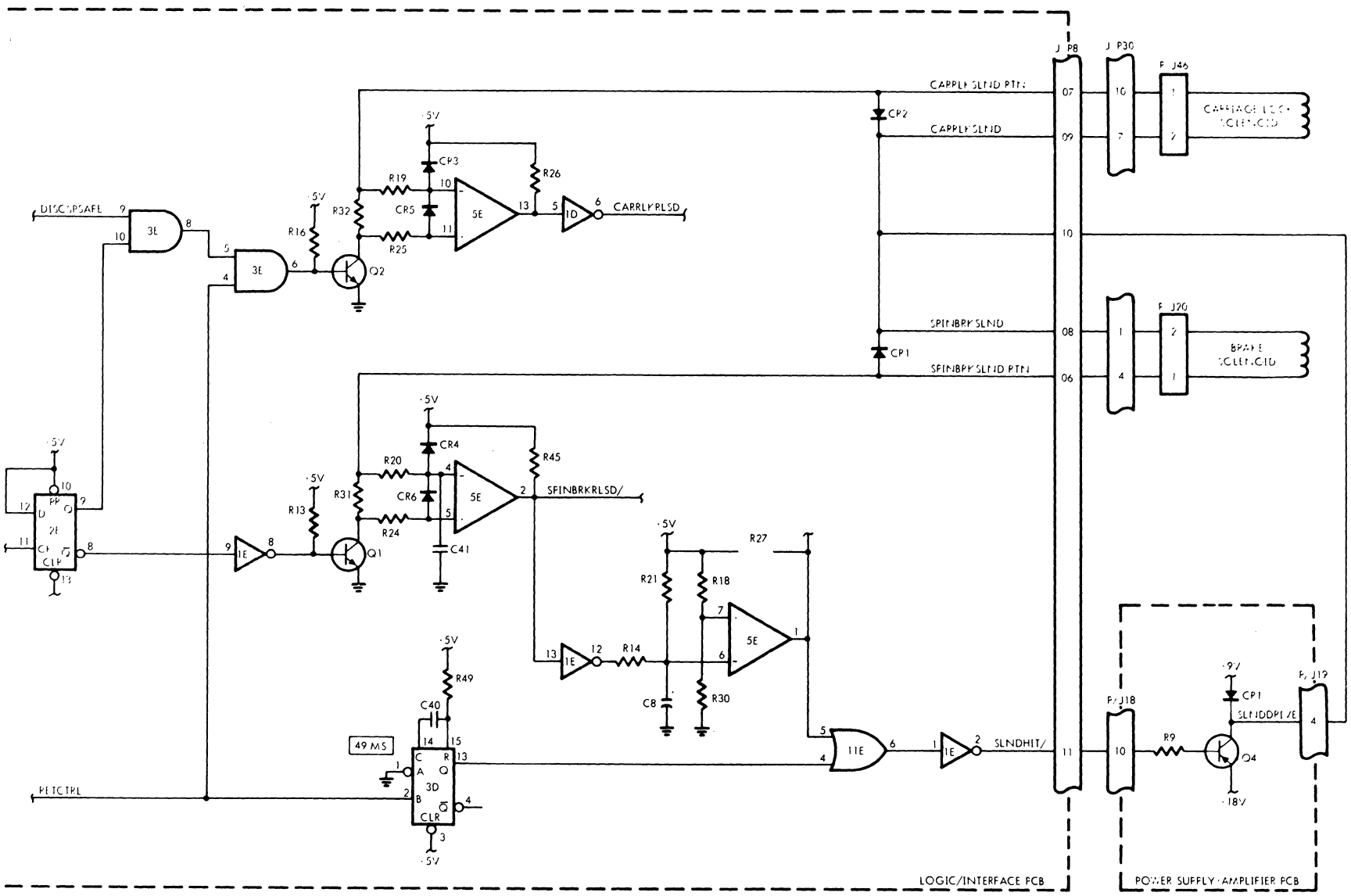


Figure 4-18. Solenoid Drive

Upon initial power-on, the signal SLNDHIT/ is active and remains active until the 30-second timer has been activated and timed out. With SLNDHIT/ active, Q4 on the power supply/amplifier PCB is turned on and provides +18V as the signal solenoid drive (SLNDDRIVE). SLNDDRIVE supplies both the brake and carriage lock solenoids. The +18V acts as a pull voltage to the solenoids and will allow the solenoids to activate as soon as the solenoid return lines (SPINBRKSLND RTN and CARRLKSLND RTN) are enabled through the turn on of transistors Q1 and Q2 respectively. After the 30-second timer times out, SLNDHIT/ becomes inactive, turning off Q4 which then drops the SLNDDRIVE signal to +9V through CR1. +9V acts as a holding voltage for the solenoids (see Figure 4-18). 18).

An alternate method of providing the solenoid pull voltage (SLNDDRIVE = +18V) is made possible for recovering from an error condition that caused retract control (RETCTRL/) to become active. This alternate method is to allow program recovery through a restore operation, rather than requiring operator intervention of a power off-on cycle. An error condition that activates RETCTRL/ will drop the carriage lock solenoid and lock the carriage in the retract position. This happens due to AND gate 3E6 being disabled, thereby turning off Q2 which disables the carriage lock solenoid return line. To recover from this under program control, if a restore operation is executed, RETCTRL/ will become inactive. This will enable AND gate 3E6, which in turn provides a return path for the carriage lock solenoid by turning on Q2. However, to unlock the solenoid it is necessary to provide the solenoid pull voltage (SLNDDRIVE = +18V). This is accomplished by RETCTRL/ going inactive, which triggers the one-shot 3D13 whose active output goes through OR gate 11E6 to generate an active SLNDHIT/ signal. This then turns on Q4 to provide +18V (see Figure 4-18).

g. 25-Second Timer

The 25-second timer is controlled by R-C network C8 and R21, voltage divider R18 and R30, comparator 5E and AND gate 4E3. 25-second timer (25SECTMR/) becomes active as soon as SPINBRKRLSD becomes active. 25 SECTMR/ remains active until C8 charges to a voltage level that is greater than the voltage level at 5E7 as supplied from voltage divider R18 and R30. When 5E6 is more positive than 5E7, the comparator will output a low and disable the leg to 4E1, thereby making 25 SECTMR/ inactive. This will also make the signal SLNDHIT/ inactive through 1E1.

When 25 SECTMR/ is active, it is used to reset the power initialize flip-flop, disable the ready signal and act as a monitor for DISCSPSAFE/ to become active before 25 SECTMR/ becomes inactive (reference Figure 4-17).

h. Start AC Motor (STACMTR/)

As shown in Figure 4-19, with both START MTR F/F and SPINBRKRLSD active, start AC motor (STACMTR/) is generated by gate 3E through inverter 1E. STACMTR/ in turn goes to the spindle motor thermocouple, and when the thermocouple is closed (motor not overheated) it goes through the thermocouple to solid state relay (SSR) K1 on the power supply/amplifier assembly. With SSR K1 energized, 115 VAC is supplied to switch S2, which in turn supplies 115 VAC to the spindle motor through both the run winding and the start winding as capacitor C2 provides phase correction. With both motor windings energized, the motor accelerates up to speed. As the current in the start winding decreases, the switch S2 will disconnect the start winding. This leaves the run winding to maintain the operating speed of the motor, with the motor torque being transmitted to the spindle through pulleys and a belt, which in turn spins the discs inside the sealed module.

i. Up-To-Speed

With the discs rotating, the signal up to speed (UPTOSP/) is generated by the servo pulse monitor in the positioning system. This signal is active, whenever the discs are rotating at greater than 70 percent of nominal speed. As shown in Figure 4-20, UPTOSP/ generates disc speed safe (DISCSPSAFE/) through delay circuit 20F2, 5E14, C7, CR8, R22, R23, R28, R29, R33, and R34.

Inverter 20F2 provides a high active signal to the R-C network of R33, R34, and C7. This R-C network provides an approximately one-second delay to insure a stable input to the comparator 5E14. Diode CR8 and R53 provide a rapid discharge path for capacitor C7. This ensures a complete sequence down cycle in the event of momentary losses of UPTOSP/. When the input to the comparator from the R-C network is more positive than the input provided by the voltage divider R22 and R23, DISCSPSAFE/ becomes active.

With DISCSPSAFE/ active the final leg to the START MTR F/F reset monitor is provided and the signal 30SECTMR/ can now become inactive without causing the START MTR F/F to be reset. The second leg of AND gate 3E8 is also satisfied and ANDed with START MTR F/F to provide an active signal to AND gate 3E6. If the second leg of this AND gate is satisfied by RETCTRL/ being inactive, the carriage lock solenoid (CARRLKSLND) can be energized.

The carriage lock solenoid is energized by turning on Q2, which supplies an active return path (CARRLKSLND RTN). The voltage to the solenoid is supplied from SLNDDRIVE by the signal CARRLKSLND (reference Figure 4-18). With the solenoid energized the carriage is free to be controlled by the servo (linear) motor of the positioning system.

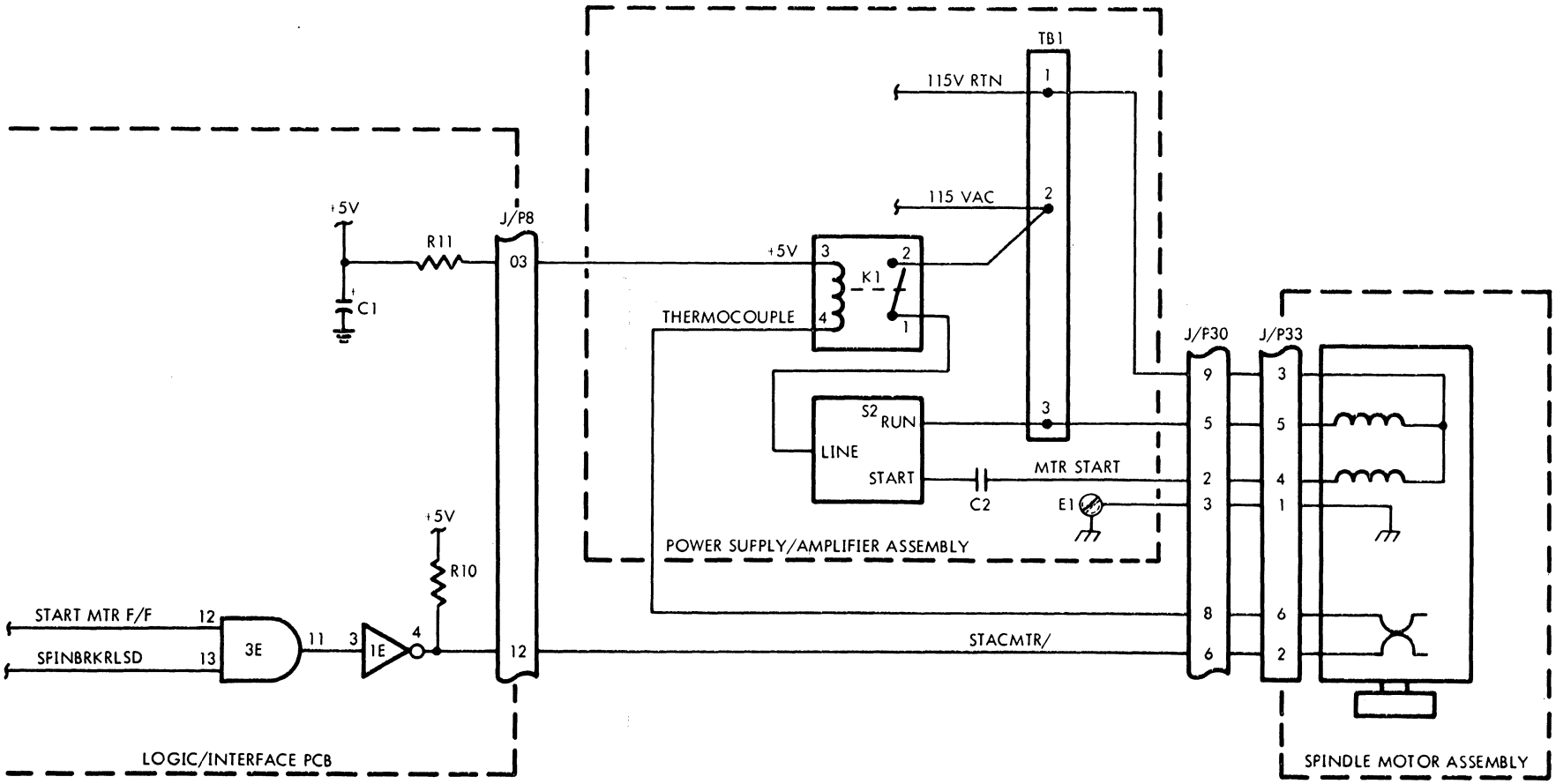


Figure 4-19. Spindle Motor Control

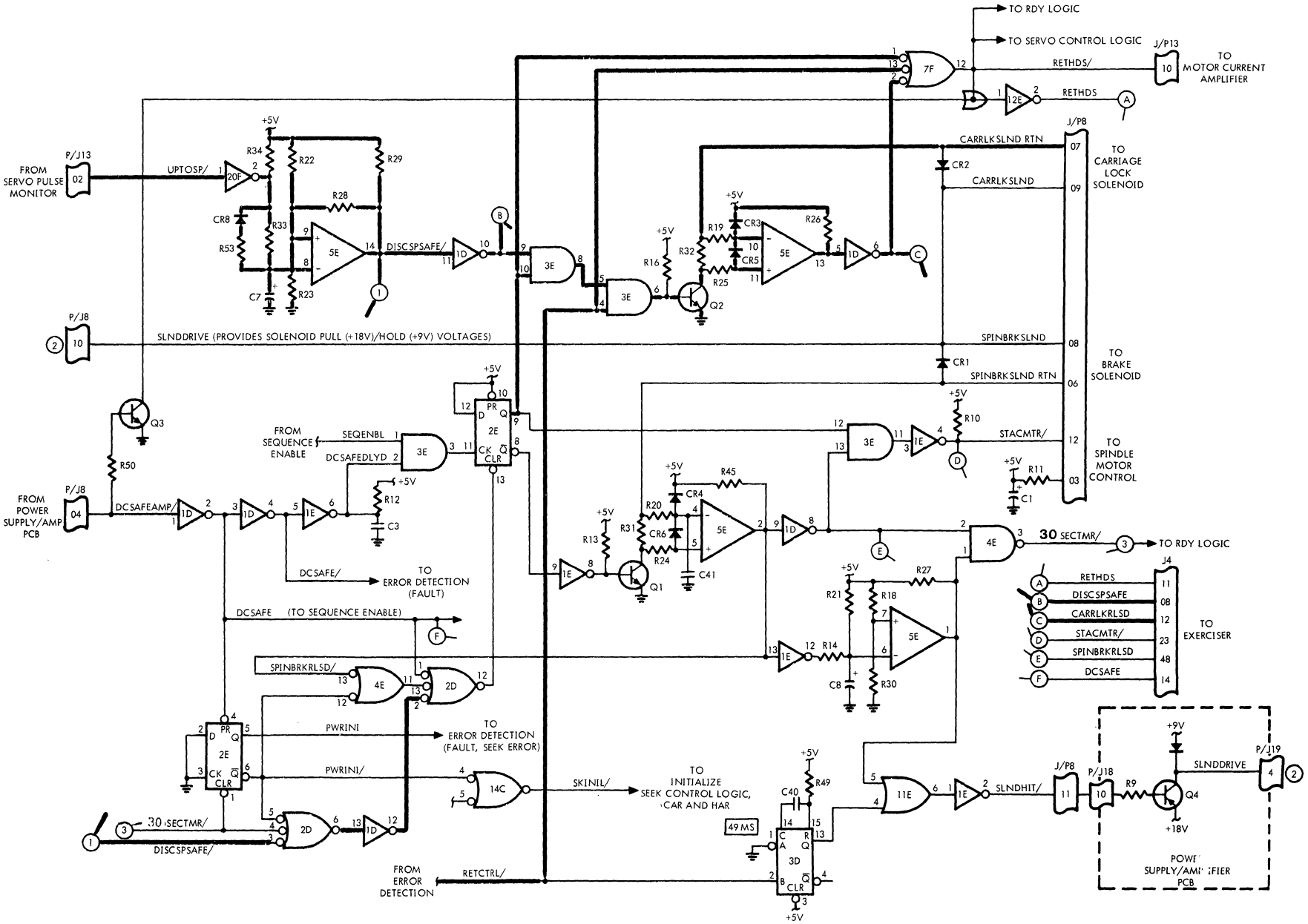


Figure 4-20. Disc Speed Safe/Carriage Unlocked

As current runs through R32, the voltage drop created causes comparator 5E13 to output a low signal. This will be inverted by 1D6 to provide an active signal carriage lock released (CARRLKRLSD). CARRLKRLSD active, blocks one leg to OR gate 7F12 to disable retract heads (RETHDS/).

j. Disable Retract Heads (RETHDS/)

When this signal is active, it disables the servo motor current amplifier from the servo electronics input. With the motor current amplifier under control of RETHDS/, the heads are driven away from (retracted) the recording surface to the outer guard band (OGB).

As shown in Figure 4-21, RETHDS/ is inactive when DCSAFE, START MTR F/F, and CARRLKRLSD are active and retract control (RETCTRL/) is inactive.

RETCTRL/ is a signal generated by the error detection logic whenever OPENCABLE/ is active or a seek error is generated by a motion command (seek or restore) that takes more than 1.5 seconds to complete. During a sequence up operation, the 1.5 second timer has no effect as PWRINI is active for greater than 1.5 seconds and this will reset the error flip-flop before the spindle motor is activated.

With RETHDS/ inactive, field effects transistor (FET) 6A15 is disabled while FET 6A10 is enabled by transistor Q4 being turned on. This allows the servo motor current amplifier to be controlled by the servo electronics as commanded by the servo control logic.

k. Servo Control Logic (Sequence Up)

Figure 4-22 presents the servo control logic for a sequence up operation. With RETHDS/ inactive, the servo control logic assumes control of the linear motor. PWRINI makes ST0/ active, which in turn causes load speed (LDSP/) and reverse (REV/) to become active through 10B10, 17E13, and 17E10.

LDSP/ and REV/ will cause the linear motor to drive the heads in reverse as soon as RETHDS/ becomes inactive. This reverse movement will bring the heads to the outer guard band (OGB/). (During an initial sequence up, the heads are already located on OGB.) As soon as the servo pulse monitor detects OGB/, this signal will be ANDed with ST0/ by gate 13E4 to activate ST1 and deactivate ST0/ through quad flip-flops 11D and 11C. ST0/ inactive will deactivate LDSP/ and REV/, while ST1 will activate LDSP/ and forward (FWD/) through gates 17E13 and 17E4. This will cause the linear motor to drive the heads forward. The forward movement will cause OGB/ to become inactive, which is ANDed with RETHDS/ inactive, ST1 active and minus threshold re-powered (MTHB/) inactive. This will activate ST2 and deactivate

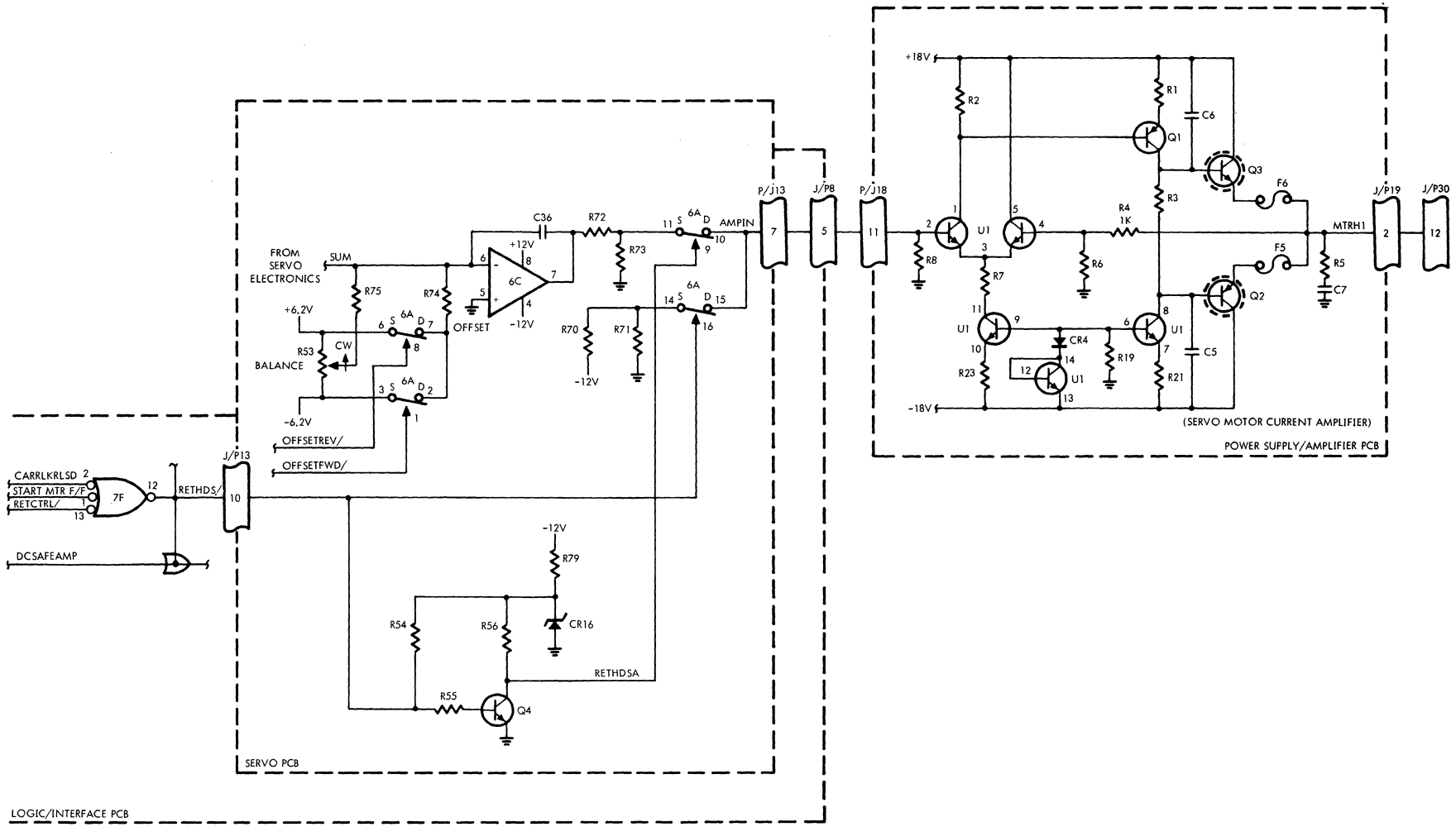


Figure 4-21. RETHDS/Control of Servo Motor

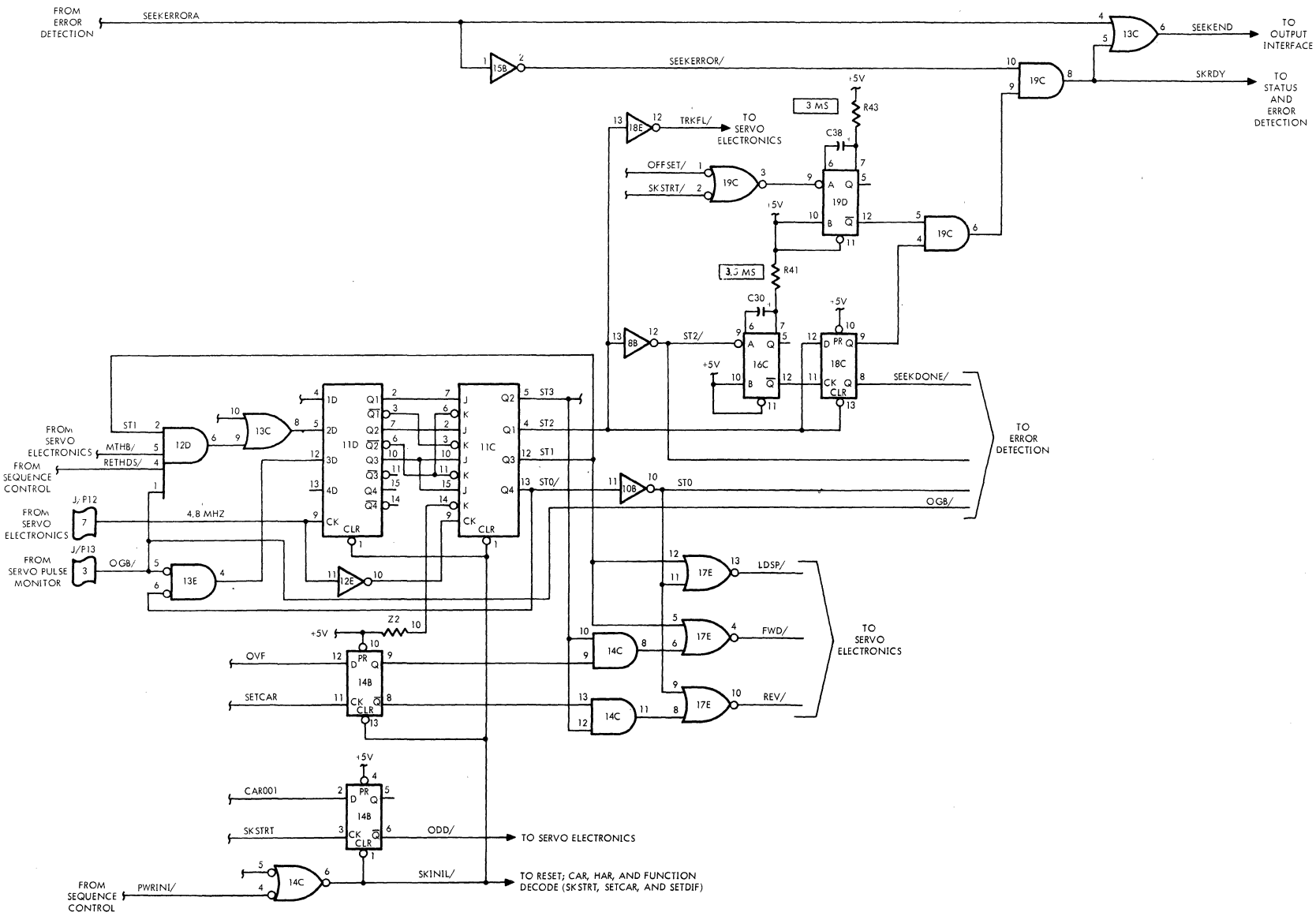


Figure 4-22. Servo Control Logic (Sequencing)

ST1. MTHB/ is generated from minus threshold (MTH/), which is a signal from the servo electronics indicating that the servo head is not positioned on a track.

MTH/ will become inactive when a cylinder boundary is being crossed. The first cylinder (track) boundary to be detected from forward motion away from OGB is cylinder zero. As soon as MTHB/ becomes inactive AND gate 12D6 will be satisfied with ST1 being deactivated and ST2 being activated. ST1 inactive will deactivate LDSP/ and FWD/, while ST2 will generate track following mode (TRKFL/) through gate 18E12. TRKFL/ goes to the servo electronics to command the servo to remain positioned on the track where it is presently located. ST2 also clocks the seek ready delay, 16C5 (3.5 ms +10 percent), which in turn clocks the seek done flip-flop 18C$\bar{9}$ upon time out of the delay.

SEEKDONE is ANDed with the output of the offset or no motion seek command start delay, 19D5, through AND gate 19C6. This signal is ANDed with seek error (SEEKERROR/) inactive through gate 19C8 to produce seek ready (SKRDY). SKRDY is sent to the status logic and also creates the signal SEEKEND through gate 13C6.

SEEKEND is transmitted through the output interface to the controller, via the data cable. This signal is transmitted regardless of unit selection to act as an interrupt to the controller. It alerts the controller that the disc drive wants attention (either completed a motion command, SKRDY, or has an error condition, SEEKERROR, not allowing it to do what was commanded). In this case, it was a sequence up operation.

With the controller being alerted, it can now select the disc drive and interrogate its status. In this case it will be on cylinder (/IONCYL) generated from SKRDY, and ready (/IRDY), which becomes active when 30 SECTMR/ becomes inactive as long as RETHDS/ and FAULT/ are inactive (reference Figure 4-23).

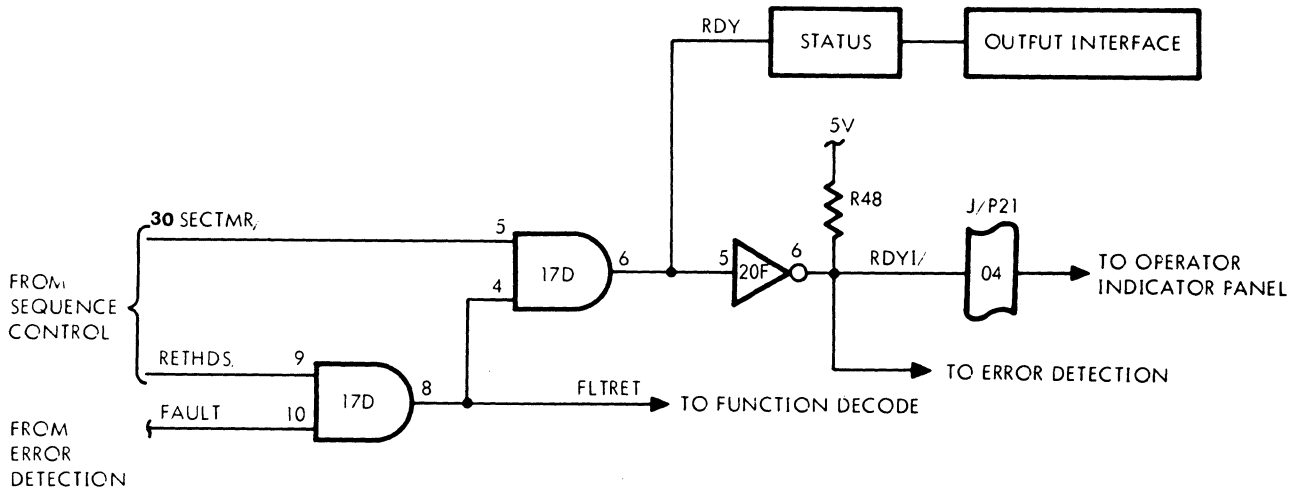


Figure 4-23. Ready Logic

l. Sequence Summary

Upon application of power, PWRINI initializes the logic, DCSAFE becomes active within 2±1 seconds. DCSAFE enables SEQENBL which is ANDed with DCSAFEDLYD to activate the STR MTR F/F. STR MTR F/F enables the spindle brake to release and generate SPINBRKRLSD, which is ANDed with STR MTR F/F to start the spindle motor. SPINBRKRLSD also starts 30 SECTMR/ which resets PWRINI and acts as a monitor to ensure that the spindle speed is safe within an allotted time.

When the disc speed becomes safe, the carriage lock is released generating CARRLKRLSD, which along with STR MTR F/F, DCSAFE and the absence of RETCTRL/ deactivates RETHDS/. This allows the servo control logic to control the linear motor.

When the 30 SECTMR/ signal becomes inactive, SLNDHIT/ becomes inactive and changes SLNDDRIVE from a solenoid pull voltage (+18V) to a solenoid hold voltage (+9V). This is becuase both solenoids (spindle brake and carriage lock) have been pulled (released).

The servo control logic positions the heads to cylinder zero and produces SKRDY and SEEKEND. SEEKEND is transmitted to the controller to notify it of the completion.

SKRDY produces ONCYL as status for the controller to interrogate, while RDY status is generated after 30 SECTMR becomes inactive.

m. Sequence Down

For a sequence down, if any of the signals DCSAFE, SPINBRKRLSD/ or DISCSPSAFE/ become inactive, the STR MTR F/F is deactivated, turning off power to the spindle motor. This will cause the spindle brake to drop out applying a brake to the spindle. RETHDS/ is activated causing the heads to be driven to the outer stop. The carriage lock will drop in place and hold the carriage in a retracted position over the outer guard band.

Function Decode

The function decode logic receives the tag (set cylinder, set head, and control) and bus (0-9) signals from either the input interface or the exerciser. As shown in Figure 4-24, the multiplexors (7B, 9C, 8C, and 10C) are enabled by MUXENBL/, which is derived from UNITSELD/ (on-line operation) or /ETESTMODE/ (exerciser operation) through OR gate 12B11. Whether the A or B inputs are transferred to the Y outputs depends on the signal TESTMODE. When TESTMODE is inactive (either exerciser not installed or exerciser installed with control switch in OFF position), the A inputs (input interface) are transferred to the Y outputs.

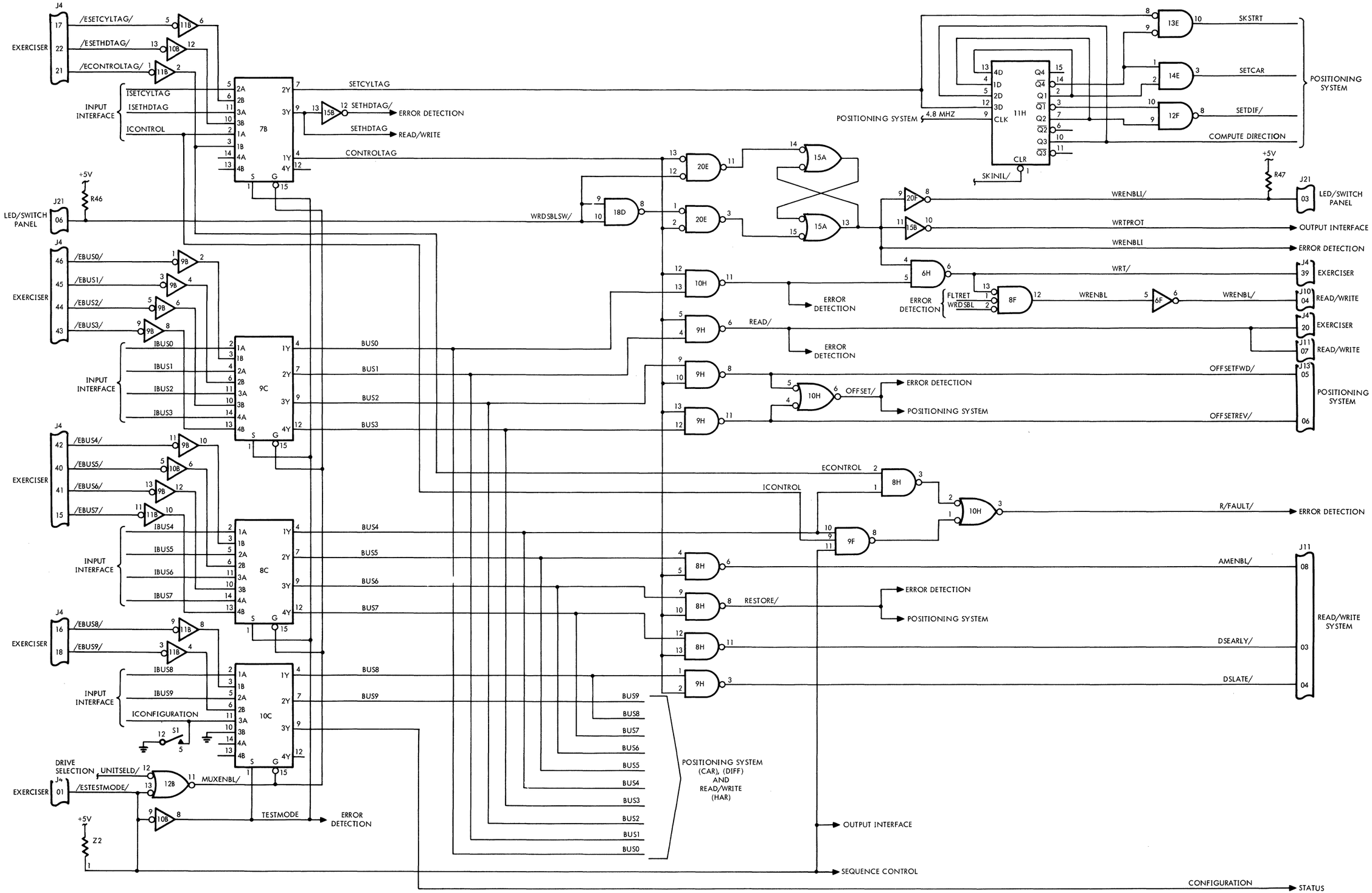


Figure 4-24. Function Decode Logic

Conversely, when TESTMODE is active, the B inputs (exerciser interface) are transferred to the Y outputs.

Table 4-2 is a matrix of the function decode, presenting the purpose the buses provide under the three different tags.

TABLE 4-2

BUS AND TAG DECODE

	SETCYLTAG	SETHDTAG	CONTROL TAG
BUS 0	CAR 1	HAR 1	WRT
BUS 1	CAR 2	HAR 2	READ
BUS 2	CAR 4	HAR 4	OFFSET FWD
BUS 3	CAR 8	HAR 8	OFFSET REV
BUS 4	CAR 16	*HAR 16	R/FAULT
BUS 5	CAR 32	*HAR 32	AMENBL
BUS 6	CAR 64	--	RESTORE
BUS 7	CAR 128	*FXHDSEL	DSERLY
BUS 8	CAR 256	--	DSLATE
BUS 9	CAR 512	--	--

* Applicable only if fixed head option is installed.

During a set cylinder tag, buses 0-9 are used to determine direction of motion, distance to be traversed (difference) and the new position of the carriage is put into the cylinder address register (CAR). This is accomplished by the buses 0-9 being sent to the positioning system and SETCYLTAG signal going to quad latch 11H, which is clocked by 4.8 MHz from the positioning system that clocks in the following sequence: A signal from Q3 to compute the direction; next, SETDIF/ which stores the value of the distance (number of cylinders) that the carriage is to move (difference between current bus value and present CAR value); next, SETCAR which stores the current bus value in the CAR (carriage position upon completion of pending seek operation), and finally, SKSTRT to initiate servo motion to go to the cylinder equal to the value in CAR.

The set head tag, besides going to error detection to determine whether or not the head circuits are safe and that an illegal head is not selected, also goes to the head address register (HAR) in the read/write system along with bus bits 0-5 and 7. The bus bits are clocked into HAR by SETHDTAG to provide the value of the desired head. Buses 4, 5, and 7 are only applicable if the fixed head option is installed.

Control tag decodes the bus bits 0-8 into commands (other than seek start). In addition to providing commands to be done by the drive, control tag while active prevents the cross-coupled

latch 15A from changing state. This is done to prevent changes at illogical times, such as during a write operation. Since control tag has to remain active during an entire write operation, switching of the write enable/disable switch will be ignored once the operation has commenced until the operation is complete as signified by control tag going inactive.

During control tag, bus 0 generates a write (WRT/) signal to the exerciser and write enable (WRENBL/) to the read/write system, provided that WRENBLI is active and FLTRET and WRDSBL are inactive. This enables the write function to transfer data from the input to the disc.

Bus 1 generates a READ/ signal to both the exerciser and the read/write system. This enables the read function to transfer data from the disc to the output.

Bus 2 (forward) and bus 3 (reverse) generate offset signals to the positioning system. The signals command the servo to move 200 microinches from the center of a track location. Bus 2 is forward (closer to spindle), while bus 3 is reverse (farther away from spindle, toward outside of disc).

Bus 4 generates a result fault (R/FAULT/) signal for the error detection logic. This signal is used to clear error conditions that generate a fault signal.

Bus 5 generates the address mark enable (AMENBL/) signal. This signal is not used with the current data format.

Bus 6 generates the RESTORE/ signal that causes the carriage to reposition itself to cylinder 0, clear various error conditions, and generates the seek initialize (SKINIL/) signal.

Bus 7 generates data strobe early (DSEARLY/) used by the read/write system to shift threshold point in an attempt to recover data that has "peak shifted" from its nominal location.

Bus 8 generates data strobe late (DSLATE/) used by the read/write system to shift a threshold point in an attempt to recover data that has "peak shifted" from its nominal location.

Bus 9 is not used with control tag.

ICONFIGURATION also goes through the mux and as shown on Figure 4-24, this signal can be permanently disabled by closing S1-5. When the mux is enabled for the input interface and ICONFIGURATION is active, CONFIGURATION is sent to the status logic to allow alternate status to be transmitted via the output interface. This alternate status is configuration information revealing whether or not the fixed head option is present and the number of movable heads (two-bit decode, value 0-3, representing 0 = 2 heads, 1 = 6 heads, 2 = 10 heads, and 3 = 14 heads).

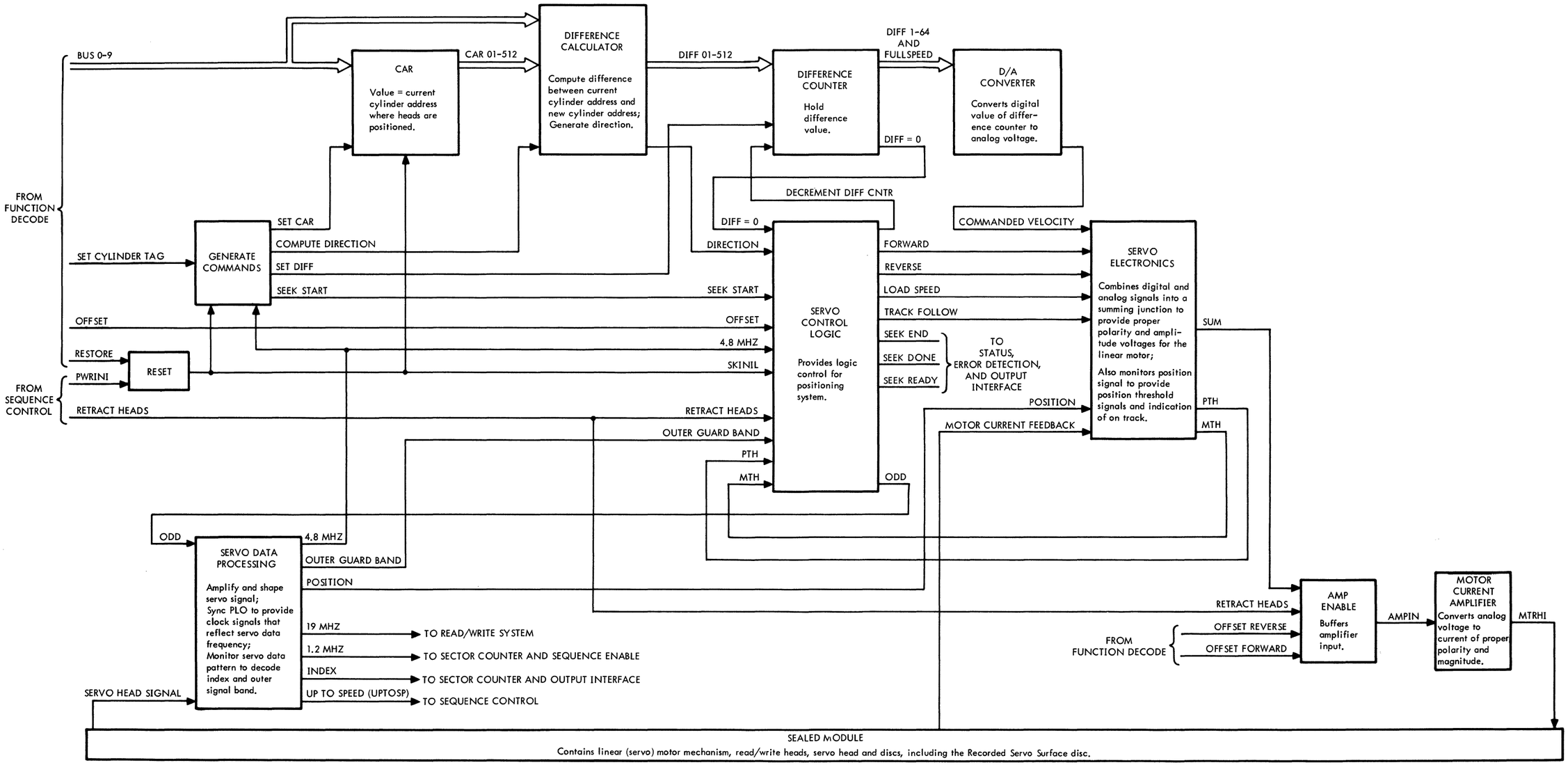


Figure 4-25. Positioning System Block Diagram

Positioning System

The positioning system provides the method or mechanism to position the read/write heads at a selected cylinder. Figure 4-25 presents a block diagram of the positioning system.

The positioning system includes a servo head that is mounted to a head carriage along with the read/write heads. The head carriage is connected to a linear motor bobbin and rides on a carriage way. The positioning system converts a positioning voltage to a linear motor drive current. The interaction of the drive current, linear motor bobbin, and motor magnet controls the movement of the linear motor bobbin in either a forward or reverse direction. It is this interaction that positions the heads.

Feedback provided by the servo head signal and motor current controls and limits carriage speed and controls the gain within the servo system. The system operates either in velocity mode or track following mode. In velocity mode the head carriage is moved from its current cylinder position to the newly selected cylinder position. In track follow mode the heads are maintained at or about the center of the selected cylinder by the null-seeking action of the servo.

The positioning system is made up of four major elements: (1) Recorded servo surface, the bottom side of the bottom disc, which provides pre-recorded data through the servo head. This data allows the positioning system to determine cylinder location and the beginning point for each track and sector location within a track; (2) servo system control, which provides the logic to direct the positioning system during the initial seek (power-on or first seek), program controlled seeks, restore operations, and retract heads in conjunction with sequence control; (3) servo data processing into clocks and position information, which amplifies, decodes, and processes the servo data from the servo head to provide a position signal, clock signals in frequency with the rotational speed of the recorded servo surface disc, index (definition point of beginning of a track), information about whether or not the disc is spinning at a speed sufficient for the heads to be loaded, and detection of the outer guard band (area beyond the read/write data area used as the head load/unload area); (4) servo motor control, which amplifies and sums the analog and digital control signals. These signals provide current of proper magnitude and polarity to the bobbin within the linear motor, which in turn provides linear direction control of the heads on the disc surface.

1. Recorded Servo Surface

The servo surface has 732 tracks of pre-recorded data, which is defined as the servo zone. The servo zone is divided into three bands; guard band 2, guard band 1, and servo data arranged

respectively from the outside of the surface to the inside of the surface (see Figure 4-26). The number of tracks and track location numbers are presented in Table 4-3.

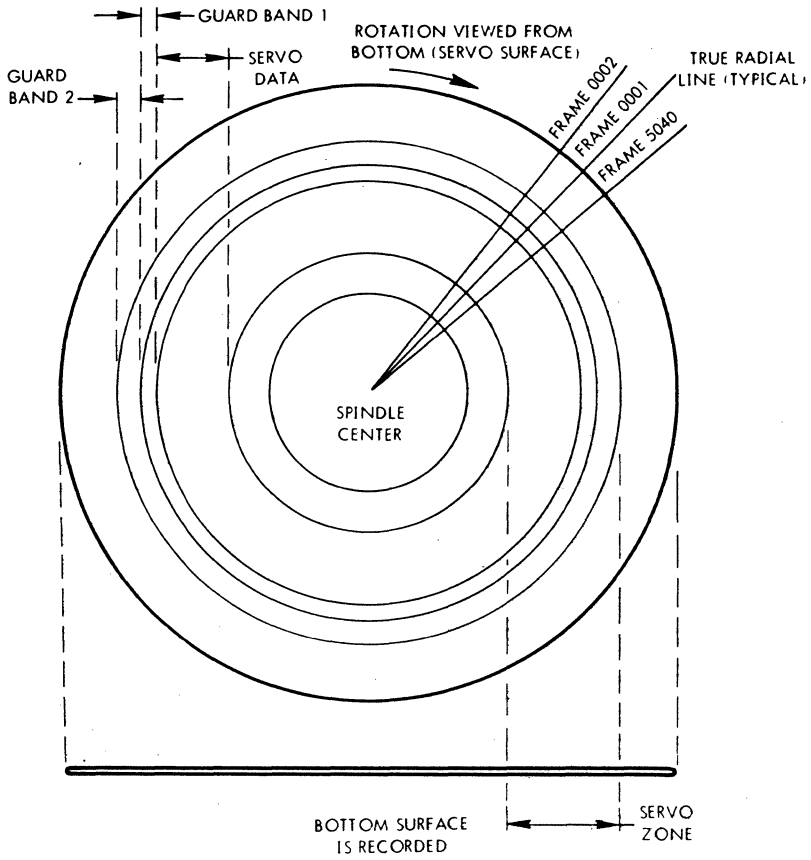


Figure 4-26. Servo Disc Layout

TABLE 4-3

SERVO ZONE

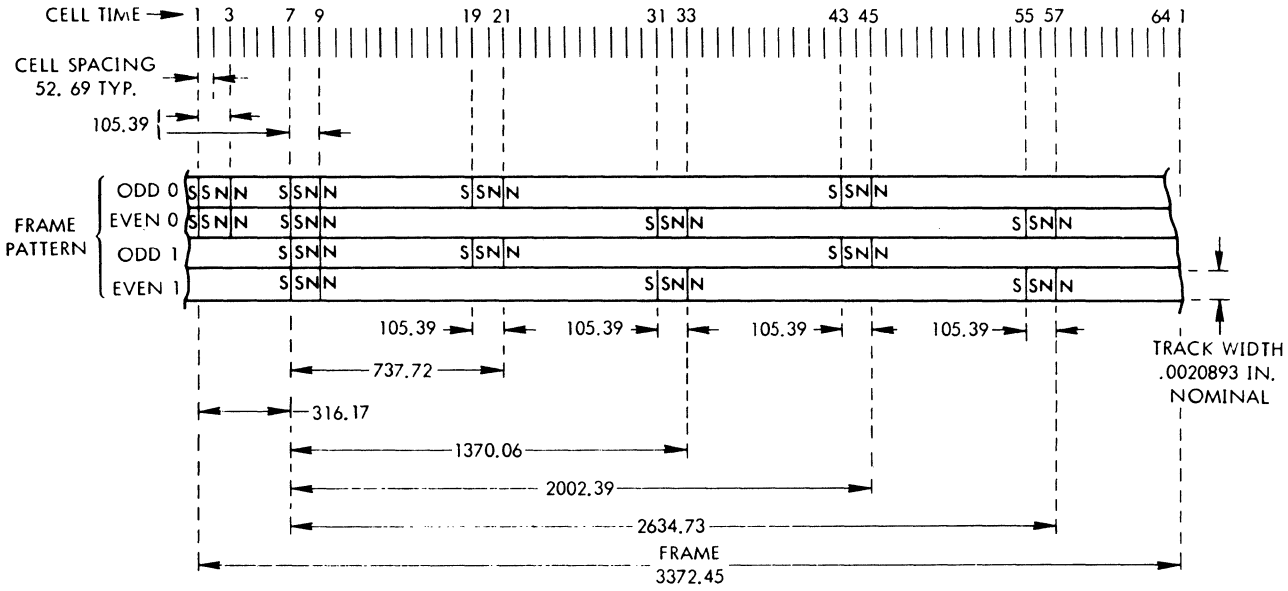
BAND	TRACK LOCATION NUMBERS	TOTAL NUMBER OF TRACKS IN BAND
Guard Band 2	-106.5 to -8.5	99
Guard Band 1	-7.5 to -1.5	7
Servo Data	-0.5 to +624.5	626

The three bands of the servo zone are further divided into two areas: (1) the outer guard band area is comprised of guard bands 1 and 2, and (2) the data area. While there is provision for 626 tracks in the data area, only 561 are used.

Each track is divided into 5040 equally spaced frames, which are numbered 1 through 5040. Each frame is further divided into 64 equally spaced cells, numbered 1 to 64 (see Figure 4-26 and 4-27).

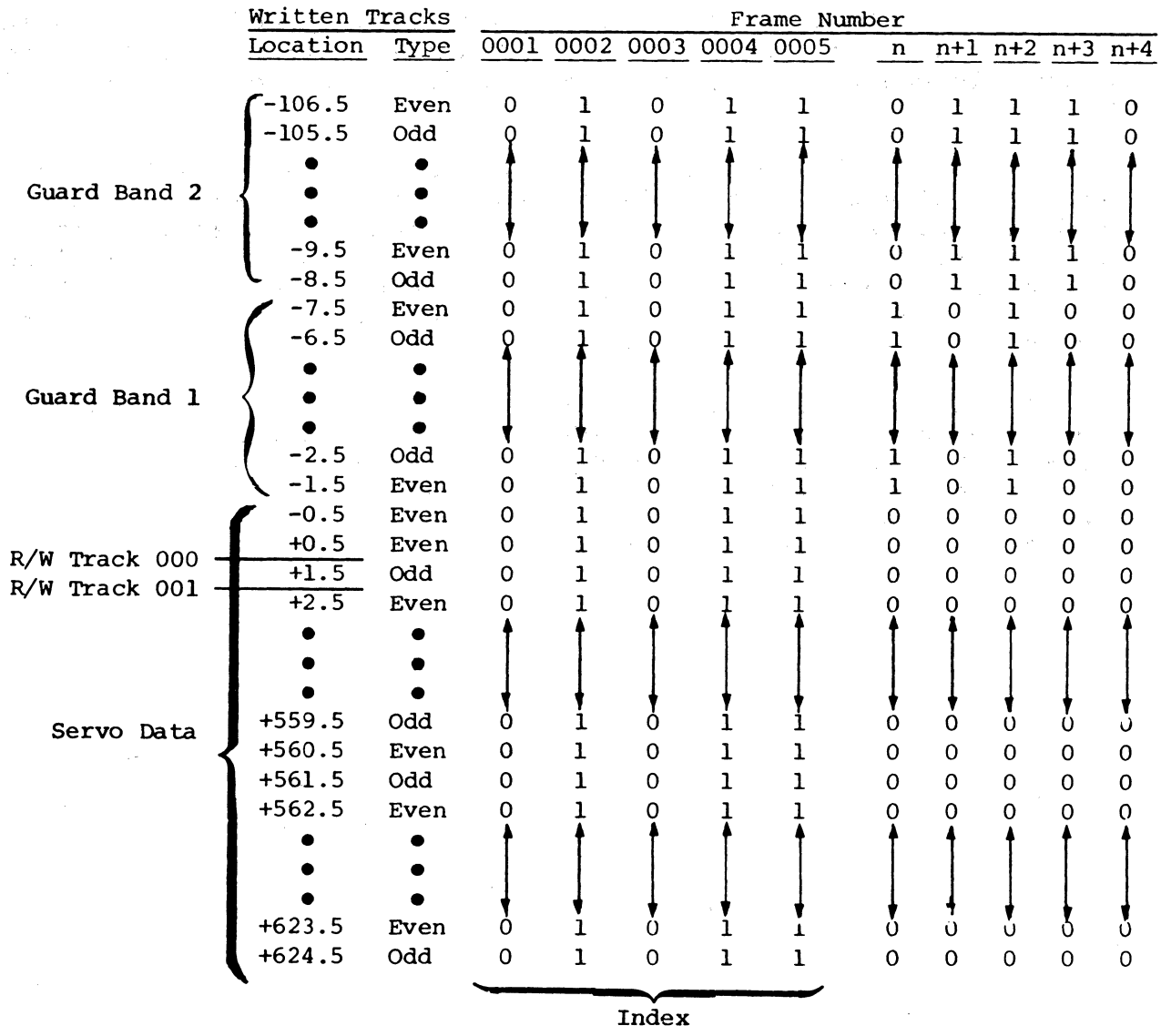
Cell 1 is the beginning of each frame while frame 1 is the beginning of each track. All frames are aligned radially to form 5040 sectors per track. Frame 1 is created by a special pattern that exists in frames 1, 2, 3, 4 and 5. This pattern is defined as index, which equals the beginning of each track. The pattern is a sequence of 01011. The index pattern exists at the beginning of all 732 servo zone tracks.

The guard bands are differentiated from each other and from the servo data patterns by unique patterns. Guard band 1 has a 5-frame pattern sequence of 10100 and guard band 2 has a 5-frame pattern sequence of 01110. The guard band patterns are written every 18 frames starting with frame 19, then 37, etc. for a total of 279 times-per-track (see Figure 4-28).



All times are at 3530 RPM and are in nanoseconds
Flux polarity as shown is reference only

Figure 4-27. Servo Track Frame Pattern



n = 19, 37, 55....5017, 5029

Frames not illustrated are '0'

Figure 4-28. Frame Arrangement

The tracks are written in odd and even frame patterns with each frame being either a 0 or 1. This provides for four possibilities; odd 0, odd 1, even 0, or even 1. Odd frames comprise odd tracks, and even frames comprise even tracks with the further distinctions of 0 or 1 within the frames providing the patterns for index or guard band detection.

The frames acquire their distinctions by the presence or absence of magnetic transitions at certain cell times within the frames. A "0" frame is distinguished by having transitions at cell times 1 and 3. All frames have transitions at cell times 7 and 9 and this is referred to as the sync pulse. Odd frames are

distinguished by transitions at cell times 19, 21 and 43, 45 while even frames have transitions at cell times 31, 33 and 55, 57 (see Figures 4-27 and 4-29).

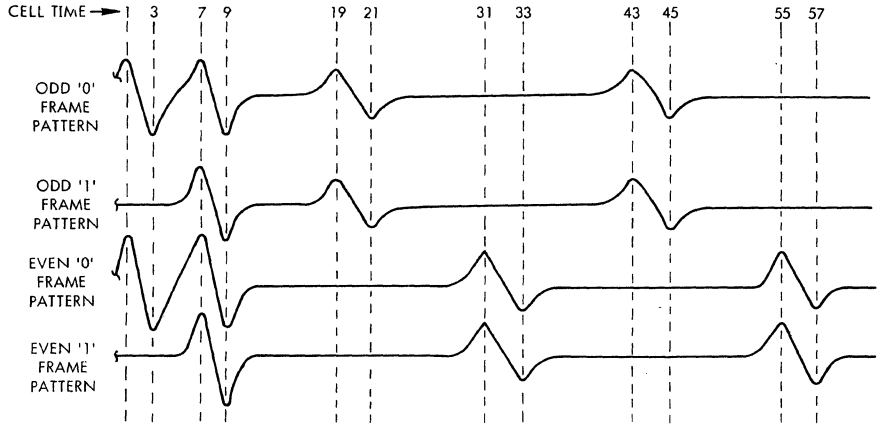


Figure 4-29. Frame Patterns

The positioning system works on a null-seeking basis while in track following mode. To accomplish this the playback through the servo head is used by the positioning system to provide the proper polarity and magnitude of current to the bobbin of the linear motor. This will cause the servo head to be positioned so that it receives an equal amplitude from two adjacent servo tracks. The reference "on track" means that the servo head is located between two adjacent servo tracks. Actually, the term "on track" refers to a read/write (R/W) track. If all of the R/W heads are aligned with the servo head relative to a true perpendicular line from the disc surface, the R/W tracks will be located at the center between two servo tracks.

A R/W track has the further distinction of being located only within the area of the servo data tracks. While there are 626 servo data tracks, there are only 561 R/W tracks.

An even R/W track is defined as the center of two adjacent servo tracks. There is an even servo track toward the outside of the disc and an odd servo track toward the inside of the disc. Conversely, an odd R/W track is defined as the center of two adjacent servo tracks, with an odd servo track toward the outside of the disc and an even servo track toward the inside of the disc.

As shown in Figure 4-28, R/W track 000 (an even track) is located between servo tracks EVEN +0.5 and ODD +1.5, with R/W track 001 (an odd track) located between servo tracks ODD +1.5 and EVEN +2.5.

In addition, all frames of the same number are aligned radially across the entire recorded surface with the sync pulses at cell times 7 and 9 written in the same polarity in every frame of every track. This causes the pulses to be additive with the result being that the sync pulses appear to be approximately twice the peak-to-peak amplitude of the pulses at cell times 19, 21, 31, 33, 43, 45, and 55-57. There is a similar effect with the pulses at cell time 1, 3, except that these pulses do not appear in every frame of every track.

2. Servo System Control

The servo system control (see Figure 4-30) provides the logic to direct the positioning system during the initial seek (power on or first seek), program control seek and restore operation.

a. Initial Seek

During an initial seek, power initialize (PWRINI) comes into OR gate 14C6 to produce seek initialize (SKINIL/). SKINIL/ resets (1) the cylinder address register (CAR) to indicate cylinder zero, (2) the set cylinder tag (SETCYLTAG) command sequencer (11H), (3) the odd flip-flop (14B5) to indicate even cylinder selection, (4) the IN flip-flop (14B9), and (5) the state registers (11C and 11D) so that ST0 is active and ST1, ST2 and ST3 are inactive.

ST0 active generates reverse (REV/) and load speed (LDSP/) which go to the servo motor control to move the heads in reverse (toward outside of discs) at a controlled speed defined by load speed. Actually, the heads will already be over the outer guard band. As soon as the discs spin at a speed sufficient for the servo data processing into clocks and position information section to detect the outer guard band 2 pattern, outer guard band (OGB/) will become active and be ANDed with ST0/ to deactivate ST0 and activate ST1.

LDSP/ generates fullspeed (FULLSP/) through OR gate 19H6, which in turn enables all the inputs to the digital to analog (D to A) converter (8C4). This will produce the maximum commanded velocity. However, velocity is held to 1 inch/second by LDSP turning off FET 7D9 in the servo motor control circuit. This places a limiting resistor in series with the DA input to the linear motor.

ST0 inactive deactivates REV/ and LDSP/; however, ST1 active generates LDSP/, this time with forward (FWD/). Assuming retract heads (RETHDS/) is inactive, this condition causes the linear motor to move the heads forward (toward center of disc) until OGB/ goes inactive (no longer on guard band 1 or 2) and minus threshold buffered (MTHB/) goes inactive.

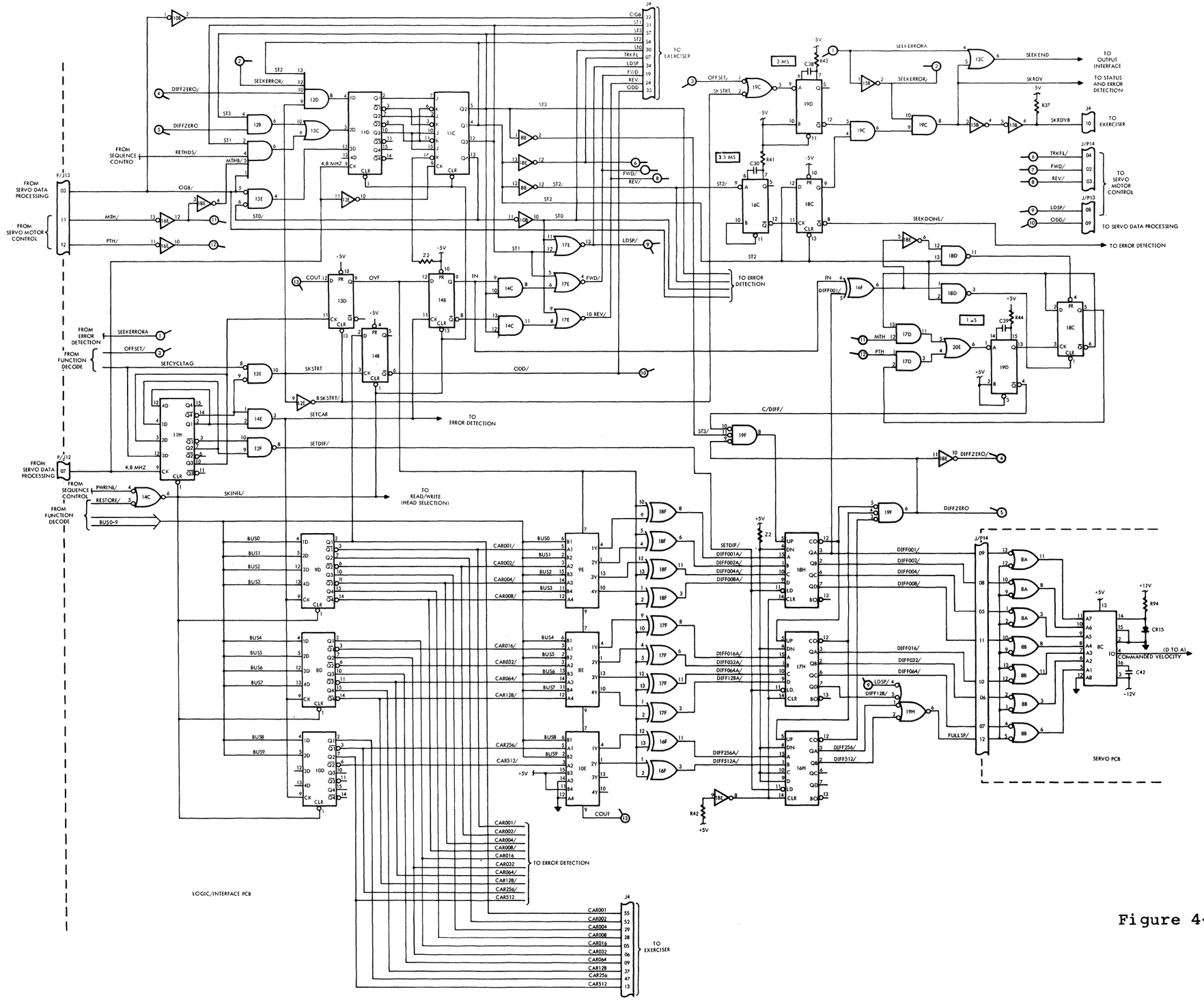


Figure 4-30. Servo System Control

With ODD/ inactive, minus threshold (MTH) will be active from the EVEN -1.5 guard band track (OGB still active) until crossing the EVEN +0.5 servo data track. When MTHB/ goes inactive, ST1 will be reset (inactive) and ST2 will become active. ST1 going inactive will deactivate FWD/ and LDSP/, which removes command velocity as the driving force for the linear motor.

ST2 active will generate track following mode (TRKFL/) and start a 3.5 millisecond timer. Track following mode will now take over in the servo motor control circuit. Through its null-seeking function, it will bring the heads to an orderly stop at the center of servo data tracks (EVEN =0.5 and ODD =1.5). This is R/W track 000 or cylinder 000, which equals the value held by the CAR.

The 3.5 millisecond delay will allow time for the servo to settle on track and upon its timeout, set the SEEK DONE flip-flop (18C9). This in turn will generate seek ready (SKRDY) status and a SEEKEND interrupt to the output interface. The system will be alerted that the drive is now on track and ready for further operation.

At completion of the initial seek, ST2 will remain active, keeping TRKFL/ active until a motion command (seek start and difference greater than zero or a restore operation) is activated.

b. Program Control Seek

A program control seek may be initiated by either the system that the drive is connected to or by an exerciser. The seek begins by placing the desired cylinder address on the input interface bus and then activating set cylinder tag (SETCYLTAG).

The bus value is evaluated in conjunction with the present CAR value by the subtractor logic. The subtractor logic is made up of the four-bit adders (8E, 9E, and 10E) and exclusive OR gates (16F, 17F, and 18F). The configuration is such that whenever the bus value is greater than the value of CAR, there will be a carry out (COUT) of the last stage, which is used to indicate forward direction. Conversely, whenever the bus value is less than the value of CAR, there is no carry out, indicating reverse direction. This is accomplished by performing a binary add of the bus bits as a positive number, with the negative number complement of the CAR bits.

This could be interpreted that the bus value (cylinder to go to) is a positive number and the present CAR value is a negative number with the resultant number representing the difference. If the result is positive, the direction is forward, or if the result is negative the direction is reverse.

EXAMPLE: The system has been ordered to move the heads to cylinder 16 and they are presently at cylinder 8. Bus value equals positive 16 and CAR value equals negative 8. Add the two together and the result is positive 8. This number equals the difference and positive equals forward.

The system has been ordered to move the heads to cylinder 8 and they are presently at cylinder 16. Bus value equals positive 8 and CAR value equals negative 16. Add the two together and the result is negative 8. This number equals the difference and negative equals reverse.

The exclusive OR gates then will operate to supply a positive value to the difference counter. This may be accomplished by using overflow (OVF) which is really carry out latched. This procedure will convert negative numbers to positive numbers, while leaving positive numbers alone.

COUT will go to the overflow latch (13D9), which is clocked by the function sequencer (11H) by the next positive going pulse of 4.8 MHz after SETCYLTAG goes active. The output of the OVF latch will go to the direction latch (14B9) and back to the subtractor circuit, allowing the circuit to finish its difference calculation.

The next (second) positive going edge of 4.8 MHz will clock the function sequencer so that AND gate 12F8 is satisfied. This will generate set difference counter (SETDIF/). SETDIF/ will go to the difference counter (16H, 17H, and 18H) to clock in the value of the difference from the output of the subtractor. What will be loaded into the difference counter will be the difference value subtracted from the maximum value that the counter can hold. For purposes of the difference counter circuit, the maximum value is 1023. By using the previous example of a difference of 8, a value of 1015 will be loaded into the difference counter, which will give an active output of DIFF008/.

DIFF008/ will go to the D to A converter to generate a commanded velocity with a voltage proportional to the active input. The voltage will go to the servo motor control circuit to provide the proper drive current when enabled.

With the difference counter loaded to this value, AND gate 19F6 will be unsatisfied due to the input pin 5 being high. This deactivates difference zero (DIFFZERO and DIFFZERO/), which primes AND gate 19F8 to allow for clock pulses to clock the difference counter. AND gates 12D8 and 12B6 are also primed to change the state registers.

The next positive going edge of 4.8 MHz will clock the function sequencer so that SETDIF/ will be deactivated and SETCAR will be activated by AND gate 14E3. SETCAR will clock CAR to

load the present bus value (cylinder to go to) into CAR. SETCAR will also clock the direction latch (14B9) to the state defined by OVF. If set, IN will be active and the direction will be primed for forward motion. IN will also go to an exclusive OR gate in the difference clock (C/DIFF/) circuit. With IN active and DIFF001/ not active, AND gate 18D11 will be primed through inverter 18E6 so that as soon as ST2 goes inactive, latch 18C5 will be set. This will prime the difference clock circuit to generate the first difference clock from a positive threshold (PTH).

The next (fourth) positive going edge of 4.8 MHz will clock the function sequencer so that the Q4 output will be active. This disables AND gate 14E3, deactivating SETCAR. This will also prime AND gate 13E10 to generate seek start (SKSTRT) as soon as SETCYLTAG goes inactive. SKSTRT will enable AND gate 12D8 along with the other active inputs and this will step the state register to activate ST3 and deactivate ST2. SKSTRT will also clock the ODD/ flip-flop (F/F) 14B6 to a state defined by CAR001/. SKSTRT will generate SKSTRT/ through inverter 12E8. This signal resets the OVF F/F and starts a 3 millisecond timer (19D5).

ST2 going inactive will deactivate TRKFL/, which will put the positioning system into velocity mode. This condition also will reset the SEEKDONE/ F/F 18C9 and disable the AND gate inputs (18D11 and 18D2) to the difference clock threshold prime F/F 18C5. ST3 going active will prime AND gate 12B6 and will generate ST3/ through inverter 8B2. ST3/ will prime AND gate 19F8.

The servo motor control circuit will now drive the motor in the direction indicated by the velocity commanded from the D to A output. As the servo head crosses tracks, positive and minus threshold (PTH/ and MTH/) signals will be generated from the position signal. PTH/ and MTH/ generate PTH and MTH through inverters 16E10 and 16E12. These signals will be used to generate clock difference counter (C/DIFF/) clocks from one-shot 19D4.

For every C/DIFF/ pulse the difference counter will be clocked up by AND gate 19F8 until all carry out (CO) outputs from the difference counter are simultaneously low. These outputs will be low whenever all four bits of the same IC are active (high). As the difference counter outputs count up, the resultant active inputs to the D to A converter become less with the resultant output of commanded velocity becoming less in magnitude. This will decrease the drive to the linear motor to zero when the difference counter equals zero.

When AND gate 19F6 is enabled, difference equal zero (DIFFZERO) is generated. This will disable AND gate 19F8 to prevent the difference counter from being clocked anymore and AND gate 12B6 will be enabled. 12B6 will be satisfied and change the state register by deactivating ST3 and activating ST2. This will

put the positioning system back into track following mode and the seek will be completed with the heads positioned at the cylinder indicated by CAR. SEEKDONE/, SKRDY, and SEEKEND will be generated as in completion of the initial seek.

c. Restore Operation

A restore operation is commenced by either the system that the drive is connected to or by an exerciser. When a restore is decoded by the function decode logic, it is sent to OR gate 14C6. From this point a restore works like an initial seek, except that there is reverse motion until the outer guard band is detected. After the detection, restore functions identically to an initial seek.

3. Servo Data Processing Into Clocks and Position Info

This section of the positioning system processes the servo data playback from the servo head. The data is used to generate a position voltage. This voltage is used by the servo motor control circuit to maintain an on track position during track following mode and velocity feedback information and to maintain input for the threshold detectors during velocity mode. The servo data is also used to provide correctional input to the 19 MHz oscillator. This allows 19 MHz to reflect the rotational speed of the disc to generate clocks which (1) generates strobes for the position circuit, (2) decodes the servo data patterns to allow detection of index and the outer guard bands and (3) monitors the frequency of index pulses to determine whether or not the drive is operating up to speed (see Figure 4-31).

a. Clock Processing

The servo data is transmitted differentially from the servo head to the servo PCB where it is ac coupled to op amp 2F8,7. Here the servo signal low amplified (SRVOSIGLOAMP) is outputted from 2F7 and ac coupled to op amp 2E11,9. Figure 4-32 illustrates the resultant clocks and strobes that are generated from this input.

The circuitry from op amp 2E11,9 through voltage controlled oscillator 1B4 make up the phase lock loop oscillator (PLO) circuit. The voltage controlled oscillator (1B4) operates at about 19 MHz with voltage correction provided on its input pin 2. The voltage correction results from a phase difference in servo data sync pulses and DIV 64. This voltage compensation acts to make the 19 MHz reflect the actual frequency of the servo data sync pulses from the disc.

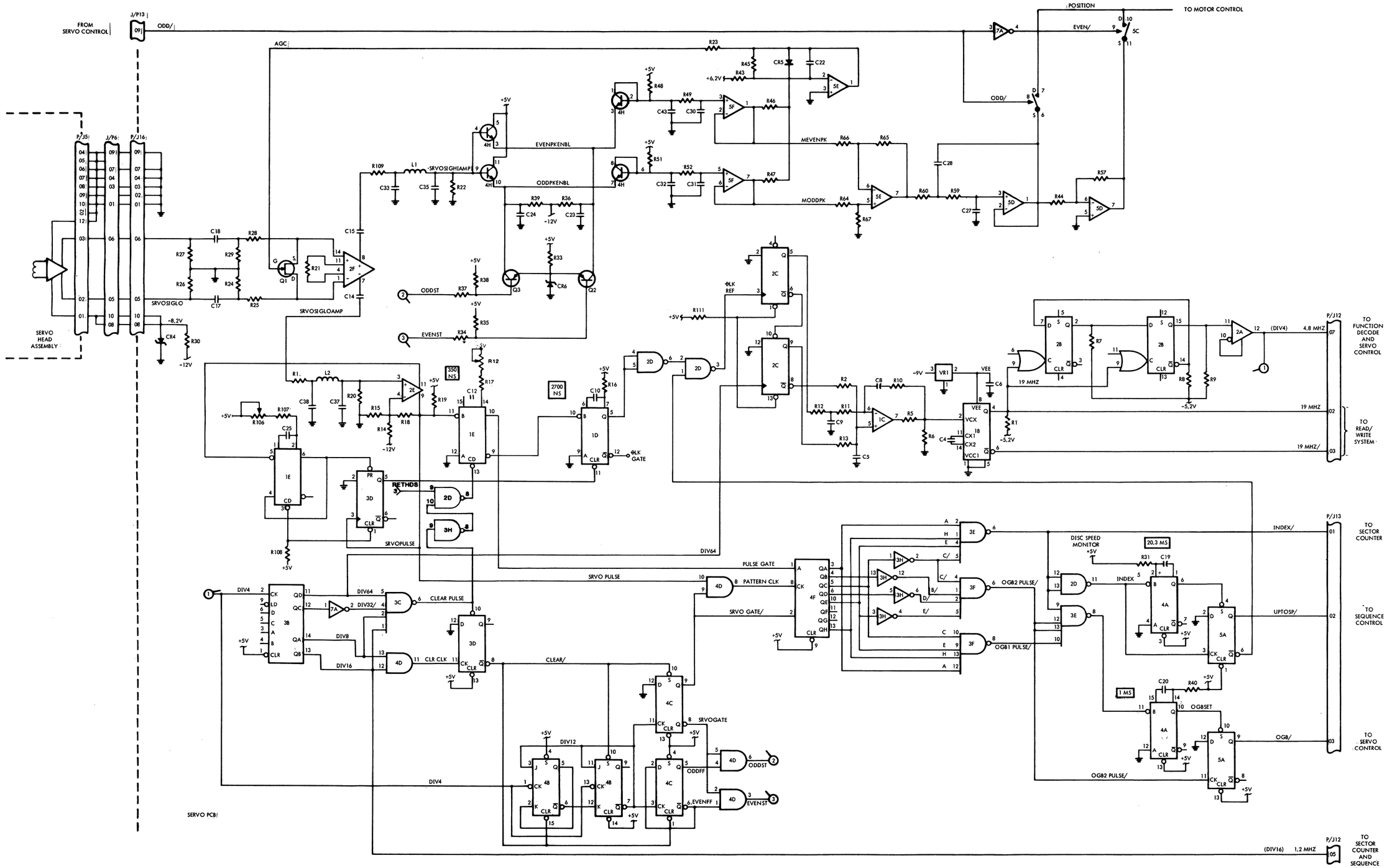
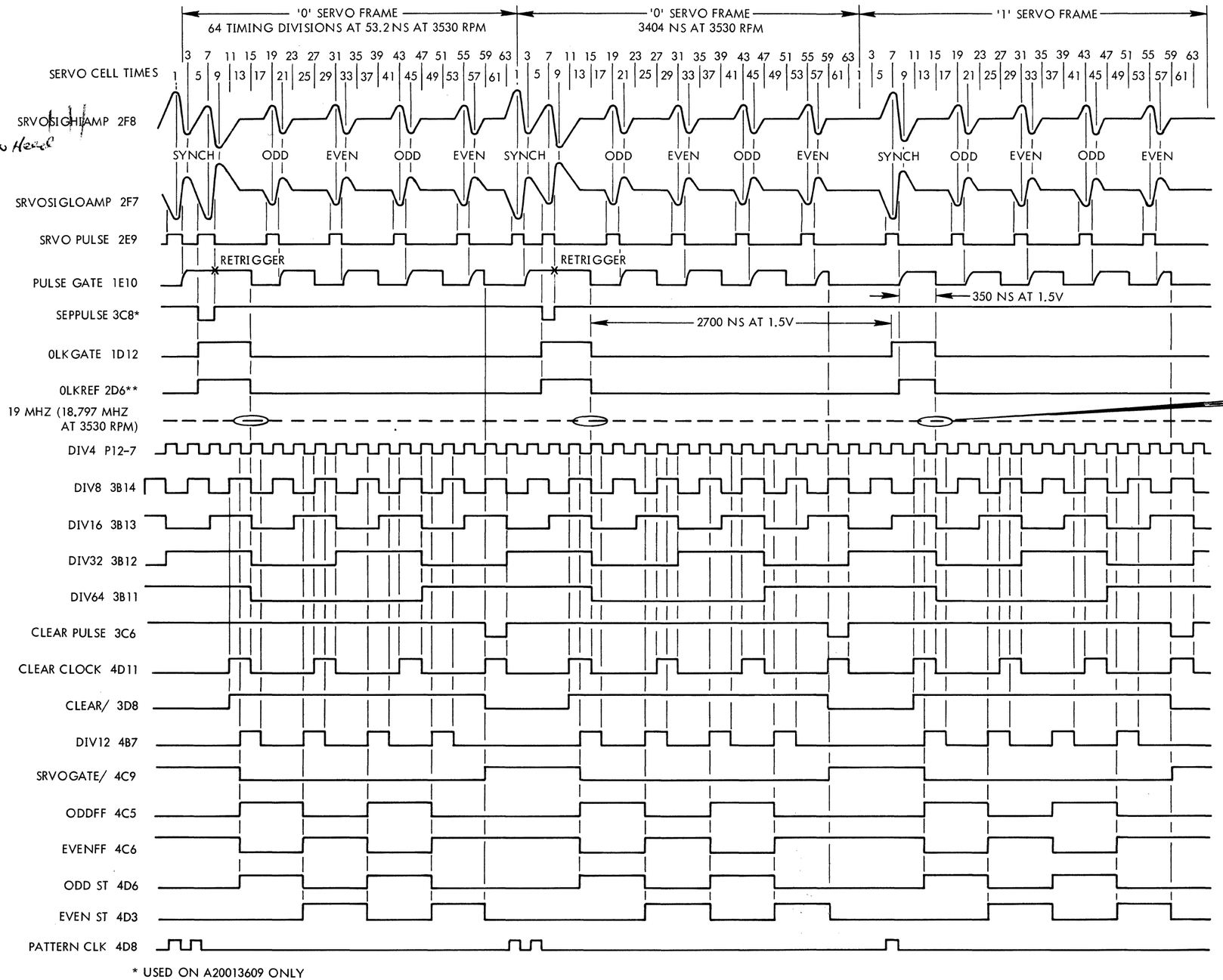
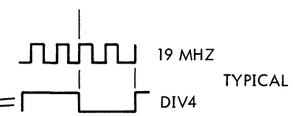
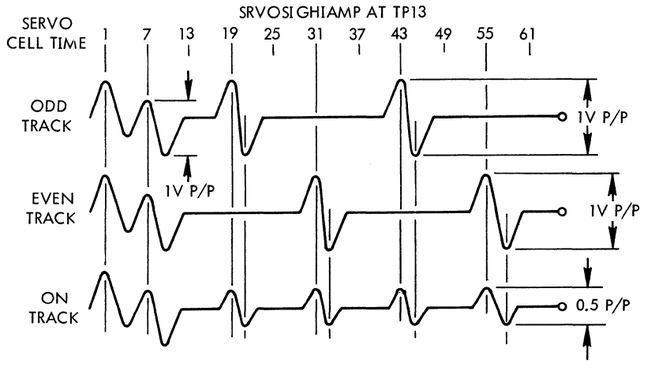


Figure 4-31. Servo Data Processing



* USED ON A20013609 ONLY
** 2D3 ON A20013609 IS OLKREF





SIGNALS SHOWN WITH RESPECT TO GND WITH ON TRACK CONDITION, NO SERVO MOTION.

ODD/EVEN PULSE AMPLITUDES WILL VARY WITH SERVO MOTION. IF THEY BECOME SMALL ENOUGH THE RESULTANT SRVOPULSE AND PULSE GATE SIGNALS WILL BE MISSING.

Figure 4-32. Servo Data Timing

The sync pulses are separated by the 350 nanosecond PULSE GATE, the 40 nanosecond separator pulse gate (SEP PULSE) and 2700 nanosecond phase lock gate (OLK GATE) one-shot circuits.

The PLO circuit works as a whole to sync the oscillator at the correct frequency and in the proper phase. Phasing is important so that the pattern decoder will be able to properly differentiate between "1's" and "0's."

F/F's 2B2 and 2B15 work as a divide by four (DIV4) circuit to generate the clock frequency 4.8 MHz. This frequency is used in the function decode and servo control logic. DIV4 is also used to generate further clock times (DIV8, DIV16, DIV32/, DIV64 and DIV12), to provide feedback (DIV64 and CLEAR PULSE) to the PLO and to generate servo gate (SRVOGATE, SRVO GATE/) and the odd and even strobes (ODDST and EVENST).

SRVO GATE/ is used with SRVO PULSE (TP11) and PULSE GATE (TP3) to drive the pattern clock shift register 4F.

SRVOGATE is used with the ODD/EVEN F/F to generate the odd and even strobes that are used by the position circuit. As illustrated in Figure 4-32, the strobes are only active during the time of the odd/even servo data pulses. This prevents the frame data and sync bits from getting into the position signal.

b. Pattern Detection

4F is a shift register, used for pattern detection of index and outer guard bands 1 and 2. The inputs (PULSE GATE and SRVO GATE/) are ANDED internally to become the data input which is clocked into the first stage of the shift register by PATTERN CLK. If both inputs are high when the positive going edge of PATTERN CLK arrives, then a "1" is clocked in; otherwise, a "0" is clocked in. The input data is then shifted through the shift register. The outputs of the shift register are monitored by AND gates 3E6, 3F6 and 3F8 to detect INDEX/, OGB2 PULSE/ and OGB1 PULSE/, respectively. Figure 4-33 illustrates INDEX/ detection.

INDEX/ is then used by the sector counter and the disc speed monitor circuit (2D11, 4A6, and 5A5) to generate up-to-speed (UPTOSP/). Upon initial POWER ON, UPTOSP/ is inactive or high. As the discs start to rotate an index pulse is detected which triggers one shot 4A-6 for about 160 milliseconds. This action removes the set from F/F 5A. A second index pulse triggers F/F 5A and activates UPTOSP, allowing phase LK gate 1 into phase detector 2C. This starts locking the phase lock loop comprised of 2C, 1C, and 1B. If the phase lock is not properly phase locked, index will not be detected. This will inactivate UPTOSP/ and remove phase L GATE/ pulses from the phase detector. When this happens, the UPTOSP/ will go high and the drive will cycle down. This action is illustrated in Figure 4-34.

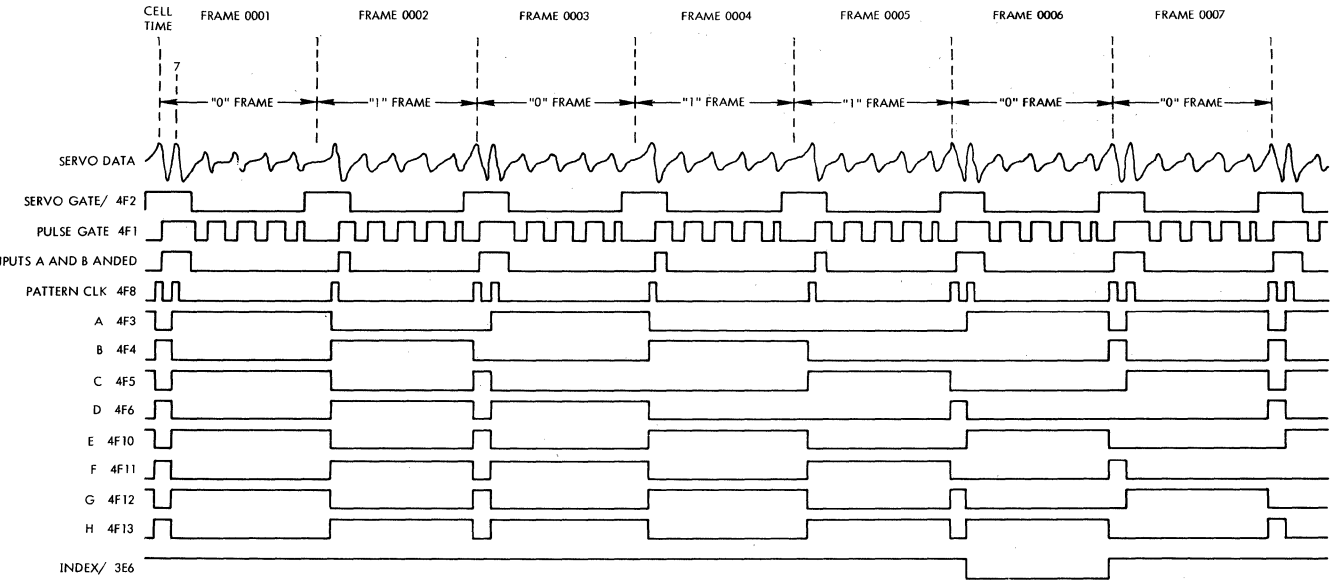


Figure 4-33. Index Pattern Detection

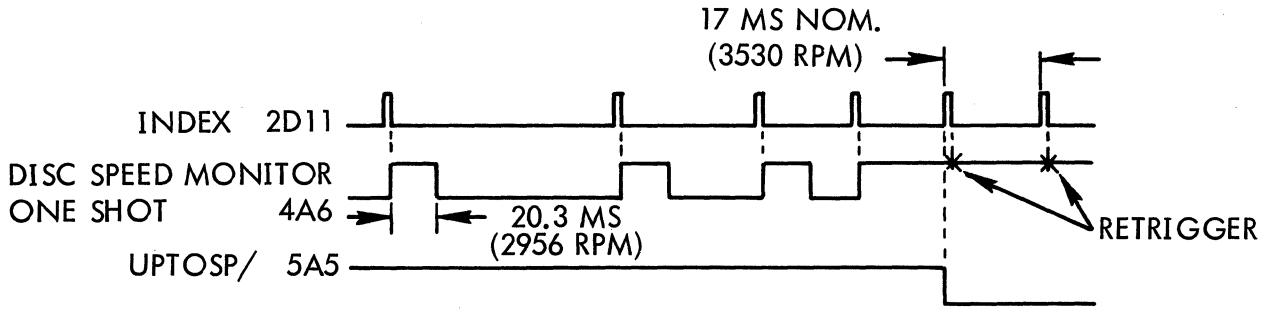


Figure 4-34. Up-To-Speed Detection

The outer guard band (OGB/) detection circuit (3E8, 4A10, and 5A9) is configured so that OGB/ will not become active until outer guard band 2 (OGB2 PULSE/) is detected. The circuit will then remain active until either outer guard band 2 or outer guard band 1 are being detected. This is illustrated in Figure 4-35.

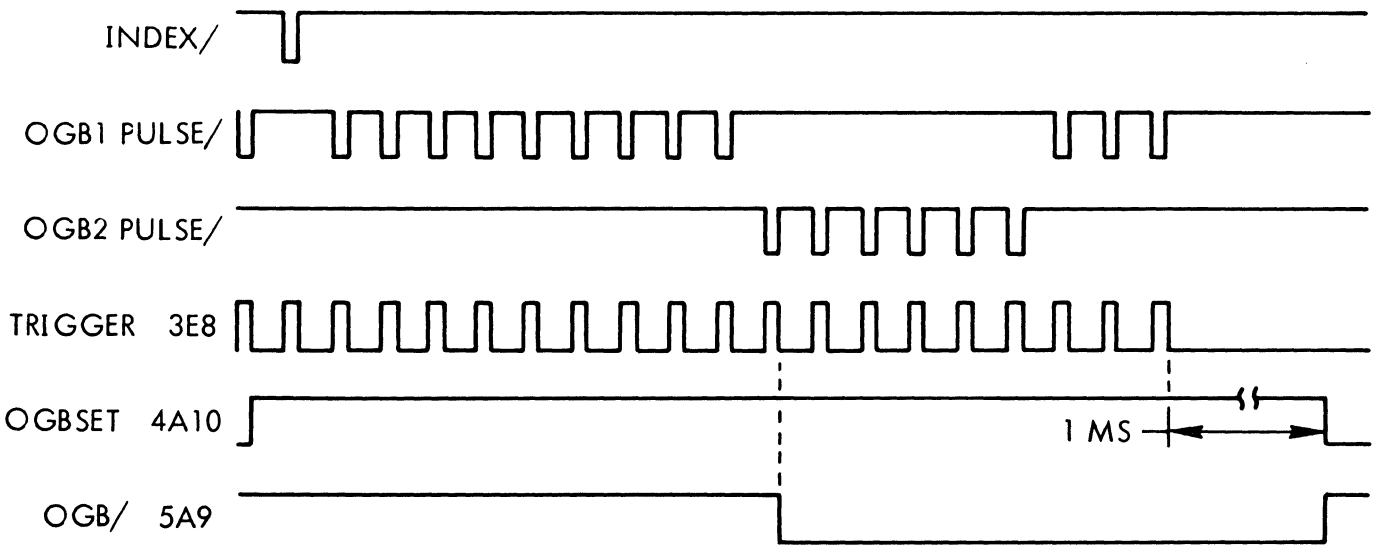


Figure 4-35. Outer Guard Band Detection

c. Position Signal Generation

The servo signal is detected and amplified by the servo head assembly. The output is then transmitted differentially to the servo PCB where it is ac coupled to op amp 2F8,7. The gain of 2F is controlled by the conductance of Q1. Q1 is varied by the AGC voltage applied to its gate. The function of AGC is to keep the servo signal at a constant amplitude. The AGC circuit is operating, whether in velocity or track following mode. However, AGC is a sampling circuit in that it is only fed during the time of odd/even strobes.

Only the pulses at cell times 19, 21, 31, 33, 43, 45, 55, and 57 are enabled by the odd/even strobes. This is illustrated in Figure 4-32. When a given strobe becomes active, such as even strobe (EVENST), Q2 will be turned off, thus enabling emitter follower 4H3,4,5. This allows detection of the negative peaks of the servo signal. Pin 3 then drives transistor 4H3,2,1 of the same transistor array package which is configured as a diode. As the signal goes negative, it charges capacitor C43 to its peak average value. As the signal goes positive it turns diode 4H3,2,1 off, which then holds the negative charge at C43. R49 and C30 smooth out any ripple present at C43.

The emitter follower action of transistor 4H3,4,5 is disabled when the even strobe is not active, due to Q2 being turned on.

When this occurs, diode 4H3,2,1 is reverse biased and C43 holds its charge until the next strobe.

The odd strobe (ODDST), Q3, transistor array 4H10,9,11 and 4H7,6,8, C32, R52, and C31 function identically to the even strobe counterparts.

Op amps 5F1 and 5F7 are configured as unity gain amplifiers. These outputs feed both the AGC circuit and the position signal circuit.

For the AGC circuit the outputs of 5F1 and 5F7 are tied into a summing junction consisting of R43, R45, R46, R47, and CR5. With +6.2V supplied as the AGC reference voltage, the AGC loop attempts to maintain the servo signal at a constant level. If the inputs to op amps 5F7 and 5F1 become less negative, the summing junction becomes more positive. This causes the output of op amp 5E1 to become more negative, which decreases the conductance of FET Q1. This allows an increase in gain of op amp 2F8,7, which increases (more negative) the input to op amps 5F1 and 5F7. The opposite condition takes place when the input to 5F1 and 5F7 becomes more negative. The nominal AGC voltage is -3.00V $\pm$ 2.00V.

For the position signal circuit, the outputs of 5F1 and 5F7 become minus even peak (MEVENPK) and minus odd peak (MODDPK). Op amp 5E7 is configured to act as a subtractor and subtracts MEVENPK from MODDPK with the resultant differ-ence then multiplied by 2 and filtered by a low pass filter. This filter consists of op amp 5D1, R59, R60, C27 and C28. The output of 5D1 is then phase shifted 180 degrees by op amp 5D7. The output of either 5D1 or 5D7 is then selected by ODD/ or EVEN/ through FET's 5C8 or 5C9 to provide the position signal. The position signal after the foregoing signal processing provides feedback to the servo motor con-trol circuit. The ODD/ or EVEN/ is made prior to servo positioning to enable the correct FET for proper feedback (it is negative feedback). The FET's are enabled by low (zero) signal and disabled by a high signal.

During track following mode, the position signal is used as feedback to find and maintain a null between two adjacent tracks. During velocity mode, position is used to keep track of crossing tracks and as a speed indicator by the frequency (rate) of crossings. Figure 4-36 illustrates position signal selection.

4. Servo Motor Control

This section of the positioning system sums together analog inputs under digital control to provide the correct magnitude and polarity for the linear motor current.

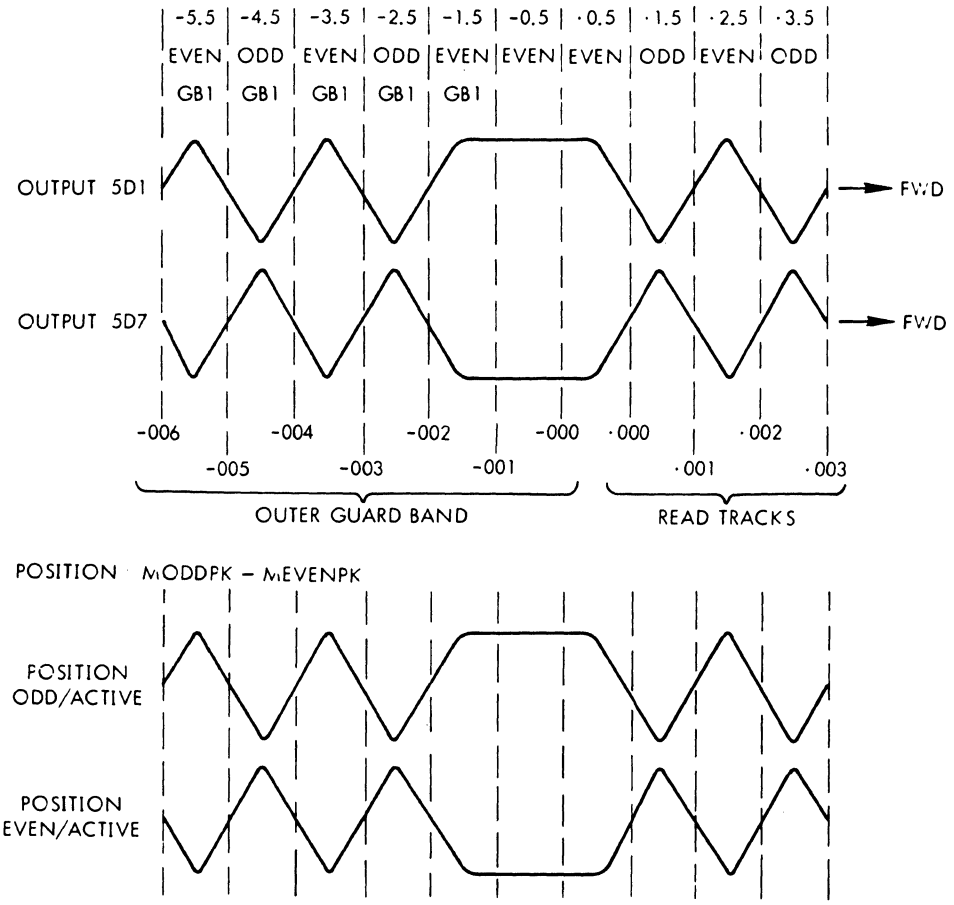


Figure 4-36. Position Signal

There are three modes of operation, one non-operational and two operational. Retract heads (RETHDS/ active) is the non-operational mode and track following (TRKFL/ active) and velocity (TRKFL/ not active) are the operational modes.

In addition, this section generates the plus and minus threshold (PTH/ and MTH/) signals from the position signal. PTH/ and MTH/ are used by the servo system control logic to generate diff clocks.

Figure 4-37 presents the servo motor control circuit.

a. Retract Heads

Retract heads (RETHDS/) is active when the unit is initially powered on or at any time DCSAFE, CARRLKRLSD, or start motor F/F are not active, or if RETCTRL/ is active. When RETHDS/ is active, all the circuitry forward of FET 6A9 is disabled by transistor Q4 being turned off. This allows the voltage divider of R54, R79, and CR16 to supply +5V to the FET which turns it off. At the same time FET 6A16 is enabled by RETHDS/ being low and this allows -12V to be supplied from R70 as AMPIN to the servo motor current

amplifier. This negative input causes MTRHI to be negative which causes the linear motor to drive the head carriage in a reverse direction to the carriage stop. This keeps the heads in the guard band area.

The reason the initial seek is a modified velocity mode is due to load speed (LDSP/) becoming active. LDSP/ through inverter 7A6 produces LDSP. This disables FET 7D9 which normally acts as a shunt around limiting resistor R98. With limiting resistor R98 in the velocity circuit, the input to the summing junction (SUM) is stepped down. This provides a slow controlled driving force through op amp 6C7 to the servo motor current amplifier.

Essentially all of the positioning system circuitry is used during the initial seek. Most of the circuitry is checked out this way under a slow speed closed loop operation.

b. Velocity Mode

In this mode, the major driving force to the linear motor is supplied by commanded velocity (D to A). In the case of an initial seek or restore operation D to A, it is at maximum value. This is due to LDSP/ generating full speed (FULLSP/), which enables all the inputs to the D to A converter in the servo system control logic. In the case of a program control seek, the D to A value is determined by the number of input gates to the D to A converter that are enabled by the difference counter output.

Op amp 8D1, R90-R93, and CR9-CR14 are configured to shape the D to A input into a non-linear velocity profile with 8D1's output being positive D to A (POSDA). This sig-nal becomes the commanded velocity input to the summing junction (SUM) if a reverse (REV/) command is active, which would enable FET 7D1.

When forward (FWD/) is active, FET 7D16 is enabled and the velocity signal is supplied by negative D to A (NEGDA). NEGDA is POSDA shifted by 180 degrees by op amp 8D7, which is configured as an inverting op amp with a unity gain.

During velocity mode, either REV/ or FWD/ will be active and either POSDA or NEGDA will become DA which will go through limiting resistors R95 and R97. R97 is a potentiometer that will adjust for desired velocity. In this case, it is 55 milliseconds maximum for 561 cylinders from seek start to seek ready. Then DA goes through either FET 7D9 (program control seek) or limiting resistor R98 (initial seek or restore operation) as controlled by LDSP.

When LDSP is active, commanded velocity is at its maxi-mum value and FET 7D9 is disabled. This introduces R98 into the circuit. This resistor value is selected to provide a driving force to the linear motor so that the head carriage is moved at the rate of 1-inch-per-second.

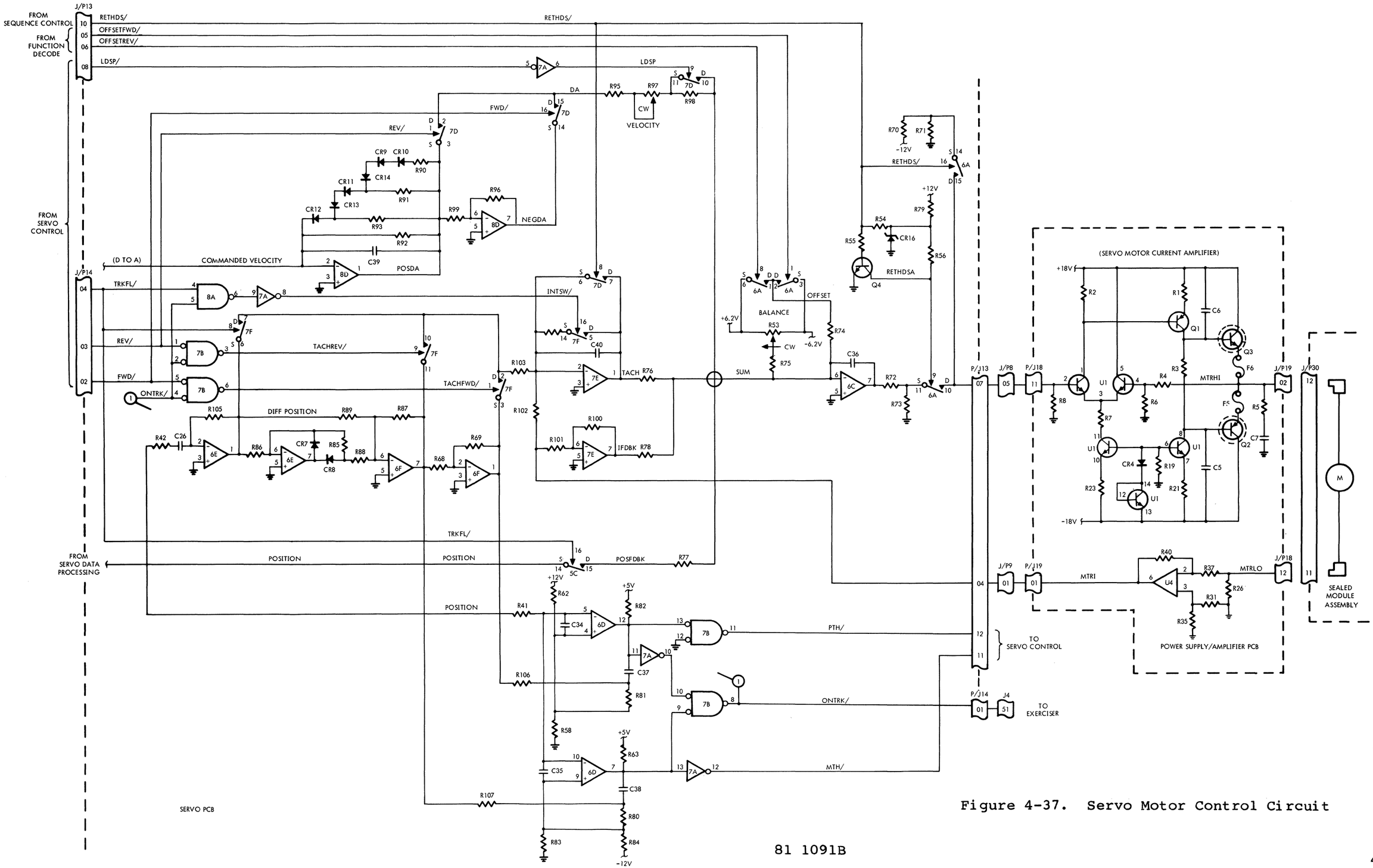


Figure 4-37. Servo Motor Control Circuit

During a program controlled seek, FET 7D9 is enabled, thus shunting R98, to allow the full value of commanded velocity to be felt at the summing junction. SUM is then inverted by op amp 6C7 with the output becoming AMPIN through FET 6A9. This provides the driving force to the motor through the motor current amplifier and starts the initial acceleration of the head carriage.

As current flows in the motor, MTRLO provides a feedback to op amp U4-6 (power supply amp).. U4 converts the current feedback to a voltage feedback with a scaled rate that becomes motor current feedback (MTRI). MTRI is fed back into the SUM junction by op amp 7E7. This feedback acts to subtract from the velocity (DA) input to SUM. This has the effect of decreasing the driving force to the motor while the motor attains its maximum speed (no more acceleration).

As current flows in the motor and the head carriage moves, the POSITION signal is generated as a sinusoidal waveform when the servo head moves across tracks. At this time TRKFL/ is not active, which disables FET 5C16 so the position feedback (POSFDBK) signal is not brought into the SUM junction. However, POSITION is differentiated by R105 and C26 which causes a 90 degree phase shift through op amp 6E1 to become DIFF POSITION. This differentiation is to convert distance versus time to velocity. DIFF POSITION is then full wave rectified by op amps 6E7, 6F7 and diodes CR7 and CR8. This provides for a positive rectified waveform on the output of 6F7, which is inverted by op amp 6F1 to become a negative rectified waveform. These waveforms are then peak detected by FET's 7F1, 7F9 and AND gates 7B3 and 7B6.

The peak detection is accomplished by on track (ONTRK/) toggling as tracks are crossed while the direction signal FWD/ or REV/ remains active during the entire motion command. This peak detected signal is then integrated by op amp 7E1 and FET 7F16 to produce a smooth dc voltage corresponding to the peaks. 7E1's output becomes the tach feedback to the SUM junction. The end result is that the tach signal provides a voltage with a scale of 140 mv/inch/sec.

Through the remainder of the motion command, velocity, tach and motor feedback are integrated at the SUM junction to provide the proper polarity and magnitude input to op amp 6C7. This causes AMPIN to furnish the proper driving force characteristics for acceleration, coast, and deceleration.

The POSITION signal also goes to comparators 6D12 and 6D7 through resistor R41. These comparators monitor threshold levels of the position signal. 6D12 provides the plus threshold detection and is active whenever the position signal is more positive than the level established by the voltage divider R58 and R62 on the plus input pin 4. The active output of 6D12 generates PTH/ through AND gate 7B11. 6D7 functions like 6D12 except that the negative

portion of the position signal is detected. This generates MTH/ through inverter 7A12.

PTH/ and MTH/ are used to generate on track (ONTRK/) when PTH/ or MTH/ are not active. PTH/ and MTH/ are also used by the servo system control logic to generate diff clocks since they are the indicators that a track is being crossed over. MTH/ is also used as the indicator of the first track after the guard band to allow the servo to be positioned to track (cylinder) 0 at completion of the initial seek, or after a restore operation. Figure 4-38 illustrates on track and threshold detection.

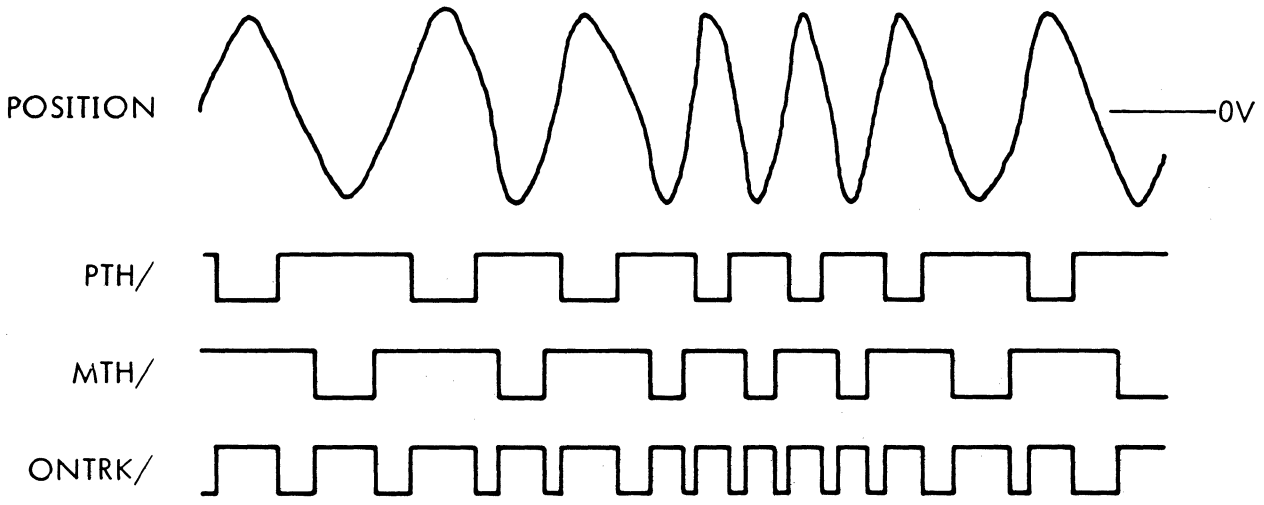


Figure 4-38. Threshold and On Track Generation

Since PTH/ and MTH/ are generated during a program controlled seek, the difference counter is counting. The number of inputs to the D to A converter decrease as it counts, which in turn decreases the commanded velocity. This continues until diff equals zero at which time there is 0 commanded velocity.

With diff equal 0 and no commanded velocity, track following (TRKFL/) mode becomes active and velocity mode is terminated.

c. Track Following Mode

When TRKFL/ is active, FET 5C16 is enabled and POSITION becomes the primary driving force to the SUM junction as the signal position feedback (POSFDBK).

The track following mode is a null-seeking operation. To accomplish this, whenever the position signal is other than 0 volts, POSFDBK provides a voltage to the SUM junction. This drives op amp 6C7 which outputs a voltage to drive the motor in the opposite direction the head carriage is drifting.

The SUM junction still has motor current feedback and tach to integrate with the position feedback signal. However, tach is generated differently in track following mode. FET 7F8 is enabled by TRKFL/. This takes the differentiated signal DIFF POSITION directly and bypasses the peak detection circuits. DIFF POSITION then becomes the TACH signal after integration by op amp 7E1.

During TRKFL/ a forward or reverse offset may be introduced to the positioning system. This offset may be helpful in recovering data. The offset is accomplished by either OFFSETFWD/ or OFFSETREV/ being active, which will enable FET's 6A1 or 6A8. With either of these FET's enabled, a positive or negative offset voltage is fed into the input to op amp 6C7.

d. Servo Motor Current Amplifier

The power amplifier converts the incoming voltage from AMPIN into a current output (MTRHI). This current may be up to 5 amps into the motor until the 3-amp fuses blow.

The MTRLO signal runs current through R26 to generate a voltage input to op amp U4. The voltage that is generated equals 1 volt per amp. The output of U4 becomes the motor current feedback (MTRI) to the SUM junction.

e. Positioning System Summary

Upon power-on, PWRINI/ is generated, which initializes the servo system control logic. This activates ST0 which activates REV/ and LDSP/. LDSP/ generates FULLSP/ which generates the maximum commanded velocity. Since TRKFL/ is not active, the positioning system operates in velocity mode, which uses commanded velocity (D to A) as the driving force for the linear motor. However, LDSP/ introduces a limiting resistor (R98) into the velocity circuit so that the driving force created is 1-inch-per-second of head carriage movement.

During power-on the heads are located in the outer guard band area. As soon as the discs are spinning rapidly enough for the outer guard band to be detected, OGB/ is activated. OGB/ active deactivates ST0 and activates ST1. This generates FWD/ and LDSP/. Speed is detected, the carriage lock is released, and the head carriage moves forward at the rate of 1-inch-per-second. This movement continues until OGB/ and MTH/ both go inactive. During PWRINI/, ODD/ is reset. This selects the output of op amp 5D7 as the position signal. Referring to Figure 4-36,

this means that the position signal goes negative (which generates MTH/) at outer guard band one track -1.5 and the signal remains negative until the boundary between servo data tracks is +0.5 and +1.5. This keeps MTH/ active during this entire time.

When OGB/ and MTH/ both go inactive, ST1 is deactivated and ST2 is activated. This deactivates FWD/ and LDSP/ and activates TRKFL/ and the 3.5 millisecond seek ready timer.

The positioning system now goes into track following mode, with the position signal as the primary driving force for the linear motor. The motor control circuit will now use the position signal to find a null between servo data tracks +0.5 and +1.5. This location equals read/write data track 000, which means that the heads will be located at cylinder 000.

The 3.5 millisecond timer is a delay to allow the positioning system to become settled on track before generating seek ready. Upon time out of the timer, both SEEK END and SKRDY are generated to notify the user via the output interface that the drive is ready to accept a command. This is assuming that there are no error conditions.

A restore operation works identically to a power-on first seek except that the heads are driven in reverse from the data tracks into the outer guard band during ST0 time.

With the drive on track and seek end and seek ready reported, a program controlled seek operation may be done.

For a program seek, the desired cylinder value is placed on the BUS. This value is compared with the CAR (reset to 000 by PWRINI/ or RESTORE/) by the subtractor to compute the difference. The subtractor logic has a carry out (COUT) if forward direction is necessary. If there is no carry out, then reverse direction is indicated.

After the subtractor logic has had time to compute the difference, SETCYLTAG is activated. SETCYLTAG is clocked into the command sequencer by 4.8 MHz. The first active output of the sequencer clocks the COUT bit into the overflow (OVF) F/F. The OVF bit goes back to the subtractor to complete the difference calculation.

The second step of the sequencer generates set difference counter (SETDIF/), which clocks the output of the subtractor logic into the difference counter. The output of the difference counter then establishes the commanded velocity by the D to A converter.

The third step of the sequencer generates SETCAR which clocks the desired cylinder value from the BUS into CAR. SETCAR also

clocks the OVF bit into the direction (IN) F/F and goes to error detection to allow an illegal cylinder check.

The fourth step of the sequencer generates seek start (SKSTRT) which (1) clocks the CAR001 bit into the odd/even F/F, (2) starts a 3 millisecond no motion seek delay, (3) activates ST3 provided the difference is not zero and there are no seek errors, and (4) deactivates ST2.

ST2 going inactive switches the positioning system from track following mode to velocity mode. Commanded velocity and FWD/ or REV/ now provide the magnitude and polarity of the driving force to the linear motor.

As the motor starts movement of the head carriage, feedback is brought into the SUM junctions from motor current and a peak detected position signal (TACH). The SUM junction integrates its various inputs to provide the proper acceleration, coast, and deceleration curve to the motor. This allows the heads to get to the desired cylinder as fast as possible without overshooting the desired cylinder.

When the heads are moving, the servo head provides a signal that becomes a sinusoidal waveform as the position signal from the head crossing servo tracks. This position signal goes to the threshold circuit where at predetermined threshold points the waveform generates positive and minus threshold signals (PTH/ and MTH/).

PTH/ and MTH/ go to the difference clock circuit, which was preset by IN (direction) and DIFF001/ to establish which threshold signal will be used to generate difference clocks (C/DIFF/). For each desired threshold signal a C/DIFF/ pulse is generated. This clocks the difference counter up toward its maximum value as long as ST3/ is active and difference equal zero (DIFFZERO) is not active.

As the difference counter is counted, there are less active outputs. This in turn causes the D to A output (commanded velocity) to decrease, thus decreasing the driving force to the motor.

The velocity mode continues until the difference counter is counted to its maximum value (all registers set) at which time a carry out is generated from all three IC's of the difference counter. This generates DIFFZERO, which shuts off the C/DIFF/ AND gate and activates ST2 while deactivating ST3.

ST2 active generates TRKFL/ and starts the 3.5 millisecond seek ready delay. TRKFL/ active terminates velocity mode and activates track following mode, which makes position feedback (POSFDBK) the primary driving force. The servo motor control

circuit operates to find a null in the position signal which will not produce any threshold signals. With no threshold signals active, ONTRK/ is active and the positioning system continues to maintain a null about the center between two adjacent servo tracks.

When the 4.5 millisecond seek ready delay times out, SEEKEND and SKRDY are activated and reported via the output interface. This indicates that the drive has completed the commanded seek operation and is now ready for further commands.

Sector Generation

The sector generator logic consists of 12 switches (one and one-half dip switches), 3 synchronous 4-bit binary counters, 1 D latch, 1 inverter and 1 OR gate (see Figure 4-39).

The sector generator may be preset for sector lengths, from 1 byte to 4096 bytes, as determined by the setting of the switches. The clock for the counters is 1.2 MHz from the positioning system. This clock is 19 MHz divided by 16, which means each clock time is equal to one byte time. Since the counter works as an up-counter, the count to be loaded into the counter is the maximum (4096) minus the desired number of bytes per sector.

The following discussion assumes 256 bytes-per-sector. Since there are 20,160 bytes around one track, this will allow 78 full sectors with a remainder sector of 192 bytes.

First, the switches are set to load a decimal value of 3840 (4096 minus 256) into the counters. Switches S2-1, 2, 3, 4, 5, 6, 7, and 8 are on and S3-1, 2, 3, and 4 are off. The switches that are on equal one less than the desired count.

Upon power-on and after the discs are spinning at a speed sufficient for the positioning system to detect INDEX/, this signal is brought into the load (LD) inputs of the counters via OR gate 14E8. At the next clock (1.2 MHz) time, the counters are loaded. After INDEX/ goes inactive, each clock input will advance the counter by one until there is a carry out (CO) of the final stage (14H15). With a carry out of the last stage, latch 15E9 is set and SECTOR is active. SECTOR is active for one clock time since the carry out of the final stage goes through inverter 14D11 and OR gate 14E8 to prime the load input. The next clock pulse reloads the counter to allow counting the next sector length.

This counting, carry out of final stage, reload count continues until the next INDEX/ pulse which starts the entire sequence over again. The fact that the 79th (remainder) sector is of a different number than the other sectors does not disorient the counter.

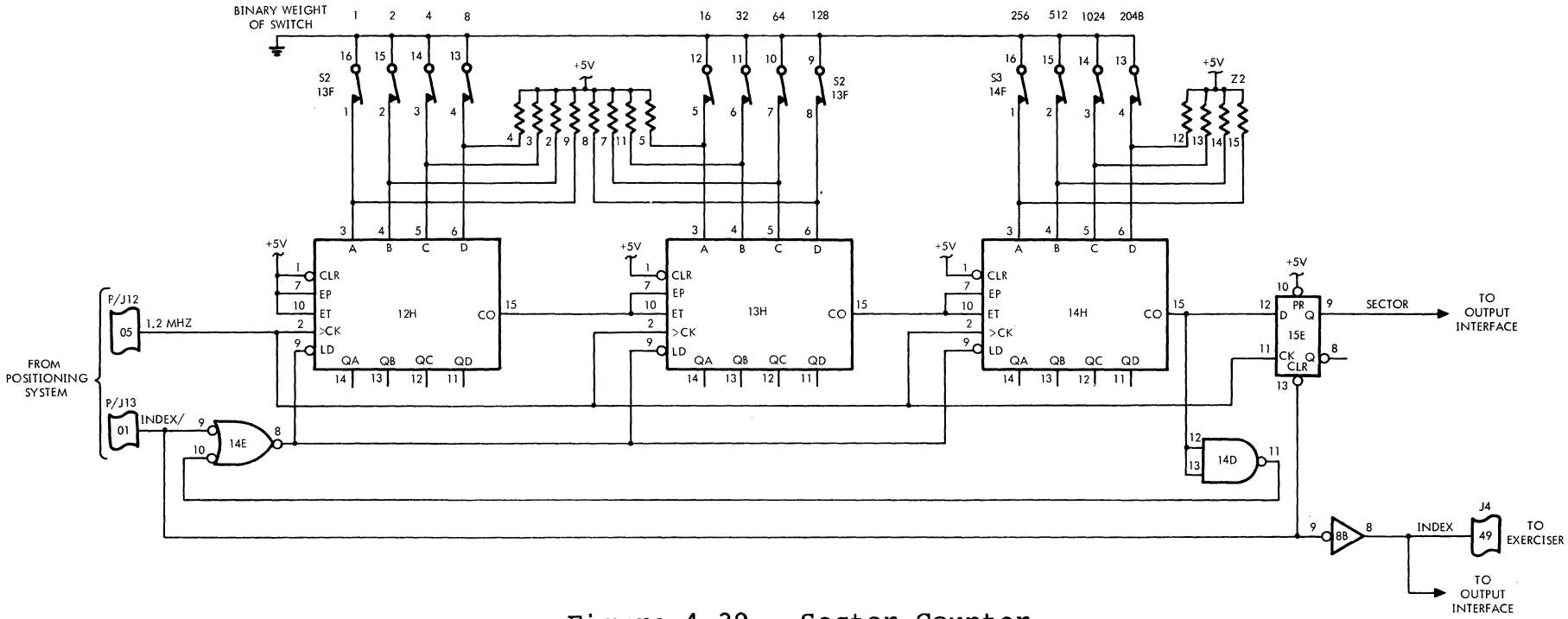


Figure 4-39. Sector Counter

The SECTOR output is sent to the output interface to allow the connecting control unit to keep track of locations around the track. Since the inputs to sector generation are derived from the positioning system all the time the discs are spinning, regardless of track following or velocity mode, the system constantly remains abreast of locations.

Read/Write System

The read/write system responds to commands from a controller via the input interface and function decode logic. The read/write system provides the means to record (write) or retrieve (read) digital data to/from a specified track on a rotating disc. It is divided into three functional circuits; (1) head selection, (2) write circuit, and (3) read circuit as shown in Figure 4-40.

1. Recording Format

The Reflex II uses a modified frequency modulation (MFM) code for recording on a disc while receiving/transmitting non-return to zero (NRZ) data at the input/output interface. This format has the following rules and conventions:

- Start writing with a field of "0's."
- Write data must be synchronized to write clock.
- Write clock to be active at least two data-bit cell times prior to write enable.
- Data-bit cell time is 105.4 nanoseconds.
- Data zero bit = flux transition at the beginning of a data cell boundary.
- Data one bit = flux transition in the middle of a data cell time.
- No flux transitions are allowed at a "01" or "10" boundary.

As the discs rotate, data is recorded/retrieved one head at a time in a circle on a disc surface. Each circle of recorded data is referred to as a track.

The REFLEX II may have either 2, 6, 10, or 14 movable read/write heads and a fixed-head-per-track option which provides 60 fixed read/write heads. Correspondingly, there may be 1, 2, 3, or 4 discs providing 1, 3, 5, or 7 recording surfaces with two heads (inner and outer) per surface. For the movable heads, there are 561 distinct locations (circles) for each head on each

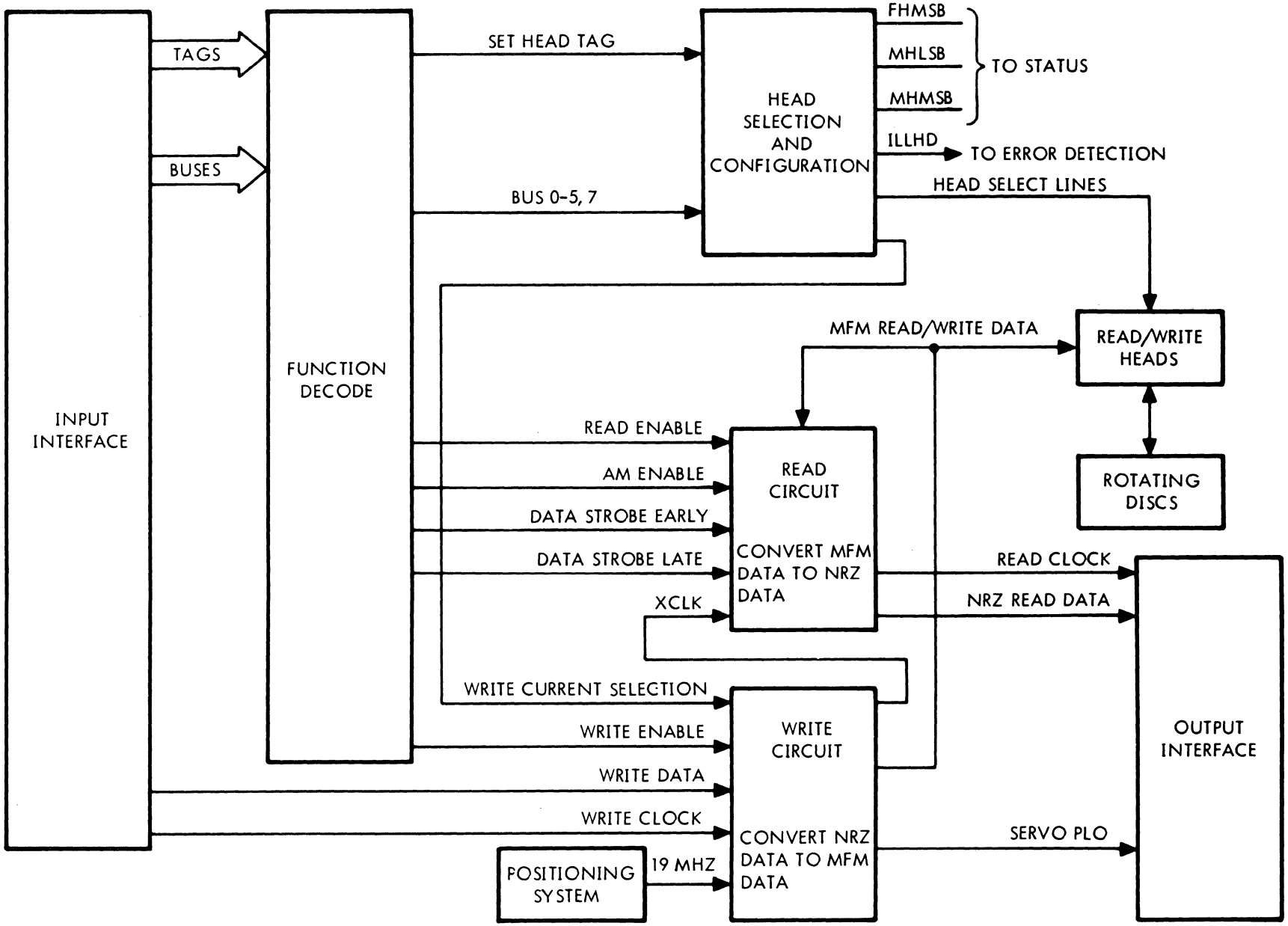


Figure 4-40. Simplified Block Diagram, Read/Write System

surface. Since there are two heads per surface, this provides 1122 circles (tracks) per surface.

All heads in the same vertical plane comprise a cylinder. All of the head assemblies are mechanically connected to a single moving mass called the carriage. Due to this mechanical bond, all of the movable heads move in unison and maintain their same relative vertical positions to each other. This would imply that there are 1122 cylinders per surface, which is true; however, the tracks are divided by two, for each head on the surface, to comprise an inner and outer group of cylinders with two separate vertical groups of heads. Therefore, there are 561 inner cylinders (all odd numbered heads) and 561 outer cylinders (all even numbered heads) with each group of heads staying within their own boundaries. This means that to select a specific track, both a cylinder address and a head address must be specified.

Figure 4-41 presents the R/W head arrangement, illustrating two heads per surface and two vertical groups of heads with one head from each group (cylinder) on each surface. Also noted is that there are either 2 or 4 R/W heads per R/W head assembly arm, with all of the arms being connected to a single movable carriage. This provides for all of the heads to move in unison and to all be positioned at the same cylinder. Then the desired head may be selected to allow writing or reading on the selected track (selected circle on one surface).

2. Head Selection

Figure 4-42 presents the circuitry for head selection, illegal head address detection, and head configuration status. 7C is the head address register (HAR). Bus bits 0-5 and 7 are clocked into the latches by the signal SETHDTAG. This happens whenever the controller desires a different head selection. The controller transmits the desired address on the bus lines (BUS0 = least significant bit) and then issues a set head tag. This information is then stored in HAR (7C) until either the next set head tag or a SKINIL/ (power initialize or a restore operation).

The outputs of HAR are sent to the exerciser (J4), the head decode logic (via J/P 10) and the illegal head detection logic.

a. Illegal Head

The illegal head detection logic uses a 4-bit magnitude comparator (7D) to compare the HAR output to the selected configuration (7E and S1). S1 contacts 6, 7, and 8 represent the head configuration of the unit. Contacts 6 and 7 are used for the moving head configuration (both closed = 2 heads, 7 open and 6 closed = 6 heads, 6 open and 7 closed = 10 heads, both open = 14 heads), while number 8 contact is for the fixed head-per-track

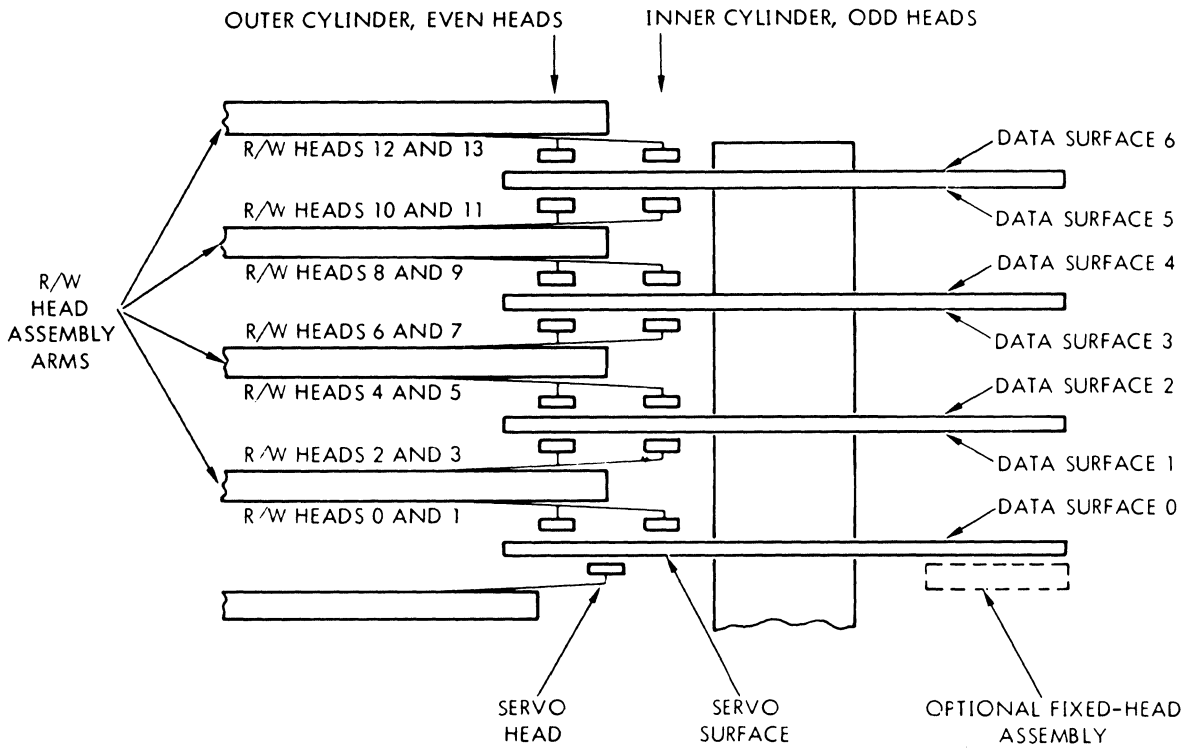


Figure 4-41. Reflex II R/W Head Arrangement

option (closed = fixed heads, open = no fixed heads). The outputs of 7E reflect the A inputs when fixed head select (FXHDSEL) is inactive and the B inputs when FXHDSEL is active.

Comparator 7D compares the HAR outputs to the configuration outputs. As long as 7D's A inputs (HAR) are less than 7D's B inputs (configuration), inverter 6F8 will be low. However, if the A inputs are equal to or greater than the B inputs, 6F8 will be high and assuming FXHDSEL is inactive, OR gate 8F, inverter 6F12 and OR gate 11E will be satisfied and an illegal head (ILLHD) indication will be transmitted to the controller via the error detection logic. When FXHDSEL is active, AND gate 7F must be satisfied by HAR 32, HAR 16, and 7D A inputs equal to or greater than 7D B inputs. An illegal head condition will not allow a write operation to occur.

b. Head Decode

The signals that go to J/P15 are for movable heads, while the signals that go to J/P17 are for fixed head selection. For discussion purposes here, it will be assumed that there are 14 movable heads only.

As mentioned earlier, there are normally 4 R/W heads on each head arm assembly (only two heads on last arm assembly). This means that the final stage of head selection is done on the head

arm assembly. The decoder on the head arm assembly requires three address lines to select one of four heads. These address lines are one chip select line and two head select lines. The chip select line enables the logic on the head arm assembly to decode the two head select lines as binary input. This provides for four possibilities. There are four head arm assemblies, each having a unique chip select input and four R/W heads per arm assembly (two R/W heads on last arm assembly). The two head select lines go to all of the head arm assemblies, but are decoded only by the arm assembly with an active chip select line.

HAR 04 and HAR 08 are decoded to provide the four chip select lines (CS1, CS2, CS3, and CS4) as conditioned by FXHDSEL being inactive. This is accomplished by inverters 3D2, 3D4, and 3D12 and AND gates 3E3, 3E6, 3E8, 3E11, 2E3, 2E6, 2E8, and 2E11. HAR 01 and HAR 02 provide the head select lines (HS1 and HS2) through AND gates 1D12 and 1D13. A matrix of movable head selection decode is presented in Table 4-4.

TABLE 4-4

MOVABLE HEAD SELECTION DECODE

					HAR 01 = HS1	I	A	I	A
					HAR 02 = HS2	I	I	A	A
HAR 04	HAR 08								
I	I	=	CS1	=	Head Selected	0	1	2	3
A	I	=	CS2	=	Head Selected	4	5	6	7
I	A	=	CS3	=	Head Selected	8	9	10	11
A	A	=	CS4	=	Head Selected	12	13	X	X

I = Inactive
A = Active

The chip select lines are active low (0V) and inactive high (+6V). The head select lines are MECL logic levels, active = -1.8V, inactive = -0.8V.

HAR 01 and FXHDSEL/ also go to the write circuit for write current selection.

3. Write Circuit

The write circuit will perform the following major functions:

- Convert NRZ data to MFM data.
- Transmit a servo clock (SRVOPLO) to controller.

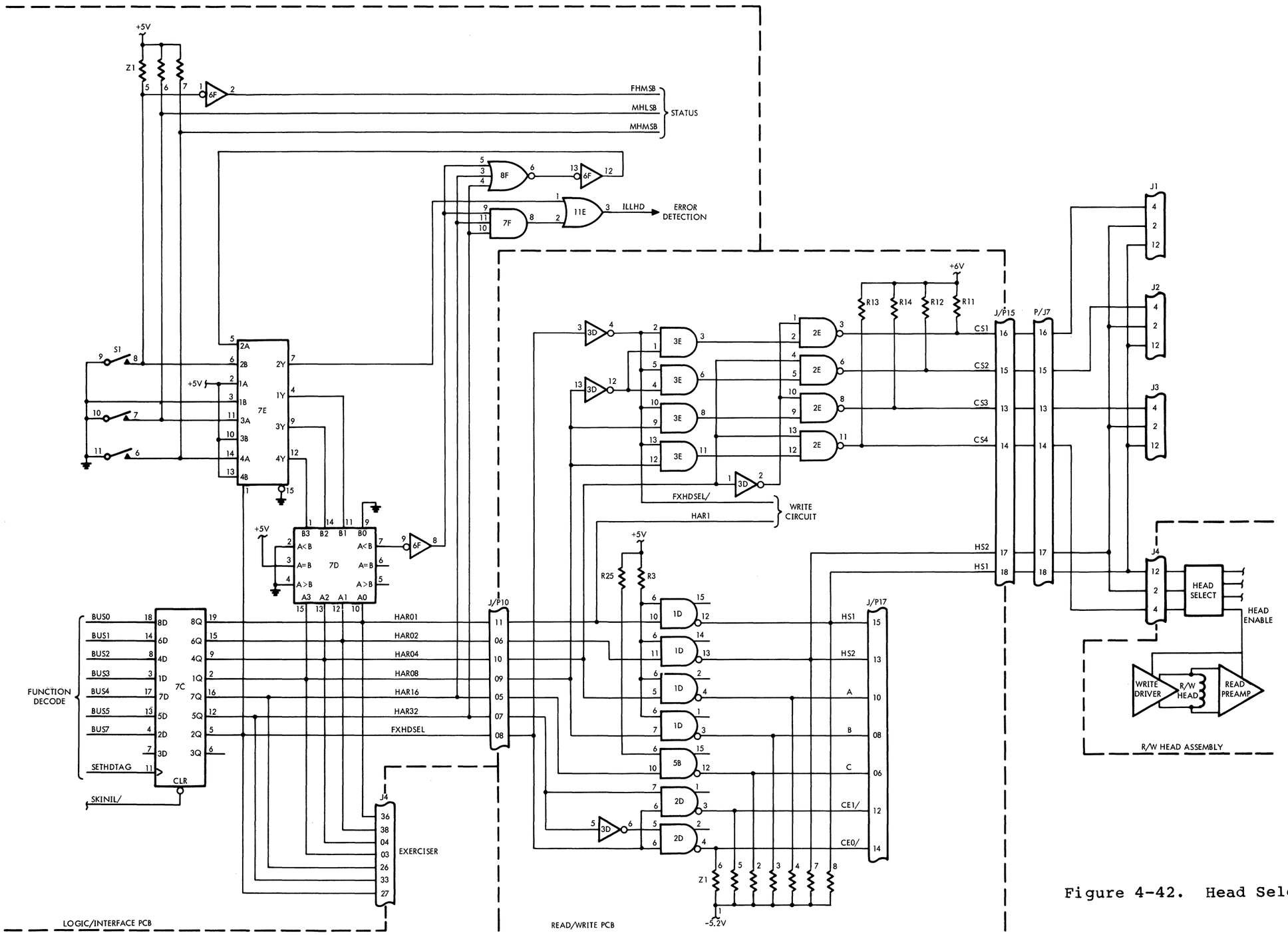


Figure 4-42. Head Selection Circuitry

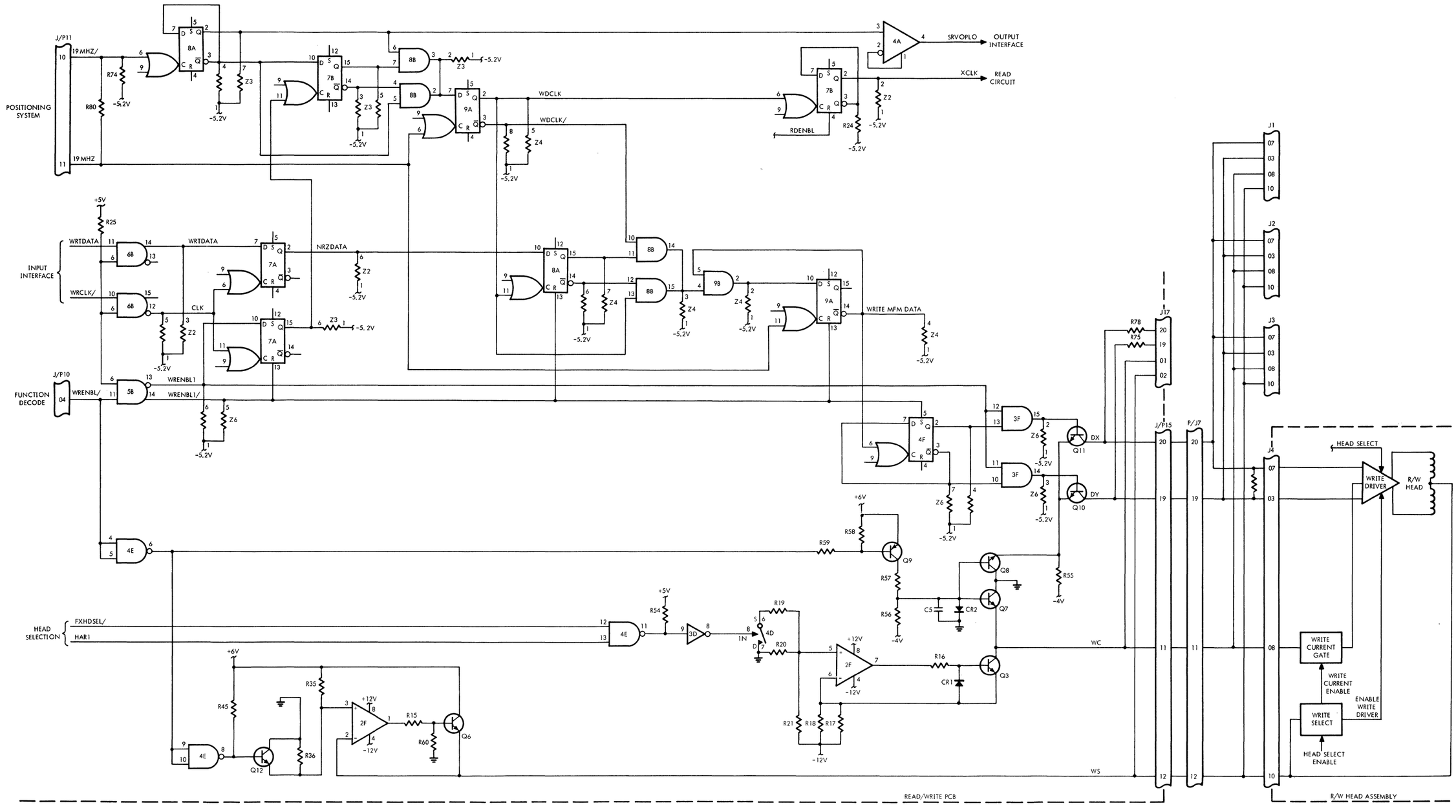


Figure 4-43. Write Circuitry

- Generate a write clock for synchronization.
- Supply write current to R/W head.
- Change the write current for inner and outer cylinders.

Prior to performing a write operation, the following must have occurred:

- Drive is selected.
- Desired head is selected.
- Write enable (WRENBL/) is activated.

Figure 4-43 presents the write circuitry and Figure 4-44 presents a timing diagram of a write operation.

The write data (IWRDATA, IWRDATA/) and write clock (IWRCLK, IWRCLK/) lines are received differentially by the input interface at which point they become single ended signals. Received data is NRZ data which is then converted by the write circuitry into MFM data prior to being recorded on the disc(s). The write clock should be a mirror image of the servo (postioning system) phase-locked oscillator (PLO) which is transmitted from the drive to the controller.

a. Enabling R/W Head Write Driver and Current Source

The write enable (WRENBL/) signal is decoded by the function decode logic from a combination of control tag, bus 0, and no fault conditions. The WRENBL/ signal drives an open collector AND gate (4E6), which in turn drives 4E8, turning off transistor Q12. This allows the positive input to 2F1 to become more positive than the negative input, causing 2F1 to go high and turn on transistor Q6. Q6 on provides the write select (WS) voltage of +3.5V $\pm$0.3V, which is one of the enabling terms for the write driver on the R/W head assembly. Q6 on also provides a center tap voltage for the R/W head coil. The WS signal is a 0$\pm$0.1V when WRENBL/ is inactive. 4E6 also drives Q9 and turns it off when WRENBL/ is active. This then turns off transistors Q7 (write current drain) and Q8 (write data lines drain).

Turning off Q7 allows Q3 to supply write current (WC) to the R/W heads. The amount of current to be sourced is dependent upon the voltage applied to the positive input to op amp 2F7. The amount of voltage is determined by FET 4D, either paralleling or not resistors R19 and R20, which will change the value of the voltage divider formed with R21. FET 4D is controlled by AND gate 4E11 from the signals HAR1 and FXHDSEL/, which come from the head selection circuit. When either FXHDSEL/ is active or FXHDSEL/ is inactive and HAR1 is inactive, 4E11 will be high,

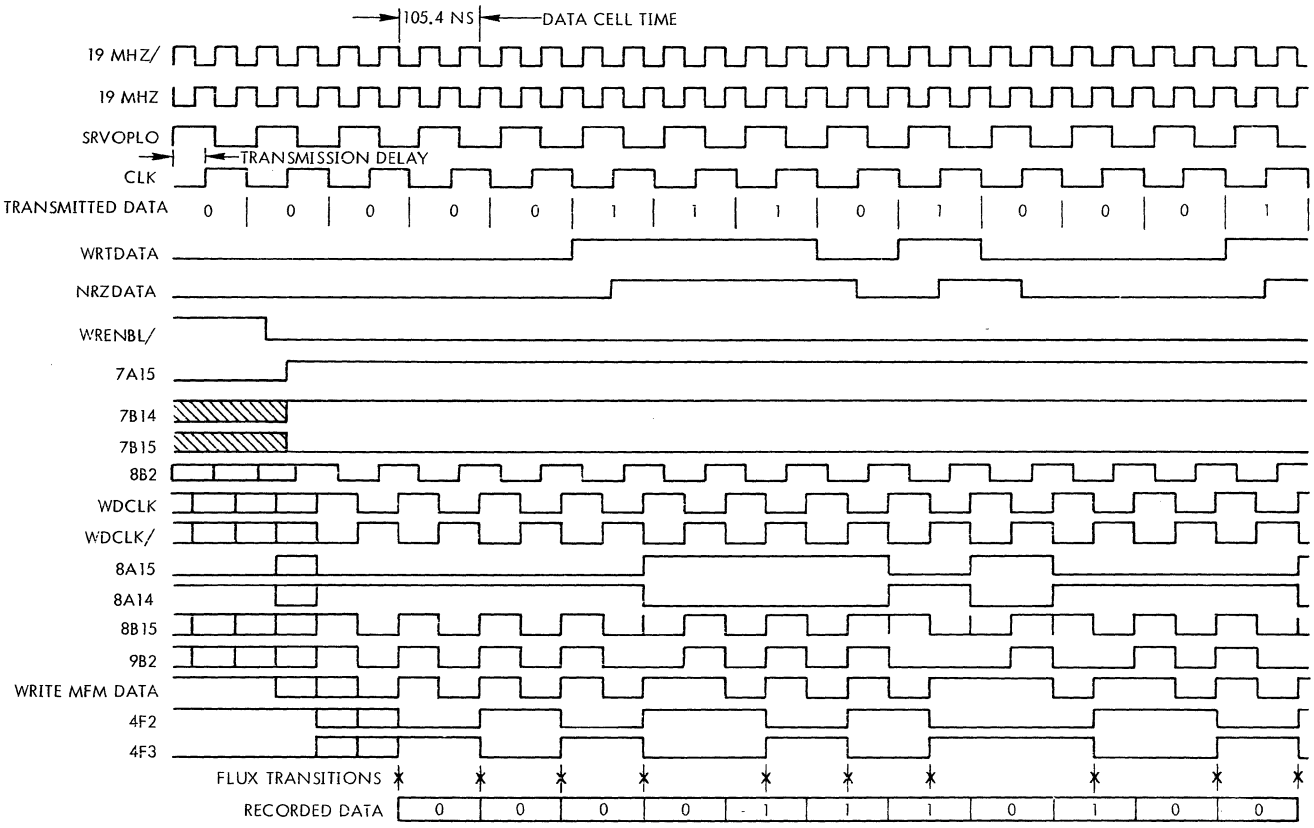


Figure 4-44. Timing Diagram

which in turn causes the output of inverter 3D to be low. This will enable FET 4D, which causes R19 and R20 to be parallel to produce the most positive voltage to the plus input of 2F7 (relative to the minus input). This causes the output of 2F7 to be more positive, allowing Q3 to source more current. The foregoing is the condition for the outer heads (even movable or all fixed heads). Under this condition 40 ma peak current is provided.

If HAR1 is active while FXHDSEL/ is inactive (indicates odd movable heads which comprise the inner group of heads), then FET 4D will not be enabled, which will unparallel R19 and R20. This will cause a reduction in the output of 2F7 so that Q3 only provides 35 ma peak current.

b. Writing Data

To write data at the proper frequency, the servo phase lock loop is brought into the write circuit as 19MHz and 19MHz/. This reflects the speed of the rotating disc and produces the signal SRVOPLO which is transmitted to the controller to be used as the controller's write clock. This in turn is retransmitted back to the drive as WRCLK. The reason for this loop is to keep the entire data path in sync with the rotational speed of the disc(s). This is also used for internal resynchronization and to develop the proper clock transitions to convert NRZ data to MFM data for recording on the disc.

When WRENBL/ becomes active an automatic phasing circuit comprised of AND gates 8B2, 8B3, flip-flops (F/F) 7A15, 7B15, and 9A2 is enabled to provide for resynchronization. This is accomplished by CLK clocking 7A15 with WRENBL1 active. This in turn clocks 7B15, allowing F/F 9A2 to be resynchronized on the next positive going pulse of 19MHz, which resyncs the internal clock pulses (WDCLK and WDCLK/). These clock pulses will now permit the proper phasing of data transitions.

WRTDATA is now clocked through F/F 7A2, becoming NRZDATA. It is then clocked through F/F 8A15 by WDCLK with the result being that 8A15 will be high if the NRZ data is a one and 8A14 high if the NRZ data is a zero. AND gate 9B2 and F/F 9A15 remove the glitches developed by exclusive OR gate of 8B14 and 8B15 with the output of 9A15 being MFM data that provides the clock for data transitions at the proper times.

F/F 4F2 divides the MFM data to alternately switch transistors Q11 and Q10 off and on through gates 3F14 and 3F15. This switching action of current in the selected R/W head creates a magnetic field by the head, which is an electromagnet. The pole piece of the R/W head has a high reluctance gap while the disc surface has a ferrous oxide coating. The disc surface is easily magnetized as the air gap between the head and disc surface provides a low reluctance path to the magnetic field. As the head is driven by current, the magnetic field that builds up bridges the low reluctance gap of air between the head and disc surface. This induces the field into the oxide surface of the disc, which becomes magnetized in the direction induced. The polarity of north and south poles is alternated by the switching action of Q10 and Q11 while the write coil is center-tapped.

This coupling of the magnetic field on to the disc creates magnets on the disc surface with each flux change (north/south pole switch) representing either 1, 1-1/2, or 2 data bits of information. This recording technique generates frequencies commonly referred to as 2F, 1-1/2F, and 1F, respectively. This is illustrated in Figure 4-44, which denotes that a "101" (or "010") alternating bit pattern produces a flux transition at the

lowest frequency (1F). A "100" or "011" pattern produces flux transitions for the first two bits at a rate 50 percent greater than 1F, thereby becoming 1-1/2F. A consecutive string of "0's" or "1's" produces flux transitions at twice the rate of an alternating bit pattern, thereby becoming 2F (twice the basic recording frequency). This triple frequency of recording is one of the earmarks of the MFM code.

In addition to the foregoing, F/F 7B2 on Figure 4-43 sends clock pulses to the read data separator circuitry whenever the unit is not reading.

4. Read Circuit

The read circuit performs the following major functions:

- Causes the selected R/W head to become a magnetic field sensor.
- Amplifies and shapes magnetic field (playback signal) induced in the R/W head into a signal usable by the data decode circuitry.
- Generates a self-clocking signal to separate the data and define the data at all times.
- Converts the MFM data recorded on the disc(s) into NRZ data to be transmitted from the drive to the controller.

Prior to performing a read operation, the following must have occured:

- Drive is selected
- Desired head is selected
- Read/ is enabled

Read/ through the generation of RDENBL, RDENBL/, and RDENBLDLY/ turns off XCLK, enables the data path to the data separator and enables the MFM to NRZ conversion circuit.

Figure 4-45 presents the read circuitry and Figure 4-46 presents a timing diagram of the data separator.

In the read mode the north and souh pole transitions of the magnetic bits recorded on the disc surface induce voltage transitions in the coil of the R/W head as the disc surface passes by the head. The induced voltage flucuations are amplified by circuitry on the R/W head assembly. R10, R31, and R33 control the gain of the final stage amplifier on the R/W head assembly. The gain remains constant but the amplitude of the signal varies

R/W HEAD ASSEMBLY
R/W HEAD
HEAD SELECT
HEAD ENABLE
DY
DX
J1
J2
J3
J4
J/P7
P/J15
J17
R75
R78
+6V
C35
R42
R41
Q5
Q2
Q4
Q1
R31
R33
R10
R34
C6
R44
R43
R39
R40
-12V
C4
C10 RDATAY/
C15 RDATAX/
L2
L4
L3
L6
C11
C12
C14
C13
R67
R68
R69
RDFILY/
RDFILX/
C21
C24
+6.2V
6F
-6.2V
C20
C29 DIFFRDATAY/
C28 DIFFRDATAX/
R76
R73
C27
-1.3V
7F
Z8
Z9
-5.2V
8F
C34
RB5
RB6
8E
Z7
9E
FROM WRITE CIRCUIT
WDCLK
7B
XCLK
R24
Z2
Z10
LIMDLY
9F
C33
RB3
RB4
RB1
PULSE WIDTH
CW
C32
XOVERDET
C23
8C
R65
R66
R64
R63
C18
C19
R89
R90
FDBK
R88
R62
R71
VR3
-9V
C26
7C
R70
R48
QUAD/
7E
VEE
VCX
7D
CX1
CX2
VCC
RDVCO
R49
C30
7Z
RDCLK
4A
OUTPUT INTERFACE
QUAD
WINDOW
ONEPLSE
ONEPLSE/
9D
RDVCO/
RDVCO
R92
8E
ONEPLSERST
Z5
8D
READDATA
RDDATA
WINDOW/
ZEROPLSE/
ZEROPLSERST
R91
READDATA/
J/P11
FROM FUNCTION DECODE
+5V
R53
R52
R25
DSEARLY/
DSLATE/
4D
R51
ODET. OFFSET
5B
R61
R50
C17
R46
R47
RDENBL
READ/
AMENBL/
6B
9B
RDENBL/
4A
4E
R30
C3
R29
R87
RDENBLDLY/
R26
TSTLKUP/
R27
R28
-5.2V

Figure 4-45. Read Circuit

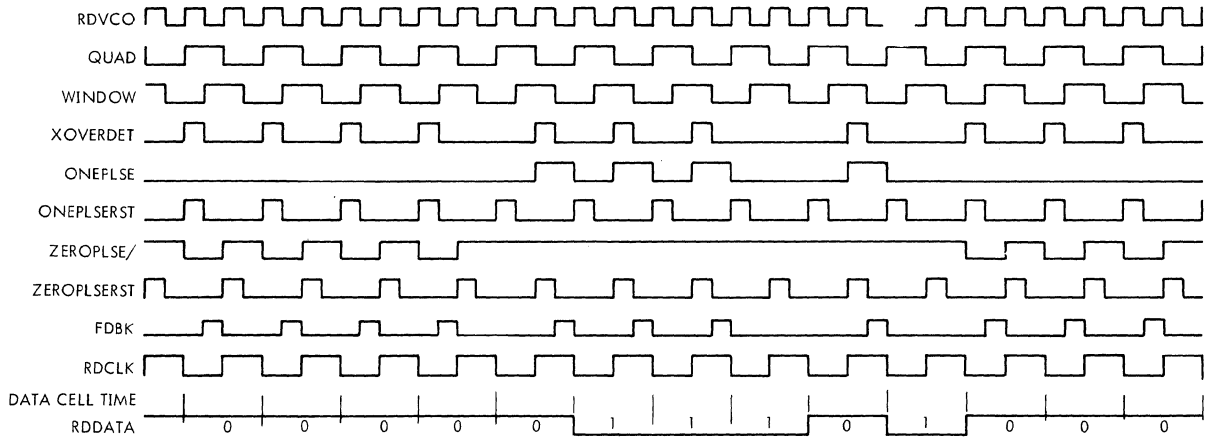


Figure 4-46. Data Separator Timing Diagram

considerably in proportion to the frequency and packing density (BPI) of the recorded data.

As mentioned in the write circuit section, there are three different frequencies used when recording on the disc, 1F, 1-1/2F and 2F. 1F is the low frequency and 1/2 of the high frequency of 2F. 1F is comprised of a stream of alternating bits (10101010) while 2F is comprised of consecutive bits of the same kind (11111 or 00000). This is demonstrated in Figure 4-47.

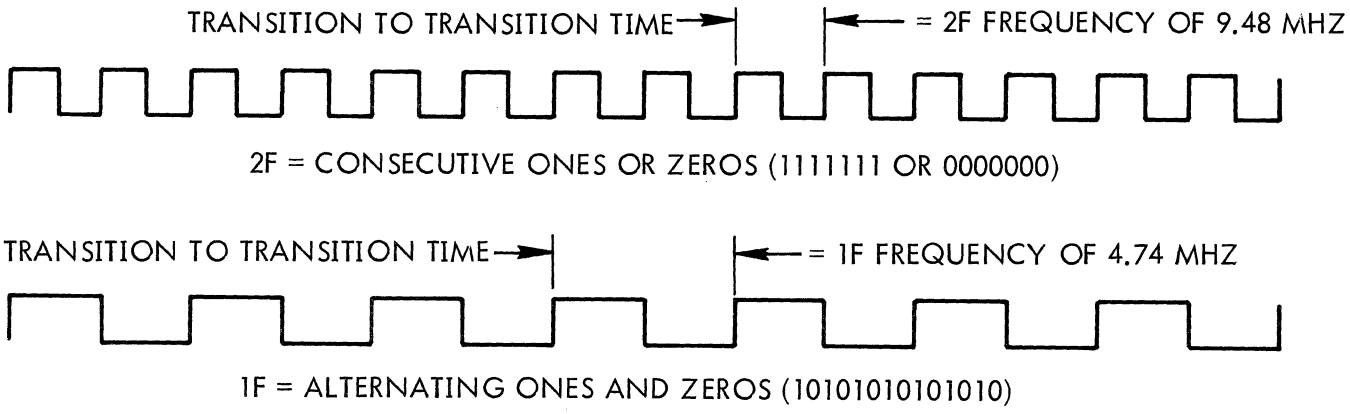


Figure 4-47. MFM Low and High Recording Frequencies

The other factor affecting the amplitude is the packing density due to the circumference of the disc changing from outside tracks to inside tracks. The overall effect of these factors is such that the amplitude of 2F data at cylinder 560 of an inner head may be only 20 millivolt peak-to-peak (P-P), measured differentially across the bases of transistors Q1 and Q2, while 1F data at cylinder 0 of an outer head will be a minimum of 130 millivolts

P-P at the bases of Q1 and Q2. These variations must be taken into account by the following circuitry to be able to differentiate valid low amplitude data from not valid high amplitude noise.

Q1, Q2, Q4, and Q5 perform the function of differential amplifiers with a total gain of approximately 15. The stream of data pulses is then ac-coupled to a four-pole filter comprised of L2, L3, L4, L6, C11, C12, C13, and C14. The filter's function is to improve the signal-to-noise ratio by attenuating high frequency noise. This filter directly couples the data to a differentiator (6F7) whose gain is controlled by C21, L5, and R68. This circuit provides a damping factor with a resonant frequency of 11.85MHz. The function of the differentiator is to shift the output so that the peak of incoming data is shifted to become the 0 volt crossover point as illustrated in Figure 4-48. This has the effect of removing the dependence on amplitude as the definition point of a flux transition (north/south pole reversal). Also the 0 volt crossover point now defines the boundaries of flux transitions.

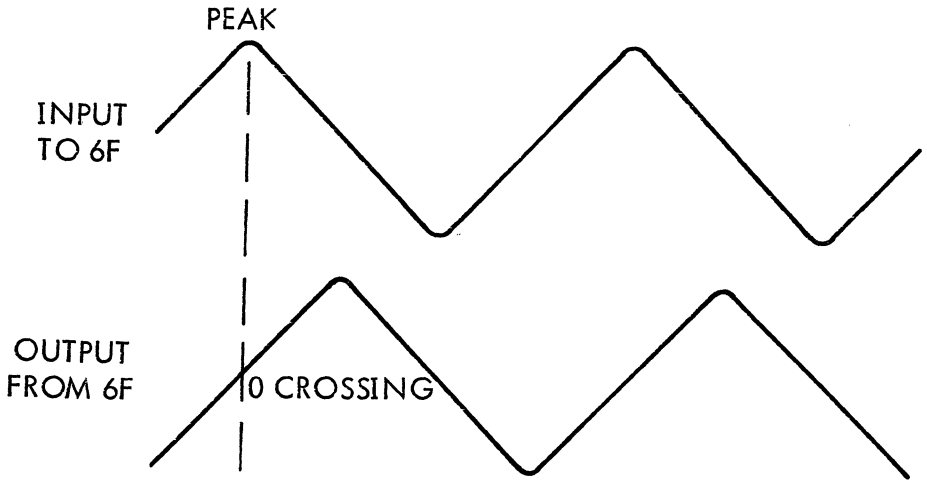


Figure 4-48. Differentiator Peak to "0" Crossing

The active differentiator output is ac-coupled to a series of gates which act as limiters and a crossover detector, which is comprised of 7F6, 7F2, and 7F14. 8F2 and 8E15 function as a frequency doubler which produces a 30-nanosecond output pulse for each transition of data. This network operates with F/F 9E15 as a filter to eliminate extra crossover transitions caused by a very good head response as illustrated in Figure 4-49.

The output of 9E15 (LIMDLY) is only enabled when RDENBL/ is active. LIMDLY drives a differential OR gate 9F2, which has an alternate input of XCLK. XCLK is active whenever the drive is not reading (RDENBL not active). This alternate input is to keep the separated data circuitry that follows operating at the 1F frequency, since XCLK is derived from the PLO frequency (19MHz)

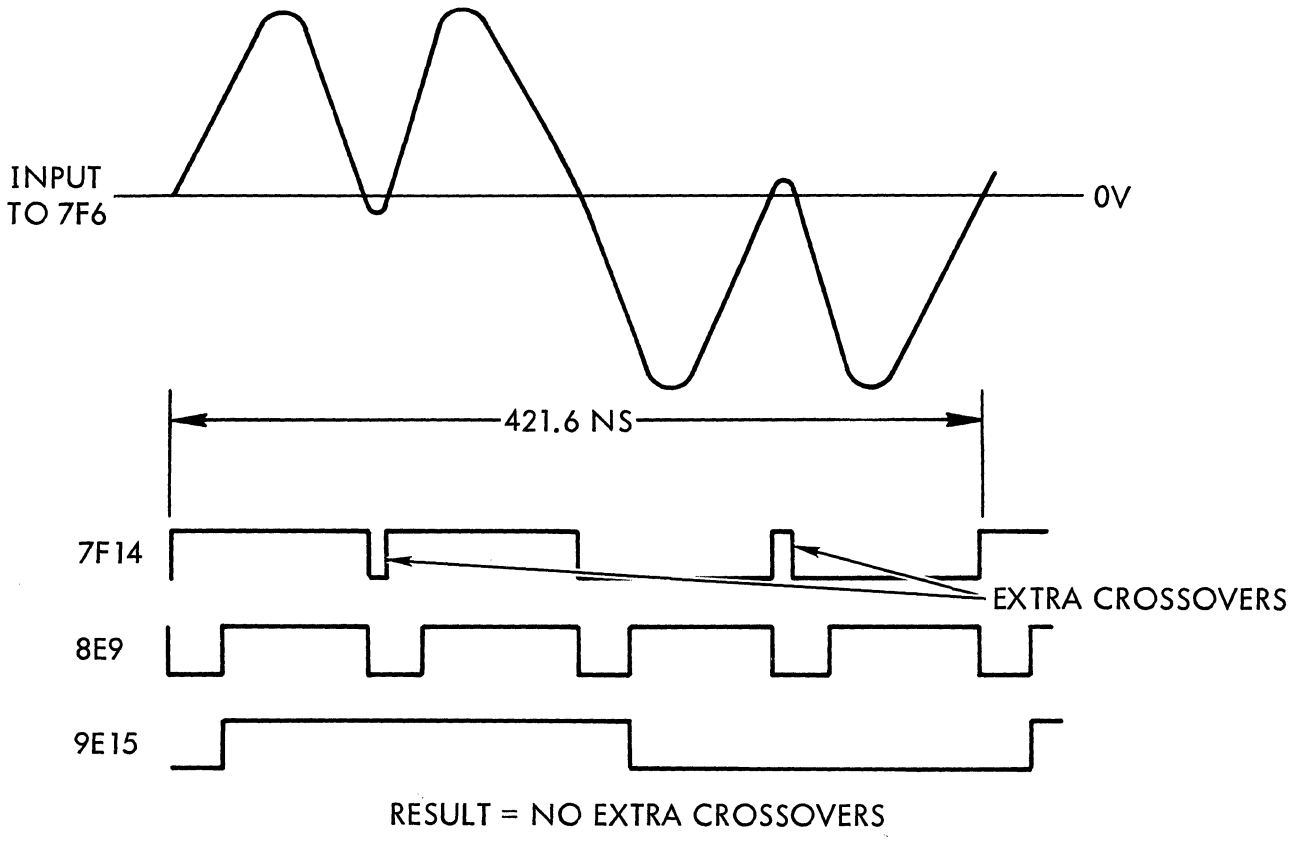


Figure 4-49. Eliminate Extra Crossovers From Very Good Head Response

divided by four. This allows the separated data circuit to operate at or near the data frequency at all times.

With RDENBL and RDENBL/ active, XCLK is shut off and LIMDLY is now gated through 8F14 and 15 and 8E10 and 11, which act as a frequency doubler. The frequency doubler's output (8E14) pulse width is controlled by potentiometer R81. While R81 provides for a variable pulse width, its function is to center the data transition (XOVERDET/) within the signal WINDOW. This function will be explained later.

The frequency doubler is buffered by 9F14, which is connected to a frequency phase detector (8C). This is the beginning of the data separator or data decoder, which is comprised of phase detector 8C, integrator 7C1, amplifier 7C7, oscillator 7D, divide by 2 F/F's 7E2 and 7E15, and feedback gates 8D15 and 8D3.

8C as a frequency phase detector requires gating that provides feedback only when there are transitions present. This is to allow it to lock to harmonics. When there is an alternating bit pattern (1010) there are transitions missing, so gates 8D3 and 8D15 degate feedback during the absence of these transitions. The phase detector reacts to any phase difference of the positive

rising edges of its inputs on pins 6 and 9 by outputing a pulse on one of its outputs (pins 4 and 12) with the pulse width proportional to the input phase difference. This output is integrated by 7C1 to provide a connection to the voltage controlled oscillator (7D) to keep it locked to the correct frequency. This is to compensate for less than perfect transition times.

While data is recorded theoretically with ideal (perfect) times from one flux transition to the next at the rate of 105.4, 158.1, or 210.8 nanoseconds (depending on data frequencies of 2F, 1-1/2F or 1F), in practice there are factors such as circuit skew, change in disc speed, difference in magnetic characteristics from point-to-point on the disc surface, etc. These variations cause actual times from one flux transition to the next to vary from ideal with the resultant time shift being referred to as peak shift.

8C and 7C1 attempt to compensate for this peak shift by 8C varying its output voltage to the input of 7C1. A reference voltage is applied to the plus input of 7C1 so that under ideal conditions the output of 7C1 is amplified by 7C7. This will provide a minus one volt level to the input of the voltage controlled oscillator (7D).

The reference level to the plus input is set by R61 (phase detector offset) so that 7C1 introduces no shift by itself when neither DSEARLY/ or DSLATE/ are active. When either DSEARLY/ or DSLATE/ are active the reference level is changed, causing a corresponding shift in time of five nanoseconds earlier or later. This is done by shifting the relative time of data transitions within the window by five nanoseconds. This will allow decoding data that has excessive peak shift.

Since the RDVCO frequency is varied by the input voltage level at 7D2, it is necessary to allow some time for settling of the input voltage when switching to RDENBL active. This settling time is necessary due to the potential phase difference that is introduced when switching from XCLK to LIMDLY. The phase difference in the input can cause large corrections to the VCO input which in turn would cause large variations in the frequency of RDVCO. The input variation is illustrated in Figure 4-50.

The MFM to NRZ conversion circuit is not enabled until after the settling time as illustrated by Figure 4-50. This is accomplished by delaying RDENBL/ for approximately 10 microseconds through 4A5, 4E3, 4C1, and 5B1 where the signal RDENBLDLY/ is generated. The delay is accomplished by the R-C network between 4E and 4C. The FET (4D) enabled by TSTLKUP/ is used for test purposes.

A preamble of zeros is necessary for the data separator to stablize and acquire correct phase lock up. The preamble is

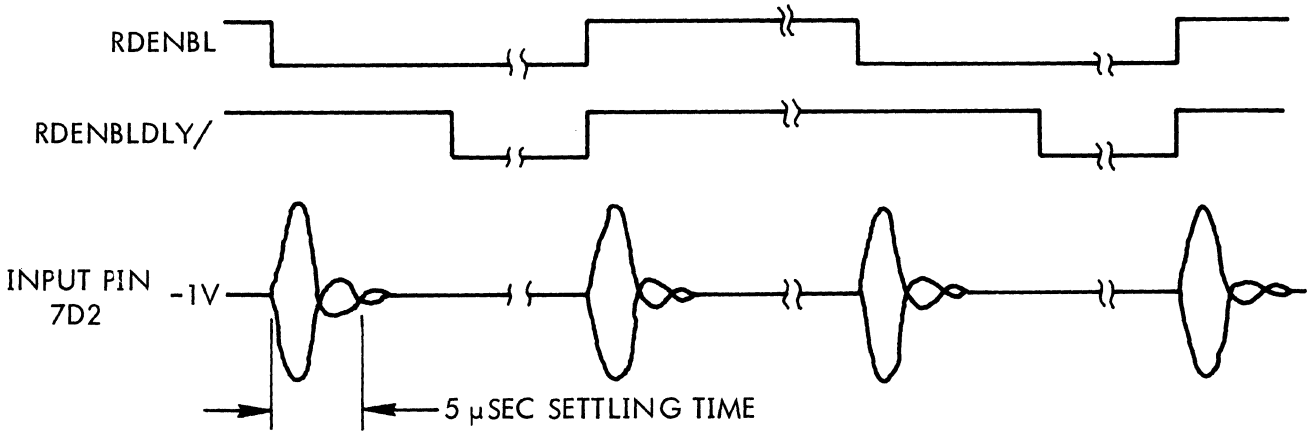


Figure 4-50. Read Phase Detection Settling Time

necessary every time there is a switch from the non-read to the read mode. The length of the preamble must start before the settling time, continue through the settling time and continue until the data separator has stabilized.

With RDVCO stable, QUAD and WINDOW will be sunk in the correct phase so that data may be correctly decoded. Assuming R81 (pulse width) to be set correctly, data can now be defined as a one or a zero by looking at the time of a data transition (XOVERDET) relative to WINDOW. Any positive transition of XOVERDET while WINDOW is positive (active) is defined as a "one." Any positive transition of XOVERDET while WINDOW is negative (WINDOW/ = positive) is defined as a "zero." If R81 is adjusted incorrectly, the foregoing definitions will flip over ones = zeros and vice versa. This happens when R81 is adjusted so that the transition of XOVERDET is adjusted too close to the edge (either edge) of its respective WINDOW (WINDOW/) signal. The correct setting of R81 is made by finding the points toward both edges of the window (points where errors are produced) and then setting the transition of XOVERDET so it is centered between the error points.

F/F's 9D2, 9D14, and 9E2 perform the function of converting the MFM data to NRZ data. 9D2 is set by transitions that are defined as "ones" while 9D14 is set by transitions that define "zeros." Under MFM code, there are always transitions for a one, while they may not be transitions for a zero, depending on what the data pattern is. Using this assumption, the READDATA F/F (9E2) only needs to look at the ONEPLSE F/F (9D2) to convert to NRZ data. This assumes that all ones are clocked in and if it's not a one, it must be a zero.

The signal QUAD defines a data cell time, with the positive going edges of QUAD defining the beginning and end of a data cell time. This allows the positive going edge of QUAD to be used as the clock to the READDATA F/F. QUAD/ is used to generate RDCLK, which means the positive going edge of RDCLK is the center of a data cell time.

RDCLK and RDDATA are sent to the output interface to be transmitted to the controller.

5. Read/Write Head Assembly

Each assembly contains either two or four R/W heads, two up heads and two down heads. Each pair is made up of an inner and outer R/W head. Each assembly has an integrated circuit that contains head decode logic, write drivers, read pre-amplifiers, and safety circuits. All but the safety circuits were discussed within the read/write system. The safety circuits are covered in Error Detection.

Error Detection

The error detection logic monitors and detects those conditions that may have an adverse effect on operation of the disc unit or may affect the integrity of recorded data. Figure 4-51 presents the error detection logic.

The error detection logic is divided into three major categories:

- Fault (unsafe condition during a read/write operation)
- Seek error (illegal seek attempted or failed to complete a motion command)
- Retract control (emergency retract condition)

1. Fault

The fault logic is primarily to detect conditions that preclude safe read/write operations (reference Figure 4-51). The conditions which produce a fault are:

- DC voltage unsafe
- R/W head circuit unsafe
- Illegal head selected
- Invalid write operation

a. DC Voltage Unsafe

The dc voltages distributed by the power supply/amplifier (+5V, ±9V, ±12V, and ±18V) are monitored on the power supply/amplifier PCB for under voltage. If any of these voltages fall below the reference level (70-80 percent) DCSAFE/ becomes inactive and latch 14A9 is set. This provides an active FAULT signal through OR gate 13A8 (reference Figure 4-51).

b. R/W Head Circuit Unsafe

Each R/W head assembly contains a circuit that monitors various conditions, which are:

- Multiple heads selected
- Write command active and R/W coil open or shorted
- Write command active and no head selected
- Write command active and write current level not correct
- Write command active and no write transitions
- Write current present and no write command

When any of the foregoing are active there will be current flow in either or both of the +6VRW, or unsafe (US) lines to the read/write PCB where three op amps (1E1, 1E13, and 1E14) and their reference and dropping resistors (R5, R6, R7, R8, and R32) monitor these lines. This produces head circuit safe (HDCKTSAFE) which is inverted through inverter 3D10.

When an unsafe condition exists, HDCKTSAFE/ will be inactive and satisfy AND gate 14D3 unless the other input to the AND gate is inactive. This leg of AND gate 14D3 will be disabled for approximately 9 microseconds at the beginning of each write command (CONTROLTAG AND BUS0) or set head tag. The purpose of these disabling windows is to allow for switching transitions that occur when switching head selection or initiating a write command.

The active output of AND gate 14D3 sets latch 14A4, which produces a FAULT through OR gate 13A8 (reference Figure 4-51).

c. Illegal Head Selected

Any time illegal head (ILLHD) is active while SETHDTAG/ is not active, a FAULT will be created through AND gate 14D8, latch 14A7, and OR gate 13A8. AND gate 14D8 is disabled during set head time to allow for logic switching in the head selection

circuit, which may produce erroneous ILLHD indications (reference Figure 4-51).

d. Invalid Write Operations

Whenever a write operation is attempted, a check is made to ensure that track following mode (SKRDY) is active, that there is no servo offset active, that read mode is not active and that write enable is active. If a write is attempted when any of the foregoing is not true, the write operation will not be allowed and a FAULT will be generated through AND gate 6H8, whose active output will set latch 14A13.

SKRDY not active would indicate a question about the location of the R/W heads, with the indication that there is either a seek error or a servo motion command in progress. OFFSET/ active indicates that the R/W heads are offset from the center of a track. In either of the above cases, a write operation would be invalid as writes are only to be accomplished when the R/W heads are located properly over the center of a track.

When READ/ is active, a write would be invalid since a common data path is used for both with no facilities for concurrent time sharing.

When WRENBLI is not active, this is an indication that the unit is to be write protected (no write allowed); therefore, a write operation is invalid.

e. Reset Fault

To reset a FAULT, either power initialize (PWRINI) from a power-on cycle or R/FAULT/ (control tag and bus 4) active will reset the fault latches (14A9, 14A4, 14A7, and 14A13) through OR gate 13E1.

When a fault is active, it will (1) be reported to the status logic to be transmitted via the output interface to the controller, (2) illuminate the fault indicator on the LED/SWITCH panel, (3) disable the ready signal (RDY) reported to the controller via the status logic, (4) extinguish the RDY indicator on the LED/SWITCH panel, (5) activate the fault/retract (FLTRET) signal to the function decode logic to disable write enable (WRENBL), and (6) activate a line for the exerciser monitor.

2. Seek Error

Conditions that produce a seek error are:

- An attempt to issue a seek command when the drive is not ready or a motion command is still in process.

- An attempt to seek an illegal cylinder address.
- A motion command has taken more than 1.5 seconds to complete (seek time-out).
- Open cable active with drive online and outer guard-band active.

Any seek error condition will cause seek incomplete status (seek end active, seek error active and on cylinder inactive) to be transmitted to the controller (reference Figure 4-51).

a. Attempted Seek While Not Ready/Motion Command in Process

AND gate 18D6 monitors for this condition. If OR gate 20E8 is satisfied (output high = active) by either not ready (RDYI/ not active) or motion command in process (SEEKDONE/ not active) when SETCAR (SETCYLTAG active) is active, AND gate 18D6 will be satisfied and set latch 15A4. Latch 15A4 produces SEEKERRORA through OR gate 13A6 (reference Figure 4-51).

b. Illegal Cylinder Address

F/F 17C6 is the illegal cylinder address flip-flop. Its D input has a group of gates (10F6, 10F8, 9F6, 12F3, and 12F11) that monitor the cylinder address register (CAR) for an address greater than 560 since 560 is the last valid cylinder address. If the output of 12F11 is high (active) when SETCAR goes inactive (clock input to F/F requires positive going edge), then F/F 17C6 will set and generate a seek error through OR gate 13A6 which in turn activates SEEKERROR/ through inverter 15B2. SEEKERROR/ goes to the positioning systems control logic to prevent the seek command from moving the carriage (reference Figure 4-51).

c. Seek Time-Out (1.5 Second Time Out)

All motion commands start a 1.5 second timer. If track following mode is not active when the timer times out, a seek error is generated by the time-out F/F 17C8. Motion commands are defined by ST3 (program seek) and ST0 (restore or first seek). Either ST0 or ST3 active causes the output of OR gate 13C11 to trigger one-shot 16C4. The $\overline{Q}$ output 16C4 goes low for the duration of time as determined by R40 and C29 (in this case, time = approximately 1.5 seconds). Since F/F 17C8 requires a positive going edge as a clock, when 16C4 times out F/F 17C8 is clocked to a state depending on its D input. Here the D input is ST2/ (track following mode). If ST2/ is not active, then F/F 17C8 is set. This generates a seek error through OR gate 13A6 and in addition activates RETCTRL/ through OR gate 16B12 and inverter 13B6. RETCTRL/ active goes to the sequence control logic to activate RETHDS/, which in turn disconnects the servo amplifier from the servo control logic and causes the carriage to retract to the outer guard band.

Even though ST0 is generated by a power-on cycle (first seek), this path will not cause a time out seek error, even if track following mode is not activated. This is due to the reset (PWRINI) which generates ST0 and is active way beyond 1.5 seconds, so that the reset overrides the time-out (reference Figure 4-51).

d. Open Cable Active While Drive Is On-Line

AND gate 11E8 monitors for this condition. Anytime OPENCABLE/ is active (cable missing or controller has a power failure) and the drive is on-line (TESTMODE is not active), AND gate 13C3 will be satisfied and if OGB/ is active, latch 15A9 will be set.

e. Resetting Seek Error

Seek error is reset by either power initialize (PWRINI) during a power-on cycle or a restore operation (control tag and bus 6) through OR gate 13E13. It should be noted that PWRINI generates ST0, which is a condition that will cause a time-out. This in turn may attempt to set F/F 17C8; however, PWRINI is active for greater than the time out (1.5 seconds) and therefore keeps the F/F reset.

Also, exerciser timer inhibit (/ETMRIHIBIT/) will reset a seek error due to a seek time-out, or will prevent this error from happening. This signal is from the exerciser.

3. Retract Control (Emergency Retract)

An emergency retract condition is generated by either

- A seek time-out seek error
- An open interface cable

a. Seek Time-Out Seek Error

As noted in the seek error writeup, retract control (RETCTRL/) can be activated by the seek time-out F/F 17C8.

b. Open Cable

Whenever OPENCABLE/ is active and TESTMODE is not active, AND gate 13C will be satisfied and generate RETCTRL/ through OR gate 16B12 and inverter 13B6. TESTMODE is only active when the exerciser is installed in the drive.

This error condition is based on the assumption that neither a controller or exerciser is connected to the drive; therefore, the carriage should be kept retracted.

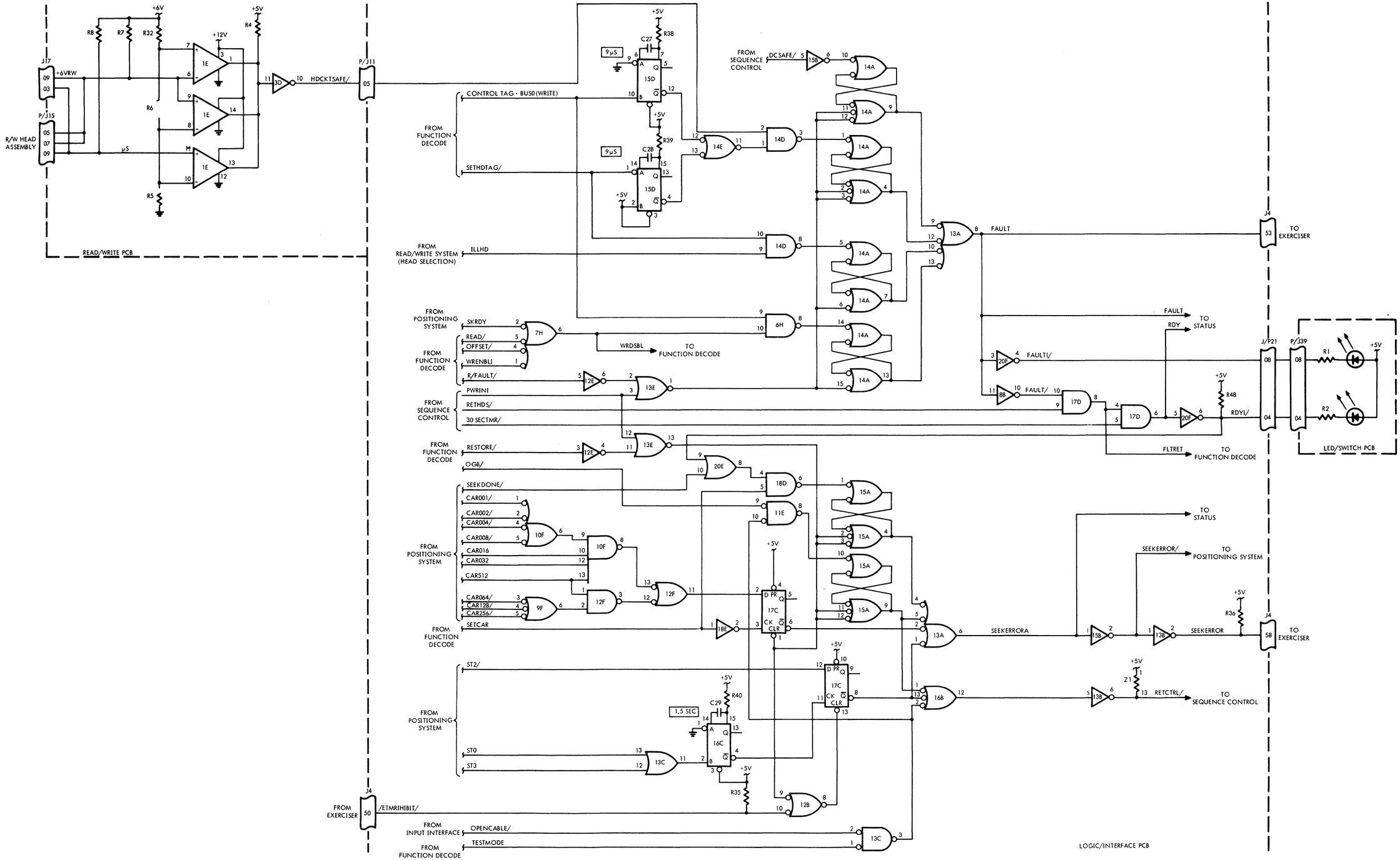


Figure 4-51. Fault Logic

Status

The status logic provides a means of multiplexing four signal lines to the output interface (see Figure 4-52). The four lines have a primary meaning (CONFIGURATION inactive) and an alternate meaning (CONFIGURATION active).

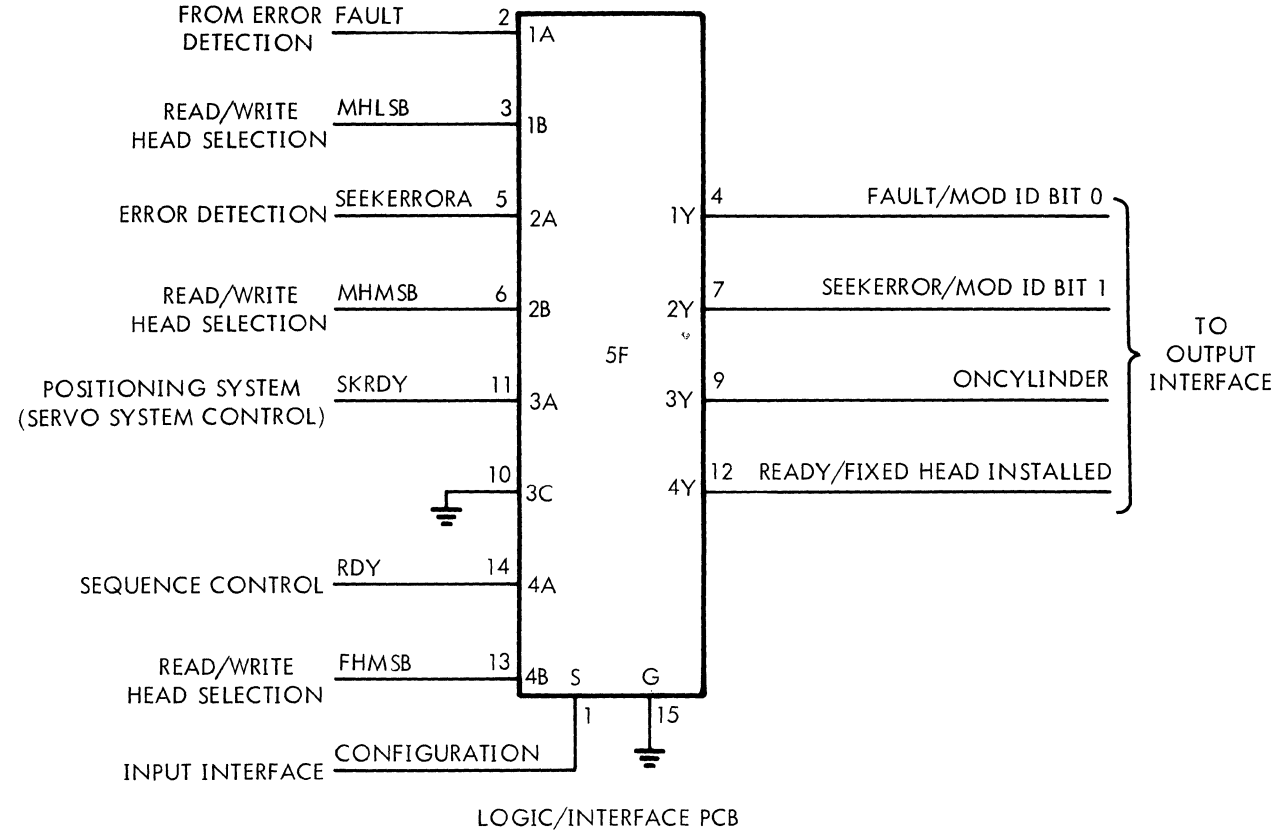


Figure 4-52. Primary/Alternate Status

During normal operation the primary status of (1) FAULT, (2) SEEKERROR, (3) ONCYLINDER, and (4) READY is sent to the output interface. If the system that the disc drive is connected to needs to interrogate the configuration (model type), the CONFIGURATION line may be activated and alternate status will be presented to the output interface. The alternate status is decoded by MOD ID BIT 0 and 1 to identify models: A, two movable heads; B, six movable heads; C, ten movable heads; and D, fourteen movable heads. The FIXED HEAD INSTALLED line denotes whether or not the optional 60 fixed heads are installed.

Output Interface

The output interface logic is the single collection point of information from within the drive to be communicated via the interface cables to a controller (see Figure 4-53). The line

drivers (1A, 2A, 1B, 2B, 3B, 1C, 2C, 3C) convert the single ended signals into differential signals for the interface. The differential signals are then transmitted via the data (J1) and signal (J2, J3) cables.

Each of the line drivers is a dual differential line driver. To permit an active output, the common D input must be active (high) along with the individual C input to enable the sections A and B inputs to be gated to the Y and Z outputs. The line drivers are configured so that all of the data cable (J1) outputs except SECTOR and INDEX are enabled all the time that the drive has power applied.

For SECTOR and INDEX to be gated into ISECTORC and IINDEXC, OPENCABLE/ must be inactive. For OPENCABLE/ to be inactive, the signal cable (J2) must be connected between the drive and controller, with the controller powered up and conditioning the input interface so that OPENCABLE/ is inactive.

The line driver outputs are only enabled for the signal cable (J2, J3) when the drive is selected (UNITSELD active) and an exerciser is not enabled if connected to the drive (/ETESTMODE/ not active). This is due to the fact that the signal cable may be a daisychain configuration and the only time that signals are to be enabled on this interface is when that drive is selected.

A normal sequence of events would be for the drive to be powered up and at the completion of the initial (first) seek, an attention interrupt would signal the controller by the SEEKEND signal through the data cable. The controller would then select the drive to check its status. With the drive selected, the status information (ready, fault, seekerror, on cylinder, write protect, index and sector) will be enabled to be transmitted to the controller. Assuming the status to be correct, the controller will be oriented to a track by index and sector. When oriented and ready to write, the servo PLO signal can be used by the controller to generate write clock pulses that reflect the rotational speed of the discs.

After writing data, the controller can read the data back by waiting for the sector where the write data started. The controller does not have to keep the drive selected during this time since index and sector are also transmitted via the data cable as IINDEXC and ISECTORC. This allows the controller to keep oriented to track location without having the drive selected. When the sector of interest is ready to be read, the drive can be reselected with a READ command being issued. Read data is transmitted via the data cable along with read clocks. These define data cell times to allow the controller to decode the data.

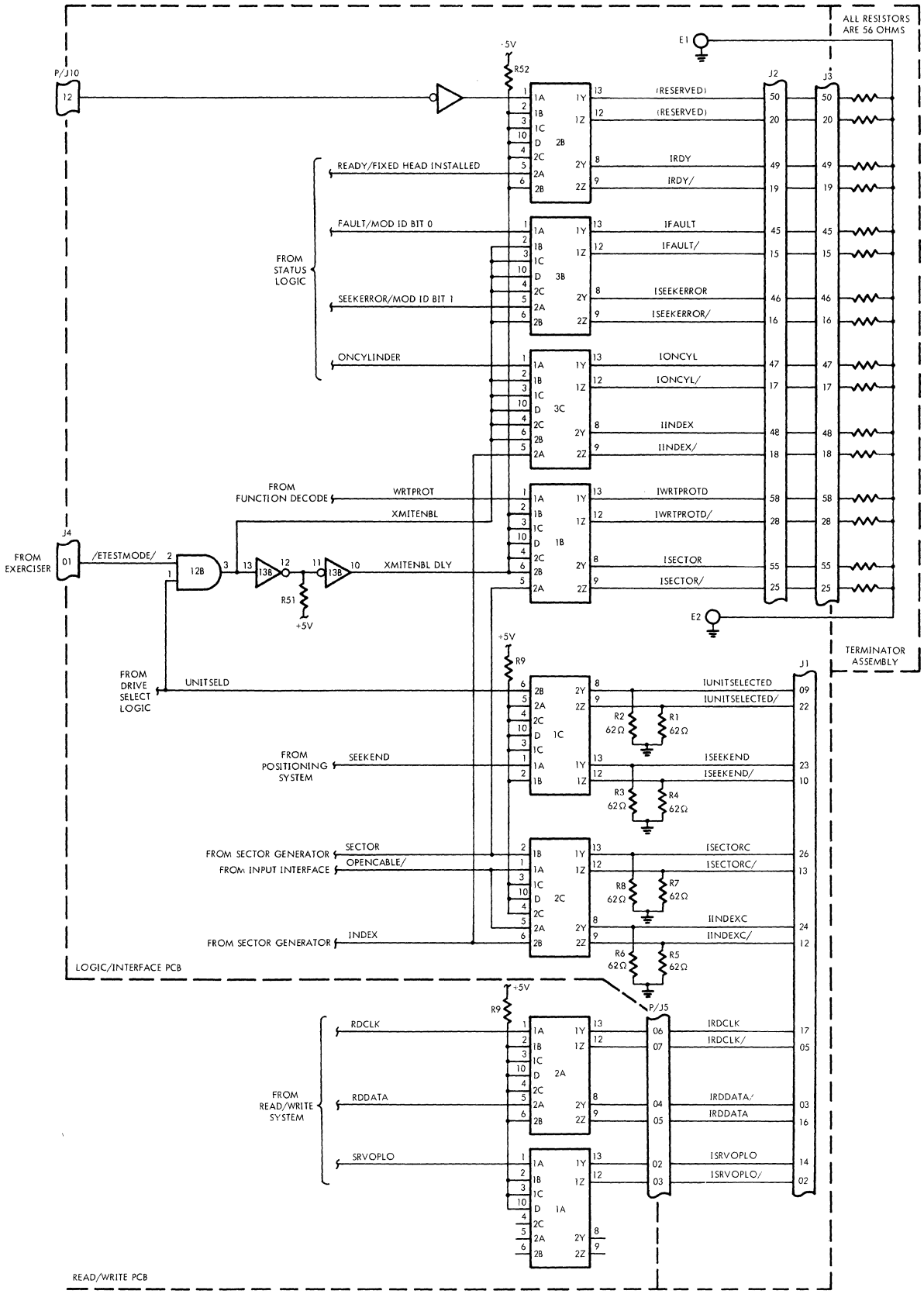


Figure 4-53. Output Interface

SECTION 5

MAINTENANCE

INTRODUCTION

This section presents information that will provide assistance in performing maintenance of the Reflex II disc drive. Maintenance is limited to checkout and corrective procedures that can be performed at the user site. Maintenance should be performed only by qualified service personnel.

For qualified personnel, fault isolation may be performed to the printed circuit board (PCB) level and to the replacement of the PCB as a unit. All of the electromechanical subassemblies are part of the module and motor assembly and must be replaced as a unit. However, several of the items that are appendages to the module and motor assembly, such as the motor, brake assembly, belt, ground brush, etc., may be replaced as subassemblies or as individual components.

PREVENTIVE MAINTENANCE

There is no prescribed periodic preventive maintenance for the Reflex II disc drive. However, there should be some seasonable checking of the unit to verify proper operation of the fans and brake. This could be done when other corrective maintenance is being performed or as the environment of the site dictates. Any accumulation of dust/dirt should also be removed on a periodic basis.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of troubleshooting and fault isolation in the event of a Reflex II malfunction, and the replacement of the defective part or assembly. Replacement procedures are listed in this section under the Removal and Replacement heading. Drawings and schematics in this section and in Section 6 will aid in defining replacement parts and in the tracing of circuits.

Troubleshooting

Malfunctions may arise from faults in the electronic, electromechanical, and mechanical units of the disc drive. The symptoms of a malfunction should be analyzed in terms of these areas:

- Read/write errors
- Seek errors

- Bad status, i.e., fault, not ready, not on cylinder, etc.
- Communication loss, i.e., fails to become selected
- Apparent loss of power

Fault Isolation

In many cases of malfunction, a visual check may find faults that preclude complex troubleshooting procedures. During visual inspection of the Reflex II, the following should be checked:

(1) Switch positions and panel indicators for correct settings and indications.

(2) Wiring, connections, and cabling for secure connections and no abrasions.

(3) Moving parts for obstruction, wear, or damages.

(4) Blown (open) fuses.

During power and/or electronic checks, the following should be inspected:

(1) Power source and main fuse.

(2) DC voltages at the power supply.

(3) All power distribution and voltage levels throughout the unit.

(4) Connections to PCB's.

Circuit test points are provided on the PCB's to facilitate identification of the failed subassembly.

Maintenance Checks

The checks described in this section are provided as information only, but they may be useful when troubleshooting the disc drive. Each check assumes the previous check(s) has been verified okay.

1. Power Supply Check

Verify availability of 115 VAC by visually checking the rotation of the blower fans on the front of the drive.

If AC is not available at this point, locations and probable causes are:

(1) P/J26; missing or defective connection

(2) S1; defective or not turned on

(3) F1 or XF1; open or missing fuse or defective fuse holder

(4) Line filter assembly; defective

(5) P/J29; missing or defective connection

(6) Line cord; defective

(7) Power source; unavailable

(8) Defective connection; between any of the above

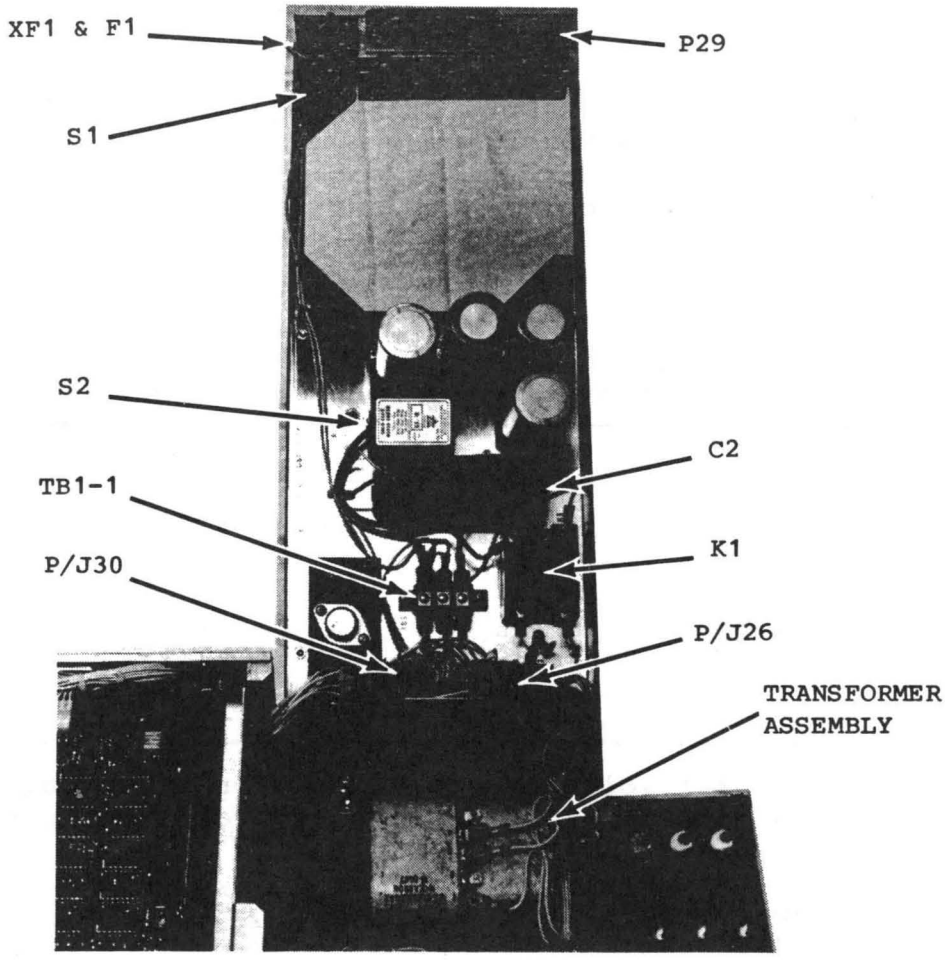


Figure 5-1. Power Supply/Amplifier Assembly

Verify operation of cooling fans and spindle motor (assuming AC available and power on/off switch is on). Potential problems and probable causes are as follows:

(1) Fan(s) not operating; defective fan(s) or connection from TB1 to fans.

(2) Spindle motor not operating;

K1; defective or not energized
S2; defective
C2; defective
P/J30; missing or defective connection
P/J33; missing or defective connection
Motor thermal; defective or overheated
P/J8; missing or defective connection
DC voltage; missing (DCSAFE not active)
Logic/interface PCB; defective
Sequence enable not active
Brake is active
Disc spin speed is unsafe (belt missing or logic failure)

Verify that power supply DC voltages are available. A quick check of all voltages may be made by verifying that J19-6 (DCSAFEAMP/) on the power supply/amplifier PCB is low (active). If DCSAFEAMP/ is not active, the individual voltages to be checked are listed in Table 5-1 (reference Schematic SC20013607 and Figure 5-2).

TABLE 5-1

VOLTAGE AND TEST POINTS FOR POWER SUPPLY/AMP PCB

Voltage	Test point	Probable cause if there is no voltage
+5V	J19-12	F3, VR3
+9V	J19-8	F3
-9V	J18-8	F4
+12V	J19-5	F2, VR2
-12V	J19-3	F1, VR1
+18V	Plus (+) terminal of C2	F2
-18V	Minus (-) terminal of C1	F1

If any or all voltages are missing or if voltages are present and DCSAFEAMP/ is still not active, other probable causes may be the:

Power supply/amplifier PCB
P/J18
P/J26
Transformer assembly (external DC source)

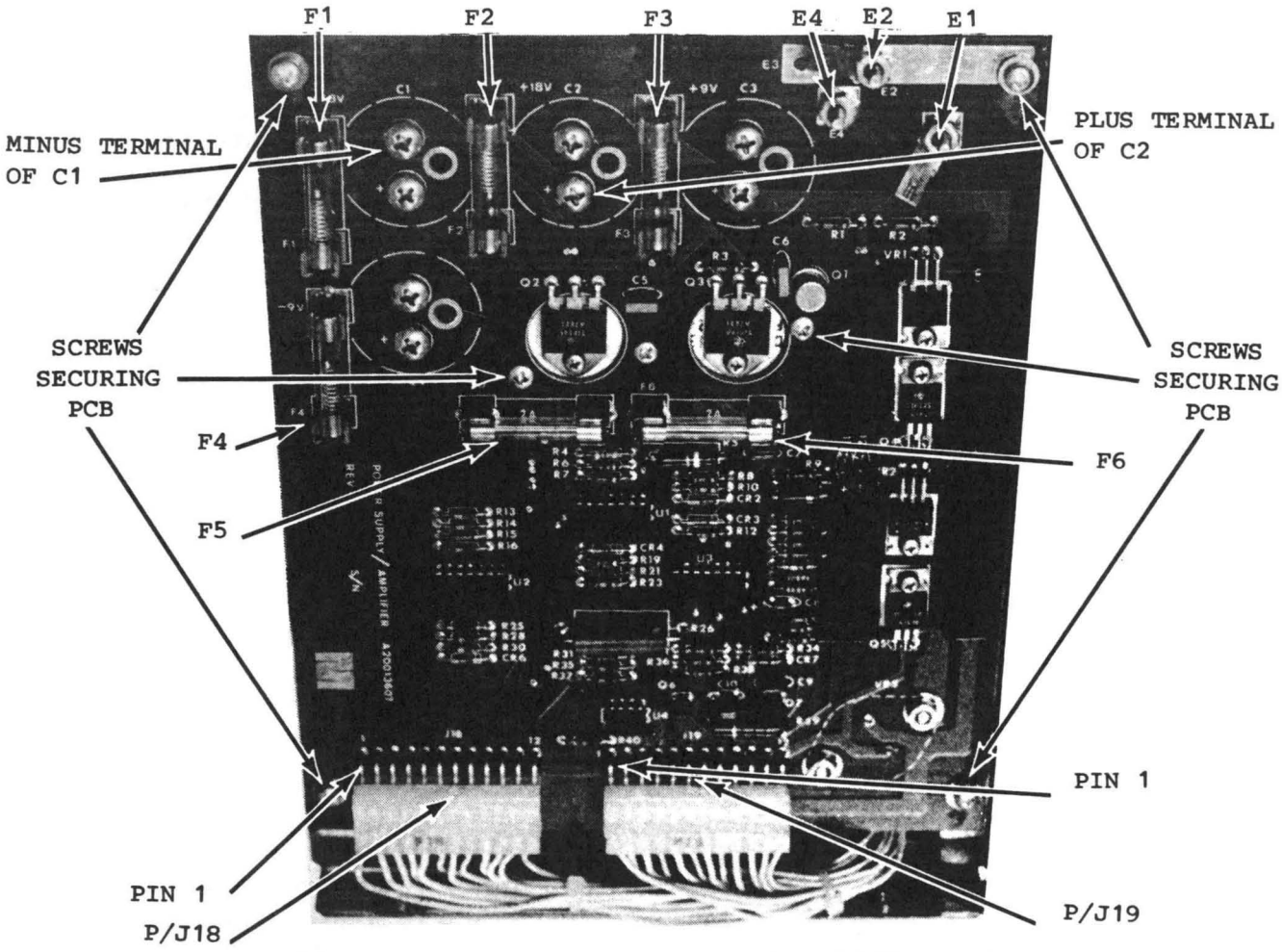


Figure 5-2. Power Supply/Amplifier PCB

2. DC Voltage Distribution

The logic/interface PCB receives +5V, +9V, -9V, +12V, and -12V from the power supply/amplifier board. In addition, it creates -5.2V from -9V. The voltage, test point, and probable causes, if voltage is not present, are listed in Table 5-2 (reference Schematic SC20013608).

TABLE 5-2

VOLTAGE AND TEST POINTS FOR LOGIC/INTERFACE PCB

Voltage	Test point	Probable cause if there is no voltage
+5V	J12-12	Connection to PCB or source
-5.2V	J11-01	Logic/interface PCB, connection to PCB or source (+9V)
+9V	J9-08	Connection to PCB or source
-9V	J12-11	Connection to PCB or source
+12V	J12-09	Connection to PCB or source
-12V	J12-10	Connection to PCB or source

The servo PCB receives +5V, -9V, +12V, and -12V from the power supply/amplifier PCB via the logic/interface PCB. It also receives -5.2V from the logic/interface PCB and in addition, creates -5.2V from -9V and +6.2V, -6.2V, and -8.2V from +12V and -12V, respectively. The voltage, test point, and probable cause if voltage is not present, are listed in Table 5-3 (reference Schematic SC20013609 or SC20013711 and Figure 5-3).

TABLE 5-3

VOLTAGE AND TEST POINTS FOR SERVO PCB

Voltage	Test point	Probable cause if there is no voltage
+5V	P12-12	Connection to PCB or source
-5.2V	P12-06	Connection to PCB or source
-5.2V	IC 1B Pin 8	Servo PCB, connection to PCB or source (-9V)
+6.2V	Cathode, CR2	Servo PCB, connection to PCB or source (+12V)
-6.2V	Anode, CR1	Servo PCB, connection to PCB or source (-12V)
-8.2V	Anode, CR4	Servo PCB, connection to PCB, servo head and/or cable, or source (-12V)
-9V	P12-11	Connection to PCB or source
+12V	P12-09	Connection to PCB or source
-12V	P12-10	Connection to PCB or source

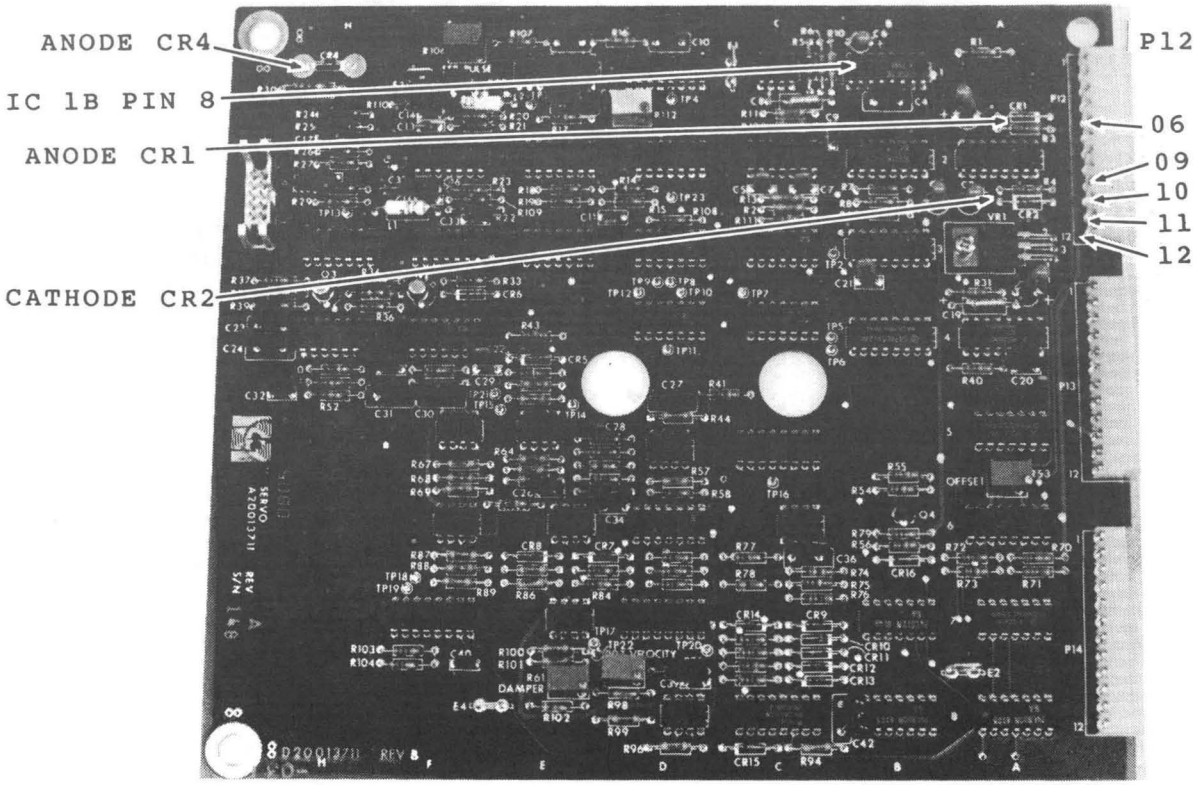


Figure 5-3. Servo DC Voltages

The read/write PCB receives +5V, +9V, -9V, +12V, and -12V from the power supply/amplifier PCB via the logic/interface PCB. It also receives -5.2V from the logic/interface PCB and, in addition, creates -4V, -5.2V, +6V, +6VRW, +6.2V, and -6.2V from -9V, +9V, +6V, +12V, and -12V, respectively. The voltage, test point, and probable cause if voltage is not present, are listed in Table 5-4 (reference Schematic SC20013610 and Figure 5-4).

TABLE 5-4

VOLTAGE AND TEST POINTS FOR READ/WRITE PCB

Voltage	Test point	Probable cause if there is no voltage
-4V	Minus side of C37	Read/write PCB, connection to PCB, head IC and/or cable, or source (-9V)
+5V	P10-01	Connection to PCB or source
-5.2V	P11-01	Connection to PCB or source
-5.2V	TP28	Read/write PCB, connection to PCB or source (-9V)
+6V	Plus side of C36	Read/write PCB, connection to PCB or source (+9V)
+6VRW	IC 1E Pin 6	Read/write PCB, connection to PCB, head IC and/or cable or source (+9V)
+6.2V	Cathode, CR4	Read/write PCB, connection to PCB or source (+12V)
-6.2V	Anode, CR5	Read/write PCB, connection to PCB or source (-12V)
+9V	P10-02	Connection to PCB or source
-9V	P10-03	Connection to PCB or source
+12V	P11-06	Connection to PCB or source
-12V	P11-02	Connection to PCB or source

As previously noted, all PCB's must be checked to verify that each PCB has its necessary voltages. However, there are some shortcuts available as revealed in Figure 5-5. By checking -4V (-9V), +5V, -5.2V, -5.2V (-9V), +6VRW (+6V, +9V), +6.2V (12V), and -6.2V (-12V) on the read/write PCB, the voltages and connections will be verified from the DC voltage source, through the power supply/amplifier PCB, through the logic/interface PCB and into the read/write PCB.

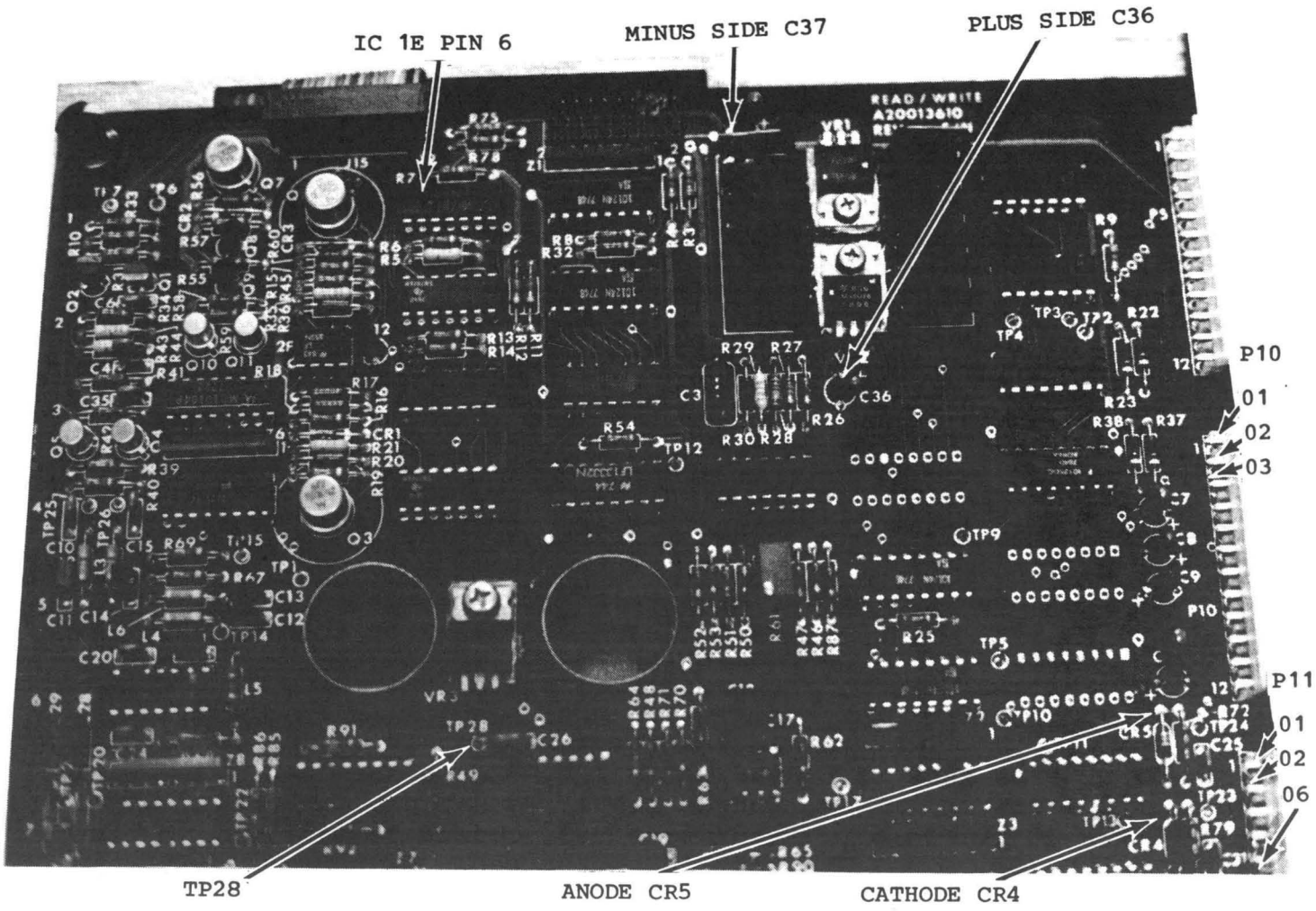


Figure 5-4. Read/Write DC Voltages

3. Sequence Up

The initiation of a sequence up is by application of power-on (AC power if internal transformer assembly, or AC and DC power if an external power supply option). The conclusion of a sequence up is the ready (RDY) term becoming active. The events in between can be monitored, for the most part, by the exerciser (see Figure 5-6). In addition to the application of power, the term sequence enable (SEQENBL) must be active. This term becomes active by (1) the unit being selected and DCSAFE active, (2), the exerciser being plugged into J4 of the disc drive, or (3), the sequence enable switch (S3-6) on the logic/interface PCB being active.

The application of power-on causes power initialize (PWRINI) to become active. PWRINI resets seek logic (SETDIF/, SETCAR, SKSTRT), odd (ODD/), forward (FWD/), ST0/, ST1, ST2, ST3, seek error logic (SEEKERRORA), and the fault logic (FAULT). PWRINI also generates the signal seek initialize (SKINIL) which resets the head address register (HAR) and the cylinder address register (CAR).

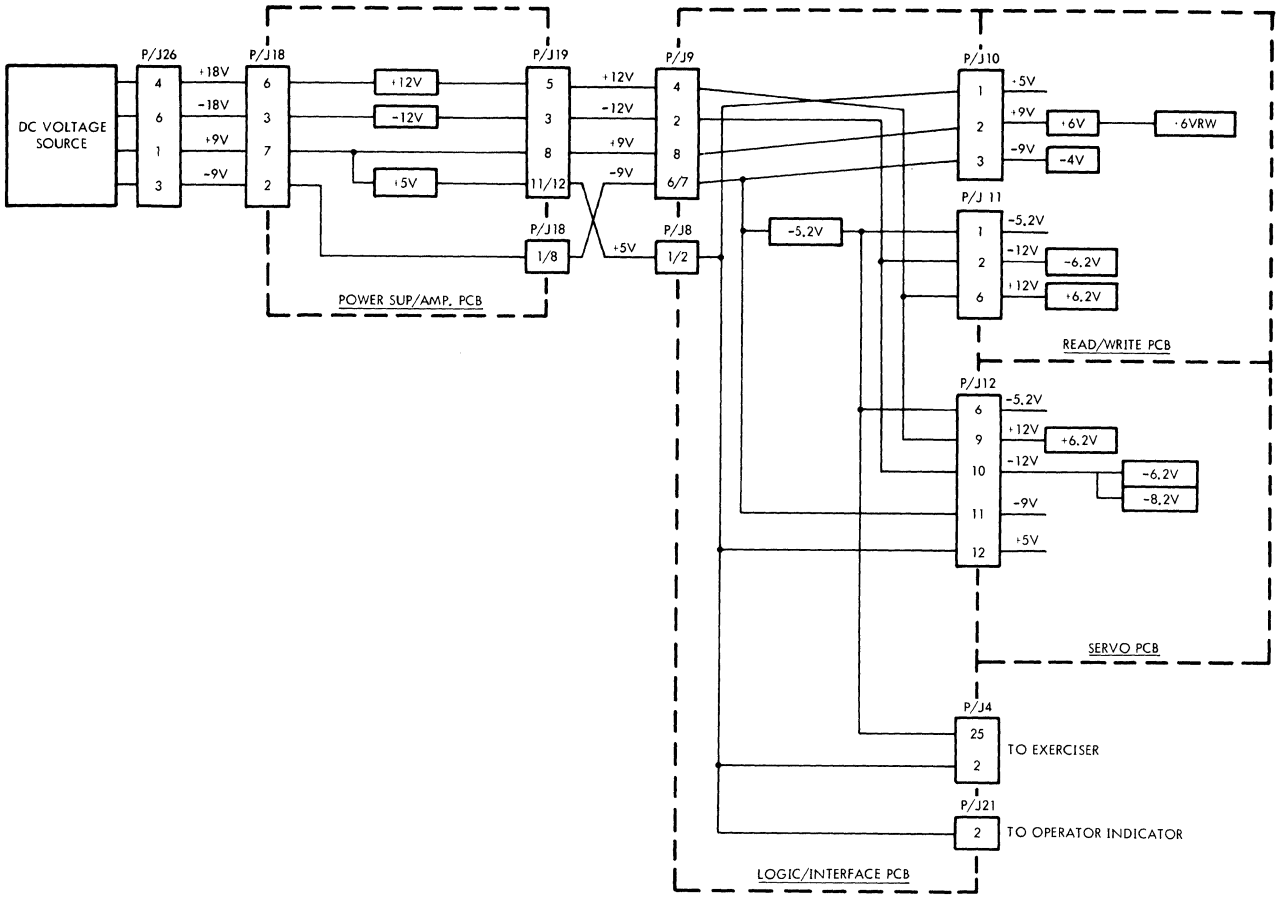


Figure 5-5. DC Voltage Distribution

PWRINI will remain active until all DC voltages are present and within tolerance on the power supply/amplifier PCB (DCSAFEAMP/), and until the spindle brake has been released (SPINBRKRLSD). The release of the spindle brake will create the signal 30 second timer (30SECTMR/). This signal will act as a monitor for disc speed.

DCSAFEDLYD and SEQENBL clock the start motor enable flip-flop. With this flip-flop active, the output releases the spindle brake. When the signal SPINBRKRLSD becomes active, it is ANDed with the output of the start motor enable flip-flop to generate start AC motor (STACMTR/) which will allow the spindle motor to start. If disc speed safe (DISCSPSAFE/) becomes active before 30SECTMR/ becomes inactive, the sequence up operation will be allowed to continue; otherwise, STACMTR/ will become inactive. Also if the brake becomes unsafe (SPINBRKRLSD inactive) at any time after PWRINI is inactive, STACMTR/ will become inactive.

Figure 5-6. Sequence Up

STACMTR/ active with DISCPSAFE/ active and RETCTRL/ inactive will activate the carriage lock solenoid (CARRLKSLND) thereby releasing the carriage. Carriage lock released (CARRLKRLSD) active with STACMTR/ active and retract control (RETCTRL/) inactive will cause retract heads (RETHDS) to become inactive.

RETCTRL/ will be inactive if an exerciser is connected to J4 of the logic/interface PCB or if the open cable (OPENCABLE/) signal is inactive. Inactive RETHDS will enable the servo amplifiers to be driven by the servo logic.

The servo control logic was initially set to drive in reverse (FWD/ reset) at load speed (LDSP/) because of ST0 being the outer guard band (OGB) during the last power off cycle, OGB and ST0 will deactivate ST0 and activate ST1. ST1 will command the servo logic to drive forward (FWD/) at LDSP/. This forward motion will continue until OGB becomes inactive. These conditions will then cause ST2 to become active and ST1 to become inactive. ST1 becoming inactive will deactivate FWD/ and LDSP/ and ST2 will create track following mode (TRKFL/). This will cause the servo to stop driving the carriage at the first cylinder forward of the outer guard band. This cylinder will be cylinder 0.

RETHDS being inactive and 30 SECTMR/ becoming inactive will generate the signal ready (RDY), provided the fault (FAULT) signal is inactive. ST2 becoming active will generate SEEKDONE/ after a 3.5 millisecond delay. SEEKDONE/ active and SEEKERRORA inactive will create seek ready (SKRDY) and SEEKEND. SKRDY creates the signal on cylinder (IONCYL) and the unit is now ready to perform commanded servo or read/write operations.

A failure to completely sequence up could be anywhere in the unit. To narrow the potential failed assembly, it is necessary to monitor the sequence to determine where it stops working. Once the point where a failure occurs is determined, troubleshooting may be restricted to that element. For instance, what if a spindle motor started but then stopped? This would be an indication that the disc did not attain a safe speed. The troubleshooting could be directed to learn why DISCSPSAFE/ has not become active before 30 SECTMR/ has become inactive.

4. Ground Brush Assembly

The ground brush assembly provides a static discharge path for the disc(s) and spindle. The brush provides ground continuity from the stationary base of the spindle shaft to the deck plate through the ground brush assembly. A poor ground contact at this point may cause sporadic (although soft) data errors.

With power on and the spindle rotating at full speed, check the continuity between the stationary base of the spindle and the ground brush assembly. If the resistance exceeds 1 ohm, clean the surface of the ground brush with a fine emery cloth. This cleaning can be done while the spindle is spinning by inserting the emery cloth between the base of the spindle and the ground brush.

CAUTION: Exercise care to avoid bending the ground spring. This spring must maintain a 150 gram force to ensure proper contact.

5. Servo Balance (Offset) Verification

Set oscilloscope to 50mV per division. Connect the oscilloscope to TP16 (position) on the servo PCB (reference Figure 5-7). With power applied to the unit and the unit in track following mode, check the voltage level when the carriage is located at cylinder 000 and cylinder 560 (outer and inner cylinders). The DC voltage level should be approximately equal above and below ground and should not exceed 200mV total (±100mV). If adjustment is necessary, refer to Servo Balance Adjustment in this section.

6. Velocity Verification

Set oscilloscope for 2V per division with a time base of 10 milliseconds per division. Install a chip clip on IC 19C on the logic/interface PCB. Sync negative on 19C2 (SKSTRT/) and scope 19C8 (SKRDY). While performing full stroke seeks (000 to 560 to 000, etc.), verify that 19C8 (SKRDY) is inactive for 55±1 milliseconds (reference Figure 5-10 and logic/interface schematic). If adjustment is required, refer to Velocity Adjustment in this section.

7. Damper Verification

Set oscilloscope to 2V per division on channel A. Set channel B to 0.5V per division. Syncing on channel A, slope 19C8 (SKRDY). Next, monitor POSITION signal at TP16 (reference Figure 5-7) with channel B while performing alternate seeks of 1, 2, 4, 8, 16, 32, 64, 128, 256, and 512. Verify that the overshoot is less than 90 percent of the peak POSITION amplitude without peak clipping. If adjustment is required, refer to Damper Adjustment in this section.

8. Pulse Gate Verification*

Set oscilloscope to 2V per division and the time base to 50 nonoseconds. Scope TP-3 (pulse gate--reference Figure 5-7) and trigger on the positive edge of PULSE GATE. Ensure that the pulse width is 350 ± 10 nanoseconds. If adjustment is required, refer to Pulse Gate Adjustment in this section.

9. Separated Pulse Verification*

Set oscilloscope to 2V per division and the time base to 50 nanoseconds. Scope TP23 (SEP PULSE--reference Figure 5-7) and trigger on the negative edge of SEP PULSE. Ensure that the pulse width is 40 ± 2 nanoseconds for REV A and 25 ± 2 nanoseconds for REV B and later. If adjustment is required, refer to SEP PULSE Adjustment in this section.

---

*PULSE GATE AND SEP PULSE are adjustments which are unique to servo PCB A20013711 only. The velocity, offset and damper adjustments are common to A20013609 and A20013711.

10. Phase Detector Offset Verification

Set oscilloscope to 0.5V per division with a time base of 5 ns per division. Sync the scope interval on channel A. Connect channel A to test point 18 of the read/write PCB (reference Figure 5-11). Connect channel B to test point 19 of the same PCB. Look at the signals in alternate mode, while the unit is in track following mode and no read or write commands are active. Verify that the positive going edges of the two signals are within 0±2 ns of each other at the threshold point (-1.3V), (reference Figure 5-12). If adjustment is necessary, refer to Phase Detector Offset Adjustment in this section.

11. Read/Write Pulse Width Verification

Set oscilloscope to 0.5V per division with a time base of 10 ns per division. Sync the scope internal on channel A. Connect channel A to test point 18 of the read/write PCB (reference Figure 5-11). Connect channel B to test point 29 of the same PCB. Center the negative pulse from channel B. Adjust the base line of channel A so that the base line is 1.3V above the centerline of the scope. Adjust the base line of channel B so that the base line is 1.0V above the centerline of the scope.

With the disc drive in track following mode and no active read or write command, verify that the negative going edge of channel A has its threshold point (-1.3V) at the center (0±2 ns) of the scope when the negative pulse of channel B is centered on the scope (reference Figure 5-13). If adjustment is necessary, refer to Pulse Width Adjustment in this section.

12. Brake Verification

The brake verification is primarily a mechanical check. Gain access to the bottom of the unit and remove the bottom access cover. Verify that there is pad material that touches the brake disc when the brake solenoid is not energized. Also verify that the pads do not touch the brake disc when the brake solenoid is energized. The above situations are the important factors and as long as the brake stops the spindle within 15 seconds, there is no requirement for further action.

The following adjustments may be performed;

- Servo PCB

  Speed (up-to-speed)
  Sep Pulse
  Pulse Gate
  Balance (offset)
  Velocity
  Damper

- Read/write PCB

  Phase detector offset
  Pulse width (detector window)

- Brake assembly

  Stop time

The procedures for performing these adjustments follow.

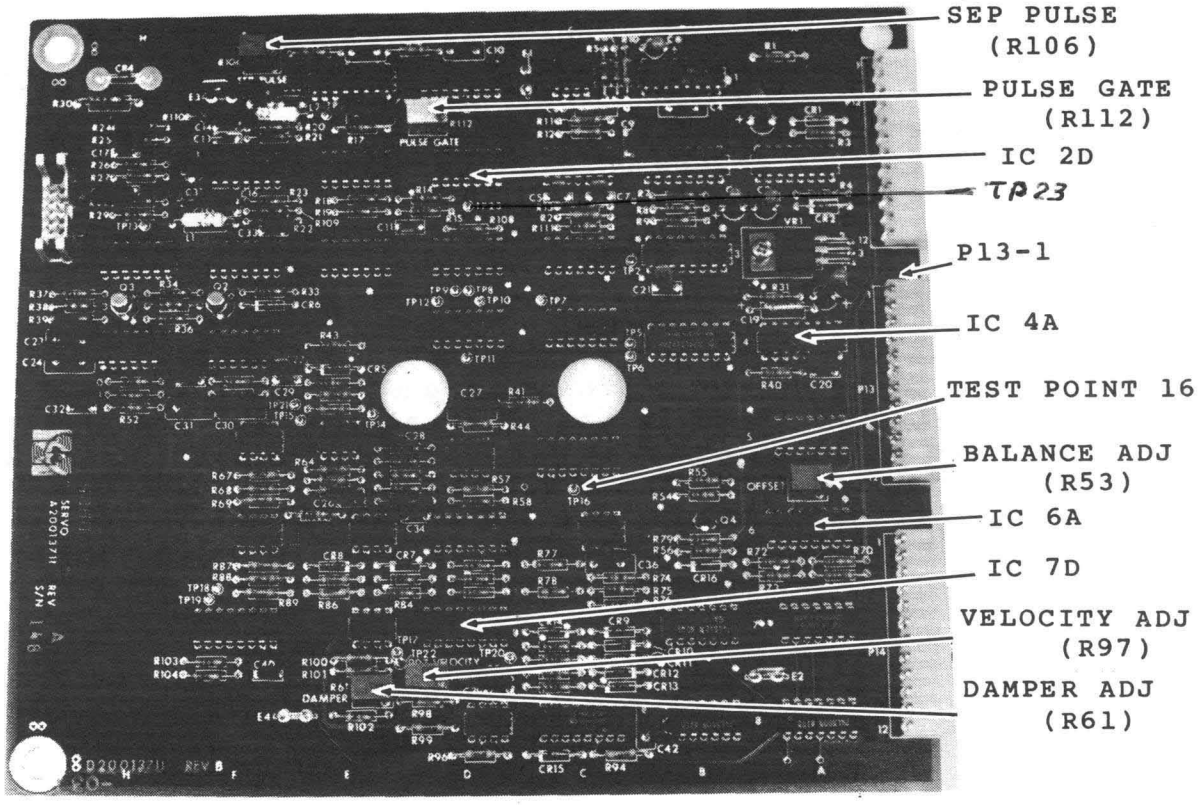


Figure 5-7. Servo Adjustments

Servo PCB Adjustments

The location of the servo adjustments is shown in Figure 5-7.

1. Speed Adjustment

NOTE

This adjustment has been deleted from the Servo PCB Alignment Procedures.

On A20013609 Rev N or less, rotate R-32 to its MAXIMUM CLOCKWISE POSITION (20K ohms).

On boards after Rev N, R-32 has been replaced with a fixed resistor.

Figures 5-8 and 5-9 pertained to the speed adjustment and have been deleted from this manual.

2. Separated Pulse Adjustment (A20013711 only)*

(1) Apply power to the unit and allow the unit to attain ready status.

(2) Set oscilloscope for an internal, negative sync on channel A with a time base of 20 nanoseconds per division.

(3) Set channel A to 2V per division and connect the channel A probe to TP23.

(4) Adjust SEP PULSE pot (R106) for a 40 nanosecond negative pulse at TP23. (On A20013711 Rev B and higher set R106 to 40 +5 -0 nanoseconds.)

TB009-003

(5) Reference Figure 5-7 for test point and pot location. D-2 F-1

3. Pulse Gate Adjustment (A20013711 only)*

(1) Apply power to the unit and allow the unit to attain ready status.

(2) Set oscilloscope for an internal, positive sync on channel A with a time base of 50 nanoseconds per division.

(3) Set Channel A to 2V per division and connect the channel A probe to TP3. E-1

(4) Adjust PULSE GATE pot (R112) for a 350 nanosecond positive pulse width. D-1

(5) Reference Figure 5-7 for test point and pot locations. E-1 D-1

4. Balance (offset) Adjustments

This adjustment is to be performed when the servo is in track following (TRKFL) mode. If for some reason the unit does not acquire TRKFL mode (i.e., new unknown unit or servo PCB has just been replaced), center both the balance pot (R53) and the velocity pot (R97(. Perform both balance and velocity adjustments assuming that centering the pots has allowed the unit to attain TRKFL mode after a power-on cycle (reference Figure 5-7).

---

*The first three adjustments are unique to the noted assembly. Only the last three adjustments are common to both boards. A20013609 REV P and higher require no disc speed adjustment. R32 (disc speed) has been disabled in those boards.

To center the balance pot use a DVM. Connect the DVM to R75 on the servo PCB to the end of R75 closest to connectors P12, P13, and P14. Adjust R53 for 0V.

(1) Apply power to the unit and allow unit to attain ready status. Verify that the TRKFL mode is active.

(2) Connect the DVM to test point 16 on the servo PCB (reference Figure 5-7).

(3) Record the DC voltage level of TP16.

(4) Perform a seek operation to cylinder 560. 230

(5) Record the DC voltage level of TP16.

(6) Adjust the balance (offset) pot R53 so that the DC voltage levels at cylinder 000 and cylinder 560 will be equally displaced above and below 0V.

(7) Perform seeks to cylinders 000 and 560. Note the voltage level of TP16 at each of these cylinders. Adjust R53 until there is an equal DC voltage displacement above and below 0V. The maximum voltage levels should not exceed ±100mV.

5. Velocity Adjustment

Verify balance adjustment before doing the velocity adjustment. Reference Figure 5-7 for test points.

(1) Apply power to the unit and allow the unit to attain ready status.

(2) Install a chip clip on IC 19C on the logic/interface PCB.

(3) Set oscilloscope for an internal, negative sync on channel A with a time base of 10 milliseconds per division.

(4) Set channels A and B for DC coupling at 2V per division with chop mode selected.

(5) Connect channel A to IC 19C pin 2 (SKSTRT/) on the logic/interface PCB.

(6) Connect channel B to IC 19C pin 8 (SKRDY) on the logic/interface PCB.

(7) Program the drive to do alternate full stroke seeks (cylinder 000 to 560 to 000, etc.).

230

(8) While doing alternate full stroke seeks, adjust the velocity pot (R97) so that channel B (SKRDY) is negative (not active) for 55 ±1 milliseconds. The time difference between a forward seek and a reverse seek should be within 5 milliseconds of each other (reference Figure 5-10).

6. Damper Adjustment

(1) Apply power to the unit and allow the unit to attain ready status.

(2) Set oscilloscope for an internal, negative sync on channel A with a time base of 10 milliseconds per division.

(3) Install a chip clip on IC 19C on the logic/interface PCB.

(4) Set channels A and B for DC coupling with A at 2V per division and B at 0.5V per division and chop mode selected.

(5) Connect channel A to IC 19C-8 (SKRDY) on the logic/interface PCB and channel B to TP16 on the servo PCB.

(6) Program the drive to do 1, 2, 4, 8, 16, 32, 64, 128, 256, and 512 alternate seeks.

(7) Adjust R61 on the servo PCB so that the overshoot on all the above seeks is 90 percent or less of the positive voltages of the position signal.

(8) Reference Figure 5-7 for test point and pot location.

Read/Write Adjustment

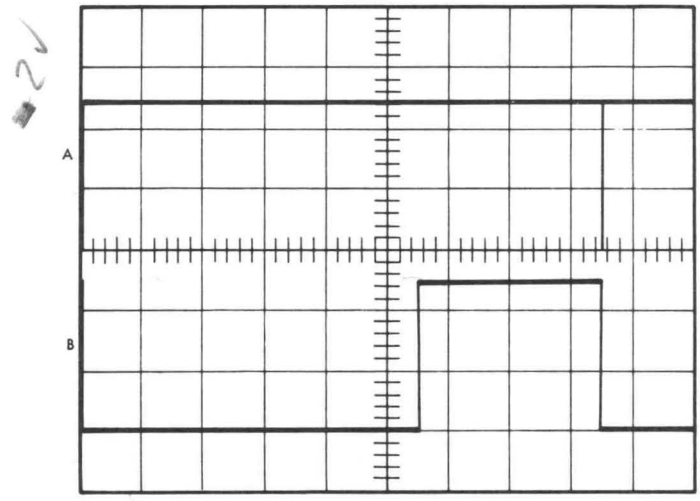
The location of the read/write adjustments is shown in Figure 5-11.

1. Phase Detector Offset Adjustment

(1) Apply power to the disc drive and allow it to attain ready status.

(2) Set oscilloscope for internal, positive sync from channel A with a time base of 5 ns per division.

(3) Set channels A and B for DC coupling 0.5V per division, with chop mode.



PROG: Alternate seeks between cylinders 000 and 560

SYNC:	Channel A	Internal	Negative	10 ms
CHAN:	A DC	2V	19C2 (SKSTRT/)	
CHAN:	B DC	2V	19C8 (SKRDY)	

MODE: **Chopped**

NOTE: Adjust R97 for Channel B (SKRDY) to go negative (inactive) for 55 ± 1 ms.

Figure 5-10. Velocity Adjustment

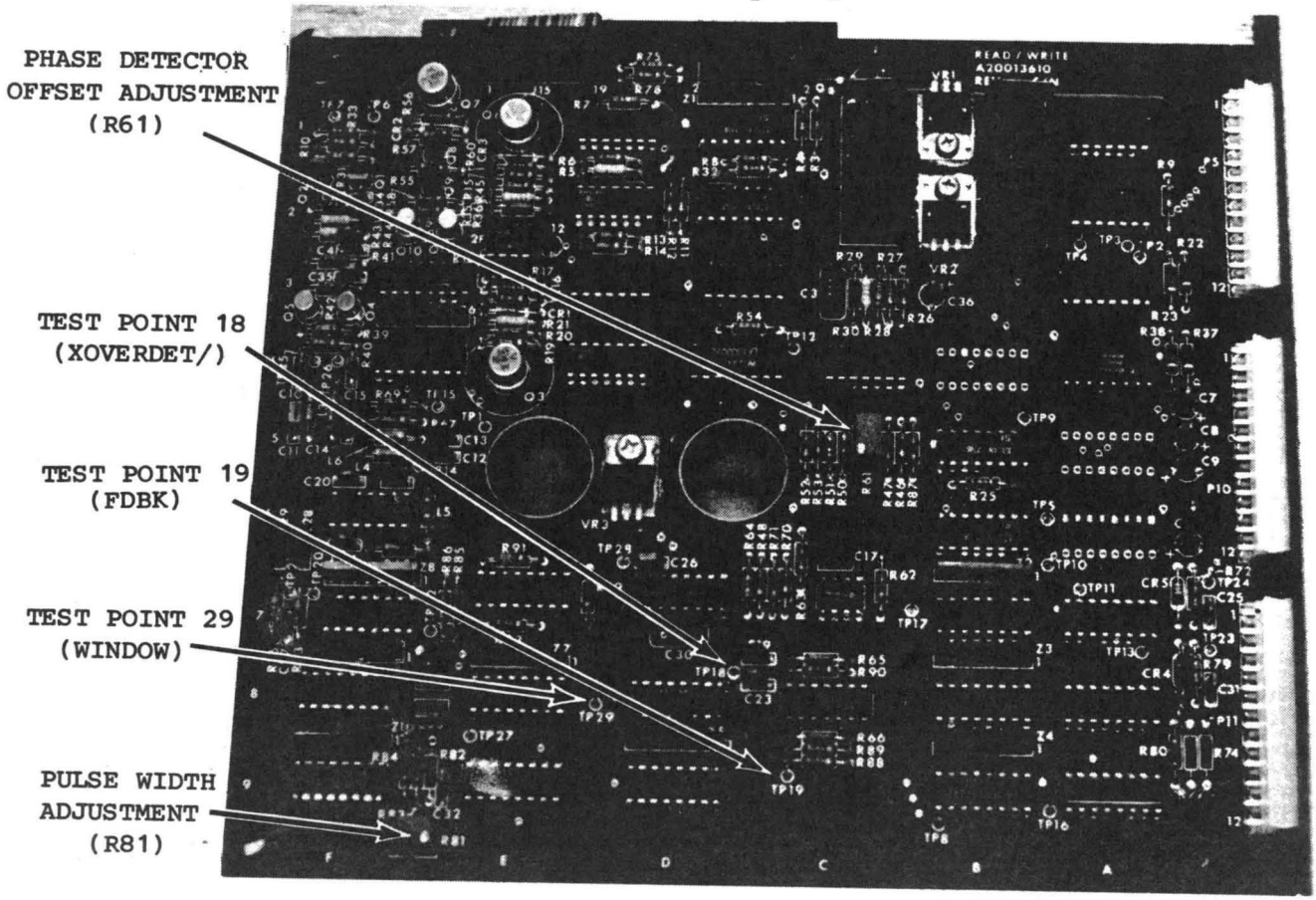


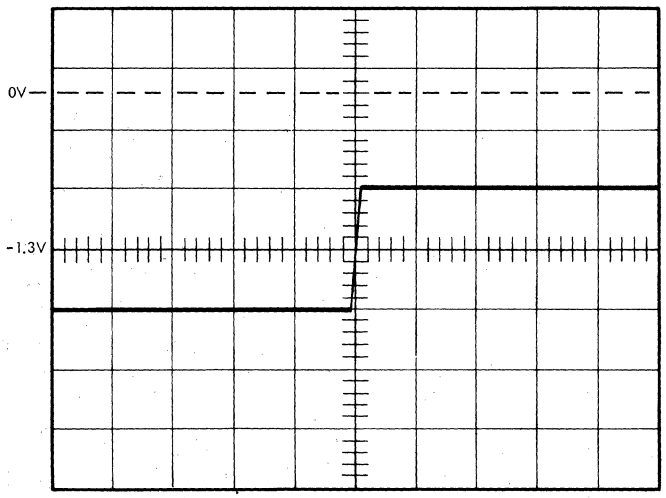
Figure 5-11. Read/Write Adjustments

(4) Adjust the base lines (0V) of both channels A and B so that the base line is 1.3V above the centerline of the scope.

(5) Connect channel A to test point 18 and channel B to test point 19 of the read/write PCB.

(6) Adjust the position of the signal so that the positive going edge of the signal from channel A has the 1.3V level (threshold) exactly at the center of the oscilloscope (reference Figure 5-12).

(7) With the disc drive in track following mode and no active read or write command, adjust the phase detector offset pot (R61) so that the positive going edge of channel B lines up with the positive going edge of the signal of channel A. The adjustment is to provide offset of 0±1 ns of the leading edge of both signals at the -1.3V level.



PROG: Disc ready; no seek, read or write; verify to 0 ± 2ns; adjust to 0 ± 1ns
SYNC: Channel A Internal Positive 5ns
CHAN: A DC 0.5V TP18 (XOVERDET/)
CHAN: B DC 0.5V TP19 (FDBK)
MODE: Chopped
NOTE: Adjust R61 so that the positive going edge of both pulses are coincident (0 ± 1ns) at the threshold level (-1.3V)

Figure 5-12. Phase Detector Offset Adjustment

2. Pulse Width (Detector Window) Adjustment

(1) Apply power to the disc drive and allow it to attain ready status.

(2) Set the oscilloscope for internal, positive sync from channel A with a time base of 10 ns per division.

(3) Set up channels A and B for DC coupling at 0.5V per division with chop mode.

(4) Adjust the base line (0V) for channel A so that the base line is 1.3V above the centerline of the scope.

(5) Adjust the base line (0V) for channel B so that the base line is 1.0V above the centerline of the scope.

(6) Connect channel A to test point 18 and channel B to test point 29 of the read/write PCB (reference Figure 5-11).

(7) Adjust the position of the negative pulse of channel B to be centered about the vertical centerline of the scope (reference Figure 5-13).

(8) With the disc drive in track following mode and no active read or write command, adjust the pulse width pot (R81) so that the negative going edge of channel A has its threshold point (-1.3V) exactly at the center of the scope (0±1ns) when the negative pulse of channel B is centered on the scope (reference Figure 5-13).

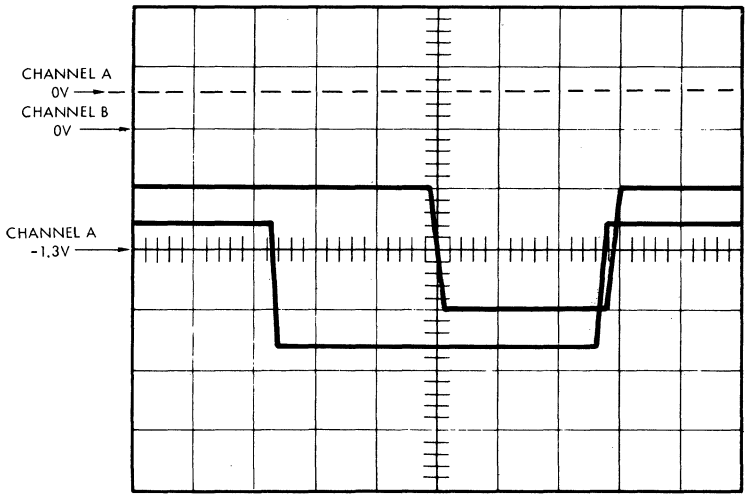
Brake Adjustment

Normally a brake adjustment should not be required during the life of the REFLEX II disc drive. However, in the event of a brake assembly replacement, an adjustment may be required. The brake adjustment procedure follows (reference Figure 5-17).

(1) Gain access to the bottom of the unit and remove the bottom access cover.

(2) Disable sequence enable (SEQENBL). This may be done by disconnecting the signal interface cable (not allowing the unit to be selected) and by not installing the exerciser. The sequence enable switch (S3-6) on the logic/interface PCB should be inactive (open). Reference the logic/interface schematic.

(3) Apply power to the unit. After the brake has energized, adjust the brake adjustment screw so that the brake



PROG:	Disc ready; no seek, read or write; verify to 0 ± 2ns; adjust to 0 ± 1ns			
SYNC:	Channel A	Internal	Positive	10ns
CHAN:	A DC	0.5V	TP18 (XOVERDET)	
CHAN:	B DC	0.5V	TP29 (WINDOW)	
MODE:	**Chopped**			
NOTE:	Adjust R81 so that the negative going edge of TP18 (XOVERDET) has its threshold point (-1.3V) exactly at the center of the scope (0 ± 1 ns), when TP29 (WINDOW) is properly adjusted. When properly adjusted, its negative pulse is centered exactly about the center of the scope face.			

Figure 5-13. Pulse Width Adjustment

pads do not contact or provide any drag to the brake disc. (Ideally, the pads are adjusted to be an equal distance away from the disc on both sides of the brake disc; however, when the sealed module is in the frame, this observation is difficult to make.)

(4) Remove power from the unit and verify that the brake pads collapse against the brake disc.

> CAUTION: Avoid turning the brake disc (spindle). Turning the spindle by hand may cause damage to the heads and/or disc(s).

REMOVAL AND REPLACEMENT

Power should be off when removing or replacing any assembly or components within the disc drive. When printed circuit boards are removed and replaced, particular care should be administered to prevent damage to any connectors and to ensure that the PCB's are properly seated in their connectors.

Printed Circuit Boards

Turn off power and remove the AC power cord from the power outlet. Remove the appropriate external covers; the PCB chassis cover and interface cover if the PCB to be replaced is read/write, servo, or logic/interface; the interface cover and power supply/amplifier chassis cover if the PCB to be replaced is power supply/amplifier. Remove and replace appropriate PCB.

1. Read/Write PCB

   (1) Disconnect P15 and, if applicable, P17.

   (2) Disconnect grounds from the board.

   (3) Disengage (lift-up) quick-locks.

   (4) Lift board to clear frame and pull out from connectors so that the connector pins will not be bent.

   CAUTION: Excessive lift will damage the connectors.

   (5) To replace PCB, reverse steps (1) through (4). For connector orientation of P15, the cable enters the connector on the side for even numbered pins. Holding P15 with the cable entering on the bottom and looking into the connector sockets, pin 1 is on the left side. Connector orientation for P17 is just the opposite of P15.

   (6) Verify read/write adjustments.

2. Servo PCB

   (1) Disconnect P16.

   (2) Disconnect grounds from the board.

   (3) Disengage (lift-up) quick-locks.

   (4) Lift board to clear frame and pull out from connectors so that the connector pins will not be bent.

   CAUTION: Excessive lift will damage the connectors.

   (5) To replace, reverse steps (1) through (4). For connector orientation of P16, the cable enters the connector on the side for even numbered pins. Holding P16 with the cable entering on the bottom and looking into the connector sockets, pin 1 is on the left side.

(6) Verify servo adjustments.

3. Logic/Interface PCB

(1) Remove both the read/write and servo PCB's.

(2) Remove interface cables (P1, P2, and P3).

(3) Disconnect P21.

(4) Disengage (lift-up) quick-locks.

(5) Lift board from end with quick-locks and J21. Work PCB out to give clearance to remove P8 and P9. (Alternate method: remove P8 and P9 before lifting the PCB.)

(6) To replace, reverse steps (1) through (5). For connector orientation of P21, the cable enters the connector on the side for the odd numbered pins. Holding P21 with the cable entering on the bottom and looking into the connector sockets, pin 1 is on the right side.

(7) Verify switch settings on logic/interface PCB (see Installation and Operation Section).

4. Power Supply/Amplifier PCB

(1) Remove interface cables (P1, P2, and P3).

(2) If applicable, remove external ground strap from E1.

(3) Remove six screws securing PCB in place (reference Figure 5-2).

(4) Remove P18 and P19.

(5) Remove PCB being careful not to lose spacers between PCB and frame. (Some units may not have spacers.)

(6) Before installing replacement PCB, add thermal compound to the conductor block affixed to Q2 and Q3.

(7) To replace, reverse steps (1) through (5).

(8) Verify ground connection for E2 and E4.

(9) Verify DC voltages.

(10) Verify servo velocity and offset adjustments.

5. LED/Switch PCB (Operator Indicator Panel)

(1) Remove two screws securing PCB chassis and swing PCB chassis open (reference Figure 5-14).

(2) Remove two screws securing LED/switch PCB.

(3) Remove P39 from LED/switch PCB.

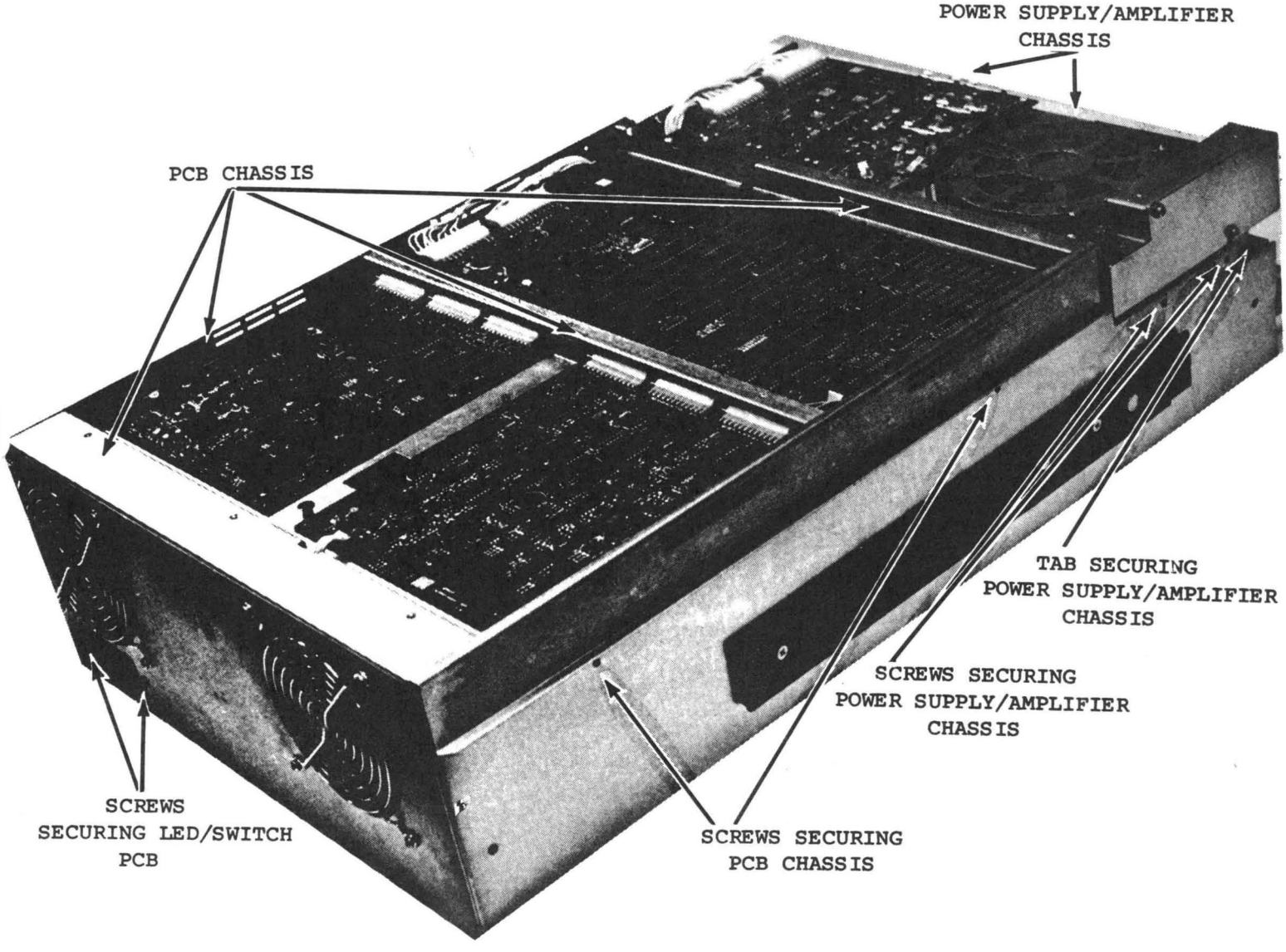


Figure 5-14. REFLEX II Front/Side View

(4) Install P39 on replacement LED/switch PCB. Connector orientation is such that the cable enters the connector on the side for the even numbered pins. Holding P39 with the cable entering on the bottom and looking into the connector sockets, pin 1 is on the left side.

(5) Align one hole of the LED/switch panel with the frame and insert a screw.

(6) Locate the LED/switch PCB to align the LED's with the holes in the panel. The alignment should allow the previously inserted screw to be started into the PCB.

(7) Movement of the PCB will now allow alignment of the second screw hole. Install the second screw and fasten both screws.

(8) Close the PCB chassis and reinstall the two screws, securing the chassis in place.

Electromechanical Assemblies

1. Sealed Module and Motor Assembly

(1) Remove power from the unit.

(2) Remove two screws securing PCB chassis and two screws securing power supply/amplifier chassis (reference Figure 5-14).

(3) Swing open both the PCB chassis and the power supply/amplifier chassis.

(4) Remove P30, P6, P7, and ground terminal from E1 of module assembly. If applicable, also P22 (reference Figure 5-15).

(5) Using a 7/16-in. hex nut driver (or equivalent), remove four nuts securing the module and motor assembly to the shock mounts on the frame.

(6) Lift entire module and motor assembly from the frame.

(7) To replace, reverse steps (1) through (6) and verify disc drive operations.

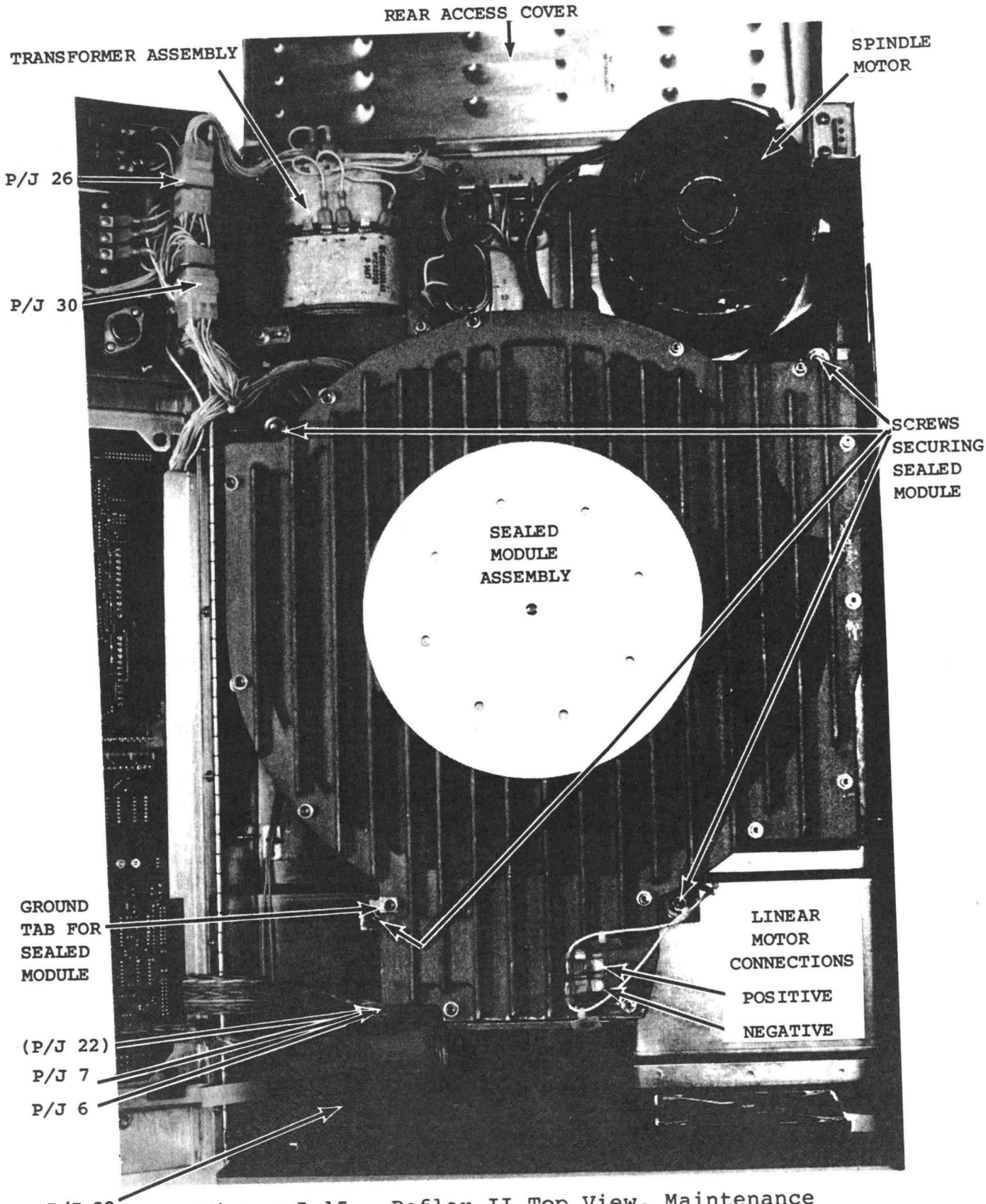


Figure 5-15. Reflex II Top View, Maintenance

2. Cooling Fan(s)

(1) Remove power from the unit.

(2) Remove two screws securing PCB chassis and swing open the PCB chassis (reference Figure 5-15).

(3) Remove four screws securing fan and fan guard.

(4) Remove P35 (or P36) from the fan and remove fan from the assembly.

(5) Remove self-locking hardware from the defective fan and install it on new fan.

(6) To replace the fans, reverse steps (1) through (4) while observing proper direction of air flow. Air flow is to be into the drive from front to rear.

3. Transformer Assembly (DC Voltage Supply)

(1) Remove power from the unit. Make certain that there is no connection of any type to a power source.

(2) Remove two screws securing rear cover and remove the rear cover (reference Figure 5-16).

(3) Remove two screws securing power and supply/amplifier chassis.

(4) Remove interface connections (P1, P2, and P3 on logic/interface PCB).

(5) Swing open power supply/amplifier chassis.

(6) Remove P26.

(7) Remove one screw securing transformer assembly to the frame and lift the transformer assembly out through the rear of the unit.

(8) To replace, reverse steps (1) through (7).

(9) Select the proper tap on the transformer (see Power Verification in Section 3).

(10) Verify DC voltages on the power supply/amplifier PCB.

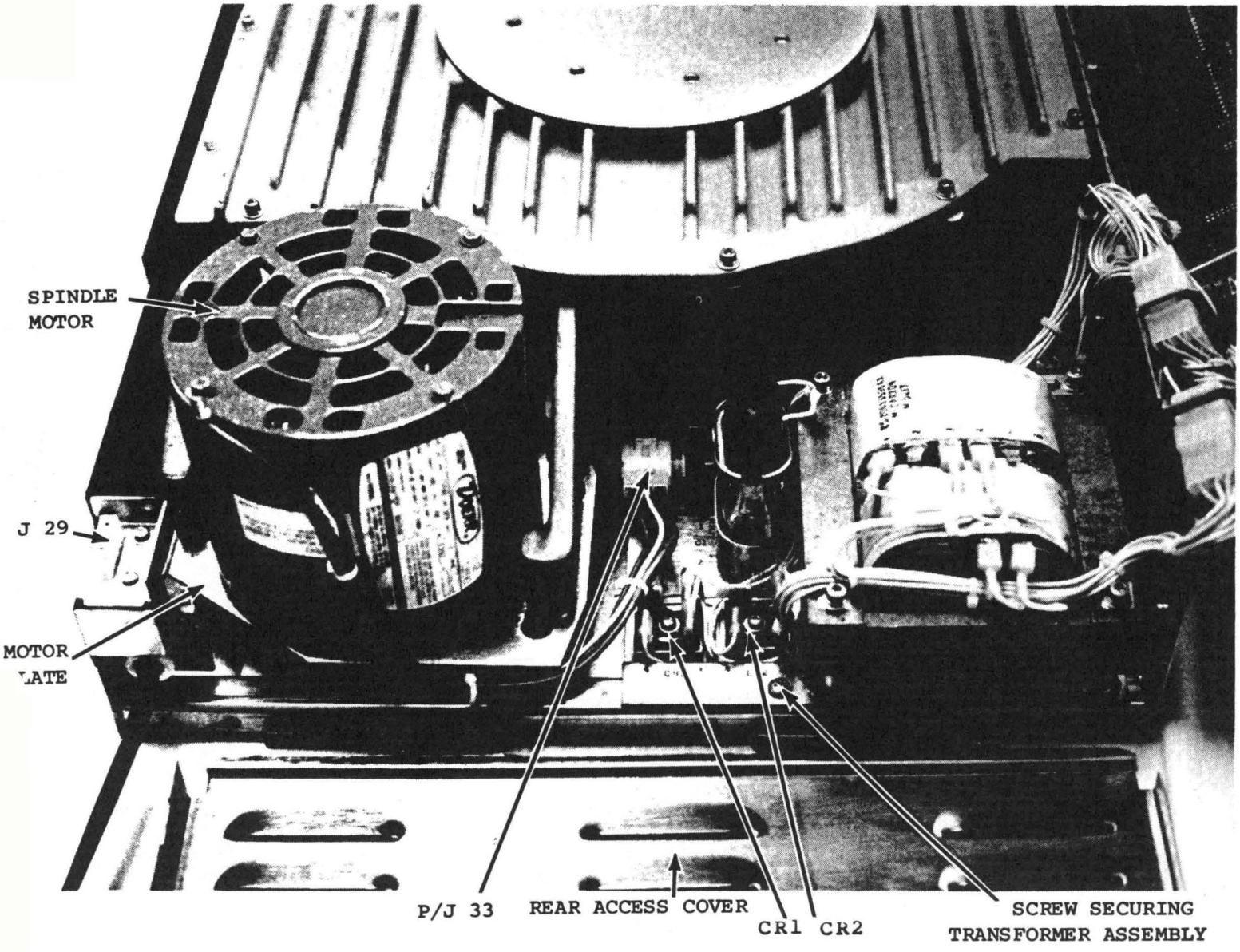


Figure 5-16. Reflex II Rear View

4. Drive Belt

(1) Remove power from the unit.

(2) Remove bottom access cover (reference Figure 5-17).

(3) Squeeze together the drive belt tension spring and remove the belt.

(4) While squeezing the drive belt tension spring, install and align new belt to the spindle and motor pulley centers.

CAUTION: Do not attempt to turn the spindle by hand. Manual rotation of the spindle may cause damage to the heads and/or disc(s).

(5) Apply power to the unit to verify dynamic alignment of the drive belt.

(6) Remove power and replace the bottom access cover, ensuring that there is no interference between the cover and the drive belt or pulleys.

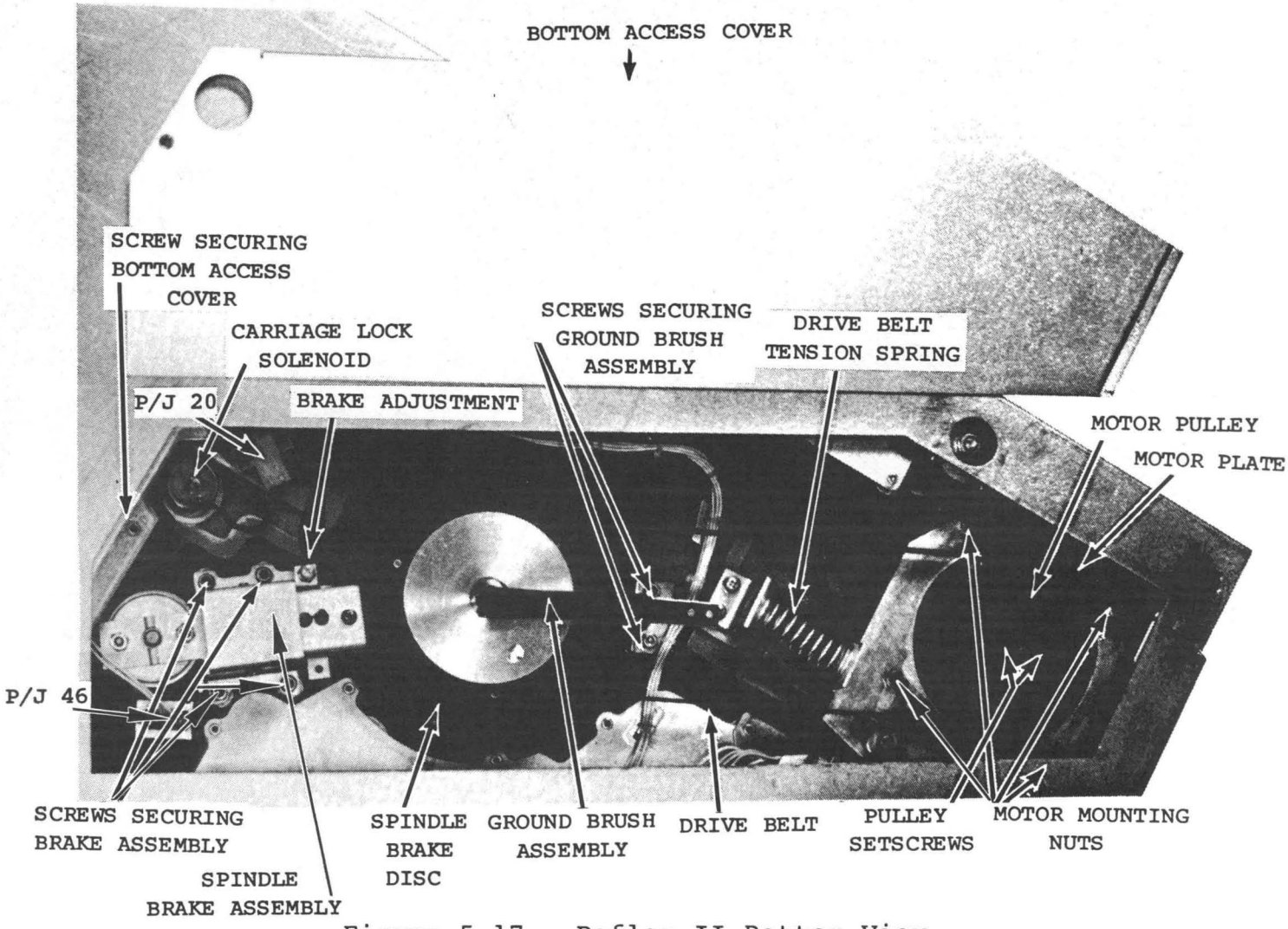


Figure 5-17. Reflex II Bottom View

5. AC Motor Pulley

(1) Remove power from the unit.

(2) Remove bottom access cover (reference Figure 5-17).

(3) Remove drive belt. Note "caution" under drive belt replacement.

(4) Using a 3/32-in. Allen wrench, remove two Allen screws (one piggy back on the other) that secure the pulley to the motor shaft. Note the position of the pulley on the shaft for alignment purposes.

(5) Remove the pulley from the shaft using care not to lose the key. If the pulley has been on the shaft for an extended period, it may be necessary to use a bearing pulley to remove the pulley from the motor shaft.

(6) To replace, reverse steps (1) through (5). Ensure proper alignment of the pulley. When replacing the bottom access cover, make certain that there is no interference between the cover and the drive belt or pulley.

6. AC Spindle Motor

(1) Remove power from the unit.

(2) Remove bottom access cover (reference Figure 5-17).

(3) Remove rear access cover (reference Figure 5-16).

(4) Remove drive belt; note "caution" under drive belt replacement.

(5) Remove the motor pulley (reference AC Motor Pulley replacement). This is necessary only if the old pulley is required for the new motor.

(6) Using an 11/32-in. open end or box wrench, remove the four nuts securing the motor to the motor plate.

(7) Remove the two screws securing the power supply/amplifier chassis (reference Figure 5-14).

(8) Remove the interface connections (P1, P2 and P3 on the logic/interface PCB) and swing open the power supply/amplifier chassis.

(9) Remove P33 and lift the motor from the disc drive.

(10) To replace, reverse steps (1) through (9).

7. AC Motor Plate

This procedure is included primarily to provide an illustration of the hardware stackup for the motor plate mounting

(see Figure 5-18). To replace the motor plate, perform the module and motor assembly replacement, and the AC spindle motor replacement (as it applies with the module out of the frame). Use a 5/32-in. Allen wrench to remove the screws securing the plate to the module.

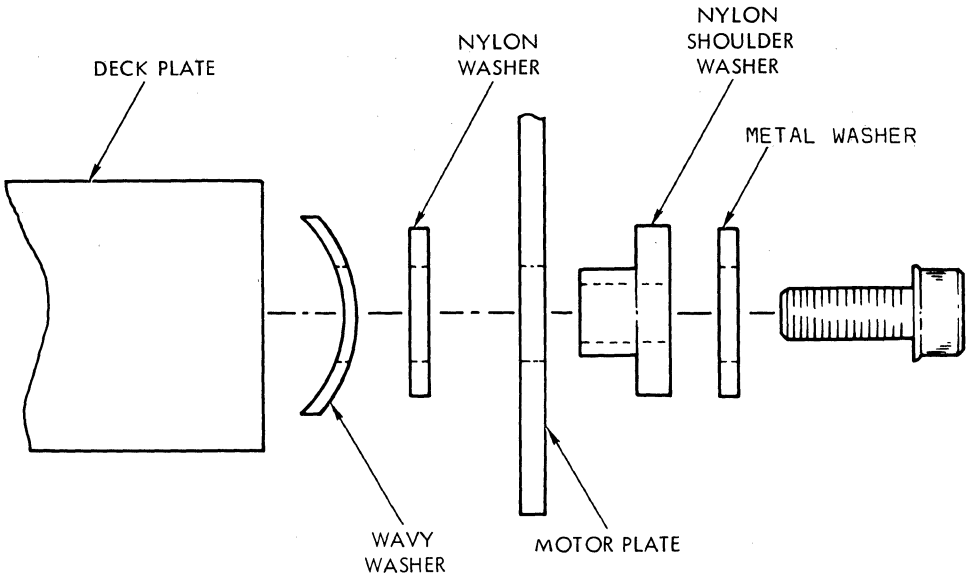


Figure 5-18. Motor Plate Hardware

8. Ground Brush Assembly

(1) Remove power from the unit.

(2) Remove the bottom access cover (reference Figure 5-17).

(3) Using a 5/32-in. Allen wrench, remove the two screws securing the ground brush assembly to the deck plate.

(4) Remove the ground brush assembly.

NOTE: When replacing the ground brush assembly it is necessary to acquire both the ground brush assembly and the ground brush damper since they are separate parts. The ground brush damper must be glued into the ground brush assembly.

(5) To replace, reverse steps (1) through (4) ensuring that the ground brush damper is in place and that there is no interference between the bottom access cover and the drive belt, pulley, or ground brush damper.

9. Brake Assembly

(1) Remove power from the unit.

(2) Remove the bottom access cover (reference Figure 5-17).

(3) Remove P46 from the brake assembly.

> CAUTION: Care must be exercised to prevent rotation of the spindle. Manual rotation of the spindle may cause damage to the heads and/or disc(s).

(4) Using a 5/32-in. Allen wrench, remove the four screws securing the brake assembly to the deck plate.

(5) Using care not to rotate the brake disc, release the brake pads from the disc and remove the brake assembly.

(6) To replace, reverse steps (3) through (5).

(7) Verify the brake assembly adjustment.

10. Line Filter Assembly

(1) Remove power from the unit, ensuring that the AC power cord is disconnected from the power source.

(2) Remove the interface cover and interface connections (P1, P2, and P3 on the logic/interface PCB).

(3) Remove the two screws securing the power supply/amplifier chassis (reference Figure 5-14).

(4) Remove the two screws securing the cover over the line filter assembly and remove the cover.

(5) Open the power supply/amplifier chassis.

(6) Remove P29 from the chassis (reference Figure 5-19).

(7) Remove the wires from S-1 that go to the line filter. If necessary, reference the line filter drawing in Section 6 for reconnection.

(8) Remove the two screws securing the line filter assembly to the chassis and remove the line filter assembly.

(9) To replace, reverse steps (1) through (8), locating P29 in the chassis so that the tab release is toward the outside of the unit.

The kit will satisfy tool requirements for miscellaneous maintenance, adjustments, troubleshooting, and procedures described in this section. There are no other special tools or equipment required. Since the sealed module assembly must be replaced as a single unit, there is no need for special cleaning agents or alignment tools.

SECTION 6

PARTS LIST, ASSEMBLY DRAWINGS AND SCHEMATICS

INTRODUCTION

This section presents information on service parts. Included are drawings, schematics, and photographs that will provide maintenance assistance by identifying the service part and item location. Also included are assembly/disassembly and troubleshooting aids.

The part number list is presented in an indented format. This shows the parts under the assembly of which they are a part. The left column lists the number of items within each given assembly.

PARTS LIST

TABLE 6-1

REFLEX II PART NUMBER AND DESCRIPTION

No. of Items	Part Number	Description	Page No.
	A20013600-XXX	Reflex II disc drive, XXX definition	6-4, 5, 6, 7
	AB20013600	Assembly/detail breakdown, Reflex II drive assembly	6-8
1	. A20013595-XXX	Assembly module and motor XXX defined on drawing	6-9
1	. . A20013065	Spindle motor assembly	6-10
2	. . A20013593-XXX	Assembly, sealed module, XXX defined on drawing	6-11
1-2-1	. . . . . A20013039	Brake assembly	6-12
1-2-9	. . . . . D20013322	Damper, ground brush	6-13
1-2-30	. . . . . CS20013069	Ground brush assembly	6-13
1-2-16	. . . . . D20013147	Washer, motor plate	6-14
1-2-17	. . . . . D20013148	Shoulder washer	6-14
1-2-7	. . . . . A20013654	Cable assembly, sealed module	6-15

TABLE 6-1 (Cont'd)

No. of Items	Part Number	Description	Page No.
4	. . D20013083-XXX	Pulley, motor, XXX defined on drawing	6-16
5	. . D20013085-XXX	Belt, drive, XXX defined on drawing	6-16
8	. . SP52040009	Setscrew, 10-32 x 5/16-in. (motor pulley)	
10	. . SP52290013	Spring, compression	
2	. A20013597-XXX	Transformer assembly, XXX defined on drawing	6-17
3	. A20013599	Frame assembly	6-18, 19, 20, 21
2	. . A20013650	Cable assembly, servo	
3	. . A20013651	Cable assembly, read,write	
4	. . A20013610	PCB, read/write	6-22
5A	. . A20013609	PCB, servo	6-23
5B	. . A20013711	PCB, servo	6-24
6	. . A20013608	PCB, logic/interface	6-25
7	. . A20013598	Power supply/amplifier assembly	6-26
1	. . . A20013588	Motor switch solid state	6-27
2	. . . A20013594	Line filter assembly	6-28
3	. . . A20013607	PCB, power supply/amplifier	6-29
14	. . . . SP54370036	Fuse 3A 3AG 250V F5, F6	
16	. . . . SP54370013	Fuse 5A 3AG 125V S/B F1 through F4	
20	. . . SP53300045	Switch, toggle DPST S1	
21	. . . SP54370039	Fuse 10A 250V S/B ceramic F1	
22	. . . SP53410019	Relay, solid state 240V K1	
8	. . A20013653	Cable assembly, frame	6-30
15	. . SP53450019	Fan, cooling 105 CFM	
4	. A20013301	PCB, terminator	6-31
7	. A20013323	PCB, lead/switch (operator panel)	6-32
8	. A20013327-001	Cable assembly, Led/switch I/O conductor	
13	. D20013324	Panel, led system	
14	. D20013633	Cover, rear screw	
15	. D20013634	Cover, interface	
16	. D20013631	Cover, PCB chassis	
18	. D20013615	Cover, power supply, amplifier PCB	

TABLE 6-2

REFLEX II OPTIONS

Part Number	Description	Page No.
A20013323	Operator indicator panel	
A20013327-001	Cable, indicator panel	
A20013597-XXX	Transformer assembly (DC power supply)	6-17
CS20013337	Chassis slides	6-32
CS20013577	Fixed head-per-track	
. A20013657	Read/write cable--fixed head	

TABLE 6-3

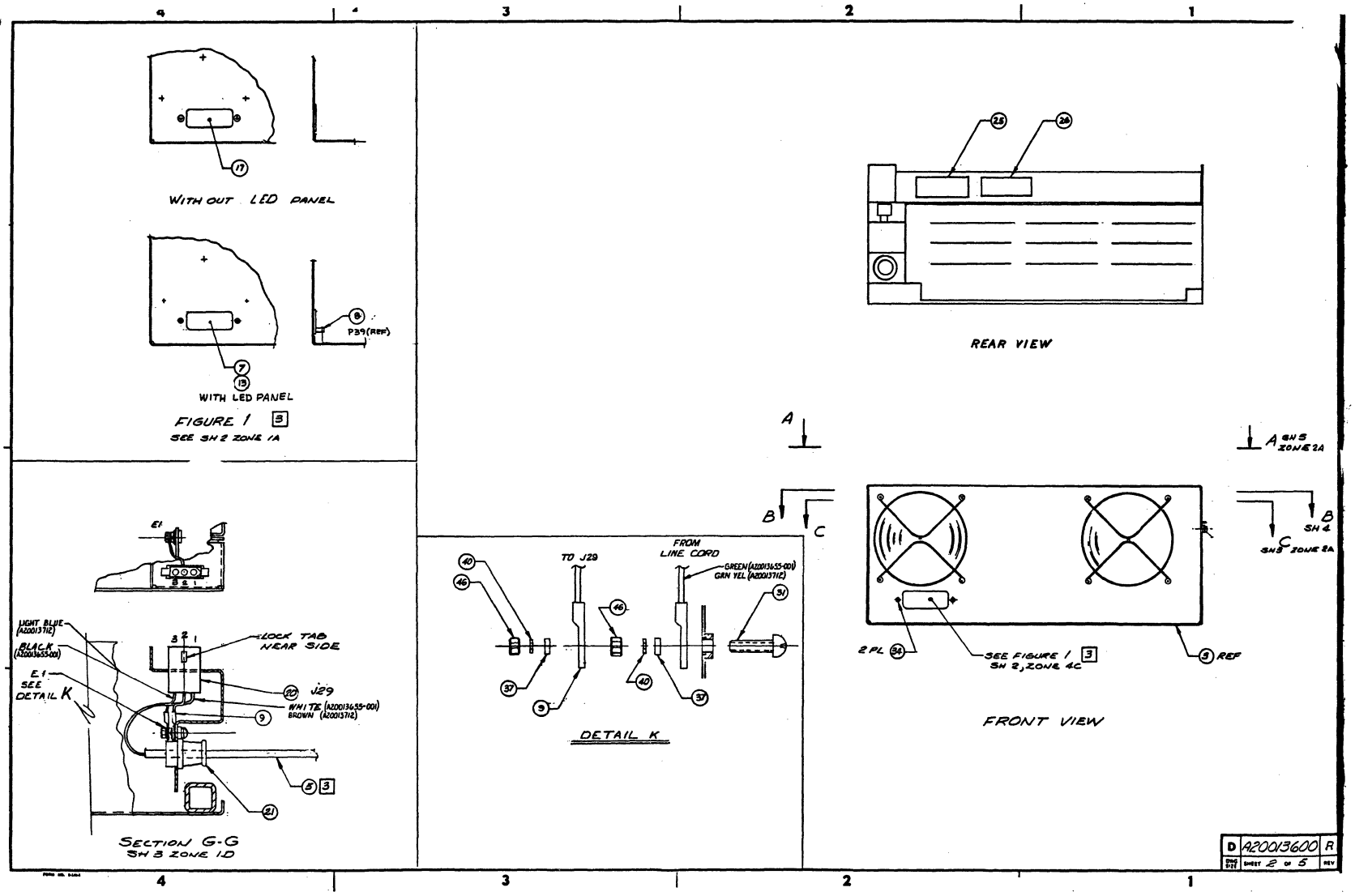
REFLEX II ACCESSORIES

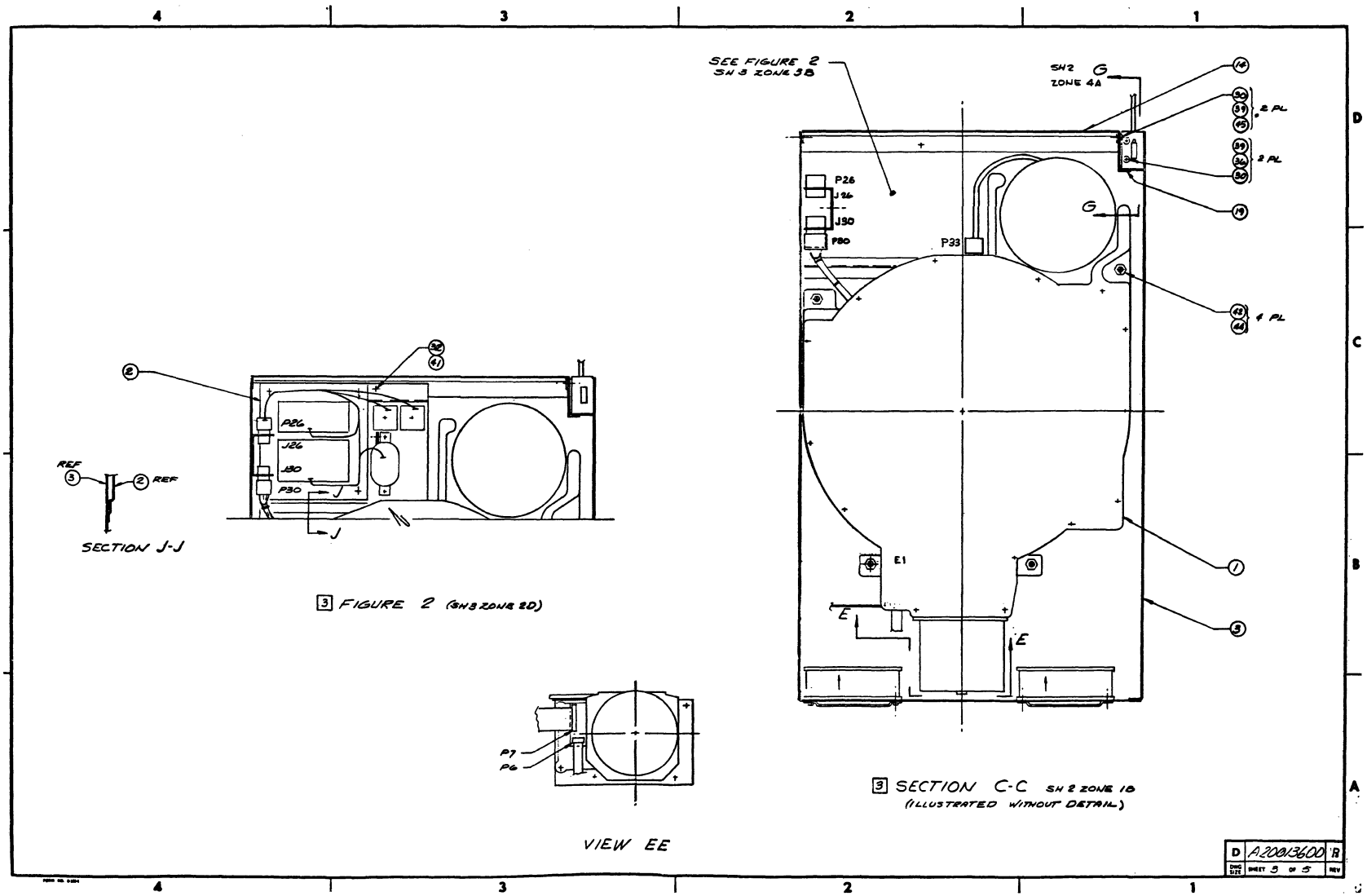
Part Number	Description	Page No.
A20000979-XXX	Data interface cable (26 cond.) XXX defined on drawing	6-33
A20013339	Signal interface cable (60 cond., 5 feet)	6-34
A20013301-001	Cable terminator assembly	6-30
A20013340	Exerciser, Mod III	6-35

TABLE 6-4

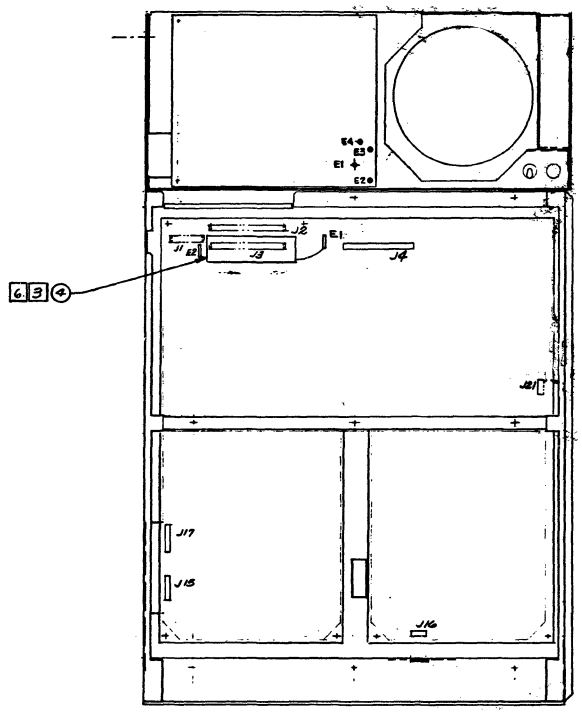
REFLEX II SCHEMATICS

Part Number	Description	Page No.
WD20013600	Wiring diagram, Reflex II	6-37
SC20013606	Schematic, head connectors	6-38
SC20013607	Schematic, power supply/amplifier	6-39, 40
SC20013608	Schematic, logic/interface	6-41 through 6-62
SC20013609	Schematic, servo	6-62, 63, 64, 65
BD20013609	Block/timing diagram, servo	6-66, 67, 68
SC20013610	Schematic, read/write	6-69, 70, 71, 72
SC20013301	Schematic, terminator	6-73
SC20013323	Schematic, led/switch	6-74


WITH OUT LED PANEL
WITH LED PANEL
P39 (REF)
FIGURE 1 3
SEE SH 2 ZONE 1A
REAR VIEW
FRONT VIEW
2 PL
SEE FIGURE 1 3 SH 2, ZONE 4C
REF
SECTION G-G
SH 3 ZONE 1D
LOCK TAB NEAR SIDE
LIGHT BLUE (A2001371Z)
BLACK (A2001365S-001)
E1 SEE DETAIL K
J29
WHITE (A2001365S-001)
BROWN (A2001371Z)
DETAIL K
TO J29
FROM LINE CORD
GREEN (A2001365S-001)
GRN YEL (A2001371Z)
SH 5 ZONE 2A
SH 4
SH 5 ZONE 2A
D A2001360O R
SHEET 2 OF 5

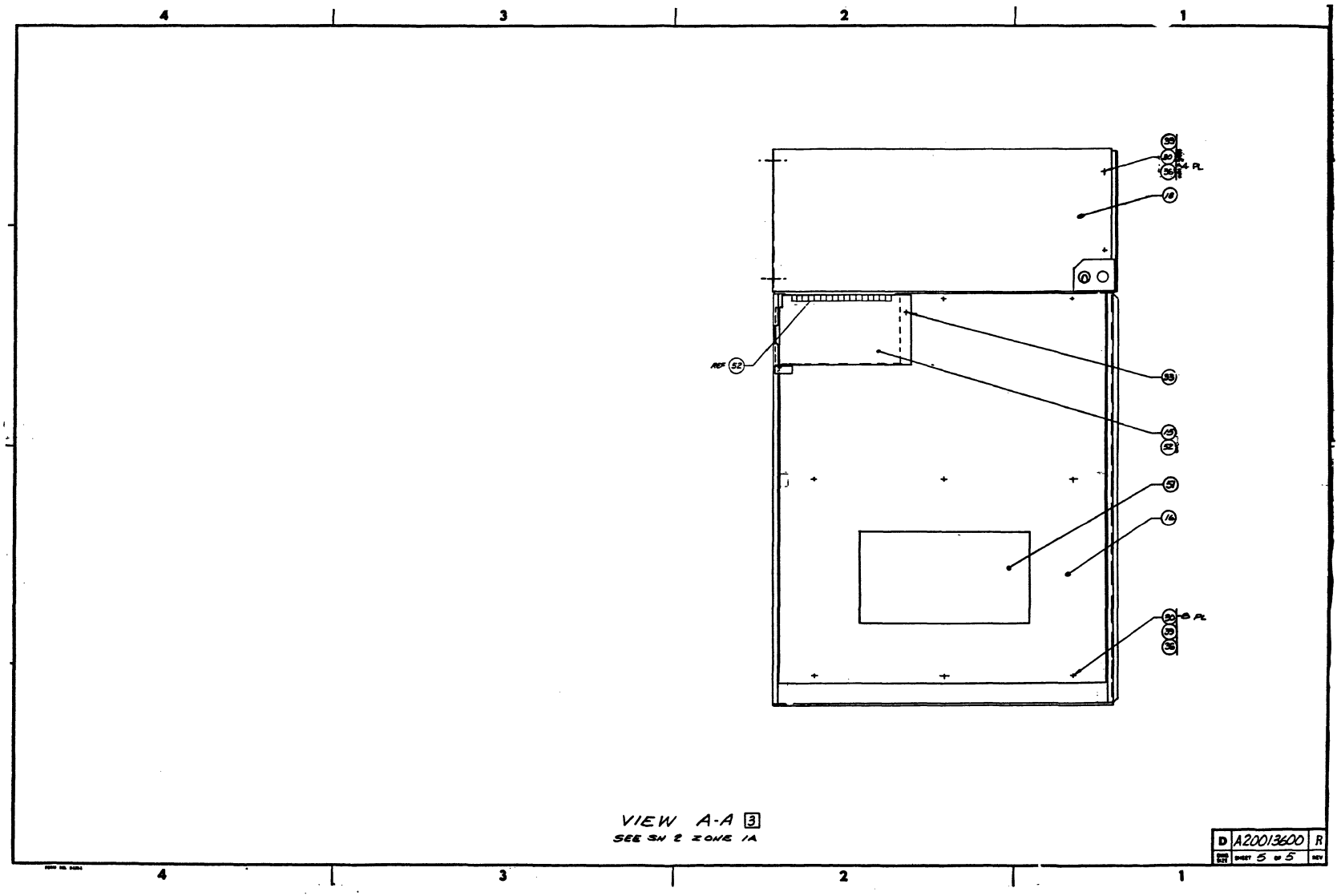


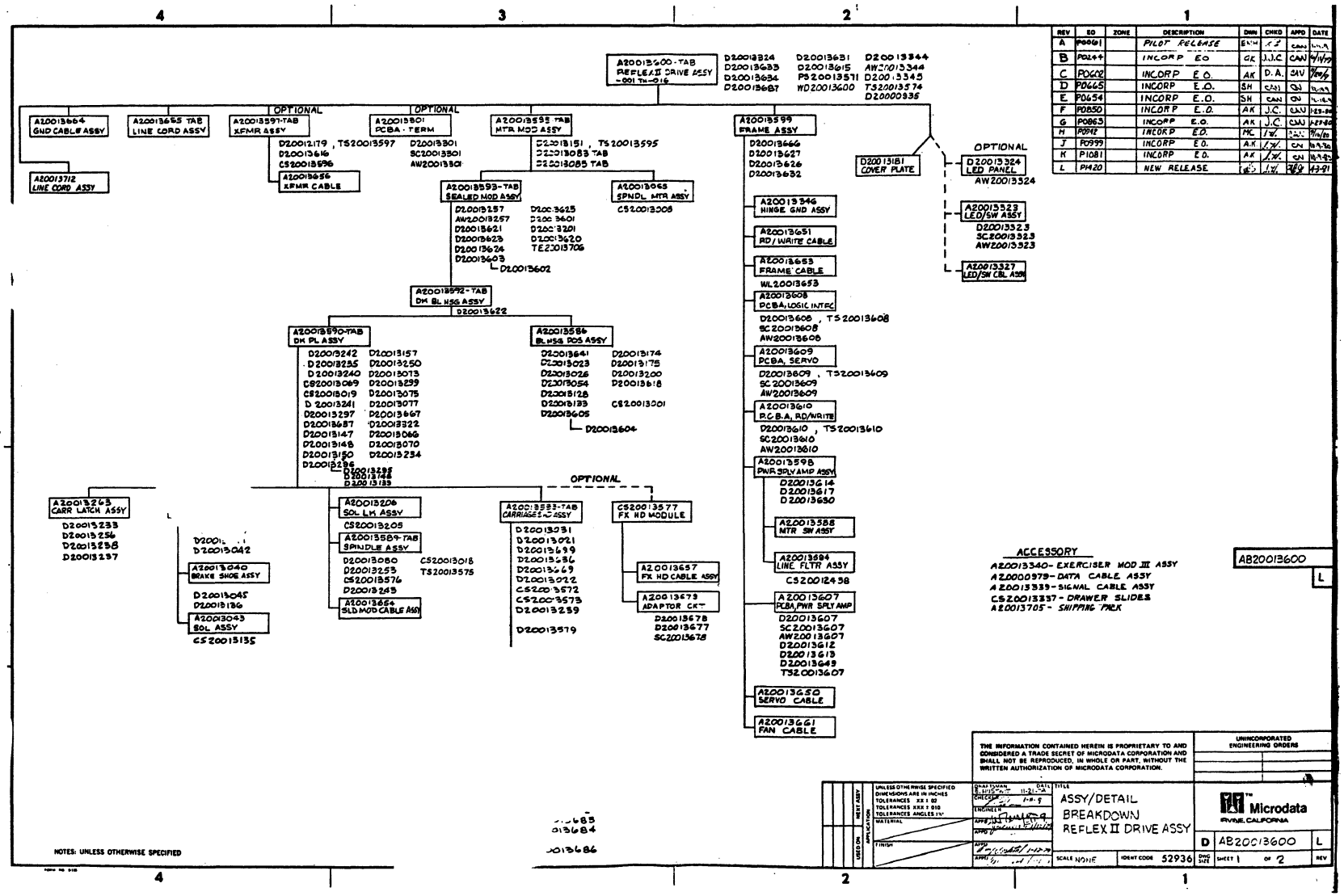
3 FIGURE 2 (SH 3 ZONE 2D)



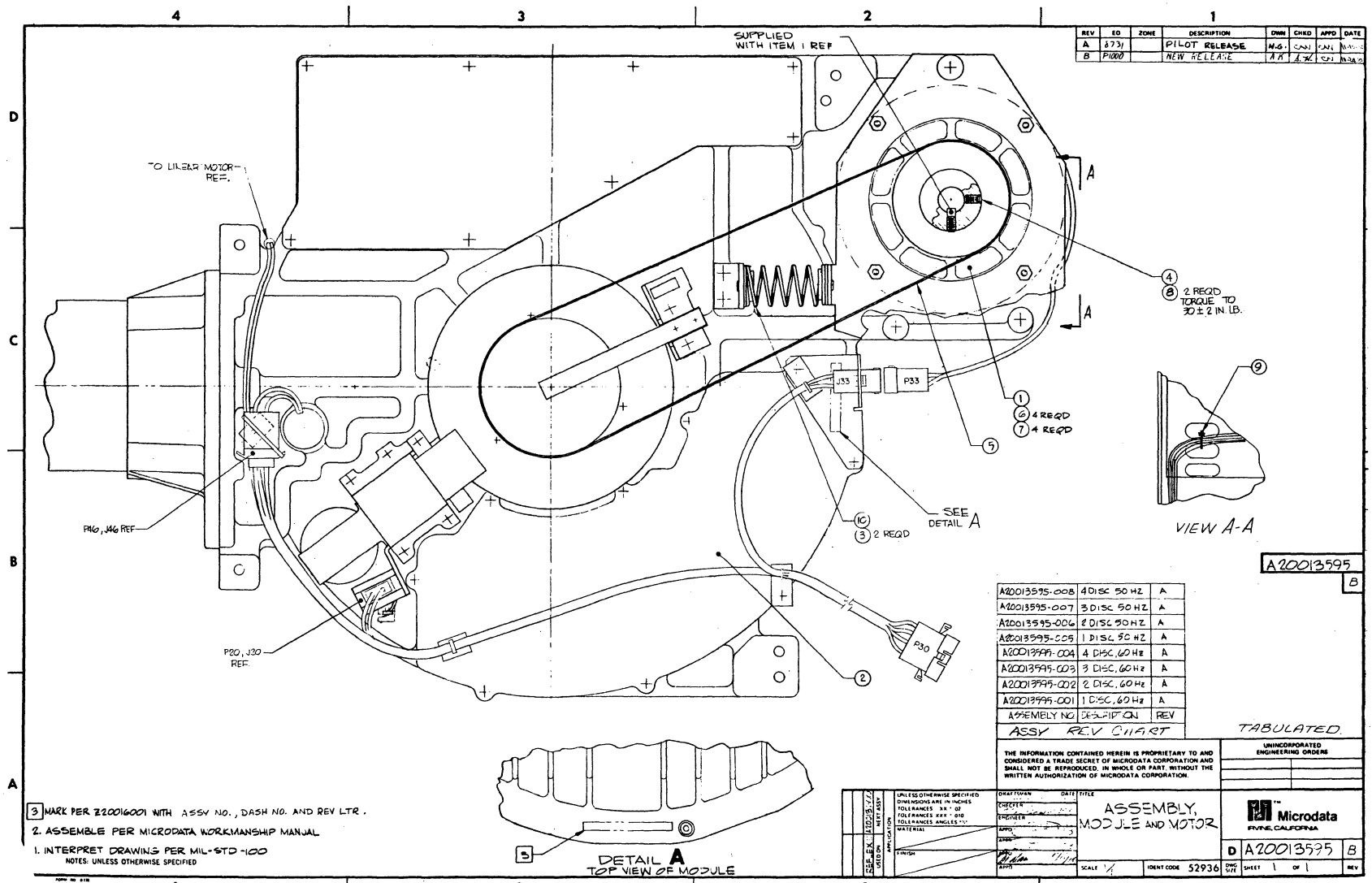
SECTION B-B
SH 2 ZONE 1A

D	A2003600	R
SIZE	SHEET 4 OF 5	REV


4
3
2
1
55
54
56
18
REF 52
53
57
32
59
16
58
39
38
4 PL
6 PL
VIEW A-A 3
SEE SH 2 ZONE 1A
D A20013600 R
SHEET 5 OF 5



REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	P0061		PILOT RELEASE	ENTH	[illegible]	CMN	[illegible]
B	P0144		INCORP EO	GE	J.J.C	CMN	9/11/79
C	P0602		INCORP E.O.	AK	D. A.	CMN	11/6/79
D	P0665		INCORP E.O.	SH	CMN	CMN	[illegible]
E	P0654		INCORP E.O.	SH	CMN	CMN	[illegible]
F	P0850		INCORP E.O.	AK	J.C.	CMN	1-23-80
G	P0863		INCORP E.O.	AK	J.C.	CMN	1-23-80
H	P0948		INCORP E.O.	MC	1/4	CMN	3/11/80
J	P0999		INCORP E.O.	AK	1/4	CMN	4-9-80
K	P1081		INCORP E.O.	AK	1/4	CMN	10-9-80
L	P1420		NEW RELEASE	[illegible]	1/4	[illegible]	11-3-81



REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	8731		PILOT RELEASE	N.G.	CAN	CAN	
B	P1000		NEW RELEASE	AA	A.M.	CAN	

A20013595-008	4 DISC 50 HZ	A
A20013595-007	3 DISC 50 HZ	A
A20013595-006	2 DISC 50 HZ	A
A20013595-005	1 DISC 50 HZ	A
A20013595-004	4 DISC, 60 Hz	A
A20013595-003	3 DISC, 60 Hz	A
A20013595-002	2 DISC, 60 Hz	A
A20013595-001	1 DISC, 60 Hz	A
ASSEMBLY NO	DESCRIPTION	REV

ASSY REV CHART — TABULATED

A20013595 B

3 MARK PER Z20016001 WITH ASSY NO., DASH NO. AND REV LTR.

2. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL

1. INTERPRET DRAWING PER MIL-STD-100

NOTES: UNLESS OTHERWISE SPECIFIED

UNINCORPORATED ENGINEERING ORDERS

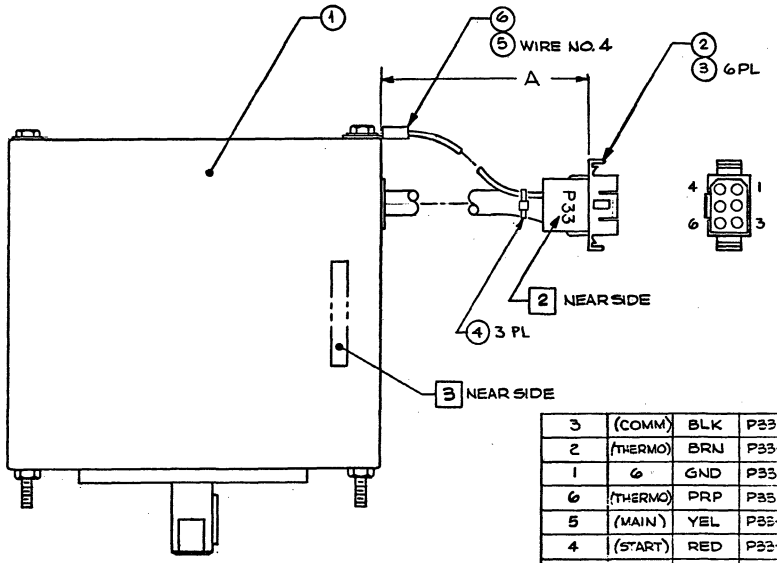
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES XX ± .02
TOLERANCES XXX ± .010
TOLERANCES ANGLES ±°
MATERIAL
FINISH

DRAFTSMAN
CHECKER
ENGINEER
APPD
ADDL
APPD

TITLE: ASSEMBLY, MODULE AND MOTOR

SCALE 1/1 | IDENT CODE 52936 | SIZE D | A20013595 B | SHEET 1 OF 1 | REV

Microdata IRVINE, CALIFORNIA



REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
AX2	6045		PROTO RELEASE AND UPDATED TO CONFORM TO LM	SHA	CAN	[illegible]	1/18/77
AX3	6290		SEE ENG. ORDER	[illegible]	CAN	[illegible]	3/1/77
AX4	6996		SEE ENG ORDER	CN	CAN	[illegible]	7/27/77
A	7212		PILOT RELEASE	CN	CAN	[illegible]	9/6/77
B	7405		SEE ENG ORDER	S.H.	[illegible]	[illegible]	10/31/77
C	7532		SEE ENG ORDER	S.H.	[illegible]	[illegible]	12/12/77
D	7723		SEE ENG ORDER	S.H.	[illegible]	[illegible]	1/31/78
E	8507		NEW RELEASE	S.H.	[illegible]	[illegible]	12/6/79

3	(COMM)	BLK	P33-3	3	11.25±.25
2	(THERMO)	BRN	P33-2	3	11.25±.25
1	6	GND	P33-1	3	13.50±.25
6	(THERMO)	PRP	P33-6	3	11.25±.25
5	(MAIN)	YEL	P33-5	3	11.25±.25
4	(START)	RED	P33-4	3	11.25±.25
WIRE NO.	TERM	FROM	TO	TERM	DIM "A"

WIRE LIST

A20013065 E

A20013065	A
ASSEMBLY NO.	REV LTR

ASSEMBLY REVISION CHART

3. MARK PER Z20016001 WITH PART NUMBER AND REVISION LETTER.
2. MARK REFERENCE DESIGNATION .12 HIGH, COLOR BLACK.
1. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL.

NOTES: UNLESS OTHERWISE SPECIFIED

UNINCORPORATED ENGINEERING ORDERS

REFLEX A20015195 USED ON NEXT ASSY APPLICATION

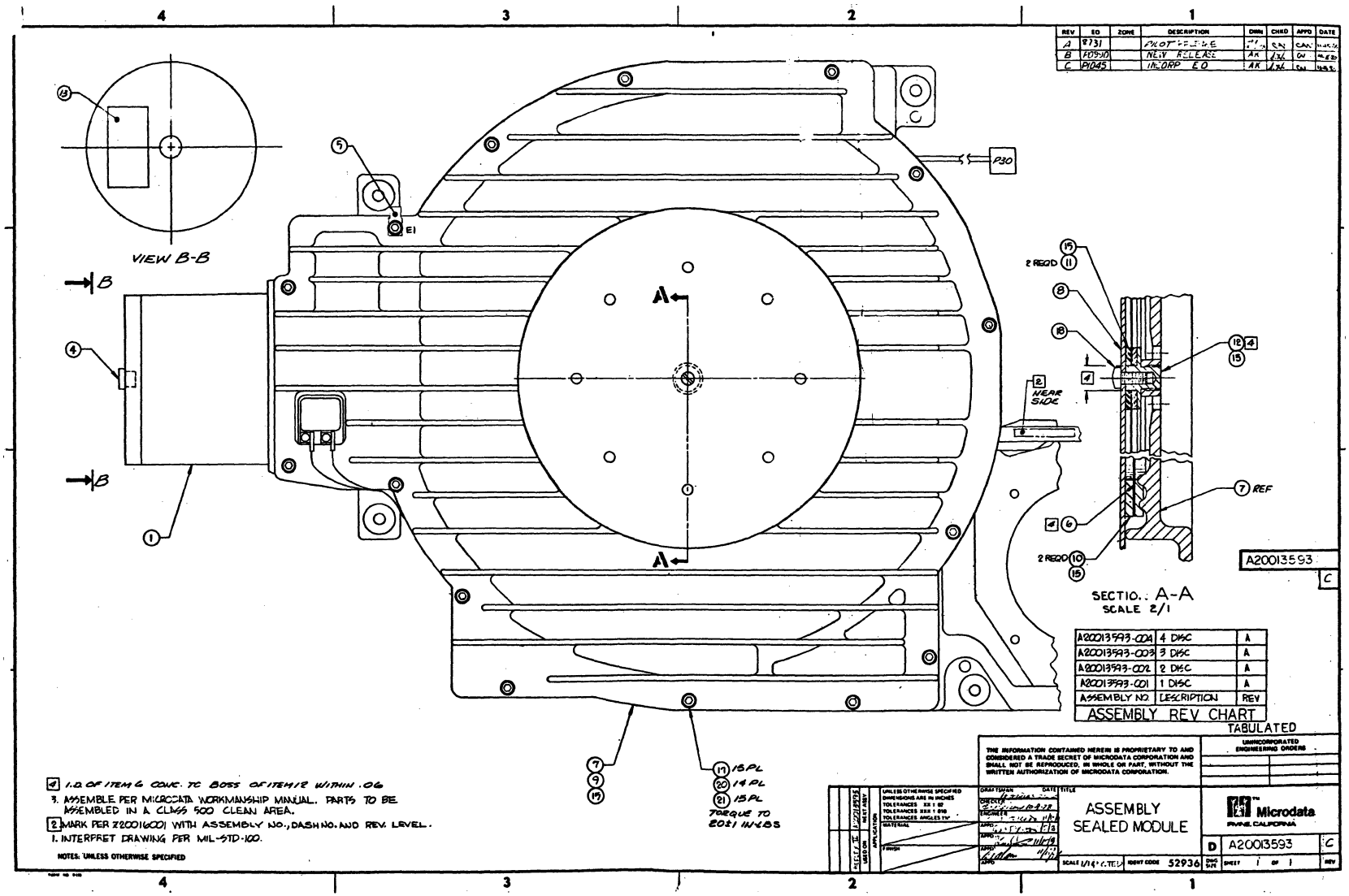
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES .XX ± .02
TOLERANCES .XXX ± .010
TOLERANCES ANGLES 1°
MATERIAL
FINISH

DRAFTSMAN ALEXANDER 1-5-77
CHECKED
ENGINEER 1/-/77
APPD 11-1-77
APPD 9-19-77
APPD 9-22-77

TITLE: SPINDLE MOTOR ASSEMBLY

Microdata IRVINE, CALIFORNIA

SCALE 1/1 IDENT CODE 52936 DWG SIZE C A20013065 E SHEET 1 OF 1 REV



REV	ECO	ZONE	DESCRIPTION	DRWN	CHKD	APPD	DATE
A	9731		PILOT RELEASE			CAN	
B	F0510		NEW RELEASE	AK		CN	
C	P1045		INCORP ECO	AK		CN	

ASSEMBLY NO.	DESCRIPTION	REV
A20013593-004	4 DISC	A
A20013593-003	3 DISC	A
A20013593-002	2 DISC	A
A20013593-001	1 DISC	A

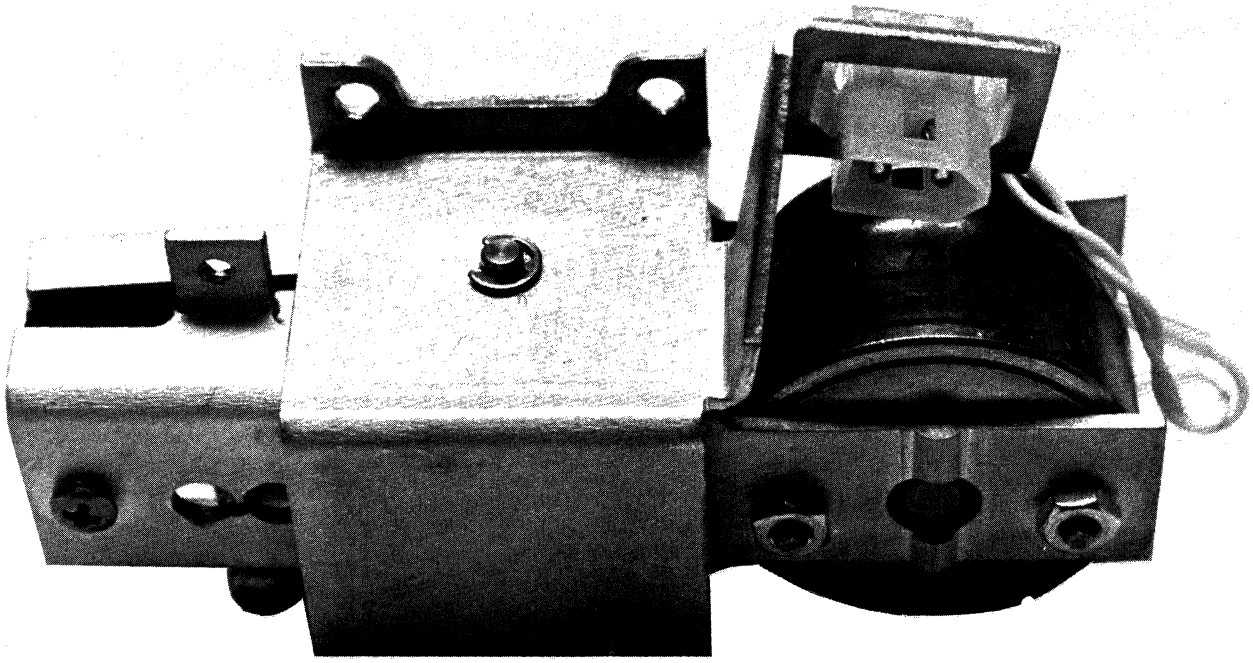
TABULATED

4. I.D. OF ITEM 6 CONC. TO BOSS OF ITEM 12 WITHIN .06
3. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL. PARTS TO BE ASSEMBLED IN A CLASS 500 CLEAN AREA.
2. MARK PER A20016001 WITH ASSEMBLY NO., DASH NO. AND REV. LEVEL.
1. INTERPRET DRAWING PER MIL-STD-100.

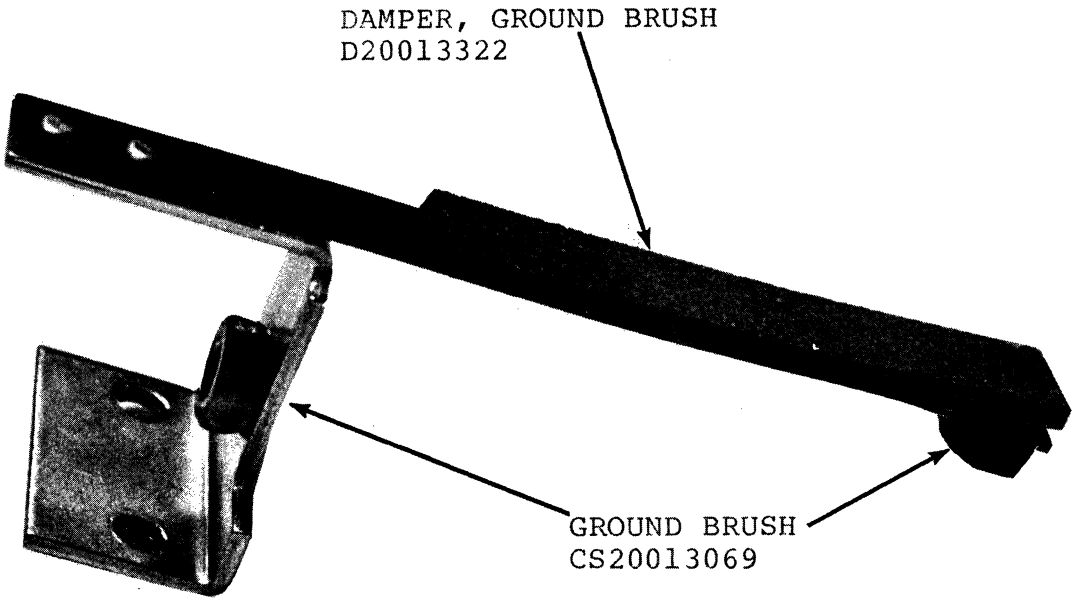
NOTES: UNLESS OTHERWISE SPECIFIED

UNINCORPORATED ENGINEERING ORDERS

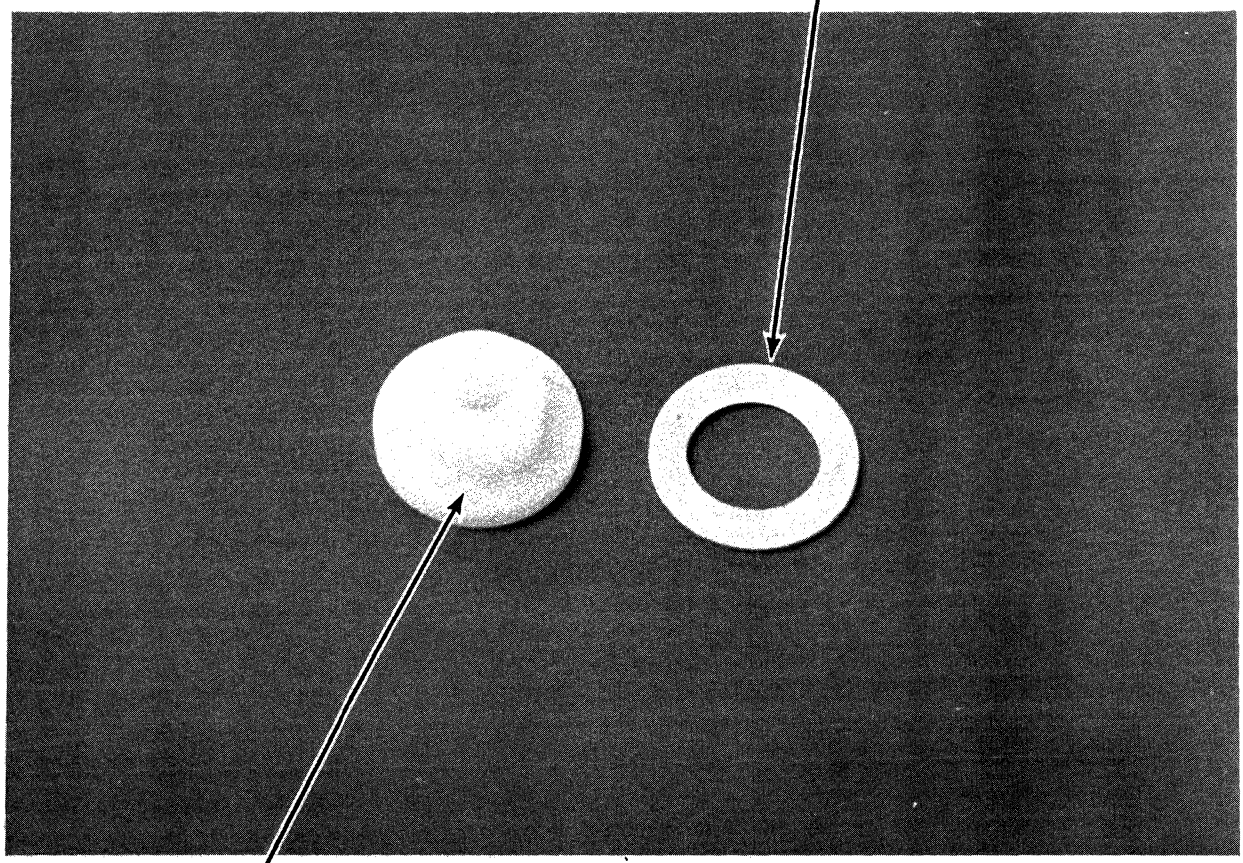
SCALE 1/1 | IDENT CODE 52936 | SHEET 1 OF 1

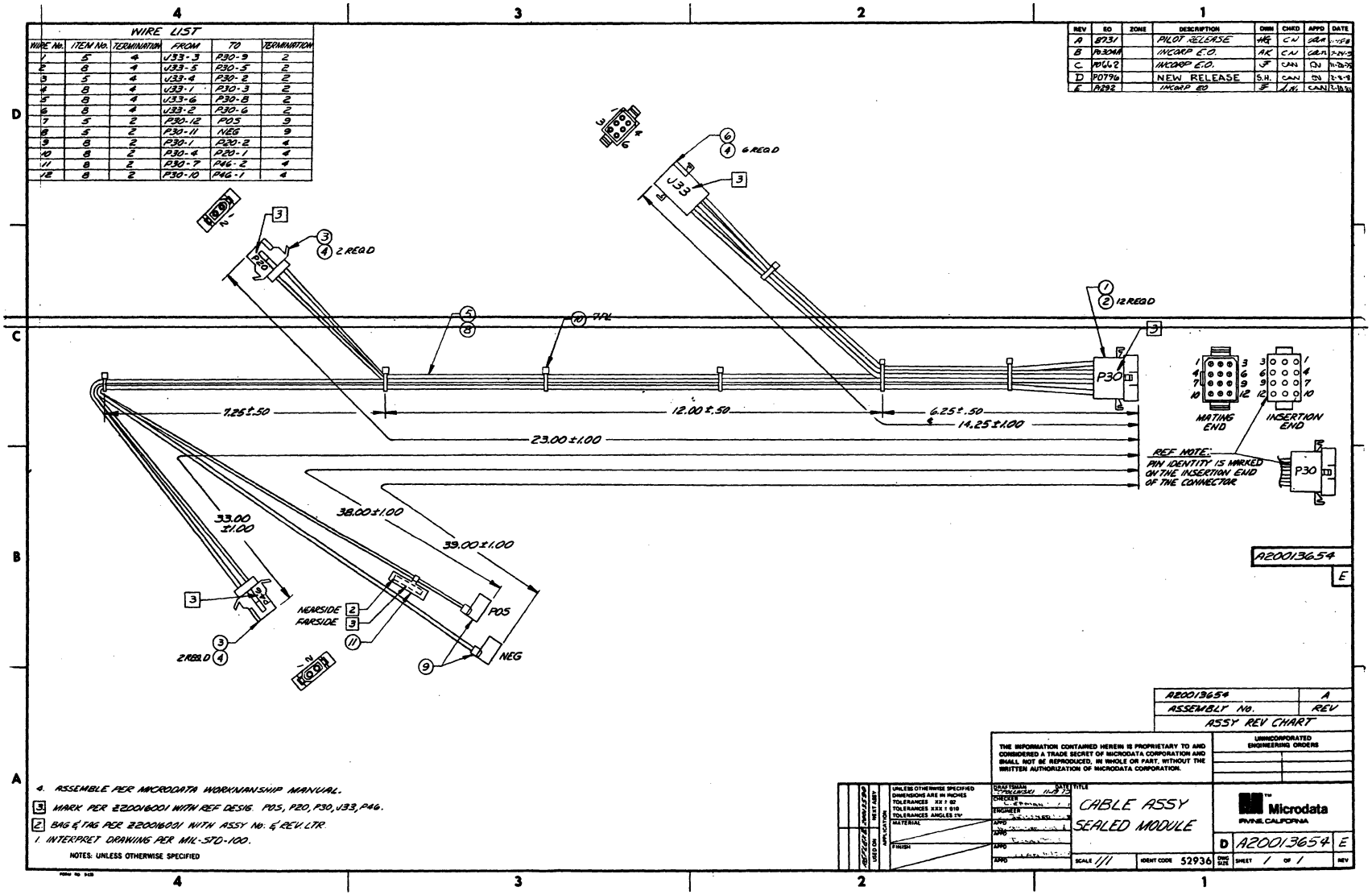


BRAKE ASSEMBLY
A20013039



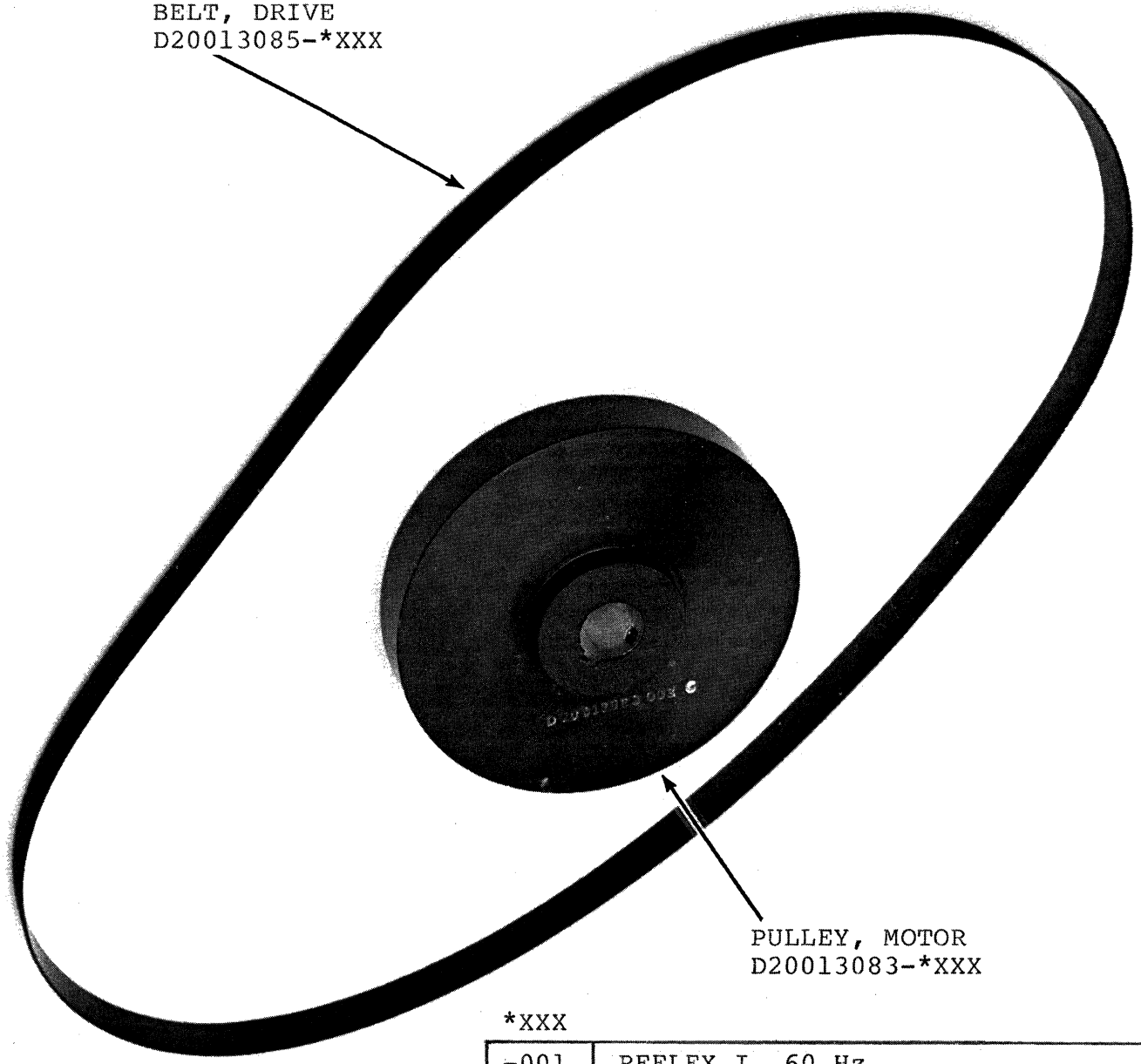
THESE PARTS ARE SUPPLIED AS SEPARATE ITEMS; IF A GROUND BRUSH ASSEMBLY IS REPLACED, BOTH PARTS MUST BE ORDERED AND THE DAMPER MUST BE GLUED TO THE GROUND BRUSH.


WASHER, MOTOR PLATE
D20013147
SHOULDER WASHER
D20013148


WIRE LIST
WIRE No. | ITEM No. | TERMINATION | FROM | TO | TERMINATION
1 | 5 | 4 | J33-3 | P30-9 | 2
2 | 8 | 4 | J33-5 | P30-5 | 2
3 | 5 | 4 | J33-4 | P30-2 | 2
4 | 8 | 4 | J33-1 | P30-3 | 2
5 | 8 | 4 | J33-6 | P30-8 | 2
6 | 8 | 4 | J33-2 | P30-6 | 2
7 | 5 | 2 | P30-12 | POS | 9
8 | 5 | 2 | P30-11 | NEG | 9
9 | 8 | 2 | P30-1 | P20-2 | 4
10 | 8 | 2 | P30-4 | P20-1 | 4
11 | 8 | 2 | P30-7 | P46-2 | 4
12 | 8 | 2 | P30-10 | P46-1 | 4
REV | ECO | ZONE | DESCRIPTION | DWN | CHKD | APPD | DATE
A 8731 PILOT RELEASE HG CN JAA 11-5-8
B P304A INCORP E.O. AK CN CAN 2-24-9
C P0642 INCORP E.O. JF CAN CN 11-20-79
D P0796 NEW RELEASE S.H. CAN CN 2-9-81
E P292 INCORP ECO JF J.M. CAN 2-10-81
J33
P30
P20
P46
6 REQ'D
2 REQ'D
12 REQ'D
TYP
7.25±.50
12.00±.50
6.25±.50
14.25±1.00
23.00±1.00
33.00±1.00
38.00±1.00
39.00±1.00
MATING END
INSERTION END
REF NOTE:
PIN IDENTITY IS MARKED ON THE INSERTION END OF THE CONNECTOR
NEARSIDE
FARSIDE
POS
NEG
A200136-54 E
A200136-54 A
ASSEMBLY No. REV
ASSY REV CHART
4. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL.
3 MARK PER 22001600I WITH REF DESIG. P05, P20, P30, J33, P46.
2 BAG & TAG PER 32001600I WITH ASSY No. & REV. LTR.
1. INTERPRET DRAWING PER MIL-STD-100.
NOTES: UNLESS OTHERWISE SPECIFIED
THE INFORMATION CONTAINED HEREIN IS PROPRIETARY TO AND CONSIDERED A TRADE SECRET OF MICRODATA CORPORATION AND SHALL NOT BE REPRODUCED, IN WHOLE OR PART, WITHOUT THE WRITTEN AUTHORIZATION OF MICRODATA CORPORATION.
UNINCORPORATED ENGINEERING ORDERS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES XX ± 02
TOLERANCES XXX ± 010
TOLERANCES ANGLES ±1°
MATERIAL
FINISH
DRAFTSMAN
CHECKER
ENGINEER
APPD
CABLE ASSY SEALED MODULE
Microdata IRVINE, CALIFORNIA
D A200136-54 E
SCALE /// IDENT CODE 52936 SIZE SHEET 1 OF 1 REV

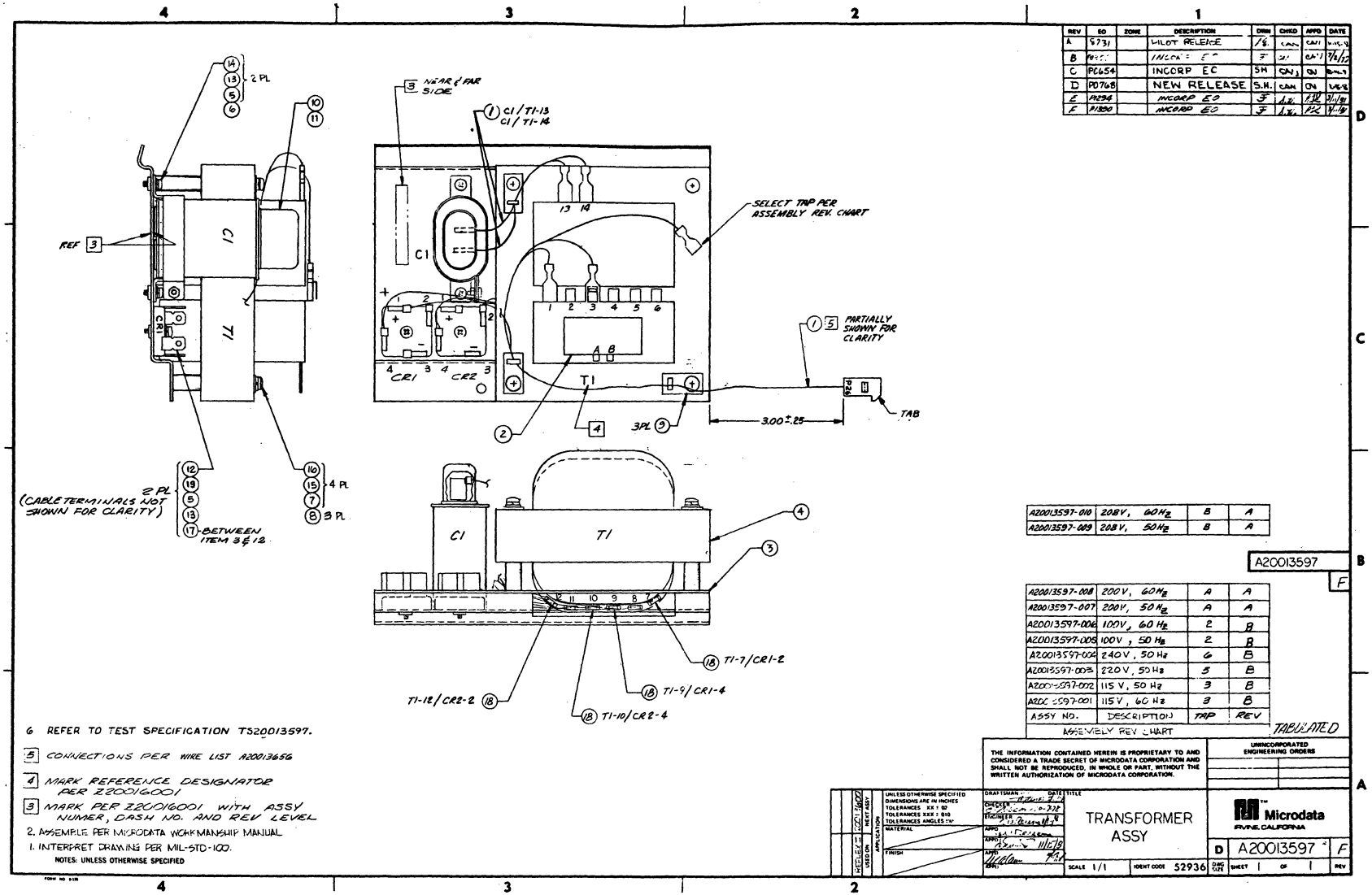
*XXX

-001	REFLEX I, 60 Hz
-002	REFLEX I, 50 Hz; REFLEX II, 60 Hz
-003	REFLEX II, 50 Hz



*XXX

-001	REFLEX I, 60 Hz
-002	REFLEX I, 50 Hz; REFLEX II, 60 Hz
-003	REFLEX II, 50 Hz



REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	5731		PILOT RELEASE	JF	CAN	CAN	11-15-77
B	P0551		INCORP EC	JF	CAN	CAN	2/1/78
C	PC654		INCORP EC	SH	CAN	CAN	5-1-78
D	PD768		NEW RELEASE	S.H.	CAN	CAN	8/8/78
E	P1294		INCORP EC	JF	J.K.	P.L.	3/1/79
F	P1390		INCORP EC	JF	J.K.	P.L.	3/1/79

A20013597-010	208V, 60Hz	B	A
A20013597-009	208V, 50Hz	B	A

A20013597 F

A20013597-008	200V, 60Hz	A	A
A20013597-007	200V, 50Hz	A	A
A20013597-006	100V, 60Hz	2	B
A20013597-005	100V, 50Hz	2	B
A20013597-004	240V, 50Hz	6	B
A20013597-003	220V, 50Hz	5	B
A20013597-002	115V, 50Hz	3	B
A20013597-001	115V, 60Hz	3	B
ASSY NO.	DESCRIPTION	TAP	REV

ASSEMBLY REV CHART — TABULATED

6 REFER TO TEST SPECIFICATION T520013597.

5 CONNECTIONS PER WIRE LIST A20013656

4 MARK REFERENCE DESIGNATOR PER Z20016001

3 MARK PER Z20016001 WITH ASSY NUMBER, DASH NO. AND REV LEVEL

2. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL

1. INTERPRET DRAWING PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

UNINCORPORATED ENGINEERING ORDERS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES XX ± 10
TOLERANCES XXX ± 010
TOLERANCES ANGLES ±1°
MATERIAL
FINISH

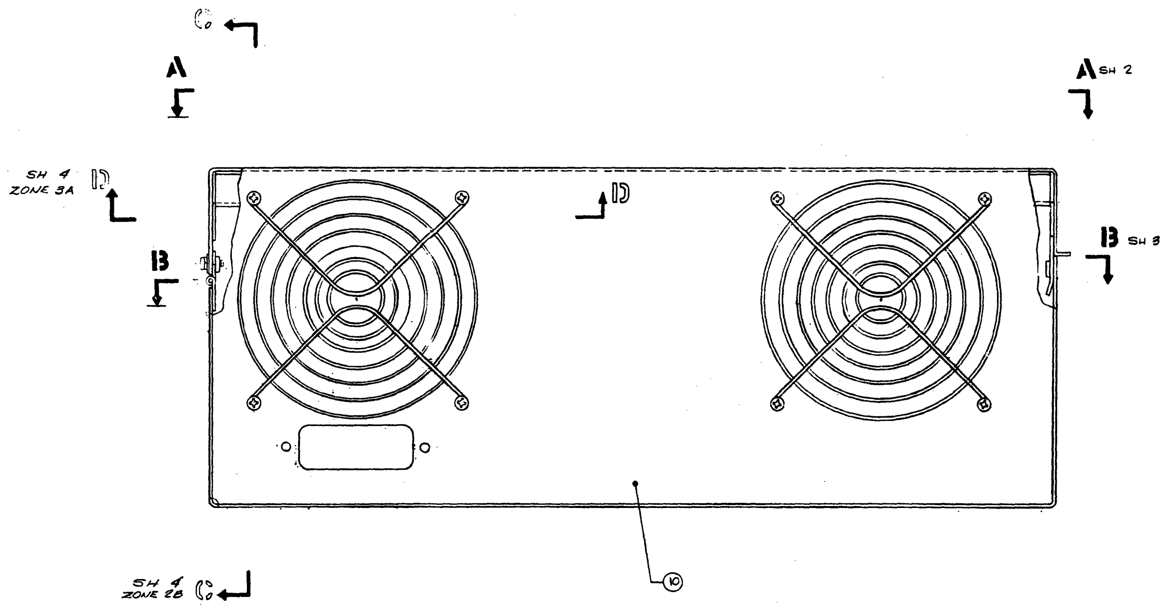
DRAFTSMAN — DATE
CHECKER — DATE
ENGINEER — DATE
APPD — DATE
APPD — DATE

TITLE: TRANSFORMER ASSY

Microdata IRVINE, CALIFORNIA

SCALE 1/1 IDENT CODE 52936 DWG SIZE D A20013597 F SHEET 1 OF 1 REV

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	8731		PILOT RELEASE	[illegible]	[illegible]	CAN	11-15-[illegible]
B	P0244		INCORP EO	[illegible]	J.J.C.	CAN	6/[illegible]/79
C	P0529		INCORP E.O.	AK	J.C.	CWJ	1-23-80
D	P0535		[illegible]	[illegible]	[illegible]	CWJ	1-23-80
E	P0850		INCORP E.O.	AK	J.C.	CAN	1-23-80
F	P0838		INCORP E.O.	A.K.	J.C.	CAN	1-23-80
G	P0987		NEW RELEASE	AK	[illegible]	CN	10-1-80
H	P1156		INCORP E.O.	AK	[illegible]	CN	10-1-80
J	P1160		INCORP E.O.	AK	[illegible]	CN	10-1-80
K	P1375		INCORP E.O.	[illegible]	[illegible]	[illegible]	3/11/81



A20013599

K

5. ON ASSEMBLIES USING D20013608 (REV P AND R) DETAIL BOARDS ONLY CUT R51 AND R52 LEADS CLOSEST TO THE EDGE OF THE BOARD (A20013608) SO THEY ARE FLUSH WITH THE BOARD. ADD A PIECE OF INSULATING TAPE (SP50650022), APPROXIMATELY 1 INCH SQUARE WITH A 1/4 INCH HOLE CUT IN THE CENTER TO THE PCB CHASSIS (D20013626) BETWEEN PRINTED CIRCUIT BOARD AND TAB.

4. MARK REF DESIGNATIONS PER Z20016001.

3. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL.

2. MARK PER Z20016001 WITH ASSY NO., DASH NO. AND REV LETTER.

1. INTERPRET DRAWING PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

A20013599	D
ASSY NO.	REV
ASSEMBLY REV. CHART	

THE INFORMATION CONTAINED HEREIN IS PROPRIETARY TO AND CONSIDERED A TRADE SECRET OF MICRODATA CORPORATION AND SHALL NOT BE REPRODUCED, IN WHOLE OR PART, WITHOUT THE WRITTEN AUTHORIZATION OF MICRODATA CORPORATION.

UNINCORPORATED ENGINEERING ORDERS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES .XX ± .02 TOLERANCES .XXX ± .010 TOLERANCES ANGLES ±1°

MATERIAL

FINISH

NEXT ASSY: A20013[illegible] — USED ON: REFLEX II — APPLICATION

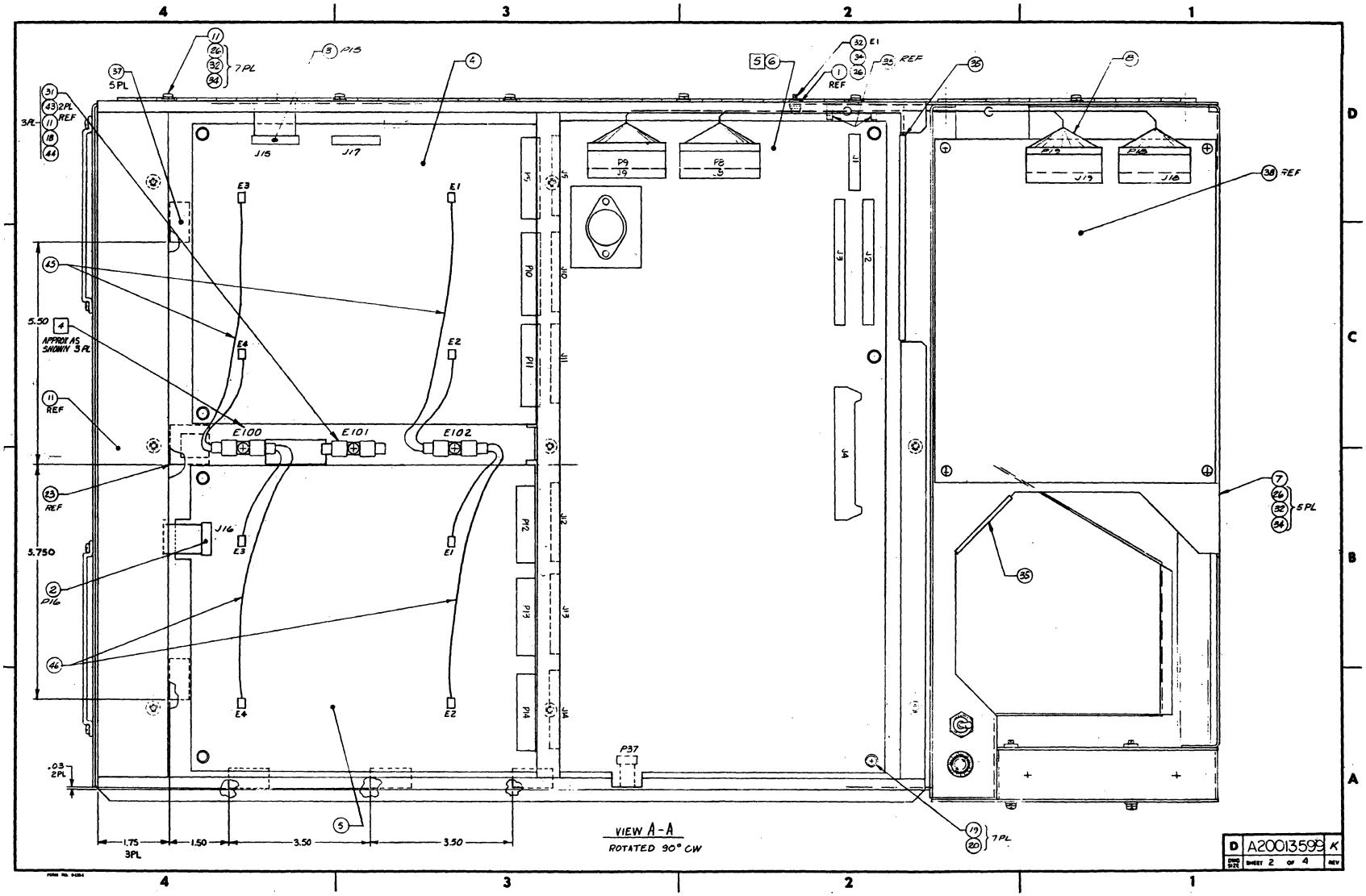
DRAFTSMAN — CHECKER — ENGINEER — APPD — DATE

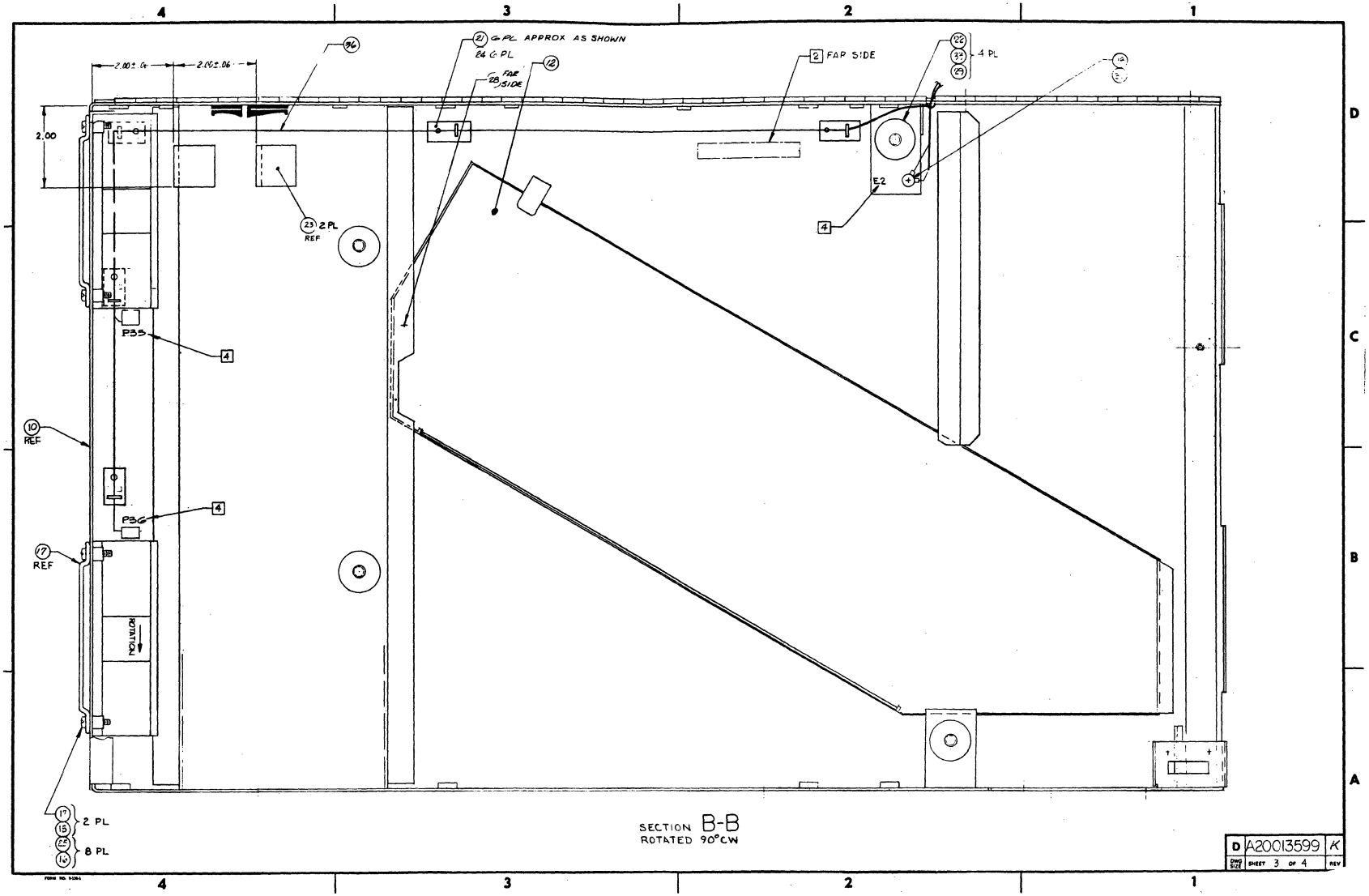
TITLE: FRAME ASSY REFLEX II

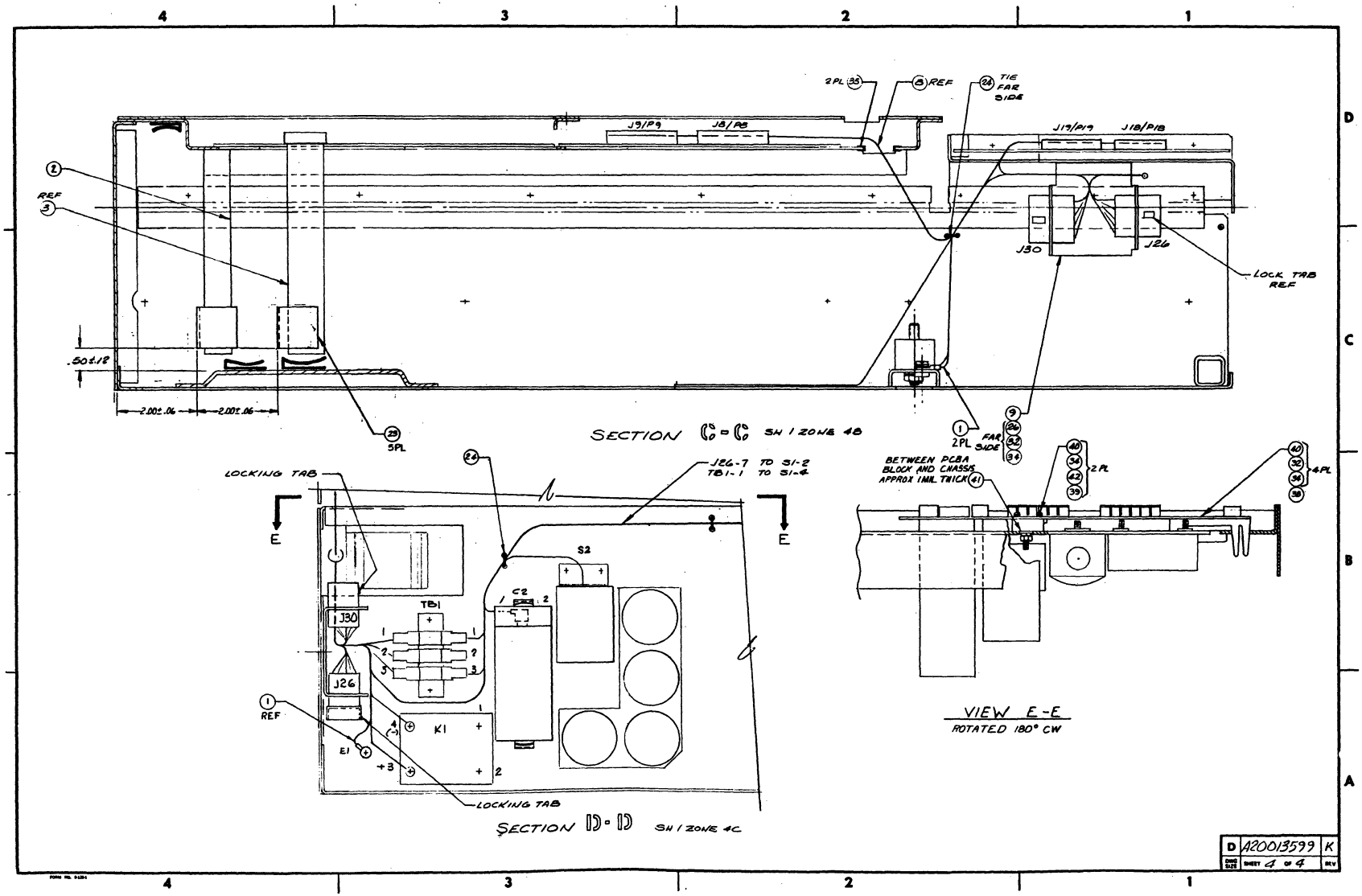
Microdata IRVINE, CALIFORNIA

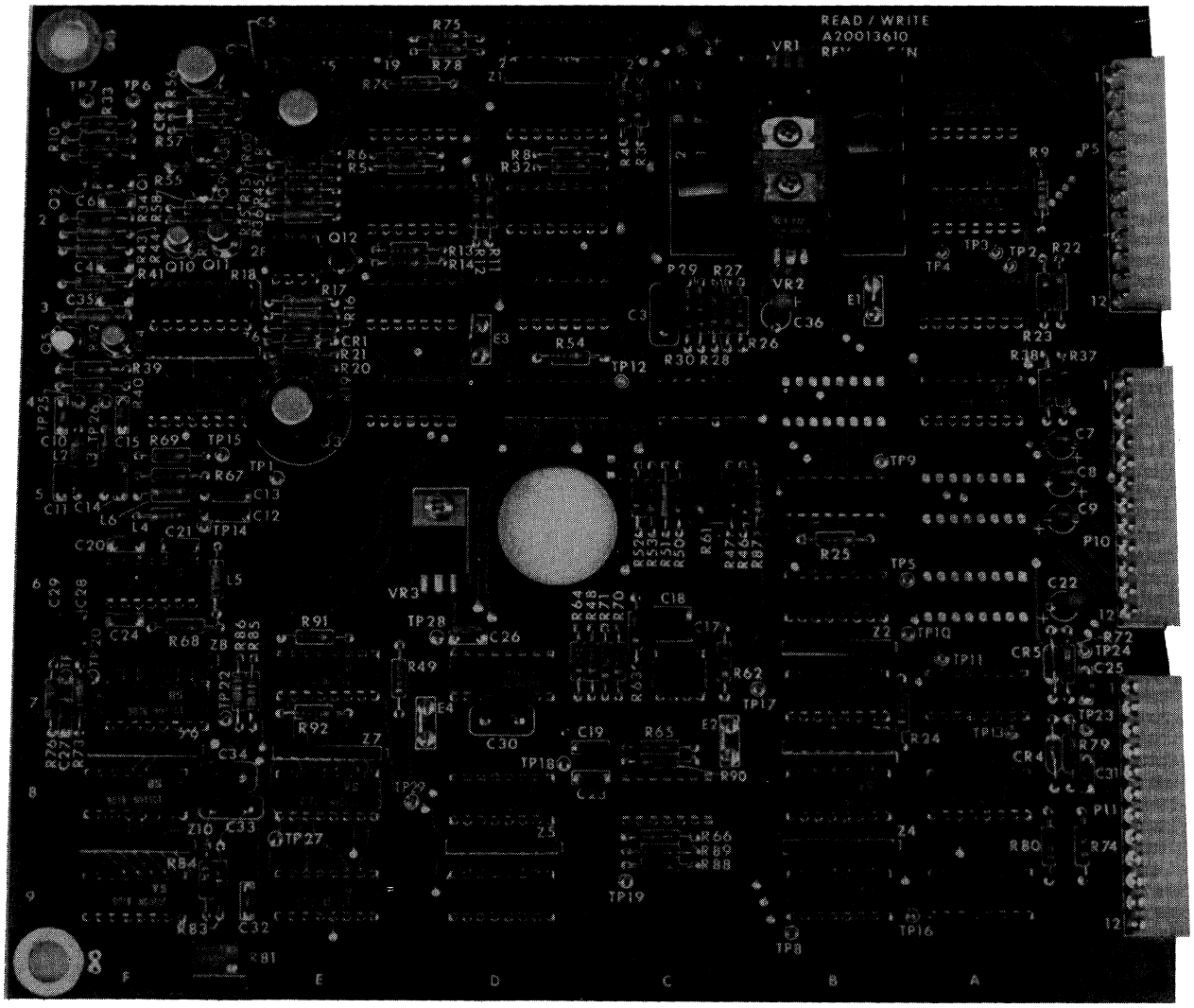
D A20013599 K

SCALE 1/1 IDENT CODE 52936 SHEET 1 OF 4

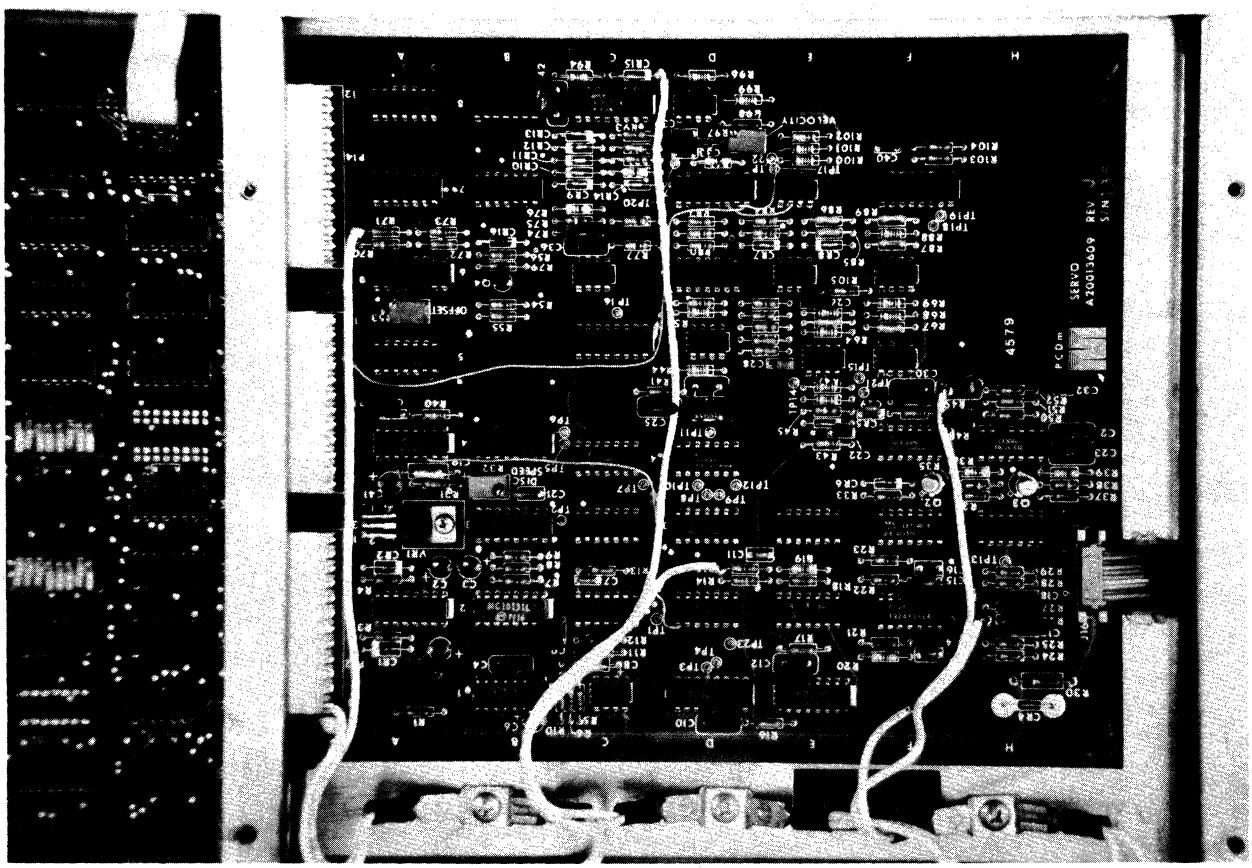

4
3
2
1
D
C
B
A
J15
J17
J18
J19
J16
P9
J9
P8
J8
E3
E1
E4
E2
E100
E101
E102
J16
P37
5.50
APPROX AS SHOWN 3 PL
5.750
.03
2PL
1.75
3PL
1.50
3.50
3.50
5PL
7PL
REF
VIEW A-A
ROTATED 90° CW
D
A20013599
K
SHEET 2 OF 4


4
3
2
1
D
C
B
A
2.00 ± .04
2.06 ± .06
2.00
(24) 6 PL APPROX AS SHOWN
24 G PL
(28) FAP SIDE
2 FAP SIDE
(22) (27) (29) 4 PL
(23) 2 PL REF
P35
P36
E2
4
(10) REF
(17) REF
ROTATION
(17) (15) (25) (14) 2 PL 8 PL
SECTION B-B
ROTATED 90°CW
D A20013599 K
DWG SIZE SHEET 3 OF 4 REV

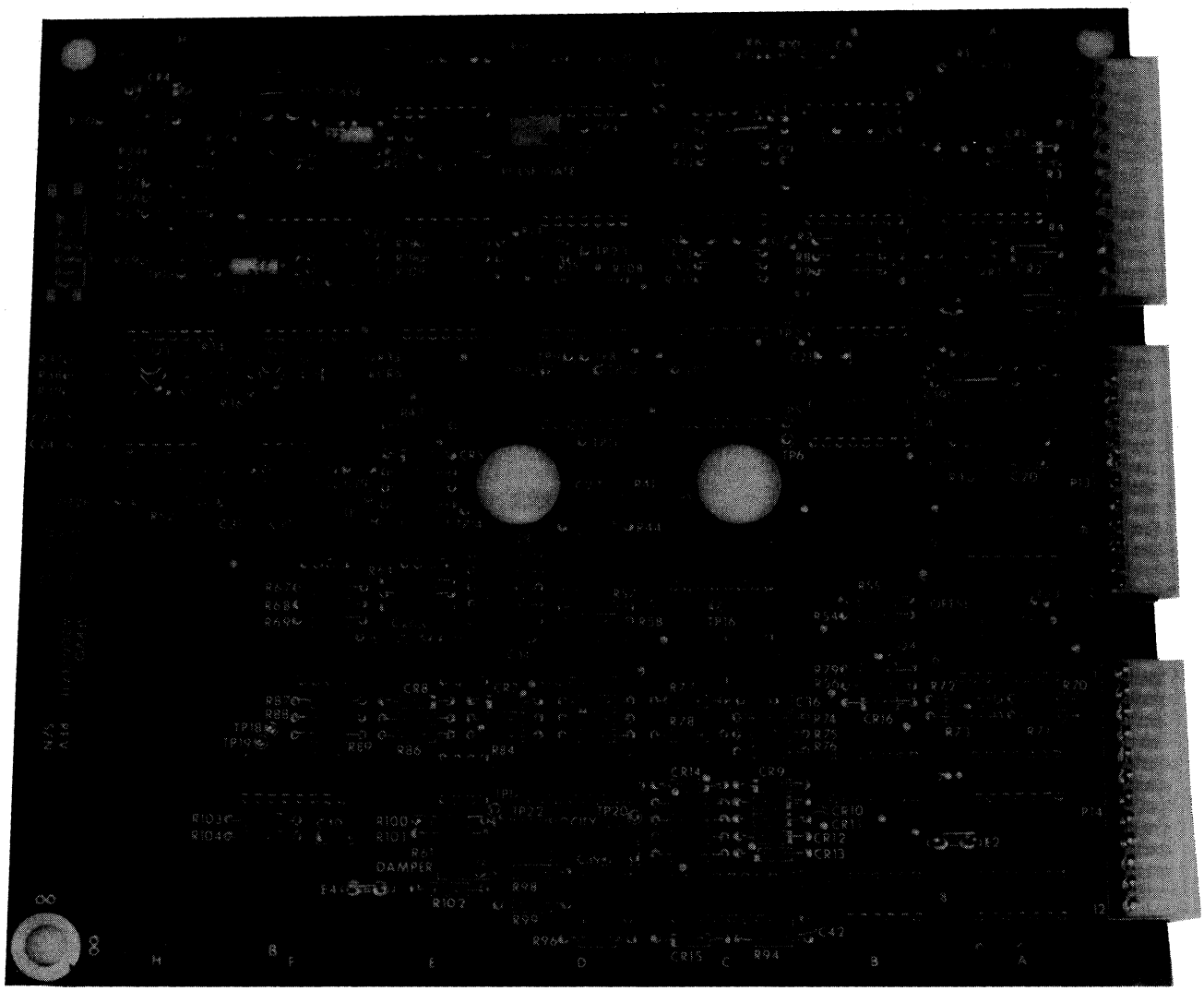

J9/P9
J8/P8
J19/P19
J18/P18
J30
J26
LOCK TAB REF
2PL 35
REF 28
24 TIE FAR SIDE
REF 2
REF 3
.50±.12
2.00±.06
2.00±.06
29 5PL
SECTION C-C SH 1 ZONE 4B
1 2PL FAR SIDE
9
94
92
94
LOCKING TAB
24
J26-7 TO S1-2
TB1-1 TO S1-4
E
E
S2
C2
TB1
J30
J26
K1
E1
+3
1 REF
LOCKING TAB
SECTION D-D SH 1 ZONE 4C
BETWEEN PCBA BLOCK AND CHASSIS APPROX 1MIL THICK 41
40
34
42
39
2PL
40
32
38
36
4PL
VIEW E-E
ROTATED 180° CW
D A20013599 K
SHEET 4 OF 4



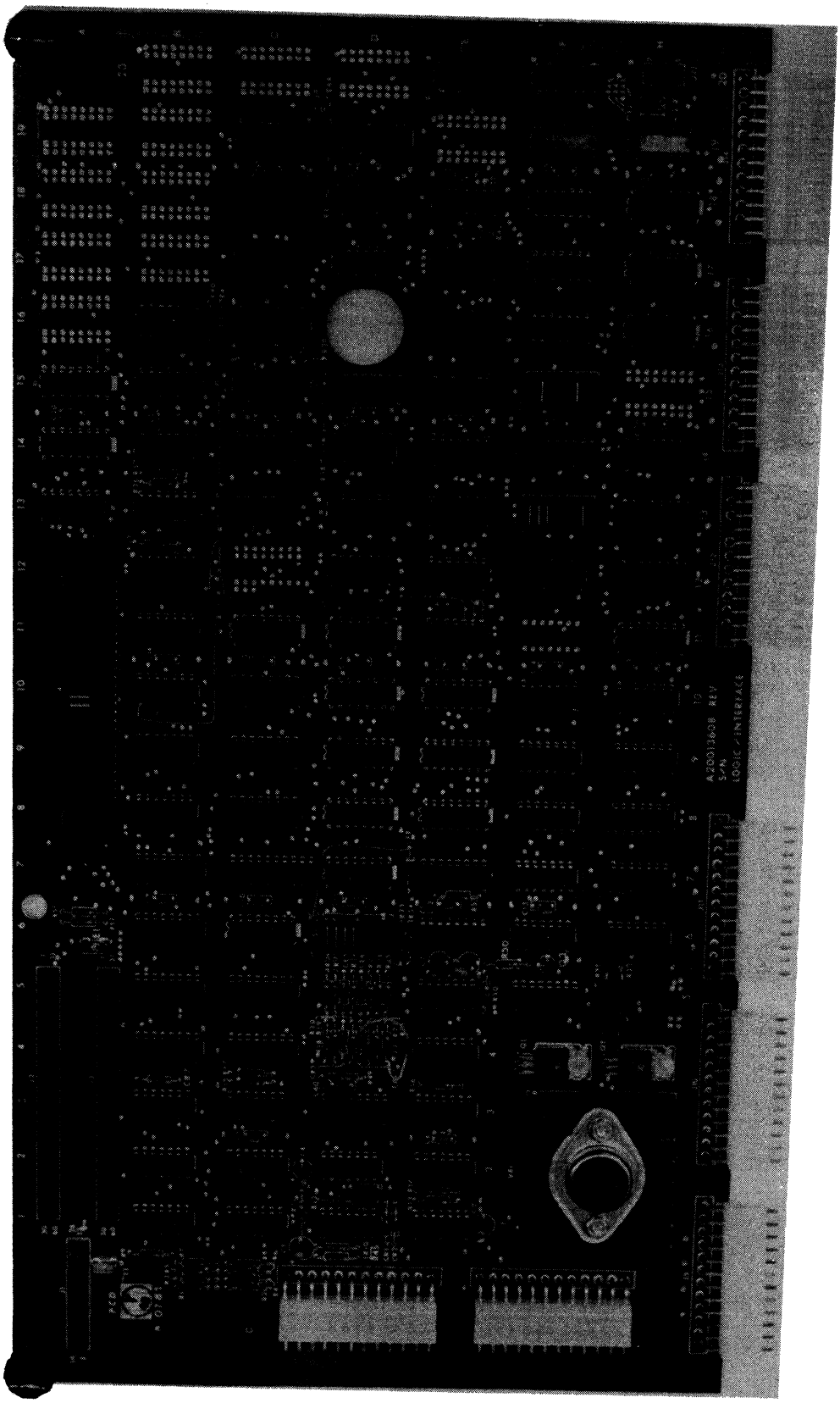
PCB, READ/WRITE
A20013610



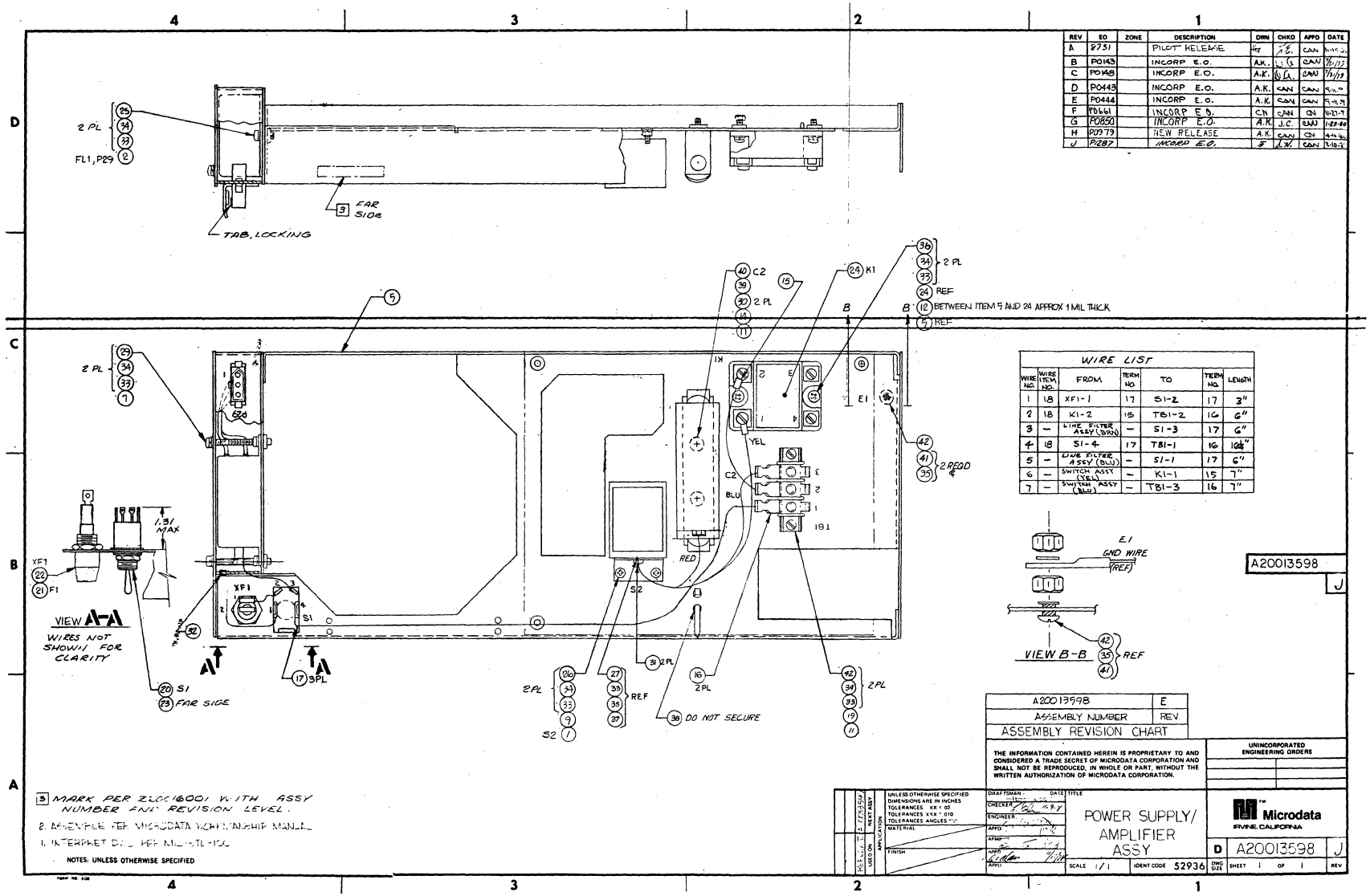
PCB, SERVO
A20013609



PCB, SERVO
A20013711



PCB,LOGIC/INTERFACE
A20013608



REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	8731		PILOT RELEASE	[illegible]	[illegible]	CAN	[illegible]
B	P0143		INCORP E.O.	AK.	[illegible]	CAN	[illegible]
C	P0148		INCORP E.O.	A.K.	[illegible]	CAN	[illegible]
D	P0443		INCORP E.O.	A.K.	CAN	CAN	[illegible]
E	P0444		INCORP E.O.	A.K.	CAN	CAN	[illegible]
F	P0661		INCORP E.O.	C.N.	CAN	CN	[illegible]
G	P0850		INCORP E.O.	A.K.	J.C.	CAN	[illegible]
H	P0979		NEW RELEASE	A.K.	CAN	CN	[illegible]
J	P1287		INCORP E.O.	[illegible]	A.K.	CAN	[illegible]

WIRE LIST

WIRE NO.	WIRE ITEM NO.	FROM	TERM NO.	TO	TERM NO.	LENGTH
1	18	XF1-1	17	S1-2	17	3"
2	18	K1-2	15	TB1-2	16	6"
3	–	LINE FILTER ASSY (BRN)	–	S1-3	17	6"
4	18	S1-4	17	TB1-1	16	10½"
5	–	LINE FILTER ASSY (BLU)	–	S1-1	17	6"
6	–	SWITCH ASSY (YEL)	–	K1-1	15	7"
7	–	SWITCH ASSY (BLU)	–	TB1-3	16	7"

A20013598 J

A20013598	E
ASSEMBLY NUMBER	REV.
ASSEMBLY REVISION CHART	

UNINCORPORATED ENGINEERING ORDERS

3 MARK PER Z1001600I WITH ASSY NUMBER AND REVISION LEVEL.

2. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL

1. INTERPRET DWG PER MIL-STD-100

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES XX ± .02 TOLERANCES XXX ± .010 TOLERANCES ANGLES ±1°

MATERIAL

FINISH

DRAFTSMAN

CHECKER

ENGINEER

APPD

APPD

APPD

TITLE: POWER SUPPLY/ AMPLIFIER ASSY

SCALE 1/1 IDENT CODE 52936 DWG SIZE D SHEET 1 OF 1

Microdata IRVINE, CALIFORNIA

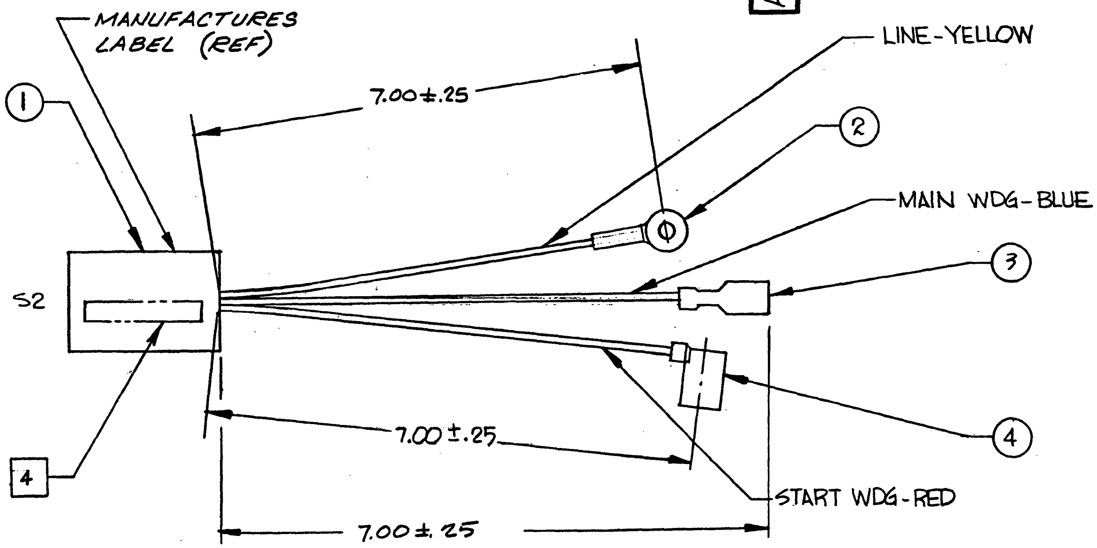
D A20013598 J

WIRE LIST

WIRE NO.	ITEM	TERM	FROM	TO (TAG)	TERM
1	1	—	LINE	K1-1	2
2	1	—	MAIN	TB1-3	3
3	1	—	START	C2-1	4

A20013588 C

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	8731		PILOT RELEASE	HG 5/15/78	CAN	CAN	11-15-8
B	P0287		INCORP E.O.	AK	J.J.C.	CAN	7-12-79
C	P0978		NEW RELEASE	AK	CAN	CN	8-18-80



A20013588	A
ASSEMBLY NO.	REV.

ASSEMBLY REV CHART

4 MARK PER Z20016001 WITH ASSY NO. & REV LTR.

THE INFORMATION CONTAINED HEREIN IS PROPRIETARY TO AND CONSIDERED A TRADE SECRET OF MICRODATA CORPORATION AND SHALL NOT BE REPRODUCED, IN WHOLE OR PART, WITHOUT THE WRITTEN AUTHORIZATION OF MICRODATA CORPORATION.

3. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL.
2. BAG AND TAG PER MARKING SPEC. Z20016001 WITH ASSY NO. AND REV. LTR. (TAG INDIVIDUALLY)
1. INTERPRET DRAWING PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON
A20013598	REFLEX II

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES .XX ± .02
TOLERANCES .XXX ± .010
TOLERANCES ANGLES ± ½°

MATERIAL

FINISH

DRAFTSMAN H. Goodies DATE 5/15/78
CHECKER E. Fulanos 10-9-78
ENGINEER
APPD G. W. Conklin 11/13/78
APPD
APPD [signature] 11/15/78
APPD

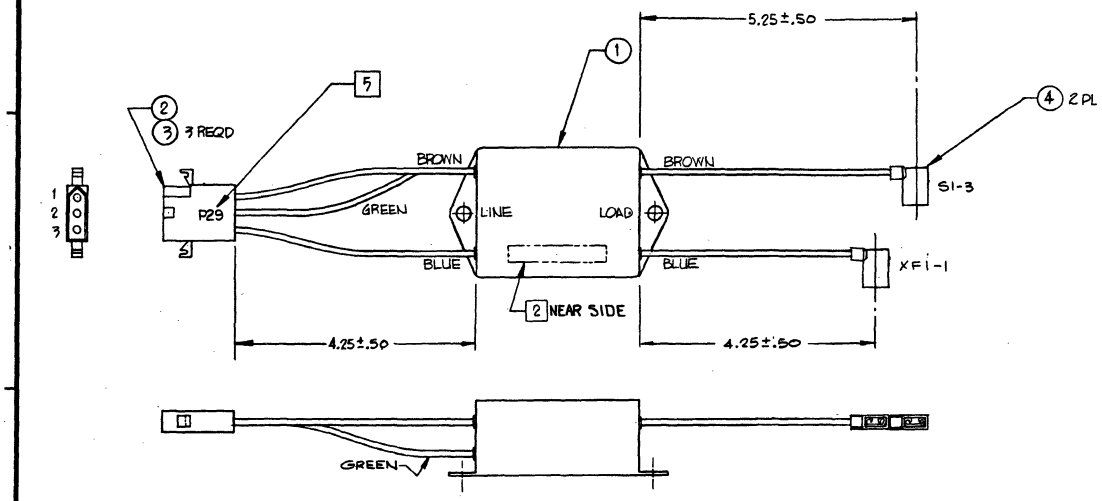
TITLE
MOTOR SWITCH ASSY-SOLID STATE

Microdata
IRVINE, CALIFORNIA

DWG SIZE			REV
B	A20013588		C
SCALE NONE	CODE IDENT 52936	SHEET 1 OF 1	REV

FORM NO. 9-137

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	8731		PILOT RELEASE	[illegible]	CAN	CAN	11-15-78
B	P0288		INCORP E.O.	OK	J.C.	CAN	7/24/79
C	P0978		NEW RELEASE	AK	CAN	CAN	9-14-80



A20013594 C

A20013594	A
ASSEMBLY NO.	REV. LTR.
ASSEMBLY REV CHART	

5. REFERENCE DESIGNATION MARKING PER Z20016001.
4.
3. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL.
2. MARK PER Z20016001 WITH ASSEMBLY NUMBER AND REVISION LETTER
1. INTERPRET DRAWING PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

UNINCORPORATED ENGINEERING ORDERS

HEPLEX II | 20013593 | NEXT ASSY | USED ON | APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES .XX ± .02
TOLERANCES .XXX ± .010
TOLERANCES ANGLES ±½°
MATERIAL
FINISH

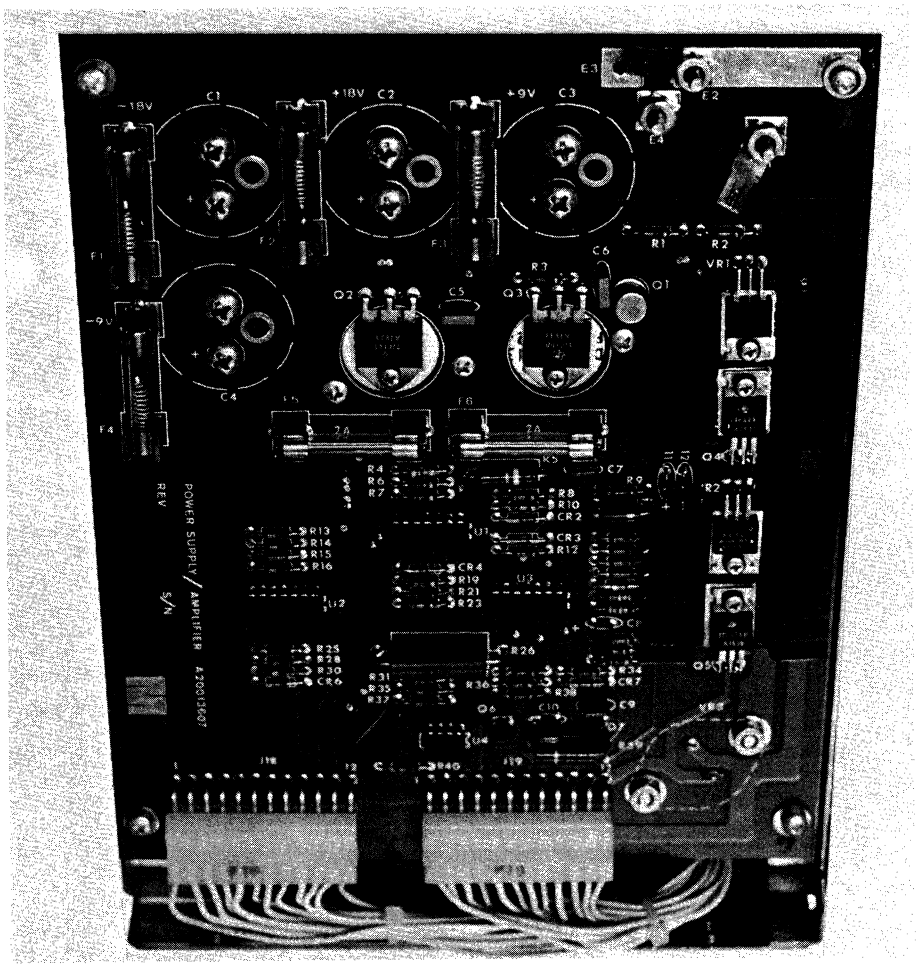
DRAFTSMAN [illegible] DATE 5/15/78
CHECKER [illegible] 10-9-78
ENGINEER [illegible] 11/13/78
APPD [illegible] 11/15/78
APPD [illegible] 11/15/78
APPD [illegible] 11/15/78

TITLE: LINE FILTER, ASSY

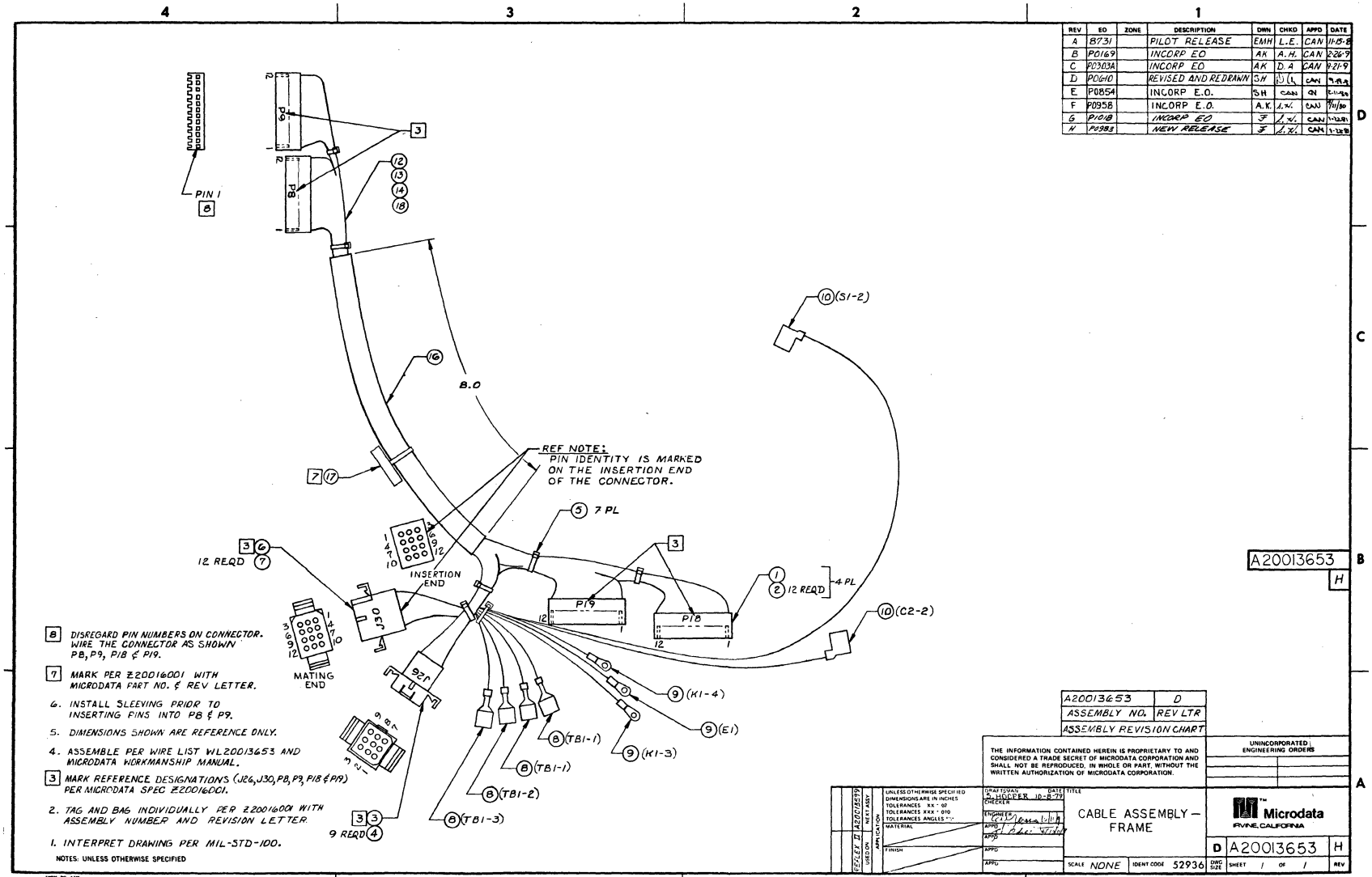
Microdata IRVINE, CALIFORNIA

SCALE NONE | IDENT CODE 52936 | DWG SIZE C | A20013594 | C | SHEET 1 OF 1 | REV

7-31-78



PCB, POWER SUPPLY/AMPLIFIER
A20013607



REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	B731		PILOT RELEASE	EMH	L.E.	CAN	11-15-8
B	P0169		INCORP EO	AK	A.H.	CAN	2-26-9
C	P0303A		INCORP EO	AK	D.A	CAN	9-21-9
D	P0610		REVISED AND REDRAWN	SH		CAN	9-9-9
E	P0854		INCORP E.O.	SH	CAN	QN	6-11-80
F	P0958		INCORP E.O.	A.K.		CAN	7/11/80
G	P1018		INCORP EO	F		CAN	1-12-81
H	P0983		NEW RELEASE	F		CAN	1-12-81

A20013653	D
ASSEMBLY NO.	REV LTR
ASSEMBLY REVISION CHART	

UNINCORPORATED ENGINEERING ORDERS

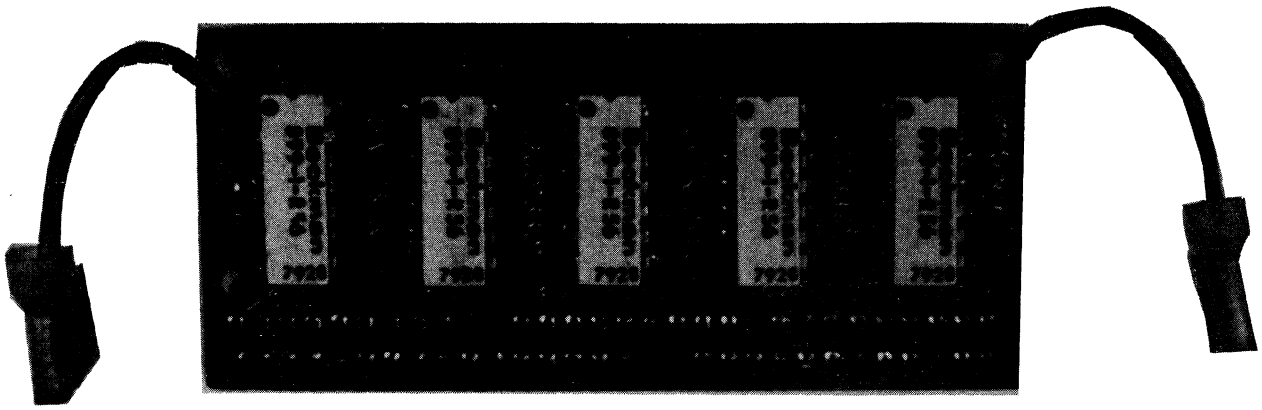
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES XX ± .02
TOLERANCES XXX ± .010
TOLERANCES ANGLES ±°
MATERIAL
FINISH

DRAFTSMAN S. HOOPER 10-8-79
CHECKER
ENGINEER
APPD
APPD
APPD

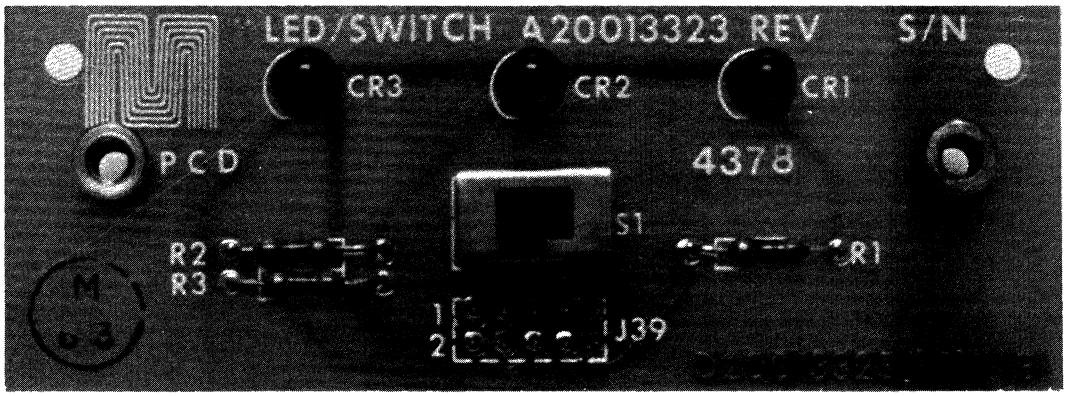
TITLE: CABLE ASSEMBLY — FRAME

Microdata
IRVINE, CALIFORNIA

SCALE NONE | IDENT CODE 52936 | DWG SIZE D | A20013653 | H
SHEET 1 OF 1 | REV

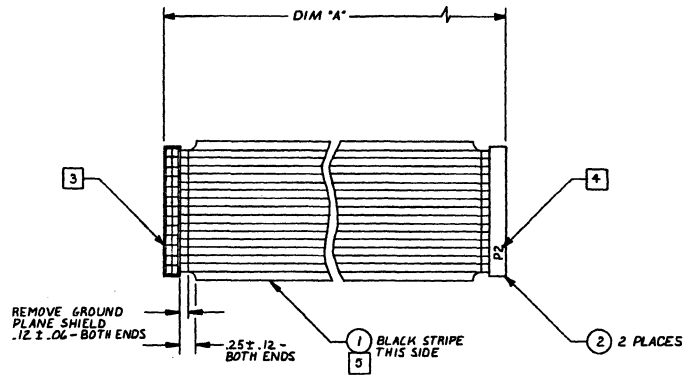


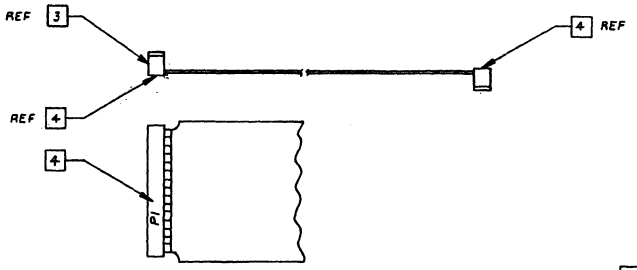
PCB, TERMINATOR
A20013301-001



PCB, LED/SWITCH
(OPERATOR INDICATOR PANEL)
A20013323

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	8816		PILOT RELEASE	MS	JRD	J.R.	1-5-79
B	9227A		INCORP E.O.	APM	mP	RJS	8/13/79
C	9258		INCORP E.O.	GM	JRD	RJS	9/1/79
D	9286		NEW RELEASE	GM	JRD	RJS	9/10/79
E	9637		INCORP E.O.	DEC	JRD	[illegible]	7-2-80





A20000979 E

ASSY NO.	REV LTR	DIM "A" (LENGTH)
A20000979-005	A	240 IN. ± 4.00
A20000979-004	A	80 IN. ± 2.00
A20000979-003	A	120 IN. ± 2.00
A20000979-002	A	60 IN. ± 2.00
A20000979-001	A	24 IN. ± 1.00

ASSY TABULATION CHART

5 BLACK OR COLORED STRIP INDICATES DRAIN WIRE.

4. MARK REF DESIGNATOR PER Z20016001 APPROXIMATELY WHERE SHOWN.

3 MARK PER Z20016001 WITH ASSY. NO., DASH NO., AND REV. LTR. APPROXIMATELY WHERE SHOWN.

2. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL.

1. INTERPRET DRAWING PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

TABULATED

UNINCORPORATED ENGINEERING ORDERS

NEXT ASSY | USED ON | APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES .XX ± .02
TOLERANCES .XXX ± .010
TOLERANCES ANGLES ±½°
MATERIAL
FINISH

DRAFTSMAN [illegible] DATE 12-31-78
CHECKER [illegible] 12/20/78
ENGINEER [illegible] 1/2/79
APPD [illegible] 1/2/79
APPD E. Ryan 1-4-79
APPD [illegible] 1-4-79
APPD

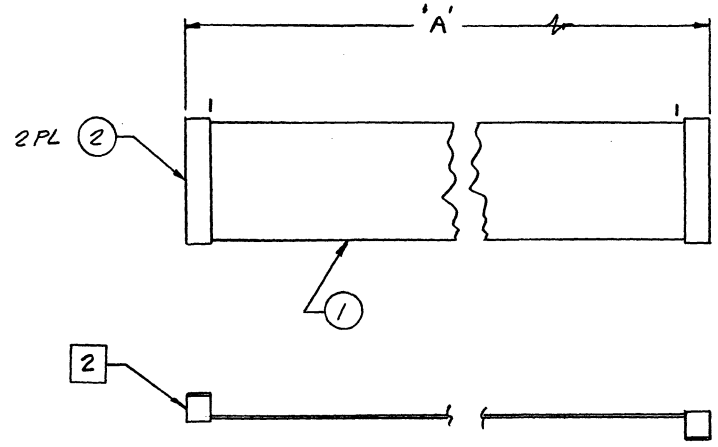
TITLE
CABLE ASSY
26 CONDUCTOR

Microdata
IRVINE, CALIFORNIA

SCALE | IDENT CODE 52936 | DWG SIZE C | A20000979 E | SHEET 1 OF 1 | REV

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A			PILOT RELEASE	RE.	CAN	RTL	9/18/78
B	8699		INCORP EO.	JGL	mp	RTL	7/11/79
C	P1001		NEW RELEASE	GM	[illegible]	RTL	1/23/81

A20013339 C



-001	100 ± 1.00		
—	60.00 ± 1.00		
DASH NO.	'A' DIM		
TABULATION BLOCK			

A20013339-001	A
A20013339	A
ASSY NO.	REV. LTR.
ASSEMBLY REV CHART	

2. MARK PER SPEC Z20016001 WITH PART NO. AND REV LTR

1. INTERPRET DWG PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY | USED ON | APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES .XX ±.02
TOLERANCES .XXX ±.010
TOLERANCES ANGLES ± ½°

MATERIAL SEE L/M

FINISH

DRAFTSMAN [illegible] DATE 8-31-78
CHECKER [illegible] 8-5-78
ENGINEER Don Dellenbaugh 8/31/78
APPD [illegible]
APPD [illegible] 9-14-78
APPD W. Spicer II 9-14-78
APPD

TITLE: CABLE ASSY - 60 COND

SCALE NONE | CODE IDENT 52936

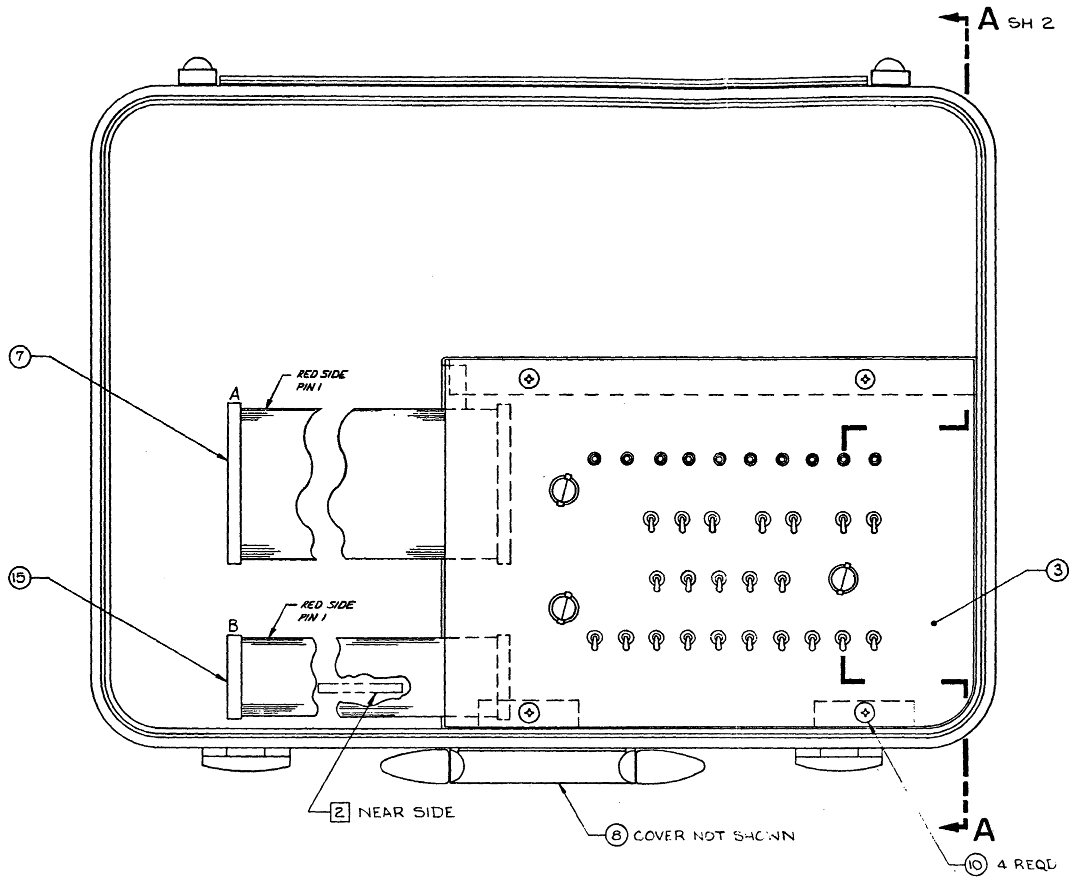
Microdata IRVINE, CALIFORNIA

DWG SIZE	SHEET	REV
B	A20013339	C

SHEET 1 OF 1

FORM NO. 9-137

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	[illegible]		PILOT RELEASE	[illegible]	J.J.C.	CAN	[illegible]
B	P04[illegible]		INCORP E.O.	A.R	J.C	CAN	[illegible]
C	P0043		INCORP E.C.	[illegible]	CAN	CN	[illegible]
D	P1257		INCORP EO	[illegible]	[illegible]	CAN	1-25-[illegible]



A20013340	B
ASSEMBLY NO.	REVISION LTR
ASSEMBLY REVISION CHART	

3. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL.
2. [2] MARK PER Z20016001 WITH PART NUMBER AND REVISION LEVEL.
1. INTERPRET DRAWING PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

UNINCORPORATED ENGINEERING ORDERS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES .XX ± .02
TOLERANCES .XXX ± .010
TOLERANCES ANGLES ±

MATERIAL: SEE L/M

FINISH

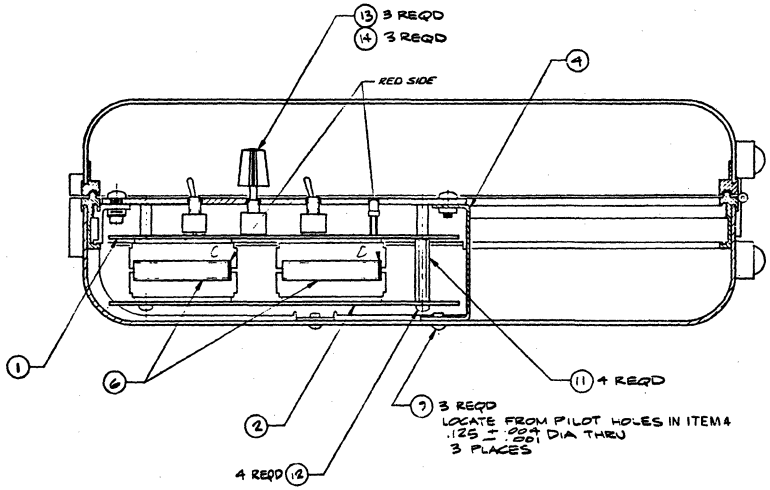
DRAFTSMAN: [illegible] WARD
CHECKER: [illegible] CHRISTIAN 12-2-78
ENGINEER: [illegible] JOHNSON 12-18-78
APPD: [illegible] BEISNER 12-18-78
APPD: [illegible] PETERSON 12-19-78
APPD: [illegible] WYATT [illegible]

TITLE: EXERCISER ASSY-MOD III

Microdata IRVINE, CALIFORNIA

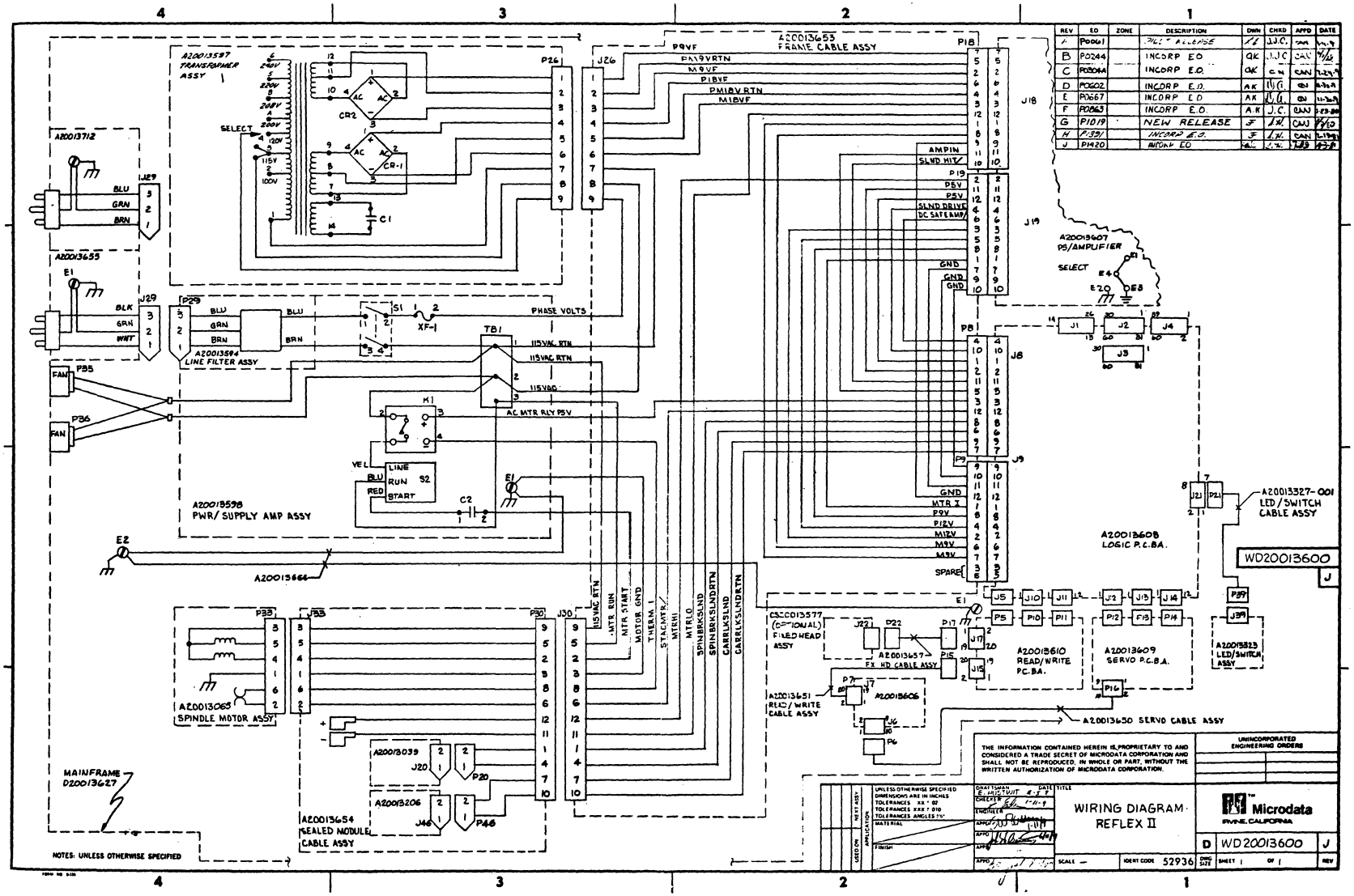
DWG SIZE D | A20013340 | REV D

SCALE 1/1 | IDENT CODE 52936 | SHEET 1 OF 2

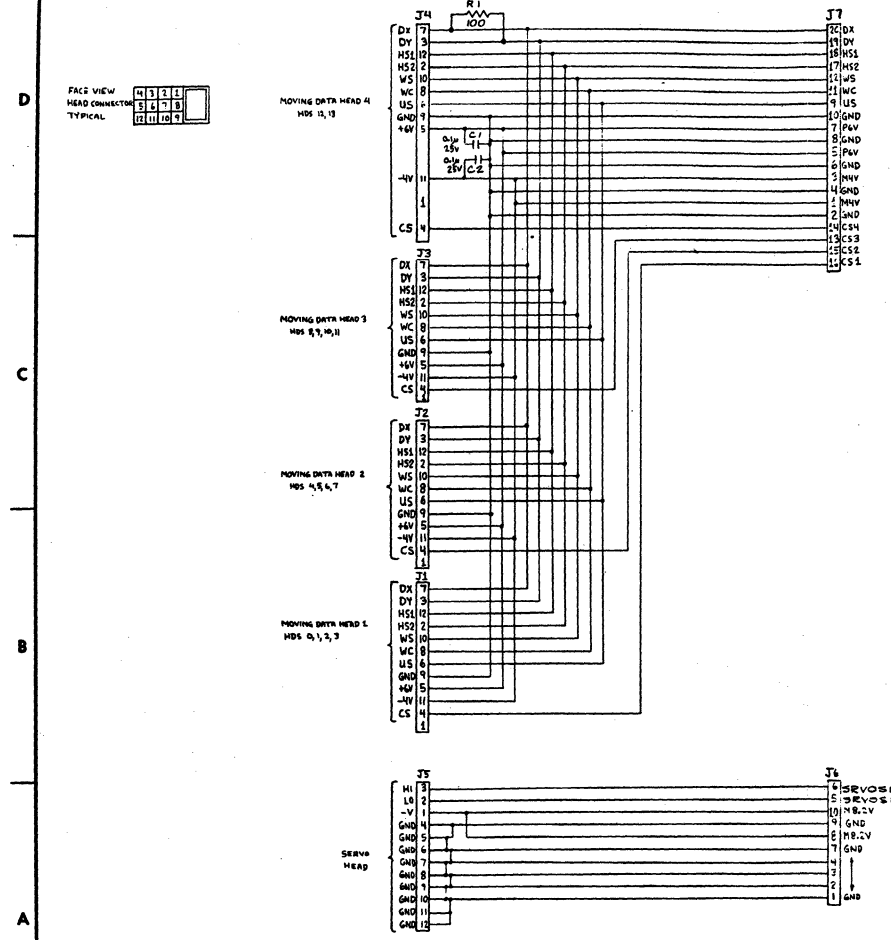


SECTION **A-A**
ROTATED 90° CW

D	A100133A0	D
SIZE	SHEET 2 OF 2	REV



REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	P0061		INITIAL RELEASE	JS	J.J.C.	CAN	11-19
B	P0244		INCORP EO	QK	J.J.C	CAN	4/12
C	P0264A		INCORP E.O.	QK	C.M	CAN	1-24-7
D	P0502		INCORP E.O.	AK	J.C.	CAN	8-30-8
E	P0667		INCORP E.O	AK	J.C.	CAN	11-26-8
F	P0863		INCORP E.O.	AK	J.C.	CAN	2-23-89
G	P1019		NEW RELEASE	JF	J.H.	CAN	7/10
H	P-391		INCORP E.O.	JF	J.H.	CAN	1-19-90
J	P1420		INCORP EO	JF	J.H.	CAN	12-3-9



INTERPRET PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
AX	7952		PROTO REL.	MG	AS	[illegible]	7/11
A	A578		PILOT RELEASE	BH	MP	[illegible]	10/1[illegible]
B	P04838		INCORP E.O.	LR	[illegible]	UNI	7/[illegible]
C	P0778		NEW RELEASE	MC	[illegible]	CWN	9/[illegible]

SC20013606 C

THE INFORMATION CONTAINED HEREIN IS PROPRIETARY TO AND CONSIDERED A TRADE SECRET OF MICRODATA CORPORATION AND SHALL NOT BE REPRODUCED, IN WHOLE OR PART, WITHOUT THE WRITTEN AUTHORIZATION OF MICRODATA CORPORATION.

UNINCORPORATED ENGINEERING ORDERS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES XX ± 02
TOLERANCES XXX ± 010
TOLERANCES ANGLES ±1°
MATERIAL
FINISH

NEXT ASSY
USED ON
APPLICATION

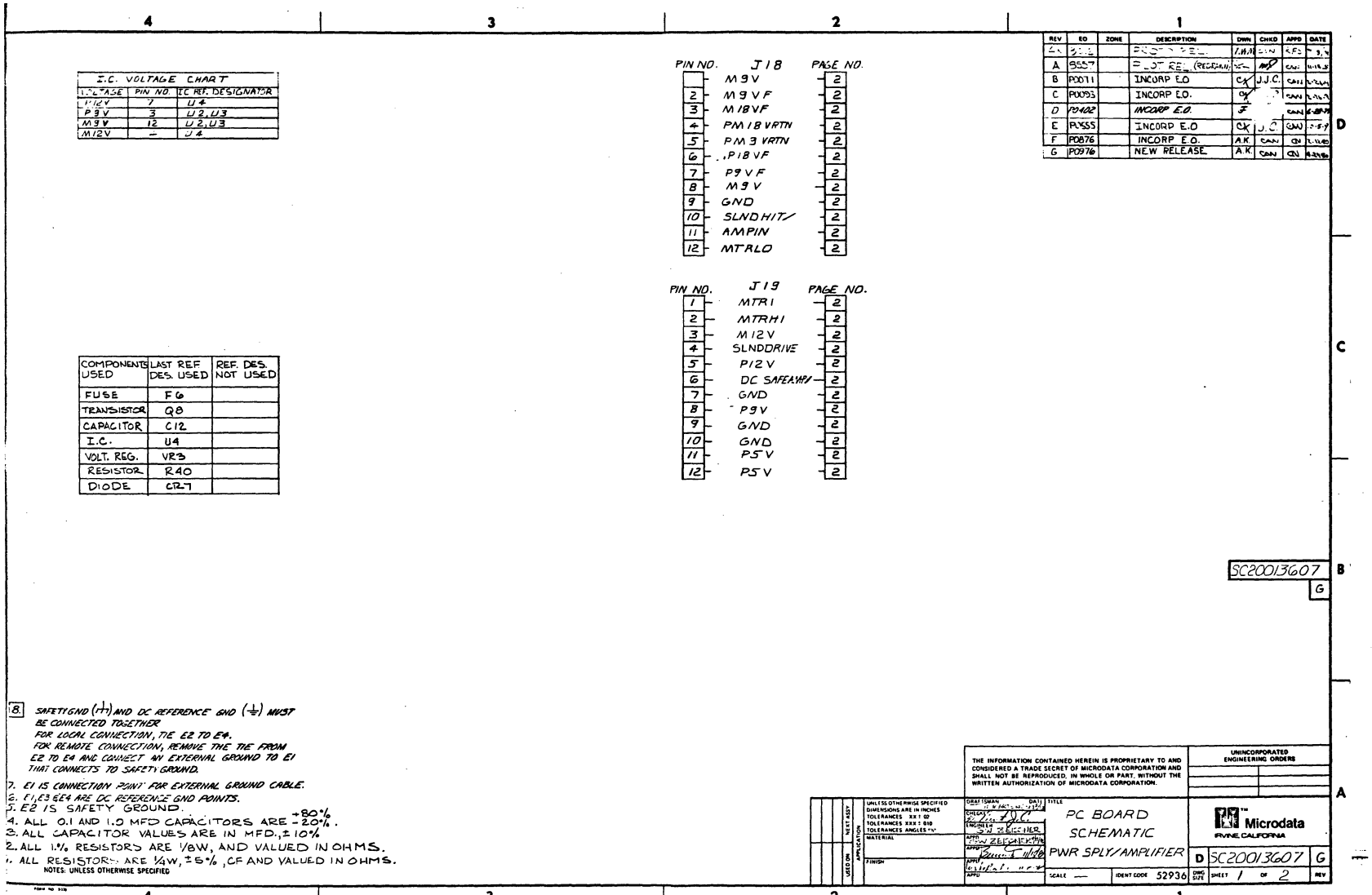
DRAFTSMAN [illegible] DATE 3-30-78
CHECKER [illegible] DATE 3-30-78
ENGINEER [illegible]
APPD [illegible]
APPD [illegible]
APPD [illegible]

TITLE SCHEMATIC — P.C.B. - HEAD CONNECTORS

Microdata
IRVINE, CALIFORNIA

D SC20013606 C

SCALE — IDENT CODE 52936 DWG SIZE SHEET OF REV



I.C. VOLTAGE CHART		
VOLTAGE	PIN NO.	IC REF. DESIGNATOR
P12V	7	U4
P9V	3	U2,U3
M9V	12	U2,U3
M12V	—	U4

COMPONENTS USED	LAST REF DES. USED	REF. DES. NOT USED
FUSE	F6	
TRANSISTOR	Q8	
CAPACITOR	C12	
I.C.	U4	
VOLT. REG.	VR3	
RESISTOR	R40	
DIODE	CR7	

PIN NO.	J18	PAGE NO.
	M9V	2
2	M9VF	2
3	M18VF	2
4	PM18VRTN	2
5	PM3VRTN	2
6	P18VF	2
7	P9VF	2
8	M9V	2
9	GND	2
10	SLNDHIT/	2
11	AMPIN	2
12	MTRLO	2

PIN NO.	J19	PAGE NO.
1	MTRI	2
2	MTRHI	2
3	M12V	2
4	SLNDDRIVE	2
5	P12V	2
6	DC SAFEAMP/	2
7	GND	2
8	P9V	2
9	GND	2
10	GND	2
11	P5V	2
12	P5V	2

REV	ECO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
A	9557		[illegible] (REDRAWN)	[illegible]	[illegible]	[illegible]	[illegible]
B	P0071		INCORP E.O	CK	J.J.C.	[illegible]	[illegible]
C	P0093		INCORP E.O.	CK	[illegible]	[illegible]	[illegible]
D	19402		INCORP E.O.	[illegible]		[illegible]	[illegible]
E	P0555		INCORP E.O	CK	J.C.	GW	[illegible]
F	P0876		INCORP E.O.	A.K	CAN	GW	[illegible]
G	P0976		NEW RELEASE.	A.K	CAN	GW	[illegible]

SC20013607 G

8. SAFETY GND (⏚) AND DC REFERENCE GND (⏚) MUST BE CONNECTED TOGETHER FOR LOCAL CONNECTION, TIE E2 TO E4. FOR REMOTE CONNECTION, REMOVE THE TIE FROM E2 TO E4 AND CONNECT AN EXTERNAL GROUND TO E1 THAT CONNECTS TO SAFETY GROUND.
7. E1 IS CONNECTION POINT FOR EXTERNAL GROUND CABLE.
6. E1,E3 &E4 ARE DC REFERENCE GND POINTS.
5. E2 IS SAFETY GROUND.
4. ALL 0.1 AND 1.0 MFD CAPACITORS ARE +80% -20%.
3. ALL CAPACITOR VALUES ARE IN MFD., ± 10%
2. ALL 1% RESISTORS ARE 1/8W, AND VALUED IN OHMS.
1. ALL RESISTORS ARE 1/4W, ±5%, CF AND VALUED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

UNINCORPORATED ENGINEERING ORDERS

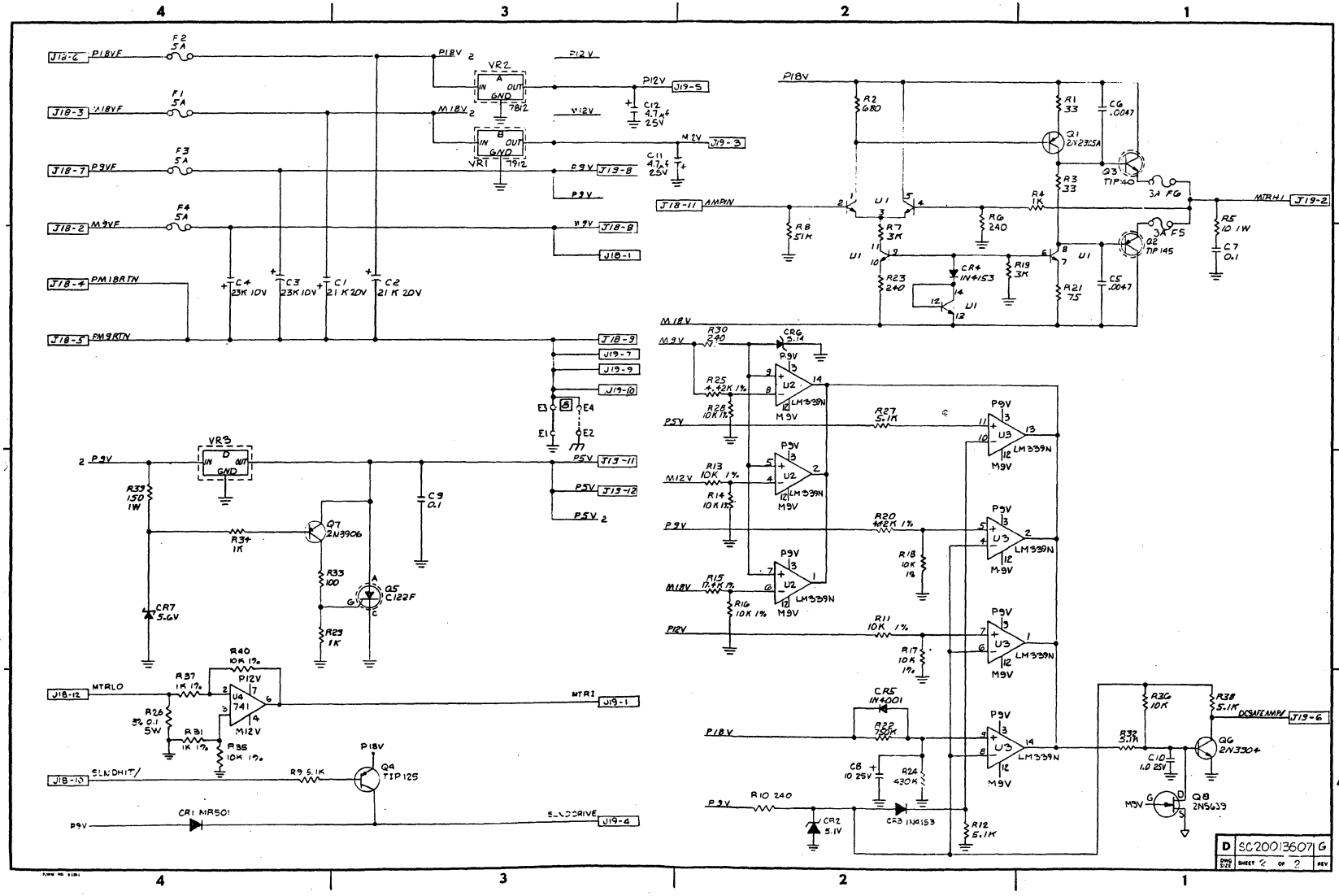
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES XX ± 02
TOLERANCES XXX ± 010
TOLERANCES ANGLES ±½°
MATERIAL
FINISH
NEXT ASSY
USED ON
APPLICATION

DRAFTSMAN [illegible] DATE [illegible]
CHECK J.J.C.
ENGINEER J.W. ZEISSLER
APPD [illegible]
APPD [illegible]
APPD [illegible]

TITLE
PC BOARD SCHEMATIC
PWR SPLY/AMPLIFIER

Microdata
IRVINE, CALIFORNIA

SCALE — IDENT CODE 52936 DWG SIZE D SC20013607 G
SHEET 1 OF 2 REV


J18-6 P18VF
J18-3 M18VF
J18-7 P9VF
J18-2 M9VF
J18-4 PM18RTN
J18-5 PM9RTN
F2 5A
F1 5A
F3 5A
F4 5A
P18V
M18V
P12V
M12V
P9V
M9V
P5V
VR2
VR1
VR3
7812
7912
C12 4.7uF 25V
C11 4.7uF 25V
C4 23K 10V
C3 23K 10V
C1 21K 20V
C2 21K 20V
C9 0.1
J19-5
J19-3
J18-8
J18-1
J18-9
J19-7
J19-9
J19-10
J19-11
J19-12
E1
E2
E3
E4
R2 680
R1 33
C6 .0047
Q1 2N2905A
Q3 TIP40
3A FG
R3 33
J18-11 AMPIN
R4 1K
R8 51K
R7 3M
R6 240
U1
R5 10 1W
C7 0.1
MTRH1 J19-2
3A FS
Q2 TIP 145
R23 240
CR4 IN4153
R19 3K
R21 7.5
C5 .0047
R30 240
CR6 5.1V
R25 402K 1%
R28 10K 1%
U2 LM339N
R27 5.1K
U3 LM339N
R13 10K 1%
R14 10K 1%
R20 402K 1%
R18 10K 1%
R15 17.4K 1%
R16 10K 1%
R11 10K 1%
R17 10K 1%
R33 150 1W
R34 1K
Q7 2N3906
R32 100
Q5 C122F
R29 1K
CR7 5.6V
R40 10K 1%
R37 1K 1%
R26 3% 0.1 5W
R31 1K 1%
R35 10K 1%
U4 741
MTRLO
MTRI J19-1
SLNDHIT/ J18-10
R9 5.1K
Q4 TIP125
CR1 MR501
SLNDRIVE J19-4
CR5 IN4001
R22 750K
C8 10 25V
R24 430K
R10 240
CR2 5.1V
CR3 IN4153
R12 5.1K
R36 10K
R38 5.1K
DCSAFEAMPV J19-6
C10 1.0 25V
Q6 2N3904
Q8 2N5639
D SC20013607 G
SHEET 2 OF 2
REV

COMPONENTS USED	LAST REF DES USED	REF DES NOT USED
RESISTORS	R53	
RES MODULE	Z2	
CAPACITORS	C40	
DIODES	CR8	
TRANSISTORS	Q3	
TEST POINTS	TP1	
E POINTS	E2	
SWITCHES	S3	

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
AX	P0283		PROTO. RELEASE	LMD	MD	AK	5/8/78
A	B760		PILOT REL.	[illegible]	MD	CAN	[illegible]
B	P0111		INCORP E.O.	[illegible]	J.J.C.	CAN	8-3-79
C	P0179		INCORP E.O.	[illegible]	J.J.C.	CAN	8-3-79
D	P0319		INCORP E.O.	[illegible]	M.J.	CAN	6-11-79
E	P0459		INCORP E.O.	MLM	[illegible]	CAN	12-7
F	P0505		INCORP E.O	MLM	[illegible]	CAN	[illegible]
G	P0553		INCORP E.O.	MLM	[illegible]	[illegible]	[illegible]
H	P0587		INCORP E.O.	MLM	[illegible]	[illegible]	[illegible]
J	P0606		INCORPORATE E.O.	MLM	[illegible]	CAN	2/27/7
K	P0641		INCORP E.O.	AK	J.C.	CAN	12/1/79
L	P0769A		INCORP E.O.	AK	J.C.	CAN	12/20/79
M	P0635		INCORP E.O.	AK	J.C.	CAN	1-21-80
N	P0919		INCORP E.O.	[illegible]	J.C.	CAN	1-21-80
P	P0869		INCORP E.O.	A.K.	[illegible]	CAN	3/5/80
R	P0982		NEW RELEASE	MC	[illegible]	CAN	5/6/80

4 FOR REVISION N OR EARLIER DETAIL BOARDS; REFER TO EO. P0869 "WAS" CONDITION FOR I.C. LOCATIONS.

3. INTERPRET DWG. PER MIL-STD-100.

2 ALL CAPACITORS ARE .01 uF, 25V.

1. ALL RESISTORS ARE 1/4 W, ± 5% VALUES IN OHMS

NOTES: UNLESS OTHERWISE SPECIFIED

R

UNINCORPORATED ENGINEERING ORDERS.

P1166	P1392
P1037	10361
P1144	

SC20013608

DRAFTSMAN	LMD	4-78
CHECKER	[illegible]	5-15-78
ENGINEER	[illegible]	[illegible]
APPD	[illegible]	[illegible]
APPD	[illegible]	[illegible]
APPD	[illegible]	[illegible]

TITLE PC BOARD SCHEMATIC LOGIC WITH INTERFACE

SCALE

IDENT CODE 52936

Microdata IRVINE, CALIFORNIA

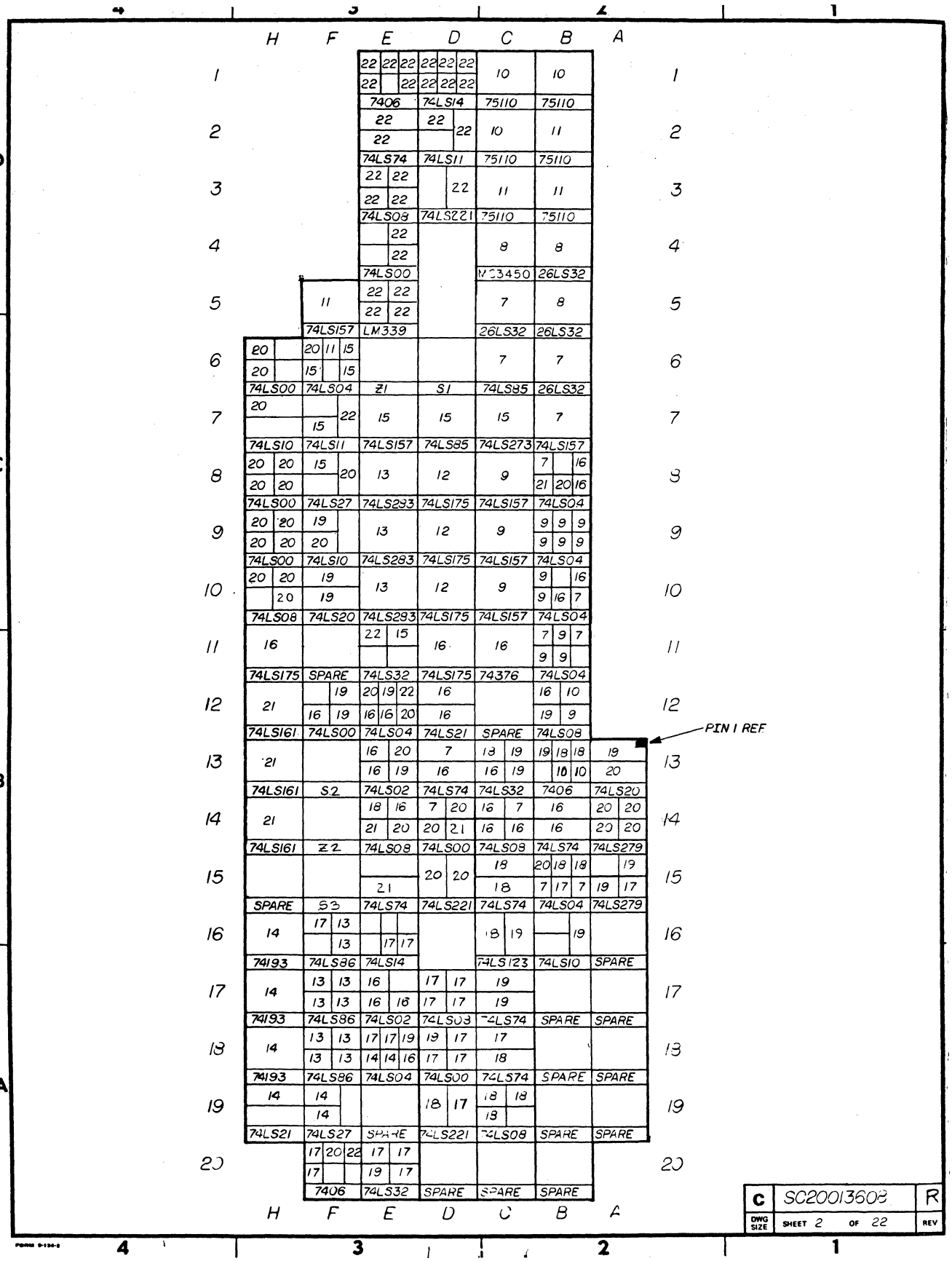
C SC20013603 R

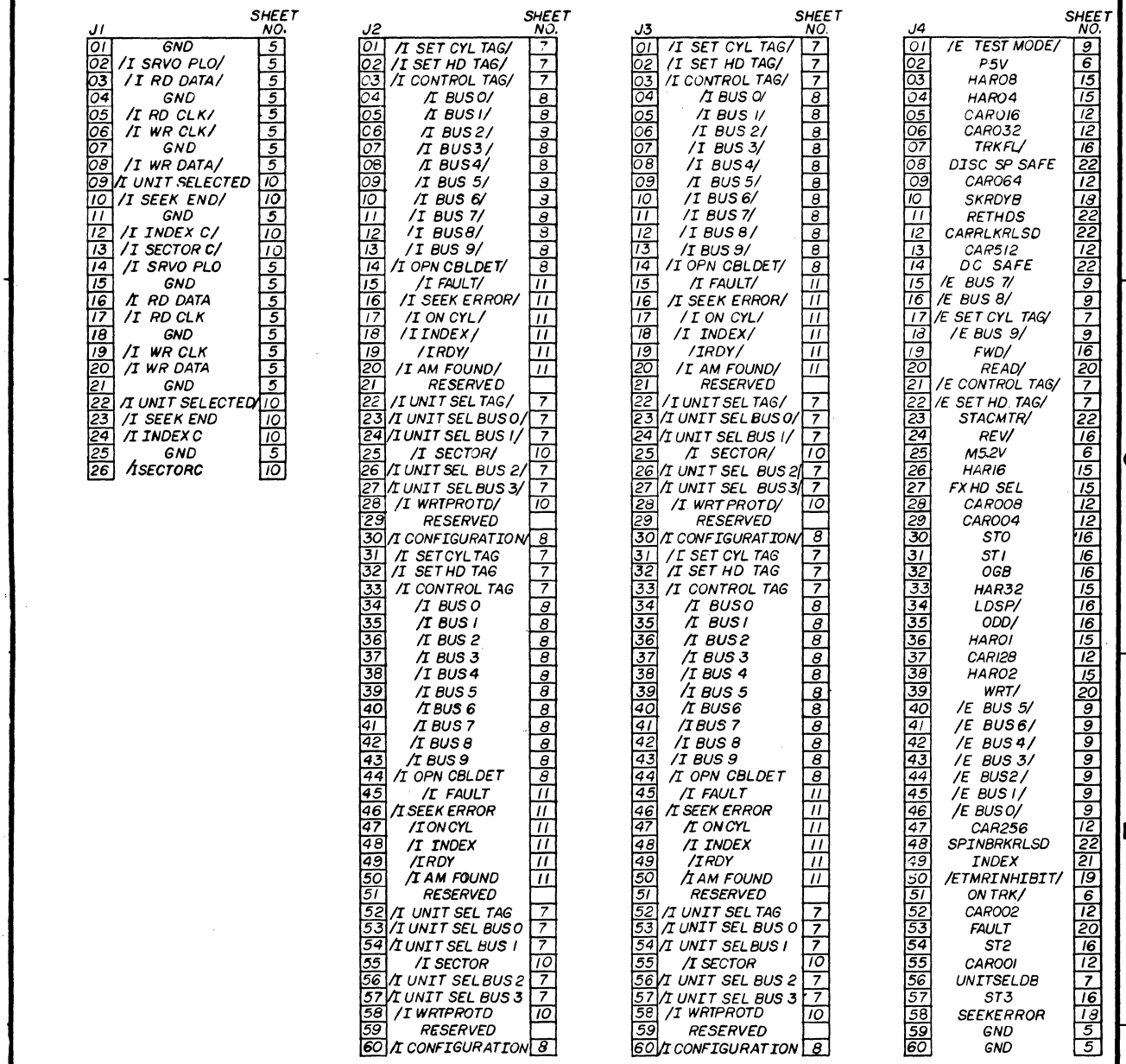
DWG SIZE

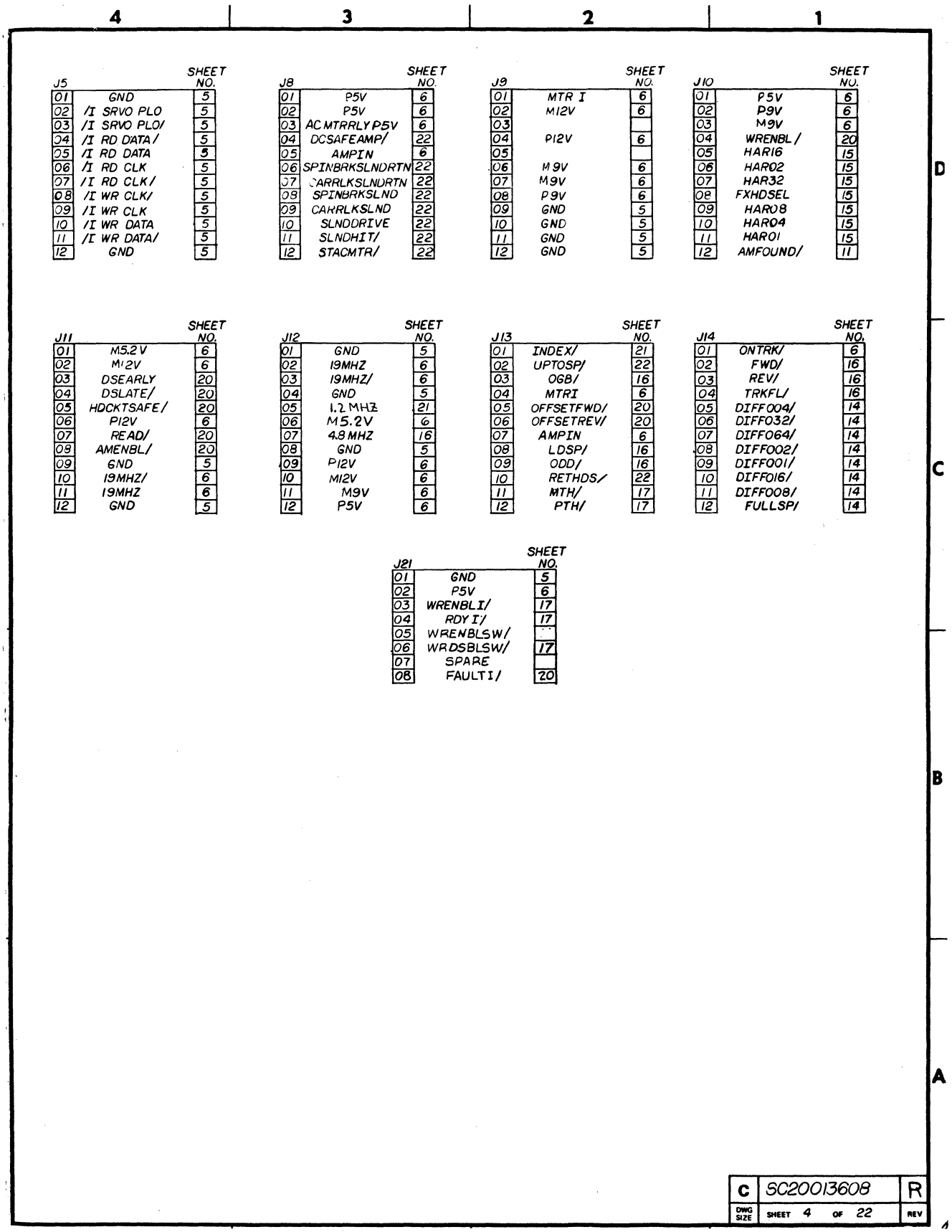
SHEET 1 OF 22

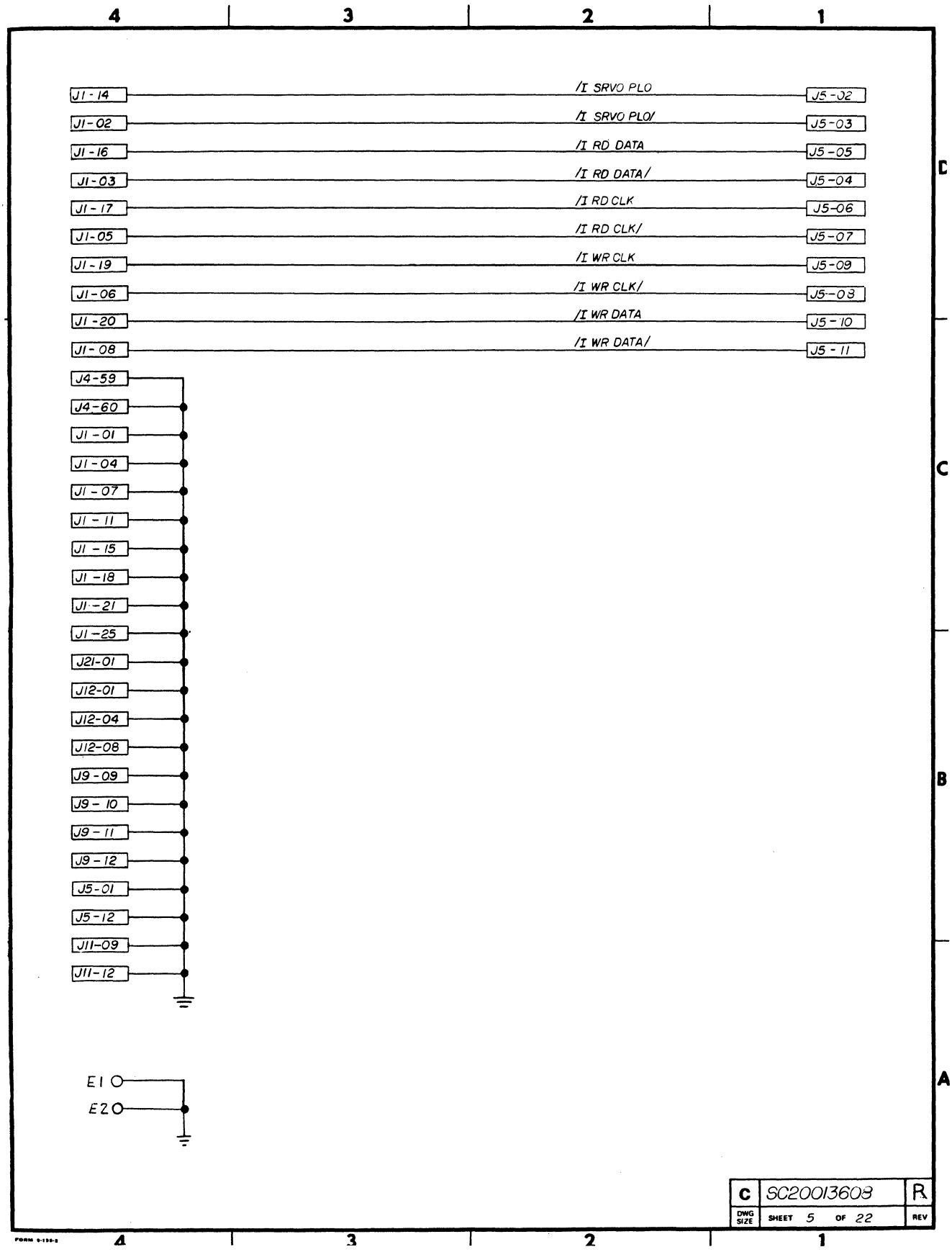
REV

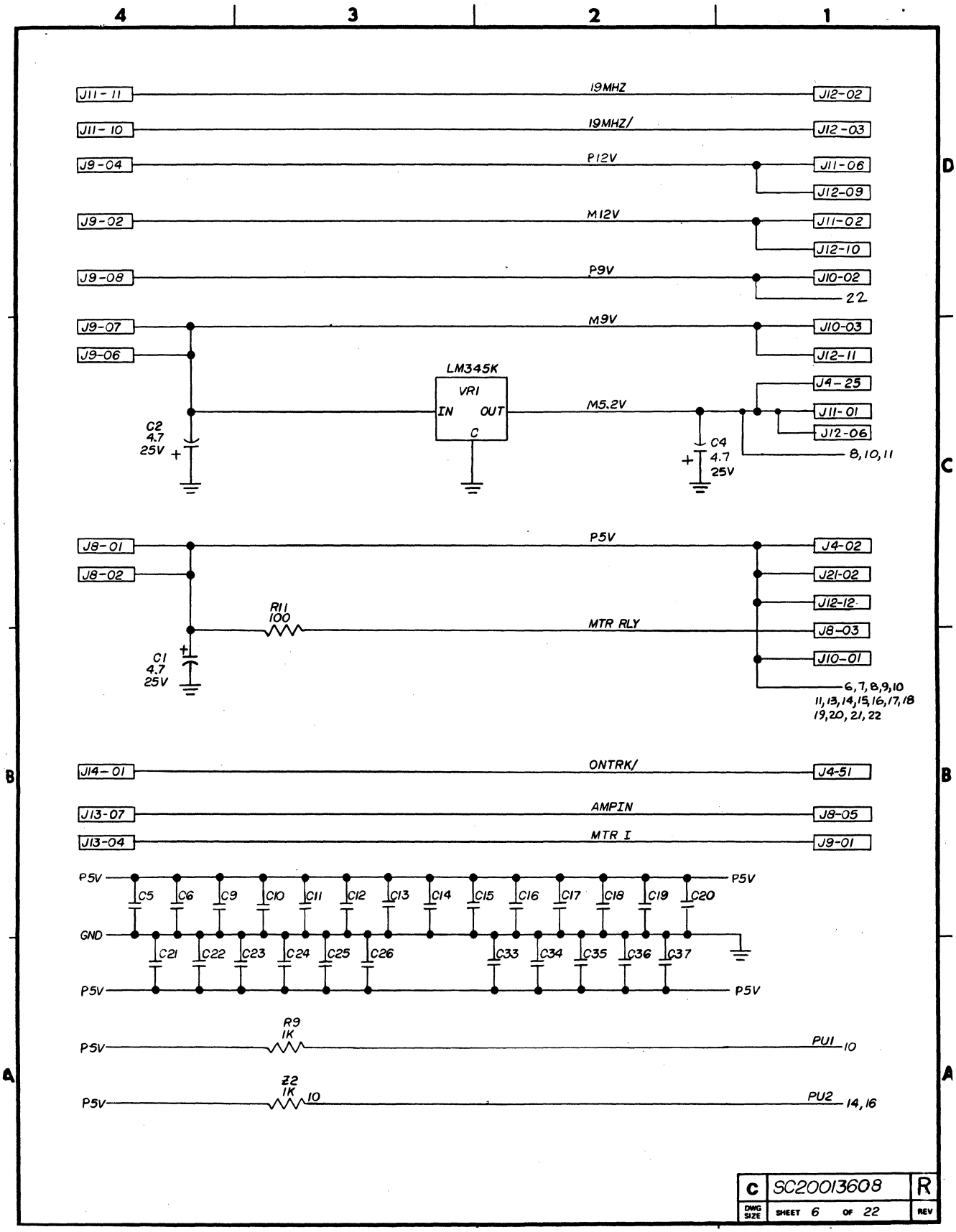
FORM 9-135-1

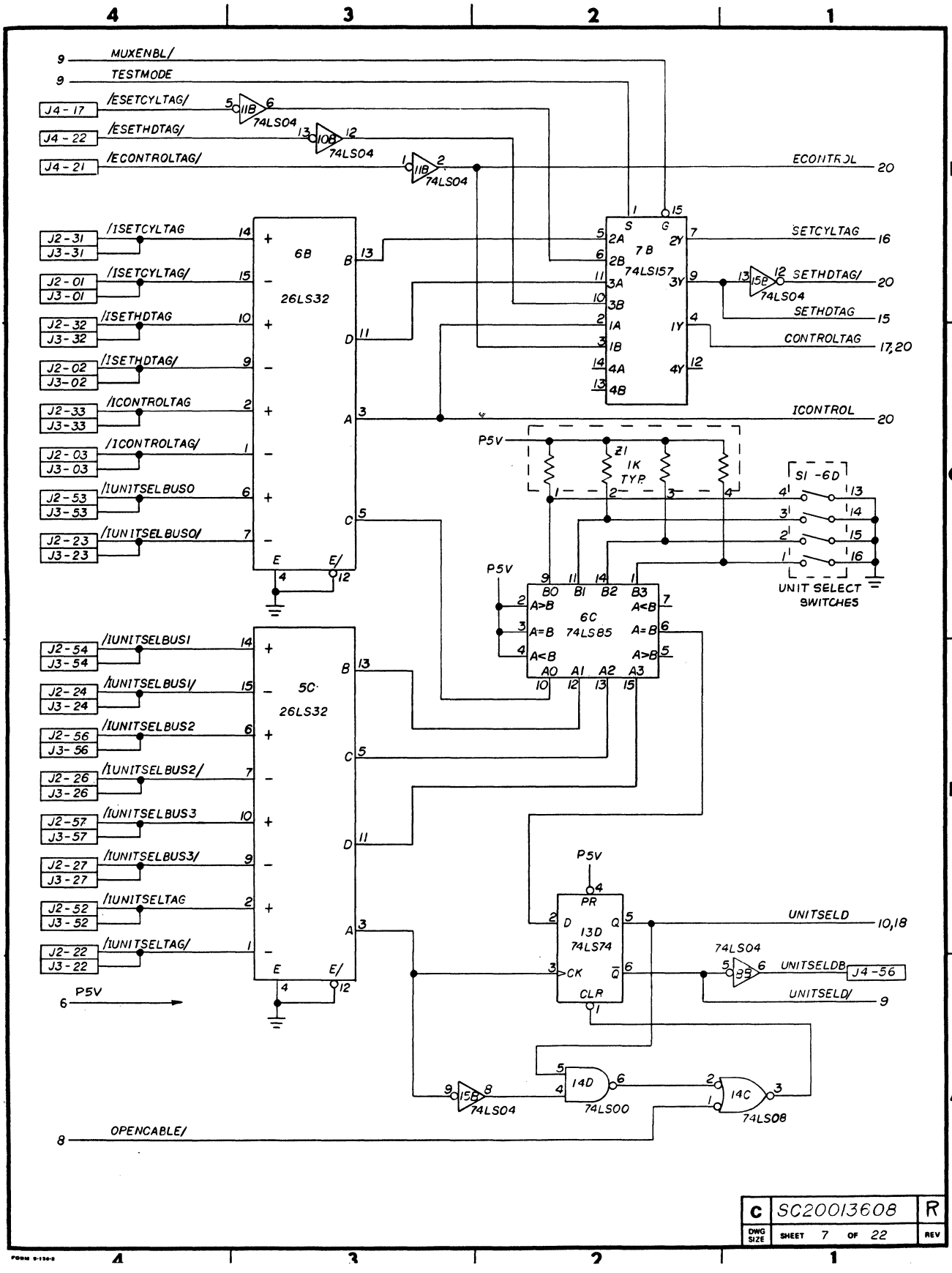

PIN 1 REF
C
SC20013603
R
DWG SIZE
SHEET 2 OF 22
REV

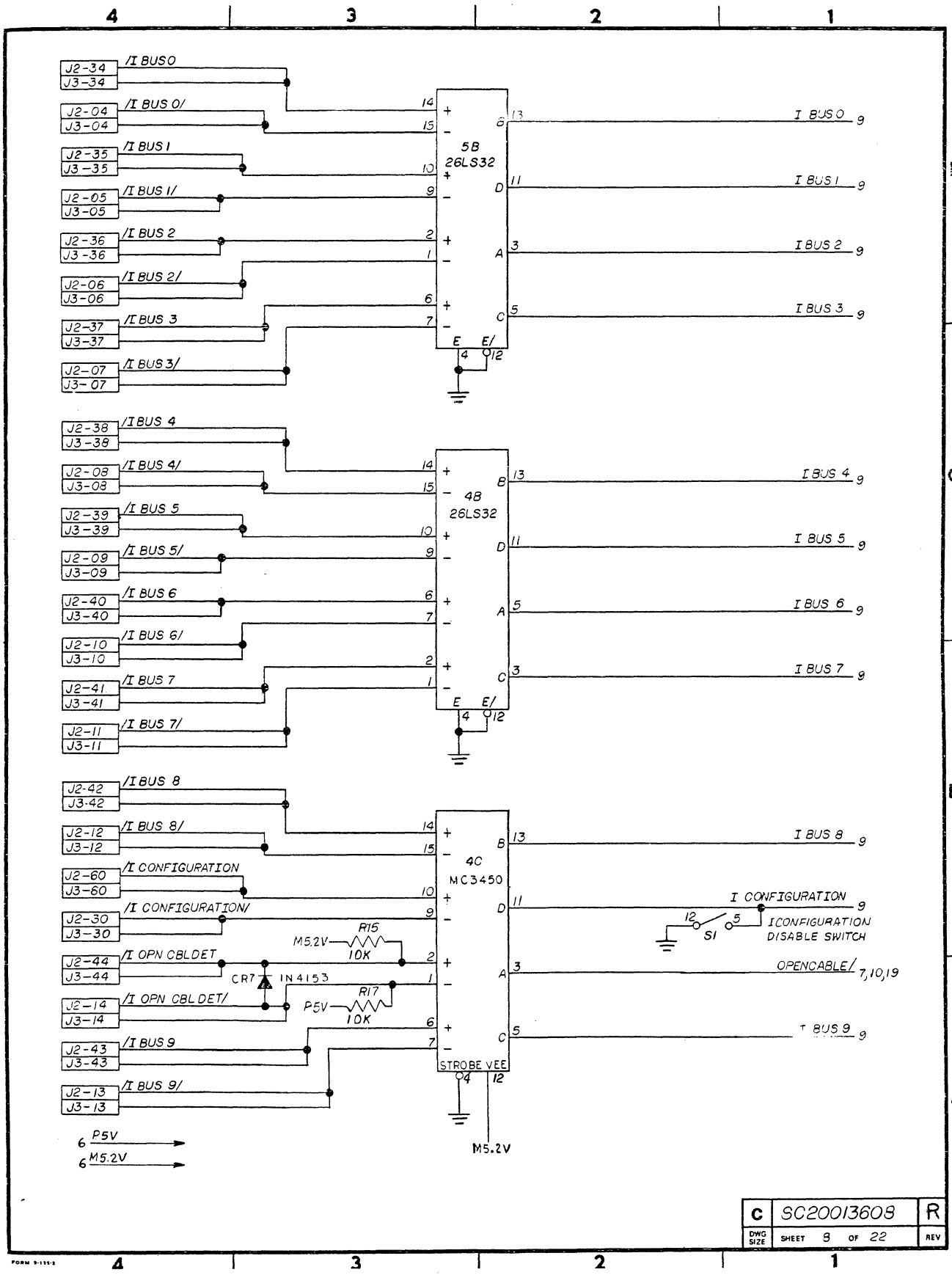

4
3
2
1
D
C
B
A
J1
SHEET NO.
01 GND 5
02 /I SRVO PLO/ 5
03 /I RD DATA/ 5
04 GND 5
05 /I RD CLK/ 5
06 /I WR CLK/ 5
07 GND 5
08 /I WR DATA/ 5
09 /I UNIT SELECTED 10
10 /I SEEK END/ 10
11 GND 5
12 /I INDEX C/ 10
13 /I SECTOR C/ 10
14 /I SRVO PLO 5
15 GND 5
16 /I RD DATA 5
17 /I RD CLK 5
18 GND 5
19 /I WR CLK 5
20 /I WR DATA 5
21 GND 5
22 /I UNIT SELECTED 10
23 /I SEEK END 10
24 /I INDEX C 10
25 GND 5
26 /I SECTOR C 10
J2
SHEET NO.
01 /I SET CYL TAG/ 7
02 /I SET HD TAG/ 7
03 /I CONTROL TAG/ 7
04 /I BUS 0/ 8
05 /I BUS 1/ 8
06 /I BUS 2/ 8
07 /I BUS 3/ 8
08 /I BUS 4/ 8
09 /I BUS 5/ 8
10 /I BUS 6/ 8
11 /I BUS 7/ 8
12 /I BUS 8/ 8
13 /I BUS 9/ 8
14 /I OPN CBL DET/ 8
15 /I FAULT/ 11
16 /I SEEK ERROR/ 11
17 /I ON CYL/ 11
18 /I INDEX/ 11
19 /IRDY/ 11
20 /I AM FOUND/ 11
21 RESERVED
22 /I UNIT SEL TAG/ 7
23 /I UNIT SEL BUS 0/ 7
24 /I UNIT SEL BUS 1/ 7
25 /I SECTOR/ 10
26 /I UNIT SEL BUS 2/ 7
27 /I UNIT SEL BUS 3/ 7
28 /I WRTPROTD/ 10
29 RESERVED
30 /I CONFIGURATION/ 8
31 /I SET CYL TAG 7
32 /I SET HD TAG 7
33 /I CONTROL TAG 7
34 /I BUS 0 8
35 /I BUS 1 8
36 /I BUS 2 8
37 /I BUS 3 8
38 /I BUS 4 8
39 /I BUS 5 8
40 /I BUS 6 8
41 /I BUS 7 8
42 /I BUS 8 8
43 /I BUS 9 8
44 /I OPN CBL DET 8
45 /I FAULT 11
46 /I SEEK ERROR 11
47 /I ON CYL 11
48 /I INDEX 11
49 /IRDY 11
50 /I AM FOUND 11
51 RESERVED
52 /I UNIT SEL TAG 7
53 /I UNIT SEL BUS 0 7
54 /I UNIT SEL BUS 1 7
55 /I SECTOR 10
56 /I UNIT SEL BUS 2 7
57 /I UNIT SEL BUS 3 7
58 /I WRTPROTD 10
59 RESERVED
60 /I CONFIGURATION 8
J3
SHEET NO.
01 /I SET CYL TAG/ 7
02 /I SET HD TAG/ 7
03 /I CONTROL TAG/ 7
04 /I BUS 0/ 8
05 /I BUS 1/ 8
06 /I BUS 2/ 8
07 /I BUS 3/ 8
08 /I BUS 4/ 8
09 /I BUS 5/ 8
10 /I BUS 6/ 8
11 /I BUS 7/ 8
12 /I BUS 8/ 8
13 /I BUS 9/ 8
14 /I OPN CBL DET/ 8
15 /I FAULT/ 11
16 /I SEEK ERROR/ 11
17 /I ON CYL/ 11
18 /I INDEX/ 11
19 /IRDY/ 11
20 /I AM FOUND/ 11
21 RESERVED
22 /I UNIT SEL TAG/ 7
23 /I UNIT SEL BUS 0/ 7
24 /I UNIT SEL BUS 1/ 7
25 /I SECTOR/ 10
26 /I UNIT SEL BUS 2/ 7
27 /I UNIT SEL BUS 3/ 7
28 /I WRTPROTD/ 10
29 RESERVED
30 /I CONFIGURATION/ 8
31 /I SET CYL TAG 7
32 /I SET HD TAG 7
33 /I CONTROL TAG 7
34 /I BUS 0 8
35 /I BUS 1 8
36 /I BUS 2 8
37 /I BUS 3 8
38 /I BUS 4 8
39 /I BUS 5 8
40 /I BUS 6 8
41 /I BUS 7 8
42 /I BUS 8 8
43 /I BUS 9 8
44 /I OPN CBL DET 8
45 /I FAULT 11
46 /I SEEK ERROR 11
47 /I ON CYL 11
48 /I INDEX 11
49 /IRDY 11
50 /I AM FOUND 11
51 RESERVED
52 /I UNIT SEL TAG 7
53 /I UNIT SEL BUS 0 7
54 /I UNIT SEL BUS 1 7
55 /I SECTOR 10
56 /I UNIT SEL BUS 2 7
57 /I UNIT SEL BUS 3 7
58 /I WRTPROTD 10
59 RESERVED
60 /I CONFIGURATION 8
J4
SHEET NO.
01 /E TEST MODE/ 9
02 P5V 6
03 HAR08 15
04 HAR04 15
05 CAR016 12
06 CAR032 12
07 TRKFL/ 16
08 DISC SP SAFE 22
09 CAR064 12
10 SKRDYB 18
11 RETHDS 22
12 CARRLKRLSD 22
13 CAR512 12
14 DC SAFE 22
15 /E BUS 7/ 9
16 /E BUS 8/ 9
17 /E SET CYL TAG/ 7
18 /E BUS 9/ 9
19 FWD/ 16
20 READ/ 20
21 /E CONTROL TAG/ 7
22 /E SET HD TAG/ 7
23 STACMTR/ 22
24 REV/ 16
25 M5.2V 6
26 HAR16 15
27 FX HD SEL 15
28 CAR008 12
29 CAR004 12
30 ST0 16
31 ST1 16
32 OGB 16
33 HAR32 15
34 LDSP/ 16
35 ODD/ 16
36 HAR01 15
37 CAR128 12
38 HAR02 15
39 WRT/ 20
40 /E BUS 5/ 9
41 /E BUS 6/ 9
42 /E BUS 4/ 9
43 /E BUS 3/ 9
44 /E BUS 2/ 9
45 /E BUS 1/ 9
46 /E BUS 0/ 9
47 CAR256 12
48 SPINBRKRLSD 22
49 INDEX 21
50 /ETMRINHIBIT/ 19
51 ON TRK/ 6
52 CAR002 12
53 FAULT 20
54 ST2 16
55 CAR001 12
56 UNITSELDB 7
57 ST3 16
58 SEEKERROR 18
59 GND 5
60 GND 5
C SC20013608 R
DWG SIZE SHEET 3 OF 22 REV

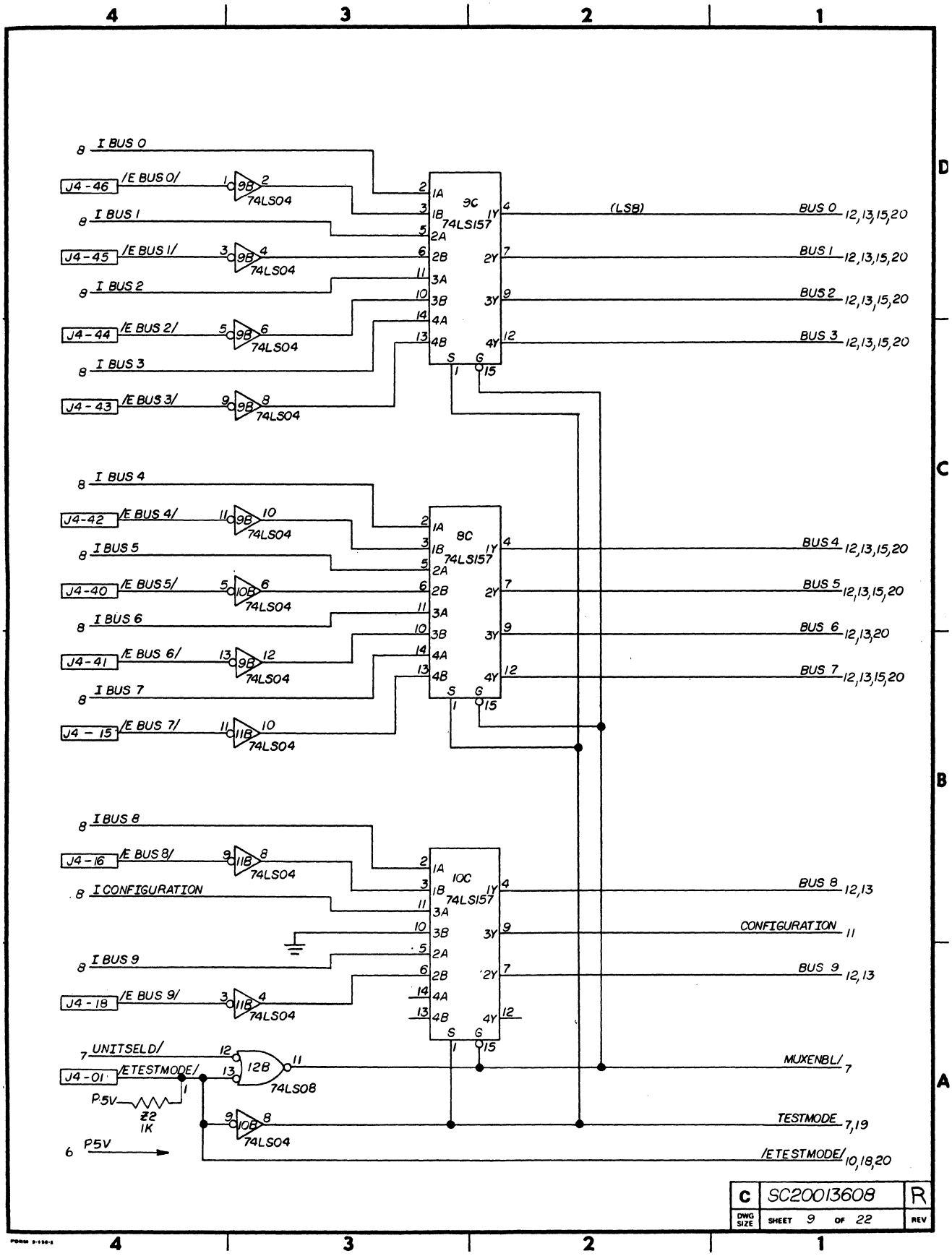

4
3
2
1
D
C
B
A
J5
01 GND 5
02 /I SRVO PLO 5
03 /I SRVO PLO/ 5
04 /I RD DATA/ 5
05 /I RD DATA 5
06 /I RD CLK 5
07 /I RD CLK/ 5
08 /I WR CLK/ 5
09 /I WR CLK 5
10 /I WR DATA 5
11 /I WR DATA/ 5
12 GND 5
J8
01 P5V 6
02 P5V 6
03 AC MTRRLY P5V 6
04 DCSAFEAMP/ 22
05 AMPIN 6
06 SPINBRKSLNDRTN 22
07 CARRLKSLNDRTN 22
08 SPINBRKSLND 22
09 CARRLKSLND 22
10 SLNDDRIVE 22
11 SLNDHIT/ 22
12 STACMTR/ 22
J9
01 MTR I 6
02 M12V 6
03
04 P12V 6
05
06 M9V 6
07 M9V 6
08 P9V 6
09 GND 5
10 GND 5
11 GND 5
12 GND 5
J10
01 P5V 6
02 P9V 6
03 M9V 6
04 WRENBL/ 20
05 HARI6 15
06 HAR02 15
07 HAR32 15
08 FXHDSEL 15
09 HAR08 15
10 HAR04 15
11 HAR01 15
12 AMFOUND/ 11
J11
01 M5.2V 6
02 M12V 6
03 DSEARLY 20
04 DSLATE/ 20
05 HDCKTSAFE/ 20
06 P12V 6
07 READ/ 20
08 AMENBL/ 20
09 GND 5
10 I9MHZ/ 6
11 I9MHZ 6
12 GND 5
J12
01 GND 5
02 I9MHZ 6
03 I9MHZ/ 6
04 GND 5
05 1.2 MHZ 21
06 M5.2V 6
07 4.8 MHZ 16
08 GND 5
09 P12V 6
10 M12V 6
11 M9V 6
12 P5V 6
J13
01 INDEX/ 21
02 UPTOSP/ 22
03 OGB/ 16
04 MTRI 6
05 OFFSETFWD/ 20
06 OFFSETREV/ 20
07 AMPIN 6
08 LDSP/ 16
09 ODD/ 16
10 RETHDS/ 22
11 MTH/ 17
12 PTH/ 17
J14
01 ONTRK/ 6
02 FWD/ 16
03 REV/ 16
04 TRKFL/ 16
05 DIFF004/ 14
06 DIFF032/ 14
07 DIFF064/ 14
08 DIFF002/ 14
09 DIFF001/ 14
10 DIFF016/ 14
11 DIFF008/ 14
12 FULLSP/ 14
J21
01 GND 5
02 P5V 6
03 WRENBLI/ 17
04 RDYI/ 17
05 WRENBLSW/ 17
06 WRDSBLSW/ 17
07 SPARE
08 FAULTI/ 20
C SC20013608 R
DWG SIZE SHEET 4 OF 22 REV

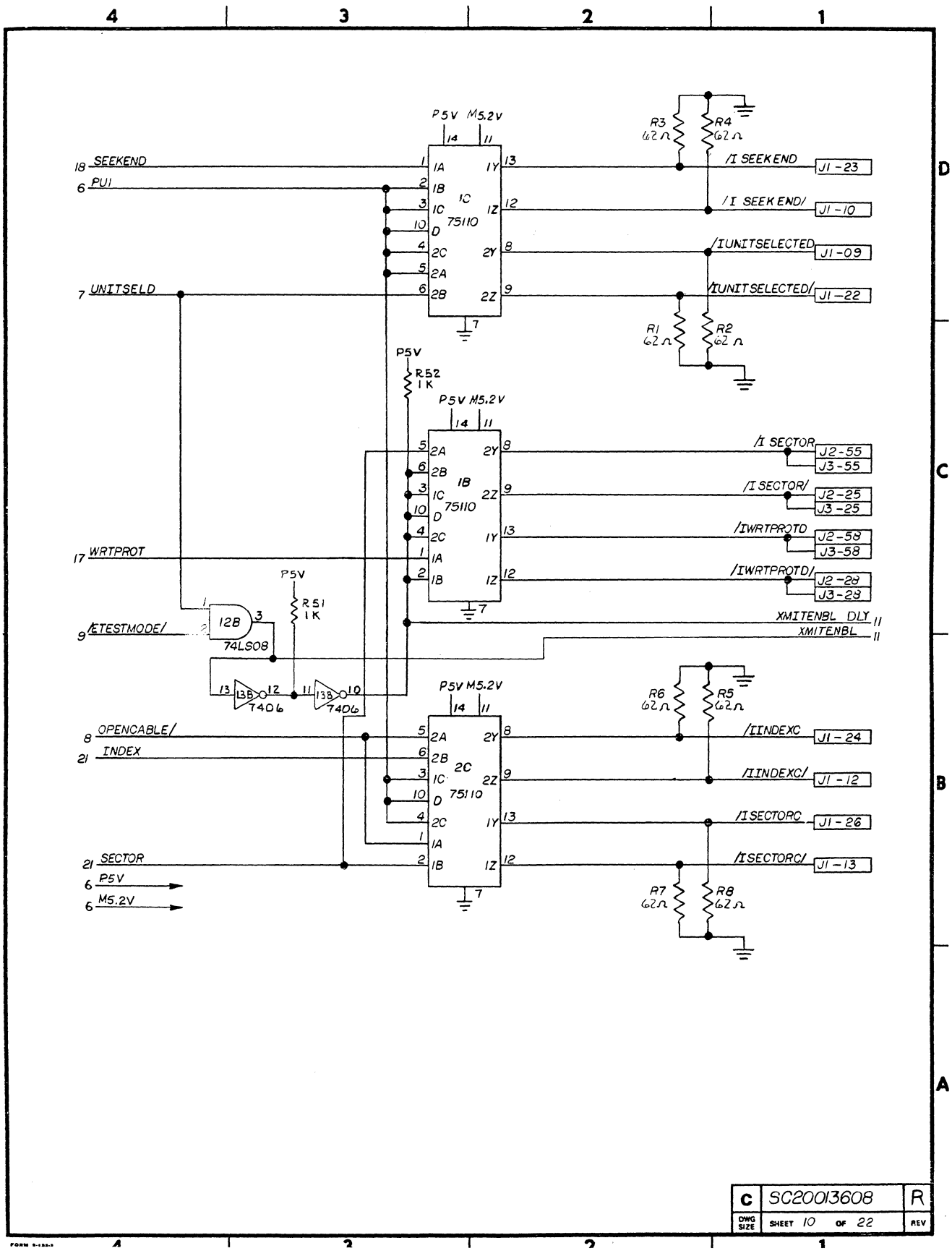

4
3
2
1
J1 - 14
/I SRVO PLO
J5 - 02
J1 - 02
/I SRVO PLO/
J5 - 03
J1 - 16
/I RD DATA
J5 - 05
J1 - 03
/I RD DATA/
J5 - 04
J1 - 17
/I RD CLK
J5 - 06
J1 - 05
/I RD CLK/
J5 - 07
J1 - 19
/I WR CLK
J5 - 09
J1 - 06
/I WR CLK/
J5 - 08
J1 - 20
/I WR DATA
J5 - 10
J1 - 08
/I WR DATA/
J5 - 11
J4 - 59
J4 - 60
J1 - 01
J1 - 04
J1 - 07
J1 - 11
J1 - 15
J1 - 18
J1 - 21
J1 - 25
J21 - 01
J12 - 01
J12 - 04
J12 - 08
J9 - 09
J9 - 10
J9 - 11
J9 - 12
J5 - 01
J5 - 12
J11 - 09
J11 - 12
E1
E2
D
C
B
A
C
SC20013603
R
DWG SIZE
SHEET 5 OF 22
REV
4
3
2
1

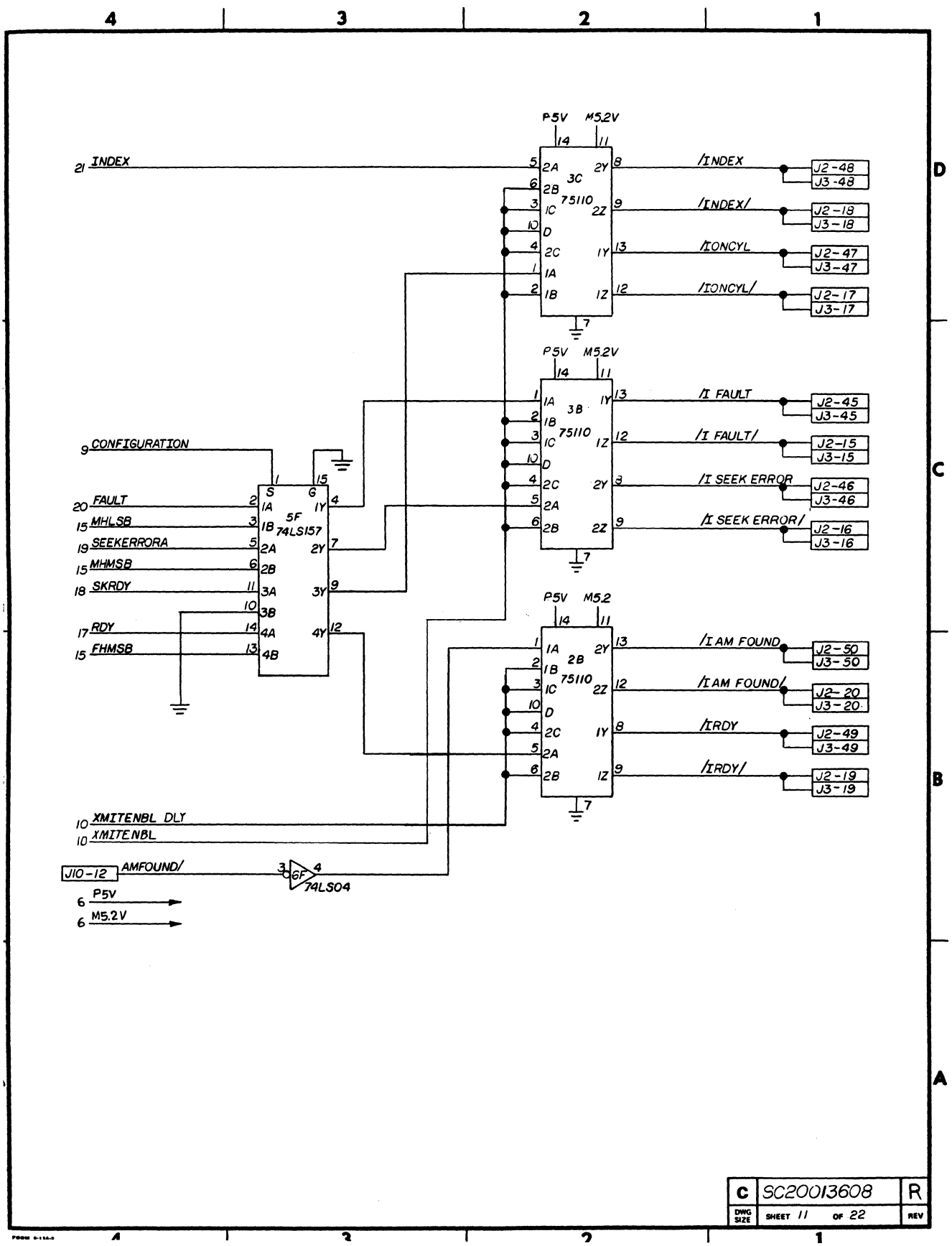

4
3
2
1
J11-11
19MHZ
J12-02
J11-10
19MHZ/
J12-03
J9-04
P12V
J11-06
J12-09
J9-02
M12V
J11-02
J12-10
J9-08
P9V
J10-02
22
J9-07
J9-06
M9V
J10-03
J12-11
LM345K
VR1
IN
OUT
C
M5.2V
J4-25
J11-01
J12-06
8,10,11
C2
4.7
25V
C4
4.7
25V
J8-01
J8-02
P5V
J4-02
J21-02
J12-12
J8-03
J10-01
R11
100
MTR RLY
C1
4.7
25V
6,7,8,9,10
11,13,14,15,16,17,18
19,20,21,22
J14-01
ONTRK/
J4-51
J13-07
AMPIN
J8-05
J13-04
MTR I
J9-01
P5V
GND
C5
C6
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C33
C34
C35
C36
C37
R9
1K
PU1
10
22
1K
10
PU2
14,16
A
B
C
D
C
SC20013608
R
DWG SIZE
SHEET 6 OF 22
REV

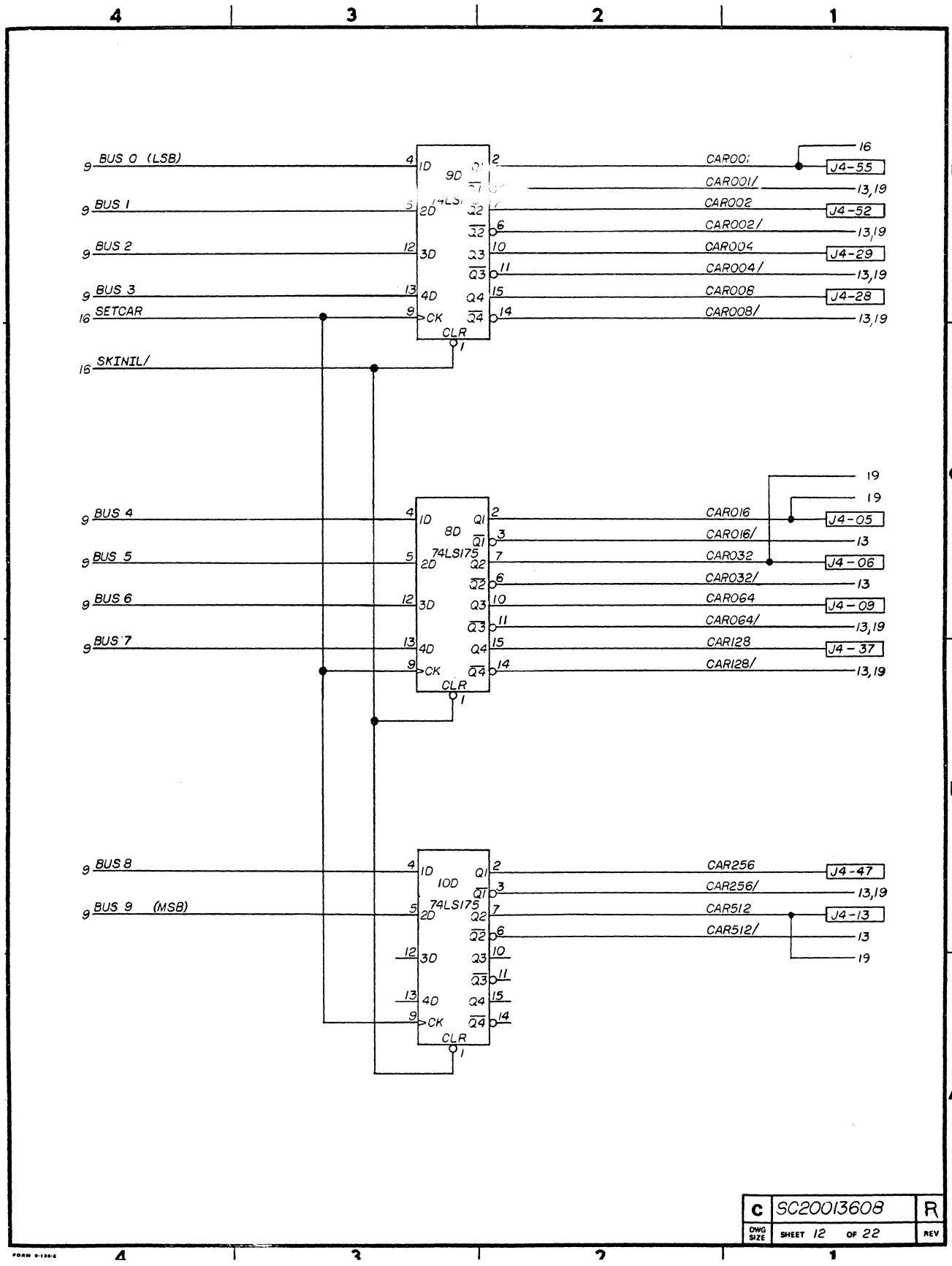

MUXENBL/
TESTMODE
/ESETCYLTAG/
/ESETHDTAG/
/ECONTROLTAG/
74LS04
ECONTROL
20
/ISETCYLTAG
/ISETCYLTAG/
/ISETHDTAG
/ISETHDTAG/
/ICONTROLTAG
/ICONTROLTAG/
/IUNITSELBUS0
/IUNITSELBUS0/
6B
26LS32
74LS157
SETCYLTAG
16
SETHDTAG/
SETHDTAG
15
CONTROLTAG
17,20
ICONTROL
P5V
1K TYP.
S1-6D
UNIT SELECT SWITCHES
6C
74LS85
/IUNITSELBUS1
/IUNITSELBUS1/
/IUNITSELBUS2
/IUNITSELBUS2/
/IUNITSELBUS3
/IUNITSELBUS3/
/IUNITSELTAG
/IUNITSELTAG/
5C
26LS32
13D
74LS74
UNITSELD
10,18
UNITSELDB
J4-56
UNITSELD/
9
14D
74LS00
14C
74LS08
OPENCABLE/
8
C
SC20013608
R
DWG SIZE
SHEET 7 OF 22
REV

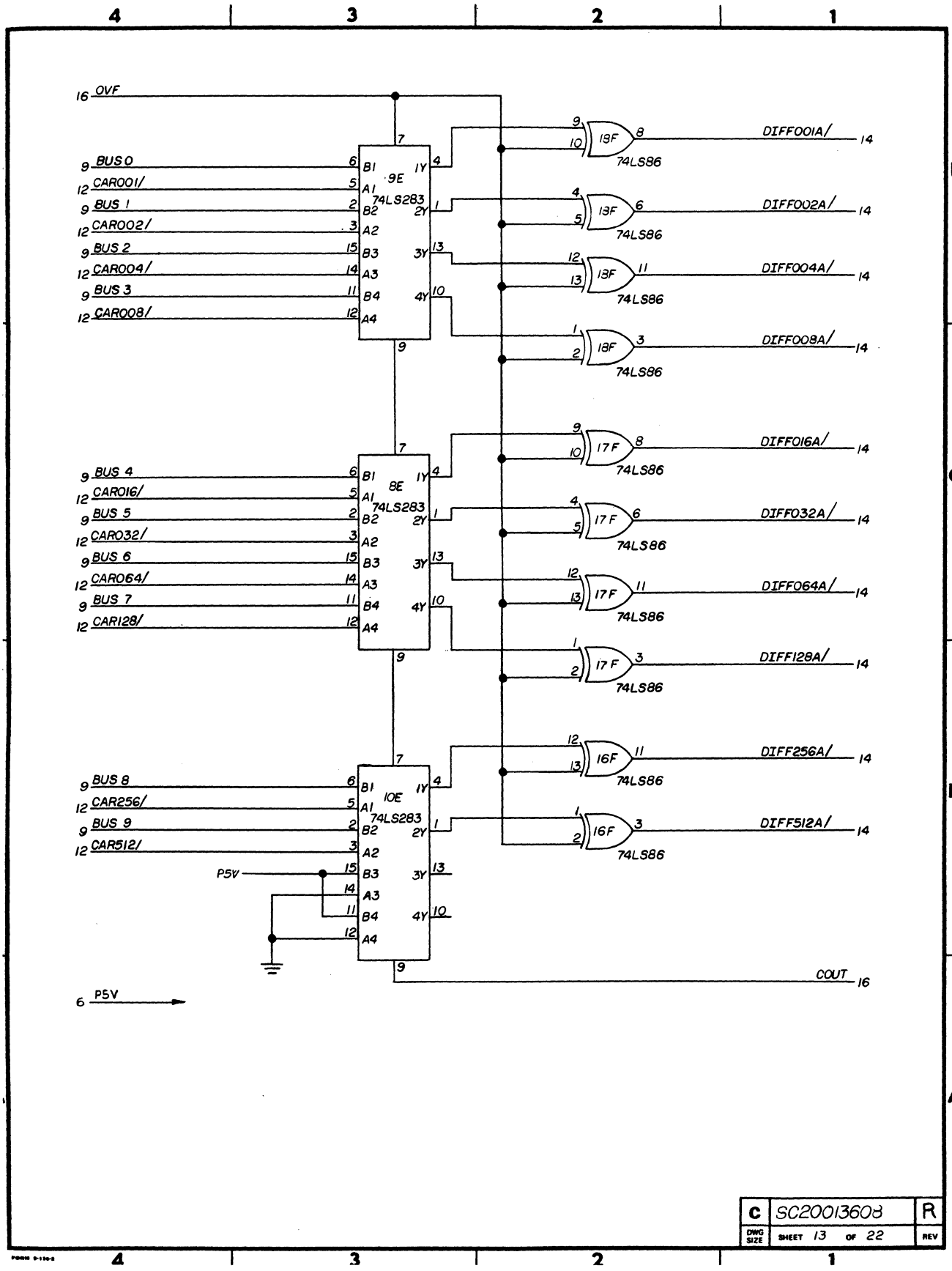

4
3
2
1
J2-34
J3-34
/I BUS0
J2-04
J3-04
/I BUS 0/
J2-35
J3-35
/I BUS 1
J2-05
J3-05
/I BUS 1/
J2-36
J3-36
/I BUS 2
J2-06
J3-06
/I BUS 2/
J2-37
J3-37
/I BUS 3
J2-07
J3-07
/I BUS 3/
5B
26LS32
I BUS 0
I BUS 1
I BUS 2
I BUS 3
J2-38
J3-38
/I BUS 4
J2-08
J3-08
/I BUS 4/
J2-39
J3-39
/I BUS 5
J2-09
J3-09
/I BUS 5/
J2-40
J3-40
/I BUS 6
J2-10
J3-10
/I BUS 6/
J2-41
J3-41
/I BUS 7
J2-11
J3-11
/I BUS 7/
4B
26LS32
I BUS 4
I BUS 5
I BUS 6
I BUS 7
J2-42
J3-42
/I BUS 8
J2-12
J3-12
/I BUS 8/
J2-60
J3-60
/I CONFIGURATION
J2-30
J3-30
/I CONFIGURATION/
J2-44
J3-44
/I OPN CBLDET
J2-14
J3-14
/I OPN CBL DET/
J2-43
J3-43
/I BUS 9
J2-13
J3-13
/I BUS 9/
4C
MC3450
STROBE VEE
M5.2V
P5V
M5.2V
R15
10K
R17
10K
CR7
IN4153
I BUS 8
I CONFIGURATION
S1
ICONFIGURATION
DISABLE SWITCH
OPENCABLE/
7,10,19
I BUS 9
6 P5V
6 M5.2V
D
C
B
A
C
SC20013608
R
DWG SIZE
SHEET 9 OF 22
REV

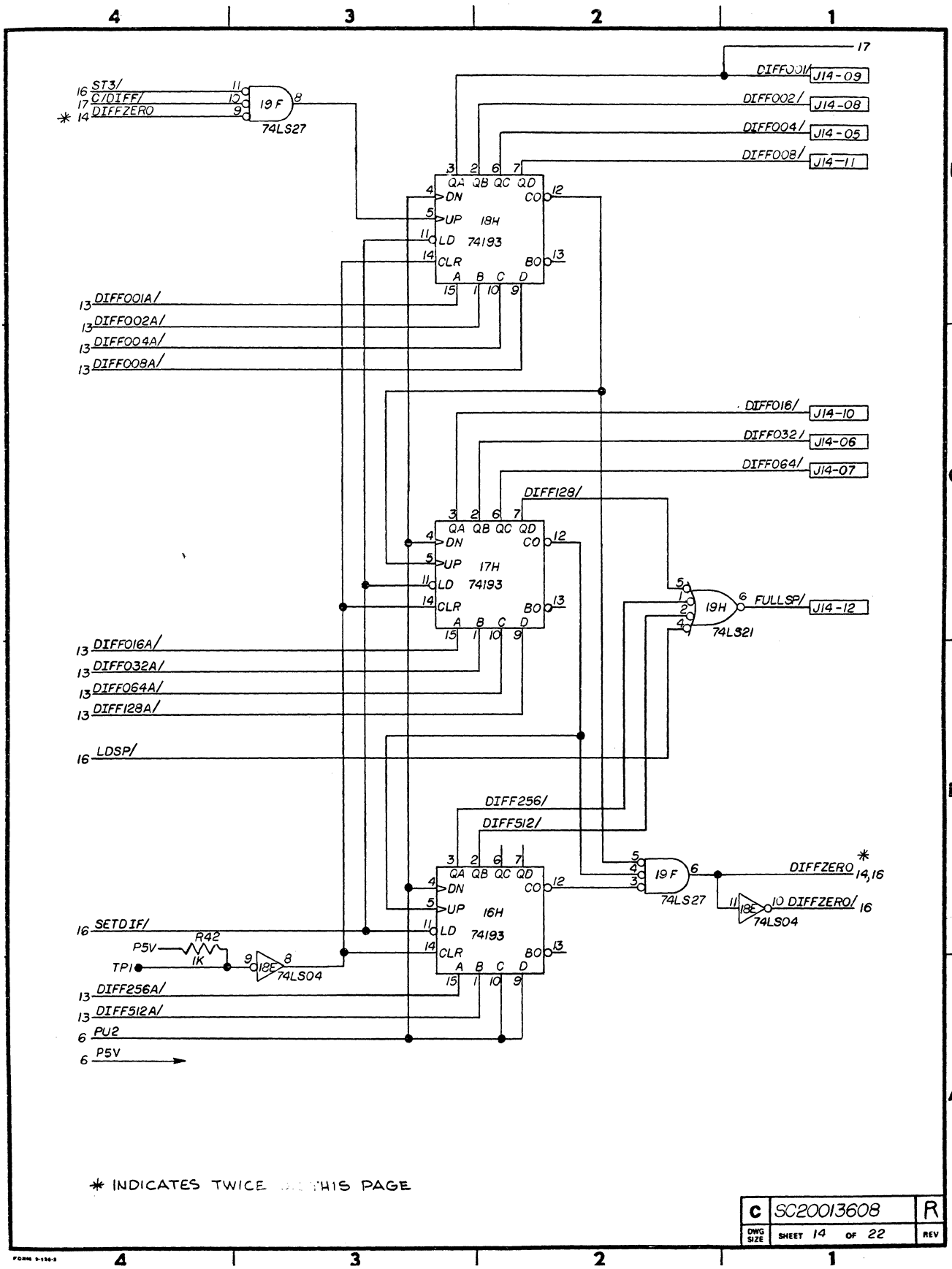

4
3
2
1
D
C
B
A
8 I BUS 0
J4-46 /E BUS 0/
9B 74LS04
8 I BUS 1
J4-45 /E BUS 1/
9B 74LS04
8 I BUS 2
J4-44 /E BUS 2/
9B 74LS04
8 I BUS 3
J4-43 /E BUS 3/
9B 74LS04
9C 74LS157
1A 1B 2A 2B 3A 3B 4A 4B S G
1Y 2Y 3Y 4Y
(LSB)
BUS 0 12,13,15,20
BUS 1 12,13,15,20
BUS 2 12,13,15,20
BUS 3 12,13,15,20
8 I BUS 4
J4-42 /E BUS 4/
9B 74LS04
8 I BUS 5
J4-40 /E BUS 5/
10B 74LS04
8 I BUS 6
J4-41 /E BUS 6/
9B 74LS04
8 I BUS 7
J4-15 /E BUS 7/
11B 74LS04
8C 74LS157
BUS 4 12,13,15,20
BUS 5 12,13,15,20
BUS 6 12,13,20
BUS 7 12,13,15,20
8 I BUS 8
J4-16 /E BUS 8/
11B 74LS04
8 I CONFIGURATION
8 I BUS 9
J4-18 /E BUS 9/
11B 74LS04
10C 74LS157
BUS 8 12,13
CONFIGURATION 11
BUS 9 12,13
7 UNITSELD/
J4-01 /ETESTMODE/
12B 74LS08
P5V
Z2 1K
9 10B 8 74LS04
6 P5V
MUXENBL/ 7
TESTMODE 7,19
/ETESTMODE/ 10,18,20
C SC20013608 R
DWG SIZE SHEET 9 OF 22 REV

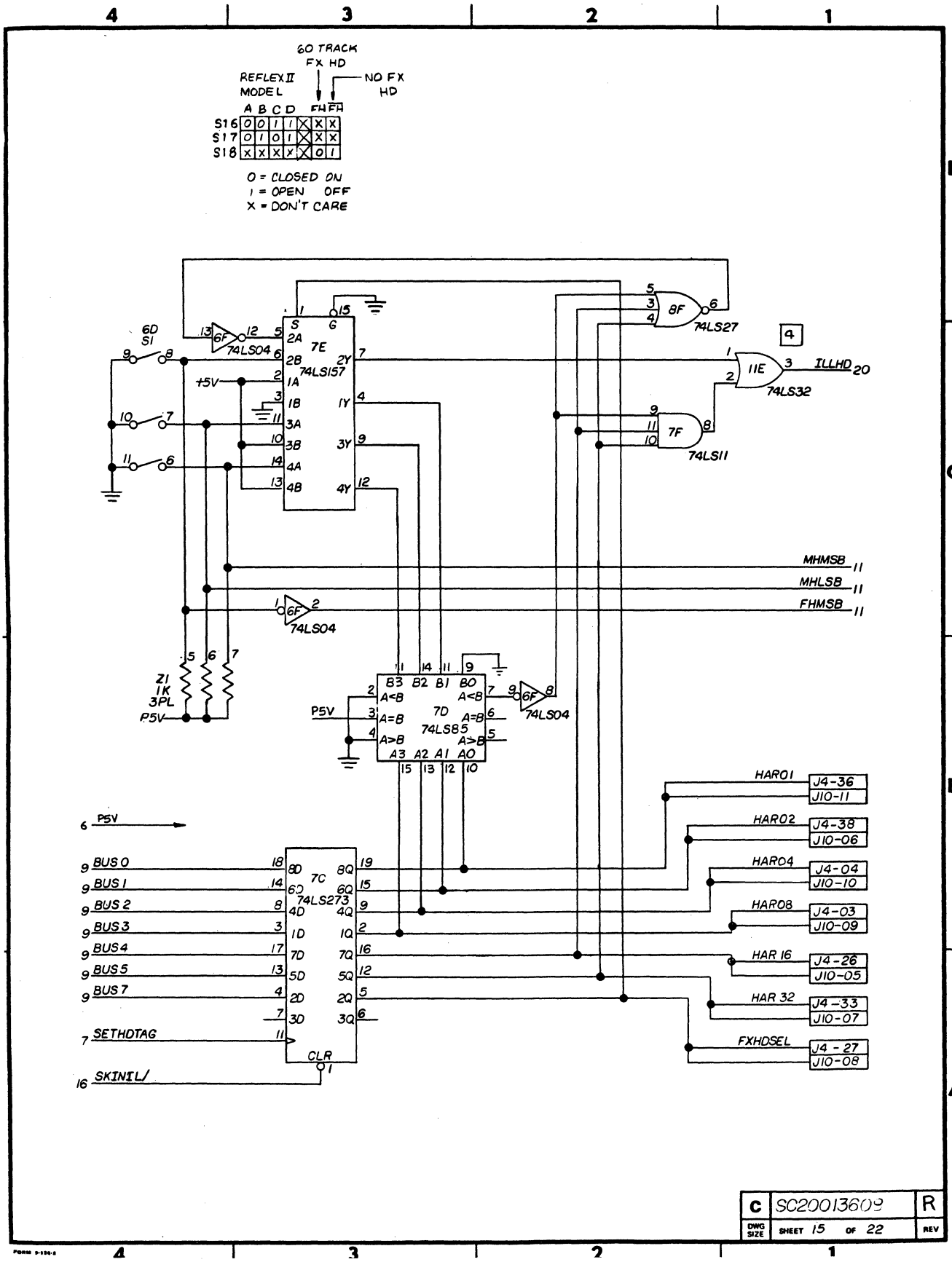

4
3
2
1
D
C
B
A
P5V M5.2V
1C
75110
18 SEEKEND
6 PUI
7 UNITSELD
R3 62Ω
R4 62Ω
/I SEEKEND
J1-23
/I SEEKEND/
J1-10
/IUNITSELECTED
J1-09
/IUNITSELECTED/
J1-22
R1 62Ω
R2 62Ω
P5V
R52 1K
1B
75110
/I SECTOR
J2-55
J3-55
/I SECTOR/
J2-25
J3-25
/IWRTPROTD
J2-58
J3-58
/IWRTPROTD/
J2-28
J3-28
17 WRTPROT
9 /ETESTMODE/
R51 1K
12B
74LS08
7406
XMITENBL DLY 11
XMITENBL 11
2C
75110
8 OPENCABLE/
21 INDEX
21 SECTOR
6 P5V
6 M5.2V
R6 62Ω
R5 62Ω
/IINDEXC
J1-24
/IINDEXC/
J1-12
/ISECTORC
J1-26
/ISECTORC/
J1-13
R7 62Ω
R8 62Ω
C
SC20013608
R
DWG SIZE
SHEET 10 OF 22
REV


4
3
2
1
D
C
B
A
P5V
M5.2V
21 INDEX
3C
75110
/INDEX
/INDEX/
/IONCYL
/IONCYL/
J2-48
J3-48
J2-18
J3-18
J2-47
J3-47
J2-17
J3-17
3B
/I FAULT
/I FAULT/
/I SEEK ERROR
/I SEEK ERROR/
J2-45
J3-45
J2-15
J3-15
J2-46
J3-46
J2-16
J3-16
2B
/I AM FOUND
/I AM FOUND/
/IRDY
/IRDY/
J2-50
J3-50
J2-20
J3-20
J2-49
J3-49
J2-19
J3-19
9 CONFIGURATION
20 FAULT
15 MHLSB
19 SEEKERRORA
15 MHMSB
18 SKRDY
17 RDY
15 FHMSB
5F
74LS157
10 XMITENBL DLY
10 XMITENBL
J10-12 AMFOUND/
6F
74LS04
6 P5V
6 M5.2V
C
SC20013608
R
DWG SIZE
SHEET 11 OF 22
REV

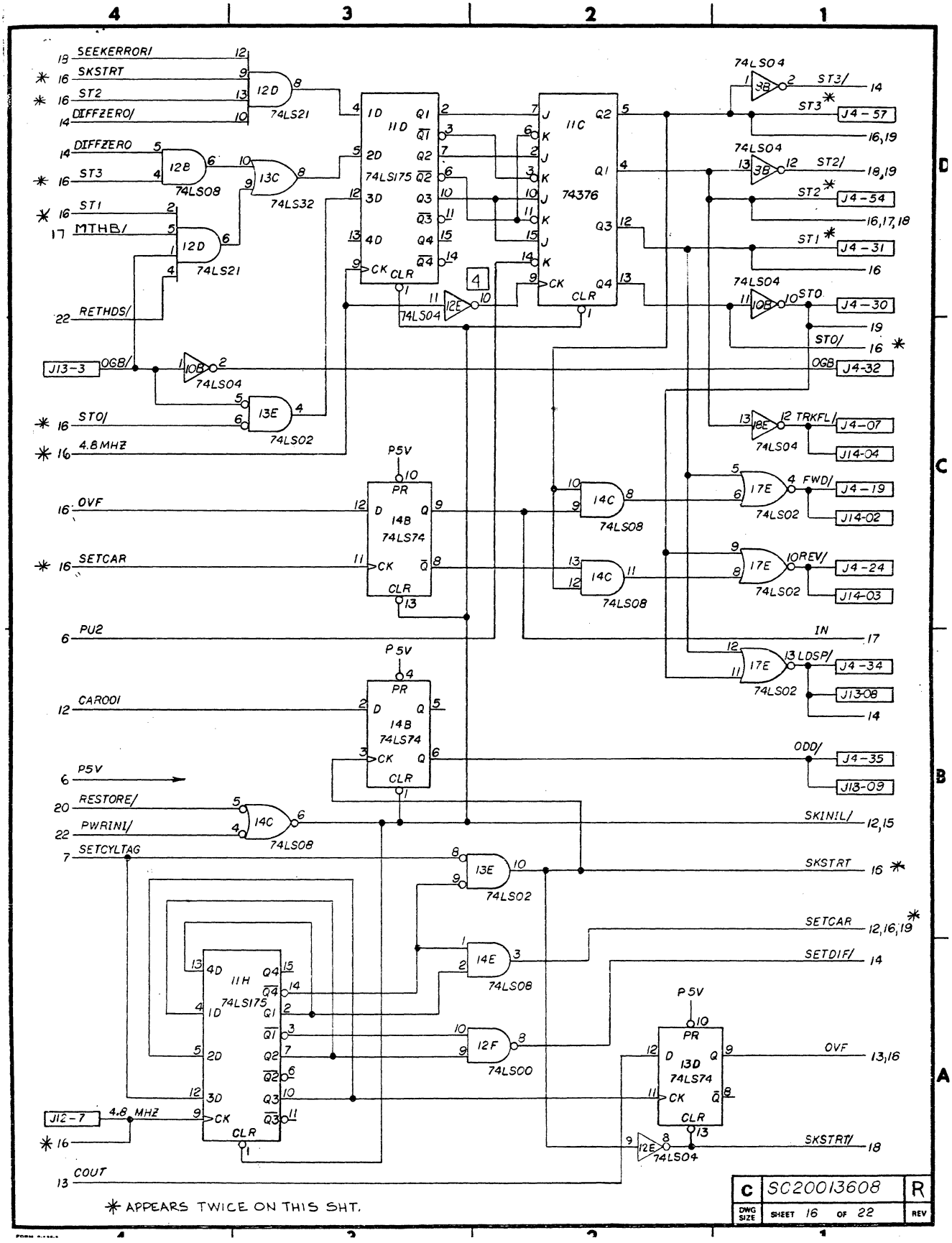

4
3
2
1
D
C
B
A
9 BUS 0 (LSB)
9 BUS 1
9 BUS 2
9 BUS 3
16 SETCAR
16 SKINIL/
9D
74LS175
1D
2D
3D
4D
CK
CLR
Q1
Q2
Q3
Q4
CAR001
CAR001/
CAR002
CAR002/
CAR004
CAR004/
CAR008
CAR008/
J4-55
J4-52
J4-29
J4-28
13,19
9 BUS 4
9 BUS 5
9 BUS 6
9 BUS 7
8D
CAR016
CAR016/
CAR032
CAR032/
CAR064
CAR064/
CAR128
CAR128/
J4-05
J4-06
J4-09
J4-37
19
13
9 BUS 8
9 BUS 9 (MSB)
10D
CAR256
CAR256/
CAR512
CAR512/
J4-47
J4-13
C
SC20013608
R
DWG SIZE
SHEET 12 OF 22
REV

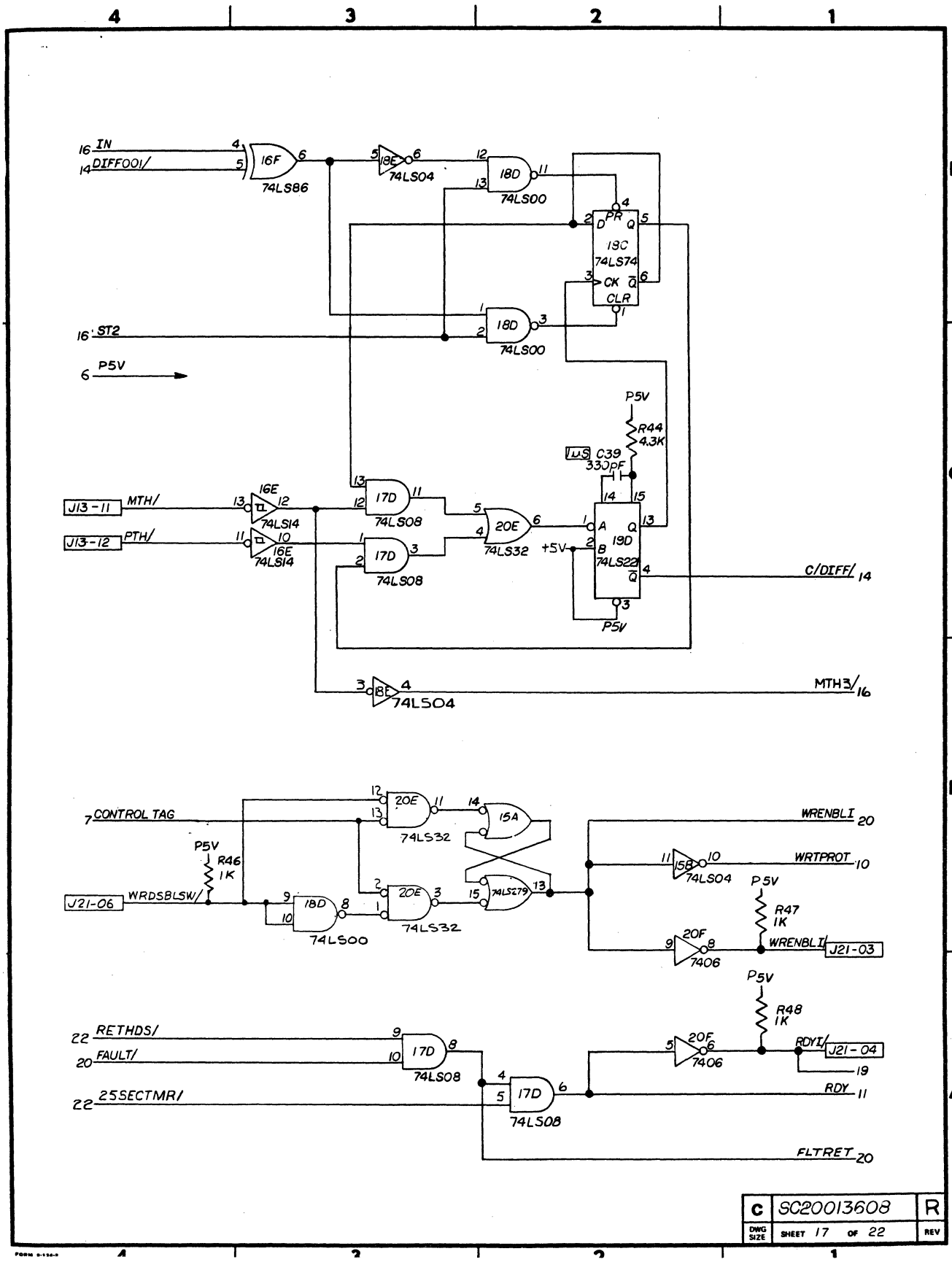

4
3
2
1
D
C
B
A
16 OVF
9 BUS 0
12 CAR001/
9 BUS 1
12 CAR002/
9 BUS 2
12 CAR004/
9 BUS 3
12 CAR008/
9 BUS 4
12 CAR016/
9 BUS 5
12 CAR032/
9 BUS 6
12 CAR064/
9 BUS 7
12 CAR128/
9 BUS 8
12 CAR256/
9 BUS 9
12 CAR512/
P5V
6 P5V
9E
8E
10E
74LS283
B1
A1
B2
A2
B3
A3
B4
A4
1Y
2Y
3Y
4Y
18F
17F
16F
74LS86
DIFF001A/
DIFF002A/
DIFF004A/
DIFF008A/
DIFF016A/
DIFF032A/
DIFF064A/
DIFF128A/
DIFF256A/
DIFF512A/
COUT
C
SC20013608
R
DWG SIZE
SHEET 13 OF 22
REV

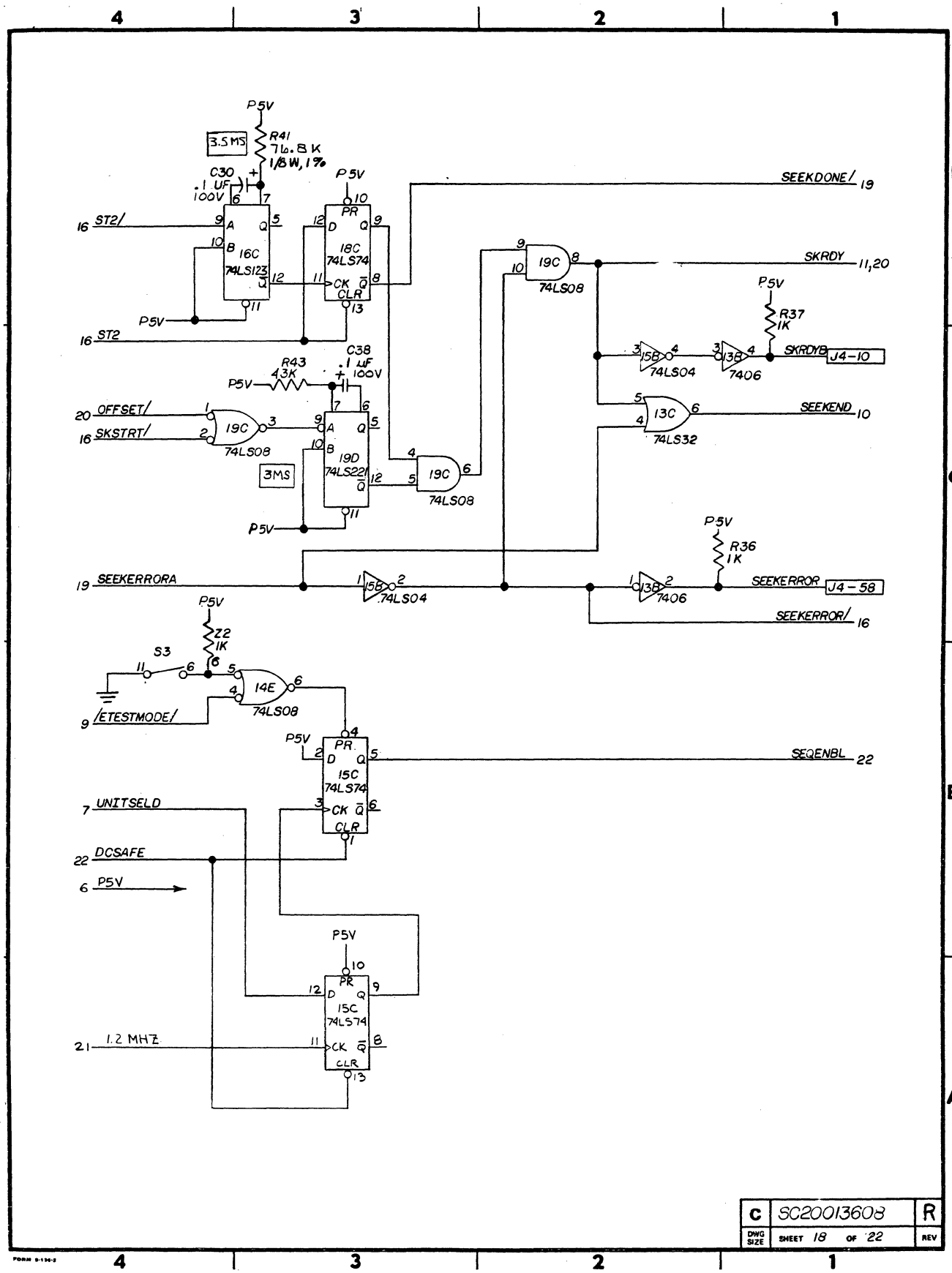

4
3
2
1
D
C
B
A
16 ST3/
17 C/DIFF/
* 14 DIFFZERO
19 F
74LS27
17
DIFF001/ J14-09
DIFF002/ J14-08
DIFF004/ J14-05
DIFF008/ J14-11
18H
74193
13 DIFF001A/
13 DIFF002A/
13 DIFF004A/
13 DIFF008A/
DIFF016/ J14-10
DIFF032/ J14-06
DIFF064/ J14-07
DIFF128/
17H
74193
19H
74LS21
FULLSP/ J14-12
13 DIFF016A/
13 DIFF032A/
13 DIFF064A/
13 DIFF128A/
16 LDSP/
DIFF256/
DIFF512/
16H
74193
19 F
74LS27
DIFFZERO */14,16
18E
74LS04
10 DIFFZERO/ 16
16 SETDIF/
P5V
R42
1K
TP1
18E
74LS04
13 DIFF256A/
13 DIFF512A/
6 PU2
6 P5V
* INDICATES TWICE ON THIS PAGE
C
SC20013608
R
DWG SIZE
SHEET 14 OF 22
REV



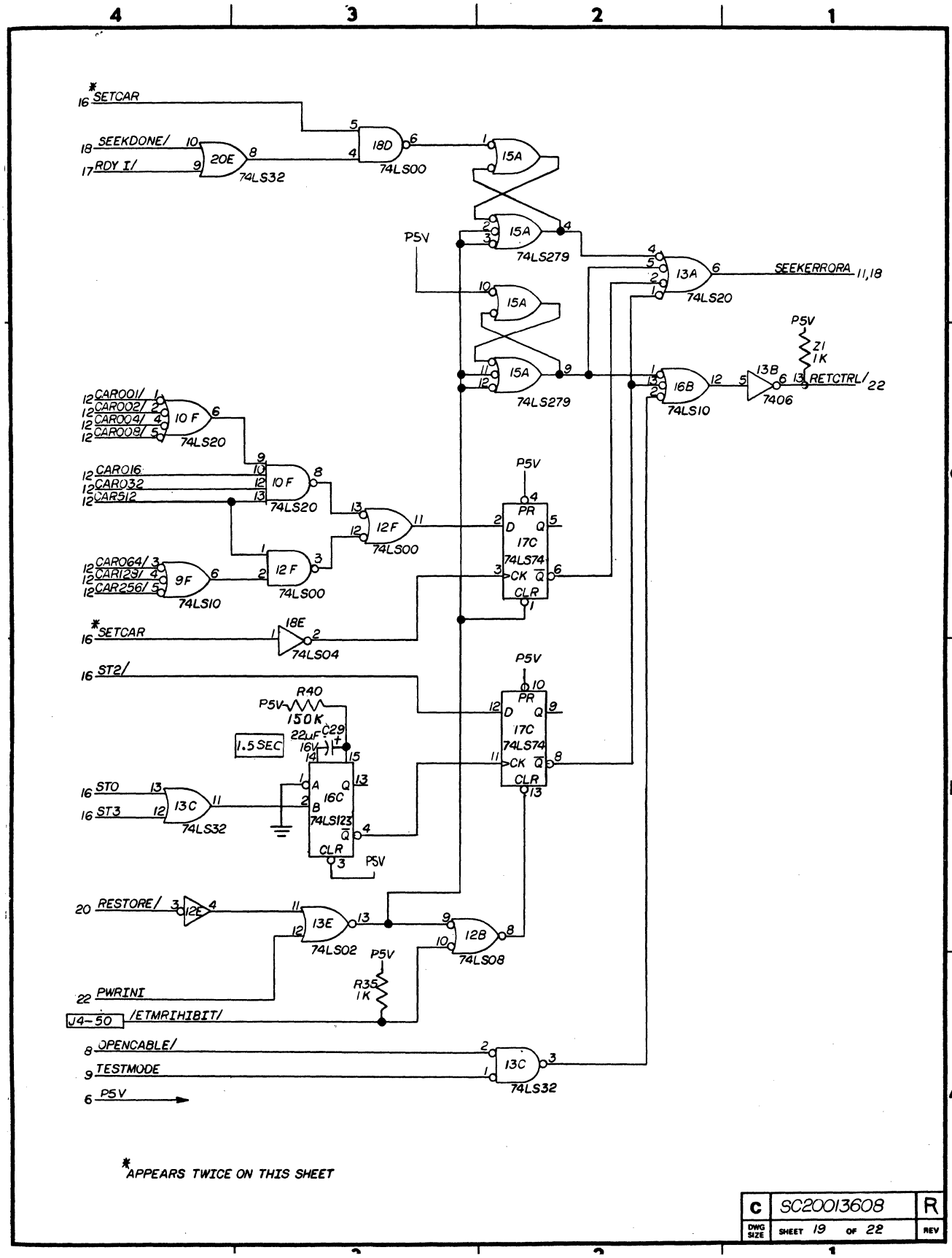
C SC20013609 R
DWG SIZE SHEET 15 OF 22 REV

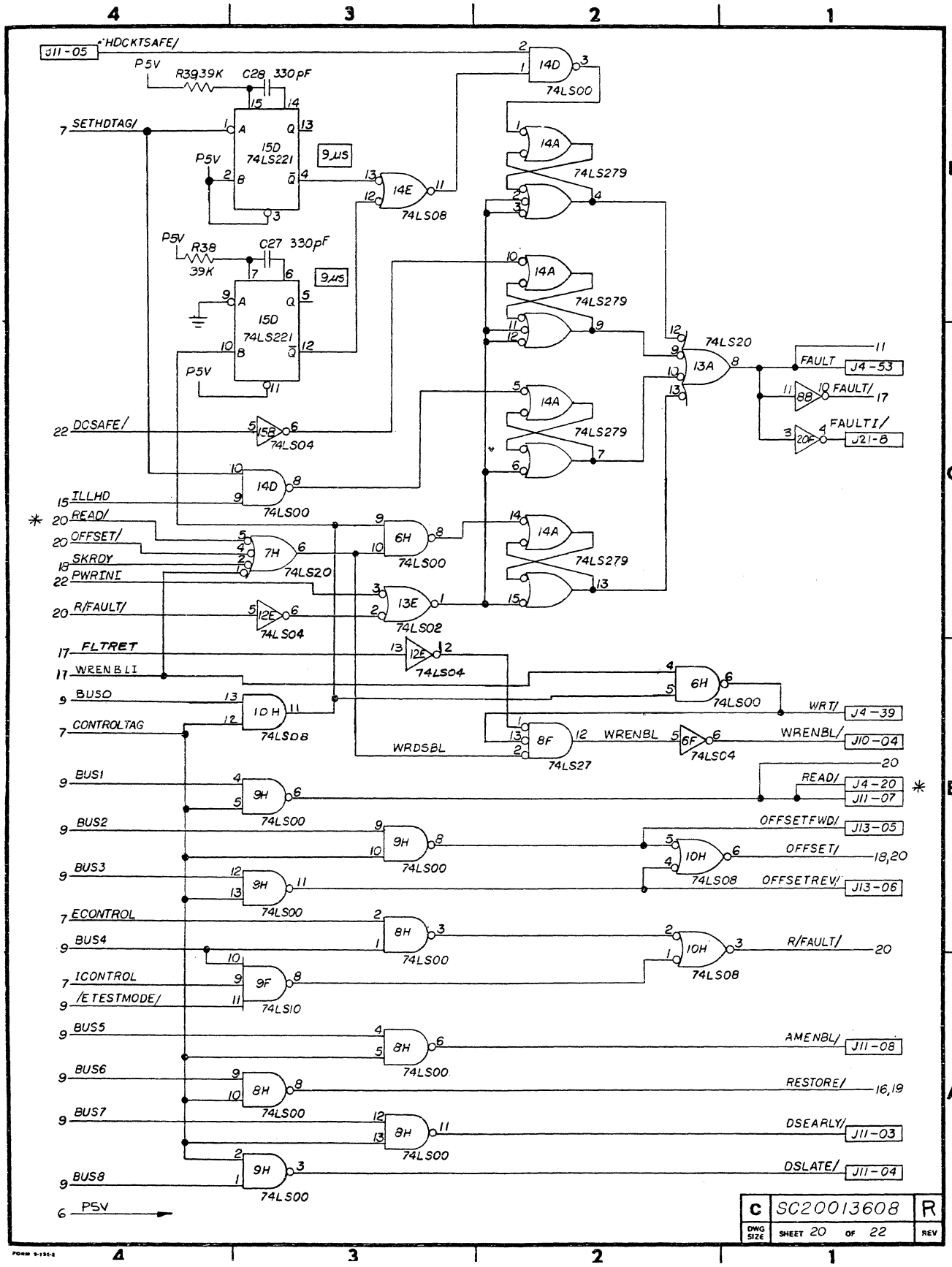

SEEKERROR/
SKSTRT
ST2
DIFFZERO/
DIFFZERO
ST3
ST1
MTHB/
RETHDS/
J13-3 OGB/
ST0/
4.8MHZ
OVF
SETCAR
PU2
CAROOI
P5V
RESTORE/
PWRINI/
SETCYLTAG
J12-7 4.8 MHZ
COUT
74LS21
74LS08
74LS32
74LS04
74LS02
74LS175
74376
74LS74
74LS00
SKINIL/ 12,15
SKSTRT 16
SETCAR 12,16,19
SETDIF/ 14
OVF 13,16
SKSTRT/ 18
ST3/ 14
ST3 J4-57 16,19
ST2/ 18,19
ST2 J4-54 16,17,18
ST1 J4-31 16
ST0 J4-30 19
ST0/ 16
OGB J4-32
TRKFL/ J4-07 J14-04
FWD/ J4-19 J14-02
REV/ J4-24 J14-03
IN 17
LDSP/ J4-34 J13-08 14
ODD/ J4-35 J13-09
* APPEARS TWICE ON THIS SHT.
C SC20013608 R
DWG SIZE SHEET 16 OF 22 REV

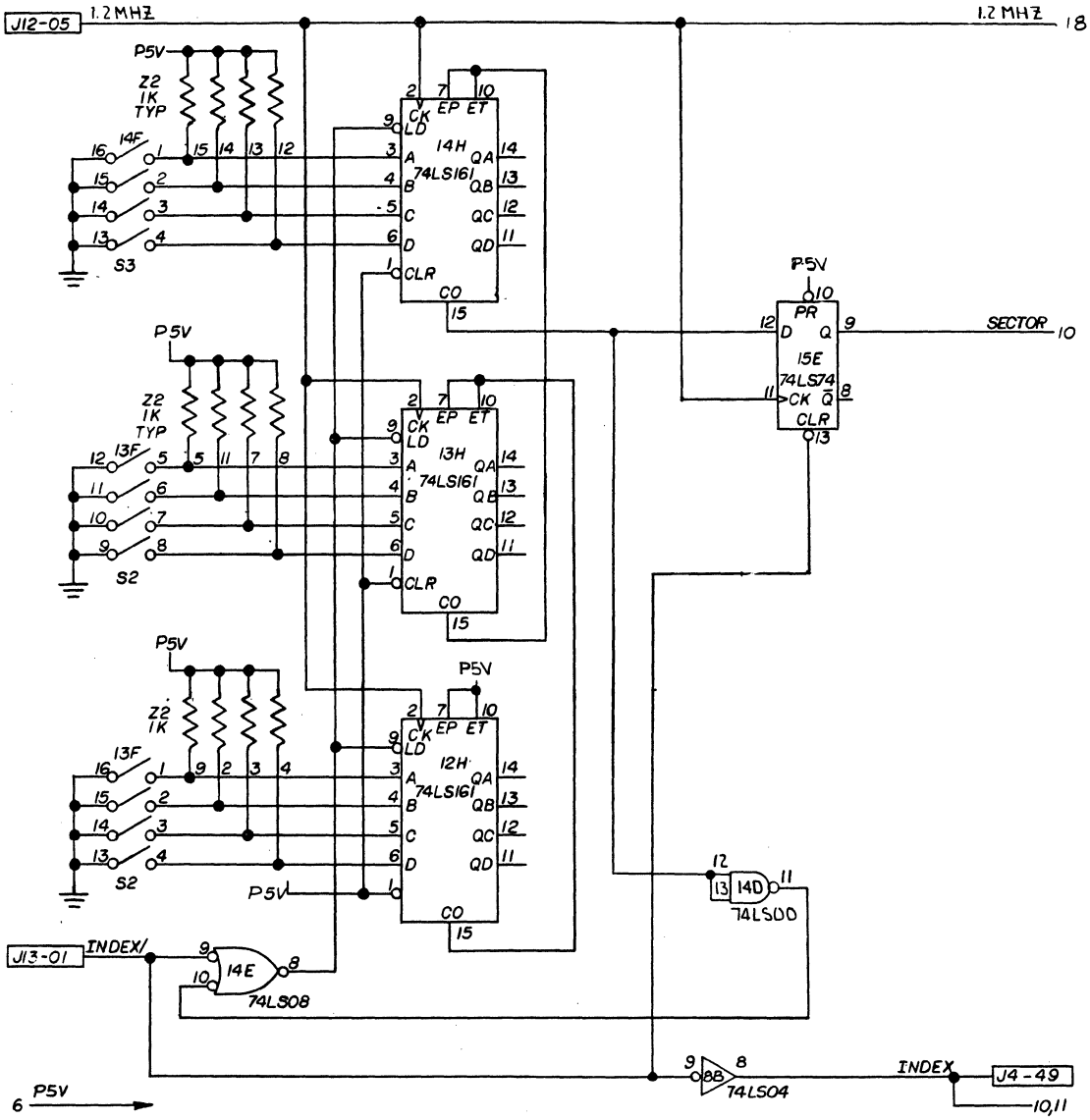

4
3
2
1
D
C
B
A
16 IN
14 DIFF001/
16F
74LS86
18E
74LS04
18D
74LS00
18C
74LS74
PR
CK
CLR
16 ST2
18D
74LS00
6 P5V
P5V
R44
4.3K
C39
330PF
J13-11 MTH/
J13-12 PTH/
16E
74LS14
17D
74LS08
20E
74LS32
+5V
19D
74LS22
C/DIFF/ 14
P5V
18E
74LS04
MTH3/ 16
7 CONTROL TAG
P5V
R46
1K
J21-06 WRDSBLSW/
18D
74LS00
20E
74LS32
15A
74LS279
WRENBLI 20
WRTPROT 10
18E
74LS04
P5V
R47
1K
20F
7406
WRENBLI
J21-03
P5V
R48
1K
22 RETHDS/
20 FAULT/
17D
74LS08
22 25SECTMR/
17D
74LS08
20F
7406
RDYI/
J21-04
19
RDY 11
FLTRET 20
C
SC20013608
R
DWG SIZE
SHEET 17 OF 22
REV



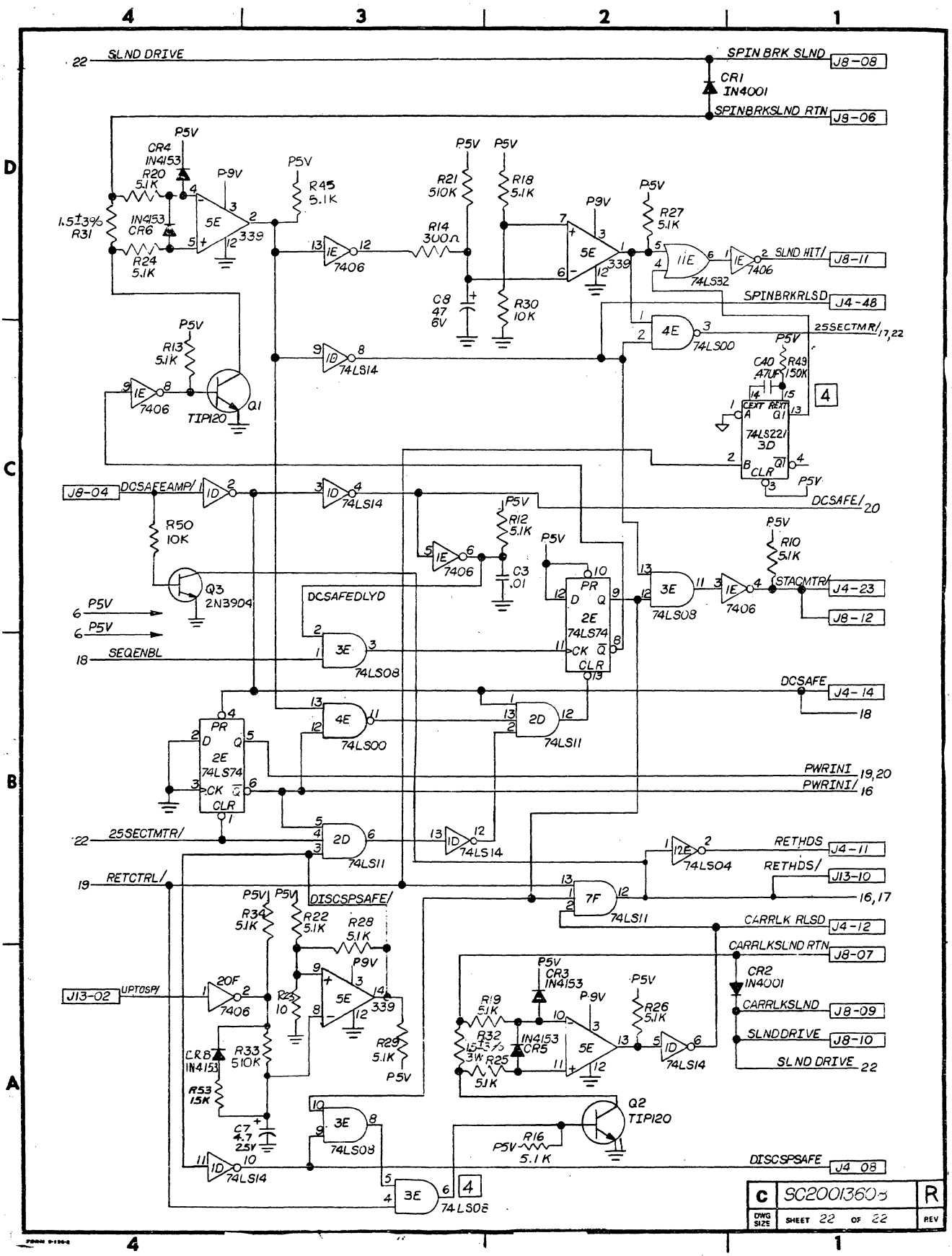
C	SC20013608	R
DWG SIZE	SHEET 18 OF 22	REV

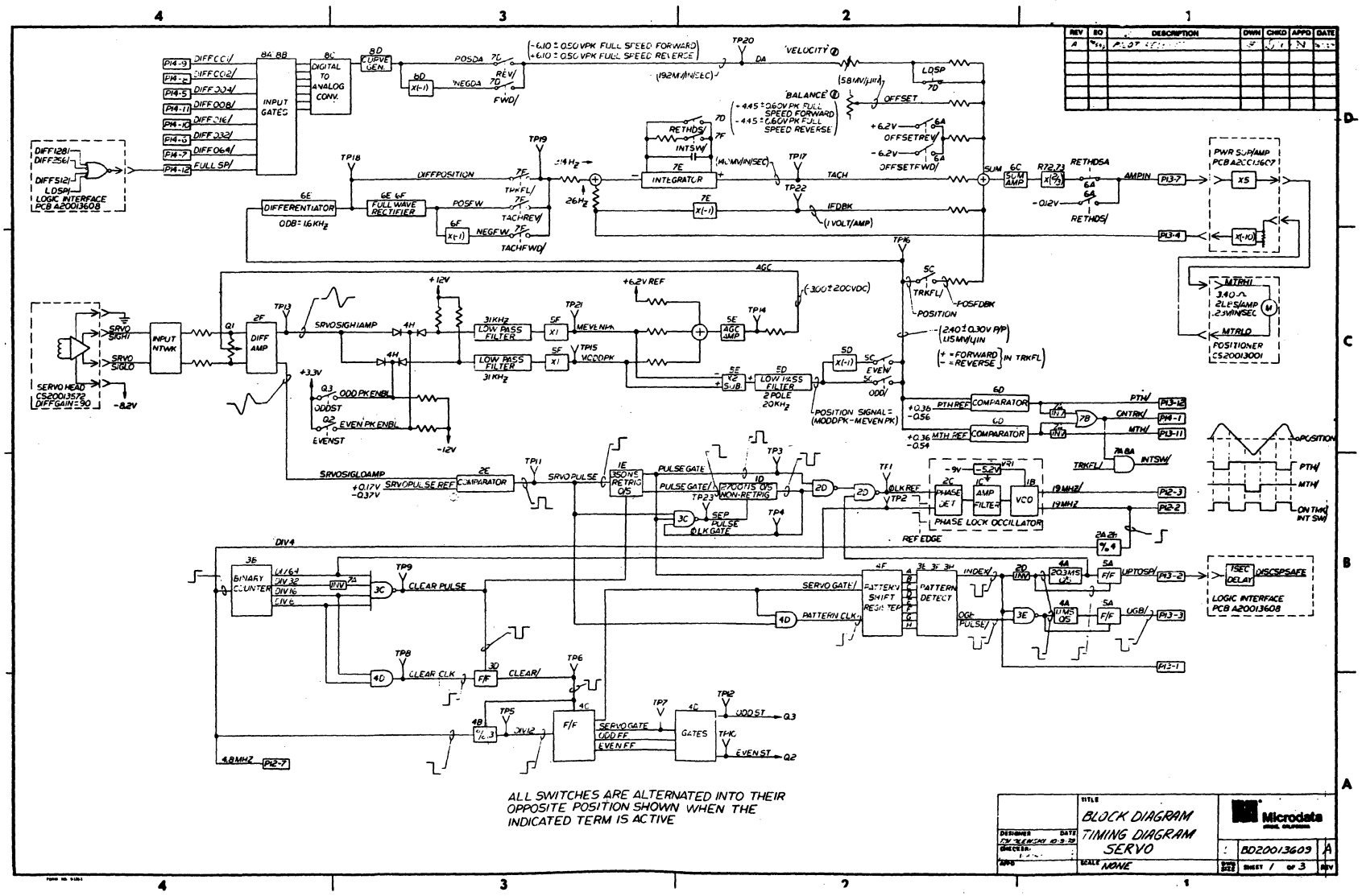

4
3
2
1
D
C
B
A
*SETCAR
SEEKDONE/
RDY I/
20E
74LS32
18D
74LS00
15A
74LS279
P5V
13A
74LS20
SEEKERRORA 11,18
Z1 1K
13B
7406
RETCTRL/ 22
16B
74LS10
CAR001/
CAR002/
CAR004/
CAR008/
10 F
74LS20
CAR016
CAR032
CAR512
12F
74LS00
CAR064/
CAR128/
CAR256/
9F
74LS10
17C
74LS74
PR
D
CK
CLR
18E
74LS04
ST2/
R40
150K
1.5 SEC
22uF
C29
16C
74LS123
STO
ST3
13C
74LS32
RESTORE/
12E
13E
74LS02
12B
74LS08
R35
1K
PWRINI
J4-50
/ETMRIHIBIT/
OPENCABLE/
TESTMODE
P5V
*APPEARS TWICE ON THIS SHEET
C
SC20013608
R
DWG SIZE
SHEET 19 OF 22
REV

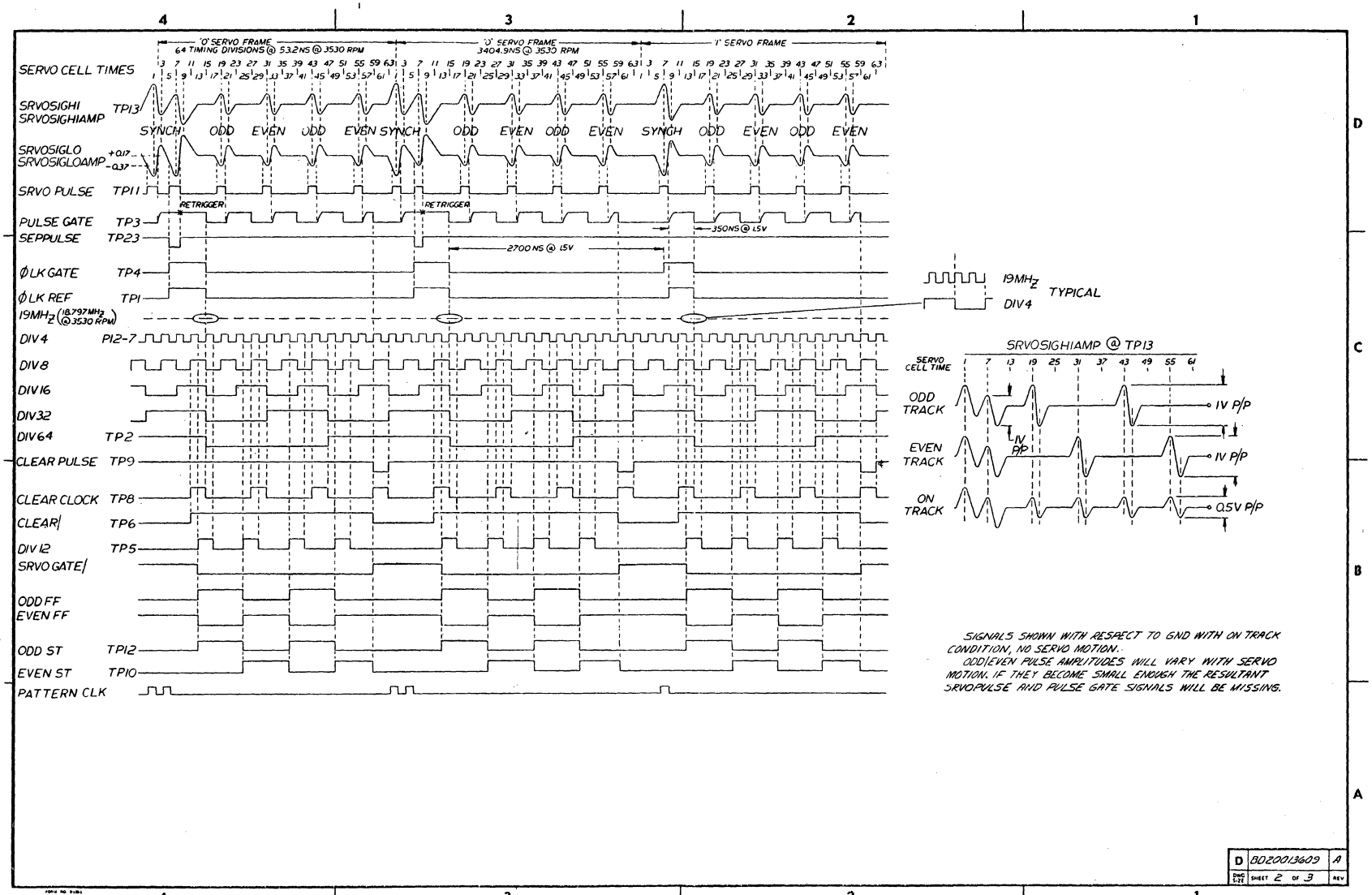

4
3
2
1
J11-05 *HDCKTSAFE/
P5V
R39 39K
C28 330pF
15D 74LS221
9µs
7 SETHDTAG/
14E 74LS08
14D 74LS00
14A 74LS279
R38 39K
C27 330pF
15B 74LS04
22 DCSAFE/
14D 74LS00
15 ILLHD
20 READ/
20 OFFSET/
19 SKRDY
22 PWRINI
7H 74LS20
6H 74LS00
13E 74LS02
20 R/FAULT/
12E 74LS04
17 FLTRET
17 WRENBLI
9 BUSO
7 CONTROLTAG
10H 74LS08
WRDSBL
8F 74LS27
WRENBL
6F 74LS04
WRT/ J4-39
WRENBL/ J10-04
9 BUS1
9H 74LS00
READ/ J4-20 J11-07
9 BUS2
OFFSETFWD/ J13-05
9 BUS3
OFFSET/ 18,20
OFFSETREV/ J13-06
7 ECONTROL
8H 74LS00
9 BUS4
10H 74LS08
R/FAULT/ 20
7 ICONTROL
9F 74LS10
9 /ETESTMODE/
9 BUS5
AMENBL/ J11-08
9 BUS6
RESTORE/ 16,19
9 BUS7
DSEARLY/ J11-03
9 BUS8
DSLATE/ J11-04
6 P5V
74LS20
13A
FAULT J4-53
88 FAULT/ 17
20F FAULTI/ J21-8
C SC20013608 R
DWG SIZE
SHEET 20 OF 22
REV
D
C
B
A

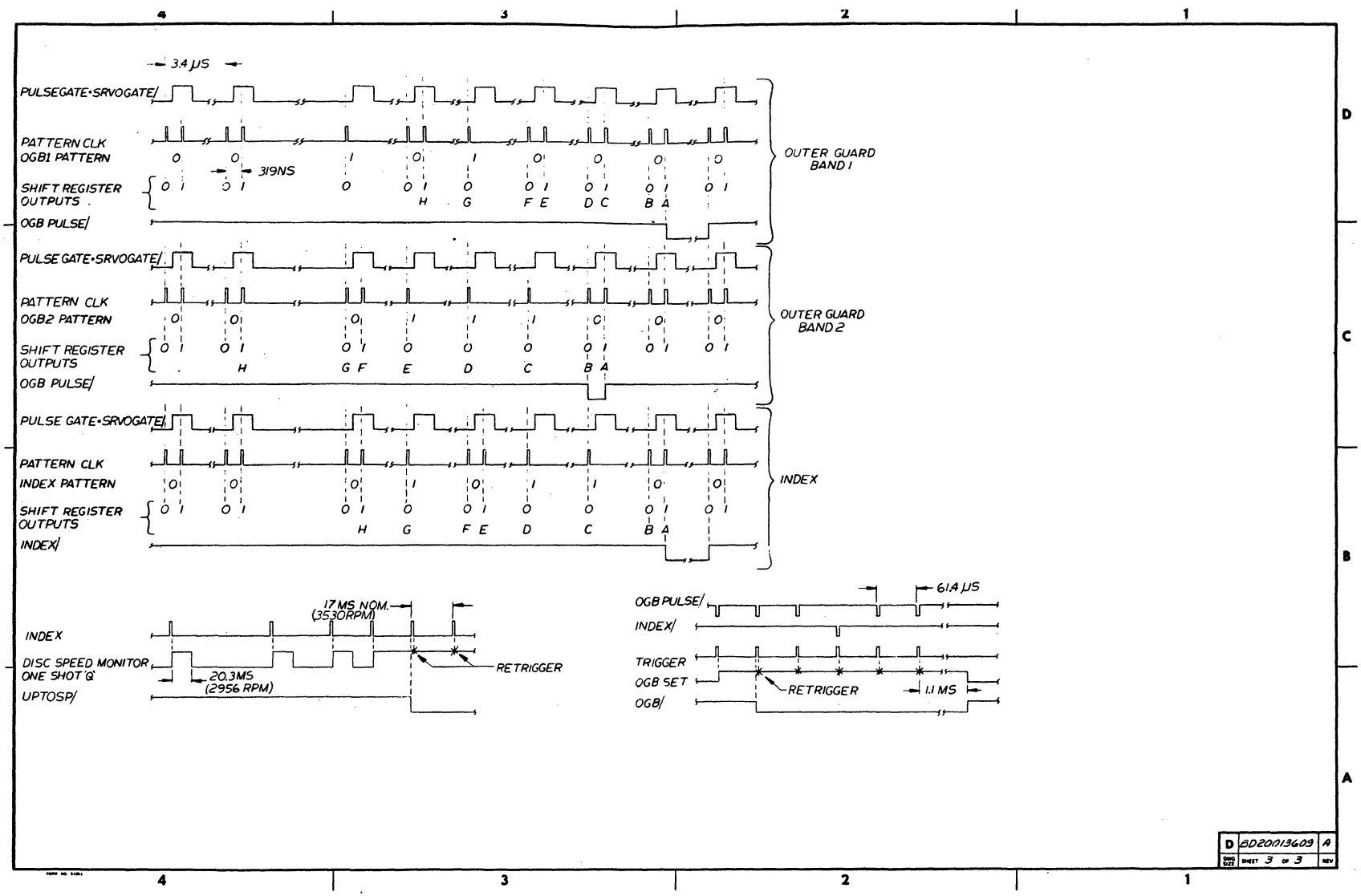


C	SC20013608	R
DWG SIZE	SHEET 21 OF 22	REV


SLND DRIVE
SPIN BRK SLND
J8-08
CR1
IN4001
SPINBRKSLND RTN
J8-06
P5V
CR4
IN4153
R20
5.1K
P9V
R45
5.1K
1.5±3%
R31
IN4153
CR6
R24
5.1K
5E
339
7406
R21
510K
R14
300Ω
R18
5.1K
R27
5.1K
SLND HIT/
J8-11
74LS32
C8
47
6V
R30
10K
SPINBRKRLSD
J4-48
25SECTMR/
17,22
4E
74LS00
C40
.47UF
R49
150K
CEXT REXT
74LS221
3D
CLR
R13
5.1K
TIP120
Q1
74LS14
J8-04
DCSAFEAMP/
DCSAFE/
20
R50
10K
Q3
2N3904
R12
5.1K
C3
.01
R10
5.1K
STACMTR/
J4-23
J8-12
DCSAFEDLYD
SEQENBL
18
3E
74LS08
2E
74LS74
PR
CK
CLR
DCSAFE
J4-14
18
4E
2D
74LS11
PWRINI
19,20
PWRINI/
16
25SECTMTR/
22
RETCTRL/
19
DISCSPSAFE/
R34
5.1K
R22
5.1K
R28
5.1K
R29
5.1K
R23
10
20F
UPTOSP/
J13-02
CR8
IN4153
R33
510K
R53
15K
C7
4.7
25V
7F
74LS04
RETHDS
J4-11
RETHDS/
J13-10
16,17
CARRLK RLSD
J4-12
CARRLKSLND RTN
J8-07
CR2
IN4001
CARRLKSLND
J8-09
SLNDDRIVE
J8-10
SLND DRIVE
22
CR3
IN4153
R19
5.1K
R32
15Ω
3W
R25
5.1K
CR5
IN4153
R26
5.1K
Q2
TIP120
R16
5.1K
DISCSPSAFE
J4 08
C
SC2001360-
R
DWG SIZE
SHEET 22 OF 22
REV

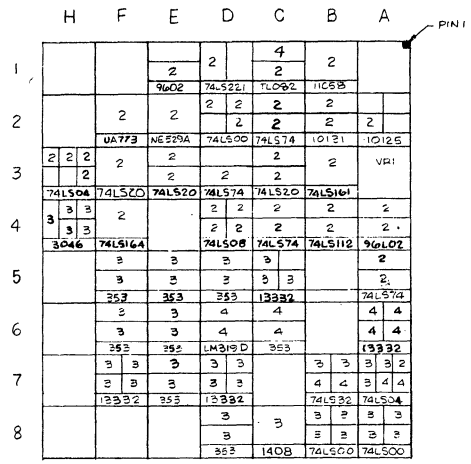

DIFFCOV
DIFFCOG
DIFFDO4
DIFFDO8
DIFF016
DIFF032
DIFF064
FULL SP
INPUT GATES
DIGITAL TO ANALOG CONV.
CURVE GEN.
POSDA
NEGDA
REV
FWD
(-6.10 ± 0.50 VPK FULL SPEED FORWARD)
(+6.10 ± 0.50 VPK FULL SPEED REVERSE)
VELOCITY
(192MV/INSEC)
(581MV/IN/SEC)
LOSP
OFFSET
BALANCE
(-4.45 ± 0.60 VPK FULL SPEED FORWARD)
(-4.45 ± 0.60 VPK FULL SPEED REVERSE)
RETHDS
INTSW
INTEGRATOR
(40 MV/MIN/SEC)
TACH
OFFSETREV
OFFSETFWD
SUM
SUM AMP
R72,73
RETHDSA
AMPIN
PWR SUP/AMP PCB A2CC13607
XS
MTRHI
MTRLO
340Ω
2 LBS/AMP
.23V/IN/SEC
POSITIONER CS20013001
DIFF128
DIFF256
DIFFS12
LDSP
LOGIC INTERFACE PCB A20013608
DIFFERENTIATOR
ODB=16KHz
FULL WAVE RECTIFIER
DIFFPOSITION
POSFW
NEGFW
TACHREV
TACHFWD
IFDBK
(1 VOLT/AMP)
26Hz
SERVO SIGHI
SERVO SIGLO
SERVO HEAD CS20013629
DIFF GAIN=90
INPUT NTWK
DIFF AMP
SRVOSIGHIAMP
LOW PASS FILTER
31KHz
MEVENHA
VCODPK
AGC AMP
(-300 ± 20CVDC)
TRKFL
POSITION
(2.40 ± 0.30V P/P)
(115MV/MIN)
(+ = FORWARD)
(- = REVERSE)
IN TRKFL
2 POLE
20KHz
POSITION SIGNAL = (MODDPK-MEVENPK)
ODDPKENBL
EVENPKENBL
ODDST
EVENST
COMPARATOR
PTHREF
MTHREF
PTH
MTH
ONTRK
INTSW
SRVOSIGLOAMP
SRVOPULSEREF
SRVOPULSE
PULSE GATE
PULSE GATE/
74LS123 DUAL NON-RETRIG
SEP PULSE @LK GATE
@LK REF
PHASE LOCK OCCILLATOR
PHASE DET
AMP FILTER
VCO
19MHz
REF EDGE
DIV4
BINARY COUNTER
DIV 64
DIV 32
DIV 16
DIV 8
CLEAR PULSE
CLEAR CLK
CLEAR/
F/F
SERVOGATE
ODDFF
EVENFF
GATES
THK
ODDST
EVENST
4.8MHz
SERVOGATE/
PATTERN SHIFT REGISTER
PATTERN DETECT
PATTERN CLK
INDEX
OGPULSE/
203MS
11MS
UPTOSP/
UGB/
1SEC DELAY
XSCSPSAFE
LOGIC INTERFACE PCB A20013608
ALL SWITCHES ARE ALTERNATED INTO THEIR OPPOSITE POSITION SHOWN WHEN THE INDICATED TERM IS ACTIVE
BLOCK DIAGRAM
TIMING DIAGRAM
SERVO
Microdata
BD20013609
SHEET 1 OF 3


'0' SERVO FRAME
64 TIMING DIVISIONS @ 5.32 NS @ 3530 RPM
'3' SERVO FRAME
3404.9 NS @ 3530 RPM
'1' SERVO FRAME
SERVO CELL TIMES
SRVOSIGHI
SRVOSIGHIAMP TP13
SYNCH ODD EVEN ODD EVEN SYNCH ODD EVEN ODD EVEN SYNCH ODD EVEN ODD EVEN
SRVOSIGLO
SRVOSIGLOAMP +0.17 -0.37
SRVO PULSE TP11
RETRIGGER
PULSE GATE TP3
SEPPULSE TP23
350NS @ 1.5V
2700 NS @ 1.5V
ØLK GATE TP4
ØLK REF TP1
19MHZ (18.797MHz @ 3530 RPM)
DIV4 P12-7
DIV8
DIV16
DIV32
DIV64 TP2
CLEAR PULSE TP9
CLEAR CLOCK TP8
CLEAR/ TP6
DIV12 TP5
SRVO GATE/
ODD FF
EVEN FF
ODD ST TP12
EVEN ST TP10
PATTERN CLK
19MHZ
DIV4
TYPICAL
SRVOSIGHIAMP @ TP13
SERVO CELL TIME
ODD TRACK
EVEN TRACK
ON TRACK
1V P/P
0.5V P/P
SIGNALS SHOWN WITH RESPECT TO GND WITH ON TRACK CONDITION, NO SERVO MOTION.
ODD/EVEN PULSE AMPLITUDES WILL VARY WITH SERVO MOTION. IF THEY BECOME SMALL ENOUGH THE RESULTANT SRVOPULSE AND PULSE GATE SIGNALS WILL BE MISSING.
D 8020013609 A
SHEET 2 OF 3


3.4 µS
PULSEGATE•SRVOGATE/
PATTERN CLK
OGB1 PATTERN
319NS
SHIFT REGISTER OUTPUTS
OGB PULSE/
OUTER GUARD BAND 1
PULSE GATE•SRVOGATE/
PATTERN CLK
OGB2 PATTERN
SHIFT REGISTER OUTPUTS
OGB PULSE/
OUTER GUARD BAND 2
PULSE GATE•SRVOGATE/
PATTERN CLK
INDEX PATTERN
SHIFT REGISTER OUTPUTS
INDEX/
INDEX
17 MS NOM. (3530RPM)
DISC SPEED MONITOR ONE SHOT 'Q'
20.3MS (2956 RPM)
UPTOSP/
RETRIGGER
OGB PULSE/
61.4 µS
INDEX/
TRIGGER
OGB SET
RETRIGGER
1.1 MS
OGB/
D
BD20013609
A
SHEET 3 OF 3

81 1091B

99-9



COMPONENTS USED	LAST REF DES USED	REF DES NOT USED
CAPACITORS	C48	C5, 25, 33 34, 37, 38
DIODES	CR16	CR3
RESISTORS	R111	R13, 21, 106, 107
TRANSISTORS	Q4	
VOLTAGE REG	VR-1	
TEST POINTS	TP-23	
INDUCTORS	L2	

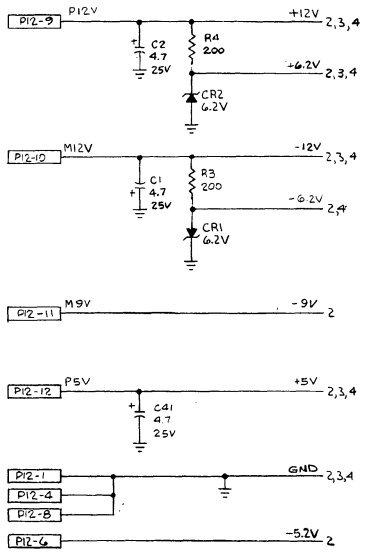
REV	EO	ZONE	DESCRIPTION	DRN	CHKD	APPD	DATE
AX	B050		PROTO RELEASE	BL	MP	RTS	4-24-74
A	A935		PILOT RELEASE	EH	MP	RTS	4/24/74
B	P0110		INCORP E.O.	CK	J.J.C.	CAN	5-15-74
C	P0125		INCORP E.O	CK	J.J.C.	CAN	5-15-74
D	P0435A		INCORP E.O.	CK	RR	CAN	7-23-74
E	P0508		INCORPORATE E.O.	MLM	RR	CAN	7/1/74
F	P0588		INCORPORATE E.O.	MLM	RR	CAN	7/1/74
G	P0554		INCORPORATE E.O.	MLM	RR	CAN	7/19/74
H	P0599		INCORPORATE E.O.	FF	W.G.	CN	8-13-74
J	P0628A		INCORP E.O.	A.K.	J.C.	CAN	9/6/74
K	P0920		INCORP E.O.	W.G.	CAN	CN	12-2-74
L	P0967		INCORP E.O.	M.C.	J.W.	CAN	4/1/80
M	P0581		NEW RELEASE	H.B.		CAN	7/16/80
N	P1073		INCORP E.O.	M.C.		CAN	7-7-80
P	P1138A		INCORP E.O.	M.C.		CAN	10-30-80
R	P1198A		INCORP E.O.	M.C.		CAN	12-29-80

PIN NO	P12	SH NO.
1	GND	1
2	19 MHZ	2
3	19 MHZ/	2
4	GND	1
5	1.2 MHZ	2
6	MS2V	1
7	4.8 MHZ	2
8	GND	1
9	P12V	1
10	M12V	1
11	M9V	1
12	P 5V	1

PIN NO.	P13	SH NO.
1	INDEX/	2
2	UPTØSP/	2
3	ØGB/	2
4	MTRI	3
5	ØFFSETFWD/	4
6	ØFFSETREV/	4
7	AMPIN	4
8	LDSP/	3
9	ØDD/	3
10	RETHDS/	4
11	MTH/	4
12	PTH/	4

PIN NO	P14	SH NO.
1	ØNTRK/	4
2	FWD/	3
3	REV/	3
4	TRKFL/	3
5	DIFFØØ4/	3
6	DIFFØ32/	3
7	DIFFØ64/	3
8	DIFFØØ2/	3
9	DIFFØØ1/	3
10	DIFFØ16/	3
11	DIFFØØ8/	3
12	FULLSP/	3

PIN NO.	J16	SH NO.
1	GND	2
2	GND	2
3	GND	2
4	GND	2
5	SRVØSIGLØ	2
6	SRVØSIGHI	2
7	GND	2
8	MB.2V	2
9	GND	2
10	MB.2V	2



IC VOLTAGE CHART		
VOLTAGE	PIN NO.	IC REFERENCE DESIGNATION
+12	12	5C, 6A, 7D, 7F
+5V	14	2D, 3D, 3E, 3F, 3H, 4C, 4D, 5A, 3C, 7A, 7B, 8A, 8B
	16	1D, 1E, 4A, 4B
GND	1	2B
	4	5C, 6A, 7D, 7F
	16	2B
	7	2C, 2D, 3D, 3E, 3F, 3H, 4G, 4D, 5A, 3C, 7A, 7B, 8A, 8B
	8	1D, 1E, 3B, 4A, 4B
-5.2V	8	2B
-12V	5	5C, 6A, 7D, 7F

6. FOR BLOCK DIAGRAM · TIMING DIAGRAM SEE BD20013609.
5. ALL DIODES ARE IN4153.
4. ALL 0.1 CAPACITORS ARE +80%/-20%, 25V.
3. ALL CAPACITORS ARE ± 10%, 50V OR HIGHER, GIVEN IN MFD'S.
2. ALL RESISTORS ARE ± 5%, 1/4 W, GIVEN IN OHMS.
1. INTERPRET DRAWING PER MIL-STD 100.

NOTES: UNLESS OTHERWISE SPECIFIED

SC20013609
R

UNINCORPORATED ENGINEERING ORDERS

REFLEX 20013609 NEXT ASSY APPLICATION USED ON

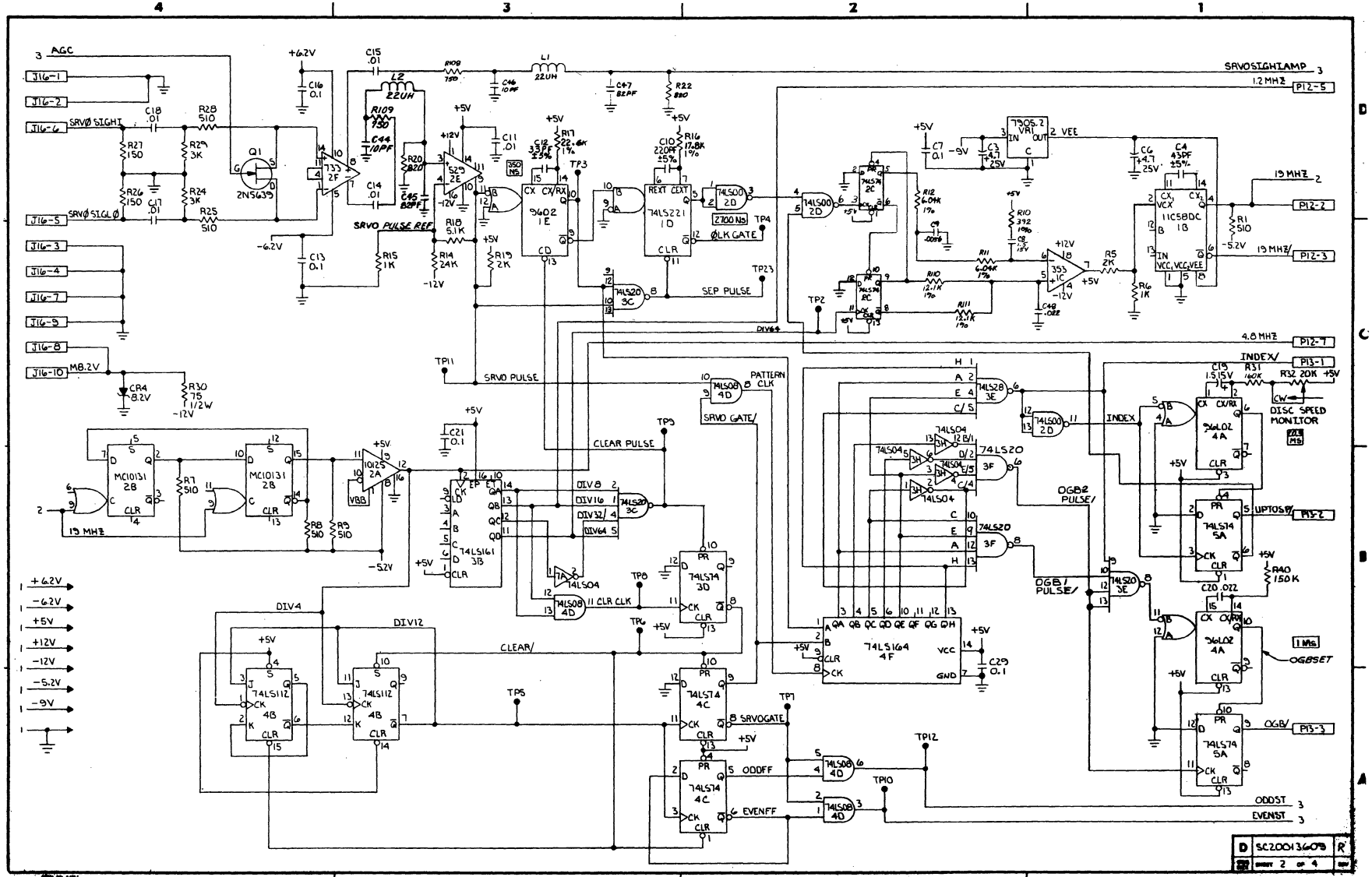
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES .XX ± .02 TOLERANCES .XXX ± .010 TOLERANCES ANGLES ±1° MATERIAL FINISH

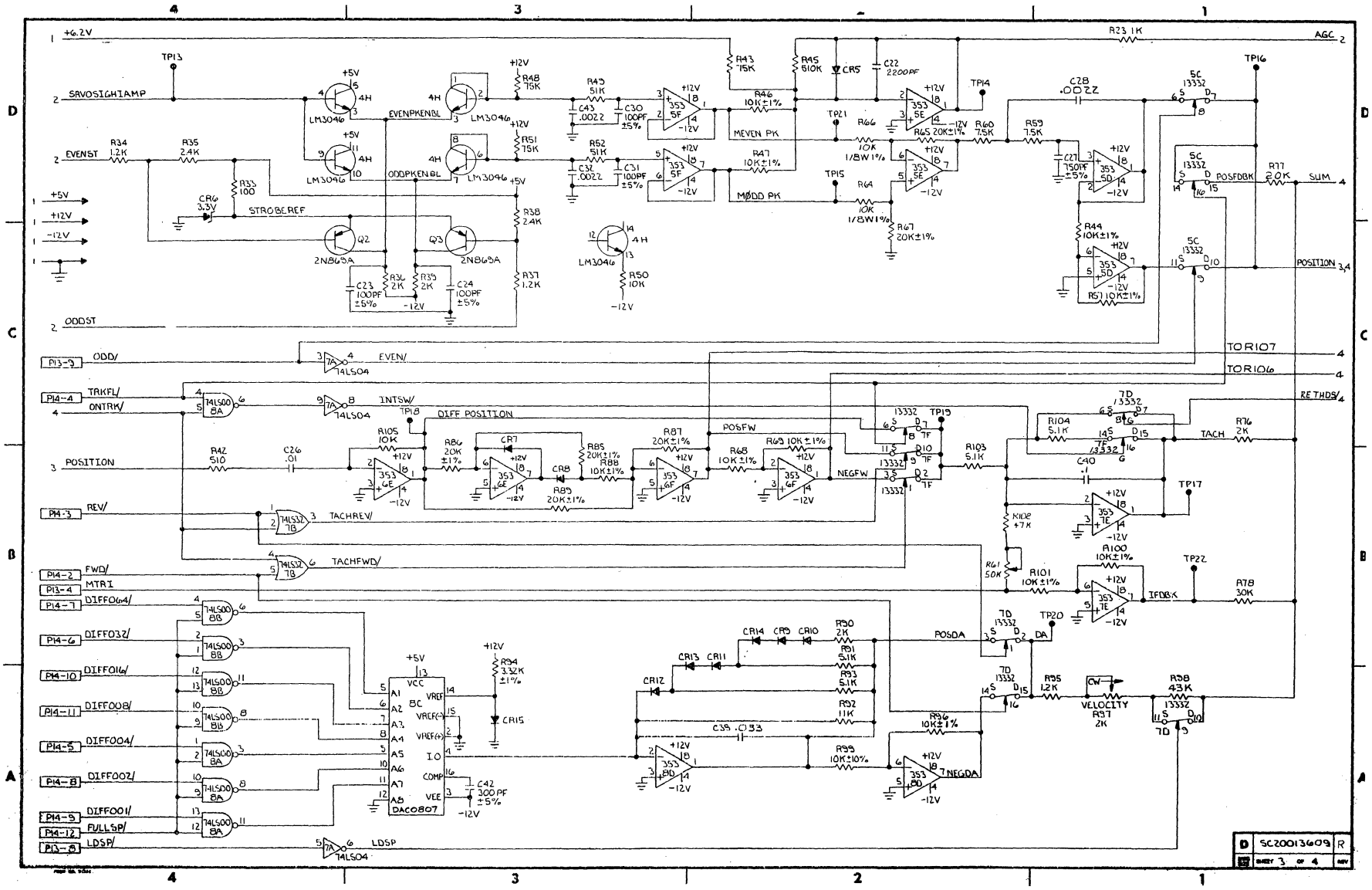
DRAFTSMAN E. HUSTWIT DATE 5-15-74
CHECKED 4-24-74
ENGINEER
APPD
APPD 4-24-74
APPD
APPD

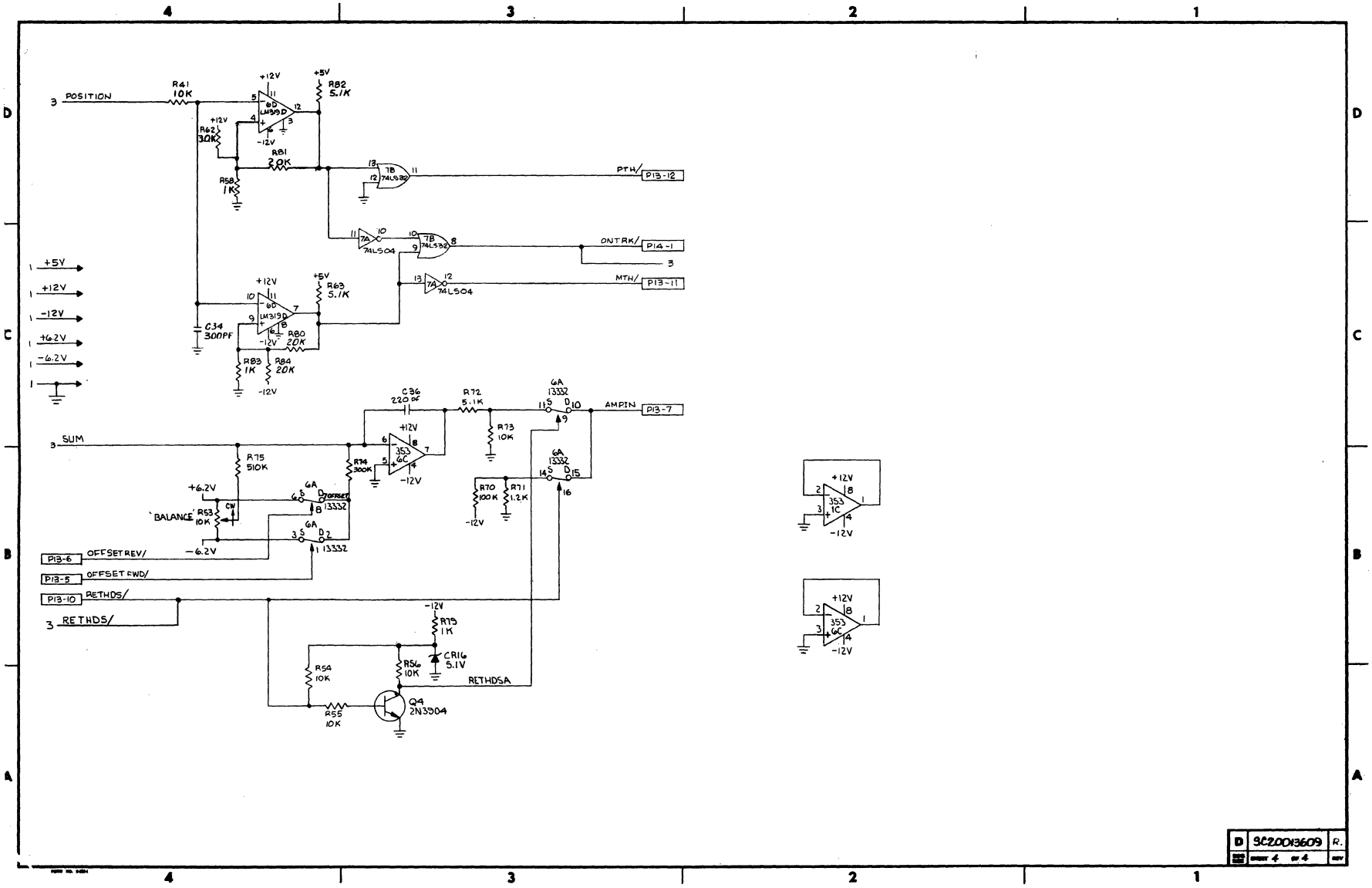
TITLE: PC B SCHEMATIC - SERVO

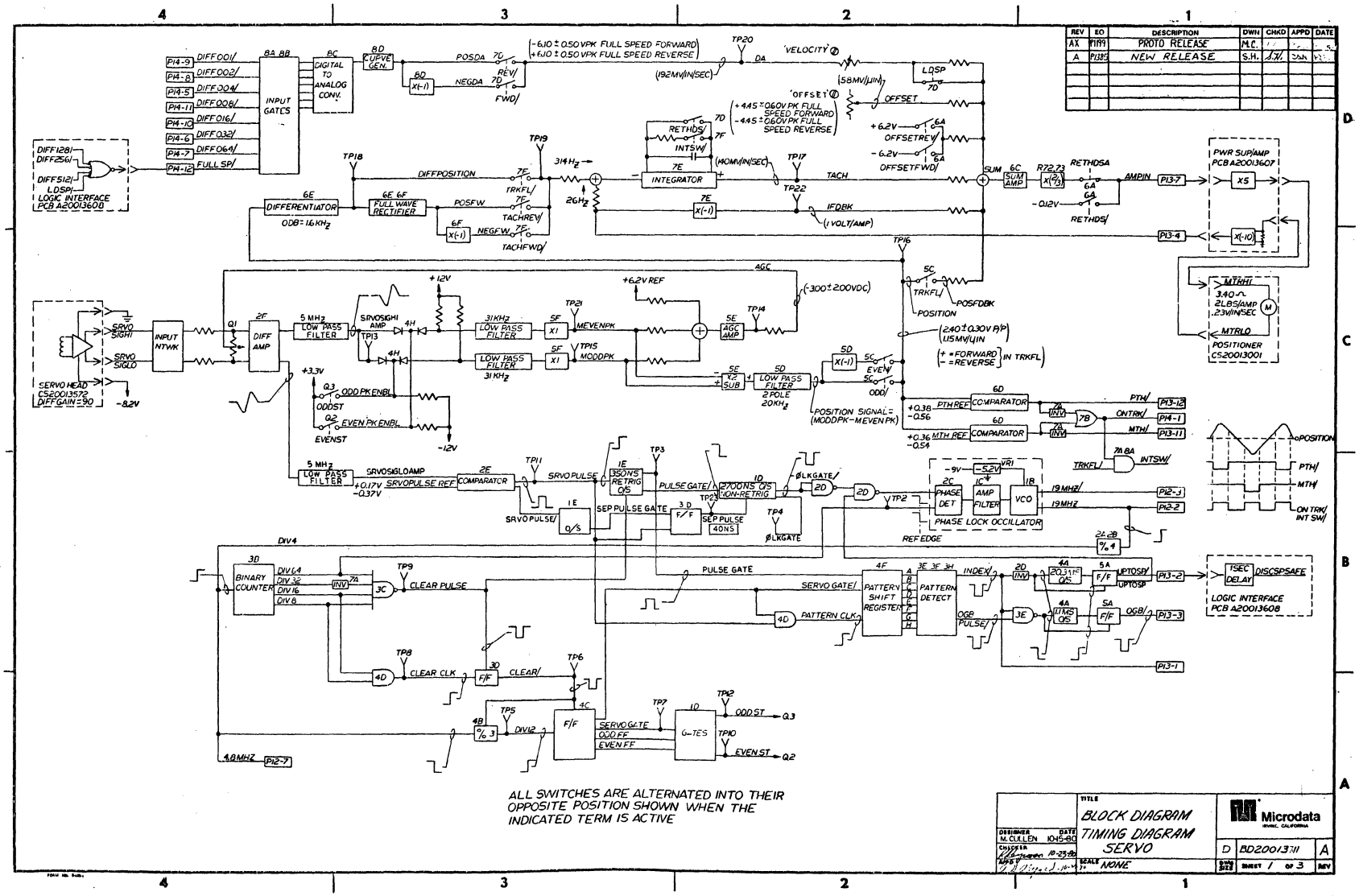
Microdata IRVINE, CALIFORNIA

SCALE NONE IDENT CODE 52936 DWG SIZE D SC20013609 REV R SHEET 1 OF 4


AGC
SRVOSIGHIAMP
1.2 MHZ
P12-5
SRVØ SIGHT
SRVØ SIGLØ
SRVO PULSE REF
SEP PULSE
ØLK GATE
19 MHZ
P12-2
P12-3
4.8 MHZ
P12-7
INDEX/
P13-1
DISC SPEED MONITOR
UPTOSS/
P13-2
OGBSET
OGB/
P13-3
SRVO PULSE
SRVO GATE/
CLEAR PULSE
PATTERN CLK
CLEAR/
DIV4
DIV12
ODDST
EVENST
ODDFF
EVENFF
SRVOGATE
OGBZ PULSE/
OGB1 PULSE/
D SC2001360B R
SHEET 2 OF 4


+6.2V
SRVOSIGHIAMP
EVENST
ODDST
STROBEREF
EVENPKENBL
ODDPKENBL
MEVEN PK
MODD PK
AGC
SUM
POSITION
POSFDBK
TACH
IFDBK
VELOCITY
DIFF POSITION
POSFW
NEGFW
POSDA
NEGDA
TACHREV/
TACHFWD/
LDSP
DAC0807
LM3046
2N869A
74LS00
74LS04
74LS32
13332
353
ODD/
EVEN/
TRKFL/
ONTRK/
INTSW/
POSITION
REV/
FWD/
MTRI
DIFF064/
DIFF032/
DIFF016/
DIFF008/
DIFF004/
DIFF002/
DIFF001/
FULLSP/
LDSP/
TO R107
TO R106
RETHDS/
SC20013609
SHEET 3 OF 4


POSITION
R41 10K
+12V
+5V
R82 5.1K
R62 30K
R61 20K
R58 1K
PTH/
P13-12
ONTRK/
P14-1
MTH/
P13-11
+5V
+12V
-12V
+6.2V
-6.2V
C34 300PF
R63 5.1K
R80 20K
R83 1K
R84 20K
C36 220 PF
R72 5.1K
R73 10K
AMPIN
P13-7
SUM
R75 510K
R74 300K
R70 100K
R71 1.2K
BALANCE
R53 10K
CW
OFFSET
P13-6 OFFSETREV/
P13-5 OFFSET FWD/
P13-10 RETHDS/
RETHDS/
R79 1K
CR16 5.1V
R54 10K
R56 10K
R55 10K
Q4 2N3904
RETHDSA
D 9C20013609 R.
SHEET 4 OF 4



ALL SWITCHES ARE ALTERNATED INTO THEIR OPPOSITE POSITION SHOWN WHEN THE INDICATED TERM IS ACTIVE

REV	EO	DESCRIPTION	DWN	CHKD	APPD	DATE
AX	P1199	PROTO RELEASE	M.C.			
A	P1385	NEW RELEASE	S.H.	J.H.	JWH	1/11

TITLE: BLOCK DIAGRAM TIMING DIAGRAM SERVO

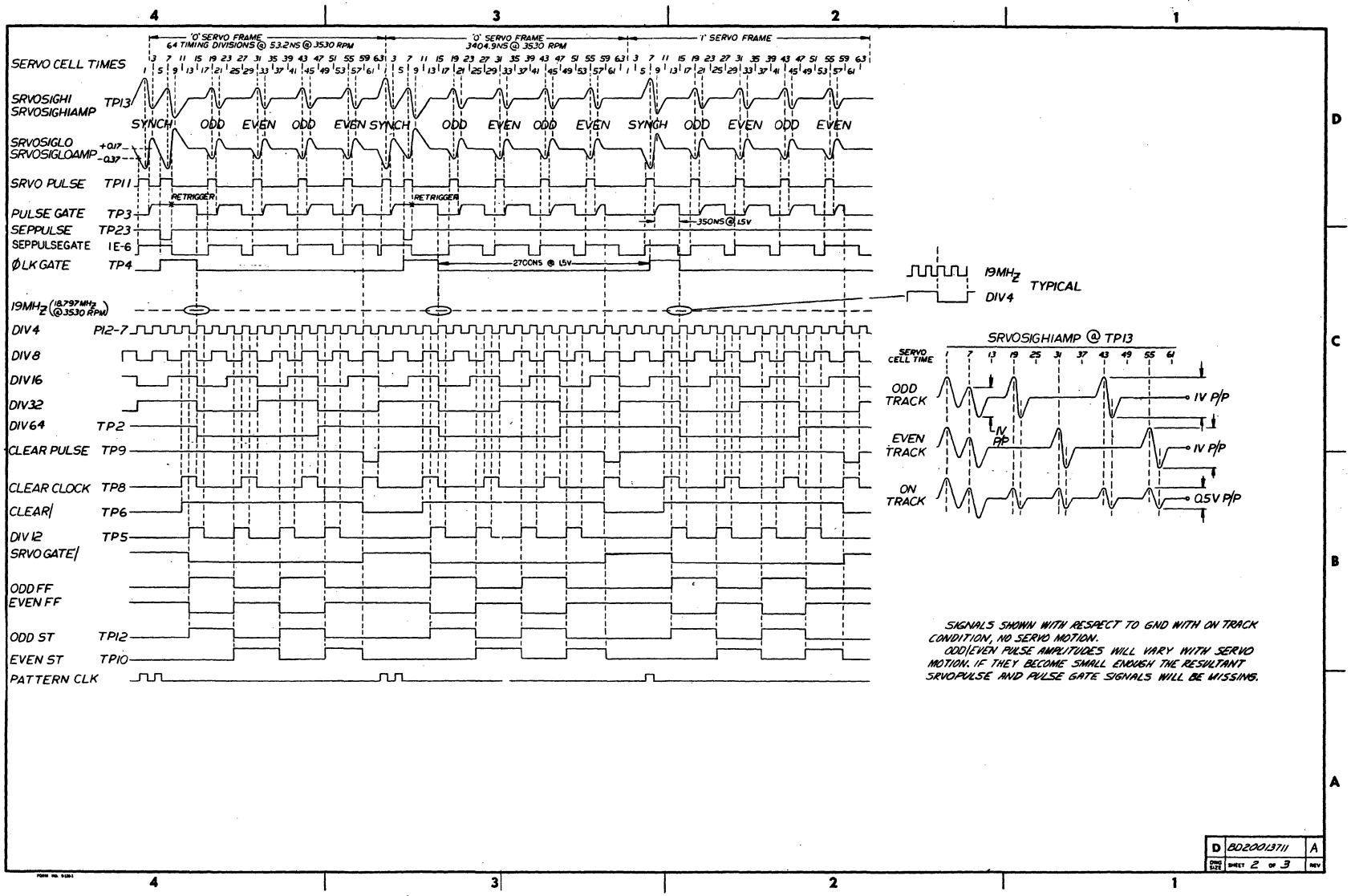
DESIGNER M. CULLEN DATE 1045-80

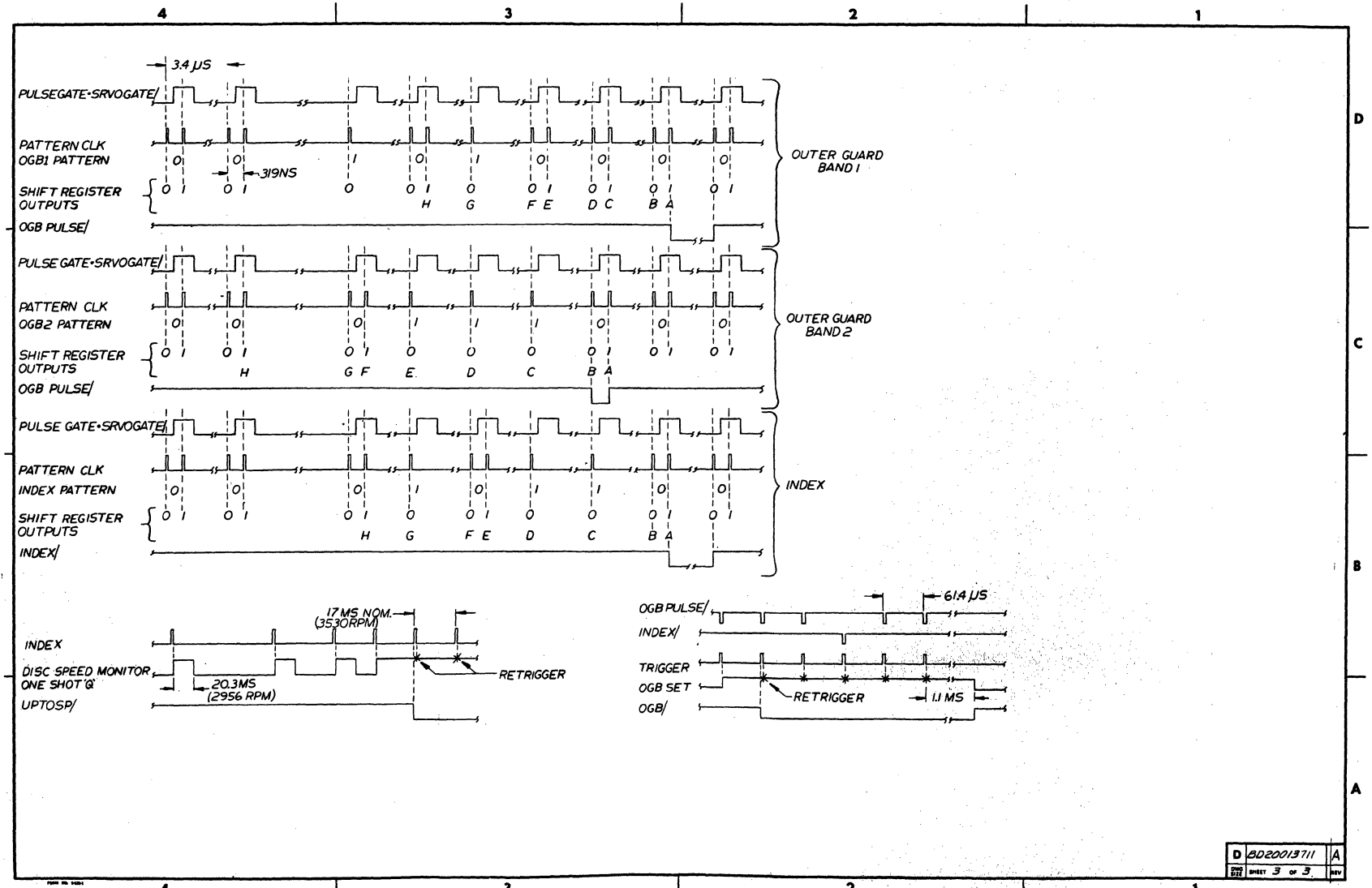
SCALE NONE

Microdata IRVINE, CALIFORNIA

D | BD20013711 | A

SHEET 1 OF 3

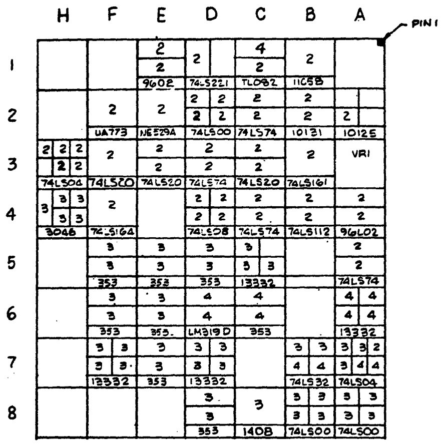

'0' SERVO FRAME
64 TIMING DIVISIONS @ 53.2NS @ 3530 RPM
'0' SERVO FRAME
3404.9NS @ 3530 RPM
'1' SERVO FRAME
SERVO CELL TIMES
SRVOSIGHI
SRVOSIGHIAMP TP13
SYNCH ODD EVEN ODD EVEN SYNCH ODD EVEN ODD EVEN SYNCH ODD EVEN ODD EVEN
SRVOSIGLO
SRVOSIGLOAMP +0.17 -0.37
SRVO PULSE TP11
RETRIGGER
PULSE GATE TP3
350NS @ 1.5V
SEPPULSE TP23
SEPPULSEGATE 1E-6
ØLK GATE TP4
270CNS @ 1.5V
19MHz (18.797MHz @3530 RPM)
DIV4 P12-7
DIV8
DIV16
DIV32
DIV64 TP2
CLEAR PULSE TP9
CLEAR CLOCK TP8
CLEAR/ TP6
DIV12 TP5
SRVO GATE/
ODD FF
EVEN FF
ODD ST TP12
EVEN ST TP10
PATTERN CLK
19MHz
DIV4
TYPICAL
SRVOSIGHIAMP @ TP13
SERVO CELL TIME
ODD TRACK
EVEN TRACK
ON TRACK
1V P/P
1V P/P
1V P/P
0.5V P/P
SIGNALS SHOWN WITH RESPECT TO GND WITH ON TRACK CONDITION, NO SERVO MOTION.
ODD/EVEN PULSE AMPLITUDES WILL VARY WITH SERVO MOTION. IF THEY BECOME SMALL ENOUGH THE RESULTANT SRVOPULSE AND PULSE GATE SIGNALS WILL BE MISSING.
D BD20013711 A
SHEET 2 OF 3


3.4 µS
PULSEGATE•SRVOGATE/
PATTERN CLK
OGB1 PATTERN
319NS
SHIFT REGISTER OUTPUTS
OGB PULSE/
OUTER GUARD BAND 1
PULSE GATE•SRVOGATE/
PATTERN CLK
OGB2 PATTERN
SHIFT REGISTER OUTPUTS
OGB PULSE/
OUTER GUARD BAND 2
PULSE GATE•SRVOGATE/
PATTERN CLK
INDEX PATTERN
SHIFT REGISTER OUTPUTS
INDEX/
INDEX
17 MS NOM. (3530RPM)
INDEX
DISC SPEED MONITOR ONE SHOT 'Q'
20.3MS (2956 RPM)
RETRIGGER
UPTOSP/
OGB PULSE/
61.4 µS
INDEX/
TRIGGER
OGB SET
RETRIGGER
1.1 MS
OGB/

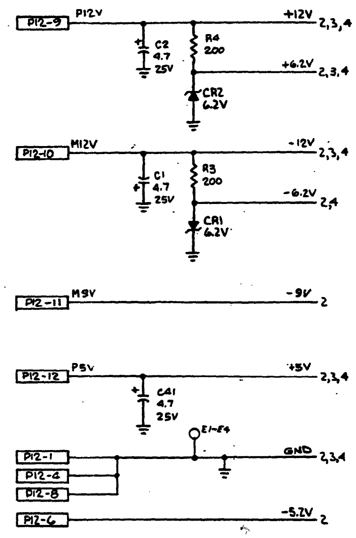
81 1091B

6-73

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
AX	P1199		PROTO RELEASE				
A	P1302		PILOT RELEASE				
B	P1385		NEW RELEASE				



COMPONENTS USED	LAST REF DES USED	REF DES NOT USED
CAPACITORS	C43	
DIODES	CR16	CR3
RESISTORS	R112	R32
TRANSISTORS	Q4	
VOLTAGE REG	VR 1	
TEST POINTS	TP 23	TP1
INDUCTORS	L2	



IC VOLTAGE CHART		
VOLTAGE	PIN NO.	IC REFERENCE DESIGNATION
+12	12	5C, 6A, 7D, 7F
+5V	14	2C, 2D, 3D, 3E, 3F, 3H, 4C, 4D, 5A, 3C, 7A, 7B, 8A, 8B
	16	1D, 1E, 4A, 4B
GND	1	2B
	4	5C, 6A, 7D, 7F
	16	2B
	7	2C, 2D, 3D, 3E, 3F, 3H, 4C, 4D, 5A, 3C, 7A, 7B, 8A, 8B
	8	1D, 1E, 3B, 4A, 4B
-5.2V	8	2B
-12V	5	5C, 6A, 7D, 7F

SC20013711 B

PIN NO	P12	SH NO.
1	GND	1
2	19 MHZ	2
3	19 MHZ/	2
4	GND	1
5	1.2 MHZ	2
6	M5.2V	1
7	4.8 MHZ	2
8	GND	1
9	P12V	1
10	M12V	1
11	M9V	1
12	P 5V	1

PIN NO.	P13	SH NO.
1	INDEX/	2
2	UPTØSP/	2
3	ØGB/	2
4	MTRI	3
5	ØFFSETFWD/	4
6	ØFFSETREV/	4
7	AMPIN	4
8	LDSP/	3
9	ØDD/	3
10	RETHDS/	4
11	MTH/	4
12	PTH/	4

PIN NO	P14	SH NO.
1	ØNTRK/	4
2	FWD/	3
3	REV/	3
4	TRKFL/	3
5	DIFF004/	3
6	DIFF032/	3
7	DIFF064/	3
8	DIFF002/	3
9	DIFF001/	3
10	DIFF016/	3
11	DIFF008/	3
12	FULLSP/	3

PIN NO.	J16	SH NO.
1	GND	2
2	GND	2
3	GND	2
4	GND	2
5	SRVØSIGLØ	2
6	SRVØSIGHI	2
7	GND	2
8	M8.2V	2
9	GND	2
10	M8.2V	2

6. FOR BLOCK DIAGRAM · TIMING DIAGRAM SEE BD20013711
5. ALL DIODES ARE 1N4153.
4. ALL 0.1 CAPACITORS ARE +80%/-20%, 25V.
3. ALL CAPACITORS ARE ± 10%, 50V OR HIGHER, GIVEN IN MFD'S.
2. ALL RESISTORS ARE ± 5%, 1/4 W, GIVEN IN OHMS.
1. INTERPRET DRAWING PER MIL-STD 100.

NOTES: UNLESS OTHERWISE SPECIFIED

UNINCORPORATED ENGINEERING ORDERS

NEXT ASSY: 20013711 · USED ON: REFLEX · APPLICATION

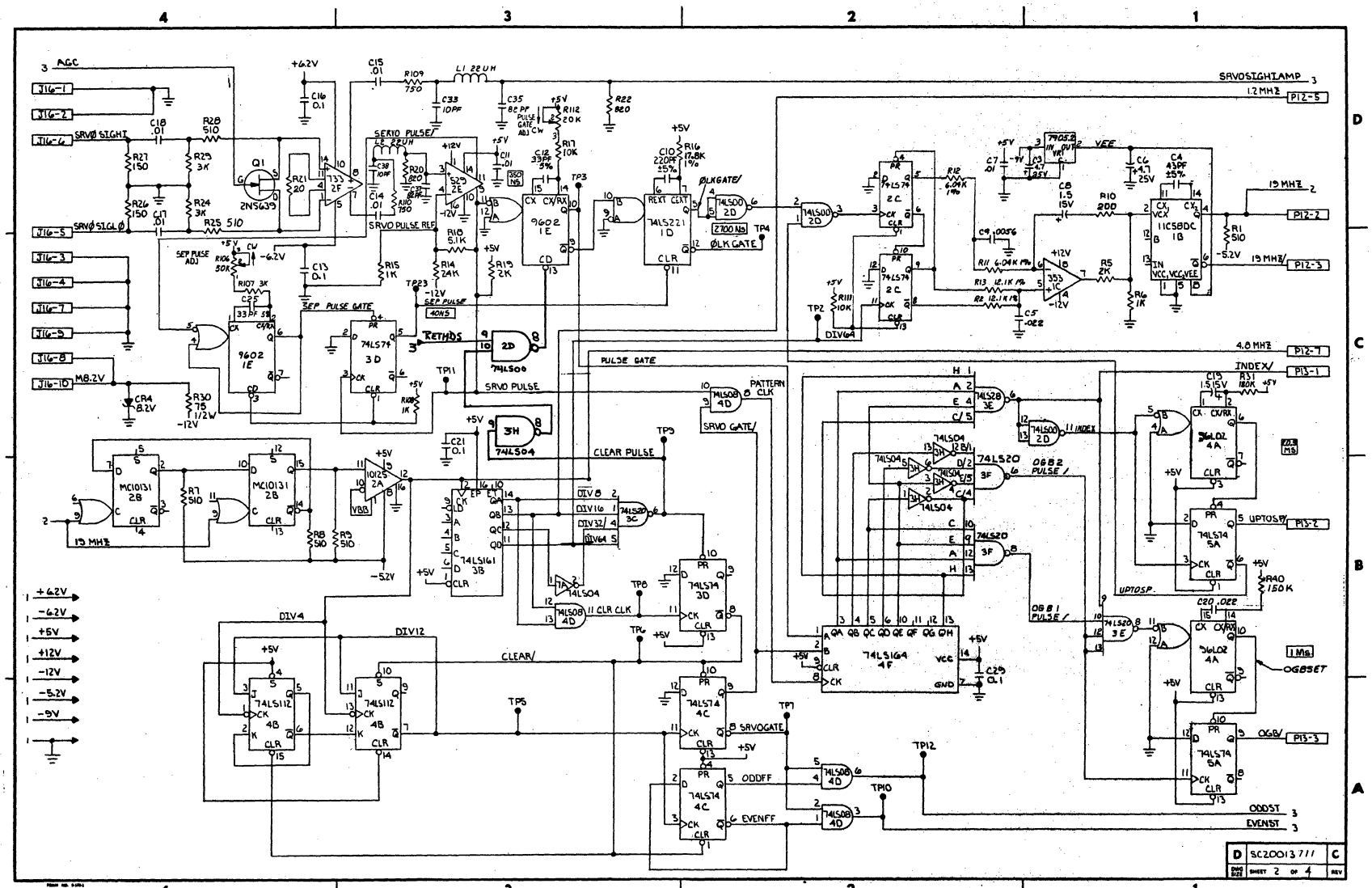
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES XX ± .02
TOLERANCES XXX ± .010
TOLERANCES ANGLES ±1/2°
MATERIAL
FINISH

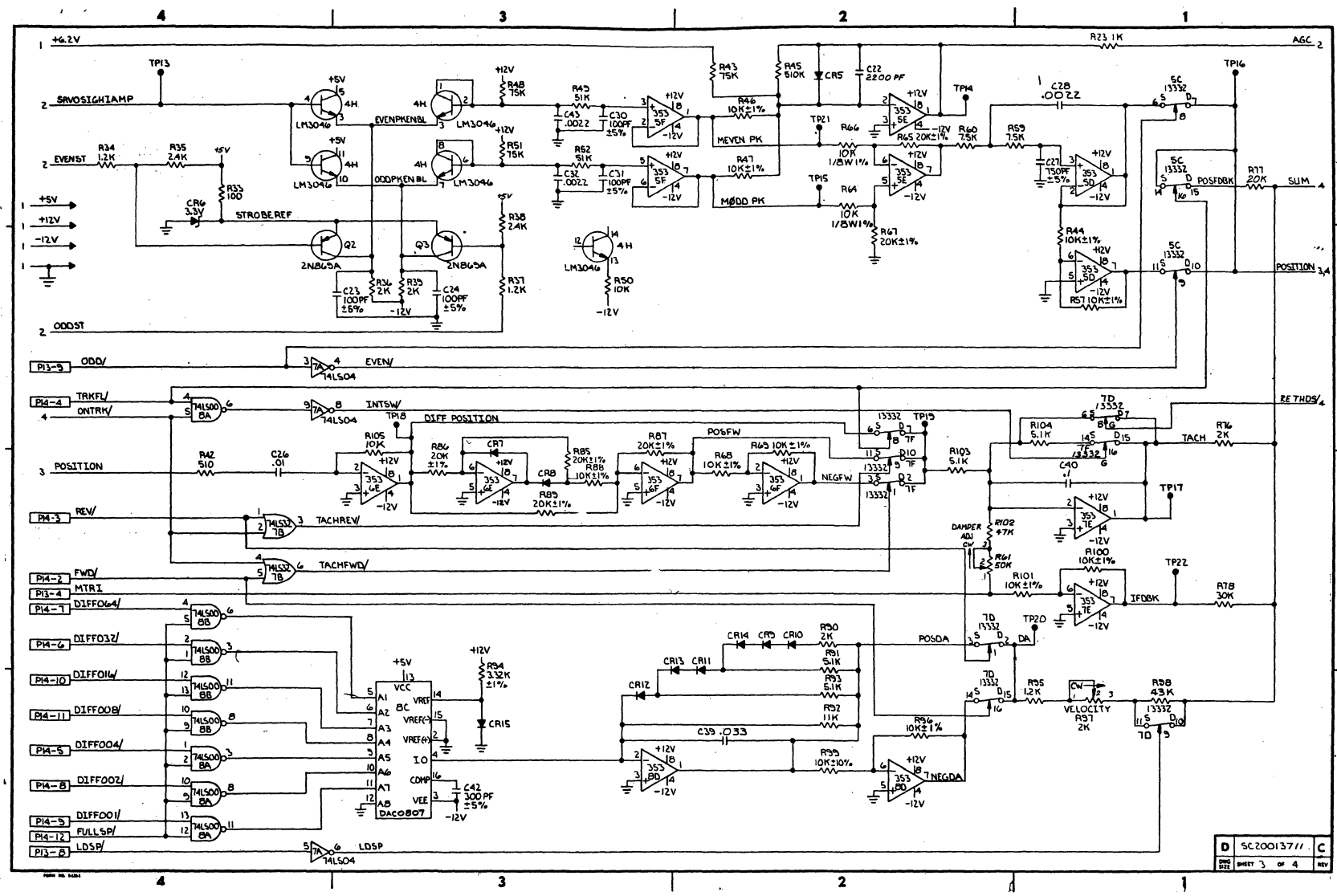
TITLE: PC B SCHEMATIC - SERVO

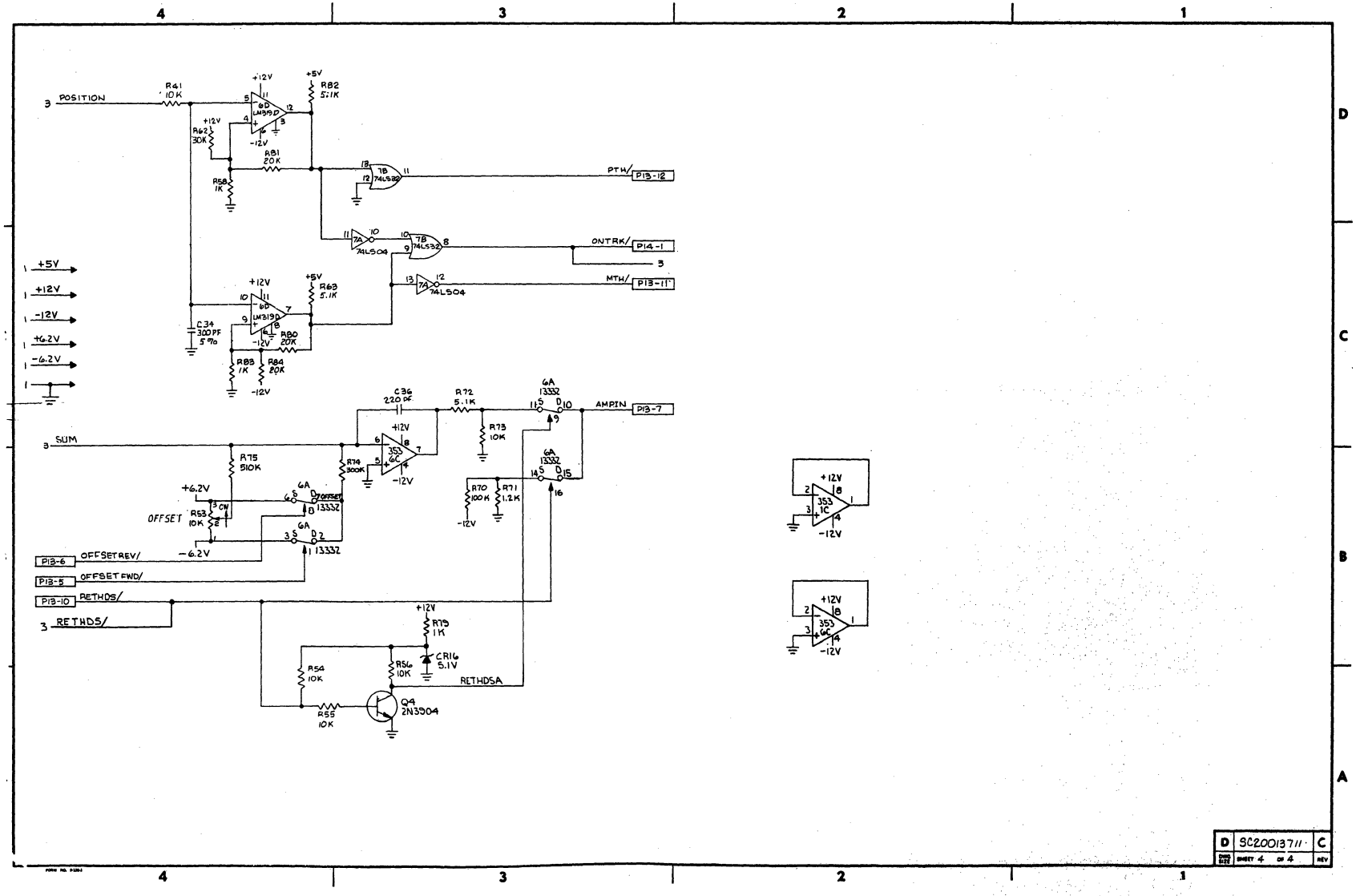
Microdata
IRVINE, CALIFORNIA

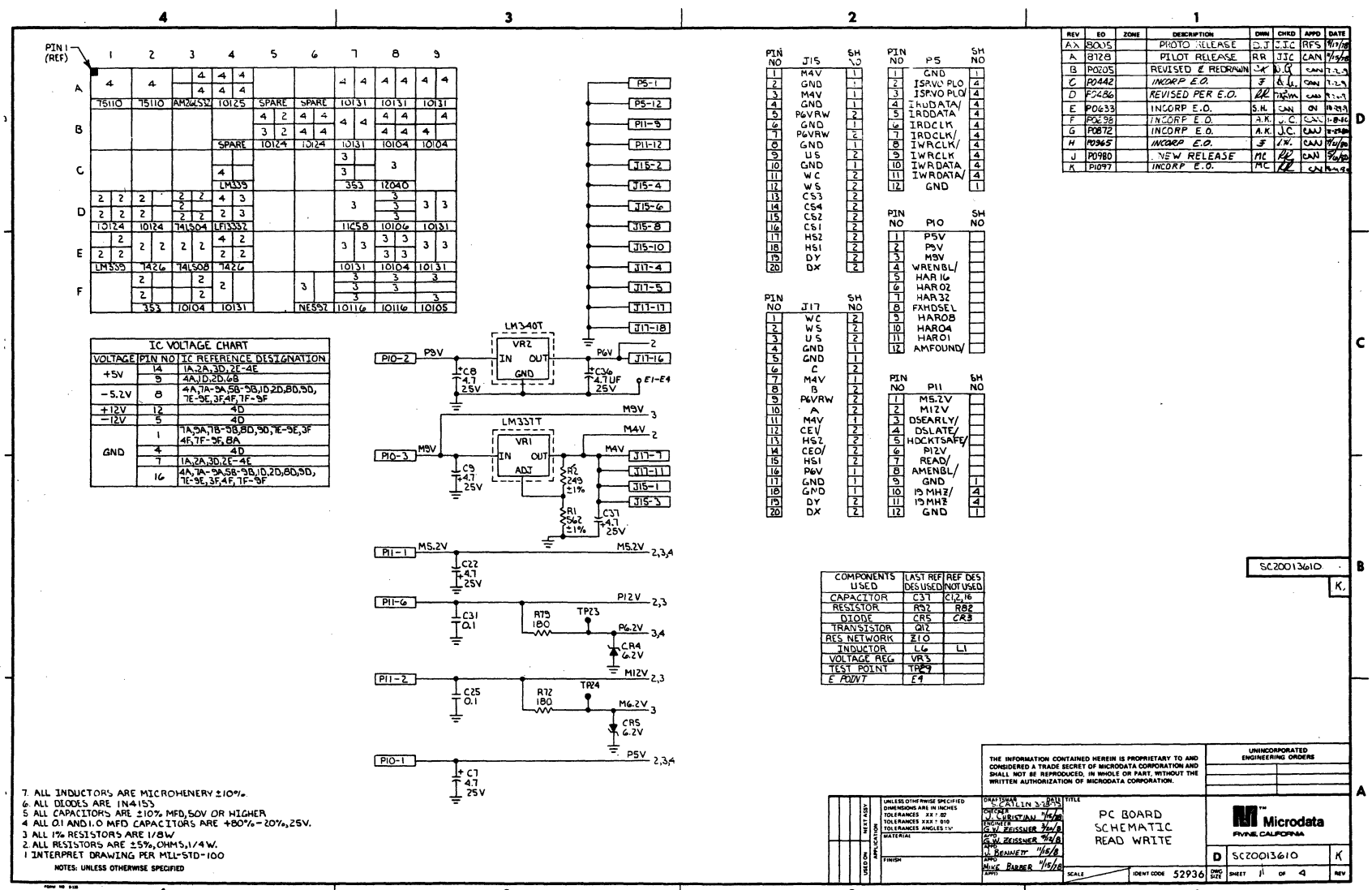
DWG SIZE		REV
D	SC20013711	C

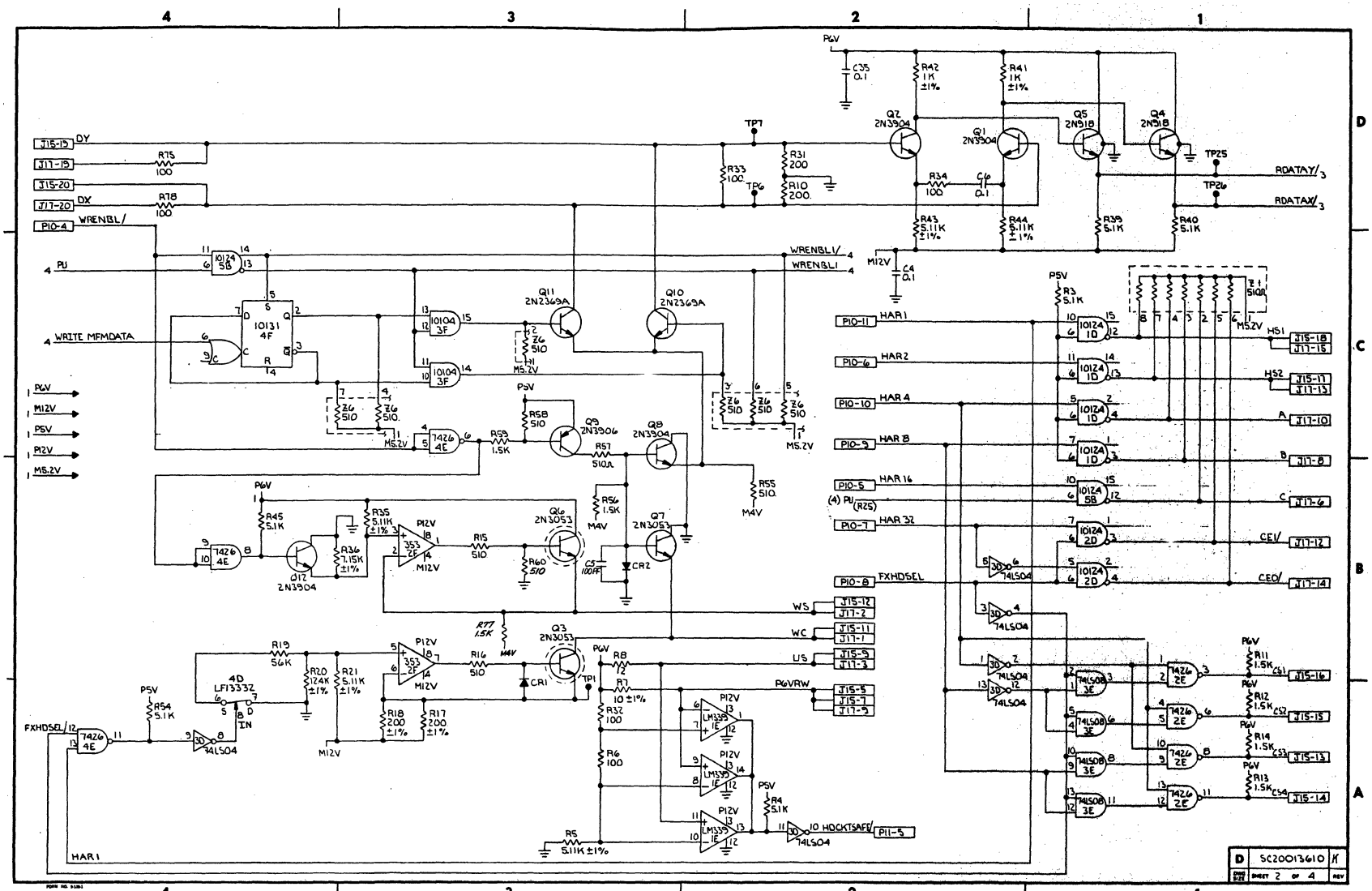
SCALE NONE · IDENT CODE 52936 · SHEET 1 OF 4

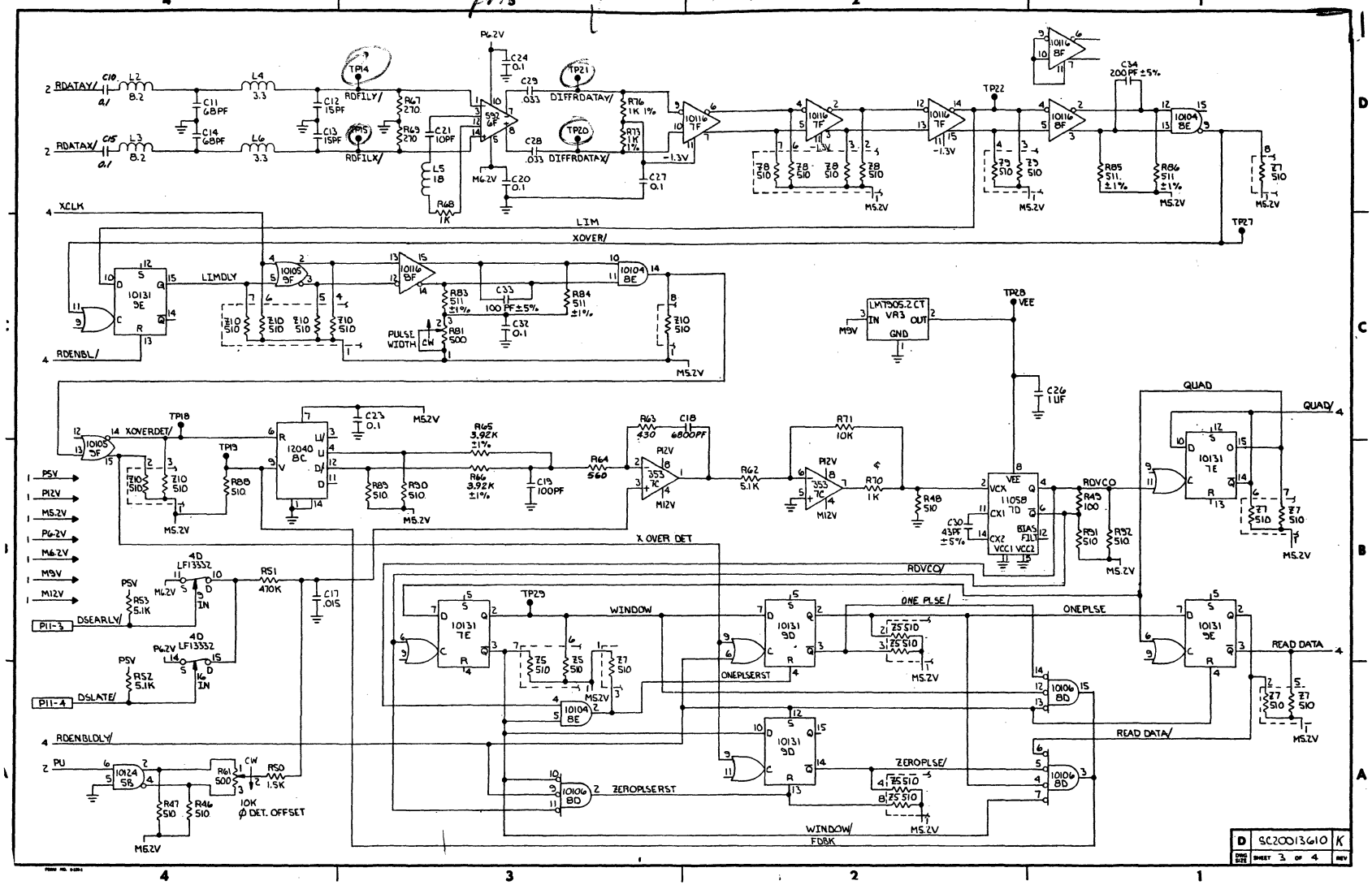

AGC
SRVOSIGHIAMP
1.2 MHZ
SERVO PULSE/
SRVO SIGHT
SRVO SIGLØ
SRVO PULSE REF
SEP PULSE GATE
SEP PULSE
RETRIG
PULSE GATE
SRVO PULSE
CLEAR PULSE
SRVO GATE/
CLEAR/
ØLKGATE/
ØLK GATE
PATTERN CLK
INDEX/
UPTOSP
ØBB1 PULSE/
ØBB2 PULSE/
OGBSET
ODDST
EVENST
SRVOGATE
ODDFF
EVENFF
DIV4
DIV12
DIV8
DIV16
DIV32
DIV64
15 MHZ
19 MHZ
4.8 MHZ
1 MHz
M8.2V
+6.2V
-6.2V
+5V
+12V
-12V
-5.2V
-9V
VEE
SC20013711


+6.2V
SRVOSIGHIAMP
EVENST
ODDST
STROBEREF
EVENPKENBL
ODDPKENBL
MEVEN PK
MODD PK
AGC
SUM
POSITION
POSFDBK
RETHDS/
TACH
IFDBK
DIFF POSITION
POSDA
NEGDA
DA
ODD/
EVEN/
TRKFL/
ONTRK/
INTSW/
POSITION
REV/
TACHREV/
TACHFWD/
FWD/
MTRI
DIFF064/
DIFF032/
DIFF016/
DIFF008/
DIFF004/
DIFF002/
DIFF001/
FULLSP/
LDSP/
DAC0807
VELOCITY
DAMPER ADJ
SC13332
D SC20013711 C
SHEET 3 OF 4


POSITION
R41 10K
+12V
+5V
R82 5.1K
R623 30K
R81 20K
R58 1K
LM319D
74LS32
74LS04
PTH/
P13-12
ONTRK/
P14-1
MTH/
P13-11
R63 5.1K
C34 300 PF 5%
R80 20K
R83 1K
R84 80K
-12V
+5V
+12V
-12V
+6.2V
-6.2V
C36 220 pF
R72 5.1K
R73 10K
6A 13332
AMPIN
P13-7
SUM
R75 510K
R74 300K
353 6C
R70 100K
R71 1.2K
OFFSET
R53 10K
OFFSET
P13-6
OFFSETREV/
P13-5
OFFSETFWD/
P13-10
RETHDS/
RETHDS/
R79 1K
CR16 5.1V
RETHDSA
R54 10K
R56 10K
R55 10K
Q9 2N3904
D SC2001371 C
SHEET 4 OF 4


PIN 1 (REF)
1 2 3 4 5 6 7 8 9
A
B
C
D
E
F
75110 75110 AM26LS32 10125 SPARE SPARE 10131 10131 10131
SPARE 10124 10124 10131 10104 10104
LM339 353 12040
10124 10124 74LS04 LF13332 11C58 10106 10131
LM339 7426 74LS08 7426 10131 10104 10131
353 10104 10131 NE592 10116 10116 10105
IC VOLTAGE CHART
VOLTAGE PIN NO IC REFERENCE DESIGNATION
+5V 14 1A,2A,3D,2E-4E
9 4A,1D,2D,6B
-5.2V 8 4A,7A-9A,5B-9B,1D,2D,8D,9D, 7E-9E,3F,4F,7F-9F
+12V 12 4D
-12V 5 4D
GND 1 7A,9A,7B-9B,8D,9D,7E-9E,3F 4F,7F-9F,8A
4 4D
7 1A,2A,3D,2E-4E
16 4A,7A-9A,5B-9B,1D,2D,8D,9D, 7E-9E,3F,4F,7F-9F
LM340T
VR2
IN OUT
GND
P6V
C8 4.7 25V
C36 4.7UF 25V
E1-E4
LM337T
VR1
IN OUT
ADJ
R2 249 ±1%
R1 562 ±1%
C37 4.7 25V
C9 4.7 25V
C22 4.7 25V
C31 0.1
C25 0.1
C7 4.7 25V
R79 180
R72 180
TP23
TP24
CR4 6.2V
CR5 6.2V
P10-2
P10-3
P11-1
P11-6
P11-2
P10-1
P8V
M8V
M4V
M5.2V
P12V
M12V
P6.2V
M6.2V
P5V
2,3,4
P5-1
P5-12
P11-9
P11-12
J15-2
J15-4
J15-6
J15-8
J15-10
J11-4
J11-5
J11-17
J11-18
J11-16
J11-7
J11-11
J15-1
J15-3
PIN NO J15 SH NO
1 M4V 1
2 GND 1
3 M4V 1
4 GND 1
5 P6VRW 2
6 GND 1
7 P6VRW 2
8 GND 1
9 U5 2
10 GND 1
11 WC 2
12 WS 2
13 CS3 2
14 CS4 2
15 CS2 2
16 CS1 2
17 HS2 2
18 HS1 2
19 DY 2
20 DX 2
PIN NO J17 SH NO
1 WC 2
2 WS 2
3 U5 2
4 GND 1
5 GND 1
6 C 2
7 M4V 1
8 B 2
9 P6VRW 2
10 A 2
11 M4V 1
12 CE\ 2
13 HS2 2
14 CE0/ 2
15 HS1 2
16 P6V 1
17 GND 1
18 GND 1
19 DY 2
20 DX 2
PIN NO P5 SH NO
1 GND 1
2 ISRVC PLO 4
3 ISRVO PLO\ 4
4 IRDATA/ 4
5 IRDATA 4
6 IRDCLK 4
7 IRDCLK\ 4
8 IWRCLK\ 4
9 IWRCLK 4
10 IWRDATA 4
11 IWRDATA\ 4
12 GND 1
PIN NO P10 SH NO
1 P5V
2 P8V
3 M8V
4 WRENBL\
5 HAR16
6 HAR02
7 HAR32
8 FXHDSEL
9 HAR0B
10 HAR04
11 HAR01
12 AMFOUND\
PIN NO P11 SH NO
1 M5.2V
2 M12V
3 DSEARLY\
4 DSLATE\
5 HDCKTSAFE\
6 P12V
7 READ\
8 AMENBL\
9 GND 1
10 19 MHZ\ 4
11 19 MHZ 4
12 GND 1
COMPONENTS USED | LAST REF DES USED | REF DES NOT USED
CAPACITOR | C37 | C12,16
RESISTOR | R92 | R82
DIODE | CR5 | CR3
TRANSISTOR | Q12 |
RES NETWORK | Z10 |
INDUCTOR | L6 | L1
VOLTAGE REG | VR3 |
TEST POINT | TP29 |
E POINT | E9 |
REV ED ZONE DESCRIPTION DWN CHKD APPD DATE
AA 80015 PROTO RELEASE D.J J.JC RFS 11/1/78
A 81128 PILOT RELEASE RR JJC CAN 7/5/80
B P0205 REVISED & REDRAWN JK D.G CAN 7-2-9
C P0442 INCORP E.O. JF D.G. CAN 7-2-9
D P2486 REVISED PER E.O. RR [illegible] CAN 7-2-9
E P0633 INCORP E.O. S.H. CAN ON 10-29-9
F P0298 INCORP E.O. A.K. J.C. CAN 1-8-80
G P0872 INCORP E.O. A.K. J.C. CAN 7-25-80
H P0965 INCORP E.O. JF J.W. CAN 9/4/80
J P0980 NEW RELEASE MC RR CAN 5/6/80
K P1097 INCORP E.O. MC RR CAN 11-4-80
7. ALL INDUCTORS ARE MICROHENERY ±10%.
6. ALL DIODES ARE 1N4153
5 ALL CAPACITORS ARE ±10% MFD,50V OR HIGHER
4 ALL 0.1 AND 1.0 MFD CAPACITORS ARE +80%-20%,25V.
3 ALL 1% RESISTORS ARE 1/8W
2. ALL RESISTORS ARE ±5%,OHMS,1/4W.
1 INTERPRET DRAWING PER MIL-STD-100
NOTES: UNLESS OTHERWISE SPECIFIED
THE INFORMATION CONTAINED HEREIN IS PROPRIETARY TO AND CONSIDERED A TRADE SECRET OF MICRODATA CORPORATION AND SHALL NOT BE REPRODUCED, IN WHOLE OR PART, WITHOUT THE WRITTEN AUTHORIZATION OF MICRODATA CORPORATION.
UNINCORPORATED ENGINEERING ORDERS
SC20013610 B
K.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES XX ± .02 TOLERANCES XXX ± .010 TOLERANCES ANGLES ±1° MATERIAL FINISH
NEXT ASSY APPLICATION USED ON
DRAFTSMAN C. CAILIN 3-18-80
CHECKED J. CHRISTIAN 9/4/80
ENGINEER G.W. ZEISSNER 9/4/80
APPD G.W. ZEISSNER 9/4/80
APPD W. BENNETT 11/6/80
APPD MIKE BARBER 11/6/80
TITLE PC BOARD SCHEMATIC READ WRITE
Microdata IRVINE, CALIFORNIA
D SC20013610 K
SCALE IDENT CODE 52936 DWG SIZE SHEET 1 OF 4 REV

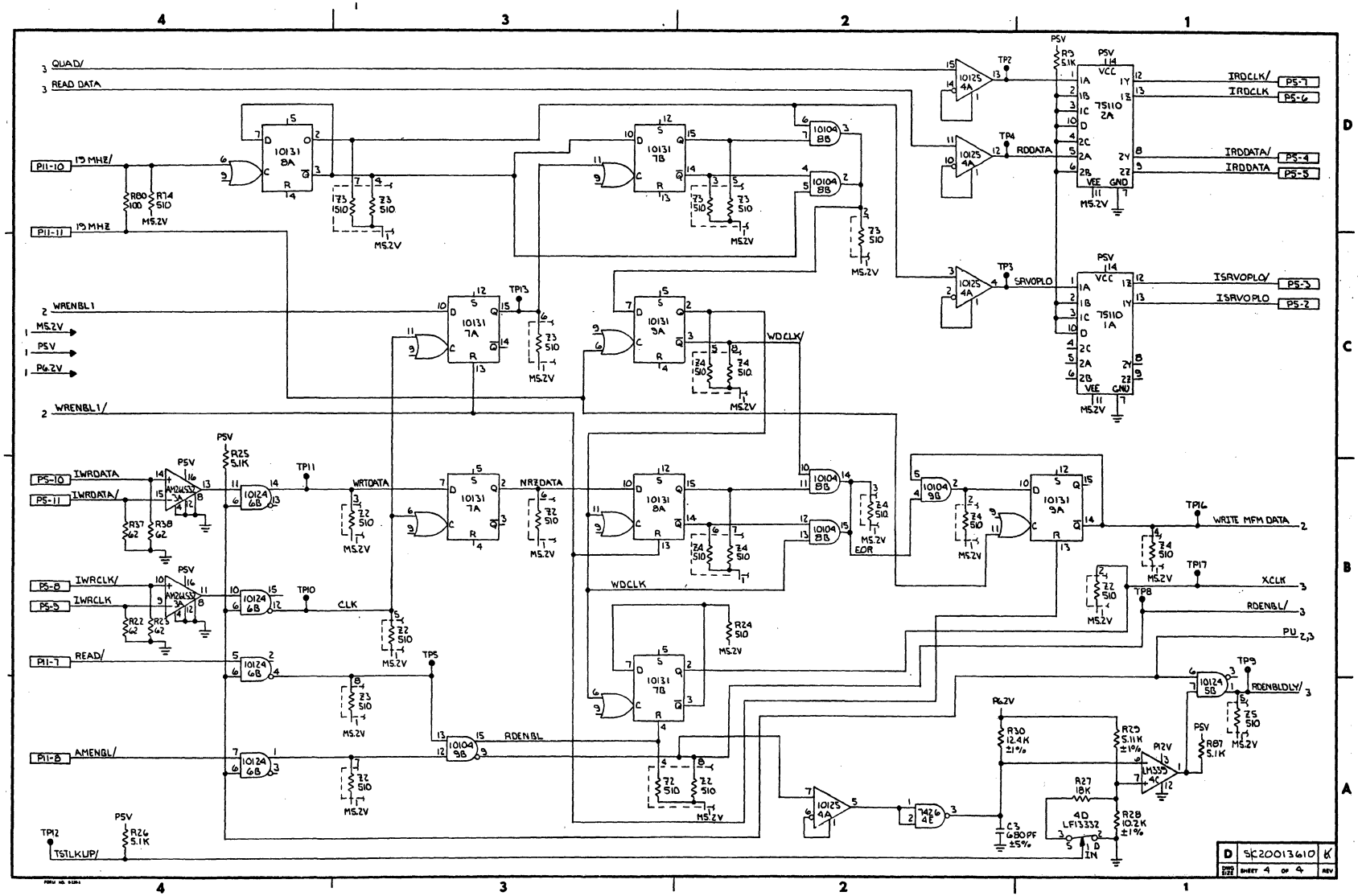

4
3
2
1
D
C
B
A
P6V
P5V
M12V
M5.2V
WRENBL/
WRENBL1/
WRENBL1
WRITE MFMDATA
PU
DY
DX
RDATAY/3
RDATAX/3
HAR1
HAR2
HAR4
HAR8
HAR16
HAR32
FXHDSEL
WS
WC
US
P6VRW
IO HOCKTSAFE/
SC20013610
K
SHEET 2 OF 4

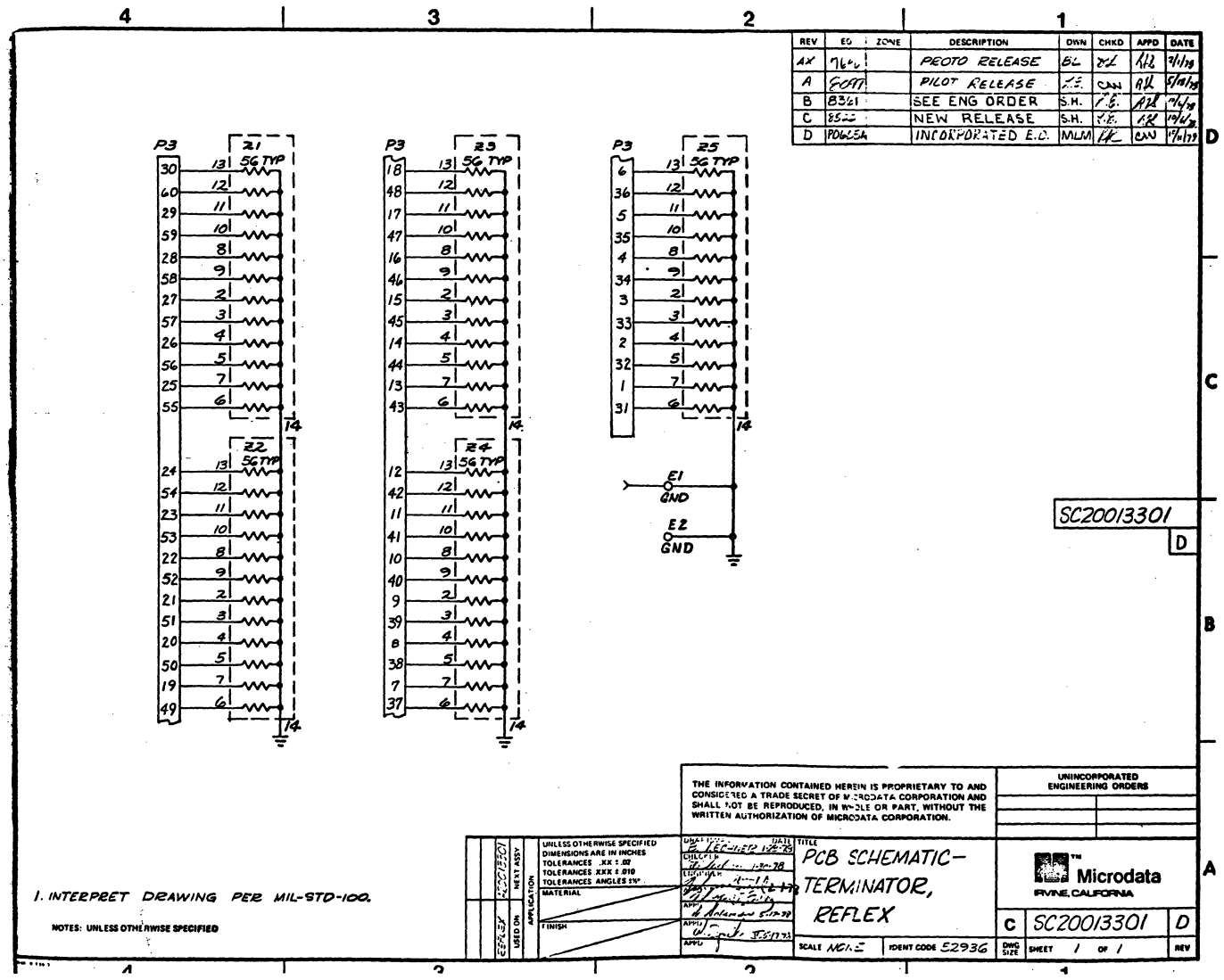


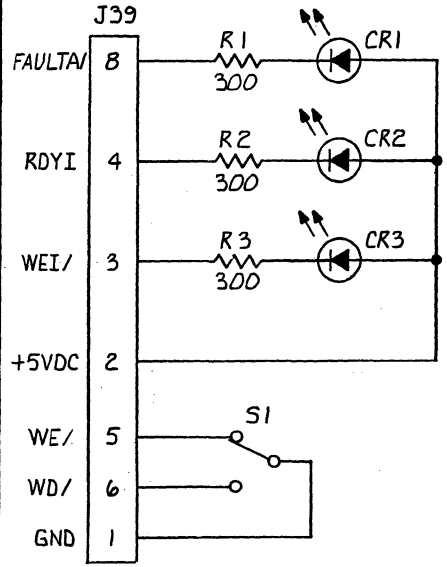
each head selected follows this path

✓ Amplitude .5 volts or .6 volts DAC 1.04 volts

WHF WCF you do write Rd - Read Mode Drive will Fault if when Select Head 19


QUAD/
READ DATA
WRENBL1
WRENBL1/
WDCLK/
WDCLK
WRTDATA
NRZDATA
CLK
RDENBL
AMENGL/
IRDCLK/
IRDCLK
IRDDATA/
IRDDATA
ISRVOPLO/
ISRVOPLO
WRITE MFM DATA
XCLK
RDENBL/
RDENBLDLY/
PU
TSTLKUP/
IWRDATA
IWRDATA/
IWRCLK/
IWRCLK
READ/
AMENGL/
RDDATA
SRVOPLO
EOR
PSV
MS.2V
P6.2V
P12V
SIZE
SHEET 4 OF 4
REV


4
3
2
1
REV | EO | ZONE | DESCRIPTION | DWN | CHKD | APPD | DATE
AX | 7602 | | PHOTO RELEASE | BL | RL | | 7/12/78
A | 6077 | | PILOT RELEASE | KE | CAN | RL | 5/9/78
B | 8361 | | SEE ENG ORDER | S.H. | KE | RL | 7/6/78
C | 8522 | | NEW RELEASE | S.H. | KE | RL | 10/6/78
D | P0625A | | INCORPORATED E.O. | MLM | KE | CAN | 12/6/78
P3
21
22
23
24
25
5G TYP
14
E1
GND
E2
GND
SC20013301
D
THE INFORMATION CONTAINED HEREIN IS PROPRIETARY TO AND CONSIDERED A TRADE SECRET OF MICRODATA CORPORATION AND SHALL NOT BE REPRODUCED, IN WHOLE OR PART, WITHOUT THE WRITTEN AUTHORIZATION OF MICRODATA CORPORATION.
UNINCORPORATED ENGINEERING ORDERS
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES .XX ± .02
TOLERANCES .XXX ± .010
TOLERANCES ANGLES ±1°
MATERIAL
FINISH
NEXT ASSY
USED ON
APPLICATION
DRAFT
CHECK
ENGR
APPD
TITLE
PCB SCHEMATIC-
TERMINATOR,
REFLEX
Microdata
IRVINE, CALIFORNIA
C
SC20013301
D
SCALE NONE
IDENT CODE 52936
DWG SIZE
SHEET 1 OF 1
REV
1. INTERPRET DRAWING PER MIL-STD-100.
NOTES: UNLESS OTHERWISE SPECIFIED



SC20013323 B

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A X	8072		PROTO RELEASE	RL	J.J.C.	RH	9/22/78
A	E385		PILOT RELEASE	L.b.	J.J.C.	RH	9/7/78
B	8517		NEW RELEASE	S.H.	L.b.	RH	10/12/78

COMPONENTS USED	LAST REF DES USED	REF DES NOT USED
LED	CR3	
RESISTOR	R3	
SWITCH	S1	

2. ALL RESISTORS ARE 1/4W, ±5%, C.F. AND VALUED IN OHMS.
1. INTERPRET PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

REFLEX A2001331D — USED ON — NEXT ASSY — APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES .XX ±.02
TOLERANCES .XXX ±.010
TOLERANCES ANGLES ±½°
MATERIAL
FINISH

DRAFTSMAN L. Reynolds DATE 4-12-78
CHECKER L. Murietta 4/25/78
ENGINEER Wayne Slyter 4-25-78
APPD Wayne Heath 4-25-78
APPD E. Flynn 8-3-78
APPD [illegible] 10-12-78

TITLE: PCB SCHEMATIC LED / SWITCH

SCALE NONE | CODE IDENT 52936

Microdata
IRVINE, CALIFORNIA

B | SC20013323 | B
DWG SIZE | SHEET 1 OF 1 | REV

FORM NO. 9-137

ASSEMBLY NO.	MODEL NO.	UL RECOGNIZED	DESCRIPTION
20013600-007	7521-7522	YES	4 DISC, 60Hz, 115VAC, 4.5A, WITH LED PANEL, WITH TERM. BD
20013600-007	7521N-7522N	NO	" " " " " " "
20013600-005	7521-7522	YES	" " " " " " "
20013600-005	7521N-7522N	NO	" " " " " " "
20013600-001	7521-7522	YES	" " " " WITH LED PANEL "
20013600-001	7521N-7522N	NO	" " " " " "

REV	EO	ZONE	DESCRIPTION	DWN	CHKD	APPD	DATE
A	7231		FIRST RELEASE	RJ	[illegible]	CWN	11-4-75
B	P0244		INCORP EO	GE	J.J.C	CWN	4/1/79
C	P0512		INCORP E.O.	F	[illegible]	CWN	5/14/79
D	P0636		INCORP E.O.	A.K.	CWN	CN	8-24-79
E	P0667		INCORP E.O.	A.K.	[illegible]	CN	9-24-79
F	P0701		INCORP E.O.	A.K.	[illegible]	CN	11-26-79
G	P0654		INCORP E.O.	S.H	CWN	CN	12-19-79
H	P0691A		INCORP E.O.	A.K	CWN	CN	2-12-80
J	P0723		INCORP E.O.	MC	J.W.	CWN	4/4/80
K	P1019		NEW RELEASE	F	J.W.	CWN	8/8/80
L	P0999		INCORP E.O.	A.K.	J.W.	CN	8-8-80
M	P1348		INCORP E.O.	F	J.W.	CWN	1-20-81
N	P1351		INCORP E.O.	F	J.W.	CWN	1-28-81
P	P1406		INCORP E.O.	F	J.W.	CWN	3-17-81
R	P1420		INCORP E.O	[illegible]	J.W.	[illegible]	4-3-81

PART NO.	REV	OPTIONS	1 DISC	2 DISC	3 DISC	4 DISC	60 Hz	50 Hz	100 V	115 V	120 V	200 V	208 V	220 V	240 V	W/O FIXED HD	W/ FIXED HD	W/O TERM BD	W/ TERM BD	W/O LED PANEL	W/ LED PANEL	W/O POWER CORD ALSO W/O POWER CORD	W/ POWER CORD	W/O INT GND	W/ INT GND	W/O EXT GND	W/ EXT GND	W/O PWR ONLY
-015	A				X		X						X				X		X	X			X	X		X		
-014	A				X	X						X					X		X	X		X		X		X		
-013	A				X		X				X						X		X	X			X	X		X		
-012	A				X	X					X						X		X	X		X		X		X		
-011	A			X		X			X								X	X		X		X		X		X		
[7] -010	A				X	X		X									X		X	X			X	X		X		
[7] -009	A				X		X	X									X		X	X			X	X		X		
[7] -008	D				X		<		X								X	X		X				X	X		X	
-007	E				X	X			X								X	X		X		X		X		X		
[7] -006	D				X		>		X								X	X			X		X	X		X		
-005	E				X	X			X								X	X			X	X		X		X		
[7] -004	D				X		>										X		X	X				X	X		X	
[7] -003	D				X		<										X		X	X				X	X		X	
[7] -002	D				X		X		X								X		X	X				X	X		X	
A20013600-001	E				X	X			X								X		X	X			X	X		X		

[3] ASSEMBLY CHART

[7] REMOVE EXISTING PLUG FROM ITEM 005 PRIOR TO SHIPMENT.

[6] FOR ASSEMBLIES A20013600-005, -006, 007 & -008 WITH PCB LOGIC W/INTERFACE A20013608 (REV A, B, D, E & G DETAIL BOARDS) USING PCB TERMINATOR BOARD A20013301-001 (REV A, B OR D DETAIL BOARDS) SOLDER THE 2 INCH LONG WIRE (FROM Z1-14 ON A20013301-001) TO THE GROUND PLANE AT THE RIGHT SIDE OF J1 ON A20013608 (COMP. SIDE). FOR ASSEMBLIES A20013600-005, -006, 007 & -008 WITH PCB LOGIC W/INTERFACE A20013608 (REV H OR HIGHER DETAIL BOARDS) USING PCB TERMINATOR BOARD A20013301-001 (REV E OR HIGHER DETAIL BOARDS) ATTACH THE FEMALE TERMINAL (FROM E2 ON A20013301-001) TO THE MALE TERMINAL E2 BELOW J1 ON A20013608 (COMP. SIDE).

5. REFER TO WIRING DIAGRAM WD20013600, ASSEMBLY BREAKDOWN AB20013600, PRODUCT SPECIFICATION PS20013571, TEST SPECIFICATION TS20013574.

[4] ACTUAL DIMENSION DETERMINED @ ASSEMBLY

[3] CONFIGURATION PER ASSEMBLY CHART AND APPLICABLE LIST OF MATERIAL.

2. ASSEMBLE PER MICRODATA WORKMANSHIP MANUAL.

1. INTERPRET DRAWING PER MIL-STD-100.

NOTES: UNLESS OTHERWISE SPECIFIED

A20013600 R

TABULATED

UNINCORPORATED ENGINEERING ORDERS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES .XX ± .02 TOLERANCES .XXX ± .010 TOLERANCES ANGLES ± 1°

MATERIAL SEE L/M

FINISH

NEXT ASSY

USED ON REFLEX II APPLICATION

DRAFTSMAN DATE

CHECKER 8-18-8

ENGINEER

APPD

APPD

APPD

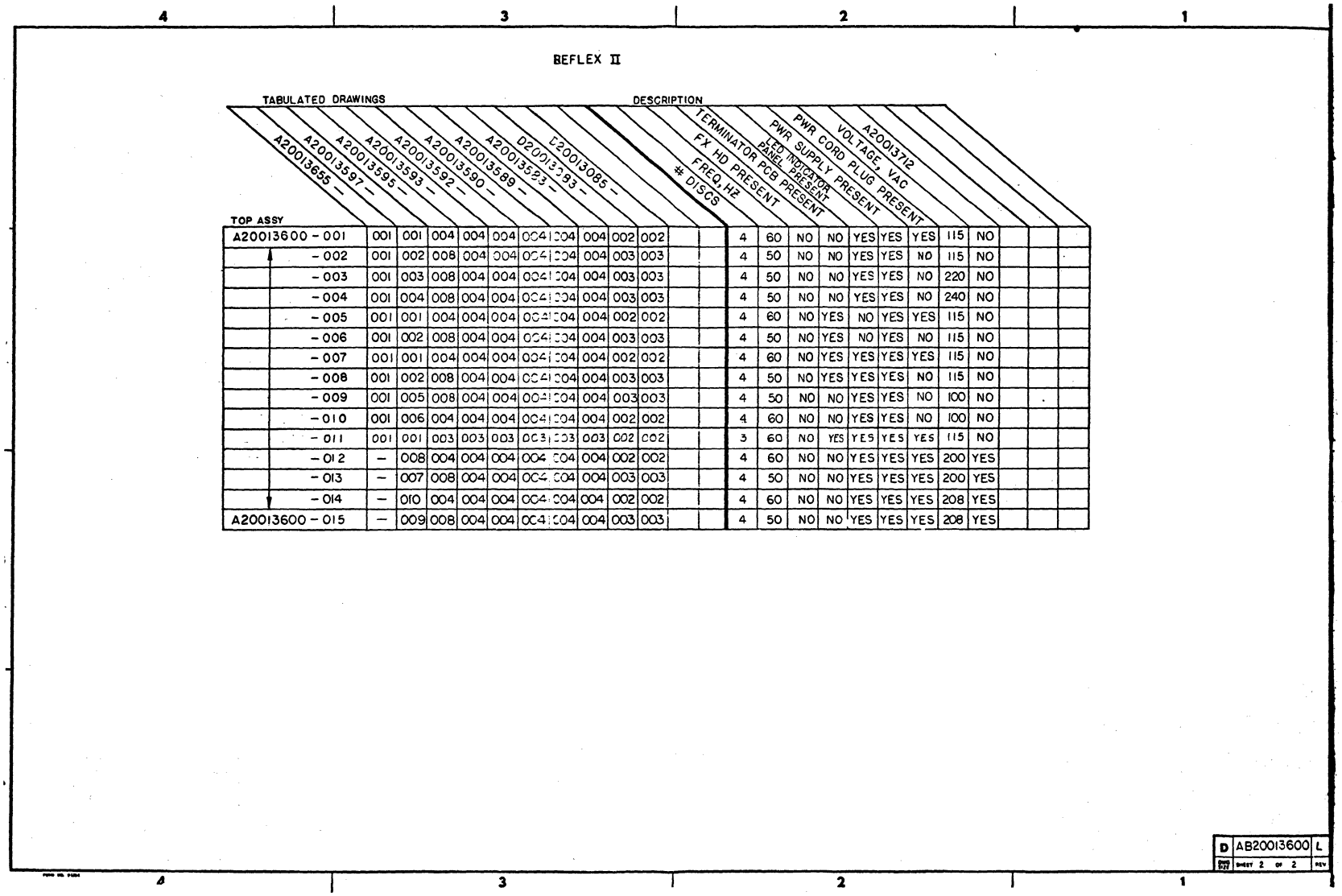
TITLE REFLEX II DRIVE ASSEMBLY

Microdata IRVINE CALIFORNIA

SCALE 1/1 IDENT CODE 52936 DWG SHT SHEET 1 OF 5

D A20013600 R

REV



REFLEX II

TABULATED DRAWINGS / DESCRIPTION	A20013655 –	A20013597 –	A20013595 –	A20013593 –	A20013592 –	A20013590 –	A20013589 –	D20013593 –	D20013085 –	# DISCS	FREQ, HZ	FX HD PRESENT	TERMINATOR PCB PRESENT	PWR SUPPLY PRESENT	LED INDICATOR PANEL PRESENT	PWR CORD PLUG PRESENT	VOLTAGE, VAC	A20013712			
TOP ASSY																					
A20013600 – 001	001	001	004	004	004	004	004	004	002	002	4	60	NO	NO	YES	YES	YES	115	NO		
– 002	001	002	008	004	004	004	004	004	003	003	4	50	NO	NO	YES	YES	NO	115	NO		
– 003	001	003	008	004	004	004	004	004	003	003	4	50	NO	NO	YES	YES	NO	220	NO		
– 004	001	004	008	004	004	004	004	004	003	003	4	50	NO	NO	YES	YES	NO	240	NO		
– 005	001	001	004	004	004	004	004	004	002	002	4	60	NO	YES	NO	YES	YES	115	NO		
– 006	001	002	008	004	004	004	004	004	003	003	4	50	NO	YES	NO	YES	NO	115	NO		
– 007	001	001	004	004	004	004	004	004	002	002	4	60	NO	YES	YES	YES	YES	115	NO		
– 008	001	002	008	004	004	004	004	004	003	003	4	50	NO	YES	YES	YES	NO	115	NO		
– 009	001	005	008	004	004	004	004	004	003	003	4	50	NO	NO	YES	YES	NO	100	NO		
– 010	001	006	004	004	004	004	004	004	002	002	4	60	NO	NO	YES	YES	NO	100	NO		
– 011	001	001	003	003	003	003	003	003	002	002	3	60	NO	YES	YES	YES	YES	115	NO		
– 012	–	008	004	004	004	004	004	004	002	002	4	60	NO	NO	YES	YES	YES	200	YES		
– 013	–	007	008	004	004	004	004	004	003	003	4	50	NO	NO	YES	YES	YES	200	YES		
– 014	–	010	004	004	004	004	004	004	002	002	4	60	NO	NO	YES	YES	YES	208	YES		
A20013600 – 015	–	009	008	004	004	004	004	004	003	003	4	50	NO	NO	YES	YES	YES	208	YES		

D | AB20013600 | L

SHEET 2 OF 2

APPENDIX A

NUMBER CONVERSIONS

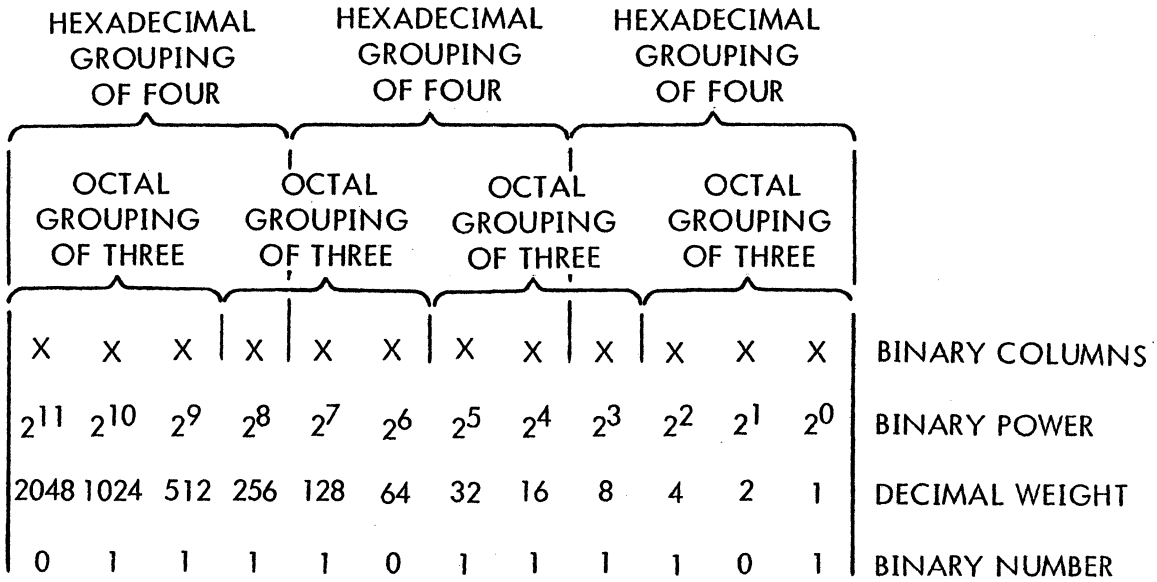
The numbering sequence for binary, octal, decimal and hexadecimal numbers are listed below:

Binary	Octal	Decimal	Hexadecimal
0	0	0	0
1	1	1	1
10	2	2	2
11	3	3	3
100	4	4	4
101	5	5	5
110	6	6	6
111	7	7	7
1000	10	8	8
1001	11	9	9
1010	12	10	A
1011	13	11	B
1100	14	12	C
1101	15	13	D
1110	16	14	E
1111	17	15	F
10000	20	16	10
10001	21	17	11
10010	22	18	12
10011	23	19	13
10100	24	20	14

etc.

Digital logic uses the binary number system for its 2-state representation, i.e., 1 or 0, yes or no, on or off. However, this digital representation becomes difficult to converse in, both verbally and in printed matter. Therefore, digital systems normally use the octal or hexadecimal number systems as a means of outside communication. These systems conveniently break the binary numbers into groups of three (octal) or four (hexadecimal) as a method for providing an easier form of communication for those who are at least somewhat familiar with digital computing systems. There is still a problem when trying to communicate with the layman who is not familiar with the innards of computers. For this reason the binary number system must be converted into the decimal number system, which is familiar to most people.

The binary number system is in powers of 2. By knowing the column weights, one can convert to decimal numbers by adding the weights of the column where there is a digital/binary 1. This may be seen, along with the octal and hexadecimal grouping, in the example that follows.



Converting Binary to Decimal

This binary number is converted to a decimal number by adding the decimal weights of the binary columns where a 1 is present. An example is shown below.

```
   1
   4
   8
  16
  32
 128
 256
 512
1024
1981
```

Converting Decimal to Binary

The decimal number obtained above can now be converted into a binary number by subtracting the decimal weights and representing each successful subtraction by placing a 1 in that binary column. An example follows.

```
1981
1024
 957
 512
 445
 256
 189
 128
  61  (no 64)
```

```
61  (no 64)
32
29
16
13
 8
 5
 4
 1  (no 2)
 1
 0
```

1024	512	256	128	64	32	16	8	4	2	1
1	1	1	1	0	1	1	1	1	0	1

Converting Binary to Hexadecimal

(1) Divide the binary number into groups of four, starting from the right bit (add leading zeros to the left group to form a group of four).

(2) Refer to the above example and convert each 4-bit group to the corresponding hexadecimal number.

Step 1: 11110111101 Binary number
0111 1011 1101 Groups of 4-bits

Step 2: 7BD Convert to hexadecimal
Hexadecimal number is 7BD

Converting Hexadecimal to Binary

Write the 4-bit binary number for each digit of the hexadecimal number. Drop any leading zeros.

3FE Hexadecimal number

001 1111 1110 Convert to binary

Binary number is 1111111110

Converting Binary to Octal or Vice Versa

Use the same procedure as for hexadecimal numbers except for the number of bits in a group. Octal conversion uses 3-bit groupings of the binary bits.

If the binary number from above is used, the octal number becomes 1776 as shown below.

1111111110 Binary number

001 111 111 110 Groups of 3-bits

1 7 7 6 Octal number

Note: Consult a good binary number textbook for additional information in this area.

APPENDIX B

GLOSSARY

BPI	(bits-per-inch) A measurement of the density of data.
CAR	(cylinder address register) - Register where the cylinder number of the location of servo head is stored.
CARRLKRLSD	(carriage lock released) - Signal indicating that the carriage lock is not active (released).
C/DIFF/	(difference clock) - Logic signal generated when servo head passes over a track. It is used for counting tracks to decrement the difference counter.
CONTROLTAG	Logic signal used to initiate control functions.
DCSAFE	(DC safe) - Logic signal indicating that DC voltages on the power supply/amplifier PCB are not below tolerance.
DIFFZERO	(difference of zero) - Logic term indicating there are no DIF bits active in the difference counter.
DSEARLY	(data strobe early) - Logic command to read circuit to strobe data 5 ns earlier than normal.
DSLATE	(data strobe late) - Logic command to read circuit to strobe data 5 ns later than normal.
FWD	(forward) - Logic command for servo to move toward the spindle.
FXHDSEL	(fixed head select) - Logic signal to select the fixed heads and deselect the moving heads.
HAR	(head address register) - A register containing the number of the read/write head being selected.

INDEX or INDEXC	(index) - Signal generated from servo track information used as read/write reference point. This signal designates the beginning of a track.
/ETMRINHIBIT/	Logic signal generated by the exerciser to inhibit the drives seek not completed in one second.
Hz	(hertz) - A term for repetetive cycles-per-second.
IN	Logic signal used to generate FWD or REV for seek operations.
LDSP	(load speed) - Logic command for servo to move at 1.5 inches-per-second.
MFM	(modified frequency modulation) - A recording method that has a flux reversal during the center of a data cell time to indicate a 1 and may or may not have a flux reversal at the beginning of a cell time to indicate a 0.
MTH	(minus threshold) - Signal indicating that the position signal has produced a level more negative than a defined threshold point.
MUXENBL	(multiplexer enable) - Logic signal that enables the input interface multiplexer.
NRZ	(non-return to zero) - A recording method that does not require a flux change to signify whether it is a 1 or a 0.
OFFSETFWD	(offset forward) - Logic command to offset servo toward the spindle for read data recovery.
OGB	(outer guard band) - Signal from servo indicating that the servo head is over the outermost portion of the disc.
ONCYL	(on cylinder) - Logic signal indicating seek done and no seek error (SKRDY).
ONTRK	(on track) - Signal from servo indicating servo head is over a track.
OPENCABLE	Controller signal that causes heads to retract and deselect the drive.

OVF	(overflow) - Logic signal used to determine if FWD or REV shall be active during a seek.
PLO	(phase lock oscillator) - Signal from the servo indicating the data frequency.
PTH	(plus threshold) - Signal indicating that the position signal has produced a level more positive than a defined threshold point. Used to generate difference clocks.
PWRINI	(power initialize) - Logic signal generated during power on cycle to initialize logic.
RDY	(ready) - Logic signal indicating RETHDS and fault are not active, and the sequence 30-second timer has timed out.
RDYI	(ready indicator) - Logic signal to LED front panel display to indicate the unit is ready.
READ	Logic command for read circuit to read data from the disc.
RETMA	Radio Electronics and Television Manufacturers Association.
REV	(reverse) - Logic command for servo to move away from the spindle.
RESTORE	Logic command for servo to return to cylinder 000 and to reset HAR to 00.
RETHDS	(retract heads) - Logic command to the servo to go to the outer most position over the head landing zone of the disc.
R/FAULT	(reset fault) - Logic signal to reset the fault latches.
RPM	(revolutions-per-minute) - A measurement of speed.
SETCAR	(set cylinder address register) - Logic signal used to clock cylinder address into the CAR.
SETCYLTAG	(set cylinder tag) - Logic signal to initiate seek operation.
SETHDTAG	(set head tag) - Logic signal used to select heads.

SEEKEND	(seek end) - Logic signal indicating a seek operation has terminated.
SKSTRT	(seek start) - Logic term used to initiate a seek.
SKRDY	(seek ready) - Logic signal generated when a seek is done, provided there are no seek errors.
SLND DRIVE	(solenoid drive) - Logic signal supplying positive voltage for the disc brake and carriage lock solenoids.
SPINBRKRLSD	(spin brake released) - Signal indicating the disc brake is not enabled.
STACMTR	(start AC motor) - Logic signal that turns on the solid state switch to drive the spindle motor.
ST0	(state 0) - Logic term that commands reverse servo at load speed.
ST1	(state 1) - Logic term that commands forward servo at load speed.
ST2	(state 2) - Logic term that commands track follow.
ST3	(state 3) - Logic term that commands either forward or reverse seek.
/ETESTMODE/	Signal generated by Reflex II exerciser when unit under exerciser control. It disables the bus and tag interface lines from the controller.
TPI	(tracks-per-inch) - A measurement of the density of data.
TRKFL	(track follow) - Logic command for servo head to track on disc servo track.
UNITSELD	(unit selected) - Signals indicate the unit has been selected.
UPTOSP/	(up-to-speed) - Signal from servo board indicating that the disc is spinning at full speed.

WRT	(write) - Logic command to write circuit to write data on the disc.
WRTPROT	(write protected) - Signal generated from write protect switch to prevent a write function from occurring.
WRENBLI	(write enable indicator) - Logic signal to LED on front panel to indicate the write protect switch is not active.
WRDSBLSW	(write disable switch) - Signal from write protect switch preventing write function to occur.