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SUBJECT: CORE DRIVERS - MODEL V AND MODEL VI
Applications, Limitations, and Modifications

To: David R. Brown

From: J. D. Childress

Date: April 1, 1954

Abstract: (This memorandum supersedes Engineering Note E-523.¹) The Model V and Model VI Core Drivers are standard test units which generate rectangular wave current pulses of variable amplitude, rise time, and duration. Model V supplies pulses negative-going from ground; Model VI, positive-going from ground.

1.0 Specifications

1.1. Dimensions:

5-1/4 x 5 x 19 inches for rack mounting.

1.2. Circuits:

Monostable multivibrator (5965)
Inverter-amplifier (1/2 - 5687)
Clamper (1/2 - 6AL5)
Cathode Follower (1/2 - 5687)
Current Amplifier (4 - 6CD6's)

1.3. Input:

Standard 0.1 μ sec pulses, -13 to -30 volts

1.4. Output:

Shape - rectangular
Rise time - less than 0.15 μ sec, and 0.2 μ sec to 1 μ sec in two overlapping ranges
Duration - less than 1 μ sec to greater than 40 μ secs²
Amplitude - variable from 0 to 1.2 amps
Output impedance - greater than 100 Ω for Model V and less than 10 Ω for Model VI

1. Boyd, Harold W., "Core Drivers - Model V and Model VI," MIT Digital Computer Laboratory Engineering Note E-523, February 10, 1953.

2. See Section 2.1.

1.5. Duty Factor:

Less than 40 percent or less than $\frac{40}{\text{output current in amps}}$ percent, whichever is smaller³

1.6. Power Requirements: (approximate during pulse)

Voltage	Model V	Model VI
+150 volts	0	0.07 to 2.0 amps
-150 volts	0.03 to 2.0 amps	0
-300 volts	0.04 amps	0.04 amps
6.3 volts, AD	11.5 amps	11.5 amps

Use separate filament supplies, center tap floating, for each type driver.

2.0 Operation

The Core Drivers (schematics C-52170 - Model V and C-52643 - Model VI, Figures 1 and 2, respectively) are shown in block diagram in Figure 3. The drivers have five stages--monostable multivibrator, inverter-amplifier, clamper, cathode follower, and current amplifiers.

2.1. Monostable Multivibrator:

The monostable multivibrator is labeled "monostable" and "bistable" because of the two options in the use of the stage. In "monostable" operation, the duration of the negative gate output to the inverter amplifier is determined by the network of C-2 (C-3), R-2, and CR-3 and is variable by the Duration Coarse and Duration Fine controls from less than 1 μ sec to greater than 40 μ secs; in "bistable" operation, the duration is fixed at greater than 40 μ secs. The duration of the gate from the multivibrator determines the duration of the output current pulse.

The multivibrator is set by a standard 0.1 μ sec pulse, amplitude -13 to -30 volts, into J1-set and can be cleared in both "monostable" and "bistable" operation by a standard 0.1 μ sec pulse, amplitude -13 to -30 volts, into J2-clear.

It is recommended that the Core Drivers be operated in the "monostable" mode whenever the duty factor is less than 40 percent. For use with a "clear" input, the Duration Coarse and Duration Fine controls are set for a pulse duration slightly greater than desired; then the multivibrator is "cleared" by a delayed pulse into J2-clear. The delay of the "clear" trigger is adjusted for exactly the pulse duration desired.

3. See Section 2.1. and 2.5.

The duty factor of the multivibrator is less than 75 percent in "bistable" operation, less than 40 percent in "monostable" operation.

2.2. Inverter-amplifier:

The negative gate from the multivibrator cuts off the normally conducting inverter-amplifier. The plate of the tube rises with a time constant depending on the plate to ground capacitance and the plate load resistance. The rise time of the plate of the inverter-amplifier determines the rise time of the output current pulse. With the Rise Time Coarse set on "short", the rise time of the output pulse is less than 0.15 μ sec, but is not variable with this setting; with the Rise Time Coarse set on either "medium" or "long", the rise time can be varied with the Rise Time Fine control from less than 0.2 μ sec to greater than 1 μ sec in overlapping ranges.

Since the latest changes (6052 and 6118), the inverter-amplifier stages of the two drivers differ. The plate load resistor has been decreased and a small inductance added in this stage of the Model VI to decrease the rise time of the output pulse. Also, in the Model VI the voltage on the plate with the tube conducting has been lowered so that the output tubes are held cut off even when their cathodes are driven 70 volts negative.

2.3. Clamper:

The plate of the inverter-amplifier rises to be clamped to a level determined by the setting of the Amplitude control (R-20). This clamping controls the amplitude of the output current pulse; the amplitude is variable from 0 to greater than 1.2 amps, the upper limit depending on the quality of 6CD6's.

There is a 0.25 μ sec condenser from the center arm of R-20 to ground (C-11 in Model V, C-14 in Model VI). This condenser lowers the effective impedance of the clamp voltage to give the output waveform in Figure 4a. Without the condenser, the waveform is shown in Figure 4b. The break in the rise (indicated by the arrow) is the point at which the diode begins to clamp; the further rise is caused by the clamp current affecting the clamp voltage.

The addition of the condenser to the center arm of R-20 has made the circuit pulse duration sensitive and prf sensitive. For long pulse durations, the clamp current causes the clamp voltage to rise, thereby increasing the output current--see Figure 4c. The time constant of the circuit is such that the current pulse changes less than 0.25 percent per microsecond duration. As the prf is increased, the average value of the clamp voltage increases; therefore the current pulse amplitude increases. For the burst of high prf pulses, the current pulses "grow" along the sequence--see Figure 4d.

2.4. Cathode Follower:

The cathode follower is used to match impedance between the inverter-amplifier and the current amplifier.

2.5. Current Amplifier:

Four 6CD6's connected in parallel form the current amplifier (pentode amplifier in the Model V and pentode cathode follower in the Model VI). The maximum amplitude of the output pulse is greater than 1.2 amps, even with marginal tubes.

The current output of the Core Drivers is limited by the screen dissipation of the 6CD6's. The maximum duty factor for four 6CD6's in the output stage is given:

$$\text{Duty factor} = \frac{40}{\text{output current in amps}} \text{ percent.}$$

A Screen Current Warning lamp gives a rough indication of the screen dissipation; for rated operation, this lamp should not glow. Note that the duty factor of the driver as a whole depends on the duty factors of both the multivibrator⁴ and the current amplifier and is equal to the smaller of the two, see Figure 5.

The output impedance of the current amplifier is a function of the current pulse amplitude and of the external load impedance. For an external load impedance of less than 100Ω (including 50Ω current measuring resistor) and output current less than 1.2 amps, the output impedance of the Model V is greater than 100Ω; of the Model VI, less than 10Ω. Note that for smaller currents, the Model V becomes more like a current source; the Model VI, more like a voltage source.

3.0 Applications, Limitations, and Modifications

The Core Drivers are designed particularly for the application of ferrite memory core testing. The stringent specifications for this application are as follows:

- Shape - rectangular with top "flat" within 0.5 percent, no overshoots
- Rise Time - 0.2 μsec, smooth with a sharp break at the top
- Duration - 2 to 3 μsec
- PRF - less than 20 kc
- Amplitude - less than 1.2 amps

The Core Drivers have faults and limitations as discussed in Section 2. For use in other applications, modifications may be necessary. A number of possible requirements for other applications and the proper modifications are listed below.

1. Decrease rise time to about 0.06 μsec - reduce plate load resistor of inverter-amplifier and/or add small inductor.

2. Long pulse duration without "droop" - increase the value of the condenser in the clamp circuit or, if the rise shape is not too important, remove it.
3. Increase output current amplitude - raise the clamp voltage or remove the condenser in the clamp circuit to increase the output of a single driver to about 2 amps.
4. Improve current source characteristics of the Model VI - change C-14 so that it is connected between the clamp voltage and the cathodes of the 6CD6's in the current amplifier. A second method is to remove C-14, replace R-37 with a 10,000 Ω potentiometer (rheostat connected), and tie the junction of R-37 and R-20 to the cathodes of the 6CD6's. With this change, R-37 (pot) would have to be adjusted for zero steady current (driver not triggered) output.
5. Improve life characteristics of the Model VI - bias the filament power supply at -90 volts or bring out separately the filaments of the 5687 and bias them at -200 volts. This is recommended for experimental or test assemblies in which Model VI's are used for long periods of time.

4.0 Conclusions

The Core Drivers work quite well in the application for which they are designed. They still have faults and idiosyncracies and must be modified for other uses.

The Model V is a better driver than the Model VI and is to be used instead of the Model VI whenever possible.

Signed



James D. Childress

Approved



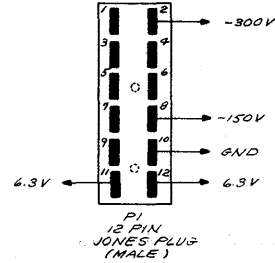
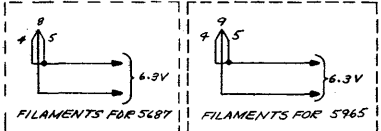
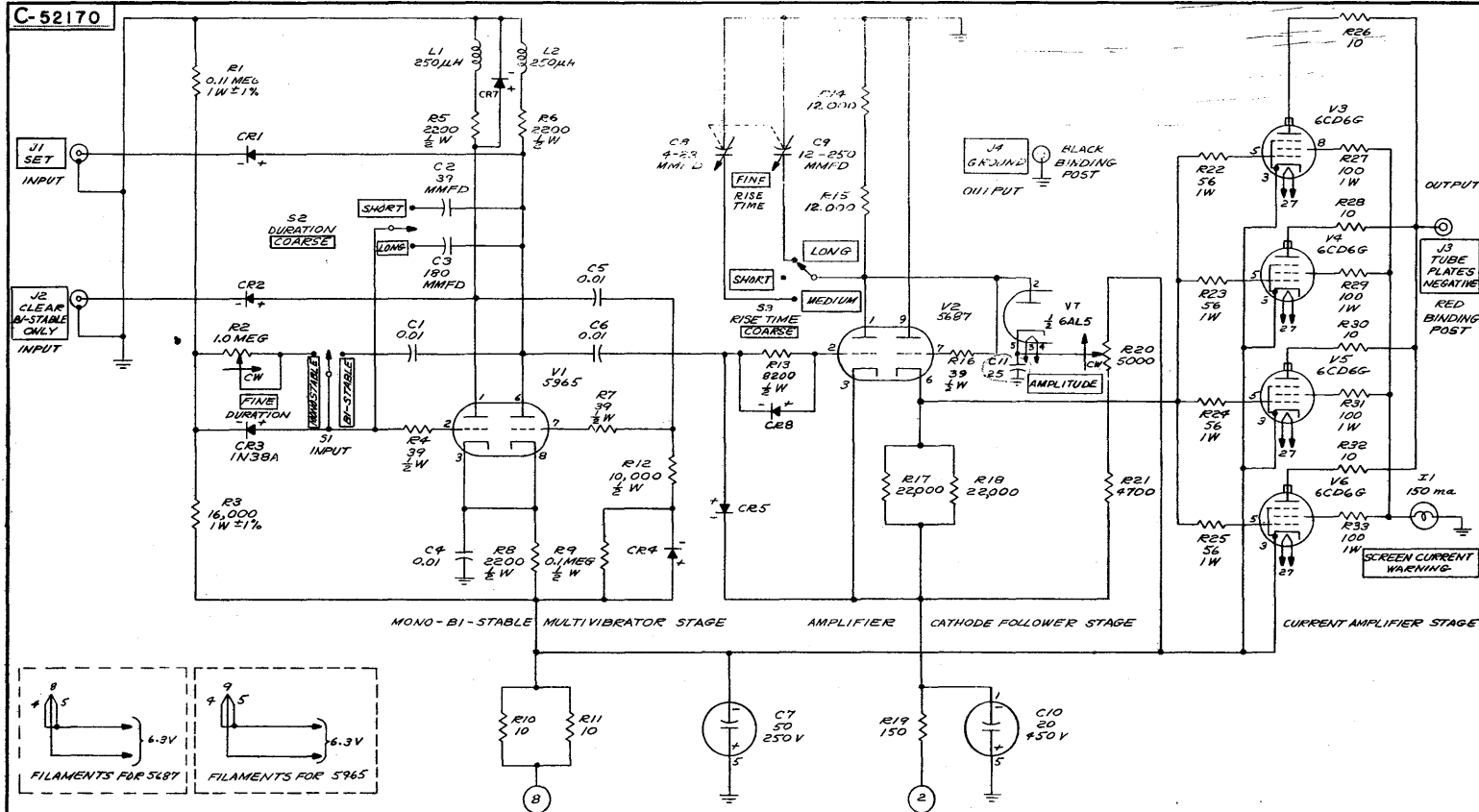
David R. Brown

JDC/jk

Drawings attached:

Figure 1 C-52170
 Figure 2 C-52643
 Figure 3 B-58376
 Figure 4 A-58374
 Figure 5 A-58375

cc: Test Equipment Committee
 Group 63 Staff
 Magnetic Memory Section - Group 62



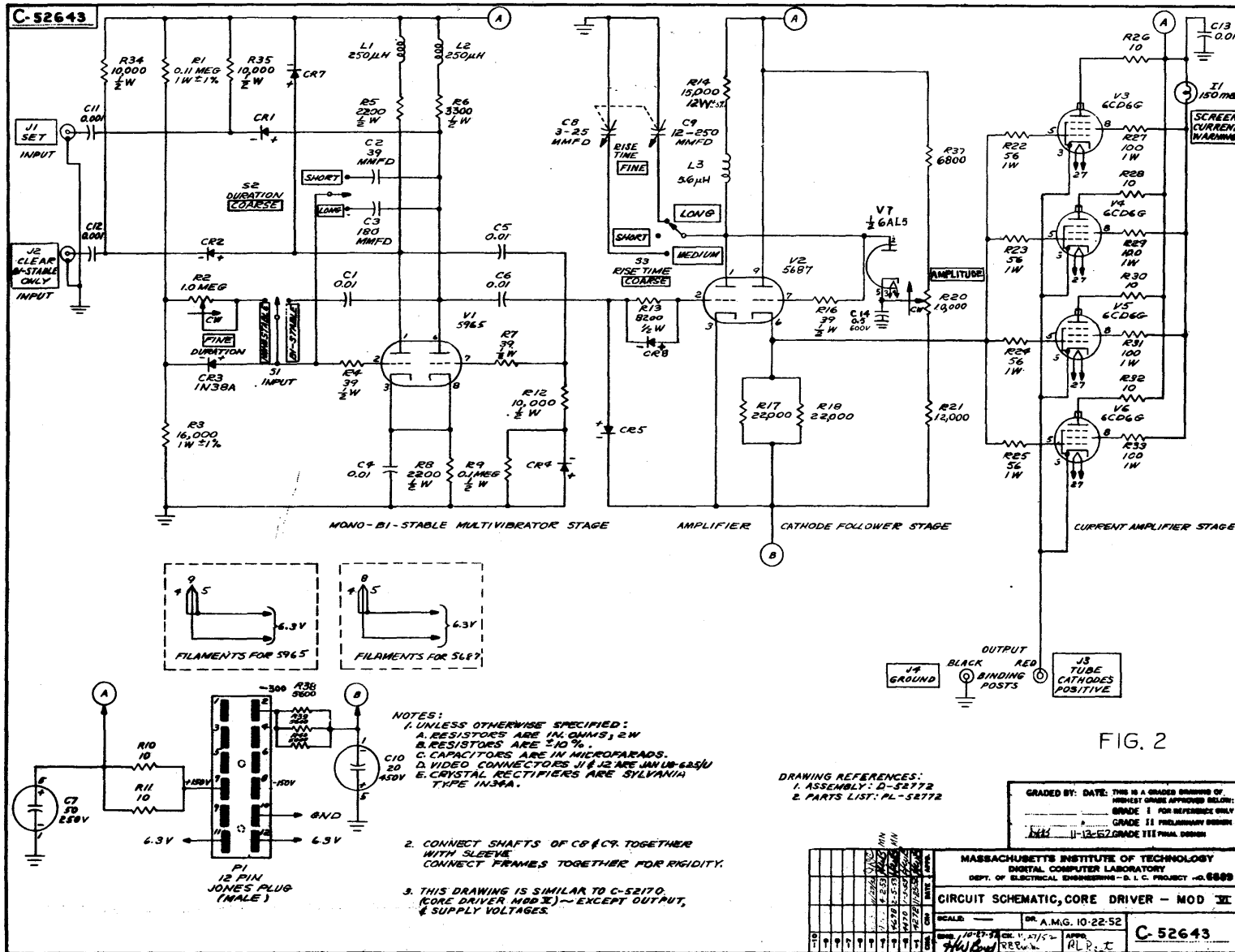
- NOTES:
- UNLESS OTHERWISE SPECIFIED:
 A. RESISTORS ARE IN OHMS; 2W.
 B. RESISTORS ARE 10%
 C. CAPACITORS ARE IN MICROFARADS.
 D. VIDEO CONNECTORS J1 & J2 ARE JANUG-200/U
 E. SUPPLY VOLTAGES.
 E. CRYSTAL RECTIFIERS ARE SYLVANIA
 TYPE IN38A.
 - USE SEPARATE FILAMENT SUPPLY OR
 ISOLATION TRANSFORMER
 - CONNECT SHAFTS OF CS #C9 TOGETHER
 WITH SLEEVE.
 CONNECT FRAMES TOGETHER FOR RIGIDITY.
 - THIS DRAWING IS SIMILAR TO C-520+3
 (CORE DRIVER MOD VI) - EXCEPT OUTPUT
 IS SUPPLY VOLTAGES.
 - TITLE OF IDENTICAL ALTERNATE UNIT IS
 "CURRENT-PULSE GENERATOR (NEGATIVE)."

DRAWING REFERENCES:
 1. ASSEMBLY: D-52622
 2. PARTS LIST: PL-52622

FIG. 1

DESIGNED BY: DATE: THIS IS A GRADED DRAWING OF
 HIGHEST GRADE APPROVED BELOW:
 GRADE I FOR REFERENCE ONLY
 GRADE II PRELIMINARY DESIGN
 GRADE III FINAL DESIGN

MASSACHUSETTS INSTITUTE OF TECHNOLOGY									
DIGITAL COMPUTER LABORATORY									
DEPT. OF ELECTRICAL ENGINEERING - D. I. C. PROJECT NO. 6889									
CIRCUIT SCHEMATIC, CORE DRIVER - MOD X, TE									
REV.	DATE	BY	CHK.	APPR.	SCALE	DR.	DATE	NO.	OF
1	9/25/52	WJ	WJ	WJ		CRD	9/25/52		
2	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
3	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
4	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
5	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
6	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
7	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
8	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
9	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
10	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
11	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
12	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
13	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
14	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
15	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
16	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
17	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
18	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
19	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
20	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
21	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
22	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
23	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
24	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
25	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
26	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
27	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
28	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
29	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
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33	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
34	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
35	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
36	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
37	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
38	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
39	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
40	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
41	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
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44	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
45	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
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47	10/1/52	WJ	WJ	WJ		CRD	9/25/52		
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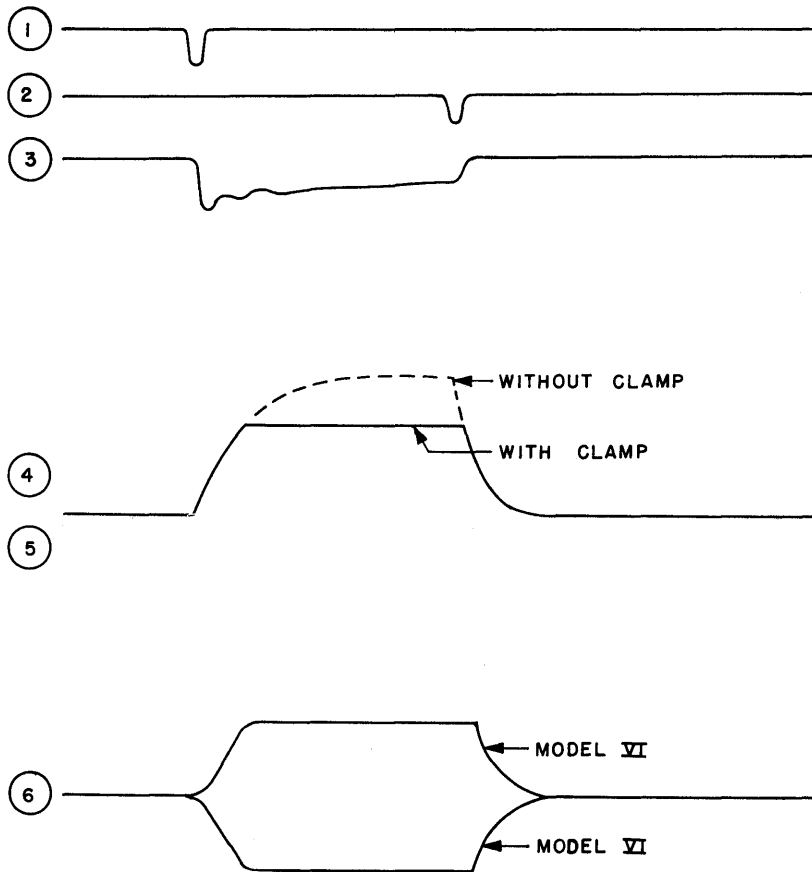
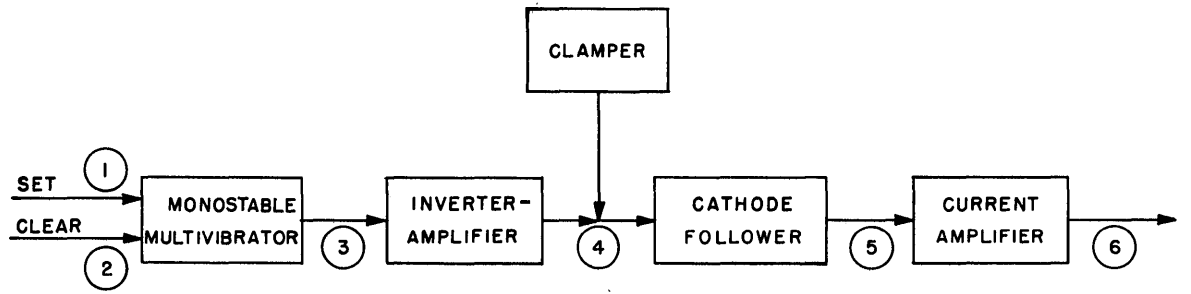


FIG. 3

BLOCK DIAGRAM AND WAVEFORMS
OF THE CORE DRIVERS

B-58376

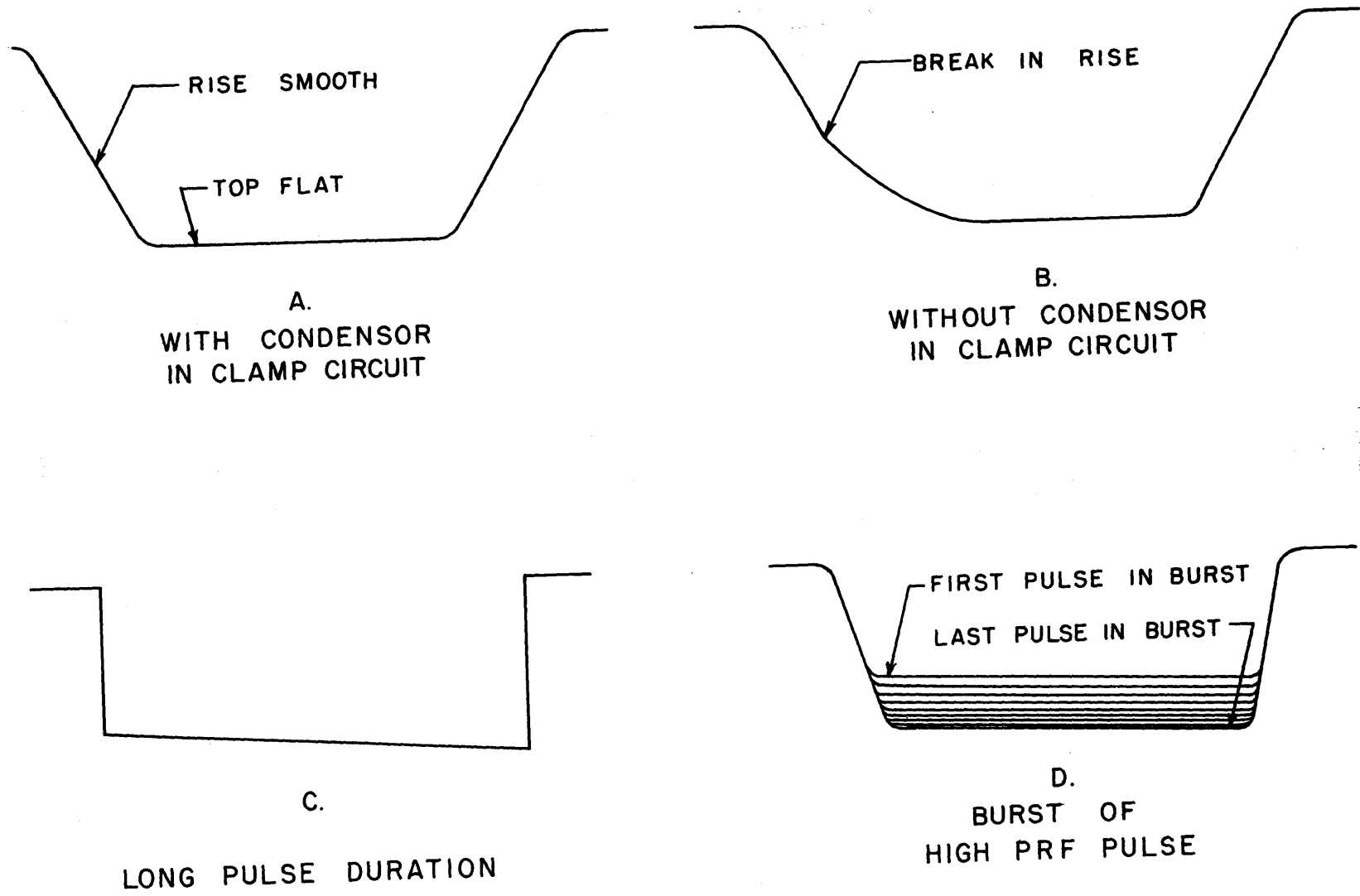


FIG. 4
OUTPUT WAVEFORMS

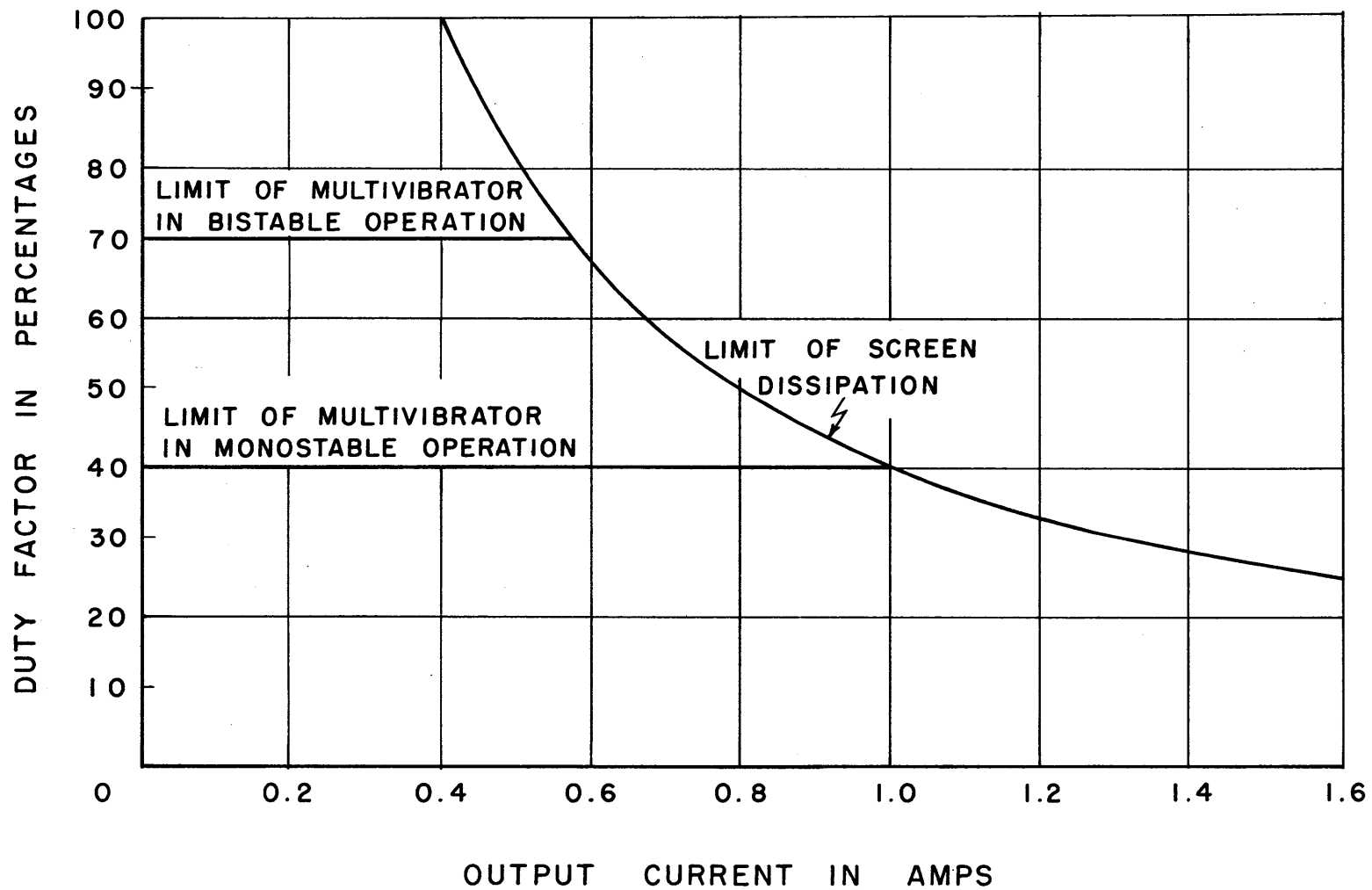


FIG. 5
DUTY FACTOR