MOTOROLA

MVME110/A1

FEBRUARY 1984

ADDENDUM

TO

MVME110-1 VMEmodule MONOBOARD MICROCOMPUTER

USER'S MANUAL

(MVME110/D2)

This addendum makes minor corrections to your MVME110/D2 user's manual. The black change bar in the margin indicates the area of inserted, revised, or deleted material.

Insert change pages attached to this addendum into your MVME110/D2 user's manual. Make certain that the pages you are replacing are removed from your manual. This page of the addendum should be placed after the user's manual title page and used as a record page of the changes made to your manual. Pages affected by this addendum are as follows:

iii/iv
1-3/1-4
2-37/2-38
4-9/4-10
4-19/4-20
5-3/5-4
5-9 through 5-44

MICROSYSTEMS

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17364 PRINTED IN USA (2/84) MPS 3M

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- A local-memory-decode PROM allows for contiguous addressing between local memory and global VMEbus memory.

- Two user-configurable jumpers which may be read by the software.

- Module status and control registers.

- An MC6840 programmable timer module provides three independent 16-bit counters/timers. Timer outputs may be cascaded for 32- or 48-bit operation.

    - Watchdog timer - uses two MC6840 timers and allows user to generate NMI and RESET if processor fails to periodically restart the counter.

- Local bus timeout.

- Interrupt handler for up to seven VME interrupt levels plus up to seven local interrupt levels. The interrupt levels of the seven local interrupt sources are user-selectable. The ABORT pushbutton switch and VME ACFAIL* line are connected to non-maskable interrupt level seven.

- The RESET and ABORT pushbutton switches may be enabled or disabled by on-board jumpers.

- Board status indicators.

    - Red FAIL LED indicates module failure.

    - Red HALT LED indicates MPU is halted.

    - Green RUN LED indicates MPU is running.

1.3 SPECIFICATIONS

General specifications for the VME110 are listed in Table 1-1.

TABLE 1-1. VME110 Specifications

CHARACTERISTIC	SPECIFICATIONS
Power requirements (with all eight sockets unpopulated)	+5 Vdc (± 5%), 2.1 A (typical), 2.4 A (max.) +12 Vdc (± 5%), 25 mA (typical), 50 mA (max.) -12 Vdc (± 5%), 25 mA (typical), 50 mA (max.) (see NOTE)
Power requirements (with all eight sockets populated)	+5 Vdc (± 5%), 2.6 A (typical), 3.0 A (max.) +12 Vdc (± 5%), 25 mA (typical), 50 mA (max.) -12 Vdc (± 5%), 25 mA (typical), 50 mA (max.) (see NOTE)
Temperature	
Operating	0° to 70° C
Storage	-55° to +85° C
Relative humidity	0% to 90% (non-condensing)
Physical characteristics	Double-high VME board
PC board only	
Height	9.2 in. (233 mm)
Depth	6.3 in. (160 mm)
Thickness	0.662 in. (16.77 mm)
PC board with connectors and front panel	
Height	10.3 in. (262 mm)
Depth	7.4 in. (188 mm)
Thickness	0.80 in. (20.3 mm)

NOTE: The currents at +12 Vdc and -12 Vdc are specified for the MVME110 module with the serial port connectors open. The actual required values depend on the load of the RS-232C ports. All serial port outputs are current-limited to sink or source 12 mA (max) each.

1.4 GENERAL DESCRIPTION

The VME110 is a high performance processing module, designed to function as either a stand-alone microcomputer, as a single CPU/system controller in a VMEbus system, or as one of several CPU elements in a multiprocessor VMEbus configuration. This module features the MC68000 16-bit microprocessor with a total address range of 16 megabytes. Sockets are provided to accommodate up to 256K bytes of user-supplied memory. Full support is provided for the I/O Channel which provides access to a large variety of peripheral and industrial I/O functions. An on-board serial communications port is also included.

TABLE 2-27. Map Decoder PROM Hex Codes

HEX CODE	SELECTED DEVICE
0	Illegal
1	RAM in socket pair 2
2	RAM in socket pair 3
3	RAM in socket pair 4
4	Illegal
5	WRITE PROTECTED RAM in socket pair 2
6	WRITE PROTECTED RAM in socket pair 3
7	WRITE PROTECTED RAM in socket pair 4
8	PROM in socket pair 1
9	PROM in socket pair 2
A	PROM in socket pair 3
B	PROM in socket pair 4
C	VMEbus
D	VMEbus
E	VMEbus
F	VMEbus

NOTE: Codes 0 and 4 are illegal because RAM may not be installed in socket pair 1. (The processor reads the power-on vector from the PROM's in these sockets.)

Memory chips of different sizes may be used as long as each socket pair contains a matching set. Illustrated in Figure 2-33 is an example configuration which has 8K ROM chips installed in socket pair 1, 4K ROM chips in socket pair 3, and 2K RAM chips in socket pairs 2 and 4. In this case, the memory chips have been arranged so that they form a contiguous 32K block of memory. The two 8K ROM chips in socket pair 1 are placed at the lowest address by programming a hexadecimal "8" into the corresponding decoder PROM locations. The 4K PROM's are placed with hexadecimal "A". The 2K RAM's in socket pair 2 correspond to a hexadecimal "1", and the write protected 2K RAM's in socket pair 4 correspond to the hex codes of "7" and "3".

Because the rest of the local memory block is not needed, the decoder PROM locations are programmed with a hex "F". This causes the board to access the VMEbus whenever that area of the map is addressed. If there is a memory board on the VMEbus which contains that address, it will be contiguous with the local memory.

It should be noted that the socket pairs do not necessarily appear in the map in order (socket pairs 1, 3, 2, 4). The placement of the chips into the 28-pin socket pairs does not govern their placement in the memory map. There are some restrictions, however. In the example just described, if the user wanted to rearrange the chips in the order 1, 2, 3, 4, he would run into difficulty. This is because the 8K of memory in socket pair 3 has to be placed on a 4K boundary. Therefore, it could not be contiguous with the 4K of memory in socket pair 2 below it in the memory map.

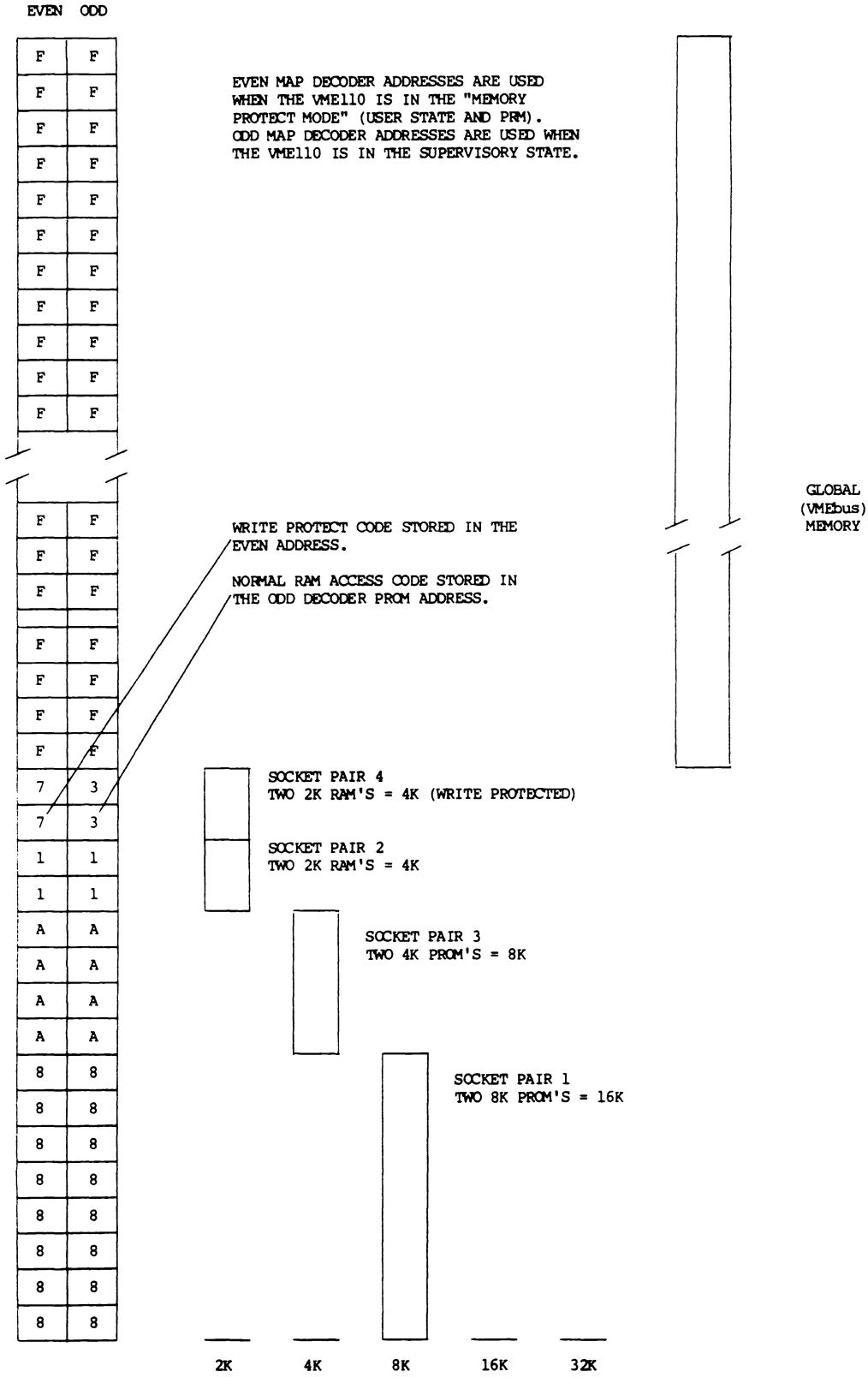


FIGURE 2-33. Map Decoder PROM Example

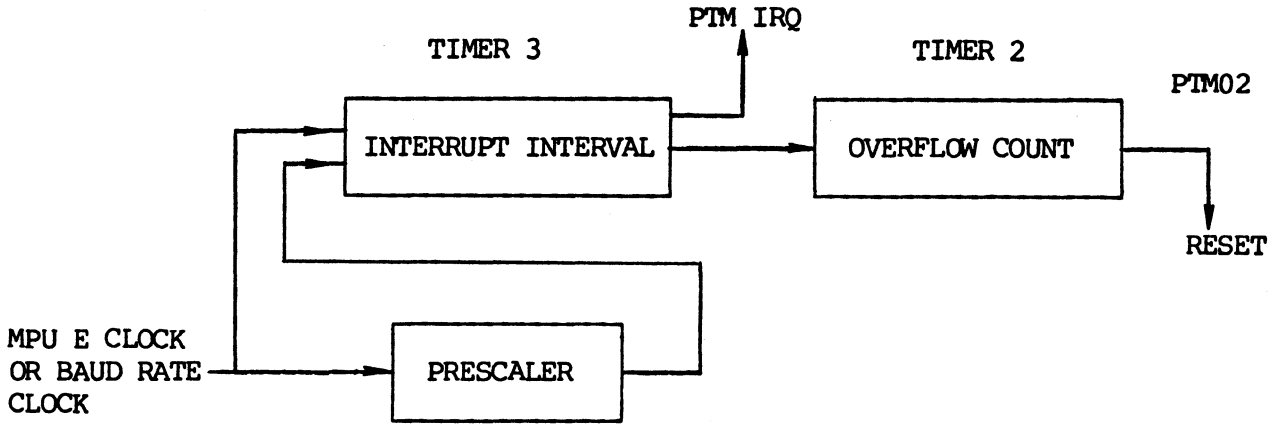


FIGURE 4-5. PTM Watchdog Timer Configuration

4.3.4.2 Asynchronous Communication Interface Adapter (ACIA). The Serial Port consists of an MC6850 ACIA, RS-232C connector and interface, and baud rate select circuitry. The port is configured as Data Communication Equipment (DCE) to be connected to Data Terminal Equipment (DTE). Table 5-3 lists the serial port connector signals. The user should refer to the ACIA data sheet for detailed register descriptions.

The following paragraph covers any special initialization procedures or considerations.

The user should perform a master reset to the ACIA after each MPU reset to ensure proper ACIA initialization. The count divide select should be selected for divide by sixteen. The ACIA Request To Send ($\overline{RTS}$) signal controls the serial port Clear To Send signal (CTS). Normally, the $\overline{RTS}$ signal should be low to allow the terminal to transmit data. If the user wishes to implement flow control, the $\overline{RTS}$ signal may be set high. This causes the CTS signal to the terminal to indicate an off condition and inhibit data transmission. The ACIA Data Carrier Detect ($\overline{DCD}$) input is permanently set low. The ACIA $\overline{CTS}$ signal is low whenever the terminal indicates it is ready.

Two optional capacitors may be installed at C43 and C44 for controlling the slew rate of the Transmit Data (TXD) and Data Terminal Ready (DTR) signals. In noisy environments, the addition of the capacitor allows the rejection of high frequency noise. Refer to the MC1489 data sheet for additional information.

4.3.4.3 Module Control Register (MCR). Memory map address FE8021 is reserved for addressing the MCR (U37).

The MCR contains six bits for controlling various board functions as described below. The MCR may only be written while in the supervisor state. A bus error will be issued if a write attempt is made while in the user state.

Upon initialization, the MCR is reset to $10, which illuminates the FAIL indicator.

7	6	5	4	3	2	1	0
PRM	WDE	SFIE	FAIL	0	0	BRC1	BRC0

PRM - PROTECT MODE
0 Protect Mode disabled.
1 Protect Mode enabled.

WDE - WATCHDOG ENABLE
0 Watchdog Timer disabled.
1 Watchdog Timer enabled.

SFIE - SYSTEM FAIL INTERRUPT ENABLE
0 interrupt disabled.
1 interrupt enabled.

FAIL - 0 No Failure. The FAIL indicator is extinguished and the VMEbus SYSFAIL* signal is deactivated.

1 Failure. The FAIL indicator is illuminated and the VMEbus SYSFAIL* signal is activated.

BRC1, BRC0 - BUS RELEASE CONTROL BITS

BRC1	BRC0	MODE SELECTED
0	0	ROR - Release on request
0	1	RBC - Release on bus clear
1	0	RWD - Release when done
1	1	RNE - Release never

Refer to paragraph 4.3.9.2 for details of these release modes.

4.3.4.4 Module Status Register (MSR). The MSR (U52) is addressed using address FE8031 of the memory map.

The MSR allows the user to read the current level of ACFAIL*, SYSFAIL*, and the user configurable jumpers. The MSR is a read-only register. Any write attempt to this register results in a bus error.

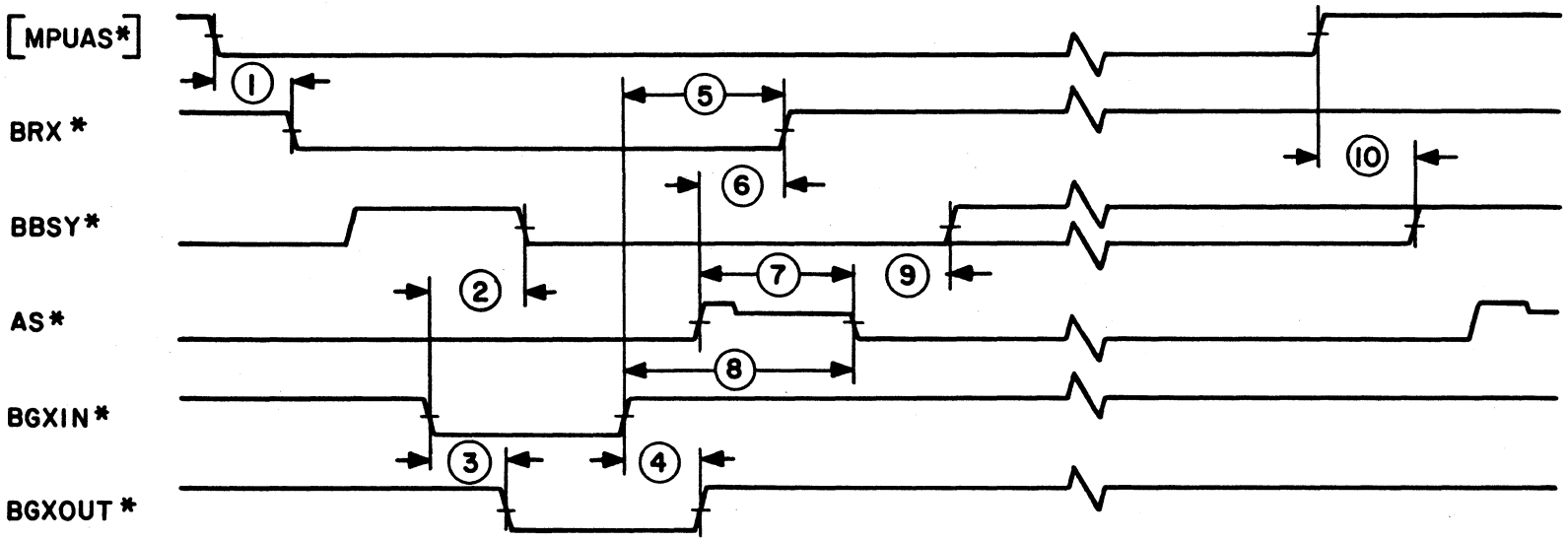
7	6	5	4	0-3
ACF	SF	SSB1	SSB0	UNDEFINED

ACF - AC FAILURE
0 VMEbus ACFAIL* false.
1 VMEbus ACFAIL* true.

SF - SYSTEM FAILURE
0 VMEbus SYSFAIL* false.
1 VMEbus SYSFAIL* true.

SSB1 - SOFTWARE STATUS BIT 1
0 Header J5 pins 3 and 5 connected.
1 Header J5 pins 1 and 3 connected.

SSB0 - SOFTWARE STATUS BIT 0
0 Header J5 pins 4 and 6 connected.
1 Header J5 pins 2 and 4 connected.



NOTE: IN THE SIGNAL NAMES ABOVE, X IS THE ARBITRATION REQUEST LEVEL SELECTED ON HEADERS J2 AND J3.

FIGURE 4-9. VMEbus Requester Timing Diagram

ROR - Release on Request. Once bus mastership has been granted, it is released when any potential bus master requests use of the bus. This mode is selected at reset and is intended for systems in which the VME110 is the primary user of the bus.

RWD - Release when Done. Once bus mastership has been granted, it is immediately released shortly after the beginning of the cycle. Arbitration of the next bus cycle may occur concurrently with the completion of the present bus cycle. Arbitration will be required on each VME110 bus cycle. This mode is useful to guarantee quick bus availability to other bus masters in the system.

The chart below demonstrates how MPU performance and VMEbus performance are affected by the various release modes.

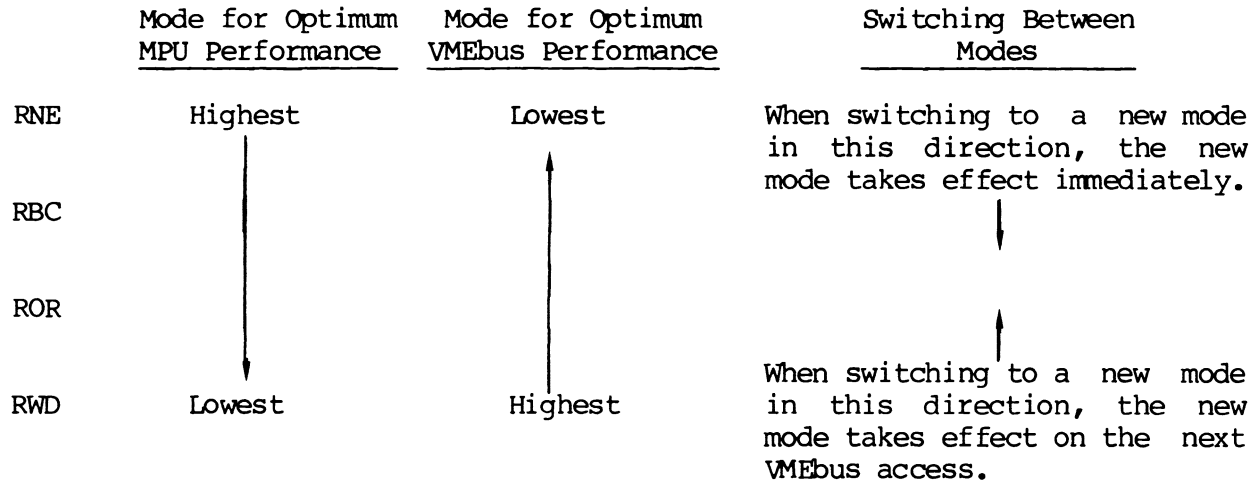


TABLE 4-6. Requester Timing

NO.	CHARACTERISTIC	TYP	MAX
1	[MPUAS*] low to BRX* low	60	70
2	BGXIN* low to BBSY* low	110	125
3	BGXIN* low to BGXOUT* low	35	50
4	BGXIN* high to BGXOUT* high	20	30
5	BGXIN* high to BRX* released	95	120
6	AS* high to BRX* released	60	95
7	AS* high pulse width	115	150
8	BGXIN* high to AS* low	130	175
9	AS* low to BBSY* high (RWD Mode)	45	65
10	[MPUAS*] high to BBSY* high (ROR and RBC Modes) (See Note)	35	50

NOTE: In the ROR and RBC modes, if the release condition is present, the bus will be released within time #10 after the completion of the current MPU cycle. The bus will also be released within time #10 after an MPU halt condition.

TABLE 5-1. VMEbus Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A24	A07	ADDRESS bus (bit 7) - One of 23 three-state driven output lines which specify an address in the memory map (see Figure 4-3).
A25	A06	ADDRESS bus (bit 6) - Similar to pin A24.
A26	A05	ADDRESS bus (bit 5) - Similar to pin A24.
A27	A04	ADDRESS bus (bit 4) - Similar to pin A24.
A28	A03	ADDRESS bus (bit 3) - One of 23 three-state driven output lines which specify a memory address. During an interrupt acknowledge cycle, address bus lines 1-3 are used to indicate the interrupt level which is being acknowledged.
A29	A02	ADDRESS bus (bit 2) - Similar to pin A28.
A30	A01	ADDRESS bus (bit 1) - Similar to pin A28.
A31	-12V	-12 Vdc power - used by logic circuits.
A32 B32 C32	+5V	+5 Vdc power - used by logic circuits.
B1	BBSY*	BUS BUSY - This bidirectional signal is driven low when the VME110 is the VMEbus master. Also an input to the arbiter to indicate that the bus may be arbitrated.
B2	BCLR*	BUS CLEAR - Input signal that causes the release of bus mastership in the RBC mode.
B3	ACFAIL*	AC FAILURE - Input signal that indicates a power failure has occurred and generates a level seven interrupt request.
B4,B6, B8,B10	BG0IN*- BG3IN*	BUS GRANT (0-3) IN - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. A grant received at the jumpered level indicates the VME110 may become the bus master. The remaining three bus-grant-in lines are connected directly to their respective bus-grant-out lines.
B5,B7, B9,B11	BG0OUT*- BG3OUT*	BUS GRANT (0-3) OUT - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. When a bus-grant-in is received at the jumpered level and the MPU is not awaiting bus mastership, the bus-grant-out signal is true on the respective level.

TABLE 5-1. VMEbus Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B12-15	BR0*-BR3*	BUS REQUEST (0-3) - The bidirectional bus request of the jumpered level is true when the MPU requires bus mastership. When one or more of the bus request lines is true in the ROR mode, bus mastership is released. When the VME110 is the system controller, bus request level three is monitored by the arbiter.
B16-19	AM0-AM3	ADDRESS MODIFIER (bits 0-3) - Similar to pin A23.
B21	SERCLK	Not used.
B22	SERDAT	Not used.
B24-30	IRQ7*-IRQ1*	INTERRUPT REQUEST (7-1) - Seven prioritized interrupt request inputs. Jumper enabled, level seven is the highest priority.
B31	+5V STDBY	Not used.
C1-8	D08-D15	DATA BUS (bits 8-15) - Eight of 16 three-state bidirectional data lines which provide the data path between VMEbus master and slave. Similar to pins A1-8.
C10	SYSFAIL*	SYSTEM FAIL - Reflects state of FAIL bit in MCR and FAIL indicator. When enabled in MCR, this bidirectional signal generates an interrupt request.
C11	BERR*	BUS ERROR - Indicates an error has occurred during data transfer cycle. The cycle is terminated and the MPU starts exception processing. When the VME110 is the system controller, this bidirectional signal is generated when a data transfer cycle did not complete within 200 us.
C12	SYSRESET*	SYSTEM RESET - Causes a board level reset when received from the VMEbus. When system controller, a board level reset causes this bidirectional signal to be generated to the VMEbus (see Figure 4-2).
C13	LWORD*	LONGWORD - Not driven. This terminated signal remains at a high level when the VME110 is bus master.
C14	AM5	ADDRESS MODIFIER (bit 5) - This output line is not driven by the VME110. AM5 always appears as a high (true) level on the VMEbus because of the backplane termination.
C15	A23	ADDRESS bus (bit 23) - Similar to pin A24.

TABLE 5-4. VME110 Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8047B01	PWB assembly, VME110
C1-9,C13-30, C41,C42	21SW992C025	Capacitor, ceramic, .100 uF @ 50 Vdc
C10,C11, C31-40	21NW9702A09	Capacitor, ceramic, .1 uF @ 50 Vdc
C12	21NW9604A11	Capacitor, ceramic, .47 uF @ 50 Vdc, ± 20%
C43,C44	(see NOTE 1)	
C45	23NW9618A33	Capacitor, 22 uF @ 25 Vdc
DL1	01NW9804B83	Delay, 50 nsec
DL2	01NW9804C34	Delay line, triple, 70 nsec
DS1,DS2	48NW9612A34	Indicator light, red, 5 Vdc
DS3	48NW9612A38	LED, green
J1,J4,J6,J13	28NW9802D04	Header, single-row post, 3-position
J2,3	28NW9802C63	Header, double-row post, 12-pin
J5	28NW9802B21	Header, double-row post, 6-pin
J7	28NW9802E30	Header, single-row post, 4-position
J8,J9,J10, J14,J16-27	28NW9802C43	Header, double-row post, 8-pin
J11,J12	28NW9802C36	Header, double-row post, 14-pin
J15	28NW9802D88	Connector, RS-232C
P1	28NW9802E51	Connector, 96-pin plug
P2	28NW9802E05	Connector, 64-pin plug
R1,R2,R4,R6, R7,R14,R16, R18,R22	06SW-124A65	Resistor, film, 4.7k ohm, 5%, 1/4 W
R3,R19,R20	51NW9626A49	Resistor network, seven 10k ohm
R5,R15	06SW-124A37	Resistor, film, 330 ohm, 5%, 1/4 W
R8,R11,R12	51NW9626A37	Resistor network, nine 10k ohm

TABLE 5-4. VME110 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R9,10	06SW-124B22	Resistor, film, 1M ohm, 5%, 1/4 W
R13	51NW9626A41	Resistor network, nine 4.7k ohm
R17	51NW9626A76	Resistor network, six 330/470 ohm
R21	51NW9626A46	Resistor network, five 4.7k ohm
S1,S2	40NW9801A54	Switch, SPDT
U1,U35	51NW9615F38	I.C. SN74LS393N
U2	51NW9615C95	I.C. SN74S74N
U3	(See NOTE 2)	I.C. Programmed PROM
U4	51NW9615G97	I.C. MC68000G8
U5,U6	51NW9615H89	I.C. SN74LS645-1N
U7	51NW9615F10	I.C. SN74LS125AN
U8,U39,U40	51NW9615C96	I.C. SN74S04N
U9,U54	51NW9615D32	I.C. SN74S02N
U10,U48	51NW9615E91	I.C. SN74LS00N
U11	(See NOTE 2)	I.C. Programmed PROM
U12,U16,U58	51NW9615C94	I.C. SN74S00N
U13,U14, U25,U26	51NW9615F65	I.C. SN74S241N
U15	51NW9615B65	I.C. MC1455P1
U17,U49	51NW9615F41	I.C. DM74LS164N
U18,U61	51NW9615E27	I.C. 74S10PC
U19	51NW9615D26	I.C. 74S113N
U20	51NW9615A36	I.C. MC7406P
U21,U34,U38	51NW9615C21	I.C. SN74LS04N
U22	(See NOTE 2)	I.C. Programmed PROM
U23	51NW9615D31	I.C. 82S131F Programmable PROM (see NOTE 3)

TABLE 5-4. VME110 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U24,U33,U45	51NW9615F85	I.C. SN74S38N
U27	51NW9615G38	I.C. SN74LS38N
U28	51NW9615G81	I.C. SN74LS132N
U29	51NW9615E33	I.C. 74S03A
U30	(See NOTE 2)	I.C. Programmed PROM
U31	51NW9615G10	I.C. SN74LS148N
U32	51NW9615E86	I.C. SN74LS151N
U36	51NW9615E93	I.C. SN74LS14N
U37	51NW9615C29	I.C. SN74LS174N
U41	51NW9615E77	I.C. SN74LS27N
U42	51NW9615E99	I.C. SN74LS374N
U43,U44	51NW9615C22	I.C. SN74LS08N
U46	51NW9615D27	I.C. SN74S32N
U47	48AW1019B01	K1135 Dual baud rate generator
U50	51NW9615J11	I.C. SN74S140N
U51	51NW9615H53	I.C. SN74LS09N
U52,U55,U59	51NW9615F02	I.C. 74LS244N
U53	51NW9615F59	I.C. MC68B40P
U56	51NW9615B29	I.C. MC1488L
U57	51NW9615D86	I.C. MC68B50P
U60	51NW9615B30	I.C. MC1489AL
U62	51NW9615H57	I.C. SN74LS194AN
U63	51NW9615E96	I.C. SN74LS245
Y1	48AW1016B01	Crystal oscillator, 16.0 MHz $\pm$ 0.05%
	02SW990D001	Nut, hex M 2.5 x .45 x 2 (2 req'd)
	02SW990D007	Nut, hex M 2 x .4 x 1.6 (4 req'd)

TABLE 5-4. VME110 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	03SW993D110	Screw, phillips, M 2 x .4 x 10 (4 req'd)
	03SW993D210	Screw, phillips, M 2.5 x .45 x 10 (3 req'd)
	03SW993D208	Screw, phillips, M 2.5 x .45 x 8 (2 req'd)
	04SW997D003	Washer, M 2.5 x .6 (2 req'd)
	04SW999D005	Washer, flat, M 2.7 x .5 (2 req'd)
	07-W4252B01	Bracket, card mounting (3 req'd)
	09NW9811A04	Socket, I.C., DIL, 16-pin, low profile (Use at U23)
	09NW9811A09	Socket, I.C., DIL, 18-pin, low profile (Use at U47)
	09NW9811A34	Socket, I.C., DIL, 64-pin (Use at U4)
XU1-XU8	09NW9811A64	Socket, I.C., DIL, 28-pin
	09NW9811A78	Socket, I.C., DIL, 20-pin (Use at U3, U11, U22, U30)
	09NW9811A46	Socket, 4-lead crystal oscillator (Use at Y1)
	29NW9805B17	Jumper, shorting insulated (Use at J1-J14, J16-J27)
	38NW9404B97	Cap, large snap-on, black
	38NW9404C04	Cap, snap-on, red
	64-W4629B01	Panel, front, MVME100 (alternate is 64-W4301B01)
	55NW9501A10	Handle, VME, single-wide (2 req'd) (See NOTE 4)
	33-W4602B01	Nameplate, MVME110
	33-W4643B01	Nameplate, VME, blank
	43NW9002B25	Bushing, retainer, metric (2 req'd) (See NOTE 4)

TABLE 5-4. VME110 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	03NW9004B48	Screw, captive, M 2.5 (2 req'd) (See NOTE 4)
	03NW9004B49	Screw, phillips, M 2.5 x 7 (See NOTE 4)
	03NW9004B44	Screw, pan-head, M 2.5 x 16 (2 req'd) (See NOTE 4)
	33-W4365B02	Label, I.D., module

NOTES: (1) C43 and C44 are optional capacitors which are not installed but may be, at the discretion of the user. Refer to paragraph 4.3.4.2.

(2) When ordering, use number labeled on part. For programming details, see Appendix A.

(3) Must be programmed by user. Refer to paragraph 2.3.15.

(4) Used only with the part number 64-W4629B01.

5.4 SCHEMATIC DIAGRAMS

Figure 5-2 (14 sheets) contains detailed schematic diagrams of the various internal modules comprising the VME110. These schematic diagrams represent the latest design. Occasionally, minor component changes are made at the factory. Therefore, when replacing a component, always use the same value as the defective component even though the schematic diagram may indicate a different value or type.

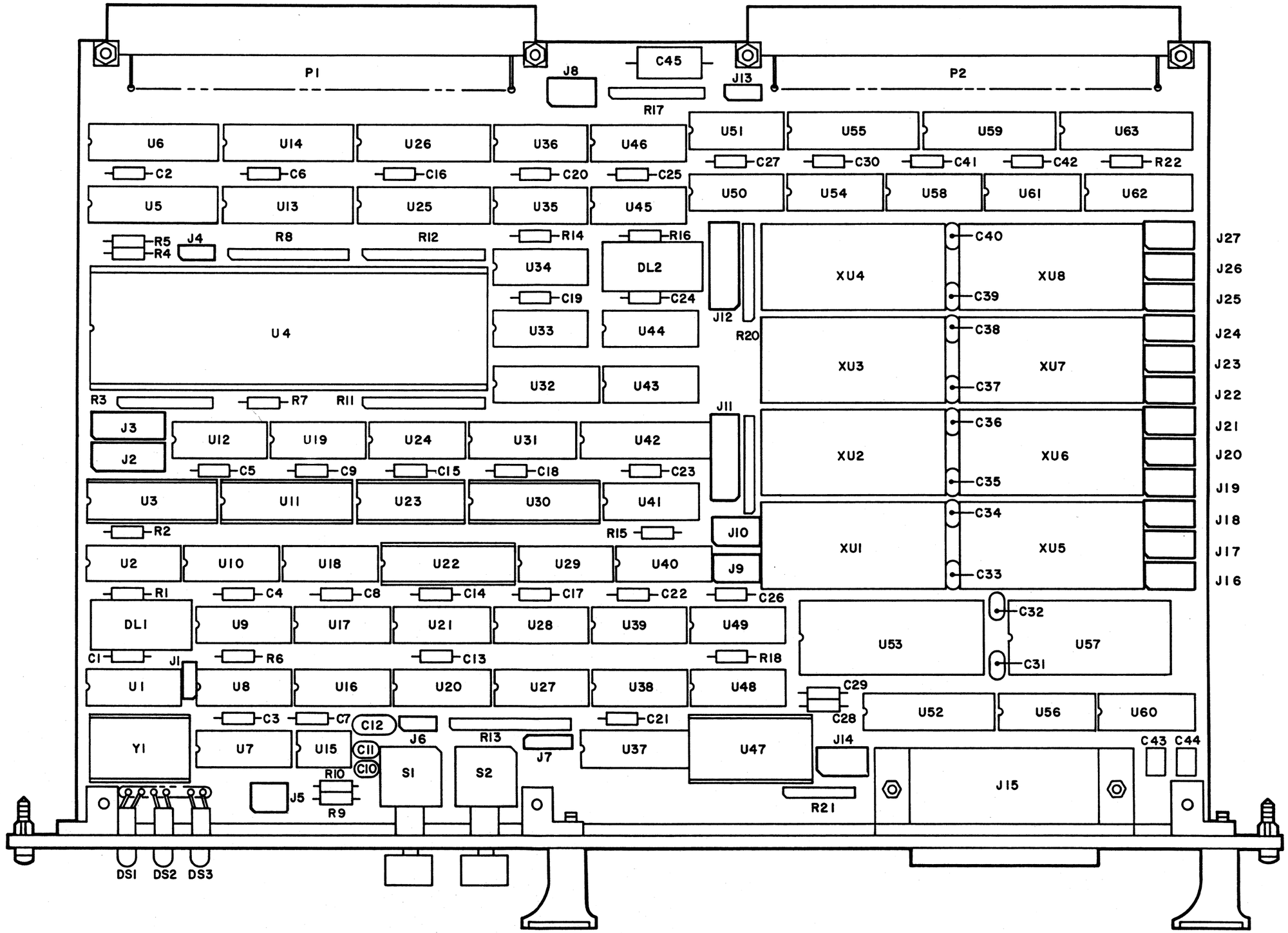


FIGURE 5-1. VME110 Module Parts Location Diagram

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3047B01.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ± 5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES – ACTIVE LOW SIGNAL.
   [] DENOTES – ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
7. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING, FOR FULL PART TYPE, REFER TO TABLE 1.
8. NOT INSTALLED,USERS OPTION.
9. NUMBERS IN PARENTHESES ARE FOR 24 PIN DEVICES. REFER TO MANUFACTURER'S CATALOGUE FOR MNEMONICS.
10. PART MOUNTED ON FRONT PANEL.

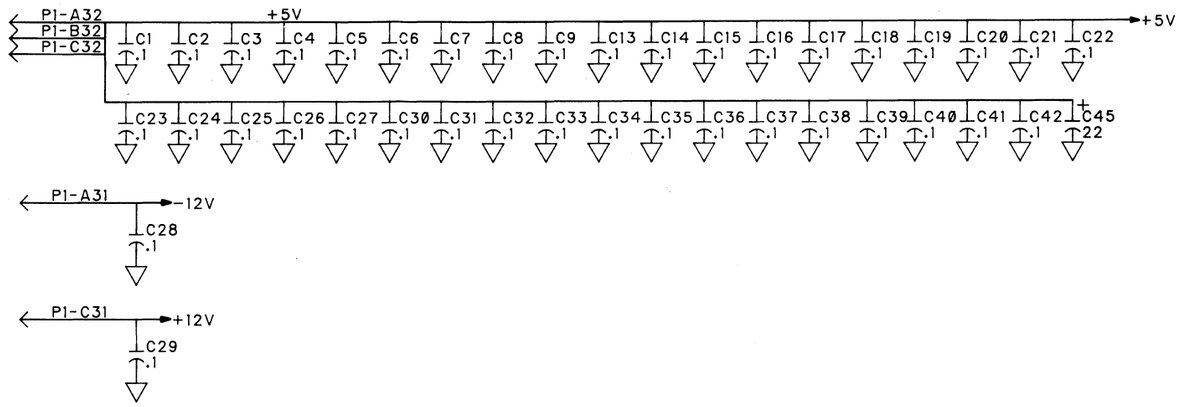
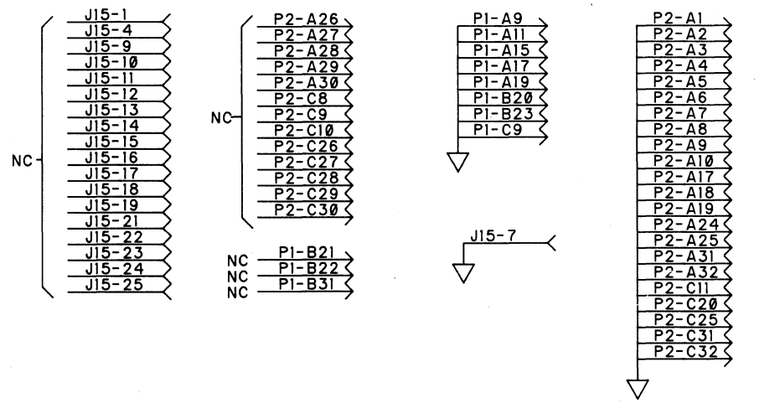


TABLE 1 (7)

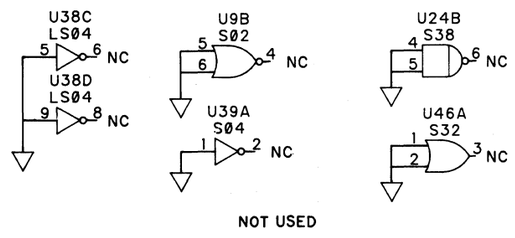
REF DES	TYPE (4)	GND	+5V	+12V	-12V
U1	74LS393	7	14		
U2	74S74	7	14		
U3	PAL16L8	10	20		
U4	MC68000L8	53,16	49,14		
U5	74LS645-1	10	20		
U6	74LS645-1	10	20		
U7	74LS125	7	14		
U8	74S04	7	14		
U9	74S02	7	14		
U10	74LS00	7	14		
U11	PAL16L8	10	20		
U12	74S00	7	14		
U13	74S241	10	20		
U14	74S241	10	20		
U15	MC1455	1	8		
U16	74S00	7	14		
U17	74LS164	7	14		
U18	74S10	7	14		
U19	74S113	7	14		
U20	7406	7	14		
U21	74LS04	7	14		
U22	PAL16L8	10	20		
U23	82S131	8	16		
U24	74S38	7	14		
U25	74S241	10	20		
U26	74S241	10	20		
U27	74LS38	7	14		
U28	74LS132	7	14		
U29	74S03	7	14		
U30	PAL16L8	10	20		
U31	74LS148	8	16		
U32	74LS151	8	16		
U33	74S38	7	14		
U34	74LS04	7	14		
U35	74LS393	7	14		
U36	74LS14	7	14		
U37	74LS174	8	16		
U38	74LS04	7	14		

TABLE 1 (7)

REF DES	TYPE (4)	GND	+5V	+12V	-12V
U39	74S04	7	14		
U40	74S04	7	14		
U41	74LS27	7	14		
U42	74LS374	10	20		
U43	74LS08	7	14		
U44	74LS08	7	14		
U45	74S38	7	14		
U46	74S32	7	14		
U47	K1135B	11	2	9	
U48	74LS00	7	14		
U49	74LS164	7	14		
U50	74S140	7	14		
U51	74LS09	7	14		
U52	74LS244	10	20		
U53	MC68B40	1	14		
U54	74S02	7	14		
U55	74LS244	10	20		
U56	MC1488	7		14	1
U57	MS68B50	1	12		
U58	74S00	7	14		
U59	74LS244	10	20		
U60	MC1489	7	14		
U61	74S10	7	14		
U62	74LS194	8	16		
U63	74LS245	10	20		
DL1	50NS DL	7	14		
DL2	70NS DL	7	14		
Y1	K1148A	7	14		
XU1	SOCKET	14	28		
XU2	SOCKET	14	28		
XU3	SOCKET	14	28		
XU4	SOCKET	14	28		
XU5	SOCKET	14	28		
XU6	SOCKET	14	28		
XU7	SOCKET	14	28		
XU8	SOCKET	14	28		



Y1	
XU8	
U63	
S2	
R22	
P2	
J27	
DS3	
DL2	
C45	
HIGHEST NUMBER USED	NOT USED
REFERENCE DESIGNATIONS	



63EW3047B REV E SH 1 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 1 of 14)

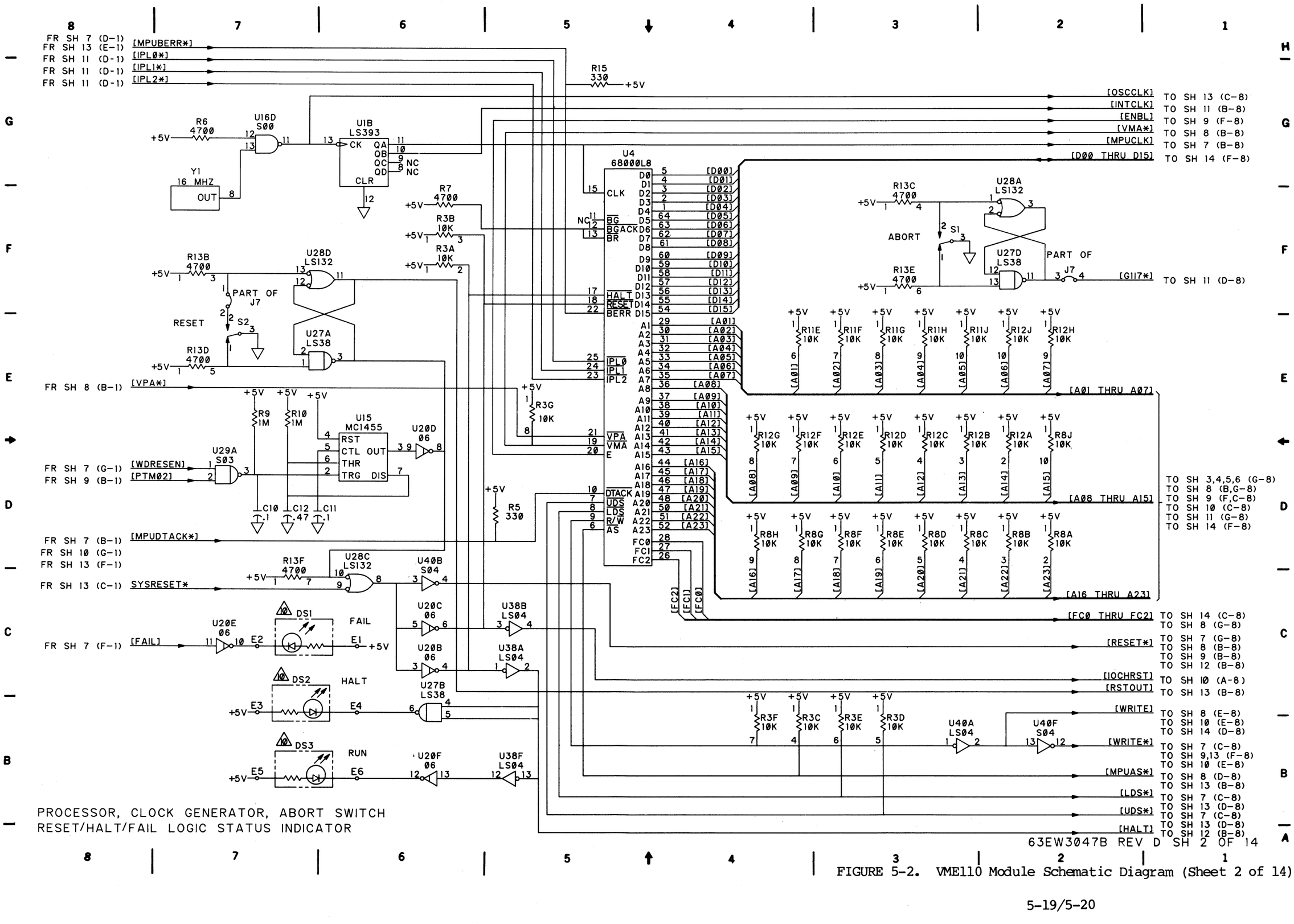
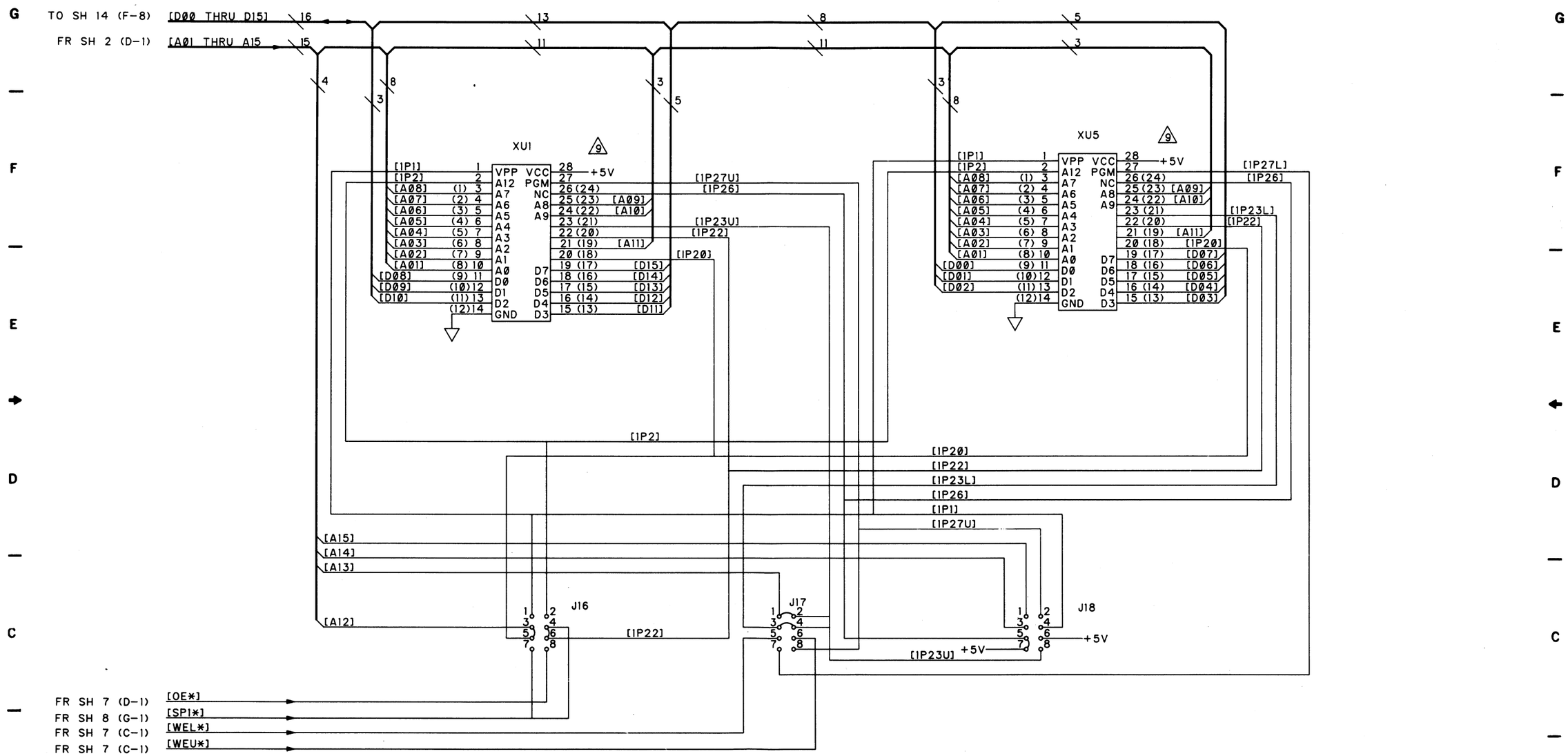
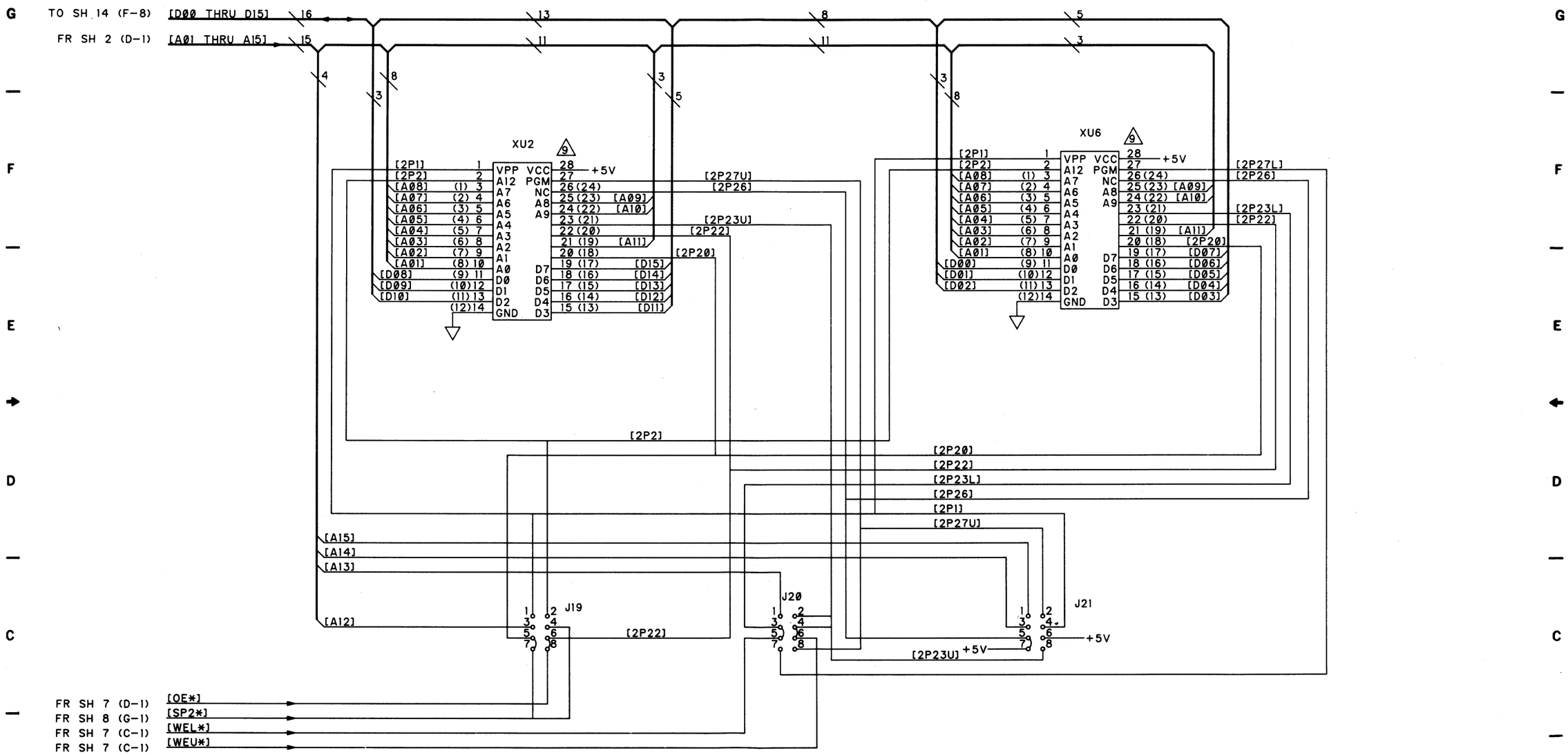


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 2 of 14)



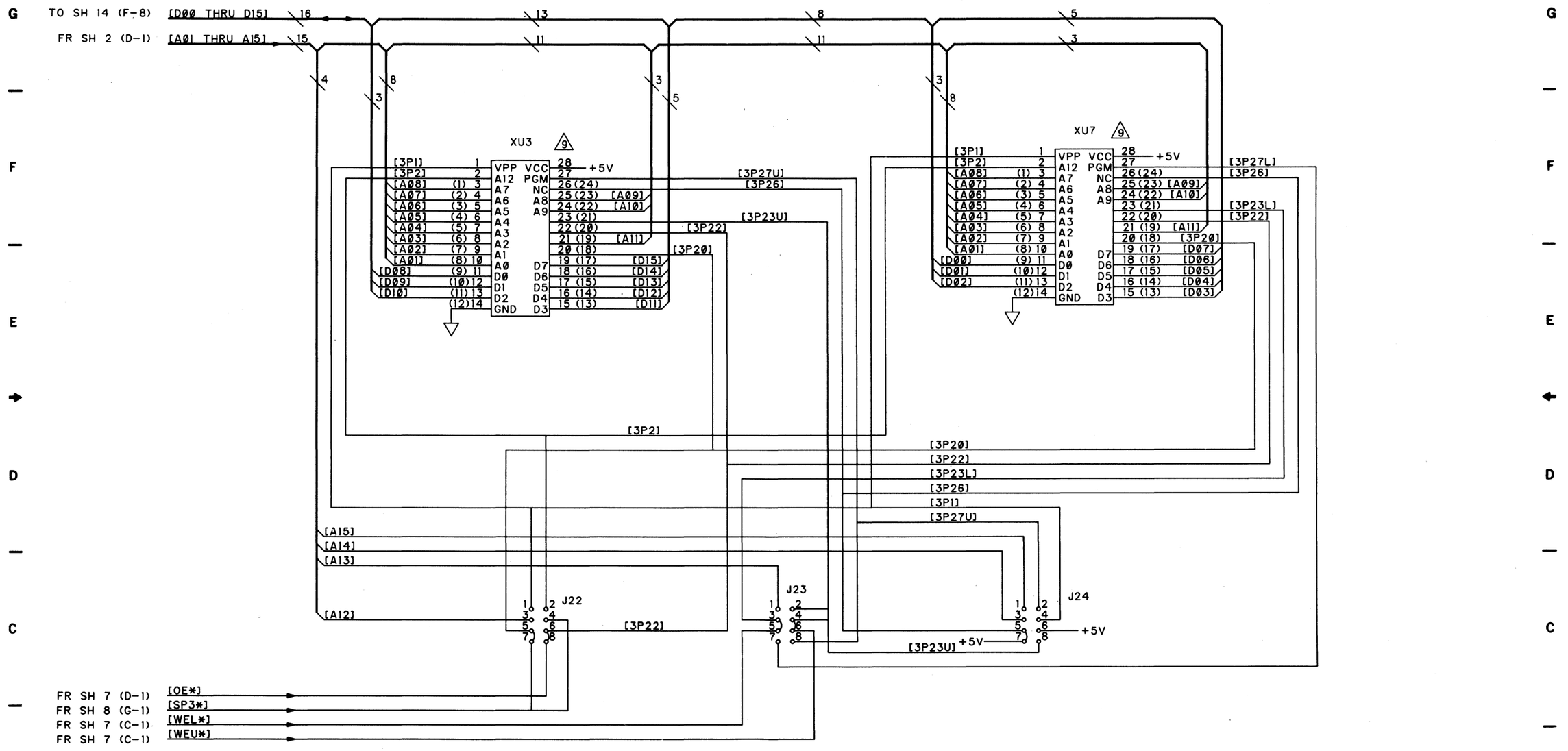
RAM/ROM
63EW3047B REV D SH 3 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 3 of 14)



RAM/ROM
63EW3047B REV D SH 4 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 4 of 14)



RAM/ROM
63EW3047B REV D SH 5 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 5 of 14)

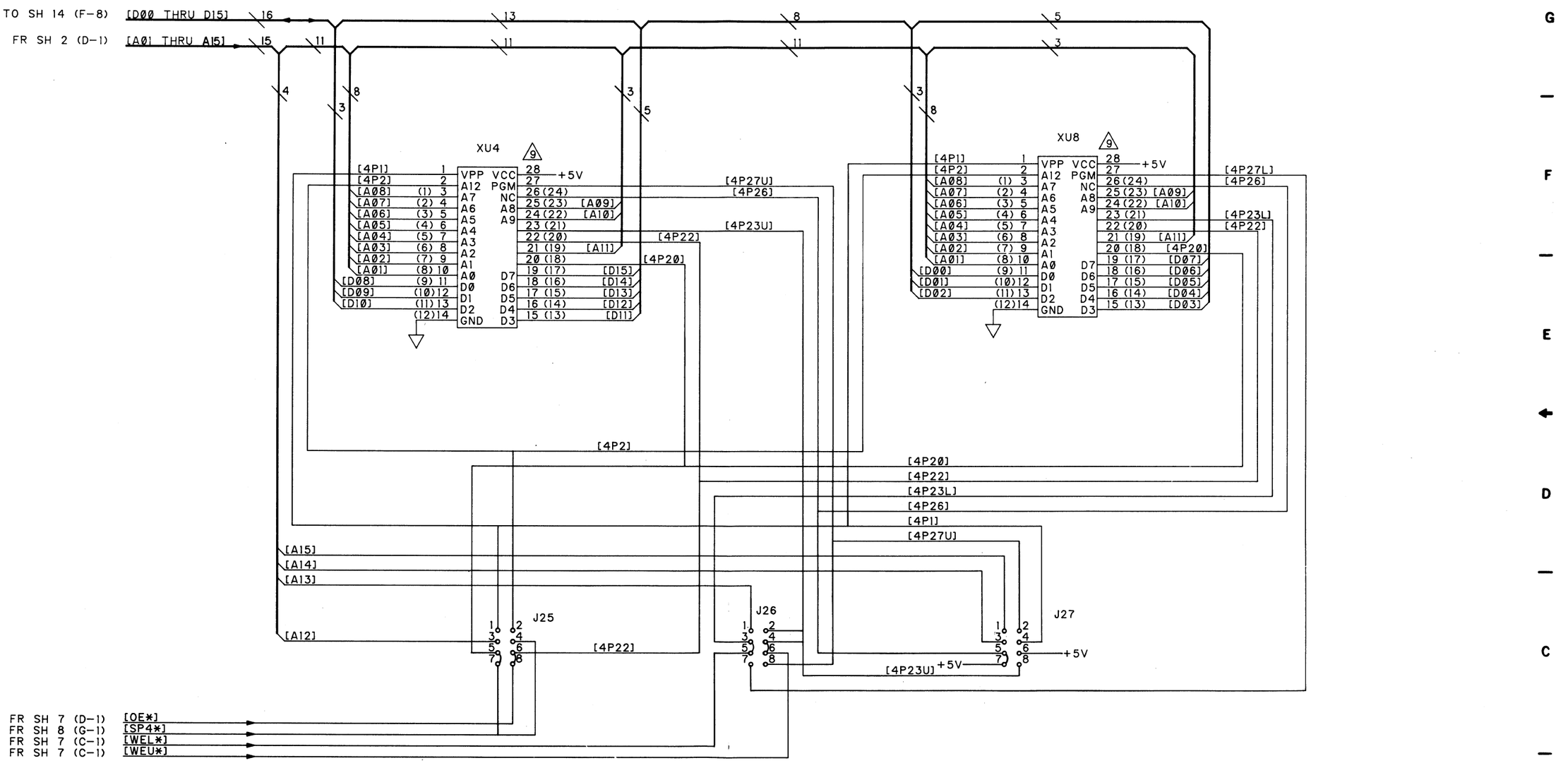


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 6 of 14)

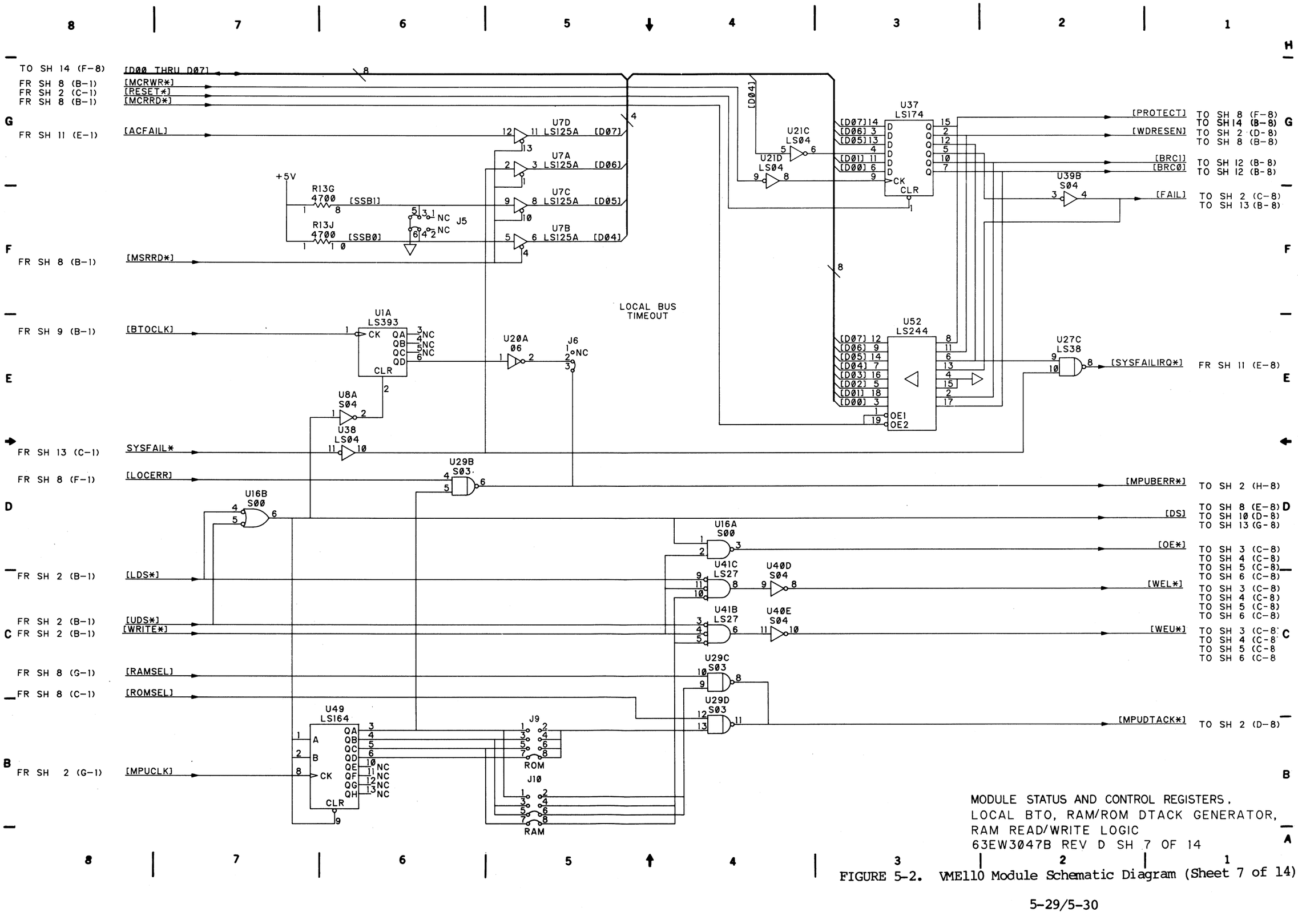


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 7 of 14)

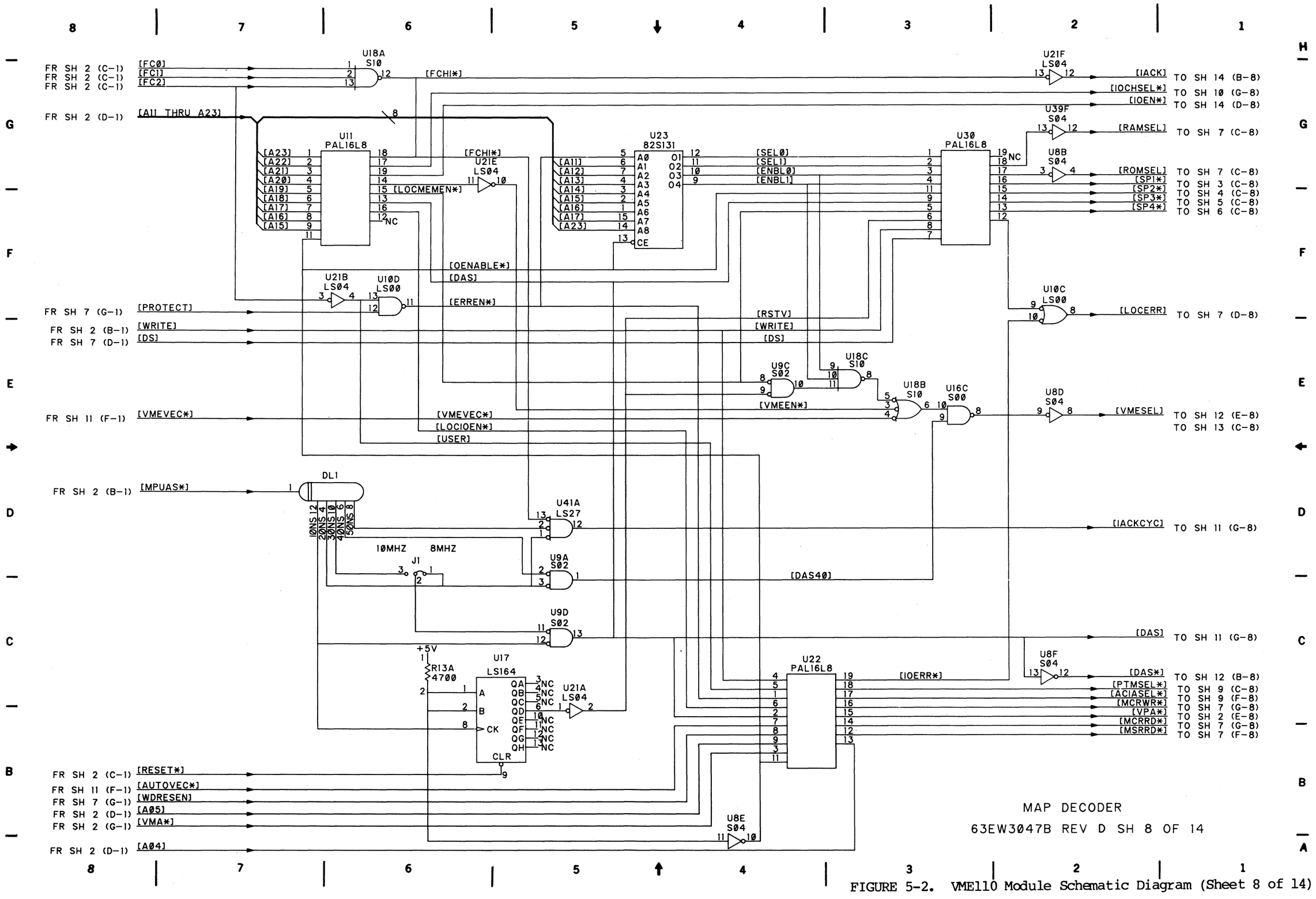
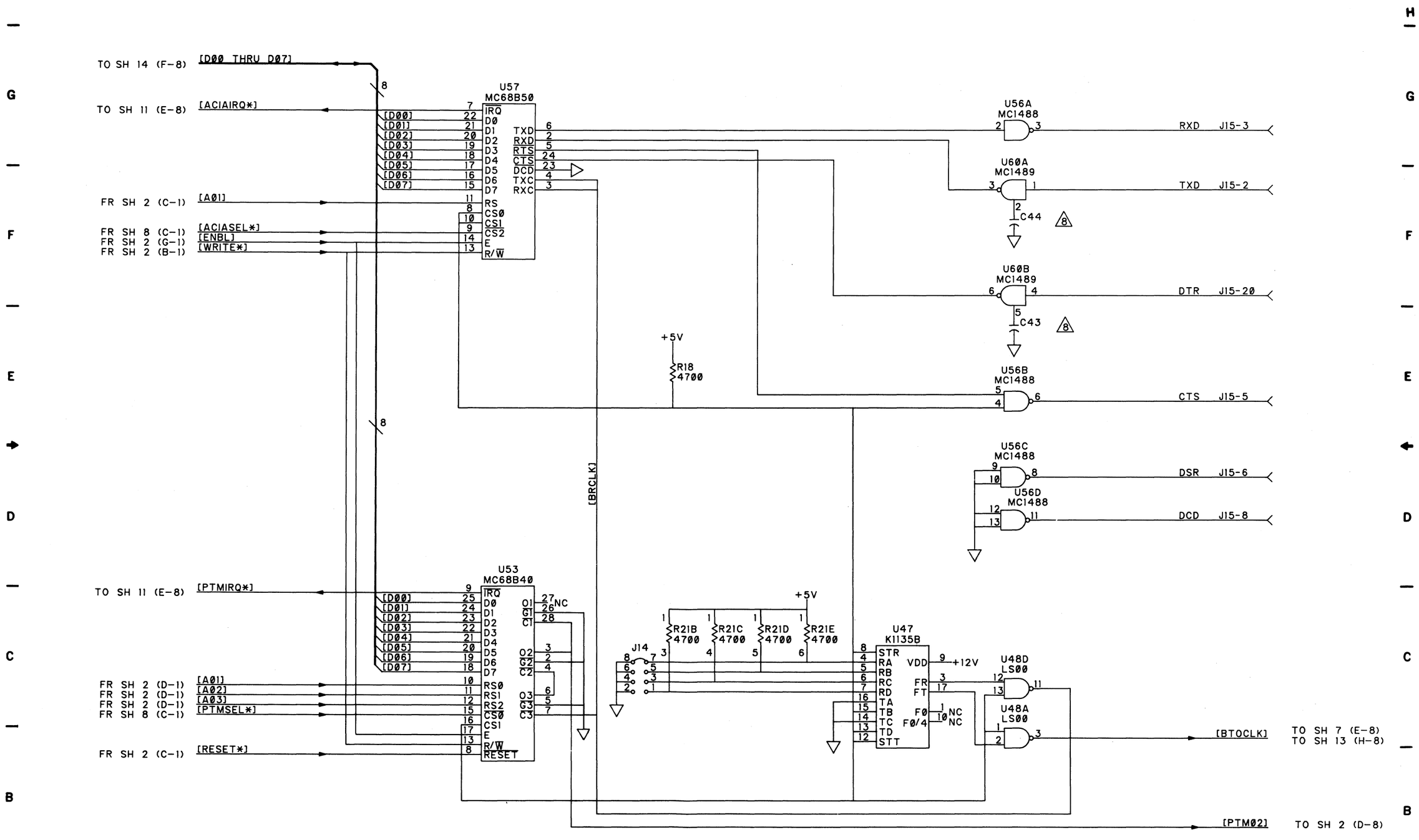


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 8 of 14)



SERIAL PORT, TIMER
BTO CLOCK GENERATOR
63EW3047B REV A SH 9 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 9 of 14)

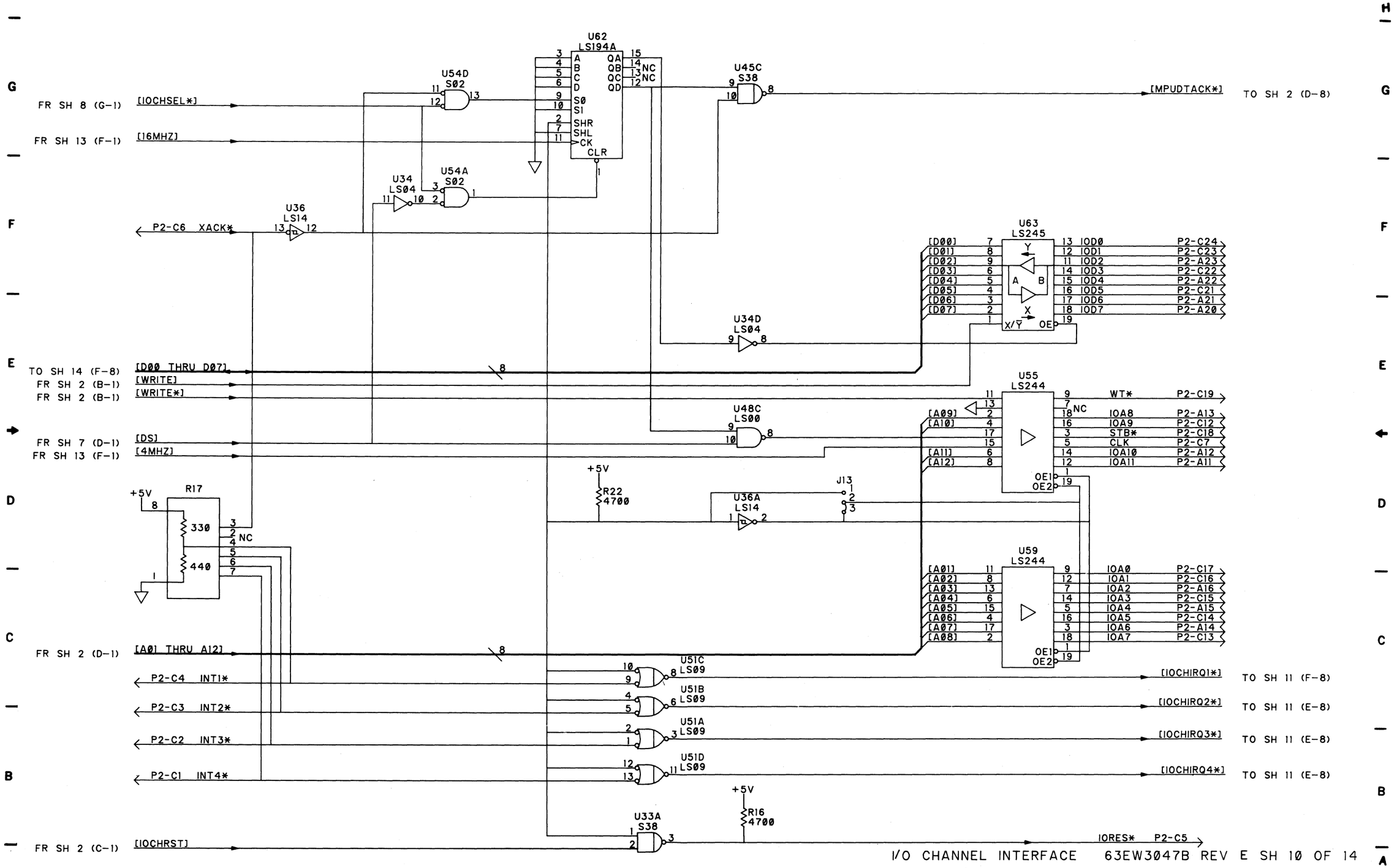
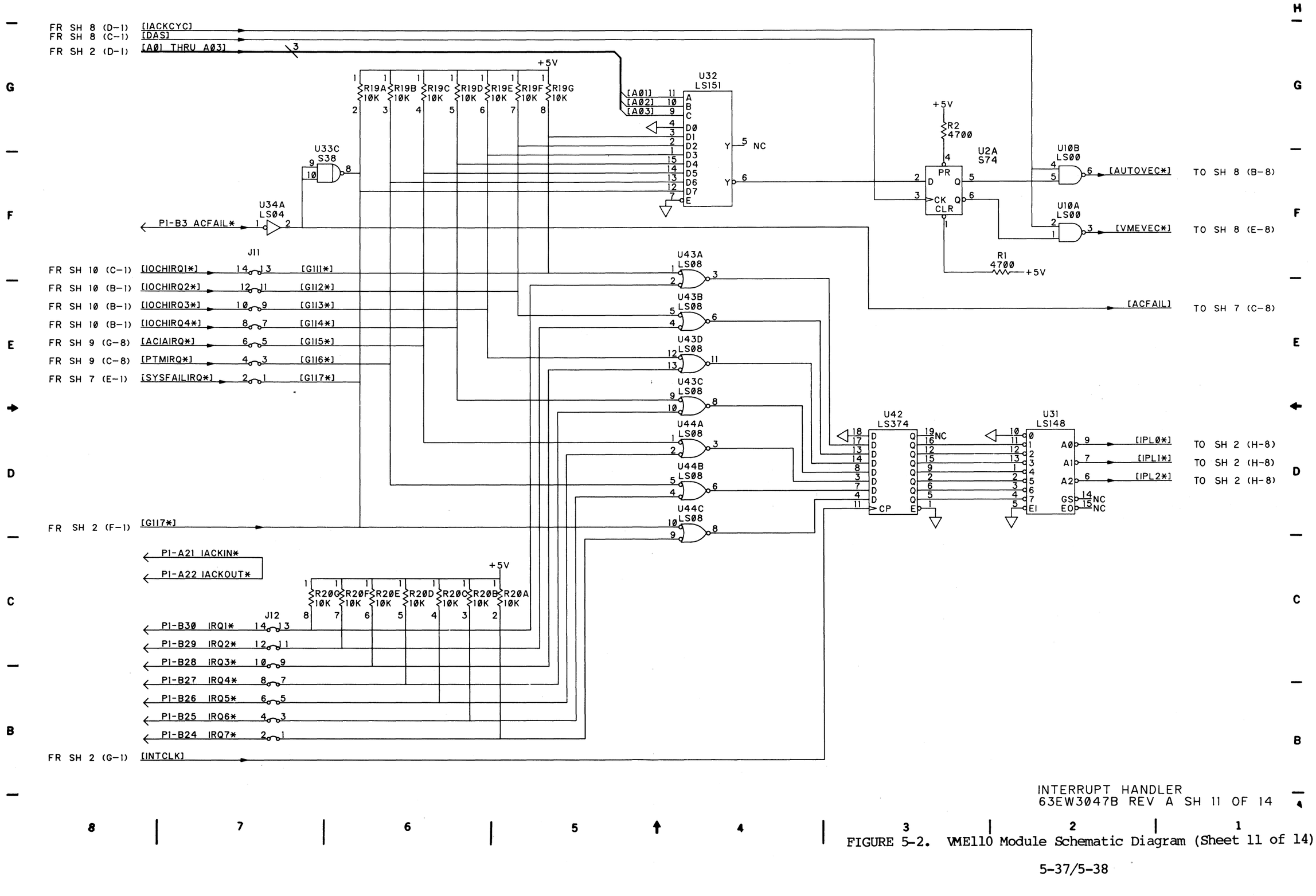
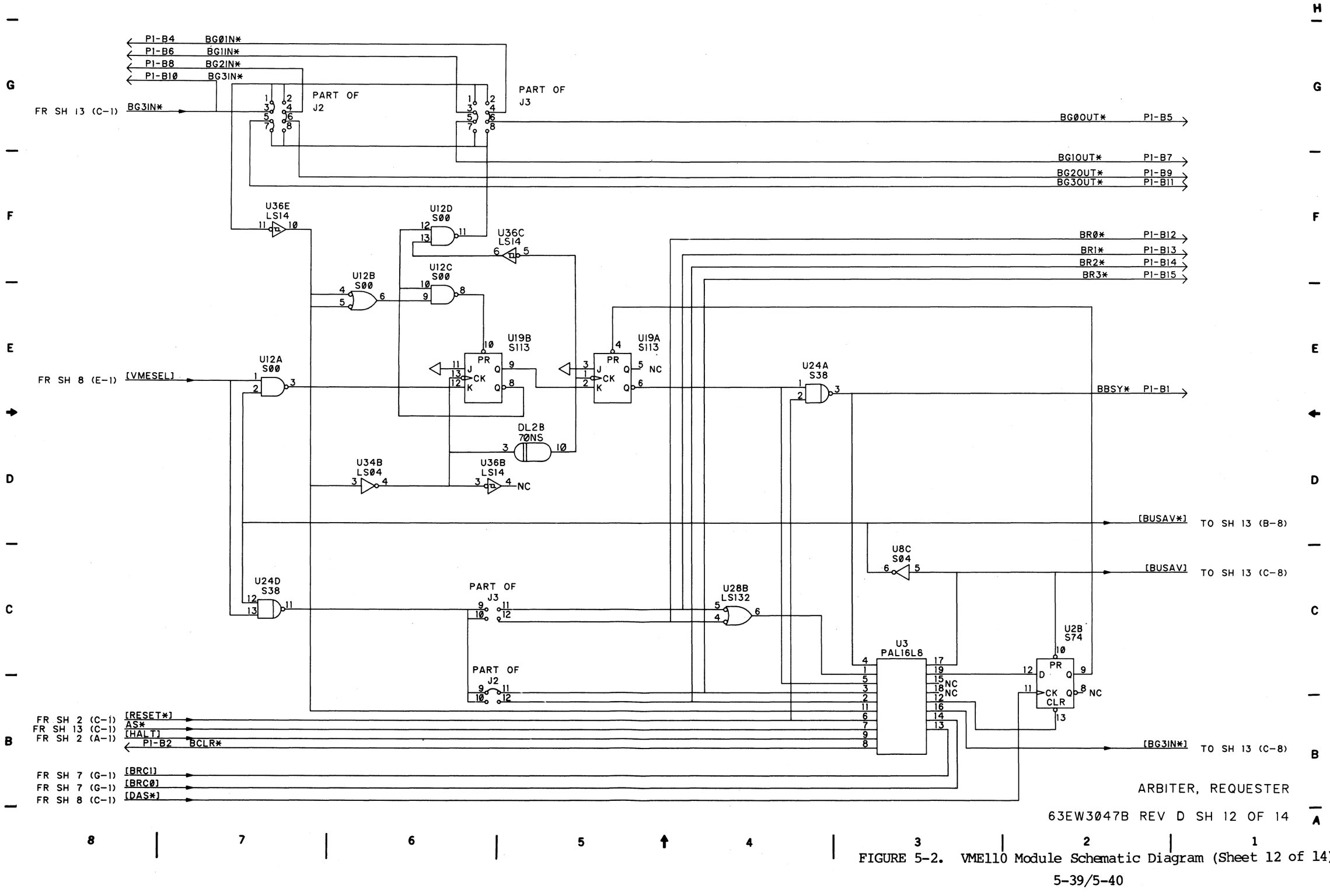


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 10 of 14)



INTERRUPT HANDLER
63EW3047B REV A SH 11 OF 14

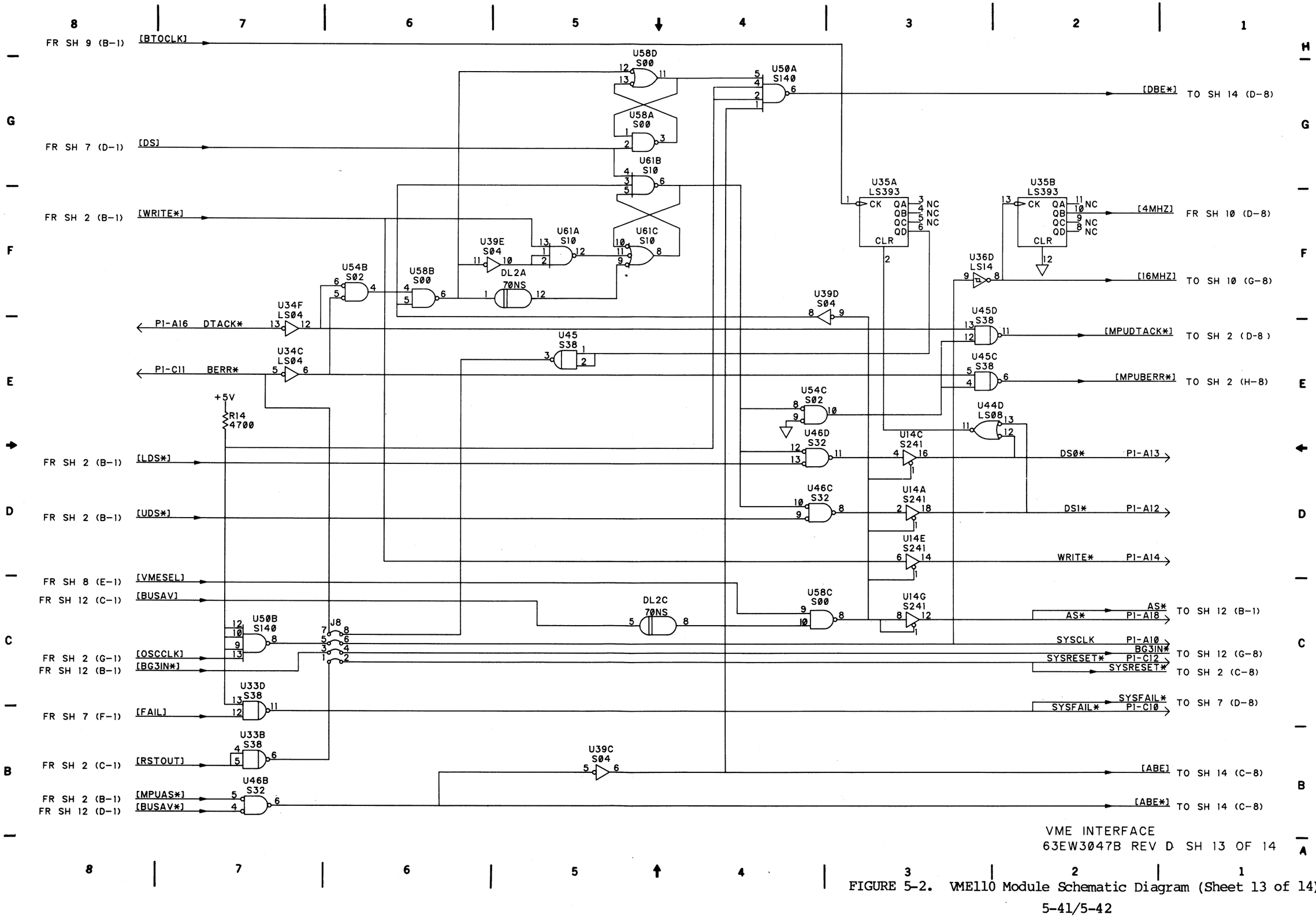
FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 11 of 14)



ARBITER, REQUESTER

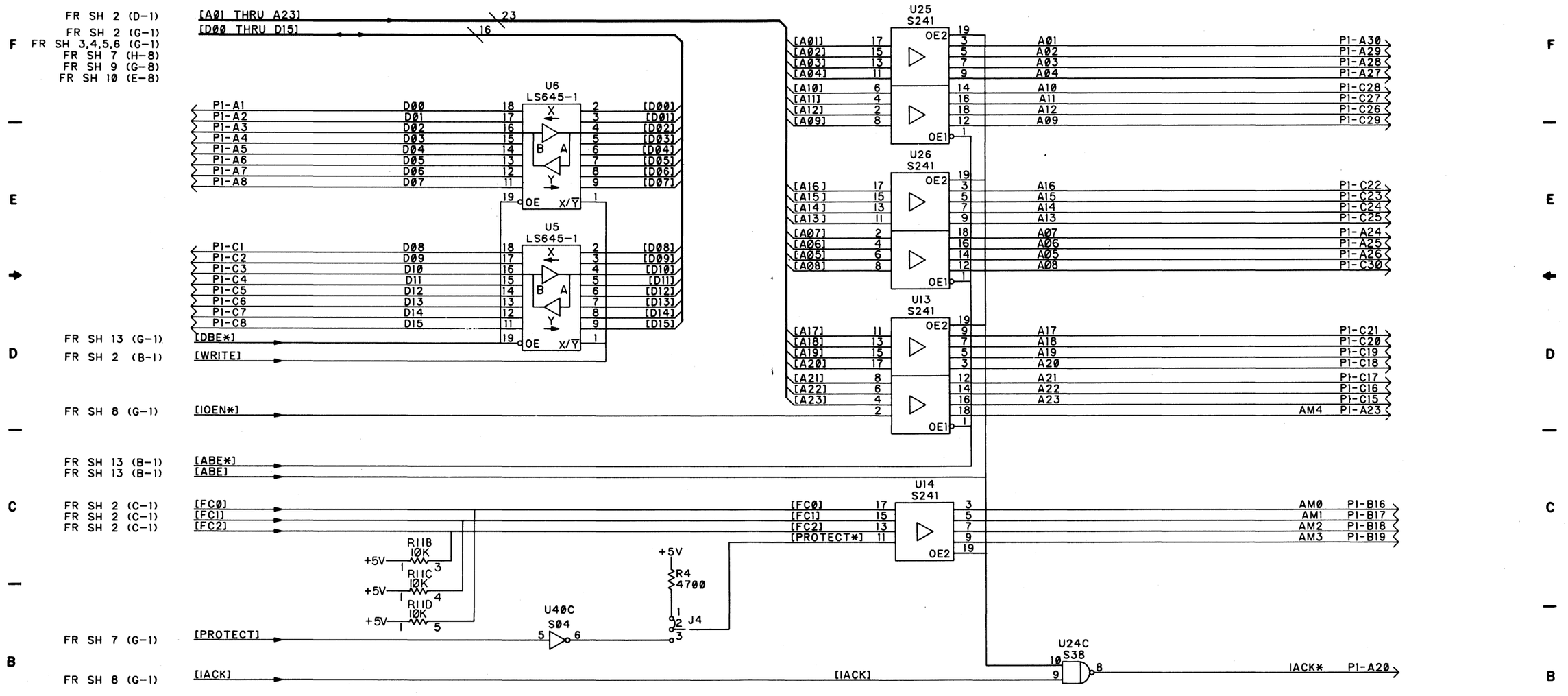
63EW3047B REV D SH 12 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 12 of 14)



VME INTERFACE
63EW3047B REV D SH 13 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 13 of 14)



VME INTERFACE
63EW3047B REV D SH 14 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 14 of 14)