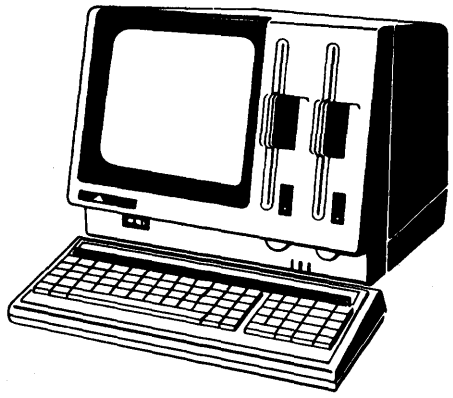
Advanced
Personal Computer
TM



APC Hard Disk Subsystem Reference Guide

NEC
NEC Information Systems, Inc.
819-000102-6002 Rev.00
4-83

APC-HARD DISK SUBSYSTEM REFERENCE GUIDE
Models APC-H26 and -H27.

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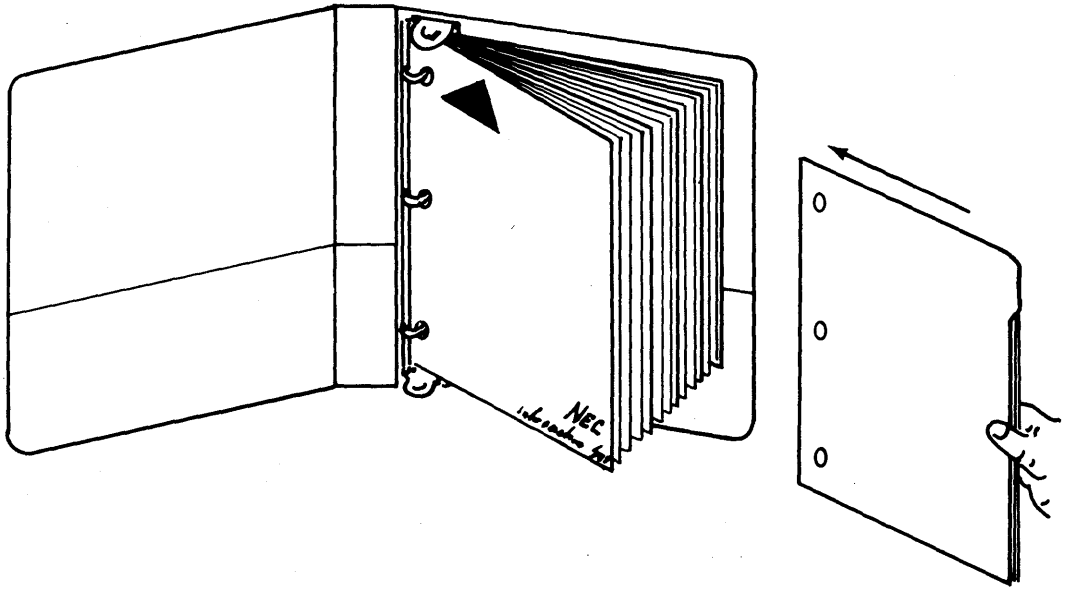

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FEDERAL COMMUNICATIONS COMMISSION RADIO FREQUENCY INTERFERENCE STATEMENT

"WARNING: This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A Computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide protection against such interference. Operation of the equipment in a residential area is likely to cause interference in which case, the user will be required to take whatever measures may be required to correct the interference."

Manufacturer's Instructions and User's Responsibilities to Prevent Radio Frequency Interference

Manufacturer's Instructions

The user must observe the following precautions in installing and operating this device:

1. Operate the equipment in strict accordance with the manufacturer's instructions for the model.
2. Ensure that the unit is plugged into a properly grounded wall outlet and that the power cord supplied with the unit is used and not modified.
3. Ensure that the unit is always operated with the factory-installed cover set on the unit.
4. Make no modification to the equipment which would affect its meeting the specified limits of the Rules.
5. Properly maintain the equipment in a satisfactory state of repair.

User's Responsibility

The user has the ultimate responsibility to correct problems arising from harmful radio-frequency emissions from equipment under his control. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures. All of these responsibilities and any others not mentioned are exclusively at the expense of the user.

1. Change in orientation of the receiving device antenna.
2. Change in orientation of the equipment.
3. Change in location of equipment.
4. Change in equipment power source.

If these attempts are unsuccessful, install one or all of the following devices:

1. Line isolation transformers
2. Line filters
3. Electro-magnetic shielding

If necessary, the user should consult the dealer, NEC, or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission to be helpful: "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402, Stock No. 004-000-00345-4.

"Note: The operator of a computing device may be required to stop operating his device upon finding that the device is causing harmful interference and it is in the public interest to stop operation until the interference problem has been corrected."

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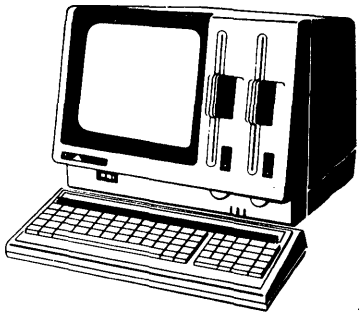
Preface

This manual is written for those who desire an understanding of the Disk Unit (DKU) operations; not only as an external storage device in an APC system configuration, but also its operations within an APC control unit. This information includes the functional capabilities of the DKU, as well as, the status information sent to the APC control unit for interrogation and processing of data and I/O commands. The manual also describes the principal features of the DKU, the applicable environmental considerations, the physical and functional capabilities of the major Printed Circuit Boards (PCB), and the disk drive assembly itself. Maintenance and installation information are mentioned on an as needed basis, only. This type of information is provided in the APC Maintenance Guide and the Hard Disk Subsystem Installation Guide.



Chapter 1

General Description

The APC disk subsystem is used as an external storage device in an APC system (see Figure 1-1). It comes as a stand-alone Disk Unit (DKU), model APC-H26, and an expansion DKU, model APC-H27. The stand-alone DKU is also referred to as the master and the expansion unit as the slave. Each model provides a disk storage capacity of approximately 10 Megabytes (MB) of formatted data. When installed together they provide an overall storage capacity of approximately 20 MBs. Included in each model is a sealed multidisk module designed to improve the operational reliability by minimizing contaminents on the recording surface (see Figure 1-2). Operational reliability is further improved with the use of magnetic heads with NEC Large Scale Integration (LSI) circuits designed to enhance the weakest signals.

The model APC—H26 contains the interface and control logic for the stand-alone and the expansion DKUs on a single Printed Circuit Board (PCB), called the 3302 Format (FMT) control PCB. Both the stand-alone and expansion DKUs contain their respective disk drive electronics.

The APC control unit houses a disk controller, called, the Disk Adapter PCB. This adapter connnects directly with the 3302 FMT PCB in the stand-alone DKU (see Figure 1-3), and contains the interface logic to support the appropriate APC system configuration.

1.1 PRINCIPAL FEATURES

The APC Disk Units (DKU) are compact, fast-access data storage devices designed for use with an APC system. Data is stored on 5.25 inch metal-oxide-coated disks that are mounted on a common rotating spindle and, along with the Read/Write (R/W) heads, are housed in an air-tight, sealed module. This arrangement assures maintenance-free operation, negating maintenance checks. The metal oxide coated disks are also known as platters.

Both models contain four 2-sided disks; each disk surface is equipped with a pair of Winchester type magnetic R/W heads. The R/W heads are supplied as standard equipment and are structured on a swing out mechanism driven by a stepping motor assembly. All heads incorporate a preamplifier to improve read data signal-to-noise ratio.

Depending on the disk configuration, that is, a stand-alone only or a stand-alone and an expansion disk unit, the disk system is capable of storing approximately 10 or 20 MBs of formatted data at a maximum recording density of 7480 bits per inch. The recording method used is the Modified Frequency Modulation (MFM) technique, and the data transfer rate is 500 KBytes per second.

1.2 MODELS

The model disk units currently available for the APC are listed below and are briefly described in the preceding text. A more detailed description is provided in subsequent chapters.

Model APC-H26 Stand-alone DKU (Master Unit).

Model APC-H27 Expansion DKU (Slave Unit).

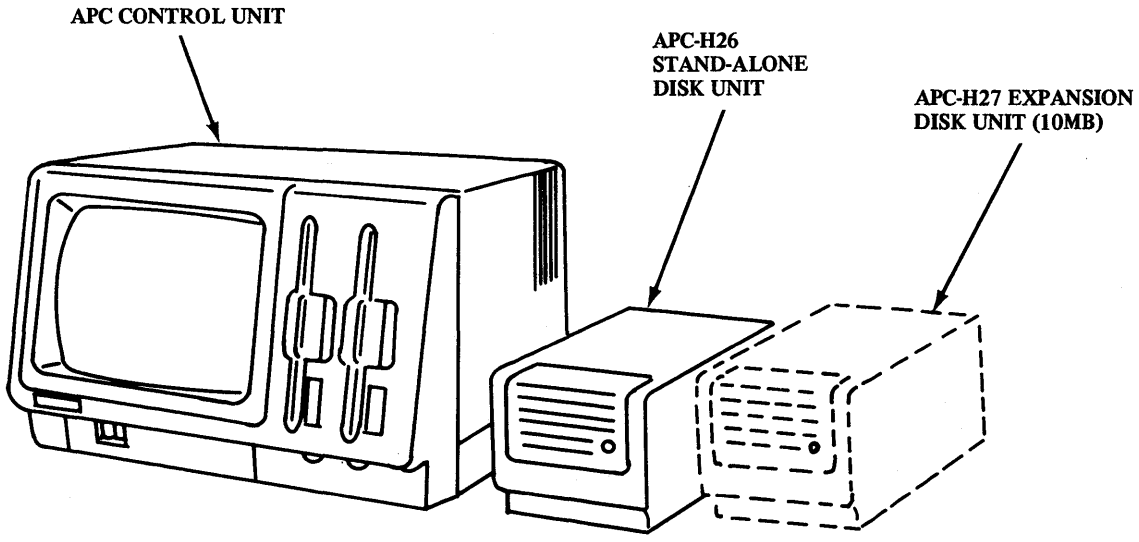


Figure 1-1 Typical APC System Configuration

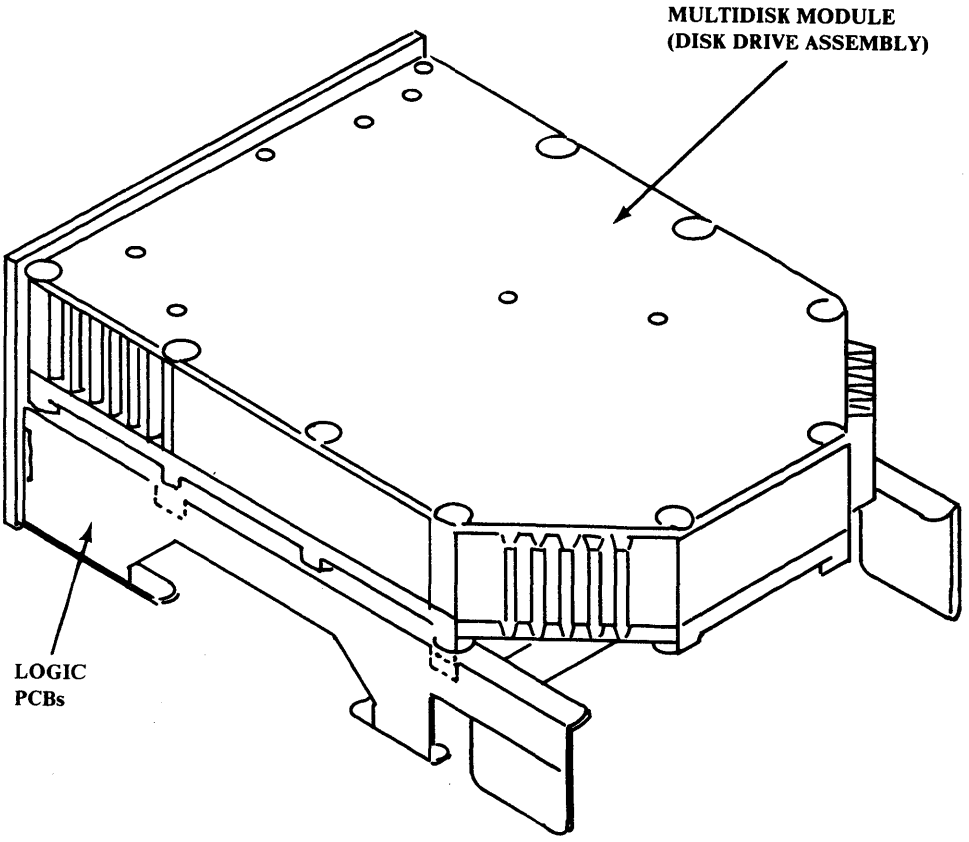


Figure 1-2 Multidisk Module (Disk Drive Assembly)

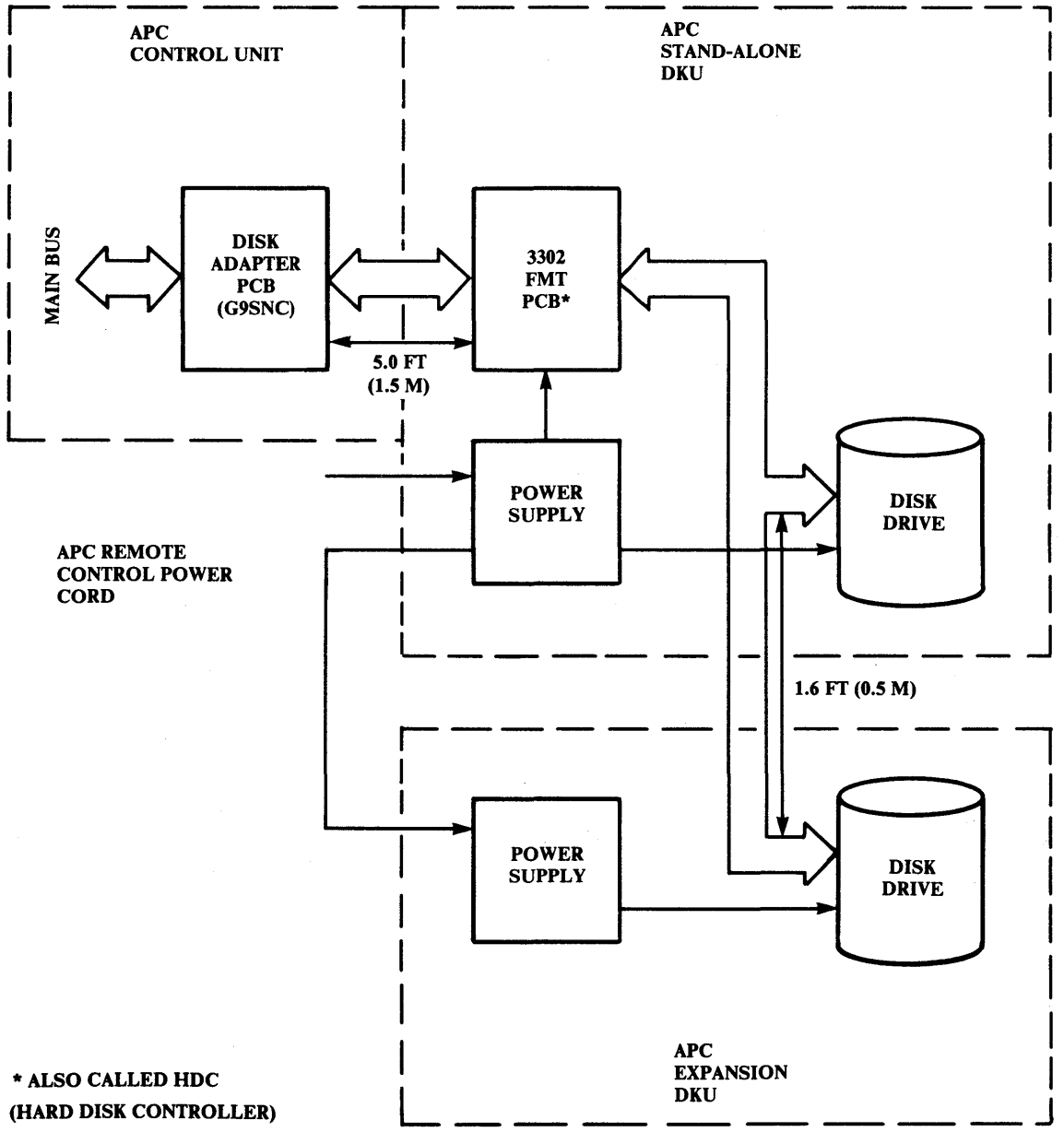


Figure 1-3 APC Stand-Alone/Expansion DKU Functional Block Diagram

1.3 DISK UNIT/MODULE ORGANIZATION

Figure 1-4 shows the physical layout of the major disk drive components contained in the sealed module within the APC Disk Unit (DKU). They are briefly described below. The associated DKU cabinetry and related components are described in subsequent chapters.

1.3.1 Sealed Module

The sealed module contains a sealing type metal cover, spindle, four 5.25 inch platters, eight Winchester type R/W heads, interface and control logic PCB, and other related components shown in the illustration and described in subsequent sections.

The metal cover seals the module against contaminents from the surrounding environment, and maintains constant filtered air flow through the module. Because the interior is sealed from the environment and kept clean by a circulatory air flow, the APC DKU is assured of stable operation under ordinary office conditions.

CAUTION

The cover is normally installed at the factory and should never be removed in the field. When the DKU is defective, return it to the local branch office for service.

The spindle supports and drives the four platters and is driven by a 115 Vac constant drive motor.

The 5.25 inch platters are two-sided magnetic disks that permit the use of Winchester type read and write heads over each surface, resulting in the high storage capabilities in each DKU. That is, each 5.25 inch disk surface has a track density of 220 tracks per inch, resulting in a maximum recording density of 7480 bits per inch. The number of sectors per track is 26 assuming formatted data. When storage is unformatted, the storage capacity and number of sectors are variable up to a maximum storage capacity of approximately 12 MBs. Additional information is provided in subsequent sections.

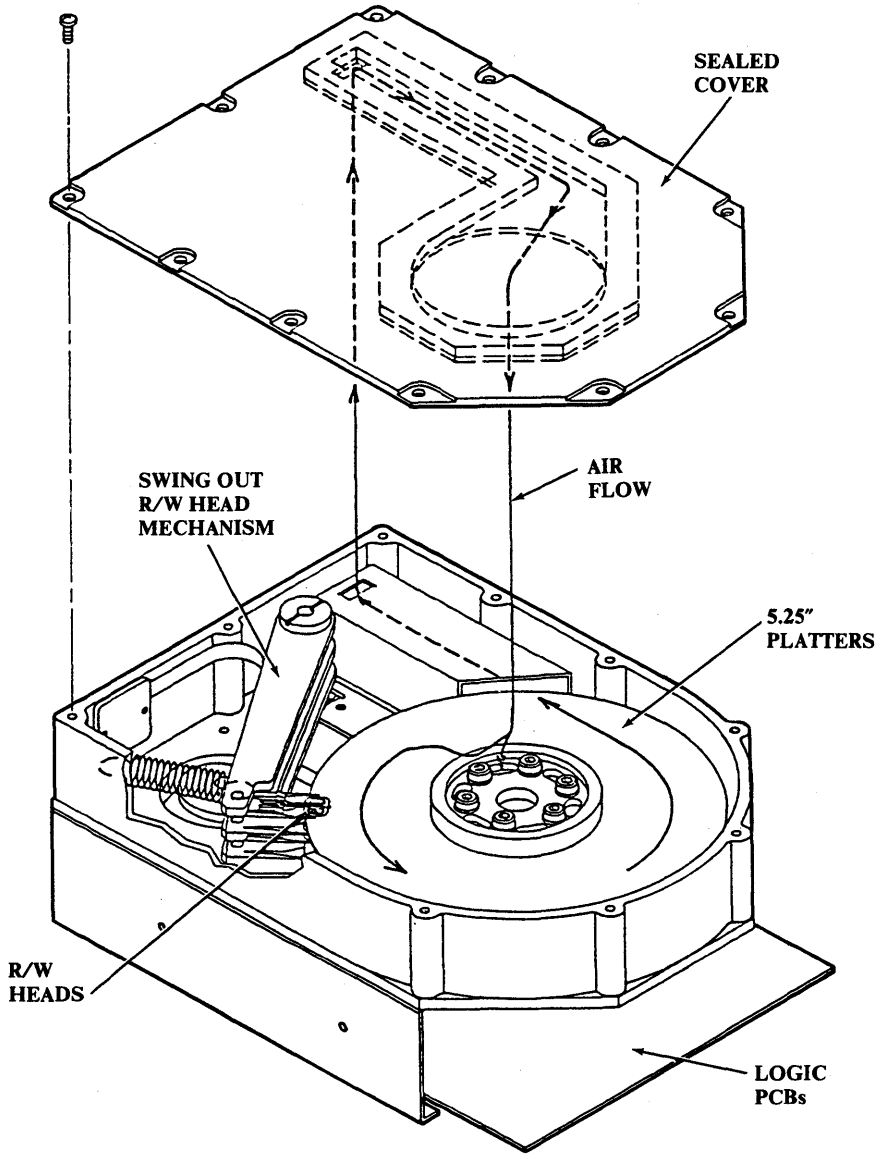


Figure 1-4 APC Disk Module (Major Components)

Winchester type R/W heads are supported by a swing-arm mechanism which is driven by a 5-phase stepping motor. This arrangement reduces the seek time to less than 2 ms.

1.3.2 Printed Circuit Boards (PCBs)

The following printed circuit boards are used in the respective APC control unit or DKU as indicated. Functional and cabling information for each PCB is provided in subsequent chapters.

1. APC Control Unit —G9SNC Disk Adapter (136-432222-B).
2. Stand-alone DKU —3302 FMT PCB (808-863492-201-A).
   —G9NXT Disk Drive Package (134-835090).
   —G9QKR VFO PCB (134-835122-0).
   —Power Supply (808-863492-201-A).
3. Expansion DKU —G9NXT Disk Drive Package (134-835090).
   —G9QKR VFO PCB (134-835122-0).
   —Power Supply (808-863492-201-A).

1.4 POWER SUPPLY

The 115 Vac, 50/60 Hz input power to the power supply simultaneously starts the power supply and fan. The power supply converts the ac input into regulated dc outputs of +5 and +24 Vdc and distributes the dc voltage throughout the DKU.

Ac input power to the DKU(s) is interlocked with the ac input power in the APC control unit. This makes the APC on/off switch the common power on/off element to all the DKU attachments, as well as, the APC control unit. Hence, the DKU attachments are turned on when the APC control unit is turned on, and are turned off when the APC control unit is turned off.

1.5 ENVIRONMENTAL/FUNCTIONAL CHARACTERISTICS

This section provides the environmental and functional characteristics for the Hard Disk Unit (DKU). This includes the environmental considerations, dimensions, weight, cabling, and an overview of the DKU functional characteristics.

1.5.1 Environmental Considerations

The environmental considerations are as follows:

1. Humidity (Noncondensing)	10% to 80%
2. Operating Temperature	50° to 90° F
3. Vibration (Operating)	Less than 0.5 G

1.5.2 Dimension/Weight

The dimensions and weight for the APC DKU are as follows.

1. Depth 15.20 inches (380 mm)
2. Height 7.00 inches (175 mm)
3. Width 10.00 inches (250 mm)
4. Weight 25.30 lbs (11.5 Kg)

1.5.3 Interface/Interlock Cabling

Two interface cables and an ac interlock cable, described below, are required to connect the stand-alone DKU to the APC control unit and, when used, the expansion unit to the stand-alone unit. Further cabling information is provided in the APC-H26/-H27 Hard Disk Subsystem Installation Guide.

1. Interface Cables
   a. Model APC-H26 Stand-alone DKU—The interface cable comes attached to the stand-alone DKU, is approximately 4.96 feet in length, and connects to the APC control unit.
   b. Model APC-H27 expansion DKU—The interface cable comes attached to the expansion DKU, is approximately 1.65 feet in length, and connects to the stand-alone DKU.
2. Ac Interlock Cable
   a. Length—between the APC control unit and stand-alone DKU. 4.96 feet
      —between the stand-alone DKU and the expansion DKU 1.65 feet
   b. Part Numbers

Ac interlock cables	
APC-H26	808-863492-207-A
APC-H27	808-863492-208-A
Ac power supply cables	
APC-H26	808-863492-209-A
APC-H27	808-863492-210-A

1.5.4 DKU Functional Characteristics

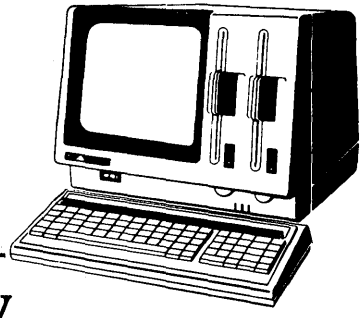
The DKU functional characteristics, summarized in Table 1-1, are estimated at 256 bytes/sector times 26 sectors/track.

Table 1-1 Functional Characteristics

FUNCTION	SPECIFICATION
1. Access Time	
a. Average seek time	120 msec
b. Maximum seek time	360 msec
c. Minimum seek time	2 msec
d. Settling time	15 msec
2. Data Transfer Rate	500 Kbytes
3. Disk (Platter) Configuration	
a. Cylinders	181 Total 174 Data CYL 6 Spare CYL 1 DIAG. CYL
b. Heads (Read/Write)	8
c. Platters	4 (2 sides each)
4. Power—115 Vac input, 50/60 Hz	±10%, 1.0A
a. +5 Vdc (output)	±5%, 1.8A (with VFO)
b. +24 Vdc (output)	±10%, 1.2A (average 2.2A (starting)
5. Recording Density	
a. Bit density	7480 BPI
b. Track density	220 TPI
6. Recording Format	MFM
7. Reliability	
a. MTBF	10,000 Power on Hours
b. Error Rate	
• Non-Recoverable	1 per 10^{12}
• Recoverable	1 per 10^{10}
• Seek errors	1 per 10^{6}
8. Rotational Speed	3600 RPM
9. Start/Stop Time	Less than 10 sec
10. Storage Capacity	
a. Formatted	9.27 MB
• Bytes/Cylinder	53,248
• Bytes/Track	6,656
b. Unformatted	12.0 MB

1.6 TYPICAL DISK DRIVE READ/WRITE OPERATION

To write data on a disk (platter) the FMT controller, described in Chapter 2, converts 8-bit parallel data characters from the APC control unit (see Figure 1-3) into bit-by-bit serial data characters. The disk drive electronics (see Chapter 3) accepts the serial data from the FMT controller and gates it to the disk drive assembly where it is written, bit-by-bit, into the designated sector (or sectors) on the selected platter. A read operation fetches bit-by-bit serial data from the designated sector (or sectors) on the selected platter, and sends this serial data to the FMT controller where it is converted back to 8 bit parallel data characters for transmission to the APC control unit.



Chapter 2

PCB Structure/Functionality

This chapter provides the structural characteristics for the two major DKU PCBs used in an APC system configuration (see Figures 1-1 and 1-3), and includes a brief description of their functional capabilities. The two major PCBs are as follows.

- G9SNC Disk Adapter (Disk Controller) PCB
- 3302 Format (FMT) Control PCB

2.1 DISK ADAPTER PCB

The disk adapter provides the interface and control logic between the APC control unit and the associated DKU attachments (see Figure 1-3). It contains the FMT interface logic and connector, resides in the APC control unit, and consists of the following logic components (see Figure 2-1).

- 8237 DMAC
- 8K Byte Static RAM
- RS422 Formatter Interface

The disk adapter fits into any blank slot in the card cage (mother board) within the APC control unit, and provides the following logic circuits.

- DMA Control Logic
- Error Detect Logic
- FMT Interface Logic
- Interrupt Logic
- I/O Decoder
- Main Bus Control
- Memory Buffer

2.1.1 Disk Adapter Operational Modes

Functionally the disk operates in two modes.

a. Internal Bus Mode
b. Main Bus Mode

A
DISK ADAPTER/DKU
BLOCK DIAGRAM

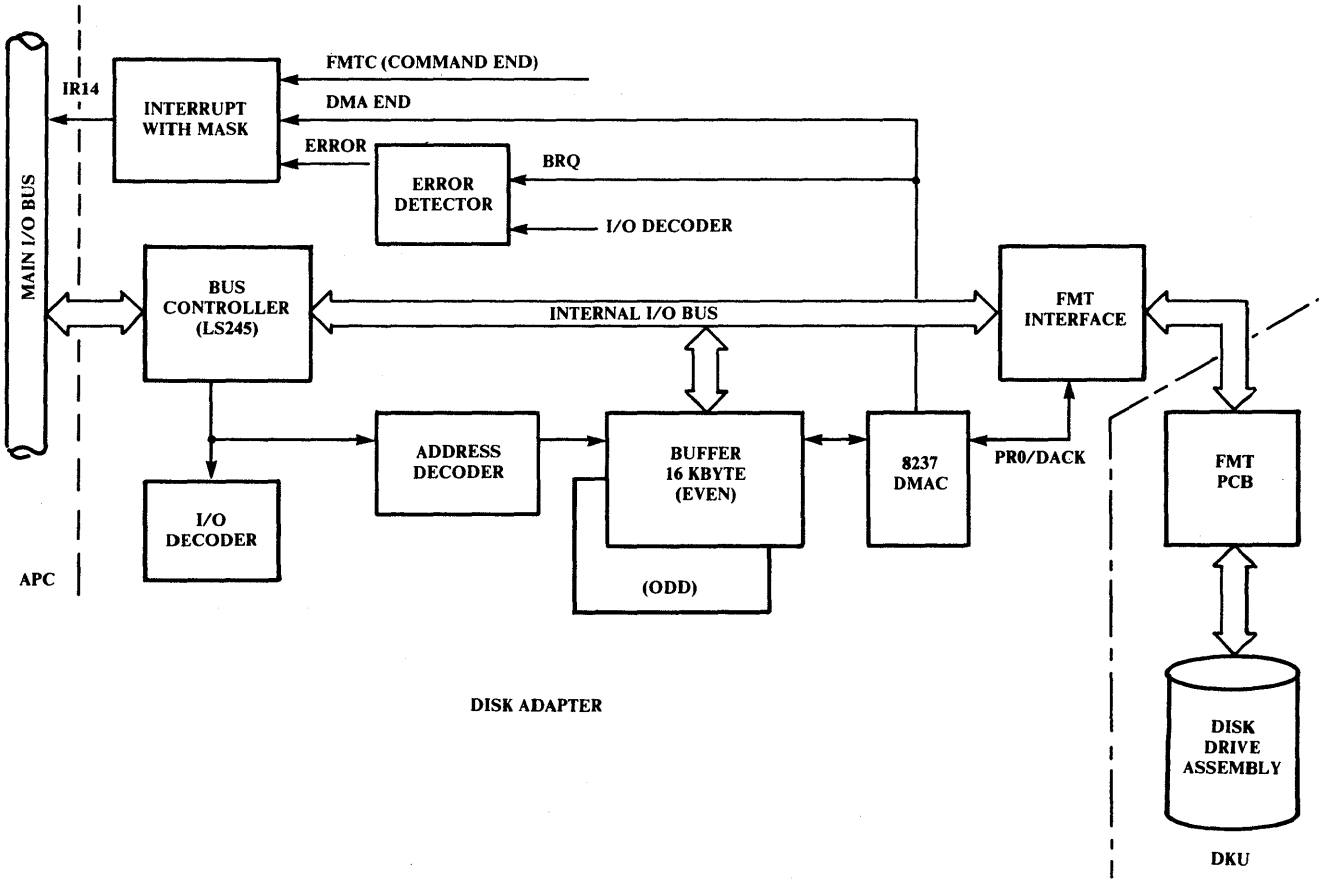


Figure 2-1 Disk Adapter Functional Block Diagram

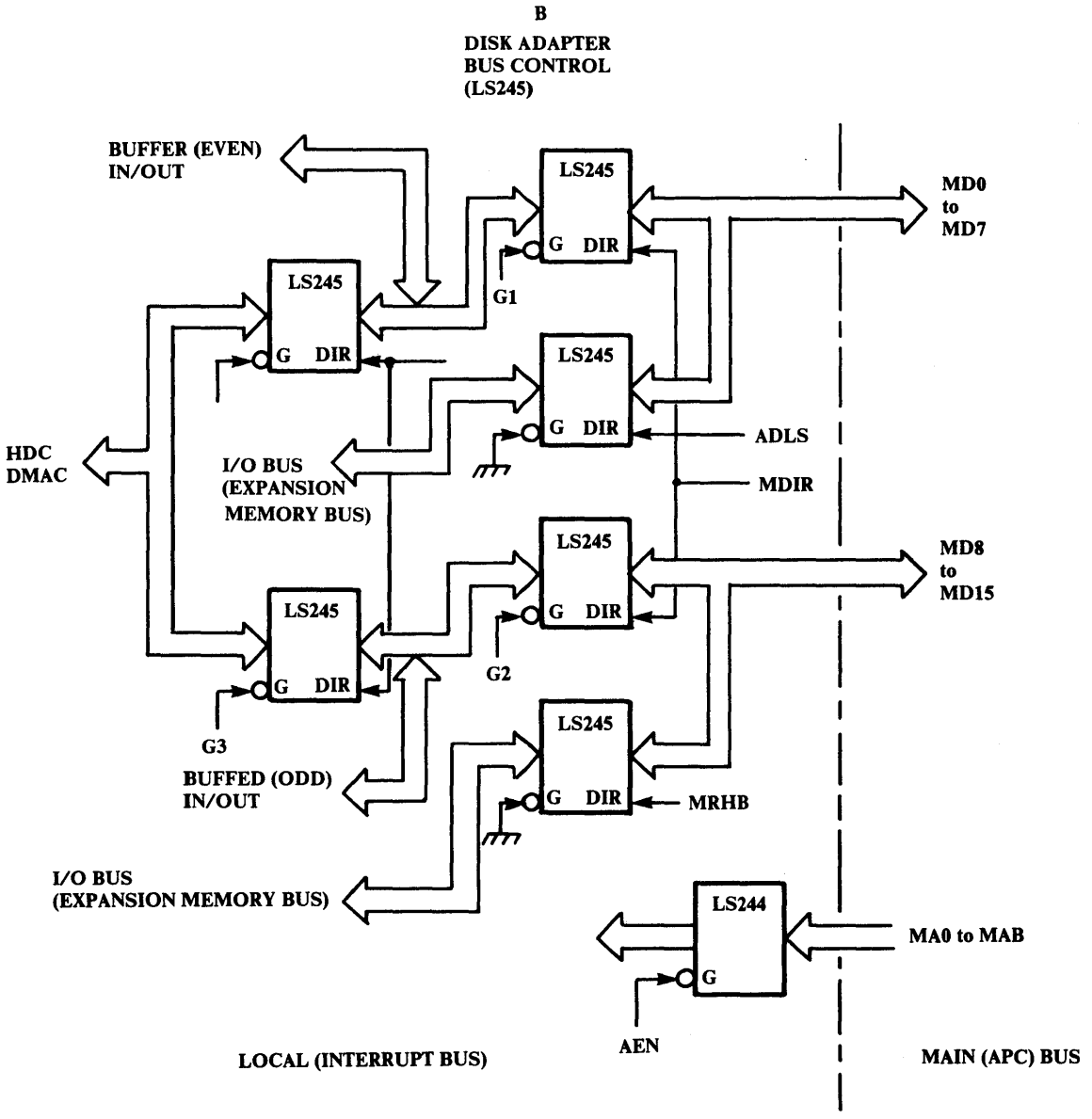


Figure 2-1 (cont'd)

The internal bus mode performs the read and write operations from the external disk drive through the Format (FMT) control PCB. This mode commences when a disk command is sent to the FMT PCB. Data transfers between the memory buffer in the disk adapter and the FMT PCB in the DKU are completely separated from the main bus in the adapter and operate within the internal bus. Access to the memory buffer, transmission of I/O instructions to the DMA controller and to the FMT PCB are inhibited.

The main access mode accesses data from the RAM in the Disk Adapter.

2.1.2 Disk Adapter Functional Capabilities

This section briefly describes the functional capabilities of the Disk Adapter logic circuits, listed earlier, and shown in the functional block diagram in Figures 2-1 and 2-2.

2.1.2.1 DIRECT MEMORY ACCESS CONTROLLER (DMAC DATA TRANSFERS)

DMAC data transfers between the FMT interface and the memory buffer, in demand or single mode, are performed through channel 1 of the DMA controller. In addition, access to the memory buffer and execution of I/O instructions for the DMA controller and FMT interface are inhibited. These operations are detected as errors. All other channels are not used and memory to memory transfers are disallowed.

2.1.2.2 ERROR DETECT LOGIC

The error detect logic monitors the DMAC logic for any possible errors. The error status is sent to the interrupt logic for transmission to the APC control unit where the error status is acted upon accordingly.

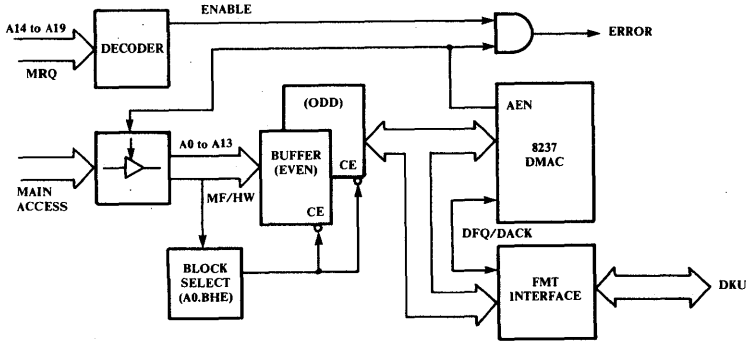


Figure 2-2 Buffer Control Block

2.1.2.3 DISK ADAPTER FMT INTERFACE LOGIC

The FMT Interface logic within the disk adapter provides the communication link between the disk adapter, specifically the DMA controller, and the FMT PCB. It is connected directly to the format control PCB (3302 FMT) in the DKU (Model APC H-26), and controls the data format to the disk drive.

Figures 2-3 and 2-4 show the electrical circuit for the RS422 interface, and Table 2-1 lists the the signal-to-pin assignment for the interface connector. In addition, Figures 2-5 and 2-6 show the timing diagrams for the FMT interface and a DMA access operation.

The FMT PCB is seen as an I/O port to the main processor in the APC control unit. This I/O port has three registers, IR0, IR2, and IR3 that are selected by the FMT control lines, and the appropriate register function is also enabled as shown in Table 2-2.

The IR0 register controls the information for an FMT operation.

The IR2 and IR3 registers correspond to the command/status register and parameter/result registers, respectively. For further details refer to FMT in Section 2.2.

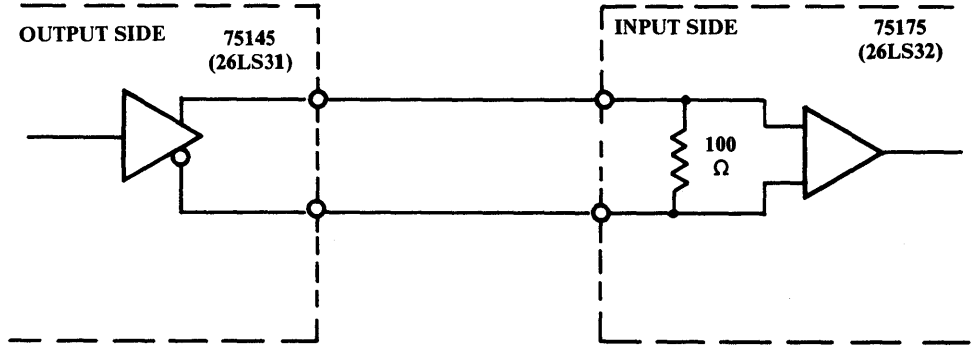


Figure 2-3 Typical Driver/Receiver Circuit

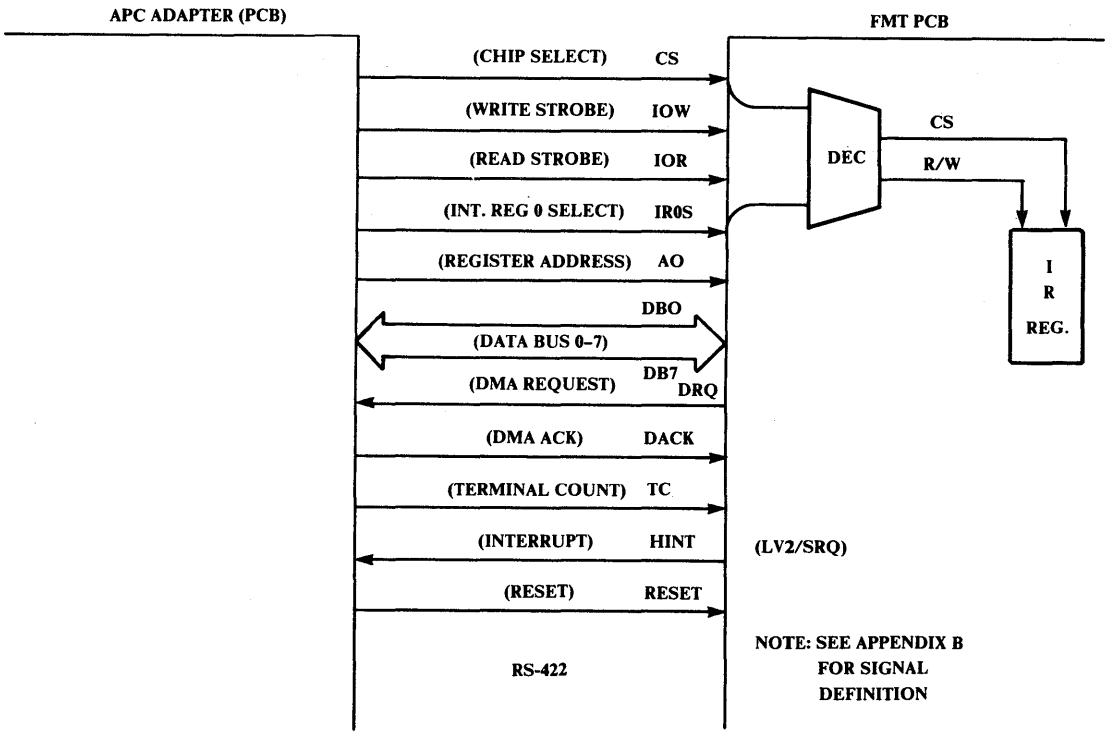


Figure 2-4 Interface Signals (Adapter to FMI)

Table 2-1 Interface Connector Signal Pin Assignment

PIN NO.	IROS-H (*1)	POLARITY	DIRECTION
1 26	GND		
2 27	IOW-H IOW-L	-	→
3 28	IOR-H IOR-L	-	→
4 29	HDCS-H HDCS-L	-	→

Table 2-1 Interface Connector Signal Pin Assignment

PIN NO.	IROS-H (*1)	POLARITY	DIRECTION
5 30	TC-H TC-L	-	→
6 31	IROS-H (*1) IROS-L	-	→
7 32	GND		
8 33	AO-H AO-L	-	→
9 34	RESET-H RESET-L	-	 →
10 35	DACK-H (*2) DACK-L	-	→
11 36			
12 37	GND		
13 38	DB7-H DB7-L	+	→ ←
14 39	DB6-H DB6-L	+	→ ←
15 40	DB5-H DB5-L	+	→ ←
16 41	DB4-H DB4-L	+	→ ←
17 42	DB3-H DB3-L	+	→ ←

Table 2-1 Interface Connector Signal Pin Assignment

PIN NO.	IROS-H (*1)	POLARITY	DIRECTION
18	DB2-H	+	→
43	DB2-L		←
19	DB1-H	+	→
44	DB1-L		←
20	DB0-H	+	→
45	DB0-L		←
21			
46			
22			
47			
23	DRQ-H	+	←
48	DRQ-L		
24	HINT-H	-	←
49	HINT-L		
25			
50			

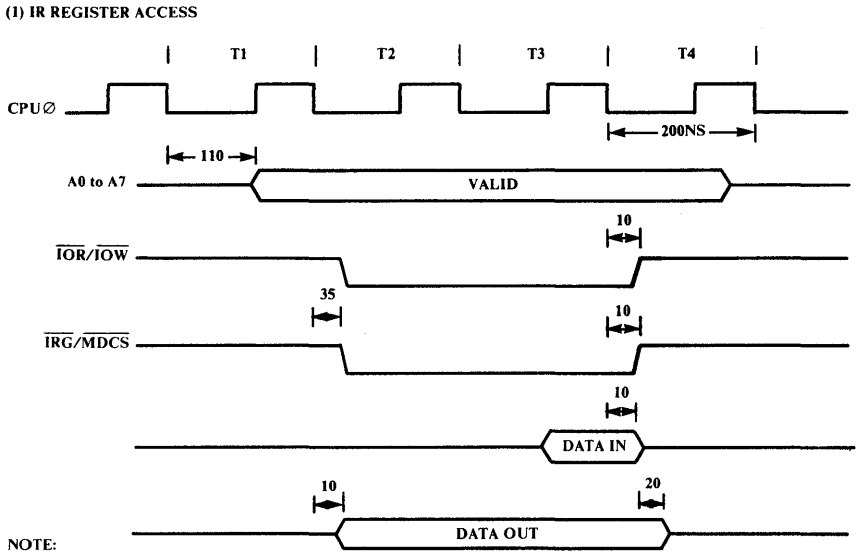


Figure 2-5 FMT Interface Timing

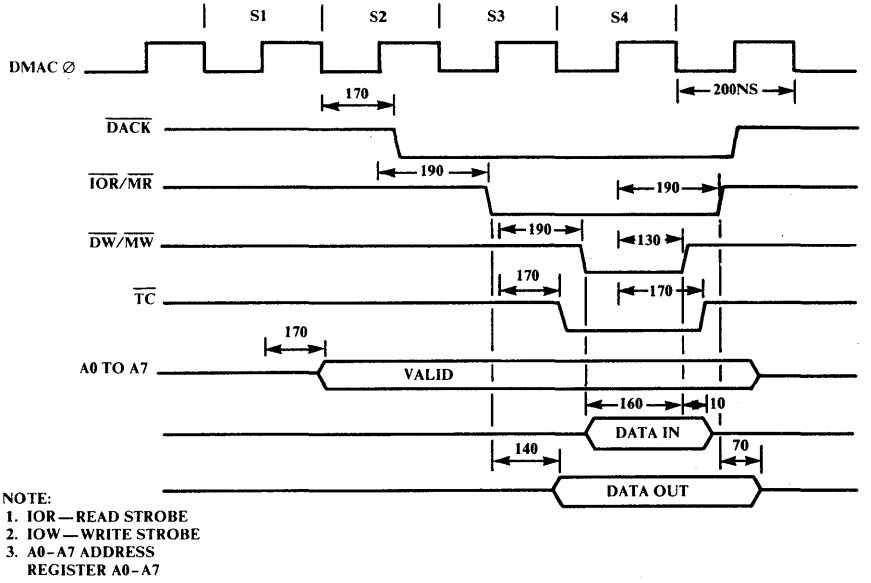


Figure 2-6 DMA Access Timing

Table 2-2 FMT Control Line Register Select/Function

REGISTER SELECT	FMT CONTROL LINES					FUNCTION
	HARD DISK CONTROLLER (HDC)	REGISTER ADDRESS (AD)	READ STROBE (IOR)	WRITE STROBE (IOW)	IR0 SELECT (IROS)	
IR3 READ	0	1	0	1	1	Result Status
IR3 WRITE	0	1	1	0	1	Parameter
IR2 READ	0	0	0	1	1	Status Reg.
IR2 WRITE	0	0	1	0	1	Command Reg.
IR2 READ	0	1	0	1	0	Info. Line
IR0 WRITE	0	1	1	0	0	Info. Line

0 — Designates active state of selected signal or register. For example, HDC = 0 and IOR (Read Strobe) = 0, HDC (FMTC) selected and Interrupt Register 3 (IR3 Read) addressed to read the result status.

2.1.2.4 INTERRUPT LOGIC

The interrupt logic processes FMT commands, DMA operations and the current error status for transmission to the APC control unit.

2.1.2.5 I/O DECODER

The I/O decoder monitors the bus controller (LS245) for I/O commands. The resulting command is returned to the bus controller for the appropriate action.

2.1.2.6 MAIN BUS CONTROLLER

The main bus controller (LS245) processes information from or to the internal bus (see Figure 2-1), the main bus in the APC control unit, the I/O decoder, address decoder, memory buffer and the FMT interface.

Two Programmable Array Logic (PAL), also known as the Programmable Logic Array (PLA), chips are used to decode I/O instructions from the main processor in the APC control unit and to control the bus interface.

2.1.2.7 MAIN PROCESSOR INTERRUPTS (INT) FROM THE APC

Interrupts to the main processor in the APC control unit are ORed with a mask designator through channel 14 in the disk adapter. Individual masking is possible with each interrupt. I/O instructions for read interrupt commands are incorporated prior to masking.

Interrupts

- DMIN —This interrupt occurs when a DMA data transfer between the FMT and the memory buffer is finished in a specified number of counts.
- HDIN —This interrupt designates the completion of a command to the FMT (HDIN = LV2 = CE + SRQ).
- MDER —Denotes error, signifying a memory access operation to the memory buffer from the APC control unit during a DMA operation.
- HDER —Denotes an error when a command is issued to HDC during an FMT command (The HDC is called the Hard Disk controller which is another name for the FMT controller described in Section 2.2).

2.1.2.8 MEMORY BUFFER

Memory is an 8K buffer that consists of four NEC 4016-3 2K × 8 bit static RAMs. In the main access mode the buffer is composed of odd and even numbered blocks and is common to the APC control unit. Address assignment is fixed at AC002 to AFFFF.

Under internal mode, the memory address is continuously assigned.

Data transfer between the buffer and FMT interface is controlled by the DMA controller. Access from the APC control unit is prohibited. If accessed by the APC control unit an error is flagged.

2.1.3 Programming Considerations

The programming considerations consist of a working knowledge of the main (APC) processors ability to access the DMA controller, memory buffer, interrupt registers and other related logic circuits in the disk adapter and HDC (or FMT controller).

Included in the programming considerations are the I/O address functions and bit maps, summarized in Section 2.1.3.2, all I/O byte operations to the main processor, and the word or byte formats to access the memory buffer. The following sections briefly describe the above operations and include additional operations, the knowledge of which, is recommended for successful programming of the HDC.

2.1.3.1 FMT I/O AND PROCESSOR MEMORY ACCESSIBILITY

In an HDC R/W data operation, during a DMA data transfer cycle, I/O and memory access operations from the main processor are not allowed. This action is because the disk adapter and main processor are not in sync with each other. Error detection logic is included to flag the respective HDC operation as an I/O access error (HDER) to the HDC, or a DMA memory access error (MAER) within the adapter. The following briefly describes the above error conditions and provides additional FMT/DMA operations.

1. FMT Complete Confirmation (Read Status)

   A read status register operation during an HDC operation generates an HDER error. To avoid this, completion of an FMT operation must be verified as follows.

   - With a read interrupt from the FMT.
   - Confirmation of an on-going HDC operation with a HDEX flag. This flag is set with a write command to FMT and is cleared by a seek Command End (CEL or CEH) or a Sense Interrupt Status Request (SRQ) command from the FMT.

2. FMT Operation Without a DMA Operation (for example, Seek Command).
   - Memory buffer accessability and I/O command operation to the DMAC allowed.
   - FMT I/O command allowed.
   - HDER generated with an I/O write command.

3. HDER Generation
   - Issuance of a DMAC/FMT I/O command during a DMA data transfer.
   - A command sent to the HDC before the HDC completes an operation.

4. MAER Generation—Access to memory buffer during a DMA data transfer operation.

2.1.3.2 I/O COMMANDS

This section categorizes the I/O commands and provides the appropriate commands, codes and other related information in Tables 2-3 through 2-7. Included are notes that briefly describe the operation and purpose of each command and related function.

Table 2-3 I/O Commands (DMA)*

CATEGORY	I/O COMMAND		DATA FIELD (HIGH BYTE)								FUNCTION
	NAME	ADDRESS	D15	D14	D13	D12	D11	D10	D9	D8	
DMA Note 1	CHANNEL 1										
	DMA ADR. L	A3	A7	A6	A5	A4	A3	A2	A1	A0	
	DMA ADR. H	A3	A15	A14	A13	A12	A11	A10	A9	A8	Read/Write
	DMA Count. L	93	C7	C6	C5	C4	C3	C2	C1	C0	(Note 3)
	DMA Count. H	93	C15	C14	C13	C12	C11	C10	C9	C8	
	Status	A9	R03	R02	R01	R00	TC3	TC2	TC1	TC0	Read
	Write CMD	A9	KS	DS	WS	PR	TM	LE	AH	MM	(Note 2)
	Register Request	99	—	—	—	—	—	RE	CSI	CS0	Write
	Single Mask	AB						MSK	CSI	CS0	Write
	Mode Register	9B	MS1	MS0	ID	AT	TR1	TR0	CS1	CS0	Write
	Clear F/F	AD									Write
	TEMP. Register	9D	D7	D6	D5	D4	D3	D2	D1	D0	Read
	Master Clear	9D									Write
	All Make	9F					MB3	MB2	MB1	MB0	Write

* See (8237) DMA LSI Functional Specifications for details.

NOTES:
1. All unused channels (CH) except CH1 must be masked.
2. Data for command register is set to all zeroes.
3. DMA address bits, A15 and A14, are ignored if memory buffer is 16 KB or less.

Table 2-4 I/O Command (HDC/FMT)

CATE-GORY	I/O COMMAND		DATA FIELD (LOW BYTE)								
	NAME	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
HDC (3302 FMT)	Result Status	A0	D7	D6	D5	D4	D3	D2	D1	D0	Read (R)
	Parameter	A0	D7	D6	D5	D4	D3	D2	D1	D0	Write (W)
	Status	92	CB	CEH	CEL	SRQ	RBQ	IER	NCI	DBQ	Read (R)
	Write CMD	92	CC4	CC3	CC2	CC1	CC0	UA2	UA1	UA0	Write (W)
3302 FMT (Notes)	Interface Register (IR)0	A2	—	CB	DACK	—	—	CE	LV2	SRQ	Read (R)
	IR0	A2	INTI	CLDB	RSTR	CLCE	0	EOP	0	HSR0	Write (W)

NOTES:
1. See 3302 FMT firmware functional specifications for detail. The FMT has the equivalent HDC I/O commands installed.
2. During a DMA operation an HDER is generated when the 3302 FMT is accessed with the execution of a format control operation.
3. LV2 interrupt bit for an IR0 read is the same as the HDIN interrupt bit for a read INT. command.

Table 2-5 I/O Command (RESET/INT)

CATE-GORY			DATA FIELD (LOW BYTE)								
	NAME	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Reset (Note 1)	H/W Reset (RST)	94									RST Write (W)
INT Note 2	INT Reset	96					HDER	MAER	DMIN		RST Read (R)
	INI/HDEX	96			HDEX	HDER	MAER	DMIN	HDIN		Read (R)
	INI Mask Set	98					IDER	DMIN	HDIN		Set INT MSK

NOTES:
1. H/W RESET command resets the hardware.
2. Interrupt RESET command data bus bit assignment.

DATA BUS BIT	DATA BUS STATUS	DESCRIPTION
D0	DMIN	Interrupt reset by TC during DMA.
D1	MAER	Reset memory access error.
D2	HDER	Reset I/O command timing error.

Table 2-6 Read INT/HDEX Command*

DATA BUS		DESCRIPTION
BIT	STATUS	
D0	X	Don't care
D1	HDIN	HDC Interrupt
D2	DMIN	TC Interrupt in DMA
D3	MAER	Memory Access Error
D4	HDER	I/O Timing Error
D5	HDEX	HDC In Operation (Note)

* The read INT/HDEX I/O command is used to sense an interrupt and an HDC execution.

NOTE:
The HDEX flag is set when an FMT command write is issued, and reset by an HDC interrupt command complete (CEL, CEH, or SRQ) signal.

Table 2-7 INT Mask Set I/O Commands

DATA BUS		DESCRIPTION
BIT	STATUS	
D1	HDIN	HDC Interrupt Mask
D2	DMIN	DMA TC Interrupt Mask
D3	IOER	MAER and HDER Mask

NOTES:
1. Set mask logic "0" (logic "1" nonmask).
2. All mask set at initial reset time.

2.2 3302 FMT DISK DRIVE CONTROLLER

The 3302 FMT disk drive controller, also called the Hard Disk Controller (HDC) or FMT PCB, resides in the model APC-H26 stand-alone DKU and provides the interface and control signals to the disk drive assembly within the stand-alone DKU and the disk adapter in the APC control unit (see Figure 2-7). Also, the FMT PCB provides the interface to the disk drive in the expansion DKU when included in the system. The physical dimensions and attached interface and power connector placements for the FMT PCB are shown in Figure 2-8. The 3302 FMT controller is composed of four sandwiched layers, including the signal ground and dc power plains. The major logic elements are as follows.

- Z80 compatible microprocessor (μPD780).
- 8K RAM of local memory.
- 2K ROM for disk drive firmware.
- D8237 DMA controller that interfaces with the disk adapter, local memory and the disk drive.
- D8255AC Programmable I/O device designed to control the transmission of the disk drive status, the device address/head address, and the step pulse for a seek operation.
- μPD3302 disk control LSI which is controlled by a subcommand sequencer. It (LSI) is intended to perform a serialize/deserialize operation on data to or from the disk drive and to modulate/demoduolate the MFM recorded data.
- 8065 BEP LSI intended to perform polynomial functions and to generate correctable 1 bit burst type errors.

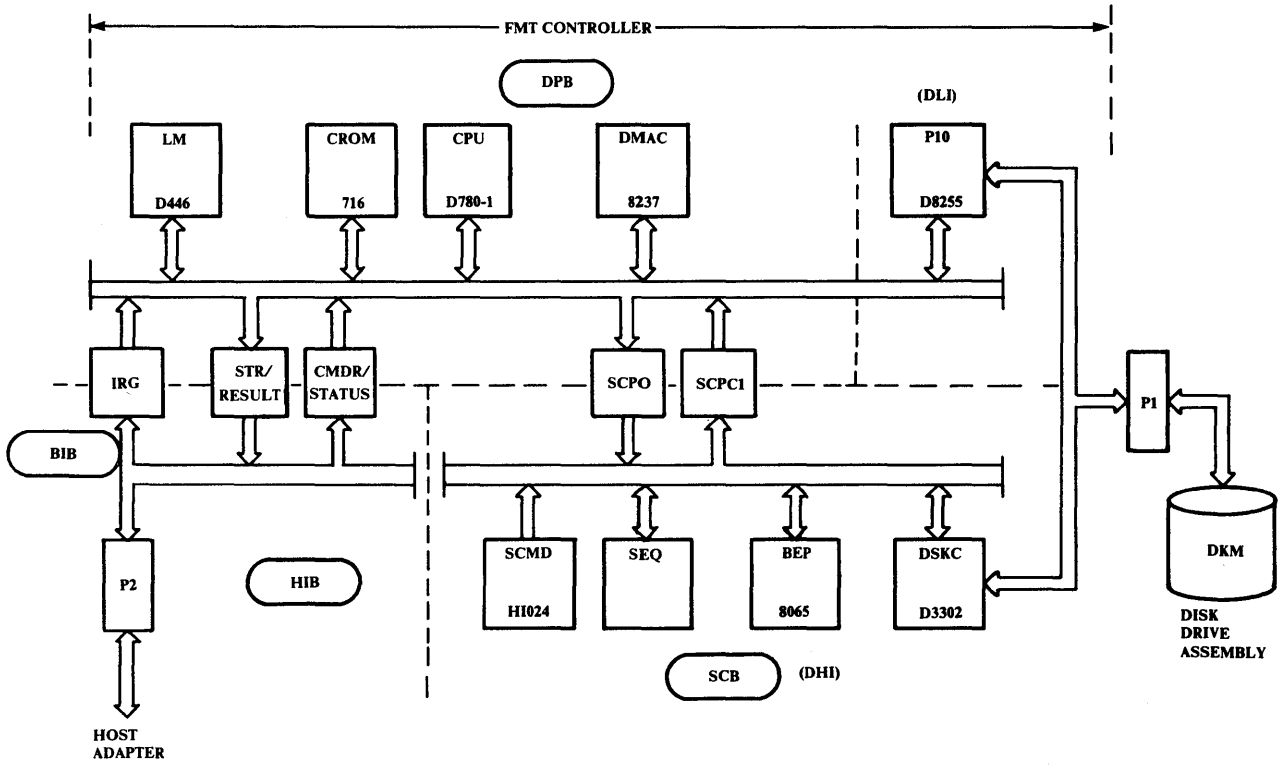


Figure 2-7 FMT Block Diagram

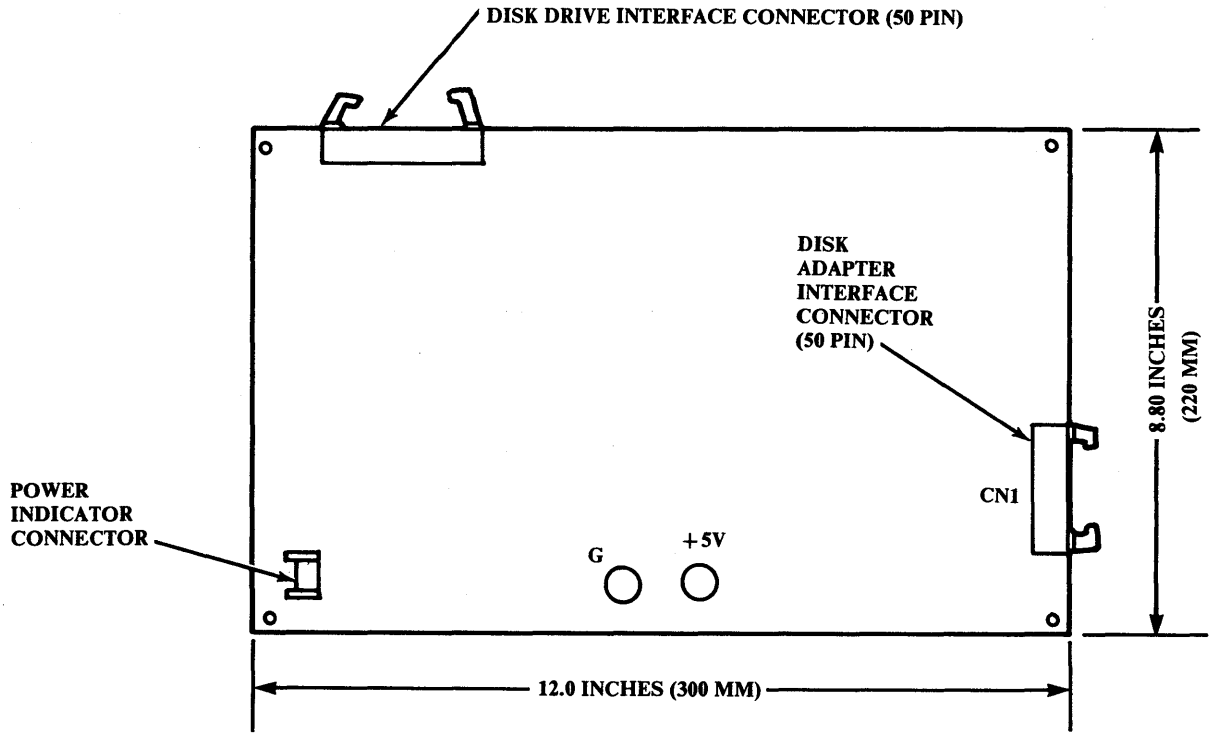


Figure 2-8 FMT PCB Physical Configuration

2.1.1 FMT Disk Operations

This section summarizes the functional capabilities of the FMT PCB operations. A more detailed description of each operation is provided in subsequent sections.

1. Performs seek operations to read or write data on a disk by moving the arm assembly (Read/Write heads) to the specified disk address.
2. Recalibrates the disk at head zero, cylinder zero.
3. Performs a read address seek operation to the specified disk address for transmission of the address to main memory.
4. Reads up to one cylinder of data from the DKU for transmission to main memory.
5. Writes up to one cylinder of main memory data into the DKU.
6. Verifies the transmission of up to a cylinder of data by checking the CHECK BYTE.

2.2.2 Firmware Overview

This section briefly describes the firmware characteristics and summarizes the firmware operation.

2.2.2.1 FIRMWARE CHARACTERISTICS

Firmware for the FMT PCB resides in the Z80 microprocessor, also called the Central Processing Unit (CPU), and provides the control procedures for all read/write and seek operations to the disk drive. It performs these procedures by decoding the main processor I/O instructions from the APC disk adapter. Firmware visibility with the adapter is provided by three registers; IR0, IR2, and IR3, all of which, reside on the FMT PCB (see Figure 2-9 and Table 2-2).

The transfer of data to form the command status and parameter/result status between the adapter and FMT is performed in the IR2 and IR3 registers (see Table 2-8). That is, initially, a disk command and its parameters are set in the IR2 and IR3 registers with an I/O command. The FMT firmware is then started and the data is stored in local memory. The Z80 CPU accepts and executes the I/O command. On completion the status is set in the IR2 and IR3 registers where they are sent to the main memory processor through the disk adapter. The IR0 register is used with firmware to set the command and receive the status (see Tables 2-9 through 2-11). The quantity of data transferred from or to the disk adapter corresponds to the number of sectors specified in the parameter.

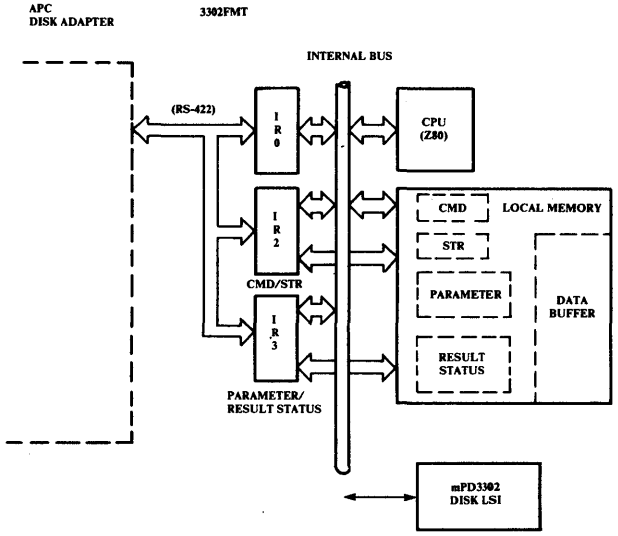


Figure 2-9 Firmware Hardware Interface

Table 2-8 FMT I/O Read/Write (Status) Commands

FMT COMMAND	R/W	I/O ADDRESS	3302 FMT
Result Status Read	R	AO	IR3 Read
Parameter Write	W	AO	IR3 Write
Status Read	R	92	IR2 Read
Command Write	W	92	IR2 Write

Table 2-9 FMT I/O Commands (RD/WR)

COMMAND	R/W	I/O ADDRESS	DATA BUS (LOW PART)							
			D7	D6	D5	D4	D3	D2	D1	D0
IR0 Read	R	A2	—	CB	DACKH	—	—	CE	LV2	SRQ
IR0 Write	W	A2	INTI	CLDB	RSTR	CLCE	0	E0P	0	HSRQ

Table 2-10 IR0 Write

DATA	NAME	DESCRIPTION	REMARKS
D0	HSRQ	SRQ interrupt mask	
D1	0	Must be zero	
D2	EOP	Notifies completion of the access to IR2/IR3 in the command set or status receive procedure...	After setting this bit, procedure completes 2 more accesses to IR2/IR3.
D3	0	Must be zero	
D4	CLCE	Interrupt LV2 reset	
D5	RSTR	Request start of the result status receiving procedure.	
D6	CLDB	Request start of disk command set procedure.	
D7	Initialize	Reset for 3302 FMT. Set 'ON', next 'OFF'. This signal must be more than 2 μsec.	AUX command corresponds to RST.

Table 2-11 IR0 Read

DATA	NAME	DESCRIPTION	REMARKS
D0	SRQ	Seek end, equipment check, ready change: '1' Issue of sense interrupt request command requested. HSRQ masking constitutes a factor in the generation of LV2.	The same as bit 4 of STR (IR2, read)
D1	LV2	Interrupt signal	LV2 = HDIN = CE + SRQ·$\overline{HSRQ}$
D2	CE	End of disk command: '1' Next command setting or CLCE setting: '0' LV2 interrupt factor.	CE = CEL + CEH corresponds to bit 6 (CEH) and bit 5 (CEL) of STR.
D3	—	Don't care	
D4	—	Don't care	
D5	DACKH	'1': CLDB disk command setting mode and RSTR result status receiving mode are started and internal DMA is started for data transfer via IR3 register.	'1' is given on the command run of read/write data also.
D6	CB	Formatter busy.	The same as bit 8 of STR.
D7	—	Don't care	

2.2.2.2 FIRMWARE OPERATIONAL OVERVIEW

There are six operational phases performed by internal firmware. They consist of a Seek Command phase, an Idle phase, a Clear Data Buffer (CLDB) phase, a Run phase, a Control End (CE) phase, and a Result Status Read (RSTR) phase. Each is briefly described below.

1. Seek Command —Denotes a seek operation occurred in the idle state and sets LV2 (SRQ) interrupt (usually at end of seek).
2. Idle phase —Waits for, accepts, and processes seek commands and associated command parameters.
3. CLDB phase —Stores the command and command parameters and sequence steps for the next phase.
4. Run phase —Executes the command, processes the applicable data, and sets the LV2 (CE) interrupt at the end of the command cycle.
5. Control End (CE) phase —Status read into IR0/IR2.
6. Result Status Read (RSTR) —Result status read into IR3.

2.2.2.3 FIRMWARE START UP

The FMT firmware start up procedure is the same as that for the Hard Disk Controller (HDC) LSI. However, the start up I/O instruction to set the command and receive the status differ somewhat, and must be performed as shown in Figures 2-10 and 2-11 and described below.

1. Command Set
   a. Check Status Register for Controller Busy (CB).
      - If busy, wait.
      - If not busy continue with step b.
   b. Initiate Clear Data Buffer (CLDB) command through the auxiliary command register.
   c. Check status register for DACKH signal being on.
      - If on, continue with step d.
      - If off, wait.
   d. Send first parameter to Data Buffer Register.
   e. Send each additional parameter, one after the other to the data buffer register. There is a minimum of 2 between transfers.

f. Before sending the last parameter, initiate an End of Process (EOP) command through the auxiliary command register.
g. After last parameter is sent, send command to the command register.
h. Check Status Register for DACKH to be off.
i. When DACKH is off, The Central Processing Unit (CPU) can perform other operations, because HDC will signal when it is completed by sending an interrupt.

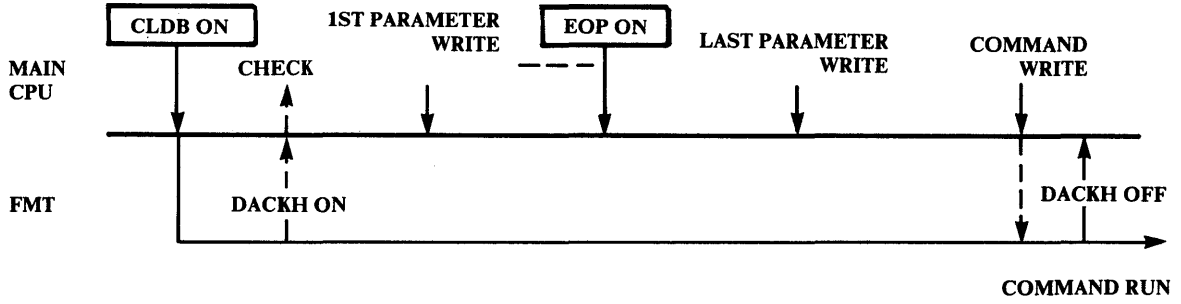
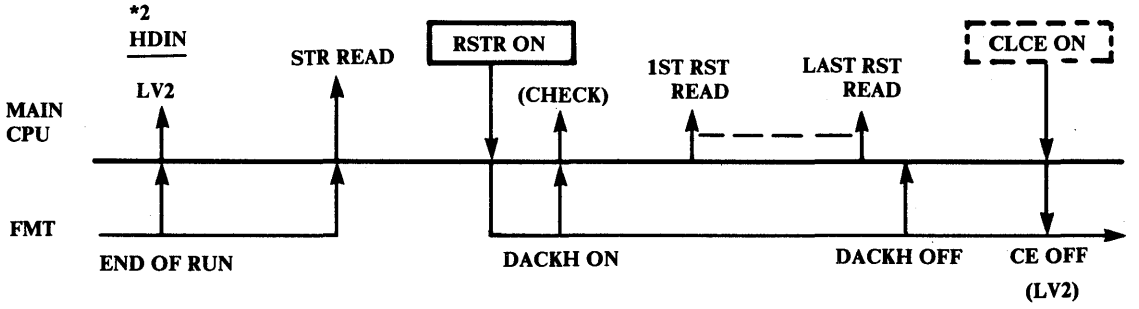


Figure 2-10 Command Set



*2 HDIN = LV2 = CE + SRQ*HSRQ

Figure 2-11 Receive Result Status

2. Receive Result Status
   a. Wait for interrupt to occur.
   b. Read interrupt register to determine what type of interrupt occurred.
   c. If an HDC interrupt has occurred, read the status register.
   d. If status/command indicates that it is necessary to read the request Result Status Read (RSTR) command through the auxiliary command register.
   e. Check status to see if DACKH is on.
      - If on, continue with step b.
      - If off, wait.
   f. Continue to read additional status, one after the other, as the command requires. A minimum of 2 is required between transfers.
   g. After last parameter is read, check status register for DACKH signal to be off. Indicates that the procedure is completed.
   h. Proceed to next command.

2.2.2.4 FIRMWARE FUNCTIONAL NOTATIONS

This section highlights the major DKU operations that a user should be aware of to understand the operation of the hard disk. The user should reference Figure 2-12 through 2-17 and Tables 2-12 through 2-18. The figures provide a flowchart of the Firmware operations, the sector format, and the appropriate timing diagrams. The tables provide the command code (Bits D7 through D4) for each command, the command name and resultant parameters, the appropriate parameters for each command, and tabulates the status in the respective status registers. Additional information is provided in Section 2.2.3.

1. A cylinder seek occurs with a Power On Reset operation or with a reset I/O command from the disk adapter (see Figure 2-12).

   A recalibrate operation is performed after every reset command.

2. After IRQ CLDB is set in a command set operation, the command operation requires a maximum delay of 50 secs for DACKH to turn on, after which, the command set operation continues. After EOP sets, the command set operation ends with two access operations (last parameter and command) and DACKH turns off.

3. The receive status operation also requires a maximum delay of 50 secs for DACKH to turn on. After RSTR sets, the operation is the same as described in step 2 above. With the number of status results determined by an execute I/O command, DACKH turns off after the final status result is read. When the number of read status is smaller than the number of result status, stalls occur causing a wait state.
4. In some cases DACKH turns on during the execution of a read/write data command.
5. The command set and receive status operations cannot be reset once they are in operation.
6. In seek and recalibrate command operations an SRQ interrupt occurs after Control End (CE) is on resulting in a new time difference between the interrupt and CE. A new command can be executed with CE on during any SRQ occurence.
7. In systems equipped with two or more DKUs a new command to the second DKU is permissible as the first DKU is performing a seek operation. An SRQ interrupt is sent when the new command ends, but the SRQ status is held until this time. However, the SRQ status is reset if the DKU that ended a seek command commences another command before accepting the SRQ status. Accordingly, a seek command can be sent to the same DKU after the SRQ status is received.

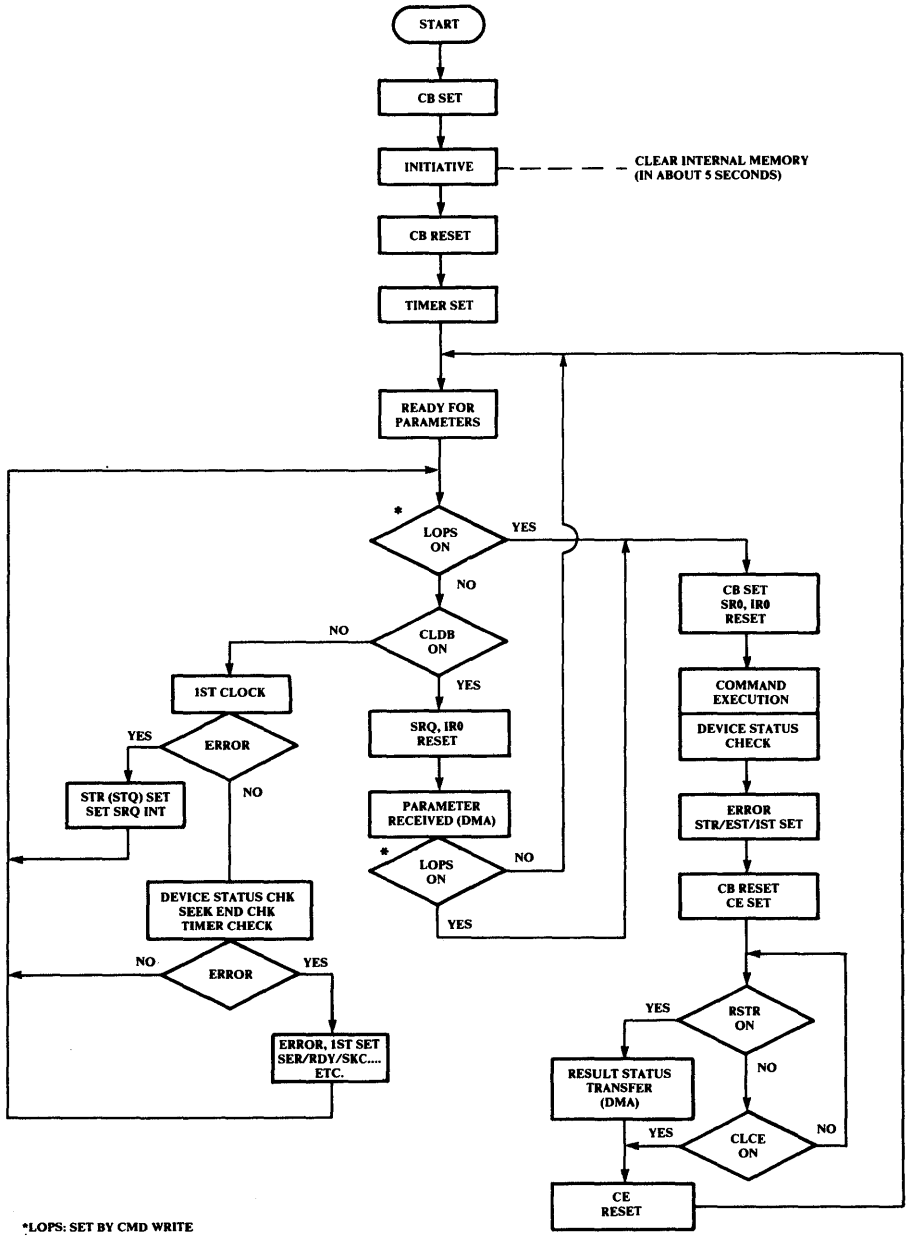


Figure 2-12 FMT Firmware Flowchart

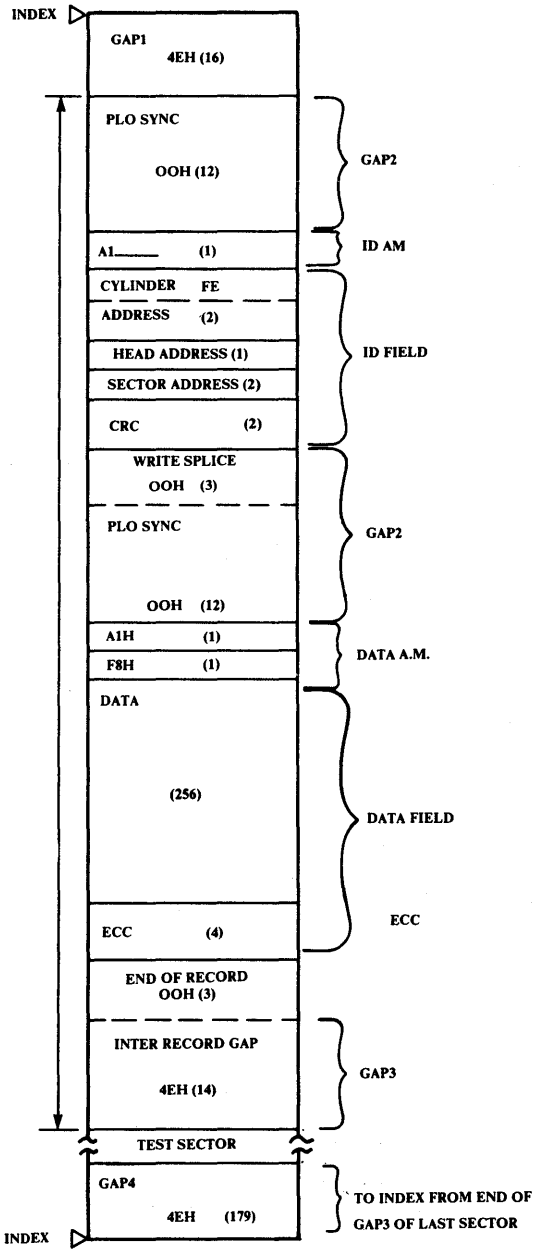


Figure 2-13 Sector Map (Disk)

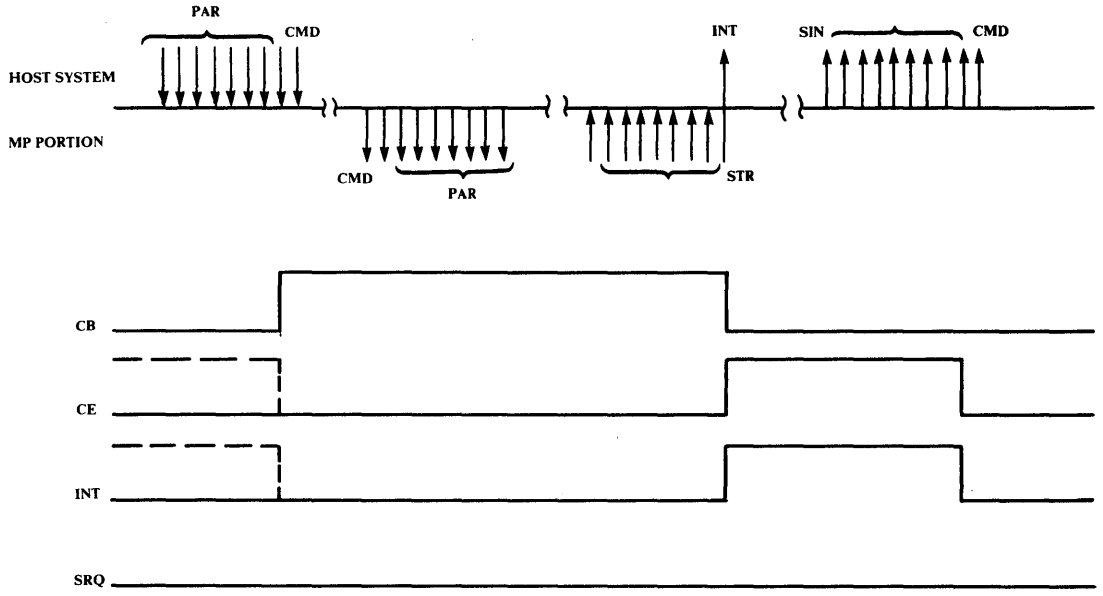


Figure 2-14 Read/Write Command Timing

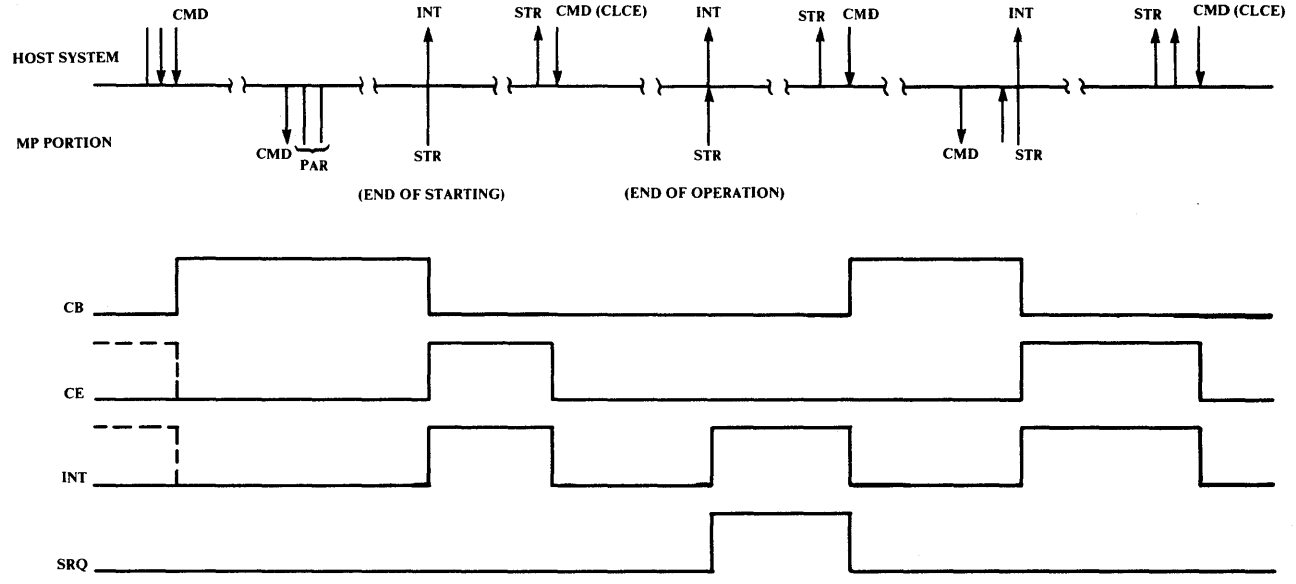


Figure 2-15 Seek/Recalibrate Timing

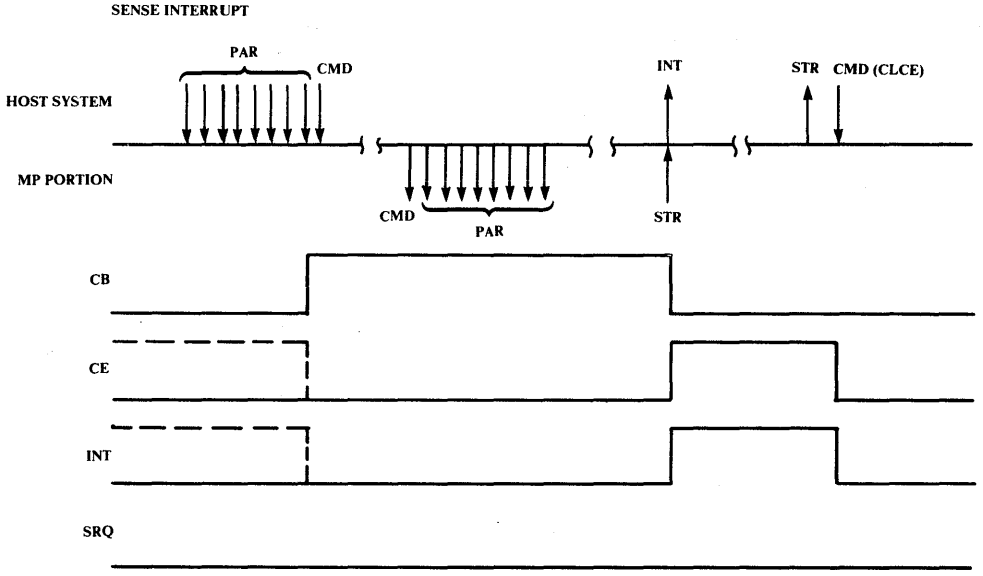


Figure 2-16 Sense Interrupt Timing

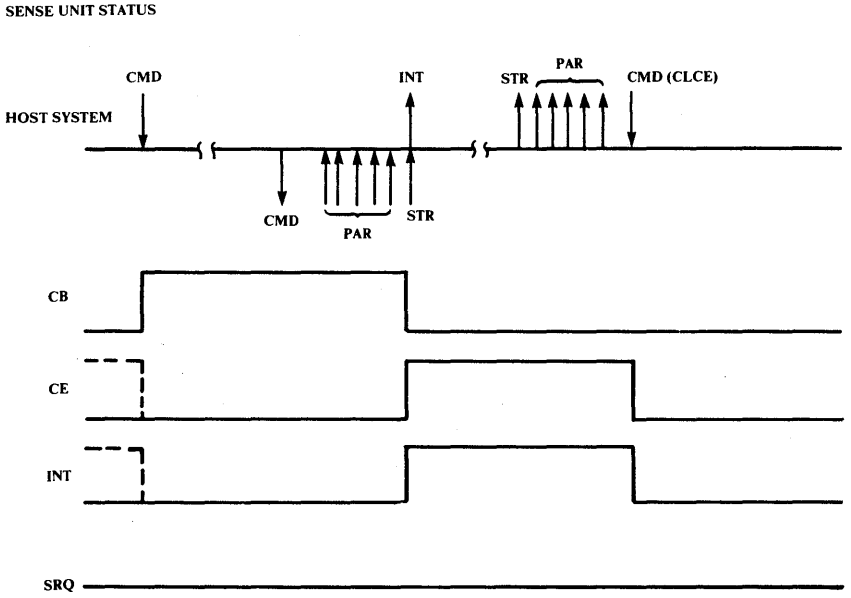


Figure 2-17 Sense Unit Status

Table 2-12 Commands/Status Results

COMMAND	OPERATIONAL PHASE	COMMAND BIT A0 = X*	Data Register (Low Byte)** D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Recali-brate	Command	0	0 1 0 1 0 UA	Command and unit address (UA)
	Result	0	Status Register	Status Register (STR)
Seek	Command	0	0 1 1 0 1 UA	Command and unit address
		1	Physical Cylinder Number	High Byte (PCNH)
		1	Physical Cylinder Number	Low Byte (PCNL)
	Result	0	Status Register	STR
Write ID	Command	0	0 1 1 1 0 UA	Command and unit address
		1	Physical Head Number	PHN
		1	Sector Count	SCNT
		1	Data Pattern	DPAT
		1	Gap Length 1	GPL1
		1	Gap Length 3	GPL3
	Result	0	Status Register	STR
		1	End Status	EST
			Sector Count	SCNT
Read ID	Command	0	1 0 0 1 0 UA	Command and unit address
		1	Physical Head Number	PHN
		1	Sector Count	SCNT
	Result	0	Status Register	STR
		1	End Status	EST
		1	Sector Count	SCNT

Table 2-12 Commands/Status Results (cont'd)

COMMAND	OPERATIONAL PHASE	COMMAND BIT A_0 = X*	DATA REGISTER (LOW BYTE)** D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Read Data		0	1 0 1 1 X UA	Command and unit address (UA)
	Command	1	Physical Head Number	PHN
		1	Logical Cylinder Number	High Byte (LCNH)
		1	Logical Cylinder Number	Low Byte (LCNL)
		1	Sector Count	SCNT
	Result	1	Status Register	STR
		1	End Status	EST
		1	Physical Head Number	PHN
		1	Logical Cylinder Number	High Byte (LCNH)
		1	Logical Cylinder Number	Low Byte (LCNL)
		1	Logical Head Number	LHN
		1	Logical Sector Number	LSN
		1	Sector Count	SCNT
Check		0	1 1 0 0 X UA	Command and UA for CMD set.
	Command	1	Physical Head Number	PHN
		1	Logical Cylinder Number	High Byte (LCNH)
		1	Logical Cylinder Number	Low Byte (LCNL)
		1	Logical Head Number	LHN
		1	Logical Sector Number	LSN
		1	Sector Count	SCNT
	Result	0	Status Register	STR
		1	End Status	EST
		1	Physical Head Number	PHN
		1	Logical Cylinder Number	High Byte (LCNH)
		1	Logical Cylinder Number	Low Byte (LCNL)
		1	Logical Sector Number	LSN
		1	Sector Count	SCNT

Table 2-12 Commands/Status Results (cont'd)

COMMAND	OPERATIONAL PHASE	COMMAND BIT A_0 = X*	DATA REGISTER (LOW BYTE)** D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Write Data	Command	0	1 1 1 1 X UA	Command and unit address (UA)
		1	Physical Head Number	PHN
		1	Logical Cylinder Number 1	LCN 1
		1	Logical Cylinder Number 2	LCN 2
		1	Logical Head Number	LHN
		1	Logical Sector Number	LSN
		1	Sector Count	SCNT
	Result	0	Status Register	STR
		1	End Status	EST
		1	Physical Head Number	PHN
		1	Logical Cylinder Number 1	High Byte (PCNH)
		1	Logical Cylinder Number 2	Low Byte (PCNL)
		1	Logical Head Number	LHN
		1	Logical Sector Number	LSN
		1	Sector Count	SCNT
Sense Interrupt Status	Command	0	0 0 0 1 X X X X	For CMD set
	Result	0	Status Register	STR
		1	Interrupt Status	IST
Sense Unit Status	Command	0	0 0 1 1 X UA	Command and unit address (UA)
		1	Status Number n	STN n
		1	Status Number n	STN n N=1: Summary Status =2: Detailed Status (HDC Detail 6) Set: Status number only
	Result	0	Status Register	STR
		1	Unit Status n	USTn n=same as
		1	Unit Status n	USTn above

Table 2-12 Commands/Status Results (cont'd)

COMMAND	OPERATIONAL PHASE	COMMAND BIT A_0 = X*	DATA REGISTER (LOW BYTE)** D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Invalid	Command	0	All Zeroes	Command
	Result	0	Status Register	STR (60)
Detect Error	Command	0	0 1 0 0 X X X X	For CMD set
	Result	0	Status Register	STR
		1	Error Address	High Byte (ADRH)
		1	Error Address	Low Byte (ADRL)
		1	Error Pattern 1	EPAT 1
		1	Error Pattern 2	EPAT 2
		1	Error Pattern 3	EPAT 3

* A_0 = 0—Command Register or status register access.
A_0 = 1—Parameter or result status access.
** Data register bits D7 through D4—command code.

Table 2-13 Parameters

COMMAND	PARAMETERS	
	NAME	HEX VALUE
SEEK	Present Cylinder Number High (PCNH) Byte	0
	Present Cylinder Number Low (PCNL) Byte	00 to B4
Write ID Write Data Read ID Read Data Check	Present Head Number (PHN)	00 to 07
	Sector Count (SCNT)	00 to FF
Write ID	Data Pattern (DPAT)	Any
	Gap Length 1 (GPLI)	10
	Gap Length 3 (GP3)	0E
Check Read Data Write Data	Logical Cylinder Number High (LCNH) Byte	FE
	Logical Cylinder Number Low (LCNL) Byte	00 to B4
	Logical Head Number (LHN)	00 to 07
Sense Unit Status	Logical Sector Number (LSN)	00 to 19
	Status Number 1 (STN 1)	Any

Table 2-14 (STR) Status Register

BIT NO.	NAME	ABBRE-VIATION	DESCRIPTION
D7	Controller	CB	1: a command is sent to HDC from the host system. 0: Controller busy (D7) reset when the host system is interrupted by HDC.
D6 D5	Command End	CEH	D6 | D5 0 | 0 Command in progress or no command sent after last reset signal or CLCE. 0 | 1 : Abnormal End 1 | 0 : Normal End 1 | 1 : Invalid Ending
D4	Sense Interrupt Status Request	SRQ	With SEN, EQC, or a change in RDY detected this bit (D4) sets initiating a SRQ from HDC.
D3	0	—	
D2	0	—	
D1	0	—	
D0	X	—	

Table 2-15 (EST) Error Status

BIT NO.	NAME	ABBRE-VIATION	DESCRIPTION
D7	End of Cylinder	ENC	Set when access is continued beyond the maximum sector number of one cylinder.
D6	0	—	
D5	Data Error	DER	Set when the data on a disk is read and an error is detected.
D4	Equipment Check	EQC	Set when a 'fault' signal is reported by the device.
D3	Not Ready	NR	Set when the device cannot perform both read and write.
D2	No Data	ND	Set when a designated sector is not detected on the track.
D1	0	—	
D0	Missing Data Mark	MDM	Set when a disk is read and the address mark of the data portion is not detected.

Table 2-16 (IST) Interrupt Status

BIT NO.	NAME	ABBRE-VIATION	DESCRIPTION
D7	Seek End	SEN	End of seek operation
D6	Ready Change	RC	The status of the device has changed.
D5	Seek Error	SER	A seek error has occurred.
D4	Equipment Check	EC	Set when a 'fault' signal is reported by the device or track '0', seek complete signal is not detected within a fixed time on 'seek' or 'recalibrate' command run.
D3	Not Ready	NR	Set then the device cannot perform both read and write.
D2	Unit Address	UA2	The device number on interruption.
D1		UA1	
D0		UA0	

Table 2-17 (US1) Unit Status 1

BIT NO.	NAME	ABBRE-VIATION	DESCRIPTION
D7			
D6			
D5			
D4	1 (Must Be One)		1
D3	Seek Complete	SC	End of seek operation
D2	Track 00	T0	Positioner is positioned at cylinder '0'.
D1	Ready	RDY	The spindle makes enough revolutions and the data area is normally loaded with a R/W head.
D0	Write Fault	WF	Turns on in any of the following cases. • Loss of Voltage • Clock Fault • Positioner of Track • Write Fault • Head Fault • Head Select Fault

Table 2-18 (US2) Unit Status 2

BIT NO.	NAME	ABBRE-VIATION	DESCRIPTION
D7			
D6			
D5			
D4			
D3			
D2	Device Type	DT	Always a 1-10 MB DKU
D1	Detailed Status 1	ST1	The code—ST0 or 1—of the detailed status information held by the device.
D0	Detailed Status 0	ST0	ST0 ST1 0 0 Spindle Speed Loss 0 1 Not Track 000 1 0 Read/Write Fault 1 1 -------

2.2.3 Command Functional Overview

This section provides a brief functional description of the following disk commands.

- Check
- Read Data
- Read ID
- Recalibrate
- Write Data
- Write ID
- Seek
- Sense Interrupt Status
- Sense Unit Status

2.2.3.1 CHECK COMMAND

The data from the data sector, selected by the Logical Cylinder Number High Byte (LCNH), Logical Cylinder Number Low Byte (LCNL), Logical Head Number (LHN), and the Logical Sector Number (LSN) during the command phase, is read but is not sent to the host system. It is treated in the same manner as a read data command described in steps 2 through 9 of the next section.

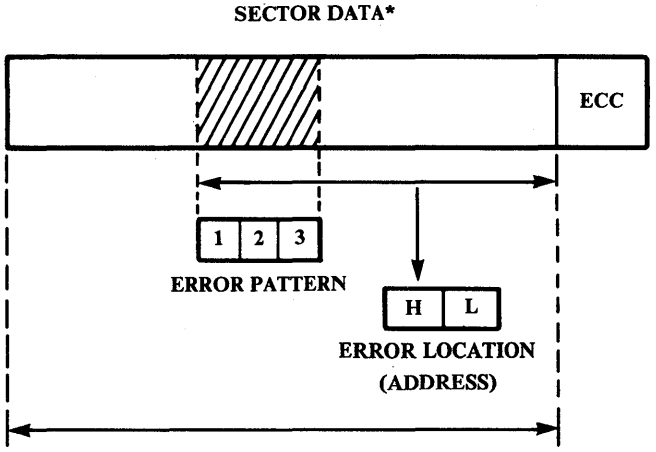
2.2.3.2 READ DATA COMMAND

1. The sectors designated by the Logical Cylinder Number High (LCNH) byte, the Logical Cylinder Number Low (LCNL) byte, the Logical Head Number (LHN), and the Logical Sector Number (LSN), activated during the command phase, are read from the DKU selected by the Unit Address (UA). This address is contained in the command word (see Table 2-12) from the host disk adapter.
2. Upon completion of a sector read operation in a multi-read sector operation, the Sector Count (SCNT) and LSN signals are upgraded to read data from the next sector.

   When the SCNT reaches zero the result (end) status is set with a stop instruction and the host adapter is notified accordingly.

   If the LSN equals the End Sector Number (ESN), the LHN is changed and the read process continues.
3. If the SCNT does not equal zero upon completion of read from the last sector, that is, the Last Sector Number (LSN) = the End Sector Number (ESN) or the Logical Head Number (LHN) = the End Track Number (ETN), the command run sequence is terminated with the End of Cylinder (ENC) bit on in the Error Status (EST) byte (see Table 2-15). The Status Register (STR) shows an abnormal ending (see Table 2-14).
4. When a fault signal is read from the device, command run is terminated with the Equipment Check (EQC) bit on in the EST byte. The STR shows an abnormal ending.
5. If the device is Not Ready (NRY), command run is terminated with the NRY bit on in the EST byte.

6. If a read error is detected in the Error Correct Code (ECC), the error is checked to determine if it is a recoverable or unrecoverable error. If recoverable, the error location and data pattern are stored and command run is terminated with the Data Error (DER) bit on in the EST byte (see Table 2-15). The host fetches this information with the detect error command to make the necessary corrections.



* SEE FIGURE 2-13

If an unrecoverable error was detected the detect error command is terminated with the DER bit on in the EST byte. The Status Register (STR) shows an abnormal ending (see Table 2-14).

7. If a designated sector is not found after a second index mark is detected, command run is terminated with the No Data (ND) bit on in the EST byte. The STR shows an abnormal ending.

8. When the Terminal Count (TC) signal turns on, data transfers to the host stops. However, a sector read operation continues until the sector designated by the Sector Count (SCNT) is found, or until another abnormal operation occurs.
9. The resulting status for a normal termination of a command are shown below.

Normal End Status

LAST SECTOR TRANSFERRED			RESULT STATUS			
LCNL	LHN	LSN	LCNH	LCNL	LHN	LSN
		0 ESN-1	No change	No change	No change	LSN+1
	0 ETN-1	ESN	No change	No change	LHN + 1	00
LCVL≠256	ETN	ESN	No change	LCNL+1	00	00
LCNL≠256	ETN	ESN	LCNH+1	00	00	00

NOTE: LHN (PHN) shows the head number for the last sector data transfer.

With an abnormal command termination the error position is set as the result status.

10. If a data address is not present after the VFO SYNC for data, command run is terminated with the Missing Data (MDM) bit on in the EST byte.

2.2.3.3 READ ID

1. A read ID operation reads the cylinder, head and sector address and the Cyclic Redundancy Character (CRC) from the ID field starting with the first sector on a track designated by the Physical Head Number (PHN) signal (see Figure 2-14). If the CRC is normal (no errors) and the address data is sent, the process stops after sending one ID data field, and command run is terminated. If abnormal, the ID data field is not sent and the process continues.
2. When a sector read operation is incomplete before SCNT equals zero, the result status contains a No Data (ND) status and the host is notified accordingly.

3. If a fault signal is received from the device the commmand run terminates with the Equipment Check (EQC) bit on in the EST byte (see Table 2-15).
4. If the device is Not Ready (NRY), command run is terminated with the NRY bit on in the EST byte.
5. If a designated sector is not found after a second index mark is detected, command run is terminated with the ND bit on in the EST byte.

2.2.3.4 RECALIBRATE

1. Seek to cylinder zero.
2. Recalibrate End of Start—Command run is normally ended after a step pulse signal is sent 256 times.
3. Recalibrate End of Operation—Track zero (T0) signal is checked at the above fixed pulse rate. When set, the recalibrate operation is normally terminated with Seek End (SEN) bit on in the IST (see Table 2-16) and the Sense Interrupt Status Request (SRQ) set.

   If the T0 (00) signal is not on after the above rate is exceeded, the recalibrate operation is terminated with the Seek Error (SER) BIT on in IST.

   If the device is Not Ready (NRY) or a fault is detected the recalibrate operation is terminated with the NRY or EQC bit on.
4. The Interrupt Status (IST) is set and the host system obtains the result of the recalibrate operation with the Sense Interrupt Status command (see Section 2.2.3.8).

2.2.3.5 WRITE DATA

1. Data from the host system is written to the sector designated by the Logical Cylinder Number High (LCNH) byte, the Logical Cylinder Number Low (LCNL) byte, the Logical Head Number (LHN), and the Logical Sector Number (LSN) in the DKU selected by the Unit Address (UA) field in the command byte (see Table 2-12).
2. Upon completion of a sector write operation, in a multi-write disk operation, the sector counter (SCNT) and the LSN signals are upgraded to write data in the next sector.

   When the SCNT reaches zero the result (end) status is set with the stop instruction and the host system is notified accordingly.

   If the LSN equals the End Sector Number (ESN), the LHN is changed to LHN + 1, the head assignment is changed, and the write process continues.

3. If the SCNT does not equal zero upon completion of a write in the last sector, the command run sequence is terminated with the End of Cylinder (ENC) bit on in the Error Status (EST) byte (see Table 2-15).
4. When a fault signal is received from the device, command run is terminated with the Equipment Check (EQC) bit on in the EST byte.
5. If the device is Not Ready (NRY), command run terminates with the NRY bit on in the EST byte.
6. If a designated sector is not found after a second index mark is detected, command run is terminated with the No Data (ND) bit on in the EST byte.
7. The resulting normal ending status is shown in the chart in step 9, Section 2.2.3.2.
8. When the Terminal Count (TC) signal turns on, all zeroes are written on the remaining sector area. However, the sector write operation continues until the sector count in the SCNT is reached, or until an abnormal operation occurs.

2.2.3.6 WRITE ID

1. A write ID operation writes the cylinder, head and sector address, and causes the generation of the Cyclic Redundancy Character (CRC) in the ID field starting with the first sector following the index mark on a track designated by the Physical Head Number (PHN).
2. Upon the completion of a write sector operation and the Sector Counter (SCNT) equals zero, the result (end) status is set with a stop instruction and the host system is notified accordingly.
3. If a fault signal is detected from the device the command run terminates with the Equipment Check (EQC) bit on in the Error Status (EST) byte (see Table 2-15).
4. If the device is Not Ready (NRY), command run is terminated with the NRY bit on in the EST byte.

2.2.3.7 SEEK OPERATION

1. Causes arm/head assembly to seek (search) the disk (platters) for the Object Cylinder Number (OCN) designated by the Physical Cylinder Number (PCNH/PCNL) during the command pause.

2. End of Seek Start Operation

   With the Present Cylinder Number (PCN) less than the OCN, repeat PCN+1 and command run (Step in Pulse) until PCN equals OCN.

   With the PCN greater than OCN, repeat PCN-1 and command run (Step Out Pulse) until PCN equals OCN.

   In either case, with PCN equal to OCN, indicates that the command and parameter are received and command run terminates normally.

3. End of Seek Operation (Seek Complete)

   A Seek Complete (SC or SKC) signal is checked at a designated pulse rate. If this signal is on, the seek operation is terminated normally and the Sense Interrupt Status Request (SRQ) signal is on with Seek End (SEN).

   If the seek complete signal is not on after a fixed time interval (the difference between OCN and PCN), the seek operation terminates with the SER flag on.

   If the device is Not Ready (NRY) or a fault signal occurs, the seek operation is terminated and the NRY or EQC bit is on.

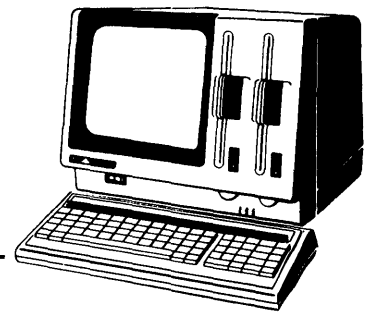
4. When the Sense Interrupt Status command is sent from the host the Interrupt Status (IST) flag is examined and the host is notified accordingly.

2.2.3.8 SENSE INTERRUPT STATUS

1. This command notifies the host of the following device status.
   - End of a seek operation (Seek or Recalibrate Operation).
   - Device ready or not ready.
2. If this command is sent without the Sense Interrupt Status Request (SRQ) signal on, an abnormal termination occurs.

2.2.3.9 SENSE UNIT STATUS

Notifies the host of a Unit Status 1 (US1) or Unit Status 2 (US2) device status (see Tables 2-17 and 2-18).



Chapter 3

Disk Drive Assembly

This chapter describes the physical characteristics and functional capabilities of the disk drive assembly used in the Model APC-H26 and Model APC-H27 Disk Units (DKUs). Both DKUs are briefly described in Chapter 1. DKU installation information is highlighted in subsequent sections with more detailed information provided in the Hard Disk Subsystem Installation Guide (Document No. 819-000102-9001).

The disk drive assembly is of modular construction designed to conserve space, enhance overall performance, and to eliminate periodic maintenance. The drive assembly uses 5.25 inch metal oxide platters, also called, disks or plates, and Winchester-type technology that provides the most modern method of storing information for high-speed computer operations and accessability. Many other features are available, several of which, are as follows.

1. Horizontal or vertical mounting.
2. 5-phase stepping motor (reduces track-to-track seek time to less than 2 ms).
3. Buffered operation (enhances random access seek operations).
4. Cam-operated swing arm mechanism (designed to support and drive the read/write heads).
5. Variable Frequency Oscillator (VFO—designed to process Return-to-Zero (RZ) data).
6. Winchester-type read/write heads (provides the latest recording method).

3.1 PHYSICAL/FUNCTIONAL ORGANIZATION

Figure 3-1 illustrates the modular construction and compactness of the disk drive assembly, and Figure 3-2 provides a functional block diagram of the disk drive logic. The disk drive assembly, also called the Disk Enclosure (DE), consists of a base plate, a swing out read/write head mechanism, magnetic read/write heads, a top sealing cover, and many other subassemblies shown in Figure 3-1. Note the "Air-Flow" path through the module when the sealing cover is in place. Included are the G9QKQ or G9NXT logic PCB and the G9QKR VFO PCB (the latter is not shown in the illustration).

The G9NXT PCB, and when installed, the G9QKR PCB, are referred to as a "Package Assembly" and provides the following disk drive logic functions (see Figure 3-2).

1. G9NXT Interface/Control Logic
   a. Interface Logic
      The interface logic consists of a microprocessor, LSIs, and other logic elements, designed to route data, addresses, device status and control signals between the disk drive and the FMT controller.
   b. Motor Logic (DC Motor AMP)
      The motor logic provides the dc power to drive the spindle motor and to control its rotational speed, and also to drive the stepping motor for seek operations.
   c. Read/Write Logic
      The read/write logic writes MFM-encoded data from the interface onto a disk (platter) and reads the MFM data from the selected disk and sends it to the interface logic for processing (also see VFO logic).
2. G9QKR VFO Logic
   The VFO logic separates clocks from MFM recorded data during a read data operation, synchronizes the clocks with the data, and sends the clocked data to the FMT as Read Clocks (RCK). The VFO performs no other operation and is required in both the stand-alone DKU and the expansion DKU.

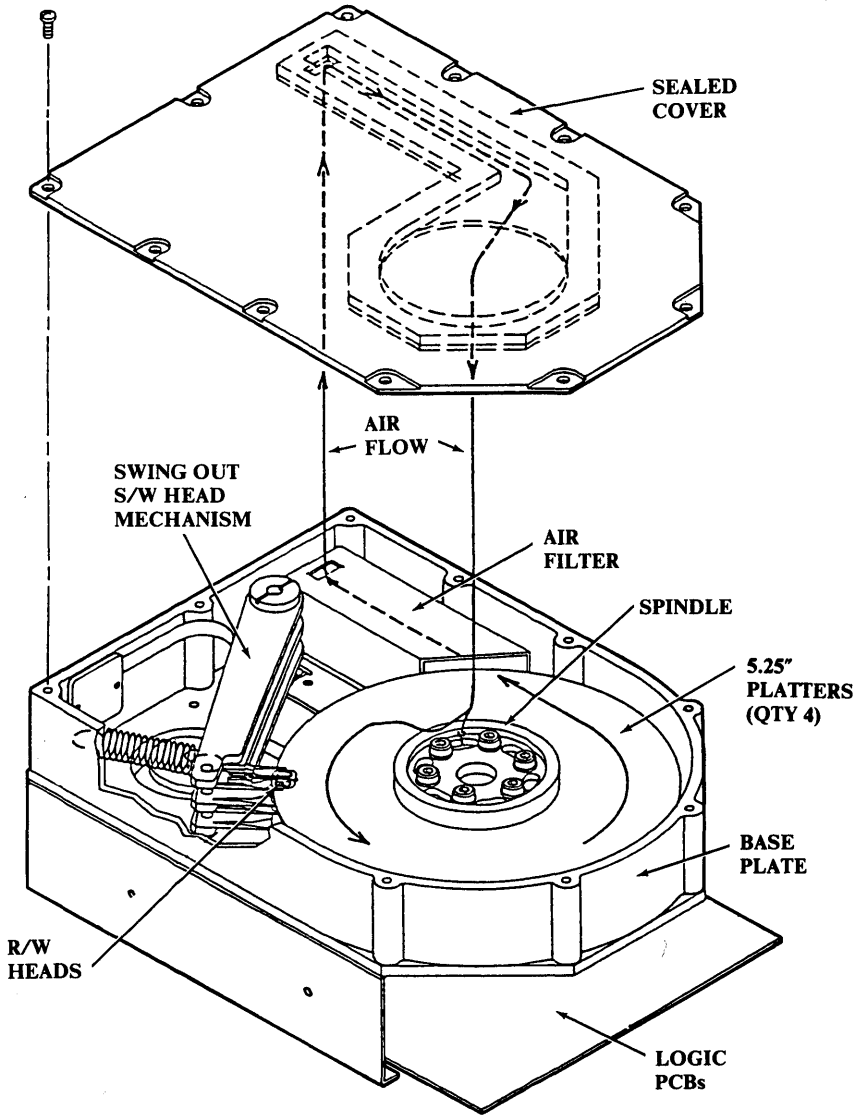


Figure 3-1 APC Disk Module (Exploded View)

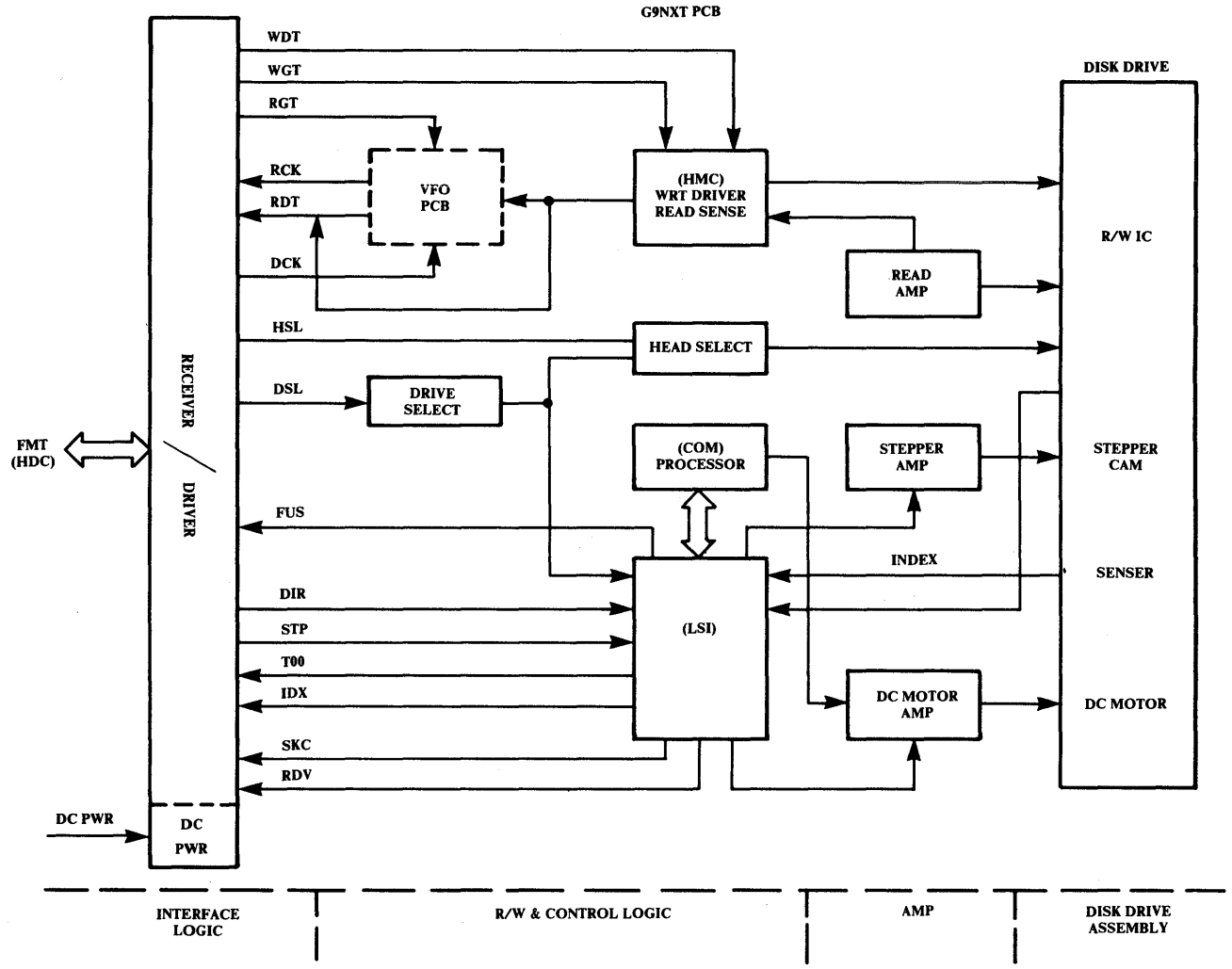


Figure 3-2 Functional Block Diagram

3.2 ENVIRONMENTAL CONSIDERATIONS AND FUNCTIONAL SPECIFICATIONS

The environmental considerations and functional specifications for the disk drive are the same as those for the DKU as described in chapter 1, Section 1.5. This is because the DKU houses the disk drive assembly and associated logic, power supply, and so forth. The only difference is the overall dimension and weight of the disk drive assembly when removed from the DKU, and are as follows.

	Disk Drive Assembly
1. Depth	8.12 inches (203 mm)
2. Height	4.06 inches (101.6 mm)
3. Width	5.84 inches (146 mm)
4. Weight	7.7 lbs (3.5 Kg)

3.3 ADDRESS/POWER/TERMINATOR CONNECTOR CONSIDERATIONS

The disk assembly contains the address, power, and terminator plugs and connectors as shown in Figure 3-3. The address and terminators are normally set at the factory. If changes are desired refer to the Hard Disk Subsystem Installation Guide for details. Additional connector information is provided in subsequent sections.

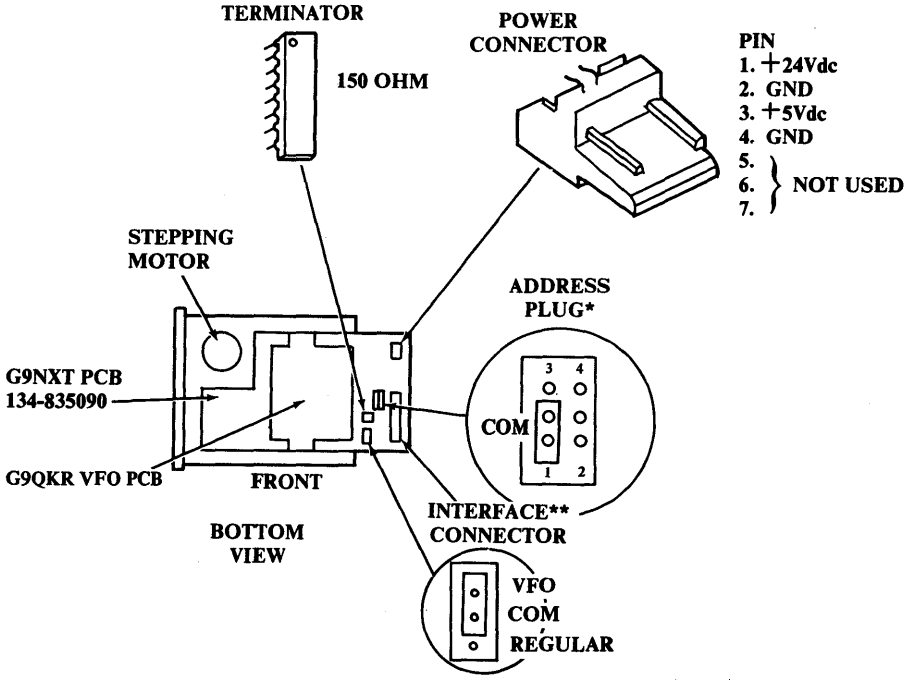
3.4 INTERFACE LOGIC CIRCUITS

Figure 3-4 illustrates a typical interface logic circuit used to process information between the disk drive assembly and the FMT controller. Positive logic is used as shown below.

Logic "0" = 0.00 Vdc to 0.40 Vdc
Logic "1" = 4.75 Vdc to 5.25 Vdc

3.5 INTERFACE CABLING CONSIDERATIONS

Figure 3-5 illustrates the type interface connector used on the disk drive assembly and provides the pin to pin assignment in each connector. Included are the signal names assigned to each pin.



* ADDRESS PLUG SET FOR MASTER (STAND-ALONE) DKU. SLAVE (EXPANSION) DKU-JUMPER PIN 2 TO COM (COMMON).
** CONNECTOR ON G9NXT PCB.

Figure 3-3 Terminator/Address Plug Layout

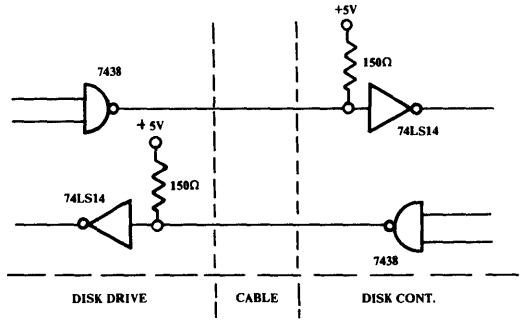


Figure 3-4 Typical Interface Logic Circuit

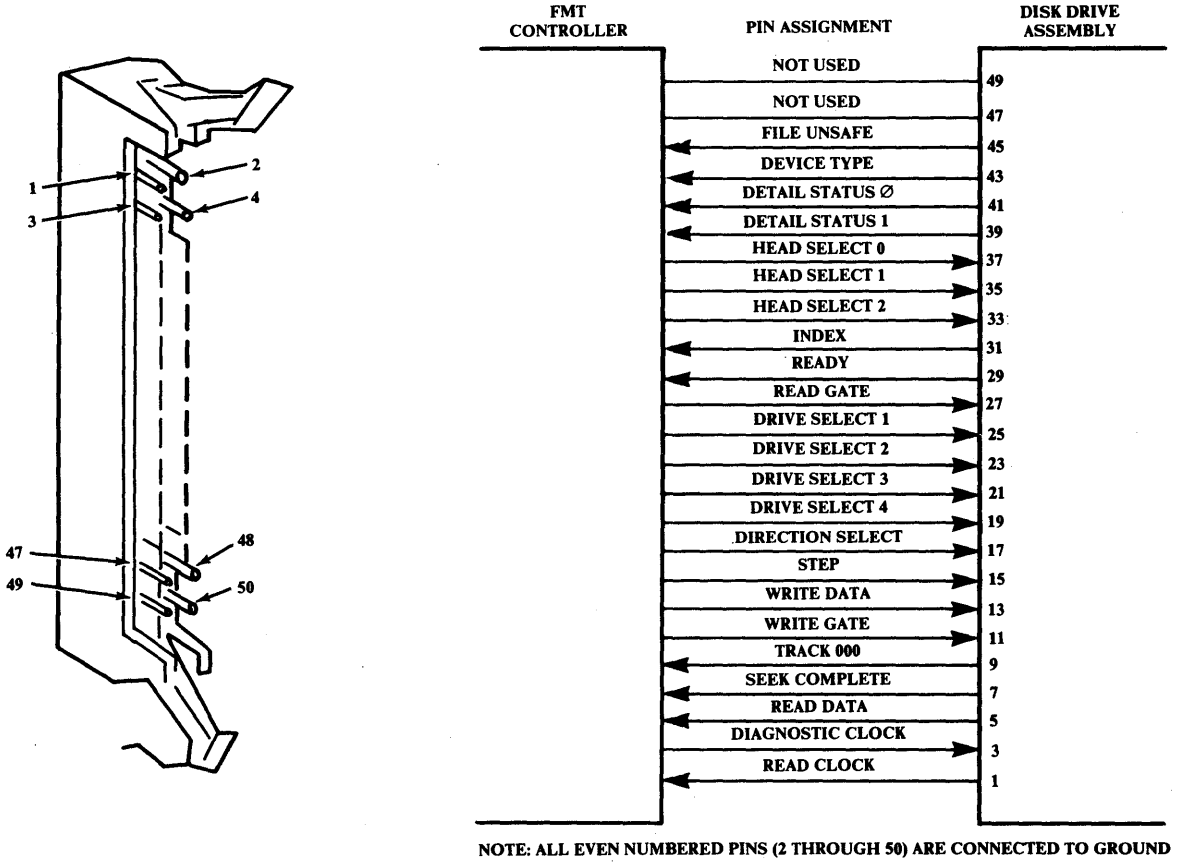


Figure 3-5 Interface Cable Connector/Pin Assignment

3.6 INTERFACE SIGNAL FUNCTIONS

This section briefly describes the function of the major interface signals used to control the flow of information through the interface logic to the FMT controller and to the disk drive assembly.

a. Detailed Status (ST0/ST1)—Defines the File Unsafe Status (FUS) as follows.

ST0	ST1	
0	1	see FUS step f1
1	0	see FUS step f2

b. Device Type (DTP)—Always a One (1) denoting a 10 MB disk drive.

c. Diagnostic Clock (DCK)—The DCK signal is used to substitute the read data signal in selected operations and is required for VFO synchronization in modes other than the read data mode. The clock period is 250 ns with a 50% duty cycle (nominal value).

d. Direction Select (DSL)—The DSL signal specifies the direction in which the read/write head assembly moves as shown below.

DSL = 0—Head assembly moves towards cylinder zero.

DSL = 1—Head assembly moves away from cylinder zero.

e. Drive Select 1 and 2 (DS1 and DS2)—The DS1 and DS2 lines enable a disk drive in the selected DKU. A disk drive is enabled and its input/output lines are active when its drive select line is low.

f. File Unsafe (FUS)—A FUS condition of Zero, indicates that a write alarm condition occurred, or that the spindle speed is out of tolerance. The following specifies the actual conditions.

1. When FUS equals zero and;

WGT = 0—Indicates that the write current is not on, there is no write current inversion 3 μsec after WGT becomes active or when,

WGT = 1—Indicates that the write drive current is activated.

2. An FUS value of zero only, indicates the spindle spped exceed its rated tolerance of +1.5%.

The FUS signal is reset to a logic "1" when the Drive Select (DS) signal is set at a logic "1".

g. Head Select 0 through 2 (HS0 through HS2)—The head select logic selects one of eight heads as shown below.

HEAD ADDRESS	HEAD SELECT CODE 0	1	2
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

h. Index (IDX) Mark signal—A negative change (logic "1" to logic "0") of the IDX mark indicates the starting point on a track.

i. Ready (RDY) signal—With the RDY and SKC signals at a logic "0" signifies that the disk drive assembly is ready to perform a read, write, or seek operation.

   The disk assembly is also ready for a disk operation after the recalibrate procedure, following a power on sequence, is completed.

j. Read Clock (RCK) signal—The RCK signal is sent to the FMT controller as RZ encoded (clocked) data (see Section 3.1, item 2).

k. Read Data (RDT) signal—The RDT signal is used with the VFO option to denote the transmission of RZ data to the FMT controller.

l. Read Gate (RGT) signal—The RGT signal enables data to be read. This signal must be zero in the data access to read data in VFO operation.

m. Seek Complete (SKC) signal—The SKC signal indicates the completion of a seek operation when zero. The SKC signal changes to zero 400 ns after the Step (STP) signal goes to zero.

n. Step (STP) signal—The STP signal moves the read/write head assembly in the direction specified in the Direction Select (DSL) signal. A STP signal change from logic zero to logic one moves the head one cylinder position. The DSL signal must be stabilized at least 40 ns before the STP signal changes. The step operation can be performed in the normal or buffered mode. The minimum STP signal interval and pulse width are 400 ns each.

o. Track 00 (T00) signal—The T00 signal, when at zero, indicates that the read/write head is at track zero (out-most data track).

p. Write Data (WDT) signal—The WDT signal implements a write operation to write data on the disk. The WDT signal must be zero when WGT is high (logic "1").

q. Write Gate (WGT) signal—When WGT signal is a low level (logic "0") data is written on the disk. If RDY or DKC signals are at a high level (logic "1") a write operation is inhibited.

3.7 DATA RECORD FORMAT

The following is a recommended example of a data record on the disk.

1	2	3	4	5	6	7	8	9	10	11	12	13
12 bytes	AM	CYL	HD	SEC	CRC	3 bytes	12 bytes	AM	256 bytes	ECC	3 bytes	14 bytes
00	A1FE					00	00	A1FE	Data		00	4E

1. 12 bytes —VFO SYNC area
2. (ALFE) —ID address mark (including missing bits)
3. —Cylinder address
4. —Head address
5. —Sector address
6. 2 byte CRC —$G(X) = X^{16} - 1$
7. 3 bytes, (00) —WRT switching gap
8. 12 bytes, (00) —VFO SYNC area
9. (A1F8) —Data address mark (including missing bits)
10. 256 data bytes —Data area
11. 4 bytes ECC —$G(X) = (X^{21} + 1)(X^{11} + X^2 + 1)$
12. 3 bytes, (00) —WRT switching gap
13. 14 bytes, (4E) —Sector separating gap

One sector is made up of items c through e, g through i, and l through q in Section 3.6 above.

- Index gap = 16 bytes, (4E)
- Rotational deviation gap = 179 bytes, (4E)—typical value.

3.8 PCB REMOVAL/REPLACEMENT AND ELECTRICAL ADJUSTMENTS

This section portrays, in picture form, the PCB removal/replacement techniques for the G9QKR (VFO) and G9QKQ/G9NXT (logic) PCBs. Included is the appropriate electrical adjustments for each PCB.

3.8.1 PCB Removal/Replacement

Figure 3-6 illustrates the recommended disassembly/assembly steps to remove or replace the VFO and/or logic PCB; either independently, or as a package. It assumes that ac power is disconnected, and that the disk drive assembly is removed from the DKU.

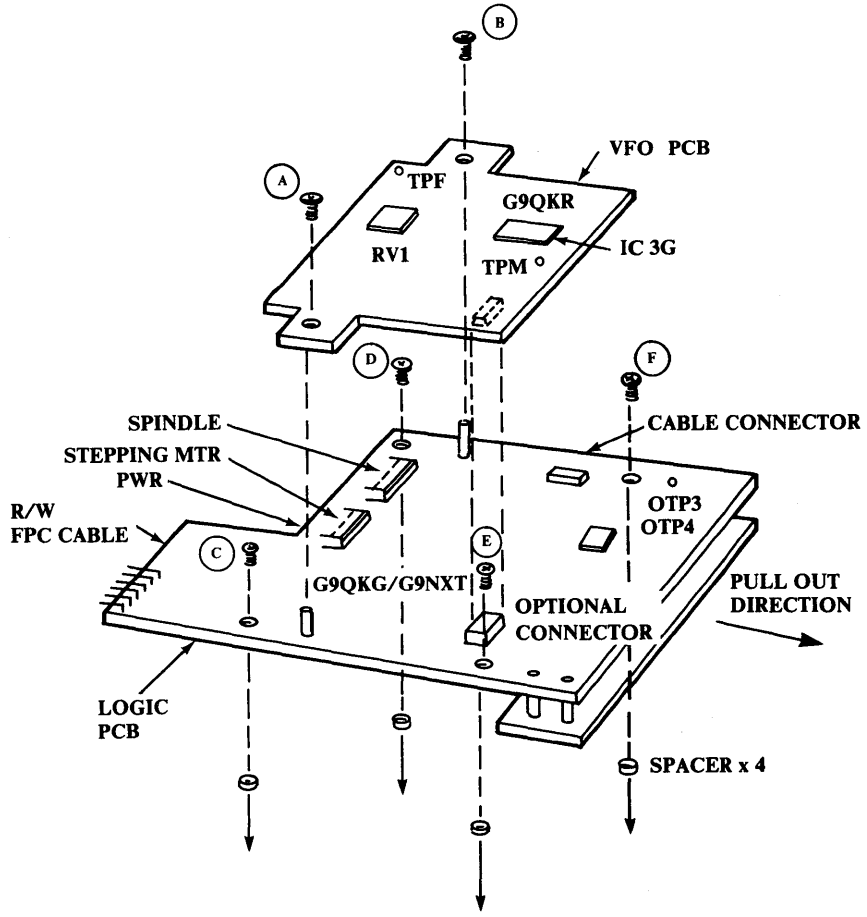


Figure 3-6 PCB Diassembly/Assembly (Disk Drive)

3.8.2 Electrical Adjustments

This section is in two parts; 1. G9QKQ/G9NXT logic PCB balance (speed) adjustment, and 2. Optional VFO PCB adjustment. Part 1 sets the spindle motor speed and part 2 balances the VFO control signal with the logic PCB.

NOTE

When the VFO and logic PCB are received and installed as a matched set, the VFO adjustments are not required. Only the logic PCB adjustment is required.

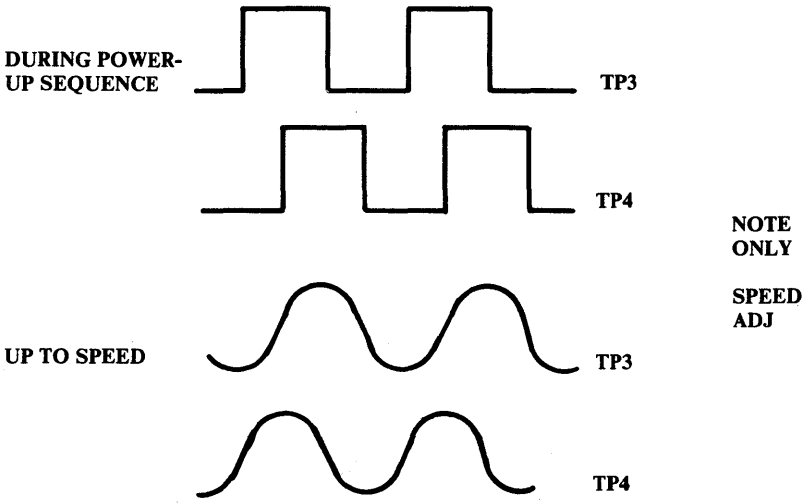
These adjustments assume that the disk assembly is installed in the DKU.

A dual channel oscilloscope, with a 10 MHz band-width, is recommended.

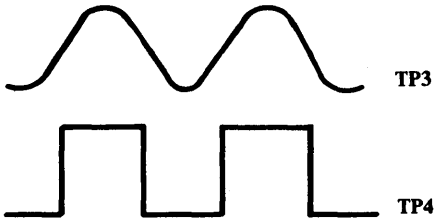
1. G9QKQ/G9NXT PCB Balance (speed) adjustment (see Figure 3-6).
   a. Attach oscilloscope as follows.

      Channel 1 to TP3
      Channel 2 to TP4

   b. Turn on the ac power and verify the phase differential shown below as the disk drive assembly comes up to, and attains its designed speed.



c. With the disk drive at a constant speed adjust RV1 until both waveforms are in phase as shown below. This adjustment sets the spindle motor at its designed speed.



2. G9QKR VFO PCB Adjustment (see Figure 3-6).

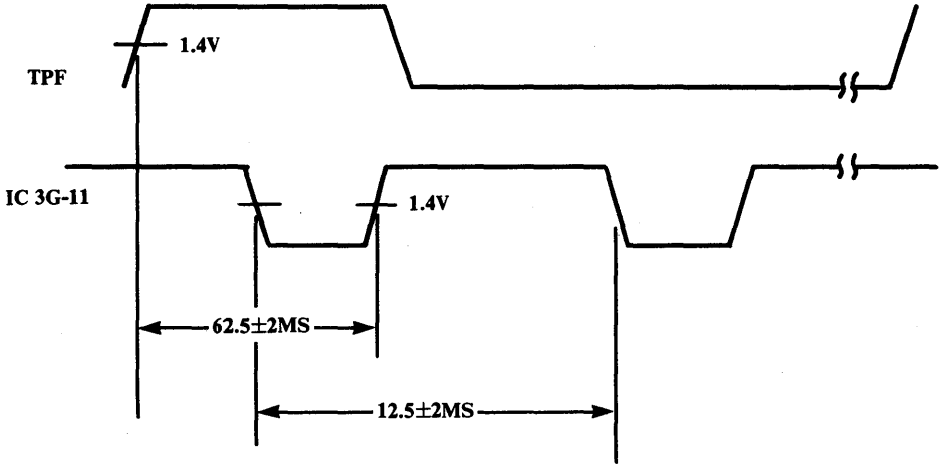
NOTE

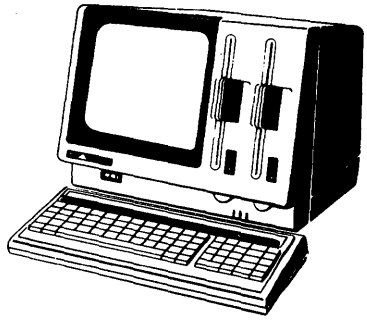
Make sure the disk drive is not being addressed.

a. Attach oscilloscope as follows.

Channel 1 to TPF
Channel 2 to IC 3G pin 11 (or TPH).

b. Adjust RV1 to produce the following waveforms.





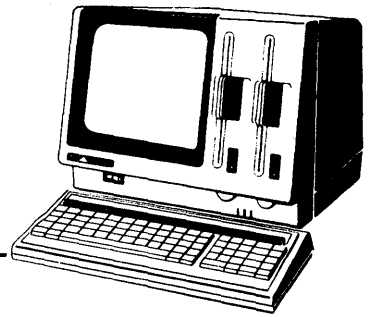
Appendix A

List of Abbreviations

ADR	Address
ADRH	Error Address High Byte
ADRL	Error Address Low Byte
A0	Address Bit 0
CB	Controller Busy
CE	Command End
CEH	Command End High Bit
CEL	Command End Low Bit
CH	Channel
CLCE	Clear Command End
CLDB	Clear Data Buffer
CMD	Command
CRC	Cyclic Redundancy Character
CS	Chip Select
CYL	Cylinder
DACK	DMA Acknowledge
DB	Data Bus
DCK	Diagnostic Clock
DER	Data Error
DIAG	Diagnostic
DMAC	Direct Memory Access Cont.
DMIN	DMA Interrupt
DPAT	Data Pattern
DRO	Data Request
DRQ	DMA Request
DS1 to DS4	Drive Select 1 to 4
DSKC	Disk Controller
DSL	Direction Select
DT or DTP	Device Type
DTLH	Data Length (High Byte)
DTLL	Data Length (Low Byte)

ECC	Error Correct Logic
ENC	End of Cylinder
EOP	End of Process
EPAT 1 through 3	Error Pattern 1 through 3
EQC	Equipment Check
ESN	End Sector Number
EST	End Status/Error Status Byte
ETN	End Track Number
FUS	File Unsafe
FM	Frequency Modulation
FMT	Format
GPL 1 through 3	Gap Length 1 through 3
HDC	Hard Disk Controller
HDER	Hard Disk (I/O Timing) Error
HDEX	Hard Disk Executing
HSL	Head Select
HSRQ	Status Request
IDX	Index Mark
IER	ID Error
I/O	Input/Output
IOER	I/O Error denoting simultaneous HDER and MAER Mask
IST	Interrupt Status
LCNH	Logical Cylinder Number (High Byte)
LCNL	Logical Cylinder Number (Low Byte)
LHN	Logical Head Number
LSN	Logical Sector Number
MA	Missing Address Mark
MAER	DMA Error
MDA	Missing A.M. in data field
MDM	Missing Data
MFM	Modified Frequency Modulation
MTFB	Mean Time Between Failures
NCN	Present Cylinder Number (NCN should read PCN).
ND	No Data
NR (NRY)	Not Ready
OCN	Object Cylinder Number
OVR	Overrun
PCB	Printed Circuit Board
PCNH	Physical Cylinder Number High
PCNL	Physical Cylinder Number Low
PHN	Physical Head Number

PLA	Programmable Logic Array
PLO	Phase Lock Oscillator
POH	Power on Hours
RC	Ready Change
RCK	Read Clock
RDT	Read Data
RDY	Ready
RGT	Read Gate
RSTR	Reset Status Register
SCMD	Seek command
SCNT	Sector Count(er)
SEN	Seek End
SER	Seek Error
SEQ	Sequence
SK or SKC	Seek Command
SEQ	Sense Interrupt Status Request
STN	Status Number
STP	Step
STR	Status Register
ST0/ST1	Status 0/Status 1
TC	Terminal Count
T0 or T00	Track 00
UA	Unit Address
UST	Unit Status
VFO	Variable Frequency Osc.
WDT	Write Data
WF	Write Fault
WGT	Write Gate



Appendix B

FMT Interface Signal Definitions

A0	Register select input. When high, the command/status register is selected. When low, the data buffer is selected.
CS	Chip Select. When low, enables reading from or writing into the register selected by A0.
DB	Data Bus. Data bus bits 0 through 7
DRQ	DMA Request. Normally low, set high to request a transfer of data between the disk controller and memory.
IOR	Write Strobe. When low, data is written into the selected register.
IOW	Read Strobe. When low, contents of selected register are read.
HINT	Interrupt request to the system, set high to make request.
RESET	Reset input. When high, sets the idle state in the DKU. The DKU remains in this state until a command is received.
TC	Terminal Count. Terminal counter input during DMA.

Note: See Section 2.1.2.3 and Figure 2-4 for additional information.

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USER'S COMMENTS FORM

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