PHILCO

TECHNICAL MANUAL
TRANSAC S-2000
INPUT-OUTPUT PROCESSOR

PHILCO CORPORATION
Government and Industrial Division
PHILADELPHIA 44, PENNA.

SERIAL NO. 120

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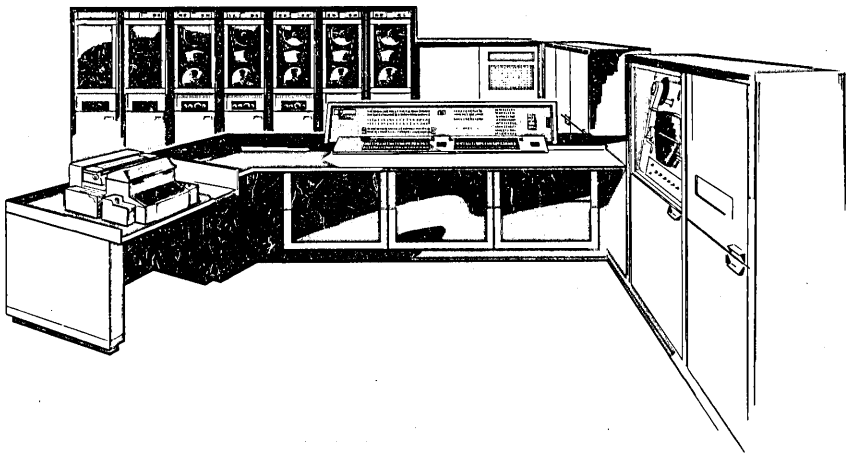

PRELIMINARY EDITION

PHILCO CORPORATION
GOVERNMENT AND INDUSTRIAL DIVISION
4700 WISSAHICKON AVENUE
PHILADELPHIA 44, PENNSYLVANIA

PREFACE

The purpose of this manual is to provide a detailed technical description of the S-2000 Input Output Processor to meet the requirements of TRANSAC Customer Engineering and other groups.

This description is based upon the Serial No. 31 IOP as of August 1959. It is not to be considered as the authoritative document in final details. The working schematics should be the reference documents consulted for any specific system.

For simplicity of presentation, functional logic drawings are employed as references for most of the description. The effect sought in these drawings is consiseness of representation. To achieve this, a direct translation from the schematic logic drawings is not always used. For example, a gate as shown on the functional drawings may not exist, per se, on the schematic logic.

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1. INTRODUCTION

The IOP Function

The IOP is used as a connecting unit between the computer memory and three types of devices to coordinate the transfer of data between memory and input-output:

1) Magnetic Tape Transports

2) Universal Buffer-Controllers

3) High-Speed Printers, Model 257

In this manual, only operations pertaining to the Magnetic Tape Transports will be considered.

Magnetic Tape Application

Magnetic Tape has several characteristics which make it an important input-output medium:

1) Relatively low cost for large amounts of stored information.

2) Compact permanent storage.

3) Convenient for off-line processing.

2. DATA REPRESENTATION ON TAPE

Physical Characteristics of Magnetic Tape

The tape used in the TRANSAC system is a one inch wide Mylar base type which comes on reels containing up to 3600 ft. Tape moves on a transport at a rate of 120 in./sec. in either direction while processing and at 180 in./sec. while rewinding.

There are 16 read heads and 16 write heads in a transport which can process 90,000 char./sec. (This transfer rate applies as long as information is passing under the heads. Since, as will be seen, almost half the tape does not contain information, an average transfer rate of about 45,000 char./sec. can be expected.)

Up to 4 transports may be processing data simultaneously, under which condition an average data transfer rate of 4 x 45,000 (or 180,000) characters per second may be achieved.

The write heads are spaced .39 in. in front of the read heads (as seen by forward moving tape) thus permitting readback of written information (for checking purposes) concurrent with writing.

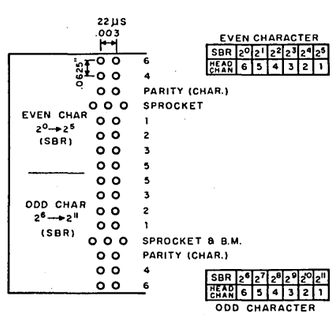
NRZ Recording Method

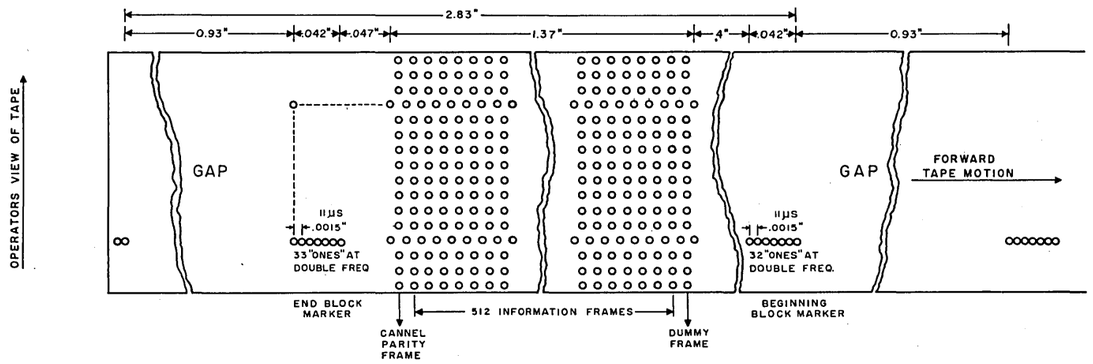
Binary digits (ones or zeros) can be written on tape by each of the 16 write heads in longitudinal channels. The Non-Return to Zero (NRZ) method of writing is used (See Figure 2-1).

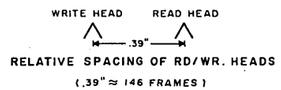
In the NRZ method each binary 1 is represented by a single flux change (either + to - or - to +). Zeros are indicated in this method as simply the lack of a flux change. The mechanics of reading and writing with the NRZ method will be elaborated in later sections.

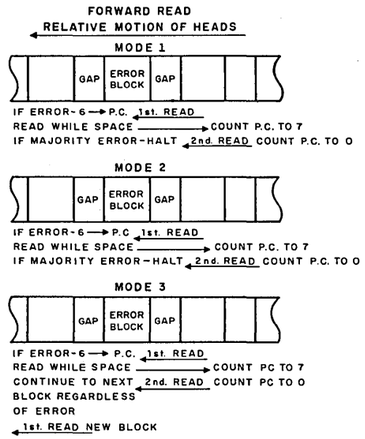
Information Format

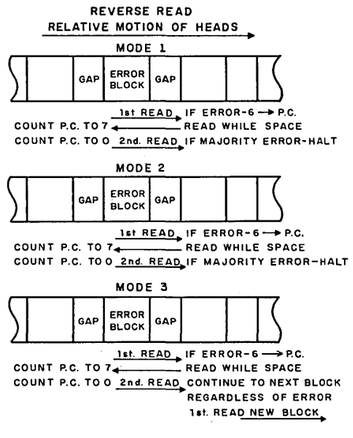
The basic unit of information (coded as binary digits) represented on tape is an alphanumeric character (by a group of 6 bits). Associated with each character on tape is a "parity bit". The parity bit is given a value (0 or 1) so that the total number of ones in the seven bit group is odd. This is termed, "odd parity".

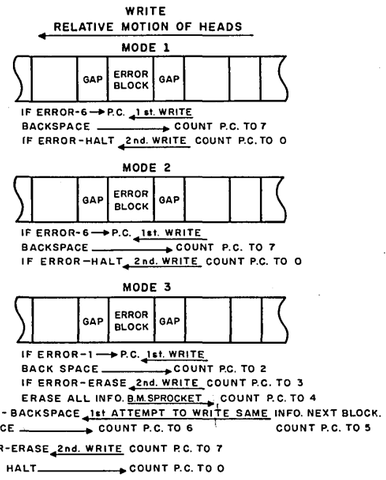


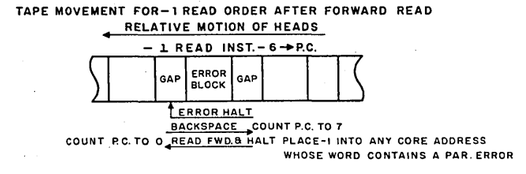


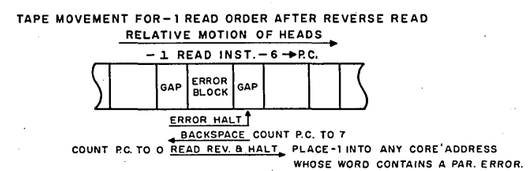


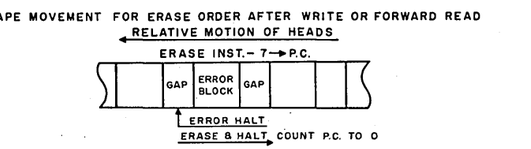


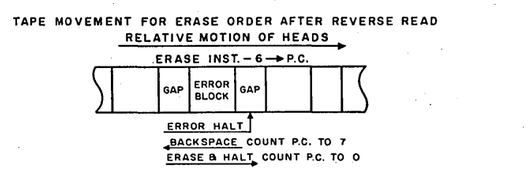












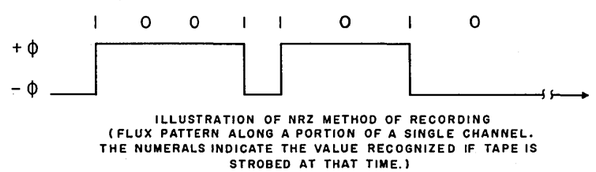


ILLUSTRATION OF NRZ METHOD OF RECORDING
(FLUX PATTERN ALONG A PORTION OF A SINGLE CHANNEL.
THE NUMERALS INDICATE THE VALUE RECOGNIZED IF TAPE IS
STROBED AT THAT TIME.)

NOTES:
1) "MAJORITY ERROR" MEANS ERROR IS SENSED DURING 2 OF 3 PASSES OVER BLOCK

Figure 2-1 Magnetic Tape Format and Movements

Two characters, with parity bits, can be written across the tape as shown in Figure 2-1. Such a set of two characters is called a "frame". A group of frames, together with certain control information, form a "block".

Reference to Figure 2-1 shows a block to consist of the following:

1) A Beginning Block Marker (BBM), for forward tape motion, which consists of 32 binary ones spaced .00133 in. apart in a single channel. (At a tape speed of 120 in./sec., a bit will appear under the heads every 11.1 μs)

2) An End Block Marker (EBM), for forward tape motion, which consists of 33 binary ones with a spacing identical to the BBM and written in the same channel.

3) Sprocket pairs (515), which consist of binary ones, are written in the channels indicated. The pairs are spaced .00266 in. apart. Note that one set of sprockets appears in the same channel as the BBM and EBM. The first sprocket pair is located about 0.4 in. from the BBM and the last pair is about 0.048 in. from the EBM.

4) A Channel Parity Frame, located between the 514th and 515th sprocket pairs, which contains bits as follows:

   In each channel(except those containing sprockets), the Channel Parity Frame contains a 1 if this will make the total number of ones in the channel (for this block) even. In all other channels, the Channel Parity Frame contains a 0.

5) A Dummy Frame, located between the 1st and 2nd sprocket pairs, the two characters of which are zeros (i.e. 000000). The parity bits associated with these characters are, of course, ones.

6) Information Frames (512) interlaced between the 2nd through 514th sprocket pairs.

7) A single "1" in the non-block mark sprocket channel corresponding to the 33rd bit of the EBM. Thus, flux in both sprocket channels in a gap is always the same, say negative.

A block is the smallest quantity of information which can be processed by a single instruction (although less than a full block may be read if a combination of instructions is used). The usable information in the block (i.e. - the 512 information frames) amounts to 128 TRANSAC words.

Division of the tape into blocks facilitates changing (i.e. - rewriting) relatively small amounts of information without disturbing the entire tape. That a division such as this is necessary results from using the NRZ method of recording. Refer to the flux pattern on Figure 2-1. which illustrates the problem. Attempting to change the value of any of the bit positions results in modification of other bits in the channel. Hence, to change any bit in a channel, the entire channel must be rewritten. In fact, due to practical considerations, all channels in a block are always rewritten during a write-type instruction. However, the channel containing the BBM, EBM, and one set of sprockets is not rewritten in the BBM region.

The BBM and EBM define the area within which the information content of the block will be found. Before any processing of a tape can be done, the entire reel must be laid off into blocks by a process called Editing. This process places BBM's and EBM's on tape at the required intervals. EBM's are rewritten after the information frames during each write instruction, but the BBM can only be rewritten by the editing operation.

Because IOP editing does not lay down sprockets, an edited EBM consists of 32 "ones" and no restoring bit is written in the non-block mark sprocket channel. Thus, gap flux after editing is the same as after a write operation.

The sprockets serve as indicators which inform the IOP that a character has passed over the read heads. Note that a sprocket follows each character whether reading takes place in the forward or reverse direction.

3. OPERATIONAL CHARACTERISTICS

IOP Sub-Sections

The IOP may be conveniently subdivided into several sections for the purpose of logical description. Refer to Figure 3-1 for a block diagram of these sections and their relationship to the Central Computer (CC) and the Transports.

The Assembly Unit (AU) contains the following:

(1) Data registers, which temporarily hold data that is moving between CC and tape.

(2) Control registers, which hold information necessary to execute a tape instruction (e.g., the type of instruction, the amount of data to be transferred, etc.). An error indicating register is included in this group. All control registers communicate (indirectly) with CC.

(3) Execution Circuits, which carry out the operations indicated by the Control Registers.

There may be from one to four AUs in each IOP; the number of transports which can operate simultaneously corresponding to the number of AUs present.

The Multiplexer handles the following control functions which are made necessary by simultaneous operation of two or more AUs:

(1) Assignment of a specific AU to perform each order received from CC (except the Rewind orders, which do not require an AU). This includes, in some instances, the establishment of communication paths between the selected AU and the required transport.

(2) Establishing a core memory access for any AU which requires it. When more than one AU requires a memory access, the Multiplexer provides a sequence for satisfying the access requirements.

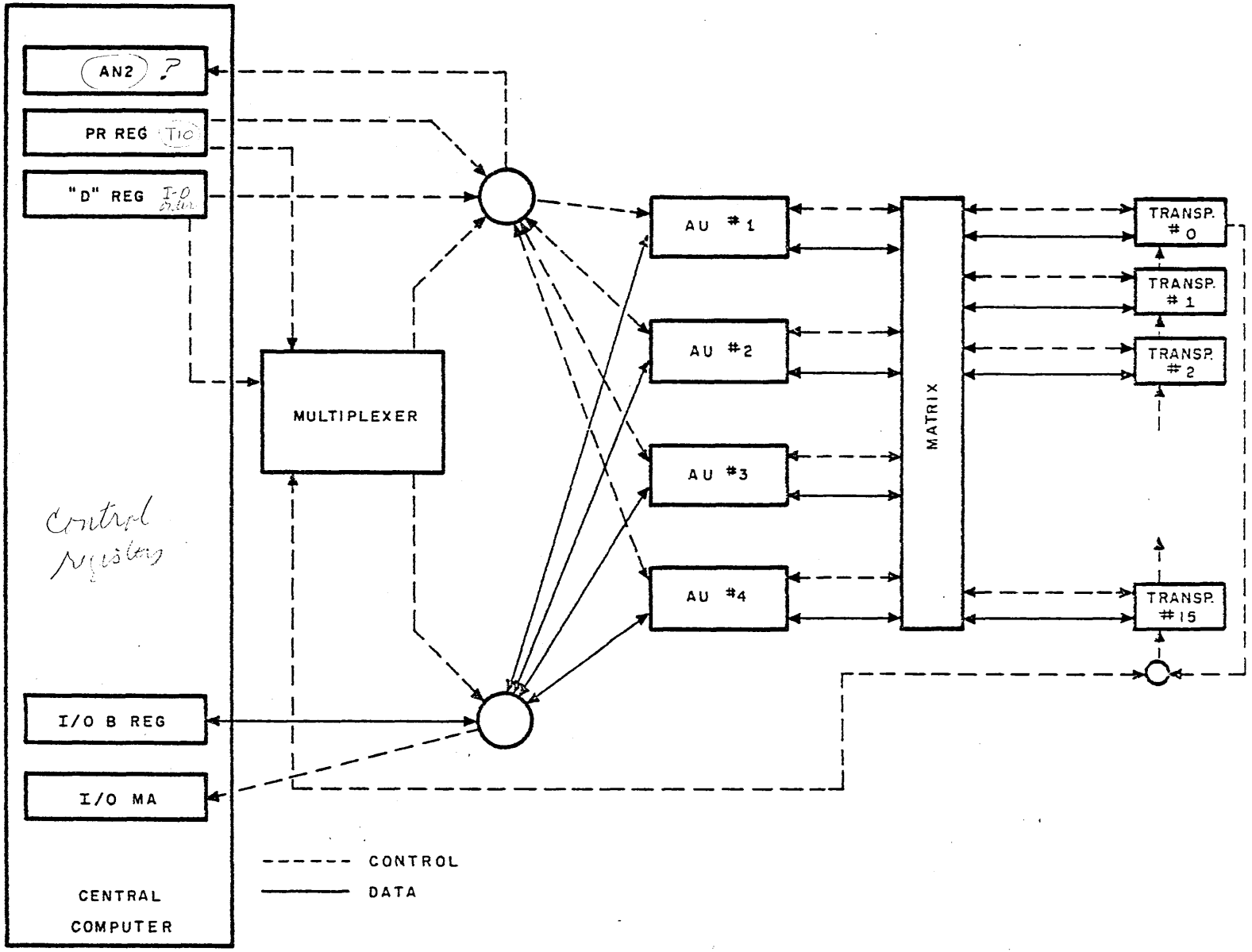


Figure 3-1 IOP System Block Diagram

The Matrix contains the circuits needed to maintain communication between any AU and any transport. Connection of a specific AU to a specific transport (referred to as "marking" the Matrix) is accomplished by the Multiplexer.

Basic Error Detecting Capabilities

The IOP automatically tests for the following conditions:

(1) A character which does not contain an odd number of 1's (including parity bit) or a channel (except a sprocket channel) which does not contain an even number of 1's (including channel parity bit). Either of these conditions indicate the pickup or dropout of information on tape and are termed "Parity Errors" when reading or writing, or "Space Errors" when spacing or positioning a tape.

(2) A block mark (BBM or EBM) which does not contain at least 25 binary ones. This condition is referred to as a "Format Error".

(3) The existence within a block of other than exactly 515 pairs of sprockets, each pair satisfying certain skew timing tolerances. This situation is called a "Sprocket Error" when reading or writing or a "Space Error" when spacing.

(4) A transport which has gone into Local Command status (i.e., can no longer be controlled by the IOP) while connected to an AU via the matrix. This condition is called "Transport Disabled".

(5) An attempt to move tape forward or backward (except by a Rewind order) beyond the ends of the tape. This results in an "End Tape Error" (if forward motion is attempted) or a "Begin Tape Error" (if backward motion is attempted).

All of these error situations will be discussed in detail later. The outline above is to provide the necessary background for understanding the tape orders.

TIO Instruction and IO Orders

The primary means of operating the Magnetic Tape System is through the stored program in Core Memory. Operation is initiated by a TIO instruction being executed in the PR Register. (The Skip instructions are discussed elsewhere.)

Execution of the TIO instruction has two results:

(1) The contents of the "D" Register (the IO Order) are made available to IOP, conveying information as to what type of tape operation is required, what transport is to be used, how far the tape is to be spaced or positioned and how much data is to be processed. See Figure 3-2.

(2) The address part of the TIO instruction is made available to the IOP to provide the first core memory address from which information will be taken when writing, or into which information will be placed when reading.

Note that, as with other input output operations, the "D" register must be loaded with appropriate control information prior to executing the TIO instruction.

For any order which requires writing,editing, or erasing of tape, a "Write Ring" must be present on the selected tape reel. Absence of the ring results in the refusal of the IOP to accept the order.

The amount of data to be processed is specified as "Number of Blocks"; each block containing 128 TRANSAC words. Words are always transferred from, or placed in, core memory in sequential addresses starting with the address specified by the TIO instruction. When more than one block is processed, the sequence of memory addresses is maintained from block to block.

The Number of Blocks field is also referred to as the NBP field (for Number of Blocks to Process).

The transport address to be used is specified by the "Which Tape" field of the "D" register; also called the Transport Address (TA) field. Since this field contains four bit positions, any one of sixteen transport addresses (numbered 0 through 15) may be specified; which

D REGISTER

STARTING ADDRESS (0-15)	BAND NO. (16-17)	DRUM STARTING ADDRESS (18-27)	UNIT ADDRESS (28-39)	BUFFER CHANNEL (40-47)	AMOUNT OF INFORMATION TO BE TRANSMITTED (48-59)	WORDS PER CARD (60-63)	COMMAND FROM (64-67)	COMMAND TO (68-71)	
			WHICH DEVICE				0000	0001	REAL TIME DEVICE → CORE
	BAND NO.	DRUM STARTING ADDRESS	WHICH DRUM		NO. OF WORDS		0001	0010	CORE → DRUM
	BAND NO.	DRUM STARTING ADDRESS	WHICH DRUM		NO. OF WORDS		0010	0001	DRUM → CORE
					NO. OF WORDS		0001	0100	CORE → PAPERTAPE PUNCH [1]
					NO. OF WORDS		0100	0001	PAPER TAPE READER → CORE [1]
					NO. OF WORDS		0001	0110	CORE → HIGH SPEED PRINTER [1]
			WHICH BUFFER	WHICH I/O	NO. OF CARDS [3]	WORDS PER CARD [3]	0001	0111	CORE → I/O DEVICE [2]
			WHICH BUFFER	WHICH I/O	NO. OF CARDS [3]	WORDS PER CARD [3]	0111	0011	I/O DEVICE → BUFFER [2]
			WHICH BUFFER				0011	0001	BUFFER → CORE
		NO. OF BLOCKS TO BE SPACED	WHICH TAPE		NO. OF BLOCKS		0001	1001	CORE → MAG. TAPE — MODE 1 — FOWARD
		NO. OF BLOCKS TO BE SPACED	WHICH TAPE		NO. OF BLOCKS		1001	0001	MAG. TAPE → CORE — MODE 1 — FOWARD
		NO. OF BLOCKS TO BE SPACED	WHICH TAPE		NO. OF BLOCKS		0001	1010	CORE → MAG. TAPE — MODE 2 — FOWARD
		NO. OF BLOCKS TO BE SPACED	WHICH TAPE		NO. OF BLOCKS		1010	0001	MAG. TAPE → CORE — MODE 2 — FOWARD
		NO. OF BLOCKS TO BE SPACED	WHICH TAPE		NO. OF BLOCKS		0001	1011	CORE → MAG. TAPE — MODE 3 — FOWARD
		NO. OF BLOCKS TO BE SPACED	WHICH TAPE		NO. OF BLOCKS		1011	0001	MAG. TAPE → CORE — MODE 3 — FOWARD
		NO. OF BLOCKS TO BE SPACED	WHICH TAPE		NO. OF BLOCKS		1101	0001	MAG. TAPE → CORE — MODE 1 — REVERSE
		NO. OF BLOCKS TO BE SPACED	WHICH TAPE		NO. OF BLOCKS		1110	0001	MAG. TAPE → CORE — MODE 2 — REVERSE
		NO. OF BLOCKS TO BE SPACED	WHICH TAPE		NO. OF BLOCKS		1111	0001	MAG. TAPE → CORE — MODE 3 — REVERSE
			WHICH TAPE				1000	1000	CONTINUE — MAG. TAPE
			WHICH TAPE				1111	1000	STOP — MAG. TAPE
			WHICH TAPE				1000	1001	RESUME — MAG. TAPE
			WHICH TAPE				1000	1010	REWIND — MAG. TAPE
			WHICH TAPE				1000	1011	REWIND W/LOCKOUT — MAG. TAPE
			WHICH TAPE				1100	1100	RELEASE — MAG. TAPE
			WHICH TAPE				1100	1101	−1 READ — MAG. TAPE
			WHICH TAPE				1100	1110	ERASE — MAG. TAPE
			WHICH TAPE				1100	1111	EDIT — MAG. TAPE

FUNDAMENTAL CODES

0000 REAL TIME DEVICES	0100 PAPER TAPE [1]
0001 MAGNETIC CORE	0101
0010 MAGNETIC DRUM	0110 HIGH SPEED PRINTER [1]
0011 BUFFER - CONTROLLER	0111 I/O DEVICE [2]

1000 THRU 1111 INCLUSIVE ARE USED FOR MAG. TAPE

NOTES

1 - CODES 0100 AND 0110 ARE USED IN INSTALLATIONS WHERE THESE DEVICES DO NOT OPERATE THROUGH A BUFFER - CONTROLLER.

2 - CODE 0111 IS USED FOR ANY DEVICE OPERATING THROUGH A BUFFER - CONTROLLER.

3 - THESE BITS ARE USED ONLY WHEN THE I/O DEVICE SPECIFIED IS A PUNCHED CARD SYSTEM

4 - UNUSED FIELDS ARE INDICATED BY A LINE IN PLACE OF A LEGEND.

Figure 3-2 Input-Output Orders

transport is selected by a given address is determined by the transport address plugs. Up to four transports may be operated simultaneously and independently. As previously mentioned, the number of transports which may operate simultaneously corresponds to the number of AUs present in the IOP. For ease of future discussion, transport 0 will be considered as being assigned address 0, transport 1 address 1 etc., unless otherwise stated.

The four bit field "Number of Blocks to be Spaced" (NBS), specifieds the number of blocks on tape which are by-passed before processing (as indicated by the Number of Blocks field) begins.

The Command field indicates which of the eighteen possible tape orders, is to be performed. Before giving a detailed description of each instruction, several terms must be defined:

(1) Busy - an AU is busy if it is connected (via the matrix) to a transport. This matrix connection is established (or "marked") at the beginning of most instructions.

(2) Release - to break the matrix connection between a transport and an AU (i.e., make the AU non-busy). Releasing occurs in various ways which will be discussed with the individual instructions.

(3) Run - an AU is in run status if tape is moving, or is in the process of starting or stopping, under control of the AU. For practical purposes, an AU which is in run status is also busy, although the converse is not necessarily true.

(4) Transport Address in AU - Stored in each AU is the address of the last transport which was connected to, or the transport which is currently connected to, the AU. This address helps to determine which AU (if any) should be used for each instruction.

(5) Class A orders - A group of orders consisting of:

Write (any mode)

Read Forward (any mode)

Read Backward (any mode)

Edit

To accept an order in this group, an AU must be in non-busy status.

(6) Class B Orders - A group of orders consisting of: Stop, Release, and Continue.

To accept an order in this group, an AU must contain the transport address specified by the order.

(7) Class C Orders - A group of orders consisting of: -1 Read, Erase, and Resume.

To accept an order in this group, an AU must contain the transport address specified by the order and also be in non-run status.

(8) Backspace - to move tape without accessing memory, in a direction opposite to that specified by the last (or current) Class A order. Thus, if backspacing occurs during a Read Forward, Mode 1 order, tape will move backward; but backspacing during a Read Backward, Mode 1 order causes tape to move forward.

For any order to be executed, the required transport must exist (as indicated by the presence of an Assigned (Address), and the transport must not be rewinding or in Local Command status. Furthermore, for execution of orders which require writing, erasing, or editing of tape, a "Write Ring" must be present on the selected tape reel. Failure to meet any of these conditions results in the TIO instruction terminating without skipping.

Magnetic Tape Orders

Read Forward, Mode 1 (Command field coding 10010001).

This order, when successfully executed, results in data being transferred to Core Memory from tape while the tape is moving forward. The quantity of information transferred is specified by the NBP field of the "D" Register, and the first Core Memory address is specified by the address part of the TIO instruction.

The Transport from which data is read is indicated by the TA field. Spacing, (i.e., by-passing) of blocks prior to reading occurs as specified by the NBS field. (If both the NBP and NBS fields are 0, 16 blocks are read).

For this order to be executed, selection of an AU must be made in one of the following ways:

(1) If the transport address in any AU is the address in the TA field of the "D" Register and that AU is non-busy, it will be selected to execute the order. Should the AU be busy, the order cannot be executed.

(2) If the transport address specified by the TA field is not contained in any AU, the highest numbered, non-busy AU will execute the order. Should all AU's be busy, the order cannot be executed, and the "Multiplexer Busy" indicator light will be lit on the operator panel.

The number in the TA field of the "D" Register is placed in the selected AU if the order can be executed.

Upon selection of an AU, the matrix is marked, and the AU is thus in busy status. Successful completion of the order (i.e., termination of the order, not due to an error) results in the AU being released.

If a Format Error occurs during a spaced block, the space portion of the order will be finished and the tape will stop with NBS = 0, NBP = initial value, the Format Error Indicator "ON" and the matrix connected to the AU. A Format Error detected during reading will cause the tape to stop at the end of that block (or at the end of recycling over that block caused by parity or sprocket errors). The matrix will remain connected, the Format Error will be "ON" and NBP will indicate the number of blocks that were not processed by the order.

Occurrence of an End Tape Error results in termination of the order. Because no block marks exist in the vicinity of the end of tape, the tape will stop in a gap with NBS and/or NBP non-zero and the matrix connected. The End Tape Error Indicator is cleared by the first sense of a BBM on a subsequent operation which reverses tape motion. Termination of the order also results if the Transport Disabled condition is recognized. This leaves the matrix connected. However, this catastrophic condition results in head positions which are unknown with respect to gap or block and rewinding is necessary.

If a parity or sprocket error occurs while spacing, the Space Error indicator is turned on, but the order is not terminated.

If a parity or sprocket error occurs while processing, the tape stops at the end of the error block and back-spaces over the block. While back-spacing, a check is made for recurrence of the error but no memory accessing exists. Should the error recur, the tape is read forward over the block into the original memory locations and the order is terminated. If the error does not recur during back-spacing, the block is also reread into the original core memory locations. A recurrence of the error during this second read results in terminating the order at the end of the block. Should the reread prove error-free, the order continues as though no error occurred.

When a sprocket or parity error terminates the order (or Format Error), an appropriate visual indicator is lit on the IOP Operator's Panel, the matrix remains connected even though the last block of the order may have been involved. The AU Control Registers retain all information necessary to Resume the order, if required (generally if NBP $\neq$ 0).

Because the number of sprocket pairs read from tape determine the number of memory accesses, limiting and correcting circuits (1) prevent more than 128 counts of the core address counter in the event of excess sprockets detected during a block; and (2) provide the additional counts necessary to give a total of 128 if sprocket pairs are missing. Such action is necessary to assure proper "jumping out" of error cycles if sprocket errors do not persist, or proper resuming if they do persist.

Termination of the order, either by completion or due to error, does not, in itself, affect the progress of the program in CC. Only by executing further TIO instructions or Skip type instructions, can the program be made cognizant of the status of the IOP.

The initiation of the order clears the Parity and Sprocket Error indicators. and Space

Read Forward, Mode 2 (Command Field coding 1010 0001)

This order is identical in every respect to the Read Forward, Mode 1, order. Its inclusion as a separate order provides a future method of incorporating "interrupt" and "non-interrrupt" read orders in the IOP.

Read Forward, Mode 3 (Command Field coding 1011 0001)

This order is similar to the Read Forward, Mode 1, order, except when a parity or sprocket error occurs while processing (not spacing) a block. A retry is made to read the error block (just as in the Mode 1 Read), but the order is not terminated if the retry is unsuccessful. Instead processing of the next block continues as though the retry were successful.

The questionable information read from the error block is retained in its proper sequential area of Core Memory (see sprocket limiting and correcting circuits described above). Upon termination of the order, if no error other than parity or sprocket has occurred, the AU is released. There is no visual indication, upon termination of the order, that an uncorrected parity or sprocket error has occurred. Furthermore, subsequent TIO or Skip instructions will not be cognizant of the error having occurred.

Read Reverse, Mode 1 (Command Field coding 1101 0001)

This order is similar to the Read Forward, Mode 1 order, except that tape moves in the reverse direction while being read. In consequence, the words read are placed in Core Memory in a sequence opposite to that which occurred while reading forward.

Consider, for example, a block of information, consisting of words W1, W2, W3, ..., W128 (as seen by forward moving tape), which is written on the tape. Reading this block forward with a starting Core Memory address of L, results in W1 being placed in location L, W2 in location (L + 1), etc., until W128 is placed in (L + 127). When this same block is read in the reverse direction, again with a starting Core Memory Address of L, W128 is placed in L, W127 is placed in (L + 1), etc., until W1 is placed in (L + 127).

The arrangement of characters within a word is the same for forward and reverse reading.

Spacing can occur before reading in reverse; the spacing also being in the reverse direction.

To read a given block in the reverse direction, the block must of course, start from a different position relative to the read heads than when reading the same block forward.

It will be noted that the time from the completion of data processing in a block until the end block mark is sensed is larger (3.5 milliseconds) for reverse reading than for forward reading (600 μsec.) because of the effect of head gap spacing on tape format. This fact is of some importance in the programming of continue, skip check and skip fault orders.

Activity, when errors occur, is similar to that which occurs when reading forward in Mode 1. (substitute Begin Tape for End Tape). (Note that back-spacing, when required while reading in the reverse direction, results in tape being moved forward.)

Read Reverse, Mode 2 (Command Field coding 1110 0001)

This order is identical to the Read Reverse, Mode 1, order and is included for future interrupt purposes.

Read Reverse, Mode 3 (Command Field coding 1111 0001)

This order is similar in operation to the Read Forward, Mode 3, order. The arrangement of words in Core Memory is similar to that achieved by the Read Reverse, Mode 1, order.

Write, Mode 1 (Command Field decoding 0001 1001)

This order, when successfully executed, results in information being transferred from Core Memory to tape while the tape moves forward. The amount of information to be written, the transport to be used, and the number of blocks to space before writing are specified, respectively, by the NBP, TA, and NBS fields of the "D" Register. If both the NBP and NBS fields are 0, 16 blocks are written. The first Core Memory address is specified by the address part of the TIO instruction.

Selection of an AU to execute the order is similar to the selection for a Read Forward, Mode 1, order. The number in the TA field of the "D" Register is stored in the selected AU if the order can be executed.

Selection of an AU results in the Matrix being marked, thus putting the AU in busy status. The AU is released when the order is terminated (if this termination was not due to an error).

Termination of the order by Format or End Tape errors, or by sensing the Transport Disabled condition occurs in the same manner, and has the same effect as described for the Read Forward, Mode 1, order.

Concurrent with writing, the written information is read back and checked for parity. (Character parity only; channel parity is not checked while writing.) Detection of a parity error, or sprocket error, during this read-back, results in the tape being back-spaced and the block rewritten. If this second write is executed without error, processing of the next block proceeds as if no error occurred. Should the error recur, however, the order is terminated at the end of the block.

The status of the AU after termination of the order (either successfully or due to an error) is the same as after a similar termination of the Read Forward, Mode 1, order (Except that the Command Register indicates Write instead of Read.)

Determination of position within a write order by means of NBS, NBP and word counter is the same as on a read order. That is, a word is considered to be processed when it is played back by the read heads, not when it is written. Counting down of NBS or NBP occurs on the fourth sprocket pair detected by the read heads at which time the word counter ripples from 0 to 127. Thereafter in the block, the word counter alone counts down once every fourth time a pair of sprockets is received.

WRITE, CHECK, THEN COUNT DOWN.

It should be remembered that, when writing, the sprocket channels and EBM are rewritten in any blocks in which writing of information occurs.

The initiation of the order clears the Parity and Sprocket Error indicators. and Space

Write, Mode 2 (Command Field decoding 0001 1010)

This order is identical to the Write, Mode 1, order and is included for future interrupt purposes.

Write, Mode 3 (Command Field decoding 0001 1011)

This order is similar to the Write, Mode 1, order, except when a parity or sprocket error occurs. In this case an attempt is made to rewrite the block as during a Write, Mode 1, order. If this

rewrite is successful, the order proceeds as in Write, Mode 1. Should a parity or sprocket error occur during the rewrite, the following action takes place:

(1) The tape is back-spaced, during which process the entire block (including sprocket channles and block marks) is erased.

(2) An attempt is made to write (the same information) in the next block on tape; retrying if the first attempt is unsuccessful.

If writing in the new block is successful, the order proceeds as if no error had occurred. However, if writing is not successful, the block is erased and the order is terminated. Note that automatic erasure can only occur following a parity or sprocket error. Other errors may terminate the order without erasing.

If sprocket or parity errors persist in all four attempts to write a block, termination of the order leaves the matrix connected but no sprocket, parity (or format) error lights are lit since the two erasures removed all errors from tape. If a format error terminates the order when either no parity nor sprocket error has existed in the block, or rewriting has cleared up sprocket or parity errors, the tape stops with the matrix connected and the Format Error light lit since the format error still exists on tape.

When erasing and rewriting in a new block is required, the entire operation is counted as only one block processed (for purposes of satisfying the NBP requirement.)

The Class C Orders

The three orders in this group are used, primarily, as corrective steps following the termination of a Class A order due to an error. An order in this group will be accepted by an AU if the transport address in the AU is the same as the address specified by the TA field of the "D" Register and if the AU is in non-run status. All three orders are capable of marking the matrix if for some reason the latter were disconnected prior to the issuance of the order.

The -1 Read Order (Command Field coding 1100 1101)

This order can be used following Read (but not Write) orders which have terminated due to a persistent parity error. Execution of this order results in the last block which was read being reread (in the same direction as the original read), into the same Core Memory locations. However, any word containing a parity error on the reread is not placed in Core Memory. Instead the number "-1" (in twos complement form) is placed in that Core Memory location. A block read in this manner does not count NBP; the core address at the termination of the order is the same as before the order was issued; and the state of the AU command register corresponding to the previous Class A order is preserved. Thus, a -1 Read block is not counted as a block processed if the original order is resumed.

Upon completion of the order, the tape is in the same position, relative to the heads, as it was when the order was given. The Parity Error indicator is reset, but the Matrix remains connected.

In order for reading to take place in the same direction as the Class A read, the tape is automatically back-spaced one block prior to the rereading portion of the order.

The initiation of the order clears the Parity and Sprocket Error indicators.

The Erase Order (Command Field coding 1100 1110)

This order is used to eliminate a block (including the sprockets and block marks) from tape. The block erased is the last block that was processed; i.e., if the last Class A order (or resumed Class A order) called for forward motion, the AU would erase one block backward; if the last command were a reverse order, the tape would be spaced forward one block and then erased one block backward. Successive blocks may be erased by the issuance of successive Erase orders.

The Erase command holds cleared the Format, Sprocket and Parity Error indicators and leaves the matrix connected at the termination of the order. Neither NBP nor the Core Address counter is stepped and the state of the Command register is preserved for Resume purposes.

The Resume Order

This order is used to complete a Class A order which has been terminated due to an error. Usually this order is preceded by either the -1 Read or Erase Order. However, initiation of a Resume always clears the Parity and Sprocket Error indicators. The activity of the Resume Order differs depending on whether the last Class A order was a read or write.

Following a read order, the Resume order simply re-starts the Class A order from the point where it was terminated. From that point, processing is considered as Class A in all respects. Consider, for example, the following case:

A Read Forward, Mode 1, order is given, which specifies that five blocks be processed. The first Core Memory location is L. During the processing of the second block, a parity error occurs which is not eliminated by re-reading. Thus the order terminates. If the Resume order is now given, and no further error terminations occur, Core Memory will contain information as follows:

Locations L through (L + 127) contain the 1st block. Locations (L +128) through (L +255) contain the 2nd block (in error)	Read by the original order
Locations (L +256) through (L +383) contain the 3rd block Locations (L +384) through (L +511) contain the 4th block Locations (L +512) through (L +639) contain the 5th block	Read following the Resume order

It is interesting to note that the above sequence of orders gives the same effect as originally performing a Read Forward, Mode 3 order (when only sprocket and parity errors occur).

If a -1 Read order is given prior to the Resume order, the same Core Memory format results; except that any words in the second block which contained parity errors would be replaced in Memory by -1.

Following a write order, the Resume order initiates rewriting of the information which could not be written by the original order. This attempted rewrite is in the next sequential block to the one which was erroneously written. Of course, if an Erase order is given prior to the Resume, (the usual procedure), the erroneously written block will no longer exist. The following example illustrates this:

A Write, Mode 1 order is given which specifies that 5 blocks be processed. The first Core Memory location is L. Termination of the order occurs following the 2nd block due to a persistent Sprocket Error. If an Erase order is now given, followed by a Resume order, information is on tape as follows:

The 1st block contains locations L through (L + 127) - Written by the original order.

The 2nd block has been erased. - Due to the Erase order.

The 3rd block contains locations (L + 128) through (L + 255)

The 4th block contains locations (L + 256) through (L + 383)

The 5th block contains locations (L + 384) through (L + 511)

The 6th block contains locations (L + 512) through (L + 639)

} Written following the Resume order.

Had the Erase order not been given, the same information would be in blocks 1, 3, 4, 5 and 6. Block 2 would still be present, however, and it would contain the information from (L + 128) through (L + 255) improperly written.

If the Resume order is given (following a Read or "Space Only" Write) and no more processing remains to be done per the original order (NBP = 0), 16 additional blocks will be processed in the manner specified by these previous Class A orders. Core Memory locations will be used which follow sequentially those memory locations actually accessed by the original order. If none were accessed, the starting location will be that given in the original order. In the case of an NBP $\neq$ 0 Write Order terminated with NBP = 0, the Resume will rewrite once the last block of the Write command.

The Release Order (Command Field coding 1100 1100)

This order allows the AU which contains the transport address specified by the TA field of the "D" Register to be released from the Matrix. If no AU contains the required transport address, the order will not be executed. Furthermore, if the Format Error, Begin Tape Error, End Tape Error, or Transport Disabled indicator is set, the order is accepted (as indicated by skipping after the TIO instruction); but releasing of the AU does not occur.

When the Release order is given while a previous order is still being processed, the order in progress is terminated at the end of the current block except as follows:

1) If a retry of the current block is called for (or if a retry is in progress when the Release order is given), this will be completed before terminating the order. Note that in the case of the previous order being a Write, Mode 3, the 3 rewrite attempts and 2 erasures provided for may all be accomplished (if required) before termination.

2) If the Release order is given during the backspace phase of a -1 Read or Erase order, termination will not occur until the order is complete.

3) If the NBS Reg. does not contain 0 at the end of the current block, spacing continues until the condition, NBS = 0, is satisfied..

The Stop Order (Command Field coding 1111 1000)

This order is similar to the Release order with the following exceptions:

The order is not affected by any error indicators being set; and execution of the order results in the Format Error, Begin Tape Error, End Tape Error; and Transport Disabled indicators being reset.

No retrys are allowed by the Stop order. If a retry is in progress when the order is executed, the retry is terminated (at the end of the current block) regardless of its status. Since termination of retrys may occur following backspacing (or erasing in the Write, Mode 3 order), the position of the heads relative to the last processed block (and hence all other blocks) is questionable following Stop orders. (That is, the heads may be either at the beginning or end of the last processed block.)

Termination while backspacing can also occur if a Stop order is executed during performance of the -1 Read or Erase orders.

Like the Release order, the Stop order cannot terminate a previous order until the NBS = 0 condition is satisfied. (A primary function of the Stop order is to terminate memory accesses, within a given time, to allow a real-time input to function. Spacing, which does not require memory accesses, need not be terminated.)

The Edit Order (Command Field coding 1100 1111)

Execution of this order results in BBM'S and EBM'S being written, at the proper intervals, until the end of tape is sensed. The final EBM may be written after sensing the end of tape. Normally the order is initiated with the "quick disconnect" device just on the takeup reel side of the heads.

Only one A. U., AU#2, can execute the Edit order. (Note: A change is anticipated which will put the Edit function in AU1.) So far as the Multiplexer is concerned, however, the Edit order is simply a class A order; and an AU is assigned on that basis. Therefore special precautions must be observed to ensure the use of AU#2.

The simplest method is to place A. U. 's 1, 3, and 4 (if they exist in the particular IOP) in Manual Mode status by operating toggles on the Operator's Panel. (These toggles are discussed in detail later.) This leaves only A. U. #2 available to accept an order from C. C. (the Edit order). Of course A. U. #2 must be non-busy; and the required transport must not be in Local Command, Rewinding, or Read Only status.

If desired, the Edit order may be executed without placing any A. U. 's in Manual Mode status if the following requirements are observed:

1) No A. U., other than A. U. #2 may contain the required transport address.

2) AU's 3 and 4, if they exist, must be busy; or AU 4 must contain the required transport address. (Note: An anticipated change will make the order of preference of AU's 1, 2, 3, 4 instead of 4, 3, 2, 1 when more than one AU can accept an order. This, in addition to having the Edit circuits in AU 1, will make condition (2) unnecessary.

3) A. U. #2 must be non-busy.

While executing the Edit order, no error indicators, except Transport Disabled and End of Tape Error can be set. (The EOT Error indicator is set when the order is complete.) Upon completion of the order the Matrix remains connected. Execution of the Stop or Release orders during the Edit has no effect.

Upon completion of the Edit command, the end of tape region should be cleaned up by issuance of several erase orders followed by a Stop or Release and Rewind. Write orders should then be issued to lay down sprockets over the entire length of tape.

The Continue Order (Command Field coding 1000 1000)

This order, following a Class A order, provides a means of processing more than 16 blocks of information without stopping tape motion. (If two consecutive Class A orders are given, tape must stop between the first and second orders.)

The specific operating characteristics of this order are not available at present.

The Rewind Order (Command Field coding 1000 1010)

This order causes tape to move in the reverse direction (at 180 in/sec) until the metallic begin tape leader is sensed. Unlike the orders considered so far, the Rewind order does not require the use of an A. U. for its execution. Upon issuance of the order, the Multiplexer tests for the following:

1) that an Assigned Address Plug for the required transport is in place.

2) that the required transport is neither in Local Command status nor already rewinding.

3) that the required transport is not presently assigned (i. e., connected, via the Matrix) to an A. U.

If these conditions are met, rewinding of the transport occurs, and the TIO instruction initiates skipping; otherwise, the TIO instruction terminates without skipping.

The transport remains in Rewind status (as sensed by the Multiplexer) for 4 seconds after actual rewinding is complete. This allows for slowing down of the drive motor. During the rewind and the subsequent 4 second delay, the Rewind indicator on the transport is lit.

If a Rewind order is issued to a transport which is already rewound, the order will be accepted (as indicated by skipping after the TIO instruction), but no tape motion occurs.

Since the Rewind order does not require the use of an A. U., it can be executed even though all A. U. 's are busy. Furthermore, any number of transports may be rewinding simultaneously.

The Rewind and Lockout Order (Command Field coding 1000 1011)

This order is similar to the Rewind order except that, upon issuance of the order, the transport is placed in Local Command status.

The Skip Instructions

The two instructions, Skip Check and Skip if no Fault, are used to inform the CC of the status of the IOP and the transports (as well as other Input/Output media). Execution of these instructions does not modify the status of the IOP or transports in any permanent way (i. e., -after the completeion of these instructions, the IOP and transports are in exactly the same state as they would have been had the instruction not been given).

A full description of these instructions is given in the TRANSAC Technical Manual, Central Computer, Section 6.15. In the paragraphs below, the possible tests pertinent to magnetic tape operation, are summarized.

The Skip Check Instruction (SKC)

Use of this instruction allows the following conditions to be tested:

1) Whether a particular AU is busy.

2) Whether a particular AU is either in "run" status or making an error retry.

3) Whether a particular transport is connected to an A.U.

4) Whether a particular transport is mechanically available.

5) Whether a particular transport is rewinding.

6) Whether a particular transport is in "Read Only" status.

7) Whether or not more than a given amount of information (say N words) remains to be processed from, or to, a particular transport to satisfy the last (or current) class A order. If the test is made during an error retry, or while writing the first block of a Resumed Write order (except in the case where no blocks had been written prior to resuming), or while the word count is being changed, and indication is given that more information remains to be processed than specified by N, no matter how large N may be. (Actually N has a maximum value of 15 blocks plus 127 words, or 2047 words.) If no AU, while processing its last (or current) class A order, used (or is using) the transport specified by the Skip Check instruction, an indication is given that less information (or an equal amount) remains to be processed than specified by N, no matter how small N may be.

For purposes of the Skip Check instruction, the least significant bit of the Word Counter is effectively held equal to "1" from BBM time until the channel parity and sprocket error tests have been completed. Thus,

the SKC instruction cannot indicate that all information in a block has been processed until it has been determined that no error retrys will be required. The effective hold to "1" is released before the test for EBM errors is made.

The Skip if No Fault instruction (SKF)

Use of this instruction allows testing for fault indications in the AU which was last connected to (or is currently connected to) the transport specified by the SKF instruction. The fault indications which may be tested are, in order of increasing seriousness: Space, End of Tape, Beginning of Tape, Parity, Format, Sprocket, and Transport Disabled. (Note: Actually, the Format Fault is considered more serious than the Sprocket Fault. An anticipated change will allow the SKF instruction to recognize this.)

A single SKF instruction indicates whether a fault (or combination of faults) more serious than a given fault (or combination of faults) exists. Hence, to determine that a particular fault (or combination of faults) exists, more than one SKF instruction must be used.

If no A. U. contains the required transport address, the effect is the same as if an A. U. containing no fault indications were interrogated.

Operator's Panel Control and Indicators (IOP)

The functions of the various indicators, switches, and plugs located on the IOP Operator's panel (see Figure 3-3) are discussed in this section.

I/O Instruction Address Lights

These lights indicate the order address as specified by the TA field of the "D" Reg. The indication is maintained as long as the "D" Reg is made available to the IOP (i. e., -during all, or part, of IT2 time.)

I/O Unit Lights

These lights, numbered 0 through 15, denote actual physical locations of transports. This number will correspond to the number on each transport.

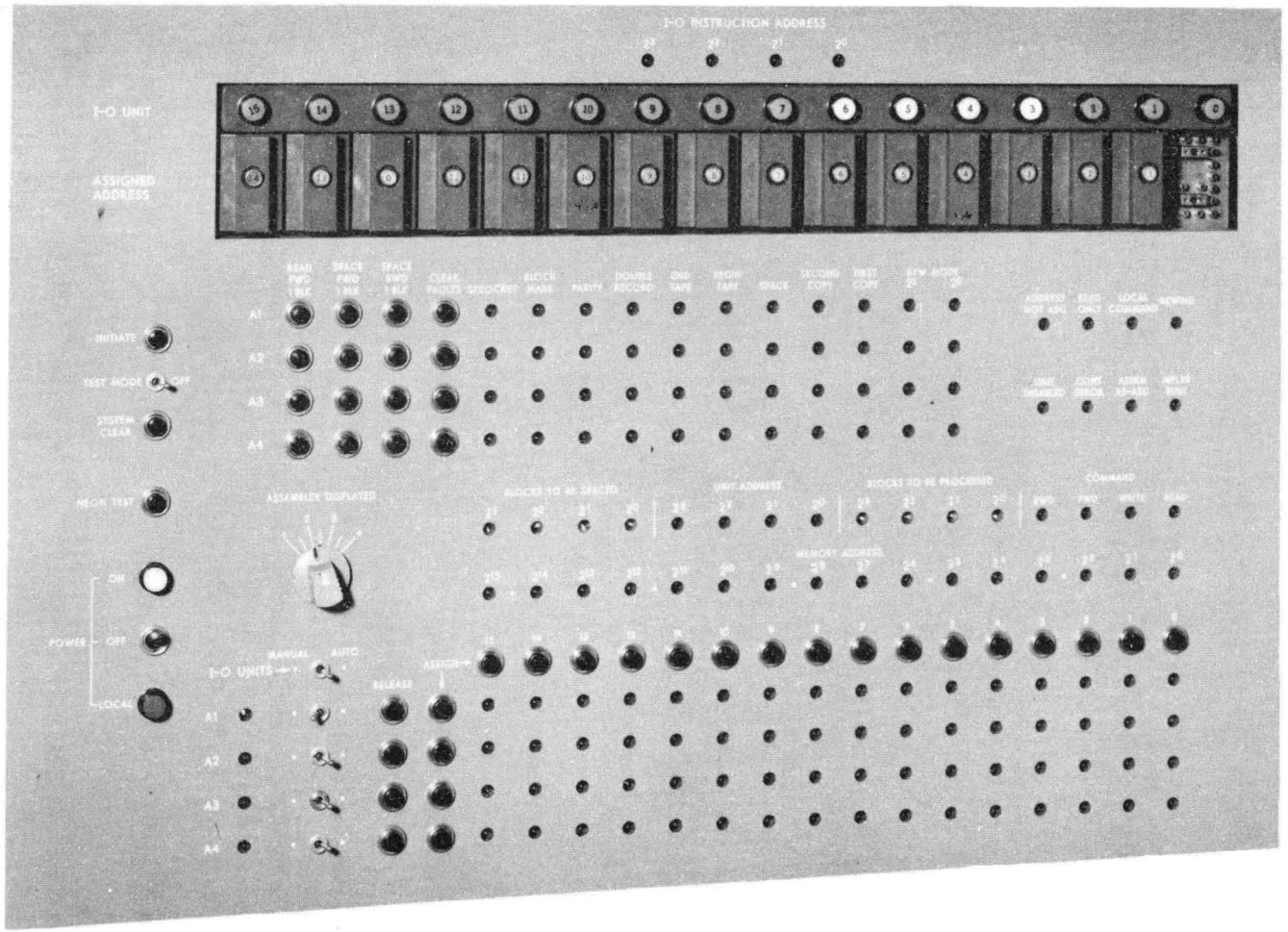


Figure 3-3 Control Panel, Input-Output Processor

Assigned Address Plugs

This section consists of 16 removable Assigned Address Plugs. Each plug is numbered and denotes a unique instruction address. For example, if assigned address plug number 5 were inserted beneath I/O unit number 2, physical transport #2 would now be logically designated and program addressable as unit number 5. The plugs have two positions in the receptacles: an "in" position for assignment (plug light illuminated) and an "out" position for storage.

Read Forward One Block Buttons

For these buttons to be operative, the associated AU must be in Manual Mode. (Refer to the description of the AU Manual-Auto Switches for the method of obtaining Manual Mode Status.) Furthermore, for proper reading, the AU must be connected to a transport via the Matrix. (Refer to the description of the Manual AU Assign buttons for the method of marking the Matrix manually.)

When one of the buttons is depressed (with the above condition satisfied) the associated AU is prepared for reading forward, but actual reading does not begin.

Now, depressing the Initiate button will cause reading of one block, without error retrys, into Core Memory addresses starting with address zero. Further depressions of the Initiate button will cause additional blocks, up to a total of 15, to be read; one block for each depression of the button. When more than one block is read in this manner, the sequence of Core Memory addresses is maintained from block to block.

Upon reading the 15th block, the Matrix is released. If, at any time before the 15th block is read, the Read Forward One Block button is depressed again, the count of 15 blocks begins anew with Core Memory address 0 the first location accessed.

Space Forward One Block Buttons

The operation of these buttons is similar to that of the Read Forward One Block buttons except that spacing occurs rather than reading.

Also , after spacing 15 blocks, further depressions of the Initiate button will cause reading (of up to 15 blocks)

Space Backward One Block Buttons

The operation of these buttons is the same as that of the Space Forward One Block Buttons except that spacing (and possibly reading) takes place in the reverse direction.

Initiate Button

This button is used in conjunction with the Read Forward One Block, Space Forward One Block, and Space Backward One Block buttons. Refer to the descriptions of those buttons.

The output of the Initiate button is available to any AU which is in Manual Mode; hence manual reading or spacing of two or more transports simultaneously is possible.

Clear Faults Buttons

These buttons reset all error conditions, including Transport Disabled, which exist in the associated AU.

Test Mode Switch

This switch has no specified function at present. It will, however, interfere with normal IOP operation if not in the OFF position.

Sprocket Light

These lights (one for each AU) indicate, when lit, that an incorrect number of sprockets has been sensed in the preceding processed block.

Block Mark Light

These lights (one for each AU) indicate, when lit, that an insufficient number of flux changes has been detected in a block mark, either at the beginning or end of the block. If the indicator is lit following spacing, any of the spaced blocks may have been faulty.

Parity Light

These lights (one for each AU) indicate, when lit, that a parity error was detected on tape in the preceding processed block. The error can be either character or channel parity.

End Tape Light

These lights (one for each AU) indicate, when lit, that the transport connected to the assembly unit indicated, has sensed the physical end of tape while tape was moving forward.

Begin Tape Light

These lights (one for each AU) indicate, when lit, that the transport connected to the AU indicated, has sensed the physical beginning of tape while tape was moving backward.

Space Light

These lights (one for each AU) indicate, when lit, that a parity error or sprocket error has been detected while spacing over one or more blocks.

Read/Write Mode Lights

These Lights (one pair for each AU) indicate the Mode of the current order as follows:

Read forward or backward, or write, mode one if 2^0 is on and 2^1 is off. Read forward or backward, or write, mode two if 2^0 is off and 2^1 is on. Read forward or backward, or write, mode three if 2^0 is on and 2^1 is on. Edit, manually space, or manually read if 2^0 is off and 2^1 is off.

Address Not Assigned Light

This light indicates, when lit, that the I/O instruction address (specified by the TA field of the "D" Reg) is not assigned to any I/O unit by an Assigned Address Plug.

Read Only Light

This light indicates, when lit, that an order has been issued to a transport which does not have a write enable ring on the supply reel.

Local Command Light

This light indicates, when lit, that the I/O unit, which has been

addressed, is in Local Command status and cannot accept instructions from a remote source.

Rewind Light

This light indicates, when lit, that the I/O unit which has been addressed is in the process of rewinding and cannot accept an instruction.

Unit Disabled Light

This light indicates, when lit, that at least one I/O has gone into Local Command Status while connected to an AU (commonly due to long or short loops in vacuum columns).

Continue Error Light

This light indicates, when lit, that the conditions necessary to execute the continue order do not exist in the AU which contains the transport address specified by the TA field of the "D" Reg.

Assembly Unit Reassigned Light

This light indicates, when lit, that a command requiring an AU has been issued with address different from that existing in any AU (Class B and C orders cannot be accepted.)

Multiplexer Busy Light

This light indicates, when lit, that all assembly units are busy. A new class A order cannot be executed until one is released. Note that an AU in manual mode is considered busy.

System Clear Button

This button, when depressed, resets all data and logical circuits to starting condition.

Neon Test Button

This button, when depressed, turns on all display neons to determine that they are functioning properly.

Assembler Displayed Switch

This rotary switch will display in the neons to the right, the information contained in assembly units, 1, 2, 3, or 4. For a description of the display, see the next five items.

Blocks to be Spaced Lights

This four bit display will indicate the number of blocks remaining to be spaced by the instruction in the assembly unit specified by the Assembler Displayed Switch.

Unit Address Lights

This four bit display indicates the address contained in the assembly unit specified by the Assembler Displayed switch.

Blocks to be Processed Lights

This four bit display indicates the number of blocks remaining to be read or written by the instruction in the assembly unit specified by the Assembler Displayed switch.

Command Lights

This four bit display indicates which Class A order is being executed (or was last executed) by the assembly unit specified by the Assembler Displayed switch. The mode of the command is indicated elsewhere.

Memory Address Lights

This 15 bit display indicates the next Magnetic Core Memory address which will be accessed by the AU specified by the Assembler Displayed Switch.

Power On Light

This light indicates when lit, that power may be turned OFF or ON from a remote position. It will be ON when the power switch is in the UP position.

Power Switch

This is a three-position switch, which, when in the UP position, will allow power to be controlled by the power switch on the computer console.

When in the center position, all power is removed from the unit.

When in the down position, power is supplied to the I/O Processor regardless of the status of the computer.

Power LOCAL Light

This light indicates, when lit, that power is on locally, and cannot be turned off from the computer console.

I/O Units Manual - Auto Switch

When in the Auto position, this switch allows normal program selection of AU's; when in the Manual position, this selection is inhibited. The Rewind orders and the Skip type instructions are not affected by the position of this switch.

Also, the I/O Unit Assign push buttons are activated when the switch is set to Manual.

AU Manual - Auto Switches

When in the Auto position, these switches allow the associated AU to be selected and used only by orders from CC.

When in the Manual position, the switches cause the associated AU to be placed in the "Manual Mode" of operation provided the AU is in non-run and non-busy status. Manual Mode operation (indicated by the AU Manual light being lit) provides the following effects:

1) The AU appears to be busy when interrogated by the Multiplexer (even though it may not be connected via the Matrix). This prevents the acceptance of Class A orders from CC.

2) The AU effectively contains no transport address. This prevents the acceptance of Class B and C orders from CC. Furthermore, skip type instructions cannot interrogate the A. U. (Note: The Unit Address lights will still indicate a transport address, but this address cannot be recognized by the Multiplexer.)

3) The Release, Manual AU Assign, Space Forward One Block, Space Reverse One Block, and Read Forward One Block push buttons associated with the AU are activated.

4) The output of the Initiate push button is made available to the AU.

Upon removing the AU from Manual Mode (by returning the AU Manual-Auto switch to Auto), all of the effects listed above, except (2), are terminated. The AU continues to effectively contain no transport address until it accepts another class A order from CC. This is necessary to prevent the possibility of two or more AU's indicating that they contain the same transport address.

Note that placing the AU Manual-Auto switch in Manual position while an order from CC is being executed will not affect performance of the order since the AU must be in non-run and non-busy status before Manual Mode can be achieved.

AU Manual Lights

These lights (located to the left of the AU Manual-Auto switches) indicate, when lit, that the associated AU is in Manual Mode. Refer to the description of the AU Manual-Auto switches.

Manual AU Assign Buttons

These push buttons allow manual marking of the Matrix under the following conditions:

1) The I/O Units Manual-Auto switch must be in the Manual position.

2) The AU associated with the particular button must be in Manual Mode (i.e., the AU Manual light must be lit.)

3) The Manual AU Assign push button must be depressed concurrent with one of the I/O Unit Assign push buttons.

When the above conditions are met, the AU associated with the Manual AU Assign button is connected to the transport associated with the I/O Unit Assign button. A light, on a horizontal line from the Manual AU Assign button and a vertical line from the I/O Unit Assign button, will light when the Matrix connection is made. (Note: It is possible to connect more than one transport at a time to an AU by this method. This should be avoided.)

Release Buttons

Depressing one of these buttons releases any Matrix connection that may exist involving the associated AU. The associated AU must be in Manual Mode for the button to be effective.

I/O Unit Assign Buttons

These buttons may be used in conjunction with the Manual AU Assign buttons to manually mark the Matrix. Refer to the description of the Manual AU Assign buttons.

The numbers, 0 through 15, associated with these buttons refer to physical locations of transports rather than logical addresses.

Matrix Connection Lights

This group of 64 lights is located below the I/O Unit Assign buttons.

A light being on indicates that the physical transport associated with the column is connected to the AU associated with the row.

Transport Controls and Indicators

The controls located below the transport door are described in the Ampex FR 300 Manual.

The transport top indicator panel, located above the door, contains several indicators and controls (Figure 3-4).

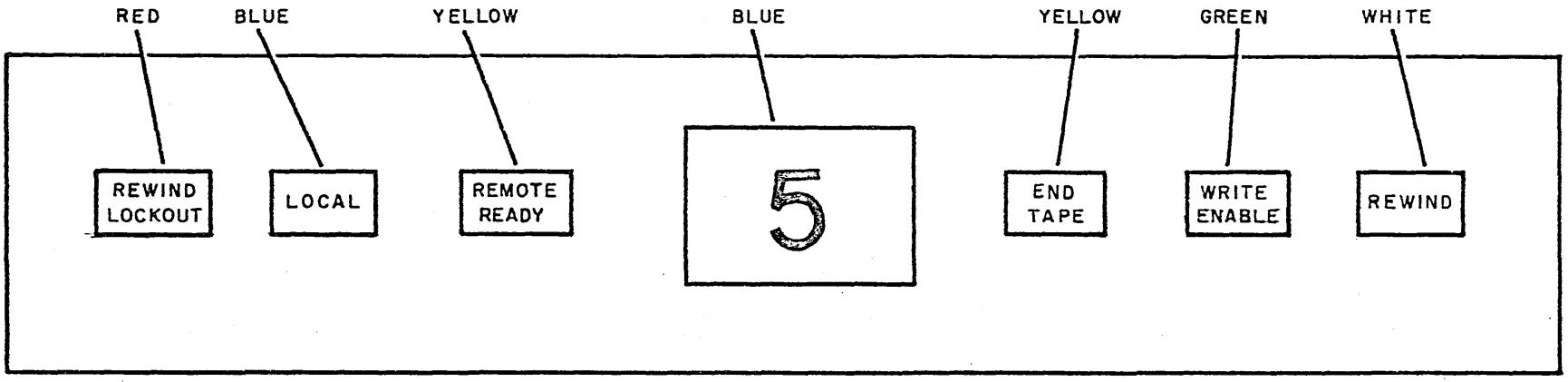


Figure 3-4 Tape Transport Top Indicator Panel

Rewind Lockout Light and Reset Switch

This light indicates that a Rewind and Lockout order has been accepted by the transport. The Rewind Lockout indication must be removed (by depressing the indicator) before the transport can be removed from Local status.

Local Light and Reset Switch

This light indicates that the transport is in Local status (i.e., it cannot be controlled from the IOP). If the condition which put the transport in Local status no longer is present, the transport can be removed from that status by depressing the Local indicator.

Remote Ready Light

This light indicates that the transport can only be controlled from the IOP. (If the Local light is also lit, the transport cannot be controlled from any source) The Remote Ready light is lit when the Auto-Standby-Manual switch, below the door, is in the Auto position.

Unit Light

This numeral indicates the physical location of the transport.

End Tape Light

This light indicates that the metallic leader, at either the beginning or end of tape, is being sensed at the appropriate sensing post. When the leader moves away from the post, the light is extinguished.

Write Enable Light

This light is lit when a Write Enable ring is on the supply tape reel.

Rewinding Light

This light indicates that a Rewind, or Rewind Lockout, order has been accepted by the transport. While the Rewinding light is lit, orders from the IOP cannot be accepted. The light is extinguished when rewinding is complete.

4. AU DATA AND CONTROL REGISTERS

The Data Registers

The Data Registers are shown on Figure 4-1. Consider the flow of data during a forward read type instruction.

Information from the read heads in the transport is placed in the Matrix Buffer Register (MBR) via the Matrix. The MBR is a 14 bit register made up of two sections; one for each character in a frame. In general, due to skew, information will not arrive at all 14 positions of the MBR simultaneously. All bits associated with a character must, however, be received by the MBR before the sprocket following that character is sensed.

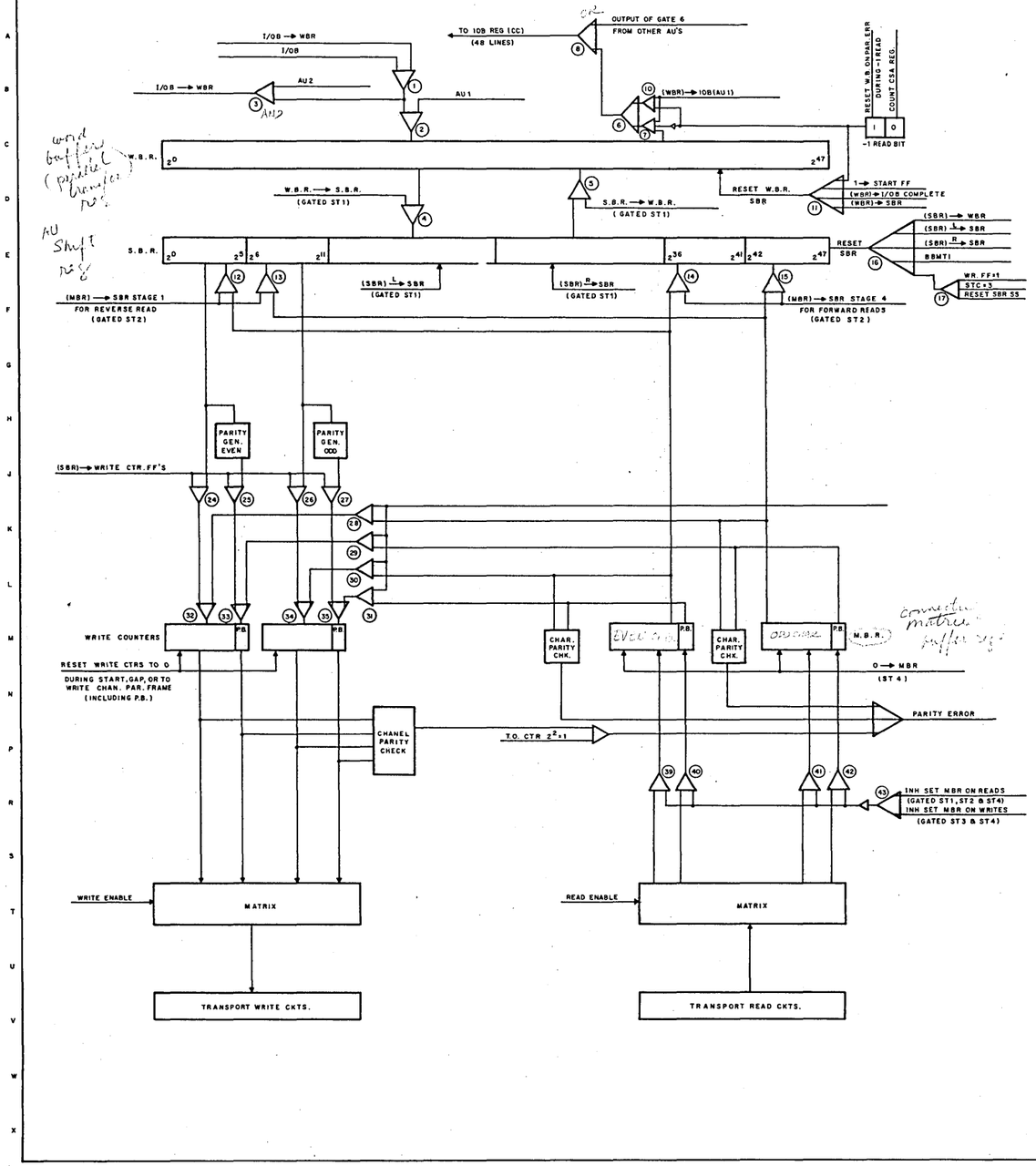
Sensing of the sprocket allows each character in the MBR to be tested for parity. Concurrent with this test, (MBR) are transferred to the Shift Buffer Reg. (SBR) and the Write Counters. (Note that the parity bits are not sent to the SBR). The MBR is cleared following this transfer in preparation for receiving the next character. From the time of sensing a sprocket, until the MBR is cleared, the reading of bits into the MBR from the transport is inhibited.

The SBR is a 48 bit register capable of shifting, either left or right, 12 positions at a time. During a shift left, for example, the binary digit in the 2^{-35} position is transferred to 2^{-23}, etc. The register is composed of shift FF's which permit shifting without an auxiliary register (contrast with shifting in the Central Computer). The shifting procedure is as follows:

First, all flipflops in the register are reset to 0. If, before this reset, a flipflop contained a 1, a pulse is propagated through a delay network. After the resetting pulse is removed, the output of the delay network can be gated into the new position.

In addition to shifts within a register, this method can be used to transfer the contents of one register to another.

It has been mentioned that following a sprocket pulse the contents of the MBR are gated into the SBR. For forward read type instructions, (MBR) are gated to positions 2^{-36} through 2^{-47} (referred to as "Stage 4"). Prior to transferring (MBR) to SBR again, the SBR is shifted left (12 places).



INDEX OF FF'S, SS'S, COUNTERS, & REGISTERS

Name	Card †	Fig	Co-ord
* AU New Order FF's	2-88/87	5-1	C-15 & 20
Address Comparison FF	1-50/75	4-2	J-5
AU Instruction Delay SS (FNO)	2-90	5-1	B-9
Auto Reset FF	1-3/78	7-1	A-11
AU Select Register	2-76	5-1	H-18 & 20
Backspace Error FF	2-71/70	4-2	M-2
BBMT1 FF	1-2/77	7-1	G-2
Begin FF	2-98		
Begin Tape Error FF	1-13/88	4-2	S-18
Block FF	1-3/78	7-1	D-8
Block/Gap FF	1-3/78	7-1	B-7
Block Mark FF	1-3/78	7-1	D-5
Block Mark Counter	1-25/100	7-1	B-23
B.M. Recognition SS's	1-25/100	7-1	A-21
* Block Mark SS's	2-73/72	7-1	C-24
Change FF	1-1/76	4-2	H-27
Char. Parity Write (Even)	1-45/70	4-1	N-4
Char. Parity Write (ODD)	1-30/55	4-1	N-6
Continue FF	1-4/79	4-2	F-19
Core Address Buffer Reg.	1-16/91	4-2	M-11
Core Address Reg.	1-35/40-60/65	4-2	K-11
* Core→Tape Req. FF	2-85/84	5-1	R-1
Core Address Adjust FF		7-1	W-28
D. R. Copy Switch FF	1-12/87		
D.R. Error F.F.	1-13/88	4-2	S-14
D.R. 1st Copy FF	1-12/87		
D.R. 2nd Copy FF	1-12/87		
Edit FF	1-4/79	4-2	F-13
Edit Continue FF	2-98		
End Tape Error FF	1-13/88	4-2	S-20
Erase FF	1-4/79	4-2	F-17
Error Read FF	1-23/98	4-2	K-29
Error Set OK FF (Even)	1-18/93	7-1	S-28
Error Set OK FF (ODD)	1-7/82	7-1	S-28
Fault Register		4-2	S-9-22
First Pass FF	1-2/77	4-2	K-17
FNO Timing FF	2-90	5-1	C-9
Format Error FF	1-13/88	4-2	S-12
Forward FF	1-22/97	4-2	F-7
Forward Holding FF	1-1/76	7-1	F-7
* Full BM not Received FF	2-73/72	7-1	D-23
Initiate FF	2-96		
Initiate Timing FF	2-96		
* IOB Full FF	2-85/84	5-1	R-4
LNO1 SS	2-77	5-1	D-27
LNO2 SS	2-77	5-1	D-30
* Manual Mode FF	2-95/94		
Manual Read Forward FF	1-21/96		
Marking SS (Matrix)	2-79	5-1	M-25
Matrix Buffer Reg	1-9/16/84/91	4-1	N-15
Matrix Marking FF's (Path)		5-1	S-26
Mode A FF	1-22/97	4-2	F-10
Mode B FF	1-22/97	4-2	F-11
NBP Register	1-39/64	4-2	J-15
NBS Register	1-36/61	4-2	H-15
Osc. Counter	1-36/61	7-1	B-16
Osc. Counter Extension	2-98		
Osc. FF	1-12/87	7-1	T-4
Osc. SS's	2-92	5-1	U-17
Parity Error FF	1-13/88	4-2	S-14
Pattern Counter	1-21/96	4-2	T-26
Print FF	1-4/79	4-2	F-14
Read FF	1-22/97	4-2	F-3
Read Enable FF	1-1/76	7-1	G-4
Release Matrix SS	2-95/94	7-1	W-13
*Release Order FF	2-71/70	4-2	F-22
Resume Write FF	1-4/79	4-2	K-20
Resume Write Enable FF	1-4/79	4-2	H-19
Reverse FF	1-22/97	4-2	F-8
Reverse Holding FF	1-1/76	7-1	F-8
Sense FF	2-98		
Shift FF (Even)	1-17/92	7-1	S-16
Shift FF (ODD)	1-8/83	7-1	S-16
Shift Buffer Reg.		4-1	D-9
*Shift Buffer Reset SS	2-73/72	7-1	F-26
Shift Transfer Ctr. (Even)	1-17/92	7-1	S-14
Shift Transfer Ctr. (ODD)	1-8/83	7-1	S-14
Space FF	1-24/99	7-1	X-20
Space Error FF	1-13/88	4-2	S-21
Sprocket Error FF	1-13/88	4-2	S-11
Sprocket Write (Even)	1-45/70	7-1	X-6
Sprocket Write (ODD)	1-30/55	7-1	V-6
ST1 T1 SS	1-18/93	7-1	K-4
ST1 T2 SS	1-7/82	7-1	K-4
ST2 T1 FF	1-18/93	7-1	K-14
ST2 T2 FF	1-7/82	7-1	K-14
ST3 T1 SS	1-18/93	7-1	K-22
ST3 T2 SS	1-7/82	7-1	K-22
ST4 T1 FF	1-18/93	7-1	K-28
ST4 T2 FF	1-7/82	7-1	K-28
ST4 Memory FF (Even)	1-5/80	7-1	S-30
ST4 Memory FF (ODD)	1-5/80	7-1	S-30
Start FF	1-3/78	7-1	D-4
Stop FF	1-3/78	7-1	D-6
Stop at End Block FF	1-24/99	7-1	E-29
*Stop Order FF	2-95/94	4-2	F-20
*STT Sprocket Enable FF	2-67/66	7-1	C-18
*Tape→Core Req. FF (Even Half)	2-85/84	5-1	R-2
*Tape→Core Req. FF (ODD Half)	2-85/84	5-1	R-3
*Time Out Counter	2-67/66	7-1	E-16
*Time Out Counter Enable FF	2-67/66	7-1	C-16
Transport Address Reg.	1-50/75	4-2	J-4
Transport Disabled FF	1-24/99	4-2	S-9
Transport Manual FF	2-96		
Word Buffer Register		4-1	B-9
Word Counter	1-39/64	4-2	R-4
Write FF	1-22/97	4-2	F-5
Write Counter FF's		4-1	N-3
Write Enable FF	1-1/76	7-1	G-6
Write Sprocket Enable FF	1-1/76	7-1	G-22
-1 Read Bit FF	1-24/99	4-1	B-16
-1Read FF	1-4/79	4-2	F-16
2^0 - 2^1 Counter	2-98		
2 SSS 1 SS	1-5/80	7-1	U-30
2 SSS 2 SS	1-5/80	7-1	U-31
*3 Frame Delay Ctr.	2-75/74	7-1	U-23
16 Reset FF	1-3/78	7-1	A-9
22/44 μs Counter	2-83	5-1	V-15

† 2-Refers to cards in the 52000 cabinet.
1-Refers to cards in the 51000 cabinet.

* 1 card required per AU

FF = FLIP FLOP
SS =

Figure 4-1 Data Register 4-2

This process is repeated until 4 frames have been assembled into a TRANSAC word in the SBR. At this time (SBR) are transferred to the Word Buffer Register (WBR).

The WBR is another 48 bit register composed of Shift FF's. Unlike the SBR, no shifting occurs within the WBR. The shifting feature is used only to transfer (SBR) to the WBR during read instructions or to transfer (WBR) to the SBR during write instructions. During read operations the WBR holds the assembled word (received from the SBR) until it can be transferred to the IOB (in C.C.) for storage in memory.

Memory access considerations (variable) determine how long the WBR must hold each word. The necessity for the WBR arises from the fact that the SBR must be free to assemble the first frame of the following word within 22 μs of completing assembly of the first word. Since memory access (for this AU) may not be provided by this time, a temporary storage location is required.

The test for channel parity is made in the Write Counters; a 14 bit register composed of counter flipflops. During a read operation each frame (including dummy and channel parity) is gated from the MBR to the Write Counters concurrent with the transfer from MBR to SBR. Each binary 1 received by one of the Write Counter FF's, results in the flip-flop being upset to the opposite state. Thus, since the Write Counters are not reset between frames, an indication is available (after the entire block is read) as to whether an odd or even number of 1's were sensed in each channel.

A similar flow of data occurs during reverse read operations except that (MBR) are gated into positions 2^0 through 2^{11} of the SBR (referred to as "Stage 1"), and the SBR is shifted right during assembly of a word.

The preceding discussion, for simplicity , dealt with data movement in terms of frames (from MBR to SBR, and through the SBR). Actually each character of a frame is handled independently under control of the associated sprocket. Thus, the even character may be transferred from MBR to SBR and to the Write Counters while the odd character is still being formed in the MBR (or vice-versa). Furthermore, the even and odd characters may be shifted through the SBR and gated into the WBR independently. The WBR must wait until both sets of characters are received, however, before a transfer to IOB Reg. request can be made by the A.U.

During write type operations the data flow is as follows:

A word from core memory is placed in the SBR via the IOB and WBR. When writing is to take place (i.e. - every 22 μs within a block), Stage 1 of the SBR is transferred to the Write Counters. Any positions of the Write Counters which receive a 1 will be upset to the opposite state. This change of state of a flipflop results in a reversal of current through the corresponding write head (in the transport) which is the necessary condition for writing a 1 in the NRZ method.

Each character is the SBR (Stage 1) is encoded to determine if the Write Counter positions for character parity must be upset.

The SBR is shifted left (12 positions) after each frame is written. Every fourth frame, a new word is brought in from core memory.

Writing of the dummy frame is accomplished simply by writing a frame with the SBR cleared to zero. Note that a parity bit (1) is written with each character of the dummy frame.

Before writing of a block begins, the Write Counters are reset to 0's. After writing the dummy frame and 512 information frames, the Write Counters are again reset. The output of the Counters at this time writes the channel parity frame. Since the flipflop for a channel in which an odd number of 1's had been written will undergo a change of state during this reset, the required effect of channel parity (that all channels contain an even number of 1's) is achieved.

During the readback phase of a write operation, information is received by the MBR just as when performing a read operation. While in the MBR each character is checked for parity, and the MBR is then cleared. No transfer of data to the SBR or to the Write Counters occurs since this would interfere with the writing process. It follows from the foregoing that channel parity cannot be checked during write operations.

Note the lines "Read Enable" and "Write Enable" going into the matrix. These lines must be active for data from the read heads (in the transport) to reach the MBR (Read En.) and for data in Write Counters to reach the write heads (Write En.)

While performing a write operation, both of these lines are active (Read En. must be active both for sensing the block marks and

for readback). During read operations only the Read En. line is active. Thus, when reading, even though the Write Counters are being stepped (for channel parity checking) no writing can take place.

The data flow during a -1 Read order is identical to other read operations except where a character parity error occurs. When this happens the -1 Read Bit FF [B-16]* is set to 1 after the word is completely assembled in SBR. The Transfer from SBR to WBR is overriden since WBR is held to zero by the -1 Read FF being in the 1 state. Now, when (WBR) are transferred to the IOB, all zeros will be sent except in the 2^0 position which is 0Red with the -1 Read Bit FF.

Control Registers

The Control Registers, mentioned earlier, will be discussed here in more detail. Included in this group are the:

1) Command Register

2) Core Storage Address Register (CSA)

3) Core Address Buffer Register (CAB)

4) Number of Blocks to Space Register (NBS)

5) Number of Blocks to Process Register (NBP)

6) Transport Address Register (TA)

7) Word Counter (WC)

8) Error Register

All of these registers are shown on Figure 4-2.

The Command Register

The Command Register holds information indicating the instruction to be performed by the AU. Comprising the register are the following flipflops:

* Symbols in brackets refer to drawing coordinates.

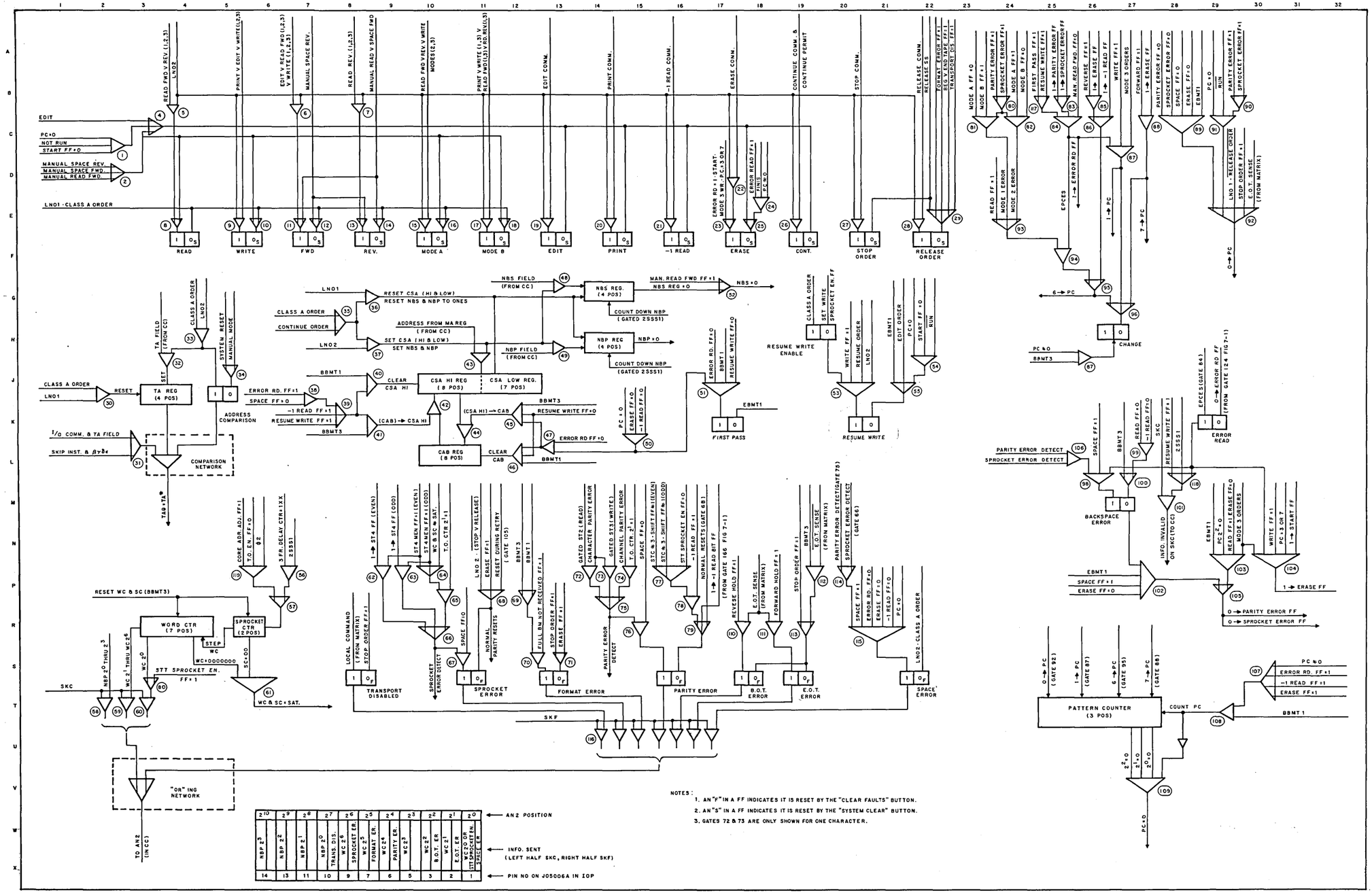


Figure 4-2 Control Registers & Misc. Execution Circuits

Read, Write, Forward, Reverse, Mode A, Mode B, Edit, Print, -1 Read, Erase, Continue, Stop Order, and Release Order [F-3 through F-22] .

Forward, Reverse, Mode A, and Mode B are used in Read and Write instructions to establish the direction of tape motion and the mode. The Mode A and Mode B FF's form a mode indicating register of which Mode B is the low order bit. Thus, for example, during a Read Fwd, Mode 1 instruction the Read, Foward, and Mode B FF's would be set to 1.

Other FF's in the register are set during the appropriate instructions. The details of setting and resetting these FF's as well as their function in the execution of an instruction, will be covered in the description of the individual instructions.

The CSA and CAB Registers

The CSA Register [K-11] is a counter type register which contains the address of the next core memory location to be accessed by the AU. Its size (15 bits) permits addressing of a 32K core memory. For smaller memories, 1, 2 or 3 of the high order positions would not be used.

Since the first memory location to be accessed is indicated by the address part of the TIO instruction, the CSA Reg is loaded from the PR in C.C. (via the MA Register, also in C.C.)

When a memory access is required, the CSA Reg. is transferred to the IO MA Register (in C.C.) from where the actual addressing is performed. Following each memory access the CSA Register is counted up by one.

There are several cases where the starting address of a block must be restored following the processing of the block from or to memory (i.e. after counting the CSA Register 128 times, the address contained before counting began must be restored). These cases are:

1) If reprocessing of the block is required due to an error in the previous processing. (Reference here is to automatic reprocessing as provided by the Read and Write instructions)

2) If a -1 Read instruction is given

3) If a Resume instruction is given following a Write instruction which has processed at least one block (not necessarily immediately following, as long as the Write FF is still set). The restoration is made on the first resumed block only.

The CAB Register [M-10] facilitates this restoration. This 8 position register can receive information from, or send information to, the 8 high order positions of the CSA. The positions of the CSA connected to the CAB are referred to as CSA High; the remaining 7 positions being CSA Low.

Note that when the CSA Register is counted 128 times (while processing a block), CSA Low will contain the same number as when counting began, but the CSA High portion will be increased by 1. Prior to processing the block the CAB Register was loaded with (CSA High); now, if restoration of the CSA is required, the CAB can be transferred back to CSA high. Thus, CSA High is restored from CAB while CSA Low is restored by the counting process.

The NBS Register

This 4 bit register is loaded from the NBS field of the "D" Register (when required) and is counted down each time a block is spaced over. The contents of the NBS register must be zero before processing to or from C.C. can begin.

The NBP Register

The NBP is also a 4 bit register which is loaded from the "D" Register. For each block processed the NBP Register is counted down by 1. The NBP Register is not counted during the reprocessing of a block due to error nor is it counted during -1 Read or Erase Instructions. If a Resume instruction is given following a Write instruction (i.e. - while the Write FF is set to 1) which has processed at least one block, the NBP Reg is not counted during processing of the first resumed block. The assumption here is that the last block processed during the Write instruction contained an error and must be rewritten, but this block was counted when previously processed.

During Skip Check instructions, (NBP) are gated to AN2 positions 2^7 through 2^{10} for comparison with the address part of the Skip Check instruction.

Transport Address Register

When a TIO instruction is given, the TA Register holds the address of the last transport which was processed through the AU. This information is used by the Multiplexer in determining which AU (if any) will perform the current instruction. The determination is based on a comparison of the TA Register with the TA field of the "D" Register. If these two quantities are equal, the "TAθ = TA*" line becomes active. Use of this line will be covered later. In the line title "TAθ = TA*", θ has the value corresponding to the particular AU (i.e. -1, 2, 3, or 4).

Note that the Compare FF [J-5] must be set to 1 for the "TAθ = TA*" line to be active. This FF is set to 1 by the first Class A instruction to use the AU and is only reset when a System Reset or Manual Mode operation is initiated. The Compare FF effectively allows the TA register a "no address" state as contrasted with zero which represents an address.

During TIO instructions, comparison is initiated by the upper leg of gate 31 becoming active. This leg represents the four lines from the TA field of the "D" Register being gated by the line "IO Command". The conditions under which this line becomes active will be covered under Multiplexer operation.

The TA Register is also used in Skip Check and Skip Fault instructions to select the proper AU for interrogation. When those instructions are being performed, the TA Register is compared with a portion of the PR to generate the "TAθ = TA*" condition. In the case of the Skip instructions, "TAθ = TA*" gates information to AN2 (in C.C.) instead of controlling Multiplexer action. Further details of this operation will be given with the Skip instruction analysis.

The contents of the TA Register can only be altered when a Class A instruction is assigned to the AU.

The Word Counter (WC) and Sprocket Counter (SC).

The WC [R-4] is a 7 position counting register which indicates the number of words remaining to be read in a block.

Closely associated with the WC is the Sprocket Counter (SC) [R-6] a two position counter. The SC is counted down once for each sprocket pair sensed following the first 3 pairs. Thus the SC is stepped

512 times while reading a block. Each time the SC counts from 0 to 3 (i.e. - every 4th count), the WC is counted down by one. This follows from the fact that 4 frames are required to make a word. The first 3 sprocket pairs are not counted because there are 3 more sprocket pairs than there are information frames.

The status of the WC and SC, with relation to the amount of information actually remaining to be read, is shown in Table I.

During a Skip Check instruction, the contents of the WC are gated to the 7 low order positions of AN2 (in C.C.) where comparison with the address part of the Skip Check instruction takes place. (Remember that the contents of the NBP were gated to positions 2^7 through 2^{10} of AN2 by the Skip Check instruction)

Table I indicates a precaution necessary when interpreting the result of the Skip Check instruction. When the WC indicates that N words remain to be read, there may actually be N + 1/2 remaining. In other words, if the result of the Skip Check instruction is taken to mean that 128-N words have been read, the $(128-N)^{th}$ word may not yet be in memory. This fact is further aggravated when several A.U.'s are being multiplexed; a delay of approximately one word time may exist between the complete assembly of a word and its transfer to memory. Programming precautions must be taken to overcome this time offset. After processing a block the WC and SC should be counted back to their initial settings. A test is made for this condition, and if it does not exist the Sprocket Error FF is set.

The Error Register

The Error Register is made up of the following 7 FF's (starting with the low order position):

1) Space Error

2) End Tape Error

3) Begin Tape Error

4) Parity Error

5) Format Error

TABLE 4-1

	SC	WC	Words Actually Remaining to be Read
Before Reading	0	0	128
After 1st SP. PR.	0	0	128
After 2nd SP. PR.	0	0	128
After 3rd SP. PR.	0	0	127-3/4
After 4th SP. PR.	3	127	127-1/2
After 5th SP. PR.	2	127	127-1/4
After 6th SP. PR.	1	127	127
After 7th SP. PR.	0	127	126-3/4
After 8th SP. PR.	3	126	126-1/2
Status after 9th through 510th pairs follows pattern established by 5th through 8th pairs.			
511th	0	1	3/4
512th	3	0	1/2
513th	2	0	1/4
514th	1	0	0
515th	0	0	0

6) Sprocket Error

7) Transport Disabled

The Space Error FF is set if a parity error of sprocket error occurs while spacing prior to processing. If parity or sprocket errors occur while spacing due to a retry or due to a -1 Read or Erase instruction the Space Error FF is not effected. Resetting of the FF occurs when a Class A order is received or when the Clear Fault button on the Operator Panel is pressed.

The End Tape Error FF is set if an attempt is made to move tape forward into the metallic end-of-tape leader. The flipflop can be reset as follows:

1) By giving an instruction, other than Rewind or Rewind L.O., which moves tape in the reverse direction. (e.g. - Read Reverse, -1 Read, or Erase).

2) By Rewinding and then giving an instruction which moves tape forward (e.g. - Read Forward or Write).

3) By performing the Stop instruction.

4) By pressing the Clear Fault button.

The Begin Tape Error FF is set if an attempt is made to move tape backward into the metallic beginning-of-tape leader. Resetting occurs as follows:

1) By giving an instruction which moves tape forward (e.g. - Read Forward or Write).

2) By performing the Stop Instruction.

3) By pressing the Clear Fault button.

The Parity Error FF is set if a character parity error or channel parity error is detected while processing a block (except when spacing or erasing for any reason or when a channel parity error is detected on -1 Read). The FF is reset as follows:

1) By backspacing due to retry of a write operation (EBM time).

2) By erasing due to either an Erase instruction or a Mode 3 Write.

3) Following a retry during a Mode 3 Read (EBM time).

4) By backspacing without a parity error or sprocket error during a read retry operation (EBM time).

5) By the initiation of any order which moves tape except Rewind and Rewind Lockout.

6) During a -1 Read instruction following each word that contained a parity error.

7) By pressing the Clear Faults button.

The Format Error FF is set if 9, but not 25, contiguous B.M. pulses are received. Resetting occurs for the duration of the Stop and Erase commands. Erasing due to Mode 3 Write also resets the F.F. as does pressing the Clear Faults button.

The Sprocket Error FF is set if the WC and SC have not been counted back to their original settings (i.e. SC = 0, WC = 0) or if either channel alone has picked up an extra sprocket when reading of a block is complete. Also, if 2 even sprockets are sensed between two odd sprockets (or vice versa) the FF is set; this implies the loss of an odd (or even) sprocket or the pickup of an even (or odd) sprocket within the sprocket region. Resetting of the FF is identical to that for the Parity Error FF with the exception of (6).

The Transport Disabled FF is set if the selected transport goes into Local Command status while connected to the AU. via the matrix. Reset is by the execution of a Stop order or pressing the Clear Faults button.

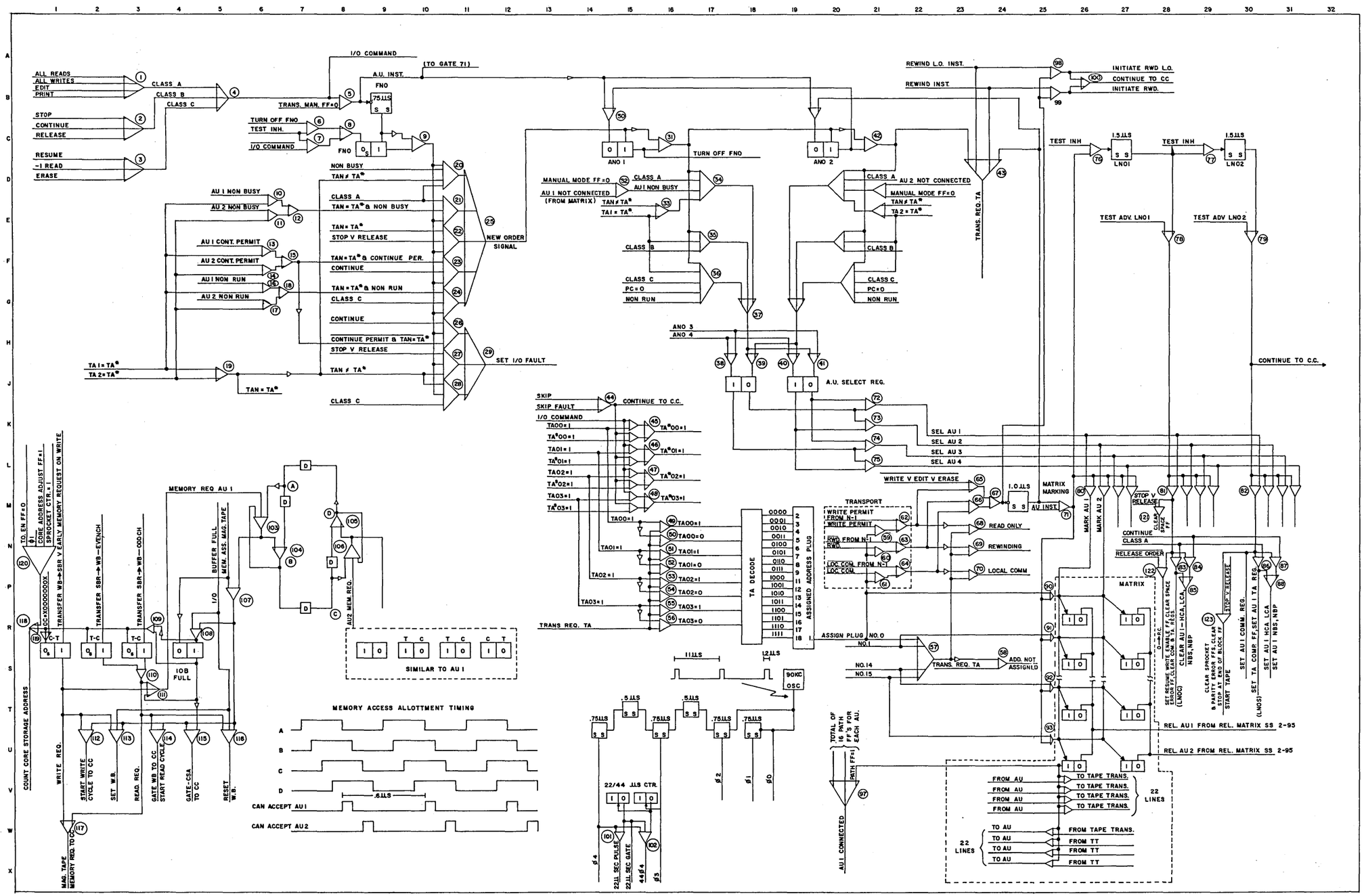


Figure 5-1 Multiplexer

Gate 20:

1) If a Class A order is in the "D" Register (i.e. - the output of gate 1 is active), and

2) If the address of the transport required by this order is not contained in the TA Reg of any AU, and

3) If at least one AU is "non-busy" (i.e. - is not connected to the matrix)

Gate 21:

1) If a Class A order is in the "D" Register, and

2) If the address of the transport required by this order is contained in the TA Register of an AU, and that particular AU is non-busy.

Gate 22:

1) If a Stop order or Release order is in the "D" Register, and

2) If the address of the transport required by this order is contained in the TA Register of an AU.

Gate 23:

1) If a Continue order is in the "D" Register, and

2) If the address of the transport required by this order is in the TA Register of an AU, and that AU will accept a Continue order. (as indicated by the "Continue Permit" line being active. This will be covered with the Continue instruction)

Gate 24:

1) If a Class C order is in the "D" Register (i.e. the output of gate 3 is active), and

2) If the address of the transport required by this order is in the TA Register of an AU, and that particular AU is in "non-run" status (i.e. - tape is not moving in the transport indicated by the TA Register.)

Under certain conditions a "Set IO Fault" signal (from gate 29) will be sent to C.C. if none of the gates 20 through 24 are satisfied. These conditions are specified by gates 26 through 28 as follows:

Gate 26 is active if a Continue order is in the "D" Register but no AU TA Register contains the required address or, if an AU does contain the address, that AU will not accept a Continue Order.

Gate 27 is active if a Stop order or a Release order is in the "D" Register and no AU TA Register contains the required address.

Gate 28 is active if a Class C order is in the "D" Register and no AU TA Register contains the required address.

Note that the absence of an active output from gate 25 does not necessarily imply an active output from gate 29 (e.g. - a Class A order in the "D" Register and all AU's' busy). The FNO FF is reset (via gate 7) when an IO command is not present.

In the operations just described it was necessary to determine if the address contained in the TA field of the "D" Register was the same as that in one of the AU TA Registers. The TA field is gated to the TA Registers for comparison (via gates 45 through 48 [L-16] by the "IO Command" signal which is the output of gate 4. Comparison is made simultaneously in all AU's.

When the output of gate 25 goes active, it has been established that an AU is available to perform the instruction. Now a particular AU must be selected.

The output of gate 25 sets the ANO 1 FF (Assembly Unit New Order - AU 1) to 1 which results in the FNO FF being reset. When this occurs the output of gate 31 becomes active conditioning gates 34, 35 and 36. An active output from one of these gates indicates that AU 1 can perform the current instruction.

Gate 34 is active if the instruction is Class A, AU 1 is non-busy, and the required transport address is not contained in the TA Register of some other AU.

Gate 35 is active if the instruction is Class B and AU 1 contains the required transport address.

Gate 36 is active if the order is Class C, AU 1 contains the required transport address, AU 1 is in non-run status, and AU 1 is not in the process of retrying due to an error or cycling in a -1 Read or Erase order.

Should any of these 3 gates become active, the AU Select Register [J-19] will be set to 0 via gates 37, 39 and 41.

When the output of gate 31 became active, the ANO 2 FF was set to 1, thus resetting ANO 1. This allowed gate 42 to go active; testing AU 2 for acceptance of the order just as gate 31 tested AU 1. Testing of AU 2 takes place even though AU 1 has accepted the order, and if AU 2 can accept the order, the AU Select Register is set to 1 (gates 39 and 40). Note that if both AU 1 and AU 2 accepted the order, the AU Select Register would be set to 1 since that was the later set. Thus, if more than one AU can accept an order (a Class A order where TAN $\neq$ TA*) the highest numbered AU will be assigned the execution of the order. The AU Select Register is decoded by gates 72 through 75 to provide an appropriate select line. Before this line can be used, however, it must be established that the required transport is able to perform the order.

The output of gate 42, in addition to testing AU 2, provided a "Transfer Requested TA" line (gate 43), which gates the TA field of the "D" Register (gates 49 through 56) to the Assigned Address Plugs via a decode network. If a plug is in place for the required transport address, a signal will be sent to the transport and to gate 57. Note that if the required plug is not in place, the Address not Assigned light will be turned on via gate 58.

In the transport, tests are made as follows:

Gate 59 indicates that the Write Ring is in the reel.

Gate 60 indicates that the transport is not rewinding

Gate 61 indicates that the transport is not in Local Command Status.

Gates 62, 63 and 64 accept similar signals from other transports.

If the selected transport is neither rewinding nor in Local Command, gate 66 will be active via gates 63 and 64. Furthermore, if the Write Ring is in the reel, or if the current order is not a Write, Edit, or Erase order, gate 65 will be active making gate 67 active.

Gate 67 fires the Matrix Marking single shot and partially conditions the rewind and rewind lockout gates (99) and (98).

The Matrix Marking single shot sustains the "Transfer Requested TA" line active via gate 43 and resets the ANO 2 FF. The SS output also will partially condition (via gate 71) the set of 4 gates of which gate 80 is typical. (The lower leg of gate 71 is conditioned by the output of gate 5, which is active during assignment of Class A, B, or C instructions).

One of the 4 gates will have an active output (which one depends on the setting of the AU Select Register) which partially conditions the inputs to a group of FF's (the Path FF's) in the Matrix. The output of the Assigned Address Plug gated by (71) provides the other condition for setting one of the FF's in the group.

For example, if transport #1 is required by the instruction, and AU #1 is assigned to execute the instruction; the FF associated with gate 91 will be set.

The setting of this FF (i.e. - marking the Matrix) establishes a path for 22 lines from transport to AU and 22 lines from AU to transport. Furthermore, gate 97 [V-20] is conditioned by this FF (or any of the FF's associated with AU 1) to generate the "AU 1 Connected" signal, which in turn is used to indicate that AU 1 is busy (see gate 32 [D-15]). Similar gates provide an indication that other AU's are connected.

After the Matrix Marking SS times out, the LNO 1 SS is fired via gate 76. During this SS timing (1.5 μs), the 4 gates of which gate 81 is typical are partially conditioned. The gate corresponding to the selected AU will have an active output to provide a condition for gates 83 and 84. If the order is Class A, the following will be performed:

1) Part of the Command Register (the Read, Write, Fwd, Reverse, Mode A, and Mode B FF's) will be cleared.

2) The TA Register will be cleared

3) The CSA Register (both High and Low) will be cleared

4) The NBS Register and NBP Register will be cleared (to ones)

5) The Space Error FF will be cleared.

6) The Resume Write Enable FF may be set.
The function of this FF is discussed later.

If the order is not Release, the Pattern Counter (PC) will be reset to 0. The use of this counter is discussed in a later section.

Following the time out of LNO 1, LNO 2 fires.

Through gating similar to that for LNO 1, LNO 2 provides a setting pulse to load the Control registers with the information required to execute the instruction. Note that setting of the Command Register is not gated by "Class A" (as was the reset). LNO 2, in the absence of a Stop or Release order, clears the Sprocket and Parity Error FF's and the Stop at End of Block FF; under the same conditions a signal is given to start tape.

Finally, the LNO 2 SS provides a "Continue to C.C." signal which allows the C.C. timing to advance from IT2 to IT3.

Timing Pulse Generating Circuits Figure 5-1

Certain pulses are continuously being generated in the Multiplexer for use by all AU's. These pulses originate with the 90 KC oscillator [T-19] which has an output as shown on the Write Timing diagram (Figure 8-1). The direct output of the oscillator is referred to as "ϕ0". When the ϕ0 line goes active, the ϕ1 SS is fired, producing a 0.75 μs pulse. The ϕ 0 line becoming inactive fires the ϕ2 SS producing another 0.75 μs pulse. A displacement of 1.2 μs (i.e. - the duration of ϕ0) exists between ϕ 1 and ϕ2.

When the ϕ 2 line goes inactive a 0.5 μs delay SS is fired which, when timed out, fires the ϕ 3 SS. This 0.75 μs pulse (ϕ 3) is displaced 1.25 μs from ϕ 2 (i.e. - the duration of ϕ2 + the .5 μs delay). Another pulse (ϕ4) is generated from ϕ 3 in a similar manner.

Note that each ϕ3 steps the 22/44 μs Counter low order FF. This produces activity of the "22 μs gate" line as shown in Figure 8-1. Also, every fourth ϕ 4 pulse is gated through gate 102 to provide a "44 ϕ4" pulse.

Remember that these pulses are available to all AU's as long as power is applied to the IOP.

5. THE MULTIPLEXING CONTROL

Assignment of AU by the Multiplexer (Figure 5-1)

In the following discussion, the method whereby the Multiplexer assigns an AU to perform an instruction will be covered. Only instructions which require the establishment of a matrix path will be discussed. This excludes the Rewind and Skip type instructions.

Assignment activity is initiated by the TIO instruction being executed in C.C. This instruction is discussed in detail elsewhere; the main points pertinent to IOP operation are as follows:

1) At IT2 the output of the command part of the "D" Register (2^{-40} - 2^{-47}) is made available, via a decode network, to the IOP. On Figure 5-1 the outputs of the decode network are shown as the inputs to gates 1, 2, and 3. (The 6 Read instructions and the 3 Write instructions are represented as the single lines "All Reads" and "All Writes" respectively). The Rewind instructions, which also come from the decode network, are discussed later.

2) Upon receipt of a "Continue to C.C." signal from the IOP, the TIO instruction proceeds to IT3. If the "Continue to C.C. signal does not arrive in C.C. within 20 μs of the start of IT2, the TIO instruction proceeds to IT3. In IT3, skipping is initiated if the "Continue to C.C." signal is present; otherwise the next sequential instruction is performed.

3) The address part of the TIO instruction is made available to the IOP via the MA Register.

When an active output is generated from gate 1, 2, or 3, the FNO (First New Order) SS is fired via gates 4 and 5 (the Transport Manual FF may be assumed in the 0 state. See Chapter 18 for details). Firing of the FNO SS sets the FNO FF to 1, and after FNO SS times out (.75 μs) the output of gate 9 becomes active. While gate 9 is active, a test is made for the availability of an AU to perform the instruction. If an AU is available the output of gate 25 ("New Order Signal") will be active. Gate 25 can be made active by any one of the gates, 20 through 24, having an active output. These gates are activated as follows:

6. BLOCK MARK AND SPROCKET RECOGNITION

As mentioned in the discussion of tape format, Block Marks are used to define the beginning and end of each block. Since Block Marks are written in the same channel as one set of sprocket pulses, it is necessary to be able to distinguish between Block Mark pulses and sprocket pulses. The distinguishing feature is the time interval between pulses (which is 11 μsec for BM pulses and 22 μs for sprocket pulses).

For BM Recognition, not only must pulses be sensed at 11 μsec intervals, but requirements must be met as to the number of pulses received. Remember that, when originally written, a BBM consisted of 32 flux changes while an EBM contained 33 changes. When sensing (either a BBM or an EBM) the following tests are made:

1. If 9 contiguous BM pulses are sensed, recognition of a BM is acknowledged.

2. If, after satisfying condition (1), 16 more contiguous BM pulses are sensed, the BM has not deteriorated to a point where rewriting is considered necessary.

Should condition (1) be satisfied but not condition (2), a Format error is indicated allowing corrective action (e.g. - Erasure) to be taken. Deterioration of a BM to the point where it cannot meet condition (1) usually means that the entire tape will have to be re-edited. Condition (2) is designed to detect gradual deterioration while relatively mild corrective action is still possible.

The circuits used for BM Recognition are on the BMC card. Refer to the functional diagram of this card (Figure 6-1) for the following description.

Assume pulses to be arriving at input 27 every 11 μsecs as shown in the timing diagram. Also assume the three single shots to be in the non-fired state as the first pulse arrives.

The first pulse arriving fires SS1 and partially conditions gates 1 and 2. Since neither SS2 nor SS3 are fired when the first pulse arrives the output of gate 3 is inactive. Thus gate 2 is inhibited and gate 1 conditioned allowing the BM counter to be reset to zero (via gate 4). Note that gate 7 insures that the output of gate 4, once active, remains active for the full duration of SS1. This relatively long reset pulse overrides

any counting effect which may have resulted from changing a FF from the 1 to the 0 state, and ensures correct operation for very narrow sprockets.

While SS1 is fired, the outputs of gates 5 and 6 are both active. When SS1 times out, the output of gate 5 goes inactive, and SS2 fires. Since the BM Counter 2^0 FF is in the 0 state at this time, the output of gate 6 remains active and SS3 cannot fire. SS2 conditions gate 2 (via gate 3) for 10 μs.

The second pulse arriving at input 27 fires SS1 again and steps the BM Counter (via gate 2). When SS1 times out, the output of gate 6 becomes inactive, but the output of gate 5 remains active (since the 2^0 FF is now equal to 1). Thus SS3 fires to condition gate 2 for the next input pulse.

Each input pulse will now step the BM Counter just as the second one did. When the 2^3 FF is set to 1 (after 9 pulses), the AU is notified that a BM has been received. When both the 2^3 and 2^4 FF's are set to 1 (after 25 pulses), the AU is notified that the BM has not deteriorated beyond a safe limit (i.e. - a Format error has not occurred).

If, at anytime while counting the BM Counter, two consecutive pulses do not arrive within about 15 μs of one another, the BM Counter will be reset to zero on the second pulse since SS2 and SS3 will be timed out. Hence the condition that pulses forming a BM must be contiguous.

Logically, the work of SS2 and SS3 could be performed by one single shot which is not conditioned by the 2^0 FF. Such an arrangement would, however, result in an excessive duty cycle for the one SS.

Recognition of incoming pulses (at input 27) as Sprocket pulses simply depends on the transport read head being in the area where Sprockets should be found (i.e. - within a block rather than in the inter-block gap). This area is defined by the STT Sprocket En. FF, the operation of which will be covered in the description of the reading process.

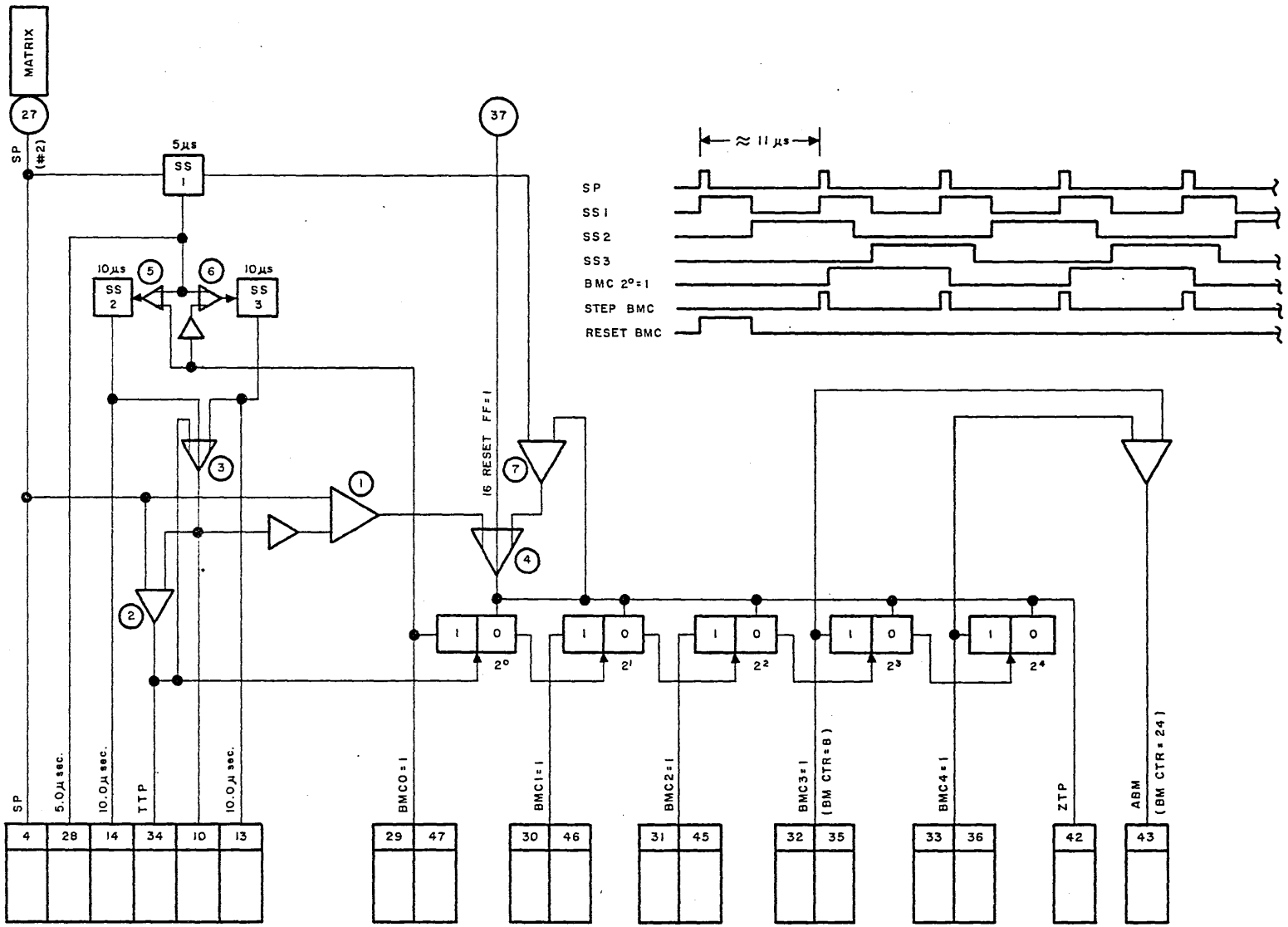


Figure 6-1 Block Mark Recognition

7. LOGIC OF READING WITHOUT ERROR

Read Forward One Block Without Spacing (no error)

The following discussion assumes that, upon execution of a TIO instruction, the Multiplexer has selected an AU to perform the reading of one block of information into CC without spacing. This implies:

1) In the Command Register, the Read FF and the Forward FF are set to 1; the Mode A and Mode B FF's are set according to the mode of reading; and all other FF's are set to 0.

2) NBS contains 0

3) NBP contains 1

4) CSA contains the first memory address

5) Any other register or FF, the resetting of which is not specifically discussed, may be assumed reset to 0 by a previous operation.

6) The Matrix has been marked.

7) A signal is received from the Multiplexer indicating the AU should proceed. (This signal is generated by the LNO 2 SS)

Reference throughout this section should be made to Figure 7-1 and the Read Timing diagram Figure 7-2.

Starting Tape Motion

If the AU is not in "Run" status when the LNOS signal is received from the Multiplexer, the Start FF [D-4] will be set to 1 via gates 165, 1, and 2 and the Block/Gap Counter FF will be cleared. (The latter action serves as a system clear for the Block/Gap FF.) The AU will not be in "Run" status if the Forward Hold, Reverse Hold, and Stop FF's are all set to 0 (see gate 12 [G-10]), and this condition prevails per the initial assumptions.

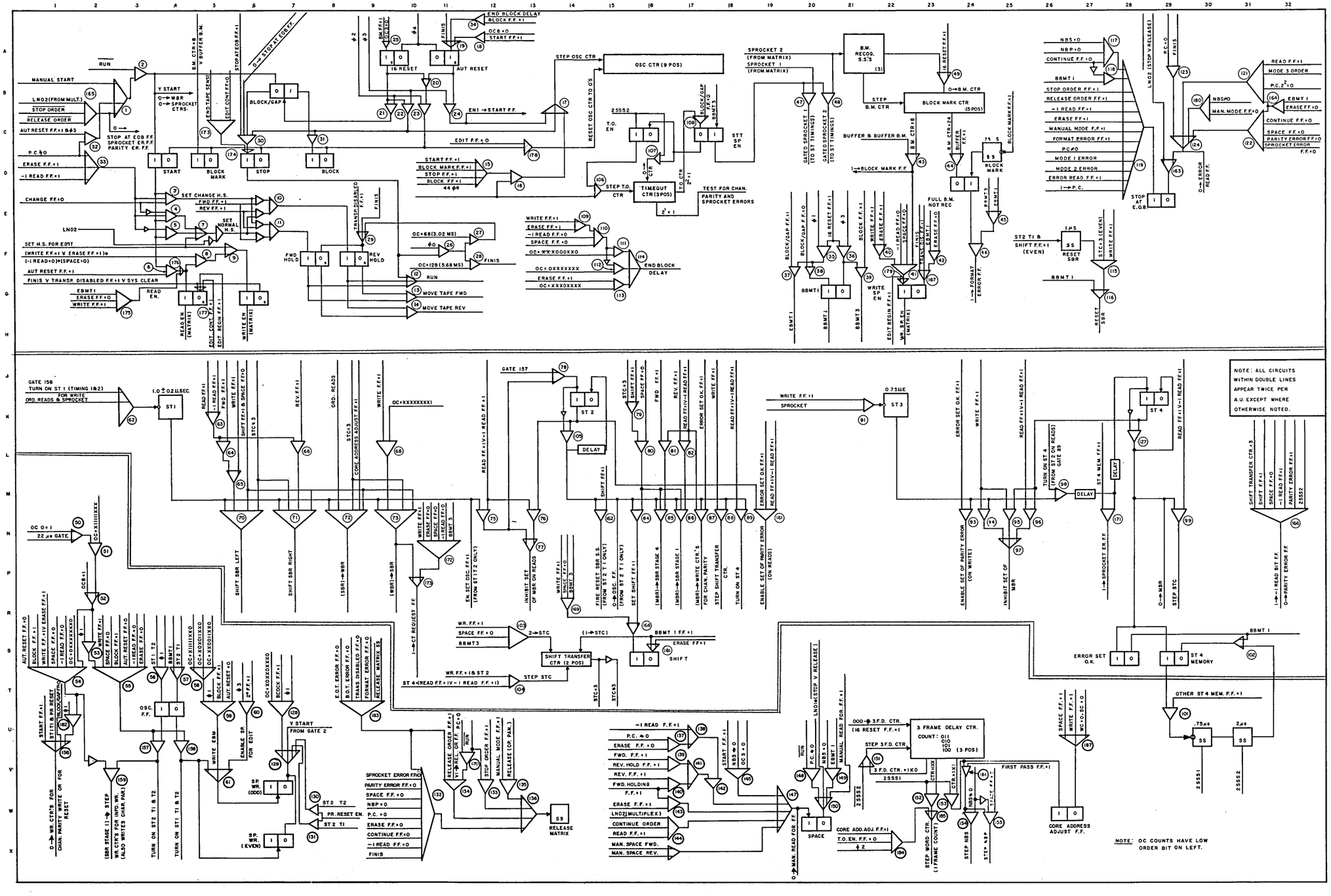
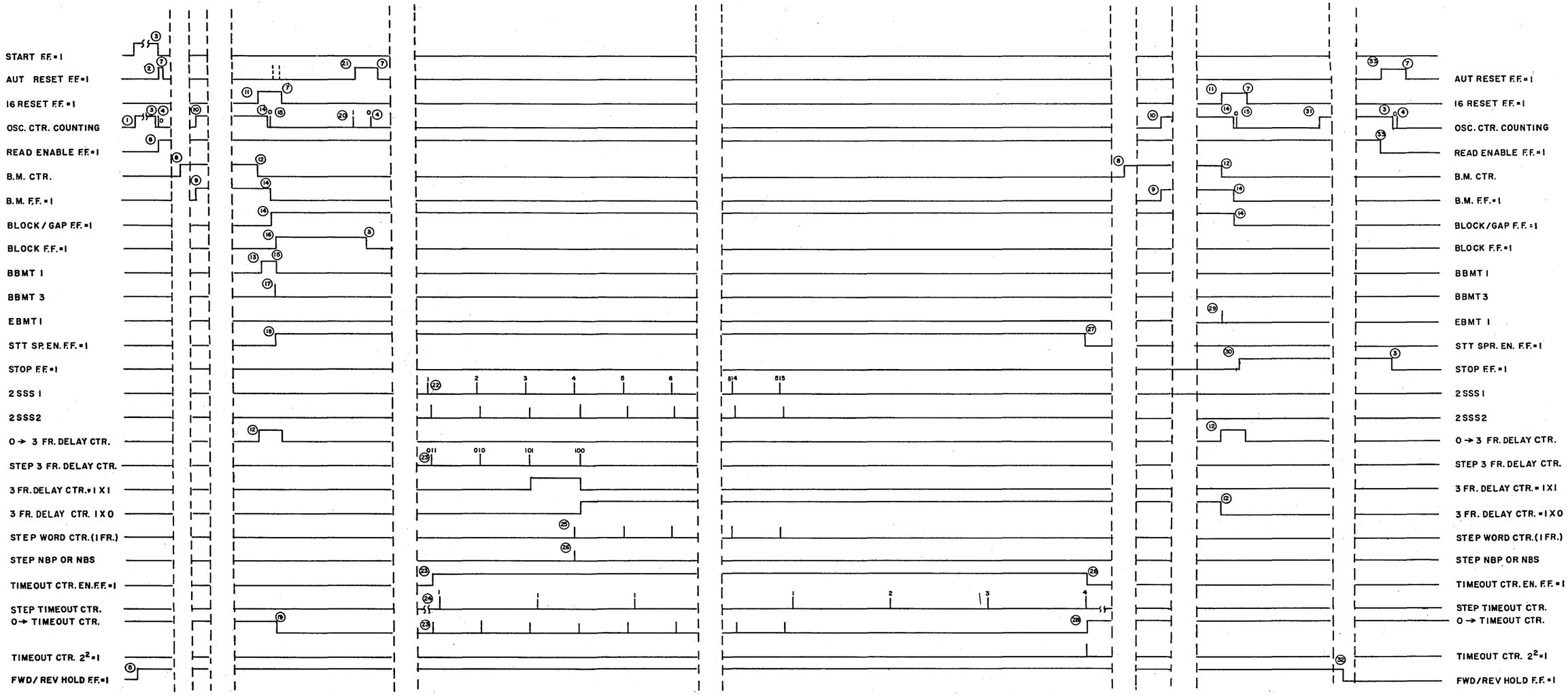


Figure 7-1 AU Execution Circuits



(1) Start FF = 1 • 44 μs count
(2) Start FF = 1 • OSC CTR = 32
(3) AUT Reset FF = 1 • $\phi 2$
(4) AUT Reset FF = 1 • $\phi 3$
(5) (Start FF = 1 • Fwd. FF = 1)
or
(Start FF = 1 • Rev. FF = 1)
(6) Start FF = 1 • AUT Reset FF = 1
(7) $\phi 4$
(8) B.M. Pulses
(9) B.M. CTR = 8
(10) B.M. FF = 1 • 44 μs count
(11) B.M. FF = 1 • OSC CTR = 8
(12) 16 Reset FF = 1
(13) 16 Reset FF = 1 • Block/Gap FF = 0 • $\phi 1$
(14) 16 Reset FF = 1 • $\phi 2$
(15) 16 Reset FF = 1 • $\phi 3$
(16) 16 Reset FF = 1 • Block/Gap FF = 1 • $\phi 3$
(17) 16 Reset FF = 1 • Block FF = 1 • $\phi 4$
(18) BBMT3
(19) STT Sprocket En. FF = 1
(20) Block FF = 1 • 44 μs Count
(21) Block FF = 1•(Write FF = Ov -1Read FF = 1 v Erase FF = 1) • OSC CTR. 2^0 = 1
(22) Both ST4 Mem. FF's = 1
(23) 2SSS2 • 3 Fr. Delay CTR. = 1 x 0
(24) Timeout CTR. En. FF = 1 • 44 μs count
(25) First Pass FF = 1 • 3 Fr. Delay CTR = 1 X X • 2 SSS 1
(26) First Pass FF = 1 • 3 Fr. Delay CTR = 1 X 1 • 2 SSS 1
(27) Timeout CTR. 2^2 = 1
(28) STT Sprocket En. FF = 0
(29) 16 Reset FF = 1•Block/Gap FF = 1 • $\phi 1$
(30) Stop at E.O.B. FF = 1 • 16 Reset FF = 1•Block/Gap FF = 0 • $\phi 3$
(31) Stop FF = 1 • 44 μs count
(32) Stop FF = 1 • OSC. CTR = 48 • $\phi 0$
(33) Stop FF = 1 • OSC. CTR = 104 • $\phi 0$

Figure 7-2 Read Timing

The upper leg of gate 5 [F-4] will be conditioned (again from the initial assumptions), so that Start FF = 1 makes the "Set Normal Hold Signal" line active through gate 7. This line, when LNO 2 retires, in conjunction with Forward FF = 1 (initial condition), sets the Forward Hold FF to 1 via gate 11.

Gate 13 will have an active output, "Move Tape Forward", which is sent to the selected transport, via the Matrix, to initiate tape motion. The AU is now in "Run" status (gate 12).

A delay of 1.4 ms is provided, before reading of tape begins, to inhibit starting transients from entering the AU. This, as well as other delays required in the AU is provided by the Oscillator Counter (OC).

The OC [A-16] is a 9-position counter which may be assumed reset to all ones initially. The positions of the counter are referred to as OC0 (low order) through OC8. When the Start FF was set to 1, gate 16 [D-12] was partially conditioned through gate 15. Each 44ϕ4 pulse will now provide a "Step OC" signal (gates 16 and 17). After OC5 is stepped up to 0 (i.e. - a count of 32), the AUT Reset FF [A-11] is set to 1 via gates 18 and 19. Since 44ϕ4 pulses arrive every 44 μs a delay of 1.4 ms was achieved between setting the Start FF and setting the AUT Reset FF.

When the AUT Reset FF is set, the Read Enable FF [G-5] is also set via gate 6. This FF provides a level, through the Matrix to the transport , which allows information sensed by the transport read heads to be sent to the IOP. In particular, the IOP may now receive BM pulses.

During the ϕ2 time following the set of AUT Reset to 1, the Start FF is reset to 0 and the OC is reset to zero (gates 20 and 23). At ϕ 3 time, the OC is rippled to all ones via gates 24 and 17; and at ϕ 4 the AUT Reset FF is reset to 0.

Note the two step method of resetting OC to all ones. First the counter is reset to zero and then it is stepped once to leave it set to all ones. This method is used to avoid the spurious counting effect which can result from setting the counter directly to all ones with a short duration pulse. Note also that the ϕ 4 clear of the AUT Reset FF overrides spurious sets of the FF at 44ϕ4 when the OC counts.

Further activity awaits the recognition of a BBM (as described previously). When the BM Counter equals 8, the BM FF is set to 1; and OC can again be stepped with 44ϕ4 pulses (gates 15, 16 and 17).

The BM FF being set to 1 fires the Block Mark SS [D-25] which in turn sets the Full BM Not Received FF to 1. When (and if) the BM Counter reaches a count of 24, the Full BM Not Received FF will be reset via gate 44. As will be mentioned shortly, a test is made of this flipflop at a time when the entire BM has passed under the read heads. If the flipflop has not been reset at this time the Format Error FF will be set.

The OC 3 FF going to 0 (i.e. - a count of 8) allows the 16 Reset FF [B-9] to be set to 1 (gate 25) which in turn resets the BM Counter to 0 (gate 49). The delay provided by OC (from the time the BM FF is set to 1, until the 16 Reset FF is set) is sufficient (.35 ms) to allow the remainder of the BM to pass under the transport read head.

During the next ϕ1 pulse, the BBMT 1 FF [G-20] is set to 1 via gates 35 and 38 (since the Block/Gap FF [B-7] is still 0). At ϕ2 time, the Block/Gap FF is upset to 1 (gate 21) while the BM FF is reset to 0 and OC is reset to zero. When ϕ3 arrives OC is stepped to ones and the Block FF [D-8] is set to 1 (gates 22 and 31). Also, during ϕ3, the BBMT 1 FF is reset (gate 36) and the "BBMT3" line is active (gate 39). The 16 Reset FF is reset at ϕ4.

The BBMT 1 and BBMT 3 signals just generated, perform various housekeeping operations prior to actually processing data. Among these operations are:

1) The resetting of the SBR by BBMT 1.

2) The resetting of the CAB Reg by BBMT 1, followed by the transfer (CSA High) → CAB by BBMT 3. This action is taken in case the block must be reprocessed due to an error.

3) Testing of the Full BM Not Received FF [D-24] by BBMT 3 (gates 45 and 46), and setting the Format Error FF if the FF has not been reset to 0.

4) The setting of the STT Sprocket Enable FF [C-18] by BBMT 3. This flipflop conditions gates 47 and 48 to allow sprocket pulses to reach the necessary circuits when reading. Gate 48 was inhibited until this time to prevent the BBM from being interpreted as a series of sprocket pulses.

Other operations of BBMT 1 and BBMT 3 will be discussed as they become relevant to the overall discussion.

Setting the Block FF to 1 allowed the OC to begin counting again via gates 15, 16, and 17. Note that after the first count, gate 112 [G-15] is conditioned generating an "End Block Delay" signal. This in turn sets the AUT Reset FF to 1 via gates 34 [A-12] and 19. During the next $\phi 2$, $\phi 3$, and $\phi 4$ times the OC is cleared to ones and the Block FF and AUT Reset FF are reset to 0. This activity produced by the Block FF has no useful effect while reading; the purpose of the Block FF will be clarified when writing is discussed.

At this point, where actual reading of information into CC is about to begin, it will be helpful to briefly state what must take place:

1) When the 1st sprocket is sensed, the MBR must be cleared to receive the first character.

2) When the 2nd sprocket is received, the dummy character is in the MBR. This character must be transferred to the Write Counters (for channel parity check) but not to the SBR (since it does not go to CC). While in the MBR, the character is checked for character parity.

3) For each of the next 512 sprockets received, a character is in the MBR which must be tested for character parity, transferred to the Write Counters (for channel parity), and transferred to the SBR (to be sent to CC). Shifting of the SBR and transfers from the SBR to the WBR must occur at the appropriate times.

4) When the last sprocket is sensed the channel parity character is in the MBR. It must be transferred to the Write Counters (for channel parity) and is also sent to the SBR. This character is not, however, sent to the WBR or CC.

5) The SC (Sprocket Ctr) must be stepped by each sprocket pair except the first 3.

6) The NBP Register must be stepped down once.

7) A test must be made for the pickup or drop out of a single sprocket within the block, and the Sprocket Error FF set if one is found. (A test of the WC which is made later, indicates an incorrect number of sprocket pairs; the pickup or drop out of a single sprocket within the block would not be detected by this test). The test referred to here cannot detect an extra sprocket if it is at the beginning or end of the block. A test for this condition is provided later.

This discussion pertains to the processing of information by characters, rather than by frames, since this is the actual procedure used. On Figure 7-1, all of the circuits within the double lines are duplicated. That is one set of circuits exist for each character in a frame.

When the 1st sprocket is sensed, the ST1 SS [K-4] is fired via gate 62. The line "Ordinary Reads & Sprocket" conditioned the gate "Ordinary Reads" being active during the -1 Read order as well as Class A Read orders.

ST 1 partially conditions gates 70 through 73. Another condition on these gates is that the Shift FF [S-16] be set to 1 and the Space FF [X-20] be set to 0. The Shift FF was set to 0 by BBMT 1, and the Space FF was cleared to 0 as the instruction began. (Gate 150 [V-20] was activated by LNO 1·($\overline{\text{STOP V RELEASE}}$)). Thus, since gates 70 through 73 are inhibited, shifting of the SBR or transferring between SBR and WBR does not occur at this time.

The line "Enable Set Osc. FF = 1" (from ST 1) is of consequence only when writing.

Gate 75 [N-12] will be fully conditioned by ST 1 since the Read FF is set to 1. This allows the ST 2 FF to be set via gate 78. Note that when ST 1 is fired or when ST 2 is set, gate 77 [N-13] is made active via gates 75 and 76 respectively. The output of gate 77 inhibits setting new information into the MBR while the contents of the MBR are being processed.

Gate 161 is inactive because the Error Set O.K. FF [S-28] was reset to 0 by BBMT 1.

When ST 1 times out, gate 105 has an active output which strobes a number of gates with the following effects:

1) Gates 162 and 88, and the line "0 → Osc. FF.", are only of interest when writing.

2) Gates 84, 85, and 86 are inhibited by gate 79 (which is a condition for gate 80) being inactive. (The Shift Transfer Counter STC [S-14] is a 2 position counter which was set to 1 by BBMT 1).

3) Gate 87 is inhibited by the Error Set O.K. FF

4) Gate 89 is active.

Hence the ST4 FF [K-28] is turned on via gate 98 [M-26] .

5) The ST 2 FF is reset after a delay.

Note that the delayed output of gate 98 strobes gate 171. If the ST4 Memory FF [S-30] is in the one state during this strobe the Sprocket Error FF will be set. At present the ST4 Memory FF is in the 0 state due to BBMT 1.

ST4 being on conditions gate 96 [N-26] to maintain the "Inhibit Set of MBR" line active. This is effectively the same inhibit discussed in connection with ST1 and ST2.

When the setting signal to ST4 subsides, the output of gate 127 becomes active with the following results:

1) ST4 Memory and Error Set OK FF's are set to 1.

2) MBR is cleared to zero.

3) STC is counted to 2 (via gates 99 [N-29] and 104 [T-13]).

4) ST4 FF is reset.

The ST4 Memory FF provides an active leg for gate 101 [U-29] ; the other leg becomes active when the ST4 Memory FF associated with the other character is set. An active output from gate 101 thus indicates that a sprocket pair has been sensed. When gate 101 becomes active, a 0.75 μs SS is fired to generate a 2SSS1" signal. When this SS times out, another SS (2 μs) is fired to give a "2SSS2" signal. The "2SSS2" pulse resets both ST4 Memory FF's to 0. Other functions of the "2SSS1" and "2SSS2" signals will be covered later.

When the ST4 FF was reset, the inhibit on setting the MBR was removed. From this time until the next sprocket is sensed, information from the read heads will be accepted by the MBR. Thus, of the 22 μs between sprockets, more than 19 μs are available for loading the MBR. This allows for considerable skew.

Sensing of the 2nd sprocket (at which time the dummy character should be in the MBR) again fires ST1 SS. Activity during this ST 1 time is similar to the first, since the Shift FF is still in the 0 state.

During the 2nd ST 2 time, however, the output of gate 87 is active since the Error Set OK FF is set to 1. Hence the contents of the MBR are gated to the Write Counters to start the channel parity count. Also, gate 161 is active to test the contents of the MBR for character parity. The ST4 FF is set via gates 89 and 98 as before.

Activity during ST4 is similar to the previous ST4 except, of course, the STC is now stepped to 3.

Arrival of the next sprocket, indicating that the first information character is in the MBR, fires ST1 as usual. Again no activity occurs during ST1 except the setting of ST2.

In ST2 time, the contents of the MBR are again tested for character parity and sent to the Write Ctrs. (gates 161 and 87). Furthermore, since the STC is now set to 3, gate 79, and hence gate 80, are active.

Gate 80 being active allows the Shift FF to be set to 1 via gates 84 and 168. Also, since gate 81 is active, an "MBR $\rightarrow$ SBR Stage 4" signal is generated via gate 85.

Activity during ST4 time is as before (With STC being stepped to 0).

During the next ST1 time (initiated by the 4th sprocket), gate 70 [N-5] will be active since the Shift FF is now set to 1 and the STC is not set to 3. (Gates 63, 64, and 65 have been active from the beginning of the instruction) The output of gate 70 going active causes the SBR to be shifted left 12 positions (that is, the half of the SBR associated with the character, odd or even, under discussion). Thus, Stage 4 is ready to receive the 2nd character.

Action in ST2 and ST4 times is similar to that for the first character. The STC is counted to 1 during ST4.

The next 2 characters are handled just as the 2nd one was, thereby filling the half of the SBR associated with even (or odd) characters. When the last of these characters was transferred to the SBR, the STC was stepped to 3 during ST4 time.

The following ST1 time finds gate 70 inhibited (STC = 3) but gate 72 enabled. (The Core Address Adjust FF was set to 1 when the 4th sprocket pair was sensed. More will be said of this FF later.) Instead of shifting, half of the SBR is transferred to the WBR. When both halves of the SBR have been transferred to the WBR, a Memory access is requested and the WBR is sent to Memory via the IOB register. The details of this process will be covered in a later section.

By transferring the SBR to the WBR, the SBR was cleared to accept the 5th character at ST2 time.

Processing of the remaining characters in the block follows the pattern established by the first 4 characters. Sensing of the 515th sprocket initiates transfer of the SBR to the WBR for the 128th (and last) time. During the ST2 time following this transfer, the MBR, which now contains the channel parity character, is transferred to the SBR as well as to the Write Ctrs. Since the SBR will be cleared before the next use (cleared by the next BBMT 1) , the presence of the parity character there presents no problem.

Consideration must now be given to the method of counting the Sprocket Counter (and consequently the Word Counter) and the NBP Register Refer to the 3 Frame Delay Counter [U-24] , which was reset to 0 by the 16 Reset FF.

This Counter is stepped, via gate 151, as each 2SSS2 signal retires unless the Counter is in the state 1XO. When the state 1XO is reached, the output of gate 151 remains active; hence, the level shifts required to count cannot be sensed.

Note the unusual counting sequence. The first four counts put the counter in the states 011, 010, 101, and 100 respectively. Since the state 100 meets the condition 1XO, only four counts can be made before resetting (with another 16 Reset signal).

Now refer to gates 152 and 153 [U-24] which are strobed by the "2SSS1" signal. Gate 152 will have an active output during the 4th "2SSS1" pulse (since the 3 Frame Delay Counter reached the status 1XX following the 3rd "2SSS2" pulse), and all subsequent "2SSS1" pulses until the 3 Frame Delay Counter is reset.

Thus, the output of gate 152 steps the SC for each sprocket pair after the third, which is the necessary effect.

Gate 153 can only become active when the 3 Frame Delay Counter is in the state 1X1. Since this state exists only during one "2SSS1" signal (the 4th), gates 154 and 155 can be strobed only once per block. Activation of gate 153 sets the Core Address Adjust FF to 1; the latter remains set because the simultaneous stepping of the sprocket counter removes the clear condition WC = 0 · SC = 0 (The SC input trigger is AC coupled).

The NBS Register is set to 0 (per the initial assumptions), and the Space FF is in the 0 state; so gate 155 will have an active output to count down the NBP Register. (The First Pass FF was set to 1 by BBMT 1 for this instruction. More will be said about this FF in the section on error retrys.)

Recall that sprocket pulses were gated to the ST timing circuits by the STT Sprocket Enable FF being set to 1. It is necessary that this FF be reset before sensing the EBM to prevent interpreting the BM pulses as sprockets. This reset is accomplished by the Timeout Counter [E-16], a 3 position counter.

Associated with the Timeout Counter is the Timeout Enable FF [E-16] which was set to 1 by the first "2SSS2" pulse. After this FF is set, each 44ϕ4 pulse steps the Timeout Counter via gate 106. Note, however, that each "2SSS2" pulse resets the counter to 0. Since "2SSS2"

pulses occur twice as frequently as 44ϕ4 pulses, the counter cannot go beyond a count of 1 while sprocket pairs are being sensed.

After the 515th sprocket pair, no more "2SSS2" pulses are generated; and the counter proceeds to a count of 4. This results in the STT Sprocket Enable FF being reset via gate 108. The test of the Write Counters for channel parity and sprocket error sensing are made when the Timeout Counter = 2 and 3 (i.e. $2^1 = 1$) or not less than 44 μsec after the last sprocket pair. Pickup, or dropout, of a single sprocket at the beginning or end of the block is detected at this time. Furthermore, any sprockets, single or pairs, which occur after the Timeout Counter reaches a count of 2 are recognized as erroneous. When the STT Sprocket Enable FF is reset, both the Timeout Enable FF and the Timeout Counter are reset to 0.

Also after the 515th sprocket pair, the SC and WC have counted back to zero, which condition resets the Core Address Adjust FF to 0.

To complete the performance of this instruction, the EBM must be sensed, tape motion stopped, and the Matrix path released.

Sensing of the EBM and setting of the 16 Reset FF occurs just as when sensing the BBM. At ϕ1 time, after the 16 Reset FF is set, gates 35 and 37 [F-20] will be active to generate an "EBMT 1" signal. This signal tests the Full BM Not Received FF [D-23] for a Format Error during sensing of the EBM. During ϕ2 time, the OC and Block Mark FF are reset as before. The Block/Gap FF is stepped back to the 0 state.

At ϕ3 time, the OC is stepped (to 1's) and an attempt is made to set the Stop FF [D-6] to 1. Note that this flipflop will be set if the Stop At End of Block FF [E-29] is in the 1 state. Since gate 117 [A-27]has been active from the time the NBP Register was counted down, the Stop at EOB FF will be held in the 1 state via gate 119.

Setting of the Stop FF allows OC to begin counting again; and at the ϕ0 time after a count of 68 is reached, gates 26 and 27 [F-11] are active to reset the Forward Hold FF. When this occurs, tape is no longer being moved by the transport. The OC provided a delay of 3 MS between reading the EBM and stopping tape motion. This allowed the read heads to be approximately centered in the inter-block gap in case the next operation requires reverse reading.

The OC continues counting after the Forward Hold FF is reset, and, at the $\phi 0$ time following a count of 104, a "Finis" signal is generated via gates 26 and 28 [F-11] .

"Finis" turns the AUT Reset FF on again (gate 19) which results in the Stop FF being reset to 0 (at $\phi 2$). OC is also reset as usual. Note that when the Stop FF is reset, gate 12 [G-10] becomes inactive returning the AU to non-run status.

The "Finis" pulse also strobes gate 132 [W-9] which will have an active output, since it is assumed that no errors have occurred. The output of gate 132 fires the Release Matrix SS [W-14] via gate 136. This SS provides a reset for all Path FF's (in the Matrix) associated with this AU (Of course, only one Path FF in this group was set.)

Resetting the Path FF's returns the AU to non-busy status.

Between resetting the Forward Hold FF (at OC = 68) and generating the "Finis" Signal (at OC = 128), approximately 2.7 MS elapsed. This delay ensures that complete mechanical stopping of tape has been accomplished prior to returning the AU to non-run and non-busy status.

Reading More Than One Block Without Spacing (no errors)

When more than one block must be read (by a single TIO instruction) the first block is treated as when reading a single block until the second time the 16 Reset FF is set.

At this time, which follows sensing of the EBM, the Stop at EOB FF [E-29] will not be set. (Since the NBP Register has not counted down to 0, gates 117 and 119 could not become active.) Thus, the Stop FF will not be set, the Forward Hold FF will not be reset, and the "Finis" signal will not be generated. This means that tape motion continues and the AU remains in run and busy status.

Reading of the second, and subsequent, blocks is similar to the first, except that the start FF will not be set prior to processing these blocks.

When the final block is being processed, the NBP Register will be counted to 0; and stopping will occur, under influence of the Stop at EOB FF, as previously described.

Reading 16 Block (no error)

Reading of 16 blocks occurs if the NBP and NBS fields of the "D" Register are both 0 when a read order is begun. This occurs as follows:

Reading of the first block begins before any interrogation of the NBP or NBS registers is made. While reading this block, the NBP Register is rippled from 0 to 15, thereby deconditioning gate 117 [A-27].

Since gate 117, and hence gate 119, had been active prior to this count down of NBP, the Stop at EOB FF will be set to 1. When "EBMT 1" is generated, however, gates 164 and 122 [C-31] will be active to reset the Stop at EOB FF via gates 124 and 163. Thus, the Stop FF cannot be set by the following $\phi 3$ pulse. The AU now must process 15 more blocks (the number now in the NBP Register) before stopping.

Note that resetting of the Stop at EOB FF by the "EBMT 1" signal is attempted even when stopping must occur (i.e. - when NBP has been counted to 0 by the current block). In this case, however, gate 119 has an active output after the "EBMT 1" signal subsides. This restores the Stop at EOB FF to the 1 state in time for the Stop FF to be set by ϕ 3.

Spacing Before Reading

The case considered here is when the NBS field of "D" is not 0 when a read order is begun (the Man. Read Forward FF = 0). The Start FF is set as during a read without spacing; but when OC reaches a count of 3, the Space FF [X-20] is set via gates 145 [V-18] and 147. All other activity while the Start FF is on, and while sensing the BBM is similar to a read without spacing.

Sensing of the first sprocket initiates, as usual, the timing sequence ST 1, ST2, and ST3. Note that gates 70 through 73, strobed by ST 1, cannot have active outputs while the Space FF is set to 1. Note, too that gates 84, 85, and 86, strobed at ST2 time, cannot become active since gate 80 is inhibited by the Space FF.

Thus, while spacing, no shifting or transferring of the SBR occurs nor is information gated from the MBR into the SBR. Parity checks are made on the contents of the MBR as usual, and the MBR is gated to the Write Counters for channel parity checking. If a parity error (either character or channel) is detected, the Space Error FF, rather than the Parity Error FF, will be set. Refer to Figure 4-2 for the setting of these FF's.

While spacing, the 3 Frame Delay Counter is stepped as usual, and gate 153 [W-24] becomes active at the proper time. This results in gate 154 becoming active to count down NBS.

When the EBM is sensed, the "EBMT 1" signal will reset the Space FF (via gates 149 and 150) if NBS were counted down to 0 during the block. Stopping of tape may now be initiated (if NBP is set to 0). or the reading phase of the instruction may begin (NBP $\neq$ 0).

If the Space FF is not reset by the "EBMT 1" signal, the AU proceeds to space over the next block.

Reverse Reading (no errors)

Reading in the reverse direction is similar to reading forward, with the following exceptions:

1) The Block Marks which were written as EBM's are sensed as BBM's (and vice-versa).

2) The Reverse FF is set in the Command Register instead of the Forward FF.

3) The Reverse Hold FF is set (via the lower leg of gate 10 [E-6]) instead of the Forward Hold FF.

4) Information transferred from the MBR to the SBR (at ST2 time) goes to Stage 1 instead of Stage 4 (gate 86 [N-16]).

5) Shifting of the SBR (at ST 1 time) is to the right instead of to the left (gate 71 [N-7]).

8. LOGIC OF WRITE WITHOUT ERROR

Writing One Block Without Spacing (no errors)

This discussion assumes familiarity with the reading process previously described. The initial assumptions are the same as when reading, except that the Write FF is set in the Command Register instead of the Read FF. References in this chapter are to Figure 7-1 and the Write Timing Diagram (Figure 8-1).

Prior to the sensing of the BBM, all activity which occurred while reading occurs during writing. Note that Y start (Gate 2) clears the Sprocket Counters to ensure pre-sprocket flux consistent with that of freshly edited tape. In addition, when the Read Enable FF is set (via gate 6 [G-3]), the Write Enable FF is also set (via gates 8 and 9).

This FF allows the output of the Write Counters to be sensed by the Write Amplifiers (in the transport) and hence for magnetization of the tape to occur. The Write Enable FF also allows the writing of sprockets in the channel which does not contain block marks.

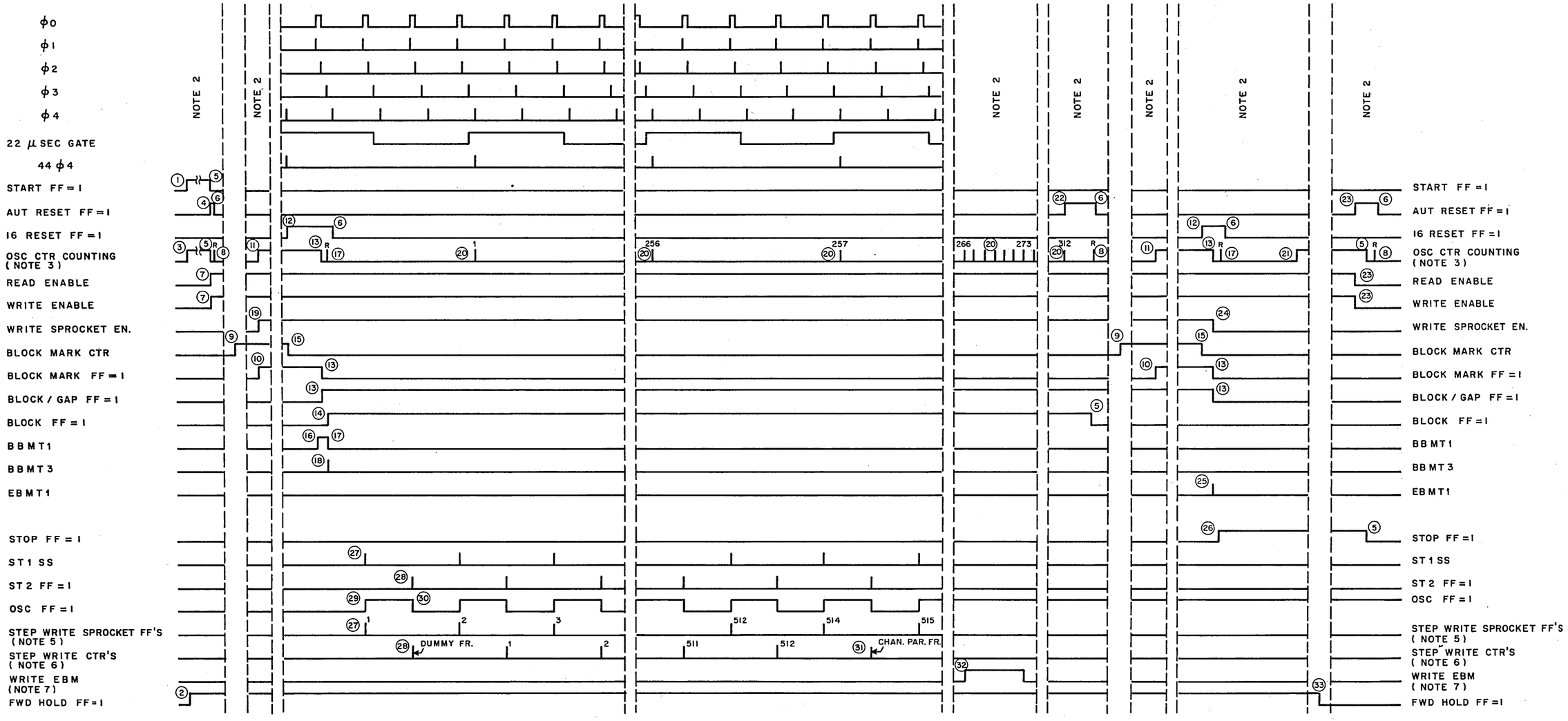
Simultaneous with the setting of the Block Mark FF, the Write Sprocket Enable FF [G-23] is set via gate 41. This FF allows the writing of sprockets in the channel containing Block Marks. Note that the Write Sprocket Enable FF was not set until the write heads were beyond the BBM; this is necessary to prevent erasure of the BBM. Furthermore, erasure in the block mark channel occurs when the block mark is sensed or before the Block FF is set, which initiates the writing of new sprockets.

Activity during the "BBMT 1" signal is similar to that when reading. However, during the "BBMT 3" pulse, several things occur which did not occur when reading.

1) The Shift FF [S-16] is set to 1 via gates 168 and 169.

2) STC [S-14] is set to 2 via gate 103.

3) A memory request is made via Gate 172 [N-10] to preload the WBR (cleared by Y Start, Gate 2) with the first word to be written in the block.



(1) LN02 · Stop Order · Release Order
(2) Start FF = 1 · Fwd FF = 1
(3) Start FF = 1 · 44Ø4
(4) Start FF = 1 · OC = 32
(5) AUT Reset FF = 1 · Ø2
(6) Ø4
(7) Start FF = 1 · AUT Reset FF = 1
(8) AUT Reset FF = 1·Ø3
(9) BM Pulses
(10) BM CTR = 8
(11) BM FF = 1 · 44Ø4
(12) BM FF = 1 · OC = 8
(13) 16 Reset FF = 1 · Ø2
(14) 16 Reset FF = 1 · Block/Gap FF = 1 · Ø3
(15) 16 Reset FF = 1
(16) 16 Reset FF = 1 · Block/Gap FF = O · Ø1
(17) 16 Reset FF = 1 · Ø3
(18) 16 Reset FF = 1 · Block FF = 1 · Ø3
(19) Write FF = 1 · Space FF = O · BM CTR = 8
(20) Block FF = 1 · 44Ø4
(21) Stop FF = 1 · 44Ø4
(22) Write FF = 1 · Block FF = 1 · OC = 312
(23) Stop FF = 1 · OC = 104 · ØO
(24) EBMT1
(25) 16 Reset FF = 1 · Block/Gap FF = 1 · Ø1
(26) Stop at EOB FF = 1 · Block/Gap FF = O · 16 Reset FF = 1 · Ø3
(27) OSC FF = 1 · Ø1 (and others)
(28) OSC FF = O · Ø1 (and others)
(29) ST1 · Ø1
(30) ST2
(31) OC = 257 · Ø1
(32) OC = 266 thru 273 · Ø1
(33) Stop FF = 1 · OC = 48·ØO

Notes:

1) Time scale varies from section to section.
2) Top 6 signals are only shown in large scale area. They are present continuously.
3) Number above pulse indicates No. of counts rather than contents. "R" indicates ripple to ones.
4) Logical equations shown do not always indicate all conditions.
5) Gate 158 on Figure 7-1
6) Gate 157 or 156 on Figure 7-1
7) Gate 59 on Figure 7-1

Figure 8-1 Write Timing

Actual writing begins when the Block FF is set. (This FF is set during 16 Reset time, as when reading.) At this point it may be helpful to state the operations which must occur while writing the block. These are:

1) 515 pairs of sprockets must be written.

2) A dummy frame, consisting of 2 BCD zeroes with parity bits, must be written between the 1st. and 2nd pairs of sprockets.

3) 512 information frames must be interlaced among the 2nd through 514th sprocket pairs.

4) A channel parity frame must be written between the 514th and 515th sprocket pairs.

Throughout the following discussion, reference should be made to Figure 8-1.

At the first ϕ 1 time following the set of the Block FF to 1, the output of gate 55 [T-2] is active. (OC8 = 1 at this time since OC has been reset.) This output strobes gates 157 and 158. Note that BBMT 1 set the OSC FF to 0; hence the output of gate 158 is active at this time. The even Sprocket Write FF [X-6] is stepped by this output while the odd Sprocket Write FF [W-6] is stepped by the output of gate 61. Also, both ST 1 SS's [K-4] are fired.

Stepping of the Sprocket Write FF's resulted in writing the 1st. sprocket pair. (The Sprocket Write FF's cause writing in the same way as the Write Counters do).

When ST 1 is fired, the output of gate 70 will be active since the Shift FF was set to 1 and STC set to 2, at BBMT 3 time. Shifting left of SBR is thus performed, but this action has no real effect since SBR was reset by BBMT 1.

Also, during ST 1 time, the OSC FF is set to 1 via gate 56 [T-3] . This setting signal comes from the ST 1 associated with the odd characters (i.e. - ST 1 T2). Gate 56 is conditioned by ϕ 1 to ensure that gates 157 and 158 cannot both have active outputs during the same ϕ 1 pulse.

Note that ST 1 does not set the ST2 FF when writing.

Upon arrival of the next $\phi 1$ signal, gate 157 is active (via gates 55, 53, and 52) to condition gate 159 [V-2] . Gate 156 [V-1]is inactive at this time, so Stage 1 of SBR is gated to the Write Counters to write the first frame. Since SBR is reset, the proper conditions exist for writing the dummy frame. Writing takes place by frames (in contrast to reading which occurs by characters) since skew is no problem.

Concurrent with the writing of the dummy frame, the ST2 FF is turned on via gate 78 [K-14] . When gate 78 becomes inactive (i.e - when $\phi 1$ subsides) the output of gate 105 becomes active, resulting in an active output from gate 88 [N-18] . Thus, STC is stepped from 2 to 3 via gate 104.

When ST2 is reset (by the delayed output of gate 105), the output of gate 162 [N-15] undergoes a change from active to inactive. This fires the Reset SBR SS [F-26] which in turn partially conditions gate 115. Since STC is now set to 3, gate 115 will be active to reset SBR via gate 116. This action is superfluous at present since SBR is already reset. Subsequent outputs from gate 115 will, however, prepare SBR to accept a new word from WBR.

In addition to the foregoing action, the OSC FF was set back to the 0 state by the outputs of gate 105. Hence, the following $\phi 1$ pulse can write the second sprocket pair.

The ST 1 SS is again fired while writing the sprocket pair, and gate 73 [N-9] has an active output (since STC is now set to 3.) This allows the contents of WBR (the word obtained by early memory request) to be transferred to SBR, thus putting the first frame of information in position to be written. As before, OSC FF is set to 1 by ST 1 SS.

Writing of the first information frame takes place during the next ϕ 1 time, and as before, gate 105 becomes active when $\phi 1$ subsides. STC is counted from 3 to 0, so that when the Reset SBR SS is fired, gate 115 [G-27] is inhibited.

During the next ST 1 time (while the 3rd sprocket pair is being written) gate 70 becomes active to shift the second information frame into position for writing (i.e. - into Stage 1).

The foregoing establishes the pattern for writing the block. Each time STC reaches a count of 3, SBR is cleared (by the SBR Reset SS) and a new word is transferred from WBR to SBR.

It must now be shown that the proper number of frames and sprocket pairs are written.

When the Block FF was set to 1, 44 $\phi 4$ pulses began stepping OC via gates 16 and 17. Note that an "End Block Delay" Signal is not generated via gates 112 and 114 [G-15] (as when reading), but must wait until OC reaches a count of 312 (i.e. - when gate 111 is satisfied).

To see how OC controls writing, refer to gate 52 [R-1] . The left leg of this gate is active (and thus enables writing via gates 53 and 55) until OC reaches a count of 256. During the time OC is set to 256, gate 52 is maintained active via gate 51 and the upper leg of gate 50. When OC is stepped to 257, gate 52 is kept active for 22 μ s via gate 51 and the lower leg of gate 50. Reference to Figure 8-1 will help to clarify the timing sequence.

Writing of the block was accomplished as follows:

1) Before the first OC count, the first 2 sprocket pairs and the dummy frame were written.

2) Before each subsequent OC count (up to a count of 257) 2 sprocket pairs and 2 information frames were written. Thus, after the first OC count and before the 257th count, 512 sprocket pairs and 512 information frames were written.

3) In the first 22 μs after the 257th OC count, the channel parity frame and the final sprocket pair were written.

The channel parity frame is written, via gates 54 and 156, by the first $\phi 1$ after OC receives its 257th count. Returning the Write Counters to the initial setting resulted in writing a 1 in any channel which contained an odd number of 1's. Normal writing, via gate 159, is inhibited while writing the channel parity frame.

Note that transfers from WBR → SBR (and corresponding memory requests) are made when the 2nd, 6th, 10th, etc., sprockets are written. In accordance with the early memory request, exactly 128 transfers and 127 requests must be made within the block. A 129th transfer and request corresponding to sprocket 514 is inhibited by the right leg of gate 68. A 128th request corresponding to the 128th transfer (sprocket 510) is prevented by holding cleared the Core to Tape Request FF. Writing of the EBM begins when OC receives its 266th count. At this time gate 58 [T-4] has an active output (the center input is active) conditioning gate 59. Each ϕ 1 pulse which is now passed through gate 59 steps the odd Sprocket Write FF (i.e. - writes a 1 in the odd Sprocket channel). Note that the center leg of gate 58 is active during both the 266 and 267 counts of OC, the right leg is active during counts 268 through 271, and the left leg is active during counts 272 and 273. Thus the output of gate 58 remains active for 8 OC timings during which 32 ϕ1 pulses are sent through gate 59.

Consider the state of the Sprocket Write (odd) FF at this time. Before writing of this block began, the FF was in the 0 state because of the Y Start Clear. During the writing of this block the FF will have been stepped 547 times (515 times while writing sprocket pairs and 32 times while writing the EBM). Since this is an odd number, the FF will now be set to 1.

When OC received its 274th count, following the writing of the 32nd. EBM pulse, the left leg of gate 128 [U-6] became active. The next ϕ 1 pulse can now set the Sprocket Write (odd) FF to 0 and thereby write the 33rd. EBM pulse. Similarly, the clear will write a 1 in the other sprocket channel at this time because the Sprocket Write (even) FF had been upset exactly 515 times.

Note the interval between the last sprocket pair and the first EBM pulse. The 1st. EBM pulse is written by the 35th ϕ1 after the last sprocket pair is written. This is a time interval of 389 μ s and a distance (at 120 in/sec) of $\approx$ 0.047 in.

Throughout the preceding discussion ϕ 1 was mentioned as the pulse which controls writing (i.e. - it conditions gates 53, 59 and 128). However, in AU 2, ϕ 2 performs these functions (ϕ 1 is used in AU 1). The use of different write times for the AU's helps to reduce crosstalk in the Matrix.

The next activity occurs when OC receives its 312th count. (This is $\approx$ 1.67 ms after the 33rd. EBM pulse was written). Gate 111 [F-15] becomes active at this time, and makes the "End Block Delay" line active via gate 114. This, in turn, sets the AUT Reset FF to 1 via gates 34 and 19. Resetting of OC and the Block FF occurs during the time the AUT Reset FF is set.

At this point it may be shown that no writing can take place via gates 55 [T-2] and 59 [T-5] except that already described. Note that for gate 55 to be fully conditioned, gate 52 must have an active output. Remember that this output became inactive after the 22 μs count pulse subsided with OC set to 257. Gate 51 cannot have an active output again unless OC reaches a count of 320 (to make the right leg of the gate active), or is reset to 1's. Since OC was reset after a count of 312, the possibility of reaching a count of 320 was eliminated. After OC is stepped to 1's, ϕ 1 pulses will be gated through gate 53, but by this time the Block FF has been reset to 0 to inhibit gate 55.

A similar situation exists at gate 59. In order for gate 58 to condition gate 59 after OC is stepped to 274, a count of 330 must be reached. The reset of OC at a count of 312 prevents this.

Note that gates 54 [T-1] and 128 [T-6] have active outputs at frequent intervals other than those mentioned (always after those mentioned). These have no effect however since they merely apply resetting pulses to FF's which are already reset.

Note, too, the condition "AUT Reset FF = 0" on gates 55 and 59. This is important in AU's which use ϕ2 as the writing pulse. Since OC is being cleared to 0 at ϕ2 time, which may result in a spurious output from gates 52 or 58, gates 55 and 59 must be disconditioned through the indeterminate period.

Readback During a Write Operation

Reading back during a write operation differs from a straight read operation in the following ways:

1) The ST 1 and ST 2 timings cannot be used.

2) Transfer of information from the MBR to the SBR cannot take place.

3) Transfer of information from the MBR to the Write Counters (for channel parity checking) cannot occur.

4) Stepping of the STC during ST 4 time cannot occur.

Checking of the character in the MBR for character parity, counting of SC and WC, and sensing of the EBM must all occur during both read and write operations.

Sensing of the first sprocket by the read head, fires the ST 3 SS [K-22] via gate 91. When ST 3 is fired, gate 93 is partially conditioned. Since, however, the Error Set O.K. FF was reset to 0 by BBMT 1, this gate cannot have an active output. The ST 3 SS turns on the ST 4 FF via gate 98. (The usual test for sprocket error is made via gate 171).

Activity during ST 4 time is the same as for read operations, except that STC is not stepped.

When the ST 3 SS is fired by the next sprocket, gate 93 is fully conditioned, and the character parity test is made.

Operations involving the 3 Frame Delay Counter and the Timeout Counter are the same as when reading. Note that when writing, the WC contains a count of words remaining to be read back rather than the number of words still to be written. Note, too, that the test for channel parity is made (by the Timeout Counter) when writing. This test should find the Write Counters all reset due to writing the channel parity frame.

Sensing of the EBM and stopping of tape at the end of a block is accomplished as when reading. When writing, however, the Write Sprocket Enable FF is reset to 0 by the "EBMT 1" pulse (gates 42 and 167). The Write Enable FF is turned off by the "Finis" signal.

Writing More Than One Block Without Spacing (no error)

The conditions which result in reading more than one block also apply to writing. That is, if the Stop At EOB FF is not held set to 1 (due to NBP being set to 0), writing of another block occurs. Note that the Write Sprocket Enable FF is cleared by each EBMT 1 and is set again by the sense of the next block mark to avoid erasing the BBM.

Spacing Before Writing

Spacing prior to writing is similar to spacing before reading, except that the abbreviated readback cycle (using ST 3 and ST 4 timings) is used instead of the full read cycle (ST 1, ST 2, & ST 4). Hence channel parity is not tested while spacing prior to writing.

9. ERROR RETRYS

Automatic Reversals of Tape Motion

During error retrys and while the Erase and -1 Read orders are being performed, automatic reversals of tape motion must occur. (Automatic is meant to imply that the action occurs without further signals from CC or Multiplexer.) These reversals are achieved under control of the Pattern Counter (PC) and Change FF.

The PC is a 3 position counter which satisfies the condition PC = 0 when no tape motion reversals are required. Any quantity other than 0 in the PC indicates, in 8's complement form, the number of sequential motion reversals which may be required for a particular operation.

The Change FF provides an indication of whether motion should be in agreement with, or contrary to, the direction specified by the Forward and Reverse FF's

Consider the following example which illustrates the use of the PC and Change FF:

If a parity error is detected while executing a Read Forward, Mode 1 order, the tape must be backspaced and then reread in the forward direction. To achieve this the PC is set to 6 and the Change FF set to 0 when the error is detected. The PC setting indicates that two motion reversals are required, and the Change FF being in the 0 state indicates that the next tape movement must be contrary to the setting of the Forward and Reverse FF's (i.e., reverse motion must occur.)

Stopping at the end of the block and restarting for the backspace are initiated by the PC $\neq$ 0 condition.

During the backspace the PC is counted to 7 (indicating one more reversal needed) and the Change FF is stepped to the 1 state indicating that the next tape movement should agree with the setting of the Forward and Reverse FF's (i.e., forward motion must occur.)

Stopping and restarting are again effected by the condition PC $\neq$ 0.

While rereading, the PC is counted from 7 to 0 (since it is a 3 position counter), but the Change FF is left in the 1 state. (As will be seen, the setting of the Change FF at this point is immaterial.)

Since the PC has reached the 0 state, it can no longer influence tape motion. Whether or not the tape stops or continues at the end of the reread is determined by other circuits.

The detailed logic of some of the general aspects of PC and Change FF operation will be discussed in the remainder of this section. Activities peculiar to the various error retry situations and the -1 Read and Erase orders are discussed with those operations.

Refer to Figure 7-1. Note here how the condition PC $\neq$ 0 sets, and holds, the Stop at EOB FF [7-E-28] * to 1 via gate 119.

When the tape stops with the PC not set to 0, a "Finis" signal is generated and the AUT Reset FF is turned on as usual. During the ϕ3 time after the AUT Reset FF is turned on, gate 32 [7-C-2] is active to turn on the Start FF via gates 1 and 2. (The AU is in non-run status, as required by gate 2, since the Stop FF was reset at ϕ2.)

In operations discussed previously (i.e., Read or Write with no errors) gate 5 became active when the Start FF was Set. Now, however, since gate 33 has an active output, gate 5 is inhibited; and gate 3 or 4 will be active depending on status of the Change FF.

If the Change FF is in the 1 state, gate 4 is active to condition gate 7. This sets the Forward Hold FF or Reverse Hold FF in agreement with the settings of the Forward and Reverse FF's just as an active output from gate 5 did. Should the Change FF be in the 0 state when the Start FF is set, gate 3 is active to set the Hold FF's contrary to the Forward and Reverse FF settings.

Note that the LNO2 signal must be gone before setting of the Hold flip-flops can occur. This ensures that when a -1 Read or an Erase order is received, gate 33 will be active at the time of the set.

The conditions for stepping the PC are shown on Figure 4-2. A stepping pulse is provided from gate 108 at each BBMT1 time while gate 107

*NOTE: In this, and subsequent, sections references are frequently made both to Figure 4-2 and Figure 7-1. To simplify the text, the figures are referred to simply as [4-X-X] and [7-X-X] respectively when coordinates are specified. If a 2-position coordinate is given, the proper figure should be clear from the context. For convenience Figures 4-2 and 7-1 are repeated in this chapter.

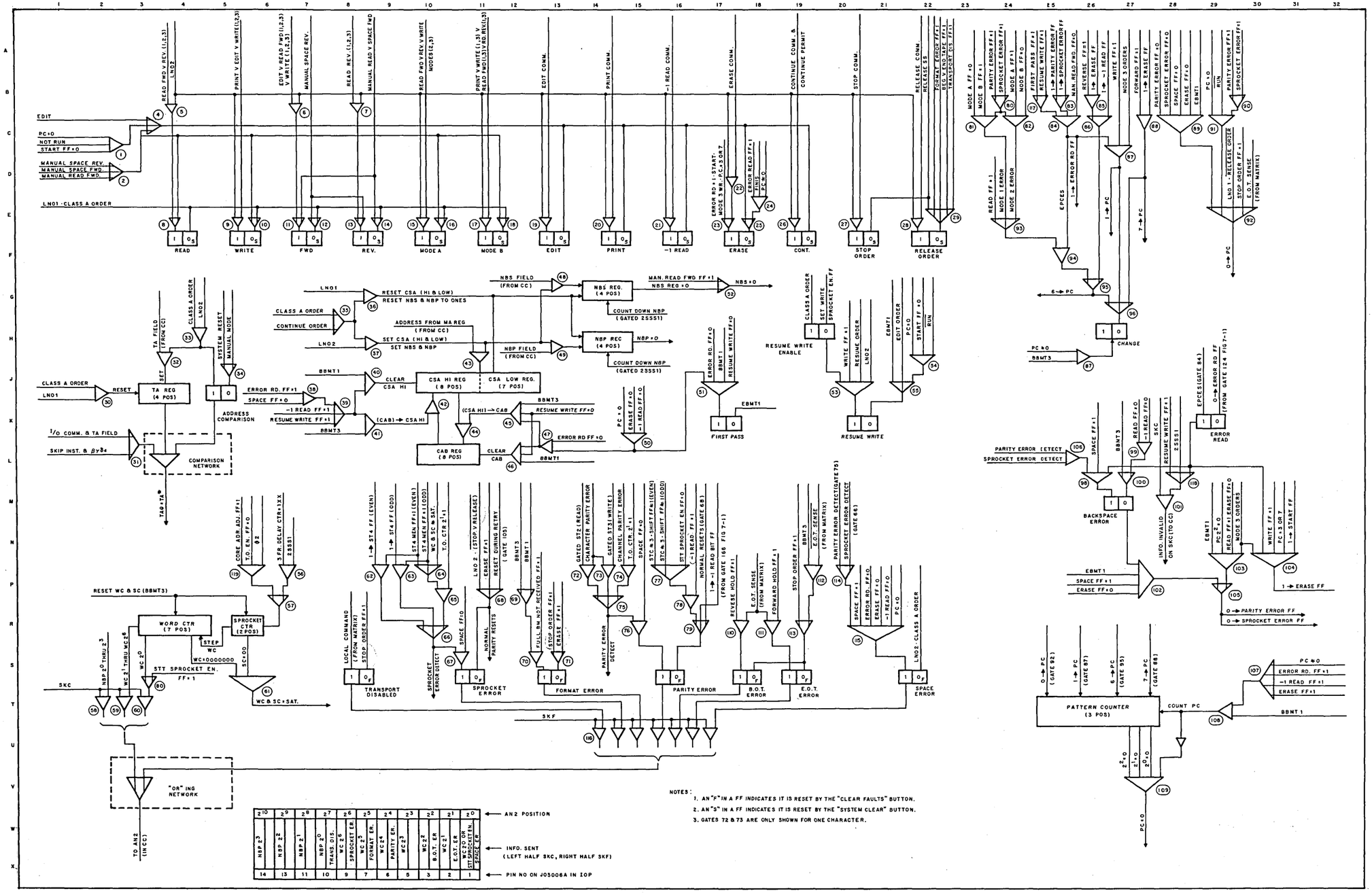


Figure 4-2 Control Registers & Misc. Execution Circuits

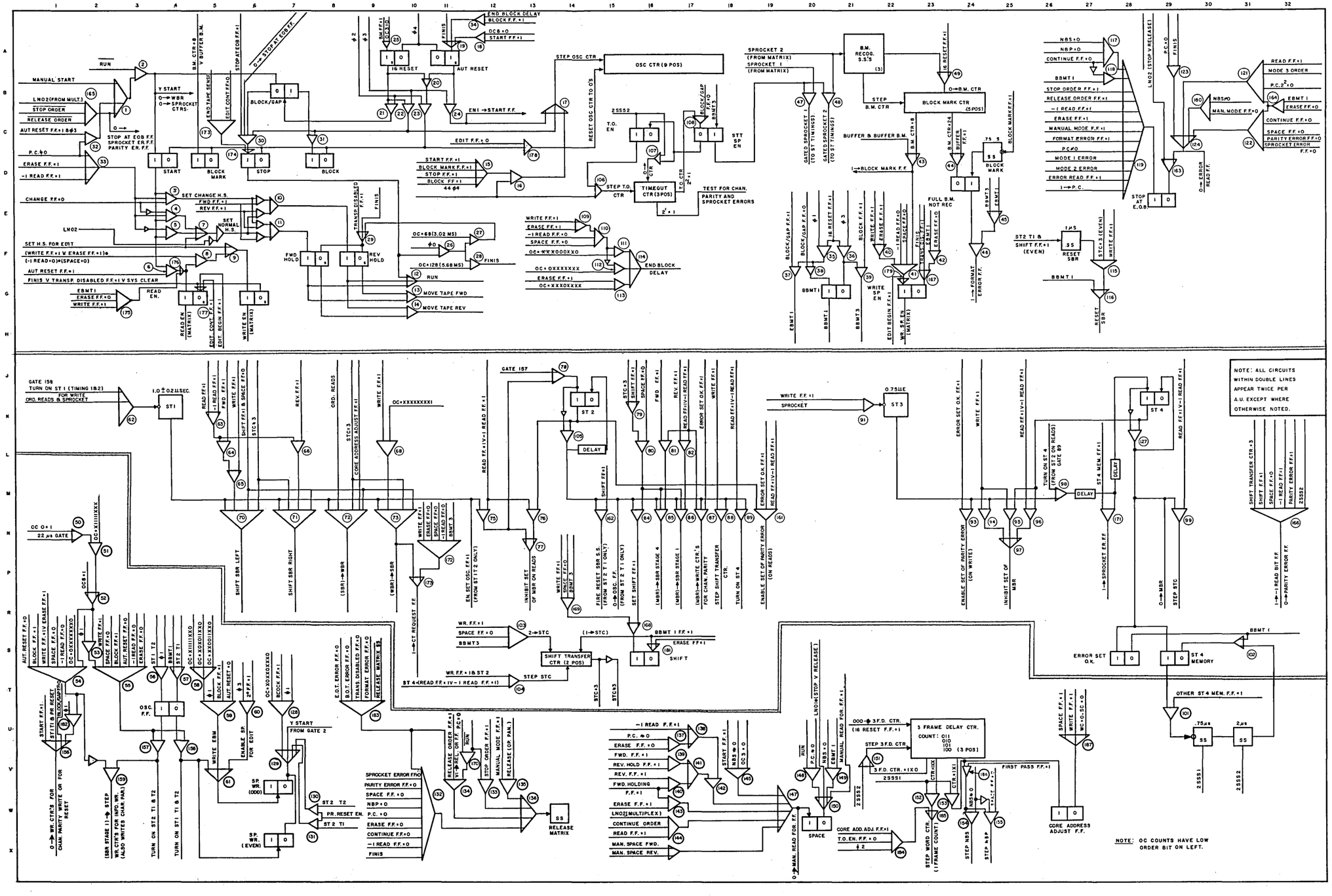


Figure 7-1 AU Execution Circuits

is made active by the condition PC≠0. Setting of the PC to 0, 1, 6, or 7 is discussed later.

Stepping of the Change FF [4-H-27] occurs at each BBMT3 time while the PC≠ 0 condition exists (gate 97). Note that the Change FF is set to 0, via gate 96, whenever the PC is set to 1, 6 or 7.

Read, Mode 1 or 2 Error Retry

If either the Parity Error FF [4-S-14] or Sprocket Error FF [4-S-10] is set while reading a block, a 6 → PC signal will be generated via gates 83 [4-B-25], 84, 94, and 95 (since the Read FF and the First Pass FF are both in the 1 state). Also, the Error Read FF [4-K-29] will be set to 1 by the output of gate 84.

Stopping of the tape at the end of the block occurs since PC≠ 0. Note that the attempted reset of the Stop at EOB FF during EBMT1 time (via gates 164 [7-C-31], 122, 124, and 163), which occurs during reading or writing without error, is now inhibited (at gate 122) by the Parity Error FF or Sprocket Error FF being set to 1. This is of no consequence to the Stop at EOB FF (which is maintained in the 1 state by PC≠ 0), but the 0 → Error Read FF signal (the output of gate 124) must not become active at this time.

Note also that the First Pass FF [4-K-17] is reset at EBMT1 time as usual.

As the "Finis" signal is generated, the following conditions (among others) prevail:

1) The PC is set to 6.

2) The Change FF is set to 0 .

3) The Error Read FF is set to 1.

4) The Parity Error FF or the Sprocket Error FF (or both) are set to 1.

Following the "Finis" signal, tape motion is restarted by the PC≠0 condition as previously described. Motion is in direction opposite to the indication of the Forward and Reverse FF's; and the Space FF [7-X-20] is set as movement begins. (Gate 137 [7-U-16] and either gate 139 or 140 are

active; hence gates 138, 141, 142, and 147 are active to set the Space FF.) This action (tape movement contrary to the Forward and Reverse FF settings while the Space FF is set) is referred to as "backspacing ".

Backspacing over the block is similar to spacing prior to reading with the following exceptions;

(1) At BBMT1 time, the PC is stepped from 6 to 7. The CAB register is not cleared during BBMT1 time since gate 47 [4-L-13] is inhibited. Also, the First Pass FF is not set at BBMT1 time since gate 51 [4-K-17] is inhibited.

(2) At BBMT3 time, the Change FF is stepped back to the 1 state via gate 97 [4-H-26] . The CSA Hi Register is not transferred to the CAB Register.

(3) The NBP Register or NBS Register cannot be stepped since gate 186 [7-W-23] is inhibited by the First Pass FF.

(4) If a parity error or sprocket error is detected, the Space Error FF cannot be set since gate 115 [4-R-21] is inhibited by the Error Read FF, Instead, the Backspace Error FF [4-M-27] is set via gate 98.

(5) At EBMT1 time:

If no error was detected, and hence the Backspace Error FF is in the 0 state (to which it is set at every BBMT3 time) the Parity Error FF and Sprocket Error FF are reset via gates 102 [4-P-27] and 105. An attempt is made to reset the Space FF [7-X-20] via gates 149 and 150, but the FF is held to 1 via gates 142 and 147.

Note that gate 89 [4-C-28] is inhibited at this time by the Space FF, so the PC cannot be reset. Similarly, gate 122 [7-C-31] will not become active, even if the error FF's are reset during EBMT1, since the Space FF = 1; hence the Error Read FF cannot be reset via gate 124.

(6) Stopping at the end of the block occurs due to PC $\neq$ 0.

(7) When the AU goes to non-run status (as the Stop FF is turned off) the Space FF is reset via gates 148 and 150 [7-W-20] .

(Gate 142 became inactive when the Forward Hold and Reverse Hold FF's were reset, so the Space FF is no longer held to the 1 state.)

At "Finis" time, following the backspace, the following conditions prevail:

(1) The PC is set to 7.

(2) The Change FF is set to 1.

(3) The Error Read FF is set to 1.

(4) The Stop at EOB FF is set to 1.

(5) The Parity Error FF or Sprocket Error FF (or both) and the Backspace Error FF are set to 1 if an error was detected while backspacing; otherwise they are all set to 0.

Following "Finis" time, motion is initiated via gate 32 as before; except now the direction of motion corresponds to the setting of the Forward and Reverse FF's (since Change FF = 1). The Space FF is not set during this pass since gate 141 is not active.

Activity during this pass differs from the backspace in the following ways:

(1) During BBMT1 time, the PC is counted from 7 to 0; hence the Change FF cannot be stepped via gate 97 [4-H-26] (i.e, it remains set to 1.)

(2) The CSA Hi Register is cleared by BBMT1 and receives the contents of the CAB Register at BBMT3 time, since gates 40 and 41 [4-K-9] are active via gates 38 and 39.

(3) Transfer of information to CC tapes place since the Space FF is not set. If a parity error or sprocket error is detected, the corresponding error FF is set. (The PC and the Change FF cannot be set via gate 84 [4-C-25] since the First Pass FF is not set.)

(4) Resetting of the Parity Error FF and Sprocket Error FF cannot occur at EBMT1 since gate 102 [4-P-27] is inhibited by the Space FF.

(5) The usual attempt to reset the Stop at EOB FF and Error Read FF via gates 164, 122 and 124 [7-C-31] is made. If neither the Parity Error FF nor the Sprocket Error FF are in the 1 state, this attempt is successful, and the original order proceeds as though no error occurred. Should either error FF still be set, the tape will stop.

When the tape stops due to a recurrent error, restarting via gate 32 [7-C-2] cannot occur since the PC is now set to 0. Thus the order is terminated. During the last "Finis" time, when the order is terminated, the Stop at EOB and Error Read FF's are reset via gates 123 [7-A-29] and 124.

Read, Mode 3

The activity when an error occurs in this mode is similar to that which occurs in modes 1 and 2 with the following exceptions:

At EBMT1 time of the second read (not the backspace) gate 103 [4-N-29] is fully conditioned. This allows the Parity Error and Sprocket Error FF's to be reset (if on due to a recurrent error) via gate 105. Furthermore, gate 121 [3-B-31] is fully conditioned which allows the Stop at EOB FF and Error Read FF to be reset via gates 124 and 163. As in Mode 1 and 2 operation, resetting the Stop at EOB FF and Error Read FF allows the order to proceed as if no error occurred.

Write, Mode 1 or 2

When a character parity error or sprocket error is sensed during the readback portion of a write order, setting of the PC, change FF, and Error Read FF occurs as when reading.

A backspace operation is initiated which is similar to the read backspace except for the following:

1) The Backspace Error FF is maintained in the 0 state via gates 99 and 100 [4-L-27] causing the Parity Error and Sprocket Error FF's to be reset via gate 102 [4-P-27] regardless of the sensing of errors during the backspace.

2) The abbreviated read cycle, using ST3 and ST4, is used.

After backspacing, rewritting is attempted. During this rewrite the readback is again tested for errors and action is taken similar to that when reading (i.e., the order continues if no error is sensed, the order terminates otherwise).

Write, Mode 3

If a parity error or sprocket error is detected while writing in this mode, the PC is set to 1 via gate 87 [4-C-27]. The output of this gate also sets the Change FF to 0 via gate 96. Backspacing is performed as in a mode 1 or 2 write; the PC being stepped to 2 in the process. Rewriting is attempted as when writing in mode 1 or 2, except that the Change FF is stepped back to 0 at BBMT3 time (since the PC is stepped to 3 at BBMT1 time.)

Should the rewrite be successful, the PC is reset to 0 via gates 89 and 92 [4-C-28] at EBMT1 time. In this case the Stop at EOB FF, after being reset via gate 122 [7-C-31], cannot be returned to the 1 state.

When the rewrite is unsuccessful, the tape stops at the end of the block with the PC set to 3 and the Change FF set to 0.

Following the "Finis" signal, the Start FF is set again via gates 32, 1 and 2 [7-C-2]. This initiates motion in the reverse direction (as when backspacing). At this time, erasing of the block occurs, rather than spacing.

The Erase FF [4-F-17] is set to 1, via gate 104 [4-N-30], concurrent with setting the Start FF. Refer to the description of the Erase order for the activity while erasing. As the block is being erased, the PC is stepped to 4, the Change FF is stepped to 1, and the Parity Error FF and Sprocket Error FF are reset.

When erasure is complete, the tape stops, a "Finis" signal is generated, and motion is again initiated in the forward direction via gates 32, 1 and 2.

During the "Finis" signal, the Erase FF was reset via gates 24 and 25 [4-E-18].

Rewriting is now attempted in the next sequential block to the one erased (since this is the first block sensed during forward motion). The

mechanics of the rewrite are similar to the previous rewrite, except the PC is stepped to 5 in the process.

Successful writing, as before, results in the PC being reset to 0 and the order continued as though no error occurred.

If, however, the error persists, a backspace and another write attempt are made. These operations are similar to the corresponding operations on the first block, except the PC is stepped to 6 and 7 during the backspace and rewrite, respectively.

Again, successful rewriting allows resetting of the PC and continuance of the order.

Should the error still persist, the block is erased while moving tape in reverse. This erasure is similar to the erasure of the first block; the PC being stepped to 0 in the process. The order is terminated following this erasure, since gate 32 [7-C-2] is inhibited.

Note that during each attempted rewrite, the contents of the CAB Register are placed in the CSA Hi Register since gate 38 [4-K-7] is active. Thus all writing is done from the same group of Core Memory Locations.

It is interesting to note also, that if any of the attempted rewrites are successful, allowing the order to proceed, the Change FF is left in the 0 state. This is of no consequence since the Change FF is only effective when the PC$\neq$ 0 condition exists (i.e., when the output of gate 33 [7-D-2] is active).

Status of the Matrix Following Errors

It has been mentioned how firing of the Release Matrix SS [7-W-13] (via gates 132 and 136) releases the Matrix following Class A orders which are terminated without error. Gate 132 is inhibited, however, if any error condition (except Space Error) exists when the "Finis" signal is generated Note, also, that if the PC $\neq$0 condition exists, gate 132 is inhibited. Thus releasing of the Matrix cannot occur during retry operations (unless the error is corrected.)

Other inhibits on gate 132 are discussed with descriptions of the -1 Read, Erase, and Continue orders.

10. LOGIC OF CLASS C ORDERS

The -1 Read Order (Command Field Coding 1100 1101)

Before executing this order, the Read FF and either the Forward or Reverse FF should be set in the Command Reg of the assigned A. U. Upon receipt of the "LN02" signal from the Multiplexer the -1 Read FF [4-F-16] is set to 1 via gate 21. Concurrent with the setting of the -1 Read FF, the PC is set to 6 via gates 86 and 95 [4-C-26]. The output of gate 95 also sets the Change FF to 0 via gate 96.

Setting of the Start FF occurs via gates 165, 1 and 2 [7-B-2] as with Class A orders. Since gate 33 [7-D-2] is active (PC≠ 0) and the Change FF is set to 0, tape motion is initiated in a direction opposite to that indicated by the Forward and Reverse FF's. When the appropriate Hold FF is set, the Space FF [7-X-20] is also set via gates 142 and 147.

While the tape is backspacing, the PC is counted to 7 and the Change FF is stepped to 1. Since gate 50 [4-L-15] is inhibited, the First Pass FF cannot be set, nor can the CAB Reg be loaded from the CSA Hi Reg. However, the CAB Reg is gated to the CSA Hi Reg since gate 39 [4-K-7] is active. Counting of the NBP Reg via gates 186 and 155 [7-W-24] is inhibited by the First Pass FF. In other respects this backspace is similar to spacing before reading Class A. Note that the Parity Error and Sprocket Error FF's are reset at EBMT1 time via gates 102 and 105 [4-P-28].

Since the PC≠ 0 condition exists, tape motion stops at the end of the block. The Space FF is reset at this time via gates 148 and 150 [7-W-20].

Tape motion is restarted in the direction indicated by the Forward and Reverse FF's since PC≠ 0 and the Change FF is in the 1 state.

As when backspacing, the CAB register is gated to the CSA Hi Reg. This allows the same Core Memory locations to be accessed during the -1 Read order as were accessed by the block read by the original order.

The PC is stepped to 0 at BBMT1 time.

Reading of the block into Core Memory now proceeds as when reading Class A except for the following:

The Parity Error FF is maintained in the 0 state (via gates 77 [4-P-16] 78, 79,) until both STC's reach a count of 3. This cancels parity errors detected in the dummy frame (during forward reads) or the channel parity frame (during reverse reads). Only errors in the information frames are relevant to the -1 Read order. Before the STC's are counted from 3 to 0, the Shift FF is set to 1, thus preventing further activity of the leftmost two legs of gate 77 for the remainder of the block .

Now, following each ST timing cycle during which the SBR becomes full (i.e., - the cycles in which the STC is stepped to 3) , gate 166 [7-M-32] is fully conditioned, at 2SSS2 time, if the Parity Error FF is in the 1 state. An active output from this gate resets the Parity Error FF (gate 79 [4-S-16]) and sets the -1 Read Bit FF to 1 (Figure 4-1 [B-16]).

Referring to Figure 4-1, note that the -1 Read Bit FF provides a reset to the WBR via gate 11 [C-15]. Furthermore, gate 10 [A-13] is partially conditioned while gate 7 is inhibited. Thus when the "(WBR) → IOB (AU1)" signal arrives, gate 6 (which represents 48 similar gates, one for each bit position) will only be active in the 2^0 position. This allows the number "-1" (in 2's compliment form) to be sent to the Memory via gate 8. Upon completion of the (WBR) → IOB transfer, the -1 Read Bit FF is reset by the "Count CSA Reg". signal.

More detail on the generation of the "(WBR)→ IOB (AU 1)" and "Count CSA Reg" signals is given in the chapter on Memory Access Multiplexing.

The foregoing procedure can occur as many times as necessary while processing the block.

Stopping occurs at the end of the block since gate 119 [7-C-28] is conditioned by the -1 Read FF. When the tape stops, the -1 Read FF is reset via gates 1 and 4 [4-C-2] . The Matrix is not released after a -1 Reade order since gate 132 [7-V-9] is inhibited by the-1 Read FF. (Note that the -1 Read FF is not reset until the $\phi 2$ time following the "Finis" signal.)

When the -1 Read order terminates, the Parity Error FF is in the 0 state since it was reset (via gates 77 [4-P-16] , 78 and 79, when the STT Sprocket Enable FF was returned to the 0 state by the Timeout Ctr. Note that channel parity errors and character parity errors in the channel parity frame (the dummy frame on reverse reads) are canceled by this reset. However, a Sprocket Error indication, if generated, is retained.

The Erase Order (Command Field coding 11 00 1110)

The Erase order causes the block marks and sprockets (and usually the information channels) of the erased block to be eliminated.

Erasing must take place while tape is moving in reverse in order for the read heads to recognize the EBM before it is erased. Because of this, and since erasure is always performed on the last block processed, the operation is different following forward and reverse orders.

When erasing follows forward orders, simply moving the tape one block in the reverse direction, with the Write Enable and Write Sprocket Enable FF's set, will give the required effect.

Upon receipt of the LN02 signal from the Multiplexer, the Erase FF is set via gates 22 and 23 [4-E-17], the PC is set to 7 via gate 88 [4-C-28], the Change FF is set to 0 via gates 88 and 96, and the Start FF is set via gates 165, 1 and 2 [7-B-2].

After the Start FF is set, the Read Enable and Write Enable FF's are set via gates 6, 8 and 9 [7-G4]. Since gate 33 [7-D-2] is active, the Reverse Hold FF is set.

When the BBM is recognized, the Write Sprocket Enable FF is set via gate 41 [7-G-22].

At BBMT1 time, the CAB Reg. cannot be cleared, nor can the First Pass FF be set, due to gate 50 [4-L-15] being inhibited. Likewise, the CSA Hi Reg cannot be gated into the CAB Reg. at BBMT3 time. The CAB Reg. cannot be gated into the CSA Hi Reg. since gate 39 [4-K-8] is not active. (It is essential that neither the CSA Hi Reg. nor the CAB Reg. be altered while erasing since a subsequent order may require the information from either.)

From this point operation is basicly a read or write (as indicated by the Command Reg.) modified by the Erase FF being set.

Note that gate 55 [7-S-2] is inhibited by the Erase FF being in the 1 state. This is necessary to prevent writing via gates 157 and 158 [7-V-3] when erasing is done with the Write FF set to 1.

While erasing, the "End Block Delay" signal is generated from

gate 114 [7-G-16] via gate 113 after the eighth count of the OC (following the set of the Block FF). This signal, as usual, turns on the AUT Reset FF, which in turn allows the Block FF and the OC to be reset. It is important that the OC be reset before gate 58 [7-S-4] can become active since writing in the odd sprocket channel via gate 59, must not occur.

When erasing while the Read FF is set to 1, the Sprocket Write FF's [7-W-6] cannot be stepped because gates 55 and 59 are inhibited. Stepping of the Write Counters (and hence writing in the information channels) can occur, however, via gate 87 [7-N-17] at each ST2 time. Since no block marks are associated with this psuedo writing, it does not detract from the effectiveness of the erase.

Transfers from SBR to WBR, or from WBR to SBR, (generated by the output of gates 72 and 73 [7-N-8] must not be permitted during the erase, as this would allow core memory accesses. These transfers are inhibited by the Shift FF [7-S-16] being held in the 0 state via gate 181.

Stopping of tape at the end of the erased block occurs since the Erase FF conditions gate 119 [7-C-28]. The Erase FF is turned off via gates 1 [4-C-2], 4, and 25 when non-run status is reached. Note that the Matrix is not released since the Erase FF is still set at "Finis" time to inhibit gate 132 [7-N-9]. Note also that the Write Sprocket Enable FF is cleared by "Finis" rather than by EBMT1 (gates 42 and 167, [7-F-23]) to assure erasure of the End Block Mark.

During execution of the Erase order, the Sprocket Error, Parity Error, and Format Error FF's are reset, and held, to 0 via gates 68 [4-R-11], 79 [4-R-16], and 71 [4-S-13] respectively.

If the Reverse FF is set when an Erase order is given, the tape must be spaced in the forward direction (i.e., backspaced) one block before erasing.

When the "LN02" signal is received, the PC is set to 6 via gates 85, [4-C-26], 86, and 95; the output of gate 95 also setting the Change FF to 0 via gate 96. Setting of the Erase and Start FF's is the same as before.

As tape begins moving forward, the Space FF is set via gates 143 and 147 [7-W-17]. The PC is stepped to 7 at BBMT1 and the Change FF is counted to 1 at BBMT3. Setting of the Write Enable and Write Sprocket Enable FF's cannot be accomplished at this time since "Space FF= 0" is a condition on gate 8 [7-F-5] and gate 41 [7-F-22].

A transfer from CSA Hi Reg. to CAB Reg, or from CAB Reg. to CSA Hi Reg, is not possible since gates 50 [4-L-15] and 39 [4-K-8] are both inactive.

Tape motion stops after spacing one block since gate 119 [7-C-28] is conditioned. The Space FF is reset at this time (gate 148 [7-V-20]), but the Erase FF remains set since gate 1 [4-C-2] is inhibited by the PC setting.

Motion is reinitiated, following the backspace, via gate 32 [7-C-2], from which point erasing is similar to erasing following forward motion.

The Resume Order (Command Field coding 1000 1001)

Operation of this order differs somewhat depending on whether it follows a Read or a Write order.

If a Resume order is given following a Read order (i.e., while the Read FF is set to 1), the Start FF is set via gates 165 [7-B-2], 1, and 2. From this point, operation is the same as if a Read order had been given. No new information is placed in the Control Registers when the Resume order is accepted; these registers are used in whatever state they were left by the preceding Read order. (Except, possibly, the Fault Register which may have been modified by an intervening order. Also, acceptance of the Resume order provides a reset to the Parity Error and Sprocket Error FF's.)

If the NBP and NBS Registers both contain 0 when the Resume order is given (with Read FF = 1), 16 blocks will be read.

When a Resume order is given following a Write order (i.e., while the Write FF is set to 1), two situations are possible:

(1) If the original Write order did not write at least one block (that is, if only spacing occurred), the Resume Write Enable FF [4-H-19] will be in the 1 state. (An exception to this is noted in the next paragraph.)

(2) If actual writing did occur, this FF will be in the 0 state.

These situations result from the fact that the "Set Write Sprocket En. FF" signal (which also sets the Resume Write En. FF to 0) is only generated when actual writing is going to occur.

(Note: If an Erase order is interjected between a Write order which only spaces and a Resume order, the Resume Write En. FF will be in the 0 state when the Resume order is accepted. The ramifications of this atypical sequence are of concern only from the programming point of view.)

Case 1:

When the Resume Write En. FF is in the 1 state, operation of the Resume is similar to that which occurs following reading, (i.e., the Start FF is set, and subsequent activity is dictated by the existing settings of the Control Registers). In this case, if the NBP and NBS Registers both contain 0 when the Resume order is accepted, 16 blocks are written.

Case 2:

If the Resume Write Enable FF is in the 0 state when the Resume order is received, the Resume Write FF [4-K-20] is set to 1 via gate 53. This allows the CAB Register to be gated to the CSA Hi Register at BBMT3 time. (Gates 40 and 41 [4-K-8] are conditioned via gate 39, while gate 45 and 46 [4-K-12] are inhibited.) Furthermore, the First Pass FF cannot be set since gate 51 [4-J-17] is inhibited.

Because the CAB Register is transferred to the CSA Hi Register, writing in the first block is from the same Core Memory locations accessed by the last block of the original Write order. Since the First Pass FF inhibits gate 186 [7-V-24], the NBP Register is not counted down during the first block. Thus, the first block written following a Resume order (with Resume Write Enable FF = 0) is essentially a retry of the last block written by the original Write order.

The Resume Write FF is reset at EBMT1 time of the first block, from which point operation is the same as in Case 1. If the NBP and NBS Registers both contained 0 when the Resume order was accepted, only one block is processed.

Note that the Resume Write FF provides an active input to gate 117 [4-B-25] to allow the "EPCES" signal to be generated (and thus initiate error retrys) when parity or sprocket errors are detected in the first block.

11. LOGIC OF THE STOP AND RELEASE ORDERS

The Stop Order (Command Field coding 1111 1000)

Acceptance of the Stop order results in the Stop Order FF [4-F-22] being set at LN02 time. This FF does the following:

(1) Sets and holds the Stop at EOB FF to 0, via gate 119 [7-C-28].

(2) Sets and holds the PC to 0, via gate 92 [4-E-30].

(3) Sets and holds to 0, the Transport Disabled FF, the Format Error FF (gate 71 [4-S-13]), and the BOT Error and EOT Error FF's (gate 113, [4-S-19]).

Tape motion, if it exists when the Stop order is received, stops at the end of the block provided gate 180 [7-C-30] is inactive when gate 30 [7-C-6] is strobed. (Gate 180 is the only source of a "0 ⟶ Stop at EOB FF" * signal which can be active concurrent with the strobing of gate 30.) If the Stop order is received during the space portion of a previous order, gate 180 allows that portion to be completed before tape motion ceases. Acceptance of the Stop order cannot initiate tape motion since gate 165 [7-B-2] cannot be activated. Furthermore, automatic restarting of tape motion via gate 32 [7-C-2] cannot occur after the Stop FF is set, since the PC has been cleared to 0.

When non-run status is achieved (and, of course, this status may already exist when the Stop order arrives), the Release Matrix SS is fired via gates 133 [7-W-11] and 136. Firing of this SS, in addition to releasing the Matrix, resets the Stop Order FF.

Note that the Stop at EOB FF and the Error Read FF are reset at "Finis" time via gates 123 [7-B-29] and 124.

* Note: When a setting pulse is applied to both sides of a FF at the same time, the state of the FF is ambiguous (on the functional drawing only; not electrically). This ambiguity can be removed, when necessary (e.g., gate 30 [7-C-6]), by "artificially" making one of the setting pulses a condition along with the state of the FF.

The Release Order (Command Field coding 1100 1100)

Acceptance of the Release order causes the Release Order FF [4-F-22] to receive a setting pulse at LN02 time (gate 28).

Note, however, that if the Format Error, BOT Error, EOT Error, or Transport Disabled FF's are not all in the 0 state, or if the Release Matrix SS is firing, the Release Order FF is held in the 0 state via gate 29. In this case, the effect in the AU is the same as if the Release order had not been given. Furthermore, if gate 29 becomes active (except due to the Release Matrix SS) after the Release Order FF is set, the Release order is also effectively nullified.

Assuming that gate 29 is not active and setting of the Release Order FF occurs, the Stop at EOB FF [7-E-29] is set and held to 1 via gate 119. Hence, unless gate 180 [7-C-30] is also active, stopping of tape motion (if motion exists) will occur at the end of the current block.

Gate 180, as usual, allows the condition NBS = 0 to be satisfied before tape motion stops.

If the PC contains 0 when non-run status is reached, gate 134 [7-W-12] becomes active to fire the Release Matrix SS. In addition to releasing the Matrix, this SS resets the Release Order FF via gate 29 [4-E-22].

Should the PC not contain 0 when non-run status is achieved, gate 134 is inhibited, and restarting of tape motion via gate 32 [7-C-2] occurs. Thus, error retrys and the -1 Read and Erase orders are not interrupted by acceptance of a Release order.

Note that when a Release order is accepted while gate 29 [4-E-22] is active, gate 134 [7-W-12] is strobed by the "1 ⟶ Release Order FF"* signal even though the Release Order FF is never actually set to 1. If at this time the PC is set to 0 and the AU is in non-run status, the only inhibit on gate 134 is provided by gate 183 [7-T-8]. (Notice that the output of gate 183 is effectively the negated output of gate 29 [4-E-22].)

Acceptance of the Release order cannot initiate tape motion since gate 165 [7-B-2] is inhibited.

* Note: Refer to footnote on page 11-1.

12. CORE MEMORY ACCESSING AND MULTIPLEXING

In this chapter information transfers between the WBR's and Core Memory will be discussed.* For these memory accesses to be accomplished, the following steps are required:

1) The AU which requires the access must so inform the Multiplexer.

2) The Multiplexer notifies CC that an access is required.

3) CC informs the Multiplexer when core memory is available for accessing. It is possible that following Step 1, and before Step 3, other AU's have informed the Multiplexer of their need for a memory access. Before Step 3 occurs, the Multiplexer will have selected one AU to receive the coming access.

4) The Multiplexer starts the core memory timing chain. At this time the contents of the CSA Reg. of the selected AU are made available to CC to specify the core address to be accessed. If the selected AU is reading from tape, the contents of the WBR must be available to CC.

5) CC informs the Multiplexer that the IOB Reg. contains the word being transferred. If the selected AU is currently reading from tape, the IOB Reg. was loaded from the WBR; if writing on tape is taking place, the IOB Reg. was loaded from core memory.

6) The Multiplexer gates the contents of the IOB Reg. into the WBR of the selected AU (if writing on tape) or clears the WBR (if reading from tape). The CSA Reg. of the selected AU is incremented by one, and the indication that the AU requires a memory access is removed. As far as the selected AU is concerned the present access is complete. (Steps 1 and 2, requesting another access for a different AU, may already be accomplished at this time.)

7) In CC the contents of the IOB Reg. are placed in memory. If reading from tape is in progress, the word received from the WBR is now in memory; if writing, the word originally in memory is restored.

*Note: For a full understanding of the operations discussed in this chapter, some knowledge of CC organization relative to memory accessing is required. This can be obtained from the Central Computer Section of the TRANSAC Technical Manual, particularly Section 6.3.

8) The Core Memory Timing Chain completes its cycle indicating that memory is again available. If Steps 1 and 2 have already taken place (for another AU), Step 3 will now occur.

Memory Accessing While Reading

The details of obtaining a memory access while reading from tape will now be considered in detail.

Referring to Figure 12-1, which shows the accessing circuits for AU1, note how the T →C Req FF's (Even and ODD) [N-6] are set to 1 via gates 15 and 16. Gates 15 and 16 are the same gates which provide the "(SBR)→WBR" signals already discussed (Chapter 7). When both T →C Request FF's are set (i.e., when both halves of the SBR have been gated into the WBR), gate 20 becomes active and in turn makes gates 21, 27 and 28 active. The output of gate 28, "M. T. Request", is the signal to CC that an AU requires a memory access.

In CC the "M. T. Request" signal partially conditions gates 3 [B-10] and 6, while inhibiting gate 7. If memory is not presently assigned (i.e., if no access is in progress), gate 3 will be fully conditioned to reset the Assign FF to 0 via gate 4. Should a memory access be in progress, the resetting of the Assign FF to 0 must await generation of a MT 13 pulse from the Core Memory Timing Chain.

When the output of gate 4 becomes inactive (when the Assign FF leaves the 1 state or when the MT 13 signal subsides), gate 5 becomes active with the following effects:

1) Both the IOB and IOMA Registers are cleared to 0.

2) The M. T. FF is set to 1 via gate 6.

Now gate 8 is active, providing a "Mem. Assigned to M. T." signal to the IOP. This signal indicates that Core Memory is available for an access by the IOP.

In the IOP the "Mem. Assigned to M. T." signal partially conditions gate 19 [L-12]. The other condition on gate 19 (that gate 29 be active) will be present if the Multiplexer has selected AU1 for the present access. (It may be assumed, at present, that this is the case; the details of the multiplexing process will be covered later.) Gate 19 becoming active achieves

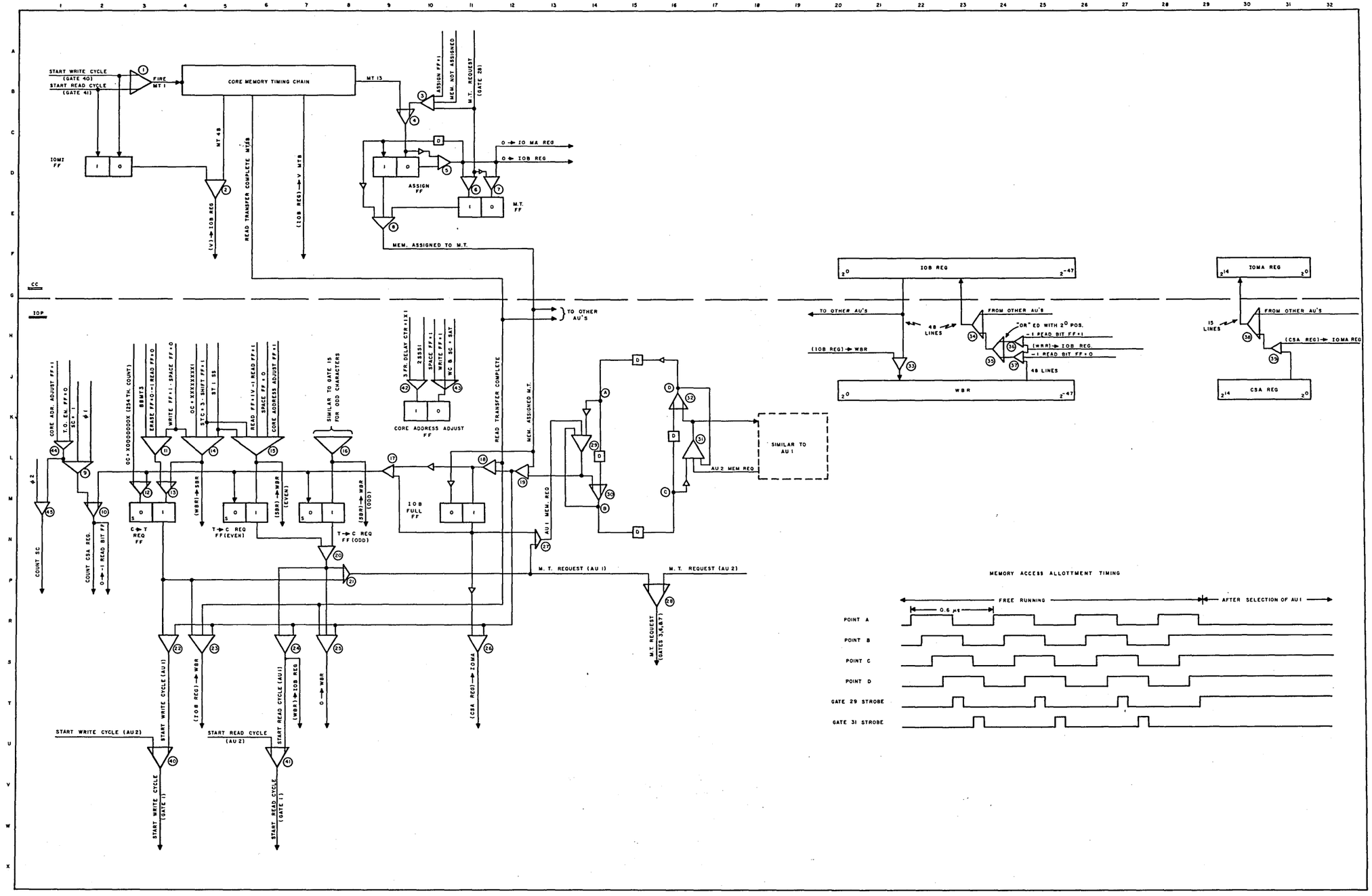


Figure 12-1 Core Memory Accessing and Multiplexing

the following:

1) The contents of the CSA Reg. are gated into the IOMA Reg via gates 26 [R-11], 39[H-31], and 38 since the IOB Full FF [N-10] is in the 0 state.

2) The contents of the WBR are gated into the IOB Reg. via gates 24[R-7], 37 [H-25], 35, and 34. (If the -1 Read Bit FF is in the 1 state, gate 36 is used instead of 37.)

3) A "Start Read Cycle" signal is sent to CC via gates 24 and 41.

Arrival of the "Start Read Cycle" signal in CC sets the IOMI FF [D-2] to 1. It also starts the Core Memory Timing Chain via gate 1.

At MT4B time, the readout of the required core memory address has occurred, thus leaving the address cleared. Note that the contents of the memory location cannot be placed in the IOB Reg. since gate 2 is inhibited.

During MT5B time the signal "Read Transfer Complete" is sent to the IOP where it sets the IOB Full FF [N-10] to 1 via gate 18 and resets the WBR via gate 25 [R-8]

When this "Read Transfer Complete" pulse subsides (it is a SS output) gate 17 [L-9] becomes active resetting the T → C Request FF's. The output of gate 17 also steps the CSA Reg. via gate 10[M-2] and resets the -1 Read Bit FF is necessary.

In CC the Core Memory Timing Chain proceeds to MT 8, at which time the contents of the IOB Reg are placed in memory. When the timing Chain reaches MT13 the Assign FF is again reset via gate 4.

Now, since gate 8 is inactive, the IOB Full FF is reset to 0. Note that the IOB Full FF had been maintaining gate 27 [N-13], and hence gate 29, active. As these gates become inactive the multiplexing circuits are freed to test AU2 for an access requirement.

Note that if AU2 initiates an access request (i.e., makes the right leg of gate 38 [p-16] active) before gate 5 [D-10] becomes inactive, the access will be granted immediately.

Memory Accessing While Writing

The process of memory accessing while writing on tape differs somewhat from the process just described for reading.

When AU1 requires a memory access, the C→T Req. FF [N-3] must be set via gate 13. Note that gate 13 can be made active in two ways:

1) Gate 14 becomes active during each (WBR) →SBR Signal (refer to Chapter 8). However, at the first (WBR) → SBR signal, the WBR must already contain the first word to be written. Hence, the first memory access in each block must be initiated by other means.

2) Gate 11 provides the first memory access of each block by setting the C→T Req. FF at BBMT3 time.

The C →T Req. FF, when set, provides a "M. T. Request" signal to CC and partially conditions gate 29 just as the T →C Req. FF's did while reading.

Activity in CC when the "M. T. Request" signal is received is identical to that which occurs while reading. That is, as soon as a memory access is available, the IOMA and IOB Registers are cleared and the "Mem. Assigned to M. T." signal is returned to the IOP.

Now, with gate 19 [M-12] active (the assumption is again made that gate 29 is active due to selection of AU1 by the multiplexing circuits), the contents of the CSA Reg are sent to the IOMA Reg (as when reading), and a "Start Write Cycle" signal is sent to CC via gates 22 [S-4] and 40.

In CC, receipt of the "Start Write Cycle" signal initiates the Core Memory Timing Chain via gate 1 [B-3] and sets the IOMI FF to 0. Now, at MT4B time the contents of the accessed core memory location are placed in the IOB Reg since gate 2 [D-5] is fully conditioned.

When the "Read Transfer Complete" signal is generated at MT5B time, the IOB Full FF [N-10] is set to 1 via gate 18 (as when reading) and the contents of the IOB Reg. are transferred to the WBR via gate 23 [S-5].

After the "Read Transfer Complete" signal subsides, gate 17 [L-9] becomes active to reset the C→T Req. FF (via gate 12) and count the CSA Reg. (via gate 10).

Remaining activity is the same as when reading. It is interesting to note that, so far as CC operation is concerned, the only difference between accessing memory while reading and while writing is the state of the IOMI FF [D-2] and its effect on gate 2.

Since, 129 setting pulses are applied to the C→T Req. FF in each block (1 via gate 11, and 128 via gate 14), the final set must not be allowed. The condition "OC= X0000000X" on gate 12, which is present during the last "(WBR)→SBR" signal (since the OC has made 254 counts at that time) provides the necessary inhibit.

Adjustment of the CSA Reg. While Reading

The Core Address Adjust FF [K-10] provides a "monitor" effect while reading which ensures the following:

1) That no more than 128 memory accesses per block can occur. This is necessary to prevent spurious modification of memory locations.

2) That the CSA Reg. is counted exactly 128 times during each block.

This is necessary for proper addressing of memory during subsequent reading.

That a special provision must be made to ensure these conditions results from the possiblity that more or less then 515 sprocket pairs may be recognized while reading a block (i.e., sprocket errors may occur.)

Note that the Core Address Adjust FF is set to 1, via gate 42, after the third sprocket pair is sensed. This is in time to condition gates 15 and 16 [L-5] when the first memory access is required (following the 7th sprockets.) The FF is reset when the WC and SC return to the original (i.e., satisfied) state; normally after 515 sprocket pairs are sensed. Since any sprockets which may be sensed after the 515th pair will find gates 15 and 16 inhibited, condition (1) is ensured.

If fewer than 515 sprocket pairs are sensed when the T.O. En.FF (refer to Fig. 7-1 [C-15]) returns to the 0 state, the SC and WC must be stepped artificially to the "satisfied" count. The T.O. En.FF will return to the 0 state whenever 2 consecutive sprockets, in the same channel, are not sensed. This FF being in the 0 state implies that the STT Sprocket En.FF is also set to 0. Hence no further ST timings can occur to provide stepping of the SC.

Counting of the SC after the T.O. En.FF is reset occurs at each $\phi 2$ time via gates 44[L-1] and 45. As soon as the "WC and SC = Sat" condition is met these counts stop since the Core Address Adjust FF is reset. Each time that the SC is counted to 1 (i.e., every 4th count), the CSA Reg is stepped by the following $\phi 1$ pulse. (The SC contains a count of 1 when normal stepping of the CSA Reg., following a memory access, occurs.) Thus condition (2) is ensured.

The adjustment of the WC and SC in the process of adjusting the CSA Reg. is incidental. Since the WC and SC are reset at each BBMT1 time, their status at the end of a block is immaterial. In fact during write and space operations the Core Address Adjust FF is held in the 0 state via gate 43 [J-11], so that counting of the SC via gate 45 cannot occur regardless of the state of the WC and SC after the T.O. En.FF is reset. No adjustment of the CSA Reg. is required while writing since memory accessing and hence counting of the CSA Reg. is controlled by highly reliable (since completely electrical) circuits rather than by sprockets sensed from tape. When spacing, of course, no memory accesses or counts of the CSA Reg. occur.

Note that adjustment of the CSA Reg. does not produce additional memory accesses. Thus, fewer than 128 accesses per block may occur.

The Multiplexing Process

It has been mentioned that when concurrent memory access requests are made from 2 or more AU's the Multiplexer must select one AU for the following access. Even when only one AU is making a request, selection must be made. For the means of accomplishing this selection, refer to the loop consisting of gates 29, 30, 31 and 32 [L-15]. (The discussion here will be confined to the multiplexing of 2 AU's; the introduction of more AU's would simply lengthen the loop.)

When neither AU is making a memory request, the center legs of gates 29 and 31 will be inactive, and the loop may be considered "free running".

While free running, activity in the loop is as shown in the timing diagram [P-26]. Consider the effect of point A becoming active:

After a short delay, point B becomes active via gate 30. Later point C is active, and still later point D. Point D becoming active results in point A, becoming inactive followed by points B, C, and D. The return of point D to inactive status allows point A to again become active. Thus a "wave of activity" is continuously circulating around the loop.

Now note the effect of the center leg of gate 29 becoming active due to a memory access request by AU1. As soon as point B is active while point A is inactive (shown as "Gate 29 Strobe" on the timing diagram), gate 29 is fully conditioned. At this time AU1 has been selected for the next access (the partial conditioning of gate 19 [M-13] reflects this selection).

Gate 29 becoming active allows point B to remain active, via gate 30, after the right leg of gate 30 has become inactive. Thus the loop is no longer free running, but is maintained in the state shown on the right portion of the timing diagram. Notice, in particular, that point C is active, thereby inhibiting gate 31 and the selection of AU2.

The memory access required by AU1 is now performed (as previously described) following which, gate 27 [N-13] becomes inactive. This allows gates 29 and 30, and hence point B, to become inactive.

Now, when point C becomes inactive, if the center leg of gate 31 is active, the selection of AU2 for an access will occur. If selection of AU2 does not occur, the loop returns to its free running state.

The "wave of activity" in the free running loop travels quite rapidly, having a period (in a 2 AU system) of .6 us. (The delays shown on the timing diagram between points A, B, C and D were assumed equal for simplicity, but will probably not actually be so.)

1. 3-3 Paragraph 5

During the recording of single blocks on magnetic tape, the block is not written if the end of tape is detected.

If the end of a tape is reached before a write order is completed, processing may be continued by initiating a Stop order or a Release, and a rewind. The Stop order, or any read or write order after the Release clears the End of Tape indicator.

In the case of a multiple block write, interrupted by the detection of the end of the tape, the old tape may be backspaced, according to the number of blocks written, before rewinding.

These blocks may be read back into memory, if necessary, and re-recorded on a new tape. The old tape may have control blocks written on it and the remaining blocks erased.

2. 3-3 Paragraph 5

When the end of a tape is reached, no error indications other than End of Tape or Transport Disabled are possible, if the tape is properly edited.

3. 3-3 Paragraph 2

In an error cycle of a read order, during the first pass in the opposite direction of the original order, a read takes place, but nothing is transmitted to memory. On the second pass in the original direction, a read into memory takes place.

4. 3-3 Paragraph 2

Error checks are made during all passes of an error cycle. Regardless of whether a parity or sprocket error is detected during back spacing, the information is transmitted to memory on the second pass in the original direction.

5. 3-10 Paragraph 1

A read forward mode 3 order is always successfully completed regardless of the event of parity or sprocket errors. At the completion of this order neither parity nor sprocket error indications remain. However, the case of a format error is different. Format errors without exception, will prevent the completion of the processing of any order. If a format error occurs during processing (Reading or Writing), the processing will be terminated at the end of the block during which the format error is detected. The processing of the

block will include any automatic re-read which may be initiated by the existence of parity and spreckel errors. If a format error is detected while spacing over blocks, the order will continue until the required number of blocks, specified in the order for spacing, have been spaced over.

6. 3-11 Paragraph 1

The time from the completion of data processing in a block to the sensing of the end block mark is still larger (3.5 milliseconds) for reverse reading than for forward reading (600 microseconds).

7. 3-13 Paragraph 3

The only indication one has if a mode 3 Write has been terminated due to the inability to clear up spreckel or parity errors is the fact that the Assembler is still indicated as busy. The two programs have removed the error indications. The number of blocks processed will not indicate that that block has been processed.

8. 3-17 Paragraph 2

In the event of an error occurring subsequent to the issuance of a Release order and before the end of that block has been reached, that block will continue to be processed, including any automatic retries, as is stipulated by the normal behaviour of the order. The assembler will not be released if the error is a Block Mark, Beginning of Tape, End of Tape, or Transport Disabled.

9. 3-17 Paragraph 2

The above situation illustrates a case whereby an input-output order, such as a Release, may be accepted, the TRD cause a skip, and still have the assembler not released due to some action caused by a former instruction.

10. 3-19 Paragraph 9

A rewind order is not accepted if:

a. A tape is currently rewinding
b. The rewind flip-flop is still set to 1
c. The tape unit is connected to an assembler.
d. The unit designated is not physically plugged in to the input-output processor.

11. 3-13 Paragraph 3

The programmer can only tell by deduction that a Mode 3 Write has failed, if a sprocket or parity error caused the failure. (See answer 7)

12. 3-18 Paragraph 4

In a system with more than one assembler, input-output orders may use the other assemblers while an Edit order is in progress with one assembler.

13. 3-18 Paragraph 3

If an assembler is in the midst of reading or writing when a Stop order is given, memory accessing continues for the remainder of the block.

14. 3-21 Paragraphs 3, 4, 5, 6.

If an address plug for either a Magnetic Tape unit or a Universal Buffer-Controller is not plugged in, a test of that Unit Availability register will find all four indicators set at 1.

INPUT-OUTPUT QUESTIONS

Question 1: In the advent of recording information on tapes and reaching the end of tape strip, what action must the program take to continue processing. Two situations may give rise to this condition. The first occurs when writing single blocks and the second occurs when writing multiple blocks. In the first case, the last (good) data block is recorded, and the next block is attempted to be recorded beyond the last recorded block mark. The second situation occurs when a multiple block order is given and several of the blocks are recorded (on good tape,) and the remaining blocks cannot be written because the end of tape strip is encountered. The question is: what can we do in each of these conditions to continue processing? For example, can a stop order be initiated and then a rewind? Or, can a release order be initiated, and then a rewind? In these cases, what clears the end-of-tape indicator? The final thought on this subject is, when reaching the end of tape, can the erase orders be given to erase the blocks recorded as part of a multiple first blocks of the multiple blocks write. Also, can we backspace several blocks, then read the blocks into memory so that they can be written on another tape, then erase these blocks,

and finally record sentinel blocks on a tape to indicate the end of tape? Finally, can these blocks be read in the reverse direction?

Question 2. Again referring to the situation of reaching end-of-tape while processing an order, how do the various errors leave us? Specifically, what is the reaction when processing the block during which time the end-of-tape indication is reached, in the case of parity error, sprocket error, format error?

Question 3. In an error cycle, which takes place during reading: is the first pass which is opposite to the direction of the original read, one of spacing or reading?

Question 4: During the last forward pass of an error cycle, when the error recurred during the backward spacing portion of the error cycle, is the forward operation one of reading or spacing?

Answer to question 4: (As interpreted by J. Stone)

In the event of parity or sprocket error during read, automatic retry is initiated. During the backspacing prior to a second attempt to read, the usual error checks are made; however, the information is not x transferred into memory. Regardless of whether an error is detected during backspacing, on the reread

attempt, information is transferred into memory.

Question 5: In reference to a read forward, mode 3 order, when a parity error is detected during the last block to be processed by the order: are the parity and sprocket flip-flops set or are they cleared by the order? Finally, is the matrix path released because the order was a mode 3 read?

Answer to question 5: (As interpreted by J. Stone)

A read forward mode 3 order is always successfully completed regardless of the event of parity or sprocket errors. At the completion of this order neither parity nor sprocket error indications remain. However, the case in the development of a format error is different. Format error without exception, will prevent the completion of the processing of any order. If a format error occurs during processing (Reading or Writing), the processing will be terminated at the end of the block during which the format error is detected. The processing of the block will include any automatic reread which maybe initiated by the existence of parity and sprocket errors. If a format error is detected while spacing over blocks the order will continue until the required number of blocks, specified in the order for spacing, have been spaced over.

Question 6: IOP Technical Manual page 3-11.

In the first paragraph of this page, are the figures given, 3.5 seconds and 600 micro. seconds correct?

Answer to question 6: The figures given were supplied by Mcd Midont, and subject to change with the insertion of the .9 inch gap.

(J. Rowe)

Question 7: In reference to the IOP Technical Manual, page 3-13 paragraph 3, which begins with "In" unredict" Is this paragraph true? If so, does this indicate that the only indication is that in the assembler availability register the assembler will be shown as busy? In such a case is the Mch reduced by 1 ? Finally, are there any forth indications?

Question 8: In reference to the Release order: If a read or write is in progress and the Release order is given, what is the effect of an error being detected before the end of block is reached?

Answer to question 8:

Insert 2.

In the event of an error occurring subsequent to the issuance of the Release order and before the end of that block has been reached, that block will continue to be processed, including any automatic retries, as is stipulated by the normal behaviour of the order. The assembler is released and the error indicator is cleared upon completion of that block.

November 10, 1959

To: R. A. Colton

Subject: Answers to Questions on Chapter 3, Technical Manual, Input-Output Processor

. . . . . .

The accompanying information has been obtained in answer to the questions raised by Chapter 3 of the Technical Manual of the Tremmac S-2000 Input-Output Processor.

The answers are made to stand alone; those with access to a Technical Manual may reference it according to the page and paragraph number indicated with each answer.

Those with the list of questions will find the answers in the same order.

Clifford A. Leventhal

CALiod

cc: J. Stone (2)

Question 9: Is it true that a situation exists where a Release order will be accepted by the 488, and YIO clears a slip, and execution because of the development of some error, the matrix is not normally released? Will the matrix be released if an error already exists?

Question 10: Concerning Reminds:

Under what circumstances is a normal order accepted? Is a normal accepted while a unit is released, reminds, connected to an accumulator, what else?

Question 11: If [illegible] means 3 words the way it is explained in the 488 Technical Manual, how can the program determine that the four counters have occurred? This is in reference to page 3-13.

Question 12: In a system with more than one Accumulator, while the only order is in progress, can other orders be interpreted [illegible] using the 488?

Question 13: If the 488 is in the midst of reading or writing a block when the Stop order is issued, when does memory addressing cease? Will it cease immediately upon issuing the Stop order, or will memory addressing continue for the remainder of the block?

Question 14: How does the program determine if an Input-Output unit is not physically plugged into the system, i.e. an address plug not plugged into the 488, or a universal Buffer-Controller (model 282) with the off-line button depressed.

PHILCO-2000 MAGNETIC TAPE CHARACTERISTICS

Philco Part Number 398-1613-N

PHILCO-2000 System Magnetic Tape has a one mil Mylar* base, is one inch wide and comes in five (5) tape lengths: 600, 1,200, 1,800, 2,400 and 3,600 feet. Data is recorded in fixed block form. Each block size is 128 words, recorded in 512 frames. Each frame contains 12 data bits, two parity bits and two timing bits. In addition to the 512 frames, a 513th frame gives each of the 14 horizontal channels an even parity bit for parity checking the block.

The density of recording on magnetic tape is 375 bits per inch and the tape speed is 120 inches per second (IPS). The end-of-block gap is 0.9 inch and the data transfer rate is 90,000 characters per second.

The tape is furnished to the user completely edited on a precision reel. Each reel is furnished in a lightweight plastic storage container.

One Inch, One Mil

MYLAR* MAGNETIC TAPE

This specification covers an instrumentation or computer grade tape suitable for digital information storage within the PHILCO-2000 System under the following conditions:

OPERATING CONDITIONS

Tape is intended to be used on Philco tape transports, operated at tape speeds of 120 IPS on recording and 180 IPS or 240 IPS on rewinding.

Recording will be digital, NRZI, at a density of 375 bits per inch (BPI) for information tracks; 16 channels are equally spaced across one-inch tape.

Tape, while in library storage and in system use will be subjected to temperature excursions from 55 degrees Fahrenheit to 100 degrees Fahrenheit with relative humidity varying between 50 and 95 percent. The tape, therefore, must meet all physical and magnetic specifications under these diverse conditions. In addition, the tape will be subjected, during transit, to more

* Registered, duPont Corporation

severe environmental conditions. Any deterioration during such transit must be of a temporary nature.

Before being placed in service, the tape will be inspected for conformance to specifications. Inspection will be performed in a controlled, dust-free area by trained personnel using precision equipment. During inspection, tape will be edited.

Editing shall define usable areas of the tape with beginning and end-of-tape block markers.

PHYSICAL CHARACTERISTICS

Dimensional

Tape Width: 1.000" + .000
- .004

Edges, when examined microscopically, shall show no tears, splits or edge cracking. In addition, tape must be free of all slitting dust.

Backing: 1 mil nominal Mylar. Variation in thickness within a reel must not be greater than +5%, -10%.

Coating Thickness: 0.45 mil max.
0.30 mil min.

Longitudinal Curvature must be less than 3/8 inch per 3 feet of tape. Measurement is to be made with oxide surface placed on a plane and with the tape permitted to assume its natural curvature.

Ultimate Tensile Strength at room temperature at 50% Relative Humidity (RH): 25,000 PSI.

Yield Strength shall be measured at a constant rate of elongation (100%/min.). At the yield point (13,000 PSI) elongation shall not exceed 6 percent. Up to the yield point the stress shall be proportional to the strain. Permanent elongation after 3 hours under 3 pounds tension shall not exceed 1½ percent.

Impact Strength: 60 Kg-cm.

Tear Strength: 12 gms.

Thermal Coefficient of expansion: 2×10^{-5} inches/inch/degrees Fahrenheit (from 70 degrees to 120 degrees Fahrenheit).

Humidity Coefficient of expansion: 1.1×10^{-5} inches/inch/% RH (20-92% RH).

Dimensional (cont'd.)

The tape shall exhibit no sticking or layer-to-layer adhesion when tested in accordance with MIL-T-21029 Specification.

Coefficient of friction on coating side shall not exceed 0.33 when measured according to Paragraph 4.4.7 of BuShips Specification W-T-0061.

The magnetic layer of the tape shall show no evidence of anchorage failure when tested in accordance with Paragraph 4.4.9 of BuShips Specification W-T-0061 and shall exhibit no visible defects.

No splices shall be permitted.

Tape shall be wound at uniform tension (not to exceed 1½ pounds) on 10½-inch diameter precision reels. Wind shall be Mylar side out.

PACKAGING

Tape reel shall be sealed in clean Polyethylene bags which shall be heat sealed and packed in paperboard boxes that hub support the reel to prevent reel and tape damage. Visible dust or dirt in the Polyethylene bag shall be cause for rejection.

Manufacturer shall ship the tape in a sturdy paperboard container that is legibly marked with the manufacturer's part number, batch number, and date of manufacture.

PERFORMANCE CHARACTERISTICS

This tape will be tested, edited, and used on the Philco transport. Operating characteristics of this transport which are pertinent to some of the requirements of this Specification are as follows:

Recording tape speed: 120 IPS ±3% (when measured between pulses 22.2 microseconds apart).

Information density: 375 BPI NRZI.

Recording Head Characteristics:

Gap Width:	.00025" (Mechanical).
Write Current:	85 ma, 0 to peak.
No. of Tracks:	16 equally spaced across 1" Tape.
Track Width:	Write - .032 ± .0005 in.
	Read - .025 ± .0005 in.

MAGNETIC PROPERTIES

Hc (Oersteds) 240-275
Br (Gauss) 850-1100
ϕr (Lines/$\frac{3}{4}$") 0.6 ± 10%

} Measured at H = 1000 Oersteds

RECORDING PROPERTIES

These properties are a prime requirement and shall, if necessary, take precedence over those listed above in MAGNETIC PROPERTIES. Testing will be done on a Philco transport having the characteristics described above in PERFORMANCE CHARACTERISTICS.

OUTPUT - Information written at 375 BPI NRZI shall produce a nominal output signal of 17 mv ± 4.5 mv, peak to peak, when measured across a 3K ohms resistive load.

RESOLUTION - Information will be written as a step function recording at 33 BPI. Rise time of write pulse will be 2 microseconds maximum between the 10 and 90 percent points. At a tape speed of 120 IPS, ±3%, the width of the playback signal, measured at 20% of peak amplitude of nominal playback signal, shall not exceed 18 microseconds.

ERRORS shall be defined as drop-outs, wherein the signal in any track, recorded at 375 BPI, NRZI, falls below 8.5 mv peak to peak amplitude; and pick-ups, signals in any track which exceed 1.5 mv peak to peak amplitude after D.C. erase.