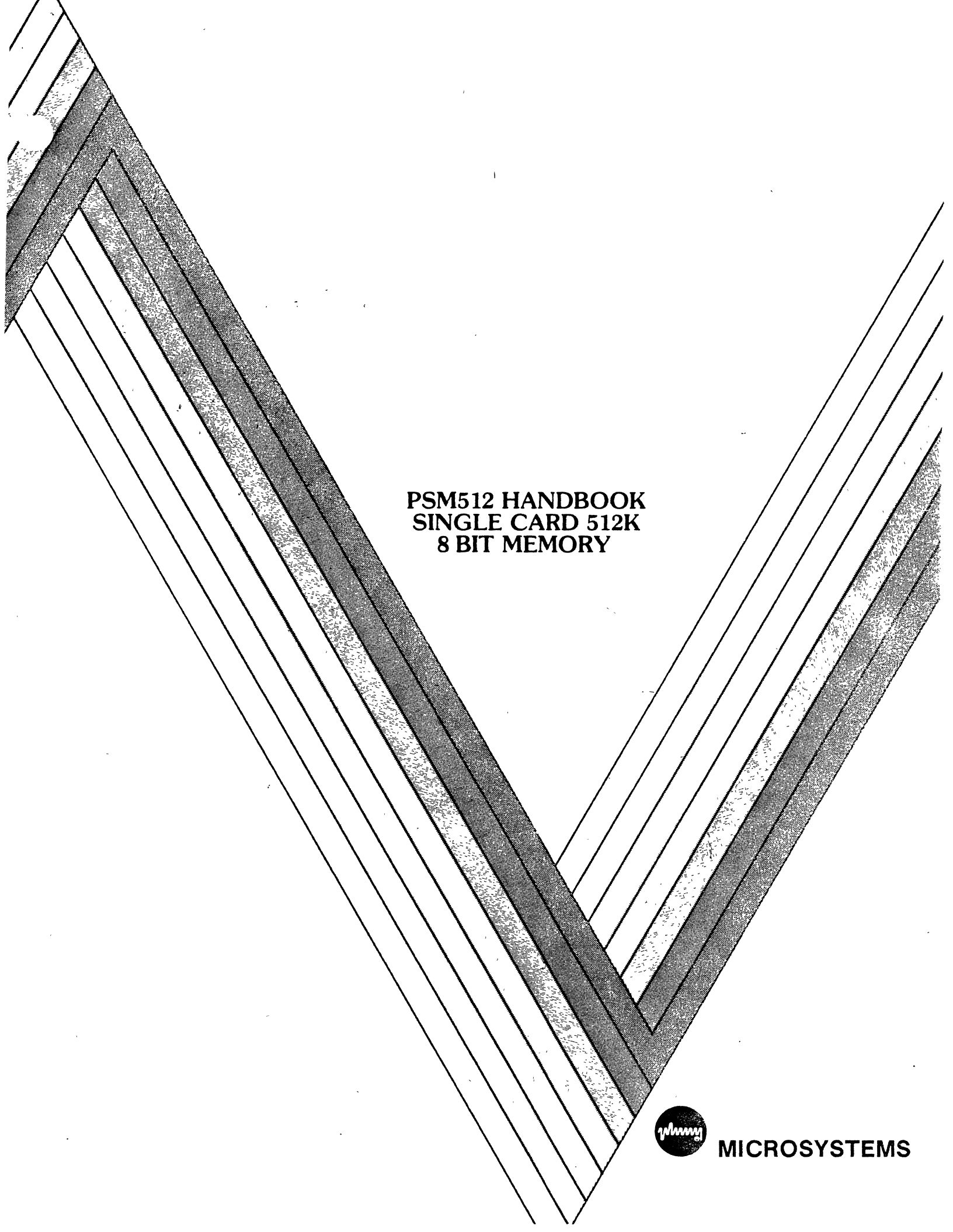

PSM512 HANDBOOK
SINGLE CARD 512K
8 BIT MEMORY

MICROSYSTEMS

PSM512 HANDBOOK
SINGLE CARD 512K
8 BIT MEMORY

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Page	21	22	23	24	25	26	27	28	29	30
Issue	1	1	1	1	1	1	1	1	1	1

Page	31	32	33	34	35	36	37	38	39	40
Issue	1	1	1	1	1	1	1	1	1	1
Page	41	42	43	44	45	46	47	48	49	50
Issue	1	1	1	1	1	1	1	1	1	1
Page	51	52	53	54	55	56	57	58		
Issue	1	1	1	1	1	1	1	1		

CONTENTS PAGE

1. SCOPE 4

2. RELATED DOCUMENTS 4

3. GENERAL DESCRIPTION 6
   3.1 System Configuration 6
   3.2 Circuit Description 6
   3.3 Mechanical Construction 8

4. SPECIFICATION SUMMARY 9

5. ELECTRICAL CHARACTERISTICS 10
   5.1 Functional Description 10
   5.2 Interface Characteristics 11
   5.3 Error Detection and Correction 21
   5.4 Power Requirements 21
   5.5 Memory Capacities 21

6. ENVIRONMENTAL SPECIFICATION 27
   6.1 Operating 27
   6.2 Storage 27

7. QUALITY AND RELIABILITY 28
   7.1 Quality Programme for Design, Manufacture and Test 28
   7.2 Reliability 28
   7.3 Mean Time Between Failures 29

8. MAINTENANCE 30

9. BOARD SET UP 31
   9.1 Interrupt 31
   9.2 Memory Mapping 33
   9.3 Refresh 43
   9.4 Data Retention 43
   9.5 Miscellaneous 43

CONTENTS PAGE

10.	SYSTEM DESCRIPTION	44
	10.1 Memory Array	44
	10.2 Address Multipying, Memory Selection and RAS Decode	46
	10.3 Refresh Logic	47
	10.4 Data Control	49
	10.5 Timing Control	50
	10.6 Error Detection and Correction	51
11.	FAULT FINDING	52
12.	INSTALLATION AND OPERATION	54
	12.1 Receiving Inspection	54
	12.2 Installation	54
	12.3 Power Requirement	54
	APPENDIX 1	55 - 57

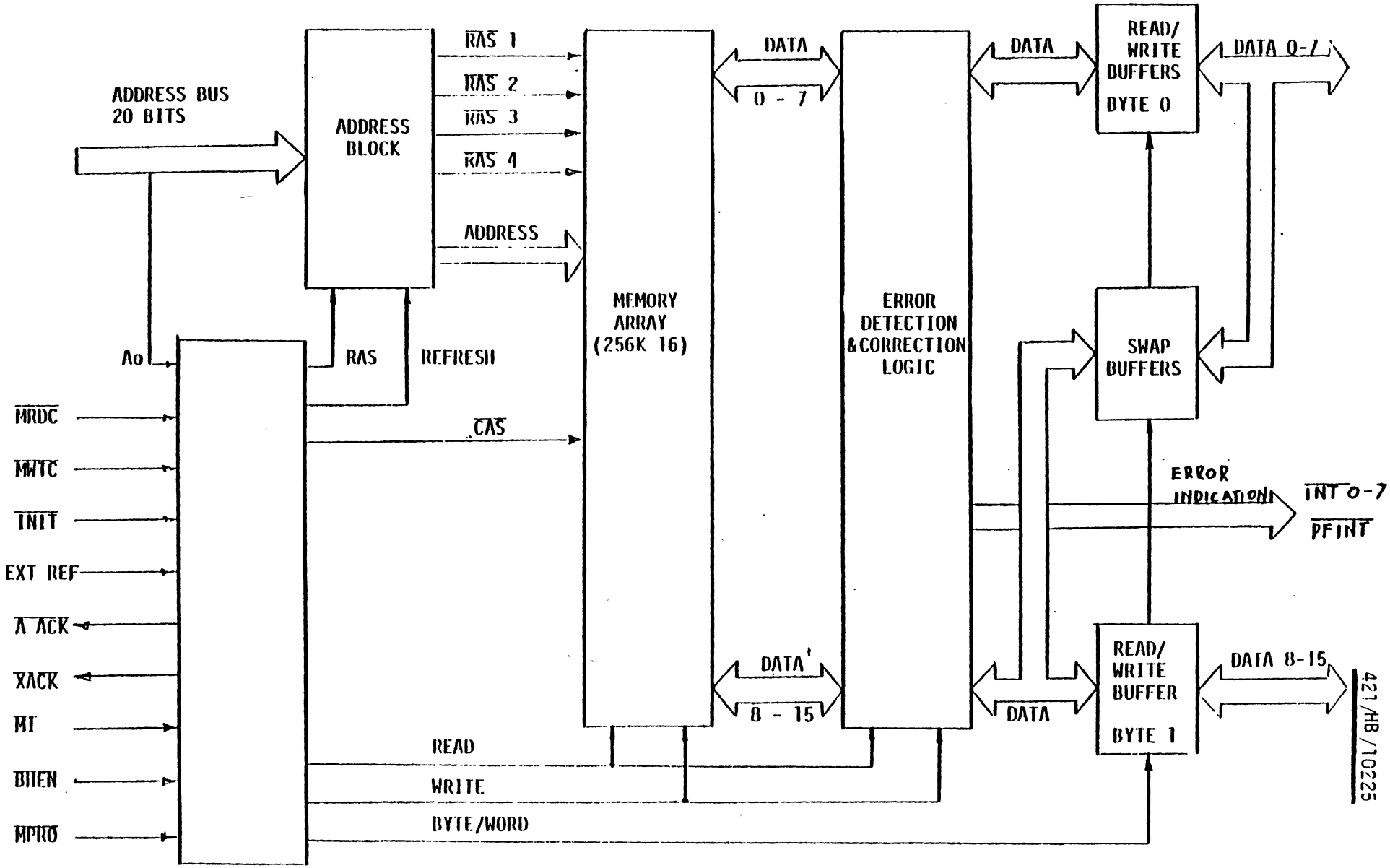
1. SCOPE

This document defines the functional, electrical and mechanical characteristics of the Plessey Semiconductors Memory PSM 512, designed and manufactured by Plessey Microsystems Limited.

The PSM 512 is part of the Plessey series of module memory systems designed for modular storage requirements.

2. RELATED DOCUMENTS

PLESSEY MICROSYSTEMS QUALITY MANUAL
PLESSEY MICROSYSTEMS ENGINEERING INSTRUCTION MANUAL
APPLICATION NOTES PSM 512.



512K 8 BIT MEMORY BLOCK SCHEMATIC

3. GENERAL DESCRIPTION

3.1 SYSTEM CONFIGURATION

The PSM 512 memory is designed to use with 8 bit and 16 bit microprocessors. The memory has a maximum capacity of 524,288 words 8 bits and operates at a maximum cycle time of 500 nano-seconds, with an access time not greater than 300 nano-seconds. The memory may be operated with an 8 bit or 16 bit word length.

The memory has an address capability of 16,048,576 words, thus 32 memory cards may be operated together to give a maximum capacity of 8,048,576 words 16 bits.

The memory is fitted with single bit error detection and correction and double error detection circuitry.
The communication between the Data Processing Equipment and the memory takes place by means of three main buses. These are:-

Bi-directional Data Bus
Control Bus
Address Bus

3.2 CIRCUIT DESCRIPTION

The memory uses the industry standard 16 pin dual-in-line 65,536 MOS dynamic RAMS.

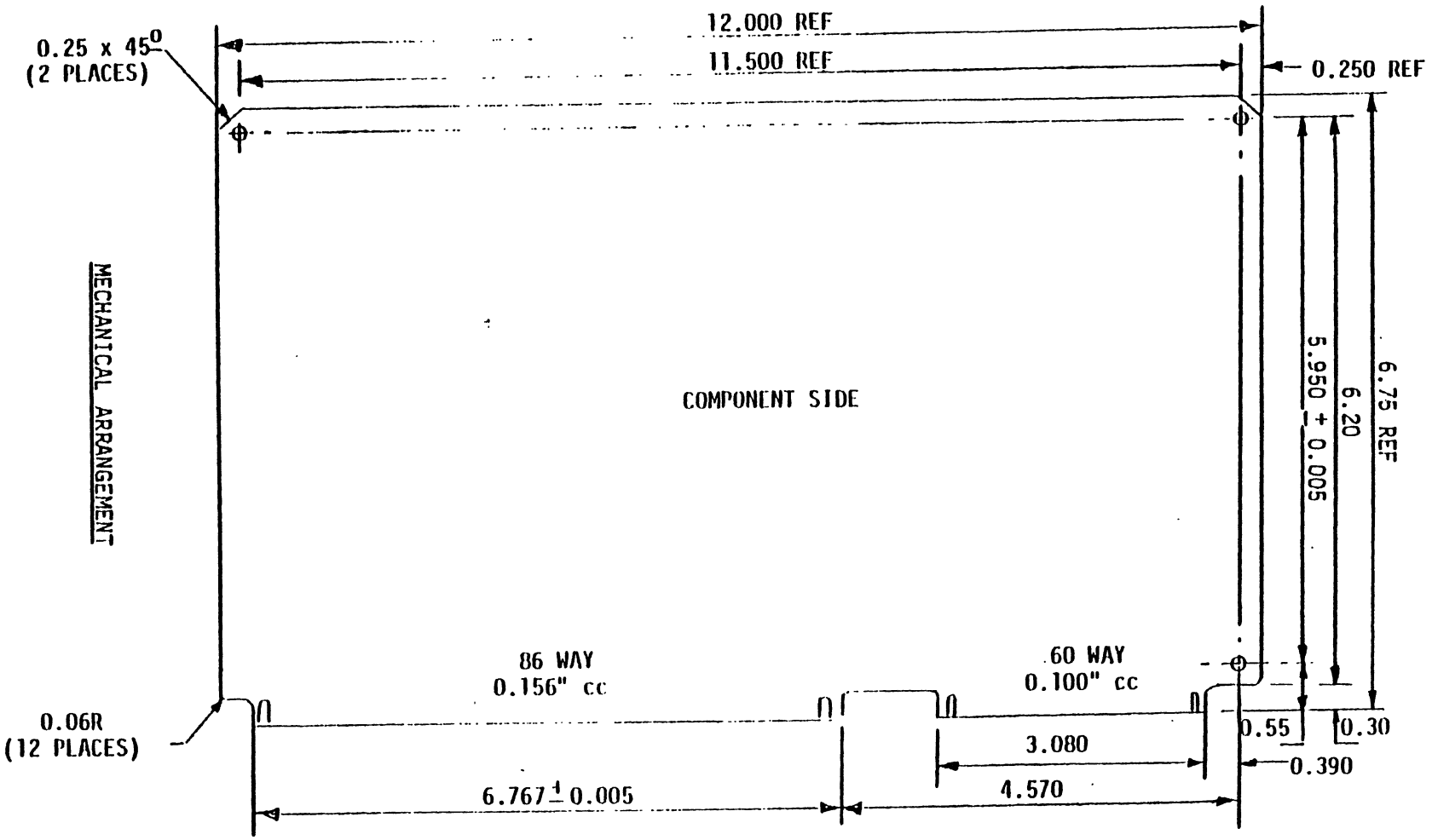
Texas 75136 Transceivers are connected to the Data bus. Address and control input lines to the memory are loaded with one LS gate with the exception of addresses $\overline{\text{ADR0}}$, $\overline{\text{ADR10}}$, $\overline{\text{ADR11}}$, $\overline{\text{ADR12}}$ and $\overline{\text{ADR13}}$ which have a maximum load of three LS gates.

The memory card can be depopulated to give different memory capacities.

On card compari tors enables the memory starting and finishing addresses to be selected by means of a dual-in-line switch. The address boundary for the starting and finishing addresses are restricted to 64K when working in a 1 megabyte field. When working in a 16 megabyte field the address is switchable into 512K blocks which cannot straddle 1 megabyte boundaries.

The internal timing signals for the memory are generated by means of dual-in-line delay lines and TTL gates.

The block diagram of the memory system is shown on Page 5.


0.25 x 45°
(2 PLACES)
12.000 REF
11.500 REF
0.250 REF
MECHANICAL ARRANGEMENT
COMPONENT SIDE
5.950 ± 0.005
6.20
6.75 REF
86 WAY
0.156" cc
60 WAY
0.100" cc
0.06R
(12 PLACES)
0.55
0.30
3.080
0.390
6.767 ± 0.005
4.570

3.3 MECHANICAL CONSTRUCTION

The memory is constructed on a single printed card.
Details of the card size are shown on Page 7.

Connection to the card is via two edge connectors, one designated P1 is 86 way, (43 + 43) on 0.156" centres.
The other designated P2 is 60 way (30 + 30) on 0.1" centres.

Maximum component height of 0.4" enables cards to be spaced on (0.6") centres.

4. SPECIFICATION SUMMARY

Word Length:	8 bits or 16 bits
Number of Words:	524,288 max.
Reliability:	Better than 200,000 hours MTBF
Cycle Time:	500 nS Read or Write
Access Time:	300 nS Variant 1** 350 nS Variant 0**
Modes of Operation:	Read Write Refresh
Electrical Interface:	TTL
Power:	Operational 5V 3.5 amps Max. Standby 5V 3.0 amps Max.
Physical Configuration:	SBC compatible 320 mm x 154 mm x 13 mm (12 in. x 6.75 in. x 0.5 in.)
Interface:	One 0.156 in. pitch edge connector 43 x 43 way. One 0.1 in. pitch edge connector 30 + 30 way
Temperature range:	0 - 55°C
Humidity:	0 - 95% without condensation
Weight:	1 Kg (2.2 lb.)

5. ELECTRICAL CHARACTERISTICS

5.1 FUNCTIONAL DESCRIPTION

The memory operates in the following modes:-

Read Cycle
Write Cycle
Refresh Cycle

5.1.1 READ CYCLE

On command from the processor, the memory places the contents of of the address location onto the Data bus.
The read data is retained in the memory.

5.1.2 WRITE CYCLE

Data presented on the Data bus by the processor is written into the addressed location.

5.1.3 REFRESH CYCLE

At least once every 2 milli-seconds the contents of the memory require to be refreshed. The memory uses distributed refresh and refresnes the contents of one row address approximately every 15 microseconds.

Refresh cycles occur asynchronously and in the event of simultaneous requests from the processor and the refresh circuitry, a priority staticiser determines which cycle the memory accepts. If the memory cycle carried out first is the refresh cycle, then the processor request is staticised and actioned on completion of the refresh cycle. When priority is given to the processor cycle, the next memory cycle will be a refresh cycle.

The on card refresh circuitry can be disabled at the interface and refresh cycles can be initiated by the processor.

5.2 INTERFACE CHARACTERISTICS

5.2.1 LOGIC LEVEL

Input and Output logic level shall be as follows:-

	MIN.	MAX.
Logic high input voltage VIH	2.2	5.25V
Logic low input voltage VIL	-0.5	0.6V
Logic high output voltage VOH	2.2	5.25V
Logic low output voltage VOL	-0.5	0.6V

Timings shall be measured at the 0.8V level for low going signals and at the 2.0V level for high going signals.

5.2.2 INTERFACE SIGNALS

Input signals are all single sided, the complement is not required.

The Data bus is connected to the memory via Texas 75136 transceivers.

The control and address inputs are loaded with one LS gate except addresses $\overline{ADR0}$, $\overline{ADR10}$, $\overline{ADR11}$, $\overline{ADR12}$ and $\overline{ADR13}$ which have a maximum of three LS gates. The control signals from the memory are driven by 74LS240 tristate gates.

The interface signals are tabulated below:-

Data (DAT Ø - DAT 15)		
Address ($\overline{ADR0}$ - $\overline{ADRF}$, $\overline{ADR10}$ - $\overline{ADR13}$)		
Reset ($\overline{INIT}$)		
Memory Read Command ($\overline{MRDC}$)		
Memory Write Command ($\overline{MWTC}$)		
Memory Inhibit ($\overline{INH}$ 1)		
External Refresh (EXT REF)		OPTIONAL
Advance Acknowledge ($\overline{AACK}$)		OPTIONAL
Transfer Acknowledge ($\overline{XACK}$)		
Memory Protect ($\overline{MPRO}$)		
Byte High Enable ($\overline{BHEN}$)		
Single Bit Error	INT0-7	OPTIONAL
Double Bit Error	PFIN	OPTIONAL

5.2.2.1 DATA (DAT Ø - DAT 15)

Data to and from the processor and memory is carried on 8 or 16 lines. When the memory is operated in the Byte mode, data is carried on 8 lines and the memory appears as an 8 bit memory. When the memory is operated in the word mode, data is carried on 16 lines and the memory appears as a 16 bit memory.

In write cycle operation data must be established at its correct level not later than the leading edge of the $\overline{\text{MWTC}}$ command. In read cycle operation, the read data is gated on the data bus and is valid at access time, and remains valid on the bus until the $\overline{\text{MRDC}}$ signal is removed.

5.2.2.2 ADDRESS ($\overline{\text{ADR0}}$ - $\overline{\text{ADRF}}$, $\overline{\text{ADR10}}$ - $\overline{\text{ADR13}}$ OPTIONAL $\overline{\text{A14}}$ - $\overline{\text{A17}}$)

Normally twenty address lines carry the address information to the memory card. The address information must be in its valid state not later than 50 nS prior to the issuing of the command signals $\overline{\text{MRDC}}$ or $\overline{\text{MWTC}}$.

Addresses $\overline{\text{ADR10}}$ - $\overline{\text{ADR13}}$ are used in conjunction with the on card DIL switch to determine the start and finish addresses.

If address inputs $\overline{\text{A14}}$ - $\overline{\text{A17}}$ are used then these are used in conjunction with the DIL switch to select the position of the memory in the address field. (See memory mapping for details).

5.2.2.3 RESET ($\overline{\text{INIT}}$)

This line when taken from the high to the low level clears the memory card internal logic.

5.2.2.4 MEMORY READ COMMAND ($\overline{\text{MRDC}}$)

This line going from the logic high to logic low state initiates a memory read cycle. In the event of the memory being busy due to a refresh cycle, the memory cycle is delayed until the refresh cycle has been completed.

5.2.2.5 MEMORY WRITE COMMAND ($\overline{\text{MWTC}}$)

This line going from the logic high to logic low state initiates a memory write cycle. In the event of the memory being busy due to a refresh cycle being in progress, the memory cycle is delayed until the refresh cycle has been completed.

5.2.2.6 EXTERNAL REFRESH (EXT REF)

This is connected by means of LK24 in which case this line when raised from the logic low state to the high state initiates a memory refresh cycle and inhibits the on board refresh circuitry. On return to the low state, the EXT REF line releases the on board refresh circuitry which will then operate in the asynchronous mode as normal unless the EXT REF line is again taken high within 15 μ seconds. The memory is thus completely under the control of the EXT REF signal provided it is pulsed every 15 μ seconds. When the refresh line is low for > 15 μ seconds the on board refresh re-asserts itself enabling the RAMS to be refreshed under idle or DMA transfer conditions.

Internal Refresh

This is achieved by connecting LK23, and under these conditions the board initiates its own refresh cycles every 15 μ seconds.

5.2.2.7 ADVANCE ACKNOWLEDGE ($\overline{\text{AACK}}$)

A signal from the memory to the processor indicating that the memory has received the command signal. This line goes from the logic high level to logic low level not later than 100 n seconds after the leading edge of the command signal and will remain at logic low level until the command signal has been removed.

5.2.2.8 TRANSFER ACKNOWLEDGE ($\overline{\text{XACK}}$)

Signal from the memory going from a logic high level to a logic low level indicating to the processor that the Data, in a write cycle, has been accepted by the memory and that the data lines may now be changed.

In a read cycle, $\overline{\text{XACK}}$ indicates that the read data has been placed on the Data Bus.

5.2.2.9 MEMORY INHIBIT ($\overline{\text{INH 1}}$)

This line taken from the high to low state 10 nano-seconds before the command signal going low prevents memory access, on both $\overline{\text{AACK}}$ and $\overline{\text{XACK}}$ remain high. If the inhibit line is taken low 50 nS after the command then an $\overline{\text{AACK}}$ may appear but XACK will remain high. This permits PROM or memory mapped I/O to be allocated space within the memory address field.

5.2.2.10 MEMORY PROTECT ($\overline{\text{MPRO}}$)

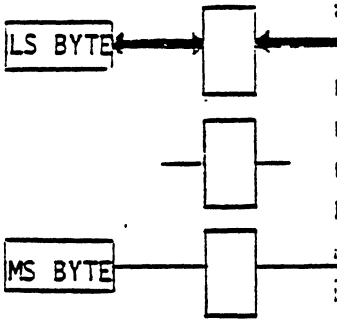
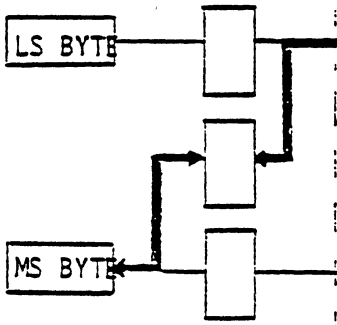
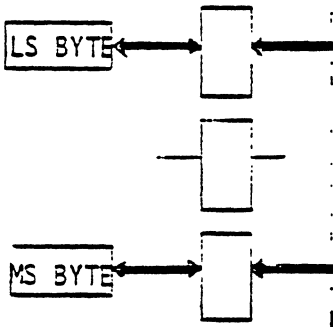
This line, via the auxiliary connector P2 on going low indicates that the input signals to the memory are no longer valid due to power failure. This line used in conjunction with an auxiliary power supply connected via the P2 connector permits the memory to preserve data in the event of main power failure.

5.2.2.11 BYTE HIGH ENABLE ($\overline{\text{BHEN}}$)

This signal from the processor is used in conjunction with address $\overline{\text{ADR0}}$ to provide Byte operation of the memory.

The memory is provided with data buffers which enables the memory's most significant data bits to be connected to Data Bus $\overline{\text{DAT0}}$ - $\overline{\text{DAT7}}$ In this configuration the memory operates as an 8 bit memory.

When $\overline{\text{BHEN}}$ is low, the memory is configured as a 16 bit memory. When $\overline{\text{BHEN}}$ is high, the Data Bus $\overline{\text{DAT0}}$ - $\overline{\text{DAT7}}$ is connected to the least significant byte or the most significant byte of the memory depending upon the level of address $\overline{\text{ADR0}}$. The truth table is shown below.

MEMORY	BUS	$\overline{BHEN}$	$\overline{ADR0}$	TRANSFER DATA PATH
	$\overline{DAT0}$-$\overline{DAT7}$ DAT8-DATF	H	H	8 BIT $\overline{DAT0}$-$\overline{DAT7}$ LSB
	$\overline{DAT0}$-$\overline{DAT7}$ DAT8-DATF	H	L	8 BIT $\overline{DAT0}$-$\overline{DAT7}$ MSB
	$\overline{DAT0}$-$\overline{DAT7}$ $\overline{DAT8}$-$\overline{DATF}$	L	H	16 BIT $\overline{DAT0}$-$\overline{DATF}$ WORD

DATA TRANSFER 8/16 BIT OPERATION

5.2.2.12 SINGLE BIT ERROR INDICATION (S.B.E.)

This indicates the occurance of a corrected single bit error in the word or checks bits being read.

This signal is optional and may be linked into INT0 - 7, power fail interrupt, or a LED, but there are conditions for its use.

1) On initial power up all memory locations which are going to be used should be written to.

2) No S.B.E. will be indicated after power up until the first read command.

3) The output signal is staticised and is reset by :

   (a) The next write command

   (b) The Initialise signal

   (c) Power switch off-on

5.2.2.13 DOUBLE BIT ERROR INDICATION

This indicates the occurrence of two or more errors in the data word read and leave the word uncorrected.

The output options to the interrupt and their re-setting are as per the single bit error indication.

5.2.4 PIN ASSIGNMENT

Two edge connectors carry the interface signals to and from the memory card. These edge connectors are designated P1 and P2.

P1 is the Bus connector and P2 is the auxiliary connector used when memory is operated in the data retention mode.

The pin assignment is tabulated below.

PIN ASSIGNMENT (PSM 512) CONNECTOR P1

COMPONENT SIDE		NON COMPONENT SIDE	
PIN	SIGNAL	PIN	SIGNAL
1	0v	2	0v
3	+5V	4	+5V
5	+5V	6	+5V
7		8	
9		10	
11	0v	12	0v
13		14	$\overline{\text{INIT}}$
15		16	
17		18	
19	$\overline{\text{MRDC}}$	20	$\overline{\text{MWTC}}$
21		22	
23	$\overline{\text{XACK}}$	24	$\overline{\text{INH 1}}$
25	A $\overline{\text{ACK}}$	26	
27	$\overline{\text{BHEN}}$	28	$\overline{\text{ADR 10}}$
29		30	$\overline{\text{ADR 11}}$
31		32	$\overline{\text{ADR 12}}$
33		34	$\overline{\text{ADR 13}}$
35	$\overline{\text{INT 6}}$	36	$\overline{\text{INT 7}}$
37	$\overline{\text{INT 4}}$	38	$\overline{\text{INT 5}}$
39	$\overline{\text{INT 2}}$	40	$\overline{\text{INT 3}}$
41	INT 0	42	INT 1
43	$\overline{\text{ADR E}}$	44	$\overline{\text{ADR F}}$
45	$\overline{\text{ADR C}}$	46	$\overline{\text{ADR D}}$
47	$\overline{\text{ADR A}}$	48	$\overline{\text{ADR B}}$
49	$\overline{\text{ADR 8}}$	50	$\overline{\text{ADR 9}}$
51	$\overline{\text{ADR 6}}$	52	$\overline{\text{ADR 7}}$
53	$\overline{\text{ADR 4}}$	54	$\overline{\text{ADR 5}}$
55	$\overline{\text{ADR 2}}$	56	$\overline{\text{ADR 3}}$
57	$\overline{\text{ADR 0}}$	58	$\overline{\text{ADR 1}}$
59	$\overline{\text{DAT E}}$	60	$\overline{\text{DAT F}}$
61	$\overline{\text{DAT C}}$	62	$\overline{\text{DAT D}}$
63	$\overline{\text{DAT A}}$	64	$\overline{\text{DAT B}}$
65	$\overline{\text{DAT 8}}$	66	$\overline{\text{DAT 9}}$
67	$\overline{\text{DAT 6}}$	68	$\overline{\text{DAT 7}}$
69	$\overline{\text{DAT 4}}$	70	$\overline{\text{DAT 5}}$
71	$\overline{\text{DAT 2}}$	72	$\overline{\text{DAT 3}}$
73	$\overline{\text{DAT 0}}$	74	$\overline{\text{DAT 1}}$
75	0v	76	0v
77		78	
79		80	
81	+5V	82	+5V
83	+5V	84	+5V
85	0v	86	0v

PIN ASSIGNMENT (PSM 512) CONNECTOR P_2

COMPONENT SIDE		NON COMPONENT SIDE	
PIN		PIN	
1	0v	2	0v
3	+5V Aux	4	+5V Aux
5		6	
7		8	
9		10	
11		12	
13		14	
15		16	
17		18	
19		20	MEMORY PROTECT ($\overline{\text{MPRO}}$)
21	0v	22	0v
23		24	
25		26	
27		28	
29		30	
31		32	
33		34	
35		36	
37		38	
39		40	
41		42	
43		44	
45		46	
47		48	
49		50	
51		52	
53		54	
55	$\overline{\text{ADR16}}$	56	$\overline{\text{ADR17}}$
57	$\overline{\text{ADR14}}$	58	$\overline{\text{ADR15}}$
59		60	

5.3 ERROR DETECTION AND CORRECTION

The memory card is fitted with single bit error detection and correction circuitry and double error detection circuitry.

Single bit error correction is automatic but an error flag may be connected to any of the bus interrupt lines by means of on board links or to an on board LED.
Double or multiple error detection flag may be connected to any of the bus interrupt lines by means of jumper links fitted on the card.

5.4 POWER REQUIREMENTS

The memory operates from a single +5V rail. The voltage and current requirements are:-

	OPERATING CURRENT			STANDBY CURRENT		
+5V ± 5%	3.0 3.5	A	typical max	2.5 3.0	A	typical max

When used in the data protect mode, a secure +5V supply (i.e. battery supported PSU) should be connected to the memory via the auxiliary connector P2. This supply must meet the requests for voltage and current stated above.

In the event of main power supply failure, the $\overline{\text{MPRO}}$ should be brought low to protect memory data.

5.5 MEMORY CAPACITIES

The memory may be depopulated to give the following capacities:-

64K 16 bits (128K bytes) and 128K 16 bits (256K bytes)

It should be noted that depopulated memories are continuous and the starting and finish address should be set accordingly.

TIMING REQUIREMENTS

READ OR WRITE CYCLE

		MIN	MAX	UNITS	
TCY	Cycle Time	500		nS	
TAS	Address to Memory Start Set up	50		"	
TAH	Address Hold Time Referenced to $\overline{AACK}$	250		"	
TCP	Command Pulse Width Referenced to $\overline{AACK}$	350		"	Notes 1 & 2
TAC	Access Time		350	"	Note 1
TAACK	Command to $\overline{AACK}$ Delay		100	"	Notes 1 & 3
TDZ	Command going positive to Read Data High Impedance	0	100	"	
TXACK	Command to XACK Delay		350	"	Notes 1 & 3
TACKH	AACK and XACK going positive reference command going positive	0	100	"	
TDS	Write Data Set up Time		390	"	
TDH	Write Data Hold Time Referenced to AACK	400		"	Note 1

Note 1. The above timings assume there is no refresh cycle in operation when command is sent. In refresh cycle inhibit, the $\overline{AACK}$ and $\overline{XACK}$ signals until the refresh cycle is complete. The Command, Address and Data signals must be maintained until the memory responds with $\overline{AACK}$ and $\overline{XACK}$ and the timings referenced to $\overline{AACK}$ observed.

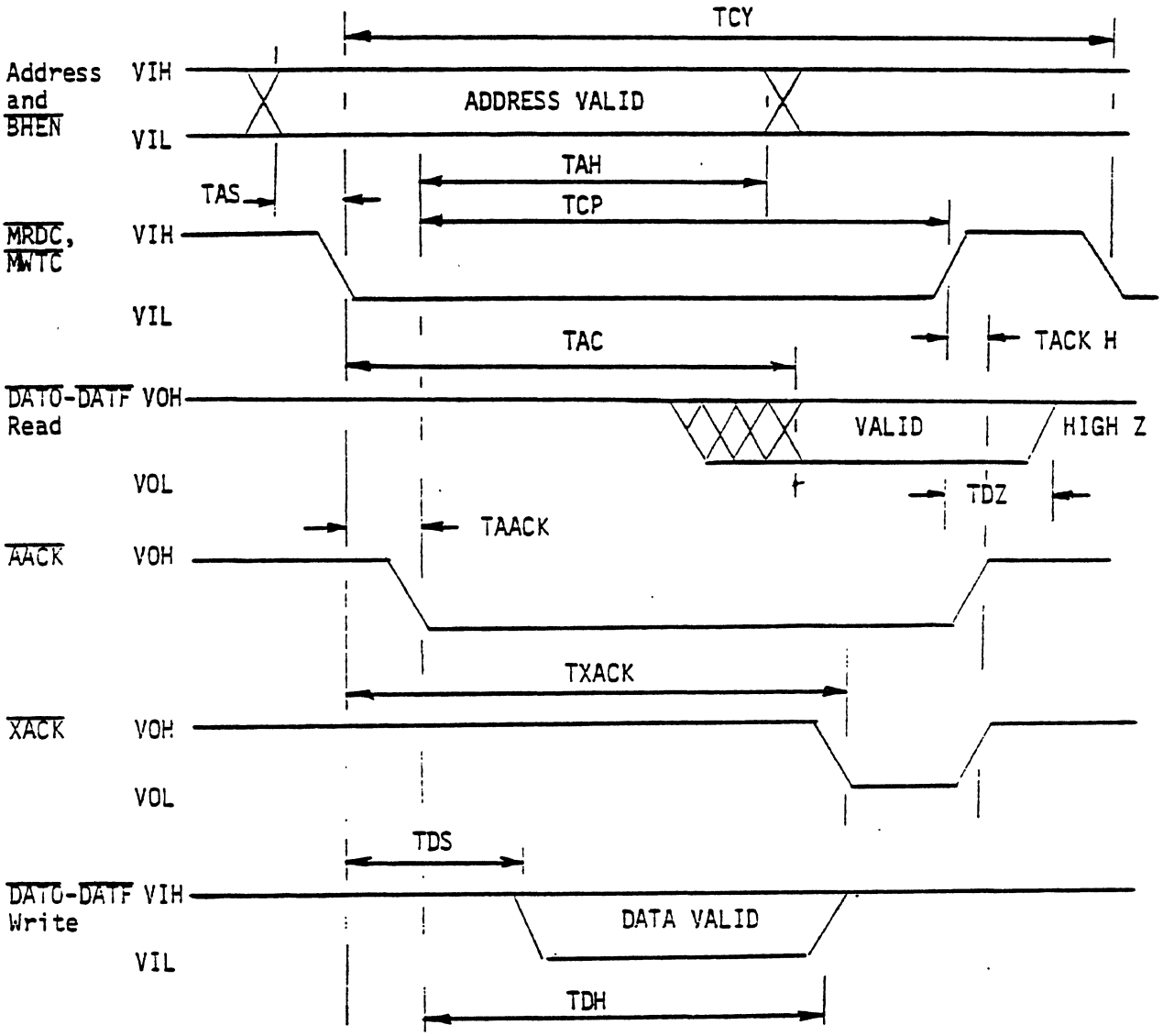
Note 2. When $\overline{AACK}$ is not used, the $\overline{XACK}$ signal should be used to control the Command, Address and Data signals.

Note 3. The $\overline{AACK}$ and XACK signals are adjustable in 25 nS steps by means of delay line taps so that their negative transition can be adjusted to suit system requirements. Unless otherwise specified by the customer the timing of $\overline{AACK}$ and $\overline{XACK}$ will be within the limits specified above when the memory is despatched from the factory.

Note 4. The board is also available using the 64K-2 part (150nS access) the access time can be reduced to 300nS and the cycle time to 470nS.

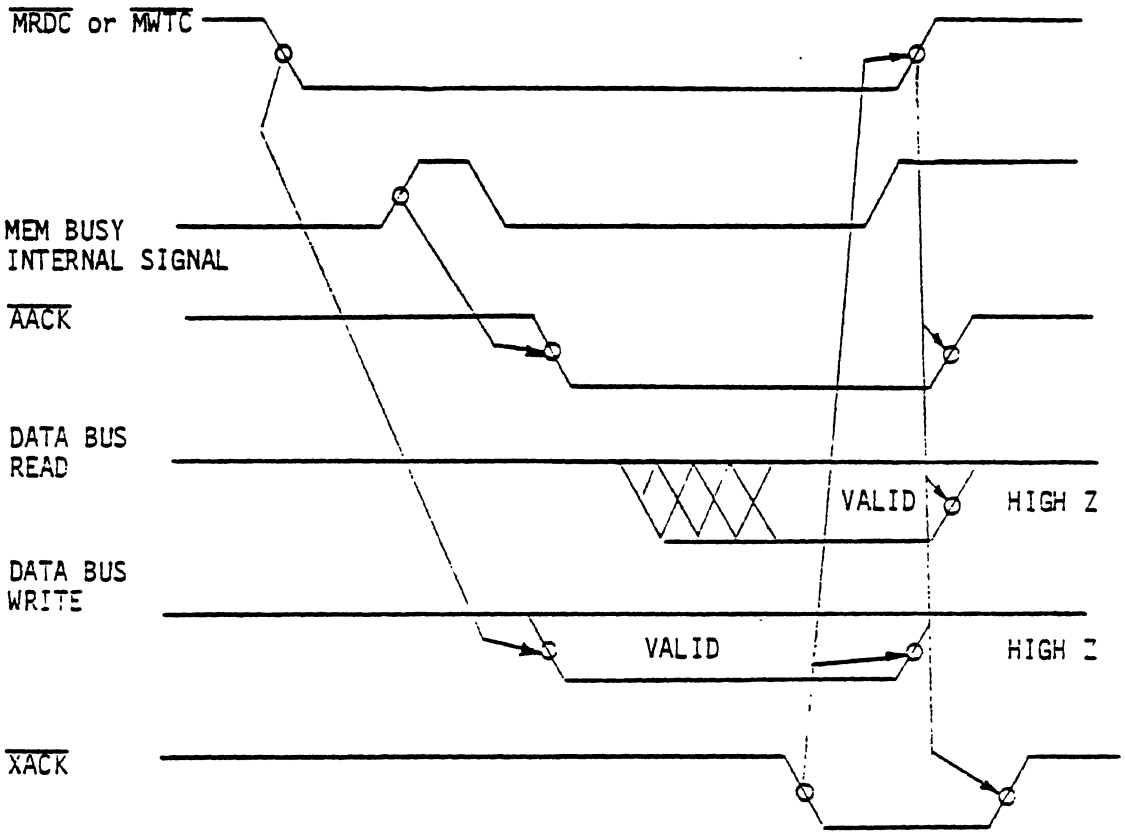
TIMING WAVEFORMS

READ OR WRITE CYCLE



TIMING WAVEFORMS

READ OR WRITE CYCLE



AACK and XACK delayed if MRDC or MWTC while Refresh Cycle is in progress.

TYPICAL HANDSHAKE OPERATION

6. ENVIRONMENTAL SPECIFICATION

6.1 OPERATING

The memory system will operate under the following conditions.

Temperature Range	0^{o} to $+55^{o}C$
Cooling Requirement	Airflow of 100 metres per minute parallel to the edge connectors

Damage may occur to the memory if run without cooling for a period in excess of 30 minutes at maximum temperature.

Relative Humidity	Up to 95% without condensation
Thermal Shock	$\pm$ $1^{o}C$ per minute
Altitude	- 300 to + 3000 M
Vibration	5 - 100Hz with 0.5g acceleration
Mechanical Shock	10g for 6 mill-seconds (half sine) when mounted in a suitable racking system

6.2 STORAGE

The memory system may be stored or transported without damage provided the environment is within the limitation shown below:-

Temperature Range	- $55^{o}C$ - + $85^{o}C$
Relative Humidity	0 - 95% without condensation
Thermal Shock	$\pm$ $10^{o}C$ per minute
Altitude	- 300m to + 16,000m
Vibration	0 - 500Hz, 2g acceleration
Mechanical Shock	20g for 6 milli-seconds (half sine)

7. QUALITY AND RELIABILITY

7.1 QUALITY PROGRAMME FOR DESIGN, MANUFACTURE AND TEST

All systems are manufactured directly in accordance with a Quality Plan. The Quality Plan monitors the systematic evolution of system design and evaluation and production activity. By this means it is possible to ensure that all systems despatched to the customer conform in all respects to the requirements set out in this product specification.

7.2 RELIABILITY

In order to maximise system reliability, all areas of activity are carefully controlled and monitored.

Design - All design activity is carried out to predetermined rules, which includes component derating, stress, reliability and maintainability analysis.

Qualification - Each design is rigorously tested to ensure conformance with the specified performance and environmental requirements.

Procurement - Components are carefully selected and obtained only from approved suppliers.

Manufacturing - Performed against planned work instructions and firm workmanship standards.

Test - All testing is performed against defined test specifications and the results recorded and retained.

Thorough screening tests (burn-in) are applied to all production, thereby ensuring that all manufacturing defects are detected and corrected at the earliest opportunity.

7.3 MEAN TIME BETWEEN FAILURES

The calculated mean time between failure (MTBF) for the memory is greater than 200,000 hours. The component failure rates used in this calculation have been derived from MIL STD 217B, British Post Office publications, manufacturers published data and in-house sources.

8. MAINTENANCE

No routine maintenance is necessary on the PSM 512 Memory Card. However it is advisable to maintain a preventable maintenance programme to give a maximum operating efficiency, this includes:-

(a) Periodic checking of the Memory EDC line should be carried out while reading from the whole memory to check that no memory device has failed and is being continually corrected as this will reduce reliability.

(b) A check that the operating voltage is within the limits of the specification, ie. 5V $\pm$ 5%.

(c) Also check airflow is adequate, clean and replace air filters as necessary.

9. BOARD SET UP

9.1 Interrupt

The memory provides an interrupt when either an un-correctable error (double bit or multi-bit) is detected or when a single bit corrected error has occurred.

The un-correctable error interrupt may be connected to either the power fail line or to one of eight interrupt lines.

The correctable error interrupt may be connected to one of eight interrupt lines.

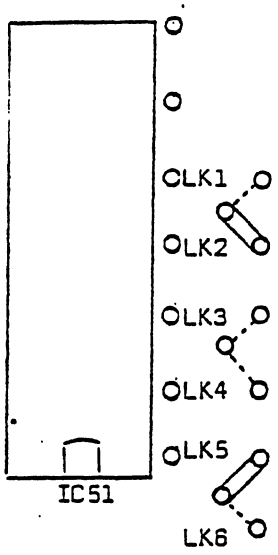
Either of the interrupts may also be connected to the LED fitted to the front of the card.

Figure 1 illustrates the different possibilities.

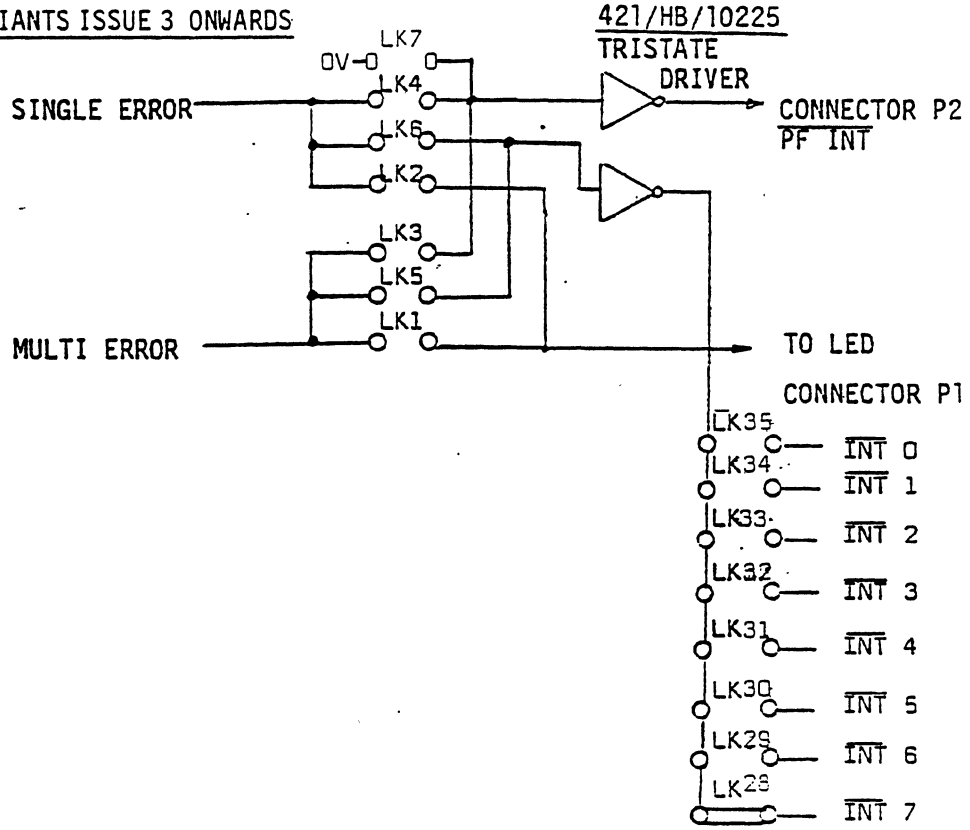
Interrupt is cleared on the next memory write cycle.

On power up due to the random data held in the RAMS, errors and consequently interrupts will occur if attempts are made to read data from the memory. The user must therefore write data to all address locations after power up, before reading data from the memory. Writing may be in 8 bit bytes or 16 bit words as the interrupt circuitry is enabled by the first read command to the memory after power-up. If the memory is used in Data Retention option this condition does not apply (see Section 9.4)

FOR 421/MB/10226/ALL VARIANTS ISSUE 3 ONWARDS



INTERRUPT LINKS
P.C.B. COMPONENT SIDE



INTERRUPT CIRCUIT

Links LK2 and LK5 fitted on shipment.

Link LK1 fitted connects Multi-error to LED Indicator.

Link LK2 fitted connects Single-error to LED Indicator.

It is not permissible to fit both LK1 and LK2.

Link LK3 fitted connects Multi-error to Power Fail Interrupt Line.

Link LK4 fitted connects Single-error to Power Fail Interrupt Line.

If neither LK3 or LK4 are fitted fit LK7 to hold $\overline{\text{PF INT}}$ high.
Only fit one of the following LK3, 4, 7.

Link 5 fitted connects Multi-error to Interrupt Bus.

Link 6 fitted connects Single-error to Interrupt Bus.

Do <u>not</u> fit both LK5 and LK6.

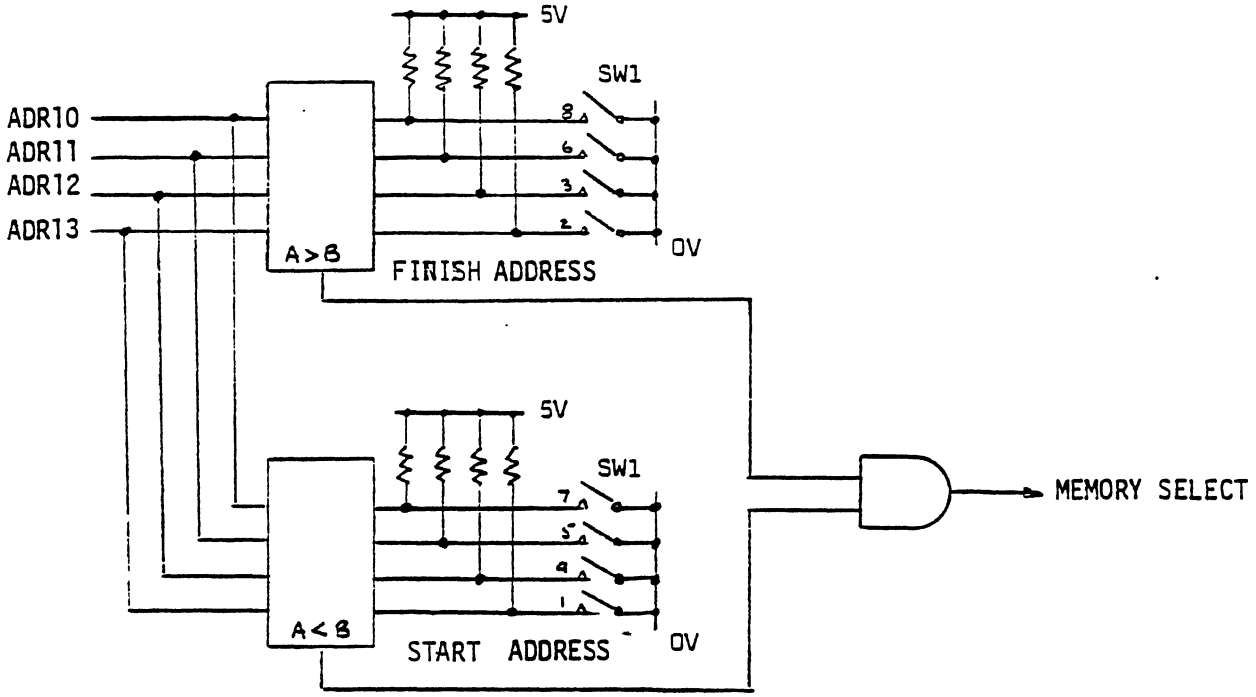
FIGURE 1: INTERRUPT FACILITIES

9.2 Memory Mapping

The user has two memory map options dependent upon the address range used.

9.2.1 Address Range 1 Megabyte (Multibus addresses ADR0 - ADR13)

Two four bit comparators are used to set the start and finish address of the memory. Multibus addresses ADR10, ADR11, ADR12 and ADR13 are fed to one set of the comparator inputs, the other set being controlled by dual-in-line switch SW1. The start and finish addresses are thus set in 64K byte steps. The circuitry is shown below.



The finish address is determined by switch positions 2, 3, 6 and 8.

The start address is determined by switch positions 1, 4, 5 and 7.

Table 1 shows the switch settings for the start address, and Table 2 the switch settings for the finish address. Table 3 shows the switch settings for a 512K byte memory with a 1 megabyte field. In the tables a "C" indicates the switch is closed, "O" indicates open.

START ADDRESS BYTES	HEX ADDRESS	MULTIBUS ADDRESS				SWITCH 1 POSITIONS			
		$\overline{ADRT0}$	$\overline{ADRT1}$	$\overline{ADRT2}$	$\overline{ADRT3}$	7	5	4	1
960K	F0000	L	L	L	L	C	C	C	C
896K	E0000	H	L	L	L	O	C	C	C
832K	D0000	L	H	L	L	C	O	C	C
768K	C0000	H	H	L	L	O	O	C	C
704K	B0000	L	L	H	L	C	C	O	C
640K	A0000	H	L	H	L	O	C	O	C
576K	90000	L	H	H	L	C	O	O	C
512K	80000	H	H	H	L	O	O	O	C
448K	70000	L	L	L	H	C	C	C	O
384K	60000	H	L	L	H	O	C	C	O
320K	50000	L	H	L	H	C	O	C	O
253K	40000	H	H	L	H	O	O	C	O
192K	30000	L	L	H	H	C	C	O	O
128K	20000	H	L	H	H	O	C	O	O
64K	10000	L	H	H	H	C	O	O	O
0K	00000	H	H	H	H	O	O	O	O

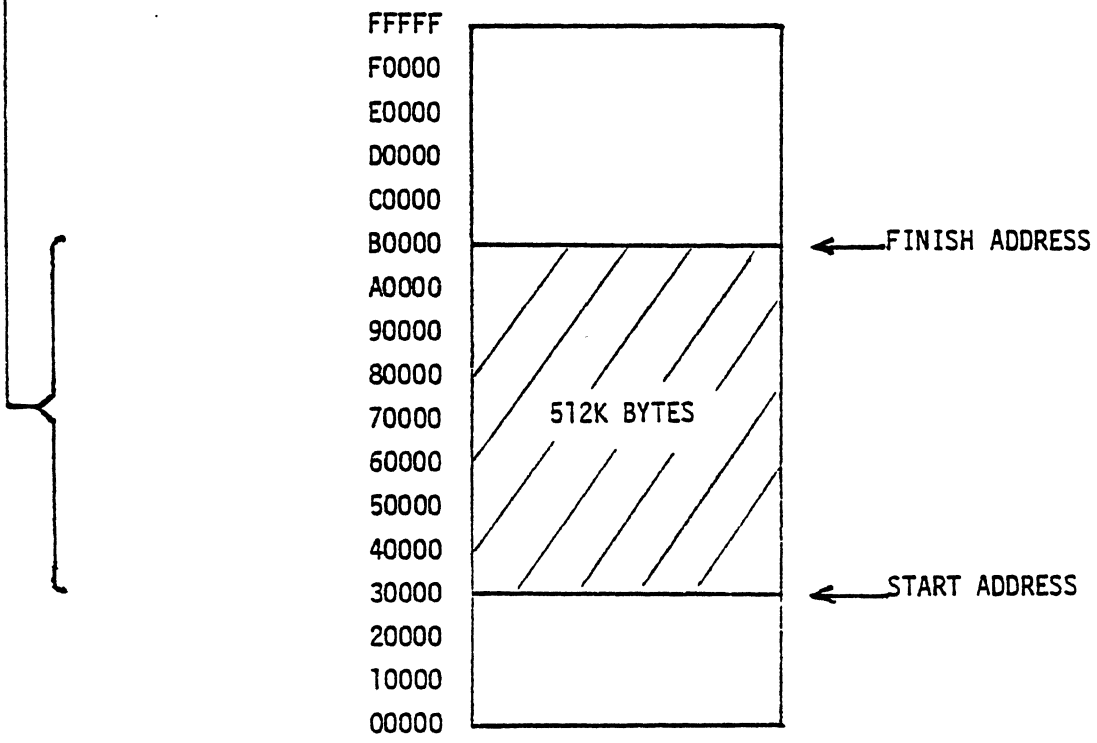
TABLE 1: START ADDRESS

FINISH ADDRESS BYTES	HEX ADDRESS	MULTIBUS ADDRESS				SWITCH 1 POSITIONS			
		$\overline{ADRT0}$	$\overline{ADRT1}$	$\overline{ADRT2}$	$\overline{ADRT3}$	8	6	3	2
1024K	FFFFF	L	L	L	L	C	C	C	C
960K	EFFFF	H	L	L	L	O	C	C	C
896K	DFFFF	L	H	L	L	C	O	C	C
832K	CFFFF	H	H	L	L	O	O	C	C
768K	BFFFF	L	L	H	L	C	C	O	C
704K	AFFFF	H	L	H	L	O	C	O	C
640K	9FFFF	L	H	H	L	C	O	O	C
576K	8FFFF	H	H	H	L	O	O	O	C
512K	7FFFF	L	L	L	H	C	C	C	O
448K	6FFFF	H	L	L	H	O	C	C	O
384K	5FFFF	L	H	L	H	C	O	C	O
320K	4FFFF	H	H	L	H	O	O	C	O
256K	3FFFF	L	L	H	H	C	C	O	O
192K	2FFFF	H	L	H	H	O	C	O	O
128K	1FFFF	L	H	H	H	C	O	O	O
64K	0FFFF	H	H	H	H	O	O	O	O

TABLE 2: FINISH ADDRESS

MEMORY MAP BYTES	HEX ADDRESS	SWITCH 1 POSITION							
		7	5	4	1	8	6	3	2
0 - 512K	00000-7FFFF	0	0	0	0	C	C	C	0
64K - 576K	10000-8FFFF	C	0	0	0	0	0	0	C
128K - 640K	20000-9FFFF	0	C	0	0	C	0	0	C
192K - 704K	30000-AFFFF	C	C	0	0	0	C	0	C
256K - 768K	40000-BFFFF	0	0	C	0	C	C	0	C
320K - 832K	50000-CFFFF	C	0	C	0	0	0	C	C
384K - 896K	60000-DFFFF	0	C	C	0	C	0	C	C
448K - 960K	70000-EFFFF	C	C	C	0	0	C	C	C
512K -1024K	80000-FFFFF	0	0	0	C	C	C	C	C
		START ADDRESS				FINISH ADDRESS			

TABLE 3: TYPICAL MEMORY MAPPING



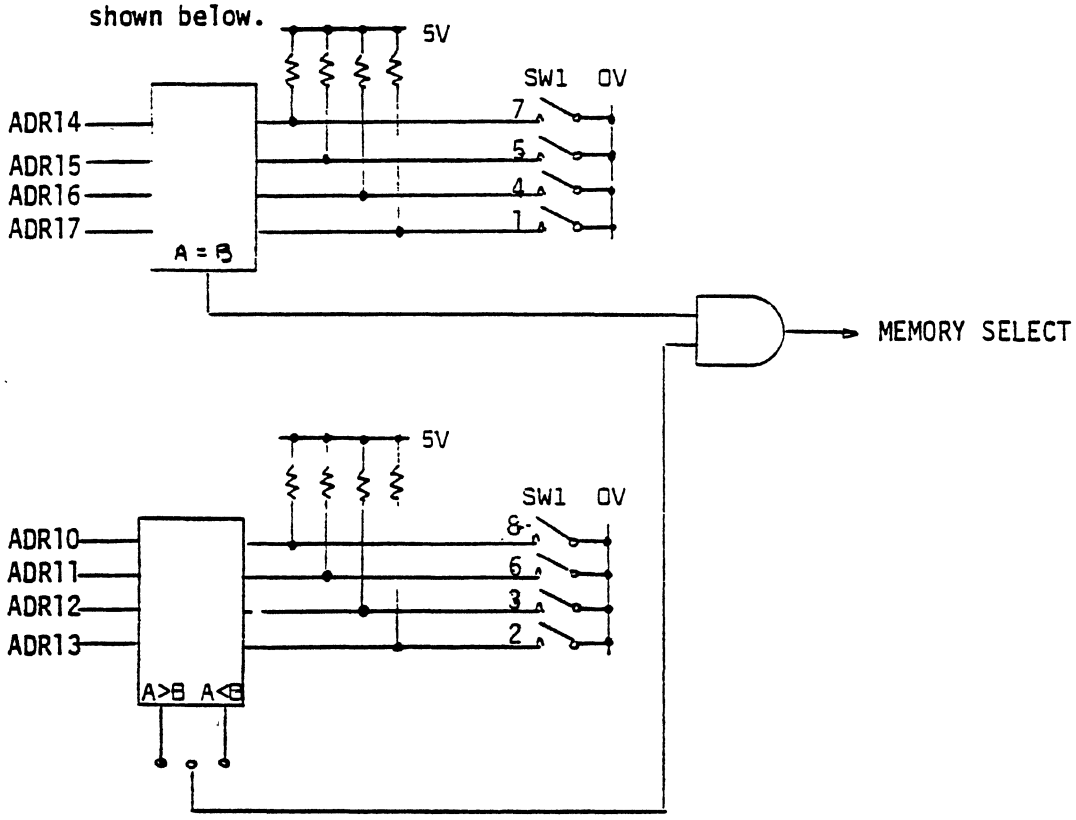
TYPICAL MEMORY MAP

It should be noted that the start, finish address technique used on the PSM512 memory allows areas at the top and bottom of the memory range to be inhibited by using Tables 1 and 2. In the example shown above, if the area addressed by HEX 30000-3FFFF was required for PROM, then the starting address would be altered to 4060. This feature is particularly useful when two PSM512 memories are occupying the whole address range of the processor. Similarly depopulated memories can be mapped as desired.

9.2.2 Address Range 16 Megabytes

Recently the Intel Multibus address range was extended to 16 megabytes with the additional four addresses $\overline{ADR14}$ - $\overline{ADR17}$ connected to the auxiliary connector P2 Pins 55, 56, 57 and 58. To operate in this configuration it is necessary to cut and strap as shown in Figure 2.

This modification reconfigures the comparator circuitry as shown below.



This allows the memory to be allocated to 1 megabyte of the address field and to occupy the top or bottom addresses of the 1 megabyte.

Table 4 shows the settings of switch SW1 to map the memory to a 1 megabyte block and Table 5 shows the allocation of the memory to the top or bottom of the 1 megabyte block. Note that in this configuration the memory must reside in the top or bottom 512K bytes, it cannot straddle the 512K boundary.

When allocated to the bottom of the 1 megabyte block, the top address limit is governed by the A < B output of the comparator so that the upper address limit can be changed by SW1 enabling PROM to be allocated address space at the top of the memories range or the use of depopulated memory. When allocated to the top of the 1 megabyte block, the starting address is governed by the A > B output so that the PROM could be allocated address space at the bottom of the memories range.

MEMORY ADDRESS BYTES	HEX ADDRESS	MULTIBUS ADDRESS				SWITCH 1 POSITION			
		$\overline{ADR14}$	$\overline{ADR15}$	$\overline{ADR16}$	ADR17	7	5	4	1
0 - 1M	000000-0FFFFF	H	H	H	H	O	O	O	O
1M - 2M	100000-1FFFFF	L	H	H	H	C	O	O	O
2M - 3M	200000-2FFFFF	H	L	H	H	O	C	O	O
3M - 4M	300000-3FFFFF	L	L	H	H	C	C	O	O
4M - 5M	400000-4FFFFF	H	H	L	H	O	O	C	O
5M - 6M	500000-5FFFFF	L	H	L	H	C	O	C	O
6M - 7M	600000-6FFFFF	H	L	L	H	O	C	C	O
7M - 8H	700000-7FFFFF	L	L	L	H	C	C	C	O
8M - 9M	800000-8FFFFF	H	H	H	L	O	O	O	C
9M - 10M	900000-9FFFFF	L	H	H	L	C	O	O	C
10M - 11M	A00000-AFFFFF	H	L	H	L	O	C	O	C
11M - 12M	B00000-BFFFFF	L	L	H	L	C	C	O	C
12M - 13M	C00000-CFFFFF	H	H	L	L	O	O	C	C
13M - 14M	D00000-DFFFFF	L	H	L	L	C	O	C	C
14M - 15M	E00000-EFFFFF	H	L	L	L	O	C	C	C
15M - 16M	F00000-FFFFFF	L	L	L	L	C	C	C	C

TABLE 4: 16 MEGABYTE MEMORY MAP

MEMORY ADDRESS BYTES	HEX ADDRESS	SWITCH 1 POSITION			
		8	6	3	2
0 - 512K	X00000 - X7FFFF	C	C	C	0
0 - 448K	X00000 - X6FFFF	0	C	C	0
0 - 384K	X00000 - X5FFFF	C	0	C	0
0 - 320K	X00000 - X4FFFF	0	0	C	0
0 - 256K	X00000 - X3FFFF	C	C	0	0
0 - 192K	X00000 - X2FFFF	0	C	0	0
0 - 128K	X00000 - X1FFFF	C	0	0	0
0 - 64K	X00000 - X0FFFF	0	0	0	0
512K - 1024K	X80000 - XFFFFF	0	0	0	C
576K - 1024K	X90000 - XFFFF	C	0	0	C
640K - 1024K	XA0000 - XFFFF	0	C	0	C
704K - 1024K	XB0000 - XFFFF	C	C	0	C
768K - 1024K	XC0000 - XFFFF	0	0	C	C
832K - 1024K	XD000 - XFFFF	C	0	C	C
896K - 1024K	XE0000 - XFFFF	0	C	C	C
960K - 1024K	XF0000 - XFFFF	C	C	C	C

TABLE 5: MEMORY WITHIN 1 MEGABYTE FIELD

FOR 421/MB/10226/ALL VARIANTS ISSUE 3 ONWARDS

FIGURE 2 16 MEGABYTE MEMORY MAPPING

Remove Links LK13, 16, 17, 18, 19 and 21.

Place Links in LK20, LK22.

Connect Wires as follows:-

Connect wire from pin shown below on LK13 to AA on connector P2 Pin 57.

" " " " " " " LK16 to Y " " P2 Pin 58.

" " " " " " " LK17 to Z " " P2 Pin 55.

" " " " " " " LK18 to X " " P2 Pin 56.

To configure 512K to the lower half of the 1 megabyte leave in Link LK15.

To configure 512K to the top half of the 1 megabyte remove LK15 and put in LK14.

FOR 421/MB/10226/ALL VARIANTS ISSUE 3 ONWARDS

9.3 Refresh

Jumper link LK23, LK38, LK39 control refresh circuitry.

For on board refresh only LK23, LK38 are in and LK39 removed.

For external refresh control only LK39, is in and LK23, LK38 removed.

For external refresh control unless the line is held low for more than 15 µS whereupon the on board refresh circuitry takes over, this is achieved by LK23, LK39 being in with LK38 removed.

9.4 Data Retention

If it is intended to use the anxiliary power supply for data retention purposes, the following action is necessary:-

Remove wire links LK24, LK25 and wire link LK40.

9.5 Miscellaneous

9.5.1 $\overline{\text{AACK}}$ Option

Jumper link LK27 connects $\overline{\text{AACK}}$ to Multibus P1 connector Pin 23 if this facility is not required, remove jumper link LK12.

9.5.2 Bus Priority

Although the memory cannot act as a Bus Master, the facility exists on the memory card to short BPRO to BPRIN by inserting link LK26. This enables the memory card, when plugged into a system with serial priority, to be positioned anywhere with the chassis.

10. SYSTEM DESCRIPTION

The Plessey PSM 512 Memory Card is a random access semiconductor memory using 64K dynamic RAMS with single bit error correction and double bit detection.

The Memory may be split up into six main sections.

10.1 Memory Array
10.2 Address Manipulation
10.3 Refresh Logic
10.4 Data Control
10.5 Timing Control
10.6 Error Detection and Correction

10.1 MEMORY ARRAY

The memory array consists of 4 rows of 22 dynamic RAMS (as shown in logic drawing sheet 2).

Each ROW containing 16 data RAMS and 6 EDC RAMS. These are all driven with the same command signals of $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address and each column (containing 4 RAMS) has command Data In and Data Out signals to complete the array.

10.1.1 THE DYNAMIC RAM

The memory is fitted with 64K x 1 dynamic RAMS.
The storage cells within the RAM are matrixed in rows and columns with a cell being selected by the row and column address being multiplied onto the device by means of the falling edge of Row Address Strobe ($\overline{RAS}$) or Column Address Strobe ($\overline{CAS}$) respectively. Data on the device Data In line may be written into the selected cell by bringing the Write Enable line ($\overline{WE}$) low when RAS and CAS are both low. Data Read from the selected cell is presented on the Data Out line at access time and remains valid until $\overline{CAS}$ returns to the high state at which time the Data Out lines revert to high impedance state.

The PSM 512 board permanently runs on a Read - Modify - Write Cycle.

In this cycle the row and column addresses are strobed in and the selected cell's data is latched onto the Data Out line at access, this remains there until $\overline{CAS}$ goes high (as in a normal read cycle) but also during the same cycle new data on the Data In line is written in by allowing $\overline{WE}$ to go low while $\overline{RAS}$ and $\overline{CAS}$ are still low. Thus enabling a Read and a Write to be achieved on one cell location in one cycle.

The only other cycle used is a Refresh cycle which is carried out by means of a $\overline{RAS}$ only cycle which is required to do 128 cycles every two milliseconds.

10.2 ADDRESS MULTIPLYING, MEMORY SELECT AND RAS DECODE

Address A0 is used in conjunction with Byte Enable (BHEN) to determine whether the memory is operating in 16 bit word of 256K or an 8 bit byte of 512K. This is done by using $\overline{BHEN}$ and A0 to control the data being driven onto the RAM or controlling the data read out of the RAM to the output bus.

The next 16 addresses ($\overline{A1}$ - $\overline{A10}$) form the multiplexed row and column addresses which are driven onto the RAM where they are latched to form a cell selection. The timing of the multiplexer is controlled by a signal called $\overline{MUX}$ unless the memory is doing a refresh cycle whereupon the refresh address is driven onto the RAM address lines.

Address A11 and A12 are fed into a two to four line decoder to form a row select which determines which row of RAMS receives a $\overline{RAS}$.

Addresses A10 - A13 are used in two hour bit magnitude comparators to determine the area in which the memory is mapped and therefore selected. One comparator is set with A > B and the other with A < B where the A input is the address with the B input switchable high or low via switches. Therefore the memory is only selected when A > B on Comparator I (IC118) and A < B on Comparator II (IC119); for further information see the memory mapping section.

10.3 REFRESH LOGIC

Dynamic RAMS require all there rows to be addressed every 2 mS and as there are 128 rows this means for a distributed refresh one row is to be refreshed every 15 µ Sec. if data is not to be lost.

This can be achieved in one of three ways.

(1) Leave control of refresh to the on board timer and refresh arbitration Logic with External Refresh signal (EXT.REF) on P1/77 disconnected.

This will result in a distributed refresh cycle every 15 µS controlled by the LS123 which makes up the timer, this then clocks a D type latch which sends out a Refresh Request (REF REQ) and goes into a latch the other side of which is Memory Request (M REQ)), so dependent on whether REF RFQ or MREQ arrives first depends on whether a refresh cycle is completed before the memory cycle or after it. At the end of the RAS only refresh cycle a counter is clocked which increments the refresh address before releasing Memory Busy to allow another cycle.

(2) This gives the driver of the board control of refresh as long as the board gets a refresh at least once every 15 µS otherwise the board initiates a refresh cycle.

This is achieved by connecting EXT.REF. into Pin 1 of IC 109 of LS123 and Pin 13 of IC 111, the LS32 to clock REF REQ; under these conditions EXT REF is held normally low, going high to initiate a refresh but if the EXT.REF has been low for 15 µSec., then the board will initiate its own.

(3) This totally handsover refresh control of the board to the EXT.REF. signal with IC109 Pin 1 held high and disables the timing circuit.

Then by connecting EXT.REF. into IC111 Pin 13 means that on each rising edge of EXT.REF. initiates a refresh cycle and counts up the refresh addresses so long as there are 128 cycles per 2 mS no data loss will occur.

10.4 DATA CONTROL

When the memory receives a command signal such as $\overline{\text{MRDC}}$ or $\overline{\text{MWTC}}$ it always initiates the same Read Modify Write cycle, the only difference is in the data control, for instance in a 16 bit read cycle the data from the RAMS (EDC and data) passes through the Error Detection and correction (EDC) device where it is corrected and is passed out onto the bus, it is also turned round and written back into the memory (16 bit), ie. on a read cycle corrected data is written back into the read location .

During a write cycle data is still read out of the RAMS but is not allowed out on the bus and the new write data passes into the EDC device which is in the write mode and therefore generates new EDC data and passes all the data through to the RAMS to be written into on the write part of the cycle.

On an (8 bit) or byte read which is controlled by A0 and $\overline{\text{BHEN}}$ where $\overline{\text{BHEN}}$ is high then A0 controls which 8 bits of the memory is read or written to.

For example in a byte read the whole word is read as a 16 bit read but this time only 8 bits are allowed out either straight out for Data 0 - 7 or byte swapped from 8 - 15 into Data 0 - 7 output.

However for a byte write the memory reads the 16 bit word with EDC check bits and corrects it, then one EDC device is put into the read mode and the other with the new 8 bits of write data on its input into the write mode. Then the new word consisting of 8 bits of read corrected data and 8 bits of new write data generate the 6 EDC check but data and the whole word is written into the memory thus completing the cycle.

10.5 TIMING CONTROL

The on board timing is controlled via delay lines, this is used to generate the command signal for the RAM's such as $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{MUX}$.

It is also used to generate the output signals such as $\overline{AACK}$, $\overline{XACK}$ and is used to strobe the multi error and single error line to determine whether a single or multibit error has occurred. The delay lines are either driven by a command signal, Read or Write or by a Refresh cycle with the Busy timer and refresh arbitration logic making sure that only one signal passes down the line at a time.

10.6 ERROR DETECTION AND CORRECTION

This is controlled by two Fujitsu MB1412A, each of which control 8 bits of data but are interconnected to form a 6 bit check bit output for the 16 bit word.

Each device has separate Read (RDO-7) and Write (WDO-7) data in as well as corrected data (DO-7) out and this is controlled by means of a single line STB. If STB is a logic low the chip is in the read function and data and check bit (S10-15) are read in and corrected data and syndrone (SO-5) outputed as well as indication whether a single bit error has occurred $\overline{RET}$ or an error has occurred in the check bit $\overline{RVC}$. (The decode of the syndrone is shown in Appendix 1).

If the STB is a logic high the chip is in the write mode and the data on the write input (WDO-7) is outputed onto the data out (DO-7) along with the check bit output (CO 0-5). The devices together correct any single bit error in data or EDC bits giving indication that a single bit error has occurred (by means of a small amount of external logic). It is also able to detect any double bit error but does not attempt to correct them. (An indication of which memory device is failing is given in the syndrone data, for information on how to decode this see fault finding).

11. FAULT FINDING

The Plessey PSM512 memory is designed as a plug in item and faulty modules should be returned to Plessey for repair.

However in order to aid the turn round of repaired modules an indication of the fault symptom is invaluable, especially when the fault is intermittent or marginal.

In order to aid diagnosis, logic diagrams are provided in the handbook together with a description of the memory system, and the following syndrone decoding chart will help in detecting any single bit errors.

The syndrone outputs appear on IC112 as listed below and this is only valid on the read half of a cycle and not on a refresh cycle, a useful strobe when the syndrone is valid is on IC111 Pin 8.

S0 is on IC112/2
S1 is on IC112/1
S2 is on IC112/13
S3 is on IC112/3
S4 is on IC112/5
S5 is on IC112/4

DATA BIT	S0	S1	S2	S3	S4	S5	ERROR	
	1	1	1	1	1	1	NONE	
0	1	1	1	0	0	0	0	
1	0	1	1	0	0	1	1	
2	1	0	1	0	0	1	2	
3	0	0	1	0	1	1	3	
4	1	1	0	0	0	1	4	
5	0	1	0	0	1	1	5	
6	1	0	0	0	1	1	6	
7	0	0	0	0	0	1	7	DATA BITS
8	1	1	0	0	1	0	8	
9	0	1	0	1	1	0	9	
10	1	0	0	1	1	0	10	
11	0	0	1	1	1	0	11	
12	1	1	0	1	0	0	12	
13	0	1	1	1	0	0	13	
14	1	0	1	1	0	0	14	
15	0	0	0	1	0	0	15	
SYNDROME BIT								
0	0	1	1	1	1	1	16	
1	1	0	1	1	1	1	17	
2	1	1	0	1	1	1	18	EDC BITS
3	1	1	1	0	1	1	19	
4	1	1	1	1	0	1	20	
5	1	1	1	1	1	0	21	

The error column gives the RAM ROW numbered from right to left looking from the connector, and any other combination indicates a multiple error.

12. INSTALLATION AND OPERATION

This sections unpacking, installation and operating instructions for the Plessey PSM512 memory.

12.1 RECEIVING INSPECTION

The PSM512 memory is fully assembled and tested prior to shipment from the factory. The units are individually packed in accordance with standard practices for electronic equipment. Every precaution is taken to ensure that each system leaving the factory is complete and ready for installation. However it is recommended that units be inspected upon receipt for shipping damage.

12.2 INSTALLATION

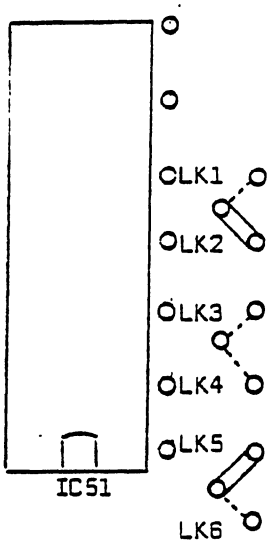
The memory is designed for mounting in a card cage and to plug into printed circuit board connectors. The interface connector pin assignment is shown on Pages 21 and 22. The PSM512 has a number of user options available, for details see Section 9 of this document. Prior to installation in the card cage check that the appropriate options have been set up.

12.3 POWER REQUIREMENT

The memory only has one power rail of +5V, this should be $\pm$ 5% and a check should be made that the board pin assignment coincides with the backplane.

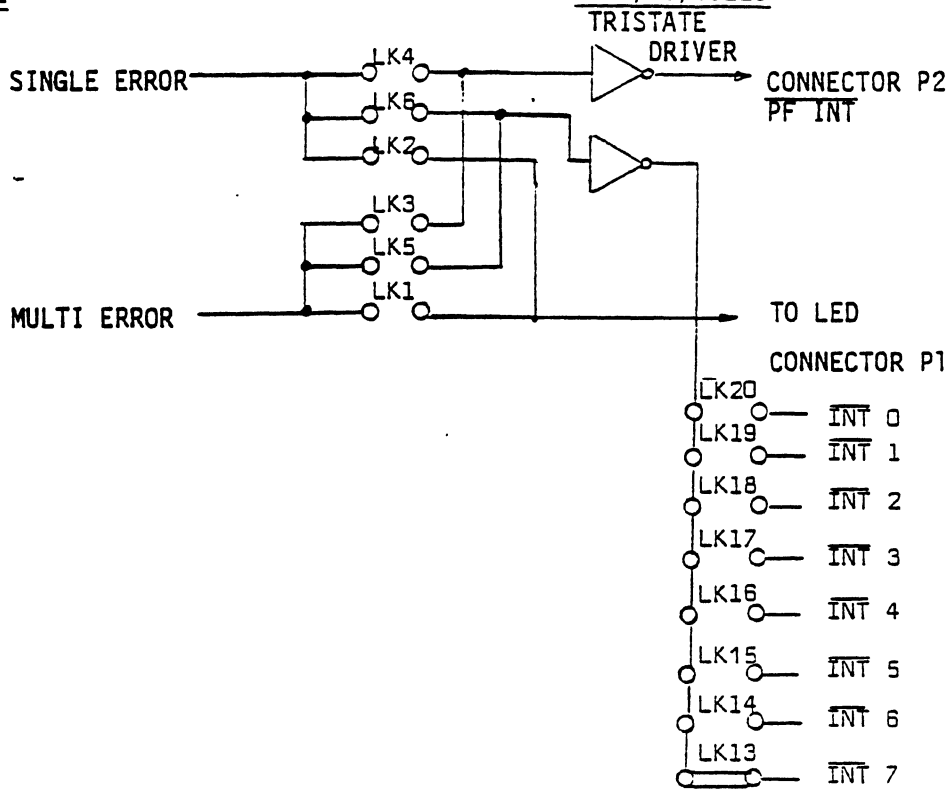
APPENDIX 1

APPLIES TO 421/MB/10226/ALL VARIANTS - ISSUE 2 ONLY



INTERRUPT LINKS
P.C.B. COMPONENT SIDE

421/HB/10225



INTERRUPT CIRCUIT

Links LK2 and LK5 fitted on shipment.

Link LK1 fitted connects Multi-error to LED Indicator.

Link LK2 fitted connects Single-error to LED Indicator.

It is not permissible to fit both LK1 and LK2.

Link LK3 fitted connects Multi-error to Power Fail Interrupt Line.

Link LK4 fitted connects Single-error to Power Fail Interrupt Line.

Do not fit both LK3 and LK4.

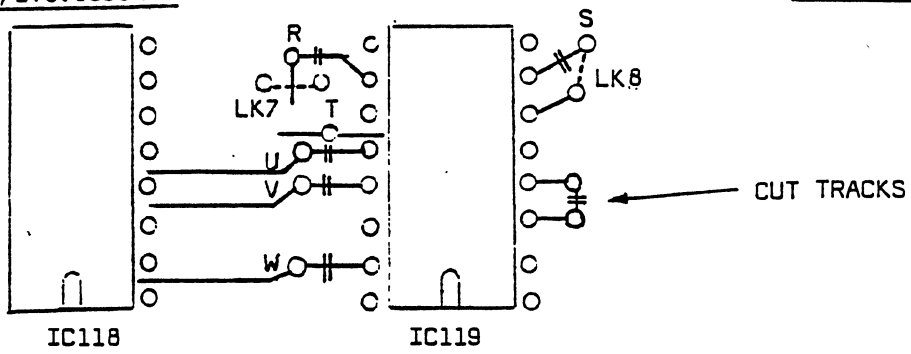
Link 5 fitted connects Multi-error to Interrupt Bus.

Link 6 fitted connects Single-error to Interrupt Bus.

Do not fit both LK5 and LK6.

NOTE:- If connection to PF Interrupt is not used it is advisable to tie the input to the tri-state driver to 0V to ensure the PF line is held at logic high when the memory card is selected.

FIGURE 1: INTERRUPT FACILITIES



Cut track as shown adjacent R.U.V.W.S. and IC119 3.4.

Fit wire Link LK8.

Connect wires from:

IC119/10	to AA	Connector P2.	Pin 57
IC119/12	to Y	Connector P2.	Pin 58
IC119/13	to Z	Connector P2.	Pin 55
IC119/15	to X	Connector P2.	Pin 56

Connect IC119 Pins 2 and 3 on solder side.

This configures 512K to the lower half of the 1 megabyte.

To configure 512K to the top half of the 1 megabyte, cut track as shown, adjacent T. Add link 7.

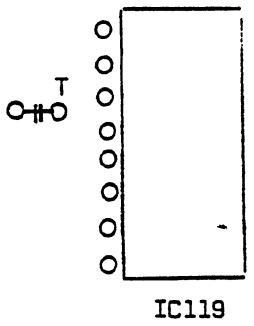


FIGURE 2: 16 MEGABYTE MEMORY MAPPING

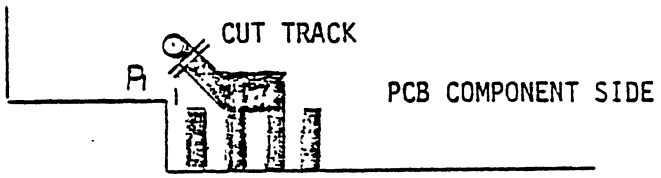
9.3 Refresh

Jumper links LK23 and LK24 control the refresh circuitry. These are located adjacent to connector P1 Pins 75, 77 and 79. For on board refresh jumper link LK21 is fitted. To control refresh externally LK24 is fitted.

9.4 Data Retention

If it is intended to use the auxiliary power supply for data retention purposes, the following actions are necessary:-

a) Cut track as shown.



b) Remove LK9 adjacent IC125 Pin 14.

c) Insert LK10 positioned below IC127.

9.5 Miscellaneous

9.5.1 A ACK Option

Jumper link LK12 connects A ACK to Multibus P1 connector Pin 25. If this facility is not required, then remove jumper link LK12.

9.5.2 Bus Priority

Although the memory cannot act as a Bus Master, the facility exists on the memory card to short BPRO to BPRIN by inserting link LK11. This enables the memory card, when plugged into a system with serial priority, to be positioned anywhere with the chassis.

SECURITY CLASSIFICATION

421/DA/10225/000
SHEET 1 OF 2

USED ON

THE PLESSEY COMPANY LIMITED
MICROSYSTEMS TOWCESTER

SIMILAR TO

SECURITY CLASSIFICATION

RECORDED BY

TITLE

512K x8 BIT MAX MEMORY

DRAWING NUMBER

421/DA/10225/000 SHEET 1 OF 2

MATERIAL

FINISH

TOLERANCES - UNLESS OTHERWISE STATED, GENERAL REQUIREMENT TO PLESSEY SPECIFICATION 2000/SP/A00000.

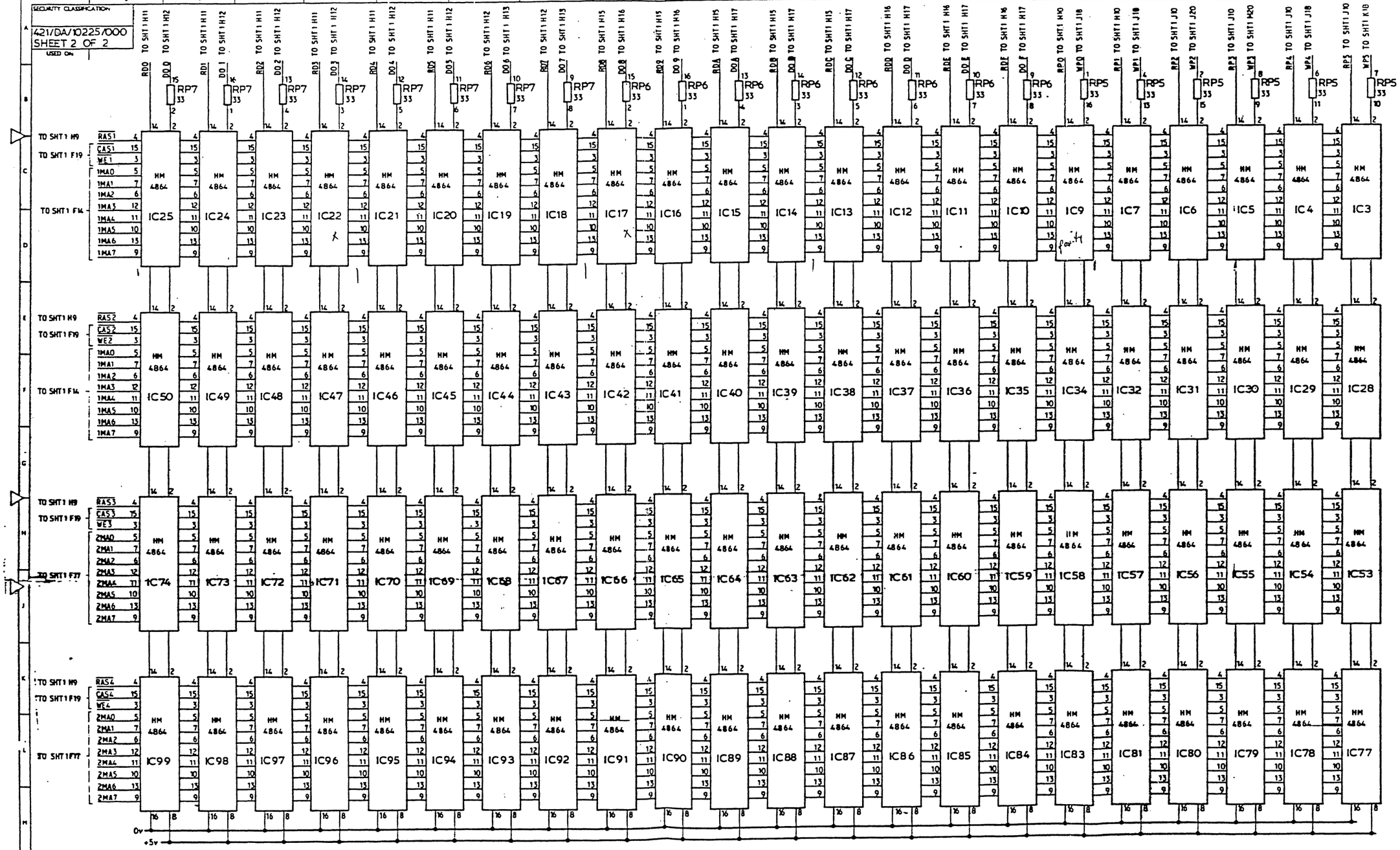
DIMENSIONS IN mm.

STATIONERY FORM P1131 JUNE 1975

SECURITY CLASSIFICATION

421/DA/10225/000
SHEET 2 OF 2

USED ON



DRN.	ISSUE No.	1	2
C.M.	DATE	21-6-81	13 10 81
CHKD	ISSUE No.	1	45/8916
D&A	MODIFIED		IV
APPD	SIZE	A1	

MATERIAL

FINISH

TOLERANCES - UNLESS OTHERWISE STATED.
GENERAL REQUIREMENT TO PLESSEY SPECIFICATION 2000/SP/GEN/01E.

DIMENSIONS IN mm

THE PLESSEY COMPANY LIMITED
MICROSYSTEMS TOWCESTER

TITLE

512K x 8 BIT MAX MEMORY

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SIMILAR TO

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SHEET 2 OF 2