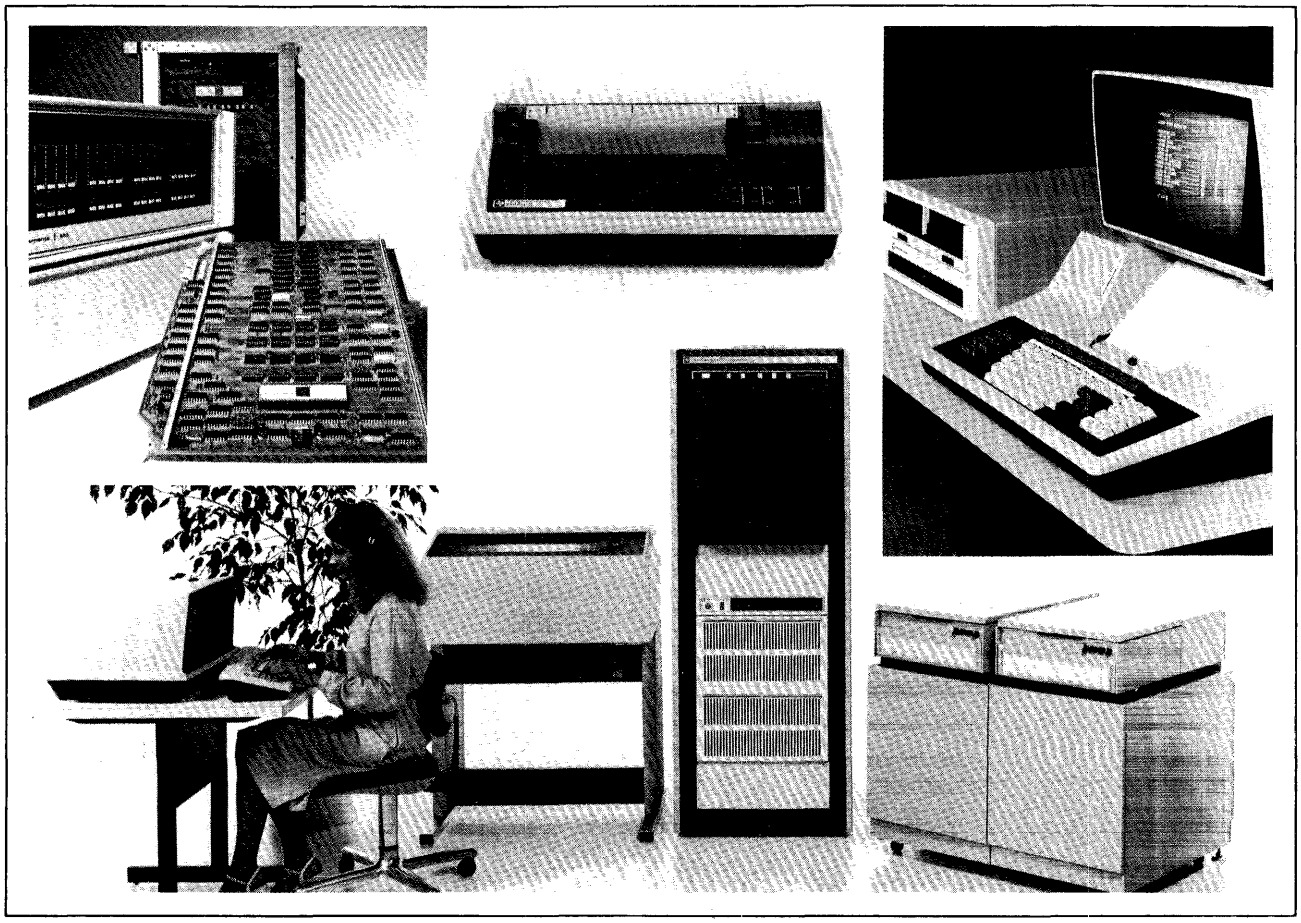
Model 990 Computer
X.21 Bit-Oriented/Character-Oriented Asynchronous Interface Module (X.21 BCAIM) Installation and Operation Manual



Part No. 2263883-9701 **
1 October 1982

TEXAS INSTRUMENTS

MANUAL REVISION HISTORY

Model 990 Computer X.21 Bit-Oriented/Character-Oriented/Asynchronous Interface Module (X.21 BCAIM) Installation and Operation Manual (2263883-9701)

Original Issue . . . . . 1 October 1982

The total number of pages in this publication is 202.

Preface

This manual contains the information necessary to install, program, and operate the X.21 bit-oriented/character-oriented/asynchronous interface module (X.21 BCAIM) in a Model 990 Computer or an expansion chassis. The information in this manual is organized into three major sections and six appendixes:

Section

1 General Description — Provides an overview of the purpose, features, and major components of the X.21 BCAIM, and general descriptions of the hardware and software.

2 Installation — Provides instructions for installing the X.21 BCAIM in a Model 990 Computer chassis or an expansion chassis.

3 Programming — Provides information needed to program and operate the X.21 BCAIM. Contains coding examples to aid the programmer in writing a device service routine (DSR) for the X.21 BCAIM.

Appendix

A BOP NRZI Protocol — Describes protocol-dependent parameters for the bit-oriented protocol BOP NRZI.

B BOP NRZ (Direct) Protocol — Describes protocol-dependent parameters for the bit-oriented protocol BOP Direct.

C BOP NRZI Protocol with Modem Clock — Describes protocol-dependent parameters for the bit-oriented protocol BOP Direct with clocking supplied by the modem.

D X.21 Switched Line Protocol — Describes protocol-dependent parameters for the X.21 Switched Line protocol.

E X.21 Switched Line State Flow — Provides flowcharts and describes the states involved in X.21 BCAIM operation on switched lines.

F X.21 Leased Line State Flow — Provides flowcharts and describes the states involved in X.21 BCAIM operation on leased lines.

The following documents contain information that may be helpful in troubleshooting and repairing the X.21 BCAIM.

Title	Part Number
X.21 Bit-Oriented/Character-Oriented/Asynchronous Interface Module Specification	2303089-9901
X.21 Bit-Oriented/Character-Oriented/Asynchronous Interface Module Maintenance Manual	2263884-9701
990 Computer Family CRU Specification	945105
Technical Aspects of Data Communication by John E. McNamara, Digital Equipment Corporation	
9900 Family Systems Design and Data Book, Microprocessor Series, First Edition	97049-118-NI
Model 990/10 Computer System Hardware Reference Manual	945417-9701
Model 990/10A Computer Maintenance Manual, General Description	2302633-9701
Model 990/12 Computer Maintenance Manual, General Description	2268239-9701
Model 990A13 Chassis Maintenance Manual, General Description	2308774-9701
Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide	943441-9701
Model 990 Computer Unit Diagnostics Handbook Volumes 1 through *6*	945400-9701 through 945400-9706
990 Family Communication Systems Field Reference Manual	2276579-9701
Model 990/12 Computer Assembly Language Programmer's Guide	2250077-9701

Contents

3 — Programming

Appendixes

Index

Illustrations

Tables

1

General Description

1.1 GENERAL

This section contains physical and functional descriptions of the Texas Instruments Model 990 Computer X.21 Bit-Oriented/Character-Oriented/Asynchronous Interface Module (X.21 BCAIM). This section also describes the interface between the host computer and the X.21 BCAIM and the interfaces between the X.21 BCAIM and supported communication devices.

Figure 1-1 is a photograph of the X.21 BCAIM board showing the arrangement of the connectors and components on the board.

1.2 PURPOSE OF EQUIPMENT

Connector P2 on the X.21 BCAIM provides an interface to allow communication between a host Model 990 Computer and devices that are compatible with the Electrical Industries Association (EIA) standard RS-232C and the Consultative Committee on International Telephone and Telegraph (CCITT) recommendation V.24. Connector P3 provides an interface between the host computer and devices that are compatible with CCITT recommendation X.21 or EIA standard RS-422. Connector P1 provides the interface between the communications register unit (CRU) of the host computer and the X.21 BCAIM.

In this manual, references to EIA or RS-232C are applicable to EIA standard RS-232C and the CCITT recommendation V.24. References to X.21 are applicable to CCITT recommendation X.21 and EIA standard RS-422.

The EIA interface at connector P2 provides full modem control and status capability for interfacing to leased-line or dial-up modems. The X.21 interface at connector P3 provides full data circuit terminating equipment (DCE) control and status capability for interfacing to a DCE on a leased or switched line. When you install the appropriate jumpers on the X.21 BCAIM board, you can use the X.21 interface at connector P3 for interfacing the host Model 990 Computer to an RS-422 local line (see Table 2-2). The RS-422 local line supports half-duplex or full-duplex, point-to-point communications. The RS-422 local line logic on the X.21 BCAIM is not electrically isolated from power and logic grounds. Any cable attached to the RS-422 interface should not exceed 15.2 meters (50 feet) in length.

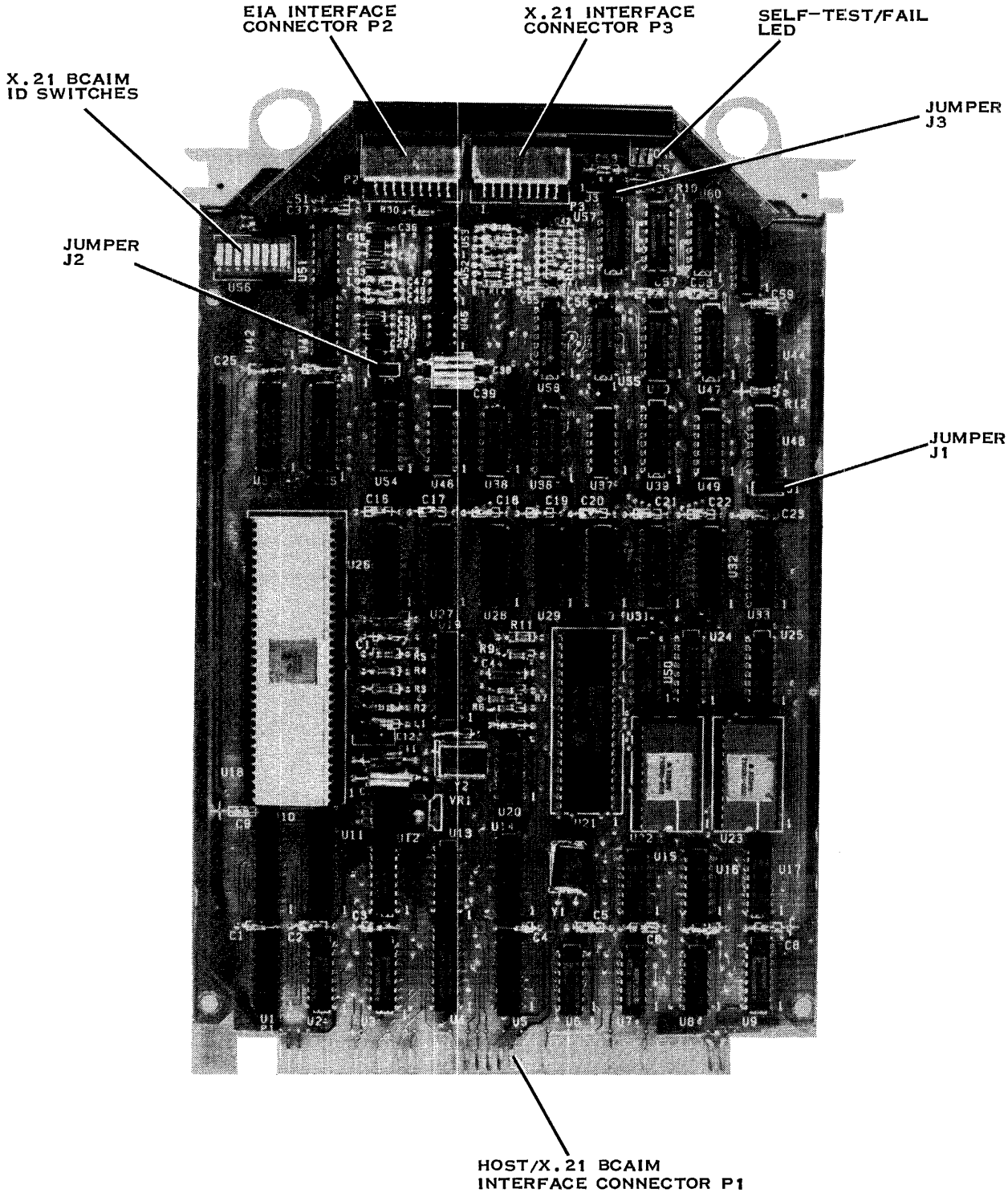


Figure 1-1. X.21 BCAIM Assembly

You can program the X.21 BCAIM to support synchronous, asynchronous, or isochronous* operation. When you program it for synchronous operation, it supports bit-oriented protocols such as Synchronous Data Link Control (SDLC), Advanced Data Communications Control Procedures (ADCCP), and High-Level Data Link Control (HDLC); however, it does not support the residue bit counts in the HDLC protocol. The X.21 BCAIM supports character-oriented protocols such as Binary Synchronous Communications (BSC or Bisync) and Digital Data Communications Message Protocol (DDCMP).

Some of the protocols mentioned in the preceding paragraph require you to download additional user-coded software to random-access memory (RAM) on the X.21 BCAIM for operation. The read-only memory (ROM) on the X.21 BCAIM contains message blocking, error detection, and cyclic redundancy check (CRC) generation routines as required to support the following:

- BSC (EBCDIC only) 3780/2780
- SDLC/HDLC bit-oriented protocols (the X.21 BCAIM does not support the residue bit counts in HDLC)
- X.21 call establishment and call reception protocol for switched X.21 operation (byte timing circuitry is not implemented on the X.21 BCAIM; therefore, it does not support selective direct call)
- X.21 leased-line operation
- Downloaded character detection routines

The X.21 BCAIM is capable of communicating at bit rates up to 9600 bits per second (bps) with synchronous or asynchronous protocols. Synchronous protocols can be externally or internally clocked. In most cases, synchronous protocols are externally clocked and asynchronous protocols are internally clocked. However, NRZI-encoded SDLC is one specific example of a synchronous protocol requiring either internal clocking or external modem clocking when it is used on the X.21 BCAIM. NRZ-encoded or direct-encoded SDLC uses the external modem clock.

1.3 PHYSICAL DESCRIPTION

The X.21 BCAIM is implemented on a half-size 990 printed circuit board (PCB) as shown in Figure 1-1. It requires one half-slot location in the host Model 990 Computer or in a CRU expansion chassis. Bottom-edge connector P1 is an 80-pin male connector that provides the connection to the host computer. Connectors P2 and P3 are 18-pin male connectors that provide interfaces to supported communication devices via the appropriate cables.

The major components on the X.21 BCAIM are:

- One TMS 9900 microprocessor with a clock driver
- One TMS 9901 programmable systems interface

* This term describes the process of transmitting and receiving asynchronous data using a clocking connection between the transmitter and receiver.

- One TMS 9903 synchronous communications controller
- 16K bytes of ROM
- 4K bytes of static RAM
- One COM 8116 baud-rate generator
- One set of eight pencil switches
- One self-test/fail light-emitting diode (LED) indicator
- EIA and X.21 interface circuitry
- CRU interface logic
- Three jumpers for network/system selection

1.3.1 Equipment Supplied

Table 1-1 lists the available X.21 BCAIM kits.

Table 1-1. X.21 BCAIM Kits

Kit Part Number	Kit Name and Contents
2303091-0001	Model 990 Computer/X.21 BCAIM interface kit 1 X.21 BCAIM, part number 2303085-0001 1 Installation and operation manual, part number 2263883-9701 1 System test procedure, part number 2303095-9901
2303091-0002	Model 990 Computer/X.21 BCAIM/Bell data set interface kit 1 X.21 BCAIM, part number 2303085-0001 1 Cable, EIA connector to external modem, 9.1 meters (30 feet), part number 2303070-0002 1 Installation and operation manual, part number 2263883-9701 1 System test procedure, part number 2303095-9901
2303091-0003	Model 990 Computer/X.21 BCAIM/X.21 network interface kit 1 X.21 BCAIM, part number 2303085-0001 1 Cable, X.21 connector to external DCE, 9.1 meters (30 feet), part number 2303094-0002 1 Installation and operation manual, part number 2263883-9701 1 System test procedure, part number 2303095-9901

A documentation kit, part number 2263893-0001, is available for your use with the X.21 BCAIM. The kit contains the following:

- A microfiche listing of the character detection routines in X.21 BCAIM ROM
- An index for the microfiche listing
- This installation and operation manual

1.3.2 X.21 BCAIM Cables

Table 1-2 lists the cables available for use with the X.21 BCAIM.

Table 1-2. X.21 BCAIM Cables

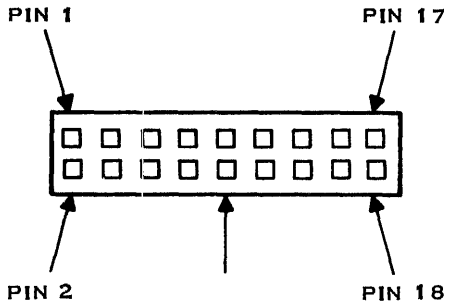
Cable Part Number	Cable Description
2303096-0001	EIA connector (P2) to internal modem, 0.5 meters (1.5 feet)
2303070-0002	EIA connector (P2) to external modem, 9.1 meters (30 feet)
2303070-0003	EIA connector (P2) to external modem, 3.0 meters (10 feet)
2303094-0001	X.21 connector (P3) to external DCE, 3.0 meters (10 feet)
2303094-0002	X.21 connector (P3) to external DCE, 9.1 meters (30 feet)

You can fabricate your own cables for interfacing the X.21 BCAIM to an RS-422 local line. Table 1-3 lists the part numbers of the housing and component parts (covers, crimp-type contacts, and polarization plugs) of a connector that mates with P3 on the X.21 BCAIM. The connector comes with contacts intended for machine crimping. Discard these contacts and use the contacts listed in Table 1-3 to assemble the connector. Refer to the illustration at the bottom of Table 1-3 for the pin number arrangement in the connector. Disregard the AMP pin numbers printed on the connector.

The recommended cable for fabricating half-duplex local line cables is a 22 or 24 AWG twisted, shielded pair, Belden 8761 or equivalent. For full-duplex applications, a four-conductor cable such as Belden 8723 or equivalent is recommended. Figure 1-4 shows the pin connections for the P3 end of an RS-422 local line.

Table 1-3. RS-422 Local Line Cable Connector Components

Component	TI Part Number	Alternate Source Part Number
Connector housing	2211973-0027	AMP 102398-0007
Connector covers (two required per connector)	2220301-0001	AMP 102396-0007
Polarization plug	0972901-0001	AMP 87077-0001
Crimp contacts	2210248-0002	AMP 87667-0001



2280247

1.4 HARDWARE FUNCTIONAL DESCRIPTION

Figure 1-2 is a functional block diagram of the X.21 BCAIM showing how the major components and areas of logic interconnect. The following paragraphs present a brief description of the function of each major component or area of logic.

1.4.1 Host CRU Control Logic

In Figure 1-2, the block of logic labeled host CRU control logic buffers all signals entering the X.21 BCAIM from the host computer. This block of logic determines whether the host computer is reading information from the X.21 BCAIM or writing information to it, and it generates the necessary strobes and enables. Logic in this block also controls timing of read and write operations and uses inputs from the other logic on the board to determine when to interrupt the host.

1.4.2 Host CRU Data Logic

The host CRU data logic includes logic to decode control information and commands or data from the host. The decoded control information passes back to the host CRU control logic where it is used in setting up bits or interrupts for firmware. It places decoded commands and data on the microprocessor parallel data bus for the TMS 9900 to process as required. The host CRU data logic also includes registers and multiplexers used to multiplex parallel data or status information onto the serial CRUBITIN line to be routed to the host computer.

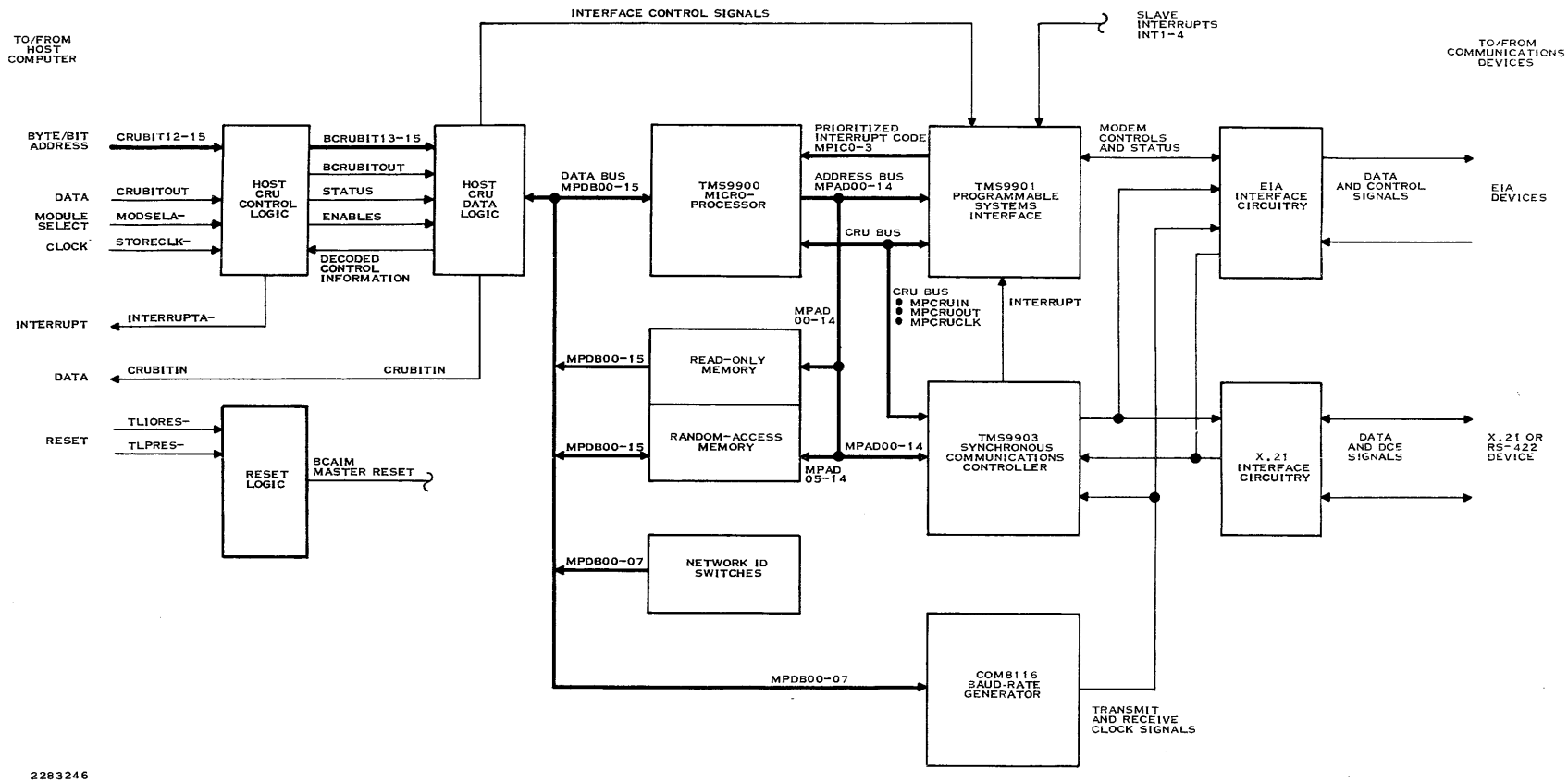


Figure 1-2. X.21 BCAIM Functional Block Diagram

1.4.3 TMS 9900 Microprocessor

The TMS 9900 microprocessor chip is the processor on the X.21 BCAIM board. Guided by instructions in ROM firmware, the microprocessor interprets requests from the host computer and executes the appropriate ROM-resident routine to process the requests. Routines to direct the TMS 9900 are coded into ROM on the X.21 BCAIM where they are accessed when a command from the host computer causes the TMS 9900 to address the appropriate routine. Instructions from the addressed routine are placed on the microprocessor data bus for the TMS 9900 to read and execute. When you download code to the RAM on the X.21 BCAIM, the TMS 9900 obtains instructions from the RAM in the same manner.

The TMS 9900 handles and routes all data entering the X.21 BCAIM board from the host computer or from the remote communication device. It routes data coming from the host to be transmitted to the remote device to RAM for temporary storage, retrieves it from RAM at the proper time, and places it on the TMS 9900's MPCRUOUT line. It then routes the data to the TMS 9903 and transmits it to the remote device via the EIA or X.21 interface circuitry.

Data coming from the remote device arrives via the EIA or X.21 interface circuitry, is routed to the TMS 9903, and then to the TMS 9900 via the MPCRUIN line. The TMS 9900 then transfers the data to RAM for temporary storage. The host empties this storage area to ensure that enough X.21 BCAIM RAM space is available for incoming communication line data.

1.4.4 Read-Only Memory (ROM)

The 16K bytes of ROM on the X.21 BCAIM contain the firmware instructions used by the TMS 9900 in processing requests from the host computer. Routines stored in ROM include those needed to provide message blocking, error detection, CRCs, character detection routines for supported protocols, and instructions for the TMS 9900.

1.4.5 Random-Access Memory (RAM)

The 4K bytes of static RAM on the X.21 BCAIM are used for temporary storage of data, as working registers for the microprocessor, as storage space for downloaded character detection routines, and as general read/write memory. All data transfers to or from RAM are via the 16-bit parallel data bus. All data entering the X.21 BCAIM is routed through the microprocessor before being placed in RAM for storage. All data leaving RAM is routed to the microprocessor where it is transferred to its destination by the microprocessor.

1.4.6 TMS 9901 Programmable Systems Interface

The TMS 9901 accepts and prioritizes interrupts from the TMS 9903 and other logic on the board. The TMS 9901 encodes the interrupts and passes the interrupts on to the TMS 9900 in the order of their priority. It also provides an X.21 signal timer and is responsible for some of the modem control and status signals.

1.4.7 TMS 9903 Synchronous Communications Controller

The TMS 9903 controls the interface between the X.21 BCAIM and the communication line. You can program it to provide or support the following:

- Synchronous, asynchronous, or isochronous operation
- Character-oriented or bit-oriented protocols
- Five, 6, 7, or 8-bit characters

- CRC generation and checking
- Two programmable sync registers
- Even, odd, or no parity
- Automatic zero insertion and deletion for bit-oriented protocols
- One or two stop bits for asynchronous operation
- Programmable internal clock rate from 50 bps to 9600 bps

The TMS 9903 operates with the EIA and X.21 interface logic and provides the interface to communication devices or communication lines at connectors P2 and P3.

1.4.8 COM 8116 Baud-Rate Generator

The COM 8116 baud-rate generator supplies transmit and receive clock signals to the TMS 9903 and the interface circuitry when you operate the X.21 BCAIM in the asynchronous mode. When you operate it in the synchronous mode, the modem normally supplies the clock signals. One type of NRZI-encoded SDLC protocol is an exception to the preceding statement. It is a synchronous protocol but it requires internal clocking from the COM 8116 when it is used on the X.21 BCAIM. You can program the COM 8116 to support transmit and receive rates from 50 bps to 9600 bps.

1.4.9 X.21 BCAIM ID Switches

The X.21 BCAIM ID switches consist of a set of eight pencil switches which you can set to produce a two-digit hexadecimal identification code for the board. The processor reads the two-digit hexadecimal code when the host issues the appropriate command.

The ID switches can be used to establish an ID for the X.21 BCAIM when you use it on a polled communications network or for any other purpose compatible with the system software.

1.4.10 EIA Interface Circuitry

The EIA interface circuitry, along with the TMS 9901 and the TMS 9903, provides an EIA RS-232C or CCITT V.24 compatible interface between the logic on the X.21 BCAIM and a communication device such as a modem. The EIA interface logic provides data input and output connections, as well as modem control and status signals. The EIA interface circuitry is capable of half-duplex or full-duplex operation at speeds up to 9600 bps.

1.4.11 X.21 Interface Circuitry

The X.21 interface circuitry works with the TMS 9901 and TMS 9903 to provide an interface that is compatible with CCITT recommendation X.21 and EIA standard RS-422. The X.21 interface circuitry supports full-duplex operation at speeds up to 9600 bps. Only the RS-232C and RS-422 modes of operation support half-duplex operation. X.21 is full-duplex; however, it is possible to run some half-duplex protocols over a full-duplex line.

1.4.12 Reset Logic

The reset logic accepts reset signals from the host computer and generates a master reset signal for the BCAIM logic.

1.5 X.21 BCAIM INTERFACES

The left side of Figure 1-3 illustrates the signals that provide the interface between the X.21 BCAIM and the CRU of the host computer. The right side of Figure 1-3 shows the signals that provide the EIA and X.21 interfaces between the board and compatible communication devices. The following paragraphs provide details of these interfaces.

NOTE

The X.21 BCAIM will not support both EIA and X.21 devices at the same time. Connection to both ports of the X.21 BCAIM can result in unpredictable operation.

1.5.1 X.21 BCAIM to Host Computer Interface

Install the X.21 BCAIM board in either the host computer chassis or a CRU expansion chassis where it can obtain power and share access to the host computer's CRU with other CRU-controlled devices. Section 2 presents instructions for installing the X.21 BCAIM in the host or expansion chassis, assigning interrupts, and so forth. The X.21 BCAIM/host CRU interface conforms to the requirements of the *990 Computer Family CRU Specification*, part number 945105. Table 1-4 lists the connector pin assignments and the functions of the X.21 BCAIM/host CRU interface signals.

1.5.2 X.21 BCAIM to Communication Device Interface

Connector P2 provides the EIA interface between the X.21 BCAIM and compatible communication devices. The interface signals at connector P2 conform to EIA standard RS-232C and to CCITT recommendation V.24. The EIA interface circuitry has the following characteristics:

- The receiver circuitry can withstand ±25 volts.
- The drivers are limited to ±6 volts.
- A positive voltage equals binary zero, signal space, or control on.
- A negative voltage equals binary one, signal mark, or control off.
- A positive voltage is a voltage greater than +3 volts.
- A negative voltage is a voltage more negative than −3 volts.

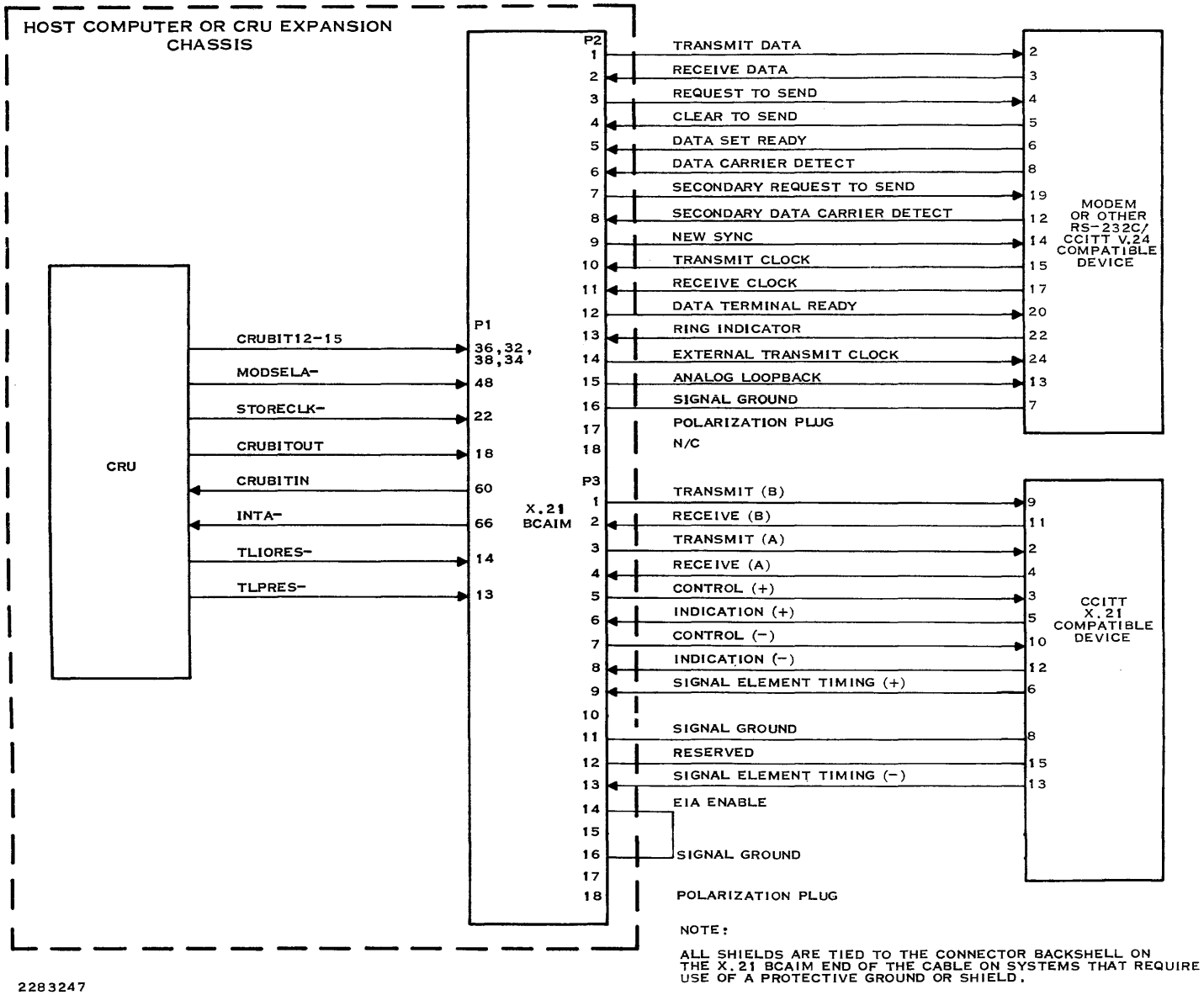


Figure 1-3. X.21 BCAIM Interfaces

Table 1-4. X.21 BCAIM/Host CRU Interface Signals

Signature	Pin Number	Function
CRUBIT12 CRUBIT13 CRUBIT14 CRUBIT15	P1-36 P1-32 P1-38 P1-34	CRUBIT12 through CRUBIT15 are decoded on the X.21 BCAIM to determine which bit of the 16-bit interface word the host is addressing.
MODSELA-	P1-48	The true state (low) of MODSELA- selects an individual CRU module such as the X.21 BCAIM.
STORECLK-	P1-22	STORECLK- (when low) indicates that a write operation is being performed. The selected module responds to this command by reading the CRUBITOUT on the positive edge of STORECLK-.
CRUBITOUT	P1-18	CRUBITOUT is the serial data signal for transferring information from the host computer to the X.21 BCAIM.
INTA-	P1-66	INTA- is the signal the X.21 BCAIM uses to interrupt the host computer when it needs interrupt service.
TLIORES-	P1-14	TILINE Input/Output Reset (TLIORES-) is the signal the host computer uses as a master reset for the X.21 BCAIM.
TLPRES-	P1-13	TILINE Power Reset (TLPRES-) is a signal the host computer power supply generates when power starts to fail and until voltages are stable during power-up.
CRUBITIN	P1-60	CRUBITIN is the serial data signal for transferring information from the X.21 BCAIM to the host computer.

Connector P3 provides the interface between the X.21 BCAIM and devices that operate in accordance with CCITT recommendation X.21 or EIA standard RS-422. The X.21 interface circuitry has the following characteristics:

- The receiver circuitry can withstand a common-mode voltage of ±7 volts.
- The drivers are limited to a differential voltage of ±6 volts.
- A positive differential voltage equals binary zero, signal space or control on.
- A negative differential voltage equals binary one, signal mark, or control off.

- A positive voltage is a differential voltage of +200 millivolts to +6 volts.
- A negative voltage is a differential voltage of −200 millivolts to −6 volts.

When you use connector P3 to interface the X.21 BCAIM to an RS-422 local line, use the pin assignments shown in Figure 1-4. Refer to paragraph 1.3.2 for information on the recommended cable and connectors for fabricating local line cables. The recommended maximum length of the RS-422 local line cable is 15.2 meters (50 feet). Operation with longer cables is often possible, depending upon the type of terminal, the type of cable, the speed of data transmission, and the electrical environment. Cables longer than 15.2 meters can often be used satisfactorily when the computer and the terminal are both located in the same building in a reasonably quiet environment.

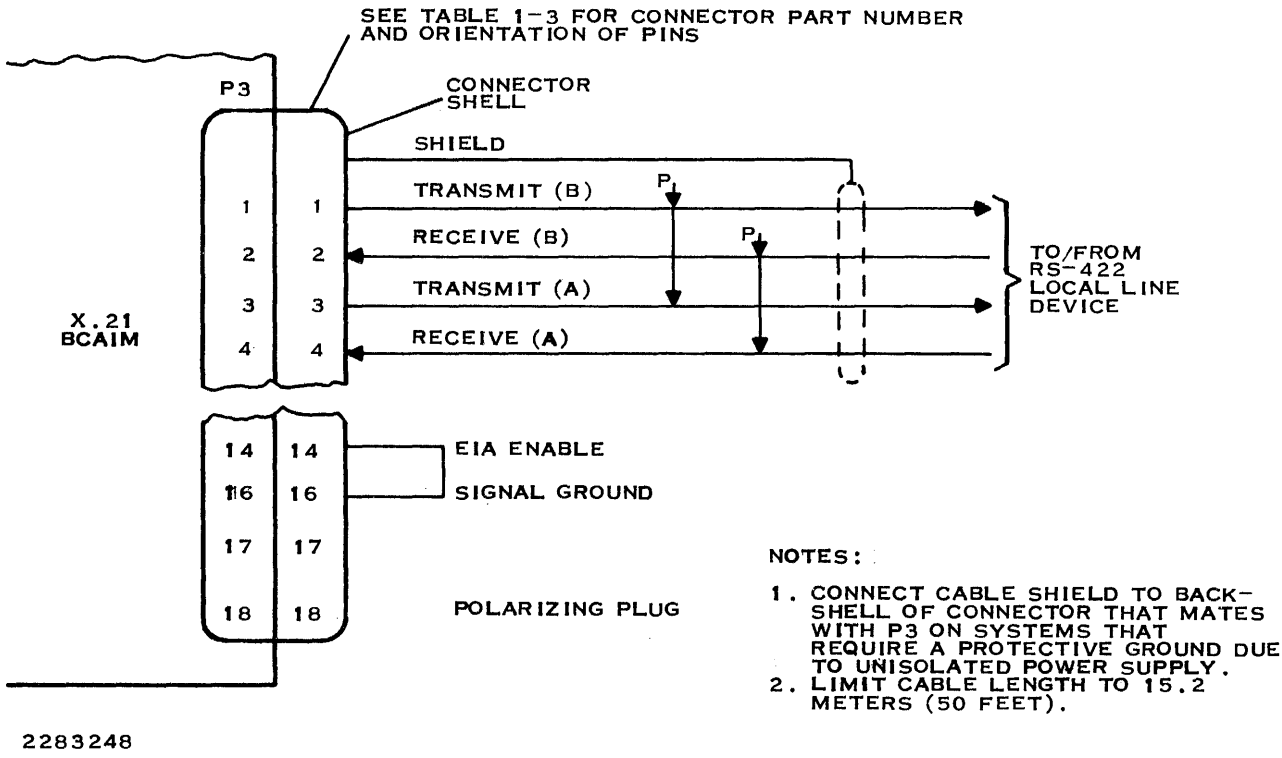


Figure 1-4. RS-422 Local Line Connections

Table 1-5 lists the connector pin assignments and the functions of the EIA signals at connector P2. Table 1-6 lists the connector pin assignments and the functions of the X.21 signals at connector P3. The EIA and CCITT designations for equivalent circuit functions are listed beside each pin where an equivalent function exists. Tables 1-7 and 1-8 present detailed descriptions of the EIA and X.21 interface signals.

Table 1-5. EIA Interface Connector (P2) Pin Assignments

Pin Number	CCITT	EIA	Function
1	103.0	BA	Transmit data
2	104.0	B	Receive data
3	105.0	CA	Request to send
4	106.0	CB	Clear to send
5	107.0	CC	Data set ready
6	109.0	CF	Data carrier detect
7	120.0	SCA	Secondary request to send
8	122.0	SCF	Secondary data carrier detect
9	—	—	New sync
10	114.0	DB	Transmit signal element timing
11	115.0	DD	Receive signal element timing
12	108.2	CD	Data terminal ready
13	125.0	CE	Ring indicator
14	113.0	DA	Transmit signal element timing (external)
15	—	—	Analog loopback
16	102.0	AB	Signal ground
17	—	—	Polarizing plug
18	—	—	Spare

Note:

Refer to Table 1-7 for detailed descriptions of the EIA interface signals.

Table 1-6. X.21 Interface Connector (P3) Pin Assignments

Pin Number	CCITT X.21	Signal Function
1	T(B)	Transmit B
2	R(B)	Receive B
3	T(A)	Transmit A
4	R(A)	Receive A
5	C(A)	Control plus
6	I(A)	Indication plus
7	C(B)	Control minus
8	I(B)	Indication minus
9	S(A)	Signal element timing plus
10	—	External signal element timing plus
11	G	Signal ground
12	—	Reserved
13	S(B)	Signal element timing minus
14	—	EIA enable
15	—	External signal element timing minus
16	G	Signal ground
17	—	Not used
18	—	Polarizing plug

Note:

Refer to Table 1-8 for detailed descriptions of the X.21 interface signals.

In Tables 1-7 and 1-8, the letters and numbers in parenthesis under the signal name are the CCITT and EIA designations for the equivalent circuit where equivalent circuits exist. The direction of information flow is indicated where applicable.

Table 1-7. EIA Interface Signal Descriptions

Signal Name	Connector/ Pin	Function
Transmit data (BA, 103) X.21 BCAIM to modem	P2-1	The X.21 BCAIM generates data signals on this circuit that are transferred to the modem for transmission of data to the remote data terminal. This circuit is held in the marking condition (logic 1 state) during intervals between characters and at all times when no data is being transmitted. The following four signals must be on before data is transmitted: Request to send (CA) Clear to send (CB) Data set ready (CC) Data terminal ready (CD)
Receive data (BB, 104) Modem to X.21 BCAIM	P2-2	The modem generates signals on this circuit in response to data signals it receives from the remote terminal. This circuit is held in the marking condition at all times when the circuit receive line signal detect (CF) is off. On a half-duplex channel, the modem holds this circuit in the marking condition when circuit request to send (CA) is on and for a brief interval following the on to off transition of request to send (CA).
Request to send (CA, 105) X.21 BCAIM to modem	P2-3	This circuit conditions the modem for data transmission and, on a half-duplex channel, controls the direction of data transmission. A transition from off to on instructs the modem to enter the transmit mode. The modem responds by turning on the transmitter and transmitting a mark condition for a preselected interval. It then turns on clear to send (CB), indicating data can be transferred to the modem via circuit transmit data (BA). The on to off transition of this circuit instructs the modem to complete transmission and to turn off the transmitter. A synchronous modem transmits the last bit combination required to complete its encoded data transmission scheme and turns off the transmitter. An asynchronous modem with soft carrier turn-off selected transmits an out-of-band tone (900 Hz for a 202 modem) for a preselected time interval and then turns off the transmitter.
Clear to send (CB, 106) Modem to X.21 BCAIM	P2-4	This circuit indicates to the X.21 BCAIM that the modem is ready to transmit data received on circuit transmit data (BA). The on to off and off to on transitions of this circuit are in response to transitions on circuit request to send (CA).

Table 1-7. EIA Interface Signal Descriptions (Continued)

Signal Name	Connector/ Pin	Function
Data set ready (CC, 107) Modem to X.21 BCAIM	P2-5	The on condition of this circuit indicates to the X.21 BCAIM that the modem is connected to a data channel and all control circuits are valid. The on condition indicates all of the following conditions have been met: 1. The local modem is connected to a data channel (off-hook in switched service). 2. The local modem is not in test, talk, or dial mode. 3. The local modem has completed any timing functions required by the switched system to complete call establishment. The circuit is in the off condition at all other times and informs the X.21 BCAIM to desregard all signals other than ring indicator (CE).
Receive line signal detect (CF, 109) Modem to X.21 BCAIM	P2-6	The on condition of this circuit indicates the modem is receiving a signal that meets its suitability criteria and the data on circuit receive data (BB) is valid. The off condition indicates that no signal is being received from the remote data terminal or that the receive signal is unsuitable for demodulation. On half-duplex channels, this signal is held off whenever request to send (CA) is on and for a brief interval after the on to off transition of request to send.
Secondary request to send (SCA, 120) X.21 BCAIM to modem	P2-7	The on condition of this signal requests the modem to transmit a tone on the secondary channel (also called the reverse channel, supervisory channel, or backward channel). TI internal modems do not provide this option.
Secondary data carrier detect (SCF, 122) Modem to X.21 BCAIM	P2-8	The on condition of this circuit indicates a tone is being received that meets the criteria of the secondary data channel. TI internal modems do not provide this option.
New sync X.21 BCAIM to modem	P2-9	This signal is biased to the off position.
Transmitter signal element timing (DB, 114) Modem to X.21 BCAIM	P2-10	Signals on this circuit provide the X.21 BCAIM with transmitter signal element timing information. The X.21 BCAIM provides signals on circuit transmit data (BA) in which transitions between signal elements nominally occur at the time of the transitions from the off to on condition of this circuit. The modem samples the data on circuit transmit data (BA) on the on to off transitions of this circuit.

Table 1-7. EIA Interface Signal Descriptions (Continued)

Signal Name	Connector/ Pin	Function
Receive signal element timing (DD, 115) Modem to X.21 BCAIM	P2-11	Signals on this circuit provide the X.21 BCAIM with received signal element timing information. The transition from on to off nominally indicates the center of each signal element on circuit receive data (BB). The modem provides signals on the receive data (BB) circuit in which transitions between signal elements nominally occur at the time of the transitions from off to on of this circuit.
Data terminal ready (CD, 108.2) X.21 BCAIM to modem	P2-12	Signals on this circuit control switching of the modem to the communication channel. The on condition prepares the modem to be connected to the communication channel and maintains a connection established by external means such as manual call origination, manual answering, or automatic call origination. TI internal modems and most external modems automatically answer an incoming call when circuit data terminal ready (CD) is turned on when a ringing signal is detected. The off condition of circuit data terminal ready (CD) causes the modem to be disconnected from the communication channel. After circuit data terminal ready (CD) is turned off in switched network applications, it cannot be turned on again until the modem turns off the circuit data set ready (CC).
Ring indicator (CE, 125) Modem to X.21 BCAIM	P2-13	The on condition of this circuit indicates that a ringing signal is being received on the communication channel. The on condition appears approximately coincidently with the on segment of the ringing signal.
Transmitter signal element timing external (DA, 113) X.21 BCAIM to modem	P2-14	Signals on this circuit provide the modem with transmitter signal element timing information. The X.21 BCAIM provides signals on the transmit data (BA) circuit in which transitions between signal elements nominally occur at the time of the transitions from the off to on condition of this signal. The modem samples the data on circuit transmit data (BA) on the on to off transitions of the circuit transmitter signal element timing (DB). You can program the X.21 BCAIM to provide the internal clock at this pin.

Table 1-7. EIA Interface Signal Descriptions (Continued)

Signal Name	Connector/ Pin	Function
Analog loopback X.21 BCAIM to modem	P2-15	The on condition of this circuit instructs modems that are capable of doing so to disconnect from the phone line and connect the transmitter output to the receiver input. For TI internal modems, all interface circuits except data set ready (CC) operate as in normal full-duplex mode. Data set ready (CC) is forced off while the modem is in analog loopback. This circuit allows the computer to exercise the X.21 BCAIM and the modem in a local test mode. The off condition of this circuit returns the modem to the normal mode.
Signal ground	P2-16	This circuit is the common ground for the EIA interface.

Table 1-8. X.21 Interface Signal Descriptions

Signal Name	Connector/ Pin	Function
Isolated ground	Backshell	The cable shield should be connected to the backshell of the connector that mates with P3 on the X.21 BCAIM on systems that require use of a protective ground.
Transmit (T) X.21 BCAIM to DCE	P3-1, P3-3	The X.21 BCAIM generates data signals on this circuit which are transferred to the DCE for transmission to a remote data terminal or an X.21 network. This circuit also transfers call information to the DCE to initiate or accept calls.
Receive (R) DCE to X.21 BCAIM	P3-2, P3-4	The DCE generates signals on this circuit in response to data signals received from the remote terminal and transfers them to the X.21 BCAIM. This circuit also transfers call information to the X.21 BCAIM to inform it to accept or initiate a call.
Control (C) X.21 BCAIM to DCE	P3-5, P3-7	The X.21 BCAIM generates signals on this circuit and transfers them to the DCE to signal the X.21 network of X.21 BCAIM state changes.
Indication (I) DCE to X.21 BCAIM	P3-6, P3-8	The DCE generates signals on this circuit and transfers them to the X.21 BCAIM to inform it of DCE state changes.

Table 1-8. X.21 Interface Signal Descriptions (Continued)

Signal Name	Connector/ Pin	Function
Signal element timing (S) DCE to X.21 BCAIM	P3-9, P3-13	Signals on this circuit provide the X.21 BCAIM with transmitter and receiver signal element timing information. The X.21 BCAIM provides signals on the transmit circuit (T) in which transitions between signal elements nominally occur at the time of the transitions from off to on condition of this signal. The DCE provides signals on the receive (R) circuit in which transitions between signal elements nominally occur at the time of the transitions from off to on condition of this signal. The X.21 BCAIM and the DCE sample data on circuits transmit (T) and receive (R) on the on to off transitions of the circuit signal element timing (S).
External signal element timing (ES) X.21 BCAIM to DCE	P3-10, P3-15	Signals on this circuit provide a loopback connector on the DCE with transmitter and receiver signal element timing information during diagnostic testing.
Signal ground (G)	P3-11	This signal is used when a zero-volt reference point between the X.21 BCAIM and the DCE is needed to reduce external signal interference.
	P3-12	Reserved.
EIA enable	P3-14	This signal is connected to pin 16 to indicate that an X.21 cable is connected to connector P3 on the X.21 BCAIM. The X.21 firmware senses this signal each time an Open or Write Parameters command is issued, and during power-up or reset operations.
Signal ground	P3-16	This signal is connected to pin 14. Refer to the description of EIA enable.

Note:

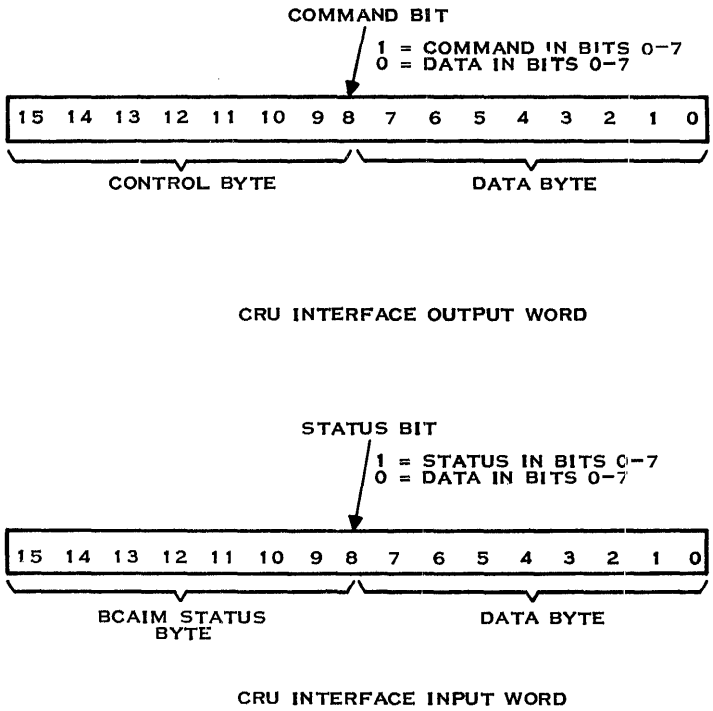
All signal circuits except EIA enable and signal ground are balanced differential circuits.

1.6 REQUEST PROCESSING OVERVIEW

Communications between the host computer and the X.21 BCAIM take place through the host computer's communications register unit (CRU). The CRU is a bit-serial interface capable of transferring from 1 to 16 bits with the load communications register (LDCR) and store communications register (STCR) instructions. The CRU also provides the capability of manipulating single bits with the set bit to zero (SBZ) and set bit to one (SBO) instructions or testing single bits with the test bit (TB) instruction.

The interface between the host computer and the X.21 BCAIM consists of one 16-bit CRU output word and one 16-bit CRU input word as shown in Figure 1-5. The CRU output word is used to convey eight bits of host CRU interface control information in bits 8 through 15, and eight bits of either data or command information from the host computer to the X.21 BCAIM in bits 0 through 7. The CRU input word conveys eight bits of X.21 BCAIM status information in bits 8 through 15, and eight bits of either data or command completion status from the X.21 BCAIM to the host computer in bits 0 through 7. Bit 8 of the control byte of the CRU output word informs the X.21 BCAIM whether bits 0 through 7 contain data or command information. Bit 8 of the control byte of the CRU input word informs the host whether bits 0 through 7 of the CRU input word contain data or status.

All commands/requests from the host computer to the X.21 BCAIM consist of five bytes of information transmitted via the data byte of the CRU output word. When the X.21 BCAIM finishes processing a request, it transmits a completion report consisting of six bytes of information back to the host via the status byte of the CRU input word.



2280754

Figure 1-5. CRU Interface Words

The host computer issues commands and/or requests to the X.21 BCAIM by setting the appropriate bits in the control byte of the CRU output word and then writing the five-byte command sequence to the data byte. When the host is ready to issue a command to the X.21 BCAIM, it must first check the bits in the control byte of the CRU input word to see if the X.21 BCAIM is busy. If the X.21 BCAIM is busy, the host sets the appropriate bits in the control byte of the CRU output word to allow the X.21 BCAIM to interrupt the host when it is ready to receive a command. When the X.21 BCAIM interrupts the host by going to a not-busy state, the host sets bit 8 in the CRU output word to indicate that command information is being sent and then writes the command byte in bits 0 through 7 of the output word.

The host then sends four additional bytes of command information (also written in bits 0 through 7 of the CRU output word) to the X.21 BCAIM to complete the five-byte command sequence. If the command issued requires data to be transferred from the host to the X.21 BCAIM, the host sets bit 8 in the control byte of the CRU output word to logic 0 to indicate that the information being sent is data. The host then transfers the data one byte at a time via bits 0 through 7 of the CRU output word. Refer to Section 3 for a more extensive overview of X.21 BCAIM command processing.

The X.21 BCAIM firmware executes the command issued by the host, then notifies the host of a proper completion of the request by echoing the command plus four bytes of status and one byte of command completion information via the CRU input word.

1.7 ON-BOARD SELF-TEST ROUTINE

The ROM firmware on the X.21 BCAIM contains a self-test routine that checks most of the hardware on the board for proper operation. The self-test routine contains a number of test programs designed to test areas of hardware on the board. It reports any problems or errors encountered by lighting the self-test/fail LED indicator located near connector P3.

The test programs execute automatically each time you power up or reset the X.21 BCAIM. The self-test/fail LED indicator on the board illuminates while the self-test programs are running and extinguishes when they complete without errors. If the LED remains lighted longer than five seconds after you power up or reset the board, it indicates that one of the programs encountered an error or a complete failure of the TMS 9900, TMS 9901, TMS 9903, RAM, ROM, or the LS362 clock generator while it was executing. Refer to the X.21 BCAIM maintenance manual for instructions on determining the cause of the problem and for information on how to repair the problem or replace the board.

2

Installation

2.1 GENERAL

This section describes how to unpack, install, and perform initial checkout of the X.21 BCAIM board. It includes power and environmental requirements of the board to aid in planning the installation. Installation information includes instructions on how to:

- Modify the host computer interrupt levels in a 6-slot, 13-slot, or 17-slot chassis
- Set the ID switches on the X.21 BCAIM
- Configure the jumpers on the X.21 BCAIM

This section also includes descriptions and illustrations of typical uses of the X.21 BCAIM in EIA and X.21 modes, including the part numbers of the cables required for each configuration. The last part of this section presents recommended methods of checking the X.21 BCAIM for proper operation after it has been installed.

2.2 UNPACKING AND INSPECTION

The X.21 BCAIM board is shipped either as a kit (part numbers 2303091-0001 through 2303091-0003) or as a part of a system where it is already installed in a Model 990 Computer. If the X.21 BCAIM board is already installed in a computer, use the unpacking and inspection instructions in the system hardware reference manual or the user's manual on the particular computer.

If the X.21 BCAIM is shipped as a kit, it is shipped in a cardboard container with the board housed in a rigid Styrofoam* container. Unpack the kit and inspect it as follows:

1. Before unpacking the cardboard shipping box, inspect it for evidence of damage such as crumpled corners, tears, water stains, and so forth.
2. Open the cardboard container and remove the Styrofoam packaged circuit board.
3. Carefully remove the X.21 BCAIM board from the Styrofoarn container and verify that the part number matches the number listed in Table 1-1.
4. Inspect the board for any loose or damaged components, cracks in the board, or loose material lodged between components that could cause a short circuit.
5. If any optional cables or parts were ordered, verify that their part numbers match those on the shipping list and inspect them carefully for damage.

* Trademark of the Dow Chemical Company.

2.3 PLANNING

The X.21 BCAIM board requires one half-slot location in a Model 990 Computer chassis or CRU expansion chassis. From this slot, the X.21 BCAIM obtains the power necessary for operation and interfaces with the CRU in the host computer. The power requirements for the board are as follows:

+5 ±0.15 Vdc	1.2 amperes
+12 ±0.36 Vdc	0.3 amperes
−12 ±0.72 Vdc	0.035 amperes

Table 2-1 presents the environmental requirements of the X.21 BCAIM board. Verify that the characteristics of the board are compatible with the planned environment.

Table 2-1. X.21 BCAIM Environmental Requirements

Operating temperature	0° C (32° F) to 65° C (149° F)
Shipping temperature	−40° C (−40° F) to 70° C (158° F)
Humidity (operating)	5 to 85% noncondensing
Humidity (nonoperating)	5 to 95%
Altitude	0 meters to +3,049 meters (0 to +10,000 feet)
Shock (operating)	1 g
Shock (shipping)	15 g to shipping container
Vibration (operating)	1 g at 5 Hz, 0.3 g 80 to 500 Hz

2.4 INSTALLATION

The following instructions for installing the X.21 BCAIM board apply when the board is packaged and shipped separately from the host computer or when the X.21 BCAIM is to be added to an existing system.

Before you install the board in the host computer chassis, do the following:

- Select a suitable chassis slot.
- Ensure that the interrupt level jumpers are configured to allow communication between the software in the host computer and the X.21 BCAIM.
- Set the X.21 BCAIM ID switches if the system software requires the board to have an ID.
- Configure the jumpers on the X.21 BCAIM board for compatibility with the system in which it is used.

The following paragraphs explain how to accomplish these tasks.

CAUTION

Always turn off power to the computer when installing or removing any circuit board from the chassis.

2.4.1 Selecting a Chassis Slot for the X.21 BCAIM

Place the X.21 BCAIM in any available slot. Ensure that the system software is informed of the CRU address of the slot and the interrupt level assigned to the X.21 BCAIM when the system is generated. The suggested range of interrupt levels for the X.21 BCAIM is between 7 and 15 since, in a typical system, it does not require a high priority interrupt level for proper operation.

2.4.2 Interrupt Connections

Interrupt connections required to interface peripheral equipment to the Model 990 Computer are usually made before the system is delivered to the customer. These interrupt assignments are coordinated with the software supplied with the system. However, if you do not purchase the X.21 BCAIM as part of a system, you must make the necessary interrupt connections as part of the board installation.

The following paragraphs explain how to modify interrupts in a 6-slot, 13-slot, or 17-slot chassis. A discussion on modifying interrupts in the 990A13 chassis introduced in mid-1982 follows the discussion of the 17-slot chassis.

2.4.2.1 6-Slot and 13-Slot Chassis Interrupts. The Model 990 Computer has 16 interrupt levels numbered 0 through 15. Interrupt level 0, which is internal to the processor, has the highest priority. Interrupt levels 3, 4, and 6 through 15 are external inputs available for assignment to peripheral controllers installed in the chassis. Interrupt level 5 is used for the real-time clock in most systems and usually is not available.

Chassis backplane wiring brings the circuit board interrupt output lines from slots 2 through 6 in a 6-slot chassis or 2 through 13 in a 13-slot chassis and the processor interrupt input lines to wire-wrap pin headers adjacent to slot 1 in each chassis. Jumper wires between the pins connect the circuit board interrupt outputs to the processor interrupt inputs. These jumpers may run directly from pin-to-pin, or they may be mounted on jumper plugs that slip over the pins. Figure 2-1 shows the jumper plugs installed in the chassis at 1A1J2 and 1A1J3. It omits the jumper wires for clarity.

There are two rows of pins in the header. The top row has 15 pins connected through the motherboard to the processor's 15 interrupt levels. The 13-slot chassis contains additional pins on the top row for special configurations such as CRU expansion. The bottom row contains 20 pins in a 6-slot chassis and 48 pins in a 13-slot chassis. Two of these pins are wired to each of the possible circuit board interrupt outputs to allow interrupts from more than one device to be connected to one interrupt level.

Figure 2-2 shows the interrupt pin assignments for the 6-slot chassis. Figure 2-3 shows the interrupt pin assignments for a 13-slot chassis. Both figures present a view of the jumper plugs as seen from the jumper wire side. The X marks identify jumper plug positions that have no corresponding pins on the header. The O marks identify jumper plug positions that have no corresponding pins on the early production header.

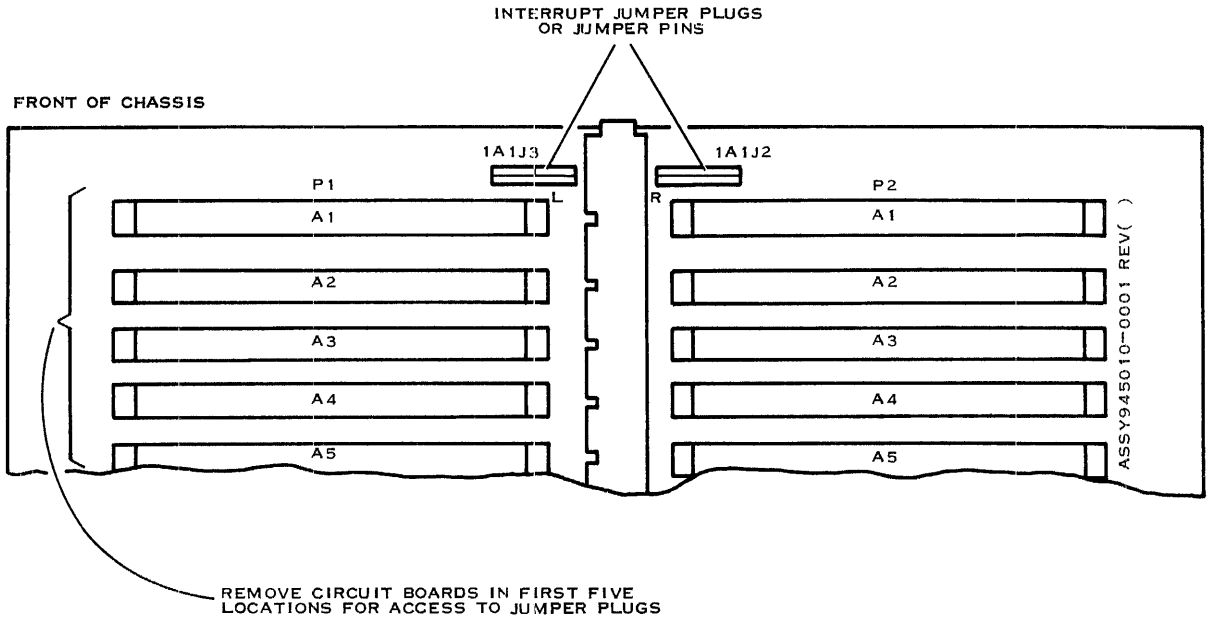


Figure 2-1. Location of Interrupt Jumpers, 6-Slot and 13-Slot Chassis

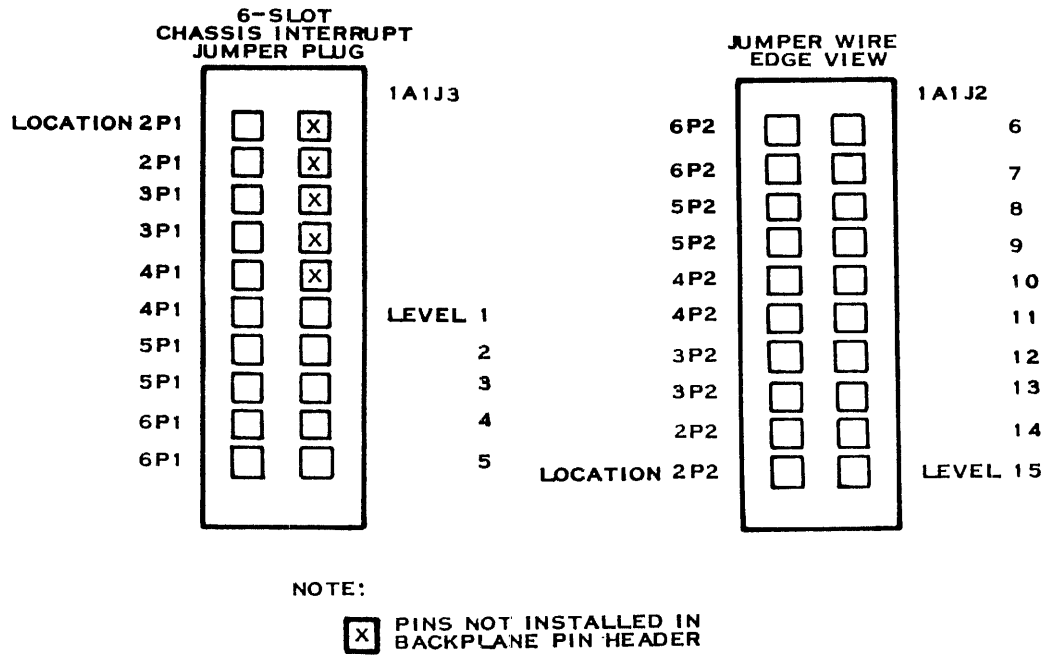


Figure 2-2. 6-Slot Chassis Interrupt Jumper Plugs

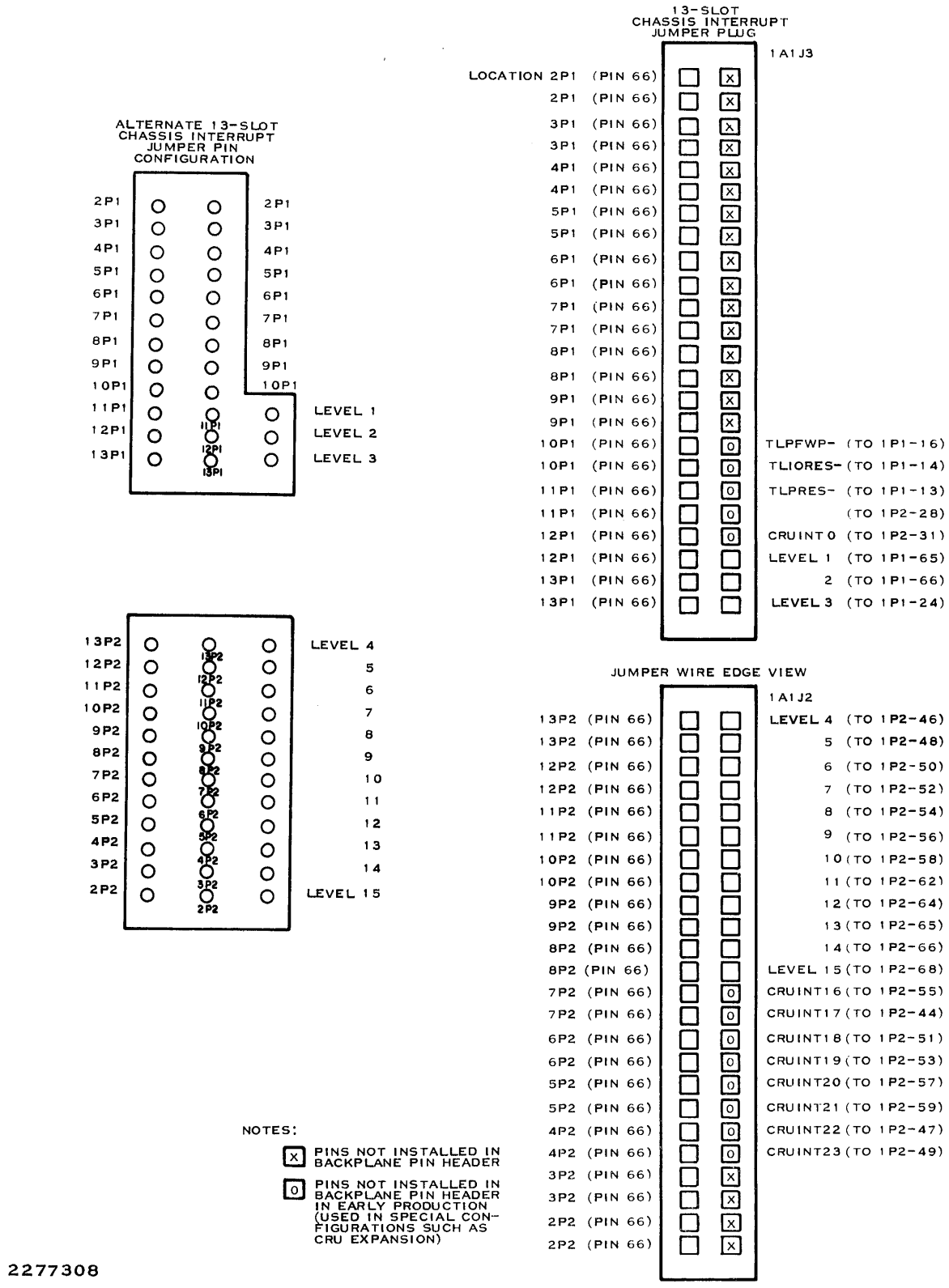


Figure 2-3. 13-Slot Chassis Interrupt Jumper Plugs

The configuration chart on top of each chassis lists the interrupt level and chassis slot assignments. Record any modifications to the interrupts on the chart.

The hardware reference manual for the Model 990 Computer contains a detailed procedure for assigning and changing interrupt levels. The following information is a brief summary of that procedure.

CAUTION

Do not remove or install any circuit board or modify any jumper while power is applied to the 990 chassis.

To gain access to the interrupt jumpers, remove the circuit boards installed in slots 1 through 5. The interrupt jumpers are visible on the motherboard just above the slot 1 connectors. The interrupt output of the X.21 BCAIM board is on pin 66 of the assigned slot location. For example, if you choose slot 11 on the P2 side of the 13-slot chassis for the X.21 BCAIM, the interrupt is found at 11P2 of the wire-wrap pin header (Figure 2-3). Install a single jumper from the 11P2 pin to the selected interrupt level input of the processor.

After completing any interrupt jumper modifications, carefully reinstall the removed circuit boards (component side up) according to the configuration chart fastened to the top of the computer. Update the configuration chart to correspond to the interrupt jumper modifications.

2.4.2.2 17-Slot Chassis Interrupts. On the 17-slot chassis, a printed circuit board, part number 2265440-0001 or optionally 2265442-0001, provides standard interrupt wiring when it is plugged into backpanel interrupt connector A23. Figure 2-4 is a view of the rear of a 17-slot chassis with the rear access cover open. It illustrates the location of connector A23.

Most 17-slot chassis are shipped from the factory with the standard interrupt board installed and require no changes. When you install the X.21 BCAIM in a particular slot, it automatically gets the interrupt level assigned to that slot. Figure 2-5 shows the standard interrupt assignments for the 17-slot chassis.

If you desire interrupts other than the standard ones provided, a kit is available (part number 2265457-0001) containing wires, jumper plugs, and instructions on how to wire the backpanel with a nonstandard interrupt scheme. Refer to the *Model 990/12 Computer Hardware User's Guide* , part number 2264446-9701, if you require more detail.

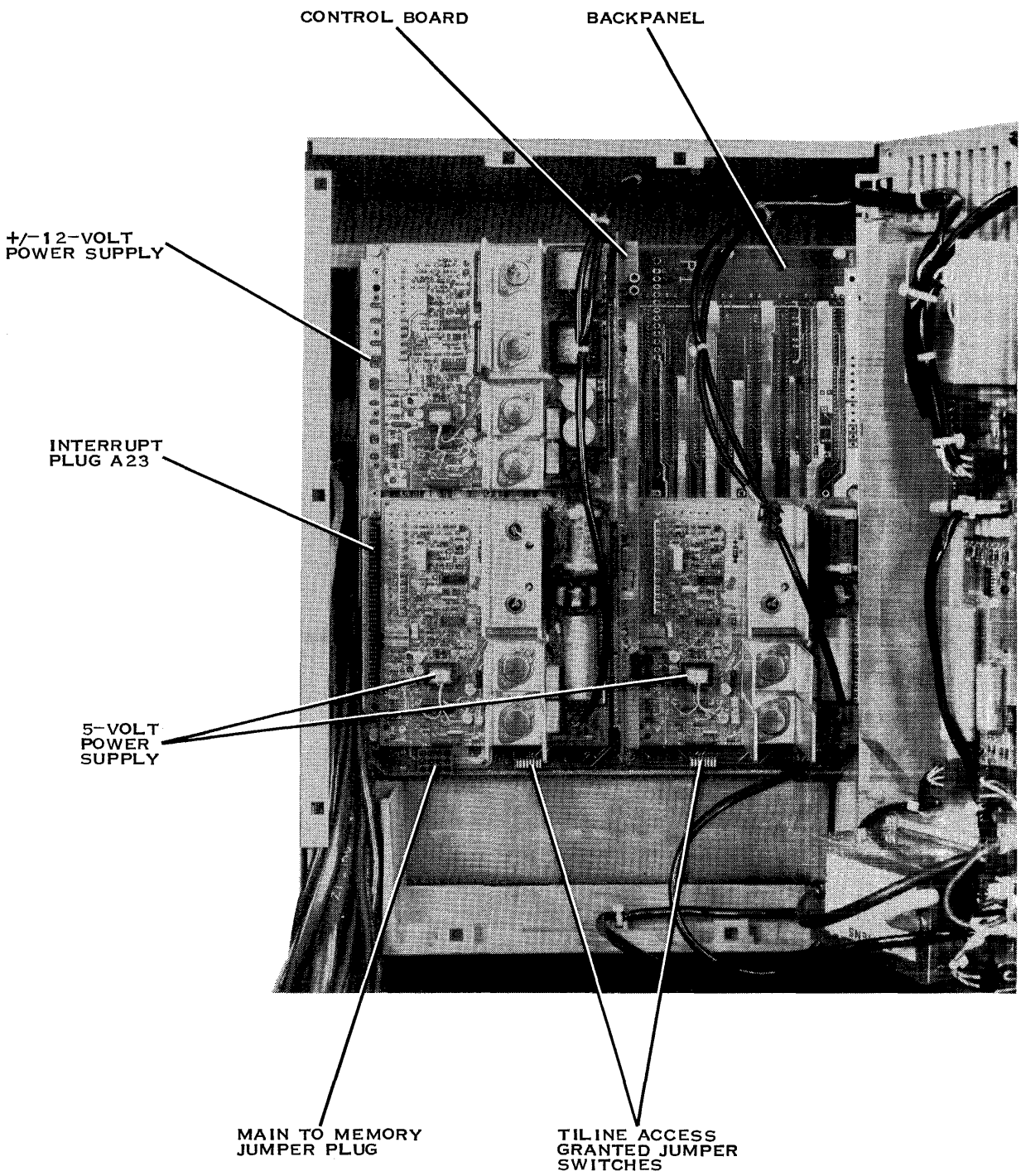


Figure 2-4. Interrupt Plug Location, 17-Slot Chassis

SLOT NUMBER	P1 (CHASSIS TOP) FIXED CRU BASE ADDRESS	P1 (CHASSIS TOP) CIRCUIT BOARD ***	P1 (CHASSIS TOP) INTERRUPT LEVEL	P2 (CHASSIS BOTTOM) FIXED CRU BASE ADDRESS	P2 (CHASSIS BOTTOM) CIRCUIT BOARD	P2 (CHASSIS BOTTOM) INTERRUPT LEVEL
1	N/A	990/12 SMI	N/A	N/A	990/12 SMI	N/A
2	NOTE	990/12 AU	N/A	NOTE	990/12 AU	N/A
3	NOTE	MEMORY CONTROLLER	N/A	NOTE	MEMORY CONTROLLER	N/A
4	NOTE	MEMORY ARRAY	N/A	NOTE	MEMORY ARRAY	N/A
5	NOTE		11	NOTE		11
6	02E0		10	02C0		10
7	02A0		15	0280		15
8	0260		12	0240		12
9	0220	FCCC	8	0200	FCCC	8
10	01E0		3	01C0		3
11	01A0	SYSTEM DISK*	13	0180	SYSTEM DISK*	13
12	0160	979A TAPE ** CONTROLLER	9	0140	979A TAPE ** CONTROLLER	9
13	0120	911 CRT #2	10	0100	911 CRT #1	10
14	00E0		11	00C0		11
15	00A0	FD1000	7	0080	FD1000	7
16	0060	LINE PRINTER	14	0040	CARD READER	4
17	0020		6	0000	733 ASR/KSR	6

NOTE:

CRU IN THIS SLOT AVAILABLE ONLY WHEN CHASSIS IS USED AS CRU EXPANSION WITH NO TILINE EXPANSION. SEE THE MODEL 990/12 COMPUTER HARDWARE USER'S GUIDE, PART NUMBER 2264446-9701 FOR MORE DETAIL.

*TILINE ADDRESS F800

**TILINE ADDRESS F880

***CONFIGURATION SHOWN FOR BOARDS MAY VARY FROM SYSTEM TO SYSTEM.

2278669

Figure 2-5. Factory Prewired Interrupts for 17-Slot Chassis

2.4.2.3 990A13 Chassis Interrupts. The 990A13 chassis is a 13-slot chassis introduced in mid-1982. Interrupt connections in the 990A13 chassis are made with a small printed circuit board (PCB) installed directly above slot 1 in the chassis. The interrupt connector is a standard 80-pin connector located at 0P2 (slot zero, P2 side), as shown in Figure 2-6. The chassis shown in Figure 2-6 is a demonstration chassis with a plexiglas top in place of the standard metal top, which allows the interrupt PCB to be seen.

Two types of interrupt boards are available: a permanent circuit board (type 13-1) with standard interrupt assignments and one programming jumper, and a fully-programmable interrupt board for nonstandard interrupt assignments. The part number of the standard type 13-1 board is 2310380-0001. The part number for the kit that contains the programmable interrupt board is 2309085-0001.

Interrupt outputs from each connector in chassis slots 2 through 13 are wired to the 80-pin connector above slot 1. Wired to the same connector are 24 CPU interrupt level lines from slot 1. Connections between slots 2 through 13 interrupt outputs and the CPU (or CRU buffer in an expansion chassis) interrupt inputs are made through the plug-in interrupt boards previously described. The following paragraphs explain how to configure standard and programmable interrupt boards.

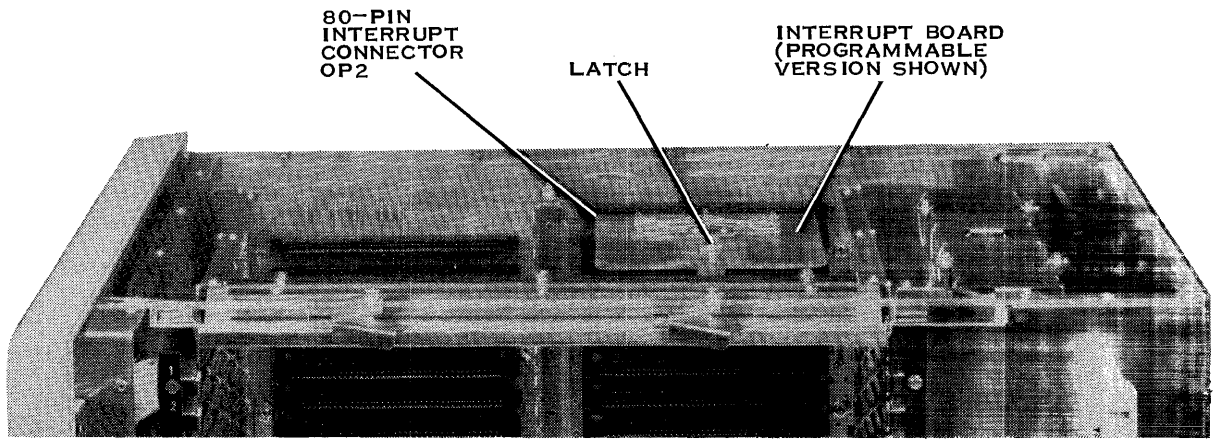


Figure 2-6. Location of Interrupt Board in 990A13 Chassis

Standard Interrupt Assignments. Figure 2-7 shows the standard interrupt board (type 13-1) and the standard interrupt assignments. If at all possible, you should use the standard interrupt assignments as they are based on extensive operating experience with Model 990 Computers.

Notice that the interrupt level for slot 8, P2 side can be either interrupt 9 or interrupt 14. A jumper on the type 13-1 board (Figure 2-7) allows selection of either interrupt. When you install the jumper parallel to the interrupt connector, interrupt 14 is selected. When you install the jumper perpendicular to the connector, interrupt 9 is selected. You must always install the jumper; otherwise, interrupts generated at the P2 side of slot 8 are not recognized.

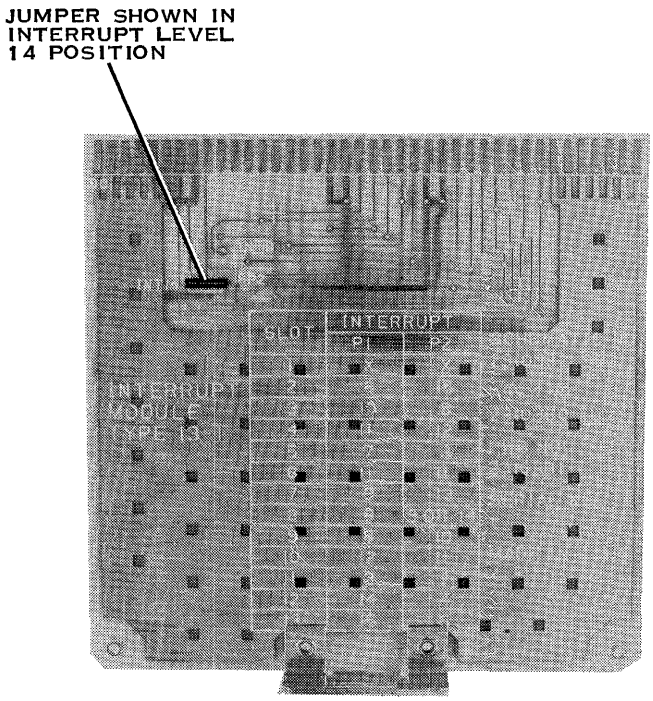
Interrupt 9 is available for use at slot 8 only if it is not used at slot 7, P1 side. Many of the full-size 990 logic boards do not generate interrupts at the P1 connector, making interrupt 9 available for use at slot 8. Refer to the installation and operation manual for the board installed in slot 7 for this information. Interrupt 14 is available for use at slot 8 with no such restrictions.

Programmable Interrupt Kit. The programmable interrupt kit allows you to configure interrupts for special requirements. The programmable interrupt kit (Figure 2-8) includes an interrupt circuit board with cold-contact terminals, a length of Teflon*-insulated 26 AWG solid wire, and a small plastic adapter tool for inserting wires in the cold-contact terminals. Place the adapter tool on the end of a Phillips-head screwdriver to press the wires into the terminals.

Figure 2-9 shows the pattern of terminals on the programmable interrupt board. Interrupt outputs from all of the P1 connectors in slots 2 through 13 are on the left side; interrupts from the P2 connectors are on the right side. The middle row of terminals contains the interrupt level inputs to slot 1. Interrupt levels 3 through 15 are the only levels available in a computer chassis. Do not make connections to levels 0 through 2 or 16 through 23 except in an expansion chassis.

Each terminal on the programmable interrupt board holds only one wire. Do not attempt to connect two wires to the same terminal; instead, run a single longer wire in a continuous daisy chain from the terminal through the other terminals. Figure 2-9 shows how a single daisy-chain wire can connect two interrupts to the same interrupt level without violating the one-wire-per-terminal rule. A single strand of wire runs through 7P1, interrupt level 13, and 7P2. This connection allows two half-size CRU boards to share interrupt level 13.

* Trademark of Du Pont de Nemours & Company Inc.



SLOT NUMBER	P1 (CHASSIS FRONT) FIXED CRU BASE ADDRESS	P1 CIRCUIT BOARD	P1 INTER-RUPT LEVEL	P2 (CHASSIS REAR) FIXED CRU BASE ADDRESS	P2 CIRCUIT BOARD	P2 INTER-RUPT LEVEL
1	N/A		N/A	N/A		N/A
2	02E0		6	02C0		15
3	02A0		10	0280		8
4	0260		11	0240		12
5	0220		7	0200		3
6	01E0		11	01C0		11
7	01A0		9	0180		13
8	0160		8	0140		9 OR 14
9	0120		8	0100		10
10	00E0		12	00C0		11
11	00A0		3	0080		7
12	0060		14	0040		4
13	0020		15	0000		6

13-SLOT CHASSIS
WITH INTERRUPT MODULE
TYPE 13-1 BOARD

2283424

Figure 2-7. Standard Interrupt Board and Interrupt Assignments

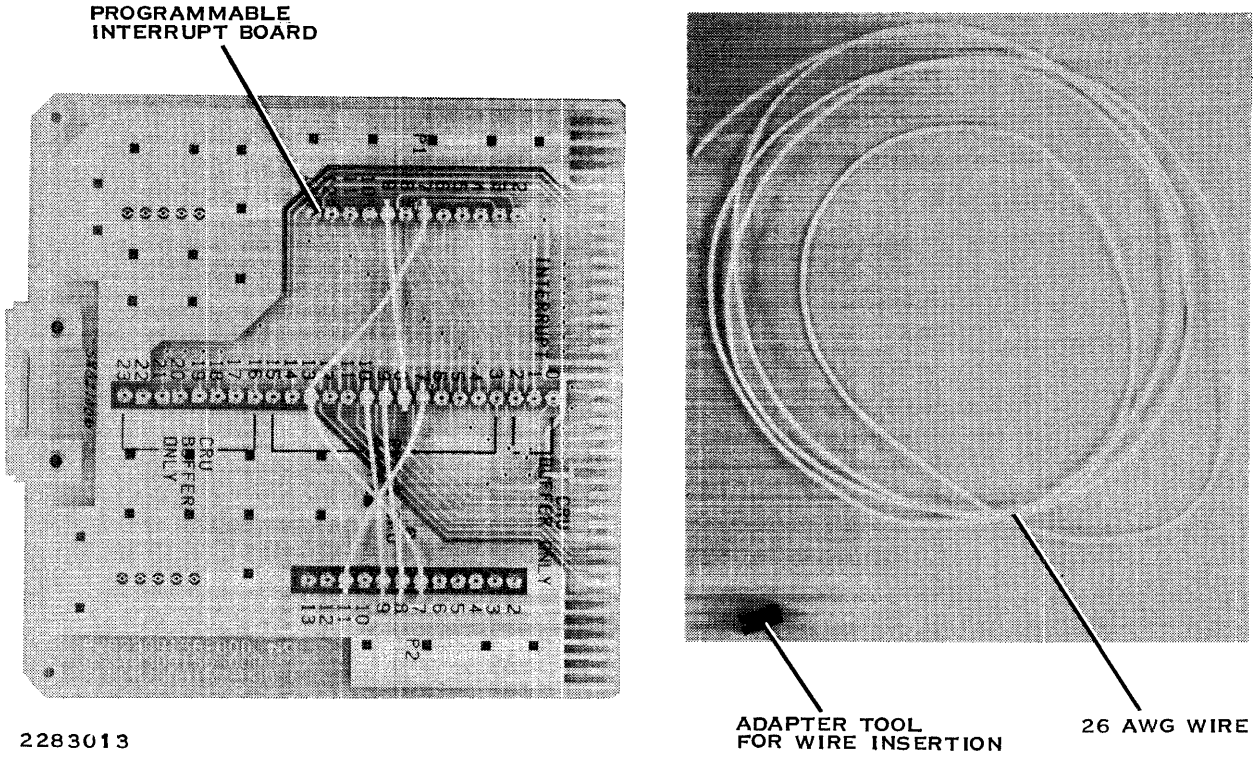
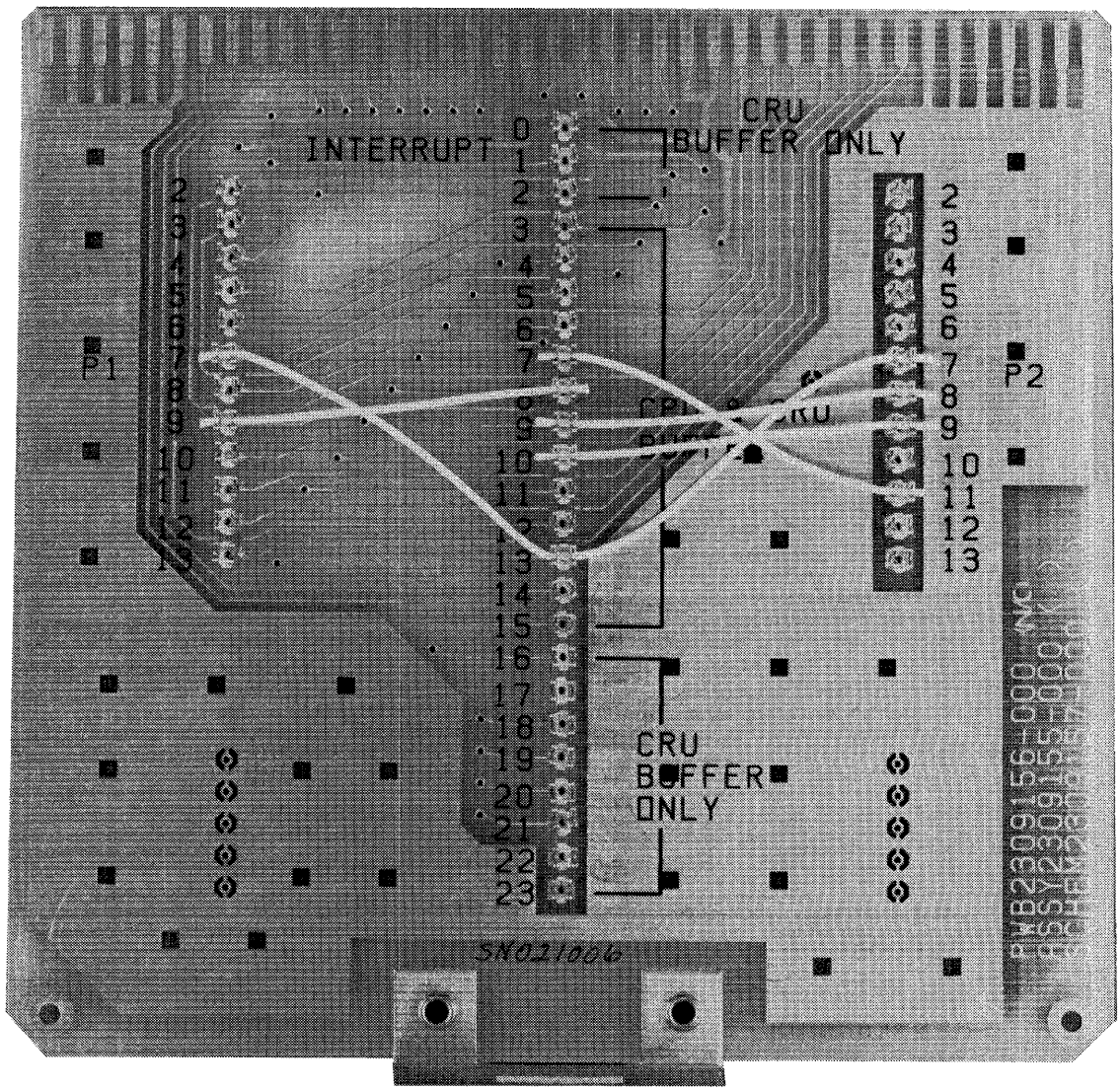


Figure 2-8. Programmable Interrupt Kit



2283014

Figure 2-9. Programmable Interrupt Wiring

Interrupt Board Installation in 990A13 Chassis.

NOTE

The following procedure requires complete removal of power, including standby power. Any data in computer memory will be lost. Save any critical data by writing it to disk or tape before turning the power off.

1. Set the rear panel ON-1/OFF-0 switch to the OFF-0 position.
2. Disconnect the ac line cord from the rear of the chassis.
3. If a standby power supply is installed, ensure that standby power is off.
4. Extend the chassis on its slides, or otherwise gain access to the right side as viewed from the front. Remove any logic boards from slots 1 through 6 for ease of access.
5. A white nylon latch knob suspends from the chassis top cover by a metal bracket. Turn the knob so the grooved front part is horizontal and parallel with the chassis top cover.
6. Orient the interrupt board with the latch bracket on top and the connector end pointed toward the chassis backpanel. Insert the board into the chassis with the board connector just touching the chassis connector.
7. Align the interrupt board so the grooved part of the nylon latch passes through the slot in the latch bracket. Adjust the board position so the connector and latch bracket are both aligned in their mating positions.
8. Gently press the interrupt board into the connector. Do not use excessive force. If the connectors do not mate on the first try, realign the board and try again. A gentle side-to-side rocking motion helps.
9. Turn the nylon latch knob 90 degrees either way to hold the interrupt board in place.
10. Reinstall any logic boards that you removed.
11. Replace the ac line cord if you removed it.
12. Turn on standby power if you turned it off at the beginning of this procedure.

2.4.3 Setting the X.21 BCAIM ID Switches

You can establish an eight-bit (two-hexadecimal digits) identification code for the X.21 BCAIM with the eight-position dual in-line package (DIP) switch located beside connector P2 on the board. Figure 2-10 shows the switch with an example setting that produces an ID code of 1C (hexadecimal).

You can use the ID code produced by the switch setting in any manner desired as long as the use is compatible with the supporting software. ID codes normally are used when the X.21 BCAIM is used in a polled network to allow the host computer a means of identifying a particular station. The TMS 9900 reads the ID code established by the switch setting when the host computer issues a Read ID Switches command (4D).

When you set the switches, take care to note that switch position 1 (the most significant bit) is on the left when you look into connectors P2 and P3 with the component side of the board up.

2.4.4 Configuring the X.21 BCAIM Jumpers

There are three jumpers located near connector P2 on the X.21 BCAIM board. Configure these jumpers as described in Table 2-2 to ensure that the board is compatible with the system in which it is installed.

2.4.5 Installing the X.21 BCAIM Board

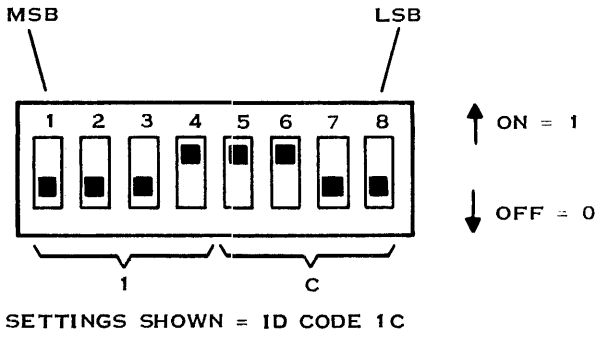
After you configure the interrupts to allow installation of the X.21 BCAIM into a particular chassis slot, set the ID switches (if required), and configure the jumpers to make the board compatible with the system, you are ready to install the X.21 BCAIM in the host computer chassis or in an expansion chassis.

X.21 BCAIM boards and other shielded boards are shipped from the factory with an insulator sleeve installed on the upper lip of the shield-stiffener. If the X.21 BCAIM is installed in a chassis with conventional (unshielded) boards, leave the insulator in place to protect the board above the X.21 BCAIM from shorting to the metal shield. When the X.21 BCAIM is installed with other shielded boards, remove the insulator from the upper lip of the shield by sliding it off as shown in Figure 2-11.

CAUTION

Always turn off power to the computer when installing or removing any circuit board from the chassis.

To install the X.21 BCAIM board, insert it into the assigned slot (with the component side toward slot 1) so that edge connector P1 mates with the computer backpanel. Push the board fully into the backpanel connector. Do not forget to update the chassis configuration label to reflect the installation of the X.21 BCAIM.



2280755

Figure 2-10. X.21 BCAIM ID Switch Settings

Table 2-2. X.21 BCAIM Jumper Configuration

Type of Network	Jumper From	Jumper To
EIA RS-232C	J1-2	J1-1
	J2-2	J2-3
	J3-2	J3-3
EIA RS-422	J1-2	J1-1
	J2-2	J2-3
	J3-1	J3-2
X.21 Leased Line	J1-3	J1-2
	J2-1	J2-2
	J3-2	J3-3
X.21 Switched Line	J1-2	J1-1
	J2-2	J2-3
	J3-2	J3-3

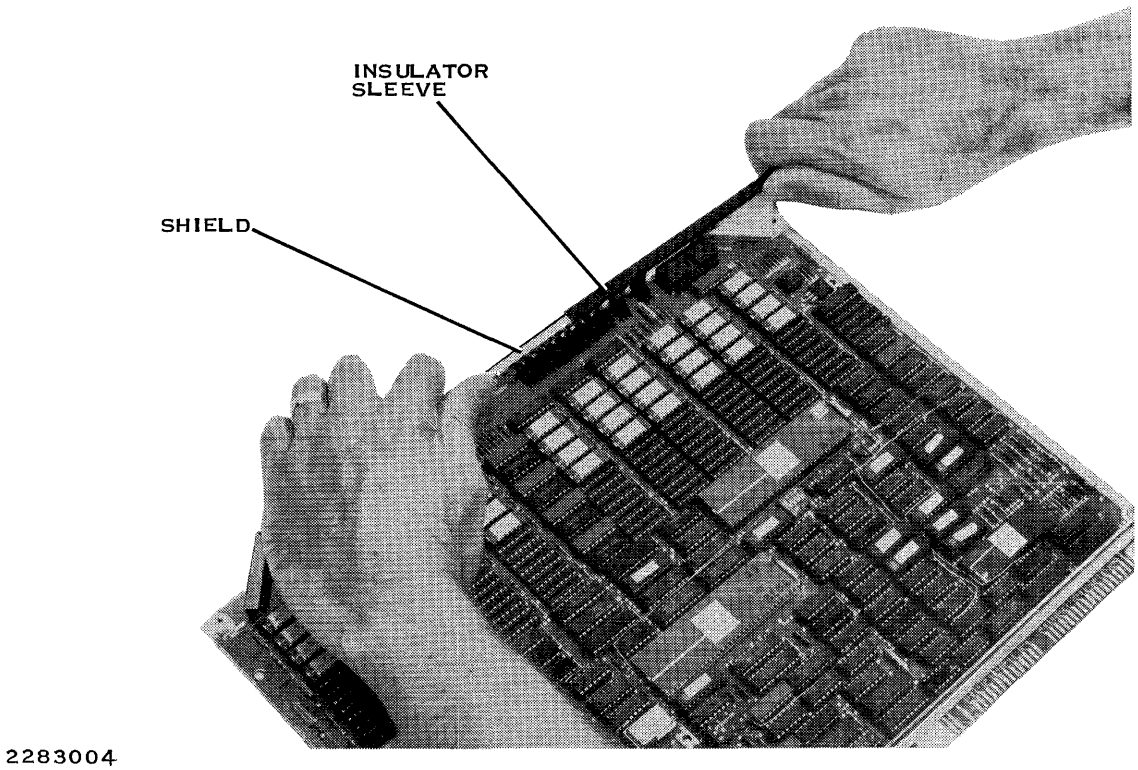


Figure 2-11. Removing the Insulator from a Shielded Board

NOTE

X.21 BCAIM boards equipped with ejectors of the type shown in Figure 2-12 will not seat properly in some chassis. If you encounter difficulty seating the board, clip the tabs on the ejectors as shown in Figure 2-12.

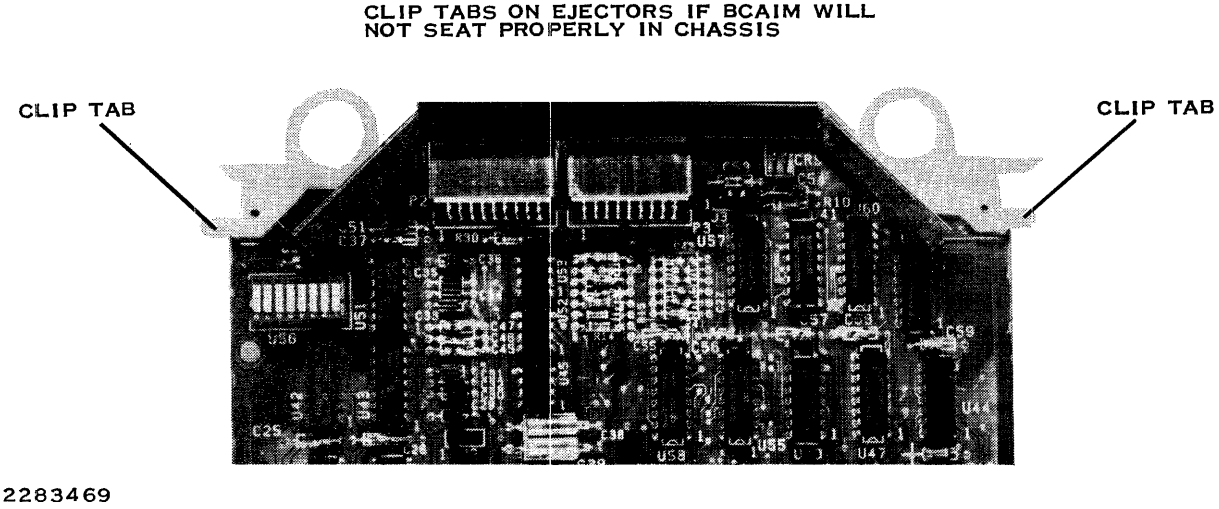


Figure 2-12. Special Installation Problems

2.4.6 Cable Connections

The cable connections required vary with the intended use of the X.21 BCAIM. Figures 2-13, 2-14, and 2-15 show the X.21 BCAIM used in typical EIA and X.21 networks with the interconnecting cables that are required for each configuration.

Figure 2-13 shows a typical EIA-mode use of the X.21 BCAIM in a dial-up system. Part numbers are shown on the equipment and cables that can be purchased from Texas Instruments.

The left side of Figure 2-13 shows the X.21 BCAIM being used with a TI internal modem and an internal automatic calling unit (ACU). This system is connected to the public switched telephone network through a data access arrangement (DAA). A DAA is required when equipment that is not Federal Communications Commission (FCC) registered is connected to a switched telephone line. A DAA is not required on a leased line connection.

The companion system illustrated on the right side of Figure 2-13 shows the X.21 BCAIM being used with equipment leased from the telephone company. In this system, the external automatic calling unit interface (EACUI) board is used to provide an interface between the Model 990 Computer and the Bell external ACU. The equipment leased from the telephone company is FCC-registered and does not require use of a DAA. For more information on the TI-supplied components shown in Figure 2-13, refer to the *990 Family Communication Systems Field Reference Manual*, part number 2276579-9701.

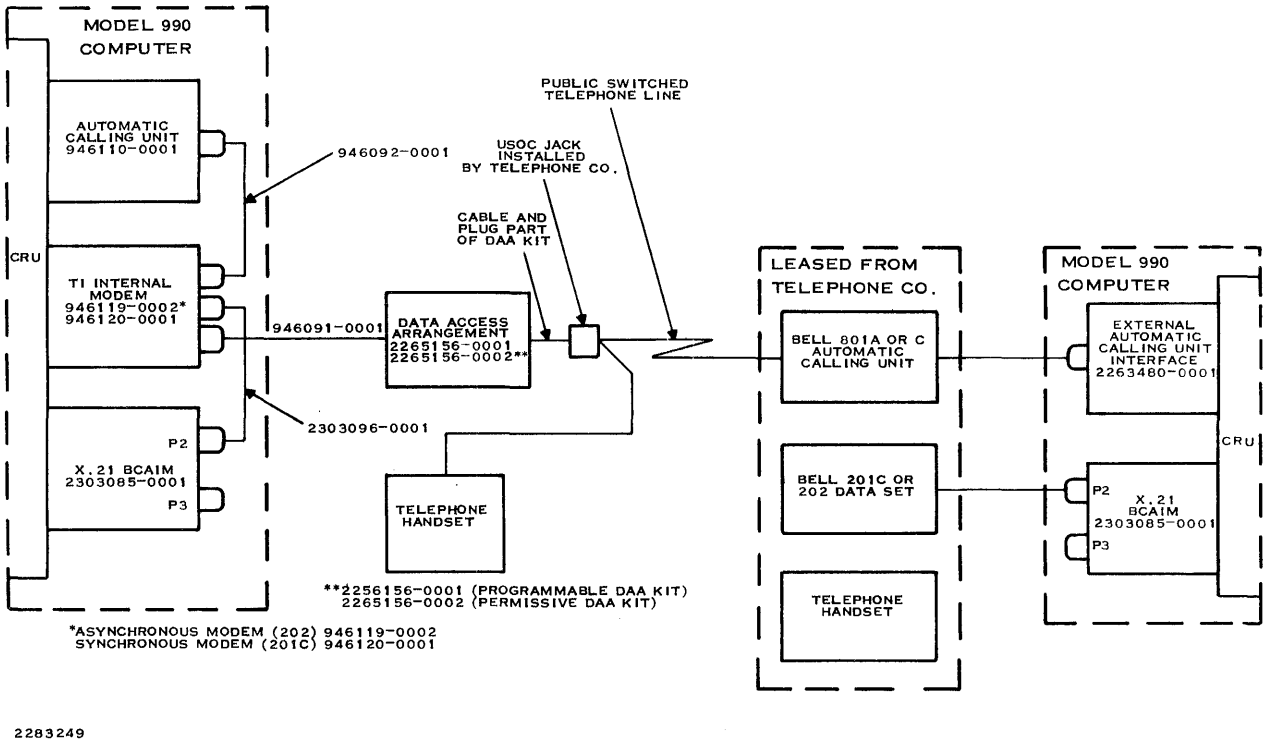


Figure 2-13. Typical EIA Mode Switched Network Installation

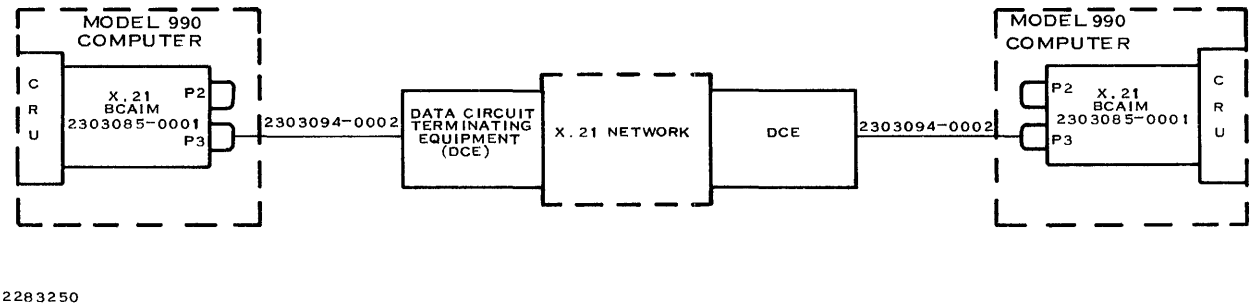


Figure 2-14. Typical X.21 Network Installation

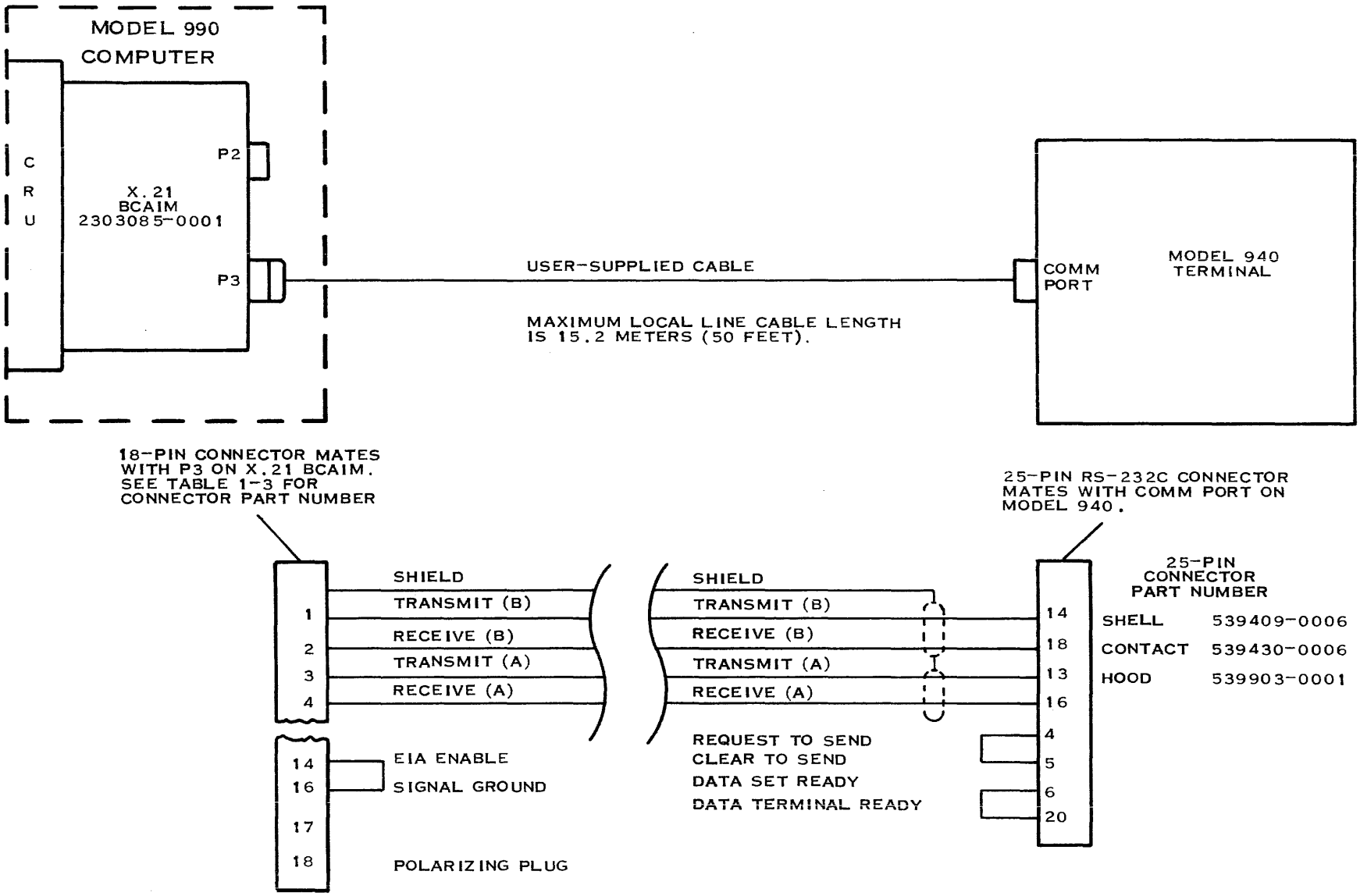


Figure 2-15. Typical EIA RS-422 Local Line Installation

Figure 2-14 shows the X.21 BCAIM being used in an X.21 network. The data circuit terminating equipment (DCE) is the interface between the X.21 BCAIM and the X.21 network. You can use the cable shown between the X.21 BCAIM and the DCE for X.21 leased or switched operation.

Figure 2-15 shows the X.21 BCAIM in a typical EIA RS-422 point-to-point local line application. Cables for local line use are user-fabricated. Table 1-3 contains the part number of an 18-pin connector that mates with P3 on the X.21 BCAIM. Figure 2-15 lists the part number of a connector that mates with the 25-pin EIA comm port connector on the Model 940 terminal. Paragraph 1.3.2 discusses the recommended cable. The shield around the conductors in the cable must be connected to the metal backshell of the connector that mates with P3 on the X.21 BCAIM in systems that require a protective ground.

2.4.7 Compatible Modems

For synchronous operation, the X.21 BCAIM is compatible with the TI internal 201C-type modem or with Bell 201, 208, 209, and 212S-type modems. For asynchronous operation, the X.21 BCAIM is compatible with the TI internal 202-type modem or with Bell 103, 113, and 212A-type modems. You can use other manufacturer's modems that are compatible with the Bell types previously mentioned.

2.5 CHECKOUT

After you install the X.21 BCAIM board in the host computer chassis in accordance with the procedures in this section, check it for proper operation by loading and executing the X.21 BCAIM diagnostic. If the diagnostic is not available, the on-board self-test routine provides an adequate verification of the board's operation. The following paragraphs discuss both methods of checking the board. Using the diagnostic is the recommended method of post-installation checkout.

2.5.1 Checkout with the Diagnostic

The instructions for loading the diagnostic (BCAIMT) for the X.21 BCAIM board are found in the *Model 990 Computer Unit Diagnostics Handbook, Volume 1*, part number 945400-9701. Volume 6 of the diagnostic handbook (part number 945400-9706) contains a program description of BCAIMT and explains how to use the tests included in the diagnostic.

The diagnostic consists of a series of tests designed to thoroughly test the hardware on the X.21 BCAIM, starting with the CRU interface logic and working through the communication channel logic. The diagnostic also includes tests that verify the proper operation of the communication line and some of the components of the communication system, depending upon how the system is configured.

After you load and initialize the diagnostic, the CRT displays guide you through the tests. The CRT displays error messages whenever the tests encounter problems on the board or in the system. The error messages indicate the problem area or the failing component in most cases.

2.5.2 Checkout with Self-Test

You can check the board with the self-test routine by simply powering up the computer and allowing the on-board self-test program to execute. The self-test/fail LED indicator located to the left of connector P2 on the component side of the board illuminates while the self-test program is executing. When the self-test program completes without error (in less than five seconds), the LED indicator should go out.

If the self-test/fail LED indicator remains illuminated after approximately five seconds, it indicates that a failure has occurred during execution of the self-test program. Try running the self-test program again by pressing RESET on the computer front panel. If the self-test/fail LED indicator still remains illuminated after five seconds, the board is faulty and should be repaired or replaced.

3

Programming

3.1 GENERAL

This section contains information needed to program and operate the X.21 BCAIM. You should be familiar with the 990 assembly language described in the *Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide*, part number 943441-9701 or the *Model 990/12 Computer Assembly Language Programmer's Guide*, part number 2250077-9701.

This section also explains error codes resulting from problems encountered during operation of the X.21 BCAIM. The discussion on command completions explains these error codes.

The meaning of some of the commands and error codes depends upon the particular protocol you select. The appendixes document protocols supported by the X.21 BCAIM. The text in this section identifies commands and error codes that are protocol dependent. Refer to the appropriate appendix for detailed definitions.

3.2 HOST/X.21 BCAIM INTERFACE

Transfers of information between the host computer and the X.21 BCAIM take place through the host computer's CRU interface via one 16-bit CRU interface output word and one 16-bit CRU interface input word. The following paragraphs and tables explain the use of the individual bits of the CRU interface words. For detailed information on how to address the bits of the CRU interface input and output words, refer to the assembly language programmer's guides referenced in paragraph 3.1.

3.2.1 CRU Interface Output Word

The host computer writes the CRU output word (Figure 3-1) to transfer data or command information to the X.21 BCAIM or to control the interface between the host and the X.21 BCAIM.

The host uses bit 8 of the output word to indicate whether bits 0 through 7 contain command information or data. When bit 8 is set to 1, it indicates bits 0 through 7 contain command information. When bit 8 is reset to 0, it indicates that bits 0 through 7 contain data. Bits 0 through 7 transfer data or commands one byte at a time from host memory to the X.21 BCAIM. The bits in the control byte (bits 8 through 15) are normally set or cleared on a single-bit basis to control the interface. Table 3-1 explains the use of the individual bits of the CRU interface output word.

Figure 3-2 is a simplified block diagram of the X.21 BCAIM interrupt logic illustrating the combinations of interrupts and enables required for the X.21 BCAIM to interrupt the host. The inputs and outputs of the logic in Figure 3-2 are the CRU bits described in Tables 3-1 and 3-2.

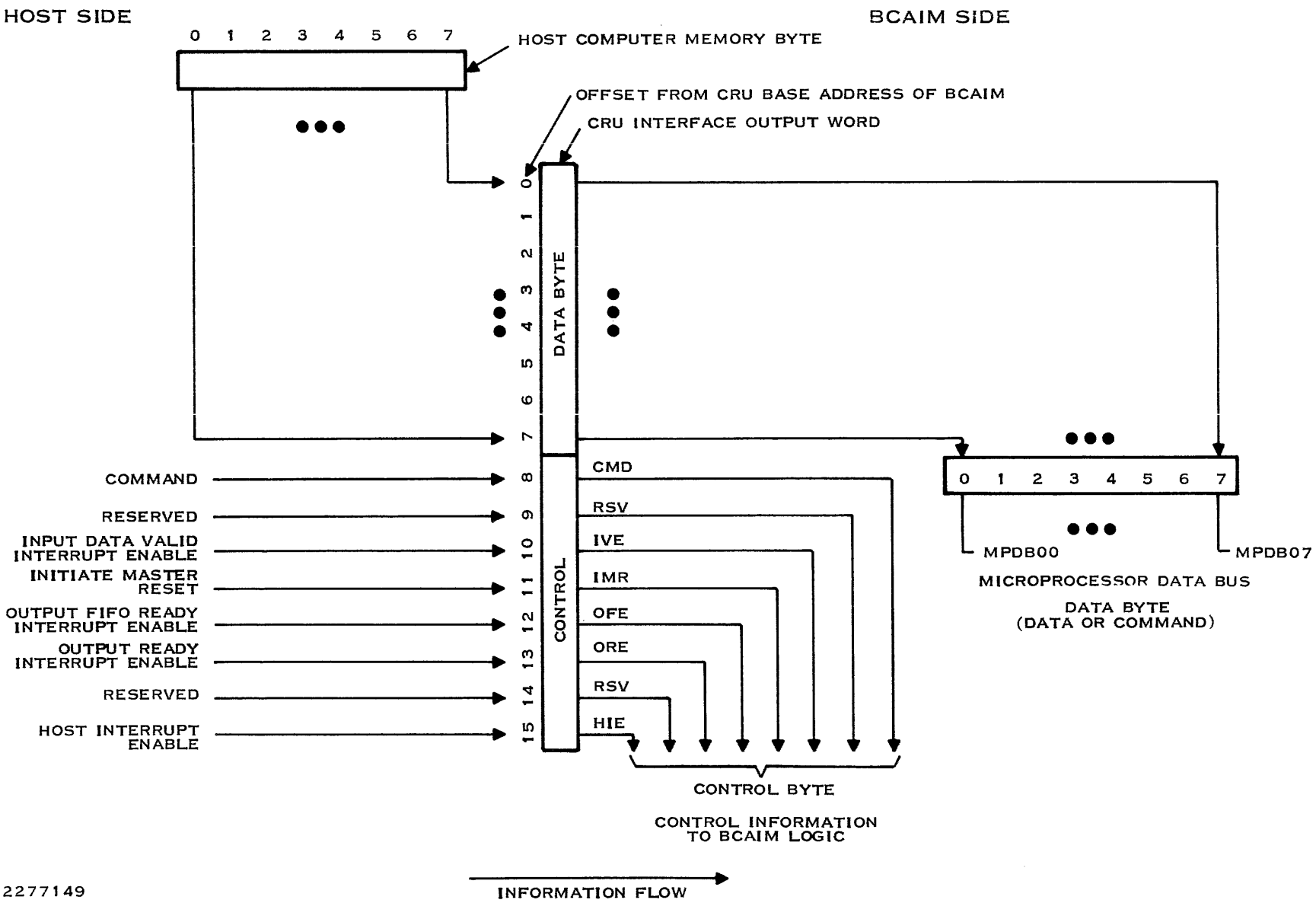


Figure 3-1. Host/Slave CRU Interface Output Word

Table 3-1. CRU Interface Output Word Bit Definitions

Bit	Mnemonic	Definition
0-7	—	Data Byte. The host uses this byte, consisting of bits 0 through 7, to transfer data or command information to the microprocessor data bus on the X.21 BCAIM. When bit 8 is set to 1, this byte contains command information. When bit 8 is set to 0, bits 0 through 7 contain data.
8	CMD	Command Bit. This bit is set to 1 to indicate a transfer of command information in bits 0 through 7, or to 0 to indicate a data transfer. Bit 8 must be set to the desired state (0 or 1) before the information is loaded in the data byte of the output word. When the command bit is set to 1, it indicates that the byte in bits 0 through 7 and the next four bytes written to the X.21 BCAIM (via the data byte) contain the parameters for an X.21 BCAIM command. The command bit need not be set to 1 during transfer of the last four bytes of the command block.
9	Reserved	This bit is reserved for future use. A master reset forces bit 9 to 0.
10	IVE	Input Data Valid Interrupt Enable. The host sets this bit to 1 to allow the X.21 BCAIM to interrupt when it has information to transfer to the host via the data byte of the CRU interface input word. Any host write to this bit (SBO or SBZ) clears the input data valid flag (input word, bit 10) and informs the X.21 BCAIM that the host has read the information in the data byte.
11	IMR	Initiate Master Reset. This bit is set to 1 to initiate a master reset of the X.21 BCAIM. The master reset causes the self-test routine on the X.21 BCAIM to execute and places the X.21 BCAIM in an initialized (idle) state. When this bit is set to 1, it causes the reset in progress bit (input word, bit 11) to be set to 1. When the X.21 BCAIM successfully completes self-test, the reset in progress bit is cleared and the output ready bit (input word, bit 13) is set in the CRU interface input word. If the self-test does not complete successfully, the X.21 BCAIM reports an error and the reset in progress bit remains set. Code the DSR for the X.21 BCAIM to time the master reset function and to report a failure if the reset does not complete in less than five seconds with no errors. This bit causes the same activity on the X.21 BCAIM as a power reset or a master reset (IMR) instruction.
12	OFE	Output FIFO Ready Interrupt Enable. The host sets this bit to 1 to allow the X.21 BCAIM to interrupt when it is ready to accept more transmit data. When ready to accept more transmit data, the X.21 BCAIM sets output ready and output FIFO ready to 1. The host is interrupted if host interrupts are enabled (HIE = 1). Refer to the discussion of bit 15 (HIE).

Table 3-1. CRU Interface Output Word Bit Definitions (Continued)

Bit	Mnemonic	Definition
13	ORE	Output Ready Interrupt Enable. Setting this bit to 1 allows the X.21 BCAIM to interrupt the host when it is prepared to receive information from the host. With this bit set to 1 and host interrupt enable (output word, bit 15) set to 1, the host is interrupted when the X.21 BCAIM sets the output ready bit (input word, bit 13) to 1. The output ready interrupt enable is set by the host when it tries to write data to the X.21 BCAIM and finds the output ready bit set to 0.
14	—	This bit is reserved for future use. It is set to 0 by a master reset.
15	HIE	Host Interrupt Enable. This bit is set to 1 to allow the host to be interrupted by the X.21 BCAIM. The host is interrupted only if this bit, the interrupt enable for the specific condition, and the specific condition are all in the true state. Refer to the discussion of the poll flag bit (input word, bit 14) and to Figure 3-2 for more detail. With the host interrupt enable bit set to 1, the poll flag bit going to 1 causes the interrupt summary bit (input word, bit 15) to be set to 1 and causes a host interrupt.

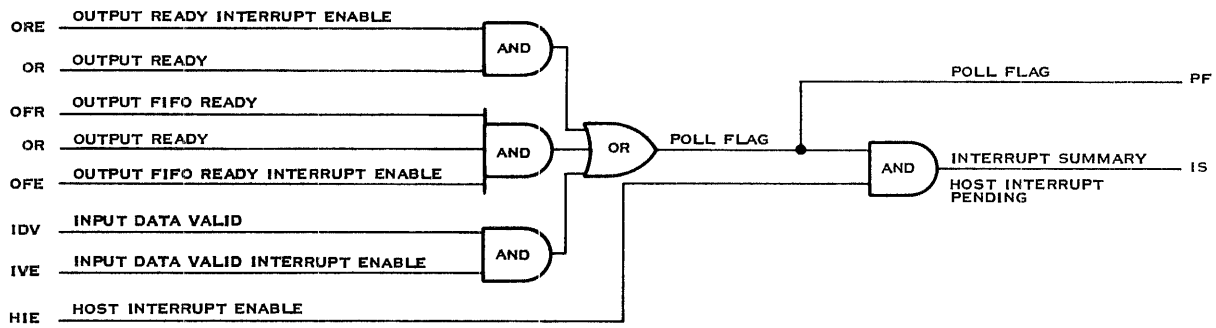


Figure 3-2. Simplified X.21 BCAIM Interrupt Logic

3.2.2 CRU Interface Input Word

Figure 3-3 illustrates the use of the bits of the CRU interface input word. The byte, consisting of bits 0 through 7, transfers data or command completion status from the X.21 BCAIM to the host. The byte, consisting of bits 8 through 15, transfers the status of the X.21 BCAIM hardware to the host computer. Bit 8 is set to 1 to indicate that bits 0 through 7 contain status information, or it is reset to 0 to indicate that they contain data.

The host reads data or command completion status one byte at a time. The host can check status bits on a single-bit basis to determine the status of the X.21 BCAIM. Table 3-2 explains the use of the individual bits of the CRU interface input word.

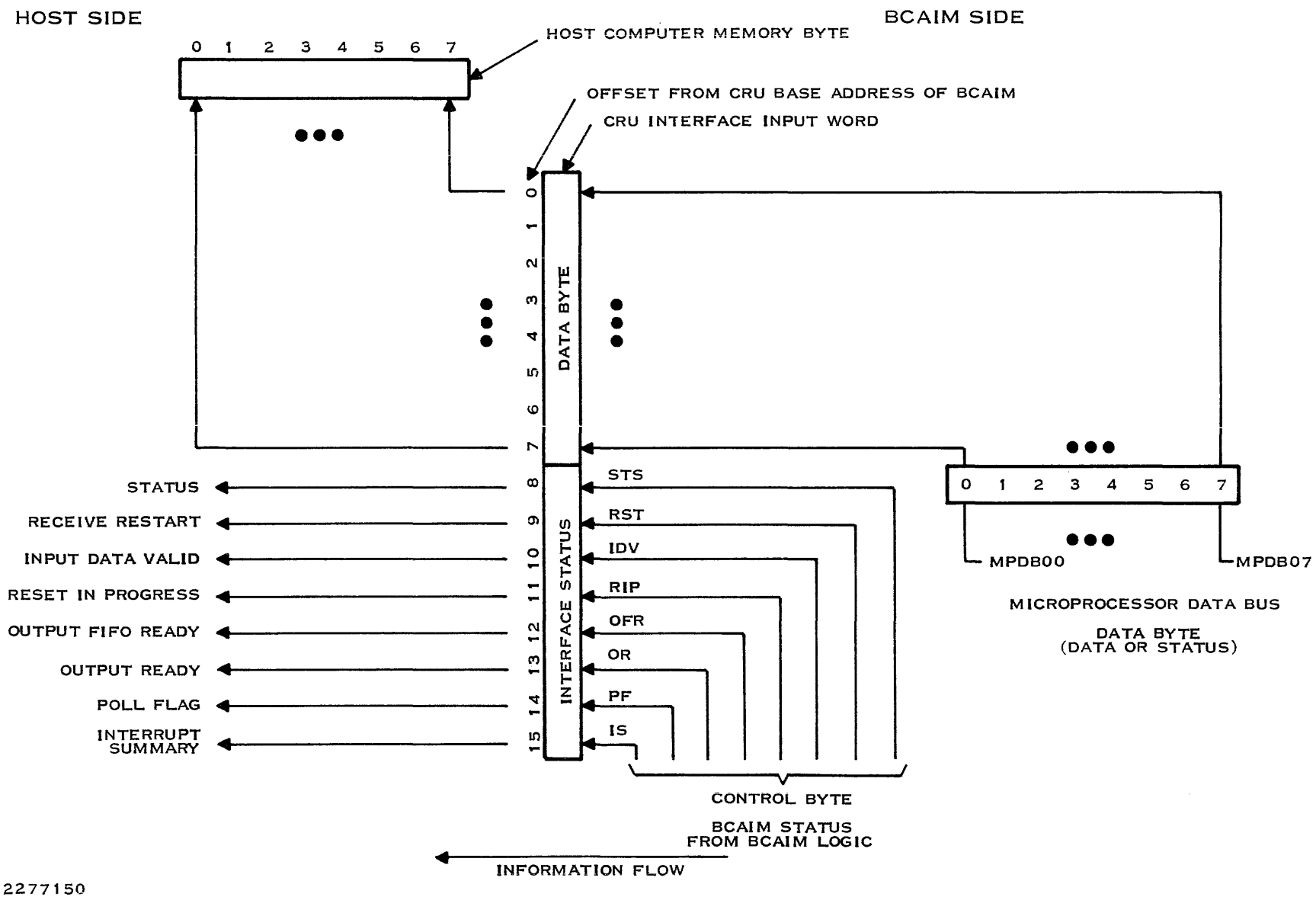


Figure 3-3. Host/Slave CRU Interface Input Word

Table 3-2. CRU Interface Input Word Bit Definitions

Bit	Mnemonic	Definition
0-7	—	Data Byte. This byte transfers data or command completion status from the X.21 BCAIM to the host computer. The byte contains status if bit 8 is set to 1 or data if bit 8 is 0.
8	STS	Status Bit. The X.21 BCAIM sets this bit to 1 to indicate that input bits 0 through 7 contain command completion status. It is set to 0 to indicate that the byte contains data. The X.21 BCAIM sets this bit to 1 for the first byte of a six-byte command completion status report. The host ignores it for the remaining five bytes of the completion report. For this bit to be valid, input data valid (input word, bit 10) must be set to 1. Anytime the host finds the status bit set to 1, it must check the receive restart (RST) bit to determine the type of status report.
9	RST	Receive Restart. The X.21 BCAIM firmware sets this bit to 1, sets the status bit to 1, and sets the input data valid flag to inform the host to reprocess the current receive request. Any time the status bit is set to 1, the host must check the receive restart bit to differentiate between normal completions and restarts. Certain receive errors invalidate the receive data and require that the X.21 BCAIM firmware restart the receive operation. When the host receives a restart report, it must initialize all parameters for the current receive request. The X.21 BCAIM firmware resets the receive restart bit after the host has reset the input data valid bit. Receive restart status reports are described in paragraph 3.3.2.
10	IDV	Input Data Valid. This bit is set to 1 when the X.21 BCAIM places information for the host to read in the data byte of the CRU interface input word. This bit interrupts the host if the host interrupt enable (output word, bit 15) and the input data valid interrupt enable (output word, bit 10) are both set to 1. The input data valid flag is reset to 0 by the process of the host writing to the input data valid interrupt enable (output word, bit 10).
11	RIP	Reset In Progress. The X.21 BCAIM sets this bit to 1 when it receives an Initiate Master Reset command (output word, bit 11 = 1) from the host computer. It is also set to 1 upon X.21 BCAIM power up. As soon as the X.21 BCAIM completes the reset, this bit is cleared. If self-test fails, it remains set.
12	OFR	Output FIFO Ready. This bit is set to 1 to inform the host that the output FIFO in X.21 BCAIM RAM is not yet full and more transmit data can be transferred to the X.21 BCAIM. When this bit is reset to 0, it informs the host that the output FIFO on the X.21 BCAIM is full. In this state, the host must stop transferring transmit data to the X.21 BCAIM until space becomes available in the output FIFO. The X.21 BCAIM still accepts commands when the output FIFO is full since it only stores data to be transmitted on the communication channel in the output FIFO. Write commands (opcode 3 and opcode 5) are the only commands that cause data to be stored in the output FIFO.

Table 3-2. CRU Interface Input Word Bit Definitions (Continued)

Bit	Mnemonic	Definition
		Other commands, such as Write Parameters (>73) and Memory Load (>0C), can ignore the state of the output FIFO ready bit when passing host data to the X.21 BCAIM since data associated with these commands is not stored in the output FIFO. Parameters coded into X.21 BCAIM firmware determine when the firmware should set the output FIFO ready flag to 1. The write FIFO thresholds command can modify these parameters. In normal use, it is intended that the X.21 BCAIM set the output FIFO ready bit to 1 when the output FIFO has enough space available for a significant number of data bytes. When the host finds the output FIFO ready bit set to 0, it sets the output FIFO ready interrupt enable bit to 1 so the X.21 BCAIM can interrupt the host when more output FIFO space is available. Upon receiving the output FIFO ready interrupt, the host can resume transferring transmit data.
13	OR	Output Ready. The X.21 BCAIM sets the output ready bit to 1 to indicate that it is ready to accept information from the host in the data byte of the CRU interface output word. This bit is set to 1 following completion of self-test and remains set until the host writes information in the data byte of the CRU interface output word. When the host writes to bit 7 of the data byte, it causes output ready to be reset. After the microprocessor on the X.21 BCAIM reads the byte from the host, it sets output ready to 1 again to indicate that the X.21 BCAIM is ready to accept more information.
14	PF	Poll Flag. This bit is set by any one of the three combinations of interrupt enables, interrupts, and conditions that follow: • Output ready interrupt enable and output ready • Output FIFO ready interrupt enable, output ready, and output FIFO ready • Input data valid interrupt enable and input data valid. If host interrupts are enabled (HIE = 1), poll flag going to 1 sets interrupt summary to 1 and interrupts the host.
15	IS	Interrupt Summary. This bit indicates that an interrupt from the X.21 BCAIM is pending when set to 1. It can be used when several controllers are connected to the same host interrupt to let the host know which controller caused the interrupt. Interrupt summary is set when poll flag and host interrupt enable are both logic 1. These same conditions are required to generate a host interrupt.

3.3 COMMAND PROCEDURE OVERVIEW

The following paragraphs present an overview of the procedure involved when the host computer issues a command to the X.21 BCAIM. This overview is intended to help you understand the use of the interrupt enables and the sequence of events that takes place when the host issues a command and the X.21 BCAIM processes the command and returns a command completion status report to the host.

Each command that the host computer issues to the X.21 BCAIM consists of a command block made up of five bytes of information transferred from the host to the X.21 BCAIM. When the X.21 BCAIM completes processing the command, a six-byte command completion status report is returned to the host. Figure 3-4 is a simplified flow diagram that illustrates how the five-byte command block is routed from the host computer to the X.21 BCAIM and how the six-byte command completion status report is returned to the host when command processing is complete.

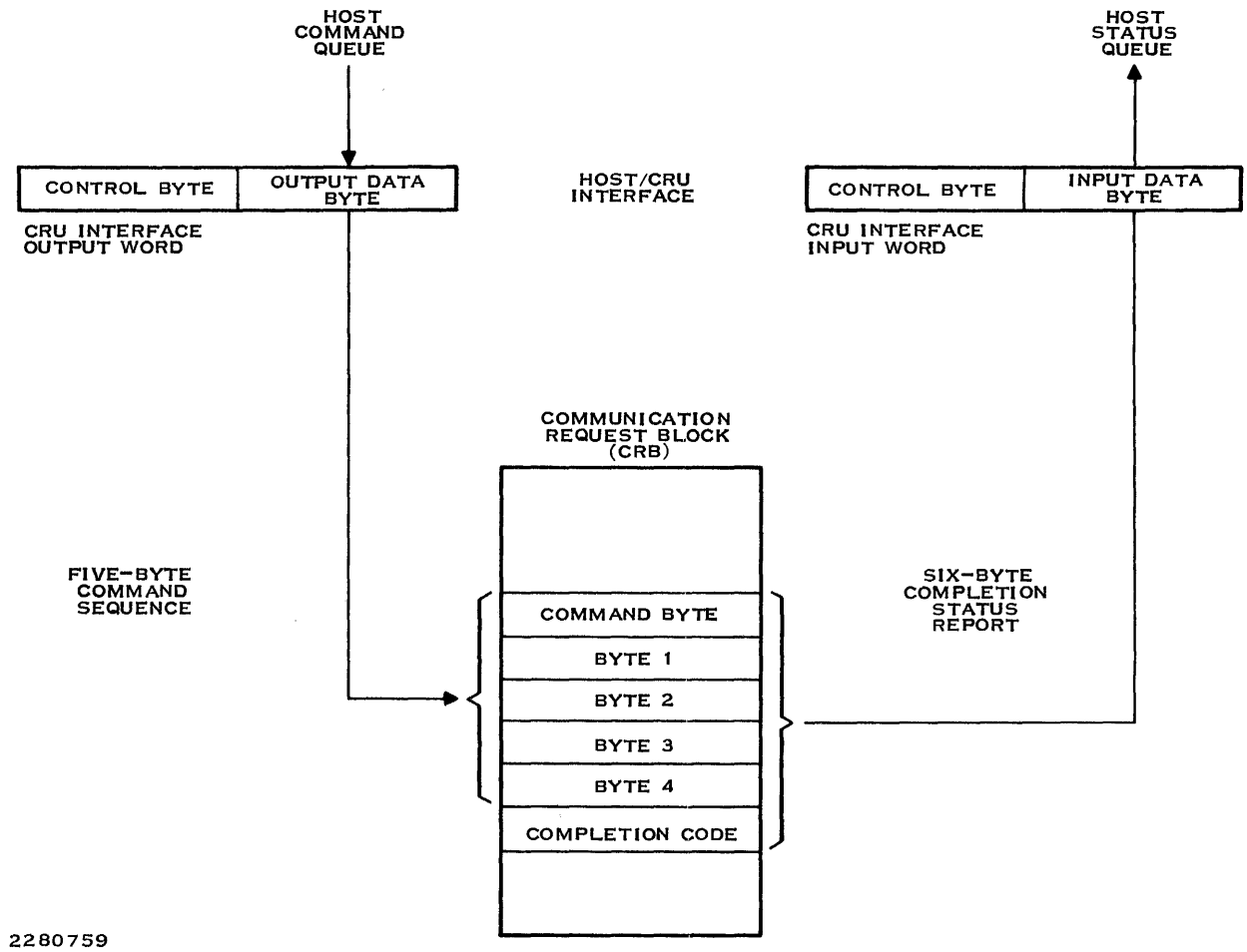


Figure 3-4. Command and Status Report Flow Diagram

The five bytes of the command block are written, one byte at a time, in the data byte of the CRU interface output word where each byte is transferred to a data structure in X.21 BCAIM RAM called a communication request block (CRB). The X.21 BCAIM firmware also stores status information in the CRB while processing the command. When processing is complete, the six-byte command completion status report is transferred to the host, one byte at a time, via the data byte of the CRU interface input word. The paragraphs that follow describe the command processing procedure in more detail.

3.3.1 Command Processing

When the host computer is ready to issue a command to the X.21 BCAIM, it must check the output ready flag (input word, bit 13) to determine whether the X.21 BCAIM is ready to accept information or not. If the X.21 BCAIM is not ready (output ready flag = 0), the host sets the output ready interrupt enable flag (output word, bit 13 = 1) and sets host interrupt enable (output word, bit 15) to 1 to allow the X.21 BCAIM to interrupt when it is ready to receive information. When the X.21 BCAIM is ready to receive information, the firmware sets the output ready flag to 1 and the host is interrupted.

To issue the first byte of the five-byte command block to the X.21 BCAIM, the host sets the command bit (output word, bit 8) to 1 to notify the X.21 BCAIM firmware that the information being transferred is command information. Then, the host writes the first byte in bits 0 through 7 of the CRU interface output word. Figure 3-5 shows how the byte is transferred from host memory to the CRU interface output word.

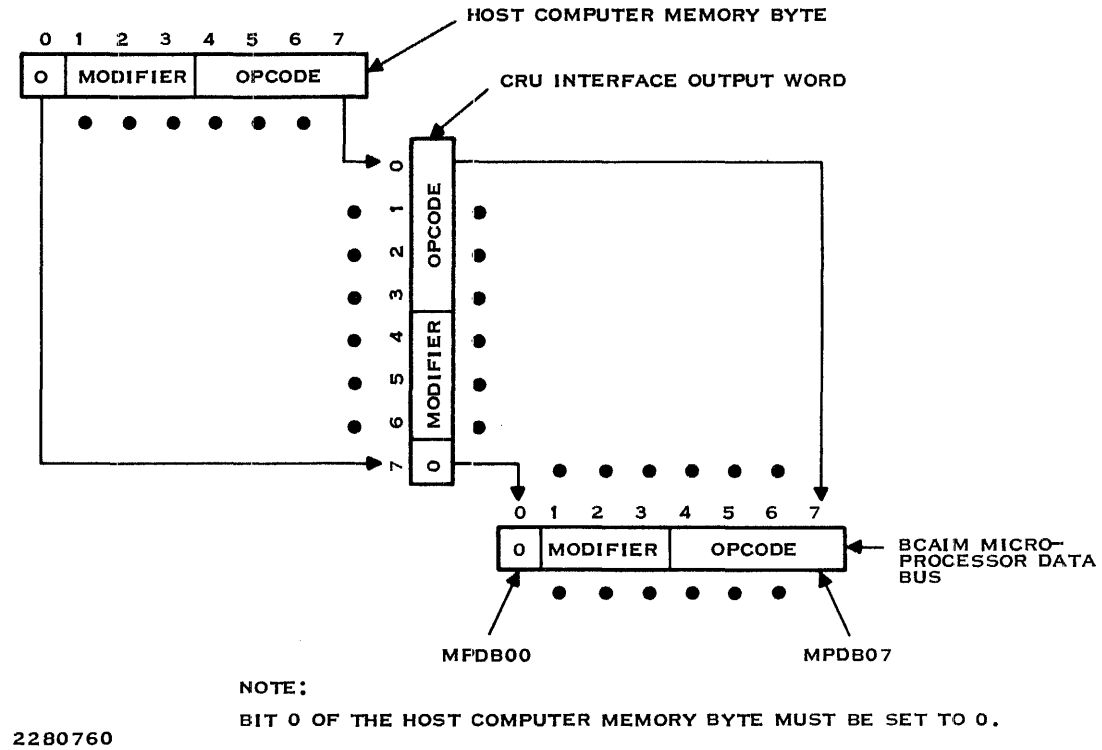


Figure 3-5. X.21 BCAIM Command Byte Format

The first byte of the five-byte command block contains a command code consisting of a four-bit opcode and a three-bit modifier written in bits 0 through 6 of the CRU interface output word. Always set bit 7 of the interface output word to zero. Four additional bytes (bytes 1 through 4) of information needed to complete the command follow the initial byte. You need not set the command bit for the remaining four bytes of the command block since the X.21 BCAIM firmware assumes that the next four bytes are part of the command block.

Figure 3-6 shows the format of a typical five-byte command block. Byte 0 contains the opcode and modifier that specify the particular command that the X.21 BCAIM firmware must execute. Bytes 1 through 4 contain additional information needed by the X.21 BCAIM firmware to process the command. The information required in bytes 1 through 4 of each command block is defined with the descriptions of command codes later in this section.

Several commands require that data be transferred to the X.21 BCAIM in addition to the five bytes of command information. Commands with data to be transferred to the X.21 BCAIM, but not to be transmitted on the communication channel, include Write Parameters (>73) and Memory Load (>0C). These commands require special host processing. Unlike commands with data to be transmitted on the communication channel, the data associated with these two commands must be transferred to the X.21 BCAIM immediately following the five bytes of the command block. The host ignores the output FIFO ready flag during the processing of these two commands and transfers a byte of data each time the X.21 BCAIM sets the output ready flag to 1. The X.21 BCAIM reports completion status immediately after all data has been transferred.

When a command requires that data be transmitted over the communication channel, the output FIFO in X.21 BCAIM RAM buffers the data. Commands with transmit data include Write commands (modifiers 0 through 4, opcode 3) and Chained Write commands (modifiers 0 through 4, opcode 5). The host must monitor the output FIFO ready flag in addition to the output ready flag when transferring data associated with these two commands.

The host can transfer transmit data to the X.21 BCAIM as long as the output FIFO ready flag is set to 1 to indicate that there is space left in the output FIFO. When the output FIFO is full, the X.21 BCAIM firmware sets the output FIFO ready flag to 0 to signal the host to stop transferring data. If the host still needs to transfer more data, it sets the output FIFO ready interrupt enable flag to allow a host interrupt when the output FIFO ready flag goes to 1 again. When the space available in the output FIFO becomes equal to or greater than the output FIFO threshold value, the firmware sets the output FIFO ready flag to 1.

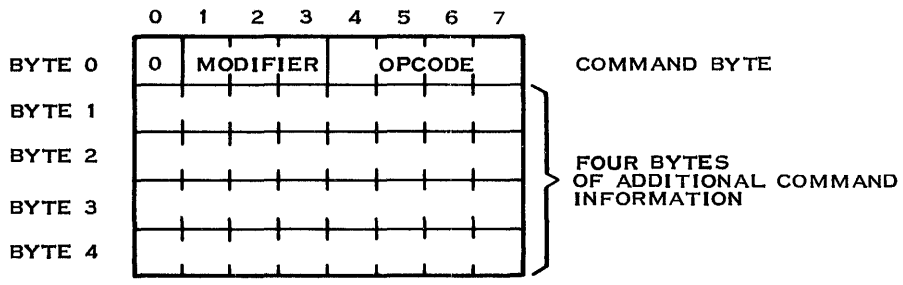


Figure 3-6. Five-Byte Command Block Format

The host can continue to issue commands during the time that the output FIFO is full since command parameters are stored in X.21 BCAIM RAM external to the output FIFO.

When the host issues multiple Write commands requiring data to be buffered in the output FIFO, it is responsible for presenting the transmit data to the X.21 BCAIM in the same order that the associated commands were issued. This is essential since the X.21 BCAIM only keeps track of the data associated with a Write command by the byte count. For instance, if the host issues two Write commands to the X.21 BCAIM, all of the data associated with the first Write command must be transferred to the X.21 BCAIM before any of the data associated with the second command can be transferred.

3.3.2 Command Completion Status Reports

After the X.21 BCAIM receives a five-byte command block from the host and the X.21 BCAIM firmware finishes processing the command, a six-byte command completion status report (Figure 3-7) is returned to the host. In the first byte (byte 0) of the command completion status report, the X.21 BCAIM echoes the command code issued by the host. Then, it transfers four additional bytes of command completion status followed by a byte containing a completion code. Command completion codes are defined later in this section.

The most significant bit of the first byte of the completion status report is an error flag. It is set to 1 when the completion code (byte 5 of the six-byte report) specifies an error condition. At all other times, the completion code byte contains status information.

Prior to sending the command completion status report, the X.21 BCAIM sets the status bit to 1 and the receive restart bit to 0 to inform the host that the next six bytes of information transferred will be a command completion status report. After the host reads the first byte of a normal status report, the status bit is ignored since it is aware that the next five bytes are going to be part of the status report.

When the X.21 BCAIM microprocessor writes the first byte of a six-byte normal command completion status report to the host, it sets the input data valid bit. The input data valid bit interrupts the host if the host has set input data valid interrupt enable and host interrupt enable to 1. If the host is not operating in the interrupt mode, it must poll the input data valid flag to determine when the X.21 BCAIM has information to transfer to the host.

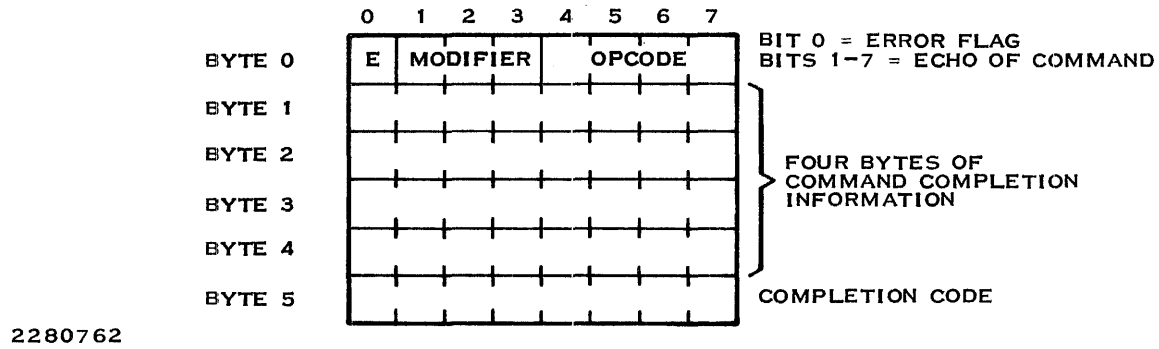


Figure 3-7. Command Completion Status Report Format

After the host reads the first byte of the completion report, it sets the input data valid interrupt enable to 1. The process of the host writing to the input data valid interrupt enable bit in the CRU interface output word clears the input data valid flag, informing the X.21 BCAIM that the host has read the byte and is ready to accept another byte. When the X.21 BCAIM places the next byte in bits 0 through 7 of the CRU interface input word, it sets input data valid again to inform the host that another byte is ready to be read. The remaining bytes of the six-byte command completion status report are transferred in the same manner.

Anytime the X.21 BCAIM sets the status bit and interrupts the host, the host must test the receive restart bit (input word, bit 9) to determine whether the status report is from a normal completion or if it is caused by an error requiring a restart of the current receive operation. Some types of receive errors cause X.21 BCAIM character detection routines to abort reception of the current data frame and use the current receive request to receive the next data frame. When this occurs, the X.21 BCAIM sets the status and receive restart bits to notify the host that the data in the current frame is invalid and that the receive operation is being restarted.

The host must discard any data already transferred from the frame currently being received and wait for the X.21 BCAIM to restart the receive operation. When a receive error causes the firmware to set receive restart, the X.21 BCAIM echoes byte 2 of the receive command block back to the host. This status report is unique in that only one byte of status is reported to the host. The X.21 BCAIM clears the status and receive restart bits after the host acknowledges reception of the status byte by clearing the input data valid flag. The X.21 BCAIM never sets the receive restart bit unless the status bit is set to 1.

If a command involves transferring data from the X.21 BCAIM to the host, the status and receive restart bits are reset to 0 and the data is transferred in bits 0 through 7 of the CRU interface input word in the same manner as the command completion status report. For Read commands, the data transfer to the host precedes the command completion status report except for the Read Parameters command (>74). The command completion status report is returned to the host immediately followed by the data associated with this command. The command completion status report precedes the data for all Host Interface requests.

3.4 X.21 BCAIM COMMANDS

The host computer controls the X.21 BCAIM by writing commands (also called requests) to the X.21 BCAIM via the CRU interface output word and monitoring the X.21 BCAIM's response to the commands by reading the CRU interface input word. This discussion provides an explanation of the command codes that can be issued to the X.21 BCAIM.

Commands to the X.21 BCAIM from the host computer each define a specific task or tasks that the X.21 BCAIM must perform. These commands are made up of a four-bit command code (called an opcode) and a three-bit modifier that the host writes to the CRU interface output word.

The command code modifiers are provided so that additional information about the command can be passed from the host to the X.21 BCAIM. The modifiers also allow one command, such as a Write command (opcode 3), to be modified into subcommands such as a Write Parameters command (modifier 7, opcode 3).

Figure 3-5 shows how the opcode and modifier are written in a host computer memory byte to be transferred to the CRU interface output word data byte. You must always set the most significant bit of the host computer memory byte to 0 when issuing commands to the X.21 BCAIM.

You can use several DX10 opcodes on the X.21 BCAIM. A discussion on how to map DX10 opcodes to X.21 BCAIM commands is presented later in this section. DX10 opcodes are used as an example; opcodes for other 990 computer operating systems have to be mapped in a similar manner.

Table 3-3 defines the X.21 BCAIM command codes. The modifiers listed in Table 3-3 are the binary value of the contents of bits 1 through 3 of the host computer memory byte (or bits 4 through 7 of the CRU output word data byte). The opcodes listed in Table 3-3 are the hexadecimal value of the contents of bits 4 though 7 of the host computer memory byte (or bits 0 through 3 of the CRU output word data byte).

Table 3-3. X.21 BCAIM Command Codes

Modifier (Bits 1-3)	Opcode (Bits 4-7)	Command	Type of Command
	0	Time-Out/Abort	Channel commands
0	0	Time-Out	
1	0	Abort Write requests	
2	0	Abort Read requests	
3	0	Abort Write and Read requests	
4	0	Abort Miscellaneous (Time-Out and Open/Close)	
5	0	Abort Write and Miscellaneous	
6	0	Abort Read and Miscellaneous	
7	0	Abort all requests	
	1	Open	
0	1	Illegal	
1	1	Open-accept	
2	1	Open-initiate	
3	1	Open-accept	
4	1	Open-initiate	
5	1	Open-accept	
6	1	Open-initiate	
7	1	Open-accept	
	2	Close	
0-7	2	Close	
	3	Write	
0	3	Write CD Entry Point 0	
1	3	Write CD Entry Point 1	
2	3	Write CD Entry Point 2	
3	3	Write CD Entry Point 3	
4-6	3	Reserved	
7	3	Write Parameters	Channel commands

Table 3-3. X.21 BCAIM Command Codes (Continued)

Modifier (Bits 1-3)	Opcode (Bits 4-7)	Command	Type of Command
	4	Read	Channel commands
0	4	Read CD Entry Point 0	
1	4	Read CD Entry Point 1	
2	4	Read CD Entry Point 2	
3	4	Read CD Entry Point 3	
4-6	4	Reserved	
7	4	Read Parameters	
	5	Chained Write	
0	5	Write CD Entry Point 0	
1	5	Write CD Entry Point 1	
2	5	Write CD Entry Point 2	
3	5	Write CD Entry Point 3	
4	5	Read CD Entry Point 0	
5	5	Read CD Entry Point 1	
6	5	Read CD Entry Point 2	Channel commands
7	5	Read CD Entry Point 3	
	6	DX10 (Protocol Dependent)	DX10 commands
0	6	Reserved	
1	6	Reserved (Rewind)	
2	6	Reserved (Unload)	
3	6	Reserved (Forward Space)	
4	6	Reserved (Backward Space)	
5	6	Write Channel CRU Interface	
6	6	Read Channel CRU Interface	DX10 commands
7	6	Reserved	
	7	Immediate Commands	Host Interface requests
0	7	Set FIFO Thresholds	
1	7	Read FIFO Counts	
2-7	7	Reserved	
0-7	8-B	Reserved	
	C	Host Interface Requests (with data buffer)	
0	C	Memory Load (multiple byte)	
1	C	Memory Dump (multiple byte)	
2	C	Read Reserved Memory Status	
3	C	X.21 Call Data Memory Load	
4	C	X.21 Call Data Memory Dump	
5-7	C	Reserved	Host Interface requests

Table 3-3. X.BCAIM Command Codes (Continued)

Modifier (Bits 1-3)	Opcode (Bits4-7)	Command	Type of Command
	D	Immediate Comrnands	Host Interface requests
0	D	BLWP Vector	
1	D	Memory Load (single word)	
2	D	Memory Dump (single word)	
3	D	Read ROM/RAM Size	
4	D	Read ID Switches	
5	D	Reserve Memory	
6	D	Release Reserved Memory	
7	D	Reserved	
			Host Interface requests
0-7	E	Reserved	
	F	Normal-Mode Diagnostic Requests	Diagnostic requests
0	F	CRU Data Transfer	
1	F	Write Interface	
2	F	Read Interface	
3-7	F	Reserved	Diagnostic requests

3.4.1 Channel Commands (Opcodes 0 Through 6)

Channel commands are commands involving interaction with the communication channel on the X.21 BCAIM.

There are two channel parameter tables in X.21 BCAIM RAM where parameters affecting communication channel operation are stored. The RS-232C, RS-422, and X.21 modes of operation of the X.21 BCAIM use the transfer channel parameter table (DTCPT). The X.21 mode of operation uses the call establishment channel parameter table (CECPT) during call establishment or call reception. In the RS-232C and RS-422 modes of operation, only the DTCPT is referenced. In the X.21 modes of operation, parameters in the CECPT are used to establish the connection, then the X.21 BCAIM is reinitialized using all applicable values from the DTCPT. In cases where values in the DTCPT are not applicable, the DTCPT parameter is ignored and its counterpart from the CECPT is used. Using two channel parameter tables in this manner allows compatibility between the earlier BCAIM board and the X.21 BCAIM.

The five bytes of information needed in the command block to issue channel commands with opcodes 0 through 5 are generally set up as follows:

Byte 0	Command code and modifier
Byte 1	Time-out value
Byte 2	Reserved
Byte 3,4	Byte count

Channel commands with opcode 6 require the five bytes of the command block to contain information other than that previously described. The opcode 6 command description includes the information required in the command block for opcode 6 commands.

The time-out value for channel-oriented commands specifies the time allowed for the command. For Open commands, the time-out specifies the maximum time allowed for completion of the command. For Read and Write commands, the time-out value specifies the maximum amount of time allowed before processing the first data character. The units of the time-out are in quarter-second or one-minute intervals as specified in the appropriate channel parameter table (Table 3-4 or Table 3-5). Bits 0 through 3 of the byte count word (bytes 3 and 4 of the command block) are not used. Bits 4 through 15 contain the 12-bit byte count.

The six bytes of information comprising the command completion status report are returned in the following format for channel commands.

Byte 0	Echo of the command byte issued
Bit 0	Error flag (= 1 if error detected)
Bits 1-7	Echo of command code
Byte 1	Time-out value
Byte 2	Reserved (echo of command block, byte 2)
Byte 3,4	Actual byte count
Bits 0-3	Reserved
Bits 4-15	12-bit byte count
Byte 5	Completion code

3.4.1.1 Time-Out/Abort Commands. The Time-Out/Abort commands (modifier 0 through 7, op-code 0) provide the capability of timing out a command or aborting all or part of the operation in progress. The command modifier (bits 1 through 3 of the command byte), specifies the type of Time-Out or Abort command to be executed.

Time-Out Command. The Time-Out command (modifier 0, opcode 0) provides the capability of notifying the host computer when the time-out value specified with the command expires. The X.21 BCAIM firmware does not queue Time-Out commands behind other commands so time-out processing begins immediately upon receiving the request. The channel parameter tables (Tables 3-4 and 3-5) specify the units of the time-out count and provide additional details on the use of the Time-Out. Only one Time-Out command can be issued to the X.21 BCAIM at one time.

Channel Abort Commands. The Channel Abort commands (modifiers 1 through 7, opcode 0) abort part or all of the operation in progress. The modifier code specifies the type of abort to be executed as follows:

Modifier Code	Type of Abort Command
1	Abort Write requests
2	Abort Read requests
3	Abort Write and Read requests
4	Abort Miscellaneous requests (Opens, Closes, Time-Outs)
5	Abort Writes and Miscellaneous
6	Abort Reads and Miscellaneous
7	Abort all requests

A modifier code of 1 causes all requests issued with a Write opcode to abort. A modifier code of 2 causes all requests issued with a Read opcode to abort. A modifier code of 3 causes all requests issued with either a Read or Write opcode to abort. A modifier code of 4 aborts any request other than a Read or Write, such as an Open Channel request. A modifier code of 5 aborts Write requests and Miscellaneous requests. Modifier code 6 aborts Read and Miscellaneous requests. Modifier code 7 aborts all requests for the communication channel.

3.4.1.2 Open Channel Command. The Open Channel command (opcode 1) enables the X.21 BCAIM communication channel for data transfer. The command modifier in byte 0 of the command block specifies the type of open. For RS-232C operation of the X.21 BCAIM, the command modifier specifies the following types of opens:

Modifier Code	Type of Open Command
0	Illegal
1	Wait for ring
2	Assert DTR
3	Wait for ring
4	Assert DTR
5	Wait for ring
6	Assert DTR
7	Wait for ring

Word CPISRF of the DTCPT specifies additional open processing when the X.21 BCAIM is operating in the RS-232C mode. The bits in CPISRF determine how the DCE signals DSR, DCD, RTS, and CTS are handled during processing of an Open Channel command.

For operation of the X.21 BCAIM in an X.21 network, the command modifier in byte 0 of the command block specifies the following types of opens:

Modifier Code	Type of Open Command
0	Illegal
1	Wait for call reception
2	Initiate call
3	Wait for call reception
4	Initiate call
5	Wait for call reception
6	Initiate call
7	Wait for call reception

When the host computer issues an Open Channel command, byte 1 of the five-byte command block specifies the maximum time allowed for completion of the command. The appropriate channel parameter table specifies the units of the time-out (quarter-second or one-minute intervals). Bytes CPOPNT and CPCDLY of the DTCPT specify two other time-out parameters associated with Open Channel commands in the RS-232C mode of operation. The Write Parameters command can modify the time-out values in the channel parameter tables as well as any other parameter specified in the channel parameter tables if other than the default parameters are needed. The Write Parameters command and the channel parameter tables are discussed in detail later in this section.

Byte 2 of the command block defines the protocol selection. The hexadecimal value of the bits in byte 2 selects protocols as follows:

Hexadecimal Value of Byte 2	Protocol Selected
0	Current channel parameter table values
1	BOP NRZI
2	BOP Direct
3	Reserved (BSC 3270)
4	BSC 3780
5	Reserved (UPA/914A Host)
6	Reserved (810 line printer)
7	Reserved (BSC 2780)
8	X.21 Protocol (Switched Line)
9	X.21 Protocol (Leased Line)
A,B	Reserved
C-F	Reserved for downloaded protocols

If byte 2 is zero, the protocol selection and the values currently in the channel parameter tables are not modified. If byte 2 is any value other than zero, the values in the selected protocol table are copied into the appropriate channel parameter table.

The most significant bit (bit 0) of the protocol select byte (byte 2) acts as a flag for write parameters in the Open Channel command. When bit 0 is zero, the host computer can issue Write Parameters commands to the X.21 BCAIM only when no channel command activity is in progress. When bit 0 is set to one, Write Parameters commands are accepted when there is channel command activity in progress.

Bit 1 of the protocol select byte acts as a flag for protocol selection when the host computer issues an Open Channel command. If bit 1 is set to zero, protocol selection data is loaded into the DTCPT. If bit 1 is set to one, protocol selection data is loaded into the CECPT.

In some cases, the X.21 BCAIM must send or receive certain signal combinations for proper open processing. Refer to the descriptions of the two channel parameter tables later in this section for more detail.

The command completion status report for Open Channel commands has the following format when operating in the X.21 switched line mode:

Byte/Bits	Meaning
Byte 0	Echo of command
Bit 0	Error flag (1 = error detected)
Bits 1-7	Echo of command code
Byte 1	Time-out value
Byte 2	Echo of command byte 2
Byte 3	>0X if an X.21 T(x) time-out occurred
Byte 4	X.21 BCAIM state at time of error
Byte 5	Completion code

A completion code of >13 indicates an X.21 time-out error. When a time-out error occurs, byte 3 of the completion status report contains >0X, where X indicates which time-out (0 through 7) occurred. Refer to the CECPT for descriptions of the time-outs.

If the completion code contains >40, it indicates that during the call, the X.21 network returned a call progress signal (CPS) requiring that the call be aborted (X.21 switched line operation only). In this case, byte 3 of the completion status report contains a code that defines why the call was aborted. The X.21 network specification defines the CPS codes.

Byte 4 of the command completion status report contains a code indicating the state that the X.21 BCAIM was in at the time the error occurred. Appendixes E and F define these states.

3.4.1.3 Close Channel Command. The Close Channel command (opcode 2) disables the communication channel. Use of this command when operating in the RS-232C mode implies deassertion of data terminal ready (DTR) and request to send (RTS) and an optional delay until the next Open command is processed. For X.21 operation, this command implies that the DTE Clear Request state be entered with an optional delay until the next Open command is processed. Any operation in progress on the communication channel when the host issues the Close Channel command is terminated with an error code >18 (line disconnect). When this command is issued, the modifier code is ignored by the X.21 BCAIM. Tables 3-7 and 3-8 define error codes.

For X.21 switched line operation, Close command completion status is reported before charge information is obtained from the X.21 network, assuming the information is requested and is available. Any information call without a request for charge information is rejected after the Ready state when the Data Transfer state is entered. After a Close command is completed for normal X.21 operation, the X.21 BCAIM signals the DTE Controlled Not Ready state. For X.21 leased line operation, the Closed state of the board is the Ready state.

3.4.1.4 Write Command. The Write command (opcode 3) specifies the transmission of host data over the X.21 BCAIM communication channel or to write parameters to either of the channel parameter tables. The five-byte command block is written to the X.21 BCAIM prior to transferring the transmit data. Multiple Write commands can be issued as long as the transmit data associated with each command is transferred to the X.21 BCAIM in the same order the commands were issued. For instance, data associated with the first Write command must be transferred to the BCAIM before any data associated with the second Write command can be transferred. The X.21 BCAIM uses only the byte count to keep track of transmit data associated with a particular Write command.

Commands to the X.21 BCAIM can be interleaved with the transmit data. When the X.21 BCAIM output FIFO is full, it will not accept transmit data; however, additional commands can be issued while waiting for more space in the FIFO.

The command modifier specifies the type of Write command to be executed as follows:

Modifier Code	Type of Write Command
0–3	Initial character detect routine entry points 0 through 3
4–6	Reserved
7	Write Parameters command

Modifiers 0 through 3 specify entry points for initial Character Detection Transmit states. Refer to the discussion of character detection routines later in this section for a general discussion on implementing character detection routine entry points. The protocol documentation in the appendixes of this manual contains specific information on character detection routine entry points for each supported protocol.

A modifier code of 4 is processed in the same manner as a modifier of 0 for bit-oriented protocols except that continuous RTS is forced after the data frame is transmitted. After a Write command with a modifier of 4 is issued, the X.21 BCAIM remains in the continuous RTS mode until a Write command with a modifier other than 4 is issued. This temporary continuous RTS mode is only implemented for bit-oriented protocols.

For asynchronous operation, a Write command with >8000 in bytes 3 and 4 of the command block forces the X.21 BCAIM into the character mode of operation. Character mode operation is discussed later in this section.

Write Parameters Command. The Write Parameters command (modifier 7, opcode 3) modifies the channel parameter tables where the X.21 BCAIM firmware obtains protocol information. Byte 1 of the command block specifies the protocol selection. The Open Channel command describes protocols that can be selected. Byte 2 specifies the offset from byte 0 into the channel parameter table to identify the location where the first byte will be written. Bytes 3 and 4 of the command specify how many bytes are being transferred into the table. The X.21 BCAIM does not accept any other commands until the Write Parameters command completes.

Bit 0 of byte 1 in the Write Parameters command can be set to allow special processing of the Write Parameters command. When bit 0 is set to zero, the Write Parameters command is allowed only when there is no other channel command activity on the board. When bit 0 is set to one, the X.21 BCAIM accepts the Write Parameters command even if there is other activity in progress provided that a special Open command was previously issued. Use extreme caution with this feature since some Write Parameter changes issued when the board is active can cause unpredictable operation.

The TMS 9903 on the X.21 BCAIM is not reset or reinitialized unless the Write Parameter command issued is one that affects TMS 9903 operation. The ability to issue Write Parameters commands when the board is active is useful for passing information from a host line control to a downloaded character detection routine while the board is operating.

Bit 1 of byte 1 of the Write Parameters command block allows you to select which channel parameter table the command will load. When bit 1 is set to zero, protocol selection data is loaded into the DTCPT. When bit 1 is set to one, protocol selection data is loaded into the CECPT.

Figure 3-8 shows how the DTCPT is organized; Table 3-4 describes how to use the information in the table. Figure 3-9 illustrates the CECPT. Table 3-5 describes the CECPT following a description of the DTCPT.

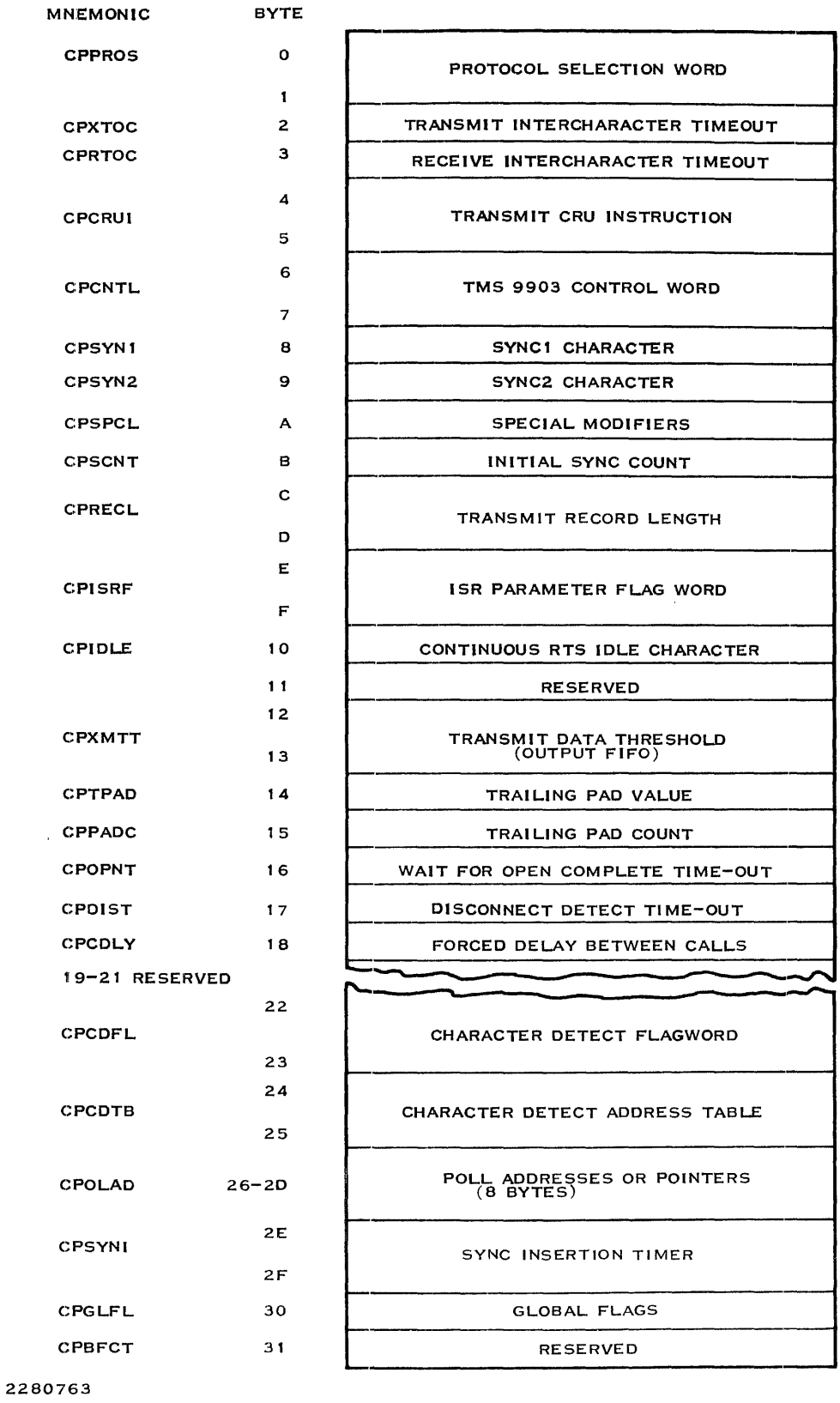


Figure 3-8. Data Transfer Channel Parameter Table

Table 3-4. Data Transfer Channel Parameter Table

Word/Byte Mnemonic	Offset	Bits	Meaning
CPPROS	0000	12-15	This word selects the operating mode of the TMS 9903. The bits of the word are used as follows:
		0,1	Reserved.
		2	Internal clock select. 0 = External clock 1 = Internal clock (rate specified by bits 4-7)
		3	Connect internal clock to transmit clock external pin. 0 = External clock connected 1 = Internal clock connected
		4-7	Transmit speed selection. 0 = 50 bps 1 = 75 bps 2 = 110 bps 3 = 134.5 bps 4 = 150 bps 5 = 200 bps 6 = 300 bps 7 = 600 bps 8 = 1200 bps 9 = 1800 bps A = 2400 bps B = 3600 bps C = 4800 bps D = 7200 bps E = 9600 bps F = (Reserved)
		8	Echo. 0 = Enable echo 1 = Disable echo
		9	RTS. 0 = Switched RTS 1 = Continuous RTS
		10	Squelch receiver during transmit. 0 = Receiver squelched 1 = Receiver not squelched
		11	Reserved.

Table 3-4. Data Transfer Channel Parameter Table (Continued)

Word/Byte Mnemonic	Offset	Bits	Meaning
CPPROS	0000	12-15	Receive speed select. 0 = 50 bps 1 = 75 bps 2 = 110 bps 3 = 134.5 bps 4 = 150 bps 5 = 200 bps 6 = 300 bps 7 = 600 bps 8 = 1200 bps 9 = 1800 bps A = 2400 bps B = 3600 bps C = 4800 bps D = 7200 bps E = 9600 bps F = (Reserved)
CPXTOC	0002	0-7	Transmit Intercharacter Time-Out. This byte contains a time-out count to specify the time interval allowed between transmit characters after the first character is transmitted. Quarter-second or one-minute time intervals are specified for this timer in bit 0 of CPISRF. The time-out for transmission of the first character is specified in byte 1 of the five-byte command block.
CPRTOC	0003	0-7	Receive Intercharacter Time-Out. This byte contains a time-out count to specify the time interval allowed between receive characters after the first character is received. Quarter-second or one-minute intervals are specified for this timer in bit 1 of CPISRF. The time-out for reception of the first character is specified in byte 1 of the five-byte command block.
CPCRUI	0004	0-15	Transmit CRU Instruction. This word contains an LDCR instruction that is referenced by an execute instruction to transmit data characters. This allows specifying the character length required by the protocol. The format is LDCR *R10,N; where N is the number of bytes per character.
CPCNTL	0006	0-15	TMS 9903 Control Word. This word specifies the contents of the control word for the TMS 9903. The least significant 12 bits of this word are stored in the TMS 9903 control register via an LDCR instruction. Refer to the *9900 Family Systems Design and Data Book, Microprocessor Series, 1st Edition*, part number 97049-118-NI, for definition of the TMS 9903 control word.
CPSYN1	0008	0-7	Sync Character. This byte is stored in the TMS 9903 sync1 register.

Table 3-4. Data Transfer Channel Parameter Table (Continued)

Word/Byte Mnemonic	Offset	Bits	Meaning
CPSYN2	0009	0-7	Sync Character. This byte is stored in the TMS 9903 sync2 register.
CPSPCL	000A	0	Special Modifiers. Bit 0 = 0 TMS 9903 transparency not selected. = 1 TMS 9903 transparency selected.
		1-7	Reserved.
CPSCNT	000B	0-7	Initial Sync Count. This byte specifies the number of sync characters to be transmitted at the start of a data frame. The byte transmitted is the value of CPSYN1.
CPRECL	000C	0-15	This word specifies the transmit record length. (Used by 2780/3780 character detection routine.)
CPISRF	000E	0-15	This word contains the ISR flags. The flags are defined as follows: Bit 0 Transmit intercharacter time-out = 0 Transmit time-out in quarter seconds = 1 Transmit time-out in minutes Bit 1 Receive intercharacter time-out = 0 Receive time-out in quarter seconds = 1 Receive time-out in minutes Bit 2 Open request time-out = 0 Open time-out in quarter seconds = 1 Open time-out in minutes Bit 3 No operation time-out = 0 No-op time-out in quarter seconds = 1 No-op time-out in minutes Bit 4 Receiver clear select = 0 Do not clear receiver after frame = 1 Clear receiver after frame Bit 5 CRB queue select = 0 Single CRB request queue = 1 Separate transmit and receive CRB queues Bit 6 RTS open assertion = 0 Do not assert RTS on opens = 1 Assert RTS on opens Bit 7 DCD select = 0 Do not wait on DCD during opens = 1 Wait for DCD during opens

Table 3-4. Data Transfer Channel Parameter Table (Continued)

Word/Byte Mnemonic	Offset	Bits	Meaning
			Bit 8 RTS open completion assertion = 0 Leave RTS in present condition after open = 1 Deassert RTS after open completion Bits 9--10 Reserved for character detect Bit 11 DSR support = 0 Wait for DSR on open and monitor DSR during connection = 1 Do not wait for DSR on open and ignore DSR during connection Bit 12 Reserved Bits 13-15 Used by X.21 BCAIM firmware only = 0 BOP mode = 2 COP synchronous mode = 4 Asynchronous mode
CPIDLE	0010	0-7	Idle Fill Character. This byte defines the character to be used for idle fill when continuous RTS is specified.
		8-15	Reserved.
CPXMTT	0012	0-15	Output FIFO Transmit Data Threshold. This word specifies the minimum number of data bytes required in the X.21 BCAIM output FIFO before data transmission is initiated. The X.21 BCAIM firmware waits until the number of bytes specified by CPXMTT has been transferred from the host to the X.21 BCAIM before initiating transmission of data over the communication line. The only exception is when the transmit request byte count is less than the value in CPXMTT. In this case, all transmit data for the request must be in the output FIFO before transmission begins.
CPTPAD	0014	0-7	This byte contains the pad data character used when pads are transmitted at the end of a data transmission block.
CPPADC	0015	0-7	This byte contains the number of times the pad character will be transmitted at the end of a data transfer.
CPOPNT	0016	0-7	The DCE interface signals must be in a specific state and must remain in that state for a specific period of time for a successful open. CPISRF specifies the state of the signals; this byte contains a timer that specifies the number of quarter-second intervals the signals are to remain in the state specified in CPISRF.

Table 3-4. Data Transfer Channel Parameter Table (Continued)

Word/Byte Mnemonic	Offset	Bits	Meaning
CPDIST	0017	0-7	This byte contains the number of quarter-second intervals that one of the DCE signals specified in CPISRF may be off (lost) before it is considered to be a disconnect condition. If one of the DCE signals is off for the period of time specified by this timer, the communication channel is disconnected.
CPCDLY	0018	0-7	This byte specifies the number of quarter-second intervals required after a successful Close before the X.21 BCAIM will process an Open request. If the X.21 BCAIM receives an Open request before this timer has expired, the request is held until the timer expires and then is processed.
CPCDFL	0022	0-15	This word contains protocol dependent character detection flags. Bit 0 Character detect flag = 0 3780 table type = 1 2780 table type Bit 1 Receiver abort detection flag = 0 Report receive abort on first character = 1 Ignore receive abort on first character Bits 2-15 Reserved
CPCDTB	0024	0-15	This word contains the address of the character detection table. The table contains the addresses of initial character detect entry points for Read, Write, and Chained Write modifier codes. When a character detection routine is downloaded, this word must be updated to contain the address of the character detect entry point table.
CPOLAD	0026	8 bytes	These eight bytes contain the poll addresses used in the implementation of receive poll address detection by character detection routines.
CPSYNI	002E	0-15	This word specifies the number of quarter-second intervals to wait before inserting a sync character in the transmit data. It is used by 2780/3780 and 3270 character detection routines.
CPGLFL	0030	0-7	This byte contains global flags and is reserved for firmware use.
CPBFCT	0031	0-7	This byte is reserved for firmware use.

MNEMONIC	BYTE(S)	
CXPROS	0	PROTOCOL SELECTION WORD
	1	
	2	RESERVED
	3	
CXCRUI	4	TRANSMIT CRU INSTRUCTION
	5	
CXCNTL	6	TMS 990 CONTROL WORD
	7	
CXSYN1	8	SYNC 1 CHARACTER
CXSYN2	9	SYNC 2 CHARACTER
CXSPCL	A	SPECIAL MODIFIERS
CXSCNT	B	INITIAL SYNC COUNT
CXXCNC	C	CALL PROGRESS INFORMATION BLOCK COUNT
CXREC1	D	CALL PROGRESS INFORMATION BLOCK LENGTH
CXISRF	E	ISR PARAMETER FLAG WORD
	F	
CXIDLE	10	CONTINUOUS RTS IDLE CHARACTER
CXREC2	11	CALL CHARGE INFORMATION LENGTH
CXCDFL	12	RECEIVE ERROR FLAG MASK
	13	
CXTPAD	14	TRAILING PAD VALUE
CXPADC	15	TRAILING PAD COUNT
CXCMTC	16	CLOCK COUNT FOR X.21
CXDIST	17	DISCONNECT DETECT TIMEOUT
CXCDLY	18	FORCED DELAY BETWEEN CALLS
CXXT0	19	X.21 TIME-OUT T0
CXXT1	1A	X.21 TIME-OUT T1
CXXT2	1B	X.21 TIME-OUT T2
CXXT3A	1C	X.21 TIME-OUT T3A
CXXT3B	1D	X.21 TIME-OUT T3B
CXXT4	1E	X.21 TIME-OUT T4
CXXT5	1F	X.21 TIME-OUT T5
CXXT6	20	X.21 TIME-OUT T6
CXXT7	21	X.21 TIME-OUT T7
CXSTBL	22	POINTER TO STEADY STATE PROCESSING TABLE
	23	
CXTRNC	24	TMS 9901 CLOCK TRAINING COUNT
	25	
CXXCNT	26	BLOCK COUNT OF DCE INFORMATION
CXREC3	27	BLOCK LENGTH OF DCE INFORMATION
CXDCEI	28	POINTER TO DCE INFORMATION TABLE
	29	
CXXPAD	2A	TERMINATING PAD CHARACTER
CXCHGC	2B	CALL CHARGE INFO BLOCK START CHARACTER
CXXCPT	2C	POINTER TO CALL PROGRESS TABLE ADDRESS
	2D	
CXREGS	2E	REGISTRATION TERMINATION CHARACTER
CXCIDL	2F	IDLE CHARACTER EXPECTED IN STATE 05
CXXSET	30	X.21 LEASED LINE ENTRY VECTOR

2283252

Figure 3-9. Call Establishment Channel Parameter Table

Table 3-5. Call Establishment Channel Parameter Table

Word/Byte Mnemonic	Offset	Bits	Meaning
XPROS	0000		This word selects the operating mode of the TMS 9903. For X.21 operation, use external clocking for both transmitter and receiver. Select disable echo, continuous RTS, and full-duplex (receiver not squelched) options. The bits of this word have the following meaning:
		0,1	Reserved.
		2	Clock select. 0 = External clock 1 = Internal clock
		3	EIA pin 24 connection. 0 = External clock on pin 24 1 = Internal clock on pin 24
		4-7	Transmit speed selection. >0 = speed A 50 bps >1 = speed B 75 bps >2 = speed C 110 bps >3 = speed D 134.5 bps >4 = speed E 150 bps >5 = speed F 200 bps >6 = speed G 300 bps >7 = speed H 600 bps >8 = speed I 1200 bps >9 = speed J 1800 bps >A = speed K 2400 bps >B = speed L 3600 bps >C = speed M 4800 bps >D = speed N 7200 bps >E = speed O 9600 bps >F = speed P Reserved
		8	Echo suppression. 0 = Enable echo 1 = Disable echo
		9	RTS selection. 0 = Switched RTS 1 = Continuous RTS
		10	Duplex selection. 0 = Half duplex (receiver squelched) 1 = Full duplex (receiver not squelched)
		11	Reserved.

Table 3-5. Call Establishment Channel Parameter Table (Continued)

Word/Byte Mnemonic	Offset	Bits	Meaning
		12-15	Receive speed selection. >0 = speed A 50 bps >1 = speed B 75 bps >2 = speed C 110 bps >3 = speed D 134.5 bps >4 = speed E 150 bps >5 = speed F 200 bps >6 = speed G 300 bps >7 = speed H 600 bps >8 = speed I 1200 bps >9 = speed J 1800 bps >A = speed K 2400 bps >B = speed L 3600 bps >C = speed M 4800 bps >D = speed N 7200 bps >E = speed O 9600 bps >F = speed P Reserved
	0002	0-15	Reserved.
CXCRUI	0004	0-15	Transmit CRU Instruction. This word contains an LDCR instruction that is referenced by an execute instruction to transmit data characters. This allows specifying the character length required by the protocol. The instruction is LDCR *R10,N, where N is the number of bits per character. Eight-bit characters are used for X.21.
CXCNTL	0006	0-15	TMS 9903 Control Word. This word specifies the contents of the control word for the TMS 9903. The least significant 12 bits of this word are stored in the TMS 9903 control register with an LDCR instruction. Refer to the *9900 Family Systems Design and Data Book, Microprocessor Series, First Edition*, part number 97049-118-NI, for definition of the TMS 9903 control word.
CXSYN1	0008	0-7	Sync1 Character. This byte is stored in the TMS 9903 sync1 register. For X.21 operation, this byte represents the International Alphabet Number 5 (IA5) 1/6 character SYN.
CXSYN2	0009	0-7	Sync2 Character. This byte is stored in the TMS 9903 sync2 register. This byte specifies the IA5 character that the network will idle during the proceed to select state. This IA5 character 2/11, is defined as a + character.
CXSPCL	000A	0	TMS 9903 transparency flag. 0 = Transparency flag off 1 = Transparency flag on
		1-7	Reserved.

Table 3-5. Call Establishment Channel Parameter Table (Continued)

Word/Byte Mnemonic	Offset	Bits	Meaning
CXSCNT	000B	0-7	Initial Sync Count. This byte specifies the number of IA5 SYN characters to be transmitted at the start of selection signal transmission.
CXXCNC	000C	0-7	This byte contains the call progress information block count.
CSREC1	000D	0-7	This byte specifies the size of the largest block of information that the X.21 network will pass during the call progress signal state.
CXISRF	000E		ISR Parameter Flag Word. This word contains the ISR flag bits. The bits are defined as follows:
		0,1	Reserved.
		2	Open command time-out. 0 = Open time-out in quarter seconds 1 = Open time-out in minutes
		3	No operation time-out. 0 = No-op time-out in quarter seconds 1 = No-op time-out in minutes
		4	Reserved.
		5	CRB queue select. 0 = Single CRB queue 1 = Separate transmit and receive queues
		6	Reserved.
		7	Even parity detection. 0 = Do not abort call on even parity character 1 = Abort call on even parity character
		8	Call charge information. 0 = Accept call charge information 1 = Do not accept call charge information
		9	Network monitor bit. 0 = Wait for network on open and monitor network while connected 1 = Do not wait for network on open and do not monitor network after connection
		10,11	Reserved.
		12	First character in DCE provided information is the keyboard identifier. For Japanese X.21 implementation, this information is in the second data character instead of the first.
		13-15	Reserved.

Table 3-5. Call Establishment Channel Parameter Table (Continued)

Word/Byte Mnemonic	Offset	Bits	Meaning
CXIDLE	0010	0-7	Idle Character. This byte specifies the IA5 data character that the X.21 network will idle during the call accepted state. This IA5 character is 0/7, the BEL character.
CXREC2	0011	0-7	Call Charge Information Length. For X.21 operation, this byte specifies the size of the largest block of information that the network will pass during the call charge information state.
CXCDFL	0012	0-15	Receive Error Flag Mask.
CXTPAD	0014	0-7	Trailing Pad Value. This byte contains the terminating pad character to be transmitted at the end of the selection sequence. For X.21 operation, this IA5 byte represents the + character 2/11.
CXPADC	0015	0-7	Trailing Pad Count. This byte contains the number of times the pad character will be transmitted at the end of the selection signal state.
CXCMTC	0016	0-7	This byte contains the clock count for X.21 operation.
CXDIST	0017	0-7	Disconnect time-out value.
CXCDLY	0018	0-7	This byte specifies the time period, in quarter-second intervals, that the X.21 BCAIM waits after a successful close request has completed before an open request is accepted.
CXXT0	0019	0-7	Time-out T0. This byte contains the maximum number of quarter-second intervals from the time the first SYN character is received in the ready state until the incoming call state is entered. This time period is nominally three seconds.
CXXT1	001A	0-7	Time-out T1. This byte contains the maximum number of quarter-second intervals from the time the X.21 BCAIM enters the call request state until the proceed to select state is entered. This time period is nominally three seconds.
CXXT2	001B	0-7	Time-out T2. This byte contains the maximum number of quarter-second intervals from the time the X.21 BCAIM enters the DTE waiting state until: 1. The proceed to select state is entered 2. The ready for data state is entered 3. The DCE clear indication state is entered This time period is nominally 20 seconds.

Table 3-5. Call Establishment Channel Parameter Table (Continued)

Word/Byte Mnemonic	Offset	Bits	Meaning
CXXT3A	001C	0-7	Time-out T3A. This byte contains the maximum number of quarter-second intervals from the time the X.21 BCAIM enters the call progress signal state until the ready for data or the DCE clear indication state is entered. This time period is nominally two seconds. If the first byte received from the network during the call progress state is an IA5 0 character 3/0, then the time period specified in CXXT3B is used.
CXXT3B	001D	0-7	Time-out T3B. This byte contains the maximum number of quarter-second intervals from the time the X.21 BCAIM enters the call progress signal state until the ready for data or the DCE clear indication state is entered. This time period is nominally 60 seconds.
CXXT4	001E	0-7	Time-out T4. This byte contains the maximum number of quarter-second intervals from the time the X.21 BCAIM enters the call accepted state until the ready for data or the DCE clear indication state is entered. This timer is reset each time a new DCE provided information state is entered. This time period is nominally two seconds.
CXXT5	001F	0-7	Time-out T5. This byte contains the maximum number of quarter-second intervals from the time the X.21 BCAIM enters the DTE clear request state until the DCE ready state is entered. This time period is nominally two seconds.
CXXT6	0020	0-7	Time-out T6. This byte contains the maximum number of quarter-second intervals from the time the X.21 BCAIM enters the DTE clear confirmation state until the DCE ready state is entered. This time period is nominally two seconds.
CXXT7	0021	0-7	Time-out T7. This byte contains the maximum number of quarter-second intervals from the time the X.21 BCAIM enters the ready state after a call in which charge information was requested until the incoming call state is entered. This time period is nominally one-half second.
CXSTBL	0022	0-15	This word contains the address of the steady state processing table.
CXTRNC	0024	0-15	This word contains the TMS 9901 clock training count.
CXXCNT	0026	0-7	This byte contains the number to be obtained from DCE provided information blocks. The size of the buffers is specified in CXREC3.
CXREC3	0027	0-7	For X.21 operation, this byte represents the largest block of information that the network will pass during the DCE provided information state.

Table 3-5. Call Establishment Channel Parameter Table (Continued)

Word/Byte Mnemonic	Offset	Bits	Meaning
CXDCEI	0028	0-15	This word contains the address of the DCE provided information table. The DCE provided information table is used to validate the first DCE provided information character of each DCE provided information block received from the network. If the character is invalid, then the decision to clear the call is based upon bits 11 and 12 of word CXISRF in the CECPT. The following layout example applies to the DCE provided information table:

Offset	Character	Meaning
>0000	2/10 (#)	Calling or called line ID
>0001	2/15 (/)	Charging information block
>0002	— —	—
>NNNN	>FF —	Table terminator

CXXPAD	002A	0-7	This byte contains the terminating pad character to be received at the end of the call progress block or DCE provided information block. For X.21 operation, this IA5 byte represents the + character, 2/11.
CXCHGC	002B	0-7	This byte contains the character that the X.21 network transmits at the start of the charging information block to identify the call as a call in which charge information will be transmitted by the network. For X.21 operation, this IA5 byte represents the / character, 2/15.
CXXCPT	002C	0-15	This word contains the address of the call progress table. The call progress table is used to convert the call progress signals received from the network into actions taken by the X.21 BCAIM firmware. The decision is based upon the first four bytes of the call progress signals, which constitute the code group. The layout of the call progress table is as follows:

Offset	Code Group	Action Value	Meaning
>0000	0	>00	Without clearing, call accepted
>0001	1	>04	With clearing, long term illegal
>0002	2	>02	With clearing, short term
>0003	3	>04	With clearing, long term illegal
>0004	4	>01	With clearing, long term
>0005	5	>01	With clearing, long term
>0006	6	>02	With clearing, short term
>0007	7	>01	With clearing, long term

Table 3-5. Call Establishment Channel Parameter Table (Continued)

Word/Byte Mnemonic	Offset	Bits	Meaning

Offset	Code Group	Action Value	Meaning
>0008	8	>03	With clearing, select signal accepted
>0009	9	>04	With clearing, long term illegal
>000A	—	>NNNN	Exception table address

Each action in the preceding table references a value in a RAM table that points to the address of a special X.21 call character detect procedure. The call character detect procedure processes the call progress signal received from the X.21 network. This simplifies changing the meaning of the code group actions when required.

The code range of call progress signals is from >00 to >99 with values separated by a , character (2/12). Any value outside this range is considered to be DCE provided information.

The exception table is a list of exceptions to the call progress table. During call signal processing, the call progress signal is checked to see if it can be found in the exception table and if not found there, the call progress table is checked.

A zero entry for the exception table address indicates that no exceptions are allowed.

Offset	Exception Code	Action Value	Meaning
>0000	>NN	>0X	Exception value
—	—	—	—
>NNNN	>FF	—	Terminator

CXREGS	002E	0-7	This byte contains the registration termination character.
CXCIDL	002F	0-7	This byte contains the idle character expected in state 05.
CXXSET	0030	0-15	This word contains the X.21 leased line vector.

3.4.1.5 Read Command. The Read command (opcode 4) specifies the reception of data into host memory from the X.21 BCAIM communication channel, to read X.21 BCAIM status, or to read protocol parameters from the channel parameter tables. The last two bytes of the five-byte command block specify the requested byte count. The data is returned to the host followed by the command completion status report. The modifier code specifies the type of Read command to be executed as follows:

Modifier Code	Type of Read Command
0-3	Modifier used to enter the character detection routine at different initial receive states
4-6	Reserved
7	Read Parameters

Data from the communication line is always transferred to the host before completion status is reported for the receive command. Data transfers can be interrupted at any time to transfer a command completion status report for another outstanding command. If more than one Read command is outstanding, the data associated with the oldest request is transferred to the host first. The Read command terminates when the byte count is decremented to zero, the character detection routine detects a terminating condition, or an error occurs.

When the X.21 BCAIM operates in the asynchronous mode, a Read command with >8000 in bytes 3 and 4 of the command block forces the board into the character read mode. Refer to the discussion on character mode operation later in this section for more information.

Six-byte command completion status reports for normal completions of Read commands follow the format described at the beginning of the channel command discussion. A special one-byte completion status report is returned to the host when specified by the character detection routine. In this case, the X.21 BCAIM uses the current request to process data from the next frame and notifies the host to do the same. When the host receives the receive restart completion status report, it must restore its data buffer address and byte count to their initial values and discard any invalid data already received. This type of status report is useful when a portion of the data has been received before the character detection routine makes a decision to ignore the data frame. The special one-byte receive reprocess completion status report consists of:

- The receive restart flag (CRU input bit 9) = 1.
- The status flag (CRU input bit 8) = 1.
- Byte 2 of the five-byte Read command block is written to the data byte of the CRU interface input word.
- The input data valid flag (CRU input bit 10) = 1.

The time-out value in byte 1 of the Read command block is handled in a different manner for receive reprocess completions. The value in byte 1 still specifies the time allowed to receive the first byte of data but for receive reprocess completions, it accumulates the total time required for all consecutive reprocesses of the same Read command. The timer is stopped each time a byte of data is processed but is restarted each time the character detection routine issues a receive restart completion report. If the accumulated time for reprocessing exceeds the time-out value in the first byte of the command block, a receive reprocess time-out error (>47) is returned for the current Read request.

Read Parameters Command. The Read Parameters command (modifier 7, opcode 4) provides a means of reading information from either of the two channel parameter tables. Byte 1 of the five-byte command block must contain an offset from byte 0 of the selected channel parameter table to the first byte that is to be read from the table. Contiguous bytes of data from the table are transferred to the host buffer starting with the byte pointed to by the offset in byte 1. Bit 1 of byte 2 (the protocol select byte) specifies which of the two channel parameter tables the data will be read from. When bit 1 is set to zero, data is read from the DTCPT, and when set to 1, data is read from the CECPT. Bytes 3 and 4 of the command block must specify the number of bytes to be transferred to the host. The six-byte command completion status report is transferred to the host before the data for this command.

3.4.1.6 Chained Write Command. The Chained Write command links a Write command and a Read command. A Chained Write command (modifiers 0 through 3, opcode 5) is issued first for the write half of the Chained Write command. Then a second Chained Write (modifiers 4 through 7, opcode 5) must be issued for the read half of the command. The command modifiers specify the write and read character detection routine entry points; 0 through 3 for write character detect entry points 0 through 3 and 4 through 7 for read character detect entry points 0 through 3. Commands >45, >55, >65, and >75 are processed in the same manner as commands >04, >14, >24, and >34. Unique processing and requirements for the Chained Write command are as follows:

- The X.21 BCAIM will not initiate the write half of a Chained Write until it receives the read half of the command.
- Separate completions are reported for each half of the command.
- If an error is detected in the write half of the command, the same error is reported for the read half. In this case, the read half of the command is not executed but is returned with the error.
- The ISR flagword CPISRF in the DTCPT must specify a single CRB request queue when Chained Write commands are used. An illegal command error is returned if a single CRB request queue is not specified.
- Only one Chained Write command can be issued to the X.21 BCAIM at one time. One Chained Write command includes both the read and write halves of the command.
- A receive restart completion is valid for the receive portion of the Chained Write command. When it occurs, only the receive portion of the request is reprocessed.

3.4.2 DX10 Channel Commands

The opcode 6 commands with modifiers 0 through 4 and 7 are reserved for future use. Opcode 6 commands with modifiers 5 and 6 are special commands that allow you to write to the communications controller CRU interface and to read information from the CRU interface. The following paragraphs present details on the use of opcode 6 commands with modifiers 5 and 6.

3.4.2.1 Write Channel Interface Command. The Write Channel Interface command (modifier 5, opcode 6), allows you to specify the state of certain CRU interface bits on the X.21 BCAIM. Bytes 1 through 4 of the five-byte command block specify the state of the interface bits (Figure 3-10). Table 3-6 explains the use of the bits in bytes 1 through 4.

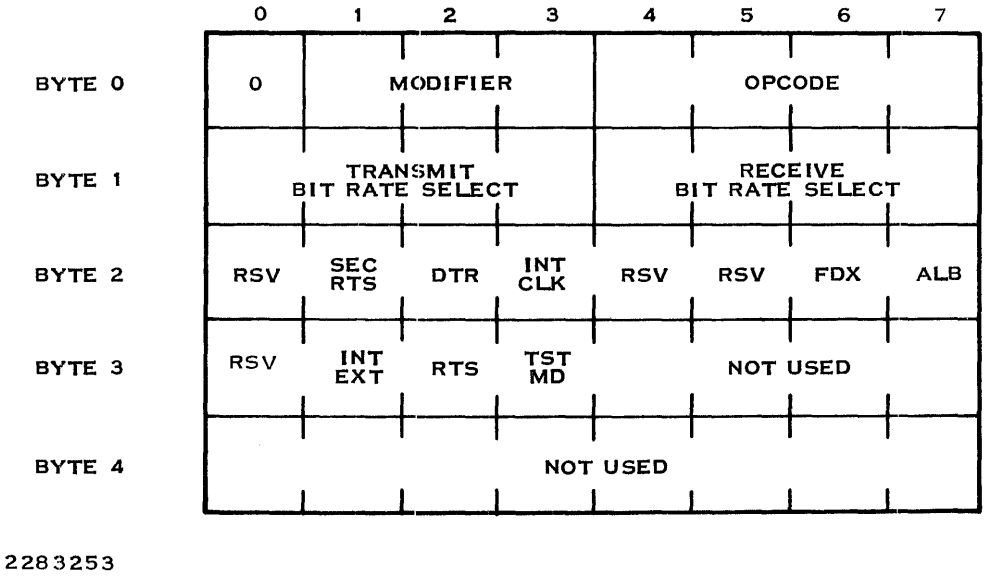


Figure 3-10. Command Block Format for Write Channel Interface Command

Table 3-6. Bit Definitions, Write Channel Interface Command

Byte	Bits	Meaning
1	0-3	Transmit Rate Selection 0 = 50 bps 1 = 75 bps 2 = 110 bps 3 = 134.5 bps 4 = 150 bps 5 = 200 bps 6 = 300 bps 7 = 600 bps 8 = 1200 bps 9 = 1800 bps A = 2400 bps B = 3600 bps C = 4800 bps D = 7200 bps E = 9600 bps F = Reserved
1	4-7	Receive Rate Selection 0 = 50 bps 1 = 75 bps 2 = 110 bps 3 = 134.5 bps 4 = 150 bps 5 = 200 bps 6 = 300 bps 7 = 600 bps 8 = 1200 bps 9 = 1800 bps A = 2400 bps B = 3600 bps C = 4800 bps D = 7200 bps E = 9600 bps F = Reserved
2	0	Reserved
2	1	Secondary Request to Send (SRTS)/ X.21 R/I Interrupt Enable (RIIE) 0 = SRTS off, RIIE on 1 = SRTS on, RIIE off
2	2	Data Terminal Ready (DTR)/ X.21 Control Enable Output 0 = DTR off, X.21 control off 1 = DTR on, X.21 control on

Table 3-6. Bit Definitions, Write Channel Interface Command (Continued)

Byte	Bits	Meaning
2	3	Internal Clock Select 0 = External clock 1 = Internal clock
2	4,5	Reserved
2	6	Full-Duplex Select 0 = Half duplex (receiver squelched during transmissions) 1 = Full duplex
2	7	Analog Loopback 0 = Analog loopback off 1 = Analog loopback on
3	0	Reserved
3	1	Output External Clock Select 0 = Internal clock 1 = External clock
3	2	Request to Send (RTS) Control 0 = Request to send off 1 = Request to send on
3	3	TMS 9903 Test Mode 0 = TMS 9903 test mode off 1 = TMS 9903 test mode on
3	4-7	Reserved
4	0-7	Reserved

3.4.2.2 Read Channel Interface Command. The Read Channel Interface command (modifier 6, opcode 6) allows you to read the status of the communication channel CRU interface. When the Read Channel Interface command is issued, byte 0 of the command block must contain the modifier and opcode. The other four bytes of the command block are not used. The status of the interface is returned in byte 1 and 2 of the command completion status report as shown in Figure 3-11. Bytes 3 and 4 of the command completion status report are not used. Byte 5 contains the command completion code. Table 3-7 explains the meaning of the bits in bytes 1 and 2 of the completion report.

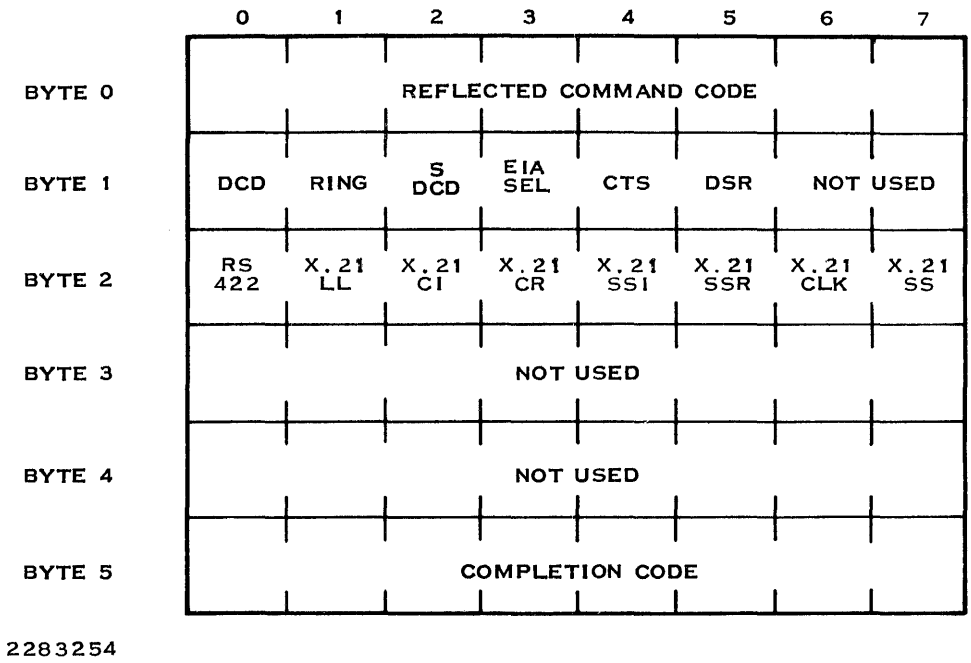


Figure 3-11. Command Completion Report for Read Channel Interface Command

Table 3-7. Bit Definitions, Read Channel Interface Command Status Byte

Byte	Bits	Meaning
1	0	Data Carrier Detect 0 = Data carrier detect off 1 = Data carrier detect on
1	1	Ring 0 = Ring off 1 = Ring on
1	2	Secondary Data Carrier Detect (SDCD) 0 = SDCD off 1 = SDCD on
1	3	EIA Select 0 = EIA cable not connected 1 = EIA cable connected
1	4	Clear to Send (CTS) 0 = CTS off 1 = CTS on
1	5	Data Set Ready (DSR) 0 = DSR off 1 = DSR on
1	6,7	Not Used
2	0	EIA RS422 Select 0 = RS422 selected 1 = RS422 not selected
2	1	X.21 Leased Line 0 = X.21 not on leased line 1 = X.21 attached to a leased line
2	2	X.21 Current Indication (I) 0 = I off 1 = I on
2	3	X.21 Current Receive (R) 0 = R off 1 = R on
2	4	X.21 Steady State Indication (I) 0 = I off 1 = I on
2	5	X.21 Steady State Receive (R) 0 = R off 1 = R on

Table 3-7. Bit Definitions, Read Channel Interface Command Status Byte (Continued)

Byte	Bits	Meaning
2	6	X.21 Clock Interrupt 0 = No interrupt 1 = Interrupt
2	7	X.21 Steady State Condition 0 = No new steady state condition 1 = New steady state condition
3	0–7	Reserved
4	0–7	Reserved

3.4.3 Immediate Commands

The opcode 7 Immediate commands described here allow you to modify the thresholds of the input and output FIFOs on the X.21 BCAIM and to modify the time-out value for the input FIFO. They also provide a means of reading the size of the FIFOs and of determining how many bytes of data are currently in each FIFO.

3.4.3.1 Set FIFO Thresholds. The Set FIFO Thresholds command (modifier 0, opcode 7) provides a way to modify the input and output FIFO thresholds. The threshold value for the input FIFO is the number of data bytes that it must contain before the X.21 BCAIM begins transferring data to the host. The output FIFO threshold is a byte count. The output FIFO entry count is decremented as each byte is transferred out of the FIFO onto the communication line. When the count is lowered to the threshold value, the X.21 BCAIM firmware sets the output FIFO ready signal to 1. The output FIFO ready signal remains 1, allowing the host to transfer transmit data to the FIFO until it is full. When the FIFO is full, the firmware sets the output FIFO ready signal to 0 where it remains until the byte count is decremented to the threshold value again.

The host can manage the input and output FIFO thresholds to optimize the amount of data transferred between the host and the X.21 BCAIM FIFOs. Each FIFO has a capacity of 64 bytes and the default FIFO threshold values allow the transfer of 75 percent of the FIFO capacity during high activity periods. The default input FIFO threshold value is 48. The default output FIFO threshold value is 16.

To issue the Set FIFO Thresholds command, the five-byte command block must contain the following:

Byte 0 — Command code and modifier.

Byte 1 — Must be zero.

Byte 2 — Must contain the output FIFO threshold value if the threshold is going to be modified. If this byte is written with zeros, the current threshold value is returned in byte 2 of the command completion status report.

Byte 3 Specifies an input FIFO time-out in quarter-second intervals. The time-out is only active when the X.21 BCAIM is operating in the character read mode. The purpose of the timer is to ensure that all data from the communication line gets transferred to the host when data reception stops. If no data is received for the time-out interval, the input FIFO threshold is set to 1 and any data in the FIFO is transferred to the host.

Byte 4 Specifies an input FIFO threshold value if the threshold is going to be modified. If this byte is written with zeros, the threshold remains unchanged and the current value of the threshold is returned in byte 4 of the command completion status report.

The six-byte command completion status report contains the following:

Byte 0 Echo of the command

Byte 1 Zero

Byte 2 Current value of the output FIFO threshold

Byte 3 Echo of the time-out value specified in byte 3 of the command block

Byte 4 Current value of the input FIFO threshold

Byte 5 Completion status

3.4.3.2 Read FIFO Counts. The Read FIFO Counts command (modifier 1, opcode 7) returns the size and byte count of data currently in the X.21 BCAIM input and output FIFOs. To issue this command, byte 0 of the command block must contain the opcode and modifier and bytes 1 through 4 must be zero. The command completion status report returns the following information:

Byte 0 Echo of command

Byte 1 Size of the output FIFO in bytes

Byte 2 Number of data bytes currently in the output FIFO

Byte 3 Size of the input FIFO in bytes

Byte 4 Number of data bytes currently in the input FIFO

Byte 5 Zero

3.4.4 Host Interface Requests

The Host Interface requests (opcode C) are commands that specify transfers of data between the host memory and X.21 BCAIM memory. The communication channel level firmware on the X.21 BCAIM does not process these requests and they are not communication channel oriented. The modifier code specifies the type of Host Interface request to be executed as follows:

Modifier Code	Type of Interface Request
0	X.21 BCAIM Memory Load
1	X.21 BCAIM Memory Dump
2	Read Reserved Memory Status
3	X.21 Call Data Memory Load
4	X.21 Call Data Memory Dump
5–7	Unused

3.4.4.1 Memory Load. The Memory Load command (modifier 0, opcode C) transfers software such as character detection routines from host memory to X.21 BCAIM RAM. The Reserve Memory command (modifier 5, opcode D) must be issued to reserve the required amount of X.21 BCAIM RAM before issuing the Memory Load command. The command completion status report associated with the Reserve Memory command returns the starting address where the download area begins.

When the Memory Load command is issued, byte 0 of the command block must contain the modifier and opcode. Bytes 1 and 2 must contain the starting address in X.21 BCAIM RAM where the data is to be transferred. Bytes 3 and 4 of the command block must contain the byte count of data to be transferred to X.21 BCAIM memory. As soon as the X.21 BCAIM accepts the byte count and load address, the data is transferred to contiguous memory locations starting at the location specified in bytes 1 and 2. Downloading can take place when the output FIFO is full since the downloaded code does not go in the FIFO.

3.4.4.2 Memory Dump. The Memory Dump command (modifier 1, opcode C) transfers data from X.21 BCAIM memory to host memory. Bytes 1 and 2 of the command block must contain the starting address in X.21 BCAIM memory of the data to be transferred. Bytes 3 and 4 must contain the byte count of data to be transferred. Data transfer to the host begins immediately after the six-byte completion status report has been transferred to the host and continues until the amount of data indicated in the byte count has been transferred or until an error occurs.

The Memory Dump command can be used at any time. Areas where the Memory Dump command can be used legally are: ROM >0 to >3FFF and RAM >9800 to >A7FF. Attempting to dump illegal areas will result in an error code of >26. An illustration showing the layout of X.21 BCAIM memory and defining the bounds of various areas of the memory can be found at the end of this section.

3.4.4.3 Read Reserved Memory Status. The Read Reserved Memory Status command (modifier 2, opcode C) reads the starting and ending addresses of X.21 BCAIM RAM that has been reserved via a Reserve Memory command (>5D). When the Read Reserved Memory Status command is issued, bytes 3 and 4 of the command block must contain a byte count of four.

The six-byte command completion status report for the Read Reserved Memory Status command is returned to the host followed by the requested number of bytes. The first two bytes contain the starting address of reserved memory; the last two bytes contain the address of the first byte beyond the reserved area. Zero values are returned if no X.21 BCAIM RAM was reserved.

3.4.4.4 X.21 Call Data Memory Load. The X.21 Call Data Memory Load command (modifier 3, opcode C) consists of three separate subcommands which allow the host to transfer selection signals to X.21 BCAIM RAM. The subopcode written in byte 1 of the command block determines the type of subcommand. A subopcode of >00 indicates address information is being transferred, >01 indicates facility request information, and >02 indicates facility registration and cancellation information. X.21 BCAIM memory is allocated dynamically for the selection signals when the host issues the command.

The allocated RAM buffer is deallocated after the data transfer state if the most significant bit of byte 2 of the command block is zero or whenever the X.21 BCAIM is reset. If the buffer is not deallocated, subsequent >3C commands cause the selection signal information currently in the buffer to be overwritten with new information. This command should be issued and completion status reported without error before an Open Initiate command is issued to begin the call.

The command block for the X.21 Call Data Memory Load command has the following format:

Byte	Description
0	Opcode and modifier (>3C)
1	Subopcode >00 = Address >01 = Facility request >02 = Facility registration and cancellation
2	D/F* (>00)
3,4	Byte count

Refer to the CCITT X.21 specification for detailed descriptions of the selection signals. It is your responsibility to ensure that data transferred to the X.21 BCAIM for subsequent transmission to the X.21 network is properly constructed. The X.21 BCAIM transmits pad characters from the CECPT after the last selection signal is transmitted to the X.21 network.

Bytes 0 through 4 of the command completion status report contain echoes of bytes 0 through 4 of the command block. Byte 5 contains the command completion code.

3.4.4.5 X.21 Call Data Memory Dump. The X.21 Call Data Memory Dump command (modifier 4, opcode C) consists of three separate subcommands, each of which transfers a different type of information from X.21 BCAIM RAM to the host. The subopcode in byte 1 of the command block determines which subcommand is issued. The command completion status report is returned prior to the requested data for each of the subcommands. It is your responsibility to ensure that the data received by the host is properly processed. The X.21 BCAIM does not include SYN or block terminating characters in the character count transferred. The actual count of characters transferred is returned in the command completion status report for each of the subcommands. The CECPT specifies the block size of buffers used in the >4C command. The following paragraphs describe the three subcommands.

* D/F is the most significant bit in byte 2 of the command block. When set, it informs the X.21 BCAIM not to deallocate the buffer after the data transfer state is entered or in the case of facility registration, until proper network response has occurred.

Call Progress Signal Dump, Subopcode >00. The Call Progress Signal Dump subcommand allows the host to transfer call progress signal information from X.21 BCAIM RAM to host memory. The X.21 BCAIM allocates an area from its buffer pool for storage of call progress information from the network during open processing and then transfers it to the host when this subcommand is issued. The buffer area can be released after the host requests call progress signal information or is released automatically when a new Open command is issued or the X.21 BCAIM is reset.

When the X.21 BCAIM receives a call progress signal from the network indicating that a call was not successful, the X.21 BCAIM returns a call progress signal error code in the command completion status report. The host can issue the >4C command to obtain the call progress signal(s) that caused the open to fail.

The format of the five-byte command block for the Call Progress Signal Dump command is as follows:

Byte	Description
0	Opcode and modifier (>4C)
1	Subopcode (>00)
2	D/F/Block number
3,4	0/Request byte count

NOTES

1. D/F is the most significant bit in byte 2 of the command block. When set, it informs the X.21 BCAIM not to deallocate the buffer.
2. The block number in byte 2 is the number of a particular block of information that is to be transferred to the host.
3. Always set the most significant bit of byte 3 to zero.
4. Bytes 3 and 4 contain the requested byte count.
5. Multiple blocks of call progress signal information are possible.

The format of the six-byte command completion status report for the Call Progress Signal Dump subcommand is as follows.

Byte	Description
0	Echo of opcode and modifier
1	Echo of subopcode
2	Echo of D/F and block number
3,4	F/C* and Actual count
5	Completion code

* F/C is the most significant bit of byte 3. When set, it indicates that this is the last block of call progress signal information received from the network.

DCE-Provided Information Dump, Subopcode >01. The DCE-Provided Information Dump subcommand allows the host to transfer DCE-provided information from X.21 BCAIM RAM to host memory. In cases where more than one block of DCE-provided information has been received, the host must check the F/C bit in the command completion status report to see if the block received is the last block received from the network. The CECPT specifies the number and size of buffers that the X.21 BCAIM allocates for DCE-provided information.

This command is issued after a successful Open command completion. The buffer area in X.21 BCAIM can be released after the host requests the DCE-provided information or is automatically released when a new Open command is issued or the X.21 BCAIM is reset. The format of the five-byte command block and the six-byte command completion status report is the same as for the Call Progress Signal Dump subcommand except the subopcode in byte 1 is >01 instead of >00.

Call Charge Information Dump, Subopcode >02. The Call Charge Information Dump subcommand allows the host to transfer call charge information from X.21 BCAIM RAM to host memory. This command is issued at completion of a call in which charging information is requested, after a Close command has successfully completed.

The buffer area in X.21 BCAIM RAM can be released after the host requests charging information or is automatically released when a new Open command is issued or the X.21 BCAIM is reset. The format of the command block and the command completion status report is the same as for the other two subcommands except that subopcode >02 is used in byte 1 of the command block. Only one charge call block is allowed.

3.4.5 Immediate Commands

The opcode D Immediate commands are commands that execute BLWP routines, load or dump one memory word, read ROM/RAM size, read the ID switches on the X.21 BCAIM, reserve X.21 BCAIM memory, or release reserved memory. Information is transferred to the X.21 BCAIM in the five bytes of the command block and returned to the host in the six bytes of the command completion status report. Each immediate request requires that the command block bytes contain specific information as indicated in the discussion on each particular command. The modifier code designates the type of Immediate command to be executed as follows:

Modifier Code	Type of Immediate Request
0	BLWP Vector
1	Memory Word Load
2	Memory Word Dump
3	Read ROM/RAM size
4	Read ID Switches
5	Reserve Memory
6	Release Reserved Memory
7	Reserved

3.4.5.1 BLWP Vector. The BLWP Vector command (modifier 0, opcode D) allows execution of a routine in X.21 BCAIM memory. A BLWP vector is two consecutive memory words containing the address of a workspace in X.21 BCAIM RAM and the address of the first instruction of a routine, respectively. Bytes 1 and 2 of the five-byte command block specify the address of the BLWP vector, with the most significant byte of the address in byte 1 of the command block.

The command completion status report is written to the host after the called routine returns via a RTWP instruction. The completion status report echos the five-byte command block and returns a completion code of >00.

3.4.5.2 Memory Word Load. The Memory Word Load command (modifier 1, opcode D) loads one word into a specific X.21 BCAIM memory location. Bytes 1 and 2 of the command block must contain the address of the memory location to be loaded. The most significant byte of the address must be in byte 1. Bytes 3 and 4 of the command block must contain the word that is to be stored in the location specified in bytes 1 and 2. Legal addresses are all of X.21 BCAIM RAM (>9800 to >A7FE). Use extreme caution with this command since it is possible to load a word in a location that may contain critical information.

3.4.5.3 Memory Word Dump. The Memory Word Dump command (modifier 2, opcode D) causes one word from X.21 BCAIM memory to be transferred to the host. Bytes 1 and 2 of the command block must contain the address in X.21 BCAIM memory of the word to be dumped. The word is returned to the host in bytes 3 and 4 of the command completion status report. Legal addresses that can be dumped are >0 to >3FFE in ROM and >9800 to >A7FE in RAM.

3.4.5.4 Read ROM/RAM Size. The Read ROM/RAM Size command (modifier 3, opcode D) allows you to check the amount of ROM and RAM installed on the X.21 BCAIM board. To issue the command, byte 0 of the five-byte command block must contain the command code >3D. The contents of the remaining four bytes are not important. The command completion status report returns an echo of the command code in byte 0, the ROM size in bytes 1 and 2, the RAM size in bytes 3 and 4, and a completion code of >00 in byte five. The ROM size in bytes 1 and 2 and the RAM size in bytes 3 and 4 are right-justified hexadecimal values indicating the number of bytes of ROM or RAM.

3.4.5.5 Read ID Switches. The Read ID Switches command (modifier 4, opcode D) causes the firmware on the X.21 BCAIM to read the eight-bit ID switch register. Byte 0 of the command block must contain the opcode and modifier; the other four bytes must be zero. The ID switch code is returned to the host in bytes 1 and 3 of the command completion status report.

3.4.5.6 Reserve Memory. The Reserve Memory command (modifier 5, opcode D) reserves an area in X.21 BCAIM RAM for downloading code. Only one area can be reserved at a time, so if an area has been reserved previously, it must be released via the Release Reserved Memory command (>6D) before the X.21 BCAIM will accept the Reserve Memory command. Byte 0 of the command block must contain the modifier and opcode. Bytes 1 and 2 must contain the size, in bytes, of the area being requested.

Bytes 1 and 2 of the command completion status report contain the length of the area (in bytes) that is reserved with the MSB in byte 1. The length is an echo of the byte count requested. Bytes 3 and 4 contain the starting address of the reserved area with the MSB in byte 3.

NOTE

Use the Reserve Memory command before opening the channel since the X.21 BCAIM firmware creates CRB buffers in the area that is available for reserving after the channel is opened. Once the firmware has allocated space for the CRB buffers needed to process a command, the memory area may be fragmented and it may not be possible to reserve enough contiguous locations for downloaded code.

3.4.5.7 Release Reserved Memory. The Release Reserved Memory command (modifier 6, opcode D) causes the X.21 BCAIM to release an area of RAM previously reserved via the Reserve Memory command. Bytes 1 and 2 of the command block must contain the starting address of the reserved area that is to be released. If the address is not the correct starting address of the reserved area, the command will be rejected.

While releasing reserved memory, it is your responsibility to ensure that all pointers or tables modified by downloaded code are restored to their original value; otherwise, unpredictable operation of the X.21 BCAIM may result.

3.4.6 Normal Mode Diagnostic Commands

The Normal Mode Diagnostic commands (opcode F) can be executed to test the host-to-slave interface and the memory bus on the X.21 BCAIM. These commands can be executed while communication programs are running.

The modifiers verify a specific input pattern, return a known pattern, or echo any input pattern desired. There is no automatic error checking involved with the opcode F commands when you use modifiers 1 or 2, but you can code the DSR for the X.21 BCAIM to check the returned patterns to determine if errors occur during execution of these tests. The modifiers used with opcode F commands are as follows:

Modifier	Meaning
0	Verifies input pattern (>AA, >55, >FF, >00)
1	Returns known pattern (>AA, >55, >FF, >00)
2	Echoes input pattern (>XX, >XX, >XX, >XX)
3-7	Unused

When using modifier 0, byte 0 of the five-byte command block must contain >0F with the input pattern in the next four bytes: byte 1 = >AA, byte 2 = >55, byte 3 = >FF, and byte 4 = >00. The input pattern is read and returned to the host in the command completion status report. The first five bytes of the completion status report echo the command and the input pattern. If errors occur during this test, byte 5 of the command completion status report returns error code >32 (host CRU interface test failure); otherwise, byte 5 is zero.

When using modifier 1, byte 0 of the five-byte command block is set to >1F and the other four bytes of the command block can be set to any value. The command completion status report returns the >1F command in byte 0 with the next four bytes set to >AA, >55, >FF, and >00 if no errors occur. A command completion code of >00 is returned in byte 5.

When using modifier 2, byte 0 of the command sequence must contain >2F with the desired input pattern in the next four bytes of the command sequence. The first five bytes of the command completion status report echo the five bytes of the command sequence. Byte 5 of the completion report is always zero since there is no error checking beyond recognizing the command code.

3.5 SELF-TEST PROGRAMS

The programs described in the following paragraphs are coded into ROM on the BCAIM and execute automatically each time the BCAIM is powered up or reset. If a program encounters an error while executing, the self-test/fail LED remains illuminated and the command completion status report indicates the component that failed during the test. Refer to the BCAIM maintenance manual for more information.

3.5.1 TMS 9900 Processor Test

The TMS 9900 Processor Test exercises all of the TMS 9900 instructions that are practical to test. If an error occurs and the processor maintains control, it reports an error code. If the processor does not maintain control, the only error indication is that the self-test/fail LED does not extinguish. Upon detection of a processor failure, it returns the following command completion report.

Byte 0	= FF	Self-test failed
Bytes 1,2	= XX	Not used
Bytes 3,4	= XX	Not used
Byte 5	= 71	Processor test error

3.5.2 ROM Cyclic Redundancy Check

The ROM Cyclic Redundancy Check uses a ROM-resident subroutine to calculate the CRC code. The calculated code is compared to a CRC code stored in the last two bytes of each ROM chip on the X.21 BCAIM and if it is different, the command completion status report contains the following information:

Byte 0	= FF	Self-test failed
Byte 1,2	= XX	Not used
Byte 3,4	= 0	MSB of ROM (see note)
	= 1	LSB of ROM (see note)
Byte 5	= 72	ROM CRC error

NOTE

There are two ROM chips on the X.21 BCAIM; one chip stores bits 0 through 7 of a 16-bit word, the other stores bits 8 through 15. If bytes 3 and 4 equal 0, the ROM chip that stores bits 0 through 7 is the failing chip. If bytes 3 and 4 equal 1, the chip that stores bits 8 through 15 is the failing chip.

3.5.3 RAM Data Storage Test

The RAM Data Storage Test checks the operation of the 4K bytes of static RAM on the X.21 BCAIM board. Each word location is loaded with its own address and after all locations have been loaded, the contents of each location is read and compared with its address. If the test detects no errors, each word location is written with the one's complement of its address. After all locations have been written, it reads each location and compares the contents with the complement of the address. The command completion status report reports errors as follows:

Byte 0	= FF	Self-test error
Byte 1,2	=	Bits that were incorrect
Byte 3,4	=	Address of failing memory location
Byte 5	= 73	RAM data test error

3.5.4 TMS 9901 Clock Test

The TMS 9901 Clock Test checks the clock section of the TMS 9901 by counting processor loops. It compares the loop count to the upper and lower limits of a count expected in a 10-millisecond interval. If the actual count is out of range, it reports the error in the command completion status report as follows:

Byte 0	= FF	Self-test failure
Byte 1,2	=	Expected loop count
Byte 3,4	=	Actual loop count
Byte 5	= 76	TMS 9901 clock test error

3.5.5 TMS 9903 Synchronous Communication Controller Test

The TMS 9903 Synchronous Communication Controller Test is a four-part test that checks different functional sections of the TMS 9903. Three of the tests are data transfer tests where data is looped back internally in the TMS 9903. The three modes are asynchronous, synchronous BSC, and synchronous SDLC. It compares the looped back data with the transmitted data for accuracy and if it detects errors, the command completion status report indicates the type of failure that occurred. The fourth test checks the CRC generator section of the TMS 9903 by comparing the CRC generated by the TMS 9903 to a software-generated CRC. The command completion status report reports any errors encountered as follows:

Byte 0	= FF	Self-test failure
Byte 1,2	= XX	Not used
Byte 3,4	= 01	Asynchronous test failed
	= 02	BSC test failed
	= 04	SDLC test failed
	= 08	CRC test failure
Byte 5	= 75	TMS 9903 test error

3.6 CHARACTER MODE OPERATION

The X.21 BCAIM supports asynchronous protocols with a special character mode operation. The character mode is implemented by issuing character mode Write and character mode Read commands. For most applications, it is not practical to operate in the character write mode without also implementing the character read mode. The following discussion describes how to implement character mode operation and points out differences between the character mode and normal operation of the X.21 BCAIM.

3.6.1 Character Write Mode

Issuing a character mode Write command places the X.21 BCAIM in the character write mode. The byte count field of the character mode Write command (bytes 3 and 4 of the command block) must contain >8000. The other three bytes of the five-byte command block contain the same information as in normal Write commands.

In the character write mode, each data byte written to the controller is transmitted on the communication line without waiting for a minimum number of bytes to be placed in the output FIFO. If the host has a block of data to transmit, the output FIFO buffers it in the normal manner. When the output FIFO fills, the output FIFO ready signal goes to zero and the host must stop transferring transmit data until the FIFO empties down to the output FIFO threshold value. When it reaches this threshold, the X.21 BCAIM firmware sets the output FIFO ready signal back to one and the host can continue transferring data.

Since there is no byte count specified with this type command, the X.21 BCAIM remains in the character write mode and transmits data bytes without needing additional Write commands. When a transmit error occurs or an Abort command is issued, the character write mode is terminated and a six-byte command completion report is returned.

Time-outs can be used in the character write mode of operation in the same manner as in normal operation if the host software requires them. In the character mode, the transmit intercharacter timer is active only when there is data in the output FIFO. When a time-out occurs, a six-byte command completion status report is returned, terminating the character write mode. A new Write command is required to resume transmit operation.

3.6.2 Character Read Mode

The X.21 BCAIM is placed in the character read mode of operation when the host issues a character mode Read command. The byte count field of the character mode Read command (bytes 3 and 4 of the five-byte command block) must contain >8000. The other three bytes of the command block contain the same information as in a normal Read command.

In the character read mode, each data byte is transferred to the host as it is received from the communication line, generating an interrupt per data byte. You can modify the input FIFO threshold value to allow several data bytes to accumulate in the input FIFO before the host is interrupted. This can be done to accept block transfers from a terminal where character echoing is not required. In this case, the host is interrupted only when the input FIFO fills to the value set by a Set FIFO Thresholds command. When interrupted, the host empties the input FIFO and then waits to be interrupted when the FIFO fills again.

When operating with the input FIFO threshold greater than 1, set the input FIFO time-out to time out if data reception stops. When the time-out occurs, the input FIFO threshold is set to 1 and the X.21 BCAIM sets the input data valid signal to 1, allowing the host to empty the input FIFO of the last data bytes received.

The character read mode is terminated with an Abort command or when an error is reported to the host.

3.6.3 Character Mode Error Reporting

The X.21 BCAIM firmware reports line disconnection errors via the six-byte command completion status report. Receive errors are detected by the character detection routine if one is used. When there is no character detection routine, the firmware reports receive errors via a one-byte completion status report. In this case, the receive restart flag and the status flag (bits 9 and 8, respectively, of the CRU interface input word) are both set to one to indicate a single-byte status report to the host. The data byte of the CRU interface input word contains the status report. The status reported in the data byte of the CRU interface input word consists of input bits 8 through 14 of the TMS 9903 CRU interface. The meaning of these bits (when set to one) varies with the mode of operation of the TMS 9903. They are defined here for the asynchronous mode of operation of the TMS 9903. For other modes, refer to the *9900 Family Systems Design and Data Book, Microprocessor Series, First Edition*, part number 97049-118-NI.

CRU Interface Data Byte	TMS 9903 Bit	Meaning for TMS 9903 Modes 5 and 6
Bit 0 (MSB)	n/a	Undefined
1	14	Receive start bit detect (used in testing)
2	13	Receive full bit detect (used in testing)
3	12	Receive framing error
4	11	Receiver overrun
5	10	Receive parity error
6	9	Receive error (error summary)
Bit 7 (LSB)	8	Ninth bit of receive data (should be zero unless nine-bit characters are used)

The character read mode remains active after the receive reprocess error report. The X.21 BCAIM firmware attempts to continue normal receive operation if the host does not abort the character read mode.

If there is no character detection routine, the most significant byte of channel parameter table word CPCDFL serves as a mask for error detection. An error is reported only when an error bit is set in bits 8 through 14 of the CRU interface input word and the corresponding bit of CPCDFL is also set to one. For example, in modes 5 and 6 (asynchronous), a value of >1800 for CPCDFL causes receiver overruns and framing errors to be reported. A value of >0400 for CPCDFL causes only parity errors to be reported.

3.6.4 Character Detection Routine Considerations

The character detection routine interface to the TMS 9903 ISR firmware in character mode is identical to other modes of operation with the following exceptions:

1. The TMS 9903 ISR does not maintain a request byte count after normal return from the character detection routine.

2. Downloaded character detection routines can support pacing of output to terminals that return wait commands to the host when terminal buffers are full. The receive character detection routine halts data transmission when it receives a wait command from the terminal. The procedure for suspending data transmission consists of the following steps:

   a. Turn off the TMS 9903 transmitter via an SBZ XMTON instruction.

   b. Suspend the transmit request time-out mechanism by clearing word CBTIMO of the transmit control block.

   c. Store a NOP instruction (>1000) in word CMXONI of the TMS 9903 IST. This prevents transmit data being stored in the output FIFO from turning on the transmitter.

3. Data transmission is resumed when the resume command is received from the terminal. The following steps are required to resume data transmission:

   a. Turn on the TMS 9903 transmitter via an SBO XMTON instruction.

   b. Activate transmit time-out by moving the contents of transmit control block word CBTIMR to transmit control block word CBTIMO.

   c. Restore an SBO XMTON instruction (>1D10) in word CMXONI of the TMS 9903 IST to enable normal transmit operation. The address of CMXONI is located in the ROM address table (Table 3-13). Refer to the discussion of character detection routines for additional information.

3.7 X.21 BCAIM COMMAND COMPLETION CODES

Command completion codes are returned in byte 5 (the last of six bytes) of the command completion status report as the result of normal completion of commands or as the result of unsolicited fatal errors requiring X.21 BCAIM reset initialization.

When the X.21 BCAIM has completed processing a command, it returns a command completion status report to the host. If the command is a communication channel Read command, the X.21 BCAIM returns the status report after any data involved in the command has been transferred to the host. For Read Parameters (>74), Read Reserved Memory Status (>2C), and Memory Dump (>1C) commands, the status report is transferred to the host prior to the data. In either case, the last byte of the command completion status report (byte 5) contains a completion code. The host reads the completion code to determine the status of the completion.

The completion code indicates an error only if the most significant bit of byte 0 of the command completion status report is set to 1. For nonfatal errors, the remaining seven bits of byte 0 echo the command code (modifier and opcode) issued by the host. When a fatal error occurs, byte 0 of the command completion status report is set to >FF.

The following paragraphs discuss nonfatal completion codes and fatal error codes. Some of the completion codes are protocol-dependent and are discussed in more detail in the appendix containing information on the particular protocol.

3.7.1 Nonfatal Error Codes

Table 3-8 describes nonfatal error codes. The hexadecimal command completion codes that appear in byte 5 of the command completion status report fall into the following categories:

Completion Code (Hexadecimal)	Type of Completion
01-2F	DX10 compatible errors
30-3F	Host/X.21 BCAIM interface errors
40-4F	ISR errors
50-5F	Reserved for host line control errors
60-7F	Buffer management and fatal errors
80-FF	Special character termination codes

Table 3-8. Nonfatal Error Codes

Error Code (Hexadecimal Value of Byte 5)	Meaning
02	Illegal Opcode. Issuing a command that is not supported by X.21 BCAIM firmware causes an illegal opcode error.
03	Channel Not Enabled. This error results from I/O requests being issued when the communications channel is not open. The TMS 9903 ISR level returns this error.
06	I/O Abort Error. The current request was terminated by an abort command to the X.21 BCAIM.
13	Time-Out Error. The time-out specified for the current command expired before the command completed.
18	Line Disconnect. If the modem on the X.21 BCAIM communication channel loses signals based on channel parameter table word CPISRF, all I/O requests are terminated with this error.

Table 3-8. Nonfatal Error Codes (Continued)

Error Code (Hexadecimal Value of Byte 5)	Meaning
19	Unable to Accept Command. The ISR level of X.21 BCAIM firmware limits the number of certain types of commands as follows: 1. Only one Time-Out command can be issued to the ISR at one time. 2. Only one Open or Close command can be issued to the ISR at one time. A violation of these limits results in the unable to accept command error.
25	No CRB Buffer Available. This error indicates that there is no X.21 BCAIM memory available to build a buffer for this request and that the CRB buffer pool has no available buffers.
26	Illegal X.21 BCAIM Address. This error is reported when an attempt is made to read or write an illegal memory address. Commands >0C, >1C, >1D, and >2D can return this error.
2D	Reserve Memory Error. This error is returned when an attempt is made to reserve more than one block of RAM.
30	Output FIFO Empty. This error indicates that the X.21 BCAIM output FIFO became empty during data transmission. Transmit data for the associated command was not transferred to the X.21 BCAIM fast enough to keep up with the communication channel.
31	Input FIFO Full. This error indicates that the input FIFO was full when the X.21 BCAIM attempted to store a byte of data received over the communication channel. It occurs when the input FIFO is not emptied as fast as data is received from the communication channel.
32	Host CRU Interface Error. This error indicates that the expected values were not received from the host when the CRU interface test (>0F) was issued.
33	Illegal Byte Count. This error indicates that an illegal byte count was specified in bytes 3 and 4 of a Memory Load command. A byte count of zero or a count that is too large for the download area causes this error.
34	Zero Byte Count. This error indicates that a zero byte count was specified with a communication channel Read or Write command.
40	Call Progress Signal Error. This error indicates that the X.21 switched line network returned a call progress signal that required the X.21 BCAIM to abort the call. The host should issue a Call Progress Signal Dump command (>4C), subopcode >00 to obtain the call progress signal that caused the call to be aborted.

Table 3-8. Nonfatal Error Codes (Continued)

Error Code (Hexadecimal Value of Byte 5)	Meaning
41	Host Buffer Overflow. This error occurs when the TMS 9903 ISR detects host buffer overflow. It indicates that the receive byte count is exhausted and the end of the data frame has not been detected. Normally, this condition is detected by a character detection routine and reported in another manner. This error code is provided for the cases where no character detection routine is present, or where host buffer overrun is not detected by the character detection routine.
43	Write Parameters ISR Error. This error occurs when any of the following conditions exist: • Other channel-oriented commands are pending. Refer to the Open and Write Parameters command descriptions for special conditions where this is allowed. • The protocol selected by the Write Parameters or Open command is undefined. • The offset into the channel parameter table is too large or the offset plus the byte count is too large (extends beyond the channel parameter table). • A zero byte count was specified with a protocol selection value of zero. A zero byte count is only allowed with a protocol selection value other than zero.
44	Undefined Protocol. This error occurs when the protocol specified in an Open command is not defined for the X.21 BCAIM.
45	Channel Already Open. The channel already is open from a previous Open command.
46	Abort Transmitted (BOP Mode). This error indicates that the 9903 was forced to transmit an abort pattern to the communication line because characters could not be loaded into the 9903 as fast as the 9903 transmitted them.
47	Receiver Reprocess Timer Expired. This error indicates that the time limit to receive a data frame from the communications line was exceeded. The time-out value specified in byte 1 of the five-byte Read command block has expired. Refer to the receive reprocess discussion earlier in this section. Special implementation of this timer is discussed there.
48	Requested X.21 Information Not Available. This error indicates that the host tried to obtain an Call Progress Signal Memory Dump (>4C) when no information was present in the X.21 BCAIM buffer(s).

Table 3-8. Nonfatal Error Codes (Continued)

Error Code (Hexadecimal Value of Byte 5)	Meaning
49	Requested X.21 Information Buffer Overflow. This error indicates that the switched line network provided more information to the X.21 BCAIM than the allocated buffer(s) could accommodate.
4D	Character Parity Error. This error indicates that the TMS 9903 detected a parity error while shifting the character to its receive buffer register.
4E	Framing Error, Asynchronous Mode. This error indicates the TMS 9903 detected that a received character had a stop bit that was not a logic one.
4F	Receiver Overrun Error. This error indicates that a data byte was received before the previous byte was processed. The byte was received when the receive buffer register loaded signal was high (logic one).
62	Memory Allocation Error. This error indicates that the BCAIM cannot allocate a buffer of the size requested by the host.
68	Memory Deallocation Error. This error indicates that the host has attempted to release a block of RAM with the wrong buffer address.
A8	Reserved.
A9	This error indicates that the X.21 BCAIM detected the wrong state (signalled by the X.21 network) to accept an Open command.
AE	This error indicates that the communication line is occupied or the X.21 BCAIM is busy.

NOTE

Error codes >60 through >7F are used for both fatal errors and normal mode errors. The two types of errors can be distinguished by the contents of byte 0 of the command completion status report where fatal errors always have >FF in byte 0. Normal mode errors set the most significant bit to one, but the remaining seven bits are an echo of the command.

3.7.2 Fatal Errors

During normal operation, several types of fatal errors can occur. The X.21 BCAIM reports the error in the command completion status report and will not accept any more commands until it is master cleared. On all fatal errors, the reset in progress bit (input word, bit 11) is set and byte 0 of the command completion status report contains the fatal error indication >FF. Bytes 1 through 4 of the command completion status report contain additional information about the error. The discussion of each fatal error explains the use of bytes 1 through 4. Byte 5 of the command completion status report contains the error code for the particular fatal error that occurred.

Table 3-9 lists the fatal errors and the hexadecimal codes that appear in byte 5 of the command completion status report when the fatal error occurs. The paragraphs following the table provide additional details on fatal errors, including information that is returned in bytes 1 through 4 of the command completion status report.

Table 3-9. Fatal Error Codes

Completion Code (Byte 5) (Hexadecimal)	Type of Error
61	X.21 BCAIM power failure
63	Illegal level 3 interrupt
65	Illegal level 5 interrupt
66	Illegal level 6 interrupt
67	Illegal level 7 interrupt
68	Illegal level 8 interrupt
69	Illegal level 9 interrupt
6A	Illegal level A interrupt
6B	Illegal level B interrupt
6C	Illegal level C interrupt
6D	Illegal level D interrupt
6E	Illegal level E interrupt
6F	Illegal level F interrupt
70	Illegal XOP encountered
71	X.21 BCAIM TMS 9900 self-test error
72	X.21 BCAIM ROM CRC error during ROM test
73	X.21 BCAIM RAM data test error
75	X.21 BCAIM TMS 9903 test failure
76	X.21 BCAIM TMS 9901 clock test failure
77	Output FIFO overflow
7D	Buffer pool initialization error

3.7.2.1 X.21 BCAIM Power Failure. This error indicates the detection of a power failure in progress. When a power failure is detected, the X.21 BCAIM drops all external modem leads and reports the failure in the command completion status report. Upon completion of the power failure error report, the X.21 BCAIM hangs in a loop awaiting a master reset. The bytes of the command completion status report contain the following information:

Byte 0	>FF (fatal error)
Byte 1,2	Workspace pointer when error occurred
Byte 3,4	Program counter when error occurred
Byte 5	Fatal error code >61

3.7.2.2 Illegal Slave Interrupt. The X.21 BCAIM reports unexpected or unsupported slave interrupts (codes >63 through >6F) as fatal errors with byte 5 of the command completion status report set to the interrupt level error code. When this error is reported, it indicates either hardware or firmware failure. The bytes of the command completion status report contain the following information:

Byte 0	>FF (fatal error)
Byte 1,2	Workspace pointer when error occurred
Byte 3,4	Program counter when error occurred
Byte 5	Fatal error code >63, >65 through >6F

3.7.2.3 Illegal Slave XOP. All unused ROM memory is initialized with XOP instructions. If an XOP instruction is encountered, it indicates X.21 BCAIM hardware or firmware errors or downloaded code errors. The bytes of the command completion status report contain the following information:

Byte 0	>FF (fatal error)
Byte 1,2	Workspace pointer when error occurred
Byte 3,4	Program counter when error occurred
Byte 5	Fatal error code >70

3.7.2.4 Buffer Pool Initialization Error. When X.21 BCAIM is initialized, all available RAM is initialized for use as a buffer pool. This error indicates a problem was detected during initialization and usually indicates broken hardware or a firmware problem. The bytes of the command completion status report contain the following information:

Byte 0	>FF (fatal error)
Bytes 1,2	Zero
Bytes 3,4	Zero
Byte 5	Fatal error code >7D

3.7.2.5 Fatal Self-Test Errors. Error codes >71 through >76 indicate fatal errors encountered during execution of the on-board diagnostic routines. Refer to paragraph 3.5 for an explanation of the information returned in the command completion status report when fatal errors resulting from diagnostic test failures occur.

3.8 DEVICE SERVICE ROUTINE (DSR) ISSUES

You must write a DSR to run under the host computer operating system and to provide the software interface between the operating system and the X.21 BCAIM firmware. The DSR must perform several specific tasks in addition to handling the general requests and commands directed to the X.21 BCAIM. For purposes of this discussion, DX10 is used as a specific operating system; however, most of the information applies to any 990 computer operating system.

The specific tasks that must be performed are:

- You must provide a DSR power-up routine to handle initialization of the X.21 BCAIM board.
- The CRU interface data transfer test (command >0F) must execute successfully before the X.21 BCAIM will accept any other commands.
- The DSR must provide mapping to allow the X.21 BCAIM to use DX10 (or other operating system) commands.

The following paragraphs explain specific tasks and provide coding examples that can be used as guides in writing the code to perform these tasks. A table showing how DX10 opcodes are mapped to X.21 BCAIM commands is presented for users who have the DX10 operating system.

Most of the coding examples presented here are self-contained; however, some routines are explained in function only. CRU definitions required for the coding examples are as follows:

CRU Input Definitions

```
STATUS    EQU  8     Status/data flag
RCVREP    EQU  9     Receive reprocess flag
IDV       EQU  10    Input data valid flag
RIP       EQU  11    Reset in progress flag
OFR       EQU  12    Output FIFO ready flag
OR        EQU  13    Output ready flag
PF        EQU  14    Poll flag
IS        EQU  15    Interrupt summary flag
```

CRU Output Definitions

```
CMD       EQU  8     Command/data flag
IDVE      EQU  10    IDV interrupt flag
IMR       EQU  11    Initiate master reset flag
OFRE      EQU  12    OFR interrupt enable
ORE       EQU  13    OR interrupt enable
HIE       EQU  15    Host interrupt enable
```

3.8.1 DSR Power-Up Routine

The power-up routine must reset the X.21 BCAIM by setting the initiate master reset bit (bit 11 of the CRU interface output word) to one. There are two possible ways that the X.21 BCAIM may fail to reset: When the self-test routine detects and reports an error, and when the reset in progress flag (bit 11 of the CRU interface input word) remains on with no error reported. The power-up code routine must detect both of these failures and take the appropriate action. The input data valid bit (bit 10 of the CRU interface input word) can be monitored to detect fatal errors reported by the self-test routine. The other reset failure can be detected by timing the reset of the board. If the reset in progress bit does not turn off (go back to logic zero) after five seconds, the board is inoperative.

You can time-out the reset in progress bit by executing a series of instructions until the desired event occurs or until the time interval allowed expires. An example of power-up coding follows with the subroutine CKTOUT performing the time-out function based on the time-out value in R6.

A CRU interface test command (>0F) must be issued to the X.21 BCAIM as the first command after successful completion of master reset. The X.21 BCAIM is ready for normal operation after it has been successfully reset and the >0F command has been executed. Refer to the command descriptions for details of the >0F command.

DSR Power Up Coding Example

```
        LI      R6,MRTIME       Time-out count for CKTOUT
        SBO     IMR             Initiate master reset
TRESET  TB      RIP             Reset complete?
        JNE     CKCRU           Yes, issue >0F command
        BL      @CKTOUT         No, check time-out
        JEQ     TERROR          Time-out expired, report error
        TB      IDV             X.21 BCAIM input pending?
        JNE     TRESET          No, wait for reset complete

*       Insert code here to read the six-byte status report
*       if an error occurs in the power up sequence.

CKCRU   EQU     $

*       Insert code here to issue the CRU interface data
*       transfer test and check the results of the test.
```

3.8.1.1 User-Supplied Status Checking Code. If an error occurs in the power-up routine with the input data valid bit set, user-supplied code should attempt to read the six-byte status report. The code required to read the six-byte status report can be similar to the example shown later for reading normal command completion status reports.

Note that the X.21 BCAIM can malfunction in a way that will prevent proper execution of the code intended to read the status report. Possible problems include status that is not meaningful, and not receiving the entire six-byte report. The code provided to check the status report must allow for the possibility of these problems and take appropriate action.

3.8.1.2 CRU Interface Data Transfer Test. After the power-up routine successfully completes, the CRU interface data transfer test (>0F) must be executed before the X.21 BCAIM will accept any other commands. After successful execution of the data transfer test, the X.21 BCAIM is ready for normal operation.

To issue the >0F command, byte 0 of the five-byte command must contain >0F, with the input pattern in the next four bytes: byte 1 =>AA, byte 2 = >55, byte 3 = >FF, and byte 4 = >00. The X.21 BCAIM reads the five bytes and compares the pattern in bytes 1 through 4 with the expected data. If the data received is not as expected, the X.21 BCAIM reports an error.

The X.21 BCAIM echoes the bytes received in the command block back to the host in the six-byte completion status report: byte 0 echos the command code, bytes 1 through 4 echo the input pattern. Byte 5 of the command completion status report contains >32 if the X.21 BCAIM detects an error in the pattern it receives; otherwise, byte 5 is zero. The code provided here should check the pattern returned in bytes 1 through 4 of the completion status report to verify that they are the same as the pattern sent to the X.21 BCAIM and should check for the presence of an error.

3.8.2 Typical X.21 BCAIM Command Sequence

The following discussion explains how to issue a typical command to the X.21 BCAIM and provides example code that you can use to issue the command.

A command is issued to the X.21 BCAIM by writing five bytes of command information to the CRU interface of the board. The command flag, bit 8 of the CRU output word, must be set to one when the first byte of the five-byte command block is written to the board but it need not be one after the first command byte is read by the X.21 BCAIM. The five-byte command block must be written as five consecutive bytes with no data bytes allowed between the first and fifth bytes.

The X.21 BCAIM indicates that it is ready to receive a command byte by setting the output ready flag (bit 13 of CRU interface input word) to one. The X.21 BCAIM hardware resets output ready to zero when the host writes a byte of information to the CRU interface output word, bits 0 through 8. The X.21 BCAIM sets output ready back to one after it reads the byte.

Commands can be issued to the X.21 BCAIM from interrupt-driven code or polling-type code. The following example assumes that the command is received from an external module via a BLWP entry. If a predetermined time-out interval expires without the X.21 BCAIM accepting a byte of information, the host sets the output ready interrupt enable bit (bit 13 of the CRU interface output word) to one. This causes the host to be interrupted when the X.21 BCAIM sets output ready to one. In this case, it is assumed that the interrupt service routine is responsible for writing the remaining command bytes to the board. The example code stores the remaining byte count in word CMDCNT and the address of the next command byte to be written to the board in word CMDADD.

Issue X.21 BCAIM Command Example

```
*
*          R8  = address of control block
*                word 0-4 = command bytes to be issued
*          R12 = X.21 BCAIM CRU base address
*
REQENT     LI    R7,5          Load command byte count
           LI    R6,CMDTO      Fetch command time-out
CMDLP      TB    OR            X.21 BCAIM ready for CMD byte?
           JEQ   WRTBYT        Yes, issue one byte
           BL    @CKTOUT       No, check time-out
           JEQ   ALTEXT        Time-out expired, exit
           JMP   CMDLP         Not expired, wait
*
WRTBYT     LDCR  *R8+,8        Write next CMD byte
           LI    R6,CMDTO      Initialize time-out
           DEC   R7            Finished command?
           JNE   CMDLP         No, continue
           RTWP                Yes, exit
*
ALTEXT     MOV   R7,@CMDCNT    Save remaining byte count
           MOV   R8,@CMDADD    Save command address
           SBO   ORE           Interrupt code will finish
           RTWP                Exit to calling routine
```

3.8.3 X.21 BCAIM Transmit Data Example

Data to be transmitted on the communications line is stored in the X.21 BCAIM output FIFO until it can be written to the communications line. Transmit data is associated with X.21 BCAIM command codes 3 and 5. Both the output ready and output FIFO ready CRU input signals must be set to one for the X.21 BCAIM to accept transmit data.

The coding example that follows illustrates one method of writing transmit data to the X.21 BCAIM. The entry to this code is assumed to be from an interrupt or a BLWP. The exit at label ENOFR forces an X.21 BCAIM interrupt to the host when both the OR and OFR input signals are one.

Write Transmit Data Example

```
*
*           Registers maintained until transmit data is
*           resident on the X.21 BCAIM are:
*
*           R1 = Transmit buffer address
*           R2 = Transmit byte count
*
XDATA       LI      R6,ORTOUT       Initialize output ready time-out
            TB      OR              Is X.21 BCAIM ready for a byte?
            JNE     CHKOR           No, wait until ready
CHKOFR      TB      OFR             Yes, output FIFO available?
            JNE     ENOFR           No, wait until available
            LDCR    *R1+,8          Yes, write a byte to X.21 BCAIM
            DEC     R2              Update byte count
            JEQ     ENDDAT          Finished when byte count = 0
            JMP     XDATA           Initialize deadman timer
*
*           Wait for the output ready signal for the
*           time interval in ORTOUT
*
CHKOR       TB      OR              Is X.21 BCAIM ready for a byte?
            JEQ     CHKOFR          Yes, check output FIFO
            BL      @CKTOUT         No, check for time-out
            JEQ     ENOFR           Time-out expired, enable interrupt
            JMP     CHKOR           Check OR again
*
*           Force the X.21 BCAIM to interrupt the host
*           when both OR and OFR signals are one
*
ENOFR       SBO     OFRE            Enable OFR interrupt
ENDDAT      RTWP
```

3.8.4 Reading X.21 BCAIM Status

The following code example illustrates one way to process a six-byte command completion status report from the X.21 BCAIM. Decoding is required to detect the initial byte of the six-byte sequence. In the example routine, data from the X.21 BCAIM is processed at program label RDATA and one-byte receive reprocess completion status reports are processed at program label REPRO. No code for the latter subroutine is provided here.

NOTE

This code does not process X.21 BCAIM data for the Memory Dump commands (>1C, >4C,>2D), the Read Reserved Memory Status command (>2C), and the Read Parameters command (>74). The six-byte command completion status report is transferred to the host before the read data for these commands. The byte returned in the command completion status report must be used to detect the end of data transfer from the X.21 BCAIM for these two commands.

It is important to note that the status bit (bit 8 of the CRU interface input word) can be set only for the first byte of the six-byte status report. The processing context must be saved if there is an exit from reading the status report before all six bytes have been read. The example changes the interrupt entry vector (INTVCT) from the general input code (INPUT) to the status code (INST) in this case. The input data valid interrupt remains enabled at all times. The contents of memory word INTVCT provide an entry vector (INPUT or INST in the example) for input data valid interrupts.

Receive Status Code Example

```
*
*           Processing for X.21 BCAIM input
*
INV         DATA  INPUT          General input interrupt vector
STV         DATA  INST           Six-byte status interrupt vector

INPUT       TB    IDV            Input byte pending from X.21 BCAIM?
            JNE   EXITS          No, exit
            TB    STATUS         Yes, is it a status byte?
            JNE   RDATA          No, receive data
            TB    RCVREP         Yes, is it a receive reprocess?
            JEQ   REPRO          Yes, process it
*
*           This will be a six-byte status report
*
            LI    R6,INTOUT      IDV time-out value
            LI    R5,STBUFF      Address of status buffer
            LI    R4,6           Initialize status byte count
INST        TB    IDV            Data byte available from X.21 BCAIM?
            JEQ   INST10         Yes, read it
            BL    @CKTOUT        No, check for time-out
            JNE   INST           Did not time-out, try again
            MOV   @STV,@INTVCT   Set status interrupt vector
            RTWP                 Time-out, exit with interrupt enabled
*
INST10      STCR  *R5+,8         Store one status byte
            SBO   IDVE           Acknowledge the byte
            DEC   R4             Have all six status bytes?
            JNE   INST           No, wait for next one
            MOV   @INV,@INTVCT   Restore vector for general input
*
*           Now pass status information to processing routine
*
*           The following code stores received data bytes into
*           the receive buffer for the current Read command.
*           This process continues until the completion status
*           for the Read command is received from the X.21 BCAIM.
*           Register conventions for the received data processing
*           are:
*
*           R7 = Receive buffer address
*           R8 = Receive byte count

RDATA       STCR  *R7+,8         Store data byte in buffer
            SBO   IDVE           Acknowledge this data byte
            INC   R8             Update receive byte count
            JMP   INPUT          Check for more input
```

3.8.5 DX10 Opcode Mapping

The DSR is responsible for mapping operating system opcodes to commands to which the X.21 BCAIM is capable of responding. Table 3-10 shows how to map DX10 operating system opcodes to X.21 BCAIM command codes.

Table 3-10. DX10 Opcode Mapping

X.21 BCAIM Command Code (Hexadecimal)	DX10 Opcode	DX10 Operation
11	0	Open
02	1	Close
12	2	Close EOF
21	3	Open rewind
22	4	Close unload
54	5	Read statistics
36	6	Forward space
46	7	Backward space
14	9	Read ASCII
04	A	Read direct
13	B	Write ASCII
03	C	Write direct
43	D	Write EOF
16	E	Rewind
26	F	Unload

Note:

DX10 opcode 8 is reserved to allow you to develop a mechanism for passing all controller commands through DX10 to the X.21 BCAIM without processing the commands.

3.9 USER-SUPPLIED PROTOCOLS

The X.21 BCAIM supports operation of user-defined and supplied protocols when they are properly downloaded, linked to existing data structures, and initialized. The steps involved in installing, linking, and initializing a protocol include:

1. Reserving X.21 BCAIM RAM for the code to be downloaded.
2. Downloading the code.
3. Linking the downloaded code to existing data structures.
4. Selecting the downloaded protocol.

The following paragraphs describe the data structures involved and provide information needed for downloading protocols.

Figure 3-12 illustrates the relationship of the protocol definition data structures involved. X.21 BCAIM ROM location >A0 contains the starting address of a 16-word protocol selection table located in X.21 BCAIM RAM. Entries in the protocol selection table point to protocol parameter tables that contain the parameters for each defined protocol. The protocol selection value (>0 through >F), specified in Open and Write Parameters commands, is doubled to provide the index to entries in the protocol selection table. For instance, if the protocol selection value in a Write Parameters command is >04, it is doubled to point to a location that is offset eight bytes from location 0 in the protocol selection table (word four of the 16-word table). Word four contains the starting address of a particular protocol parameter table. The range of protocol selection values reserved for user-defined protocols is >C through >F.

Each nonzero entry in the protocol selection table points to a protocol parameter table in X.21 BCAIM RAM. There are existing entries for protocols with protocol parameter tables resident on the X.21 BCAIM. Locations that contain zero indicate that no protocol is currently defined for that particular protocol selection value.

The protocol parameter tables contain parameters that help define a particular protocol. When selected by an Open or Write Parameters command, the contents of the selected protocol parameter table are copied into one of the channel parameter tables where the information is used to control the communication link. Parameter values that are copied into the channel parameter tables can be modified by a Write Parameters command. The Write Parameters command discussion describes the contents of the channel parameter tables in detail.

The first step in downloading code is to reserve enough X.21 BCAIM RAM space for the downloaded code. This can be done by issuing a Reserve Memory command (modifier 5, opcode D). X.21 BCAIM memory can be reserved in any size block as long as the required amount of space is available.

After reserving the necessary memory space, download the software module(s) with the Memory Load command (modifier 0, opcode C). The downloaded software must be correctly relocated for its starting address in X.21 BCAIM memory prior to downloading. Refer to the discussion on command codes earlier in this section for details on how to use each command.

When you download a new protocol parameter table, you must update existing X.21 BCAIM data structures to recognize the new protocol selection code. Typically, initialization code is written to perform the update, downloaded, and then the BLWP command is used to execute the downloaded initialization code. You must provide your own initialization code.

The initialization code must store the address of the newly defined protocol parameter table in the protocol selection table, using the protocol selection value doubled as a byte offset into the protocol selection table. Additionally, you must store the address of the character detection routine entry point table in word CPCDTB of the protocol parameter table. Entry point tables for character detection routines are discussed in more detail later in this section.

After the required intialization is complete, select the new protocol for operation with an Open or Write Parameters command.

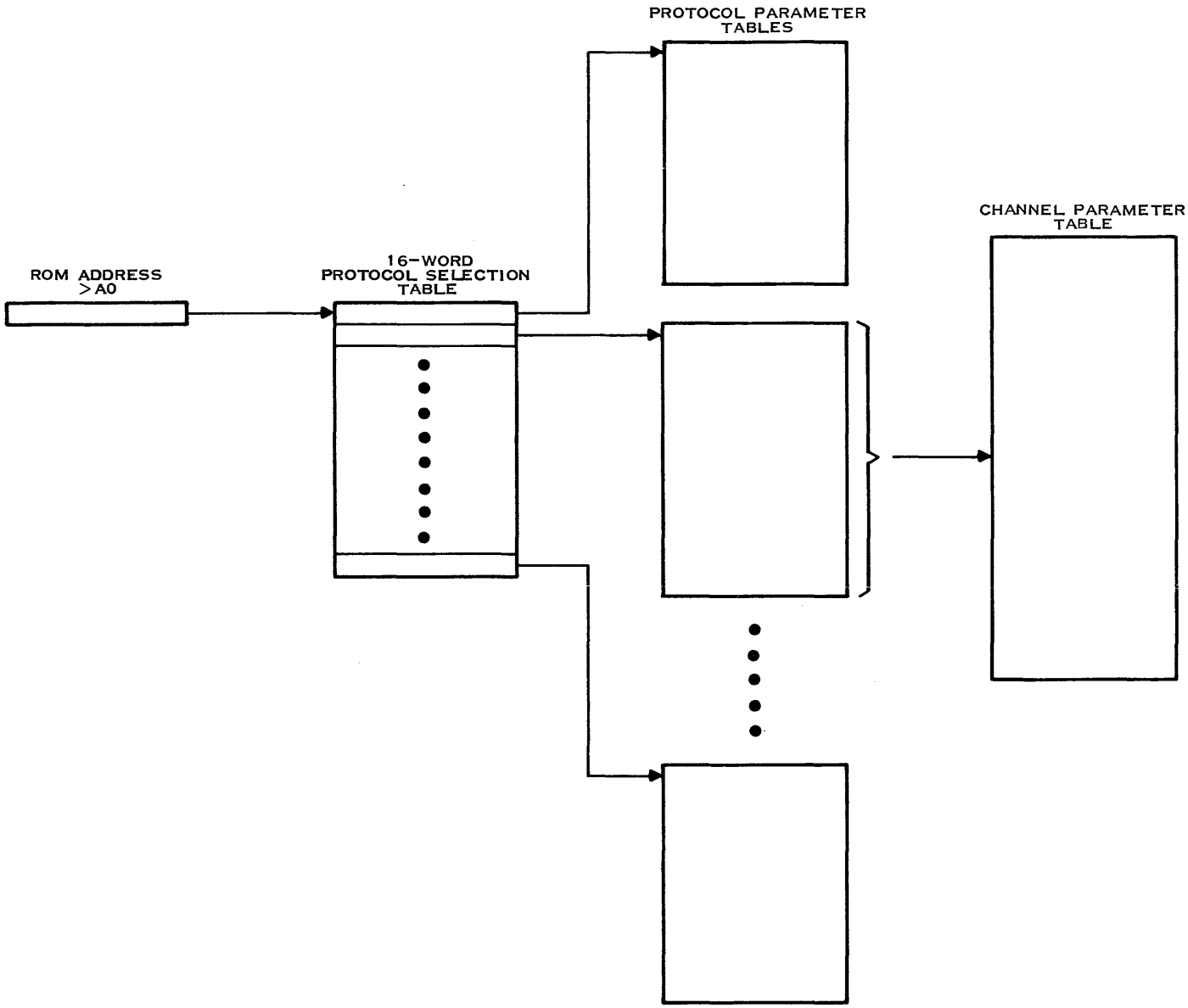


Figure 3-12. Protocol Data Structures

3.10 CHARACTER DETECTION ROUTINES

The following paragraphs describe general aspects of character detection routines. You can find specific information related to the character detection routines used by the protocols supported by the X.21 BCAIM in the appendixes. The user documentation kit described in Section 1 contains microfiche listings of example character detection routines. These listings may be helpful in writing character detection routines to support other protocols.

3.10.1 X.21 BCAIM Control Block

The control block is the X.21 BCAIM data structure that provides an interface between the 9903 ISR and the character detection routine. It is described here for those who wish to download character detection routines. Figure 3-13 shows the format of the control block. Table 3-11 describes how to use the words in the control block.

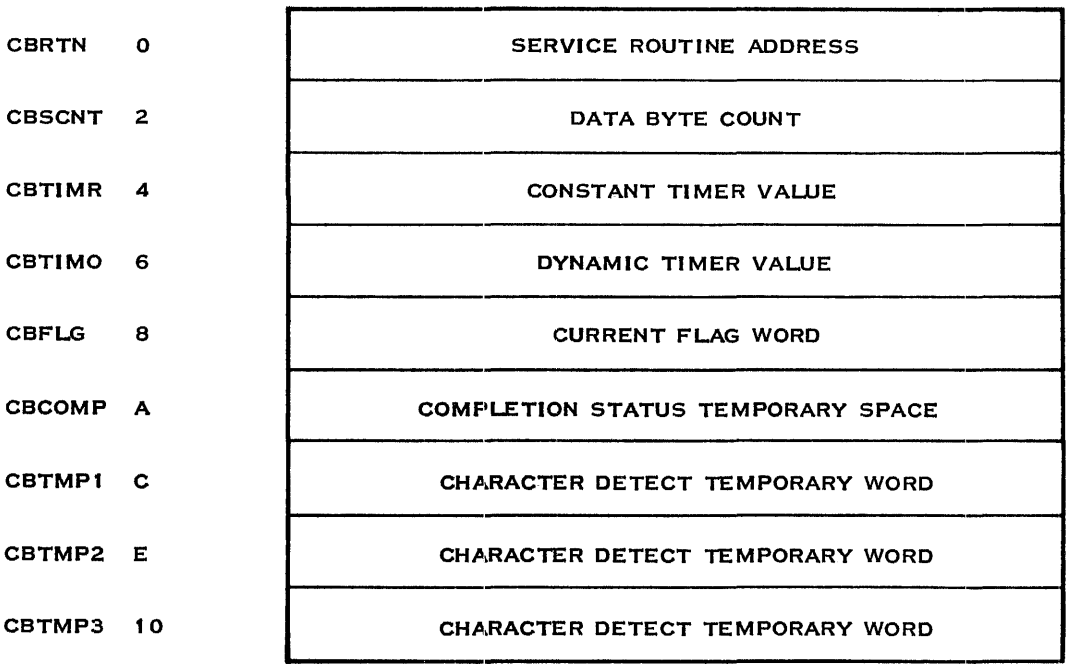


Figure 3-13. Control Block Format

Table 3-11. Control Block Word Definitions

Word	Definition
CBRTN	This word contains the current character detection routine address. A zero in this location indicates that a character detection routine was not specified.
CBSCNT	This word contains the byte count relative to the communication line. It starts equal to the byte count in the host request and is counted down.
CBTIMR	This word contains the constant timer value initialized from the inter-character time-out in the channel parameter table.
CBTIMO	This word contains the dynamic timer value that is initialized from the time-out byte of the host request for the first character, and from the CBTIMR word for subsequent characters. This word is initialized each time a data character is transferred to or from the communication line.
CBFLG	This word contains flags related to the current request. The bits are defined as follows: Bit 0 = 0 for write operation = 1 for read operation Bits 1,2 = Reserved Bit 3 = Completion report required Bits 4-7 = For protocol-dependent use Bits 8-15 = Reserved
CBCOMP	The 9900 ISR code uses this word as a temporary location for the completion status of the current request. It is not generally available for use by the character detection routine.
CBTMP1	This word is a temporary storage location provided for use by the character detection routine. It is preserved by the X.21 BCAIM firmware during processing of the request.
CBTMP2	Same as CBTMP1.
CBTMP3	Same as CBTMP1.

3.10.2 Character Detection Routine Entry Point Tables

You can replace the character detection routines existing in X.21 BCAIM ROM or add new routines when necessary to support a user-defined protocol. The downloaded character detection routine must include a table of character detection routine initial entry addresses. You must include the pointer to this table in the protocol parameter table. The character detection routine initial entry address table must contain four addresses for transmit followed by four addresses for receive (Table 3-12). These addresses are used for initial entry into the character detection routines and are selected by the modifiers in Read and Write commands.

Table 3-12. Example Character Detection Routine Entry Table

	CD Entry Point	Request	Command Modifier
CDTBL	DATA XMTONE	Transmit	0
	DATA XMTTWO		1
	DATA >FFFF		2
	DATA 0		3
	DATA RCVONE	Receive	0
	DATA RCVTWO		1
	DATA >FFFF		2
	DATA RCVALL		3

Only command modifiers in the range of 0 to 3 are legal. You can make any modifier within this range illegal by putting >FFFF in the corresponding table location. To specify that no character detection processing is necessary, such as for canned transmit messages, place an address of 0 in the corresponding table location. When you do not specify a character detection routine (by a zero entry point table entry) the requested byte count determines the end of the data transfer.

In Table 3-12, the example transmit and receive commands with modifier 2 would be considered illegal and rejected since the corresponding table location contains >FFFF. The transmit command with modifier 3 would not call a character detection routine since it has an address of 0 in the corresponding table location.

3.10.3 Character Detect Timer

A timer is implemented in X.21 BCAIM RAM as word TCKCNT. The address of TCKCNT can be found at X.21 BCAIM ROM location >A6. A nonzero value placed in TCKCNT is decremented each quarter-second until the value reaches zero. The 9903 timer interrupt processor routine performs the decrement. A character detection routine can use this timer by storing a nonzero value in TCKCNT and then monitoring TCKCNT.

3.10.4 Calling Conventions

When you download character detection routines, they must conform to the following conventions to interface properly with the 9903 ISR. Upon entry, the character detection address is picked up from offset word 0 of the control block and placed in register R8. The routine is called via:

```
BL      *R8
JMP     NRML        Normal return
JMP     TOSS        Toss character return
JMP     RESTART     Restart CRB return (receive only)
```

with R10 = Character in the high byte
R1 = Receive control block address
R3 = Transmit control block address
R7 = Unused in transmit mode,
in receive mode =

bit 0	unused (zero)
bit 1	TMS 9903 input bit 14
bit 2	TMS 9903 input bit 13
bit 3	TMS 9903 input bit 12
bit 4	TMS 9903 input bit 11
bit 5	TMS 9903 input bit 10
bit 6	TMS 9903 input bit 9
bits 7-15	Receive character

R9 = 0

NOTE

The definition of the TMS 9903 input bits can be found in the *9900 Family Systems Design and Data Book, Microprocessor Series, First Edition*, part number 97049-118-NI.

3.10.5 Registers Available for Character Detect Usage

You can use registers R6, R7, and R8 as scratch registers while in the character detection transmit code and registers R6 and R8 while in the character detection receive code. You must preserve the other registers.

3.10.6 Character Detect Return

The exit from the character detection routine differs if it is a normal return, a toss-character return, or a restart CRB return. The restart CRB option is only available on receive requests. The code that follows indicates the three exit paths. The character detection routine may change the entry address by storing the new address in offset word 0 of the control block.

For normal returns, it exits via:

```
B       *R11
        with
          R1   =  Receive control block address or
          R3   =  Transmit control block address
          R9   =  Completion information or 0 if
                  no completion information
          R10  =  Character in most significant byte
*
*  For toss-character returns, it exits via:
*
INCT      R11
B       *R11
with R1  = Receive control block address or
     R3  = Transmit control block address
     R10 = Character in most significant byte
           (transmit)
```

Tossing a transmit character means that the character in R10 is transmitted but the output FIFO pointer and count are not updated. Tossing a receive character means that the character is ignored and the input FIFO is not updated.

For restart receive CRB returns, it exits via:

```
INCT      R11
INCT      R11
B       *R11
with R1 = Receive control block address
```

For example, you can use the return to restart receive processing when address validation fails while receiving poll messages. The character detection routine performs this validation.

3.10.7 Completion Status Conventions

The character detection routines included in X.21 BCAIM firmware report completion status in R9. In R9, bits 8 through 11 are common to all protocols; bits 12 through 15 are unique for each protocol. The protocol appendix defines the unique bits. The common bits have the following meaning.

Bit 8 = Character detect completion status flag.
Additional completion information is contained in bits 12-15.
Bit 9 = CRC/LRC error flag.
Bit 10 = Host buffer overrun flag.
Bit 11 = Receiver overrun.

The completion status in R9 indicates an error only if bit 0 is set to one. If bits 9, 10, or 11 in R9 are one, bit 0 (the error bit) must also be set to one.

3.10.8 ROM Address Table

There is a table of addresses in X.21 BCAIM ROM that is useful if you download code. Table 3-13 lists the addresses and identifies the tables or other data structures to which they point.

3.11 X.21 BCAIM RAM CONFIGURATION

Figure 3-14 shows how to use the RAM on the X.21 BCAIM. You can legally use Memory Dump and Memory Load commands to dump or load addresses from >9800 to >A7FE. Use extreme caution with the Memory Load command (>1D) since it is possible to destroy critical information in X.21 BCAIM RAM.

Table 3-13. ROM Address Table

X.21 BCAIM ROM Address	Contents
>A0	Address of the protocol selection table.
>A2	Address of the DTCPT.
>A4	Address of the 9903 interrupt service table (IST). This table contains request and interrupt workspaces for the 9903 interrupt service routine (ISR) as well as other information used by the 9903 ISR.
>A6	Address of the character detection timer word TCKCNT.
>A8	Address of the transmitter enable instruction (at CMXONI) used by character detection routines during character mode operation.
>AA	Address of the CECPT.
>AC	Address of ROM-resident table of valid DCE provided information block starting characters.
>AE	Address of ROM-resident call progress code group table.
>B0	Address of X.21 clock interrupt vector.
>B2	Address of TMS 9903 clock interrupt vector.
>B4	Address of X.21 TMS 9903 receive interrupt vector.
>B6	Address of X.21 steady-state interrupt vector.
>B8	Address of TMS 9901 clock interrupt vector.
>BA	Address of X.21 TMS 9903 transmit interrupt vector.
>BC	Address of board mode word. 0 = RS-232C 1 = RS-422 2 = X.21 leased line 3 = X.21 switched line
>BE	Address of ROM-resident X.21 switched line PPT.
>C0	Address of ROM-resident X.21 leased line PPT.

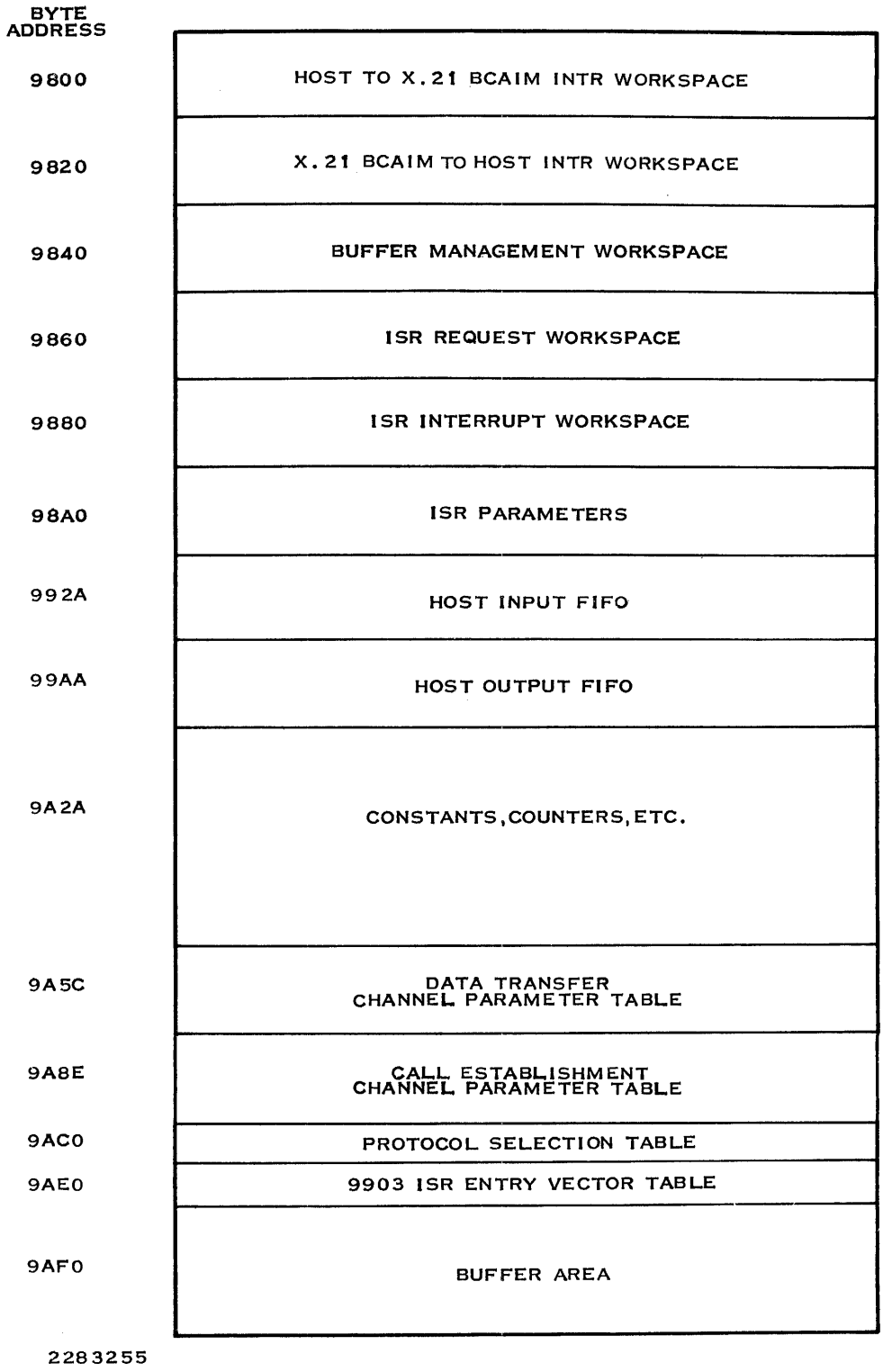


Figure 3-14. X.21 BCAIM RAM Layout

Appendix A

BOP NRZI Protocol

A.1 GENERAL

This appendix describes the use of certain protocol-dependent parameters in the BOP NRZI protocol.

A.2 COMPLETION STATUS

The completion status is reported in the sixth byte (completion status byte) of the six-byte status report. The completion status in ROSW 0 indicates an error only if the error flag (bit 0 of completion status byte 0) is set to one. Bits 8 through 11 of the status byte are common to all of the protocols and have the following meaning:

Bit	Meaning
8	Character detect completion status flag
9	CRC/LRC error flag
10	Host buffer overrun flag
11	Receiver overrun

The meaning of the hexadecimal code contained in bits 12 through 15 of the status byte is unique for each protocol. Bits 12 through 15 have the following meaning in the BOP NRZI protocol.

Hexadecimal Value of Status Bits 12-15	Meaning
0	Flag detected
1	Receive abort detected
4	Receive holding register overrun

A.3 DEFAULT PROTOCOL PARAMETERS

The default values for specific parameters (from the channel parameter table) are as follows:

Parameter	Default
Selection word	The default selection specifies internal clocking at 9600 bps with switched RTS in half-duplex mode.
Intercharacter time-outs	The default intercharacter time-out for receive and transmit is two time-out intervals or between a quarter and half second.
TMS 9903 control word	The TMS 9903 control register is set to >E43. See *9900 Family Systems Design and Data Book, Microprocessor Series, First Edition*, part number 97049-118-NI, for definition of the TMS 9903 control bits. The TMS 9903 control word selects NRZI encoding.
Leading flag character	The default leading flag character is >7E.
Initial sync count	Two leading flag characters are transmitted before a frame.
Modem signals	Bits 6, 7, 8, and 11 of CPISRF specify processing based on various modem signals. The default specifies: 1. Wait for data set ready (DSR) for open completion. 2. Must have a continuous DSR signal to maintain connected state.
Trailing pads	The default parameters specify transmitting one >FF pad byte after each frame that does not have another data frame immediately following.
Disconnect detection	If the modem signals required by bits 6, 7, 8, and 11 of CPISRF are lost for one second, the communication link will be disconnected.
Call delay	No delay is forced between successive connections.
Time-outs	Open time-outs are in one-minute increments. All other time-outs default to quarter-second increments.
Continuous RTS idle character	The default idling character is >7E when continuous RTS is specified.

A.4 CHARACTER DETECTION ROUTINE INITIAL ENTRY POINT TABLE

The character detection routine initial entry point table for the BOP NRZI protocol is as follows.

	CD Entry Point	Request	Command Modifier
TBSDLC	DATA XDSDLC	Transmit	0 Write Data
	DATA XDSDLC		1 Write Data
	DATA XDSDLC		2 Write Data
	DATA XDSDLC		3 Write Data
	DATA RDSDLC	Receive	0 Read Data
	DATA RDPOLL		1 Read Poll
	DATA RDSDLC		2 Read Data
	DATA RDPOLL		3 Read Poll

NOTE

In the BOP NRZI protocol, special command modifier 4 processing is available. For transmit requests, a command modifier of 4 causes CONTINUOUS RTS IDLE CHARACTER to be transmitted and RTS to remain high at the end of the frame. For both transmit and receive requests, the initial CD entry point selected for a command modifier 4 is the same entry as if a command modifier 0 had been used. Modifier 4 is a temporary method of keeping the channel open when more data is to be transmitted or received. The first write command received with any modifier other than 4 causes an immediate return to switched RTS. Receive character detection entry point 0 is taken for the read portion of a Chained Write command with a modifier of 4.

A.5 RECEIVE CHARACTER PROCESSING FLAGWORD (R7)

The receive character flagword (register R7) contains the flags passed from the 9903 ISR to the character detection routine each time the receive character detection routine is entered. The bits of the receive character flagword in register R7 are used as follows in the BOP NRZI protocol:

Least Significant Byte	Receive data character (right justified)	
Most Significant Byte	Bit 7	Set to zero
	Bit 6	Receive flag detected
	Bit 5	Last five bits received prior to the flag character are all ones without being followed by a zero
	Bit 4	Receiver overrun
	Bit 3	Receiver holding register overrun. Receiver holding register altered before receive holding register loaded (RHRL) is reset
	Bit 2	Receive holding register loaded
	Bit 1	Receive abort
	Bit 0	Set to zero

A.6 POLL ADDRESS VALIDATION

The Read Poll command (opcode 4, modifier 1 or 3) causes the address field of the incoming frame to be verified. Only the first two bytes of the poll address table contained in the channel parameter table are used. To accept a broadcast frame, one byte in the poll address table must be >FF. If the address does not match either byte in the poll address table, the frame is ignored and the character detection routine takes a receive reprocess exit.

Appendix B

BOP NRZ (Direct) Protocol

B.1 GENERAL

This appendix describes the use of certain protocol-dependent parameters in the BOP direct protocol.

B.2 COMPLETION STATUS

The completion status is reported in the sixth byte (completion status byte) of the six-byte status report. The completion status indicates an error only if the error flag (bit 0 of completion status byte 0) is set to one. Bits 8 through 11 of the status byte are common to all of the protocols and have the following meaning:

Bit	Meaning
8	Character detect completion status flag
9	CRC/LRC error flag
10	Host buffer overrun flag
11	Receiver overrun

The meaning of the hexadecimal code contained in bits 12 through 15 of the status byte is unique for each protocol. Bits 12 through 15 have the following meaning in the BOP direct protocol.

Hexadecimal Value of Status Bits 12–15	Meaning
0	Flag detected
1	Receive abort detected
4	Receive holding register overrun

B.3 DEFAULT PROTOCOL PARAMETERS

The default values for specific parameters (from the channel parameter table) are as follows:

Parameter	Default
Selection word	The default selection specifies external timing with continuous RTS in full-duplex mode.
Intercharacter time-outs	The default intercharacter time-out for receive and transmit is two time-out intervals or between a quarter and half second.
TMS 9903 control word	The TMS 9903 control register is set to >643. See *9900 Family Systems Design and Data Book, Microprocessor Series, First Edition*, part number 97049-118-NI, for definition of the TMS 9903 control bits. The TMS 9903 control word selects NRZ (direct) encoding.
Leading flag character	The default leading flag character is >7E.
Modem signals	Bits 6, 7, 8, and 11 of CPISRF specify processing based on various modem signals. The default specifies: 1. Wait for data set ready (DSR) for open completion. 2. Must have a continuous DSR signal to maintain connected state.
Trailing pads	The default parameters specify transmitting one >FF pad byte after each frame that does not have another data frame immediately following.
Disconnect detection	If the modem signals required by bits 6, 7, 8, and 11 of CPISRF are lost for one second, the communication link will be disconnected.
Call delay	No delay is forced between successive connections.
Initial sync count	One leading flag character is transmitted before a frame.
Time-outs	Open time-outs are in one-minute increments. All other time-outs default to quarter-second increments.
Continuous RTS idle character	The default idling character is >7E when idle character continuous RTS is specified.

B.4 CHARACTER DETECTION ROUTINE INITIAL ENTRY POINT TABLE

The character detection routine initial entry point table for the BOP direct protocol follows.

	CD Entry Point	Request	Command Modifier
TBSDLC	DATA XDSDLC	Transmit	0 Write Data
	DATA XDSDLC		1 Write Data
	DATA XDSDLC		2 Write Data
	DATA XDSDLC		3 Write Data
	DATA RDSDLC	Receive	0 Read Data
	DATA RDPOLL		1 Read Poll
	DATA RDSDLC		2 Read Data
	DATA RDPOLL		3 Read Poll

NOTE

In the BOP direct protocol, special command modifier 4 processing is available. For transmit requests, a command modifier of 4 causes a continuous RTS idle character to be transmitted and the RTS signal to remain high at the end of the frame. For both transmit and receive requests, the initial CD entry point selected for a command modifier 4 is the same entry as if a command modifier 0 had been used. Modifier 4 is used as a temporary method of keeping the channel open when more data is to be transmitted or received. The first write command modifier received other than 4 causes an immediate return to switched RTS. Receive character detection entry point 0 is taken for the receive portion of a Chained Write command with modifier 4.

B.5 RECEIVE CHARACTER PROCESSING FLAGWORD

The receive character flagword (register R7) contains the flags passed from the 9903 ISR to the character detection routine each time the receive character detection routine is entered. The bits of the receive character flagword in register R7 are used as follows in the BOP direct protocol:

Least Significant Byte	Receive data character (right-justified)	
Most Significant Byte	Bit 7	Set to zero
	Bit 6	Receive flag detected
	Bit 5	Last five bits received prior to the flag character are all ones without being followed by a zero
	Bit 4	Receiver overrun
	Bit 3	Receiver holding register overrun. Receiver holding register altered before receive holding register loaded (RHRL) is reset.
	Bit 2	Receive holding register loaded.
	Bit 1	Receive abort
	Bit 0	Set to zero

B.6 POLL ADDRESS VALIDATION

The Read Poll command (opcode 4, modifier 1 or 3) causes verification of the address field of the incoming frame. Only the first two bytes of the poll address table contained in the channel parameters table are used. To accept a broadcast frame, one byte in the poll address table must be >FF. If the address does not match either byte in the poll address table, the frame is ignored and the character detection routine takes a receive reprocess exit.

Appendix C

BOP NRZI Protocol with Modem Clock

C.1 GENERAL

This appendix describes the use of certain protocol-dependent parameters in a user-loaded BOP NRZI protocol that obtains timing from the modem-supplied clock.

C.2 COMPLETION STATUS

The completion status is reported in the sixth byte (completion status byte) of the six-byte status report. The completion status in ROSW 0 indicates an error only if the error flag (bit 0 of completion status byte 0) is set to one. Bits 8 through 11 of the status byte are common to all of the protocols and have the following meaning:

Bit	Meaning
8	Character detect completion status flag
9	CRC/LRC error flag
10	Host buffer overrun flag
11	Receiver overrun

The meaning of the hexadecimal code contained in bits 12 through 15 of the status byte is unique for each protocol. Bits 12 through 15 have the following meaning in the BOP NRZI protocol.

Hexadecimal Value of Status Bits 12-15	Meaning
0	Flag detected
1	Receive abort detected
4	Receive holding register overrun

C.3 DEFAULT PROTOCOL PARAMETERS

The default values for specific parameters (from the channel parameter table) are as follows:

Parameter	Default
Selection word	This word should specify external timing with continuous RTS in the full-duplex mode.
Intercharacter time-outs	The intercharacter time-out for receive and transmit is two time-out intervals or between a quarter and half second.
TMS 9903 control word	The TMS 9903 control register is set to >8643. See *9900 Family Systems Design and Data Book, Microprocessor Series, First Edition*, part number 97049-118-NI, for definition of the TMS 9903 control bits. The TMS 9903 control word selects direct encoding with the BOP NRZI encode and decode circuits enabled.
Leading flag character	The default leading flag character is >7E.
Initial sync count	Two leading flag characters are transmitted before a frame.
Modem signals	Bits 6, 7, 8, and 11 of CPISRF specify processing based on various modem signals. The default specifies: 1. Wait for data set ready (DSR) for open completion. 2. Must have a continuous DSR signal to maintain connected state.
Trailing pads	One >FF pad byte should be transmitted after each frame that does not have another data frame immediately following.
Disconnect detection	If the modem signals required by bits 6, 7, 8, and 11 of CPISRF are lost for one second, the communication link will be disconnected.
Call delay	No delay is forced between successive connections.
Time-outs	Open time-outs are in one-minute increments. All other time-outs default to quarter-second increments.
Continuous RTS idle character	The default idling character is >7E when continuous RTS is specified.

C.4 CHARACTER DETECTION ROUTINE INITIAL ENTRY POINT TABLE

The character detection routine initial entry point table for BOP NRZI protocol with modem-supplied clock follows.

	CD Entry Point	Request	Command Modifier
TBSDLC	DATA XDSDLC	Transmit	0 Write Data
	DATA XDSDLC		1 Write Data
	DATA XDSDLC		2 Write Data
	DATA XDSDLC		3 Write Data
	DATA RDSDLC	Receive	0 Read Data
	DATA RDPOLL		1 Read Poll
	DATA RDSDLC		2 Read Data
	DATA RDPOLL		3 Read Poll

NOTE

In the BOP NRZI protocol with modem-supplied clock, special command modifier 4 processing is available. For transmit requests a command modifier of 4 causes CONTINUOUS RTS IDLE CHARACTER to be transmitted and RTS to remain high at the end of the frame. For both transmit and receive requests, the initial CD entry point selected for a command modifier 4 is the same entry as if a command modifier 0 had been used. Modifier 4 is a temporary method of keeping the channel open when more data is to be transmitted or received. The first write command received with any modifier other than 4 causes an immediate return to switched RTS. Receive character detection entry point 0 is taken for the read portion of a Chained Write command with a modifier of 4.

C.5 RECEIVE CHARACTER PROCESSING FLAGWORD (R7)

The receive character flagword (register R7) contains the flags passed from the 9903 ISR to the character detection routine each time the receive character detection routine is entered. The bits of the receive character flagword in register R7 are used as follows in the BOP NRZI protocol:

Least Significant Byte	Receive data character (right justified)
Most Significant Byte	Bit 7 Set to zero
	Bit 6 Receive flag detected
	Bit 5 Last five bits received prior to the flag character are all ones without being followed by a zero
	Bit 4 Receiver overrun
	Bit 3 Receiver holding register overrun. Receiver holding register altered before receive holding register loaded (RHRL) is reset
	Bit 2 Receive holding register loaded
	Bit 1 Receive abort
	Bit 0 Set to zero

C.6 POLL ADDRESS VALIDATION

The Read Poll command (opcode 4, modifier 1 or 3) causes verification of the address field of the incoming frame. Only the first two bytes of the poll address table contained in the channel parameter table are used. To accept a broadcast frame, one byte in the poll address table must be >FF. If the address does not match either byte in the poll address table, the frame is ignored and the character detection routine takes a receive reprocess exit.

Appendix D

X.21 Switched Line Protocol

D.1 GENERAL

This appendix describes the use of certain protocol-dependent parameters in the X.21 switched line protocol. The X.21 BCAIM call establishment channel parameter table (CECPT) in Section 3 defines this protocol.

D.2 COMPLETION STATUS

The completion status is reported in the sixth byte (completion status byte) of the six-byte status report. The completion status indicates an error only if the error flag (bit 0 of byte 0) is set to one. An error from an Open command, returned in the command completion status report, indicates that the X.21 network did not establish a connection.

D.3 DEFAULT PROTOCOL PARAMETERS

The default values for specific parameters (from the channel parameter table) are as follows:

Parameter	Default
Selection word	The default selection specifies external clocking with continuous RTS in full-duplex mode.
TMS 9903 control word	The TMS 9903 control register is set to >0083. See *9900 Family Systems Design and Data Book, Microprocessor Series, First Edition*, part number 97049-118-NI, for definition of the TMS 9903 control bits.
Leading sync character	The default leading sync character is >16.
Initial sync count	Two leading flag characters are transmitted before a frame.
Call progress signal block size	The default value is one call progress signal block with a maximum character count of >1C.

Parameter	Default
DCE signals	Bits 7, 8, 9, and 11 of CXISRF specify processing based on various DCE signals. The default specifies: 1. Abort call on even parity. 2. Accept call charge information. 3. Wait for network responses to complete open. 4. First character of network information is valid.
Charge information block length	The default charge information block length is >1C bytes.
Trailing pads	The default parameters specify transmitting one >2B pad byte after each data block.
Disconnect detection	If the I signal is lost for 16 bit times, the communication link will be disconnected.
Call delay	A two-second delay is forced between successive connections.
Time-outs	Open time-outs are in quarter-second increments. All other time-outs default to quarter-second increments. Nominal default time-out periods are: T0 = 3 seconds, T1 = 3 seconds, T2 = 20 seconds, T3A = 2 seconds, T3B = 60 seconds, T4 = 2 seconds, T5 = 2 seconds, T6 = 2 seconds, T7 = 0.5 seconds
DCE provided information block	The default value is one DCE provided information block of >80 bytes.
Call charge start character	The default call charge information block start character is >2F.
Registration/ termination character	The default facility registration/cancellation termination character is >2D.
Network idle character	The network idle character expected in state 05 during call initiation is >2B.

Appendix E

X.21 Switched Line State Flow

E.1 GENERAL

The protocol for handling calls on the X.21 network requires the DTE and DCE to go through a number of different states to originate, connect, and disconnect calls. The states involved fall into the following major groups:

- Quiescent states
- Call establishment states
- Call reception states
- Call clearing states

This appendix describes the conditions necessary for entry into and exit from each state, DTE and DCE termination states allowed in each state, and error conditions that are applicable to each state for X.21 switched operation of the X.21 BCAIM.

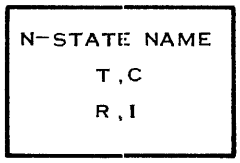
Figures E-2 through E-5 illustrate the flow within each group of states. Figure E-1 is a legend for the other illustrations. Each block in Figures E2 through E-5 contains the state number, the state name, and the state of the signals on the following circuits:

Transmit	(T)
Receive	(R)
Control	(C)
Indication	(I)

The blocks marked with an asterisk indicate that a string of characters is being transmitted or received in that state on a particular circuit instead of having a steady-state signal. An X in any block indicates that the state of the particular signal does not matter.

E.2 STATE DESCRIPTIONS

The state descriptions in the following paragraphs are closely tied to the flowcharts in Figures E-2 through E-5.



N = STATE NUMBER

T = SIGNAL ON TRANSMIT (T) CIRCUIT
C = SIGNAL ON CONTROL (C) CIRCUIT
R = SIGNAL ON RECEIVE (R) CIRCUIT
I = SIGNAL ON INDICATION (I) CIRCUIT

SYMBOLS FOR SIGNALS ON THESE CIRCUITS ARE:

0 = BINARY 0 CONDITION
1 = BINARY 1 CONDITION
+ = IA5 + CHARACTER
OFF = THIS CIRCUIT IS IN THE OFF CONDITION
ON = THIS CIRCUIT IS IN THE ON CONDITION
IA5 = CONTINUOUS STRING OF IA5 CHARACTERS
D = DATA
BEL = IA5 BEL CHARACTER
SYN = SYNCHRONIZATION CHARACTER
X = DON T CARE

2283256

Figure E-1. X.21 Switched Line Flowchart Legend

E.2.1 State 01, Ready

In this state, T = 1, C = off, R = 1, and I = off.

E.2.1.1 State 01 Entry Conditions. The X.21 BCAIM enters state 01 from state 14 when the host issues an Open accept command to X.21 BCAIM. It remains in this state until the network initiates a call or the Open accept command times out.

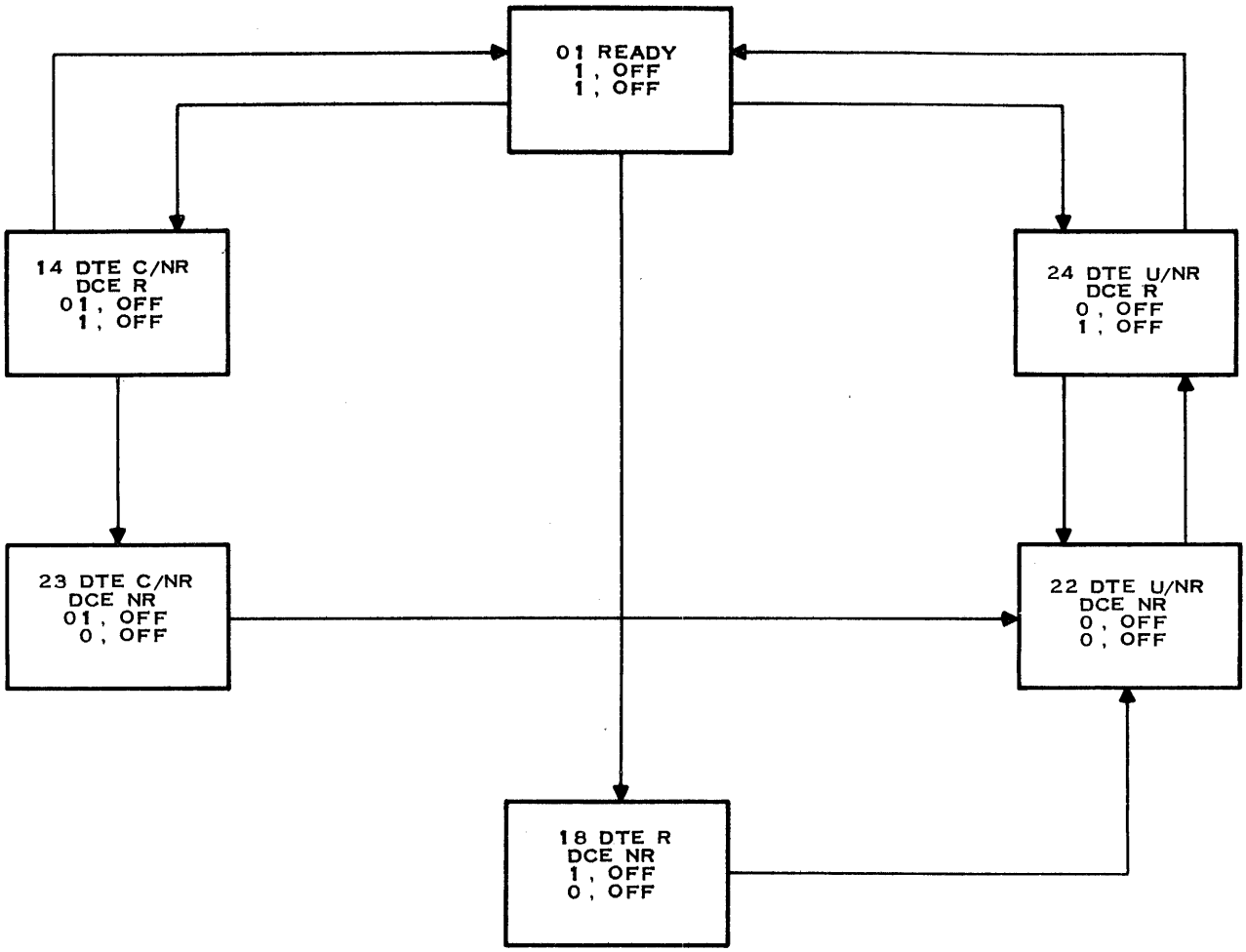
The X.21 BCAIM enters state 01 from state 14 when the host issues an Open initiate command to the X.21 BCAIM. It remains in this state for the minimum time allowed before entering state 02. Any call from the network causes a call collision and the Open initiate command is retried.

The X.21 BCAIM enters state 01 from state 21 in clear processing. Entry from state 21 indicates that either the network cleared the call or connection, or that the X.21 BCAIM cleared the call or connection. The X.21 BCAIM waits in state 01 until the T7 timer expires if both of the following conditions are true:

- If the X.21 BCAIM enters this state via state 21 from state 13
- If bit 8 of word CXISRF in the CECPT is not set

Any other entry from state 21 causes the X.21 BCAIM to remain in this state the minimum allowed time before entering state 14.

The X.21 BCAIM enters state 01 from state 24 in reset processing. During reset processing, entry from state 24 causes it to remain in this state the minimum allowed time before entering state 14. Any call from the network is cleared during reset processing.



NOTES:

1. STATE 14 IS THE NORMAL CLOSED STATE OF THE X.21 BCAIM
2. RESET AND POWER-UP PROCESSING ENTER STATES 22 OR 24.

2283257

Figure E-2. X.21 Switched Line Quiescent States Flowchart

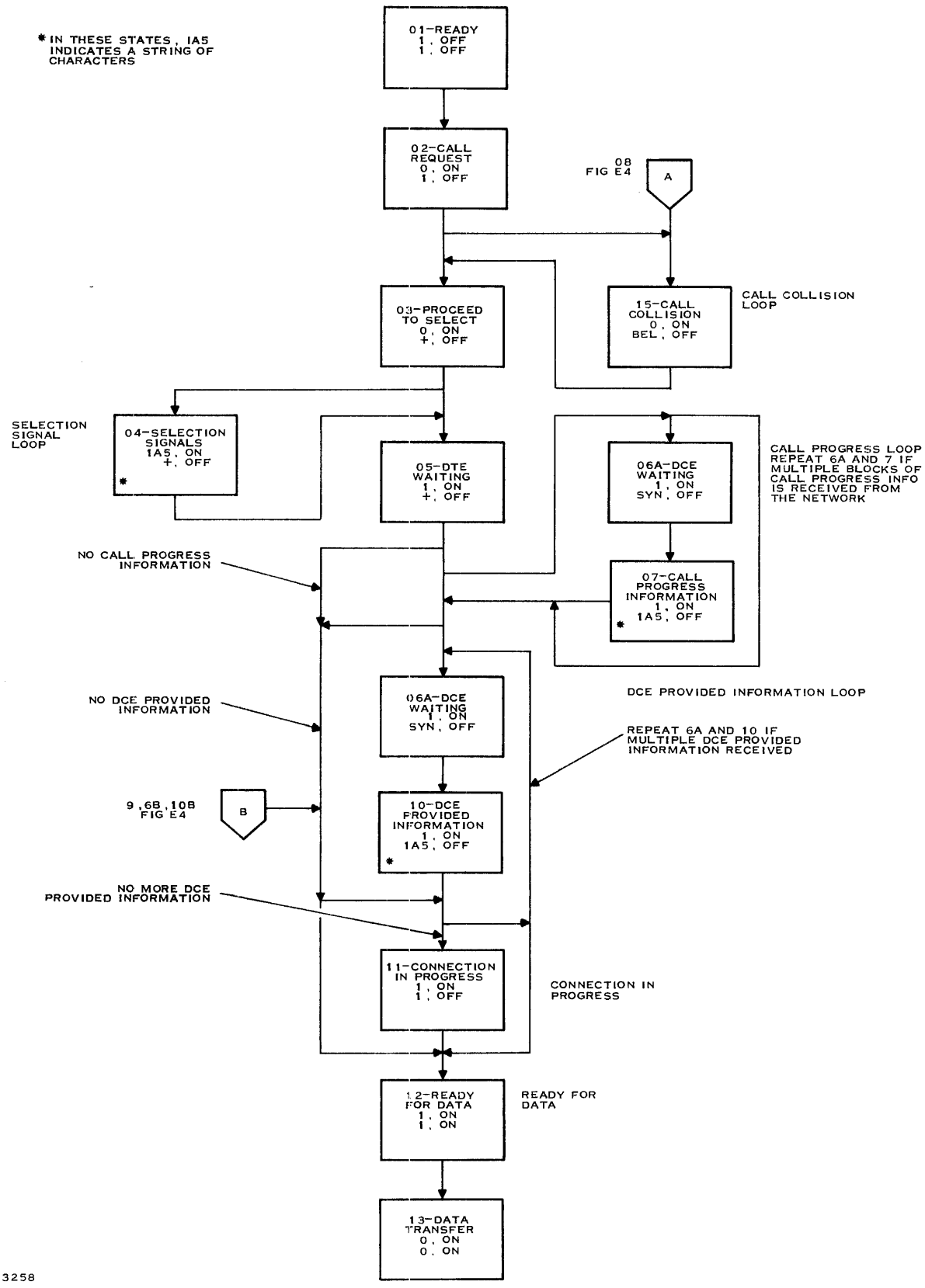


Figure E-3. X.21 Switched Line Call Establishment States Flowchart

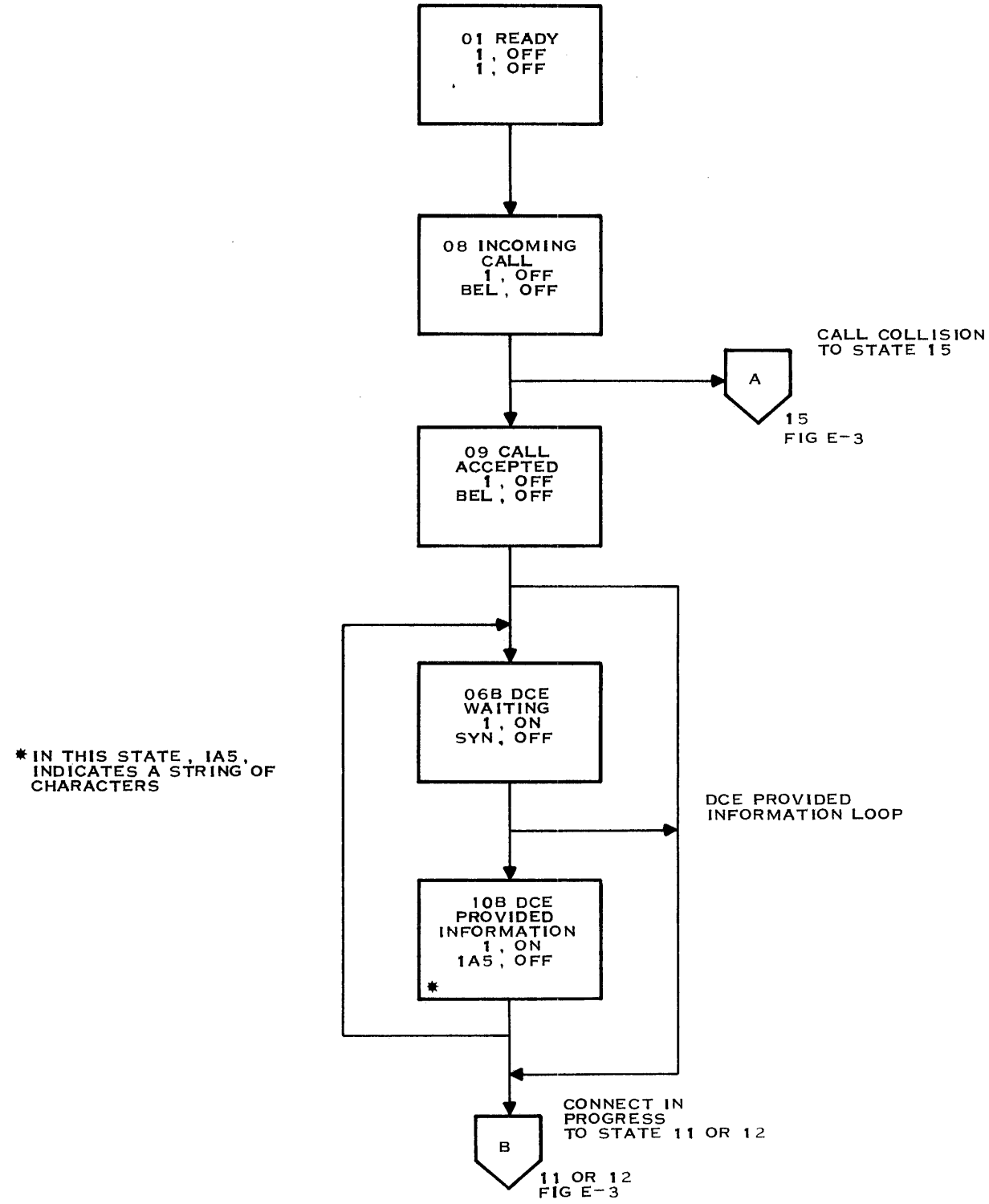


Figure E-4. X.21 Switched Line Call Reception States Flowchart

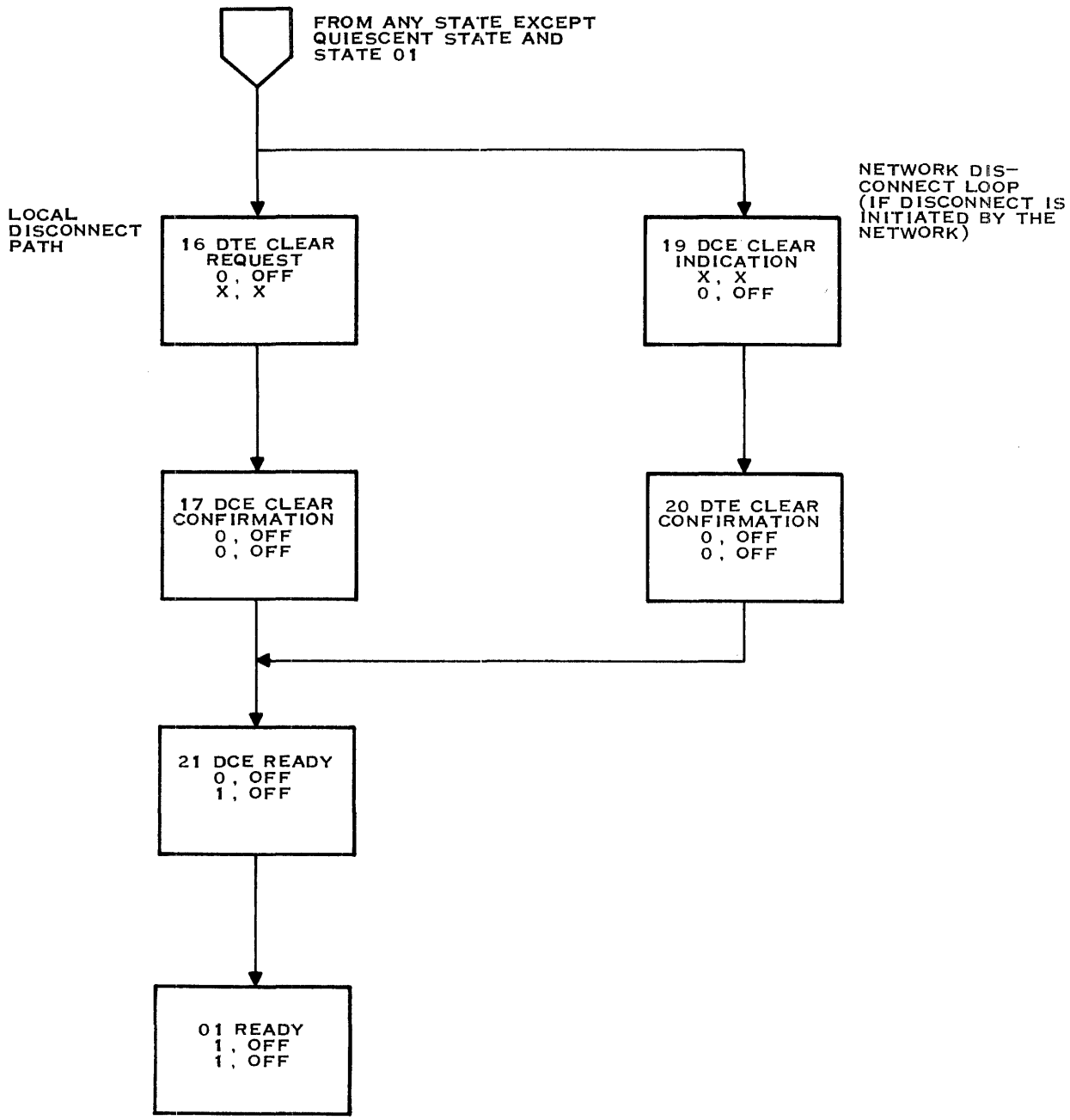


Figure E-5. X.21 Switched Line Call Clearing States Flowchart

E.2.1.2 State 01 Exit Conditions. An exit from state 01 to state 02 occurs when an Open initiate command is issued. The signals in state 02 are as follows:

Next State	State Name	State of Signals	State Set By
02	Call Request	T = 0 C = On R = 1 I = Off	DTE

The T signal transition from 1 to 0 must be within seven bit times of the C Signal transition from off to on. Either transition can occur first.

An incoming call causes an exit from state 01 to state 08. The signals in state 08 are as follows:

Next State	State Name	State of Signals	State Set By
08	Incoming Call	T = 1 C = Off R = BEL I = Off	DCE

The incoming call state (08) starts upon reception of two or more SYN characters followed by a continuous transmission of BEL characters.

Time limit T0 is defined as the time period from when the X.21 BCAIM detects the first SYN character, to the start of state 08. This time period is normally three seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time limit T7 is normally 0.5 seconds and is defined as the time period from when the network enters state 01 until the start of state 08. This time allows the network to provide call charge information to the X.21 BCAIM. Refer to state 10 BIS for information on charge information. The X.21 BCAIM enters state 14 when it exceeds this time limit.

E.2.1.3 DTE Termination States Allowed from State 01. The X.21 BCAIM enters state 14 when it is powered up but not open. This condition indicates to the X.21 network that the X.21 BCAIM has completed power up but has not received commands from the host to allow communication with the network. The signals in state 14 are as follows:

Next State	State Name	State of Signals	State Set By
14	DTE Cont, N/R DCE Ready	T = 01 C = Off R = 1 I = Off	DTE

The X. 21 BCAIM enters state 24 when it is not powered up or when it is reset. This indicates to the network that the X.21 BCAIM is not currently functional, that the X.21 cable is disconnected, or that a DCE error exists. The result is that the X.21 BCAIM is unable to function in the X.21 network. The signals in state 24 are as follows:

Next State	State Name	State of Signals		State Set By
24	DTE Uncont, N/R DCE Ready	T = 0 R = 1	C = Off I = Off	DTE

E.2.1.4 DCE Termination States Allowed from State 01. The X.21 BCAIM enters state 18 when either the network or the DCE is unable to continue call processing. This state causes the X.21 BCAIM to terminate all outstanding requests and report a disconnect error code. The signals in state 18 are as follows:

Next State	State Name	State of Signals		State Set By
18	DTE Ready DCE Not Ready	T = 1 R = 0	C = Off I = Off	DCE

E.2.1.5 Other Error Conditions in State 01.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends upon several factors. If the character is garbled and not a result of the transition to state 18, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 18, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends upon several factors. If the character is garbled and not due to transition to state 18, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 18, the character is tossed.

- Invalid I Circuit Transition — The X.21 BCAIM's response to reception of an invalid I circuit response is to clear the call.

E.2.2 State 02, Call Request

The X.21 BCAIM enters state 02 when the DTE is requesting a call. In this state, T = 0, R = 1, C = on, and I = off.

E.2.2.1 State 02 Entry Conditions. The X.21 BCAIM enters state 02 from state 01 when the host issues an Open initiate command. It remains in this state until conditions allow it to enter state 03 or until the T1 time-out expires. Entering state 15 terminates any call from the network.

E.2.2.2 State 02 Exit Conditions. The X.21 BCAIM exits state 02 and goes to state 01 if the T1 timer expires. Time-out T1 starts after signaling state 02 and expires if the X.21 BCAIM does not enter state 03. The duration of this timer is normally three seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 03 when it receives two or more SYN characters followed by continuous (+) characters. The signals in state 03 are as follows:

Next State	State Name	State of Signals	State Set By
03	Proceed to Select	T = 0 C = On R = + I = Off	DCE

The X.21 BCAIM enters state 15 upon reception of two or more SYN characters followed by a continuous transmission of BEL characters. The signals in state 15 are as follows:

Next State	State Name	State of Signals	State Set By
15	Call Collision	T = 0 C = On R = BEL I = Off	DCE

E.2.2.3 DTE Termination States Allowed from State 02. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
16	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

E.2.2.4 DCE Termination States Allowed from State 02. The X.21 BCAIM enters state 19 when the network or DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report a disconnect error. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.2.5 Other Error Conditions in State 02.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

- Invalid I Circuit Transition — The X.21 BCAIM's response to reception of an invalid I circuit response is to clear the call.

E.2.3 State 03, Proceed to Select

The X.21 BCAIM enters state 03 when the DCE is responding to DTE calling. In this state, T = 0, C = on, R = +, and I = off.

E.2.3.1 State 03 Entry Conditions. The X.21 BCAIM enters state 03 from state 02 after it receives an Open initiate command from the host. It remains in this state until conditions allow it to enter state 04 or state 05. During this state, it receives continuous (+) characters from the network.

E.2.3.2 State 03 Exit Conditions. An exit from state 03 to state 04 occurs when the X.21 BCAIM transmits two or more SYN characters followed by transmission of the first character of selection signal information from a buffer in X.21 BCAIM RAM. This buffer is described in the description of the X.21 Call Data Memory Load command. Entering state 04 when direct call capability exists on a per call basis indicates an addressed call request. The signals in state 04 are as follows:

Next State	State Name	State of Signals	State Set By
04	Selection Signals	T = IA5 C = On R = + I = Off	DTE

The X.21 BCAIM setting a steady binary 1 condition on the T circuit causes an exit from state 03 to state 05. Entering state 05 when direct call capability exists indicates a request for a direct call. The host requests a direct call by setting bit 6 in word CXISRF of the CECPT to a 1.

Entering state 05 when direct call capability exists on a per-call basis indicates a request for a direct call. Entering state 05 when direct call capability is provided on a subscription basis is mandatory. The signals in state 05 are as follows:

Next State	State Name	State of Signals	State Set By
05	DTE Waiting	T = 1 C = On R = + I = Off	DTE

E.2.3.3 DTE Termination States Allowed from State 03. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or if an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
16	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

E.2.3.4 DCE Termination States Allowed from State 03. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report a disconnect error. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.3.5 Other Error Conditions in State 03.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 19, the character is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

- Invalid I Circuit Transition — The X.21 BCAIM's response to reception of an invalid I circuit response is to clear the call.

E.2.4 State 04, Selection Signals
Facility registration/cancellation state. In this state, T = IA5, C = on, R = +, and I = off.

E.2.4.1 State 04 Entry Conditions. The X.21 BCAIM enters state 04 from state 03 when the host issues an Open initiate command. In this state, the DTE transmits selection signals to the network. The selection signal state is entered by transmission of two or more SYN characters to the network followed by the transmission of the first character in the preloaded selection signal buffer. It remains in this state until conditions allow it to enter state 05. While in state 04, it receives continuous (+) characters from the network.

The host is not required to include the terminating character (+) in the preloaded selection signal buffer. The X.21 BCAIM obtains the terminating character from the CECPT.

The selection sequence consists of one of the following items:

1. A facility request block. Each facility request block consists of one or more facility request signals separated by a comma (,) character. The end of the facility request block is terminated by a dash (-) character.

   a. The facility request signal consists of a faciltiy request code and may contain one or more facility request parameters.

   b. The facility request code, facility parameter and subsequent facility parameters are separated by a slash (/) character. This feature may not be implemented on some networks yet.

2. An address block. Each address block consists of one or more address signals, each signal is separated by a comma (,) character.

   a. Each address signal consists of a full address signal or an abbreviated address signal.

   b. An abbreviated address signal is preceded by a period (.) character.

3. A facility request block followed by an address block.

4. A facility registration/cancellation block.

5. Each facility registration/cancellation block consists of one or more facility registration/cancellation signals separated by a comma (,) character. The end of the facility registration/cancellation block is terminated by a dash (-) character.

A facility registration/cancellation signal consists of up to four ordered elements: facility request code, indicator, registration parameter, and address signal. If an element is not to be sent in the sequence, insert a 0 character in the position for the replaced character. Eliminate the elements in reverse order for cancellation if less than four are used.

E.2.4.2 Exit Conditions from State 04. When the X.21 BCAIM sets a steady binary 1 condition on the T circuit, it causes an exit to state 05. The signals in state 05 are as follows:

Next State	State Name	State of Signals	State Set By
05	DTE Waiting	T = 1 C = On R = + I = Off	DTE

E.2.4.3 DTE Termination States Allowed from State 04. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
16	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

E.2.4.4 DCE Termination States Allowed from State 04. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report a disconnect error code. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.4.5 Other Error Conditions in State 04.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 19, the character is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

- Invalid I Circuit Transition — The X.21 BCAIM's response to reception of an invalid I circuit response is to clear the call.

E.2.5 State 05, DTE Waiting
This is the wait for network state. In this state, T = 1, C = on, R = +, and I = off.

E.2.5.1 State 05 Entry Conditions. The X.21 BCAIM enters this state from state 03 or state 04 when the host issues an Open initiate command. It remains in this state until conditions allow it to enter states 06A, 11, or 12 or until the T2 time-out expires.

While in state 05, it receives continuous (+) characters from the network.

E.2.5.2 State 05 Exit Conditions. Time-out T2, starts after the X.21 BCAIM signals state 05 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally 20 seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 06A when it receives two or more SYN characters. The signals in state 06A are as follows:

Next State	State Name	State of Signals	State Set By
06A	DCE Waiting	T = 1 C = On R = SYN I = Off	DCE

The X.21 BCAIM enters state 11 when it receives a steady-state 1 on the R circuit. The signals in state 11 are as follows:

Next State	State Name	State of Signals	State Set By
11	Connection in Progress	T = 1 C = On R = 1 I = Off	DCE

The X.21 BCAIM enters state 12 is when it receives a steady-state 1 condition on the R circuit and a steady-state on condition on the I circuit. The signals in state 12 are as follows:

Next State	State Name	State of Signals	State Set By
12	Ready for Data	T = 1 C = On R = 1 I = On	DCE

E.2.5.3 DCE Termination States Allowed from State 05. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
16	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

E.2.5.4 DCE Termination States Allowed from State 05. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. State 19 causes the X.21 BCAIM to terminate all outstanding requests and report disconnect errors. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.5.5 Other Error Conditions in State 05.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to states 11, 12, or 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to states 11, 12, or 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to states 11, 12, or 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to states 11, 12, or 19, the character is tossed.

- Invalid I Circuit Transition — The X.21 BCAIM's response to reception of an invalid I circuit response is to clear the call.

E.2.6 State 06A, DCE Waiting
This is the network waiting state. In this state, T = 1, C = on, R = SYN, and I = off.

E.2.6.1 State 06A Entry Conditions. The X.21 BCAIM enters state 06A from states 05, 07, or 10 when the host issues an Open initiate command. It remains in this state until conditions allow it to enter state 07, 10, 11, or 12 or until the T2 time-out expires.

E.2.6.2 State 06A Exit Conditions. Time-out T2 starts after signaling state 05 and it expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally 20 seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 07 upon reception of a numeric character. The signals in state 07 are as follows:

Next State	State Name	State of Signals	State Set By
07	Call Progress Signals	T = 1 C = On R = IA5 I = Off	DCE

The X.21 BCAIM enters state 10 upon reception of a valid DCE character. Refer to the definition of the word CXDCEI in the description of the CECPT in Section 3. The signals in state 10 are as follows:

Next State	State Name	State of Signals	State Set By
10	DCE Provided Information	T = 1 C = On R = IA5 I = Off	DCE

The X.21 BCAIM enters state 11 upon reception of a steady-state 1 condition on the R circuit. The signals in state 11 are as follows:

Next State	State Name	State of Signals		State Set By
11	Connection in Progress	T = 1 R = 1	C = On I = Off	DCE

The X.21 BCAIM enters state 12 upon reception of a steady-state 1 condition on the R circuit and a steady-state on condition on the I circuit. The signals in state 12 are as follows:

Next State	State Name	State of Signals		State Set By
12	Ready for Data	T = 1 R = 1	C = On I = On	DCE

E.2.6.3 DTE Termination States Allowed from State 06A. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals		State Set By
16	DTE Clear Request	T = 0 R = X	C = Off I = X	DTE

E.2.6.4 DCE Termination States Allowed from State 06A. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect error codes. The signals in state 19 are as follows:

Next State	State Name	State of Signals		State Set By
19	DCE Clear Request	T = X R = 0	C = X I = Off	DCE

E.2.6.5 Other Error Conditions in State 06A.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19, the character is tossed.

E.2.7 State 06B, DCE Waiting

This is the network waiting state. In this state, T = 1, C = on, R = SYN, and I = off.

E.2.7.1 State 06B Entry Conditions. The X.21 BCAIM enters this state from states 09 or 10 BIS when the host issues an Open accept command or when the network establishes a call to provide call charge information. It remains in this state until conditions allow it to enter states 10 BIS, 11 or 12 or until the T4 time-out expires.

E.2.7.2 State 06B Exit Conditions. Time-out T4 starts after signaling state 09 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally two seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 10 BIS upon reception of a valid DCE information character. Refer to the the description of word CXDCEI in the CECPT discussion in Section 3. The signals in state 10 BIS are as follows:

Next State	State Name	State of Signals	State Set By
10 BIS	DCE Provided Information	T = 1 C = On R = IA5 I = Off	DCE

The X.21 BCAIM enters state 11 upon reception of a steady-state 1 condition on the R circuit. The signals in state 11 are as follows:

Next State	State Name	State of Signals	State Set By
11	Connection in Progress	T = 1 C = On R = 1 I = Off	DCE

The X.21 BCAIM enters state 12 upon reception of a steady-state 1 condition on the R circuit and a steady-state on condition on the I circuit. The signals in state 12 are as follows:

Next State	State Name	State of Signals	State Set By
12	Ready for Data	T = 1 C = On R = 1 I = On	DCE

E.2.7.3 DTE Termination States Allowed from State 06B. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
16	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

E.2.7.4 DCE Termination States Allowed from State 06B. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect error codes. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.7.5 Other Error Conditions in State 06B.

- Even Character Parity Detected -- The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, the character is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19, the character is tossed.

E.2.8 State 07, Call Progress Signal Sequence
In this state, T = 1, C = on, R = IA5, and I = off.

E.2.8.1 State 07 Entry Conditions. The X.21 BCAIM enters state 07 from state 06A when the host issues an Open initiate command. The DCE uses this state to transmit call progress signals to the X.21 BCAIM. It enters the call progress signal state when it receives a numeric character from the network and remains in this state until conditions allow it to enter state 06A, 11, or 12.

The host is not required to search for the terminating character when call progress information is requested. Refer to the description of the Call Progress Signal Dump command in Section 3.

The call progress sequence consists of one or more call progress signal blocks. The plus (+) character terminates the end of a call progress block. The Call Progress Signal Dump command does not return the termination character.

Each call request signal block consists of one or more call progress signals separated by a comma (,) character. The call progress signal consists of two numeric characters.

E.2.8.2 State 07 Exit Conditions. Time-out T2 starts after signaling state 05 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally 20 seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time-out T3A starts after detection of state 07 or state 10 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally two seconds. This timer is reset and restarted after each detection of either state. If the first character in the call progress sequence is a 0, time-out T3B replaces time-out T3A. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time-out T3B starts after detection of state 07 or state 10 and it expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally 60 seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 06A upon reception of two or more SYN characters after it detects a terminating character. The signals in state 06A are as follows:

Next State	State Name	State of Signals	State Set By
06A	DCE Waiting	T = 1 C = On R = SYN I = Off	DCE

The X.21 BCAIM enters state 11 upon reception of a steady-state 1 condition on the R circuit. The signals in state 11 are as follows:

Next State	State Name	State of Signals	State Set By
11	Connection in Progress	T = 1 C = On R = 1 I = Off	DCE

The X.21 BCAIM enters state 12 upon reception of a steady-state 1 condition on the R circuit and a steady-state on condition on the I circuit. The signals in state 12 are as follows:

Next State	State Name	State of Signals	State Set By
12	Ready for Data	T = 1 C = On R = 1 I = On	DCE

E.2.8.3 DTE Termination States Allowed from State 07. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
16	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

E.2.8.4 DCE Termination States Allowed from State 07. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect error codes. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.8.5 Other Error Conditions in State 07.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to transition to state 11, 12, or 19, the character is tossed.

E.2.9 State 08, Incoming Call

In this state, T = 1, C = off, R = BEL, and I = off.

E.2.9.1 State 08 Entry Conditions. The X.21 BCAIM enters state 08 from state 01 when the host issues an Open accept command or when the network establishes a call to provide call charge information. It remains in this state until conditions allow it to enter state 09 or state 15, or until the T0 time-out expires. While in state 08, it receives continuous BEL characters from the network.

E.2.9.2 State 08 Exit Conditions. The X.21 BCAIM enters state 09 when it sets a steady-state on condition on the C circuit. The signals in state 09 are as follows:

Next State	State Name	State of Signals	State Set By
09	Call Accepted	T = 1 C = On R = BEL I = Off	DTE

Time-out T0, is defined as the time period from when the X.21 BCAIM detects the first SYN character until it enters state 08. The X.21 BCAIM enters state 14 when it exceeds this time limit.

State 15 is the call collision state. The X.21 BCAIM enters it by setting a steady-state 0 on the T circuit and a steady-state on condition on the C circuit. The signals in state 15 are as follows:

Next State	State Name	State of Signals	State Set By
15	Call Collision	T = 0 C = On R = BEL I = Off	DTE

E.2.9.3 DTE Termination States Allowed from State 08. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
6	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

E.2.9.4 DCE Termination States Allowed from State 08. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect error codes. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.9.5 Other Error Conditions in State 08.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

- Invalid I Circuit Transition — The X.21 BCAIM's response to reception of an invalid I circuit response is to clear the call.

E.2.10 State 09, Call Accepted
In this state, T = 1, C = on, R = BEL, and I = off.

E.2.10.1 State 09 Entry Conditions. The X.21 BCAIM enters state 09 from state 08 when the host issues an Open accept command or when the network is establishing a call to provide call charge information. It remains in this state until conditions allow it to enter state 06B, 11, or 12 or until the T4 time-out expires. While in this state, it receives continuous BEL characters from the network.

E.2.10.2 State 09 Exit Conditions. Time-out T4 starts after signaling state 09 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally two seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 06B upon reception of two or more SYN characters. The signals in state 06B are as follows:

Next State	State Name	State of Signals	State Set By
06B	DCE Waiting	T = 1 C = On R = SYN I = Off	DCE

The X.21 BCAIM enters state 11 upon reception of a steady-state 1 condition on the R circuit. The signals in state 11 are as follows;

Next State	State Name	State of Signals	State Set By
11	Connection in Progress	T = 1 C = On R = 1 I = Off	DCE

The X.21 BCAIM enters state 12 upon reception of a steady-state 1 condition on the R circuit and a steady-state on condition on the I circuit. The signals in state 12 are as follows:

Next State	State Name	State of Signals	State Set By
12	Ready for Data	T = 1 C = On R = 1 I = On	DCE

E.2.10.3 DTE Termination States Allowed from State 09. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
16	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

E.2.10.4 DCE Termination States Allowed from State 09. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect error codes. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.10.5 Other Error Conditions in State 09.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19 the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19, the character is tossed.

E.2.11 State 10, DCE Provided Information

In this state, T = 1, C = on, R = IA5, and I = off.

E.2.11.1 Entry Conditions for State 10. The X.21 BCAIM enters state 10 from state 06A when the host issues an Open initiate command. The DCE uses this state to transmit DCE-provided information signals to the X.21 BCAIM. It enters the DCE-provided information state upon reception of a valid DCE-provided information starting character from the network. This state is held until conditions allow it to enter state 06A, 11, or 12.

The DCE-provided information sequence consists of one or more DCE-provided information blocks. The first character in each DCE-provided information block is validated against a table to ensure that the information received from the network is DCE-provided information. Refer to the description of word CXDCEI in the discussion of the CECPT in Section 3.

In the Japanese implementation of X.21, the second character in the DCE-provided information block is validated against a table to ensure that the information received from the network is DCE-provided information. Refer to the description of word CXDCEI and to bit 12 in word CXISRF of the CECPT in Section 3. The first character in the DCE-provided information represents the keyboard type identification.

Each DCE-provided information block can be no greater than a total of 128 characters and can have inserted SYN characters. The DCE-provided information dump command does not return inserted SYN characters.

The (+) character terminates the end of a DCE-provided information block. The DCE-provided information dump command does not return the termination character.

Currently, the called line identification block is the only DCE-provided information block defined for X.21 operation. Refer to the specification for the particular network to see if the called line identification option is implemented.

When present, called line identification occurs after the X.21 BCAIM receives all state 07s.

Called line identification blocks begin with a number (#) 2/10 character. Called line identification blocks are separated by a comma (,) character. The following items represent possible called line identification blocks:

#NN +	NN	= National Number
#NTN +	NTN	= Network Terminal Number
##DNIC (+) NTN +	DNIC	= Data Network ID Code
##DCC (+) NN +	DCC	= Data Country Code

Called line identification blocks consist of one or more called line identification signals.

In networks where the destination network does not provide called line identification, the originating network provides a dummy line identification. The dummy line identification consists of two characters, (+ −).

E.2.11.2 Exit Conditions from State 10. Time-out T2 starts after signaling state 05 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally 20 seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time-out T3A is started after detection of state 07 or state 10 and expires if state 12 is not entered. The duration of this timer is normally two seconds. This timer is reset and restarted after each detection of either state. If the first character in the call progress sequence is a 0, time-out T3B replaces time-out T3A. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time-out T3B starts after detection of state 07 or state 10 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally 60 seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 06A upon reception of two or more SYN characters after it detects a terminating character. The signals in state 06A are as follows:

Next State	State Name	State of Signals	State Set By
06A	DCE Waiting	T = 1 C = On R = SYN I = Off	DCE

The X.21 BCAIM enters state 11 upon reception of a steady-state 1 condition on the R circuit. The signals in state 11 are as follows:

Next State	State Name	State of Signals	State Set By
11	Connection in Progress	T = 1 C = On R = 1 I = Off	DCE

The X.21 BCAIM enters state 12 upon reception of a steady-state 1 condition on the R circuit and a steady-state on condition on the I circuit. The signals in state 12 are as follows:

Next State	State Name	State of Signals	State Set By
12	Ready for Data	T = 1 C = On R = 1 I = On	DCE

E.2.11.3 DTE Termination States Allowed from State 10. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
16	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

E.2.11.4 DCE Termination States Allowed from State 10. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect error codes. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.11.5 Other Error Conditions in State 10.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19, the character is tossed.

E.2.12 State 10 BIS, DCE-Provided Information
In this state, T = 1, C = on, R = IA5, and I = off.

E.2.12.1 State 10 BIS Entry Conditions. The X.21 BCAIM enters state 10 BIS from state 06B when the host issues an Open accept command or when the X.21 BCAIM is waiting for the network to provide call charge information. The DCE uses this state to transmit DCE-provided information signals to the X.21 BCAIM. It enters the DCE-provided information state when it receives a valid DCE-provided information starting character from the network. It remains in this state until conditions allow it to enter state 06B, 11, or 12.

The DCE-provided information sequence consists of one or more DCE-provided information blocks. The first character of each DCE-provided information block is validated against a table to ensure that the information received from the network is DCE-provided information. Refer to the description of word CXDCEI in the CECPT discussion in Section 3.

In the Japanese implementation of X.21, the second character in the DCE-provided information block is validated against a table to ensure that the information received from the network is DCE-provided information. Refer to the description of word CXDCEI and bit 12 of word CXISRF of the CECPT in Section 3. The first character in the DCE-provided information represents the keyboard-type identification.

Each DCE-provided information block can be no greater than a total of 128 characters and can have inserted SYN characters. The DCE-provided information dump command returns inserted SYN characters.

The plus (+) character terminates the end of a DCE-provided information block. The DCE-provided information dump command does not return termination characters.

Currently, only the calling line identification block and the charging information block are defined for X.21 operation. Refer to the specification for the particular network to see if either option is implemented.

Calling line identification blocks begin with a number (#), 2/10 character and are separated by a comma (,) character. The following items represent possible calling line identification blocks:

#NN +	NN	= National Number
#NTN +	NTN	= Network Terminal Number
##DNIC (+) NTN +	DNIC	= Data Network ID Code
##DCC (+) NN +	DCC	= Data Country Code

Calling line identification blocks consist of one or more calling line identification signals.

In networks where the originating network does not provide calling line identification, a dummy line identification, or the DNIC number is provided. The dummy line identification consists of two characters (+ −).

A charging information block begins with a slash (/), 2/15 character. This optional information is provided after the X.21 BCAIM completes a call in which charging information is requested. The specification is for the network to establish (within 0.2 seconds after entering state 01) an incoming call to the X.21 BCAIM to provide call charge information. In the X.21 BCAIM implementation this time duration is normally 0.5 seconds.

E.2.12.2 Exit Conditions for State 10 BIS. Time-out T4 starts after signaling state 09 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally two seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 06B upon reception of two or more SYN characters after it detects a terminating character. The signals in state 06B are as follows:

Next State	State Name	State of Signals	State Set By
06B	DCE Waiting	T = 1 C = On R = SYN I = Off	DCE

The X.21 BCAIM enters state 11 upon reception of a steady-state 1 condition on the R circuit. The signals in state 11 are as follows:

Next State	State Name	State of Signals	State Set By
11	Connection in Progress	T = 1 C = On R = 1 I = Off	DCE

The X.21 BCAIM enters state 12 upon reception of a steady state 1 condition on the R circuit and a steady-state on condition on the I circuit. The signals in state 12 are as follows:

Next State	State Name	State of Signals		State Set By
12	Ready for Data	T = 1 R = 1	C = On I = On	DCE

E.2.12.3 DTE Termination States Allowed from State 10 BIS. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals		State Set By
16	DTE Clear Request	T = 0 R = X	C = Off I = X	DTE

E.2.12.4 DCE Termination States Allowed from State 10 BIS. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect errors. The signals in state 19 are as follows:

Next State	State Name	State of Signals		State Set By
19	DCE Clear Request	T = X R = 0	C = X I = Off	DCE

E.2.12.5 Other Error Conditions in State 10 BIS.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 11, 12, or 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 11, 12, or 19, the character is tossed.

E.2.13 State 11, Connection in Progress
In this state, T = 1, C = on, R = 1, and I = off.

E.2.13.1 State 11 Entry Conditions. The X.21 BCAIM enters state 11 from state 05, 06A, 06B, 07, 09, 10, or 10 BIS when the host issues an Open initiate or Open accept command. The DCE uses this state to inform the X.21 BCAIM that a connection is in progress. It remains in state 11 until conditions allow it to enter state 12.

The X.21 BCAIM can enter state 11 in an off-byte boundary. This means that the X.21 BCAIM can receive invalid bytes, with or without correct parity during the transition to this state. The X.21 BCAIM does not report these invalid characters as errors.

E.2.13.2 State 11 Exit Conditions. Time-out T2 starts after signaling state 05 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally 20 seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time-out T3A starts after detection of state 07 or state 10 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally two seconds. It is reset and restarted after each detection of either state. If the first character in the call progress sequence is a 0, time-out T3B replaces time-out T3A. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time-out T3B starts after detection of state 07 or state 10 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally 60 seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time-out T4 starts after signaling state 09 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally two seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 12 upon reception of a steady-state on condition on the I circuit. The signals in state 12 are as follows:

Next State	State Name	State of Signals		State Set By
12	Ready for Data	T = 1 R = 1	C = On I = On	DCE

E.2.13.3 DTE Termination States Allowed from State 11. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals		State Set By
16	DTE Clear Request	T = 0 R = X	C = Off I = X	DTE

E.2.13.4 DCE Termination States Allowed from State 11. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect error codes. The signals in state 19 are as follows:

Next State	State Name	State of Signals		State Set By
19	DCE Clear Request	T = X R = 0	C = X I = Off	DCE

E.2.13.5 Other Error Conditions in State 11.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 12 or 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 12 or 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 12 or 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 12 or 19, the character is tossed.

E.2.14 State 12, Ready for Data

In this state, T = 1, C = on, R = 1, and I = on.

E.2.14.1 State 12 Entry Conditions. The X.21 BCAIM enters state 12 from state 05, 06A, 06B, 07, 09, 10, 10 BIS, or 11 when the host issues an Open initiate or an Open accept command. The DCE uses this state to inform the X.21 BCAIM that a connection is established and that the data transfer state is about to be entered.

The X.21 BCAIM can enter state 12 in an off-byte boundary. This means that the X.21 BCAIM can receive invalid bytes with or without correct parity during the transition to this state. The X.21 BCAIM does not report these invalid characters as errors.

E.2.14.2 State 12 Exit Conditions. Time-out T2 starts after signaling state 05 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally 20 seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time-out T3A starts after detection of state 07 or state 10 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally two seconds. It is reset and restarted after each detection of either state. If the first character in the call progress sequence is a 0, time-out T3B replaces time-out T3A. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time-out T3B starts after detection of state 07 or state 10 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally 60 seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

Time-out T4 starts after signaling state 09 and expires if the X.21 BCAIM does not enter state 12. The duration of this timer is normally two seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 13 after state 12 is detected. The signals in state 13 are as follows:

Next State	State Name	State of Signals	State Set By
13	Data Transfer	T = D C = On R = D I = On	DCE

E.2.14.3 DTE Termination States Allowed from State 12. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
16	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

E.2.14.4 DCE Termination States Allowed from State 12. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect errors. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.14.5 Other Error Conditions in State 12.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

E.2.15 State 13, Data Transfer
In this state, T = D, C = on, R = D, and I = on.

E.2.15.1 State 13 Entry Conditions. The X.21 BCAIM enters state 13 from state 12 when the host issues an Open initiate or Open accept command. In this state, data is transfered from the X.21 BCAIM to a remote site. It remains in state 13 until the host issues a Close command or until it enters state 19. This is the normal open state for switched X.21 operation.

E.2.15.2 State 13 Exit Conditions. The X.21 BCAIM enters state 16 when the host issues a Close command or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals	State Set By
16	DTE Clear Request	T = 0 C = Off R = X I = X	DTE

The X.21 BCAIM enters state 19 when the network or the DCE is terminating the connection. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect error codes. The signals in state 19 are as follows:

Next State	State Name	State of Signals	State Set By
19	DCE Clear Request	T = X C = X R = 0 I = Off	DCE

E.2.16 State 14, DTE Controlled Not Ready, DCE Ready
In this state, T = 1, C = off, R = 1, and I = off.

E.2.16.1 State 14 Entry Conditions. State 14 is the normal closed state of the board. The X.21 BCAIM enters it from state 01 when the X.21 BCAIM is not open and not processing Open commands. It remains in this state until the host issues an Open command, the X.21 BCAIM board is reset, or until it enters state 23.

E.2.16.2 State 14 Exit Conditions. The X.21 BCAIM enters state 01 when it receives an Open command from the host. The signals in state 01 are as follows:

Next State	State Name	State of Signals	State Set By
01	Ready	T = 1 C = Off R = 1 I = Off	DTE

The X.21 BCAIM enters state 23 after the network signals a steady-state 0 on the R circuit with a steady-state off on the I circuit. The signals in state 23 are as follows:

Next State	State Name	State of Signals	State Set By
23	DTE C/NR DCE NR	T = 01 C = Off R = 0 I = Off	DCE

E.2.17 State 15, Call Collision
In this state, T = 0, C = on, R = BEL, and I = off.

E.2.17.1 State 15 Entry Conditions. The X.21 BCAIM enters state 15 from state 02 or state 08 when the host issues an Open initiate command. The DCE uses this state to inform the X.21 BCAIM that a call collision has taken place and to proceed with the X.21 call. State 15 is held until conditions allow the X.21 BCAIM to enter state 03. During this state, it receives continuous BEL characters from the network.

E.2.17.2 State 15 Exit Conditions. Time-out T1 starts after signaling state 02 and expires if the X.21 BCAIM does not enter state 03. The duration of this timer is normally three seconds. The X.21 BCAIM enters state 16 when it exceeds this time limit.

The X.21 BCAIM enters state 03 after a (+) character is detected on the R circuit. The signals in state 03 are as follows:

Next State	State Name	State of Signals		State Set By
03	Proceed to Select	T = 0 R = +	C = On I = Off	DCE

E.2.17.3 DTE Termination States Allowed from State 15. The X.21 BCAIM enters state 16 when the host issues an abort with an Open pending or when an error occurs that causes the X.21 BCAIM to close the channel. The signals in state 16 are as follows:

Next State	State Name	State of Signals		State Set By
16	DTE Clear Request	T = 0 R = X	C = Off I = X	DTE

E.2.17.4 DCE Termination States Allowed from State 15. The X.21 BCAIM enters state 19 when the network or the DCE is terminating the call. This state causes the X.21 BCAIM to terminate all outstanding requests and report disconnect error codes. The signals in state 19 are as follows:

Next State	State Name	State of Signals		State Set By
19	DCE Clear Request	T = X R = 0	C = X I = Off	DCE

E.2.17.5 Other Error Conditions in State 15.

- Even Character Parity Detected — The X.21 BCAIM's response to reception of a character with even parity depends on several factors. If the character is garbled and not due to transition to state 19, it is processed as specified by bit 7 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

- Invalid Character — The X.21 BCAIM's response to reception of an invalid character depends on several factors. If the character is garbled and not due to transition to state 19, it is processed as specified by bit 11 of the word CXISRF in the CECPT. If the error is due to the transition to state 19, the character is tossed.

E.2.18 State 16, DTE Clear Request
This is the DTE clearing state. In this state, T = 0, C = off, R = X, and I = X.

E.2.18.1 State 16 Entry Conditions. The X.21 BCAIM enters state 16 from any state other than state 01 or a quiescent state. It enters this state when the host issues a Close request or when it senses a condition that requires the board to close. In this state, any outstanding requests are returned to the host with a disconnect error code. It remains in this state until conditions allow it to enter state 17 or until time-out T5 expires.

During this state, there is the possibility of a clear collision occurring. A clear collision occurs when both the DCE and DTE signals clear during the same time interval. It is possible for the DTE to fail to detect state 17. If time-out T5 expires, the X.21 BCAIM enters state 18.

E.2.18.2 State 16 Exit Conditions. Time-out T5 starts after signaling state 16 and expires if the X.21 BCAIM does not enter state 21. The duration of this timer is normally two seconds. The X.21 BCAIM enters state 18 when it exceeds this time limit.

The X.21 BCAIM enters state 17 after the network signals a steady-state 0 on the R circuit with a steady-state off on the I circuit. The signals in state 17 are as follows:

Next State	State Name	State of Signals	State Set By
17	DCE Clear Confirmation	T = 0 C = Off R = 0 I = Off	DCE

E.2.19 State 17, DCE Clear Confirmation
This is the DCE clearing state. In this state, T = 0, C = off, R = 0, and I = off.

E.2.19.1 State 17 Entry Conditions. The X.21 BCAIM enters this state from state 16 when the host issues a Close request or when the X.21 BCAIM senses a condition that requires the board to close. This state is held until conditions allow it to enter state 21 or until time-out T5 expires.

E.2.19.2 State 17 Exit Conditions. Time-out T5 starts after signaling state 16 and expires if the X.21 BCAIM does not enter state 21. The duration of this timer is normally two seconds. The X.21 BCAIM enters state 18 when it exceeds this time limit.

The X.21 BCAIM enters state 21 after the network signals a steady-state 1 on the R circuit. The signals in state 21 are as follows:

Next State	State Name	State of Signals	State Set By
21	DCE Ready	T = 0 C = Off R = 1 I = Off	DCE

E.2.20 State 18, DTE Ready, DCE Not Ready
State 18 is a quiescent state. In this state, T = 1, C = off, R = 0, and I = off.

E.2.20.1 State 18 Entry Conditions. The X.21 BCAIM enters state 18 from state 01 when the DCE goes not ready, or from states 17 and 20 if the T5 or T6 time-out occurs. When it enters from state 01, this state is held the minimum required duration and then it enters state 22. Entering this state forces the X.21 BCAIM to terminate any outstanding I/O requests and report disconnect error codes to the host.

E.2.20.2 State 18 Exit Conditions. The X.21 BCAIM enters state 22 after it signals a steady-state 0 on the T circuit. It enters this state when an Open command times out and the DCE has not signaled DCE ready, or when an error condition causes the X.21 BCAIM to abort the Open command and close the channel. The signals in state 22 are as follows:

Next State	State Name	State of Signals		State Set By
22	DTE U/NR DCE NR	T = 0 R = 0	C = Off I = Off	DTE

E.2.21 State 19, DCE Clear Indication
This is a DCE clearing state. In this state, T = X, C = X, R = 0, and I = off.

E.2.21.1 State 19 Entry Conditions. The X.21 BCAIM enters state 19 from any nonquiescent state or from any state other than state 01. Entry into this state occurs when the DCE goes not ready anytime the X.21 BCAIM is not in a quiescent state or in state 01. When the X.21 BCAIM detects this state, it enters state 20. Entering this state forces the X.21 BCAIM to terminate any outstanding I/O requests and report disconnect error codes to the host.

E.2.21.2 State 19 Exit Conditions. The X.21 BCAIM enters state 20 after it signals a steady-state 0 on the T circuit and a steady-state off on the C circuit. The signals in state 20 are as follows:

Next State	State Name	State of Signals		State Set By
20	DTE Clear Confirmation	T = 0 R = 0	C = Off I = Off	DTE

E.2.22 State 20, DTE Clear Confirmation
This is the DTE clearing state. In this state, T = 0, C = off, R = 0, and I = off.

E.2.22.1 State 20 Entry Conditions. The X.21 BCAIM enters state 20 from state 19 due to the network clearing a connection or a call in progress. It remains in this state until the network signals state 21 or the T6 time-out expires.

E.2.22.2 State 20 Exit Conditions. Time-out T6 starts after detection of state 20 and expires if the X.21 BCAIM does not enter state 21. The duration of this timer is normally two seconds. The X.21 BCAIM enters state 18 when it exceeds this time limit.

The X.21 BCAIM enters state 21 after the network signals a steady-state 1 on the R circuit. The signals in state 21 are as follows:

Next State	State Name	State of Signals		State Set By
21	DCE Ready	T = 0 R = 1	C = Off I = Off	DCE

E.2.23 State 21, DCE Ready

In this state, T = 0, C = off, R = 1, and I = off.

E.2.23.1 State 21 Entry Conditions. The X.21 BCAIM enters state 21 from states 17 or 20 when the host issues a Close request, when it senses a condition that requires the board to close, or when the network clears a connection or a call in progress. This state is held until conditions allow it to enter state 01 or until the T5 or T6 timers expire.

E.2.23.2 State 21 Exit Conditions. Time-out T5 starts after signaling state 16 and expires if the X.21 BCAIM does not enter state 21. The duration of this timer is normally two seconds. The X.21 BCAIM enters state 18 when it exceeds this time limit.

Time-out T6 starts when state 20 is detected and expires if the X.21 BCAIM does not enter state 21. The duration of this timer is normally two seconds. The X.21 BCAIM enters state 18 when it exceeds this time limit.

The X.21 BCAIM enters state 01 after it signals a steady-state 1 on the C circuit. The signals in state 01 are as follows:

Next State	State Name	State of Signals		State Set By
01	Ready	T = 1	C = Off	DTE
		R = 1	I = Off	

E.2.24 State 22, DTE Uncontrolled Not Ready, DCE Ready

In this state, T = 0, C = off, R = 1, and I = off.

E.2.24.1 State 22 Entry Conditions. The X.21 BCAIM enters state 22 from state 18 or when it successfully completes reset processing and detects that the DCE is not ready. It remains in this state until the network enters state 24. Open channel requests issued by the host during this state cause the Open command to be returned with error.

E.2.24.2 State 22 Exit Conditions. The X.21 BCAIM enters state 24 when the network signals a steady-state 1 condition on the R circuit. The signals in state 24 are as follows:

Next State	State Name	State of Signals		State Set By
24	DTE U/NR	T = 0	C = Off	DTE
	DCE R	R = 1	I = Off	

E.2.25 State 23, DTE Controlled Not Ready, DCE Not Ready

In this state, T = 1, C = off, R = 0, and I = off.

E.2.25.1 State 23 Entry Conditions. The X.21 BCAIM enters state 23 from state 14 when it is in a normal closed state and the DCE signals not ready. It remains in this state the minimum required duration before entering state 22.

E.2.25.2 State 23 Exit Conditions. The X.21 BCAIM enters state 22 when it signals a steady state 0 on the T circuit. The signals in state 22 are as follows:

Next State	State Name	State of Signals		State Set By
22	DTE U/NR DCE NR	T = 0 R = 0	C = Off I = Off	DCE

E.2.26 State 24, DTE Uncontrolled Not Ready, DCE Ready
In this state, T = 0, C = off, R = 0, and I = off.

E.2.26.1 State 24 Entry Conditions. The X.21 BCAIM enters state 24 from states 01 or 22, or when it has successfully completed reset processing and finds the DCE ready. It remains in this state the minimum required duration before entering state 01.

E.2.26.2 State 24 Exit Conditions. The X.21 BCAIM enters state 01 when it signals a steady-state 1 on the T circuit. The signals in state 01 are as follows:

Next State	State Name	State of Signals		State Set By
01	Ready	T = 1 R = 1	C = Off I = Off	DTE
22	DTE U/NR DCE NR	T = 0, R = 0	C = Off I = Off	DCE

Appendix F

X.21 Leased Line State Flow

F.1 GENERAL

The protocol for handling calls on a X.21 leased line requires the DTE and DCE to go through a number of different states to originate, connect, and disconnect calls. The states involved fall into the following major groups:

- Quiescent states
- Data transfer states

This appendix describes the conditions necessary for entry into and exit from each state, DTE and DCE termination states allowed in each state, and error conditions that are applicable to each state for operation of the X.21 BCAIM on X.21 leased lines.

Figures F-2 and F-3 illustrate the flow within each group of states. Figure F-1 is a legend for the other illustrations. Each block in Figures F2 and F-3 contains the state number, the state name, and the state of the signals on the following circuits:

Transmit (T)
Receive (R)
Control (C)
Indication (I)

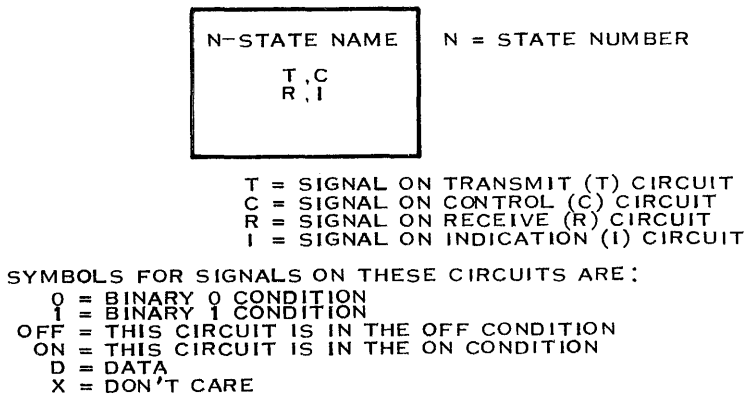
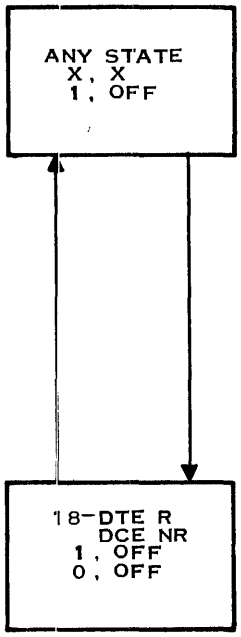


Figure F-1. X.21 Leased Line Flowchart Symbols



NOTE

STATE 01 OR 18 IS THE NORMAL CLOSED STATE OF THE BOARD

2283262

Figure F-2. X.21 Leased Line Quiescent or Clearing States Flowchart

F.2 STATE DESCRIPTIONS

The state descriptions in the following paragraphs are closely tied to the flowcharts in Figures E-2 through E-5.

F.2.1 State 01, Ready

In this state, T = 1, C = off, R = 1, and I = off.

F.2.1.1 State 01 Entry Conditions. The X.21 BCAIM enters state 01 from state 18. This state is the normal quiescent open state for the X.21 BCAIM in leased line operation. Open commands are reported back as successful when the X.21 BCAIM enters this state and becomes stable. Refer to word CXOPNT of the CECPT in Section 3 for more information.

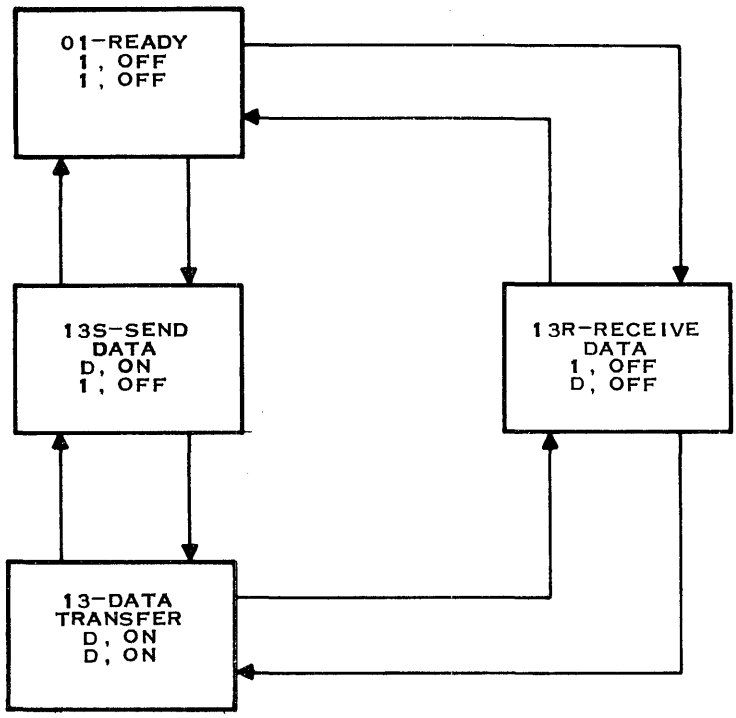


Figure F-3. X.21 Leased Line Data Transfer States Flowchart

F.2.1.2 State 01 Exit Conditions. The X.21 BCAIM enters the receive data state (state 13R) from state 01 whether any read commands are active on the X.21 BCAIM or not. The network signals the receive data state with a steady-state on condition on the I circuit. The signals in state 13R are as follows:

Next State	State Name	State of Signals	State Set By
13R	Receive Data	T = 1 C = Off R = D I = On	DCE

The X.21 BCAIM enters the send data state (state 13S) from state 01 when the host issues an Open command with continuous carrier. The X.21 BCAIM signals the send data state with a steady-state on condition on the C circuit and data transmission on the T circuit. The signals in state 13S are as follows:

Next State	State Name	State of Signals	State Set By
13S	Send Data	T = D C = On R = 1 I = Off	DTE

F.2.1.3 DCE Termination States Allowed from State 01. The X.21 BCAIM enters state 18 from state 01 when neither the network nor the DCE is able to maintain a useable connection. The signals in state 18 are as follows:

Next State	State Name	State of Signals		State Set By
18	DTE Ready DCE Not Ready	T = 1 R = 0	C = Off I = Off	DCE

F.2.2 State 13, Data Transfer
In this state, T = D, C = on, R = D, and I = on.

F.2.2.1 State 13 Entry Conditions. The X.21 BCAIM enters state 13 from state 13R or 13S if it is ready to transmit data and finds the network already transmitting data. This state transfers data between the X.21 BCAIM and a remote site. State 13 is held until the Write command completes and continuous carrier is not specified in the DTCPT, until the host issues a Close Channel command, or until the X.21 BCAIM enters state 19.

F.2.2.2 State 13 Exit Conditions. The X.21 BCAIM enters state 13R from state 13 when it has no transmit commands active and continuous carrier is not specified. The X.21 BCAIM signals the receive data state with a steady-state 1 condition on the T circuit and a steady-state off condition on the I circuit. The signals in state 13R are as follows:

Next State	State Name	State of Signals		State Set By
13R	Receive Data	T = 1 R = D	C = Off I = On	DTE

The X.21 BCAIM enters state 13S from state 13 when the network signals with a steady-state 1 condition on the R circuit and a steady-state off condition on the I circuit.

Next State	State Name	State of Signals		State Set By
13S	Send Data	T = D R = 1	C = On I = Off	DCE

F.2.2.3 DTE Termination States Allowed from State 13. The X.21 BCAIM enters state 01 when it is issued a Close command or when it detects an error which forces a Close to be processed. All I/O commands except the Close return to the host with a disconnected error code. The signals in state 01 are as follows:

Next State	State Name	State of Signals		State Set By
01	DTE Clear Request	T = 1 R = 1	C = On I = On	DTE

F.2.2.4 DCE Termination States Allowed from State 13. The X.21 BCAIM enters state 18 when neither the network nor the DCE is able to maintain a useable connection. All I/O commands return to the host with a disconnected error code. The signals in state 18 are as follows:

Next State	State Name	State of Signals	State Set By
18	DTE Ready DCE Not Ready	T = X C = X R = 0 I = Off	DCE

F.2.3 State 13R, Receive Data
In this state, T = 1, C = off, R = D, and I = on.

F.2.3.1 State 13R Entry Conditions. The X.21 BCAIM enters state 13R from state 01 or 13 when the network is transmitting data. This state receives data from a remote site. State 13R is held until the host issues a Write command, until the network finishes transmission, until the host issues a Close command, or until the X.21 BCAIM enters state 19.

F.2.3.2 State 13R Exit Conditions. State 01 is entered when the network signals the ready state by placing a steady-state 1 condition on the R circuit and a steady-state off condition on the I circuit. The signals in state 01 are as follows:

Next State	State Name	State of Signals	State Set By
01	Ready	T = 1 C = Off R = 1 I = Off	DCE

The X.21 BCAIM enters state 13 when the X.21 BCAIM is ready to process transmit commands from the host. The X.21 BCAIM signals the data transfer state by placing data on the T circuit and a steady-state on condition on the C circuit. The signals in state 13 are as follows:

Next State	State Name	State of Signals	State Set By
13	Data Transfer	T = D C = On R = D I = On	DTE

F.2.3.3 DTE Termination States Allowed from State 13R. The X.21 BCAIM enters state 01 when it is issued a Close command or when it detects an error that forces a Close to be processed. All I/O commands except the Close command return with a disconnected error code. The signals in state 01 are as follows:

Next State	State Name	State of Signals	State Set By
01	DTE Clear Request	T = 1 C = Off R = 1 I = Off	DTE

F.2.3.4 DCE Termination States Allowed from State 13R. The X.21 BCAIM enters state 18 when neither the network nor the DCE is able to maintain a useable connection. All I/O commands return with a disconnected error code. The signals in state 18 are as follows:

Next State	State Name	State of Signals		State Set By
18	DTE Ready DCE Not Ready	T = X R = 0	C = X I = Off	DCE

F.2.4 State 13S, Send Data
In this state, T = D, C = on, R = 1, and I = off.

F.2.4.1 State 13S Entry Conditions. The X.21 BCAIM enters state 13S from states 01 or 13 when the network is receiving data. This state transmits data to a remote site. State 13 is held until the network begins to send data to the X.21 BCAIM, until the X.21 BCAIM completes all Write commands and continuous carrier is not specified, until the host issues a Close command, or until it enters state 19.

F.2.4.2 State 13S Exit Conditions. The X.21 BCAIM enters state 01 (the ready state) when it signals a steady-state 1 condition on the T circuit and a steady-state off condition on the C circuit. The signals in state 01 are as follows:

Next State	State Name	State of Signals		State Set By
01	Ready	T = 1 R = 1	C = Off I = Off	DTE

The network signals entry into state 13 with data on the R circuit and a steady-state on condition on the I circuit. The signals in state 13 are as follows:

Next State	State Name	State of Signals		State Set By
13	Data Transfer	T = D R = D	C = On I = On	DCE

F.2.4.3 DTE Termination States Allowed from State 13S. The X.21 BCAIM enters state 01 when the host issues a Close command or when it detects an error that forces a Close command to be processed. All I/O commands except the Close command return with a disconnected error code. The signals in state 01 are as follows:

Next State	State Name	State of Signals		State Set By
01	Ready	T = 1 R = 1	C = Off I = Off	DTE

F.2.4.4 DCE Termination States Allowed from State 13S. The X.21 BCAIM enters state 18 when neither the network nor the DCE is able to maintain a useable connection. All I/O commands return with a disconnected error. The signals in state 18 are as follows:

Next State	State Name	State of Signals	State Set By
18	DTE R DCE N/R	T = X C = X R = 0 I = Off	DCE

F.2.5 State 18, DTE Ready, DCE Not Ready
In this state, T = 1, C = off, R = 0, and I = off.

F.2.5.1 State 18 Entry Conditions. The X.21 BCAIM enters state 18 from state 01, 13, 13R, or 13S when the DCE goes not ready. When it enters from state 01, state 18 is held until it reenters state 01. Entry into state 18 forces the X.21 BCAIM to return all outstanding I/O requests to the host with a disconnected error code and to process a Close.

F.2.5.2 State 18 Exit Conditions. The X.21 BCAIM enters state 01 after the network signals a steady-state 1 on the R circuit. The signals in state 01 are as follows:

Next State	State Name	State of Signals	State Set By
01	Ready	T = 1 C = Off R = 1 I = Off	DCE

Alphabetical Index

Introduction

HOW TO USE INDEX

The index, table of contents, list of illustrations, and list of tables are used in conjunction to obtain the location of the desired subject. Once the subject or topic has been located in the index, use the appropriate paragraph number, figure number, or table number to obtain the corresponding page number from the table of contents, list of illustrations, or list of tables.

INDEX ENTRIES

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections — Reference to Sections of the manual appear as "Sections x" with the symbol x representing any numeric quantity.

- Appendixes — Reference to Appendixes of the manual appear as "Appendix y" with the symbol y representing any capital letter.

- Paragraphs — Reference to paragraphs of the manual appear as a series of alphanumeric or numeric characters punctuated with decimal points. Only the first character of the string may be a letter; all subsequent characters are numbers. The first character refers to the section or appendix of the manual in which the paragraph may be found.

- Tables — References to tables in the manual are represented by the capital letter T followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the table). The second character is followed by a dash (-) and a number.

  Tx-yy

- Figures — References to figures in the manual are represented by the capital letter F followed immediately by another alphanumeric character (representing the section or appendix of the manual containing the figure). The second character is followed by a dash (-) and a number.

  Fx-yy

- Other entries in the Index — References to other entries in the index preceded by the word "See" followed by the referenced entry.

USER'S RESPONSE SHEET

Manual Title: Model 990 Computer X.21 Bit-Oriented/Character-Oriented/Asynchronous Interface Module (X.21 BCAIM) Installation and Operation Manual (2263883-9701)

Manual Date: 1 October 1982 **Date of This Letter:** _____

User's Name: _____ **Telephone:** _____

Company: _____ **Office/Department:** _____

Street Address: _____

City/State/Zip Code: _____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

CUT ALONG LINE

Location in Manual	Comment/Suggestion
_____	_____
	_____
	_____
	_____
_____	_____
	_____
	_____
	_____
_____	_____
	_____
	_____
	_____

NO POSTAGE NECESSARY IF MAILED IN U.S.A.
FOLD ON TWO LINES (LOCATED ON REVERSE SIDE), TAPE AND MAIL

FOLD

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 7284 DALLAS, TX

POSTAGE WILL BE PAID BY ADDRESSEE

TEXAS INSTRUMENTS INCORPORATED
DIGITAL SYSTEMS GROUP

ATTN: TECHNICAL PUBLICATIONS
P.O. Box 2909 M/S 2146
Austin, Texas 78769

FOLD

TEXAS INSTRUMENTS
INCORPORATED
DIGITAL SYSTEMS GROUP
POST OFFICE BOX 2909 AUSTIN, TEXAS