SuperTAP™ Advanced Development Tool for Intel Architectures

For Intel386™EX Processor

Highlights

- Industry's most portable, and versatile in-circuit tool:
  – Software development and test
  – Hardware design and debug
  – Integration
  – Manufacturing Test
  – Field Service
- For software development, SuperTAP is better than a monitor or ROM Emulator:
  – Provides communications path between target and host debugger *without* using target resources
  – Provides run control over the execution of code
  – Provides fast code downloads
  – Provides read/write access to registers and memory
  – Provides both hardware and software breakpoints
  – Real-time view and control of code execution history
  – Visibility of events (bus cycle and code conditions)
  – Ability to map memory address space
  – Works on stable or unstable systems
  – Ability to revive system after software crash
  – Extensive macro language automates debugging
  – Null target mode allows code development without a target system
- For hardware design and integration, SuperTAP's advanced emulation features fit in a hand-held package:
  – Real-Time emulation to 33 MHz
  – Selectable 3- or 5-volt operation
  – Support for *all* i386EX modes and memory models
  – 64K frame trace buffer with timestamp
  – Trace pre-qualification, positioning and post-filtering
  – Advanced, GUI State-Machine Event System
  – Non-Stop Emulation (NSE™) Trace System
  – Non-Stop Emulation (NSE) Event System
  – Overlay Memory substitution for RAM and ROM
  – Versatile communications include 115KBaud RS232 and High-Speed RS422
  – ONCE™ mode support
  – Complete i386EX PQFP and TQFP adapter support

SuperTAP™—Price and Performance

In the tradition of CodeTAP®, SuperTAP was designed with advanced technology to give embedded engineers all the debugging functions they use most, such as software and hardware breakpoints and modification of memory and processor registers.

As Applied's third generation CodeTAP, SuperTAP sets a new standard in emulation, adding high-performance features such as a real-time 64K deep trace buffer (including address, data, processor status, and timestamp), target monitoring, selectable triggering, extended overlay memory and communications—all in an affordable, small-footprint device.

With support for popular compilers and hosts, SuperTAP fits easily into your environment. And thanks to its low cost, you can increase tool availability, boost the whole team's productivity, and reduce time to market.

Applied Microsystems Corporation

Patented Emulation Technology

Applied invented CodeTAP emulation technology (U.S. Patent No. 5,228,039) to provide low-cost visibility and control for executing and debugging code.

In the CodeTAP tradition, SuperTAP fits in your pocket and is affordable. However, SuperTAP's extended features compare to traditional high-end ICEs and will appeal to software and hardware developers alike.

Behind the tool is a dual processor architecture that guarantees real-time operation, provides fast code downloads and trace uploads. You get the benefit of advanced technology you won't find in look-alike devices.

The bottom line? We think you'll agree—SuperTAP is the best tool in the industry for i386EX debugging.

More Than a Development Tool

SuperTAP offers value that goes beyond the development and debug phases. A complete C macro language lets you automate complex test scripts. SuperTAP's portable size and communications make it quick and easy to use in the field as well as around the office. Clip-on adapters make production line testing go more quickly. And Performance Analysis, using Applied's unique CodeTEST product, provides unsurpassed embedded software testing capabilities.

Non-Stop Emulation (NSE™)

SuperTAP was designed to support real-time critical applications. SuperTAP offers NSE trace and event subsystems that can be utilized with the target running or paused. SuperTAP also offers fast peek/poke to memory and registers.

NSE™ Trace Subsystem

A 64K deep x 80-bit wide real-time trace buffer helps you locate bugs by providing a history of microprocessor events. On each bus cycle, SuperTAP captures everything you need to track data movement and program execution flow. Captured information includes address, data, processor status, and timestamp.

SuperTAP's NSE (Non-Stop Emulation) feature means you can upload, view and trigger trace without stopping the target processor. Executed code is displayed in assembly and C-source with symbols or raw bus cycles. The trace buffer includes the capability to search for bus cycles containing any combination of address, data, and processor status information to speed analysis.

Triggering trace is easy: SuperTAP offers pre-, post- and center- triggering capabilities.

Trace information can be pre-qualified through SuperTAP's Event Subsystem, so you capture only the information you want to see. You can also use built-in Logic State Analysis, which tracks external signals, to qualify events. Timestamp provides accurate event timing, from 25 ns to 8 hours.

Breakpoint Subsystem

Extensive breakpoints work together with the Event System to facilitate code and hardware testing and analysis. You can set breakpoints in your source code symbolically, by specifying function or variable names, or you can just point and click.

You can detect a variety of events using software breakpoints, hardware access breakpoints, and hardware execution breakpoints. Hardware execution breakpoints break immediately before an instruction executes. They prevent false triggering due to pre-fetching. Unlike software breakpoints, hardware execution breakpoints work in ROM as well as RAM.

Hardware access breakpoints can trigger on address, data value, and cycle type. Cycle types include read, write, I/O, DMA, interrupt-acknowledge, and pre-fetch.

NSE™ Event Subsystem

The Event system dramatically simplifies debugging of obscure or intermittent problems. Sixteen comparators and four trigger levels let you define complex, nested conditions to qualify breakpoints or trace. Forward and backward branching among trigger levels allows repetitive capture of isolated events in trace. SuperTAP's Event System provides you the ability to define up to eight active bus events at the same time to troubleshoot a complex condition. Two 32-bit event counters provide passcount information for triggers.

Furthermore, SuperTAP's NSE capability allows you to modify your triggers without stopping the target processor. Triggers include address match, address range, data match, data range, and bus cycle (read/write, halt, I/O, interrupt, DMA). Event actions include break emulation, change trigger level, count, assert trigger out, and Trace control.

Overlay Memory Subsystem

For convenient debugging of target PROM and RAM, you can map up to 1 MB of overlay memory to target addresses with an unlimited number of 4K blocks. 4 MB and 8 MB options are available. At full processor speed, overlay requires no wait states. And because overlay memory is based on addresses, it doesn't require chip selects.

Map address space is automatically generated by a .MAP file. Attributes include target read/write, read-only or neither, and overlay read/write or guarded. Guarded memory instantly detects corrupted pointers.

High-Speed Communications

In addition to high-speed RS-232 serial communications, SuperTAP supports high-speed RS-422 serial communications with actual transfer rates up to 7 MByte/min. For example, a 256K file downloads in just two seconds. These significantly shortened download times mean substantial productivity gains.

Hardware Diagnostics

Testing hardware integrity is simplified with stand-alone mode. In this mode, SuperTAP behaves just like a bare processor, eliminating the need to remove and replace chips for testing.

SuperTAP also lets you continue to communicate with and troubleshoot your target under conditions that cause other tools to crash. A second processor continuously monitors the emulation processor for RESET, HOLD, READY, Vcc, clock, and hung bus cycles. If anything goes wrong, SuperTAP not only will help you recover from the condition, but tell you why it happened.

Performance Analysis

For the most powerful software measurements, team SuperTAP with CodeTEST software verification tools. Combined, SuperTAP and CodeTEST become the ultimate embedded development platform, and are a must for industries requiring proof of compliance to specification such as in aerospace or medical fields. For commercial high volume product
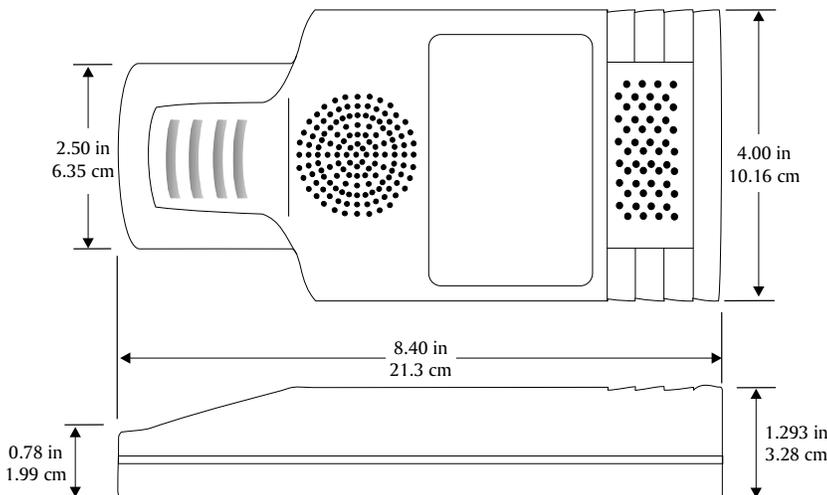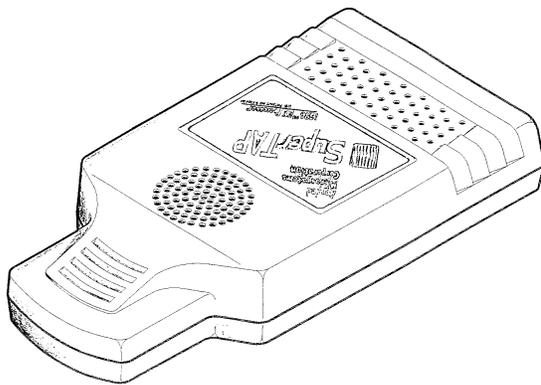

CodeTEST Software Verification Tools bring a new dimension to software test and verification.

development, SuperTAP and CodeTEST can reduce the chance and expense of product recalls.

CodeTEST provides Performance Analysis—including function and task execution times as well as call-pair views—Coverage Analysis, Memory Allocation Analysis and Extended Trace Analysis—all non-sampled, all while the target runs in real time.

For more information about CodeTEST, refer to the CodeTEST data sheet.

Industry Leading Debugger

Applied has partnered with leaders in the industry to ensure your SuperTAP is part of a complete, integrated environment.

SuperTAP comes complete with debugger as well as cross-linker/locator tools to support the outputs of most leading X86 compilers.

For more information about SuperTAP's debugger, supported host operating systems, and user interface, see the SuperTAP debugger specification sheets.

2.50 in
6.35 cm

4.00 in
10.16 cm

8.40 in
21.3 cm

0.78 in
1.99 cm

1.293 in
3.28 cm

Dimensions of the SuperTAP Advanced Development Tool.

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Distributors and Representatives located worldwide.
For the nearest location, call 1-800-426-3925 or (206) 882-2000

CAD-UL® XDB High Level Language Debugger
For the SuperTAP™ Advanced Development Tool

A Complete, Integrated Toolchain Environment

XDB from CAD-UL offers full support of 16-bit and 32-bit Intel architectures on PC and Sun hosts. Support of CPU protection mechanisms are provided by supplying flat and segmented memory models and subsystems.

Asynchronous memory access during emulation provides dynamic control that makes it much easier to debug real-time critical software.

XDB debugger is packaged with the LINK386 linker/locator system which supports allocation of descriptor tables, multitasking models, GATE definitions, absolute linkable and relocatable (loadable) code, and supports standard object formats.

Customized for SuperTAP

All of SuperTAP's features have graphical window displays and easy point-and-click access through the interface including Trace, Event and Breakpoint system and Overlay. XDB is available for 16-bit and 32-bit development and comes complete with locator that provides interoperability for a variety of compilers including CAD-UL, Borland, Intel, Microsoft, Metaware, Watcom and other compilers that generate OMF symbolic format.

SuperTAP facilitiates debugging by providing complete i386EX register information. Field definitions and online help are provided for all registers. Bit modifications are enabled with convenient point and click access.
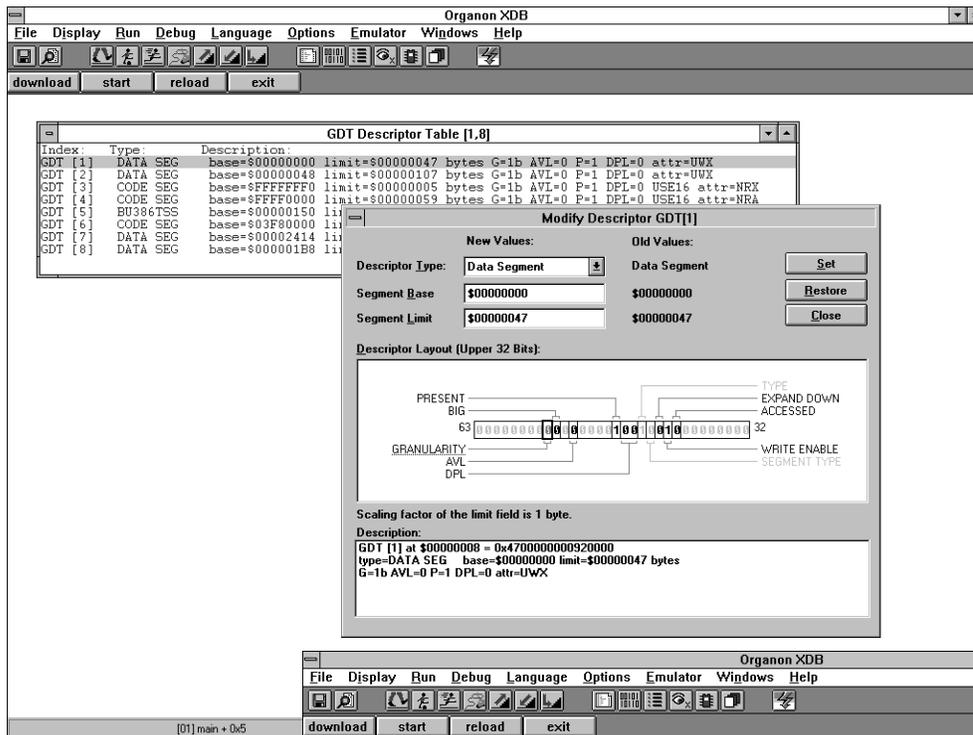
SuperTAP offers complete C/C++ debugging with high-level, assembly, and bus cycle display options. Trace is 64K deep, recording data values, execution, and timestamp.

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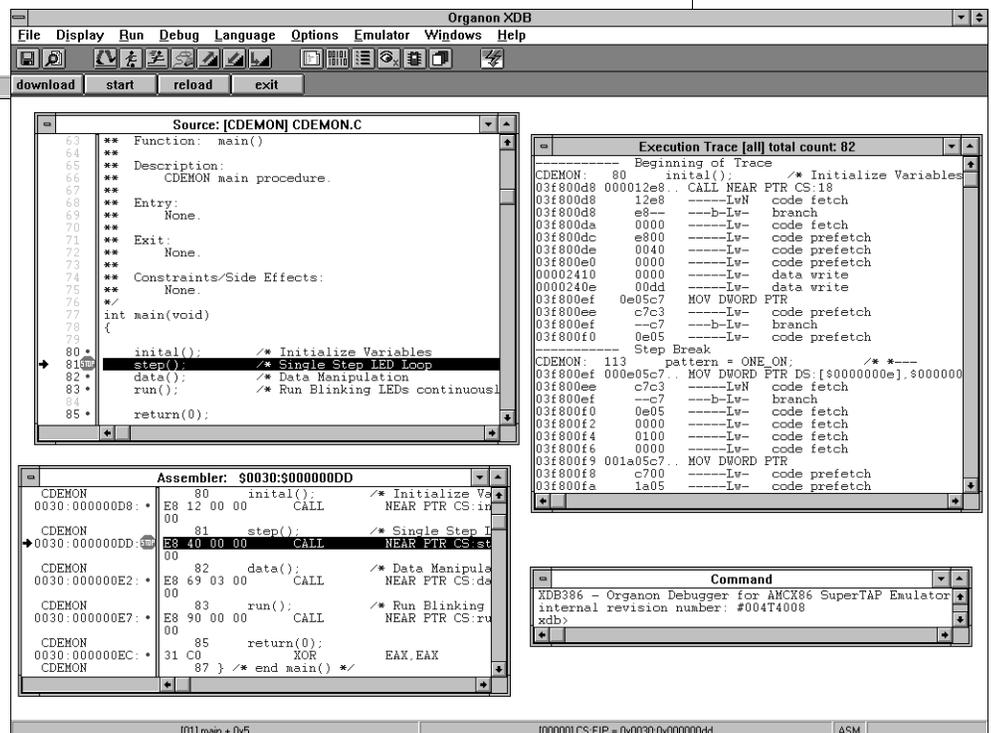
SuperTAP™ Advanced Development Tool
for the Intel386™EX CPU with CAD-UL® XDB

Microprocessors Supported
Intel i386EX CPU (all modes)

Speed
To 33 MHz
3–5 volt operation at any speed

Packages Supported
PQFP (132-pin) clip-on
TQFP 144-pin solder-down
PQFP 132-pin solder-down

Communications
RS-232C host serial port (115K baud)
RS-422 serial interface (7 MByte/min)
(Both included in standard configuration)

SuperTAP Debugger and Hosts
CAD-UL XDB
Windows 3.11 / Windows 95/ Windows
  NT / OS/2 compatible
OSF-Motif, Sun-OS
(All X86 modes & models supported)

Included With Debugger
CAD-UL LINK386 linker/locator

Complete Integrated Toolchain
Add CAD-UL IDE Compiler, Assembler,
  Linker and Libraries for a complete,
  integrated toolchain
Compatible with SSI linker and locator
  and Phar Lap linc/loc (C support only;
  sold separately)

Memory Model Support
Flat, Small, Small ROM, Compact, Large

Macro Language
Full C-like expression language

Compilers Supported
CAD-UL C/C++ Compiler
CO386
Intel ASM-286/386
Intel PL/M-286/386
Intel iC-286/386
Microsoft C/C++
Borland C/C++
MetaWare High C
Watcom C/C++
Other compilers that generate OMF386
  symbolic format

Language Support
Assembler
C
C++
PLM

Performance Analysis
Timestamp with scalable resolution

Overlay Memory
1 MB zero wait state to 33 MHz
4 MB, 8 MB optional
Unlimited number of 4K blocks
Attributes: target or overlay,
  read/write, read-only or guarded.

Trace Subsystem
Featuring NSE™
64K deep X 80-bit wide real-time trace
  history including 20 address bits, 16
  data bits, 4 execution bits, and
  timestamp
Display executed code in assembly and
  C-source with symbols or raw
  bus cycles
Trigger trace upon events
View dynamic trace display without
  stopping emulation
Record DMA cycles
Timestamp with from 25 ns to 8 hours

Event and Breakpoint Subsystem
Featuring NSE™ dynamic triggering
Unlimited software execution breakpoints
Hardware resources include:
  8 hardware *execution* breakpoints
  8 address access breakpoints
  7 data access breakpoints
  Two 32-bit counters
Four trigger levels
Up to 8 inputs in one level
Up to 8 active bus events at one time
Triggering:
  Address match
  Address range
  Data match
  Data range
  Bus cycle (read, write, halt, I/O,
    interrupt, DMA)
  PINSTATE (INT 0–6, TIMERIN,
    TIMEROUT)
Event actions
  Break emulation
  Change trigger level
  Count
  Assert trigger out
  Trace one cycle/trace on/trace off

Target Diagnostics
Monitor target Vcc, RESET, HOLD, and
  READY
Monitor target clock
Monitor bus timeout

Power Requirements
Powered from external supply
Input power 115 VAC, 47 Hz–63 Hz or
  230 VAC, 47 Hz–63 Hz

Physical Specifications
Dimensions (LHW): 8.4 x 1.24 x 4.0"
  (21.43 x 3.17 x 10.16 cm)
Ambient humidity: 0–90% non-
  condensing
Operating temperature: 32–104° F
  (0–40° C)

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