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K105-D LOGIC ANALYZER

USERS MANUAL ADDENDUM

Z80 DISASSEMBLER

PRELIMINARY

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CONTENTS

INTRODUCTION

This addendum provides the user with specific information on the Z80 target microprocessor Disassemblers. Included in the addendum is a microprocessor pinout diagram, microprocessor-to-logic analyzer connection data, screen displays of the preprogrammed menus, a screen display of captured data in the disassembled format and special notes on the disassembler/logic analyzer.

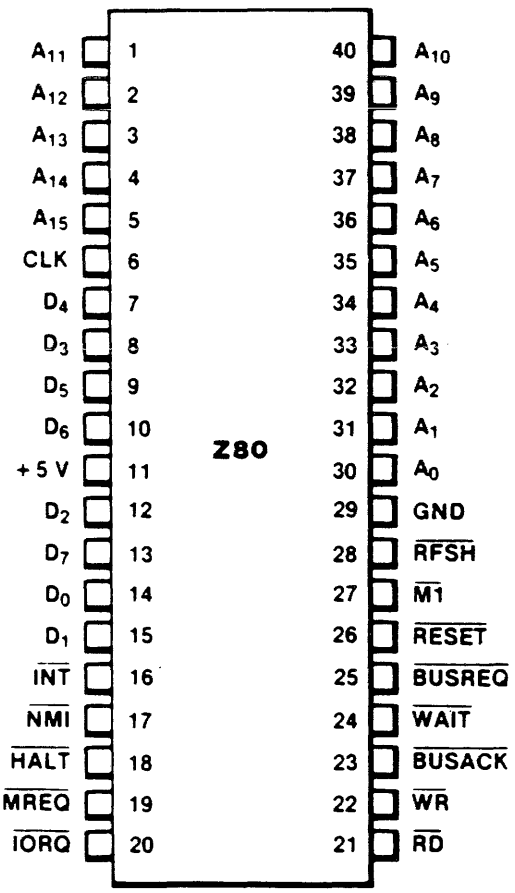

Figure 1-1. Z80 Microprocessor Pinout Diagram

Table 1-1. Microprocessor-To-Logic Analyzer Connection Data

Z80 SIGNAL	Z80 PIN	K105-D PIN ASSIGNMENT	RTE PIN ASSIGNMENT
A11	1	C3	J1-45
A12	2	C4	J1-47
A13	3	C5	J1-49
A14	4	C6	J1-51
A15	5	C7	J1-53
CLK	6	BK	J1-78
D4	7	A4	J1-69
D3	8	A3	J1-67
D5	9	A5	J1-71
D6	10	A6	J1-73
+5V	11	NOT CONNECTED	NOT CONNECTED
D2	12	A2	J1-65
D7	13	A7	J1-75
D0	14	A0	J1-61
D1	15	A1	J1-63
$\overline{INT}$	16	D6	J1-52
$\overline{NMI}$	17	D7	J1-54
$\overline{HALT}$	18	D4	J1-48
$\overline{MREQ}$	19	D2	J1-44
$\overline{IORQ}$	20	D1,CJ	J1-42,57
$\overline{RD}$	21	D3,BJ	J1-46,80
$\overline{WR}$	22	DJ	J1-58
$\overline{BUSACK}$	23	NOT CONNECTED	NOT CONNECTED
$\overline{WAIT}$	24	D5	J1-50
$\overline{BUSREQ}$	25	NOT CONNECTED	NOT CONNECTED
$\overline{RESET}$	26	NOT CONNECTED	NOT CONNECTED
$\overline{M1}$	27	D0	J1-40
$\overline{RFSH}$	28	NOT CONNECTED	NOT CONNECTED
GND	29	GND A-B-C-D SECT.	J1-1,2,37,38,59,60
A0	30	B0	J1-62
A1	31	B1	J1-64
A2	32	B2	J1-66
A3	33	B3	J1-68
A4	34	B4	J1-70
A5	35	B5	J1-72
A6	36	B6	J1-74
A7	37	B7	J1-76
A8	38	C0	J1-39
A9	39	C1	J1-41
A10	40	C2	J1-43

NOTE: The J1 Scrambler board is equivalent to the J7 Motherboard.

ATTACHMENT TO A TARGET SYSTEM

Figure 1-2 illustrates a typical RTE (Real Time Execution) to target system connection.

The RTE probe connectors are labeled to identify the input probe that must be plugged into the specific connector. The user shall remove the probe tips and install the probes, label up, into the RTE connectors. When connecting the microprocessor dip-cable into the RTE, special attention should be given to the keyed position of the connectors. The user should also ensure that pin 1 of the dip-clip is aligned with pin 1 of the microprocessor when connecting to the target microprocessor.

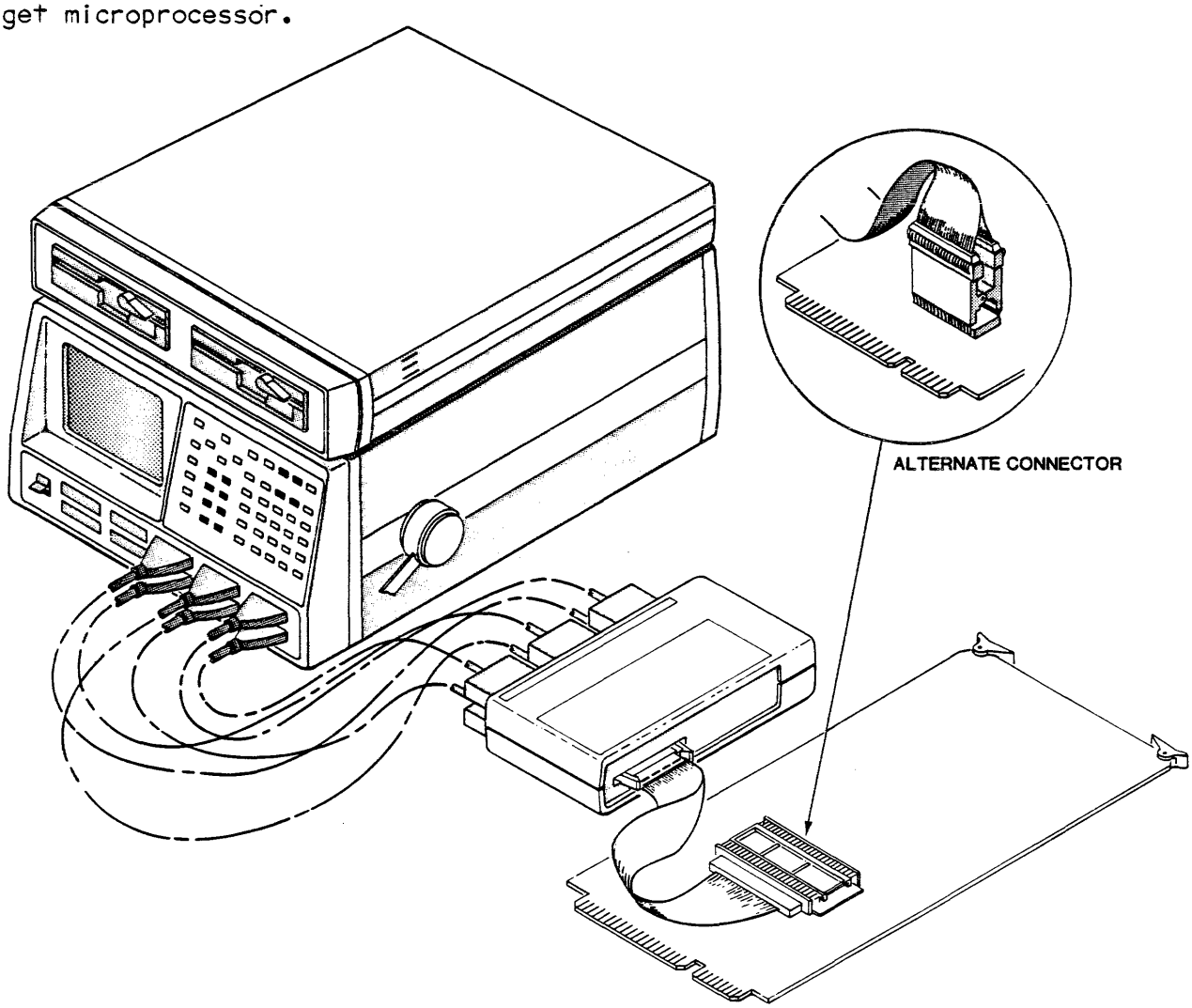

Figure 1-2. Typical RTE to Target System Connection

NOTE: Figure 1-2 shows one of several possible connections of the RTE to a target system. As the configuration of the microprocessor pinouts change, the RTE to target system interface may also change.

ATTACHMENT TO A TARGET SYSTEM

```
* * * * * * * * * * * * * * * * * * * * * * * * *
*                                               *
*                    CAUTION                    *
*                                               *
* In the event the microprocessor on your       *
* target system is soldered to the board and    *
* the alternate connector is being used, there  *
* is the possibility of inducing reflective     *
* noise into the test signals.  To eliminate    *
* this problem, we recommend varying the        *
* threshold voltage levels beyond noise levels. *
*                                               *
* * * * * * * * * * * * * * * * * * * * * * * * *
```

LOADING THE DISASSEMBLER

The following procedure provides step-by-step instructions for loading the Disassembler:

a. Enter the Disk Operating System screen.

b. Gently insert the disk into Drive B, with the disk slot toward the rear of the unit and the label up. Next, lock the disk in place with the drive latch handle.

c. Depress function key F3 to display the B directory.

d. Depress 1 to select the Recall function.

e. Use the right arrow cursor to enter the filename field and then use either the up or down cursor to select the Disassembler.

f. Depress function key F4 to load the Disassembler.

g. Depress the Format key to enter the Format screen.

h. Depress 6 and then DATA to enter Disassembler mode.

```
* * * * * * * * * * * * * * * * * * *
*                                     *
*               CAUTION               *
*                                     *
*  It is suggested that the user      *
*  make a backup copy of the          *
*  master disk prior to attempting    *
*  use of the disassembler.           *
*                                     *
* * * * * * * * * * * * * * * * * * * *
```

SPECIFICATIONS

PHYSICAL DIMENSIONS AND WEIGHT

Height - 2.25 inches (5.7 cm)
Width - 9.5 inches (24.1 cm)
Depth - 5.5 inches (14 cm)

Weight - 1 lb. 11 oz. (.77 kg) with flat cable, device clip and probe printed circuit board

ELECTRICAL CHARACTERISTICS

Loading (Signal Inputs)

Input Resistance - 1 megohm ±2% to threshold (-1.4 volts)

Input Impedance - 150 ohms (approximate)

Typical Rise/Fall Distortion - heavily dependent on [illegible] processor and its support devices. The 8086/8088 microprocessor slows approximately 5 nanoseconds on edge rates.

Loading (Ground/Reference Input)

Input Resistance - Less than 1 ohm referenced to target system ground.

Ground Difference Immunity - ± 0.25 maximum volts between logic analyzer ground and target system ground.

Reflected Noise Into Target System

Probed with Dip Clip or Circuit Board Socket - heavily dependent on target system ground. Typically, the system noise is reduced due to slower edge rates caused by probe load. This condition occasionally masks the problem being pursued.

SCREEN DISPLAYS OF PREPROGRAMMED SET UP MENUS

Figures 3-1 through 3-4 illustrate the preprogrammed setup menus downloaded from disk to the K105-D. Figure 3-4 illustrates the Disassembled Data. When in the Disassembled Data display, sequential depression of the SHIFT and V keys causes the software version number for the disassembler to be displayed.

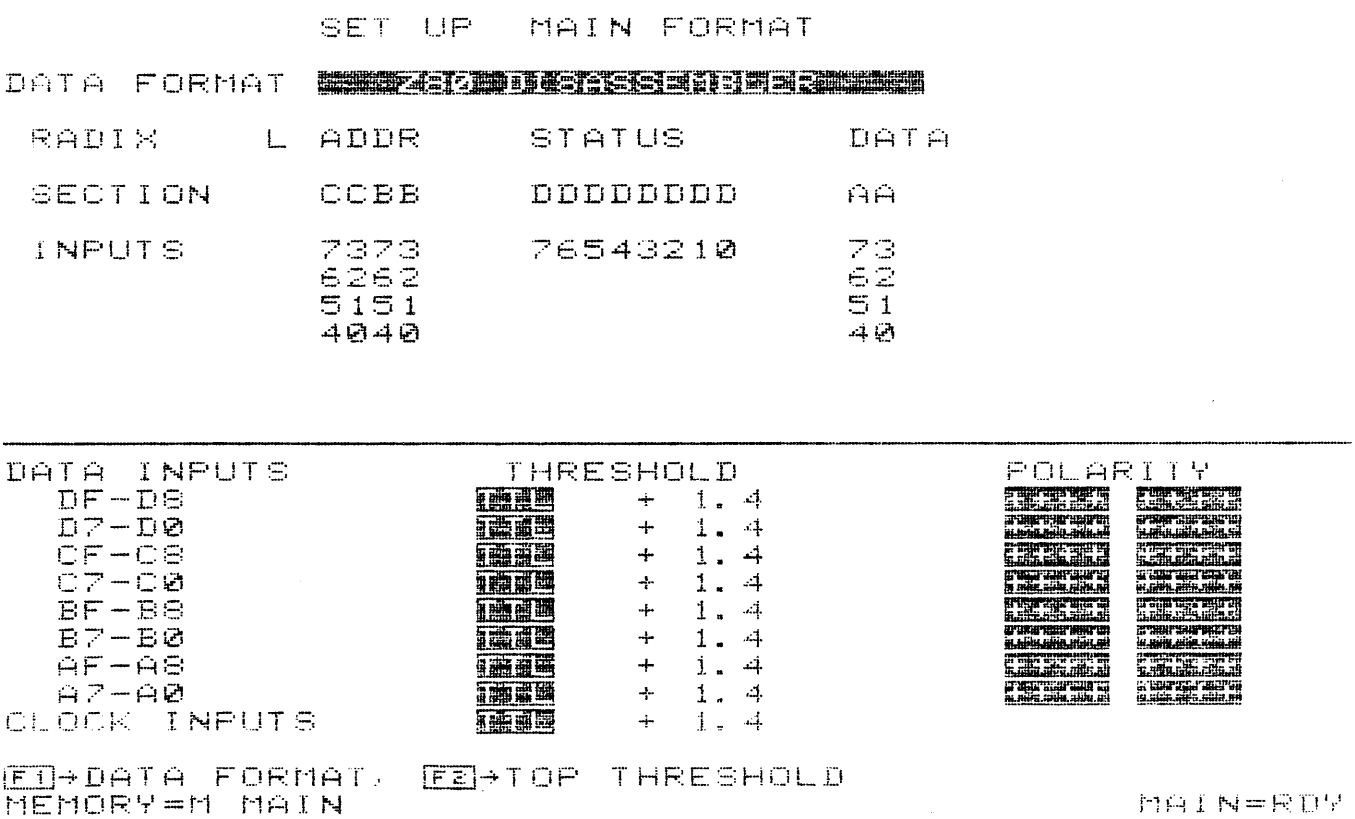

Figure 3-1. Disassembler Data Format Set Up Menu

SCREEN DISPLAYS OF PREPROGRAMMED SET UP MENUS (cont'd)

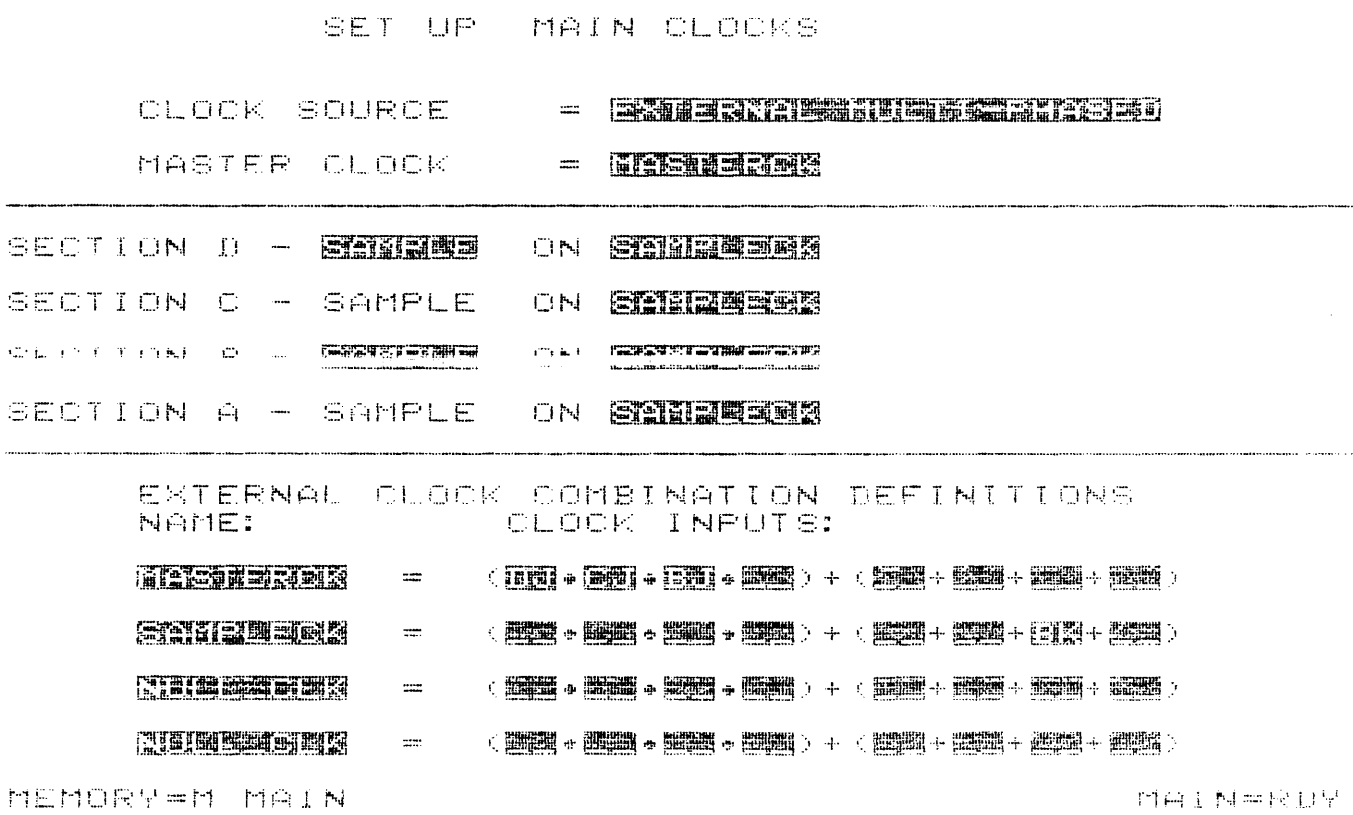

Figure 3-2. Clock Set Up Menu

SCREEN DISPLAYS OF PREPROGRAMMED SET UP MENUS (cont'd)

```
                SET UP  MAIN TRACE

LVL     COMMAND SEQUENCE:
0: TRACE  UNTIL    SAMPLE = ENABLE
1: TRACE  UNTIL    SAMPLE = TRIGGER
2: LINK ON ENTRY TO LEVEL
   TRACE  FOR    00512 CLOCKS
   _____
```

```
        PATTERN DEFINITIONS:
 NAME:          ADDR     STATUS        DATA
00 ENABLE   =XXXX     XXXXXXXX      XX
01 TRIGGER  =XXXX     XXXXXXXX      XX
02 _        =XXXX     XXXXXXXX      XX
```

```
F1→TOP CMD, F2→TOP PTRN
MEMORY=M MAIN                                   MAIN=RDY
```

Figure 3-3. Trace Control Set Up Menu

NOTE: In disassembler mode, the trace control patterns are formatted into address, status and data. When the status field is selected as the active field, the possible choices are the status conditions of the processor as follows:

(0) READ	(5) HALT
(1) WRITE	(6) ACK
(2) INPUT	(7) INT
(3) OUTPUT	(8) NMI
(4) FETCH	

In Edit mode, status bits can be edited on a bit-by-bit basis. "X" selects all don't cares.

SCREEN DISPLAYS OF PREPROGRAMMED SET UP MENUS (cont'd)

```
                          Z80 DISASSEMBLER          CLK= 50 nSEC

     S=XXXX                        XX                              X
FRAME  ADDR                        OBJ CODE     MNEMONIC           L
C  436  0B0A                       C3020B       JP    0B02         1
   439  0B02                       F5           PUSH  AF           1
   440  FF8F  WRITE                27                              1
   441  FF8E  WRITE                20                              1
   442  0B03                       DBDC         IN    A,(DC)       1
   444  27DC  INPUT                00                              1
   445  0B05                       F1           POP   AF           1
   446  FF8E  READ                 20                              1
   447  FF8F  READ                 27                              1
   448  0B05                       C505         ADD   H,05         1
   450  0B08                       D3DC         OUT   (DC),A       1
   452  2ADC  OUTPUT               2A                              1
   453  0B0A                       C3020B       JP    0B02         1
   456  0B02                       F5           PUSH  AF           1
   457  FF8F  WRITE                2A                              1
   458  FF8E  WRITE                28                              1
   459  0B03                       DBDC         IN    A,(DC)       1
   461  2ADC  INPUT                0D                              1
   462  0B05                       F1           POP   AF           1
   463  FF8E  READ                 28                              1
   464  FF8F  READ                 2A                              1

CONTROL=0436       REF=1023          R-C=+ 587  (29.35 MS)
F1→PG UP F2→PG DOWN F3→DSPLY OBJ F4→DSPLY MNEMONICS
MEMORY=A MAIN                                  MAIN=RDY
```

Figure 3-4. Captured Data in Disassembled Format

NOTES:

1. After the disassembler data format, and clock select menus of the logic analyzer are pre-programmed, the trace control selections must be made by the user before making a recording. The trace control selections determine exactly which portions of the data stream are recorded or ignored.

2. Although displayed, the sample labeled "SAMP" is not decoded.

3. If the disassembler is loaded and active, and an additional disassembler is to be loaded, always return to the Data Format screen to ensure the necessary tables are set up.

4. The SEARCH and COMPARE keys are not active in the Data Display Screen. The Edit mode can be used to change the search word. After leaving Edit mode, the NEXT and PREVIOUS keys locate target data in memory. If the search word is not active, the NEXT and PREVIOUS keys update the display to the next or previous trace level transition.

5. Depression of the F3 function key changes the display of recorded information. Code is not disassembled, but recorded information is displayed from the control cursor (C) position to the end of memory as frame number, address, status and data.

   If recorded data is displayed in object format, depressing the F4 function key invokes the disassembly process for data from the control cursor to the end of memory.

6. Illegal instructions are displayed as ???.

7. The disassembler is first downloaded from disk to the K105-D and the disassembler format is selected. The trace patterns are then configured as desired.