ALADDiN™ V

M1541/M1542

Socket 7
North Bridge -

Version 1.20

Please contact ALi applications department at 408-467-7456 to verify that all information is current before beginning a design using this datasheet.

M1541 : AGP, CPU-to-PCI bridge, Memory, Cache and Buffer Controller

1.1 Features

- **Supports all Socket 7 processors**. Host bus at 100MHz, 83.3MHz, 75MHz, 66 MHz, 60 MHz and 50MHz at 3.3V/2.5V.
  - Supports linear wrap mode for Cyrix M1 & M2
  - Supports Write Allocation feature for K6
  - Supports Pseudo Synchronous AGP and PCI bus access
  (CPU bus 75MHz - AGP bus 60MHz, PCI bus 30MHz,
  CPU bus 83.3MHz - AGP bus 66MHz, PCI bus 33MHz,
  CPU bus 100MHz - AGP bus 66MHz, PCI bus 33MHz)

- **Supports Pipelined-Burst SRAM/Memory Cache**
  - Direct mapped, 256KB/512KB/1MB
  - Write-Back/Dynamic-Write-Back cache policy
  - Built-in 16K*2 bit SRAM for MESI protocol to reduce cost and enhance performance
  - Built-in 16K*10 bit SRAM for TAG data to reduce cost and enhance performance (reserved)
  - Cacheable memory up to 128MB with 8-bit Tag SRAM when using 512KB L2 cache, 256MB when using 256KB L2 cache.
  - Cacheable memory up to 512MB with 10-bit Tag SRAM when using 512KB L2 cache, 1GB when using 256KB L2 cache
  - 3-1-1-1-1-1-1-1 for Pipelined Burst SRAM/ Memory Cache at back-to-back burst read and write cycles.
  - Supports 3.3V/5V SRAMs for Tag Address.
  - Supports CPU Single Read Cycle L2 Allocation.

- **Supports FPM/EDO/SDRAM DRAMs**
  - 8 RAS Lines up to 4G Byte support
  - 64-bit data path to Memory
  - Symmetrical/Asymmetrical DRAMs
  - 3.3V or 5V DRAMs
  - No buffer needed for RASJ and CASJ and MA
  - CBR and RAS-only refresh for FPM
  - CBR and RAS-only refresh and Extended refresh and self refresh for EDO
  - CBR and Self refresh for SDRAM
  - 32 QWORD deep merging buffer for 3-1-1-1-1-1-1-1 posted write cycle to enhance high speed CPU burst access
  - 6-3-3-3-3-3-3-3 for back-to-back FPM read page hit
    5-2-2-2-2-2-2-2 for back-to-back EDO read page hit
    6-1-1-1-1-1-1-1 for back-to-back SDRAM read page hit
    X-2-2-2-2-2-2-2 for retired data for posted write on FPM and EDO page-hit
    X-1-1-1-1-1-1-1 for retired data for posted write SDRAM page-hit
    Supports SDRAM internal bank operation
  - Enhanced DRAM page miss performance
  - Supports 64, 128, 256M-bit technology of DRAMs
  - Supports Programmable-strength CAS//MA buffers.
  - Supports Error Checking & Correction (ECC-at or below 83.3 MHz only) and Parity for DRAM
  - Supports 4 single-sided DIMMs based on x4 DRAMs
  - Supports 4 single and double-sided DIMMs based on x8 and x16 DRAMs
  - Supports 4 single-sided registered DIMMs based on 4 bits data width SDRAM

- **Synchronous/Pseudo Synchronous 25/30/33MHz 3.3V/5V tolerance PCI interface**
  - Concurrent PCI architecture
  - PCI bus arbiter: Five PCI masters and M1533/ M1543 (ISA Bridge) and AGP Master supported
  - 6 DWORDs for CPU-to-PCI Memory write posted buffers
  - Converts back-to-back CPU to PCI memory write to PCI burst cycle
  - 80/22 DWORDs for PCI-to-DRAM Write-posted/ Read-prefetching buffers
  - PCI-to-DRAM up to 133 MB/sec bandwidth (even when L1/L2 write back)
  - L1/L2 pipelined snoop ahead for PCI-to-DRAM cycle
  - Supports PCI mechanism #1 only
  - PCI spec. 2.1 support. (N(32/16/8)+8 rule, passive release, fair arbitration)
  - Enhanced performance for Memory-Read-Line and Memory-Read-Multiple and Memory-write-Invalidate PCI commands.

- **Enhanced Power Management**
  - ACPI support
  - Supports PCI bus CLKRUN function
  - Supports Dynamic Clock Stop
  - Supports Power On Suspend
  - Supports Suspend to Disk
  - Supports Suspend to DRAM
  - Self Refresh during Suspend

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- **Accelerated Graphics Port (AGP) Interface**
  - Supports AGP specification V1.0
  - Supports up to 64 entries table look aside buffer for Graphic Address Remapping Table (GART)
  - AGP 66MHz protocol
  - AGP 1X and 2X sideband address function
  - 28 entries Request queue
  - 32 QWORDs Read buffer
  - 16 QWORDs Write buffer

- **35x35 mm 456-pin BGA package**

Table of Contents :

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1.2 Introduction

Aladdin-V is the succeeding generation chipset of ALADDIN-IV from Acer Labs. It maintains the best system architecture (2-chip solution) to achieve the best system performance with the lowest system cost (TTL-free). ALADDIN-V consists of two BGA chips to give the 586-class system a complete solution with most up-to-date features and architecture for the most engaging multimedia/ multithreading OS and software applications. It utilizes the modern BGA package to improve the AC characterization, resolves system bottleneck and makes the system manufacturing easier.

M1541 includes the higher CPU bus frequency (up to 100 MHz) interface for the incoming Cyrix M2 and AMD K6, PBSRAM and Memory Cache L2 controller, internal MESI tag bits (16Kx2)and TAG RAM (16Kx10) to reduce cost and enhance performance, high performance FPM/EDO/SDRAM DRAM controller, PCI 2.1 compliant bus interface, smart deep buffer design for CPU-to-DRAM, CPU-to-PCI, and PCI-to-DRAM to achieve the best system performance, and also the highly efficient PCI fair arbiter. M1541 also provides the most flexible 64-bit memory bus interface for the best DRAM upgrade ability and ECC/Parity design to enhance the system reliability.

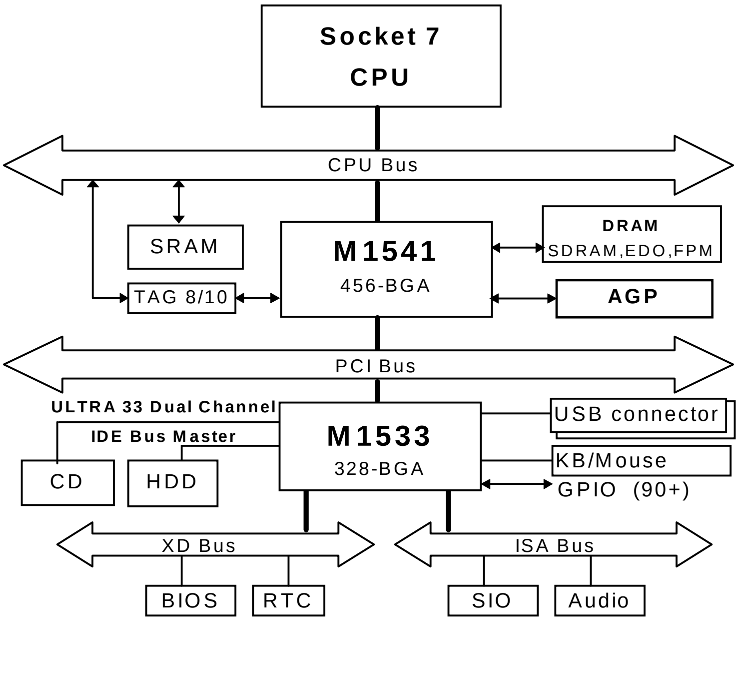
With the AGP interface design, the dedicated PCI_66 AGP interface is concurrent with CPU and PCI interface. The deep buffer of the read and write buffer design makes the utilization of memory bandwidth more efficient. The interface supports AGP specification V1.0. Supports up to 64 entries of table look aside buffer for Graphic Address Remapping Table (GART). The interface not only supports the AGP 66MHz protocol, but also the AGP 1X and 2X sideband address function.

With the concurrent bus design, PCI-to-PCI access can run concurrently with CPU-to-L2 and CPU-to-DRAM access, PCI-to-DRAM access can run concurrently with CPU-to-L2 access. M1541 also supports the snoop ahead feature to achieve the PCI master full bandwidth access (133Mbytes). M1541 also provides the enhanced power management features including ACPI support, suspend DRAM refresh, and internal chip power control to support Microsoft On Now technology OS.

M1533 provides the best power management system solution. M1533 integrates ACPI support, deep green function, 2-channel dedicated Ultra-33 IDE master controller, 2-port USB controller, SMBus controller, and PS2 Keyboard/Mouse controller. (see figure 1-1)

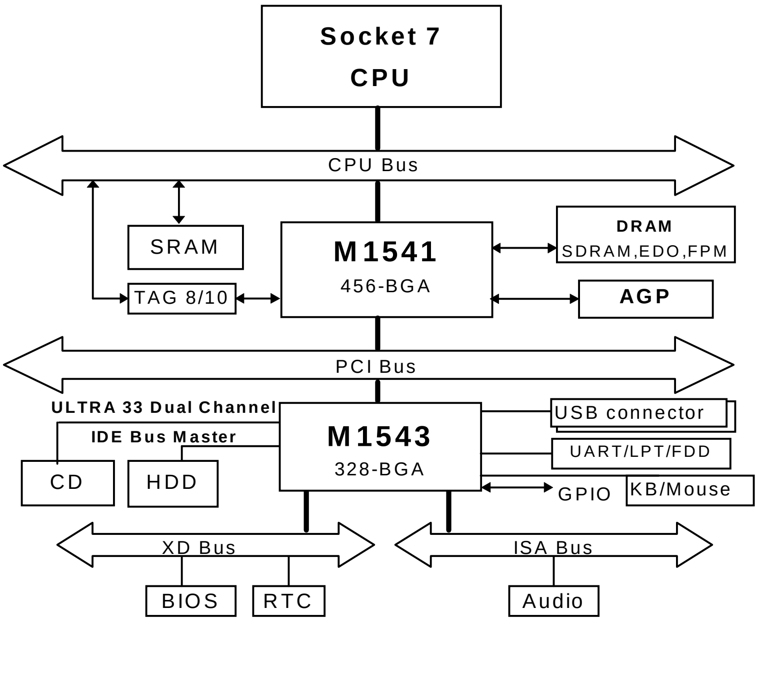
M1543 provides the best desktop system solution. M1543 integrates ACPI support, green function, 2-channel dedicated Ultra-33 IDE Master controller, 2-port USB controller, SMBus controller, PS/2 Keyboard/ Mouse controller and the Super I/O (Floppy Disk Controller, 2 serial port/1 parallel port) support. (see figure 1-2)

In the following diagram, ALADDIN-V gives a highly integrated system solution and a most up-to-date architecture, which provides the best cost/performance system solution for Desktop and also for Notebook vendors.



Aladdin V System Block Diagram with M1533

Figure 1-1



Aladdin V System Block Diagram with M1543

Figure 1-2

Section 2 : Pin Description

2.1 Pinout Diagram

M1541 for ATX, NLX, LPX form factor

M1541

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	HD 35	HD 37	HD 40	HD 43	HD 46	HD 50	HD 54	HD 59	WRJ	NAJ	ADS J	BEJ 5	BEJ 0
B	HD 34	NC	HD 39	HD 42	HD 45	HD 49	HD 53	HD 58	HD 63	KEN J	HLO CKJ	BEJ 6	BEJ 1
C	HD 33	HD 36	HD 38	HD 41	HD 44	HD 48	HD 52	HD 57	HD 62	AHO LD	EAD SJ	BEJ 7	BEJ 2
D	HD 30	HD 31	HD 32	NC	NC	HD 47	HD 51	HD 56	HD 61	CAC HEJ	BOF FJ	HITM J	BEJ 3
E	HD 27	HD 26	HD 28	HD 29	VDD _A	VDD _A	VSS_ P	HD 55	HD 60	MIOJ	BRD YJ	DCJ	BEJ 4
F	HD 24	HD 23	HD 22	HD 25	VDD _A								
G	HD 21	HD 20	HD 19	HD 18	VDD _B								
H	HD 17	HD 16	HD 15	HD 14	HD 13								
J	HD 12	HD 11	HD 10	HD 9	HD 8								
K	HD 7	HD 6	HD 5	HD 4	HD 3								
L	HD 2	HD 1	HD 0	HA 18	SMIA CTJ						G	G	G
M	HA 17	HA 16	HA 15	HA 14	HA 13						G	G	G
N	HA 12	HA 11	HA 10	HA 9	HA 8						G	G	G
P	HA 7	HA 6	HA 5	HA 4	HA 3						G	G	G
R	HA 19	HA 20	HA 21	HA 22	HA 23						G	G	G

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GWE J	CAD VJ	CAD SJ	TIO 5	TIO 8	TAG WEJ	MD 5	MD 7	MD 9	MD 11	MD 45	MD 46	NC
B	BWE J	CCS J	TIO 3	TIO 6	TIO 9	MD 3	MD 38	MD 40	MD 42	MD 44	NC	MD 13	MD 14
C	COE J	TIO 0	TIO 4	TIO 7	MD 34	MD 36	MD 6	MD 8	MD 10	MA 14	NC	MD 47	MD 15
D	TIO 1	HCL KIN	MD 32	MD 33	MD 2	MD 4	MD 39	MD 41	MD 43	MD 12	SCA SJ2	SCA SJ1	SCA SJ0
E	MKRE FRQJ	TIO 2	MD 0	MD 1	MD 35	MD 37	VDD _P	VDD _P	VDD _C	SCA SJ3	CAS J1	CAS J4	CAS J0
F									VDD _C	RAS J2	RAS J1	RAS J0	CAS J5
G									VDD _5S	RAS J6	RAS J5	RAS J4	RAS J3
H									SRA SJ3	SRA SJ2	SRA SJ1	SRA SJ0	RAS J7
J									MA 4	MA 3	MA 2	MA 1	MA 0
K									MA 9	MA 8	MA 7	MA 6	MA 5
L	G	G	G						CLK EN6	MA 13	MA 12	MA 11	MA 10
M	G	G	G						MPD 1	MPD 5	CLK EN0	CLK EN2	CLK EN4
N	G	G	G						MPD 7	MPD 2	MPD 6	MPD 0	MPD 4
P	G	G	G						DPL LO	CAS J2	CAS J6	MPD 3	DPL LI1
R	G	G	G						MWE J1	MWE J0	CAS J3	MWE J2	DPL LI0

T	HA 24	HA 25	HA 26	GNT J4	REQ J4						G	G	G	G	G	G						MD 48	ECA SJ1	ECA SJ5	MWE J3	CAS J7
U	HA 27	HA 28	HA 29	GNT J3	REQ J3																	MD 18	MD 50	MD 17	MD 49	MD 16
V	HA 30	GNT J2	REQ J2	GNT J1	REQ J1																	CLK EN1	MD 20	MD 52	MD 19	MD 51
W	HA 31	AD 31	GNT J0	REQ J0	PHL DJ																	OSC 32KI	MD 53	CLK EN7	CLK EN5	CLK EN3
Y	AD 30	AD 29	AD 28	AD 27	VDD _5																	VDD _C	MD 55	MD 22	MD 54	MD 21
AA	AD 26	AD 25	AD 24	CBE J3	VDD _B																	VDD _C	MD 57	MD 24	MD 56	MD 23
AB	AD 23	AD 22	AD 21	AD 20	VDD _B	VDD _B	VDD _B	PCIM RQJ	RST J	AD 0	PCI CLK	SBA 5	GAD 29	GAD 24	GAD 21	GAD 16	GTR DYJ	GCL KIN	GAD 12	Vref	VDD _P	VSS_ P	MD 59	MD 26	MD 58	MD 25
AC	AD 19	AD 18	AD 17	AD 16	AD 14	AD 10	AD 7	AD 4	AD 2	AD 1	PHL DAJ	SBA 4	GAD 30	GAD 25	GAD 22	GAD 17	GDEV SELJ	GPA R	GAD 13	GAD 8	GAD 6	NC	NC	MD 28	MD 60	MD 27
AD	CBE J2	FRA MEJ	NC	NC	AD 15	AD 11	CBE J0	AD 5	AD 3	RBF J	SBA 1	SB_ STB	GAD 31	GAD 26	GAD 23	GAD 18	GFRA MEJ	GSE RRJ	GAD 14	GAD 9	GAD 7	GAD 3	TES TJ	SUSP ENDJ	MD 61	MD 29
AE	IRDY J	TRD YJ	NC	DEV SELJ	CBE J1	AD 12	AD 8	AD 6	ST0	ST2	SBA 0	SBA 3	SBA 7	GAD 27	GCB EJ3	GAD 19	GIRD YJ	GPE RRJ	GAD 15	GAD 10	AD- STB0	GAD 4	MD 63	MD 30	NC	MD 62
AF	NC	STO PJ	LOC KJ	SER RJ	PAR	AD 13	AD 9	GRE QJ	GGN TJ	ST1	PIPE J	SBA 2	SBA 6	GAD 28	AD- STB1	GAD 20	GCB EJ2	GST OPJ	GCB EJ1	GAD 11	GCB EJ0	GAD 5	GAD 2	GAD 1	GAD 0	MD 31

TOP VIEW

Figure 2-1. M1541 Pin Diagram

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M1541

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	MD 46	MD 45	MD 11	MD 9	MD 7	MD 5	TAG WEJ	TIO 8	TIO 5	CAD SJ	CAD VJ	GWE J	BEJ 0	BEJ 5	ADS J	NAJ	WRJ	HD 59	HD 54	HD 50	HD 46	HD 43	HD 40	HD 37	HD 35
B	MD 14	MD 13	NC	MD 44	MD 42	MD 40	MD 38	MD 3	TIO 9	TIO 6	TIO 3	CCS J	BWE J	BEJ 1	BEJ 6	HLO CKJ	KEN J	HD 63	HD 58	HD 53	HD 49	HD 45	HD 42	HD 39	NC	HD 34
C	MD 15	MD 47	NC	MA 14	MD 10	MD 8	MD 6	MD 36	MD 34	TIO 7	TIO 4	TIO 0	COE J	BEJ 2	BEJ 7	EAD SJ	AHO LD	HD 62	HD 57	HD 52	HD 48	HD 44	HD 41	HD 38	HD 36	HD 33
D	SCA SJ0	SCA SJ1	SCA SJ2	MD 12	MD 43	MD 41	MD 39	MD 4	MD 2	MD 33	MD 32	HCL KIN	TIO 1	BEJ 3	HIT MJ	BOF FJ	CAC HEJ	HD 61	HD 56	HD 51	HD 47	NC	NC	HD 32	HD 31	HD 30
E	CAS J0	CAS J4	CAS J1	SCA SJ3	VDD _C	VDD _P	VDD _P	MD 37	MD 35	MD 1	MD 0	TIO 2	MKRE FRQJ	BEJ 4	DCJ	BRD YJ	MIOJ	HD 60	HD 55	VSS_ P	VDD _A	VDD _A	HD 29	HD 28	HD 26	HD 27
F	CAS J5	RAS J0	RAS J1	RAS J2	VDD _C																	VDD _A	HD 25	HD 22	HD 23	HD 24
G	RAS J3	RAS J4	RAS J5	RAS J6	VDD _5S																	VDD _B	HD 18	HD 19	HD 20	HD 21
H	RAS J7	SRA SJ0	SRA SJ1	SRA SJ2	SRA SJ3																	HD 13	HD 14	HD 15	HD 16	HD 17
J	MA 0	MA 1	MA 2	MA 3	MA 4																	HD 8	HD 9	HD 10	HD 11	HD 12
K	MA 5	MA 6	MA 7	MA 8	MA 9																	HD 3	HD 4	HD 5	HD 6	HD 7
L	MA 10	MA 11	MA 12	MA 13	CLK EN6						G	G	G	G	G	G						SMIA CTJ	HA 18	HD 0	HD 1	HD 2
M	CLK EN4	CLK EN2	CLK EN0	MPD 5	MPD 1						G	G	G	G	G	G						HA 13	HA 14	HA 15	HA 16	HA 17
N	MPD 4	MPD 0	MPD 6	MPD 2	MPD 7						G	G	G	G	G	G						HA 8	HA 9	HA 10	HA 11	HA 12
P	DPL LI1	MPD 3	CAS J6	CAS J2	DPL LO						G	G	G	G	G	G						HA 3	HA 4	HA 5	HA 6	HA 7
R	DPL LI0	MWE J2	CAS J3	MWE J0	MWE J1						G	G	G	G	G	G						HA 23	HA 22	HA 21	HA 20	HA 19

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T	CAS J7	MWE J3	ECA SJ5	ECA SJ1	MD 48						G	G	G	G	G	G						REQ J4	GNT J4	HA 26	HA 25	HA 24
U	MD 16	MD 49	MD 17	MD 50	MD 18																	REQ J3	GNT J3	HA 29	HA 28	HA 27
V	MD 51	MD 19	MD 52	MD 20	CLK EN1																	REQ J1	GNT J1	REQ J2	GNT J2	HA 30
W	CLK EN3	CLK EN5	CLK EN7	MD 53	OSC 32KI																	PHL DJ	REQ J0	GNT J0	AD 31	HA 31
Y	MD 21	MD 54	MD 22	MD 55	VDD _C																	VDD _5	AD 27	AD 28	AD 29	AD 30
AA	MD 23	MD 56	MD 24	MD 57	VDD _C																	VDD _B	CBE J3	AD 24	AD 25	AD 26
AB	MD 25	MD 58	MD 26	MD 59	VSS_ P	VDD _P	Vref	GAD 12	GCL KIN	GTR DYJ	GAD 16	GAD 21	GAD 24	GAD 29	SBA 5	PCIC LK	AD 0	RST J	PCIM RQJ	VDD _B	VDD _B	VDD _B	AD 20	AD 21	AD 22	AD 23
AC	MD 27	MD 60	MD 28	NC	NC	GAD 6	GAD 8	GAD 13	GPA R	GDEV SELJ	GAD 17	GAD 22	GAD 25	GAD 30	SBA 4	PHL DAJ	AD 1	AD 2	AD 4	AD 7	AD 10	AD 14	AD 16	AD 17	AD 18	AD 19
AD	MD 29	MD 61	SUSP ENDJ	TES TJ	GAD 3	GAD 7	GAD 9	GAD 14	GSE RRJ	GFRA MEJ	GAD 18	GAD 23	GAD 26	GAD 31	SB_ STB	SBA 1	RBF J	AD 3	AD 5	CBE J0	AD 11	AD 15	NC	NC	FRA MEJ	CBE J2
AE	MD 62	NC	MD 30	MD 63	GAD 4	AD- STB0	GAD 10	GAD 15	GPE RRJ	GIRD YJ	GAD 19	GCB EJ3	GAD 27	SBA 7	SBA 3	SBA 0	ST2	ST0	AD 6	AD 8	AD 12	CBE J1	DEV SELJ	NC	TRD YJ	IRDY J
AF	MD 31	GAD 0	GAD 1	GAD 2	GAD 5	GCB EJ0	GAD 11	GCB EJ1	GST OPJ	GCB EJ2	GAD 20	AD- STB1	GAD 28	SBA 6	SBA 2	PIPE J	ST1	GGN TJ	GRE QJ	AD 9	AD 13	PAR	SER RJ	LOC KJ	STO PJ	NC

BOTTOM VIEW (chip rotated left-right)

Figure 2-2. M1541 Pin Diagram

M1542 for Baby AT form factor

M1542

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	NC	STO PJ	LOC KJ	SER RJ	PAR	AD 13	AD 9	GRE QJ	GGN TJ	ST1	PIPE J	SBA 2	SBA 6	GAD 28	AD- STB1	GAD 20	GCB EJ2	GST OPJ	GCB EJ1	GAD 11	GCB EJ0	GAD 5	GAD 2	GAD 1	GAD 0	MD 31
B	IRDY J	TRD YJ	NC	DEV SELJ	CBE J1	AD 12	AD 8	AD 6	ST0	ST2	SBA 0	SBA 3	SBA 7	GAD 27	GCB EJ3	GAD 19	GIRD YJ	GPE RRJ	GAD 15	GAD 10	AD- STB0	GAD 4	MD 63	MD 30	NC	MD 62
C	CBE J2	FRA MEJ	NC	NC	AD 15	AD 11	CBE J0	AD 5	AD 3	RBF J	SBA 1	SB_ STB	GAD 31	GAD 26	GAD 23	GAD 18	GFRA MEJ	GSE RRJ	GAD 14	GAD 9	GAD 7	GAD 3	TES TJ	SUSP ENDJ	MD 61	MD 29
D	AD 19	AD 18	AD 17	AD 16	AD 14	AD 10	AD 7	AD 4	AD 2	AD 1	PHL DAJ	SBA 4	GAD 30	GAD 25	GAD 22	GAD 17	GDEV SELJ	GPA R	GAD 13	GAD 8	GAD 6	NC	NC	MD 28	MD 60	MD 27
E	AD 23	AD 22	AD 21	AD 20	VDD _B	VDD _B	VDD _B	PCIM RQJ	RST J	AD 0	PCI CLK	SBA 5	GAD 29	GAD 24	GAD 21	GAD 16	GTR DYJ	GCL KIN	GAD 12	Vref	VDD _P	VSS_ P	MD 59	MD 26	MD 58	MD 25
F	AD 26	AD 25	AD 24	CBE J3	VDD _B																	VDD _C	MD 57	MD 24	MD 56	MD 23
G	AD 30	AD 29	AD 28	AD 27	VDD _5																	VDD _C	MD 55	MD 22	MD 54	MD 21
H	HA 31	AD 31	GNT J0	REQ J0	PHL DJ																	OSC 32KI	MD 53	CLK EN7	CLK EN5	CLK EN3
J	HA 30	GNT J2	REQ J2	GNT J1	REQ J1																	CLK EN1	MD 20	MD 52	MD 19	MD 51
K	HA 27	HA 28	HA 29	GNT J3	REQ J3																	MD 18	MD 50	MD 17	MD 49	MD 16
L	HA 24	HA 25	HA 26	GNT J4	REQ J4						G	G	G	G	G	G						MD 48	ECA SJ1	ECA SJ5	MWE J3	CAS J7
M	HA 19	HA 20	HA 21	HA 22	HA 23						G	G	G	G	G	G						MWE J1	MWE J0	CAS J3	MWE J2	DPL LI0
N	HA 7	HA 6	HA 5	HA 4	HA 3						G	G	G	G	G	G						DPL L0	CAS J2	CAS J6	MPD 3	DPL LI1
P	HA 12	HA 11	HA 10	HA 9	HA 8						G	G	G	G	G	G						MPD 7	MPD 2	MPD 6	MPD 0	MPD 4
R	HA 17	HA 16	HA 15	HA 14	HA 13						G	G	G	G	G	G						MPD 1	MPD 5	CLK EN0	CLK EN2	CLK EN4

T	HD 2	HD 1	HD 0	HA 18	SMIA CTJ						G	G	G	G	G	G						CLK EN6	MA 13	MA 12	MA 11	MA 10
U	HD 7	HD 6	HD 5	HD 4	HD 3																	MA 9	MA 8	MA 7	MA 6	MA 5
V	HD 12	HD 11	HD 10	HD 9	HD 8																	MA 4	MA 3	MA 2	MA 1	MA 0
W	HD 17	HD 16	HD 15	HD 14	HD 13																	SRA SJ3	SRA SJ2	SRA SJ1	SRA SJ0	RAS J7
Y	HD 21	HD 20	HD 19	HD 18	VDD _B																	VDD _5S	RAS J6	RAS J5	RAS J4	RAS J3
AA	HD 24	HD 23	HD 22	HD 25	VDD _A																	VDD _C	RAS J2	RAS J1	RAS J0	CAS J5
AB	HD 27	HD 26	HD 28	HD 29	VDD _A	VDD _A	VSS_ P	HD 55	HD 60	MIOJ	BRD YJ	DCJ	BEJ 4	MKRE FRQJ	TIO 2	MD 0	MD 1	MD 35	MD 37	VDD _P	VDD _P	VDD _C	SCA SJ3	CAS J1	CAS J4	CAS J0
AC	HD 30	HD 31	HD 32	NC	NC	HD 47	HD 51	HD 56	HD 61	CAC HEJ	BOF FJ	HIT MJ	BEJ 3	TIO 1	HCL KIN	MD 32	MD 33	MD 2	MD 4	MD 39	MD 41	MD 43	MD 12	SCA SJ2	SCA SJ1	SCA SJ0
AD	HD 33	HD 36	HD 38	HD 41	HD 44	HD 48	HD 52	HD 57	HD 62	AHO LD	EAD SJ	BEJ 7	BEJ 2	COE J	TIO 0	TIO 4	TIO 7	MD 34	MD 36	MD 6	MD 8	MD 10	MA 14	NC	MD 47	MD 15
AE	HD 34	NC	HD 39	HD 42	HD 45	HD 49	HD 53	HD 58	HD 63	KEN J	HLO CKJ	BEJ 6	BEJ 1	BWE J	CCS J	TIO 3	TIO 6	TIO 9	MD 3	MD 38	MD 40	MD 42	MD 44	NC	MD 13	MD 14
AF	HD 35	HD 37	HD 40	HD 43	HD 46	HD 50	HD 54	HD 59	WRJ	NAJ	ADS J	BEJ 5	BEJ 0	GWE J	CAD VJ	CAD SJ	TIO 5	TIO 8	TAG WEJ	MD 5	MD 7	MD 9	MD 11	MD 45	MD 46	NC

TOP VIEW

Figure 2-3. M1542 Pin Diagram

M1542

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	MD 31	GAD 0	GAD 1	GAD 2	GAD 5	GCB EJ0	GAD 11	GCB EJ1	GST OPJ	GCB EJ2	GAD 20	AD- STB1	GAD 28	SBA 6	SBA 2	PIPE J	ST1	GGN TJ	GRE QJ	AD 9	AD 13	PAR	SER RJ	LOC KJ	STO PJ	NC
B	MD 62	NC	MD 30	MD 63	GAD 4	AD- STB0	GAD 10	GAD 15	GPE RRJ	GIRD YJ	GAD 19	GCB EJ3	GAD 27	SBA 7	SBA 3	SBA 0	ST2	ST0	AD 6	AD 8	AD 12	CBE J1	DEV SELJ	NC	TRD YJ	IRDY J
C	MD 29	MD 61	SUSP ENDJ	TES TJ	GAD 3	GAD 7	GAD 9	GAD 14	GSE RRJ	GFRA MEJ	GAD 18	GAD 23	GAD 26	GAD 31	SB_ STB	SBA 1	RBF J	AD 3	AD 5	CBE J0	AD 11	AD 15	NC	NC	FRA MEJ	CBE J2
D	MD 27	MD 60	MD 28	NC	NC	GAD 6	GAD 8	GAD 13	GPA R	GDEV SELJ	GAD 17	GAD 22	GAD 25	GAD 30	SBA 4	PHL DAJ	AD 1	AD 2	AD 4	AD 7	AD 10	AD 14	AD 16	AD 17	AD 18	AD 19
E	MD 25	MD 58	MD 26	MD 59	VSS_ P	VDD _P	Vref	GAD 12	GCL KIN	GTR DYJ	GAD 16	GAD 21	GAD 24	GAD 29	SBA 5	PCI CLK	AD 0	RST J	PCIM RQJ	VDD _B	VDD _B	VDD _B	AD 20	AD 21	AD 22	AD 23
F	MD 23	MD 56	MD 24	MD 57	VDD _C																	VDD _B	CBE J3	AD 24	AD 25	AD 26
G	MD 21	MD 54	MD 22	MD 55	VDD _C																	VDD _5	AD 27	AD 28	AD 29	AD 30
H	CLK EN3	CLK EN5	CLK EN7	MD 53	OSC 32KI																	PHL DJ	REQ J0	GNT J0	AD 31	HA 31
J	MD 51	MD 19	MD 52	MD 20	CLK EN1																	REQ J1	GNT J1	REQ J2	GNT J2	HA 30
K	MD 16	MD 49	MD 17	MD 50	MD 18																	REQ J3	GNT J3	HA 29	HA 28	HA 27
L	CAS J7	MWE J3	ECA SJ5	ECA SJ1	MD 48						G	G	G	G	G	G						REQ J4	GNT J4	HA 26	HA 25	HA 24
M	DPL LI0	MWE J2	CAS J3	MWE J0	MWE J1						G	G	G	G	G	G						HA 23	HA 22	HA 21	HA 20	HA 19
N	DPL LI1	MPD 3	CAS J6	CAS J2	DPL L0						G	G	G	G	G	G						HA 3	HA 4	HA 5	HA 6	HA 7
P	MPD 4	MPD 0	MPD 6	MPD 2	MPD 7						G	G	G	G	G	G						HA 8	HA 9	HA 10	HA 11	HA 12
R	CLK EN4	CLK EN2	CLK EN0	MPD 5	MPD 1						G	G	G	G	G	G						HA 13	HA 14	HA 15	HA 16	HA 17

T	MA 10	MA 11	MA 12	MA 13	CLK EN6						G	G	G	G	G	G						SMIA CTJ	HA 18	HD 0	HD 1	HD 2
U	MA 5	MA 6	MA 7	MA 8	MA 9																	HD 3	HD 4	HD 5	HD 6	HD 7
V	MA 0	MA 1	MA 2	MA 3	MA 4																	HD 8	HD 9	HD 10	HD 11	HD 12
W	RAS J7	SRA SJ0	SRA SJ1	SRA SJ2	SRA SJ3																	HD 13	HD 14	HD 15	HD 16	HD 17
Y	RAS J3	RAS J4	RAS J5	RAS J6	VDD _5S																	VDD _B	HD 18	HD 19	HD 20	HD 21
AA	CAS J5	RAS J0	RAS J1	RAS J2	VDD _C																	VDD _A	HD 25	HD 22	HD 23	HD 24
AB	CAS J0	CAS J4	CAS J1	SCA SJ3	VDD _C	VDD _P	VDD _P	MD 37	MD 35	MD 1	MD 0	TIO 2	MKRE FRQJ	BEJ 4	DCJ	BRD YJ	MIOJ	HD 60	HD 55	VSS_ P	VDD _A	VDD _A	HD 29	HD 28	HD 26	HD 27
AC	SCA SJ0	SCA SJ1	SCA SJ2	MD 12	MD 43	MD 41	MD 39	MD 4	MD 2	MD 33	MD 32	HCL KIN	TIO 1	BEJ 3	HITM J	BOF FJ	CAC HEJ	HD 61	HD 56	HD 51	HD 47	NC	NC	HD 32	HD 31	HD 30
AD	MD 15	MD 47	NC	MA 14	MD 10	MD 8	MD 6	MD 36	MD 34	TIO 7	TIO 4	TIO 0	COE J	BEJ 2	BEJ 7	EAD SJ	AHO LD	HD 62	HD 57	HD 52	HD 48	HD 44	HD 41	HD 38	HD 36	HD 33
AE	MD 14	MD 13	NC	MD 44	MD 42	MD 40	MD 38	MD 3	TIO 9	TIO 6	TIO 3	CCS J	BWE J	BEJ 1	BEJ 6	HLO CKJ	KEN J	HD 63	HD 58	HD 53	HD 49	HD 45	HD 42	HD 39	NC	HD 34
AF	NC	MD 46	MD 45	MD 11	MD 9	MD 7	MD 5	TAG WEJ	TIO 8	TIO 5	CAD SJ	CAD VJ	GWE J	BEJ 0	BEJ 5	ADS J	NAJ	WRJ	HD 59	HD 54	HD 50	HD 46	HD 43	HD 40	HD 37	HD 35

BOTTOM VIEW

Figure 2-4. M1542 Pin Diagram

2.2. Pin Description Table :

Pin Name	Type	Description
Host Interface :	3.3V/(2.5)	
HA[31:3]	I/O Group A	**Host Address Bus Lines**. HA[31:3] have two functions. As inputs, along with the byte enable signals, these pins serve as the address lines of the host address bus which define the physical area of memory or I/O being accessed. As outputs, the M1541 drives them during inquiry cycles on behalf of PCI masters.
BEJ[7:0]	I Group A	**Byte Enables**. These are the byte enable signals for the data bus. BEJ[7] applies to the most significant byte while BEJ[0] applies to the least significant byte. They determine which byte of data must be written to the memory, or are requested by the CPU. In local memory read and line-fill cycles, these inputs are ignored by the M1541.
ADSJ	I Group A	**Address Strobe**. The CPU will start a new cycle by asserting ADSJ first. The M1541 will not precede to execute a cycle until it detects ADSJ active.
BRDYJ	O Group A	**Burst Ready**. The assertion of BRDYJ means the current transaction is complete. The CPU will terminate the cycle by receiving 1 or 4 active BRDYJs depending on different types of cycles.
NAJ	O Group A	**Next Address**. It is asserted by the M1541 to inform the CPU that pipelined cycles are ready for execution.
AHOLD	O Group A	**CPU Ahold Request Output**. It connects to the input of CPU AHOLD pin and is actively driven for inquiry cycles.
EADSJ	O Group A	**External Address Strobe**. This signal is connected to the CPU EADSJ pin. During PCI cycles, the M1541 will assert this signal to proceed snooping.
BOFFJ	O Group A	**CPU Back-Off**. If BOFFJ is sampled active, CPU will float all its buses in the next clock. M1541 will assert this signal to request CPU floating all its output buses.
HITMJ	I Group A	**Primary Cache Hit and Modified**. When snooped, the CPU asserts HITMJ to indicate that a hit to a modified line in the data cache occurred. It is used to prohibit another bus master from accessing the data of this modified line in the memory until the line is completely written back.
MIOJ	I Group A	**Host Memory or I/O**. This bus definition pin indicates the current bus cycle is either memory or input/ output.
DCJ	I Group A	**Host Data or Code**. This bus definition pin is used to distinguish data access cycles from code access cycles.
WRJ	I Group A	**Host Write or Read**. When WRJ is driven high, it indicates the current cycle is a write. Inversely, if WRJ is driven low, a read cycle is performed.

HLOCKJ	I Group A	**Host Lock**. When HLOCKJ is asserted by the CPU, the M1541 will recognize the CPU is locking the current cycles.
CACHEJ	I Group A	**Host Cacheable**. This pin is used by the CPU to indicate the system that CPU wants to perform a line fill cycle or a burst write back cycle. If it is driven inactive in a read cycle, the CPU will not cache the returned data, regardless of the state of KENJ.
KENJ/INV	O Group A	**Cache Enable Output**. This signal is connected to the CPU KENJ and INV pins. KENJ is used to notify the CPU whether the address of the current transaction is cacheable. INV is used during L1 snoop cycles. The M1541 drives this signal high (low) during the EADSJ assertion of a PCI master write (read) snoop cycle.
SMIACTJ	I Group A	**SMM Interrupt Active**. This signal is asserted by the CPU to inform the M1541 that SMM mode is being entered.
HD[63:0]	I/O Group A	**Host Data Bus Lines**. These signals are connected to the CPU data bus. HD[63] applies to the most significant bit and HD[0] applies to the least significant bit.
DRAM Interface 3.3V/5V Tolerance		
MPD[7:0]	I/O Group C	**DRAM Parity /ECC check bits**. These are the 8 bits for parities/ECC check bits over DRAM data bus. MPD[7] applies to the most significant bit and MPD[0] applies to the least significant bit when MPD[7:0] serves as parity bits.

Pin Description Table (continued)

Pin Name	Type	Description
RASJ[7:0] / SCSJ[7:0]	O Group C	**Row Address Strobe** (FPM/EDO) of DRAM row **SDRAM Chip Select Strobe (SDRAM)**. These are multifunction pins
CASJ[7:0] / SDQM[7:0]	O Group C	**Column Address Strobes or Synchronous DRAM Input/Output Data Mask** These CAS signals should be connected to the corresponding CASJs of each bank of DRAM. The value of CASJs equals that of HBEJs for write cycles. During DRAM read cycles, all of CASJs will be active. In SDRAM, these pins act as synchronized output enables during a read cycle and the byte mask during write cycle, these pins are connected to SDRAM DQM[7:0].
ECASJ[5/1] / ESDQM[5/1]	O Group C	**Extra Column Address Strobes 5 and 1 or Extra Synchronous DRAM Input/Output Data Mask5 and 1**. These are copies of CASJ[5/1] or SDQM[5/1] signals. These are used to balance the loading at ECC memory configurations mode because these signals are double-loaded.
MA[14:0]	O Group C	**DRAM Address** These signals are the address lines[14:0] of all DRAMs. The M1541 supports DRAM types ranging from 256K to 256Mbits.
SRASJ[3:0]	O Group C	**SDRAM Row Address Strobe** The SRASJ[3:0] are multiple copies of SDRAM row address strobe for the loading purpose. When SRASJ[3:0] is sampled active at the rising edge of the SDRAM clock the row address is latched into the SDRAMs.
SCASJ[3:0]	O Group C	**SDRAM Column Address Strobe** The SCASJ[3:0] are multiple copies of SDRAM column address strobe for the loading purpose. When SCASJ[3:0] is sampled active at the rising edge of the SDRAM clock the Column address is latched into the SDRAMs.
MWEJ[3:0]	O Group C	**DRAM Write Enable**. These are the DRAM write enable signals and behave according to the early-write mechanism, i.e., they activate before the CASJs do. For refresh cycles, it will remain deasserted. For sharing load purpose, the MWEJ[3:0] are multiple copies of the same Memory Write Enable signal.
MD[63:0]	I/O Group C	**Memory Data**. These pins are connected to DRAM data bits. MD[63] applies to the most significant bit and MD[0] applies to the least significant bit.
CLKEN[7:0]	O Group C	**SDRAM Clock Enable.** These signals are used as SDRAM clock enable to do self refresh during suspend. For sharing load purposes, the CLKEN[7:0] are multiple copies of the same SDRAM clock enable signal.
DPLLO	O Group C	**DRAM PLL output** The Clock output sent to external clock buffer then sent to SDRAM as clock source.
DPLLI[1:0]	I Group C	**DRAM PLL input** There are two Feedback clocks. One to compensate the write circuit. One to compensate the read circuit.

Secondary Cache Interface 3.3V/5V tolerance		
CADVJ	O Group B	**Synchronous SRAM Advance**. This signal will make PBSRAM/Memory Cache internal burst address counter advance.
CADSJ	O Group B	**Synchronous SRAM Address Strobe**. This signal connects to PBSRAM/ Memory Cache ADSCJ.
CCSJ	O Group B	**Synchronous SRAM Chip Select**. This signal connects to PBSRAM/Memory Cache CE1J to mask ADSPJ and enable ADSCJ sampling.
GWEJ	O Group B	**Synchronous SRAM Global Write Enable**. This signal will write all the byte lanes data into PBSRAM/Memory Cache.
COEJ	O Group B	**Synchronous SRAM Output Enable**. This signal will enable the data output driving of PBSRAM/Memory Cache.
BWEJ	O Group B	**Synchronous SRAM Byte-Write Enable**. This signal connects to byte write enable of PBSRAM/Memory Cache.

Pin Description Table (continued)

Pin Name	Type	Description
MKREFRQJ	I/O Group B	**Memory Cache REFresh ReQuest /Acknowledge** MKREFRQJ connected to DRAM Cache. This signal is normally driven by the Memory cache and will be sample by M1541 on each rising clock edge. The high state indicates no refresh request by Memory cache. Memory cache will signal a refresh request by driving this signal low for one clock, then driving high for one clock, then tri-state until M1541 grants the request. The M1541 signals refresh acknowledge by driving the signal low for once clock, then driving high for one clock then tri-state until the next request by Memory cache. Upon detecting that M1541 has driven this signal low, DRAM cache will begin a twenty clock refresh cycle and will let the signal float for one clock then drive the signal high until another refresh cycle is required.
TAG Interface 3.3V/5V Tolerance		
TIO[9:0]/	I/O Group B	**SRAM Tag[9:0]** . These signals are SRAM tag address bit 10. If only one TAG SRAM is used, it should connect to TIO[7:0]. If system requires more cacheable memory rang, another TAG SRAM will be required. The connect sequence is from TIO[8] to TIO[9]
TAGWEJ	O Group B	**Tag Write Enable**. This signal, when asserted, will write into the external tag new state and tag addresses.
PCI Interface 3.3V/5V Tolerance		
AD[31:0]	I/O Group B	**PCI Address and Data Bus Lines**. These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions. During Configuration cycle, M1541 will use AD11 as IDSEL and AD12 for PCI-to-PCI bridge IDSEL internally. The AD11 and AD12 should not connect to any PCI device IDSEL pin.
CBEJ[3:0]	I/O Group B	**PCI Bus Command and Byte Enables**. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.
FRAMEJ	I/O Group B	**Cycle Frame of PCI Buses**. This indicates the beginning and duration of a PCI access. It will be as an output driven by M1541 on behalf of CPU, or as an input during PCI master access.
DEVSELJ	I/O Group B	**Device Select**. When the target device has decoded the address as its own cycle, it will assert DEVSELJ.
IRDYJ	I/O Group B	**Initiator Ready**. This signal indicates the initiator is ready to complete the current data phase of transaction.
TRDYJ	I/O Group B	**Target Ready**. This pin indicates the target is ready to complete the current data phase of transaction.
STOPJ	I/O Group B	**Stop**. This signal indicates the target is requesting the master to stop the current transaction.

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LOCKJ	I/O Group B	**Lock Resource Signal**. This pin indicates the PCI master or the bridge intends to do exclusive transfers.
REQJ[4:0]	I Group B	**Bus Request signals of PCI Masters**. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter.
GNTJ[4:0]	O Group B	**Grant signals to PCI Masters**. When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus.
PHLDJ	I Group B	**PCI bus Hold Request**. This active low signal is a request from M1533/M1543 for the PCI bus.
PHLDAJ	O Group B	**PCI bus Hold Acknowledge**. This active low signal grants PCI bus to M1533/M1543.
PAR	I/O Group B	**Parity bit of PCI bus**. It is the even parity bit across PAD[31:0] and CBEJ[3:0].
SERRJ/ CLKRUNJ	I/O Group B	**System Error or PCI Clock RUN**. If the M1541 detects parity errors in DRAMs, it will assert SERRJ to notify the system. As CLKRUNJ, this signal will connect to M1533 CLKRUNJ to start, or maintain the PCI CLOCK.
PCIMRQJ	O Group B	**ACPI Total PCI Request**. This signal is used to notify M1533/M1543 there is PCI master requesting PCI bus.

Pin Description Table (continued)

Pin Name	Type	Description
Clock, Reset, and Suspend		
HCLKIN	I Group B	**CPU bus Clock Input**. This signal is used by all of the M1541 logic that is in the Host clock domain.
RSTJ	I Group B	**System Reset**. This pin, when asserted, resets the M1541 state machine, and sets the register bits to their default values. When SUSPENDJ active, the suspend survival circuit will not be reset. When SUSPENDJ is de-asserted , the suspend survival circuit will be reset too.
PCICLK	I Group B	**PCI bus Clock Input**. This signal is used by all of the M1541 logic that is in the PCI clock domain.
SUSPENDJ	I Group C	**Suspend**. When actively sampled, the M1541 will enter the I/O suspend mode. This signal should be pulled high when the suspend feature is disabled.
CLK32KI	I Group C	**32KHz clock** The refresh reference clock of frequency 32KHz during suspend mode. This signal should be pulled to a fixed value when the suspend feature is disabled.
TESTJ	I Group C	**NAND tree test input** Test mode setting input When setting this signal to Low, M1541 will be at NAND tree test mode. For normal operation, this signal should be pulled high to VDD_C the same power plane supporting DRAM suspend logic.
AGP interface		
ST[2:0]	O Group B.	**Status** bus provides information from the arbiter to a Master on what it may do. ST[2:0] only have meaning to AGP master when its GGNTJ is asserted, otherwise these signals have no meaning and must be ignored. ST[2:0] : 000 Indicates that previously requested low priority read or flush data is being returned to the master 001 indicates that previously requested high priority read data is being returned to the master 010 indicates that the master is to provide low priority write data for a previous enqueued write command 011 indicates that the master is to provide high priority write data for a previous enqueued write command 100-110 Reserved 111 Indicates that the master has been given permission to start a bus transaction. The master may enqueue A.G.P. requests by asserting PIPEJ or start a PCI transaction by asserting FRAMEJ. ST[2:0] are always an output from M1541 and an input to the AGP graphic controller master.

SBA[7:0]	O Group B	**Sideband address port** provides an additional bus to pass address and command to the target from the master. SBA[7:0] are outputs from a master and an input to the target. This port is ignored by the target until enabled.
PIPEJ	I Group B	**Pipelined** request is asserted by the current master to indicated a full width request is to be enqueued by the target. The master enqueues one request each rising edge of CLK while PIPEJ is asserted. When PIPEJ is deasserted no new requests are across the AD bus. PIPEJ is a sustained tri-state signal from graphics controller and is an input to M1541
RBFJ	I Group B	**Read Buffer Full** indicates if the master is ready to accept previously requested low priority read data or not. When RBFJ is asserted the arbiter is not allow to initiate the return of low priority read data to the master.
AD_STB0	I/O Group B	**AD bus Strobe 0** provides timing for 2X data transfer mode on the GAD[15:0] . The agent that is providing data drives this signal.
AD_STB1	I/O Group B	**AD bus Strobe 1** provides timing for 2X data transfer mode on the GAD[31:15] . The agent that is providing data drives this signal.
SB_STB	I Group B.	**Sideband probe** provides timing for SBA[7:0] and is always driven by the A.G.P. compliant master

Pin Description Table (continued)

Pin Name	Type	Description
PCI 66 Interface 3.3V/5V Tolerance		
GAD[31:0]	I/O Group B	**A.G.P. PCI Address and Data Bus Lines**. These lines are connected to the A.G.P. PCI bus. AD[31:0] contain the information of address or data for PCI transactions.
GCBEJ[3:0]	I/O Group B	**A.G.P. PCI Bus Command and Byte Enables**. There are different meanings. Provided command information(Different command than PCI) by the master when requests are being enqueued using PIPEJ. Provides valid byte information during A.G.P> write transactions and is driven by the master, The M1541 drives to “0000” during the return of A.G.P. read data and is ignored by the A.G.P. compliant master.
GFRAMEJ	I/O Group B	**Cycle Frame of PCI Buses**. Not used at A.G.P. mode. FRAMEJ remains deasserted by its own pull up resister Only used during PCI operation on A.G.P. This indicates the beginning and duration of a PCI access. It will be as an output driven by M1541 when a PCI transaction is initiated by M1541 or as an input during A.G.P master access.
GDEVSELJ	I/O Group B	**Device Select**. Not used by A.G.P. Only used during PCI operation on A.G.P. When the target device has decoded the address as its own cycle, it will assert DEVSELJ.
GIRDYJ	I/O Group B	New meaning. GIRDYJ indicates the A.G.P. compliant master is ready to provided all write data for the current transaction. Once GIRDYJ is asserted for a write operation, the master is not allowed to insert wait states. The assertion of GIRDYJ for reads, indicates that the master is ready to transfer a subsequent block of read data. The master is never allowed to insert a wait state during the initial block of read transaction. However, it may insert wait states after each block transfer. There is no GFRAMEJ IRDYJ relationship for A.G.P. transactions. When a PCI transaction is proceeded at AGP bus, this signal is the same definition of PCI spec.V2.1.
GTRDYJ	I/O Group B	New meaning. GTRDYJ indicates the A.G.P. compliant target is ready to provide read data for the entire transaction (When transaction can complete within four clocks) a block or is ready to transfer a (initial or subsequent) block of data, when the transfer required more than four clocks to complete. The target is allowed to insert wait states after each block transfer on both read and write transactions.
GSTOPJ	I/O Group B	**Stop**. Not used by A.G.P. Only used during PCI operation on A.G.P. This signal indicates the target is requesting the master to stop the current transaction.

GREQJ	I Group B	**Bus Request signals of PCI Masters**. Same as PCI. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter. As AGP signal, it is used to request bus ownership when PIPEJ (not SBA[7:0]) is used to enqueue AGP request.
GGNTJ	O Group B	**Grant signals to PCI Masters**. Same meaning as PCI. When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus. Additional information is provided on ST[2:0]. The additional information indicates that the master is the recipient of previously requested read data (high or low priority), it is to provided write data (high or low priority), for a previously enqueued write command or has been given permission to start a bus transaction (A.G.P. or PCI)
GPAR	I/O Group B	**Parity bit of PCI bus**. Not used by A.G.P. Used during PCI operation on A.G.P.. It is the even parity bit across GAD[31:0] and GCBEJ[3:0].
GSERRJ	I Group B	**System Error.** Same as PCI. Maybe used by an A.G.P. compliant master to report a catastrophic error when the core logic supports a GSERRJ pin for the A.G.P. port.
GPERRJ	O Group B	**Parity Error**. Not used by A.G.P. For PCI operation per exception granted by PCI 2.1 specification.
GCLKIN	I/O Group B	**Clock** provides timing for A.G.P and PCI operation on A.G.P.

Pin Description Table (continued)

Pin Name	Type	Description
Power Pins		
VDD_A	P	**VDD 3.3V or 2.5V Power for CPU interface Group_A.** This power is used for CPU interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VDD_B	P	**VDD 3.3V Power for Group_B.** This power is used for AGP interface, PCI interface, Tag interface, L2 cache control signals and internal core circuit. It must connect to 3.3V.
VDD_C	P	**VDD 3.3V Power for Memory interface for Group_C.** This power is used for DRAM interface signals during normal operation and suspend refresh. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.
VDD_5	P	**VDD 5.0V Power for Group B.** This pin supplies the 5V input tolerance circuit.
VDD_5S	P	**VDD 5.0V Power for Group C.** This pin supplies the memory interface 5V input tolerance circuit.
VDD_P	P	**PLL analog 3.3V VDD : for internal PLL VDD 3.3V.**
VSS_P	P	**PLL analog 3.3V VSS : for internal PLL VSS.**
Vref	P	**Reference voltage for A.G.P. interface :** Input reference voltage for differential input. It equals to 0.4VDD_B.
Vss	P	**Ground.**

2.3 Numerical Pin List

Pin No.	Name	Type
A1	HD35	I/O
A2	HD37	I/O
A3	HD40	I/O
A4	HD43	I/O
A5	HD46	I/O
A6	HD50	I/O
A7	HD54	I/O
A8	HD59	I/O
A9	WRJ	I
A10	NAJ	O
A11	ADSJ	I
A12	BEJ5	I
A13	BEJ0	I
A14	GWEJ	O
A15	CADVJ	O
A16	CADSJ	O
A17	TIO5	I/O
A18	TIO8	I/O
A19	TAGWEJ	O
A20	MD5	I/O
A21	MD7	I/O
A22	MD9	I/O
A23	MD11	I/O
A24	MD45	I/O
A25	MD46	I/O
A26	NC	-
B1	HD34	I/O
B2	NC	-
B3	HD39	I/O
B4	HD42	I/O
B5	HD45	I/O
B6	HD49	I/O
B7	HD53	I/O
B8	HD58	I/O
B9	HD63	I/O
B10	KENJ	O
B11	HLOCKJ	I
B12	BEJ6	I
B13	BEJ1	I
B14	BWEJ	O
B15	CCSJ	O
B16	TIO3	I/O
B17	TIO6	I/O
B18	TIO9	I/O
B19	MD3	I/O
B20	MD38	I/O
B21	MD40	I/O
B22	MD42	I/O
B23	MD44	I/O
B24	NC	-
B25	MD13	I/O
B26	MD14	I/O
C1	HD33	I/O
C2	HD36	I/O
C3	HD38	I/O
C4	HD41	I/O
C5	HD44	I/O
C6	HD48	I/O
C7	HD52	I/O
C8	HD57	I/O
C9	HD62	I/O
C10	AHOLD	O
C11	EADSJ	O
C12	BEJ7	I
C13	BEJ2	I
C14	COEJ	O
C15	TIO0	I/O
C16	TIO4	I/O
C17	TIO7	I/O
C18	MD34	I/O
C19	MD36	I/O
C20	MD6	I/O
C21	MD8	I/O
C22	MD10	I/O
C23	MA14	I/O
C24	NC	-
C25	MD47	I/O
C26	MD15	I/O
D1	HD30	I/O
D2	HD31	I/O
D3	HD32	I/O

D4	NC	-
D5	NC	-
D6	HD47	I/O
D7	HD51	I/O
D8	HD56	I/O
D9	HD61	I/O
D10	CACHEJ	I
D11	BOFFJ	O
D12	HITMJ	I
D13	BEJ3	I
D14	TIO1	I/O
D15	HCLKIN	I
D16	MD32	I/O
D17	MD33	I/O
D18	MD2	I/O
D19	MD4	I/O
D20	MD39	I/O
D21	MD41	I/O
D22	MD43	I/O

Pin No.	Name	Type
D23	MD12	I/O
D24	SCASJ2	O
D25	SCASJ1	O
D26	SCASJ0	O
E1	HD27	I/O
E2	HD26	I/O
E3	HD28	I/O
E4	HD29	I/O
E5	VDD_A	P
E6	VDD_A	P
E7	VSS_P	P
E8	HD55	I/O
E9	HD60	I/O
E10	MIOJ	I
E11	BRDYJ	O
E12	DCJ	I
E13	BEJ4	I
E14	MKREFRQJ	I/O
E15	TIO2	I/O
E16	MD0	I/O
E17	MD1	I/O
E18	MD35	I/O
E19	MD37	I/O
E20	VDD_P	P
E21	VDD_P	P
E22	VDD_C	P
E23	SCASJ3	O
E24	CASJ1	O
E25	CASJ4	O
E26	CASJ0	O

F1	HD24	I/O
F2	HD23	I/O
F3	HD22	I/O
F4	HD25	I/O
F5	VDD_A	P
F22	VDD_C	P
F23	RASJ2	O
F24	RASJ1	O
F25	RASJ0	O
F26	CASJ5	O
G1	HD21	I/O
G2	HD20	I/O
G3	HD19	I/O
G4	HD18	I/O
G5	VDD_B	P
G22	VDD_5S	P
G23	RASJ6	O
G24	RASJ5	O
G25	RASJ4	O
G26	RASJ3	O

Pin No.	Name	Type
H1	HD17	I/O
H2	HD16	I/O
H3	HD15	I/O
H4	HD14	I/O
H5	HD13	I/O
H22	SRASJ3	O
H23	SRASJ2	O
H24	SRASJ1	O
H25	SRASJ0	O
H26	RASJ7	O
J1	HD12	I/O
J2	HD11	I/O
J3	HD10	I/O
J4	HD9	I/O
J5	HD8	I/O
J22	MA4	O
J23	MA3	O
J24	MA2	O
J25	MA1	O
J26	MA0	O
K1	HD7	I/O
K2	HD6	I/O
K3	HD5	I/O
K4	HD4	I/O
K5	HD3	I/O
K22	MA9	O
K23	MA8	O
K24	MA7	O
K25	MA6	O
K26	MA5	O
L1	HD2	I/O
L2	HD1	I/O
L3	HD0	I/O
L4	HA18	I/O
L5	SMIACTJ	I
L11	VSS	P
L12	VSS	P
L13	VSS	P
L14	VSS	P
L15	VSS	P
L16	VSS	P
L22	CLKEN6	O
L23	MA13	O
L24	MA12	O
L25	MA11	O
L26	MA10	O
M1	HA17	I/O
M2	HA16	I/O
M3	HA15	I/O
M4	HA14	I/O

Pin No.	Name	Type
M5	HA13	I/O
M11	VSS	P
M12	VSS	P
M13	VSS	P
M14	VSS	P
M15	VSS	P
M16	VSS	P
M22	MPD1	I/O
M23	MPD5	I/O
M24	CLKEN0	O
M25	CLKEN2	O
M26	CLKEN4	O
N1	HA12	I/O
N2	HA11	I/O
N3	HA10	I/O
N4	HA9	I/O
N5	HA8	I/O
N11	VSS	P
N12	VSS	P
N13	VSS	P
N14	VSS	P
N15	VSS	P
N16	VSS	P
N22	MPD7	I/O
N23	MPD2	I/O
N24	MPD6	I/O
N25	MPD0	I/O
N26	MPD4	I/O
P1	HA7	I/O
P2	HA6	I/O
P3	HA5	I/O

P4	HA4	I/O
P5	HA3	I/O
P11	VSS	P
P12	VSS	P
P13	VSS	P
P14	VSS	P
P15	VSS	P
P16	VSS	P
P22	DPLLO	O
P23	CASJ2	O
P24	CASJ6	O
P25	MPD3	I/O
P26	DPLLI1	I
R1	HA19	I/O
R2	HA20	I/O
R3	HA21	I/O
R4	HA22	I/O
R5	HA23	I/O
R11	VSS	P

Pin No.	**Name**	**Type**
R12	VSS	P
R13	VSS	P
R14	VSS	P
R15	VSS	P
R16	VSS	P
R22	MWEJ1	O
R23	MWEJ0	O
R24	CASJ3	O
R25	MWEJ2	O
R26	DPLLI0	I
T1	HA24	I/O
T2	HA25	I/O
T3	HA26	I/O
T4	GNTJ4	O
T5	REQJ4	I
T11	VSS	P
T12	VSS	P
T13	VSS	P
T14	VSS	P
T15	VSS	P
T16	VSS	P
T22	MD48	I/O
T23	ECASJ1	O
T24	ECASJ5	O
T25	MWEJ3	O
T26	CASJ7	O
U1	HA27	I/O
U2	HA28	I/O
U3	HA29	I/O
U4	GNTJ3	O

U5	REQJ3	I
U22	MD18	I/O
U23	MD50	I/O
U24	MD17	I/O
U25	MD49	I/O
U26	MD16	I/O
V1	HA30	I/O
V2	GNTJ2	O
V3	REQJ2	I
V4	GNTJ1	O
V5	REQJ1	I
V22	CLKEN1	O
V23	MD20	I/O
V24	MD52	I/O
V25	MD19	I/O
V26	MD51	I/O
W1	HA31	I/O
W2	AD31	I/O
W3	GNTJ0	O
W4	REQJ0	I

Pin No.	Name	Type
W5	PHLDJ	I
W22	OSC32KI	I
W23	MD53	I/O
W24	CLKEN7	O
W25	CLKEN5	O
W26	CLKEN3	O
Y1	AD30	I/O
Y2	AD29	I/O
Y3	AD28	I/O
Y4	AD27	I/O
Y5	VDD_5	P
Y22	VDD_C	P
Y23	MD55	I/O
Y24	MD22	I/O
Y25	MD54	I/O
Y26	MD21	I/O
AA1	AD26	I/O
AA2	AD25	I/O
AA3	AD24	I/O
AA4	CBEJ3	I/O
AA5	VDD_B	P
AA22	VDD_C	P
AA23	MD57	I/O
AA24	MD24	I/O
AA25	MD56	I/O
AA26	MD23	I/O
AB1	AD23	I/O
AB2	AD22	I/O
AB3	AD21	I/O
AB4	AD20	I/O
AB5	VDD_B	P

AB6	VDD_B	P
AB7	VDD_B	P
AB8	PCIMRQJ	O
AB9	RSTJ	I
AB10	AD0	I/O
AB11	PCICLK	I
AB12	SBA5	O
AB13	GAD29	I/O
AB14	GAD24	I/O
AB15	GAD21	I/O
AB16	GAD16	I/O
AB17	GTRDYJ	I/O
AB18	GCLKIN	I
AB19	GAD12	I/O
AB20	Vref	P
AB21	VDD_P	P
AB22	VSS_P	P
AB23	MD59	I/O
AB24	MD26	I/O

Pin No.	Name	Type
AB25	MD58	I/O
AB26	MD25	I/O
AC1	AD19	I/O
AC2	AD18	I/O
AC3	AD17	I/O
AC4	AD16	I/O
AC5	AD14	I/O
AC6	AD10	I/O
AC7	AD7	I/O
AC8	AD4	I/O
AC9	AD2	I/O
AC10	AD1	I/O
AC11	PHLDAJ	O
AC12	SBA4	O
AC13	GAD30	I/O
AC14	GAD25	I/O
AC15	GAD22	I/O
AC16	GAD17	I/O
AC17	GDEVSELJ	I/O
AC18	GPAR	I/O
AC19	GAD13	I/O
AC20	GAD8	I/O
AC21	GAD6	I/O
AC22	NC	-
AC23	NC	-
AC24	MD28	I/O
AC25	MD60	I/O
AC26	MD27	I/O
AD1	CBEJ2	I/O
AD2	FRAMEJ	I/O
AD3	NC	-

AD4	NC	
AD5	AD15	I/O
AD6	AD11	I/O
AD7	CBEJ0	I/O
AD8	AD5	I/O
AD9	AD3	I/O
AD10	RBFJ	I
AD11	SBA1	O
AD12	SB_STB	I
AD13	GAD31	I/O
AD14	GAD26	I/O
AD15	GAD23	I/O
AD16	GAD18	I/O
AD17	GFRAMEJ	I/O
AD18	GSERRJ	I
AD19	GAD14	I/O
AD20	GAD9	I/O
AD21	GAD7	I/O
AD22	GAD3	I/O

Pin No.	**Name**	**Type**
AD23	TESTJ	I/O
AD24	SUSPENDJ	I
AD25	MD61	I/O
AD26	MD29	I/O
AE1	IRDYJ	I/O
AE2	TRDYJ	I/O
AE3	NC	
AE4	DEVSELJ	I/O
AE5	CBEJ1	I/O
AE6	AD12	I/O
AE7	AD8	I/O
AE8	AD6	I/O
AE9	ST0	O
AE10	ST2	O
AE11	SBA0	O
AE12	SBA3	O
AE13	SBA7	O
AE14	GAD27	I/O
AE15	GCBEJ3	I/O
AE16	GAD19	I/O
AE17	GIRDYJ	I/O
AE18	GPERRJ	O
AE19	GAD15	I/O
AE20	GAD10	I/O
AE21	AD_STB0	I/O
AE22	GAD4	I/O
AE23	MD63	I/O
AE24	MD30	I/O
AE25	NC	
AE26	MD62	I/O

AF1	NC	
AF2	STOPJ	I/O
AF3	LOCKJ	I/O
AF4	SERRJ	O
AF5	PAR	I/O
AF6	AD13	I/O
AF7	AD9	I/O
AF8	GREQJ	I
AF9	GGNTJ	O
AF10	ST1	O
AF11	PIPEJ	I
AF12	SBA2	O
AF13	SBA6	O
AF14	GAD28	I/O
AF15	AD_STB1	I/O
AF16	GAD20	I/O
AF17	GCBEJ2	I/O
AF18	GSTOPJ	I/O
AF19	GCBEJ1	I/O
AF20	GAD11	I/O

Pin No.	Name	Type
AF21	GCBEJ0	I/O
AF22	GAD5	I/O
AF23	GAD2	I/O
AF24	GAD1	I/O
AF25	GAD0	I/O
AF26	MD31	I/O

2.4 Alphabetical Pin List

Pin No.	Name	Type
AE21	AD_STB0	I/O
AF15	AD_STB1	I/O
AB10	AD0	I/O
AC10	AD1	I/O
AC6	AD10	I/O
AD6	AD11	I/O
AE6	AD12	I/O
AF6	AD13	I/O
AC5	AD14	I/O
AD5	AD15	I/O
AC4	AD16	I/O
AC3	AD17	I/O
AC2	AD18	I/O
AC1	AD19	I/O
AC9	AD2	I/O
AB4	AD20	I/O
AB3	AD21	I/O
AB2	AD22	I/O
AB1	AD23	I/O
AA3	AD24	I/O
AA2	AD25	I/O
AA1	AD26	I/O
Y4	AD27	I/O
Y3	AD28	I/O
Y2	AD29	I/O
AD9	AD3	I/O
Y1	AD30	I/O
W2	AD31	I/O
AC8	AD4	I/O
AD8	AD5	I/O
AE8	AD6	I/O

AC7	AD7	I/O
AE7	AD8	I/O
AF7	AD9	I/O
A11	ADSJ	I
C10	AHOLD	O
A13	BEJ0	I
B13	BEJ1	I
C13	BEJ2	I
D13	BEJ3	I
E13	BEJ4	I
A12	BEJ5	I
B12	BEJ6	I
C12	BEJ7	I
D11	BOFFJ	O
E11	BRDYJ	O
B14	BWEJ	O
D10	CACHEJ	I
A16	CADSJ	O
A15	CADVJ	O

Pin No.	Name	Type
E26	CASJ0	O
E24	CASJ1	O
P23	CASJ2	O
R24	CASJ3	O
E25	CASJ4	O
F26	CASJ5	O
P24	CASJ6	O
T26	CASJ7	O
AD7	CBEJ0	I/O
AE5	CBEJ1	I/O
AD1	CBEJ2	I/O
AA4	CBEJ3	I/O
B15	CCSJ	O
M24	CLKEN0	O
V22	CLKEN1	O
M25	CLKEN2	O
W26	CLKEN3	O
M26	CLKEN4	O
W25	CLKEN5	O
L22	CLKEN6	O
W24	CLKEN7	O
C14	COEJ	O
E12	DCJ	I
AE4	DEVSELJ	I/O
R26	DPLLI0	I
P26	DPLLI1	I
P22	DPLLO	O
C11	EADSJ	O
T23	ECASJ1	O
T24	ECASJ5	O

AD2	FRAMEJ	I/O
AF25	GAD0	I/O
AF24	GAD1	I/O
AE20	GAD10	I/O
AF20	GAD11	I/O
AB19	GAD12	I/O
AC19	GAD13	I/O
AD19	GAD14	I/O
AE19	GAD15	I/O
AB16	GAD16	I/O
AC16	GAD17	I/O
AD16	GAD18	I/O
AE16	GAD19	I/O
AF23	GAD2	I/O
AF16	GAD20	I/O
AB15	GAD21	I/O
AC15	GAD22	I/O
AD15	GAD23	I/O
AB14	GAD24	I/O
AC14	GAD25	I/O

Pin No.	Name	Type
AD14	GAD26	I/O
AE14	GAD27	I/O
AF14	GAD28	I/O
AB13	GAD29	I/O
AD22	GAD3	I/O
AC13	GAD30	I/O
AD13	GAD31	I/O
AE22	GAD4	I/O
AF22	GAD5	I/O
AC21	GAD6	I/O
AD21	GAD7	I/O
AC20	GAD8	I/O
AD20	GAD9	I/O
AF21	GCBEJ0	I/O
AF19	GCBEJ1	I/O
AF17	GCBEJ2	I/O
AE15	GCBEJ3	I/O
AB18	GCLKIN	I
AC17	GDEVSELJ	I/O
AD17	GFRAMEJ	I/O
AF9	GGNTJ	O
AE17	GIRDYJ	I/O
W3	GNTJ0	O
V4	GNTJ1	O
V2	GNTJ2	O
U4	GNTJ3	O
T4	GNTJ4	O
AC18	GPAR	I/O
AE18	GPERRJ	O
AF8	GREQJ	I

Pin No.	Name	Type
AD18	GSERRJ	I
AF18	GSTOPJ	I/O
AB17	GTRDYJ	I/O
A14	GWEJ	O
N3	HA10	I/O
N2	HA11	I/O
N1	HA12	I/O
M5	HA13	I/O
M4	HA14	I/O
M3	HA15	I/O
M2	HA16	I/O
M1	HA17	I/O
L4	HA18	I/O
R1	HA19	I/O
R2	HA20	I/O
R3	HA21	I/O
R4	HA22	I/O
R5	HA23	I/O
T1	HA24	I/O
T2	HA25	I/O
T3	HA26	I/O
U1	HA27	I/O
U2	HA28	I/O
U3	HA29	I/O
P5	HA3	I/O
V1	HA30	I/O
W1	HA31	I/O
P4	HA4	I/O
P3	HA5	I/O
P2	HA6	I/O
P1	HA7	I/O
N5	HA8	I/O
N4	HA9	I/O
D15	HCLKIN	I
L3	HD0	I/O
L2	HD1	I/O
J3	HD10	I/O
J2	HD11	I/O
J1	HD12	I/O
H5	HD13	I/O
H4	HD14	I/O
H3	HD15	I/O
H2	HD16	I/O
H1	HD17	I/O
G4	HD18	I/O
G3	HD19	I/O
L1	HD2	I/O
G2	HD20	I/O
G1	HD21	I/O
F3	HD22	I/O
F2	HD23	I/O
F1	HD24	I/O
F4	HD25	I/O
E2	HD26	I/O
E1	HD27	I/O
E3	HD28	I/O
E4	HD29	I/O
K5	HD3	I/O
D1	HD30	I/O
D2	HD31	I/O
D3	HD32	I/O
C1	HD33	I/O
B1	HD34	I/O
A1	HD35	I/O
C2	HD36	I/O
A2	HD37	I/O
C3	HD38	I/O
B3	HD39	I/O
K4	HD4	I/O
A3	HD40	I/O

Pin No.	Name	Type
C4	HD41	I/O
B4	HD42	I/O
A4	HD43	I/O
C5	HD44	I/O
B5	HD45	I/O
A5	HD46	I/O
D6	HD47	I/O
C6	HD48	I/O
B6	HD49	I/O
K3	HD5	I/O
A6	HD50	I/O
D7	HD51	I/O
C7	HD52	I/O
B7	HD53	I/O
A7	HD54	I/O
E8	HD55	I/O
D8	HD56	I/O
C8	HD57	I/O
B8	HD58	I/O
A8	HD59	I/O
K2	HD6	I/O
E9	HD60	I/O
D9	HD61	I/O
C9	HD62	I/O
B9	HD63	I/O
K1	HD7	I/O
J5	HD8	I/O
J4	HD9	I/O
D12	HITMJ	I
B11	HLOCKJ	I

AE1	IRDYJ	I/O
B10	KENJ	O
AF3	LOCKJ	I/O
J26	MA0	O
J25	MA1	O
L26	MA10	O
L25	MA11	O
L24	MA12	O
L23	MA13	O
C23	MA14	I/O
J24	MA2	O
J23	MA3	O
J22	MA4	O
K26	MA5	O
K25	MA6	O
K24	MA7	O
K23	MA8	O
K22	MA9	O
E16	MD0	I/O
E17	MD1	I/O

Pin No.	Name	Type
C22	MD10	I/O
A23	MD11	I/O
D23	MD12	I/O
B25	MD13	I/O
B26	MD14	I/O
C26	MD15	I/O
U26	MD16	I/O
U24	MD17	I/O
U22	MD18	I/O
V25	MD19	I/O
D18	MD2	I/O
V23	MD20	I/O
Y26	MD21	I/O
Y24	MD22	I/O
AA26	MD23	I/O
AA24	MD24	I/O
AB26	MD25	I/O
AB24	MD26	I/O
AC26	MD27	I/O
AC24	MD28	I/O
AD26	MD29	I/O
B19	MD3	I/O
AE24	MD30	I/O
AF26	MD31	I/O
D16	MD32	I/O
D17	MD33	I/O
C18	MD34	I/O
E18	MD35	I/O
C19	MD36	I/O
E19	MD37	I/O

B20	MD38	I/O
D20	MD39	I/O
D19	MD4	I/O
B21	MD40	I/O
D21	MD41	I/O
B22	MD42	I/O
D22	MD43	I/O
B23	MD44	I/O
A24	MD45	I/O
A25	MD46	I/O
C25	MD47	I/O
T22	MD48	I/O
U25	MD49	I/O
A20	MD5	I/O
U23	MD50	I/O
V26	MD51	I/O
V24	MD52	I/O
W23	MD53	I/O
Y25	MD54	I/O
Y23	MD55	I/O

Pin No.	**Name**	**Type**
AA25	MD56	I/O
AA23	MD57	I/O
AB25	MD58	I/O
AB23	MD59	I/O
C20	MD6	I/O
AC25	MD60	I/O
AD25	MD61	I/O
AE26	MD62	I/O
AE23	MD63	I/O
A21	MD7	I/O
C21	MD8	I/O
A22	MD9	I/O
E10	MIOJ	I
E14	MKREFRQJ	I/O
N25	MPD0	I/O
M22	MPD1	I/O
N23	MPD2	I/O
P25	MPD3	I/O
N26	MPD4	I/O
M23	MPD5	I/O
N24	MPD6	I/O
N22	MPD7	I/O
R23	MWEJ0	O
R22	MWEJ1	O
R25	MWEJ2	O
T25	MWEJ3	O
A10	NAJ	O
A26	NC	
AC22	NC	-
AC23	NC	-
AD3	NC	-

AD4	NC	-
AE25	NC	-
AE3	NC	-
AF1	NC	-
B2	NC	-
B24	NC	-
C24	NC	-
D4	NC	-
D5	NC	-
W22	OSC32KI	I
AF5	PAR	I/O
AB11	PCICLK	I
AB8	PCIMRQJ	O
AC11	PHLDAJ	O
W5	PHLDJ	I
AF11	PIPEJ	I
F25	RASJ0	O
F24	RASJ1	O
F23	RASJ2	O

Pin No.	Name	Type
G26	RASJ3	O
G25	RASJ4	O
G24	RASJ5	O
G23	RASJ6	O
H26	RASJ7	O
AD10	RBFJ	I
W4	REQJ0	I
V5	REQJ1	I
V3	REQJ2	I
U5	REQJ3	I
T5	REQJ4	I
AB9	RSTJ	I
AD12	SB_STB	I
AE11	SBA0	O
AD11	SBA1	O
AF12	SBA2	O
AE12	SBA3	O
AC12	SBA4	O
AB12	SBA5	O
AF13	SBA6	O
AE13	SBA7	O
D26	SCASJ0	O
D25	SCASJ1	O
D24	SCASJ2	O
E23	SCASJ3	O
AF4	SERRJ	O
L5	SMIACTJ	I
H25	SRASJ0	O
H24	SRASJ1	O
H23	SRASJ2	O

H22	SRASJ3	O
AE9	ST0	O
AF10	ST1	O
AE10	ST2	O
AF2	STOPJ	I/O
AD24	SUSPENDJ	I
A19	TAGWEJ	O
AD23	TESTJ	I/O
C15	TIO0	I/O
D14	TIO1	I/O
E15	TIO2	I/O
B16	TIO3	I/O
C16	TIO4	I/O
A17	TIO5	I/O
B17	TIO6	I/O
C17	TIO7	I/O
A18	TIO8	I/O
B18	TIO9	I/O
AE2	TRDYJ	I/O
Y5	VDD_5	P

Pin No.	Name	Type
G22	VDD_5S	P
E5	VDD_A	P
E6	VDD_A	P
F5	VDD_A	P
AA5	VDD_B	P
AB5	VDD_B	P
AB6	VDD_B	P
AB7	VDD_B	P
G5	VDD_B	P
AA22	VDD_C	P
E22	VDD_C	P
F22	VDD_C	P
Y22	VDD_C	P
AB21	VDD_P	P
E20	VDD_P	P
E21	VDD_P	P
AB20	Vref	P
L11	VSS	P
L12	VSS	P
L13	VSS	P
L14	VSS	P
L15	VSS	P
L16	VSS	P
M11	VSS	P
M12	VSS	P
M13	VSS	P
M14	VSS	P
M15	VSS	P
M16	VSS	P
N11	VSS	P

N12	VSS	P
N13	VSS	P
N14	VSS	P
N15	VSS	P
N16	VSS	P
P11	VSS	P
P12	VSS	P
P13	VSS	P
P14	VSS	P
P15	VSS	P
P16	VSS	P
R11	VSS	P
R12	VSS	P
R13	VSS	P
R14	VSS	P
R15	VSS	P
R16	VSS	P
T11	VSS	P
T12	VSS	P
T13	VSS	P

Pin No.	**Name**	**Type**
T14	VSS	P
T15	VSS	P
T16	VSS	P
AB22	VSS_P	P
E7	VSS_P	P
A9	WRJ	I

Section 3 : Function Description

3.1 System Architecture

In the following illustration, ALADDIN-V gives a highly integrated system solution and a most up-to-date system architecture, which includes the Accelerated Graphics Port, .Parity/ECC, PBSRAM/Memory Cache, SDRAM, ACPI, Ultra-33 IDE Master, USB, PS2 Keyboard/Mouse, and highly concurrent multi-bus with smart deep FIFO between the buses, such as the HOST/ A.G.P./ DRAM/ PCI/ ISA/ DEDICATED IDE/USB buses. Using ALADDIN-V, you can achieve a TTL free solution and provide the best system performance.

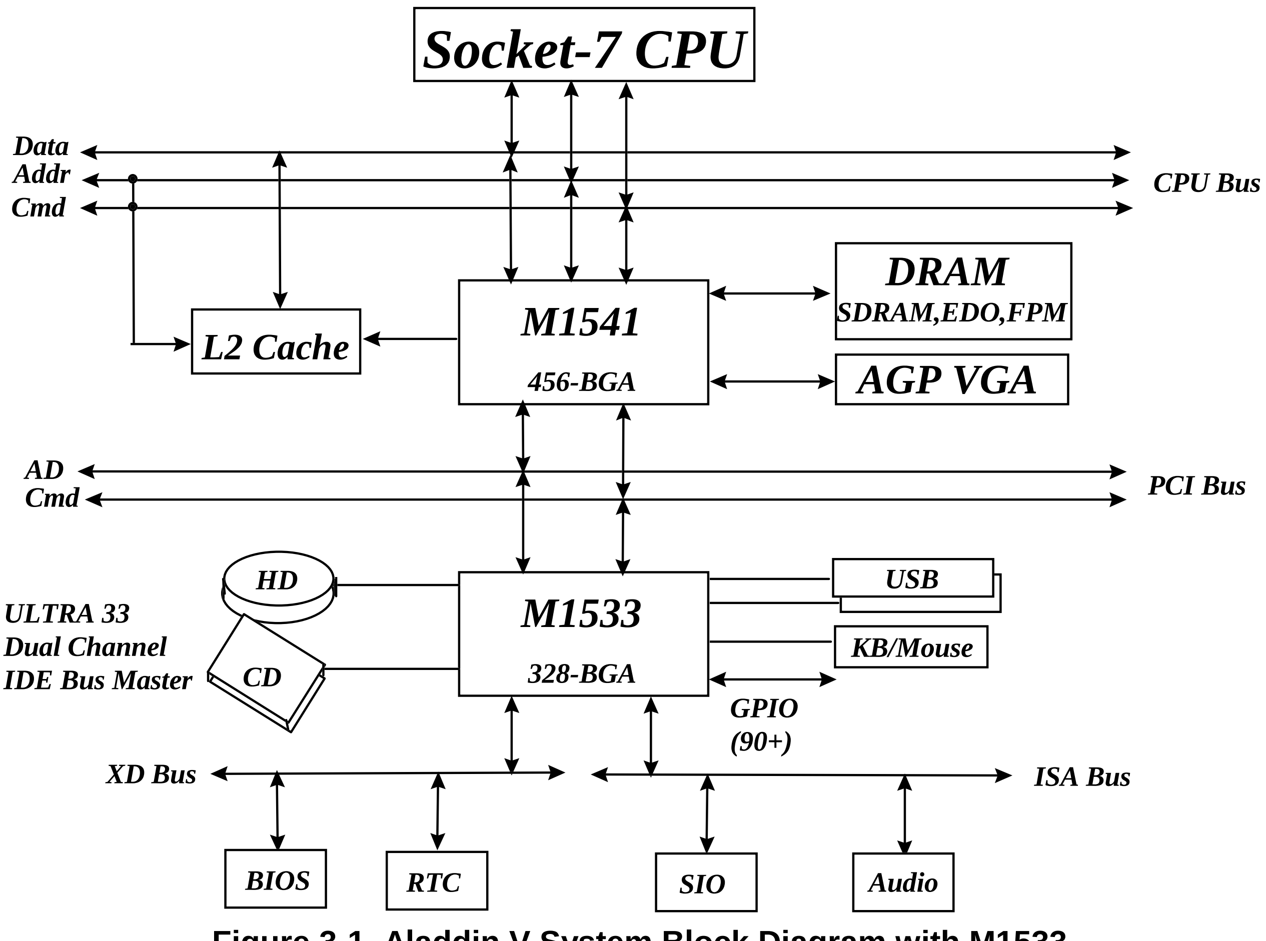


Figure 3-1. Aladdin V System Block Diagram with M1533

As the North bridge, the M1541 provides a complete integrated solution for the system controller and data path components in a socket-7 processor system. It provides a 64-bit CPU bus interface, AGP bus interface, 32-bit PCI bus interface, 64/72 DRAM data bus with ECC or parity, secondary cache interface including Pipelined Burst SRAM or Memory Cache, PCI master to DRAM interface, and 5 PCI masters, CPU, and M1533/M1543 arbiter. The following figure shows the highly efficient data path in the M1541. The M1541 bus interfaces are designed to interface with 2.5V, 3.3V and 5V buses. It directly connects to 3.3V or 2.5V CPU bus, 3.3V or 5V Tag, 3.3V or 5V DRAM bus, and 3.3V or 5V PCI bus.

The M1533 provides a highly integrated PCI-to-ISA bridge solution for the best Notebook system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, and Enhanced Green function.

The M1543 provides a highly integrated PCI-to-ISA bridge solution for the best Desktop system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, Green function, and the Super I/O function.

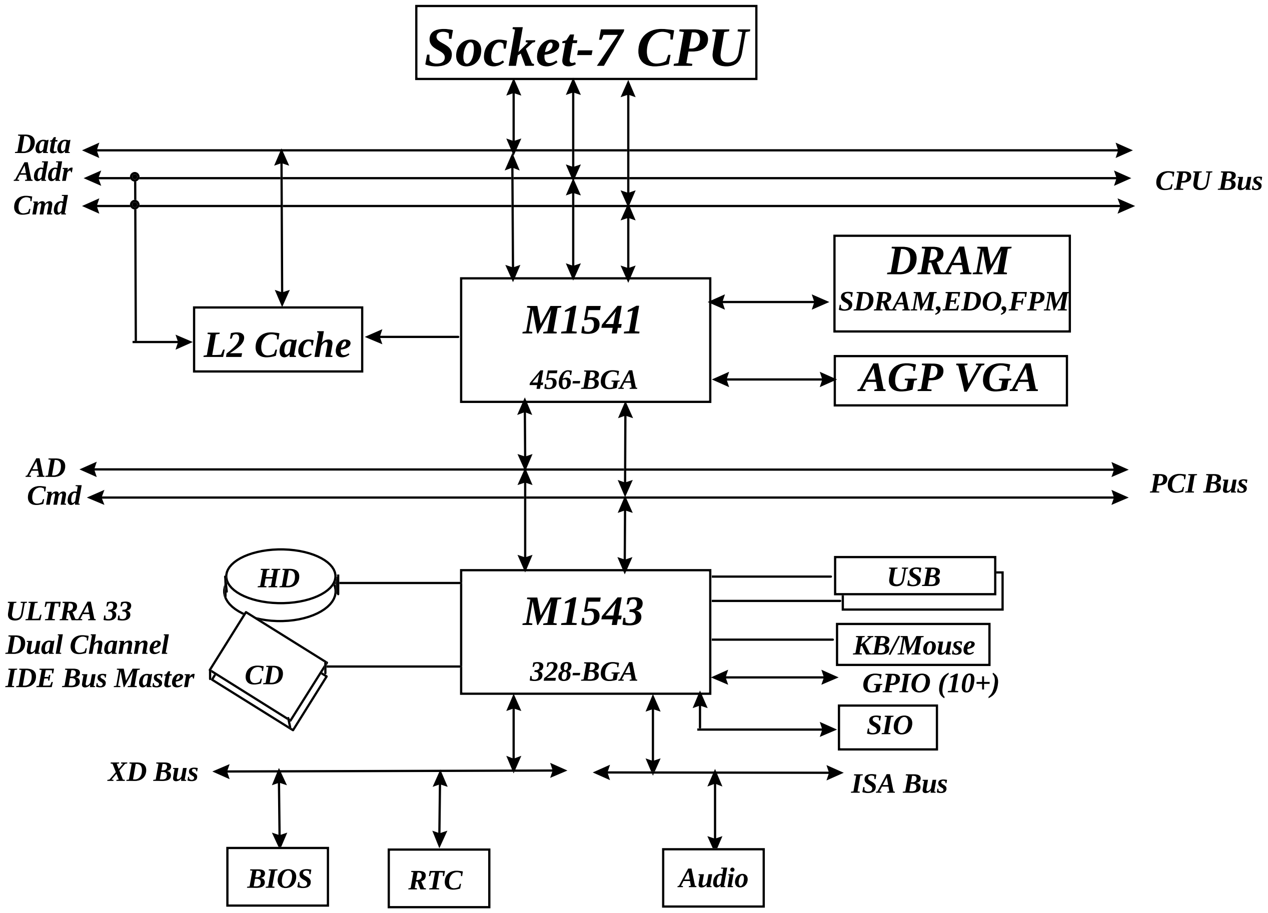


Figure 3-2. Aladdin V System Block Diagram with M1543

3.2 Data Path and Buffer Architecture

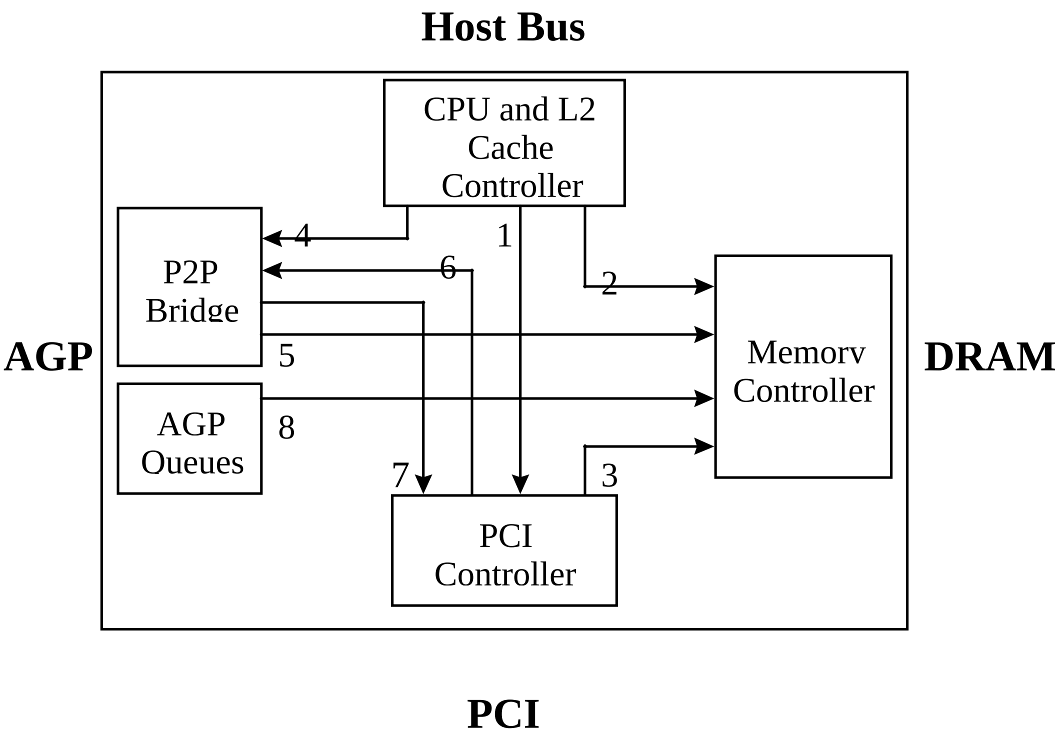


Figure 3-3. Data Path and Buffer Architecture

1 : CPU to PCI – 6 DWORDs memory write buffer

2 : CPU to Memory – 32 QWORDs write buffer

3 : PCI to Memory – 80 DWORDs write posted buffer & 22 DWORDs read pre-fetch buffer

4 : CPU to AGP – 8 DWORDs posted write buffer

5 : PCI_66 to Memory – 40 QWORDs write buffer and 32 QWORDs read buffer

6 : PCI to AGP - 8 DWORDs write posted buffer

7 : PCI_66 to PCI - 2 DWORDs write posted buffer

8 : AGP to Memory – 16 QWORDs write buffer and 32 QWORDs read buffer

3.3 CPU Interface

The M1541 supports all Pentium-class CPUs including Intel P54C/P55C, Cyrix M1/M2, AMD K5/K6. Furthermore, M1541 supports a high performance CPU interface with bus frequency up to 100 MHz to achieve the Pentium II-class system performance. M1541 also supports Cyrix Linear Wrap mode for M1 and M2 to gain the best system performance. M1541 can also interface to 2.5V CPU I/O interface for Notebook use. In higher CPU bus frequency interface, M1541 will do the so-called pseudo-synchronous design instead of the asynchronous design. When 75/83.3/100 MHz CPU bus is used, the PCI bus will be running at 30/33/33 MHz (divide CPU bus by 2/2.5/3). The pseudo-synchronous clock design is a better solution than the pure asynchronous clock design, it eliminates the performance degradation to synchronize two asynchronous buses and helps the chip reliability to resolve the chip testing issue.

3.4 Clock Design Philosophy

The system provides 4 clocks (HCLKIN, PCICLK, CLK32KI, GCLKIN) for M1541, HCLKIN has the same frequency with the CPUCLK, Cache clock, and SDRAM clock. PCICLK has the same frequency with the PCI bus clock, and CLK32KI is a 32.768KHz frequency clock from M1533/M1543 CLK32KO or from the system board clock source. GCLKIN provides the clock source of A.G.P. and PCI operation on A.G.P.

System designer should minimize the clock skew between CPUCLK, Cache clock, SDRAM clock, and HCLKIN, and also the skew between PCICLK and PCI bus clock. Regarding the skew between M1541 HCLKIN and PCICLK, PCICLK should lag HCLKIN for 1 ~ 4 ns. The internal clock design philosophy uses the HCLKIN running the state machine of CPU interface, L2 controller, and DRAM controller, and uses the PCICLK running the PCI state machine, and automatically takes good care of the internal signal interface between different clock frequency state machines. Also M1541 will support the internal smart clock control, it will shut off the internal clock when the CPU or PCI bus is idle to save the power consumption. CLK32KI clock is used for the DRAM Suspend refresh clock. It is a clock input and not necessarily relative to HCLKIN or PCICLK.

3.5 Cache Memory Timing/Configuration

The M1541 integrates a high performance L2 write back/dynamic-write-back direct mapping cache controller using MESI protocol of L1 and L2, and has an L2 MESI tag 16K2 bits built-in to maintain the data coherence for optimizing CPU bus utilization. The L2 cache can be configured for Memory Cache or Pipelined Burst SRAM with cache size ranging from 256KB, 512KB to 1MB. The cacheable region can be up to 1GB under 256KB L2 cache memory configuration, by using 8K10 tag RAM or two 8K8 tag RAM option. When using an 8K8 tag RAM under 256KB L2 cache , the cacheable region of the system is 256MB. The controller can perform a dynamic-write-back cycle to DRAM, which the L1 write cycle will be directed to DRAM intelligently with 3-1-1-1 timing without stalling the CPU execution. Also M1541 can support the CPU single read cycle L2 allocation feature, M1541 will do the L2 line fill even when the CPU issues only a single read cycle to improve the L2 hit rate for some special application. The following table shows the best performance for the L2 Read/Write access.

The timing of cache memory system is shown in following table :

Table 3-1

	READ	WRITE	B2B READ	B2B WRITE
PBSRAM and Memory cache	3-1-1-1	3-1-1-1	3-1-1-1-1-1-1-1	3-1-1-1-1-1-1-1

The following L2 Cache Table shows the different configurations supported by M1541.

Table 3-2

Config	DATA SRAM			External TAG SRAM				Internal MESI 8K1x4	Note
Cache Size	**Size**	**Bank**	**Address lines**	**Address lines**	**Data Lines**	**Ext. Tag Size**	**Cacheable DRAM Size**		
256K	(32K32)*2 or (32K64)*1	1	A3-A17	A5-A17	A18-A25	8K8	64M	8K2 MESI	
512K	(64K32)*2 or (64K64)*1	1	A3-A18	A5-A18	A19-A26	16K8	128M	16K2 MESI	
512K	(32K64)*2 (32K32)*4	2	A3-A18	A5-A18	A19-A26	16K8	128M	16K2 MESI	
1M	(64K32)*4 or (64K64)*2	2	A3-A19	A5-A19	A20-A26	32K8	128M	32K1 as dirty bit	TAG[7] as valid bit.
256K	(32K32)*2 or (32K64)*1	1	A3-A17	A5-A17	A18-A27	8K10	256M	8K2 MESI	
512K	(64K32)*2 or (64K64)*1	1	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	
512K	(32K64)*2 (32K32)*4	2	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	
1M	(64K32)*4 or (64K64)*2	2	A3-A19	A5-A19	A20-A28	32K10	512M	32K1 as dirty bit	TAG[9] as valid bit.

The following table shows the different standard SRAM access time requirements for different CPU clock frequencies.

Table 3-3.

CPU Bus Frequency (MHz)	PBSRAM/Memory cache Clock-to-Output Access Time (ns)	Tag RAM Access Time (ns)
50	13.5	20
60	10	15
66	8.5	15
75	7	12
83	6	9
100	5	8

~~Table 3-4~~

The following table shows different L2 timings supported by M1541

Table 3-5

	READ	WRITE	B2B READ	B2B WRITE
PBSRAM and Memory cache	3-1-1-1	3-1-1-1	3-1-1-1-1-1-1-1	3-1-1-1-1-1-1-1

In the following figures, two recommended cache subsystems are shown as follows :

Figure 3-4. Pipelined Burst SRAM L2 with single bank 256K & 8-bit Tag RAM (256M cacheable region, upgrade to 1G)

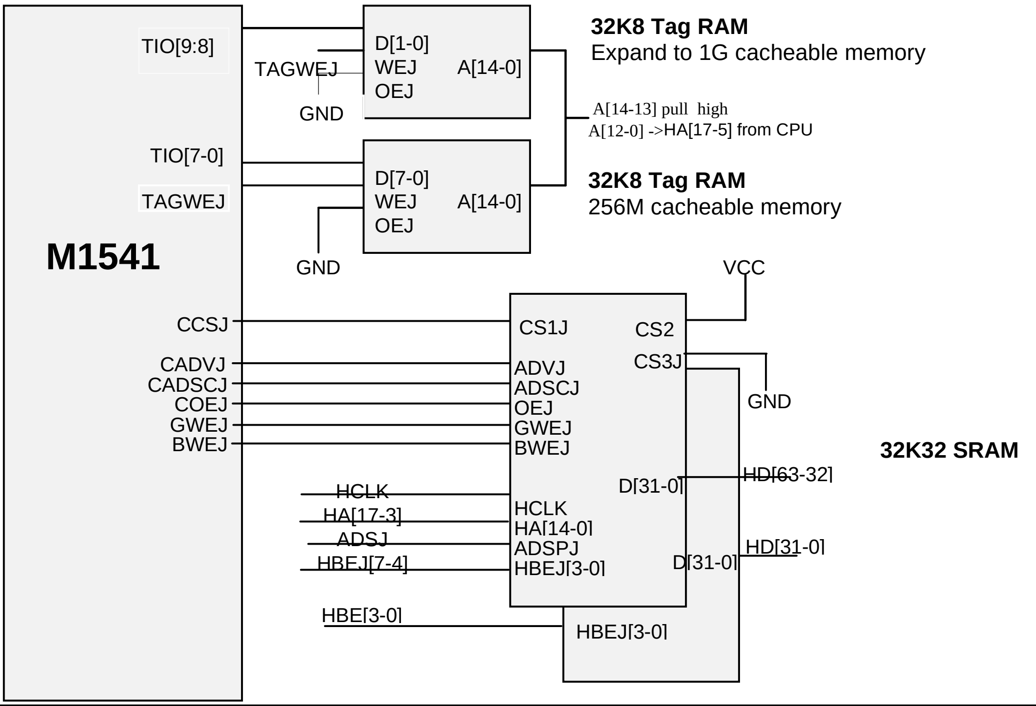


Figure 3-5. Pipelined Burst SRAM L2 with single bank 512K & 8-bit Tag RAM (128M cacheable region, upgrade to 512M)

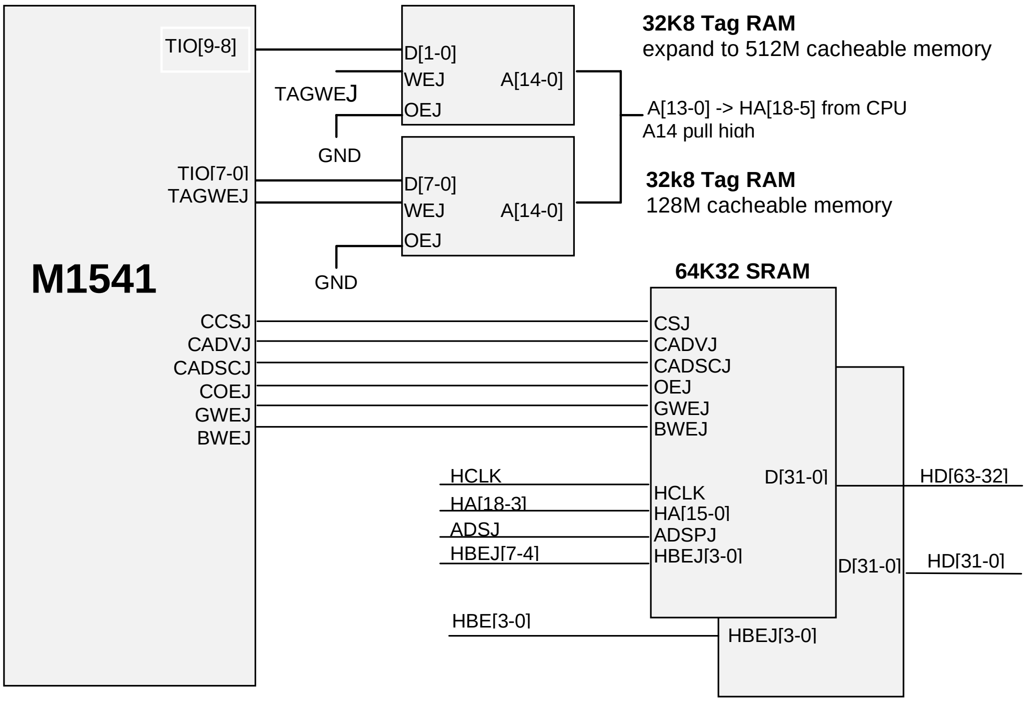
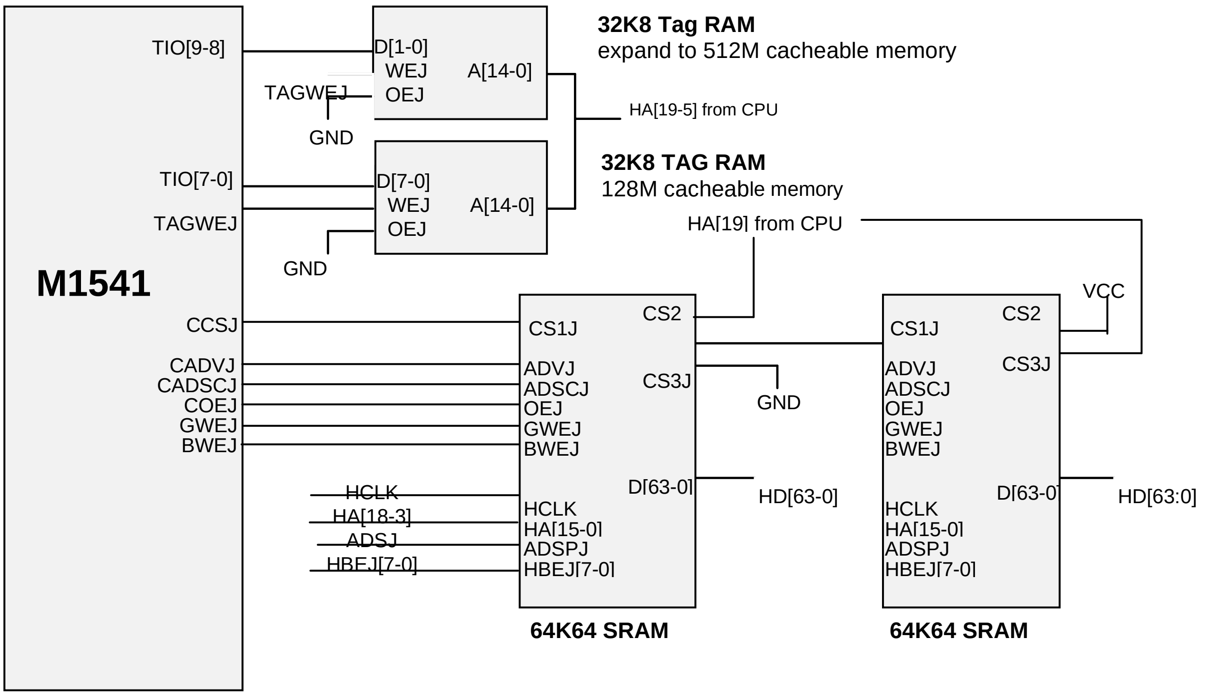


Figure 3-6. Pipelined Burst SRAM L2 with Double bank 1M & 8-bit Tag RAM (128M cacheable region, upgrade to 512M)



3.6 Internal TAG SRAM

The M1541 integrates a high speed TAG SRAM the size is 16K10. With the built in TAG RAM at 83MHz hot bus frequency system, the timing will keep at 3-1-1-1 to meet the best performance. When using internal TAG RAM only, M1541 can not support 1M L2 size. When the system needs 1M L2, it must use external TAG mode.

The timing of cache memory system use internal TAG RAM at 83 or 100 MHz hot bus frequency is shown in following table :

Table 3-6.

	READ	WRITE	B2B READ	B2B WRITE
PBSRAM and Memory cache	3-1-1-1	3-1-1-1	3-1-1-1-1-1-1-1	3-1-1-1-1-1-1-1

The following L2 Cache Table shows the different configurations supported by M1541 by using the internal TAG RAM (Not every version of M1541 supports internal TAG solution, please add external TAG solution on your motherboard design)

Table 3-7.

Config	DATA SRAM			Internal TAG SRAM				Internal MESI 8K1x4	Note
Cache Size	Size	Bank	Address lines	Address lines	Data Lines	Int. Tag Size	Cacheable DRAM Size		
256K	(32K32)*2 or (32K64)*1	1	A3-A17	A5-A17	A18-A27	8K10	256M	8K2 MESI	
512K	(64K32)*2 or (64K64)*1	1	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	
512K	(32K32)*4 or (32K64)*2	2	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	
1M	64K32)*4 or (64K64)*2	2	A3-A19	A5-A19	A20-A27 Ext. TAG A28-A31 Int. TAG	32K4	4G	32K1 as dirty bit Int. 32K1 as valid bit	External 32K8 required

3.7 SYSTEM MEMORY TIMING/CONFIGURATION

The DRAM controller of the M1541 supports a 64-bit memory bus for 8 banks of single-sided SIMMs or 4 banks of double sided SIMMs, and also supports the 64-bit memory bus for 8 banks of single-sided DIMMs or 4 banks of double sided DIMMs.

The controller can handle 8 banks of single-sided or 4 banks of double-sided 64-bit memory, with the memory size ranging from 2MB to 4GB(with 256Mbits technology). It also supports a programmable driving capability of MA/CAS and MD/MPD to optimize the access timing and the system cost in certain system memory configurations. Both the EDO and FPM are supported with an optimized timing to support the possible cacheless systems in low end market segments. The SDRAM features are also configured in this chip. M1541 supports a high performance SDRAM controller to push the new DRAM performance to the high edge. M1541 also enhances the DRAM page miss access timing for multithreading and multitasking application. For the best DRAM performance, M1541 has integrated a 32-QWORD deep merging DRAM write buffer. The deep buffer can post the CPU write data and also the PCI master write data and do byte merge to relief the DRAM bus access.

Although M1541 can support up to 8 banks of SDRAM (up to 4 DIMMs), the system is designed for 100 MHz CPU Front Side Bus frequency. Consider the loading of data bus, only three DIMM solution will be available at 100 MHz FSB design. M1541 achieves the best Performance/cost system solution.

As to the System Management RAM (SMRAM), the M1541 allows several optional non-cacheable spaces to map the SMRAM which includes regions such as 38000h-3FFFFh to B page, A/B region to A/B page and D page to B region.

3.7.1 Memory Types Supported

Table 3-8. EDO/FP Memory Structure Supported

Memory Structure	Address mode	Address size	Memory Structure	Address mode	Address size
4Mbits			2Mx8	Asymmetric	11x10
512Kx8	Asymmetric	10x9	4Mx4	Symmetric	11x11
1Mx4	Symmetric	10x10	4Mx4	Asymmetric	12x10
16Mbits			64Mbits		
1Mx16	Asymmetric	**11x9**	4Mx16	Symmetric	11x11
1Mx16	Asymmetric	12x8	8Mx8	Asymmetric	12x11
1Mx16	Symmetric	10x10	16Mx4	Symmetric	12x12
2Mx8	Asymmetric	12x9			

3.7.2 MA Mapping Table Supported

In the following table, ALADDIN-V supports a versatile memory MA mapping table to accommodate many different approaches of DRAM populated banks.

DRAM Address translation supported for some specific purpose

Table 3-9. Normal EDO/FP DRAM Address Translation

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	-	A16	A15	A24	A23	A14	A13	A12	A21	A20	A19	A18	A17	A16	A15
Column	-	A4	A3	A26	A24	A22	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 10 x 9, 10 x 10, 11 x 10, 11 x 11, 12 x 10

Table 3-10. 1M x 16, 2M x 8 EDO/FP DRAM Address Translation

Specific DRAM Address Translation Table for Asymmetric 1M x 16

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	-	A16	A15	A11	A22	A14	A13	A12	A21	A20	A19	A18	A17	A16	A15
Column	-	A4	A3	-	-	-	A23	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 1Mx16(12 x 8), 2Mx8(12 x 9)

Table 3-11. 1Mx16, 64M bit EDO/FP DRAM Address Translation

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	-	A16	A15	A25	A22	A14	A13	A12	A21	A20	A19	A18	A17	A16	A15
Column	-	A4	A3	A26	A24	A23	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 4Mx16(11 x 11), 8Mx8(12 x 11), 16Mx4(12 x 12)

Address Size = 1Mx16 (11x9)

Synchronous DRAM Address Translation Table :

Table 3-12. The connection from MA[14:0] to DIMMs

M1541 signal	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10	MA11	MA12	MA13	MA14
DIMM signal	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10/AP	NC(A11)	NC(A13), BA1	BA0	NC(A12)
DIMM pin no.	33	117	34	118	35	119	36	120	37	121	38	123	132, 39	122	126

SDRAM type to MA table 3-13

DRAM type	Bank	Row address x Column address	MA Table
256Mb	4	13 x 9	3-15
		13 x 10	3-17
		13 x 11	3-19
	2	14 x 9	3-15
		14 x 10	3-17
		14 x 11	3-19
128Mb	4	12 x 9	3-16
		12 x 10	3-18
		12 x 11	3-20
	2	13 x 9	3-16
		13 x 10	3-17
		13 x 11	3-20
64Mb	4	11 x 8	3-14
		12 x 8	3-14
		11 x 9	3-16
		12 x 9	3-16
		11 x 10	3-18
		12 x 10	3-18
	2	13 x 8	3-14
		13 x 9	3-16
		13 x 10	3-18
16Mb	2	11 x 8	3-14
		11 x 9	3-16
		11 x 10	3-18

Table 3-14. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A23	A11	A23	A24	A22	A14	A13	A12	A21	A20	A19	A18	A17	A16	A15
Column	-	A11	A23	-	AP	-	-	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 11 x 8, 12 x 8, 13 x 8,

Table 3-15. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Row	A26	A12	A24	A25	A22	A14	A13	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A12	A24	-	AP	-	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 13 x 9, 14 x 9

Table 3-16. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A24	A12	A24	A25	A22	A14	A13	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A12	A24	-	AP	-	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 11 x 9, 12 x 9, 13 x 9,

Table 3-17. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A27	A13	A25	A26	A22	A14	A24	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A13	A25	-	AP	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 13 x 10, 14x10

Table 3-18. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A25	A13	A25	A26	A22	A14	A24	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A13	A25	-	AP	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 11 x 10, 12 x 10, 13 x 10

Table 3-19. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A28	A14	A26	A27	A22	A25	A24	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A14	A26	A13	AP	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 13 x 11, 14 x 11

Table 3-20. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A26	A14	A26	A27	A22	A25	A24	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A14	A26	A13	AP	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 12 x 11, 13 x 11

3.7.3 Outstanding DRAM timing

Table 3-21. CPU to DRAM read performance Summary for EDO/FPM DRAMs

DRAM speed	DRAM type	Performance (in Host CLK)					
Read (Burst rate)		50 MHz	60 MHz	66 MHz	75 MHz	83 MHz	100 MHz
50 ns	EDO	x-222	x-222	x-222	x-222	x-333	x-333
	FPM	x-333	x-333	x-333	x-333	x-333	x-333
60 ns	EDO	x-222	x-222	x-222	x-222	x-333	x-333
	FPM	x-333	x-333	x-333	x-333	x-444	x-444
70 ns	EDO	x-333	x-333	x-333	x-333	x-333	x-333
	FPM	x-333	x-444	x-444	x-444	x-444	x-444

Page hit		50/60/66 MHz	75/83/100 MHz
60 ns	EDO/FPM	5	6
Row Miss			
60 ns	EDO/FPM	8	8
Page Miss			
60 ns	EDO/FPM	11	11

Back-to-back Burst Reads with Page hit		50/60/66 MHz	75 MHz	83/100 MHz
60 ns	EDO	5-222-2222	6-222-2222	6-333-3333
60 ns	FPM	5-333-3333	6-333-3333	6-444-4444

Table 3-22. CPU to DRAM Write Performance Summary

DRAM speed	DRAM type	Performance (in Host CLK)			
Posted Single Write with Write Buffer Empty		50 MHz	60/66 MHz	75/83 MHz	100 MHz
60 ns	EDO/FPM	3	3	3	3

Posted Burst Write with Write Buffer Empty		50 MHz	60/66 MHz	75/83 MHz	100 MHz
60 ns	EDO/FPM	3-111	3-111	3-111	3-111

Single Retire Hit		50/60 MHz	66 MHz	75/83 MHz	100 MHz
60 ns	EDO	3	3	3	4
60 ns	FPM	3	4	4	5

Single Retire Row Miss with RAS-CAS = 2T		50/60 MHz	66 MHz	75/83 MHz	100 MHz
60 ns	EDO	5	5	5	6
60 ns	FPM	5	6	6	7

Single Retire Page Miss with RAS-CAS = 2T		50/60 MHz	60/66 MHz	75/83 MHz	100 MHz
60 ns	EDO	8	8	8	8
60 ns	FPM	8	9	9	9

Retire Burst		50/60 MHz	66 MHz	75/83 MHz	100 MHz
60 ns	EDO	x-222	x-222	x-222	x-333
60 ns	FPM	x-222	x-333	x-333	x-444

Table 3-23. SDRAM Performance Summary

Cycle Type	100/83/75 MHz		66/60/50 MHz	
CAS Latency	CL=3	CL=2	CL=3	CL=2
Burst Read Page Hit	8-1-1-1	7-1-1-1	7-1-1-1	6-1-1-1
Read Bank Miss	11-1-1-1	9-1-1-1	10-1-1-1	8-1-1-1
Read Page Miss	14-1-1-1	11-1-1-1	13-1-1-1	10-1-1-1
Back-to-back Burst Read Page Hit	8-1-1-1-1-1-1-1	7-1-1-1-1-1-1-1	7-1-1-1-1-1-1-1	6-1-1-1-2-1-1-1
Write Page Hit	4	4	3	3
Write Row Miss	7	6	6	5
Write Page Miss	10	8	9	7

Posted Write	4-1-1-1	4-1-1-1	3-1-1-1	3-1-1-1
Write Retire rate from Posted Write Buffer	-1-1-1	-1-1-1	-1-1-1	-1-1-1

3.7.4 EDO/FPM DRAM Configuration

ALADDIN-V supports 8 banks of single sided SIMMs or 4 banks of double sided SIMMs maximum so that any mentioned combination can be fully supported. The following diagram shows some possible applications.

Figure 3-7. Two Double-Sided DRAM Banks (EDO/FPM)

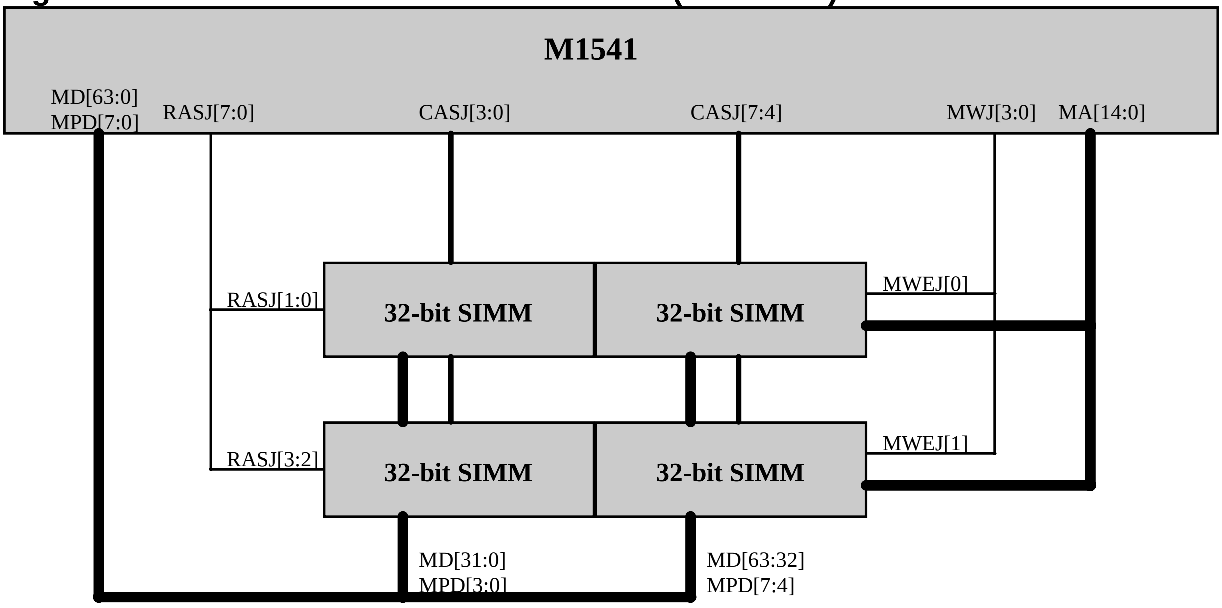
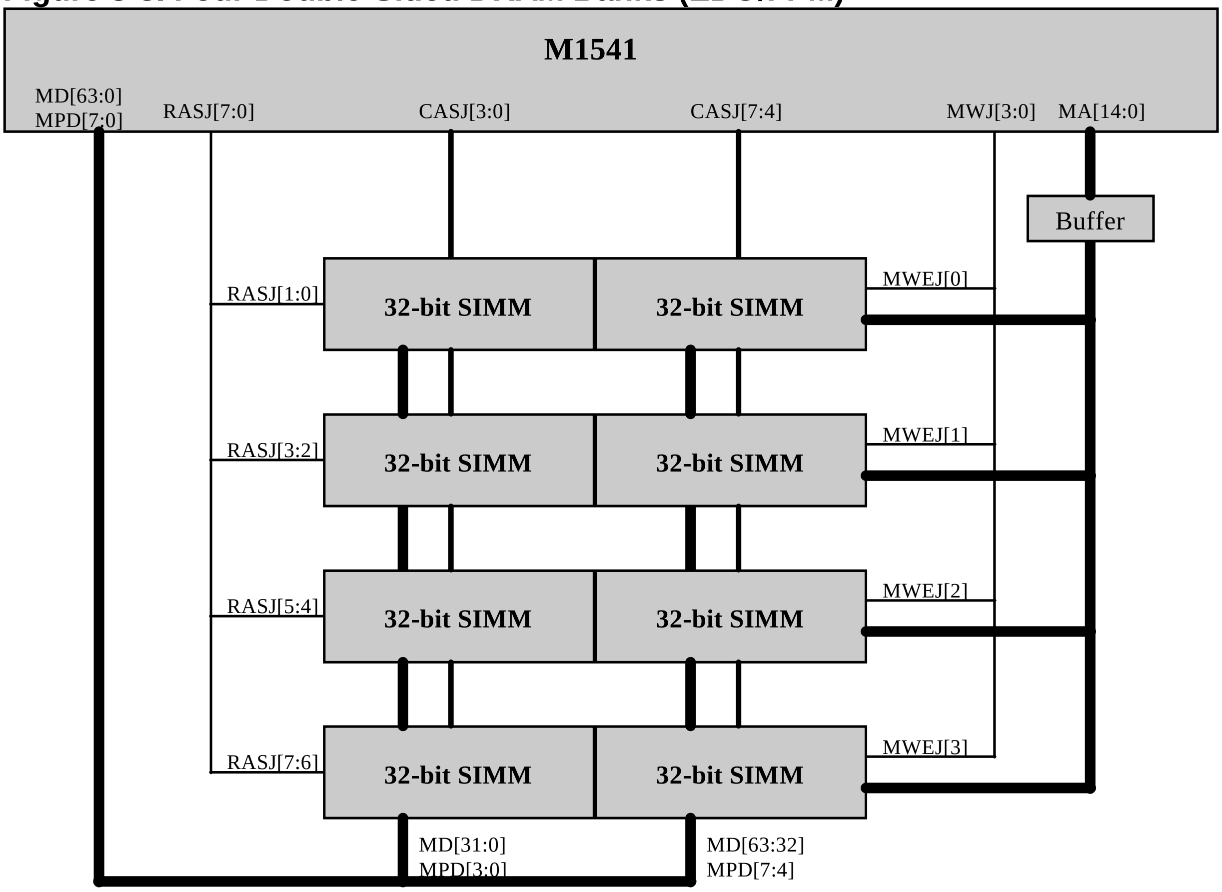


Figure 3-8. Four Double-Sided DRAM Banks (EDO/FPM)



3.7.5 SDRAM Support

Aladdin V supports the most popular synchronous DRAM (SDRAM) at technology of 16Mb, 64Mb, 128Mb, and 256Mb with extra performance and flexibility. Interleaved and linear wrap type for both CAS latency 2 and 3 with burst length 4 are supported. Users are permitted to use pure SDRAM up to 8 banks single sided or 4 banks of double sided, or mix with FPM/EDO DRAM on a row-by-row basis without any constraint. Furthermore, M1541 supports Enhanced Page mode which not only minimizes the effect of CAS latency (CL) and RAS Precharge time (Trp) but also largely enhances the overall performance of the system. JEDEC standard for SDRAM including 2n rule are supported too.

ALADDIN-V utilizes SDRAM commands that support both SDRAM and PC SDRAM. The commands are :

- Mode Register Set (MRS)
- CAS-Before-RAS Refresh (CBR)
- Self-Refresh (SEFR)
- Precharge All Banks (PALL)
- Precharge Selected Bank (PRCH)
- Row Active (RACT)
- Write (WRITE)
- Read (READ)
- No Operation (NOP)
- Device Deselect (DESL)

The following Table shows the command truth table M1541 supports.

Table 3-24. Command Truth Table

Function	Symbol	CKE	CSJ	SRASJ	SCASJ	WEJ	A[14:11]	A10-(AP)	A[9:0]
Mode Register Set	MRS	H *1	L	L	L	L	L	L	V *2
Self-Refresh	SEFR	L	L	L	L	H	L	L	L
Precharge All Banks	PALL	H	L	L	H	L	K	H	K
Precharge Selected Bank	PRCH	H	L	L	H	L	V	L	K
Row Active	RACT	H	L	L	H	H	V *3	V *3	V *3
Write	WRITE	H	L	H	L	L	V	L	V *4
Read	READ	H	L	H	L	H	V	L	V *4
No Operation	NOP	H	L	H	H	H	K	K	K
Device Deselect	DESL	H	H	H	H	H	K	K	K
CAS-before-RAS	CBR	H	L	L	L	H	K	K	K

Notes :

1. V = Valid, L = Logic Low, H = Logic High. K = Keep the value in previous cycle.
2. Please refer to Table 3-25.

3. A[11:0] shows the Row Address.
4. A[11], A[9:0] is used as the Column Address.

In terms of Wrap Type of SDRAM, ALADDIN-V supports both Interleave mode and Linear (Sequential) mode. The following table shows the Mode Register Set Table supported by M1541.

Table 3-25. Mode Register Set

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	ADDRESS
0	0	0	0	0	CAS Latency			Burst Type	Burst Length			Mode Register

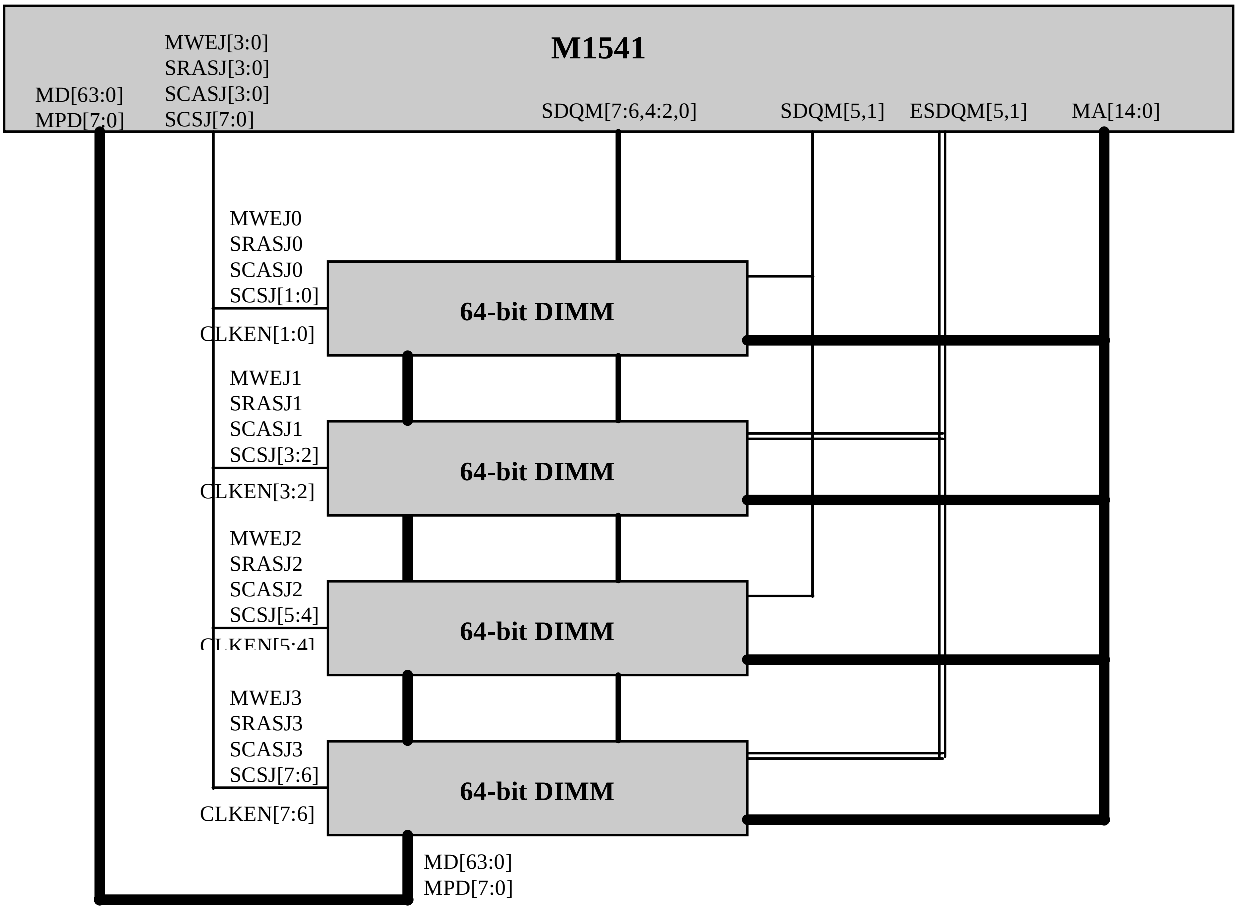
A6	A5	A4	CAS Latency	Index-48h bit4
0	1	0	2	1
0	1	1	3	0

A3	Burst Type	Description
0	Sequential	for M1/M2 Linear Wrap Mode
1	Interleave	for P54C/P55C/K5/K6 Interleave mode

A2	A1	A0	Burst Length
0	1	0	4
Others			Not Support

ALADDIN-V supports one set of SDRAM control signals. Following figure show the topological configuration when supporting SDRAM.. The following figure shows 8-bank support of SDRAM.

Figure 3-9. Four DIMMs Architecture


M1541
MWEJ[3:0]
SRASJ[3:0]
SCASJ[3:0]
SCSJ[7:0]
MD[63:0]
MPD[7:0]
SDQM[7:6,4:2,0]
SDQM[5,1]
ESDQM[5,1]
MA[14:0]
MWEJ0
SRASJ0
SCASJ0
SCSJ[1:0]
CLKEN[1:0]
64-bit DIMM
MWEJ1
SRASJ1
SCASJ1
SCSJ[3:2]
CLKEN[3:2]
64-bit DIMM
MWEJ2
SRASJ2
SCASJ2
SCSJ[5:4]
64-bit DIMM
MWEJ3
SRASJ3
SCASJ3
SCSJ[7:6]
CLKEN[7:6]
64-bit DIMM
MD[63:0]
MPD[7:0]

3.7.6 DRAM Load Analysis for each memory configuration and memory type.

The existing versatile/complicated memory configuration, which might result in a big variation of DRAM loading and the control signal timing. ALADDIN-V is designed to target some large reasonable memory types and number of banks to optimize COST and TIMING. If only 4 banks of single sided DRAM SIMMs or 2 banks of double sided DRAM SIMMs or 8banks of single sided DRAM DIMMs or 4 banks of double sided DRAM DIMMs are designed in motherboard, M1541 is designed to be TTL free for the DRAM control signals buffer.

3.8 CPU-to-PCI Posted Write Buffer

The M1541 integrates a 6-DWORD CPU-to-PCI posted write buffer to enhance the CPU-to-PCI performance. With this buffer, the M1541 can minimize the latency of CPU-to-PCI write cycles and maximize the concurrency of CPU bus and PCI bus when CPU writes data to PCI bus. The PCI burst write cycles and fast back-to-back cycles for CPU-to-PCI access are also supported by this buffer.
In addition, the M1541 CPU-to-PCI posted write buffer supports data merge, it can improve the CPU-to-PCI non-32 bits access performance.

3.9 PCI MASTER Latency and Throughput Analysis

The M1541 includes a smart PCI-to-DRAM interface, including a smart deep PCI-to-DRAM buffer and the enhanced PCI arbiter. All these components are designed to optimize the system performance and maximize the PCI bus bandwidth.

3.9.1 Smart Deep Post Write & Pre-fetch Buffer

The smart deep PCI-to-DRAM buffer of M1541 plays the key role to boost PCI master read/write performance. It consists of 80 DWORDs posted write buffer and 22 DWORDs pre-fetch buffer.

The 80 DWORDs PCI-to-DRAM posted write buffers enhance the PCI master bandwidth of accessing DRAM. With the implementation of L1/L2 write back merge and smart buffer management, the M1541 can sustain the ultimate 133-Mbytes/sec bandwidth for PCI master writing to local memory. More significantly, the maximum bandwidth is independent of results from the L1/L2 snooping and write back cycle, the DRAM types and L2 types.

On the other hand, to optimize the PCI master read performance when accessing DRAM, the M1541 includes 22 DWORDs PCI-to-DRAM read pre-fetch buffers. With the implementation of L1/L2 write back and smart buffer management, the M1541 can sustain the ultimate 133 Mbytes/sec bandwidth for PCI Master reading from Local memory. And the maximum bandwidth is independent of results of the L1/L2 snooping, write back cycle and L2 types.

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Considering the performance and concurrency of multi-master systems, for example the MPEG/Multimedia applications, the PCI-to-DRAM read pre-fetch buffer of M1541 is configured as two independent units. Each unit pre-fetches and keeps data independently with the other one. With this configuration, the M1541 minimizes the PCI master read latency and reduces the overhead of snooping and pre-fetching.

3.9.2 PCI 2.1 Compliant

The M1541 is fully compliant to the PCI 2.1 Specification. The M1541 supports Passive Release and programmable latency control timers for the first and subsequent data transaction. With the flexible PCI latency control, it can achieve the best system performance.

3.9.3 Pipelined Snoop Ahead

The M1541 utilizes an enhanced pipelined snoop protocol to minimize the L1 & L2 snoop overhead. While snooping L1 & L2, the M1541 also performs speculative read to DRAM such that the latency of master read cycle can be minimized. It combines with the deep smart read/write buffer to optimize PCI master performance.

3.9.4 PCI Arbiter

The M1541 integrates an enhanced PCI arbiter. It provides a fair arbitration by using a PCI and CPU Time Slice mechanism. The arbitration algorithm is also designed to minimize the snoop overhead. Besides the M1533/M1543 ISA bridge and AGP master, the M1541 supports up to 5 PCI masters to make the system motherboard design more flexible and engaging.

To balance the bandwidth of ISA masters and PCI masters and utilize the most bandwidth of PCI bus, the M1541 also supports passive release of PCI 2.1 latency requirements, which makes PCI master access possible when ISA master is active. By this way, the ALADDIN-V can target the best system performance and the most concurrency between PCI bus and ISA bus.

3.9.5 ACPI Support

The M1541 provides the scheme to support ACPI relative functions. By means of PM2_BASE_ADDRESS register (Index-E8h - Index-E9h) and PM2_CONTROL register (Index-EAh bits[1:0]), software can easily enable/disable PCI arbiter as ACPI requirement. In addition, PCIMRQJ signal makes ISA Bridge aware of PCI master bus request to generate SMI/SCI.

3.10 Low Power Features

The ALADDIN-V supports sophisticated power saving features, called Power On Suspend (Sleeping), Suspend to DRAM (Suspend), and Suspend to Disk. Under Power On Suspend state, the system will turn off the signal event of host and keep the DRAM refresh active through the M1541 DRAM interface that is triggered by a 32.768KHz clock source. After the Power On suspend event is triggered, by programming a bit of M1533/M1543 internal register, the M1533/M1543 will initiate a handshake with the M1541. During the handshake, the M1533/M1543 will issue STPCLK to the host, stop the system clock generator, pull the I/O output level to leakageless polarity and turn on the SUSPEND REFRESH circuit to sustain the DRAM data. Theoretically, the only power request under the Power On suspend is the circuit of DRAM suspend refresh. M1541 core has two different power planes, one for the Suspend Refresh circuit, the other is for the other circuit except Suspend Refresh circuit. During Suspend to DRAM state, the system designer can shut off the power except the DRAM suspend refresh circuit to save more system power. Under the Suspend to Disk, only the M1533/M1543 resume circuit is powered and get the minimized system power consumption.

The M1541 and the M1533/M1543 are designed with a very sophisticated I/O circuit and to perform the leakage control under the power saving mode, which is very popular in notebook designs.

For desktop designs, the Power On suspend can provide the system a very efficient **STAND-ON** feature that is more demanding in future home PC systems for Microsoft On Now technology OS.

In the M1533/M1543 of ALADDIN-V, the solution gives a deep green function. Regarding deep PMU for Peripheral device, one might design a dedicated PMU device to accompany the Power On suspend feature to form a very deep power saving system, such as a notebook system.

To leave the power saving mode, ALADDIN-V provides several internal event detectors or external event detectors. The system will resume in a very careful/dedicated process and protocol to recover the system to original status, same as the status before entering.

3.11 DRAM Refresh

The M1541 provides CAS-before-RAS (CBR) refresh and RAS-only refresh for FPM DRAM, CAS-before-RAS (CBR) refresh and RAS-only refresh and Extended refresh and self refresh for EDO DRAM, and CAS-before-RAS (CBR) refresh and Self refresh for SDRAMs. FPM/EDO refresh methods use "staggered" and "smart refresh" (i.e. refresh is only performed on banks that are populated) algorithm. The DRAM refresh rate can be controlled via the Index 45h Bits[2:0].

3.12 ECC/Parity Algorithm

The M1541 provides an ECC DRAM data integrity feature. The ECC feature provides single-error correction, double-error detection, and detection of all errors confined to a single nibble (SEC-DEC-S4ED) for DRAM data integrity. The M1541 will generate 8-bit ECC check bits for 64-bit data to DRAM when the ECC feature is enabled and the current DRAM cycle is a write access operation.

If a partial write (less than 64-bit write) event occurs, a read-modified-write operation will be performed by the M1541. The M1541 will detect all single bit, double-bit errors, and all errors confined to a single nibble when ECC is enabled and a DRAM read cycle is performed. The M1541 also corrects all single-bit errors and the corrected data is then transferred to the requester (CPU or PCI). This corrected data will not be written back to DRAM in the current M1541 version. The ECC errors are latched until cleared by software. The software programmer also can detect 64 from 72-bit wide SIMMs or check ECC circuit operations via the ECC (parity) test mode. The ECC check bits (or parities) can be forced to any value during all DRAM write access cycles in the ECC/Parity test mode. All the DRAM read leadoff latency timings should add 1 HCLKIN when the ECC feature is enabled.

The M1541 also provides another DRAM data integrity feature -- conventional DRAM even parity generation and checking when Index 50h bit0 is set to '0'. The DRAM parity checking error reporting condition and status also are defined in Index 50h-51h. The software can differentiate the 64 from 72-bit wide SIMMs or check parity circuit operation via the ECC/Parity test mode. The conventional Parity check will not degrade the system performance.

3.13 AGP and PCI-to-PCI bridge

The M1541 has a built in PCI-to-PCI bridge device to support the AGP interface. The Device ID is M5247. Behind the PCI to PCI bridge is an 66MHz PCI bus which meets the PCI revision 2.1 specification to support the AGP interface. The interface provides three significant performance extensions to the PCI specification which are intended to optimize the AGP for high performance 3D graphics applications. These extensions are

(1) Deep pipeline memory read buffer (32 QWORDs) and memory write buffer (16 QWORDs), fully hiding memory access latency

(2) Demultiplexing of address and data on the bus use the “IDLE band” signals, allowing almost 100% bus efficiency

(3) AC timing for 133 MHz data transfer rate, up to 533 Mbytes/sec data throughput

The M1541 supports a physically, logically and electrically independent AGP interface. Support both the PIPEJ and SBA[7-0] addressing method and RBFJ flow control. The design is following the AGP revision 1.0 specification. The interface will support the PCI 66 mode, AGP 1X mode and 2X modes.

When at PCI 66 mode, the FRAMEJ protocol will be followed.

When at 1X transfer mode, the operation is similar to the PCI. All timings are referenced to the AGP clock. It will provide a peak bandwidth of 266Mbyte/sec.

When at 2X transfer mode, the data transfer rate of the AD, C/BEJ and SBA signals are double. With 2X transfer, QWORD transfers only require one clock cycle, and sideband commands only require one clock per 16-bit command.
For maximum software compatibility, two-level GART (Graphics Address Re-mapping Table) is set up and maintained by mini-port driver supported by ALi. So the actual table implementation is abstracted to a common API.

Besides, the 8 DWORDs PCI to PCI_66 posted write buffer and the 2 DWORDs PCI_66 to PCI posted write buffer make M1541 perform outstanding multi-master system performance. Especially when AGP 3D engine on AGP bus and video processor like MPEG2 accelerator on 33 MHz PCI bus.

Section 3 : Function Description

3.1 System Architecture

In the following illustration, ALADDIN-V gives a highly integrated system solution and a most up-to-date system architecture, which includes the Accelerated Graphics Port, .Parity/ECC, PBSRAM/Memory Cache, SDRAM, ACPI, Ultra-33 IDE Master, USB, PS2 Keyboard/Mouse, and highly concurrent multi-bus with smart deep FIFO between the buses, such as the HOST/ A.G.P./ DRAM/ PCI/ ISA/ DEDICATED IDE/USB buses. Using ALADDIN-V, you can achieve a TTL free solution and provide the best system performance.

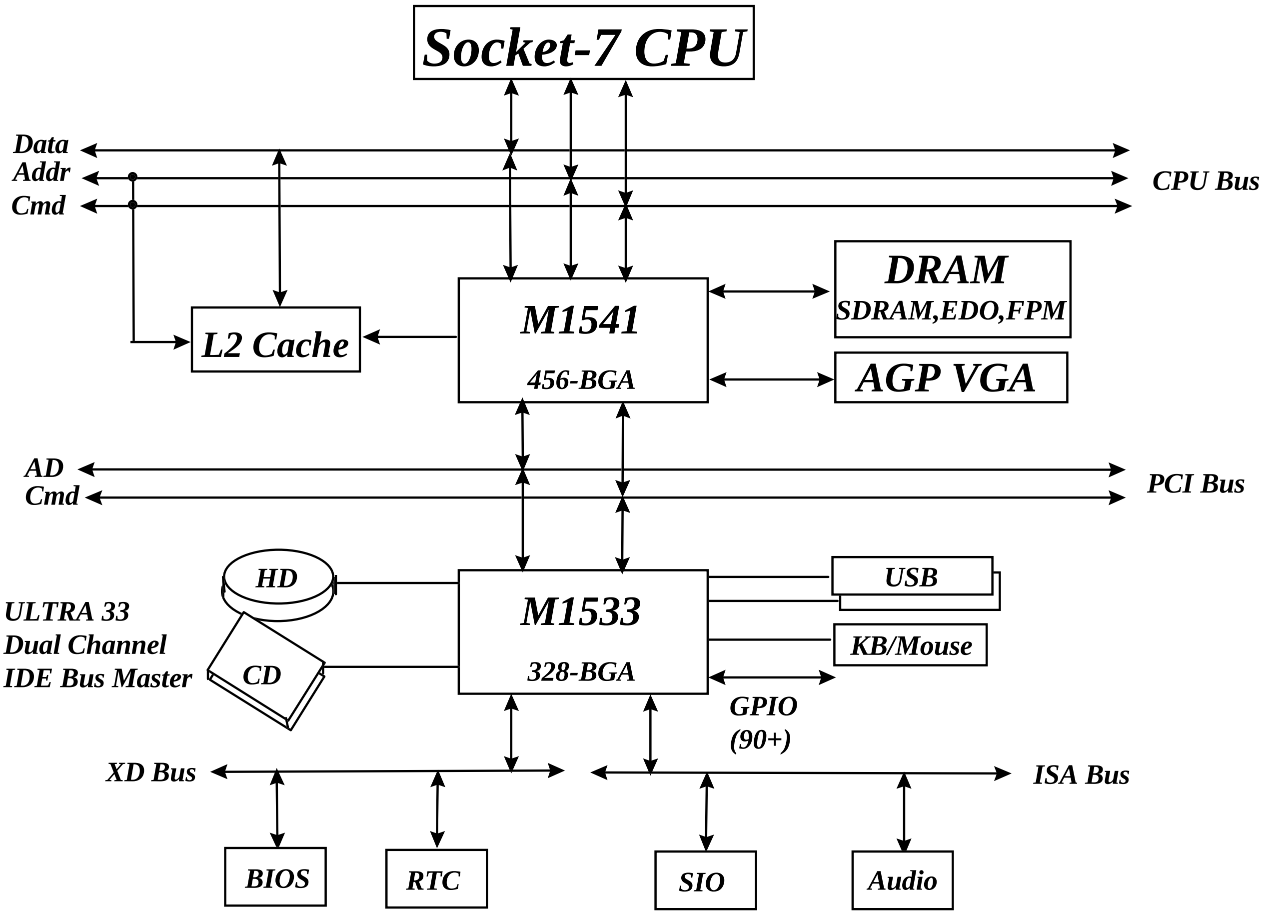

Figure 3-1. Aladdin V System Block Diagram with M1533

As the North bridge, the M1541 provides a complete integrated solution for the system controller and data path components in a socket-7 processor system. It provides a 64-bit CPU bus interface, AGP bus interface, 32-bit PCI bus interface, 64/72 DRAM data bus with ECC or parity, secondary cache interface including Pipelined Burst SRAM or Memory Cache, PCI master to DRAM interface, and 5 PCI masters, CPU, and M1533/M1543 arbiter. The following figure shows the highly efficient data path in the M1541. The M1541 bus interfaces are designed to interface with 2.5V, 3.3V and 5V buses. It directly connects to 3.3V or 2.5V CPU bus, 3.3V or 5V Tag, 3.3V or 5V DRAM bus, and 3.3V or 5V PCI bus.

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The M1533 provides a highly integrated PCI-to-ISA bridge solution for the best Notebook system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, and Enhanced Green function.

The M1543 provides a highly integrated PCI-to-ISA bridge solution for the best Desktop system. It comprises a 2-channel dedicated Ultra-33 IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse controller, 2-port Universal Serial Bus feature, PCI 2.1 Compliance operation, ACPI, Green function, and the Super I/O function.

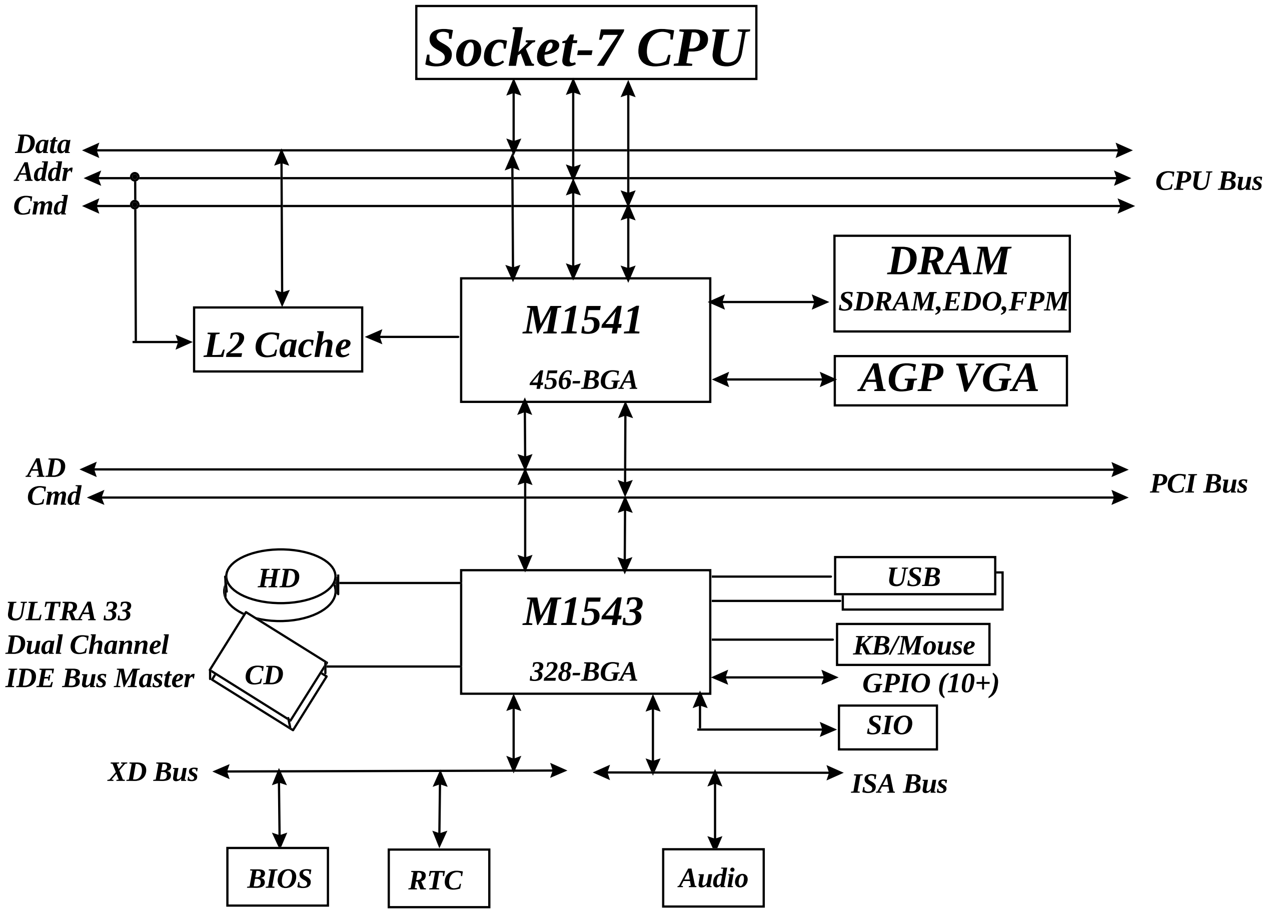


Figure 3-2. Aladdin V System Block Diagram with M1543

3.2 Data Path and Buffer Architecture

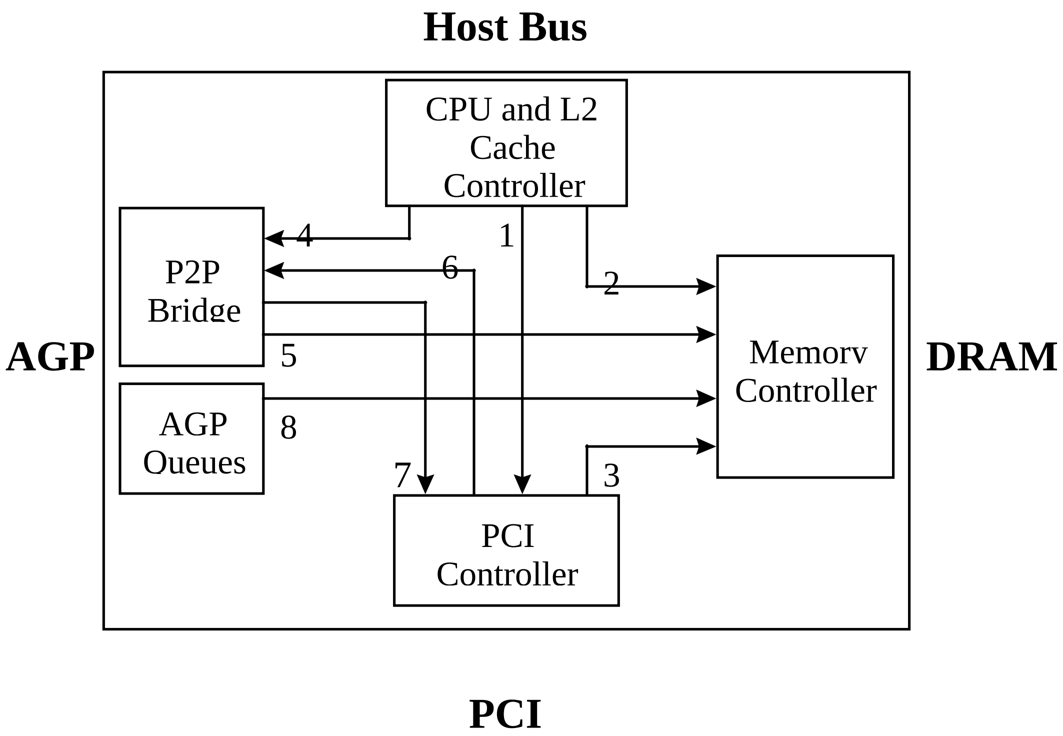


Figure 3-3. Data Path and Buffer Architecture

1 : CPU to PCI – 6 DWORDs memory write buffer

2 : CPU to Memory – 32 QWORDs write buffer

3 : PCI to Memory – 80 DWORDs write posted buffer & 22 DWORDs read pre-fetch buffer

4 : CPU to AGP – 8 DWORDs posted write buffer

5 : PCI_66 to Memory – 40 QWORDs write buffer and 32 QWORDs read buffer

6 : PCI to AGP - 8 DWORDs write posted buffer

7 : PCI_66 to PCI - 2 DWORDs write posted buffer

8 : AGP to Memory – 16 QWORDs write buffer and 32 QWORDs read buffer

3.3 CPU Interface

The M1541 supports all Pentium-class CPUs including Intel P54C/P55C, Cyrix M1/M2, AMD K5/K6. Furthermore, M1541 supports a high performance CPU interface with bus frequency up to 100 MHz to achieve the Pentium II-class system performance. M1541 also supports Cyrix Linear Wrap mode for M1 and M2 to gain the best system performance. M1541 can also interface to 2.5V CPU I/O interface for Notebook use. In higher CPU bus frequency interface, M1541 will do the so-called pseudo-synchronous design instead of the asynchronous design. When 75/83.3/100 MHz CPU bus is used, the PCI bus will be running at 30/33/33 MHz (divide CPU bus by 2/2.5/3). The pseudo-synchronous clock design is a better solution than the pure asynchronous clock design, it eliminates the performance degradation to synchronize two asynchronous buses and helps the chip reliability to resolve the chip testing issue.

3.4 Clock Design Philosophy

The system provides 4 clocks (HCLKIN, PCICLK, CLK32KI, GCLKIN) for M1541, HCLKIN has the same frequency with the CPUCLK, Cache clock, and SDRAM clock. PCICLK has the same frequency with the PCI bus clock, and CLK32KI is a 32.768KHz frequency clock from M1533/M1543 CLK32KO or from the system board clock source. GCLKIN provides the clock source of A.G.P. and PCI operation on A.G.P.

System designer should minimize the clock skew between CPUCLK, Cache clock, SDRAM clock, and HCLKIN, and also the skew between PCICLK and PCI bus clock. Regarding the skew between M1541 HCLKIN and PCICLK, PCICLK should lag HCLKIN for 1 ~ 4 ns. The internal clock design philosophy uses the HCLKIN running the state machine of CPU interface, L2 controller, and DRAM controller, and uses the PCICLK running the PCI state machine, and automatically takes good care of the internal signal interface between different clock frequency state machines. Also M1541 will support the internal smart clock control, it will shut off the internal clock when the CPU or PCI bus is idle to save the power consumption. CLK32KI clock is used for the DRAM Suspend refresh clock. It is a clock input and not necessarily relative to HCLKIN or PCICLK.

3.5 Cache Memory Timing/Configuration

The M1541 integrates a high performance L2 write back/dynamic-write-back direct mapping cache controller using MESI protocol of L1 and L2, and has an L2 MESI tag 16K2 bits built-in to maintain the data coherence for optimizing CPU bus utilization. The L2 cache can be configured for Memory Cache or Pipelined Burst SRAM with cache size ranging from 256KB, 512KB to 1MB. The cacheable region can be up to 1GB under 256KB L2 cache memory configuration, by using 8K10 tag RAM or two 8K8 tag RAM option. When using an 8K8 tag RAM under 256KB L2 cache , the cacheable region of the system is 256MB. The controller can perform a dynamic-write-back cycle to DRAM, which the L1 write cycle will be directed to DRAM intelligently with 3-1-1-1 timing without stalling the CPU execution. Also M1541 can support the CPU single read cycle L2 allocation feature, M1541 will do the L2 line fill even when the CPU issues only a single read cycle to improve the L2 hit rate for some special application. The following table shows the best performance for the L2 Read/Write access.

The timing of cache memory system is shown in following table :

Table 3-1

	READ	WRITE	B2B READ	B2B WRITE
PBSRAM and Memory cache	3-1-1-1	3-1-1-1	3-1-1-1-1-1-1-1	3-1-1-1-1-1-1-1

The following L2 Cache Table shows the different configurations supported by M1541.

Table 3-2

Config	DATA SRAM			External TAG SRAM				Internal MESI 8K1x4	Note
Cache Size	**Size**	**Bank**	**Address lines**	**Address lines**	**Data Lines**	**Ext. Tag Size**	**Cacheable DRAM Size**		
256K	(32K32)*2 or (32K64)*1	1	A3-A17	A5-A17	A18-A25	8K8	64M	8K2 MESI	
512K	(64K32)*2 or (64K64)*1	1	A3-A18	A5-A18	A19-A26	16K8	128M	16K2 MESI	
512K	(32K64)*2 (32K32)*4	2	A3-A18	A5-A18	A19-A26	16K8	128M	16K2 MESI	
1M	(64K32)*4 or (64K64)*2	2	A3-A19	A5-A19	A20-A26	32K8	128M	32K1 as dirty bit	TAG[7] as valid bit.
256K	(32K32)*2 or (32K64)*1	1	A3-A17	A5-A17	A18-A27	8K10	256M	8K2 MESI	
512K	(64K32)*2 or (64K64)*1	1	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	
512K	(32K64)*2 (32K32)*4	2	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	
1M	(64K32)*4 or (64K64)*2	2	A3-A19	A5-A19	A20-A28	32K10	512M	32K1 as dirty bit	TAG[9] as valid bit.

The following table shows the different standard SRAM access time requirements for different CPU clock frequencies.

Table 3-3.

CPU Bus Frequency (MHz)	PBSRAM/Memory cache Clock-to-Output Access Time (ns)	Tag RAM Access Time (ns)
50	13.5	20
60	10	15
66	8.5	15
75	7	12
83	6	9
100	5	8

~~Table 3-4~~

The following table shows different L2 timings supported by M1541

Table 3-5

	READ	WRITE	B2B READ	B2B WRITE
PBSRAM and Memory cache	3-1-1-1	3-1-1-1	3-1-1-1-1-1-1-1	3-1-1-1-1-1-1-1

In the following figures, two recommended cache subsystems are shown as follows :

Figure 3-4. Pipelined Burst SRAM L2 with single bank 256K & 8-bit Tag RAM (256M cacheable region, upgrade to 1G)

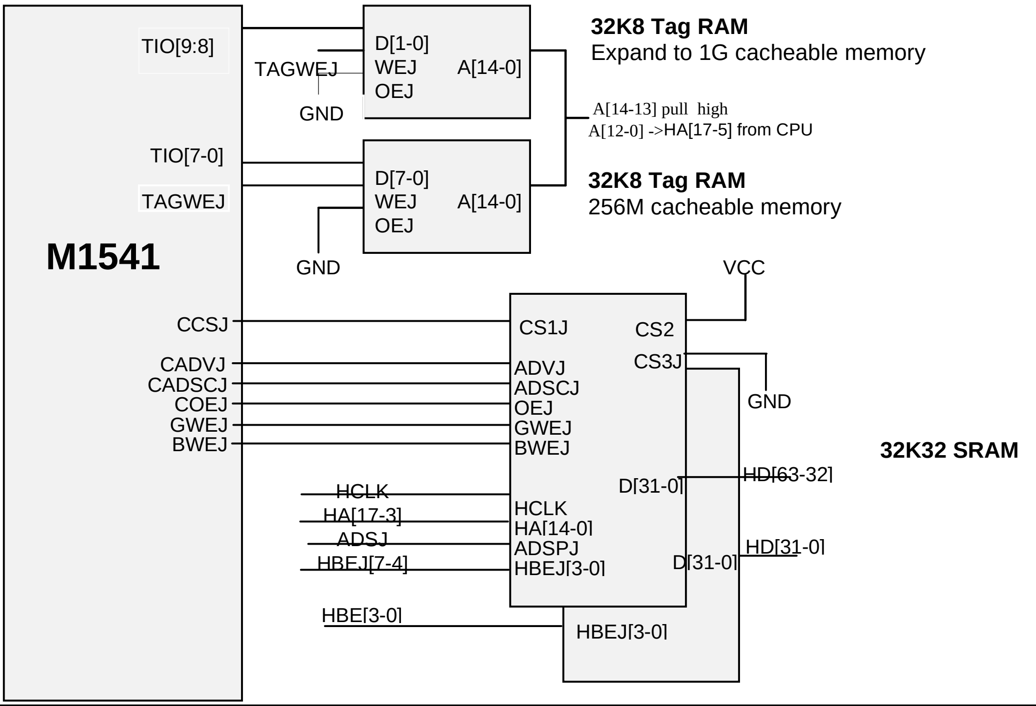


Figure 3-5. Pipelined Burst SRAM L2 with single bank 512K & 8-bit Tag RAM (128M cacheable region, upgrade to 512M)

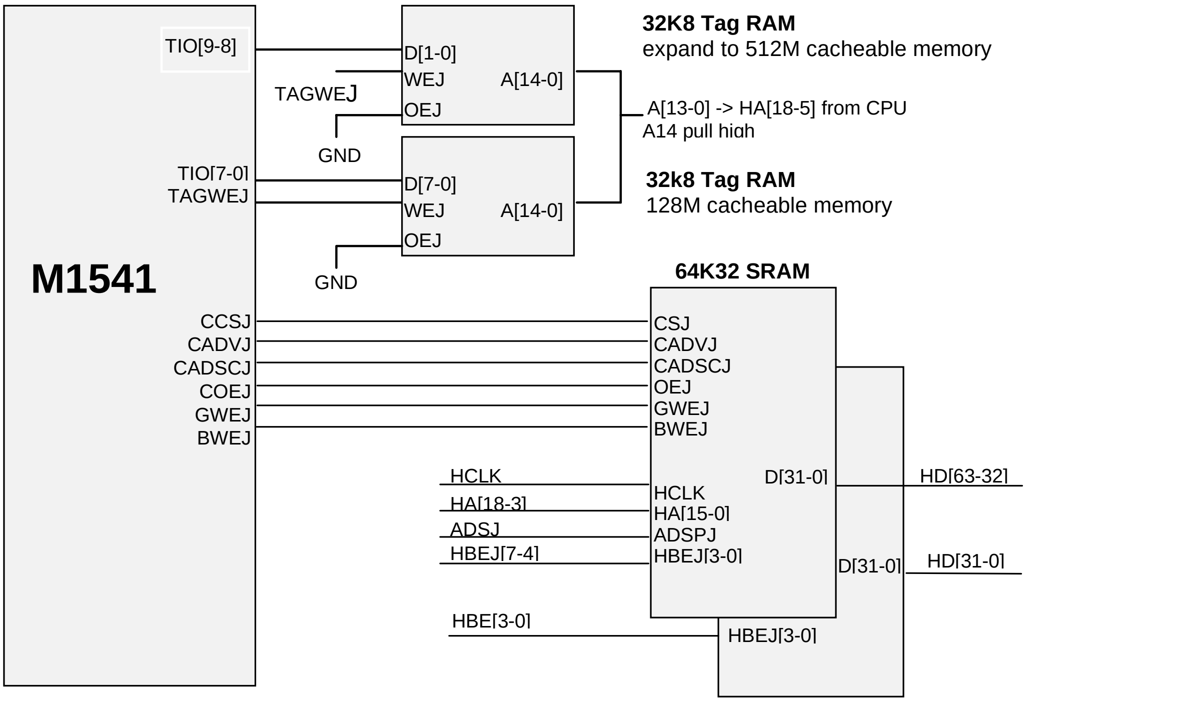
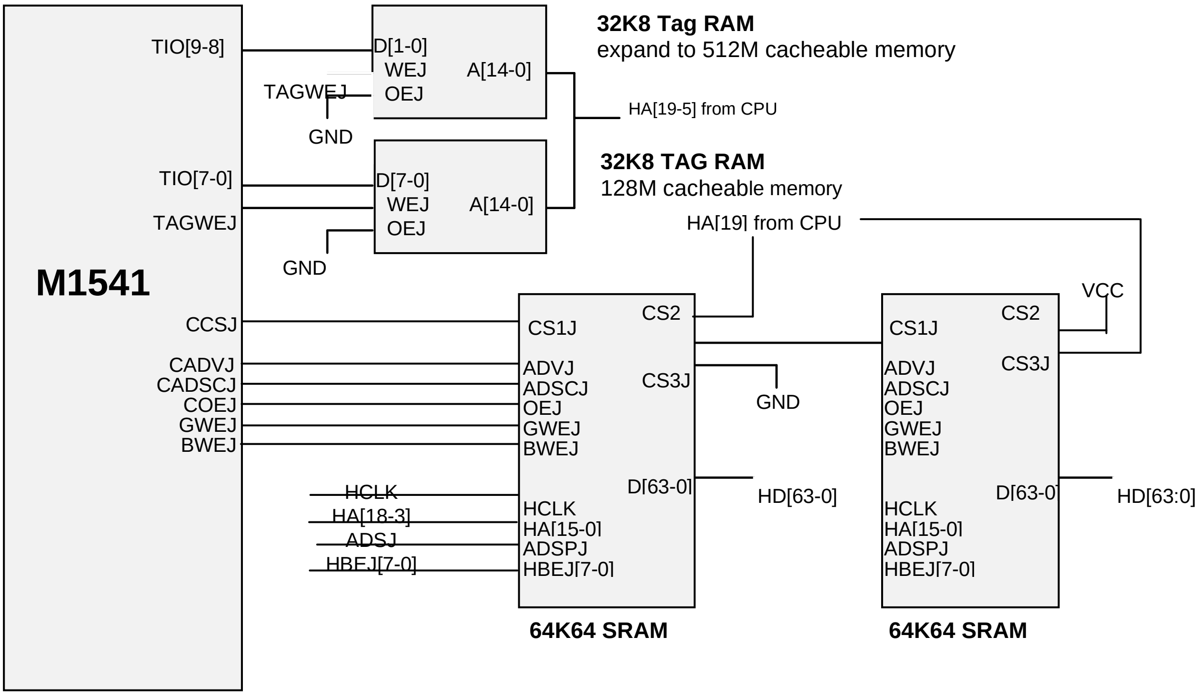


Figure 3-6. Pipelined Burst SRAM L2 with Double bank 1M & 8-bit Tag RAM (128M cacheable region, upgrade to 512M)



3.6 Internal TAG SRAM

The M1541 integrates a high speed TAG SRAM the size is 16K10. With the built in TAG RAM at 83MHz hot bus frequency system, the timing will keep at 3-1-1-1 to meet the best performance. When using internal TAG RAM only, M1541 can not support 1M L2 size. When the system needs 1M L2, it must use external TAG mode.

The timing of cache memory system use internal TAG RAM at 83 or 100 MHz hot bus frequency is shown in following table :

Table 3-6.

	READ	**WRITE**	**B2B READ**	**B2B WRITE**
PBSRAM and Memory cache	3-1-1-1	3-1-1-1	3-1-1-1-1-1-1-1	3-1-1-1-1-1-1-1

The following L2 Cache Table shows the different configurations supported by M1541 by using the internal TAG RAM (Not every version of M1541 supports internal TAG solution, please add external TAG solution on your motherboard design)

Table 3-7.

Config	DATA SRAM			Internal TAG SRAM				Internal MESI 8K1x4	Note
Cache Size	Size	Bank	Address lines	Address lines	Data Lines	Int. Tag Size	Cacheable DRAM Size		
256K	(32K32)*2 or (32K64)*1	1	A3-A17	A5-A17	A18-A27	8K10	256M	8K2 MESI	
512K	(64K32)*2 or (64K64)*1	1	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	
512K	(32K32)*4 or (32K64)*2	2	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	
1M	64K32)*4 or (64K64)*2	2	A3-A19	A5-A19	A20-A27 Ext. TAG A28-A31 Int. TAG	32K4	4G	32K1 as dirty bit Int. 32K1 as valid bit	External 32K8 required

3.7 SYSTEM MEMORY TIMING/CONFIGURATION

The DRAM controller of the M1541 supports a 64-bit memory bus for 8 banks of single-sided SIMMs or 4 banks of double sided SIMMs, and also supports the 64-bit memory bus for 8 banks of single-sided DIMMs or 4 banks of double sided DIMMs.

The controller can handle 8 banks of single-sided or 4 banks of double-sided 64-bit memory, with the memory size ranging from 2MB to 4GB(with 256Mbits technology). It also supports a programmable driving capability of MA/CAS and MD/MPD to optimize the access timing and the system cost in certain system memory configurations. Both the EDO and FPM are supported with an optimized timing to support the possible cacheless systems in low end market segments. The SDRAM features are also configured in this chip. M1541 supports a high performance SDRAM controller to push the new DRAM performance to the high edge. M1541 also enhances the DRAM page miss access timing for multithreading and multitasking application. For the best DRAM performance, M1541 has integrated a 32-QWORD deep merging DRAM write buffer. The deep buffer can post the CPU write data and also the PCI master write data and do byte merge to relief the DRAM bus access.

Although M1541 can support up to 8 banks of SDRAM (up to 4 DIMMs), the system is designed for 100 MHz CPU Front Side Bus frequency. Consider the loading of data bus, only three DIMM solution will be available at 100 MHz FSB design. M1541 achieves the best Performance/cost system solution.

As to the System Management RAM (SMRAM), the M1541 allows several optional non-cacheable spaces to map the SMRAM which includes regions such as 38000h-3FFFFh to B page, A/B region to A/B page and D page to B region.

3.7.1 Memory Types Supported

Table 3-8. EDO/FP Memory Structure Supported

Memory Structure	Address mode	Address size	Memory Structure	Address mode	Address size
4Mbits			2Mx8	Asymmetric	11x10
512Kx8	Asymmetric	10x9	4Mx4	Symmetric	11x11
1Mx4	Symmetric	10x10	4Mx4	Asymmetric	12x10
16Mbits			64Mbits		
1Mx16	Asymmetric	**11x9**	4Mx16	Symmetric	11x11
1Mx16	Asymmetric	12x8	8Mx8	Asymmetric	12x11
1Mx16	Symmetric	10x10	16Mx4	Symmetric	12x12
2Mx8	Asymmetric	12x9			

3.7.2 MA Mapping Table Supported

In the following table, ALADDIN-V supports a versatile memory MA mapping table to accommodate many different approaches of DRAM populated banks.

DRAM Address translation supported for some specific purpose

Table 3-9. Normal EDO/FP DRAM Address Translation

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	-	A16	A15	A24	A23	A14	A13	A12	A21	A20	A19	A18	A17	A16	A15
Column	-	A4	A3	A26	A24	A22	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 10 x 9, 10 x 10, 11 x 10, 11 x 11, 12 x 10

Table 3-10. 1M x 16, 2M x 8 EDO/FP DRAM Address Translation

Specific DRAM Address Translation Table for Asymmetric 1M x 16

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	-	A16	A15	A11	A22	A14	A13	A12	A21	A20	A19	A18	A17	A16	A15
Column	-	A4	A3	-	-	-	A23	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 1Mx16(12 x 8), 2Mx8(12 x 9)

Table 3-11. 1Mx16, 64M bit EDO/FP DRAM Address Translation

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	-	A16	A15	A25	A22	A14	A13	A12	A21	A20	A19	A18	A17	A16	A15
Column	-	A4	A3	A26	A24	A23	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 4Mx16(11 x 11), 8Mx8(12 x 11), 16Mx4(12 x 12)

Address Size = 1Mx16 (11x9)

Synchronous DRAM Address Translation Table :

Table 3-12. The connection from MA[14:0] to DIMMs

M1541 signal	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10	MA11	MA12	MA13	MA14
DIMM signal	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10/AP	NC(A11)	NC(A13), BA1	BA0	NC(A12)
DIMM pin no.	33	117	34	118	35	119	36	120	37	121	38	123	132, 39	122	126

SDRAM type to MA table 3-13

DRAM type	Bank	Row address x Column address	MA Table
256Mb	4	13 x 9	3-15
		13 x 10	3-17
		13 x 11	3-19
	2	14 x 9	3-15
		14 x 10	3-17
		14 x 11	3-19
128Mb	4	12 x 9	3-16
		12 x 10	3-18
		12 x 11	3-20
	2	13 x 9	3-16
		13 x 10	3-17
		13 x 11	3-20
64Mb	4	11 x 8	3-14
		12 x 8	3-14
		11 x 9	3-16
		12 x 9	3-16
		11 x 10	3-18
		12 x 10	3-18
	2	13 x 8	3-14
		13 x 9	3-16
		13 x 10	3-18
16Mb	2	11 x 8	3-14
		11 x 9	3-16
		11 x 10	3-18

Table 3-14. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A23	A11	A23	A24	A22	A14	A13	A12	A21	A20	A19	A18	A17	A16	A15
Column	-	A11	A23	-	AP	-	-	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 11 x 8, 12 x 8, 13 x 8,

Table 3-15. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Row	A26	A12	A24	A25	A22	A14	A13	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A12	A24	-	AP	-	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 13 x 9, 14 x 9

Table 3-16. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A24	A12	A24	A25	A22	A14	A13	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A12	A24	-	AP	-	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 11 x 9, 12 x 9, 13 x 9,

Table 3-17. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A27	A13	A25	A26	A22	A14	A24	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A13	A25	-	AP	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 13 x 10, 14x10

Table 3-18. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A25	A13	A25	A26	A22	A14	A24	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A13	A25	-	AP	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 11 x 10, 12 x 10, 13 x 10

Table 3-19. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A28	A14	A26	A27	A22	A25	A24	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A14	A26	A13	AP	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 13 x 11, 14 x 11

Table 3-20. Synchronous DRAM Address Translation:

MA[14:0]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Row	A26	A14	A26	A27	A22	A25	A24	A23	A21	A20	A19	A18	A17	A16	A15
Column	-	A14	A26	A13	AP	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 12 x 11, 13 x 11

3.7.3 Outstanding DRAM timing

Table 3-21. CPU to DRAM read performance Summary for EDO/FPM DRAMs

DRAM speed	**DRAM type**	**Performance (in Host CLK)**					
Read (Burst rate)		50 MHz	60 MHz	66 MHz	75 MHz	83 MHz	100 MHz
50 ns	EDO	x-222	x-222	x-222	x-222	x-333	x-333
	FPM	x-333	x-333	x-333	x-333	x-333	x-333
60 ns	EDO	x-222	x-222	x-222	x-222	x-333	x-333
	FPM	x-333	x-333	x-333	x-333	x-444	x-444
70 ns	EDO	x-333	x-333	x-333	x-333	x-333	x-333
	FPM	x-333	x-444	x-444	x-444	x-444	x-444

Page hit		50/60/66 MHz	75/83/100 MHz
60 ns	EDO/FPM	5	6
Row Miss			
60 ns	EDO/FPM	8	8
Page Miss			
60 ns	EDO/FPM	11	11

Back-to-back Burst Reads with Page hit		50/60/66 MHz	75 MHz	83/100 MHz
60 ns	EDO	5-222-2222	6-222-2222	6-333-3333
60 ns	FPM	5-333-3333	6-333-3333	6-444-4444

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Table 3-22. CPU to DRAM Write Performance Summary

DRAM speed	DRAM type	Performance (in Host CLK)			
Posted Single Write with Write Buffer Empty		50 MHz	60/66 MHz	75/83 MHz	100 MHz
60 ns	EDO/FPM	3	3	3	3

Posted Burst Write with Write Buffer Empty		50 MHz	60/66 MHz	75/83 MHz	100 MHz
60 ns	EDO/FPM	3-111	3-111	3-111	3-111

Single Retire Hit		50/60 MHz	66 MHz	75/83 MHz	100 MHz
60 ns	EDO	3	3	3	4
60 ns	FPM	3	4	4	5

Single Retire Row Miss with RAS-CAS = 2T		50/60 MHz	66 MHz	75/83 MHz	100 MHz
60 ns	EDO	5	5	5	6
60 ns	FPM	5	6	6	7

Single Retire Page Miss with RAS-CAS = 2T		50/60 MHz	60/66 MHz	75/83 MHz	100 MHz
60 ns	EDO	8	8	8	8
60 ns	FPM	8	9	9	9

Retire Burst		50/60 MHz	66 MHz	75/83 MHz	100 MHz
60 ns	EDO	x-222	x-222	x-222	x-333
60 ns	FPM	x-222	x-333	x-333	x-444

Table 3-23. SDRAM Performance Summary

Cycle Type	100/83/75 MHz		66/60/50 MHz	
CAS Latency	CL=3	CL=2	CL=3	CL=2
Burst Read Page Hit	8-1-1-1	7-1-1-1	7-1-1-1	6-1-1-1
Read Bank Miss	11-1-1-1	9-1-1-1	10-1-1-1	8-1-1-1
Read Page Miss	14-1-1-1	11-1-1-1	13-1-1-1	10-1-1-1
Back-to-back Burst Read Page Hit	8-1-1-1-1-1-1-1	7-1-1-1-1-1-1-1	7-1-1-1-1-1-1-1	6-1-1-1-2-1-1-1
Write Page Hit	4	4	3	3
Write Row Miss	7	6	6	5
Write Page Miss	10	8	9	7

Posted Write	4-1-1-1	4-1-1-1	3-1-1-1	3-1-1-1
Write Retire rate from Posted Write Buffer	-1-1-1	-1-1-1	-1-1-1	-1-1-1

3.7.4 EDO/FPM DRAM Configuration

ALADDIN-V supports 8 banks of single sided SIMMs or 4 banks of double sided SIMMs maximum so that any mentioned combination can be fully supported. The following diagram shows some possible applications.

Figure 3-7. Two Double-Sided DRAM Banks (EDO/FPM)

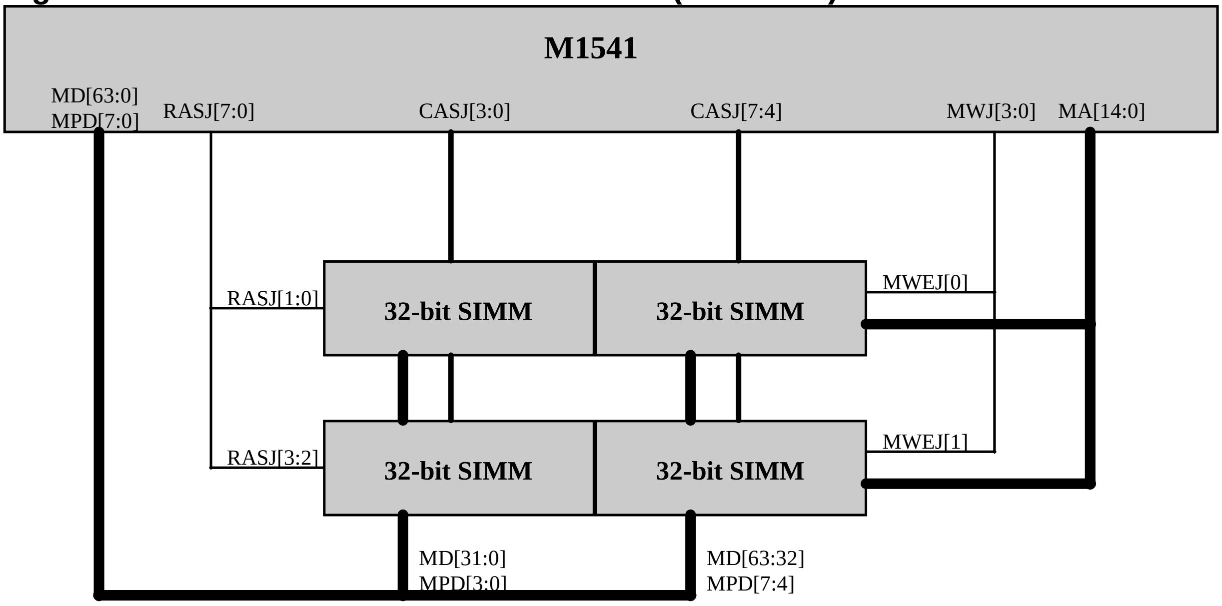
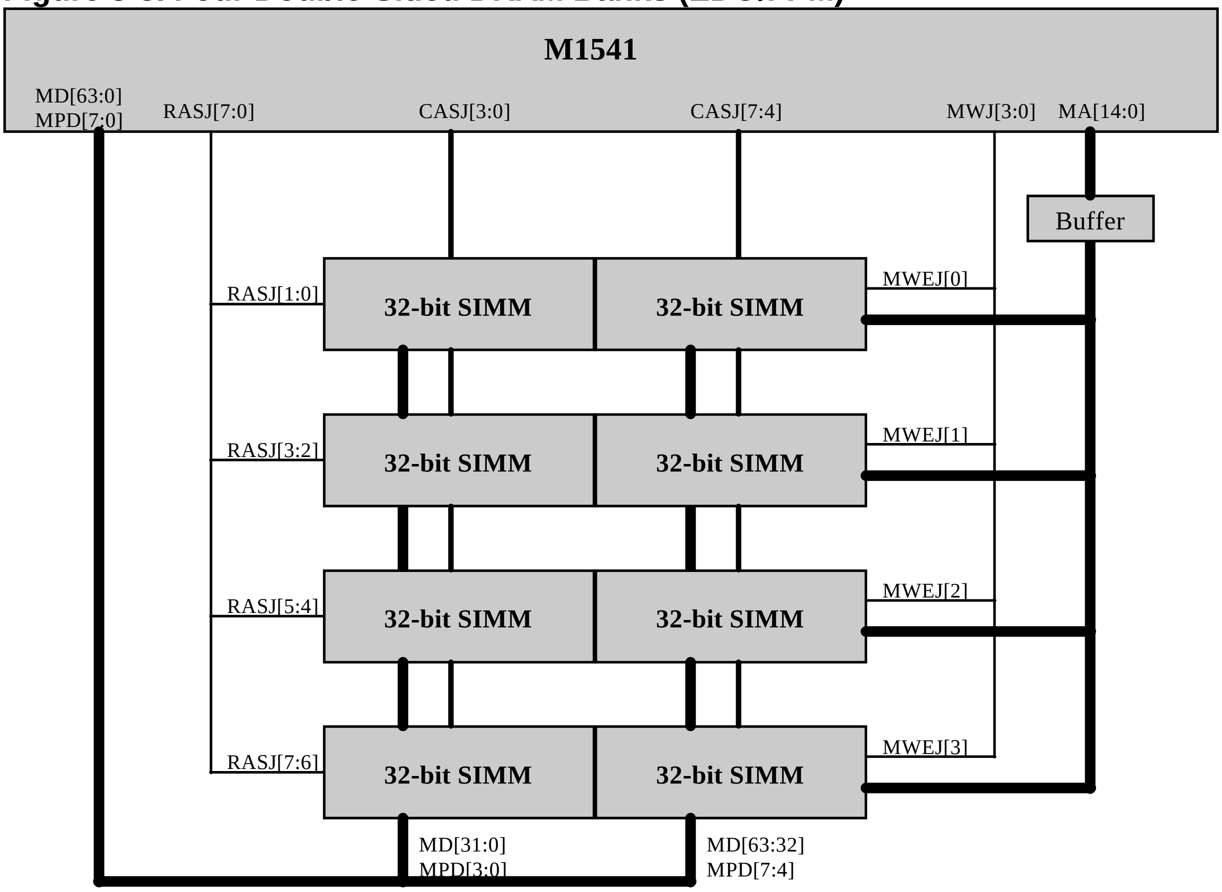


Figure 3-8. Four Double-Sided DRAM Banks (EDO/FPM)



3.7.5 SDRAM Support

Aladdin V supports the most popular synchronous DRAM (SDRAM) at technology of 16Mb, 64Mb, 128Mb, and 256Mb with extra performance and flexibility. Interleaved and linear wrap type for both CAS latency 2 and 3 with burst length 4 are supported. Users are permitted to use pure SDRAM up to 8 banks single sided or 4 banks of double sided, or mix with FPM/EDO DRAM on a row-by-row basis without any constraint. Furthermore, M1541 supports Enhanced Page mode which not only minimizes the effect of CAS latency (CL) and RAS Precharge time (Trp) but also largely enhances the overall performance of the system. JEDEC standard for SDRAM including 2n rule are supported too.

ALADDIN-V utilizes SDRAM commands that support both SDRAM and PC SDRAM. The commands are :

- Mode Register Set (MRS)
- CAS-Before-RAS Refresh (CBR)
- Self-Refresh (SEFR)
- Precharge All Banks (PALL)
- Precharge Selected Bank (PRCH)
- Row Active (RACT)
- Write (WRITE)
- Read (READ)
- No Operation (NOP)
- Device Deselect (DESL)

The following Table shows the command truth table M1541 supports.

Table 3-24. Command Truth Table

Function	Symbol	CKE	CSJ	SRASJ	SCASJ	WEJ	A[14:11]	A10-(AP)	A[9:0]
Mode Register Set	MRS	H *1	L	L	L	L	L	L	V *2
Self-Refresh	SEFR	L	L	L	L	H	L	L	L
Precharge All Banks	PALL	H	L	L	H	L	K	H	K
Precharge Selected Bank	PRCH	H	L	L	H	L	V	L	K
Row Active	RACT	H	L	L	H	H	V *3	V *3	V *3
Write	WRITE	H	L	H	L	L	V	L	V *4
Read	READ	H	L	H	L	H	V	L	V *4
No Operation	NOP	H	L	H	H	H	K	K	K
Device Deselect	DESL	H	H	H	H	H	K	K	K
CAS-before-RAS	CBR	H	L	L	L	H	K	K	K

Notes :

1. V = Valid, L = Logic Low, H = Logic High. K = Keep the value in previous cycle.
2. Please refer to Table 3-25.

3. A[11:0] shows the Row Address.
4. A[11], A[9:0] is used as the Column Address.

In terms of Wrap Type of SDRAM, ALADDIN-V supports both Interleave mode and Linear (Sequential) mode. The following table shows the Mode Register Set Table supported by M1541.

Table 3-25. Mode Register Set

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	ADDRESS
0	0	0	0	0	CAS Latency			Burst Type	Burst Length			Mode Register

A6	A5	A4	CAS Latency	Index-48h bit4
0	1	0	2	1
0	1	1	3	0

A3	Burst Type	Description
0	Sequential	for M1/M2 Linear Wrap Mode
1	Interleave	for P54C/P55C/K5/K6 Interleave mode

A2	A1	A0	Burst Length
0	1	0	4
Others			Not Support

ALADDIN-V supports one set of SDRAM control signals. Following figure show the topological configuration when supporting SDRAM.. The following figure shows 8-bank support of SDRAM.

Figure 3-9. Four DIMMs Architecture

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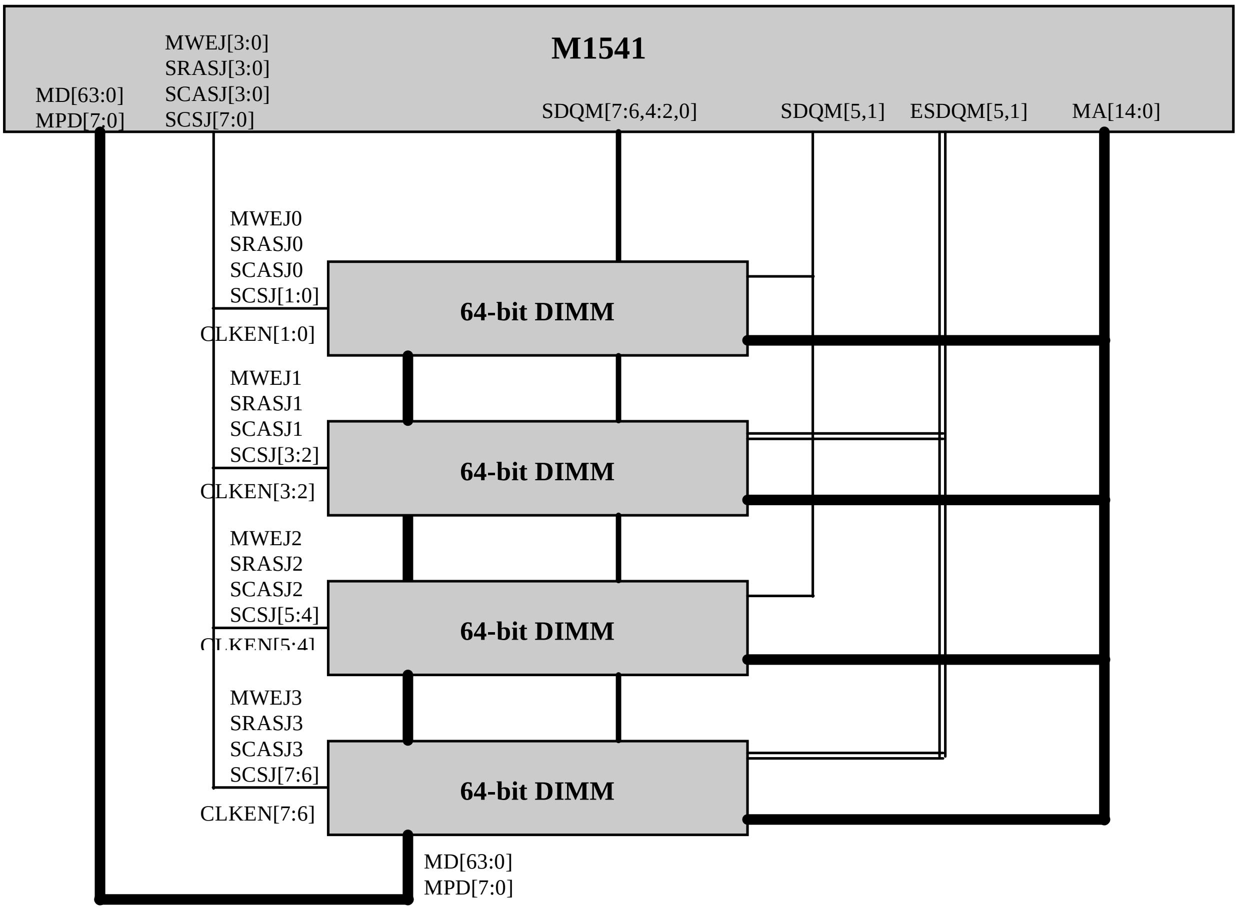
M1541
MWEJ[3:0]
SRASJ[3:0]
SCASJ[3:0]
SCSJ[7:0]
MD[63:0]
MPD[7:0]
SDQM[7:6,4:2,0]
SDQM[5,1]
ESDQM[5,1]
MA[14:0]
MWEJ0
SRASJ0
SCASJ0
SCSJ[1:0]
CLKEN[1:0]
64-bit DIMM
MWEJ1
SRASJ1
SCASJ1
SCSJ[3:2]
CLKEN[3:2]
64-bit DIMM
MWEJ2
SRASJ2
SCASJ2
SCSJ[5:4]
64-bit DIMM
MWEJ3
SRASJ3
SCASJ3
SCSJ[7:6]
CLKEN[7:6]
64-bit DIMM
MD[63:0]
MPD[7:0]

3.7.6 DRAM Load Analysis for each memory configuration and memory type.

The existing versatile/complicated memory configuration, which might result in a big variation of DRAM loading and the control signal timing. ALADDIN-V is designed to target some large reasonable memory types and number of banks to optimize COST and TIMING. If only 4 banks of single sided DRAM SIMMs or 2 banks of double sided DRAM SIMMs or 8banks of single sided DRAM DIMMs or 4 banks of double sided DRAM DIMMs are designed in motherboard, M1541 is designed to be TTL free for the DRAM control signals buffer.

3.8 CPU-to-PCI Posted Write Buffer

The M1541 integrates a 6-DWORD CPU-to-PCI posted write buffer to enhance the CPU-to-PCI performance. With this buffer, the M1541 can minimize the latency of CPU-to-PCI write cycles and maximize the concurrency of CPU bus and PCI bus when CPU writes data to PCI bus. The PCI burst write cycles and fast back-to-back cycles for CPU-to-PCI access are also supported by this buffer.
In addition, the M1541 CPU-to-PCI posted write buffer supports data merge, it can improve the CPU-to-PCI non-32 bits access performance.

3.9 PCI MASTER Latency and Throughput Analysis

The M1541 includes a smart PCI-to-DRAM interface, including a smart deep PCI-to-DRAM buffer and the enhanced PCI arbiter. All these components are designed to optimize the system performance and maximize the PCI bus bandwidth.

3.9.1 Smart Deep Post Write & Pre-fetch Buffer

The smart deep PCI-to-DRAM buffer of M1541 plays the key role to boost PCI master read/write performance. It consists of 80 DWORDs posted write buffer and 22 DWORDs pre-fetch buffer.

The 80 DWORDs PCI-to-DRAM posted write buffers enhance the PCI master bandwidth of accessing DRAM. With the implementation of L1/L2 write back merge and smart buffer management, the M1541 can sustain the ultimate 133-Mbytes/sec bandwidth for PCI master writing to local memory. More significantly, the maximum bandwidth is independent of results from the L1/L2 snooping and write back cycle, the DRAM types and L2 types.

On the other hand, to optimize the PCI master read performance when accessing DRAM, the M1541 includes 22 DWORDs PCI-to-DRAM read pre-fetch buffers. With the implementation of L1/L2 write back and smart buffer management, the M1541 can sustain the ultimate 133 Mbytes/sec bandwidth for PCI Master reading from Local memory. And the maximum bandwidth is independent of results of the L1/L2 snooping, write back cycle and L2 types.

Considering the performance and concurrency of multi-master systems, for example the MPEG/Multimedia applications, the PCI-to-DRAM read pre-fetch buffer of M1541 is configured as two independent units. Each unit pre-fetches and keeps data independently with the other one. With this configuration, the M1541 minimizes the PCI master read latency and reduces the overhead of snooping and pre-fetching.

3.9.2 PCI 2.1 Compliant

The M1541 is fully compliant to the PCI 2.1 Specification. The M1541 supports Passive Release and programmable latency control timers for the first and subsequent data transaction. With the flexible PCI latency control, it can achieve the best system performance.

3.9.3 Pipelined Snoop Ahead

The M1541 utilizes an enhanced pipelined snoop protocol to minimize the L1 & L2 snoop overhead. While snooping L1 & L2, the M1541 also performs speculative read to DRAM such that the latency of master read cycle can be minimized. It combines with the deep smart read/write buffer to optimize PCI master performance.

3.9.4 PCI Arbiter

The M1541 integrates an enhanced PCI arbiter. It provides a fair arbitration by using a PCI and CPU Time Slice mechanism. The arbitration algorithm is also designed to minimize the snoop overhead. Besides the M1533/M1543 ISA bridge and AGP master, the M1541 supports up to 5 PCI masters to make the system motherboard design more flexible and engaging.

To balance the bandwidth of ISA masters and PCI masters and utilize the most bandwidth of PCI bus, the M1541 also supports passive release of PCI 2.1 latency requirements, which makes PCI master access possible when ISA master is active. By this way, the ALADDIN-V can target the best system performance and the most concurrency between PCI bus and ISA bus.

3.9.5 ACPI Support

The M1541 provides the scheme to support ACPI relative functions. By means of PM2_BASE_ADDRESS register (Index-E8h - Index-E9h) and PM2_CONTROL register (Index-EAh bits[1:0]), software can easily enable/disable PCI arbiter as ACPI requirement. In addition, PCIMRQJ signal makes ISA Bridge aware of PCI master bus request to generate SMI/SCI.

3.10 Low Power Features

The ALADDIN-V supports sophisticated power saving features, called Power On Suspend (Sleeping), Suspend to DRAM (Suspend), and Suspend to Disk. Under Power On Suspend state, the system will turn off the signal event of host and keep the DRAM refresh active through the M1541 DRAM interface that is triggered by a 32.768KHz clock source. After the Power On suspend event is triggered, by programming a bit of M1533/M1543 internal register, the M1533/M1543 will initiate a handshake with the M1541. During the handshake, the M1533/M1543 will issue STPCLK to the host, stop the system clock generator, pull the I/O output level to leakageless polarity and turn on the SUSPEND REFRESH circuit to sustain the DRAM data. Theoretically, the only power request under the Power On suspend is the circuit of DRAM suspend refresh. M1541 core has two different power planes, one for the Suspend Refresh circuit, the other is for the other circuit except Suspend Refresh circuit. During Suspend to DRAM state, the system designer can shut off the power except the DRAM suspend refresh circuit to save more system power. Under the Suspend to Disk, only the M1533/M1543 resume circuit is powered and get the minimized system power consumption.

The M1541 and the M1533/M1543 are designed with a very sophisticated I/O circuit and to perform the leakage control under the power saving mode, which is very popular in notebook designs.

For desktop designs, the Power On suspend can provide the system a very efficient **STAND-ON** feature that is more demanding in future home PC systems for Microsoft On Now technology OS.

In the M1533/M1543 of ALADDIN-V, the solution gives a deep green function. Regarding deep PMU for Peripheral device, one

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might design a dedicated PMU device to accompany the Power On suspend feature to form a very deep power saving system, such as a notebook system.

To leave the power saving mode, ALADDIN-V provides several internal event detectors or external event detectors. The system will resume in a very careful/dedicated process and protocol to recover the system to original status, same as the status before entering.

3.11 DRAM Refresh

The M1541 provides CAS-before-RAS (CBR) refresh and RAS-only refresh for FPM DRAM, CAS-before-RAS (CBR) refresh and RAS-only refresh and Extended refresh and self refresh for EDO DRAM, and CAS-before-RAS (CBR) refresh and Self refresh for SDRAMs. FPM/EDO refresh methods use "staggered" and "smart refresh" (i.e. refresh is only performed on banks that are populated) algorithm. The DRAM refresh rate can be controlled via the Index 45h Bits[2:0].

3.12 ECC/Parity Algorithm

The M1541 provides an ECC DRAM data integrity feature. The ECC feature provides single-error correction, double-error detection, and detection of all errors confined to a single nibble (SEC-DEC-S4ED) for DRAM data integrity. The M1541 will generate 8-bit ECC check bits for 64-bit data to DRAM when the ECC feature is enabled and the current DRAM cycle is a write access operation.

If a partial write (less than 64-bit write) event occurs, a read-modified-write operation will be performed by the M1541. The M1541 will detect all single bit, double-bit errors, and all errors confined to a single nibble when ECC is enabled and a DRAM read cycle is performed. The M1541 also corrects all single-bit errors and the corrected data is then transferred to the requester (CPU or PCI). This corrected data will not be written back to DRAM in the current M1541 version. The ECC errors are latched until cleared by software. The software programmer also can detect 64 from 72-bit wide SIMMs or check ECC circuit operations via the ECC (parity) test mode. The ECC check bits (or parities) can be forced to any value during all DRAM write access cycles in the ECC/Parity test mode. All the DRAM read leadoff latency timings should add 1 HCLKIN when the ECC feature is enabled.

The M1541 also provides another DRAM data integrity feature -- conventional DRAM even parity generation and checking when Index 50h bit0 is set to '0'. The DRAM parity checking error reporting condition and status also are defined in Index 50h-51h. The software can differentiate the 64 from 72-bit wide SIMMs or check parity circuit operation via the ECC/Parity test mode. The conventional Parity check will not degrade the system performance.

3.13 AGP and PCI-to-PCI bridge

The M1541 has a built in PCI-to-PCI bridge device to support the AGP interface. The Device ID is M5247. Behind the PCI to PCI bridge is an 66MHz PCI bus which meets the PCI revision 2.1 specification to support the AGP interface. The interface provides three significant performance extensions to the PCI specification which are intended to optimize the AGP for high performance 3D graphics applications. These extensions are

(1) Deep pipeline memory read buffer (32 QWORDs) and memory write buffer (16 QWORDs), fully hiding memory access latency

(2) Demultiplexing of address and data on the bus use the “IDLE band” signals, allowing almost 100% bus efficiency

(3) AC timing for 133 MHz data transfer rate, up to 533 Mbytes/sec data throughput

The M1541 supports a physically, logically and electrically independent AGP interface. Support both the PIPEJ and SBA[7-0] addressing method and RBFJ flow control. The design is following the AGP revision 1.0 specification. The interface will support the PCI 66 mode, AGP 1X mode and 2X modes.

When at PCI 66 mode, the FRAMEJ protocol will be followed.

When at 1X transfer mode, the operation is similar to the PCI. All timings are referenced to the AGP clock. It will provide a peak bandwidth of 266Mbyte/sec.

When at 2X transfer mode, the data transfer rate of the AD, C/BEJ and SBA signals are double. With 2X transfer, QWORD transfers only require one clock cycle, and sideband commands only require one clock per 16-bit command.
For maximum software compatibility, two-level GART (Graphics Address Re-mapping Table) is set up and maintained by mini-port driver supported by ALi. So the actual table implementation is abstracted to a common API.

Besides, the 8 DWORDs PCI to PCI_66 posted write buffer and the 2 DWORDs PCI_66 to PCI posted write buffer make M1541 perform outstanding multi-master system performance. Especially when AGP 3D engine on AGP bus and video processor like MPEG2 accelerator on 33 MHz PCI bus.

Section 4 : Configuration Registers

4.1 Register Summary :

Configuration Cycle Ports			
IO address	**Attribute**	**Name**	**Default Value**
0CF8h	Read/Write	CFGADR - Configuration Address Register	00000000h
0CFCh	Read/Write	CFGDAT - Configuration Data Register	00000000h

M1541 PCI Configuration Space Mapped Registers			
Index	**Attribute**	**Name**	**Default Value**
01h-00h	Read only	VID - Vendor Identification Register	10B9h
03h-02h	Read only	DID - Device Identification Register	1541h
05h-04h	Read/Write	COM - Command Register	0006h
07h-06h	Read Only, Read/Write Clear	DS - Device Status Register	0410h
08h	Read Only	RI - Revision ID Register	00h
09h	Read Only	Reserved Registers	00h
0Ah	Read Only	SCC - Sub-Class Code Register	00h
0Bh	Read Only	CC - Class Code Register	06h
0Ch	Read Only	Reserved Registers	00h
0Dh	Read/Write	LT - PCI Latency Timer value	20h
0Eh	Read only	Device 0 Head Type Register	00h
0Fh	Read only	Reserved Registers	00h
13h-10h	Read only	Device 0 Aperture Base Configuration Register	00000000h
2Bh-14h	Read only	Reserved Registers	00h
2Dh-2Ch	Locked Read/Write	SVID - Sub-Vendor Identification	10B9h
2Fh-2Eh	Locked Read/Write	SDID - Sub-Device Identification	1541h
33h-30h	Read only	Reserved Registers	00h
34h	Locked Read/Write	Device 0 Capabilities Pointer	0bh
3Fh-35h	Read only	Reserved Registers	00h
40h	Read/Write	L12CP - L1, L2 Cache Performance	00h
41h	Read/Write	L2CCI - L2 Cache Configuration-1	-
42h	Read/Write	L2CCII - L2 Cache Configuration-2	00h
43h	Read/Write	PLCTL-Pipe Line Control	00h
44h	Read/Write	FPM/EDO DRAM Timing Configuration - 1	00h
45h	Read/Write	FPM/EDO DRAM Timing Configuration - 2	00h
46h	Read/Write	FPM/EDO DRAM Timing Configuration - 3	00h
47h	Read/Write	FPM/EDO DRAM Timing Configuration - 4	00h
48h	Read/Write	SDRAM Configuration-1	00h
49h	Read/Write	SDRAM Configuration-2	00h
4Ah	Read/Write	DRAM Controller Configuration	00h
4Bh	Read/Write	DRAM Sequencing Configuration	00h
4Ch	Read/Write	DRAM Master Latency-1	00h
4Dh	Read/Write	DRAM Master Latency-2	00h
4Eh	Read/Write	DRAM Master Slice-1	00h
4Fh	Read/Write	DRAM Master Slice-2	00h
50h	Read/Write	ECCP - ECC/Parity Feature	00h

Index	Attribute	Name	Default value
51h	Read/Write	ECCE - ECC or Parity Error Status.	00h
52h	Read/Write	Reserved.	00h
53h	Read/Write	DRAM Posted Write Buffer Control.	00h
54h	Read/Write	Memory Hole.	00h
55h	Read/Write	SMRM - SMRAM Mapping.	00h
56h	Read/Write	SHADRI - SHADOW Regions Read Enable - 1	00h
57h	Read/Write	SHADRII - SHADOW Regions Read Enable - 2	00h
58h	Read/Write	SHADWI - SHADOW Regions Write Enable - 1	00h
59h	Read/Write	SHADWII - SHADOW Regions Write Enable - 2	00h
5Ah	Read/Write	SHADCI - SHADOW Regions Cacheable Enable - 1	00h
5Bh	Read/Write	SHADCII - SHADOW Regions Cacheable Enable - 2	00h
5Ch	Read/Write	Reserved Register	00h
5Dh	Read/Write	DRAM Clock Gated Start Point Control	00h
5Eh	Read/Write	DRAM Refresh Control	00h
5Fh	Read/Write	DRAM Page Mode Counter Control	00h
60h	Read/Write	DB0CI - DRAM Row0 Configuration -1	07h
61h	Read/Write	DB0CII - DRAM Row0 Configuration-2	40h
62h	Read/Write	DB1CI - DRAM Row1 Configuration -1	00h
63h	Read/Write	DB1CII - DRAM Row1 Configuration-2	00h
64h	Read/Write	DB2CI - DRAM Row2 Configuration -1	00h
65h	Read/Write	DB2CII - DRAM Row2 Configuration-2	00h
66h	Read/Write	DB3CI - DRAM Row3 Configuration -1	00h
67h	Read/Write	DB3CII - DRAM Row3 Configuration-2	00h
68h	Read/Write	DB4CI - DRAM Row4 Configuration -1	00h
69h	Read/Write	DB4CII - DRAM Row4 Configuration-2	00h
6Ah	Read/Write	DB5CI - DRAM Row5 Configuration -1	00h
6Bh	Read/Write	DB5CII - DRAM Row5 Configuration-2	00h
6Ch	Read/Write	DB6CI - DRAM Row6 Configuration -1	00h
6Dh	Read/Write	DB6CII - DRAM Row6 Configuration-2	00h
6Eh	Read/Write	DB7CI - DRAM Row7 Configuration -1	00h
6Fh	Read/Write	DB7CII - DRAM Row7 Configuration-2	00h
70h	Read/Write	SDM256MB[7:0] - 256Mbit SDRAM select	00h
71h	Read/Write	SDM4BANK[7:0] - SDRAM internal 2/4 Banks select	00h
72h	Read/Write	SDRAM100 - SDRAM 100 MHz timing select	00h
73h	Read/Write	SDRAM100 - SDRAM 100 MHz timing select	00h
83h-74h	Read only	Reserved Registers	00h
85h-84h	Read/Write	PCI Programmable Frame Buffer Memory Region	00h
86h	Read/Write	CPU to PCI Write Buffer Option	00h
87h	Read/Write	H2PO - CPU to PCI Option	00h

PCI 33 to Host Interface			
Index	**Attribute**	**Name**	**Default value**
88h	Read/write	P2HO - PCI to Main Memory / PCI Arbiter Option	00h
89h	Read/write	PCI Arbiter Time Slice	20h
8Ah	Read/write	CPU Arbiter Time Slice	20h
8Bh	Read/write	PCIRC - PCI Retry Control for P2H cycle	00h
8Ch	Read/write	PCI to Main Memory Option	00h
8Dh	Read/write	PCI Clock Control	00h
8Eh	Read/write	Internal Arbiter Write Control	00h
8Fh	Read/write	Internal Arbiter P2H Read Control	00h
90h	Read/write	LRWCTL – Lock Read/Write Control	00h
91h	Read/write	BRSYCTL - Broadcast and Synchronous Cycle Control	00h
0AFh-92h	Read only	Reserved Registers	00h
AGP Interface Registers			
0B3h-0B0h	Read only	AGP Capability Identifier Registers	0010E002h
0B7h-0B4h	Locked Read/write	AGP Status Registers	1C000203h
0BBh-0B8	Read/write	AGP Command/Enable Registers	00000000h
0BFh-0BCh	Read/write	Aperture Control Register	00000000h
0C3h-0C0h	Read/write	GTLB Control Register	00000000h
0D3h-0D0h	Read/write	L1/L2 Cache Flush Control	00h
0C8h	Read/write	AGP Control Register I	0BFh
0C9h	Read/write	AGP Control Register II	0Ah
0DFh-0C4h	Read Only	Reserved Registers	00h
Green Function Registers			
0E0h	Locked Read/write	Power Management Capability Identifier Register	01h
0E1h	Locked Read/write	Power Management Next Item Pointer Register	00h
0E3h-0E2h	Locked Read/write	Power Management Capabilities Register	0000h
0E5h-0E4h	Locked Read/write	Power Management Control and Status Register	0000h
0E6h	Locked Read/write	PMCSR PCI to PCI Bridge Support Extensions	0000h
0E7h	Locked Read/write	Data Register	00h
0E9h-0E8h	Locked Read/write	Base Address of ACPI PM2_CNTL Port	0000h
0EAh	Read/Write	PM2C - ACPI PM2_CNTL Function	00h
0EBh	Read/Write	GCKCTL - Gated Clock Control Register	00h
0ECh	Read/Write	POD - Programmable Output Driving Strength	00h
0EDh	Read/Write	Hardware Setting Register	00h
0EEh	Read/Write	Miscellaneous - 1	00h
0EFh	Read/Write	Miscellaneous - 2	00h
0F3h	Read/Write	Predict the next SDM Control Signal	00h
0F5h	Read/Write	DMRDPL Status Register	00h
0F6h	Read/Write	GDPL Status Register	00h
0F7h	Read/write	GCLK PLL Control Register	00h
0FFh-0EEh	Read Only	Reserved Registers	00h

ACPI PM2_CNTL I/O Port			
IO address	**Attribute**	**Name**	**Note**
0000h-0FFFFh	Read/Write	PM2_CNTL - ACPI PM2_CNTL I/O Port	The address is defined by M1541 index 0E9h-0E8h

M5243 Configuration Space Mapped Registers			
Index	**Attribute**	**Name**	**Default Value**
01h-00h	Read Only	VID - Vendor Identification Register	10B9h
03h-02h	Locked Read/Write	DID - Device Identification Register	5243h
05h-04h	Read/Write	COM - Command Register	0006h
07h-06h	R Only, R/W Clear	DS - PCI_66 Device Status Register	0400h
08h	Read Only	RI - Revision ID Register	00h
09h	Read Only	Reserved Register	00h
0Ah	Read Only	SCC - Sub-Class Code Register	04h
0Bh	Read Only	CC - Class Code Register	06h
0Ch	Read Only	Reserved Register	00h
0Dh	Read/Write	LT - PCI Latency Timer value	20h
18h-0Eh	Read Only	Reserved Registers	00h
19h	Read/Write	Secondary Bus Number Register	00h
1Ah	Read/Write	Subordinate Bus Number Register	00h
1Bh	Read/Write	Secondary Master Latency Timer Value	20h
1Ch	Read/Write	I/O Base Address Register	0F0h
1Dh	Read/Write	I/O Limit Address Register	00h
1Fh-1Eh	Read/Write	Secondary PCI-to-PCI Status Register	00h
21h-20h	Read/Write	Memory Base Address Register	0FFF0h
23h-22h	Read/Write	Memory Limit Address Register	0000h
25h-24h	Read/Write	Pre-fetchable Memory Base Address Register	0FFF0h
27h-26h	Read/Write	Pre-fetchable Memory Limit Address Register	0000h
33h-28h	Read Only	Reserved Registers	00h
34h	Locked Read/Write	Capability Pointer Register	0E0h
3Dh-35h	Read Only	Reserved Registers	00h
3Fh-3Eh	Read/Write	PCI-to-PCI Bridge Control Register	0000h
83h-40h	Read Only	Reserved Registers	00h
85h-84h	Read/Write	PCI_66 Programmable Frame Buffer Memory Region	0000h
86h	Read/Write	CPU to PCI_66 Write Buffer Option	00h
87h	Read/Write	CPU to PCI_66 Option	00h
PCI_66 to Host Interface			
88h	Read/Write	PCI_66 to Main Memory /PCI_66 Arbiter Option	00h
89h	Read/Write	PCI_66 Arbiter Time Slice	20h
8Ah	Read/Write	CPU Arbiter Time Slice	20h
8Bh	Read/Write	PCI_66 Retry Control for PCI-66 to Host Cycle	00h

8Ch	Read/Write	PCI_66 to Main Memory Option	00h
8Dh	Read Only	Reserved Register	00h
8Eh	Read/Write	AGP Write/AGP Read Arbiter Time Slice	20h
8Fh	Read/Write	PCI_33 to PCI_66 Write Arbiter Time Slice	20h
0DFh-90h	Read Only	Reserved Register	00h
PCI_66 Green Function Support			
0E0h	Locked Read/write	PCI_66 Power Management Capability Identifier Register	01h
0E1h	Locked Read/write	PCI_66 Power Management Next Item Pointer Register	00h
0E3h-0E2h	Locked Read/write	PCI_66 Power Management Capabilities Register	0000h
0E5h-0E4h	Locked Read/write	PCI_66 Power Management Control and Status Register	0000h
0E6h	Locked Read/write	PCI_66 PMCSR PCI-to-PCI Bridge Support extensions	00h
0E7h	Locked Read/write	Data Register	00h
0FFh-E8h	Read Only	Reserved Register	00h

4.2 Configuration Cycle Ports

I. M1541 PCI Mechanism #1 Configuration Cycle Ports

I/O Address : **0CF8h**

Register Name : **CFGADR - Configuration Address Register**

Default Value : 00000000h

Attribute : Read/Write

Size : This register must be 32-bit I/O access in PCI configuration access mechanism #1. An 8-bit or 16-bit access will pass through the Configuration Address Register onto the PCI bus.

Bit Number	Bit Function
31 (0)	PCI Configuration Space Access. 0 : Configuration Disable. 1 : Configuration Enable. When this bit is set to 1, accesses to PCI configuration space are enabled. Otherwise, accesses to PCI configuration space are disabled.
30-24 (00h)	Reserved.
23-16 (00h)	Bus Number. When the bus number is programmed to 00H, the target of the configuration is directly connected to the M1541 and a type 0 configuration cycle is generated. If the bus number is non-zero, a type 1 configuration cycle is generated on the PCI bus.
15-11 (00h)	Device Number. It is used by M1541 to drive the IDSEL lines that select a specific PCI device during initialization. The IDSEL lines are only driven when Bus Number is 0h. As for the others, the M1541 will send the configuration to a PCI or PCI bridge device.
10-8 (0h)	Function Number. It is used to select a specific device function during initialization.
7-2 (00h)	Register Number. It is used to select a specific register during initialization.
1-0 (0h)	Reserved. Fixed at '00'.

I/O Address **0CFCh**

Register Name : **CFGDAT - Configuration Data Register**

Default Value 00000000h

Attribute Read/Write

Size This register may be 8-bit or 16-bit or 32-bit I/O access in configuration access mechanism #1.

Description This register contains the information which is sent or received during the PCI bus data phase of configuration write or read cycles. CPU access of 8, 16 or 32-bit wide to this register are supported.

Note : M1541 only supports PCI mechanism #1 access.

4.3 M1541 PCI Configuration Space Mapped Registers

The M1541 will respond to CPU/PCI configuration access for which AD11=IDSEL is high during the address phase.

Register Index : **01h-00h**

Register Name : **VID - Vendor Identification Register**

Default Value : 10B9h

Attribute : Read Only

Size : 16 bits

Description : This is a 16-bit value assigned to Acer Labs Inc. This register is combined with index 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index : **03h-02h**

Register Name : **DID - Device Identification Register**

Default Value : 1541h

Attribute : Read Only

Size : 16 bits

Description : This is a 16-bit value assigned to the M1541.

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Register Index : **05h-04h**

Register Name : **COM - Command Register**

Default Value : 0006h

Attribute : Read/Write

Size : 16 bits

Bit Number	**Bit Function**
15-9 (000h)	Reserved.
8 (0)	Enable the SERRJ Output Driver. 0 : Disable. 1 : Enable. SERRJ uses an o/d (Open Drain) pad in M1541. The motherboard design should use a pull-up resistor (2.2KΩ) to keep this pin logic high. When the DRAM ECC/Parity check or the PCI Parity check is enabled and an error is found, the M1541 will drive SERRJ low to M1533/M1543 generate NMI when this bit is enabled. Disabling the SERRJ output driver will always keep this output logic high. This bit is reset to 0 and should be set to 1 once memory has been scrubbed by BIOS in systems that wish to report DRAM ECC/Parity error.
7 (0)	Enable Address/Data Stepping. M1541 does not support this feature. Write to this bit has no effect.
6 (0)	Respond to Parity Errors. 0 : Disable. 1 : Enable. The M1541 will do a PCI parity check in CPU to PCI read and PCI to local memory write. This bit is used to enable the parity check. When a parity error is detected, the M1541 will assert SERRJ and set the Parity Error Bit in the DS register.
5 (0)	Enable VGA Palette Snooping. M1541 does not support this feature. Write to this bit has no effect.
4 (0)	Enable Postable Memory Write Command. M1541 does not support this feature. Write to this bit has no effect.
3 (0)	Enable Special Cycle. M1541 does not support this feature. Write to this bit has no effect.
2 (1)	Control to Act As a PCI Bus Master. M1541 does not support to disable bus master operations. This bit is set to 1 during Power-On to enable PCI master operations. Write to this bit has no effect.
1 (1)	Enable Response to Memory Access. M1541 always accepts PCI master accesses to local memory. This bit is read only and always set to 1. Write to this bit has no effect.
0 (0)	Enable Response to I/O Access. M1541 does not respond to any PCI master I/O accesses. Write to this bit has no effect.

Register Index : **07h-06h**

Register Name : **DS - Device Status Register**

Default Value : 0410h

Attribute : Read Only, Read/Write Clear

Size : 16 bits

Bit Number	Bit Function
15 (0)	Detected Parity Error. This bit is set by the M1541 whenever it detects a parity error in a PCI transaction even if parity error handling is disabled (as controlled by bit6 in the command register). Software can reset this bit to 0 by writing a 1 to it.
14 (0)	Signaled System Error. The M1541 will set this bit whenever it asserts SERRJ. Software can reset this bit to 0 by writing a 1 to it.
13 (0)	Received Master Abort. This bit is set by M1541 whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.
12 (0)	Received Target Abort. This bit is set by the M1541 whenever its initiated transaction is terminated with a target abort. This bit is cleared by writing a 1 to it.
11 (0)	Send Target Abort. This bit is set by devices that act as a target to terminate a transaction by target abort. The M1541 never terminates a transaction with target abort therefore this bit is never set. A write to this bit has no effect.
10-9 (10)	DEVSELJ Timing. 00 : Fast. 01 : Medium. 10 : Slow. The M1541 timing for DEVSELJ assertion. Slow timing is selected.
8-5 (0h)	Reserved.
4 (1)	Capability List (CAP_LIST) 1 : The configuration space implements a list of capabilities (Read Only)
3-0 (0h)	Reserved.

Register Index **08h**

Register Name : **RI - Revision ID Register**

Default Value 00h (A0 Stepping)

Attribute Read Only

Size 8 bits

Description This register contains the version number of M1541. The value 00 means A0 stepping. This register will be different at different versions of M1541

Register Index **09h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Register Index **0Ah**

Register Name : **SCC - Sub-Class Code Register**

Default Value 00h : Host Bridge

Attribute : Read Only

Size : 8 bits

Description : These registers contain the sub-Class Codes of the M1541.

Register Index **0Bh**

Register Name : **CC - Class Code Register**

Default Value 06h, Bridge device

Attribute : Read Only

Size : 8 bits

Description : These registers contain the Class Codes of the M1541.

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Register Index **0Ch**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Register Index : **0Dh**

Register Name : **LT - PCI Latency Timer value**

Default Value : 20h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-3 (04h)	Master Latency Timer Count Value. LT is used to control the amount of time the M1541, as a bus master, can burst data to the PCI Bus. It can be used to guarantee a minimum amount of the system resources.
2-0 (0h)	Reserved. They are assumed to be 0 when determining the Count Value.

Register Index : **0Eh**

Register Name : **Device 0 Head Type Register**

Default Value : 00h

Attribute : Read Only

Register Index : **0Fh**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Register Index : **13h-10h**

Register Name : **Device 0 Aperture Base Configuration Register**

Default Value : 00000000h

Attribute : Read Only

Size : 32 bits

Description :

Index 0BCh bit[3-0]		Index 13h-10h = D[31-0]	
0000	0MB	D[31-0] = ‘0’	
0001	1MB	D[31-20] R/W	D[19:0]=’0’
0010	2MB	D[31-21] R/W	D[20:0]=’0’

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0011	4MB	D[31-22] R/W	D[21:0]=’0’
0100	8MB	D[31-23] R/W	D[22:0]=’0’
0110	16MB	D[31-24] R/W	D[23:0]=’0’
0111	32MB	D[31-25] R/W	D[24:0]=’0’
1000	64MB	D[31-26] R/W	D[25:0]=’0’
1001	128MB	D[31-27] R/W	D[26:0]=’0’
1010	256MB	D[31-28] R/W	D[27:0]=’0’

Register Index : **2Bh-14h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Register Index : **2Dh-2Ch**
Register Name : **SVID - Sub-Vendor Identification**
Default Value : 10B9h (for Acer Labs Inc)
Attribute : Locked Read/Write
Size : 16 bits
Description : If Index-90h bit0 = 1, then this port can be Read or Written.

Register Index : **2Fh-2Eh**
Register Name : **SDID - Sub-Device Identification**
Default Value : 1541h
Attribute : Locked Read/Write
Size : 16 bits
Description : If Index-90h bit0 = 1, then this port can be Read or Written.

Register Index : **33h-30h**
Register Name : **Reserved Registers**
Default Value : 00h
Attribute : Read Only

Register Index : **34h**
Register Name : **Device 0 Capabilities Pointer**
Default Value : 0B0h
Attribute : Locked Read/Write
Size : 8 bits
Description : Pointer to the start of AGP standard register block
If index-90h bit 1=1, then this port can be Read or Written

Register Index : **3Fh-35h**
Register Name : **Reserved Registers**
Default Value : 00h
Attribute : Read Only

Register Index : **40h**

Register Name : **L12CP - L1, L2 Cache Performance**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	Reserved
6 (0/1)	Use M1541 as internal TAG RAM 0 : Disable, M1541 internal TAG will not be used 1 : Enable , M1541 internal TAG will be used When powering on, this value will be decided by the HA[23]. The default is pull low and set 0 to Disable the internal TAG. If pull high HA[23], the power on value will set to 1 to enable the TAG. After powering on, this bit can be read and written.
5 (0)	Use M1541 as internal MESI 0 : Enable 1 : Disable This bit is used to support the internal MESI RAMs. When system uses the internal MESI RAMs, this bit must set to 0 (Power on default) to enable internal MESI RAMs for best performance. When disabling this bit, the MESI circuit will use External TAG SRAM as MESI SRAM.
4 (0)	Supports Cyrix M1/M2 "1+4" Burst Mode & K6 Write Allocation Feature. 0 : Disable. 1 : Enable. This bit is used to support the Cyrix M1/M2 "1+4" mode to toggle cache address, DRAM Memory address, and issues the correct KENJ disregarding CPU CACHEJ if it is a local memory cycle. This bit is also used to support K6 Write Allocation Feature. If this bit is enabled, M1541 will assert KENJ during CPU single local memory write cycle.
3 (0)	Supports M1/M2 Linear Burst Order. 0 : Disable. 1 : Enable. This bit is used to support the Cyrix M1/M2 linear burst mode to toggle cache address and DRAM Memory address. When it is disabled, Intel toggle mode (interleaved burst) is selected.
2 (0)	L1 Snoop HITMJ Check Point. 0 : 3rd CPU Clock after asserting EADSJ. 1 : 2nd CPU Clock after asserting EADSJ. This bit controls the HITMJ strobe point during L1 snoop cycle. Value 0 is recommended during normal operation.

1 (0)	L2 Cache Hit/Miss Check Point (L2 Hit/Miss). 0 : T3end (3rd CPU Clock after Sampling ADSJ). 1 : T2end (2nd CPU Clock after Sampling ADSJ). This bit controls the cycle checkpoint of L2 access. When using internal TAG, the Value can be set to 1 for best performance. For external TAGs, the value is decided by the Host frequency and TAG RAM speed. When set to T2end and L2 cache hit, the first BRDYJ sent to CPU will be at the third clock from ADSJ. When set to T3end and L2 cache hit, the first BRDYJ sent to CPU will be at the fourth clock from ADSJ.
0 (0)	L1 Cache ON/OFF. 0 : Disable Internal Cache. 1 : Enable Internal Cache This bit is used to disable or enable L1 cache. When this bit is reset to 0, the M1541 will negate KENJ to prevent either L1 or L2 line fill. When this bit is set to '1', the M1541 will assert KENJ for cacheable memory cycles.

Register Index : **41h**

Register Name : **L2CCI - L2 Cache Configuration-1**

Default Value : Hardware Strobe Value

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7(0)	Reserved
6(0)	CPU read DRAM command mode 0 : Synchronous mode 1 : Bypass mode When this bit is set to bypass mode, DRAM cycle will start at the same cycle assigned by host bus check point defined by index 40h bit 1. Otherwise, one additional clock is added to synchronize for decoding usage.
5 (0/1)	L2 Cache Bank Select. 0 : 1-bank Pipelined Burst SRAM / Memory Cache. 1 : 2-bank Pipelined Burst SRAM / Memory Cache. The default value is determined by power on hardware strobe from HA[19]. If the system does not implement the correct hardware strobe, BIOS should program the correct L2 configuration for normal operation after sorting L2 cache.
4 (0/1)	L2 Cache Type Select. 0 : Pipelined Burst SRAM. 1 : MOSYS DRAM Cache. The default value is determined by hardware strobe from HA[22]. The system must implement the correct hardware strobe for Memory Cache use.
3-2 (0/1,0/1)	L2 Cache Size. 00 : 256 01 : 512K. 10 : 1M. 11 : None. The default value is determined by hardware strobe from HA[21:20]. If the system does not implement the correct hardware strobe, BIOS should program the correct L2 configuration for normal operation after sorting L2 cache.

1 (0)	TAG[9-8] Configuration. 0 : TAG[9-8] are disabled. 1 : TAG[9-8] are enabled. '1' means TAG[9-8] are used to extend cacheable region. When using external TAG SRAM and only one 8-bit wide SRAM is used, then the user must set to disable this bit. If using two 8-bit wide SRAMs or one 10-bit wide SRAM, then enable this bit. The More TAG width, the more cacheable memory range. To enable this bit, the index 41h bit 0 must set to 0.
0 (0)	External TAG Enable 0 : Enable 1 : Disable This bit is used to choose the external TAG. When enabling this bit, at least one 8-bit wide SRAM should be connected to TAG[7-0].

The following L2 Cache Table shows the different configurations supported by M1541.

Table 4-1. Index 40h bit6=0 Disable internal TAG at all cache size
index 40h bit5=1 Enable internal MESI support

Config	DATA SRAM			External TAG SRAM				Internal	Index	Index
Cache Size	Size	Bank	Address lines	Address lines	Data Lines	Ext. Tag Size	Cacheable DRAM Size	MESI 8K1x4	41h Bit[3-2]	41h Bit[1-0]
256K	(32K32)*2 or (32K64)*1	1	A3-A17	A5-A17	A18-A25	8K8	256M	8K2 MESI 8K2 tag	00	00
512K	(64K32)*2 or (64K64)*1	1	A3-A18	A5-A18	A19-A26	16K8	128M	16K2 MESI	01	00
512K	(32K64)*2 (32K32)*4	2	A3-A18	A5-A18	A19-A26	16K8	128M	16K2 MESI	01	00
1M	(64K32)*4 or (64K64)*2	2	A3-A19	A5-A19	A20-A26	32K8	128M	32K1 as dirty bit TAG[7] as valid bit,	10	00
256K	(32K32)*2 or (32K64)*1	1	A3-A17	A5-A17	A18-A27	8K10	1G	8K2 MESI 8K2 tag	00	10
512K	(64K32)*2 or (64K64)*1	1	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	01	10
512K	(32K64)*2 (32K32)*4	2	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	01	10
1M	(64K32)*4 or (64K64)*2	2	A3-A19	A5-A19	A20-A28	32K10	512M	32K1 as dirty bit TAG[9] as valid bit	10	10

Table 4-2. Index 40h bit6=1 Enable internal TAG at all cache size

Config	**DATA SRAM**			**Internal TAG SRAM**				**Internal MESI 8K1x4**	**Index 41h Bit[3-2]**	**Index 41h Bit[1-0]**
Cache Size	**Size**	**Bank**	**Address lines**	**Address lines**	**Data Lines**	**Int. Tag Size**	**Cacheable DRAM Size**			
256K	(32K32)*2 or (32K64)*1	1	A3-A17	A5-A17	A18-A27	8K10	256M	8K2 MESI	00	01
512K	(64K32)*2 or (64K64)*1	1	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	01	01
512K	(32K32)*4 or (32K64)*2	2	A3-A18	A5-A18	A19-A28	16K10	512M	16K2 MESI	01	01
1M	64K32)*4 or (64K64)*2	2	A3-A19	A5-A19	A28-A31 (A20-A27 will use external TAG)	32K4	4G	32K2 MESI (one 32K1 is from internal TAG) External 32K8 TAG required	10	00

Register Index: **42h**

Register Name : **L2CCII - L2 Cache Configuration-2**

Default Value: 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	L2 TAG Output Delay. 0 : Disable. 1 : Enable. This bit is used to increase L2 Tag data hold time when M1541 wants to update the L2 Tag content. The M1541 will delay the Tag data output floating timing by one half CPU clock when this bit is enabled. A '1' is recommended during normal operation.
6 (0)	CPU Single Read Cycle L2 Cache Allocation. 0 : Enable. 1 : Disable. When this bit is disabled, the M1541 will only do the L2 Cache allocation after it decodes the CPU burst line-fill cycle. The CPU single read cycle will start a DRAM single read cycle if this cycle is a DRAM cycle and not hit the L2 Cache. When this bit is enabled, the M1541 will also do the L2 Cache allocation after it decodes the CPU single read cycle. The M1541 will issue the AHOLD to hold CPU cycle, start a burst DRAM read cycle to get the whole line data, write the date to the L2 Cache, and then de-assert AHOLD and return the BRDYJ to CPU. This feature is used to increase the L2 hit rate when CPU issues the single cycle instead of the line-fill cycle in some special application. A '0' is recommended in normal operation.
5 (0)	Cache-ability of Address Region from A0000h to BFFFFh. 0 : Disable. 1 : Enable. This bit is used to enable the cache-ability of address region from A0000h to BFFFFh if this region is programmed as local memory (Index-54h bit3 =1). If Index-54h bit3 = 0, this bit must be 0.
4 (0)	L2 Dirty Bit Setting. 0 : Normal. 1 : Force Non-dirty (Dirty Bit =0).

	When this bit is set to 1, all tag lookups will ignore the tag dirty bit and force non-dirty. This bit is set to 1 only at initializing L2 cache.
3 (0)	L2 force Cache Hit 0 : Disable 1 : Enable When this bit is set to 1, It will force the read memory cycle all are L2 cache hit. This bit is used to initialize L2 cache.
2 (0)	L2 Cache Miss or Invalidate. 0 : Normal. 1 : Force L2 Cache Miss or Invalidate. This will force non-dirty also. When this bit is set to 1, all tag lookups result in a miss. This bit is used to initialize L2 cache. This bit also forces at non-dirty situations.
1 (0)	L2 Dirty Bit Setting. 0 : Normal. 1 : Force Dirty (Dirty Bit =1). When this bit is set to 1, all tag lookups will ignore the tag dirty bit and force dirty. This bit can be used to flush L2 cache in green application. Software can set this bit and then read all L2 cache tag address to flush the cache data to DRAM.
0 (0)	L2 Cache ON/OFF. 0 : Disable External Cache. 1 : Enable External Cache. This bit is used to disable or enable L2 cache.

Register Index : **43h**

Register Name : **PLCTL-Pipe Line Control**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7 (0)	Force Snoop INV 0 : disable 1 : enable When set to enable, all the snoop cycles will be forced INV sent to CPU no matter what the other snoop cycle is read or write to memory.
6 (0)	Dynamic Write Back enable 0 : disable 1 : enable This feature is used to optimize DRAM buffer usage. When CPU issues a write cycle and hits to the L2 Cache, the data will write to L2 cache and also the DRAM Posted Write Buffer if the feature is enabled and the buffer is not full. It can keep L2 cache clean to speed up later L2 cache accesses. If this feature is disabled, the CPU hit L2 Cache write cycle will directly write to L2 Cache and make the hit line as dirty in L2 Tag.
5-4(00)	DRAM Read Pipe Mode 00 : disable 01 : NA slow timing 10 : NA assert Middle timing 11 : NA assert Fast timing This bit is used to enable the assertion of NAJ when the cycle is a DRAM access cycle. When this bit is disabled, the M1541 will not assert NAJ during DRAM access. When set to ‘11’, NAJ will assert when internal host interface send the read control signal to DRAM controller. When set to ‘10’, NAJ will assert when DRAM controller receives the read control signal. When set to ‘01’, NAJ will assert when DRAM controller reads the data from DRAM.
3(0)	Reserved 0 is recommended for normal operation.

2(0)	Single Write Pipe enable 0 : disable 1 : enable This feature is used to optimize pipeline performance. When CPU issues a single write cycle and NAJ will assert to CPU. The assert will be at T2 when bit1 is set to 1.
1(0)	Fast NAJ asserted in single write cycle 0 : disable 1 : enable This bit controls the NAJ assertion point during CPU single write cycle. When enabled, NAJ will assert at T2 to achieve the best CPU single write performance. If set to disable, then NAJ will not send to CPU.
0 (0)	L2 Pipeline Function Option 0 : Disable 1 : Enable This bit is used to enable the assertion of NAJ when the cycle is an L2 access cycle. When this bit is disabled, the M1541 will not assert NAJ during L2 access.

Register Index : **44h**

Register Name : **FPM/EDO DRAM Timing Configuration - 1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	EDO/FPM DRAM to CAS Delay : Trcd ROW Address Hold Time: Trow 1st COL Address Setup Time: Tcol Trcd=Trow+Tcol Trcd Trow Tcol 00: 5T 2T 3T 01: 4T 2T 2T 10: 3T 1T 2T 11: 2T 1T 1T
5-4 (00)	FPM/EDO DRAM Write Timing 00: X-5-5-5 01: X-4-4-4 10: X-3-3-3 11: X-2-2-2 This bit is used to control the FPM/EDO DRAM write timing. Please refer to lead off table in Section 3.5.3 for the X value.
3-2 (00)	EDO DRAM Read Timing 00: X-5-5-5 01: X-4-4-4 10: X-3-3-3 11: X-2-2-2 This bit is used to control the EDO DRAM read timing. Please refer to lead off table in Section 3.5.3 for the X value.

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1-0 (00)	Fast Page Mode DRAM Read Timing 00: X-6-6-6 01: X-5-5-5 10: X-4-4-4 11: X-3-3-3 This bit is used to control the Fast Page Mode DRAM Read timing. Please refer to lead off table in Section 3.5.3 for the X value.

Register Index : **45h**

Register Name : **FPM/EDO DRAM Timing Configuration -2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	EDO/FPM Cycle Time 00: 13T 01: 11T 10: 10T 11: 9T These two bits control the minimum duration of the consecutive RASJ in row miss and refresh cycle.
5-4 (00)	EDO/FPM RAS Pulse Width 00: 7T 01: 6T 10: 5T 11: 4T These two bits control the minimum duration of every RASJ active time.
3 (0)	EDO/FPM Command to command Interval 0: 3T 1: 2T This bit controls the duration of the consecutive command in page hit cycle.
2 (0)	EDO/FPM CAS Pre-charge Time 0: 2T 1: 1T This bit controls the CASJ pre-charge high time.
1-0 (00)	EDO/FPM RAS Pre-charge Time 00: 6T 01: 5T 10: 4T 11: 3T These two bits control the RASJ pre-charge high time in row miss and refresh cycle.

Register Index : **46h**

Register Name : **FPM/EDO DRAM Timing Configuration-3**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7 (0)	Fast Back-to-Back 0 : Disable 1 : Enable If this bit is set to enable, the EDO performance is X-2-2-2-2-2-2-2 when index 44h bit[3-2] (EDO DRAM read timing) is set to '11'. There is no additional turnaround cycle between two cascade pipeline cycles.
6 (0)	EDO Detect Mode 0 : Disable 1 : Enable For the EDO detection procedure, please refer to the DRAM type detection figure in the Hardware and Software programming section.
5-4 (00)	EDO Detection Timer 00 : 128 to 256 CPU CLKs 01 : 256 to 512 CPU CLKs 10 : 512 to 1024 CPU CLKs 11 : 1024 to 2048 CPU CLKs These two bits combined with bit 6 (EDO Detection Mode) are used to do the EDO detection. When bit 6=1, M1541 will latch DRAM data after the EDO detect timer time-out. If the DRAM is EDO then the data will be correct. If it is FPM DRAM, the latch data is error.
3-0 (0h)	Reserved.

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Register Index : **47h**

Register Name : **FPM/EDO DRAM Timing Configuration-4**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-3 (00h)	Reserved
2 (0)	FPM/EDO Bank Miss Insert 1 wait 0: Disable 1: Enable If this bit is enable, FPM/EDO RASJ active will delay 1T to increase MA to RASJ Setup time for row miss cycle.
1 (0)	FPM/EDO Enhanced Page Mode 0: Disable 1: Enable If this bit is enable, all of the FPM/EDO pages will be closed after N memory clocks of idle cycle on DRAM bus. The N is defined at index 5h bit[7-6].
0 (0)	FPM/EDO Bank Miss Detection 0 : Disable 1 : Enable If this bit is enable, the FPM/EDO RASJ pre-charge cycle will be skipped and M1541 will assert RASJ active directly at ROW miss cycle.

Register Index : **48h**

Register Name : **SDRAM Configuration-1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-5 (00)	SDRAM operation mode selection 000 : normal operation 001 : NOP(no operation) command enable 010 : PALL(pre-charge all banks) command enable 011 : MRS(mode register set) command enable 100 : CBR(CAS before RAS refresh) enable 111 : Auto Initialization : only 1 MDR with HA = Mode is needed others : reserved **Note** : (1) Before switching from one mode of SDRAM to another mode, the BIOS should ensure the DRAM buffer is empty. For example, by issuing a DRAM read cycle to flush the DRAM buffer. (2) In the MRS mode, the MA is translated as the column address and the BIOS should issue the appropriate CPU addresses to program the SDRAMs. (3) NOP mode is used to force all CPU cycles to DRAM to generate an SDRAM NOP command on the memory interface. (4) PALL mode is used to force all CPU cycles to DRAM to generate an SDRAM pre-charge all banks command on the memory interface. (5) MRS command is used to convert all CPU cycles to commands on the memory interface. (6) MA[11:0] lines are used to drive command: MA[2:0] = '010' for burst of 4 mode. MA[3] = '1/0' for interleave/linear wrap mode. MA[4] = '1/0' for the value of CAS Latency (3 HCLKINs / 2 HCLKINs). MA[6:5] = '01' and MA[11:7]= '00000'. All these modes are used to initialize SDRAM. Please refer to the hardware and software setup section.

4 (0)	SDRAM CAS Latency Trcd Timing CL Trcd 0 : 3T 3T 1 : 2T 2T This bit is used to control read data valid wait states after read command has been issued. '0' means the CAS Latency is 3 HCLKINs, and 1 means the CAS Latency is 2 HCLKINs. Trcd is defined as the delay time from the “active” command to the “read/write” command.
3-2 (00)	SDRAM RASJ pre-charge time 00 : 5T 01 : 4T 10 : 3T 11 : 2T These two bits are used to control the period from the “pre-charge” command to the “active” command.
1-0 (00)	SDRAM RASJ cycle time and SDRAM RASJ low pulse duration setting Trc Tras 00 : 10T 7T 01 : 9T 6T 10 : 8T 5T 11 : 7T 4T The Trc defines the period from the “refresh/active” command to the “active” command. The Tras defines the period from the “active” command to the “pre-charge” command.

Register Index : **49h**

Register Name : **SDRAM Configuration-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7 (0)	JEDEC "2n rule" restricted 0 : yes 1 : no (the interval between two commands are not limited to be even-numbered) This bit is used to support TI 2n rule SDRAM, the interval between two commands has to be limited to even-numbers.
6 (0)	SDRAM REFRESH cycle Pre-charge all internal banks 0 : Disable 1 : Enable If this bit is enable, the “pre-charge All Banks” command after the “CAS-before-RAS refresh” command will be eliminated.
5 (0)	SDRAM Pre-charge ALL command Insert 1 wait 0 : Disable 1 : Enable If this bit is enable, the “pre-charge all banks”, “pre-charge selected banks” and “row active” commands will delay 1T to increase control signal setup time when index 49h bit2 =1 (SDRAM bank miss detection Enable).
4 (0)	SDRAM Command Insert 1 wait 0 : Disable 1 : Enable If this bit is enable, all the SDRAM commands will delay 1T to increase MA, SRASJ, SCASJ, MWEJ control signal setup time .
3 (0)	SDRAM Enhanced Page Mode 0 : Disable 1 : Enable If this bit is enable, all SDRAM internal banks are closed after ‘N’ memory clocks of DRAM idle cycle. The ‘N’ is defined at index 5Fh bit[7-6] (Enhanced Page Mode counter).

2 (0)	SDRAM Bank Miss Detection 0 : Disable 1 : Enable If this bit is enable, all SDRAM internal banks are closed in page miss cycle. Under this condition, the "active " command is asserted instead of "precharge" command to enhance the row miss performance when row miss happens.
1 (0)	SDRAM Internal Page Detection 0 : Disable 1 : Enable If this bit is enable, M1541 will keep multi-internal banks opened. Such that the possibility of page hit cycle is maximized and improve the row/bank switch performance.
0 (0)	SDRAM Pipe Function 0 : Disable 1 : Enable If this bit is enable, M1541 will optimize the sequence and operate two consequent cycles. If this bit is disable, the next command will begin after the previous data output of the current command.

Register Index : **4Ah**

Register Name : **DRAM Controller Configuration**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	Write Buffer Threshold 00 : 2 LINEs 01 : 4 LINEs 10 : 6 LINEs 11 : 8 LINEs These two bits set the DRAM write buffer threshold. Whenever the content of DRAM write buffer over its threshold and index 4Ah bit5=1 (Write buffer threshold detect enable), the DRAM sequence will treat the DRAM write buffer as the highest priority and grant its arbitration to the DRAM write buffer to avoid the DRAM write buffer full.
5 (0)	Write Buffer Threshold Detect 0 : Disable 1 : Enable This bit is used to control the DRAM sequence to grant its arbitration to DRAM posted write buffer. Whenever the number of the data reside in the DRAM posted write buffer is greater than the threshold set at index 4Ah bit[7-6] (Write buffer threshold). We recommend to enable this bit at normal operation.
4 (0)	Mixed DRAM Command Interval bit 4 FPM/EDO to SDRAM SDRAM to FPM/EDO 0 4 6 1 3 5 This bit is used to prevent the errors when both FPM/EDO and SDRAM at the DRAM bus different banks at the same time. This bit will decide the interval required to exchange the RASJ, CASJ and MWEJ control signal between accessing different types of DRAM composed of FPM/EDO and SDRAM.

3 (0)	Supports two DIMMs only 0 : Disable 1 : Enable If this bit is set to Enable, the M1541 only supports 2 DIMMs SDRAM. The RASJ[7-4] become copy of the RASJ[3-0]. This configuration is designed to share the RASJ loading on two DIMMs layout.
1	Fast Next Mode 0 : Disable 1 : Enable If this bit is disabled, DRAM controller will respond the command immediately. If this bit is enabled, DRAM controller will respond the command sent to DRAM at the next cycle.
2,0 (0)	Reserved.

Register Index : **4Bh**

Register Name : **DRAM Sequencing Configuration**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7 (0)	DRAM Sequencing Parking Select 0 : CPU 1 : AGP This bit decides when there are no request from CPU and AGP, the DRAM sequencing will park the grant to CPU or AGP.
6 (0)	AGP HPR Dominate Arbitration Mode. 0 : Disable 1 : Enable If this bit is enable, DRAM sequencing will distinguish the priority of AGP read request. High-Priority-Read Request of AGP read command will be treated as highest priority then CPU. The second priority is the Low-Priority-Read Request. If disabled, all AGP High-Priority-Read and Low-Priority-Read Requests will be treated as the same.
5-4 (00)	Arbitration Mode 00 : AGP → CPU → PCI → WBF 01 : CPU → AGP → PCI → WBF 10 : CPU → PCI → AGP → WBF 11 : AGP → CPU → PCI → WBF Round Robins These two bits control the arbitration priority of the DRAM sequencer. A DRAM master with higher priority always gets faster service whenever it issues DRAM requests.
3	Snoop first 0 : Disable 1 : Enable After this bit has been enabled, the DRAM sequencer will grant its arbitration to the host whenever a snoop cycle is pending and the host is requesting the usage of the DRAM. The DRAM sequencer will treat the Snoop cycle to be the first priority.

2	DRAM Sequencing Bypass Mode. 0 : Disable 1 : Enable When enabled, the DRAM sequencer will bypass the host request to the DRAM controller as soon as possible. Otherwise, all commands issued to the DRAM controller will be synchronized by the internal clock.
1	GART Table check point 0 : T2 1 : T3 This bit controls the GART hit/miss checkpoint timing. The cycle begins from the issued request command.
0 (0)	Supports DRAM Posted Write Buffer Read-Around-Write Cycle. 0 : Enable 1 : Disable This bit is used to control buffer for back-to-back CPU write and read cycles. Since the M1541 implements the DRAM write buffer to post CPU write cycles, the M1541 will do the read first and then flush the DRAM write buffer if this feature is enabled and the required data of the read cycle do not reside in the buffer. When this bit is disabled, the M1541 will flush the DRAM write buffer data first, and then do the CPU read cycle. A ‘0’ is recommended for normal operation.

Register Index : **4Ch**

Register Name : **DRAM Master latency-1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-4 (0h)	DRAM Write Buffer (DMWBF) Latency. These bits set the DRAM write buffer to DRAM request latency. When the request time is out of the latency, DMWBF will become a higher priority request. 0000 : 0 clock 0001 : 4 clocks 0010 : 8 clocks 0011 : 12 clocks 0100 : 16 clocks 0101 : 20 clocks 0110 : 24 clocks 0111 : 28 clocks 1000 : 32 clocks 1001 : 36 clocks 1010 : 40 clocks 1011 : 44 clocks 1100 : 48 clocks 1101 : 52 clocks 1110 : 56 clocks 1111 : 60 clocks

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3-0 (0h)	Host Latency. These bits set the Host to DRAM request latency. When the request time is out of the latency, Host will become a higher priority request. 0000 : 0 clock 0001 : 4 clocks 0010 : 8 clocks 0011 : 12 clocks 0100 : 16 clocks 0101 : 20 clocks 0110 : 24 clocks 0111 : 28 clocks 1000 : 32 clocks 1001 : 36 clocks 1010 : 40 clocks 1011 : 44 clocks 1100 : 48 clocks 1101 : 52 clocks 1110 : 56 clocks 1111 : 60 clocks

Register Index : **4Dh**

Register Name : **DRAM Master Latency-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-4 (0h)	AGP Latency. These bits set the AGP to DRAM request latency. When the request time is out of the latency, AGP will become a higher priority request. 0000 : 0 clock 0001 : 4 clocks 0010 : 8 clocks 0011 : 12 clocks 0100 : 16 clocks 0101 : 20 clocks 0110 : 24 clocks 0111 : 28 clocks 1000 : 32 clocks 1001 : 36 clocks 1010 : 40 clocks 1011 : 44 clocks 1100 : 48 clocks 1101 : 52 clocks 1110 : 56 clocks 1111 : 60 clocks

3-0 (0h)	PCI Latency. These bits set the PCI DRAM request latency. When the request time is out of the latency, PCI will become a higher priority request. 0000 : 0 clock 0001 : 4 clocks 0010 : 8 clocks 0011 : 12 clocks 0100 : 16 clocks 0101 : 20 clocks 0110 : 24 clocks 0111 : 28 clocks 1000 : 32 clocks 1001 : 36 clocks 1010 : 40 clocks 1011 : 44 clocks 1100 : 48 clocks 1101 : 52 clocks 1110 : 56 clocks 1111 : 60 clocks

Register Index : **4Eh**

Register Name : **DRAM Master Slice-1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-4 (0h)	DMWBF Slice. These bits set the DRAM write buffer to DRAM access slice. After a DRAM request has been granted, the DRAM sequencer will not change its arbitration until the number of access is greater than the slice or the request has been de-asserted. 0000 : 1 command 0001 : 2 commands 0010 : 3 commands 0011 : 4 commands 0100 : 5 commands 0101 : 6 commands 0110 : 7 commands 0111 : 8 commands 1000 : 9 commands 1001 : 10 commands 1010 : 11 commands 1011 : 12 commands 1100 : 13 commands 1101 : 14 commands 1110 : 15 commands 1111 : 16 commands

3-0 (0h)	Host Slice. These bits set the Host to DRAM access slice. After a DRAM request has been granted, the DRAM sequencer will not change its arbitration until the number of access is greater than the slice or the request has been de-asserted. 0000 : 1 command 0001 : 2 commands 0010 : 3 commands 0011 : 4 commands 0100 : 5 commands 0101 : 6 commands 0110 : 7 commands 0111 : 8 commands 1000 : 9 commands 1001 : 10 commands 1010 : 11 commands 1011 : 12 commands 1100 : 13 commands 1101 : 14 commands 1110 : 15 commands 1111 : 16 commands

Register Index : **4Fh**

Register Name : **DRAM Master Slice-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-4 (0h)	AGP Slice. These bits set the AGP to DRAM access slice. After a DRAM request has been granted, the DRAM sequencer will not change its arbitration until the number of access is greater than the slice or the request has been de-asserted. 0000 : 1 command 0001 : 2 commands 0010 : 3 commands 0011 : 4 commands 0100 : 5 commands 0101 : 6 commands 0110 : 7 commands 0111 : 8 commands 1000 : 9 commands 1001 : 10 commands 1010 : 11 commands 1011 : 12 commands 1100 : 13 commands 1101 : 14 commands 1110 : 15 commands 1111 : 16 commands

3-0 (0h)	PCI Slice. These bits set the PCI to DRAM access slice. After a DRAM request has been granted, the DRAM sequencer will not change its arbitration until the number of access is greater than the slice or the request has been de-asserted. 0000 : 1 command 0001 : 2 commands 0010 : 3 commands 0011 : 4 commands 0100 : 5 commands 0101 : 6 commands 0110 : 7 commands 0111 : 8 commands 1000 : 9 commands 1001 : 10 commands 1010 : 11 commands 1011 : 12 commands 1100 : 13 commands 1101 : 14 commands 1110 : 15 commands 1111 : 16 commands

Register Index : **50h**

Register Name : **ECCP - ECC/Parity Feature**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	Reserved.
6 (0)	SERRJ Duration. 0 : SERRJ will be asserted for 1 PCI Clock. 1 : SERRJ will be asserted until all the ECC(parity) Error Flags are cleared. When the M1541 detects an ECC or parity error, the M1541 will assert SERRJ for 1 PCI Clock (pulse mode) if this bit is set to '0'. Otherwise, the M1541 will assert the SERRJ to report the memory error until all the ECC/parity error flags are cleared (level mode). This bit is used to control the assertion time of SERRJ.
5 (0)	SERRJ on Parity or Multiple-bit ECC Error. 0 : Disable 1 : Enable. When this bit is set to '0', the M1541 will not assert the SERRJ signal when the memory parity or multiple-bit error occurs. Disabling this bit will disable the DRAM parity error check or DRAM ECC multiple-bit error check. Otherwise, the memory data error will be reported to the system via SERRJ assertion to generate NMI (Non-Maskable Interrupt).
4 (0)	SERRJ on Single-bit ECC Error. 0 : Disable. 1 : Enable. When this bit is set to '0', the M1541 will not assert SERRJ on single-bit DRAM ECC errors. Disabling this bit will disable the DRAM ECC single-bit error check. Otherwise, the M1541 will assert SERRJ to generate NMI (Non-Maskable Interrupt) when it detects a single-bit DRAM ECC error.
3-1 (000)	Reserved.
0 (0)	DRAM Data Integrity Mode. 0 : Parity. 1 : ECC.

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	When this bit is set to '0', the DRAM data integrity will be implemented by the parity algorithm. Otherwise, the ECC data integrity will be implemented.

Register Index : **51h**

Register Name : **ECCE - ECC or Parity Error Status**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-5 (0h)	ECC Multiple-bit or Parity First Row error. These 3 bits record the first row associated with the ECC multiple-bit or parity error. When an error is detected, these bits are updated and ECCE[4] (this index bit[4]) is set.
4 (0)	ECC Multiple-bit Error or Parity Error Flag. The M1541 sets this bit to '1' when either an ECC multiple-bit error or parity error has been detected, depending on whether ECC or parity feature is enabled, respectively. A write of '1' by software to ECCE[4] will clear this bit and write of '0' has no effect on it.
3-1 (0h)	ECC Single-bit First Row Error. These 3 bits record the first row associated with the ECC single-bit error. When an error is detected, these bits are updated and ECCE[0] is set.
0 (0)	ECC Single-bit Error Flag. The M1541 sets this bit to '1' when an ECC single-bit error has been detected and the ECC function is enabled. A write of '1' by software to ECCE[0] will clear this bit and write of '0' has no effect on it.

Register Index : **52h**

Register Name : **Reserved**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Register Index : **53h**

Register Name : **DRAM Posted Write Buffer Control**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	CPU IDLE SEL TIMER 00 : 2 CPU CLKs 01 : 4 CPU CLKs 10 : 6 CPU CLKs 11 : 8 CPU CLKs The CPU idle select timer is used to control the clock that keep internal host clock running when gated clock is enable.
5 (0)	CPU to DRAM Posted Write Buffer Concurrent with PCI-to-DRAM Write 0 : Enable 1 : Disable If disabled, the CPU to DRAM posted write buffer cycle will not be concurrent with PCI-to-DRAM write cycle.
4 (0)	CPU-to-DRAM Posted Write Buffer Concurrent with PCI-to-DRAM Read. 0 : Enable 1 : Disable If this bit is set to disable, the CPU to DRAM posted write buffer cycle will not be concurrent with PCI-to-DRAM read cycle.
3-1 (00)	DRAM Posted Write Buffer Idle Flush Timer 000 : 4 clocks 001 : 8 clocks 010 : 12 clocks 110 : 16 clocks 111 : 32 clocks Other : reserved These three bits control the IDLE flush timer of DRAM post write buffer when index 53h bit0 is set to enable.

0 (0)	DRAM Posted Write Buffer Idle Flush 0 : Enable 1 : Disable This option enables the idle timer for each line of DRAM posted write buffer. By enabling this option, M1541 will keep data in DRAM posted write buffer until that idle timer timeout then flush the data. Otherwise, the posted write data will be always flushed without any latency time.

Register Index : **54h**

Register Name : **Memory Hole**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-6 (00)	Reserved.
5 (0)	14-15M Memory Location. 0 : Local Memory Area. 1 : Non-Local Memory Area. When this bit is set to '1', all memory access address from 14M to 15M will be decoded as local memory cycle and access local DRAM if total memory size is beyond 15M. Otherwise, it will be decoded as non-local memory and pass through to PCI bus.
4 (0)	15-16M Memory's Location. 0 : Local Memory Area. 1 : Non-Local Memory Area. When this bit is set to '1', all memory access address from 15M to 16M will be decoded as local memory cycle and access local DRAM if total memory size is beyond 16M. Otherwise, it will be decoded as non-local memory and pass through to PCI bus.
3 (0)	Page A-B as Local Memory Area. 0 : Non-local Memory Area. 1 : Local Memory Area. When this bit is set to '1', all memory access address from A0000h to BFFFFh will be decoded as local memory cycle and access local DRAM. Otherwise, it will be decoded as non-local memory and pass through to PCI bus.
2 (0)	Force Address Region 80000h-9FFFFh as Non-local Memory Area. 0 : Local Memory Area. 1 : Non-local Memory Area. When this bit is set to '1', all memory access address from 80000h to 9FFFFh will be decoded as non-local cycle and pass through PCI bus. Otherwise, it will be decoded as local memory and access to DRAM.
1-0 (00)	Reserved.

Register Index : **55h**

Register Name : **SMRM - SMRAM Mapping**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-5 (0h)	Reserved.
4 (0)	SMM Page -A or -B Region Code/Data Split. 0 : Disable. 1 : Enable. **Note**: This bit is valid only if this register bit [3:2]="01". When this bit is enabled, only the cycle command with DCJ='0' can access SMRAM. The CPU data access will pass through PCI bus.
3-2 (00)	SMRAM Region. 00: SMM Region at D000 Segment will be re-mapped to B000 Segment. 01: SMM Region at A000 or B000 Segment. 10: SMM Region at 3000 Segment will be re-mapped to B000 Segment. 11 : Reserved. Please refer to the following table.6-5
1 (0)	SMRAM Access Control. 0 : Disable. 1 : Enable. When this bit is disabled, SMRAM can only be accessed during SMI handler. Otherwise, SMRAM area can be accessed any time. This bit is used in SMRAM initialization and must be set to '0' when the initialization process is finished.
0 (0)	Supports SMRAM Mapping. 0 : Disable. 1 : Enable. This bit is used to disable or enable SMRAM Mapping.

Table 4-3 The following is M1541 address re-mapping table for SMRAM mapping enable.

Bit [3-1]	SMIACTJ	CPU Logical Address	Re-mapped Physical Address	Access DRAM Y/N
000	0	D0000	B0000	Y
000	1	D0000	non-local	N
001	X	D0000	B0000	Y
010	0	A0000/ B0000	A0000/ B0000	Y
010	1	A0000/ B0000	non-local	N
011	X	A0000/ B0000	A0000/ B0000	Y
100	0	30000	B0000	Y
100	1	30000	30000	Y
101	X	30000	B0000	Y

Register Index : **56h**

Register Name : **SHADRI - SHADOW Regions Read Enable - 1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	DC000h-DFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region DC000h-DFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
6 (0)	D8000h-DBFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D8000h-DBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
5 (0)	D4000h-D7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D4000h-D7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
4 (0)	D0000h-D3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D0000h-D3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
3 (0)	CC000h-CFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region CC000h-CFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

2 (0)	C8000h-CBFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C8000h-CBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
1 (0)	C4000h-C7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C4000h-C7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
0 (0)	C0000h-C3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C0000h-C3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

Register Index : **57h**

Register Name: **SHADRII - SHADOW Regions Read Enable - 2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	FC000h-FFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable When this bit is enabled, address region FC000h-FFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
6 (0)	F8000h-FBFFFh Shadow Region Read Enable. 0 : Disable 1 : Enable. When this bit is enabled, address region F8000h-FBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
5 (0)	F4000h-F7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region F4000h-F7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
4 (0)	F0000h-F3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region F0000h-F3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
3 (0)	EC000h-EFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region EC000h-EFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

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2 (0)	E8000h-EBFFFh Shadow Region Read Enable 0 : Disable. 1 : Enable. When this bit is enabled, address region E8000h-EBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
1 (0)	E4000h-E7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region E4000h-E7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
0 (0)	E0000h-E3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region E0000h-E3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

Register Index : **58h**

Register Name : **SHADWI - SHADOW Regions Write Enable - 1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7(0)	DC000h-DFFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region DC000h-DFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
6 (0)	D8000h-DBFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D8000h-DBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
5 (0)	D4000h-D7FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D4000h-D7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
4 (0)	D0000h-D3FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region D0000h-D3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
3 (0)	CC000h-CFFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region CC000h-CFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

2 (0)	C8000h-CBFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C8000h-CBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
1 (0)	C4000h-C7FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region C4000h-C7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
0 (0)	C0000h-C3FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When the above bits are enabled, the corresponding memory address region write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

Register Index : **59h**

Register Name : **SHADWII - SHADOW Regions Write Enable - 2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	FC000h-FFFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region FC000h-FFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
6 (0)	F8000h-FBFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region F8000h-FBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
5 (0)	F4000h-F7FFFh Shadow Region Write Enable 0 : Disable. 1 : Enable. When this bit is enabled, address region F4000h-F7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
4 (0)	F0000h-F3FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region F0000h-F3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
3 (0)	EC000h-EFFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region EC000h-EFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

2 (0)	E8000h-EBFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region E8000h-EBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
1 (0)	E4000h-E7FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region E4000h-E7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.
0 (0)	E0000h-E3FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable. When this bit is enabled, address region E0000h-E3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

Register Index : **5Ah**

Register Name : **SHADCI - SHADOW Regions Cacheable Enable - 1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	DC000h-DFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[7] = '1', address region DC000h-DFFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
6 (0)	D8000h-DBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[6] = '1', address region D8000h-DBFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
5 (0)	D4000h-D7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[5] = '1', address region D4000h-D7FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
4 (0)	D0000h-D3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[4] = '1', address region D0000h-D3FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
3 (0)	CC000h-CFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[3] = '1', address region CC000h-CFFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.

2 (0)	C8000h-CBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[2] = '1', address region C8000h-CBFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
1 (0)	C4000h-C7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable When this bit is enabled and SHADRI[1] = '1', address region C4000h-C7FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
0 (0)	C0000h-C3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRI[0] = '1', address region C0000h-C3FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.

Register Index : **5Bh**

Register Name : **SHADCII - SHADOW Regions Cacheable Enable - 2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	FC000h-FFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[7] = '1', address region FC000h-FFFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
6 (0)	F8000h-FBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[6] = '1', address region F8000h-FBFFFh memory access will become cacheable. Otherwise, it will be non-cacheable
5 (0)	F4000h-F7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[5] = '1', address region F4000h-F7FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
4 (0)	F0000h-F3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[4] = '1', address region F0000h-F3FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
3 (0)	EC000h-EFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[3] = '1', address region EC000h-EFFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.

2 (0)	E8000h-EBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[2] = '1', address region E8000h-EBFFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
1 (0)	E4000h-E7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[1] = '1', address region E4000h-E7FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.
0 (0)	E0000h-E3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable. When this bit is enabled and SHADRII[0] = '1', address region E0000h-E3FFFh memory access will become cacheable. Otherwise, it will be non-cacheable.

Register Index : **5Ch**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read/Write

Register Index : **5Dh**

Register Name : **DRAM Clock Gated Start Point Control**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-5,3 (0)	Reserved
4 (0)	Ignore DRAM Posted Write Buffer (DMWBF) over threshold when other is latency out 0 : Disable 1 : Enable This bit is used to mask the feature set at index 4Ah bit5. When DRAM write buffer over the threshold will be ignore if there is any other DRAM request which is out of latency when this bit is set to '1'. --
2 (0)	CLKEN gated control enable for notebook power saving 0 : Disable 1 : Enable This bit is used to control the gated clock circuit. When enabling this bit, the SDRAM interface is idle. The SDRAM CLKEN will insert to reduce the SDRAM power consumption.
1-0 (00)	DRAM Controller Gated Clock Timer 00 : 12 CPU CLKs -- Wake up delay 1 wait 01 : 8 CPU CLKs – Wake up delay 1 wait 10 : 8 CPU CLKs – Wake immediately 11 : 4 CPU CLKs – Wake immediately These two bits control the gated time and wakeup up time of the DRAM sequencer and the DRAM controller.

Register Index : **5Eh**

Register Name : **DRAM Refresh Control** (00h, R/W)

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	FPM/EDO Refresh Mode 0 : CAS before RAS Refresh 1 : RAS only Refresh This bit is used to control DRAM refresh mode. In suspend mode, only the CAS-before-RAS mode is supported to save power consumption.
6 (0)	Self Refresh Mode 0 : Disable 1 : Enable This bit is used to support the self-refresh function of EDO/FPM DRAM.
5-4 (00)	Refresh period adjustment when CPU CLOCK changes 00 : Refresh period/1 when CPU clock /1 01 : Refresh period/2 when CPU clock /2 10 : Refresh period/4 when CPU clock /4 11 : Refresh period/8 when CPU clock /8 When system enters power saving mode, some system will reduce the CPU frequency. When CPU frequency is reduced, in order to sustain the same refresh rate. These two bits must be set to adjust the refresh period which is based on CPU frequency.
3 (0)	Refresh Queue 0 : Disable 1 : Enable This bit is used to control the DRAM Refresh Queue. M1541 has implemented 4 DRAM Refresh Queues. When DRAM refresh request collides with DRAM bus activity, this DRAM refresh will be delayed until the DRAM bus activity is finished. If the DRAM Refresh Queues are full, the DRAM refresh request becomes the top priority, and the other DRAM bus activity will be delayed.

2-0 (0)	DRAM Refresh Period 000 : 1024 CPU Clocks (15 us in 66Mhz). 001 : 2048 CPU Clocks (30 us in 66Mhz). 010 : 4096 CPU Clocks (60 us in 66Mhz). 011 : 8192 CPU Clocks (120 us in 66Mhz). 100 : 16384 CPU Clocks (256 us in 66Mhz). These three bits are used to control the period to refresh DRAMs

Register Index : **5Fh**

Register Name : **DRAM Page Mode Counter Control (00h, R/W)**

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	Enhanced Page Mode Counter 00 : 4 CPUCLKs 01 : 8 CPUCLKs 10 : 12 CPUCLKs 11 : 16 CPUCLKs These two bits decide the duration from the time that sequencing have not accept a command, then close all DRAM pages after this duration.
5-1 (00h)	Reserved.
0 (0)	DRAM Refresh Function 0 : Enable 1 : Disable If this bit is enable, DRAM controller performs refresh cycle according to the period defined by x5Eh[2:0]. Otherwise, the DRAM controller will not perform refresh cycle.

Register Index : **60h**

Register Name : **DB0CI - DRAM Row0 Configuration -1**

Default Value : 07h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0 (07h)	Row0 DRAM Top Address Boundary-1. A27-A20 Address Boundary.

Register Index : **61h**

Register Name : **DB0CII - DRAM Row0 Configuration-2**

Default Value : 40h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (01)	DRAM MA Definition. When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01) 00 : Row0 DRAM Memory address mapping is Disable 01 : Row0 DRAM Memory address mapping uses Table 4-4. 10 : Row0 DRAM Memory address mapping uses Table 4-5. 11 : Row0 DRAM Memory address mapping uses Table 4-6. When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11) 00 : Row0 DRAM Memory address mapping uses Table 4-7 01 : Row0 DRAM Memory address mapping uses Table 4-8 10 : Row0 DRAM Memory address mapping uses Table 4-9 11 : Row0 DRAM Memory address mapping uses Table 4-10 These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 0.
5-4 (0h)	Row0 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Registered Synchronous DRAM 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 0.
3-0 (0h)	Row0 DRAM Top Address Boundary-2. A31-A28 Address Boundary.

	These four bits are used to combine index-60h to decide the top memory size for DRAM Row 0.

Table 4-4. The following types of FPM/EDO DRAMs are supported when bits [7:6] = '01'.

Memory Organization	Memory Size	Row Address	Column Address
512Kx8	4Mb	10	9
1Mx4	4Mb	10	10
1Mx16	16Mb	10	10
2Mx8	16Mb	11	10
4Mx4	16Mb	11	11
4Mx4	16Mb	12	10

Table 4-5. The following types of FPM/EDO DRAMs are supported when bits [7:6] = '10'.

Memory Organization	Memory Size	Row Address	Column Address
4Mx16	64Mb	11	11
8Mx8	64Mb	12	11
16Mx4	64Mb	12	12

Table 4-6. The following types of FPM/EDO DRAMs are supported when bits [7:6] = '11'.

Memory Organization	Memory Size	Row Address	Column Address
1Mx16	16Mb	12	8
2Mx8	16Mb	12	9

Table 4-7. The following types of SDRAMs are supported when bit[7:6] = '00'

Memory Organization	Memory Size	Row Address	Column Address
2Bx512Kx16	16Mb	11	8
2Bx2Mx16	64Mb	13	8
4Bx1Mx16	64Mb	12	8
4Bx512Kx32	64Mb	11	8

Table 4-8. The following types of SDRAMs are supported when bit[7:6] = '01'

Memory Organization	Memory Size	Row Address	Column Address
2Bx1Mx8	16Mb	11	9
2Bx4Mx8	64Mb	13	9
4Bx2Mx8	64Mb	12	9
4Bx1Mx16	64Mb	11	9
2Bx4Mx16	128Mb	13	9
4Bx2Mx16	128Mb	12	9
2Bx8Mx16	128Mb	14	9
4Bx4Mx16	128Mb	13	9

Table 4-9. The following types of SDRAMs are supported when bit[7:6] = '10'

Memory Organization	Memory Size	Row Address	Column Address
2Bx2Mx4	16Mb	11	10
2Bx8Mx4	64Mb	13	10
4Bx4Mx4	64Mb	12	10
4Bx2Mx8	64Mb	11	10

2Bx8Mx8	128Mb	13	10
4Bx4Mx8	128Mb	12	10
2Bx16Mx8	256Mb	14	10
4Bx8Mx8	256Mb	13	10

Table 4-10. The following types of SDRAMs are supported when bit[7:6] = '11'

Memory Organization	Memory Size	Row Address	Column Address
2Bx16Mx4	128Mb	13	11
4Bx8Mx4	128Mb	12	11
2Bx32Mx4	256Mb	14	11
4Bx16Mx4	256Mb	13	11

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The M1541 supports 8 rows of DRAM. DRAM Rowx Configuration register defines populated DRAM type and Top Address Boundary for each row. DB0CI and DB0CII define for Row 0, DB1CI and DB1CII define for Row 1, DB2CI and DB2CII define for Row 2, DB3CI and DB3CII define for Row 3, DB4CI and DB4CII define for Row 4, DB5CI and DB5CII define for Row 5, B6CI and DB6CII define for Row 6, and DB7CI and DB7CII define for Row 7. Contents of these 8-bit registers represent the boundary address in 1MB granularity and DRAM type populated.

The M1541 uses " Not less than" policy to determine which row memory address resides. For this reason, the address boundary for each row in index 6Fh to 60h should be the maximum memory value (Top address boundary) minus 1, as the following below description.

DB0CII[3:0]&DB0CI[7:0] = Total amount of memory in row0 -1 (Unit: 1MB).

DB0CII[5:4] define different DRAM Type for row0.

DB0CII[7:6] define different MA Type or unpopulated for row0.

DB1CII[3:0]&DB1CI[7:0] = Total amount of memory in (row0 + row1) - 1 (Unit: 1MB).

DB1CII[5:4] define different DRAM Type for row1.

DB1CII[7:6] define different MA Type or unpopulated for row1.

DB2CII[3:0]&DB2CI[7:0] = Total amount of memory in (row0 + row1 + row2) - 1 (Unit: 1MB).

DB2CII[5:4] define different DRAM Type for row2.

DB2CII[7:6] define different MA Type or unpopulated for row2.

DB3CII[3:0]&DB3CI[7:0] = Total amount of memory in (row0 + row1 + row2 + row3) - 1 (Unit: 1MB).

DB3CII[5:4] define different DRAM Type for row3.

DB3CII[7:6] define different MA Type or unpopulated for row3.

DB4CII[3:0]&DB4CI[7:0] = Total amount of memory in (row0 + row1 + row2 + row3 + row4) - 1 (Unit: 1MB).

DB4CII[5:4] define different DRAM Type for row4.

DB4CII[7:6] define different MA Type or unpopulated for row4.

DB5CII[3:0]&DB5CI[7:0] = Total amount of memory in (row0 + row1 + row2 + row3 + row4 + row5) -1 (Unit: 1MB).

DB5CII[5:4] define different DRAM Type for row5.

DB5CII[7:6] define different MA Type or unpopulated for row5.

DB6CII[3:0]&DB6CI[7:0] = Total amount of memory in (row0 + row1 + row2 + row 3 + row4 + row5 + row6) -1 (Unit: 1MB).

DB6CII[5:4] define different DRAM Type for row6.

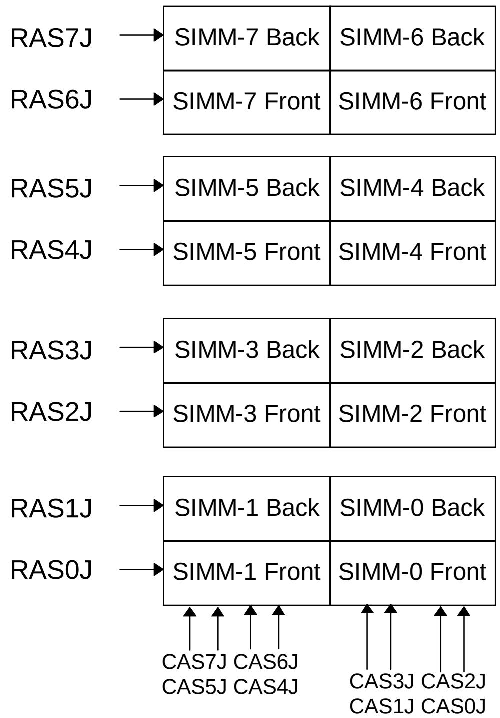
DB6CII[7:6] define different MA Type or unpopulated for row6.

DB7CII[3:0]&DB7CI[7:0] = Total amount of memory in (row0 + row1 + row2 + row3 + row4 + row5 + row6 + row7) -1 (in 1MB).

DB7CII[5:4] define different DRAM Type for row7.

DB7CII[7:6] define different MA Type or unpopulated for row7.

As an example of a system configuration where 8 physical rows are configured for either single-sided or double-sided SIMMs, the DRAM will be configured like the following figure.



In this configuration, the M1541 will drive two RASJ lines to the SIMM bank. If the single-sided SIMMs are populated, the even RASJ is used and the odd RASJ is not used. If the double-sided SIMMs are populated, both RASJ lines are used.

Example A

Two single-sided 1MB X 32 FPM DRAMs (standard MA mapping) are populated at row 0, a total of 8 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 07h DB0CII = 40h
DB1CI = 07h DB1CII = 00h
DB2CI = 07h DB2CII = 00h
DB3CI = 07h DB3CII = 00h
DB4CI = 07h DB4CII = 00h
DB5CI = 07h DB5CII = 00h
DB6CI = 07h DB6CII = 00h
DB7CI = 07h DB7CII = 00h

Example B

Four single-sided 1MB X 32 EDO DRAMs (1Mx16 MA mapping) are populated on row 0 and row 2, a total of 16 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 07h DB0CII = D0h
DB1CI = 07h DB1CII = 00h
DB2CI = 0Fh DB2CII = D0h
DB3CI = 0Fh DB3CII = 00h
DB4CI = 0Fh DB4CII = 00h
DB5CI = 0Fh DB5CII = 00h
DB6CI = 0Fh DB6CII = 00h
DB7CI = 0Fh DB7CII = 00h

Example C

Two double-sided 2MB X 32 FPM DRAMs (standard MA mapping) are populated on row 4 , row 5, row 6, and row 7, a total of 32 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 00h DB0CII = 00h
DB1CI = 00h DB1CII = 00h
DB2CI = 00h DB2CII = 00h
DB3CI = 00h DB3CII = 00h

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DB4CI = 07h DB4CII = 40h

DB5CI = 0Fh DB5CII = 40h

DB6CI = 17h DB6CII = 40h

DB7CI = 1Fh DB7CII = 40h

Example D

One double-sided 2MB X 32 EDO DRAMs (1Mx16 MA mapping) are populated on row 2 and row 3, and one double-sided 8MB X 32 FPM DRAMs (64Mb MA mapping) are populated on row 6 and row 7, a total of 80 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 00h DB0CII = 00h

DB1CI = 00h DB1CII = 00h

DB2CI = 07h DB2CII = D0h

DB3CI = 0Fh DB3CII = D0h

DB4CI = 0Fh DB4CII = 00h

DB5CI = 0Fh DB5CII = 00h

DB6CI = 2Fh DB6CII = 80h

DB7CI = 4Fh DB7CII = 80h

Register Index : **62h**

Register Name : **DB1CI - DRAM Row1 Configuration -1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	Row1 DRAM Top Address Boundary- 1. A27-A20 Address Boundary.

Register Index : **63h**

Register Name : **DB1CII - DRAM Row1 Configuration-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	DRAM MA Definition. When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01) 00 : Row1 DRAM Memory address mapping is Disable 01 : Row1 DRAM Memory address mapping uses Table 4-4. 10 : Row1 DRAM Memory address mapping uses Table 4-5. 11 : Row1 DRAM Memory address mapping uses Table 4-6. When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11) 00 : Row1 DRAM Memory address mapping uses Table 4-7. 01 : Row1 DRAM Memory address mapping uses Table 4-8. 10 : Row1 DRAM Memory address mapping uses Table 4-9. 11 : Row1 DRAM Memory address mapping uses Table 4-10. These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 1.
5-4 (0h)	Row1 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Registered Synchronous DRAM 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 1.

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3-0 (0h)	Row1 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide the top memory size for DRAM Row 1.

Register Index : **64h**

Register Name : **DB2CI - DRAM Row2 Configuration-1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	Row2 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **65h**

Register Name : **DB2CII - DRAM Row2 Configuration-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	DRAM MA Definition. When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01) 00 : Row2 DRAM Memory address mapping is Disable 01 : Row2 DRAM Memory address mapping uses Table 4-4 10 : Row2 DRAM Memory address mapping uses Table 4-5 11 : Row2 DRAM Memory address mapping uses Table 4-6 When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11) 00 : Row2 DRAM Memory address mapping uses Table 4-7 01 : Row2 DRAM Memory address mapping uses Table 4-8 10 : Row2 DRAM Memory address mapping uses Table 4-9 11 : Row2 DRAM Memory address mapping uses Table 4-10 These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 2.
5-4 (0h)	Row2 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Registered Synchronous DRAM 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 2.

3-0 (0h)	Row2 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide the top memory size for DRAM Row 2.

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Register Index : **66h**

Register Name : **DB3CI - DRAM Row3 Configuration-1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row3 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **67h**

Register Name : **DB3CII - DRAM Row3 Configuration-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	DRAM MA Definition. When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01) 00 : Row3 DRAM Memory address mapping is Disable 01 : Row3 DRAM Memory address mapping uses Table 4-4 10 : Row3 DRAM Memory address mapping uses Table 4-5 11 : Row3 DRAM Memory address mapping uses Table 4-6 When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11) 00 : Row3 DRAM Memory address mapping uses Table 4-7 01 : Row3 DRAM Memory address mapping uses Table 4-8 10 : Row3 DRAM Memory address mapping uses Table 4-9 11 : Row3 DRAM Memory address mapping uses Table 4-10 These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 3.
5-4 (0h)	Row3 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Registered Synchronous DRAM 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 3.
3-0 (0h)	Row3 DRAM Top Address Boundary-2. A31-A28 Address Boundary.

	These four bits are used to combine index-60h to decide the top memory size for DRAM Row 3.

Register Index : **68h**

Register Name : **DB4CI - DRAM Row4 Configuration-1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row4 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **69h**

Register Name : **DB4CII - DRAM Row4 Configuration-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	DRAM MA Definition. When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01) 00 : Row4 DRAM Memory address mapping is Disabled 01 : Row4 DRAM Memory address mapping uses Table 4-4 10 : Row4 DRAM Memory address mapping uses Table 4-5 11 : Row4 DRAM Memory address mapping uses Table 4-6 When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11) 00 : Row4 DRAM Memory address mapping uses Table 4-7 01 : Row4 DRAM Memory address mapping uses Table 4-8 10 : Row4 DRAM Memory address mapping uses Table 4-9 11 : Row4 DRAM Memory address mapping uses Table 4-10 These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 4.
5-4 (0h)	Row4 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Registered Synchronous DRAM 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 4.
3-0 (0h)	Row4 DRAM Top Address Boundary-2. A31-A28 Address Boundary.

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	These four bits are used to combine index-60h to decide the top memory size for DRAM Row 4.

Register Index : **6Ah**

Register Name : **DB5CI - DRAM Row5 Configuration-1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-0(00h)	Row5 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **6Bh**

Register Name : **DB5CII - DRAM Row0 Configuration-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-6 (00)	DRAM MA Definition. When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01) 00 : Row5 DRAM Memory address mapping is Disable 01 : Row5 DRAM Memory address mapping uses Table 4-4 10 : Row5 DRAM Memory address mapping uses Table 4-5 11 : Row5 DRAM Memory address mapping uses Table 4-6 When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11) 00 : Row5 DRAM Memory address mapping uses Table 4-7 01 : Row5 DRAM Memory address mapping uses Table 4-8 10 : Row5 DRAM Memory address mapping uses Table 4-9 11 : Row5 DRAM Memory address mapping uses Table 4-10 These two bits are used to program the Memory MA used on FPM or EDO DRAM/ Synchronous DRAM Row 5.

5-4 (0h)	Row5 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Registered Synchronous DRAM 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 5.
3-0 (0h)	Row5 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide the top memory size for DRAM Row 5.

Register Index : **6Ch**

Register Name : **DB6CI - DRAM Row6 Configuration-1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row6 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **6Dh**

Register Name : **DB6CII - DRAM Row6 Configuration-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	DRAM MA Definition. When set to Fast Page Mode DRAM or EDO DRAM (bit[5:4] = 00 or 01) 00 : Row6 DRAM Memory address mapping is Disable 01 : Row6 DRAM Memory address mapping uses Table 4-4 10 : Row6 DRAM Memory address mapping uses Table 4-5 11 : Row6 DRAM Memory address mapping uses Table 4-6 When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11) 00 : Row6 DRAM Memory address mapping uses Table 4-7 01 : Row6 DRAM Memory address mapping uses Table 4-8 10 : Row6 DRAM Memory address mapping uses Table 4-9 11 : Row6 DRAM Memory address mapping uses Table 4-10 These two bits are used to program the Memory MA used on FPM or EDO DRAM/ Synchronous DRAM Row 6.
5-4 (0h)	Row6 DRAM Type. 00 : Standard Fast-Page Mode DRAM 01 : EDO DRAM 10 : Registered Synchronous DRAM 11 : Synchronous DRAM These two bits are used to program the DRAM type used on DRAM Row 6.

3-0 (0h)	Row6 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide the top memory size for DRAM Row 6.

Register Index : **6Eh**

Register Name : **DB7CI - DRAM Row7 Configuration-1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-0 (00h)	Row7 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Index : **6Fh**

Register Name : **DB7CII - DRAM Row7 Configuration-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-6 (00)	DRAM MA Definition. When set to Fast Page mode DRAM or EDO DRAM (bit[5:4] = 00 or 01) 00 : Row7 DRAM Memory address mapping is Disable 01 : Row7 DRAM Memory address mapping uses Table 4-4 10 : Row7 DRAM Memory address mapping uses Table 4-5 11 : Row7 DRAM Memory address mapping uses Table 4-6 When set to Register SDRAM or SDRAM (bit[5:4] = 10 or 11) 00 : Row7 DRAM Memory address mapping uses Table 4-7 01 : Row7 DRAM Memory address mapping uses Table 4-8 10 : Row7 DRAM Memory address mapping uses Table 4-9 11 : Row7 DRAM Memory address mapping uses Table 4-10 These two bits are used to program the Memory MA used on FPM or EDO DRAM / Synchronous DRAM Row 7.

5-4 (0h)	Row7 DRAM Type. 00 : Standard Fast-Page Mode DRAM. 01 : EDO DRAM. 10 : Registered Synchronous DRAM 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 7.
3-0 (0h)	Row7 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide the top memory size for DRAM Row 7.

Register Index : **70h**

Register Name : **SDM256MB[7:0] - 256Mbit SDRAM select**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	ROW7 sets to 256Mbit SDRAM 0 : Disable 1 : Enable When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW7. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW7.
6 (0)	ROW6 sets to 256Mbit SDRAM 0 : Disable 1 : Enable When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW6. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW6.
5 (0)	ROW5 sets to 256Mbit SDRAM 0 : Disable 1 : Enable When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW5. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW5.
4 (0)	ROW4 sets to 256Mbit SDRAM 0 : Disable 1 : Enable When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW4. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW4.

3 (0)	ROW3 sets to 256Mbit SDRAM 0 : Disable 1 : Enable When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW3. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW3.
2 (0)	ROW2 sets to 256Mbit SDRAM 0 : Disable 1 : Enable When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW2. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW2.
1 (0)	ROW1 sets to 256Mbit SDRAM 0 : Disable 1 : Enable When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW1. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW1.
0 (0)	ROW0 sets to 256Mbit SDRAM 0 : Disable 1 : Enable When this bit is disabled, SDRAM memory technology 128Mbit, 64Mbit or 16Mbit is supported by ROW0. When this bit is enabled, SDRAM memory technology 256Mbit is supported by ROW0.

Register Index : **71h**

Register Name : **SDM4BANK[7:0] - SDRAM internal 2/4 Banks select**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	Number of SDRAM internal bank of ROW7 0 : 2 Banks, 1 : 4 Banks This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.
6 (0)	Number of SDRAM internal bank of ROW6 0 : 2 Banks, 1 : 4 Banks This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.
5 (0)	Number of SDRAM internal bank of ROW5 0 : 2 Banks, 1 : 4 Banks This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.
4 (0)	Number of SDRAM internal bank of ROW4 0 : 2 Banks, 1 : 4 Banks This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.
3 (0)	Number of SDRAM internal bank of ROW3 0 : 2 Banks, 1 : 4 Banks This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.
2 (0)	Number of SDRAM internal bank of ROW2 0 : 2 Banks, 1 : 4 Banks This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.
1 (0)	Number of SDRAM internal bank of ROW1 0 : 2 Banks, 1 : 4 Banks This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.
0 (0)	Number of SDRAM internal bank of ROW0 0 : 2 Banks, 1 : 4 Banks This bit decides whether the SDRAM internal organization is 2 banks or 4 banks.

Register Index : **72h**

Register Name : **SDRAM100 - SDRAM 100 MHz timing select.**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	Trcd (SDRAM SRASJ to SCASJ delay) select when bit6 = 1 enable 0 : Trcd = 3 CLKs 1 : Trcd = 2 CLKs When bit 6 = 1 enable separate setting for Trcd and CL, this bit will decide the Trcd. For M1541/M1542A1 E and later versions.
6 (0)	Enable the separate setting for Trcd (SDRAM SRASJ to SCASJ delay) and CL (SCASJ Latency) 0 : Disable 1 : Enable When this bit set to 1, Trcd will be decided by index 72h bit 7 and CL will be decided by index 48h bit 4. For M1541/M1542A1 E and later versions
5-3 (0h)	Reserved.
2 (0)	Internal command sent to SDRAM controller delay 1 CPU clock 0 : Enable. 1 : Disable. When this bit is set to enable, the command sent to SDRAM controller will add one CPU clock delay.
1 (0)	The SDRAM change row delays 1 CPU clock for 100 MHz. 0 : Disable. 1 : Enable. For 100MHz frequency, the consecutive different row read cycle performs X-1-1-1-2-1-1-1 when the second cycle is a page hit read.
0 (0)	SDRAM ensures 4 data duration intervals. 0 : Disable 1 : Enable This option will ensure four data duration between each DRAM cycle and prevent current cycle from being interrupted by the next DRAM command.

Register Index : **73h**

Register Name : **100 MHz Frequency timing Control**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits ---

Bit Number	Bit Function
7-5 (00h)	Reserved
4-3 (00)	Clock delay of DRAM Read Pipe Function 00 : 0 ns 01 : 1 ns 10 : 2 ns 11 : 3 ns When index 73h bit 2 (MD input pipeline function) is enabled, these two bits control the clock delay of the additional MD input pipeline stage. By this function, M1541 minimizes the MD setup time.
2 (0)	DRAM Read Pipe Function 0 : Disable 1 : Enable This configuration setting adds an additional pipeline stage for memory data input path. It is used for minimizing the MD required setup time when supporting 100MHz SDRAM bus.
1 (0)	SDRAM Command and Data Output Pipeline Function 0 : Disable 1 : Enable This configuration enables an additional pipeline stage for SDRAM control signal and write data. The additional pipeline stage clock source is ahead by PLL. With this additional pipeline stage, M1541 can maintain enough signal setup time for SDRAM when running at 100 MHz.
0 (0)	75-100 MHz frequency MD output pipe 0 : Disable 1 : Enable This option is used to add an additional internal output data pipeline stage.

Register Index : **83h-74h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

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Register Index : **85h-84h**

Register Name : **PCI Programmable Frame Buffer Memory Region**

Default Value : 00h

Attribute : Read/Write

Size : 16 bits

Bit Number	**Bit Function**
15-4 (000h)	Starting Address of Programmable Frame Buffer The 12 bits correspond to A[31:20] of the starting address. The remaining bits A[19:0] are assumed to be zero.
3-0 (0h)	Size of Programmable Frame Buffer 0000 : 1 MBytes. 0001 : 2 MBytes. 0010 : 4 MBytes. 0011 : 8 MBytes. 0100 : 16 MBytes. 1XXX : all CPU to PCI Memory Write cycle into buffer The Frame Buffer Region should not overlap with local memory.

Register Index : **86h**

Register Name : **CPU to PCI Write Buffer Option**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-4 (0h)	Reserved
3 (0)	LINEAR_WORD-Merge for Frame Buffer Cycle 0 : disable, 1 : enable When this bit is enable, only the words which address are consecutive linear can be merged into one line.
2 (0)	Use PCI Write-Burst for Frame Buffer cycle 0 : disable, 1 : enable If this bit is enable, consecutive PCI write cycle which the address is reside the frame buffer region will become burst cycle on the PCI bus.
1 (0)	VGA 0A0000-0BFFFF Fixed frame buffer 0 : disable, 1 : enable This bit is used to enable both the Frame buffer which address is fixed at 0A0000h-0B0000h and the Host to PCI_33 write buffer for Frame buffer cycle.
0 (0)	Programmable Frame buffer 0 : disable, 1 : enable This bit is used to combine with index 85h and 84h to enable the PCI Frame buffer and CPU to PCI_33 write buffer.

Register Index : **87h**

Register Name : **H2PO - CPU to PCI Option**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	PCI signal Distributed Output 0 : Disable, 1 : Enable If this bit is enable, the PCI interface output signals are stepping.

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6 (0)	APIC support, i.e. invalidate PCI to DRAM Read Ahead Buffer (P2HR) buffer when PHLDAJ goes low 0 : disable, 1 : enable When APIC is supported in Dual Processor system, this bit must be set to '1' to invalidate PCI to DRAM Read Ahead Buffer since the M1541 cannot realize Interrupt Synchronous event. But in Single Processor systems, the M1541 can detect Interrupt Synchronous event to invalidate PCI to DRAM Read Ahead Buffer automatically. This bit is recommended to be reset to '0' in Single Processor systems.
5 (0)	Translate CPU Shutdown cycle to Port 92 cycle 0 : enable, 1 : disable When this bit is set to ‘1’, the M1541 will forward a shutdown special cycle from CPU bus to PCI bus. When this bit is set to ‘0’, the M1541 will translate the shutdown cycle to I/O write cycle with I/O address 092h and write data is 01h.
4(0)	H2P CLKRUN Control Mode 0 : Normal mode, 1 : Safe Mode If this bit is set to ‘0’, the internal PCI clock is gated after the host to PCI cycle is complete. If this bit is set to ‘1’, the internal PCI clock is gated when the next cycle is not Host to PCI cycle.
3-2 (00)	H2PW Buffered Cycle Flush Waits Selection 00 : Wait 0 PCICLKs, 01 : Wait 2 PCICLKs 10 : Wait 3 PCICLKs, 11 : Wait 4 PCICLKs These 2 bits define the latency time from the time H2P write data get into H2PW buffer to the time assert flush request. This option will increase the possibility for merging the consequent H2PW cycle.
1 (0)	CPU Lock cycle when writing to FRAME buffer 0 : Ignore Lock, treat is as non lock cycle, 1 : normal When this configuration is set to ‘1’, CPU to PCI write cycle with HLOCKJ asserted will not be buffered. M1541 treats this kind of cycle as non-buffer cycle.
0 (0)	CPU-to-PCI Lock cycle. 0 : normal , 1 : Ignore lock If this bit is set to ‘0’, M1541 will transfer host lock cycle to PCI lock cycle. If this bit is set to ‘1’, M1541 will ignore the HLOCKJ and no PCI lock cycle will be generated.

4.4 PCI_33 PCI to Host interface

Register Index : **88h**

Register Name : **P2HO - PCI to Main Memory / PCI Arbiter Option**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	PCI master RETRY GAT mode 0 : disable 1 : enable When this bit is enable, if PCI master is retried during a read transaction, the master will be marked as a GAT master. When the same master retry the transaction at a later time, M1541 will flush the designed buffers before granting the bus ownership to it.
6 (0)	PCI Master Lock signal for PCI Arbiter 0 : enable 1 : disable When this bit is enable, the arbiter will not re-arbitrate the PCI bus during the locked transaction.
5 (0)	Flush H2PW buffer before grant to PCI 0 : Enable 1 : Disable When this bit is enable and index 88h bit0=1(IAS master GAT mode disable) or bit3=1 (Force PCI GAT mode disable), M1541 will flush internal CPU to PCI posted write buffer before granting the PCI_33 bus ownership to the master in GAT mode.
4 (0)	PCI Master LOCKJ signal for P2H cycle. 0 : Enable 1 : Disable When this bit is enable, the M1541 will recognize LOCKJ signaled by PCI master. Otherwise the M1541 will ignore the LOCKJ signal issued by PCI master.

3 (0)	Force PCI GAT Mode 0 : disable 1 : enable When this bit is enable, the M1541 will flush all necessary internal buffers before granting to the PCI master.
2 (0)	CPU access PCI during Passive Release 0 : disable 1 : enable This bit controls CPU to PCI access during Passive Release. When it is enabled, CPU to PCI access is allowed during Passive Release. Otherwise, arbiter only accepts another PCI master access to local DRAM.
1 (0)	Passive Release of PHOLD 0 : disable 1 : enable When this bit is enabled, the M1541 will recognize Passive Release signaled from M1533/M1543 by de-asserting PHOLDJ for a PCI Clock and then asserting PHOLDJ for a PCI Clock. The M1541 will de-assert the PHLDAJ signal and re-arbitrate PCI bus request and possibly allow the CPU to access PCI depending on the bit 2 setting. When this bit is disabled, the M1541 does not recognize Passive Release, i.e. , PHLDAJ will be continued to be asserted. A value '1' is recommended for normal operation.
0 (0)	ISA master GAT mode 0 : enable 1 : disable When this bit is enable, the M1541 will perform the similar operation as described in this index bit7 for the ISA master.

Register Index : **89h**

Register Name : **PCI Arbiter Time Slice**

Default Value : 20h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0 (20h)	Number of PCI clocks for PCI Bus time slice. The time-slice will guarantee the minimum clocks that the PCI master be granted the ownership of PCI bus. The time-slice counter is started when PCI grant is asserted and bus is idle. The bits 1-0 are assumed to be "00" and are ignored.

Register Index : **8Ah**

Register Name : **CPU Arbiter Time Slice**

Default Value : 20h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0 (20h)	Number of PCI clocks for CPU Bus time slice The time-slice will guarantee the minimum clocks that the CPU master be granted the ownership of PCI bus. The time-slice counter is started when PCI grant is asserted and bus is idle. Bits 1-0 are assumed to be "00" and are ignored.

Register Index : **8Bh**

Register Name : **PCIRC - PCI Retry Control for P2H Cycle**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	Reserved
5-4 (00)	Time Slice Scaling for CPU and PCI Master in "Passive Release" Period 00 : divide by 2 01 : divide by 4 10 : divide by 8 11 : divide by 1 These bits provide software configuration of resizing the number of time slice in index 89h and 8Ah.
3-2 (0)	Retry latency for Second Data Phase control 00 : Retry on first Data phase if wait state > 8 PCI clocks 01 : Retry on first Data phase if wait state > 4 PCI clocks 10 : Retry on first Data phase if wait state > 2 PCI clocks 11 : Never Retry on Second Data phase These bits are used to retry a PCI master cycle when the latency to the second data phase is about to exceed the programmed number of PCI clocks. When these bits are set to '11', the M1541 will complete the second data transfer regardless of latency.
1-0 (0)	Retry latency for First Data Phase control 00 : Retry on first Data phase if wait state > 32 PCI clocks 01 : Retry on first Data phase if wait state > 16 PCI clocks 10 : Retry on first Data phase if wait state > 8 PCI clocks 11 : Never Retry on Second Data phase These bits are used to retry a PCI master cycle when the latency to the first data phase is about to exceed the programmed number of PCI clocks. When these bits are set to '11', the M1541 will complete the first data transfer regardless of latency.

Register Index : **8Ch**

Register Name : **PCI to Main Memory Option**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7(0)	Enable PCI master0 as Non_Preempt master (for P2P) 0 : disable, 1 : enable, when this bit is enable, PCI master0 will be treated as a non_preempt master. During its access, the PCI bus ownership will not be re-arbitrated.
6(0)	PCI Master Access M1541 Configuration Register. This bit decides whether the PCI master can access the configuration register or not. 0 : disable, only CPU can access M1541 configuration register. 1 : enable
5(0)	P2HW burst support. This bit provides the capability of supporting the PCI master burst write transaction. 0 : enable, 1 : disable
4(0)	P2HR burst support. This bit provides the capability of supporting the PCI master burst read transaction. 0 : enable, 1 : disable
3(0)	PCI master Read pre-fetch. This bit controls the M1541's ability to pre-fetch data for PCI master read transaction. 0 : enable, 1 : disable
2-0 (000)	P2H Read buffer Pre-fetch Threshold. These bits control the M1541's pre-fetch behavior in the case of PCI master read and pre-fetch is enable. 000 : 1 buffer 001 : 2 buffers 010 : 3 buffers 011 : 4 buffers 100 : 5 buffers 101 : 6 buffers 110 : 7 buffers 111 : 8 buffers

Register Index : **8Dh**

Register Name : **PCI Clock Control**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-5 (0h)	P2HW Slice Control Timer. These bits control the time slice for PCI-to-DRAM write in the M1541 internal write bus. 0000 : 0 CLK 0001 : 1 CLK 0010 : 2 CLKs 0011 : 3 CLKs : 1111 : 15 CLKs
4 (0)	Miss Read Pending Delay Timeout Retry 0 : enable, 1 : disable When enabled, PCI master read will not be retried until the M1541 issues a read transaction to memory even if the PCI master's time slice has expired.
3 (0)	Internal Write Bus Pipeline Function. 0 : Disable, 1 : Enable, this bit enables the M1541 internal write bus pipeline function.
2-0 (000)	PCI Frequency Mode 110 : 2X 101 : 2.5X 011 : 3X others : Reserved These bits reflect the relationship between CPU external frequency and PCI bus frequency. In order to keep the PCI frequency at 33 MHz, different CPU external frequencies should be set to different modes.

CPU External Frequency	PCI Frequency Mode	PCI Frequency
50/60/66 MHz	110 : 2X	25/30/33 MHz
75/83 MHz	101 : 2.5X	30/33 MHz
100 MHz	011 : 3X	33 MHz

Register Index : **08Eh**

Register Name : **Internal Arbiter Write Control**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit	**Description**
7-4 (0h)	AGPW Slice Control Timer. These bits control the time slice for AGP to DRAM write in the M1541 internal write bus 0000 : 0 CLK 0001 : 1 CLK 0010 : 2 CLKs : : 1111 : 15 CLKs
3-0 (0h)	G2HW Slice Control Timer. These bits control the time slice for PCI_66 to DRAM write in the M1541 internal write bus 0000 : 0 CLK 0001 : 1 CLK 0010 : 2 CLKs : : 1111 : 15 CLKs

Register Index : **08Fh**

Register Name : **Internal Arbiter P2H Read Control**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit	**Description**
7-4 (0h)	G2HR Slice Control Timer. These bits control the time slice for PCI_66 to Host Read in the M1541 internal read bus 0000 : 0 CLK 0001 : 1 CLK 0010 : 2 CLKs : : 1111 : 15 CLKs
3-0 (0h)	P2HR Slice Control Timer. These bits control the time slice for PCI_33 to Host read in the M1541 internal read bus 0000 : 0 CLK 0001 : 1 CLK 0010 : 2 CLKs : : 1111 : 15 CLKs

Register Index : **90h**

Register Name : **LRWCTL - Lock Read/Write Control**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	Interrupt line register read/write control 0 : disable, 1 : enable When this bit is enable, M1541 interrupt line register located at index 3Ch is unlock and can be read and written. When this bit is disable, M1541 interrupt line register located at index 3Ch is read only.
6 (0)	AGP register Locked read/write control 0 : disable (Read only), 1 : enable (Read/Write) When this bit is enable, M1541 AGP register located at index 0b7h to 0b0h all are unlock and can be read and written. When this bit is disable, M1541 AGP register located at index 0b7h to 0b0h are read only.
5 (0)	Power Management Locked read/write control 0 : disable (Read only), 1 : enable (Read/Write) When this bit is enable, M1541 Power management register located at index 0e7h to 0e0h all are unlock and can be read and written. When this bit is disable, M1541 Power management register located at index 0e7h to 0e0h are read only.
4 (0)	PLL control register Locked read/write control 0 : disable (Read only), 1 : enable (Read/Write) When this bit is enable, M1541 PLL control register located at index 0EDh are unlock and can be read and written. When this bit is disable, M1541 PLL control register located at index 0EDh are read only.
3 (0)	M5243 PCI to PCI bridge Device Identification Register Locked read/write control 0 : disable (Read only), 1 : enable (Read/Write) When this bit is enable, M5243 DID register located at M5243 index 03h to 02h all are unlock and can be read and written. When this bit is disable, M5243 DID register located at M5243 index 03h to 02h are read only.

2 (0)	M1541 Power management Base address of ACPI PM2_CNT port register Locked read/write control 0 : disable (Read only) 1 : enable (Read/Write) When this bit is enable, M1541 Base address of ACPI PM2_CNT port register located at index 0e9h to 0e8h all are unlock and can be read and written. When this bit is disable, M1541 Base address of ACPI PM2_CNT port register located at index 0e9h to 0e8h are read only.
1 (0)	M1541 Device 0 Capabilities Pointer register Locked read/write control 0 : disable (Read only) 1 : enable (Read/Write) When this bit is enable, M1541 Device 0 Capabilities Pointer register located at index 34h is unlock and can be read and written. When this bit is disable, M1541 Device 0 Capabilities Pointer register located at index 34h is read only.
0 (0)	M1541 sub-vender identification register Locked read/write control 0 : disable (Read only) 1 : enable (Read/Write) When this bit is enable, M1541 sub-vender identification register located at index 2dh to 2ch are unlock and can be read and written. When this bit is disable, M1541 sub-vender identification register index 2dh to 2ch is read only.

Register Index : **91h**

Register Name : **BRSYCTL - Broadcast and Synchronous cycle Control**

Default Value : 13h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-2	Reserved
0 (1)	INTA, Special cycle broadcast to both PCI_66 and PCI_33 bus 0 : disable 1 : enable This bit enables M1541 broadcast the interrupt acknowledge and special cycle to both PCI and AGP bus.

Register Index : **0AFh-92h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

4.5 AGP Interface Registers

Register Index : **0B3h-0B0h**

Register Name : **A.G.P. Capability Identifier Registers**

Default Value : 0010E002h

Attribute : Read Only

Size : 32 bits

Bit Number	Bit Function
31-24 (00h)	Reserved
23-20 (1h)	Major A.G.P. Revision Number (Hardwired to "0001")
19-16 (0h)	Minor A.G.P. Revision Number (Hardwired to "0000")
15-8 (0E0h)	Next Capability Pointer (Hardwired to "11100000"=0e0h) Point to PCI bus Power Management Control
7-0 (02h)	A.G.P. Capability ID (Defaults to "00000010"=02h)

Register Index : **0B7h-0B4h**

Register Name : **A.G.P. Status Registers**

Default Value : 1C000203h

Attribute : Locked Read/write

Default is read only. When index-90h bit 0 is 1, these bits can read/write.

Size : 32 bits

Bit Number	Bit Function
31-24 (1Ch)	A.G.P. Request Queue Depth (Locked Read/Write, Default=1Ch) These bits show the depth of the AGP request queue depth.
23-10 (0000h)	Reserved, Hardwired to '0' (Read only)
9 (1)	SBA (Side Band Address) function (Locked Read/write) 0 : not supported, 1 : support
8-2 (00h)	Reserved
1 (1)	A.G.P. Data Transfer Type Supported (Locked Read/Write) - 2X clocking mode 0 : not supported, 1 : supported
0 (1)	A.G.P. Data Transfer Type Supported (Locked Read/Write) - 1X clocking mode 0 : not supported, 1 : supported

Register Index : **0BBh-0BA,0B8h**

Register Name : **A.G.P. Command Registers**

Default Value : 0000000h

Attribute : Read/Write

Size : 32 bits

Bit Number	**Bit Function**
31-24 (00h)	RQ_DEPTH A.G.P. Request Queue Depth
23-10 (0000h)	Reserved, Hardwired to '00000' (Read only)
9 (0)	SBA_ENABLE (Read/write) 0 : disable 1 : enable This bit can enable or disable the SBA function.
8 (0)	AGP_ENABLE (Read/Write) 0 : disable 1 : enable This bit can enable or disable the AGP function.
7-2 (00h)	Reserved.
1 (0)	A.G.P. Data Transfer Type Supported - 2X clocking mode 0 : disable 1 : enable This bit can enable or disable the 2X function.
0 (0)	A.G.P. Data Transfer Type Supported - 1X clocking mode 0 : disable 1 : enable This bit can enable or disable the 1X function.

Register Index : **0B9h**

Register Name : **A.G.P. Enable Registers**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit No.	Description
7-1 (00)	Reserved
0 (0)	AGP_Enable (Read/Write) 0 : Disable 1 : Enable This bit can enable /disable the AGP function.

Register Index : **0BFh-0BCh**

Register Name : **Aperture Control Register**

Default Value : 00000000h

Attribute : Read/write

Size : 32 bits

Bit Number	Bit Function
31-12 (00000h)	Graphics Aperture Remapping Table Base address The address is from A[31] to A[12]. It is based on 4K bytes boundary.
11-4 (00h)	Reserved.
3-0 (0h)	Graphics Aperture Size(Defaults to "0000") GA_SIZE 0000 0MB x10 D[31:0] => '0' 0001 1MB x10 D[31:20] R/W, D[19:0] => '0' 0010 2MB x10 D[31:21] R/W, D[20:0] => '0' 0011 4MB x10 D[31:22] R/W, D[21:0] => '0' 0100 8MB x10 D[31:23] R/W, D[22:0] => '0' 0110 16MB x10 D[31:24] R/W, D[23:0] => '0' 0111 32MB x10 D[31:25] R/W, D[24:0] => '0' 1000 64MB x10 D[31:26] R/W, D[25:0] => '0' 1001 128MB x10 D[31:27] R/W, D[26:0] => '0' 1010 256MB x10 D[31:28] R/W, D[27:0] => '0'

Register Index : **0C3h-0C0h**

Register Name : **GTLB Control Register**

Default Value : 00000000h

Attribute : Read/Write

Size : 32 bits

Bit Number	**Bit Function**
31-20 (000h)	NLVM_TOP[31-20] These bits set the top address of the NLVM (Non-Local Video Memory) region bit : 31 30 ….. 21 20 NVLM_TOP Address : 31 30 ….. 21 20 The address is from A[31] to A[20]. NLVM_TOP[31-20] must be greater than NLVM_BASE[31-20] for meaningful memory region definition.
19-8 (000h)	NLVM_BASE[31-20] These bits set the bottom address of the NLVM region bit : 19 18 ….. 9 8 NVLM_BASE Address : 31 30 ….. 21 20 The address is from A[31] to A[20]. NLVM_BASE[31-20] must be less than NLVM_TOP[31-20] for meaningful memory region definition.
7(1)	GART Table enable control 0 : Enable, 1 : Disable This bit controls the enable/disable of the GART maintenance.
4(1)	GART Table size 0 : 32 entries, 4-sector associate 1 : 64 entries, 8-sector associate This bit controls the GART size. There are 2 options : (1) 32 entries and 4-sector associate (2) 64 entries and 8-sector associate Set this bit to '1' is recommended to get the most hit rate.
6-5,3-0 (0)	Reserved.

Register Index : **0DFh-0D4h, 0CFh-0CAh,0C7h-0C4h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Register Index : **0C8h**

Register Name : **AGP Control Register I**

Default Value : BFh

Attribute : Read/Write

Size : 8 bits

Bit no.	Description
7(1)	Buffer Depth selection for AGP read data buffer 0 : 16 QW, 1 : 32 QW This bit selects the AGP read data buffer depth. Choosing 32 QW is recommended.
6-4(011)	The available space of AGP read data buffer for asserting an AGP request to memory 000 : 0 QW available 001 : 4 QW available 010 : 8 QW available 011 : 12 QW available 100 : 16 QW available 101 : 20 QW available 110 : 24 QW available 111 : 28 QW available These bits decide when to assert the AGP request to DRAM. If the buffer available space is greater than the setting, AGP request will issue to DRAM. For example, if setting these bits to ‘011’, the buffer will begin to issue AGP request to DRAM when the buffer empty space is more than 12 Qwords.
3(0)	Enable to lower the LPR/HPR dequeue priority when AGP read data buffer is full. 0 : disable, 1 : enable
2(0)	Enable to upgrade the LPR/HPR dequeue priority when AGP write data buffer is full. 0 :disable, 1 : enable
1-0(11)	Queue depth selection of AGP request queue 00 : 8, 01 : 16 10 : 24, 11 : 32

	These two bits select the AGP request queue depth. Set to 32-queue depths is recommended.

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Register Index : **0C9h**

Register Name : **AGP Control Register II**

Default Value : 0Ah

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	Output delay control of AD_STB[1:0] 00 : Default (The default value is 3.5ns) 01 : Default - 1 ns 10 : Default +1 ns 11 : AD_STB[1:0] output is generated by 133 MHz clock (Double of the AGP clock : GCLKIN). These two bits select the output delay of AD_STB[1:0]. The default delay is 3.5 ns.
5 (0)	Flush Host to PCI-66 write command if it was asserted before a FLUSH command 0 : Enable 1 : Disable If set to ENABLE, the Host to PCI_66 write buffer will be flushed before a FLUSH command
4 (0)	Delay enqueue LWT command when Fence is occurring until the command before fence is dequeue 0 : Enable 1 : Disable IF set to ENABLE, system will delay the LWT command enqueue until those commands before fence are dequeued.
3 (1)	Fast assertion of read request 0 : Disable 1 : Enable If set to ENABLE, system will issue the read request immediately.
2-0 (010)	The threshold QW number for AGP read data buffer to assert an AGP read request on AGP BUS 000 : 0 QW available 001 : 4 QW available 010 : 8 QW available 011 : 12 QW available

	100 : 16 QW available 101 : 20 QW available 110 : 24 QW available 111 : 28 QW available The threshold length is 4QW when 2x transfer is selected, else 2QW when 1x transfer is selected

Register Index : **0D3-0D0h**

Register Name : **L1/L2 Cache Flush Control**

Default Value : 00h

Attribute : Read/Write

Size : 32 bits

Bit Number	**Bit Function**
31-12 (00000h)	Cache flush page address [31-12]. These bits control the cache flush page register. Bits 31-12 correspond to address 31-12.
11-9 (0h)	Reserved.
8 (0)	Cache flush enable – L1/L2_FLUSH 0 : Disable Flush or Finish Flush 1 : Enable Flush When this bit is enable. The L1/L2 cache region indicated by Cache Flush page register (index 0D3h-0D0h bit 31-12) will be flushed to DRAM by hardware directly. When the hardware finishes the flush process, this bit will be cleared to 0.
7-0 (00h)	Reserved

4.6 Green Function Register

Register Index : **0E0h**

Register Name : **Power Management Capability Identifier Register**

Default Value : 01h

Attribute : Locked Read/Write

Bit Number	Bit Function
7-0 (01h)	Capability Identifier. The capability identifier, when read by system software as 01h indicates that the data structure currently being pointed to is the PCI Power management data structure. The register's default is read only, when index 90h bit 5 = 1 , this register can read/write.

Register Index : **0E1h**

Register Name : **Power Management Next Item Pointer Register**

Default Value : 00h

Attribute : Locked Read/Write

Bit Number	Bit Function
7-0 (00h)	Next Item Pointer This field provides an offset into the PCI function's PCI configuration space pointing to the location of next item in the function's capability list. If there are no additional items in the capability list, this register is set to 00h. The register default is read only. When index 90h bit 5 = 1, this register can read/write.

Register Index : **0E3h-0E2h**

Register Name : **Power Management Capabilities Register**

Default Value : 0000h

Attribute : Locked Read/write. The register default is read only, when index 90h bit 5 = 1, this register can read/write.

Bit Number	Bit Function

15-11 (00000)	PME_Support XXXX1 : PMEJ can be asserted from D0 XXX1X : PMEJ can be asserted from D1 XX1XX : PMEJ can be asserted from D2 X1XXX : PMEJ can be asserted from D3 hot 1XXXX : PMEJ can be asserted from D3 cold These five bits field indicate the power state in which the function may assert PMEJ. A value of '0' for any bit indicates that the function is not capable of asserting the PMEJ signal while in that power state.
10 (0)	D2_Support 0 : Do not support D2 1 : Support D2 If this bit is set to '1', M1541 supports the D2 power management state.
9 (0)	D1_Support 0 : Do not support D1 1 : Support D1 If this bit is set to '1', M1541 supports the D1 power management state.
8-6 (000)	Reserved
5 (0)	Device Specific Initialization (DSI) If this bit is set to '1', it indicates the function requires a device specific initialization sequence following transaction to the D0 un-initialized state.
4 (0)	Auxiliary Power Source This bit is only meaningful if the bit 15 (PMEJ can be asserted from D3 cold) = 1 0 : Supply its own auxiliary power source 1 : Support PMEJ in D3 cold requires auxiliary power supplied by the system by way of proprietary delivery vehicle.
3 (0)	PME clock 0 : No PCI clock is required for M1541 to generate PMEJ. 1 : M1541 relies on the presence of the PCI clock for PMEJ operation.
2-0 (001)	Version of PCI power management interface specification The version support is V1.0 now.

Register Index : **0E5h-0E4h**

Register Name : **Power Management Control and Status Register**

Default Value : 0000h

Attribute : Locked Read/write. Some bits can read/write, some bits are Locked read/write. These bits marked with Locked read/write default is read only, when index 90h bit 5 = 1, these bits can read/write.

Bit Number	Bit Function
15 (0)	PME_Status (Read/Write_clear). This bit is set when the function would normally assert the PMEJ signal independent of the state of the PME_EN (index 0E4h bit 8) 0 : The function does not support PMEJ generation from D3 cold state. 1 : Indeterminate at time of initial OS boot if function supports PMEJ from D3 cold state. Write 1 to this bit will clear this bit to 0 and cause the M1541 to stop asserting a PMEJ (if enabled). Writing a “0” has no effect..
14-13 (00)	Data_scale (Locked read/write) These two-bit field indicates the scaling factor to be used when interpreting the value of the DATA register(index 0e7h). The value & meaning of this field will vary depending on which data value has been selected bit[12-9] (DATA_select) field.
12-9 (0h)	Data_select (read/write) These four bits are used to select which data is to be reported through DATA register (index 0E7h) and data scale (bit[14-13]) field.
8 (0)	PME_EN (read/write) 0 : PMEJ assertion is disable 1 : Enable the function to assert PMEJ
7-2 (00h)	Reserved (Locked read/write)
1-0 (00)	Power State (read/write) 00 : D0 01 : D1 10 : D2 11 : D3 hot These two bits are used to determine the current power state of a function and to set the function into a new power state. If software attempts to write an unsupported, optional state to this field. The write operation must complete normal on the bus, however the data is discarded and no state change occurs.

Register Index : **0E6h**

Register Name : **PMCSR PCI-to-PCI Bridge Support Extensions**

Default Value : 00h

Attribute : Locked Read/write. The register default is read only, when index 90h bit 5 = 1 , this register can read/write.

Bit Number	**Bit Function**
7 (0)	Bus Power/Clock Control Enable 0 : Bus power/clock control mechanism has been disabled 1 : Bus power/clock control mechanism has been enabled When the Bus Power/Clock control mechanism is disabled, the bridge's PMCSR Power State field cannot be used by the system software to control the power or clock of the bridge's secondary bus.
6 (0)	B2/B3 support for D3 hot 0 : The bridge function is programmed to D3 hot, its secondary bus' will have its power removed (B3) 1 : The bridge function is programmed to D3 hot, its secondary bus' PCI clock will be stopped (B2) The state of this bit determines the action that is to occur as a direct result of programming the function to D3 hot. This bit is only meaningful if bit 7=1 (Bus Power/Clock control enable)
5-0 (00h)	Reserved

Register Index : **0E7h**

Register Name : **Data Register**

Default Value : 00h

Attribute : Locked Read/Write. The register default is read only, when index 90h bit 5 = 1 , this register can read/write.

Bit Number	**Bit Function**
7-0 (00h)	Data[7-0]. This register is used to report the state dependent data requested by the Data_Select (index 0E4h bit[12-9]) field. The value of this register is scaled by the value reported by the Data_Scale (index 0E4h bit[12-9]) field.

Register Index : **0E9h-0E8h**

Register Name : **BASE ADDRESS OF ACPI PM2_CNTL PORT**

Locked read/write, control bit is index 90h bit 2. If index 90h bit2 = '1' then enable write this register.

Default Value : 0000h

Attribute : Locked Read/Write

Size : 16 bits

Bit Number	**Bit Function**
15-0 (0000h)	Base Address of ACPI PM2_CNTL Port. This 16-bit register is programmed as the I/O base address of ACPI PM2_CNTL Port. The default value is 0000h, and can be programmed by software to move the base address of ACPI PM2_CNTL Port.

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Register Index : **0EAh**

Register Name : **PM2C - ACPI PM2_CNTL function**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-6 (00)	5-V Suspend Refresh period 00 : 15 us 01 : 30 us 10 : 60 us 11 : 120 us These 2 bits define the DRAM suspend refresh period when M1541 enters the suspend mode.
5-4 (00)	Reserved
3 (0)	CLKRUNJ/SERRJ Function Select 0 : SERRJ 1 : CLKRUNJ This bit is used to define the CLKRUNJ/SERRJ pin function. When this bit is programmed to '0', SERRJ function is selected. In this configuration, M1541 can support DRAM ECC/PARITY and the PCI Parity check error report. When this bit is programmed to '1', CLKRUNJ function is selected. M1541 can support Mobile PCI Specification 2.0 CLKRUNJ function through this configuration.
2 (0)	Host to PCI IO Cycle Trap Support 0 : normal 1 : Delay BRDYJ for 1 CPU CLK M1541 will delay all the PCI IO cycle by one CPU clock when this bit is set to ‘1’. The BRDYJ to CPU will delay one CPU clock compared to normal IO access. This is to make sure CPU can IO trap this IO instruction. So after SMM mode, an IO restart can function correctly.

1-0 (00)	ACPI PM2_CNTL FUNCTION 00 : Disable 01 : Enable, monitor the IO port access defined by index 0E9h~0E8h 10 : Enable, receive the IO port access defined by index 0E9h-0E8h and NOT transfer access to PCI bus 11 : Reserved These two bits define the way that M1541 responses to the ACPI PM2_CNTL port write. M1541 has implemented the ACPI PM2_CNTL I/O Port, and the address is defined by Index 71h-70h. When these two bits are programmed to be '00', M1541 will disable the ACPI PM2_CNTL I/O Port decode, and pass the I/O cycle to PCI bus. When these two bits are programmed to be '01', M1541 will snoop the ACPI PM2_CNTL I/O Port write data, and pass the I/O cycle to PCI bus. In this setting, M1541 just do the snoop write, and all the cycle will be terminated by M1533/M1543. When these two bits are programmed to be '10', M1541 will terminate the ACPI PM2_CNTL I/O Port access, and will not pass the I/O cycle to PCI bus.

Register Index : **0EBh**

Register Name : **GCKCTL - Gated Clock Control Register**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Description
7 (0)	Host interface Clock Control 0 : Disable Gated Clock 1 : Enable Gated Clock This bit is used to control the Host CPU interface clock. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal clock when there is no Host activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.
6 (0)	DRAM Sequencing, DRAM Controller clock turn off in MD idle cycle 0 : disable 1 : enable This bit is used to control the internal clock regarding the Memory Data Bus. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal DRAM controller clock when there is no Memory Data Bus activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.
5 (0)	DMWBF/L2 Controller clock turn off in CPU idle cycle 0 : disable 1 : enable This bit is used to control the internal DRAM controller clock regarding the DRAM & Cache Controller. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal DRAM posted write buffer controller and L2 cache controller clock when there is no Host Bus activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.
4 (0)	AGP to Host Buffer clock control 0 : Disable Gated Clock 1 : Enable Gated Clock This bit is used to control the internal clock regarding the AGP to Host Buffer. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal clock when there is no AGP master activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.
3 (0)	Host to PCI_66 Buffer clock control 0 : Disable Gated Clock

	1 : Enable Gated Clock This bit is used to control the internal clock regarding the Host to PCI_66 Interface Logic. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal clock when there is no Host to PCI_66 activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.
2 (0)	PCI_66 to Host Buffer clock control 0 : Disable Gated Clock 1 : Enable Gated Clock This bit is used to control the internal clock regarding the PCI_66 to Host Buffer. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal clock when there is no PCI_66 master activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.
1 (0)	Host to PCI interface logic clock control 0 : Disable Gated Clock 1 : Enable Gated Clock This bit is used to control the internal clock regarding the Host to PCI Interface Logic. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal clock when there is no Host to PCI activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.
0 (0)	PCI to Host Buffer Clock Control 0 : Disable Gated Clock 1 : Enable Gated Clock This bit is used to control the internal clock regarding the PCI to Host Buffer. When this bit is programmed to be '0', the clock never stops. When this bit is programmed to be '1', M1541 will automatically stop the internal clock when there is no PCI master activity. This bit is suggested to be set to '0' in desktop application; to be '1' in notebook application to save more power.

Register Index : **0ECh**

Register Name : **POD - Programmable Output Driving Strength**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	Reserved
5 (0)	MAA[1:0] Driving Capability Select. 0 : 32 mA 1 : 16 mA This bit controls the strength of the output buffers driving the MAA[1:0] pins.
4 (0)	MA[14:2] Driving Capability Select. 0 : 32 mA 1 : 16 mA This bit controls the strength of the output buffers driving the MA[11:2] pins.
3 (0)	CASJ[7:0] Driving Capability Select. 0 : 24 mA 1 : 12 mA This bit controls the strength of the output buffers driving the CASJ[7:0] pins.
2 (0)	RASJ[7:0] Driving Capability Select. 0 : 24 mA 1 : 12 mA This bit controls the strength of the output buffers driving the RASJ[7:0]
1 (0)	MD[63:0],MPD[7:0] Driving Capability Select. 0 : 16 mA 1 : 10 mA This bit controls the strength of the output buffers driving the MD[63:0], MPD[7:0] pins.
0 (0)	HD[63:0] Driving Capability Select. 0 : 16 mA 1 : 12 mA This bit controls the strength of the output buffers driving the HD[63:0] pins.

Register Index : **0EDh**

Register Name : **Hardware setting register**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-5 (000)	HOST bus frequency (read only) 000 : Reserved 001 : 60MHz 010 : 66MHz 011 : 75MHz 100 : 83MHz 101 : 90MHz 110 : 100 MHz 111 : Reserved (HA[31:29] as hardware setting pin). These three bits are hardware strobe from HA[31:29] to indicate the CPU bus frequency for BIOS POST procedure reference.
4 (0)	CPU clock PLL enable 0 : disable 1 : enable (HA[28] as hardware setting pin). This bit is hardware strobe from HA[28] to enable the CPU PLL circuit for 100MHz clock compensation. Locked read/write, controlled by index 90h bit 4.
3-1 (000) For M1541 A1 C and earlier version	CPU CLK compensate select 000 : No compensate 001 : 1 buffer 010 : 2 buffers 011 : 3 buffers 100 : 4 buffers 101 : 5 buffers 110 : 6 buffers 111 : 7 buffers (HA[27-25] as hardware setting pin) These three bits are hardware strobe from HA[27-25] to enable the CPU PLL compensate circuit for 100MHz clock compensation. Locked read/write, controlled by index 90h bit 4

0 (0) For M1541 A1 C and earlier version	CPU CLK PLL internal test select 0 : Normal 1 : Test (HA[24] as hardware setting pin)
3-2 (00) For M1541 A1 D and later version	CPU CLK compensate select 00 : No compensate 01 : 2 buffer 10 : 4 buffers 11 : 6 buffers (HA[27-26] as hardware setting pin). These three bits are hardware strobe from HA[27-26] to enable the CPU PLL compensate circuit for 100MHz clock compensation. Locked read/write, controlled by index 90h bit 4.
1-0 (00) For M1541 A1 D and later version	HD output clock select 00 : default 01 : ahead 1 ns 10 : ahead 2 ns 11 : ahead 3 ns These two bits control the CPU interface HD data bus output synchronization clock (HA[25-24] as hardware setting pin).

Register Index : **0EEh**

Register Name : **Miscellaneous-1**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	Reserved.
5-4 (00) For M1541 A1 C and earlier versions	MESI clock select 00 : HCLK_IN, Host clock input 01 : ADV_CLK, Advance clock 10 : Ahead 2 ns 11 : Ahead 3 ns These two bits select which clock source for internal TAG/MESI SRAM usage.
5-4 (00) For M1541 A1 D and later versions	MESI clock select 00 : HCLK_IN, Host clock input 01 : Ahead 1 ns 10 : Ahead 2 ns 11 : Ahead 3 ns These two bits select which clock source for internal TAG/MESI SRAM usage.
3-2 (00)	SDRAM memory write Data Ahead clock select 00 : Ahead 4 ns 01 : Ahead 1 ns 10 : Ahead 2 ns 11 : Ahead 3 ns When index 0EEh bit1 (100Mhz SDRAM memory write Data ahead clock select use internal ahead clock) =0, these two bits define how much the advanced clock for DMW circuit leads the M1541 internal host clock.
1 (0) For M1541 A1 C and earlier version	100Mhz SDRAM memory write Data ahead clock select 0 : External clock 1 : Internal Ahead clock This bit is used for selecting the DRAM memory write circuit clock. When this bit is set to'0', the DRAM memory write circuit will use the clock which is input from DPLLI0 instead of the internal PLL. The data and control signal sent to DRAM will use DPLLI1

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	as clock source. For C and earlier versions, this bit should set to '1'
1 (0) For M1541 A1 D and later version	100Mhz SDRAM memory write Data ahead clock select 0 : ahead clock 1 : clock test mode This bit is used for selecting the DRAM memory write circuit clock. When this bit is set to '0', the DRAM memory write circuit will use the ahead clock. The data and control signal sent to DRAM will use ahead clock as clock source. When set to 1, the circuit will be in clock test mode for chip testing only For D and later versions, this bit should set to '0'
0 (0)	Reserved

Register Index : **0EFh**

Register Name : **Miscellaneous-2**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

When SDRAM PLL is set to Digital PLL, this index should be set to 0A3h (recommended)

When SDRAM PLL is set to Analog PLL, this index should be set to 0A0h

When SDRAM PLL is set to disable, this index should be set to 00h

Bit Number	Bit Function
7-6 (00)	SDRAM Memory Read PLL reference clock select 00 : HCLK from output of Host PLL 01 : HCLK from output of Host PLL + 1 buffer 10 : Reference HCLK 11 : Reference HCLK + 1 buffer These two bits select the reference clock source of PLL for SDRAM.
5 (0)	SDRAM Memory Read PLL enable 0 : Disable 1 : Enable If this bit is enable, the SDRAM controller will use internal Digital or Analog PLL for the automatic adjustment mechanism. The Digital or Analog PLL will be decided by bit 0.
4-2 (000)	DRAM Memory Read PLL compensate 000 : 0 buffer, no compensation 001 : 1 buffer 010 : 2 buffers 011 : 3 buffers 100 : 4 buffers 101 : 5 buffers 110 : 6 buffers 111 : 7 buffers These three bits control the compensation of SDRAM clock source of PLL.
1 (0)	SDRAM DPLL Auto enable 0 : Disable 1 : Auto If this bit is enable, the SDRAM controller will use internal Digital PLL for the automatic adjustment

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	mechanism.
0 (0)	SDRAM Analog PLL/DPLL select 0 : Select Analog PLL 1 : Select Digital PLL This bit is used to select the SDRAM controller clock source.

Register Index : **0F3h**

Register Name : **Predict the next SDM Control Signal**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
3 (0)	Predict the next SDRAM control signal 0 : disable 1 : enable

Register Index : **0F5h**

Register Name : **DMRDPL Status Register**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	SDRAM DPLL Status (Read Only) 0 : Feedback clock lag reference clock. 1 : Feedback clock ahead reference clock. This bit indicates the status of Digital PLL for M1541 SDRAM clock source.
6-0 (00h)	SDRAM DPLL counter (Read/Write) These bits indicate the status of Digital PLL for M1541 SDRAM clock source. Writing to these bits will control the DPLL delay stage and thus control the output clock phase. Reading data from these bits indicate current delay stage.

Register Index : **0F6h**

Register Name : **GDPL Status register**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	AGP DPLL status (Read only) 0 : Feedback clock lag reference clock. 1 : Feedback clock ahead reference clock. This bit indicates the status of Digital PLL for M1541 internal AGP source.
6-0 (00h)	AGP DPLL counter (Read/Write) These bits indicate the status of Digital PLL for M1541 internal AGP clock source. Writing to these bits will control the DPLL delay stage and thus control the output clock phase. Reading data from these bits indicate current delay stage.

Register Index : **0F7h**

Register Name : **GCLK PLL Control Register**

Default Value : 00h

Attribute : Read/write

Size : 8 bits

When AGP PLL is set to Digital PLL, this index should be set to 043h (recommended)

When AGP PLL is set to Analog PLL, this index should be set to 01h

When AGP PLL is set to disable, this index should be set to 00h

Bit Number	Bit Function
7 (0)	Reserved
6 (0)	GCLK DPLL auto enable 0 : disable 1 : auto enable When this bit is set to '1', the Digital PLL for AGP clock will adjust automatically.
5-2 (00)	Reserved
1 (0)	GCLK PLL/DPLL select 0 : Analog PLL 1 : Digital PLL This bit selects the Digital or Analog version of PLL for M1541 internal AGP clock.

0 (0)	GCLK clock select 0 : External clock 1 : PLL clock If this bit is set to ‘1’, the M1541 internal AGP clock source will be the internal PLL. Otherwise, the clock source will be the external clock input clock GCLKIN.

Register Index : **0FFh-0F8h, 0F4h, 0F2h-0F0h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

4.7 ACPI PM2_CNTL I/O Port

Register Name : **PM2_CNTL - ACPI PM2_CNTL I/O Port**

I/O Address : **0000h - 0FFFFh Movable**

The address is defined by M1541 index 0E9h-0E8h

Default Value : 00h

Attribute : Read/Write

Size : This register must be 8-bit I/O access.

Bit Number	Bit Function
7-1 (00h)	Reserved.
0 (0)	PCI Master Arbiter Function. 0 : enable. 1 : disable. This bit is used to control the PCI Master Arbiter Function. When this bit is set to be '1', the M1541 internal PCI master arbiter will be disabled, and the M1541 on behalf of the CPU host is the only one master in the system. In normal operation, the bit must be set to '0'.

4.8 M5243 Configuration Space

M1541 built-in PCI-to-PCI bridge M5243 PCI_66 Configuration Space -- Device 1 *

The M1541 will respond to PCI-to-PCI bridge configuration access for which AD12=IDSEL is high during the address phase.

The PCI to PCI bridge is called M5243 and is a Device -1 device.

Register Index **01h-00h**

Register Name **VID - Vendor Identification Register**

Default Value 10B9h

Attribute Read Only

Size 16 bits

Description This is a 16-bit value assigned to Acer Labs Inc. This register is combined with index 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index **03h-02h**

Register Name **DID - Device Identification Register**

Default Value 5243h

Attribute Locked Read/Write

Size 16 bits

Description This is a 16-bit value . Default is 5243h.

It is controlled by index 90h bit 3(P2P_BRI_DEV_ID_EN), when the bit = '1' then enable write this port)

Register Index **05h-04h**

Register Name **COM - Command Register**

Default Value 0006h

Attribute Read/Write

Size 16 bits

Bit Number	**Bit Function**
15-9 (000h)	Reserved.
8 (0)	Enable the GSERRJ Output Driver. 0 : Disable. 1 : Enable.

	GSERRJ uses an o/d (Open Drain) pad in M5243. The motherboard design should use a pull-up resistor (2.2KΩ) to keep this pin logic high. When the PCI_66 Parity check is enabled and an error is found, the M5243 will drive GSERRJ low to M1533/ M1543 to generate NMI when this bit is enabled. Disabling the GSERRJ output driver will always keep this output logic high. This bit is reset to 0 and should be set to 1 by BIOS in systems that wish to report Parity error.
7 (0)	Enable Address/Data Stepping. M5243 does not support this feature. Write to this bit has no effect.
6 (0)	Respond to Parity Errors. 0 : Disable. 1 : Enable. The M5243 will do a PCI parity check in CPU to PCI read and PCI to local memory write. This bit is used to enable the parity check. When a parity error is detected, the M5243 will assert GSERRJ and set the Parity Error Bit in the DS register.
5 (0)	Enable VGA Palette Snooping. 0 : No broadcasting for I/O write 3C6H, 3C8H, 3C9H 1 : Broadcasting for I/O write 3C6H, 3C8H, 3C9H
4 (0)	Enable Post Memory Write Command. M5243 does not support this feature. Write to this bit has no effect.
3 (0)	Enable Special Cycle. M5243 does not support this feature. Write to this bit has no effect.
2 (1)	Control to Act As a PCI Bus Master. M5243 does not support to disable bus master operations. This bit is set to 1 during Power-On to enable PCI master operations. Write to this bit has no effect.
1 (1)	Enable Response to Memory Access. M5243 always accepts PCI master accesses to local memory.
0 (0)	Enable Response to I/O Access. M5243 responds to any PCI master I/O accesses.

Register Index : **07h-06h**

Register Name : **DS - PCI_66 Device Status Register**

Default Value : 0400h

Attribute : Read Only, Read/Write Clear

Size : 16 bits

Bit Number	**Bit Function**
15 (0)	Detected Parity Error. This bit is set by the M5243 whenever it detects a parity error in a PCI_66 transaction even if parity error handling is disabled (as controlled by bit6 in the command register). Software can reset this bit to 0 by writing a 1 to it.
14 (0)	Signaled System Error. The M5243 will set this bit whenever it asserts GSERRJ. Software can reset this bit to 0 by writing a 1 to it.
13 (0)	Received Master Abort. This bit is set by M5243 whenever it terminates a CPU to PCI_66 transaction with master abort. This bit is cleared by writing a 1 to it.
12 (0)	Received Target Abort. This bit is set by the M5243 whenever its initiated CPU to PCI_66 transaction is terminated with a target abort. This bit is cleared by writing a 1 to it.
11 (0)	Send Target Abort. This bit is set by devices that act as a target to terminate a transaction by target abort. The M5243 never terminates a transaction with target abort therefore this bit is never set. A write to this bit has no effect.
10-9 (10)	DEVSELJ Timing. Read Only 00 : Fast. 01 : Medium. 10 : Slow. The M5243 timing for DEVSELJ assertion. Slow timing is selected. The actual timing of DEVSELJ is medium
8-5 (0h)	Reserved
4 (0h)	CAP_LIST, read only If write '1' to M5243 offset 90h bit 0 then this bit = '1' If write '0' to M5243 offset 90h bit 0 then this bit = '0'
3-0 (0h)	Reserved.

Register Index **08h**

Register Name : **RI - Revision ID Register**

Default Value 00h (A0 Stepping)

Attribute Read Only

Size 8 bits

Description This register contains the version number of PCI_66 device. The value 00 means A0 stepping.

Register Index **09h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Register Index 0Ah
Register Name : **SCC - Sub-Class Code Register**
Default Value 04h : PCI to PCI Bridge
Attribute : Read Only
Size : 8 bits
Description : These registers contain the sub-Class Codes of the PCI_66.

Register Index **0Bh**
Register Name : **CC - Class Code Register**
Default Value 06h, Bridge device
Attribute : Read Only
Size : 8 bits
Description : These registers contain the Class Codes of the PCI_66.

Register Index **0Ch**
Register Name : **Reserved Registers**
Default Value : 00h
Attribute : Read Only

Register Index : **0Dh**
Register Name : **LT - PCI Latency Timer value**
Default Value : 20h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-3 (04h)	Master Latency Timer Count Value. LT is used to control the amount of time the M5243, as a bus master, can burst data to the PCI_66 Bus. It can be used to guarantee a minimum amount of the system resources.
2-0 (0h)	Reserved. They are assumed to be 0 when determining the Count Value.

Register Index : **0Eh**
Register Name : **Head type**
Default Value : 01h
Attribute : Read only

Size : 8 bits

Register Index : **0Fh-18h**

Register Name : **Reserved**

Register Index : **19h**

Register Name : **Secondary Bus Number Register**

Default Value : 01h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-0 (00h)	Bus Number assigned to the second bus of "virtual" PCI-to-PCI bridge

Register Index : **1Ah**

Register Name : **Subordinate Bus Number Register**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	Bus Number for the subordinate bus that resides at the level below A.G.P. (Default "00000000")

Register Index : **1Bh**

Register Name : **Secondary Master Latency Timer value**

Default Value : 20h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0 (20h)	Timer Value for Latency Counter

Register Index : **1Ch**

Register Name : **I/O Base Address Register**

Default Value : 0F0h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-4 (0fh)	Corresponds to A[15:12] of the I/O Base Address
3-0 (0h)	Reserved

Register Index : **1Dh**

Register Name : **I/O limit Address Register**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function

7-4 (00h)	Corresponds to A[15:12] of the I/O limit Address
3-0 (00h)	Reserved

Register Index : **1Fh-1Eh**

Register Name : **Secondary PCI-PCI Status Register**

Default Value : 00h

Attribute : Read/Write

Size : 16 bits

Bit Number	Bit Function
15 (0)	Set when M5243 detects a parity error AGP.
14 (0)	Set when M5243 asserts GSERRJ.
13 (0)	Set when receives a Master Abort at CPU to AGP cycle.
12 (0)	Set when receives a Target Abort at CPU to AGP cycle.
11-0 (000h)	Reserved.

Register Index : **21h-20h**

Register Name : **Memory Base Address Register**

Default Value : 0FFF0h

Attribute : Read/Write

Size : 16 bits

Bit Number	Bit Function
15-4 (0FFFh)	Corresponds to A[31:20] of the CPU to AGP non-prefetchable memory Base Address
3-0 (0h)	Reserved

Register Index : **23h-22h**

Register Name : **Memory Limit Address Register**

Default Value : 0000h

Attribute : Read/Write

Size : 16 bits

Bit Number	Bit Function
15-4 (000h)	Corresponds to A[31:20] of the CPU to AGP non-pre-fetchable memory Limit Address
3-0 (0h)	Reserved

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Register Index : **25h-24h**

Register Name : **Pre-fetchable Memory Base Address Register**

Default Value : 0FFF0h

Attribute : Read/Write

Size : 16 bits

Bit Number	Bit Function
15-4 (0fffh)	Corresponds to A[31:20] of the CPU to AGP Pre-fetchable memory Base Address
3-0 (0h)	Reserved

Register Index : **27h-26h**

Register Name : **Pre-fetchable Memory Limit Address Register**

Default Value : 0000h

Attribute : Read/Write

Size : 16 bits

Bit Number	Bit Function
15-4 (000h)	Corresponds to A[31:20] of the CPU to AGP Pre-fetchable Memory Limit Address
3-0 (0h)	Reserved

Register Index : **33h-28h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Register Index : **34h**

Register Name : **Capability pointer Register**

Default Value : 0E0h

Attribute : Locked Read/write

Size : 8 bits

Bit Number	Bit Function
7-0 (0e0h)	Point to the start index of AGP standard register block Default is pointer to index 0E0h. If M1541 index 90h bit1=1 then this register can be read/written

Register Index : **3Dh**

Register Name : **Interrupt pin**

Default Value : 00h

Attribute : Read only

Size : 8 bits

Register Index : **3Ch**

Register Name : **Interrupt line**

Default Value : 00h

Attribute : Lock Read/Write (control bit M1541 offset 90 bit 7)

Size : 8 bits

Register Index : **3Bh-35h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Register Index : **3Fh-3Eh**

Register Name : **PCI-to-PCI Bridge Control Register**

Default Value : 0000h

Attribute : Read/Write

Size : 16 bits

Bit Number	**Bit Function**
15-11 (00h)	Reserved
10 (0)	Discard Timer Status when set to 1, indicates that a delayed transaction has been discarded
9 (0)	Secondary Discard Timer Enable 0 : disable 1 : enable
8-4 (00h)	Reserved

3 (0)	VGA Enable (Control the routing of CPU-initiated transactions target VGA compatible I/O (3B0h~3BBh & 3Coh~3DFh) and memory (0A0000h~0BFFFFh)address region to AGP. 0 : disable 1 : enable
2 (0)	ISA Enable (Control the routing of CPU-initiated transaction target ISA I/O address region to AGP) 0 : disable, forward to AGP if in the range between IOBASE and IOLIMIT 1 : enable, forward the top 768Bytes of each 1KByte block (IOBASE~IOLIMIT) to primary PCI.
1 (0)	System Error Enable (Control the routing of GSERRJ from AGP side to SERRJ on the primary PCI) 0 : disable (forwarding of GSERRJ to primary SERRJ is disable) 1 : enable (forward to primary PCI)
0 (0)	Parity Error Response Enable 0 : disable (ignores address and data parity errors on the AGP) 1 : enable (assert GSERRJ)

Register Index : **83h-40h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Register Index : **85h-84h**

Register Name : **PCI_66 Programmable Frame Buffer Memory Region**

Default Value : 0000h

Attribute : Read/Write

Size : 16 bits

Bit Number	Bit Function
15-4 (000h)	Starting address of Programmable Frame Buffer The 12-bits correspond to A[31:20] of the starting address. The remaining bits A[19:0] is assumed to be zero. These bits combined with bits 3-0 can determine the Frame Buffer starting address and stopping address. When Index-86h bit 0 is set to '1', the M5243 will decode the boundary and enable CPU to PCI write buffer.
3-0 (0h)	Size of Programmable GFrame Buffer 0000 : 1 MBytes. 0001 : 2 MBytes. 0010 : 4 MBytes. 0011 : 8 MBytes. 0100 : 16 MBytes. 1XXX : all CPU to PCI_66 Memory Write Cycle into buffer The GFrame Buffer Region should not overlap with local memory.

Register Index : **86h**

Register Name : **CPU to PCI_66 Write Buffer Option**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-6 (00)	Reserved
5 (0)	GCLKRUNJ/GSERRJ function select 0 : GSERRJ 1 : GCLKRUNJ This bit decides whether the GCLKRUNJ/GSERRJ will be GCLKRUNJ or GSERRJ.
4 (0)	GPERRJ on PCI_66 bus forward to PERRJ on PCI_33 bus enable 0 : disable 1 : enable When enable this bit, the PCI_66 bus GPERRJ error will reflect at PCI_33 PERRJ signal.
3 (0)	LINEAR_WORD-Merge for GFrame Buffer Cycle 0 : disable 1 : enable When this bit is enabled, only the consecutive linear increased addresses can be merged. Otherwise, the second write cycle will write into a new Host to PCI_66 Write Buffer location instead of merging with the previous buffer location posted by the first write cycle.
2 (0)	Use PCI_66 Write-Burst 0 : disable 1 : enable This bit is used to enable PCI_66 write burst capability. If this bit is enabled, the consecutive PCI_66 write cycles will become a burst cycle on the PCI_66 bus.
1 (0)	VGA 0A0000-0BFFFF Fixed Frame Buffer 0 : disable 1 : enable This bit is used to enable 0A0000h-0BFFFFh Frame Buffer and the Host to PCI_66 Write Buffer.

0 (0)	Programmable Frame Buffer. 0 : disable 1 : enable This bit is used to combine with index 85h-84h to enable the programmable PCI_66 Frame Buffer and the Host to PCI Write Buffer.

Register Index : **87h**

Register Name : **CPU to PCI_66 Option**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7 (0)	Reserved.
6 (0)	Monochrome Device Adapter Enable 0 : disable 1 : enable If this bit is set to enable and M5243 index 3Eh bit3=1(VGA enable), then the Memory region 0B7FFFh-0B0000h and IO address 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh will send forward to PCI_33.
5 (0)	Graphic Non_buffer FRAMEJ Request control 0 : Enable the Graphic Non_buffer FRAMEJ request control 1 : Disable the Graphic Non_buffer FRAMEJ request control This bit is used to control the internal Non_buffer FRAMEJ request control
4-0 (00h)	Reserved

4.8.1 PCI_66 to Host Interface Register

Register Index : **88h**

Register Name : **PCI_66 to Main Memory / PCI_66 Arbiter Option**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7 (0)	PCI_66 master GAT mode 0 : disable 1 : enable When this bit is enabled, if PCI_66 master is retried during a read transaction, the master will be marked as a GAT master. When the same master retries the transaction at a later time, M5243 will flush the designed buffers before granting the bus ownership to it.

6-4 (000)	Reserved.
3 (0)	Force PCI_66 GAT Mode 0 : disable 1 : enable When this bit is enabled, the M5243 will flush all necessary internal buffers before granting to the PCI_66 master.
2 (0)	Force Host to PCI_66 write request to assert all the time 0 : disable 1 : enable When this bit is enabled, the M5243 will always assert its request for PCI_66 bus ownership.
1-0 (00)	Reserved

Register Index : **89h**

Register Name : **PCI_66 Arbiter Time Slice**

Default Value : 20h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-0 (20h)	Number of PCI_66 clocks for PCI_66 bus time slice The time-slice will guarantee the minimum clocks that the PCI_66 master be granted the ownership of PCI_66 bus. The time-slice counter is started when PCI_66 grant is asserted and bus is idle. The bits 1-0 are assumed to be "00" and are ignored.

Register Index : **8Ah**

Register Name : **CPU Arbiter Time Slice**

Default Value : 20h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-0 (20h)	Number of PCI_66 clocks for CPU Bus time slice. The time-slice will guarantee the minimum clocks that the CPU master be granted the ownership of PCI_66 bus. The time-slice counter is started when PCI_66 grant is asserted and bus is idle. The bits 1-0 are assumed to be "00" and are ignored..

Register Index : **8Bh**

Register Name : **PCI_66 Retry Control for PCI-66 to Host Cycle**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	**Bit Function**
7-4 (0h)	Reserved
3-2 (00)	Retry Latency for PCI_66 to PCI_33 Cycle Control 00 : Retry on first Data phase if wait state > 32 PCI_66clocks or Retry on Second Data phase if wait state > 8 PCI_66 clocks 01 : Retry on first Data phase if wait state > 16 PCI_66 clocks or Retry on Second Data phase if wait state > 4 PCI_66 clocks The following setting is pseudo delay transaction mode 10 : Retry on first Data phase if wait state > 2 PCI_66 clocks or Retry on Second Data phase if wait state > 2 PCI_66 clocks 11 : Never Retry on first Data phase. Never Retry on Second Data phase

1-0 (00h)	Retry Latency for PCI_66 to Host Cycle Control 00 : Retry on first Data phase if wait state > 32 PCI_66 clocks or Retry on Second Data phase if wait state > 8 PCI_66 clocks 01 : Retry on first Data phase if wait state > 16 PCI_66 clocks or Retry on Second Data phase if wait state > 4 PCI_66 clocks The following setting is pseudo delay transaction mode 10 : Retry on first Data phase if wait state > 2 PCI_66 clocks or Retry on Second Data phase if wait state > 2 PCI_66 clocks 11 : Never Retry on first Data phase Never Retry on Second Data phase

Register Index : **8Ch**

Register Name : **PCI_66 to Main Memory Option**

Default Value : 00h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7 (0)	Check PCI_66 master memory read multiple command 0 : enable 1 : disable When this bit is enable, the M5243 will recognize memory read multiple PCI_66 command.
6-2 (00)	Reserved
1-0 (00)	PCI_66 to Host Read Buffer Pre-fetch Threshold 00 : Reserved 01 : Pre-fetch two lines at most 10 : Pre-fetch three lines at most 11 : Reserved

Register Index : **8Dh**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Register Index : **8Eh**

Register Name : **AGP Write/AGP Read Arbiter Time Slice**

Default Value : 020h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function

7-0 (20h)	Number of PCI_66 clocks for AGP write/AGP read master bus time slice The Time-Slice will guarantee the minimum clocks that the AGP write/AGP read master be granted the ownership of PCI_66 bus. The time-slice counter is started when PCI_66 grant is asserted and bus is idle. The bits 1-0 are assumed to be "00" and are ignored.

Register Index : **8Fh**

Register Name : **PCI_33 to PCI_66 Write Arbiter Time Slice**

Default Value : 20h

Attribute : Read/Write

Size : 8 bits

Bit Number	Bit Function
7-0 (20h)	Number of PCI_66 clocks for PCI_33 to PCI_66 write bus time slice The Time-Slice will guarantee the minimum clocks that the PCI_66 master be granted the ownership of PCI_66 bus. The time-slice counter is started when PCI_66 grant is asserted and bus is idle. The bits 1-0 are assumed to be "00" and are ignored.

Register Index : **0DFh-90h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

4.8.2 PCI_66 Green Function Support

Register Index : **0E0h**

Register Name : **PCI_66 Power Management Capability Identifier Register**

Default Value : 01h

Attribute : Locked Read/Write

Bit Number	Bit Function
7-0 (01h)	PCI_66 Capability Identifier The capability identifier, when read by system software as 01h indicates that the data structure currently being pointed to is the PCI Power management data structure. The register default is read only, when M1541 index 90h bit 5 = 1 , this register can be read/write.

Register Index : **0E1h**

Register Name : **PCI_66 Power Management Next Item Pointer Register**

Default Value : 00h

Attribute : Locked Read/write

Bit Number	Bit Function
7-0 (00h)	PCI_66 Next Item Pointer This field provides an offset into the function's PCI configuration space pointing to the location of next item in the function's capability list. If there are no additional items in the capabilities list, this register is set to 00h. The register default is read only, when M1541 index 90h bit 5 = 1 , this register can read/write.

Register Index : **0E3h-0E2h**

Register Name : **PCI_66 Power Management Capabilities Register**

Default Value : 0000h

Attribute : Locked Read/write. The register default is read only, when M1541 index 90h bit 5 = 1, this register can read/write.

Bit Number	**Bit Function**
15-11 (00000)	PCI_66 PME_Support XXXX1 : PMEJ can be asserted from D0 XXX1X : PMEJ can be asserted from D1 XX1XX : PMEJ can be asserted from D2 X1XXX : PMEJ can be asserted from D3 hot 1XXXX : PMEJ can be asserted from D3 cold These five bits field indicate the power states in which function may assert PMEJ. A value of ‘0’ for any bit indicates that the function is not capable of asserting the PMEJ signal while in that power state.
10 (0)	PCI_66 D2_Support 0 : Do not support D2 1 : Support D2 If this bit is a ‘1’ , M5243 supports the D2 power management state.
9 (0)	PCI_66 D1_Support 0 : Do not support D1 1 : Support D1 If this bit is a ‘1’, M5243 supports the D2 power management state.
8-6 (000)	Reserved
5 (0)	PCI_66 Device Specific Initialization (DSI) 0 : Not required 1 : Required If this bit is ‘1’, it indicates that the function requires a device specific initialization sequence following transition to the D0 un-initialized state.
4 (0)	PCI_66 Auxiliary Power Source This bit is only meaningful if the bit 15 (PMEJ can be asserted from D3 cold) = 1 0 : Supply own auxiliary power source 1 : Support for PMEJ in D3 cold requires auxiliary power supplied by the system by way of proprietary delivery vehicle.

3 (0)	PCI_66 PME clock 0 : It indicates that M5243 relies on the presence of the PCI_66 clock for PMEJ operation 1 : It indicates that no PCI clock is required for M5243 to generate PMEJ.
2-0 (001)	Version of PCI_66 power management interface specification The version support is V1.0 now.

Register Index : **0E5h-0E4h**

Register Name : **PCI_66 Power Management Control and Status Register**

Default Value : 0000h

Attribute : Some bits can read/write, some bits are Locked read/write. These bits marked with Locked read/write default is read only, when index 90h bit 5 = 1 , these bits can read/write.

	Bit Function
15 (0)	PCI_66 PME_Status (Read/Write_clear) This bit is set when the function would normally assert the PMEJ signal independent of the state of the PME_EN (index 0E4h bit 8) Write "1" to this bit will clear this bit to "0" and cause the M5243 to stop asserting a PMEJ (if enable). Writing a "0" has no effect. This bit defaults to "0" if the M5243 does not support PMEJ generation from D3 cold.
14-13 (00)	PCI_66 Data_scale (Locked read/write) These two bits field indicate the scaling factor to be used when interpreting the value of the DATA register(index 0e7h) . The value & meaning of this field varies depending on which data value has been selected bit[12-9] (DATA_select) field.
12-9 (0h)	PCI_66 Data_Select (read/write) These four bits are used to select which data is to be reported through DATA register (index 0E7h) and data scale (bit[14-13]) field.
8 (0)	PCI_66 PME_EN (read/write) 0 : PMEJ assertion is disable 1 : Enable the function to assert PMEJ
7-2 (00h)	Reserved (Locked read/write)
1-0 (00)	PCI_66 Power State (read/write) 00 : D0 01 : D1 10 : D2 11 : D3 hot These two bits are used to determine the current power state of a function and set the function into a new power state. If software attempts to write an unsupported, optional state to this field. The write operation must complete normal on the bus, however the data is discarded and no state change occurs.

Register Index : **0E6h**

Register Name : **PCI_66 PMCSR PCI to PCI Bridge Support Extensions**

Default Value : 00h

Attribute : Locked Read/write. The register default is read only, when index 90h bit 5 = 1 , this register can read/write.

Bit Number	**Bit Function**
7 (0)	PCI_66 Bus Power/Clock Control Enable 0 : PCI_66 Bus power/clock control mechanism has been disabled 1 : PCI_66 Bus power/clock control mechanism has been enabled When the Bus Power/Clock control mechanism is disabled, the bridge's PMCSR Power State field cannot be used by the system software to control the power or clock of the bridge's secondary bus.
6 (0)	B2/B3 support for D3 hot 0 : The bridge function is programmed to D3 hot, its secondary bus will have its power removed (B3) 1 : The bridge function is programmed to D3 hot, its secondary bus PCI_66 clock will be stopped (B2) The state of this bit determines the action that is to occur as a direct result of programming the function to D3 hot. This bit is only meaningful if bit 7=1 (PCI_66 Bus Power/Clock control enable)
5-0 (00h)	Reserved.

Register Index : **0E7h**

Register Name : **Data Register**

Default Value : 00h

Attribute : Locked Read/write. The register default is read only, when index 90h bit 5 = 1 , this register can read/write.

Bit Number	**Bit Function**
7-0 (00h)	PCI_66 Data[7-0] This register is used to report the state dependent data requested by the Data_Select (index 0E4h bit[12-9]) field. The value of this register is scaled by the value reported by the Data_Scale (Index 0E4h bit[12-9]) field.

Register Index : **0FFh-E8h**

Register Name : **Reserved Registers**

Default Value : 00h

Attribute : Read Only

Section 5 : Hardware Setup Guide

The M1541 will strobe the hardware setting value in the respective registers when the RSTJ goes inactive. BIOS can utilize the register value to save the software programming time to detect L2 type, size, PLL enable/disable and setting the bus frequency. For notebook applications, it is recommended to use software programming to reduce power consumption since the pull-up and pull-down resistors will continuously consume system power. If the BIOS wants to utilize the hardware setting value, the system board designer must make sure the strobe value is identical to their definition. Otherwise, the software programming must be used to detect the hardware configuration. The HA[31:19] default is pull low by M1541. The pull low resistor range is from 60K Ohm to 20K Ohm and the typical value is 40K Ohm. If circuit needs to pull high, a below or equal to 10K pull high resistor is required.

Pin Name	Description	Pull-up	Pull-down	Register	Note
HA[31..29]	Indicate Host frequency	-	-	Index-0EDh bits[7:5]	(1)
HA[28]	CPU interface PLL support	Enable	Disable	Index-0EDh bit[4]	-
HA[27:25]	CPUCLK compensate select	-	-	Index 0EDh bits [3-1]	(4)
HA[24]	CPUCLK PLL internal test select	Test mode	Normal mode	Index 0EDh bit[0]	
HA[27-26]	CPUCLK compensate select	-	-	Index 0EDh bits[3-2]	(5)
HA[25-24]	HD output clock select	-	-	Index 0EDh bit[1-0]	(6)
HA[23]	Internal TAG support	Enable	Disable	Index-040h bit[6]	-
HA[22]	L2 cache type select	MOSYS cache	PB_SRAM	Index-41h bit[4]	-
HA[21..20]	Cache size detect	-	-	Index-41h bits[3:2]	(3)
HA[19]	L2 bank select	2-bank	1-bank	Index-41h bit[5]	-

Note : (1)

HA31	HA30	HA29	Host frequency
0	0	0	Reserved
0	0	1	60 MHz
0	1	0	66 MHz
0	1	1	75 MHz
1	0	0	83 MHz
1	0	1	90 MHz
1	1	0	100 MHz
1	1	1	Reserved

The Host frequency setting is only for BIOS to reference. It will not influence the internal circuit behavior.

(3)

HA21	HA20	Cache size
0	0	256KB
0	1	512KB
1	0	1MB
1	1	None

Note (4) For M1541 A1 C and earlier version

HA27	HA25	HA24	CPU CLK compensate select
0	0	0	No compensate
0	0	1	1 buffer
0	1	0	2 buffers
0	1	1	3 buffers
1	0	0	4 buffers
1	0	1	5 buffers
1	1	0	6 buffers
1	1	1	7 buffers

For M1541 A1 D and later version

Note (5)

HA27	HA26	CPU CLK compensate select
0	0	No compensate
0	1	2 buffers
1	0	4 buffers
1	1	6 buffers

Note (6)

HA25	HA24	HD output clock select
0	0	default
0	1	ahead 1 ns
1	0	ahead 2 ns
1	1	ahead 3 ns

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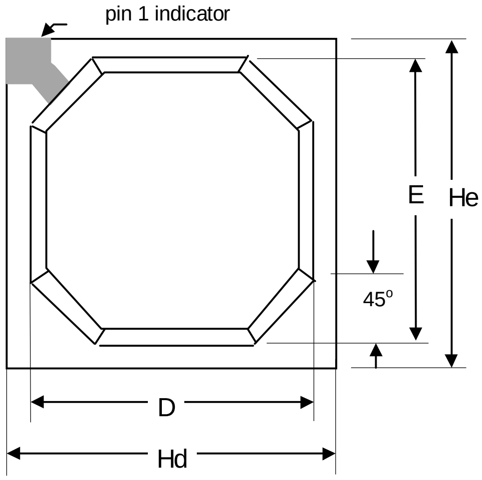
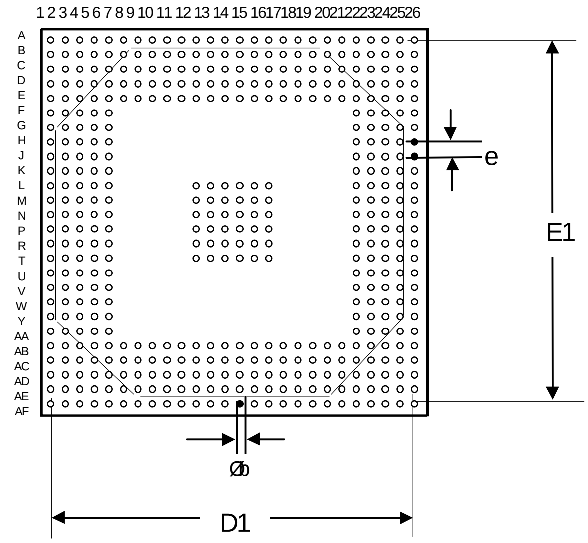
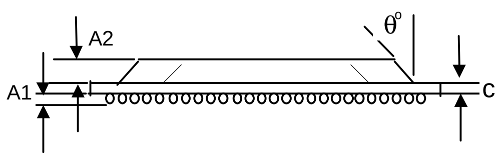
Section 6 : Packaging Information

456L BGA Dimension Spec (35 x 35 mm)







Symbol	Min.	Nom.	Max.
A1	0.50	0.60	0.70
A2	1.12	1.17	1.22
b	0.60	0.75	0.90
c	0.51	0.56	0.61
D	29.80	30.00	30.20
D1	31.55	31.75	31.95
E	29.80	30.00	30.20
E1	31.55	31.75	31.95
e		1.27	
Hd	34.80	35.00	35.20
He	34.80	35.00	35.20
°	23°	30°	37°

Section 7 : Revision History

Initial version	10/15/97	
p.6-9,11-13,18,20,25,28-30,36-38,40,59,65,81,82,95,97,108,109	10/20/97	
p.2,6-9,16-22,28	10/23/97	
p.45,104,118-121,123,125,126,128,130,133,134	11/20/97	
p.32	12/19/97	
Appendix A	02/16/98	
p.45,63-65,72,81,96-99,101-103,105-107,113,115-117,128,130,136	03/12/98	
p.117,118	04/08/98	
p.96,114	04/15/98	
p.57,101	06/02/98	
p.128	06/03/98	
p.1	06/12/98	
p.27,28,31,56,64,72,96-98,103,105,115-117	06/19/98	
p.52,57,65,81,96,97	07/16/98	HHC

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