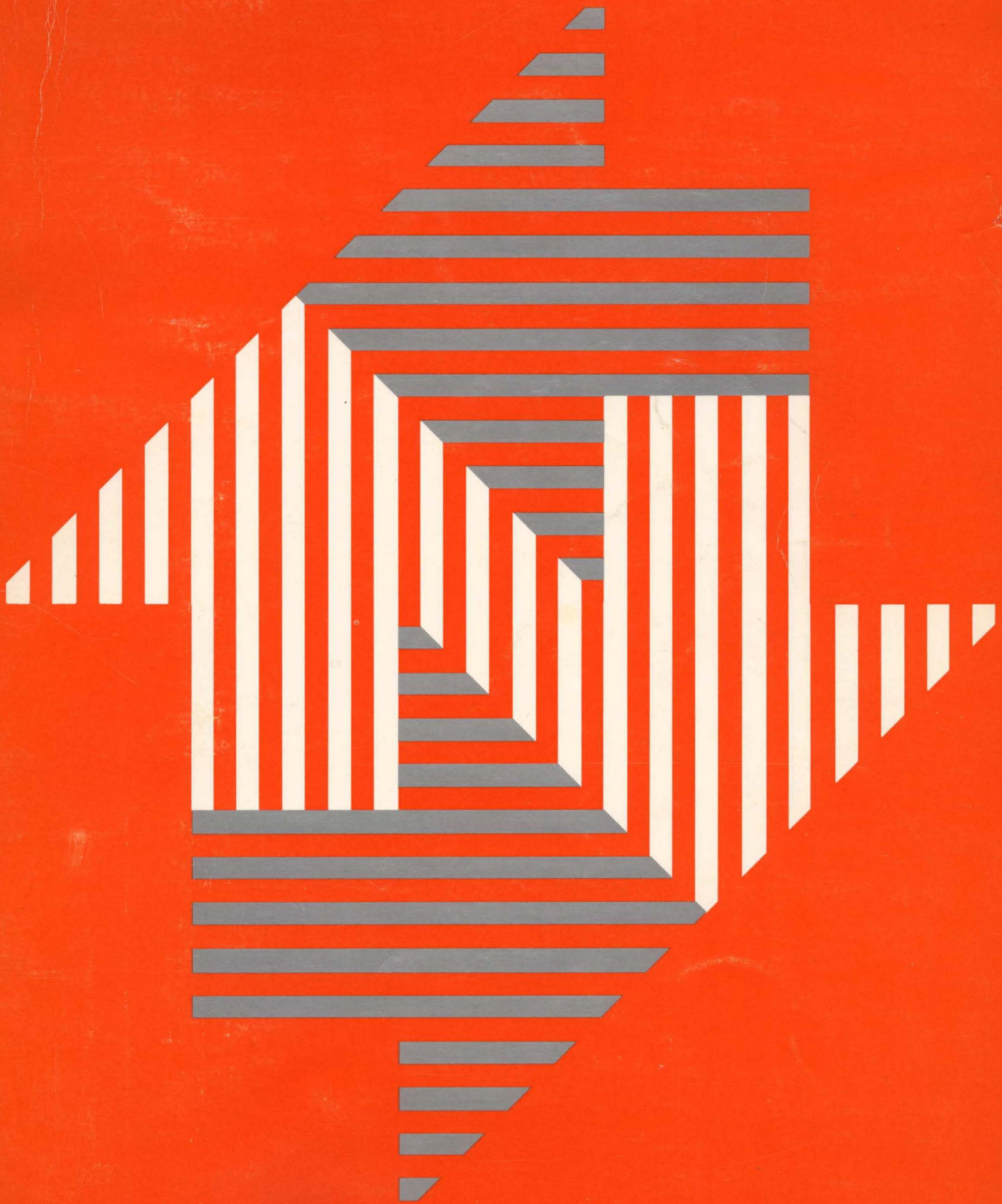


AMI

# Guide to MOS Products

AMI

Guide to MOS Products



May  
1977

# Future Products

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## MEMORIES

- RAM – 1024 x 1 bit High Speed (60/45 ns), VMOS, 16 pins
  - RAM – 1024 x 4 bit Static, VMOS
  - RAM (S6518) – 1024 x 1 bit Static CMOS, 18 pins
  - RAM – 4096 x 1 bit Static, N-Channel depletion load
  - RAM – 1024 x 4 bit Static N-Channel depletion load
  - ROM – 2048 x 8 bit High Speed (less than 200 ns) VMOS
- 

## AMI 6800 MICROCOMPUTER SYSTEMS FAMILY

### Depletion Mode Circuits

- 8 bit MPU (S6800) – functionally identical to enhancement mode S6800 circuit
- Peripheral Interface Adapter (S6820) – functionally identical to enhancement mode S6820 circuit

### Industrial Temperature Range Circuits (-40° to +85°C)

- 8 bit MPU (S6800I) – functionally identical to S6800
- Peripheral Interface Adapter (S6820I) – functionally identical to S6820

### Two-Chip Microcomputer System

- MPU (S6802) – with on-chip 128 x 8 RAM and a clock generator
- Input/Output (S6846) – with 10 bidirectional input/output lines, 2K bytes of ROM and a programmable timer.

### Peripheral Circuits

- General Purpose Bus Interface Circuit (S68488) – conforms to IEEE 488 specifications.
  - Serial Synchronous Data Adapter (S6852) – a bus compatible high speed synchronous communications interface.
  - Video Generator Circuit – provides composite video input to a color or monochrome standard TV receiver (used as a low cost graphics terminal).
  - Advanced Data Link Controller (S6854) – compatible with data link communications standards such as ANSI – ADCCP, IBM – SDLC, and HDLC
  - Programmable Timer Module (S6840) – provides interval timing for controlling machine interfaces
- 

## TELECOMMUNICATIONS CIRCUITS

- Auto Dialer (S2560) – a CMOS dialer with BCD display output; operates directly from telephone line
  - Tone Ringer (S2561) – a CMOS externally triggerable bell ringer simulator
- 

## CONSUMER CIRCUITS

- Microprocessor/Controller (S2000) – a versatile controller with internal RAM and ROM, wide variety of interface for external I/O and memory. Keyboard inputs can interface with capacitive TouchControl switches.
- 

## ORGAN CIRCUITS

- Noise Generator (S2688) – P-channel ion implanted MOS seventeen-bit shift register clocked by an internal RC oscillator. Outputs wide bandwidth pseudo white noise for cymbal, brush, sandblock, snaredrum, and other sound generation. (Second source for National MM 5837)
  - Analog Shift Register (S10111) – similar to the S10110, but with an on-chip clock
- 

## WATCH/CLOCK CIRCUITS

- LCD Watch Circuit (S2733) – four digits, six functions
  - LCD Watch Circuit – six digits, seven functions
  - LCD Watch Circuit – six digits, multiple functions
  - Clock Radio Circuit – high feature circuit for use with LED, fluorescent or gas discharge displays
  - 12V Auto Clock Circuit (S2709) – for use with fluorescent display (4 MHz crystal input)
- 

## LIQUID CRYSTAL DISPLAYS

- 24-hour Clock Display
- Alphanumeric Clock Display
- 4½-digit Instrument Display
- Calculator Display

# EDGE INDEX

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- 1** ORDERING INFORMATION/PACKAGING \_\_\_\_\_  
*(AMI Sales Offices, Distributors, Representatives)*
- 2** MEMORIES \_\_\_\_\_
- 3** AMI 6800 MICROCOMPUTER SYSTEMS FAMILY \_\_\_\_\_
- 4** COMMUNICATIONS AND INTERFACE CIRCUITS \_\_\_\_\_
- 5** ORGAN CIRCUITS \_\_\_\_\_
- 6** WATCH/CLOCK CIRCUITS \_\_\_\_\_
- 7** LIQUID CRYSTAL DISPLAYS \_\_\_\_\_
- 8** APPLICATION NOTES \_\_\_\_\_
- 9** CUSTOM CAPABILITIES \_\_\_\_\_
- 10** AMI PRODUCT ASSURANCE PROGRAM \_\_\_\_\_
- 11** MOS PROCESSES \_\_\_\_\_

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This catalog prepared for American Microsystems, Inc., by The Vada Company.

# **MOS/LSI is the Business of AMI**

. . . and MOS/LSI is AMI's main business. The first company to successfully produce commercial quantities of MOS circuits in 1966, AMI has ever since provided leadership in circuit design, manufacturing technology, and new product and market development.

**DESIGN EXPERIENCE** — Many areas of application in which MOS is used today was pioneered with an AMI-designed device. This accumulated experience results in high performance standard products and imaginatively designed cost-effective custom circuits.

**PROCESS VERSATILITY** — AMI's head start in the industry gives it a mature capability in every one of the major production processes. P-channel metal gate — high and low threshold, with and without ion implantation; P and N channel silicon gate; and CMOS silicon gate make up the company's current repertoire. V/MOS, a new technology developed by AMI for high speed, high density products, is in an advanced R&D stage.

**PRODUCTION CAPABILITY** — AMI has two major manufacturing facilities: Santa Clara, California with 332,000 sq. feet, and Pocatello, Idaho with 94,000 sq. feet. Assembly is done at a third major location — a wholly-owned 98,000 sq. ft. facility at Inchon, Korea. This complex of plants can produce over 1,000,000 LSI circuits a month. At all facilities AMI uses the latest production equipment in order to maximize yields of today's larger circuits.

**PRODUCT RELIABILITY** — Years of concentration on process control and a conservative attitude toward process changes has earned AMI an envied reputation of reliability, and has enabled AMI to become one of the major suppliers of MOS memories to markets throughout the world.

**IT'S STANDARD AT AMI** — The company's dedication to a fine line of standard MOS/LSI products is reflected in the variety and number of state-of-the-art products listed in this catalog.

## **AMI and Made-to-Order MOS**

Since 1966, AMI has designed and manufactured over 1,000 custom MOS circuits. The largest design engineering staff in the industry has helped to keep AMI in the number one position among custom MOS producers.

If your product can be controlled by an MOS circuit, and you plan to manufacture it in high volume, you should contact your nearest AMI Sales Office or the main office in Santa Clara, California. AMI will be happy to discuss the possibility of designing a custom circuit for your application, or manufacturing such a circuit from your tooling.

## **LCDs from AMI**

Six years of experience in field effect liquid crystal display manufacture have helped AMI become a leader in this display technology. In addition to its production facility in Santa Clara, California, a new LCD plant has been constructed in Taichung, Taiwan. AMI formulates its own highly stable moisture insensitive liquid crystal materials that operate at 3 Vac drive.

AMI offers a comprehensive line of standard and custom watch displays (utilizing its proprietary AEA "continuous digit" process) and a series of large area displays for clocks and instrumentation.

# Numerical Index

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Device	Page	Device	Page	Device	Page
TCK100 . . . . .	4-25	S4006 . . . . .	2-2	S6830 . . . . .	3-31
S10110 . . . . .	5-3	S4008 . . . . .	2-2	S6831 . . . . .	3-33
S10129 . . . . .	5-9	S4008-9 . . . . .	2-2	S6834 . . . . .	3-36
S10130 . . . . .	5-11	S4015 . . . . .	2-3	S6834-1 . . . . .	3-36
S10131 . . . . .	5-13	S4015-2 . . . . .	2-3	S6850 . . . . .	3-41
S1103 . . . . .	2-2	S4025 . . . . .	2-3	S6860 . . . . .	3-46
S1103-1 . . . . .	2-2	S4025-2 . . . . .	2-3	D8151A . . . . .	7-7
S1103A . . . . .	2-2	S50240 . . . . .	5-17	D8154A . . . . .	7-7
S1103A-1 . . . . .	2-2	S50241 . . . . .	5-17	D8158A . . . . .	7-8
S1103A-X . . . . .	2-2	S50242 . . . . .	5-17	D8159A . . . . .	7-8
S1103X . . . . .	2-2	S50243 . . . . .	5-2	D8163A . . . . .	7-2
S1424A . . . . .	6-3	S50244 . . . . .	5-2	D81xx . . . . .	7-9
S1424C . . . . .	6-3	S50245 . . . . .	5-2	D8300A . . . . .	7-10
S1425A . . . . .	6-3	S5101 . . . . .	2-7	D8301A . . . . .	7-10
S1427A . . . . .	6-3	S5101-1 . . . . .	2-7	D8302A . . . . .	7-10
S146 . . . . .	2-2	S5101-2 . . . . .	2-7	S8564 . . . . .	2-2
S1856 . . . . .	6-9	S5101-3 . . . . .	2-7	S8771 . . . . .	2-2
S1883 . . . . .	4-3	S5101-8 . . . . .	2-7	S8865 . . . . .	2-2
S1998A . . . . .	6-14	S5101L . . . . .	2-7	S8890 . . . . .	5-20
S1998B . . . . .	6-14	S5101L-1 . . . . .	2-7	S8996 . . . . .	2-2
S1998C . . . . .	6-14	S5101L-2 . . . . .	2-7	S9260 . . . . .	4-21
EVK200 . . . . .	3-62	S5101L-3 . . . . .	2-7	S9261 . . . . .	4-21
S2193 . . . . .	5-7	S5204A . . . . .	2-23	S9262 . . . . .	4-16
S2222 . . . . .	2-2	S5232 . . . . .	2-18	S9263 . . . . .	4-21
S2222A . . . . .	2-2	S6508 . . . . .	2-13	S9264 . . . . .	4-21
EVK300 . . . . .	3-62	S6508A . . . . .	2-13	S9265 . . . . .	4-21
S2350 . . . . .	3-51	S6800 . . . . .	3-9	S9266 . . . . .	4-16
S2559 . . . . .	4-2	S6810 . . . . .	3-22	S9660 . . . . .	5-24
S2567 . . . . .	5-15	S6810-1 . . . . .	3-22	EVK99 . . . . .	3-64
S2600 . . . . .	4-10	S6810A . . . . .	2-2	S9996 . . . . .	2-2
S2601 . . . . .	4-10	S6810A-1 . . . . .	2-2		
S3514 . . . . .	2-18	S6820 . . . . .	3-25		

# Functional Index

Device	Page	Device	Page	Device	Page
<b>RAMs</b>		<b>S6800 MICROCOMPUTER SYSTEMS FAMILY</b>		<b>ORGAN CIRCUITS</b>	
<i>(Selection Guide on Page 2-2)</i>		<i>(Selection Guide on Page 3-3)</i>		<i>(Selection Guide on Page 5-2)</i>	
S1103 . . . . .	2-2	EVK200 . . . . .	3-62	S10110 . . . . .	5-3
S1103-1 . . . . .	2-2	S2350 . . . . .	3-51	S10129 . . . . .	5-9
S1103A . . . . .	2-2	EVK300 . . . . .	3-62	S10130 . . . . .	5-11
S1103A-1 . . . . .	2-2	S5204A . . . . .	2-23	S10131 . . . . .	5-13
S1103A-X . . . . .	2-2	S6800 . . . . .	3-9	S2193 . . . . .	5-7
S1103X . . . . .	2-2	S6810 . . . . .	3-22	S2567 . . . . .	5-15
S146 . . . . .	2-2	S6810-1 . . . . .	3-22	S50240 . . . . .	5-17
S2222 . . . . .	2-2	S6810A . . . . .	2-2	S50241 . . . . .	5-17
S2222A . . . . .	2-2	S6810A-1 . . . . .	2-2	S50242 . . . . .	5-17
S4006 . . . . .	2-2	S6820 . . . . .	3-25	S50243 . . . . .	5-2
S4008 . . . . .	2-2	S6830 . . . . .	3-31	S50244 . . . . .	5-2
S4008-9 . . . . .	2-2	S6831 . . . . .	3-33	S50245 . . . . .	5-2
S4015 . . . . .	2-3	S6834 . . . . .	3-36	S8890 . . . . .	5-20
S4015-2 . . . . .	2-3	S6834-1 . . . . .	3-36	S9660 . . . . .	5-24
S4025 . . . . .	2-3	S6850 . . . . .	3-41		
S4025-2 . . . . .	2-3	S6860 . . . . .	3-46	<b>WATCH/CLOCK CIRCUITS</b>	
S5101 . . . . .	2-7	EVK99 . . . . .	3-64	<i>(Selection Guide on Page 6-2)</i>	
S5101-1 . . . . .	2-7			S1424A . . . . .	6-3
S5101-2 . . . . .	2-7	<b>DATA COMMUNICATIONS CIRCUITS</b>		S1424C . . . . .	6-3
S5101-3 . . . . .	2-7	<i>(Selection Guide on Page 4-2)</i>		S1425A . . . . .	6-3
S5101-8 . . . . .	2-7	S1883 . . . . .	4-3	S1427A . . . . .	6-3
S5101L . . . . .	2-7	S2350 . . . . .	3-51	S1856 . . . . .	6-9
S5101L-1 . . . . .	2-7	S6850 . . . . .	3-41	S1998A . . . . .	6-14
S5101L-2 . . . . .	2-7	S6860 . . . . .	3-46	S1998B . . . . .	6-14
S5101L-3 . . . . .	2-7			S1998C . . . . .	6-14
S6508 . . . . .	2-13	<b>TELECOMMUNICATIONS CIRCUITS</b>		<b>LCDs</b>	
S6508A . . . . .	2-13	<i>(Selection Guide on Page 4-2)</i>		<i>(Selection Guide on Page 7-2)</i>	
S6810 . . . . .	3-22	S2559 . . . . .	4-2	D8151A . . . . .	7-7
S6810-1 . . . . .	3-22	<b>REMOTE CONTROL CIRCUITS</b>		D8154A . . . . .	7-7
S6810A . . . . .	2-2	<i>(Selection Guide on Page 4-2)</i>		D8158A . . . . .	7-8
S6810A-1 . . . . .	2-2	S2600 . . . . .	4-10	D8159A . . . . .	7-8
		S2601 . . . . .	4-10	D8163A . . . . .	7-2
		<b>INTERFACE CIRCUITS (TOUCHCONTROL)</b>		D81xx . . . . .	7-9
		<i>(Selection Guide on Page 4-2)</i>		D8300A . . . . .	7-10
		TCK100 . . . . .	4-25	D8301A . . . . .	7-10
<b>ROMs/PROMs</b>		S9260 . . . . .	4-21	D8302A . . . . .	7-10
<i>(Selection Guide on Page 2-2)</i>		S9261 . . . . .	4-21		
S3514 . . . . .	2-18	S9262 . . . . .	4-16		
S5204A . . . . .	2-23	S9263 . . . . .	4-21		
S5232 . . . . .	2-18	S9264 . . . . .	4-21		
S8771 . . . . .	2-2	S9265 . . . . .	4-21		
S8564 . . . . .	2-2	S9266 . . . . .	4-16		
S8865 . . . . .	2-2				
S8996 . . . . .	2-2				
S9996 . . . . .	2-2				
S6830 . . . . .	3-31				
S6831 . . . . .	3-33				
S6834 . . . . .	3-36				
S6834-1 . . . . .	3-36				
<b>CHARACTER GENERATOR</b>					
<i>(Selection Guide on Page 2-2)</i>					
S8564 . . . . .	2-2				

# Industry Crossreference Guide

Device No.	Replacement	Compatibility (P) OR (F)*
<b>ELECTRONIC ARRAYS</b>		
EA4600	S6831C	P
EA5316	S1998A,B,C	P
<b>FAIRCHILD</b>		
3514	S3514	P
3817	S1998A,B,C	F
6103	S1424A	N/A
93415	S4015	P
93425	S4025	P
<b>GENERAL INSTRUMENTS</b>		
AY-5-1013	S1883	F
R03-16,382	S8996	P
R05-8192	S8865	P
CK-3300	S1998A,B,C	F
AY-1-0212A	S50242	P
AY-1-2006	S10131	P
<b>HARRIS SEMICONDUCTOR</b>		
HM6508	S6508	P
<b>INTEL</b>		
1103	S1103	P
1103-1	S1103-1	P
1103A	S1103A	P
1103A-1	S1103A-1	P
1103A-2	S1103A-2	P
2115	S4015	P
2125	S4025	P
2146	S146	P
2316A	S6831A	P
2316B	S6831B	P
5101	S5101	P
8316A	S6831A	P
8316B	S6831B	P
<b>INTERSIL</b>		
IM6508	S6508	P
ICM7206(A)	S2559	F
ICM7210	S2733	P
TCA350	S10110	P
<b>MOSTEK</b>		
MK2500	S5232	P
MK2600	S3514	P
MK4006	S4006	P
MK4008	S4008	P
MI4008-9	S4008-9	P
MK50240	S50240	P
MK50241	S50241	P
MK50242	S50242	P

Device No.	Replacement	Compatibility (P) OR (F)*
MK50380	S1998A,B,C	F
MK5085,6	S2559	P
<b>MOTOROLA</b>		
MC6800	S6800	P
MC6820	S6820	P
MC6850	S6850	P
MCM6810	S6810	P
MCM6830	S6830	P
M6860	S6860	P
MCC14483	S2733	P
<b>NATIONAL SEMICONDUCTOR</b>		
74C920	S5101	P
MM58127	S1424A	N/A
MM58128	S1424A	N/A
MM58129	S1424A	N/A
MM58130	S1424A	N/A
MM5204C	S5204A	P
5232	S5232	P
5233	S3514	P
MM5316	S1998A,B,C	P
MM5384	S1998A,B,C	F
MM5385	S1998A,B,C	F
MM5386	S1998A,B,C	F
MM5387	S1998A,B,C	F
<b>RCA</b>		
TA6979	S1424A	N/A
<b>SIGNETICS</b>		
1103	S1103	P
1103-1	S1103-1	P
<b>SMC MICROSYSTEMS</b>		
COM2017	S1883	F
<b>TEXAS INSTRUMENTS</b>		
TMS6011	S1883	F
TMS1951	S1998A,B,C	P
TPO232	S1424A	N/A
TPO233	S1424A	N/A
TPO237Y	S2733	P
<b>WESTERN DIGITAL</b>		
TR1602A	S1883	F

\*(P) = Pin-for-pin  
(F) = Functionally



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## **Ordering Information/ Packaging**

# Sales Offices

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## DOMESTIC

### Western Area

100 East Wardlow Road  
Suite 203  
Long Beach, California 90807  
Tel: (213) 595-4768  
TWX: 910-341-7668

3031 Tisch Way  
Suite 202, Drawer No. 126  
San Jose, California 95128  
Tel: (408) 249-4450  
TWX: 910-338-7330

### Central Area

500 Higgins Road  
Suite 210  
Elk Grove Village, Illinois 60007  
Tel: (312) 437-6496  
TXW: 910-222-2853

725 So. Central Expressway  
Suite B5  
Richardson, Texas 75080  
Tel: (214) 231-5721  
TWX: 910-867-4766

29200 Vassar Avenue  
Suite 303  
Livonia, Michigan 48152  
Tel: (313) 478-9339  
TWX: 810-242-2903

Fox Meadows Office Building  
Suite 101  
3030 Harbor Lane North  
Minneapolis, Minnesota 55441  
Tel: (612) 559-9004  
TWX: 910-576-2699

### Eastern Area

20 Robert Pitt Drive  
Room 212  
Monsey, New York 10952  
Tel: (914) 352-5333  
TWX: 710-577-2827

1420 Providence Turnpike  
Suite 220  
Norwood, Massachusetts 02062  
Tel: (617) 762-0726  
TWX: 710-336-0073

237 Whooping Loop  
Altamonte Springs, Florida 32701  
Tel: (305) 830-8889  
TWX: 810-853-0269

Axe Wood East  
Butler & Skippack Pikes  
Suite 3A  
Ambler, Pennsylvania 19002  
Tel: (215) 643-0217  
TWX: 510-661-3878

## INTERNATIONAL

### Hong Kong

American Microsystems, Ltd.  
703 Fu House  
Ice House Street  
Hong Kong, B.C.C.  
Tel: 5-265907  
TLX: 76333

### Japan

AMI Japan  
7th Floor Daiwa Bank Building  
1-6-21, Nishi-Shimbashi  
Minato-ku, Tokyo 105  
Japan  
Tel: (501) 2241  
TLX: 781-0222-5351

### KMI

Inchon Export Industrial Estate  
Block 1  
Hyo Sung-Dong Buk-ku  
Inchon, Korea

AMI Microsystems, GMBH  
Suite 237  
Rosenheimer Strasse 30/32  
8000 Munich 80, West Germany  
Tel: (SV 089) 48 30 81  
TLX: 841-522743

AMI Microsystems, SPA  
Via Pascoli 60  
20133 Milano  
Italy  
Tel: 29 37 45  
TLX: 843 32644

AMI Microsystems, Ltd.  
108A Commercial Road  
Swindon, Wiltshire  
England  
Tel: (0793) 31345 or 25445  
TLX: 851-449349

AMI Microsystems, S.A.R.L.  
124 Avenue de Paris  
94300 Vincennes, France  
Tel: (01) 374 00 90  
TLX: 842-670500

# Distributors

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## WESTERN AREA AND CANADA

Sterling Electronics  
2001 E. University Dr.  
Phoenix, Arizona 85034  
Tel: (602) 258-4531  
TWX: 667317

3540D Pan American Freeway N.E.  
Albuquerque, New Mexico 87107  
Tel: (505) 345-6601  
TWX: 660441

Intermark Electronics  
1020 Stewart Dr.  
Sunnyvale, California 94086  
Tel: (408) 738-1111  
TWX: 910-339-9312

1802 E. Carnegie Ave.  
Santa Ana, California 93708  
Tel: (213) 436-5275  
(714) 540-1322  
TWX: 910-595-1583

Intermark Electronics Cont.  
4040 Sorrento Valley Blvd.  
San Diego, California 92121  
Tel: (714) 279-5200  
TWX: 910-335-1515

Schweber Electronics  
3000 Redhill Ave.  
Costa Mesa, California 92626  
Tel: (714) 556-3880  
(213) 537-4320  
TWX: 910-595-1720

**Semicomp Corp.**

4029 Westerly Pl.  
Newport Beach, California 92660  
Tel: (714) 833-3070  
(213) 595-5153  
TWX: 910-595-1572

**R. V. Weatherford**

6921 San Fernando Rd.  
Glendale, California 91201  
Tel: (213) 849-3451  
TWX: 910-498-2223

1550 Babbitt Ave.  
Anaheim, California 92805  
Tel: (714) 634-9600  
TWX: 910-593-1334

3240 Hillview Ave.  
Palo Alto, California 94304  
Tel: (415) 493-5373  
TWX: 910-373-2177

1095 E. 3rd St.  
Pomona, California 91766  
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(213) 966-8461  
TWX: 910-581-3811

7872 Raytheon Rd.  
San Diego, California 92111  
Tel: (714) 278-7400  
TWX: 910-335-1570

3355 W. Earll Dr.  
Phoenix, Arizona 85017  
Tel: (602) 272-7144  
TWX: 910-951-0636

3905 S. Mariposa  
Englewood, Colorado 80110  
Tel: (303) 761-5432  
TWX: 910-933-0173

541 Industry Dr.  
Seattle, Washington 87188  
Tel: (206) 243-6340  
TWX: 910-444-2054

**Century Electronics**

8155 W. 48th Ave.  
Wheatridge, Colorado 80030  
Tel: (303) 424-1985  
TWX: 910-938-0393

121 Elizabeth N. E.  
Albuquerque, New Mexico 87123  
Tel: (505) 292-2700  
TWX: 910-989-0625

2150 So. 3rd. West  
Salt Lake City, Utah 84115  
Tel: (801) 487-8551  
TWX: 910-925-5686

**Cesco Electronics Ltd.**

98 Quest St. — Vallies G1K6W8  
Quebec  
Canada  
Tel: (418) 524-4641  
TWX: 011-285

24 Martin Ross Ave. M3J2K9  
Toronto, Ontario  
Canada  
Tel: (416) 661-0220  
TWX: 02-29697

1300 Carling Ave. K1Z7L2  
Ottawa, Ontario  
Canada  
Tel: (613) 729-5118  
TWX: 013-3584

4050 Jean Tolon H4P1W1  
Montreal, Quebec  
Canada  
Tel: (514) 735-5511  
TWX: 05-25590

**Schweber Electronics**

2724 Rena Road LHT3J9  
Mississauga, Ontario  
Canada  
Tel: (416) 678-9050  
TWX: 516-334-7474

**CENTRAL AREA****R. M. Electronics**

3323A Northridge Rd.  
Arlington Heights, Illinois 60004  
Tel: (312) 394-2050

4860 S. Division  
Kentwood, Michigan 49508  
Tel: (616) 531-9300  
TWX: 810-273-8779

**Sterling Electronics**

4613 Fairfield St.  
Metairie, Louisiana 70002  
Tel: (504) 887-7610  
TWX: 58328

4201 Southwest Freeway Dock 2  
Houston, Texas 77027  
Tel: (713) 627-9800  
TWX: 910-881-5041

2875 Merrell Rd.  
Dallas, Texas 75229  
Tel: (214) 357-9131  
TWX: 910-861-9159

**Arrow Electronics**

9700 Newton Ave. So.  
Bloomington, Minnesota 55431  
Tel: (612) 888-5522  
TWX: 910-576-3125

**Schweber Electronics**

23880 Commerce Park Rd.  
Buckwood, Ohio 44122  
Tel: (716) 461-4000  
No TWX — Use L. I.

**Component Specialties Inc.**

10907 Shady Trail  
Dallas, Texas 75220  
Tel: (214) 357-6511  
TWX: 910-861-4999

7313 Ashcroft No. 202  
Houston, Texas 77036  
Tel: (713) 771-7237  
TWX: 910-881-2422

**R. V. Weatherford**

10836 Grissom Lane, Suite 102  
Dallas, Texas 75229  
Tel: (214) 243-1571  
TWX: 910-860-5544

3500 WTC Jester  
Houston, Texas 77018  
Tel: (713) 688-7406  
TWX: 910-881-6222

**EASTERN AREA****Schweber Electronics**

Finance Dr.  
Commerce Industrial Park  
Danbury, Connecticut 06810  
Tel: (203) 792-3500  
TWX: 710-456-9405

2830 N. 28th Terrace  
Hollywood, Florida 33020  
Tel: (305) 927-0511  
TWX: 510-954-0304

4126 Pleasantdale Rd.  
Atlanta, Georgia 30340  
Tel: (404) 449-9170

5640 Fisher Lane  
Twinbrook Parkway  
Rockville, Maryland 20852  
Tel: (301) 881-3300  
TWX: 710-828-0536

213 — 3rd Ave.  
Waltham, Massachusetts 02154  
Tel: (617) 890-8484  
TWX: 710-324-1463

43 Blemond Dr.  
Somerset, New Jersey 08873  
Tel: (201) 469-6008  
TWX: 710-480-4733

Jericho Turnpike  
Westbury, L. I., New York 11590  
Tel: (516) 334-7474  
TWX: 510-222-3660

**Schweber Electronics Cont.**

2 Twon Line Circle  
 Rochester, New York 14623  
 Tel: (716) 461-4000  
 No TWX - Use L. I.

101 Rock Rd.  
 Horsham, Pennsylvania 19044  
 Tel: (215) 441-0600  
 No TWX

**Sterling Electronics**

20 Summer St.  
 Watertown, Massachusetts 02172  
 Tel: (617) 926-9720  
 TWX: 92-2453

774 Pfeiffer Blvd.  
 Perth Amboy, New Jersey 08861  
 Tel: (201) 442-8000  
 TWX: 138679

**Sterling Electronics Cont.**

1001 W. Broad St.  
 Richmond, Virginia 23220  
 Tel: (804) 359-0221  
 TWX: 827444

## Representatives

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**WESTERN AREA****Hecht, Henschen & Associates, Inc.**

P.O. Box 21166  
 Phoenix, Arizona 85036  
 Tel: (602) 275-4411  
 TWX: 910-951-0635

**Northwest Marketing Assoc.**

12835 Bellevue Redmond Road  
 Suite 203E  
 Bellevue, Washington 98005  
 Tel: (206) 455-5846  
 TWX: 910-443-2445

1337 North 7000 West  
 West Bountiful, Utah 84087  
 Tel: (801) 292-8991

**Hadden Associates**

7138 Convoy Court  
 San Diego, California 92111  
 Tel: (714) 565-9445  
 TWX: (910) 335-1569

**Lindberg Company**

6140 E. Evans Avenue  
 Denver, Colorado 80222  
 Tel: (303) 758-9033

**Thresum Associates, Inc.**

1901 Old Middlefield Way  
 Mountain View, California 94043  
 Tel: (415) 965-9180

**CENTRAL AREA****Beneke & McCaul**

Box 144  
 12825 Bristol  
 Grandview, Missouri 64030  
 Tel: (816) 765-2998

226 Cahmonix Ct.  
 St. Louis, Missouri 63141  
 Tel: (314) 434-6242

**Ammon & Rizos**

4255 LBJ Freeway  
 Suite 251  
 Dallas, Texas 75234  
 Tel: (214) 233-5591  
 TWX: 910-860-5137

**Ammon & Rizos Cont.**

3300 Chimney Rock  
 Suite 211  
 Houston, Texas 77056  
 Tel: (713) 781-6240  
 TWX: 910-881-6382

P.O. Box 12274  
 Oklahoma City, Oklahoma 73112  
 Tel: (405) 373-2748

**Technical Representatives, Inc.**

6515 E. 82nd Street  
 Suite No. 110  
 Indianapolis, Indiana 46250  
 Tel: (317) 849-6454  
 TWX: 810-260-1792

2118 Inwood Dr. Suite 102  
 Ft. Wayne, Indiana 46805  
 Tel: (219) 484-1432

**Oasis Sales, Inc.**

2250-K Landmeier  
 Elk Grove Village, Illinois 60007  
 Tel: (312) 640-1850

**S.A.I. Marketing Corporation**

9880 East Grand River Avenue  
 Brighton, Michigan 48116  
 Tel: (313) 227-1786

**Northstar Components**

3030 Harbor Lane  
 Plymouth, Minnesota 55441  
 Tel: (612) 553-1888

**EASTERN AREA****Can Tec**

41 Cloepatra Drive  
 Ottawa, Ontario  
 Canada K2G-0B6  
 Tel: (613) 225-0363

**Can Tec Cont.**

15432 Oakwood Street  
 Pierredonsa, Quebec  
 Canada H9Y 1Y2  
 Tel: (514) 620-3121

624 Elliot Crescent  
 Milton, Ontario  
 Canada L9T 3G4  
 Tel: (416) 624-9696

**Rep, Inc.**

1944 Cooledge Road  
 Tucker, Georgia 30084  
 Tel: (404) 938-4358  
 TWX: 810-766-4913

11527 So. Memorial Pkwy.  
 P.O. Box 4286  
 Huntsville, Alabama 35802  
 Tel: (205) 881-9270  
 TWX: 810-726-2102

7330 Chapel Hill Road  
 Suite 206A  
 Raleigh, North Carolina 27607  
 Tel: (919) 851-3007

**Coulbourn DeGrief, Inc.**

5205 East Drive  
 Baltimore, Maryland 21227  
 Tel: (301) 247-4646  
 TWX: 710-236-9011

**Masin-Esco, Inc.**

132 W. Greenbrook Road  
 North Caldwell, New Jersey 07006  
 Tel: (201) 226-2550

333 Jackson Avenue  
 Syosett, New York 11791  
 Tel: (516) 364-0310

**Advanced Components Corporation**

Box 276  
 North Syracuse, New York 13212  
 Tel: (315) 699-2671

# International Distributors and Representatives

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AMI Microsystems Europe has Distributors and Representatives in all major countries of Europe. Contact your nearest Sales Office (see page 1-2) for a current list of their names and addresses.

## Argentina

### S.I.E.S.A.

Avda. Roque Saenz  
Pena 1142 No - B  
Buenos Aires  
35-6784

## Australia

### CEMA Distributors Pty. Ltd.

G.P.O. Box 578  
Crows Nest, N.S.W. 2065  
439-4655

### Warburton Frank, Pty. Ltd.

199 Parramatta Road  
Auburn, N.S.W. 2144  
648-1771

## Austria

### Ing. Ernst Steiner

Geylinggasse 16  
A-1130 Wien  
822 674

## Belgium

### Ritro Electronics B.V.

Plantin en Moret us Lei  
B-2000 Antwerpen  
353 272

## Brazil

### Datatronix Electronica Ltda.

Av. Pacaembu, 746 - CONJ. 11  
Sao Paulo, Brazil  
209-0134

## Denmark

### Rifa Kontaktbureau

Vermundsgade 19  
DK-2100 Copenhagen  
Tel: 172-4511

## England

### Adrian Electronics Ltd.

28 High Street  
Winslow, Budkinghamshire  
MK 18 3HF  
Winslow 3535

### APEX Components, Ltd.

396 Bath Road, Slough  
Berkshire, England  
Burnham 63741

### Quarndon Ltd.

Slack Lane  
Derby DE3 3ED  
33-651

## Finland

### Atomica AB

P.O. Box 125  
SF-00121 Helsinki 12  
66 17 99

## France

### Electronique MS

89-93, Rue des Alpes  
Cidex L 180  
F-94533 Rungis  
686-7425

## PEP Produits Electroniques

### Professionnels S.A.R.L.

2-4 rue Barthelemy  
F-92120 Montrouge  
735 33 20

## Holland

### Ritro Electronics B.V.

Gelreweg 22  
Barneveld,  
Tel: 5041

## Greece

### Extant, Ltd.

53/55 Evelpidon Street  
Athens 812

## Hong Kong

### Shanklin Co. Ltd.

Rm 503-5 KAM Chung Bldg.  
54 Jaffe Road  
(05) 281-521-3

## India

### Radiosound

42, Canady Bridge  
Bombay 400 004  
353997

## Israel

### Tadiran Ltd. Microelectronics

P.O. Box 648  
Tel Aviv  
857 121

**Italy**

**Celdis Italiana S.p.A.**  
via Luigi Barzini 20  
1-20125, Milano  
68 06 81

**Japan**

**Matsushita Electric Trading Co. Ltd.**  
71, -Chome, Kawaramachi  
Higashi-ku  
Osaka, Japan

**Micro-Systems, Inc. (M.S.I.)**  
15-29, Mita 4-Chome  
Minato-ku  
Tokyo 108

**Taiyo Electric Company**  
Nakazawa Bldg. 53  
1-Chome-Yoyog  
Shibuya-ku, Tokyo

**Mexico**

**ROW International**  
10080 North Wolfe Road  
Cupertino, Ca. 95014  
(408) 446-1662

**Netherlands**

**RITRO Electronics B.V.**  
Gelreweg 22/P.O. 123  
Barneveld  
50 41

**New Zealand**

**David J. Reid (NZ) Ltd.**  
P.O. Box 2630  
Auckland 1, New Zealand  
492-139

**Norway**

**Rifa-Sverre Hoeyem A/5**  
Tolbodg 6  
Oslo 1, Norway  
Tel: 413755

**Republic of South Africa**

**Radiokom (Pty) Ltd.**  
P.O. Box 56310  
Pinegowrie 2123  
Johannesburg  
48-5712

**Tecnetics (Pty) Ltd.**  
Fernridge Centre  
H. Verword Drive  
Randburg 2001  
Johannesburg  
Tel: 48-6429

**Spain**

**Ataio Ingenieros S.A.**  
Enrique Larreta, 10 y 12  
Madrid 16,  
Tel: 215-3543

**Sweden**

**Rifa AB**  
FAck  
S-161 11 Bromma  
826-2600

**Switzerland**

**GED (Sales) S.A.**  
Muehlebachstr. 54  
CH-8008 Zuerich  
Tel: 472-850

**Taiwan**

**General Industries (Taiwan) Inc.**  
11th Floor, Room D  
Fortune Building  
52 Chang An E. Road Sec 2  
Taipei 104  
5221204

**West Germany**

**Omni-Ray GmbH**  
Ritzbruch 41 (Postfach 3175)  
D-4054 Nettetal 1  
02153/7691 (Tel)

**Mikrotec GmbH**  
Johannesstr. 91  
D-7000 Stuttgart 1  
Tel: 22 80 7

**Aktir Electronic GmbH**  
Leonorenstr. 49  
D-1000 Berlin 46  
Tel: 030/771-4408

**Ditronic GmbH**  
Im Asemwald 8/18  
D-7000 Stuttgart 70  
Tel: (0711) 724 844

**Ultratronik GmbH**  
Roseggerstrasse 12  
D-8031 Oberalting/Seefeld  
Tel: (08152) 7696

**Yugoslavia**

**ISKRA IEZE**  
TOZD Mikroelektronika  
Stegne 17  
61000 Ljubljana

# Ordering Information

Any product in this Guide to MOS Products can be ordered using the simple system described below. With this system, it is possible to completely specify any standard device in this catalog, in a manner that is compatible with AMI's order processing methods. The example below shows how this ordering system works and will help you to order your parts in a manner that can be expedited rapidly and accurately.

All orders (except those in sample quantities) are normally shipped in plastic carriers or aluminum tube containers, which

protect the devices from static electricity damage under all normal handling conditions. Either container is compatible with standard automatic IC handling equipment.

Any device described in this catalog is an AMI Standard Product. However, ROM devices that require mask preparation or programming to the requirements of a particular user, devices that must be tested to other than AMI Quality Assurance standard procedures, or other devices requiring special masks are sold on a negotiated price basis.

S 6 8 1 0 A - 1 P

Device Number — prefix S, followed by four numeric digits that define the basic device type. If there are versions to the basic device, the four numeric digits will be followed by additional alphanumeric digits, in this example A-1. The last digit should always be followed by a space.

Package Type — a single letter designation which identifies the basic package type. The letters are coded as follows:

- P — Plastic package
- E — Cer-DIP package
- S — SLAM package
- C — Ceramic (three-layer) package
- T — TO type package

*(See page 1-11 for envelope drawings of all packages.)*

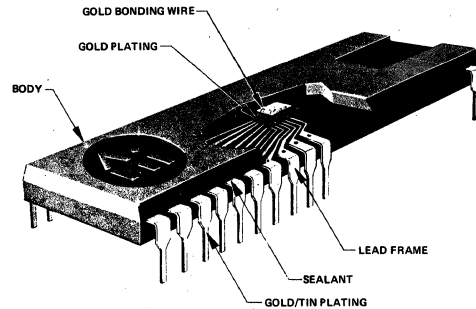
# Packages

## PLASTIC PACKAGE

The AMI plastic dual-in-line package is the equivalent of the widely accepted industry standard, refined by AMI for MOS/LSI applications. The package consists of a silicone body, transfer-molded directly onto the assembled lead frame and die. The lead frame is Kovar or Alloy 42, with external pins tin plated. Internally, there is a 50  $\mu\text{m}$ . gold spot on each die attach pad and on bonding fingertips. Gold bonding wire is attached with thermocompression gold ball bonding technique.

Materials of the lead frame, the package body, and the die attach are all closely matched in thermal expansion coefficients, to provide optimum response to various thermal conditions. During manufacture every step of the process is rigorously monitored to assure maximum quality of the AMI plastic package.

Available in: 8, 14, 16, 18, 22, 24, 28 and 40 pin configurations.

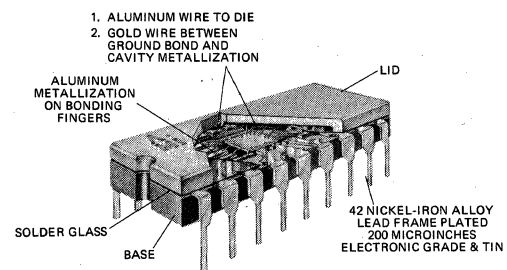


## Cer-DIP PACKAGE

The Cer-DIP dual-in-line package has the same high performance characteristics as the standard three-layer ceramic package, yet approaches plastic in cost. It is a military approved type package, with excellent reliability characteristics. Although the Cer-DIP concept has been around for a number of years, AMI leads the technology with this package, having eliminated the device instability and corrosion problems of earlier Cer-DIP processes.

The package consists of an Alumina ( $\text{Al}_2\text{O}_3$ ) base and the same material lid, hermetically fused onto the base with low temperature solder glass (at approximately 475°C). Inert gasses are sealed inside the die cavity.

Available in: 16, 18, 22, 24, and 28 pin configurations.



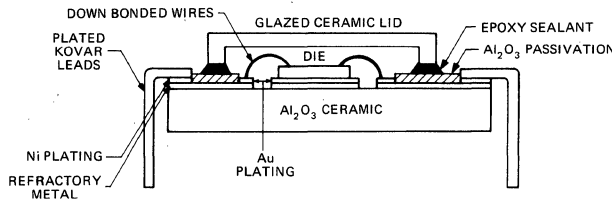
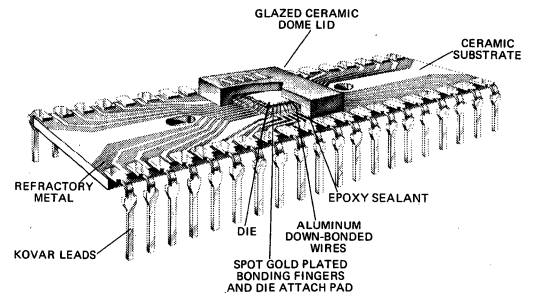


## SLAM PACKAGE

The SLAM (single layer metallization) dual-in-line package is an AMI innovation that offers a lower cost alternative to three-layer ceramic packages, without sacrifice of performance or reliability.

The SLAM package uses the same basic materials as ceramic, but is constructed in a simpler and thereby more reliable manner. It uses a 96% Alumina base, one basic refractory metallization layer, coated with an Alumina passivation layer, and brazed-on Kovar leads. The leads are suitable for either socket insertion or soldering. Either a glazed ceramic or a Kovar lid is used to hermetically seal the package. The glazed ceramic lid is attached with an epoxy resin sealant, but a gold-silicon eutectic solder is used for Kovar lids.

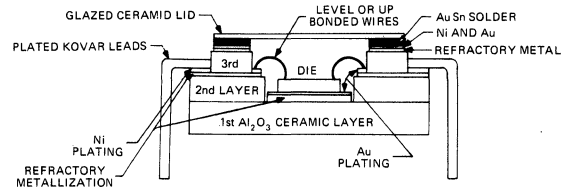
Available in: various 14 to 40 pin configurations.



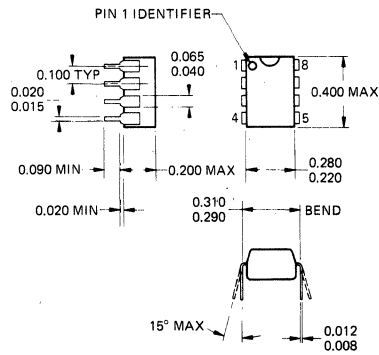
**EPOXY SEAL PACKAGE**

## CERAMIC PACKAGE

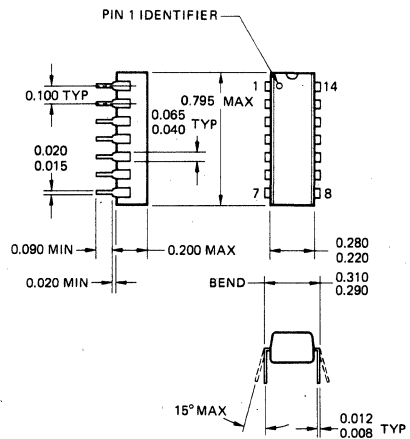
Industry standard high performance, high reliability package, made of three layers of Al<sub>2</sub>O<sub>3</sub> ceramic and nickel-plated refractory metal. The cavity is sealed with a glazed ceramic lid, using a controlled devitrified low temperature glass sealant. Package leads are of Kovar, nickel-plated and solder dipped for socket insertion or soldering.



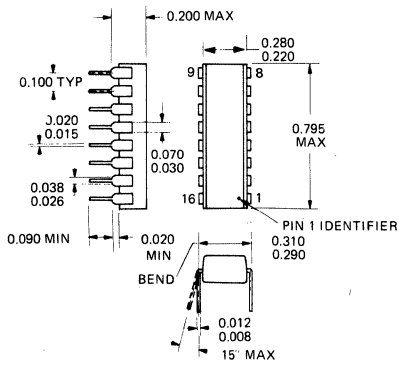
8-PIN PLASTIC



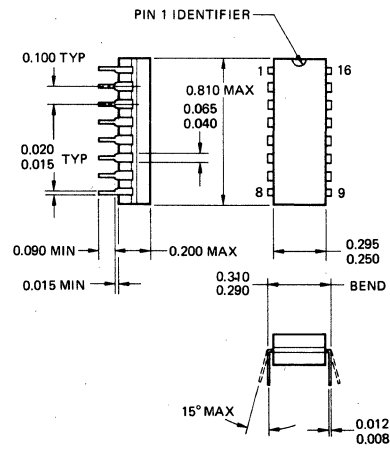
14-PIN PLASTIC



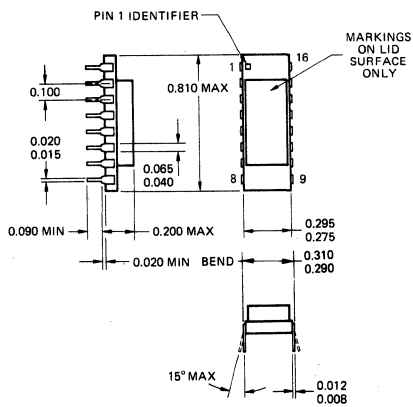
16-PIN PLASTIC



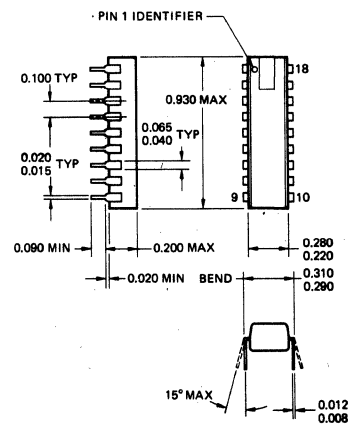
16-PIN Cer-DIP



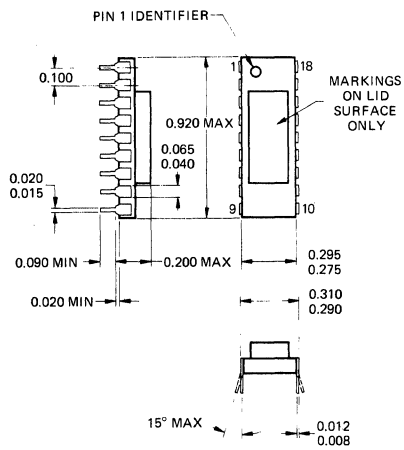
16-PIN CERAMIC



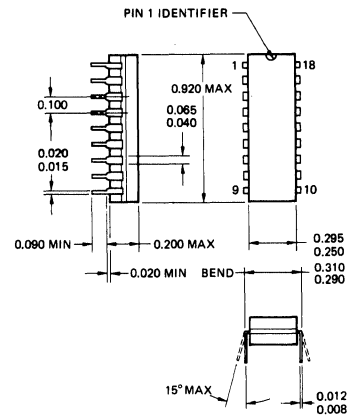
18-PIN PLASTIC



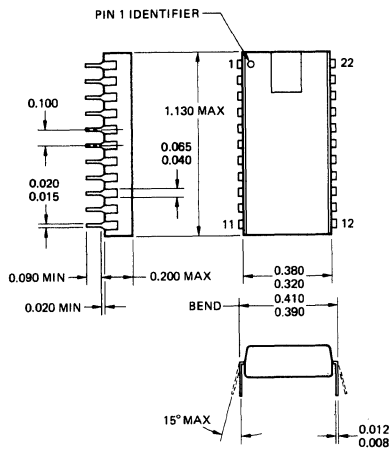
### 18-PIN CERAMIC



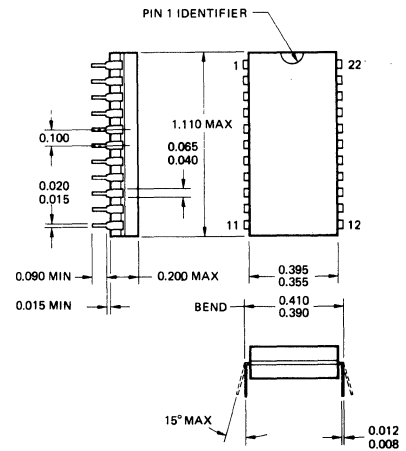
### 18-PIN Cer-DIP



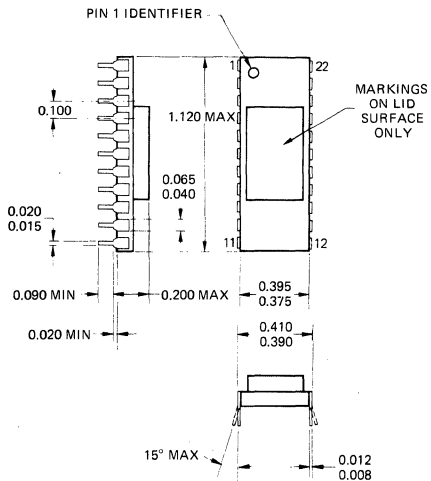
### 22-PIN PLASTIC



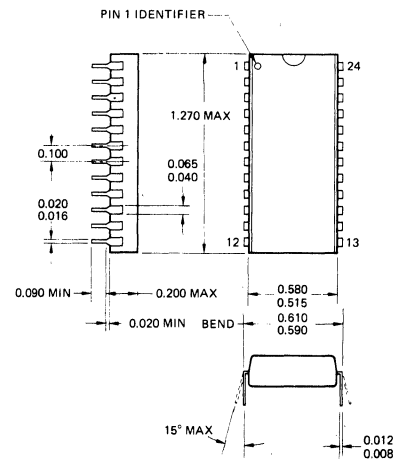
### 22-PIN Cer-DIP



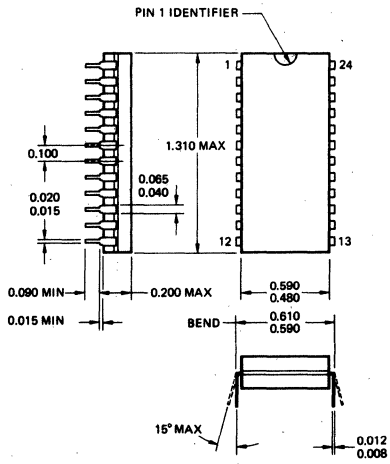
### 22-PIN CERAMIC



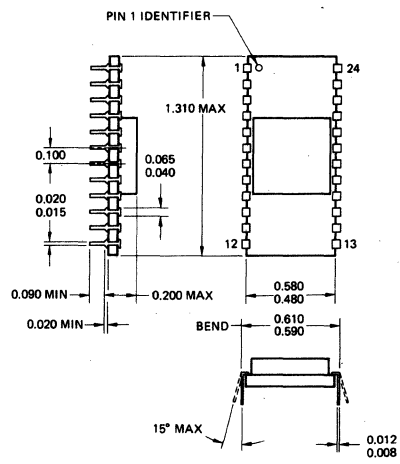
### 24-PIN PLASTIC



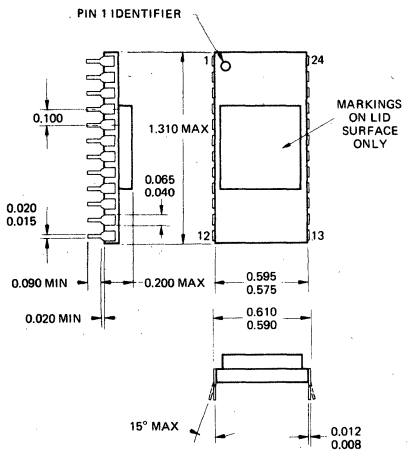
24-PIN Cer-DIP



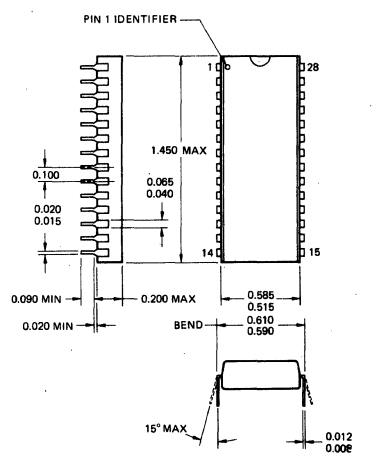
24-PIN SLAM



24-PIN CERAMIC

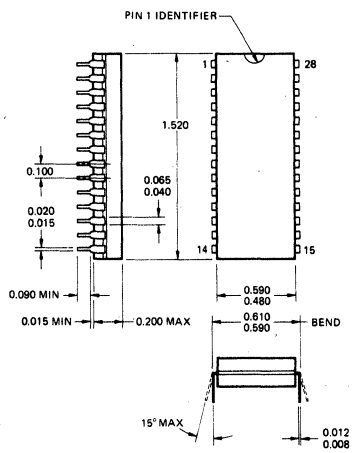


28-PIN PLASTIC

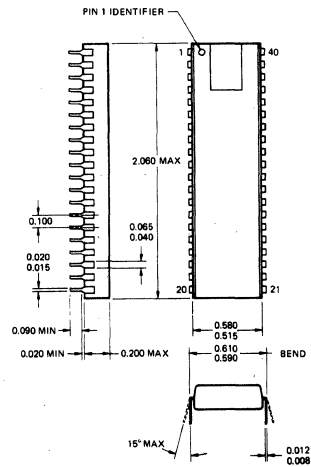


87686

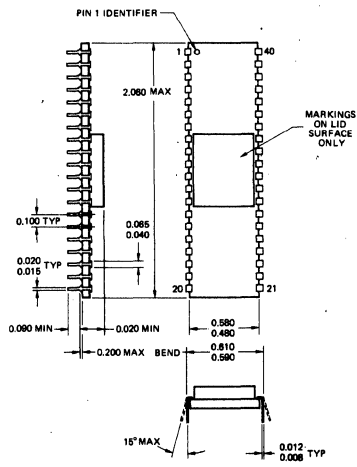
28-PIN Cer-DIP



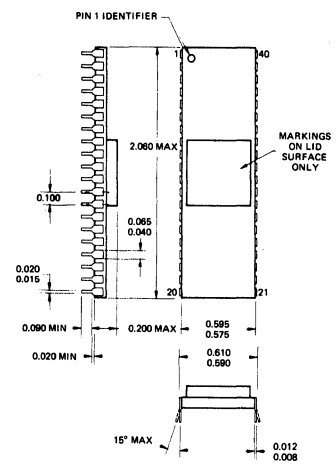
40-PIN PLASTIC



### 40-PIN SLAM



### 40-PIN CERAMIC



# AMERICAN MICROSYSTEMS, INC.

## TERMS OF SALE

1. **ACCEPTANCE:** THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items described above and acknowledged hereby are firm and not subject to audit, price revision, or price redetermination.
2. **PAYMENT:**
  - (a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.
  - (b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.
  - (c) Each shipment shall be considered a separate and independent transaction, and payment therefor shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.
3. **TAXES:** Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority, (national, state, local or other) applicable to the products covered by this order, or the manufacturer or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.
4. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, Railway Express, Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.
5. **DELIVERY:** Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lock-outs, slow-downs, shortages, factory or labor conditions, errors in manufacture, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.
6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS
7. **INSPECTION:** Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.
8. **WARRANTY:** The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.
9. **GENERAL:**
  - (a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.
  - (b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.
  - (c) In no event shall Seller be liable for consequential or special damages.
  - (d) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.
  - (e) Except to the extent provided in Paragraph 10, below, this order is not subject to cancellation or termination for convenience.
  - (f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities, domestic or foreign.
  - (g) In the event that the cost of the products are increased as a result of increases in materials, labor costs, or duties, Seller may raise the price of the products to cover the cost increases.
  - (h) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.
10. **GOVERNMENT CONTRACT PROVISIONS:** If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Armed Services Procurement Regulation are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be - i.e., "Contracting Officer" shall mean "Buyer", "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Rhodesia and Certain Communist Areas; 7-103.16, Contract Work Hours and Safety Standards Act - Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity Clause; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government (only to the extent that Buyer's contract is terminated for the convenience of the government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-103.24, Responsibility for Inspection; 7-103.25, Commercial Bills of Lading Covering Shipments Under FOB Origin Contracts; 7-103.27, Listing of Employment Openings; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.15, Examination of Records by Comptroller General; 7-104.20, Utilization of Labor Surplus Area Concerns.

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**Memories**

## RAMs

Part No.	Organization	T <sub>Acc</sub> (ns)	R/W T <sub>Cycle</sub> (ns)	Operating Power (mW)	Standby Power (mW)	Supplies (V)	I/O	Clocks	Process	Packages	
S2222	512 x 1 Static	200	470	7.5	0.002	+10	MOS	0	} CMOS	P,E	
S2222A	512 x 1 Static	400	940	7.5	0.01	+10	MOS	0		SiGate	P,E
S1103	1024 x 1 Dynamic	310	580	450	—	+16, +19	MOS/Sense A.	3	} CMOS SiGate	P,E	
S146	1024 x 1 Dynamic	210	390	550	—	+19, +22	MOS/Sense A.	3		P-SiGate	P,E
S1103-1	1024 x 1 Dynamic	180	360	550	—	+19, +22	MOS/Sense A.	3		P-SiGate	P,E
S1103X	1024 x 1 Dynamic	120	270	550	—	+19, +22	MOS/Sense A.	3		P-SiGate	P,E
S1103A	1024 x 1 Dynamic	205	580	425	2.0	+16, +19	MOS/Sense A.	2		P-SiGate	P,E
S1103A-1	1024 x 1 Dynamic	145	340	660	0.2	+19, +22	MOS/Sense A.	2		P-SiGate	P,E
S1103A-X	1024 x 1 Dynamic	125	285	660	0.2	+19, +22	MOS/Sense A.	2		P-SiGate	P,E
S4006	1024 x 1 QuasiStat	400	650	450	50	-12, +5	TTL	0		P-I <sup>2</sup>	E,C
S4008	1024 x 1 QuasiStat	500	900	450	50	-12, +5	TTL	0		P-I <sup>2</sup>	E,C
S4008-9	1024 x 1 QuasiStat	800	1000	450	50	-12, +5	TTL	0		P-I <sup>2</sup>	E,C
S4015	1024 x 1 Static	95	120	500	—	+5	TTL/Open C.	2		N-SiGate	E
S4015-2	1024 x 1 Static	70	90	625	—	+5	TTL/Open C.	2		N-SiGate	E
S4025	1024 x 1 Static	95	120	500	—	+5	TTL/3-State	2		N-SiGate	E
S4025-2	1024 x 1 Static	70	90	625	—	+5	TTL/3-State	2		N-SiGate	E
S5101	256 x 4 Static	650	650	110	0.05	+5	TTL/3-State	4		} CMOS SiGate	P,E,C
S5101-1	256 x 4 Static	450	450	110	0.05	+5	TTL/3-State	4			P,E,C
S5101-2	256 x 4 Static	450	450	110	0.7	+5	TTL/3-State	4	P,E,C		
S5101-3	256 x 4 Static	650	650	110	0.7	+5	TTL/3-State	4	P,E,C		
S5101-8	256 x 4 Static	800	800	110	2.5	+5	TTL/3-State	4	P,E,C		
S5101L	256 x 4 Static	650	650	110	0.05	+5	TTL/3-State	4	P,E,C		
S5101L-1	256 x 4 Static	450	450	110	0.05	+5	TTL/3-State	4	P,E,C		
S5101L-2	256 x 4 Static	450	450	110	0.7	+5	TTL/3-State	4	P,E,C		
S5101L-3	256 x 4 Static	650	650	110	0.7	+5	TTL/3-State	4	P,E,C		
S6508	1024 x 1 Static	460	730	50	0.5	+5	TTL	2	CMOS		E,C
S6508A	1024 x 1 Static	300	465	50	0.5	+5	TTL	2	CMOS	E,C	
S6810	128 x 8 Static	1000	1000	650	N/A	+5	TTL	0	N-SiGate	P,E,S	
S6810-1	128 x 8 Static	575	575	650	N/A	+5	TTL	0	N-SiGate	P,E,S	
S6810A	128 x 8 Static	450	450	350	N/A	+5	TTL	0	N-SiGate	P,E,S	
S6810A-1	128 x 8 Static	350	350	400	N/A	+5	TTL	0	N-SiGate	P,E,S	

## ROMs/PROMs

Part No.	Description	Organization	Max. Power Dissip. (mW)	Supplies (V)	Max. Access Time	Process	Packages
S3514	4096 Bit Static ROM	512 x 8	500	+5,-12	1 $\mu$ s	P-I <sup>2</sup>	P,E
S5204A	4096 Bit Static EPROM	512 x 8	750	+5,-12	750 ns	P-SiGate	C
S5232	4096 Bit Static ROM	512 x 8 or 1024 x 4	500	+5,-12	1 $\mu$ s	P-I <sup>2</sup>	P,E
S8564	9 x 7 Charac. Gen./ROM	64 Word	1100	+5,-12	450 ns	P-I <sup>2</sup>	P,E
S8771	5120 Bit ROM	512 x 10	1000	+5,-12	450 ns	P-I <sup>2</sup>	P,E
S8865	8192 Bit ROM	2048 x 4	635	+5,-12	1.3 $\mu$ s	P-I <sup>2</sup>	P,E
S8996	16,384 Bit ROM	4096 x 4	368	+5,-12	1.8 $\mu$ s	P-I <sup>2</sup>	P,E
S9996	16,384 Bit ROM	2048 x 8	368	+5,-12	1.8 $\mu$ s	P-I <sup>2</sup>	P,E
S6830	8192 Bit Static ROM	1024 x 8	650	+5	575 ns	N-SiGate	P,E
S6831	16,384 Bit Static ROM	2048 x 8	150	+5	450 ns	N-SiGate	C
S6834	4096 Bit Static EPROM	512 x 8	750	+5,-12	575 ns	P-SiGate	C
S6834-1	4096 Bit Static EPROM	512 x 8	750	+5,-12	750 ns	P-SiGate	C

Note: All ROMs are mask-programmable for custom patterns to meet your requirements.

## Future Products

**RAM** — 1024 x 1 bit High Speed (60/45 ns), VMOS, 16 pins

**RAM** — 1024 x 4 bit Static, VMOS

**RAM (S6518)** — 1024 x 1 bit Static CMOS, 18 pins

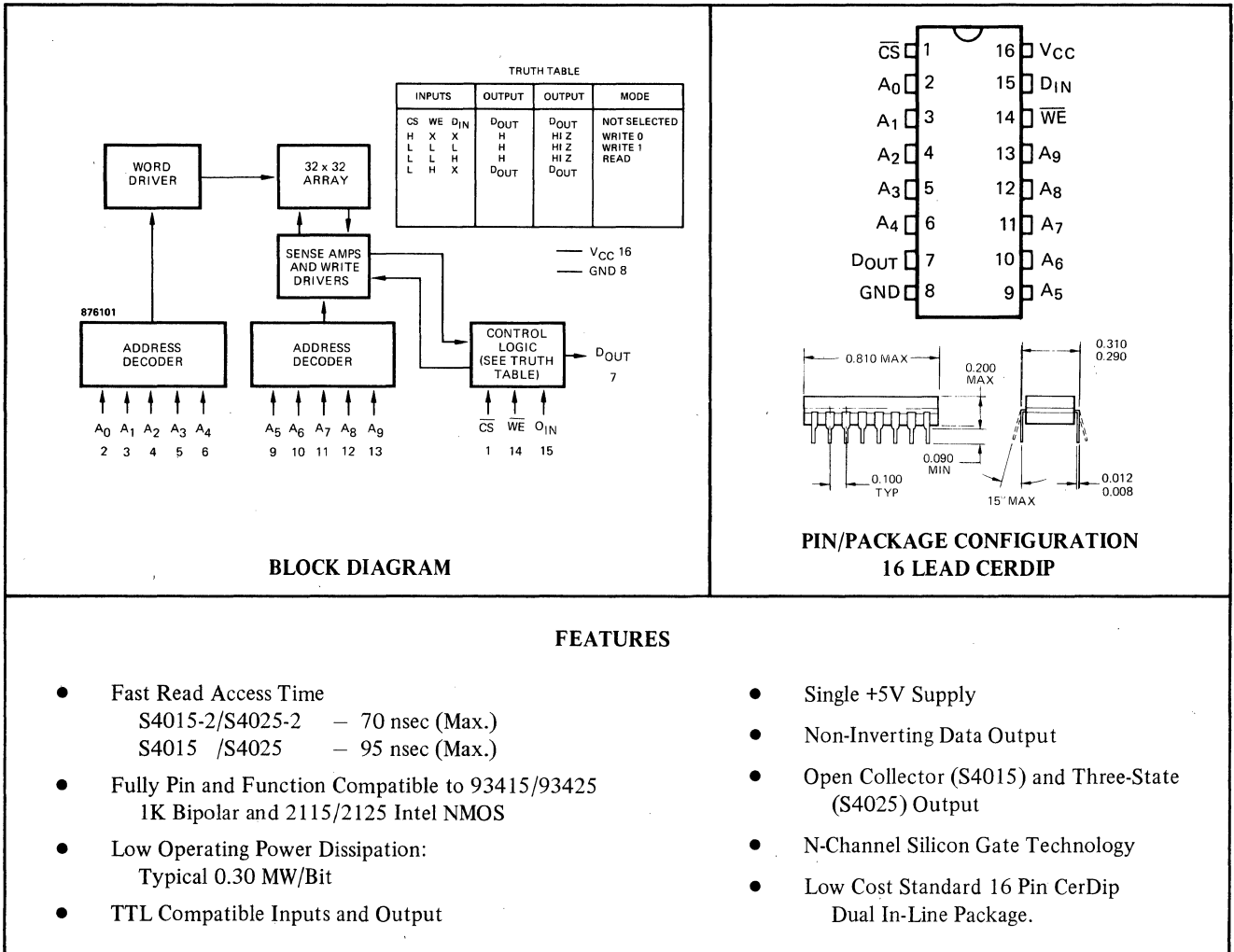
**RAM** — 1024 x 4 bit Static N-Channel depletion load

**RAM** — 4096 x 1 bit Static, N-Channel depletion load

**ROM** — 2048 x 8 bit High Speed (less than 200 ns) N-Channel



### ADVANCED PRODUCT DESCRIPTION



### FUNCTIONAL DESCRIPTION

The AMI S4015 and S4025 are a family of 1024 words by 1 bit fully decoded static Random Access Memories. These RAMs are designed for buffer and control storage and high performance, main memory applications. They are fully compatible with TTL logic families in all respects: inputs, outputs, and single +5V supply. Both open collector (S4015) and three-state output (S4025) are available.

### TYPICAL APPLICATIONS

Buffer, Cache, Mainframe Memory, Control Storage, Add-On Memory, Etc.

The S4015 and S4025 family is fabricated with N-Channel MOS silicon gate process. The design takes advantage of depletion load transistors to achieve higher speed. The simple design and process allows the production of high speed MOS RAMs which are compatible to the performance of Bipolar RAMs, but offering the advantages of lower power dissipation and cost.

**Absolute Maximum Ratings\***

Temperature Under Bias .....	-10°C to +85°C
Storage Temperature .....	-65°C to +150°C
All Output or Supply Voltages .....	-0.5 to +7 Volts
All Input Voltages .....	-0.5 to +5.5 Volts
D.C. Output Current .....	20mA

**\*Comment:**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. Characteristics [1]**  $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $75^\circ C$

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
$V_{OL1}$	S4015-2 Output Low Voltage			0.45	V	$I_{OL} = 16mA$
$V_{OL2}$	S4015 Output Low Voltage			0.45	V	$I_{OL} = 12mA$
$V_{OL3}$	S4025 Family Output Low Voltage			0.45	V	$I_{OL} = 7mA$
$V_{IH}$	Input High Voltage	2.1			V	
$V_{IL}$	Input Low Voltage			0.8	V	
$I_{IL}$	Input Low Current		-1	-40	$\mu A$	$V_{CC} = Max., V_{IN} = 0.4V$
$I_{IH}$	Input High Current		1	40	$\mu A$	$V_{CC} = Max., V_{IN} = 4.5V$
$I_{CEX}$	S4015 Family Output Leakage Current		10	100	$\mu A$	$V_{CC} = Max., V_{OUT} = 4.5V$
$ I_{OFF} $	S4025 Family Output Current (High Z)		10	50	$\mu A$	$V_{CC} = Max., V_{OUT} = 0.5V/2.4V$
$I_{OS} [2]$	S4025 Family Current Short Circuit to Ground			-100	mA	$V_{CC} = 4.5V$
$V_{OH}$	S4025 Family Output High Voltage	2.4			V	$I_{OH} = -3.2mA$
$I_{CC1}$	S4015, S4025, Power Supply Current		60	100	mA	All Inputs Grounded, Output Open
$I_{CC2}$	S4015-2, S4025-2, Power Supply Current		100	125	mA	All Inputs Grounded, Output Open

NOTES: 1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:

$$\begin{aligned} \theta_{JA} (@ 400 \text{ f}_{PM} \text{ air flow}) &= 45^\circ C/W \\ \theta_{JA} (\text{still air}) &= 60^\circ C/W \\ \theta_{JC} &= 25^\circ C/W \end{aligned}$$

2. Duration of short circuit current should not exceed 1 second.

**TRUTH TABLE**

Inputs			Output S4015 Family	Output S4025 Family	Mode
CS	WE	$D_{IN}$	$D_{OUT}$	$D_{OUT}$	
H	X	X	H	High Z	Not Selected
L	L	L	H	High	Write "0"
L	L	H	H	High	Write "1"
L	H	X	$D_{OUT}$	$D_{OUT}$	Read

S4015 Family A.C. Characteristics <sup>[1]</sup>  $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $75^\circ C$

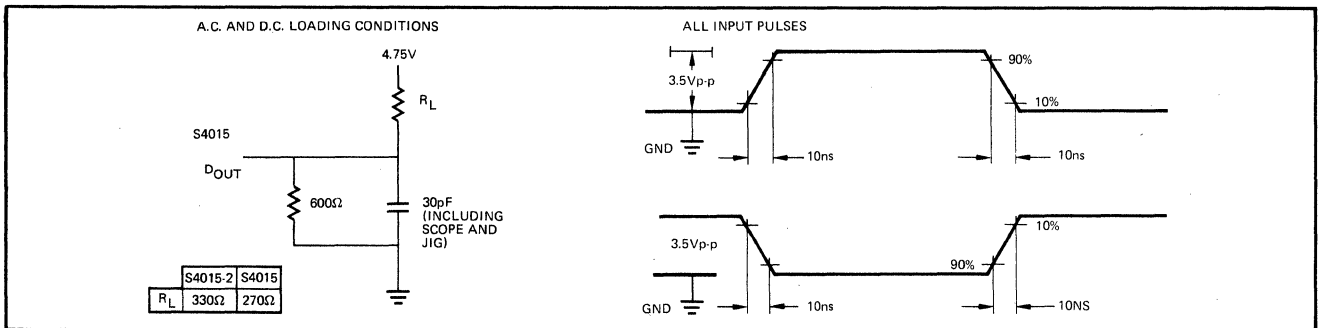
### READ CYCLE

Symbol	Test	S4015-2 Limits		S4015 Limits		Units
		Min.	Typ. Max.	Min.	Typ. Max.	
$t_{ACS}$	Chip Select Time	5	40	5	45	ns
$t_{RCS}$	Chip Select Recovery Time		40		40	ns
$t_{AA}$	Address Access Time	60	70	75	95	ns
$t_{OH}$	Previous Read Data Valid After Change of Address	10		10		ns

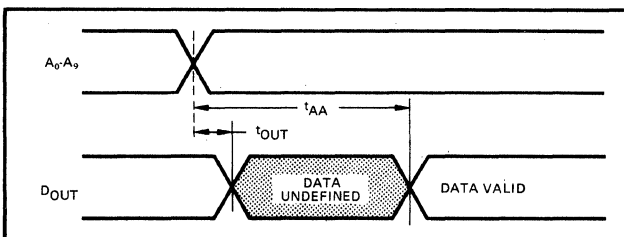
### WRITE CYCLE

Symbol	Test	S4015-2 Limits			S4015 Limits			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{WS}$	Write Enable Time			40			40	ns
$t_{WR}$	Write Recovery Time	5		45	5		45	ns
$t_W$	Write Pulse Width	50			50			ns
$t_{WSD}$	Data Set-Up Time Prior to Write	5			5			ns
$t_{WHD}$	Data Hold Time after Write	5			5			ns
$t_{WSA}$	Address Set-Up Time	15			30			ns
$t_{WHA}$	Address Hold Time	5			5			ns
$t_{WSCS}$	Chip Select Set-Up Time	5			5			ns
$t_{WHCS}$	Chip Select Hold Time	5			5			ns

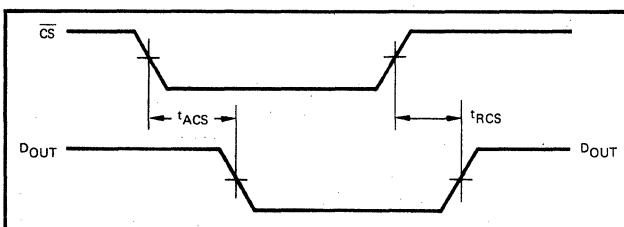
### TEST CONDITIONS



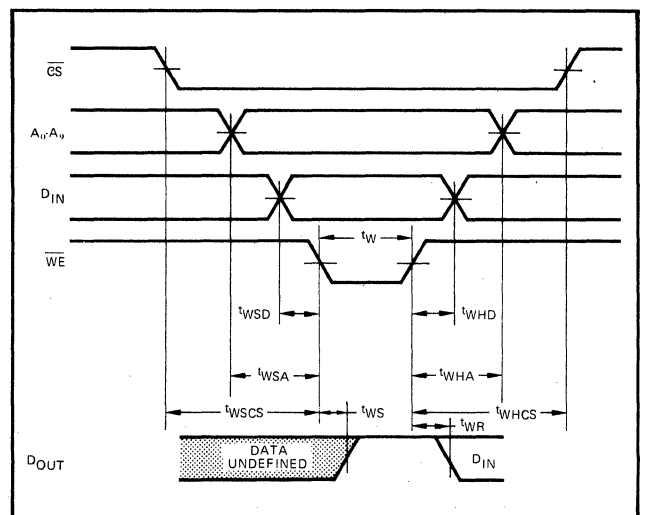
### READ CYCLE



### PROPAGATION DELAY FROM CHIP SELECT



### WRITE CYCLE



**S4025 Family A.C. Characteristics [1]**  $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $75^\circ C$

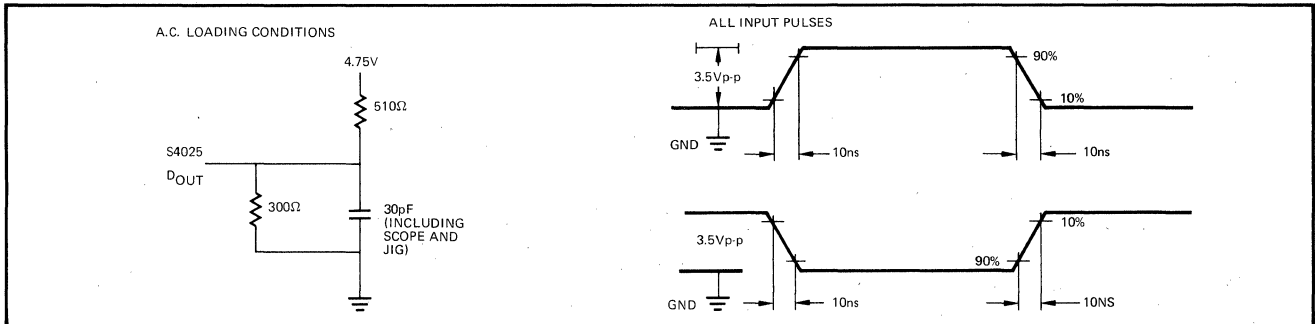
**READ CYCLE**

Symbol	Test	S4025-2 Limits		S4025 Limits		Units
		Min.	Typ. Max.	Min.	Typ. Max.	
$t_{ACS}$	Chip Select Time	5	40	5	45	ns
$t_{ZRCS}$	Chip Select to HIGH Z		40		40	ns
$t_{AA}$	Address Access Time		60 70		75 95	ns
$t_{OH}$	Previous Read Data Valid after Change of Address	10		10		ns

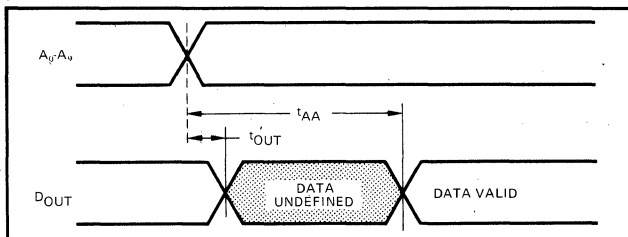
**WRITE CYCLE**

Symbol	Test	S4025-2 Limits			S4025 Limits			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{ZWS}$	Write Enable to HIGH Z			40			40	ns
$t_{WR}$	Write Recovery Time	5		45	5		45	ns
$t_W$	Write Pulse Width	50			50			ns
$t_{WSD}$	Data Set-Up Time Prior to Write	5			5			ns
$t_{WHD}$	Data Hold Time After Write	5			5			ns
$t_{WSA}$	Address Set Up Time	15			30			ns
$t_{WHA}$	Address Hold Time	5			5			ns
$t_{WSCS}$	Chip Select Set-Up Time	5			5			ns
$t_{WHCS}$	Chip Select Hold Time	5			5			ns

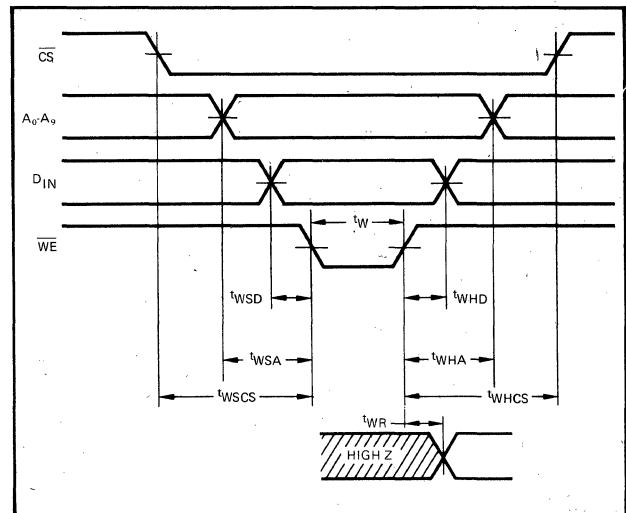
**TEST CONDITIONS**



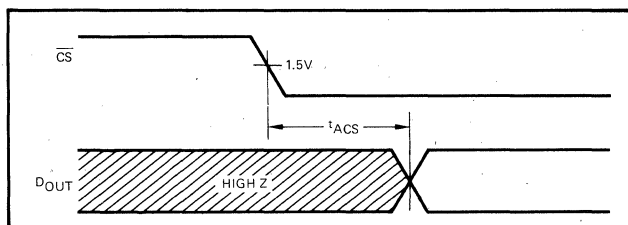
**READ CYCLE**



**WRITE CYCLE**

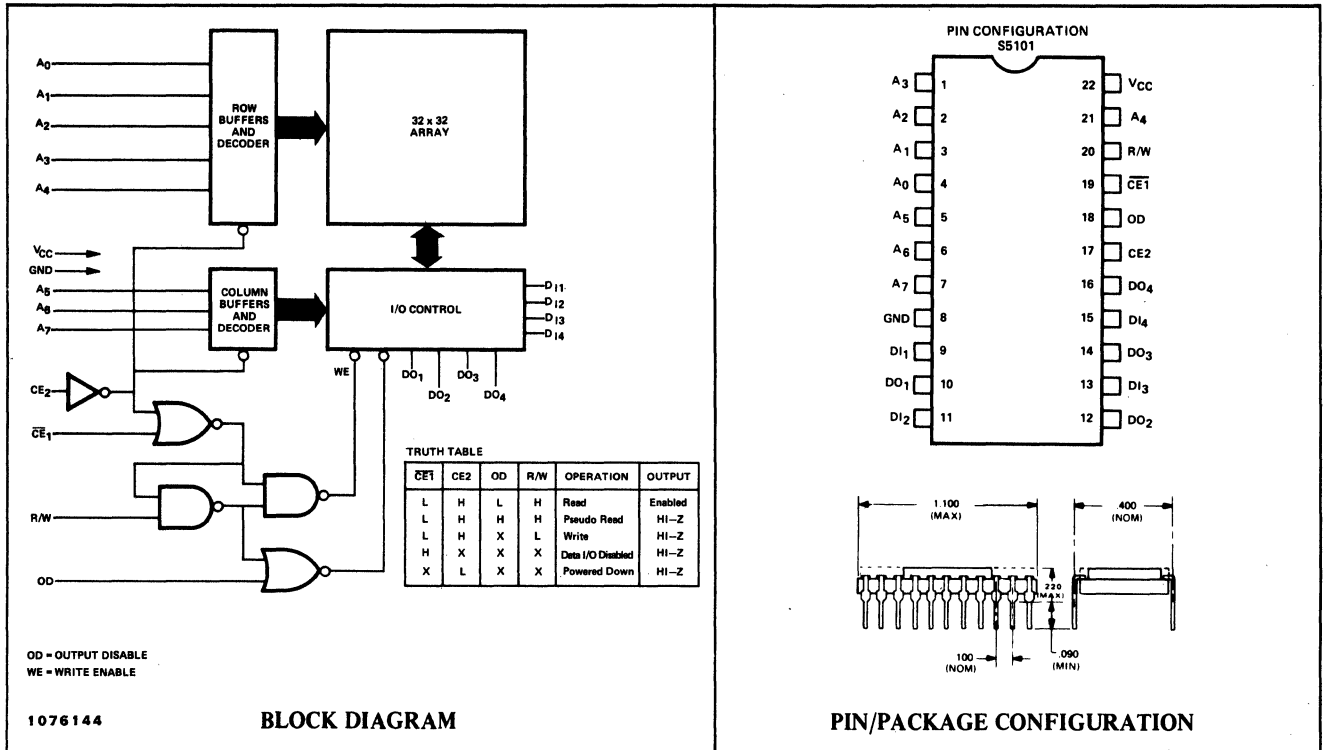


**PROPAGATION DELAY FROM CHIP SELECT**



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

## ADVANCED PRODUCT DESCRIPTION



## FEATURES

- Ultra Low Standby Power – 50 Nanowatt/Bit Maximum
- Fast Access Time: 450 nsec Maximum
- Static – No Refresh
- Single +5 Volt Power Supply
- Completely TTL Compatible – All Inputs and Outputs
- Data Retention at 2.0V
- Pin Compatible, Industry Standard
- Low Power Replacement for N-Channel Static 2101
- Three State Output
- Common or Separate I/O
- 22 Pin Dual In-Line Package

## FUNCTIONAL DESCRIPTION

The AMI S5101 family of 256 x 4 bit high speed CMOS RAMs offers ultra low power and fully static operation with a single 5 volt power supply. With data inputs and outputs on adjacent pins, either separate or common data I/O applications can be easily selected for maximum design flexibility. The very low power of these RAMs makes them an ideal choice where battery augmented non-volatile RAM storage is mandatory.

The S5101 family is totally static, making clocking unnecessary for a new address to be accepted. The stored data is read out nondestructively and in the same polarity as the

original input data. The outputs are disabled with output disable (O.D.), either ( $\overline{CE}_1$ ) or  $\overline{CE}_2$ , or during a write cycle ( $R/W = \text{LOW}$ ). The read/write input or output disable input allows these RAMs to be used in common data I/O systems by forcing the output into a high impedance state during a write operation.

When deselected, the S5101 and S5101-3 draw only 10 microamps and 140 microamps, respectively, from the 5 volt supply. The S5101L and S5101L-3 are identical to the S5101 and S5101-3, respectively, with the additional feature of guaranteed data retention at a power supply voltage as low as 2.0 volts.

**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias	0°C to 70°C	Maximum Power Supply Voltage	+11V
Storage Temperature	- 65°C to + 150°C	Power Dissipation	1 Watt
Voltage on Any Pin with Respect to Ground	- 0.3V to V <sub>CC</sub> + 1.0V		

**\*COMMENT:** Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. CHARACTERISTICS** T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 5V ± 5% (Unless otherwise specified)

SYMBOL	PARAMETER	LIMIT		UNITS	TEST CONDITIONS
		MIN.	MAX.		
I <sub>LI</sub>	Input Leakage Current		1	μA	V <sub>IN</sub> = 0V to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		1	μA	$\overline{CE}_1 = V_{IH}$ CE <sub>2</sub> = V <sub>IN</sub> V <sub>OUT</sub> = 0V or V <sub>CC</sub>
I <sub>CC</sub>	Operating Supply Current		22	mA	Outputs = Open, V <sub>IN</sub> = V <sub>IL</sub> to V <sub>CC</sub>
I <sub>CCL</sub>	Standby Supply Current S5101 S5101-3		10 140	μA μA	V <sub>IN</sub> = 0V to V <sub>CC</sub> except CE <sub>2</sub> ≤ 0.2V
V <sub>IL</sub>	Input Low Voltage	- 0.3	0.65	V	
V <sub>IH</sub>	Input High Voltage	2.2	V <sub>CC</sub>	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = - 1 mA

**LOW V<sub>CC</sub>[1] DATA RETENTION CHARACTERISTICS FOR S5101L, S5101L-3** T<sub>A</sub> = 0°C to 70°C

SYMBOL	PARAMETER	LIMIT		UNITS	TEST CONDITIONS
		MIN.	MAX.		
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	2.0		V	CE <sub>2</sub> ≤ 0.2V
I <sub>CCDR</sub>	Data Retention Supply Current S5101L S5101L-3		2 30	μA μA	V <sub>CC</sub> = V <sub>DR</sub> t <sub>R</sub> = t <sub>F</sub> = 20 ns
t <sub>CDR</sub>	Chip Deselect to Data Retention Time	0		ns	
t <sub>R</sub>	Operation Recovery Time	t <sub>RC</sub> [2]		ns	

**NOTES:** [1] For guaranteed low V<sub>CC</sub> Data Retention @ 2.0V, order should include S5101L or S5101L-3 Numbers.  
 [2] t<sub>RC</sub> = Read Cycle Time.

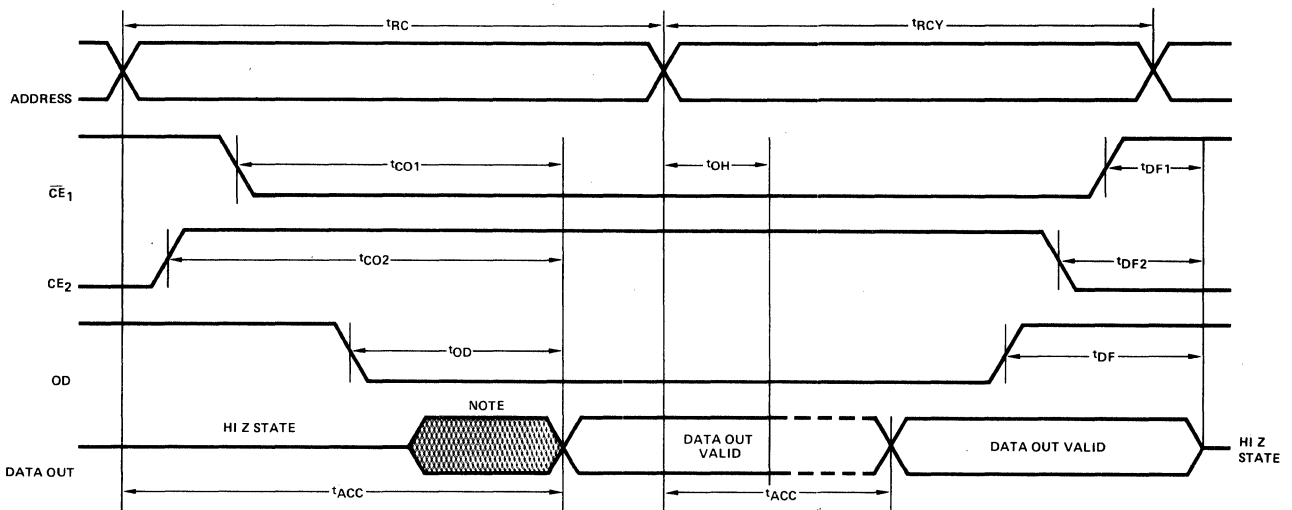
## A.C. CHARACTERISTICS

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$  (Unless otherwise specified)

### READ CYCLE

SYMBOL	PARAMETER	S5101-1 & S5101L-1 LIMITS		S5101, S5101L S5101-3, S5101L-3 LIMITS		S5101-8 LIMITS		UNITS	COMMENTS
		MIN	MAX	MIN	MAX	MIN	MAX		
$T_{RC}$	Read Cycle Time	450		650		800		ns	SEE A.C. CONDITIONS OF TEST AND A.C. TEST LOAD
$T_{ACC}$	Access Time		450		650		800	ns	
$T_{CO1}$	CE1 to Output Delay		420		600		800	ns	
$T_{CO2}$	CE2 to Output Delay		500		700		900	ns	
$T_{OD}$	Output Disable to Enabled Output Delay		300		350		500	ns	
$T_{DF}$	Output Disable To Output HI-Z Stage Delay	30		50		50		ns	
$T_{DF1}$	CE1 To Output HI-Z Delay	30		50		50		ns	
$T_{DF2}$	CE2 To Output HI-Z Delay	30		50		50		ns	
$T_{OH}$	Output Data Valid Into Next Cycle	30		50		50		ns	

### READ CYCLE



NOTE: THE INDETERMINATE STATE OF THE OUTPUT WILL OCCUR FOR SOME TIME PERIOD BETWEEN  $t_{OH}$  AND THE FULL DURATION OF  $t_{CO1}$ , AFTER BOTH OD AND CE1 HAVE GONE LOW.

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**A.C. CHARACTERISTICS FOR WRITE CYCLE – SEPARATE OR COMMON DATA I/O USING OUTPUT DISABLE**

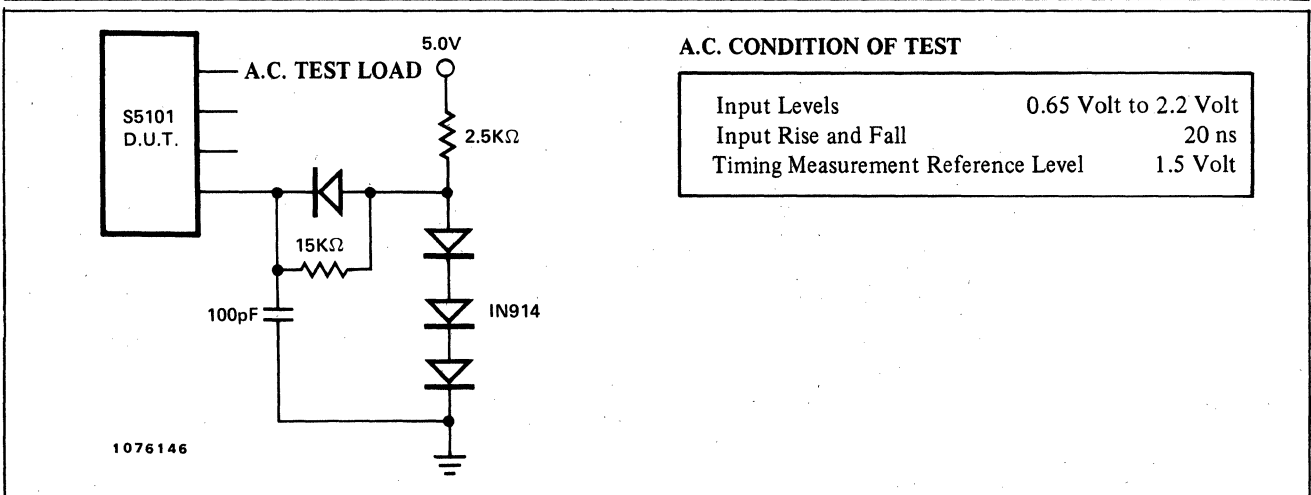
$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 5\%$  (Unless otherwise specified)

**WRITE CYCLE**

SYMBOL	PARAMETER	S5101-1 & S5101L-1 LIMITS		S5101, S5101L S5101-3, S5101L-3 LIMITS		S5101-8 LIMITS		UNITS	COMMENTS
		MIN	MAX	MIN	MAX	MIN	MAX		
$T_{WC}$	Write Cycle Time	450		650		800		ns	SEE A.C. CONDITIONS OF TEST AND A.C. TEST LOAD
$T_{AW}$	Address To Write Delay	130		150		200		ns	
$T_{CW1}$	CE1 to Write Delay	400		550		800		ns	
$T_{CW2}$	CE2 to Write Delay	400		550		800		ns	
$T_{DW}$	Data Set-Up to End of Write Time	250		400		500		ns	
$T_{DH}$	Data Hold After End of Write Time	50		100		100		ns	
$T_{WP}$	Write Pulse Width (For Write Cycle 1)	250		400		500		ns	
$T_{WR}$	End of Write to New Address Recovery Time	70		100		100		ns	
$T_{DS}$	Output Disable to Data-In Set-Up Time	130		150		200		ns	

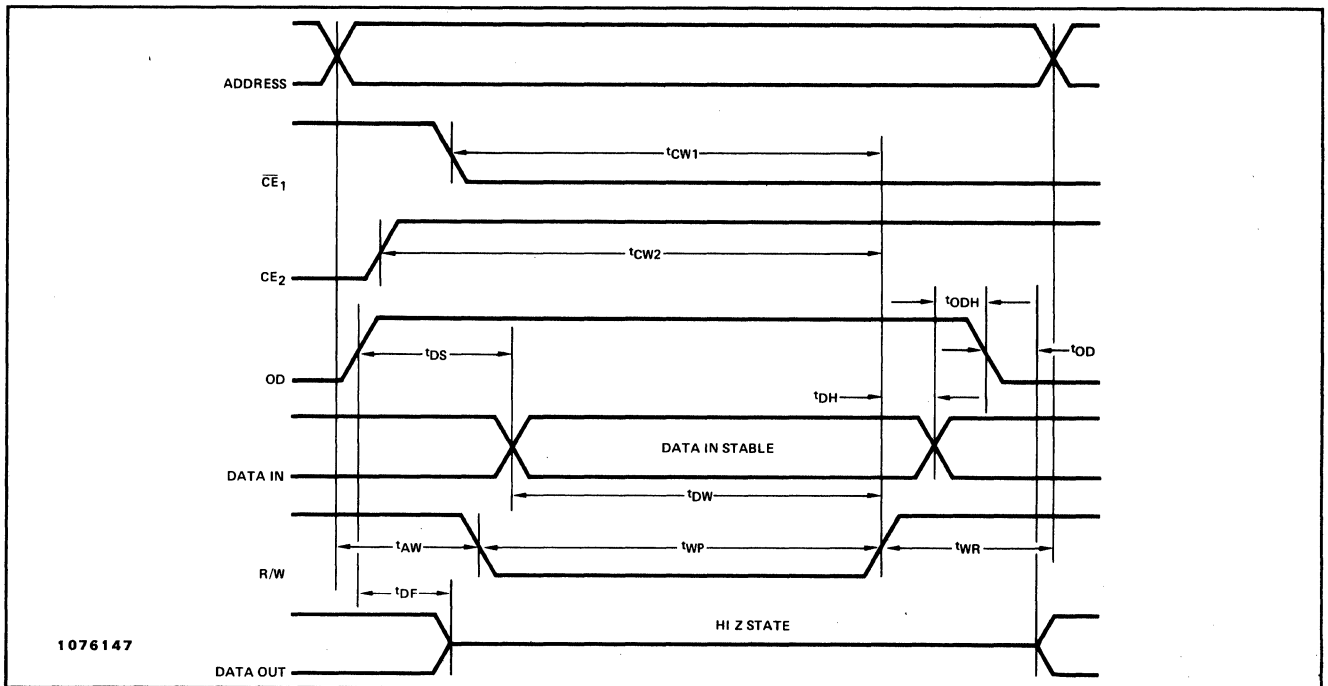
**CAPACITANCE**

SYMBOL	PARAMETERS	LIMIT		UNITS	TEST CONDITIONS
		MIN.	MAX.		
$C_{IN}$	Input Capacitance		8	pF	$V_{IN} = 0\text{V}$ , on all Input Pin
$C_O$	Output Capacitance		12	pF	$V_O = 0\text{V}$





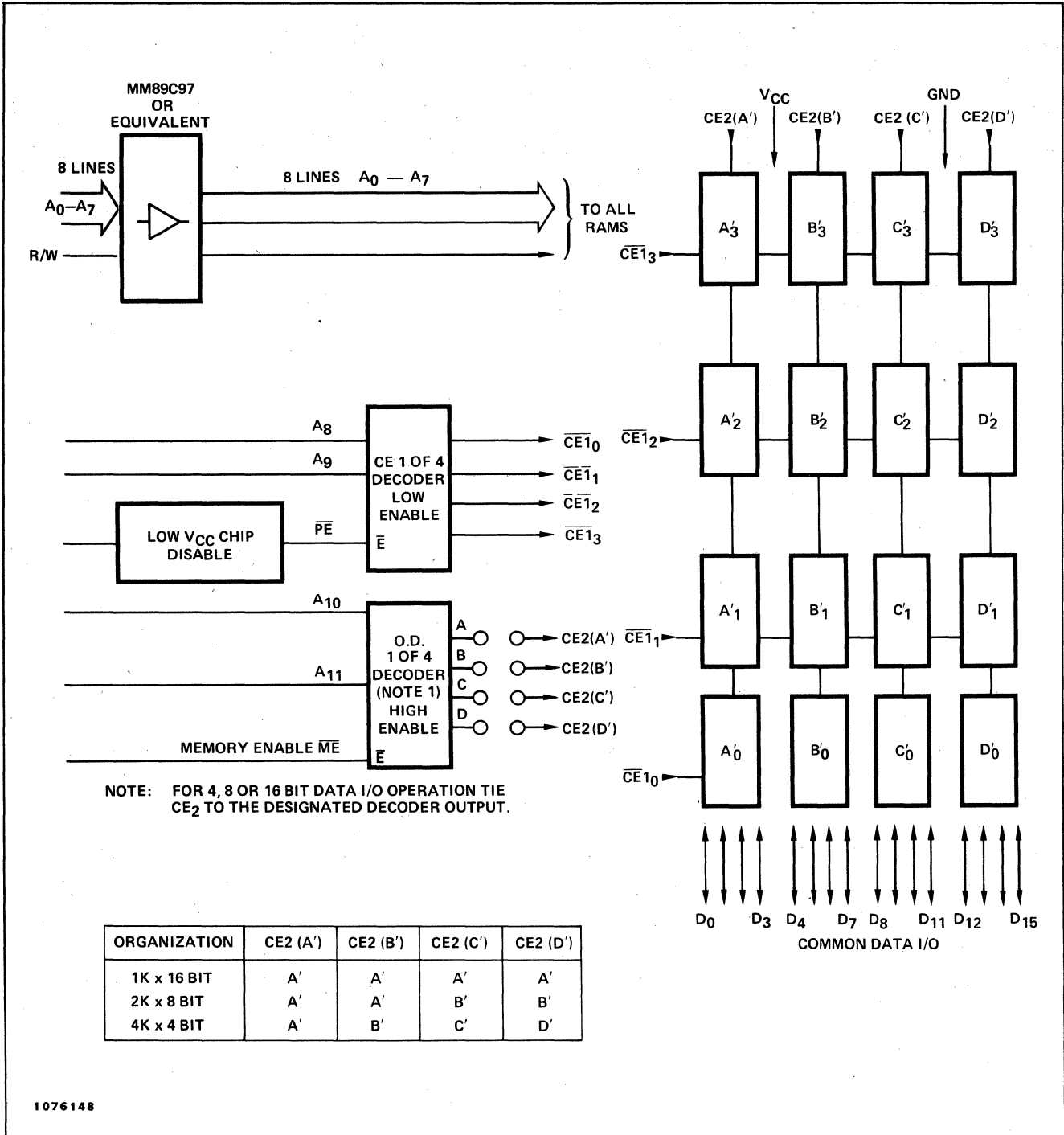
**WRITE CYCLE 1 – FOR SEPARATE OR COMMON DATA I/O**



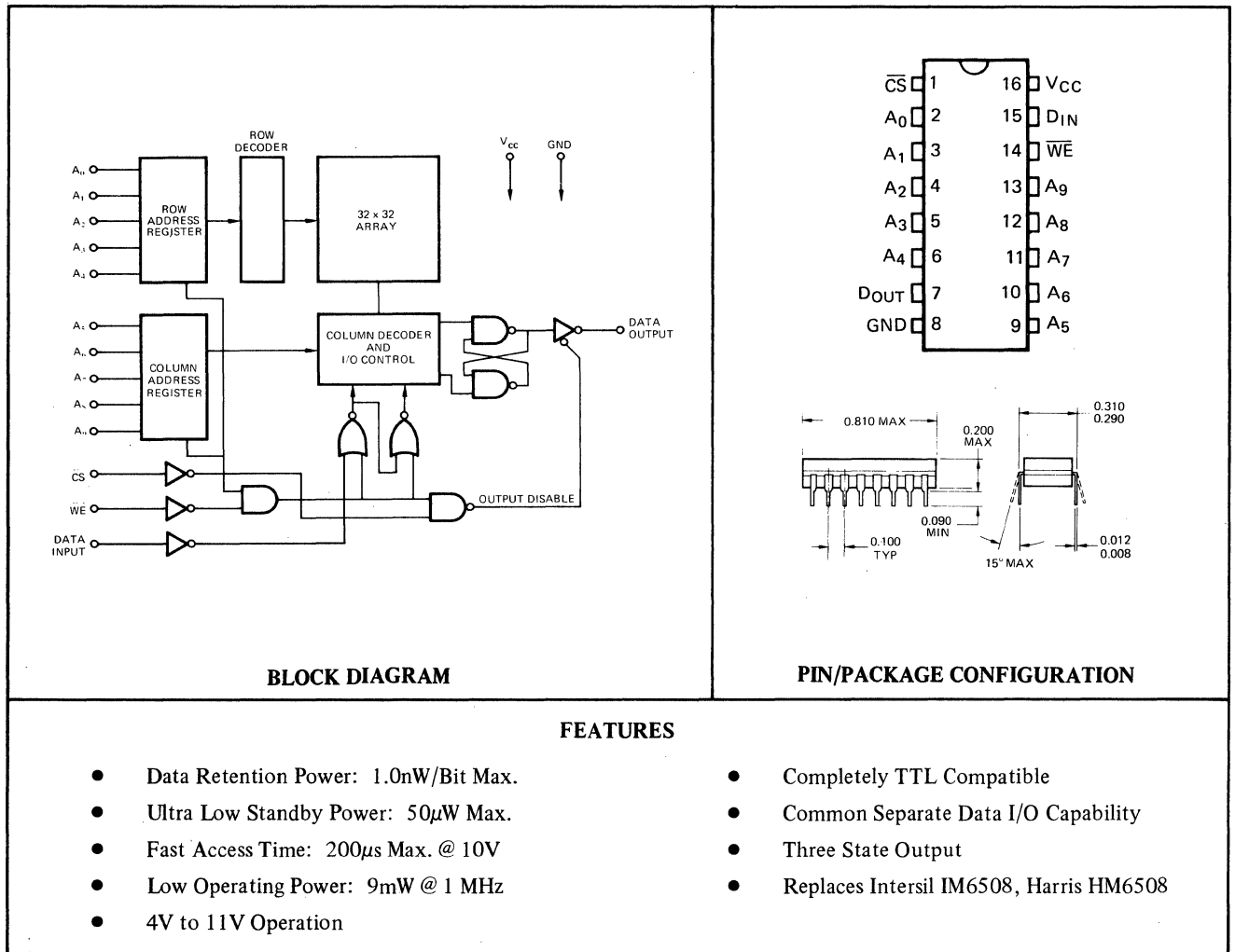
**PRODUCT SELECTION GUIDE**

DEVICE NUMBER	ACCESS TIME (NS)	STANDBY CURRENT $\mu$ A/DEVICE	POWER DOWN GUARANTEED AT 2.0V
S5101-3	650	140	NO
S5101L-3	650	140	YES
S5101	650	10	NO
S5101L	650	10	YES
S5101-2	450	140	NO
S5101L-2	450	140	YES
S5101-1	450	10	NO
S5101L-1	450	10	YES
S5101-8	800	500	NO

A 1024 x 16 BIT (or 2K x 8 or 4K x 4) CMOS READ/WRITE MEMORY



### ADVANCED PRODUCTION DESCRIPTION



### FUNCTIONAL DESCRIPTION

The AMI S6508 family of 1024 x 1 bit RAMs offers ultra low power dissipation and static operation with a single 4V to 11V power supply. Either separate or common Data I/O can be easily selected to maximize design flexibility. In applications requiring both high speed yet very low power for battery augmented non-volatile RAM storage, the S6508 family would be an ideal selection.

Address registers included in the device can improve and simplify system performance while reducing memory system package count. These internal registers latched on the HIGH to LOW transition of the chip select ( $\overline{CS}$ ). With  $\overline{CS}$  in the LOW state, S6508 family can perform the Read ( $\overline{WE} = \text{HIGH}$ ) or Write ( $\overline{WE} = \text{LOW}$ ) operations. The address which is written into or read out of was stored in the input registers when  $\overline{CS}$  went LOW.

CMOS TO CMOS – S6508A/S6508A-1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	-0.5V to $V_{CC} + 1.0V$
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C

AC CHARACTERISTICS ( $V_{CC} = 5.0V, 10V, C_L = 50pF, T_A = 25^\circ C$ )

SYMBOL	PARAMETER	LIMIT		LIMIT		UNITS
		S6508A-1		S6508A		
		MIN	MAX	MIN	MAX	
$T_{AC}$	Access Time from $CS_1$		200		350	ns
	$V_{CC} = 5V$		95		150	ns
$T_{EN}$	Output Enable Time		120		210	ns
	$V_{CC} = 10V$		55		90	ns
$T_{DIS}$	Output Disable Time		120		210	ns
	$V_{CC} = 10V$		55		90	ns
$T_{CS1}$	$CS_1$ Pulse Width (POS)					
	$V_{CC} = 5V$	135		235		ns
$\overline{T_{CS1}}$	$CS_1$ Pulse Width (NEG)					
	$V_{CC} = 10V$	65		95		ns
$T_{WP}$	Write Pulse Width (NEG)					
	$V_{CC} = 5V$	135		235		ns
$T_{ADD}$	Address Setup Time					
	$V_{CC} = 10V$	5		10		ns
$T_{ADDH}$	Address Hold Time					
	$V_{CC} = 5V$	60		105		ns
$T_{DS}$	Data Setup Time					
	$V_{CC} = 10V$	30		45		ns
$T_{PH}$	Data Hold Time					
	$V_{CC} = 5V$	0		0		ns
	$V_{CC} = 10V$	0		0		ns

**DC CHARACTERISTICS** ( $V_{CC} = 4V$  to  $11V$ ,  $T_A = \text{Industrial}$ )

SYMBOL	PARAMETER	LIMIT		UNITS	TEST CONDITIONS
		MIN	MAX		
$V_{IH}$	Logical "1" Input Voltage	$70\% V_{CC}$		V	$0V \leq V_{IN} \leq V_{CC}$ $I_{OUT} = 0$
$V_{IL}$	Logical "0" Input Voltage		$20\% V_{CC}$	V	
$I_{IL}$	Input Leakage	-1.0	1.0	$\mu A$	
$V_{OH}$	Logical "1" Output Voltage	$V_{CC} - 0.01$		V	
$V_{OL}$	Logical "0" Output Voltage		$GND + 0.01$	V	
$I_O$	Output Leakage	-1.0	1.0	$\mu A$	
$I_{CC}$	Supply Current S6508A		500	$\mu A$	
$I_{CC}$	Supply Current S6508A-1		100	$\mu A$	
$I_{CC}$	Supply Current S6508A/S6508A-1		3.5	mA	
$C_{IN}$	Input Capacitance		7.0	pF	
$C_O$	Output Capacitance		10.0	pF	

<sup>1</sup> Devices with data retention guaranteed at  $V_{CC} = 2.0$  are available.

**CMOS TO TTL – S6508/S6508-1**

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	+8.0V
Input or Output Voltage Supplied	GND -0.5V to $V_{CC} + 0.5V$
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C

**AC CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 10\%$ ,  $C_L = 50pF$  (One TTL Load),  $T_A = 0^\circ C$  to  $+70^\circ C$ )

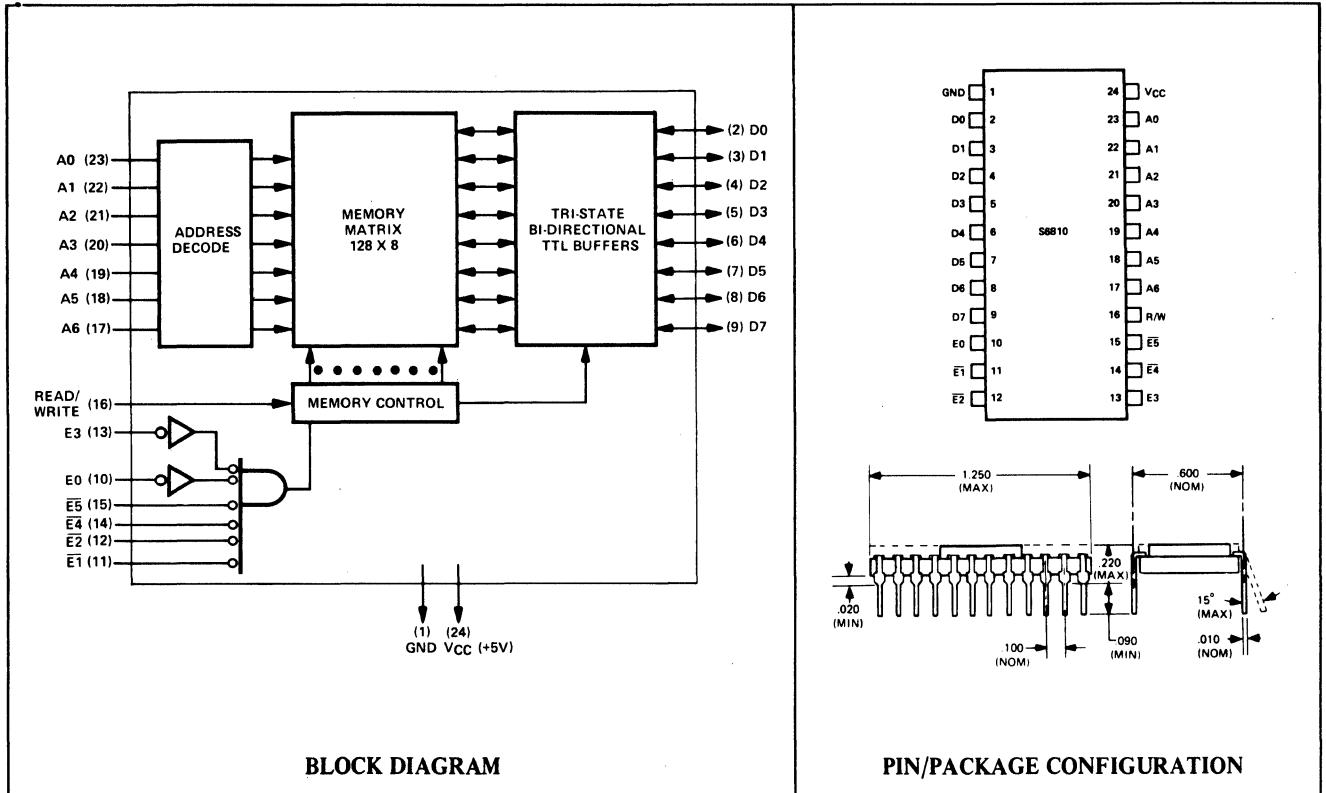
SYMBOL	PARAMETER	LIMIT S6508-1		LIMIT S6508		UNITS
		MIN	MAX	MIN	MAX	
$T_{AC}$	Access Time from $CS_1$		300		460	ns
$T_{EN}$	Output Enable Time		180		285	ns
$T_{DIS}$	Output Disable Time		180		285	ns
$T_{CS1}$	$CS_1$ Pulse Width (POS)	165		270		ns
$T_{\overline{CS1}}$	$CS_1$ Pulse Width (NEG)	300		460		ns
$T_{WP}$	Write Pulse Width (NEG)	165		270		ns
$T_{ADDS}$	Address Setup Time	7		15		ns
$T_{DS}$	Data Setup Time	165		270		ns
$T_{DH}$	Data Hold Time	0		0		ns

DC CHARACTERISTICS ( $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$ )

SYMBOL	PARAMETER	LIMIT		UNITS	TEST CONDITIONS
		MIN	MAX		
$V_{IH}$	Logical "1" Inputs Voltage	$V_{CC}-2.0$	0.8	V	$0V \leq V_{IN} \leq V_{CC}$ $I_{OUT} = 0$ $I_{OH} = -0.2mA$ $I_{OUT} = 0$ $I_{OL} = 2.0mA$ $0V \leq V_O \leq V_{CC}$ $V_{IN} = V_{CC}^1$ $V_{IN} = V_{CC}^1$ $f_c = 1MHz$
$V_{IL}$	Logical "0" Input Voltage		0.8	V	
$I_{IL}$	Input Leakage	-1.0	1.0	$\mu A$	
$V_{OH2}$	Logical "1" Output Voltage	$V_{CC}-0.01$		V	
$V_{OH1}$	Logical "1" Output Voltage	2.4		V	
$V_{OL2}$	Logical "0" Output Voltage		GND+0.01	V	
$V_{OL1}$	Logical "0" Output Voltage		0.45	V	
$I_O$	Output Leakage	-1.0	1.0	$\mu A$	
$I_{CC}$	Supply Current S6508		100	$\mu A$	
$I_{CC}$	Supply Current S6508-1		10	$\mu A$	
$I_{CC}$	Supply Current S6508/S6508-1		1.7	mA	
$C_{IN}$	Input Capacitance		7.0	pF	
$C_O$	Output Capacitance		10.0	pF	

<sup>1</sup>Devices with data retention guaranteed at  $V_{CC} = 2.0V$  are available.

## ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM

PIN/PACKAGE CONFIGURATION

### FEATURES

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Six Chip Enable Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 1.0 $\mu$ s for S6810  
575 ns for S6810-1

### FUNCTIONAL DESCRIPTION

The S6810 is a static 128 x 8 Read/Write Memory designed and organized to be compatible with the S6800 Microprocessor. Interfacing to the S6810 consists of an 8 Bit Bi-directional Data Bus, Seven Address Lines, a single Read/Write

Control line, and six Chip Enable lines, four negative and two positive.

For ease of use, the S6810 is a totally static memory requiring no clocks or cell refresh. The S6810 is fabricated with N channel silicon gate technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

### ABSOLUTE MAXIMUM RATINGS

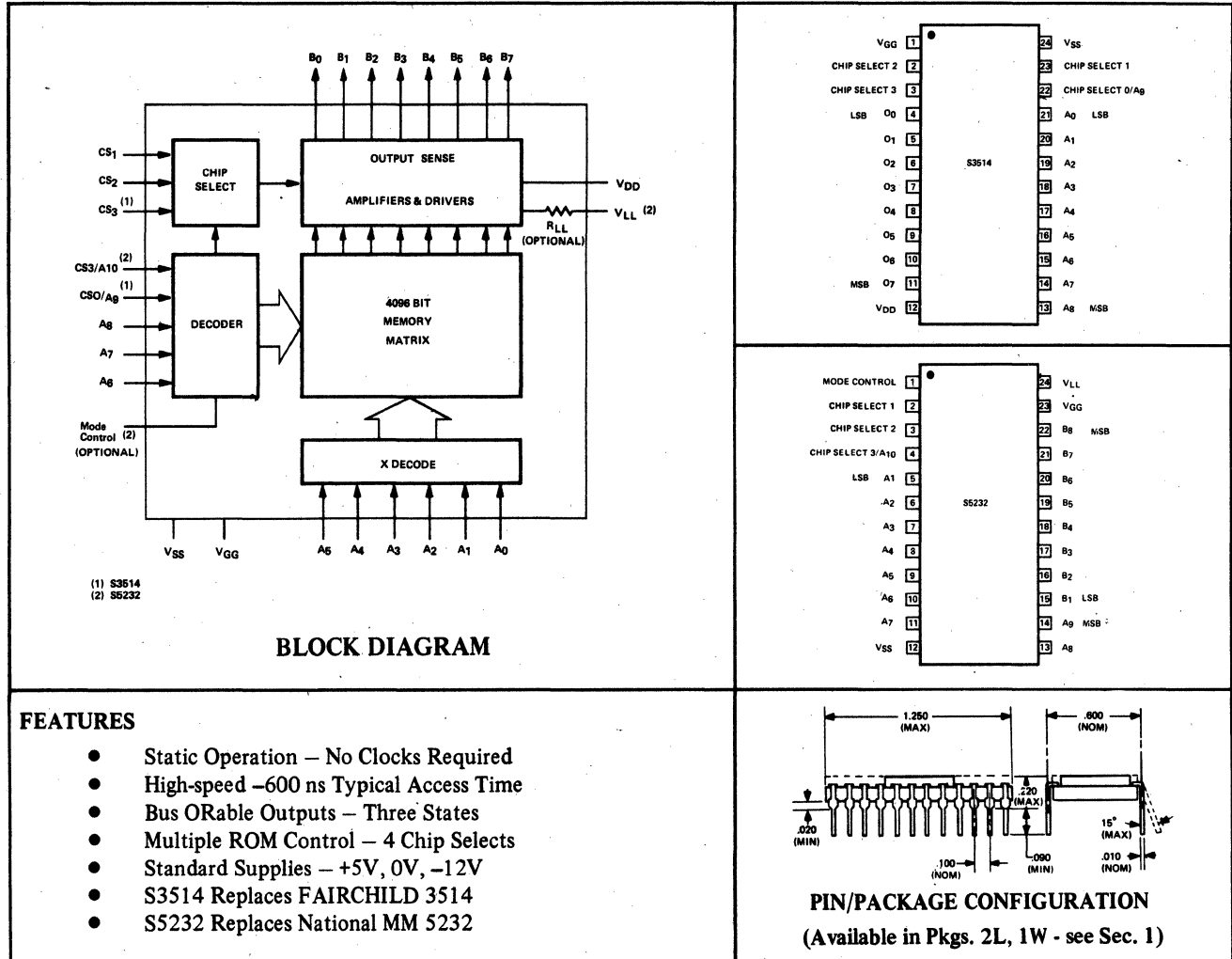
Supply Voltage $V_{CC}$	-0.3 to +7.0V
Input Voltage $V_{in}$	-0.3 to +7.0V
Operating Temperature Range $T_A$	0 to +70°C
Storage Temperature Range $T_{stg}$	-55 to +150°C

# S3514 S5232

4096 BIT STATIC  
MOS READ ONLY MEMORY



## ADVANCED PRODUCT DESCRIPTION



### FUNCTIONAL DESCRIPTION

The AMI S3514 and S5232 are TTL compatible MOS read-only memories (ROM) designed to store 4096 bits of information by programming one mask pattern. The word and bit organizations of these ROMs are either 512 x 8 or 1024 x 4. Both ROMs have push-pull outputs that can be in one of three states: HIGH, LOW or open (unselected state). This, plus the programmable Chip Selects, enables the use of several ROMs in parallel with no external components.

Since the ROM is a static device, no clocks are required, making these ROMs both versatile and easy to use.

Low threshold-voltage processing, utilizing AMI's I<sup>2</sup>TM is used with P-channel, depletion-mode MOS technology to provide direct output interfacing with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

### TYPICAL APPLICATIONS

Code Conversion, Table Lookup, Microprogramming, Control Logic.



## ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to $V_{SS}$ (except $V_{GG}$ )	+0.3V to -10V
Voltage on $V_{GG}$ Terminal Relative to $V_{SS}$	+0.3V to -20V
Operating Temperature Range (Ambient)	0°C to +70°C
Storage Temperature Range (Ambient)	-55°C to +150°C

## RECOMMENDED OPERATING CONDITIONS

(0°C ≤  $T_A$  ≤ 70°C)

	Parameter	Min.	Max.	Units	Notes (Page 5-8)
$V_{SS}$	Supply Voltage	+4.75	+5.25	V	
$V_{DD}$	Supply Voltage	0	0	V	Note 1
$V_{GG}$	Supply Voltage	-11.4	-12.6	V	
$V_{LL}$	Output Load Voltage	0	-12.6	V	Note 2, 7
$V_{IL}$	Input Voltage, LOW Level	0	$V_{SS}-4.0$		
$V_{IH}$	Input Voltage, HIGH Level	$V_{SS}-1.5$	$V_{SS}$	V	Note 3
$V_{IH}$	Input Voltage, HIGH Level	$V_{SS}-2.0$	$V_{SS}$	V	Note 4

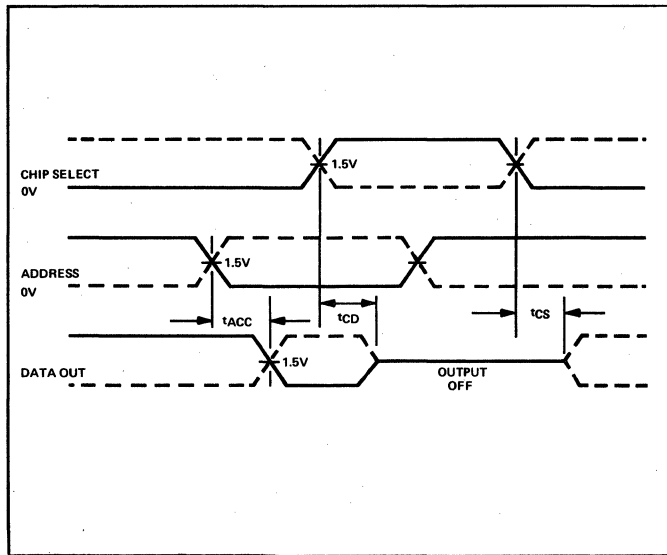
## ELECTRICAL CHARACTERISTICS

( $V_{SS} = +5.0V \pm 5\%$ ;  $V_{DD} = 0V$ ;  $V_{GG} = -12V \pm 5\%$ ;  $V_{LL} = -12V \pm 5\%$ ; 0°C ≤  $T_A$  ≤ 70°C unless noted otherwise)

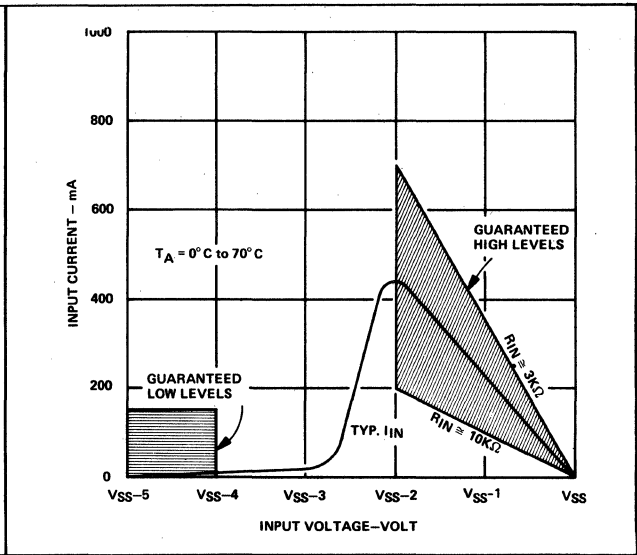
	Parameter	Min.	Max.	Units	Notes (Page 5-8)
$I_{SS}$	Supply Current, $V_{SS}$		28.0	mA	Note 5
$I_{GG}$	Supply Current, $V_{GG}$		28.0	mA	Note 5
$R_{LL}$	Output Load Resistor	500	2000	Ω	Note 7
$I_{I(L)}$	Input Leakage Current,		1.0	μA	$V_I = V_{SS} - 6.0V$ . Note 3
$I_{IL}$	Input Current, LOW Level	0	-150	μA	$V_I = V_{SS} - 4.0V$ . Note 4
$I_{IH}$	Input Current, HIGH Level	-200	-700	μA	$V_I = V_{SS} - 2.0V$ . Note 4
$V_{OL}$	Output Voltage, LOW Level		0.4	V	$I_{OL} = 1.6mA$
$V_{OH}$	Output Voltage, HIGH Level	2.4		V	$I_{OH} = -100\mu A$
$I_{O(L)}$	Output Leakage Current		+10	μA	Outputs disabled ( $V_O = V_{SS} - 6V$ )
$C_{IN}$	Input Capacitance		10	pF	Note 6
$C_O$	Output Capacitance		10	pF	Note 6
$t_{ACCESS}$	Address to Output Access Time		1000	nsec	Note 8, See Timing
$t_{CS}$	Chip Select to Output Delay		800	nsec	
$t_{CD}$	Chip Deselect to Output Delay		800	nsec	

- NOTES:**
1. Not available on S5232
  2. Not available on S3514
  3. This parameter is for inputs without active pull-ups (programmable).
  4. This parameter is for inputs with active pull-ups (programmable) for TTL interfaces. As the TTL driver goes to a HIGH level it must only provide  $V_{SS}-2.0V$  (this voltage must not be clamped) and the input circuit pulls the output of the TTL device to  $V_{SS}$ . See Optional Input Pull-up Characteristics.
  5. Inputs at  $V_{SS}$ , outputs unloaded.  $V_{DD}$  current comes only from the output loads.
  6.  $V_{Bias} - V_{SS} = 0V$ ;  $f = 1\text{ MHz}$ .
  7. This option available only on S5232 with 1024 x 4 organization. For 512 x 8 organization,  $V_{LL} = 0V$ . For 1024 x 4 organization,  $V_{LL} = 0V$  if  $R_{LL}$  is not programmed in; and  $V_{LL} = -12V \pm 5\%$ , if  $R_{LL}$  is programmed in. See output stage circuit options.
  8. Outputs sinking 1.6mA or sourcing  $-100\mu A$  and total load capacitance = 75pF.

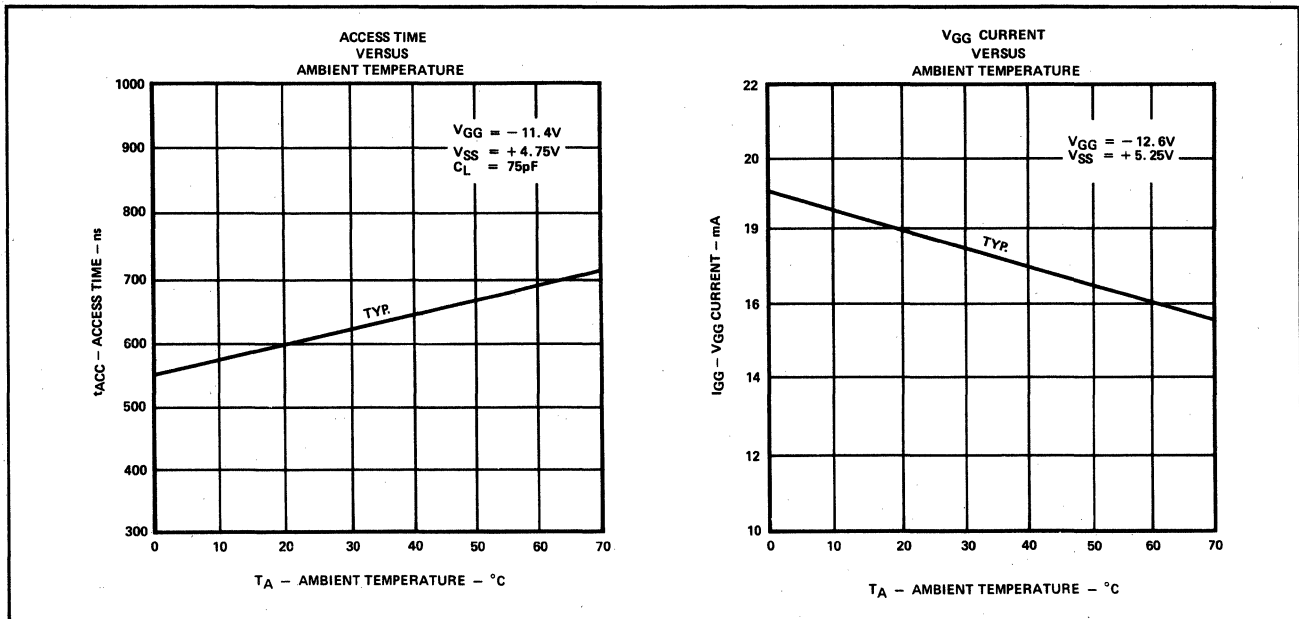
**TIMING CHARACTERISTICS**



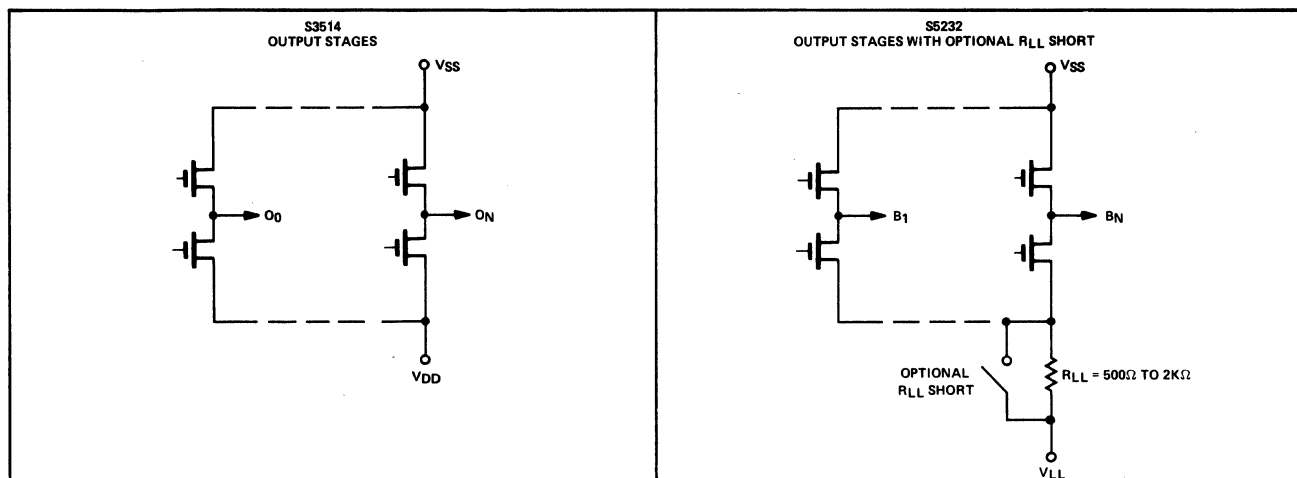
**OPTIONAL INPUT PULL-UP CHARACTERISTICS**



**TYPICAL CHARACTERISTICS**



## OUTPUT STAGE CIRCUIT OPTIONS



## OPERATING MODE

### S3514

Function	512 x 8	1024 x 4
Chip Select 0/A9	1 or 0	A9
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3	1 or 0	1 or 0

1 = Most Positive = High Level Voltage

### S5232

Function	512 x 8	1024 x 4
Mode Control	1	0
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3/A10	1 or 0	address A10

1 = Most Positive = High Level Voltage

512 x 8: Chip Select 0/A9 operates as Chip Select 0.

512 x 8: Mode Control – High  
Chip Select 3/A10 operates as Chip Select 3.

1024 x 4: \*A9 – Low enables odd outputs (O<sub>1</sub>, O<sub>3</sub>, O<sub>5</sub>, O<sub>7</sub>)  
A9 – High enables even outputs (O<sub>0</sub>, O<sub>2</sub>, O<sub>4</sub>, O<sub>6</sub>)

1024 x 4: Mode Control – Low  
\*A10 – High enables even outputs (B<sub>2</sub>, B<sub>4</sub>, B<sub>6</sub>, B<sub>8</sub>)  
A10 – Low enables odd outputs (B<sub>1</sub>, B<sub>3</sub>, B<sub>5</sub>, B<sub>7</sub>)

\*See note 9 on the following page.

\*See note 9 on the following page.

Chip Selects: Four programmable chip selects provide control over 16-S3514 ROMS with no external decoding.

Chip Selects: Three programmable chip selects provide control over 8-S5232 ROMs with no external decoding.

## AMI ROM PUNCHED-CARD CODING FORMAT<sup>1</sup>

### First Card

Cols.	Information Field
1–30	Customer
31–50	Customer Part Number
60–72	AMI Part Number <sup>2</sup>

### Second Card

1	Organization <sup>3</sup>
3	CS <sub>0</sub> <sup>4</sup> /A <sub>9</sub> <sup>8</sup>
5	CS <sub>3</sub> <sup>4</sup>
7	CS <sub>2</sub> <sup>4</sup>
9	CS <sub>1</sub> <sup>4</sup>
11	Active Pull-ups <sup>5</sup>

### First Card

Cols.	Information Field
1–30	Customer
31–50	Customer Part Number
60–72	AMI Part Number <sup>2</sup>

### Second Card

1	Organization <sup>3</sup>
3	CS <sub>3</sub> <sup>4</sup> /A <sub>10</sub> <sup>9</sup>
5	CS <sub>2</sub> <sup>4</sup>
7	CS <sub>1</sub> <sup>4</sup>
9	Active Pull-ups <sup>5</sup>
11	Series resistor to V <sub>LL</sub> <sup>6</sup>

AMI ROM PUNCHED-CARD CODING FORMAT<sup>1</sup> (Cont.)

S3514

S5232

Data Cards/512 x 8 Organization

- 1-4 Decimal Address
- 6-13 Output O7 - O0 (MSB thru LSB)
- 15-17 Octal Equivalent of output data<sup>7</sup>

Data Cards/1024 x 4 Organization

- 1-4 Decimal Address (0-1022) even addresses
- 6-9 Output (MSB-LSB)
- 11-12 Octal Equivalent of output data<sup>7</sup>
- 50-53 Decimal Address (1-1023) odd addresses
- 55-58 Output (MSB-LSB)
- 60-61 Octal Equivalent of output data<sup>7</sup>

Data Cards/512 x 8 Organization

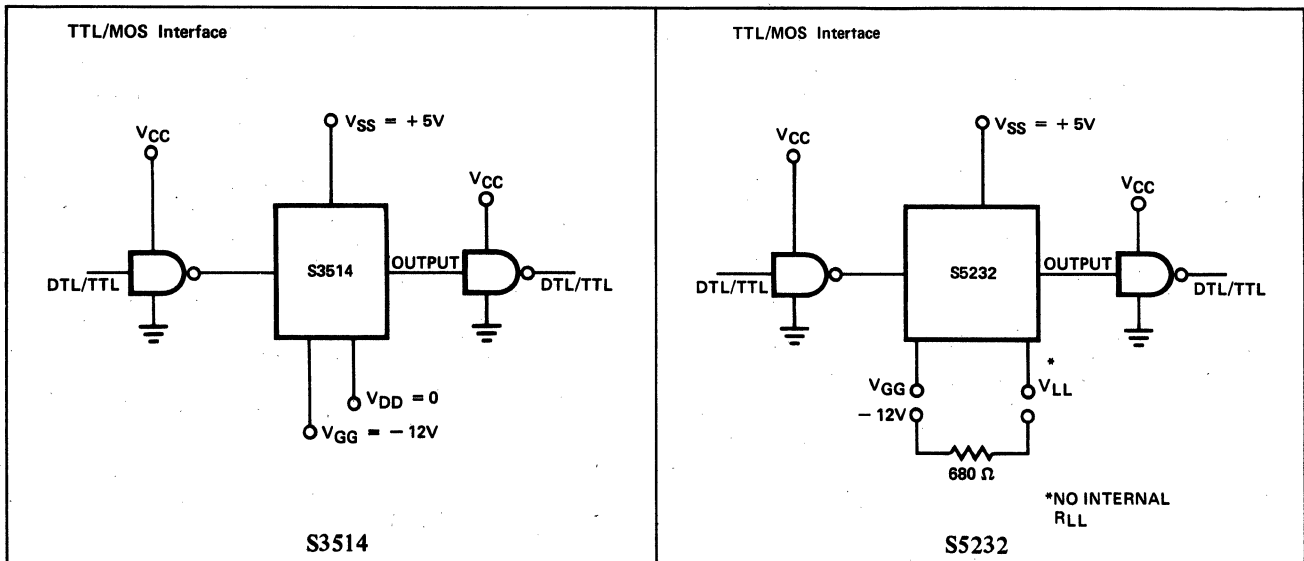
- 1-4 Decimal Address
- 6-13 Output B8-B1 (MSB thru LSB)
- 15-17 Octal Equivalent of output data<sup>7</sup>

Data Cards/1024 x 4 Organization

- 1-4 Decimal Address (0-1022) even addresses
- 6-9 Output (MSB-LSB)
- 11-12 Octal Equivalent of output data<sup>7</sup>
- 50-53 Decimal Address (1-1023) odd addresses
- 55-58 Output (MSB-LSB)
- 60-61 Octal Equivalent of output data<sup>7</sup>

- NOTES:
1. Positive logic formats accepted only.
  2. Assigned by Marketing Department; may be left blank.
  3. A "0" indicates 512 x 8; a "1" indicates 1024 x 4.
  4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.
  5. A "1" indicates active pull-ups; a "0" indicates no pull-ups.
  6. A "0" indicates an internal resistor, a "1" indicates no internal resistor. Available only with 1024 x 4 organization.
  7. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 10011110 would be separated into groups 10/011/110 and the resulting octal equivalent number is 236.
  3. For 1024 x 4 organization, CS0/A9 input acts as A9 address. A9 LOW enables odd outputs; A9 HIGH enables even outputs. For this case, a "0" is required in this field. However, if it is required that A9 HIGH should enable odd outputs and A9 LOW should enable even outputs, a "1" may be punched in this field.
  9. For 1024 x 4 organization, CS3/A10 acts as A10 address. A10 LOW enables odd outputs; and A10 HIGH enables even outputs. For this case, a "0" is required in this field. However, if it is required that A10 HIGH should enable odd outputs and A10 LOW should enable even outputs, a "1" may be punched in this field.

TYPICAL APPLICATION



\*For applications where  $V_{GG}$  is connected to  $V_{LL}$ , where low power dissipation is required on outputs and where a constant external resistance is preferred, the internal resistor can be programmed out and an external 680Ω resistor can be connected as shown.

### ADVANCED PRODUCT DESCRIPTION

**BLOCK DIAGRAM**

**PIN/PACKAGE CONFIGURATION**

#### FEATURES

<ul style="list-style-type: none"> <li>● On-Board Programmability</li> <li>● Fast Access Time – 750 ns Max.</li> <li>● High Speed Programming – Less than 1 Minute for all 4096 Bits</li> <li>● Programmed with R/W, CS and V<sub>PROG</sub> Pins</li> <li>● Completely TTL Compatible – Excluding the V<sub>PROG</sub> Pin during Read or Write</li> </ul>	<ul style="list-style-type: none"> <li>● Ultraviolet Light Erasable – Less than 10 Minutes</li> <li>● Static Operation – No Clocks Required</li> <li>● Three-State Data I/O</li> <li>● Standard Power Supplies +5V and -12V</li> <li>● Mature P-Chan Process</li> </ul>
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#### FUNCTIONAL DESCRIPTION

The S5204A is a high speed, static, 512 x 8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24 pin hermetically sealed dual in-line package the bit pattern can be erased by exposing the chip to an ultra-violet light source

through the transparent lid, after which a new pattern can be written.

#### TYPICAL APPLICATIONS

- |  |   |
|--|---|
| <ul style="list-style-type: none"> <li>● Random Logic Replacement</li> <li>● Programmable Waveforms</li> <li>● Character Generation</li> <li>● Electronic Keyboards</li> </ul> | <ul style="list-style-type: none"> <li>● ROM Program Debugging</li> <li>● Code Translation</li> <li>● Microprogramming</li> <li>● Look-up Tables</li> </ul> |
|--|---|

#### ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V <sub>SS</sub> except the V <sub>PROG</sub> pin	+0.3 to -20V
Voltage on the V <sub>PROG</sub> pin relative to V <sub>SS</sub>	+0.3 to -60V
Operating Temperature	0°C to +70°C
Storage Temperature (programmed)	-55°C to +85°C
Storage Temperature (unprogrammed)	-55°C to 150°C

**NOTE:** This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS ( $V_{CC} = +5.0V \pm 5\%$ ,  $V_{GG} = -12.0V \pm 5\%$ ,  $T_A = 0 - 70^\circ C$  unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
$V_{IL}$	INPUT VOLTAGE LOW		0.8	V
$V_{IH}$	INPUT VOLTAGE HIGH	$V_{CC} - 2.25$	$V_{CC} + 3$	V
$V_{OL}$	OUTPUT VOLTAGE LOW $I_{OL} = 1.6 \text{ ma}$		0.4	V
$V_{OH}$	OUTPUT VOLTAGE HIGH $I_{OH} = 200 \mu A$	2.4		V
$I_{LI}$	INPUT LEAKAGE CURRENT		10	$\mu a$
$I_{LO}$	OUTPUT LEAKAGE CURRENT $CS = 5V$		20	$\mu a$
$I_{GG}$	$V_{GG}$ SUPPLY CURRENT		45	ma
$I_{CC}$	$V_{CC}$ SUPPLY CURRENT		50	ma
$P_D$	POWER DISSIPATION		750	mw

NOTE: Program input  $V_{PROG}$  may be tied to  $V_{CC}$  during the Read.

AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
$T_{ACC}$	ACCESS TIME		750	ns
$T_{CO}$	CHIP SELECT TO OUTPUT DELAY		400	ns
$T_{DD}$	CHIP DESELECT TO OUTPUT DELAY			ns

PROGRAM CHARACTERISTICS (R/W  $G_{nd}$ , Program pulse rise and fall time (10% to 90%) are both at  $1\mu s$  max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
$T_{AS}$	ADDRESS SET UP TIME	10		$\mu s$
$T_{CSS}$	CHIP SELECT SET UP TIME	10		$\mu s$
$T_{DS}$	DATA SET UP TIME	10		$\mu s$
$T_{AH}$	ADDRESS HOLD TIME	10		$\mu s$
$T_{CSH}$	CHIP SELECT HOLD TIME	10		$\mu s$
$T_{DH}$	DATA HOLD TIME	10		$\mu s$
$T_{PWL}$	PROGRAM PULSE WIDTH LOW	3	5	ms
$T_{PWH}$	PROGRAM PULSE WIDTH HIGH	500		$\mu s$
$V_{PROG}^*$	PROGRAM AMPLITUDE	-55	-50	V
$I_{PROG}$	PROGRAM CURRENT		35	ma
$T_{WS}$	WRITE SET UP TIME	10		$\mu s$
$T_{WH}$	WRITE HOLD TIME	5		$\mu s$
$T_{RS}$	READ SET UP TIME	10		$\mu s$

\*Note that in the WRITE mode the MIN value of  $V_{PROG}$  should not be exceeded and that chip select, address, and data lines may remain at TTL level, as in the READ mode

## INTERFACE DESCRIPTION

Pin	Label	Function
(15)	D0	<p><b>Data Lines</b> – with the R/W line selected for Read (<math>V_{IH}</math>), the Data Line (D0 through D7) are set to reflect the contents of the selected memory location. When the R/W line is set for Write (<math>V_{IL}</math>), the Data Lines are stored at the addressed location of the 5204A when <math>V_{PROG}</math> is present. The Data Bus output drivers are three-state devices that remain in the high impedance (off) state whenever CS is in the <math>V_{IH}</math> state or when R/W is in the <math>V_{IL}</math> state.</p> <p><b>Read/Write</b> – When this input line is set to <math>V_{IH}</math>, the device is in the Write mode, a low (<math>V_{IL}</math>) signal puts it into the Read mode.</p> <p><b>Chip Select</b> – This input line must be set to <math>V_{IL}</math> for a Read or Write operation to be performed. When it is High (<math>V_{IH}</math>) the output data bus is set to a high-impedance three-state condition.</p> <p><b>Program</b> – In the Write mode, a 50Volt programming pulse at this input causes the data at the Data Lines to be stored in the selected address location. This pin should be tied to <math>V_{CC}</math> for normal Read operations.</p> <p><b>Address Lines</b> – These lines select the 8 bit word in memory for Read or Write operation.</p>
(16)	D1	
(17)	D2	
(18)	D3	
(19)	D4	
(20)	D5	
(21)	D6	
(22)	D7	
(2)	R/W	
(3)	CS	
(4)	$V_{PROG}$	
(5)	A0	
(6)	A1	
(7)	A2	
(8)	A3	
(9)	A4	
(10)	A5	
(11)	A6	
(13)	A7	
(14)	A8	

## CONTROL FUNCTION TRUTH TABLE

CS	R/W	$V_{PROG}$	MODE	OUTPUTS
0	1	$V_{PROG}$	Write	Active Data Inputs
0	0	$V_{CC}$	Read	Active
1	X	X	Standby	Floating

## OPERATION

Initially, and after each erasure, all bits of the 5204A are in the LOW state (output 0 volts). Data is stored by selectively programming a HIGH into the desired bit locations. The R/W input (pin 2) is used to select the desired mode of operation. When the R/W input is HIGH the chip is in the write enable mode of operation. The outputs (D<sub>0</sub> – D<sub>7</sub>) are disabled (floating) with the corresponding pins becoming the data inputs. The word address is selected in the same manner as in the Read mode. Data to be programmed is presented 8 bits in parallel and after the address and data are set up a programming pulse ( $V_P = -50$  volts) is applied.  $V_{PROG}$  electrically writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a HIGH during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and  $V_{PROG}$  inputs are common and the device to be programmed is selected by means

of the chip select input as during read operations.

The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses (N) times the program pulse width ( $t_{pw}$ ) ( $N \times t_{pw} \geq 60$  msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

The read operation is accomplished by a LOW at the R/W input with the program input connected to  $V_{SS}$  potential. True data (data out = data in) is valid after the address is stable. The CS input will disable (float) the outputs when HIGH to allow capability with bus organized systems.

Erasure is accomplished by exposing the array to a 2537Å ultra-violet light source (such as Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54, Turner Designs PROM Eraser, Model 30 or equivalent) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

FIGURE 1 – TEST CONDITIONS

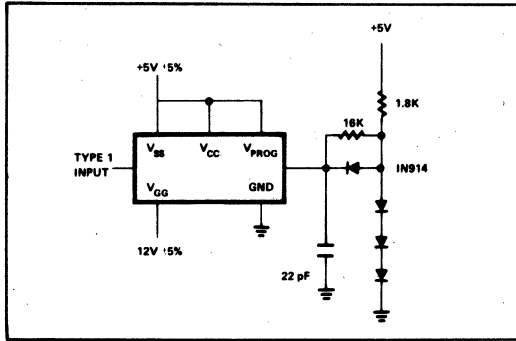


FIGURE 2 – READ CYCLE TIMING WAVEFORMS

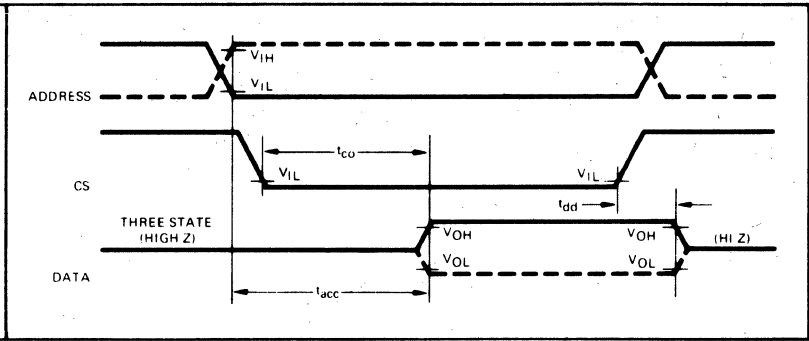


FIGURE 3 – PROGRAMMING CYCLE TIMING WAVEFORMS

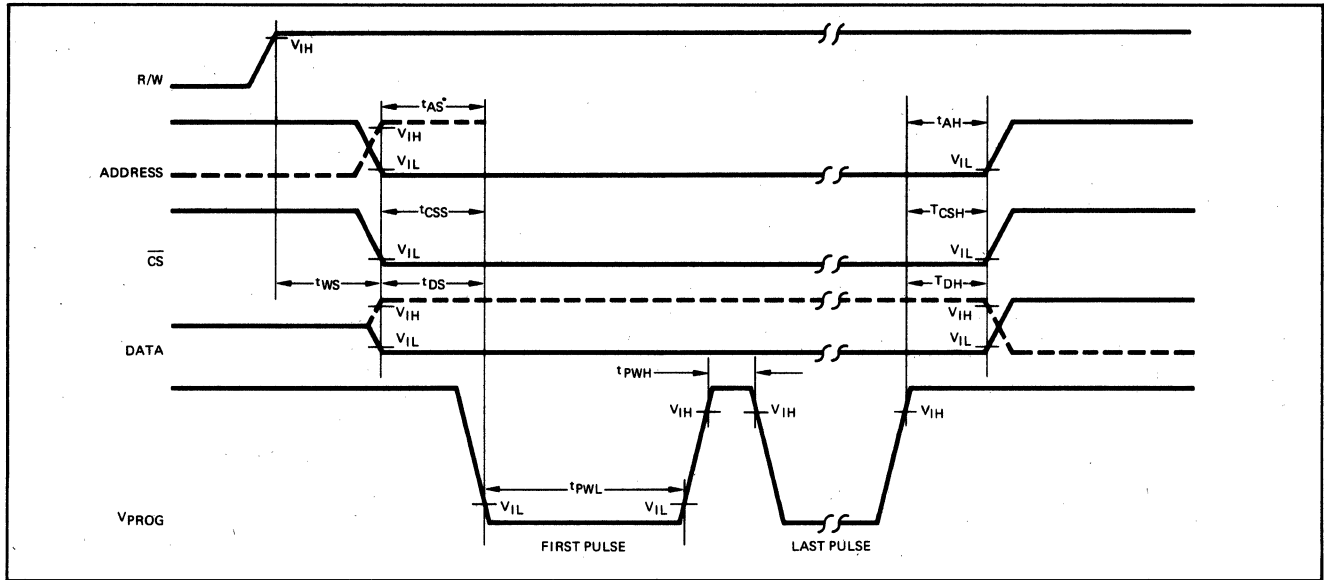
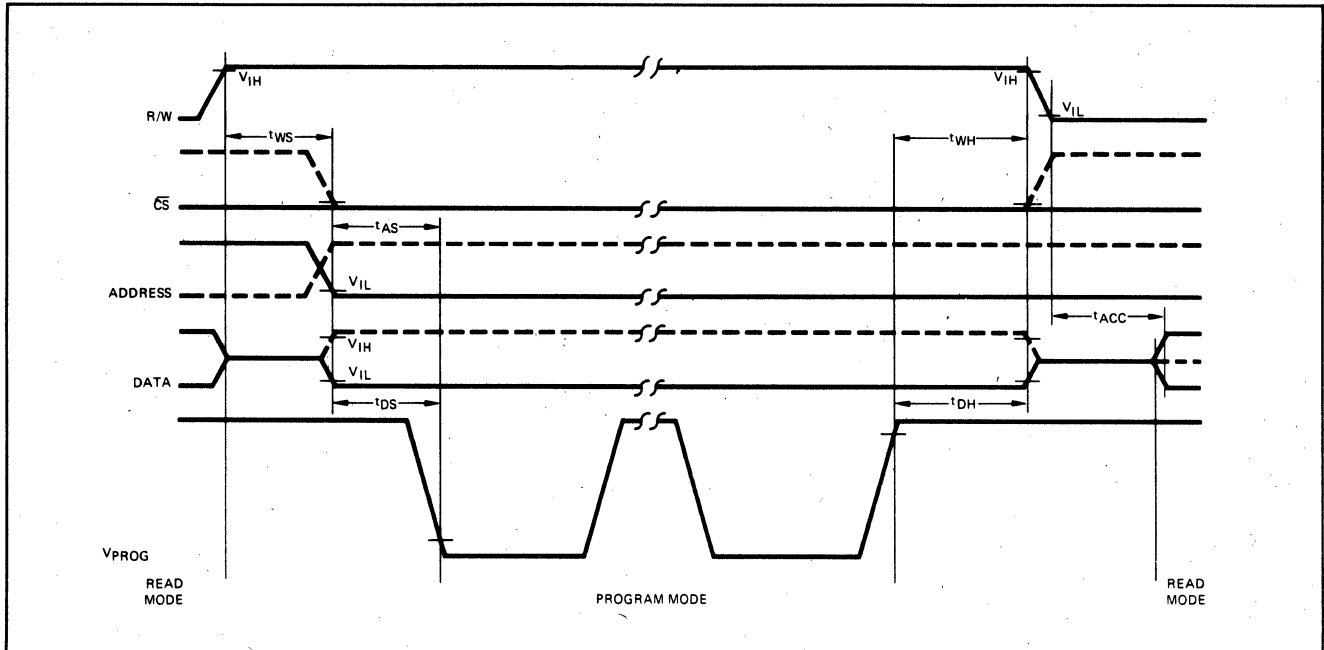
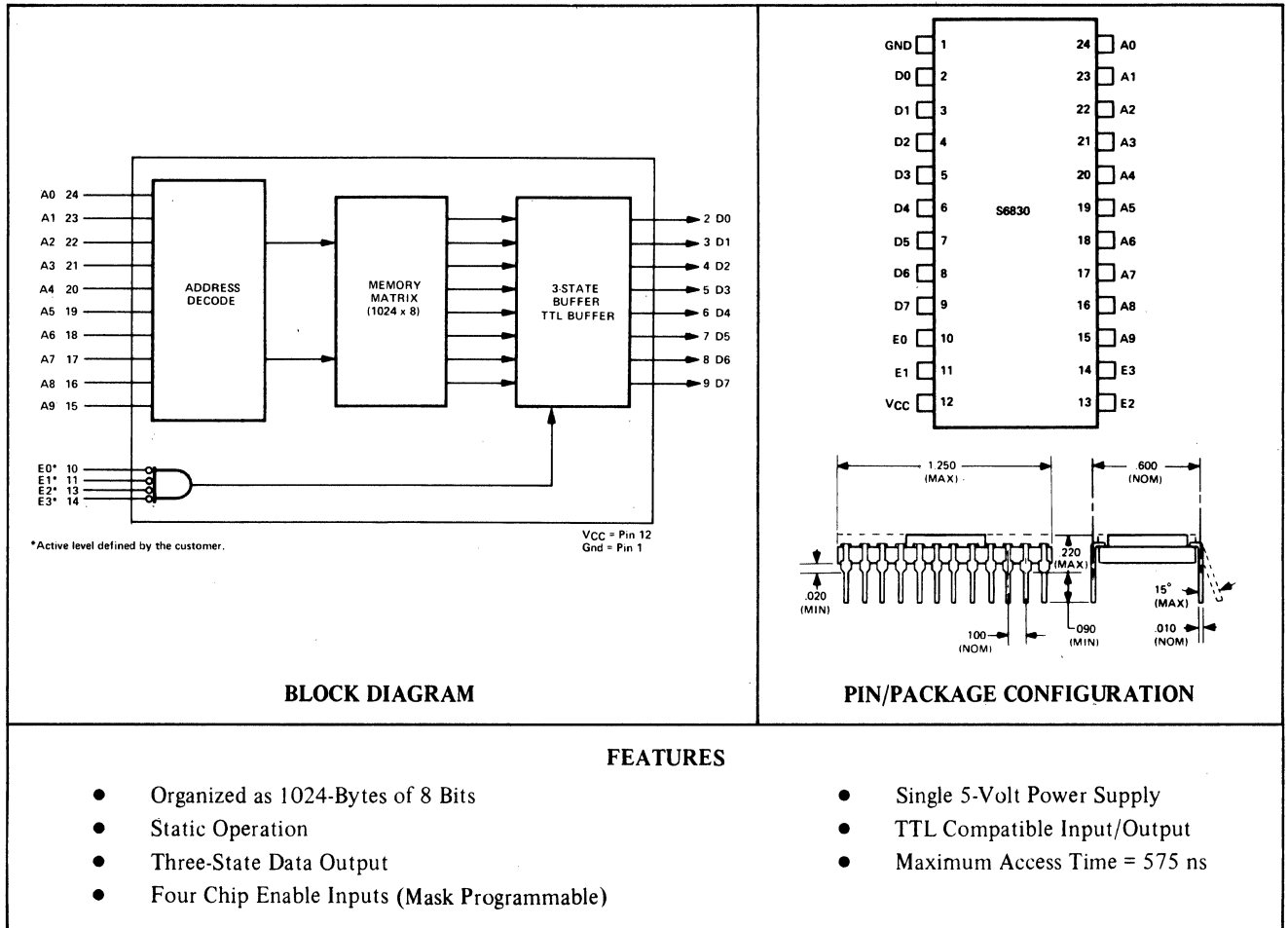


FIGURE 4 – READ/PROGRAM/READ CYCLE TIMING WAVEFORM







### FUNCTIONAL DESCRIPTION

The S6830 is a mask programmable read only memory organized 1024 words x 8 bits for application in byte organized systems. The S6830 is totally bus compatible with the S6800 microprocessor. Interfacing to the S6830 consists

of an 8 bit three-state data bus, four mask programmable chip selects and ten address lines.

The S6830 is a totally static memory requiring no clocks. Access time is compatible with maximum data rates in a S6800 microprocessor system. The device operates from a single +5 volt power supply and is fabricated with N channel silicon gate technology.

### ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply Voltage $V_{CC}$	-0.3 to +7.0V
Input Voltage $V_{in}$	-0.3 to +7.0V
Operating Temperature Range $T_A$	0 to +70°C
Storage Temperature Range $T_{stg}$	-55 to +150°C

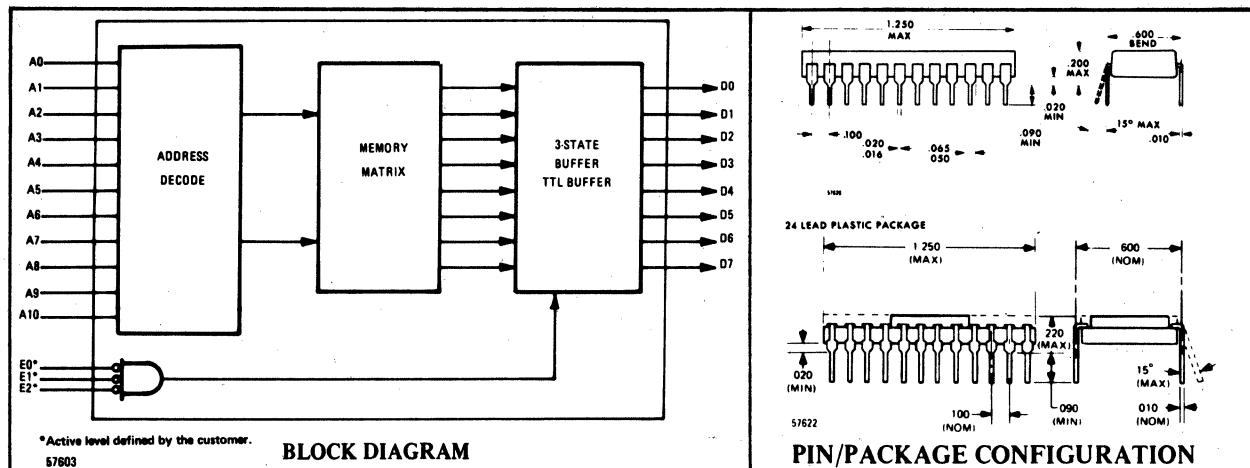
NOTE: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

# S6831/A/B/C

2048 X 8  
READ ONLY MEMORY



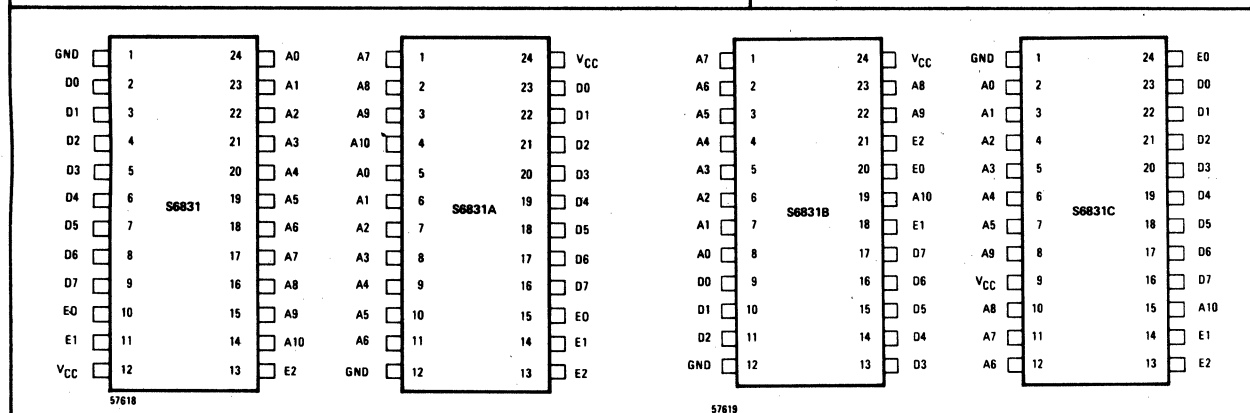
## ADVANCED PRODUCT DESCRIPTION



\*Active level defined by the customer.  
57603

**BLOCK DIAGRAM**

**PIN/PACKAGE CONFIGURATION**



## FEATURES

- Maximum Access Time = 450 ns @  $C_L = 130$  pF
- Low Power 150 mW avg.
- Organized as 2048-Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- 3 Chip Enable Inputs (Mask Programmable)
- The S6831 is pinout similar with the S6830
- The S6831A is pinout compatible with the 2316A, 8316A
- The S6831B is pinout compatible with the Intel 2316B, MC68317
- The S6831C is pinout compatible with the EA4600
- Single 5-Volt Power Supply
- TTL Compatible Input/Output

## FUNCTIONAL DESCRIPTION

The S6831/A/B/C is a 16,384 bit Read Only Memory organized 2K words x 8 bits. This ROM has been designed to supply large bit storage, high performance memory for micro-

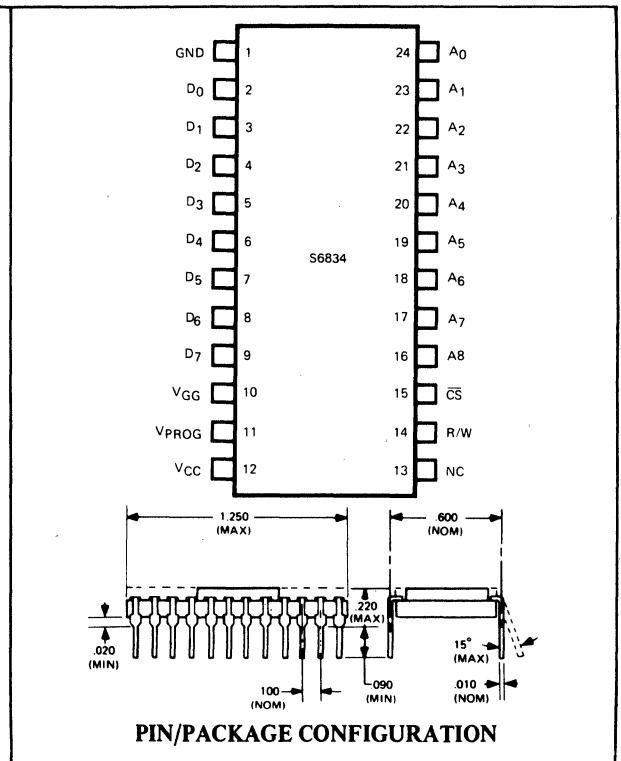
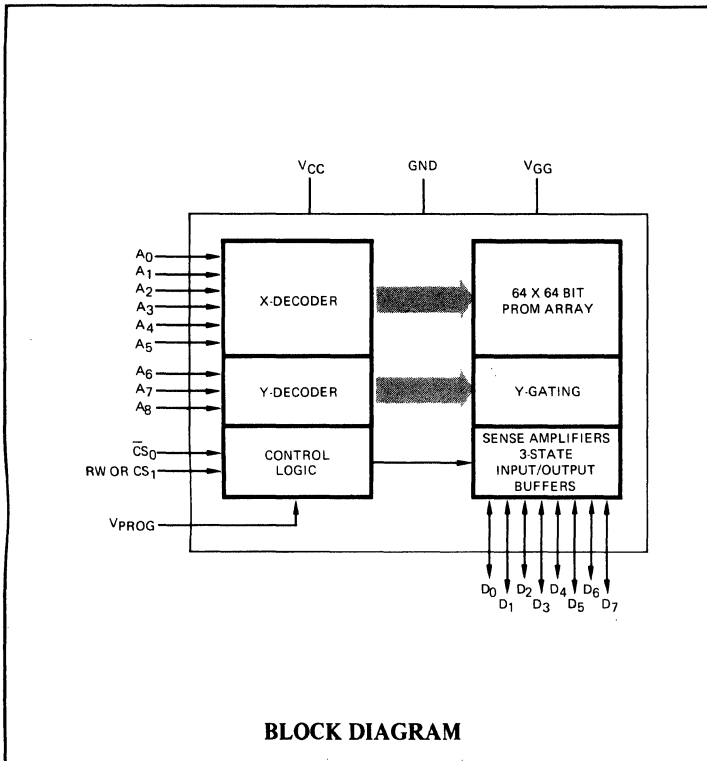
processors and other demanding applications with simple interface requirements. The device will operate from a single +5V supply and is manufactured with a N-channel silicon gate depletion load technology. This device is available in all common high density ROM pinouts.

## ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply Voltage $V_{CC}$	- 0.5 to + 7.0V	Operating Temperature Range $T_A$	0 to + 70°C
Input Voltage $V_{in}$	- 0.5 to + 7.0V	Storage Temperature Range $T_{stg}$	- 55 to + 150°C

**NOTE 1** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

For a Complete Data Sheet See Page 3-33.



### FEATURES

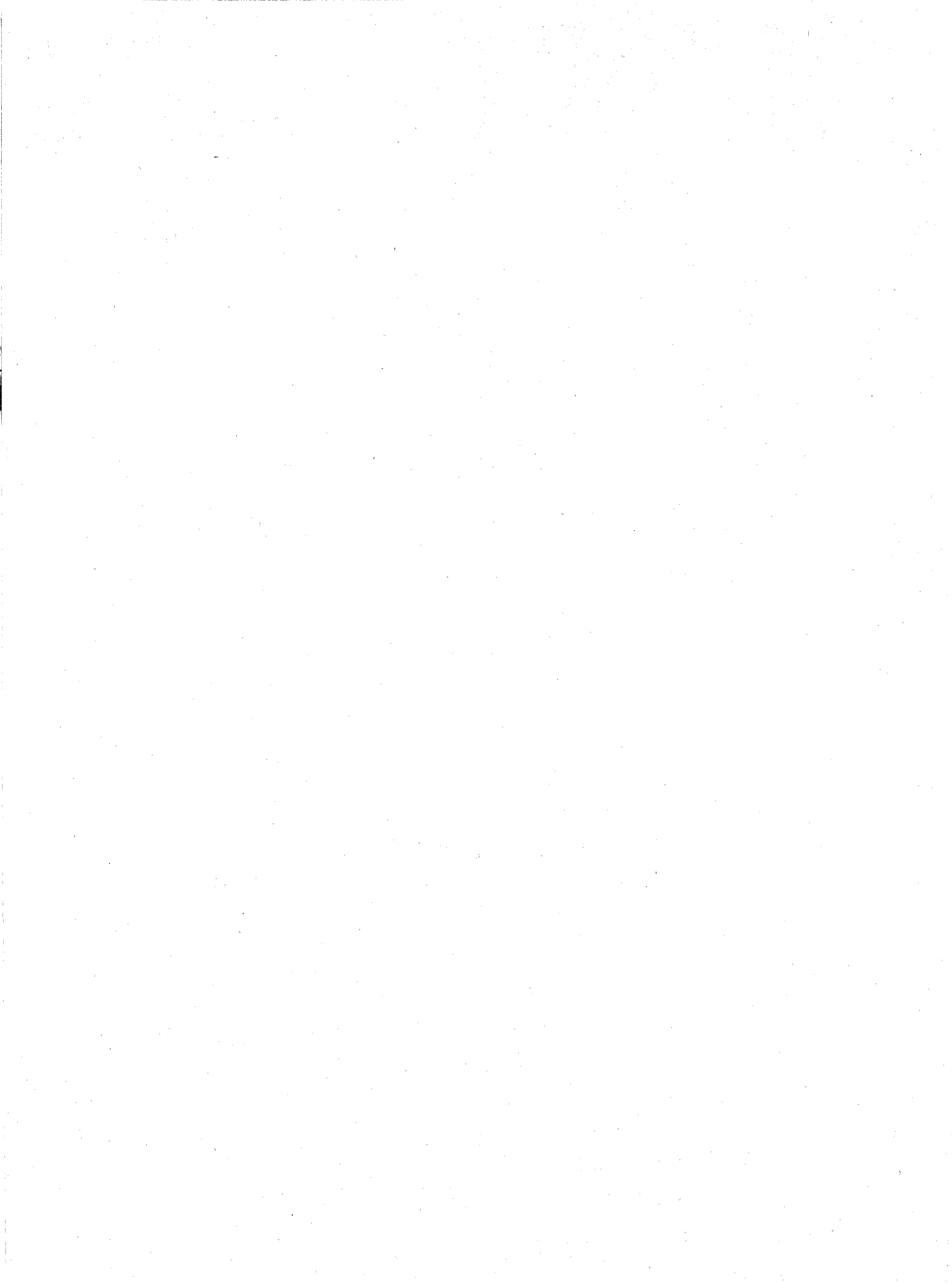
- On-Board Programmability
- Fast Access Time – 500 ns Typ.
- Pin Configuration Similar to the S6830  
1K x 8 Bit ROM
- High Speed Programming – Less than 1 Minute for  
all 4096 Bits
- Programmed with R/W, CS and V<sub>PROG</sub> Pins
- Completely TTL Compatible – Excluding the  
V<sub>PROG</sub> Pin during Read and Write
- Ultraviolet Light Erasable – Less than 10 Minutes
- Static Operation – No Clocks Required
- Three-State Data I/O
- Standard Power Supplies +5V and –12V
- Mature P-Chan Process

### FUNCTIONAL DESCRIPTION

The S6834 is a high speed, static, 512 x 8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24 pin hermetically sealed dual in-line package the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written.

### TYPICAL APPLICATIONS

- ROM Program Debugging
- Code Translation
- Microprogramming
- Look-up Tables
- Random Logic Replacement
- Programmable Waveforms
- Character Generation
- Electronic Keyboards



# 3

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## **AMI 6800 Microcomputer Systems Family**



# The AMI 6800 Microcomputer Systems Family

Part No.	Description	Input/Output	Power Supply (V)	Process	Packages
S6800	Microprocessor, 8-bit (MPU)	TTL	+5V	N-SiGate	C,S,P
S6810	RAM, 128 x 8	TTL	+5V	N-SiGate	S,E,P
S6810-1	RAM, 128 x 8	TTL	+5V	N-SiGate	S,E,P
S6810A	RAM, 128 x 8	TTL	+5V	N-SiGate	S,E,P
S6810A-1	RAM, 128 x 8	TTL	+5V	N-SiGate	S,E,P
S6830	ROM, 1024 x 8	TTL	+5V	N-SiGate	S,E,P
S6831	16,384 Bit Static ROM	TTL	+5V	N-SiGate	S,P
S6834	4096 Bit Static EPROM	TTL	+5, -12V	P-SiGate	C
S6820	Peripheral Interface Adapter (PIA)	TTL	+5V	N-SiGate	S,P,C
S6850	Asynchronous Communications Interface (ACIA)	TTL	+5V	N-SiGate	S,E,P
S2350	Synchronous Receiver/Transmitter (USRT)	TTL	+5V	N-SiGate	S,P,C
S6860	0-600 BPS Digital Modem	TTL	+5V	N-SiGate	P,S
S5204A	4096 Bit Static EPROM	TTL	+5, -12V	P-SiGate	C

## Future Products

### DEPLETION MODE CIRCUITS

S6800 – 8-bit Microprocessor

S6820 – Peripheral Interface Adapter

### INDUSTRIAL TEMPERATURE RANGE

CIRCUITS (-40° to +85°C)

S6800I – 8-bit Microprocessor

S6820I – Peripheral Interface Adapter

S6810I – RAM 128 x 8

### TWO-CHIP MICROCOMPUTER SYSTEM

S6802 – MPU with on-chip 128 x 8 RAM and a clock generator.

S6846 – Input/output with 2K bytes of ROM and a programmable timer.

### PERIPHERAL CIRCUITS

S68488 – General Purpose Bus Interface Circuit – confirms to IEEE 488 specifications.

S6852 – Serial Synchronous Data Adapter – a bus compatible high speed synchronous communications interface.

S6847 – Video Generator Circuit – provides composite video input to a color or monochrome standard TV receiver (used as a low cost graphics terminal).

S6854 – Advanced Data Link Controller – compatible with data link communications standards such as ANSI-ADCCP, IBM-SDLC, and HDLC

S6840 – Programmable Timer Module – provides interval timing for controlling machine interfaces.

# AMI 6800 Microcomputer Hardware and Support Systems

## AMI 6800 Microcomputer Systems Family

*(an LSI family of microcomputer parts, all compatible in signal and load levels, bus protocol, etc.)*

S6800 Microprocessor (MPU) (8-bit Parallel)  
S6810 128 x 8 Static RAM  
S6820 Peripheral Interface Adapter (PIA)  
S6830 1024 x 8 ROM  
S6831 2048 x 8 ROM  
S6834 512 x 8 EPROM  
(Erasable and Reprogrammable)  
S6850 Asynchronous Communications Interface Adapter (ACIA)  
S6860 Digital Modem  
S2350 Universal Synchronous Receiver/Transmitter (USRT)  
SS101 256 x 4 Static CMOS RAM

## Cross-Product and Timesharing Software

*(for AMI 6800 program development on large scale computers and timeshare networks.)*

Cross-Assembler  
(ANSI FORTRAN IV, also available on National CCS timeshare)  
Linking Loader  
(ANSI FORTRAN IV, also available on National CCS timeshare)  
Simulator  
(ANSI FORTRAN IV, also available on National CCS timeshare)

## Prototyping and Evaluation Aids

*(for circuit and program evaluation, design development and simple programming.)*

EVK 300 Prototyping Board  
EVK 200 Prototyping Board Kit  
EVK 100 Prototyping Board Kit  
EVK 99 Prototyping Board Kit

## Applications and Customer Support

Applications Engineering  
Microcomputer Workshops  
and Seminars

## Support Documentation

Hardware Reference Manual  
Assembly Language Programming  
Manual  
Software Data Book  
Product Brochures and Data  
Sheets  
Application Notes



To take full advantage of microcomputers, look to AMI for the superior AMI 6800 family of microcomputer hardware and all the support you need to put it together. AMI offers everything from simple prototyping boards to the resourceful, convenient, and sophisticated Microcomputer Development Center, and some of the most advanced resident and crossproduct software in the industry. AMI offers total support – to make your product design and development task quick, economical, and reliable. It allows you to get your product on the market earlier and thereafter support it better.

### Microcomputer Development Center (MDC)

*(for complete and effective initial hardware and program development and systems integration; for subsequent product hardware and software expansion, customer support, incoming parts testing, and multiple other uses.)*

#### Interface Modules

Quad Flexible Disk Interface  
 RS 232 Interface  
 Current Loop Interface  
 Printer Interface  
 Hi Speed Tape Reader Interface  
 EPROM Programmer AMI 512 x 8  
 General Purpose Peripherals Interface (User Defined)  
 Data Acquisition\* A/D  
 Analog Output\* D/A

#### Peripherals

Dual Disk Controller/ Dual Disk Drive (1 Min/2 Max)  
 TTY/Modem

Matrix Printer  
 Hi Speed Tape Reader

#### Memory Modules

16K Bytes NMOS Dynamic RAM  
 8K Bytes EPROM 8K Bytes ROM

#### Hardware Modules

Debug Extender  
 User Breadboard (Wire-Wrap Terminals)  
 EPROM Programmer AMI 512 x 8  
 Logic Analyzer

#### Software Systems

Disk Operating and File Management System  
 Resident Assembler & Loader  
 Resident Text Editor  
 Debug Control  
 Resident Trace Program  
 Edit & Special Functions Control

\*Planned Extension

# AMI 6800 Microcomputer Systems

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## THE FIRST FAMILY

The AMI S6800 Microcomputer Systems Family is an LSI integrated circuit family for building microcomputers. In its hardware concept it is the same as the SSI and MSI families, except with SSI/MSI each integrated circuit is only an individual logic element (or segment of a larger random logic circuit), whereas in the LSI family each is a whole subsystem of a microcomputer.

By bringing to LSI microcomputer hardware the advantages of the family concept — a series of functionally and electrically matched circuits — the AMI S6800 allows the circuit designer to build complete microcomputer systems of different configurations by simply selecting from the matched subsystem circuits, interconnecting them with the microprocessor into a system, and providing the necessary operating voltages and clock signals. Such a method is superior to choosing an MPU and then matching different memory or I/O circuits to it through interfaces, as must be done with many microprocessor products. The matched LSI family makes the design task simple, fast, and the functional complexity of the system can be increased, while physical size is reduced.

The AMI S6800 Microcomputer Family is a leader in developing this family concept, because S6800 has a wide selection of compatible memory, I/O, and auxiliary circuits, has comprehensive hardware and software support, and wide user acceptance.

## COMPLETE AND EASY

The AMI S6800 Microcomputer Family hardware includes the S6800 Microprocessor, a selection of RAM, ROM, and PROM memories, a wide variety of data input/output circuits, and various other support circuits. These components may be assembled in a building block manner into a simple or complex microcomputer system, for many general and special purpose applications. It remains to the user to integrate the microcomputer into his own larger system and to program it for a specific task.

One important design feature of the S6800 family is that within any microcomputer system all components are directly compatible in the system bus and I/O protocol, as well as in individual signal functions, circuit performance characteristics, and logic levels. All operate on a single +5V power supply.

To facilitate system design and programming, AMI provides versatile and easy to use prototyping hardware, various software packages for program generation, an

economical CRT/disc system for on-site program generation and debugging, comprehensive hardware and software reference documentation, and other applications support. Such backup is a continuous and expanding effort at AMI.

## THE BASIC SYSTEM

A basic S6800 system is shown in Figure 1. In this system the S6800 Microprocessor (MPU) is supported by RAM and ROM (or PROM) memory and controls one input/output circuit. The 1024-byte ROM (or 512-byte erasable PROM) is used to store the operating program, the 128-byte RAM provides working storage for the MPU, and the Peripheral Interface Adapter (PIA) provides two independently programmable 8-bit input/output ports for communicating with two peripheral devices.

The S6800 system is bus oriented. Eight lines form the data bus and 16 more lines make up the address bus. The MPU controls the bus and all other devices — the memories and the PIA — attach to the bus and wait for instructions from the MPU to supply or receive data. In the system shown in Figure 1, the MPU uses address lines A2, A13, and A14 to select one of the three devices on the bus and uses the Read/Write and Valid Memory Address lines to instruct the devices to receive or send data to the MPU. When communicating with the PIA, address lines A0 and A1 are used to select among the two peripheral devices A and B; the CA1, CA2, CB1, and CB2 lines can be used to send out control signals to the peripherals, or receive service requests.

The basic system is a complete microcomputer, which can be used for a large variety of applications. It is simple but versatile. It can be easily reprogrammed by changing the ROM or using the erasable PROM instead. The user must provide only the two-phase clock signal source, a power-up/restart circuit, and a single +5V power supply to complete the hardware.

## AN S6800 SYSTEM EXPANDS GRACEFULLY

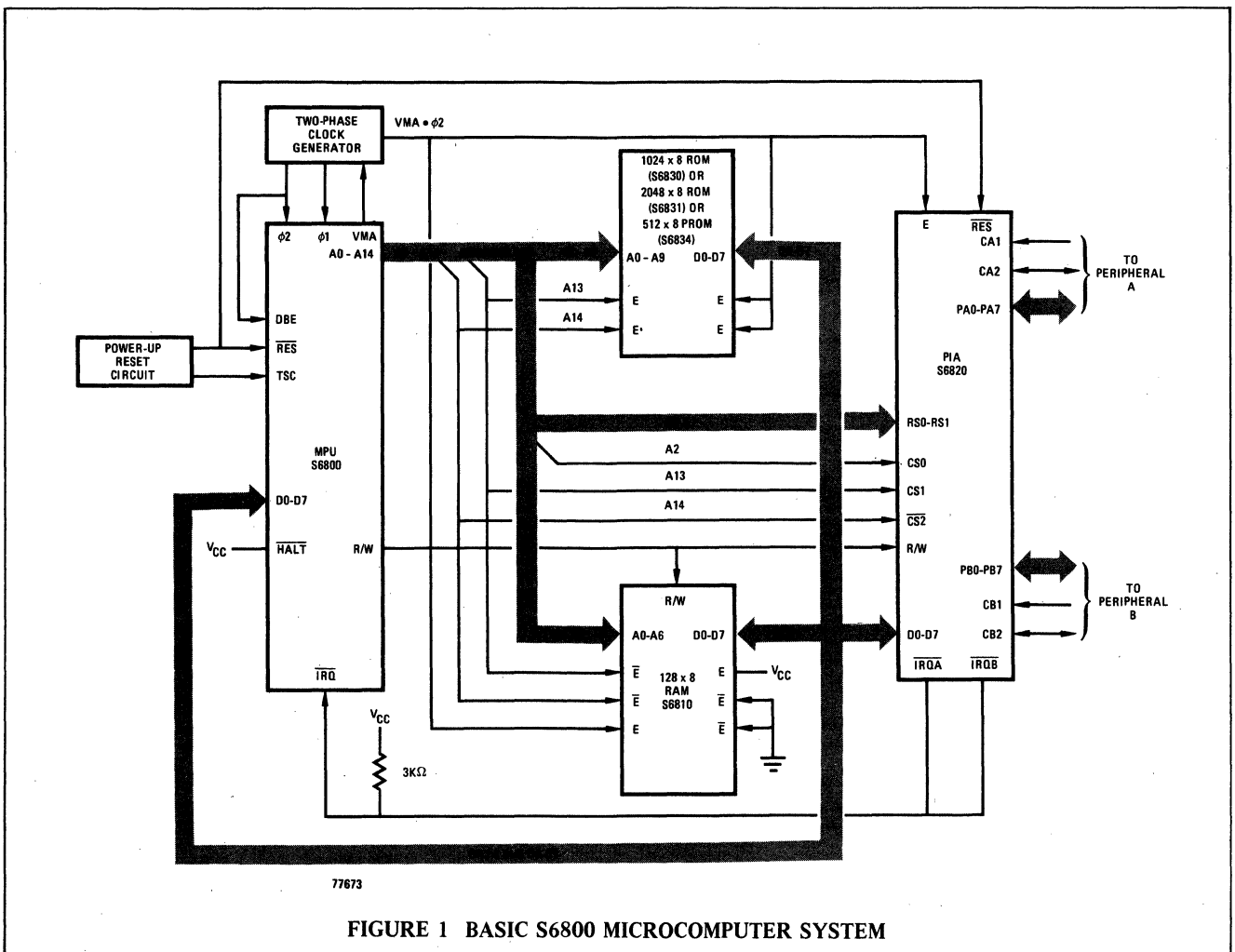
The S6800 Microcomputer Family is easy to expand. It has every one of the basic types of memories — RAM, ROM, and PROM — and all essential forms of interfaces for digital telecommunication and peripherals — serial, parallel, asynchronous, and synchronous. System memory is easy to expand because multiple addressing modes of the MPU make memory access fast and efficient; all I/O devices are designed for operational flexibility and efficiency in MPU cycle

utilization. Memory, I/O, and other devices in the S6800 family are all compatible in load levels and the entire system can run on one common clock. Consequently, you often can eliminate all circuit design, save for the simple clock and power-up/restart circuits.

In general, the system can be expanded in a modular manner by simply connecting the required devices onto the bus. These can be any combination of memory and input/output circuits. In this modular manner a system of nearly any complexity and configuration can be assembled. Because you are designing with a small number of integrated circuits, your circuit layout task is simple and the entire microcomputer can be located on a single circuit card. (Systems with more than ten devices on the bus require the

addition of address and data bus buffers to operate at full speed).

In some special purpose applications you may need to attach your own interface devices to the bus. As a result, more circuit design will be required, but you will find the S6800 MPU easy to work with. It has features that allow it to be used in many different modes of operation and in various systems. For example, by using the Halt, Three State Control, and Data Bus Enable lines you can easily design a direct memory access system, in which either the MPU or a peripheral device can read or write into the RAM and utilize the bus on a priority basis. You can also design a multi-processor system, in which several MPUs are attached to the same bus and share processing assignments, as well as memory space.



## S6800 INPUT/OUTPUT

One other important advantage that S6800 has to offer in comparison with any other microcomputer system is input/output versatility. In any computer system, large or small, the CPU internal functions are determined by its architecture and the user usually has little opportunity or need to alter them. On the other hand, the I/O configuration is almost always determined by the user and subject to change as peripherals are added or other system alterations are introduced. The I/O configuration is important to the user because it affects the efficiency of the CPU itself, determines the ease and speed with which peripherals can interact with the system and determines the throughput rate of the system.

Therefore, the efficiency and versatility with which a CPU can handle its I/O — both in hardware and software — is an important criteria and of particular concern to the user. It is in this area that the S6800 MPU excels.

- In an S6800 system, the MPU relegates most of the I/O control to such I/O interfaces as the PIA or ACIA. Each of these circuits is programmable and can interface with peripheral devices without directly involving the MPU. For example, the MPU can preprogram a PIA to either input data into the MPU or to receive it. Thereafter, the PIA circuits assume all functions of interfacing with the peripherals and the MPU never has to look at the interface until service is required. It must service interrupts from the PIA, but never needs to wait for input data to become available or for output data to be accepted. This relieves the MPU of its I/O functions, makes it more efficient in its primary task of data processing, and significantly increases system throughput.

- The I/O interfaces and memory are both located in the same address space within the S6800 system. The MPU can access any I/O device the same as a memory location — with address lines, instead of separate I/O control lines. Therefore, it can manipu-

late data in the I/O interface registers with the same programmed instructions as it uses for memory locations. This adds programming flexibility and increases system efficiency.

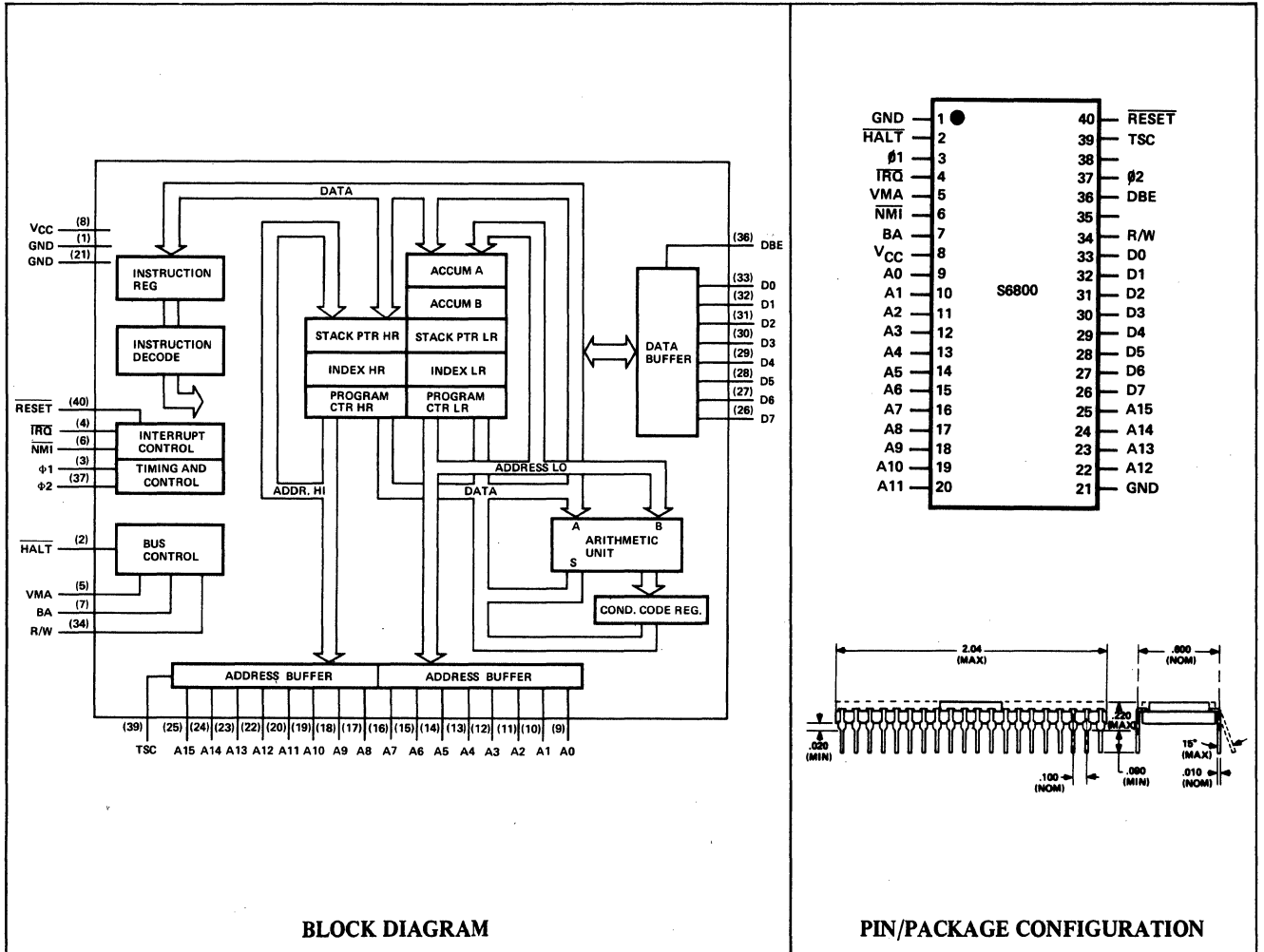
- The S6800 Instruction Set complements the above I/O addressing capability with specific instructions that can be used to access memory as well as I/O circuit registers and perform directly various manipulations on the data.

## S6800 INSTRUCTION SET

The S6800 MPU has a set of 72 basic instructions. These include binary and decimal arithmetic functions, as well as logical, shift, rotate, load, store, branch, interrupt, and stack manipulation functions. Most of the instructions have several variations and most can be used with several memory addressing modes. Thus, the total complex of instructions available to the programmer actually is 197.

An instruction can be from one to three bytes long, depending on the addressing mode used with the instruction. In single byte instructions no memory address is required because the operation is performed on one of the internal MPU registers. In multiple byte instructions the second and third byte can be the operand, or a memory address for the operand.

A noteworthy feature of the S6800 MPU is that some of the instructions can operate directly on any memory location. In most computer systems it is common that the processor fetches an operand from memory, stores it in the accumulator, then executes the operation in the ALU, and finally writes the result back into the memory. The S6800 is able to accomplish the same with only a single instruction, because it operates with any external location in the same manner as with an internal register. For example, it can directly increment or decrement the contents of a memory location. Because the MPU addresses I/O devices just like a memory location, it can do the same with registers inside the PIA or ACIA.



## FEATURES

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus – 65536 Bytes of Addressing
- 72 Instructions – Variable Length
- Seven Addressing Modes – Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- 2 Microsecond Instruction Execution
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt – Internal Registers Saved in Stack
- Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Access (DMA) and Multiple Processor Capability
- Clock Rates as High as 1 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage $V_{CC}$	-0.3 to +7.0V
Input Voltage $V_{in}$	-0.3 to +7.0V
Operating Temperature Range $T_A$	0 to +70°C
Storage Temperature Range $T_{stg}$	-55 to +150°C

**DC (STATIC) CHARACTERISTICS**

( $V_{CC} = 5.0\text{ V} \pm 5\%$ ,  $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels) Logic $\phi 1, \phi 2$	$V_{IH}$ $V_{IHC}$	+ 2.4 $V_{CC} - 0.3$	— —	$V_{CC}$ $V_{CC} + 0.1$	Vdc
Input Low Voltage (Normal Operating Levels) Logic $\phi 1, \phi 2$	$V_{IL}$ $V_{ILC}$	-0.3 -0.1	— —	+ 0.4 +0.3	Vdc
Clock Overshoot/Undershoot – Input High Level – Input Low Level	$V_{OS}$	$V_{CC} - 0.5$ -0.5	— —	$V_{CC} + 0.5$ +0.5	Vdc
Input High Threshold Voltage $\overline{\text{Reset}}, \overline{\text{NMI}}, \overline{\text{Halt}}, \overline{\text{IRQ}}, \text{Data}$	$V_{IHT}$	+ 2.0	—	—	Vdc
Input Low Threshold Voltage $\overline{\text{Reset}}, \overline{\text{NMI}}, \overline{\text{Halt}}, \overline{\text{IRQ}}, \text{Data}$	$V_{ILT}$	—	—	+ 0.8	Vdc
Input Leakage Current ( $V_{in} = 0$ to 5.25 V, $V_{CC} = 5.25\text{V}$ ) Logic* $\phi 1, \phi 2$	$I_{in}$	— —	— —	2.5 100	$\mu\text{Adc}$
Three-State (Off State) Input Current ( $V_{in} = 0.4$ to 2.4 V, $V_{CC} = \text{max}$ ) Data A0-A15, R/W	$I_{TSI}$	— —	— —	10 100	$\mu\text{Adc}$
Output High Voltage ( $I_{Load} = -100\ \mu\text{Adc}$ , $V_{CC} = \text{min}$ )	$V_{OH}$	+ 2.4	—	—	Vdc
Output Low Voltage ( $I_{Load} = 1.6\ \text{mAdc}$ , $V_{CC} = \text{min}$ )	$V_{OL}$	—	—	+ 0.4	Vdc
Power Dissipation	$P_D$	—	0.600	1.2	W
Capacitance** ( $V_{in} = 0$ , $T_A = 25^\circ\text{C}$ , $f = 1.0\ \text{MHz}$ ) Logic Data, TSC $\phi 1, \phi 2$ A0-A15, R/W	$C_{in}$   $C_{out}$	— — 80	— — 120	10 15 160 12	pF   pF

\*Except IRQ and NMI, which require 3 k $\Omega$  pullup load resistors for wire-OR capability at optimum operation.

\*\*Capacitances are periodically sampled rather than 100% tested.

### AC (DYNAMIC) CHARACTERISTICS

( $V_{CC} = 5.0 \text{ volt} \pm 5\%$ ,  $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min.	Typ	Max.	Unit
Frequency of Operation	f	0.1	—	1.0	MHz
Clock Timing for 1-MHz Operation (Figure 1) ( $C_{\text{clock}} = 200 \text{ pF}$ ) Cycle Time	$t_{\text{cyc}}$	1.0	—	10	$\mu\text{s}$
Clock Pulse Width (Measured at $V_{CC} - 0.3 \text{ V}$ ) $\phi 1$ $\phi 2$	$PW_{\phi H}$	430 450	— —	4500 4500	ns
Total $\phi 1$ and $\phi 2$ UP Time	$t_{\text{ut}}$	940	—	—	ns
Rise and Fall Times $\phi 1, \phi 2$ (Measured between 0.3 V and $V_{CC} - 0.3 \text{ V}$ )	$t_r, t_f$	5.0	—	50	ns
Delay Time or Clock Overlap (Measured at 0.5 V)	$t_d$	0	—	9100	ns
Overshoot/Undershoot Duration	$t_{\text{os}}$	0	—	40	ns

### READ/WRITE TIMING

Figures 2 and 3,  $f = 1.0 \text{ MHz}$ , Loading = 130 pF and one TTL Load except VMA and BA Loading = 30 pF and one

Characteristic	Symbol	Min.	Typ	Max.	Unit
Read/Write Setup Time from MPU	$T_{\text{ASR}}$	—	100	300	ns
Address Setup Time from MPU	$T_{\text{ASC}}$	—	200	300	ns
Memory Read Access Time $t_{\text{cyc}} - (T_{\text{ASC}} + T_{\text{DSU}} + t_r)$	$T_{\text{ACC}}$	—	—	575	ns
Data Setup Time	$T_{\text{DSU}}$	100	—	—	ns
Address Setup Time from MPU for VMA	$T_{\text{VSC}}$	—	150	300	ns
Data Hold Time	$T_{\text{H}}$	10	30	—	ns
Enable High Time for DBE Input	$T_{\text{EH}}$	470	—	—	ns
Data Setup Time from MPU	$T_{\text{ASD}}$	—	150	200	ns

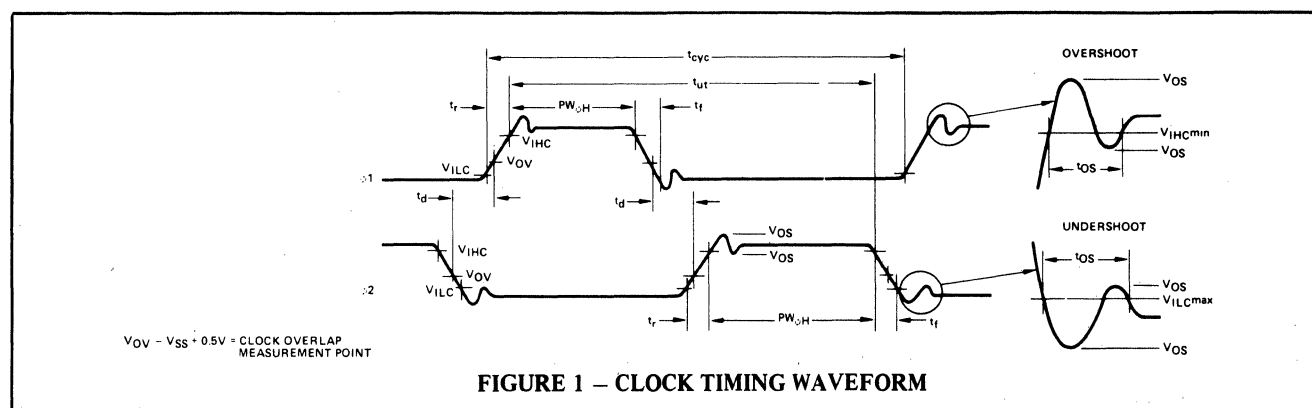


FIGURE 2 – READ DATA FROM MEMORY OR PERIPHERALS

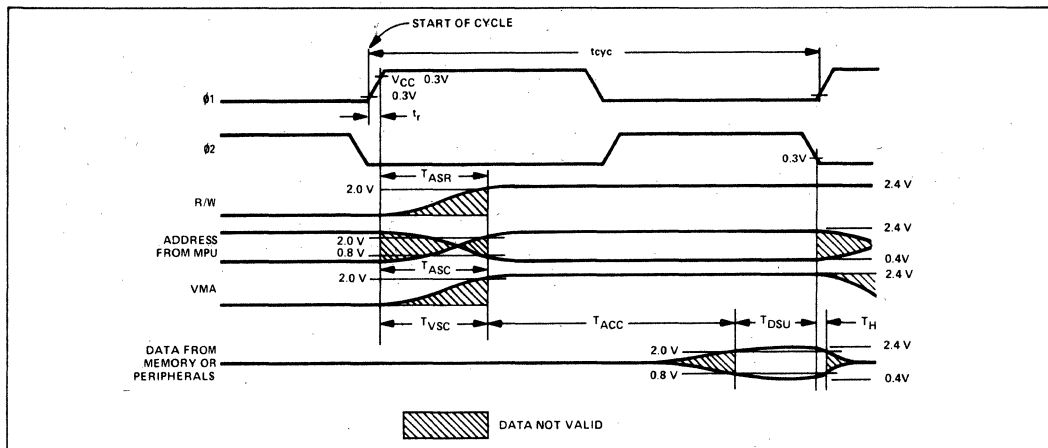
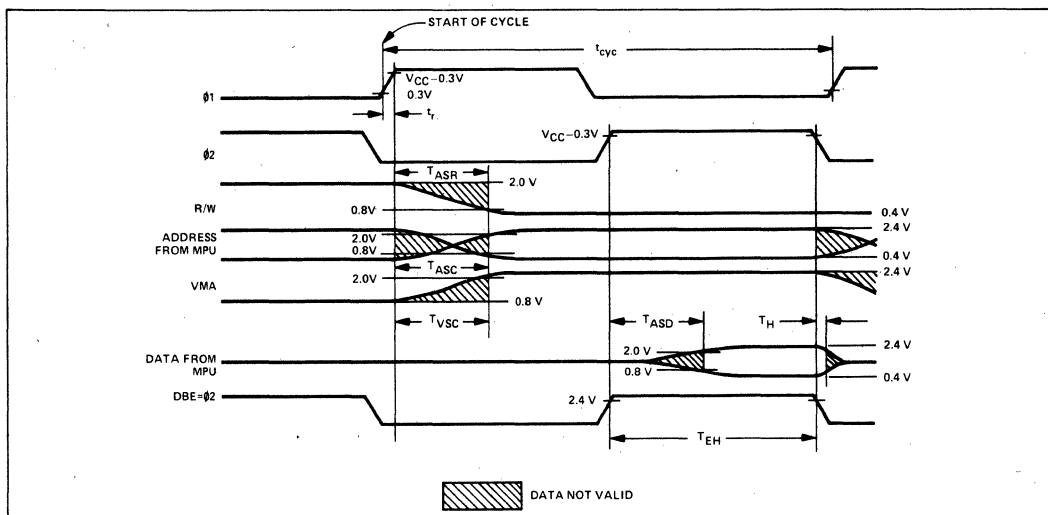


FIGURE 3 – WRITE DATA IN MEMORY OR PERIPHERALS

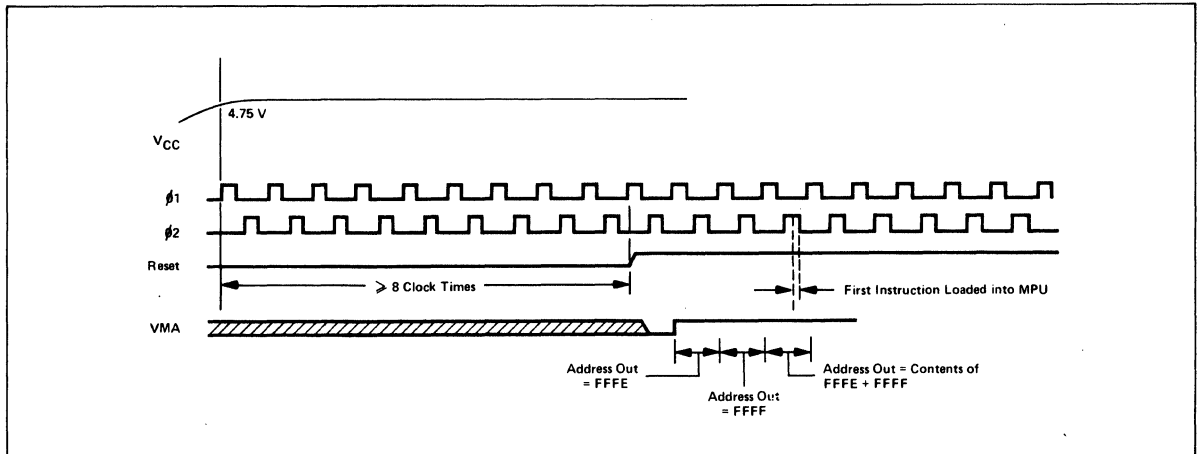


INTERFACE DESCRIPTION

Pin	Label	Function
$\phi 1$	(3)	Clocks Phase One and Phase Two – Two pins are used for a two-phase non-overlapping clock that runs at the VCC voltage level.
$\phi 2$	(37)	
$\overline{\text{RESET}}$	(40)	<b>Reset</b> – This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$ .  Reset must be held low for at least eight clock periods after VCC reaches 4.75 volts (Figure 4). If $\overline{\text{RESET}}$ goes high prior to the leading edge of $\phi 2$ , on the next $\phi 1$ the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.



FIGURE 4 INITIALIZATION OF MPU AFTER RESTART



INTERFACE DESCRIPTION (CONT'D)

Pin	Label	Function
VMA	(5)	<b>Valid Memory Address</b> – This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 30 pF may be directly driven by this active high signal.
A0 • • • A15	(9)    (25)	<b>Address Bus</b> – Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130 pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.
TSC	(39)	<b>Three-State Control</b> – This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 500 ns after TSC = 2.4 V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The phi1 clock must be held in the high state and the phi2 in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 5.0 μs or destruction of data will occur in the MPU.
D0 • • D7	(33)   (26)	<b>Data Bus</b> – Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load at 130 pF.
DBE	(36)	<b>Data Bus Enable</b> – This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it can be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.
R/W	(34)	<b>Read/Write</b> – This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the off (high-impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 130 pF.

INTERFACE DESCRIPTION (CONT'D)

Pin	Label	Function
$\overline{\text{HALT}}$	(2)	<p><b><math>\overline{\text{Halt}}</math></b> – When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction. Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode.</p> <p>Transition of the <math>\overline{\text{Halt}}</math> line must not occur during the last 250 ns of phase one. To insure single instruction operation, the <math>\overline{\text{Halt}}</math> line must go high for one Phase One Clock cycle.</p>
BA	(7)	<p><b>Bus Available</b> – The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the <math>\overline{\text{Halt}}</math> line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.</p>
$\overline{\text{IRQ}}$	(4)	<p><b>Interrupt Request</b> – This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.</p> <p>The <math>\overline{\text{Halt}}</math> line must be in the high state for interrupts to be recognized.</p> <p>The <math>\overline{\text{IRQ}}</math> has a high impedance pullup device internal to the chip; however a 3 k<math>\Omega</math> external resistor to VCC should be used for wire-OR and optimum control of interrupts.</p>
$\overline{\text{NMI}}$	(6)	<p><b>Non-Maskable Interrupt</b> – A low-going edge on this input requests that a non-mask interrupt sequence be generated within the processor. As with the <math>\overline{\text{Interrupt Request}}</math> signal, the processor will complete the current instruction that is being executed before it recognizes the <math>\overline{\text{NMI}}</math> signal. The interrupt mask bit in the Condition Code Register has no effect on <math>\overline{\text{NMI}}</math>. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away in the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.</p> <p><math>\overline{\text{NMI}}</math> has a high impedance pullup resistor internal to the chip; however a 3 k<math>\Omega</math> external resistor to VCC should be used for wire-OR and optimum control of interrupts.</p> <p>Inputs <math>\overline{\text{IRQ}}</math> and <math>\overline{\text{NMI}}</math> are hardware interrupt lines that are acknowledged during <math>\phi_2</math> and will start the interrupt routine on the <math>\phi_1</math> following the completion of an instruction.</p> <p><b>INTERRUPTS</b> – As outlined in the interface description the S6800 requires a 16-bit vector address to indicate the location of routines for Restart, Non-maskable Interrupt, and Maskable Interrupt. Additionally an address is required for the Software Interrupt Instruction (SWI). The processor assumes the uppermost eight memory locations, FFF8 – FFFF, are assigned as interrupt vector addresses as defined in Figure 5.</p> <p>After completing the current instruction execution the processor checks for an allowable interrupt request via the <math>\overline{\text{IRQ}}</math> or <math>\overline{\text{NMI}}</math> inputs as shown by the simplified flow chart in Figure 6. Recognition of either external interrupt request or a Wait for Interrupt (WAI) or Software Interrupt (SWI) instruction causes the contents of the Index Register, Program Counter, Accumulators and Condition Code Register to be transferred to the stack as shown in Figure 7.</p>

FIGURE 5 MEMORY MAP FOR INTERRUPT VECTORS

Vector		Description
MS	LS	
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request

FIGURE 6 – MPU FLOW CHART

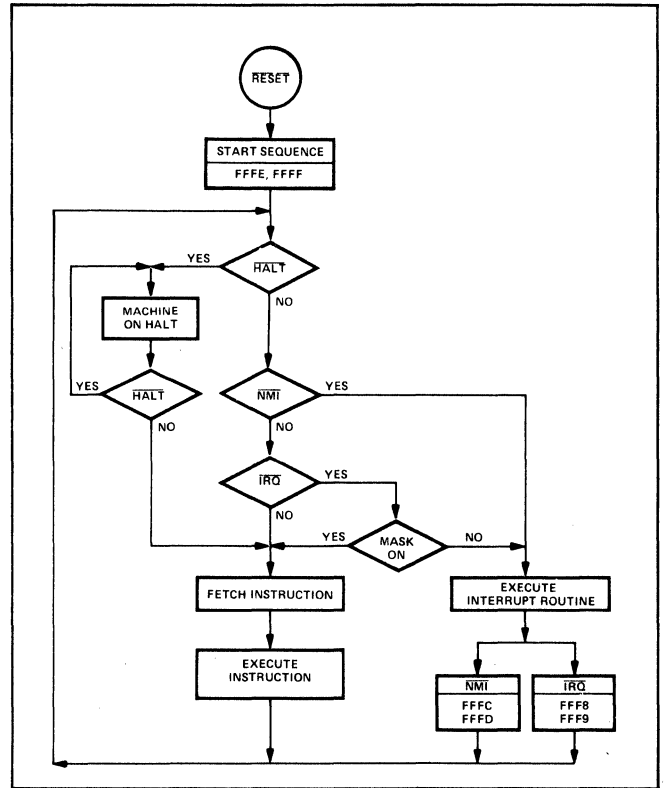


FIGURE 7 – SAVING THE STATUS OF THE MICROPROCESSOR IN THE STACK

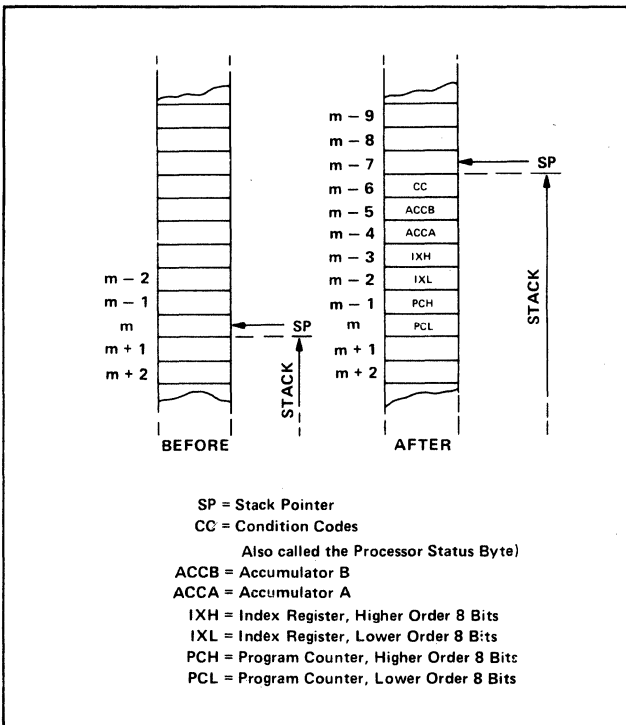
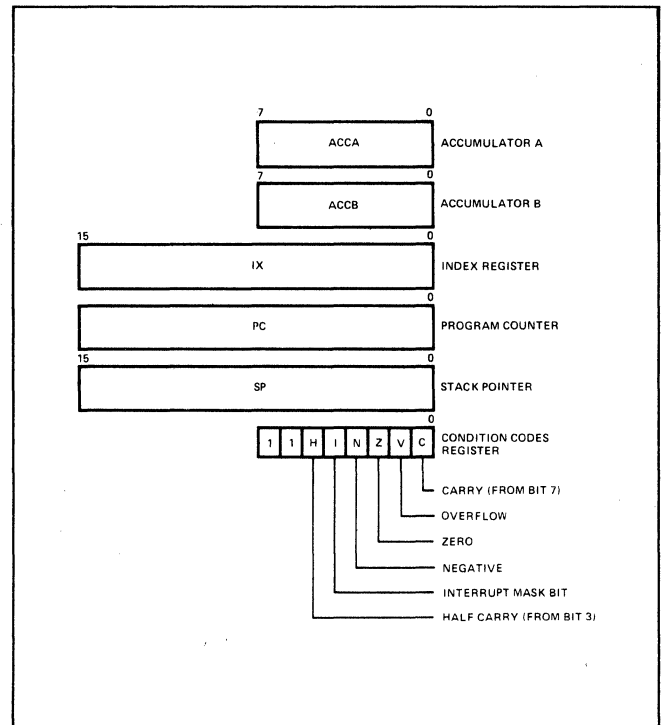


FIGURE 8 – PROGRAMMING MODEL OF THE MICROPROCESSOR



## MPU REGISTERS

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer.

**Program Counter** – The program counter is a two byte (16-bits) register that points to the current program address.

**Stack Pointer** – The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

**Index Register** – The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

**Accumulators** – The MPU contains two 8-bit accumulators that are used to hold operands and results from the arithmetic logic unit (ALU).

**Condition Code Register** – The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

## MPU ADDRESSING MODES

The S6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Figure 9 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

### ACCUMULATOR ADDRESSING (ACCX)

OP CODE
---------

A single byte instruction addressing operands only in accumulator A or accumulator B.

### IMPLIED ADDRESSING

OP CODE
---------

Single byte instruction where the operand address is implied by the instruction definition (i.e., Stack Pointer, Index Register or Condition Register).

### IMMEDIATE ADDRESSING

OP CODE	IMMEDIATE OPERAND
HIGHER	IMMEDIATE OPERAND LOWER

Two or three byte instructions with an eight or sixteen bit operand respectively. For accumulator operations the eight bit operand is contained in the second byte of a two byte instruction. For Index Register operations (e.g. LDX) sixteen bit operand is contained in the second and third byte of a three byte instruction.

### DIRECT ADDRESSING

OP CODE	ADDRESS 0-255
---------	---------------

Two byte instructions with the address of the operand contained in the second byte of the instruction. This format allows direct addressing of operands within the first 256 memory locations.

### EXTENDED ADDRESSING

OP CODE	ADDRESS HIGHER	ADDRESS LOWER
---------	----------------	---------------

Three byte instructions with the higher eight bits of the operand address contained in the second byte and the lower eight bits of address contained in the third byte of the instruction. This format allows direct addressing of all 65,536 memory locations.

### INDEXED ADDRESSING

OP CODE	INDEX ADDRESS
---------	---------------

Two byte instructions where the 8 bit unsigned address contained in the second byte of the instruction is added to the sixteen bit Index Register resulting in a sixteen bit effective address. The effective address is stored in a temporary register and the contents of the Index Register are unchanged.

### RELATIVE ADDRESSING

OP CODE	RELATIVE ADDRESS
---------	------------------

Two byte instructions where the relative address contained in the second byte of the instruction is added to the sixteen bit program counter plus two. The relative address is interpreted as a two's complement number allowing relative addressing within a range of -125 to +129 bytes of the present instruction.





FIGURE 9 S6800 INSTRUCTION SET (CONT'D)

Instruction	Mnemonic	Addressing Modes						Boolean/Arith Operation	Condition Reg.												
		Implied		Direct		Immediate			Extended		Indexed		Relative		5	4	3	2	1	0	
		OP	MC	PB	OP	MC	PB		OP	MC	PB	OP	MC	PB	OP	MC	PB	H	I	N	Z
Branch to subroutine	BSR											8D	8	2	} See Special Operations	•	•	•	•	•	•
Jump to subroutine	JSR						BD	9	3	AD	8	2	•	•		•	•	•	•		
Jump	JMP						7E	3	3	6E	4	2	•	•		•	•	•	•		
Return from subroutine	RTS	39	5	1										•		•	•	•	•	•	
Return from interrupt	RTI	3B	10	1										Note 10		•	•	•	•	•	•
Software interrupt	SWI	3F	12	1										•		•	•	•	•	•	
Wait for interrupt	WAI	3E	9	1										•		•	•	•	•	•	
No operation	NOP	02	2	1										•		•	•	•	•	•	
Clear	CLRA	4F	2	1										00 → A		•	•	R	S	R	R
	CLRB	5F	2	1										00 → B		•	•	R	S	R	R
	CLR						7F	6	3	6F	7	2			00 → M	•	•	R	S	R	R
Clear carry	CLC	0C	2	1										0 → C	•	•	•	•	•	R	
Clear interrupt mask	CLI	0E	2	1										0 → I	•	R	•	•	•	•	
Clear overflow	CLV	0A	2	1										0 → V	•	•	•	•	R	•	
Set carry	SEC	0D	2	1										1 → C	•	•	•	•	•	S	
Set interrupt mask	SEI	0F	2	1										1 → I	•	S	•	•	•	•	
Set overflow	SEV	0B	2	1										1 → V	•	•	•	•	S	•	

CONDITION CODE SYMBOLS:

- H Half-carry from bit 3;
- I Interrupt mask
- N Negative (sign bit)
- Z Zero (byte)
- V Overflow, 2's complement
- C Carry from bit 7
- R Reset Always
- S Set Always
- † Test and set if true, cleared otherwise
- Not Affected

LEGEND:

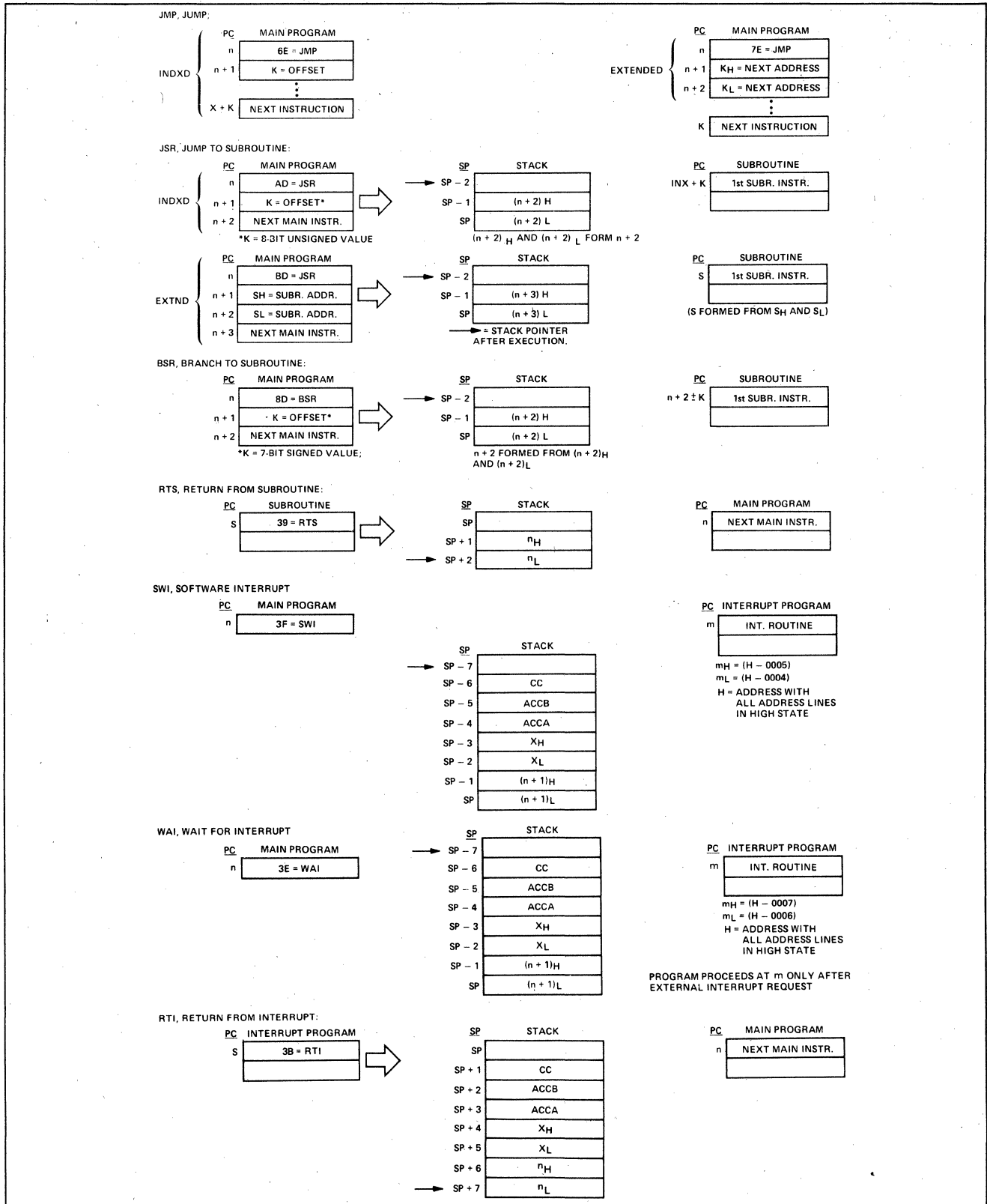
- OP Operation Code (Hexadecimal);
- MC Number of MPU Cycles;
- PB Number of Program Bytes;
- + Arithmetic Plus;
- Arithmetic Minus;
- Boolean AND;
- M<sub>SP</sub> Contents of memory location pointed to by Stack Pointer;
- + Boolean Inclusive OR;
- ⊕ Boolean Exclusive OR;
- M Complement of M;
- Transfer Into;
- 0 Bit = Zero;
- 00 Byte = Zero;

Note - Accumulator addressing mode instructions are included in the IMPLIED addressing.

CONDITION CODE REGISTER NOTES:

- (Bit set if test is true and cleared otherwise)
- 1 (Bit V) Test: Result = 10000000?
- 2 (Bit C) Test: Result = 00000000?
- 3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
- 4 (Bit V) Test: Operand = 10000000 prior to execution?
- 5 (Bit V) Test: Operand = 01111111 prior to execution?
- 6 (Bit V) Test: Set equal to result of N \* C after shift has occurred.
- 7 (Bit N) Test: Sign bit of most significant (MS) byte = 1?
- 8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
- 9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
- 10 (All) Load Condition Code Register from Stack. (See Special Operations)
- 11 (Bit I) Set when interrupt occurs, if previously set, a Non-Maskable Interrupt is required to exit the wait state.
- 12 (ALL) Set according to the contents of Accumulator A

SPECIAL OPERATIONS





**SYSTEMS OPERATION**

To demonstrate the great versatility of the functional building block concept, a typical system configuration is shown. This configuration will demonstrate how easily a basic system may be upgraded and expanded for a number of different applications.

The Microprocessing Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system (Figure 10). Such a system can easily be adapted for a number of small scale applications by simply changing the content of the ROM.

**TWO-PHASE CLOCK CIRCUITRY AND TIMING**—The MPU requires a two-phase non-overlapping clock which has a frequency range as high as 1 MHz. In addition to the two phases, this circuit should also generate an enable signal E, and its complement  $\bar{E}$ , to enable ROMs, RAMs, PIAs and ACIAs. This Enable signal and its complement is obtained by ANDing  $\phi 2$  and VMA (Valid Memory Address).

**CHIP SELECTION AND ADDRESSING**—The minimum system configuration permits direct selection of the ROM, RAM, ACIA and PIA without the use of special TTL select logic. This is accomplished by simply wiring the address lines A13 and A14 to the Enable or chip select lines on the memories and PIA. This permits the devices to be addressed as follows:

Device	A14	A13	Hex Addresses
RAM	0	0	0000–007F
PIA	0	1	2004–2007 (Registers)
ROM	1	1	6000–63FF

Other addressing schemes can be utilized which use any combination of two of the lines A10 through A14 for chip selection.

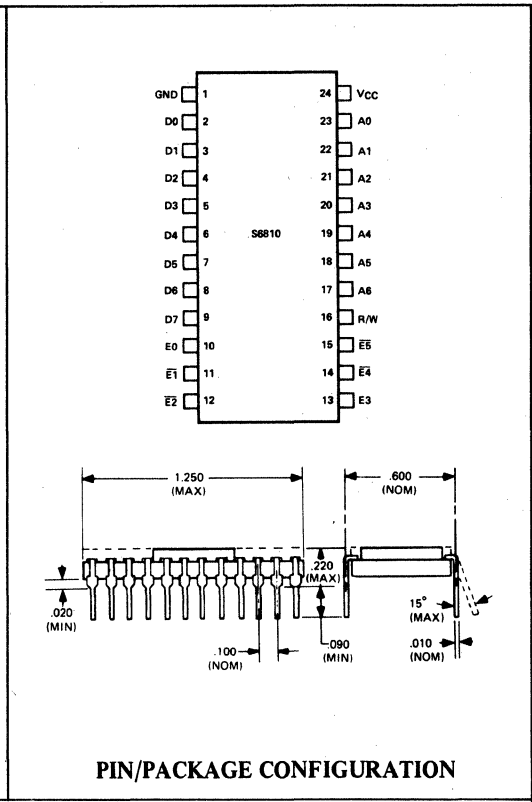
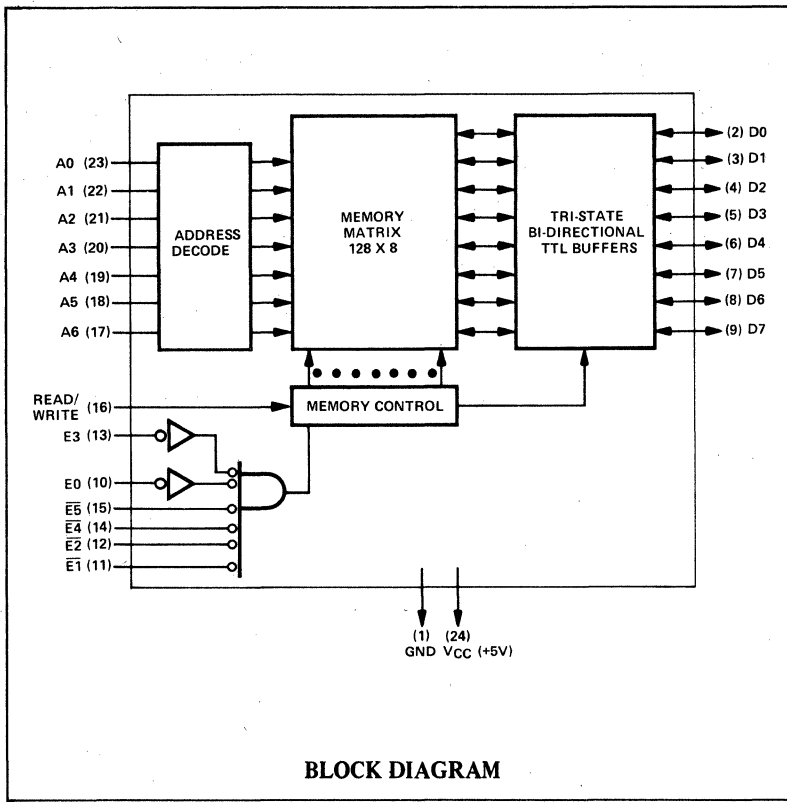
**PERIPHERAL CONTROL**—All control and timing for the peripherals that are connected to the PIA is accomplished by software routines under the control of the MPU.

**RESTART AND NON-MASKABLE INTERRUPT**—Since this basic system does not have a nonvolatile RAM, special circuitry to handle loss of power using NMI is not required. Circuitry is, however, required to insure proper initialization of the MPU when power is turned on. This circuit should insure that the Restart signal is held low for eight  $\phi 1$  clock cycles after the VCC power supply reaches a voltage of approximately 4.75 volts DC. Also, in order to insure that a PIA or ACIA is not inadvertently selected during the power-on sequence, Three-State Control (TSC) should be held high until the positive transition of Restart.

**HALT**—The  $\bar{\text{Halt}}$  line is tied to VCC and will automatically place the MPU in the run state when power is turned on. This signal may be used to halt the MPU if a switch is used to tie the line to ground for HALT and to VCC for RUN.

# S6810

128 X 8 STATIC  
READ/WRITE MEMORY



### FEATURES

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Six Chip Enable Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 1.0 $\mu$ s for S6810  
575 ns for S6810-1

### FUNCTIONAL DESCRIPTION

The S6810 is a static 128 x 8 Read/Write Memory designed and organized to be compatible with the S6800 Micro-processor. Interfacing to the S6810 consists of an 8 Bit Bi-directional Data Bus, Seven Address Lines, a single Read/Write

Control line, and six Chip Enable lines, four negative and two positive.

For ease of use, the S6810 is a totally static memory requiring no clocks or cell refresh. The S6810 is fabricated with N channel silicon gate technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage $V_{CC}$	-0.3 to +7.0V
Input Voltage $V_{in}$	-0.3 to +7.0V
Operating Temperature Range $T_A$	0 to +70°C
Storage Temperature Range $T_{stg}$	-55 to +150°C

### DC (STATIC) CHARACTERISTICS

( $V_{CC} = 5.0 \text{ Volt} \pm 5\%$ ;  $T_A = 25^\circ\text{C}$  unless otherwise noted)

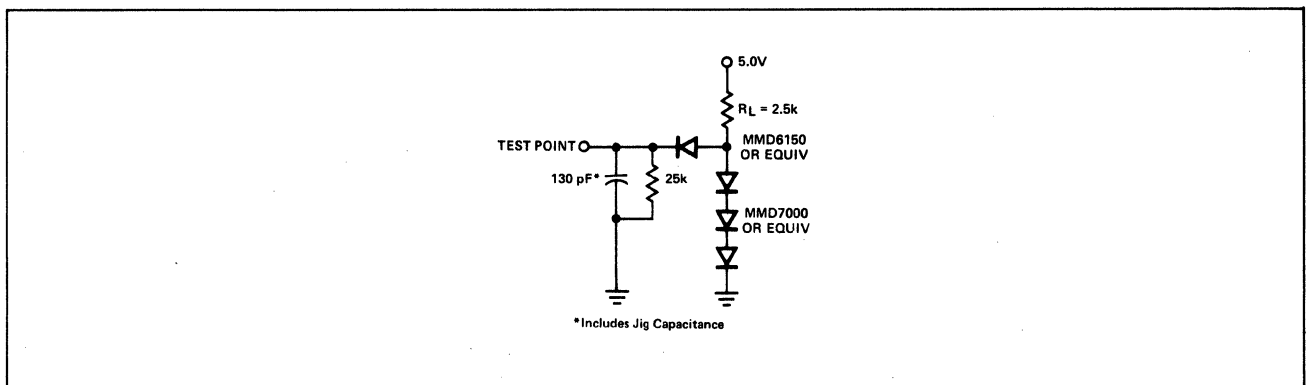
Characteristic	Symbol	Min.	Typ.	Max.	Unit	Condition
Input High Voltage (Normal Operating Levels)	$V_{IH}$	2.4	—	5.25	V	
Input Low Voltage (Normal Operating Levels)	$V_{IL}$	-0.3	—	0.4	V	
Input Current ( $A_n, R/W, E_n, \bar{E}_n$ ) ( $V_{in} = 0$ to $5.25 \text{ V}$ )	$I_{in}$	—	—	2.5	$\mu\text{A}$	
Input High Threshold Voltage	$V_{IHT}$	2.0	—	—	V	
Input Low Threshold Voltage	$V_{ILT}$	—	—	0.8	V	
Output High Voltage ( $I_{OH} = -100 \mu\text{A}$ )	$V_{OH}$	2.4	—	—	V	
Output Low Voltage ( $I_{OL} = 1.6 \text{ mA}$ )	$V_{OL}$	—	—	0.4	V	
Output Leakage Current ( $D0 - D7$ ) ( $V_O = 2.4 \text{ V}, E = 0.4 \text{ V}, \bar{E} = 2.4 \text{ V}$ )	$I_{LIH}$	—	—	10	$\mu\text{A}$	
Output Leakage Current ( $D0 - D7$ ) ( $V_O = 0.4 \text{ V}, E = 0.4 \text{ V}, \bar{E} = 2.4 \text{ V}$ )	$I_{LOL}$	—	—	10	$\mu\text{A}$	
Supply Current ( $V_{CC} = 5.25 \text{ V}, T_A = 0^\circ\text{C}$ )	$I_{CC}$	—	—	130	mA	
Input Capacitance	$C_{IN}$	—	—	7.5	pF	$f = 1.0\text{MHz}, T_A = 25^\circ\text{C}$
Output Capacitance	$C_{OUT}$	—	—	15	pF	

### AC (DYNAMIC) CHARACTERISTICS

( $V_{CC} = 5.0 \text{ Volt} \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Characteristic	Symbol	Min.	Max.	Unit
Address Setup Time	$t_{AS}$	30	—	ns
Address Hold Time	$t_{AH}$	0	—	ns
Chip Enable Pulse Width	$t_{CS}$	800 400	—	ns

FIGURE 1 – AC TEST LOAD



**READ CYCLE**

(All timing with  $t_r = t_f = 20$  ns, Load of Figure 1)

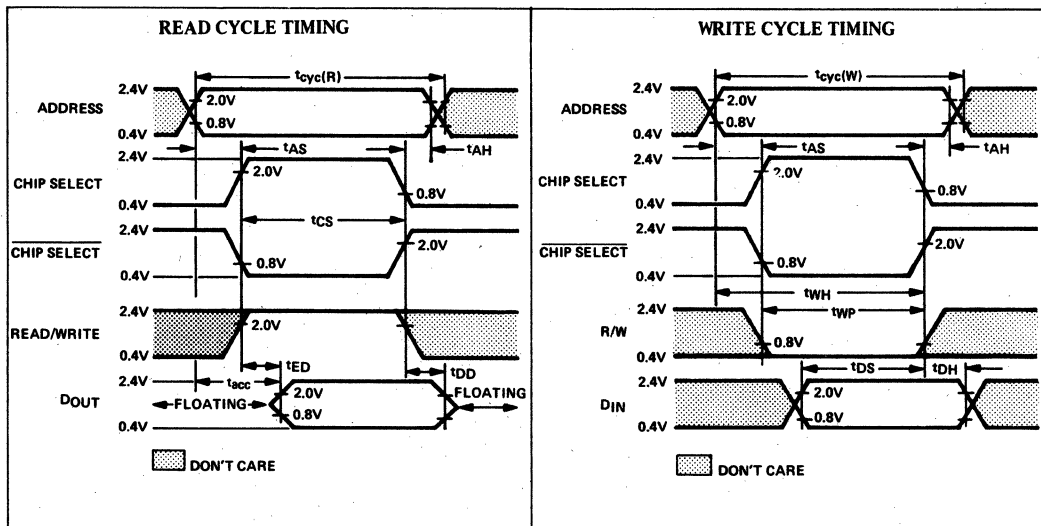
Characteristic		Symbol	Min.	Max.	Unit
Read Cycle Time	S6810	$t_{cyc}(R)$	1000	—	ns
	S6810-1		575	—	ns
Output Enable Delay Time	S6810	$t_{ED}$	—	400	ns
	S6810-1		—	300	ns
Output Disable Delay Time	S6810	$t_{DD}$	10	200	ns
	S6810-1		10	150	ns
Read Access Time	S6810	$t_{acc}$	—	1000	ns
	S6810-1		—	575	ns

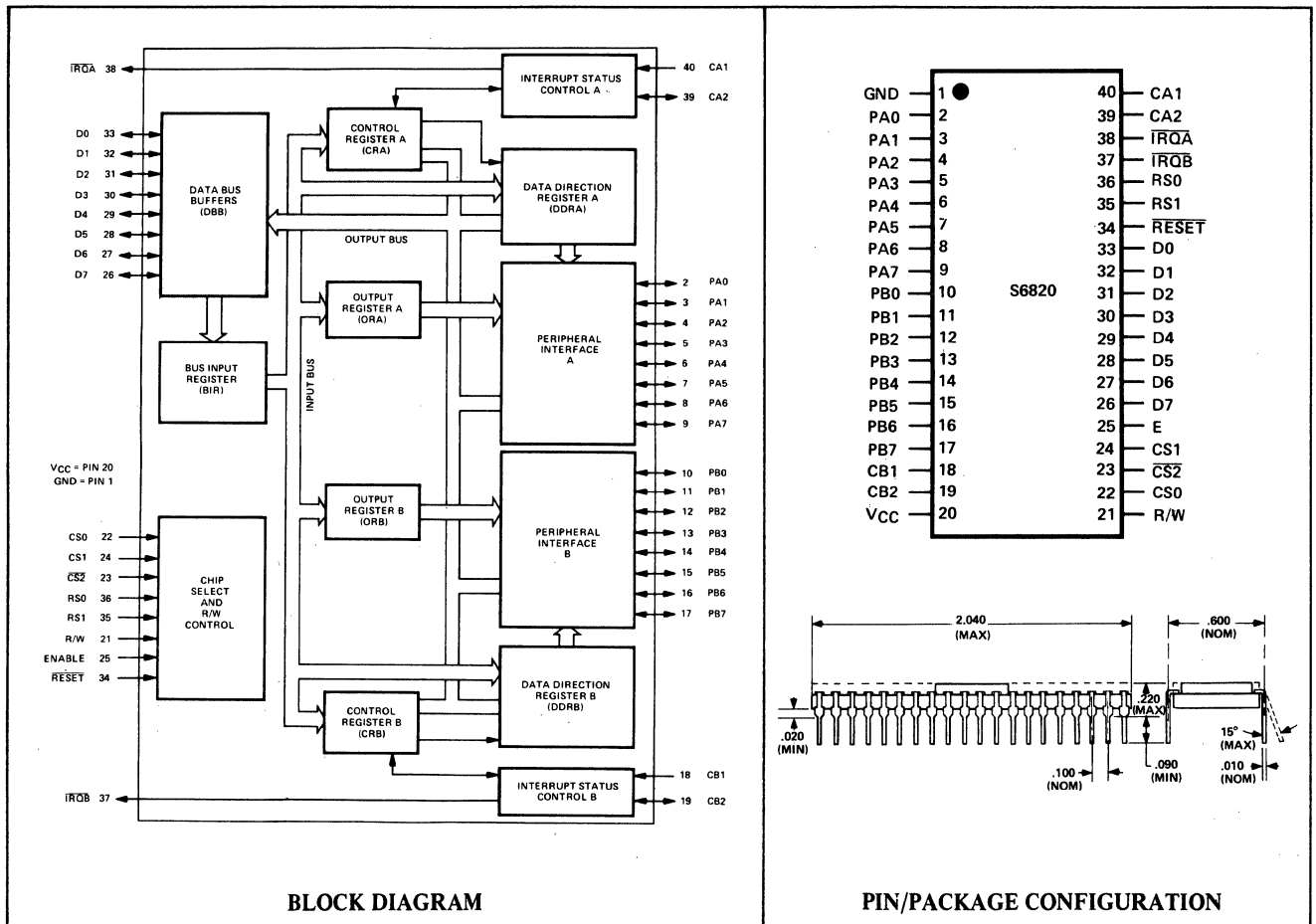
**WRITE CYCLE**

(All timing with  $t_r = t_f = 20$  ns, Load of Figure 1)

Characteristic		Symbol	Min.	Max.	Unit
Write Cycle Time	S6810	$t_{cyc}(W)$	1000	—	ns
	S6810-1		500	—	ns
Write Pulse Width	S6810	$t_{WP}$	800	—	ns
	S6810-1		400	—	ns
Write Pulse Hold Time	S6810	$t_{WH}$	1000	—	ns
	S6810-1		500	—	ns
Data Setup Time	S6810	$t_{DS}$	500	—	ns
	S6810-1		300	—	ns
Data Hold Time	S6810 S6810-1	$t_{DH}$	0	—	ns

**TIMING CHARACTERISTICS**





### FEATURES

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Compatible Peripheral Lines

### FUNCTIONAL DESCRIPTION

The S6820 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the S6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional

peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and

**FUNCTIONAL DESCRIPTION (CONT'D)**

each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

The PIA interfaces to the S6800 MPU with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the S6800 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage $V_{CC}$	-0.3 to +7.0V
Input Voltage $V_{in}$	-0.3 to +7.0V
Operating Temperature Range $T_A$	0 to +70°C
Storage Temperature Range $T_{stg}$	-55 to +150°C

**NOTE:** This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

**DC (STATIC) CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 25^\circ C$  unless otherwise noted.)

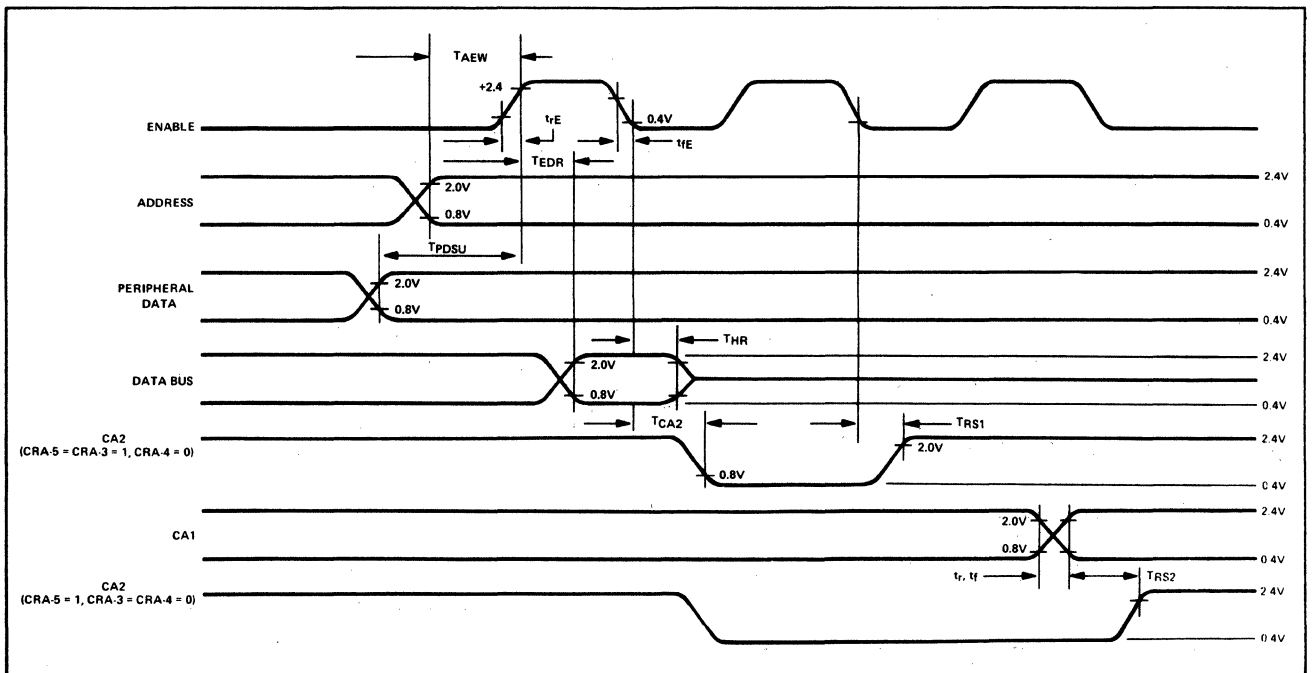
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels)	$V_{IH}$	+2.4	-	$V_{CC}$	Vdc
Input Low Voltage (Normal Operating Levels)	$V_{IL}$	-0.3	-	+0.4	Vdc
Input High Threshold Voltage All Inputs Except Enable	$V_{IHT}$	+2.0	-	-	Vdc
Input Low Threshold Voltage All Inputs Except Enable	$V_{ILT}$	-	-	+0.8	Vdc
Input Leakage Current ( $V_{in} = 0$ to 5.0 Vdc) R/W, Reset, RS0, RS1, CS0, CS1, CS2, CA1, CB1, Enable	$I_{in}$	-	1.0	2.5	$\mu A_{dc}$
Three-State (Off State) Input Current ( $V_{in} = 0.4$ to 2.4 Vdc, $V_{CC} = \max$ ) D0-D7, PB0-PB7, CB2	$I_{TSI}$	-	2.0	10	$\mu A_{dc}$
Input High Current ( $V_{IH} = 2.4$ Vdc) PA0-PA7, CA2	$I_{IH}$	100	250	-	$\mu A_{dc}$
Input Low Current ( $V_{IL} = 0.4$ Vdc) PA0-PA7, CA2	$I_{IL}$	-	1.0	1.6	mAdc
Output High Voltage ( $V_{CC} = \min$ , $I_{Load} = -100 \mu A_{dc}$ , Enable Pulse Width < 25 $\mu s$ )	$V_{OH}$	+2.4	-	-	Vdc
Output Low Voltage ( $V_{CC} = \min$ , $I_{Load} = 1.6$ mAdc)	$V_{OL}$	-	-	+0.4	Vdc
Output High Current (Sourcing) ( $V_{OH} = 2.4$ Vdc) ( $V_{OH} = 1.5$ Vdc, the current for driving other than TTL, e.g., Darlington Base) PB0-PB7, CB2	$I_{OH}$	-100 -1.0	-1000 -2.5	-	$\mu A_{dc}$ mAdc
Output Low Current (Sinking) ( $V_{OL} = 0.4$ Vdc)	$I_{OL}$	1.6	-	-	mAdc
Output Leakage Current (Off State) IRQA, IRQB	$I_{off}$	-	1.0	10	$\mu A_{dc}$
Power Dissipation	$P_D$	-	300	600	mW
Input Capacitance ( $V_{in} = 0$ , $T_A = 25^\circ C$ , $f = 1.0$ MHz) D0-D7, PA0-PA7, PB0-PB7, CA2, CB2 R/W, Reset, RS0, RS1, CS0, CS1, CS2, CA1, CB1 Enable	$C_{in}$	-	-	10 7.0 20	pF
Output Capacitance ( $V_{in} = 0$ , $T_A = 25^\circ C$ , $f = 1.0$ MHz)	$C_{out}$	-	-	10	pF

AC (DYNAMIC) CHARACTERISTICS Loading = 30 pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2  
= 130 pF and one TTL load for D0-D7, IRQA, IRQB

**READ TIMING CHARACTERISTICS (Figure 1)**

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Delay Time, Address valid to Enable positive transition	TAEW	180	—	—	ns
Delay Time, Enable positive transition to Data valid on bus	TEDR	—	—	395	ns
Peripheral Data Setup Time	TPDSU	300	—	—	ns
Data Bus Hold Time	THR	10	—	—	ns
Delay Time, Enable negative transition to CA2 negative transition	TCA2	—	—	1.0	μs
Delay Time, Enable negative transition to CA2 positive transition	TRS1	—	—	1.0	μs
Rise and Fall Time for CA1 and CA2 input signals	t <sub>r</sub> , t <sub>f</sub>	—	—	1.0	μs
Delay Time from CA1 active transition to CA2 positive transition	TRS2	—	—	2.0	μs
Rise and Fall Time for Enable input	t <sub>rE</sub> , t <sub>fE</sub>	—	—	25	μs

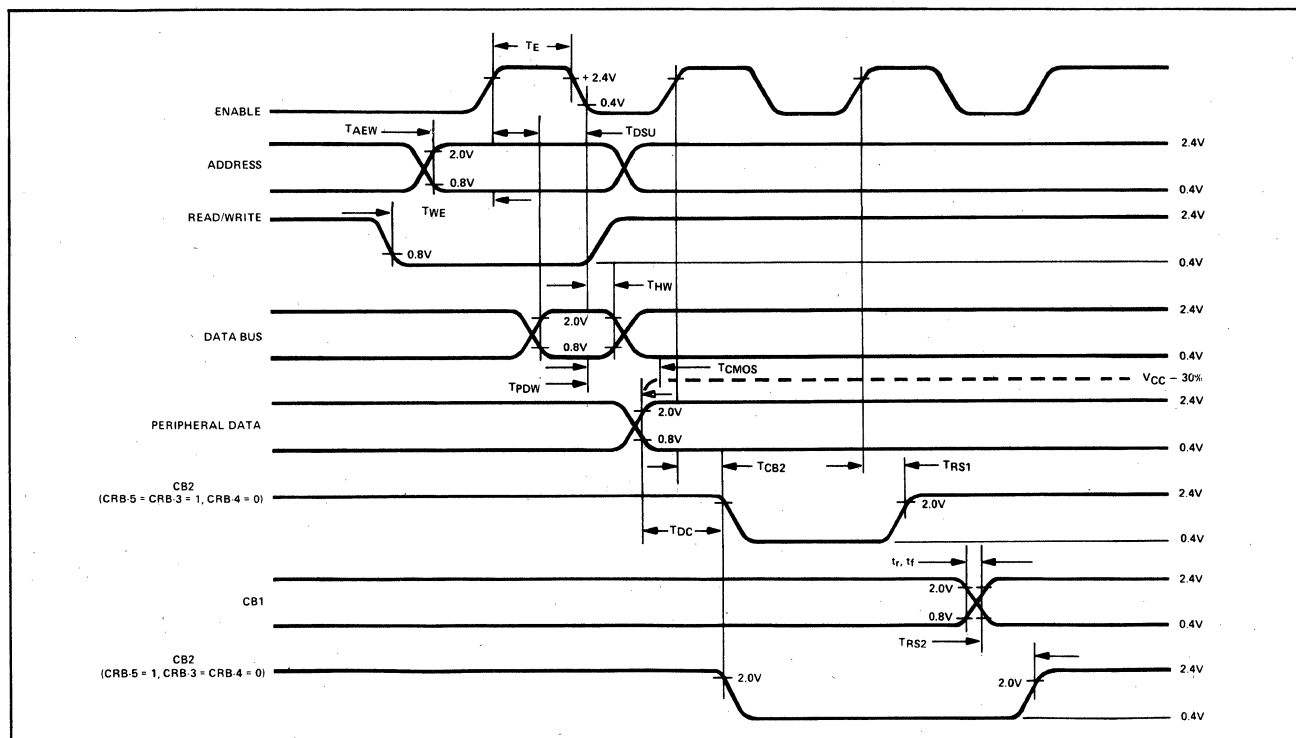
**FIGURE 1 – READ TIMING CHARACTERISTICS**



WRITE TIMING CHARACTERISTICS (Figure 2)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Enable Pulse Width	$T_E$	0.470	—	25	$\mu s$
Delay Time, Address valid to Enable positive transition	$T_{AEW}$	180	—	—	ns
Delay Time, Data valid to Enable negative transition	$T_{DSU}$	300	—	—	ns
Delay Time, Read/Write negative transition to Enable positive transition	$T_{WE}$	130	—	—	ns
Data Bus Hold Time.	$T_{HW}$	10	—	—	ns
Delay Time, Enable negative transition to Peripheral Data valid	$T_{PDW}$	—	—	1.0	$\mu s$
Delay Time, Enable negative transition to Peripheral Data valid, CMOS (VCC - 30%) PA0-PA7, CA2	$T_{CMOS}$	—	—	2.0	$\mu s$
Delay Time, Enable positive transition to CB2 negative transition	$T_{CB2}$	—	—	1.0	$\mu s$
Delay Time, Peripheral Data valid to CB2 negative transition	$T_{DC}$	0	—	1.5	$\mu s$
Delay Time, Enable positive transition to CB2 positive transition	$T_{RS1}$	—	—	1.0	$\mu s$
Rise and Fall Time for CB1 and CB2 input signals	$t_r, t_f$	—	—	1.0	$\mu s$
Delay Time, CB1 active transition to CB2 positive transition	$T_{RS2}$	—	—	2.0	$\mu s$

FIGURE 2 – WRITE TIMING CHARACTERISTICS





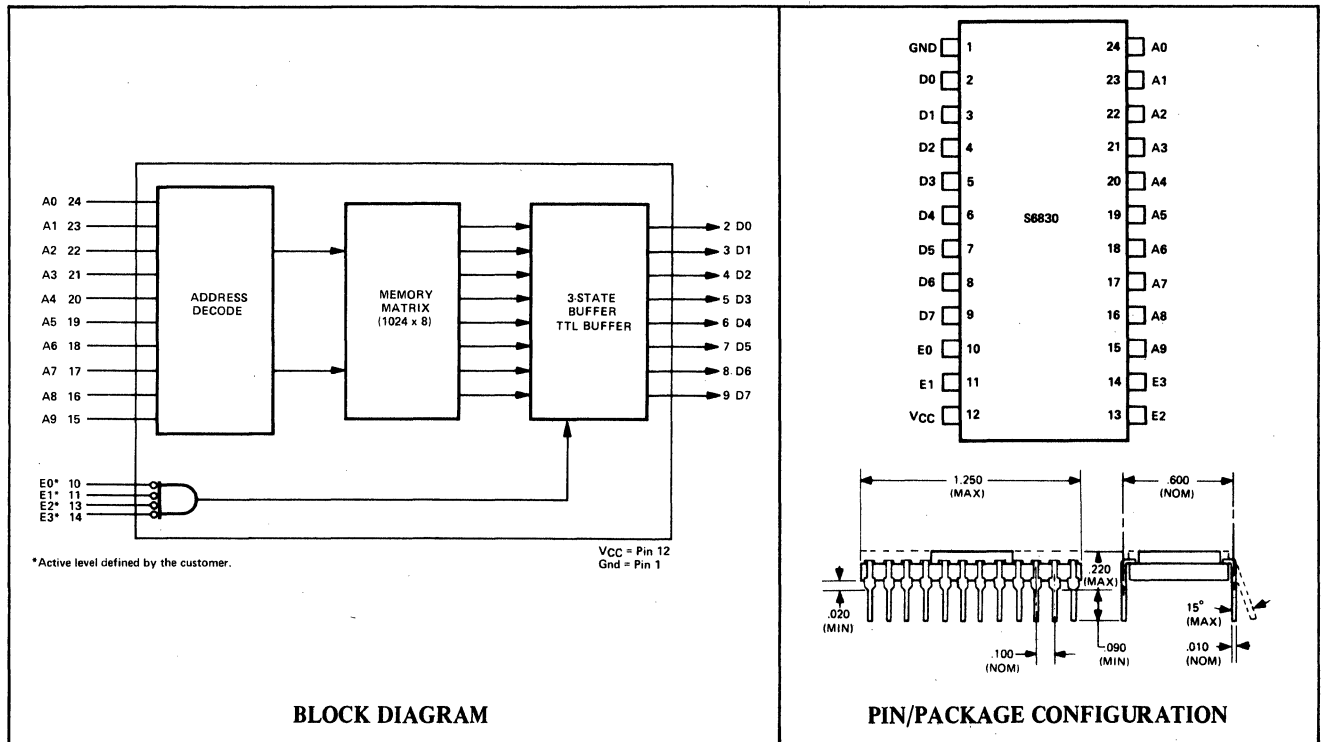
## INTERFACE DESCRIPTION

### MPU/PIA INTERFACE

Pin	Label	Function
(33)	D0	<b>Bi-Directional Data</b> – The bi-directional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.
(32)	D1	
(31)	D2	
(30)	D3	
(29)	D4	
(28)	D5	
(27)	D6	
(26)	D7	
(25)	E	<b>Enable</b> – The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the S6800 $\phi$ 2 Clock.  The E pulse is used to condition the interrupt/control lines CA1, CA2, CB1, and CB2. At least one E pulse must occur from the inactive edge to the active edge of the input signal to set the interrupt flag, when the lines are used as inputs.
(21)	R/W	<b>Read/Write</b> – This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.
(34)	$\overline{\text{RESET}}$	<b>Reset</b> – The active low $\overline{\text{Reset}}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.
(22)	CS0	<b>Chip Select</b> – These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{\text{CS2}}$ must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse.
(24)	CS1	
(23)	$\overline{\text{CS2}}$	
(36)	RS0	<b>PIA Register Select</b> – The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.  The Register select lines should be stable for the duration of the E pulse while in the read or write cycle.
(35)	RS1	
(38)	$\overline{\text{IRQA}}$	<b>Interrupt Request</b> – The active low Interrupt Request lines ( $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ ) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are “open source” (no load device on the chip) and are capable of sinking a current of 1.6 mA from an external source. This permits all interrupt request lines to be tied together in a wire-OR configuration.  Each Interrupt Request line has two internal interrupt flag bits that will cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.  Servicing an interrupt by the MPU is accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.  The Interrupt Flag is cleared (zeroed) as a result of an MPU Read Peripheral Data Operation.
(37)	$\overline{\text{IRQB}}$	

PIA/PERIPHERAL INTERFACE

Pin	Label	Function
(2)	PA0	<p><b>Section A Peripheral Data</b> – Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a “1” in the corresponding Data Direction Register bit for those lines which are to be outputs. A “0” in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of one standard TTL load.</p> <p>The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical “1” written into the register will cause a “high” on the corresponding data line while a “0” results in a “low”. Data in Output Register A may be read by an MPU “Read Peripheral Data A” operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic “1” output and less than 0.8 volt for a logic “0” output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.</p>
(3)	PA1	
(4)	PA2	
(5)	PA3	
(6)	PA4	
(7)	PA5	
(8)	PA6	
(9)	PA7	
(10)	PB0	
(11)	PB1	
(12)	PB2	
(13)	PB3	
(14)	PB4	
(15)	PB5	
(16)	PB6	
(17)	PB7	
(40)	CA1	<p><b>Interrupt Input</b> – Peripheral Input lines CA1 and CB1 are input-only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.</p>
(18)	CB1	
(39)	CA2	<p><b>Peripheral Control</b> – The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents one standard TTL load. The function of this signal line is programmed with Control Register A.</p>
(19)	CB2	<p><b>Peripheral Control</b> – Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliamperes at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.</p>
(1)	GND	<b>Ground</b>
(20)	VCC	+5 Volts ± 5%



## FEATURES

- Organized as 1024-Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Four Chip Enable Inputs (Mask Programmable)
- Single 5-Volt Power Supply
- TTL Compatible Input/Output
- Maximum Access Time = 575 ns

## FUNCTIONAL DESCRIPTION

The S6830 is a mask programmable read only memory organized 1024 words x 8 bits for application in byte organized systems. The S6830 is totally bus compatible with the S6800 microprocessor. Interfacing to the S6830 consists

of an 8 bit three-state data bus, four mask programmable chip selects and ten address lines.

The S6830 is a totally static memory requiring no clocks. Access time is compatible with maximum data rates in a S6800 microprocessor system. The device operates from a single +5 volt power supply and is fabricated with N channel silicon gate technology.

## ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply Voltage $V_{CC}$	-0.3 to +7.0V
Input Voltage $V_{in}$	-0.3 to +7.0V
Operating Temperature Range $T_A$	0 to +70°C
Storage Temperature Range $T_{stg}$	-55 to +150°C

**NOTE:1.** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

**DC (STATIC) CHARACTERISTICS**

( $V_{CC} = +5 \text{ Volt} \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ) **RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage (Norm. Op. Levels)	$V_{IH}$	2.4	5.25	Vdc
Input Low Voltage (Norm. Op. Levels)	$V_{IL}$	-0.3	0.4	Vdc
Input Current ( $V_{in} = 0$ to $5.25 \text{ V}$ )	$I_{in}$	-	2.5	$\mu\text{A}$ dc
Input High Threshold Voltage	$V_{IHT}$	2.0	-	Vdc
Input Low Threshold Voltage	$V_{ILT}$	-	0.65	Vdc
Output High Voltage ( $I_{OH} = -100 \mu\text{A}$ )	$V_{OH}$	2.4	-	Vdc
Output Low Voltage ( $I_{OL} = 1.6 \text{ mA}$ )	$V_{OL}$	-	0.45	Vdc
Output Leakage Current ( $V_{OH} = 2.4 \text{ V}$ , $E = 0.4 \text{ V}$ , $\bar{E} = 2.4 \text{ V}$ )	$I_{LOH}$	-	10	$\mu\text{A}$ dc
Output Leakage Current ( $V_{OH} = 0.4 \text{ V}$ , $E = 0.4 \text{ V}$ , $\bar{E} = 2.4 \text{ V}$ )	$I_{LOL}$	-	10	$\mu\text{A}$ dc
Supply Current ( $V_{CC} @ 5.25\text{V}$ , $T_A = 0^\circ\text{C}$ )	$I_{CC}$	-	130	$\text{mA}$ dc

**CAPACITANCE**

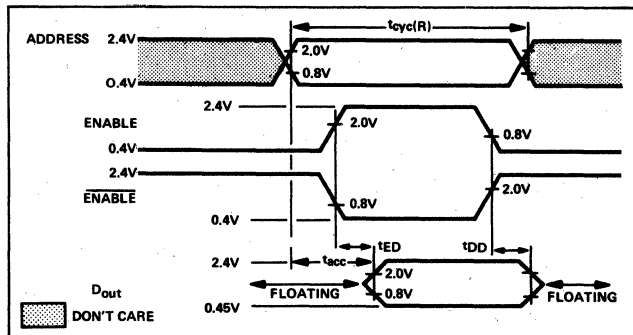
Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Capacitance	$C_{in}$	-	-	7.5	pF	$f = 1.0 \text{ MHz}$
Output Capacitance	$C_{out}$	-	-	15	pF	$T_A = 25^\circ\text{C}$

**AC (DYNAMIC) CHARACTERISTICS READ CYCLE** (All timing with  $t_r = t_f = 20 \text{ ns}$ , Load of Figure 1)

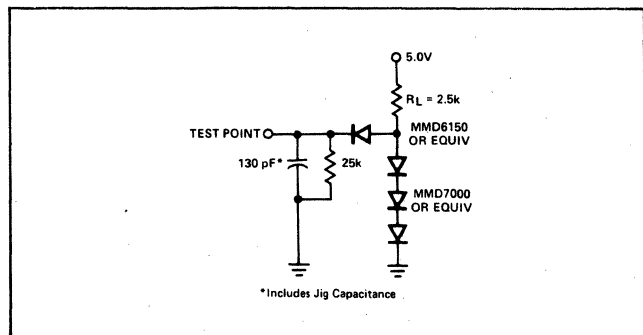
$V_{CC} = +5 \text{ Volt} \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$

Characteristic	Symbol	Min.	Max.	Unit
Read Cycle Time	$t_{cyc}(R)$	575	-	ns
Output Enable Delay Time	$t_{ED}$	-	300	ns
Output Disable Delay Time	$t_{DD}$	10	150	ns
Read Access Time	$t_{acc}$	-	575	ns

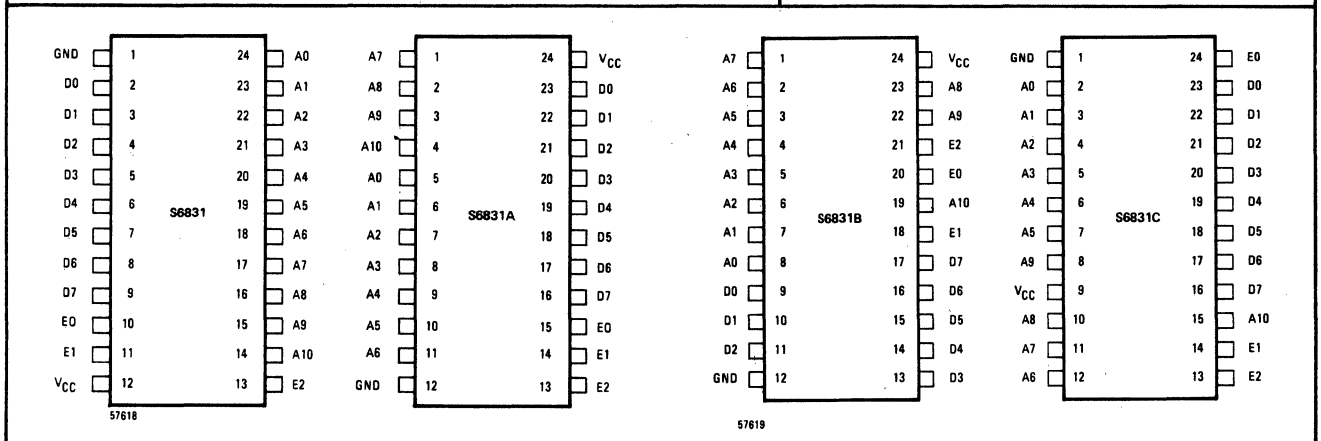
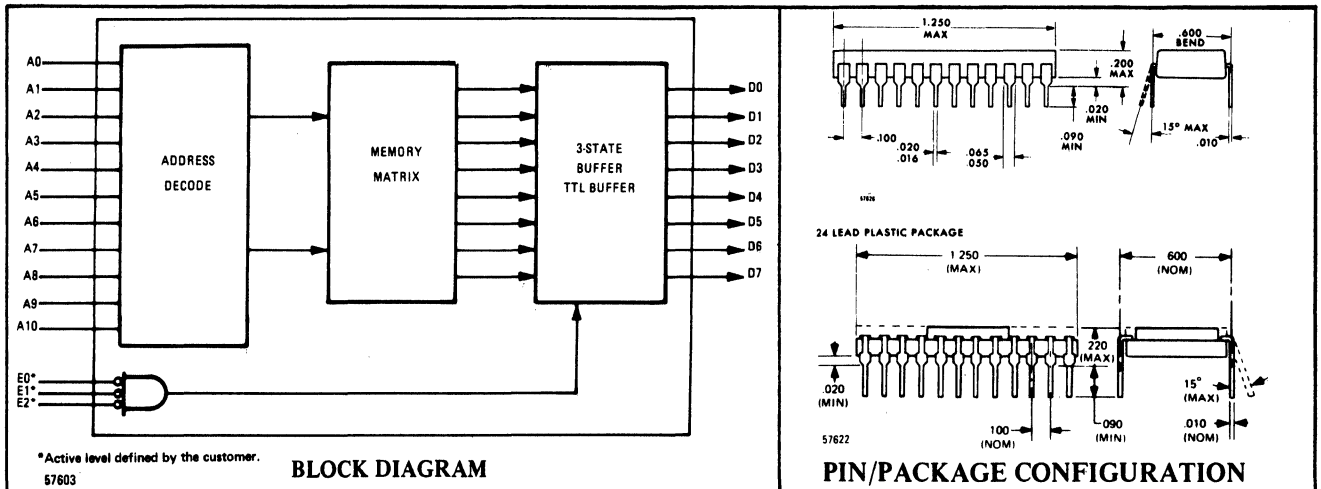
**READ CYCLE TIMING**



**FIGURE 1 – AC TEST LOAD**



### ADVANCED PRODUCT DESCRIPTION



- Maximum Access Time = 450 ns @  $C_L = 130$  pF
- Low Power 150 mW avg.
- Organized as 2048-Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- 3 Chip Enable Inputs (Mask Programmable)
- The S6831 is pinout similar with the S6830
- The S6831A is pinout compatible with the 2316A, 8316A

- The S6831B is pinout compatible with the Intel 2316B, MC68317
- The S6831C is pinout compatible with the EA4600
- Single 5-Volt Power Supply
- TTL Compatible Input/Output

### FUNCTIONAL DESCRIPTION

The S6831/A/B/C is a 16,384 bit Read Only Memory organized 2K words x 8 bits. This ROM has been designed to supply large bit storage, high performance memory for micro-

processors and other demanding applications with simple interface requirements. The device will operate from a single +5V supply and is manufactured with a N-channel silicon gate depletion load technology. This device is available in all common high density ROM pinouts.

### ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply Voltage $V_{CC}$	- 0.5 to + 7.0V	Operating Temperature Range $T_A$	0 to + 70°C
Input Voltage $V_{in}$	- 0.5 to + 7.0V	Storage Temperature Range $T_{stg}$	- 55 to + 150°C

**NOTE 1** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC (STATIC) CHARACTERISTICS ( $V_{CC} = +5 \text{ Volt} \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$V_{IH}$	Input High Voltage (Norm. Op. Levels)	2.0	—	5.25	Vdc	
$V_{IL}$	Input Low Voltage (Norm. Op. Levels)	-0.5	—	0.8	Vdc	
$I_I$	Input Current ( $V_I = 0$ to $5.25 \text{ V}$ )	—	—	2.5	$\mu\text{A}$ dc	
$V_{OH}$	Output High Voltage ( $I_{OH} = -100 \mu\text{A}$ )	2.4	—	—	Vdc	
$V_{OL}$	Output Low Voltage ( $I_{OL} = 2.1 \text{ mA}$ )	—	—	0.4	Vdc	
$I_{LOH}$	Output Leakage Current ( $V_O = 2.4, \bar{E} = 0.4\text{V}, E = 2.4\text{V}$ )	—	—	10	$\mu\text{A}$ dc	
$I_{LOL}$	Output Leakage Current ( $V_O = 0.4\text{V}, \bar{E} = 0.4\text{V}, E = 2.4\text{V}$ )	—	—	10	$\mu\text{A}$ dc	
$I_{CC}$	Supply Current ( $V_{CC} = 5.25\text{V}, T_A = 0^\circ\text{C}$ )	—	30	—	$\text{mA}$ dc	

CAPACITANCE

Symbol	Characteristic	Min.	Typ.	Max	Unit	Conditions
$C_{in}$	Input Capacitance	—	—	7.5	pF	$f = 1.0 \text{ MHz}$
$C_{out}$	Output Capacitance	—	—	10	pF	$T_A = 25^\circ\text{C}$

AC (DYNAMIC) CHARACTERISTICS  $V_{CC} = +5 \text{ Volt} \pm 5\%$ ;  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$

READ CYCLE (All timing with  $t_r = t_f = 20 \text{ ns}$ , Load of Figure 1)

Symbol	Characteristic	Min.	Max.	Unit
$t_{cyc}(R)$	Read Cycle Time	450	—	ns
$t_{ED}$	Output Enable Delay Time	—	200	ns
$t_{DD}$	Output Disable Delay Time	10	150	ns
$t_{ACC}$	Read Access Time	—	450	ns

READ CYCLE TIMING

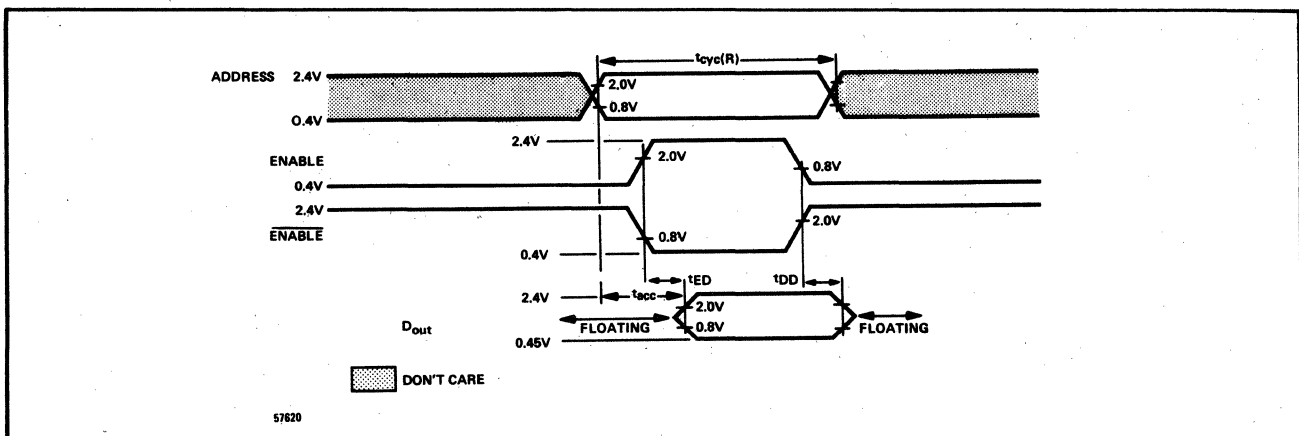
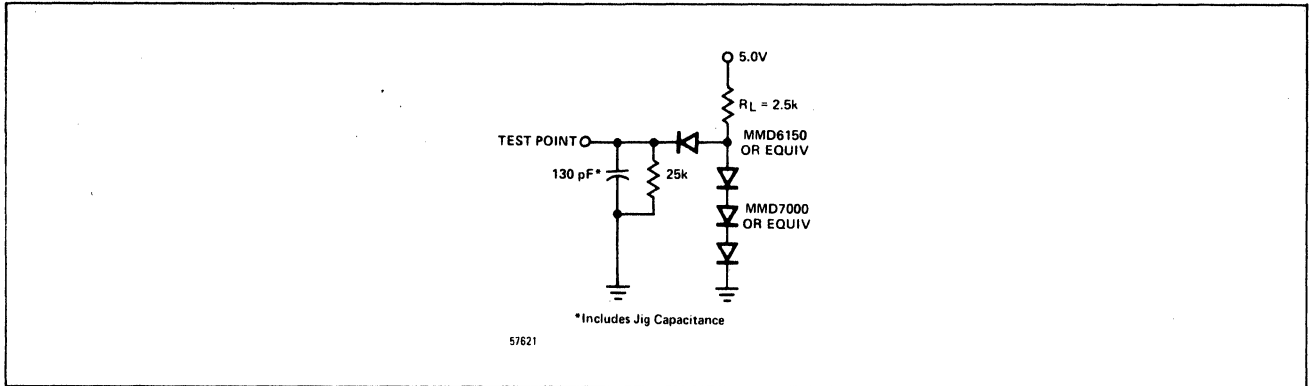


FIGURE 1 -- AC TEST LOAD



### CUSTOM PROGRAMMING

The preferred method of pattern submission is the AMI Hex format as described below with its built-in address space

mapping and error checking. This is the format produced by the AMI Assembler/Loader. The format is as follows and may be on paper tape, punched card or other media readable by AMI.

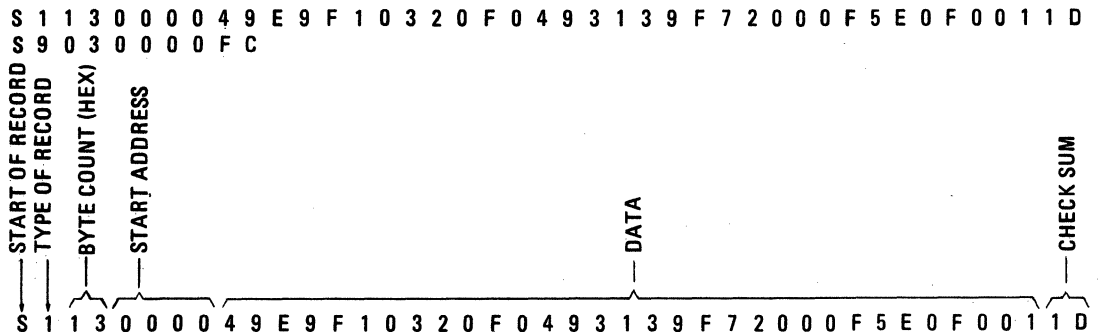
#### ASCII Character

#### Description

1	<b>Start of record (S)</b>
2	<b>Type of record</b> 0 - Header record 1 - Data record 9 - End of file record
3 - 4	<b>Byte Count</b> Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length being defined in each record by the byte count.
5, 6, 7, 8	<b>Address Value</b> The memory location where this record is to be stored.
9, ..., N	<b>Data</b> Each data byte is represented by two hex characters. Most significant character first.
N + 1, N + 2	<b>Checksum</b> The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

AMI will accept the input format used for the EA4600 or for the Intel 8316A or B in addition to the above format.

**EXAMPLE:**

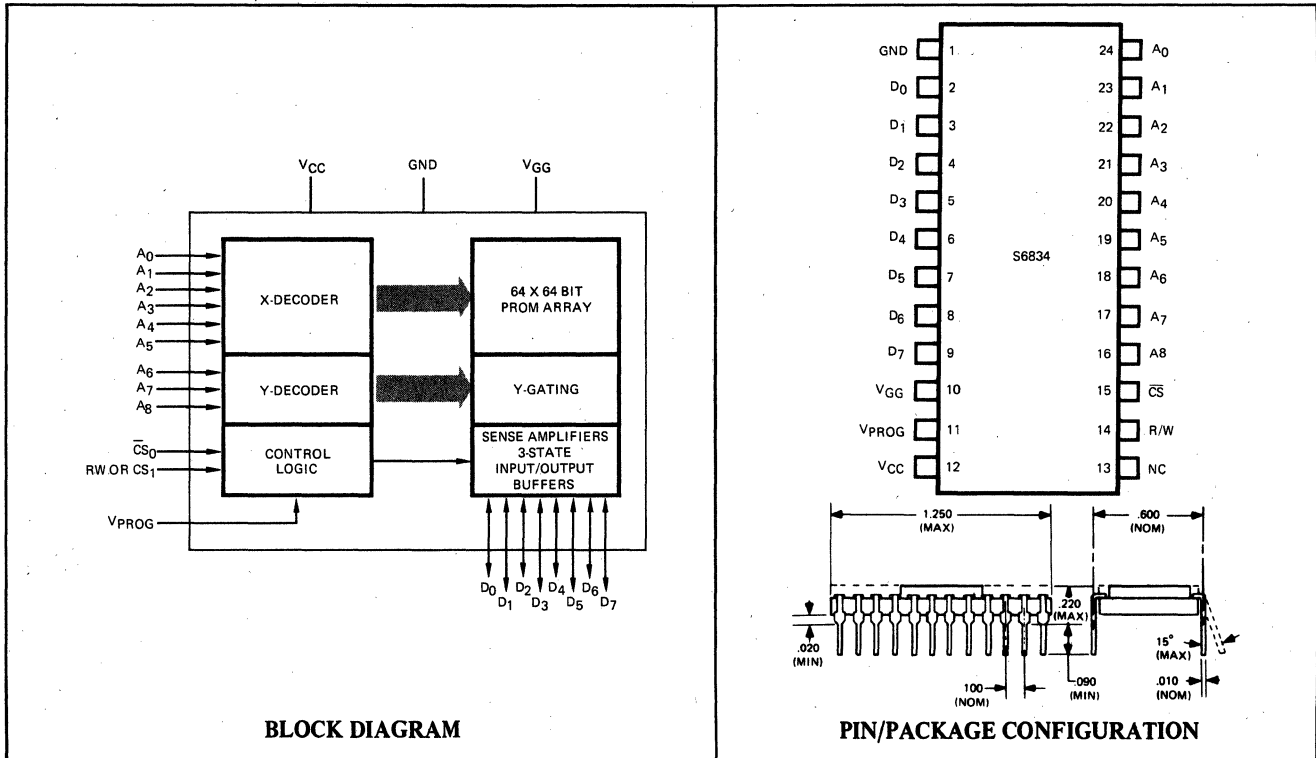


# S6834

512 X 8 BIT  
ERASEABLE AND  
ELECTRICALLY REPROGRAMMABLE  
READ ONLY MEMORY

# AMI

AMERICAN MICROSYSTEMS, INC.



BLOCK DIAGRAM

PIN/PACKAGE CONFIGURATION

## FEATURES

- On-Board Programmability
- Fast Access Time – 500 ns Typ.
- Pin Configuration Similar to the S6830  
1K x 8 Bit ROM
- High Speed Programming – Less than 1 Minute for  
all 4096 Bits
- Programmed with R/W, CS and VPROG Pins
- Completely TTL Compatible – Excluding the  
VPROG Pin during Read and Write
- Ultraviolet Light Erasable – Less than 10 Minutes
- Static Operation – No Clocks Required
- Three-State Data I/O
- Standard Power Supplies +5V and -12V
- Mature P-Chan Process

## FUNCTIONAL DESCRIPTION

The S6834 is a high speed, static, 512 x 8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24 pin hermetically sealed dual in-line package the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written.

## TYPICAL APPLICATIONS

- ROM Program Debugging
- Code Translation
- Microprogramming
- Look-up Tables
- Random Logic Replacement
- Programmable Waveforms
- Character Generation
- Electronic Keyboards



### ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to $V_{SS}$ except the $V_{PROG}$ pin	+0.3 to -20V
Voltage on the $V_{PROG}$ pin relative to $V_{SS}$	+0.3 to -55V
Operating Temperature	0°C to +70°C
Storage Temperature (programmed)	-55°C to +85°C
Storage Temperature (unprogrammed)	-55°C to 150°C

**NOTE:** This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

### DC (STATIC) CHARACTERISTICS ( $V_{CC} = +5.0V \pm 5\%$ , $V_{GG} = -12.0V \pm 5\%$ , $T_A = 0 - 70^\circ C$ unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
$V_{IL}$	INPUT VOLTAGE LOW		0.8	V
$V_{IH}$	INPUT VOLTAGE HIGH	$V_{CC} - 2.25$	$V_{CC} - 0.3$	V
$V_{OL}$	OUTPUT VOLTAGE LOW $I_{OL} = 1.6 \text{ ma}$		0.4	V
$V_{OH}$	OUTPUT VOLTAGE HIGH $I_{OH} = 200\mu A$	2.4		V
$I_{LI}$	INPUT LEAKAGE CURRENT		10	$\mu a$
$I_{LO}$	OUTPUT LEAKAGE CURRENT $CS = 5V$		20	$\mu a$
$I_{GG}$	$V_{GG}$ SUPPLY CURRENT		45	ma
$I_{CC}$	$V_{CC}$ SUPPLY CURRENT		50	ma
$P_D$	POWER DISSIPATION		750	mw

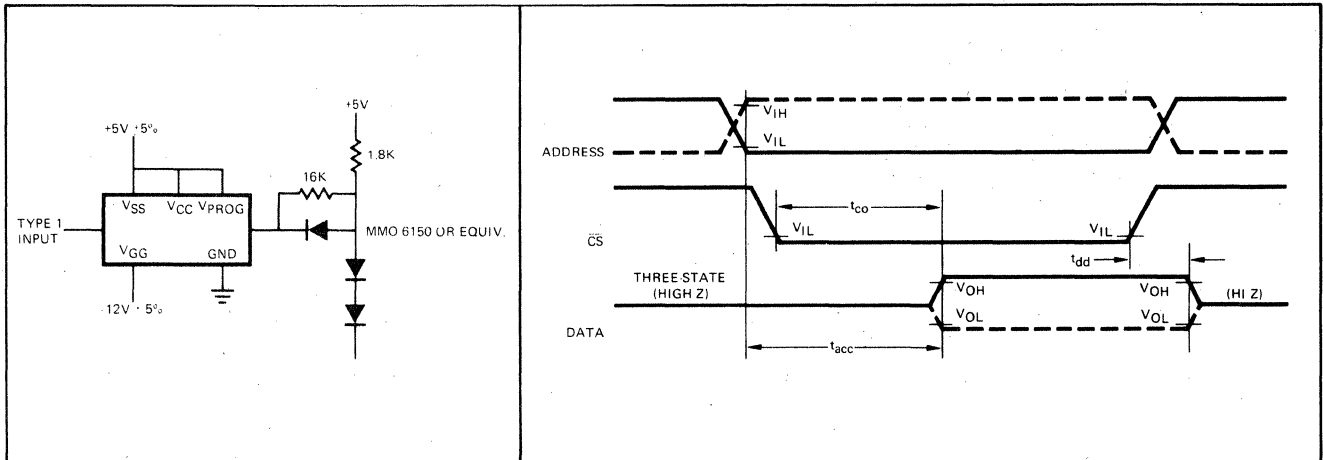
**NOTE:** Program input  $V_{PROG}$  may be tied to  $V_{CC}$  during the Read.

### AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX		UNIT
			(6834)	(6834-1)	
$T_{ACC}$	ACCESS TIME		575	750	ns
$T_{CO}$	CHIP SELECT TO OUTPUT DELAY		300	400	ns
$T_{DD}$	CHIP DESELECT TO OUTPUT DELAY		250	325	ns

FIGURE 1 — TEST CONDITIONS

FIGURE 2 — READ CYCLE TIMING WAVEFORMS



PROGRAM CHARACTERISTICS (R/W  $G_{nd}$ , Program pulse rise and fall time (10% to 90%) are both at 1 $\mu$ s max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
$T_{AS}$	ADDRESS SET UP TIME	10		$\mu$ s
$T_{CSS}$	CHIP SELECT SET UP TIME	10		$\mu$ s
$T_{DS}$	DATA SET UP TIME	10		$\mu$ s
$T_{AH}$	ADDRESS HOLD TIME	10		$\mu$ s
$T_{CSH}$	CHIP SELECT HOLD TIME	10		$\mu$ s
$T_{DH}$	DATA HOLD TIME	10		$\mu$ s
$T_{pWL}$	PROGRAM PULSE WIDTH LOW	3	5	ms
$T_{pWH}$	PROGRAM PULSE WIDTH HIGH	500		$\mu$ s
$V_{PROG}^*$	PROGRAM AMPLITUDE	-55	-50	V
$I_{PROG}$	PROGRAM CURRENT		35	ma
$T_{WS}$	WRITE SET UP TIME	10		$\mu$ s
$T_{WH}$	WRITE HOLD TIME	5		$\mu$ s
$T_{RS}$	READ SET UP TIME	10		$\mu$ s

\*Note that in the WRITE mode the MIN value of  $V_{PROG}$  should not be exceeded and that chip select, address, and data lines may remain at TTL level, as in the READ mode

FIGURE 3 — PROGRAMMING CYCLE TIMING WAVEFORMS

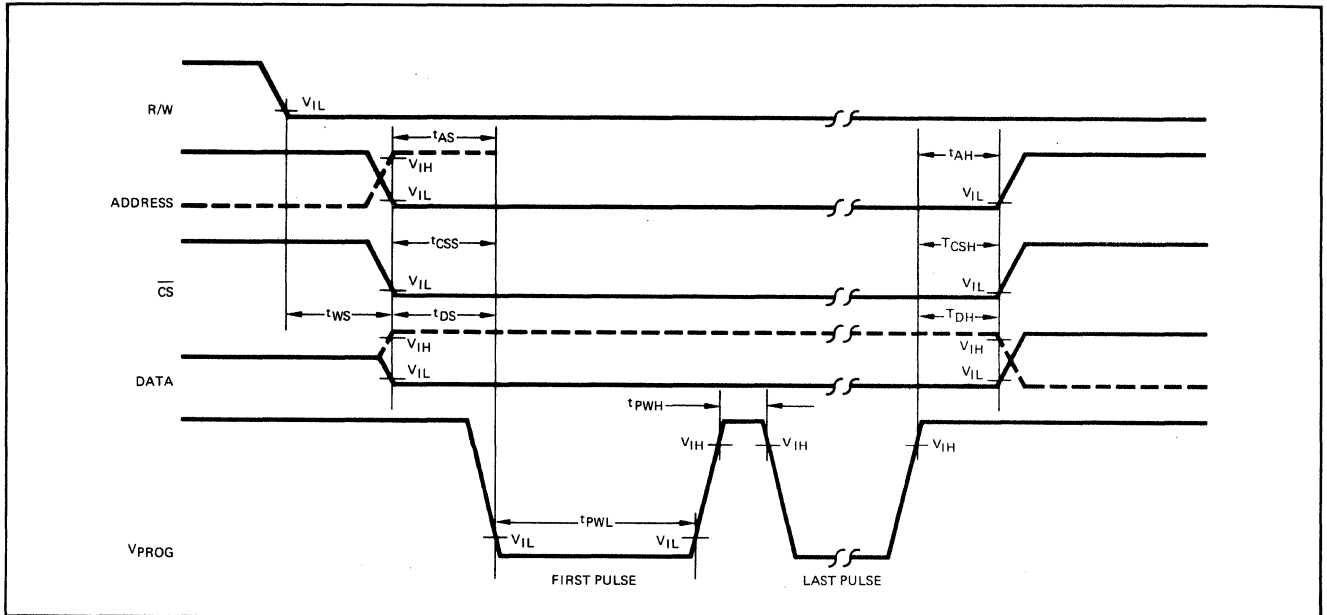
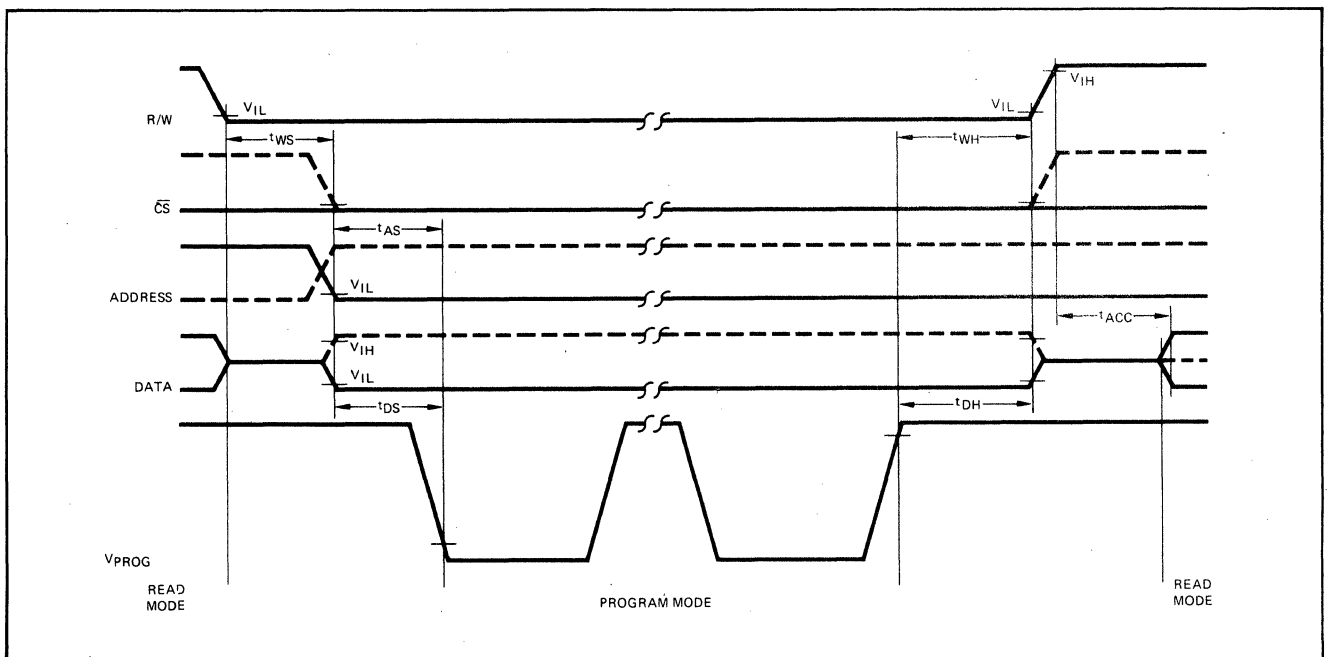


FIGURE 4 — READ/PROGRAM/READ CYCLE TIMING WAVEFORM



CONTROL FUNCTION TRUTH TABLE

CS	R/W	V <sub>PROG</sub>	MODE	OUTPUTS
0	0	V <sub>PROG</sub>	Write	Active Data Inputs
0	1	V <sub>CC</sub>	Read	Active
1	X	X	Standby	Floating

### OPERATION

Initially, and after each erasure, all bits of the 6834 are in the logic "0" state (output 0 volts). Data is stored by selectively programming a logic "1" into the desired bit locations. The R/W input (pin 14) is used to select the desired mode of operation. When the R/W input is at logic "0" the chip is in the write enable mode of operation. The outputs ( $O_1 - O_8$ ) are disabled (floating) with the corresponding pins becoming the data inputs ( $O_1 \rightarrow D_{IN 1}$  etc.). The word address is selected in the same manner as in the read mode. Data to be programmed are presented 8 bits in parallel and after the address and data are set up a programming pulse ( $V_P - 50$  volts) is applied.  $V_{PROG}$  electrically writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a logic "1" during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and  $V_{PROG}$  inputs are common and the device to be programmed is selected by means of the chip select input as during read operations.

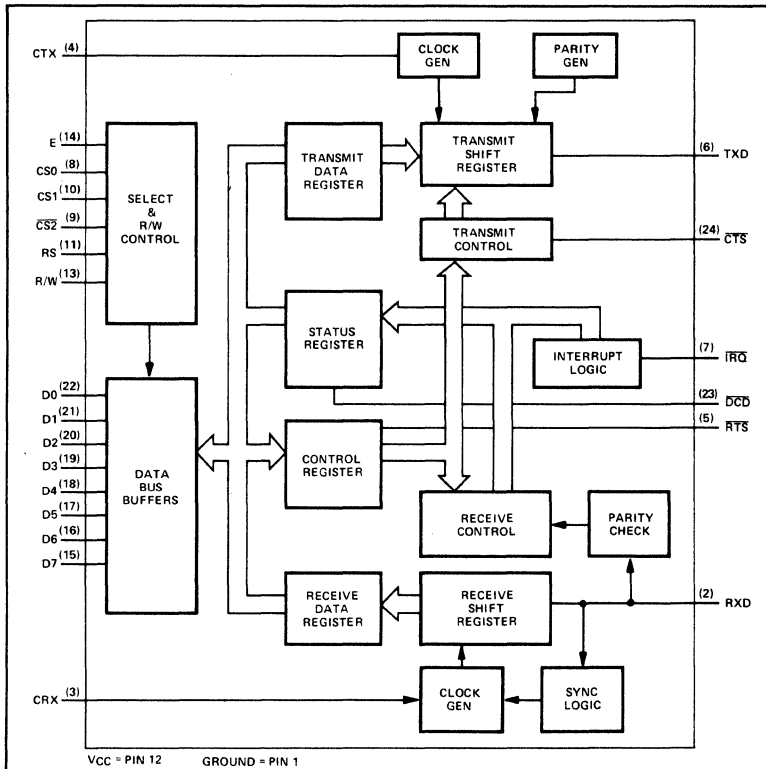
The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses ( $N$ ) times the program pulse width ( $t_{pw}$ ) ( $N \times t_{pw} \geq 60$  msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

The read operation is accomplished by a logic "1" at the R/W input with the program input connected to  $V_{SS}$  potential. True data (data out = data in) is valid after the address is stable. The CS input will disable (float) the outputs when at a logic "1" to allow or tie capability.

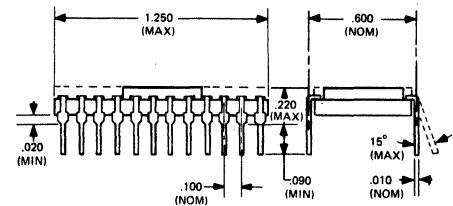
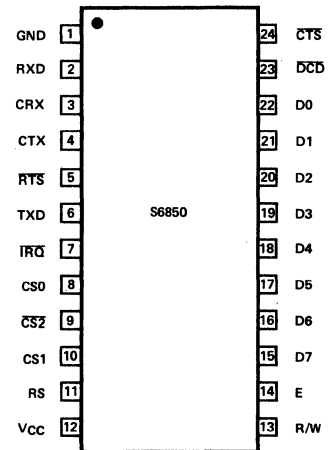
Erasure is accomplished by exposing the array to a high intensity ultra-violet light source (such as, Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

### INTERFACE DESCRIPTION

Pin	Label	Function
(2)	D0	<b>Data Lines</b> – with the R/W line selected for Read ( $V_{IH}$ ), the Data Lines (D0 through D7) are set to reflect the contents of the selected memory location. When the R/W line is set for Write ( $V_{IL}$ ), the Data Lines are input to the addressed location of the 6834 when $V_{PROG}$ is present. The Data Bus output drivers are three-state devices that remain in the high impedance (off) state when CS is in the $V_{IH}$ state of when R/W is in the $V_{IL}$ state.
(3)	D1	
(4)	D2	
(5)	D3	
(6)	D4	
(7)	D5	
(8)	D6	
(9)	D7	
(14)	R/W	
(15)	CS	<b>Chip Select</b> – This input line must be set to $V_{IL}$ for a Read or Write operation to be performed. When it is High ( $V_{IH}$ ) the output data bus is set to a high-impedance three-state condition and disables the Write operation.
(11)	$V_{PROG}$	<b>Program</b> – In the Write mode, a programming pulse ( $-50V$ dc) at this input causes the data at the Data Lines to be stored in the selected address. This pin should be tied to $V_{CC}$ for normal Read operations.
(24)	A0	<b>Address Lines</b> – These lines select the 8 bit word in memory for Read or Write operation
(23)	A1	
(22)	A2	
(21)	A3	
(20)	A4	
(19)	A5	
(18)	A6	
(17)	A7	
(16)	A8	



**BLOCK DIAGRAM**



**PIN/PACKAGE CONFIGURATION**

### FEATURES

- 8 Bit Bidirectional Data Bus for Communication with MPU.
- False start bit deletion.
- Peripheral/modem control functions.
- Double buffered Receiver and Transmitter
- One or two stop bit operation.
- Eight and nine-bit transmission with optional even and odd parity.
- Parity, overrun and framing error checking.
- Programmable control register.
- Optional ÷1, ÷16, and ÷64 clock modes.
- Up to 500,000 bps transmission.

### FUNCTIONAL DESCRIPTION

The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight bit

bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage $V_{CC}$	-0.3 to +7.0V	Operating Temperature Range $T_A$	0 to +70°C
Input Voltage $V_{in}$	-0.3 to +7.0V	Storage Temperature Range $T_{stg}$	-55 to +150°C

**NOTE:** This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

**DC (STATIC) CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 25^\circ C$  unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels)	$V_{IH}$	+2.4	—	$V_{CC}$	Vdc
Input Low Voltage (Normal Operating Levels)	$V_{IL}$	-0.3	—	+0.4	Vdc
Input High Threshold Voltage All Inputs Except Enable	$V_{IHT}$	+2.0	—	—	Vdc
Input Low Threshold Voltage All Inputs Except Enable	$V_{ILT}$	—	—	+0.8	Vdc
Input Leakage Current ( $V_{in} = 0$ to 5.0 Vdc) R/W, RS, CS0, CS1, $\overline{CS2}$ , Enable	$I_{in}$	—	1.0	2.5	$\mu A_{dc}$
Three-State (Off State) Input Current ( $V_{in} = 0.4$ to 2.4 Vdc, $V_{CC} = \max$ ) D0-D7,	$I_{TSI}$	—	2.0	10	$\mu A_{dc}$
Output High Voltage ( $I_{Load} = -100 \mu A_{dc}$ , Enable Pulse Width < 25 $\mu s$ ) All Outputs Except $\overline{IRQ}$	$V_{OH}$	+2.4	—	—	Vdc
Output Low Voltage ( $I_{Load} = 1.6 \text{ mA}_{dc}$ ) Enable Pulse Width < 25 $\mu s$	$V_{OL}$	—	—	+0.4	Vdc
Output Leakage Current (Off State) $\overline{IRQ}$	$I_{LOH}$	—	1.0	10	$\mu A_{dc}$
Power Dissipation	$P_D$	—	300	525	mW
Input Capacitance ( $V_{in} = 0$ , $T_A = 25^\circ C$ , $f = 1.0 \text{ MHz}$ ) D0-D7 R/W, RS, CS0, CS1, $\overline{CS2}$ , RXD, CTX, CRX, $\overline{CTS}$ , $\overline{DCD}$ Enable	$C_{in}$	—	—	10	pF
Output Capacitance ( $V_{in} = 0$ , $T_A = 25^\circ C$ , $f = 1.0 \text{ MHz}$ )	$C_{out}$	—	—	10	pF

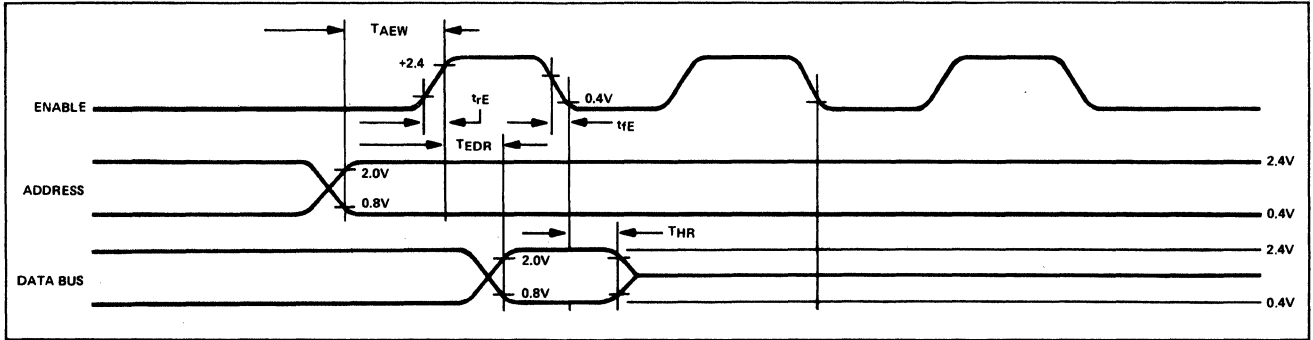
**AC (DYNAMIC) CHARACTERISTICS**

Loading = 130 pF and one TTL load for D0-D7 = 20pF and 1 TTL load for  $\overline{RTS}$  and TXD = 100pF and 3K $\Omega$  to  $V_{CC}$  for  $\overline{IRQ}$ .

**READ TIMING CHARACTERISTICS** (Figure 1)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Setup Time, Address valid to Enable positive transition	$T_{AEW}$	180	—	—	ns
Setup Time, Enable positive transition to Data valid on bus	$T_{EDR}$	—	—	395	ns
Data Bus Hold Time	$T_{HR}$	10	—	—	ns
Rise and Fall Time for Enable input	$t_{rE}$ , $t_{fE}$	—	—	25	$\mu s$

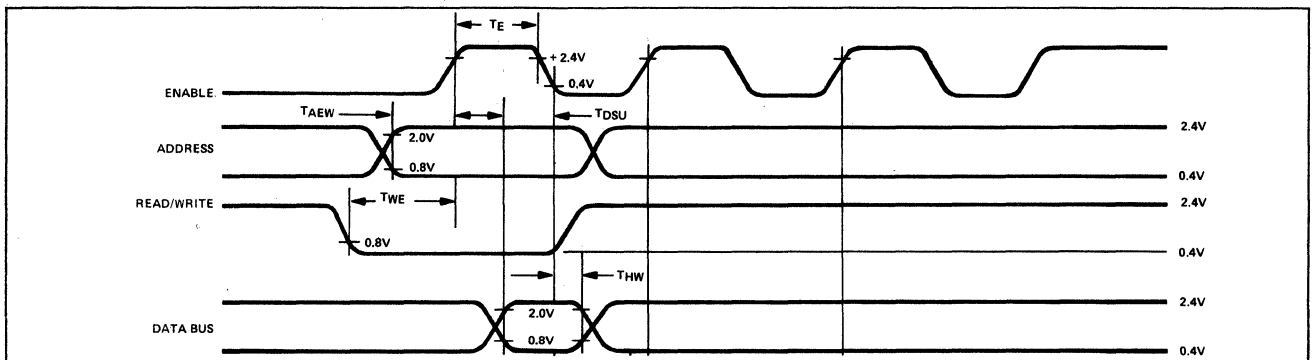
**FIGURE 1 – READ TIMING CHARACTERISTICS**



**WRITE TIMING CHARACTERISTICS (Figure 2)**

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Enable Pulse Width	$T_E$	0.470	—	25	$\mu s$
Setup Time, Address valid to Enable positive transition	$T_{AEW}$	180	—	—	ns
Setup Time, Data valid to Enable negative transition	$T_{DSU}$	300	—	—	ns
Setup time, Read/Write negative transition to Enable positive transition	$T_{WE}$	130	—	—	ns
Data Bus Hold Time	$T_{HW}$	10	—	—	ns

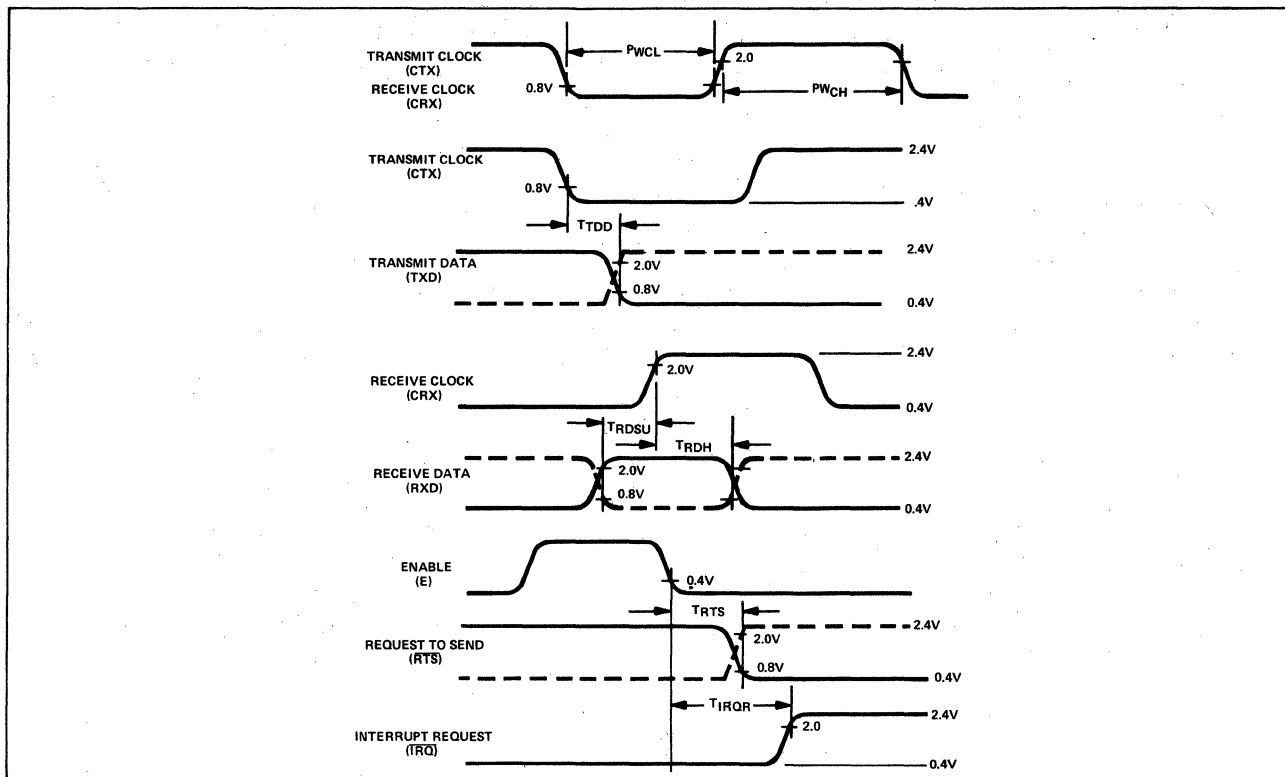
**FIGURE 2 – WRITE TIMING CHARACTERISTICS**



**TRANSMIT/RECEIVE CHARACTERISTICS (Figure 3)**

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency	$f_c$			500	KHz
÷ 1 mode				800	KHz
÷ 16 mode				800	KHz
Clock Pulse Width, Low State	$PW_{CL}$	600			nsec
Clock Pulse Width, High State	$PW_{CH}$	600			nsec
Delay Time, Transmit Clock to Data Out	$T_{TDD}$			1.0	$\mu sec$
Set up Time, Receive Data	$T_{RDSU}$	500			nsec
Hold Time, Receive Data	$T_{RDH}$	500			nsec
Delay Time, Enable to $\overline{IRQ}$ Reset	$T_{IRQR}$			1.2	$\mu sec$
Delay Time, Enable to $\overline{RTS}$	$T_{RTS}$			1.0	$\mu sec$

FIGURE 3 – TRANSMIT/RECEIVE TIMING



MPU/ACIA INTERFACE

Pin	Label	Function
(22)	D0	<b>ACIA BI-DIRECTIONAL DATA LINES</b> —The bi-directional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation. The Read/Write line is in the read (high) state when the ACIA is selected for a read operation.
(21)	D1	
(20)	D2	
(19)	D3	
(18)	D4	
(17)	D5	
(16)	D6	
(15)	D7	
(14)	E	<b>ACIA ENABLE SIGNAL</b> —The Enable signal (E) is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the S6800 $\phi 2$ clock.
(13)	R/W	<b>READ/WRITE CONTROL SIGNAL</b> —The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), the ACIA output driver is turned on and a selected register is read. When it is low, the ACIA output driver is turned off and the MPU writes into a selected register. Thus, the Read/Write signal is used to select the Read Only or Write Only registers within the ACIA.
(8)	CS0	<b>CHIP SELECT SIGNALS</b> —These three high impedance TTL compatible input lines are used to address an ACIA. A particular ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from ACIA are then performed under the control of Enable, Read/Write, and Register Select.
(10)	CS1	
(9)	CS2	



**MPU/ACIA INTERFACE (CONT'D)**

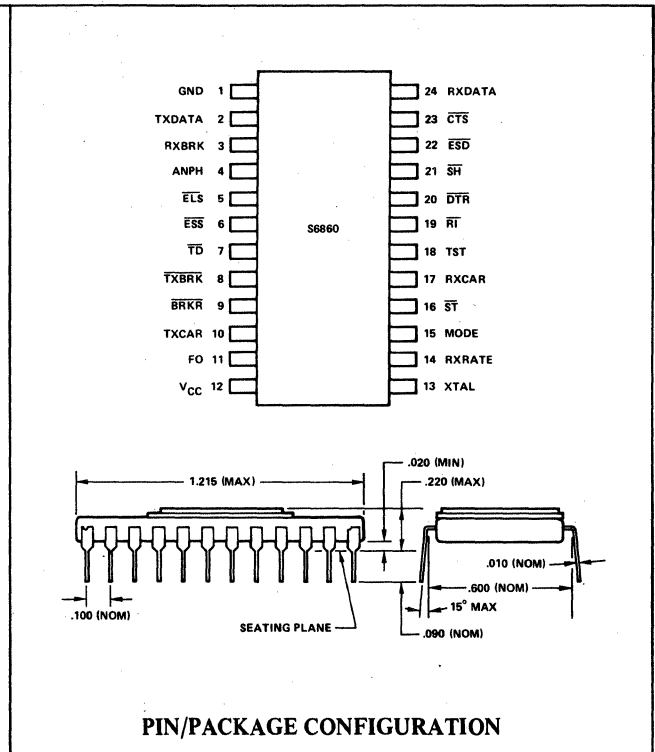
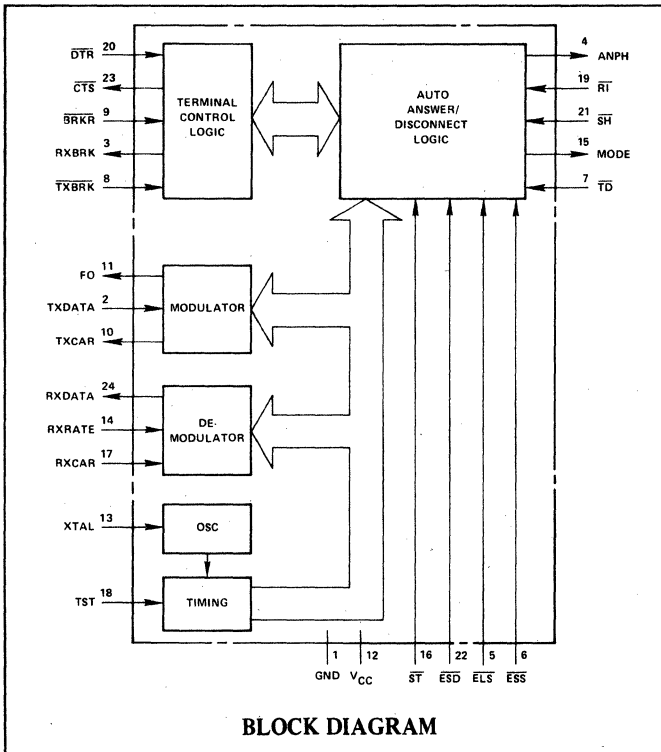
Pin	Label	FUNCTION
(11)	RS	<b>REGISTER SELECT SIGNAL</b> —The Register Select line is a high impedance input that is TTL compatible and is used to select the Transmit/Receive Data or Control/Status registers in the ACIA. The Read/Write signal line is used in conjunction with Register Select to select the Read Only or Write Only register in each register pair.
(7)	$\overline{\text{IRQ}}$	<b>INTERRUPT REQUEST SIGNAL</b> —Interrupt request is a TTL compatible, open drain active low output that is used to interrupt the MPU. The Interrupt Request remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

**ACIA/MODEM OR PERIPHERAL INTERFACE**

Pin	Label	FUNCTION
(4)	CTX	<b>TRANSMIT CLOCK</b> —The Transmit Clock is a high impedance TTL compatible input used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(3)	CRX	<b>RECEIVE CLOCK</b> —The Receive Clock is a high impedance TTL compatible input used for synchronization of received data. (In the $\div 1$ mode, the clock and data must be synchronized externally.) The receiver strobes the data on the positive transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(2)	RXD	<b>RECEIVED DATA</b> —The Received Data line is a high impedance TTL compatible input through which data is received in a serial NRZ(Non Return to Zero) format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 Kbps when external synchronization is utilized.
(6)	TXD	<b>TRANSMIT DATA</b> —The Transmit Data output line transfers serial NRZ data to a modem or other peripheral device. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.
(24)	$\overline{\text{CTS}}$	<b>CLEAR-TO-SEND</b> —This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem's "clear-to-send" active low output by inhibiting the Transmitter Data Register Empty status bit (TDRE).
(5)	$\overline{\text{RTS}}$	<b>REQUEST-TO-SEND</b> —The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The active state is low. The Request-to-Send output is controlled by the contents of the ACIA control register.
(23)	$\overline{\text{DCD}}$	<b>DATA CARRIER DETECTED</b> —This high impedance TTL compatible input provides automatic control of the receiving end of a communications link by means of the modem "Data-Carrier-Detect" or "Received-Line-Signal Detect" output. The $\overline{\text{DCD}}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receiver Interrupt Enable (RIE) is set.
(12)	VCC	+5 volts $\pm$ 5%
(1)	GND	GROUND

# S6860

0-600 BPS  
DIGITAL MODEM



## FEATURES

- Full or half duplex operation
- Originate and answer mode
- Auto answer and disconnect
- Modem self test
- TTL compatible terminal interfaces
- Crystal/External reference control
- Compatible functions for 100 series data sets and 1001 A/B data couplers

## FUNCTIONAL DESCRIPTION

The S6860 is a 0-600 bps Digital Modem circuit designed to be integrated into a wide range of equipment utilizing serial data communications.

The modem provides the necessary modulation, demodulation and supervisory control functions to implement a serial data communications link, over a voice grade channel, utilizing frequency shift keying (FSK) a bit rates up to 600 bps. The S6860 can be implemented into a wide range of data handling

systems, including stand alone modems, data storage devices, remote data communication terminals and I/O interfaces for minicomputers.

N-channel silicon gate technology permits the S6860 to operate using a single voltage supply and be fully TTL compatible.

The modem is compatible with the S6800 microcomputer family, interfacing directly with the Asynchronous Communications Interface Adapter (ACIA) to provide low-speed data communications capability.

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage $V_{CC}$	- 0.3 to +7.0V	Operating Temperature Range $T_A$	0 to 70°C
Input Voltage $V_{IN}$	- 0.3 to +7.0V	Storage Temperature Range $T_{STG}$	- 50 to 150°C

**NOTE:** This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

## DC (STATIC) CHARACTERISTICS

( $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 25^\circ C$  unless otherwise noted.)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT
$V_{IH}$	Input High Voltage, All inputs Except Crystal	2.0	—	$V_{CC}$	Vdc
$V_{IL}$	Input Low Voltage, All inputs Except Crystal	-0.3	—	0.8	Vdc
$V_{IN}$	Crystal Input Voltage (Crystal Input Driven from an External Reference, Input Coupling Capacitor = 200 pF, Duty Cycle = $50 \pm 5\%$ )	1.5	—	2.0	$V_{p-p}$
$I_{IN}$	Input Current ( $V_{IN} = GND$ ) All Inputs Except RXCAR, TXDATA, $\overline{TD}$ , TST, $\overline{RI}$ , $\overline{SH}$ $\overline{RI}$ , $\overline{SH}$ Inputs	—	—	-0.2 -1.6	mAdc
$I_{IL}$	Input Leakage Current ( $V_{IN} = 0$ to 5.0 Vdc)	—	—	1.	$\mu$ Adc
$V_{OH1}$	Output High Voltage, All Outputs Except ANPH and TXCAR ( $I_{OH1} = -0.04$ mAdc, Load A)	2.4	—	$V_{CC}$	Vdc
$V_{OL1}$	Output Low Voltage, All Outputs Except ANPH and TXCAR ( $I_{OL1} = 1.6$ mAdc, Load A)	-0.3	—	0.4	Vdc
$I_{OH2}$	Output High Current, ANPH ( $V_{OH2} = 0.8$ Vdc, Load B)	0.3	—	—	mAdc
$V_{OL2}$	Output Low Voltage, ANPH ( $I_{OL2} = 0$ , Load B)	-0.3	—	0.3	Vdc
$C_{IN}$	Input Capacitance ( $f = 0.1$ MHz)	—	5.	—	pF
$C_{OUT}$	Output Capacitance ( $f = 0.1$ MHz)	—	10	—	pF
$V_{CO}$	Transmit Carrier Output Voltage (Load C)	0.20	0.35	0.50	V(RMS)
$V_{2H}$	Transmit Carrier Output 2nd Harmonic (Load C)	-25	-32	—	dB
$I_{DD}$	$V_{CC}$ Supply Current (All Inputs at GND & All Outputs Open)	—	30	65	mAdc

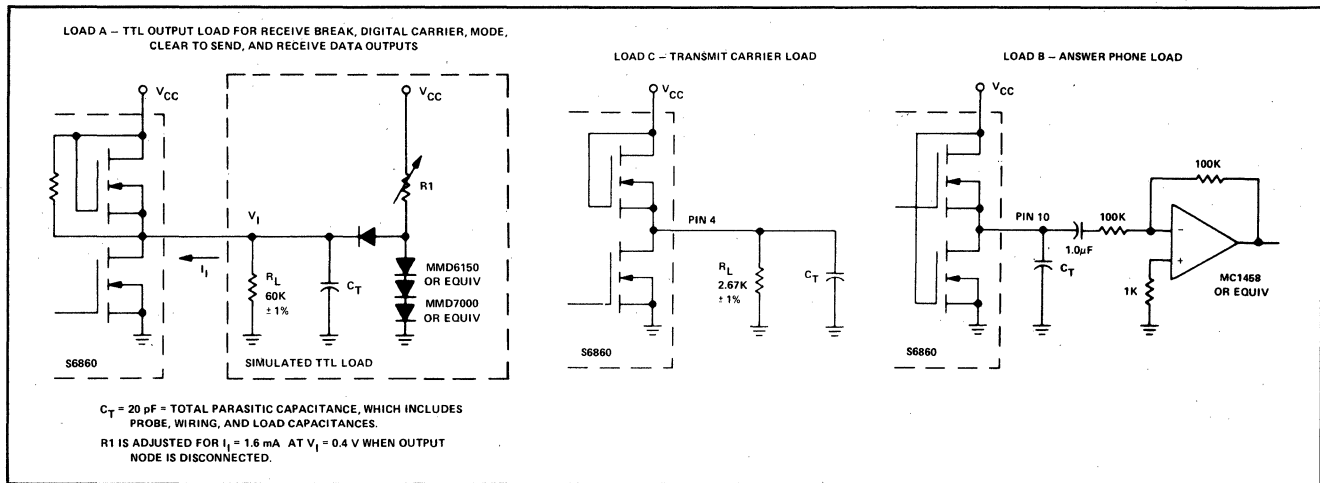
## AC (DYNAMIC) CHARACTERISTICS

(Loading is as shown in Figure 1 unless otherwise noted.)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT
$t_r$	Input Transition Times, All Inputs Except Crystal	—	—	1.*	$\mu$ s
$t_f$	(Operating in the Crystal Input Mode; from 10% to 90% Points)	—	—	1.*	
$t_r$	Input Transition Times, Crystal Input	—	—	30	ns
$t_f$	(Operating in External Input Reference Mode)	—	—	30	
$t_r$	Output Transition Times, All Outputs Except TXCAR	—	—	5.	$\mu$ s
$t_f$	(From 10% to 90% Points)	—	—	5.	

\*Maximum Input Transition Times are  $\leq 0.1 \times$  Pulse Width or the specified maximum of 1.0  $\mu$ s, whichever is smaller.

FIGURE 1 TEST LOADING



MODEM/TERMINAL INTERFACE

PIN	LABEL	FUNCTION
(2)	TXDATA	<b>Transmit Data</b> - Serial data transferred to the modem via the ACIA for transmitting to the receiving terminal.
(8)	$\overline{\text{TXBRK}}$	<b>Transmit Break</b> - Used to signal the remote modem to stop transmitting data. A Transmit Break (low) greater than 34 ms forces the modem to send a continuous space signal for 233 ms. Transmit Break must be initiated only after $\overline{\text{CTS}}$ has been established. This is a negative edge sense input. Prior to initiating $\overline{\text{TXBRK}}$ this input must be held high for a minimum of 34 ms.
(24)	RXDATA	<b>Receive Data</b> - The data resulting from demodulating the Receive Carrier signal. A high level is a mark.
(3)	RXBRK	<b>Receive Break</b> - Upon receipt of a continuous 150 ms space, the modem automatically clamps the Receive Break output high. This output is also clamped high until Clear-to-Send is established.
(9)	$\overline{\text{BRKR}}$	<b>Break Release</b> - The Receive Break output (clamp high condition) can be removed by holding the Break Release signal low for at least 20 $\mu\text{s}$ after receiving a minimum 150 ms space signal.
(20)	$\overline{\text{DTR}}$	<b>Data Terminal Ready</b> - Enables the modem function when low. When $\overline{\text{DTR}}$ is held high for 34 ms minimum, a disconnect is initiated and will occur 3 sec. later.
(23)	$\overline{\text{CTS}}$	<b>Clear-to-Send</b> - A low on the $\overline{\text{CTS}}$ output indicates the Transmit Data input has been unclamped from a steady Mark, thus allowing data transmission.
(16)	$\overline{\text{ST}}$	<b>Self Test</b> - With this input at a low level, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal. Channel establishment, which occurred during the initial handshake, is not lost during self test. The Mode Control output changes state during Self Test, permitting the receive filters to pass the local Transmit Carrier.

$\overline{\text{ST}}$	SH	RT	MODE
H	L	H	H
H	H	L	L
L	L	H	L
L	H	L	H

(18)	TST	<b>Test Clock</b> - A high input signal decreases the modem test time. This input <b>must be low</b> for normal operation.
(11)	FO	<b>Frequency Output</b> - A test signal is output to decrease modem test time. The signal is a square wave at the transmit frequency.

## EXTERNAL MODEM INTERFACE

PIN	LABEL	FUNCTION
(12)	V <sub>CC</sub>	+ 5 Volts ± 5%
(1)	GND	Ground
(22)	$\overline{\text{ESD}}$	<b>Enable Space Disconnect</b> – When $\overline{\text{ESD}}$ is strapped low and $\overline{\text{DTR}}$ is pulsed to initiate a disconnect, the modem transmits a space for either 3 s or until a loss of threshold is detected, whichever occurs first. If $\overline{\text{ESD}}$ is strapped high, data instead of a space is transmitted. A disconnect occurs at the end of 3 s.
(5)	$\overline{\text{ELS}}$	<b>Enable Long Space Disconnect</b> – A strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 1.5 s.
(6)	$\overline{\text{ESS}}$	<b>Enable Short Space Disconnect</b> – A strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 0.3 s. <b>ESS and ELS must not be simultaneously strapped low.</b>
(13)	XTAL	<b>Crystal</b> – A 1.0 MHz crystal is required to use the on-chip oscillator. A 1.0 MHz square wave can also be applied to this pin to satisfy the clock requirements. Crystal parameters are as follows:

Mode:	Parallel
Frequency:	1.0 MHz ± 0.1%
Series Resistance:	750 ohms max
Shunt Capacitance:	7.0 pF max
Temperature:	0 - 70°C
Test Level:	1.0 mW
Load Capacitance:	13 pF

When using the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be ≤ 9 pF at the crystal input.

(14)	RXRATE	<b>Receive Data Rate</b> – The demodulator has been optimized for signal-to-noise performance at 300 bps and 600 bps. The Receive Data Rate input must be low for 0-600 bps and should be high for 0-300 bps.
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## MODEM/DATA COUPLER INTERFACE

PIN	LABEL	FUNCTION
(15)	MODE	<b>Mode</b> – Indicates the Originate (high) or Answer (low) status of the modem. This output changes when a Self Test ( $\overline{\text{ST}}$ ) signal is applied.
(19)	$\overline{\text{RI}}$	<b>Ring Indicator</b> – The modem function will recognize the receipt of a call from the CBT if at least 20 cycles of the 20 - 47 Hz ringing signal (low level ≥ 50% of the duty cycle) are present. The CBS $\overline{\text{RI}}$ signal must be level-converted to TTL according to the EIA RS-232 specification before interfacing it with the modem function. The receipt of a call from the CBS is recognized if the $\overline{\text{RI}}$ signal is present for at least 51 ms. This input is held high except during ringing. A $\overline{\text{RI}}$ signal automatically places the modem function in the Answer Mode.
(21)	$\overline{\text{SH}}$	<b>Switch Hook</b> – Interfaces directly with the CBT type Data Coupler and via the EIA RS-232 level conversion for the CBS type. An $\overline{\text{SH}}$ signal automatically places the modem function in the Originate Mode.  $\overline{\text{SH}}$ is low during origination of a call. The modem will automatically hang up 17 s after releasing $\overline{\text{SH}}$ if the handshaking routine has not been accomplished.

MODEM/DATA COUPLER INTERFACE (Continued)

PIN	LABEL	FUNCTION
(4)	ANPH	<b>Answer Phone</b> – Upon receipt of <u>Ring Indicator</u> or <u>Switch Hook</u> signal and <u>Data Terminal Ready</u> , the Answer Phone output goes high ( $[\overline{SH} + \overline{RI}] \bullet \overline{DTR}$ ). This signal drives the base of a transistor which activates the Off Hook and Data Transmission control lines in the data coupler. Upon call completion, the Answer Phone signal returns to a low level.
(7)	$\overline{TD}$	<b>Threshold Detect</b> – This input is derived from an external threshold detector. If the signal level is sufficient, the $\overline{TD}$ input must be low for 20 $\mu$ s at least once every 32 ms to maintain normal operation. An insufficient signal level indicates the absence of the Receive Carrier; an absence for less than 32 ms will not cause channel establishment to be lost; however, data during this interval will be invalid.  If the signal is present and the level is acceptable at all times, then the threshold input can be low permanently.  Loss of threshold for 51 ms or longer results in a loss of Cler-to-Send. The Transmit Carrier of the originate modem is clamped off and a constant Mark is transmitted from the answer modem.
(17)	RXCAR	<b>Receive Carrier</b> – The FSK input to the demodulators. The local Transmit Carrier must be balanced or filtered out prior to this input, leaving only the Receive Carrier in the signal. The Receive Carrier must also be hard limited. Any half cycle period greater than or equal to 429 $\pm$ 1.0 $\mu$ s for the low band or 235 $\pm$ 1.0 $\mu$ s for the high band is detected as a space.
(10)	TXCAR	<b>Transmit Carrier</b> – A digitally synthesized sine wave derived from a 1.0 MHz crystal reference (see Figure 2). Frequency characteristics are given in the following table.

MODE	DATA	FREQUENCY	TOLERANCE*
Originate	Mark	1270 Hz	- 0.15 Hz
Originate	Space	1070 Hz	- 0.09 Hz
Answer	Mark	2225 Hz	- 0.31 Hz
Answer	Space	2025 Hz	- 0.71 Hz

\*The reference frequency tolerance is not included.

The proper output frequency is transmitted within 3.0  $\mu$ s following a data bit change with no more than 2.0  $\mu$ s phase discontinuity. The typical output level is 0.35 V (RMS) into a 100K-ohm load impedance.

The second harmonic is typically 32 dB below the fundamental (see Figure 3).

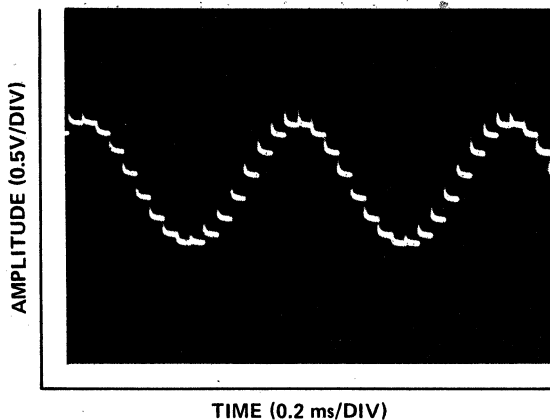


FIGURE 2 TRANSMIT CARRIER SINE WAVE

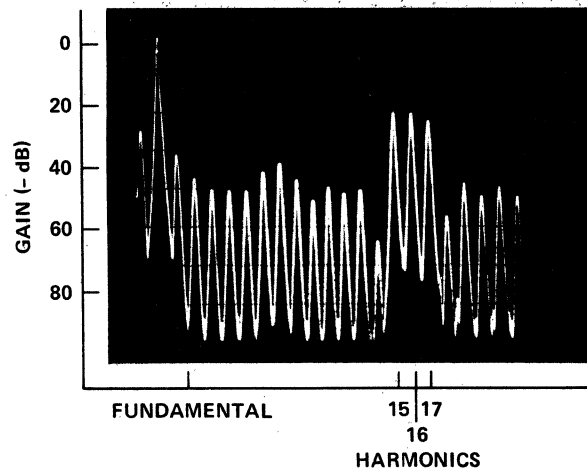
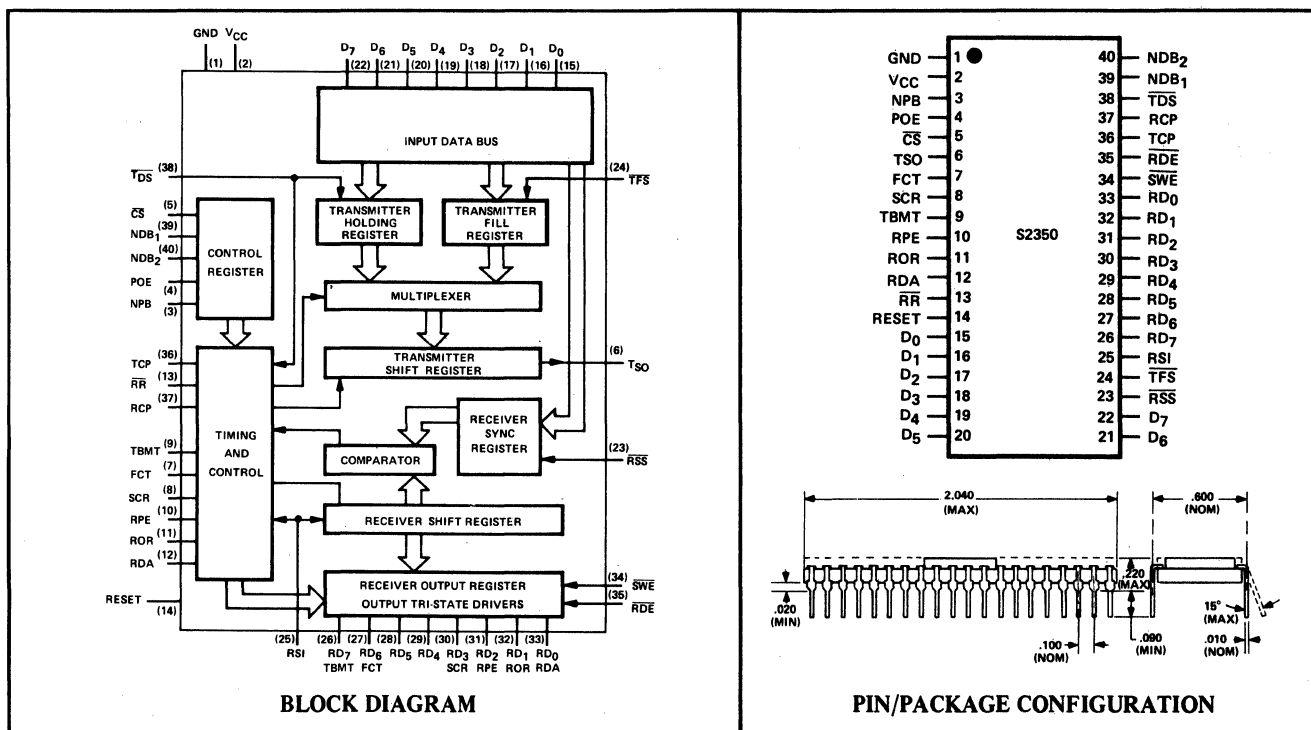


FIGURE 3 TRANSMIT CARRIER FREQUENCY SPECTRUM



### FEATURES

- 500 KHz Data Rates
- Internal Sync Detection
- Fill Character Register
- Double Buffered Input/Output
- Bus Oriented Outputs
- 5-8 Bit Characters
- Odd/Even or No Parity
- Error Status Flags
- Single Power Supply (+5v)
- Input/Output TTL Compatible

### FUNCTIONAL DESCRIPTION

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream, bit synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous for-

matting a 5, 6, 7, or 8 bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8 bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character in the transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

## TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- High Speed Terminals
- Time Division Multiplexing
- Industrial Data Transmission

## ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to + 70°C
Storage temperature	-65°C to +150°C
Positive voltage on any pin with respect to GROUND	+7 volt
Negative voltage on any pin with respect to GROUND	-0.5 volt
Power dissipation	0.75 watt

## DC (STATIC) CHARACTERISTICS\*

V<sub>CC</sub> = +5V ±5% ±5%, T<sub>A</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub>	Volt	V <sub>IN</sub> = 0 to V <sub>CC</sub> Volts
V <sub>IL</sub>	Input Low Voltage	-0.5	+0.8	Volt	
I <sub>IL</sub>	Input Leakage Current		10	μa	
V <sub>OH</sub>	Output High Voltage	2.4		Volts	I <sub>OH</sub> = -100μa
V <sub>OL</sub>	Output Low Voltage		+0.4	Volts	I <sub>OL</sub> = 1.6ma
C <sub>IN</sub>	Input Capacitance		10	pf	} V <sub>IN</sub> = 0 Volt f = 1.0 MHZ
C <sub>OUT</sub>	Output Capacitance		12	pf	
I <sub>CC</sub>	V <sub>CC</sub> Supply Current		100	ma	No Load

\*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

## AC (DYNAMIC) CHARACTERISTICS

V<sub>CC</sub> = +5V ±5%, T<sub>A</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC	500	KHz	

## Input Pulse Widths

PTCP	Transmit Clock	900		nsec	C <sub>L</sub> = 20pf 1TTL Load
PRCP	Receive Clock	900		nsec	
PRST	Reset	500		nsec	
PTDS	Transmit Data Strobe	200		nsec	
PTFS	Transmit Fill Strobe	200		nsec	
PRSS	Receive Sync Strobe	200		nsec	
PCS	Control Strobe	200		nsec	
PRDE	Receive Data Enable	400		nsec	Note 1
PSWE	Status Word Enable	400		nsec	Note 1
PRR	Receiver Restart	500		nsec	

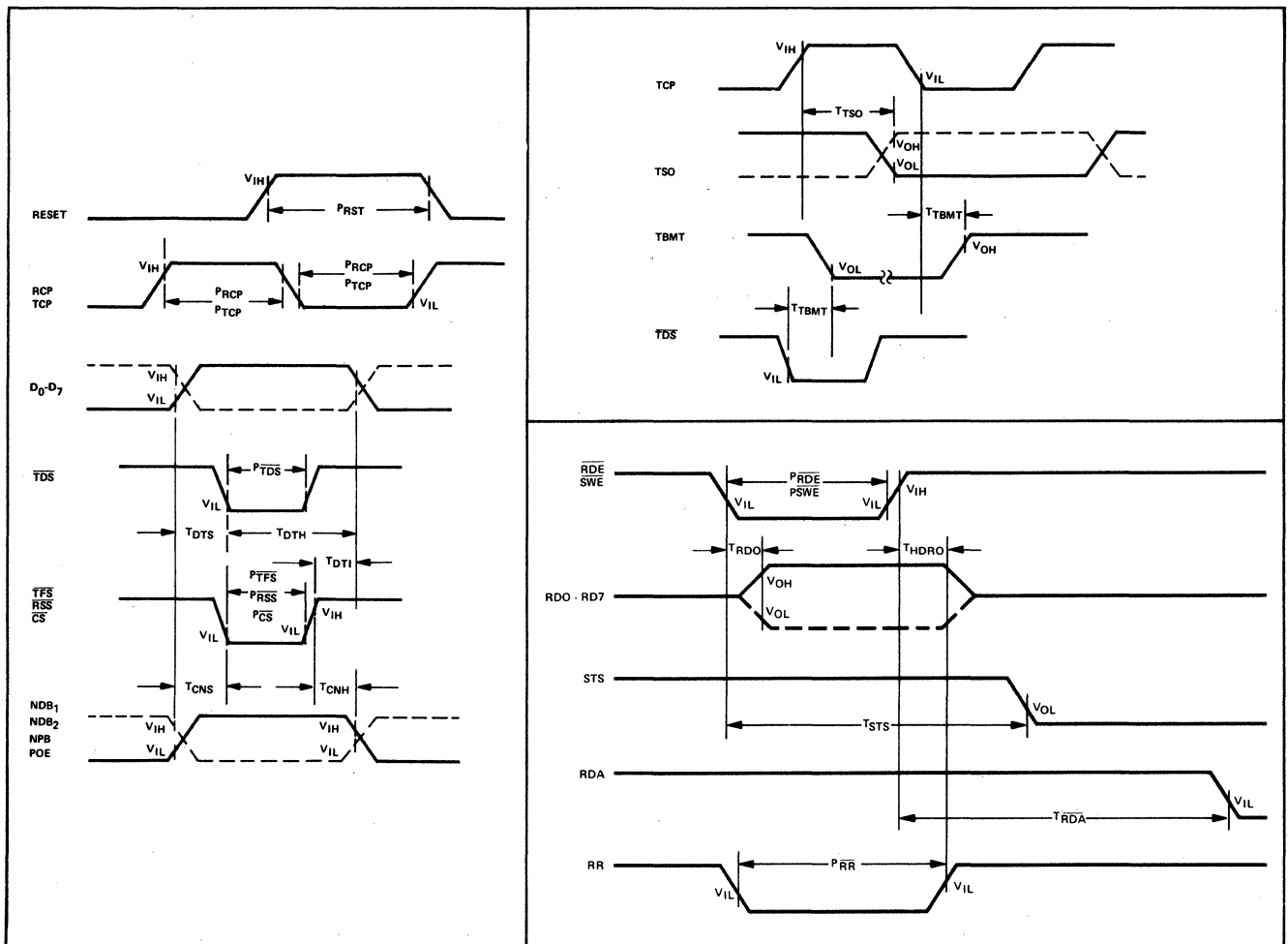


## AC (DYNAMIC) CHARACTERISTICS (CONT'D) SWITCHING CHARACTERISTICS

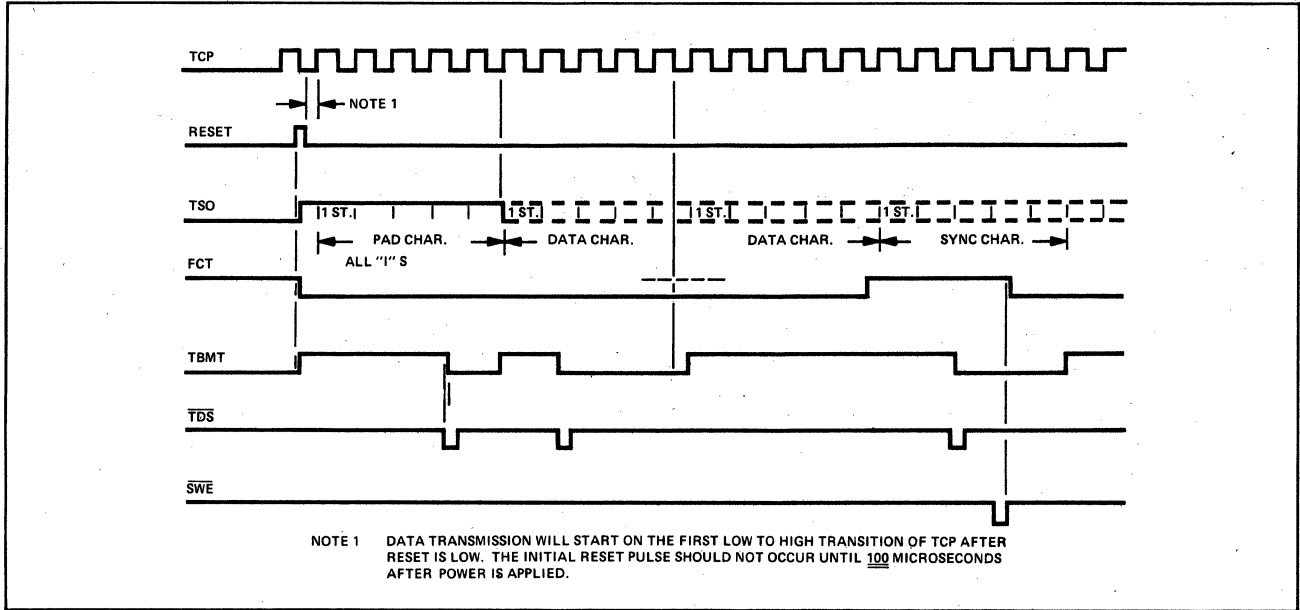
TTSO	Delay, TCP Clock to Serial Data Out		700	nsec	1TTL Load $C_L = 130$ pf
TBMT	Delay, TCP Clock to TBMT Output		1.4	$\mu$ sec	
TBMT	Delay, $\overline{TDS}$ to TBMT		700	nsec	
TSTS	Delay, $\overline{SWE}$ to Status Reset		700	nsec	
TRDO	Delay, $\overline{SWE}$ , $\overline{RDE}$ to Data Outputs		400	nsec	
THRDO	Hold Time $\overline{SWE}$ , $\overline{RDE}$ to Off State		400	nsec	
TDTS	Data Set Up Time $\overline{TDS}$ , $\overline{TFS}$ , $\overline{RSS}$ , $\overline{CS}$	0		nsec	
TDTH	Data Hold Time $\overline{TDS}$	700		nsec	
TDTI	Data Hold Time $\overline{TFS}$ , $\overline{RSS}$	200		nsec	
TCNS	Control Set Up Time NDB1, NDB2, NPB, POE	0		nsec	
TCNH	Control Hold Time NDB1, NDB2, NPB, POE	200		nsec	
TRDA	Delay $\overline{RDE}$ to $\overline{RDA}$ Output	700		nsec	

NOTE 1: Required to reset status and flags.

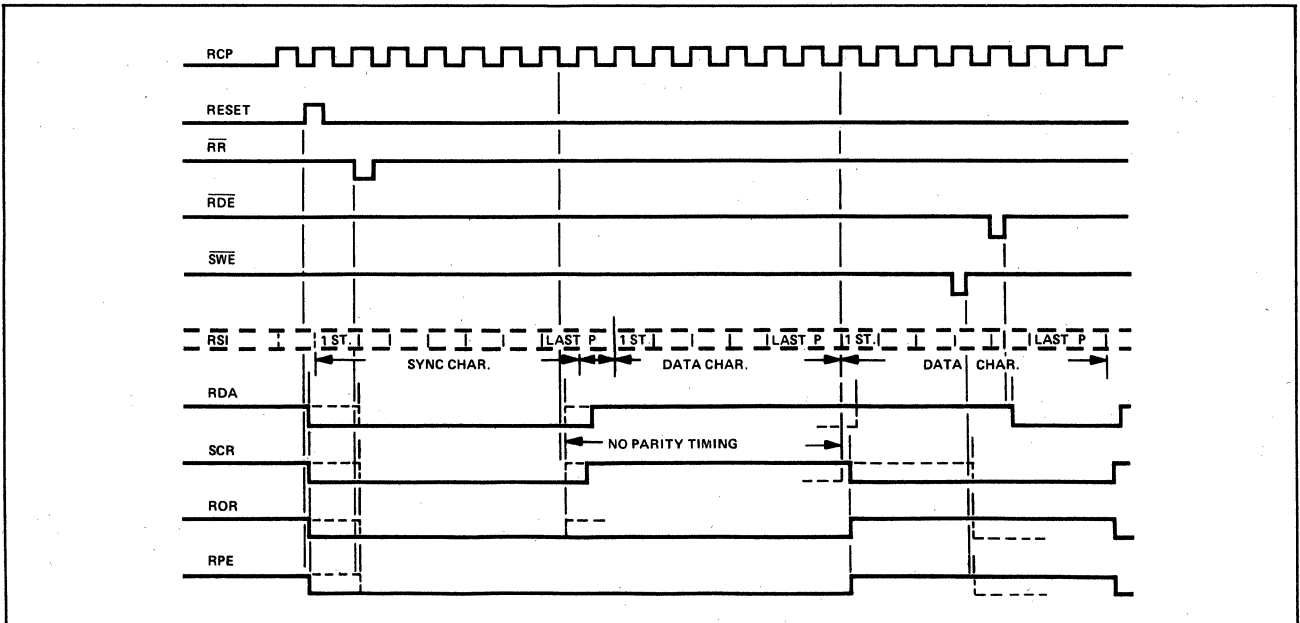
## TIMING WAVEFORMS



TRANSMITTER TIMING DIAGRAM



RECEIVER TIMING DIAGRAM



**MPU/ACIA INTERFACE (CONT'D)**

Pin	Label	Function
(1)	GND	Ground
(2)	V <sub>CC</sub>	+5 VOLTS ±5%
(14)	RESET	<p>MASTER RESET A V<sub>IH</sub> initializes both the receiver and transmitter. The Transmitter Shift Register is set to output a character of all logic 1's. FCT is reset to V<sub>OL</sub> and TBMT set to V<sub>OH</sub> indicating the Transmitter Holding Register is empty.</p> <p>The receiver status is initialized to a V<sub>OL</sub> on RPE, SCR, and RDA. The sync character detect logic is inhibited until a RR pulse is received.</p>
(15)	D0	<p>DATA INPUTS Data on the eight data lines are loaded into the Transmitter Holding Register by <math>\overline{TDS}</math>, the Transmitter Fill Register by <math>\overline{TFS}</math>, and the Receiver Sync Register by <math>\overline{RSS}</math>. The character is right justified with the LSB at D0. For word lengths less than 8 bits, the unused inputs are ignored. Data transmission is LSB first.</p>
(16)	D1	
(17)	D2	
(18)	D3	
(19)	D4	
(20)	D5	
(21)	D6	
(22)	D7	
(38)	$\overline{TDS}$	TRANSMIT DATA STROBE A V <sub>IL</sub> loads data on D0-D7 into the Transmitter Holding Register and resets TBMT to a V <sub>OL</sub> .
(24)	$\overline{TFS}$	TRANSMIT FILL STROBE A V <sub>IL</sub> loads data on D0-D7 into the Transmitter Fill Register. The character in the Transmitter Fill Register is transmitted whenever a new character is not loaded in the allotted time.
(23)	$\overline{RSS}$	RECEIVER SYNC STROBE A V <sub>IL</sub> loads data on D0-D7 into the Receiver Sync Register. SCR is set to V <sub>OH</sub> whenever data in the Receiver Shift Register compares with the character in the Receiver Sync Register.
(9)	TBMT	<p>TRANSMIT BUFFER EMPTY A V<sub>OH</sub> indicates the data in the Transmitter Holding Register has been transferred to the Transmitter Shift Register and new data may be loaded. TBMT is reset to V<sub>OL</sub> by a V<sub>IL</sub> on <math>\overline{TDS}</math>. A V<sub>IH</sub> on RESET sets TBMT to a V<sub>OH</sub>.</p> <p>TBMT is also multiplexed onto the RD7 output (26) when <math>\overline{SWE}</math> is at V<sub>IL</sub> and <math>\overline{RDE}</math> is at V<sub>IH</sub>.</p>
(6)	TSO	TRANSMITTER SERIAL OUTPUT Data entered on D0-D7 are transmitted serially, least significant bit first, on TSO at a rate equal to the Transmit Clock frequency, TCP. Source of the data to the transmitter shift register is the Transmitter Holding Register or Transmitter Fill Register.
(36)	TCP	TRANSMIT CLOCK Data is transmitted on TSO at the frequency of the TCP input in a NRZ format. A new data bit is started on each negative to positive transition (V <sub>IL</sub> to V <sub>IH</sub> ) of TCP.
(26)	RD7	<p>RECEIVED DATA OUTPUTS RDO-RD7 contain data from the Receiver Output Register or selective status conditions, depending on the state of <math>\overline{SWE}</math> and <math>\overline{RDE}</math> per the following table:</p>
(27)	RD6	
(28)	RD5	
(29)	RD4	
(30)	RD3	
(31)	RD2	
(32)	RD1	

MPU/ACIA INTERFACE (CONT'D)

Pin	Label	Function																																																												
(33)	RD0	<table border="1"> <tr> <td>(34)</td> <td>(35)</td> <td>(33)</td> <td>(32)</td> <td>(31)</td> <td>(30)</td> <td>(39)</td> <td>(28)</td> <td>(27)</td> <td>(26)</td> </tr> <tr> <td><math>\overline{SWE}</math></td> <td><math>\overline{RDE}</math></td> <td>RD0</td> <td>RD1</td> <td>RD2</td> <td>RD3</td> <td>RD4</td> <td>RD5</td> <td>RD6</td> <td>RD7</td> </tr> <tr> <td>V<sub>IL</sub></td> <td>V<sub>IL</sub></td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>V<sub>IL</sub></td> <td>V<sub>IH</sub></td> <td>RDA</td> <td>ROR</td> <td>RPE</td> <td>SCR</td> <td>V<sub>OL</sub></td> <td>V<sub>OL</sub></td> <td>FCT</td> <td>TBMT</td> </tr> <tr> <td>V<sub>IH</sub></td> <td>V<sub>IL</sub></td> <td>DB0</td> <td>DB1</td> <td>DB2</td> <td>DB3</td> <td>DB4</td> <td>DB5</td> <td>DB6</td> <td>DB7</td> </tr> <tr> <td>V<sub>IH</sub></td> <td>V<sub>IH</sub></td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> </table> <p>X Output is in the OFF or Tri-State condition            DB0 LSB of Receiver Output Register            DB7 MSB of Receiver Output Register            The two unused outputs are held at V<sub>OL</sub> in the output status condition.</p>	(34)	(35)	(33)	(32)	(31)	(30)	(39)	(28)	(27)	(26)	$\overline{SWE}$	$\overline{RDE}$	RD0	RD1	RD2	RD3	RD4	RD5	RD6	RD7	V <sub>IL</sub>	V <sub>IL</sub>	X	X	X	X	X	X	X	X	V <sub>IL</sub>	V <sub>IH</sub>	RDA	ROR	RPE	SCR	V <sub>OL</sub>	V <sub>OL</sub>	FCT	TBMT	V <sub>IH</sub>	V <sub>IL</sub>	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	X	X	X	X	X
(34)	(35)	(33)	(32)	(31)	(30)	(39)	(28)	(27)	(26)																																																					
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V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	X	X	X	X	X																																																					
(35)	$\overline{RDE}$	RECEIVE DATA ENABLE A V <sub>IL</sub> enables the data in the Receiver Output Register onto the output data lines RD0–RD7. The trailing edge (V <sub>IL</sub> to V <sub>IH</sub> transition) of $\overline{RDE}$ resets RDA to the V <sub>OL</sub> condition.																																																												
(7)	FCT	FILL CHARACTER TRANSMITTED A V <sub>OH</sub> on FCT indicates data from the Transmitter Fill Register has been transferred to the Transmitter Shift Register. FCT is reset to V <sub>OL</sub> when data is transferred from the Transmitter Holding Register to the Transmitter Shift Register, or on the trailing edge (V <sub>IL</sub> to V <sub>IH</sub> ) of the $\overline{SWE}$ pulse, or when RESET is V <sub>IH</sub> . FCT is multiplexed onto the RD6 output (27) when $\overline{SWE}$ is at V <sub>IL</sub> and $\overline{RDE}$ is at V <sub>IH</sub> .																																																												
(25)	RSI	RECEIVER SERIAL INPUT Serial data is clocked into the Receiver Shift Register, least significant bit first, on RSI at a rate equal to the Receive Clock frequency RCP.																																																												
(37)	RCP	RECEIVE CLOCK Data is transferred from RSI input to the Receiver Shift Register at the frequency of the RCP input. Each data bit is entered on the positive to negative transition (V <sub>IH</sub> to V <sub>IL</sub> ) of RCP.																																																												
(12)	RDA	RECEIVED DATA AVAILABLE A V <sub>OH</sub> indicates a character has been transferred from the Receiver Shift Register to the Receiver Output Register. RDA is reset to V <sub>OL</sub> on the trailing edge (V <sub>IL</sub> to V <sub>IH</sub> transition) of $\overline{RDE}$ , by a V <sub>IL</sub> on $\overline{RR}$ or a V <sub>IH</sub> on RESET. RDA is multiplexed onto the RD0 output (33) when $\overline{SWE}$ is V <sub>IL</sub> and $\overline{RDE}$ is V <sub>IH</sub> .																																																												
(8)	SCR	SYNC CHARACTER RECEIVED A V <sub>OH</sub> indicates the data in the Receiver Shift Register is identical to the data in the Receiver Sync Register. SCR is reset to a V <sub>OL</sub> when the character in the Receiver Shift Register does not compare to the Receiver Sync Register, on the trailing edge (V <sub>IL</sub> to V <sub>IH</sub> transition) of $\overline{SWE}$ , by a V <sub>IL</sub> on $\overline{RR}$ or a V <sub>IH</sub> on RESET. SCR is multiplexed onto the RD3 output (30) when $\overline{SWE}$ is a V <sub>IL</sub> and $\overline{RDE}$ is V <sub>IH</sub> .																																																												

**MPU/ACIA INTERFACE (CONT'D)**

Pin	Label	Function															
(34)	$\overline{\text{SWE}}$	<p><b>STATUS WORD ENABLE</b> A <math>V_{IL}</math> enables the internal status conditions onto the output data lines RD0–RD7.</p> <p>The trailing edge of <math>\overline{\text{SWE}}</math> pulse resets FCT, ROR, RPE, and SCR to <math>V_{OL}</math>.</p>															
(11)	ROR	<p><b>RECEIVER OVERRUN</b> A <math>V_{OH}</math> indicates data has been transferred from the Receiver Shift Register to the Receiver Output Register when RDA was still set to <math>V_{OH}</math>. The last data in the Output Register is lost.</p> <p>ROR is reset by the trailing edge (<math>V_{IL}</math> to <math>V_{IH}</math>) of <math>\overline{\text{SWE}}</math>, a <math>V_{IL}</math> on <math>\overline{\text{RR}}</math>, a <math>V_{IH}</math> on RESET or a <math>V_{OL}</math> to <math>V_{OH}</math> transition of RDA.</p> <p>ROR is multiplexed onto the RD1 output (32) when <math>\overline{\text{SWE}}</math> is <math>V_{IL}</math> and <math>\overline{\text{RDE}}</math> is <math>V_{IH}</math>.</p>															
(10)	RPE	<p><b>RECEIVER PARITY ERROR</b> A <math>V_{OH}</math> indicates the accumulated parity on the received character transferred to the Output Register does not agree with the parity selected by POE.</p> <p>RPE is reset with the next received character with correct parity, the trailing edge (<math>V_{IL}</math> to <math>V_{IH}</math>) of <math>\overline{\text{SWE}}</math>, a <math>V_{IL}</math> on <math>\overline{\text{RR}}</math> or a <math>V_{IH}</math> on RESET.</p> <p>RPE is multiplexed onto the RD2 output (31) when <math>\overline{\text{SWE}}</math> is <math>V_{IL}</math> and <math>\overline{\text{RDE}}</math> is <math>V_{IH}</math>.</p>															
(13)	$\overline{\text{RR}}$	<p><b>RECEIVER RESTART</b> A <math>V_{IL}</math> resets the receiver section by clearing the status RDA, SCR, ROR, and RPE to <math>V_{OL}</math>. The trailing edge of <math>\overline{\text{RR}}</math> (<math>V_{IL}</math> to <math>V_{IH}</math>) also puts the receiver in a bit transparent mode to search for a comparison, each bit time, between the contents of the Receiver Shift Register and the Receiver Sync Register. The number of data bits per character for the comparison is set by NDB1 and NDB2. After a compare is made SCR is set to <math>V_{OH}</math>, the sync character is transferred to the Receiver Output Register, and the receiver enters a word synchronous mode framing an input character each word time.</p> <p>NOTE: Parity is not checked on the first sync character but is enabled for every succeeding character.</p>															
(39)	NDB1	<p><b>NUMBER DATA BITS</b> The number of Data Bits per character are determined by NDB1 and NDB2. The number of data bits does not include the parity bit.</p> <table border="1"> <thead> <tr> <th>NDB2</th> <th>NDB1</th> <th>CHARACTER LENGTH</th> </tr> </thead> <tbody> <tr> <td><math>V_{IL}</math></td> <td><math>V_{IL}</math></td> <td>5 Bits</td> </tr> <tr> <td><math>V_{IL}</math></td> <td><math>V_{IH}</math></td> <td>6 Bits</td> </tr> <tr> <td><math>V_{IH}</math></td> <td><math>V_{IL}</math></td> <td>7 Bits</td> </tr> <tr> <td><math>V_{IH}</math></td> <td><math>V_{IH}</math></td> <td>8 Bits</td> </tr> </tbody> </table> <p>For character lengths less than 8 bits, unused inputs are ignored and unused outputs are held to <math>V_{OL}</math>. Data is always right justified with D0 and RD0 being the least significant bits.</p>	NDB2	NDB1	CHARACTER LENGTH	$V_{IL}$	$V_{IL}$	5 Bits	$V_{IL}$	$V_{IH}$	6 Bits	$V_{IH}$	$V_{IL}$	7 Bits	$V_{IH}$	$V_{IH}$	8 Bits
NDB2	NDB1	CHARACTER LENGTH															
$V_{IL}$	$V_{IL}$	5 Bits															
$V_{IL}$	$V_{IH}$	6 Bits															
$V_{IH}$	$V_{IL}$	7 Bits															
$V_{IH}$	$V_{IH}$	8 Bits															
(3)	NPB	<p><b>NO PARITY BIT</b> A <math>V_{IH}</math> eliminates generation of a parity bit in the transmitter and checking of parity in the receiver. With parity disabled, the RPE status bit is held at <math>V_{OL}</math>.</p>															
(4)	POE	<p><b>PARITY ODD/EVEN</b> A <math>V_{IH}</math> directs both the transmitter and receiver to operate with even parity. A <math>V_{IL}</math> forces odd parity operation. NPB must be <math>V_{IL}</math> for parity to be enabled.</p>															
(5)	CS	<p><b>CONTROL STROBE</b> A <math>V_{IL}</math> loads the control inputs NDB1, NDB2, POE, and NPB into the Control Register. For static operation, <math>\overline{\text{CS}}</math> can be tied directly to ground.</p>															

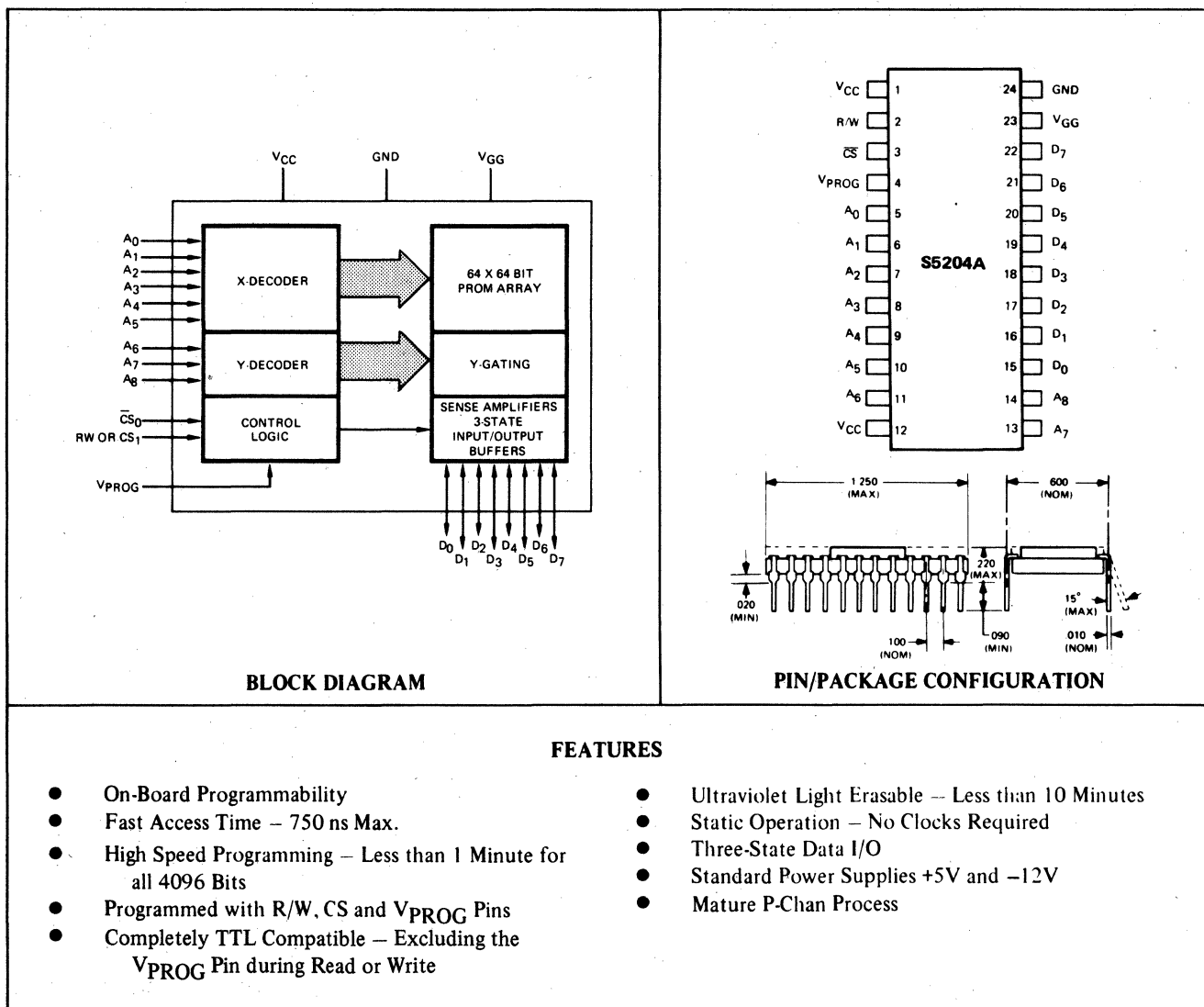
# S5204A

512 X 8 BIT  
ERASABLE AND  
ELECTRICALLY REPROGRAMMABLE  
READ ONLY MEMORY

# AMI

AMERICAN MICROSYSTEMS, INC.

## ADVANCED PRODUCT DESCRIPTION



## FEATURES

- On-Board Programmability
- Fast Access Time – 750 ns Max.
- High Speed Programming – Less than 1 Minute for all 4096 Bits
- Programmed with R/W, CS and VPROG Pins
- Completely TTL Compatible – Excluding the VPROG Pin during Read or Write
- Ultraviolet Light Erasable – Less than 10 Minutes
- Static Operation – No Clocks Required
- Three-State Data I/O
- Standard Power Supplies +5V and -12V
- Mature P-Chan Process

## FUNCTIONAL DESCRIPTION

The S5204A is a high speed, static, 512 x 8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL com-

patible during both read and write modes. Packaged in a 24 pin hermetically sealed dual in-line package the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written.

## TYPICAL APPLICATIONS

- ROM Program Debugging
- Code Translation
- Microprogramming
- Look-up Tables
- Random Logic Replacement
- Programmable Waveforms
- Character Generation
- Electronic Keyboards

# AMI 6800 Microcomputer Systems Support

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## HARDWARE/SOFTWARE SUPPORT AIDS

The S6800 Microcomputer Family hardware is completely supported by an array of application program development software, various levels of hardware and software reference documentation, a software development station, and a hardware prototyping evaluation board. These comprehensive software and hardware aids have many advanced timesaving features that make the S6800 software/hardware support structure the most modern and convenient.

The Microprocessor Development Center is a complete self-contained S6800 microcomputer/keyboard/CRT, with a floppy disc. It provides the user with a complete, convenient, and economical hardware and software development facility. The MDC software includes an Assembler, Text Editor, and extensive Debug and Trace Package, and hardware Test Programs.

The EVK Series prototyping boards are fully functional microcomputers, with the MPU, ROM, RAM, and PROM memory, as well as I/O provisions on the board. The S6800 bus extends to the edge connector, so that any amount of external I/O can be connected also. It has a resident operating system program stored in ROM and all PROM programming hardware is right on the board. This board can be used for circuit evaluation, PROM programming, or as a microprocessor board in low quantity systems.

**Cross-Assembler.** The AMI 6800 Cross-Assembler is designed to operate on large-scale computers and converts S6800 Assembly Language input statements into machine language for the purpose of generating application programs. It defines the form and syntax according to which the S6800 instruction set can be structured into statements and thus forms the backbone for the usage of the S6800 Microcomputer System. The Cross-Assembler contains many advanced programming features for convenience and efficiency.

- **Full Macro Capability** – a sequence of instructions and associated variable parameters can be designated by a symbolic label. The assembler will substitute the complete sequence for the label, wherever the label is called out.

- **Conditional Assembly** – when parts of a program are the same for different versions of the program, the conditional assembly feature can be used to instruct the assembler to automatically include only those parts needed for a particular version of the program.
- **Relocatable Program Segments** – the object code within a program segment is always defined with respect to the start of the segment, thus allowing the Linking Loader to assign actual memory addresses later. This gives maximum flexibility in final assembly.

The Cross-Assembler is available for computers supporting standard ANSI FORTRAN IV. For low-cost, high-speed program development, it is also written in SYSTEM 360/370 BAL and is available through timesharing networks, such as National CSS, Inc.

**Linking Loader.** – The Linking Loader is a program used to assign fixed memory locations to programs generated by the Cross-Assembler and thus structure the users program for a particular memory configuration. The Linking Loader is programmed to operate on the same (large-scale) computer as the Cross-Assembler and is also available on timesharing networks (NCSS and others). It can be used to produce a listing of the external definitions and load map, and a program tape suitable for a prototype system hexadecimal loader or a PROM programmer. Alternatively, it can also generate memory image file for use by the AMI S6800 Simulator program described below.

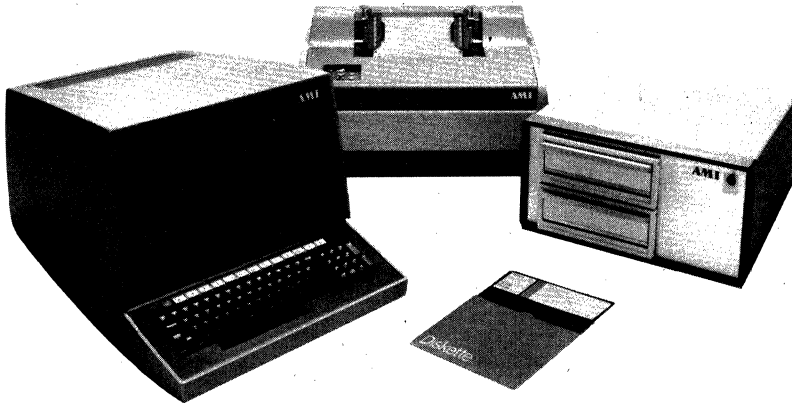
**Simulator.** – The AMI S6800 Simulator program is a means by which the user can conveniently check out the operation of programs written for the S6800. It is a program that can be operated on a cross-computer (other than S6800) and cause that computer to respond the same as a S6800 would.

The simulator simulates all S6800 Microprocessor hardware. A complete set of commands is provided for loading and examining the simulated registers and memory, and for controlling the simulator.

## AMI 6800 Microcomputer Development Center

What is the AMI 6800 MDC? An intelligent standalone software development and hardware debugging station, serving completely the combined needs of the design engineer and the programmer. It consists of a S6800 based CRT/keyboard microcomputer terminal, a dual drive floppy disc memory, and an optional hard copy printer.

A program in development (or in operation) can be viewed on the CRT and edited on the keyboard. Program files can be assembled and stored in the floppy disk memory, under control of the disk memory operating system software. The modular bus oriented card cage in the CRT terminal provides versatile facilities for developing and testing 6800 hardware.



### CRT/Keyboard Terminal

- Capability for generating 256 unique ASCII input characters
- 12-inch diagonal CRT display – 25 lines of 80 characters
- 16 K bytes of user available RAM, expandable to 48 K
- Full cursor and editing controls
- Special function controls
- Peripheral interconnects

### Floppy Disk Memory

- IBM 3740 data format compatible
- Data storage capacity of 256,256 bytes per diskette
- Provides instant on-line access to over 500,000 bytes and virtually unlimited removable media storage
- Fully supported by FDOS-II Disk Operating and File Management System software
- Two full-sector buffers enable completely asynchronous data transfer at rates up to 500,000 bytes per second
- Diskettes available from AMI and multiple other sources

### Standard MDC Card Modules

- S6800 MPU Card
- EPROM/ROM Program Storage Card
- RAM Card
- Keyboard/Telecommunications Card
- Debug Card
- Peripheral Interface Card
- EPROM Programmer Card
- CRT Driver and Refresh RAM Cards

### Optional Matrix Printer

Completely self contained impact printer, 120 cps, sprocket-fed, handles paper widths from 4 to 9½ inches. Can print original and four copies. Standard print format is 10 characters per inch horizontal, 6 lines per inch vertical. Buffered, 75,000 cps parallel transfer, optional serial interfaces allow from 100 to 9600 baud serial transfer.



## MDC Hardware Capabilities

The AMI 6800 MDC is a multifunction development center that single-handedly satisfies your requirements for software development, hardware development, and prototype checkout. The MDC can also double as a standalone communications terminal, a general purpose data processing system, or as an incoming parts tester.

**Software Development** – write, debug and operate S6800 programs on the CRT terminal, using its internal RAM and the dual drive floppy disc for storage. The MDC comes with a full complement of support software, including the FDOS-II Disk Operating and File Management System, a Text Editor, an Assembler, Debugger, Trace, Telecommunications and Utilities.

**Hardware Development** – breadboard such circuitry as interfaces or memories right on the MDC wirewrap prototyping board and plug into the CRT terminal card cage to operate with the MDC's S6800 based central processor in solving

development problems. Use the control panel type functions of the CRT terminal for single step, stop-on-address, display, alter, and other similar program operations. The bus oriented card cage, position interchangeable plug-in card modules, and an extender card provide the flexibility to make hardware development easy. There is also a complete keyboard controlled PROM programmer within the CRT terminal.

**Prototype Checkout** – with the advantages of a real-time test environment, rapid test program retrieval, single or multiple step execution, and hardware as well as software breakpoints, the checkout of prototype S6800 circuitry is easy and efficient.

**Standalone Communications Terminal** – the CRT terminal has both RS-232 and current loop interfaces, supported by telecommunications firmware, for operation as a general purpose standalone intelligent terminal.

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## MDC Software Capabilities

The AMI 6800 MDC offers total facilities for rapidly developing applications and systems software. The entire MDC software system is at the user's instant disposal – a few simple keystrokes are needed to instantly access and execute any program. The FDOS-II disk based operating system provides complete system resource control to the programmer.

**FDOS-II Disk Operating and File Management System** – contains a resident module for bootstrapping the floppy disk memory and for disk I/O handling. It also contains an executive that performs all of the disk memory command line interpretations, file management and operational functions of the dual disk system. In addition, there are utility I/O and EPROM programming routines in FDOS-II.

**The Text Editor** – program provides the means for rapidly creating, examining and modifying stored files. The total capability of MDC's Text Editor exceeds that of many large minicomputer systems, and includes such features as string searches and string substitutions.

**The Symbolic Assembler** – translates assembler language statements into executable machine language code. In conjunction with FDOS-II Operating and File Management System, assembling has been reduced to a series of simple operator keystrokes. Results of the assembly, automatically stored on disk, are immediately available for reference or execution.

**MDC's Extensive Debug Program** – effectively automates the functions of a computer control panel. Given control by simply pressing the DEBUG key or via program traps, Debug immediately responds with the display of machine and program status. Additional functions include:

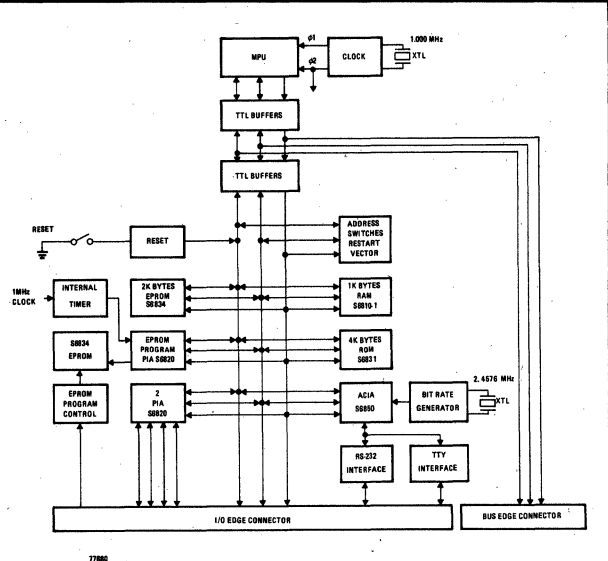
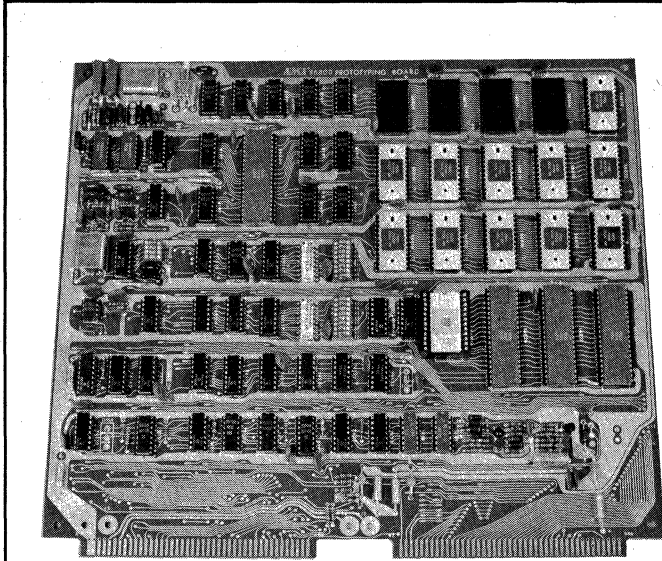
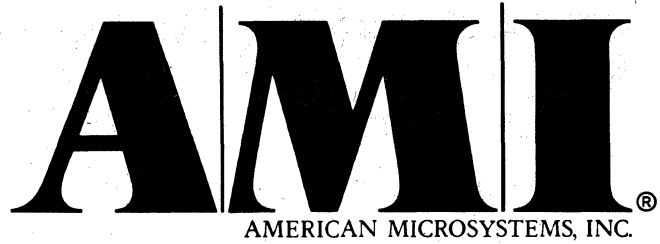
- Register/data display and modification
- Instruction/subroutine step
- User definable debug macros
- Snapshot debug data of a running program
- Breakpoints (stop-on-address compare)
- Comment and header line displays

**MDC's Trace Package** – gives Debug the ability to display a trace of machine register contents, instruction mnemonics and operands before execution of any instruction or subroutine in the user's program. Microprocessor debugging has never been made easier.

**MDC's Test Programs** – are a set of self-test and diagnostics which verify that the hardware associated with the MDC is operating correctly. The programs are also helpful in isolating malfunctioning components. The program for testing the basic hardware is resident in EPROM and is activated by the keyboard TEST key.

# EVK200 EVK300

PROTOTYPING BOARDS



**BLOCK DIAGRAM**

## FEATURES

- 4 K bytes ROM
- 2K Bytes EPROM (EVK300)
- 512 Bytes EPROM (EVK200)
- 1K Bytes RAM
- EPROM Programming for S6834
- 3 PIA's = 58 I/O Lines
- TTY Current Loop or RS232 Interface
- TTY Operating System Program
- ROM Subroutine Program Library
- Totally Buffered MPU Lines
- Single +5V Power Supply except when using EPROMs or RS232 Interface
- Restart Address Selection
- Selectable DMA Mode
- Interval Timer
- Tiny Basic

## FUNCTIONAL DESCRIPTION

The EVK Series Prototyping Board is a single PCB, hardware/software prototyping system. It allows system development using a functionally compatible system and reduced development time. With this board, the basic 6800 family parts (S6800, S6810-1, S6820, S6830, S6834 and S6850) can be evaluated. It can also serve as a general purpose microcomputer for low volume systems to which the user can easily add I/O and memory. The 10½" x 12" card has two edge connectors, one for the MPU Bus and one for I/O. The EVK 300 is a fully assembled board, but the EVK 200 is in a kit form.

All of the S6800 microprocessor lines are available at the bus edge connector and are buffered to allow 40 mA of drive capacity for expanding the development system. The standard system clock is adjustable from 300 kHz to 1MHz by using the potentiometers on the board. An optional 1 MHz crystal may be selected to control the accuracy for those applications requiring critical timings.

An on-board interval timer gives 1 ms and 100µs timing marks for general use and for EPROM programming. Three types of DMA operation are possible using the Prototyping Board, Halt Processor, Cycle Steal or Multiplexing.

## MEMORY

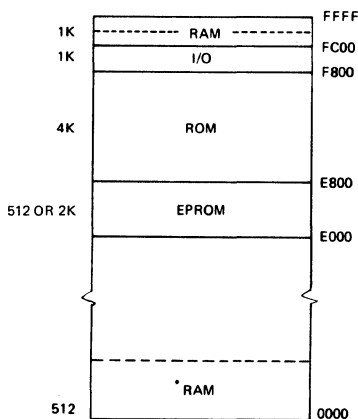
Memory and I/O addresses are assigned to the upper 8K bytes of the available memory space. (See memory map for address assignments.) This gives the system developer the flexibility to use the remaining 56K bytes as he wishes. All of the memory and I/O on the board may be disabled externally by an edge connector line called MEMORY DISABLE, leaving the MPU free to operate totally in an external memory.

The S6831 ROM contains the Prototype Operating Library (PROTO) and a ROM Subroutine Library (RS)<sup>3</sup>. The 2K of EPROM locations may also be used for program verification.

The RAM is assigned to the upper 1K of available memory space. The PROTO and (RS)<sup>3</sup> programs require about 256 bytes of this RAM so the rest is available for general programming. With all restart vectors automatically assigned to the upper memory addresses, restart vectoring is forced from a set of 16 switches. This allows the restart address to be vectored to any memory location.

The RAM has further been divided into two 512 byte sections such that the upper 512 bytes remain fixed in the assigned address block and the lower 512 bytes are moveable through a switch selection option. 512 bytes of RAM are relocatable to the lowest address space to take advantage of the S6800's direct addressing mode. This is only recommended if no external memory is added. When adding external memory, it is advisable to use the RAM in the upper address space and the external memory as the low addresses.

### ADDRESS ASSIGNMENT MEMORY MAP



\*Optional Low order RAM assignment

### I/O

An S6850 ACIA is used to provide a 20 mA current loop interface to a TTY or RS232 terminal. A 20 mA current loop interface and an EIA RS232 interface are both available on the board. A bit rate generator allows operation using any of the standard communication frequencies (see table) so a large variety of terminal types can be used.

Three S6820 PIAs allow up to 58 I/O lines, giving flexibility in I/O through the parallel interfaces.

### Communication Frequencies (baud)

50	600
75	1200
110	1800
134.5	2400
150	4800
200	9600
300	19.2K

### EPROM PROGRAMMING

Unique to the AMI 6800 Prototyping Board is the ability to program S6834 EPROMs (512 x 8) on the board. The programming software can program an EPROM from any memory location, RAM, ROM or EPROM. It can verify a word and, if desired, change a single bit in the EPROM, provided that the change is from LOW to HIGH.

### SOFTWARE

The Prototyping Board Software is comprised of a TTY Operating Program (PROTO) and is supported by a ROM Subroutine Library (RS)<sup>3</sup>. The PROTO program operates on the following commands:

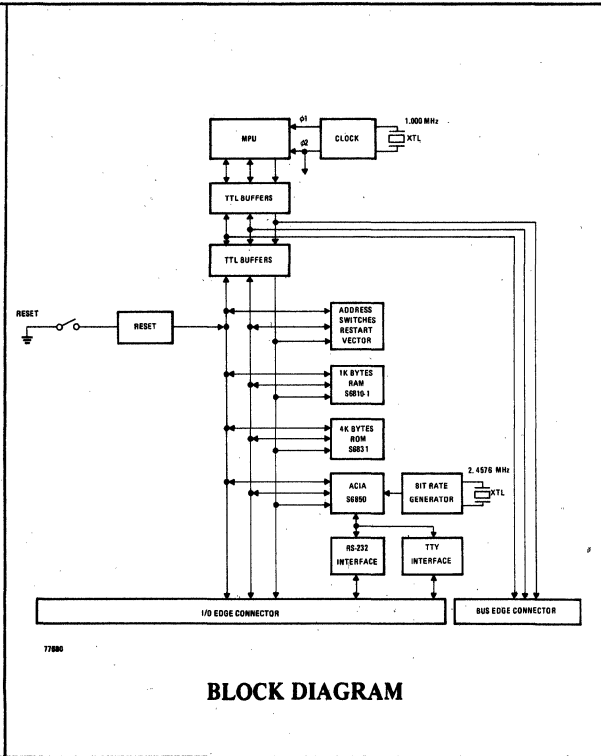
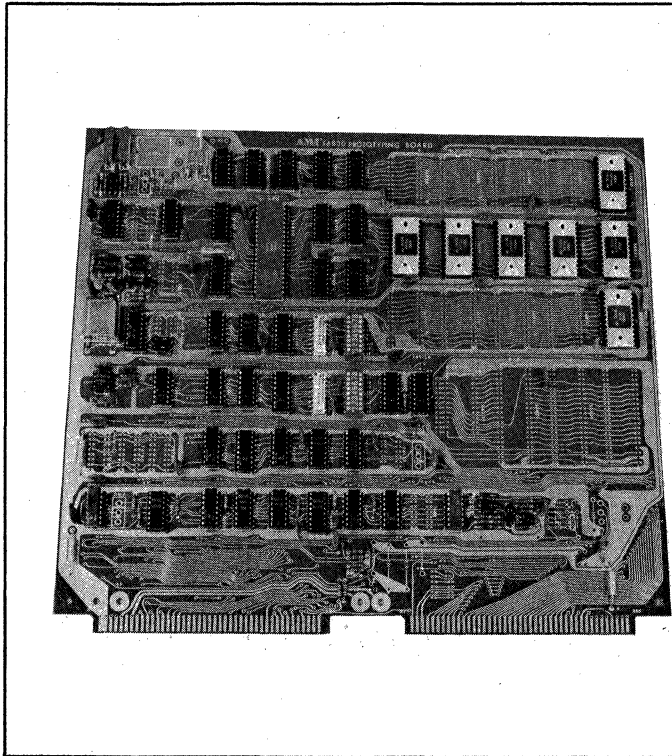
- L Load Memory from TTY paper tape
- P Punch Memory to TTY paper tape
- S Set Memory to a given value
- D Display the contents of a memory location
- G Go to a specific address and begin program execution
- R Print contents of MPU registers on the TTY
- B Burn (program) an EPROM from Memory location indicated
- V Verify the contents of an EPROM with a specified memory location
- M Move a specific block of memory to a designated location
- E Punch end of tape

### AN EXCLUSIVE BONUS — AMI 6800 TINY BASIC

—a high level interpretive language derived from the standard Dartmouth Basic. Furnished to EVK 300 users at no charge upon submittal of warranty registration.

# EVK99 EVK100

PROTOTYPING KIT



## FEATURES

- 2K Bytes ROM
- 512 Bytes RAM
- TTY Current Loop Interface
- TTY Operating System Program
- PROTO and (RS)<sup>3</sup>
- Totally Buffered MPU Lines
- Single +5V Power Supply
- Restart Address Selection
- Expandable to EVK 300

## FUNCTIONAL DESCRIPTION

The EVK 100 Prototyping Board is a kit for a single PCB, hardware/software prototyping system. It allows system development using a functionally compatible system and reduced development time. With this board, the basic 6800 family parts (S6800, S6810-1, S6820, S6830, S6834 and S6850) can be evaluated. It can also serve as a general purpose microcomputer for low volume systems to which the user can easily add I/O and memory. The 10½" x 12" card has two edge connectors, one for the MPU Bus and one for I/O.

All of the S6800 microprocessor lines are available at the bus edge connector and are buffered to allow 40 mA of drive

capacity for expanding the development system. The standard system clock is adjustable from 300 kHz to 1MHz by using the potentiometers on the board.

The EVK 99 is a minimum kit that includes the printed circuit board, the S6800 MPU, four S6810 RAMs (128 bytes each), one S6831 ROM, the S6820 Peripheral Interface Adapter, and the S6850 Asynchronous Communications Interface Adapter. The circuit board is identical to all other EVK Series boards and therefore allows expansion to any more complex EVK configuration.

# 4

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## **Communications and Interface Circuits**



## Data and Telecommunications Circuits

Part No.	Description	Word Length (Bits)	Max. Clock Freq. (KHz)	Input/Output	Power Supply (V)	Process	Packages
S1883	Asynchronous Receiver/Transmitter	5, 6, 7, 8	200	TTL	-12,±5	P-1 <sup>2</sup>	S,P
S2350	Synchronous Receiver/Transmitter	5, 6, 7, 8	500	TTL	+5	N-SiGate	S,P
S2559	Digital Tone Generator	N/A	N/A	TTL-MOS	+3.5 to +13	CMOS	P
S6850	Asynchronous Receiver/Transmitter	7,8	800	TTL	+5	N-SiGate	E,P

## Remote Control Circuits

Part No.	Description	No. of Control Functions	I/O Bits	Power Supply (V)	Process	Packages
S2600	Remote Control Transmitter	31 (10 dedicated)	11	+7 to +10	CMOS	P
S2601	Remote Control Receiver	31 (10 dedicated)	5	+10 to +18	P-1 <sup>2</sup>	P

## TouchControl Interface Circuits

Part No.	Description	Power Supply (V)	I/O	Power Dissip. (mW)	Process	Packages
S9260/61	7-switch Interface	-13.5 to -18	MOS/TTL	200	P-1 <sup>2</sup>	P
S9262	14-switch Interface <sup>(3)</sup>	-13.5 to -18	MOS/TTL	200	P-1 <sup>2</sup>	P
S9263/64/65	16-switch Interface	-13.5 to -18	MOS/TTL	200	P-1 <sup>2</sup>	P
S9266	32-switch Interface <sup>(3)</sup>	-13.5 to -18	MOS/TTL	200	P-1 <sup>2</sup>	P
TCK100 TouchControl Demonstration Kit—a complete TouchControl switch panel with S9263 for demonstrating its use with LEDs and/or connecting to your logic circuitry.						



### THE TOUCHCONTROL CONCEPT

The S9260 series of MOS TouchControl interface circuits permit almost any control panel containing mechanical switches to be easily replaced by a flat-surface capacitive control panel providing superior styling, reliability, ease of cleaning, and safety. Connecting directly to a screened or etched pattern on the panel's reverse side, these MOS circuits provide outputs to drive a variety of logic systems from household appliances to industrial controls. All system functions are then selected by merely touching the flat conductive TouchControl "switch" areas that have been deposited on the panel's front surface in practically any configuration desired.

The S9260, S9261, S9263, S9264, and S9265 circuits provide an individual output for each of up to 16 TouchControl switches. For applications requiring more switches or encoded outputs, refer to AMI's S9262 and S9266, which can interface with up to 32 switches.

### TYPICAL APPLICATIONS

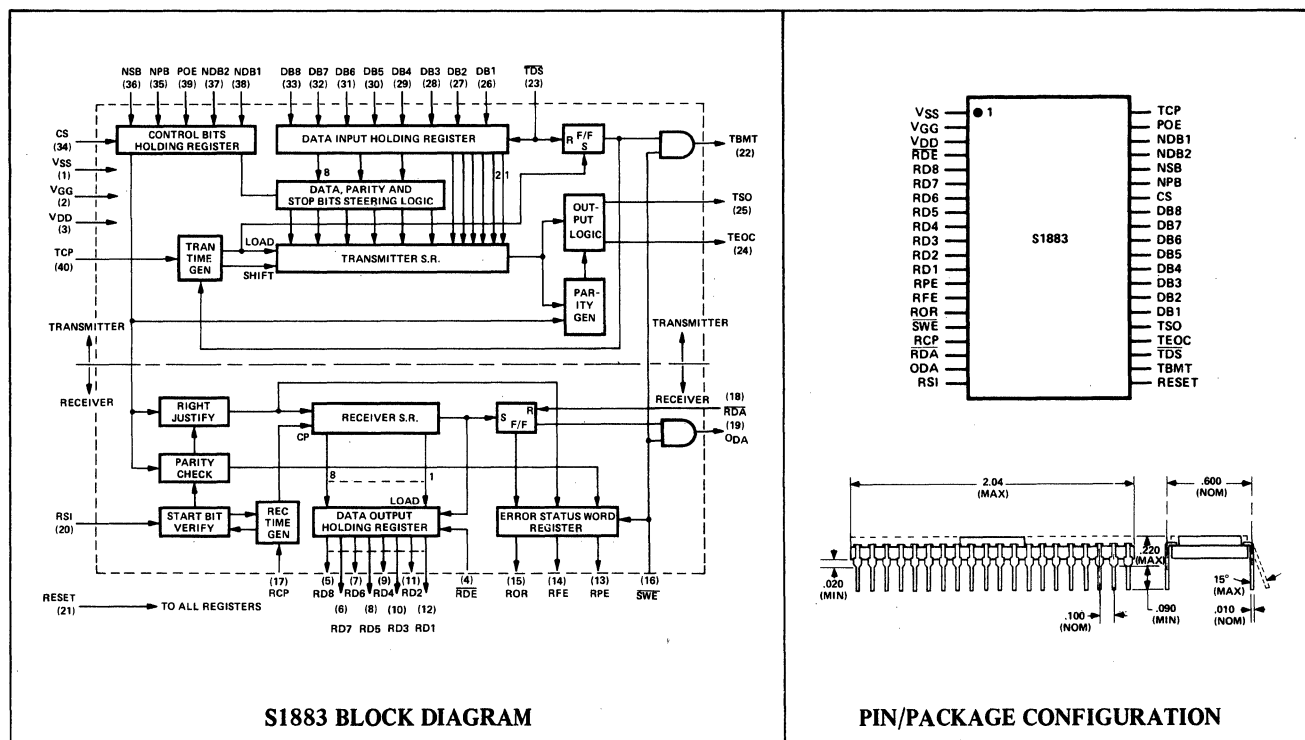
- Appliance Control Panels
- Home Entertainment Systems
- Power Tool Controls
- Television Sets
- Automotive Controls
- Telephones
- Games
- Fast Food Waterproof Keyboards
- Moisture Proofing
- Industrial Controllers
- Computer Terminals
- Keyboards
- Instrumentation
- 16 to 1 Multiplexers
- Microprocessor Interface
- Vending Machines
- Cash Registers

## Future Products

### TELECOMMUNICATIONS CIRCUITS

**Auto Dialer (S2560)** — a CMOS dialer with BCD display output; operates directly from telephone line.

**Tone Ringer (S2561)** — a CMOS externally triggerable bell ringer simulator.



**S1883 BLOCK DIAGRAM**

**PIN/PACKAGE CONFIGURATION**

### FEATURES

- 12.5 K Baud Data Rates
- 5-8 Bit Word Length
- Parity Generation/Checking Odd, Even, None
- Framing and Overflow Error Detection
- 1, 1.5, or 2 Stop Bits
- Double Buffered Input/Output
- Independent Transmit/Receive Rates
- Start and Stop Bits Generated and Detected
- Interchangeable with TMS6011, COM2017, TR1602, AY-5-1013
- Tri-State Outputs

### FUNCTIONAL DESCRIPTION

The S1883 Universal Asynchronous Receiver Transmitter (UART) is a single chip MOS/LSI device that totally replaces the asynchronous parallel to serial and serial to parallel conversion logic required to interface a word parallel controller or data terminal to a bit serial communication network.

For asynchronous data transmission with a non-contiguous data bit stream, the UART automatically inserts a START bit preceding each character and under program control 1, 1.5, or 2 stop bits at the end of each character. To detect incoming characters in a noisy environment the UART employs a START bit detection network and allows errorless recovery of data with up to 42% distortion.

The UART will transmit or receive data characters of 5, 6, 7, or 8 bit length. Options allow the generation and checking of

odd, even parity or no parity. The odd or even parity bit is automatically added to the character length for transmission. The parity bit is removed, checked and an error flag set if incorrectly received.

The data or baud rate at the receiver input and transmitter output are determined independently by external clock inputs. The clock inputs must be 16 times the data rate required at the serial input and output. The independent clocks allow for either half or full duplex operation.

The UART provides a buffer register in both the transmitter and receiver to allow a full character time for responding to a received data ready or transmit data request signal. The UART generates a MARK signal if the transmit register is not loaded with a data character and also indicates an overflow error if two characters are received without a RDA input.

**TYPICAL APPLICATIONS**

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- Industrial Data Transmission
- TTY Terminals
- Time Division Multiplexing

**ABSOLUTE MAXIMUM RATINGS**

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Positive Voltage on Any Pin with Respect to VSS	+3 Volt
Negative Voltage on Any Pin with Respect to VSS	-20.0 Volt

**NOTE:** Stresses greater than those listed as Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operation section of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC (STATIC) CHARACTERISTICS**       $T_A = 0^\circ - +70^\circ\text{C}$ ,  $V_{SS} = +5 \text{ Volt} \pm 5\%$ ,  $V_{GG} = -12 \text{ Volt} \pm 5\%$

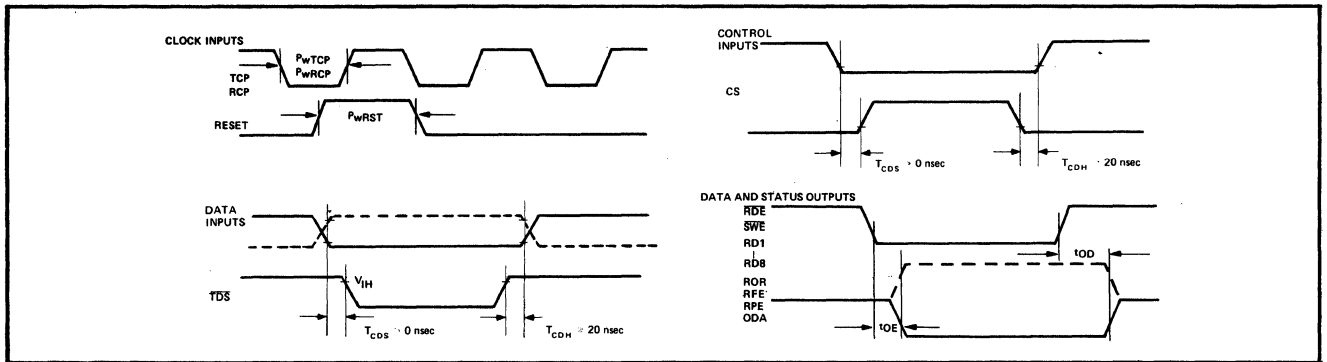
Symbol	Parameter	Min	Max	Unit	Condition
V <sub>IH</sub>	Input High Voltage	V <sub>SS</sub> - 1.0	V <sub>SS</sub> + 0.3	Volt	Internal Pull-up Resistor Provided
V <sub>IL</sub>	Input Low Voltage	V <sub>GG</sub>	0.8	Volt	
I <sub>LI</sub>	Input Load Current		-1.2	mamp	V <sub>IN</sub> = 0 Volt
V <sub>OH</sub>	Output High Voltage	2.4		Volt	I <sub>OH</sub> = - 100 uamp
V <sub>OL</sub>	Output Low Voltage		.4	Volt	I <sub>OL</sub> = 1.6 mamp
C <sub>IN</sub>	Input Capacitance		20	pf	V <sub>IN</sub> = V <sub>SS</sub>
C <sub>OUT</sub>	Output Capacitance		10	pf	V <sub>OUT</sub> = V <sub>SS</sub>
I <sub>SS</sub>	V <sub>SS</sub> Supply Current		30	mamp	SWE = RDE = V <sub>IL</sub>
I <sub>GG</sub>	V <sub>GG</sub> Supply Current		40	mamp	ITTL Load

**AC (DYNAMIC) CHARACTERISTICS**       $T_A = 0^\circ\text{C} - +70^\circ\text{C}$ ;  $V_{SS} = +5 \text{ Volt} \pm 5\%$ ;  $V_{GG} = -12 \text{ Volt} \pm 5\%$

Symbol	Parameter	Min	Max	Unit	Condition
TCP, RCP	Clock Frequency	DC	200	KHz	
<b>Input Pulse Widths</b>					
PWTCP	Transmit Clock	2.5		usec	C <sub>L</sub> = 20pf 1 TTL Load
PWRCP	Receive Clock	2.5		usec	
PWCS	Control Strobe	250		nsec	
PWTDS	Transmit Data Strobe	250		nsec	
PWRST	RESET	1.0		μsec	
PWSWE	Status Word Enable	500		nsec	
PWRDA	Reset Data Available	500		nsec	
PWRDE	Receive Data Enable	250		nsec	
<b>Switching Characteristics</b>					
t <sub>CDS</sub>	Control Set Up Time	0		nsec	Figure 1
t <sub>CDH</sub>	Control Hold Time	20		nsec	Figure 1
t <sub>OE</sub>	Output Enable Time		500	nsec	
t <sub>OD</sub>	Output Disable Time		500	nsec	



## TIMING WAVEFORMS (Figure 1)



## PIN DEFINITIONS

Pin	Label	Function
(1)	VSS	+5 Volt $\pm$ 5%
(2)	VGG	-12 Volt $\pm$ 5%
(3)	VDD	Ground
(21)	RESET	The transmitter status outputs TBMT and TEOC are set to VOH indicating the input transmitter buffer register is empty. The TSO output generates VOH or MARK until a valid data character has been loaded into the transmitter and valid data transmission begins. The receiver status output ODA, is reset to the VOL state.

(38)	NDB1	Number Data Bits/Character
(37)	NDB2	Number Data Bits/Character
(36)	NSB	Number Stop Bits

The bit length of each data character and the number of stop bits added to each transmitted character are defined by these three inputs.

The character word length does not include the parity bit and is common to both the transmitter and receiver if operating in the full duplex mode.

NSB	NDB2	NDB1	BITS/CHARACTER	STOP BITS
VIL	VIL	VIL	5	1
VIL	VIL	VIH	6	1
VIL	VIH	VIH	7	1
VIL	VIH	VIH	8	1
VIH	VIL	VIL	5	1.5
VIH	VIL	VIH	6	2
VIH	VIH	VIL	7	2
VIH	VIH	VIH	8	2

(35) NPB NO PARITY BIT. A VIH eliminates the PARITY bit from being transmitted causing the STOP bit(s) to immediately follow the last data bit. The receiver assumes the bit(s) following the last data bit to be STOP bits. The RPE output is also forced to a VOL condition.

(39) POE PARITY ODD/EVEN. If the NPB input is VIL, the parity mode is ODD if POE is VIL and EVEN if POE is VIH. The parity mode is the same for both the transmitter and receiver.

(34) CS CONTROL STROBE. A VIH loads POE, NDB1, NDB2, NPB, NSB into the CONTROL HOLDING REGISTER.

To load the control inputs for static operation CS can be hard-wired to VIH.

(26)	DB1	TRANSMITTER DATA BITS. Input data on DB1-DB8 are strobed into the DATA INPUT HOLDING REGISTER by TDS.
(27)	DB2	
(28)	DB3	Input data is assumed right justified so DB1 is always the least significant bit and is the bit
(29)	DB4	
(30)	DB5	

Pin	Label	Function
(31)	DB6	transmitted following the START bit. For data words less than eight bits, the unused bits are don't care inputs.
(32)	DB7	
(33)	DB8	
(23)	$\overline{TDS}$	TRANSMITTER DATA STROBE. A $V_{IL}$ enters data on the DB1-DB8 inputs into the INPUT HOLDING REGISTER. If the transmitter is in the idle state with both TBMT and TEOC at $V_{OH}$ , the START bit will be generated on the first negative transition of the input clock TCP following the return of $\overline{TDS}$ to a $V_{IH}$ state.
(25)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on DB1-DB8 are serially transmitted on TSO. A START (SPACE) bit precedes each character. A PARITY bit, if selected, and the correct number of STOP bits follow the last valid data bit. The TSO output is $V_{OH}$ (MARK) when a valid character is not being transmitted.
(22)	TBMT	TRANSMITTER BUFFER EMPTY. A $V_{OH}$ indicates the character in the INPUT HOLDING REGISTER has been transferred into the transmitter and a new character may be loaded into the INPUT HOLDING REGISTER. One complete character time (START BIT, DATA BITS, PARITY BIT, AND STOP BIT(S)) is available to load the next character. If a $\overline{TDS}$ is not generated within the time allotted, the TSO output will go into an idle state of $V_{OH}$ or a MARK condition. TBMT will remain in the tri state mode unless $SWE$ is a $U_{ZL}$ .
(24)	TEOC	TRANSMITTER END OF CHARACTER. A $V_{OL}$ to $V_{OH}$ transition indicates the transmission of the character and stop bits have been completed. The $V_{OH}$ is maintained until the leading edge of the next START bit (MARK to SPACE transition) is generated.
(40)	TCP	TRANSMITTER CLOCK PULSE. The transmitter input clock must be 16 times faster than the desired baud rate at TSO.
(17)	RCP	RECEIVER CLOCK PULSE. The receiver input clock must be 16 times the baud rate of data received on RSI.
(20)	RSI	RECEIVER SERIAL INPUT. Serial input data is received on RSI at a baud rate 1/16th the rate of RCP. The $V_{IH}$ to $V_{IL}$ (MARK to SPACE) transition beginning each START bit synchronizes the receiver to the incoming data. Data is assumed to be received least significant bit first.
(12)	RD1	RECEIVER DATA. Data outputs from the DATA OUTPUT HOLDING REGISTER are active only when $RDE$ is a $V_{IL}$ . The eight data outputs are in a tri-state mode if $RDE$ is a $V_{IH}$ . Data is presented at the outputs right justified with RD1 the least significant bit. For data word lengths less than 8 bits the unused bits will appear as $V_{OL}$ .
(11)	RD2	
(10)	RD3	
(9)	RD4	
(8)	RD5	
(7)	RD6	
(6)	RD7	
(5)	RD8	
(4)	$\overline{RDE}$	RECEIVER DATA ENABLE. A $V_{IL}$ enables data in the DATA OUTPUT HOLDING REGISTER to the RECEIVER DATA output pins. For an output configuration not requiring a tri-state condition for RD1-RD8 the RDE input can be tied directly to ground enabling the data outputs at all times.
(19)	ODA	OUTPUT DATA AVAILABLE. A $V_{OH}$ indicates a complete character has been received and transferred to the DATA OUTPUT HOLDING REGISTER. The ODA output will be in the tri-state mode unless $SWE$ is a $V_{IL}$ . For contiguous data inputs on RSI data will remain in the holding register one character time before being lost.
(18)	$\overline{RDA}$	RESET DATA AVAILABLE. A $V_{IL}$ resets the ODA to a $V_{OL}$ . If ODA is not reset by $\overline{RDA}$ the ROR will be set when the next complete character is received and transferred to the DATA OUTPUT HOLDING REGISTER.
(15)	ROR	RECEIVER OVERRUN. A $V_{OH}$ indicates a second character has been received and transferred to the DATA OUTPUT HOLDING REGISTER without an intervening RDA. If the previously received character has not been unloaded from the register the next character will be loaded and the first character lost. ROR will remain in the tri-state mode unless $SWE$ is a $V_{IL}$ .
(14)	RFE	RECEIVER FRAMING ERROR. A $V_{OH}$ indicates a correct STOP bit was not received following the START bit and correct number of data bits. RFE will remain in the tri-state mode unless $SWE$ is a $V_{IL}$ .

Pin	Label	Function
(13)	RPE	RECEIVER PARITY ERROR. A $V_{OH}$ indicates the accumulated parity on the received character does not compare with the parity mode set by POE. RPE will remain in the tri-state mode unless $\overline{SWE}$ is a $V_{IL}$ .
(16)	$\overline{SWE}$	STATUS WORD ENABLE. A $V_{IL}$ enables the status outputs ODA, ROR, RFE, RPE and TBMT on the respective output lines. When $\overline{SWE}$ is $V_{IH}$ all status outputs are in the tri-state mode.  For output configurations not requiring a tri-state condition for the status outputs, $\overline{SWE}$ may be tied directly to ground.

### APPLICATION DATA

Asynchronous data communications is typified by low data rates, non-contiguous data messages, and a MARK condition on the line between characters. As a result, each data character must be framed for recognition by START and STOP bits. The S1883 UART provides all the logic required to provide a complete full-duplex (transmit and receive simultaneously) asynchronous communication channel for baud rates up to 9600 bps. Included in the S1883 capabilities are; automatic START and STOP bit generation and detection; PARITY generation and detection on variable length characters; tri-state outputs for data and status for data bus configurations, double buffering for less critical timing, and a receiver allowing acceptance of data with up to 42% distortion.

### RECEIVER OPERATION

Asynchronous communication line discipline dictates that each character, regardless of width, must be preceded by a START bit. The receiver input logic detects the  $V_{IH}$  to  $V_{IL}$  (MARK to SPACE) transition on the RSI line that is the leading edge of the START bit. For one half bit time after the leading edge, RSI is sampled for a  $V_{IL}$  to insure a proper START bit was present. The following data bits are then clocked into the receiver in the center of each bit period. If RSI returns to the  $V_{IH}$  condition before the mid-point of the START bit, the receiver returns to a search for a MARK to SPACE transition.

If at the time of transfer ODA has not been reset by a  $\overline{RDA}$ , indicating the previous character has not been read, the ROR error flag is set to  $V_{OH}$ . The previous data character and status will be lost as the new character is loaded. One full character time is available, assuming contiguous data input at RSI, after ODA is set to read the output character. The data is available at the outputs RD1-RD8 right justified with RD1 the least

significant bit. For character widths less than 8 bits the unused outputs are forced to  $V_{OL}$ .

For data bus configurations the output data and status are tri-state lines enabled by  $\overline{RDE}$  and  $\overline{SWE}$  respectively. For polled systems  $\overline{SWE}$  can be strobed for detection of ODA and error conditions prior to reading data. For interrupt driven systems  $\overline{SWE}$  can be tied directly to ground and ODA used as a data ready interrupt input. A minimum of one character time is available to test the remaining error status bits and input the data character. Typically the same signal can be used for  $\overline{RDE}$  and  $\overline{RDA}$ .

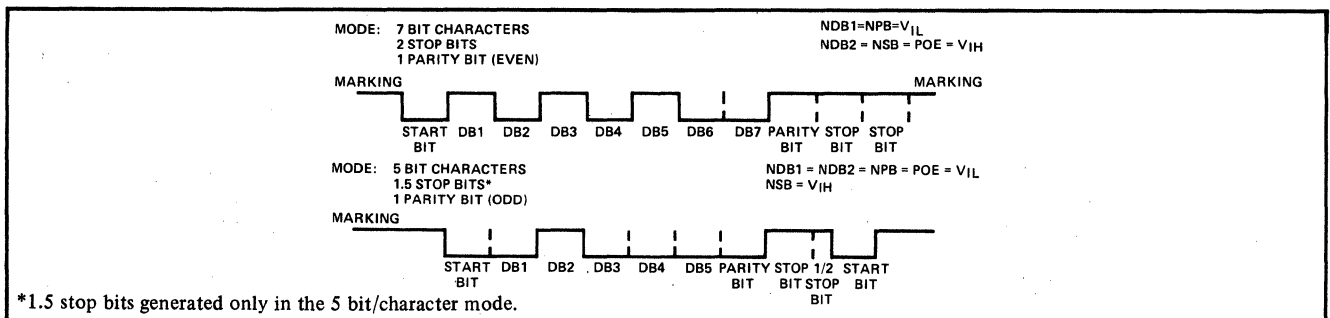
### TRANSMITTER OPERATION

The transmit section of the S1883 is reset to a MARK condition with  $V_{OH}$  on TSO after receiving a pulse on RESET. Additionally, the transmitter is reset to a character request mode with TBMT and TEOC both at  $V_{OH}$ . If the character format is not static, the word length NDB1 and NDB2, parity mode NPB and POE, and number of stop bits NSB should be strobed into the UART with CS.

If both the DATA INPUT HOLDING REGISTER and the TRANSMITTER SHIFT REGISTER are empty the transmitter is in the idle state with TSO, TBMT and TEOC all at  $V_{OH}$ . The START bit for a data character loaded with a  $\overline{TDS}$  pulse during the idle state is generated at the first negative transition of the TCP following the trailing edge of  $\overline{TDS}$ . TBMT goes to  $V_{OL}$  with the first  $\overline{TDS}$ . As soon as the character is transferred from the INPUT HOLDING REGISTER to the SHIFT REGISTER, TBMT returns to a  $V_{OH}$  and a second character can be loaded. Each character is transmitted with a START bit and 1, 1.5 or 2 stop bits controlled by the respective inputs.

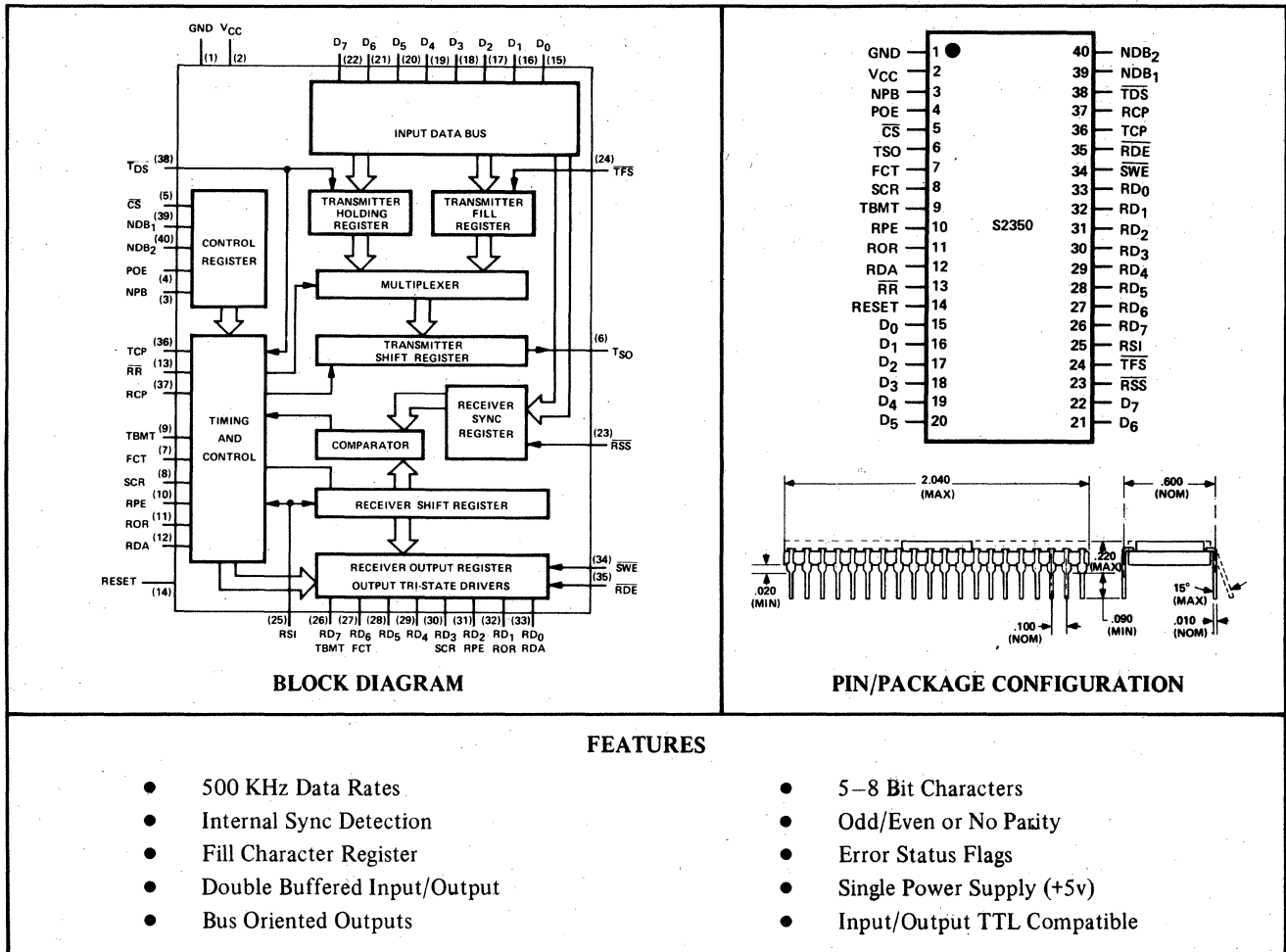
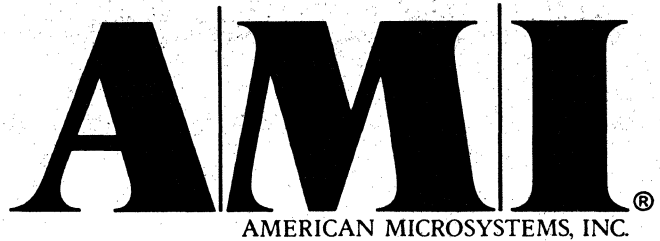
The TEOC is set to  $V_{OH}$  after the generation of the last STOP bit indicating the complete character has been transmitted.

### TYPICAL DATA FORMAT



# S2350

UNIVERSAL SYNCHRONOUS  
RECEIVER/TRANSMITTER (USRT)



## FUNCTIONAL DESCRIPTION

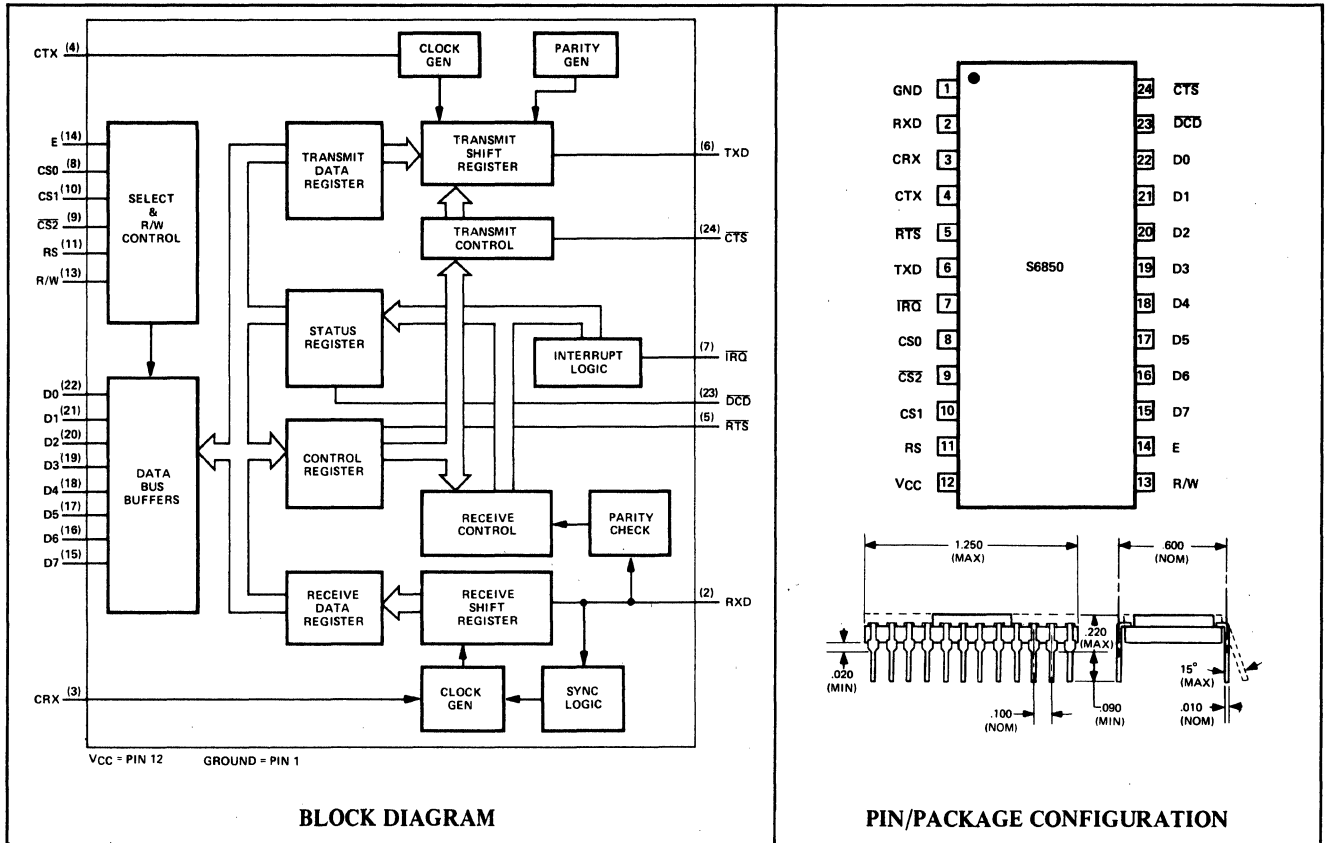
The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous for-

matting a 5, 6, 7, or 8 bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8 bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character in the transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.



### FEATURES

- 8 Bit Bidirectional Data Bus for Communication with MPU.
- False start bit deletion.
- Peripheral/modem control functions.
- Double buffered Receiver and Transmitter
- One or two stop bit operation.
- Eight and nine-bit transmission with optional even and odd parity.
- Parity, overrun and framing error checking.
- Programmable control register.
- Optional ÷1, ÷16, and ÷64 clock modes.
- Up to 500,000 bps transmission.

### FUNCTIONAL DESCRIPTION

The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight bit

bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

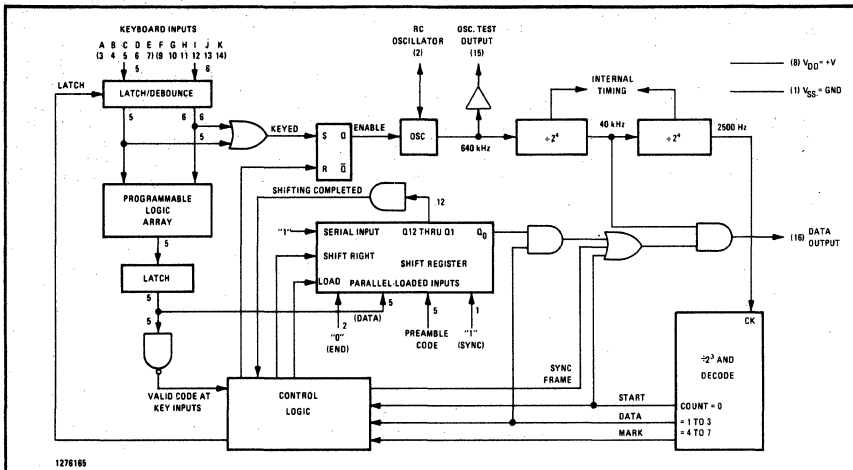
# S2600/S2601

REMOTE-CONTROL  
2-CHIP SET

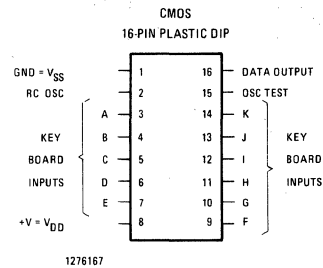
# AMI

AMERICAN MICROSYSTEMS, INC.®

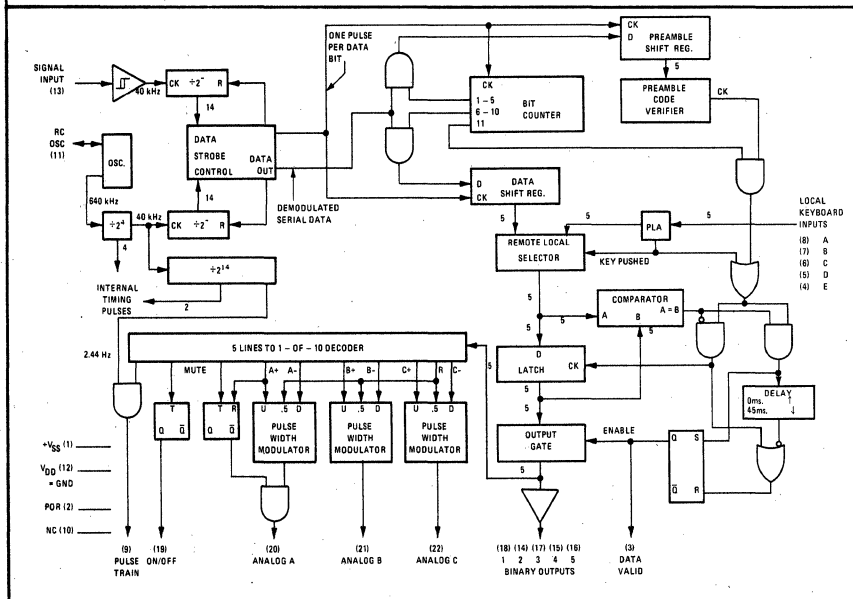
## ADVANCED PRODUCT DESCRIPTION



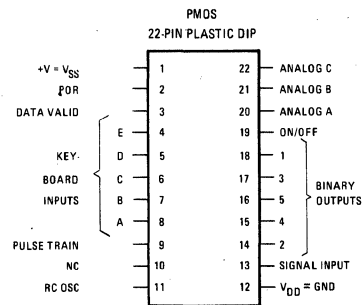
S2600 TRANSMITTER - BLOCK DIAGRAM



S2600 PIN CONNECTIONS



S2601 RECEIVER - BLOCK DIAGRAM



S2601 PIN CONNECTIONS

## FEATURES

- Small Parts Count - No Crystals Required
- Easily Used in LED or Ultrasonic Schemes
- Very Low Reception Error
- Low Power Drain by CMOS Transmitter
- 31 Commands - 5-bit Output Bus
- 3 Analog (LP Filterable PWM) Outputs
- Muting (Analog Output Kill/Restore)
- Indexing Output - 2½ Hz Pulse Train
- Toggle Output (On/Off)
- Mask Programmable Codes

## FUNCTIONAL DESCRIPTION

The S2600/S2601 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, etc.

The use of a synchronizing marker technique has eliminated the need for highly accurate frequencies generated by crystals. The S2600 Transmitter generates a 40 kHz carrier which it pulse-code-modulates with a message of 12 bits, each bit preceded by a synchronizing marker pulse.

Only bits 7 thru 11 contain command data; bits 1 and 12 denote sync and end-of-message, respectively; and bits 2 thru 6 constitute a fixed preamble which must be received correctly, or else the command bits are ignored. The S2601 Receiver produces an output only after two complete, consecutive, identical, 12-bit transmissions. Marker pulses, preamble bits, and redundant transmissions, have given the S2600/S2601 system a very high immunity to noise, without a large number of discrete components.

### S2600 Transmitter

The S2600 is a CMOS device with an on-chip oscillator, 11 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator requires only an external resistor and capacitor, and to conserve power, runs only during transmission. Keyboard inputs are active-low, and have internal pull-up resistors to  $V_{DD}$ . When one keyboard input from the group A thru E is activated with one from the group F thru K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2600/S2601 CODING," below. This code is loaded into the 13-bit shift register in parallel with the sync, preamble, and end bits.

The transmitter output is a 40 kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds

of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

### S2601 Receiver

The S2601 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40 kHz signal input, and 11 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to  $V_{SS}$ ; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2601, overriding any 40 kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40 kHz signal from the local RC oscillator timing chain. A 40 kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to  $\pm 24\%$  with respect to the receiver oscillator frequency.

Decoded data bits from the next five bit frames following the initial synchronizing frame are compared with the fixed preamble code. The next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, and if the preamble bits are correct, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next 12-bit transmission. In the case where 2 identical, proper, 12-bit transmissions are immediately followed either by transmissions with erroneous preamble codes or by nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to  $V_{DD}$ . The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

The S2601 has five other outputs: Pulse Train, On/Off, Analog A, Analog B, and Analog C. The states of these outputs

**S2601 Receiver (Continued)**

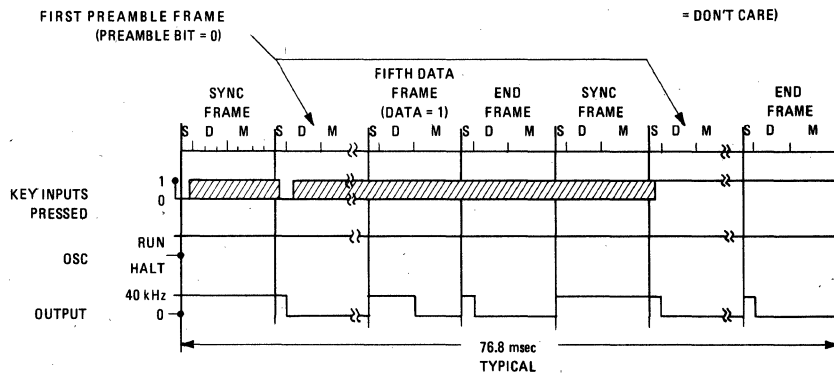
are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated. The Pulse Train output provides a 2.44 Hz square wave (50% duty factor) whenever 11011 appears at the Binary Outputs, but otherwise it remains at a logic "0". This pulse train can be used for indexing, e.g., for stepping a TV channel selector.

The On/Off ("mains") output changes state each time 01111 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

Analog Outputs A, B, and C are 10 kHz pulse trains whose duty factors are independently controllable. With a simple low-pass filter each of these outputs can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. Each Analog Output increases its duty factor in response to a particular Binary

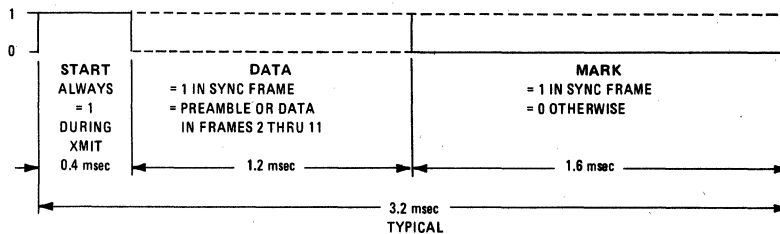
Output code and decreases its duty factor in response to another code — 6 codes in all. The entire range of 0% to 100% duty factor can be traversed in 6.6 seconds. All three Analog Outputs are set to 50% duty factor whenever 01011 appears at the Binary Outputs. Analog A is mutable; 01100 sets it to 0% duty factor. If 01100 then disappears and reappears, the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2601 has an on-chip power-on reset (POR) circuit which sets the Pulse Train and On/Off Outputs to "0," sets the Analog Outputs at 50% duty factor, and insures that Analog A is muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V<sub>SS</sub>; pulling it low causes a reset.



1276169

**MESSAGE FORMAT**



1276170

**MESSAGE FRAME FORMAT**



## S2600/S2601 CODING

TRANSMITTER KEYBOARD INPUT PINS TIED TO VSS	RECEIVER KEYBOARD INPUT PINS TIED TO VDD (See Note 1)	RESULTING RECEIVER BINARY OUTPUTS					RECEIVER DEDICATED FUNCTIONS
		1	2	3	4	5	
AB	—	0	0	0	0	0	
EK	—	0	0	0	0	1	
EJ	—	0	0	0	1	0	
EI	—	0	0	0	1	1	
EH	BC	0	0	1	0	0	Increase Analog C pulse width
EG	—	0	0	1	0	1	
EF	—	0	0	1	1	0	
DK	AE	0	0	1	1	1	Decrease Analog B pulse width
DJ	—	0	1	0	0	0	
DI	—	0	1	0	0	1	
DH	—	0	1	0	1	0	
DG	DE	0	1	0	1	1	RESET Analog (see Note 2)
DF	CE	0	1	1	0	0	MUTE (see Note 3)
CK	—	0	1	1	0	1	
CJ	—	0	1	1	1	0	
CI	CD	0	1	1	1	1	Toggle On/Off Output
CH	—	1	0	0	0	0	
CG	—	1	0	0	0	1	
CF	—	1	0	0	1	0	
BK	AD	1	0	0	1	1	Increase Analog B pulse width
BJ	BD	1	0	1	0	0	Decrease Analog C pulse width
BI	—	1	0	1	0	1	
BH	—	1	0	1	1	0	
BG	AB	1	0	1	1	1	Increase Analog A pulse width
BF	—	1	1	0	0	0	
AK	—	1	1	0	0	1	
AJ	—	1	1	0	1	0	
AI	BE	1	1	0	1	1	Activate Pulse Train Output
AH	—	1	1	1	0	0	
AG	—	1	1	1	0	1	
AF	AC	1	1	1	1	0	Decrease Analog A pulse width
—	—	1	1	1	1	1	Rest State

- Notes:
- Receiver keyboard inputs override any ultrasonic input.
  - Sets Analog A, B, and C waveforms to 50% Duty Factor.
  - First operation sets Analog A to 0% Duty Factor; second operation restores former Analog A Duty Factor.

## ELECTRICAL SPECIFICATIONS – S2600 TRANSMITTER

All voltages measured with respect to VSS.

### ABSOLUTE MAXIMUM RATINGS

Operating ambient temperature $T_A$	0 to +70°C	Positive voltage on any pin	+12V
Storage temperature	-65°C to +150°C	Negative voltage on any pin	-0.3V

### ELECTRICAL CHARACTERISTICS

Unless otherwise noted,  $V_{DD} = 8.5 \pm 1.5V$  and  $T_A = 0$  to +70°C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$f_0$	Oscillator frequency		640		kHz	ROSC = 12K, COSC = 100 pF
$\Delta f_0/f_0$	Frequency deviation	-10		+10	%	Fixed ROSC, COSC, VDD
$I_{DD}$	Supply current			2	mA	During transmission Data Output = 1 mA
$V_{IH}$	Input "1" threshold	25	50		%VDD	
$V_{IL}$	Input "0" threshold		50	75	%VDD	
$I_{IL}$	Input source current	50		200	$\mu A$	@ $V_I = 0V$
$I_{OH}$	Output source current	1	1.5		mA	@ $V_O = V_{DD} - 3V$
$I_{OL}$	Output sink current	-2	-5		mA	@ $V_O = +0.5V$

**ELECTRICAL SPECIFICATIONS – S2601 RECEIVER**

All voltages measured with respect to VDD.

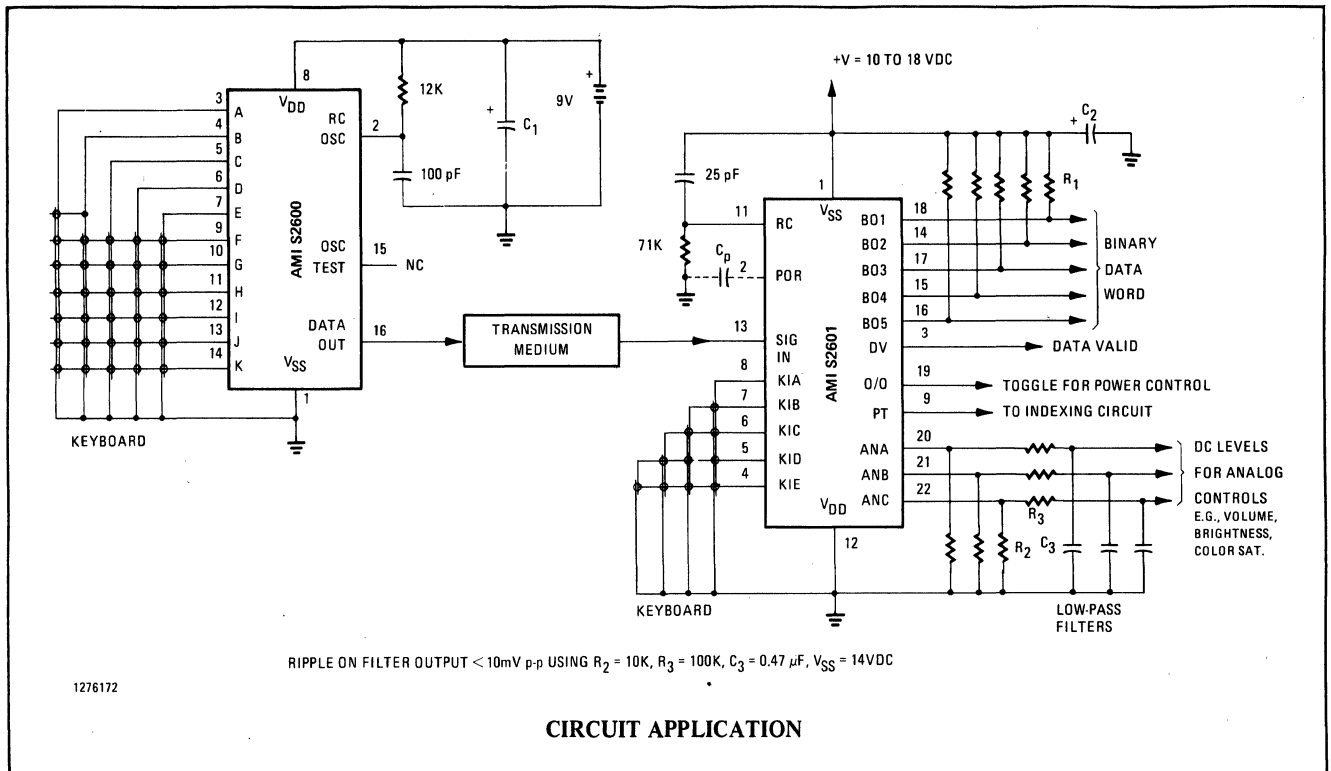
**ABSOLUTE MAXIMUM RATINGS**

Operating ambient temperature $T_A$	0 to +70°C	Positive voltage on any pin	$V_{SS} + 0.3V$
Storage temperature	-65°C to +150°C	Negative voltage on any pin	$V_{SS} - 22V$
$V_{SS}$ power supply voltage	+22V		

**ELECTRICAL CHARACTERISTICS**

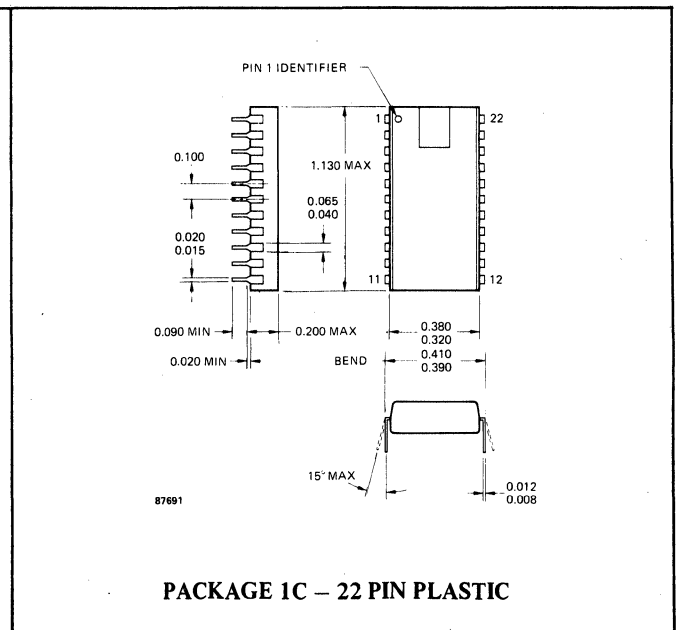
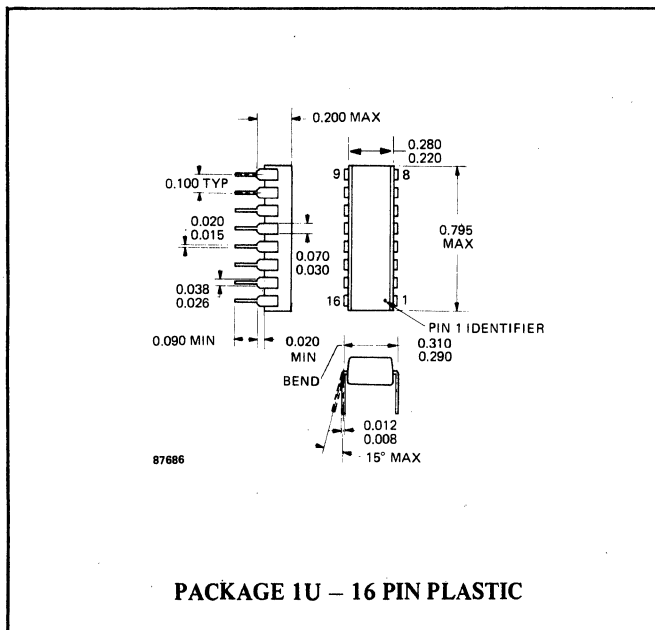
Unless otherwise noted,  $V_{SS} = 14 \pm 4V$  and  $T_A = 0$  to +70°C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$f_0$	Oscillator frequency		640		kHz	ROSC = 71K, COSC = 25 pF Fixed ROSC, COSC, $V_{SS}$ No loads
$\Delta f_0/f_0$	Frequency deviation	-10		+10	%	
$I_{SS}$	Supply current		14	20	mA	
Signal Input:						
$V_{IH}$	"1" threshold		70	85	% $V_{SS}$	
$V_{IL}$	"0" threshold	30	45		% $V_{SS}$	
$V_{IH} - V_{IL}$	Voltage hysteresis	10		55	% $V_{SS}$	
Keyboard and POR Inputs:						
$V_{IH}$	"1" voltage	.5	1.3		V	@ $V_I = V_{SS} - 10V$
$V_{IL}$	"0" voltage		1.3	5.5	V	
$I_{IL}$	Source current	50		500	$\mu A$	
	Debounce delay (Keyboard inputs only)	1.45		2.2	msec	
Binary Outputs (open source):						
$I_{OL}$	Sink current	-.5	-.75		mA	@ $V_0 = V_{SS} - 7V$
	Duration	34.9			msec	$f_0 = \text{Min}$
Analog Outputs (open drain):						
$I_{OH}$	Source current	1	1.2		mA	@ $V_0 = V_{SS} - 1V$
Data Valid, Pulse Train, and On/Off Outputs:						
$I_{OH}$	Source current	1	1.5		mA	@ $V_0 = V_{SS} - 2V$
$I_{OL}$	Sink current	-40	-50		$\mu A$	@ $V_0 = .7V$
$t_r$	Risetime (.1 $V_{SS}$ to .9 $V_{SS}$ )			5	$\mu sec$	$R_L = \infty$ ; $C_L < 50$ pF
$t_f$	Falltime (.9 $V_{SS}$ to .1 $V_{SS}$ )			5	$\mu sec$	$R_L = \infty$ ; $C_L < 50$ pF



### S2600 TRANSMITTER

### S2601 RECEIVER



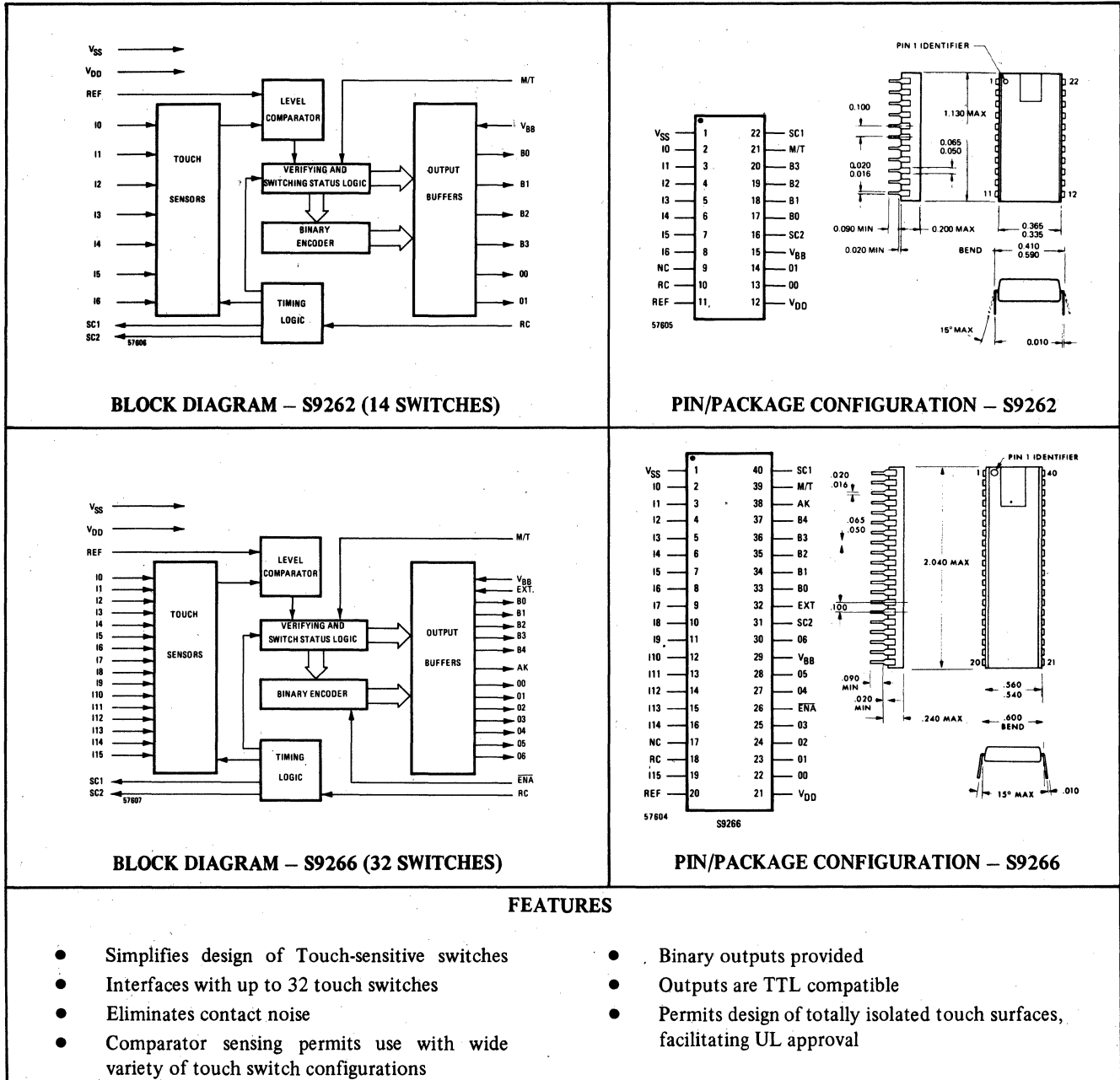
# S9262/S9266

MULTIPLEXED  
TOUCHCONTROL INTERFACE

# AMI

AMERICAN MICROSYSTEMS, INC.

## ADVANCED PRODUCT DESCRIPTION



### FUNCTIONAL DESCRIPTION

Fabricated with P-channel ion implanted MOS/LSI technology, AMI TouchControl integrated circuits\* are designed to interface with a variety of touch panel switches and provide a high degree of flexibility in the selection of touch panel materials, layout of touch pad configurations, and design of switching functions. These parts are designed to address an array of TouchControl switches in either a 2 x 7 matrix (S9262) or a 2 x 16 matrix (S9266) to interface with a total of

either 14 or 32 switches. The outputs are binary encoded for easy interfacing with microprocessors or TTL, CMOS or MOS logic.

Both momentary and "push on – push off" (toggle) switching operations are available on AMI TouchControl circuits and are electrically selected by the logic level of the M/T input pin. To ensure reliable switch action, a built in delay is incorporated in all circuits requiring a minimum touch time for switch response.

## ABSOLUTE MAXIMUM RATINGS

Voltage on any pin except EXT relative to $V_{SS}$ :	+ 0.3V to - 20V	Operating temperature range:	0°C to + 50°C
Voltage on EXT pin relative to $V_{SS}$ :	+ 0.3V to - 27V	Storage temperature (Ambient)	- 65°C to + 150°C

\*For non-multiplexed TouchControl circuits see AMI S9260, S9261, S9263, S9264, S9265

## ELECTRICAL CHARACTERISTICS

(0°C ≤  $T_A$  ≤ 50°C;  $V_{SS} = 0V$ ;  $V_{DD} = -13.5V$  to  $-18.0V$  unless otherwise specified.)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
$V_{IL}$	Input logic 0 level – all except “I” inputs.	+ 0.3	0	- 1.5	Volts	Note: M/T and ENA inputs are internally pulled up to $V_{SS}$ .
$V_{IH}$	Input logic 1 level – all except “I” inputs.	- 10.0	- 12.0	- 18.0	Volts	
$f_{RC}$	Internal oscillator frequency measured at RC input.	50		100	kHz	Frequency measured at RC Input = 50 kHz.
$T_S$ $T_{RST}$	Switch delay time Time to reset all latches using M/T input.	50	100	200	msec msec	
$V_{OL}$ $V_{OH}$	Output low voltage. Output high voltage	$V_{SS}$		- 1.0 $V_{DD}$	Volts	$V_{BB} = V_{SS}$ ; 10K resistive load to $V_{DD}$ .
$V_{OL}$ $V_{OH}$	Output low voltage. Output high voltage	$V_{SS}$ $V_{BB} + 0.4$		$V_{SS} - 0.5$ $V_{BB}$	Volts	
SC1, SC2	Scan clock output. Output low voltage Output high voltage.	$V_{SS}$		- 1.5 $V_{DD}$		Max. capacitive loading ≤ 150 pF.

## OPERATION

Device operation can be understood by referring to Figure 1, depicting a typical application of the S9266. Each of the 32 pairs of series capacitors labeled S1 – S32 is one touch switch located on a TouchControl panel constructed of glass, printed circuit board, epoxy, or other dielectric material. (For details on touch panel configuration and operation, see the TouchControl application note included in this APD.) In each capacitor pair, the two common plates represent the conductive area on the control panel surface that is to be touched. The other two plates are formed by two conductive surfaces parallel to the touched surface and located directly under it on the reverse side of the panel. Referring again to Figure 1, the S9266 generates a clock signal on output SC1 and a similar signal on output SC2. The SC1 clock output is connected to the common conductors of 16 of the 32 touch switches; the SC2 clock connects to the remaining 16 switches. For each touch switch the clock signal passes through the two series capacitors and is detected in the MOS circuit. When a panel switch surface is touched, the signal level into the chip diminishes, and the on-chip differential amplifier senses the change and performs the appropriate switching function.

## I INPUTS

Inputs from the touch switch pads to the TouchControl circuit are labeled I0 through I15 (S9266), or I0 through I16 (S9262). The I inputs in conjunction with SC1 and SC2 outputs form a touch switch matrix of 2 x 16 or 2 x 7, respectively. In both these parts the outputs are binary coded and will be described later.

## RC INPUT

A resistor connected to  $V_{DD}$  and a capacitor connected to  $V_{SS}$  are connected to the RC input pin to establish the on-chip clock frequency that controls the rate of multiplexing and the touch switch delay time. Nominal values for these components are suggested in Figure 1, but they may be varied to change clock frequency over a range of 50kHz to 100 kHz.

## REF INPUT

In order to allow flexibility in the choice of TouchControl panel materials, switch layout, and switch size, AMI TouchControl inputs have been designed to detect a differential change rather than an absolute change in level. To obtain a reference level, two resistors are connected to input REF, one connected to input REF, one connected to  $V_{SS}$  and the other to  $V_{DD}$ .

**V<sub>BB</sub> SUPPLY**

The sources of all output devices (both "O" and "B" outputs) are common and connected to pin V<sub>BB</sub>. This allows TTL compatibility as shown in Figure 1, as well as the ability to drive higher level signals. For instance, if V<sub>SS</sub> = 0 volts, V<sub>DD</sub> = -16 volts, and V<sub>BB</sub> = V<sub>SS</sub>, then active outputs would drive a load connected to V<sub>DD</sub> towards V<sub>SS</sub>.

**M/T INPUT**

The M/T input pin selects the mode of switch operation, either momentary or toggle. Applying V<sub>SS</sub> to the M/T pin selects momentary operation in which appropriate outputs are active only for the duration of touching a switch. In this mode, no output is active when no switch is touched. A V<sub>DD</sub> level applied to M/T causes the circuit to operate in the toggle mode for "push-on, push-off" operation. Subsequent activation of the switch will toggle the corresponding output on and off alternately. It should be noted that each input should be cleared to the off state before selecting a new input to obtain meaningful data from the binary outputs. To reset all outputs when the toggle mode is selected, a pulse of V<sub>SS</sub> level may be applied to the M/T input.

**SC1 and SC2 OUTPUTS**

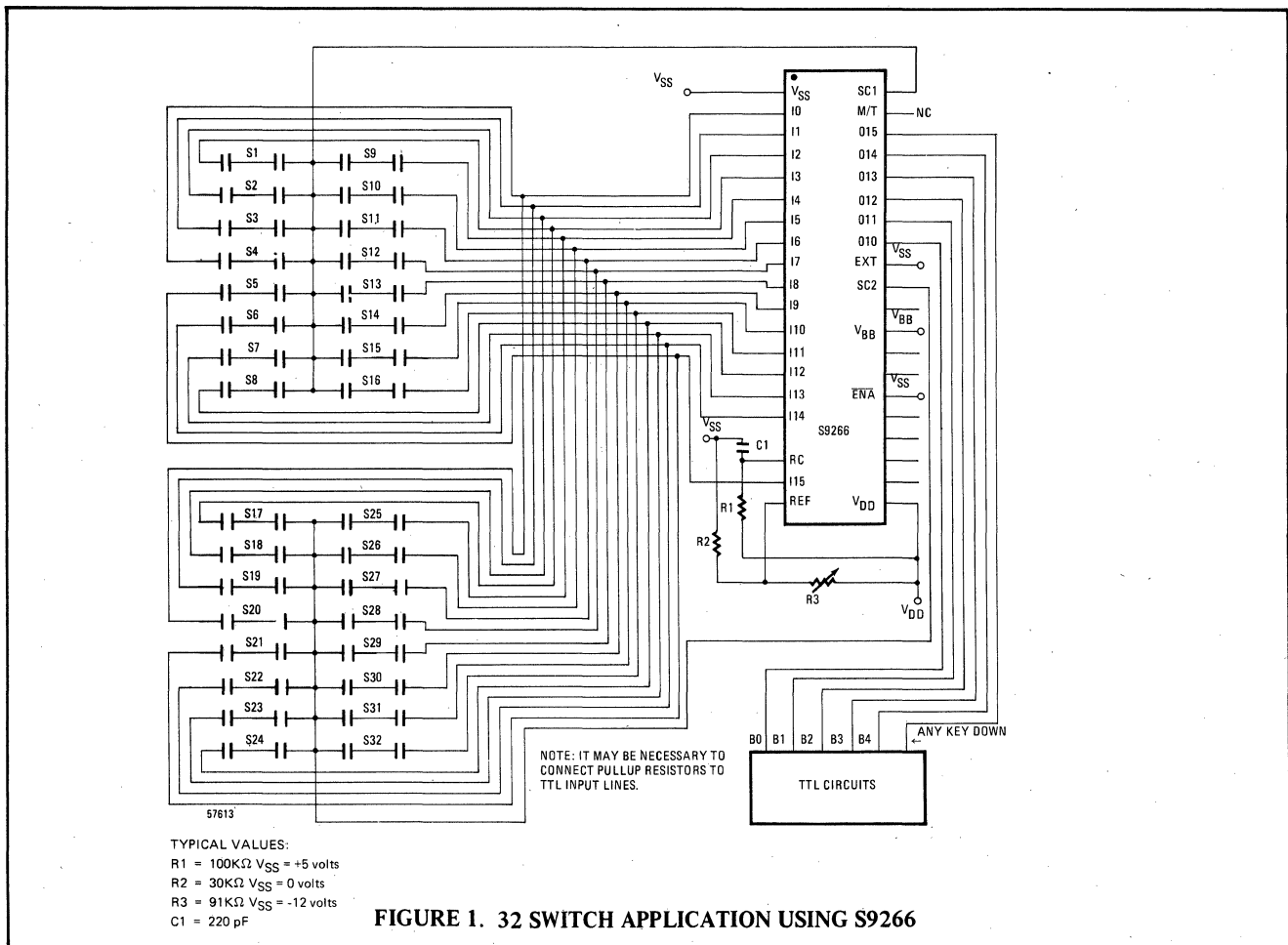
The S9262 and S9266 have multiplexed inputs, using 2 x 7 and 2 x 16 matrices, respectively, to provide 14 and 32 input states. Clock signals SC1 and SC2 are used along with the "I" inputs to form these matrices as connected in the schematic of Figure 1.

**O OUTPUTS**

Each output pin labeled "O" corresponds to an input pin labeled "I". Whenever an input is selected, the output becomes active and will drive an external load toward supply voltage V<sub>BB</sub>. This is true for momentary operation only; toggle operation is described in the section labeled "M/T input." When "O" outputs are not active, they are high impedance open drain.

**B AND AK OUTPUTS**

The S9262 has four and the S9266 has five outputs labeled "B." These supply a binary code relating to the state of the inputs. Fourteen unique states are available on S9262 and thirty-two on S9266. The output configuration is identical to the "O" outputs. An extra output labeled AK is available on the S9266 and is active whenever any key is selected.



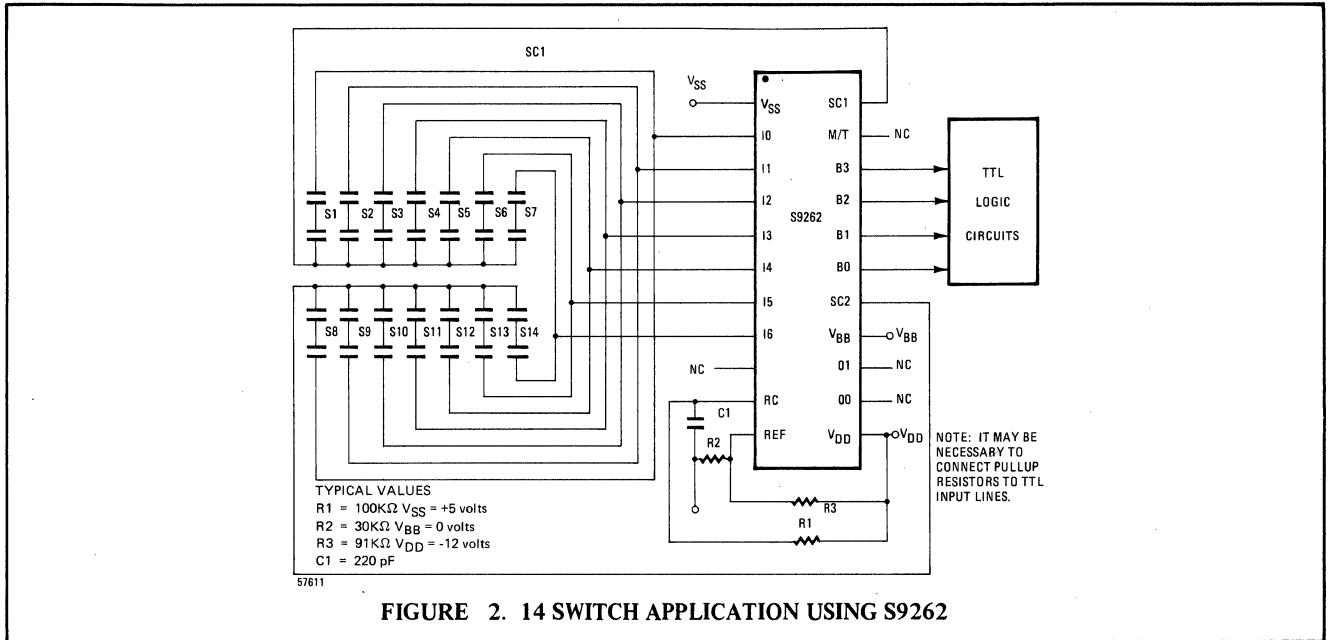


FIGURE 2. 14 SWITCH APPLICATION USING S9262

TABLE 1. OUTPUT ENCODING  
(V<sub>BB</sub> = 0 VOLTS)

SCAN OUTPUT	TOUCHED INPUT	"B" OUTPUTS				"O" OUTPUTS						AK OUTPUT			
		B0	B1	B2	B3	B4	O0	O1	O2	O3	O4		O5	O6	
SC1	10	0	0	0	0	0	1	0	0	0	0	0	0	0	1
SC1	11	1	0	0	0	0	0	1	0	0	0	0	0	0	1
SC1	12	0	1	0	0	0	0	0	1	0	0	0	0	0	1
SC1	13	1	1	0	0	0	0	0	0	1	0	0	0	0	1
SC1	14	0	0	1	0	0	0	0	0	0	1	0	0	0	1
SC1	15	1	0	1	0	0	0	0	0	0	1	0	0	0	1
SC1	16	0	1	1	0	0	0	0	0	0	0	0	1	0	1
SC1	17	1	1	1	0	0	0	0	0	0	0	0	0	0	1
SC1	18	0	0	0	1	0	0	0	0	0	0	0	0	0	1
SC1	19	1	0	0	1	0	0	0	0	0	0	0	0	0	1
SC1	110	1	0	1	0	0	0	0	0	0	0	0	0	0	1
SC1	111	1	1	0	1	0	0	0	0	0	0	0	0	0	1
SC1	112	0	0	1	1	0	0	0	0	0	0	0	0	0	1
SC1	113	1	0	1	1	0	0	0	0	0	0	0	0	0	1
SC1	114	0	1	1	1	0	0	0	0	0	0	0	0	0	1
SC1	115	1	1	1	1	0	0	0	0	0	0	0	0	0	1
SC2	10	0	0	0	0	1	0	0	0	0	0	0	0	0	1
SC2	11	1	0	0	0	1	0	0	0	0	0	0	0	0	1
SC2	12	0	1	0	0	1	0	0	0	0	0	0	0	0	1
SC2	13	1	1	0	0	1	0	0	0	0	0	0	0	0	1
SC2	14	0	0	1	0	1	0	0	0	0	0	0	0	0	1
SC2	15	1	0	1	0	1	0	0	0	0	0	0	0	0	1
SC2	16	0	1	1	0	1	0	0	0	0	0	0	0	0	1
SC2	17	1	1	1	0	1	0	0	0	0	0	0	0	0	1
SC2	18	0	0	1	1	1	0	0	0	0	0	0	0	0	1
SC2	19	1	0	0	1	1	0	0	0	0	0	0	0	0	1
SC2	110	0	1	0	1	1	0	0	0	0	0	0	0	0	1
SC2	111	1	1	0	1	1	0	0	0	0	0	0	0	0	1
SC2	112	0	0	1	1	1	0	0	0	0	0	0	0	0	1
SC2	113	1	0	1	1	1	0	0	0	0	0	0	0	0	1
SC2	114	0	1	1	1	1	0	0	0	0	0	0	0	0	1
SC2	115	1	1	1	1	1	0	0	0	0	0	0	0	0	1
-	None	1	1	1	1	1	0	0	0	0	0	0	0	0	0

### ENA INPUT

Available on the S9266, the ENA input allows the outputs to be bussed and may be gated off by application of a logic 1 level. V<sub>SS</sub> applied to the input enables all five outputs and AK.

### EXT

The EXT pin is available on the S9266 and is used to supply a higher clock voltage to the TouchControl panel whenever that may be necessitated by smaller touch switch size. When the higher clock voltage level for SC1 and SC2 is not required, this pin should be connected to V<sub>DD</sub>.

### TOUCHCONTROL APPLICATION NOTES

#### PANEL CONSTRUCTION

A TouchControl switch panel consists of a single sheet of a rigid material with conductive surfaces applied on both sides as shown in Figure 3.

A number of materials may be used for touch panels, the selection of the material most suited for a particular application being dependent on such things as durability, appearance, ease of assembly, cost, and dielectric constant of the material.

Regardless of the selected panel material, a touch switch is formed by applying a single conductive surface to its front surface with two other conductive surfaces applied directly in line on the reverse side of the panel. Figure 3 shows three views of a typical touch panel containing two TouchControl switches. On switch one, conductive surface A is applied to the front of the panel and is the surface to be applied to effect a switch closure. Surfaces B and C are applied directly in line with A on the opposite side of the panel. A should cover completely and may overlap surfaces B and C.

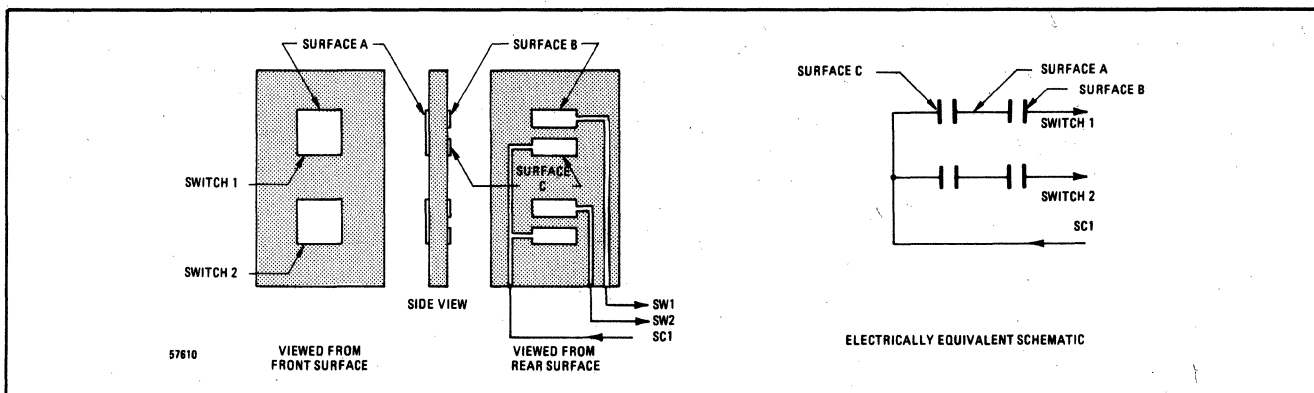


FIGURE 3. CONSTRUCTION OF A TWO SWITCH TOUCHCONTROL PANEL WITH EQUIVALENT ELECTRICAL CIRCUIT.

The application of the conductive surfaces depends on selection of the panel materials. If glass is used, for example, it is common to apply a coating of tin oxide, which is then fired on for durability; rear surface conductors may be screened on with a conductive ink. Touch panels may be made more simply from double-sided printed circuit boards in which the conductive TouchControl surfaces are created by standard etching. For breadboarding purposes, a number of conductive tapes and paints are available and may be applied to a variety of touch panel materials.

**ELECTRICAL OPERATION**

The three conductive surfaces in a TouchControl switch combine to form two capacitors connected in series, as shown in the schematic diagram of Figure 3. An AC signal generated in the MOS circuit is applied to the rear conductive surface labeled C. This signal is coupled through to surface A by the capacitor formed by C and A. The signal is then coupled to surface B by the capacitor formed by A and B and applied to one of the inputs of the MOS circuit, which detects the signal's presence. When surface A is touched, the amplitude of the signal is significantly decreased because of body capacitance. This is sensed by the MOS circuit, and the appropriate switching function is performed.

dielectric constant, A is area, and d is the material's thickness, it is apparent that minimum switch size is dependent on the thickness and dielectric constant of the panel material. If, for example, the panel is made from 1/8" thick glass with a dielectric constant of 8, then the minimum area of each of the two rear surface conductors is 0.5 sq. inches. Since the touch surface must cover the entire area of the two rear conductors, it must, then, be at least 1.0 sq. inch. It is desirable to separate the two rear-surface conductors by at least 0.125 inches, so the touch surface would be somewhat larger than 1.0 sq. inch. Higher capacitance, and thus smaller touch switches, can be obtained by using epoxy printed circuit material; though the dielectric constant is lower (around 5.0) the thickness can be decreased substantially.

**TOUCH SWITCH LAYOUT GUIDELINES**

AMI TouchControl circuits have been designed to interface with a variety of touch switch configurations. However, there are several guidelines that must be observed to insure a satisfactory TouchControl system.

The size of a TouchControl switch is dependent on the amount of capacitance needed to couple the clock signal to the "I" inputs of the MOS circuits. Because the input capacitance associated with the circuit input is typically five picofarads, it is advisable that each of the two series capacitors formed by the three conductive TouchControl panel surfaces be no less than seven picofarads. Since the capacitance in picofarads can be calculated by  $C = 0.22\epsilon A / d$ , where  $\epsilon$  is the

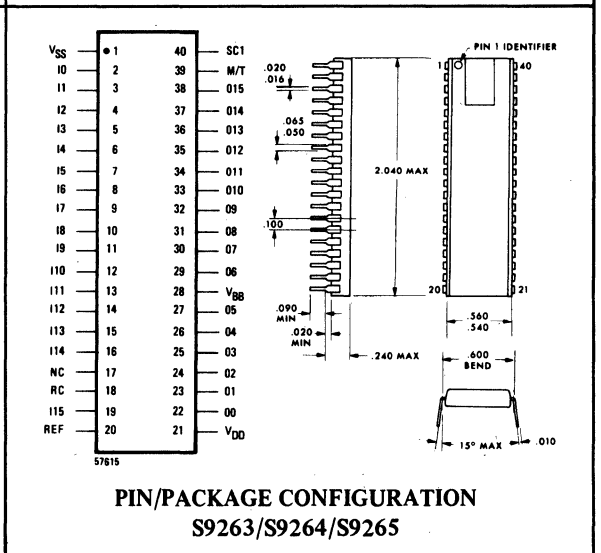
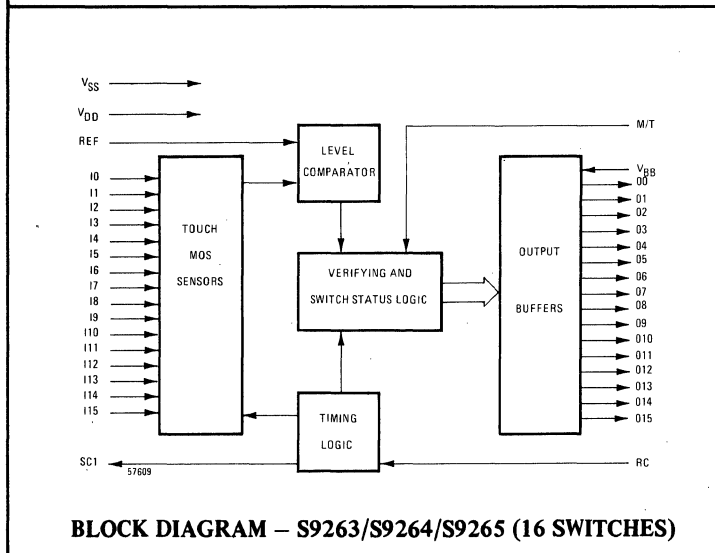
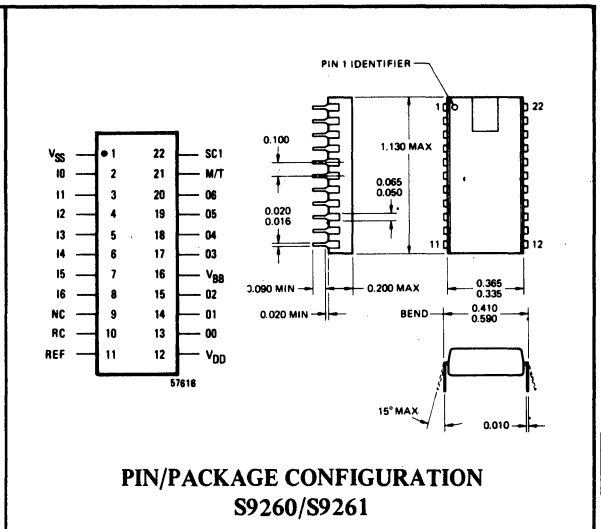
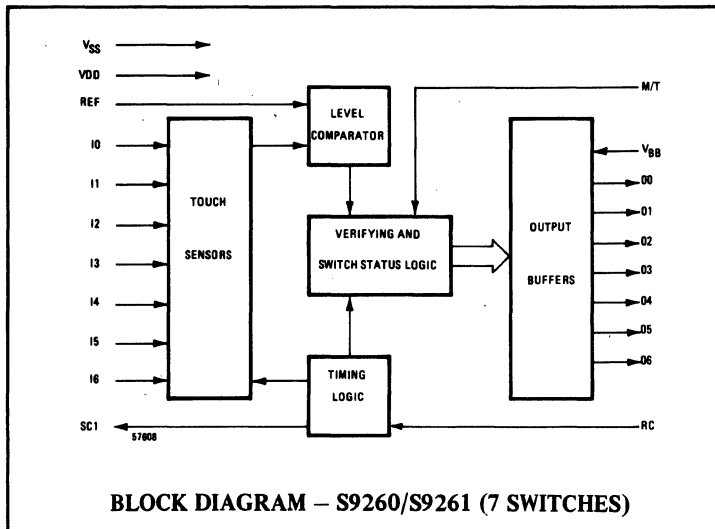
**CIRCUIT TO PANEL CONNECTIONS**

There are a number of ways to make the necessary connections between TouchControl circuits and panels. A simple approach is to use a printed circuit board for the touch panel. In this case, the connections to the circuit are made by the etched copper pattern. In laying out a printed circuit, it is important to keep the copper traces running to the individual touch pads separated from each other as much as possible. In most instances a minimum spacing of 0.125" between traces is acceptable, though wider spacing might be necessary in cases where traces will run parallel to each other for distances of over six inches. It is also important to keep the clock output (SC1) at least 0.75 inches away from any input trace. These spacing requirements are guidelines to be followed regardless of the touch panel material.

With glass touch panels, a simple method for breadboarding systems is to fasten individual wires onto the conductive surfaces with a conductive epoxy. For production situations, it is possible to locate the electronic circuitry on a separate printed circuit board. Contact to the glass touch panel can be made through spring contacts mounted in the appropriate locations on the circuit board. An alternate approach is to route the traces on the glass to an edge of the glass, making connection through an edge connector, keeping in mind the spacing requirements between traces.



#### ADVANCED PRODUCT DESCRIPTION



#### FEATURES

- Interfaces with up to 16 touch switches
- Eliminates contact noise
- Comparator sensing permits use with wide variety of touch switch configurations
- Momentary or toggle operation electrically selectable
- Outputs are TTL/CMOS/MOS compatible
- Simplifies design of touch-sensitive switches

#### FUNCTIONAL DESCRIPTION

Fabricated with P-channel ion implanted MOS/LSI technology, the S9260 family\* of TouchControl integrated circuits has been designed to interface with a variety of touch panel switches and provide a high degree of flexibility in the selection of touch panel materials, layout of touch pad configurations, and design of switching functions. These circuits can interface directly with either seven TouchControl switches (22 lead versions) or sixteen TouchControl switches (40 lead ver-

sions). For each TouchControl switch input there is a corresponding output that may be used to interface with various logic families such as CMOS or TTL.

Both momentary and "push on – push off" (toggle) switching operations are available on all AMI TouchControl circuits and are electrically selected by the logic levels of one input pin. To ensure reliable switch action, a built-in delay is incorporated in all circuits requiring a minimum touch time for switch response.

**ABSOLUTE MAXIMUM RATINGS**

Voltage on any pin relative to $V_{SS}$ :	+ 0.3V to - 20V	Storage temperature (Ambient)	- 65°C to + 150°C
Operating temperature range:	0°C to + 50°C		

\*FOR MULTIPLEXED TOUCHCONTROL CIRCUITS SEE AMI S9262 and S9266.

**ELECTRICAL CHARACTERISTICS**

(0°C <  $T_A$  < 50°C;  $V_{SS} = 0V$ ;  $V_{DD} = - 13.5V$  to - 18.0V unless otherwise specified.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{IL}$	Input logic 0 level – all except “I” inputs.	+ 0.3	0	- 1.5	Volts	Note: M/T input is internally pulled up to $V_{SS}$
$V_{IH}$	Input logic 1 level – all except “I” inputs	- 10.0	- 12.0	- 18.0	Volts	
$f_{RC}$	Internal oscillator frequency measured at RC input.	50		100	kHz	
$T_S$	Switch delay time	50		200	msec	Frequency measured at RC Input = 50 kHz
$T_{RST}$	Time to reset all latches using M/T input.		100		msec	
$V_{OL}$	Output low voltage	$V_{SS}$		- 1.0	Volts	$V_{BB} = V_{SS}$ ; 10K resistive load to $V_{DD}$
$V_{OH}$	Output high voltage			$V_{DD}$		
$V_{OL}$	Output low voltage	$V_{SS}$		$V_{SS} - 0.5$	Volts	$V_{SS} = +5V$ ; $V_{BB} = 0V$
$V_{OH}$	Output high voltage	$V_{BB} + 0.4$		$V_{BB}$		$V_{DD} = 12V$ ; 2800Ω resistive load to $V_{SS}$
SC1	Scan clock output: Output low voltage Output high voltage	$V_{SS}$		- 1.5 $V_{DD}$		Max. capacitive loading < 150 pF

**OPERATION**

Device operation can be understood by referring to Figure 1, depicting a typical application of the S9263. Each of the sixteen pairs of series capacitors labeled S1 – S16 is one touch switch located on a TouchControl panel. (For details on touch panel configuration and operation, see the TouchControl application note included in this APD.) In each capacitor pair, the two common plates represent the conductive area on the control panel surface that is to be touched. The other two plates are formed by two conductive surfaces parallel to the touched surface and located directly under it on the reverse side of the panel. Referring again to Figure 1, the S9263 generates a clock signal on output SC1 that is applied to one plate of each capacitor pair; this signal passes through the two series capacitors and is detected in the MOS circuit. When a panel switch surface is touched, the signal level into the chip diminishes, and the on-chip differential amplifier senses the change and performs the appropriate switching function. For example, if surface S1 is touched, the signal at input I3 decreases, and output O3, normally open, now becomes active and drives the S1 input to the TTL circuitry toward voltage level  $V_{BB}$ .

**I INPUTS**

Inputs from the touch switch pads to the TouchControl circuit are labeled I0 through I15 (S9263, S9264, and S9265) or I0 through I6 (S9260 and S9261). Each I input relates directly to an O output of identical numeral.

**RC INPUT**

A resistor connected to  $V_{DD}$  and a capacitor connected to  $V_{SS}$  are connected to the RC input pin to establish the on-chip clock frequency that controls the touch switch delay time. Nominal values for these components are suggested in Figure 1, but they may be varied to change clock frequency over a range of 50 kHz to 100 kHz.

**REF INPUT**

In order to allow flexibility in the choice of TouchControl panel materials, switch layout, and switch size, AMI Touch Control inputs have been designed to detect a differential change rather than an absolute change in level. To obtain a reference level, two resistors are connected to input REF, one to  $V_{SS}$  and the other to  $V_{DD}$ .

## O OUTPUTS

Each output pin labeled "O" corresponds to an input pin labeled "1." Whenever an input is selected, the output becomes active and will drive an external load toward supply voltage  $V_{BB}$ . When outputs are not active, they are high impedance open drain.

## $V_{BB}$ SUPPLY

The sources of all output devices are common and connected to pin  $V_{BB}$ . This allows TTL compatibility as shown in Figure 1, as well as the ability to drive higher level signals. For instance, if  $V_{SS} = 0$  volts,  $V_{DD} = -16$  volts, and  $V_{BB} = V_{SS}$ , then active outputs would drive a load connected to  $V_{DD}$  towards  $V_{SS}$ . The  $V_{BB}$  pin can be used also to switch analog signals; in this configuration the analog signals are applied to the "O" pins and  $V_{BB}$  is the output pin.

## M/T INPUT

The M/T input pin selects the mode of switch operation, either momentary or toggle. With no connection to the M/T pin momentary operation is selected, and appropriate outputs are active only for the duration of touching a switch. In this mode, no output is active when no switch is touched. A  $V_{DD}$

level applied to M/T causes the circuit to operate in the toggle mode. In this condition, the brief touch of any switch will turn on the appropriate output, which will remain latched on until the switch is touched again. Subsequent activations of the switch will toggle the corresponding output on and off alternately. To reset all outputs when the toggle mode is selected, a pulse of  $V_{SS}$  level may be applied to the M/T input.

## SCI OUTPUT

The SCI output provides the clock signal for the Touch-Control panel. Its frequency is determined by the RC time constant, and it is connected in common with one of each of the two common conductive surfaces on the reverse side of the touch panel.

## MOMENTARY AND TOGGLE COMBINATION

The S9261, S9264, and S9265 contain several outputs that are permanently in the momentary mode of operation. With the M/T input at  $V_{SS}$  these parts function identically to the S9260 and S9263. With M/T at a logic 1 level, however, the S9261 has four momentary and three toggle inputs. Table 1 shows the combinations available on all three parts.

TABLE 1. COMPARISON OF FEATURES

Part Number	Pin Count	Touch Switch Capacity			Number of Outputs
		Total Touch Switch Interface Capability	Touch Inputs Selectable For Either Momentary Or Toggle Operation Through Use of M/T Input	Touch Switch Inputs Fixed In Momentary Operation (Not affected by state of M/T input)	
S9260	22	7	7	0	7
S9261	22	7	3 (I4 thru I6)	4 (I0 thru I3)	7
S9263	40	16	16	0	16
S9264	40	16	8 (I8 thru I15)	8 (I0 thru I7)	16
S9265	40	16	12 (I4 thru I15)	4 (I0 thru I3)	16

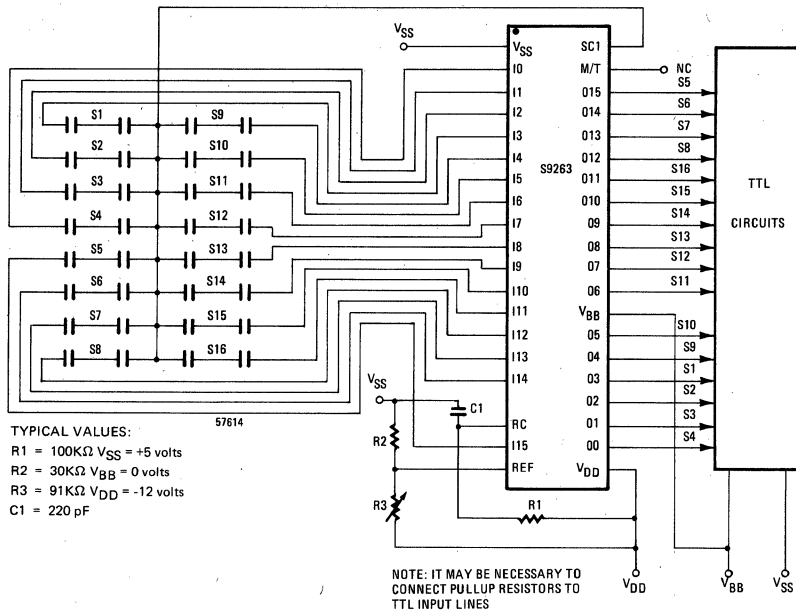


FIGURE 1. 16 SWITCH APPLICATION USING S9263

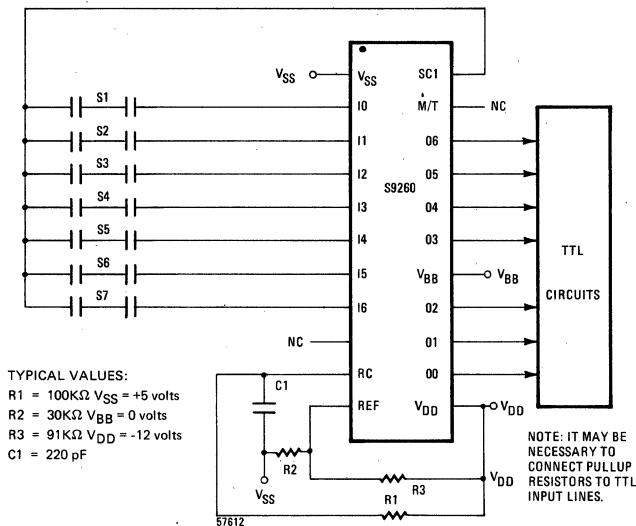
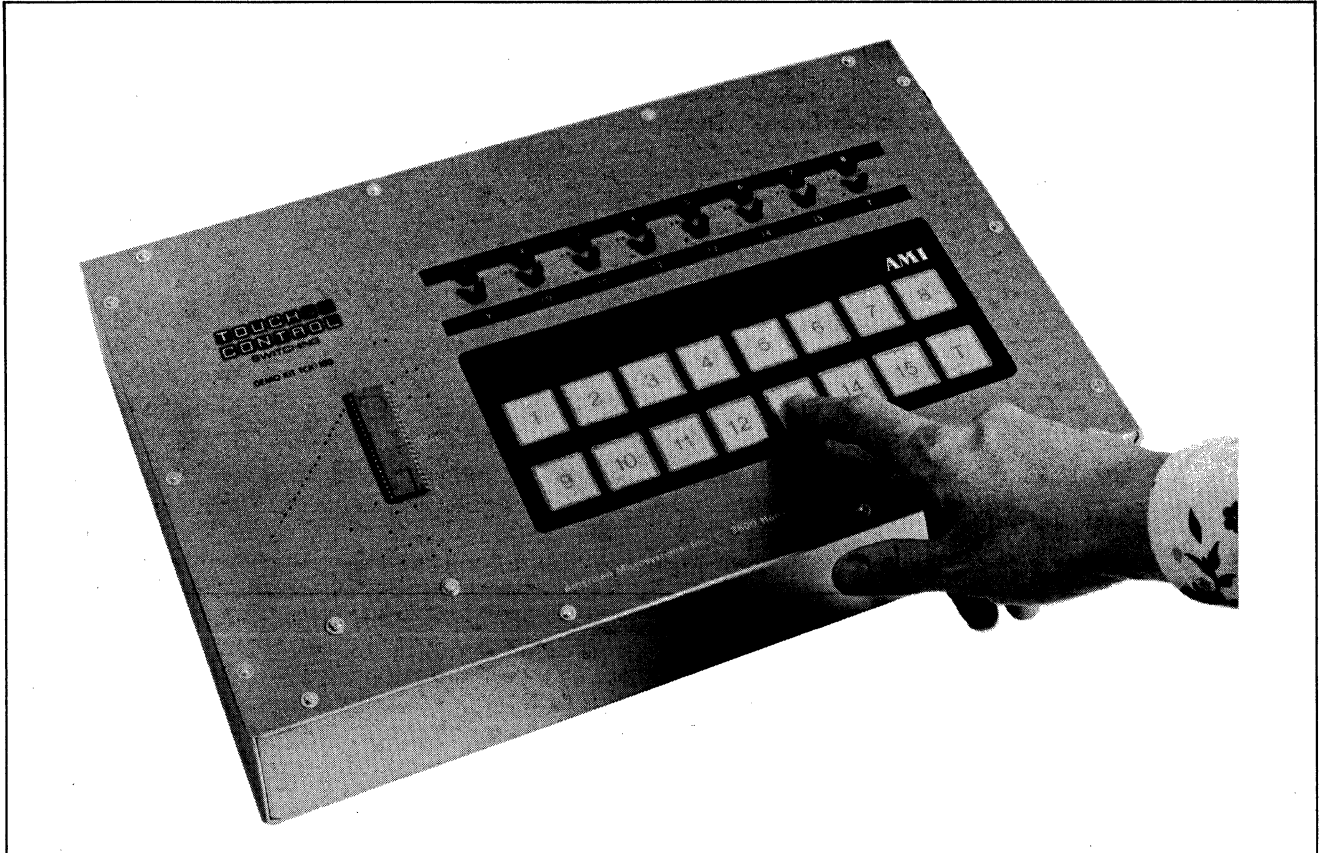


FIGURE 2. 7 SWITCH APPLICATION USING S9260

TOUCHCONTROL APPLICATION NOTES

See Application Notes at the end of S9262/S9266 data sheet pages in this Section.



### FEATURES

- 16 TouchControl Switches can Operate in Different Modes
- Quick and Convenient for Demonstrating TouchControl Concept
- Interfaces Easily to External Logic for Prototype Development
- Can Drive up to 16 LED Indicators
- Provisions for Adding Power Supply Components (for 115 VAC Operation)

### INTRODUCTION

The AMI TouchControl kit demonstrates the ease with which this unique system of capacitive switching may be implemented. Included in the kit are a printed circuit board and AMI's newly developed S9263 TouchControl circuit. The printed wiring board, which has 16 touch switches etched onto its top surface, contains on its reverse side all the interconnection necessary to interface the S9263 inputs with the 16 touch switches and the S9263 outputs with 16 light emitting diodes. As the touch switches

are activated, the corresponding diodes are lighted to indicate the output states of the S9263. If desired, external logic may be operated by connecting a cable directly to the S9263 outputs.

Additional components required for the kit are readily available, and assembly of the kit should take less than an hour's time. The circuit board may be mounted either on standoffs or on a standard aluminum chassis box.

**PARTS LIST FOR AMI TOUCHCONTROL KIT:**

QUANTITY REQUIRED	DESCRIPTION	QUANTITY REQUIRED	DESCRIPTION
1	S9263 TouchControl circuit (Included)	16	3.3K $\Omega$ Resistor ¼ Watt
1	Printed wiring board (Included)	1	Transistor 2N3569 or equivalent
1	Transformer, 12.6 volt 300mA	1	500 $\mu$ F capacitor/20 volts
	Radio Shack P/N 273-1385 or equivalent	1	0.33 $\mu$ F capacitor
1	Line cord	1	270 pF capacitor
1	Diode IN920 or equivalent	16	Light emitting diode — MV5023 or equivalent
2	100K $\Omega$ Resistor ¼ Watt		
1	60K $\Omega$ Resistor ¼ Watt	1	Aluminum chassis box—15" x 9" Bud No. AC1421 or equivalent (optional)
1	15K $\Omega$ Resistor ¼ Watt		
1	10K $\Omega$ Resistor ¼ Watt		

**ASSEMBLY**

The circuit board may be assembled easily by referring to Figure 2, a view of the reverse side of the board. For appearance, it is recommended that all components except the LED's and the S9263 be mounted on the reverse side of the board, with all leads cut off flush with the board's top surface.

For convenience, a 15 volt power supply is provided on the circuit board, so that the system may be plugged into a standard 110 volt outlet. If desired, an external DC supply of 15 volts may be used, connecting the positive and negative outputs to the corresponding holes designated for C1. If a DC supply is used, the transformer, diode, and C1 may be eliminated.

**OPERATION**

The AMI TouchControl kit provides sixteen touch switches that interface with the S9263 to activate sixteen light emitting diodes. Each of the switches numbered from one to fifteen has a light associated with it which is labeled with the same number. The switch labeled "T" is used to select the mode of operation of the S9263, either momentary or toggle. When the LED labeled "T" is off, touch pads one through fifteen operate as momentary switches, and any switch's corresponding LED will turn on when the switch is touched, remaining on only for the duration of touching the switch. If "T" is touched, the "T" LED will turn on and stay on even after "T" is untouched. The S9263 is now operating in a toggle mode, and the brief touch of any switch from one through fifteen will cause its corresponding LED to turn on and latch. Subsequent activations of the switch will turn the LED

off and on alternately. Touching "T" once again causes the "T" LED to turn off, and the S9263 once again operates in the momentary mode. By removing the 0.33 $\mu$ F capacitor, it is possible to use the "T" pad as a clear switch. In this mode, all numbered pads function as "push on, push off" switches. Touching the "T" pad turns off all LED's corresponding to the numbered switches.

To operate external logic systems with the TouchControl kit, a cable may be soldered, using a grounded soldering iron, directly to the outputs of the S9263. The voltage on an output that is turned off (corresponding LED is off) is - 15 volts (or  $V_{DD}$ ). When turned on, the output will rise towards ground ( $V_{SS}$ ). Appropriate loading conditions are specified in the advanced product description for this part.

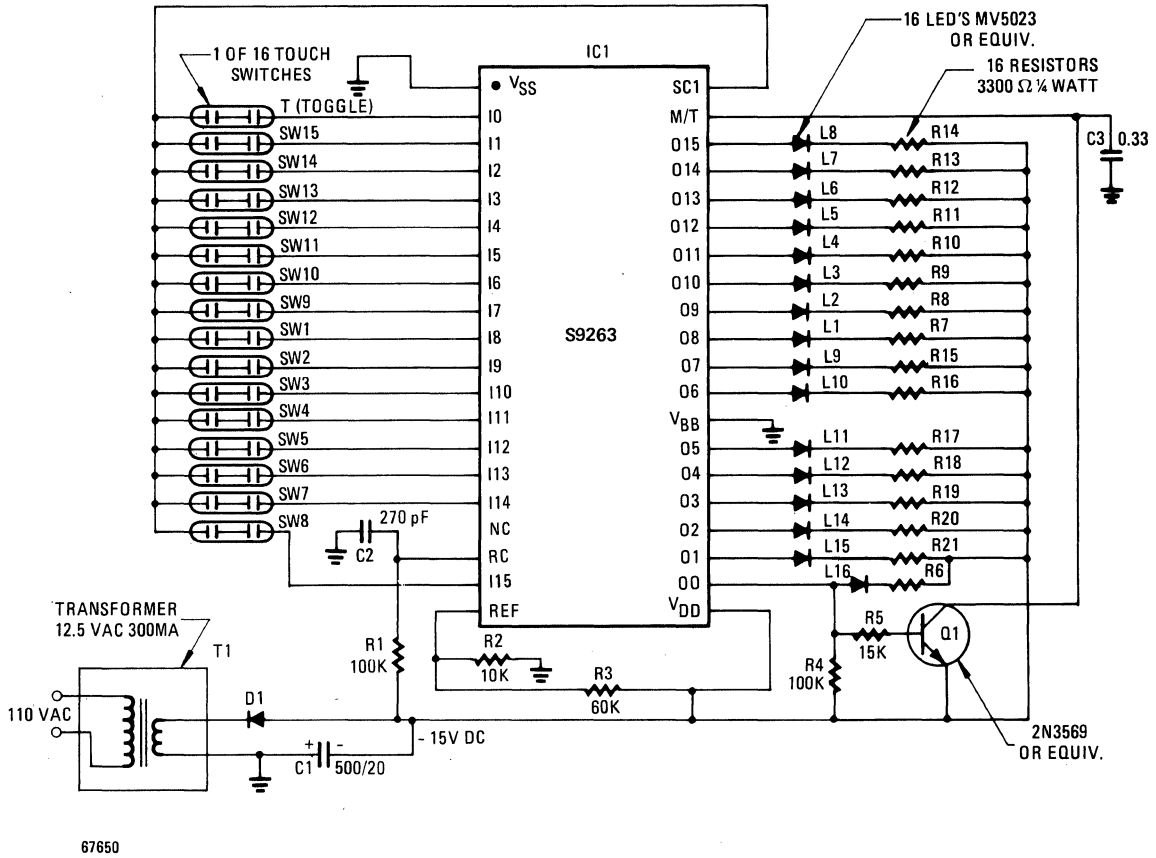


FIGURE 1. SCHEMATIC DIAGRAM OF TCK-100

**PARTS LIST FOR ASSEMBLING TCK – 100 KIT:**

PART NUMBER	PART DESCRIPTION	PART NUMBER	PART DESCRIPTION
R1, R4	100 K $\Omega$ ¼ Watt resistor	Q1	NPN transistor 2N3569 or equivalent
R2	10 K $\Omega$ ¼ Watt resistor	D1	Diode IN920 or equivalent
R3	60 K $\Omega$ ¼ Watt resistor	L1 thru L16	Light emitting diode – MV5023 or equivalent
R5	15 K $\Omega$ ¼ Watt resistor	IC1	AMI integrated circuit S9263
R6 thru R21	3.3 K $\Omega$ ¼ Watt resistor	T1	Transformer 12.6 VAC @ 300 mA. Radio Shack P/N 273-1385 or equivalent
C1	500 $\mu$ F capacitor 20 Volts		
C2	270 pF capacitor		
C3	0.33 $\mu$ F capacitor		

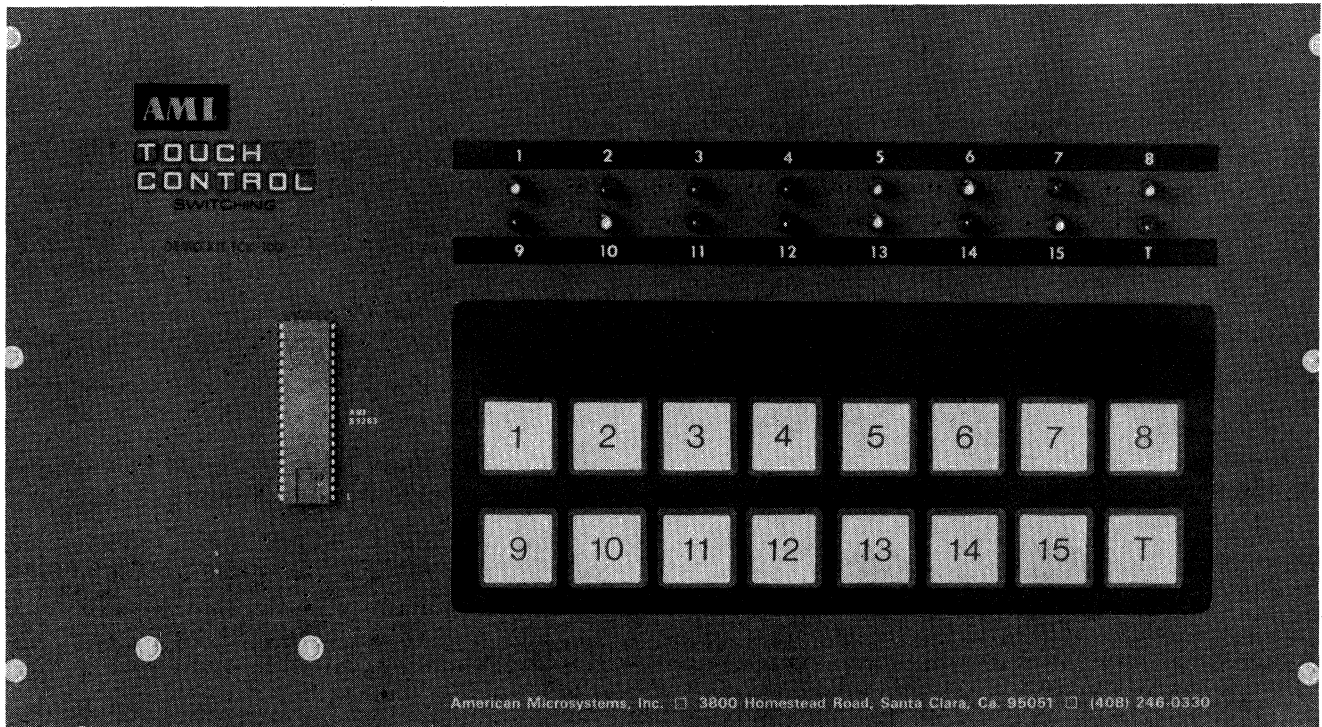


FIGURE 2. REAR OF CIRCUIT BOARD

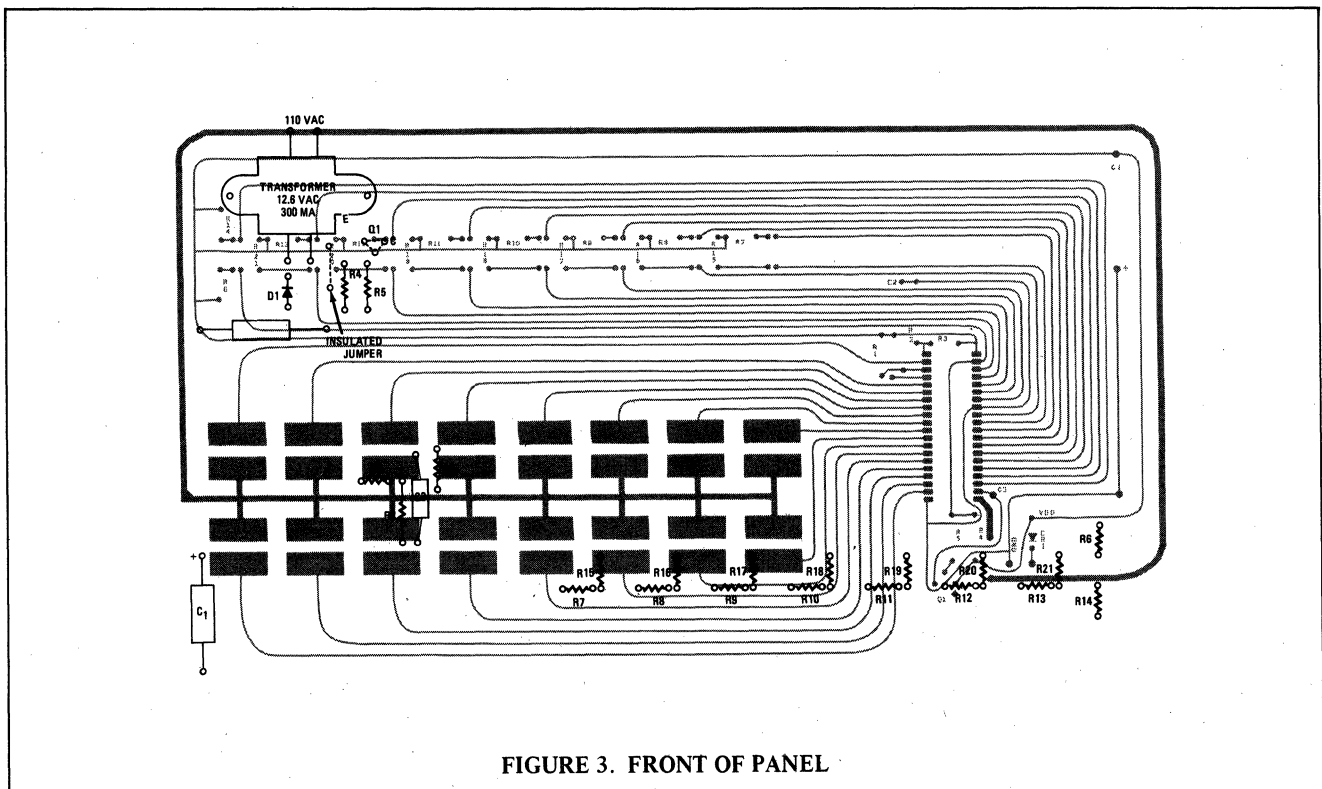


FIGURE 3. FRONT OF PANEL



# 5

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## Organ Circuits

## Organ Circuits

Part No.	Description	Input/Output	Power Supply (V)	Process	Packages
S10110	Analog Shift Register	Analog	-24	P-I <sup>2</sup>	P
S2193	Seven-Stage Frequency Divider	MOS	-14; -28	P-I <sup>2</sup>	P
S10129	Seven-Stage Frequency Divider <sup>(1)</sup>	MOS	-14, -27	P-I <sup>2</sup>	P
S10130/31	Six-Stage Frequency Divider <sup>(1)</sup>	MOS	-14, -27	P-I <sup>2</sup>	P
S2567	Rhythm Counter	MOS	-15, -27	P-HI V <sub>T</sub>	P
S50240/41/42	Top Octave Synthesizer	MOS	-14	P-I <sup>2</sup>	P
S50243/44/45	Top Octave Synthesizer <sup>(2)</sup>	MOS	-14	P-I <sup>2</sup>	P
S8890	Rhythm Generator <sup>(3)</sup>	MOS	-12	P-I <sup>2</sup>	C,P,S
S9660	Rhythm Generator <sup>(1)</sup> <sup>(3)</sup>	MOS	-12	P-I <sup>2</sup>	P

(1) Various Printouts Available

(2) Identical to S50240/41/42 except maximum operating frequency is 800 KHz

(3) Programmable ROM Pattern

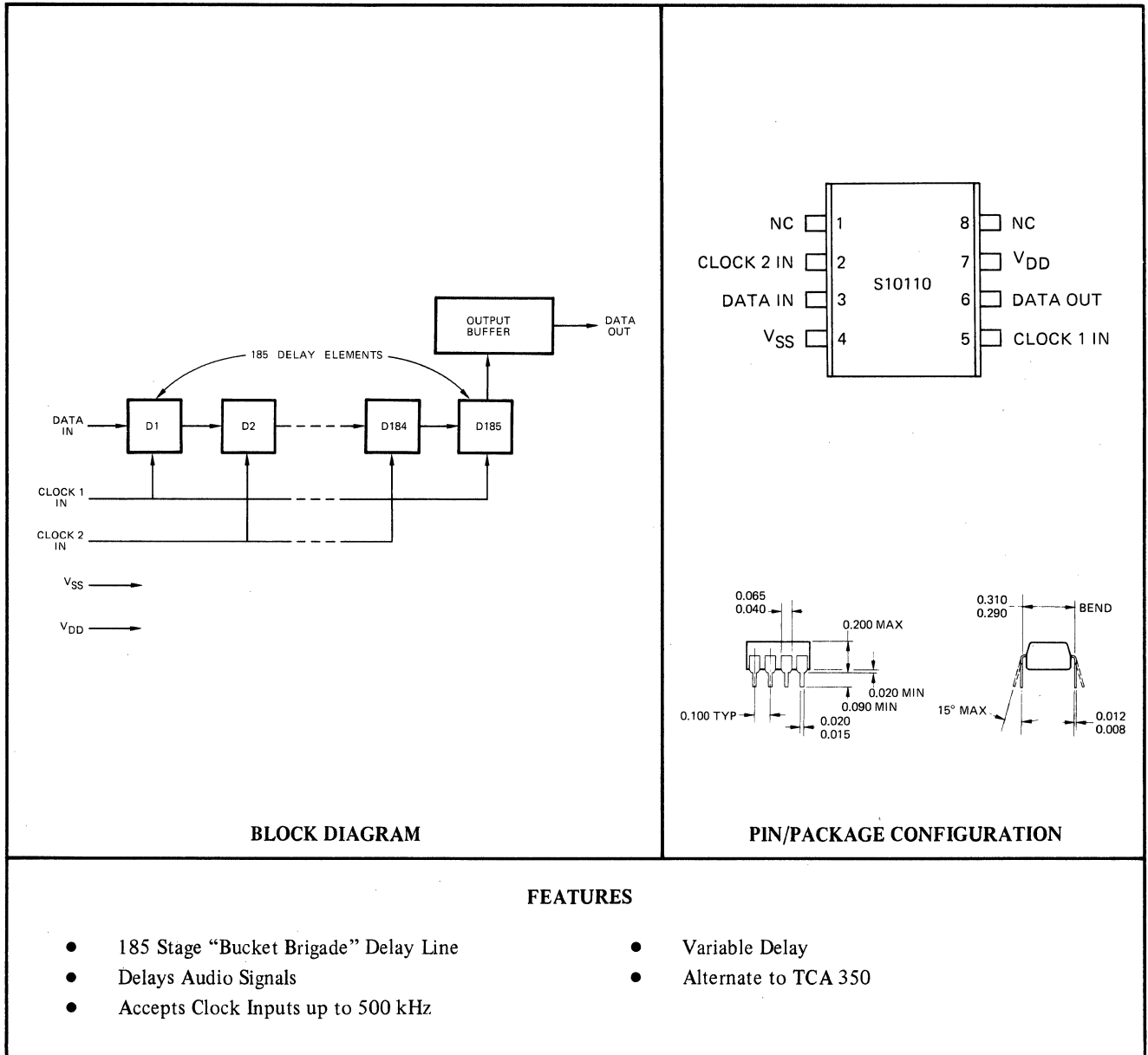
## Future Products

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**S2688** – Noise Generator – P-channel ion implanted MOS seventeen-bit shift register clocked by an internal RC oscillator. Outputs wide bandwidth pseudo white noise and is used for cymbal, brush, sandblock, snare drum, and other sound generation. (Second source for National MM5837).

**S10111** – Analog Shift Register similar to the S10110 with the addition of an on-chip clock.

### ADVANCED PRODUCT DESCRIPTION



### FUNCTIONAL DESCRIPTION

The S10110 analog shift register is a monolithic circuit fabricated with P-channel ion-implanted MOS technology. The part differs from a digital shift register, which is capable of only digital input and output information, in that an audio signal is typically supplied as the data input to the analog

register, and the output is the same audio signal delayed in time. The amount of signal delay is dependent on the number of bits of delay (185) and the frequency of the two symmetrical clock inputs. Since each negative-going clock edge transfers data from one stage to the next, the analog signal delay equals  $185 \div 2 \times$  clock frequency.

**OPERATION**

Device operation may be understood by referring to Figure 1. This is an actual schematic diagram of the analog shift register, or "bucket brigade," showing typical external bias techniques.

**Data In Input:**

The analog signal, or audio signal, to be delayed is applied to pin 3. This input must be biased to a negative voltage of approximately - 8 volts, and two resistors may be used as a voltage divider to provide this bias. They must be chosen so that  $(R_1) \cdot (R_2) \div (R_1 + R_2)$  is less than 20 K $\Omega$ . The input signal applied to this input through series capacitor C<sub>IN</sub> may be as high as 6 volts peak to peak.

**CLOCK 1 and CLOCK 2 Inputs:**

Applied respectively to pins 5 and 2, Clock 1 and Clock 2 are two symmetrical non-overlapping negative-going clocks used to transfer the analog data along the 185 bit delay line. Although these clocks may have a duty cycle as low as 25% (i.e.: each clock signal is at a negative level for 25% of its period), better output signals will be obtained with both clock duty cycles closer to 50%. It is important, however, that no overlap of the clock signals occurs at a level more negative than V<sub>SS</sub> - 0.8 volts.

Referring again to Figure 1, it can be seen that when Clock 1 is negative, data is transferred from the data input to capacitor C1; likewise, data is transferred from each even-numbered capacitor to the capacitor to its right. When Clock 2 is negative, data is transferred from C1 to C2 and from each other odd-numbered capacitor to the capacitor to its right. In this manner, data is shifted from the input to C185 after a total of 185 negative clock pulses has occurred (i.e.: 93 periods of Clock 1 and 92 periods of Clock 2).

**Data Out Output:**

The output of the S10110 analog shift register is a single device, T187, with its drain at V<sub>DD</sub> and its source connected to pin 6. If a 47K resistor to V<sub>SS</sub> is supplied at this pin, T187 functions as a source follower.

Referring to Figure 3, it can be seen that the output potential during Clock 2 is a constant value near - 10 volts. When Clock 1 switches on (negative), the output instantaneously drops to a level of approximately - 30 volts; this is caused by the 20 volt swing of Clock 1 and C185. As Clock 1 remains on, device T185 transfers charge from C184 to C185, and the output voltage becomes more positive, depending on the charge previously stored on C184. It is during this part of Clock 1 that the output reflects the analog data stored on C1 185 bits earlier. Since the clock signal now appears on the output, it is necessary to apply the appropriate filtering to obtain the delayed analog signal.

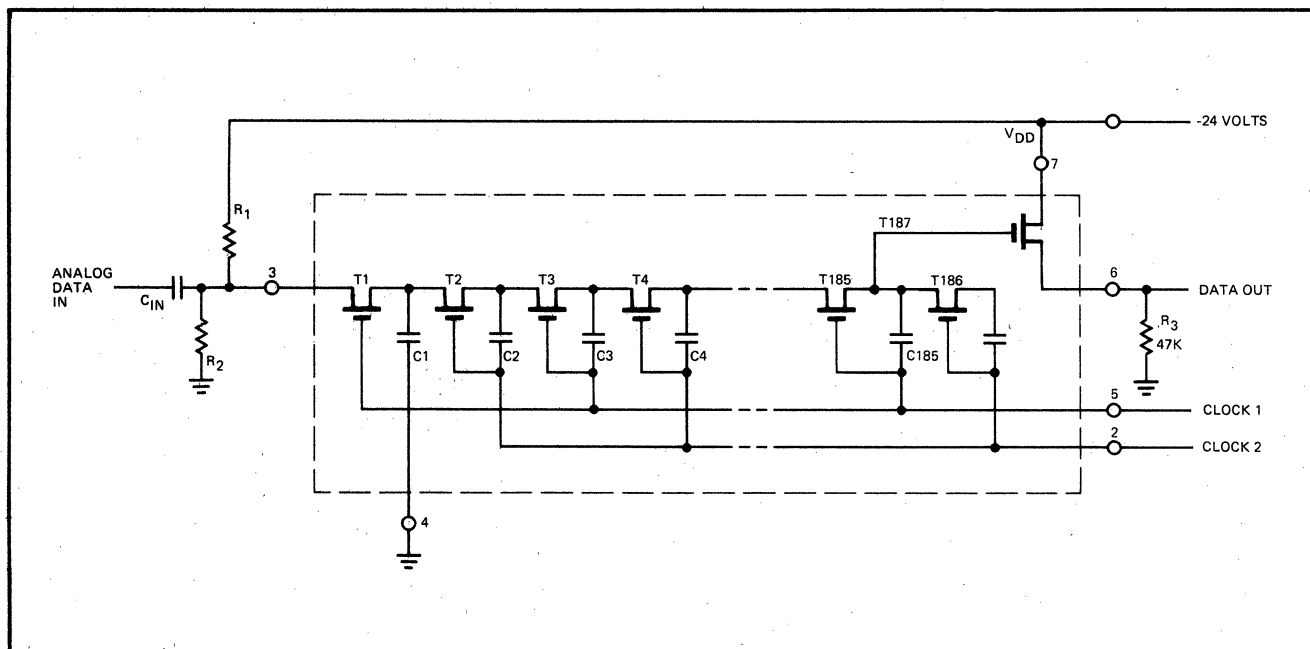


FIGURE 1. SCHEMATIC DIAGRAM AND PINOUTS OF S10110

277183

## APPLICATIONS

- Delay of Audio Signals
- Electronic Chorus
- Electronic Vibrato
- String Ensemble
- Reverberation
- Rotating Speaker Simulation

## ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V <sub>SS</sub> :	+ 0.3V to - 30V	Storage temperature (ambient):	- 65°C to + 150°C
Operating temperature range:	0°C to + 70°C		

## ELECTRICAL CHARACTERISTICS

(0°C < T<sub>A</sub> < 70°C; V<sub>DD</sub> = - 24V ± 2V; V<sub>SS</sub> = 0V.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V <sub>CLKL</sub>	CLOCK 1 and CLOCK 2 Inputs Logic Level "0"	V <sub>SS</sub>		V <sub>SS</sub> - 0.8	Volts	No overlap of signals more negative than V <sub>SS</sub> - 0.8V
V <sub>CLKH</sub>	CLOCK 1 and CLOCK 2 Inputs Logic Level "1"	- 18		- 20	Volts	See Figure 2
t <sub>CLKH</sub>	Duration of CLOCK Logic "1" Level	0.2 x T <sub>CLK</sub>				See Figure 2
f <sub>CLK</sub>	CLOCK Input Frequency	5		500	kHz	
V <sub>BIN</sub>	Input Bias Voltage	- 7.5		- 8.5	Volts	See Figure 1
R <sub>BIN</sub>	Resistance of the Bias Voltage Source at Input			20	KΩ	R <sub>BIN</sub> = (R1) x (R2) ÷ (R1 + R2) See Figure 1
V <sub>DIN</sub>	Signal Level at Data In Input			6	Volts P - P	
a	Analog Signal Attenuation			4	dB	
t <sub>D</sub>	Signal Delay		185			
f <sub>3dB</sub>	3dB Response Point		2 x f <sub>CLK</sub> 0.1 x f <sub>CLK</sub>			

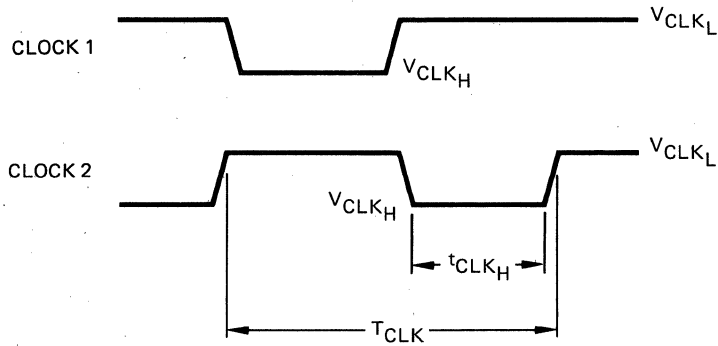


FIGURE 2. TIMING DIAGRAM OF CLOCK 1 and CLOCK 2 SIGNALS

277184

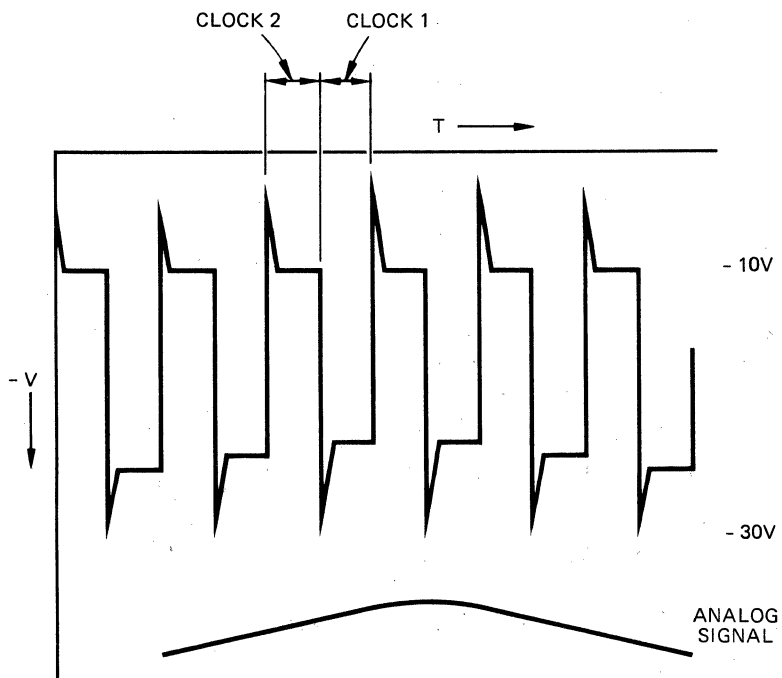
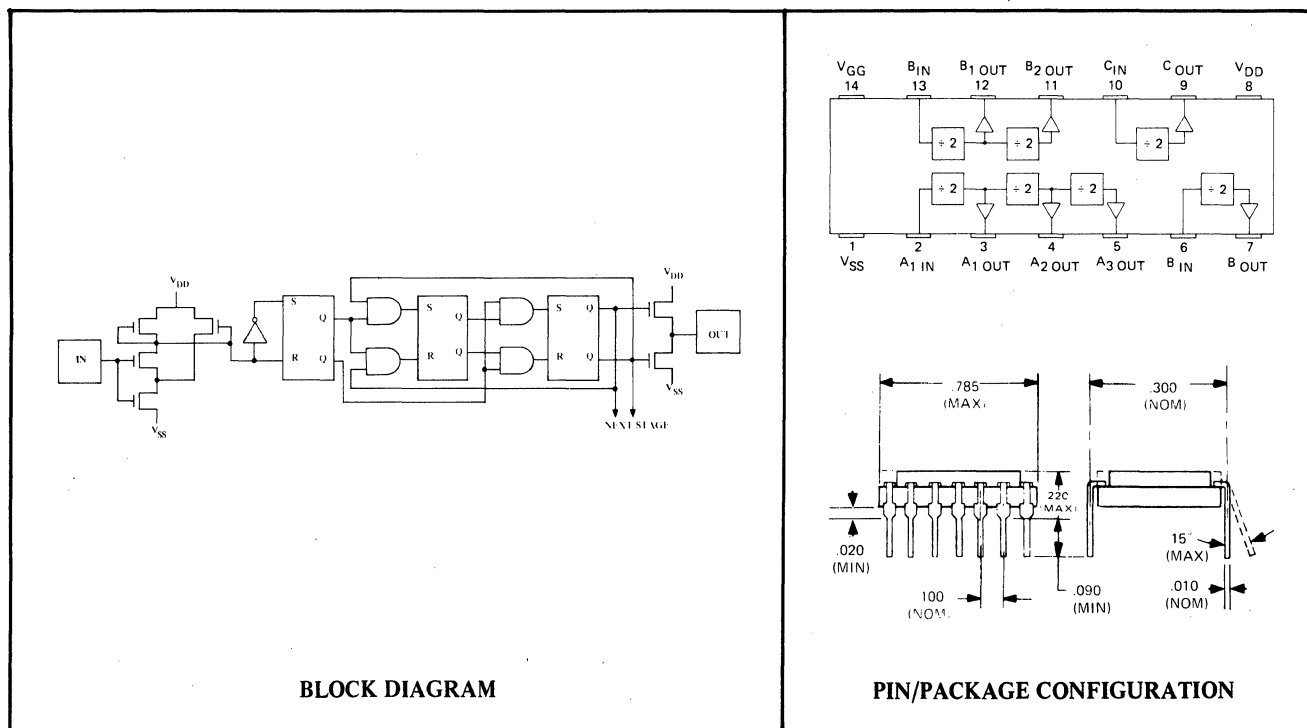


FIGURE 3. S10110 OUTPUT WAVEFORM

277185



**BLOCK DIAGRAM**

**PIN/PACKAGE CONFIGURATION**

### FEATURES

- Pin for Pin Equivalent to SESCOSEM SFF5002
- Contains Seven Triggerable Flip-Flops
- Schmidt Trigger Inputs
- Triggers on Negative Going Input
- 2 Power Supplies  $-14V, -28V$
- High Impedance Inputs
- Push-Pull Outputs
- 1 MHz Input Frequency

### FUNCTIONAL DESCRIPTION

This FREQUENCY DIVIDER provides seven stages of binary division in a 14 lead, dual in-line package. P-Channel enhancement mode technology is utilized. This device has buffered outputs for low source impedance drive and short circuit protection. The S2193 is ideally suited for tone generation in electronic organs.

Each divider stage of the S2193 consists of an asynchronous, decoupled flip-flop. The seven stages are internally connected in cascades of one, two, and three flip-flops each.

One side of each flip-flop drives a push-pull output buffer, which provides low output impedance in both logic states. The buffer outputs will drive both capacitive loads and discrete

circuits with well defined levels. The buffers have low standby current and are powered by  $V_{DD}$ . This voltage functions as a clamp voltage and thus sets the output amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

### APPLICATIONS

Electronics music tone synthesis, frequency division, N Stage dividers, low frequency generation, timing and control waveforms, binary counters.

**ABSOLUTE MAXIMUM RATINGS**

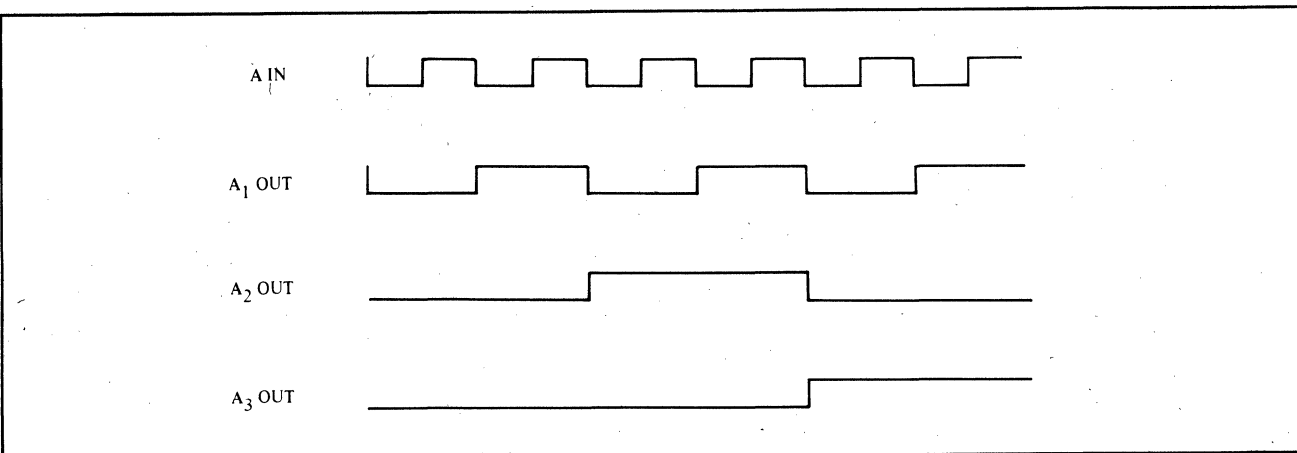
Positive Voltage on any Pin . . . . .	$V_{SS} + 0.3V$
Negative Voltage on any Pin . . . . .	$V_{SS} - 30V$
Storage and Operating Chip Temperature . . . . .	$- 55^{\circ}C$ to $+150^{\circ}C$
Operating Ambient Temperature . . . . .	$0^{\circ}C$ to $+ 70^{\circ}C$

**DYNAMIC CHARACTERISTICS**

( $T_A = 0^{\circ}$  to  $+ 70^{\circ}C$ ,  $V_{SS} = \text{Ground}$ ,  $V_{DD} = -14V \pm 1V$ ,  $V_{GG} = -28 \pm 1V$ )

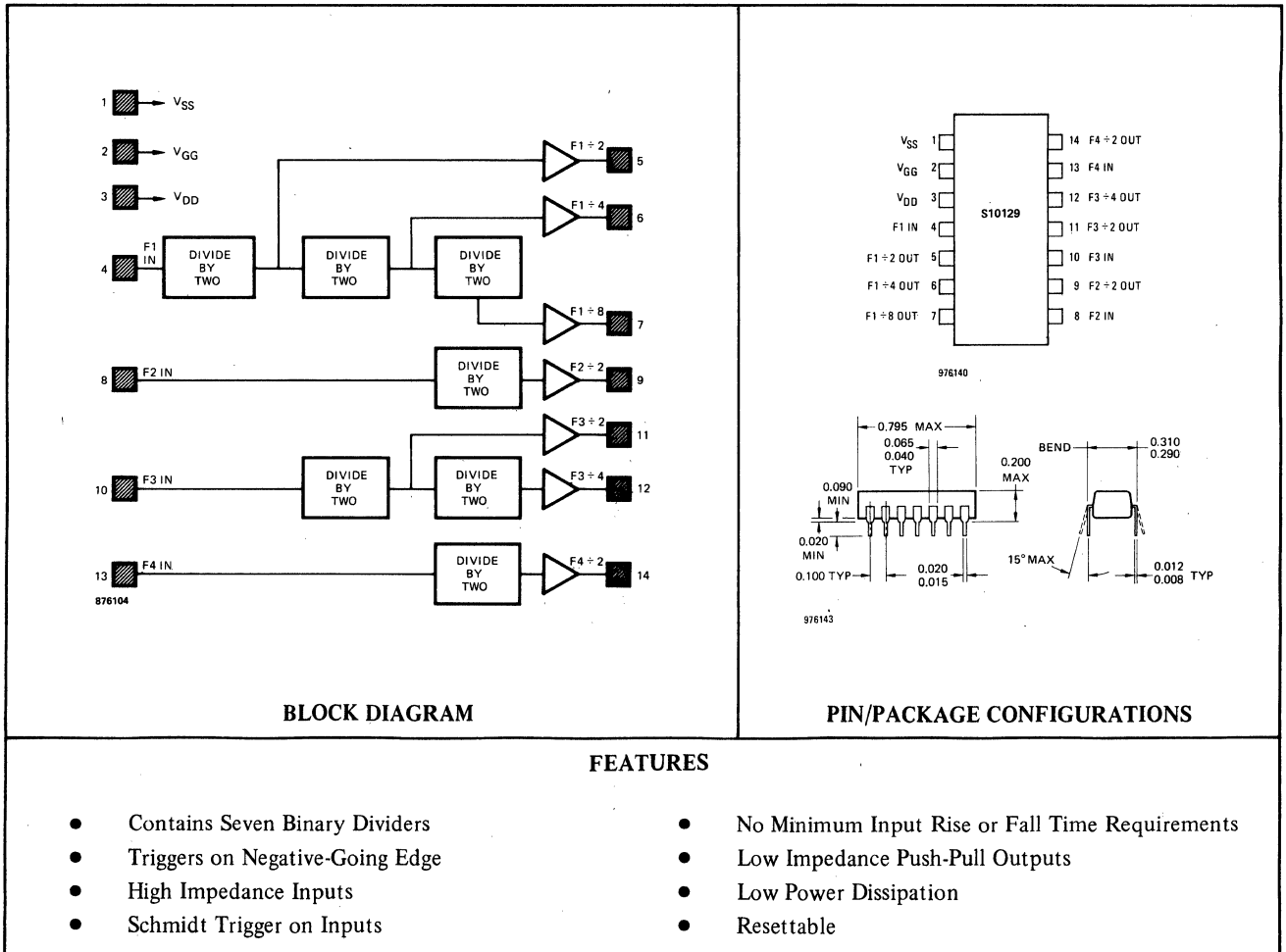
		MIN	TYP	MAX	UNITS	CONDITIONS
$V_{IH}$	Input High Level	$V_{SS} - 2.0$		+ 0.3	Volts	
$V_{IL}$	Input Low Level			-8.0	Volts	
$V_{OH}$ $V_{OL}$	Output High Level Output Low Level	$V_{SS} - 1.6$		-11.0 -8.0	Volts Volts Volts	$I_{OUT} = 0.8 \text{ mA}$ $I_{OUT} = + 0.1 \text{ mA}$ $I_{OUT} = + 0.8 \text{ mA}$
PW	Input Pulse Width	300			ns	Load = 1 m $\Omega$ and 10 pF
f	Input Frequency			100	kHz	
$t_r$	Output Transition Time		0.6		us	
$I_{GG}$	$V_{GG}$ Supply Current			14	mA	
$I_{DD}$	$V_{DD}$ Supply Current			1.0	mA	

**TIMING CHARACTERISTICS**





### ADVANCED PRODUCT DESCRIPTION



### FUNCTIONAL DESCRIPTION

The S10129 is a monolithic frequency divider circuit fabricated with P-Channel ion-implanted MOS technology. The circuit provides seven stages of binary division in a 3 - 2 - 1 - 1 configuration; the S10129 is ideally suited for tone generation in electronic organs.

All inputs to the device are buffered to permit easy triggering of the divider stages. Outputs of each divider are buffered to provide low output impedance in both logic states to drive external circuitry as well as other dividers. The buffers have low standby current and are powered by VDD. This voltage functions as a clamp voltage and thus sets the output

amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

All divider outputs may be reset to a logic low level (VSS) by momentarily applying a logic low level to the VGG supply input. This is particularly desirable in some electronic organs in which phase relationships are important.

### APPLICATIONS

Electronic organ frequency generator, organ pedal frequency generator, electronic music synthesizers, N stage dividers, low frequency generation, binary counters.

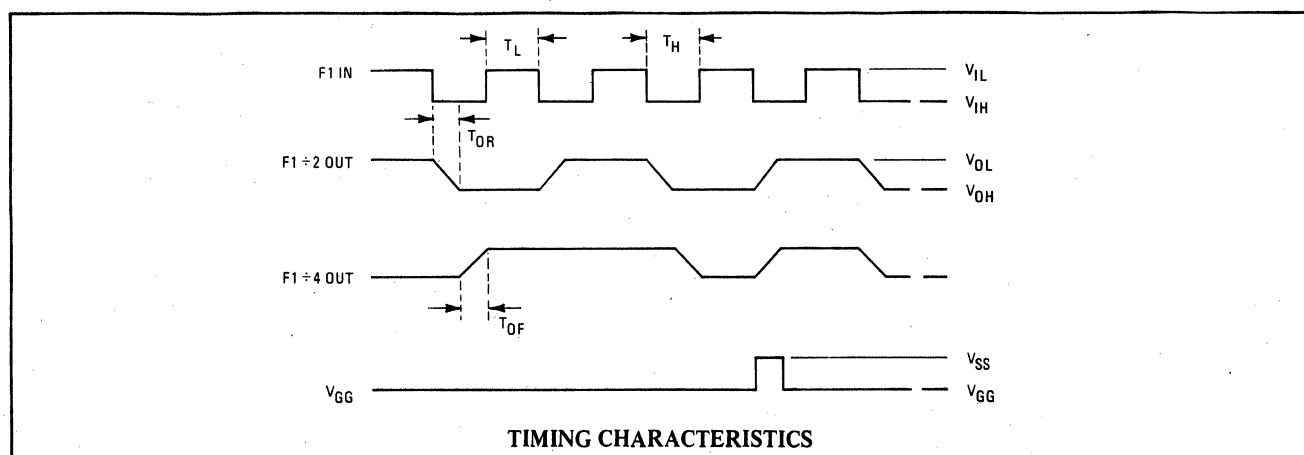
**ABSOLUTE MAXIMUM RATINGS**

Voltage on any pin relative to V <sub>SS</sub>	+ 0.3V to - 20V	Storage temperature	- 55°C to + 150°C
Voltage on V <sub>GG</sub> relative to V <sub>SS</sub>	+ 0.3V to - 30V	Operating temperature (ambient)	0°C to 70°C

**ELECTRICAL CHARACTERISTICS**

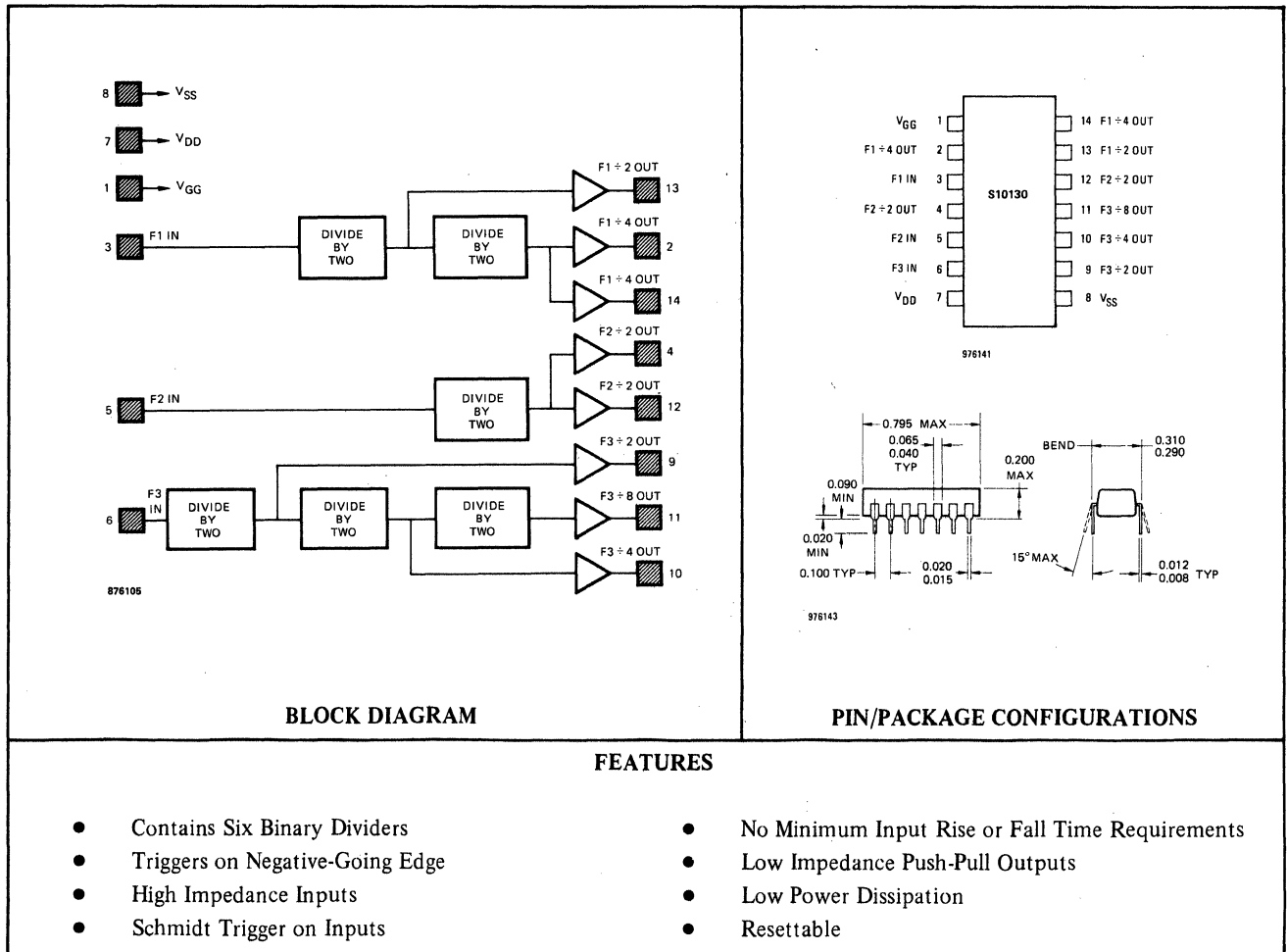
(0°C ≤ T<sub>A</sub> ≤ 70°C V<sub>DD</sub> = - 11V to - 16V; V<sub>GG</sub> = - 25V to - 29V unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V <sub>IL</sub>	Input Clock Low	V <sub>SS</sub> + 0.3		V <sub>SS</sub> - 2.0	Volts	
V <sub>IH</sub>	Input Clock High	V <sub>SS</sub> - 8		V <sub>GG</sub>	Volts	
f <sub>IN</sub>	Input Clock Frequency	DC		250	kHz	
T <sub>H</sub> , T <sub>L</sub>	Input Clock on & off times	1.5			μs	
V <sub>R</sub>	Voltage applied to V <sub>GG</sub> input to cause a reset condition	V <sub>SS</sub>		V <sub>SS</sub> - 0.5	Volts	
T <sub>R</sub>	Duration of V <sub>R</sub> to cause reset	10			μs	50% to 50% point
V <sub>OH</sub>	Output high level	- 11		V <sub>DD</sub>	Volts	V <sub>DD</sub> = - 12V V <sub>GG</sub> = - 26V 5.5KΩ load to V <sub>SS</sub>
V <sub>OL</sub>	Output low level	V <sub>SS</sub>		- 1	Volts	V <sub>DD</sub> = - 12V V <sub>GG</sub> = - 26V 5.5KΩ load to V <sub>DD</sub>
C <sub>IN</sub>	Input Capacitance		5	10	pF	Applies only to clock inputs
T <sub>OR</sub> , T <sub>OF</sub>	Output rise and fall time		1	2	μs	40 pF load applied
I <sub>GG</sub>	V <sub>GG</sub> supply current		2	3	mA	V <sub>DD</sub> = - 12V V <sub>GG</sub> = - 26V No load
I <sub>DD</sub>	V <sub>DD</sub> supply current		5	7	mA	V <sub>DD</sub> = - 12V V <sub>GG</sub> = - 26V No load



**TIMING CHARACTERISTICS**

### ADVANCED PRODUCT DESCRIPTION



### FUNCTIONAL DESCRIPTION

The S10130 is a monolithic frequency divider circuit fabricated with P-Channel ion-implanted MOS technology. The circuit provides six stages of binary division in a 3 - 2 - 1 configuration; the S10130 is ideally suited for tone generation in electronic organs.

All inputs to the device are buffered to permit easy triggering of the divider stages. Outputs of each divider are buffered to provide low output impedance in both logic states to drive external circuitry as well as other dividers. The buffers have low standby current and are powered by VDD. This voltage functions as a clamp voltage and thus sets the output

amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

All divider outputs may be reset to a logic low level (VSS) by momentarily applying a logic low level to the VGG supply input. This is particularly desirable in some electronic organs in which phase relationships are important.

### APPLICATIONS

Electronic organ frequency generator, organ pedal frequency generator, electronic music synthesizers, N stage dividers, low frequency generation, binary counters.

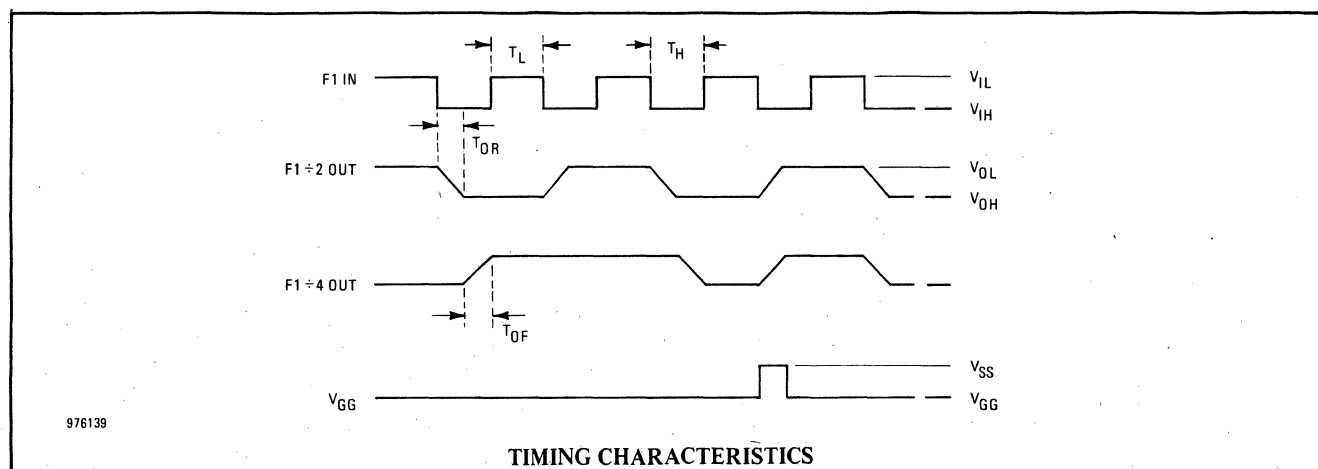
**ABSOLUTE MAXIMUM RATINGS**

Voltage on any pin relative to VSS	+ 0.3V to - 20V	Storage temperature	- 55°C to + 150°C
Voltage on VGG relative to VSS	+ 0.3V to - 30V	Operating temperature (ambient)	0°C to 70°C

**ELECTRICAL CHARACTERISTICS**

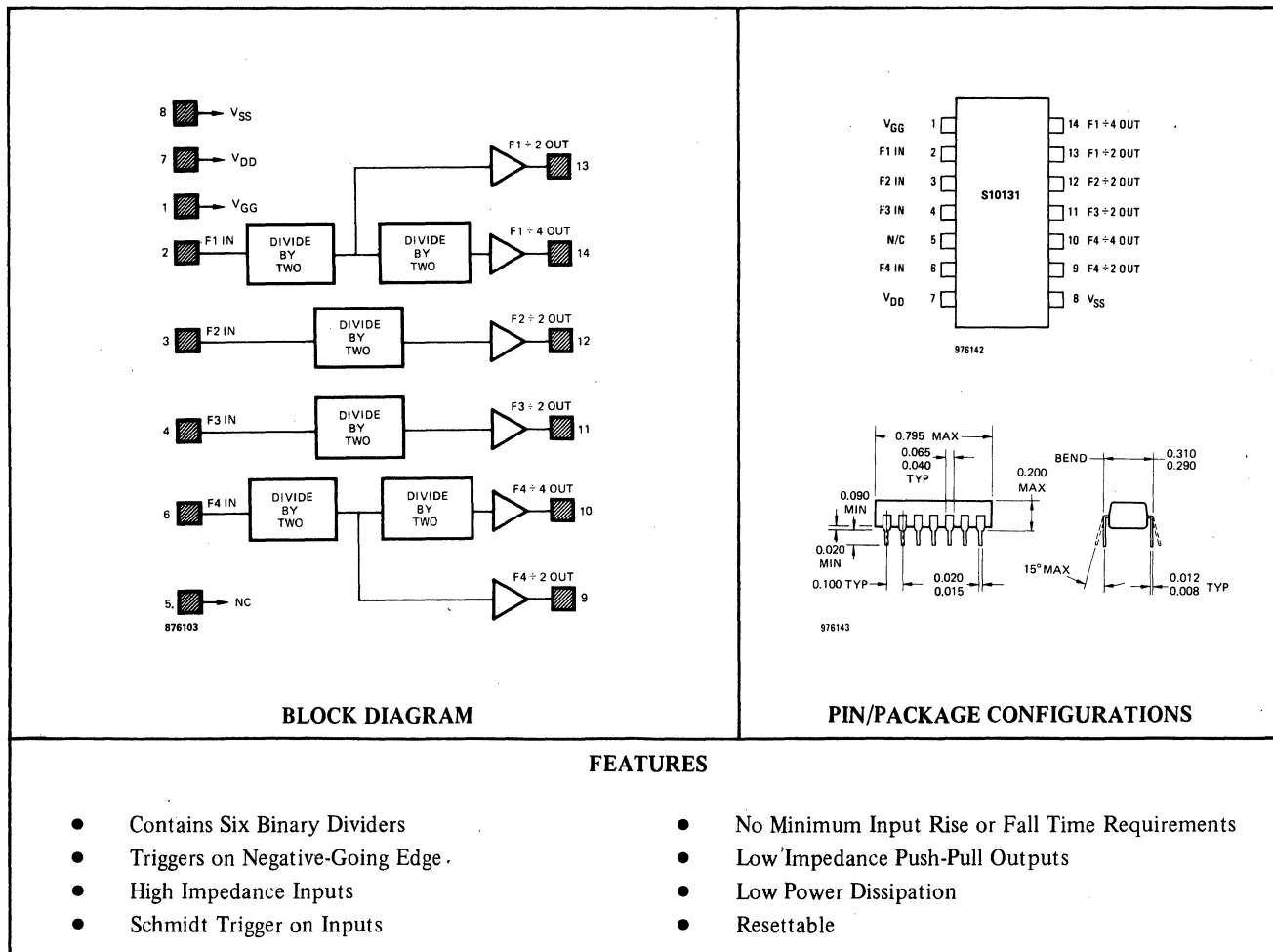
(0°C ≤ TA ≤ 70°C; VDD = - 11V to - 16V; VGG = - 25V to - 29V unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
VIL	Input Clock Low	VSS + 0.3		VSS - 2.0	Volts	
VIH	Input Clock High	VSS - 8		VGG	Volts	
fIN	Input Clock Frequency	DC		250	kHz	
TH, TL	Input Clock on & off times	1.5			μs	
VR	Voltage applied to VGG input to cause a reset condition	VSS		VSS - 0.5	Volts	
TR	Duration of VR to cause reset	10			μs	50% to 50% point
VOH	Output high level	- 11		VDD	Volts	VDD = - 12V VGG = - 26V 5.5KΩ load to VSS
VOL	Output low level	VSS		- 1	Volts	VDD = - 12V VGG = - 26V 5.5KΩ load to VDD
CIN	Input Capacitance		5	10	pF	Applies only to clock inputs
TOR, TOF	Output rise and fall time		1	2	μs	40 pF load applied
IGG	VGG supply current		2	3	mA	VDD = - 12V VGG = - 26V No load
IDD	VDD supply current		5	7	mA	VDD = - 12V VGG = - 26V No load



**TIMING CHARACTERISTICS**

### ADVANCED PRODUCT DESCRIPTION



### FUNCTIONAL DESCRIPTION

The S10131 is a monolithic frequency divider circuit fabricated with P-Channel ion-implanted MOS technology. The circuit provides six stages of binary division in a 2 - 2 - 1 - 1 configuration; the S10131 is ideally suited for tone generation in electronic organs.

All inputs to the device are buffered to permit easy triggering of the divider stages. Outputs of each divider are buffered to provide low output impedance in both logic states to drive external circuitry as well as other dividers. The buffers have low standby current and are powered by VDD. This voltage functions as a clamp voltage and thus sets the output

amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

All divider outputs may be reset to a logic low level (VSS) by momentarily applying a logic low level to the VGG supply input. This is particularly desirable in some electronic organs in which phase relationships are important.

### APPLICATIONS

Electronic organ frequency generator, organ pedal frequency generator, electronic music synthesizers, N stage dividers, low frequency generation, binary counters.

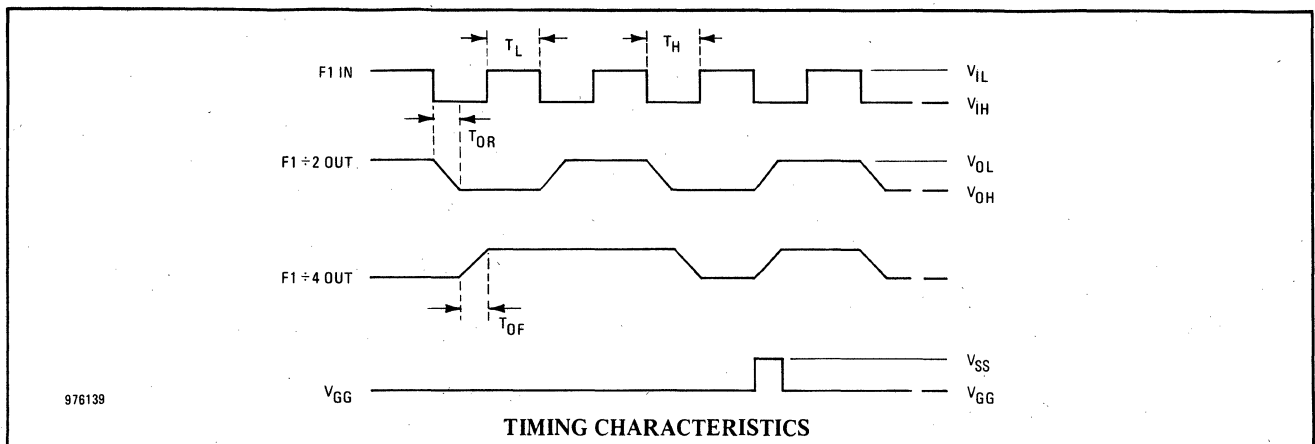
**ABSOLUTE MAXIMUM RATINGS**

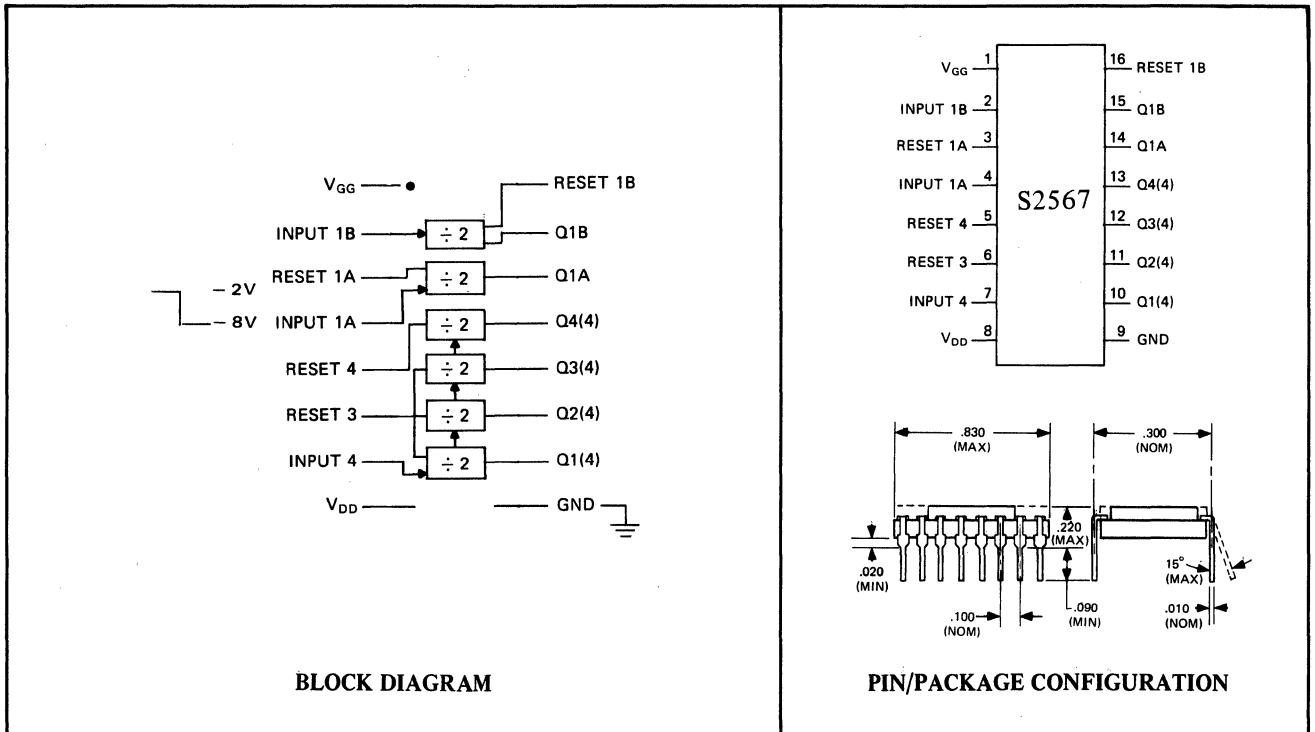
Voltage on any pin relative to V <sub>SS</sub>	+ 0.3V to - 20V	Storage temperature	- 55°C to + 150°C
Voltage on V <sub>GG</sub> relative to V <sub>SS</sub>	+ 0.3V to - 30V	Operating temperature (ambient)	0°C to 70°C

**ELECTRICAL CHARACTERISTICS**

(0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>DD</sub> = - 11V to - 16V; V<sub>GG</sub> = - 25V to - 29V unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V <sub>IL</sub>	Input Clock Low	V <sub>SS</sub> + 0.3		V <sub>SS</sub> - 2.0	Volts	
V <sub>IH</sub>	Input Clock High	V <sub>SS</sub> - 8		V <sub>GG</sub>	Volts	
f <sub>IN</sub>	Input Clock Frequency	DC		250	kHz	
T <sub>H</sub> , T <sub>L</sub>	Input Clock on & off times	1.5			μs	
V <sub>R</sub>	Voltage applied to V <sub>GG</sub> input to cause a reset condition	V <sub>SS</sub>		V <sub>SS</sub> - 0.5	Volts	
T <sub>R</sub>	Duration of V <sub>R</sub> to cause reset	10			μs	50% to 50% point
V <sub>OH</sub>	Output high level	- 11		V <sub>DD</sub>	Volts	V <sub>DD</sub> = - 12V V <sub>GG</sub> = - 26V 5.5KΩ load to V <sub>SS</sub>
V <sub>OL</sub>	Output low level	V <sub>SS</sub>		- 1	Volts	V <sub>DD</sub> = - 12V V <sub>GG</sub> = - 26V 5.5KΩ load to V <sub>DD</sub>
C <sub>IN</sub>	Input Capacitance		5	10	pF	Applies only to clock inputs
T <sub>OR</sub> , T <sub>OF</sub>	Output rise and fall time		1	2	μs	40 pF load applied
I <sub>GG</sub>	V <sub>GG</sub> supply current		2	3	mA	V <sub>DD</sub> = - 12V V <sub>GG</sub> = - 26V No load
I <sub>DD</sub>	V <sub>DD</sub> supply current		5	7	mA	V <sub>DD</sub> = - 12V V <sub>GG</sub> = - 26V No load





### FEATURES

- Pin for pin Equivalent to GEM567 and MC1181L
- Organ Rhythm Sections
- Portable Rhythm Sections
- Automatic Rhythm Organs

### FUNCTIONAL DESCRIPTION

The S2567 RESETTABLE RHYTHM COUNTER is a six-stage asynchronous binary counter designed for driving the count-address inputs of the S2566 RHYTHM GENERATOR. The internal partitioning and multiple-reset capability of the S2567

permit simultaneous generation of different meter rhythms. In more elaborate applications, where several S2567 Resettable Rhythm Counter is made by P-channel enhancement mode technology and appears in a 16 lead dual in-line package.

**ABSOLUTE MAXIMUM RATINGS (@ 25°C, unless noted)**

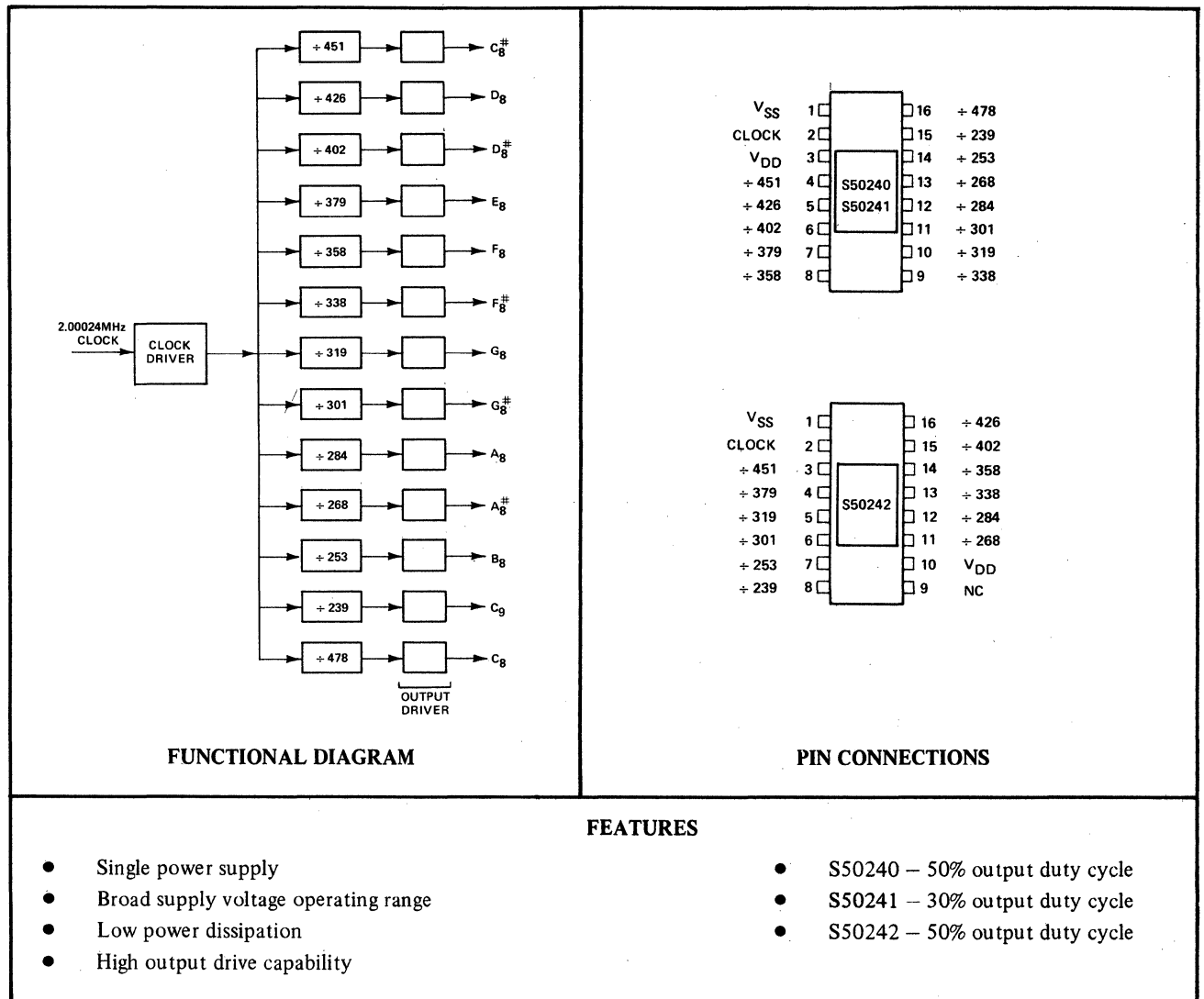
	SYMBOL	MIN.	MAX.	UNITS
Logic Supply Voltages	$V_{GG}$	+0.3	-33	Volts
	$V_{DD}$	+0.3	-25	Volts
Trigger Voltage	$V_I$	+0.3	-18	Volts
Power Dissipation	$P_D$		250	mW
Storage Temperature	$T_S$	-55	+100	°C
Operating Temperature	$T_A$	0	+60	°C

**DYNAMIC CHARACTERISTICS**  
 (T = 25°C)

	SYMBOL	MIN.	TYP	MAX	UNITS
Operating Voltage Ranges	$V_{GG}$	-25	-27	-29	Volts
	$V_{DD}$	-14	-15	-16	Volts
Inputs: (pins 2 thru 7, and 16)					
Input Frequency	$f_I$	DC		100	kHz
Logic "0" Level	$V_{IH}$	+0.3		-2.0	Volts
Logic "1" Level	$V_{IL}$	-8.0		-18	Volts
Rise and Fall Times	$t_r, t_f$			25	$\mu s$
Pulse Width	$PW_I$	2			$\mu s$
Leakage Current ( $V_{ILT} = -18V$ )	$I_{IL}$			1	$\mu A$
Outputs: (pins 10 thru 15, each loaded 20K to gnd and 20K to $V_{DD}$ )					
Logic "0" Level	$V_{OH}$	0		-1.5	Volts
Logic "1" Level	$V_{OL}$	-9.0		$V_{DD}$	Volts
Reset Propagation Delay				2.0	$\mu A$
Supply Currents: (no output loads)	$I_{GG}$		4	6	mA
	$I_{DD}$			20	$\mu A$



### ADVANCED PRODUCT DESCRIPTION



### FUNCTIONAL DESCRIPTION

The S5024 is one of a family of ion-implanted, P-channel MOS, synchronous frequency dividers.

Each output frequency is related to the others by a multiple  $12\sqrt{2}$  providing a full octave plus one note on the equal tempered scale.

Low threshold voltage enhancement-mode, as well as depletion mode devices, are fabricated on the same chip allowing the S5024 family to operate from a single, wide tolerance

supply. Depletion-mode technology also allows the entire circuit to operate on less than 360 mW of power. The circuits are packaged in 16 pin plastic dual-in-line packages.

RFI emanation and feed-through are minimized by placing the input clock between the  $V_{DD}$  and  $V_{SS}$  pins. Internally the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise time under no load conditions to reduce the R. F. harmonic content of each output signal.

**ABSOLUTE MAXIMUM RATINGS**

Voltage on any pin relative to VSS	+0.3 V to - 20V	Storage Temperature (Ambient)	- 65°C to + 150°C
Operating Temperature (Ambient)	0°C to 50°C		

**RECOMMENDED OPERATING CONDITIONS**

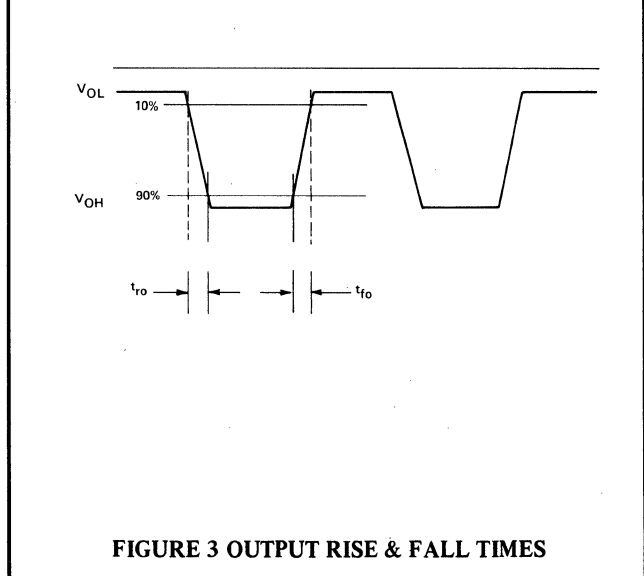
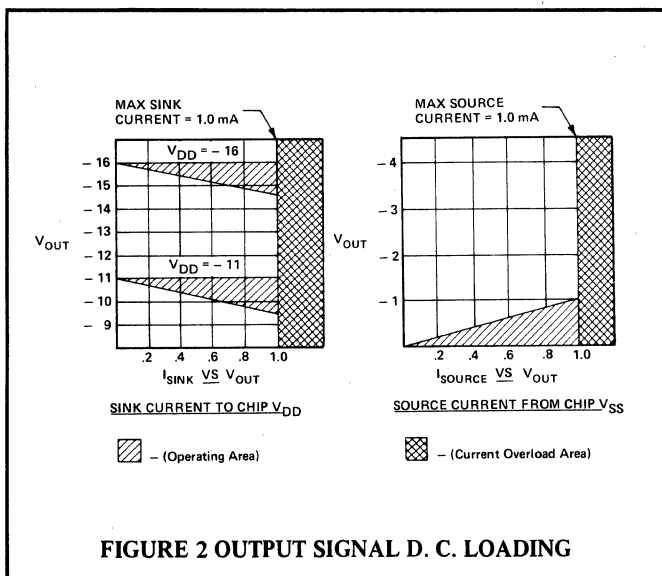
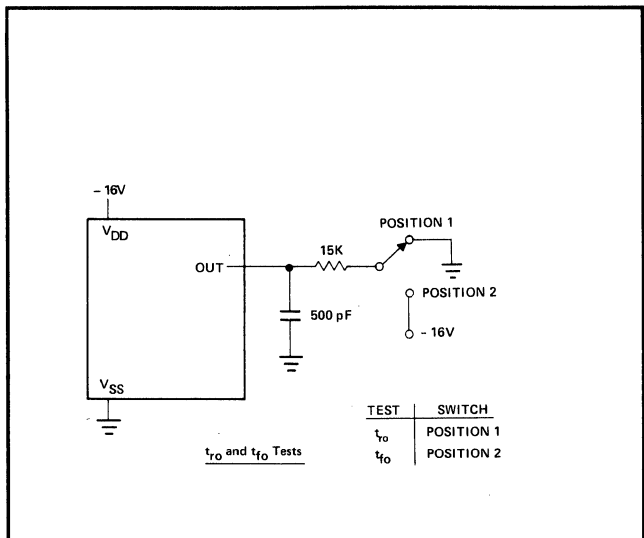
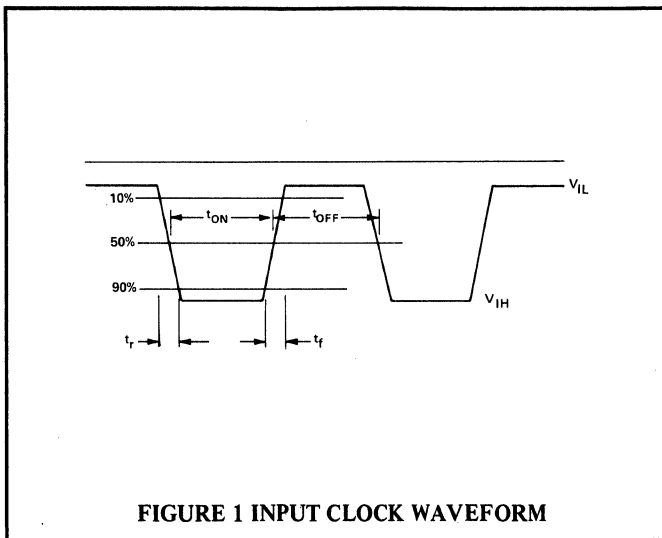
(0°C ≤ T<sub>A</sub> ≤ 50°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	FIGURE
V <sub>SS</sub>	Supply Voltage	0		0	V	
V <sub>DD</sub>	Supply Voltage	- 11.0	- 14.0	- 16.0	V	

**ELECTRICAL CHARACTERISTICS**

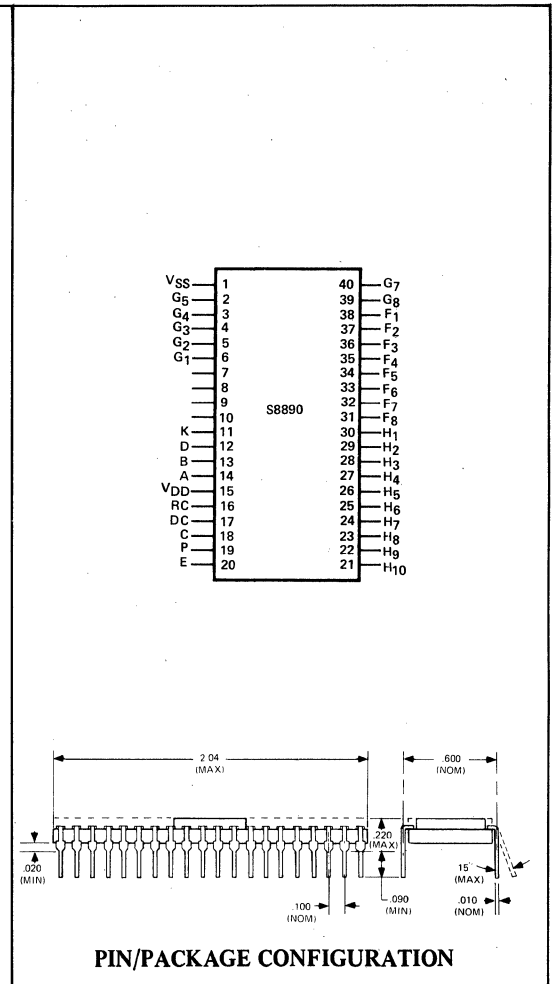
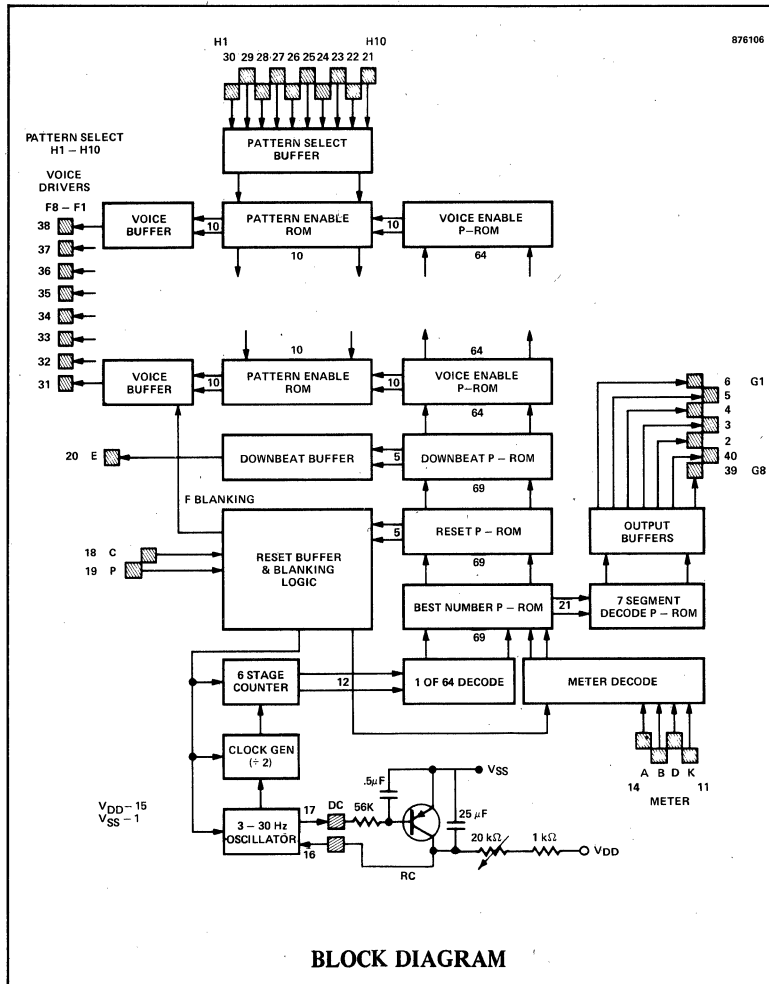
(0°C ≤ T<sub>A</sub> ≤ 50°C; V<sub>DD</sub> = - 11 to - 16V unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	FIGURE
V <sub>IL</sub>	Input Clock, Low	0		- 1.0	V	Figure 1
V <sub>IH</sub>	Input Clock, High	- 10.0		V <sub>DD</sub>	V	Figure 1
f <sub>1</sub>	Input Clock Frequency	100	2000.240	2500	kHz	
t <sub>r</sub> , t <sub>f</sub>	Input Clock Rise & Fall Times 10% to 90% @ 2.5MHz			50	nsec	Figure 1
t <sub>ON</sub> , t <sub>OFF</sub>	Input Clock On and Off Times @ 2.5MHz		200		nsec	Figure 1
C <sub>I</sub>	Input Capacitance		5	10	pF	
V <sub>OH</sub>	Output, High @ 1.0 mA	V <sub>DD</sub> + 1.5		V <sub>DD</sub>	V	Figure 2
V <sub>OL</sub>	Output, Low @ 1.0 mA	V <sub>SS</sub> -1.0		V <sub>SS</sub>	V	Figure 2
t <sub>ro</sub> , t <sub>fo</sub>	Output Rise & Fall Times, 500 pF Load 10% to 90%	250		2500	nsec	Figure 3
t <sub>ON</sub>	Output Duty Cycle- S50240, S50242 S50241		50 30		% %	
I <sub>DD</sub>	Supply Current		14	22	mA	Outputs Unloaded



# S8890

## RHYTHM GENERATOR



### FEATURES

- Drives 9 Instruments
- 64 Bit Pattern
- 10 Rhythm Patterns per Instrument
- 5 Mask Programmable Reset Counts
- 7 Segment Count Display Output
- Internal Oscillator

### TYPICAL APPLICATIONS

- Organ Rhythm Sections
- Portable Rhythm Sections
- Automatic Rhythm Organs
- Music Synthesizer

### FUNCTIONAL DESCRIPTION

The rhythm generator is a counter-ROM specifically designed for electronic organ and other electronic instruments. This product contains an internal oscillator, a 6 bit counter, and a ROM that drives nine rhythm instruments and also drives a seven segment sequence count display.

The oscillator frequency is determined by an external network. The 6 bit counter has control inputs that allow the counter to reset at any one of five counts. Five reset counts are mask programmed to user requirements. The 64th count is normally programmed as the 5th reset selection option. The

counter contains a start input that holds the system in the reset mode until a start command is impressed.

The counter outputs drive a 64 word ROM. The ROM has two types of rhythm instrument outputs and a rhythm count output. The rhythm instrument outputs provide a trigger with up to 64 counts. One of the instrument outputs contains only one rhythm pattern for each reset option. This output can be programmed to generate a downbeat trigger at the beginning of each measure. The remaining eight instrument outputs each contain 10 rhythm patterns which may be simultaneously selected to overlay multiple rhythm patterns.

The rhythm count outputs provide a seven segment code that can be used as a visual display of the musical timing. For example, if 4/4 timing is provided by the programmable option, and the appropriate control lined ( $I_R$ ) are activated then the seven segment display will provide the pattern in Figure 2. Four numbers (1, 2, 3 or 4) will be displayed, one for each group of four quarter notes in a 16 note measure. The pattern will repeat for subsequent measures. Other sequences can be programmed for alternate timing schemes.

Internal input pull-up resistors to  $V_{DD}$  are provided on all inputs except the oscillator input. Output buffers consist of a single ended device to  $V_{SS}$ . The product is fabricated with  $I^2T^M$  technology and is packaged in a 40 lead dual in-line package.

## FUNCTIONAL DESCRIPTION OF INPUT/OUTPUT PINS

### DUMP CHARGE:

Provides base current when required through an RC delay of approximately 25 msec to a PNP transistor which should be connected across the capacitor in the oscillator.

Input	Rhythm	Bits/Beat
A	3/4	3
B	5/4	4
D	6/8	4
K	3/4	4
Default	4/4	4

The chip input functions are as follows.

### METER:

$V_{SS}$  applied to the following inputs sets up the chip with a programmable number of bits per beat, beats per measure and measures before reset. A currently programmed example follows.

Beats/Measure	Measure/Reset	Bits/Reset
3	4	36
5	2	40
6	2	48
3	4	48
4	4	64

### RESET:

#### C Input

When allowed to approach  $V_{DD}$ , the outputs are held disabled and the system is held ready to begin with the first bit of the First measure. The system starts when  $V_{SS}$  is applied.

### PATTERN SELECT:

#### H1 – H10 Inputs

$V_{SS}$  applied to one enables one combination of the voices in a specific rhythm pattern. Any combination of patterns may be enabled at the same time. The customer must provide the voice pattern as a function of each pattern selected and of each bit time.

### OUTPUT DUTY CYCLE:

#### P Input

When allowed to approach  $V_{DD}$ , the voice inputs are held off for one half of each bit time. When held at  $V_{SS}$ , the voice outputs are constantly valid. Note that neither option hides the short ( $<80 \mu\text{sec}$ ) decode spikes.

The chip output functions are as follows.

### VOICE DRIVERS:

#### F1 – F8

When selected, internally, the outputs provide a low resistance path to  $V_{SS}$  which is suitable for driving a transistor interface.

### BEAT NUMBER DISPLAY:

#### G1 – G8 (less 6)

When selected, internally, the outputs provide a low resistance path to  $V_{SS}$  suitable for sinking the current required to drive a GE7 segment display tube. The ROM driving these outputs must be programmed to match the meter program.

### DOWNBEAT:

#### $\bar{E}$

When selected internally, the output provides a low resistance path to  $V_{SS}$ .

The Oscillator Interconnects are as follows.

### RC PAD:

A 25  $\mu\text{F}$  capacitor to  $V_{SS}$  and a series combination of a 20  $\text{K}\Omega$  potentiometer and a 1  $\text{K}\Omega$  resistor to  $V_{DD}$  will allow a range of about 1.5 to 15 bits/second.

$\text{TM}I^2$  is a registered trademark of AMI's Ion Implant process.

**P-ROM PROGRAMMING FORMATS**

Programming the Rhythm Generator requires 132 IBM cards punched with the data outlined below. Each card should end with CXXXX - NNN where XXXX is a number provided by AMI and NNN is the card number.

**DOWNBEAT ROM:**

Columns	Contents
1 - 64	Enter '1' for the first bit of each measure of the given meter. (No gate = '1')
72 - 80	CXXXX - NNN per above.
Card	Meter
001	N
002	K
003	D
004	B
005	A

**RESET ROM:**

Columns	Contents
1 - 64	Enter '1' for the last bit before a reset and for all subsequent bits. (No gate = '1')
72 - 80	CXXXX - NNN per above.
Card	Meter
006	N (Meter N must not have a reset before 64)
007	K
008	D
009	B
010	A

NOTE: '1' always means an activated output and, thus, may represent a gate or a lack of one.

**BEAT NUMBER ROM:**

Card	Column	Content
A	1 - 50	Enter '1' for each bit where the NUMBER should be on. (No gate = '1'). Enter the first 50 bits on Card A, last 14 bits on Card B.
B	1 - 14	Meter bit pattern
B	16 - 20	7 Segment Display Pattern
A&B	72 - 80	CXXXX - NNN per above.

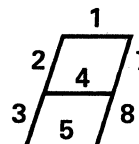
Enter the beat number data on adjacent cards starting with 011 for A and 012 for B and ending on or before 052.

Order data by Meter bit patterns as follows:

first	N	'00001'
first	K	'00010'
first	D	'00100'
first	B	'01000'
last	A	'10000'
unused		00000

Group beat numbers in order within each meter using the following decode for numerical compatibility with GE7 Segment tubes.

Segments to be activated (Gate = '1')	Beat Number to be displayed							
	1	2	3	4	5	6	7	None
G1 col. 22	0	1	1	0	1	1	1	0
G2 col. 23	0	0	0	1	1	1	0	0
G3 col. 24	0	1	0	0	0	1	0	0
G4 col. 25	0	1	1	1	1	1	0	0
G5 col. 26	0	1	1	0	1	1	0	0
G7 col. 27	1	0	1	1	1	1	1	0
G8 col. 28	1	1	1	1	0	0	1	0



**VOICE ENABLE ROM:**

Column	Contents
1 - 64	Enter a '1' for each bit where the selected H should turn on the selected F. (No gate = '1')
67 - 68	Voice (f) number (2 digit)
72 - 80	CXXXX - NNN per above.

Card	Input	Outputs
053 - 060	H1	F1 through F8 in order
061 - 068	H2	F1 through F8 in order
069 - 076	H3	F1 through F8 in order
077 - 084	H4	F1 through F8 in order
085 - 092	H5	F1 through F8 in order
093 - 100	H6	F1 through F8 in order
101 - 108	H7	F1 through F8 in order
109 - 116	H8	F1 through F8 in order
117 - 124	H9	F1 through F8 in order
125 - 132	H10	F1 through F8 in order

### ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin	$V_{SS} + 0.3V$
Negative Voltage on any Pin	$V_{SS} - 28V$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Ambient Temperature	$0^{\circ}C$ to $+70^{\circ}C$

### STATIC CHARACTERISTICS

( $V_{DD} = -12.1 \pm 5\%$ ,  $V_{SS} = GRD$ ,  $T = 0^{\circ}$  to  $+70^{\circ}C$ )

Symbol	Parameters	Min	Typ	Max	Units	Conditions
$V_{IH}$	Input high level	$V_{SS} - 0.7$			Volts	Internal
$V_{IL}$	Input low level			$V_{DD} + 2.0$	Volts	Resistor to $V_{DD}$
$V_{OH}$	Output high level	$V_{SS} - 2.0$			Volts	$I_O = 2$ mA
$V_{OL}$	Output low level			$V_{DD} + 1.0$	Volts	External $30$ K $\Omega$ to $V_{DD}$
$I_{DC}$	Dump charge output current	1.0			mA	
$V_{RC}$	Discharge enable voltage		$V_{SS} - 7.0$		Volts	

### APPLICATION DATA

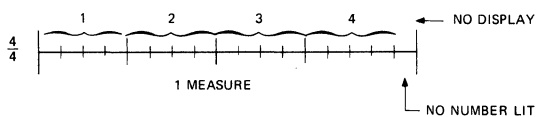


FIGURE 1. BEAT NUMBER DISPLAY ROM

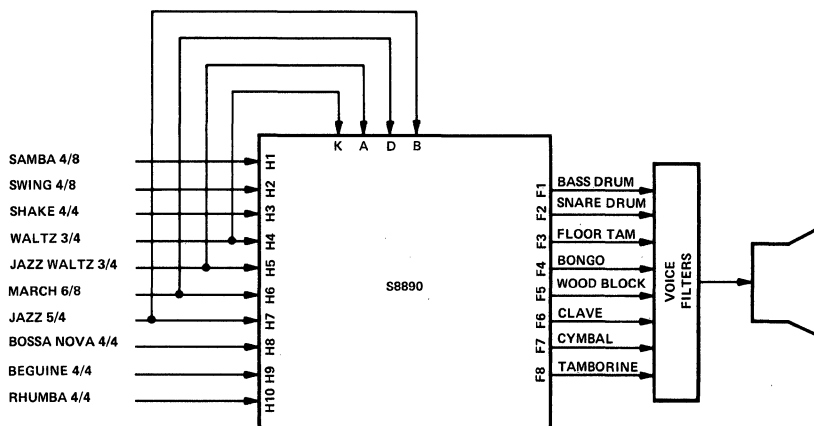


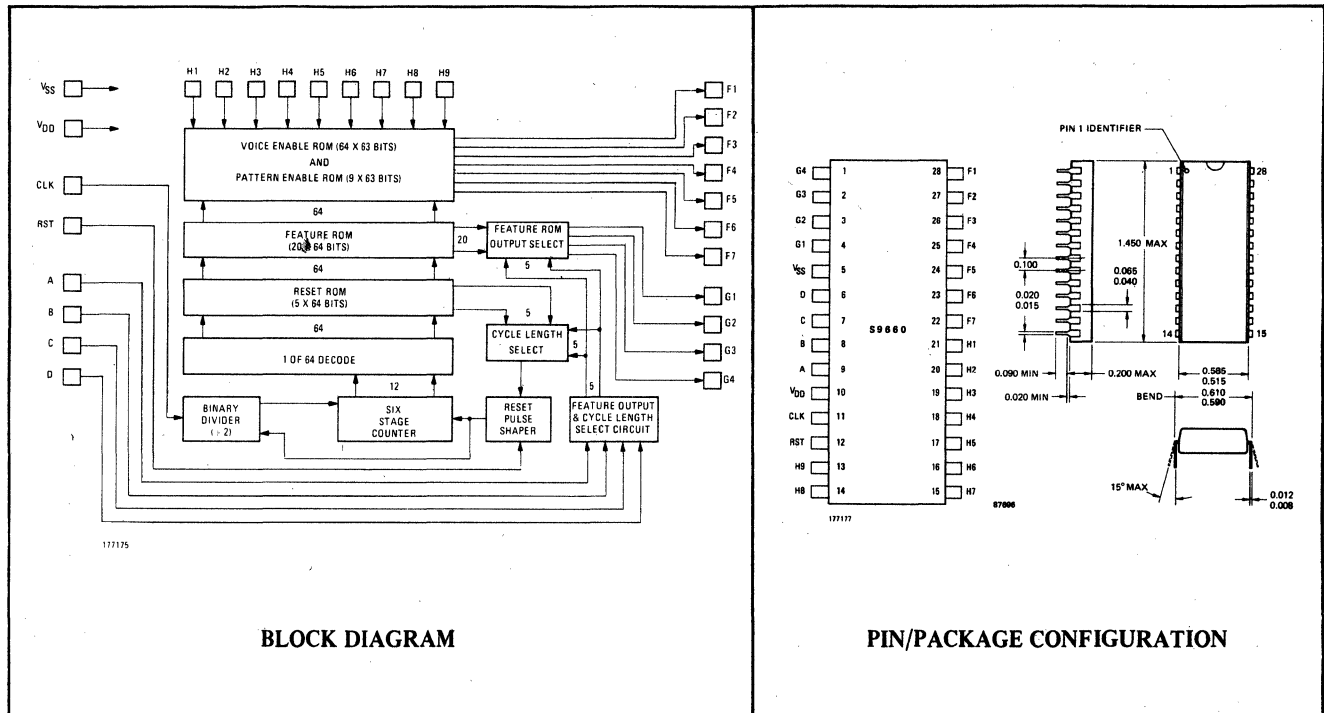
FIGURE 2. TYPICAL RHYTHM UNIT BLOCK DIAGRAM

# S9660

RHYTHM GENERATOR

# AMI

AMERICAN MICROSYSTEMS, INC.



BLOCK DIAGRAM

PIN/PACKAGE CONFIGURATION

## FEATURES

- Drives 7 Instruments
- 64 Bit Patterns
- 9 Rhythm Patterns
- 4 Feature Outputs
- 5 Programmable Feature Selections
- All Rhythm Patterns Additive
- 5 Programmable Resets
- All Counters and Decoders Internal
- All Patterns User Programmable

## FUNCTIONAL DESCRIPTION

The S9660 rhythm generator is a counter-ROM specifically designed for use in rhythm sections of electronic organs and independent electronic rhythm units. This product contains a six stage counter, all internal ROM decoding, a 4K bit pattern ROM, and a 1K bit feature ROM. A total of nine distinct 64-bit rhythm patterns are generated and may be used to control up to seven rhythm instruments. In addition, the feature ROM provides four outputs that may be used for automatic chord gating, walking bass, or to create rhythm pattern variation.

The 6-bit counter may be reset at any bit from 1 through 64 to obtain any desired counter cycle. This counter cycle

control is determined by the user's individually programmed ROM pattern, which allows the electrical selection of up to five different counter cycle lengths in one S9660.

The counter outputs drive a 64 x 63 bit rhythm pattern ROM and a 64 x 20 bit feature ROM. The rhythm pattern ROM drives seven instrument outputs and generates nine rhythm patterns which may be simultaneously selected to overlay multiple rhythm patterns. The feature ROM drives four outputs; depending on which of the five reset conditions is selected, the four outputs each contain five distinct 64 bit patterns. These may be used to drive such features as walking bass, automatic chording, or rhythm variation.



Internal input pull-up resistors to  $V_{DD}$  are provided on all inputs, and output buffers consist of open drain devices with source connected to  $V_{SS}$ . The product is fabricated with P-channel ion implanted MOS technology and is packaged in a 28 lead dual in-line plastic package.

### TYPICAL APPLICATIONS

Organ Rhythm Sections, Portable Rhythm Units, Automatic Chording Systems, Walking Bass.

### OPERATIONAL DESCRIPTION

A block diagram of the S9660 appears in Figure 1, along with a typical timing diagram in Figure 2. All rhythm patterns, feature patterns, and counter cycle lengths are user programmable.

#### CLK Input (pin 11):

A clock frequency from an external oscillator is supplied to this pin to provide the timing information to the 6 bit rhythm counter. As this frequency is varied, the speed, or tempo, of the generated rhythm is varied.

As indicated in the block diagram, the CLK input is divided by two and then applied to the 6 stage counter. This means that each of the output bit periods is equal to two input clock periods. For example, if the rhythm counter is programmed to recycle every 48 bits, and the cycle is divided into two measures of 4 beats each, then each beat contains 6 bits; if the CLK input frequency is 30 Hz, then, rhythm timing will be 15 bits per second, or 900 bits per minute, or 150 beats per minute.

#### H Inputs (pins 13 through 21):

Normally pulled to  $V_{DD}$ , application of a  $V_{SS}$  level to any of the 9 H inputs enables one combination of voices that comprise a specific rhythm pattern. Any combination of patterns may be enabled simultaneously by applying  $V_{SS}$  to other H inputs. The user must provide the desired voice pattern as a function of each H pattern selected and of each bit time. This is programmed in the Voice Enable ROM.

#### RST Input (pin 12):

Normally pulled to  $V_{DD}$ , application of a  $V_{SS}$  level to the RST input enables the rhythm counter. When RST is left unconnected, the binary divider ( $\div 2$ ) and the

rhythm counter chain are reset to count one, and all "F" outputs are held in an off condition. When  $V_{SS}$  is applied, the bit pattern selected for the first address of the ROM (count one) will activate the appropriate "F" outputs. Subsequent clock pulses at the CLK input will cause the counter to advance its count as indicated in the timing diagram.

#### A, B, C, D Inputs (pins 9, 8, 7, and 6):

These inputs control two functions, the selection of cycle length (or counter reset bit) and the bit patterns of the four G outputs. Normally pulled to  $V_{DD}$ , these outputs may be selected (only one at a time) by applying  $V_{SS}$ . A fifth condition called "default," or "N," occurs when none of the four A, B, C, or D inputs is selected.

Up to five reset bits (or counter lengths) may be programmed so that five different counter lengths may be selected by use of A, B, C, or D. These resets are programmed by the Reset ROM. This allows a 4/4 rhythm to contain 64 bits and a 3/4 rhythm to contain 48 bits, for example, so that when switching from a swing beat to a jazz waltz it is not necessary for the player to adjust the tempo control.

For each of the five A, B, C, D, or Default conditions there is a unique pattern supplied on the four G outputs. This information is programmed into the Feature ROM.

#### F Outputs (pins 22 through 28):

When selected internally by the Voice Enable ROM, these seven open drain outputs provide a low resistance path to  $V_{SS}$ . These outputs are suitable for driving a transistor interface to electronic rhythm voice generators. Decode spikes may appear at the F outputs, though they are of short enough duration ( $< 80 \mu s$ ) that most instrument voice generators would be unaffected.

#### G Outputs (pins 1, 2, 3, and 4):

When selected internally by the Feature ROM, the four open drain G outputs provide a low resistance path to  $V_{SS}$ . Five distinct patterns are available on each of the outputs and are selected by the A, B, C, D, inputs. The decode spikes mentioned in the "F" output paragraph may also be present in the "G" outputs.

**ABSOLUTE MAXIMUM RATINGS**

Positive voltage on any pin	V <sub>SS</sub> + 0.3 Volts	Storage temperature	- 65°C to + 150°C
Negative voltage on any pin	V <sub>SS</sub> - 28 Volts	Operating Ambient Temperature	0°C to + 70°C

**ELECTRICAL SPECIFICATIONS**

(0°C ≤ t<sub>a</sub> ≤ 70°C; - 10 Volts ≥ V<sub>DD</sub> ≥ - 14 Volts unless otherwise specified)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V <sub>IL</sub>	Input logic "0"	V <sub>DD</sub>	V <sub>DD</sub> + 2.0	Volts	See Note 1
V <sub>IH</sub>	Input logic "1"	V <sub>SS</sub> - 0.7	V <sub>SS</sub>	Volts	
V <sub>CLKL</sub>	Input logic "0" (CLK input)	V <sub>DD</sub>	V <sub>DD</sub> + 1.0	Volts	
V <sub>CLKH</sub>	Input logic "1" (CLK input)	V <sub>SS</sub> - 0.7	V <sub>SS</sub>	Volts	
t <sub>cr</sub> , t <sub>cf</sub>	CLK input rise and fall time		100	μs	Measured at 10% to 90% of V <sub>DD</sub>
f <sub>c</sub>	Clock frequency (CLK input)	DC	5K	Hz	
V <sub>OL</sub>	Output logic "0"				See Note 2
V <sub>OH</sub>	Output logic "1"	V <sub>SS</sub> - 2.0	V <sub>SS</sub>	Volts	V <sub>DD</sub> = - 12.0 Volts I <sub>out</sub> = 1 mA maximum
P	Average power dissipation		300	MW	Measured at 25°C

- NOTES:
1. Internal 5μA minimum pullup to V<sub>DD</sub> is provided.
  2. External load to V<sub>DD</sub> is required.

**PROGRAMMING INSTRUCTIONS**

Programming of the S9960 is a straightforward process requiring the user to supply a total of 110 cards. There are three ROM sections to be programmed, the Reset ROM, the Feature ROM, and the Voice Enable ROM. Detailed instructions for punching the cards required to program these three ROMs are supplied below. In column 72 - 80 of each card, as described below, two numbers appear - CXXXX and NNN. The CXXXX is a number to be given to the user by AMI prior to punching the card deck, and NNN is the sequence number of the card.

**RESET ROM:**

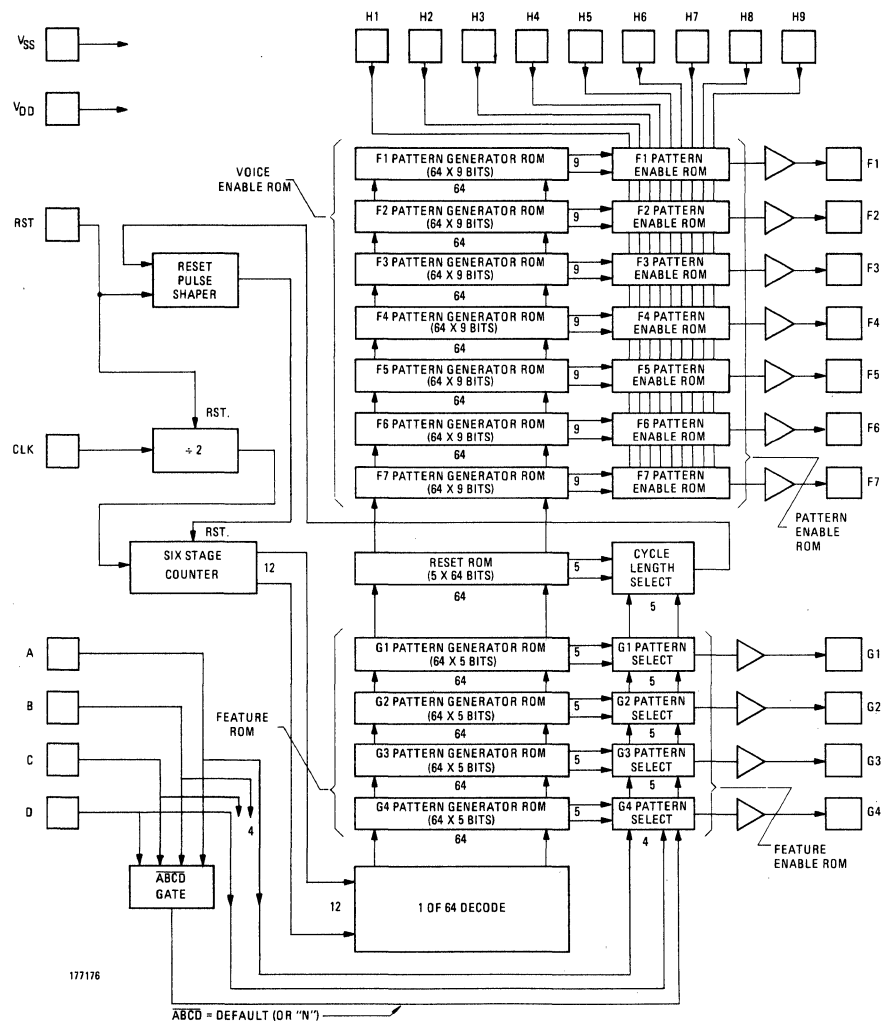
A total of five cards are required to program the reset ROM. Their card numbers are 001 through 005. Each card

determines at what bit the rhythm counter will reset (i.e., the number of bits per cycle) for one of the five electrically selected conditions, A, B, C, D, or N (N =  $\overline{ABCD}$ ). Card 001 corresponds to N, 002 to D, 003 to C, 004 to B, and 005 to A.

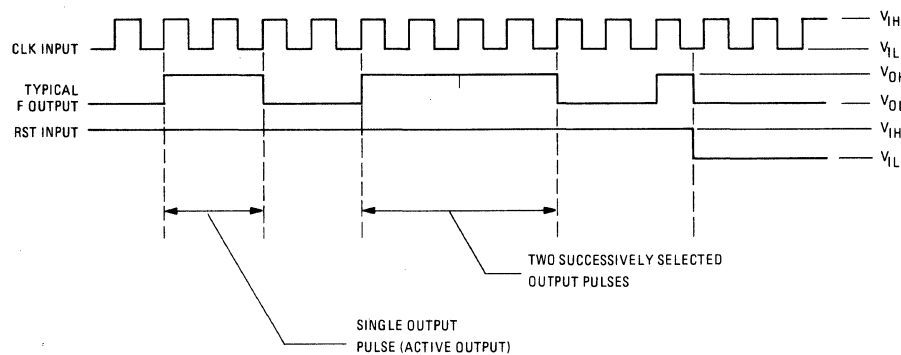
Columns	Contents
1 - 64	Enter a "1" for the last bit before an internal reset occurs and for all subsequent bits through 64.
72 - 76	CXXXX - To be assigned by AMI, as stated above.
78 - 80	Enter number of the card (001 through 005).

Example: If card 003 has all ones in columns 48 through 64, then whenever the C input is selected, the rhythm generator will reset at the end of bit 48, giving a 48 bit cycle length.

**FIGURE 1.  
DETAILED  
BLOCK DIAGRAM**



**FIGURE 2.  
TIMING DIAGRAM**



**FEATURE ROM:**

A total of 42 cards are required to program the feature ROM. The cards are grouped in pairs, and each pair determines the bit pattern that will appear on a given G output for a given A, B, C, D, or N input selection. The G1 output is programmed by cards 6 – 15, G2 by cards 16 – 25, G3 by cards 26 – 35, and G4 by cards 36 – 45. Cards 46 and 47 must be present, but they are not used to program any G outputs.

The five pairs of cards corresponding to each output are arranged so that the bit pattern programmed by the first pair will be selected by the A input, the second by B, and the third, fourth and fifth by C, D, and N, respectively. For example, if input C is selected, the bit pattern appearing at the G2 output would be that programmed by cards 20 and 21.

First card in pair (21 cards: 6, 8, 10, . . . , 44):

Column 1 – 50 – First 50 bits of 64; enter a “1” at the location of each bit where an active output is desired.

Second card in pair (21 cards: 7, 9, 11, . . . , 45):

Column 1 – 14 – Last 14 bits of 64; enter a “1” at the location of each bit where an active output is desired.

Card 46:

Columns 1 – 50 – Enter nothing.

Card 47:

Columns 1 – 14 – Enter nothing.

Column 16 – 20:

Cards 7, 17, 27, 37 – . . . . . Enter “10000.”

Cards 9, 19, 29, 39 – . . . . . Enter “01000.”

Cards 11, 21, 31, 41 – . . . . . Enter “00100.”

Cards 13, 23, 33, 43 – . . . . . Enter “00010.”

Cards 15, 25, 35, 45 – . . . . . Enter “00001.”

Card 47 – . . . . . Enter “00000.”

Column 22 – 28:

Cards 7, 9, 11, 13, 15 – . . . . . Enter “1000000.”

Cards 17, 19, 21, 23, 25 – . . . . . Enter “0100000.”

Cards 27, 29, 31, 33, 35 – . . . . . Enter “0010000.”

Cards 37, 39, 41, 43, 45 – . . . . . Enter “10001000.”

Column 72 – 76 (all cards) – . . . . . Enter CXXXX  
(as assigned by AMI).

Column 78 – 80 (all cards) – . . . . . Enter card number  
(006 through 047).

**VOICE ENABLE ROM:**

This ROM is programmed by a total of 63 cards, numbered 048 through 110. The cards are in nine groups (H1, H2, . . . , H9) of seven cards each (F1, F2, . . . , F7).

Card	Input	Outputs
048-054	H1	F1 through F7 in order
055-061	H2	F1 through F7 in order
062-068	H3	F1 through F7 in order
069-075	H4	F1 through F7 in order
076-082	H5	F1 through F7 in order
083-089	H6	F1 through F7 in order
090-096	H7	F1 through F7 in order
097-103	H8	F1 through F7 in order
104-110	H9	F1 through F7 in order

**Column**

- 1 – 64 Enter a “1” for each bit where the selected H should turn on the desired F output.
- 67 – 68 Voice number (F1, F2, F3, F4, F5, F6, or F7).
- 72 – 76 Enter CXXXX (as assigned by AMI).
- 78 – 80 Enter card number (046 through 110).

**CUSTOMIZING THE S9660:**

The S9660 has been designed to offer a wide variety of features for use in both low cost rhythm units and electronic organs. It is possible, however, in many circumstances to modify this part to fit particular applications.

A few examples of such modifications are the addition of an additional F output in place of an H pattern input and vice versa, the blanking of 50% of the output pulsewidth, and the addition of more G outputs. To minimize cost, this circuit may be supplied in a smaller package if some of the existing features are not needed.

These modifications may be readily accomplished by minor changes to the bonding of the circuit. To determine if a proposed feature set is feasible, consult AMI’s Application Department.

# 6

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## **Watch/Clock Circuits**

## Watches/Clocks Circuits

Part No.	Description	Power Supply (V)	Process	Packages
S1424A	Five-function (3½-digit) Watch	+1.5	CMOS	Die
S1424C	Five-function (3½-digit) Watch	+1.5	CMOS	Die
S1425A	Five-function (3½-digit) Watch	+1.5	CMOS	Chip Carrier
S1427A	Five-function (3½-digit) Watch	+1.5	CMOS	P
S1856	LED/Gas D. Auto Clock (3½ digits)	+6 to +16	P-I <sup>2</sup>	P
S1998A	50/60 Hz Line Clock (4 digits) - LED	+8 to +26	P-I <sup>2</sup>	P
S1998B	50/60 Hz Line Clk.—Gas Discharge	+8 to +33	P-I <sup>2</sup>	P
S1998C	50/60 Hz Line Clk.—Fluorescent	+8 to +26	P-I <sup>2</sup>	P

## Future Products

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### LCD WATCH CIRCUITS

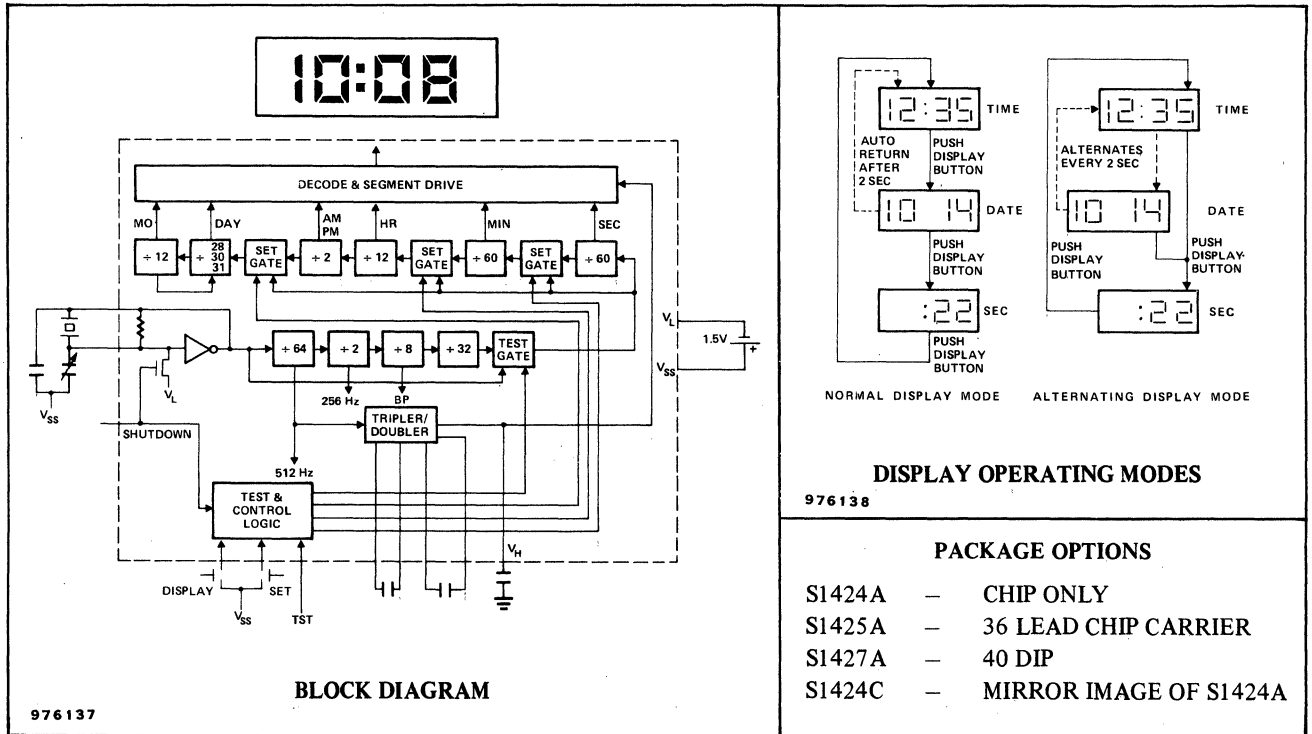
- (S2733) — 4-digit, 6-function
- 6-digit, 7-function
- 6-digit, multi-function

### CLOCK RADIO CIRCUIT

High feature circuit for use with LED, fluorescent and gas discharge displays

### AUTO CLOCK CIRCUIT (S2709)

12V Auto Clock Circuit for use with fluorescent display  
(4m Hz crystal input)



### FEATURES

- Drives Standard 3½ Digit Display
- 12 Month Calendar Memory
- One Push Button Controls Display
- Uses Single 1.5V Battery
- Displays Time, Month-Date, or Seconds
- Additional Alternating Time/Date Display Mode
- Voltage Doubler or Tripler LCD Drive Options

### FUNCTIONAL DESCRIPTION

The AMI S1424A/S1425A/S1427A/S1424C is a single chip, silicon gate CMOS watch circuit designed to drive a 3½ digit, field effect, liquid crystal display. Hour and minutes or seconds can be displayed continuously. Month and date are displayed on interrogation. A continuous display alternating

between time and date is also selectable (see operating modes above).

Only two single pole single throw switches are required to accomplish all display and setting functions. The circuit provides a full calendar function which needs to be reset only once every four years.

Display Operation is illustrated on page one. Operation in either the normal or alternating display mode is selected by the Set button during setting of the watch. When operating in the normal mode, the display initially shows hours and minutes. The absence of a colon distinguishes the Month-Date display from the Hour-Minute and Seconds display. The Seconds display is obvious as only the last two digits are used and the display is incrementing once per second.

All display and setting operations are controlled by two inputs, the Display input and the Set input. In Normal Operation only the Display input is used. Both inputs have an internal pulldown to  $-V_L$  so that a single pole, single throw contact may be used.

### DATE DISPLAY

The date is displayed in the normal operating mode by pushing the display button until the readout changes to Month-Date (1/2 sec. max.). The circuit will readout Month-Date for 2 to 3 seconds and return to Hours-Minutes automatically. If readout of Month-Date in excess of 2 seconds is desired, the display button is held in the depressed condition for the required time period. Upon release of the display button, the readout will return to Hour-Minute.

### TESTING

A test input (TST) is furnished to facilitate high speed testing of the circuit. An internal pulldown to  $V_L$  allows this pin to float during normal operation.

### SECONDS DISPLAY

In the normal operating mode the display button is pushed twice within two seconds to change from an Hour-Minutes readout to Seconds. The first press of the display button changes the readout to Month-Date. Pressing the display button again while Month-Date is being displayed causes the readout to change from Month-Date to Seconds. Once Seconds appears, the display button is released and Seconds will be shown continuously. Pressing the display button a third time will return the readout to Hours-Minutes. This scheme allows all information to be viewed using one push button input and Seconds to be viewed without continually pressing a button. Seconds display in the alternating display mode is described below.

### ALTERNATING TIME/DATE DISPLAY

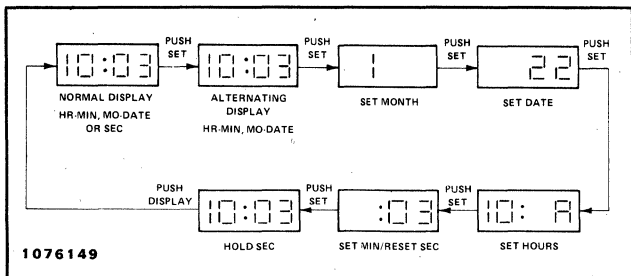
In the alternating display mode, the watch will alternately display Hours-Minutes then Month-Date for two seconds intervals. Pushing the display button will call up seconds. Another push restores the alternating Time/Date display.

### SHUTDOWN

A shutdown input (SD) is provided to reduce power consumption of the watch module during storage. When this input is connected to  $V_{SS}$  the oscillator is stopped and all other node voltages within the CMOS chip are held constant.

### SETTING OPERATION

Five setting states and two normal operating states are included in the setting sequence. Each state is uniquely identified by the display as shown below. Hours, minutes, and seconds are distinguished from month and date by the colon. In the hours set mode the fourth digit is either an A or P to indicate AM or PM.



Only the set input is required to select the desired setting state. Connecting the Set input repeatedly to  $V_{SS}$  causes the circuit to advance through its set and run states at the rate of one state per Set switch closure. When the display is in the desired setting state the display button is used to set the displayed quantity. Connecting the display input to  $V_{SS}$  causes the selected quantity (month, date, hours or minutes) to be advanced at the rate of one unit per second. In all setting states, timekeeping is not interrupted nor is any counter advanced until the display button is depressed. In all setting states except minutes, only the quantity being displayed can be changed and that change cannot happen until the display button is depressed. In the set minutes state, seconds are reset to zero and held when minutes are advanced. After minutes are set and the display is returned to the run mode, the colon is held on. Seconds counting is resumed from zero by pressing the display button.



## SETTING OPERATION

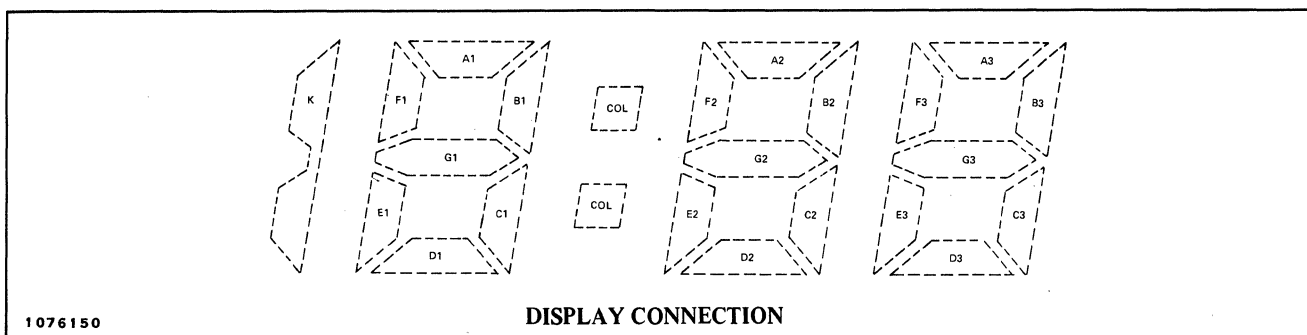
### Detailed Procedure

To set the watch, use the following procedure (it is assumed the watch is in the Normal Operating state):

1. Depress the Set button. Circuit will advance to the alternating Time/Date operating mode.
2. Depress the Set button until the display shows Month (shown in left most digits). Release the Set button.
3. Depress the Display button to advance Month to the proper value. Release the Display button.
4. Depress the Set button until the display shows Date (in right most digits). Release the Set button.
5. Depress the Display button to advance Date to the proper value. Release the Display button.
6. Depress the Set button until the display shows Hours (shown in left most digits), and A or P (shown in right most digit). Release the Set button.
7. Depress the Display button to advance Hours to the proper value. Release the Display button.
8. Depress the Set button until the display shows minutes (shown in right most digits) and colon. Release the Set button.
9. Depress the Display button to advance minutes to approximately one minute past the present time. Release the Display button. Depressing the Display button also resets the seconds counter to zero and hold.
10. Depress Set button until the display shows hours and minutes. Release the Set button.
11. When time reaches the start of the minute set in step 9 (showing on display), depress the Display button. The seconds counter is then started and the watch is in normal operation.

## FUNCTIONAL DESCRIPTION OF INPUTS/OUTPUTS

SET	- Setting Sequence Advance Button	TST	- High Speed Test Control Input
DISPLAY	- Date, Seconds Display/Counter Advance Button	BP	- 32 Hz Backplane Driver
SD	- Oscillator Shutdown Control	CAP 2, CAP 3	- Voltage Tripler Capacitor Connection
VL	- Divider Voltage Supply (- 1.5V)	CAP 1, 512	- Voltage Doubler/Tripler Capacitor Connection
VH	- LCD Driver Voltage Supply (- 4.5V)	OSCIN	- Gate of Oscillator Inverter
VSS	- Most Positive Voltage Supply	OSCOU	- Output of Oscillator Inverter



1076150

**ABSOLUTE MAXIMUM RATINGS**

Storage chip temperature	- 55°C to + 150°C	Negative Voltage (on TST, OSC <sub>OUT</sub> , OSC <sub>IN</sub> , 512Hz, DISPLAY, SET, SD)	V <sub>L</sub> - 0.3V
Operating ambient temperature	- 10°C to + 70°C	Negative Voltage on all other pins	V <sub>H</sub> - 0.3V
Positive Voltage on any pin	+ 0.3V		

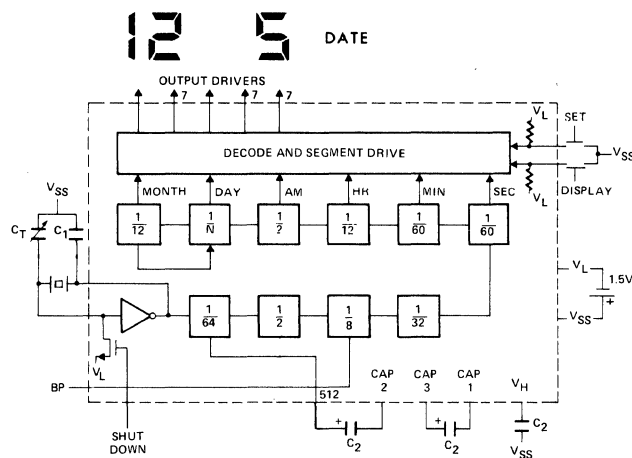
**SPECIFICATIONS**

(T<sub>A</sub> = 25°C, V<sub>L</sub> = - 1.5 ± 5%, V<sub>H</sub> = - 2.9V to - 4.6V, V<sub>SS</sub> = 0V, FREQ = 32768 Hz)

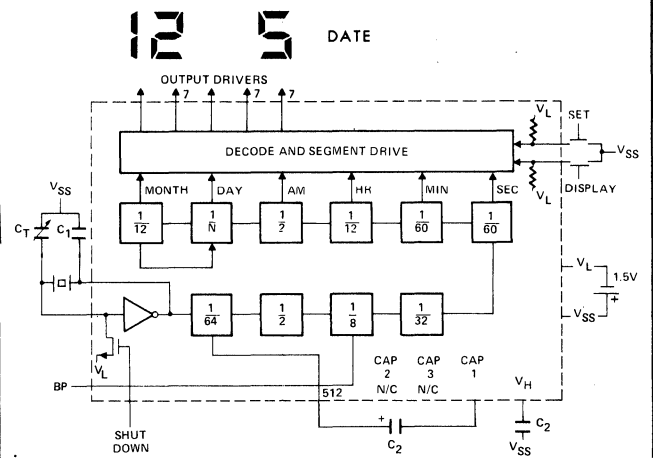
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V <sub>S</sub>	Starting Voltage	- 1.45	- 1.1		Volts	
R (SEG)	Segment Resistance Both States		20		Kohm	I <sub>0</sub> = 10 μA
R (BP)	Back Plate Resistance Both States		6	12	Kohm	I <sub>0</sub> = 10 μA to V <sub>H</sub> or V <sub>SS</sub>
R <sub>H</sub> (512)	512 Hz on Resistance to V <sub>SS</sub>		5	17	Kohm	I <sub>0</sub> = 10 μA
R <sub>L</sub> (512)	512 Hz on Resistance to V <sub>L</sub>			13	Kohm	I <sub>0</sub> = 10 μA
PW (512)	Pulse Width		976		μs	
I <sub>L</sub>	- V <sub>L</sub> Supply Current		2.8	6.0	μA	
I <sub>H</sub>	- V <sub>H</sub> Supply Current			1.0	μA	Outputs open ckt
V <sub>H</sub>	Display Drive Voltage		4.5	12.0	Volts	C <sub>2</sub> = .05 μF
I <sub>IN</sub>	Input Current (Display Set)			1.0	μA	Input connected to V <sub>SS</sub>
	(Shutdown)			0.5	μA	Input connected to V <sub>SS</sub>
R <sub>INOSC IN</sub>	Resistance to V <sub>L</sub>		250		KΩ	During Shutdown

**CRYSTAL REQUIREMENTS**

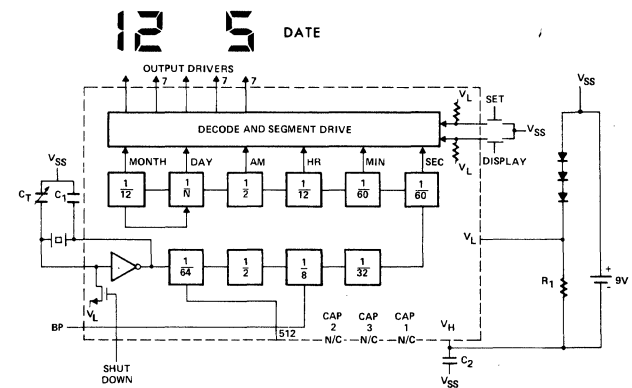
Symbol	Parameter	Value	Units	Notes
F <sub>a</sub>	Oscillator Frequency	32.768	kHz	Typical Crystal is AMI's S23210 Series
R <sub>s</sub>	Series Resistance	40	Kohms	
C <sub>M</sub>	Motional Capacitance	.003	pF	
C <sub>L</sub>		10	pF	
Q		35	K	



1076151A VOLTAGE TRIPLER CONNECTION

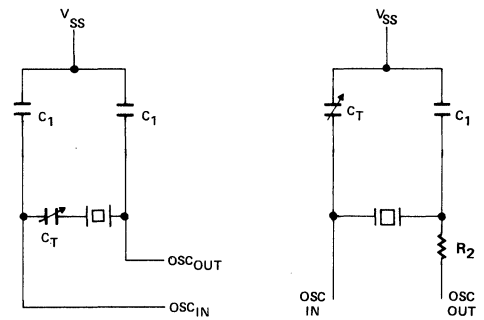


1076151B VOLTAGE DOUBLER CONNECTION



FOR BATTERY OPERATED CLOCK, USING  
9V TRANSISTOR-RADIO BATTERY

1076151C



SERIES TUNING CIRCUIT

PARALLEL TUNING CIRCUIT

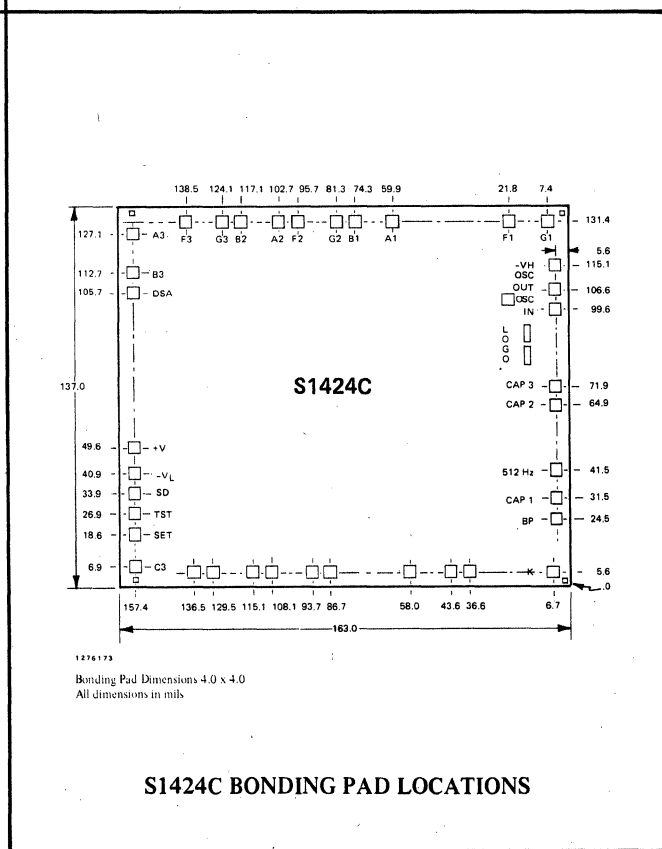
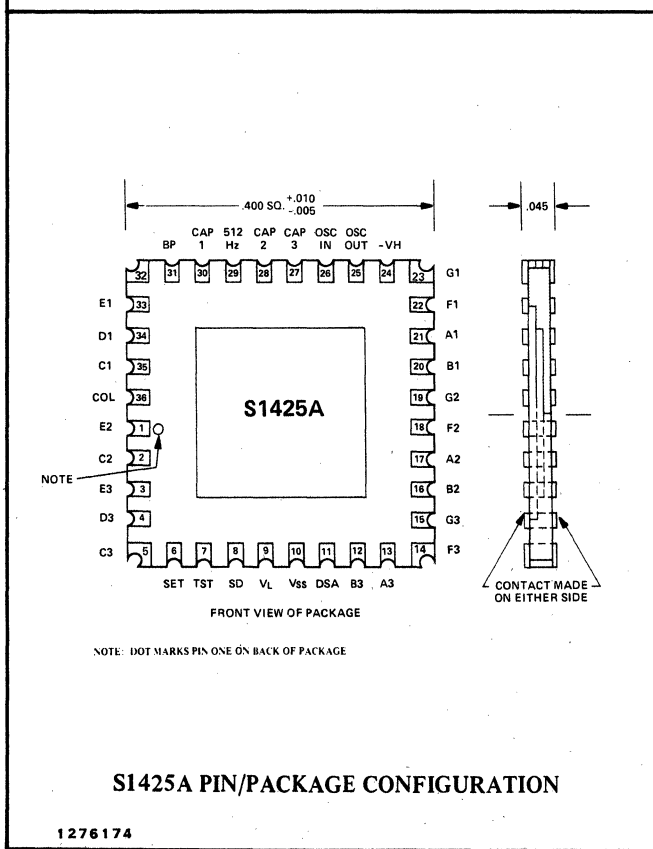
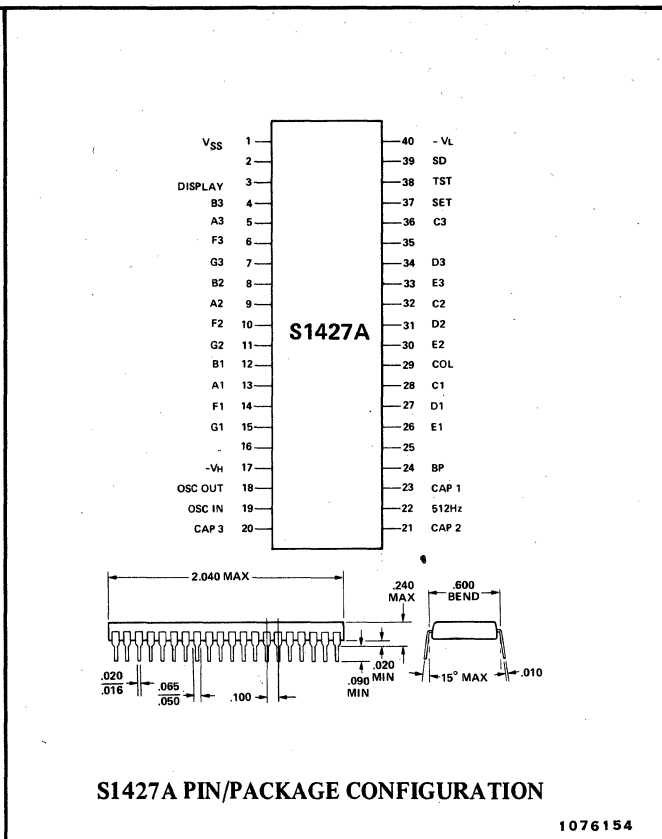
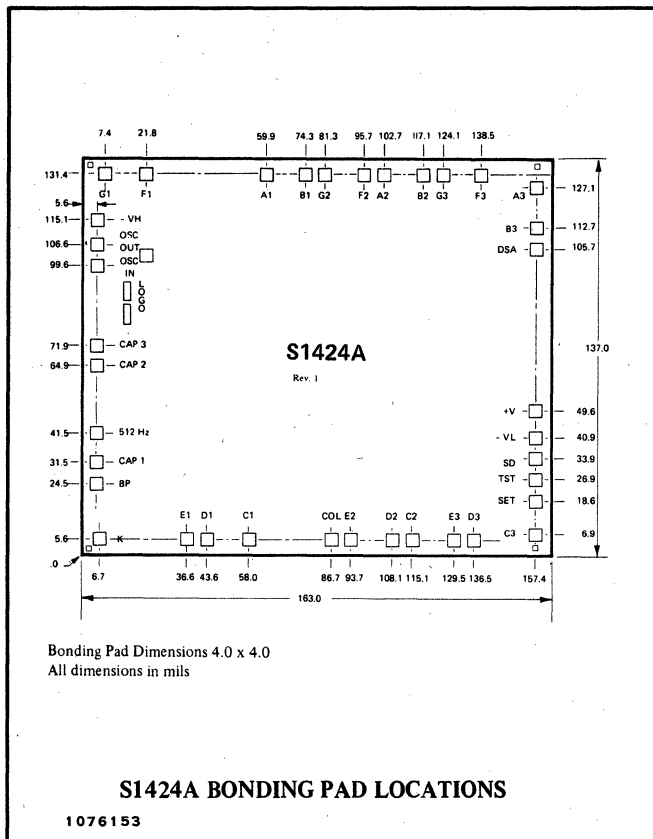
TUNING CIRCUITS

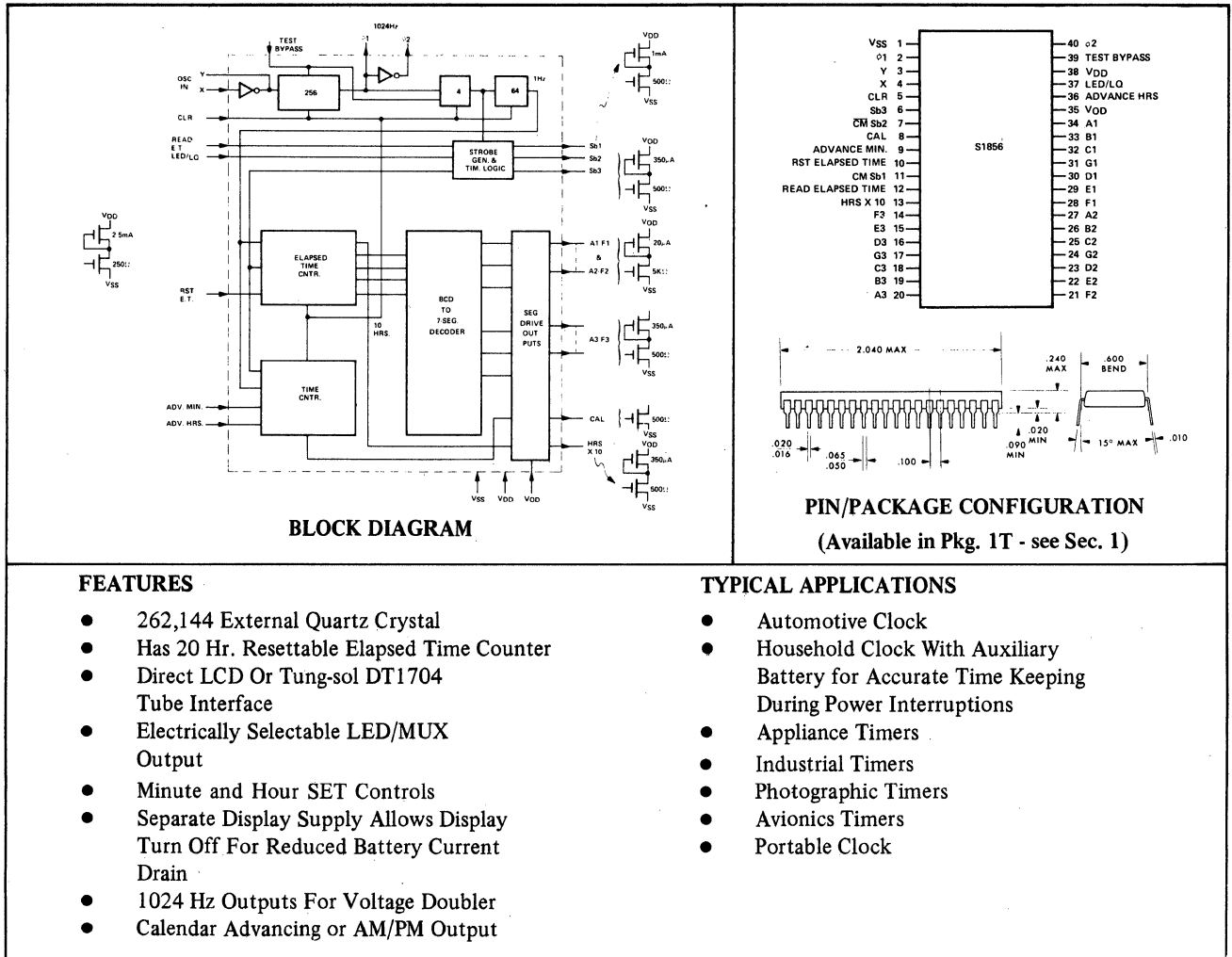
1076152

### EXTERNAL COMPONENT LIST

C <sub>1</sub>	33 pF	R <sub>1</sub>	390 Kohms
C <sub>T</sub>	5 - 50 pF	R <sub>2</sub>	100 - 300 Kohms
C <sub>2</sub>	.05 μF	XTAL	32.768 kHz
		D	IN914

Capacitor values for use in watch modules. When using S1427A (DIP), parameters should consider line and package capacitance.





## FUNCTIONAL DESCRIPTION

The S1856 Digital Clock provides the circuitry to implement a 4 digit time keeper with separate elapsed time counter. It is an MOS LSI circuit consisting of down counters, combinational logic, BCD to 7-seg decoder and output buffer transistors in a 40 pin DIP. The circuit has a separate output pin to drive each segment of a Liquid Crystal Display directly. However if the LED mode of operation is selected, only the HRS x 10 and F3 through A3 outputs are used to provide segment drive current. In this mode of operation segment drivers F3 through

A3 are multiplexed at 25% duty cycle to provide MINUTES, 10's of MINUTES and HOURS information.

The ELAPSED TIME COUNTER can be reset and displayed separately without affecting the state of the time keeper. The ELAPSED TIME COUNTER has the added feature of displaying SECONDS, 10's of SECONDS and MINUTES automatically during the first 10 minutes after a reset has occurred. The counter will then display MINUTES, 10's of MINUTES, HOURS and 10's of HOURS for the remainder of its 20 hour capacity.

**OPERATIONAL DESCRIPTION**

The clock circuit block diagram is shown on the previous page. The input transistor of the circuit forms an oscillator circuit with an external quartz crystal and a few other components (see application drawings). The resultant 262.144 kHz signal is amplified and clipped in the input stage. A chain of binary down counters divides the square wave frequency by 256 to supply two complementary outputs,  $\emptyset 1$  and  $\emptyset 2$  at 1024 Hz. These low impedance outputs can drive an external voltage doubler as well as allow an accurate frequency tuning on the oscillator.

Next a divide by four stage produces a 64 Hz signal from which the three strobes Sb1, Sb2, and Sb3 are generated. The strobe generator also contains logic to synchronize the display outputs with the external strobes as well as control the segments for Liquid Crystal Display operation. The 64 Hz signal also inputs to a divide by 64 stage to produce a 1 Hz signal which inputs to both the TIME COUNTER and the ELAPSED TIME COUNTER.

The TIME COUNTER contains the binary stages and the decoding logic to generate the BCD code for MINUTES, HOURS and HRS x 10. This data is strobed into the BCD to 7-segment DECODER and loaded into the output buffers in synchronization with the appropriate strobe, Sb1, Sb2 or Sb3.

The ELAPSED TIME COUNTER functions similarly to the TIME COUNTER with the additional decoding of SECONDS and 10's of SECONDS to the display instead of HRS and HRS x 10 during the first 10 minutes after reset.

An internal connection to VDD supply at pin 37 holds the clock in the liquid crystal mode and the outputs are interfaced directly with the LCD as shown in Figure 2 below.

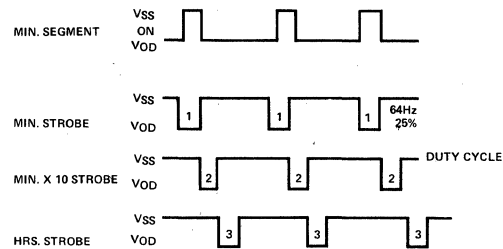
To assure longevity of the LCD display, a 64 Hertz signal is applied to the individual segments. When the applied segment signal is in-phase with the 64 Hertz backplate (LCD common

terminal) voltage, no visibility occurs. When the applied signal is 180° out of phase with the backplate voltage, visibility occurs. The waveforms shown in Figure 2 represent these conditions.

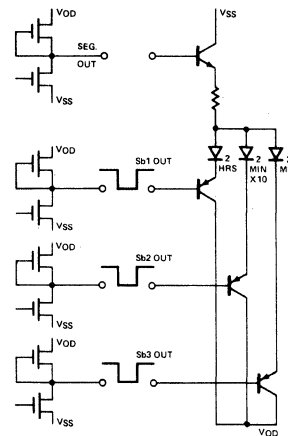
The backplate voltage is generated by buffering the signal which drives the timing counters. This assures that visibility of the display will not occur through synchronizing problems or rise and fall time differences.

The phase of the segment outputs is generated from the contents of data latches and buffer circuits. This provides an active pull-up or pull-down to both terminals of the segments at all times, thus eliminating the effect of capacitive coupling across the LCD segment. (See Figure 2)

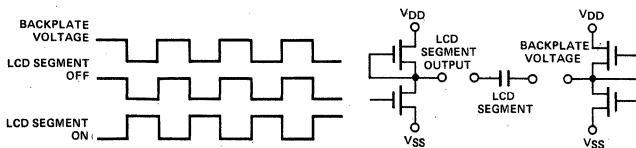
When pin 37 is connected to VSS the multiplexed mode of operation is selected. An ON segment in this mode is driven by a pull-down to VSS which is true during its appropriate strobe time as shown in Figure 3 below.



A typical LED interface circuit is shown below in Figure 4. In this mode the HRS x 10 digit is a steady state DC output and can be used at any of the 3 strobe times.



**FIG. 4 MOS/LED INTERFACE**



**FIG. 2 LCD OUTPUT DRIVE**

## FUNCTIONAL DESCRIPTION OF INPUTS

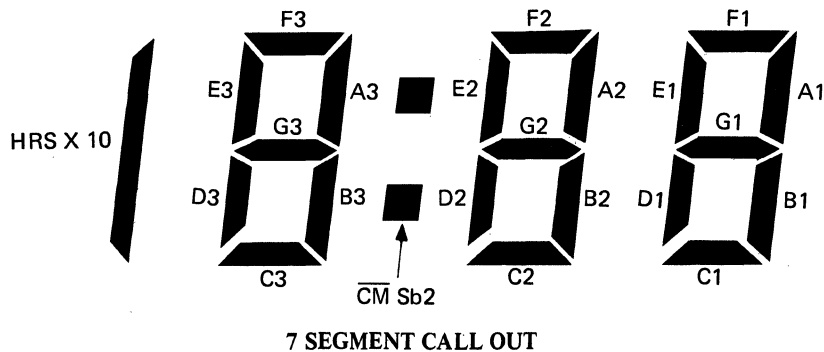
VSS	Positive voltage supply return line for circuit.
Y	Oscillator pull-up resistor connection. A 10K $\Omega$ resistor to VCC from this pin serves as the 262.144 kHz oscillator load.
X	Oscillator input pin. Provides amplification at oscillation frequency of the output from the external crystal and RC network.
CLR	Master Clear. Resets all counters to zero when connected to VSS.
ADV. MIN.	Sets MINUTES with carry to MINUTES x 10 at a one per second rate when connected to VSS.
RST ET	Displays contents of ELAPSED TIME COUNTER when connected to VSS, otherwise time of day is displayed.
VOD	Negative power supply input for output buffers only. Allows display to be turned off while internal clock counters continue to operate.

ADV. HRS.	Sets HRS with carry to HRS x 10, at a one per second rate connected to VSS.
LED/LQ	Mode select pin. When connected to VSS the LED mode is selected. In this mode the three strobe outputs are used to multiplex outputs A3 through F3 to drive MINUTES, MINUTES x 10 and HRS x 10 digits. This occurs at 64 Hz 25% duty rate. In this mode outputs A1 through F1 and A2 through F2 remain off at negative supply level, VOD.
VDD	Negative power supply input for internal logic can be connected to VOD for single supply operation.
TEST BYPASS	When connected to VSS time counters advance at 1024 x normal rate. Used for automatic testing of the clock circuitry.

## FUNCTIONAL DESCRIPTION OF OUTPUTS

$\phi 1$	Voltage doubler and frequency check output. This supplies a 1024 Hz square wave signal which swings between the VSS and VDD voltage levels.
$\phi 2$	Same as $\phi 1$ but 180° out of phase.
Sb3	Strobe signal for HRS digit. 64 Hz 25% duty cycle with voltage swing from VSS to VOD. Used only in LED mode.

$\overline{CM}$ Sb2	Drives colon in Liquid Crystal mode and serves as MIN x 10 digit strobe in LED mode. Voltage swing VSS to VOD.
CAL OUT	Calendar advance output. This pin has internal pulldown to VSS only for stepping motor interface. An external 30 k $\Omega$ resistor may be connected to VOD to drive an external latch for AM-PM display.
CM Sb1	Drives display back plan in LIQUID CRYSTAL mode and serves as MINUTES digit strobe in LED mode. Voltage swing VSS to VOD.



**ABSOLUTE MAXIMUM RATINGS:**

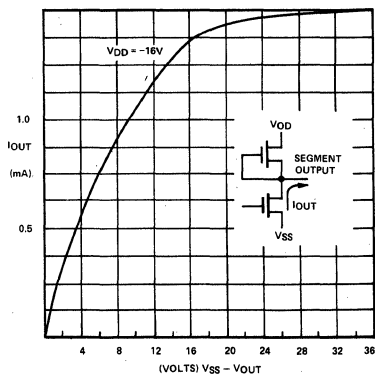
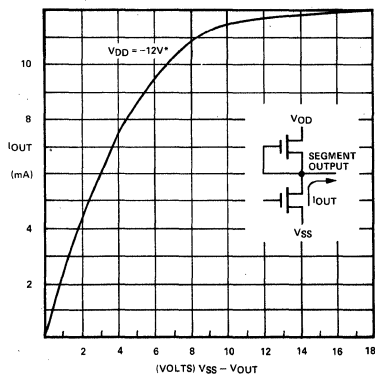
Positive Voltage on any Pin	$V_{SS} + 0.3V$
Negative Voltage on any Pin	$V_{SS} - 28V$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature	$-40^{\circ}C$ to $+100^{\circ}C$

**DYNAMIC CHARACTERISTICS**

( $T_A = -40^{\circ}C$  to  $+70^{\circ}C$ ,  $V_{SS} = 0V$ ,  $V_{DD} = -6V$  to  $-16V$ ,  $V_{OD} = -5V$  to  $-28V$ )

	Min.	Typ.	Max.	Units	Conditions
$V_{IL}$ (OSC X)	$V_{DD}$		$V_{SS} - 6$	Volts	An internal resistor of $700 K\Omega$ (typical) to $V_{DD}$ is provided for all control inputs.
$V_{IH}$	$V_{SS} - 1$		$V_{SS} + 0.3$	Volts	
$V_{IH}$ (Control)	$V_{SS} - 0.5$		$V_{SS} + 0.3$	Volts	
$V_{IL}$	$V_{DD}$		$V_{SS} - 6$	Volts	
$V_{OH}$ (Outputs)	$V_{SS} - 1$			Volts	Open circuit
$V_{OL}$			$V_{DD}$	Volts	Open circuit
$I_{DD}$		10	15	mA	$V_{DD} = -14V$
$I_{DD}$		10		mA	$V_{DD} = -6V$

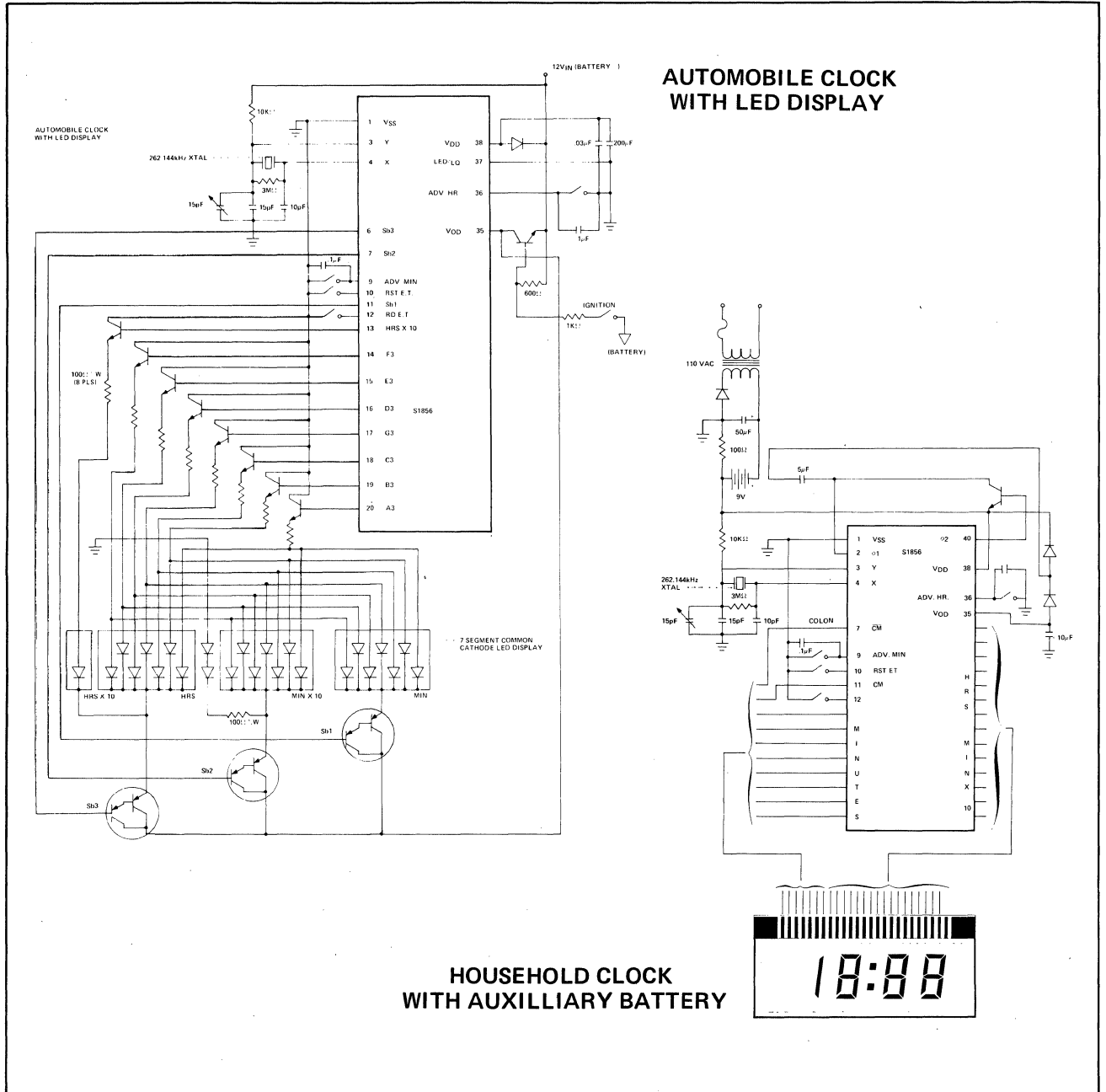
**TYPICAL PERFORMANCE CHARACTERISTICS**



\*TOTAL AVG. CURRENT FOR 7 SEGMENTS < 30mA

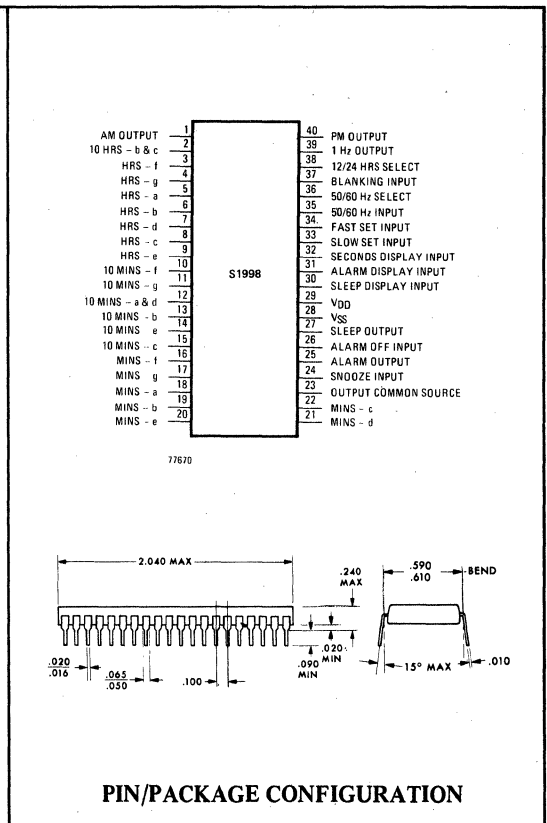
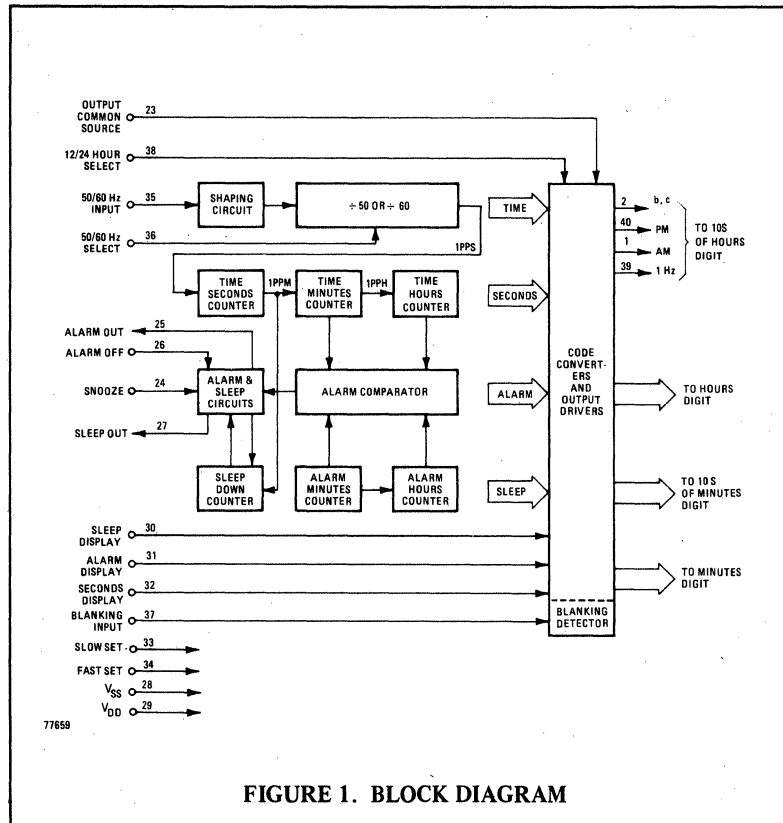
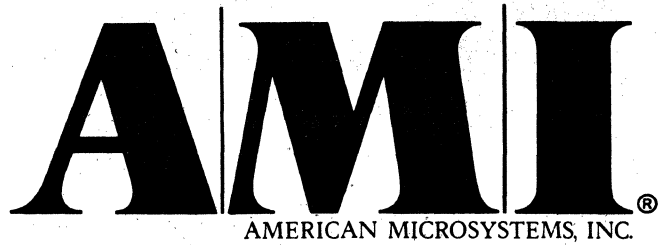


## APPLICATION DATA



# S1998A/B/C

DIGITAL ALARM CLOCK/CLOCK RADIO



## FEATURES

### Lowest System Cost

- Direct LED Drive – S1998A
- Direct GAS DISCHARGE Drive – S1998B
- Direct FLUORESCENT Drive – S1998C
- Clock Input Noise Rejection Circuitry on Chip

### Provides Bright Uniform LED Display – S1998A

- 12.5 mA/Segment – Weighted Average over 12 hour period in 12 hour mode

### Universally Applicable

- 50 or 60 Hz Inputs
- 12 or 24 Hour Mode
- AM/PM Indication in 12 Hour Mode

### Multiple Sources

- Pin Compatible with S1998, MM 5316, MM 5387, EA 5316, FCI 3817, TMS 1951
- Alternate to MM 5384, MM 5385/5386, MK 50380, MK 50365/50366, CK 3300/3400

### Provides Versatility

- Reset-to-zero capability, for elapsed time and also count-down timers
- Blanking Control allows parallel use of multiple circuits with single display (MULTIPLE EVENT TIMER)

### Additional Features

- Power Failure Indication
- 1 Hz Output Blanking
- Presetable 59-Minute Count-Down Timer
- Alarm with Unlimited Snooze Repeat

**FUNCTIONAL DESCRIPTION:**

The S1998A/B/C are three improved versions of the industry-standard S1998 digital alarm clock radio circuit. The S1998A can be directly substituted for the S1998 in high current/low voltage display applications (e.g. common cathode LED displays) where the common source line is connected to  $V_{SS}$ . For higher voltage displays such as gas discharge, the S1998B should be selected; for fluorescent displays the S1998C is appropriate. The circuits interface directly with both solid state and fluorescent/gas discharge displays. The timekeeping function will operate from either a 50 Hz or 60 Hz input and display output may be in either 12-hour or 24-hour format.

The circuits are monolithic integrated circuits using P-Channel, low threshold enhancement mode and ion-implanted depletion mode devices. They are packaged in 40-lead dual-in-line silicone plastic packages.

Outputs consist of display drivers, sleep delay (e.g., timed radio turnoff), and alarm enable. Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication. The devices operate over a power supply range of 8 to 26 volts (S1998A/C) or 8 to 35 volts (S1998B) and do not require regulated supplies.

Clock input noise rejection circuitry eliminates the need for externally filtering the line frequency input. Reset-to-zero circuitry is included for timer/elapsed time applications, and the blanking control allows use of several circuits in parallel with a single display (multiple event timing).

**TYPICAL APPLICATIONS**

Alarm Clocks, Clock Radios, Desk Clocks, Appliance Timers and Elapsed Timers for Industry, Photography, Sports and Avionics.

**OPERATIONAL DESCRIPTION**

A block diagram of the S1998A/B/C digital alarm clock circuit is shown on page 1. The various display modes provided by the circuit are shown in Table 1; functions of the setting controls are listed in Table 2.

**50/60 Hz input (pin 35):** A noise rejection circuit is provided to allow use of either 50Hz or 60Hz unfiltered sine wave input. The noise rejection circuitry uses a Schmitt trigger with a clamp to limit negative excursions in excess of  $V_{DD}$ . When used with a 1 M $\Omega$  resistor the circuit will reject line transients that could cause the clock to gain time or cause damage to the circuit. The output of the circuit is shaped and drives a counter-chain which performs the timekeeping function.

**50 or 60 Hz Select Input (pin 36):** A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1-pps time base. This counter is programmed to divide by 60 simply by leaving pin 36 unconnected; pull-down to  $V_{DD}$  is provided by an internal resistor. Operation at 50 Hz is programmed by connecting pin 36 to  $V_{SS}$ .

**Display Mode Select Inputs (pins 30 thru 32):** In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal pull-down resistors allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table 1. Alternate display modes are selected by applying  $V_{SS}$  to the appropriate pin. As shown in the Block Diagram (Figure 1) the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The Display Mode Select Inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

**Time Setting Inputs (pins 33 and 34):** Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table 2. Again, internal pull-down resistors are provided; application of  $V_{SS}$  to these pins affects the control functions. Note that the control functions are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, for elapsed time or timer applications, the clock time may be reset to 0:00:00 in the 24-hour format (12:00:00 AM in the 12-hour format) by selecting seconds display and simultaneously actuating both slow and fast set inputs.

**Blanking Control Input (pin 37):** Connecting this Schmitt trigger input to  $V_{DD}$  places all display drivers in a non-conducting, high-impedance state, thereby inhibiting the display. See Figure 2. Conversely,  $V_{SS}$  applied to this input enables the display.

**Output Common Source Connection (pin 23):** All display output drivers are open-drain devices with all sources common to pin 23 (Figure 2). When using fluorescent tube displays, brightness control is achieved by use of the Blanking Voltage, as shown in Figure 10. For gas discharge applications (S1998B) common source should be connected to  $V_{DD}$  externally (see Figure 9).

When using LED displays the S1998A is connected as shown in Figure 4 to provide direct drive to the display. The 16 to 26 volt  $V_{DD}$  supply insures low output on resistance. The resistor  $R_{LED}$  limits the common source current to 200mA average. (Note: A transistor may be substituted for  $R_{LED}$  to provide a brightness control.) To achieve this current drive capability, the common source of the S1998A is internally connected to  $V_{SS}$ . The common source (pin 23) must be connected to the power supply in the user's application; any connection to  $V_{SS}$  (pin 28) is optional.

**12 or 24 Hour Select Input (pin 38):** By leaving this pin unconnected, the outputs for the most significant display digit (10's of hours) are programmed to provide a 12 hour display format. An internal pull-down resistor is again provided.

Connecting this pin to  $V_{SS}$  programs the 24-hour display format. Also, the output connections (pins 1, 2 and 40) are different for each format. Figure 3 illustrates these differences. In addition to displaying 10's of hours, this digit provides an AM/PM indication (12 hour format only) and the power failure indication. In the 12-hour format, AM indication is provided by segment "f"; PM indication by segment "e." The power failure indication consists of a flashing of the AM or PM indicator at a 1 Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal. In the 24-hour format, the power failure indication consists of flashing segments "a", "d", "e", "g" of the HR x 10 digit.

**Alarm Operation and Output (pin 25):** The alarm comparator (Figure 1) senses coincidence between the alarm counter (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver (Figure 2), the S1998 output that is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes during which the alarm will sound if the latch output is not temporarily inhibited by another latch set by the snooze input (pin 24) or reset by the alarm off input (pin 26).

**Snooze Input (pin 24):** Momentarily connecting pin 24 to  $V_{SS}$  inhibits the alarm output for between 8 and 9 minutes after which the alarm will again be sounded. This input is

pulled down to  $V_{DD}$  by an internal resistor. The snooze feature may be repeatedly used during the period in which the alarm latch remains set.

**Alarm Off Input (pin 26):** Momentarily connecting pin 26 to  $V_{SS}$  resets the alarm latch and thereby silences the alarm. This input is also returned to  $V_{DD}$  by an internal resistor. The momentary alarm off input also readies alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm off input should remain at  $V_{SS}$ .

**Sleep Timer and Output (pin 27):** The sleep output at pin 27 can be used to turn off a radio after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode (Table 1) and setting the desired time interval (Table 2). This automatically results in a current source output via pin 27, which can be used to turn on a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning off the radio. This turn-off may also be manually controlled (at any time in the countdown) by a momentary  $V_{SS}$  connection to the snooze input (pin 24). The output circuitry is the same as the alarm output (Figure 2).

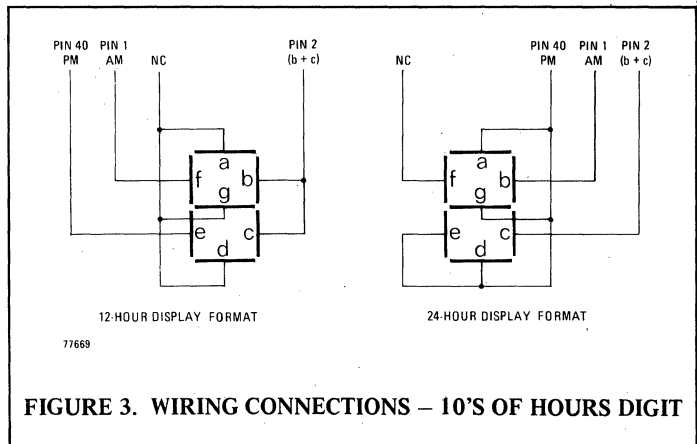
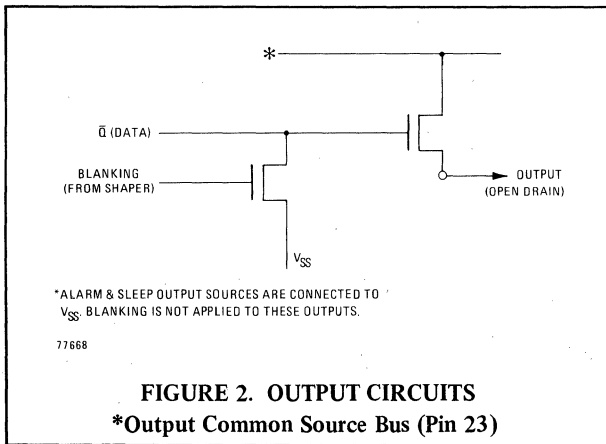


TABLE 1. DISPLAY MODES

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

\*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (No other mode selected).

TABLE 2. SETTING CONTROL FUNCTIONS

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow Fast Both	Minutes Advance at 2 Hz Rate Minutes Advance at 60 Hz Rate Minutes Advance at 60 Hz Rate
Alarm	Slow Fast Both	Alarm Minutes Advance at 2 Hz Rate Alarm Minutes Advance at 60 Hz Rate Alarm Resets to 12:00 AM (12-hour format) Alarm Resets to 0:00 (24-hour format)
Seconds	Slow Fast Both	Input to Entire Time Counter is Inhibited (Hold) Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes Time Resets to 12:00:00 AM (12-hour format) Time Resets to '0:00:00 (24-hour format)
Sleep	Slow Fast Both	Subtracts Count at 2 Hz Subtracts Count at 60 Hz Subtracts Count at 60 Hz

\*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

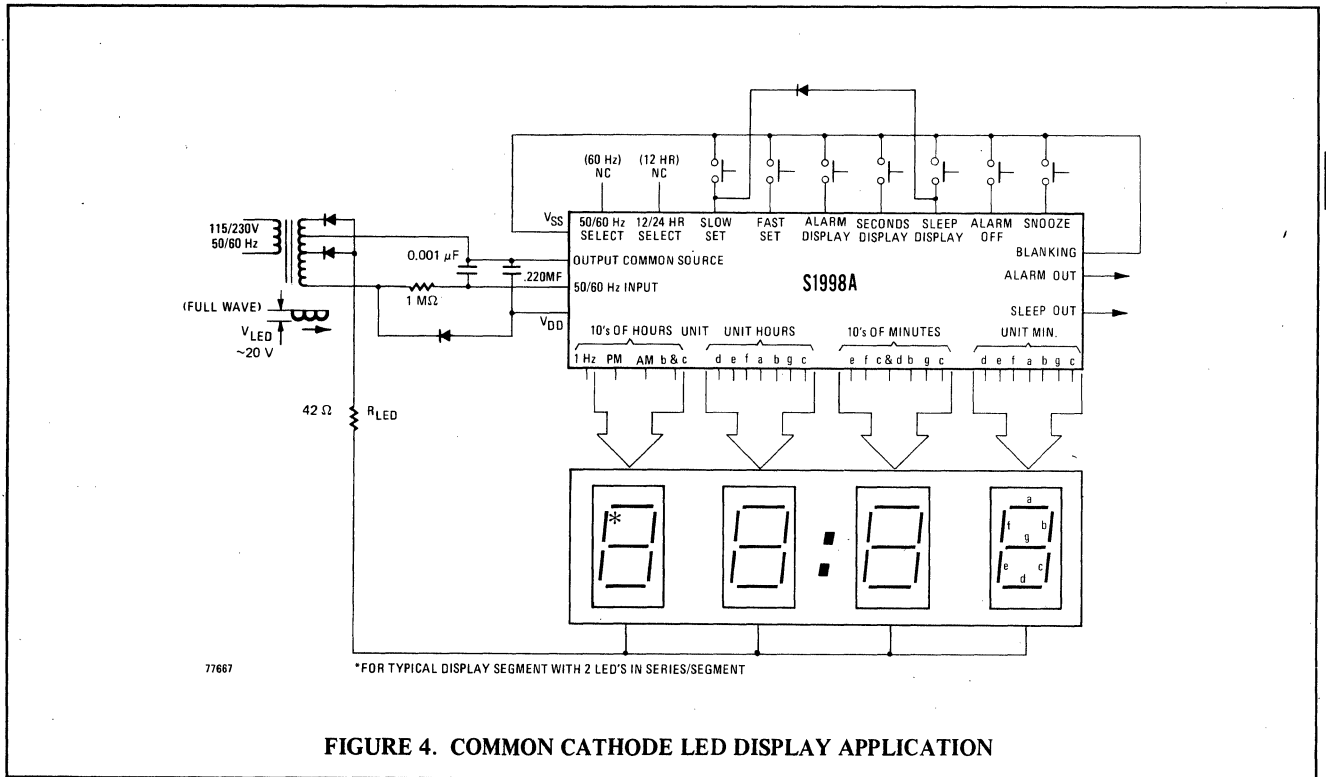


FIGURE 4. COMMON CATHODE LED DISPLAY APPLICATION

## S1998A

### ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin	$V_{SS} + 0.3V$	Storage Temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Negative Voltage on any Pin	$V_{SS} - 30V$	Operating Ambient Temperature	$-25^{\circ}C$ to $+70^{\circ}C$

S1998A CONTINUED

STATIC CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ ,  $V_{SS} = +21 \pm 5\text{V} = V_{COM}^*$ ;  $V_{DD} = \text{GROUND}$ ; Common Source +  $V_{SS}$  Internally connected).

	MIN	TYP	MAX	UNITS	CONDITIONS
Power Supply Current		3.5	5	mA	$V_{SS} = +8\text{V}$ (no output loads) $V_{SS} = +26\text{V}$
		4	6	mA	
$V_{SS}$ Range	+ 8		+ 26	V	
50/60 Hz Input:					
Frequency	DC	50 or 60	5K	Hz	
Voltage					
$V_{IH}$ Logical High Level	$V_{SS} - 1$		$V_{SS}$	V	Internal resistor to $V_{DD}$ on all inputs except CLOCK, BLANK
$V_{IL}$ Logical Low Level	$V_{DD}$		$V_{DD}+1$	V	
Power Failure Detect Voltage:	8 5		16	V	
Output Currents*:					
PM (24 hr. Mode)					$V_{SS} = +16\text{V}$ to + 26 V $V_{OH} = V_{SS} - 3\text{V}$ $V_{OL} = V_{SS} - 10\text{V}$
$I_{OH}$ Logical High Level	32			mA	
$I_{OL}$ Logical Low Level			10	$\mu\text{A}$	
10's of Hours (b & c) (12 hr Mode); 10's of Minutes (a & d)					
$I_{OH}$ Logical High Level	16			mA	$V_{OH} = V_{SS} - 3\text{V}$ $V_{OL} = V_{SS} - 10\text{V}$
$I_{OL}$ Logical Low Level			10	$\mu\text{A}$	
All Other Display					(9 mA in 12-hour mode, with weighted average of 12.5 mA (see Note 1).
10's of Hours (b & c) (24 Hr. Mode)					
PM (12 hr. Mode)					
$I_{OH}$ Logical High Level (24 Hour Mode)	8 <sup>(1)</sup>			mA	$V_{OH} = V_{SS} - 3\text{V}$ $V_{OL} = V_{SS} - 10\text{V}$
$I_{OL}$ Logical Low Level			10	$\mu\text{A}$	
Alarm, Sleep					
$I_{OH}$ Logical High Level	500			$\mu\text{A}$	$V_{OH} = V_{SS} - 2\text{V}$

\* $V_{COM}$  is the voltage on Pin 23

$I_{COM}$  (pin 23 current) should not exceed 200 mA Average. RLED is chosen to provide this limit.

Note 1:

Output current is a function of the number of segments "ON", supply voltage, LED voltage, and RLED, where RLED is chosen to limit total Common Source current to 200 mA average.

Minimum current per segment occurs at maximum number of segments "ON". In 12-hour mode, this is 21 segments at time 12:08; in 24-hour mode, this is 25 segments at time 20:08.

A more meaningful measure of output segment current is a WEIGHTED AVERAGE over an extended period. Over any 12 hour period, in the 12-hour mode, the WEIGHTED AVERAGE output current per segment is 12.5 mA.

(Conditions:  $V_{SS} = 26\text{V}$ ,  $V_{LED} = 20\text{V}$ ,  $V_{DISPLAY} = 3.2\text{V}$ ,  
 $R_{LED} = 42\Omega$  to limit  $I_{COM}$  to 200 mA average.

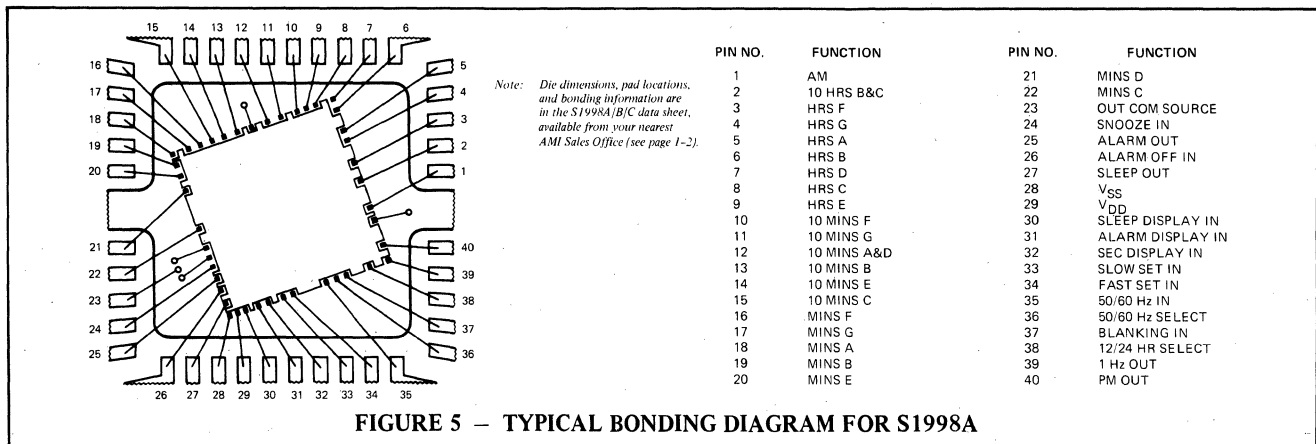


FIGURE 5 - TYPICAL BONDING DIAGRAM FOR S1998A

## S1998B

### ADVANCED PRODUCT DESCRIPTION

#### ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin	$V_{SS} + 0.3V$	Negative Voltage on any Pin	$V_{SS} - 30V$
Negative Voltage on Supplies and Outputs	$V_{SS} - 40V$	Storage Temperature	$-55^{\circ}C$ to $+150^{\circ}C$
		Operating Ambient Temperature	$-25^{\circ}C$ to $+70^{\circ}C$

S1998B (Common source and  $V_{SS}$  separate)

#### STATIC CHARACTERISTICS

$T_A = 25^{\circ}C$ ,  $V_{SS} = 32 \pm 3V$ ,  $V_{DD} = V_{COM} = GROUND$

	MIN	TYP	MAX	UNITS	CONDITIONS
$I_{SS}$ Power Supply Current		3.5 4	5 6	mA mA	$V_{SS} = +8V$ (no output loads) $V_{SS} = +35V$
$V_{SS}$ Range	+ 8		35	V	
50/60 Hz Input:					
Frequency	DC	50 or 60	5K	Hz	
Voltage					
$V_{IH}$ Logical High Level	$V_{SS} - 1$		$V_{SS}$	V	Internal resistor to $V_{DD}$ on all inputs except CLOCK, BLANK
$V_{IL}$ Logical Low Level	$V_{DD}$		$V_{DD} + 1$	V	
Power Failure Detect Voltage:	10		18	V	
Output Currents**:					$V_{SS} = +29$ to $35$ , $V_{DD} = 0V$
PM (24 hr. Mode)					Pin 23 = 0V
$I_{OH}$ Logical High Level	2.8			mA	$V_{OH} = V_{DD} + 8V$
$I_{OL}$ Logical Low Level			2	$\mu A$	$V_{OL} = V_{SS}$
10's of Hours (b & c) (12 hr Mode); 10's of Minutes (a & d)					
$I_{OH}$ Logical High Level	1.4			mA	$V_{OH} = V_{DD} + 8V$
$I_{OL}$ Logical Low Level			2	$\mu A$	$V_{OL} = V_{SS}$
All Other Display					
10's of Hours (b & c) (24 Hr. Mode) PM (12 hr. Mode)					
$I_{OH}$ Logical High Level	.7			mA	$V_{OH} = V_{DD} + 8V$
$I_{OL}$ Logical Low Level			2	$\mu A$	$V_{OL} = V_{SS}$
Alarm Sleep					
$I_{OH}$ Logical High Level	500			$\mu A$	$V_{OH} = V_{SS} - 2V$

\* $V_{COM}$  is the voltage on Pin 23

\*\* $I_{COM}$  (pin 23 current) should not exceed 40 mA Average

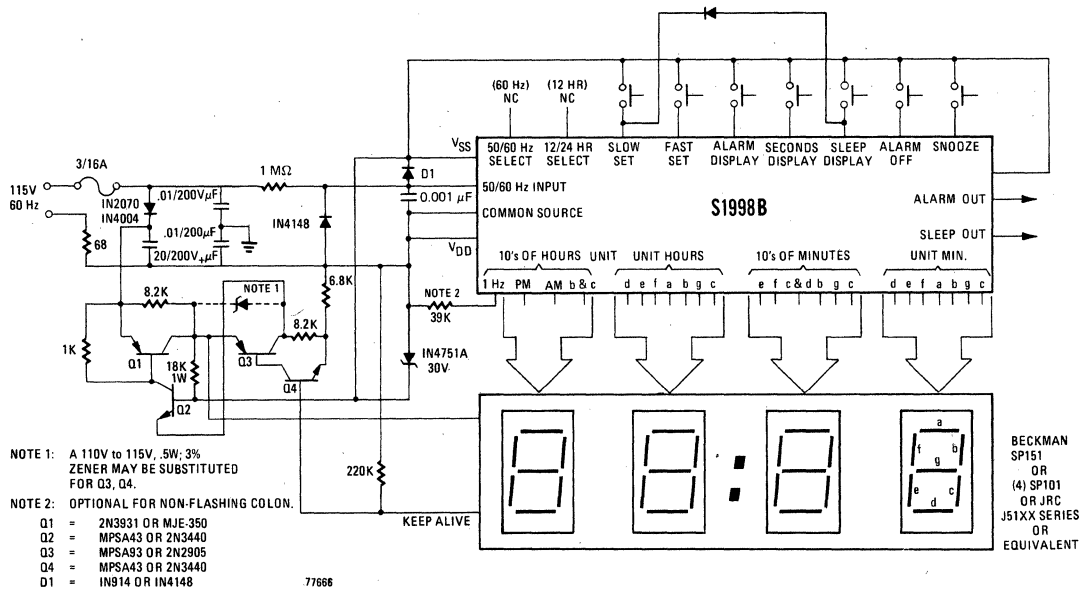


FIGURE 6. GAS DISCHARGE DISPLAY APPLICATION  
(with "Keep Alive" voltage regulator)



## S1998C

### ABSOLUTE MAXIMUM RATINGS

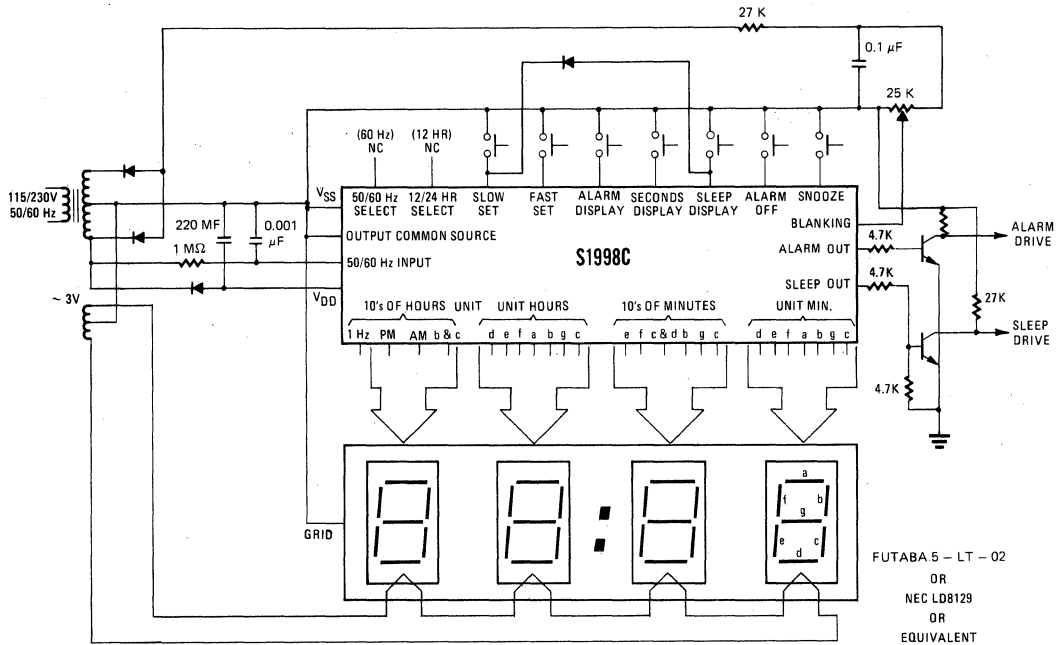
Positive Voltage on any Pin	$V_{SS} + 0.3V$	Storage Temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Negative Voltage on any Pin	$V_{SS} - 30V$	Operating Ambient Temperature	$-25^{\circ}C$ to $+70^{\circ}C$

### STATIC CHARACTERISTICS

$T_A = 25^{\circ}C$ ,  $V_{SS} = +21 \pm 5V$ ,  $V_{DD} = GROUND$

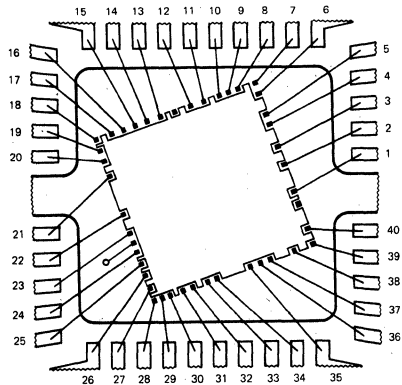
	MIN	TYP	MAX	UNITS	CONDITIONS
$I_{SS}$ Power Supply Current		3.5	5	mA	$V_{SS} = +8V$ (no output loads)
$V_{SS}$ Range	+ 8	4	+ 26	V	$V_{SS} = +26V$
50/60 Hz Input:					
Frequency	DC	50 or 60	5K	Hz	
Voltage					
$V_{IH}$ Logical High Level	$V_{SS} - 1$		$V_{SS}$	V	Internal resistor to $V_{DD}$ on all inputs except CLOCK, BLANK
$V_{IL}$ Logical Low Level	$V_{DD}$		$V_{DD}+1$	V	
Power Failure Detect Voltage:	8		16	V	
Output Currents*:					$V_{SS} = +16V$ to $+26V$
PM (24 hr. Mode)					
$I_{OH}$ Logical High Level	16			mA	$V_{OH} = V_{SS} - 2V$
$I_{OL}$ Logical Low Level			1	$\mu A$	$V_{OL} = V_{DD}$
10's of Hours (b & c) (12 hr Mode);					
10's of Minutes (a & d)					
$I_{OH}$ Logical High Level	8			mA	$V_{OH} = V_{SS} - 2V$
$I_{OL}$ Logical Low Level			1	$\mu A$	$V_{OL} = V_{DD}$
All Other Display					
10's of hours (b & c) (24 Hr. Mode)					
PM (12 hr. Mode)					
$I_{OH}$ Logical High Level	4			mA	$V_{OH} = V_{SS} - 2V$
$I_{OL}$ Logical Low Level			1	$\mu A$	$V_{OL} = V_{DD}$
Alarm, Sleep					
$I_{OH}$ Logical High Level	500			$\mu A$	$V_{OH} = V_{SS} - 2V$

\* $I_{COM}$  (pin 23 current) should not exceed 25 mA average



77665

FIGURE 7. FLUORESCENT DISPLAY APPLICATION



PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	AM	21	MINS D
2	10 HRS B&C	22	MINS C
3	HRS F	23	OUT COM SOURCE
4	HRS G	24	SNOOZE IN
5	HRS A	25	ALARM OUT
6	HRS B	26	ALARM OFF IN
7	HRS D	27	SLEEP OUT
8	HRS C	28	V <sub>SS</sub>
9	HRS E	29	V <sub>DD</sub>
10	10 MINS F	30	SLEEP DISPLAY IN
11	10 MINS G	31	ALARM DISPLAY IN
12	10 MINS A&D	32	SEC DISPLAY IN
13	10 MINS B	33	SLOW SET IN
14	10 MINS E	34	FAST SET IN
15	10 MINS C	35	50/60 Hz IN
16	MINS F	36	50/60 Hz SELECT
17	MINS G	37	BLANKING IN
18	MINS A	38	12/24 HR SELECT
19	MINS B	39	1 Hz OUT
20	MINS E	40	PM OUT

Note: Die dimensions, pad locations, and bonding information are in the S1998A/B/C data sheet, available from your nearest AMI Sales Office (see page 1-2).

FIGURE 8 - TYPICAL BONDING DIAGRAM FOR S1998C

# 7

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## **Liquid Crystal Displays**

## Liquid Crystal Displays

Device No.	Description	Application	Compatible Circuit
D8151A Series	A 3½-digit display with extremely large digits in a popular-sized display package. Special order option available: <ul style="list-style-type: none"> <li>• Custom artwork</li> </ul>	Watch	S1408 S1424A
D8154A Series	A 4-digit alphanumeric watch display with annunciators in a very popular glass size, destined to become an industry standard. Special order option available: <ul style="list-style-type: none"> <li>• Custom artwork</li> </ul>	Watch	Intersil 7210 Harris
D8158A Series (formerly D8145A)	A very popular glass size for 3½-digit watch display. The glass size is the prime industry standard, and will be used for several new digit configurations. Special order options available: <ul style="list-style-type: none"> <li>• Custom artwork</li> </ul>	Watch	S1408 S1424A
D8159A Series	A small 3½-digit ladies watch display	Watch	S1424A
D8163A Series	A 6-digit alphanumeric watch display	Watch	Micropower
D81xxA Series	A 3½-digit five-function alphanumeric "Uni-Sex" sized display that could be used in either a man's or ladies' watch.	Watch	S1408, S1424A
D8300A Series	A 5½-digit clock display with "Date" and "Sec" annunciators, packaged in a popular glass size, with a primary digit height of 0.7 in.	Clock	Nortec 5022 Micropower MPS7125
D8301A Series	A 3½-digit combination clock/instrument display, packaged in a popular glass size, with a digit height of 0.5 in.	Clock/ Instrument	S1408, S1424A
D8302A Series	A 3½-digit clock display with "AM/PM" annunciators, packaged in a popular glass size, with a digit height of 1.1 in.	Clock	S1408, S1424A

## Future Products

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24-hour Clock Displays  
 Alphanumeric Clock Displays  
 4½-digit Instrument Displays  
 Calculator Displays

# AMI Liquid Crystal Displays

## QUALITY BASED ON EXPERIENCE

Until a few years ago, liquid crystals were a laboratory curiosity with little commercial value. AMI was one of the first companies to work on a practical liquid crystal product, and in 1971 introduced LCD displays in their calculator product line. Today, the Company has grown to become one of the largest suppliers of field-effect type LCDs, manufacturing displays for a variety of OEM applications. AMI has full capability to design, produce original artwork, and manufacture field-effect liquid crystal displays of various configurations. This enables AMI to control each and every operation, thus reducing costs and establishing rigid quality assurance requirement standards, unsurpassed in the industry.

## VARIETY OF PRODUCTS

Presently AMI delivers large numbers of LCDs to watch manufacturers throughout the world. In addition to watch products, further research and engineering is continuing in many process and product areas to meet ongoing commercial and industrial LCD needs for miniaturization, larger area displays, improved characteristics, extended life, and reduced operating voltages. Though AMI is production oriented, a major part of the Company's continuing success is its commitment to custom products.

AMI liquid crystal displays provide the high degree of readability needed in digital applications — and with only a

fraction of the power required by other types of displays. Liquid crystals exhibit effective readability under almost all lighting conditions; diffused lighting does not adversely affect the display, thus no washing out occurs under direct sunlight.

## BUILT-IN RELIABILITY

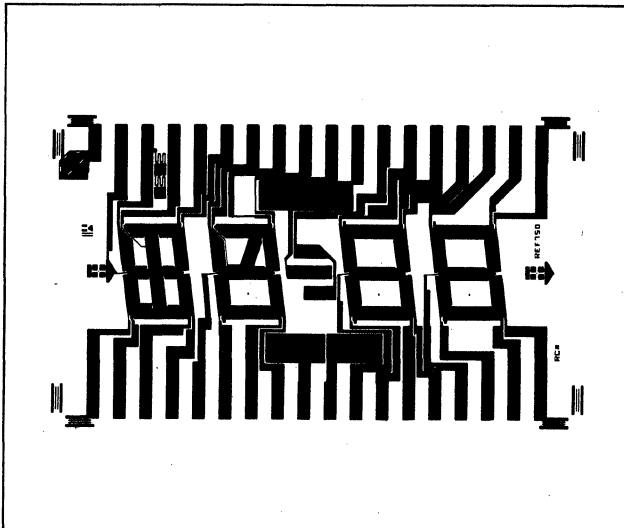
Each display is a plug-in type, able to interface directly with MOS watch circuits, including the AMI S1424 CMOS series.

AMI LCDs feature glass-to-glass construction, assuring mechanical durability and long life. In addition, the use of the twisted nematic field-effect technique for the LCDs (as opposed to dynamic scattering), allows compact designs and lowest operating voltages. All AMI watch displays are on at 3 volts and are completely turned off at 1 volt. During the off condition a display draws no power.

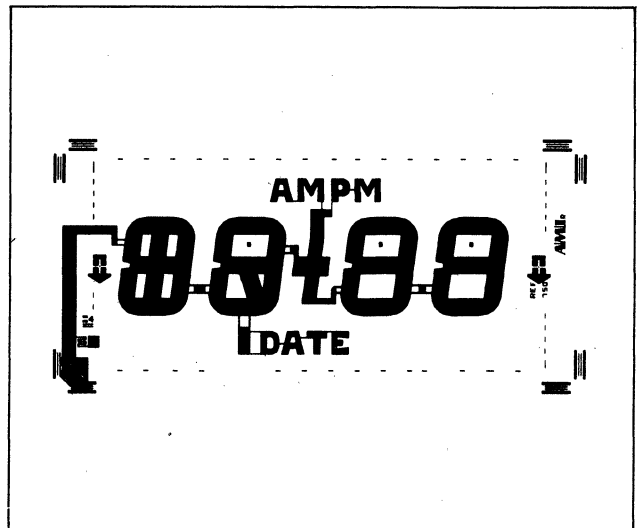
Other outstanding features of AMI liquid crystal displays include stable liquid crystal materials, excellent UV immunity, and extended life projections under recommended input signal conditions.

## QUALITY CONTROL OF LCDs

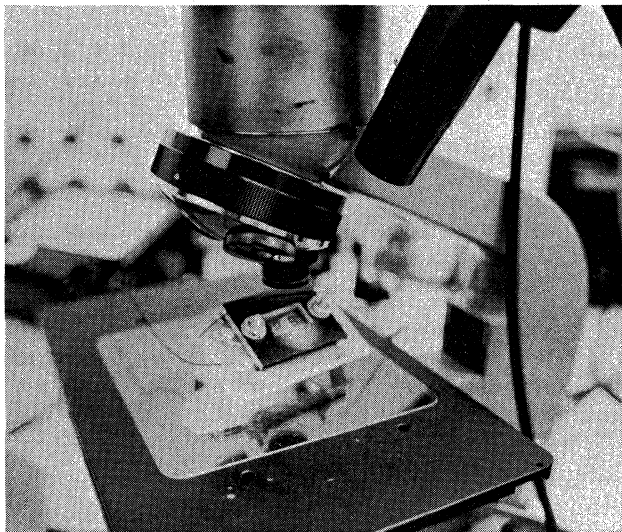
In order to ensure the highest degree of reliability of AMI liquid crystal displays, there are two significant test/failure programs conducted continuously in manufacturing: 1) Production Testing, and 2) Reliability Testing.



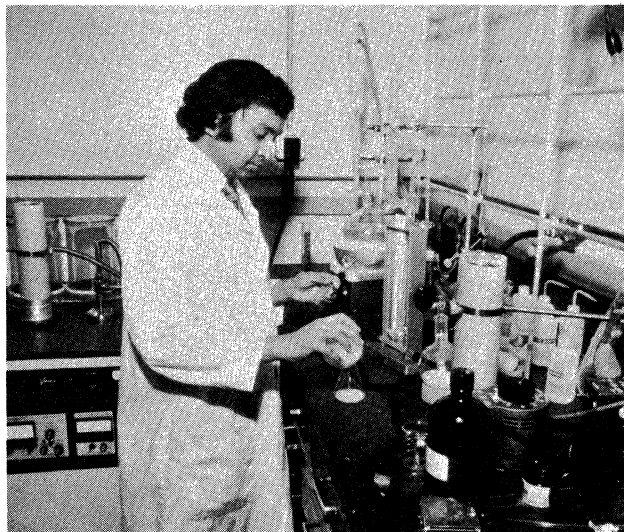
ARTWORK FOR A TYPICAL FRONT PLANE OF A WATCH DISPLAY



ARTWORK FOR A TYPICAL BACK PLANE OF A WATCH DISPLAY



**THE VIEWING ANGLE IS CHECKED ON DISPLAY CELLS WITH A DIGITAL PHOTOMETER**



**THE MATERIALS FOR AMI DISPLAYS ARE MADE IN OUR OWN LABORATORIES**

### **Production Testing**

Every display manufactured by AMI is subjected to electrical, visual and dimensional testing and inspection prior to shipment. Electrical testing verifies functional performance; the visual inspection assures cosmetic and physical acceptance; and the dimensional checks assure conformance to drawings.

Electro-optical tests are performed on sample quantities periodically, to assure acceptable levels of response time, contrast ratio, operating current (at room ambient as well as operating temperature extremes) and other specification requirements.

Reliability testing is performed on sample lots of production displays to verify operational capabilities after the displays are subjected to environmental extremes. These tests include:

- Operating Life Tests
- High Temperature Storage
- Low Temperature Storage
- Thermal Cycling
- Temperature-Humidity
- Ultraviolet Exposure
- Seal Integrity (Dye Penetrant)

# LCDs Are Changing!

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When LCDs were first introduced in the early 1970s, they started out fast, but sometimes were backed up by very little technological knowhow. A large number of would-be manufacturers appeared on the scene and along with them came some inferior products — both in reliability and appearance. As a result, many large potential users pulled back and some misconceptions about LCDs arose. (For example, the old wives' tale that "LCDs dry out after a while" still can be heard from an occasional bystander.)

By now several years of experience have been accumulated and a few stable high quality LCD manufacturers have emerged as the industry leaders. Therefore, it is time to look at the technology and its products again. The development of LCDs is still advancing very rapidly, but trends in products and materials, as well as some user experience, are established. Now, a user needs to continuously update his information on specific characteristics of LCDs, follow new kinds of products, recognize the widening range of applications of LCDs, and be familiar with general trends in technology.

## TYPES OF DISPLAYS

LCD operational modes are well known: excitation applied to the crystalline material inside the display changes its molecular orientation, thus modifying the light passing through. The more common twisted-nematic field-effect displays usually have a black or dark image on a clear or light colored background, however, the image may be reversed by rotating one of the two polarizers 90 degrees. The less common dynamic scattering displays have a white image on a clear or reflective mirrored background.

In field-effect displays, various color combinations of digits and backgrounds can be obtained by varying the tint or percent transmissiveness of the polarizers used. For example, a black image is usually obtained by using 42% transmissive polarizers. Changing to higher percentage transmissive polarizers (55%) gives blue digits. The 42% to 46% transmissive polarizers are most commonly used — mainly due to their wide availability, and because black digits are usually preferred (they yield a higher effective contrast ratio, when viewed on a light background). By changing the color of the rear reflector (reflective mode) some interesting color combinations are possible.

Both field-effect and dynamic-scattering displays can operate either in the reflective or transmissive mode. Since the LCDs emit no light of their own, a reflective mode LCD becomes less readable at very low light levels. Transmissive-mode displays, properly back-lighted by an external source, can provide low-ambient performance equivalent to light-emit-

ting displays, such as gas-discharge displays or LEDs. The trade-off is the increased power consumption of the light source, which partially negates the LCD low power advantage. The light source, of course, does not have to be operated continuously, and may be switched on only during low ambient conditions. It is important to note that an LCD is the *only* type of display available today that can have a provision for nighttime viewing and yet have increased readability in high ambient light.

Most liquid crystal displays are fabricated using screening or photo techniques, with Schiff Base, Esters, or Bi-phenyls as the liquid crystal material inside the cell. Field-effect LCDs have the liquid crystal material sandwiched between two glass sheets, separated by approximately one-half mil (12 microns), and sealed at the perimeters. As with semiconductors, yield is the most important factor in manufacturing. With small displays, the major constraint on yield is line resolution in the image displayed. Manufacturers using screening techniques have design rules which limit them to 5-7 mil lines between 7-segment displays, with reasonable yields. However, photo techniques allow higher tolerances—on the order of 2 to 4 units and AMI's AEA Process can yield 1 mil spacing.

## OTHER ADVANTAGES

Liquid crystal displays have a number of distinct advantages that explain why a great deal of effort is going into the technology.

**Low Power Consumption.** The power requirements of LCDs are remarkably low. A twisted-nematic field-effect display, as used in a digital watch, typically requires less than one microwatt with all segments energized. In comparison, a four-digit LED watch display typically consumes 50 milliwatts, when operated at 3 to 4 volts! The low voltage, low current requirements of LCDs make them naturally compatible with CMOS circuits. (A dynamic-scattering type liquid crystal display, operating at 12 to 20 volt levels, dissipates approximately 40 to 50 microwatts.)

**Alphanumerics/Pictures/Symbols.** The ability to mix alphanumerics of any font, pictures, and symbols in a single envelope is another advantage of LCDs. In essence, any image that can be photographed can be presented as a liquid crystal display.

The advantages of LCDs are accompanied by some operational *trade-offs*. These trade-offs are relatively slow turn-on/turn-off times, and somewhat limited operational temperature ranges, as compared to other types of displays. However, advancements in materials, packaging, and the understanding of failure modes have resulted in continuous improvement of these parameters.

LCDs are noted for their faster response times above 25°C, while becoming slower as they approach 0°C. Response times (sometimes referred to as switching times) are dependent also on drive levels, the liquid crystal material, and the distance separating the front and back plates of the display cell. Tighter spacing of the plates results in faster switching times, but from a manufacturing yield standpoint, the tighter tolerances are more difficult to maintain, particularly in the larger instrumentation type displays.

It is important to understand the terms used to describe switching time. Some data sheets specify switching time excluding the trigger signal. This kind of specification "hides" the trigger transition, which can often involve an additional 50-100 ms! A realistic specification gives response times (200 ms turn-on, 350 ms turn-off are typical) from the trigger signal to within 10% of full change of image (or to 95% on).

A designer does have some opportunity to choose a trade-off for his particular application. For example, for a given display configuration tighter tolerances between the glass plates may be possible, a different mixture of LC material be used, or a higher drive voltage might be applied. The trade-off might involve some additional cost for the display, or display drive system. Here again, all manufacturers are gradually reducing the cost of LCDs, as better materials and methods develop.

Field-effect LCDs generally have an operating range of 0° to 60°C (32°F to 144°F), and a storage range of -40°C to 65°C (-40°F to 149°F). While other display technologies may have broader operating ranges, 0° to 60°C encompasses most

of the range in which a device with a display might be viewed by an operator.

#### WHAT ABOUT LIFE PROJECTIONS?

When choosing a supplier of LCDs, the buyer should not hesitate to request and review real-time life data. The buyer should be cautious, however, when claims for 20,000 or 30,000 plus hours of actual life are being presented. If an LCD manufacturer is keeping up with technology, he is continually implementing new or improved materials, life testing of these materials must be started over again, and consequently, it is impossible to have any large number of test hours accumulated. Instead, what is most important is to review the *trends* in life data -- is the manufacturer improving?

When dealing with a reputable manufacturer, you may find a standard "one year from date of shipment" warranty. *This is not unusual among component companies, and does not mean that the display is going to fail immediately after the one year.* Since valid life data takes time to accumulate, you should be more interested in the characteristics of the materials being used, and what trends, if any, are showing up in actual life testing. Also, you need to know *what the design goal is for projected life, and does the company have the data to support advancements being made towards that design goal?* AMI, for example, guarantees displays for two years from date of shipment, however we have a 50,000 hours (6 years) design goal as a minimum, and data from real-life testing leads us to believe that projected life over 50,000 hours, when the display is properly driven, is certainly possible in the future.



# Watch Displays

The drawings on the following pages represent some of the more popular watch display configurations made by AMI. For detailed specifications request data sheets from your nearest AMI Sales Office.

All AMI watch displays utilize highly stable moisture insensitive liquid crystal materials and all will operate reliably at 3Vac drive.

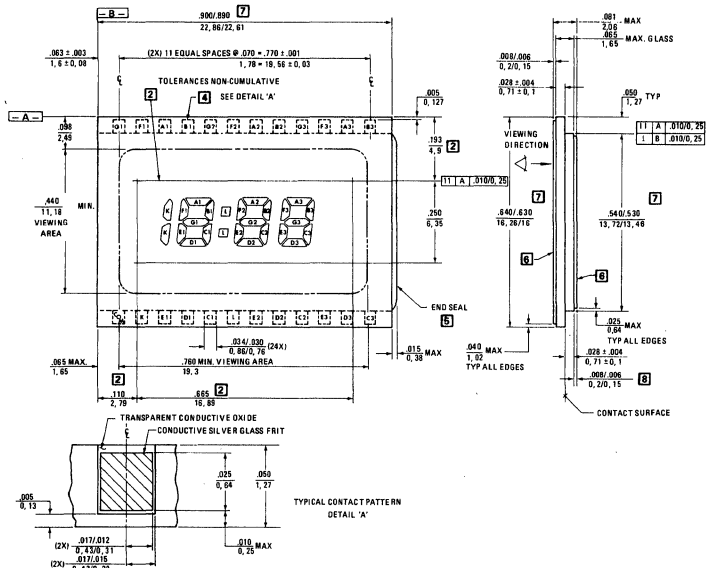
## D8151A Series

FONT STYLE



Digits are 0.250 in. (6,35) high

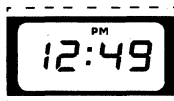
(Above is actual size)



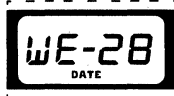
MINIMUM VIEWING AREA: 0.760 x 0.440 in.

## D8154A Series

FONT STYLE



TIME

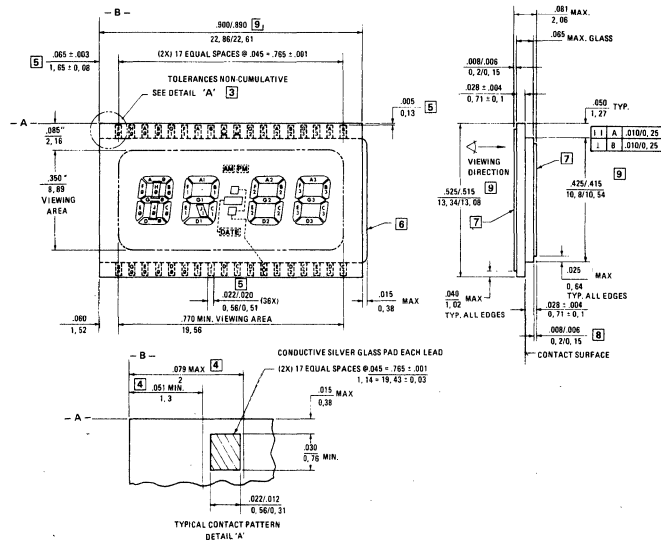


DAY-DATE



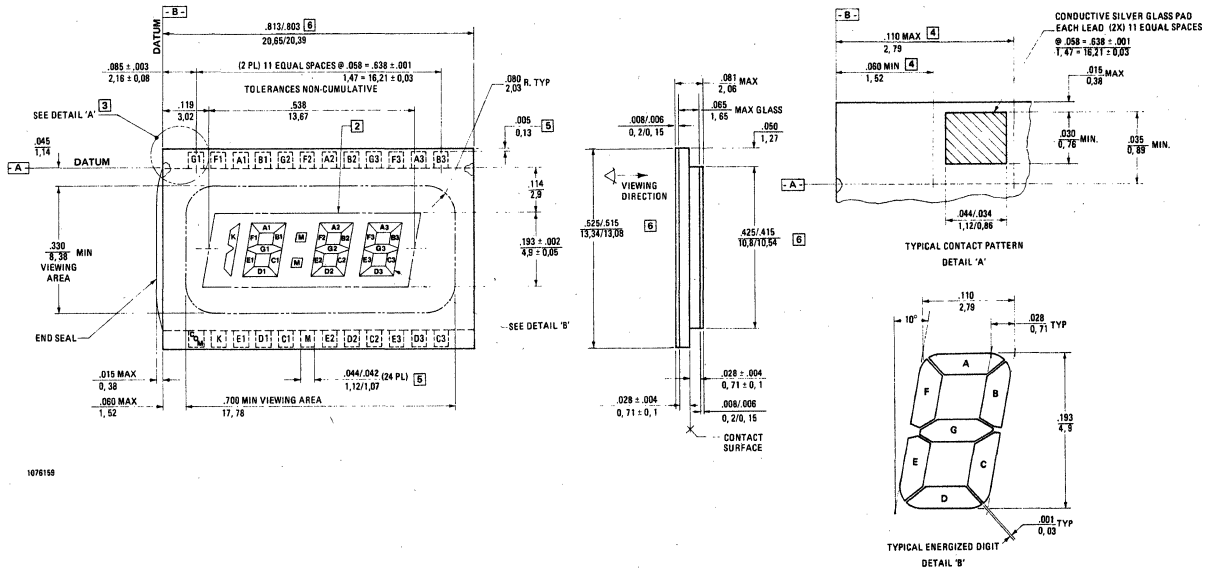
MONTH-DATE

(Above are actual size)



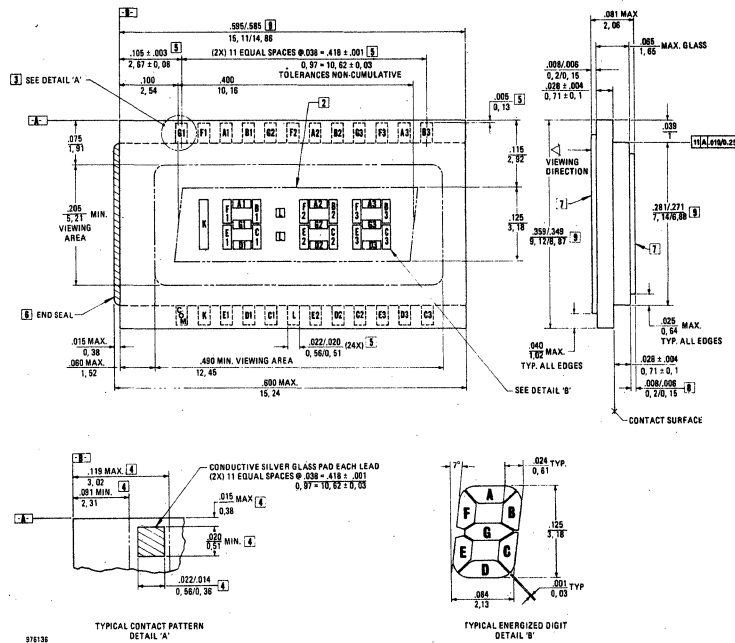
MINIMUM VIEWING AREA: 0.770 x 0.350 in.

# D8158A Series



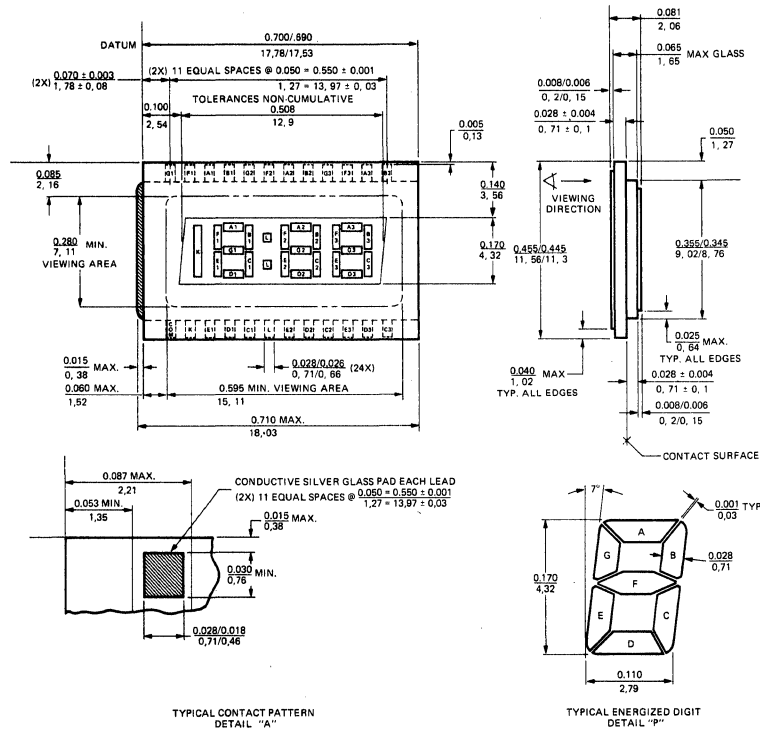
MINIMUM VIEWING AREA: 0.700 x 0.330 in. (17, 78mm x 8, 38mm)

# D8159A Series



MINIMUM VIEWING AREA: 0.490 x 0.205 in. (12, 45mm x 5, 21mm)

## D81XX Series



## AMI Custom LCDs

AMI Display Systems has full design and manufacturing capabilities for custom LCD displays and welcomes your inquiries. Our applications engineering staff is prepared to assist in defining your display needs and then will design original artwork according to your digit configuration, display size and reflector (if needed) requirements. Our manufacturing facilities

can handle large or small production runs, under rigid quality assurance controls.

Contact AMI Display Systems Marketing Department for further information.

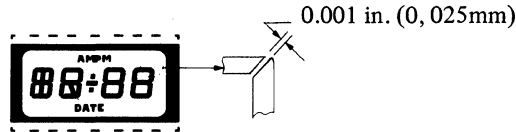


# AEA Process Displays

AMI Display Systems has introduced a new LCD manufacturing technique that dramatically improves the aesthetics of liquid crystal watch displays. This technique – the AEA Process – eliminates the need for a large gap (0.004 to 0.008 in) between adjoining segments of seven segment displays and instead, yields displays with only a 0.001 in space. It is a state-of-the-art proprietary process that allows AMI to manufacture watch displays far superior in this viewing quality to any others in the industry.

At a time when LCD watches are rapidly growing in popularity and many new models are appearing, AEA Process Displays can significantly enhance the appearance of your ladies and men's watches.

AMI can deliver these new high quality AEA Process Displays in watch-size displays described in this catalog, with any number of standard or custom digits and annunciators.



When the display is energized, segments appear to the eye to be continuous instead of broken.

## Prototype Fee and Delivery Information:

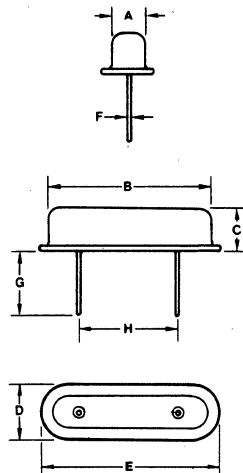
Existing AMI Glass Size and Pin-outs, Custom  
 Digit Artwork . . . . . \$1,400.00  
 Existing AMI Glass Size, Custom Pin-outs and  
 Digit Artwork . . . . . \$2,000.00

Custom Glass Size and Artwork . . . . . \$8,000.00  
 (All prices are based on a minimum of 10 sample units)  
 Delivery Time to First Samples: minimum 6 weeks, maximum 10 weeks

# Quartz Crystals-32 KHz

**S23200 Series, S23210 Series, Model S23221** – The S23200 Family of quartz crystals is basically an X-Y flexure design, but with the added feature of *four-point suspension* for the quartz element, that provides maximum resistance to shock and vibration.

This family of 32 KHz devices can be provided in three basic frequency tolerance classifications: ±30 ppm (parts per million); ±50 ppm; ±100 ppm correlated to a certain C<sub>L</sub> (load capacitance).



DIM.	INCHES	mm
A – MAX	*0.120	3.05
B – MAX	0.472	11.99
C – MAX	0.123	3.12
D – MAX	0.170	4.32
E – MAX	0.520	13.21
F – MAX	**0.013	0.33
G – MIN	0.180	4.57
H – NOM	0.289	7.34

\*Max. 0.125 with dot mark  
 \*\*Max. 0.015 with solder

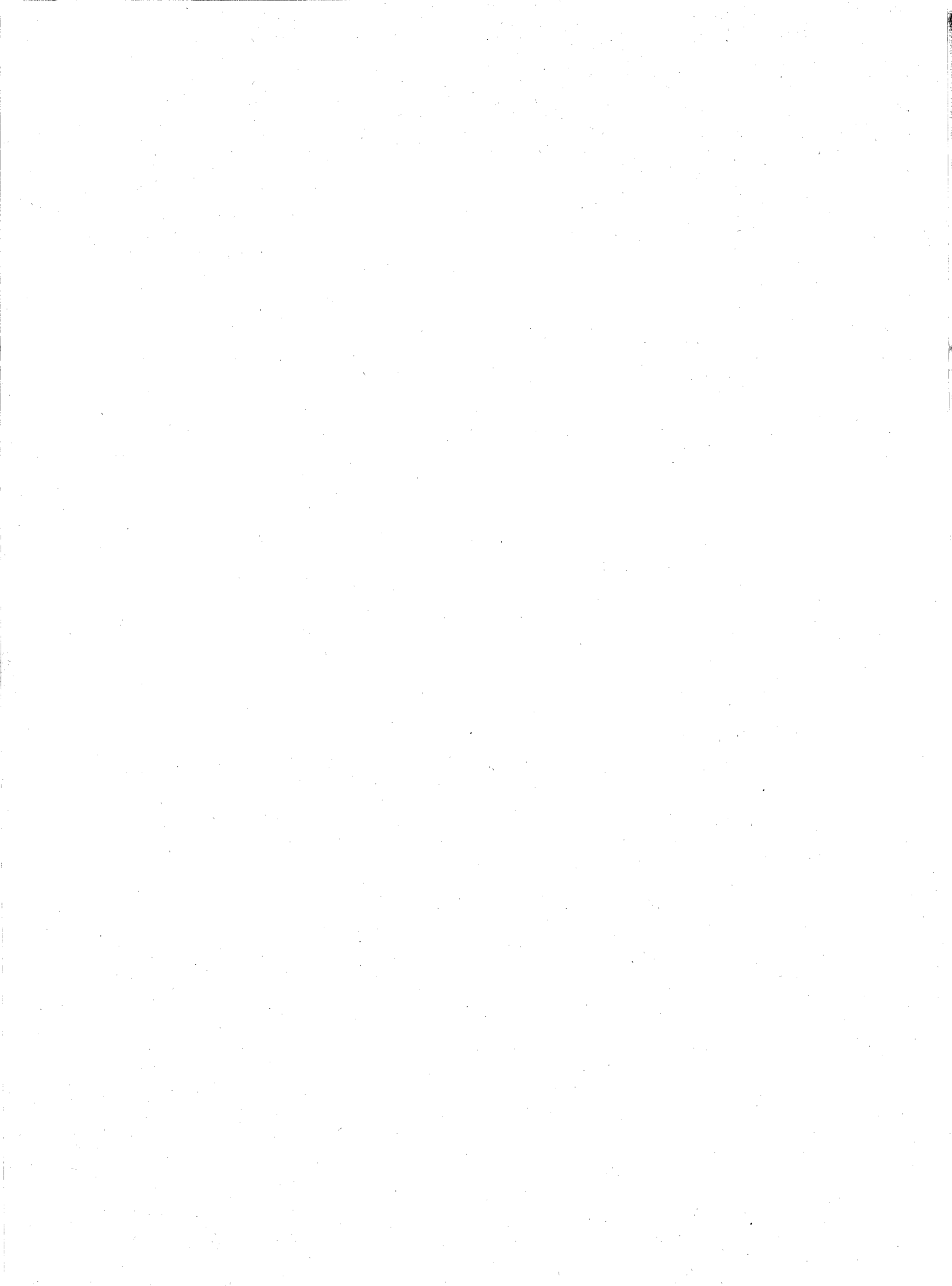


# 8

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## **Application Notes**





## Programming AMI S6834 and S5204A EPROMS

by David Erickson and Fred Mulholland

The versatility of ultraviolet light erasable PROMs has added a new dimension to system design. Custom and low volume systems can be economically programmed without the burden of mask charges and minimum order requirement of mask programmable ROMs. As EPROM uses spread, the demands for easier and quicker ways to program these devices also grows. AMI's EPROMs provide a solution to these needs by allowing the user to implement on-board programmability.

The design of the AMI S6834 and S5204 has been done in such a way that only one pin ( $V_{prog}$ ) needs to be biased at the programming voltage (-50 volts); the rest remain at TTL levels (I will hereafter only refer to the S6834 but the same rules apply to the S5204). This allows the user to do all selection and address/data logic at TTL levels, while preparing to program the EPROMs. This is a feature not found on other EPROMs, which variously require that data, address, and chip select pins alike be biased for programming. For example, the address and data line must be switched to -48 volts to program the Intel 1702 EPROM and likewise for the National 5204 EPROM data lines require a special programming voltage. In case of Intel's 2704/2708 EPROMs the chip select lines require special voltages. Thus, AMI EPROMs stand alone in programming simplicity. (Users of the AMI S5204 should note that if a National 5204 part is put into a programmer designed

for the AMI S5204 it will not program, because the data lines remain at TTL levels.)

### ON-BOARD PROGRAMMING

There are some important aspects of system design that must be remembered when attempting to implement on-board programming. These requirements may demand some design constraints that often make it advisable to provide a separate programming socket for the EPROMs.

Programming specifications for the S6834 require that there be a minimum time duration programming pulse. The gate charge is deposited in the gate region for the selected address during the first few (3 to 5) milliseconds of each pulse, but approximately 60 milliseconds of charge time is required to permanently charge the gate for memory retention. Since, for example, the S6800 microprocessor is a dynamic device, data and address timing in other circuits on the board is much faster than the 3 to 5 milliseconds required for EPROM programming.

Thus, the first consideration for on-board programming is that of providing latches for address and data retention while programming. Figure 1 shows how this may be accomplished in a microprocessor system. With the extra latching the

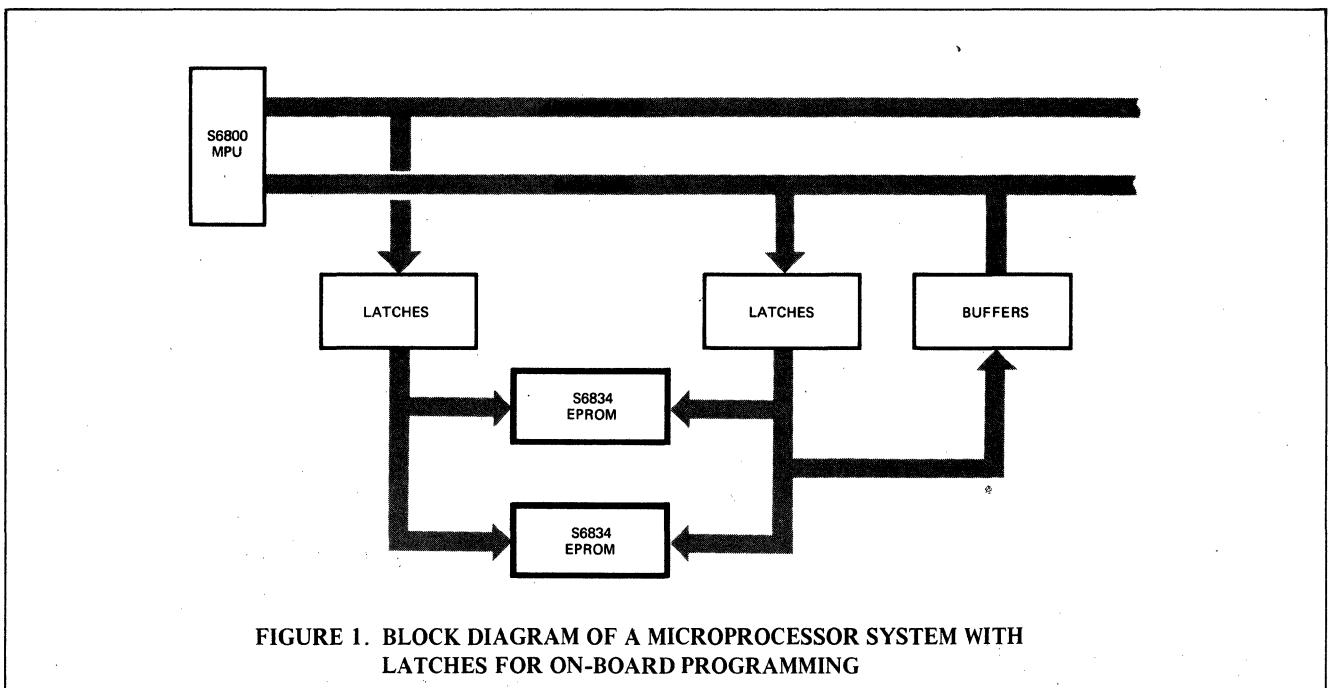


FIGURE 1. BLOCK DIAGRAM OF A MICROPROCESSOR SYSTEM WITH LATCHES FOR ON-BOARD PROGRAMMING

system clocks must be slowed down to allow data and address propagation through the EPROM latches. This, however, may be limited only to EPROM access cycles by using additional clock control circuitry and address traps.

Another precaution necessary for on-board programming is the layout of the high potential (-50 Vdc) programming line ( $V_{prog}$ ) to access all the EPROM chips. If any other lines are close, a small sliver or splash of solder may destroy many MOS or TTL circuits before it is found. Therefore, it is safer to keep the high potential localized to one small area of the board and thus minimize high voltage exposure of the other circuits.

The programming voltage may be bussed to the  $V_{prog}$  pin of each EPROM socket and pulsed by way of a transistor from the EPROM control circuits. Figure 2 shows how the  $V_{prog}$  line may be connected. Selection is achieved by enabling the CS line for each particular EPROM being programmed.

On-board programming offers major cost savings, however, and justification for the extra circuitry may be easily demonstrated. J.J. McDowell<sup>(1)</sup> has pointed out the following areas of cost savings:

1. A reduction of part numbers
2. Elimination of special field marking for parts
3. Elimination of assembly errors caused by placement of reprogrammed individual EPROMs in wrong slots.

<sup>(1)</sup>J.J. McDowell, "Program Erasable PROMs," *Electronic Design*, Vol. 24, No. 12, June 7, 1976.

<sup>(2)</sup>See also AMI EVK300 *Prototyping Board Manual*.

4. A reduction in RPOM handling.
5. A reduction in tape handling.
6. Quicker and easier field updates.

#### DEDICATED-SOCKET PROGRAMMING

A viable alternative to on-board programming is that of using a dedicated socket for EPROM programming. This is the approach used on the AMI EVK 300 Prototyping Board. It overcomes the two major problems of data line latches and voltage distribution, noted under on-board programming.<sup>(2)</sup>

Figure 3 shows a block diagram of how dedicated-socket programming is implemented. The address and data are latched in the S6820 PIA dedicated to the S6834 programming socket. To program an EPROM, the S6800 writes the address and data into the PIA registers, turns on the WRITE line and pulses the  $V_{prog}$  line via an external control signal. Two timing pulses (1 ms and 100  $\mu$ s) are used on the AMI EVK 300 board to allow the processor to determine when the charge time has reached its specified duration.

There may be penalties in using a dedicated socket, however. Most obvious is the added circuit board space required for the programming circuitry. Besides the socket itself, a 40-pin PIA timing divider (three TTL DIPs) and related transistor driver hardware are all needed. On the other hand, these parts can also be put to other uses. For example, the timing circuit is always present and may be used as a general purpose interval timer. The PIA (EPROM socket) may be connected to an edge connector and used as a general purpose PIA, when not programming an EPROM (the PIA is really not 100% dedicated). But remember that the CA1 and CB1 lines (Interval Timer) are not available in this case. This also allows the socket to be remotely located, away from the board itself. So, even the penalty of added real estate may be used to an advantage.

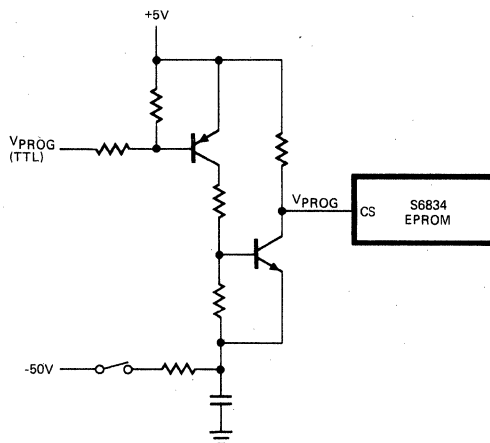
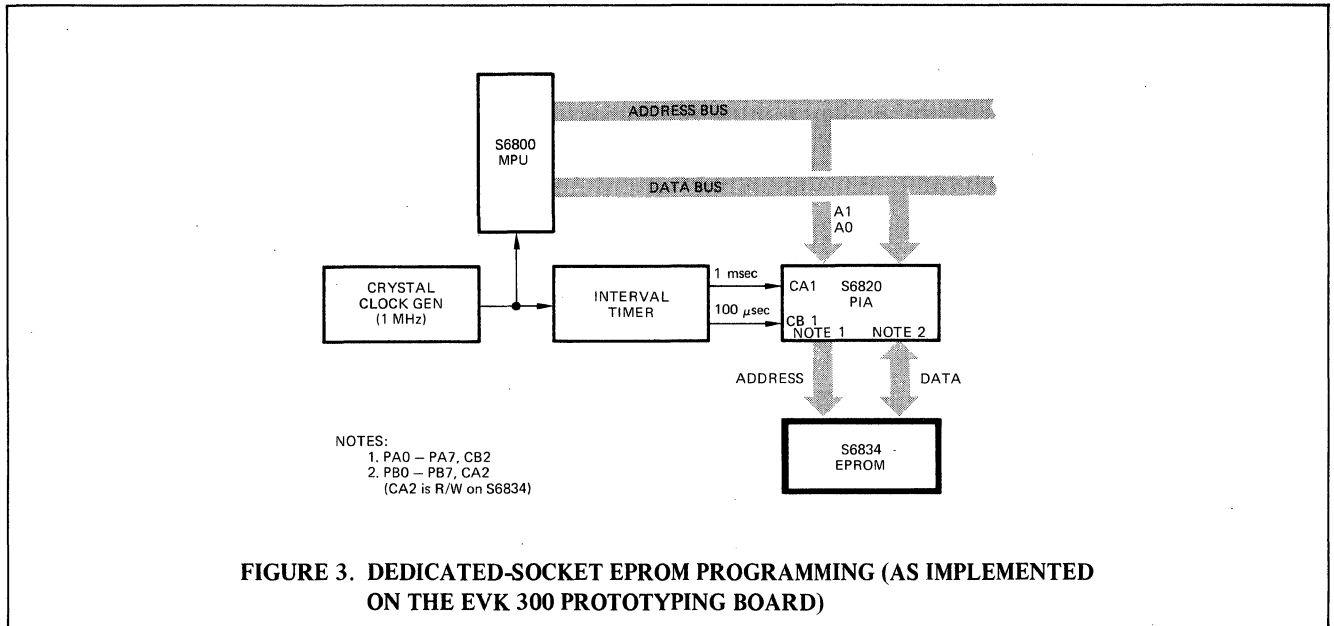


FIGURE 2. EPROM PROGRAMMING CIRCUIT (SHOWING HOW THE  $V_{prog}$  PIN MAY BE DRIVEN)



## OTHER ALTERNATIVES

As already mentioned, the EVK 300 already has an EPROM programmer for S6834s, with the program controller operational on the board. Also, the AMI S6800 MDC 100 can program both S6834 and S5204 EPROMs. On either of these devices programming EPROMs is a matter of following the

simple instructions provided and is the quickest way to program for anyone who does not wish to design a program of his own. Another source of commercially available programmers is Data I/O Corp. which now has the personality cards to program AMI EPROMs. In an occasional emergency, AMI will program a small number of EPROMs for a nominal fee.

## MOS Circuits for Electronic Organs

by Ridge Cotton

### INTRODUCTION

Music has always been a reflection of culture, and strangely enough, a rather accurate indication of the technological sophistication of a group, or period. Most of the earliest music depended almost entirely on rhythm, and it is not a coincidence that "primitive" music used simple rhythm instruments. These instruments were the only ones available.

With time, and accompanying sophistication, techniques for producing string, woodwind, and brass musical instruments developed and also with time, have been improved. It is only natural that electronic methods for the production of music would appear. The electronic organ is probably one of the most outstanding examples of electronically produced music, and the development of the electronic organ mirrors the developments that have occurred in electrical technology.

Early vacuum tube organs were replaced by solid state organs as transistors became available. Now, integrated circuits, specifically, MOS/LSI circuits, are a dominant factor in electronic music. One reason is the ability of MOS technology to produce circuits for accurate tone generation, eliminating the need for repeated tuning -- and circuits for rhythm patterns, enhancing the sound of the organ by simulating drums and other basic percussion instruments.

At the present time, there are as many different approaches to the design of an electronic organ as there are organ manufacturers. However, there are certain elements basic to almost any electronic organ system.

### TONE GENERATION

Musical tones occur in groups of twelve, called octaves. Since the frequency of any tone in an octave is exactly half the frequency of the corresponding tone in the adjacent, higher octave, typical modern electronic organs first generate the 12 frequencies in the top octave. The remaining tones are obtained easily with binary dividers. For example, an organ producing 96 tones requires the 12 top octave frequencies and 84 binary dividers. The block diagram of a typical electronic organ in Figure 1 exhibits this approach.

### KEYING

Once the tones have been generated, some form of keying is required to switch the appropriate tones to the filters after the musician has selected the tone at the manuals or pedals. One of two basic keying approaches, ac or dc, is generally used.

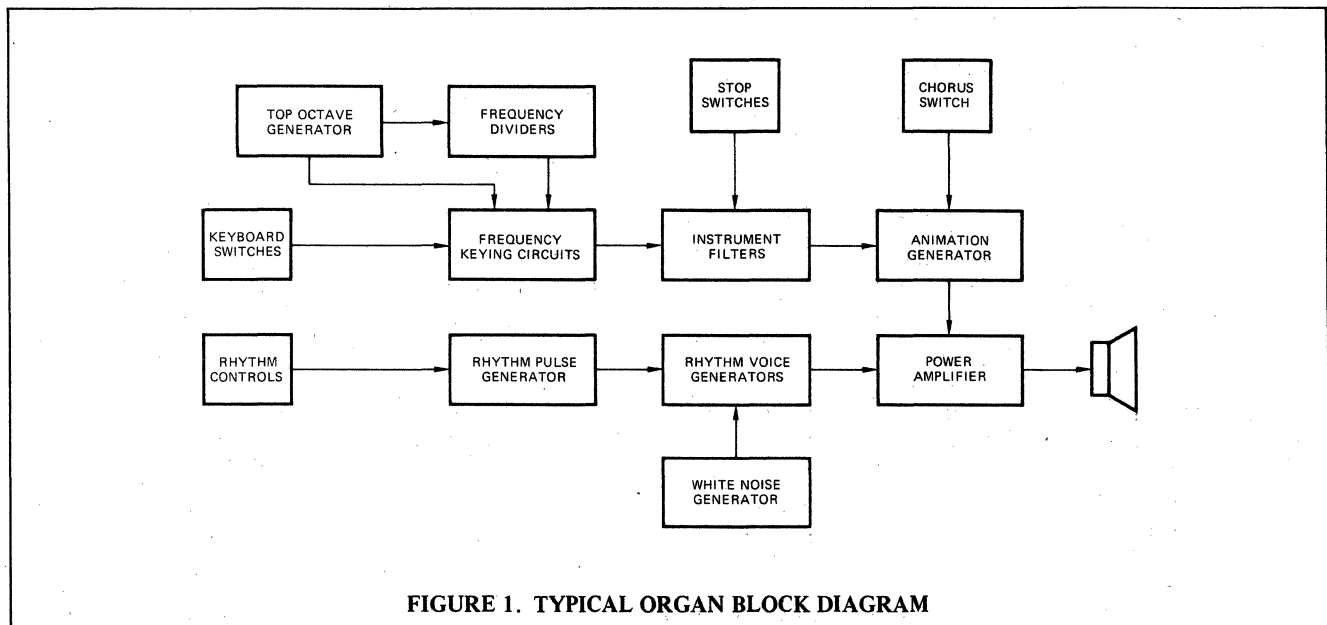


FIGURE 1. TYPICAL ORGAN BLOCK DIAGRAM

### FILTERING

Filters are used to shape the tone waveforms to simulate the various voices of the organ -- flute, trumpet, etc. The signals are then mixed, amplified, and routed to the organ speaker. Volume is controlled by a swell pedal which attenuates the signals entering the amplifier.

### ANIMATION

Because electronic music can have a tendency to sound dull or lifeless, it is desirable to add more depth to the sound. This can be achieved by various types of circuitry located somewhere between the filter outputs and the power amplifier. Because these circuits add "life" to the music, much as stereo adds "life" to mono, they are often called animation circuits.

### RHYTHM

In addition to these areas electronic rhythm generators are becoming increasingly popular. Although not essential to an electronic organ, they now appear in varying degrees of complexity in most electronic organs being produced. Rhythm generators enhance the music by creating the illusion of a drum, and also help the organist maintain tempo.

### TOP OCTAVE GENERATOR

Because all musical frequencies are exactly half of corresponding frequencies in the next highest octave, it is beneficial to generate the 12 frequencies of the highest, or top, octave. Generation of the top 12 frequencies in an electronic organ can be accomplished several different ways. The most obvious method uses 12 independent oscillators. The major disadvantage of this approach is high initial labor cost for tuning. In addition, the oscillators can change frequency with time, requiring further organ tuning at varying intervals. The AMI top octave generators S50240, S50241, and S50242, eliminate both of these difficulties by dividing a single master frequency by 12 parallel divider chains; their outputs are the 12 top octave frequencies. This approach generates the top octave with a high degree of accuracy ( $\pm 1.1\%$  error on all frequencies).

### DIVIDER TONE GENERATOR

After the top octave frequencies have been generated, the remaining octave tones are obtained with binary dividers, such as the newly introduced S10129/30/31 six and seven stage divider circuits.

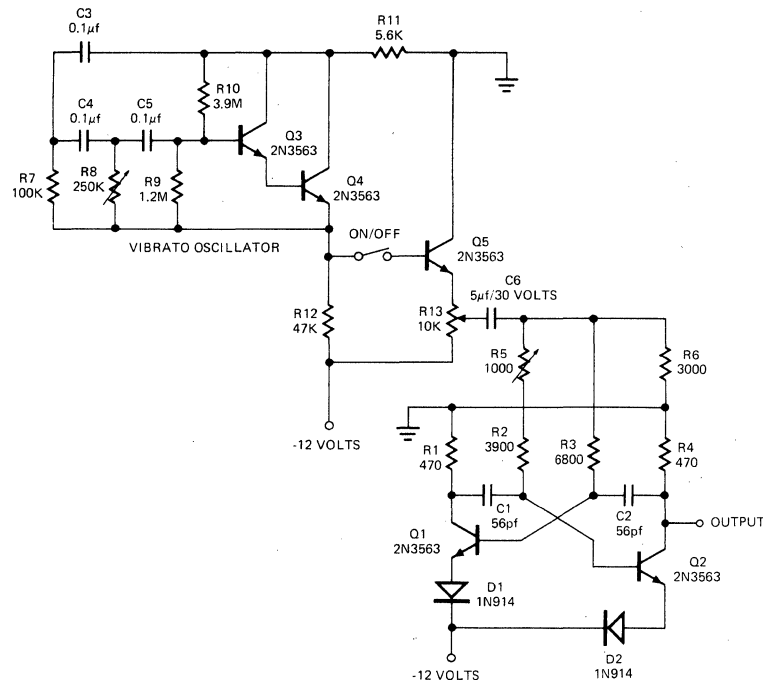


FIGURE 2. TYPICAL MASTER OSCILLATOR AND VIBRATO GENERATOR

A typical organ, Figure 1, requires the generation of seven octaves, or 84 frequencies. The organ shown in Figure 1 could use either 14 six-stage dividers (10131) or 12 seven-stage dividers (10129). It is also feasible to use the 12 top octave generator frequencies in place of the 12 highest frequency divider outputs. In this case, the organ could be built with only 12 six-stage dividers.

Another typical divider application is shown later in Figure 9. This three-octave "toy" organ uses S2193 dividers. It is relatively easy to build, requiring only a low-current (<100 mA) power supply, a power amplifier, and a speaker.

### KEYING

With ac keying, Figure 3, frequencies from the tone generator pass directly through the keyboard switches to the bus outputs. As a result, annoying "key clicks" occur when the key switch is closed because the tone signal is applied instantly to the ac bus. Also, with ac keying, desirable

"sustain" of musical notes cannot be obtained because the tone signal is removed instantly once the key switch is opened. In other words, musical notes "click" on when selected, and cannot linger unless the organist holds a finger or a foot on the selected key or pedal.

However, ac keying is often desirable because of lower costs. If the organ is a simpler, basic musical instrument, ac keying is tolerable from both cost and aesthetic viewpoints. As the organ develops sophistication, ac keying loses its advantage. Consider, for example, the organ in Figure 3. This organ requires more pitches, or "footages," because the upper manual supplies both 8' and 4' pitches. With ac keying, another set of contacts is required for each additional footage. If additional 16', 2', and 1' pitch outputs were also desired, the total number of contacts per key would reach five. Obviously, the economic advantages of ac keying decrease under these circumstances.

With dc keying, a single contact key switch can control any number of output pitches. Also, "key click" is eliminated, and the desirable "sustain" feature is possible. Figure 4 shows a

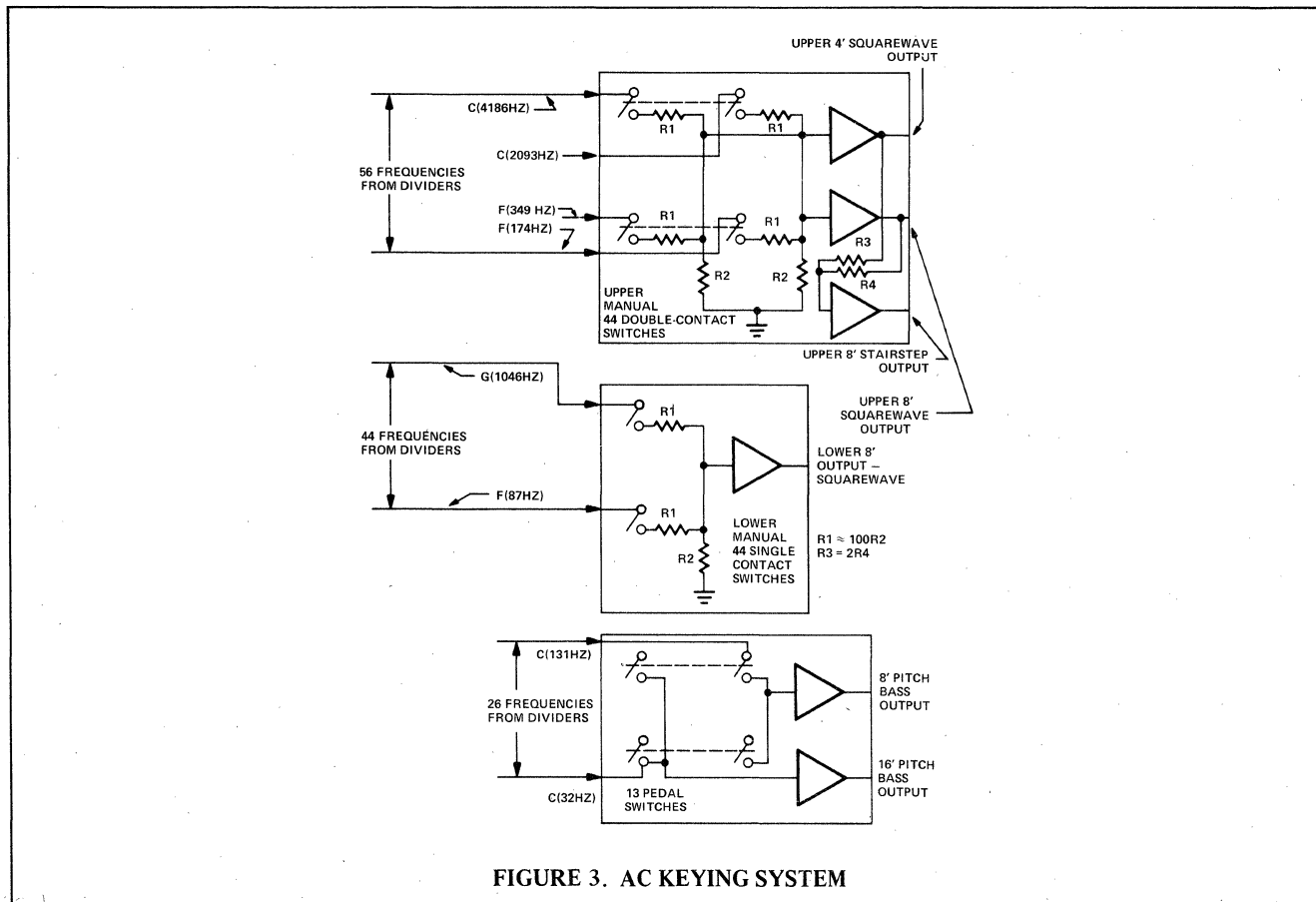


FIGURE 3. AC KEYING SYSTEM

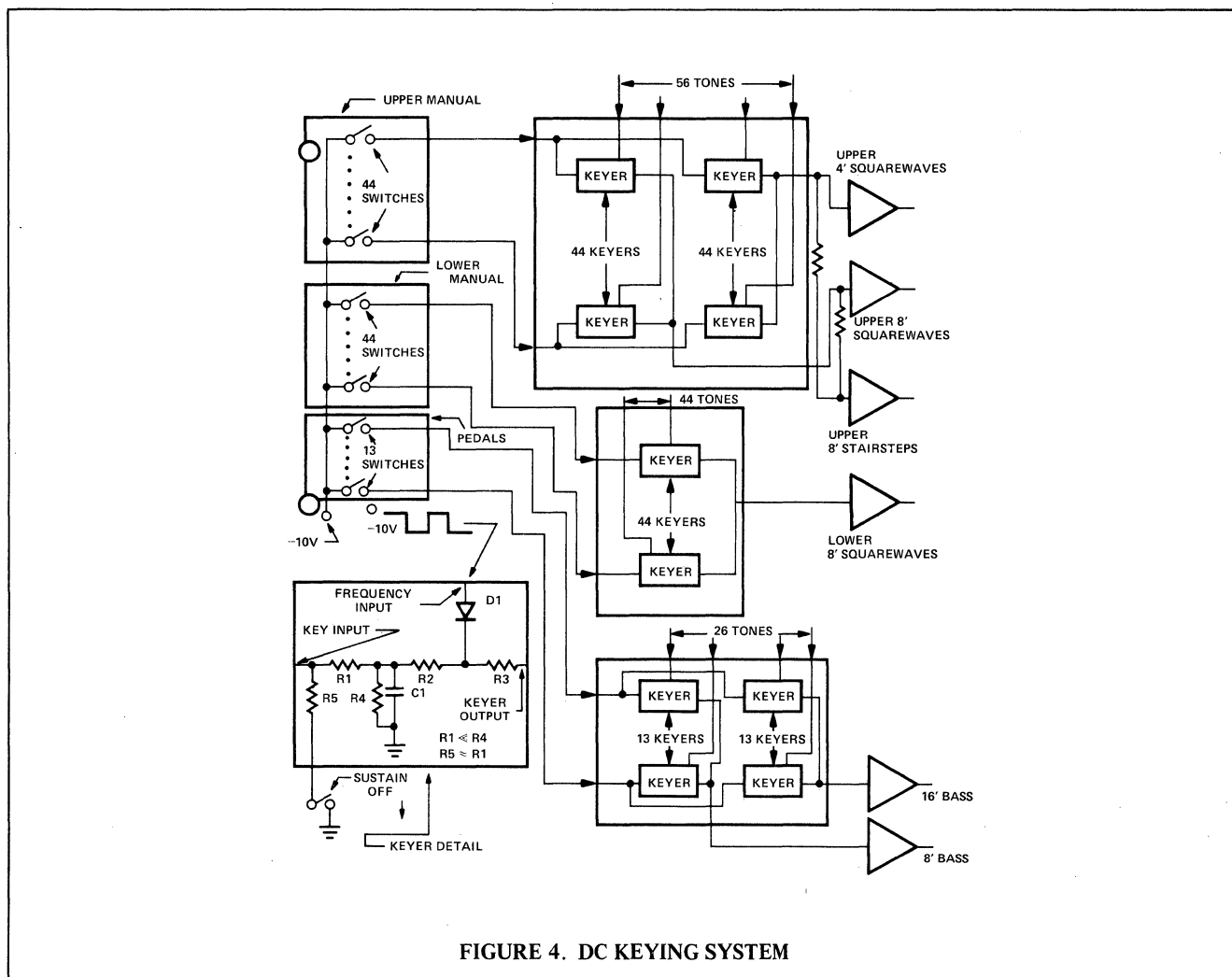


FIGURE 4. DC KEYING SYSTEM

dc keying system. If you check the keyer detail exploded view, you will note that the appropriate frequency is applied constantly to diode D1, normally back-biased. When the key contact is closed, a negative potential is applied to the key input, causing C1 to charge up relatively fast. This forward biases D1 and applies the signal to the bus. The charging time constant of C1 + R1 eliminates "key click," and when the key is released, C1 discharges through R4. This causes the ac signal to decay slowly, obtaining "sustain." If R5 is grounded, C1 discharges much faster, eliminating long sustain.

### MOS KEYING

Many of the disadvantages of ac keying are more than adequately eliminated by dc keying. However, the addition of "footages" or pitches requires an additional set of diode keyers for each pitch when using dc keying, much the same as

ac keying requires additional sets of contacts. But, with dc keying, there is an attractive alternative. As shown in Figure 5, a large number of dc keyers can be included on one MOS/IC chip, significantly reducing the number of components required for additional pitches. In addition, MOS dividers can be incorporated on the same keyer chip, eliminating the need for separate divider packages.

The result — an electronic organ keying system which works with only one top octave generator system, one key switch per key, and provides 16', 8', 4', 2', and 1' pitch outputs. Thus, it proves cost-effective in many electronic organ designs to replace standard IC divider packages and discrete diode keyer circuits with MOS/LSI systems. The high complexity of such MOS divider-keyer systems, combined with the widely varying musical requirements of the increasingly large number of organ models available, make the design of a standard MOS keyer product impractical. Such an attempt

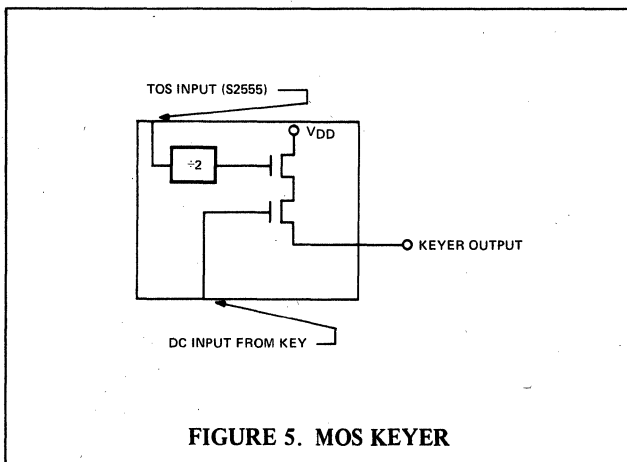


FIGURE 5. MOS KEYER

could result in a new "standard" product for each new organ model. A solution is to obtain a custom MOS/LSI circuit designed specifically for a particular organ model or line of models.

**FILTERING**

After an electronic organ generates the required frequencies and incorporates a keying system for selection of those tones, it must then offer a filtering mechanism to simulate the various classes of musical instrument sounds -- string, brass, flutes, etc. These are known as "voices" and are selected by activating switches called "stops." Three typical voice filters are illustrated in Figure 6. The component values are not listed because they depend on the specific voice to be simulated.

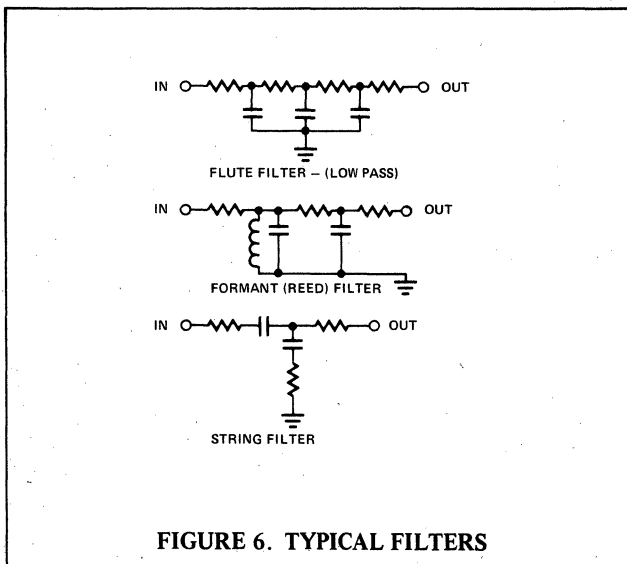


FIGURE 6. TYPICAL FILTERS

Of the many harmonics contained in the input waveforms, the filters must pass only those which are relevant to the voice desired, and certain waveforms are more suitable for filtering than others, depending on the voice to be imitated. A low pass flute filter, for example, attempts to pass only the fundamental sinewave. (Flutes actually possess more harmonics, but, generally, electronic organs tend to have flute voices made of sinewaves.) A squarewave is the best type of waveform input for this filter, because it contains no second harmonics, and the filter has only to suppress third harmonics and above to achieve the sinewave. The hallow sound produced by a square waveform makes it useful for producing the clarinet voice, also.

Even though a squarewave is ideal for producing flute and clarinet voices, it is useless for reed voices, since these sounds require a full set of harmonics, even as well as odd. A squarewave input to a reed filter produces an unpleasant, hallow musical result. Stairstepping approaches are often used to generate a waveform with all harmonics. Stairstepping is a process which adds octaves of squarewaves to approximate a sawtooth waveform. The sawtooth waveform approximation improves with the addition of more octaves. Referring back to Figures 3 and 4, a stairstepping method was used to add the 4' and 8' output busses to obtain an 8' stairstep. An obvious advantage of this method is the very small number of components involved. The disadvantage lies in the musical result since the 8' stairstepped output contains only two octaves, whereas three or even four would be musically superior. Further, the 4' output is not stairstepped at all, and it would be impossible to obtain a stairstepped 4' output without adding either an additional set of contacts in an ac keying system, or an additional set of diode keyers in a dc keying system.

There are, fortunately, other methods of obtaining stairstepped waveforms, and Figure 7 illustrates an approach which obtains these stairstepped waveforms at the tone generation stage, prior to the keyer stage. This method provides additional steps in the waveform and, hence improved sound quality. However, it may require additional dividers and a large resistor network.

**ANIMATION**

When multiple frequencies are played simultaneously in an electronic organ, those which are octaves of each other are locked in phase. This can result in a somewhat lifeless quality to the music. To overcome the problem, various types of electronic phase shifting circuits can be placed between the voice filter outputs and the power amplifier. The analog shift register is a versatile MOS product that is now enjoying wide useage in these animation generating circuits.

The analog shift register, sometimes called a bucket brigade, operates in a manner similar to a digital shift register, except that analog (or audio) signal levels are applied to the



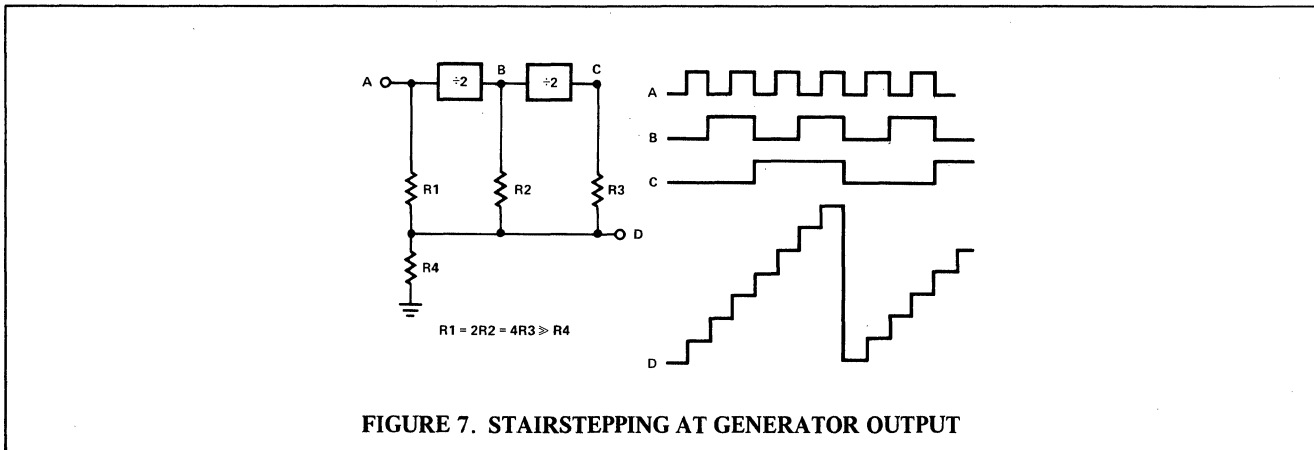


FIGURE 7. STAIRSTEPPING AT GENERATOR OUTPUT

input, delayed, and picked up at the output. AMI's S10110 analog register has 185 bits of delay and can be clocked at up to 500 KHz. Since audio signals may contain harmonics of up to 15 KHz, typically the lowest clock frequency applied to a bucket brigade is 30 KHz. By modulating the clock frequency, the engineer can use the S10110 to provide such animation effects on vibrato, string chorus generation, rotating speaker simulation, and echo production.

### RHYTHM

Rhythm generation adds to the music by simulating percussion instruments and by maintaining tempo for the organist. Relatively sophisticated rhythm systems have become practical in moderately priced organs because of the large storage capacity of a single MOS chip.

Basically, a rhythm system requires a rhythm generator device capable of producing several rhythm patterns for a given instrument and circuits which simulate the sounds of various rhythm instruments, see Figure 8.

Although the rhythm voice generators tend to be produced largely with discrete components, AMI's S2688 noise generator circuit is most useful in creating the effects of such instruments as cymbals, sandblock, snare drums and maracas. Fabricated in P-channel ion implanted MOS, the S2688 is a 17 bit shift register with exclusive OR feedback, designed to provide a constant output of white noise, which is necessary for creating these voices, as provided by AMI's S8890 and S9660 devices. The production of rhythm patterns often requires a minimum sequence length of 32 bits. A sequence length of 64 bits provides almost all rhythm patterns desirable. Eight to ten outputs, each capable of producing a 32 to 64-bit sequence, can simulate most of the common rhythm patterns.

Control terminals for altering the sequence at the outputs make it possible to program a read only memory in the

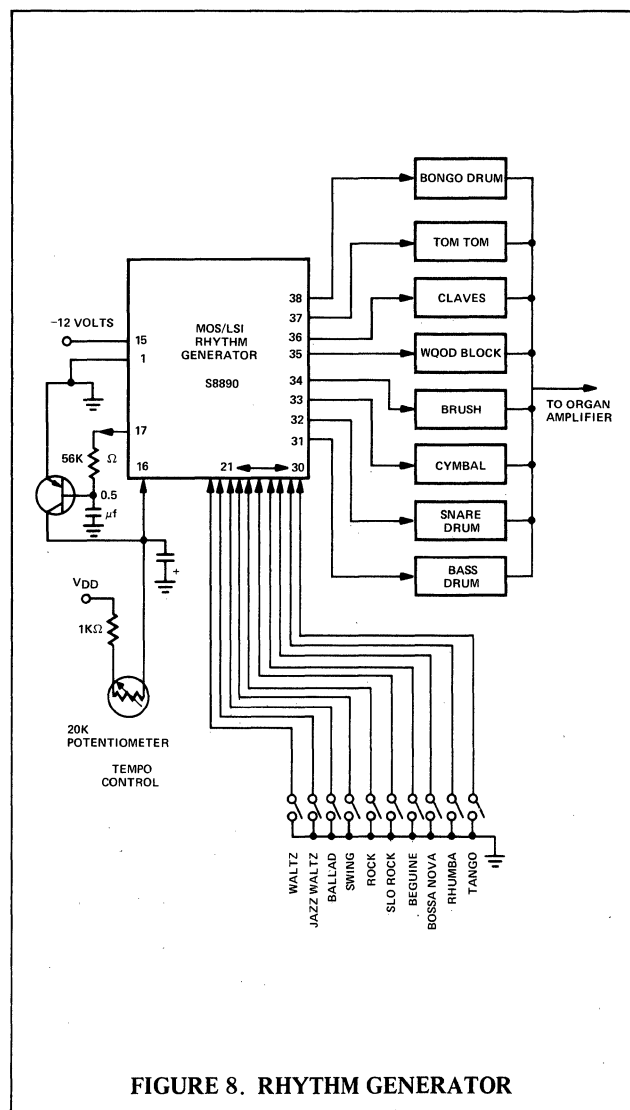


FIGURE 8. RHYTHM GENERATOR



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**AMI Custom MOS LSI**

### **WORLDWIDE FACILITIES OF AMI**

AMI, one of the world's largest designers and manufacturers of advanced MOS/LSI integrated circuits, has facilities in several major locations. Corporate headquarters are in Santa Clara, California, with 327,000 square feet of manufacturing and office space and over 1,500 employees. Administration, R&D majority of the engineering staff, engineering production line, one of two major wafer fabrication facilities, and a final test facility all are located in Santa Clara.

Another major fabrication facility is in Pocatello, Idaho, where there are 103,000 square feet of plant and some 400 employees. At this facility some engineering, assembly, and final test are performed.

In Inchon, Korea, is KMI — the major circuit assembly plant of AMI. It covers 116,000 square feet of floor space and employs about 1,700 persons.

A new assembly facility — TMI — has just been completed in Taichung, Taiwan. Initially it will be used for the assembly of liquid crystal displays, but later will expand into other products.

In Swindon, England a sizeable design engineering staff is dedicated to circuit development and applications support of AMI European customers.

# Custom Capabilities

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## WHAT ARE CUSTOM MOS/LSI MICROCIRCUITS?

AMI custom microcircuits are complex digital circuits designed to perform a specific function. Most could be described as "dedicated microprocessors". Because they are designed from scratch for a particular end product, custom microcircuits waste no space or capability, packing the maximum number of functions into the minimum area on the MOS/LSI chip. For volume applications, when compared with microprocessors, combinations of standard microcircuits, discrete electronic components, or electromechanical devices, custom microcircuits are often the most cost effective alternative.

No other company can match AMI's track record in developing state-of-the-art custom MOS circuits. Since 1966 AMI has been providing customers with circuits that have enhanced the marketability of their products by added features, continuously increasing reliability and reduced space requirements.

AMI not only has the experience but also the design engineering organization, and the technologically advanced production and testing facilities, to make the highest quality MOS/LSI circuits. Because AMI also manufactures standard, memory, and microprocessor products, all using a variety of advanced microcircuit process technologies, the company can be objective in helping customers determine their most cost effective approach. For example, AMI will participate in the design cycle of the custom circuit only to the extent needed by the customer. This ranges from zero to the complete design task.

With more than 1,000 custom devices designed and manufactured during the past 10 years, AMI has more experience than any other IC manufacturer in building a wide variety of custom microcircuits. The following are some of the products in which AMI custom circuits are being used:



## CONSUMER

- Oven/Range Controls
- Dryer Controls
- Juke Boxes
- Automotive

- Clocks
- Fuel Injection
- Ignition Systems
- Speed Controls
- Anti-Skid Braking
- Radio Functions

- Television Tuners
- HiFi Tuners
- Video Games
- Citizen Band Radio
- Garage Door Openers
- Burglar Alarms
- Water Sprinkler Controls

## BUSINESS

- Business Calculators
- Scientific Calculators
- Printing Calculators
- Coin Changers
- Vending Machines

## COMMUNICATIONS/NAVIGATION

- Facsimile Transmission Systems
- Data Modems
- Switching Systems
- Telephone Equipment
- Police Band Radio

## INDUSTRIAL/INSTRUMENTATION

- Industrial Timers
- X-Y Plotters
- Environmental Controls
- Medical Monitoring Equipment
- Digital Thermometers

## GOVERNMENT/MILITARY

- Secure Communication Links
- IMP Satellite
- Lunar Lander
- Viking Mars Lander
- Inertial Guidance Computers
- Sonobuoys

## TERMINAL/PERIPHERAL

- Point-of-Sale Terminals
- Fast Line Printers
- Keyboard Scanner
- Code Converters
- Character Generators
- Credit Card Verification System

## THE CUSTOM MOS/LSI DECISION

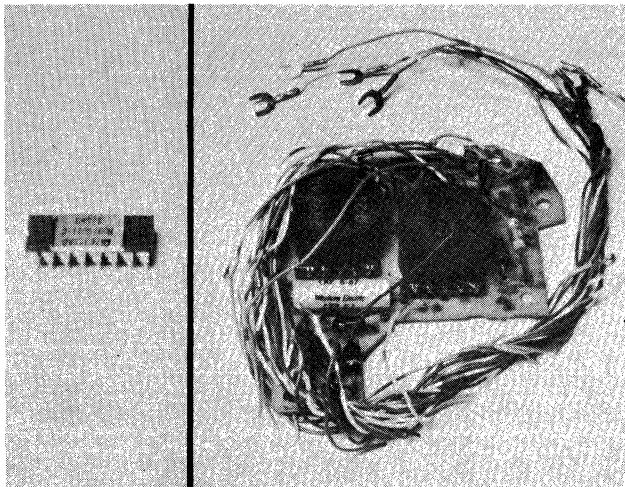
How do you know if custom circuits are right for you?

There are four general considerations involved in the choice between custom and standard MOS/LSI circuits:

- circuit complexity,
- economy,
- digital content,
- need for confidentiality.

An application suitable for custom circuitry is usually one requiring moderately complex circuit functions -- i.e., more than 100 logic gates. Fewer gates than this, in most cases, will not justify the extensive engineering, design and manufacturing effort required for custom circuit development. Less complex functions can be implemented economically with standard MSI and SSI components.

With increasing function complexity problems of space, heat dissipation, power supply size, interconnections and reliability usually develop. In such cases custom design circuits often offer performance, cost and reliability advantages.



Because of the custom circuit development and design costs, there must be sufficient production volume to amortize the initial outlay over the life of the product. Generally, with two year volume of more than 35,000 units, the use of an AMI-designed custom circuit begins to become cost-effective. If a customer designs his own circuit and AMI manufactures it from the resultant tooling, volumes as low as 5,000 or 10,000 can become economically practical.

Another important consideration affecting cost is the number of components in a system, eliminated by the substitution of a single custom circuit. A reduction in component count significantly reduces the number of electrical interconnections, lowers manufacturing costs, and increases

product reliability. Improved reliability reduces troubleshooting problems at the board, subsystem, and system levels, minimizes field repairs, and usually reduces warranty problems. The reduction of components also decreases assembly, initial checkout, and inventory costs.

A third factor affecting the custom circuit decision is the adaptability of the required functions to digital design. MOS/LSI circuits are highly efficient in decision-making or controlling functions, but some functions cannot be best resolved digitally and require analog circuitry. The importance of this factor, however, is diminishing as new custom circuit designs increasingly enable analog functions to be performed by digital circuits.

A final consideration of importance in a competitive environment is confidentiality of design. AMI is sensitive to this requirement and treats the creation of each circuit as a highly proprietary project, insuring complete security all through design and manufacture.

## ALTERNATIVES TO CUSTOM . . .

- **Electromechanical Controls.** These suffer in comparison with MOS circuits in three respects: reliability, because of moving parts and contact wear; design in convenience, because they require greater space; functional limitations, when there is a need to perform highly complex tasks.

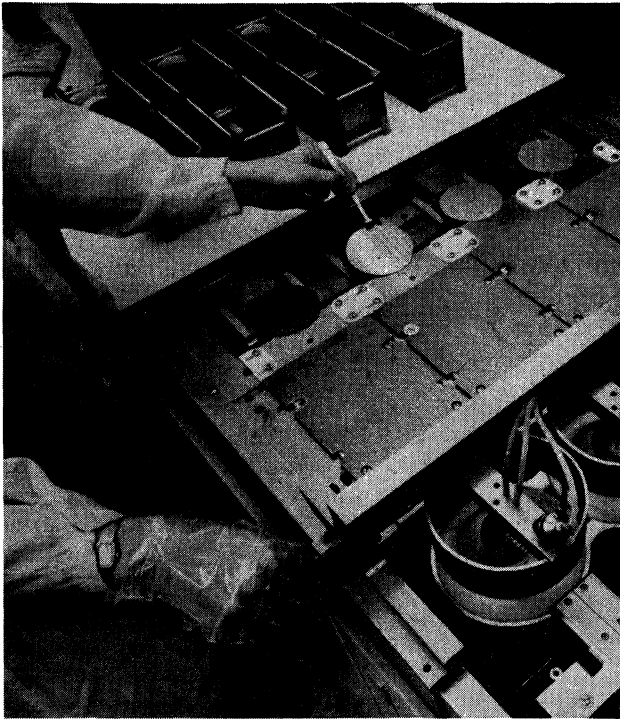
- **Hardwired Logic.** This alternative uses discrete electronic components interconnected to form logic blocks. Production is generally more expensive, due to the high cost of labor and materials involved, and a great deal more space is required. Power requirements far exceed those of an equivalent MOS circuit.

- **Standard Circuits.** The use of standard microcircuits to perform the same functions as a custom device often requires many components, additional assembly costs, more power and space, with a resulting drop in reliability.

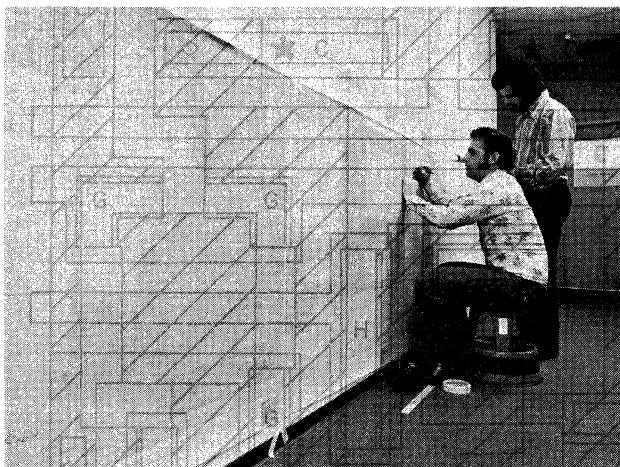
- **Microprocessors.** The AMI 6800 microprocessor family is ideal for lower volume applications, requiring the computing power and programmability of a computer. Using a standard microprocessor entails several microcircuits, and much of the combined capability may not actually be used in the application. A custom circuit, on the other hand, can incorporate only the necessary functions—onto one chip—thus conserving cost and space.

## COST AND RISK IN USING CUSTOM CIRCUITS

Costs of custom circuits vary widely, depending on the complexity of the design. But they may not be as high as generally believed, and current trends indicate a continuing decrease. The plot below gives some guidelines for comparing custom circuits with standard microprocessors.



The cost of designing and manufacturing a custom circuit must be weighed against the many benefits, all of which can be reduced to dollar savings. For example, by placing more functions on a single chip and reducing the need for other components, product assembly costs are reduced, along with inventory requirements. Reliability is improved and with it, labor costs for servicing and warranty repair. A reduced component count can mean a smaller product (requiring less material), lowered shipping costs and easier handling, reduced power consumption, and improved maintainability. All these also enhance product marketability.



Risks in going custom are minimal because of AMI's comprehensive quality assurance and testing program. Breadboarding and/or computer simulation of the circuit logic are used by AMI to fully debug the circuit before production begins. In the early design stages AMI test engineers review the design to make sure the circuit can be adequately and economically tested. Prototypes are provided to customers for their evaluation and approval before production begins. And once production starts, AMI maintains a complete lot traceability system as part of the quality assurance program. Dual fabrication assembly facilities assure uninterrupted supply of product.

#### HOW AMI WORKS WITH ITS CUSTOMERS TO PRODUCE CUSTOM MICROCIRCUITS

There are two ways AMI usually teams up with its customers:

- AMI designs and manufactures the circuit to meet customer requirements, or
- the customer designs the circuit, with AMI assistance, and AMI manufactures.

In addition, AMI is flexible in making other special arrangements.

#### THE TOTAL AMI APPROACH

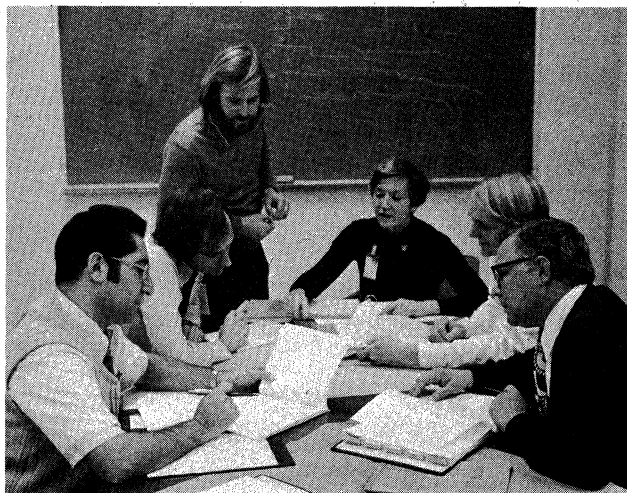
AMI's custom capability encompasses the entire development sequence of a product. The services which AMI provides to the customer start with five conceptual planning steps:

- System Definition
- System Design and Partitioning
- Preliminary Logic Design and Simulation
- Final Logic Design
- Chip Circuit Design

First, system definition requires the customer to have full knowledge of the system requirements for the circuit. Working with AMI's MOS/LSI application experts, the two companies form a team to develop a system which not only meets the needs, but also optimizes performance and economy.

Step two, system partitioning, follows the joint system definition. Partitioning involves the cataloging of functions into MOS subfunctions and then into chip functions. During this step of the program the best MOS process for the application is selected. Usually, functional flow charts and timing diagrams are generated as a preliminary step in the logic design.

Once partitioning is accomplished, preliminary logic design and simulation can be done. The chip functions, as catalogued in step two, are translated into MOS logic diagrams and traditional breadboarding techniques are quite often used to verify these logic designs. AMI also uses proprietary com-



puterized simulation programs for verification. These programs check the design, as well as help reduce time and cost of design verification.

Final logic design is next. First, errors discovered through breadboarding or simulation are corrected. Earlier partitioning may be refined, if the final logic design indicates a need. During the final logic design step, all system design objectives are analyzed again, MOS logic diagrams are finalized, chip sizes are estimated, and testing procedures are generated.

And then—chip circuit design. The topological chip layout is a precise science. The exact dimensions and placement of each transistor and other functions must be determined. The list of factors affecting chip design is almost endless: the use of space, the economy of functions, the versatility of functions, the power requirements, the manufacturing processes, the interconnections, the packaging, the performance of the circuit, the reliability of the design, and so on. All must be considered in the circuit layout design leading to final topological definition. Here again, AMI uses computerized circuit analysis programs to validate chip design and verify that the design meets performance objectives determined during system definition. The computerized analysis not only substantiates the logic, it is an integral part of the ongoing quality assurance program at AMI.

#### CUSTOMER TOOLING: THE COOPERATIVE APPROACH

In this approach to custom MOS/LSI the customer designs the circuit, thus having complete control over the logic and electrical requirements, the design budget and schedule, the design changes prior to tooling, and the manufacture of the tooling itself.

Design workshops, consultation and information documentation packages are provided by AMI according to the needs of the customer. Also, sensitivity to confidentiality is a prime aspect of the way AMI does business.

AMI divides its customer interfacing procedure into four phases: Phase One is a feasibility study; Phase Two is preliminary wafer fabrication (a sample run); Phase Three, pre-production yield evaluation; and Phase Four, production.

The Phase One feasibility study ideally starts before MOS logic is drawn. AMI customer tooling engineers can provide suggestions on the MOS design, discuss process and design rule parameters, provide a standard test device, help plan ahead for testing, and provide information on the packaging and tooling interface. With this background, the engineers can give assistance if questions or problems arise during the course of the design.

AMI's experience has shown that the customer tooling interface works best when the customer is fully aware from the start of how AMI will manufacture the device. If the customer has already designed the circuit, the Phase One Feasibility Study begins when AMI provides a process and design rule questionnaire. This also gives AMI information about customer package requirements, testing needs and tooling interface level. AMI customer tooling engineers will review the data to determine if AMI can meet all the customer requirements. At the end of this first phase AMI supplies the customer—without charge—a program plant, a firm quotation for the next two phases (preliminary wafer fabrication and yield evaluation), and a budgetary quotation for production.

During Phase Two, AMI will process one wafer lot and then map, optically inspect, package, and ship sample quantities of untested devices and, if the customer requires them, several untested wafers. Further, AMI guarantees that these sample devices will be within the agreed-upon process parameter values, and will meet AMI's standards of processing quality and workmanship. The customer can supply working plates for Phase Two, or AMI will accept pattern generator tape of 10x reticles.





After the customer approves the Phase Two sample devices, AMI moves to Phase Three—preproduction yield evaluation. Here AMI generates the required manufacturing documentation, writes, rewrites or runs acceptance on the test program, and builds the wafer probe cards and the program board for AMI's own testers. AMI then makes several reproducibility runs of wafers and sorts them for yield information. AMI charges a fixed price for the Phase Two and this portion of the Phase Three effort.

From the reproducibility runs AMI will assemble and final test an appropriate number of good devices. The unit cost will be based on the costs for assembly, type of package and final test. These units in effect provide the customer a low volume production run for additional evaluation and start-up production commitments.

Preproduction deliveries actually start during Phase Three. Initial production deliveries during Phase Four normally begin 9 to 11 weeks after approval of the preproduction units.

#### **CUSTOMER SUPPLIED TOOLING INTERFACE REQUIREMENTS**

When the customer provides the tooling, AMI prefers to work with customer-supplied working plates at both the Phase One (feasibility) and Phase Two (prototyping) interface levels. If the customer does not supply working plates, AMI will make them from other tooling; pattern generator tapes, CAD tapes, 10x reticles or other artwork. However, tooling other than working plates will move some cost from Phase Three to Phase Two.

In Phases Three and Four (yield evaluation and production), for quality control and logistics reasons AMI prefers to make its own working plates from original customer provided tooling. A pattern generator tape is the preferred interface level. However, AMI will also accept 10x reticles and compatible CAD tapes.

#### **CUSTOMER TOOLING PREFERRED DESIGN PACKAGE:**

- Pattern Generator Tape
- Sentry 600 Test Tape with Program Board
- Copy of Composite or 200x plot with critical dimensions noted
- Electrical Specification
- Bonding Diagram
- Logic Diagram
- Packaging Requirements
- Five Standard Devices fully tested to customer specification.

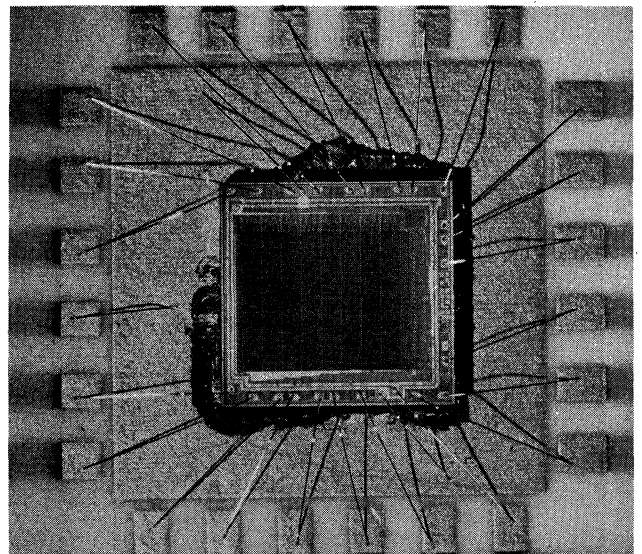
#### **CUSTOMER SUPPLIED TEST PROGRAMS**

Because the development of test programs is still one of the most significant problem areas in customer tooling, AMI requests that customers who design the custom circuit themselves meet the following test requirements:

- Design the device to be testable on the Sentry 600
- Keep the test short (2 sec. max.)
- Completely check out work pattern before supplying to AMI
- Make sure the device meets the specification supplied (electrical limits, test word)
- Supply a minimum of 5 standard parts fully tested to specification (all limits, all conditions)

#### **AMI MAKES THE FOLLOWING CUSTOMER TOOLING INTERFACE DOCUMENTS AVAILABLE TO THE CUSTOMER:**

- AMI processes, technical descriptions
- General customer tooling interface book
- Sentry 600 tape interface
- AMI testing requirements
- Electromask pattern generator tape interface
- 10x reticles and working plate interface
- Packages and packaging requirements
- Sample electrical specification
- Probe card specifications
- Design rules and process parameters, including AMI's standard test device (*all processes available under non-disclosure agreements only*).



### AMI'S DEDICATION TO CUSTOM

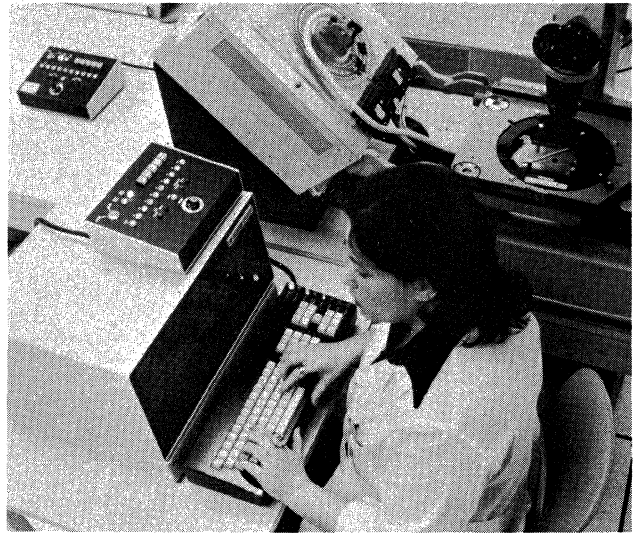
**Human Resources** — AMI's engineering staff is without peer in experience designing custom MOS/LSI circuits. The company is presently completing new custom designs at the rate of four per month.

AMI divides engineering into five major functional categories:

- **Development Engineering** — responsible for circuit development.
- **Customer Tooling Engineering** — verifies customer provided materials and makes conversions to AMI standard design techniques.
- **Product Engineering** — insures the manufacturability and cost effectiveness of AMI products.
- **Test Engineering and ROM Engineering** — an inhouse group that serves special needs of the other technical groups.
- **Engineering Support** — provides a wide variety of functions with a sophisticated array of automated systems discussed later in this brochure.

In areas other than engineering, highly personalized program support starts with the signing of the contract and continues throughout the life of the project. Dedicated program managers continuously monitor the progress, report periodically to the customer, and control the scheduling.

**Automated Facilities—Computer Aided Design (CAD)**—AMI has one of the most advanced CAD organizations in the microelectronics business, with a wealth of experience in supporting custom work. The tools for design automation are employed at many points in the custom design cycle, from the early logic stage to the making of production tooling:



1. Early in design a set of computer programs are used to assure that the logic is sound. The logic is modeled, exercised, and logic paths are determined for use later in test program generation. This step utilizes AMI's in-house Burroughs 6700 computer.

2. During the circuit design and topological layout phase several computer models are employed to identify potential problems, such as undesirable circuit interactions. The circuit is modeled exactly as it behaves and the results are used to assure that it will operate within allowable tolerances. The models used are probably the most sophisticated in the custom MOS industry.

3. Still another set of computer programs is used to check the physical layout of circuits on the chip. These programs make sure that all design rules are met for the particular MOS process being used.

4. AMI has developed an advanced method for symbolic layout of MOS integrated circuits (SLIC) that reduces design cycle time by about 30%. This method minimizes hand drafting, by substituting symbols for complex multilevel circuit architecture. The designer must still draw by hand, but with the use of SLIC gets a better feel for how the total circuit is developing.

It is important to point out that AMI does not use "computer designed" or standard cell circuits. AMI's circuits are laid out by experienced designers for minimum chip size and the computer is used only as an aid.

5. Just prior to the start of manufacturing, a laser interferometer pattern generator is employed to make the tooling plates. Using this extremely accurate machine, chip circuitry can be scaled up or down to produce greater yields per wafer, if necessary.

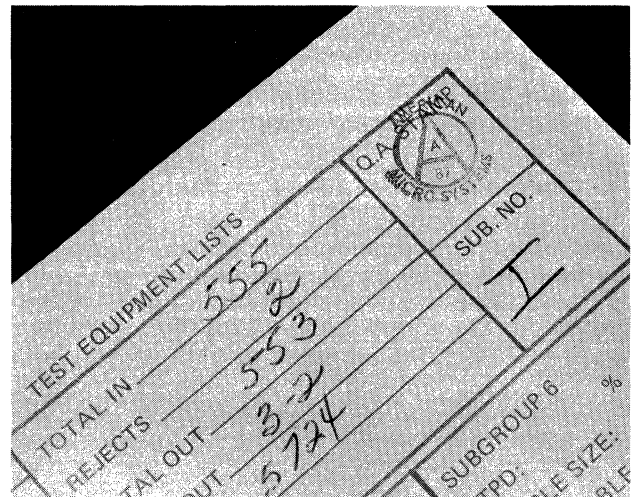
### DESIGN AID TOOLS

- On-site Burroughs 6700 computer with multiprocessing capability
- Computer terminals (remote job entry and dial-in), located throughout the Santa Clara and Pocatello engineering facilities. Terminals tie into the on-site 6700 and timesharing services.
- Two Computervision interactive graphics systems, that allow on-line generation and editing of composite drawings; includes six drafting surfaces and two CRT displays.
- High-speed, high resolution Electromask pattern generator.
- Calcomp plotter facility, which provides a reliable backup for the pattern generator.
- Computer aided design software for logic simulation, system simulation, circuit analysis, circuit layout, design rule checking, test pattern generation, and ROM masking.

### AMI'S EXTENSIVE QUALITY ASSURANCE PROGRAM

The AMI Quality Assurance Program is an ongoing activity that pervades the entire design and manufacturing process. The quality assurance function includes a special group of inspectors, organizationally separate from production. The main responsibility of these inspectors is to examine and test custom circuits and all the raw materials that go into them. The following is a partial list of the quality control checkpoints in the creation of a custom circuit. At each of these preproduction steps, meticulous checks of both design and workmanship are made.

- Final logic design (system objectives are reviewed)
- Chip circuit design (uses computerized circuit analysis to verify that performance meets objectives)
- Composite check, to assure that design modes are met and continuity is verified
- Working plates check
- Mask fabrication checks
- Wafer fabrication checks
- Wafer sort (functional requirements are checked)
- Scribe and break with 100% optical inspection
- Die attach checks
- Lead bonding check, followed by 100% preseat optical inspection
- Seal checks
- Final tests
- Final electrical and environmental product assurance tests



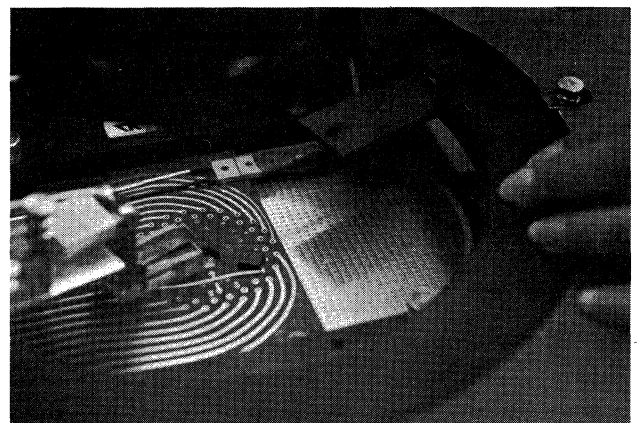
Only after the checks at each of these steps have been completed is a device considered fully manufacturable. It is then turned over to production with its yield history. The production facility continues its own quality control checks, starting from wafer fabrication on through final quality assurance tests.

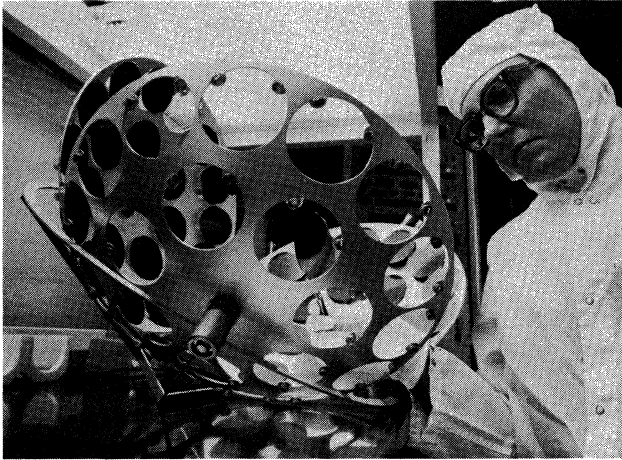
### TEST EQUIPMENT

AMI has made one of its two largest capital investments in automated testing systems. The company has the following test systems available:

- 12 Fairchild Sentry 600 Automated Test Systems. These machines are used for debugging prototypes, for solving design and testing problems and for production testing.
- A wide range of other testers, including a Teradyne J-384 and eight Programmable Automated Function Testers.

Information on all test equipment available at AMI is available on request.



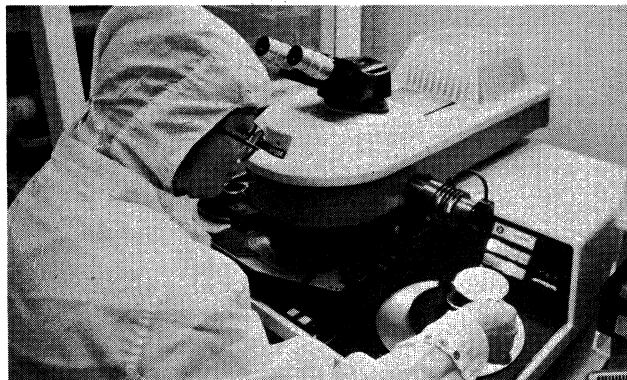


### MOS PROCESSES

As an MOS industry leader, AMI is continuously investigating and researching new processes, production developments and techniques to improve product capability, reliability, and cost effectiveness. Currently, six basic MOS processes and numerous variations are used at AMI. Only those processes which prove reliability reproducible in a production environment are used. (See also Section 11 for technical descriptions of the processes.)

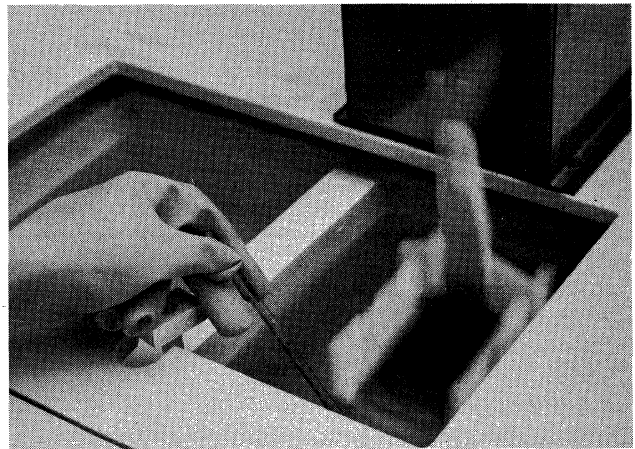
### P-CHANNEL, HIGH VOLTAGE, METAL GATE

This is the most mature process and because of its relative simplicity, has the lowest production cost per wafer. It provides high noise immunity, making it ideal for applications involving mechanical equipment which can generate rf noise and where low power dissipation is not a prime requirement. Because of the high voltage requirements associated with this process, the circuits produced are somewhat more difficult to interface with bipolar circuits than those produced with low voltage processes. The high voltage P-channel process is also less efficient in chip area utilization, especially when higher speeds are required.



### P-CHANNEL, ION IMPLANTED, METAL GATE

The ion implanted P-channel process is very similar to high voltage P-channel, except it has lower thresholds. (It is also known as the low voltage P-channel process.) It allows the use of depletion mode devices as load transistors, which greatly increase device speed per unit area, can lower power, improve noise margins, make bipolar interfacing easier, permit the use of unregulated power supplies (at the expense of greater chip area) and allow generation of full amplitude signals on the chip, with only one power supply. This latter feature can be especially useful in converting certain logic to much simpler forms and thus reducing chip area significantly. This process has been used in custom applications, where speed, noise immunity, and wide power supply tolerances are required.



### P-CHANNEL, SILICON GATE

This process has been used mostly in memories. Its two main features are (1) somewhat smaller transistor structures, and (2) availability of a partial third layer for interconnects, which can significantly reduce cell area and interconnections between cells. The device response is as fast as in P-channel low voltage process, but slower than in N-channel or CMOS processes.

### N-CHANNEL, SILICON GATE

N-channel devices are inherently faster than their P-channel counterparts. In addition, the N-channel process allows high density designs because: (1) for a given device N-channel can charge or discharge a node faster than P-channel, (2) it has the self-aligning gate feature and, (3) the extra layer of interconnect, inherent in silicon gate, can be used to reduce chip interconnect area. Wafer processing is simple and, therefore, this is the lowest cost high-performance process. Interfacing with bipolar devices is easy because the circuit output is positive with respect to ground (like in a NPN transistor). This process is typically used for high speed dynamic circuits.

### N-CHANNEL ION IMPLANTED SILICON GATE (WITH DEPLETION LOADS)

This is a high performance process with all the advantages of N-channel Ion Implanted SiGate process, plus the increased speed associated with the availability of depletion loads. It is best suited for single supply (5 to 9 V) circuits that have high performance requirements and also must have high packing densities. The slight drawback of this process is the increased complexity arising from the additional processing steps, however, as more production experience is gained, it is becoming the most commonly used for custom designs.

### CMOS, SILICON GATE

The CMOS process has many advantages. The biggest asset is that its circuits draw very little static power (the

majority of power is consumed when switching occurs). CMOS Silicon Gate is also very fast, although as the operating frequency increases, the power dissipation approaches that found in other processes. CMOS also has very high noise immunity – comparable to ion implanted circuits using depletion mode load transistors. Like ion implanted depletion mode circuits, CMOS operates on a single power supply voltage, whose range can be very wide. The area used per logic function is quite large, but is likely to decrease as more experience is gained in designing CMOS circuits. CMOS chips are currently finding their way into ultralow power applications, such as electronic watches, clocks, and very low power memories. Also, in automotive electronics, where low standby current and high noise immunity are important, and in telecommunications circuits, where low power and high performance are required.

Comparison of AMI's MOS Processes

Parameter	P-Channel HiV <sub>T</sub> Metal Gate	P-Channel I <sup>2</sup> Metal Gate	P-Channel SiGate	N-Channel SiGate	N-Chann. I <sup>2</sup> SiGate W/DEPL.	Complementary CMOS
Speed (per unit area)	6	4	5	3	1	2
Power Consumption (low speed)	6	2	4	5	3	1
Area (per logic function)	4	3	3	2	1	6
Noise Immunity	4	2	5	5	3	1
Logic Flexibility	3	1	3	3	1	2
On-Chip Clock Generation	4	2	5	4	2	1
Bipolar Compatibility	5	2	3	1	1	2
Power Supply Latitude	4	2	4	5	2	1
Process Simplicity	1	2	2	3	5	6
Process Maturity	1	2	2	4	5	4

Rankings are relative among the processes, with the lowest number being most desirable.



# 10

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## **AMI Product Assurance Program**





# Product Assurance Program

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## INTRODUCTION

Quality is one of the most used, least understood, and variously defined assets of the semiconductor industry. At AMI we have always known just how important effective quality assurance, quality control, and reliability monitoring are in the ability to deliver a repeatably reliable product. Particularly, through the manufacture of custom MOS/LSI, experience has proved that one of the most important tasks of quality assurance is the effective control and monitoring of manufacturing processes. Such control and monitoring has a twofold purpose: to assure a consistently good product, and to assure that the product can be manufactured at a later date with the same degree of reliability.

To effectively achieve these objectives, AMI has developed a Product Assurance Program consisting of three major functions:

- Quality Control
- Quality Assurance
- Reliability

Each function has a different area of concern, but all share the responsibility for a reliable product.

### The AMI Product Assurance Program

The program is based on MIL-STD-883, MIL-M-38510, and MIL-Q-9858A methods. Under this program, AMI manufactures highest quality MOS devices for all segments of the commercial and industrial market and, under special adaptations of the basic program, also manufactures high reliability devices to full military specifications for specific customers.

The three aspects of the AMI Product Assurance Program — Quality Control, Quality Assurance, and Reliability — have been developed as a result of many years of experience in MOS device design and manufacture.

**Quality Control** establishes that every method meets, or fails to meet, product parameters — *QA checks results*.

**Quality Assurance** establishes that every method meets, or fails to meet, processing or production standards — *QA checks methods*.

**Reliability** establishes that QA and QC are effective — *Reliability checks device performance*.

One indication that the AMI Product Assurance Program has been effective, is that NASA has endorsed AMI products for flight quality hardware since 1967. The Lunar Landers and Mars Landers all have incorporated AMI circuits, and AMI circuits have also been utilized in the Viking and Vinson programs, as well as many other military airborne and reconnaissance hardware programs.

## QUALITY CONTROL

The Quality Control function in AMI's Product Assurance Program involves constant monitoring of all aspects of materials and production, starting with the raw materials purchased, through all processing steps, to device shipment. There are three major areas of Quality Control:

- Incoming Materials Control
- Microlithography Control
- Process/Assembly Control

### Incoming Materials Control

All purchased materials, including raw silicon, are checked carefully to various test and sampling plans. The purpose of incoming materials inspection is to ensure that all items required for the production of AMI MOS circuits meet such standards as are required for the production of high quality, high reliability devices.

Incoming inspection is performed to specifications agreed to by suppliers of all materials. The Quality Control group continuously analyzes supplier performance, performs comparative analysis of different suppliers, and qualifies the suppliers.

Tests are performed on all direct material, including packages, wire, lids, eutectics, and lead frames. These tests are performed using a basic sampling plan in accordance with MIL-S-19500, generally to a Lot Tolerance Percent Defective (LTPD) level of 10%. The AQL must be below 1% overall.

Two incoming material inspection sequences illustrate the thoroughness of AMI Quality Control:

- Purchased packages are first inspected visually. Then, dimensional inspections are performed, followed by a full functional inspection, which subjects the packages to an entire production run simulation. Finally, a full electrical evaluation is made, including checks of the insulation, resistance, and lead-to-lead isolation. A package lot which passes these tests to an acceptable LTPD level is accepted.
- Raw silicon must also pass visual and dimensional checks. In addition, a preferential etch quality inspection is performed. For this inspection, the underlayers of bulk silicon are examined for potential anomalies such as dislocation, slippage, or etch pits. Resistivity of the silicon is also tested.

### Microlithography Control

Microlithography involves the processes which result in finished working plates, used for the fabrication of wafers. These processes are pattern or artwork generation, photo-reduction, and the actual printing of the working plates.

Pattern generation now is the most common practice at AMI. The circuit layout is digitized and stored on a tape, which then is read into an automated pattern generator, which prints a highly accurate 10x reticle directly.

In cases where the more traditional method of artwork generation is used whether Rubylith, Gerber Plots, AMI generated or customer generated — the artwork is thoroughly inspected. It is checked for level-to-level registration and dimensional tolerances. Also, a close visual inspection of the workmanship is made. AMI artwork is usually produced at 200x magnification and must conform to stringent design rules, which have been developed over a period of years, as part of the process control requirements.

Acceptable artwork is photographically reduced to a 20x magnification, and then further to a 10x magnification. The resulting 10x reticles are then used for producing 1x masters. The masters undergo severe registration comparisons to a registration master and all dimensions are checked to insure that reductions have been precise. During this step, image and geometry are scrutinized for missing or faded portions and other possible photographic omissions.

For a typical P-channel silicon gate device, master sets are checked at all six geometry levels in various combinations against each other and against a proven master set. Allowable deviations within the die are limited to 0.5 micron, deviations within a plate are limited to 1 micron, and all plate deviations are considered cumulatively.

Upon successful completion of a device master set, it is released to manufacturing where the 1x plates are printed. A sample inspection is performed by manufacturing on each 30-plate lot and the entire lot is returned to Quality Control for final acceptance. Quality Control performs audits on each manufacturing inspector daily, by sample inspection techniques.

The plates can be rejected first by manufacturing, when the 30-plate lots are inspected, or by Quality Control when the lots are submitted for final acceptance. If either group rejects the plates, they are rescreened and then undergo the same inspection sequence. In the rescreening process, the plates undergo registration checks; visual checks for pin holes, protrusions, and faded or missing images, as well as all critical dimension checks.

#### Process Control

Once device production has started in manufacturing, AMI Quality Control becomes involved in one of the most important aspects of the Product Assurance Program — the analysis and monitoring of virtually all production processes, equipment, and devices.

Process controls are performed in the fabrication area, by the Quality Control Fabrication Group, to assure adherence to

specifications. This involves checks on operators, equipment and environment. Operators are tested for familiarity with equipment and adherence to procedure. Equipment is closely checked both through calibration and maintenance audits. Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possibility of contamination or adverse effects due to temperature or humidity excesses.

Experience has proven that such close control of the operators, equipment, and environment is highly effective towards improved quality and increased yields.

In addition to the specification adherence activities of the QC Fabrication Group, a QC Laboratory performs constant process monitoring of virtually every step of all processes. Specimens are taken from all production steps and critically evaluated. Sampling frequency varies, depending on the process, but generally, oxidation, diffusion, masking, and evaporation are the most closely monitored steps.

Results are supplied both to manufacturing and engineering. When evidence of a problem occurs, QC provides recommendations for corrections and follows up the corrective action taken.

Optical inspections are performed at several steps; quality control limits are based on a 10% LTPD. The chart in Figure 1 shows process steps and process control points.

#### QUALITY ASSURANCE

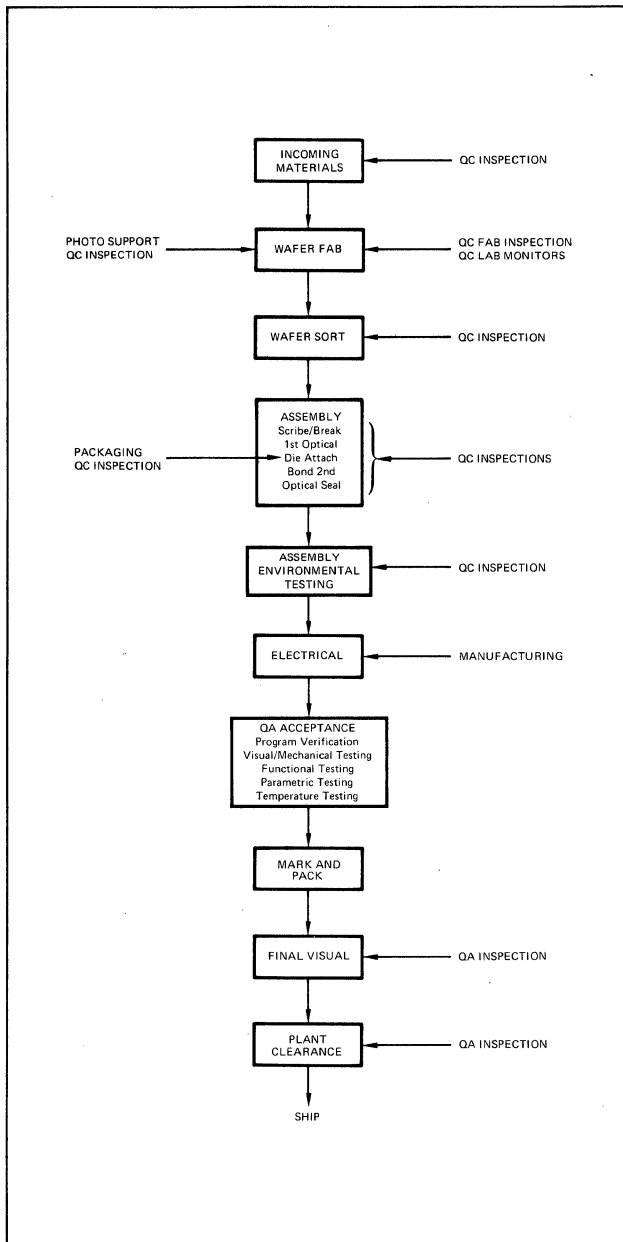
The Quality Assurance function in the Product Assurance Program involves checking the ability of manufactured parts to meet specifications. In addition, the QA group also is responsible for calibration of all equipment, and for the maintenance of AMI internal product specifications, to assure that they are always in conformance with customer specifications, or other AMI specifications.

After devices undergo 100% testing in manufacturing, they are sent to Quality Assurance for acceptance. Lots are defined, and using the product specifications, sample sizes are determined, along with the types of tests to be performed and the test equipment to be used. Lots must pass QA testing either with an LTPD or 10%, or less, if the specification requires tighter limits.

Three types of tests are performed on the samples: visual/mechanical, parametric, and functional. All tests are performed both at room temperature and at elevated temperature. In addition, a number of other special temperature tests may be performed, if required by the specification. Generally, high temperature tests are at 125°C.

To perform the tests, QA uses AMI *PAFT* test systems, ROM test systems, Macrodata testers, Fairchild *Sentry* systems,

**Figure 1. Flowchart of Product Assurance Program Implementation**



Western Digital *Spartan* systems, *Impact* testers, and various bench test units. In special instances a part may also be tested in a real life environment, in the equipment which is to finally utilize it.

If a lot is rejected during QA testing, it is returned to the production source for an electrical rescreening. It is then returned to QA for acceptance, but is identified as a resubmitted lot. If it fails again, it is discarded and corrective action

in engineering is initiated. As evidence of the problem is detected, the parts may also be traced all the way back to the wafer run, to analyze the cause.

When a lot is acceptable, it is sent to packaging and then to finished goods. When parts are sent from finished goods, they are again checked by the QA group to a 10% LTPD, with visual/mechanical tests. Also, all supporting documentation for the parts is verified, including QA acceptance, special customer specifications, certificates of compliance, etc. Only after this last check are devices considered ready for plant clearance.

If there are customer returns, they are first sample tested by QA, to determine the cause of the return. (Many times an invalid customer test will incorrectly cause returns.) After QA evaluates all returns, they are sent to Reliability for failure analysis.

## RELIABILITY

The Reliability function in the Product Assurance Program involves process qualification, device qualification, package qualification, reliability program qualification, and failure analysis. To perform these functions AMI Reliability group is organized into two major areas:

- Reliability Laboratory
- Failure Analysis

### Reliability Laboratory

AMI Reliability Laboratory is responsible for the following functions:

- New Process Qualification
- Process Change Qualification
- Process Monitoring
- New Device Qualification
- Device Change Qualification
- New Package Qualification
- Device Monitoring
- Package Change Qualification
- Package Monitoring
- High Reliability Programs

There are various closely interrelated and interactive phases involved in the development of a new process, device, package, or reliability program. A process change may affect device performance, a device change may affect process repeatability, and a package change may affect both device performance and process repeatability. To be effective, the Reliability Laboratory must monitor and analyze all aspects of new or changed processes, devices, and packages. It must be determined what the final effect is on product reliability, and then evaluate the merits of the innovation or change.

### Process Qualification

For example, AMI Research and Development group recommends a new process or process alteration when it feels that the change can result in product improvement. The Reliability Laboratory then performs appropriate environmental and electrical evaluations of new process. Typically, a special test vehicle, or "rel chip", generated by R&D during process development, is used to qualify the recommended new process or process change.

The rel chip is composed of circuit elements similar to those that may be required under worst-case circuit design conditions. The rel chip elements are standard for any given process, and thus allow precise comparisons between diffusion runs. The following is an example of what is included on a typical rel chip:

- A discrete inverter and an MOS capacitor
- A large P-N junction covered by an MOS capacitor
- A large P-N junction area (identical to the junction area above, but without the MOS capacitor)
- A large area MOS capacitor over substrate
- Several long contact strings with different contact geometries.
- Several long conductor geometries, which cross a series of eight deeply etched areas.

Each circuit element of a rel chip allows a specific test to be performed. As an example, the discrete inverter and MOS load device accommodate power life tests. As a consequence, any type of parameter drift can be observed. The MOS capacitor, covering the large P-N junction, can serve to indicate the presence of contamination in the oxide, under the oxide, or in the bulk silicon. If unusual drift is evidenced, the location of contamination can be determined through analysis of the additional MOS capacitor and the large P-N junction area. The metal conductor interconnecting contacts is useful for life testing under relatively high current conditions. It facilitates the detection of metal separation when moisture or other contaminants are present.

The conductors crossing deeply etched areas allow the checking of process control. Rather than depending upon optical inspection of metal quality, burned out areas caused by high currents are readily identified and provide a quantitative measure of metal quality.

If the Reliability Laboratory determines that a recommended new process or process change is viable for manufacturing purposes, further analysis is necessary to determine that production devices can be manufactured in high volume, in a repeatable and reliable manner.

### Process Monitoring

In addition to process qualification, the Reliability group also conducts ongoing process monitoring programs. Once every 90 days each major production process is evaluated using rel chips as test vehicles. The resulting test data is analyzed for parameter limits and process stability. In this manner AMI can help assure repeatability and high product quality.

### Package Qualification

New packages are also qualified before they are adopted. To analyze packages, a qualification matrix is designed, according to which the new package and an established package (used for control) are tested concurrently. The test matrix consists of a full spectrum of electrical and environmental stress tests, in accordance with MIL-STD-883.

### Failure Analysis

Another important function of the Reliability group is failure analysis. Scanning electron microscopes, high power optical microscopes, diagnostic probe stations, and other equipment is used in failure analysis of devices submitted from various sources. It is the function of the Reliability group to determine the cause of failure and recommend corrective action.

The Reliability group provides a failure analysis service for the previously mentioned in-house programs and for the evaluation of customer returns. All AMI customers are provided a failure analysis service for any part that fails within one year from date of purchase and the results of the analysis are returned in the form of a written report.

### SUMMARY

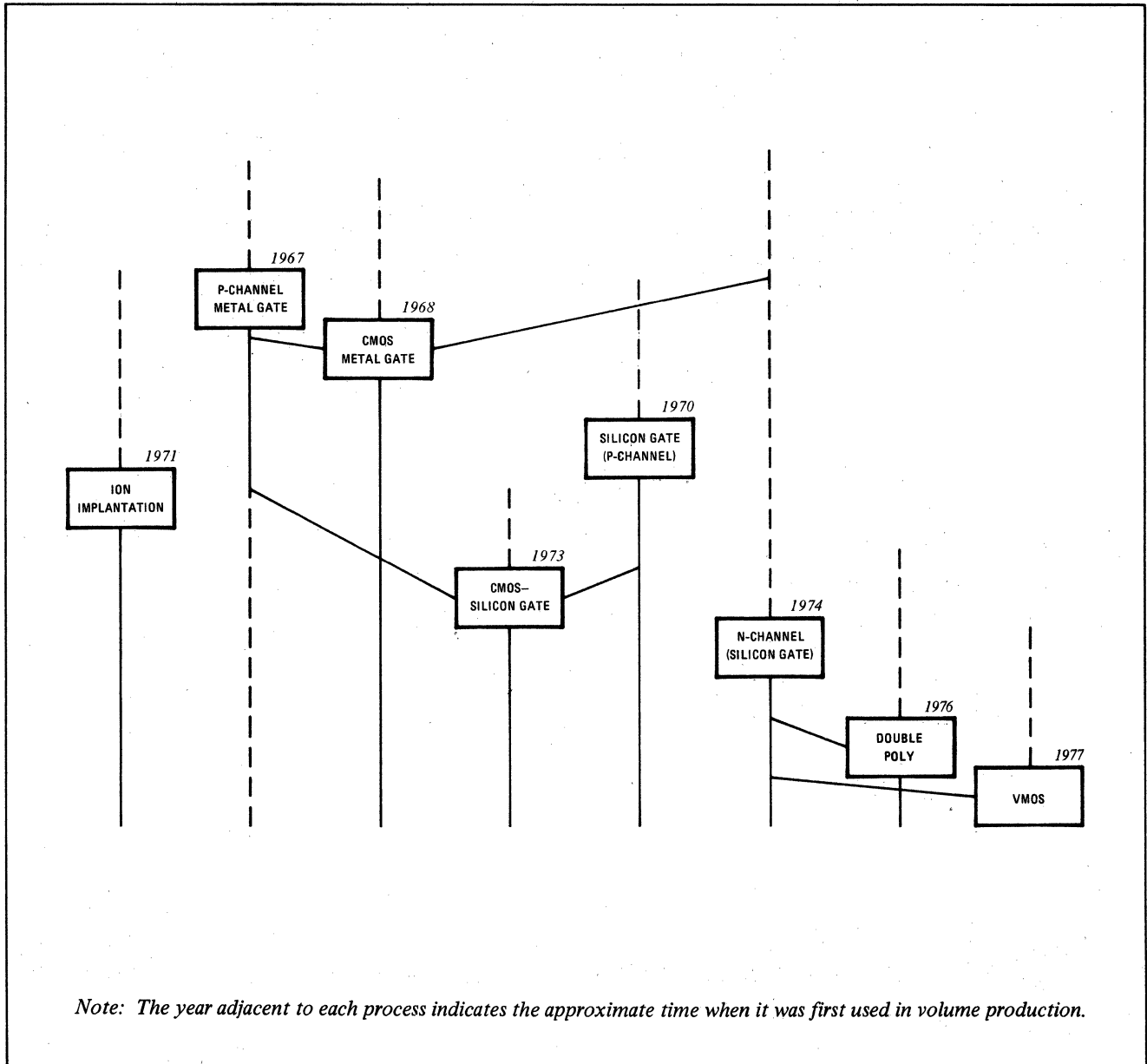
The Product Assurance Program at AMI is oriented towards process control and monitoring, and the evaluation of devices. The Program consists of three major functions: Quality Control, Quality Assurance, and Reliability. Constant monitoring of all phases of production, with information feedback at all levels, allows fast and efficient detection of problems, evaluation and analysis, correction, and verification of the correction. The overall result is a line of products which are highly repeatable and reliable, with a very low reject level.

# 11

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## **MOS Processes**

**FIGURE 11-1. EVOLUTION OF MAJOR MOS PROCESSES, CHRONOLOGICAL CHART**



# MOS Processes

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## INTRODUCTION

From the first attempts, some dozen years ago, to manufacture MOS devices commercially, the MOS integrated circuit industry has grown to be one of the largest in all of electronics. MOS/LSI circuits are found in virtually every kind of electronic test and measurement instrument, and are the mainstay of such end products as calculators, digital watches and clocks, computer memories, automotive control systems, home appliances, entertainment systems, and many others.

Every major integrated circuits manufacturer today has some type of MOS product line and MOS is growing faster than any other segment of the entire electronics industry—both, by the increasing demand for existing products and through innovative expansion into new applications.

Manufacturing technologies in the MOS industry have evolved from a single early MOS process to several basic processes and many variations thereof, variously developed and used by different manufacturers. It is the purpose of this section to survey the basic MOS processes and provide a comparative overview.

## EVOLUTION OF MOS

The earliest commercial MOS processes were developed by trial and error to the point where a manufacturer could produce a device that worked satisfactorily and would give a reasonable yield. It made sense for the manufacturer to stay with his process faithfully, for fear of disturbing a working combination of process steps and thus interrupting the entire production. This was the only practical and profitable manner of producing devices during the early years of MOS.

Out of this empirical heritage grew a more thorough understanding of the technology—both from the accumulation of production experience, as well as from research into the processing steps and the basic properties of materials. As a result, the MOS industry increased its facility to predictably vary processing techniques, introduce entirely new process steps, and use new materials. An early example of the alteration of processing techniques was the variation of *oxide thickness*; *ion implantation* became an entirely new process step; and the *polysilicon gate electrode* or *silicon nitride passivation* exemplifies the use of a new material. Some of the newest processes, such as VMOS, illustrate even more fundamental deviation—a completely new structural form of the classic MOS transistor device.

The earliest MOS process (see Figure 11-1) was the *P-channel Metal Gate*. Although there were prior unsuccessful attempts by various manufacturers to develop a process and become established in the MOS business, not until 1967, when American Microsystems began to manufacture and market its products, was it proven that MOS integrated circuits are an economically and technologically viable product. Thus, the P-channel Metal Gate process became the progenitor for an entire MOS industry, and was the foundation for development of all the other processes.

As new MOS processes were developed, each was refined for particular performance characteristics or some manufacturing advantage. Now, it is common that a particular process has a preferred application—a specific product or type of circuit. Today, there is no major MOS manufacturer who still uses only one process.

## THE MOS TRANSISTOR

MOS integrated circuits are based on the MOS (metal-oxide-silicon) transistor, also called a MOSFET. These transistors are the result of early research done by Sah, Ihantola and Moll, Hofstein and Heiman, Heil, as well as many others. Some of their work dates as far back as 1930. The following four pages contain a brief summary of the physicochemical and electronic theory of MOS transistors, followed by a discussion of some specific MOS transistor design considerations.

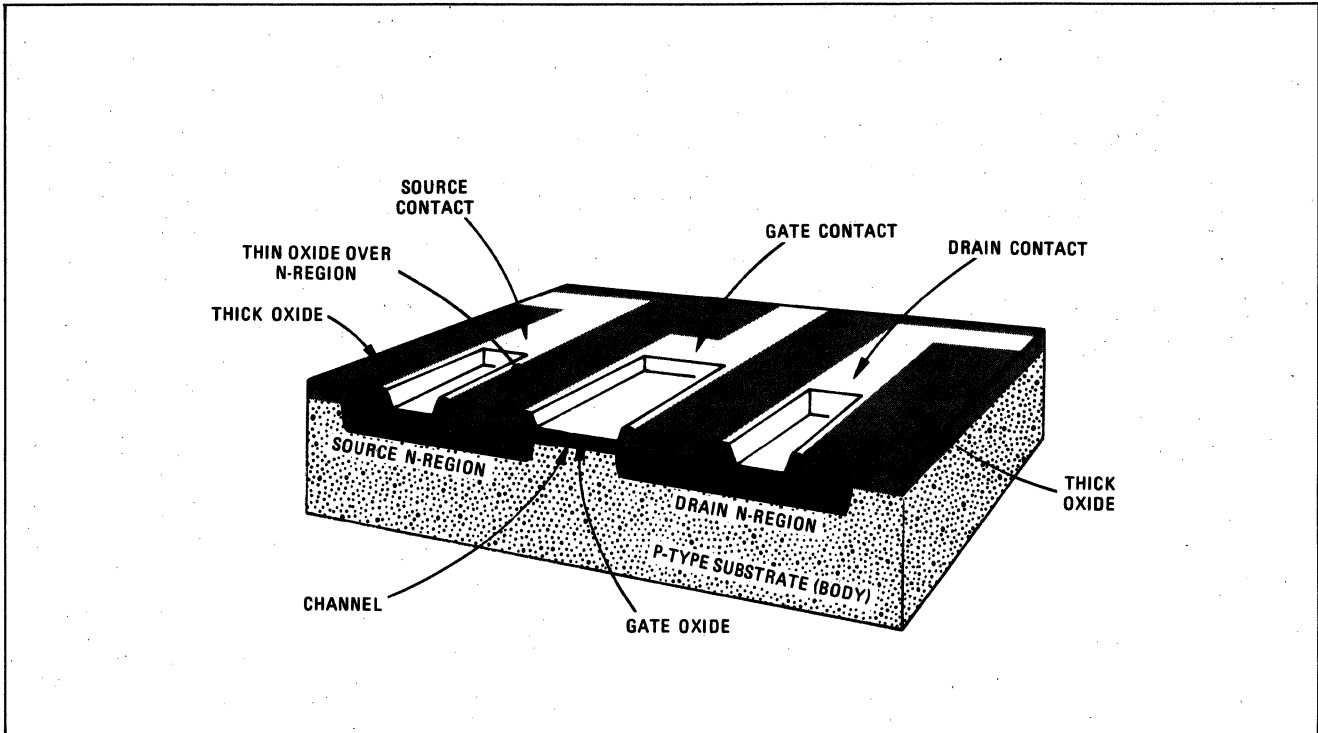
## P-CHANNEL AND N-CHANNEL TRANSISTORS

If an electrode is located near the surface of bulk semiconductor material, a voltage applied to the electrodes causes the conducting properties of the semiconductor surface to be altered. This is referred to as the *surface field effect* and is the fundamental phenomenon on which operation of the MOS transistor is based.

The bulk semiconductor material, or substrate, can be either P-type or N-type silicon. If P-type silicon is used, as shown in Figure 11-2, two N regions are diffused into the substrate. The electrode is positioned in the area between the two N regions and insulated from the substrate by a thin layer of a dielectric, such as silicon dioxide. Now, as long as the voltage on the electrode is slightly negative with respect to the substrate, it will cause the P-type silicon near the surface to become *accumulated* with positive charges, attracted by the negative electrical field of the electrode. As the electrode voltage is changed to be slightly positive with respect to the substrate, the surface will begin to be *depleted* of mobile positive charges and will cause a predominantly negative charge to appear. And if the voltage is increased still further, the surface becomes *inverted* and contains what may be thought of as a continuous layer of mobile negative charges—in the form of electrons. Thus, the surface essentially becomes N-type silicon. It is this latter state of *inversion* that is of prime interest, because it creates a conducting N channel between the two N regions, and thus allows current to flow.

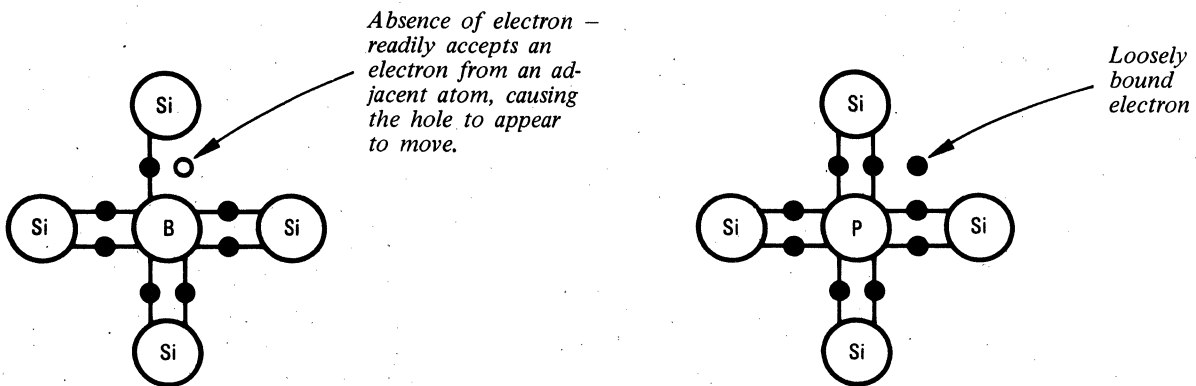
In an MOS transistor the two N regions are known as the *source* and *drain*, whereas the electrode is referred to as the *gate*. (The lamination in the gate area gives rise to the name *metal-oxide-silicon*, or *MOS*.) The electrode voltage required to create the conducting channel is referred to as the *threshold voltage*  $V_T$  and is an important parameter in circuit design, because it represents that gate voltage required to turn the transistor on. Threshold voltage is discussed in more detail later.

FIGURE 11-2. CROSSSECTION OF AN N-CHANNEL TRANSISTOR



**P-type and N-type Silicon**

*P-type silicon is made by doping pure silicon, during its crystal growth stages, with impurity (dopant) atoms, commonly boron. The boron impurity causes the silicon to become a semiconductor, which conducts by virtue of mobile positive charges dispersed throughout its structure. The positive charges are the absence of an electron in the outermost shell of the silicon atoms, usually referred to as "holes". In a similar manner, N-type silicon is made by doping pure silicon with impurity atoms such as phosphorus, antimony, or arsenic, which leaves an "extra" loosely bound electron in the outermost shell of the silicon atoms. Thus, in N-type silicon conduction takes place by means of mobile negative charges.*



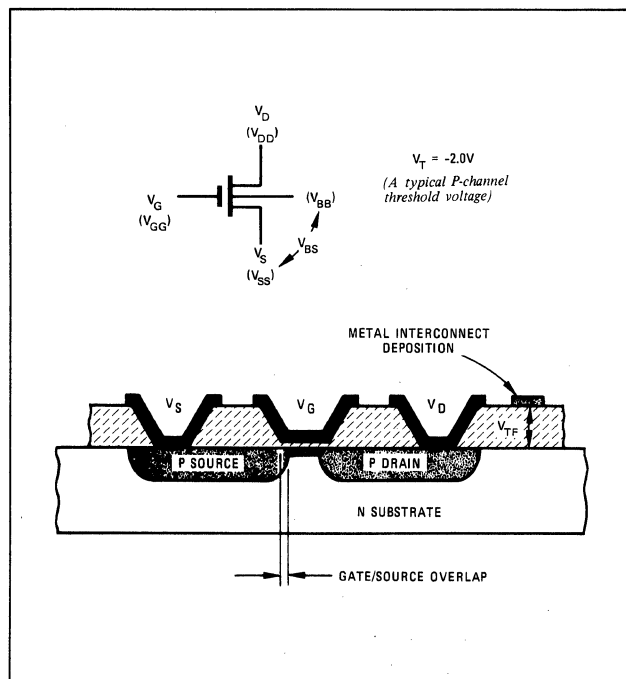


The above structure is that of an *N-channel MOS transistor operating in the enhancement mode*. That is, as the gate voltage is raised, it enhances the flow of current in the N channel between the source and drain. It is equally possible, however, to make a *P-channel enhancement mode transistor*, by diffusing two P regions in an N-type substrate and then increasing the gate voltage in a negative direction, to accumulate positive charge at the surface and thus create a P channel between the source and drain. Figure 11-3 shows a P-channel transistor.

In contrast to the enhancement mode transistor, there can also be a *depletion mode transistor*—which simply refers to the fact that the transistor is in a conducting state without any bias voltage on the gate; a bias must be applied to decrease the current flow.

There are two ways in which a depletion mode transistor can be made. First, it is actually more characteristic for an N-channel transistor device to operate in depletion mode, rather than in enhancement. A part of the reason is because the silicon dioxide insulating layer between the gate electrode and the substrate always has an internal positive charge, which acts toward the formation of an N channel, in much the same way as an applied positive gate bias does. Therefore, an N-channel transistor may intrinsically be a depletion mode device and special processing techniques are required to cause it to operate in enhancement mode.

**FIGURE 11-3. CROSSSECTION AND SCHEMATIC SYMBOL OF A P-CHANNEL TRANSISTOR**



Another way to make depletion mode transistor is by ion implantation. In the case of a P-channel transistor, the N-type substrate is bombarded with P-type (acceptor) impurity ions, to actually convert the surface of the substrate to P-type. Thus, a P channel is formed and will conduct current between the source and drain without any gate bias. Ion implantation is a special technique, described and illustrated in more detail later.

### VOLTAGE-CURRENT CHARACTERISTICS

The voltage-current relationships in an MOS transistor can be considered by using the P-channel transistor shown in Figure 11-3. If the gate voltage  $V_G$  becomes more negative than the threshold voltage  $V_T$  (-2.0 volts with respect to the substrate surface under the gate electrode, assuming  $V_S = 0V$ ), a channel is formed and hole current can flow between the source and the drain. There is a voltage drop along the channel (the channel acts as a resistive element) and because of this gradient,  $V_T$  is defined with respect to one point in the channel. This point is where the channel joins the source region, where the channel and source voltage is the same. Thus,  $V_T$  is actually defined with respect to the source and the common expression for it is:

$$V_T = V_G - V_S \quad (\text{when the channel starts to form})$$

The magnitude of the channel current depends on the drain voltage  $V_D$ . With the source at 0V, current will flow any time  $V_D$  is negative.

As  $V_D$  is increased in the negative direction, current increases in a linear manner, until the transistor is saturated, at which time further increase in  $V_D$  does not materially increase the current. The point of saturation depends on the voltage applied to the gate, as shown by the series of drain current curves in Figure 11-4. The gate voltage can be used to raise the upper limit (saturation level) of current flow, and the maximum current is limited either by the dielectric breakdown between the gate electrode and the substrate, or by other factors described below. The gate voltage  $V_G$  is related to the drain voltage at saturation,  $V_{D \text{ Sat}}$ , by the following equation:

$$V_{D \text{ Sat}} = V_G - V_T$$

The saturation point often is also referred to as *pinch-off*, due to the fact that an inversion layer no longer exists adjacent to the drain (channel current, however, continues to flow).

When an MOS transistor is in a circuit, the drain may be connected to a drain supply voltage, designated  $V_{DD}$ , or the drain connection may serve as the output of the circuit. Both conditions are shown in the inverter circuit, Figure 11-5. The gate commonly serves as the input connection, or it may also be connected to a supply voltage, designated  $V_{GG}$ . The source

serves as the reference against which  $V_T$  and all other voltages are measured. It is common to have the source tied to ground, but it may also be at a voltage other than ground. If the source is tied to a supply voltage, that voltage is designated  $V_{SS}$ .

The substrate, or body, is also commonly tied to ground, although back biasing the substrate is a specific technique for changing the effective  $V_T$  value. The influence of substrate back bias on  $V_T$  is referred to as the *body effect* and is, for example, used with N-channel devices to raise the  $V_T$  to an operationally more desirable value than the intrinsic  $V_T$ .

Considering the effects of both the source and substrate bias on the gate threshold voltage, and using the P-channel transistor in Figure 11-3 as an example, their relationships are as follows. The  $V_T$  is always -2V with respect to the source. That means that if  $V_{SS}$  is, for example, changed from 0 to +5V,  $V_G$  required to turn the transistor on will change from -2V to +3V – provided that the substrate voltage is also changed to +5V, so that there is no substrate-to-source bias. If the source now is returned to 0V, while the substrate remains at +5V,

FIGURE 11-4. DRAIN CHARACTERISTIC CURVES OF AN MOS TRANSISTOR

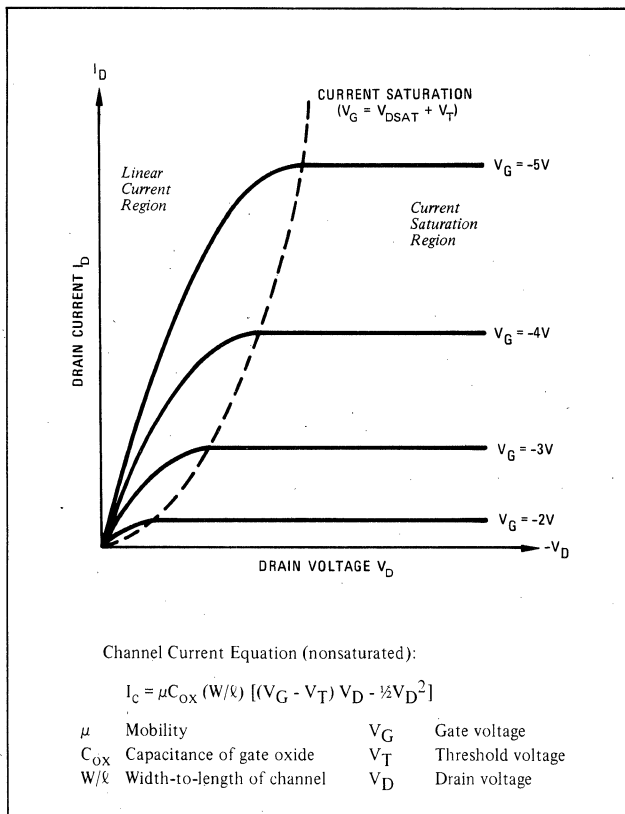
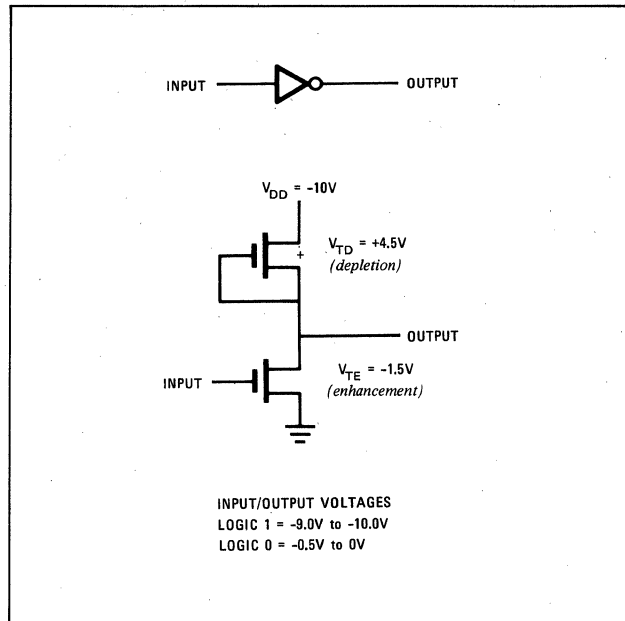


FIGURE 11-5. TYPICAL INVERTER USING BOTH DEPLETION AND ENHANCEMENT MODE TRANSISTORS



there is 5 volts back bias and this causes the body effect to shift  $V_T$  by an amount approximated by the formula:

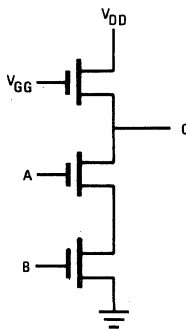
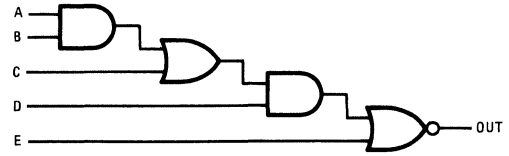
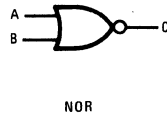
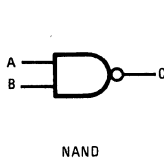
$$\Delta V_T = -\gamma \sqrt{V_{BS}}$$

Where  $V_{BS}$  is the substrate-to-source back bias the  $\gamma$  is the *body effect* term (a constant that typically varies from 0.5 to 0.75, depending on the process and the doping concentrations). Thus, the effective  $V_T$  in this example is  $-2 - (0.5 \sqrt{5}) \approx -3.1$  volts (using  $\gamma = 0.5$ ).

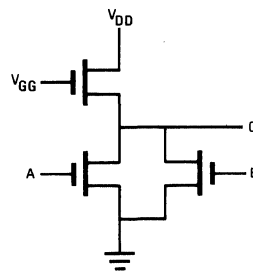
Note that there can never be any forward substrate-to-source bias (of 0.6 volts or more), because it would cause current flow between the substrate and the source, the same as in a forward biased diode. By the same token, if back bias is increased beyond the diode breakdown voltage, conduction will occur also. This is characteristically what happens when the drain voltage  $V_D$  is increased much beyond its value at channel current saturation. In such case the drain-to-substrate junction breaks down and avalanching of drain current takes place.

In summary, the operating range of an MOS transistor, is defined by the drain, source, substrate, or gate voltages. The drain, source, and substrate voltages can be between a forward bias condition of less than 0.6V and a back bias up to the diode breakdown voltage of the drain-substrate junction. Any time the voltages are outside this range there is conduction between either the source or drain and the substrate, and the transistor is not performing its proper function. The gate voltage is limited by gate-to-substrate breakdown.

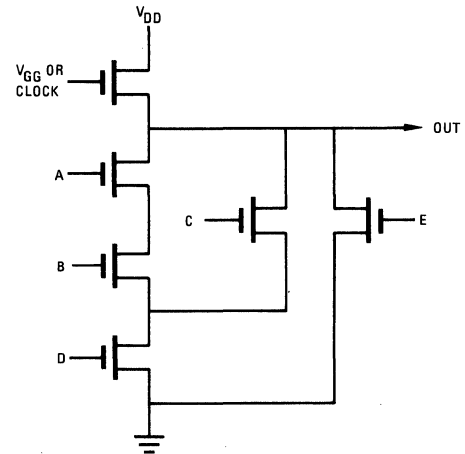
## Implementing Logic With MOS Transistors



NAND Gate



NOR Gate



Multiple Logic Element

In addition, depending on the proximity of the drain and source regions (i.e., the length of the channel), another type of breakdown, known as *punch-through* can also occur and become the limiting factor. In punch-through the substrate in the area between the drain and source becomes depleted and current flow through it increases, until it is limited by the external circuit.

### OTHER MOS CIRCUIT ELEMENTS

In designing circuits with MOS devices, resistive and capacitive elements can be implemented in several different ways. A resistor can either be a diffused or ion implanted strip in bulk silicon, or, more commonly, a high impedance MOS transistor is used solely as the resistive load. With a properly selected gate bias voltage the MOS transistor generally turns out to be a more compact load. Likewise, a capacitor can either be constructed by an electrode over bulk silicon region (Figure 11-12), or, more often, the parasitic capacitances of transistors are utilized (as described on page 11-9 and illustrated in Figure 11-8).

### MOS DESIGN CONSIDERATIONS

In the design and manufacture of an MOS integrated circuit, there always are several main objectives of performance, cost, manufacturing feasibility, etc. Such objectives must be given priorities and optimized.

This is equally true for an MOS manufacturer who is planning a standard product, as for an end user considering the design of a custom circuit. Some of the essential parameters that must be considered are as follows:

- Speed—the slowest internal propagation delay allowable in the circuit and the output signal rise and fall times.
- Power—the amount of power that may be consumed during operation. It is related to junction temperature, and usually affects chip size.
- Type of Logic—will the circuit be static or dynamic, does it consist of all random logic or of repetitive segments of logic, like in a shift register? These considerations determine basic approaches to design and topological layout of the chip.

- Application—factors that depend on the basic nature and environment of the equipment in which the circuit is to be used. Includes design considerations related to temperature, humidity, electrical noise, range of power consumption, and others.
- Power Supplies—the number of different voltages available to the circuit; their polarities and ranges.
- Clock Signals—the amplitude and frequency of needed clock signals, as well as requirements to gate or otherwise process the signals. (The amplitudes and duration of clock voltage levels are critical to the design of conduction ratios and coupler transistors.)
- Interface Requirements—the requirements to respond to certain voltage or current conditions at input or output.
- Packaging—the type of packages in which it is possible to mount the finished chip (depending on factors such as heat dissipation, size, etc.). Packages can be plastic, ceramic, Cer-DIP, or other types.
- Final Cost—the cost of the finished packaged and fully-tested device. (Cost depends on the process, manufacturing yields, testing and packaging costs, etc.)

The MOS design engineer can begin to achieve some of these objectives during system design, partitioning, and circuit design stages, but in integrated circuits the fundamental decisions occur at the atomic structure level of materials and the microscopic dimensional level of individual circuit elements. Here the design engineer can fix performance characteristics of individual devices (transistors, resistors, etc.) and thereby structure the performance of the whole circuit. The specific device performance characteristics that the designer is concerned with are exemplified by those described on this and the following page, but to implement them he makes certain process and device dimension oriented decisions, listed below:

- Materials—the kind of substrate to be used, its doping concentrations, choice of silicon or aluminum for the gate electrode, etc.
- Process Techniques—the type of diffusion to be used; its duration; use of ion implantation for altering the threshold voltages; or the use of any other special steps or procedures. (*A particular combination of Materials and Process Techniques defines the MOS process.*)
- Device Configuration—the size and dimensional proportions of the channel, drain, and source regions of each transistor; spacing between circuit elements and between interconnections; thickness of oxide and metal deposits (*most of these dimensions are incorporated into the final masks used in manufacturing.*)

Therefore, to fully appreciate the difference between MOS processes, one must understand both the basic device choice of a particular material, process steps, and device dimensions.

### THRESHOLD VOLTAGE $V_T$

One of the most basic determinants of device performance characteristics is the threshold voltage  $V_T$ . The concept of  $V_T$  and its role as a current determinant in an MOS transistor was described above, but it is important to consider the many different ways in which the  $V_T$  level can be altered in a transistor.

The level of  $V_T$  in an MOS transistor is very important because, in addition to affecting the amount of current, it affects the interface signal voltages, the level and polarity of power supply voltages needed in the circuit (thereby the power consumption), and indirectly also the speed of the transistor. Generally, in enhancement mode devices  $V_T$  must be sufficiently above or below 0V to provide a definite *on* and *off* biasing range, but not so much that it makes interfacing input signals difficult or causes high power consumption. A lower threshold is particularly important when a clock signal is used to turn the transistor *on* and *off*.

One fundamental determinant of  $V_T$  is the doping level of the substrate: the higher the dopant concentration in the substrate the higher the threshold voltage. Doping level of the substrate is determined at the time when the crystal is grown, but can be altered by ion implantation. Ion implantation consists of bombarding the surface of the substrate with dopant ions to change the substrate characteristics in the surface layer, where it interacts with the electric field of the gate electrode.

Another determinant of  $V_T$  is the gate insulator—both its thickness and the material itself (commonly silicon dioxide). A decrease in thickness lowers  $V_T$ , but at the same time increases the risk of capacitive shorting between the gate electrode and the substrate or diffused regions. Different dielectric materials have been tried by various manufacturers to overcome the shorting.

An intrinsic determinant of  $V_T$  is the choice of gate electrode and substrate materials. This relates to the physics concept of *work function*, which represents the binding energy of an electron in a particular material. When polycrystalline doped silicon is used as a gate electrode instead of aluminum, the work function changes in such a way as to cause a lower  $V_T$ . This is a basic difference between *aluminum gate* and *silicon gate* processes.

In relation to substrate material, there are two basic crystalline structures that can be used in MOS transistors. One is known as  $\langle 111 \rangle$  silicon and causes a relatively higher  $V_T$ , the other is  $\langle 100 \rangle$  silicon and causes a lower  $V_T$ . There are, however,

some tradeoffs between the two, relating to a parasitic field oxide threshold voltage  $V_{TF}$ , discussed later under the P-channel Metal Gate process.

### W/l RATIO

One of the very important dimension-related design parameters is the width-to-length ratio of the transistor channel. The  $W/l$  ratio determines the total resistance of the channel, is one determinant of speed, and relates to the overall size of the transistor. Thus, it affects the final chip size, which, in turn, relates to the yield and thereby to final costs.

It is a typical procedure for a designer to start out with the basic speed requirements of a circuit, then calculate the inherent capacitance of all transistors that are used as loads in the circuit, and finally choose the  $W/l$  of all driving transistors to provide the drive current, corresponding to the speed requirements. Figure 11-6 shows how the speed of a typical pair of inverters relates to the  $W/l$  ratio of their transistors.

Another use of the  $W/l$  ratio is in calculating the voltage drop across a transistor. In an inverter, as in Figure 11-5, where two transistors are connected in series, the relative voltage drop across each transistor is determined by choosing the two  $W/l$  ratios, so that their resistances are in the corresponding proportion.

### CAPACITANCE

Another major concern in MOS transistor design is capacitance. Capacitance usually is considered in several parts.

First, the gate electrode and the surface of the silicon substrate form a parallel plate capacitor, with the silicon oxide serving as the dielectric. Second, both are source and drain junctions with the substrate constitute a capacitor, with the depletion region acting as the dielectric. Third, there is capacitance between the gate electrode and both the source and the drain.

This latter capacitance is particularly important in all transistors in which the gate electrode overlaps the source and drain regions and it does so in all except those manufactured by the *self-aligning gate* processes, see Figure 11-3. This overlap is necessary in manufacture, to allow for mask tolerances: the gate electrode metal deposit must always reach all the way from the source to the drain and the only way to assure this is to allow a positive (overlap) mask tolerance.

Capacitance, of course, affects the speed of a transistor and also its power consumption. The more capacitance loading a transistor presents to an input signal, the more time is required to turn the transistor on. Power consumption considerations become particularly important at high operating frequencies.

In addition to having undesirable effects on circuit performance, the intrinsic capacitances can also be used beneficially in MOS circuit design. In dynamic MOS circuits capacitance is very often used for temporary storage of charge representing a logic level. In a typical MOS shift register stage, Figure 11-7, the equivalent capacitances  $C1$  and  $C2$  are used to store data between clock pulses. Capacitance  $C1$ , for example, represents the sum of the drain-to-substrate capacitance of  $Q3$ , gate capacitance of  $Q4$ , and also the capacitance of the interconnect line between  $Q3$  and  $Q4$ .

FIGURE 11-6. TYPICAL INVERTER PAIR DELAY VS.  $W/l$  FOR VARIOUS MOS PROCESSES

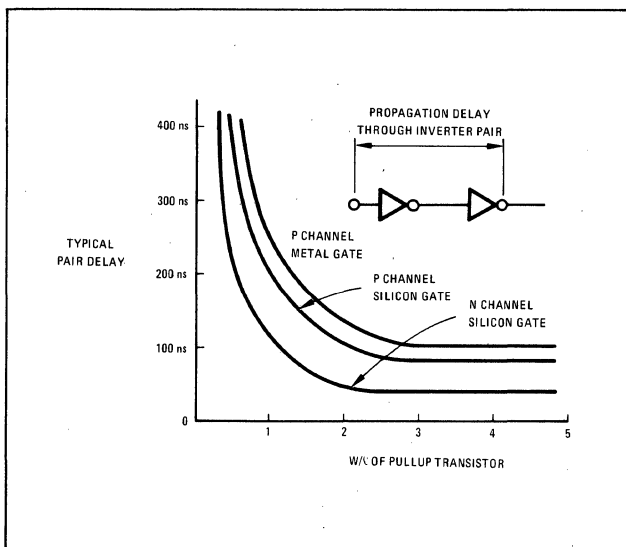
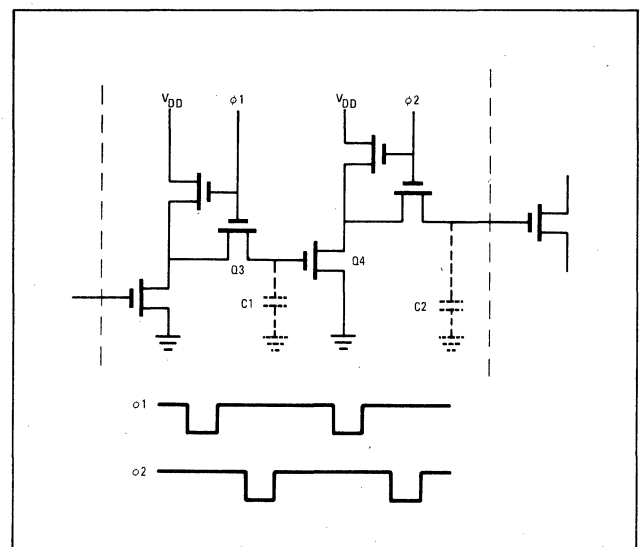


FIGURE 11-7. TYPICAL P-CHANNEL SHIFT REGISTER STAGE



In a similar manner, dynamic RAMs used parasitic capacitances of transistors for storage of the logic 1 or 0 bit, until the emergence of the single transistor cell introduced the use of a dedicated capacitor. (See Figure 11-12.)

**MOBILITY**

The term *mobility* (designated  $\mu$ ) refers to the intrinsic current carrying properties of N and P doped silicon. In N-doped silicon the majority current carriers are free electrons (see inset on page 11-4), whereas in P-doped silicon current is carried by means of holes. The mobility of electrons is approximately 2.5 times that of holes and therefore N-channel transistors are faster than P-channel. For the same channel size (or  $W/l$  ratio) N-channel transistor can also carry more current.

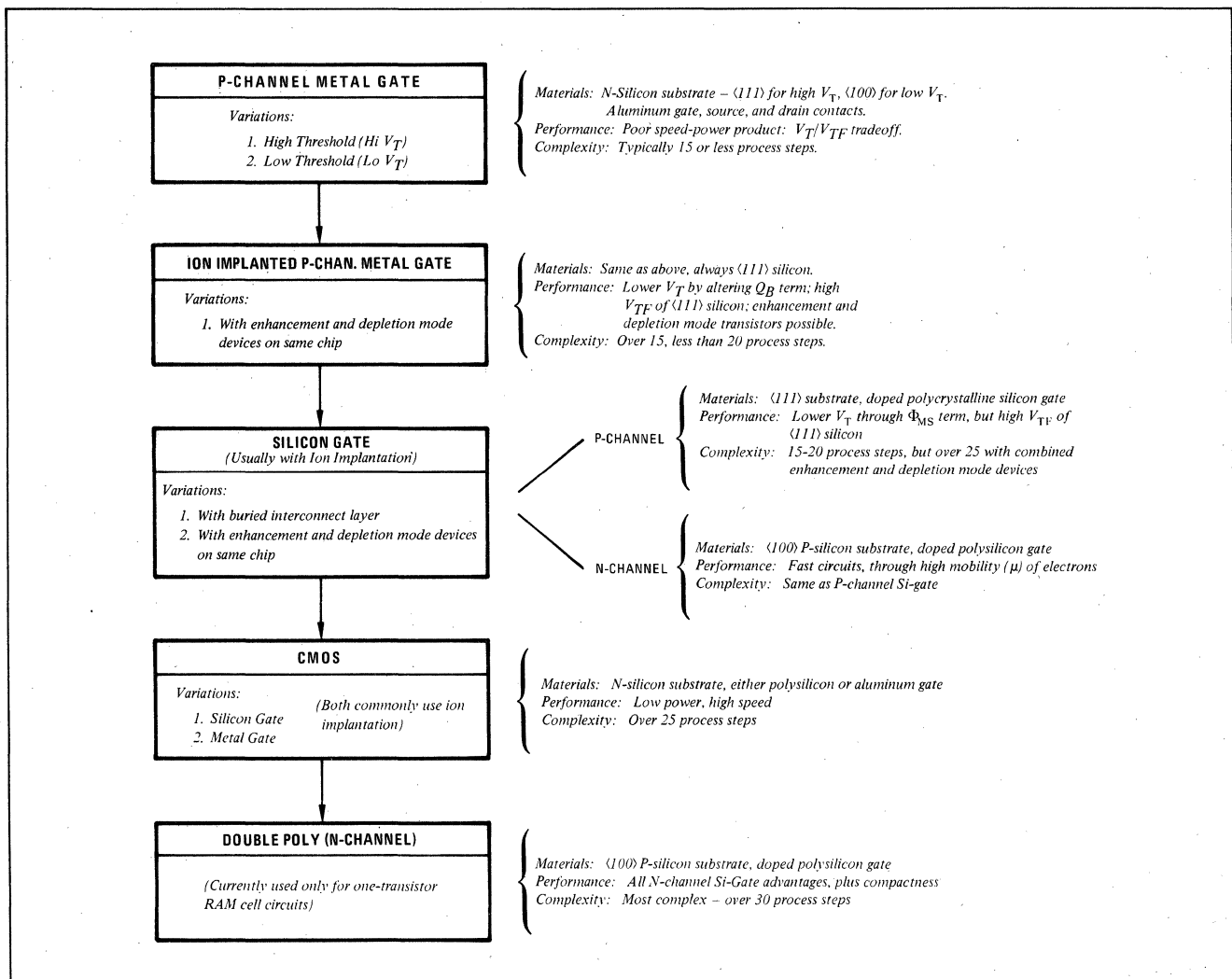
**PROCESS DESCRIPTIONS**

Each of the major MOS processes is described on the following pages. First, the established production proven processes are described, followed by those advanced processes, which are starting to go into volume production now. In each case, the basic processes is described first, followed by an explanation of its advantages, applications, etc. The less common processes, such as MNOS (metal-Nitride Oxide-Silicon) are not described.

**P-CHANNEL METAL GATE PROCESS**

Of all the basic MOS processes, P-channel Metal Gate is the oldest and the most completely developed. It has served as the foundation for the MOS/LSI industry and still finds

**FIGURE 11-8. SUMMARY OF MOS PROCESS CHARACTERISTICS**



use today in some devices. Several versions of this process have evolved since its earliest days. A cross-section of a P-channel metal gate MOS transistor is shown in Figure 11-3. A thin slice (8 to 10 mils) of lightly doped N-type silicon wafer serves as the substrate or body of the MOS transistor. Two closely spaced, heavily doped P-type regions, the source and drain, are formed within the substrate by selective diffusion of an impurity that provides holes as majority electrical carriers. A thin deposited layer of aluminum metal, the gate, covers the area between the source and drain regions, but is electrically insulated from the substrate by a thin layer (1000-1500 Å) of silicon dioxide. The P-channel transistor is turned on by a negative gate voltage and conducts current between the source and the drain by means of holes as the majority carriers.

The basic P-channel metal gate process can be subdivided in two general categories: *high-threshold* and *low-threshold*. Various manufacturers use different techniques (particularly so with the low threshold process) to achieve similar results, but the difference between them always rests in the threshold voltage  $V_T$  required to turn a transistor on. The high threshold  $V_T$  is typically -3 to -5 volts and the low threshold  $V_T$  is typically -1.5 to -2.5 volts.

The most common manner in which the difference in threshold voltages is achieved is by the use of substrates with different crystalline structures. The high  $V_T$  process uses (111) silicon, whereas the low  $V_T$  process uses (100) silicon. The difference in the silicon structure causes the inherent potential (work function) across the interface between the substrate and the silicon dioxide gate dielectric to change in such a manner that it lowers the threshold voltage  $V_T$ .

One of the main advantages of lowering  $V_T$  is the ability to interface the device with TTL circuitry. However, the use of (100) silicon carries with it a distinct disadvantage also. Just as the surface layer of the (100) silicon can be inverted by a lower  $V_T$ , so it also can be inverted at other random locations — through the thick oxide layers — by large voltages that may appear in the metal interconnections between circuit components. This is undesirable because it creates parasitic transistors, which interfere with circuit operation. The maximum voltage that can be carried in the interconnections is called the parasitic field oxide threshold voltage  $V_{TF}$ , (see Figure 11-3) and generally limits the overall voltage at which a circuit can operate. This, then, is the main factor that limits the use of the low  $V_T$  process. A drop in  $V_{TF}$  between a high  $V_T$  and low  $V_T$  process may, for example, be from -28V to -17V.

The low  $V_T$  process, because of its lower operating voltages, usually produces circuits with a lower operating speed than the high  $V_T$  process, but is easier to interface with other circuits, consumes less power, and therefore is more suitable for clocked circuits. Both P-channel metal gate processes yield devices slower in speed than those made by other MOS

processes, and have a relatively poor speed/power product. Both processes require two power supplies in most circuit designs, but the high  $V_T$  process, because it operates at a high threshold voltage, has excellent noise immunity.

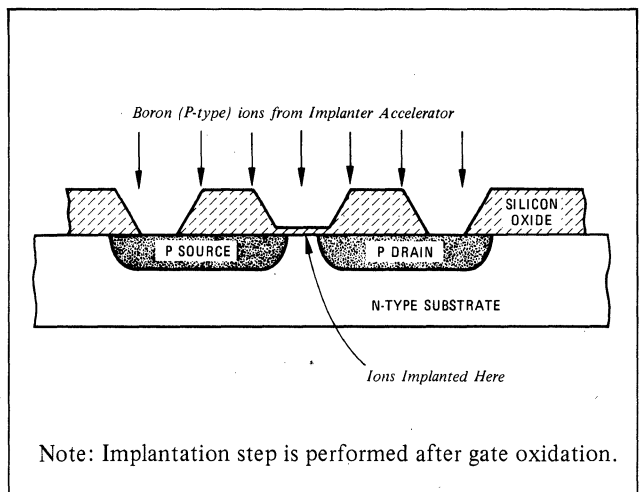
### ION IMPLANTED P-CHANNEL METAL GATE PROCESS

The P-channel Ion Implanted process uses essentially the same geometrical structure and the same materials as the high  $V_T$  P-channel process, but includes the ion implantation step. The purpose of ion implantation is to introduce P-type impurity ions into the substrate in the limited area under the gate electrode. By changing the characteristics of the substrate in the gate area, it is possible to lower the threshold voltage  $V_T$  of the transistor, without influencing any other of its properties.

Figure 11-9 shows the ion implantation step in a diagrammatic manner. It is performed after the gate oxide is deposited, but before the source, gate, and drain metallization deposition. The wafer is exposed to an ion beam which penetrates through the thin gate oxide layer and implants ions into the silicon substrate. Other areas of the substrate are protected both by the thicker oxide layer and sometimes also by other masking means. Ion implantation can be used with any process and, therefore could, except for the custom of the industry, be considered a special technique, rather than a process in itself.

The implantation of P-type ions into the substrate, in effect, reduces the effective concentration of N-type ions in the channel area and thus lowers the  $V_T$  required to turn the transistor on. At the same time, it does not alter the N-type ion concentration elsewhere in the substrate and therefore, does not reduce the parasitic field oxide threshold voltage  $V_{TF}$  (a

FIGURE 11-9. DIAGRAM OF ION IMPLANTATION STEP



problem with the low  $V_T$  P-channel Metal Gate process, described above). The  $\langle 111 \rangle$  silicon usually is used in ion-implanted transistors.

In fact, if the channel area is exposed to the ion beam long enough, the substrate in the area can be turned into P-type silicon (while the body of the substrate still remains N-type) and the transistor becomes a depletion mode device. In any circuit some transistors can be made enhancement type, while others are depletion type, and the combination is a very useful circuit design tool.

The Ion-implanted P-channel Metal Gate process is very much in use today. Among all the processes, it represents a good optimization between cost and performance and thus is the logical choice for many common circuits, such as memory devices, data handling (communication) circuits, and others.

Because of its low  $V_T$ , it offers the designer a choice of using low power supply voltages to conserve power or increase supply voltages to get more driving power and thus increase speed. At low power levels it is more feasible to implement clock generating and gating circuits on the chip. In most circuit designs only a single power supply voltage is required.

### P-CHANNEL SILICON GATE PROCESS

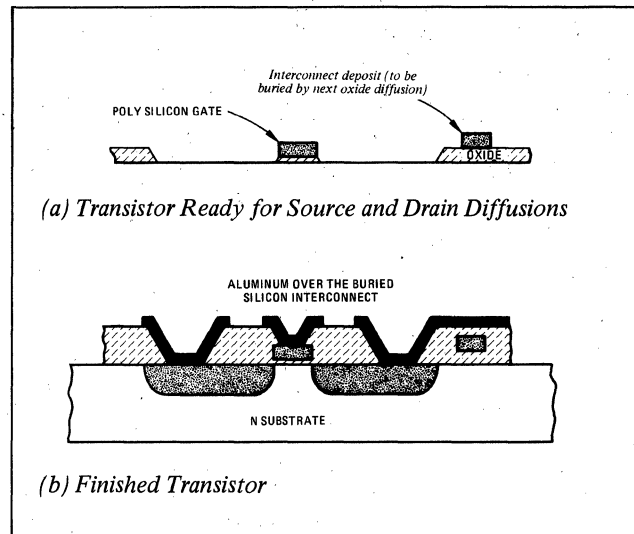
The Silicon Gate process is significantly different from the metal gate processes, in that it uses a polysilicon gate electrode material, rather than aluminum. Although the process is more complex than metal gate, several advantages arise from the basic change in materials.

Figure 11-10 shows the crosssection of a typical silicon gate P-channel transistor. The materials are the same as for metal gate, except the gate electrode is doped polycrystalline silicon (in this instance P-doped), which is deposited over the silicon oxide gate dielectric in an epitaxial reactor.

The first advantage of a polysilicon gate electrode is that it reduces the threshold voltage  $V_T$ , (by acting through the *work function*, described previously). Thus, the silicon gate gives the same advantage as either ion implantation or the change of substrate in the low  $V_T$  process. A typical  $V_T$  of a silicon gate P-channel transistor is -1 to -2 volts.

Another aspect of the silicon gate is the possibility of a buried layer of interconnect lines, in addition to the normal aluminum interconnections deposited on the surface of the chip. This gives the circuit designer more latitude in layout and often allows the reduction of the total chip size. Because the polysilicon gate electrode is deposited in a separate step, after the thick oxide layer is in place, the simultaneous deposition of additional polysilicon interconnect lines is only a matter of masking. These interconnect lines are buried by later steps, as shown in Figure 11-10.

FIGURE 11-10. CROSSSECTION OF A SILICON GATE MOS TRANSISTOR



One minor limitation associated with the buried interconnect lines is their location. Because the source and drain diffusions are done after the polysilicon is deposited [see (a) of Figure 11-10] the interconnect lines cannot be located over these diffusion regions.

A third advantage of a silicon gate is associated with the reduction of overlap between the gate and both the source and drain. This reduces the parasitic capacitance at each location and improves speed, as well as power consumption characteristics. Whereas in the metal gate process, the P region source and drain diffusion must be done prior to deposition of the gate electrode, in silicon gate process, the electrode is in place during diffusion, see (a) of Figure 11-10. Therefore, no planned overlap for manufacturing tolerance purposes need exist (as described under Capacitance, on page 11-9) and the gate is said to be *self-aligned*. The only overlap that occurs is due to the normal lateral extension of the source and drain regions during the diffusion process.

The silicon-gate process produces devices that are more compact than metal gate, and are slightly faster because of the reduced gate overlap capacitance. Because the basic silicon gate process is relatively simple, it is also economical. It is a versatile process that is used in memory devices and most any other circuit.

### N-CHANNEL PROCESS

Historically, N-channel process and its advantages were known well at the time when the first P-channel devices were successfully manufactured, however it was much more difficult to produce N-channel. One of the main reasons (described pre-



viously on page 11-5) was that the polarity of intrinsic charges in the materials combined in such a way that a transistor was on at 0V and had a  $V_T$  of only a few tenths of a volt (*positive*). Thus, the transistor operated as a marginal depletion mode device, without a well defined *on/off* biasing range. Attempts to raise  $V_T$  by varying gate oxide thickness and back biasing the substrate, created other objectionable results and it was not until research into materials, along with ion implantation, silicon gates, and other improvements came about that N-channel became practical for high density circuits.

The N-channel process gained its strength only after the P-channel process, ion implantation, and silicon gate all were already well developed. N-channel went into volume productions with advent of the 4K dynamic RAM and the microprocessor, both of which required speed and high density. Because P-channel processes were nearing their limits in both of these respects, N-channel became the logical answer.

The N-channel process is structurally different from any of the processes described so far, in that the source, drain, and channel all are N-type silicon, whereas the body of the substrate is P-type. Conduction in the N-channel is by means of electrons, rather than holes.

The main advantage of the N-channel process is that the mobility of electrons is about three times greater than that of holes and, therefore, N-channel transistors are faster than P-channel. In addition, the increased mobility allows more current flow in a channel of any given size, and therefore N-channel transistors can be made smaller. The positive gate voltage allows an N-channel transistor to be completely compatible with TTL. Figure 11-2 shows the crosssection of an N-channel transistor that uses both, a silicon gate and ion implantation.

Because N-channel is relatively new, however, its production techniques and variations in applications still are undergoing development. However, the combination of high speed, TTL compatibility, low power requirements, and compactness have already made N-channel the most widely used process. The cost of N-channel has been coming down also.

In addition to its use in large memory chips and microprocessors, N-channel has become a good general purpose process for circuits in which compactness and high speed are important. Most N-channel devices operate on a single +5V power supply and their threshold voltages range between +0.8 and +1.7. Higher voltages can be used to increase operating speed and a second supply voltage is required on devices that use substrate back bias.

## CMOS

The basic CMOS circuit is an inverter, which consists of two adjacent transistors — one an N-channel, the other a P-channel, as shown in Figure 2-11. The two are fabricated on the same substrate, which can be either N or P type.

The CMOS inverter in Figure 2-11 is fabricated on an N-type silicon substrate in which a P “tub” is diffused to form the body for the N-channel transistor. All other steps, including the use of silicon gates and ion implantation, are much the same as for other processes.

The main advantage of CMOS is its extremely low power consumption. When the common input to both gate electrodes is at a logic 1 (a positive voltage) the N-channel transistor is biased on, the P-channel is off, and the output is near ground potential. Conversely, when the input is at a logic 0 level, its negative voltage biases only the P-channel transistor on and the output is near the drain voltage  $+V_{DD}$ . In either case, only one of the two transistors is on at a time and thus, there is virtually no current flow and no power consumption. Only during the transition from one logic level to the other are both transistors on and current flow increases momentarily.

Silicon Gate CMOS is also fast, approaching speeds of bipolar TTL circuits. On the other hand, the use of two transistors in every device makes CMOS slightly more complex, costly, and requires more chip size. For these reasons, the original popularity of CMOS was in SSI logic elements and MSI circuits — logic gates, inverters, small shift registers, counters, etc. These CMOS devices constitute a logic family in the same way as TTL, ECL, and other bipolar circuits do and in the areas of very low power consumption, high noise immunity, and simplicity of operation, are still widely accepted by discrete logic circuit designers.

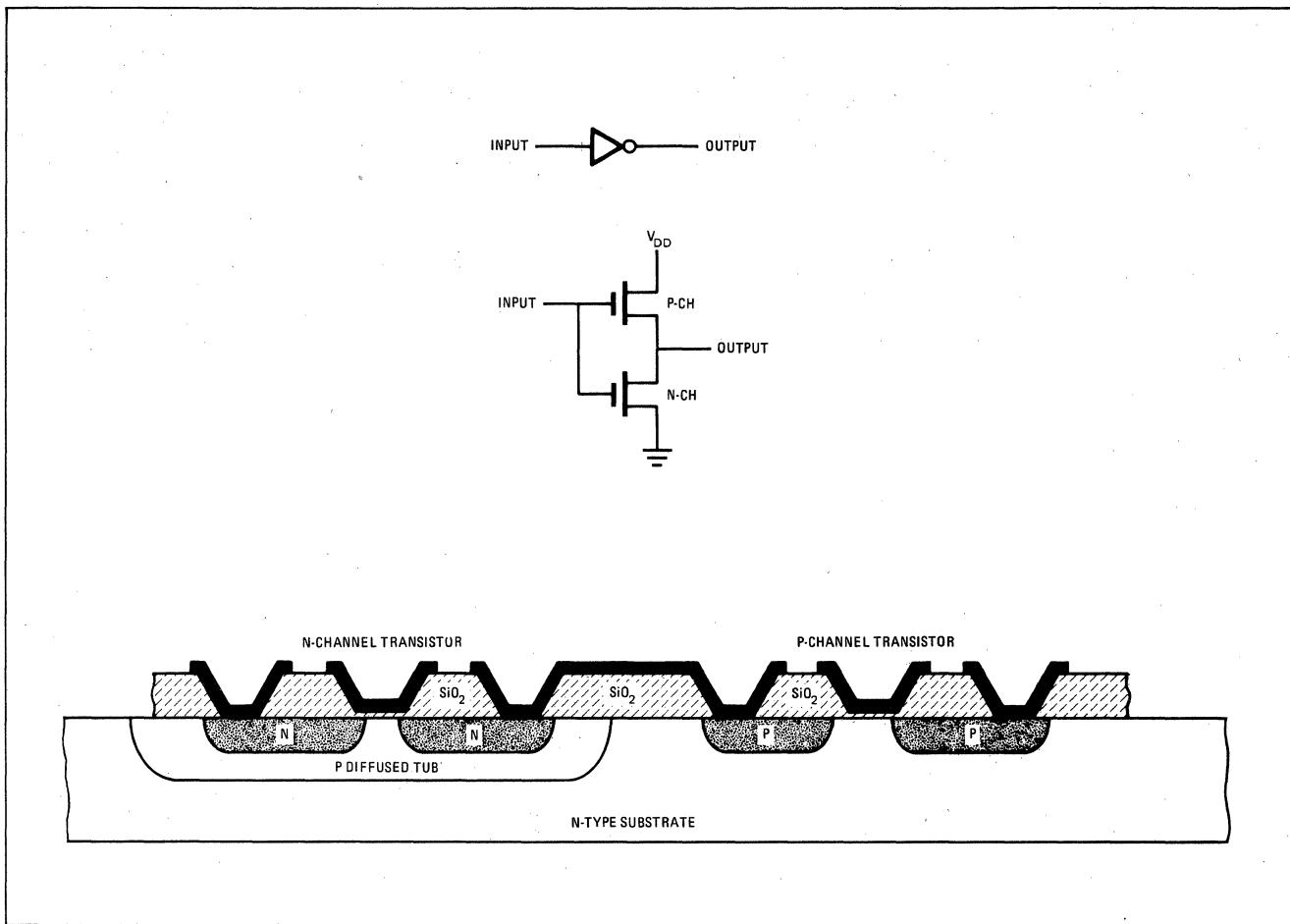
Low power CMOS circuits made the watch circuit possible and also have been used in space exploration, battery operated consumer products, and automotive control devices. As experience was gained with CMOS, tighter design rules and reduced device sizes have been implemented and now LSI circuits, such as 1K RAM memories and microprocessors, are being manufactured in volume.

CMOS circuits can be operated on a single power supply voltage, which can be varied from +3 to about +18 volts, with a higher voltage giving more speed and higher noise immunity.

## ADVANCED PROCESSES

Because large scale integration holds so much promise in the competitive integrated circuits industry, a massive and continuously increasing amount of research and development effort has gone into LSI processes since early and mid 1960's. One of the most active stimulants of process research, and thereby also a good example of its achievements, is the semiconductor memory. In 1969 the MOS industry did its best to come up with a memory device 256 bits large. Soon the 1K dynamic RAM followed and the continuous market demand for improved products has been so strong that the process technology has been pushed to the point where memories of 4, 8, and 16 thousand bit capacity are now commonplace.

FIGURE 11-11. CROSECTION AND SCHEMATIC DIAGRAM OF A CMOS INVERTER



Improvements in access speeds, reliability, and the cost-per-bit all have advanced by a similar scale.

The latest MOS RAMs are static and match access speeds of bipolar memories (below 50 nanoseconds), while maintaining the low cost and high packing density characteristic of MOS. In size, the industry has firmly set its sights on the 65K bit memory.

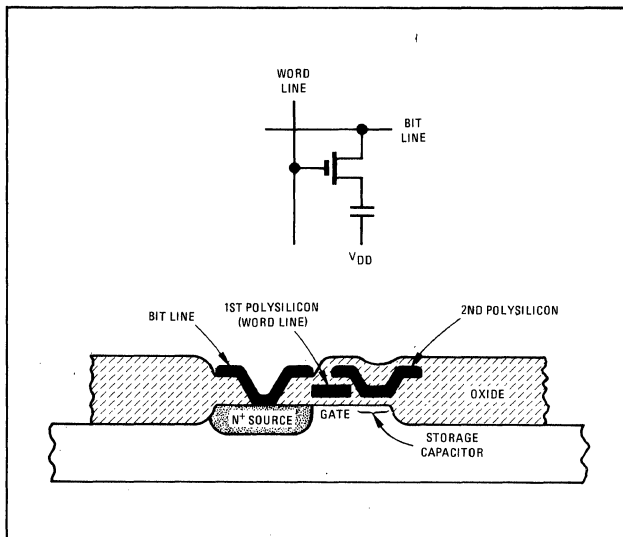
This incredible technology leap has come about because MOS process research has been able to come up with a continuous stream of innovations. At the time of publication of this document, several new MOS processes are coming into production, and several more are off in the future only by a product generation or two. In the first category is Double Poly (or Split Gate), VMOS, and D-MOS (which are all described separately below), but in the second category there is Silicon-on-Sapphire (SOS), several mechanically small but technically significant variations on existing processes, and the CCD (Charge Coupled Device) technology application to high density memories.

### DOUBLE POLY

Double Poly (also referred to as Split Gate) is actually not a full MOS process in the usual sense, because it is currently used only in a particular transistor-capacitor configuration. Using a simplified N-channel transistor, the double poly process is used to construct the random access memory cell shown in Figure 11-12.

The source diffusion and gate structure is essentially as in a classical N-channel transistor, but in place of the drain there is a storage capacitor. When voltages are applied both to the source and to the gate (during write operation), charge flows from the source through the channel into the capacitor, and remains there after removal of gate voltage. To sense the charge (during read), the gate voltage is turned on and the charge flows thru the source diffusion onto the bit line, where it is detected by a sense amplifier. In this manner the transistor-capacitor functions as a single-transistor dynamic RAM cell.

**FIGURE 11-12. DOUBLE POLY SINGLE-TRANSISTOR RAM CELL**



The main advantage of the double poly RAM cell is its compactness. The gate polysilicon layer is overlapped by the capacitor polysilicon and thus uses about half of the space of a typical N-channel 4K one-transistor RAM cell (though more than a VMOS RAM cell). For this reason the double poly cell is used in most 16K RAMs.

The basic double polysilicon layer concept, including the accompanying possibility of an added buried interconnect layer (same as was described for the P-channel Silicon Gate process above), can also be extended in the future into random logic design.

## VMOS

AMI's patented VMOS process is a significant departure from the other processes described so far. The VMOS transistor is constructed along the sides of a V-shaped groove, that has been etched into the silicon, as shown in the simplified diagram of Figure 11-13(a). (A distinction arises between the VMOS transistor and the planar transistor, whose source, gate, and drain are laid out in the usual manner, along the surface plane of the substrate.)

The source is a heavily N doped region, diffused into the substrate (heavy doping is denoted by + after the N). An epitaxially grown layer over the source constitutes the channel. The lower part of this layer is more heavily P-doped and its depth determines the effective channel length. The upper part, designated  $\pi$ , is very lightly P-doped and is used as an isolating layer, to improve device performance characteristics (as described below). The drain is a heavily N-doped diffusion on the surface of the structure.

The gate oxide and gate electrode are deposited all along the bias surfaces of the V-groove, as shown in the crosssection (b), and a field oxide layer extends over the drain. On the surface of a die, the VMOS transistor appears as in (c).

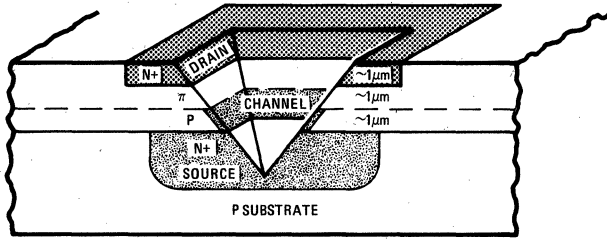
In producing a VMOS device, the source diffusion, epitaxial growth of the channel layer, drain diffusions and insulating oxide all are completed first and only then the V-groove is etched. The precise V shape of the groove results because of the interaction of the etchant with the anisotropic crystal structure.

The VMOS process has several significant advantages:

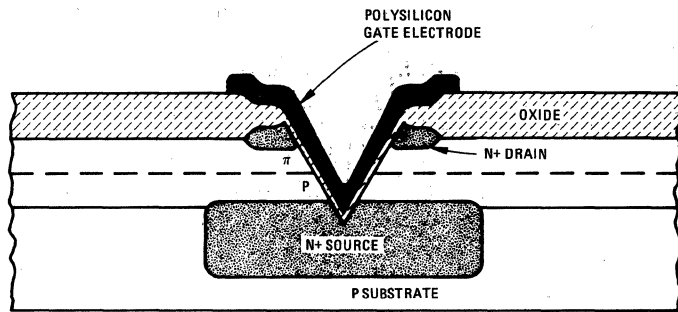
- Because it uses the sides of the V-groove for device construction, the VMOS transistor requires a much smaller chip surface area than any planar transistor. For this reason, very high density circuits can be built with VMOS.
- Devices with very short channels and large  $W/\ell$  ratios can be built, making possible the design of very high speed circuits, that can carry large currents. In any planar process the channel length can be no smaller than the physical limits of photolithographic masks, whereas in VMOS the effective channel length is controlled only by diffusion and epitaxial thickness, and can be  $2 \mu\text{m}$  or less. On the other hand, channel width is the perimeter distance around all four sides of the V-groove (at the channel elevation) and this clearly is an advantage in getting a high  $W/\ell$  ratio without using up a large surface area. (The perimeter distance is 2-3 times that of a corresponding chip surface area planar device.)
- The  $\pi$  type epitaxial layer isolates the heavily doped  $N^+$  drain from the P channel and thus reduces substrate-to-drain capacitance and increases drain breakdown voltage. Other parasitic capacitances are also typically smaller than those of planar devices and so the overall power consumption at a given operating speed is smaller than that of other processes (with the exception of CMOS).

On the strength of its density and speed advantages, VMOS appears to be most promising for next generation memories — the 16K and larger RAMs. However, various other device configurations, besides the floating source transistor shown in Figure 11-13, are possible and thus VMOS can become a good all-purpose process — usable on ROMs, EPROMs, microprocessors, and random logic. For example, in a ROM the  $N^+$  source diffusion is eliminated and instead, the entire substrate is N type. In this manner all the cells have a common grounded source and a very simple straightforward structure results.

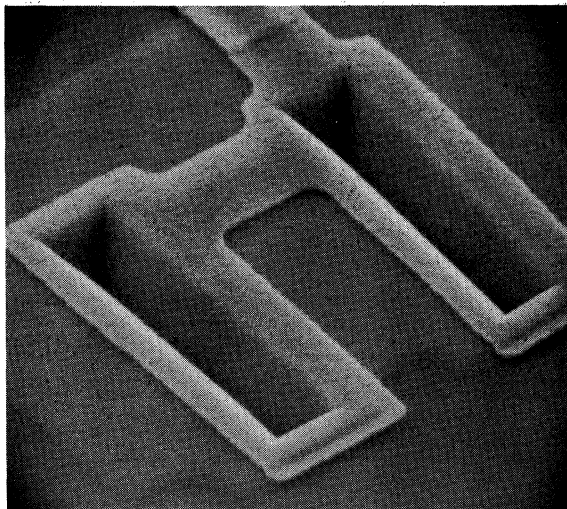
FIGURE 11-13. THE VMOS TRANSISTOR



a. The V-groove of a Floating Source VMOS Transistor



b. Crosssection of a Completed Floating Source VMOS Transistor



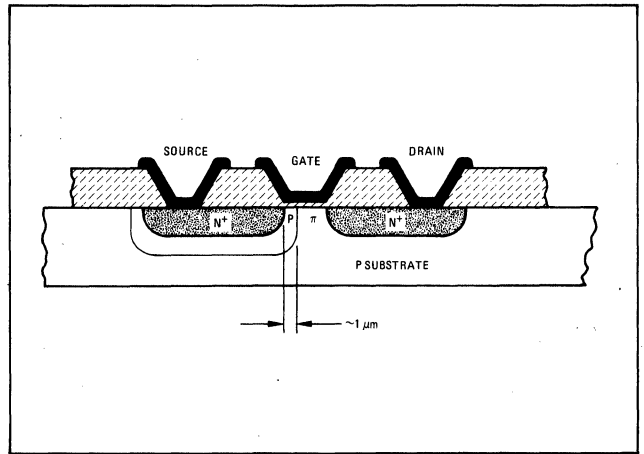
c. Photograph of Two Parallel VMOS Transistors with Surface V-Groove Dimensions of  $6\mu\text{m} \times 23\mu\text{m}$

## D-MOS

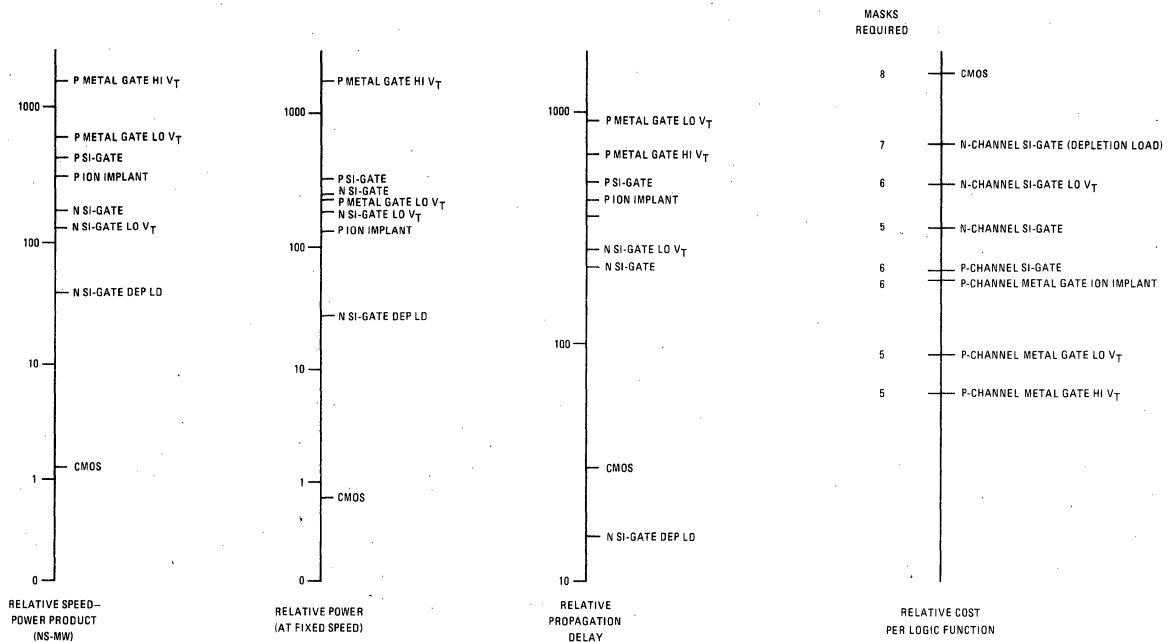
The D-MOS, or double-diffused processes, is similar to VMOS in that it sidesteps the photolithographic masking dimensional limitations and creates a short P/π channel MOS transistor by a diffusion step. Unlike VMOS, however, D-MOS is a planar process and similar to N-channel in other respects.

To make the transistor shown in Figure 11-14, a P-diffusion of the source area is followed by an N-diffusion, so that the result is an N<sup>+</sup> source located within a larger P tub. As can be seen in the figure, the lateral expansion difference between the two diffusions creates a P channel region. By controlling the duration of the two sequential diffusions, the P channel length, and thereby the device characteristics, are determined. The resulting transistor is fast and can carry high currents.

FIGURE 11-14. THE D-MOS TRANSISTOR



### Comparative Data on Major MOS Processes





American Microsystems, Inc.  
3800 Homestead Road  
Santa Clara, California 95051  
408 246-0330