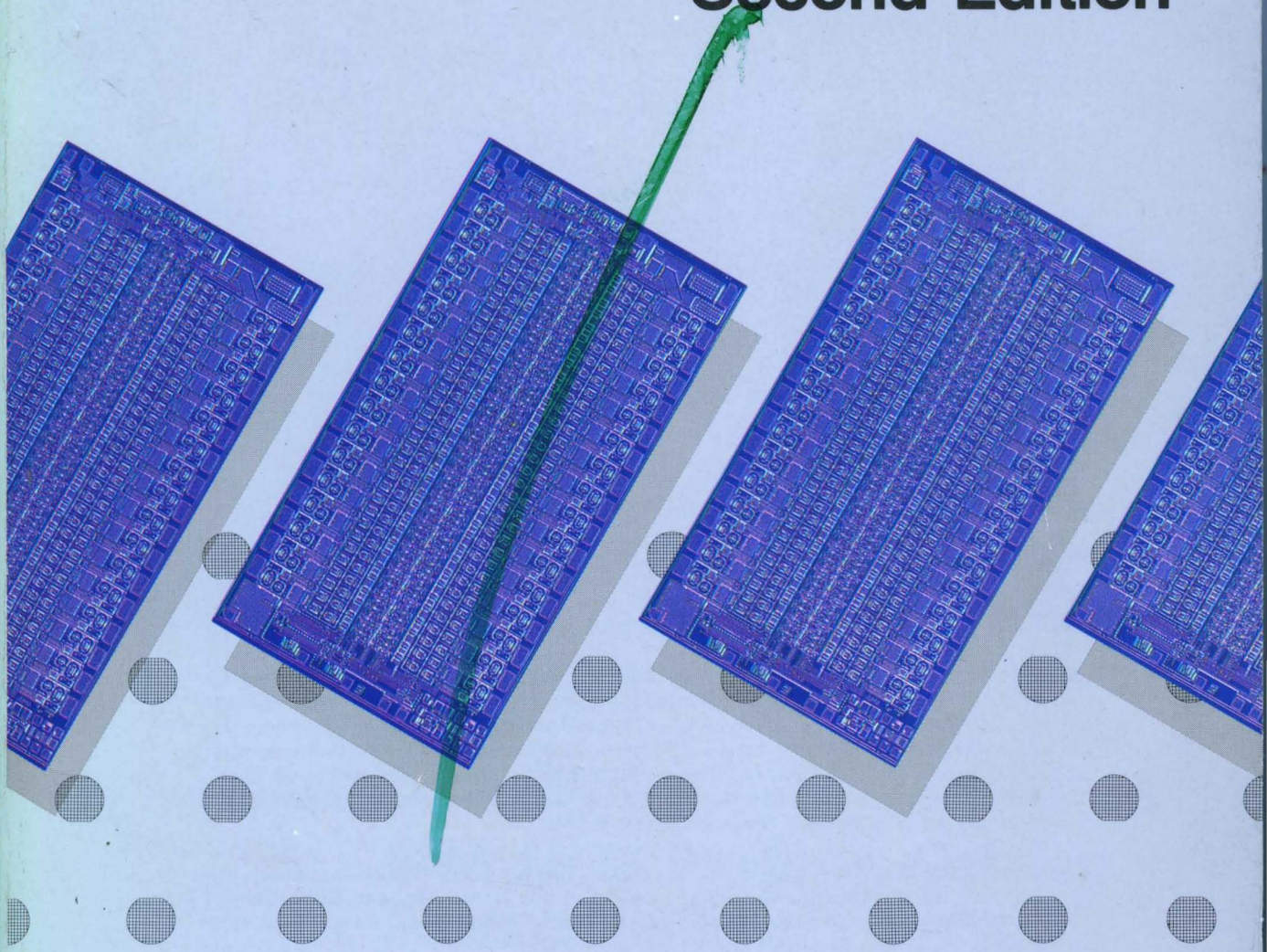
1984 MOS Products Catalog
Second Edition



GOULD

AMI Semiconductors

GOULD
AMI Semiconductors

Information furnished by Gould AMI in this publication is believed to be accurate. Devices sold by Gould AMI are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Gould AMI makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Gould AMI makes no warranty of merchantability or fitness for any purposes. Gould AMI reserves the right to discontinue production and change specifications and prices at any time and without notice.

Advanced Product Description means that this product has not been produced in volume, the specifications are preliminary and subject to change, and device characterization has not been done. Therefore, prior to programming or designing this product into a system, it is necessary to check with Gould AMI for current information.

Preliminary means that this product is in limited production, the specifications are preliminary and subject to change. Therefore, prior to programming or designing this product into a system, it is necessary to check with Gould AMI for current information.

These products are intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically **not** recommended without additional processing by Gould AMI for such application.

MOS Products Catalog-30M-6/84-Printed in U.S.A.

AMI®

A Subsidiary
of Gould Inc.

1984 MOS Products Catalog
Second Edition

AMI®

A Subsidiary of Gould Inc.

Introduction

American Microsystems, Inc. headquartered in Santa Clara, California is the semiconductor industry leader in the design and manufacture of custom MOS/VLSI (metal-oxide-silicon very-large-scale-integrated) circuits. It manufactures special circuits for the leading computer manufacturers, telecommunications companies, automobile manufacturers and consumer product companies worldwide. AMI is a wholly owned subsidiary of Gould, Inc.

Along with being the leading designer of custom VLSI, AMI is a major alternate source for the S6800 8-bit microprocessor family and the S80 Family of microprocessors, which are integrated systems in silicon based on the popular Z80™ microprocessor. This microprocessor family combines advanced microprocessor, memory, and custom VLSI technologies on a single chip.

The company provides the market with selected low power CMOS Static RAMs, and 16K, 32K, 64K, 128K and 256K ROMs for all JEDEC pinouts or as EPROM replacements.

The most experienced designer of systems-oriented MOS/VLSI communication circuits, AMI provides components for station equipment, PABX and Central Office Switching systems, data communications and advanced signal processing applications.

AMI is a leading innovator in combining digital and analog circuitry on a single silicon chip, and is a recognized leader in switched capacitor filter technology.

Processing technologies range from the advanced, small geometry, high performance silicon gate CMOS to mature PMOS metal gate and to silicon gate N-Channel. Over 27 variations are available.

AMI has design centers in Santa Clara; Pocatello, Idaho; and Swindon, England. Wafer fabrication plants are in Santa Clara and Pocatello, and assembly facilities are in Seoul, Korea and the Philippines. A joint venture company in Graz, Austria Microsystems International, serves the European semiconductor market with complete design and manufacturing capabilities. A recently formed joint venture company in Japan, Asahi Microsystems Inc., designs and will in the future produce integrated circuits for the Japanese and Pacific Basin market.

Field sales offices are located throughout the United States, in Europe and in the Far East. Their listing, plus those of domestic and international representatives and distributors appear on pages B.39 through B.47 of this publication.

Z80 is a registered trademark of Zilog, Inc.

Table of Contents

AMI®

A Subsidiary
of Gould Inc.

Indices

Indices

Numerical Index

Indices

Functional Index

Functional Index

Cross Reference Guide

Communication Products

Cross Reference by Manufacturer

Manufacturer	Part Number	AMI Functional Equivalent Part
AMD	7910	S3530
Cherry	820X	S2561
ERSO	CIC 9187	2559
ERSO	CIC 9110E	S25610
EXAR	XR2120	S35212
G.I.	ACF 7310,12,7410	3526
G.I.	ACF 7323C	3525
G.I.	ACF 7363C	3525
G.I.	ACF 7383C	3525
G.I.	AY5-9100	2560A
G.I.	AY5-9151	2560A
G.I.	AY5-9152	2560A
G.I.	AY5-9153	2560A
G.I.	AY5-9154	2560A
G.I.	AY5-9158	2560A
G.I.	AY5-9200	2563A
G.I.	AY3-9400	2559
G.I.	AY3-9401	2559
G.I.	AY3-9410	2559
G.I.	AY5-9800	3525
Hitachi	HD 44211	3507
Hitachi	HD 44231	3506
Intel	2913	3507
Intel	2914	3507
Intersil	ICM 7206	2559
Mitel	MT 4320	3525
Mitel	ML 8204	2561A
Mitel	ML 8205	2561A
Mitel	MT 8865	3525
Mitel	8204	S2561
Mostek	MK 5087	2559E
Mostek	MK 5089	25089
Mostek	MK 50981	2560A
Mostek	MK 50982	2560A
Mostek	MK 50991	2560A
Mostek	MK 50992	2560A
Mostek	MK 5116	3507
Mostek	MK 5151	3507
Mostek	MK 5170	2562/2563
Mostek	MK 5175	25610
Mostek	MK 5387	2559
Mostek	MK 5389	25089
Mostek	5091	2559
Mostek	5092	2559
Mostek	5094	2559
Mostek	5382	2569
Mostek	5170	2563A
Mostek	5175	S25610
Mostek	5380	2559
Motorola	MC 14400	3507
Motorola	MC 14401	3507
Motorola	MC 14402	3507
Motorola	MC 14408	2560A
Motorola	MC 14409	2560A
Motorola	MC14412	S3530
Motorola	MC6170	S35212
Motorola	MC145433	S3526/S3526M
Motorola	MC145432	S3526M*
Motorola	MC14413	S3526/S3526M
National	TP53130	S2579
National	TP5088	S2579
National	MF10	S3528/S3529

* For Direct Replacement

Note: X Denotes any number

Communication Products

Cross Reference by Manufacturer

Manufacturer	Part Number	AMI Functional Equivalent Part
National	MF6	S3528/S3529
National	MM74HC942	S3530
National	MM74HC943	S3530
National	MM 5393	2560A
National	MM 5395	2559
National	TP5700	S2550
NEC	μPD 7720	2811
Nitron	NC 320	2560A
Phillips	TDA 1077	2559
RCA	CD 22859	2559
Reticon	R5632	S35212*
Reticon	R5612	S3526/S3526M
Reticon	R5604	S3528/S3529
Reticon	R5605	S3528/S3529
Reticon	R5606	S3528/S3529
Reticon	R5609	S3528/S3529
Reticon	R5611	S3529
Reticon	R5612	S3528/S3529
Reticon	R5614	S3528/S3529
Reticon	R5615	S3528/S3529
Reticon	R5616	S3528/S3529
Reticon	R5620	S3528/S3529
Reticon	R5621	S3528/S3529
Reticon	R5622	S3528/S3529
Sanyo	7350	S2560A
Sanyo	7351	S2560A
Seiko	S7220A	S2560A
Seiko	STC2560	S2560A
Seiko	S7210A	S25610
Sharp	408X	2559
Siliconix	DF 320	2560A
Siliconix	DF 321	2560A
Siliconix	DF 322	2560A
T.I.	TCM 170X	S2550
T.I.	TCM 5089	S25089*
T.I.	TCM 509X	2559
T.I.	TCM 508X	2559
T.I.	TCM 150X	S2561
T.I.	TMS 99532	S3530
SSI	201	S3525A
SSI	202	S3525A
SSI	203	S3525A
Teltone	M-980	S3524
Teltone	M-900	S3525A
Teltone	M-907	S3525A
Teltone	M-917	S3525A
Teltone	M-927	S3525A
Teltone	M-947	S3525B*
Teltone	M-948	S3525A
Teltone	M-056	S3525A
Teltone	M-957	S3525A
Teltone	M-967	S3525A

* For Direct Replacement

Note: X Denotes any number

Cross Reference Guide

Memory Products

CMOS RAMs

Vendor	256 × 4	1K × 1	1K × 4	4K × 1
AMI	S5101		S6514	
FUJITSU	—	—	6514/8414	8404
HARRIS	6561	6508	6514	6504
HITACHI	435101	—	4334	4315
INTERSIL	6551	6508	6514	6504
MOTOROLA	145101	146508	—	146504
NATIONAL	74C920	74C929	6514	6504
NEC	5101	6508	444/6514	—
OKI	573	574	5115	—
RCA	5101	1821	1825	5104
SSS	5101	5102	—	—
TOSHIBA	5101	5508	5514	5504

BYTE WIDE NMOS ROMs

Vendor	2K × 8	4K × 8	4K × 8*	8K × 8-24 Pin	8K × 8-28 Pin	16K × 8	32K × 8
AMI	S68A316	S68A332	S2333	S68A364	S2364A	S23128A	S23256B
AMD	AM9218	9232	9233	AM9264	AM9265	AM92128	
NEC/EA	μPD2316	μPD2332A	μPD2332B	μPD8364	μPD2364	μPD23128	μPD23256
FAIRCHILD	F68316	F3532	F3533	F3564			
FUJITSU							
GI	R03-9316		R03-9333	R03-9364	R03-9365	SPR-128	
GTE	2316	2332		2364			
MOS				MPS2364			
MOSTEK	MK34000			MK36000	MK37000		MK38000
MOTOROLA	MCM68A316	MCM68A332		MCM68365			MCM65256
SIGNETICS	2616	2632		2664A	2664AM	23128	23256
SYNERTEK	SY2316	SY2332	SY2333	SY2364	SY2365	SY23128	SY23256
OKI	MSM2916						
ROCKWELL	R2316	R2332		R2364A	R2364B		
SGS	M2316						
TOSHIBA	TSU2316		TSU333-2				
NATIONAL		MM52132		MM52164			
VTI		VT2332	VT2333		VT2365A	VT23129	VT23256

*Pin compatible with 2732 EPROM

DEVICE	DESCRIPTION	1.5MHz "A" VERSION	2.0MHz "B" VERSION		0 – 70°C	–40/+85°C 1MHz	ROM PROGRAMMABLE	REPLACES
S1602	UART (UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER)			P C D	P C D			S1883, MB8868A, AY-5-1013, AY-3-1015, TR1863, □□ TR1602, TMS6011, NATIONAL 5303, SMC2502
S2350	USRT (UNIVERSAL SYNCHRONOUS RECEIVER/TRANSMITTER)			P C D	P C D			
S6800	MPU (MICROPROCESSOR)	X	X	P C D	P C D			MC6800, HD46800D, F6800
S6801	8-BIT MICROCOMPUTER 2K ROM, 128 BYTES RAM, UART, TIMER, I/O			P C D	C D	X		MC6801, HD6801X
S6802	8-BIT MICROPROCESSOR WITH CLOCK AND 128 BYTES RAM	X	X	P C	P C			MC6802, HD46802, F6802
S6803	S6801 WITHOUT ROM			P C D	C			MC6803
S6803NR	S6803 WITHOUT RAM			P C D	C			MC6803NR
S6805	8-BIT MICROCOMPUTER WITH 1.1K BYTES ROM, 64 BYTES RAM, TIMER, I/O			P C D	P C D	X		MC6805P2, HD6805S
S6808	MICROPROCESSOR AND CLOCK	X	X	P C	P C			MC6808, HD46808, F6808
S6809	ENHANCED 8-BIT MPU	X	X	P C D	P C D			MC6809, HD6809, F6809E
S6809E	ENHANCED 8-BIT MPU EXTERNAL CLOCK INPUT			P C D	P C D			MC6809E, HD6809E, F6809E
S6810	RAM (128x8)	X	X	P C D	P C D			MC6810, HD46810, F6810
S6810-1	RAM LOW COST (575ns)			P C D	P C D			
S6821	PIA	X	X	P C D	P C D			MC6821, HD46821, F6821, SY6520 □□
S6840	TIMER	X	X	P C D	P C D			MC6840, HD46840, F6840
S6846	ROM, I/O, TIMER	X	X	P C D	P C D	X		MC6846, HD46846, F6846
S6850	ACIA	X	X	P C D	P C D			MC6850, HD46850, F6850
S6852	SSDA	X	X	P C D	P C D			MC6852, HD46852, F6852
S6854	ADLC	X	X	P C D	P C D			MC6854, HD46854, F6854
S68045	CRT CONTROLLER	X	X	P C D	P C D	X		MC6845, HD46505, SY6545□□
S6551/6551A	ACIA/BAUD RATE GENERATOR		X	P C D	P C D			SY6551, ROCKWELL 6551
S9900	16-BIT MICROPROCESSOR			P C				TMS9900
S9980A	16-BIT μPROCESSOR—8-BIT DATA BUS			P C D				TMS9980A
S9901	PCI			P C D				TMS9901
S9902	ACC			P C D				TMS9902

PART NUMBER CONVENTIONS

S = AMI PRODUCT PREFIX
68 = FAMILY DESIGNATION
A = BUS SPEED (OPTIONAL)
NONE – 1MHz
A = 1.5MHz
B = 2.0MHz

00 = PART DESIGNATION
I = QUALIFIER (OPTIONAL)
NONE 0–70°C
I –40/+85°C

P = PACKAGE TYPE
P = PLASTIC
C = CERAMIC
D = CERDIP

□□ FUNCTIONAL REPLACEMENT

☒ = AVAILABLE □ = NOT AVAILABLE OR NOT APPLICABLE

AMI®

A Subsidiary of Gould Inc.

Gate Arrays

I. Introduction

As the semiconductor industry has marched into the new era of VLSI, a new market has appeared—fast turn custom or, as it is now called, semicustom. AMI, a leader in custom MOS since 1966, is also a leader in this new semicustom market. AMI has introduced CAD software and hardware tools to allow customers to design, simulate, and layout circuits using AMI gate array and standard cell families. Figure 1-3 show the economic tradeoffs between gate array, standard cell, and full custom, all of which are offered by AMI. The best solution for your needs will depend upon your volume requirements and circuit complexity.

Figure 1. Cost vs. Volume Alternatives

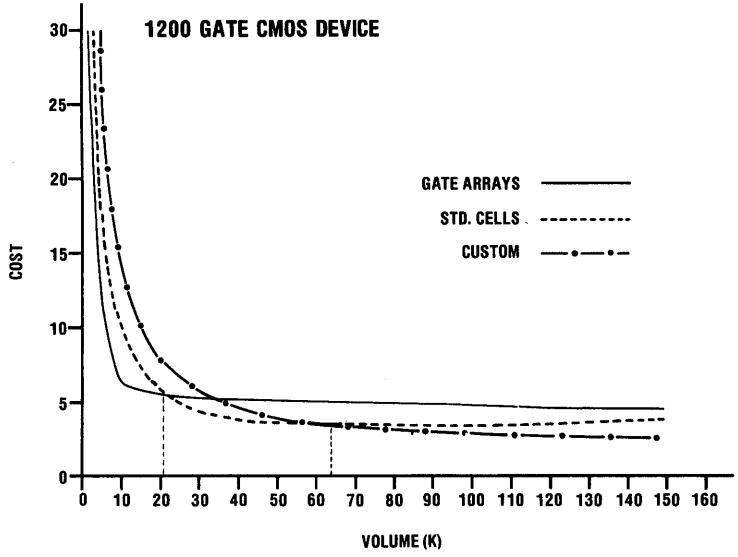


Figure 2. Cost vs. Volume Alternatives

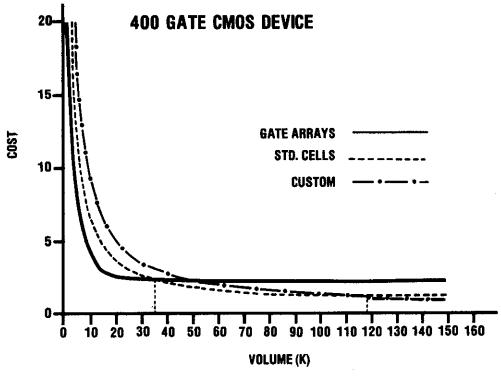
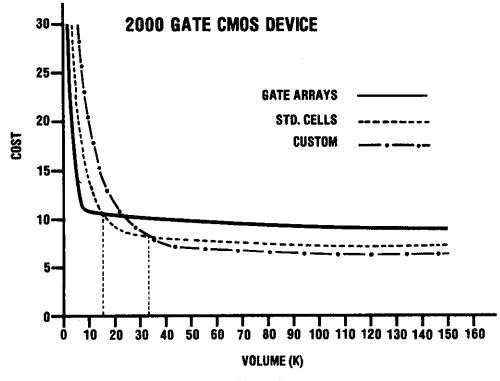


Figure 3. Cost vs. Volume Alternatives



Gate Arrays

The simplest semicustom ICs are gate arrays. A gate array consists of uncommitted component matrices of transistors (usually P- and N-type for CMOS) that allow user-defined interconnections through a single or double layer of metal. Since arrays employ fixed component locations and geometries, AMI can process the wafers up to the metallization stage and inventory the wafers for future customization. Thus gate arrays look like late mask programmable ROMs and benefit from this large-volume production because they appear to be a standard product. AMI can offer them at an economical price and with fast prototyping and production turn on spans.

The second semicustom product group is standard cells. Standard cells employ fully customized process/mask sets and must pass through all process steps before a user-specified circuit is completed. To design such chips, AMI customers use precharacterized functional cells from AMI cell libraries. Placing and routing the cells is done on AMI computers using specially developed software. Standard cell designs usually result in smaller chips since only the component structures required for the user specified circuit are included, thus chips designed with cells are less expensive than gate array designed chips.

The key to success in this new market is flexibility. Flexibility to the user entails: low risk circuit implementation, short development span, lower development cost, lower piece part cost (over discrete implementations), easy to change or modify, enhanced product features, etc. For the manufacturer, flexibility means: ease of manufacture, economies of scale, and easy interface with customers. One last point: AMI offers the user the opportunity to migrate at a low cost, from a gate array to a standard cell (or possibly full custom) to further enhance his/her product. By using analog cells, significant advances in chip function integration are at the user's disposal.

In addition, AMI offers a wide selection of packages to meet specific user needs. AMI offers the CAD tools needed to work in the new market. AMI also offers the training required to move customers quickly and easily into this new technology. See the "Custom Solutions" section in this catalog for more details.

2 Micron Products

AMI is developing 2 micron CMOS technology to support the next generation of gate arrays and standard cells. These products will offer size and performance improvements of up to 50% from their 3 micron counterparts.

Introduction of the first 2 micron gate array family is planned for fourth quarter 1984 and is expected to offer capabilities of up to 10,000 gates.

II. Gate Arrays

- Arrays of Uncommitted CMOS Transistors Programmed by Metal Layer Interconnect to Implement Arbitrary Digital Logic Functions
- Multiple Developmental Interfaces: AMI or Customer Designed
- Three Array Families—5-Micron Single Metal CMOS, 3-Micron Single Metal CMOS, and 3-Micron Double Metal Versions
- Multiple Array Configurations—From 300 to 1260 Gates for 5-Micron Devices, and 500 to 4000 Gates for 3-Micron Devices
- Quick Turn Prototypes and Short Production Turn-On Time
- Economical Semicustom Approach for Low-to-Medium Production Volume Requirements
- Advanced Oxide-Isolated Silicon Gate CMOS Technology
- High Performance—2 to 3ns Typical Gate Delay for 3-Micron Devices
- Broad Power Supply Range
- TTL or CMOS Compatible I/O
- Up to 124 I/O Connections
- Numerous Package Options
- Full Military Temperature Range (−55°C to 125°C) and MIL-STD-883 Class B Screening Available

Five-Micron Gate Array Family

The family of 5-micron CMOS products is offered in six configurations with circuit complexities equivalent to 300, 400, 540, 770, 1000, and 1260 two-input gates, respectively. All pads can be individually configured as inputs, outputs, or I/O's. Input switching characteristics can be programmed for either CMOS or TTL compatibility. LS buffer output drivers will support CMOS levels of two low power schottky TTL loads. TTL buffer outputs will also provide CMOS levels and are capable of driving up to six LS TTL loads. All output drivers can be programmed for tri-state or open drain (open collector) operation as required.

General Description

AMI's gate array products consist of arrays of CMOS devices whose interconnections are initially unspecified. By "programming" interconnect at the metal layer mask level, virtually arbitrary configurations of digital logic can be realized in an LSI implementation.

AMI gate array designs are based on topological cells—i.e., groups of uncommitted silicon-gate N-Channel and P-Channel transistors—that are placed at regular intervals along the X and Y axes of the chip with intervening polysilicon underpasses. Pads, input protection circuitry, and uncommitted output drivers are placed around the periphery.

Compared to SSI/MSI logic implementations, AMI's gate array approach offers lower system cost and, in addition, all the benefits of CMOS LSI. The lower system cost is due to significant reductions in component count, board area and power consumption. Product reliability, a strong function of component count, is thereby greatly enhanced. And compared to fully custom LSI circuits, the gate array offers several advantages: low development cost; shorter development time; shorter production turn-on time; and low unit costs for small to moderate production volumes.

AMI's CMOS gate arrays are offered in three families: the 5-micron UA series, the 3-micron single metal GA series, and the 3-micron double metal GA-D series. The 5-micron UA series has been in production since 1980 and well over one hundred circuits have been produced in that technology. The 3-micron GA and GA-D series are the high-speed high-density devices fabricated in AMI's state-of-the-art 3-micron CMOS processes.

The CMOS technology used for these products is AMI's 5-micron, oxide-isolated, silicon gate CMOS process. This process offers all the conventional advantages of CMOS—i.e., very low power consumption, broad power supply voltage range (3V to 12V ± 10%), and high noise immunity—as well as dense circuits with high performance. Gate propagation delays are in the five to ten ns range for 5 volt operation at room temperature. AMI gate array products can be supplied in versions intended for operation over the standard commercial temperature range (0°C to +70°C), the industrial range (−40°C to +85°C), or the full military range (−55°C to +125°C). MIL-STD-883 Class B screening, including internal visual inspection and

high temperature burn-in, is offered. Similarly, customer-specified high reliability screening is available for commercial and industrial applications.

Table 1. Gate Array SSI Functional Macros

DESCRIPTION	TTL FUNCTIONAL EQUIVALENCE	GATE COUNT
INVERTER	1/6 LS04	1
DUAL-INVERTER DRIVER	1/6 LS04	1
TRIPLE-INVERTER DRIVER	1/6 LS04	2
QUADRUPLE-INVERTER DRIVER	1/6 LS04	2
QUINTUPLE-INVERTER DRIVER	1/6 LS04	3
2-INPUT NAND	1/4 LS00	1
3-INPUT NAND	1/3 LS10	1.5
4-INPUT NAND	1/2 LS20	2
5-INPUT NAND	—	2.5
2-INPUT AND	1/4 LS08	1.5
3-INPUT AND	1/3 LS11	2
4-INPUT AND	1/2 LS21	2.5
2-INPUT NOR	1/4 LS02	1
3-INPUT NOR	1/3 LS27	1.5
4-INPUT NOR	—	2
5-INPUT NOR	1/2 S260	2.5
2-INPUT OR	1/4 LS32	1.5
3-INPUT OR	—	2
4-INPUT OR	—	2.5
EXCLUSIVE OR	1/4 LS86	2.5
EXCLUSIVE NOR	—	2.5
2-IN AND/2-IN NOR	—	1.5
2-WIDE AND-OR-INVERT	1/2 S51	2
2-IN OR/2-IN NAND	—	1.5
2-WIDE OR-AND-INVERT	—	2
INTERNAL TRI-STATE DRIVER	—	2
2 TO 1 MULTIPLEXER	—	1
SET-RESET LATCH	1/4 LS279	2
CLOCKED LATCH	1/4 LS75*	2.5
CLOCKED LATCH WITH SET	—	3
D FLIP-FLOP WITH RESET	1/4 LS175**	5
D FLIP-FLOP WITH SET	—	5
D FLIP-FLOP SET AND RESET	—	6
TTL LEVEL TRANSLATOR	—	2

* Both polarities of the enable signal are required for CMOS CLK

** CLK and CLK are required for CMOS. The 74LS175 is reset on a positive going transition of the control signal whereas the CMOS implementation resets on a negative going transition of the same signal.

The current AMI array family, 300 gates to 1260 gates, is run in a 3-12V CMOS process (internally coded as CVA process).

In conjunction with these arrays, AMI has developed a set of "functional overlays." These are basic logic element building blocks—e.g. two input and larger gates of various types, flip-flops, and so forth—from which complete logic designs can

D.C. characteristics for the 5 micron gate array family are summarized in Table 4.

Table 2. Gate Array MSI/LSI Functional Macros

DESCRIPTION	TTL FUNCTIONAL EQUIVALENCE	GATE COUNT
3 TO 8 DECODER	LS138	23
4 TO 16 DECODER	LS154	56
8 TO 1 MULTIPLEXER	LS151	28
4-BIT FULL ADDER	LS283	60
8-BIT FULL ADDER		120
12-BIT FULL ADDER		180
16-BIT FULL ADDER		240
LOOK-AHEAD CARRY GENERATOR	LS182	34
4-BIT PRESETTABLE AND EXPANDABLE BINARY COUNTER	LS163	52
4-BIT EXPANDABLE BINARY COUNTER	LS163*	39
4-BIT PRESETTABLE BINARY COUNTER	LS163*	47
4-BIT BINARY COUNTER	LS163*	34
8-BIT PRESETTABLE BINARY COUNTER		104
12-BIT PRESETTABLE BINARY COUNTER		156
16-BIT PRESETTABLE BINARY COUNTER		208
4-BIT EXPANDABLE & PRESETTABLE BINARY UP/DOWN COUNTER	LS169	62
4-BIT EXPANDABLE BINARY UP/DOWN COUNTER	LS169*	49
4-BIT PRESETTABLE BINARY UP/DOWN COUNTER	LS169*	58
4-BIT BINARY UP/DOWN COUNTER	LS169*	44
4-BIT EXPANDABLE & PRESETTABLE DECADE COUNTER	LS162	56
4-BIT EXPANDABLE DECADE COUNTER	LS162*	43
4-BIT PRESETTABLE DECADE COUNTER	LS162*	51
4-BIT DECADE COUNTER	LS162*	38
4-BIT EXPANDABLE & PRESETTABLE DECADE UP/DOWN COUNTER	LS168	66
4-BIT EXPANDABLE DECADE UP/DOWN COUNTER	LS168*	53
4-BIT PRESETTABLE DECADE UP/DOWN COUNTER	LS168*	62
4-BIT DECADE UP/DOWN COUNTER	LS168*	48
4-BIT BIDIRECTIONAL SHIFT REGISTER	LS194	62
4-BIT PARALLEL-ACCESS SHIFT REGISTER	LS195	42
8-BIT PARALLEL LOAD SHIFT REGISTER	LS165	88
8-BIT SHIFT/STORAGE SHIFT REGISTER	LS299	137
8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER	LS164	49
8-BIT PARALLEL IN/SERIAL-OUT SHIFT REGISTER	LS166	78
8-BIT SYNCHRONOUS-LOAD SHIFT REGISTER	LS166	78
8-BIT SERIAL-IN/SERIAL-OUT SHIFT REGISTER	LS 91	48

* Simplified version of the TTL function

be developed. Each functional overlay corresponds to a metal interconnect pattern that is superimposed on a set of uncommitted transistors (and polysilicon underpasses) in the array to implement the logic element. Typical functional overlay logic elements and the number of equivalent two-input gates are shown in Table 2.

Currently over 75 functional cells exist for this family.

Three-Micron Gate Array Family

As part of AMI's long range semi-custom strategy in MOS/VLSI, AMI will continue to introduce new gate array products. These new products will offer performance and cost advantages not currently realizable. In conjunction with these new array products, AMI has introduced computer-aided design tools to automate the entire gate array design process.

Table 3. AMI Gate Array Configurations

3μ Double Metal Family

Part No.	Eq. 2-Input Gates	Total Pads	General I/O	Power Only
GA-1000D	1152	68	64	4
GA-2000D	2070	88	84	4
GA-3000D	3080	106	102	4
GA-4000D	4012	124	120	4

3μ Single Metal Family

Part No.	Eq. 2-Input Gates	Total Pads	General I/O
GA-500	540	40	40
GA-1000	1040	54	52
GA-1500	1500	64	64
GA-2000	2025	74	74
GA-2500	2500	84	84

5μ Single Metal Family

Part No.	Eq. 2-Input Gates	Total Pads	Low Power I/O	High Power I/O	Input Only
UA-1	300	40	17	20	3
UA-2	400	46	23	20	3
UA-3	540	52	25	24	3
UA-4	770	62	31	28	3
UA-5	1000	70	35	32	3
UA-6	1260	78	39	36	3

The newest gate array family is the high-performance GA and GA-D series which is based on AMI's 3-micron CMOS silicon gate process technology.

The AMI GA and GA-D series are designed for 5V operation over military temperature range (−55 to 125°C). Besides high speed (2 to 3ns typical delay) and high density (up to 4K gates), it features total I/O flexibility

Total Flexibility of I/O Options

Peripheral cell design offers total flexibility in determining pin-out configurations and maximizes the number of options associated with each pad. Each pin in the 3-micron gate array can serve any of the following functions:

- TTL Output Driver
- LSTTL Output Driver
- CMOS Output Driver
- Open Drain Output
- Tristate Output
- Analog Switch
- CMOS Input
- V_{DD} Supply
- V_{SS} Supply

Furthermore, the peripheral cell also contains high impedance transistors that can be used as pull-ups or pull-downs if required.

The single metal version provides up to 2500 gates and the double metal GA-D version 4000 gates. See Table 3 for configurations.

In conjunction with these new array products, AMI offers a complete powerful set of design automation software to allow users complete design flexibility. Using a terminal tied to a central AMI owned or customer owned minicomputer or mainframe, the user has access to a complete set of design automation tools including:

- Schematic capture
- Logic simulation
- Circuit simulation
- Interactive or autoplace and route
- Automated placement and routing

AMI Service Makes It Simple

AMI is committed to providing service which makes getting your gate arrays nearly as simple as buying off-the-shelf, standard circuits. From your logic description, net list, database tape, or whatever format in which **you** choose to supply us the design information, AMI has proven procedures designed to assure that you'll get circuits on time and that they work the first time.

- You supply **logic** and **specifications** and we'll complete the VLSI implementation for you.
- You supply **logic using AMI macros** and we'll complete schematic capture, logic simulation, placement and routing, and the fabrication process.
- You do your own **schematic capture** on any of several AMI approved workstations and give us a **net list** and we'll complete the process.
- You supply the **database tape** and we'll fabricate, package and test your gate array circuits.

Regardless of how or at what stage you supply your design data, you can be confident that your completed ICs are only a short time away. Why? Because AMI's entire manufacturing cycle, including planning and tracking procedures, has been developed during 17 years of experience

in delivering customized solutions for our customers. Producing small volumes of a large number of different designs is our standard way of doing business.

Our commitment to you won't get lost in the shuffle as is often the case with large producers of commodity circuits. Best yet, you get **service** and AMI's **total MOS/VLSI capability.**

You Get State-of-the-Art CMOS Technology

The advanced CMOS process technology used for AMI gate array products offers all of the conventional advantages of CMOS—very low power consumption, broad power supply voltage range, high noise immunity—as well as dense circuits with high performance. Arrays are currently available in 5-micron single metal, 3-micron single and double metal, and in 1984, 2-micron double metal processes.

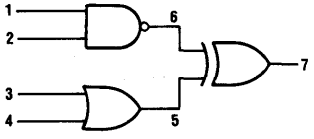
You Get Leading Edge Design Support

AMI's CAD Technology is the most advanced integrated software system for MOS/VLSI circuit design available in the industry. It uses a common database for logic simulation, mask layout and test program generation. The common database approach eliminates errors due to data file transcription steps and allows a gate array design to be converted into a standard cell or a full custom circuit without entering the same logic description again.

The heart of the system is **BOLT**™ (**B**lock **O**riented **L**ogic **T**ranslator) which is a hardware description language and a compiler for the language. It allows the system designer to describe the logic network in a hierarchical fashion due to an unlimited macro nesting capability.

The logic description database is created by compiling a BOLT description of the logic network into the HOLD™ (see below) database format. Figure 4 shows a simple logic network and the corresponding BOLT syntax.

Figure 4. Logic Network & BOLT Syntax




```
6 • NAND  1  2;
5 • OR    3  4;
7 • EXOR  5  6;
```

HOLD™ (**H**ierarchically **O**rganized **L**ogic **D**atabase) is created by the BOLT compiler using the AMI macro library and the BOLT description of the circuit. HOLD contains the description of the circuit for AMI CAD programs and is updated after mask layout to include key performance information, e.g. net capacitance after routing.

SIMAD™ is an event and table driven, MOS logic simulator that creates a logic model of the circuit to be validated from the HOLD database. Nodes may assume any one of six logic states 0, 1, X, L, H, and Z, thus allowing accurate simulation of transmission gates.

Since each logic device in the model can be assigned propagation delays, SIMAD also allows timing verification, including race detection.

GAPAR™ is the software package that does automatic placement and routing of arrays. GAPAR will complete at least 98% of the wiring connections on a 100% utilized array. The GAPAR system's correct-by-construction interactive editor can be used to manually connect any unrouted connections or to manually route critical delay paths.

DELAY™ updates the HOLD database after routing with propagation delay parameters based on actual capacitance data.

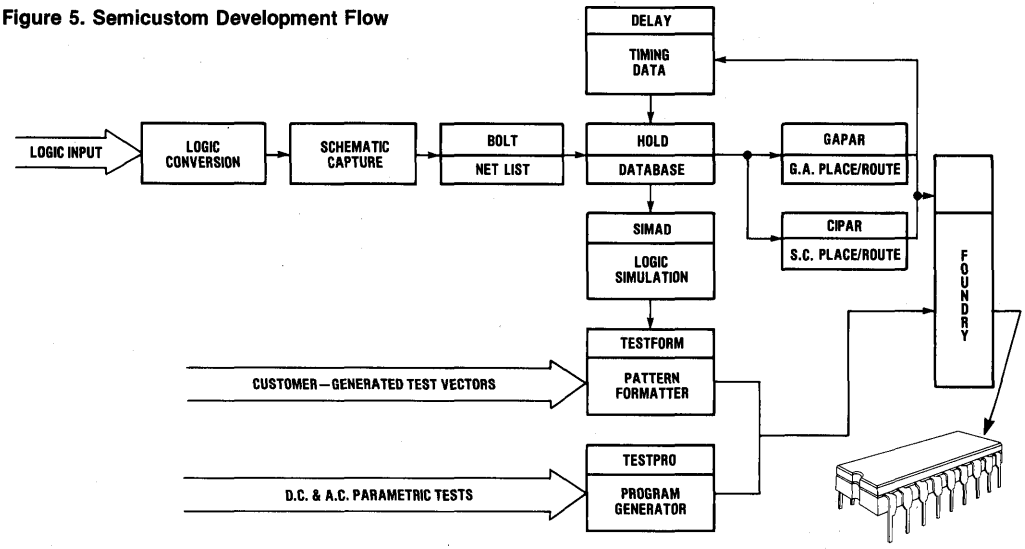
TESTFORM™ generates compressed functional test patterns from the SIMAD logic simulation results.

TESTPRO™ allows off-line generation of D.C. parametric tests in the Factor™ test language used in Fairchild test systems. Its output is merged with the compressed functional patterns from TESTFORM, and the result is a test program that can be tailored for use in any Sentry™ tester.

AMI's software makes it reasonably simple to convert a gate array to a standard cell or full custom circuit, resulting in lower circuit costs when your volume warrants it. Plus you get even more.

- We offer design training classes with full-time instructors.
- AMI has design centers to allow you to do your design with our engineers available to assist you.
- AMI's software is available on a variety of computer systems and workstations.
- Through volume purchase agreements we can help you get discounts on the hardware/software configuration that best fits your needs.

Figure 5. Semicustom Development Flow



Packages

Pinout or lead count varies with die size and array complexity. The arrays are offered in standard plastic and ceramic dual-in-line packages with pin counts ranging from 16 to 64, JEDEC-Standard leadless and leaded chip carriers, miniflat packs to 84 pins, and pin grid arrays to 144 pins. AMI gate array products are also available in wafer or unpackaged die form.

Table 4. D.C. Electrical Characteristics, 5-Micron Gate Arrays
Specified @ $V_{DD} = 5V \pm 10\%$ or $10V \pm 10\%$, $V_{SS} = 0V$, $T_A = -55°$ to $+125°C$

Symbol	Parameter	V_{DD}	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Low Level Output Voltage				0.05	V	$I_{OL} = 1.0\mu A$
	High Power Output	5			0.4	V	$I_{OL} = 2.4mA$
	High Power Output	10			0.5	V	$I_{OL} = 4.8mA$
	Low Power Output	5			0.4	V	$I_{OL} = 0.8mA$
	Low Power Output	10			0.5	V	$I_{OL} = 1.6mA$
V_{OH}	High Level Output Voltage		$V_{DD} - .05$			V	$I_{OH} = -1.0\mu A$
	High Power Output	5	2.4			V	$I_{OH} = -1.6mA$
	High Power Output	10	9.5			V	$I_{OH} = -1.0mA$
	Low Power Output	5	2.4			V	$I_{OH} = -0.8mA$
	Low Power Output	10	9.5			V	$I_{OH} = -0.4mA$
V_{IL}	Input Low Voltage	5	0.0		0.8	V	TTL Input
		5	0.0		1.5	V	CMOS Input
		10	0.0		3.0	V	CMOS Input
V_{IH}	Input High Voltage	5	2.0		V_{DD}	V	TTL Input
		5	3.5		V_{DD}	V	CMOS Input
		10	7.0		V_{DD}	V	CMOS Input
I_{IN}	Input Leakage Current	5	−1		1	μA	$V_{IN} = V_{DD}$ or V_{SS}
I_{OZ}	High Impedance Output Leakage Current	5	−10	0.001	10	μA	$V_{OH} = V_{DD}$ or V_{SS}
C_{IN}	Input Capacitance			5		pF	Any Input

AMI®

A Subsidiary
of Gould Inc.

Standard Cells

AMI's Standard Cell Capabilities

What are Standard Cells?

Standard cells are circuit "building blocks" which have been previously designed, characterized and stored in a computer database. These building block cells can range from simple digital circuit elements such as logic gates (AND, NAND, NOR, OR, etc.) to more complex digital subsystems such as UARTs, CPU cells, memory cells, etc. The cells can also include basic analog circuit elements (operational amplifiers, comparators, etc.), as well as complicated analog subsystems (analog-to-digital converters, switched capacitor filters, etc.). Both the digital and analog cells are available, in a standard cell library, to be integrated into various application specific circuits.

Two basic types of circuits can be constructed from a standard cell library. The first type, Semicustom Standard Cell Circuits, utilizes only those cells which exist in the standard cell library. The semicustom designer selects the necessary cells from the library and, the circuit design is completed by automatically "placing" the cells and "routing" the interconnections between cells.

The second type of standard cell circuit, Interactive Custom Standard Cell Circuits, is distinguished by either of two characteristics: 1) interactive placement and routing or 2) integration of custom circuitry. Interactive layout is used to minimize the die size and/or to optimize overall circuit performance. With this technique, an experienced circuit designer uses an interactive CAD (Computer Aided Design) system to "manually" place the cells and route the necessary interconnections. If specialized functions cannot be efficiently implemented with the available cells or if rigorous performance criteria must be met, custom circuitry can be used in conjunction with the standard cells, to meet the requirements of a given circuit. This sort of custom standard cell circuit can be placed and routed interactively or, if the custom circuit elements can be grouped into one or more custom cells, automatic layout can be performed.

Standard Cells Benefits

Standard Cell Benefits Standard cell circuits offer a simple, low-cost, low-risk method of designing a semicustom or custom circuit for a specific application.

Compared to optimized full custom circuits, standard cell circuits offer substantial savings in both development cost and time span. Also, because the cells have been individually simulated and characterized, it is more likely that a standard cell circuit will work properly the first time. In exchange for these benefits, the production unit prices of a standard cell circuit are slightly higher than the prices of a comparable optimized custom circuit.

At the other end of the custom spectrum, standard cell circuits compare favorably with gate arrays. Although the development cost and time span are not as low as those of a gate array, standard cell circuits can offer significant advantages in unit pricing, functional capabilities, and circuit performance.

By combining the advantages of optimized full custom circuits and gate arrays, standard cell circuits provide a cost effective custom solution for medium production volumes of ten to fifty thousand units per year. In addition to their relative advantages, standard cell circuits offer all of the expected benefits of any custom or semicustom design—low cost, high reliability, reduced space and power requirements, superior performance and proprietary protection.

Standard Cells at AMI

AMI's standard cells are presently designed for use with a state-of-the-art 3-micron, silicon-gate CMOS process. Although the drawn geometries in this process are 3 microns, the effective channel lengths are typically less than 2 microns. AMI will introduce their fourth generation standard cell families, in 2-micron CMOS, during the second half of 1984.

There are two broad categories of standard cells, in AMI's present 3-micron cell families. The first category, Standard Cells, are characterized by their fixed cell heights and variable cell widths. These Standard Cells have been designed with horizontal power and ground busses running through each cell, in order to eliminate the need for separate power supply connections to each cell. Also, the need for inefficient route-through cells is minimized, by providing all signal inputs and outputs at both the top and bottom edges of each cell.

The second category of standard cells, Macro Cells, are recognized by their high degree of cell complexity, variable cell heights and variable cell widths. Macro Cells are circuit subsystems which have been designed as relatively large, internally customized cells. Possible Macro Cells include CPU, UART, memory, A/D converter and display driver cells.

AMI Standard Cell Design

From a design point of view, both Standard Cells and Macro Cells are treated in the same manner. Each cell is initially designed on a color graphics terminal, with the help of AMI's SIDS™ (Symbolic Interative Design System). SIDS is a custom circuit CAD system developed by AMI and proven in the design of over 100 Optimized Full Custom and Interactive Custom Standard Cell circuits. Once the cell's SIDS layout has been completed and satisfactory electrical performance has been verified (using ASPEC and AMI's proprietary circuit models), the cell can be stored in a standard cell library database.

A standard cell chip is designed by selecting cells from the standard cell library and then using CAD tools, such as CIPAR™ (Circuit Interactive Place And Route), to arrange the desired cells and perform the necessary interconnections. If the circuit requires any unique cells or custom circuitry, the SIDS-based design approach facilitates the integration of the special circuitry with the standard cells. With 18 years of experience in the design of over 3000 circuits, AMI is uniquely qualified to offer the best solution to

your Semicustom and Interactive Custom Standard Cell Circuit needs.

Standard Cell Families

AMI's present generation of standard cells contains three different 3-micron CMOS cell families. Two of these families are best suited for high-performance, high-density digital circuits, with limited analog functions. The third family is capable of higher operating voltages and, it offers extensive analog, digital and high-voltage capabilities. For a summary of AMI's standard cell families, please refer to Table 3, at the end of this section.

Single-Metal Standard Cells

The single-metal cell family is used for primarily digital circuits, with an operating voltage range of 2.5 volts to 6.0 volts. At the cell level, the single-metal cells can operate at speeds of up to 35 MHz. However, the resistivity of the polysilicon interconnect limits the overall circuit performance to around 20 MHz.

Double-Metal Standard Cells

The double-metal cell family also operates at 2.5V to 6.0V and, its functional capabilities are similar to those of the single-metal cell family. The double-metal cell level performance is also 35 MHz but, significantly higher performance can be achieved at the circuit level. Because a second layer of metal is available for cell interconnection, circuit density can be improved and, the entire circuit can operate at 35 MHz.

High-Voltage/Analog Standard Cells

This single-metal cell family offers extensive analog design capability (as well as digital) and can operate at voltages up to 10 volts. In addition, a patented design technique allows the construction of 30-volt output buffers. This 30-volt output capability is used in AMI's CSDD™ (Custom Smart Display Driver) Macro Cells.

Standard Cell Development Flexibility

AMI offers four basic options for developing a standard cell circuit. These options are summarized in Table 1.

Table 1.

	AMI DESIGNED DEVELOPMENT	SHARED DEVELOPMENT	WORKSTATION DEVELOPMENT	CUSTOMER DESIGNED DEVELOPMENT
FUNCTIONAL SPECIFICATION	C	C	C	C
LOGIC SCHEMATIC	C	C	C	C
ELECTRICAL SPECIFICATION	C	C	C	C
BREADBOARD (IF BUILT)	C	C	C	C
MOS LOGIC SCHEMATIC (LOGIC USING CELL ELEMENTS)	O	C	C	C
LOGIC SIMULATION	A	C	C	C
TEST VECTOR GENERATION	A	O	O	C
CIRCUIT DESIGN	A	O	O	C
TEST PROGRAM DEVELOPMENT/DEBUG	A	O	O	O
LAYOUT PLAN (CELL LOCATION)	A	O	O	O
LAYOUT (INTERCONNECTION)	A	A	A	O
PATTERN GENERATOR TAPE (COMPUTER TAPE OF LAYOUT)	A	A	A	O
PHOTO MASKS	A	A	A	A
WAFER FABRICATION	A	A	A	A
ASSEMBLY	A	A	A	A

A = AMI
TASK C = CUSTOMER TASK
O = OPTIONAL - CUSTOMER OR AMI TASK

AMI Designed Development

For an AMI designed development, the customer provides a functional description, logic schematic and complete electrical specification. AMI will use this input to perform all of the other design activities, including standard cell/MOS logic design, development of any special cells, logic simulation, critical path analysis, layout, mask generation, wafer fabrication, assembly and test development. This development option allows the customer to draw upon AMI's vast MOS circuit design experience, when the customer does not wish to be an active participant in the entire design process.

Shared Development

In a shared development, certain intermediate tasks can either be done by AMI or by the customer. These tasks include logic simulation, critical path analysis, layout planning, test vector generation and test program generation. The customer can decide whether to do one of these tasks, several tasks or all of them.

To assist in a shared development, AMI can provide the customer with a **Standard Cell Design Manual.** The **Design Manual** is a complete technical reference for AMI Standard Cell Design. It contains general information on designing with AMI's standard cells, including how to estimate the circuit's AC performance, power consumption and die size. The **Design Manual** also includes a complete set of detailed data sheets for each of the individual cells. In order to keep the **Design Manual** current, an update subscription is available.

Workstation Development

AMI's standard cells are supported on several commercially available engineering workstations, including DAISY and MENTOR. AMI will provide a standard cell library database for use with the workstation. The customer can use the workstation to perform schematic capture, netlist generation and logic simulation. AMI will accept a netlist and will complete the development from that point.

Customer Designed Development

For customers who wish to perform the entire circuit design, AMI will license the use of all cell families. The standard cell tooling database may be used in conjunction with the customer's own CAD tools or, the customer may license the necessary circuit design tools directly from AMI.

In a customer designed development, the customer is responsible for the entire circuit design, up to the creation of a pattern generator tape. The PG tape will be used to make the wafer processing masks. This type of development allows interested customers to use their own MOS design capabilities, without having to build a mask making or wafer fabrication facility.

Development Schedule

One of the primary objectives of standard cell circuits is to design a high-performance MOS/VLSI chip in the shortest time span possible.

With standard cells, circuit design can be almost eliminated because the functional and performance characteristics of the individual cells have already been determined. Most of the remaining circuit design is devoted to verifying that the overall circuit's timing and power requirements have been met.

When standard cells are used, layout can be done automatically, with a CAD place and route program such as CIPAR. Because most of the layout only involves the interconnection of previously designed cells, the possibility of error is greatly reduced. All of these factors combine to decrease the development span and increase the likelihood that the first silicon will work properly.

Development Cost

Most AMI standard cell developments cost between $20,000 and $75,000. Several factors affect this development cost, including die size, circuit complexity, speed requirements, development task responsibilities and test development responsibilities.

The most obvious factor affecting the development cost is the die size and number of cells required to implement the desired circuit functions. The "2-input gate equivalence" given in Table 3 can be used as a shortcut method to determine the die size, without performing a detailed analysis of the circuit. With a larger die size, development costs will rise.

Similarly, development costs are increased if special layout is required to meet critical timing requirements, if new cells are required, or if the circuit contains very little repetitive logic.

Because of the flexibility of AMI's design interface, development costs can vary widely, depending on how many of the development tasks are performed by the customer. For instance, a development that starts with a functional circuit description will be more expensive than a development from a customer's netlist.

One of the most important development tasks is the test development. Not only does the quality of the production parts depend upon a thorough test program, the test development also accounts for fifteen to forty percent of the total development cost. If a customer is able to provide detailed testing information, the test development cost can be substantially reduced.

Table 2 provides a summary of the high- and low-cost development options for several different circuit sizes. The first column is based upon an AMI designed development, where the customer has provided a functional description, logic schematic and complete electrical specification. The second column assumes a shared (or workstation) development with a netlist input, completed logic simulation, and customer-supplied test program. In this example, AMI is responsible for the basic development tasks of automatic layout, mask-making, wafer fabrication, assembly and test program review.

Table 2. AMI Standard Cell Development Cost

3-Micron, Single-Metal CMOS Standard Cells

Number of 2-Input Equivalent Gates	Netlist Input (Automatic Layout)		Logic Diagram Input (Interactive Layout)	
	Relative Cost	Typical Span	Relative Cost	Typical Span
200	1.00	9 weeks	1.80	13 weeks
1000	1.25	10 weeks	2.50	17 weeks
1500	1.35	10 weeks	2.95	19 weeks
2000	1.50	11 weeks	3.35	21 weeks
2500	1.60	11 weeks	3.75	23 weeks

Table 3. Single-Metal CMOS Standard Cell Summary

Cell Name	Description	2-Input Gate Equivalent	CMOS 4000 Functional Equivalent	TTL 74LS00 Functional Equivalent
AA025	2-Input AND	1.5	1/4 4081	1/4 74LS08
AA027	2-Input AND	1.5	1/4 4081	1/4 74LS08
AA035	3-Input AND	2.0	1/3 4073	1/3 74LS11
AA045	4-Input AND	2.5	1/2 4082	1/2 74LS21
AO015	1x2-Input AND into 2-Input OR	2.5		
AO025	2x2-Input AND into 2-Input OR	3.0	1/4 4019	
AO035	3x2-Input AND into 3-Input OR	4.5		
AO045	2x3-Input AND into 2-Input OR	4.0		
AO055	1x3-Input AND + 1x2-Input AND into 2-input OR	3.5		
AO065	1x3-Input AND + 1x2-Input AND into 3-input OR	4.5		
AO075	1x2-Input AND into 3-input OR	3.5		
AO085	1x3-Input AND into 2-Input OR	3.0		
AO095	1x3-Input AND into 3-Input OR	4.0		
DF0F5	D-Type Flip-Flop, without Set or Reset	6.0		
DF105	D-Type Flip-Flop, with Set	7.0		
DF115	D-Type Flip-Flop, with Reset	7.0		1/4 74LS175
DF125	D-Type Flip-Flop, with Set and Reset	8.0	1/2 4013[1]	1/2 74LS74
DF127	D-Type Flip-Flop, with Set and Reset	8.0	1/2 4013[1]	1/2 74LS74
DF205	D-Type Flip-Flop, only Q Out	5.5		
DF207	D-Type Flip-Flop, only Q Out	5.5		
DF3F5	D-Type Flip-Flop, with Synchronous Load	8.5		
DL115	Data Latch, with Reset	4.5		
DL117	Data Latch, with Reset	4.5		
DL245	Data Latch, with only Q Out, GT/GTN	2.5		
EN015	Exclusive NOR	2.5	1/4 4077	1/4 74LS266
EO015	Exclusive OR	2.5	1/4 4070	1/4 74LS86
IB01C5	Input Pad, CMOS, Core Limited	1.0		
IB01P5	Input Pad, CMOS, Pad Limited	1.0		
IB09C5	Input Pad, TTL, Core Limited	1.25		
IB09P5	Input Pad, TTL, Pad Limited	1.25		
IN015	Inverter	0.5	1/6 4069	1/6 74LS04
IN017	Inverter	0.5	1/6 4069	1/6 74LS04
IO03C5	I/O Pad, CMOS, Core Limited	4.5		
IO03P5	I/O Pad, CMOS, Pad Limited	4.5		
IT015	Internal Tri-State Buffer, Non-Inverting	2.0		
IT017	Internal Tri-State Buffer, Non-Inverting	2.75		
IT025	Internal Tri-State Buffer, Inverting	1.5		
IT027	Internal Tri-State Buffer, Inverting	3.25		
MC015	Static Power-On-Reset	2.5		
MU215	2:1 Digital Multiplexer	3.0	1/4 40257	1/4 74LS157
NA025	2-Input NAND	1.0	1/4 4011	1/4 74LS00
NA027	2-Input NAND	1.0	1/4 4011	1/4 74LS00
NA035	3-Input NAND	1.5	1/3 4023	1/3 74LS10
NA037	3-Input NAND	1.5	1/3 4023	1/3 74LS10
NA045	4-Input NAND	2.0	1/2 4012	1/2 74LS20
NA055	5-Input NAND	2.5		

Table 3. Single-Metal CMOS Standard Cell Summary (Continued)

Cell Name	Description	2-Input Gate Equivalent	CMOS 4000 Functional Equivalent	TTL 74LS00 Functional Equivalent
NO025	2-Input NOR	1.0	1/4 4001	1/4 74LS02
NO027	2-Input NOR	1.0	1/4 4001	1/4 74LS02
NO035	3-Input NOR	1.5	1/3 4025	1/3 74LS27
NO045	4-Input NOR	2.0	1/2 4002	
OB03C5	Output Pad, TTL/CMOS, Core Limited	1.0		
OB03P5	Output Pad, TTL/CMOS, Pad Limited	1.0		
OB09C5	Output Pad, TS, Core Limited	3.5		
OB09P5	Output Pad, TS, Pad Limited	3.5		
OR025	2-Input OR	1.5	1/4 4071	1/4 74LS32
OR027	2-Input OR	1.5	1/4 4071	1/4 74LS32
OR035	3-Input OR	2.0	1/3 4075	
OR045	4-Input OR	2.5	1/2 4072	
PP01C	V_{SS} Power Pad, Core Limited	n/a		
PP01P	V_{SS} Power Pad, Pad Limited	n/a		
PP02C	V_{DD} Power Pad, Core Limited	n/a		
PP02P	V_{DD} Power Pad, Pad Limited	n/a		
RA015	RAM 0 Configuration 1 (16 x 8)	568.5		
RA0A5	RAM Core Cell	60.0		
RA0B5	RAM Write Address Decode	52.5		
RA0C5	RAM Read Address Decode	36.0		
SC105	Synchronous Counter, with Ripple Carry and Set	10.5		
SC115	Synchronous Counter, with Ripple Carry and Reset	10.5		
SC125	Synchronous Counter, with Ripple Carry and Reset	11.5		
SC925	Up/Down Counter with Ripple Carry and Set	17.5		
TF105	Toggle Flip-Flop, with Set	7.0		
TF115	Toggle Flip-Flop, with Reset	7.0		
TF125	Toggle Flip-Flop, with Set/Reset	8.0		
ZZ01	Vertical Route Through	n/a		
ZZ02	Right P-Well End Cell	n/a		
ZZ03	Left P-Well End Cell	n/a		

[1]DF125: Reset and Set are asserted Low
4013: Reset and Set are asserted High

Table 3. 3μ Double-Metal CMOS Standard Cell Summary

Cell Name	Description	2-Input Gate Equivalent	CMOS 4000 Functional Equivalent	TTL 74LS00 Functional Equivalent
AA025	2-Input AND	1.5	1/4 4081	1/4 74LS08
AA027	2-Input AND	1.5	1/4 4081	1/4 74LS08
AA035	3-Input AND	2.0	1/3 4073	1/3 74LS11
AA045	4-Input AND	2.5	1/2 4082	1/2 74LS21
A0015	1x2-Input AND into 2-Input OR	2.5		
A0025	2x2-Input AND into 2-Input OR	3.0	1/4 4019	
A0035	3x2-Input AND into 3-Input OR	4.5		
A0045	2x3-Input AND into 2-Input OR	4.0		
A0055	1x3-Input AND + 1x2-Input AND into 2-Input OR	3.5		
A0065	1x3-Input AND + 1x2-Input AND into 3-Input OR	4.5		
A0075	1x2-Input AND into 3-Input OR	3.5		
A0085	1x3-Input AND into 2-Input OR	3.0		
A0095	1x3-Input AND into 3-Input OR	4.0		
DF0F5	D-Type Flip-Flop, without Set or Reset	6.0		
DF105	D-Type Flip-Flop, with Set	7.0		
DF115	D-Type Flip-Flop, with Reset	7.0		1/4 74LS175
DF125	D-Type Flip-Flop, with Set and Reset	8.0	1/2 4013[1]	1/2 74LS74
DF127	D-Type Flip-Flop, with Set and Reset	8.0	1/2 4013[1]	1/2 74LS74
DF205	D-Type Flip-Flop, only Q Out	5.5		
DF207	D-Type Flip-Flop, only Q Out	5.5		
DL115	Data Latch, with Reset	4.5		
DL117	Data Latch, with Reset	4.5		
DL245	Data Latch, with only Q Out, GT/GTN	2.5		
EN015	Exclusive NOR	2.5	1/4 4077	1/4 74LS266
E0015	Exclusive OR	2.5	1/4 4070	1/4 74LS86
IB01C5	Input Pad, CMOS, Core Limited	1.0		
IB01P5	Input Pad, CMOS, Pad Limited	1.0		
IB09C5	Input Pad, TTL, Core Limited	1.25		
IB09P5	Input Pad, TTL, Pad Limited	1.25		
IN015	Inverter	0.5	1/6 4069	1/6 74LS04
IN017	Inverter	0.5	1/6 4069	1/6 74LS04
IO03C5	I/O Pad, CMOS, Core Limited	4.5		
IO03P5	I/O Pad, CMOS, Pad Limited	4.5		
IT015	Internal Tri-State Buffer, Non-Inverting	2.0		
IT017	Internal Tri-State Buffer Non-Inverting	2.75		
IT025	Internal Tri-State Buffer, Inverting	1.5		
IT027	Internal Tri-State Buffer, Inverting	3.25		
MC015	Static Power-On-Reset	2.5		
MU215	2:1 Digital Multiplexer	3.0	1/4 40257	1/4 74LS157
NA025	2-Input NAND	1.0	1/4 4011	1/4 74LS00
NA027	2-Input NAND	1.0	1/4 4011	1/4 74LS00
NA035	3-Input NAND	1.5	1/3 4023	1/3 74LS10
NA037	3-Input NAND	1.5	1/3 4023	1/3 74LS10
NA045	4-Input NAND	2.0	1/2 4012	1/2 74LS20
NA055	5-Input NAND	2.5		

Table 3. 3μ Double-Metal CMOS Standard Cell Summary (Continued)

Cell Name	Description	2-Input Gate Equivalent	CMOS 4000 Functional Equivalent	TTL 74LS00 Functional Equivalent
NO025	2-Input NOR	1.0	1/4 4001	1/4 74LS02
NO027	2-Input NOR	1.0	1/4 4001	1/4 74LS02
NO035	3-Input NOR	1.5	1/3 4025	1/3 74LS27
NO045	4-Input NOR	2.0	1/2 4002	
OB03C5	Output Pad, TTL/CMOS, Core Limited	1.0		
OB03P5	Output Pad, TTL/CMOS, Pad Limited	1.0		
OB09C5	Output Pad, TS, Core Limited	3.5		
OB09P5	Output Pad, TS, Pad Limited	3.5		
OR025	2-Input OR	1.5	1/4 4071	1/4 74LS32
OR027	2-Input OR	1.5	1/4 4071	1/4 74LS32
OR035	3-Input OR	2.0	1/3 4075	
OR045	4-Input OR	2.5	1/2 4072	
PP01C	V_{SS} Power Pad, Core Limited	n/a		
PP01P	V_{SS} Power Pad, Pad Limited	n/a		
PP02C	V_{DD} Power Pad, Core Limited	n/a		
PP02P	V_{DD} Power Pad, Pad Limited	n/a		
RA015	RAM 0 Configuration 1 (16 x 8)	568.5		
RA0A5	RAM Core Cell	60.0		
RA0B5	RAM Write Address Decode	52.5		
RA0C5	RAM Read Address Decode	36.0		
SC105	Synchronous Counter, with Ripple Carry, Set	10.5		
SC115	Synchronous Counter, with Ripple Carry, Reset	10.5		
SC125	Synchronous Counter, with Ripple Carry, Reset	11.5		
SC925	Up/Down Counter, with Ripple Carry, Set, Reset	17.5		
TF105	Toggle Flip-Flop, with Set	7.0		
TF115	Toggle Flip-Flop, with Reset	7.0		
TF125	Toggle Flip-Flop, with Set, Reset	8.0		
ZZ01	Vertical Route Through	n/a		
ZZ02	Right P-Well End Cell	n/a		
ZZ03	Left P-Well End Cell	n/a		

[1]DF125: Reset and Set are asserted Low
4013: Reset and Set are asserted High

AMI®

A Subsidiary
of Gould Inc.

Spectrum of Custom Solutions

Spectrum of Custom Solutions

No other company can match AMI's track record in developing state-of-the-art custom MOS products. With more than 2000 custom devices designed and manufactured since 1966, AMI has more experience than any other integrated circuit company in building a wide variety of custom integrated circuits.

AMI not only has the experience, but the design engineering organization and the advanced production and testing facilities to produce the highest quality MOS/VLSI circuits. And because AMI also offers standard memory, microprocessor, telecommunication and consumer products and the widest variety of custom VLSI processes in the industry, we're able to be objective in helping customers determine their most cost effective approach.

The Spectrum of Solutions

The decision to use a custom circuit depends on your system design requirements — such things as complexity, features, size and power limitations. But no longer is your custom decision limited by low volume or short development time — not when you come to AMI.

AMI has a full spectrum of custom solutions to assure you get that solution which meets your system performance and time-to-market requirements at the lowest possible cost.

AMI's spectrum of solutions bridges the total span of volume, timing and interface needs of our customers. From semicustom designs, to full custom design — somewhere on the spectrum, your development time and volume requirements can be met. For customers who already have their designs, AMI can provide custom fabrication from the customer's tooling. We will teach custom design if that's what the customers need. And we can even go a step further and license the technology for a customer to set up his own fabrication capability. No other company offers such a spectrum of solutions. And no other company has more experience at helping you pick the best solution for your needs.

Semicustom Gate Arrays

Gate arrays are the best solution for circuits of moderate complexity in low-to-medium volume applications or where the shortest possible development time is required. AMI offers both gate arrays and standard cell design methods for semicustom circuit development.

AMI CMOS semicustom gate arrays are standard logic layouts of everything except the final metal interconnect pattern. Since only the final pattern needs to be developed to customize your circuits, both development time spans and development costs are dramatically reduced. Because wafers containing arrays are preprocessed and inventoried, production lead times are short.

For more details on AMI's gate arrays, refer to the "Gate Array" section of this catalog.

Standard Cell Custom

Standard cells are custom circuits which are designed from computer stored modular cells. The computer assembles the cells into a collection of functional blocks to form a custom circuit. Since standard cells utilize predesigned cells, development time is reduced dramatically and development costs are cut 30 to 50 percent over conventional custom design. Circuit size is likely to be slightly larger than a conventional custom circuit, so they are most appropriate where rapid development is more important than minimal size. Standard cells are cost effective in volume levels beginning around 10,000 circuits.

For more details on AMI standard cells refer to the "Standard Cell" section of this catalog.

The Advantages of Custom Circuits

Since a single custom MOS/VLSI chip can replace expensive electromechanical devices, discrete logic components, or less efficient general purpose LSI circuits, it offers a number of benefits not available with standard logic.

Custom circuits save money. Grouping functions onto a single chip lowers production and inventory costs dramatically. That reduces your product manufacturing costs as well.

Custom circuits are more reliable. Putting a complete system on a chip trims component count, improving both product reliability and production yields. Rework, repair and replacements are minimized.

Custom circuits reduce space and power requirements. Fewer components means both space and power requirements are reduced.

Custom circuits offer superior performance. Since the circuit is designed to your requirements, features and functions can be incorporated which are not available in general purpose chips. Special tailoring reduces test requirements as well.

Custom circuits offer proprietary protection. Being tailored exactly to your requirements, a custom circuit cannot be easily duplicated. This can help put you ahead — and keep you ahead — of your competition.

Optimized Custom Design

Where end product volume is high — beyond 50,000 units per year — or where special requirements for lowest power, minimal space or highest performance exist, the solution is likely to be conventional custom design. By optimizing circuit elements and layout for a specific part, die size is substantially smaller than using semicustom design methods. In high volume applications, a smaller die size results in lower unit cost to the customer.

Spectrum of Custom Solutions

In addition, custom designs allow you to combine logic elements, memory, and analog circuits in a single device. This design flexibility is not available in gate arrays and only available to a limited extent in standard cells.

Digital and Analog Combinations

AMI is a leading innovator in combining digital and analog functions on a single chip. We can combine any of the functions below into an optimum circuit configuration to meet your needs. Unique combinations of these functions are already used in many applications in the communications, consumer, and industrial marketplace.

DIGITAL	ANALOG
PLA	OP AMP
ALU	Oscillator
Inverter	Comparator
RAM and ROM	Voltage Reference
Shift Register	A/D and D/A Converters
Interface Driver	Switched Capacitor Filters
Automatic Power Down	Programmable Power Down
	Phase Locked Loops

Instrumental in the design of custom circuits is our Symbolic Interactive Design System (SIDS). The design is done primarily with SIDS where a layout designer works with symbols directly at a large screen alphanumeric color CRT. After the SIDS circuit design has been completed and verified, the symbols are converted to polygons and a 10X reticle tape is prepared.

With SIDS, error correction, circuit modification and area relocations take only minutes. That significantly reduces design cycle time and development costs.

Computer-aided hand-drawn layouts are used to reduce extremely complex circuits to the absolute smallest size. Development time and costs are higher, but in certain cases, size or complexity requirements may require the hand-drawn approach.

Customer Owned Tooling (Silicon Foundry)

For customers who require the support of AMI's silicon foundry, we offer vast production capacity and a large engineering staff. Over the past decade, AMI has produced over 1200 circuits from customer designs—everything from standard products to gate arrays, standard cells, and full (interactive) custom circuits. When you use AMI's foundry services, you'll receive experienced support and a broad line of processes to choose from. AMI has full in-house manufacturing capability so none of our work is subcontracted. In addition, since AMI produces no systems, we won't be competing with you in your markets.

- AMI offers flexible design input options:
  - Referral to qualified AMI-subcontracted design houses
  - Customer generated workstation designs
  - Pattern generator tapes
  - Database tapes
  - Working plates
- World's broadest process capability—over 27 processes
  - PMOS
  - CMOS: 7.5μ to 3.0μ
  - NMOS: 6.0μ to 3.0μ
- Packaging Flexibility
  - Wafers
  - Dice
  - Broad range of IC packages
- Additional resources for the customer in design/development/production
- Advanced technology
- Low cost
- Short design-to-production cycle—4-5 weeks
- Best quality (currently 0.04%)
- Multiple source security for critical customer devices
- Design security with non-disclosure agreements
- Control of design/development/production

Semicustom Group

One of the most innovative approaches to AMI's IC business has been the organization of specialized departments for marketing, training, technology interfaces and applications support. Because of AMI's experience in the semicustom business, many customers depend upon AMI to provide the leadership in these areas.

The Corporate Training Department provides seven different training courses which are the best in our industry. Training courses which cover Gate Array and Standard Cell Design, CAD Software, Workstation Interface Training, and the usage of AMI Family Cells are offered on a monthly basis. As a result of this training, customer learning and personal productivity is enhanced which produces excellent results in first time circuit successes.

TIS Marketing is responsible for the licensing of AMI's CAD Technology. The CAD System is composed of 56 different software programs which cover the applications of Schematic Entry, Logic Simulation and layout of Standard Cells, Gate Arrays and Full Custom Circuits. AMI's CAD System is the only portable integrated CAD package in the world which has been developed, tested, and utilized and tested internally by a silicon foundry.

The Technology Interface Department is the consulting arm of the Semicustom Group. If you desire to build a manufacturing facility, install a new process line for manufacturing, or just ask questions, the Technology Interface Department is ready to support you.

AMI CAD Technology

AMI provides advanced computer-aided design tools for MOS/VLSI circuit design in an integrated system that supports the full continuum of design styles, from semicustom gate arrays to custom standard cells, macro cells, and handcrafted circuitry.

The complete system includes programs for design capture, design verification, mask design using automatic and interactive placement and routing techniques, symbolic mask design, and test program development.

All of AMI's design tools operate from a common database, HOLD™. This logic database is accessed by all AMI CAD tools requiring a logic description of the circuit being designed. Since the circuit description is entered into the computer only once, time is saved and the possibility of transcription errors is eliminated.

Customers using major workstations can interface with AMI's CAD system at several points during the design cycle. You can perform schematic capture on your workstation, then turn the netlist over to AMI and we'll complete the design process for you. Or you can go a step further and do the logic simulation and timing verification on your workstation and then let AMI take it from there. If your workstation has the capability you can also do the physical layout yourself and provide AMI with a database tape.

AMI will also license its software for you to use on your own computer system. AMI's CAD system can easily be configured on small computer systems to support just one user (a workstation) or on large computer systems to support an entire design department (time-sharing). All AMI CAD software has been developed in portable programming languages, primarily FORTRAN and PASCAL, thereby minimizing the difficulty of installing the software on different computer systems.

Design Capture

- **Schematic Entry (EAZEL™)**

Permits designer to create and edit circuit schematics interactively, using a monochrome or color graphics terminal. Creates a logic database (HOLD).

- **Hardware Description Language Compilation (BOLT™)**

Compiles the hardware description of a circuit into a common logic database (HOLD) file used by other AMI CAD tools.

- **HOLD to BOLT Decompilation (UNBOLT™)**

Converts a HOLD file created by EAZEL or BOLT and possibly modified during mask design, back into a hardware description language file, for inspection purposes.

- **Electrical Rules Checking (CHEER™)**

Verifies that the circuit description stored in a HOLD file does not violate any common electrical rules.

Logic Design

- **Logic Simulation (SIMAD™)**

Digitally simulates logic network behavior for both logic design verification and functional test pattern development.

- **Test Vector Language Compilation (TESS™)**

Allows designers to enter and generate tests for validating chip designs.

- **Propagation Delay Calculation (DLAY™)**

Provides accurate propagation delay parameters based on mask layout information.

Circuit Simulation/Analysis

- **Circuit Simulation (AMISPICE™)**

Determines transistor level circuit behavior in terms of node voltages, branch currents and component power dissipations.

- **Switched Capacitor Filter Analysis (SCARII™)**

Provides simulation and optimization of switched capacitor circuits.

- **Pole-Zero Analysis (PZSLIC™)**

Calculates the location of poles and zeros in the S-plane during frequency domain analysis of linear ICs.

- **Manufacturing Statistical Analysis (MSAS™)**

Analyzes parametric test data to obtain component model parameter data for use in circuit design.

Mask Design

- **Standard Cell Placement and Routing (CIPAR™)**

Automatically/interactively creates a chip floor plan, a complete standard cell circuit layout, or a macro cell chip.

- **Gate Array Placement and Routing (GAPAR™)**

Automatically creates a complete single or double metal gate array layout (some interactive editing is required).

- **Symbolic Interactive Design (SIDS™)**

Permits symbolic design and checking of custom cells and circuits, using a color alphanumerics terminal.

- **Mask Layout Editing (GLIDE™)**

Permits manual entry and editing of geometric database (GDB) files.

- **Symbolic Design Rule Checking (SDRC™)**

Performs design rule checking of symbolic mask files.

- **Symbolic Trace and Netlist Extraction (STRACE™)**

Extracts netlists from symbolic mask (SIDS) files for use in continuity checking.

- **Symbol to Polygon Conversion (STP™)**

Converts a file containing a symbolic layout to one containing an equivalent geometric layout.

- **Symbolic Printer (SPRINT™)**

Prints/plots a symbolic layout file.

- **Gate Array Design Rule Checking (GADRC™)**

Performs design rule checking of gate array mask (GDB) files.

- **Gate Array Trace and Netlist Extraction (GATRACE™)**

Extracts netlist from gate array mask (GDB) files for use in continuity checking.

- **Geometrical Mask Plotting (GPLOT™)**

Creates a Versatec plot of a geometric database (GDB) file.

- **Logic Database Netlist Extraction (HOLDNET™)**

Extracts netlists from logic (HOLD) databases for use in continuity checking.

- **Continuity Checking (COMPARE™)**

Compares the logic description to the circuit traced from the mask layout.

- **Netlist File Dump Utility (DUMPNET™)**

Produces an easy-to-read listing of the transistors and their interconnections contained in a netlist file.

- **Mask Capacitance Extraction (GCAP™)**

Produces a nodal capacitance report from geometrical mask data.

- **Polygon to Rectangle Conversion (SMASH™)**

Fractures polygon mask data into rectangles for further processing by pattern generators.

- **Pattern Generation (PATGEN™)**

Prepares PG tapes from fractured geometric mask data files.

- **Calma Stream Format Conversion (STREAMTOGDB™)**

Converts Calma stream format files to AMI geometric database (GDB) format.

- **CIF Format Conversion (CIFTOGDB™)**

Converts Caltech Intermediate Form data files to AMI geometric database (GDB) format.

- **Pattern Generator Tape Conversion (PGTOGDB™)**

Converts pattern generator tapes to AMI geometric database (GDB) format so the PG data can be examined on a graphics system.

Test Design

Test Program Generation (TESTPRO™)

Automatically generates parametric test programs.

- **Test Pattern Formatting (TESTFORM™)**

Generates a compressed functional test pattern based on stimuli/response bit patterns obtained during logic simulation.

- **TDX Format Tape Reading (READTDX™)**

Permits reading a TDX format tape on host computer.

- **TDX Format Tape Writing (WRITETDX™)**

Permits writing a TDX format tape from host computer.

User Interface

Background Mode Execution (RUN)

Allows program to be executed in background mode, thereby freeing up the user's terminal for other uses.

- **Background Mode Job Cancellation (CANCEL)**

Permits users to inspect lists of background jobs they are currently executing and individually cancel any or all of them.

- **Template Editor (TED)**

Provides forms entry capability for entry and saving of information needed to run various AMI CAD tools.

- **Online Assistance (HELP)**

Provides a listing of all AMI CAD tools with brief descriptions, and/or more complete information on a specific tool selected by the user.

State of the Art Packaging

AMI's packaging capability spans a broad spectrum, beginning with plastic, ceramic and CERDIP and going on to chip carriers, die bonding to PC boards and, most recently, mini-flat packs. As well as being a leader in plastic packaging for the high volume, low cost consumer industry, AMI's high reliability plastic packages and chip carriers are accepted under the stringent requirements in the Telecom and Automotive industries. For more detailed information see the "Packaging" section in the back of this catalog.

AMI Delivers Quality

AMI quality controls for in-process wafer inspection and final assembly and test are the best in the industry. Our care in fabrication, assembly and test mean that you get products that meet your specifications for reliability. In fact, our own in-house standards are tougher than most of our customers require. Most importantly, AMI is committed to making sure that everything we do is done right, every time we do it.

The Industry's Highest Standard

AMI has consistently pursued product excellence and has reached for higher quality levels in finished products shipped. Circuits are inspected to 0.04% AQL or your specifications, whichever is more stringent.

This 0.04% AQL can put you in a superior competitive position. Your incoming test and assembly costs come down since there is less reworking on the line. And your customers receive a more reliable product.

Quality Checks

Among the routine quality controls exercised over every product at AMI are:

- Full logic design checks against system specifications
- Circuit simulation to verify performance against objectives
- Working plates check on automatic checkers
- Automated mask fabrication checks
- In-process wafer fabrication checks
- Wafer sort tests
- 100% optical inspection at dicing
- 100% die attach checking
- 100% lead bonding inspection prior to package sealing
- Seal checks, fine and gross leak tests
- Final digital and analog tests
- Customer specified environmental tests

Meticulous in-process checks are performed on design and workmanship at every step, to ensure a full manufacturable device. In manufacture, lot process and yield data are captured and examined as a matter of routine.

For more information, see the "Product Assurance" section at the back of this catalog.

AMI

A Subsidiary of Gould Inc.

Communication Products

For more information on those data sheets which are not included in their entirety refer to AMI's Telecom Design Manual or contact Telecom Marketing at (408) 554-2070

Communication Products Selection Guide

STATION PRODUCTS

Part No.	Description	Process	Power Supplies	Packages
S2550A	Speech Network with Tone Ringer	CMOS	Line Powered	18 Pin
S2559A/B	DTMF Generator	CMOS	3.5V to 13V	16 Pin
S2559E/F	DTMF Generator	CMOS	2.5V to 10V	16 Pin
S2579	BCD Input DTMF Dialer	CMOS	3.0V to 10V	16 Pin
S2859	DTMF Generator	CMOS	3.0V to 10.0V	16 Pin
S2560A	Pulse Dialer	CMOS	1.5V to 3.5V	18 Pin
S2560G/I	Pulse Dialer	CMOS	2.0V to 3.5V	18 Pin
S2561, S2561C	Tone Ringer	CMOS	4.0V to 12.0V	18 Pin
S2561A	Tone Ringer	CMOS	4.0V to 12.0V	8 Pin
S2563A	Pulse Repertory Dialer, Line Powered	CMOS	2V to 5.5V	40 Pin
S2569/A	DTMF Generator with Redial	CMOS	2.0V to 3.5V	16 Pin
S2569B/C	DTMF Generator with Redial	CMOS	2.0V to 3.5V	18 Pin
S25089	DTMF Generator	CMOS	2.5V to 10V	16 Pin
S25610	Repertory Dialer	CMOS	1.5V to 3.5V	18 Pin
S25610E	DTMF Repertory Dialer	CMOS	2.0V to 3.5V	18 Pin
S25910/S25912	DTMF Repertory Dialer	CMOS	Line Powered	16 Pin

PCM PRODUCTS

S3506	A-Law Combo Codec with Filters	CMOS	±5V	22 Pin
S3507/A	μ-Law Combo Codec with Filters	CMOS	±5V	22/28 Pin
S44230/31/32/33/34	Hitachi Second Source Codecs with Filters	CMOS	+5V	16 Pin

SIGNAL PROCESSORS

SSPCP/M-1	Software Simulator/Assembler Program Package			
S28211	Signal Processing Peripheral (ROM Programmed)	NMOS	5V	28 Pin
S28212A/B	Signal Processing Peripheral (Externally Programmed)	NMOS	5V	64 Pin
S28214	Fast Fourier Transformer	NMOS	5V	28 Pin
S28215	Digital Filter/Utility Peripheral	NMOS	5V	28 Pin

MODEM AND FILTER PRODUCTS

S3522	Bell 212/V.22 Modem Filter	CMOS	9V to 11V	16 Pin
S35212	Bell 212/V.22 Modem Filter with I/O Filtering	CMOS	8V to 12V	24 Pin
S3524	Digital Frequency Detector	CMOS	±5V	8 Pin
S3525A/B	DTMF Bandsplit Filter	CMOS	10.0V to 13.5V	18 Pin
S3526	2600Hz Band-Pass/Notch Filter	CMOS	9V to 13.5V	14 Pin
S3526M	2600Hz Band-Pass/Notch Filter	CMOS	9.0V to 13.5V	16 Pin
S3528	Programmable Low Pass Filter	CMOS	9V to 13.5V	18 Pin
S3529	Programmable High Pass Filter	CMOS	9.0V to 13.5V	18 Pin
S3530	Single Chip Bell 103/V.21 Modem	CMOS	9.5V to 10.5V	28 Pin

Advanced Product Description **S2550A**

TWO TO FOUR WIRE TELEPHONE HYBRID WITH TONE RINGER

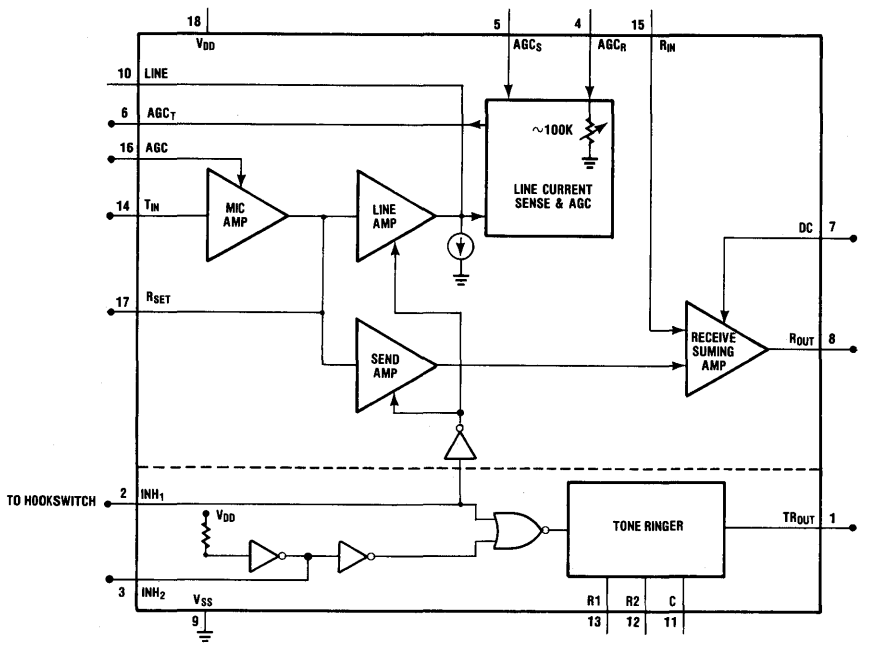
Features

- ☐ Monolithic IC Consisting of the Speech Network and Tone Ringer
- ☐ Interfaces With Inexpensive Condenser Electret Microphone, Electromagnetic Receiver and a Piezoelectric Ringer Transducer
- ☐ Automatic Gain Adjustment for Loop Loss Compensation
- ☐ Low Voltage CMOS Process for Operation Over Varying Loop Lengths and Currents
- ☐ Uses Inexpensive and Non-Critical External Components

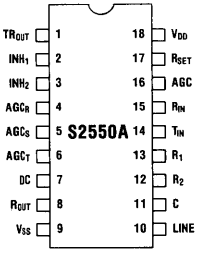
General Description

The S2550A is a monolithic CMOS IC consisting of a hybrid circuit for telephone speech functions and a tone ringer circuit. The hybrid circuit performs the 2/4 wire conversion for transmission and reception of speech in a telephone handset. The tone ringer circuit generates an audible tone coincident with the incoming ringing signal through a piezoelectric transducer or a high impedance speaker.

Functional Block Diagram



Pin Configuration



Circuit Description

The S2550A consists of the following functional blocks.

1. Transmitting transconductance amplifier with AGC. The transconductance is programmed by an external resistor to R-set.
2. Receiving transconductance amplifier with AGC. The output current level is adjusted on pin "DC".
3. Hybrid circuit. An external RC circuit must be added to compensate the phase shift for different line length and line impedance.
4. Line current sensing circuit for automatic gain control.
5. Tone ringer with output stage capable of driving a piezoelectric transducer or a high impedance speaker.

Voltage gain of the first stage of transmitting amplifier can be adjusted by the ratio of the negative feedback resistors R11, R12. Current gain and current level is programmed by R13.

The Inhibit Input 1 turns off the speech part of the circuit and activates the tone ringer if it is set to logical "1". Setting it to logical "0" activates the speech circuit and puts the tone ringer output to a high impedance state. AGC input is active when connected to pin AGC_T via capacitor. The side tone cancelling current is connected to the receiver input pin R_{IN}.

The automatic gain control of the receiver amplifier is provided by connection of input R_{IN} to AGC_R via a capacitor.

Tone ringer frequency is set by RC time constant on pins R1, R2 and C. The Inhibit Input 2 is provided to inhibit the oscillator by setting the necessary delay to avoid false ringing.

Absolute Maximum Ratings

Line Voltage V_L	15V
Line Current I_L	120mA
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +140°C

S2550A Electrical Characteristics (@ 25°C. Measured Using Circuits of Figures 1 and 2.)

Parameter	Min.	Typ.	Max.	Test Conditions
Sending Gain $G_S = 20 \log \frac{V_L}{V_T}$	 28dB 27dB	 40dB 33dB	 43dB 37dB	f = 1000Hz V_T = 10mV P-P I_L = 20mA I_L = 60mA
Sending Gain Flatness		±0.5dB		I_L = 20 to 80mA f = 300 to 3400Hz
Sending Distortion @ 20mA I_L		2.5%	5%	f = 1000Hz V_T = 10mV P-P
Receiving Gain $G_R = 20 \log \frac{V_R}{V_L}$	 −7dB −13dB	 −1dB −6dB	 +3dB −2dB	f = 1000Hz V_L = 100mV P-P I_L = 20mA I_L = 60mA
Receiving Gain Flatness		±0.5dB		I_L = 20 to 80mA f = 300 to 3400Hz
Receiving Distortion @ 20mA I_L		2%	5%	f = 1000Hz V_R = 100mV P-P
Side Tone $G_L = 20 \log \frac{V_R}{V_T}$	 18dB 12dB	 29dB 21dB	 36dB 28dB	f = 1000Hz V_T = 10mV P-P I_L = 20mA I_L = 60mA

S2550A Electrical Characteristics (continued)

Parameter	Min.	Typ.	Max.	Test Conditions
Sending Noise		20dBrnC0		I_L = 60mA V_T = 0V
V_{IL} Logic "0" Input Voltage			.3V Max.	
V_{IH} Logic "1" Input Voltage		V_{DD}		
I_L (Operating Current)	20mA	10mA Min.		Note 1
V_{DD} (Operating Voltage)	2.0V		12V	Note 2

Note 1. Although the S2550 is tested to a 20mA minimum loop current, it will normally work down to a 10mA loop current.
Note 2. This is a voltage guideline, not a tested specification. The S2550A is tested at specific loop currents, not voltages.

Table 1. S2550A Pin/Function Descriptions

Pin #	Name	Function
1	TR_{OUT}	Tone ringer output.
2	INH_1	This input selects the tone ringer or the speech network depending on the input level. A high level inhibits speech network but enables the tone ringer. A low level enables the speech network but inhibits the tone ringer.
3	INH_2	For normal operation this pin can be left open. It has an internal pull-up resistor. To avoid false ringing, a capacitor can be connected to V_{SS} from this pin to create a delay in response time to ringing signal.
4	AGC_R	A capacitor (C4) connected between this pin and R_{IN} allows loop loss compensation for receiving gain. This input looks like a variable resistor varying with loop current.
5	AGC_S	This input also looks like a variable resistor varying with loop current; can be used to modify the artificial line consisting of R7, R8, and C5.
6	AGC_T	This input is used to adjust sending gain.
7	DC	This input controls DC current through receiver by ratio of two resistors, R_9 and R_{10}.
8	R_{OUT}	Receiver output, capable of driving low impedance receivers (300Ω value suggested).
9	V_{SS}	Negative power terminal.
10	LINE	Line Input. AC input impedance seen by the phone line is primarily a function of resistor R3 and Cap C2 connected between LINE, V_{DD} and V_{SS}. This pin modulates the line current.
11	C	This pin is to connect external capacitor to form R-C oscillator for tone ringer.
12	R_2	External resistor to form R-C oscillator for tone ringer.
13	R_1	Tone ringer input to modulate ringing frequency.
14	T_{IN}	Microphone input to sending amplifier.
15	R_{IN}	Input of receiving amplifier.
16	AGC	AGC input for sending amplifier.
17	R_{SET}	Input to second stage sending amplifier. (22K for R13 gives approximately 50mA line current at 4.5V. R_{SET} is inversely proportional to line current.)
18	V_{DD}	Positive power terminal.

Figure 1. Test Set-Up Using Loop Simulator Shown in Figure 2 to Test Hybrid Functions

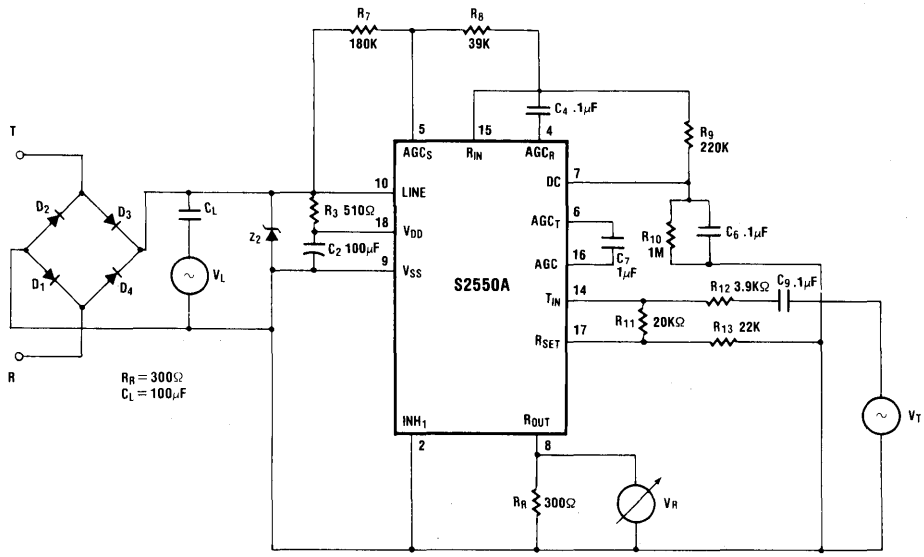


Figure 2. Loop Simulator

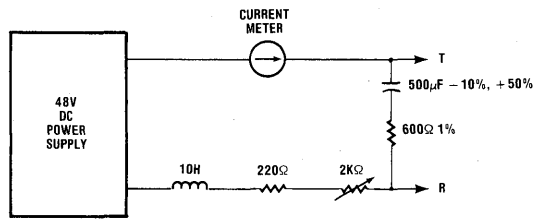
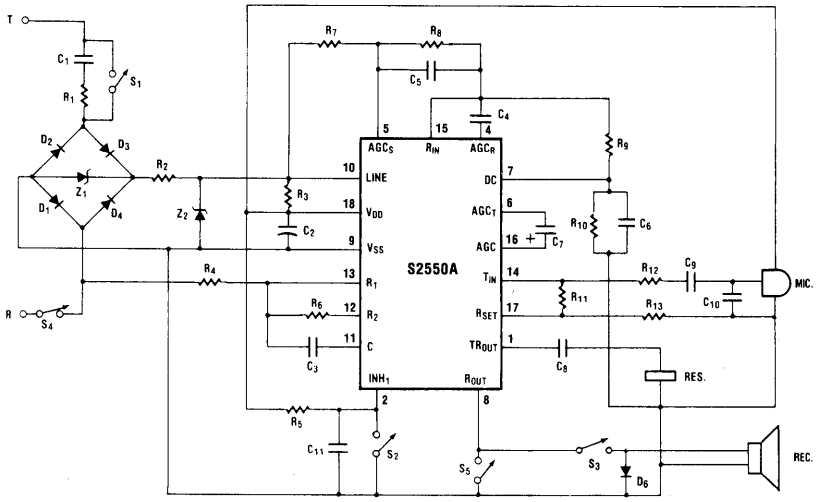


Figure 3. Typical Application Circuit for a Rotary Dial Telephone



NOTES: CIRCUIT SHOWN WITH CONTACT POSITIONS IN THE ON-HOOK STATE. S1, S2 and S3 ARE HOOKSWITCH CONTACTS. S4 AND S5 ARE ROTARY DIAL CONTACTS.

Parts List for Application Circuit of Figures 1, 3, 4, 5

R1	= 2KΩ	R23	= 5KΩ	C15	= 100μF
R2	= 20Ω	R24	= 5KΩ	C16	= 1μF
R3	= 510Ω	R25	= 1KΩ		
R4	= 5.6MΩ	R26	= 100KΩ	Q1	= 2N5401
R5	= 1MΩ	R27	= 20KΩ	Q2	= 2N5550
R6	= 500KΩ	R28	= 10KΩ	Q3	= 2N5550
R7	= 180KΩ	R29	= 7.5KΩ	Q4	= 2N5550
R8	= 39KΩ				
R9	= 220KΩ	C1	= 1μF	Z1	= 110V ZENER
R10	= 1MΩ	C2	= 100μF	Z2	= 12V ZENER
R11	= 20KΩ	C3	= .001μF	Z3	= 3.9V ZENER
R12	= 3.9KΩ	C4	= .1μF		
R13	= 22KΩ	C5	= 220pF	D1-D4	= 1N4004
R14	= 20MΩ	C6	= .1μF		
R15	= 1KΩ	C7	= 1μF	D5-D6	= 1N914
R16	= 5KΩ	C8	= 1μF		
R17	= 150KΩ	C9	= .1μF	MIC	= EM-60 (PRIMO ELECTRO DYNAMIC)
R18	= 10KΩ	C10	= .01μF		
R19	= 750KΩ	C11	= .1μF	RES	= PIEZOELECTRIC TRANSDUCER OR SPEAKER
R20	= 750KΩ	C12	= 15μF		
R21	= 750KΩ	C13	= 270pF	REC	= ELECTROMAGNETIC RECEIVER (300Ω IMPEDANCE)
R22	= 900Ω	C14	= 1μF		
				X	= 3.58 MHz Crystal

Figure 4. A Typical Application Circuit for an Electronic Telephone (Circuit Shown With Hookswitch Contact Position S1-S5 in the On-Hook State.)

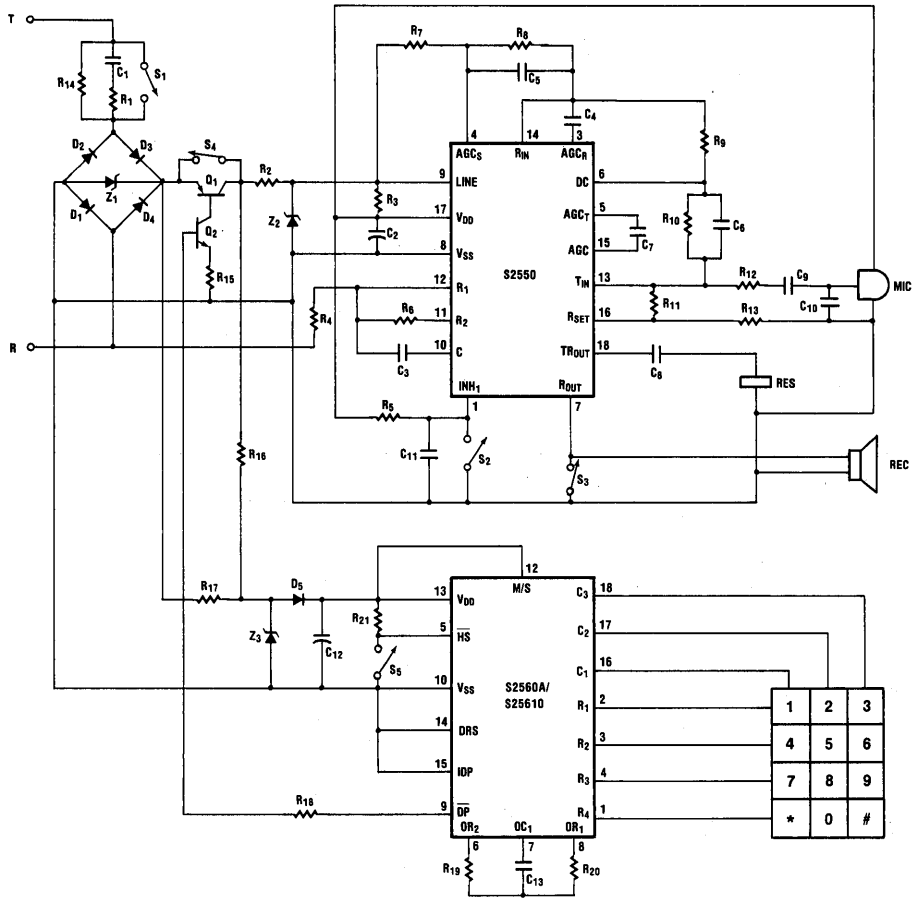
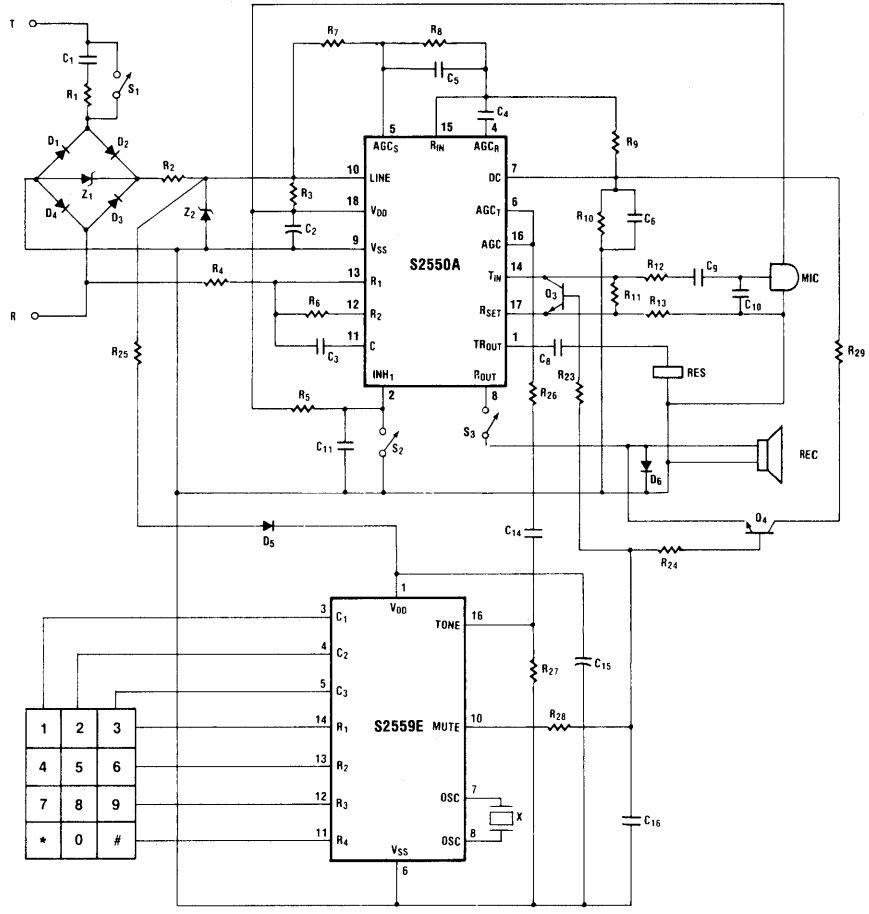


Figure 5. A Typical Application Circuit for an Electronic Telephone With DTMF (Circuit Shown With Hookswitch Contact Position S1-S3 in the On-Hook State.)



AMI®

A Subsidiary of Gould Inc.

S2559A/B/E/F

DTMF TONE GENERATOR

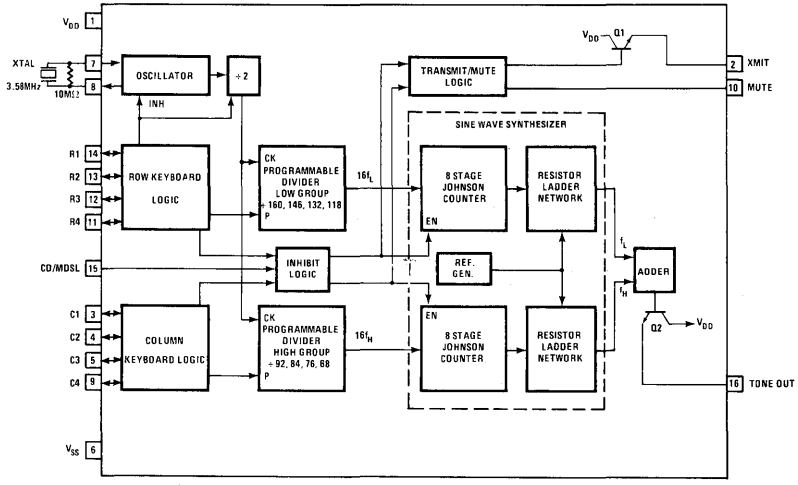
Features

- ☐ Wide Operating Supply Voltage Range: 3.5 to 13.0 Volts (A,B) 2.5 to 10 Volts (E,F)
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V
- ☐ Uses TV Crystal Standard (3.58MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability
- ☐ Mute Drivers On-Chip
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- ☐ The Total Harmonic Distortion is Below Industry Specification
- ☐ Oscillator Resistor On Chip (2559E,F)
- ☐ On-Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range
- ☐ Single Tone as Well as Double Tone Capability
- ☐ Four Options Available:
  - A:3.5 to 13.0V Mode Select
  - B:3.5 to 13.0V Chip Disable
  - E:2.5 to 10V Mode Select
  - F:2.5 to 10V Chip Disable

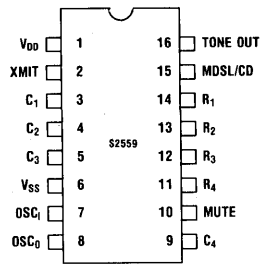
General Description

The S2559 DTMF Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton

Block Diagram



Pin Configuration



General Description (Continued)

telephone keyboard or calculator type X-Y keyboard and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinudsoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2559 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, Point-of-Sale, and Credit Card Verification Terminals and process control.

Absolute Maximum Ratings (2559A,B)

DC Supply Voltage ($V_{DD} - V_{SS}$) S2559 A, B	+ 13.5V
Operating Temperature	− 0°C to + 70°C
Storage Temperature	− 55°C to + 155°C
Power Dissipation at 25°C	500mW
Input Voltage	$-0.6 \leqslant V_{IN} \leqslant V_{DD} + 0.6$

S2559A & B Electrical Characteristics:

(Specifications apply over the operating temperature range of 0°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			3.5		13.0	V
	Non Tone Out Mode (No Key Depressed)			3.0		13.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT		3.5		0.4	40	μA
	and MUTE Outputs Unloaded)		13.0		1.5	130	μA
	Operating (One Key Selected, Tone, XMIT		3.5		0.95	2.9	mA
	and MUTE Outputs Unloaded)		13.0		11	33	mA
	Tone Output						
V_{OR}	Single Tone	Row Tone, $R_L = 390\Omega$	5.0	417	596	789	mVrms
	Mode Output	Row Tone, $R_L = 240\Omega$	12.0	378	551	725	mVrms
V_{OC}	Voltage	Column Tone, $R_L = 390\Omega$	5.0	534	781	1022	mVrms
		Column Tone, $R_L = 240_\Omega$	12.0	492	722	955	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.5 – 13.5	1.75	2.54	3.75	dB
%DIS	Distortion*		3.5 – 13.5			10	%

S2559A & B Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage	$I_{OH} = 15mA$	3.5	2.0	2.3		V
	(No Key Depressed)(Pin 2)	$I_{OH} = 50mA$	13.0	12.0	12.3		V
I_{OF}	XMIT, Output Source Leakage Current $V_{OF} = 0V$		13.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low,		3.5		0	0.4	V
	(No Key Depressed) No Load		13.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High,		3.5	3.0	3.5		V
	(One Key Depressed) No Load		13.0	13.0	13.5		V
I_{OL}	MUTE, Output Sink	$V_{OL} = 0.5V$	3.5	0.66	1.7		mA
	Current		13.0	3.0	8.0		mA
I_{OH}	MUTE, Output Source	$V_{OH} = 2.5V$	3.5	0.18	0.46		mA
	Current	$V_{OH} = 9.5V$	13.0	0.78	1.9		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current	$V_{OL} = 0.5V$	3.5	0.26	0.65		mA
	One Key Selected	$V_{OL} = 0.5V$	13.0	1.2	3.1		mA
I_{OH}	Output Source Current	$V_{OH} = 2.5V$	3.5	0.14	0.34		mA
	One Key Selected	$V_{OH} = 9.5V$	13.0	0.55	1.4		mA
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	$V_{IL} = 13.0V$	13.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	$V_{IH} = 0.0V$	13.0			1.0	μA
I_{IL}	Sink Current	$V_{IL} = 0.5V$	3.5	24	93		μA
	No Key Selected	$V_{IL} = 0.5V$	13.0	27	130		μA
t_{START}	Oscillator Startup Time		3.5		3	6	ms
			13.0		0.8	1.6	ms
$C_{I/O}$	Input/Output Capacitance				12	16	pF
					10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, $V_{IL} = 3.5V$ (Pull-down)	3.5	7	17		μA
		Sink Current $V_{IL} = 13.0V$ (Pull-down)	13.0	150	400		μA
I_{IH}		Source Current, $V_{IH} = 3.0V$ (Pull-up)	3.5	90	230		μA
		Source Current, $V_{IH} = 12.5V$ (Pull-up)	13.0	370	960		μA

*Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

S2559A & B Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
I_{IH}	Mode Select Input (S2559A)	Source Current, $V_{IH} = 0.0V$ (Pull-up)	3.5	1.5	3.6		μA
		Source Current, $V_{IH} = 0.0V$ (Pull-up)	13.0	23	74		μA
I_{IL}	Chip Disable Input (S2559B)	Source Current, $V_{IL} = 3.5V$ (Pull-down)	3.5	4	10		μA
		Sink Current, $V_{IL} = 13.0V$ (Pull-down)	13.0	90	240		μA

Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... +10.5V
Operating Temperature ..... −0°C to +70°C
Storage Temperature ..... −30°C to +125°C
Power Dissipation at 25°C 1000mW
Digital Input ..... $V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$
Analog Input ..... $V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$

S2559E/F Electrical Characteristics:

(Specifications apply over the operating temperature range of 0°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				2.5		10.0	V
	Non Tone Out Mode (No Key Depressed)				1.6		10.0	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)			3.0		0.3	30	μA
				10.0		1.0	100	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)			3.0		1.0	2.0	mA
				10.0		8	16.0	mA
	Tone Output							
S2559E/F V_{OR}	Single Tone Mode Output Voltage	Row Tone,	$R_L = 390\Omega$	3.5	335	465	565	mVrms
				5.0	380	540	710	mVrms
		Row Tone,	$R_L = 240\Omega$	10.0	380	550	735	mVrms
dB_{CR}	Ratio of Column to Row Tone (Dual Tone Mode) 2559E/F			3.5 – 10.0	1.0	2.0	3.0	dB
%DIS	Distortion* 2559E/F			3.5 – 10.0			7	%
	2559G/H			4.0 – 10.0			7	%

S2559E/F Electrical Characteristics: (continued)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High	(I_{OH} = 15mA)	3.0	1.5	1.8		V
	(No Key Depressed)(Pin 2)	(I_{OH} = 50mA)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF} = 0V		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low,		2.75		0	0.5	V
	(No Key Depressed), No Load		10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High,		2.75	2.5	2.75		V
	(One Key Depressed) No Load		10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink	V_{OL} = 0.5V	3.0	0.53	1.3		mA
	Current		10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source	V_{OH} = 2.5V	3.0	0.17	0.41		mA
	Current	V_{OH} = 9.5V	10.0	0.57	1.5		mA

*Distortion is defined as "the ratio of the total power of all extraneous frequencies, in the VOICE and above 500Hz, to the total power of the DTMF frequency pair".

Table 1. Comparisons of Specified vs Actual Tone Frequencies Generated by S2559

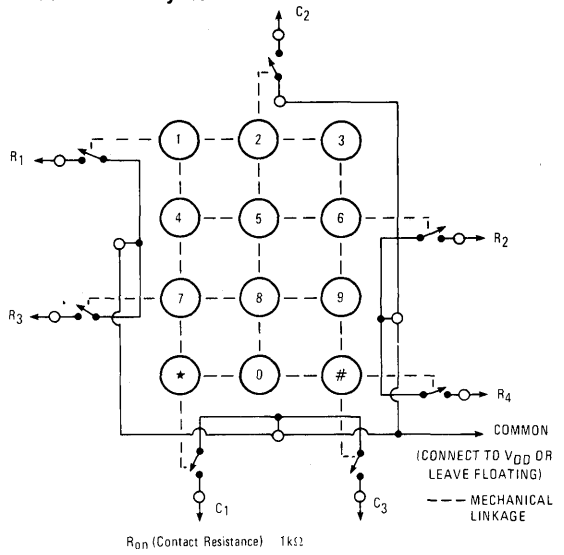
ACTIVE INPUT	OUTPUT FREQUENCY Hz		% ERROR SEE NOTE
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	−0.32
C3	1,477	1,417.9	−0.35
C4	1,633	1,645.0	+0.73

NOTE: % Error does not include oscillator drift.

Table 2. XMIT and MUTE Output Functional Relationship

OUTPUT RELEASED	'DIGIT' KEY DEPRESSED	'DIGIT' KEY	COMMENT
XMIT	V_{DD}	High Impedance	Can source at least 50mA at 10V with 1.5V max. drop
MUTE	V_{SS}	V_{DD}	Can source or sink current

Figure 1. Standard Telephone Push Button Keyboard



Circuit Description

The S2559 is designed so that it can be interfaced easily to the dual tone signaling telephone system and that it will more than adequately meet the recommended telephone industry specifications regarding the dual tone signaling scheme.

Design Objectives

The specifications that are important to the design of the DTMF Generator are summarized below: the dual tone signal consists of linear addition of two voice frequency signals. One of the two signals is selected from a group of frequencies called the "Low Group" and the other is selected from a group of frequencies called the "High Group". The low group consists of four frequencies 697, 770, 852 and 941 Hz. The high group consists of four frequencies 1209, 1336, 1477 and 1633 Hz. A keyboard arranged in a row, column format (4 rows x 3 or 4 columns) is used for number entry. When a push button corresponding to a digit (0 thru 9) is pushed, one appropriate row (R1 thru R4) and one appropriate column (C1 thru C4) is selected. The active row input selects one of the low group frequencies and the active column input selects one of the high group frequencies. In standard dual tone telephone systems, the highest high group frequency of 1633Hz (Col. 4) is not used. The frequency tolerance must be ±1.0%. However, the S2559 provides a better than .75% accuracy. The total harmonic and intermodulation distortion of the dual tone must be less than 10% as seen at the telephone terminals. (Ref. 1.) The high group to low group signal amplitude ratio should be 2.0 ±2dB and the absolute amplitude of the low group and high group tones must be within the allowed range. (Ref. 1.) These requirements apply when the telephone is used over a short loop or long loop and over the operating temperature range. The design of the S2559 takes into account these considerations.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSC_I and OSC_O terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

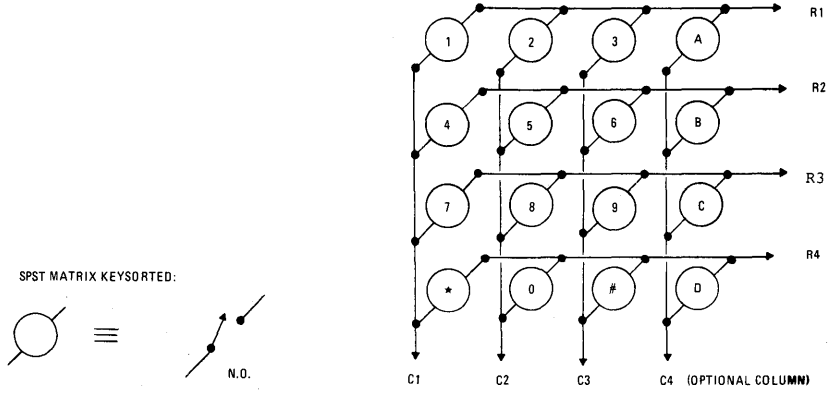
Keyboard Interface

The S2559 employs a calculator type scanning circuitry to determine key closures. When no key is depressed, active pull-down resistors are "on" on the row inputs and active pull-up resistors are "on" on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull-up or pull-down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The advantage of the scanning technique is that a keyboard arrangement of SPST switches are shown in Figure 2 without the need for a common line, can be used. Conventional telephone push button keyboards as shown in Figure 1 or X-Y keyboards with common can also be used. The common line of these keyboards can be left unconnected or wired "high".

Logic Interface

The S2559 can also interface with CMOS logic outputs directly. The S2559 requires active "High" logic levels. Since the active pull-up resistors present in the S2559 are fairly low value (500Ω typ), diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their "Low" state.

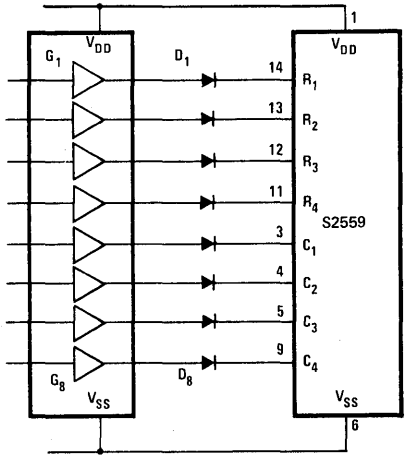
Figure 2. SPST Matrix Keyboard Arranged in the 2 of 8 Row, Column Format



Tone Generation

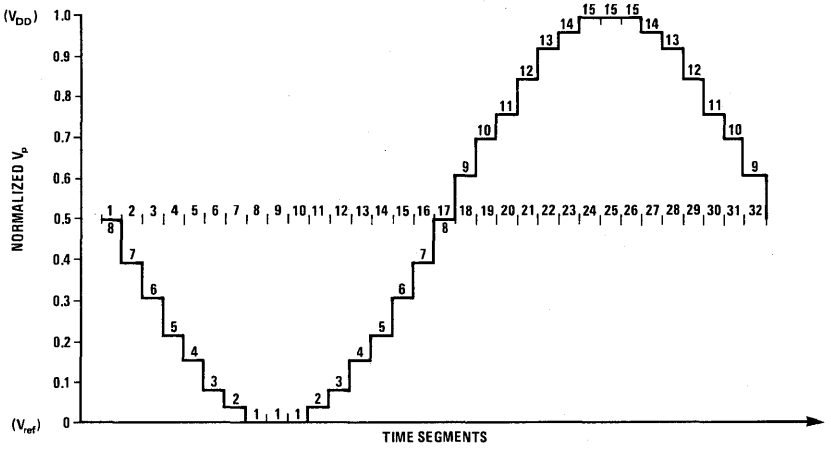
When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD} - V_{REF}$) of the stairstep function is fairly constant. V_{REF} is so chosen that V_P falls within the allowed range of the high group and low group tones.

Figure 3. Logic Interface for Keyboard Inputs of the S2559



G1 THRU G8 ANY TYPE CMOS GATE
D1 THRU D8 DIODES TYPE IN914 (OPTIONAL)

Figure 4. Stairstep Waveform of the Digitally Synthesized Sinewave



The individual tones generated by the sinewave synthesizer are then linearly added and drive a bipolar NPN transistor connected as emitter follower to allow proper impedance transformation, at the same time preserving signal level.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by activating the appropriate row input or by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Mode Select

S2559A and S2559C have a Mode Select (MDSL) input (Pin 15). When MDSL is left floating (unconnected) or connected to V_{DD}, both the dual tone and single tone modes are available. If MDSL is connected to V_{SS}, the single tone mode is disabled and no output tone is produced if an attempt for single tone is made. The S2559B and S2559D do not have the Mode Select option.

Chip Disable

The S2559B and S2559F have a Chip Disable input at Pin 15 instead of the Mode Select input. The chip disable for the S2559B and S2559F is active "high." When the chip disable is active, the tone output goes to V_{SS}, the row, column inputs go into a high impedance state, the oscillator is inhibited and the MUTE and XMIT outputs go into active states. The effect is the device essentially disconnects from the keyboard. This allows one keyboard to be shared among several devices.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ± 0.02%
$R_S \leq 100\Omega$, $L_M = 96MHY$
$C_M = 0.02pF$, $C_h = 5pF$

MUTE, XMIT Outputs

The S2559A, B, E, F have a CMOS buffer for the MUTE output and a bipolar NPN transistor for the XMIT output. With no keys depressed, the MUTE output is "low" and the XMIT output is in the active state so that substantial current can be sourced to a load. When a key is depressed, the MUTE output goes high, while the XMIT output goes into a high impedance state. When Chip Disable is "high" the MUTE output is forced "low" and the XMIT output is in active state regardless of the state of the keyboard inputs.

Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the Digital Tone Generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the Tone Output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 5 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 5 volts. The load resistor value also controls the amplitude. If R_L is low the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than 5kΩ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3581A) and amplitudes at the selected frequencies can be noted. This measurement also permits verification of the preemphasis between the individual frequency tones.

Distortion is defined as "the ratio of the **total** power of all extraneous frequencies in the **voiceband** above 500Hz accompanying the signal to the power of the frequency **pair**." This ratio must be less than 10% or when expressed in dB must be lower than – 20dB.

(Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

$$\text{Dist.} = \frac{\sqrt{(V_1)^2 + (V_2)^2 + \ldots + (V_N)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

where $(V_1) \ldots (V_N)$ are extraneous frequency (i.e., intermodulation and harmonic) components in the 500Hz to

3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$DIST_{dB} = 20 \log \frac{\sqrt{(V_1)^2 + (V_2)^2 + \ldots (V_N)^2}}{\sqrt{(V_L)^2 + (V_H)^2}}$$

$$= 10\{\log[(V_1)^2 + \ldots (V_N)^2] - \log[(V_L)^2 + (V_L)^2 + (V_H)^2]\} \ldots (1)$$

An accurate way of measuring distortion is to plot a spectrum of the signal by using a spectrum analyzer (H-P type 3580A) and an X-Y plotter (H-P type 7046A). Individual extraneous and signal frequency components are then noted and distortion is calculated by using the expression (1) above. Figure 6 shows a spectrum plot of a typical signal obtained from a S2559 device operating from a fixed supply of 4Vdc and R_L = 10kΩ in the test circuit of Figure 5. Mathematical analysis of the spectrum shows distortion to be – 30dB (3.2%). For quick estimate of distortion, a rule of thumb as outlined below can be used.

"As a first approximation distortion in dB equals the difference between the amplitude (dB) of the extraneous component that has the highest amplitude and the amplitude (dB) of the low frequency signal." This rule of thumb would give an estimate of – 28dB as distortion for the spectrum plot of Figure 6 which is close to the computed result of – 30dB.

In a telephone application amplitude and distortion are affected by several factors that are interdependent. For detailed discussion of the telephone application and other applications of the 2559 Tone Generator, refer to the applications note "Applications of Digital Tone Generator."

Ref. 1: Bell System Communications Technical Reference, PUB 47001, "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment," August 1976.

Figure 5. Test Circuit for Distortion Measurement

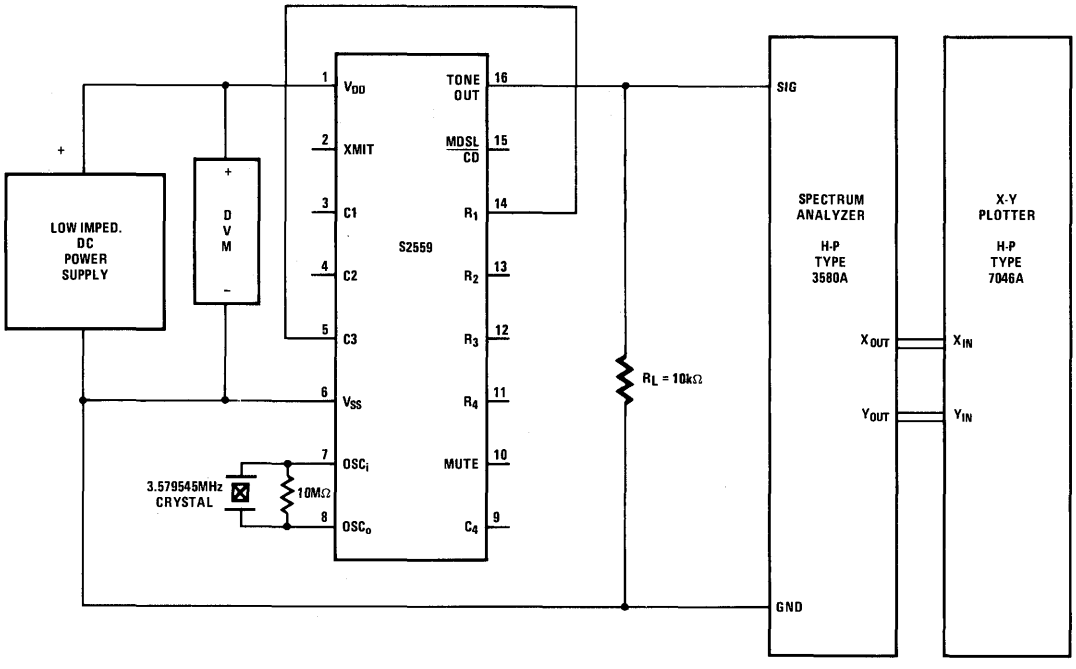
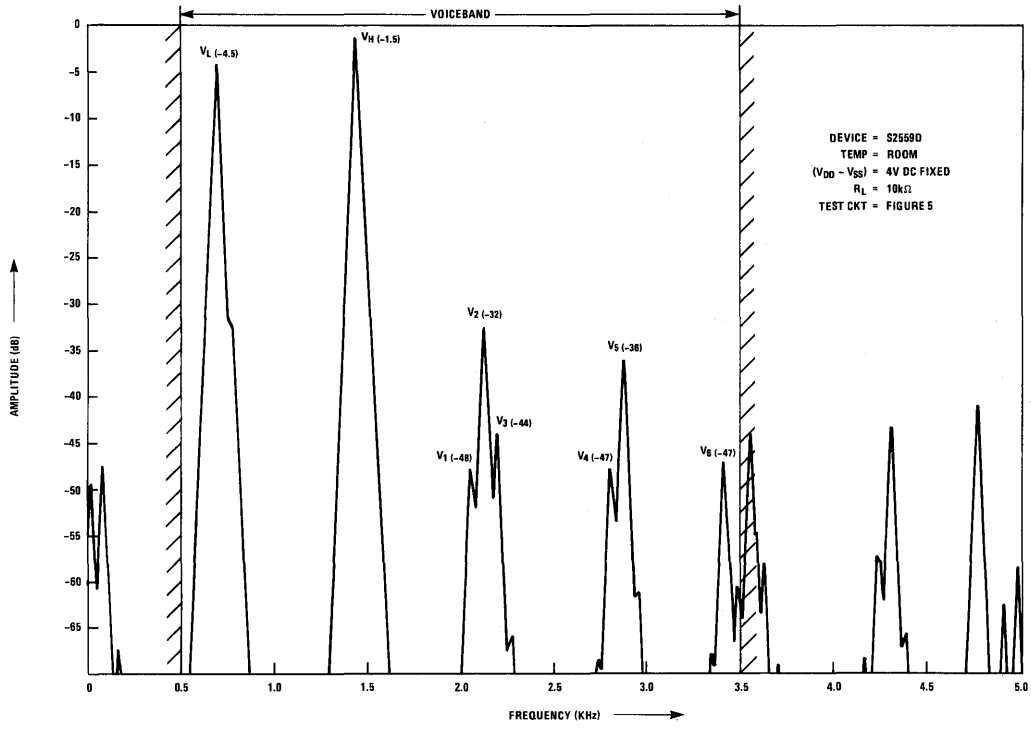


Figure 6. A Typical Spectrum Plot



DTMF Tone Generator With Binary Input

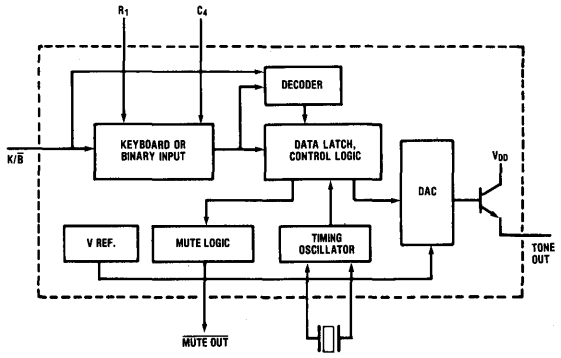
Features

- ☐ Low Voltage CMOS Process
- ☐ Uses Binary Input or Standard 3 × 4 X-Y Keyboard With Common Terminal
- ☐ Uses Standard TV Crystal (3.58MHz)
- ☐ On-Chip Reference Voltage
- ☐ The Total Harmonic Distortion is Below Industry Specification

General Description

The S2579 DTMF Generator is specifically designed to interface with External Logic or microprocessors. The S2579 can interface directly to a standard 3 × 4 keyboard with common terminal. Capable of generating 16 dual tone standard frequencies, it can operate from 3.0 to 10 volts. The electrical specifications for both S2579 and S2859 devices are identifical; please refer to S2859 data sheet for details.

Block Diagram



Pin Configuration

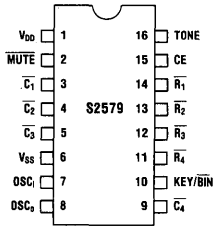
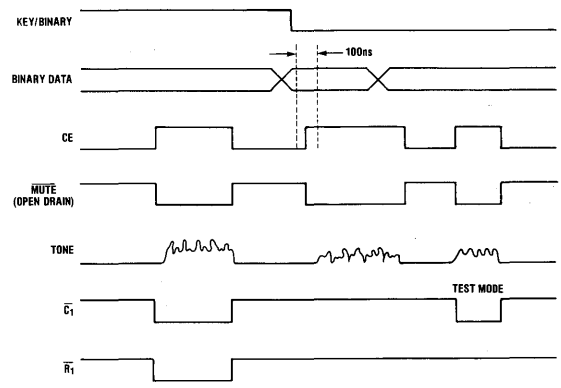


Table 1. Functional Truth Table for Logic Interface

Keyboard Inputs	Binary Inputs						Frequencies Generated	
	C1	C2	R1	R2	R3	R4	F1	Fh
1	*	*	0	0	0	1	697	1203
2	*	*	0	0	1	0	697	1336
3	*	*	0	0	1	1	697	1477
4	*	*	0	1	0	0	770	1209
5	*	*	0	1	0	1	770	1336
6	*	*	0	1	1	0	770	1477
7	*	*	0	1	1	1	852	1209
8	*	*	1	0	0	0	852	1336
9	*	*	1	0	0	1	852	1477
0	*	*	1	0	1	0	941	1336
*	*	*	1	0	1	1	941	1209
#	*	*	1	1	0	0	941	1477
A	*	*	1	1	0	1	697	1633
B	*	*	1	1	1	0	770	1633
C	*	*	1	1	1	1	852	1633
D	*	*	0	0	0	0	941	1633
	0	*		VALID DATA				Fh
	*	0		VALID DATA			F1	

* Indicates Normally Open.

Figure 1.



AMI

A Subsidiary of Gould Inc.

S2859

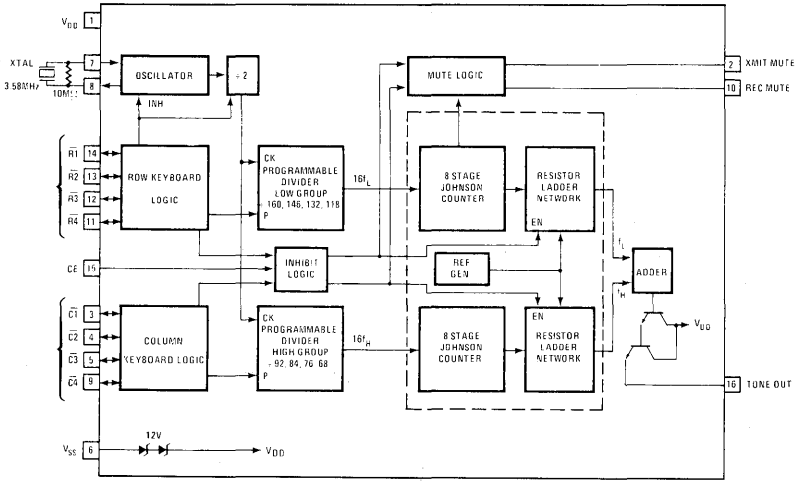
DTMF TONE GENERATOR

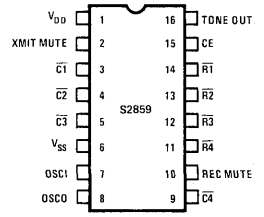
COMMUNICATION PRODUCTS

Features

- ☐ Wide Operating Supply Voltage Range: 3.0 to 10 Volts
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V
- ☐ Uses TV Crystal Standard (3.58 MHz) to Derive All Frequencies thus Providing Very High Accuracy and Stability
- ☐ Timing Sequence for XMIT, REC MUTE Outputs
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard with Common Terminal
- ☐ The Total Harmonic Distortion is Below Industry Specification
- ☐ On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range
- ☐ Single Tone as Well as Dual Tone Capability
- ☐ Darlington Configuration Tone Output

Block Diagram





General Description

The S2859 DTMF Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton telephone keyboard or X-Y keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2859 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, point-of-sale, and credit card verification terminals and process control.

Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD} - V_{SS}$)	+ 10.5V
Operating Temperature	0°C to + 70°C
Storage Temperature	− 55°C to + 125°C
Power Dissipation at 25°C	500mW
Input Voltage	$V_{SS} - 0.6 \leq V_{IN} \leq V_{DD} + 0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of − 0°C to + 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				3.0	—	10.0	V
	Non Tone Out Mode (Mute Outputs Toggle With Key Depressed)				2.2	—	10.0	V
V_Z	Internal Zener Diode Voltage, I_Z = 5mA			—	—	12.0	—	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone and Mute Outputs Unloaded)			3.0 10.0	— —	0.001 0.003	0.3 1.0	mA mA
	Operating (One Key Selected, Tone and Mute Outputs Unloaded)			3.0 10.0	— —	1.3 11	2.0 18	mA mA
	Tone Output							
V_{OR}	Single Tone Mode Output Voltage	Row	$R_L = 100\Omega$	5.0	366	462	581	mVrms
		Tone	$R_L = 100\Omega$	10.0	370	482	661	mVrms
dB_{CR}	Ratio of Column to Row Tone			3.0 – 10.0	1.0	2.0	3.0	dB
%DIS	Distortion*			3.0 – 10.0	—	—	10	%
	REC, XMIT MUTE Outputs							
I_{OH}	Output Source Current		$V_{OH} = 1.2V$	2.2	0.43	1.1	—	mA
			$V_{OH} = 2.5V$	3.0	1.3	3.1	—	mA
			$V_{OH} = 9.5V$	10.0	4.3	11	—	mA

*Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair"

AMI

A Subsidiary of Gould Inc.

S2560A

PULSE DIALER

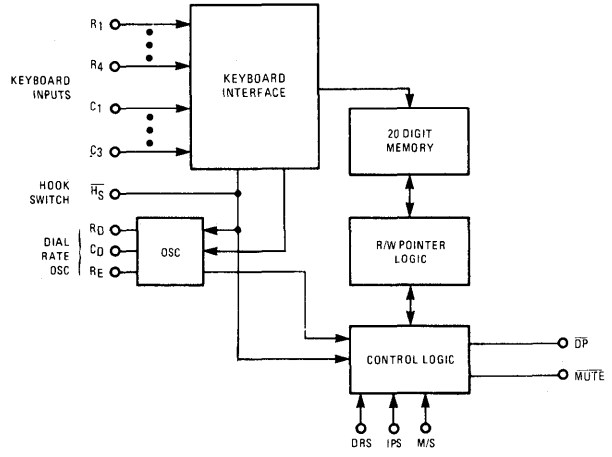
Features

- ☐ Low Voltage CMOS Process for Direct Operation from Telephone Lines
- ☐ Inexpensive R-C Oscillator Design Provides Better than ± 5% Accuracy Over Temperature and Unit to Unit Variations
- ☐ Dialing Rate Can be Varied by Changing the Dial Rate Oscillator Frequency
- ☐ Dial Rate Select Input Allows Changing of the Dialing Rate by a 2:1 Factor Without Changing Oscillator Components
- ☐ Two Selections of Mark/Space Ratios (33⅓/66⅔ or 40/60)
- ☐ Twenty Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Mute and Dial Pulse Drivers on Chip
- ☐ Accepts DPCT Keypad with Common Arranged in a 2 of 7 Format; Also Capable of Interface to SPST Switch Matrix

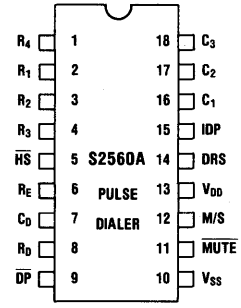
General Description

The S2560A Pulse Dialer is a CMOS integrated circuit that converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone lines with minimum interface. Storage is provided for 20 digits, therefore, the last dialed number is available for redial until a new number is entered. IDP is scaled to the dialing rate such as to produce smaller IDP at higher dialing rates. Additionally, the IDP can be changed by a 2:1 factor at a given dialing rate by means of the IDP select input.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leqslant V_{DD} - V_{SS} \leqslant 3.5V$ unless otherwise specified.

Symbol	Parameter	V_{DD}-V_{SS} (Volts)	Min.	Max.	Units	Conditions
	Output Current Levels					
I_{OLDP}	DP Output Low Current (Sink)	3.5	125		µA	V_{OUT} = 0.4V
I_{OHDP}	DP Output High Current (Source)	1.5 3.5	20 125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	MUTE Output Low Current (Sink)	3.5	125		µA	V_{OUT} = 0.4V
I_{OHM}	MUTE Output High Current (Source)	1.5 3.5	20 125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLT}	Tone Output Low Current (Sink)	1.5	20		µA	V_{OUT} = 0.4V
I_{OHT}	Tone Output High Current (Source)	1.5	20		µA	V_{OUT} = 1V
V_{DR}	Data Retention Voltage		1.0		V	"On Hook" $\overline{HS}$ = V_{DD}. Keyboard open, all other input pins to V_{DD} or V_{SS}
I_{DD}	Quiescent Current	1.0		750	nA	
I_{DD}	Operating Current	1.5 3.5		100 500	µA µA	$\overline{DP}$, $\overline{MUTE}$ open, $\overline{HS}$ = V_{SS} ("Off Hook") Keyboard processing and dial pulsing at 10 pps at conditions as above
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	1.5 to 2.5 2.5 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50K\Omega \leqslant R_D \leqslant 750K\Omega$; $100pF \leqslant C_D{}^* \leqslant 1000pF$; $750k\Omega \leqslant R_E \leqslant 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD} - V_{SS}$)	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of ($V_{DD} - V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leqslant V_I \leqslant V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded. When power is first applied to the device, the device should be in "On Hook" condition ($\overline{HS} = 1$). This is necessary because there is no internal power or reset on chip and for proper operation all internal latches must come up in a known state. In applications where the device is hard wired in "Off Hook" ($\overline{HS} = 0$) condition, a momentary "On Hook" condition can be presented to the device during power up by use of a capacitor resistor network as shown in Figure 6.

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

The device contains an oscillator circuit that requires three external components: two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including the "on hook" condition. For a dialing rate of 10pps the oscillator should be adjusted to 2400Hz. Typical values of external components for this are R_D and $R_E = 750k\Omega$ and $C_D = 270pF$. It is recommended that the tolerance of resistors to be 5% and capacitor to be 1% to insure a 10% tolerance of the dialing rate in the system.

Keyboard Interface (S2560A)

The S2560A employs a scanning technique to determine a key closure. This permits interface to a DPCT keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2) and interface to a SPST switch matrix (Figure 7). A high level on the appropriate row and column inputs constitutes a key closure for logic interface. When using a SPST switch matrix, it is necessary to add small capacitors (30pF) from the column inputs to V_{SS} to insure that the oscillator is shut off after a key is released or after the dialing is complete.

OFF Hook Operation: The device is continuously powered through a 150kΩ resistor during Off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The $\overline{DP}$ output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during the pulse break. The $\overline{MUTE}$ output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

ON Hook Operation: The device is continuously powered through a 10-20MΩ resistor during the ON hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20pps can be achieved. Dialing rates of 7 and 14pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14pps, IDP's of 1143ms and 572ms can be similarly obtained. If the IDP select is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10pps an IDP of 800ms is obtained and at 20pps an IDP of 400ms is obtained.

The user can enter a number up to 20 digits long from a standard 3x4 double contact keypad with common (Figure 1). It is also possible to use a logic interface as shown in Figure 2 for number entry. Antibounce protection circuitry is provided on chip (min. 20ms) to prevent false entry.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed twenty.

Auto Dialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

Table 1. S2560A/S2560B Pin/Function Descriptions

Pin	Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	2, 3, 4, 1, 16, 17, 18	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 2. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 20ms).
Inter-Digit Pause Select (IDP)	15	One programmable line is available that allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceding the first dialed pulse is an inter-digit time equal to the selected IDP. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Dial Rate Select (DRS)	14	A programmable line allows selection of two different output rates such as 7 or 14 pps, 10 or 20 pps, etc. See Tables 2 and 3.
Mark/Space (M/S)	12	This input allows selection of the mark/space ratio, as per Table 3.
Mute Out ($\overline{MUTE}$)	11	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.
Dial Pulse Out ($\overline{DP}$)	9	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator (R_E, C_D, R_D)	6, 7, 8	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	5	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	13, 10	These are the power supply inputs. The device is designed to operate from 1.5V–3.5V.

Figure 1. Standard Telephone Pushbutton Keyboard

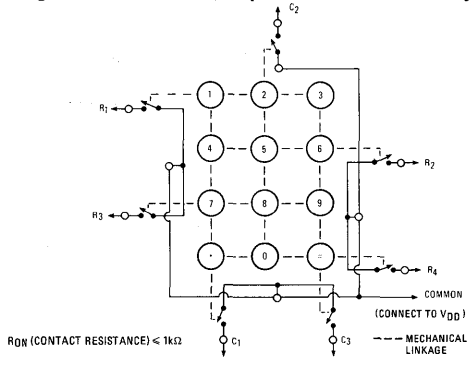


Figure 2. Logic Interface for the S2560

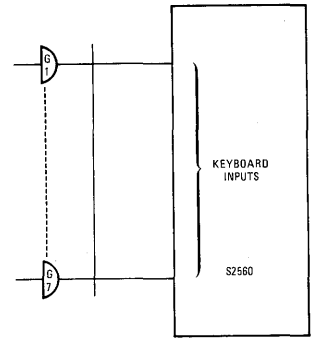


Figure 3. Timing

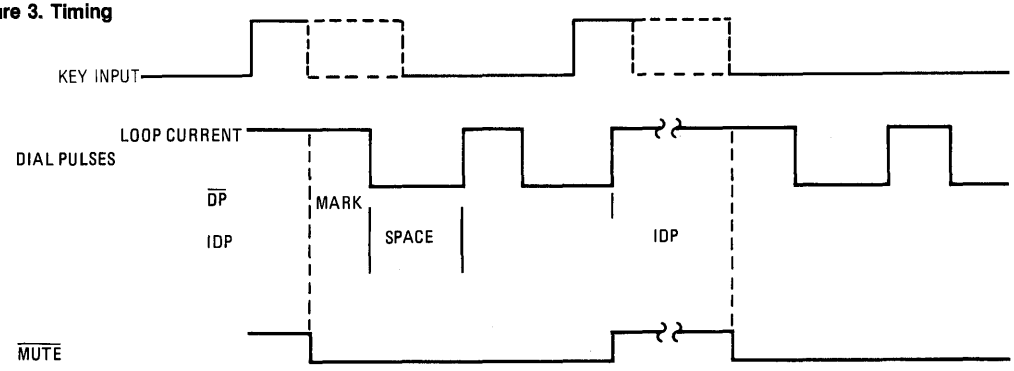


Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)	
					DRS = V_{SS}	DRS = V_{DD}	IPS = V_{SS}	IPS = V_{DD}
5.5/11	1320				5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680	Select components in the			7	14	1142	571
7.5/15	1800	ranges indicated in table			7.5	15	1066	533
8/16	1920	of electrical specifications			8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
$(f_d/240)$/ $(f_d/120)$	f_d				$(f_d/240)$	$(f_d/120)$	$\frac{1920}{f_i} \times 10^3$	$\frac{960}{f_i} \times 10^3$

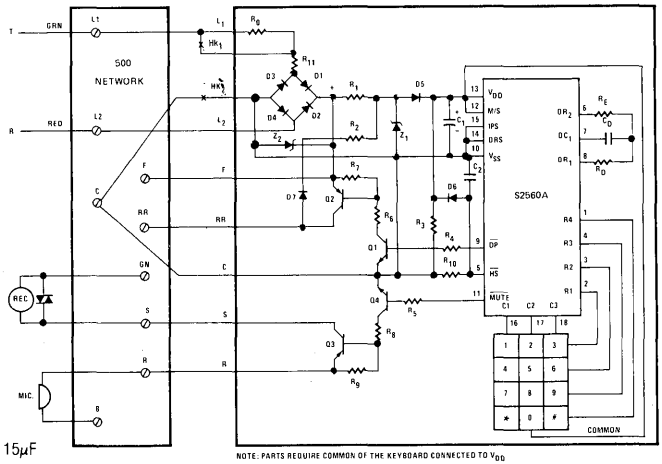
NOTE: IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14pps, and IDP of either 1142ms or 571ms can be selected.

Table 3.

Function	Pin Designation	Input Logic Level	Selection
Dial Pulse Rate Selection	DRS (14)	V_{SS} V_{DD}	(f/240)pps (f/120)pps
Inter-Digit Pause Selection	IDP (15)	V_{DD} V_{SS}	$\frac{960}{f}$ s $\frac{1920}{f}$ s
Mark/Space Ratio	M/S (12)	V_{SS} V_{DD}	33⅓/66⅔ 40/60
On Hook/Off Hook	$\overline{HS}$ (5)	V_{DD} V_{SS}	On Hook Off Hook

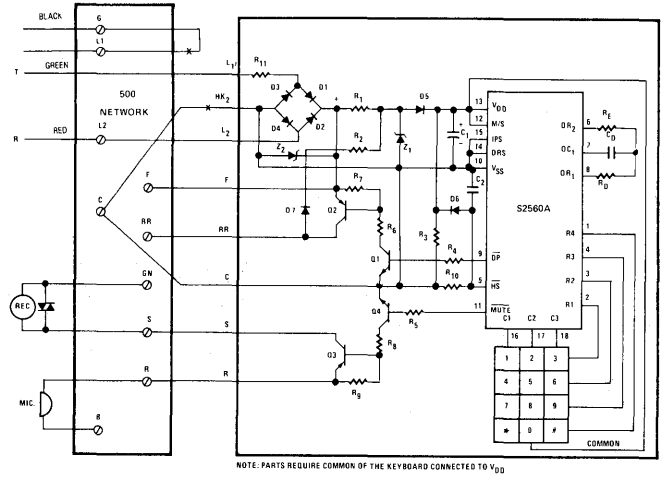
NOTE: f is the oscillator frequency and is detemined as shown in Figure 5.

Figure 4. Pulse Dialer Circuit with Redial



$R_0 = 10\text{-}20M\Omega$, $R_1 = 150k\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$, $R_{10} = 47k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, D_1—$D_4 = IN4004$, D_5, D_6, $D_7 = IN914$, $C_1 = 15\mu F$
$R_E = R_D = 750k\Omega$, $C_D = 270pF$, $C_2 = 0.01\mu F$
Q_1, $Q_4 = 2N5550$ TYPE Q_2, $Q_3 = 2N5401$ TYPE
$Z_2 = IN5379$ 110V ZENER OR 2XIN4758

Figure 5. Pulse Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



$R_1 = 10\text{-}20M\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$
$R_{10} = 47k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, D_1—$D_4 = IN4004$
D_5, D_6, $D_7 = IN914$, $C_1 = 15\mu F$
R_E, $R_D = 750k\Omega$, $C_D = 270pF$
$C_2 = 0.01\mu F$, Q_1, $Q_4 = 2N5550$
Q_2, $Q_3 = 2N5401$
$Z_2 = 150V$ ZENER OR VARISTOR TYPE GE MOV150

Figure 6. Circuit for Applying Momentary "ON Hook" Condition During Power Up

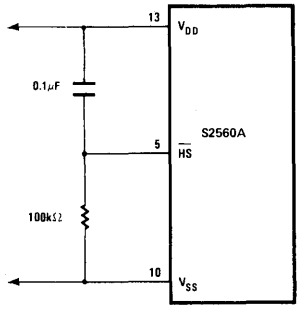
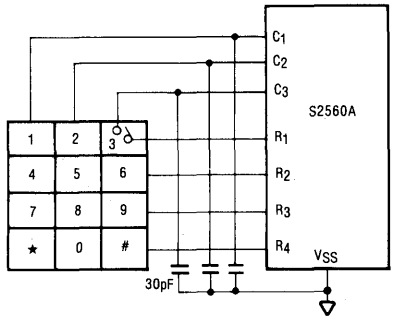


Figure 7. SPST Switch Matrix Interface



Advanced Product Description

S2560G/S2560G1

PULSE DIALER

General Description

The S2560G is a modified version of the S2560A Pulse Dialer with complete pin/function compatibility. It is recommended to be used in all new and existing designs. Most electrical specifications for both devices are identical. Please refer to S2560A data sheet for details. S2560G1 is low voltage version of S2560G.

Differences between the two devices are summarized below:

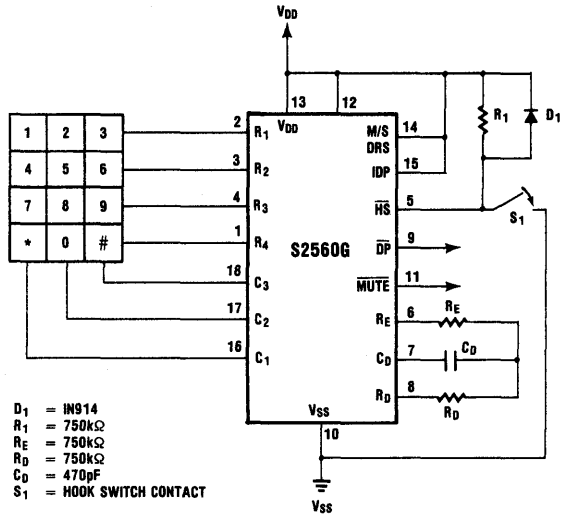
	2560G	2560G1	2560A
Operating Voltage, Dialing:	2.0V to 3.5V	1.5V to 3.5V	1.5V to 3.5V
Operating Voltage, Voice Mode:	1.5V to 3.5V	1.5V to 3.5V	1.5V to 3.5V
Data Retention Voltage (Minimum):	1.0V	1.0V	1.0V
I_{DD} Operating Current:	200μA@2.0V 1000μA@3.5V	100μA@1.5V 500μA@3.5V	100μA@1.5V 500μA@3.5V
I_{DD} Standby Current:	2μA@1V	750μA@1V	750nA@1V
Keyboard Debounce Time:	10msec		16msec
X-Y Keyboard Interface:	Does not need capacitors		Capacitors required between column inputs and V_{SS}
Redial Buffer:	22 digits		20 digits
Dialing Characteristics:	Can dial more than 22 digits. Redial disabled if more than 22 digits are entered.		Accepts a maximum of 20 digits. Will not dial additional digits.
Inter-digit pause timing	Follows dial pulses.		Precedes dial pulses

Application Suggestions

1) In most existing designs, the S2560G will work in place of S2560A without any modifications. Problems may arise however, if the keyboard bounce time exceeds 10ms. In such a case, the device may interpret a single key entry as a double key. To avoid this false detection, the keyboard debounce time can be easily increased from 10ms to 20ms by changing the Oscillator Frequency from 2400Hz down to 1200Hz. This is done by changing the value of the capacitor connected to pin 7 from 270pF to 470pF. To preserve the dialing rate at 10pps and IDP at 800ms the DRS and IDP pins now must be connected to V_{DD} instead of V_{SS}. Figure 1 shows the implementation details. Note, that interfacing with X-Y keyboard no longer requires capacitors to V_{SS} from column pins.

2) The hookswitch input pin (pin 5) must be protected from spikes that can occur when the phone goes from off-hook condition to on-hook. Voltage exceeding V_{DD} on this pin can cause the device to draw excessive current. This will discharge the capacitor across V_{DD} and V_{SS} causing the supply voltage to drop. If the voltage drops below 1 volt (data retention voltage) the device could lose redial memory. To prevent the voltage on the hookswitch pin from exceeding V_{DD}, an external diode must be added on the hookswitch pin as shown in Figure 1.

Figure 1. Transient Protection Technique Using Diode Between V_{DD} and $\overline{HS}$



A Subsidiary of Gould Inc.

Advanced Product Description

S2561/S2561A/S2561C

TONE RINGER

Features

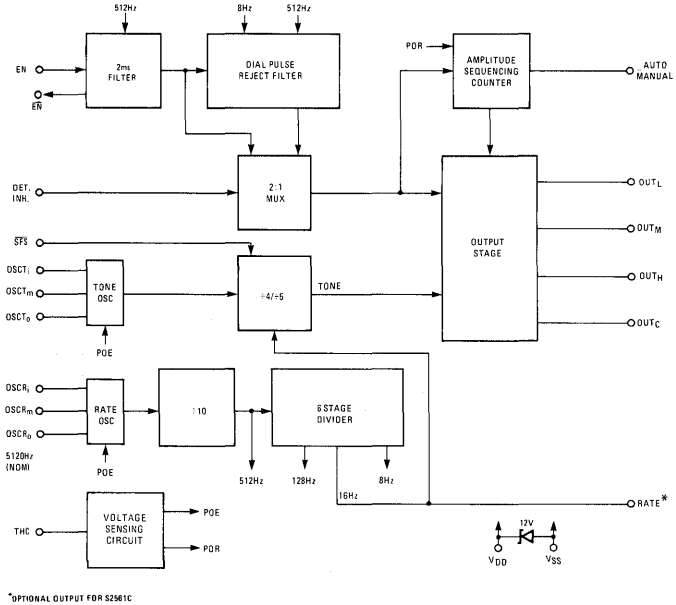
- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- ☐ Also Capable of Logic Interface for Non-Telephone Applications
- ☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
- ☐ 50mW Output Drive Capability at 10V Operating Voltage
- ☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- ☐ Single Frequency Tone Capability

General Description

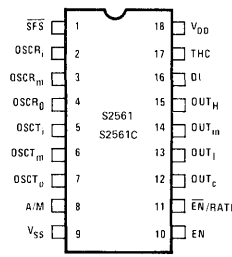
The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

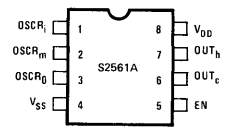
Data Subject to change at any time without notice. These sheets transmitted for information only.

Block Diagram



Pin Configuration





Absolute Maximum Ratings:

Supply Voltage	+ 12.0V*
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	− 40°C to + 125°C
Voltage at any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Lead Temperature (Soldering, 10sec)	300°C

*This device incorporates a 12V internal zener diode across the V_{DD} to V_{SS} pins. Do NOT connect a low impedance power supply directly across the device unless the supply voltage can be maintained below 12V or current limited to <25mA.

Electrical Characteristics:

Specifications apply over the operating temperature and $3.5V \leqslant V_{DD}$ to $V_{SS} < 12.0V$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{DS}	Operating Voltage (V_{DD} to V_{SS})	8.0	12.0	V	Ringing, THC pin open
V_{DS}	Operating Voltage	4.0		V	"Auto" mode, non-ringing
I_{DS}	Operating Current		500	μA	Non-ringing, $V_{DD} = 10V$, THC pin open, DI pin open or V_{SS}
I_{OHC}	Output Drive Output Source Current (OUT_H, OUT_C outputs)	5		mA	$V_{DD} = 10V$, $V_{OUT} = 8.75V$
I_{OLC}	Output Sink Current (OUT_H, OUT_C outputs)	5		mA	$V_{DD} = 10V$, $V_{OUT} = 0.75V$
I_{OHM}	Output Source Current (Out_M output)	2		mA	$V_{DD} = 10V$, $V_{OUT} = 8.75V$
I_{OLM}	Output Sink Current (OUT_M output)	2		mA	$V_{DD} = 10V$, $V_{OUT} = 0.75V$
I_{OHL}	Output Source Current (OUT_L output)	1		mA	$V_{DD} = 10V$, $V_{OUT} = 8.75V$
I_{OLL}	Output Sink Current (OUT_L output)	1		mA	$V_{DD} = 10V$, $V_{OUT} = 0.75V$
	CMOS to CMOS				
V_{IH}	Input Logic "1" Level	0.7 V_{DD}	$V_{DD} + 0.3$	V	All inputs
V_{IL}	Input Logic "0" Level	$V_{SS} - 0.3$	0.3 V_{DD}	V	All inputs
V_{OHR}	Output Logic "1" Level (Rate output)	0.9 V_{DD}		V	$I_O = 10\mu A$ (Source)
V_{OLR}	Output Logic "0" Level (Rate output)		0.5	V	$I_O = 10\mu A$ (Sink)
V_{OZ}	Output Leakage Current (OUT_H, OUT_M outputs in high impedance state)		1 1	μA μA	$V_{DD} = 10V$, $V_{OUT} = 0V$ $V_{DD} = 10V$, $V_{OUT} = 10V$
C_{IN}	Input Capacitance		7.5	pF	Any pin
Δfo/fo	Oscillator Frequency Deviation	− 5	+ 5	%	Fixed RC component values $1M\Omega \leqslant R_{ri}$, $R_{ti} \leqslant 5M\Omega$; $100k\Omega \leqslant R_{rm}$, $R_{tm} \leqslant 750k\Omega$; $150pF \leqslant C_{ro}$, $C_{to} \leqslant 3000pF$; 330pF recommended value of C_{ro} and C_{to}, supply voltage varied from 9V ± 2V (over temperature and unit-unit variations)
R_{LOAD}	Output Load Impedance Connected Across OUT_H and OUT_C	600		Ω	Tone Frequency Range = 300Hz to 3400Hz
I_{IH}, I_L	Leakage Current, $V_{IN} = V_{DD}$ or V_{SS}		100	nA	Any input, except DI pin $V_{DD} = 10V$
V_{TH}	POE Threshold Voltage	6.5	8	V	
V_Z	Internal Zener Voltage	11	13	V	$I_Z = 5mA$

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leqslant V_I \leqslant V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

Functional Description

The S2561 is a CMOS device capable of simulating the effects of the telephone bell. This is achieved by producing a tone that shifts between two predetermined frequencies (512 and 640Hz) with a frequency ratio of 5:4 at a 16Hz rate.

Tone Generation: The output tone is derived from a tone oscillator that uses a 3 pin R-C oscillator design consisting of one capacitor and two resistors. The oscillator frequency is divided alternately by 4 or 5 at the shift rate. Thus, with the oscillator adjusted for 5120Hz, a tone signal is produced that alternates between 512Hz and 640Hz at the shift rate. The shift rate is derived from another 3 pin R-C oscillator which is adjusted for a nominal frequency of 5120Hz. It is divided down to 16Hz which is used to produce the shift in the tone frequency. It should be noted that in the special case where both oscillators are adjusted for 5120Hz, it is only necessary to have one external R-C network for one oscillator with the other oscillator driven from it. The oscillators are designed such that for fixed R-C component values an accuracy of ±5% can be obtained over the operating supply voltage, temperature and unit-unit variations. See Table 1 for component and frequency selections. In the single frequency mode, activated by connecting the $\overline{SFS}$ input to V_{SS} only the higher frequency continuous tone is produced by using a fixed divider ratio of 4 and by disabling the shift operation.

Ring Signal Detection: In the following description it is assumed that both the tone and rate oscillators are adjusted for a frequency of 5120Hz. Ringing signal (nominally 42 to 105 VAC, 20Hz, 2 sec on/4 sec off duty cycle) applied by the central office between the telephone line pair is capacitively coupled to the tone ringer circuitry as shown in Figure 2. Power for the device is derived from the ringing signal itself by rectification (diodes D1 thru D4) and zener diode clamping (Z_2). The signal is also applied to the EN input after limiting and clamping by a resistor (R_2) and internal diodes to V_{DD} and V_{SS} supplies. Internally the signal is first squared up and then processed thru a 2ms filter followed by a dial pulse reject filter. The 2ns filter is a two-stage register clocked by a 512Hz signal derived from the rate oscillator by a divide by 10 circuit. The squared ring signal (typically a square wave) is applied to the D input of the first stage and also to reset inputs of both stages. This provides for rejection of spurious noise spikes. Signals exceeding a duration of 2ms only can pass through the filter.

The dial pulse reject filter is clocked at 8Hz derived from the rate oscillator by divide by 640 circuit. This circuit is designed to pass any signal that has at least two transitions in a given 125ms time period. This insures that signals below 8Hz will be rejected with certainty. Signals over 16Hz will be passed with certainty and between 8Hz and 16Hz there is a region of uncertainty. By adjusting the rate oscillator to a different frequency the break points of 10Hz and 20Hz the rate oscillator can be adjusted to 6400Hz. Of course this also increases the tone shift rate to 20Hz. The action of the dial pulse reject filter minimizes the dial pulse interference during dialing although it does not completely eliminate it due to the rather large region of uncertainty associated with this type of discrimination circuitry. The dial pulse filter also has the characteristic that an input signal is not detected unless its duration exceeds 125ms. This insures that the tone ringer will not respond to momentary bursts of ringing less than 125 milliseconds in duration (Ref. 1).

In logic interface applications, the 2ms filter and the dial pulse reject filter can be inhibited by wiring the Det. INHIBIT pin to V_{DD}. This allows the tone ringer to be enabled by a logic '1' level applied at the "ENABLE" input without the necessity of a 20Hz ring signal.

Voltage Sensing: The S2561 contains a voltage sensing circuit that enables the output stage and the rate and tone oscillators, only when the supply voltage exceeds a predetermined value. Typical value of this threshold is 7.3 volts. This prduces two benefits. First, it insures that the audible intensity of the output tone is fairly constant throughout the ringing period; and secondly, it insures proper circuit operation during the "auto" mode operation by reducing the power consumption to a minimum when the supply voltage drops below 7.3 volts. This extends the supply voltage decay time beyond 4 seconds (off period of the ring signal) with an adequate filter capacitor and insures the proper functioning of the "amplitude sequencing" counter. It is important to note that the operating supply voltage should be well above the threshold value during the ringing period and that the filter capacitor should be large enough so that the ripple on the supply voltage does not fall below the threshold value. A supply voltage of 10 to 12 volts is recommended.

In applications where the tone ringer is continuously powered and below the threshold level, the internal threshold can be bypassed by connecting the THC pin to V_{DD}. The internal threshold can also be reduced by

connecting an external zener diode between the THC and V_{DD} pins.

Auto Mode: In the "auto" mode, activated by wiring the "auto/manual" input to V_{SS}, an amplitude sequencing of the output tone can be achieved. Resistors R_L and R_M are inserted in series with the Out_L and Out_M outputs, respectively, and paralleled with the Out_H output (Figure 1). Load is connected across Out_H and Out_C pins. R_L is chosen to be higher than R_M. In this manner the first ring is of the lowest amplitude, second ring is of medium amplitude and the third and consecutive rings thereafter are at maximum amplitude. For the proper functioning of the "amplitude sequencing" counter the device must have at least 4.0 volts across it throughout the ring sequence. The filter capacitor is so chosen that the supply voltage will not drop below 4.0 volts during the off period. At the end of a ring sequence when the off period substantially exceeds the 4 second duration, the counter will be reset. This will insure that the amplitude sequencing will start correctly beginning a new ring sequence. The counter is held in reset during the "manual" mode operation. This produces a maximum ring amplitude at all times.

Figure 1-A. Output Stage Connected for Auto Mode Operation

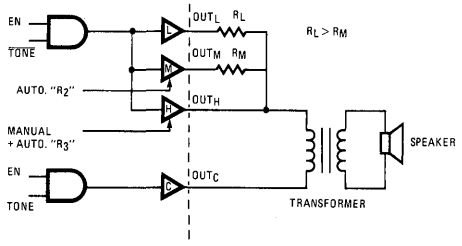


Figure 1-B. Output Stage Connected for Manual Mode Operation

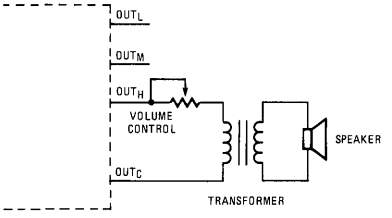
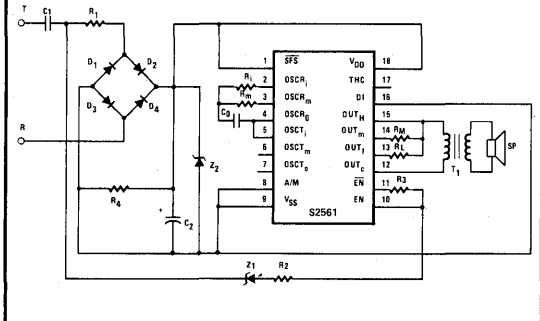
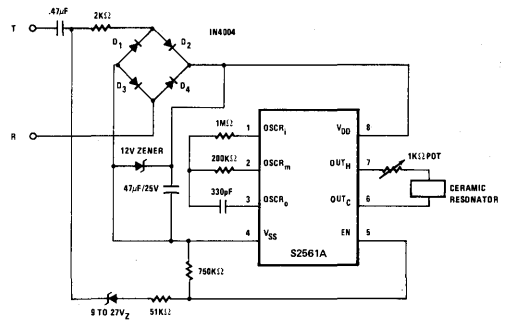


Figure 2-A. Typical Telephone Application of the S2561



C_1	.47μF/200V	R_1	2KΩ	R_i	1MΩ	R_L	18KΩ	SP	8ΩSPEAKER
C_2	47μF/25V	R_2	51KΩ	R_m	200KΩ	R_M	3.3KΩ	T_1	2000Ω/8ΩXFMR
D_1–D_4	IN4004	R_3	10MΩ	C_0	300pF	R_4	100KΩ	Z_1	9 TO 27V ZENER
Z_2	IN4742 12V ZENER								

Figure 2-B. Typical Telephone Application of the S2561A



Output Stage: The output stage is of push-pull type consisting of buffers L, M, H and C. The load is connected across pins Out_H and Out_C (Figure 2). During ringing, the Out_H and Out_C outputs are out of phase with each other and pulse at the tone rate. During a non-ringing state, all outputs are forced to a known level such as ground which insures that there is no DC component in the load. Thus, direct coupling can be used for driving the load. The major benefit of the push-pull arrangement is increased power output. Four times as much power can be delivered to the load for the same operating voltage. Buffers M and H are three-state. In the "auto" mode buffer M is active only during the second ring and in the "high impedance" state at all other times. Buffer H is active beginning the third ring. In the "manual" mode buffers H, L and C are active at all times while buffer M is in a high impedance state. The output buffers are so designed that they can source or sink 5mA at a V_{DD} of 10 volts without appreciable voltage drop. Care has been taken to make them symmetrical in both source and sink configurations. Diode clamping is provided on all outputs to limit the voltage spikes associated with transformer drive in both directions V_{DD} and V_{SS}.

Normal protection circuits are present on all inputs.

Table 1. S2561/S2561C Pin/Function Descriptions (S2561A)

Pin	Number	Function
Power (V_{DD}*, V_{SS}*)	18, 9 8,4	These are the power supply pins. The device is designed to operate over the range of 3.5 to 12.0 volts. A range of 10 to 12 volts is recommended for the telephone application.
Ring Enable (EN*, $\overline{EN}$)	10, 11, 5	These pins are for the 20Hz ring enable input. They can also be used for DC level enabling by wiring the DI pin to V_{DD}. $\overline{EN}$ is available for the S2561 only.
Auto/Manual (A/M)	8	"Auto" mode for amplitude sequencing is implemented by wiring this pin to V_{SS}. "Manual" mode results when connected to V_{DD}. The amplitude sequencing counter is held in reset during the "manual" mode.
Outputs (Out_L, Out_M, Out_H^*, Out_C^*)	13, 14, 15, 7, 6	These are the push-pull outputs. Load is directly connected across Out_H and Out_C outputs. In the "auto" mode, resistors R_L and R_M can be inserted in series with the Out_L and Out_M outputs for amplitude sequencing (see Figure 1).
Oscillators Rate Oscillator ($OSCR_i^*$, $OSCR_m^*$ $OSCR_o^*$)	2, 3, 4, 1, 2, 3	These pins are provided to connect external resistors RR_i, RR_m and capacitor CR_o to form an R-C oscillator with a nominal frequency of 5120Hz. See Table 2 for components selection.
Tone Oscillator ($OSCT_i$, $OSCT_m$, $OSCT_o$)	5, 6, 7	These pins are provided to connect external resistors RT_i, RT_m and capacitor CT_o to form an R-C oscillator from which the tone signal is derived. With the oscillator adjusted to 512Hz and 640Hz results. See Table 2 for components selection.
Threshold Control (THC)	17	The internal threshold voltage is brought out to this pin for modification in non-telephone applications. It should be left open for telephone applications. For power supplies less than 9V connect to V_{DD}.
Rate	11	This is an optional output for the S2561C version which replaces the EN output. This is a 16Hz output that can be used by external logic as shown in Figure 3-A to produce a 2sec on/4sec off waveform.

Table 1. (Continued)

Pin	Number	Function
Detector Inhibit (DI)	16	When this pin is connected to V_{DD}, the dial pulse reject filter is disabled to allow DC level enabling of the tone ringer. This pin should be hardwired to V_{SS} in normal telephone-type applications.
Single Frequency Select (SFS)	1	When this pin is connected to V_{SS}, only a single frequency continuous tone is produced as long as the tone ringer is enabled. In normal applications this pin should be hardwired to V_{DD}.

*Pinouts of 8 pin S2561A package.

Table 2. Selection Chart for Oscillator Components and Output Frequencies

Tone/Rate Oscillator Frequency (Hz)	Oscillator Components R_I (kΩ)	R_M (kΩ)	C_O (pF)	Rate (Hz)	Tone (Hz)
5120	1000	200	330	16	512/640
6400	Select components in the ranges indicated in the table of electrical characteristics			20	640/800
3200				10	320/400
8000				25	800/1000
fo				$\frac{fo}{320}$	$\frac{fo}{10}$ $\frac{fo}{8}$

Applications

Typical Telephone Application: Figure 2 shows the schematic diagram of a typical telephone application for the S2561 tone ringer. Circuit power is derived from the telephone lines by the network formed by capacitor C_1, resistor R_1, diode bridge D_1 through D_4, and filter capacitor C_2. C_2 is chosen to be large enough so as to insure that the power supply ripple during ringing does not fall below the internal threshold level (typ. 7.3 volts) and to provide large enough decay time during the off period. A typical value of C_2 may be .47μF. C_1 and R_1 are chosen to satisfy the Ringer Equivalence Number (REN) specification (Ref. 1). For REN = 1 the resistor should be a minimum of 8.2kΩ. It must be noted that the amount of power that can be delivered to the load depends upon the selection of C_1 and R_1.

The device is enabled by limiting the incoming ring signal through resistors R_2, R_3 and diodes d_5 and d_6. Zener diode Z_1 (typ. 9-27 volts) may be required in certain applications where large voltage transients may occur on the line during dial pulsing. The internal 2ms filter and the dial pulse reject filter will suppress any undesirable components of the signal and will only respond to the normal 20Hz ring signal. Ring signals with frequencies above 16Hz will be detected.

The configuration shown will produce a tone with frequency components of 512Hz and 540 Hz with a shift rate of approximately 16 Hz and deliver at least 25mW to an 8Ω speaker through a 2000Ω:8Ω transformer. If "manual" mode is used, a potentiometer may be inserted in series with the transformer primary to provide volume control. If "automatic" mode is used, resistors R_L and R_M can be chosen to provide desired amplitude sequencing. Typically, signal power

will be down 20 log $\frac{R_{LOAD}}{R_L + R_{LOAD}}$ dB during the

first ring, and down 20 log $\frac{R_{LOAD}}{R_M + R_{LOAD}}$ dB during the

Figure 3-A. Simulation of the Telephone Bell in Non-Telephone Applications

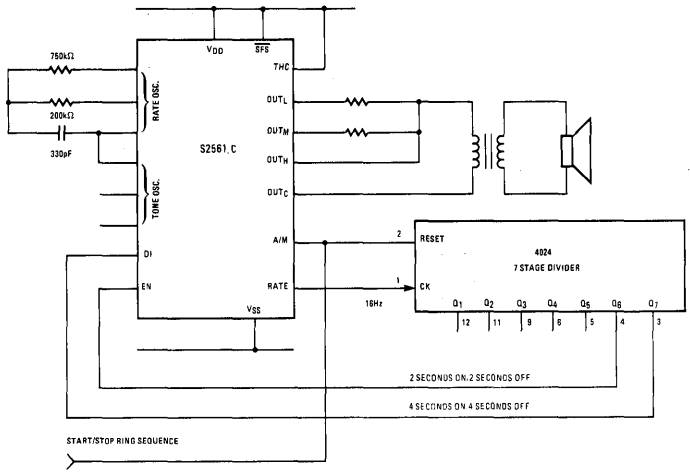
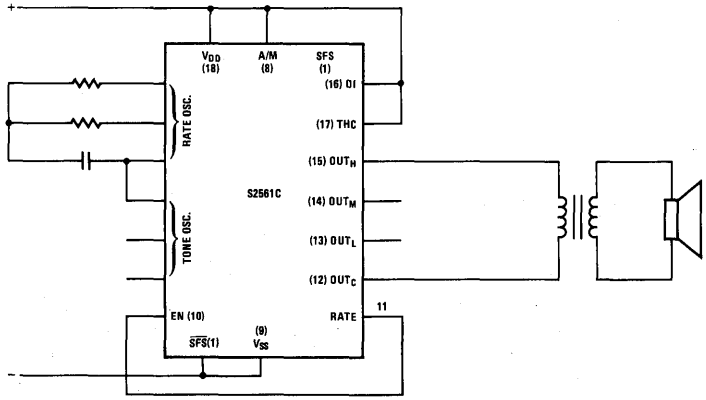


Figure 3-B. Single Frequency Tone Application in Alarms, Buzzers, Etc.



second ring with maximum power delivered to the load beginning the third and consecutive rings.

In applications where dial pulse rejection is not necessary, such as in DTMF telephone systems, the ENABLE pin may be connected directly to V_{DD}. Det. Inh pin must be connected to V_{DD} to allow DC level enabling of the ringer.

Non-Telephone Applications: The configuration shown in Figure 3-A may be used in non-telephone applications where it is desired to simulate the telephone bell.

The internal threshold is bypassed by wiring THC to V_{DD}. The rate output (16Hz) is divided down by a 7-stage divider type 4024 to produce two signals: a 2 second on/2 second off signal and a 4 second on/4 second off signal. The first signal is connected to the EN pin and the second to the DI pin to produce a 2 second on/4 second off telephone-type ring signal. The ring sequence is initiated by removing the reset on the divider. If "auto" mode is used, a reset signal must be applied to the "amplitude sequencing" counter at the end of a ring sequence so that the circuit will respond correctly to a new ring sequence. This is done by temporarily connecting the "auto/manual" input to V_{SS}.

Figure 3-B shows a typical application for alarms, buzzers, etc. Single frequency mode is used by connecting the $\overline{SFS}$ input to V_{SS}. A suitable on/off rate can be determined by using the 7-stage divider circuit. If tinuous tone is not desired, the 16Hz output can be used to gate the tone on and off by wiring it into the ENABLE input.

Many other configurations are possible depending upon the user's specific application.

Reference 1. Bell system communications technical reference:

PUB 47001 of August 1976.
"Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment"—2.6.1 and 2.6.3

AMI

A Subsidiary of Gould Inc.

S2563A

REPERTORY DIALER

Features

- ☐ Specifically Designed for Telephone Line Powered Applications
- ☐ CMOS Process Achieves Low Power Operation
- ☐ 8 or 16 Digit Number Capability (Pin Programmable)
- ☐ Dial Pulse and Mute Output
- ☐ Tone Outputs Obtained by Interfacing With Standard AMI S2859 Tone Generator
- ☐ Two Selections of Dial Pulse Rate
- ☐ Two Selections of Inter-Digit Pause
- ☐ Two Selections of Mark/Space Ratio
- ☐ Memory Storage of 29 8-Digit Numbers or 16-Digit Numbers with Standard AMI S5101 RAM
- ☐ 16-Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Accepts the Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboards; Also Capable of Logic Interface
- ☐ Can Use Standard 3×4 or 4×4 Keyboards
- ☐ Inexpensive, but Accurate R-C Oscillator Design
- ☐ BCD Output with Update for Single Digit Display

General Description

The S2563A is an improved version of the S2562 repertory dialer and can replace the S2562 in existing applications using local power. It is however specifically designed for applications that will only use telephone line power. To achieve this following changes were made to the S2562 design.

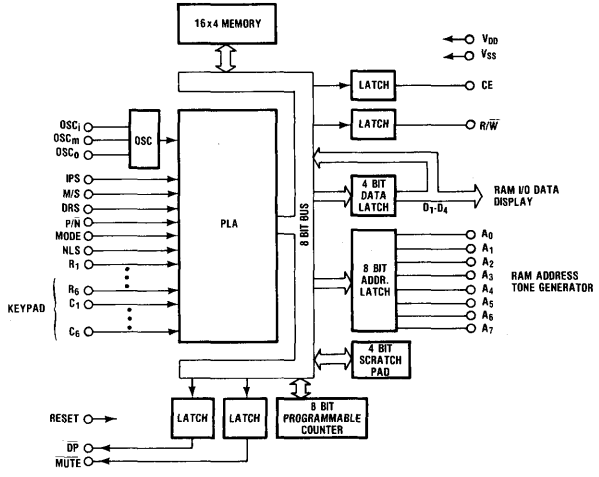
a. $\overline{PF}$ output was replaced by a level reset input which allows the device to be totally powered down in the on-hook state of the telephone.

b. To reduce power consumption in the associated S5101 memory in the standby mode, the interface was changed so that its CE_2 input rather than the the $\overline{CE_1}$ input is controlled by the device.

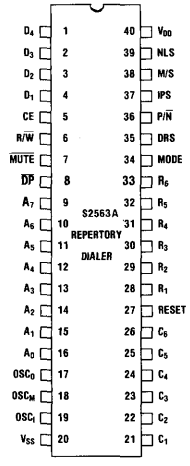
c. Process was changed to a lower voltage CMOS process. Additionally a mark/space selection input (M/S) was added to allow selection of either 40/60 or 33/67 ratio. Provision was also made to allow the device to work with a standard 3×4 or 4×4 keyboard.

Data subject to change at any time without notice. These sheets transferred for information only.

Block Diagram



Pin Configuration



AMI®

A Subsidiary of Gould Inc.

Advanced Product Description **S2569/S2569A**

DTMF TONE GENERATOR WITH REDIAL

Features

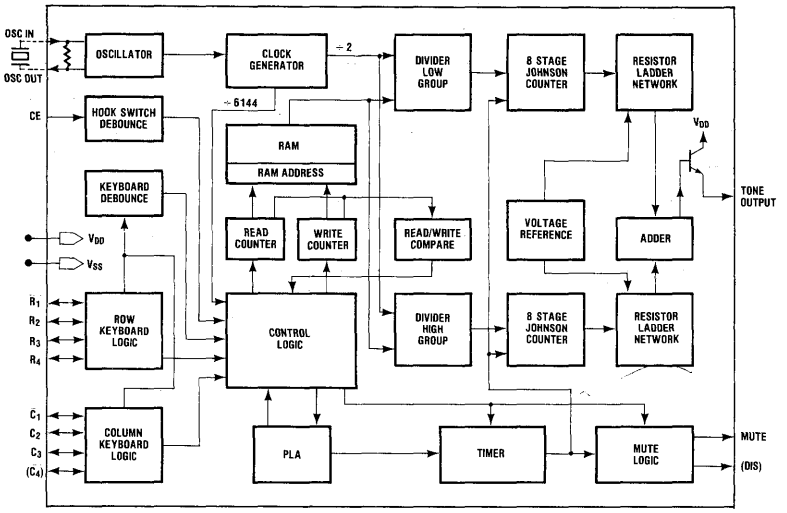
- ☐ Wide Operating Supply Voltage Range (2.50-10V)
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines
- ☐ 21 Digit Memory for Redial
- ☐ Uses Standard 3x4 (S2569A) or 4x4 (S2569) SPST or X-Y Matrix Keyboard
- ☐ The Total Harmonic Distortion is Below Industry Specification (Max. 7% Over Typical Loop Current Range)
- ☐ Separate Control Keys (S2569) for Disconnect, Pause, Redial and Flash in Column Four
- ☐ Allows Dialing of * and # Keys on S2569. For S2569A Redial Initiated by * or # Key as First Key Offhook, * or # can be Dialed After First Key Offhook.

General Description

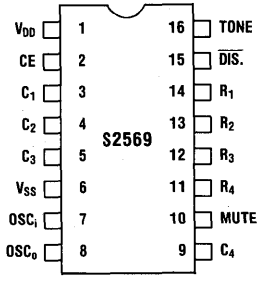
The S2569/S2569A are members of the S2559 Tone Generator family with the added features of Redial, Disconnect, Pause and Flash. They produces the 12 dual tones corresponding to the 12 keys located on the conventional Touch-Tone® telephone keypad. The S2569 has separate keys, located in column four, which initiate the Disconnect(D), Pause(P), Redial(R), and Flash(F) functions. (Note: column four keys do not generate tones.) Only the redial feature is available on the S2569A. Redial on the S2569A is initiated by pressing * or # as the first key offhook.

A voltage reference generated on the chip regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

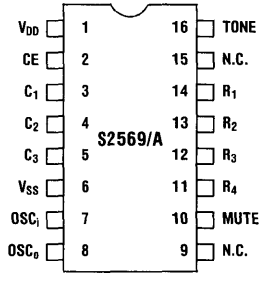
Block Diagram



S2569 Pin Configuration



S2569/A Pin Configuration



Touch-Tone is a registered trademark of AT&T

Absolute Maximum Rating:

DC Supply Voltage (V_{DD}-V_{SS})	+13.5V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +140°C
Power Dissipation at 25°C	500mW
Input Voltage	$V_{SS} - 0.6 < V_{IN} < V_{DD} + 0.6V$

S2569A Electrical Characteristics: Specifications apply over the operating temperature range of 0°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.

Symbol	Parameter/Conditions	($V_{DD} - V_{SS}$) Volts	Min.	Max.	Unit
	Supply Voltage				
V_{DD}	Tone Out Mode (Valid Key Depressed)		2.50	10.0	V
	Non Tone Out Mode (No Key Depressed)		1.50	10.0	V
V_{DR}	Data Retention Voltage		1.0		V
	Supply Current				
I_{DD}	STANDBY (NO Key Depressed, Tone, Mute and Flash Outputs Unloaded, CE = low	2.00 5.00		1 20	μA μA
	Operating (One Key Selected, Tone, Mute and Flash Outputs Unloaded).	3.00		2.5	mA
	Operating During Flash	3.0		300	μA
	Tone Output				
V_{OR}	Low Group Frequency Voltage (R_L = 390kΩ)	5.0	330	690	mVrms
dBcr	Ratio Of Column To Row Tone	2.5–5.0	1.0	3.0	dB
% DIS	Distortion*	2.5–10.0		7	%
	Mute and Flash Outputs				
I_{OH}	Output Source Current V_{OH} = 2.7V	3.0	1.0		mA
I_{OL}	Output Sink Current V_{OL} = 0.3V	3.0	1.0		mA

* Distortion measured in accordance with the specifications described as "ratio of total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair"

NOTE: R_L = load resistor connected from output to V_{SS}.

Basic Chip Operation

The dual tone signal consists of linear addition of two voice frequency signals. One of four signals is selected from a group of frequencies called "low group" and the other is selected from a group of frequencies called "high group". The low group consists of four frequencies; 697, 770, 852 and 941 Hz. The high group consists of three frequencies; 1209, 1336 and 1477 Hz.

When a push button corresponding to a digit (0 thru 9, *, #) is pushed, one appropriate row (R_1 thru R_4) and one appropriate column (C_1 thru C_3) is selected. The active row input selects one of the low group frequencies and active column input selects one of the high group frequencies.

Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide-by-16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function. This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P (V_{DD}-V_{REF}) of the stairstep function is fairly constant. V_{REF} is chosen so that V_P falls within the allowed range of the high group and low group tones.

Normal Dialing

Tone dialing starts as soon as the first digit is entered and debounced. The entered digits are stored sequentially in the internal memory. Pauses may be entered when required in the dial sequence by pressing the "P" key, which provides access pause for future redial. Any number of access pauses may be entered as long as the total entries do not exceed the total number of available digits. Numbers up to 21 digits can be redialed. Numbers exceeding 21 digits will clear redial buffer. Note that only the S2569 has "Pause" capability and the access pause is included in the 21 digit maximum number.

Redial

The last number dialed is retained in the memory and therefore can be redialed by going off hook and pressing the "R" key on the S2569 (located at column 4 and row 3). The S2569A does not use column four and Redial is initiated by "#" or "*" key as the first key off-hook. Tone dialing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the tone dialing output will stop and will resume only after the user pushes any key except Flash and Disconnect keys. During redial all keys are ignored until 70ms after the last digit is dialed (except Disconnect). (Note that the "Pause" function is not available on the S2569A.)

Disconnect/Flash Functions

The S2569 has a push-pull buffer for Disconnect output. With no keys depressed the Disconnect output is high. When the Disconnect key is depressed the Disconnect output goes low until the key is released. Disconnect output can also be used to implement a "Flash" function. When the Flash key is depressed the Disconnect output goes low for 608ms.

Figure 1

1	2	3	D
4	5	6	P
7	8	9	R
*	0	#	F

S2569 Keypad

1	2	3
4	5	6
7	8	9
*	0	#

S2569A Keypad

Keyboard Interface

The S2569/A employs a scanning circuitry to determine key closures. When no key is depressed active pull down resistors are on on the row inputs and active pull up resistors are on on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull up or pull down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The value of pull down and pull up resistors will vary with supply voltage. Typical values of pull up and pull down resistors are shown in Table 1.

Table 1. Typical Resistance Values

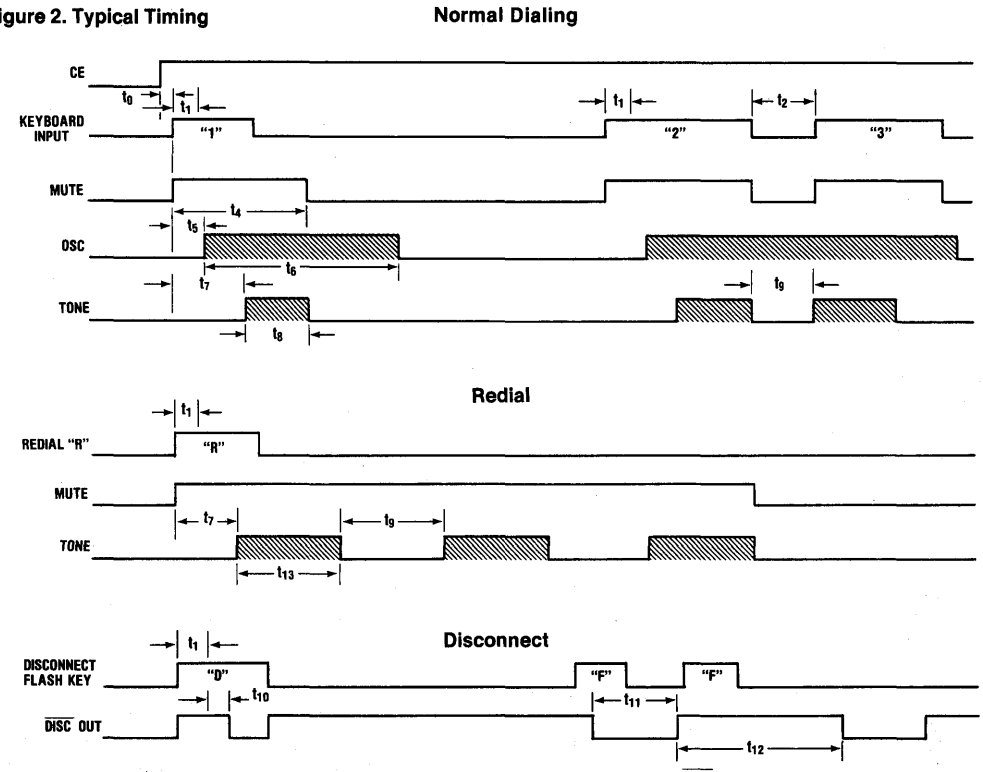
V_{DD}	PULL UP RESISTANCE (TYP.)
2.0V	3.3 K ohm
5.0V	1.5 K ohm
10.0V	1.3 K ohm
V_{DD}	**PULL DOWN RESISTANCE (TYP.)**
2.0V	340 K ohm
5.0V	36.6 K ohm
10.0V	16.6 K ohm

Table 2. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2569/A

ACTIVE INPUT	OUTPUT FREQUENCY HZ SPECIFIED	ACTUAL	% ERROR
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1339	1331.7	−0.32
C3	1477	1471.9	−0.35

NOTE: % error does not include oscillator drift.

Figure 2. Typical Timing



t_0 : OFF HOOK TO KEYBOARD INPUT DELAY TIME:0ms
t_1 : DEBOUNCE TIME:18ms
t_2 : KEY RELEASE TIME:6ms
t_4 : MIN. MUTE PULSE WIDTH:73ms
t_5 : OSC START UP:3ms
t_6 : OSC MIN. ON TIME:142ms
t_7 : TONE OUTPUT DELAY TIME:21ms
t_8 : MIN. TONE OUT TIME:70ms
t_9 : MIN. OFF TIME:70ms
t_{10} : $\overline{\text{DISC}}$ DELAY TIME:4ms
t_{11} : MAX. OUTPUT PULSE:608ms
t_{12} : MIN. DISC OFF TIME:50ms
t_{13} : TONE ON TIME:70ms

Logic Interface

The S2569/A can also interface with CMOS logic outputs directly. The S2569/A requires active high logic levels. Since the pull up resistors present in the S2569/A are fairly low values, diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their low logic state.

Figure 3a. Typical Application Circuit for Line Powered DTMF Dialer With Redial S2569

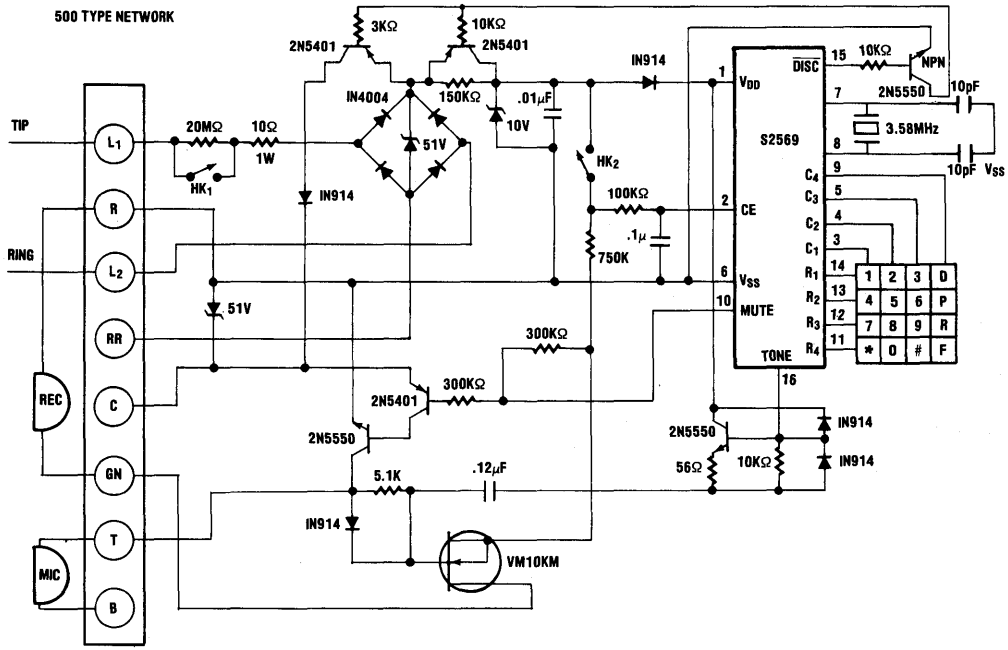
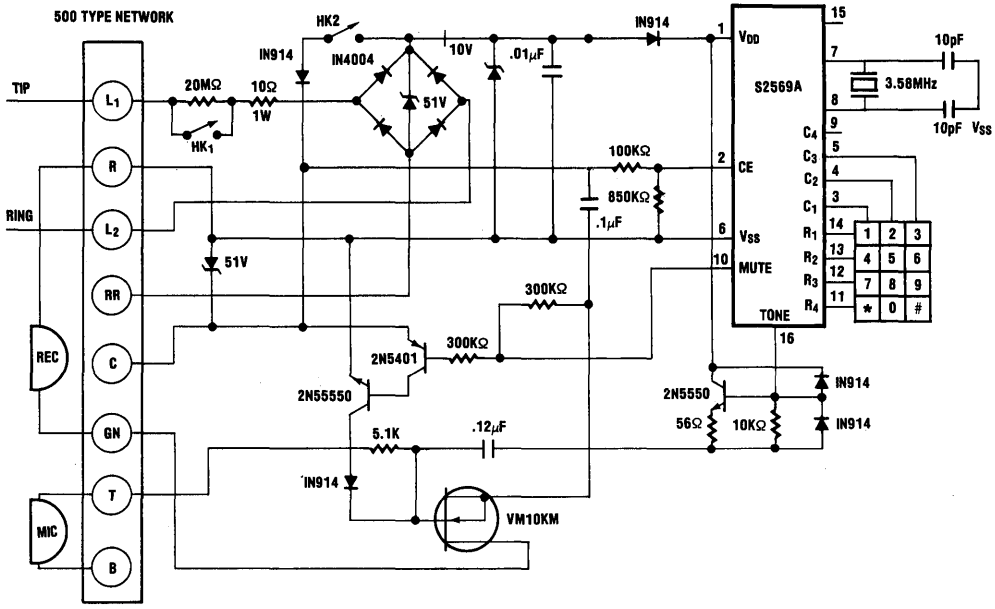


Figure 3b. Typical Application Circuit for Line Powered DTMF Dialer With Redial S2569A



Chip Enable

The S2569/A has a Chip Enable input at pin 2. The Chip Enable for the S2569/A is an active "high". When the Chip Enable is "low", the Tone output goes to V_{SS}, the oscillator is inhibited and the Mute and Disconnect outputs will go into a low state.

Mute Output

The S2569/A has a push-pull buffer for Mute output. With no keys depressed the Mute output is low, when a key is depressed the Mute output goes high until the key is released. Note that minimum mute pulse width is 70ms.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor (1MΩ) on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_i and OSC_o terminals to implement the oscillator function.

Oscillator Crystal Specifications

Frequency 3.579545MHz ± .02%, Rs<100Ω,
Lm = 96Mhy, Cm = .02pF Ch = 5pF

Test Mode

The S2569/A will enter the test mode if all rows are pulled high momentarily. 16 times the low group frequency will appear at mute output depending on which row is selected. Also, 16 times the high group frequency will appear at disconnect output depending upon which column is selected.

AMI

A Subsidiary of Gould Inc.

Advanced Product Description **S2569B/C**

DTMF TONE GENERATOR WITH REDIAL

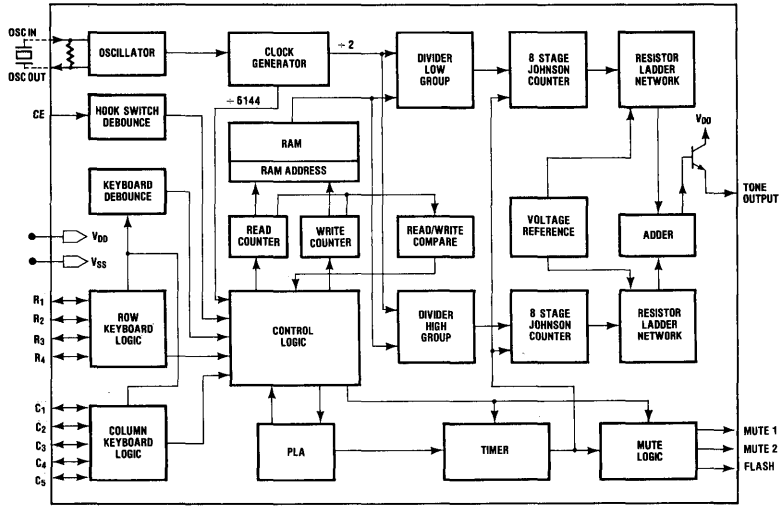
Features

- ☐ Wide Operating Supply Voltage Range (2.50–10V)
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines
- ☐ 21 Digit Memory for Redial
- ☐ Uses 4x5 SPST or X-Y Matrix Keyboard
- ☐ The Total Harmonic Distortion is Below Industry Specification (Max. 7% Over Typical Loop Current Range)
- ☐ Separate Control Keys for Flash and Redial
- ☐ Allows Dialing of *, # and A Through D Keys

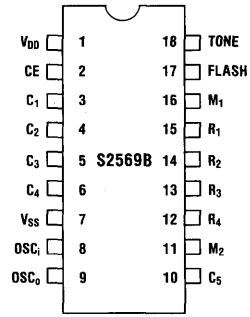
General Description

The S2569B and S2569C are members of the S2559 Tone Generator family with the added features of Redial and Flash. The devices produce 16 dual tones corresponding to the 16-digit keys located on the conventional Touch-Tone® telephone keypad. Function keys for Redial(R) and Flash(F) are located in column five. A voltage reference generated on the chip regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. The S2569B and S2569C versions differ in the duration of the flash output.

Block Diagram



Pin Configuration



Absolute Maximum Rating:

DC Supply Voltage (V_{DD}-V_{SS})	8.0V
Operating Temperature, 2569B	−25°C to +70°C
Operating Temperature, 2569C	0°C to +70°C
Storage Temperature	−65°C to +140°C
Power Dissipation at 25°C	500mW
Input Voltage	$-0.6<V_{IN}<V_{DD}+0.6V$

S2569B/C Electrical Characteristics: (Specifications apply over the operating temperature range of 0°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions	($V_{DD}-V_{SS}$) Volts	Min.	Max.	Unit
	Supply Voltage				
V_{DD}	Tone Out Mode (Valid Key Depressed)		2.50	5.0	V
	Non Tone Out Mode (No Key Depressed)		1.50	5.0	V
	Supply Current				
I_{DD}	STANDBY (NO Key Depressed, Tone, Mute and Flash Outputs Unloaded, CE = low	2.00 5.00		1 20	μA μA
	Operating (One Key Selected, Tone, Mute and Flash Outputs Unloaded).	3.00		2.5	mA
	Operating During Flash	3.0		300	μA
	Tone Output				
V_{OR}	Low Group Frequency Voltage (R_L = 1kΩ)	3.0	246	310	mVrms
dBcr	Ratio Of Column To Row Tone: 2569B 2569C	2.5-5.0 2.5-5.0	2.4 1.0	3.0 3.0	dB dB
% DIS	Distortion*	2.5-10.0		7	%
	Mute and Flash Outputs				
I_{OH}	Output Source Current V_{OH} = 2.7V	3.0	1.0		mA
I_{OL}	Output Sink Current V_{OL} = 0.3V	3.0	1.0		mA

* Distortion measured in accordance with the specifications described as "ratio of total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

NOTE: R_L = load resistor connected from output to V_{SS}.

Basic Chip Operation

The dual tone signal consists of linear addition of two voice frequency signals. One of two signals is selected from a group of frequencies called "low group" and the other is selected from a group of frequencies called "high group". The low group consists of four frequencies; 697, 770, 852 and 941 Hz. The high group consists of four frequencies; 1209, 1336, 1477 and 1633 Hz.

When a push button corresponding to a digit (0 thru D, *, #) is pushed, one appropriate row (R_1 thru R_4) and one appropriate column (C_1 thru C_4) is selected. The active row input selects one of the low group frequencies and active column input selects one of the high group frequencies.

Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide-by-16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function. This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD}-V_{REF}$) of the stair-step function is fairly constant. V_{REF} is chosen so that V_P falls within the allowed range of the high group and low group tones.

Normal Dialing

Tone dialing starts as soon as the first digit is entered and debounced. The entered digits are stored sequentially in the internal memory. Numbers up to 21 digits can be redialed. Numbers exceeding 21 digits will clear redial buffer. Note that the S2569B/C will not accept roll over entries.

Redial

The last number dialed is retained in the memory and therefore can be redialed by going offhook and pressing the "R" key (located at column 5 and row 3). Tone dialing will start when the key is depressed and finish after the entire number is dialed out.

If the redial key is held down, tone dialing will stop after the first digit is dialed, and will resume again when the key is released. This provides for single digit access codes. During Redial the S2569B/C will ignore any keyboard entry. Keys will be accepted 70ms after last number is dialed.

Redial Inhibit

Redial can be inhibited by dialing (*), (#), and Flash, in normal dialing sequence. Numbers exceeding 21 digits and single tones will also inhibit redial.

Flash Output

The S2569B/C has a push-pull buffer for Flash output. With no keys depressed the Flash output is low. When the Flash key is depressed, the Flash output goes high for 90ms (S2569B) or 608ms (S2569C).

Keyboard Interface

The S2569B employs a scanning circuitry to determine key closures. The active pull up or pull down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The values of pull down and pull up resistors will vary with supply voltage. Typical values of pull up and pull down resistors are shown in Table 1.

Table 1. Typical Resistance Values

V_{DD}	PULL UP RESISTANCE (TYP.)
2.0V	3.3 K ohm
5.0V	1.5 K ohm
V_{DD}	**PULL DOWN RESISTANCE (TYP.)**
2.0V	340 K ohm
5.0V	36.6 K ohm

Table 2. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2569B/C

ACTIVE INPUT	OUTPUT FREQUENCY HZ SPECIFIED	ACTUAL	% ERROR
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1339	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

NOTE: % error does not include oscillator drift.

Figure 1. Standard Telephone Push Button Keyboard

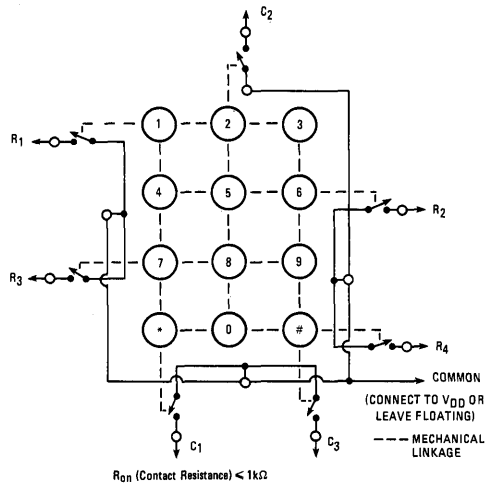
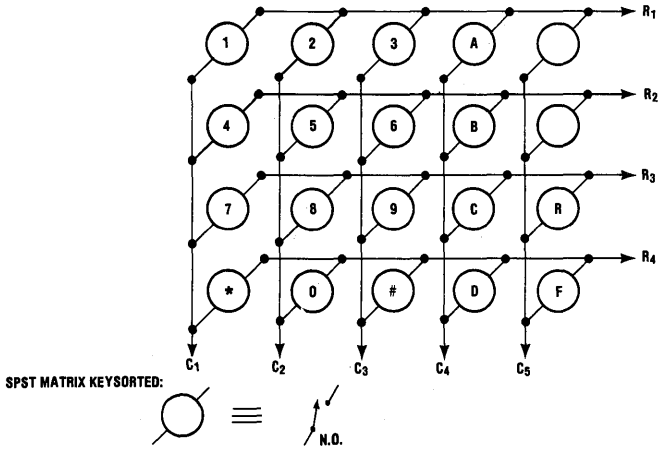


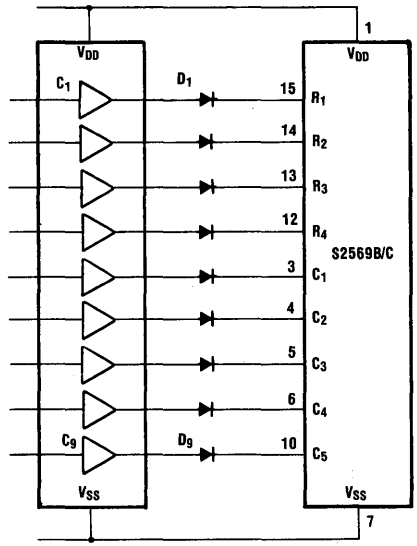
Figure 2. SPST Matrix Keyboard Arranged in the 2 of 8 Row, Column Format



Logic Interface

The S2569B can also interface with CMOS logic outputs directly. The S2569B/C requires active high logic levels. Since the pull up resistors present in the S2569B/C are fairly low values, diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their low logic state.

Figure 3. Logic Interface for Keyboard Inputs of the S2569B



G_1 THRU G_9 ANY TYPE CMOS GATE
D_1 THRU D_9 DIODES TYPE IN914 (OPTIONAL)

Chip Enable

The S2569B/C has a Chip Enable input at pin 2. The Chip Enable for the S2569B/C is an active "high". When the Chip Enable is "low", the tone output goes to V_{SS}, the oscillator is inhibited and the Mute and Disconnect outputs will go into a low state.

Mute Outputs (M1, M2)

The S2569B/C has push-pull buffers for Mute outputs. With no keys depressed the Mute outputs are low. When a key is depressed the outputs go high until the key is released. M1 will stay high for additional 250ms. Note that minimum mute pulse width is 70ms for M2 and 320ms for M1.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor (1MΩ) on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_i and OSC_o terminals to implement the oscillator function.

Oscillator Crystal Specifications

Frequency 3.579545MHz + .02% Rs<100 ohm, LM = 96 Mhy, Cm = .02pF Ch = 5pF.

Single Tone Mode

The S2569B/C is capable of dialing single as well as dual tones. Single tones in either the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column.

Note that two keys have to be depressed simultaneously or the output will be the normal dual tones. If the keys are depressed within 10msec of each other, the single tone will be generated. If not, the standard dual tone representing the first key depressed will be sent and the second button will be ignored.

Test Mode

The S2569B/C will enter the test mode if all rows are pulled high momentarily. 16 times the low group frequency will appear at the M2 output depending on which row is selected. Also 16 times high group frequency will appear at the Flash output depending on which column is selected.

Figure 4. Stairstep Waveform of the Digitally Synthesized Sinewave

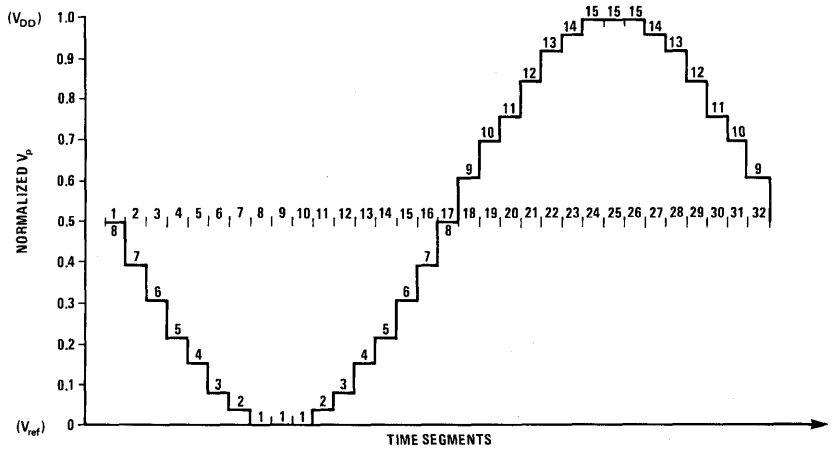
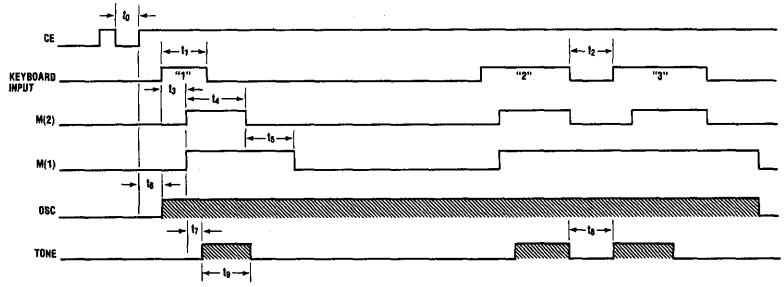
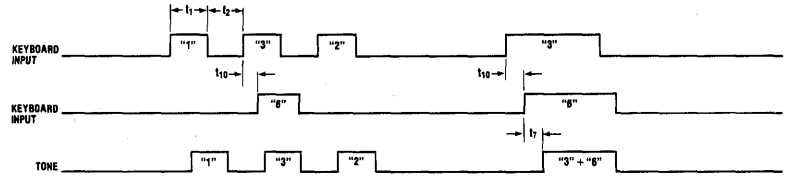


Figure 5. Typical Timing

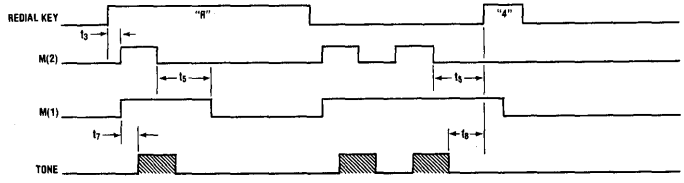
Normal Dialing



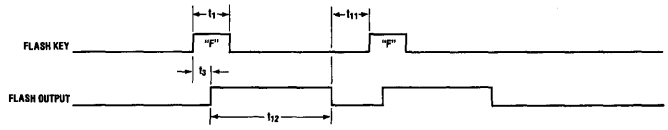


t_0 : MIN RESET TIME:12ms
t_1 : DEBOUNCE TIME:15ms
t_2 : KEY RELEASE TIME:6ms
t_3 : MUTE DELAY TIME:18ms
t_4 : MIN. MUTE PULSE WIDTH:70ms
t_5 : OSC START UP TIME:10ms
t_6 : M(1) TURN OFF TIME:250ms
t_7 : TONE DELAY TIME:3ms
t_8 : MIN. TONE OUT:70ms
t_9 : TONE OFF TIME:70ms
t_{10} : MAX. DELAY TIME:10ms

Redial

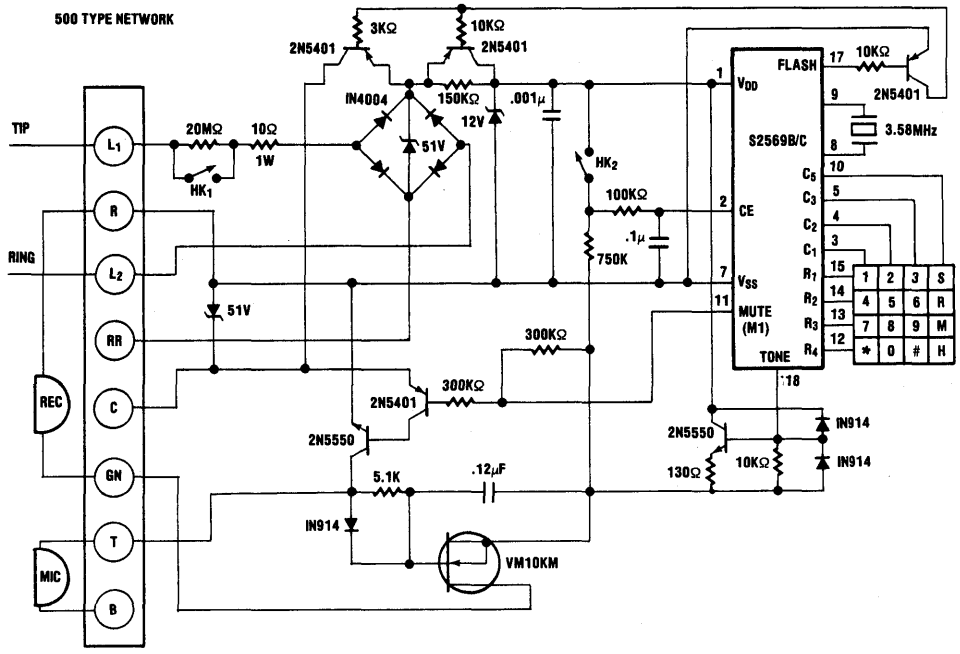


Flash



t_{11} : MIN TIME TO ENTER KEY:50ms
t_{12} : FLASH PULSE WIDTH:90ms (S2569B) OR 608ms (S2569C)

Figure 7. Typical Applications Circuit for Line Powered DTMF Dialer With Redial



AMI

A Subsidiary of Gould Inc.

S25089

DTMF TONE GENERATOR

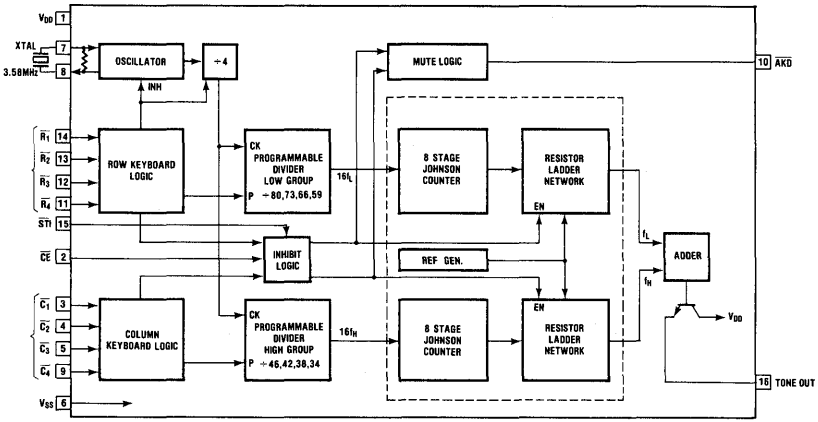
Features

- ☐ Wide Operating Voltage Range: 2.5 to 10 Volts
- ☐ Optimized for Constant Operating Supply Voltages, Typically 3.5V
- ☐ Tone Amplitude Stability is Within ±1.5dB of Nominal Over Operating Temperature Range
- ☐ Low Power CMOS Circuitry Allows Device Power to to be Derived Directly From the Telephone Lines or From Small Batteries
- ☐ Uses TV Crystal Standard (3.58MHz) to Derive All Frequencies Thus Providing Very High Accuracy and Stability
- ☐ Specifically Designed for Electronic Telephone Applications
- ☐ Interfaces Directly to a Standard Telephone Push-Button Keyboard With Common Terminal
- ☐ Low Total Harmonic Distortion
- ☐ Single Tone as Well as Dual Tone Capability
- ☐ Direct Replacement for Mostek MK5089 Tone Generator

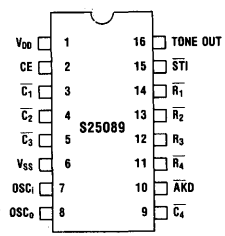
General Description

The S25089 DTMF Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is very stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage (V_{DD}-V_{SS}) ..... +10.5V
Operating Temperature: S25089 ..... −25°C to +70°C
Operating Temperature: S25089-2 ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation at 25°C 500mW
Input Voltage ..... $V_{SS} - 0.6 \leq V_{IN} \leq V_{DD} + 0.6$
Input/Output Current (except tone output) 15mA
Tone Output Current 50mA

Electrical Characteristics: (Specifications apply over the operating temperature range of 0°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			2.5	—	10.0	V
	Non Tone Out Mode ($\overline{AKD}$ Outputs toggle with key depressed)			1.6	—	10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected,		3.0	—	1	20	μA
	Tone and $\overline{AKD}$ Outputs Unloaded)		10.0	—	5	100	μA
	Operating (One Key Selected,		3.0	—	.9	1.25	mA
	Tone and $\overline{AKD}$ Outputs Unloaded)		10.0	—	4.5	10.0	mA
	Tone Output						
V_{OR}	Dual Tone Row Tone	$R_L = 10k\Omega$	3.0	−11.0		−8.0	dBm
	Mode Output Amplitude	$R_L = 100k\Omega$	3.5	−10.0		−7.0	dB
dB_{CR}	Ratio of Column to Row Tone**		2.5-10.0	2.4	2.7	3.0	dB
%DIS	Distortion*		2.5-10.0	–	–	10	%
NKD	Tone Output—No Key Down					−80	dBm
	$\overline{AKD}$ Output						
I_{OL}	Output On Sink Current	$V_{OL} = 0.5V$	3.0	0.5	1.0	—	mA
I_{OH}	Output Off Leakage Current		10.00		1	10	μA
	Oscillator Input/Output						
I_{OL}	One Key Selected	$V_{OL} = 0.5V$	3.0	0.21	0.52	—	mA
	Output Sink Current	$V_{OL} = 0.5V$	10.0	0.80	2.1	—	mA
I_{OH}	Output Source Current	$V_{OH} = 2.5V$	3.0	0.13	0.31	—	mA
	One Key Selected	$V_{OH} = 9.5V$	10.0	0.42	1.1	—	mA
t_{START}	Oscillator Startup Time with Crystal as Specified		3.0-10.0	—	2	5	ms
$C_{I/O}$	Input/Output		3.0	—	12	16	pF
	Capacitance		10.00	—	10	14	pF

*Distortion measured in accordance with the specifications described in REF. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

**S25089-2 available with range of 1.0dB to 3.0dB.
S25088 available with 0dB ratio (column and row amplitude equal).

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		$(V_{DD}-V_{SS})$ Volts	Min.	Typ.	Max.	Units
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		—	V_{SS}		$.2(V_{DD} - V_{SS})$	V
V_{IH}	Input Voltage, High		—	$.8(V_{DD} - V_{SS}$	—	V_{DD}	V
I_{IH}	Input Current	$V_{IH} = 0.0V$	3.0	30	90	150	μA
	(Pull up)	$V_{IH} = 0.0V$	10.0	100	300	500	μA

Oscillator

The S25089 contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_I and OSC_O terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 4 and then drives two sets of programmable dividers, the high group and the low group.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ±0.02%

R_S 100Ω, L_M = 96mH

C_M = 0.02pF C_H = 5pF C_L = 12pF

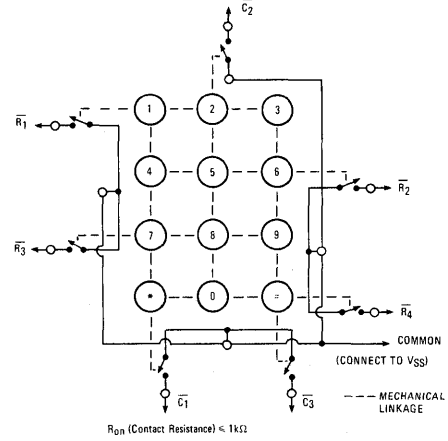
Keyboard Interface

The S25089 can interface with the standard telephone pushbutton keyboard (see Figure 1) with common. The common of the keyboard must be connected to V_{SS}.

Logic Interface

The S25089 can also interface with CMOS logic outputs directly (see Figure 2). The S25089 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 20kΩ-100kΩ.

Figure 1. Standard Telephone Push Button Keyboard



Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divided by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson

counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP (V_{DD}-V_{REF}) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

The individual tones generated by the sinewave synthesizer are then linearly added and drive an NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level. This allows the device to drive varying resistive loads without significant variation in tone amplitude. For example, a load resistor change from 10kΩ to 1kΩ causes a decrease in tone amplitude of less than 1dB.

Dual Tone Mode

When one row and one column is selected, dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys that are not either in the same row or in the same column are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column. This is slightly different from the MK5089 which requires a low to a single column pin to get a column tone.

Inhibiting Single Tones

The $\overline{STI}$ input (pin 15) is used to inhibit the generation of other than dual tones. It has an internal pull down to V_{SS} supply. When this input is left unconnected or connected to V_{SS}, single tone generation as described in the preceding paragraph (Single Tone Mode) is suppressed with all other functions operating normally. When this input is connected to V_{DD} supply, single or dual tones may be generated as previously described (Single Tone Mode, Dual Tone Mode).

Chip Enable Input (CE, Pin 2)

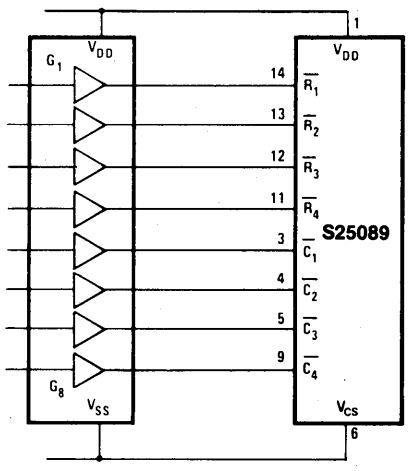
The chip enable input has an internal pull-up to V_{DD} supply. When this pin is left unconnected or connected to V_{DD} supply the chip operates normally. When connected to V_{SS} supply, tone generation is inhibited. All other chip functions operate normally.

Table 1. Comparison of Specified Vs. Actual Tone Frequencies Generated by S25089

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR
	SPECIFIED	ACTUAL	SEE NOTE
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

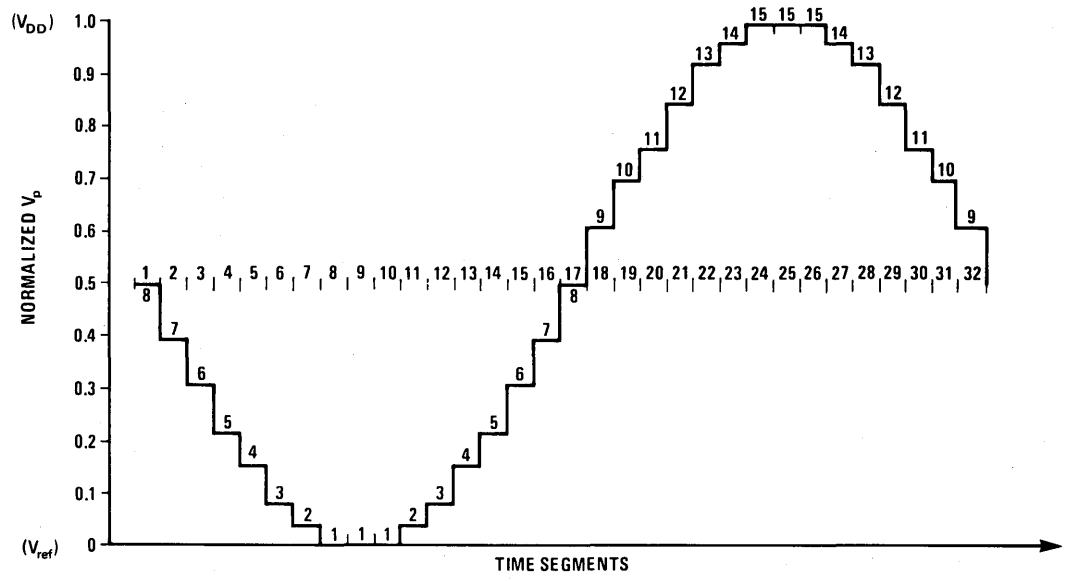
Figure 2. Logic Interface for Keyboard Inputs of the S25089



G1 THRU G8 ANY TYPE CMOS GATE

COMMUNICATION PRODUCTS

Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



Reference Voltage

The structure of the reference voltage employed in the S25089 is shown in Figure 4. It has the following characteristics:

a) V_{REF} is proportional to the supply voltage. Output tone amplitude, which is a function of (V_{DD} - V_{REF}), increases with supply voltage (Figure 5).
b) The temperature coefficient of V_{REF} is low due to a single V_{BE} drop. Use of a resistive divider also provides an accuracy of better than 1%. As a result, tone amplitude variations over temperature and unit to unit are held to less than ± 1.0dB over nominal.
c) Resistor values in the divider network are so chosen that V_{REF} is above the V_{BE} drop of the tone output transistor even at the low end of the supply voltage range. The tone output clipping at low supply voltages is thus eliminated, which improves distortion performance.

$\overline{AKD}$ (Any Key Down or Mute) Output

The $\overline{AKD}$ output (pin 10) consists of an open drain N channel device (see Figure 6.) When no key is depressed the $\overline{AKD}$ output is open. When a key is depressed the $\overline{AKD}$ output goes to V_{SS}. The device is large enough to sink a minimum of 500μA with voltage drop of 0.2V at a supply voltage of 3.5V.

Figure 4. Structure of the Reference Voltage

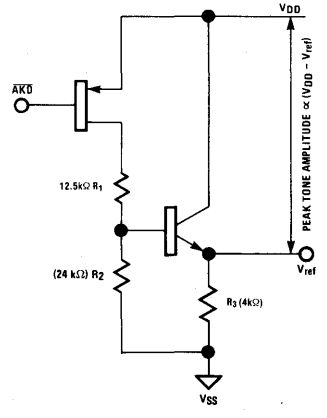


Figure 5. Typical Single Tone Output Amplitude Vs Supply Voltage (R_L = 10k)

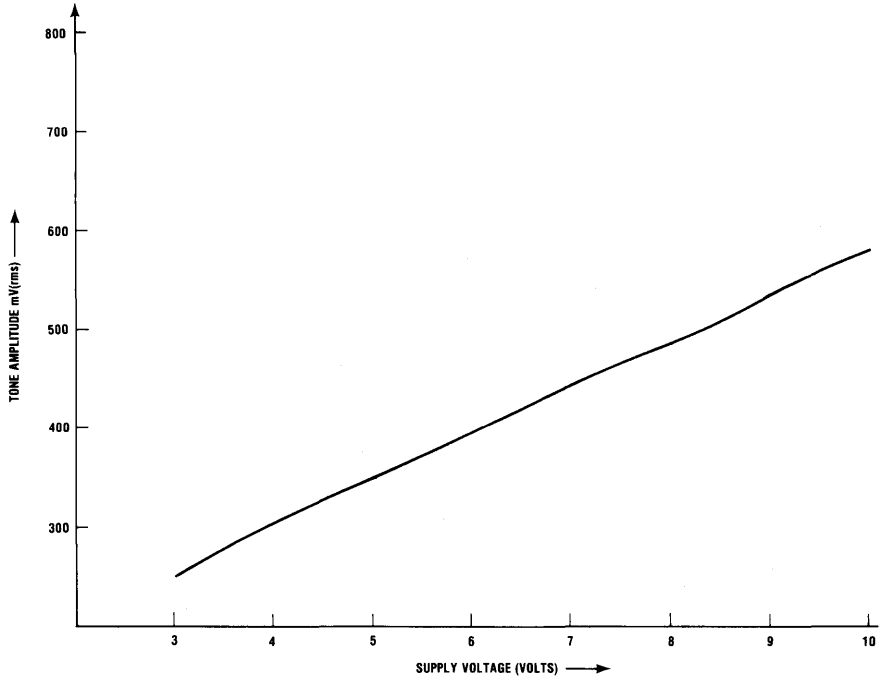
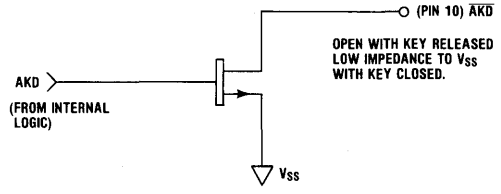


Figure 6. AKD output Structure



AMI

A Subsidiary of Gould Inc.

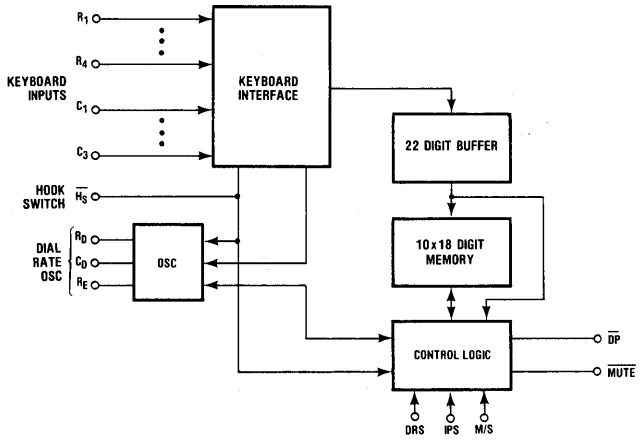
S25610

10 MEMORY PULSE DIALER

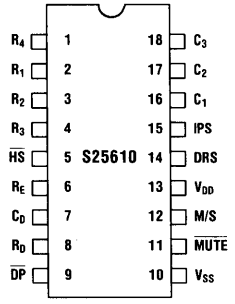
Features

- ☐ Complete Pin Compatibility With S2560A and S2560G Pulse Dialer Allowing Easy Upgrading of Existing Designs.
- ☐ Ten 18-Digit Number Memories Plus Last Number Redial (22 Digit) Memory On Chip.
- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines.
- ☐ Inexpensive R-C Oscillator Design With Accuracy Better Than ±5% Over Temperature and Unit-Unit Variations.
- ☐ Independent Select Inputs for Variation of Dialing Rates (10pps/20pps), Mark/Space Ratio (33⅓-66⅔/40-60), Interdigit Pause (400ms/800ms).
- ☐ Can Interface With Inexpensive XY Matrix or Standard 2 of 7 Keyboard With Common. Also Capable of Logic Interface (Active High).
- ☐ Mute and Pulse Drivers On Chip.
- ☐ Call Disconnect by Pushing * and # Keys Simultaneously.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leq V_{DD} - V_{SS} \leq 3.5V$ unless otherwise specified.

Symbol	Parameter	V_{DD}-V_{SS} (Volts)	Min.	Max.	Units	Conditions
	Operating Voltage					
V_{DD}	Data Retention		1.0		V	On Hook, (HS = V_{DD})
V_{DD}	Non Dialing State		1.5	3.5	V	Off Hook, Oscillator Not Running
V_{DD}	Dialing State		2.0	3.5	V	Off Hook, Oscillator Running
	Operating Current					
I_{DD}	Data Retention	1.0		2.0	μA	On Hook, (HS = V_{DD}) (Note 1)
I_{DD}	Non Dialing	1.5		10	μA	Off Hook (HS = V_{SS}), Oscillator Not Running, Outputs Not Loaded
I_{DD}	Dialing	2.0 3.5		100 500	μA μA	Off Hook, Oscillator Running, Outputs Not Loaded
	Output Current Levels					
I_{OLDP}	DP Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHDP}	DP Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	MUTE Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHM}	MUTE Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
fo	Oscillator Frequency	2.0		10	kHz	
Δfo/fo	Frequency Deviation	2.0 to 2.75 2.75 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50k\Omega \leq R_D \leq 750k\Omega$; $100pF \leq C_D{}^* \leq 1000pF$; $750k\Omega \leq R_E \leq 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD}-V_{SS}$)	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of ($V_{DD}-V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

Note 1: 750nA max. data retention part available. V_{DD} = 1.0 Volt

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

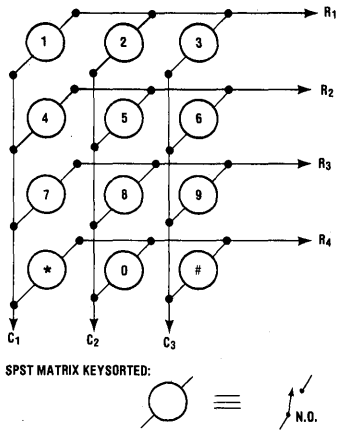
The device contains an oscillator circuit that requires three external components; two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including

the "on hook" condition. For a dialing rate of 10pps the oscillator should be adjusted to 2400Hz. Typical values of external components for this are R_D, R_E = 750kΩ and C_D = 270pF. It is recommended that the tolerance of resistors to be 1% and capacitor to be 5% to insure a ± 10% tolerance of the dialing rate in the system.

Keyboard Interface

The S25610 employs a scanning technique to determine a key closure. This permits interface to a DPCT (Double Pole Common Terminal) keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2),or a XY matrix. A high level on the appropriate row and column inputs constitutes a key closure for logic interface.

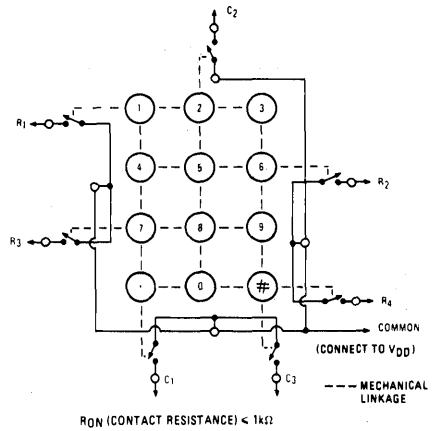
Figure 1. SPST Matrix Keyboard Arranged in a Row, Column Format



On Hook Operation: The device is continuously powered through a 10-20MΩ resistor during the on hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed. DP and mute outputs are low in the on hook state.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

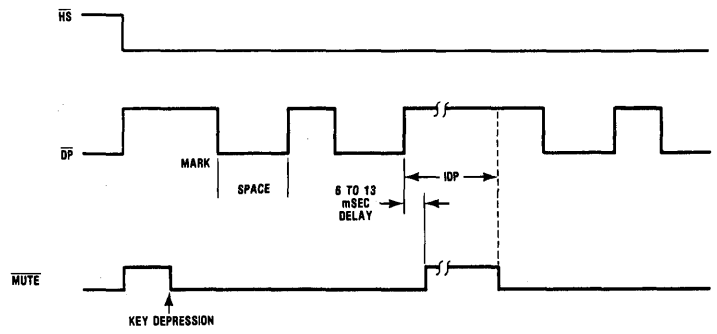
Figure 2. Standard Telephone Pushbutton Keyboard



Off Hook Operations: The device is continuously powered through a 150kΩ resistor during off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The DP output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during this pulse break. The MUTE output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20pps can be achieved. Dialing rates of 7 and 14pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

Figure 3. Timing (Off Hook)



The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14pps, IDP's of 1143ms and 572ms can be similarly obtained. If the IDP select pin is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10pps an IDP of 800ms is obtained and at 20pps an IDP of 400ms is obtained.

The user can enter a number up to 22 digits long from a standard 3 x 4 XY matrix keypad (Figure 1). It is also possible to use a logic interface or a keyboard with common (Figure 2) for number entry. Antibounce protection circuitry is provided on chip (min. 9ms) to prevent false entry.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed 22.

Redialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key twice. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

Memory Dialing

Dialing of a number stored in memory is initiated by going OFF hook and pushing the "#" key followed by the single digit address. Numbers can be cascaded after dialing of the first number is completed.

Table 1. S25610 Pin/Function Descriptions

Pin Functions	Pin Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	7 2, 3, 4, 1, 16, 17, 18	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 2. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 10ms).
Inter-Digit Pause Select (IPS)	15	One programmable line is available that allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 4. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 4.
Dial Rate Select (DRS)	14	A programmable line allows selection of two different output rates such as 7 or 14pps, 10 or 20pps, etc. See Tables 2 and 4.
Mark/Space (M/S)	12	This input allows selection of the mark/space ratio, as per Table 4.
Mute Out ($\overline{MUTE}$)	11	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.
Dial Pulse Out ($\overline{DP}$)	9	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator (R_E, C_D, R_D)	6, 7, 8	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	5	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	13, 10	These are the power supply inputs. The device is designed to operate from 1.5V to 3.5V.

Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)	
					DRS = V_{SS}	DRS = V_{DD}	IPS = V_{SS}	IPS = V_{DD}
5.5/11	1320	Select components in the ranges indicated in table of electrical specifications			5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680				7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920				8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
$(f_d/240)$/ $(f_d/120)$	f_d				$(f_d/240)$	$(f_d/120)$	$\frac{1920}{f_i} \times 10^3$	$\frac{960}{f_i} \times 10^3$

Notes:
1. IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14pps, an IDP of either 1142ms or 571ms can be selected.

Operating Characteristics

Normal Dialing

Off Hook, [D1] , - - - - - - - [Dn]

Dial pulsing to start as soon as first digit is entered (debounced and detected on chip). Pause may be entered in the dialing sequence by pressing the "#" key. Total number of digits entered not to exceed 22. Numbers exceeding 22 digits can be dialed but only after the first 22 digits have been completely dialed out. In this case redialing function is inhibited.

Storing of a Telephone Number(s)

Numbers can be stored as follows:

Off Hook, [*] , [D1] , - - - - [Dn] , [*] , [LOC]
[*] , [D1] , - - - [Dn] , [*] , [LOC]

etc.

Earpiece is muted in this operation to alert the user that a store operation is underway.

Memory Dialing

Off Hook, [#] , [LOC]

Numbers can be cascaded repeating [#] , [LOC] sequence after completion of dialing of present sequence. If an access pause has been stored in "LOC", dialing will halt until the "#" key is pushed again.

Redialing

Last number dialed can be redialed as follows:

Off Hook, [#] , [#]

Last number for this purpose is defined as the last number remaining in the buffer. Access pause is terminated by pushing the "#" key as usual.

Special Sequences

There are some special sequences that provide for mixed dialing or other features such as call disconnect, redial inhibit or memory clear as follows:

a. Normal dialing followed by repertory dialing

Off Hook, [D1] , - - - [Dn] - - - - - [*] , [#] , [LOC]
(wait for dialing to complete before pressing star key)

b. Normal dialing after memory dialing or redialing

Off hook, [#] , [#] - - - - - [D1] - - - [Dn]
or
[LOC]
(wait for dialing to complete before pressing D1 key)

c. Disconnecting call

Off hook, - - - - - , [*] [#]

Pushing * and # keys simultaneously causes DP and mute outputs to go low and remain low until the keys are released. This causes a break in the line. If the keys are held down for a sufficiently long time (approx. 400ms), the call will be disconnected and new dial tone will be heard upon release of the keys. This feature is convenient when disconnecting calls by the normal method, i.e., hanging up the phone or depressing hookswitch is cumbersome.

d. Inhibiting future redialing of a normally dialed number

Off hook, [D1] - - - [Dn] - - - - - [*] , [*]
(wait for dialing to complete before pressing star key)

Pushing * key twice after normal dialing is completed instructs the device to clear the redial buffer.

e. To clear a memory location(s)

Off hook, [*] , [#] , [*] [LOC1] ,- - - [*] , [#] , [*] [LOCn]

Essentially this operation is equivalent to storing a pause in the memory location.

The various operating characteristics are summarized in Table 3.

COMMUNICATION PRODUCTS

Table 3. Summary of Operating Characteristics

1) Normal Dialing: off hook , D1 - - - - - Dn

2) Inhibit Redialing: off hook , D1 - - - Dn - - - - - - - - - - - - * , *
(wait for dialing to complete before pressing star key)

3) Redialing: off hook , # , #

4) Storing of Number(s): off hook , * , D1 , - - - Dn , * LOC1 - - - - - -
- - * , D1 , - - - Dn , * LOCn

5) Memory Dialing: off hook , # LOC1 - - - - - - - - - - - - # , LOCn
(wait for dialing to complete before pressing # key)

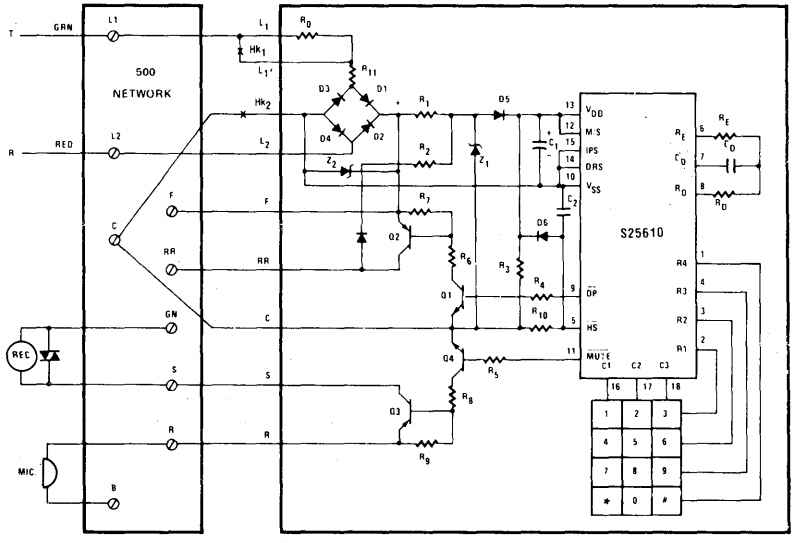
6) Normal Dialing + Memory Dialing: off hook , D1 - - - Dn - - - - - - - - - - - - * , # , LOCn
(wait for dialing to complete before pressing star key)

7) Recall + Normal Dialing: off hook , # , # or LOCn , - - - - - - - - - - - - - D1 - - Dn
(wait for dialing to complete before pressing D1 key)

8) Call Disconnect: off hook , - - - - , * #

9) Clear Memory Location(s): off hook , * , # , * , LOCn - - - * , # , * LOCn

Figure 4. Memory Dialer Circuit with Redial



R_0 = 10-20MΩ, R_1 = 150kΩ, R_2 = 2kΩ
R_3 = 470kΩ, R_4, R_5 = 10kΩ, R_{10} = 47kΩ
R_6, R_8 = 2kΩ, R_7, R_9 = 30kΩ, R_{11} = 20Ω, 2W
Z_1 = 3.9V, D_1—D_4 = IN4004, D_5, D_6, D_7 = IN914, C_1 = 15μF

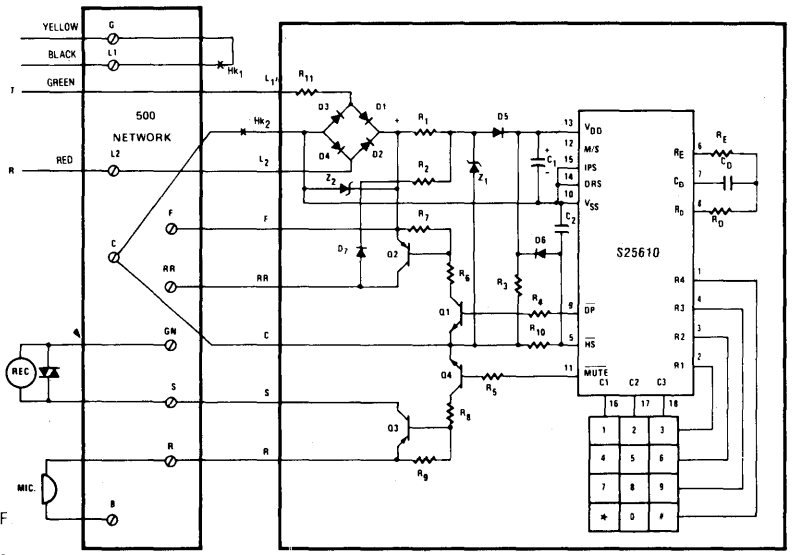
$R_E = R_0$ = 750kΩ, C_D = 270pF, C_2 = 0.01μF
Q_1, Q_4 = 2N5550 TYPE Q_2, Q_3 = 2N5401 TYPE
Z_2 = IN5379 110V ZENER OR 2XIN4758

Table 4.

Function	Pin Designation	Input Logic Level	Selection
Dial Pulse Rate Selection	DRS	V_{SS} V_{DD}	(f/240)pps (f/120)pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	$\frac{960}{f}$ s $\frac{1920}{f}$ s
Mark/Space Ratio	M/S	V_{SS} V_{DD}	33⅓/66⅔ 40/60
On Hook/Off Hook	HS	V_{DD} V_{SS}	On Hook Off Hook

NOTE: f is the oscillator frequency and is detemined as shown in Figure 5.

Figure 5. Memory Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



$R_1 = 10\text{-}20M\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$
$R_{10} = 47k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, $D_1 — D_4 = IN4004$
D_5, D_6, $D_7 = IN914$, $C_1 = 15\mu F$
R_E, $R_D = 750k\Omega$, $C_D = 270pF$
$C_2 = 0.01\mu F$, Q_1, $Q_4 = 2N5550$
Q_2, $Q_3 = 2N5401$
$Z_2 = 150V$ ZENER OR VARISTOR TYPE GE MOV150

A Subsidiary of Gould Inc.

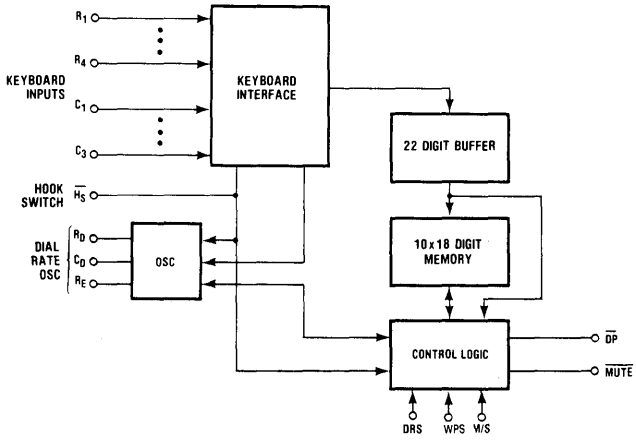
S25610E

10 MEMORY PULSE DIALER

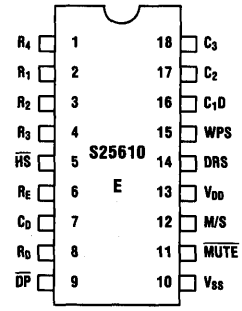
Features

- ☐ Modified Version of the S25610 Repertory Dialer. Optimized for European Applications
- ☐ Ten 18-Digit Number Memories Plus Last Number Redial (22 Digit) Memory On Chip.
- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines.
- ☐ Inexpensive R-C Oscillator Design With Accuracy Better Than ±5% Over Temperature and Unit-Unit Variations.
- ☐ Independent Select Inputs for Variation of Dialing Rates (10pps/20pps), Mark/Space Ratio (33⅓-66⅔/40-60)
- ☐ Can Interface With Inexpensive XY Matrix or Standard 2 of 7 Keyboard With Common. Also Capable of Logic Interface (Active High).
- ☐ Mute and Pulse Drivers On Chip.
- ☐ Call Disconnect by Pushing * and # Keys Simultaneously.
- ☐ Pin Selectable Access Pause/Wait Functions
- ☐ Auto Pause Insertion

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leq V_{DD} - V_{SS} \leq 3.5V$ unless otherwise specified.

Symbol	Parameter	V_{DD}-V_{SS} (Volts)	Min.	Max.	Units	Conditions
	Operating Voltage					
V_{DD}	Data Retention		1.0		V	On Hook, ($\overline{HS} = V_{DD}$)
V_{DD}	Non Dialing State		1.5	3.5	V	Off Hook, Oscillator Not Running
V_{DD}	Dialing State		2.0	3.5	V	Off Hook, Oscillator Running
	Operating Current					
I_{DD}	Data Retention	1.0		750	mA	On Hook, ($\overline{HS} = V_{DD}$)
I_{DD}	Non Dialing	1.5		10	μA	Off Hook ($\overline{HS} = V_{SS}$), Oscillator Not Running, Outputs Not Loaded
I_{DD}	Dialing	2.0 3.5		100 500	μA μA	Off Hook, Oscillator Running, Outputs Not Loaded
	Output Current Levels					
I_{OLDP}	DP Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHDP}	DP Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	MUTE Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHM}	MUTE Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
fo	Oscillator Frequency	2.0		10	kHz	
Δfo/fo	Frequency Deviation	2.0 to 2.75 2.75 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50k\Omega \leq R_D \leq 750k\Omega$; $100pF \leq C_D{}^* \leq 1000pF$; $750k\Omega \leq R_E \leq 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD} - V_{SS}$)	V_{DD} + 0.3	V	
V_{IL}	Logical "0"		V_{SS} − 0.3	20% of ($V_{DD} - V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

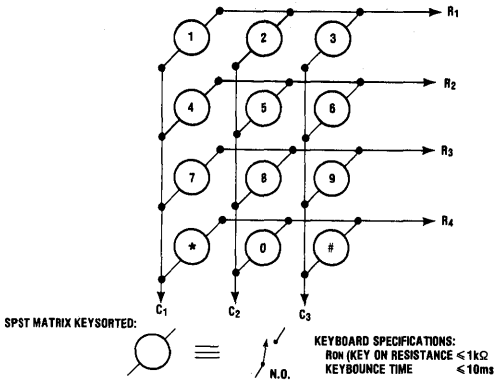
The device contains an oscillator circuit that requires three external components; two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including

the "on hook" condition. For a dialing rate of 10pps the oscillator should be adjusted to 2400Hz. Typical values of external components for this are R_D, R_E = 750kΩ and C_D = 270pF. It is recommended that the tolerance of resistors to be 1% and capacitor to be 5% to insure a ± 10% tolerance of the dialing rate in the system.

Keyboard Interface

The S25610 employs a scanning technique to determine a key closure. This permits interface to a DPCT (Double Pole Common Terminal) keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2),or a XY matrix. A high level on the appropriate row and column inputs constitutes a key closure for logic interface.

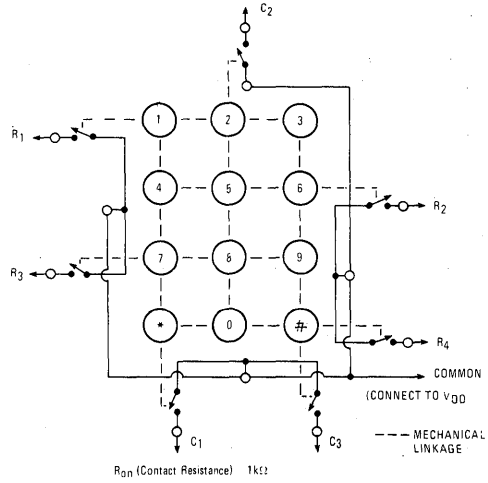
Figure 1. SPST Matrix Keyboard Arranged in a Row, Column Format



On Hook Operation: The device is continuously powered through a 10-20MΩ resistor during the on hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed. DP and mute outputs are low in the on hook state.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

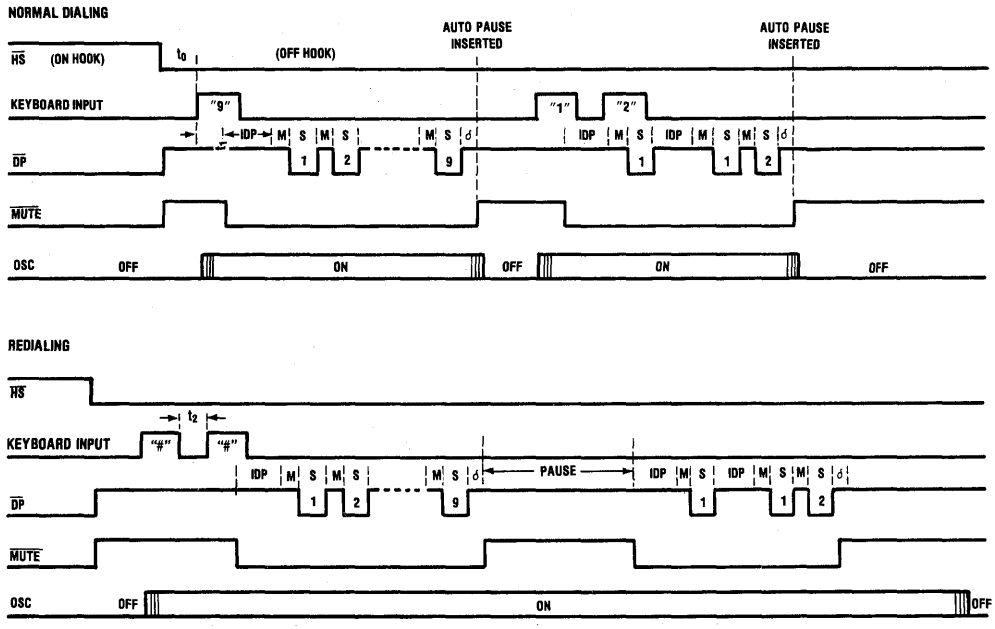
Figure 2. Standard Telephone Pushbutton Keyboard



Off Hook Operations: The device is continuously powered through a 150kΩ resistor during off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The DP output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during this pulse break. The MUTE output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20pps can be achieved. Dialing rates of 7 and 14pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

Figure 3. Timing (Dial, Redial)



t_1 : KEY DEBOUNCE TIME: 10ms
t_2 : KEY RELEASE TIME: 2ms
δ : PULSE TURNOFF TO MUTE TURNOFF DELAY TIME: 200μs
t_0 : OFF HOOK TO KEYBOARD INPUT DELAY TIME: 2ms

NOTE: TYPICAL WAVEFORMS DURING NORMAL DIALING AND REDIALING (ASSUMES PAUSE OPTION IS SELECTED) (TIME BASED ON OSCILLATOR FREQUENCY OF 2400Hz)

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and it is a function of the dialing rate selected by the dial rate select input. If the oscillator is set to 2400Hz so that a dialing rate of 10pps is obtained with DRS = V_{SS}. Then an IDP of 800ms is automatically selected. Switching the dialing rate to 20pps (DRS = V_{DD}) will lower the IDP to 400ms.

The user can enter a number up to 22 digits long from a standard 3 x 4 XY matrix keypad (Figure 1). It is also possible to use a logic interface or a keyboard with common (Figure 2) for number entry. Antibounce protection circuitry is provided on chip (min. 9ms) to prevent false entry.

Table 1. S25610E Pin/Function Descriptions

Pin Functions	Pin Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	2, 3, 4, 1, 16, 17, 18	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 2. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 10ms).
Wait-Pause Select (WPS)	15	This is a Tri-Function input pin. Leaving it open selects the access wait function. Connect to V_{DD} selects access pause duration of 3.2sec. and connection to V_{SS} selects the access pause duration of 6.4sec. For detailed description of wait/pause functions see Operating Characteristics.
Dial Rate Select (DRS)	14	A programmable line allows selection of two different output rates such as 7 or 14pps, 10 or 20pps, etc. See Tables 2 and 4. Interdigit Pause (IDP) is a function of the selected dialing rate.
Mark/Space (M/S)	12	This input allows selection of the mark/space ratio, as per Table 4.
Mute Out ($\overline{MUTE}$)	11	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing. Normally it is "high" and "low" during dialing. It is "low" on hook.
Dial Pulse Out ($\overline{DP}$)	9	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise. On hook it is "low".
Dial Rate Oscillator	6, 7, 8	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	5	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.It is debounced during dialing. An interruption of 150ms or less will be ignored while that excess of 300ms will cause the device to go into standby condition.
Power (V_{DD}, V_{SS})	13, 10	These are the power supply inputs. The device is designed to operate from 1.5V to 3.5V.

Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)
					DRS = V_{SS}	DRS = V_{DD}	
5.5/11	1320	Select components in the ranges indicated in table of electrical specifications			5.5	11	1454 / 727
6/12	1440				6	12	1334 / 667
6.5/13	1560				6.5	13	1230 / 615
7/14	1680				7	14	1142 / 571
7.5/15	1800				7.5	15	1066 / 533
8/16	1920				8	16	1000 / 500
8.5/17	2040				8.5	17	942 / 471
9/18	2160				9	18	888 / 444
9.5/19	2280				9.5	19	842 / 421
10/20	2400	750	750	270	10	20	800 / 400
(f_d/240)/ (f_d/120)	f_d				(f_d/240)	(f_d/120)	$\frac{1920}{f_i}\times10^3$ / $\frac{960}{f_i}\times10^3$

Notes:
1. IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14pps, an IDP of either 1142ms or 571ms can be selected.

Operating Characteristics

Normal Dialing

Off Hook, [D1] , - - - - - - - [Dn]

Dial pulsing to start as soon as first digit is entered and debounced on the chip. Total number of digits entered not to exceed 22. Numbers exceeding 22 digits can be dialed but only after the first 22 digits have been completely dialed out. Access wait or pause can be inserted by pressing the "#" key. Any number of waits or pauses can be entered as long as the total number of digits does not exceed 22. Additionally in the "pause" mode, pause is inserted automatically (two maximum) if no further digits are entered by the time mute turns off. (Figure 3.)

Storing of a Telephone Number(s)

Numbers can be stored as follows:

Off Hook, [*] , [D1] , - - - - [Dn] , [*] , [LOC]

[*] , [D1] , - - - [Dn] , [*] , [LOC]

Access wait/pause can be inserted in the stored sequence by pushing the "#" key. Any number of waits/pauses may be stored as long as the total number of digits does not exceed 22.

Memory Dialing

Off Hook, [#] , [LOC]

Numbers can be cascaded repeating [#] , [LOC] sequence after completion of dialing of present sequence. If an access pause has been stored in "LOC", dialing will halt until the "#" key is pushed again. If an access pulse is detected dialing will stop for the selected duration.

Redialing

Last number dialed can be redialed as follows:

Off Hook, [#] , [#]

Last number for this purpose is defined as the last number remaining in the buffer. Access pause is terminated by pushing the "#" key as usual. If the device is operated in the "pause" mode and if an access pause was automatically inserted during normal dialing, during redialing the dialing will be stopped for the pause duration selected.

Special Sequences

There are some special sequences that provide for mixed dialing or other features such as call disconnect, redial inhibit or memory clear as follows:

a. Normal dialing followed by repertory dialing

Off Hook, [D1] , - - - [Dn] - - - - - [*] , [#] , [LOC]

(wait for dialing to complete before pressing star key)

b. Normal dialing after memory dialing or redialing

Off hook, [#] , [#] - - - - - [D1] - - - [Dn]

or

[LOC]

(wait for dialing to complete before pressing D1 key)

c. Disconnecting call

Off hook, - - - - - , [*] [#]

Pushing * and # keys simultaneously causes DP and mute outputs to go low and remain low until the keys are released. This causes a break in the line. If the keys are held down for a sufficiently long time (approx. 400ms), the call will be disconnected and new dial tone will be heard upon release of the keys. This feature is convenient when disconnecting calls by the normal method, i.e., hanging up the phone or depressing hookswitch is cumbersome.

d. Inhibiting future redialing of a normally dialed number

Off hook, [D1] - - - [Dn] - - - - - [*] , [*]

(wait for dialing to complete before pressing star key)

Pushing * key twice after normal dialing is completed instructs the device to clear the redial buffer.

e. To clear a memory location(s)

Off hook, [*] , [#] , [*] [LOC1] ,- - - [*] , [#] , [*] [LOCn]

Essentially this operation is equivalent to storing a pause in the memory location.

The various operating characteristics are summarized in Table 3.

COMMUNICATION PRODUCTS

Table 3. Summary of Operating Characteristics

1) Normal Dialing: off hook , [*D1] - - - - - [Dn]

2) Inhibit Redialing: off hook , [D1] - - - [Dn] - - - - - - - - - - - [*] , [*]
(wait for dialing to complete before pressing star key)

3) Redialing: off hook , [#] , [#]

4) Storing of Number(s): off hook , [*] , [D1] , - - - [Dn] , [*] [LOC1] - - - - - -
- - [*] , [D1] , - - - [Dn] , [*] [LOCn]

5) Memory Dialing: off hook , [#] [LOC1] - - - - - - - - - - - [#] , [LOCn]
(wait for dialing to complete before pressing # key)

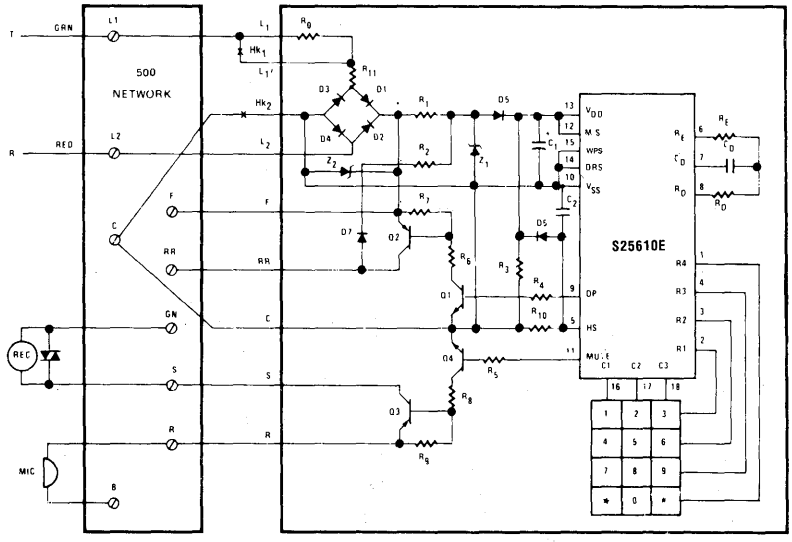
6) Normal Dialing + Memory Dialing: off hook , [D1] - - - [Dn] - - - - - - - - - - - [*] , [#] , [LOCn]
(wait for dialing to complete before pressing star key)

7) Recall + Normal Dialing: off hook , [#] , [#] or [LOCn] , - - - - - - - - - - - - [D1] - - [Dn]
(wait for dialing to complete before pressing D1 key)

8) Call Disconnect: off hook , - - - - , [*] [#]

9) Clear Memory Location(s): off hook , [*] , [#] , [*] , [LOCn] - - - [*] , [#] , [*] [LOCn]

Figure 4. Memory Dialer Circuit with Redial



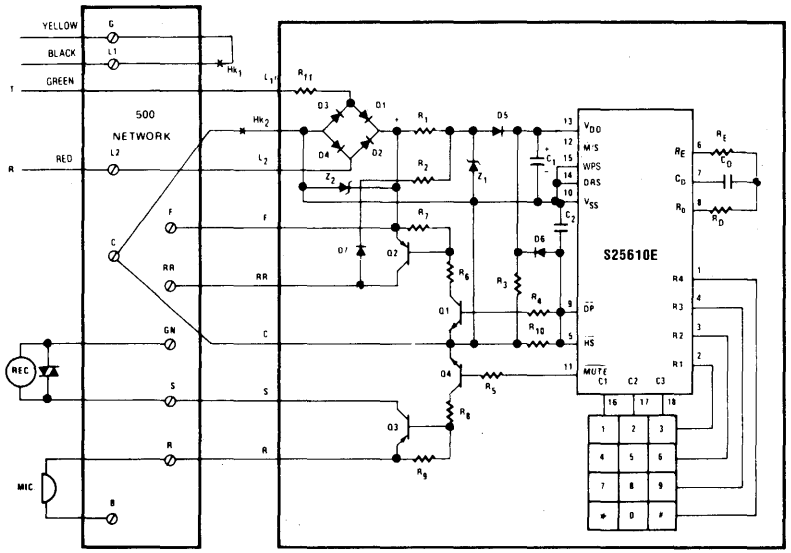
R_0 = 10-20MΩ, R_1 = 150kΩ, R_2 = 2kΩ
R_3 = 470kΩ, R_4, R_5 = 10kΩ, R_{10} = 47kΩ
R_6, R_8 = 2kΩ, R_7, R_9 = 30kΩ, R_{11} = 20Ω, 2W
Z_1 = 3.9V, D_1—D_4 = IN4004, D_5, D_6, D_7 = IN914, C_1 = 15μF

R_E = R_D = 750kΩ, C_D = 270pF, C_2 = 0.01μF
Q_1, Q_4 = 2N5550 TYPE Q_2, Q_3 = 2N5401 TYPE
Z_2 = IN5379 110V ZENER OR 2XIN4758

Table 4.

Function	Pin Designation	Input Logic Level	Selection
Dial Rate Selection and Inter-Digit Pause Selection	DRS	V_{DD}	$\frac{960}{f}$ s IDP (f/120)pps (f/240)pps
		V_{SS}	$\frac{1920}{f}$ s IDP
Mark/Space Ratio	M/S	V_{SS} V_{DD}	33⅓/66⅔ 40/60
On Hook/Off Hook	$\overline{HS}$	V_{DD} V_{SS}	On Hook Off Hook

Figure 5. Memory Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



R_1 = 10-20MΩ, R_2 = 2kΩ
R_3 = 470kΩ, R_4, R_5 = 10kΩ
R_6, R_8 = 2kΩ, R_7, R_9 = 30kΩ
R_{10} = 47kΩ, R_{11} = 20Ω, 2W
Z_1 = 3.9V, D_1—D_4 = IN4004
D_5, D_6, D_7 = IN914, C_1 = 15μF
R_E, R_D = 750kΩ, C_D = 270pF
C_2 = 0.01μF, Q_1, Q_4 = 2N5550
Q_2, Q_3 = 2N5401
Z_2 = 150V ZENER OR VARISTOR TYPE GE MOV150

AMI

A Subsidiary of Gould Inc.

Advanced Product Description **S25910/S25912**

10 MEMORY DTMF DIALER

Features

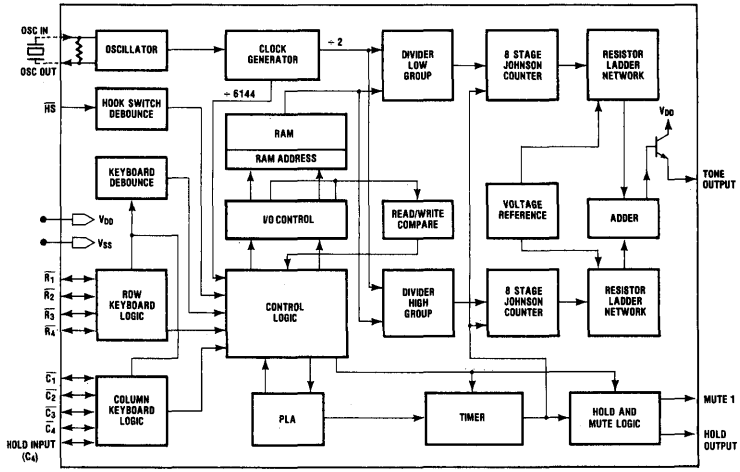
- ☐ Ten 16- Digit Numbers Stored on Chip Plus 16 Digit Redial Buffer
- ☐ Operates with 4x4 Keyboard (S25910) or 3x4 Keyboard (S25912)
- ☐ S25910 Has Separate Keys for Store, Redial, Memory Dial and Hold Functions
- ☐ S25912 uses # and * Keys for Storage and Retrieval of Numbers in Memory
- ☐ Low Data Retention Current: 1μA Max.
- ☐ S25912 Pin Compatible with AMI's S2559 Tone Generator Family
- ☐ Telephone Line Powered Operation

General Description

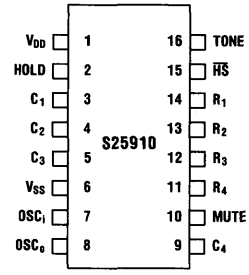
The S25910/S25912 are monolithic CMOS integrated circuits intended for DTMF memory dialer applications. They provide normal DTMF dialing functions and the capability to store and retrieve ten 16-digit numbers, plus last number dialed, from on-chip memory.

The S25910 has separate key inputs to activate store, redial, memory dial, and hold functions. The S25912 interfaces to a 3x4 keyboard and uses the # and * keys for memory storage and retrieval. The low data retention current of 1μA maximum for both the S25910/S25912 eliminate battery backup requirements and allow operation from telephone line power.

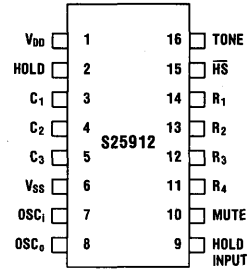
Block Diagram



S25910 Pin Configuration



S25912 Pin Configuration



Absolute Maximum Rating:

DC Supply Voltage (V_{DD}-V_{SS})	+13.5V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +140°C
Power Dissipation at 25°C	500mW
Input Voltage	$-0.6<V_{IN}<V_{DD}+0.6V$

Electrical Characteristics: Specifications apply over the operating temperature range of 0°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.

Symbol	Parameter/Conditions	($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Unit
	Supply Voltage					
V_{DD}	Tone Out Mode (Valid Key Depressed)		2.50		10.0	V
	Non Tone Out Mode (No Key Depressed)		1.50		10.0	V
	Supply Current					
I_{DD}	STANDBY (NO Key Depressed, Tone, Mute and Flash Outputs Unloaded, HS HIGH	1.0 10.0			1 100	μA μA
	Operating (One Key Selected, Tone, Mute Unloaded)	2.5			2.5	mA
	Data Retention	1.0			1	μA
	Tone Output					
V_{OR}	Low Group Frequency Amplitude ($R_L = 1k\Omega$)	3.0		278		mVrms
dBcr	Ratio Of Column To Row Tone	2.5–10.0	1.0		3.0	dB
% DIS	Distortion*	2.5–10.0			7	%
	Mute Output					
I_{OH}	Output Source Current $V_{OH} = 2.25V$	2.5	0.5			mA
I_{OL}	Output Sink Current $V_{OL} = 0.25V$	2.5	0.5			mA

* Distortion measured in accordance with the specifications described as "ratio of total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

NOTE: R_L = load resistor connected from output to V_{SS}.

Functional Description

Basic Chip Operation

The dual tone signal consists of linear addition of two voice frequency signals. One of four signals is selected from a group of frequencies called "low group" and the other is selected from a group of frequencies called "high group". The low group consists of four frequencies; 697, 770, 852 and 941 Hz. The high group consists of three frequencies; 1209, 1336 and 1477 Hz.

When a push button corresponding to a digit (0 thru 9, *, #) is pushed, one appropriate row (R_1 thru R_4) and one appropriate column (C_1 thru C_4) is selected. The active row input selects one of the low group frequencies and active column input selects one of the high group frequencies. In addition to generating DTMF tones, the S25910 has special function push buttons in column 4 which do not generate tones.

Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide-by-16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function. This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P (V_{DD}-V_{REF}) of the stair-step function is fairly constant. V_{REF} is chosen so that V_P falls within the allowed range of the high group and low group tones.

Normal Dialing

Tone dialing starts as soon as the first digit is entered and 10ms debounce is complete. Entered digits are stored sequentially in the internal buffer. Numbers up to 16 digits can be redialed. Numbers exceeding 16 digits will clear the redial buffer and inhibit the memory dialing of these numbers.

Memory Dialing

Dialing a number stored in memory on the S25910 is initiated by going off hook and pushing the "M" button followed by the single digit address. Tone dialing will start after the address key is depressed and debounced by 10ms. Memory dialing sequence is complete after the entire number stored in memory has been dialed. Cascading of numbers is possible with the S25910. Memory dialing with the S25912 is initiaited by going off hook and pressing the "*" key followed by the address location. Cascading of numbers on the S25912 is not possible.

Keyboard Interface

The S25910/S25912 employ a scanning circuitry to determine key closures. When no key is depressed, active pull down resistors are on on the row inputs and active pull up resistors are on on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull up or pull down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The values of pull down and pull up resistors will vary with supply voltage. Typical values of pull up and pull down resistors are shown in Table 1.

Chip Enable ($\overline{HS}$)

The S25910/S25912 have a $\overline{HS}$ input (chip enable) at pin 15. The $\overline{HS}$ pin is an active "low". When the $\overline{HS}$ pin is "high," the tone output goes to V_{SS}, the oscillator is inhibited, keyboard scanning is disconnected, and the mute and hold outputs will go to a low state.

Mute Output

The S25910/S25912 have a push-pull buffer for Mute output. With no keys depressed the Mute output is low, when a key is depressed the Mute output goes high and stays high until the key is released.

Table 1. Typical Resistance Values

V_{DD}	PULL UP RESISTANCE (TYP.)
2.0V	3.3 K ohm
5.0V	1.5 K ohm
10.0V	1.3 K ohm
V_{DD}	**PULL DOWN RESISTANCE (TYP.)**
2.0V	340 K ohm
5.0V	36.6 K ohm
10.0V	16.6 K ohm

Table 2. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S25910/S25912

ACTIVE INPUT	OUTPUT FREQUENCY Hz		% ERROR
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1339	1331.7	−0.32
C3	1477	1471.9	−0.35

NOTE: % error does not include oscillator drift.

Operating Characteristic Symbol Definition

[X] — Indicates pressing digit or feature button to initiate function.

[D1] - - - [Dn] — Digits of stored number.

[R] — Redial button.

[S] — Memory store button.

[Ln] — Memory location storage number (0 through 9).

[M] — Memory recall button.

[H] — Hold button.

Summary of Operations (S25910)

Normal Dialing

Off Hook [D1] - - - - [Dn]

Number length can exceed 16 digits. In such a case redial will be inhibited.

Redial

Off Hook [R]

Store

Off Hook [S] [Ln] [D1] - - - [Dn] [S] [Ln] [D1] - - [Dn]

Cascading is permitted during store sequence.

Memory Dial

Off Hook [M] [Ln] - - - - - - - - - - - - [M] [Ln] - - - -

(wait for dialing to complete)

Cascading of numbers is permitted as indicated above.

Mixed Dialing

Off Hook Normal dialing, memory dialing.
Off Hook Redial, memory dial.
Off Hook Memory dial, memory dial

Off Hook - - Voice mode - - - [H] - - - - - - - - - - - [H]

Initiate Terminate

a. On the first depression of hold key both hold and mute outputs go high. These outputs stay high until the hold mode is cleared by a second depression of hold key.

b. An alternating alerting single tone appears on the tone out pin (pin 16) during hold mode with a repetition rate of approximately 800ms on/off.

Table 4. Summary of Operating Characteristics (S25912)

Normal Dialing

Off Hook [D1] - - - - [Dn]

Number length can exceed 16 digits. In such a case redial will be inhibited.

First key cannot be [*] or [#]

Redial

Off Hook [#] [#]

Memory Store

Off Hook [*] [Ln] [D1] - - - - [Dn]

Memory Dial

Off Hook [#] [Ln]

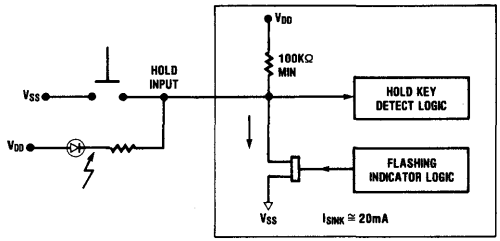
Hold

Off Hook - - Voice mode - - - [H] - - - - - - - - - - - [H]

Initiate Terminate

NOTE: Cascading or mixing of operations is not possible.

Figure 1. Block Diagram of Hold Input Circuitry (S25912)



Description of Hold Operation (S25912)

When "hold" key is first depressed, a flip-flop is set internally. Mute and hold outputs go "high". Tone output goes into a single tone mode with a repetition rate of 800ms on/off. Hold input will have a repetition rate of 100ms on/off to facilitate flashing of the "hold" indicator. "Hold" key must be debounced for 10ms. Second depression of the "hold" key resets the flip-flop and clears out the hold mode. Mute and hold outputs return to V_{SS}. Tone output returns to V_{SS} and hold input returns to open drain condition. See waveform details (Figure 5).

Figure 2. S25910 Memory Dialer Applications Circuit

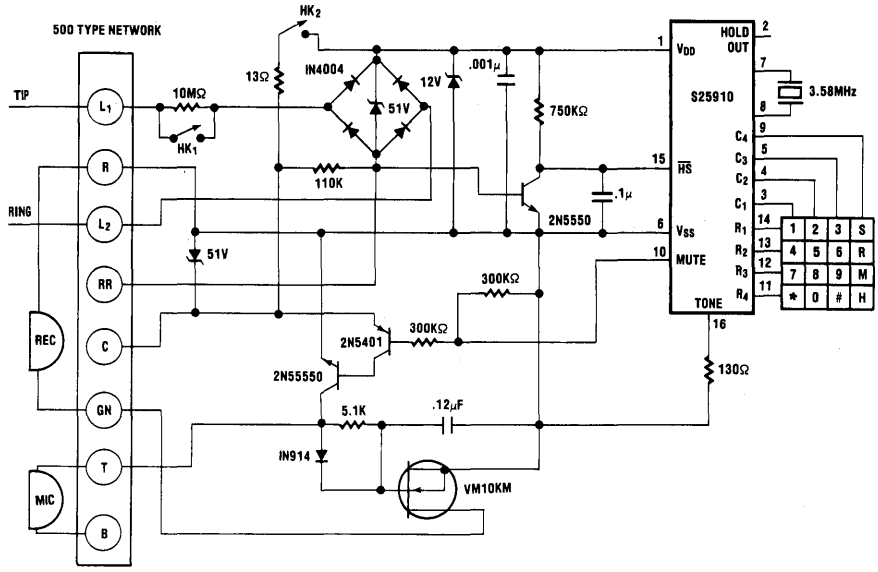
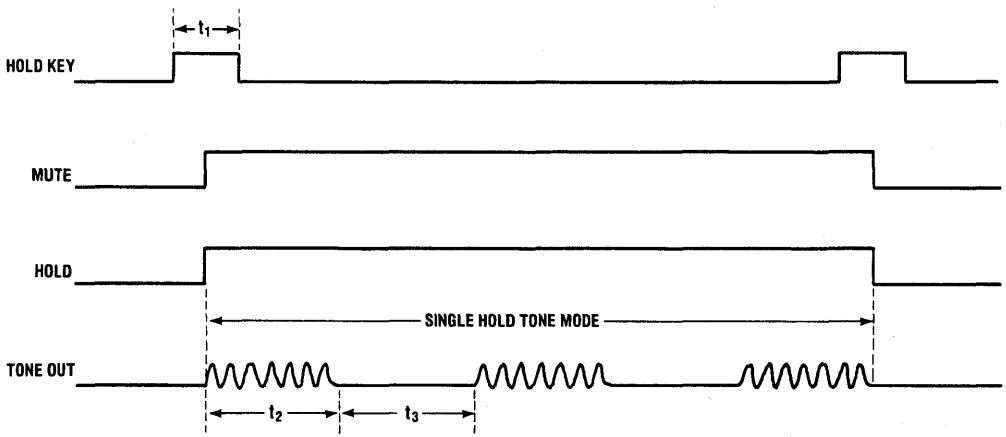


Figure 3. S25910 Timing Diagram Hold Waveform Details



t_1: 10ms MIN
t_2, t_3: APPROXIMATELY 800ms

Figure 4. S25912 Memory Dialer Applications Circuit

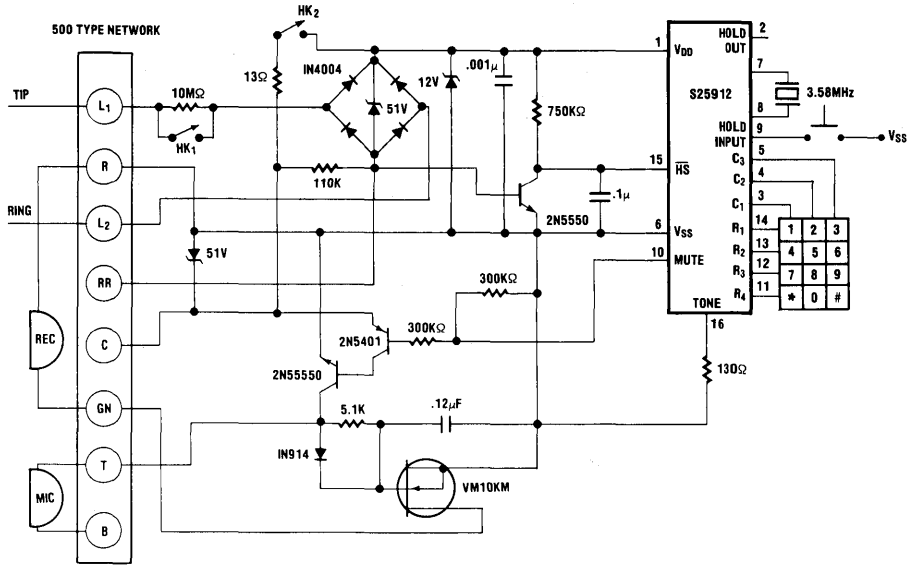
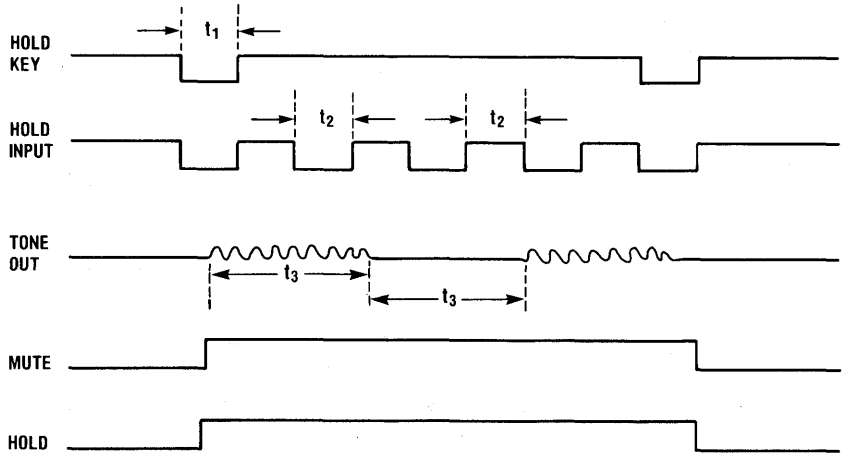


Figure 5. S25912 Timing Diagram Hold Operation



t_1: 10ms MIN t_2: 100ms TYP t_3: 800ms TYP

AMI

A Subsidiary of Gould Inc.

S3506/S3507/S3507A

CMOS SINGLE CHIP μ-LAW/A-LAW SYNCHRONOUS COMBO CODECS WITH FILTERS

COMMUNICATION PRODUCTS

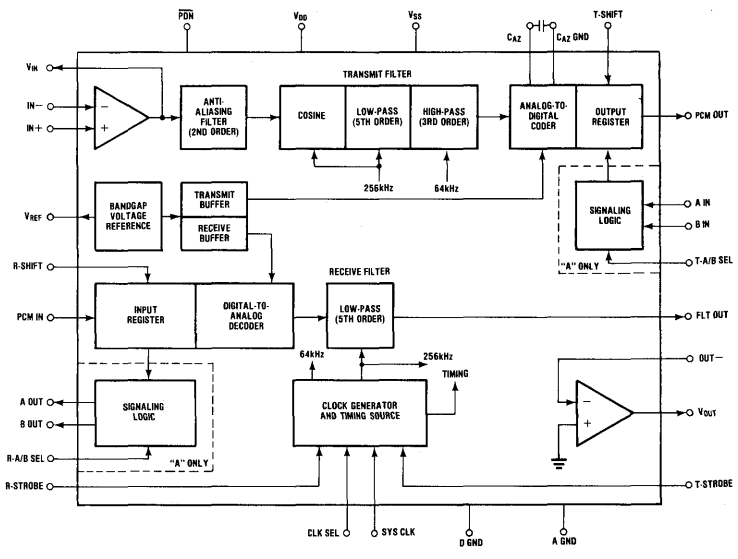
Features

- ☐ Independent Transmit and Receive Sections With 75dB Isolation
- ☐ Low Power CMOS 80mW (Operating) 8mW (Standby)
- ☐ Stable Voltage Reference On-Chip
- ☐ Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- ☐ Input Analog Filter Eliminates Need for External Anti-Aliasing Prefilter
- ☐ Input/Output Op Amps for Programming Gain
- ☐ Output Op Amp Provides ± 3.1V into a 600Ω Load or Can Be Switched Off for Reduced Power (70mW)
- ☐ Special Idle Channel Noise Reduction Circuitry for Crosstalk Suppression
- ☐ Encoder has Dual-Speed Auto-Zero Loop for Fast Acquisition on Power-Up
- ☐ Low Absolute Group Delay = 450μsec. @ 1kHz

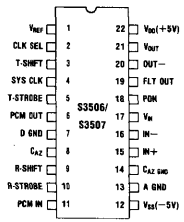
General Description

The S3506 and S3507 are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analog↔digital conversion circuits that conform to the desired transfer characteristic. The S3506 provides the European A-Law companding and the S3507 provides the North American μ-Law companding characteristic.

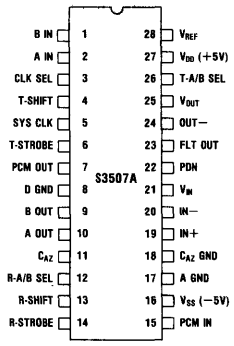
Block Diagram



Pin Configuration (22 Pin)



Pin Configuration (28 Pin)

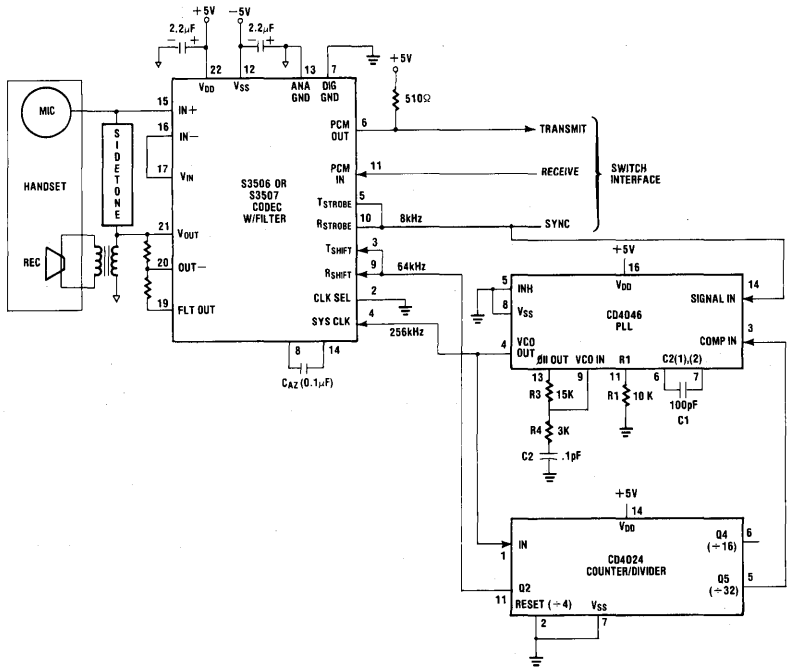


A Digital Telephone Application

Most new PABX designs are using PCM techniques for voice switching with an increasing trend toward applying them at the telephone level. The simplest form of a digital telephone design uses four wire pairs to interface to the switch. Two pairs carry transmit and receive PCM voice data. One pair supplies an 8kHz synchronizing clock signal and the remaining pair supplies power to the telephone. More sophisticated designs reduce costs by time-division-multiplexing and superimposition techniques which minimize the number of wire pairs. The AMI Single-chip Codec is ideally suited for this application because of the low component count and its simplified timing requirements. Figure 6 shows a schematic for a typical digital telephone design.

Since asynchronous time slot operation is not necessary, transmit and receive timing signals are common. A phase-lock-loop derives the 256kHz system clock and 64kHz shift clock from the 8kHz synchronizing signal received from the switch. The synchronizing signal also serves as the transmit/receive strobe signal since its duty cycle is not important for Codec operation. Microphone output feeds directly into the coder input while the decoder output drives the receiver through an impedance transformer to complete the design.

Figure 6. Voice Processing in a Digital Telephone Application



Single Chip Codecs With Filters

S44231 A-Law Synchronous Codec
S44232 μ-Law Synchronous Codec
S44233 A-Law Asynchronous Codec
S44234 μ-Law Asynchronous Codec

Features

- ☐ Synchronous or Asynchronous Operation for 2048/1544/1536 KHz PCM Rate
- ☐ Precision Voltage Reference
- ☐ Meets or Exceeds AT&T D3, CCITT G.711, G.712 and G.733 Specifications
- ☐ Low Power Dissipation: 60mW Typical
- ☐ Auto-Zero Cancel Circuitry Requires No External Components
- ☐ Input Op Amp for Gain Adjustment
- ☐ Anti-aliasing Filter
- ☐ Licensed Second Source for Hitachi

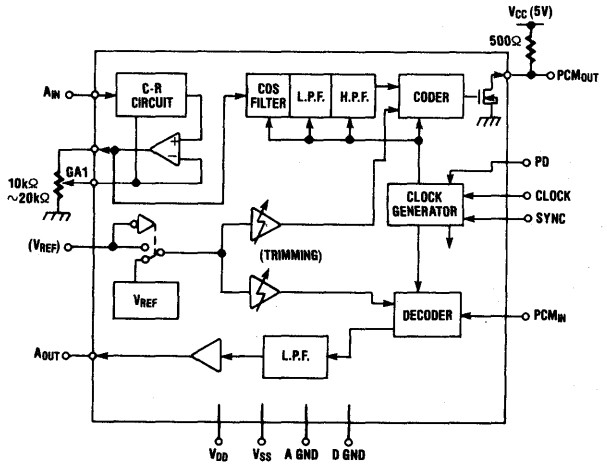
General Description

The S44231/2/3/4 are monolithic silicon gate CMOS chips designed to perform the per channel voice frequency encoding/decoding used in PCM systems. The chips contain the band limiting filters and analog ↔ digital circuits necessary to conform to A-Law/μLaw companding characteristics called out in CCITT specifications.

These circuits provide the interface between the analog signals of the subscriber loop and the digital signals of the PCM highway in a digital telephone switching system. The devices operate from dual power supplies of ±5V.

For a sampling rate of 8kHz, PCM input/output data rate can be selected from 1536/1544/2048MHz in synchronous operation. This selection is achieved automatically.

Block Diagram



Pin Configuration

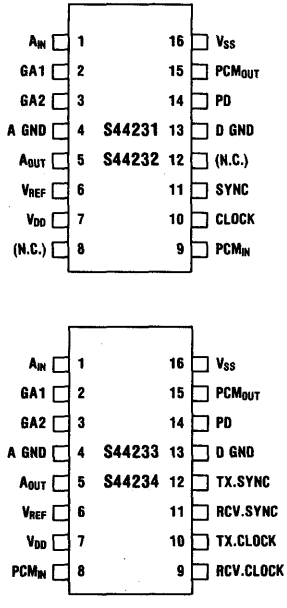


Table 1A. Pin Descriptions (S44231/S44232)

No.	Symbol	Function	Remarks
1	A_{IN}	Analog Input	
2	GA1	Gain Adjust1	Feed-Back Input
3	GA2	Gain Adjust2	$10k\Omega \leqslant RL \leqslant 20k\Omega CL < 100pF$
4	A GND	Analog Ground	
5	A_{OUT}	Analog Output	$RL \geqslant 3k\Omega, CL \leqslant 100pF$
6	V_{REF}	External V_{REF}	Open or (2-3V)
7	V_{DD}	Positive Power Supply	$5V \pm 5\%$
8	(N.C.)		
9	PCM_{IN}	PCM Data Input	(TTL)
10	CLOCK	PCM Bit Clock	(TTL) 2048/1544/1536kHz
11	SYNC	Synchronization	(TTL) 8kHz
12	(N.C.)		
13	D GND	Digital Ground	
14	PD	Power Down	(TTL) "0" = down
15	PCM_{OUT}	PCM Data Output	Open Drain
16	V_{SS}	Negative Power Supply	$-5V \pm 5\%$

Table 1B. Pin Descriptions (S44233/S44234)

No.	Symbol	Function	Remarks
1	A_{IN}	Analog Input	
2	GA1	Gain Adjust1	Feed-Back Input
3	GA2	Gain Adjust2	$10k\Omega \leqslant RL \leqslant 20k\Omega CL < 100pF$
4	A GND	Analog Ground	
5	A_{OUT}	Analog Output	$RL \geqslant 3k\Omega, CL \leqslant 100pF$
6	V_{REF}	External V_{REF}	Open or (2-3V)
7	V_{DD}	Positive Power Supply	$5V \pm 5\%$
8	(N.C.)		
9	RCV_{CLK}	RCV PCM Bit Clock	(TTL) 2048/1544/1536kHz
10	TX_{CLK}	TX PCM Bit Clock	(TTL) 2048/1544/1536kHz
11	RCV SYNC	Synchronization	(TTL) 8kHz
12	TX SYNC	Synchronization	(TTL) 8kHz
13	D GND	Digital Ground	
14	PD	Power Down	(TTL) "0" = down
15	PCM_{OUT}	PCM Data Output	Open Drain
16	V_{SS}	Negative Power Supply	$-5V \pm 5\%$

Absolute Maximum Rating

No.	Item	Rating
1	V_{DD}	−0.3 to +6V
2	V_{SS}	+0.3 to +6V
3	Storage Temperature	−55°C to 125°C
4	Power Dissipation	0.5W
5	Digital Input Voltage	$-0.3V<V_{IN}<V_{DD}+0.3V$
6	Analog Input Voltage	$V_{SS}-0.3V<V_{IN}<V_{DD}+0.3V$

Electrical Characteristics

1) Static Characteristics (V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_A = 0 − 70°C)

Symbol	Pin	Descriptions	Specifications				Note/Conditions
			Min.	Typ.	Max.	Unit	
I_{DD}	7	V_{DD} Current (Open)		6.0	10.0	mA	
I_{SS}	16	V_{SS} Current (Open)	−10.0	−6.0		mA	
I_{DDST}	7	V_{DD} Current (Standby)		0.6	1.0	mA	
I_{SSST}	16	V_{SS} Current (Standby)	−0.2			mA	
I_L	1,2,9 10,14	Leak Current	−10.0 −10.0		10.0 10.0 10.0	μA μA μA	VM = 0.8V VM = 2.0V V_{DD} = VM = 5.25V
I_{PL}	6,11	Pull Up Current	−100		100	μA	
I_{DL}	15	Leak Current	−10		10.0	μA	V_{DD} = VM = 5.25V
C_{AIN1}	1,2	Analog Input Capacitance		100	200	pF	at 1kHz Vbias = 0
C_{AIN2}	1,2	Analog Input Capacitance			40	pF	at 1MHz Vbias = 0
CD_{IN}	6,9,10 11,14	Input Capacitance			10	pF	at 1MHz Vbias = 0
R_{OUTA}	5	A_{OUT} Resistance			30	Ω	
R_{OUTG}	3	GA2 Resistance			30	Ω	
V_{GSW}		GA2 Output Swing	−3.0		3.0	V	RL = 10kΩ
V_{OFFIN}		Analog Offset Input	−500		500	mV	Note 1
V_{OFFG}		GA2 Offset Output	−50		50	mV	Note 1
V_{OFFA}		A_{OUT} Offset Output	−50		50	mV	PCM_{IN} = +0-Code
CD_{OUT}	15	PCM_{OUT} Capacitance			15.0	pF	at 1MHz Vbias = 0
V_{OL}	15	PCM_{OUT} Low Voltage			0.4	V	RL = 500Ω + I_{OL} = 0.8mA
V_{OH}	15	PCM_{OUT} High Voltage	$V_{CC}-0.3$			V	I_{OH} = −150μA
V_{IH}	10,11 2,14	Digital Input High Voltage	2.4			V	
V_{IL}	10,11 2,14	Digital Input Low Voltage			0.8	V	
R_{AIN}	1	Analog Input Resistance	50	200		kΩ	at 1MHz

NOTE 1) Analog Input Amplifire Gain = 0dB (GA1 is connected to GA2)

2) Dynamic Characteristics (V_{DD} = 5 ± 0.25V, V_{SS} = −5 + 0.25V, V_{CC} = 5 ± 0.25V, T_A = 0 − 70°C, See Figure 4)

Symbol	Descriptions	Specifications				Notes
		Min.	Typ.	Max.	Unit	
FS	Synchronization Rate		8		kHz	
FC	PCM Bit Clock Rate		1536/1544/ 2048		kHz	
t_{WC}	Clock Pulse Width	200			ns	
t_{WSH}	SYNC Pulse High Width	200			ns	
t_{WSL}	SYNC Pulse Low Width	8			μs	
t_r	Logic Input Rise Time			50	ns	
t_f	Logic Input Fall Time			50	ns	
t_{SC}	SYNC to Clock Delay	−50		100	ns	NOTE 1
t_{CD}	Clock to PCM_{OUT} Delay			220	ns	NOTE 1, 2, 3
t_{SU}	PCM_{IN} Setup Time			65	ns	NOTE 1
t_{HD}	PCM_{IN} Hold Time			120	ns	NOTE 1

NOTE 1) t_r, t_f of digital input or clock is assumed 5ns for timing measurement.
2) PCM_{OUT} LOAD CONDITION: 500Ω 165pF + two LS-TTL Equivalent (I_{IL} = 0.8mA, I_{IH} = −150μA) Threshold Level (V_{OH} = 2.4V, V_{OL} = 0.4V)
3) t_{CD} Specification is permitted in all of the region of the specification TSC and also it specifies the go-high timing from 8th bit-low-state.

3) System Related Characteristics (V_{DD} = 5 ± 0.25V, V_{SS} = 5 ± .025V, V_{CC} = 5 ± 0.25V, T_A = 0 − 70°C, Input Amplifier Gain = 0dB, V_{REF}-pin remains open, GA2 Load = 10KΩ, A_{OUT} Load = 3KΩ)

Symbol	Descriptions	Test Conditions		Specifications				Notes
				Min.	Typ.	Max.	Unit	
SDA	Signal to Dist.	820Hz tone	−45dBm0	24			dB	p-wgt
	(A to A)		−40	29			dB	
			−30 to 3	35			dB	Note 1
SNA	Signal to Dist.	Noise	−55dBm0	13.5			dB	
	(A to A)		−40	28.5			dB	
			−34	33.5			dB	
			−27 to −6	35.5			dB	
			−3	27.5			dB	
SDX	Signal to Dist.	820Hz tone	−45dBm0	25			dB	p-wgt
	(A to D)		−40	30			dB	
			−30 to 3	35			dB	Note 1
SDR	Signal to Dist.	820Hz tone	−45dBm0	25			dB	p-wgt
	(D to A)		−40	30			dB	
			−30 to 3	35			dB	Note 1
GTA	Gain Track.	820Hz tone	−55 to −50dBm0	−2.0		2.0	dB	
	(A to A)		−50 to −40	−0.8		0.8	dB	
			−40 to +3	−0.4		0.4	dB	Note 1
GNA	Gain Track.	Noise	−60 to −55dBm0	−1.0		1.0	dB	
	(A to A)		−55 to −10	−0.5		0.5	dB	

3) System Related Characteristics (continued)

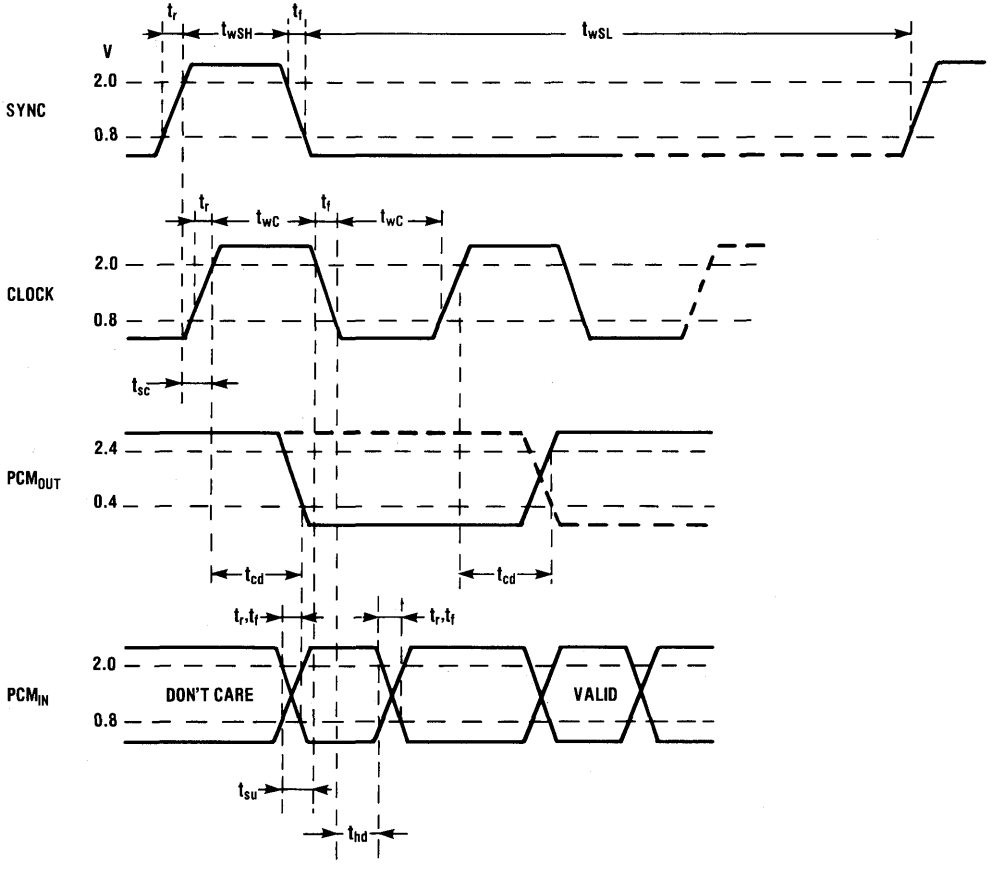
Symbol	Descriptions	Test Conditions		Specifications Min.	Typ.	Max.	Unit	Notes
GTX	Gain Track. (A to D)	820Hz tone	−55 to −50	−0.8		0.8	dB	
			−50 to −40	−0.4		0.4	dB	
			−40 to +3 dBm0	−0.2		0.2	dB	Note 1
GTR	Gain Track. (D to A)	820Hz tone	−55 to −50	−0.8		0.8	dB	
			−50 to −40	−0.4		0.4	dB	
			−40 to +3 dBm0	−0.2		0.2	dB	Note 1
FRX	Freq. Response (A to D) (Loss)	Relative to 820Hz	0.06kHz	24				
			0.2	−0.15		2.5		
			0.3 to 3	−0.15		0.2	dB	Note 1
		0dBm0	3.3	−0.15		0.65		
			3.4	−0.15		0.9		
			4.0	14				
FRR	Freq. Response (D to A) (Loss)	Relative to 820Hz	0 to 3 kHz	−0.15		0.2		
			3.3	−0.15		0.65	dB	
		0dBm0	3.4	−0.15		0.9		Note 1
			4.0		14			
AIL	Analog Input Level	820Hz 0dBm0	25°C nom. P.S.	1.217	1.231	1.246	Vrms	Note 1
AOL	Analog Output Level	820Hz 0dBm0	25°C nom. P.S.	1.217	1.231	1.246	Vrms	Note 1
AT	AIL, AOL Variation with temp.	Relative to 25°C nominal P.S.			0.001		dB/°C	
AP	AIL, AOL Variation with P.S.	25°C, Supplies ±5%			±0.05		dB	
ALS	GAIN Variation over Temp. P.S.	A to D D to A	INITIAL	−0.15		0.15	dB	
AIP	Peak Analog Input			3.0			V	
AOP	Peak Analog Output			2.5			V	
PDL	Propagation Delay	A to A	0dBm0			540	μs	
DD	Delay Distortion	A to A	0.5 to 0.6kHz			1.4		rel.
		0dBm0	0.6 to 1.0			0.7	μs	to
			1.0 to 2.6			0.25		min.
			2.6 to 2.8			1.4		delay
PSRR	PSRR	A to A	V_{DD} + 100mV op 1kHz	30				
		A_{IN} = A GND	V_{SS} + 100mV op 1kHz	30			dB	
			V_{DD} + 100mV op 3kHz	20				
			V_{SS} + 100mV op 3kHz	20				

3) System Related Characteristics (continued)

Symbol	Descriptions	Test Conditions	Specifications Min.	Typ.	Max.	Unit	Notes
ICNA	Idle Channel Noise	A to A A_{IN} = A GND			−70	dBm0P	A-Law
ICNX	Idle Channel Noise	A to D A_{IN} = A GND			−72	dBm0P	A-Law
ICNR	Idle Channel Noise	D to A PCM_{IN} = +0-Code			−78	dBm0P	A-Law
ICNA	Idle Channel Noise	A to A A_{IN} = A GND			20	dBmrnco	μ-Law
ICNX	Idle Channel Noise	A to D A_{IN} = A GND			18	dBrnco	μ-Law
ICNR	Idle Channel Noise	D to A PCM_{IN} = +0-Code			12	dBrnco	μ-Law
IM1	Intermodulation	A to A (2a-b) a;0.47kHz, −4dBm0 b;0.32, −4			−38	dBm0	
IM2	Intermodulation	A to A (a-b) a;1.02kHz, −4dBm0 b;0.05, −23			−52	dBm0	
ICS	Single Freq. Noise	A to A 8, 16, 24, 32, A_{IN} = A GND 40kHz			−50	dBm0	
DIS	Discrimination	A to A 0dBm0 4.6 to 200kHz	30			dB	
XTKA	A_{IN} to A_{OUT} Crosstalk	820Hz 0dBm0			−65	dB	Note 1
XTKD	PCM_{IN} to PCM_{OUT}	820Hz 0dBm0			−65	dB	Note 1

Note 1. Test conditions for S44231/S44232 versions are referenced to 1020Hz tone.

Timing Diagram



AMI

A Subsidiary of Gould Inc.

Advanced Product Description **SSP CP/M-1**

Software Simulator/Assembler Program Package

Features

- ☐ Provides Exact Simulation of Operation of AMI S28211 Signal Processing Peripheral
- ☐ Runs on Systems Using CP/M-80 2.2 Operating System
- ☐ Supplied on Standard 1Bm 8″ Single Density (3740) Format Disc
- ☐ Allow Continuous or Step-by-Step Operation
- ☐ Allows Setting of Breakpoints on All Major Flags
- ☐ Trace Buffer Allows Storage and Display of Status of Previous 50 Instructions During Continuous Operation
- ☐ Fully Documented

General Description

The SSP CP/M-1 is a software simulator for the AMI S28211 Signal Processing Peripheral (SPP). For information on the SPP chip please refer to the S28211 Advanced Product Description.

The SSP CP/M-1 package allows the user to simulate operation of the S28211 chip on any host computer which supports the following minimum hardware configuration.

1. Z80, 8080, 8085 CPU
2. 64K of Memory
3. CP/M-80 2.2 Operating System

The SSP CP/M-1 package allows the user to simulate the operation of the S28211 chip either in a step mode or free running, with or without breakpoints. Data I/O for the simulation may be provided by means of files or directly from the terminal. An assembler allows the user to input the SPP program (in SPP Assembly Language) and the memory data either from a file or from the keyboard. The assembly listing may be dumped to file which can then be used to generate the ROM mask for the S28211 by AMI. During simulation a trace buffer may be used to store the last 50 (maximum) instructions executed. This greatly facilitates continuous simulation in conjunction with the breakpoints which may be set on (1) any individual instruction (2) the input flag (3) the output flag (4) overflow in the accumulator. The trace feature, either using the trace buffer or in the step-by-step mode, gives the user the complete status of the simulation, including the last instruction executed and the conditions of all internal registers, counters, latches, and busses.

AMI

A Subsidiary of Gould Inc.

Advanced Product Description **S28211**

SIGNAL PROCESSING PERIPHERAL

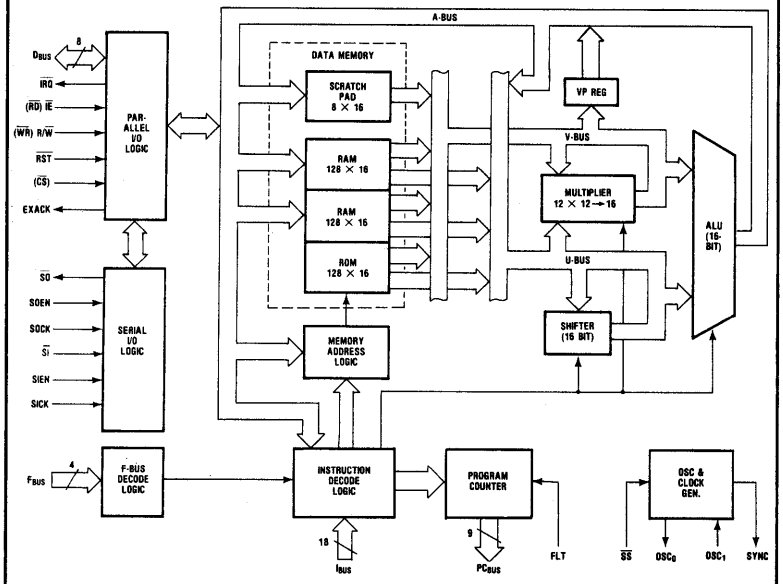
Features

- ☐ Single-Chip Programmable Digital Signal Processor
- ☐ May Be Customized (ROM Programmed) With Customer Generated Routines
- ☐ Self-Emulation Capability
- ☐ Standard Preprogrammed Processors Available
- ☐ Fetch/Multiply/Add/Store Cycle
- ☐ 512 Word × 18 Bit Instruction Memory
- ☐ Unique Three Port Data Memory
  256 × 16 RAM/128 × 16 ROM
- ☐ 12 × 12 Pipelined Multiplier With 16 Bit Product
- ☐ 16 Bit Accumulator With Overflow Detect/Protect
- ☐ Double Buffered Asynchronous Serial I/O Port
- ☐ μP-Compatible I/O Port i.e. 6800 (A Version), 8080 (B Version), etc.
- ☐ External Instruction Memory Version Available For Program Development (S28212)

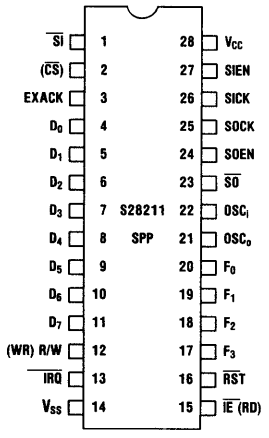
General Description

The S28211 is a single-chip microcomputer which has been optimized to execute digital signal processing algorithms commonly used in applications such as telecommunications speech processing, industrial process control instrumentation, etc. It may be used as a stand alone unit, or may be operated as a peripheral in a microprocessor based system. The latter configuration allows arrays of S28211s to be used together for increased processing throughput. The S28211's multibus, pipelined architecture and powerful multioperation instructions make it possible to write very compact algorithms. This allows the available memory to be used efficiently and increases the execution speed of a given algorithm. The S28211 may be custo-

Simplified Block Diagram



Pin Configuration



NOTE:
PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION

customized with user generated algorithms (Factory ROM Programmed). A selection of support tools (Assembler, Simulator, Real-time Emulator) are available for this task. In addition, a family of pre-programmed S28211s are available for standard applications.

Functional Description

The main functional elements of the S28211 (see Block Diagram) are:

1. a 512 × 18 ROM which contains the user program.
2. a 3-port 384 × 16 data memory (one input and two output ports) which allows simultaneous readout of two words.
3. a 12-bit × 12-bit high-speed parallel multiplier with 16-bit rounded product.
4. an Arithmetic/Logic Unit (ALU).
5. I/O and control circuits.

The S28211 is implemented in a combination of clocked and static logic which allows complete overlap of the multiply operation with the read, accumulate, and write operations. The basic instruction cycle is Read, Modify, Write, where the "Read" brings the operands from the data memory to the multiplier and/or the ALU, the "modify" operates on those operands and/or the product of the previous operands, and the "Write" stores the result of the "Modify." The cycle time for the instruction is 300 nanoseconds. This results in an arithmetic throughput of about 3.3 multiply and accumulate operations per microsecond.

The S28211 is intended to be used as a microprocessor peripheral. The S28211 control interface is directly compatible with the 6800 microprocessor bus (A version) or 8080/8085/Z80 microprocessor bus (B version), but can be adapted to other 8-bit microprocessors with the addition of a few MSI packages.

Operating in a microprocessor system, the S28211 can be viewed as a "hardware subroutine" module. The microprocessor can call up a "subroutine" by giving a command to the S28211. A powerful instruction set (including conditional branching and one level of subroutine) permits the S28211 to function independently of the microprocessor once the initial command is given. The S28211 will interrupt the microprocessor upon completion of its task. The microprocessor is free to perform other operations in the interim.

The S28211 contains a high-speed serial port for direct interface to an analog-to-digital (A/D) converter. In many applications, real-time processing of sampled analog data can be performed within the S28211 without tying up the main microprocessor. Data transfer to the microprocessor occurs upon completion of the S28211 processing.

Separate input and output registers exchange data with the S28211 data ports. Serial interface logic optionally converts the parallel 2's complement data to serial 2's complement or sign + magnitude format. Data format and source (serial or parallel port) is software selectable.

The S28211 is a memory-mapped peripheral, occupying 16 locations of the microprocessor memory space. Selecting the correct S28211 address will activate the corresponding control mode.

The control modes and the LIBL instruction enable real-time modification of the S28211 programs. This permits a single S28211 program to be used in several different applications. For example, an S28211 might be programmed as a "universal" digital filter, with cutoff frequency, filter order, and data source (serial or parallel port) selected at execution time by the control microprocessor.

AMI

A Subsidiary of Gould Inc.

Advanced Product Description **S28212A/B**

SIGNAL PROCESSING PERIPHERAL

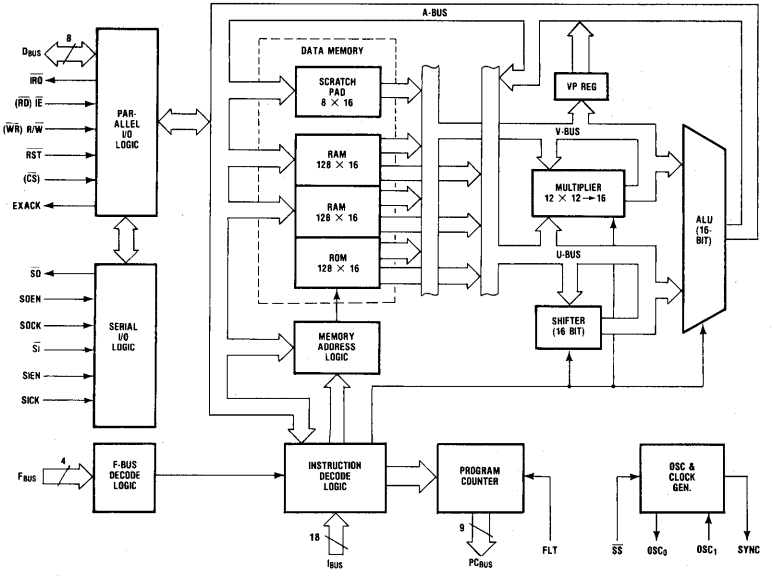
Features

- ☐ Programmable Digital Signal Processor
- ☐ Executes S28211 Functions From External Memory At Full Speed
- ☐ Fetch/Multiply/Add/Store In Single 300 nanosec. Cycle
- ☐ Addressing Capability Of 512 Instructions
- ☐ Unique Three Port Data Memory With 256 Words Of RAM And 128 Words Of ROM
- ☐ 12x12 Multiplier With 16 Bit Product
- ☐ 16 Bit Accumulator With Overflow Detect/Protect
- ☐ Double Buffered Asynchronous Serial I/O Port
- ☐ Microprocessor Compatible I/O Port For 6800 Family (A Version) or 8080/85/Z80 etc. (B Version)

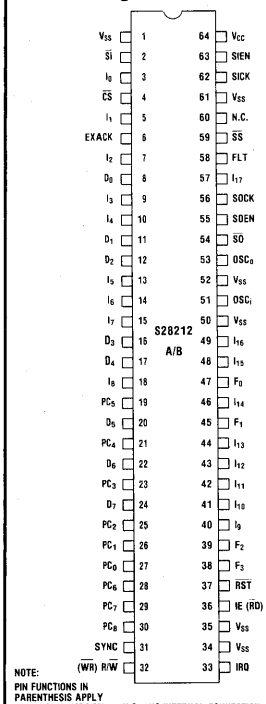
General Description

The S28212 is an external instruction memory version of the S28211 Signal Processing Peripheral. The internal program counter and instruction bus are made accessible via dedicated pins on the 64-pin package to allow the device to operate from an external instruction memory at full speed. This device may be used in place of the mask-programmed S28211 in development or small medium production run applications. In addition to the externally accessible program counter and instruction bus, the device also features a sync output to synchronize the external circuitry to the internal instruction cycle, and a single-step capability. This allows the device to execute programs one step at a

Simplified Block Diagram



Pin Configuration



NOTE:
PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION
N.C. = NO INTERNAL CONNECTION

General Description (Continued)

time, to simplify the debugging process. To aid the designer in writing software for this device a mnemonic assembler and simulation program (SSPCP/M-1) is available. For information regarding the main architecture and programming of the device, please refer to the S28212 full Data Sheet.

Functional Description

The main functional elements of the S28212 (see Block Diagram) are:

1. A dedicated interface to an external program memory with a 9-bit address drive capability.
2. A 3-port 384x16 data memory (one input and two output ports) which allows simultaneous readout of two words.
3. A 12-bitx12-bit high-speed parallel multiplier with 16-bit rounded product.
4. An Arithmetic/Logic Unit (ALU).
5. I/O and control circuits.

The S28212 is implemented in a combination of clocked and static logic which allows complete overlap of the multiply operation with the read, accumulate, and write operations. The basic instruction cycle is Read, Modify, Write, where the "Read" brings the operands from the data memory to the multiplier and/or the ALU, the "Modify" operates on those operands and/or the product of the previous operands, and the "Write" stores the result of the "Modify". The cycle time for the instruction is 300 nanoseconds. This results in an arithmetic throughput of about 3.3 multiply and accumulate operations per microsecond.

The S28212 is intended to be used as a microprocessor peripheral. The S28212 control interface is directly compatible with the 6800 microprocessor bus (A Version) or 8080/8085/Z80 microprocessor bus (B Version) but can be adapted to other microprocessors with the addition of a few SSI packages.

Operating in a microprocessor system, the S28212 can be viewed as a "hardware subroutine" module. The microprocessor can call up a "subroutine" by giving a command to the S28212. A powerful instruction set (including conditional branching and one level of subroutine) permits the S28212 to function independently of the microprocessor once the initial command is given. The S28212 will interrupt the microprocessor upon completion of its task. The microprocessor is free to perform other operations in the interim.

The S28212 contains a high speed serial port for direct interface to an analog-to-digital (A/D) converter or Codec. In many applications, real time processing of sampled analog data can be performed with the S28212 without tying up the main microprocessor. Data transfer to the microprocessor occurs upon completion of the S28212 processing.

Separate input and output registers exchange data with the S28212 data ports. The serial interface logic optionally converts the parallel 2's complement data to serial 2's complement or sign + magnitude format. Data format and source (serial or parallel port) is software selectable.

The S28212 is a memory mapped peripheral, occupying 16 locations of the microprocessor memory space. Selecting the correct S28212 address will activate the corresponding control mode. The control modes and the LIBL instruction enable real-time modification of the S28212 programs. This permits a single S28212 program to be used in several different applications. For example, an S28212 might be programmed as a "universal" digital filter, with cut-off frequency, filter order, and data source (serial or parallel port) selected at execution time by the control microprocessor.

The S28212 allows the user:
—Sixteen control junctions
—three page modes for data memory
—four addressing modes

and a powerful double op-code instruction set* for compact real time DSP algorithm development.

For further details see the final data sheet.

* See Tables 1 and 2

S28211 Object Code Instruction Formats

SPP ADDRESSING MODES	← 16 BITS →					
	I_{17}-I_{13}				I_1	I_0
Offset Addressin (UV/US)	OP2 5 Bits	OP1 5 Bits	0_3 3 Bits	0_2 3 Bits	0-US 1-UV	0
Direct Addressing (D)	OP2 5 Bits	OP1 5 Bits	Direct Address 7 Bits			1
Direct Transfer (DT)	OP2 5 Bits	OP1* 4 Bits	Transfer Address 9 Bits			
Literal (L)	OP2 5 Bits	Literal Data Word 13 Bits				

*Bit 0 of OP1 (18) is set to zero in this address mode.

Table 1. SSPP Instruction Set-OP1 Instructions

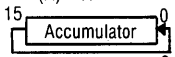
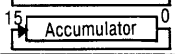
Type	Mnemonic	Hex Code I12-I8	Address Modes	Operations	Description
No Operation	**NOP**	00	- - -	None	**No OP**eration
Accumulator Operations 1. Arithmetic	**CLA**	12	- - -	0→A	**CL**ear **A**ccumulator
	ABS	02	- - -	ABS (A)→A	**ABS**olute value of accumulator is placed in accumulator.
	NEG	04	- - -	−(A)→A	**NEG**ate accumulator contents (two's complement) and replace in accumulator.
	SHR	0A	- - -	(A)/2→A	**SH**ift **R**ight accumulator contents 1-bit position. Equivalent to dividing contents by two.
	SHL	1A	- -	2(A)→A	**SH**ift **L**eft accumulator contents 1-bit position. Equivalent to multiplying contents by two
	SGV	03	UV/US, D	(A)→A, if sign (A) = sign V/S −(A)→A, if sign (A) ≠ sign V/S	**Sign** of RAM output **V** is the of accumulator contents. Accumulator contents are negated (two's complement) if different sign from V. Useful in implementing hard limiter function.
Accumulator Operations 2. Logical	**CMP**	06	- - -	(A)→A	**CoMP**lement accumulator contents. Logically inverts every bit in accumulator. (One's complement.)
	LRL	1E	- -		**L**ogical **R**otate **L**eft accumulator. Shifts contents 1-bit position left, and B_{15}–B_0 position.
	LRR	0E	- -		**L**ogical **R**otate **R**ight accumulator. Shifts contents 1-bit position right, and B_0–B_{15} position.
Addition Operations	**AUZ**	1B	UV/US	(U) + 0→A	**A**dd **U** and **Z**ero. Loads RAM output U into the accumulator.
	AVZ	11	UV/US, D	(V/S) + 0→A	**A**dd **V**/S and **Z**ero. Loads RAM output V/S into the accumulator.
	AVA	19	UV/US, D	(V/S) + (A)→A	**A**dd **V**/S and **A**ccumulator contents. Sum is placed back into accumulator.
	AUV	1D	UV/US	(U) + (V/S)→A	**A**dd RAM outputs **U** and **V**/S and place sum in accumulator.
	AIZ	14	- -	(IR) + 0→A	**A**dd **I**nput Register and **Z**ero Loads input register contents into accumulator.
Subtraction Operations	**SZU**	0B	UV/S	0 − (U)→A	**S**ubtract **Z**ero and **U**. Negates and loads RAM output U into the accumulator.
	SVA	09	UV/US, D	(V/S) − (A)→A	**S**ubtract **V**/S and **A**ccumulator contents. The difference (V − A) is placed in the accumulator.
	SVU	0D	UV/US	(V/S) − (U)→A	**S**ubtract RAM outputs **V** and **U** and place difference (V − U) in the accumulator.
Multiply/ Add Operations	**APZ**	10	- - - (current inst.) UV/US, D (prec. instr)	(P) + 0→A	**A**dd **P**roduct and **Z**ero. Loads multiplier product into the accumulator. The multiplier inputs were set up in the preceding instruction by addressing mode.
	APU	1C	UV (current instr) UV/US, D (prec. instr)	(P) + (U)→A	**A**dd **P**roduct and RAM output **U**. Sum is placed in accumulator. The multiplier inputs were set up in preceding instruction by addressing mode.
Multiply/ Subtract Operations	**SPA**	08	- - - (current instr) UV/US, D (prec. instr)	(P) − (A)→A	**S**ubtract **P**roduct and **A**ccumulator contents. Difference (P − A) is placed in accumulator. The multiplier inputs were set up in preceding instruction by addressing mode.
	SPU	0C	UV/US (current instr) UV/US, D (prec. instr)	(P) − (U)→A	**S**ubtract **P**roduct and RAM output **U**. Difference (P − U) is placed in accumulator. The multiplier inputs were set up in preceding instruction by addressing mode.
Logical Operations	**DVA**	0F	UV/US.D	(V/S) AND (A)→A	Logical **AND V**/S and **A**ccumulator contents. Result is placed in accumulator
	DUV	1F	UV/US	(U) AND (V/S)→A	Logical **AND** RAM outputs **U** and **V**/S. Result is placed in accumulator.
	RVA	07	UV/US.D	(V/S) OR (A)→A	Logical **OR V**/S and **A**ccumulator contents. Result is placed in accumulator.
	RUV	17	UV/US	(U) OR (V/S)→A	Logical **OR** RAM outputs **U** and **V**/S. Result is placed in accumulator.

Table 1. SSPP Instruction Set-OP1 Instructions (continued)

Type	Mnemonic	Hex Code I12-I8	Address Modes	Operations	Description
No Operation	**NOP**	00	- - -	None	**No OP**eration
	XVA	05	UV/US.D	(V/S) EXOR (A)→A	Logical e**X**clusive or **V**/S and **A**ccumulator contents. Result is placed in accumulator.
	XUV	15	UV/US	(U) EXOR (V/S)→A	Logical e**X**clusive OR RAM outputs **U** and **V**/S. Result is placed in accumulator.

Table 2. SSPP Instruction Set-OP2 Instructions

Type	Mnemonic	Hex Code I16-I12	Address Modes	Operations	Description
No Operation	**NOP**	00	- - -	None	**No OP**eration
Load Instructions	**LLTI**	15	Literal	HHH→IR	**L**oad **LiT**eral in **I**nput register. A 12-bit (3 hex digits) literal is transferred to the input register. This instruction cannot be used with an OP1 instruction or with a specified addressing mode. Literal is left justified to occupy bits 4-15 in register.
	LIBL	0C	- - -	(IR)→BAS (IR)→LC	**L**oad **I**nput contents to **B**ase register and **L**oop counter. See Figure 4. Clears input flag (LOW).
	LACO	03	- - -	(A)→OR	**L**oad **AC**cumulator contents into the **O**utput Register. This is the basic data output instruction. Sets output flag (HIGH). The IRQ line will be set low if the SRO mode is not set.
	LAXV	09	UV/US, D	(A)→IX, V/S (A)→A	**L**oad **A**ccumulator contents into index register and RAM location **V**/S. Accumulator is truncated to 5 most significant bits after the operation. See Figure 4.
	LALV	0D	UV/US, D	(A)→LC, V/S	**L**oad **A**ccumulator to **L**oop counter and RAM location **V**/S. See Figure 4.
	LABV	08	UV/US, D	(A)→BAS, V/S (A)→A	**L**oad **A**ccumulator to **B**ase and RAM location **V**/S. Truncate accumulator contents to most significant 5 bits after the operation. See Figure 4.
Data Transfer Instructions	**TACU**	1A	UV/US	(A)→U	**T**ransfer **A**ccumulator **C**ontents into RAM location **U**.
	TACV	1D	UV/US, D	(A)→V/S	**T**ransfer **A**ccumulator **C**ontents into RAM location **V**/S.
	TIRV	1C	UV/US, D	(IR)→V/S	**T**ransfer **I**nput **R**egister Contents to RAM location **V**/S. This is the basic data input instruction. Clears input flag (LOW).
	TVPV	09	UV/US, D	VP→V/S	**T**ransfer contents of **VP** register (equals previous value of output V) to RAM location **V**/S.
	TAUI	1E	UV/US	(A)→U	**T**ransfer **A**ccumulator contents into RAM location **U** using **I**ndex register as base.
Register Manipulation Instruction	**INIX**	12	- - -	(IX) + 1→IX	**IN**crement the **I**nde**X** register.
	DECB	07	- - -	(BAS)—1→BAS	**DEC**rement the **B**ase register.
	INCB	11	- - -	(BAS) + 1→BAS	**INC**rement the **B**ase register.
	SWAP	0F	- - -	BAS↔IX	**SWAP** the roles of Base and Index registers.
Unconditional Branch Instruction	**JMUD**	14	DT	HH→PC	**J**u**M**p **U**nconditionally **D**irect to location indicated by 8-bit two hex digits) literal HH. Cannot be used with an OP1 instruction requiring specific addr. mode.
	JMUI	16	UV/US, D	[(IX)]→PC	**J**u**M**p **U**nconditionally **I**ndirect to location indicated by contents of RAM address pointed to by index and displacement indicated by V/S. $[V/S)_{0-7}$→PC.

Table 2. SSPP Instruction Set–OP2 Instructions (continued)

Type	Mnemonic	Hex Code I16-I12	Address Modes	Operations	Description
No Operation	**NOP**	00	- - -	None	**No OP**eration
Conditional Branch Instructions	**JMCD**	0E	DT	HH→PC, if LC≠0 (LC)——→LC	**JuMp Conditionally Direct** to location indicated by 8-bit (two hex digits) literal HH, if loop counter is *not zero. Loop Counter is decremented after the* test.
	JMPZ	04	DT	HH→PC if (A) = 0	**JuMP** to location specified if accumulator contents are **Z**ero as a result of previous instruction.
	JMPN	02	DT	HH→PC if (A)≥0	**JuMP** to location specified if accumulator contents are **N**egative as a result of previous instruction.
	JMPO	01	DT	HH→PC if (A) Overflows	**JuMP** to location specified if accumulator **O**verflows as a result of previous instruction. Clears overflow flag.
	JMIF	05	DT	HH→PC if IF = 0	**JuMp** if **I**nput **F**lag is low to location specified (Note 4). IRQ line will be set low if the SRI mode is not set.
	JMOF	06	DT	HH→PC if OF = 0	**JuMp** if **O**utput **F**lag is high to location specified (Note 4).
Subroutine Instruction	**JMSR**	0A	DT	(PC) + 1→RAR, HH→PC	**JuMp** to **SubR**outine. Execution jumps unconditionally to location indicated by 8-bit (two hex digits) literal HH. Return address is stored in RAR. Cannot be used with an OP1 instruction requiring specified address mode.
	RETN	0B	- - -	(RAR)→PC	**RET**ur**N** from subroutine. Execution continues at instruction following the JMSR instruction.
Complex Instructions	**JCDT**	13	DT	HH→PC if LC≠0 (LC)—1→LC (BAS) + 1→BAS, (IX) + 1→IX	**J**ump **C**onditionally **D**irect Dual **T**racking. Increment base and Index registers. Loop Counter is decremented after test.
	JCDI	17	DT	HH→PC if LC ≠0, (BAS) + 1→BAS (LC)—1→LC	Jump **C**onditionally **D**irect and **I**ncrement base register. *Loop Counter is decremented after test.*
	TVIB	1B	UV/US	(VP)→V/S, (BAS) + 1→BAS	**T**ransfer contents of VP register to RAM location **V**/S **I**ncrement **B**ase register.
	TAIB	19	UV/US, D	(A)→V/S (BAS) + 1→BAS	**T**ransfer **A**ccumulator contents into RAM location V/S and **I**ncrement **B**ase register.
	MODE	10	- - -	*Control mode* replaces OP1	*OP1 code in this instruction can select any one of* the several control **MODE**s/operations specified in Table 1.
	REPT	18	- - -	PC inhibited if LC≠0 (next instruction) (LC)—1→LC (each iteration of next instruction.)	**REP**eat next instruction until LC = 0. Increment PC to access next instruction, then suppresses increment of PC if LC≠0. Loop Counter is decremented when REPT is executed, so that number of repeats is equal to original value of LC.

NOTES:

1. Whenever the Index register is selected by an instruction OP2 it controls the entire line of code.
2. Loop Counter cannot underflow.
3. S refers to scratchpad.
4. Input flag is low if SPP has not received a new input word.
5. (A) represents truncation of the accumulator to 5 most significant bits (sign and 4 MSB).
6. Multiplier input latches and the VP register are not updated when either the DT or L addressing modes are used in conjunction with an OP2 instruction.
7. - - - indicates don't care address mode.
8. When D address mode is used, accumulator contents as a result of previous instruction replace U input to multiplier.

AMI

A Subsidiary of Gould Inc.

S28214

FAST FOURIER TRANSFORMER

Features

- ☐ Performs 32 Complex Point Forward or Inverse FFT in 1.3msec, Using Decimation in Frequency (DIF)
- ☐ Transform Expandable either by Using Multiple S28214s (for Minimum Processing Time) or by a Single S28214 (for Minimum Hardware)
- ☐ Operates with any 8- or 16-Bit Microprocessor
- ☐ μP-Compatible I/O Port i.e., 6800 (A version), Z80 (B version)
- ☐ Basic Resolution of 57dB. Optional Conditional Array Scaling (CAS) Routine Increases Dynamic Range to 70dB
- ☐ Optional Windowing Routine Incorporated to Permit Use of Arbitrary Weighting Function
- ☐ Coefficient Generation On Chip, with Rotation Algorithm for Transform Expansion up to 512 Points
- ☐ Optional Power Spectrum Computation

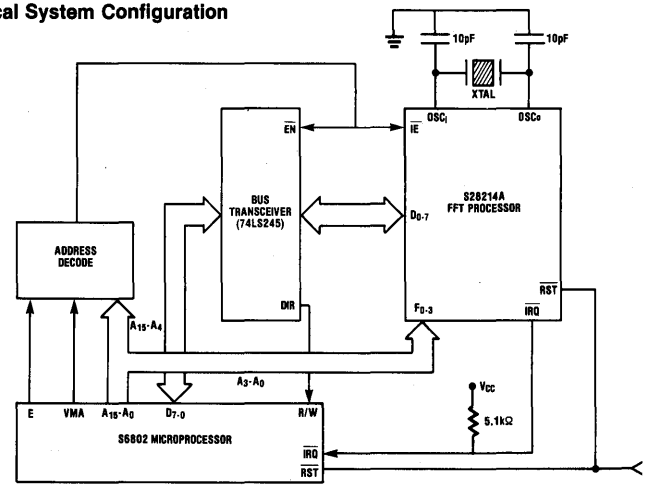
General Description

The AMI S28214 Fast Fourier Transformer is a preprogrammed version of the S28211 Signal Processing Peripheral.

For further information on the internal operation of the S28211, please refer to the S28211 Product Description.

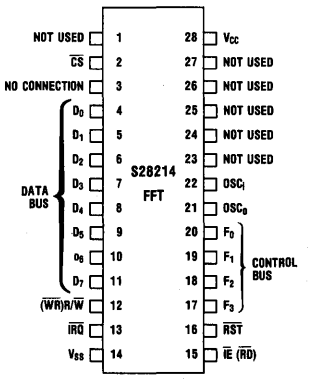
It calculates FFTs and IFFTs using a decimation in frequency (DIF) technique for minimum distortion. The S28214 calculates a 32 complex point FFT using internally generated coefficients in a single pass. A coefficient rotation algorithm allows larger FFTs to be implemented (in blocks of 32 points). This implementation may be carried out by successive passes of the data through the two main routines in the S28214, allowing larger transforms to be carried out with a single S28214. Alternatively, an array of S28214s may be used to increase the transformation speed by parallel processing.

Typical System Configuration



NOTES:
(1) S6802 AND S28214A USED IN THIS ILLUSTRATION
(2) SYSTEM MEMORY (RAM, ROM/EPROM) NOT SHOWN
(3) THE USE OF AT CUT XSTAL IS RECOMMENDED.

Pin Configuration



NOTE: PIN FUNCTIONS IN PARENTHESIS APPLY ONLY TO B VERSION

S28214 Pin Functions/Descriptions

Pin	Number	Function
D_0-D_7	4-11	(Input/Output) Bi-directional 8-bit data bus. Data is Two's Complement coded.
F_0-F_3	20-17	(Input) Control Function bus. Four Microprocessor address lines (typically A_0-A_3) are used to control the S28214.
$\overline{IE}$ or ($\overline{RD}$)	15	IE (S28214A): (Input) Interface Enable. A low level on this line enables data transfer on the data bus and control functions on the F-bus. Usually generated by microprocessor address decode logic. RD (S28214B): (Input) Read Data Strobe. A low level indicates a valid read cycle.
($\overline{CS}$)	2	(Input) Chip Select. LOW active.
R/$\overline{W}$ or ($\overline{WR}$)	12	R/W (S28214A): (Input) Read/Write Select. When HIGH, output data from the S28214 may be read, and when LOW data may be written into the S28214. WR (S28214B): (Input) Write Data Strobe. A low level indicates a valid write cycle.
$\overline{IRQ}$	13	(Output) Interrupt Request. This open drain output goes low when the S28214 has completed the execution of a routine and output data is available.
$\overline{RST}$	16	(Input) When LOW all registers and counters will be cleared, including the program counter, and all control functions cleared.
OSC_i, OSC_0	22, 21	Oscillator input and output. For normal operation a crystal is connected between these pins to generate the internal clock signals. Alternatively, an external square wave signal may be connected to OSC_i pin with OSC_0 pin left open.
V_{CC}	28	Positive power supply connection.
V_{SS}	14	Negative power supply connection. Normally connected to ground.

In addition to the above, pins 24-27 and 1 are connected to V_{SS} and Pin 23 is left open.

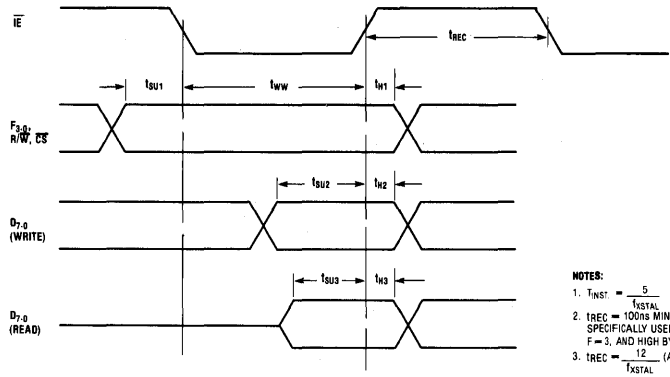
Absolute Maximum Ratings

Supply Voltage 7.0VDC
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +125°C
Voltage at any Pin ..... V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10sec.) ..... 200°C

Electrical Specifications (V_{CC} = 5.0V ± 5%; V_{SS} = 0V, T_A = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.0		V_{CC} + 0.3	V	V_{CC} = 5.0V
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	V_{CC} = 5.0V
I_{IN}	Input Logic Leakage Current		1.0	2.5	mA	V_{IN} = 0V to 5.25V
C_I	Input Capacitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	I_{LOAD} = −100mA, V_{CC} = min, C_L = 30pF
V_{OL}	Output LOW Voltage			0.4	V	I_{LOAD} = 1.6mA, V_{CC} = min, C_L = 30pF
f_{CLK} XSTAL	Max. Crystal Clock Frequency	5		16.66	MHz	V_{CC} = 5.0V
P_D	Power Dissipation			800	mW	V_{CC} = 5.0V

Figure 1. F-Control Bus and Read/Write Data Timing (S28214)



NOTES:
1. $T_{INST.} = \frac{5}{f_{XSTAL}}$
2. t_{REC} = 100ns MIN. (DURATION IN BETWEEN TWO IE STROBES SPECIFICALLY USED TO SET UP READ OR WRITE LOW BYTE, F = 3, AND HIGH BYTE, F = 2, VIA D_{0-7} LINES).
3. $t_{REC} = \frac{12}{f_{XSTAL}}$ (ALL CASES EXCEPT ONE INDICATED IN NOTE 2).

S28214 Timing Specifications (5V ± 5%, T_A = 0°C – 70°C)

Refer to Figure 1

Symbol	Min.	Typ.	Max.	Units	Comment
t_{WW}	100			ns	
t_{REC}	100 or $\frac{12}{f_{XSTAL}}$			ns	See Notes
t_{SU1}	25			ns	
t_{SU2}	25			ns	
t_{SU3}	30			ns	
t_{H1}	10			ns	
t_{H2}	10			ns	
t_{H3}	10			ns	

Functional Description

The S28214 is a high speed microcomputer organized for efficient signal processing and contains a data memory, instruction memory, an arithmetic unit incorporating a 12-bit parallel multiplier, as well as control registers and counters.

The Instruction ROM contains the various routines; the names and starting addresses of which are shown in Table 1A.

The Data ROM contains the coefficients required to execute the functions. 256x16 of Data RAM is provided, (128x16) of RAM to be used at a time; to hold the 32 point complex signal data during processing, as well as the power spectrum of the output and various other parameters, including the total number of points in the desired transform. The memory is organized as a 32x4 matrix, with the data arranged in columns, as shown in Table 1B. Refer to Table 2 for various page mode selections between the two (128x16) Data RAM sections and coefficient ROM.

The word length used in the S28214 gives the transformed data a resolution of up to 57dB, but the total dynamic range can be increased up to 70dB by using the Conditional Array Scaling (CAS) routine incorporated.

The S28214 is intended to be used in a microprocessor system using an 8- or 16-bit microprocessor, ROM, RAM and an optional DMA Controller or Address Generator. The S28214 is used as a memory mapped peripheral, and should be assigned a block of 16 addresses. It is used as a "hardware subroutine" function. The microprocessor controls the flow of data, including I/O, and calls the routines in the S28214 to cause the FFT to be executed. The S28214 responds to the microprocessor with the $\overline{IRQ}$ line when the processing of each routine is completed. In the case of a 32 point transform this signifies the completion of the transform, and in larger transforms it signifies that the microprocessor should unload the output data, load the next input data and call te next routine to be executed. The data is stored externally in RAM. Input data to be transformed is loaded into displacements 0 and 1 of the S28214 data memory. At the end of the FFT routine output data overwrites the input data. If power spectrum flag (PSF) is set, the S28214 computes the sum of the squares of the real and imaginary components of the output data and places the result in displacement 3 of the data memory. Both complex FFT data and power spectrum data are thus available. Windowing weights may be loaded into the S28214 prior to processing if the windowing routine is to be used. A 6800 compatible source listing of a suitable control program is available to the S28214 user at no charge.

Figure 2. Simplified Block Diagram of S28214

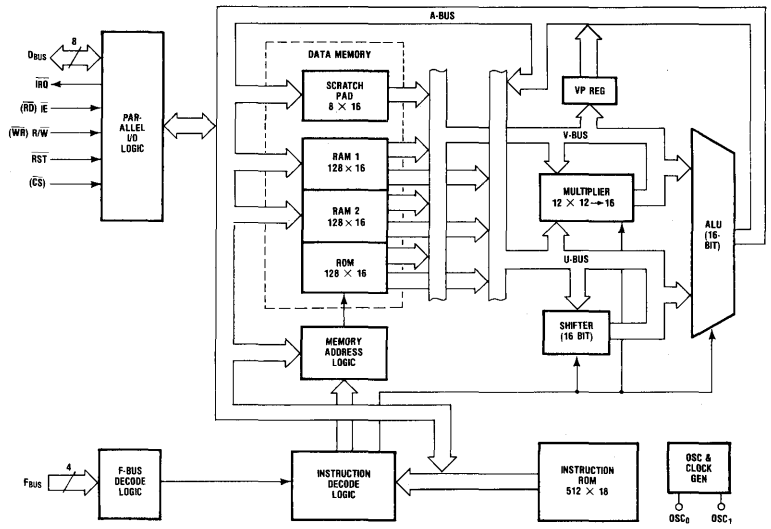


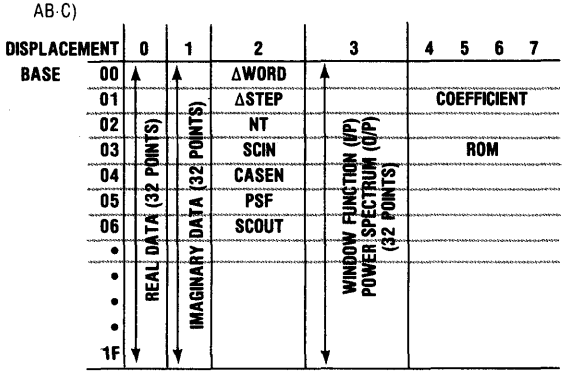
Table 1. Software Model of S28214

A. Routine Locations in Instruction Memory

LOC (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY PT. "INIT" ROUTINE
04	ENTRY PT. "FFT32" ROUTINE
D3	ENTRY PT. "COMPAS" ROUTINE
EA	ENTRY PT. "SCALE" ROUTINE
DC	ENTRY PT. "WINDOW" ROUTINE
E4	ENTRY PT. "CONJUG" ROUTINE

B. Data Memory Map

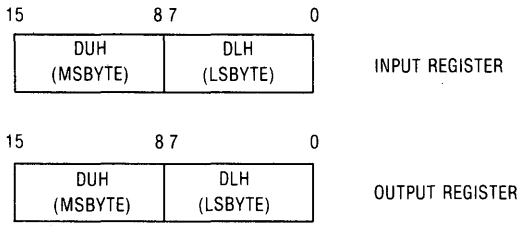
(Note: Address [Base AB, Displacement C] is written as AB·C)



C. Control Functions

F-BUS (HEX)	MNEMONIC	FUNCTION
1	RST	RESETS CHIP
2	DUH	SELECTS MSBYTE
3	DLH	SELECTS LSBYTE
4	XEQ	STARTS EXECUTION
9	BLK	SELECTS BLOCK MODE
F	NOR	SET PAGE MODES (SEE TABLE 2)
F	ROM	
E	RAM	

D. Input and Output Registers



CODE IS TWO'S COMPLEMENT.

NOTE: A DUH BYTE MAY BE LOADED WITHOUT A DLH, BUT THE REVERSE CANNOT BE DONE.

The Control Functions

The S28214 is controlled by the host microprocessor by means of the F-bus, Interface Enable ($\overline{IE}$) and the Read-Write (R/$\overline{W}$) lines.

The 12 most significant address lines decode a group of 16 addresses to activate the $\overline{IE}$ line each time an address in the group is called, and the S28214 is controlled by reading to or writing from those addresses. Only 8 of these addresses are used as described in Table 2. Throughout this Product Description these addresses will be referred to as NNNX (X = 0-F).

Table 2: S28214 Control Functions

MNEMONIC	F-BUS HEX	DATA	TYPE OF OPERATION	FUNCTION
RST	1	XX	READ/WRITE	CLEARS ALL REGISTERS. STARTS PROGRAM EXECUTION AT LOCATION 00. THIS IS THE IDLE STATE. THIS INSTRUCTION SHOULD PRECEDE BLOCK READ, BLOCK WRITE AND EXECUTE COMMANDS.
DUH	2	HH	READ/WRITE	READS FROM OR WRITES INTO S28214 THE UPPER HALF OF THE DATA WORD. (SEE TABLE 1.D.)
DLH	3	HH	READ/WRITE	READS FROM OR WRITES INTO S28214 THE LOWER HALF OF THE DATA WORD. (SEE TABLE 1.D)
XEQ	4	HH	WRITE	STARTS EXECUTION AT LOCATION HH
BLK	9	XX	READ/WRITE	INITIATES A BLOCK READ OR BLOCK WRITE OPERATION. THE ENTIRE DATA RAM CAN BE ACCESSED SEQUENTIALLY BEGINNING WITH VALUES OF BASE AND DISPLACEMENT INITIALIZED USING "BLOCK TRANSFER SET UP" ROUTINE. IF A RESET OPERATION IS PERFORMED PRIOR TO BLOCK COMMAND THE DATA MEMORY ADDRESS IS INITIALIZED TO BASE 0, DISPLACEMENT 0. BLOCK READ OR WRITE OPERATION CAN BE TERMINATED ANY TIME BY PERFORMING A RESET OPERATION. THE INDEX REGISTER IS USED TO ADDRESS THE MEMORY DURING BLOCK TRANSFER AND INTERNAL ADDRESSING IS SEQUENCED AUTOMATICALLY.
NOR	F	XX	READ	SET PAGE MODE NORMAL. RAM1 + ROM. THIS IS ALSO DEFAULT MODE AT RESET.
ROM	F	XX	WRITE	SET PAGE MODE TO RAM2 + ROM.
RAM	E	XX	READ	SET PAGE MODE TO RAM1 + RAM2

NOTE: XX = Don't care
HH = 2 Hex characters (8-bit data)

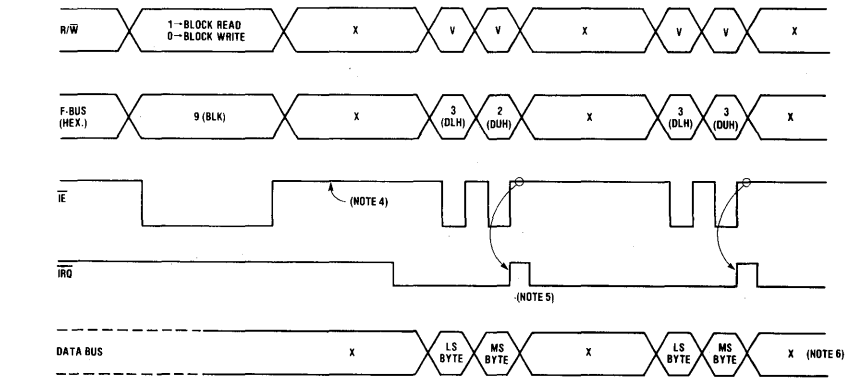
Initial Set-Up Procedure

After power up, the $\overline{RST}$ line should be held low for a minimum of 300nsec. If this line is connected to the reset line of the microprocessor this condition will be met easily. This will clear the Base and Index Registers, which are used for memory addressing, the Loop Counter and the Program Counter. Address zero in the Instruction ROM contains a Jump to Zero instruction, and thus the S28214 will remain in an idle state after being reset. Every routine in the memory is also terminated with a Jump to Zero instruction, and thus the S28214 will also remain in this same idle state after the execution of each routine. The $\overline{IRQ}$ line will signal this condition each time (except after the initial reset).

The Block Transfer Operation

Block transfer is the mode used to load and unload the main data blocks into the S28214 at up to 4Mbytes/sec. In this mode the data memory is addressed by the Index Register, and after initialization the internal addressing is sequential and automatic. The sequence generated is that after each word transfer (16-bit words as 2 bytes, or 8-bit words as MSbyte (DUH) only) the base is incremented. After base 1F (31) has been reached, the base resets to 00 and the displacement increments. After base 1F displacement 3 has been reached (i.e., the highest address in the RAM, 1F.3), both base and displacement reset to zero. Note that when the BLK command is given the Read/Write line is latched internally, and remains latched until the RST command is given. The block transfer sequence and timing are shown in Figure 3.

Figure 3. Block Transfer Sequence and Timing



NOTES: (1) X = DON'T CARE OR NOT VALID, V = VALID
(2) TIMING SHOWN ABOVE IS NOT NECESSARILY TO SCALE. REFER TO FIGURE 1 FOR SPECIFICATIONS.
(3) PULL UP RESISTOR ON $\overline{IRQ}$ PIN ASSUMED IN THE ABOVE ILLUSTRATION.
(4) IF INTERRUPT HANDSHAKE IS USED BETWEEN S28214 AND PROCESSOR, INTERRUPT MASK MAY BE CLEARED HERE.
(5) $\overline{IRQ}$ TRANSITIONS DUE TO INTERNAL STATUS OF IR/OR IN S28214.
(6) READ OR WRITE CYCLES TO CONTINUE UNTIL RESET (USING F = 1).

In 6800 Assembly Language a Block Write would be executed with the following code:

```
LDX     OFFST     ;LOAD MEMORY START ADDRESS INTO INDEX REG.
STA     A BLK     ;WRITE DUMMY DATA TO ADDRESS $NNN9,BLOCK MODE.
LDA     A 0,X     ;READ FIRST BYTE FROM MEMORY.
STA     A DLH     ;WRITE INTO S28214 AS LSBYTE. ADDRESS $NNN3
LDA     A 1,X     ;READ SECOND BYTE FROM MEMORY.
STA     A DUH     ;WRITE INTO S28214 AS MSBYTE.ADDRESS $NNN2
LDA     A 2,X     ;SECOND WORD.
 .         .           .
 .         .           .
 .         .           .
LDA     A 62,X    ;32ND. WORD,LSBYTE.
STA     A DLH     ;
LDA     A 63,X    ;32ND. WORD,MSBYTE.
STA     A DUH     ;END OF TRANSFER.
STA     A RST     ;WRITE DUMMY DATA TO ADDRESS $NNN1.RESET.
```

Block Read would be executed by substituting LDA A for STA A, and vice versa.

where:

```
RST     EQU $NNN1
DLH     EQU $NNN3
DUH     EQU $NNN2
BLK     EQU $NNN9
```

The above code assumes that the block transfer is controlled by the host processor, not using DMA. Note that DLH must always precede DUH. 8-bit data may be transferred using DUH only, assuming that the significance of the data is correct.

The FFT Routines

Six individual routines are stored in the S28214 Instruction memory. Two or more of these are used in the computation of an FFT, depending on the transform size and the options selected. The starting addresses of the routines are shown in Table 3.

Selection of a particular sequence of routines will depend on the user's transform requirements and the function of each routine is covered later in this section. However general outline of the routines is given below.

1. **Block Transfer Set-Up (INIT)** — Presets the Index Register which controls addressing of the data memory.
2. **FFT32** — The output of this routine is the FFT. It can be used once for 32 point transform or more than once for larger transforms.
3. **COMPAS** — Decomposes larger transforms into blocks for execution by FFT32.
4. **SCALE** — A routine which ensures uniformity of scaling for data transformed during previous, present and subsequent passes.
5. **WINDOW** — Allows each data point to be multiplied by a weighting coefficient, thus accounting for the finite sample period.
6. **CONJUG** — Conjugates input data

Table 3. FFT Routines and Their Starting Addresses

LOCATION (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY POINT FOR "INIT" ROUTINE
	(IR) = BASE, DISPLACEMENT
	$(BASE)_{4-0} \leftarrow (IR)_{15-11}, (DISP)_{1,0} \leftarrow (IR)_{9,8}$
	Returns to Idle state (IRQ not set after execution of INIT Routine) Exec. Time = 0.9μs
04	ENTRY POINT FOR "FFT32" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP2) = SCIN, CASEN, PSF
	Perform 32 point FFT. Sets IRQ, Returns to Idle state. Exec. Time = 1.2 ms to 1.8ms.
	(OR) = SCOUT (DISP0) = Transformed Data (Real), (DISP1) = Transformed Data (Imag.) (DISP2) = SCOUT, (DISP3) = Power Spectrum Data if PSF = 1
D3	ENTRY POINT FOR "COMPAS" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP2) = WORD, STEP, NT, SCIN, CASEN
	Perform COMPAS, Sets IRQ, Returns to Idle State Exec. Time = 233 to 374μsec.
	(DISP0) = Output Data (Real), (DISP1) = Output Data (Imag.) (DISP2) = SCOUT, (OR) = SCOUT
EA	ENTRY POINT FOR "SCALE" ROUTINE
	(IR) = SCIN, (DISP0) = Data (Real), (DISP1) = Data(Imag.)
	Performs scaling, Sets IRQ. Returns to Idle State Exec. Time = 51 to 250μsec.
	(DISP0) = Scaled Data (Real), (DISP1) = Scaled Data (Imag.)
DC	ENTRY POINT FOR "WINDOW" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP3) = Multiplying Factors
	Performs multiplication, Sets IRQ, Returns to Idle State Exec. Time = 49μsec.
	(DISP0) = Output Data (Real), (DISP1) = Output Data (Imag.)
E4	ENTRY POINT FOR "CONJUG" ROUTINE
	No set-up required. Conjugates input data (negates imaginary components). Sets IRQ. Returns to Idle State. Exec. time = 30μsec.

NOTE: ABOVE EXECUTION TIMES DO NOT INCLUDE DATA TRANSFER.

1. Block Transfer Set-Up (INIT). Entry Address 01.

This routine presets the Index Register to allow block transfer to commence at any location other than 00.0 in the S28214 data RAM. An eight-bit word is loaded into the upper half of the input register and the routine executed as shown:

```
DUH     EQU $HHH2       ;
XEQ     EQU $HHH4       ;
LDA     A #$XX          ; Load start address for block transfer
STA     A DUH           ; Write into S28214 as MS Byte
LDA     A #1            ; Load start address for 'INIT' Routine
STA     A XEQ           ; Execute INIT
```

where XX represents the start address for block transfer. The routine will be executed in 3 instruction cycles (0.9msec.) and the S28214 will return to the idle state. Block transfer may then commence immediately.

2. FFT32. Entry Address = 04.

This is the basic 32 complex point FFT routine. For a 32 point FFT this routine is called once only and the output of the routine is the FFT. Larger FFTs are computed by decimating them into 32 point arrays before final processing of these arrays using FFT32 to obtain the final outputs. The following data is loaded into the S28214, using block write starting at address 00.0, i.e., INIT is not used.

32 words of real input data (addresses 00.0 – 1F.0)

32 words of imaginary input data (addresses 00.1F – 1F.1)

3 dummy words (to skip addresses) (addresses 00.2 – 02.2)

SCIN (input scaling parameter) (address 03.2)

CASEN (CAS Enable) (address 04.2)

PSF (Power spectrum flag) (address 05.2)

Note that CASEN (Conditional array scaling enable) and PSF are not modified during processing, and need only be loaded once. CASEN should be positive to inhibit CAS (e.g. 0000) and negative to enable CAS (e.g. 8000). Note that SCIN is not needed if CAS is not enabled. PSF should be zero if the power spectrum output is not needed, any non-zero value (e.g. 0100) will cause the power spectrum to be computed. The block transfer should be terminated with the RST command, and the FFT32 routine called. Flow charts for loading and dumping the data are shown in Figure 4. The following sequence will cause the execution of the entire function:

```
CLR     B               ;CLEAR B ACC.
STA     A RST           ;RESET S28214 REGISTERS.
SEI                     ;SET INT. MASK.
STA     A BLK           ;SET UP BLOCK WRITE.
JSR       BLKWT         ;WRITE 64 WORDS OF DATA.
STA     A DUH           ;WRITE DUMMY DATA TO 00.0
STA     A DUH           ;.....TO 00.1
STA     A DUH           ;.....TO 00.2
LDA     A SCIN          ;FETCH SCIN.
STA     A DLH           ;WRITE TO ADDRESS 00.3
STA     B DUH           ;COMPLETE WORD XFER.
LDA     A CASEN         ;FETCH CAS ENABLE.
STA     A DUH           ;WRITE TO ADDRESS 00.4
LDA     A PSF           ;FETCH PS FLAG.
STA     A DUH           ;WRITE TO ADDRESS 00.5
STA     A RST           ;RESET S28214.
LDA     A #4            ;FFT32 START ADDRESS.
STA     A XEQ           ;START EXECUTING.
CLI                     ;CLEAR INT. MASK.
WAI                     ;WAIT FOR ROUTINE END.
LDA     A DLH           ;START OF INT. ROUTINE.
LDA     B DUH           ;(DUMMY).READ SCOUT.
LDA     B SCIN          ;FETCH SCIN.
STA     A SCIN          ;SCOUT]SCIN
SBA                     ;COMP.SCOUT WITH SCIN.
BEQ       READ          ;JUMP IF NO CHANGE.
STA     A SCLP          ;(SCOUT-SCIN) ] SCLP
LDA     A PASSN         ;FETCH PASS #
CMP     A #1            ;IS THIS 1ST.PASS?
BEQ       READ          ;IF SO, JUMP
JSR       SKOUT         ;SCALE PREVIOUS ARRAYS
LDA     A #3            ;(ASSUME PSF SET.)
STA     A DUH           ;PRESET TO ADDRESS 00.3
LDA     A #1            ;
STA     A XEQ           ;EXECUTE INIT.
STA     A BRV           ;TURN ON BIT REV.MUX.
LDA     A BLK           ;SET UP BLOCK READ.
JSR       BLKRD         ;READ DATA.
STA     A RST           ;END
```

The routine execution time is variable, depending on whether CASEN and PSF are set. The times are:

1. CAS-OFF. PSF-OFF 3730 instruction cycles (1.119msec.)
2. CAS-OFF. PSF-ON 3862 instruction cycles (1.159msec.)
3. CAS-ON . PSF-OFF 5867max. instruction cycles (1.760msec.)
4. CAS-ON . PSF-ON 5999max. instruction cycles

When CAS is enabled, the time depends on the number of times overflow is corrected. At the end of the routine the complex output data will have overwritten the input data in the memory (addresses 00.0 to 1F.1) and the power spectrum data will be in displacement 3 (addresses 00.3 - 1F.3). The output scaling factor (SCOUT) will be loaded in the output register, generating the $\overline{IRQ}$ to signify to the host processor that the routine has completed processing.

Figure 4A. Flowchart for Subroutine FT32IN

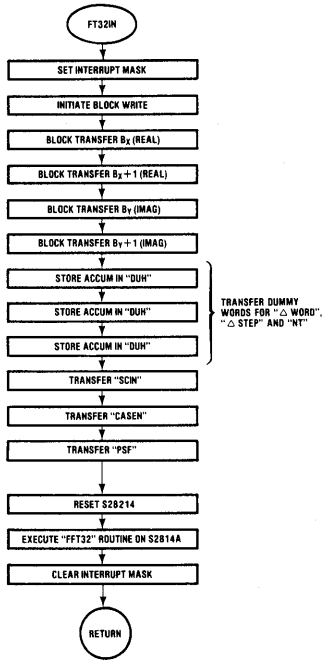
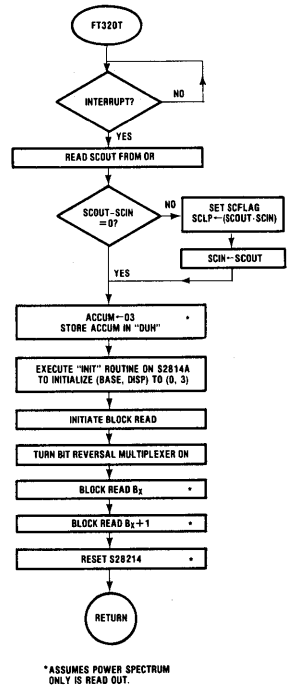


Figure 4B. Flowchart for Subroutine FT32OT



3. Combination Pass Routine, COMPAS. Entry Address = D3.

This is the decomposition routine that breaks up larger transforms into a number of 32 point transforms to be executed by FFT32. The N data points are split into N/16 blocks of 16 points, and pairs of blocks are passed through COMPAS. The procedure is repeated one or more times if N is greater than 64, but for a 64 point FFT the resulting data is ready for processing using FFT32. The procedure is explained in greater detail in the section "Executing Larger Transforms". The following data is loaded into the S28214 before execution:

32 words of real input data (addresses 00.0 - 1F.0)
32 words of imaginary input data (addresses 00.1-1F.1)
Δ WORD (address 00.2)
Δ STEP Set up parameters (address 01.2)
NT (address 02.2)
SCIN (address 03.2)
CASEN (address 04.2)
PSF (address 05.2)

The new parameters required, D WORD, D STEP and NT are dependent on the size of the transform and D WORD changes with each pass through the COMPAS routine. The values required are shown in the tables in sections "Executing 64 Point Transforms" and "Executing Larger Transforms". Flow charts for loading and dumping the data are shown in Figure 5. The routine execution time varies with transform size and depends on whether CAS is enabled or not, as shown:

TRANSFORM SIZE	64 POINT	128 POINT	256 POINT	512 POINT
Without CAS, Inst. cycles, (msec.)	776 (233)	828 (248)	842 (253)	949 (255)
With CAS. (Max.) Inst. cycles (msec.)	1172(352)	1224(367)	1238(371)	1245(374)

4. Data Point Scaling Routine, SCALE. Entry location = EA.

If CAS is enabled, then routines COMPAS, and FFT32 will scale all 32 data points being processed if an overflow occurs during that pass. The value of SCOUT allows the data during subsequent passes to be scaled automatically during the pass. However, data points which have already been processed must also be scaled, so that all the data is scaled by the same factor during each processing step. SCALE is a routine that allows this to be done at high speed. Each block to be scaled is block loaded into the S2814A, the routine SCALE executed, and the block dumped back into the original locations in memory.

Care must be taken to keep track of which blocks have already been processed during each step, so that blocks do not get missed or scaled twice. The execution time depends on the scaling factor (SCOUT), as shown below:

Scaling Factor (SCOUT)	**1**	**2**	**3**	**4**	**5**
Execution time. Inst. Cycles, (msec.)	170(51)	336(101)	502(151)	668(200)	834(250)

Figure 5A. Flowchart for Subroutine CSIN

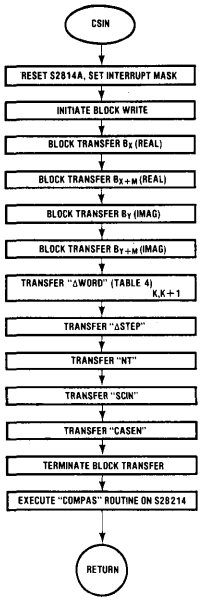
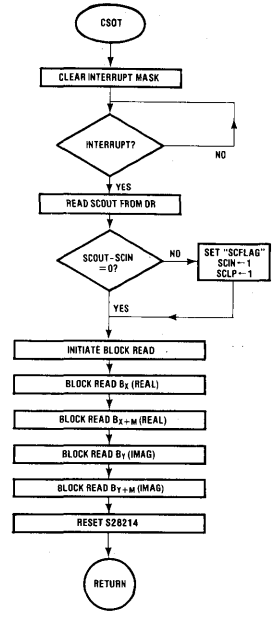


Figure 5B. Flowchart for Subroutine CSOT



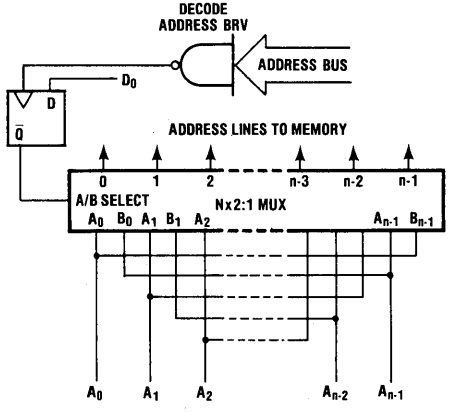
5. Windowing Routine, WINDOW. Entry Address = DC

In order to allow the input data points to be windowed, a routine is provided to multiply the 32 real or complex points loaded in the S28214 by 32 window points. This is done on each block of 32 points prior to commencing the actual FFT processing. The input data required, in addition to the normal input data, are the 32 points of the window. They should be loaded into displacement 3 of the S28214 RAM and the routine WINDOW executed. The windowed data points will be returned to their original positions in the memory, so that COMPAS or FFT32 may then be executed immediately without further processing. The entire data can be loaded in a single block transfer operation by using INIT to preset the start address to 00.3. The 32 point window data is then loaded, followed by the signal data. This is possible because after loading the window the memory address will automatically reset to 00.0, the start address for the real data. The parameters are then loaded into displacement 2 addresses in the usual way. They will not be affected by the windowing operation. The total execution time is 163 instruction cycles, 49msec.

Executing FFTs

Executing the FFTs consists of loading data blocks, executing routines in the S28214 and dumping the data. However, the sequence of the FFT output data is scrambled, and in order to use the results meaningfully, it must be unscrambled. This is done by reversing the order of the bits of the address lines for the final output data. Thus, for a 2^N point FFT the N address lines A_0, A_1, A_2 ..... A_{N-1} must be reversed to the sequence A_{N-1}, A_{N-2} ..... A_1, A_0 to address the output buffer memory. This is most conveniently done as the data points are being dumped out of the S28214 after the processing of the FFT32 routine(s). The bit reversal can be done either by software or hardware. The hardware realization is shown in Figure 6, and an example of software bit reversal is given in the section "Executing 32 Point Transforms."

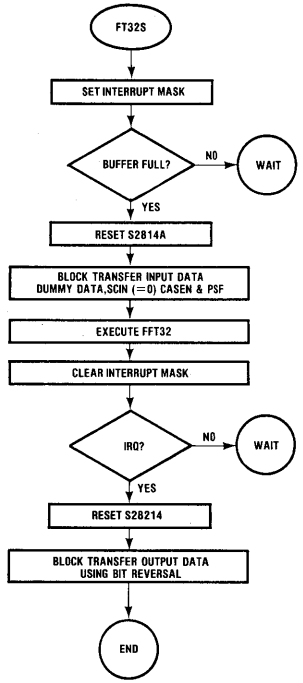
Figure 6. Bit Reversal Hardware



Executing 32 Point Transforms

The basic 32 point transform is easily implemented with the S28214 since it simply requires the loading of the 32 real or complex data points and the 3 parameters SCIN, CASEN and PSF, executing FFT32 once only and dumping the data using bit reversal. The flowchart for this sequence is shown in Figure 7. It is assumed that the loading of data from the source into the input buffer and dumping of data from the output buffer to destination is carried out by the microprocessor NMI (non-maskable interrupt) routine. The parameter SCIN should be set to zero, and the output data should be scaled (multiplied) by $2^{(SCOUT)}$ if absolute levels are wanted.

Figure 7. Flowchart for 32 Point FFT



COMMUNICATION PRODUCTS

Executing 64 Point Transforms

This is the simplest expansion of the FFT. The first step is to use COMPAS (twice) to decimate the data into two 32 point transforms, and then use FFT32 (twice) to produce the transforms. This is shown in the signal flow graph in Figure 8. The flow graph is independent of whether one or two S28214s are used, since the two passes through each of the 2 routines (COMPAS and FFT32) can be carried out sequentially or in parallel.

The set up parameters for the 64 point FFT are:

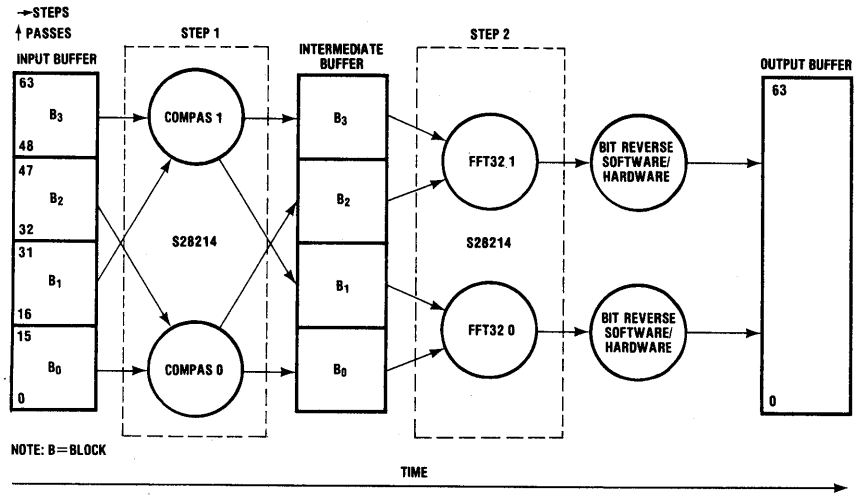
For COMPAS 0: ΔWORD = 8070
ΔSTEP = 4000 NT = 0001

For COMPAS 1: ΔWORD = C070

The treatment of SCIN and SCOUT is dealt with in the next section.

Note: All values in Hex.

Figure 8. 64 Point FFT Flowgraph



Executing Larger Transforms

The execution of larger transforms follows the same sequence as the 64 point transforms: namely the decimation of the data into a series of 32 point blocks that can be processed using FFT32. For a 2^N point FFT this involves N-5 steps of processing using COMPAS, and each step requires $2^{(N-5)}$ passes through the COMPAS routine. This is followed by $2^{(N-5)}$ passes through the FFT32 routine. Within each step, each pass may be carried out sequentially using a single S28214, or in parallel using $2^{(N-5)}$ chips. There are also intermediate sequential + parallel combinations possible, of course, using fewer chips. A signal flow graph for 1 step is shown in Figure 9.

At the start of each step, SCIN should be set to zero. For the remaining passes in that step the value of SCOUT for the current pass should be used for SCIN for the next pass. The outputs of previously computed passes must be scaled using routine SCALE each time SCOUT increases during a pass. The maximum value of SCOUT after executing COMPAS is 1, and after executing FFT32 it is 5.

A flow chart for an N point transform control program is shown in Figure 10. The routine is called NFFT and uses the following subroutines:

CSIN — procedure for loading S28214 with COMPAS input data (Figure 5A)

CSOT — procedure for dumping COMPAS output data (Figure 5B)

SCLPRV — procedure for scaling previously computed blocks of data in each step. See Figure 10.

FT32IN — procedure for loading S28214 with FFT32 input data (Figure 4A)

FT32OT — procedure for dumping FFT32 output data (Figure 4B)

The values of ΔWORD, ΔSTEP and NT are shown in Tables 4 and 5.

Figure 9. N Point FFT Flowgraph

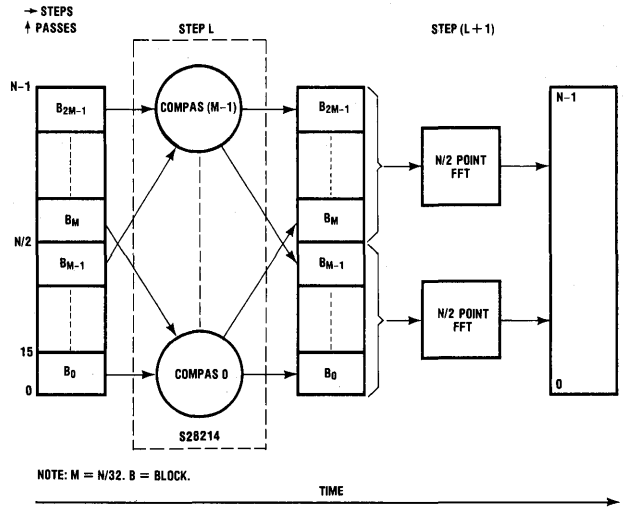
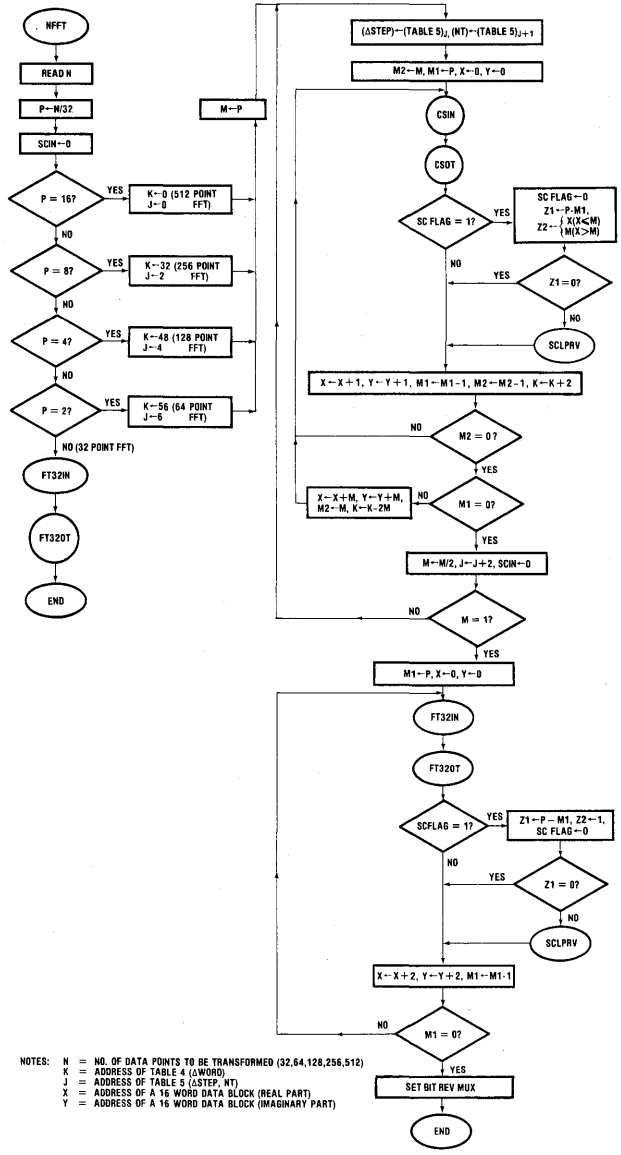


Figure 10. Flow Chart for N Point FFT, Routine "NFFT"



NOTES: N = NO. OF DATA POINTS TO BE TRANSFORMED (32,64,128,256,512)
X = ADDRESS OF TABLE 4 (ΔWORD)
J = ADDRESS OF TABLE 5 (ΔSTEP, NT)
X = ADDRESS OF A 16 WORD DATA BLOCK (REAL PART)
Y = ADDRESS OF A 16 WORD DATA BLOCK (IMAGINARY PART)

Figure 11. Flow Chart for Subroutine "SCLPRV"

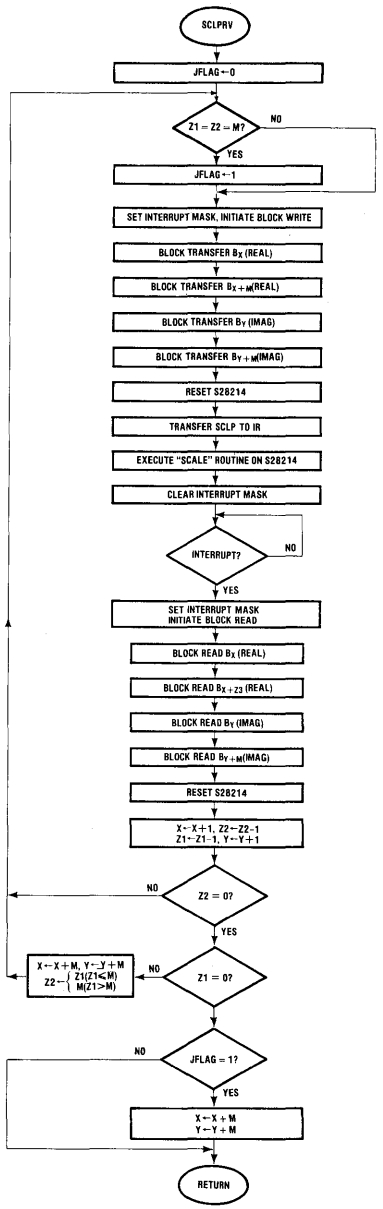


Table 4. (ΔWORD)

ENTRY PT for	K	VALUE	COMMENTS
512→	0	00	(ΔWORD L)
point	1	80	(ΔWORD H)
x'form	2	00	
	3	88	
	4,	00	
	5	90	
	6	00	
	7	98	
	8	00	
	9	A0	
	10	00	
	11	A8	
	12	00	
	13	B0	
	14	00	
	15	B8	
	16	00	
	17	C0	
	18	00	
	19	C8	
	20	00	
	21	D0	
	22	00	
	23	D8	
	24	00	
	25	E0	
	26	00	
	27	E8	
	28	00	
	29	F0	
	30	00	
	31	F8	
256 →	32	10	
point	33	80	
x'form	34	10	
	35	90	
	36	10	

Table 4. (Continued)

ENTRY PT for	K	VALUE
	37	A0
	38	10
	39	B0
	40	10
	41	C0
	42	10
	43	D0
	44	10
	45	E0
	46	10
	47	F0
128 → point x'form	48	30
	49	80
	50	30
	51	A0
	52	30
	53	C0
	54	30
	55	E0
64 → point x form	56	70
	57	80
	58	70
	59	C0

Table 5. (ΔSTEP, NT)

ENTRY PT for	J	VALUE	COMMENTS
512 point	0	08	ΔSTEP(DUH)
x'form	1	0F	NT(DLH)
256	2	10	"
	3	07	"
128	4	20	"
	5	03	"
64	6	40	"
	7	01	"

NOTE: FOLLOWING LOADING OF THE N.T. BYTE, A DUMMY DUH MUST BE LOADED TO COMPLETE WORD LOADING, OTHERWISE THE S28214 DOES NOT RECOGNIZE THE COMPLETION OF THE TRANSFER.

Hardware

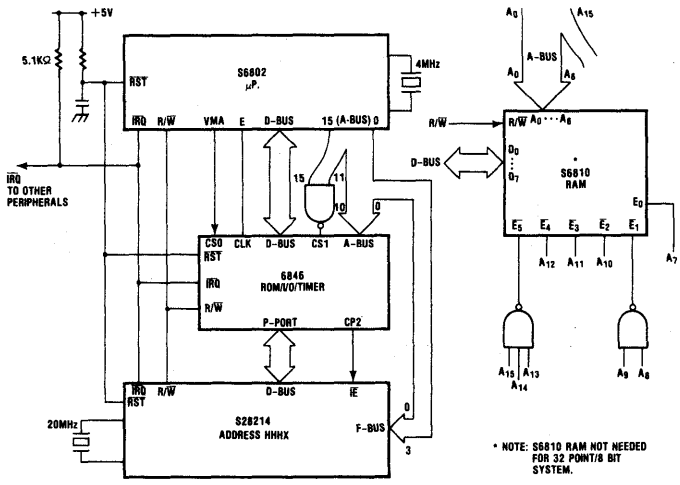
Hardware for a 32 point FFT is shown in Figure 12. All data transfer and control is handled by the S6802. A suitable analog interface is shown in Figure 13. The sampling clock is derived from the microprocessor clock, and the NMI signal is generated by the EOC (end of conversion) output of the A/D converter. The availability of the next input sample is signalled with the NMI line.This system may be expanded simply by adding more memory. The memory requirements are shown in Table 6. A word may be up to 16 bits long. In order to speed up the complete procedure it is necessary to use DMA for block transfer of data. The S28214 will transfer data at up to 4Mbytes/sec.

Table 6. Memory Requirements for Data Point Storage

TRANSFORM SIZE (POINTS)	WORD LENGTH (BITS)	MEMORY REQUIREMENTS
32	8	64 bytes
	10/12	See Note 1
	16	128 bytes
64	8	128 bytes
	10/12	See Note 1
	16	256 bytes
128	8	256 bytes
	10/12	768 nibbles
	16	1024 bytes
256	8	512 bytes
	10/12	1536 nibbles
	16	1024 bytes
512	8	1024 bytes
	10/12	3072 nibbles
	16	2048 bytes

Note 1: In practice the memory realization for these cases will be the same as for 16-bit systems.

Figure 12. 32/64 Joint FFT Hardware



Data Bus Interface

Figure 14 shows how to interface the S28214 with a typical 6800 family microprocessor data bus. Note that the data bus must be isolated from the microprocessor system data bus by use of a PIA as in Figure 12 or a 74LS245 or 74LS645 type data transceiver as shown in Figure 14, since the S28214 drive capability is only one TTL load. The bus isolation may be omitted in some small systems. A simplified interface between S28214B with a Z-80 microprocessor type bus is shown in Figure 15 (see page 20).

Figure 13. Analog Interface

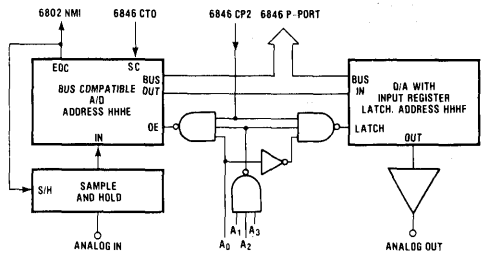


Figure 14. Interfacing the S28214A with a Microprocessor

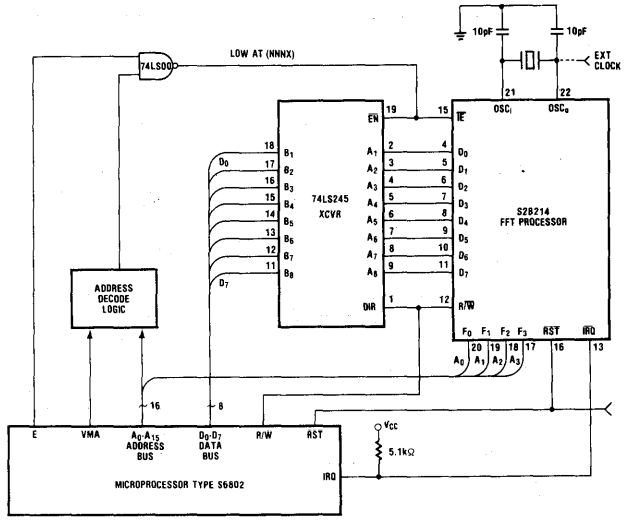
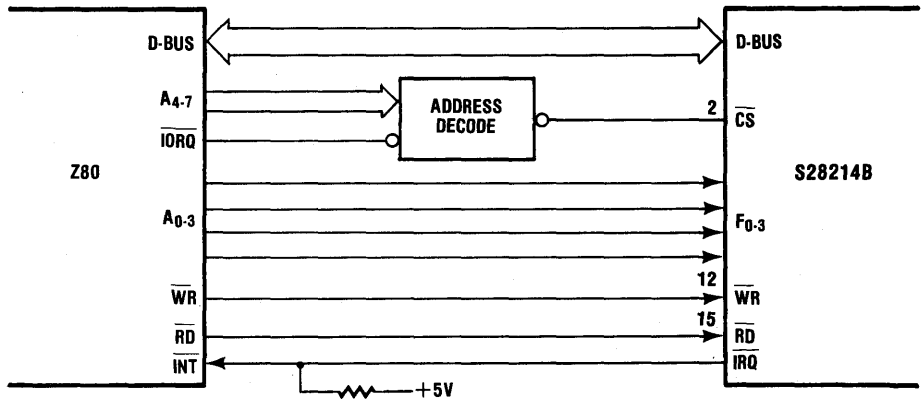


Figure 15. Interfacing S28214B to Z80 Microprocessors



FFT Resolution and Dynamic Range

The use of the Decimation in Frequency (DIF) algorithm in the S28214 ensures optimum signal to noise ratio, (SNR) for the architecture used. The use of the Conditional Array Scaling (CAS) gives a total dynamic range of approximately 70dB on all sizes of Transforms. The maximum resolution obtainable is approximately 57dB. CAS operates by detecting overflow in the butterfly computation routine. As soon as an overflow is detected the two points being combined in that butterfly are halved in magnitude (both the real and imaginary portions) and the butterfly recomputed. A flag is set, all previously computed butterfly outputs are then scaled, and all the inputs to subsequent butterflies are scaled before computation begins, so that at the end of the pass all points have been scaled equally. A scale factor is made available (SCOUT) so that the remaining data points in larger transforms, i.e., those other than the 32 in the S28214 when the overflow occurred, may also be scaled to keep them all in line. Thus, CAS operates as a discrete AGC, halving the signal levels each time an overflow is detected. By using SCOUT after executing the FFT the output may be expanded, so that the levels displayed in the spectrum will increase monotonically as the input increases.

AMI
A Subsidiary of Gould Inc.

Advanced Product Description **S28215**

DIGITAL FILTER/UTILITY PERIPHERAL

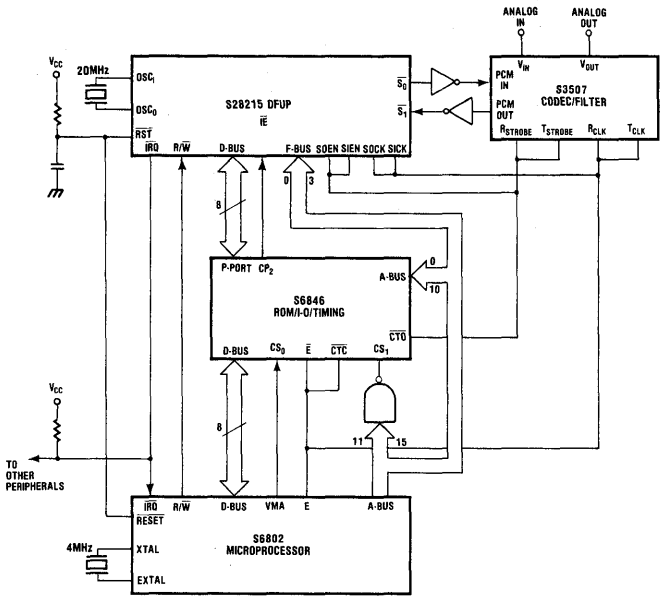
Features

- ☐ S28211 Signal Processing Peripheral Programmed With Filter and Utility Routines
- ☐ Microprocessor Compatible Interface Plus Asynchronous Serial Interface
- ☐ Two Independent 32 Tap Transversal Filter Routines, Cascadable into a Single 60 Tap Filter
- ☐ Two Recursive (biquadratic) Filters Providing a Total of 16 Filter Sections
- ☐ Computation Functions: Two Integrating, Two Rectifying, Squaring, and Block Multiply Routines
- ☐ Conversion Functions: μ255 Law-to-Linear, Linear-to-μ255 Law, and Linear-to-dB Transformations
- ☐ Generator Functions: Sine and Pseudo-Random Noise Patterns
- ☐ μP-Compatible I/O Port; i.e. 6800 (A Version), 8080 (B Version)

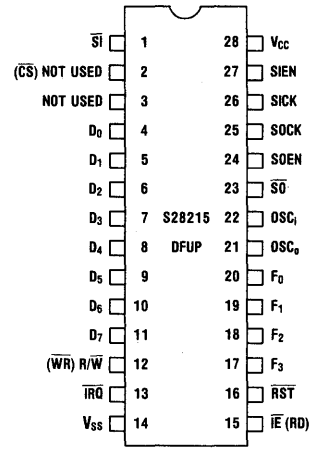
General Description

The AMI S28215 Digital Filter/Utility (DFUP) is a pre-programmed version of the S28211. Architectural and internal operating details of the S28211 may be found in the S28211 Advanced Product Description. The S28215 has been programmed with a collection of filter, computational, conversion, and generator routines which may be selected individually, or cascaded under control of

Block Diagram



Pin Configuration



NOTE: PIN FUNCTIONS IN PARENTHESIS APPLY ONLY TO 8 VERSION

General Description (Continued)

of the host processor. This arrangement allows a wide range of signal processing functions frequently required in application areas such as telecommunications, test and instrumentation, industrial automation, process control, etc., to be satisfied by a single S28215 DFUP.

The I/O structure of the S28215 provides flexibility and easy interfacing in microprocessor based systems. Input and output data transfers may be accomplished serially, as shown in the block diagram, using a μ255-law Codec such as the S3507, or using linear A/D and D/A converters. Data may also be transferred in parallel under control of a host processor, such as the S6802. Routines may be executed individually, completely under control of the host processor, or internal transfer addresses may be set up by the host, allowing routines to be cascaded internally. The ability to cascade routines allows complicated functions to be completed without intervention by the host processor.

Absolute Maximum Ratings

Supply Voltage	7.0VDC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Voltage at any Pin	V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C

Electrical Specifications: $V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_A = 0°C$ to $+70°C$, unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input HIGH Logic "1" Voltage	2.0		$V_{CC}+0.3$	V	$V_{CC} = 5.0V$
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	$V_{CC} = 5.0V$
I_{IN}	Input Logic Leakage Current		1.0	2.5	μAdc	$V_{IN} = 0V$ to 5.25V
C_I	Input Capacitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	$I_{LOAD} = -100\mu A$, $V_{CC} = min$, $C_L = 30pF$
V_{OL}	Output LOW Voltage			0.4	V	$I_{LOAD} = 1.6mA$, $V_{CC} = min$, $C_L = 30pF$
f_{CLK}	Clock Frequency	5.0	20		MHz	$V_{CC} = 5.0V$
P_D	Power Dissipation		700		mW	$V_{CC} = 5.0V$
$f_{CLK}(max)$	Maximum Clock Frequency		20.0		MHz	$V_{CC} = 5.0V$

S28215 Pin Functions/Descriptions

Microprocessor Interface (16 Pins)

D_0-D_7	(Input/Output) Bi-directional 8-bit data bus.
F_0-F_3	(Input) Control Mode/Operation Decode. Four Microprocessor address leads are used for this purpose. See "CONTROL MODES AND OPERATIONS." (Table 2)
$\overline{IE}$	(Input) Interface Enable. A low level on this pin enables the SPP microprocessor interface. Generated by microprocessor address decode logic.
(RD)	Read Data Pin. HIGH active. Used when interfacing to 8080/Z80μP.
R/$\overline{W}$ ($\overline{W/R}$)	(Input) Read/Write Select. When HIGH, output data from the SPP is available on the data bus. When LOW, data can be written into SPP. WR used when interfacing with 8080/Z80 μP.
$\overline{IRQ}$	(Output) Interrupt Request. This open drain output goes LOW when the SPP needs service from the microprocessor.
$\overline{RST}$	(Input) When LOW, clears all internal registers and counters, clears all modes and initiates program execution at location 00.
$\overline{CS}$	Chip Select pin. LOW active. Used when interfacing with a 8080/Z80 μP.

Serial Interface (6 pins)

SICK, SOCK	(Input) Serial Input/Output clocks. Used to shift data into/out of the serial port.
$\overline{SI}$	(Input) Serial Input. Serial data input port. Data is entered MSB first and is inverted.
SIEN	(Input) Serial Input Enable. A HIGH on this input enables the serial input port. The length of the serial input word (16 bits maximum) is determined by the width of this strobe.
$\overline{SO}$	(Output) Serial Output. Three-state serial output port. Data is output MSB first and is inverted.
SOEN	(Input) Serial Output Enable. A HIGH on this input enables the serial output port. The length of the serial output (16 bits maximum) is determined by the width of this strobe.

Miscellaneous

OSC_i, OSC_o	An external crystal with suitable capacitors to ground can be connected across these pins to form the time base for the SPP. An external clock can also be applied to OSC_i input if the crystal is not used.
V_{CC}, V_{SS}	Power supply pins $V_{CC} = +5V$, $V_{SS} = 0$ volt (Ground)

Functional Description

The S28215 is a pre-programmed version of AMI's Signal Processing Peripheral. This is a high speed microcomputer organized for efficient signal processing and contains a data memory, instruction memory, an arithmetic unit incorporating a 12-bit parallel multiplier, as well as control registers and counters. For more detailed information about the chip, please refer to the S28211 Advanced Product Description.

The S28215 Instruction ROM contains the various routines which make up the DFUP package. The routines together with their starting addresses in the Instruction ROM, are shown in Table 1A.

The Data ROM contains the parameters required to execute the functions. 128 words of Data RAM and an 8 word scratchpad are provided to hold the signal data and the jump addresses for cascading routines. The Data memory is arranged as a matrix of 32x8 words, as shown in Table 1B. The RAM utilization is routine dependent and is illustrated in the routine descriptions.

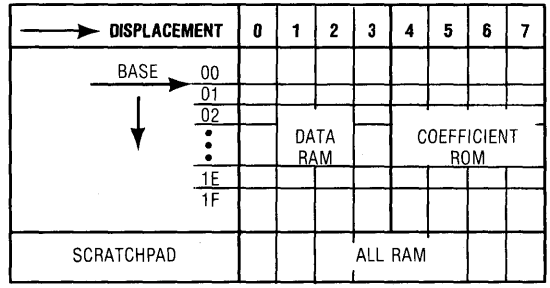
Table 1. Software Model of S28215

A. Routine Locations in Instruction Memory

(LOC (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY POINT "INIT" ROUTINE
04	ENTRY POINT "SETUP" ROUTINE
18 or 19*	ENTRY POINT "LINIP" ROUTINE
1B or 1C*	ENTRY POINT "MULIP" ROUTINE
34	ENTRY POINT "LINO1" ROUTINE
36	ENTRY POINT "LINO2" ROUTINE
38	ENTRY POINT "MULOP" ROUTINE
65	ENTRY POINT "DBOP" ROUTINE
80	ENTRY POINT "BMPY" ROUTINE
87	ENTRY POINT "IIR1" ROUTINE
96,97 or 98*	ENTRY POINT "IIR2" ROUTINE
A7	ENTRY POINT "FIR1" ROUTINE
AF, B0 or B1*	ENTRY POINT "FIR2" ROUTINE
BC	ENTRY POINT "RECT" ROUTINE
BF	ENTRY POINT "SQUAR" ROUTINE
C4	ENTRY POINT "FINT" ROUTINE
CA	ENTRY POINT "RINT" ROUTINE
CE	ENTRY POINT "SQUINT" ROUTINE
D6	ENTRY POINT "SINE" ROUTINE
E5	ENTRY POINT "NSET" ROUTINE
E9	ENTRY POINT "NOISE" ROUTINE

*See Routine descriptions for explanation of alternative entry points

B. Data Memory Map



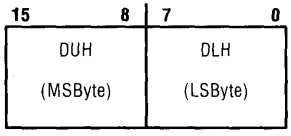
NOTE: Address [Base AB, Displacement C] is written as AB.C

C. Control Functions

F-Bus (HEX)	MNEMONIC
0	CLR
1	RST
2	DUH
3	DLH
4	XEQ
5	SRI
6	SRO
7	SMI
8	SMO
9	BLK
B	SOP
C	COP

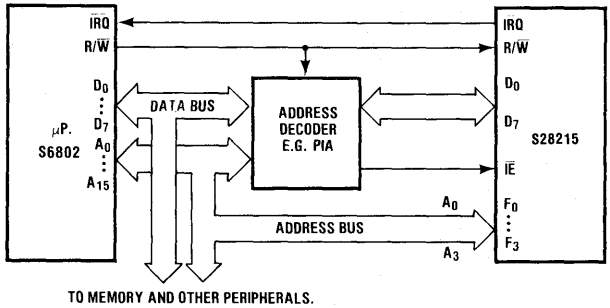
See Table 2 for descriptions

D. Input and Output Registers



Code is Two's Complement

Figure 1. Connection of S28215 as a Memory Mapped Peripheral



AMI

A Subsidiary of Gould Inc.

S3522

BELL 212A/CCITT V.22 COMPATIBLE MODEM FILTER WITH EQUALIZER

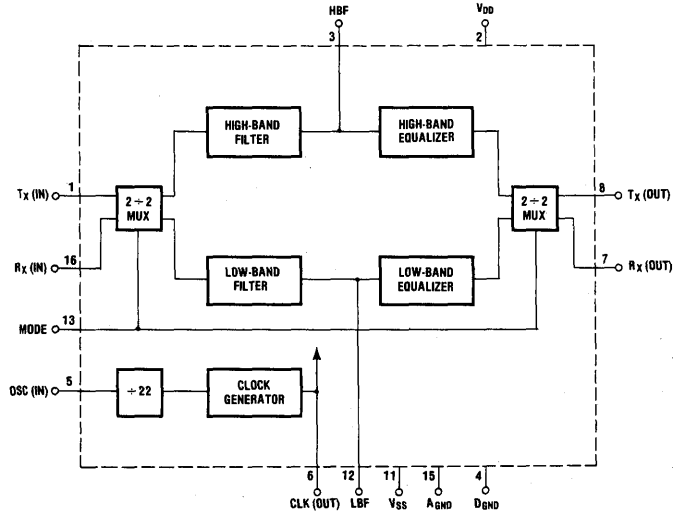
Features

- ☐ CCITT V.22 Compatible
- ☐ Usable for Bell 103/113 Applications
- ☐ High and Low Band Filters with Compromise Group Delay Equalizers
- ☐ Originate/Answer Operating Modes
- ☐ Buffered Clock Output
- ☐ Excellent Rejection of CCITT Guard Tones
- ☐ Low Power CMOS 50mW Typ.
- ☐ ±5 Volt Operation
- ☐ Low Cost 16-Pin Package

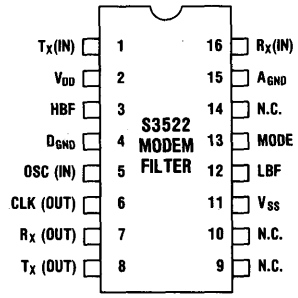
General Description

The AMI S3522 Modem Filter is a 16-pin monolithic CMOS integrated circuit designed to implement both the filtering and equalizing functions required in Bell 212A and CCITT V.22 Modems. The S3522 includes both the transmit signal shaping filter and the receive signal separation filter and features on-chip originate/answer mode selection logic. In addition, half-channel compromise amplitude and group delay equalization is included, giving full compromise equalization through the transmit and receive filter pair. The S3522 features excellent rejection of the CCITT Guard Tones at 550Hz: Low-Band (56dB), High-Band (61dB) and 1800Hz: Low-Band (48dB), High-Band (28dB).

Block Diagram



Pin Configuration



Functional Description

The S3522 is shown in simplified form in the block diagram. It consists of a low-band filter (800-1600Hz), a high-band filter (2000-2800Hz), and half-channel compromise group delay equalizers for both bands (see Figure 1). A changeover switch selects the routing of the input signals into the 2 filters, and another changeover switch routes the filter outputs to the appropriate output pins. The switches are controlled by the MODE selector, allowing the chip to be used in both the ORIGINATE and ANSWER modes without external switching. The outputs of both filters are brought out on separate pins, LBF and HBF. This allows the user to bypass the group delay equalizers if desired. Note that in this mode the filter outputs are not routed through the changeover switch, and external switching must be provided if mode changing is required. The filters are implemented using CMOS Switched Capacitor Filter technology, using a clocking frequency of 104.7kHz. The internal clocks are derived from the externally supplied 2.304MHz clock signal.

NOTE: External buffering is required for the LBF and HBF outputs.

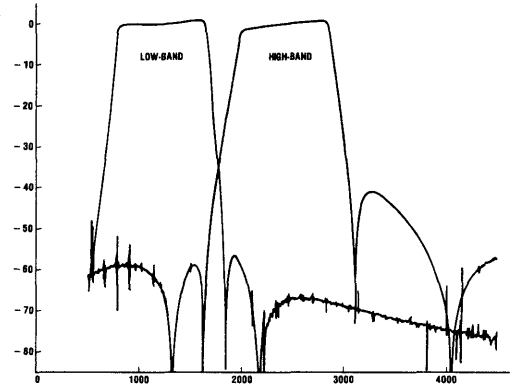
Low-Band Filter

The characteristics of the low-band filter are shown in Figure 2. The in-band response rises slightly near the top end of the pass-band, to compensate for typical line characteristics. The out-of-band attenuation ensures adequate rejection of the high-band signal and pilot tones at either 550Hz or 1800Hz. The weighted adjacent channel rejection exceeds 60dB. The group delay response of the filter is compensated by the compromise equalizer, which also compensates for the group delay distortion of typical lines. Only half the line characteristic is compensated in the filter, since 2 filters will always be connected in tandem in an end-to-end application. The group delay characteristic of the low-band filter is shown in Figure 3.

High-Band Filter

The characteristics of the high-band filter are shown in Figure 4. The in-band response has a slope of approximately 1.5dB from edge-to-edge, to compensate for typical line characteristics in this region. The out-of-band attenuation ensures adequate rejection of the low-band signal and pilot tones at either 550Hz or 1800Hz. The weighted adjacent channel rejection exceeds 60dB. Group delay compensation for the filter and half-channel characteristics is provided, as with the low-band filter. The group delay characteristic of the high-band filter is shown in Figure 5.

Figure 1. Typical Amplitude Response



Input and Output Considerations

The input signals to the S3522 should ideally be symmetrical about ground (0 volts). However D.C. offset existing at the input pins will not be transmitted to the outputs, since both filters have transmission zeroes at D.C. Since switched capacitor filters are sampled data circuits, care must be taken to avoid aliasing problems caused by signals around the sampling frequency. In the S3522 this means that an anti-aliasing filter should be used at the Receive Input if there is any possibility of input signal components lying in the region of 205.4 ± 3kHz and multiples of this frequency. A smoothing filter may be required at the Transmit Output where the signal is to be transmitted over a telephone line. Care must be taken to avoid distorting the group delay characteristics of the system if a smoothing filter is used. See Figure 6 for Typical Anti-Aliasing Circuit.

Clock Considerations

The S3522 is designed to operate with an externally

Figure 2. Typical Low-Band Amplitude

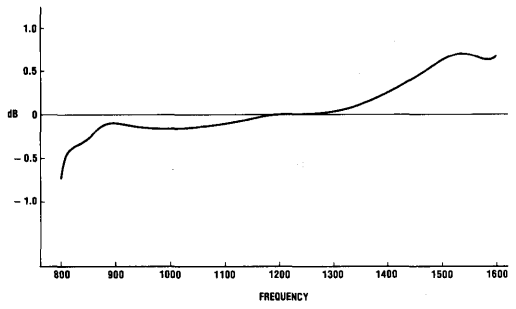


Figure 3. Typical Low-Band Group Delay

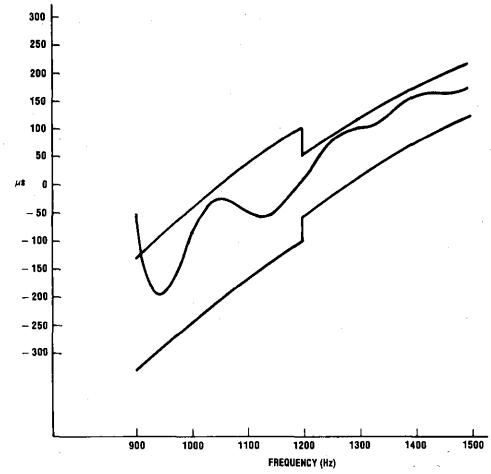


Figure 4. Typical High-Band Amplitude

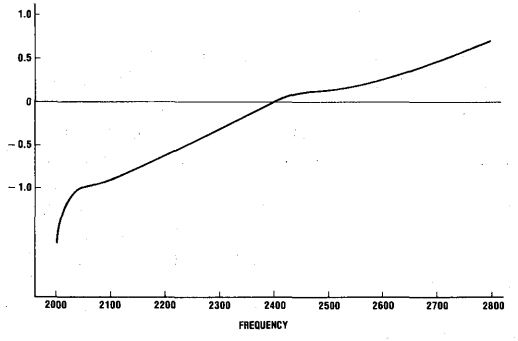


Figure 5. Typical High-Band Group Delay

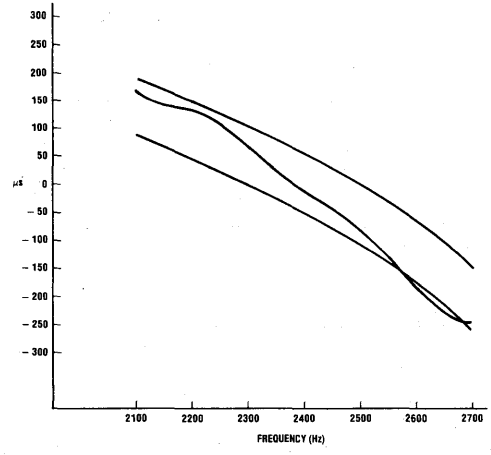
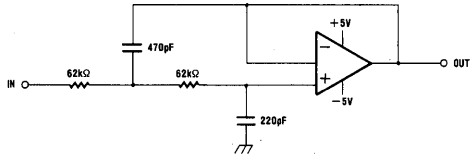


Figure 6. Anti-Aliasing L.P. Filter for S3522 at T_X (OUT) and R_X (IN)

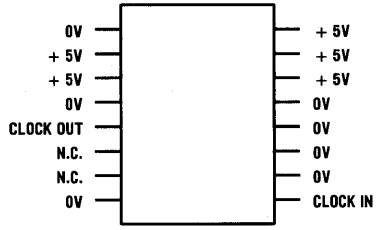


supplied 2.304MHz clock. The accuracy and stability of this frequency will directly affect the accuracy and stability of the filter characteristics. The center frequency and bandwidth may be scaled directly in proportion to the clock frequency if desired to modify them for other applications. The 2.305MHz frequency may be derived from the more commonly available 2.4576MHz by dividing this frequency by 15/16, using a binary rate multiplier (BRM). The BRM will generate an uneven pulse train, since it does the frequency division by eliminating one pulse out of each group of sixteen. This does modify the performance of the S3522, since it effectively modulates the sampling frequency. However, the only consequence is the generation of low level out-of-band signals, the largest of which is more than 50dB below the signal level. The in-band performance is not measureably affected. The BRM can be either TTL (7497), using the 0 and + 5 volt supplies, or CMOS (4089) using the − 5 and + 5 volt supplies. The 4089 requires a 10 volt supply for guaranteed operation at this frequency. The S3522 will operate with a clock "0" level anywhere between + 1.4 and − 5 volts. Both 7497 and 4089 circuits are shown in Figure 7.

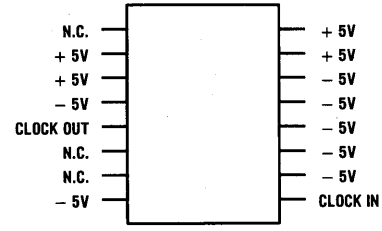
COMMUNICATION PRODUCTS

Figure 7. Connections for Clock Divider Circuits

7497 Circuit



4089 Circuit



Pin/Function Descriptions

Pin	Name	Function
1	$TX_{(IN)}$	Transmit Signal Input.
2	V_{DD}	Positive Voltage Supply (4.5 to 5.5 Volts).
3	$HBF_{(OUT)}$	Output from high-band filter without delay equalizer circuit. NOTE that the signal appearing at this pin depends on the state of the MODE input. See text for further information.
4	D_{GND}	Digital Ground. Connect to the ground line common to other digital circuits in system.
5	$OSC_{(IN)}$	2.304MHz Clock Input. This input is TTL and CMOS compatible.
6	$CLK_{(OUT)}$	104.7kHz Buffered Clock Output. This reference output is available to drive other circuitry. The frequency is the Input Clock Frequency divided by 22. The output will drive one CMOS load.
7	$RX_{(OUT)}$	Receive Signal Output. This output will drive a 20kΩ load.
8	$TX_{(OUT)}$	Transmit Signal Output. This output will drive a 20kΩ load.

Pin/Function Descriptions (Continued)

Pin	Name	Function
9, 10	N.C	No Connection.
11	V_{SS}	Negative Voltage Supply (−4.5 to −5.5 Volts).
12	$LBF_{(OUT)}$	Output from low-band filter without delay equalizer circuit. NOTE that the signal appearing at this pin depends on the state of the MODE input. See text for further information.
13	MODE	Originate Answer Mode Control Input. A logic '0' on this pin sets the device to the ORIGINATE mode, with the transmit signal in the low-band and the receive signal in the high-band. A logic '1' sets the device to the ANSWER mode, with the transmit signal in the high-band and the receive signal in the low-band. This input is CMOS and open collector TTL compatible.
14	N.C.	No Connection.
14	A_{GND}	Analog Ground. Connect to the ground line common to other analog circuitry in the system.
16	$RX_{(IN)}$	Receive Signal Input.

Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... +15.0V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +115°C
Analog Input ..... $V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°$ to $+70°C$, $V_{DD} = +5V$, $V_{SS} = -5V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply Voltage	4.5	5	5.5	V
V_{SS}	Negative Supply Voltage	−4.5	−5	−5.5	V
V_{IH} (MODE)	High Level Logic Input	4			V
V_{IH} (OSC-IN)	High Level Logic Input		2.8		V
V_{IL} (MODE, OSC-IN)	Low Level Logic Input	V_{SS}		+0.8	V
V_{OL} (CLK OUT)	Low Level Logic Output (1 CMOS Load)	V_{SS}		$V_{SS}+0.5$	V
V_{OH} (CLK OUT)	High Level Logic Output (1 CMOS Load)	$V_{DD}-0.5$		V_{DD}	V
R_{IN} (TX IN, RX IN)	Input Resistance		5		M_Ω
C_{IN} (TX IN, RX IN)	Input Capacitance		10		pF
R_{OUT} (TX OUT, RX OUT)	Output Resistance		2		k_Ω
I_{DD}, I_{SS}	Supply Currents		5	10	mA

A.C. System Specifications: $T_A = 0°$ to $-70°C$, $V_{DD} = +5V$, $V_{SS} = -5V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
f_{OL}	Low-Band Center Frequency		1200		Hz
f_{OH}	High-Band Center Frequency		2400		Hz
BW	Bandwidth (both bands) (−1dB)		800		Hz
A_{FO}	Gain at Center Frequencies	−0.5	0	+0.5	dB
A_{FREL}	Gain Relative to Center Frequency: See Figures 2 and 3				
	@ 800Hz (Low-Band Filter)	−1.0	−0.25	+0.5	dB
	900Hz (Low-Band Filter)	−0.5	0	+0.5	dB
	1500Hz (Low-Band Filter)	0	+0.50	+1.0	dB
	1600Hz (Low-Band Filter)	+0.25	+0.75	+1.25	dB
	2000Hz (High-Band Filter)	−2.0	−1.5	0	dB
	2100Hz (High-Band Filter)	−1.30	−0.8	0	dB
	2700Hz (High-Band Filter)	0	+0.50	+1.0	dB
	2800Hz (High-Band Filter)	+0.25	+0.75	+1.25	dB
GD_{REL}	Group Delay Relative to Center Frequency: See Figures 4 and 5				
	@ 900Hz (Low-Band Filter)		−70		μsec
	1100Hz (Low-Band Filter)		−80		μsec
	1300Hz (Low-Band Filter)		+90		μsec
	1500Hz (Low-Band Filter)		+70		μsec
	2100Hz (High-Band Filter)		+190		μsec
	2300Hz (High-Band Filter)		+50		μsec
	2500Hz (High-Band Filter)		−80		μsec
	2700Hz (High-Band Filter)		−210		μsec
R_{AC}	Adjacent Channel Rejection	50			dB
V_O (Peak-to-Peak)	Output Voltage Swing		6		V
V_{NL} C-Message Weighted	Noise Level, Low-Band		240		μV RMS
V_{NH} C-Message Weighted	Noise Level, High-Band		240		μV RMS

COMMUNICATION PRODUCTS

AMI®

A Subsidiary of Gould Inc.

S35212

212A/V.22 MODEM FILTER WITH EQUALIZERS

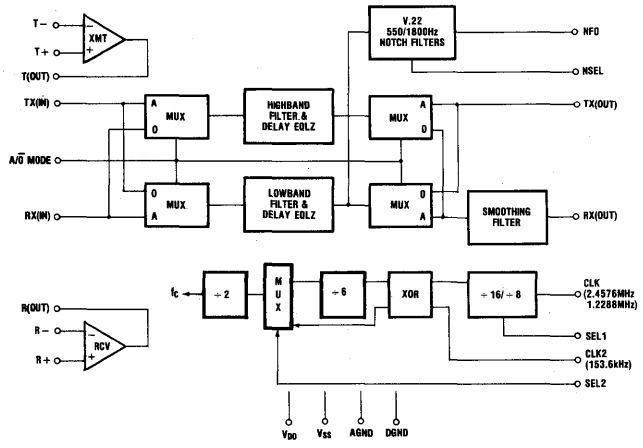
Features

- ☐ Bell 212A/V.22 Compatible
- ☐ Usable for Bell 103/113 Applications
- ☐ High and Low Band Filters With Compromise Group Delay Equalizers and Smoothing Filters
- ☐ Guard Tone Notch Filters for CCITT V.22 Applications
- ☐ Originate/Answer Operating Modes
- ☐ Low Power CMOS: 75 mW Typ.
- ☐ Wide Supply Operation (±4V to ±6V)
- ☐ Two Uncommitted Operational Amps.
- ☐ Choice of Clocking Frequencies: 2.4576MHz, 1.2288MHz, or 153.6kHz
- ☐ Detection of Call Progress Tones

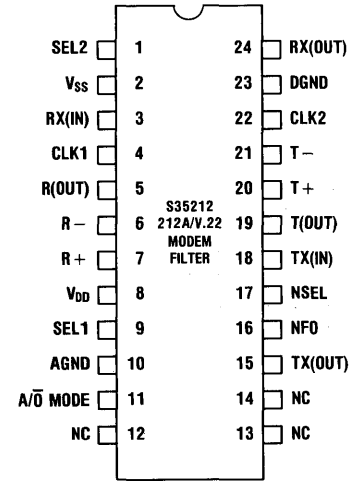
General Description

The AMI S35212 Modem Filter is a monolithic CMOS integrated circuit designed to implement both the filtering and equalizing functions required in Bell 212A and CCITT V.22 modems. The S35212 includes both the transmit signal shaping filter and the receive signal separation filter and features on-chip originate/answer mode selection. In addition, half-channel compromise amplitude and group delay equalizers are included giving full compromise equalization through the transmit and receive filter pair. For CCITT V.22 applications a notch filter is included. It can be programmed to provide rejection at 1800Hz or 550Hz. Two uncommitted operational amplifiers are provided which can be used

Block Diagram



Pin Configuration



General Description (continued)

for gain control or anti-aliasing filters. A continuous low pass filter is also included on the RX(OUT) which acts as a smoothing filter. Provision is made (via SEL2) to switch the filter between the Call Progress Tone Detection mode and the normal Data Transmission mode. For maximum flexibility the S35212 may be operated from a 2.4576MHz, 1.2288MHz, or 153.6kHz clock.

Pin/Function Description

Pin Name	Pin Number	Function
SEL2	1	Logic '0' for normal operation. Logic '1' scales down the frequency response by a factor of 6 for Call Progress Tone Detection through the high group filter.
V_{SS}	2	Negative Supply Voltage (typically − 5 Volts).
RX (IN)	3	Receive Signal Input.
CLK1	4	2.4576MHz or 1.2288MHz Clock Input. This input is TTL and CMOS compatible. Leave open when using CLK2.
R (OUT)	5	Receive Uncommitted Op Amp Output.
R −	6	Receive Uncommitted Op Amp Negative Input.
R +	7	Receive Uncommitted Op Amp Positive Input.
V_{DD}	8	Positive Supply Voltage (typically + 5 Volts).
SEL1	9	Logic '0' selects 1.2288MHz. Logic '1' selects 2.4576MHz clock into Pin 4.
AGND	10	Analog Ground.
MODE	11	Originate/Answer Mode Control Input. A logic '0' sets the device in originate mode with the transmit signal in the low-band and receive signal in the high-band. A logic '1' reverses the connections.
NC	12	No Connection.
NC	13	No Connection.
NC	14	No Connection.
TX (OUT)	15	Transmit Signal Output. This output will drive a 20k load.
NFO	16	Notch Filter Output. This output will drive a 20k load.
NSEL	17	A logic '0' on this input programs the notch filter to reject 550Hz. A logic '1' programs it to reject 1800Hz.
TX (IN)	18	Transmit Signal Input.
T (OUT)	19	Transmit Uncommitted Op Amp Output.
T +	20	Transmit Uncommitted Op Amp Positive Input.
T −	21	Transmit Uncommitted Op Amp Negative Input.
CLK2	22	153.6kHz Clock Input. This input is TTL and CMOS compatible. Leave open when using CLK1.
DGND	23	Digital Ground.
RX (OUT)	24	Receive Signal Output. This output will drive a 20k load.

Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$) ..... + 13.5V
Operating Temperature ..... 0°C to + 70°C
Storage Temperature ..... − 55°C to + 125°C
Analog Input ..... $V_{SS} - 0.3V \leqslant V_{IN} \leqslant V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$; $V_{DD} = +5V$; $V_{SS} = -5V$ unless otherwise specified

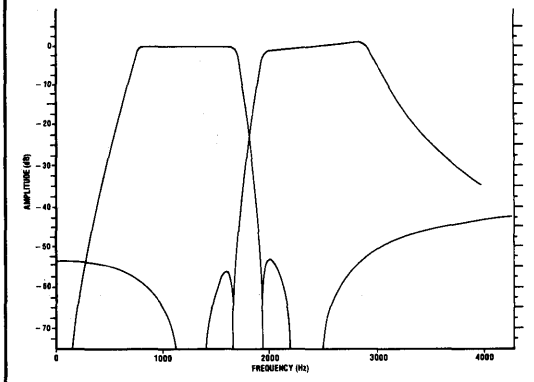
Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Logic Input (Pins 1, 9, 11, 17)	4		V_{DD}	V
V_{IH}	High Level Logic Input (Pins 4 and 22)	2.0		V_{DD}	V
V_{IL}	Low Level Logic Input (Pins 1, 4, 9, 11, 17, 22)	V_{SS}		$V_{SS} + 0.8$	V
R_{IN}	Input Resistance (Pins 3 and 18)		5		MΩ
C_{IN}	Input Capacitance (Pins 3 and 18)		10		pF
P_D	Power Dissipation @ ± 6V		75	150	mW

A.C. System Specifications: $T_A = 25°C$; $V_{DD} = +5V$; $V_{SS} = -5V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_O	Reference Signal Level Input		1		VRMS
V_{MAX}	Maximum Signal Level Input		1.4		VRMS
BW	Bandwidth (both bands; − 3dB)		960		Hz
A_{FO}	Gain at Center Frequencies		0		dB
ICN_L	Idle Channel Noise-Low Band Filter		22	33	dBrnC0
ICN_H	Idle Channel Noise-High Band Filter		23	33	dBrnC0
N_{FT}	Clock Feedthrough with Respect to Signal Level	TX RX	− 23 − 60		dB dB

Frequency (Hz)		Relative Gain (dB)	
		Min.	Max.
Low Band	400		− 35
	800	− 1	+ 1
	1200	− 1	+ 1
	1600	− 1.5	+ 1
	1800		− 18
	2000		− 48
	2400		− 55
	2800		− 50
High Band	800		− 50
	1200		− 53
	1600		− 50
	2000	− 2.5	+ 0.5
	2400	− 1	+ 1
	2800	0	+ 2.5
	3200		− 10
	3500		− 20

Figure 1. Typical Amplitude vs. Frequency Plot



Call Progress Mode Operation

By switching Pin 1 (SEL2) the center frequencies of the filters will shift down to one-sixth of their original values. This is done by dividing the clock frequency by 6. As a result, the 1200Hz filter will be centered around 200Hz and the 2400Hz filter will be centered around 400Hz when Pin 1 is switched high.

With the high group filter centered at 400Hz, its pass-band will be approximately 300Hz to 480Hz. This allows the precision dial tone of 350/440Hz to pass, as well as audible ringing at 440/480Hz. Half of the busy or re-order tone of 480/620Hz will also pass through the high group filter in this mode.

By using a suitable detector circuit combined with a method of timing determination it is possible to build a more intelligent MODEM that can communicate back to its terminal or computer the status of the phone call.

Figure 2. Typical Low-Band Amplitude vs. Frequency Plot

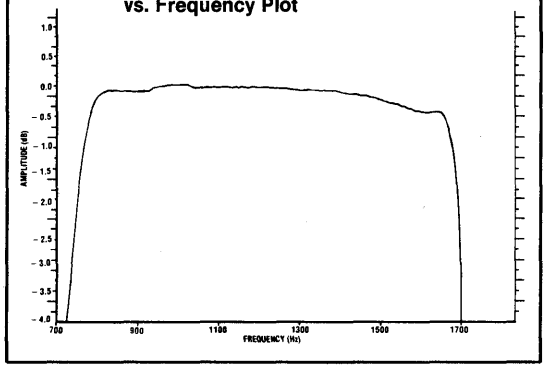


Figure 3. Typical Low-Band Group Delay vs. Frequency Plot

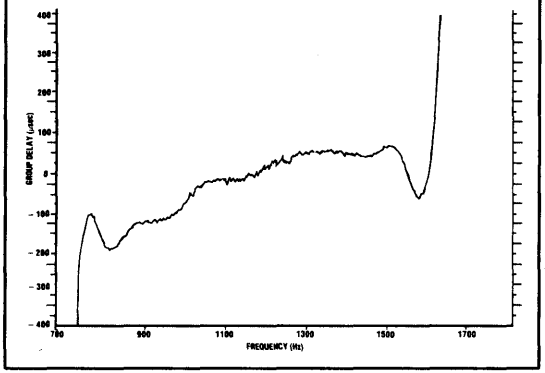


Figure 4. Typical High-Band Amplitude vs. Frequency Plot

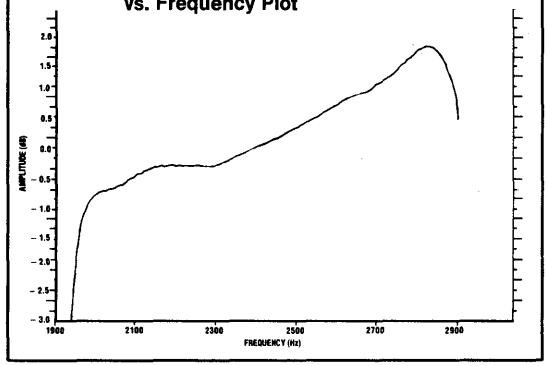
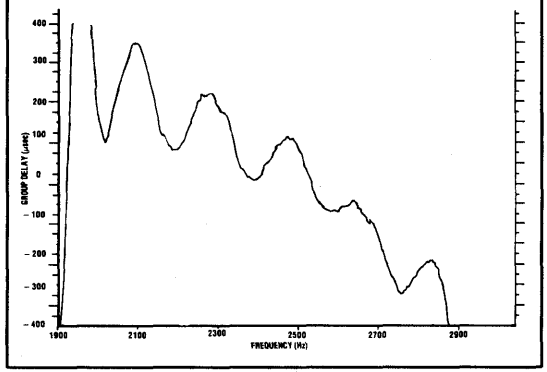


Figure 5. Typical High-Band Group Delay vs. Frequency Plot



A Subsidiary of Gould Inc.

Advanced Product Description **S3524A**

2600Hz Digital Frequency Detector

Features

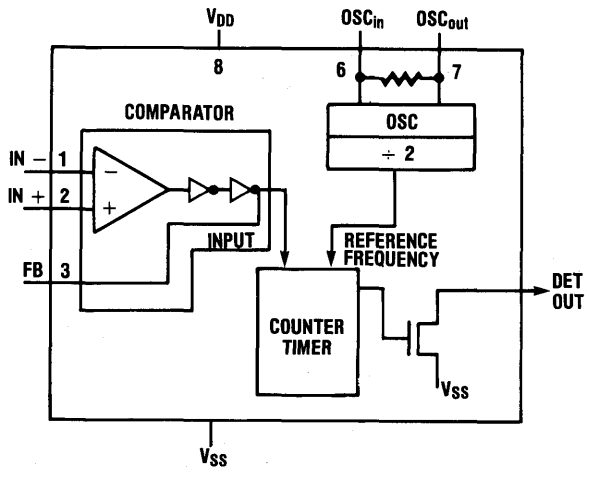
- ☐ 2600Hz Center Frequency With 70Hz Bandwidth.
- ☐ Small 8-Pin Minidip Package
- ☐ Operation From a Low Cost 3.58MHz TV Color-burst Crystal or External Clock
- ☐ Input Comparator for Squaring and Sensitivity Adjustment
- ☐ Low Power CMOS Technology

Description

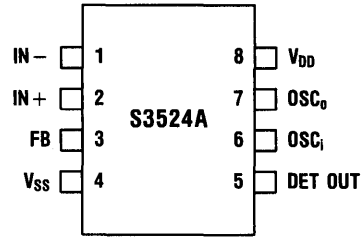
The S3524 is a digital Frequency Detector used to accurately determine if an incoming tone is within a set of predefined limit frequencies. It checks every period of the incoming signal, giving a true output for each period falling within the desired bandwidth.

The S3524A, using a 3.582MHz clock, will detect a 2600Hz frequency within 70Hz bandwidth. It is primarily designed to follow the S3526B 2600Hz bandpass filter as shown in Figure 2.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage (V_{DD}-V_{SS})	±15V
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Analog Input	$V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

DC Electrical Operating Characteristics: T_A = 0°C to +70°C

Symbol	Parameter Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to GND)	4.75	5	5.25	V
V_{SS}	Negative Supply (Ref. to GND)	−4.75	−5	−5.25	V
PD	Power Dissipation			100	mW
V_{IN}	Input Signal Level	43			mV (RMS)
R_O	Load Resistance	6			k Ω

Pin Description

Name	Number	Description
V_{DD}	8	Positive Power Supply. Typically +5V.
V_{SS}	4	Negative Power Supply. Typically −5V.
IN−	1	Input comparator for setting sensitivity and squaring of analog signals. Signal sensitivity is controlled by selecting external resistors.
IN+	2	
FB	3	
DET OUT	5	The detector output. Open drain type output for ease of interface. DET OUT will be high after one full cycle of valid signal is detected, and will remain high until an out of frequency cycle is detected.
OSC IN	6	Oscillator terminals for 3.58MHz reference crystal or clock. Uses standard TV crystal or a rail-to-rail CMOS clock may be used.
OSC OUT	7	

Operation and Applications Information

Figure 1.

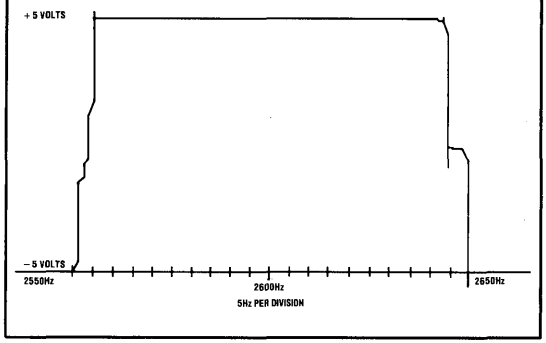


Figure 2. Representative Circuit

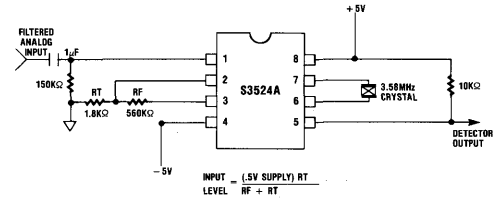
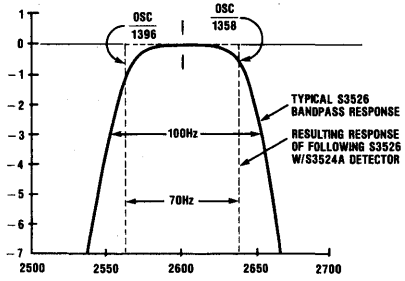


Figure 3. Effective Response of S3526 Bandpass Filter Followed by S3524A Digital Detector



IN SINGLE SUPPLY SITUATION THE GROUND FOR THE SENSITIVITY ADJUSTMENT WOULD BE 1/2 (V_{DD}-V_{SS}) AS DETERMINED BY A REGULATOR OR RESISTIVE VOLTAGE DIVIDER. OFFSET COMPENSATION WOULD BE DONE BY VARYING THE HALF VOLTAGE POINT SLIGHTLY IF DESIRED.

Figure 5. A Typical Detection Bandwidth 2600 for Application Circuit in Figure 4 at 10V

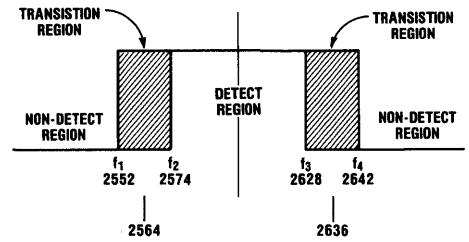
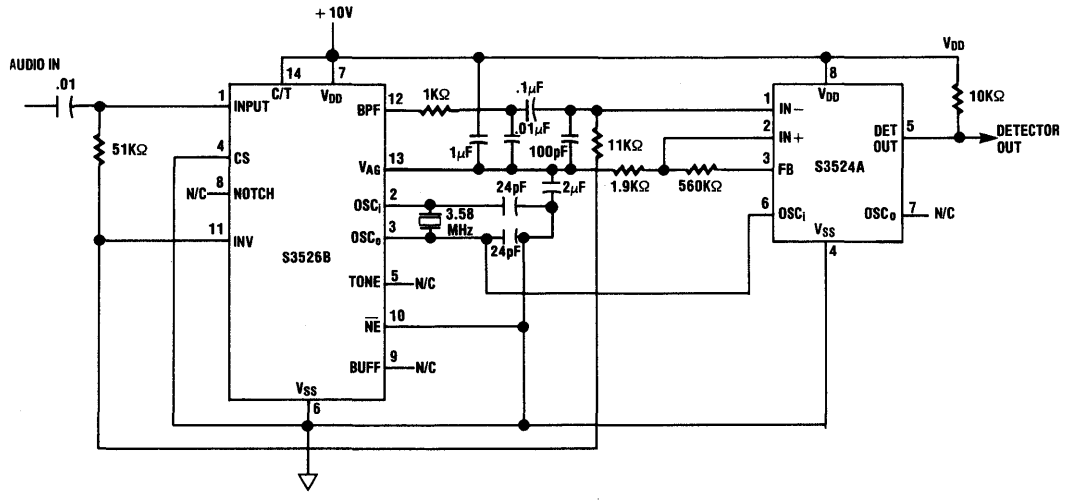


Figure 4. Circuit Example Showing S3526B and S3524A Combined to Provide Narrow Detection Bandwidth



AMI®

A Subsidiary of Gould Inc.

S3525A/S3525B

DTMF BANDSPLIT FILTER

COMMUNICATION PRODUCTS

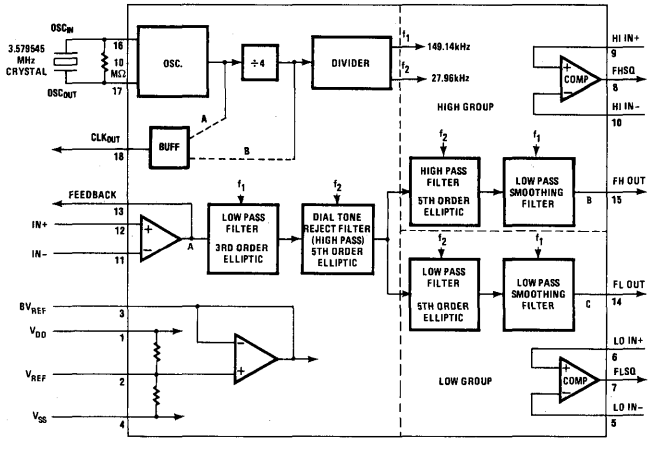
Features

- ☐ CMOS Technology for Wide Operating Single Supply Voltage Range (7.0V to 13.5V). Dual Supplies (±3.5V to ±6.75V) Can Also Be Used.
- ☐ Uses Standard 3.58MHz Crystal as Time Base. Provides Buffered Clock to External Decoder Circuit.
- ☐ Ground Reference Internally Derived and Brought Out.
- ☐ Uncommitted Differential Input Amplifier Stage for Gain Adjustment
- ☐ Filter and Limiter Outputs Separately Available Providing Analog or Digital Outputs of Adjustable Sensitivity.
- ☐ Can be Used with Variety of Available Decoders to Build 2-Chip DTMF Receivers.

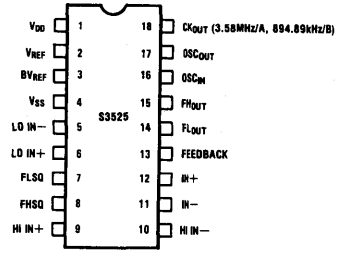
General Description

The S3525 DTMF (Touch Tone®) Bandsplit Filter is an 18-pin monolithic CMOS integrated circuit designed to implement a high quality DTMF tone receiver system when used with a suitable decoder circuit. The device includes a dial tone filter, high group and low group separation filters and limiters for squaring of the filtered signals. An uncommitted input amplifier allows a programmable gain stage or anti-aliasing filter. The dial tone filter is designed to provide a rejection of at least 52dB in the frequency band of 300Hz to 500Hz. The difference between the S3525A and the S3525B is the frequency of output clock signal at the CKOUT pin. In the S3525B, it is a 894.89kHz square wave while in the S3525A, it is a 3.58MHz buffered oscillator signal. The S3525A can be used with digital DTMF decoder chips that need the TV crystal time base allowing use of only one crystal between the filter and decoder chips.

Block Diagram



Pin Configuration



® Registered trademark of AT&T

Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD} - V_{SS}$)	+15.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +125°C
Analog Input	$V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

DC Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref to V_{SS})		9.6	12.0	13.5	V
$V_{OL(CKOUT)}$	Logic Output "Low" Voltage $I_{OL} = 160\mu A$			$V_{SS} + 0.4$		V
$V_{OH(CKOUT)}$	Logic Output "High" Voltage $I_{OH} = 4\mu A$			$V_{DD} - 1.0$		V
$V_{OL(FH, FL)}$	Comparator Output Voltage Low	500pF Load			$V_{SS} + 0.5$	V
		10kΩ Load			$V_{SS} + 2.0$	V
$V_{OH(FH, FL)}$	Comparator Output Voltage High	500pF Load	$V_{DD} - 0.5$			V
		10kΩ Load	$V_{DD} - 2.0$			V
$R_{INA\ (IN-, IN+)}$	Analog Input Resistance		8			MΩ
$C_{INA\ (INA-, IN+)}$	Analog Input Capacitance				15	pF
V_{REF}	Reference Voltage Out		0.49 ($V_{DD} - V_{SS}$)	0.50 ($V_{DD} - V_{SS}$)	0.51 ($V_{DD} - V_{SS}$)	V
$V_{OR} = [BV_{REF} - V_{REF}]$	Offset Reference Voltage				50	mV
P_D	Power Dissipation	$V_{DD} = 10V$		170		mW
		$V_{DD} = 12.5V$		400		mW
		$V_{DD} = 13.5V$			650	mW

AC System Specifications:

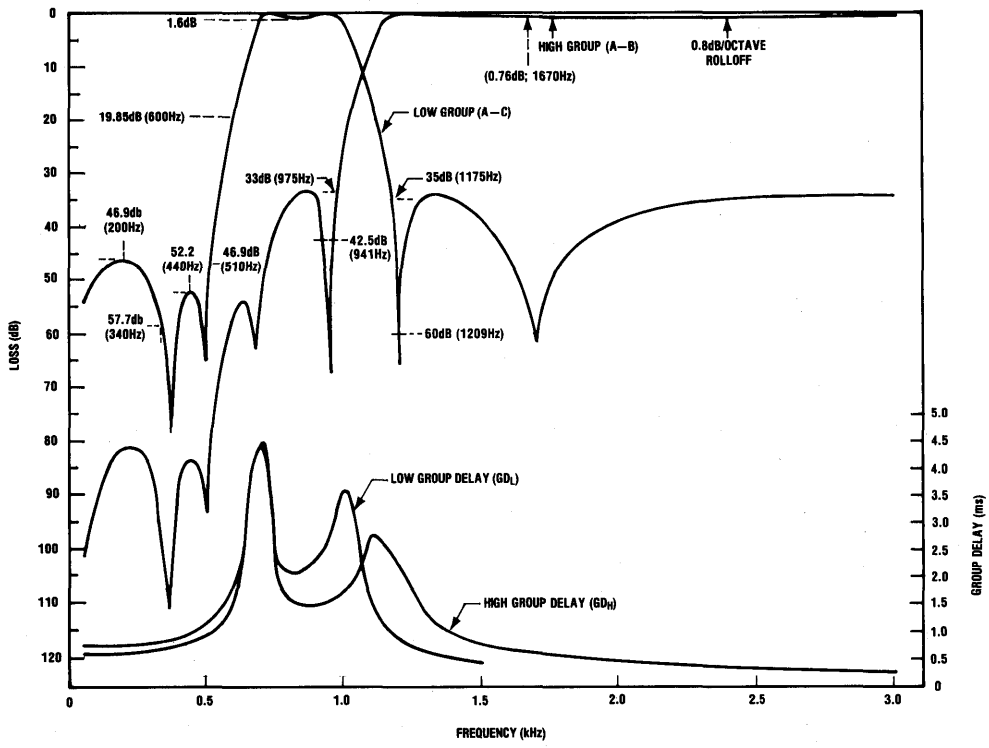
Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
A_F	Pass Band Gain		5.5	6	6.5	dB
DTR_L	**Dial Tone Rejection** Dial Tone Rejection is measured at the output of each filter with respect to the passband Low Group Rejection	350Hz	55	59		dB wrt 700Hz
		440Hz	50	53		dB wrt 700Hz
DTR_H	High Group Rejection	Either Tone	55	68		dB wrt 1200Hz

AC System Specifications (Continued)

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
	Attenuation Between Groups				
	Attenuation of the nearest frequency of the opposite group is measured at the output of each filter with respect to the passband				
GA_L	Attenuation of 1209Hz	50	>60		dB wrt 700Hz
GA_H	Attenuation of 941Hz	40	42		dB wrt 1200Hz
	Total Harmonic Distortion				
THD	Total Harmonic Distortion (dB). Dual tone of 770Hz and 1336Hz sine-wave applied at the input of the filter at a level of 3dBm each. Distortion measured at the output of each filter over the band of 300 Hz to 10kHz ($V_{DD} = 12V$)			−40	dB
	Idle Channel Noise				
ICN	Idle Channel Noise measured at the output of each filter with C-message weighting. Input of the filter terminated to BV_{REF}			1	mV_{rms}
	Group Delay (Absolute)				
GD_L	Low Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms
GD_H	High Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms

Pin #	Function	Descriptions
16,17	OSC_{IN}, OSC_{OUT}	These pins are for connection of a standard 3.579545MHz TV crystal and a 10MΩ ±10% resistor for the oscillator from which all clocking is derived. Necessary capacitances are on-chip, eliminating the need for external capacitors.
18	CKOUT (S3525A)	Oscillator output of 3.58MHz is buffered and brought out at this pin. This output drives the oscillator input of a decoder chip that uses the TV crystal as time base. (Only one crystal between the filter and decoder chips is required.)
18	CKOUT (S3525B)	This is a divide by 4 output from the oscillator and is provided to supply a clock to decoder chips that use 895kHz as time base.
11,12,13	IN−, IN+, Feedback	These three pins provide access to the differential input operational amplifier on chip. The feedback pin in conjunction with the IN− and IN+ pins allows a programmable gain stage and implementation of an anti-aliasing filter if required.
15,14	FH OUT, FL OUT	These are outputs from the high group and low group filters. These can be used as inputs to analog receiver circuits or to the on-chip limiters.
9,10,5,6	HI IN−, HI IN+ LO IN−, LO IN+	These are inputs of the high group and low group limiters. These are used for squaring of the respective filter outputs. (See Figure 2.)
8,7	FHSQ, FLSQ	These are respectively the high group and low group square wave outputs from the limiters. These are connected to the respective inputs of digital decoder circuits.
1,4	V_{DD}, V_{SS}	These are the power supply voltage pins. The device can operate over a range of $7V \leqslant (V_{DD} - V_{SS}) \leqslant 13.5V$.
2	V_{REF}	An internal ground reference is derived from the V_{DD} and V_{SS} supply pins and brought out to this pin. V_{REF} is $1/2(V_{DD} - V_{SS})$ above V_{SS}.
3	BV_{REF}	Buffered V_{REF} is brought out to this pin for use with the input and limiter stages.

Figure 1. Typical S3525 DTMF Bandsplit Filter Loss/Delay Characteristics



Input Configurations

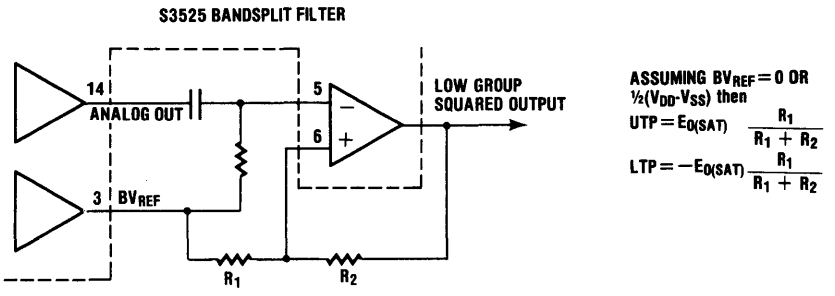
The applications circuits show some of the possible input configurations, including balanced differential and single ended inputs. Transformer coupling can be used if desired. The basic input circuit is a CMOS op amp which can be used for impedance matching, gain adjustment, and even filtering if desired. In the differential mode, the common mode rejection is used to reject power line-induced noise, but layout care must be taken to minimize capacitive feedback from pin 13 to pin 12 to maintain stability.

Since the filters have approximately 6dB gain, the inputs should be kept low to minimize clipping at the analog outputs (FL_{OUT} and FH_{OUT}).

Output Considerations

The S3525 has both analog and digital outputs available. Most integrated decoder circuits require digital inputs so the on-chip comparators are used with hysteresis to square the analog outputs. The sensitivity of the receiver system can be set by the ratio of R1 and R2, shown in Figure 2. The amount of hysteresis will set the basic sensitivity and eliminate noise response below that level.

Figure 2. Typical Squaring Circuit



Crystal Oscillator

The S3525 crystal oscillator circuit requires a 10 Meg ohm resistor in parallel with a standard 3.58MHz television colorburst crystal. For this application, however, crystals with relaxed tolerances can be used. Specifications can be as follows:

Frequency	3.579545 ±.02%
RS≤180Ω	L_M~96MH
C_L = 18pF	C_h = 7pF

Alternate Clock Configurations

If 3.58MHz is already available in the system it can be applied directly as a logic level to the OSC_{IN} (pin 16). [Max. zero~30% V_{DD}, min. one~70% V_{DD}]. Waveforms not satisfying these logic levels can be capacitively coupled to OSC_{IN} as long as the 10 Meg ohm feedback resistor is installed.

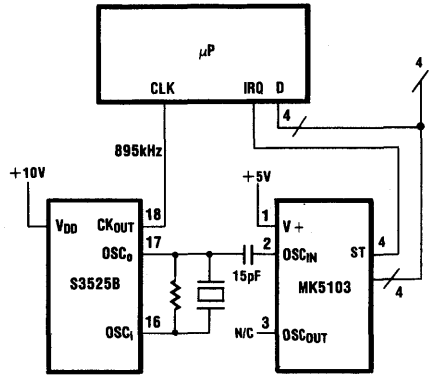
The S3525A provides a buffered 3.58MHz signal from the on-chip oscillator to external decoders or other devices requiring 3.58MHz. The S3525B provides a buffered ÷4 output at 895kHz to drive certain tone decoders and microprocessors. If both frequencies are required in a system, the 3.58MHz can be capacitively coupled as shown in Figure 2A.

Applications

The circuits shown are not necessarily optimal but are intended to be good starting points from which an optimal design can be developed for each individual application.

Companion decoders to be used with the S3525 vary in performance and features. Nitron's NC2030 and MOSTEK's MK5102/03 are available units that can be used with the S3525.

Figure 2A. S3525B Driving MK5103



Typical Applications

- ☐ Wireline DTMF Signal Receivers
- ☐ Radio DTMF Signal Receivers
- ☐ Dial Tone Detectors
- ☐ Offsite Data Collectors/Test Instruments
- ☐ Security Alarms
- ☐ Remote Command Receivers
  - — Phone Message Playback
  - — Camera Controllers
  - — Robot Arm Controllers

Figure 3. DTMF Keyboard

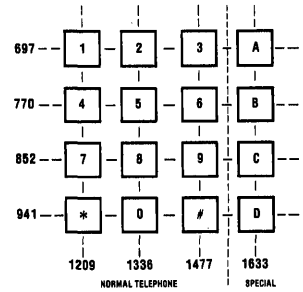


Figure 4. AMI/Mostek 2 Chip DTMF Receiver

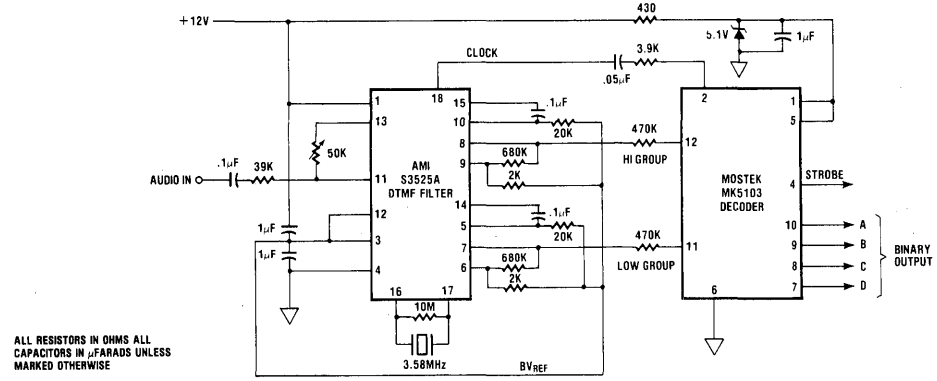
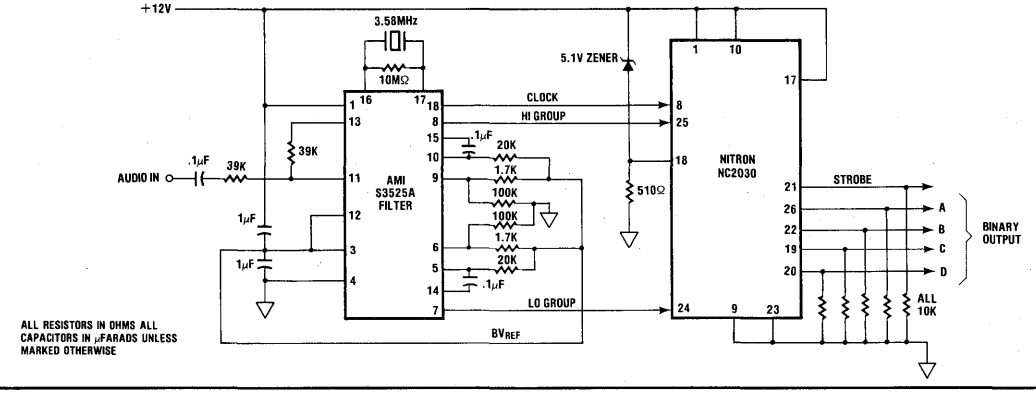
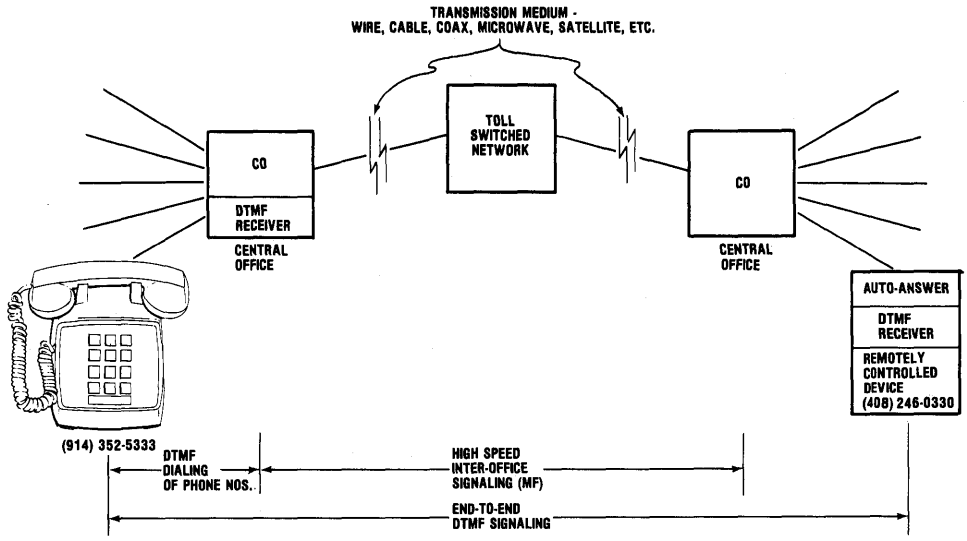


Figure 5. AMI/Nitron 2 Chip DTMF Receiver



Additional information can be obtained from the S3525 Applications Note # AN-301 available on request from AMI, and from the suppliers of the decoder circuits.

Figure 6. DTMF End-to-end Signaling Using the Telephone Network



Remote Control

In some systems, a telephone set is used to do remote controlling. A remote device to be signalled is interconnected to the telephone network with its own number (see Figure 6). When that number is dialed, the connection is established. The calling party continues to push the buttons on his telephone, sending command codes.* The DTMF Receiver at the central office is disconnected once the line connection is established, so no problem arises in the telephone network. Now the DTMF Receiver in the answering device is detecting and responding to the dialed digits, performing the control functions.

Dial Tone Detector

Since the frequency response of switched capacitor filters can be varied directly by varying the clock frequency, the S3525 can be used for other Telecommunications applications.

One application is a dial tone detector for telephone accessory equipment to determine the presence or absence of dial tone. Precision dial tone is a combination of 350 and 440Hz. By using a crystal of 1.758MHz the 3dB points of the low group filter output will be 334 to 496Hz. Thus, all the energy from precision dial tone will be available at the low group output.

* Need "Polarity Guard" or non-reversing central office so encoder stays enabled.

A Subsidiary of Gould Inc.

Advanced Product Description **S3526**

SINGLE FREQUENCY TUNEABLE BANDPASS/NOTCH FILTER/TONE GENERATOR

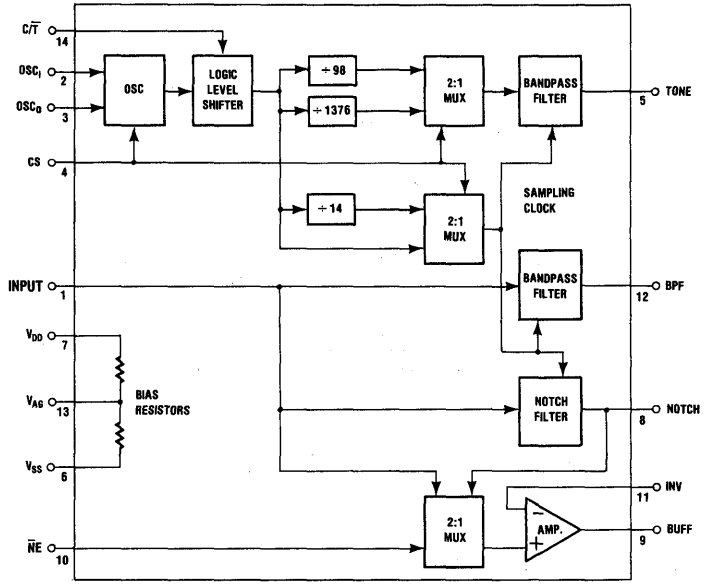
Features

- ☐ Center Frequency of Filters Match and Track Frequency of Generated Tone
- ☐ Tone Frequency Adjustable Over a 100Hz to 5kHz Range
- ☐ Unfiltered Input, Input with Notched Tone, Input Tone and Tone Generator Outputs
- ☐ Operation from a Crystal or External CMOS/TTL Clock
- ☐ Operation at 2600Hz from a Low Cost 3.58MHz TV Color Burst Crystal or 256kHz Ext. Clock
- ☐ Buffered Output Drives 600Ω Loads
- ☐ Single or Split Supply Operation
- ☐ Low Power CMOS Technology

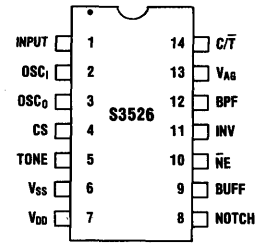
General Description

The S3526 is a low power CMOS Circuit which may be used in a variety of single frequency (SF) communication applications such as SF-Tone Receivers, Tone Remote Control in Mobile systems, Loopback Diagnostics in Modems, control of Echo Cancellers, dialing and privacy functions in Common Carrier Radio Telephone, etc. The main functional blocks of the S3526 include a low distortion tone (sinewave) generator whose frequency may be programmed using a crystal (i.e. 2600Hz using a low cost TV color burst crystal) or external clock time base; a bandpass filter used to extract tone information from the input signal; a band reject filter which is used to "Notch" out tone information from the input signal; and a buffer amplifier with selectable input (unfiltered input signal, or input signal with tone notched) capable of driving a 600Ω load.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$) ..... + 15.0V
Operating Temperature ..... 0°C to + 70°C
Storage Temperature ..... − 65°C to + 150°C
Input Voltage, All Pins ..... $V_{SS} - 0.3V < V_{IN} < V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to + 70°C, $(V_{DD} - V_{SS}) = 10V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation (Maximum @13.5V)		100	275	mW
R_{IN}	Input Resistances (Except Input)	8			MΩ
C_{IN}	Input Capacitances			15.0	pF

General Analog Signal Parameters: $T_A = 0°C$ to + 70°C, $(V_{DD} - V_{SS}) = 10V$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Straight Through Gain (Measured at − 10dBm0)	− 0.5	0	0.5	dB
Z_{IN}	Input Impedance (Input, Pin 1)		2.5		MΩ
TLP	Transmission Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level (+ 3dBm0)		2.1		VRMS
R_L	Load Resistance (BPF, NOTCH)	10			kΩ
R_L	Load Resistance (BUFF)	600			ohms
V_{OSB}	Buffer Output Offset Voltage		± 50	± 150	mV
ICN_P	Idle Channel Noise in Pass Condition		2		dBrnC0
V_{OUT}	Output Signal Level into R_L for NOTCH, BPF, BUFF	2.0	2.1		VRMS
V_{OT}	Sine Wave (Tone) Output (Load = 10KΩ)		$0.6(V_{DD} - V_{SS})$ ± 0.5dB		Vpk-pk
V_{TD}	Sine Wave Distortion ($f_{OSC} = 3.58MHz$) (See Figure 4)		− 35		dB

Filter Performance Specifications
Band Pass Filter Characteristics $T_A = 0°C$ to + 70°C, $(V_{DD} - V_{SS}) = 10V$, $f_{OSC} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{FS}	Maximum Input Voltage (+ 3dBm0)		2.1		VRMS
A_{BP}	Passband Gain @ − 10dBm0	− 0.8	0	+ 0.8	dB
I_{CN}	Idle Channel Noise		24		dBrnC0
V_{OS}	Output Offset		± 50	± 150	mV
	2600Hz Bandpass Filter Response (referenced from 2600Hz, + 3dBm0) (See Figures 1 and 2)				
	DC to 1600Hz		− 80		dB
	2100Hz		− 63	− 50	dB
	2400Hz		− 37	− 30	dB
	2540Hz		− 7.0	− 3	dB
	2560Hz	− 3	− 1.8		dB
	2640Hz	− 3	− 1.0		dB
	2660Hz		− 5.4	− 3	dB
	2800Hz		− 35	− 30	dB
	3100Hz		− 58	− 50	dB
	3600Hz		− 74		dB
DR	Dynamic Range (V_{FS} to ICN)		70		dB

COMMUNICATION PRODUCTS

Notch Filter Characteristics $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$ (Symmetrical Supplies), $f_{OSC} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{FS}	Maximum Input Voltage (+3dBm0)		2.1		VRMS
A_{BR}	Passband Gain @ −10dBm0)	−0.5	0	+0.5	dB
ICN	Idle Channel Noise		18		dBrnC0
V_{OS}	Output Offset		±100	±225	mV
DR	Dynamic Range (V_{FS} to ICN)		75		dB
	2600Hz Notch Filter Response (referenced from 1000Hz, (+3dBm0) (See Figures 1 and 3)				
	250Hz to 2200Hz	−0.5	±0.1	0.5	dB
	2200Hz to 2400Hz	−5.0		0.5	dB
	2585Hz to 2615Hz		−70	−53	dB
	2800Hz to 3000Hz	−5.0		0.5	dB
	3000Hz to 3400Hz	−0.5	±0.1	0.5	dB

Digital Electrical Parameters $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$

Symbol	Mode Control Logic Levels	Min.	Typ.	Max.	Units
V_{IH}	C/T CMOS Operation (Pin 14)	$V_{DD} - 0.5$		V_{DD}	V
V_{IL}	C/T TTL Operation (Pin 14)	V_{SS}		$V_{DD} - 4$	V
V_{IH}	CS for Low Speed Clock Input	$V_{DD} - 0.5$		V_{DD}	V
V_{IL}	CS for Crystal or High Speed Clock	V_{SS}		V_{AG}	V
	CMOS Logic Levels				
V_{IH}	Input Voltage "1" Level	$V_{AG} + 2$		V_{DD}	V
V_{IL}	Input Voltage "0" Level	V_{SS}		$V_{AG} - 2$	V

Control Pin Definitions

Pin#	Name	Connection	Operation	Note
14	C/T	V_{DD} to $(V_{DD} - 0.5V)$	CMOS Logic Levels	1
		$(V_{DD} - 4V)$ to V_{SS}	TTL Logic Levels	
4	CS	V_{DD}	Ext. Low Speed Sq. Wave Clock @ Pin 3	2
		V_{SS} or V_{AG}	Crystal Connected Between Pins 2 and 3 or High Speed Clock to Pin 2	
10	$\overline{NE}$	V_{DD} to .7 $(V_{DD} - V_{SS})$	Buffer Out = Input Signal	
		V_{SS} to .3 $(V_{DD} - V_{SS})$	Buffer Out = Notch Filter Out	

NOTES: 1) CMOS logic levels are same as V_{DD} and V_{SS} supply voltage levels. For TTL interface ground of TTL logic must be connected to V_{SS} supply pin.
2) For ext. low speed clock operation pin 2 must be connected to V_{DD}. For ext. high speed clock, drive pin 2, leave pin 3 open.
3) The performance specifications are guaranteed with ±5% power supplies for normal operation.

Pin Function Description

Pin	No.	Function
Input	1	This pin is the analog input to the filters and the buffer. It is a high impedance input ($Z \cong 2.5M\Omega$).
OSC_I OSC_O	2 3	These pins are the timing control for the entire chip. A crystal may be connected across these two pins in parallel with a 10MΩ resistor. Another option is to provide an ext clock at pin 3 and connect pin 2 to V_{DD}. TTL or CMOS may be used. As a third choice, a CMOS level external clock may be applied to pin 2 directly leaving pin 3 open.
CS	4	Clock Select-This pin when tied to V_{DD} configures the chip to operate from a low speed clock. When tied to V_{AG} or V_{SS} the chip operates from external crystal or high speed clock.
TONE	5	This is an output pin providing a sine wave with a frequency of fosc ÷ 1376 if CS is low or fosc ÷ 98 if CS is high.
V_{SS}	6	Negative supply voltage pin. Typically $-5V \pm 5\%$
V_{DD}	7	Positive supply voltage pin. Typically $+5V \pm 5\%$.
NOTCH	8	Band Reject (Notch) Filter-This is the output of the filter that notches the tone information from the input signal. It is capable of driving a load $\geq 10k\Omega$.
BUFF	9	Buffer Output-The buffer is capable of driving a 600Ω load and provides from its output either the signal input without filtering, or the signal input with the tone frequency notched out.
$\overline{NE}$	10	Notch Enable-This pin controls which signal is presented to the buffer input. A logic high (V_{DD}) connects the input signal. A logic low (V_{SS}) connects the output of the band reject (notch)filter.
INV	11	Inverting-This is the inverting input of the buffer.
BPF	12	Band Pass Filter-This is the output of the band pass filter which will pass any energy at the tone frequency present in the input signal. It is capable of driving a load $\geq 10k\Omega$.
V_{AG}	13	Analog Ground-This is the analog ground pin. When used with a single supply, this pin is ½ ($V_{DD} - V_{SS}$) ±100mV. When used with ±5V supplies, this point is at ground. The S3526 has internal voltage divider resistors to V_{DD} and V_{SS} of $\cong 20k\Omega$.
$C/\overline{T}$	14	CMOS/TTL-This pin determines whether CMOS or TTL levels will be accepted at pin 3 for a clock input. When tied to V_{DD}, the chip accepts CMOS logic levels. When tied to a point $\leq (V_{DD} - 4V)$, the chip accepts TTL levels. For crystal operation pin 14 should be at V_{DD}.

Application Information

The S3526 device is a very versatile filter chip. Although it was designed for the telephone market SF signaling application when used with the commonly available TV colorburst crystal, it will work over a wide range of frequencies. Typically, it will cover from 100Hz to 5kHz providing coverage of the entire voice band for in-band signaling.

Because it is a very high Q filter the transient response time must be considered when determining the maximum data rate for a particular frequency. This response is illustrated in Figure 5 and shows that it is quite adequate for 10 pulse-per-second (50% duty cycle) data rate at 2600Hz. But the same data rate could not be used at 500Hz, for example, as a detector could not differentiate between tone on and tone off conditions.

Figure 1. Typical Filter Performance Curves at 2600Hz

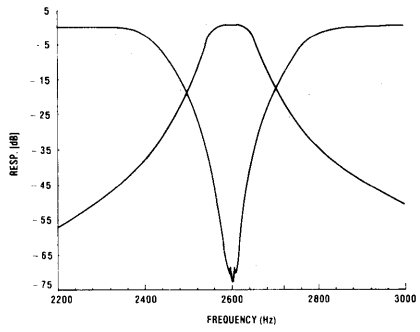


Figure 2. Typical Bandpass Response

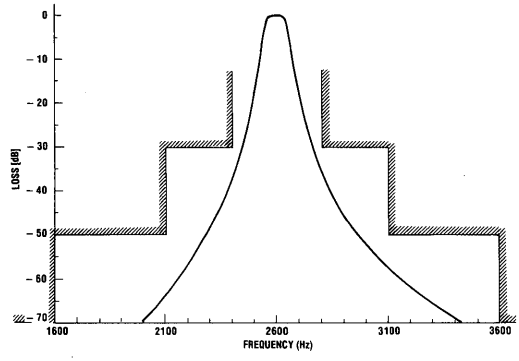


Figure 3. Typical Notch Response

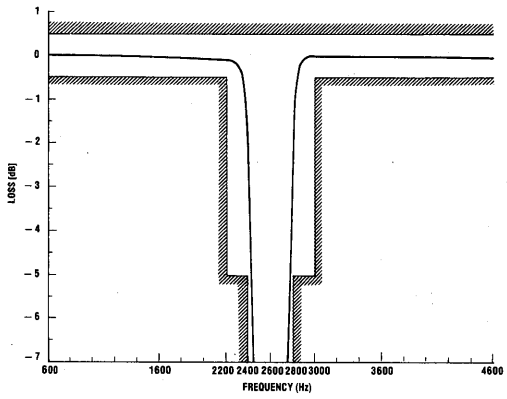


Figure 4. Typical Sine Wave Output Spectrum from Pin 5

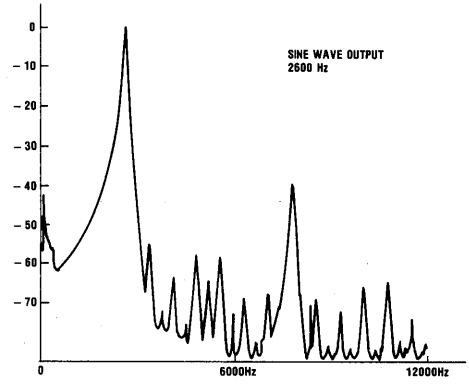


Figure 5. Typical Delay Characteristics at + 3dBmO with 2600Hz Pulsed at 10pps with 50% Duty Cycle

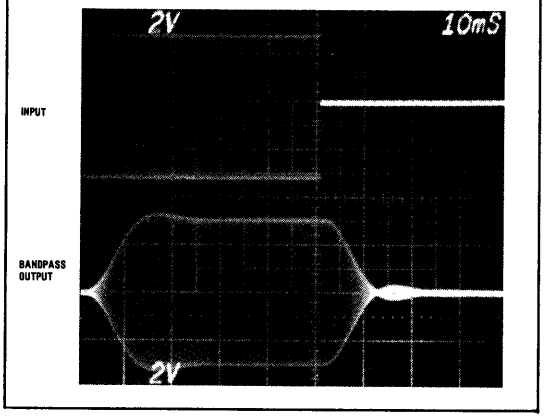
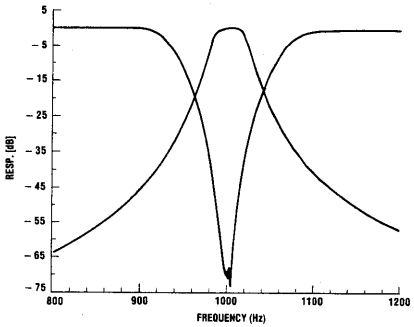


Figure 6. Typical Filter Performance Curves at 1000Hz



The combination of tone generator, notch filter, and bandpass filter allows one to generate a signaling tone at the sending end and notch it out at the receiving end, as well as detect it through the bandpass filter. For reliable detection the output of the bandpass filter can be compared with the output of the bandreject filter. If the output of the BR filter is within a fixed ratio of the BP filter (such as 10dB) then the signal present may be considered voice rather than signaling and ignored.

In situations where the entire voice band is desired except during signaling the buffer output can be switched straight through to the input. When the output of the filters indicates that a signaling tone is present, the $\overline{NE}$ pin can be switched low, switching the notch filter into the signal path to prevent the tone from reaching the listener or from being passed further down the system to another signaling receiver.

By using the notch filter with telephone accessories it can be guaranteed that the accessory will not violate the telephone company specifications about transmitting 2600Hz into the lines, causing disconnected calls.

Power Supplies

The S3526 will work with either single or dual power supplies. When used with dual power supplies (± 5V) the analog inputs and outputs will be referenced to ground. If an external clock signal is provided, rather than using a crystal, it must be swinging from V_{SS} to V_{AG} for TTL swings or from V_{SS} to V_{DD} for CMOS swings. If this is not convenient the signal can be capacitively coupled into pin 3 as illustrated in Figure 7. In the dual supply mode, the power supplies should track or maintain close tolerances for maximum accuracy. If the supplies should skew, the filter characteristics will change very slightly and in most applications, will have no effect at all but can be seen if the curves are plotted on high accuracy equipment.

When using the S3526 on a single power supply the analog inputs and outputs will be referenced to V_{AG} which is ½ ($V_{DD} - V_{SS}$). This means that the analog signals may need to be capacitively coupled in and out if they are normally ground referenced. For example, the input may appear as in Figure 8. But when an external clock is used in the single supply situation it can be direct coupled TTL levels referenced to ground.

Selecting Clocking Sources

The switched capacitor filter design allows the S3526 to be easily tuned by varying the clock frequency. This makes it useful for many applications in telephone signaling, data communications, medical telemetry, test equipment, automatic slide projectors, etc. The necessary clock frequency can be determined by multiplying the desired center frequency by 1376. This frequency

can then be provided from a crystal, an external clock, or a rate multiplier chip. With Clock Select (CS), pin 4 tied low the TONE, pin 5, will provide the desired frequency and the filters will be centered around that frequency. There are many common, low cost microprocessor frequency crystals available that might be very close to a desired frequency. Table 1 illustrates some possible application frequencies. For example, by using a standard 3.00MHz crystal the 2175Hz tone would be 2180Hz or .23% high.

If it is desired to use a lower frequency clock and precision tone generation is not required the external clock can be determined by multiplying the center frequency by 98.4, and tying Clock Select (CS) pin 4 high. Note that the TONE, pin, 5, is not accurate in this situation, being .41% higher than the filter center frequency, although it will fall well within the passband of both filters and be perfectly usable.

Figure 7. External Clock Drive

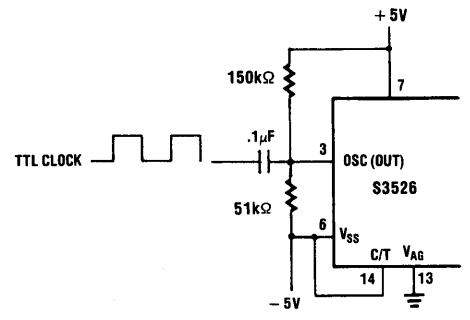


Figure 8.

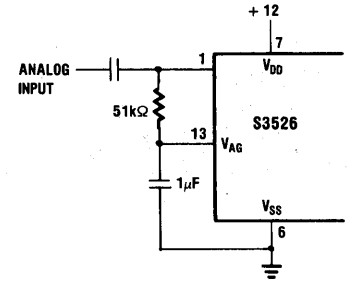


Table 1. Tone and Clock Frequencies for Various Applications

Tone In Hertz	Application	XTAL or HIGH Freq. Clock (MHz)	Ext. Clock Input (Hz)
550	Pilot Tone—Data Comm	.756800	54,120
1000	Test Tone	1.376000	98,400
1020	Test Tone	1.403520	100,368
1400	Medical Telemetry	1.926400	137,760
1600	SF Signaling—Military	2.201600	157,440
1800	Pilot Tone-Data Comm	2.476800	177,120
1850	Pilot Tone-Radio	2.545600	182,040
1950	Pilot Tone-Radio	2.683200	191,880
2125	Echo Suppressor Disable	2.924000	209,100
2150	Echo Suppressor Disable	2.958400	211,560
2175	Guard Tone-Radio	2.992800	214,020
2280	SF Signaling-Telephone	3.137280	224,352
2400	SF Signaling-Telephone	3.302400	236,160
2600	SF Signaling-Telephone	3.579545	256,000
2713	Loopback Tone-Datacom	3.733088	266,959
2800	SF Signaling-Telephone	3.852800	275,520
2805	Signaling Tone-Radio	3.859680	276,012
3825	SF Signaling-European	5.263200	376,380

AMI

A Subsidiary of Gould Inc.

Advanced Product Description **S3526M**

SINGLE FREQUENCY TUNABLE BANDPASS/NOTCH FILTER/TONE GENERATOR

Features

- ☐ Center Frequency of Filters Match and Track Frequency of Generated Tone
- ☐ Clock Tunable Tone Frequency, Adjustable Over a 100Hz to 5kHz Range
- ☐ Available Outputs: Bandpass, Notch, Straight Through Switchable to Notch, and Center Frequency Tone
- ☐ Operation from a Crystal or External CMOS/TTL Clock
- ☐ Operation at 2600Hz from a Low Cost 3.58MHz TV Color Burst Crystal or 2.048MHz or 1.536MHz External Clocks
- ☐ Buffered Output Drives 600Ω Loads
- ☐ Single or Split Supply Operation
- ☐ Low Power CMOS Technology

Typical Applications for the S3526M Bandpass/Notch Filter

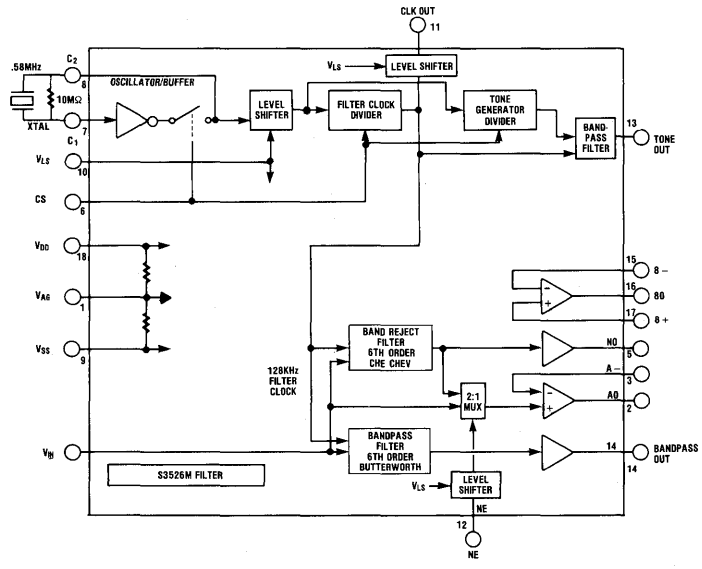
Telecommunications:

- ☐ 2600Hz Telephone Signaling
- ☐ Pilot Tone Filtering for Mobile Radio
- ☐ Telephone Loopback Line Testing
- ☐ Single Frequency Detection and/or Removal Filtering

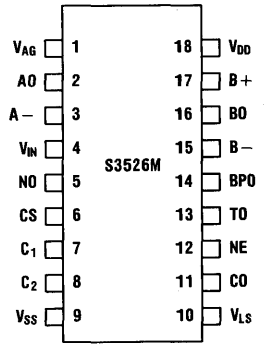
Instrumentation

- ☐ Data Communications
- ☐ Medical Telemetry
- ☐ Portable Instrumentation
- ☐ Test Tone Generation and Notching

Block Diagram



Pin Configuration



AMI

A Subsidiary of Gould Inc.

S3528

PROGRAMMABLE LOW PASS FILTER

Features

- ☐ Cutoff Frequency Selectable in 64 Steps Via Six Bit Control Word
- ☐ Continuously Tuneable Cutoff Frequency Variable Via External Clock (Crystal, Resonator, or TTL/CMOS Clock)
- ☐ Cutoff Frequency (f_C) Range of 10Hz to 20kHz, 40Hz to 20kHz Via Popular 3.58MHz TV Crystal
- ☐ Seventh Order Ellipitical Ladder Filter with Cosine Prefiltering Stage
- ☐ Passband Ripple: <0.1dB
- ☐ Stopband Attenuation: >51dB for $f>1.3f_C$
- ☐ Uncommitted Input and Output Op Amps for Anti-Aliasing and Smoothing Functions
- ☐ Steps May Be Custom Programmed from a Set of 2,048 Discrete Points Via Internal ROM
- ☐ Low Power CMOS Technology

Typical Applications for the S3528 and S3529 Programmable Filters

Telecommunications

- ☐ PBX and Trunk Line Status Monitoring
- ☐ Automatic Answering/Forwarding/Billing Systems
- ☐ Anti-Alias Filtering
- ☐ Adaptive Filtering

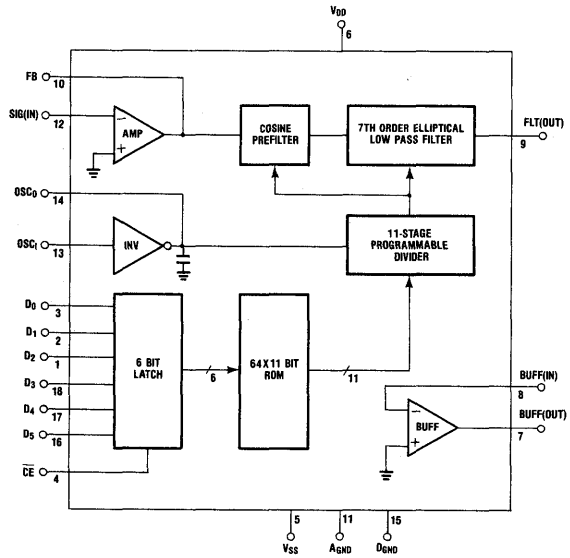
Remote Control

- ☐ Alarm Systems
- ☐ Heating Systems
- ☐ Acoustic Controllers

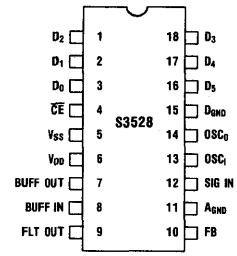
Test Equipment/Instrumentation

- ☐ Spectrum Analyzers
- ☐ Computer Controlled Analog Circuit Testers
- ☐ Medical Telemetry/Filtering
- ☐ ECG Signal Filtering
- ☐ Automotive Command Selection and Filtering

S3528 Block Diagram



Pin Configuration



Typical Applications for the S3528 and S3529 Programmable Filters (continued)

Audio

- ☐ Electronic Organs
- ☐ Speech Analysis and Synthesis
- ☐ Speaker Crossovers
- ☐ Sonabuoys
- ☐ Spectrum Selection
- ☐ Low Distortion Digitally Tuned Audio Oscillators

General Description

The S3528's CMOS design using switched-capacitor techniques allows easy programming of the filter's cutoff frequency (f_C) in 64 steps via a six-bit control word. For dynamic control of cutoff frequencies, the S3528 can operate as a peripheral to a microprocessor system with the code for the cutoff frequency being latched in from the data bus. When used with the companion high pass filter, the S3529, a bandpass or a bandreject filter with a variable center frequency is obtained. For special applications the S3528's internal ROM can be customized to accommodate a specific set of cutoff frequencies from a choice of 2,048 possibilities.

Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$)	+ 15.0V
Operating Temperature	0°C to + 70°C
Storage Temperature	− 65°C to + 150°C
Input Voltage, All Pins	$V_{SS} - 0.3V \leq V_{IN} \leq V_{DD} + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to $+70°C$, $(V_{DD} - V_{SS}) = 10V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation @10V @13.5V		60 135	110 225	mW mW
R_{IN}	Input Resistance (Pins 1-4, 8, 12, 13, 16-18)	8			MΩ
C_{IN}	Input Capacitance (Pins 1-4, 8, 12, 13, 16-18)			15.0	pF

General Analog Signal Parameters: $(V_{DD} - V_{SS}) = 10V$, $T_A = 0°C$ to $+70°C$, $f_{clock} = 3.58MHz$

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Pass Band Gain at 0.6 f_C	−0.5	0	0.5	dB
V_0	Reference Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level (+ 3dBm0)		2.1		VRMS
R_L	Load Resistance FLT OUT, Pin 9	10			kΩ
R_L	Load Resistance BUFF OUT, Pin 7	600			ohms
V_{OUT}	Output Signal Level into R_L for FLT OUT, BUFF OUT, $V_{IN} = 2.1V$	2.0	2.1		VRMS
THD	Total Harmonic Distortion at .3f_C		.3		%
WBN	Wideband Noise (to 30kHz) $f_C = 3.2kHz$		.15		mVRMS
WBN	Wideband Noise (to 80kHz) $f_C = 15kHz$		.13		mvRMS
ICN	Idle Channel Noise $f_C = 3200Hz$		8	23	dBrnC0
V_{OS}	Buffer Output (Pin 7) Offset Voltage		±10	±30	mV
V_{OFS}	Filter Output (Pin 9) Offset Voltage		±80	±200	mV

Filter Performance Specifications

Low Pass Filter Characteristics: $f_{clock} = 3.58MHz$, $(V_{DD} - V_{SS}) = 10V$, $T_A = 0°C$ to $+70°C$

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
	Pass Band Ripple (Ref. 0.6 f_C)		−0.5	±0.05	0.5	dB
Filter Response(1): F_C = 3200Hz (Pin 9)						
	(See Figure 5)	(fc) 3200Hz	−0.5	±0.1	0.5	dB
		(1.06fc) 3372Hz	−5.5	−3.0	−0.5	dB
		(1.27fc) 4060		−42		dB
		(1.3fc) 4155		−51	−48	dB
		(1.32fc) 4235		−65	−48	dB
		(1.62fc) 5175		−75	−48	dB
	(1.3fc Upward)	4155 to 100,000Hz		< −51		dB
DR	Dynamic Range (V_{FS} to ICN)			82		dB

Digital Electrical Parameters: $V_{DD} = +5V$, $V_{SS} = -5V$, $T_A = 0°C$ to $+70°C$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	Volts
V_{IL}	Input Low Voltage	V_{SS}		0.8	Volts
I_N	Input Leakage Current ($V_{IN} = 0$ to 4VDC)			10	μADC
C_{IN}	Input Capacitance			15	pF
Digital Timing Characteristics					
t_{CE}	Chip Enable Pulse Width	200	300		nsec
t_{AS}	Address Setup Time		300		nsec
t_{AH}	Address Hold Time		20		nsec
f_{osc}	Crystal Oscillator Frequency(2)		3.58		MHz
t_{SET}	Settling Time from $\overline{CE}$ to Stable f_C ($f_C = 3200$)(3)		6		msec

1.) Filter Response Referenced to f = 1,920Hz

2.) The tables are based on common TV crystal. See paragraph on "Clock Frequencies" for more detail.

3.) $t_{SET} = \frac{10,000}{f_c} + 3msec$

Pin Function Description

Pin Name	Number	Function
V_{DD}	6	Positive supply voltage pin. Normally +5V ±10%.
V_{SS}	5	Negative supply voltage pin. Normally −5V ±10%.
A_{GND}	11	Analog ground reference point for analog input and output signals. Normally connected to ground.
D_{GND}	15	Digital ground reference point for digital input signals. Normally connected to ground.
D_0	3	Control word Inputs: The set of six bits allows selection of one of sixty-four cutoff frequencies. The 6 bit control word is latched on the rising edge of $\overline{CE}$. The high-impedance inputs may be bridged directly across a microprocessor data bus. These inputs are TTL or CMOS compatible. A "1" is 2.0V to V_{DD}, and a "0" is 0.8V to V_{SS}.
D_1	2	
D_2	1	
D_3	18	
D_4	17	
D_5	16	
$\overline{CE}$	4	Chip Enable: This pin has 3 states. When $\overline{CE}$ is at V_{DD} the data in the latch is presented to the ROM and the inputs have no effect. When $\overline{CE}$ is at ground the data presented on the inputs is read into the latch but the previous data is still in the ROM. Returning $\overline{CE}$ to V_{DD} presents the new data to the ROM and f_C changes. When $\overline{CE}$ is at V_{SS} the inputs go directly to the ROM, changing f_C immediately. This is the configuration for a fixed filter; $\overline{CE}$ is at V_{SS} and the D_0 through D_5 are tied to V_{DD} or V_{SS}/D_{GRND} depending on the desired f_C.

Pin Function Description (continued)

Pin Name	Number	Function
OSC_I OSC_O	13 14	Oscillator In and Oscillator Out: Placing a crystal and a 10MΩ resistor across these pins creates the time base oscillator. An inexpensive choice is to use the 3.58MHz TV colorburst crystal.
SIG IN	12	Signal Input: This is the inverting input of the input op amp. The non-inverting input is internally connected to Analog Ground.
FB	10	Feedback: This is the feedback point for the input op amp. The feedback resistor should be ⩾10kΩ for proper operation.
FLT OUT	9	Filter Out: This is the high impedance output of the programmable low pass filter. Loads must be ⩾10kΩ.
BUFF IN	8	Buffer Input: The inverting input of the buffer amplifier.
BUFF OUT	7	Buffer Out: The buffer amplifier output to drive low impedance loads. This pin may drive as low as 600Ω loads.

Example of Circuit Connection for S3528
Figure 1. Stand Alone Operation

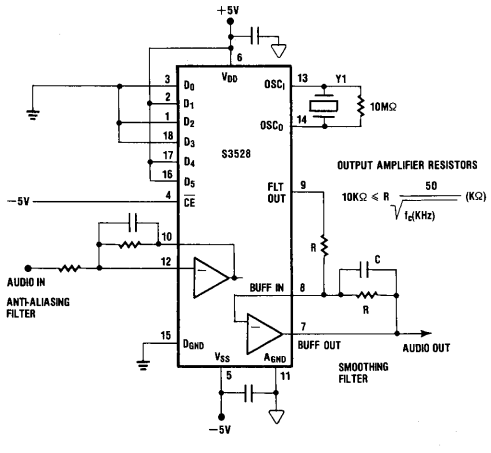
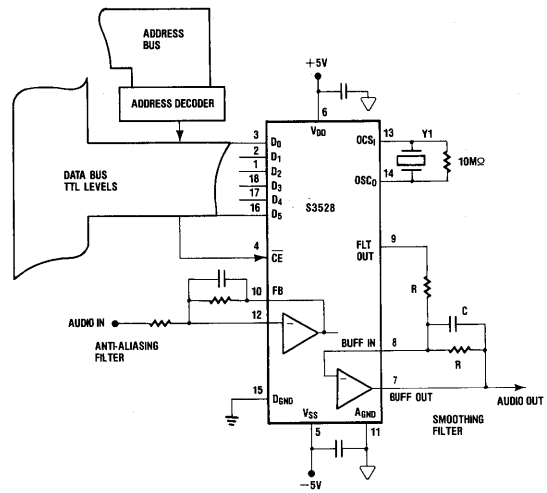


Figure 2. Microprocessor Interface



Operation

S3528 Filter is a CMOS Switched Capacitor Filter device designed to provide a very accurate, very flat, programmable filter that can be used in fixed applications where only one cutoff frequency is used, or in dynamic applications where logic or a microprocessor can select any one of 64 different cutoff frequencies. It is normally clocked by an inexpensive TV color burst crystal and provides the cutoff frequencies seen in Table 1 when the Data Bus pins are programmed.

All that is required for fixed operation is a 10MΩ resistor, the 3.58MHz TV crystal, and some resistors and capacitors around the input and output amplifiers to set the gain, anti-aliasing, and smoothing. The Data Bus pins are programmed from the table to either a "1" (+5V) or a "0" (ground or −5V) for the desired cutoff frequency. The $\overline{CE}$ pin is tied low, to V_{SS}.

Operation (continued)

The ROM is addressed by the contents of the latch and presents an 11-bit word to the programmable divider which divides f_{CLK}.

The FILTER OUT pin is capable of driving a 10kΩ load directly or, for smoothing and driving a 600Ω load, the output buffer amplifier can be used for impedance matching.

As illustrated in the curves of Figures 3, and 5 through 7, the passband ripple (for fc<18kHz) is less than ±0.1dB and the stop band rejection is better than 50dB, as measured on a network analyzer.

For microprocessor controlled operation, the Data Bus can be bridged across a regular TTL bus and when $\overline{CE}$ is strobed, the data present will be latched in and the filter will settle down to its new cutoff frequency. In CMOS systems, the Data Bus and $\overline{CE}$ can be swung rail-to-rail. A_{GND} and D_{GND} must be at ½ the supply voltage.

The following table illustrates the available cutoff frequencies based on using a 3.58MHz TV crystal for a time base, by approximately 100Hz steps through the voice band from 100Hz to 3900Hz. Note that the hex input code for each frequency in the voice band is one-hundredth of the cutoff frequency. For 3200Hz, the hex code is 32, for 900Hz it is 09. Additional frequencies are listed with their codes on the right side of the Table 1.0.

Table 1.0—Standard Frequency Table: Programmable Filter S3528. f_{CLOCK} = 3.58MHz

Voice Band

Input Code (HEX) D_5–D_0	Divider Ratio	f_c Actual (Hz)
00	2048	44
01	895	100
02	447	200
03	298	300
04	224	399
05	179	500
06	149	601
07	128	699
08	112	799
09	99	904
10	89	1005
11	81	1105
12	74	1209
13	69	1297
14	64	1398
15	60	1491
16	56	1598
17	53	1688
18	50	1790
19	47	1904
20	45	1989
21	43	2081
22	41	2183
23	39	2295
24	37	2418
25	36	2486
26	34	2632
27	33	2711
28	32	2797
29	31	2887
30	30	2983
31	29	3086
32	28	3196
33	27	3314
34	26	3442
36	25	3579
37	24	3728
39	23	3891

Additional Points Available

Input Code (HEX) D_5–D_0	Divider Ratio	f_c Actual (Hz)
0A	188	476
0B	358	250
0C	90	994
0D	87	1028
0E	85	1053
0F	78	1147
1A	61	1467
1B	58	1542
1C	52	1721
1D	46	1945
1E	44	2034
1F	40	2237
2A	38	2350
2B	35	2557
2C	22	4067
2D	20	4474
2E	18	4971
2F	16	5593
35	15	5965
38	14	6392
3A	12	7457
3B	10	8949
3C	9	9943
3D	6	14915
3E	5	17897
3F	4	22372

$$f_{cutoff} = \frac{f_{CLOCK}}{40\ (\text{Divider Ratio})}$$

Figure 3. Family off Loss Curves for 4 Different Control Codes

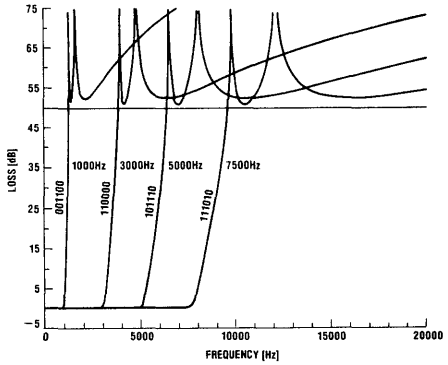


Figure 4. Address and Chip Enable Timing

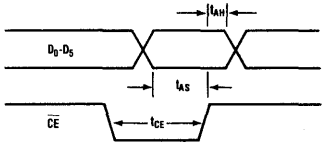


Figure 5. Loss Curve, Control = 110010, f_C = 3200Hz

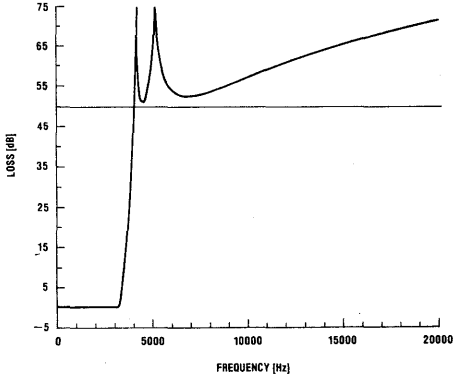


Figure 6. Passband Control Detail, Control = 110010, f_C = 3200Hz

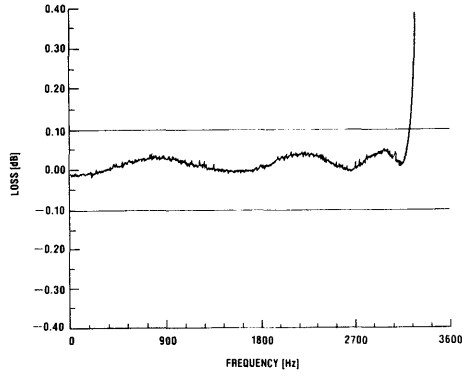


Figure 7. Family of Loss Curves for 4 Different Control Codes

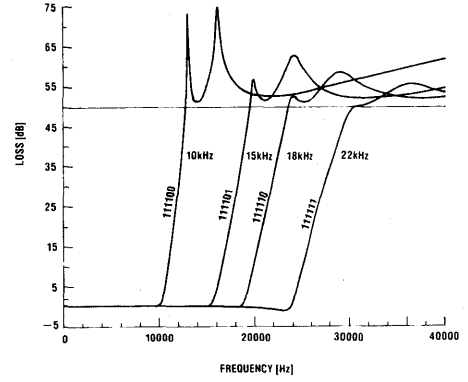


Figure 8. Loss and Group Delay, Fc = 3200Hz

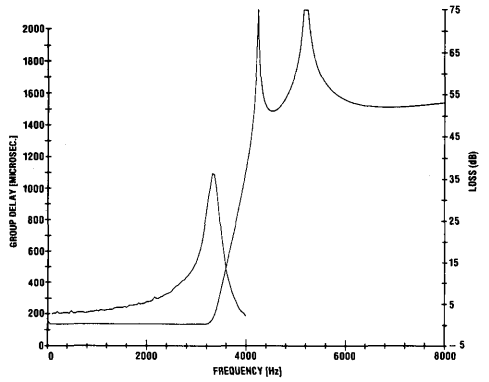
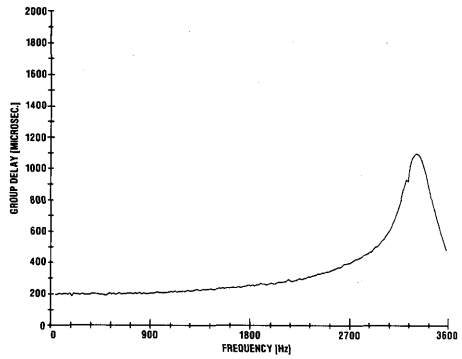


Figure 9. Group Delay, Control = 110010, FC = 3.2kHz

$$GD_{f_C = x} \doteq GD_{f_C = 3.2kHz} \left(\frac{3.2kHz}{x\ kHz} \right)$$



Applications Information

Many filter applications can benefit from the S3528, particularly if extremely flat passband response with precise, repeatable cutoff frequencies are required. Or, if the same performance is required at different frequencies it can be switched or microprocessor controlled. The circuits (Figures 1 and 2) illustrate how the S3528 might be connected for two different uses. The "stand alone" drawing (Figure 1) shows how it would be programmed as a fixed, 3200Hz low pass filter. The other drawing (Figure 2) shows a microprocessor driven application that lets the cutoff frequency be varied on command.

Some fields that can use such a filter are speech analysis and scrambling, geo-physical instrumentation, under water accoustical instrumentation, two-way radio, telecommunications, electronic music, remotely programmable test equipment, tracking filter, etc.

Anti-Aliasing

In planning an application the basic fundamentals of sampling devices must be considered. For example, aliasing must be taken into consideration. If a frequency close to the sampling frequency is presented to the input it can be aliased or folded back into the passband. Because the S3528 has an input cosine filter the effective sample frequency is twice the filter clock frequency of 40 times the cutoff frequency. If $f_C = 1000Hz$ and a signal of 79,200Hz is put into the filter, it will alias the 80kHz effective sampling frequency of the input cosine filter and appear as an 800Hz signal at the output. This means that for some applications the input op amp must be used to construct a simple one or two pole RC anti-aliasing filter to insure performance. In many situations, however, this will not be necessary since the input signal will already be band-limited.

Smoothing

In addition, all sampling devices will have aliased components near the clock frequency in the output. For example, there will be small components at $f_{clk} \pm f_{in}$ in the output waveform. This can be reduced by constructing a simple smoothing filter around the output buffer amplifier. Because of the sinx/x characteristics of a sample and hold stage the aliasing components are already better than 30dB down. The clock feed through is approximately −50dBV. This means that a simple one pole filter can provide another 20dB of rejection to keep the aliasing below 50dB down. In the case of a 3kHz f_{CUTOFF} and the smoothing filter designed for a 3dB point at $4f_{CUTOFF}$ the smoothing filter will affect

Smoothing (continued)

the 3kHz point by .25dB. If this is not desirable then the smoothing filter might be constructed as a second order filter.

For a fixed application, anti-aliasing and smoothing are straight forward. For a dynamic operation, the desired operating range of frequencies must be considered carefully. It may be necessary to switch in or out additional components in the RC filters to move cutoff frequencies. The S3528 has a ratio of cutoff frequencies of 550:1 and to use the full range would require some switching.

Notch Rejection

The filter is designed to have 51dB of rejection at $1.3f_{CUTOFF}$ and greater. If greater rejection of a specific tone or signal frequency is desired, the cutoff frequency can be selected to position the undesired tone at $1.325f_{CUTOFF}$ or $1.62f_{CUTOFF}$. This will place it in a notch as illustrated in Figure 5.

The S3529 (High Pass Filter) and the S3528 (Low Pass Filter) can be used together to make either Band Pass or Band Reject/Notch filters. The control code selection determines the bandwidth of the resulting filter.

It should be noted that with the S3528 and S3529 data pins connected in parallel and their analog inputs and outputs in series a bandpass filter of approximately 10% bandwidth is created.

Figure 10. S3528 and S3529 in Parallel Notch Configuration—Narrow Bandwidth

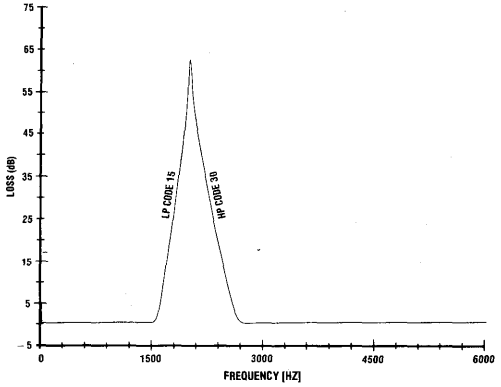


Figure 11. Cascaded S3528 and S3529 Control = 100001 Bandpass Configuration—10% Bandwidth

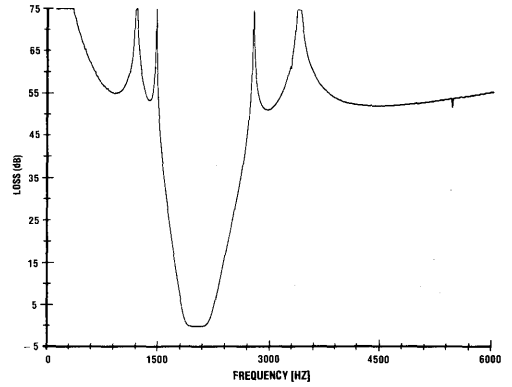


Figure 12. S3528 and S3529 in Parallel Notch Configuration—Wide Bandwidth

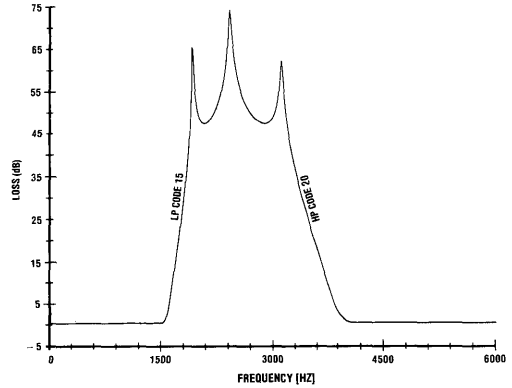
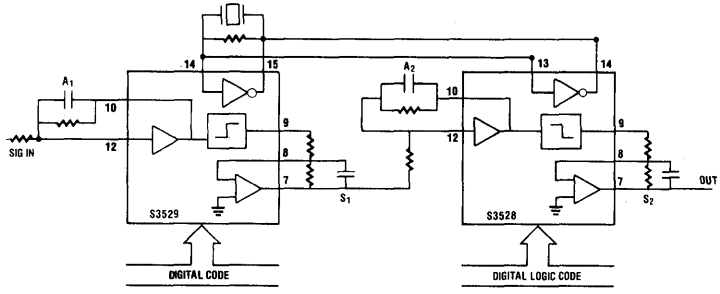


Figure 13. Bandpass Application: General Case Configuration



Note:

– Anti-aliasing and smoothing filters on both chips A1, A2, S1, S2

– Lowpass after highpass to remove higher harmonics, unless cosine input filter of lowpass needed to clean noisy input signal

– For wider band width two different oscillators can be used.

– If filter clock (f_{clock}) for lowpass is an integer multiple of the f_{clock} for highpass, then S1 and A2 may be removed without causing beat frequencies.

- For same digital logic code
  N = multiple of clock#1 to clock#2

$$f_{cL} = \frac{.9 f_{cu}}{N}$$

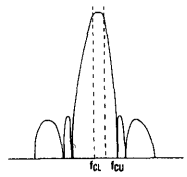


Figure 14. Notch Applications: General Case Configuration

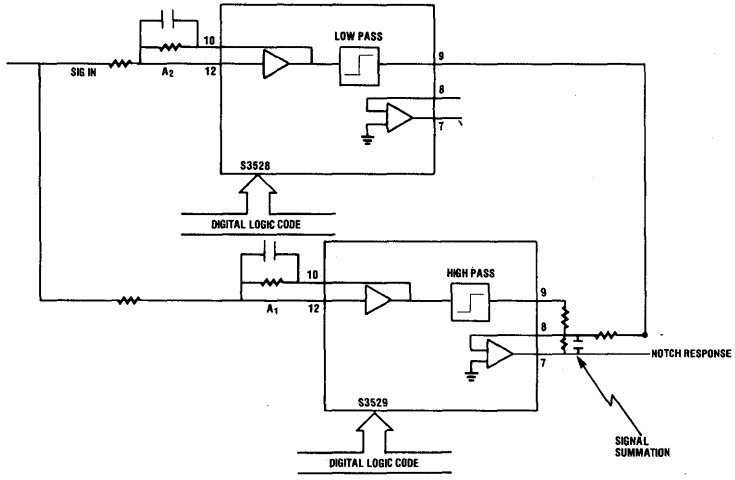
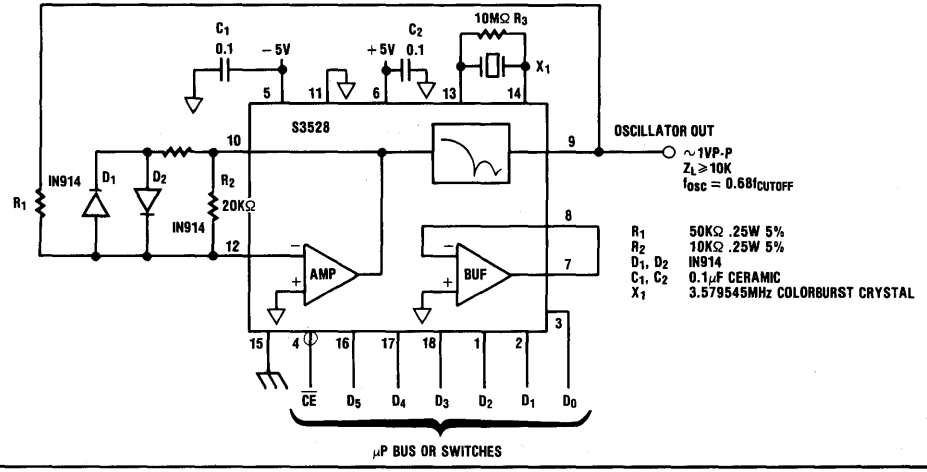


Figure 15. Low Distortion Digitally Tuned Audio Oscillator Application Circuit



Crystal Oscillator

The S3528 crystal oscillator circuit requires a 10 Meg ohm resistor in parallel with a standard 3.58MHz television colorburst crystal. For this application, however, crystals with relaxed tolerances can be used. Specifications can be as follows:

Frequency	3.579545 ±.02%
RS≤180Ω	L_M~96MH
C_L = 18pF	C_h = 7pF

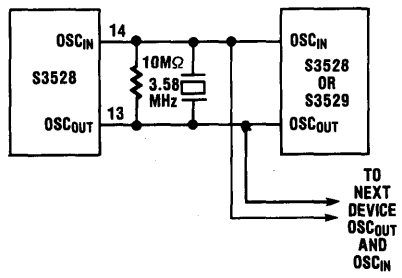
Alternate Clock Configurations

If 3.58MHz is already available in the system it can be applied directly as a logic level to the OSC_{IN} (pin 13). [Max. zero~30% (V_{DD}-V_{SS}), min. one~70% (V_{DD}-V_{SS})]. Waveforms not satisfying these logic levels can be capacitively coupled to OSC_{IN} as long as the 10 Meg ohm feedback resistor is installed as shown in Figure 16.

Although the tables are constructed around the TV colorburst crystal, other clock frequencies can be used from crystals or external clocks to achieve any cutoff frequency in the operating range. For example, by using a rate multiplier and duty-cycle restorer circuit between the system clock and the S3528, and switching the inputs to the S3528, almost any cutoff frequency between 40Hz and 35kHz can be selected. The clock input frequency can be anywhere between 500kHz and 5MHz.

In addition to crystals or external clocks the S3528 can be used with ceramic resonators such as the Murata CSA series "Ceralock" devices. All that is required is the resonator and 2 capacitors to V_{SS}. Although the resonators are not quite as accurate as crystals they can be less expensive.

Figure 16. S3528 Driving Additional S3528 or S3529 Devices



AMI®

A Subsidiary of Gould Inc.

Advanced Product Description **S3529**

PROGRAMMABLE HIGHPASS FILTER

Features

- ☐ Cutoff Frequency Selectable in 64 Steps Via Six-Bit Control Word
- ☐ Cutoff Frequency (f_C) Range of 10Hz to 20kHz, 40Hz to 20kHz Via 3.58MHz TV Crystal
- ☐ Seventh Order Elliptical Filter
- ☐ Passband Ripple: 0.1dB
- ☐ Stopband Attenuation: 51dB for f<.77 f_C
- ☐ Clock Tunable Cutoff Frequency Continuously Variable Via External Clock (Crystal, Resonator, or TTL/CMOS Clock)
- ☐ Uncommitted Input and Output Op Amps for Anti-Aliasing and Smoothing Functions
- ☐ Low Power CMOS Technology

Typical Applications for the S3528 and S3529 Programmable Filters

Telecommunications

- ☐ PBX & Trunk Line Status Monitoring
- ☐ Automatic Answering/Forwarding/Billing Systems
- ☐ Adaptive Filtering

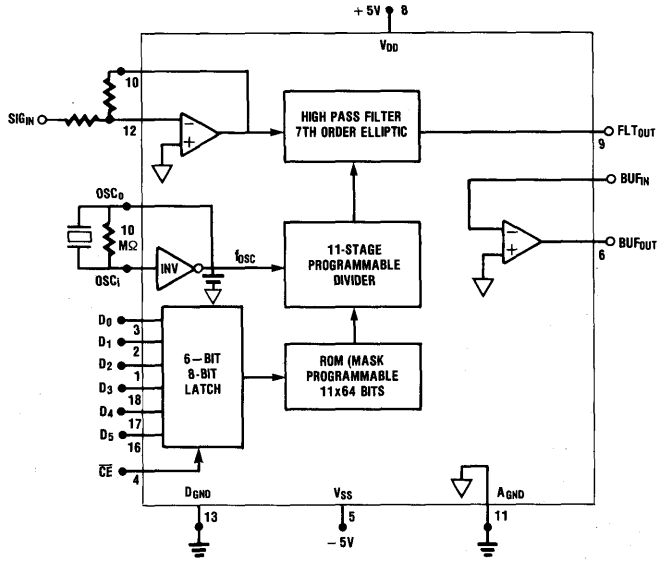
Remote Control

- ☐ Alarm Systems
- ☐ Heating Systems
- ☐ Acoustic Controllers

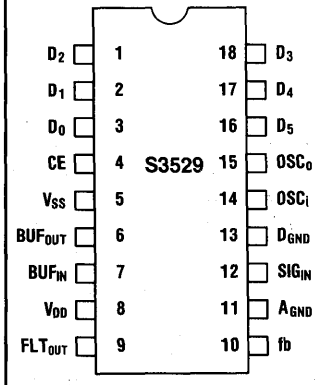
Test Equipment/Instrumentation

- ☐ Spectrum Analyzers
- ☐ Computer Controlled Analog Circuit Testers
- ☐ Medical Telemetry Filtering
- ☐ ECG Signal Filtering
- ☐ Automotive Command Selection and Filtering

Block Diagram



Pin Configuration



General Description

The S3529's CMOS design using switched-capacitor techniques allows easy programming of the filter's cut-off frequency (f_C) in 64 steps via a six-bit control word. For dynamic control of cutoff frequencies, the S3529 can operate as a peripheral to a microprocessor system with the code for the cutoff frequency being latched in from the data bus. When used with the companion low pass filter, the S3528, a bandpass filter with a variable center frequency is obtained. For special applications the S3529's internal ROM can be customized to accomodate a specific set of cutoff frequencies from a choice of 2,048 possiblities.

Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$) ..... + 15.0V
Operating Temperature ..... 0°C to + 70°C
Storage Temperature ..... − 65°C to + 150°C
Input Voltage, All Pins ..... $V_{SS} - 0.3V \leq V_{IN} \leq + 0.3V$

D.C. Electrical Operating Characteristics: $T_A = 0°C$ to $+ 70°C$, $(V_{DD} - V_{SS}) = 10V$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation @10V		60	110	mW
	@13.5V		135	225	mW
R_{IN}	Input Resistance (Pins 1-4, 7, 12, 14, 16-18)	8			MΩ
C_{IN}	Input Capacitance (Pins 1-4, 7, 12, 14, 16-18)			15.0	pF

Digital Electrical Parameters: $V_{DD} = + 5V$, $V_{SS} = - 5V$, $T_A = 0°C$ to $+ 70°C$ unless otherwise specified

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	V
V_{IL}	Input Low Voltage	V_{SS}		0.8	V
I_N	Input Leakage Current ($V_{IN} = 0$ to 4VDC)			10	μADC
C_{IN}	Input Capacitance			15	pF

Digital Timing Characteristics

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
t_{CE}	Chip Enable Pulse Width	200	300		ns
t_{AS}	Address Setup Time		300		ns
t_{AH}	Address Hold Time		20		ns
f_{OSC}	Crystal Oscillator Frequency(1)		3.58		MHz
t_{SET}	Settling Time From CE to Stable f_C ($f_C = 3200$)(2)		6		ms

Notes:

1. The tables are based on the common 3.58MHz color burst TV crystal.
2. $t_{SET} = \frac{10,000}{f_C} + 3msec$

General Analog Signal Parameters: ($V_{DD} - V_{SS}$) = 10V, T_A = 0°C to + 70°C, f_{OSC} = 3.58MHz

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Pass Band Gain at 2.2 f_C	−0.5	0	0.5	dB
V_{MAX}	Reference Level Point (0dBm0)		1.5		VRMS
V_{FS}	Maximum Input Signal Level (+3dBm0)		2.1		VRMS
R_L	Load Resistance (FLT_{OUT}, Pin 9)	10			kΩ
R_L	Load Resistance (BUF_{OUT}, Pin 7)	600			Ω
V_{OUT}	Output Signal Level into R_L for FLT_{OUT}, BUF_{OUT}	2.0	2.1		VRMS
T_{HD}	Total Harmonic Distortion: Input code 22, Frequency = 2kHz; Bandlimited to $f_{clk/2}$		.15		%
WBN	Wideband Noise: Input code 22, Bandlimited to 15kHz		.25		mVRMS
V_{OS}	Buffer Output (Pin 7) Offset Voltage		±10		mV
V_{OES}	Filter Output (Pin 9) Offset Voltage		±80		mV

Filter Performance Specifications: High Pass Filter Characteristics (f_{OSC} = 3.58MHz) ($V_{DD} - V_{SS}$) = 10V, T_A = 0°C to + 70°C

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
	Passband ripple (Ref. 2.2 f_C) $f_C \leq f < 7f_C$		−0.5	±0.05	0.5	dB
Filter Response: f_C = 1005Hz						
	(f_C)	1005Hz	−0.5	±0.1	0.5	dB
	(0.96 f_C)	960	−5	−3.0	−1	db
	(0.768 f_C)	772		−53	−43	db
	(.754 f_C)	758		−85	−43	db
	(.614 f_C)	617		−70	−43	db
	Stopband	$f < .768\ f_C$		< −53		db
DR	Dynamic Range (V_{FS} to WBN)			78		dB

Pin Description

Pin Name	Pin#	Function
V_{DD}	8	Positive supply voltage pin. Normally +5 volts.
V_{SS}	5	Negative supply voltage pin. Normally −5 volts.
A_{GND}	11	Analog ground reference point for analog input signals. Normally connected to ground.
D_{GND}	13	Digital ground reference point for digital input signals. Normally connected to ground.
D_0	3	The input bus to allow selection of the desired cutoff frequency. The value of the word presented to these pins selects the cutoff frequency. It is latched in on the rising edge of $\overline{CE}$. These are high impedance CMOS inputs and can be bridged directly across a microprocessor data bus.
D_1	2	
D_2	1	
D_3	18	
D_4	17	
D_5	16	

Pin Description (Continued)

Pin Name	Pin#	Function
$\overline{CE}$	4	Chip Enable: This pin has 3 states. When $\overline{CE}$ is at V_{DD} the data in the latch is presented to the ROM and the inputs have no effect. When $\overline{CE}$ is at ground the data presented on the inputs is read into the latch but the previous data is still in the ROM. Returning $\overline{CE}$ to V_{DD} presents the new data to the ROM and f_{cutoff} changes. When $\overline{CE}$ is at V_{SS} the inputs go directly to the ROM, changing f_{cutoff} immediately. The configuration for a fixed filter is: $\overline{CE}$ at V_{SS} and the D_0 through D_5 are tied to V_{DD} or V_{SS}/D_{GND} depending on the desired f_{cutoff}.
OSC_i	14	Oscillator In and Oscillator Out. Placing a crystal and a 10MΩ resistor across these pins creates the time base oscillator. An inexpensive choice is to use the 3.58MHz TV crystal.
OSC_o	15	
SIG_{IN}	12	Signal Input. This is the inverting input of the input op amp. The non-inverting input is internally connected to Analog Ground.
FB	10	Feedback. This is the feedback point for the input op amp. The feedback resistor should be ⩾10kΩ for proper operation.
FLT_{OUT}	9	The high impedance output of the high pass filter. Load should be 10KΩ.
BUF_{IN}	7	The inverting input of the buffer amplifier.
BUF_{OUT}	6	The buffer amplifier output to drive low impedance loads. Load should be ⩾600Ω.

Example of Circuit Connection for S3529

Figure 1. Stand Alone Operation

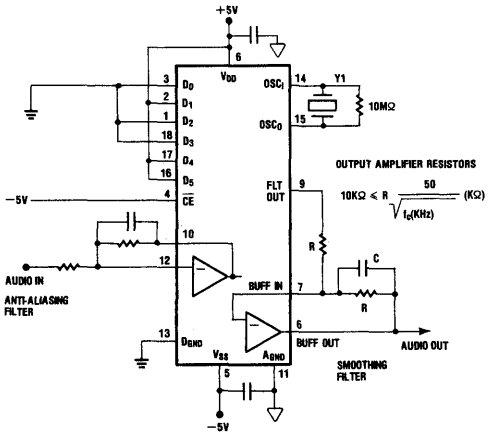


Figure 2. Microprocessor Interface

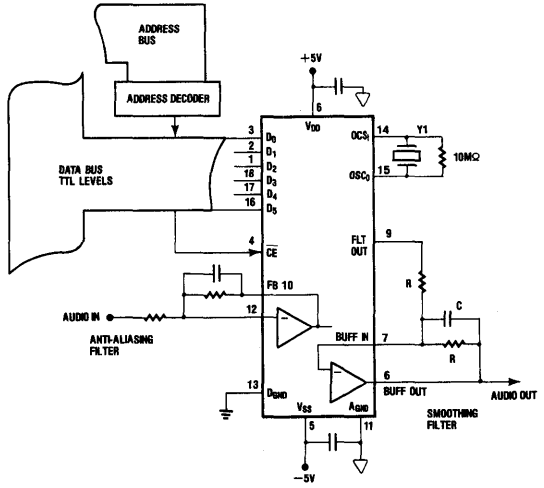


Table 1. Standard Frequency Table: Programmable Filter S3529, f_{clock} = 3.58MHz

Voice Band Input D_5-D_0 (HEX)	Divider Ratio	f_c Actual (Hz)	Additional Points Input Code D_5-D_0 (HEX)	Divider Ratio	f_c Actual (Hz)
00	2048	40	0A	188	433
01	895	91	0B	358	227
02	447	182	0C	90	904
03	298	273	0D	87	935
04	224	363	0E	85	957
05	179	455	0F	78	1043
06	149	546	1A	61	1334
07	128	635	1B	58	1402
08	112	726	1C	52	1565
09	99	822	1D	46	1768
10	89	914	1E	44	1849
11	81	1005	1F	40	2034
12	74	1099	2A	38	2136
13	69	1179	2B	35	2325
14	64	1271	2C	22	3697
15	60	1355	2D	20	4067
16	56	1453	2E	18	4519
17	53	1535	2F	16	5085
18	50	1627	35	15	5423
19	47	1731	38	14	5811
20	45	1808	3A	12	6779
21	43	1892	3B	10	8135
22	41	1985	3C	9	9039
23	39	2086	3D	6	13559
24	37	2198	3E	5	16270
25	36	2260	3F	4	20338
26	34	2392			
27	33	2465			
28	32	2543			
29	31	2625			
30	30	2712			
31	29	2805			
32	28	2905			
33	27	3013			
34	26	3129			
36	25	3254			
37	24	3389			
39	23	3537			

$$f_{CUTOFF} = \frac{f_{clock}}{44\ (\text{Divider Ratio})}$$

Alternate Clock Configurations

If 3.58MHz is already available in the system it can be applied directly as a logic level to the OSC_{IN} (pin 14). (Max. zero~30% V_{DD}, min. one~70% V_{SS}). Waveforms not satisfying these logic levels can be capacitively coupled to OSC_{IN} as long as the 10MΩ feedback resistor is installed as shown in Figure 3.

Figure 3. External Driving S3529 Pin OSC_i

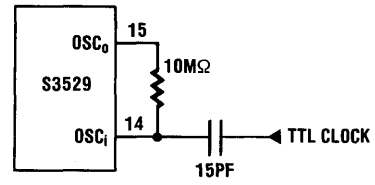


Figure 4. Passband Detail, Control = 110010, f_c = 1005Hz

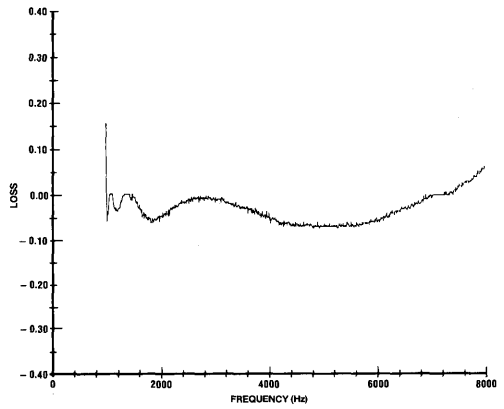


Figure 5. Loss Curve, Control = 110010, f_c = 1005Hz

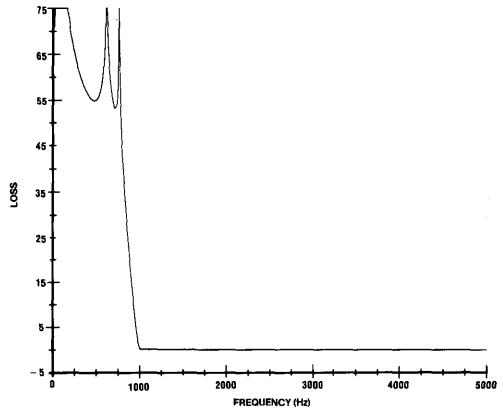


Figure 6. Loss Response, DC to Clock Detail, Control = 110010, f_c = 1005Hz

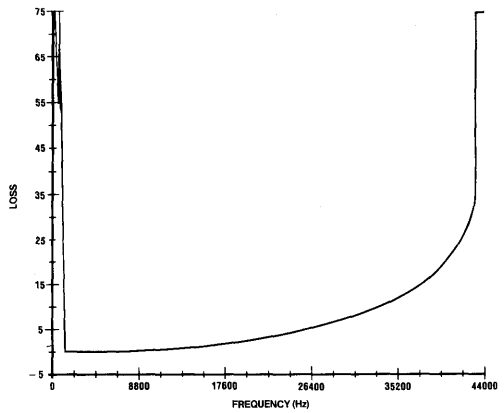


Figure 7. Cascaded S3528 And S3529 Control=100001 Bandpass Configuration—10% Bandwidth

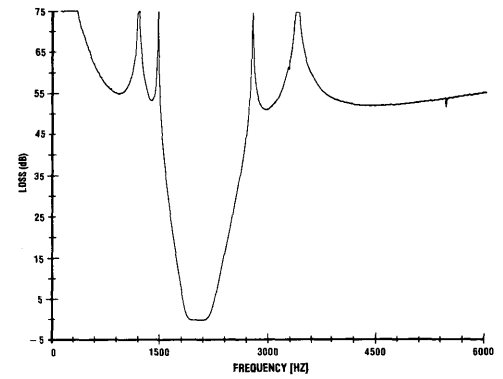


Figure 8. S3528 and S3529 in Parallel Notch Configuration—Narrow Bandwidth

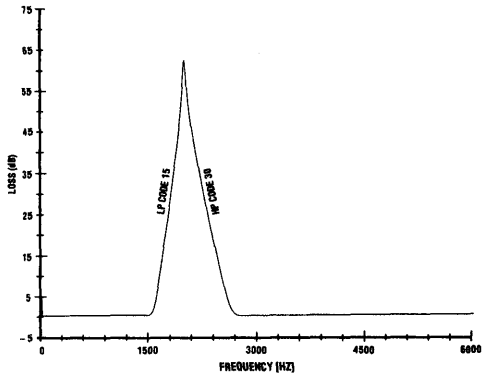
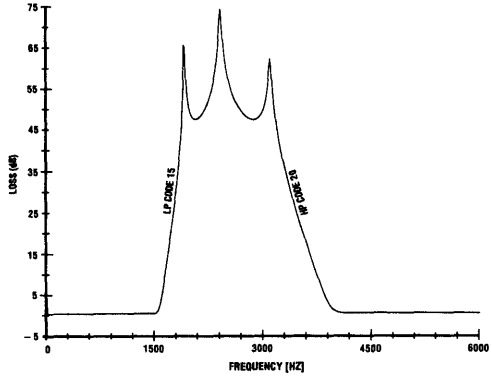


Figure 9. S3528 and S3529 in Parallel Notch Configuration—Wide Bandwidth

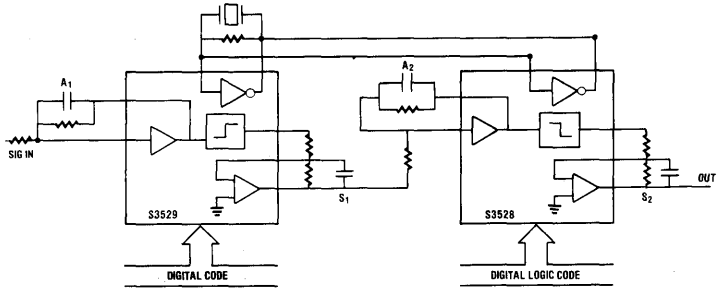


Applications Information

The S3529 (High Pass Filter) has a very sharp 50dB drop off at f_C. The Passband Ripple is less than 0.5dB. Note that unlike passive element filters, attenuation increases for sampled-data filters at the higher frequencies due to the sample and hold effect. ($f_{CLOCK} = 44xf_{CUTOFF}$).

The S3529 (High Pass Filter) and the S3528 (Low Pass Filter) can be used together to make either Band Pass or Band Reject filters. The control code selection determines the bandwidth of the resulting filter.

Figure 10. Bandpass Application: General Case Configuration



Note:

— Anti-aliasing and smoothing filters on both chips A1, A2, S1, S2

— Lowpass after highpass to remove higher harmonics, unless cosine input filter of lowpass needed to clean noisy input signal

— For wider band width two different oscillators can be used.

— If filter clock (f_{clock}) for lowpass is an integer multiple of the f_{clock} for highpass, then S1 and A2 may be removed without causing beat frequencies.

- For same digital logic code
  N = multiple of clock#1 to clock#2

$$f_{cL} = \frac{.9 f_{cu}}{N}$$

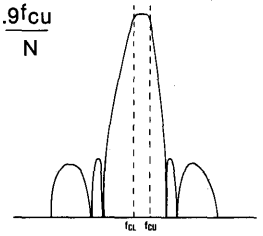


Figure 11. Notch Applications: General Case Configuration

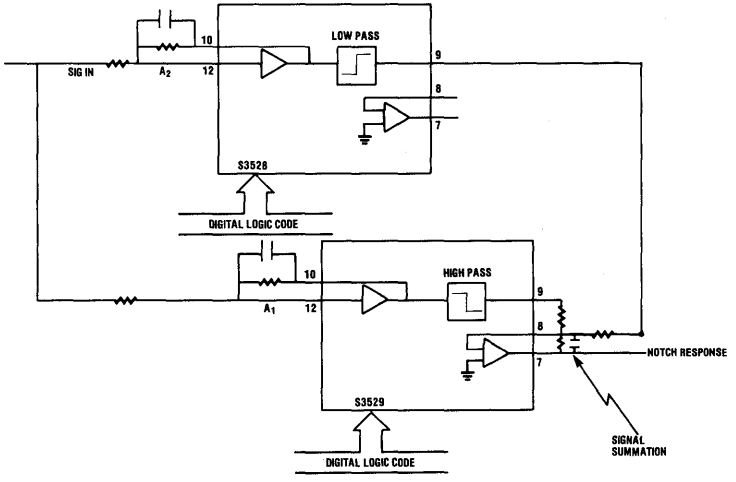


Figure 12. Sampling Theory

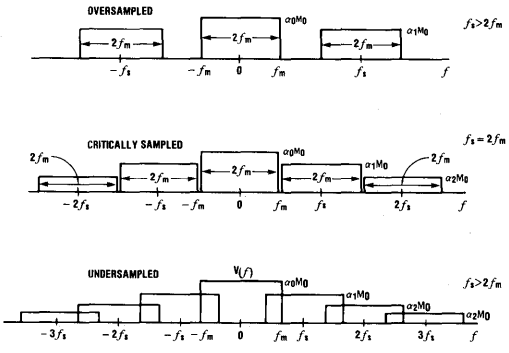
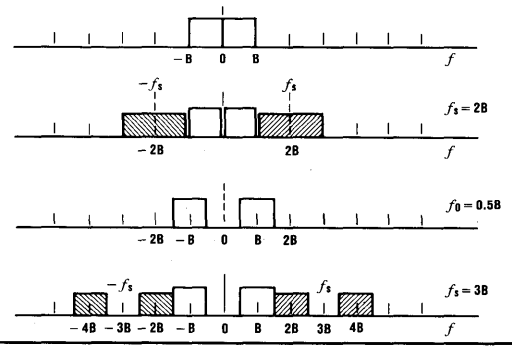
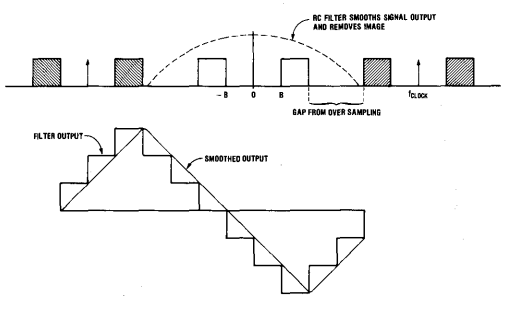


Figure 13. Avoiding Aliasing



Note that critical sampling avoids aliasing, but in the above example no real life filter can separate the message from the image. One must oversample in real life.

Figure 14. Implementation



Applications Information

Anti-Aliasing

fs = sampling frequency
fm = frequency bandwidth of message

In planning an application the fundamentals of sampling devices must be considered.

☐ Make certain the harmonic image does not fold into the desired pass band. i.e, Oversample.

☐ Bandlimit the input so that the input frequencies, noise, and tails will not come too close to the clock and be folded back into the pass band.

☐ Bandlimit the output so that the image is sufficiently attenuated and the switched capacitor output is smoothed. i.e., kill the higher order terms in the Fourier Series.

☐ For dynamic operation check for aliasing at each cutoff frequency.

A Subsidiary of Gould Inc.

S3530

BELL 103/V.21 SINGLE CHIP MODEM

COMMUNICATION PRODUCTS

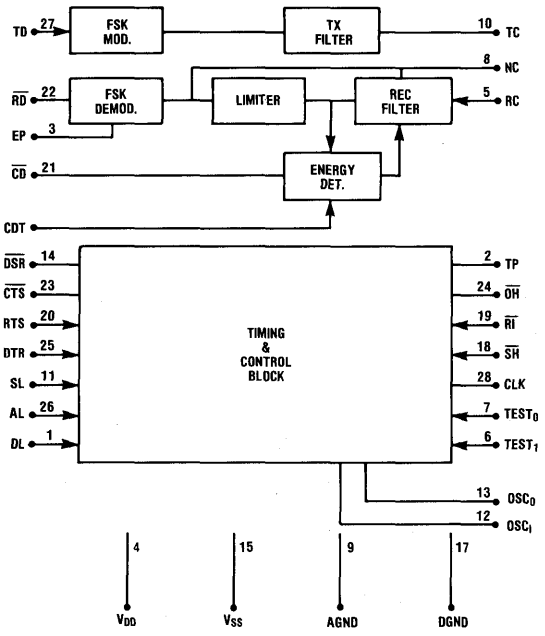
Features

- ☐ Single-Chip 300 bps, Full Duplex, Asynchronous FSK Modem
- ☐ Bell 103/113 & CCITT V.21 Operation (Selectable)
- ☐ Auto Answer/Originate Operating Modes
- ☐ Manual Mode
- ☐ No External Filtering Required
- ☐ Phase Continuous Transmit Carrier Frequency Switching
- ☐ RS-232 Control Interface
- ☐ Passthru Mode for Protocol Independence
- ☐ Low Cost 3.58MHz (TV Crystal) Time Base
- ☐ Digital & Analog Loopback Modes
- ☐ UART Clock Output (4.8KHz)
- ☐ V.25 Tone Generation

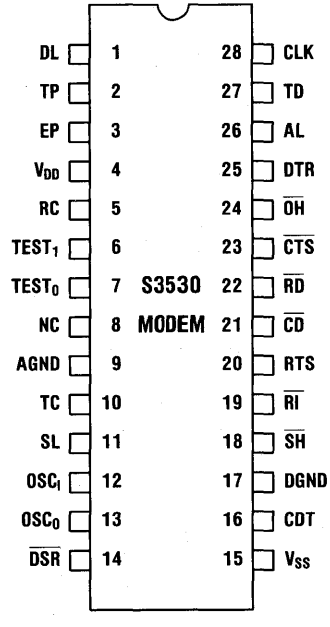
General Description

The S3530 is a Monolithic CMOS Single-Chip Full Duplex FSK Modem integrated circuit which may be operated in Bell 103/113 or CCITT V.21 applications. The S3530 features on-chip transmit and receive filtering; answer/originate mode selection; RS-232 control interface; digital and analog loopback test modes; and generation of both the 4.8KHz UART clock and V.25 Answer Tone. The S3530 is designed for use in stand-alone modem applications and in applications in which the modem function is designed directly into the DTE.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage (V_{DD}-V_{SS}) ..... +12.0V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Input Voltage, All Pins ..... V_{SS} − 0.3V≤V_{IN}≤V_{DD} + 0.3V

D.C. Electrical Operating Characteristics: T_A = 0°C to +70°C; (V_{DD}-V_{SS}) = 10V; (±5.0V)

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Positive Supply Voltage (ref. to DGND and AGND, both at 0 Volts)	+4.75	+5.0	+5.25	VDC
V_{SS}	Negative Supply Voltage (ref. to DGND, AGND)	−4.75	−5.0	−5.25	VDC
P_D	Power Dissipation, Operating (@ ±5V)		110		mW
R_{IN}	Input Resistance	8			MΩ
C_{IN}	Input Capacitance			15	pF

Analog Signal Parameters: T_A = 0°C to 70°C; ±5 VDC. f_{OSC} = 3.58MHz

Symbol	Parameter/Conditions	Min.	Typ	Max.	Unit
f_{OSC}	Oscillator Frequency		3.579545 ±0.02%		MHz
f_t	Transmit Frequency Tolerance		±1.2		Hz
t_D	Transmit 2nd Harmonic Attenuation with respect to Carrier Level		50		dB
T_{OUT}	Transmit Output Level into 10KΩ min., 25pF max.		−9		dBm
	Carrier Input Range (CDT open)	−48		0	dBm
DNR	Dynamic Range (CDT open)		48		dB
	Bit Jitter (Input = −30 dBm) Bit Bias Bias Distortion		100 1 3		μSec % %

Signal Input and Output Compatibility Table

Pin Name	No.	Input	Output	Voltage Level Low	Voltage Level High	Logic Family	IOL Milliamps
$\overline{SH}$	18	X		−3	+3	CMOS	
$\overline{RI}$	19	X		−3	+3	CMOS	
$TEST_0$	7	X		−3	+3	CMOS	
$TEST_1$	6	X		−3	+3	CMOS	
$\overline{OH}$	24		X	+0.4	+2.4	LSTTL	0.4
CLK	28		X	+0.4	+2.4	LSTTL	0.4
$\overline{CD}$	21		X	+0.4	+2.4	LSTTL	0.4
$\overline{RD}$	22		X	+0.4	+2.4	TTL	1.6
$\overline{CTS}$	23		X	+0.4	+2.4	TTL	1.6
$\overline{DSR}$	14		X	+0.4	+2.4	TTL	1.6
RTS	20	X		+0.8	+2.0	TTL	
TD	27	X		+0.8	+2.0	TTL	
DTR	25	X		+0.8	+2.0	TTL	
AL	26	X		+0.8	+2.0	TTL	
DL	1	X		+0.8	+2.0	TTL	
SL	11	X		+0.8	+2.0	TTL	

Pin/Function Descriptions

Pin #	Name	Function
25	DTR (Data Terminal Ready)	A high level on this input enables all the other inputs and outputs and must be present before the device will enter the data mode either manually or automatically. The device will enter an irreversible disconnect sequence if the input is turned off (low level) for more than 14 mSec during a data call. A pulse duration of less than 6 mSec will not be detected.
20	RTS (Request to Send)	A high level on this input with the DTR input in the on condition causes the device to enter the originate mode. $\overline{OH}$ will go low to seize the phone line. Auto dialing can be performed by turning the RTS input on and off to effect dial pulsing. This input must remain high for the duration of data transmission. (Auto answer will **not** function if RTS is high)
23	$\overline{CTS}$ (Clear to Send)	This output goes to a low level at the completion of the handshaking sequence and turns off when the modem disconnects. It is always turned off if the device is in the digital loopback mode. Data to be transmitted should not be applied at the TD input until this output turns on.
21	$\overline{CD}$ (Carrier Detect)	This output goes to a low level to indicate that the receive data carrier has been received at a level of at least −43dBm. It turns off if the received data carrier falls below the carrier detection threshold of −48dBm. During the off state, the Receive Data is clamped to the MARK state.
27	TD (Transmit Data)	Data bits to be transmitted are presented to this input serially by the data terminal. A high level is considered a binary '1' or MARK and a low level is considered a binary '0' or SPACE. The data terminal should hold this input in the MARK state when data is not being transmitted. During handshaking this input is ignored.
22	$\overline{RD}$ (Received Data)	The device presents data bits demodulated from the received data carrier at this output. This output is forced high if the DTR input or the carrier detect output is off.
14	$\overline{DSR}$ Data Set Ready	This output, when low, indicates to the data terminal that the modem is ready to transmit data.
19	$\overline{RI}$ (Ring Indicator)	This input when high permits auto answer capability. The data access arrangement should apply a low level to $\overline{RI}$ when a ringing signal is detected. The level should be low for at least 107msec. The input can remain low until reset by DTR or loss of carrier. Similarly, in manual mode, the answer mode is entered by applying a low level to this input, unless RTS is high.
26	AL (Analog Loopback)	This input allows the data terminal to make the telephone line busy (off hook) and implement the analog loopback mode. A high level on this input while DTR is high causes the device to make the $\overline{OH}$ output low and to enter the analog loopback mode. The receive filter center frequency is switched to correspond to the transmit filter center frequency and the transmit data carrier output is internally connected to the receive data carrier input, as well as being available at TC.
11	SL (Select)	A high level on this input selects the CCITT V.21 data transmission format. Applying a low level selects the Bell 103 data transmission format.
16	CDT (Carrier Detect Threshold)	Applying a variable voltage level between 0 and −5V at this pin allows control of the receiver carrier detection threshold. This will override the internally determined threshold. If CDT is set to a voltage between +1.5 and +2.0V the AGC will be disabled during the test modes of pins 6 & 7.
28	CLK (Clock)	A 4.8KHz LSTTL compatible square wave output is provided for supplying the 16X clock signal required by a UART for 300 bits/sec. data rate. This output facilitates the integration of the modem function in the data terminal.

Pin/Function Descriptions (Continued)

Pin #	Name	Function
24	$\overline{OH}$ (Off-Hook)	This output goes to a low level when either the $\overline{SH}$ or the RTS input is on in the originate mode, and when a valid ring signal is detected on the $\overline{RI}$ input in the answer mode. This output is off if DTR is off or if the disconnect sequence has been completed.
10	TC (Transmit Carrier)	This analog output is the modulated transmit data carrier. Its frequency depends upon whether the modem is in the answer or originate mode and if a mark or space condition is being sent (Table 1). Typically, the output level is at −9dBm.
7 6	Test 0 Test 1	These are test inputs and must be tied to V_{SS} for normal applications. See table under Passthru Mode.
5	RC (Receive Carrier)	This analog input is the data carrier received by the data access arrangement from the line. The modem demodulates this signal to generate the receive data bits.
17	DGND (Digital Ground)	Digital ground (0 Volts).
9	AGND (Analog Ground)	Analog ground (0 Volts).
8	NC	No connect.
4,15	V_{DD}, V_{SS}	Positive and negative power pins, respectively (±5V).
18	$\overline{SH}$ (Switch Hook)	This input is used to manually place the device in the originate mode. The device will make the $\overline{OH}$ output low and start the originate sequence if $\overline{SH}$ input is low and DTR is on. This can be a level or a momentary low-going pulse input (min. 54 mS). A pulse duration of less than 27 mS will not be detected. $\overline{RI}$ should be high if $\overline{SH}$ is to be exercised. Once RI has been activated then RTS has no effect.
13,12	OSC_O, OSC_I	These are terminals for connecting an external 3.579545MHz TV crystal. All internal clock signals are derived from this time base. An external clock signal may instead be applied at the OSC_I input. Feedback resistor and capacitors are integrated on the chip but additional 20pF caps to V_{SS} from each pin are required.
1	DL (Digital Loopback)	A high level on this input causes the device to enter the digital loopback mode. In this mode, the received data from the remote end is internally looped back to TD and $\overline{DSR}$ is forced high to signal to the DTE that the modem is not ready for transmission. The received data is not available on $\overline{RD}$ during the DL mode.
2	TP (Test Point)	Test Pin. Must be connected to either V_{SS} or V_{DD} for normal operations.
3	EP (Eye Pattern)	Output (analog) of the demodulator prior to slicing. Do not load.

Table 1. 103/V.21 Mark and Space Frequencies

Mode	Transmit Frequency (Hz)		Receive Frequency (Hz)	
	Mark	Space	Mark	Space
Bell 103 Originate	1270	1070	2225	2025
Bell 103 Answer	2225	2025	1270	1070
CCITT V.21 Originate	980	1180	1650	1850
CCITT V.21 Answer	1650	1850	980	1180
CCITT V.25 Answer Tone	2100			

Operation of S3530 Modem Chip

A. Bell 103/113 Mode

In the answer mode the S3530 stands idle waiting for an incoming call. As long as DTR is true, when a low from the ring detector is presented to $\overline{RI}$ the S3530 sets $\overline{OH}$ and $\overline{DSR}$ low which enables the hookswitch relay, connecting the modem to the phone line in the answer mode. The S3530 waits 2.1 seconds, and then sends carrier at 2225 Hz (mark) to the originate modem. When the originate modem returns with 1270 Hz (mark) the S3530 carrier detect circuit turns on within 106 msec and sets $\overline{CD}$ and $\overline{CTS}$ both low indicating the handshaking sequence is completed. Data can be be sent and received.

Originate Mode

In the originate mode a call is initiated, if DTR is high, by applying a high to the RTS input in auto mode or a negative pulse or low to $\overline{SH}$ in manual mode. This will cause $\overline{OH}$ to go low pulling in the hookswitch relay to connect the telephone line, and putting the S3530 in the originate mode. After a suitable time, or when dial tone is detected, RTS can be pulsed off to provide dial pulses*. The $\overline{OH}$ will go on and off, pulsing the line with the desired digits. When the answering modem comes on line it will wait 2.1 seconds ("billing delay") and then send the 2225 Hz answer tone. 106 milliseconds later the $\overline{CD}$ pin will go low indicating received carrier. 190 msec later the S3530 will respond with 640 msec of 1270 Hz. At the end of that time $\overline{CTS}$ (Clear-to-Send) will go low indicating to the terminal side that the communications link has been established.

Abort Mode

There is an automatic abort feature in the S3530 to avoid tying up a system should there be difficulty in establishing the link. If no carrier is detected within 14 seconds after the device has been put into the answer or originate mode it will abort the call by turning off $\overline{OH}$ and disconnecting the telephone line. $\overline{DSR}$ will also go off (high). This abort time can be extended by pulsing RTS low for about 1msec before the 14 seconds have elapsed. This will reset the abort timer. If it does time out DTR will need to be pulsed off to reset the S3530.

Shutdown Mode

Should the received carrier fall below – 48 dBm during data exchange for more than 213 msec the S3530 will terminate the call and go on-hook, disconnecting the telephone line.

Manual Operation

The S3530 can be operated manually as well as automatically. To put it in the Answer Mode apply a negative pulse (– 5V) on $\overline{RI}$ of greater than 107msec. If $\overline{RI}$ is tied low then the device will go into the Answer Mode whenever DTR is enabled.

Similarly, to put it in the Originate Mode, $\overline{SH}$ can be pulled low for more than 54msec. By tying $\overline{SH}$ low, the S3530 will go into the Originate Mode whenever DTR is enabled.

Passthru Mode

Through the "Test 0" and "Test 1" lines the S3530 can be put into the Passthru Mode. In this mode the protocol handshake is disabled, i.e., the transmit and receive functions are enabled but become independent of timing and control. $\overline{CD}$ works as usual. The Answer or Originate modes are selected in the same manner with $\overline{SH}$ or $\overline{RI}$.

TEST 0 PIN 7	TEST1 PIN 6	S3530 STATUS	1 = + 5V (V_{DD}) 0 = – 5V (V_{SS})
0	0	NORMAL	
1	0	PASSTHRU	

B. V.21 Mode

The S3530 will perform the same operations described above in the CCITT V.21 mode if the SL pin is tied high. The basic principle is the same but the frequencies and the timings are switched to conform to V.21 specifications. See the timing charts and Table 1 for additional details. When in V.21 mode the V.25 answer tone of 2100Hz will be generated upon answering.

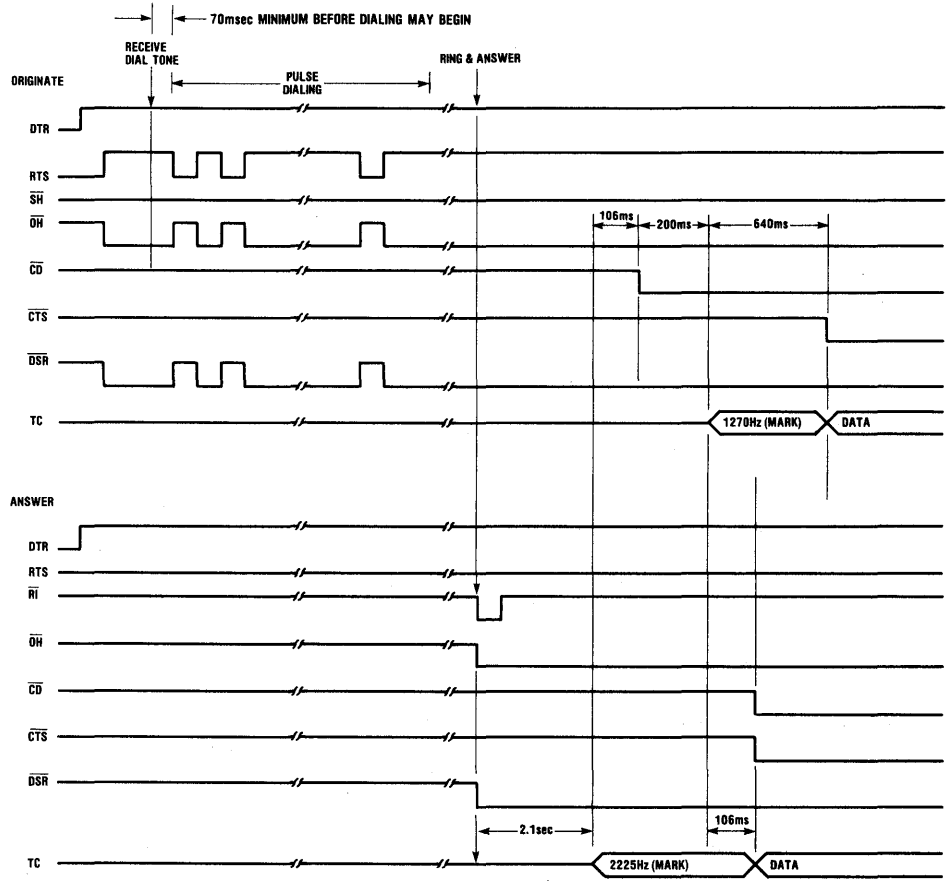
Diagnostic Modes

The S3530 has two diagnostic modes available to the operator. By putting the AL pin high while DTR is high, the device enters the Analog Loopback Mode. $\overline{OH}$ goes low to busy out the phone line. The receive filter center frequency moves to the transmit center frequency and the TC signal is internally connected to the RC input. The transmit signal also remains available on the TC pin. Thus any digital data input at TD is coded and sent out via TC, and at the same time back through the analog input, decoded, and out on the $\overline{RD}$ pin.

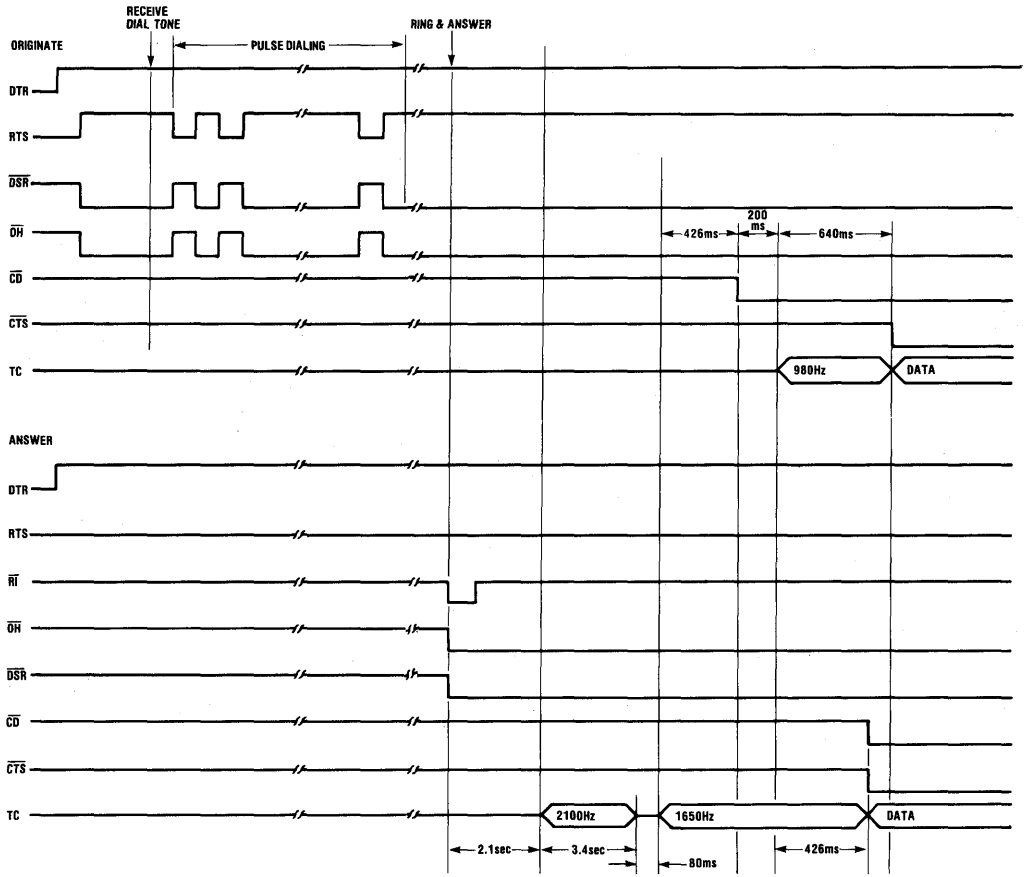
By putting the DL pin high the S3530 enters the Digital Loopback mode. In this mode any data received from the remote end of the telephone line is retransmitted back to its source and $\overline{DSR}$ is forced high. The digital or decoded data is not available at the $\overline{RD}$ output in this mode.

*(Note that $\overline{OH}$ only follows RTS. The proper timing for dialing must come from the terminal on the RTS line.)

S3530 Modem Timing Chart for 103 Operating Mode



S3530 Modem Timing Chart for V.21 Operating Mode



Application Circuits

Two applications circuits are illustrated. The first circuit is for a stand-alone RS-232 interface modem to be used as a peripheral accessory to a terminal or computer. Plugging into an RS-232 serial port on one side and into a standard modular telephone jack on the other side it is a stand-alone direct connect modem for operation at rates up to 300 bps.

The second circuit is an add-on modem for building into a computer and connecting to the internal parallel buss structure. The ACIA or UART does the parallel-to-serial and serial-to-parallel conversion required. The edge connector is numbered for an Apple II application but the same interface applies to most μP systems.

Both circuits are intended for direct connection to the telephone line. This requires meeting FCC Part 68 requirements for network protection as well as protection of the modem. No suppression components are illustrated on these examples as the design of the interface will vary depending on the needs of the designer. After a design is completed it must be subjected to Part 68 certification before sale to the public.

If one wants to avoid the protection/certification details then a certified DAA (Data Access Arrangement) such as the Cermetek CH1810 can be used instead. The DAA is designed to handle the telephone line interface including the 4 wire to 2 wire function and is already registered with the FCC.

Whether using a DAA or not, the S3530 requires very few external components.

Hybrid Functions

In the stand-alone circuit the hybrid 4 wire to 2 wire converter utilizing the dual op amp was configured to provide 1:1 conversion in each direction. A – 9dBm voltage level from the Transmit Carrier pin on the S3530 is amplified by the op amp to compensate for the losses in the 300Ω matching resistor and the coupling transformer. The transmit carrier is delivered to the line at – 9dBm.

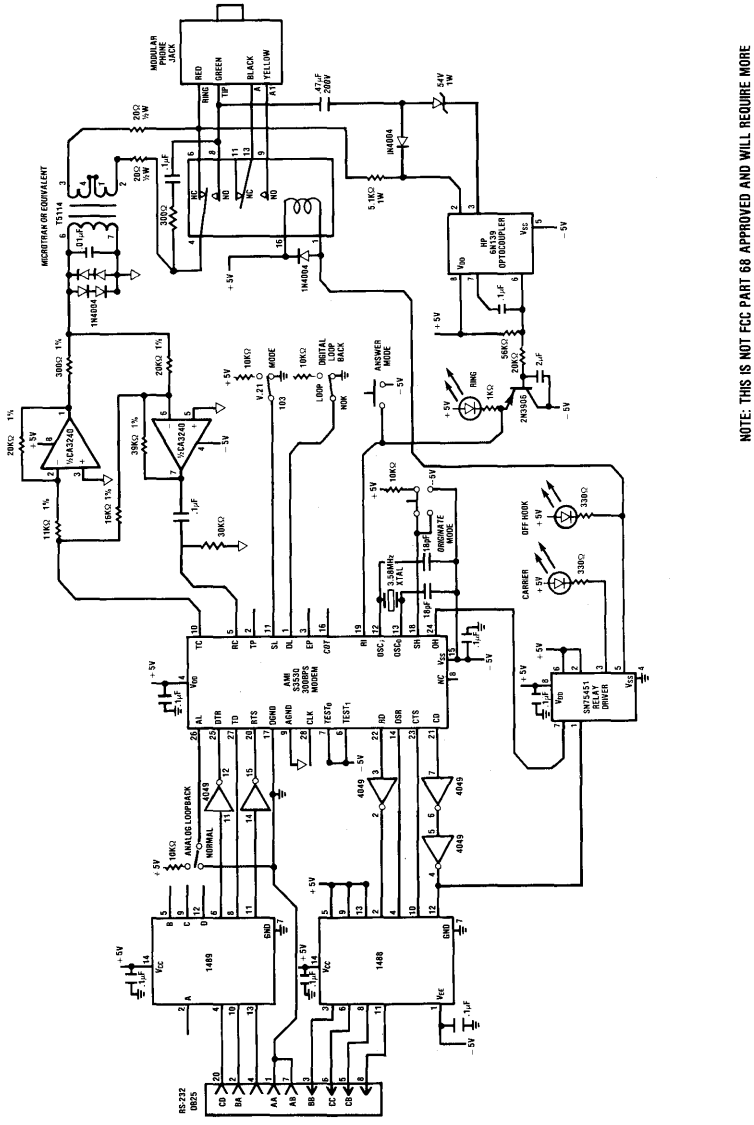
In the receive direction the loss in the coupling transformer is compensated for by the other half of the op amp. If there is a – 20dBm signal across Tip and Ring then a – 20dBm signal is delivered to the Receive Carrier pin on the S3530.

The 300Ω resistor is to provide the proper termination so that Tip and Ring look like a 600Ω AC impedance to the line. The 16KΩ resistor from the Transmit Carrier pin to the inverting input of the receive op amp is to provide sidetone suppression. The transmit carrier is provided through the 16KΩ resistor 180° out of phase from the transmit carrier presented to the line. Thus, the transmit carrier is cancelled out and not presented to the Receive Carrier pin on the S3530. Under ideal conditions 20dB or more of cancellation might be achieved, but because telephone lines vary considerably, a cancellation of around 10dB is a more realistic number. The 20Ω resistors in series with Tip and Ring increase the DC impedance of the modem to the line. This is because the transformer is very close to the 100Ω minimum DC impedance specification in the off-hook condition.

NOTE once again, that only minimal transient protection is illustrated in these examples. This must be added to meet the needs of the application and the FCC Part 68 requirements.

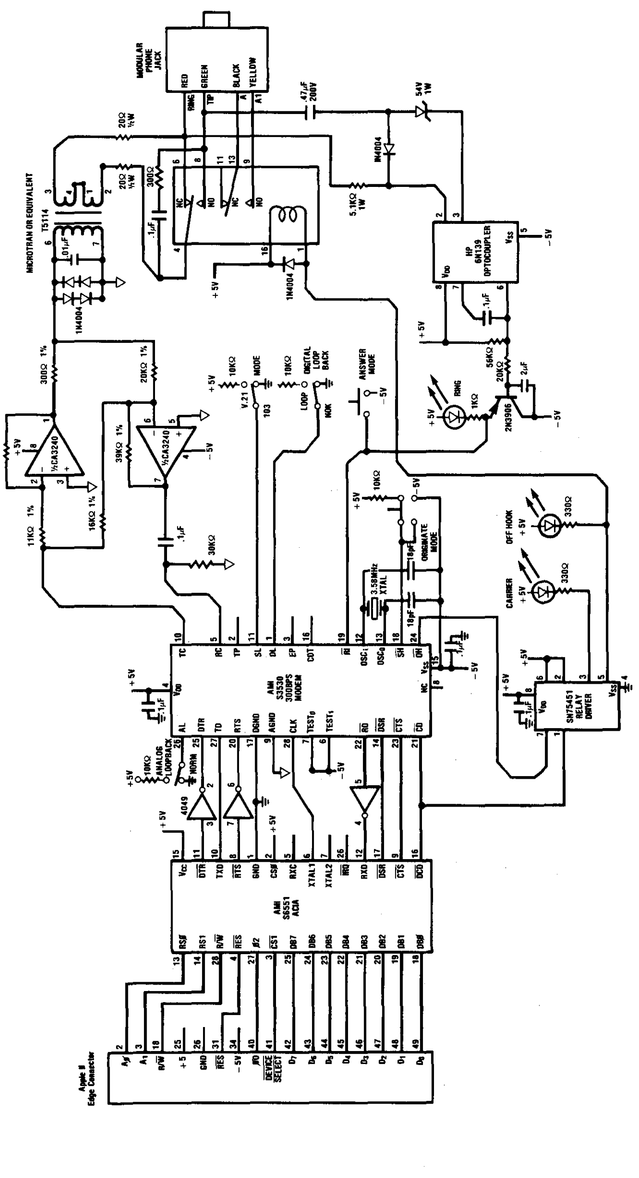
Also, the transformer listed is rated to 75mA loop current. To go to the maximum loop current the Microtran number would be T5115 for 120mA loop current capability. The DC resistance may be slightly different and the various components will need to be adjusted to retain the necessary levels of AC and DC specifications.

Suggested Serial Interface Application Schematic for S3530



NOTE: THIS IS NOT FCC PART 68 APPROVED AND WILL REQUIRE MORE TRANSIENT PROTECTION AND AN FCC CERTIFICATION TEST. THIS SCHEMATIC IS INTENDED AS A SUGGESTED STARTING POINT ONLY, AND SHOULD BE ADOPTED TO FIT EACH PARTICULAR APPLICATION.

Suggested Parallel Interface Application Schematic for S3530 and Apple II



NOTE: THIS IS NOT FCC PART 68 APPROVED AND WILL REQUIRE MORE TRANSIENT PROTECTION AND AN FCC CERTIFICATION TEST. THIS SCHEMATIC IS INTENDED AS A SUGGESTED STARTING POINT ONLY, AND SHOULD BE ADOPTED TO FIT EACH PARTICULAR APPLICATION.

AMI

A Subsidiary
of Gould Inc.

Consumer Products

Contact factory for complete data sheets

Consumer Products Selection Guide

SPEECH PRODUCTS

Part No.	Description	Process	Power Supplies	Packages
S3620	Speech Synthesizer	CMOS	+ 5V	22 Pin
S36128	131,072 Bit Female Speech ROM	NMOS	+ 5V	28 Pin
EVK3620	Speech Synthesis Evaluation Board			

DRIVERS

Part No.	Description	Process	Power Supply	Outputs	Packages
S4520	30-Volt Dichroic LCD Driver	CMOS	+ 3V to + 16V/ − 30V to − 5V	30/32/38	40 Pin
S4521	32 Bit Driver	CMOS	+ 3V to + 13V	32	40 Pin
S4535	32 Bit, High Voltage, Driver	CMOS	+ 5V/ + 20 - + 60	32	40 Pin
S4534	10 Bit, High Voltage, High Current Driver	CMOS	+ 5V − 12V/ + 20 to + 60	10	18 Pin
S2809	Universal Driver	PMOS	+ 8V to + 22V	32	40 Pin

REMOTE CONTROL CIRCUITS

Part No.	Description	Process	Power Supply	Commands	Packages
S2600	Remote Control Encoder	CMOS	+ 7V to 10V	31	16 Pin
S2601	Remote Control Decoder	PMOS	+ 10V to 18V	31	22 Pin
S2604	Remote Control Encoder	CMOS	+ 9V	18	16 Pin
S2605	Remote Control Decoder	CMOS	+ 9V	18	22 Pin
S2742	Remote Control Decoder	PMOS	+ 15V	512	18 Pin
S2743	Remote Control Encoder	PMOS	+ 9V	512	16 Pin
S2747	Remote Control Encoder	CMOS	+ 9V	512	16 Pin
S2748	Remote Control Decoder	CMOS	+ 12V	512	16 Pin

ORGAN CIRCUITS

Part No.	Description	Process	Packages
S10110	Analog Shift Register	PMOS	8 Pin
S10430	Divider-Keyer	PMOS	40 Pin
S2688	Noise Generator	PMOS	8 Pin
S50240	Top Octave Synthesizer	PMOS	16 Pin
S50241	Top Octave Synthesizer	PMOS	16 Pin
S50242	Top Octave Synthesizer	PMOS	16 Pin

CLOCK CIRCUITS

Part No.	Description	Process	Power Supply	Digits	Packages
S4003	Fluorescent Automotive Digital Clock (12 Hour + Date + Rally Timer)	PMOS	+ 12V	4	40 Pin
S2709A	Vacuum Fluorescent Digital Clock	PMOS	+ 12V	4	22 Pin

A/D CONVERTER AND DIGITAL SCALE CIRCUIT

Part No.	Description	Process	Power Supply	Digits	Packages
S4036	General Purpose A/D Converter and Digital Scale Circuit	CMOS	+ 9V	4	24 Pin

AMI®

A Subsidiary of Gould Inc.

S3620

LPC-10 SPEECH SYNTHESIZER

CONSUMER PRODUCTS

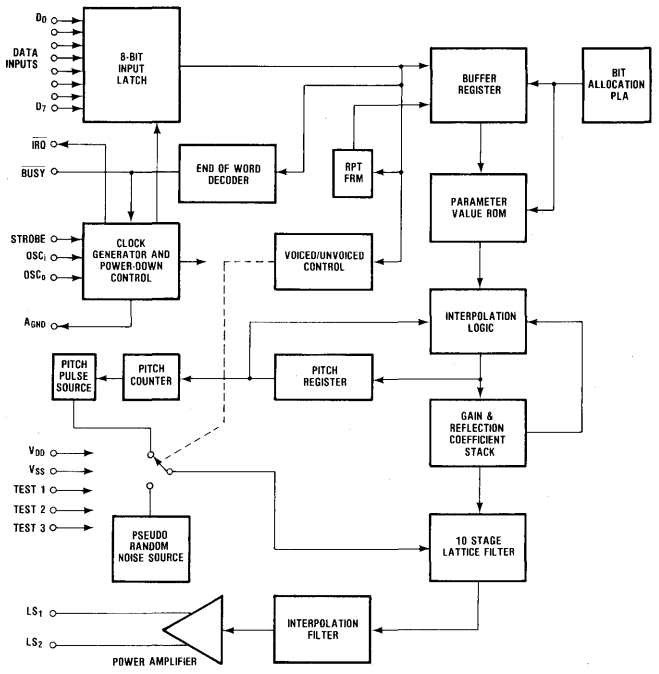
Features

- ☐ Simple Microprocessor Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ 5-8 Volts Single Power Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 20mW Audio Output
- ☐ Low Data Rate

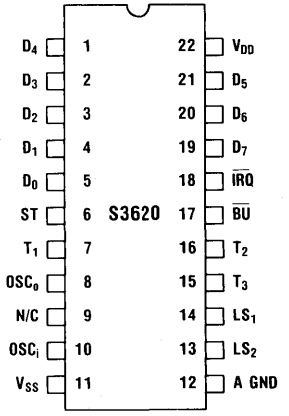
General Description

The S3620 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an external memory. The digital interface circuitry is fully microprocessor compatible and allows the processor to load the data with or without a DMA controller. The loading takes place on a handshake basis, and in the absence of a response from the processor the synthesizer automatically shuts down and goes into the powerdown mode. A busy signal allows the processor to sense the status of the synthesizer. The input data

Block Diagram



Pin Configuration



N/C = NO CONNECTION

rate is 2.0K bits/sec. max., but typically the average data rate will be reduced to about 1.4K bits/sec. by means of the data rate reduction techniques used internally.

The synthesizer is realized using analog switched-capacitor filter technology and operates at 8K samples/sec. An output interpolating filter and bridge power amplifier give 20mW output power at 5 volts supply and allow the device to be connected directly to a 100Ω loudspeaker.

The S3620 also features an on-chip oscillator, requiring only a 640kHz ceramic resonator and a 120pF capacitor for normal operation.

AMI is able to provide a speech analysis service to generate the LPC parameters from customers' word lists.

Absolute Maximum Ratings*

Supply Voltage	11 Volts DC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Voltage at any Pin	V_{SS} −0.3 to V_{DD} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications: (V_{DD} = 5.0V ± 10%, V_{SS} = 0V, C_{AG} = 0.047μF, T_A = 0° to 70°C, unless otherwise specified)

D.C. Characteristics

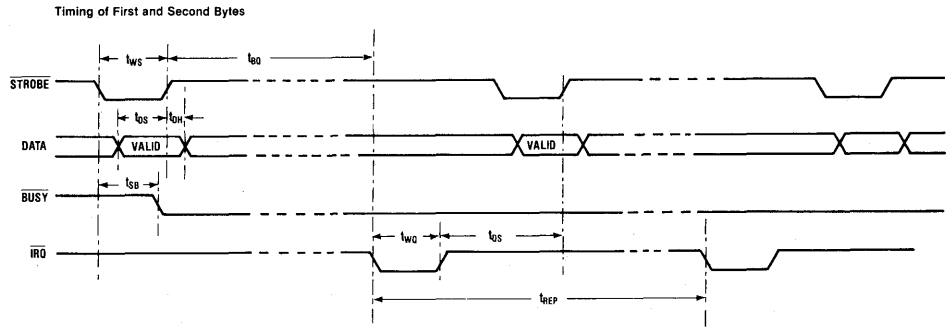
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.4		V_{DD}	V	
V_{IL}	Input Low Logic "0" Voltage	0		0.8	V	
I_{IN}	Input Leakage Current			10	μA	V_{IN} = 0 to V_{DD}
V_{OL}	Output Low Voltage ($\overline{BU}$, $\overline{IRQ}$)			0.4	V	I_{OL} = 1.6mA
V_{OS}	DC Offset Voltage, Audio Output		0.5 V_{DD}		V	R_{LOAD} = 100Ω
I_{DD}	Supply Current, Operating			35	mA	
I_{DDL}	Supply Current, Powerdown			4	mA	

AC Characteristics

P_O	Audio Output Power		20		mW	R_{LOAD} = 100Ω
t_{DS}	Data Set-up Time	100			nsec	See Figure 1
t_{DH}	Data Hold Time	10			nsec	See Figure 1
t_{WS}	Strobe Pulse Width	3.2		100	μsec	See Figure 1
t_{SB}	1st Strobe to Busy Delay		100	500	nsec	See Figure 1
t_{BQ}	1st Strobe to 1st IRQ Delay		19		msec	See Figure 1
t_{REP}	IRQ Repetition Rate		250		μsec	See Figure 1
t_{WQ}	IRQ Pulse Width	3		3.5	μsec	See Figure 1
t_{QS}	IRQ to Strobe Delay[See Note 1]			200	μsec	See Figure 1
F_{OSC}	Oscillator Resonator Frequency	−1%	640	+1%	KHz	See Figure 1
R_{LOAD}	Audio Output Load Impedance		100		Ω	
C_{INOSC}	Input Capacitance, Oscillator		100		pF	
C_{IN}	Input Capacitance, Digital Interface		7		pF	

NOTE 1: Failure to respond to an IRQ with a new strobe within the specified period results in the chip going into the power down mode.

Figure 1. Timing Requirements



Pin Function/Description

D_0 through D_7	**Data Inputs.** The speech data (in quantized form is loaded on these line in 8-bit bytes.)
ST	**Strobe Input.** A rising edge on this input strobes in the data bytes. Enunciation will commence after the first frame of data has been loaded. If no strobe is received by the chip in response to an IRQ output then enunciation stops immediately and the chip goes into power down mode.
$\overline{BU}$	**Busy Output.** This open drain output signals that enunciation is in progress by going low.
$\overline{IRQ}$	**Interrupt Request Output.** This open drain output signals that the chip is ready to receive the next byte of data. Failure to respond within the prescribed time results in the chip going into the power-down mode.
LS1 and 2	**Loudspeaker Outputs.** These pins are used to connect the chip to the loudspeaker. They are D.C. coupled and have an offset of half the supply voltage. The audio output is balanced on the two outputs.
OSC_i, OSC_o	**Oscillator Input and Output.** A 640KHz ceramic resonator (MuRata CSB640A or equivalent) should be connected between these pins for normal operation, or an external 640KHz signal may be fed into OSC_i. When a resonator is used, a 120pF capacitor should be connected between OSC_i input and ground.
T_1, T_2, T_3	**Test Inputs and Outputs.** These inputs should be left unconnected for normal operation.
V_{SS}	Most negative supply input. Normally connected to 0V.
V_{DD}	Most positive supply input.
A_{GND}	**Analog Ground.** An internally generated level approximately half way between V_{SS} and V_{DD}. A 0.047μF decoupling capacitor C_{AG} should be connected from this pin to V_{SS}. Do not connect this pin to a voltage supply.

Circuit Description

The main components of the S3620 LPC-10 Speech Synthesizer are shown in the block diagram.

Input Latch—This 8-bit latch stores the input data after the strobe pulse and loads it into the Coefficient Address Registers.

End of Word Decoder—This circuit detects the special code indicating that the last byte loaded in the Input Latch denotes the end of the speech word data and initiates the power down routine after the previous frame has been enunciated.

Buffer Registers—The data from the Speech Data ROM is assembled into frames and then decimated into the 12 parameters required for LPC-10 synthesis: pitch, gain and the 10 lattice filter coefficients. The parameters are stored in an encoded format and the decoding is done in the parameter value ROM. The coefficient address registers are used to store the assembled frame data and address this ROM.

Bit Allocation PLA—A programmable logic array is used to control the allocation of bits in the Buffer Register to the 12 parameters. The allocation and permissible variations are shown in Figure 2.

Parameter Value ROM—This ROM is used as a look-up table to decode the stored parameters into the LPC coefficients.

Interpolation Logic—The coefficients for each frame of speech, normally 20msec. are interpolated four times per frame to generate smoother and more natural sounding speech. Hence, the interpolation period is one quarter of a frame period, normally 5msec. After interpolation, the coefficients are used to drive the pitch-pulse source, the voiced/unvoiced switch, the lattice filter and the gain control. Interpolation is inhibited when a change from voiced to unvoiced speech, or vice versa, is made.

Pitch Register and Counter—This register stores the pitch parameter used to control the pitch counter.

Pitch-pulse Source—This is the signal source for voiced speech (vowel sounds). It is realized in switched-capacitor technology and generates symmetrical bipolar pulses at the rate specified by the pitch parameter and controlled by the pitch counter.

Pseudo-random Noise Source—This is the signal source for unvoiced speech (fricatives and sibilants) and consists of a 15-bit linear code generator giving a periodicity of 32767 sampling periods (4.096sec.). The output of this generator is scaled to a lower value and used as a random sign, constant amplitude signal.

Voiced/Unvoiced Speech Selector Switch—This switch determines whether the voiced or unvoiced signal source is used to drive the filter during a given frame.

LPC-10 Parameter Stack—This stack of 10 filter coefficients is used to control the lattice filter. The coefficients have an accuracy of 8-bits plus sign.

10 Stage Lattice Filter—The filter which simulates the effect of the vocal tract on the sound source (glottis) in the human speaker is realized here as a switched-capacitor (analog sampled data) 10 stage lattice filter. The filter parameters are determined dynamically by the time varying coefficients in the Parameter Stack and the filter operates at a sampling frequency of 8KHz (clock frequency/80).

Gain Controller—This controls the input signal level to the lattice filter to vary the sound level, and is an integral part of the lattice filter.

Interpolation Filter—The output signal from the lattice filter is sampled at 8KHz, and consequently its spectrum is rich in aliasing (foldover) distortion components above 4KHz (See Figure 3). The signal is cleaned up by passing it through a 4KHz low pass filter sampled at 160KHz. The spectrum of the output signal contains no aliasing distortion components below 156KHz, making the output suitable for feeding directly into a loudspeaker after amplification. This filter is also realized using switched-capacitor filter technology.

Power Amplifier—The amplifier brings up the level of the signal to give an output level of 20mW RMS into a 100Ω load. The output is a balanced bridge configuration with anti-phase signals on the 2 output pins.

Clock Generators and Power-down Control—This block contains the oscillator and timing circuits and also generates the analog ground reference voltage.

Speech Data Compression

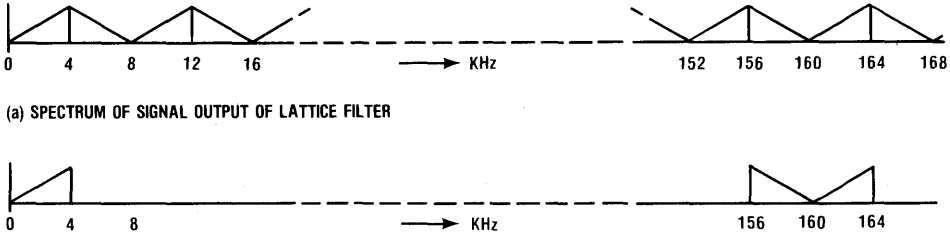
The speech data rate of the synthesizer is reduced to less than 2000 bits/sec for storage by means of a non-linear quantization technique. Each of the 12 coefficients is constrained to have a fixed set of values in an optimized manner. The actual values are dependent on the speech data and generated automatically in the analysis process. The parameters used to specify the coefficients are stored in the speech data ROM and

Figure 2. Packed Quantized Data Formats

	BYTE 5								BYTE 4								BYTE 3								BYTE 2								BYTE 1							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
VOICED	← PITCH →								← K10,K9,K8,K7,K6,K5 →								← K4,K3, K2, K1 →								← K4,K3, K2, K1 →										V/UV	REPT	← GAIN →				
UNVOICED	← NOT USED →																← K4,K3, K2, K1 →								← K4,K3, K2, K1 →										V/UV	REPT	← GAIN →				
REPEAT	← NOT USED →																																← PITCH →				GAIN			REPT*
END OF WORD	← NOT USED →																																0	0	0	0	0	0	0	0

*NOTE: 0 = SINGLE (OR LAST) REPEAT. 1 = MULTIPLE REPEAT.

Figure 3.



(a) SPECTRUM OF SIGNAL OUTPUT OF LATTICE FILTER

(b) SPECTRUM OF SIGNAL AT OUTPUT OF INTERPOLATION FILTER.
NOTE: IN BOTH CASES A SIN x/x CHARACTERISTIC MODULATES THE SPECTRA. THIS IS OMITTED FOR SIMPLICITY.

used to address the coefficient look-up table ROM. The packing formats for the speech data are shown in Figure 2.

The speech data rate is further reduced by two other techniques shown in Figure 2. A substantial reduction is achieved by reducing the order of the lattice filter (the LPC order) to 4 during periods of unvoiced speech. This allows a 40% data reduction during these periods, which themselves typically account for 30-40% of speech (in the English language). A second reduction is obtained by detecting periods during which the filter parameters may be the same as those in the previous frame. Only the gain and pitch parameters are updated in such a frame, allowing an 80% data reduction.

Generation of Speech Data for the S3620

The speech data input to the S3620 is in a compressed format as explained in the previous section. AMI is able to provide a complete speech analysis service for this purpose and can supply the data programmed into EPROMs or mask programmed ROMs up to 128k bits. Customers who have LPC speech analysis facilities and wish to generate their own data should contact AMI for further details of the quantization technique used and the availability of software to accomplish this.

Interfacing

The S3620 is designed to be easily interfaced to an 8-bit microprocessor system such as the S6800 family. The timing requirements are shown in Figure 1. The first data byte should be present at the data input lines when the strobe line is taken to a logic 1 to begin enunciation and in response to each $\overline{IRQ}$. The busy output may be used to identify the $\overline{IRQ}$ source during polling in a multiple interrupt system. A typical system configuration is shown in Figure 4. The S3620 occupies a single address in the microprocessor's memory space and data is loaded by writing it into that address after reading it from memory. The Address decode function may be realized using a PIA. An alternative interface technique is to write the data directly into the S3620 while reading it from the memory. This can be accomplished by mapping the S3620 into the entire address space of the speech data portion of the memory, so that the strobe is generated each time a byte of data is read from the speech memory. This can save hardware, as well as microprocessor instructions, since the loading of each byte is now accomplished in a single Read cycle instead of a Read cycle followed by a Write cycle. An example of this interfacing is shown in Figure 5, where the speech data occupies the memory addresses 0000 to 7FFF.

Applications

Toys and Games
EDP
Instrumentation
Communications
Industrial Controls
Automotive
Appliances

Figure 4. Typical System Configuration

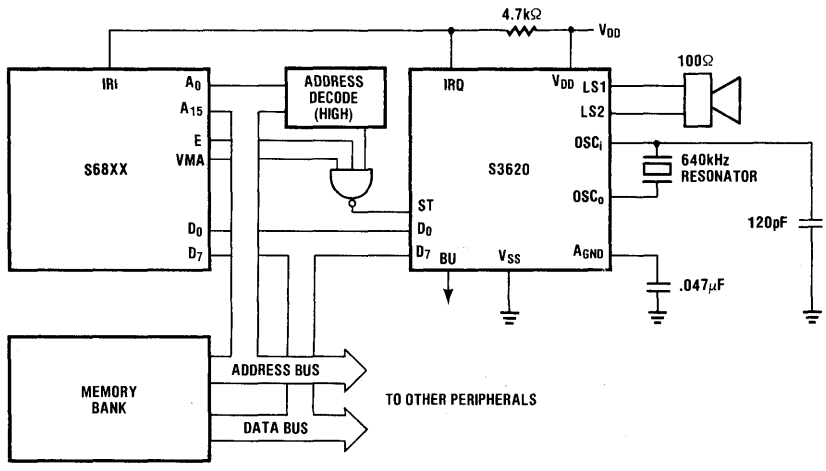
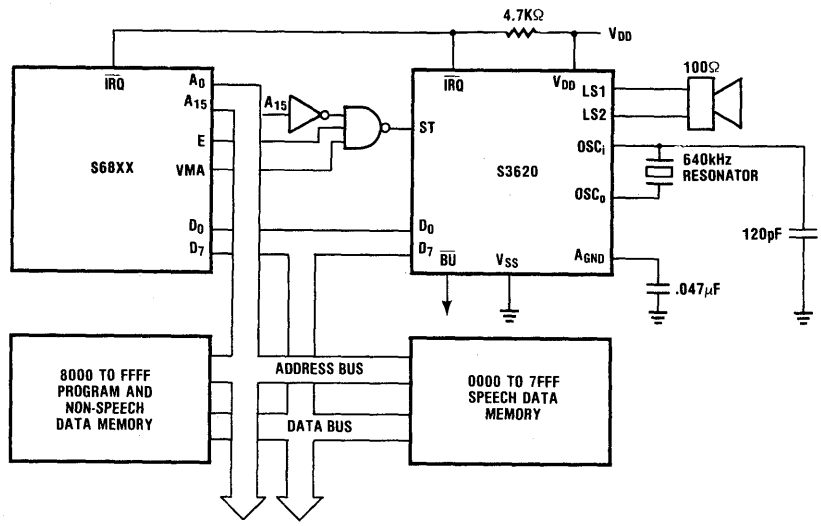


Figure 5.



CONSUMER PRODUCTS

A Subsidiary of Gould Inc.

S36128

131,072 BIT NMOS FEMALE SPEECH ROM

Features

- ☐ Approximately 100 Seconds of Stored Speech
- ☐ Vocabulary for Telecommunications, Industrial and Numeric Applications
- ☐ High Quality and Natural Sounding Female Voice
- ☐ Used with Gould AMI's S3620 LPC-10 Speech Synthesizer
- ☐ Ideal for Evaluation and Prototyping

General Description

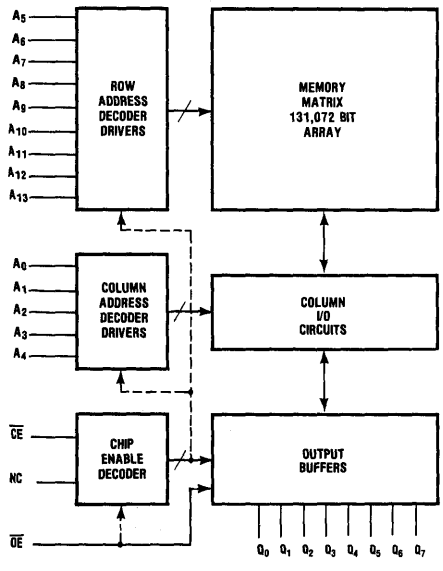
The S36128 is a 131,072 bit (organized as 16,384 words by 8-bits) static NMOS ROM mask programmed with speech data.

The S36128 speech ROM is fully TTL compatible on all inputs and outputs and has a single + 5V power supply.

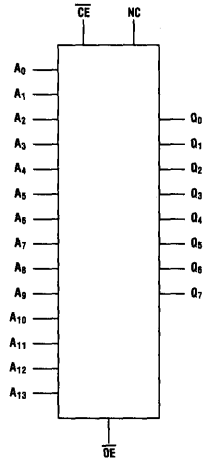
The speech data programmed in the S36128 contains words and phrases suitable for telecommunications and industrial applications, such as telephone answering, status announcements, timekeeping and emergency messages.

The S36128 is pin and electrically compatible with the Gould AMI S23128, a 131,072 bit static mask programmable NMOS ROM. The S23128 can be used by customers who want to program in their own vocabularies.

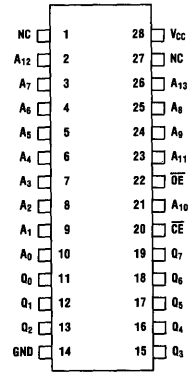
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A_0-A_{13}	Address Inputs
Q_0-Q_7	Data Outputs
OE/CE	Output Enable/Chip Enable
V_{CC};GND;NC	5V;Ground; No Connect

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin With Respect to Ground	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −400μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current	−10		10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current	−10		10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			40	mA	Chip Enabled
I_{SB}	Power Supply Current—Standby			20	mA	Chip Disabled

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

Operating Description

The S36128 is to be used with the AMI S3620 female parameter LPC (Linear Predictive Coding) speech synthesizer. Words are listed (see page 3) with their beginning address. Word data ends at the last byte before the following word. The speech data is packed into 8-bit bytes. These bytes are fed in parallel by the user's controller to the S3620 speech synthesizer which performs all of the unpacking and decoding of the formatted data. This unpacking is transparent to the user.

Rom Data Format

The ROM data begins with an address field which gives the starting address of each word in the vocabulary list in sequence. The addresses are given next to the appropriate word in the vocabulary listing also. The starting address upper half (SUH) is given first and the starting address lower half (SLH) follows. A section of data for internal use follows. The actual speech data begins immediately afterwards.

Address Field Format

LOCATION (DECIMAL)	CONTENTS b7	b6	b5	b4	b3	b2	b1	b0	WORD
0	0	0	SUH						1
1	SLH								
2	0	0	SUH						2
3	SLH								
⋮	⋮								⋮
2n−2	0	0	SUH						n
2n−1	SLH								
2n	0	0	EUH						END ADDRESS OF LAST WORD
2n+1	ELH								
2n+2	1	0	0	0	0	0	0	0	END OF ADDRESS FIELD
2n+3	0	0	0	0	0	0	0	0	

n = NUMBER OF WORDS STORED IN THE SPEECH ROM
SUH = STARTING ADDRESS:UPPER HALF
SLH = STARTING ADDRESS:LOWER HALF
EUH = END ADDRESS:UPPER HALF
ELH = END ADDRESS:LOWER HALF

Actual Data

Address	Data	
0000	01 1D 01 A4 02 10 02 89 03 04 03 88 03 D9 04 5F	
0010	04 AE 05 3D 05 A6 06 38 06 C3 07 72 08 2E 08 E4	Address
0020	09 95 0A 6D 0B 11 08 D9 0C 50 0C C3 0D 38 0D A6	Field
0030	0E 24 0E C1 0F 2F 0F C3 10 43 10 DD 11 74 11 F7	
0040	12 7E 13 06 13 8B 14 08 14 93 15 09 15 7C 16 63	
0050	16 EB 17 7B 17 E0 18 9D 18 DE 19 B0 1B 68 1B EE	
0060	1D 16 1D 9F 1E 68 1E E9 1F 5F 1F CF 20 47 20 D3	
0070	21 53 22 4A 22 FF 23 37 23 A9 24 36 24 CB 25 30	
0080	25 9D 26 0C 26 53 27 13 27 CF 28 7A 28 FE 29 77	
0090	29 C8 2A CE 2B C3 2C 48 2C A8 2D 38 2D C1 2E CB	
00A0	2F AB 2F F7 30 1F 31 3E 31 CF 32 5F 32 99 35 57	
00B0	36 3B 36 8A 37 A9 39 E7 3A A0 3B 3C 3B 5A 3B 69	
00C0	3B 75 3B 7B 3B 97 80 00 A0 D3 21 53 3B 3C 3B 5A	Internal
00D0	19 B0 1B 68 3B 3C 38 5A 22 4A 22 FF B7 A9 39 E7	Use Only
00E0	9B EE 1D 16 1F 5F 1F CF 04 AE 05 3D 16 EB 17 7B	
00F0	3B 75 3B 7B 2F F7 30 1F 03 04 03 88 3B 75 38 7B	
0100	A8 7A 28 FE AD C1 2E CB 3B 3C 3B 5A A0 47 20 D3	
0110	B0 1F 31 3E 3B 69 3B 75 AA CE 2B C3 00 06 70 6E	Speech
0120	26 F0 2B 93 A6 27 E0 28 8D BD 27 F0 26 8D C5 26	Data
0130	F0 05 DB B6 28 F0 03 E2 B6 69 F1 02 E8 A6 EA F1	Begins at
0140	02 7E 91 E8 D2 08 7B 9A ED C3 07 B8 91 AE A4 07	Address
0150	BC 9D 2E A5 16 73 95 EE 95 15 7C 95 2E 86 26 74	011D
0160	A4 AE 76 26 74 B4 2E 77 42 35 C5 AD 75 72 67 D1	

Word List of Telephone Application Vocabulary

Guide:

Items terminating with a single period (.) are intended for use at the end of a sentence or are a complete sentence themselves.

Items terminating with three periods (. . .) are intended for use at the beginning of a sentence.

All other words carry no restrictions.

"""""""Numbers"""""""

Word	Beginning Address	Word	Beginning Address
1. One	011D	16. Sixteen	08E4
2. Two	01A4	17. Seventeen	0995
3. Three	0210	18. Eighteen	0A6D
4. Four	0289	19. Nineteen	0B11
5. Five	0304	20. Twenty	0BD9
6. Six	0388	21. Thirty	0C50
7. Seven	03D9	22. Forty	0CC3
8. Eight	045F	23. Fifty	0D38
9. Nine	04AE	24. Sixty	0DA6
10. Ten	053D	25. Seventy	0E24
11. Eleven	05A6	26. Eighty	0EC1
12. Twelve	0638	27. Ninety	0F2F
13. Thirteen	06C3	28. Hundred	0FC3
14. Fourteen	0772	29. Thousand	1043
15. Fifteen	082E	30. Million	10DD

"""""""Days of The Week"""""""

31. Monday	1174	35. Friday	138B
32. Tuesday	11F7	36. Saturday	1408
33. Wednesday	127E	37. Sunday	1493
34. Thursday	1306		

"""""""Words and Phrases"""""""

38. After	1509
39. After the tone.	157C
40. Again	1663
41. A.M.	16EB
42. And	177B
43. Area code	17E0
44. At	189D
45. At this number.	18DE
46. This is an automatic message.	19B0
47. Before	1B68
48. Business hours are . . .	1BEE
49. Connected.	1D16
50. Emergency	1D9F
51. Error.	1E68
52. Fire . . .	1EE9
53. From	1F5F
54. Function	1FCF
55. Good-by.	2047
56. Hello.	20D3
57. Identification	2153
58. I'm sorry.	224A
59. Is	22FF
60. Later	2337
61. Medical . . .	23A9
62. Number	2436
63. Oh	24CB
64. Off.	2530
65. On. (opposite of off)	259D
66. On	260C

"""""""Words and Phrases""""""" (Continued)

67.	Please call . . .	2653
68.	Please enter . . .	2713
69.	Please wait.	27CF
70.	P.M.	287A
71.	Police . . .	28FE
72.	Port	2977
73.	Press the pound key.	29C8
74.	Press the star key.	2ACE
75.	Status	2BC3
76.	Switch	2C48
77.	Terminated.	2CA8
78.	Thank you.	2D38
79.	Thank you for calling.	2DC1
80.	The time is . . .	2ECB
81.	Through	2FAB
82.	To	2FF7
83.	To change your entry . . .	301F
84.	To exit . . .	313E
85.	Warning!	31CF
86.	With	325F
87.	You are listening to Natural Voice from AMI .	3299
88.	You have dialed	3557
89.	Your	363B
90.	Your call back number	368A
91.	Your call cannot be answered at this time.	37A9
92.	Your party	39E7
93.	Zero	3AA0
94.	200ms pause	3B3C
95.	100ms pause	3B5A
96.	80ms pause	3B69
97.	40ms pause	3B75
98.	Tone	3B7B to 3B97

Words can be concatenated to form phrases or sentences. Some examples are:

Sample One:

Hello. / 200ms / This is an automatic message. / You are listening to Natural Voice from AMI. / / 200ms / Thank you for calling. / 200ms / Good-by.

Sample Two:

Business hours are / Monday / thru / Friday / from / 9 / A.M. / to / 7 / 40ms / P.M. /

Sample Three:

Please call / your party / before / 3 / P.M.

Sample Four:

Please enter / your call back number / with / 40ms / area code / after the tone. / 200ms / tone /

Sample Five:

To exit / 80ms / press the pound key.

AMI

A Subsidiary of Gould Inc.

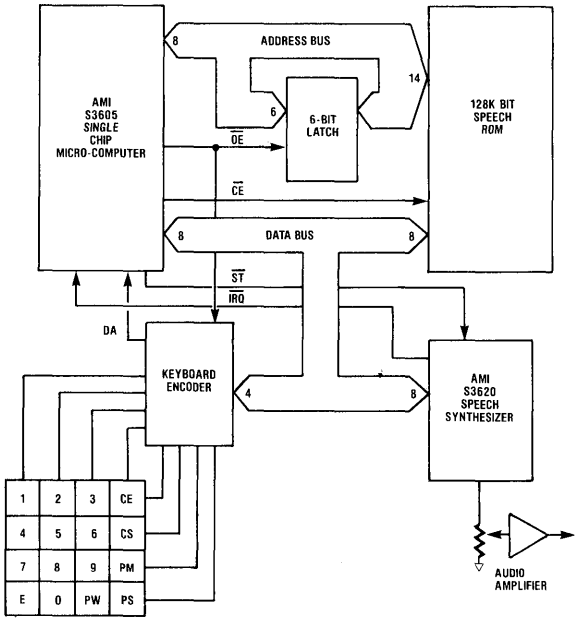
EVK 3620

SPEECH SYNTHESIS EVALUATION BOARD

Features

- Needs only a + 5V source and either an 8 ohm or 100 ohm loudspeaker for complete operation. (With the addition of a 7805 regulator and a capacitor it can be run by a 9V battery eliminator similar to calculators and video games.)
- Large speech vocabulary (up to 100 seconds of speech stored in a 128K bit ROM).
- Demonstrates the wide application range of the S3620 speech synthesis chip.
- Programmed microcomputer (S3605) provides several modes of operation such as:
  - — Play a single word
  - — Build and play a phrase
  - — Repeat word or phrase
  - — Play preprogrammed messages
  - — Play the entire vocabulary
- Edge connector for interfacing with user system for product prototyping.
- Onboard audio amplifier.

EVK 3620 Speech Board Block Diagram



Edge Connector Assignments

GROUND	A	1	GROUND
+ 5V	B	2	+ 5V
≥ + 8V	C	3	≥ + 8V
	D	4	
8 OHM OUT	E	5	8U
100 OHM OUT	F	6	100 OHM OUT
D_4	H	7	D_0
D_5	J	8	D_1
D_6	K	9	D_2
D_7	L	10	D_3
	M	11	
A_7	N	12	A_0
A_8	P	13	A_1
A_9	R	14	A_2
A_{10}	S	15	A_3
A_{11}	T	16	A_4
A_{12}	U	17	A_5
A_{13}	V	18	A_6
OE	W	19	DA
ST	X	20	
	Y	21	IRQ
	Z	22	CE

A Subsidiary of Gould Inc.

S4520

30-Volt Dichroic LCD Driver

Features

- ☐ High Voltage Outputs Capable of a 32-Volt Swing
- ☐ Drives Up to 38 Devices
- ☐ Cascadable
- ☐ On-Chip Oscillator
- ☐ Requires Only 4 Control Lines
- ☐ CMOS Construction For:
  - Wide Supply Range
  - Low Power Consumption
  - High Noise Immunity
  - Wide Temperature Range

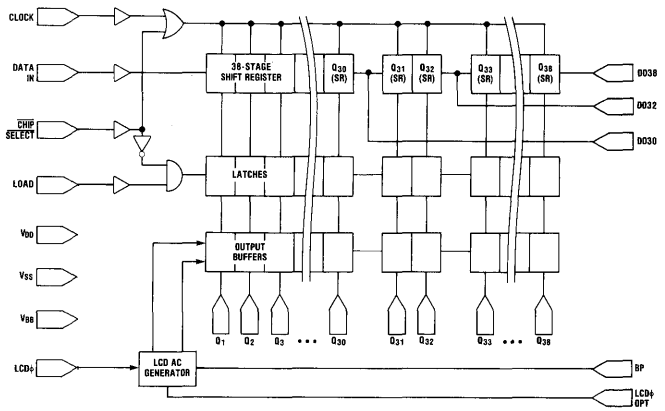
Applications

- ☐ Liquid Crystal Displays
- ☐ Flat Panel Displays
- ☐ Print Head Drives

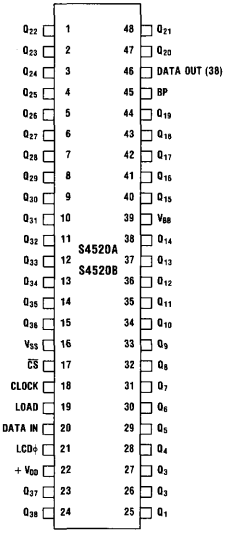
General Description

The AMI S4520 is a CMOS/LSI circuit that drives high-voltage dichroic liquid crystal displays, usually under microprocessor control. The S4520 requires only four control inputs (CLOCK, DATA IN, LOAD and $\overline{\text{CHIP SELECT}}$) due to its serial input construction. It can latch the data to be output, relieving the microprocessor from the task of generating the required waveforms, or it may be used to bring data directly to the drivers. The A.C. frequency of the backplane output can be generated by the internal oscillator or, the user has the option of supplying this signal from an external source. If the internal oscillator is used to generate the backplane signal, the frequency will be determined by an external resistor and capacitor. One S4520 circuit can drive 38 segments. Other packaging options can provide 30 or 32 segment drivers.

Block Diagram



Pin Configuration



Absolute Maxiumum Ratings

V_{DD} ..... −0.3 to +17V
V_{BB} ..... V_{SS} +0.3V to V_{DD} −32V
Inputs (CLK, DATA IN, LOAD, LCDϕ) ..... V_{SS} −0.3V to V_{DD} +0.3V
Power Dissipation 250mW
Storage Temperature ..... −65°C to +125°C
Operating Temperature ..... −55°C to +85°C

Electrical Characteristics: $3V \leqslant V_{DD} \leqslant 16V$, $-55°C \leqslant T_A \leqslant +85°C$, unless otherwise noted

Symbol	Parameter	Min.	Max.	Units	Test Condition
	Power Supply				
V_{DD}	Logic Supply Voltage	3	16	V	
V_{BB}	Display Supply Voltage	$V_{DD}-32$ $V_{DD}-32$	$V_{DD}-15$ $V_{DD}-22$	V V	$V_{DD} \leqslant 11V$ $V_{DD} \geqslant 11V$
I_{DD}	Supply Current (external oscillator) Supply Current (internal oscillator)		200 200 750	μA μA μA	CMOS input levels. No loads. $V_{DD} \leqslant 5V$ V_{DD} = 16V; CMOS input levels. No loads.
I_{BB}	Display Driver Current		−200	μA	f_{BP} = 100Hz. No loads.
	Inputs (CLK, DATA IN, LOAD, $\overline{CS}$)				
V_{IH}	Input High Level	$0.5V_{DD}$	V_{DD}	V	$V_{DD} \geqslant 5V$
V_{IL}	Input Low Level	V_{SS}	$0.2V_{DD}$	V	
I_L	Input Leakage Current		5	μA	
C_I	Input Capacitance		5	pF	
$V_{O_{AVG}}$	DC Bias (Average) Any Segment Output to Backplane		±25	mV	$f_{BP} \leqslant 100Hz$
V_{IH}	LCDϕ Input High Level	$0.9V_{DD}$	V_{DD}	V	Externally Driven
V_{IL}	LCDϕ Input Low Level	V_{BB}	$0.1V_{DD}$	V	Externally Driven
	Capacitance Loads (typical)				
$C_{L_{SEG}}$	Segment Output		1000	pF	$f_{BP} \leqslant 100Hz$
$C_{L_{BP}}$	Backplane Output		40000	pF	$f_{BP} \leqslant 100Hz$
R_{SEG}	Segment Output Impedance		10	KΩ	I_L = 10 μA
R_{BP}	Backplane Output Impedance		312	Ω	I_L = 10 μA
R_{DO}	Data Out Output Impedance		3	KΩ	I_L = 10 μA

Operating Notes

1. The shift register loads and shifts on the falling edge of CLK. DATA OUT changes on the rising edge of CLK.
2. The buffer number corresponds to how many clock pulses have occurred since its data was present at the input (e.g., the data on Q_{10} was input 10 clock pulses earlier). DATA is shifted into Segment 1 and shifted out from Segments 30, 32 or 38, depending on bonding option used.
3. A logic 1, shifted into the shift register (through DATA IN), causes the corresponding segment's output to be out of phase with the backplane.
4. A logic 1 on LOAD causes a parallel load of the data in the shift register, into the latches that control the output drivers.
5. LOAD may also be held high while clocking. In this case, the latch is transparent and, the falling edge of LOAD will latch the data.
6. To cascade units, (a) connect the DATA OUT of one chip to the DATA IN of the next chip, and (b) either connect the backplane of one chip to LCDϕ of all other chips (thus one RC provides frequency control for all chips) **or** connect LCDϕ of all chips to a common driving signal. If the former is chosen, the backplane that is tied to the LCDϕ of the other chips should **not** also be connected to the backplanes of those chips.
7. The LCDϕ pin can be used in two modes, driven or self-oscillating. If LCDϕ is driven, the circuit will sense this condition. If the LCDϕ pin is allowed to oscillate, its frequency is determined by an external capacitor. The Backplane frequency is a divide by 256 of the LCDϕ frequency, in the self-oscillating mode.
8. If LCDϕ is driven externally, it is in phase with the backplane output.
9. Backplanes can be tied together, if they have the same signal applied to their LDCϕ inputs.
10. In the self-oscillating mode, the backplane frequency is approximately defined by the relationship $f_{BP}(Hz) = 10 \div R(C + .0002)$ at $V_{DD} = 5V$, R in KΩ, C in μF.

    examples: R = 56KΩ, C = .0015 μF: $f_{BP} \doteq 100Hz$
    R = 110Ω, C = .00068 μF: $f_{BP} \doteq 100Hz$
11. Minimum value of R for RC oscillator is 50KΩ.
12. Power consumption increases for clock rise or fall times greater than 100ns.

Pin Description

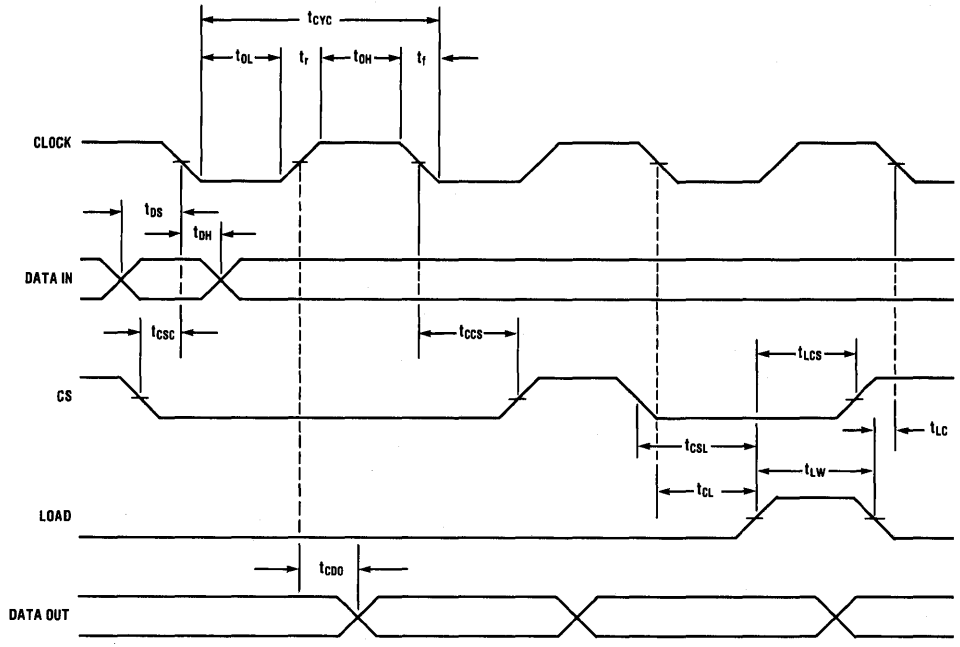
Pin #*	Pin #**	Name	Description
22	23	V_{DD}	Logic Supply Voltage
39	40	V_{BB}	Display Supply Voltage
16	17	V_{SS}	Ground Connection
17	18	$\overline{CS}$	Chip Select Inverse Input
18	19	CLOCK	System Clock Input
19	20	LOAD	Input Signal to Latch Shift Register Data
21	22	LCDϕ	LCD Oscillator Input
21	22	LCDϕ OPTION	LCD Oscillator Option (S4520A,S4520C)
20	21	DATA IN	Data Input to Shift Register
46	47	D038	Data Output from Shift Register (after bit 38)—Primarily used for cascading
45	46	BP	Backplane Drive Output
1-15,23-38 40-44, 47,48	1-16,24-39, 41-45, 48	Q_1-Q_{38}	Segment Outputs

*S4520A-Internal Oscillator, 48-Pin Plastic DIP
**S4520C-Internal Oscillator, 48-Lead Ceramic Chip Carrier
S4520B-External Oscillator, 48-Pin Plastic DIP
S4520D-External Oscillator, 48-Lead Ceramic Chip Carrier

Timing Characteristics:

Symbol	Parameter	Min.	Max.	Units	V_{DD}
t_{CYC}	Cycle time (noncascaded)	1000 500 320		ns ns ns	3.0V 5.0V ≥7.5V
t_{CYC}	Cycle time (cascaded)	1300 600 350		ns ns ns	3.0V 5.0V ≥7.5V
t_{OL}, t_{OH}	Clock pulse width low/high	450 220 140		ns ns ns	3.0V 5.0V ≥7.5V
t_{OH}	Clock pulse width high (cascaded)	750 320 180		ns ns ns	3.0V 5.0V ≥7.5V
t_r, t_f	Clock rise, fall (Note 12)		1	μs	
t_{DS}	Data In setup	300 150 120		ns ns ns	3.0V 5.0V ≥7.5V
t_{CSC}	$\overline{CS}$ setup to Clock	200 100 50		ns ns ns	3.0V 5.0V ≥7.5V
t_{DH}	Data hold	10		ns	
t_{CCS}	$\overline{CS}$ hold	450 220 140		ns ns ns	3.0V 5.0V ≥7.5V
t_{CL}	Load pulse setup (Note 5)	500 280 180		ns ns ns	3.0V 5.0V ≥7.5V
t_{LCS}	$\overline{CS}$ hold (rising LOAD to rising $\overline{CS}$)	300 200 150		ns ns ns	3.0V 5.0V ≥7.5V
t_{LW}	Load pulse width (Note 5)	500 220 140		ns ns ns	3.0V 5.0V ≥7.5V
t_{LC}	Load pulse delay (Falling load to falling clock)	0		ns	
t_{CDO}	Data Out valid from Clock		550 220 110	ns ns ns	3.0V 5.0V ≥7.5V
t_{CSL}	$\overline{CS}$ setup to LOAD	0		ns	

Figure 1. Signal Timing Diagram



Logic Truth Table

DATA IN	CLOCK	$\overline{\text{CHIP SELECT}}$	LOAD	O_1(SR)	O_4(SR)	BP	O_4(DRIVER)
X	X	1	0	NC	NC	0	QN(L)
X	X	1	1	NC	NC	1	QN(L)
0	⌐	0	0	NC	NC	1	QN(L)
0	⌐	0	1	NC	NC	1	QN(L)
0	⌐	0	0	0	QN—1→QN	1	QN(L)
0	⌐	0	1	0	QN—1→QN	1	QN(SR)
1	⌐	0	0	NC	NC	1	QN(L)
1	⌐	0	1	NC	NC	1	QN(L)
1	⌐	0	0	1	QN—1→QN	1	QN(L)
1	⌐	0	1	1	QN—1→QN	1	QN(SR)

Notes: NC = No Change SR = Shift Register L = Latch

Chip Select Inverse Input

The $\overline{CS}$ input is used to enable clocking of the shift register. When $\overline{CS}$ is low, the chip will be selected and the shift register will be enabled. When $\overline{CS}$ is high, the shift register will be disabled and the output buffers will be driven by the data in the latches.

Clock Input

The CLOCK input is used to clock data serially, into the shift register. A clock signal may be continuously present, because the shift register is enabled only when $\overline{CS}$ is low.

Load Input

The LOAD input controls the operation of the data latches and allows new data to be loaded into the shift register, without changing the appearance of the display. When LOAD is high, the values in the shift register will be loaded into the data latches. If desired, LOAD can be held high and the data latches will be transparent. The LOAD input is disabled when $\overline{CS}$ is high.

LCD Oscillator Input

When used with an external oscillator, the LCD oscillator is driven by the input voltage level. In this configuration, the backplane output will be in phase with the input waveform. In the self-oscillating mode, an external resistor and capacitor are connected to the oscillator input pin, and the backplane frequency will be a divide by 256 of the internal oscillator frequency.

LCD Oscillator Option

When the internal oscillator is used, the LCD oscillator option is internally (or externally) connected to the LCD oscillator input and, it provides the oscillator feedback. When used with an external oscillator, the LCD oscillator option is not connected (i.e. LCDϕ OPTION is grounded).

Data Input

Data present at DATA IN will be clocked into the shift register, when $\overline{CS}$ is low. Data is loaded into the shift register on the falling edge of the clock and shifts to the output on the rising clock edge.

Data Output

Depending on the packaging option selected, DO30, DO32 and DO38 are buffered outputs driven by the corresponding element of the shift register. The value of DOxx will be the same as the value of the matching shift register bit (i.e. the value at DO32 will be the same as bit 32 of the shift register). The data output is typically used to drive the data input of another S4520. By cascading S4520 circuits in this manner, additional display elements can be driven.

Backplane Output

The backplane output provides the voltage waveform for the LCD backplane. When used with the internal oscillator, the backplane frequency will be equal to the oscillator frequency divided by 256:

$$f_{BP} = f_{OSC}\,(\text{int}) \div 256.$$

With an external oscillator, the backplane frequency will be in phase with and equal in magnitude to the input signal.

Segment Drive Outputs

The segment drive outputs provide the segment drive voltage to the LCD. With a logic level "1" in the latch associated with the segment drive output, the output voltage will be out of phase with the backplane (i.e the segment will be ON). A logic level "0" will cause the segment drive to be in phase with the backplane output voltage.

Figure 2. Typical Application

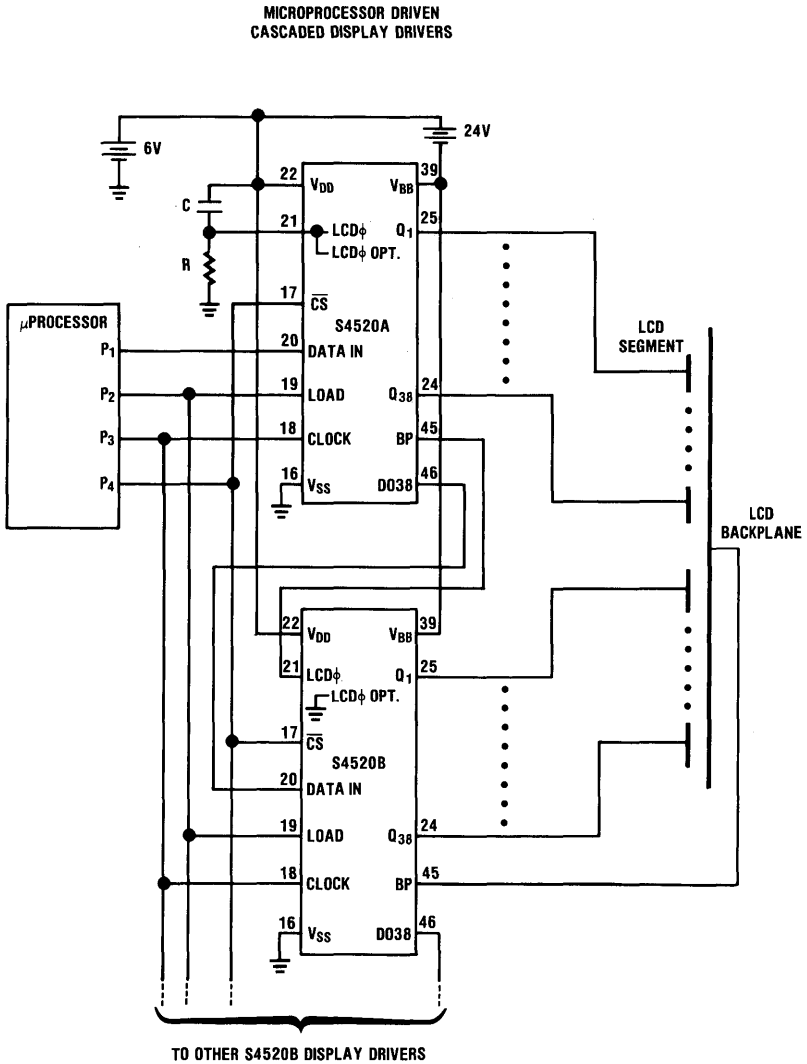
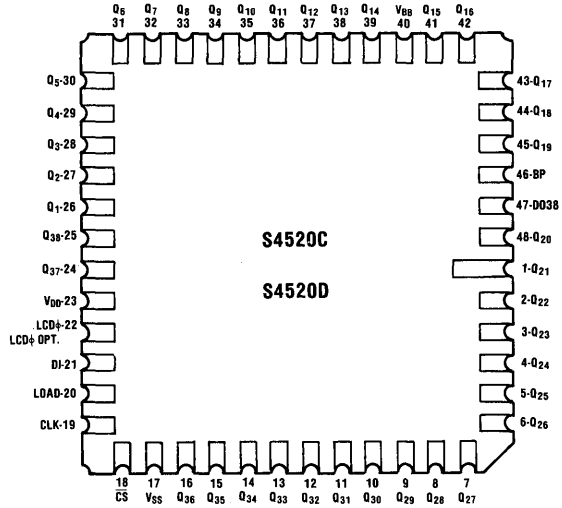


Figure 3. 48-Lead Ceramic Chip Carrier



NOTE: VIEWED FROM THE BOTTOM SIDE OF THE PACKAGE

Ordering Instructions

1. All orders must specify a package type (i.e. S4520A, 48-pin plastic DIP)
2. All orders must specify whether an internal oscillator or external oscillator will be used (i.e. S4520B, external oscillator).
3. A set-up charge or minimum order quantity may apply for packaging options not shown. Please contact factory for further information.

AMI

A Subsidiary of Gould Inc.

S4521

32 BIT DRIVER

Features

- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ On Chip Oscillator
- ☐ Requires Only 3 Control Lines
- ☐ CMOS Construction For:
  - Wide Supply Range
  - High Noise Immunity
  - Wide Temperature Range

Applications:

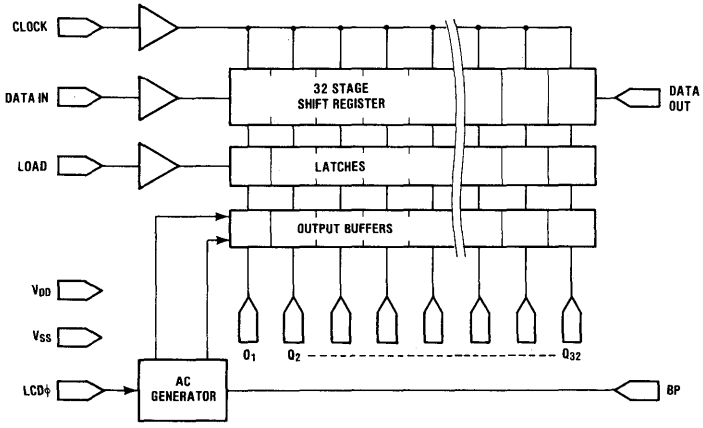
- ☐ Liquid Crystal Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

General Description

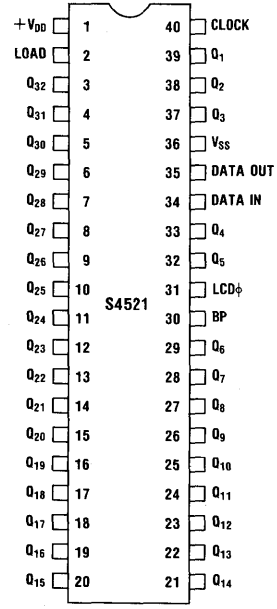
The AMI S4521 is an MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control. This device requires only three control lines due to its serial input construction. It latches the data to be output, relieving the microprocessor from the task of generating the required waveform, or it may be used to bring data directly to the drivers. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations. It is especially well suited to driving liquid crystal displays, with a backplane A.C. signal option that is provided. The A.C. frequency of the backplane output that can be user supplied or generated by attaching a capacitor to the LCDϕ input, which controls the frequency of the internal oscillator. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together. The S4521F version is available in a surface-mountable plastic mini-flat pack.

CONSUMER PRODUCTS

Functional Block Diagram



Pin Configuration



Absolute Maximum Ratings

V_{DD}	-0.3 to $+17V$
Inputs (CLK, DATA IN, LOAD, LCDϕ)	$V_{SS}-0.3$ to $V_{DD}+0.3V$
Power Dissipation	250mW
Storage Temperature	$-65°C$ to $+125°C$
Operating Temperature	$-40°C$ to $+85°C$

Electrical Characteristics: $3V \leqslant V_{DD} \leqslant 13V$, unless otherwise noted

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{DD}	Supply Voltage	3	13	V	
	Supply Current				
I_{DD1}	Operating		200	μA	f_{BP} = 120Hz, No Load, $V_{DD}=5V$
I_{DD2}	Quiescent		200	μA	LCDϕ High or Low, $f_{BP}=0$
					Load @ Logic 0, $V_{DD}=5V$
	Inputs (CLK, DATA IN, LOAD)				
V_{IH}	High Level	0.6 V_{DD}	V_{DD}	V	$3V \leqslant V_{DD} < 5V$
		0.5 V_{DD}	V_{DD}	V	$5V \leqslant V_{DD} \leqslant 13V$
V_{IL}	Low Level	V_{SS}	0.2 V_{DD}	V	
I_L	Input Current		5	μA	
C_I	Input Capacitance		5	pF	
f_{CLK}	CLK Rate	DC	2	MHz	50% Duty Cycle
t_{DS}	Data Set-Up Time	100		ns	Data Change to CLK Falling Edge
t_{DH}	Data Hold Time	10		ns	Falling CLK Edge to Data Change
t_{PW}	Load Pulse Width	200		ns	
t_{PD}	Data Out Prop. Delay		220	ns	$C_L=30pF$, From Rising CLK Edge
t_{LC}	Load Pulse Set-Up	300		ns	Falling CLK Edge to Rising Load Pulse
t_{LCD}	Load Pulse Delay	0		ns	Falling Load Pulse to Falling CLK Edge
V_{0AVG}	DC Bias (Average) Any Q Output to Backplane		±25	mV	f_{BP} = 120Hz
V_{IH}	LCDϕ Input High Level	.9 V_{DD}	V_{DD}	V	Externally Driven
V_{IL}	LCDϕ Input Low Level	V_{SS}	.1 V_{DD}	V	Externally Driven
	Capacitance Loads				
C_{LQ}	Q Output		50,000	pF	f_{BP} = 120Hz
C_{LBP}	Backplane		1.5	μF	f_{BP} = 120Hz, See Note 8
R_{ON}	Q Output Impedance		3.0	KΩ	I_L = 10μA, $V_{DD}=5V$
R_{ON}	Backplane Output Impedance		100	Ω	$I_L=10\mu A$, $V_{DD}=5V$
R_{ON}	Data Out Output Impedance		3.0	KΩ	$I_L=10\mu A$, $V_{DD}=5V$

Operating Notes

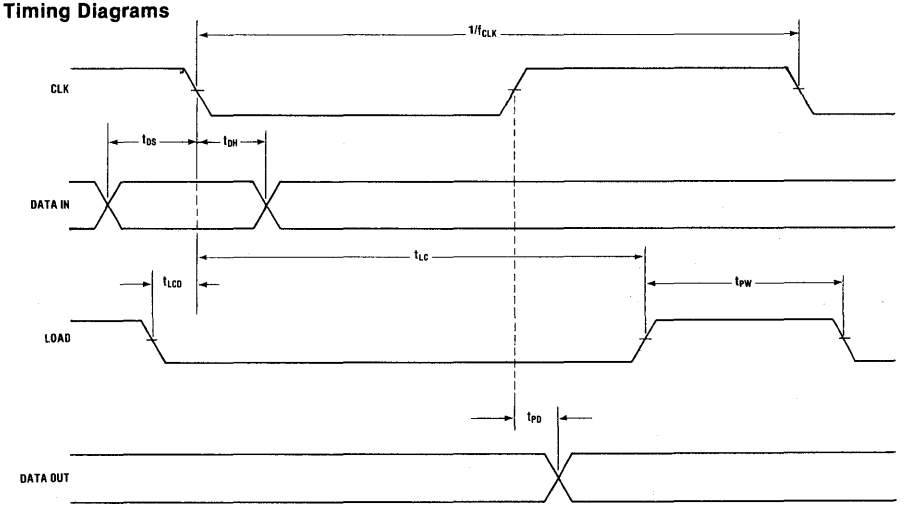
1. The shift register shifts on the falling edge of CLK. It outputs on the rising edge of the CLK.
2. The buffer number corresponds to how many clock pulses have occurred since its data was present at the input (e.g., the data on Q10 was input 10 clock pulses earlier).
3. A logic 1 on Data In causes a Q output to be out of phase with the Backplane.
4. A logic 1 on Load causes a parallel load of the data in the shift register, into the latches that control the Q output drivers.
5. To cascade units, (a) connect the Data Out of one chip to Data In of next chip, and (b) either connect Backplane of one chip to LCDϕ of all other chips (thus one RC provides frequency control for all chips) or connect LCDϕ of all chips to a common driving signal. If the former is chosen, the Backplane that is tied to the LCDϕ inputs of the other chips should **not** also be connected to the Backplanes of those chips.
6. If LCDϕ is driven, it is in phase with the Backplane output.
7. The LCDϕ pin can be used in two modes, driven or self-oscillating. If LCDϕ is driven, the circuit will sense this condition. If the LCDϕ pin is allowed to oscillate, its frequency is determined by an external capacitor. The Backplane frequency is a divide by 32 of the LCDϕ frequency, in the self-oscillating mode.
8. In the self-oscillating mode, the backplane frequency is approximately defined by the relationship $f_{BP}(Hz) = 0.2 \div C(in\ \mu F)$ at $V_{DD} = 5V$.
9. If the total display capacitance is greater than 100,000 pF, a decoupling capacitor of 1μF is required across the power supply (pins 1 and 36).

Pin Description

Pin #	Name	Description
1	V_{DD}	Logic and Q Output Supply Voltage
2	LOAD	Signal to Latch Data from Registers
30	BP	Backplane Drive Output
31	LCDϕ	Backplane Drive Input
34	DATA IN	Data Input to Shift Register
35	DATA OUT	Data Output from Shift Register-primarily used in cascading
36	V_{SS}	Ground Connection
40	CLOCK	System Clock Input
3-29, 32-33, 37-39	Q_1-Q_{32}	Direct Drive Outputs

CONSUMER PRODUCTS

Signal Timing Diagrams



A Subsidiary of Gould Inc.

S4535

32 BIT, HIGH VOLTAGE DRIVER

Features

- ☐ High Voltage Outputs Capable of 60 Volt Swing
- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

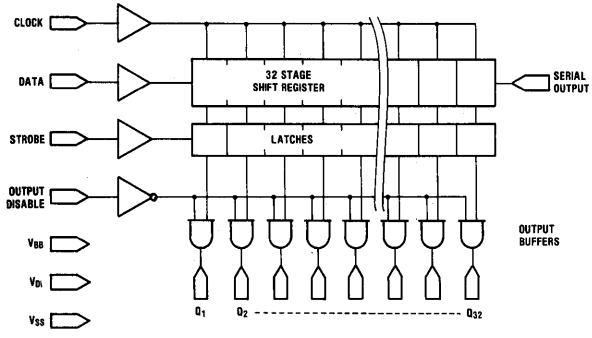
Applications:

- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

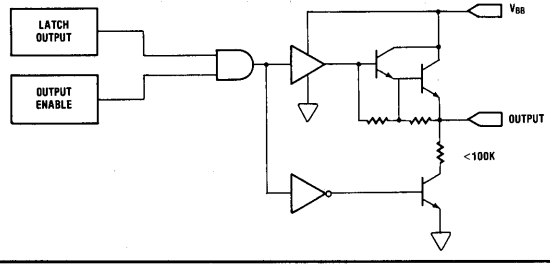
General Description

The AMI S4535 is a high voltage MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 25mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

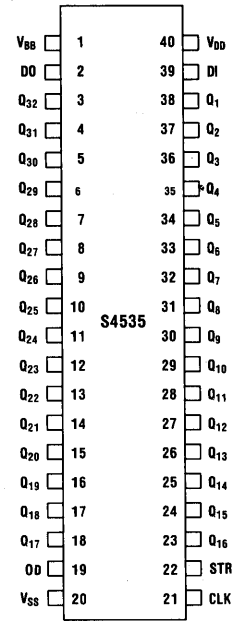
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



Absolute Maximum Ratings at 25°C

V_{BB}	65V
V_{DD}	12V
V_{IN}	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Logic)	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Display)	V_{SS} – .3V to V_{BB} + .3V
Power Dissipation	1.6W
Operating Temperature	0°C to + 70°C*
Storage Temperature	– 65°C to + 125°C

* Extended temperature range available. Please contact AMI for price and delivery information.

Operational Specification: $0°C \leq T_A \leq 70°C$ (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IL}	Input Zero Level	–0.3	0.8	V	
V_{IH}	Input One Level	3.5	V_{DD}+0.3	V	
V_{SL}	Signal Out Zero Level	V_{SS}	0.5	V	$I_{SO} = -20\mu A$
V_{SH}	Signal Out One Level	V_{DD}–0.5	V_{DD}	V	$I_{SO} = 20\mu A$
V_{DD}	Logic Voltage Supply	4.5	5.5	V	
V_{BB}	Display Voltage Supply	20	60	V	
I_{DD}	Logic Supply Current		35	mA	No Loads, T=25°C
I_{BB}	Display Supply Current		10 168	mA mA	No Loads, T=25°C With Load
V_{OL}	Output Zero Level	V_{SS}	1.0	V	$I_O = -20\mu A$
V_{OH}	Output One Level	V_{BB}–2.5 V_{BB}–3.2	V_{BB} V_{BB}	V V	I_O=5mA I_O=25mA, One Output
t_{SD}	Serial Out Prop. Delay		500	ns	C_L=50pF
t_{PD}	Parallel Out Prop. Delay		5	μs	C_L=50pF
t_W	Input Pulse Width	500		ns	
t_{SU}	Data Set-Up Time	150		ns	
t_H	Data Hold Time	50		ns	

CONSUMER PRODUCTS

Functional Description

Serial data present at the input is transferred to the shift register on the Logic "0" to Logic "1" transition of the clock input signal. On succeeding clock pulses, the registers shift data information towards the serial data output. The input serial data must be presented prior to the rising edge of the clock input waveform.

Information present at any register is transferred to its respective latch when the strobe signal is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the strobe signal is held high.

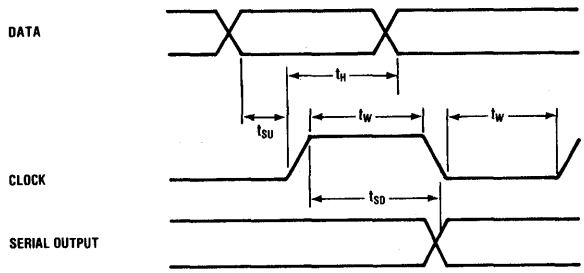
When the output disable input is high, all of the high voltage buffers are disabled without affecting the information stored in the latches or shift register. With the output disable signal low, the high voltage outputs are controlled by the state of the latches.

Pin Description

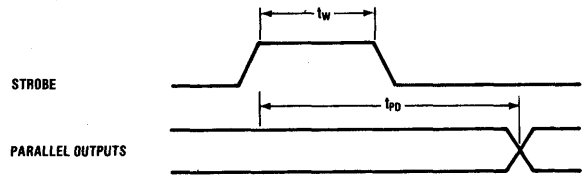
Pin #	Name	Description
20	V_{SS}	Ground Connection
2	DO	Output of Shift Register—primarily used for cascading
19	OD	Output Disable
1	V_{BB}	Q Output Drive Voltage
21	CLK	System Clock Input
40	V_{DD}	Logic Supply Voltage
22	STR	Strobe to Latch Data from Registers
39	DI	Data Input to Shift Register
3-18 and 23-38	Q_1-Q_{32}	Direct Drive Outputs

Signal Timing Diagrams

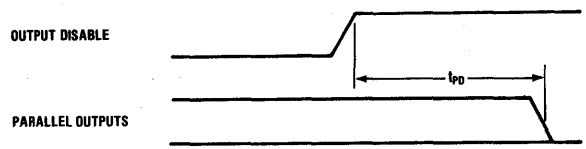
Data Write



Data Read



Output Inhibit



A Subsidiary of Gould Inc.

S4534

10 BIT, HIGH VOLTAGE HIGH CURRENT DRIVER

CONSUMER PRODUCTS

Features

- ☐ Outputs Capable of 60 Volt Swings at 25mA
- ☐ Drives Up to 10 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

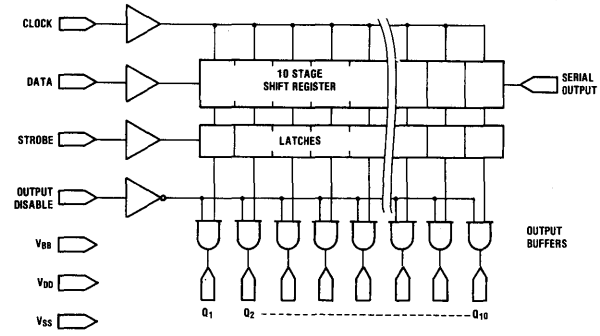
Applications:

- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

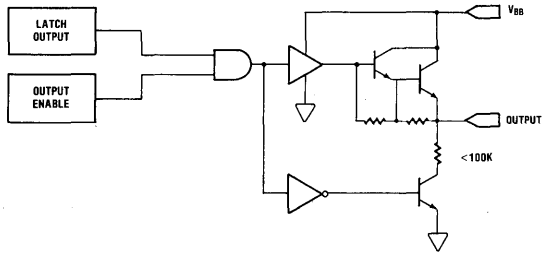
General Description

The AMI S4534 is a high voltage, high current MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 50mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 10 devices and more can be driven by cascading several drivers together.

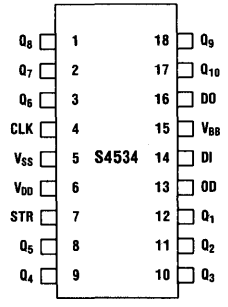
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



Absolute Maximum Ratings at 25°C

V_{BB}	65V
V_{DD}	4.5 to 15V
V_{IN}	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Logic)	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Display)	V_{SS} – .3V to V_{BB} + .3V
Power Dissipation	1.2W
Operating Temperature	0°C to +70°C
Storage Temperature	–65°C to +125°C

Operational Specification: $0°C \leqslant T_A \leqslant 70°C$ (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IL}	Input Zero Level	–0.3	1.1	V	
V_{IH}	Input One Level	3.4 3.6	$V_{DD}+0.3$ $V_{DD}+0.3$	V V	$4.75V \leqslant = V_{DD} < 5.25V$ $5.25V \leqslant V_{DD} \leqslant 12.0V$
I_{IN}	Input Leakage Current		1.0	μA	$V_{DD} = 5V$
V_{SL}	Signal Out Zero Level	V_{SS}	0.7	V	$I_{SO} = -20\mu A$
V_{SH}	Signal Out One Level	$V_{DD}-.95$ 4.3	V_{DD} V_{DD}	V V	$I_{SO} = 20\mu A$, $4.75V \leqslant V_{DD} < 5.25V$ $I_{SO} = 20\mu A$, $5.25V \leqslant V_{DD} \leqslant 12.0V$
V_{DD}	Logic Voltage Supply	4.75	12	V	
V_{BB}	Display Voltage Supply	20	60	V	
I_{DD}	Logic Supply Current		20 30	mA mA	No Loads, $V_{DD} = 5V$ No Loads, $V_{DD} = 10V$
I_{BB}	Display Supply Current		6	mA	No Loads, T = 25°C
V_{OL}	Output Zero Level	V_{SS}	1.0	V	$I_O = -20\mu A$
V_{OH}	Output One Level	$V_{BB}-2.5$	V_{BB}	V	$I_O = 25mA$
t_{SD}	Serial Out Prop. Delay	60	375	ns	$C_L = 50pF$
t_{PD}	Parallel Out Prop. Delay		5	μs	$C_L = 50pF$
t_W	Input Pulse Width	375		ns	
t_{SU}	Data Set-Up Time	150		ns	
t_H	Data Hold Time	40		ns	

Functional Description

Serial data present at the input is transferred to the shift register on the Logic "0" to Logic "1" transition of the clock input signal. On succeeding clock pulses, the registers shift data information towards the serial data output. The input serial data must be presented prior to the rising edge of the clock input waveform.

Information present at any register is transferred to its respective latch when the strobe signal is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the strobe signal is held high.

When the output disable input is high, all of the high voltage buffers are disabled without affecting the information stored in the latches or shift register. With the output disable signal low, the high voltage outputs are controlled by the state of the latches.

At low logic supply voltages, it is possible that the serial data output (DO) may be unstable for up to 2μs, after the rising edge of the strobe (STR) or output disable (OD) inputs.

Table 1.

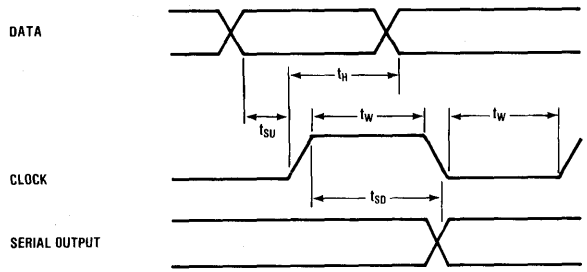
NUMBER OF OUTPUTS ON (I_{OUT} = 25mA)	MAX. ALLOWABLE DUTY CYCLE AT AMBIENT TEMPERATURE OF				
	25°C	40°C	50°C	60°C	70°C
10	100%	97%	85%	73%	62%
9	↑	100%	94%	82%	69%
8	↑	↑	100%	92%	78%
7	↑	↑	↑	100%	89%
6	↑	↑	↑	↑	100%
1	100%	100%	100%	100%	100%

Pin Description

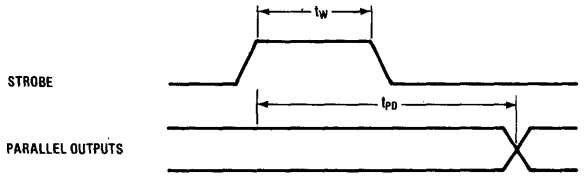
Pin #	Name	Description
5	V_{SS}	Ground Connection
16	DO	Output of Shift Register—primarily used in cascading
13	OD	Output Disable
15	V_{BB}	Q Output Drive Voltage
4	CLK	System Clock Input
6	V_{DD}	Logic Supply Voltage
7	STR	Strobe to Latch Data from Registers
14	DI	Data Input to Shift Register
1-3, 8-12, 17-18	Q_1-Q_{10}	Direct Drive Outputs

Signal Timing Diagrams

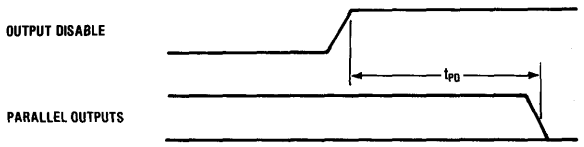
Data Write



Data Read



Output Inhibit



CONSUMER PRODUCTS

AMI®

A Subsidiary of Gould Inc.

Advanced Product Description **S2809**

UNIVERSAL DISPLAY DRIVER

Features

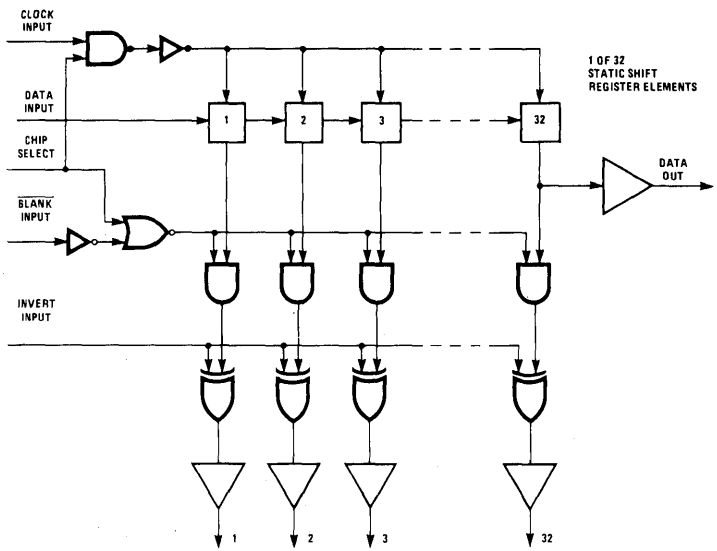
- ☐ 32 Bit Storage Register
- ☐ 32 Output Buffers
- ☐ Expansion Capability for More Bits
- ☐ Reduced RFI Emanation
- ☐ Wired OR Capability for Higher Current

General Description

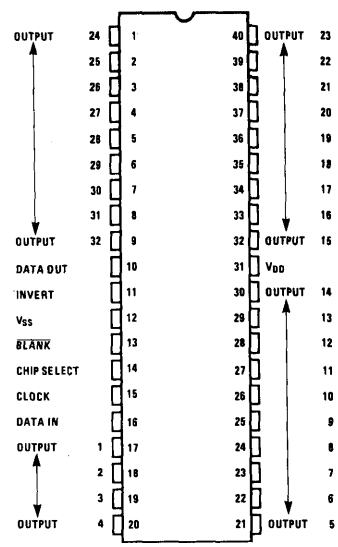
The S2809 Universal Driver is a P-Channel MOS integrated circuit. Data is clocked serially into a 32-bit master-slave static shift register. This provides static parallel drive to the output bits through drive buffers. To reduce RFI emanation, capacitors have been integrated on the circuit for reduction of output switching speeds. Serial interconnection of circuits is made possible by the Data Out Output, allowing additional bits to be driven.

Two or more outputs may be wired together for higher sourcing currents; useful in applications such as triac triggering or low voltage incandescent displays. The S2809 can also be used as a parallel output device for μC's such as AMI's S2000 series single chip microcomputer.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Operating Ambient Temperature T_A ..... 10°C to +70°C
Storage Temperature ..... −65°C to +150°C
V_{SS} Supply Voltage ..... +25V
Positive Voltage on Any Pin ..... V_{SS} +0.3V

Electrical Characteristics (V_{DD} = 0V, 8V < V_{SS} < 22V, T_A = 10°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Logic 1 Level (Data, Clock, Invert, Chip Select Inputs)	V_{SS} −0.7		V_{SS} +0.3	V	
V_{IL}	Logic 0 Level (Data, Clock Invert, Chip Select Inputs)	V_{DD}		V_{SS} −7	V	
V_{BH}	Logic 1 Level ($\overline{\text{Blank}}$ Input)	V_{SS} −4.0		V_{SS} +0.3	V	
V_{BL}	Logic 0 Level ($\overline{\text{Blank}}$ Input)	V_{DD}		V_{SS} −7	V	
I_B	Current Sinked or Sourced by $\overline{\text{Blank}}$ Input			1.0	μA	Voltage applied to $\overline{\text{Blank}}$ Input between V_{DD} & V_{SS}
C_B	Capacitance of $\overline{\text{Blank}}$ Input			12	pF	
I_{OH}	Output Source Current	9.0			mA	$V_{OUT} = V_{SS}$ −3
I_{OH}	Output Source Current	4.0			mA	$V_{OUT} = V_{SS}$ −1.5
I_{OS}	Sink Current Output Load Device			50	μA	Output voltage = V_{SS}
I_{OS}	Sink Current Output Load Device	10			μA	Output voltage = V_{DD} +3V
I_L	Output Leakage Current (Output Off)			10.0	μA	
I_{DD}	Supply Current			3.0	mA	Not including output source and sink current
I_{OM}	Maximum Total Output Loading			300	mA	All outputs on
f_c	Clock Frequency	DC		100K	Hz	
t_{ON}	Clock Input Logic I Level Duration	3.0			μs	
t_{OFF}	Clock Input Logic 0 Level Duration	6.5			μs	
t_{ro}, t_{fo}	Display Output Current Rise and Fall Times	10		150	μs	*Measured between 10% and 90% of output current V_{SS} < +11V, I_{OH} = 9ma

* **NOTE:** With supply voltages higher than 11 volts, delay exists before an output rise or fall. This delay will not exceed 100μs with a 22 volt supply.

CONSUMER PRODUCTS

Functional Description

The 32-bit static shift register stores data to be used for driving 32 output buffers. Data is clocked serially into the register by the signal applied to the Clock Input whenever a logic 1 level is applied to the Chip Select Input; during this time, outputs are not driven by the shift register but will go to the logic level of the invert input. With a logic 0 level applied to the Chip Select Input, the 32 outputs are driven in parallel by the 32-bit register. It is possible to connect S2809 circuits in series to drive additional bits by use of the Data Output.

Clock Input

The Clock Input is used to clock data serially into the 32-bit shift register. The signal at the Clock Input may be continuous, since the shift register is clocked only when a logic 1 level is applied to the Chip Select Input. As indicated in Table 1, data is transferred from QN-1 to QN on the negative transition of the Clock Input.

Data Input

Whenever a logic 1 level is applied to the Chip Select Input, data present at the the Data Input is clocked into the 32-bit master-slave shift register. Data present at the input to the register is clocked into the master element during the logic 1 clock level and thus must be valid for the duration of the positive clock pulsewidth. This information is transferred to the slave section of each register bit during the clock logic 0 level.

Chip Select

The Chip Select Input is used to enable clocking of the shift register. When a logic 1 level is applied to this input, the register is clocked as described above. During this time, the output buffers are not driven by the register outputs, but will be driven to the logic level present at the Invert Input. With a logic 0 level at the Chip Select Input, clocking of the register is disabled, and the output buffers are driven by the 32 shift register elements.

Blank Input

This input may be used to control display intensity by varying the output duty cycles. With a logic 0 level at the Blank Input, all outputs will turn off (i.e., outputs will go to the logic level of the Invert Input). With a logic 1 level at the Blank Input, outputs are again driven in parallel by the 32 shift register elements (assuming the Chip Select Input is at logic 0).

The Blank Input has been designed with a high threshold to allow the use of a simple RC time constant to control the display intensity. This has been shown in Figure 1.

Invert Input

The Invert Input is used to invert the state of the outputs, if required. With a logic 0 level on this input, the logic level of the outputs is the same as the data clocked into the 32-bit shift register. A logic 1 level on the Invert Input causes all outputs to invert.

This input may also be used when driving liquid crystal displays, as shown in Figure 5.

Data Output

The Data Out signal is a bufferered output driven by element 32 of the shift register. It is of the same polarity as this last register bit and may be used to drive the Data Input of another S2809. In this manner, S2809 circuits may be cascaded to drive additional bits.

Table 1. Logic Truth Table

DATA IN	CLOCK	CHIP SELECT	$\overline{\text{BLANK}}$	INVERT	Q1	QN	DRIVER OUTPUT
X	X	0	0	0			0
X	X	0	0	1		NO CHANGE	1
X	X	0	1	0			QN
X	X	0	1	1			$\overline{\text{QN}}$
0	⌐	1	X	0	0	QN – 1→QN	0
1	⌐	1	X	0	1	QN – 1→QN	0
0	⌐	1	X	1	0	QN – 1→QN	1
1	⌐	1	X	1	1	QN – 1→QN	1

Figure 1. Typical Display Intensity Control

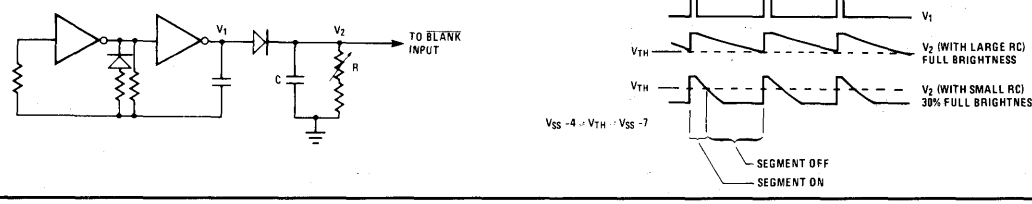


Figure 2. LED Drive — Series

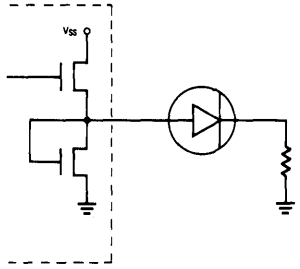


Figure 3. LED Drive — Shunt

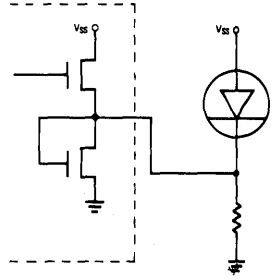


Figure 4. Vacuum Fluorescent Drive

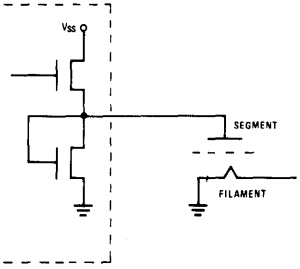


Figure 5. Liquid Crystal Drive

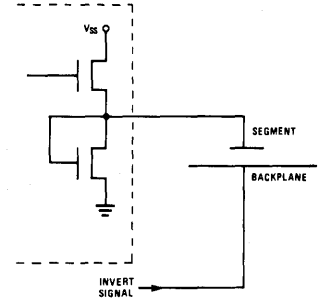
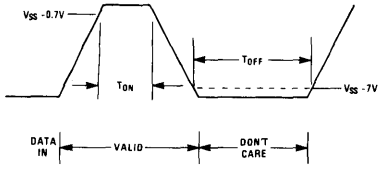
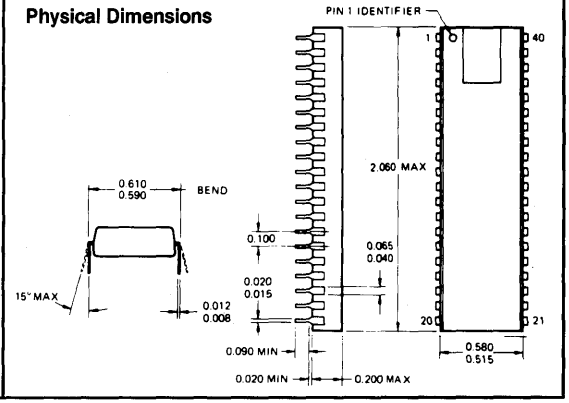


Figure 6. Clock Input Waveform



Physical Dimensions



AMI®

A Subsidiary of Gould Inc.

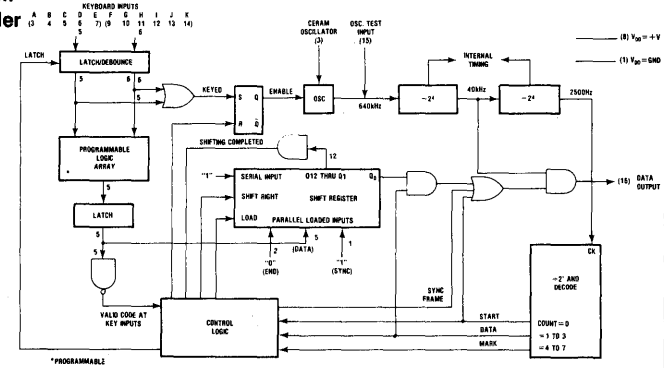
Advanced Product Description **S2600/S2601**

ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

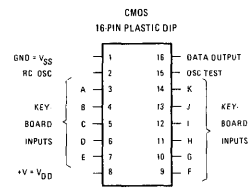
Features

- ☐ Small Parts Count — No Crystals Required
- ☐ Easily Used in LED, Ultrasonic, RF, or Hardwire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 31 Commands — 5-bit Output Bus With Data Valid
- ☐ 3 Analog (LP Filterable PWM) Outputs
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Indexing Output — 2½ Hz Pulse Train
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

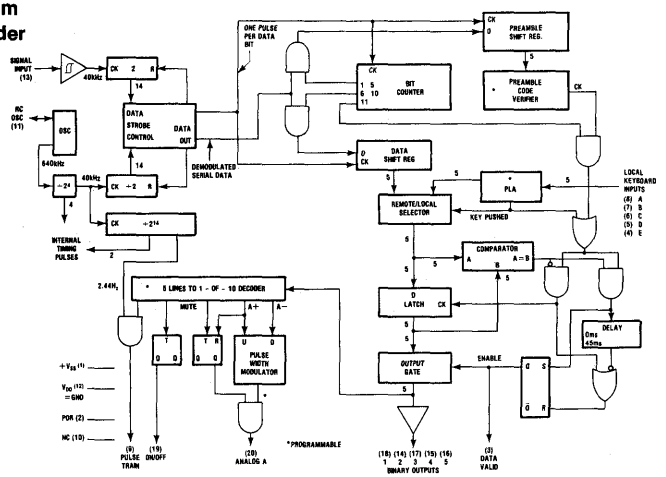
Block Diagram
S2600 Encoder



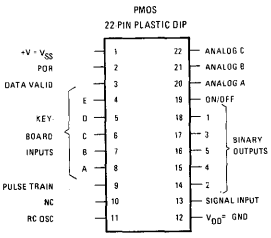
Pin Configuration
S2600



Block Diagram
S2601 Decoder



Pin Configuration
S2601



Functional Description

The S2600/S2601 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a synchronizing marker technique has eliminated the need for highly accurate frequencies generated by crystals. The S2600 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 thru 6 constitute a fixed preamble which must be received correctly for the command bits to be received, and bits 7 through 11 contain the command data. The S2601 Decoder produces an output only after two complete, consecutive, identical, 12-bit transmissions. Marker pulses, preamble bits, and redundant transmissions, have given the S2600/S2601 system a very high immunity to noise, without a large number of discrete components.

S2600 Encoder

The S2600 is a CMOS device with an on-chip oscillator, 11 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator requires only an external resistor and capacitor, and to conserve power, **runs only during transmission.** Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group A through E is activated with one from the group F through K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2600/S2601 CODING," below. This code is loaded into a shift register in parallel with the sync, preamble, and end bits, to form the 12-bit message.

The transmitter output is a 40 kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in a 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The Test input is used for functional testing of the device. A low level input will cause the oscillator frequency to be gated to the Data Output pin. This input has an internal pull-up resistor to V_{DD}.

S2601 Decoder

The S2601 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40kHz signal input, and 11 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2601, overriding any 40kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40kHz signal from the local RC oscillator timing chain. A 40kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ± 24% with respect to the receiver oscillator frequency.

Decoded data bits from the next five bit frames following the initial synchronizing frame are compared with the fixed preamble code. The next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, and if the preamble bits are correct, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next 12-bit transmission. In the case where 2 identical, proper, 12-bit transmissions are immediately followed either by transmissions with erroneous preamble codes or by

nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

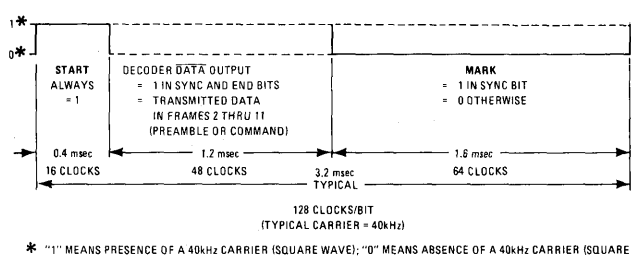
The S2601 has five other outputs: Pulse Train, On/Off, Analog A, Analog B, and Analog C. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated. The Pulse Train output provides a 2.44Hz square wave (50% duty factor) whenever 11011 appears at the Binary Outputs, but otherwise it remains at a logic "0". This pulse train can be used for indexing, e.g., for stepping a TV channel selector.

The On/Off ("mains") output changes state each time 01111 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

Analog Outputs A, B and C are 10kHz pulse trains whose duty factors are independently controllable. With a simple low-pass filter each of these outputs can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. Each Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code—6 codes in all. The entire range of 0% to 100% duty factor can be traversed in 6.5 seconds or at a rate of the oscillator frequency divided by 2^{12}. All three Analog Outputs are set to 50% duty factor whenever 01011 appears at the Binary Outputs. Analog A is mutable; 01100 sets it to 0% duty factor. If 01100 then disappears and reappears, the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2601 has an on-chip power-on reset (POR) circuit which sets the Pulse Train and On/Off Outputs to "0", sets the Analog Outputs at 50% duty factor, and insures that Analog A is muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

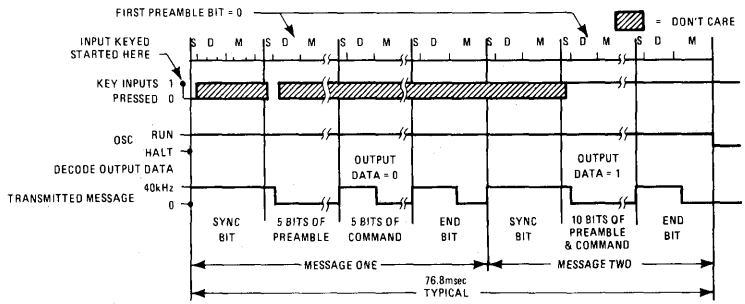
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

** IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



A Subsidiary of Gould Inc.

Advanced Product Description

S2604/S2605

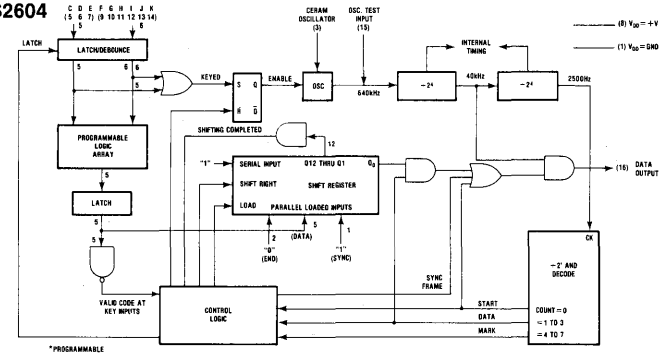
ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

Features

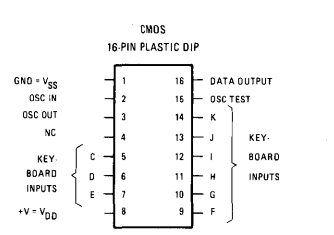
- ☐ Accurate Data Transmission - No Frequency Trimming Required
- ☐ Easily Used in LED, Ultrasonic, RF, or Hardwire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 18 Commands—5-bit Output Bus with Data Valid
- ☐ Analog (LP Filterable PWM) Output
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

CONSUMER PRODUCTS

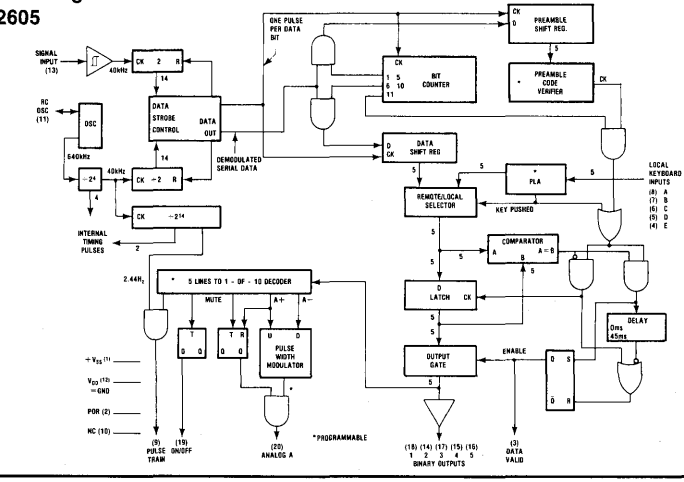
Block Diagram S2604



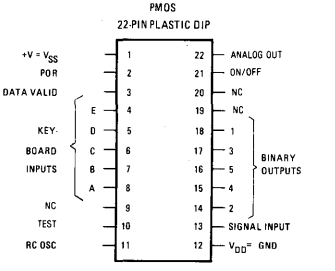
Pin Configuration S2604



Block Diagram S2605



Pin Configuration S2605



Functional Description

The S2604/S2605 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a ceramic resonator with the S2604 Encoder eliminates the need to trim the S2605 decoder oscillator.

The S2604 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 through 6 constitute a fixed preamble which must be received correctly for the command bits to be received, and bits 7 through 11 contain the command data. The S2605 Decoder produces an output only after two complete, consecutive, identical transmissions. Marker pulses, preamble bits, and redundant transmissions, have given the S2604/S2605 system a very high immunity to noise, without a large number of discrete components.

S2604 Encoder

The S2604 is a CMOS device with an on-chip oscillator, 9 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator uses an external ceramic resonator, and to conserve power, **runs only during transmission**. Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group C through E is activated with one from the group F through K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2604/S2605 CODING," below. This code is loaded into a shift register in parallel with the sync and end bits to form the message.

The transmitter output is a 40kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The S2604 Encoder is, however, silenced automatically by an on-chip duration limiter if a transmission persists for 6½ seconds (FOSC = 320kHz). The absence of a keyboard closure will reset the duration limiter so that a new 6½ second interval starts with the next key closure.

S2605 Decoder

The S2605 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40kHz signal input, and 8 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2605, overriding any 40kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40kHz signal from the local RC oscillator timing chain. A 40kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ± 24% with respect to the receiver oscillator frequency.

Decoded data bits from the next five bit frames following the initial synchronizing frame are compared with the fixed preamble code. The next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, and if the preamble bits are correct, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next 12-bit transmission. In the case where 2 identical, proper, 12-bit transmissions are immediately followed either by transmissions with erroneous preamble codes or by nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

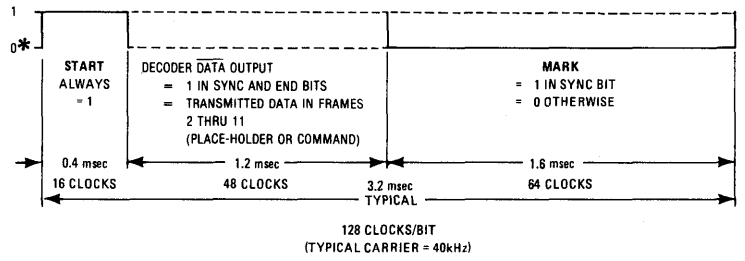
The S2605 has two other outputs: On/Off, and Analog. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated.

The On/Off ("mains") output changes state each time 10011 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

The Analog Output is a 10kHz pulse trains whose duty factors are independently controllable. With a simple low-pass filter each of these outputs can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. Each Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code. The Analog Output is mutable; 11110 sets it to 0% duty factor. If 11110 then disappears and reappears while the On/Off output is "On", the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2605 has an on-chip power-on reset (POR) circuit which sets the On/Off Outputs to "0", sets the Analog Outputs at 50% duty factor, and insures that Analog is not muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

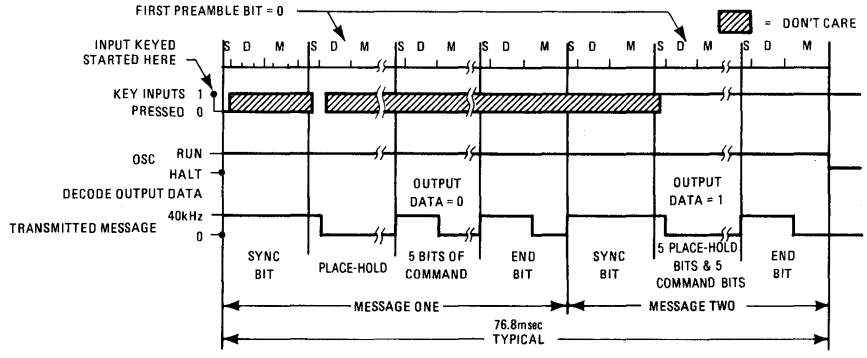
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



S2604/S2605 Coding

TRANSMITTER KEYBOARD INPUT PINS TIED TO V_{SS}	RECEIVER KEYBOARD INPUT PINS TIED TO V_{DD} (Note 1)	RESULTING RECEIVER BINARY OUTPUTS					RECEIVER DEDICATED FUNCTIONS
		1	2	3	4	5	
— (Note 2)		1	1	1	1	1	
DI		0	1	1	1	1	
CF		0	1	1	1	0	
DF		0	1	1	0	1	
EF		0	1	1	0	0	
CG		0	1	0	1	1	
DG		0	1	0	1	0	
EG		0	1	0	0	1	
CH		0	1	0	0	0	
DH		0	0	1	1	1	
EH		0	0	1	1	0	
EI	AE	1	0	1	0	0	
EJ	BE	1	1	0	0	0	
CI	A	1	1	1	0	0	INCREASE ANALOG (Note 5)
CJ	B	1	1	1	0	1	DECREASE ANALOG (Note 5)
CK	E	1	1	1	1	0	MUTE TOGGLE (Note 4)
EK	C	0	0	0	0	1	
DK	D	1	0	0	1	1	TOGGLE ON/OF OUTPUT
DJ	EC	0	0	0	0	0	
INVALID (Note 3)		1	1	1	1	1	(Note 3)
	AC	1	0	0	0	1	INCREASE ANALOG (Note 5)
	BC	1	0	0	1	0	DECREASE ANALOG (Note 5)

NOTES:

1. RECEIVER KEYBOARD INPUTS OVERRIDE ANY REMOTE SIGNAL.
2. REST STATE, "DATA VALID" OUTPUT **INACTIVE**
3. ANY SINGLE CLOSURE, INVALID COMBINATION OF 2 CLOSURES, OR COMBINATION OF 3 OR MORE CLOSURES OF S2604 TRANSMITTER INPUTS C, D, E, F,
4. THE MUTE TOGGLE WILL FUNCTION ONLY WHEN THE "ON/OFF" OUTPUT IS **ON.** HOWEVER MUTE IS **CLEARED** BY TURNING "ON/OFF" **OFF,** THEN **ON** AGAIN.
5. THE PULSEWIDTH OF THE ANALOG OUTPUT MAY BE CHANGED ONLY WHEN THE "ON/OFF" OUTPUT IS **ON.**

Electrical Specifications—2604 Encoder— All voltages measured with respect to V_{SS}

Absolute Maximum Ratings

Operating Ambient Temperature T_A ..... 0 to +70°C
Storage Temperature ..... −65°C to +150°C
Positive Voltage on any Pin ..... +14V
Negative Voltage on any Pin ..... −0.3V

Electrical Characteristics: Unless otherwise noted, $V_{DD} = 8.5 \pm 1.5V$ and $T_A = 0$ to +70°C.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f0	Oscillator Frequency	50	320	2000	kHz	
I_{DD}	Supply Current			2	mA	During Transmission, Data Output = 1mA
	Standby			10	μ	No transmission (25°C)
V_{IH}	Input "1" Threshold	20			$\%V_{DD}$	
V_{IL}	Input "0" Threshold			80	$\%V_{DD}$	
I_{LL}	Input Source Current	50		300	μA	$V_I = 0V$
I_{OH}	Output Source Current	1	1.5		mA	$V_O = V_{DD} - 3V$
I_{OL}	Output Sink Current	−.2	−.5		mA	$V_O = +0.5V$

Note: Circuit operates with V_{DD} from 3.0V to 12.0V.

Electrical Specifications—2605 Decoder—All voltages measured with respect to V_{DD}

Absolute Maximum Ratings

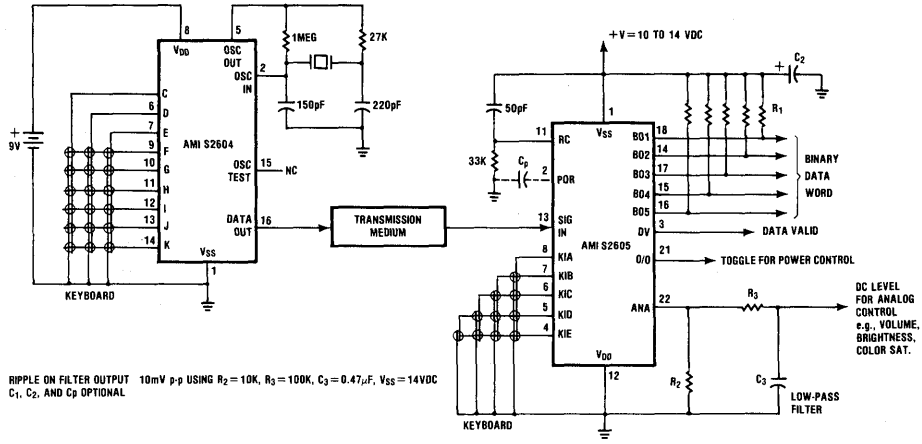
Operating Ambient Temperature T_A ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
V_{SS} Power Supply Voltage ..... +31V
Positive Voltage on any Pin ..... V_{SS} +0.3V
Negative Voltage on any Pin ..... V_{SS} −31V

Electrical Characteristics: Unless otherwise noted, $V_{SS} = 12 \pm 2V$ and $T_A = 0$ to +70°C.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f0	Oscillator Frequency	512	640	768	kHz	
Δf0/f0	Frequency Deviation	−10		+10	%	Fixed R_{OSC}, C_{OSC}, V_{SS}
I_{SS}	Supply Current		34	50	mA	No Loads, $V_{DD} = 14V$
			28		mA	$V_{DD} = 10V$
Signal Input:						
V_{IH}	"1" Threshold			85	$\%V_{SS}$	
V_{IL}	"0" Threshold	30			$\%V_{SS}$	
V_{IH}-V_{IL}	Voltage Hysteresis	5		35	$\%V_{SS}$	
Keyboard and POR Inputs:						
V_{IH}	"1" Voltage	$V_{SS}-.5$	$V_{SS}-3.0$		V	
V_{IL}	"0" Voltage			$V_{SS}-5.5$	V	
I_{LL}	Source Current	50	150	300	μA	$V_I = V_{SS}-10V$
	Debounce Delay (Keyboard Inputs Only)	1.45		2.2	msec	
Binary Outputs (open source):						
I_{OL}	Sink Current	−0.7			mA	$V_O = V_{SS}-5.2V$, $V_{SS} = 16V$
		−0.50	−0.60		mA	$V_O = V_{SS}-5.2V$, $V_{SS} = 10V$
	Duration	34.9			msec	f0 = 704 kHz
Analog Output (open drain):						
ΔV_{step}	Step Voltage Change		$V_{SS}/64$		V	
I_{OH}	Source Current		1.04		mA	$V_O = V_{SS}-0.5V$, $V_{SS} = 10V$
			1.15		mA	$V_O = V_{SS}-0.5V$, $V_{SS} = 14V$
		1.0	1.2		mA	$V_O = V_{SS}-1V$
f_{step}	Analog Step Rate		10		kHz	(f0 ÷ 64)
Data Valid and On/Off Outputs:						
I_{OH}	Source Current	1	1.5		mA	$V_O = V_{SS}-2V$
I_{OL}	Sink Current	−30	−50		μA	$V_O = .7V$
t_r	Risetime (.1 V_{SS} to .9 V_{SS})			10	μsec	$R_L = \infty$, C_L 50pF
t_f	Falltime (.9 V_{SS} to .1 V_{SS})			10	μsec	$R_L = \infty$, C_L 50pF

Note: Circuit operates with V_{SS} from 7.0V to 30.0V

Typical Bench Test Setup, Using a 320kHz Ceramic Resonator with S2604



AMI

A Subsidiary of Gould Inc.

S2743/S2742

ENCODER/DECODER REMOTE CONTROL 2-CHIP SET

CONSUMER PRODUCTS

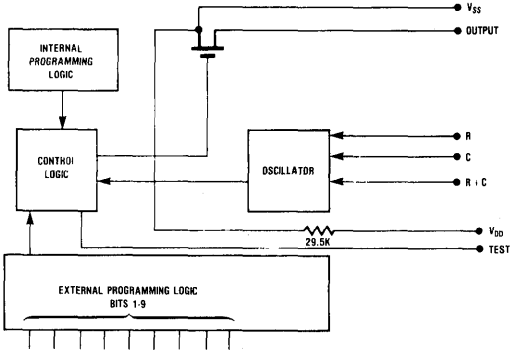
Features

- ☐ RC Oscillator Used—No Crystal Required
- ☐ Phase Locked Loop on Decoder for Reliable Operation
- ☐ 512 User Selectable Address Codes
- ☐ Encoder Operates on a Single Rail 9 Volt Supply — Suitable for Inexpensive and Convenient Battery Operation
- ☐ User can Determine the Type of Transmission Medium to Use

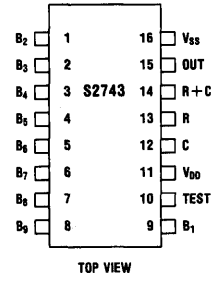
Applications

- ☐ Entry Access Systems
- ☐ Remote Engine Starting for Vehicles and Standby Generators
- ☐ Security Systems
- ☐ Traffic Control
- ☐ Paging Systems
- ☐ Remote Control of Domestic Appliances

Block Diagram 2743 Encoder

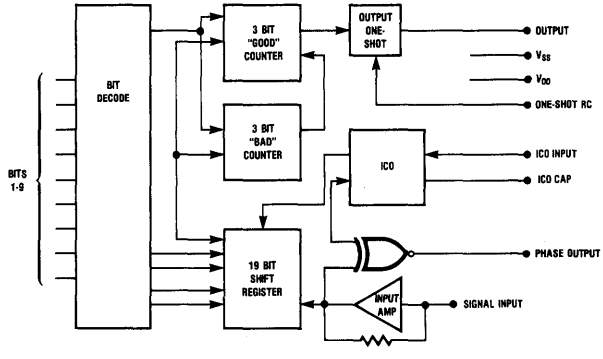


Pin Configuration 2743

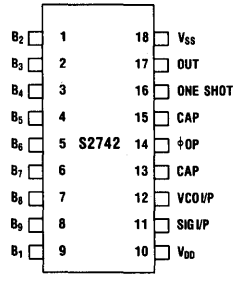


TOP VIEW

Block Diagram 2742 Decoder



Pin Configuration 2742



TOP VIEW

General Description—Encoder/Decoder

This two-chip PMOS set includes a user-programmable serial data encoder for use in a simple low-power transmitter and a serial data decoder for use in a user addressable receiver. The user can select the transmission medium (RF, infrared, or hardwire). The externally selectable message allows up to 512 codes or addresses; this is done with the nine binary inputs on each device. An additional 3 bits of address can be programmed on chip as a fixed preamble.

The serial data encoder encodes by means of a frequency-shift-keyed trinary data pattern composed of 16 data bits. Each data bit will have a length equivalent to 32 cycles of high frequency clock (20kHz typical). Each trinary data pattern will be 512 cycles of 1/2 the oscillator frequency length. The encoder frequency oscillator reference is controlled with an external RC network. The encoder transmitter can be powered by a single 9 volt battery so that a single momentary push button will activate the encoder and transmitter. In the off position there is no current flow.

The serial data decoder in conjunction with a receiver amplifier decodes the transmitted 16-bit coded signal. The on-chip phase-locked-loop locks in on the 20kHz signal even if the transmitted frequency differs from the receiver by up to ± 15%. The coded signal input is compared with the externally selected code. The serial decoder looks at the transmitted signal a minimum of three times before validating a good message. A 3-bit "good" code counter or a 3-bit "bad" code counter accumulates the number of successive good and bad codes being received.

The decoder has an on-chip one-shot which is user programmed by an external RC combination. Whenever three complete good codes are received in the "good" counter a signal enables the one-shot which controls the signal valid output. If a series of three sequential bad codes enter the "bad" code counter the "bad" counter resets the "good" code counter and one-shot period and will not allow an active output until the end of the one-shot period. Any "good" code resets the "bad" code counter. If the "good" counter has accumulated three good codes and activated the output one shot, any occasional "good" code (occurring within the one-shot period) will maintain the output by retriggering the one-shot. The output appears like a single switch, on when "good" codes are received, off when not, with the minimum total period being determined by twice the one-shot period. The one-shot can be used to prevent the output from switching on and off too rapidly due to system noise. The typical RC components shown in the block diagram give a period of about one second.

Functional Description—Serial Data Encoder

The AMI serial data encoder is comprised of three sections: Oscillator, Programming Logic, and Control Logic. Specifically it will provide logical ones "1", logical zeroes "0", and synchronization pulses "S" and arrange them into a trinary data pattern composed of 16 data bits. Each data bit will be 32 cycles of the high frequency (HF-1/2 Oscillator Frequency) in length. Each trinary data pattern will be 512 cycles of 1/2 the Oscillator Frequency length.

A logical "1" is represented by 32 cycles of the high frequency.

A logical "0" is represented by 16 cycles of the high frequency followed directly by 8 cycles of the low frequency (LF = 1/2 HF).

A synchronization pulse "S" is represented by 16 cycles of the low frequency.

A 16-bit data pattern will be encoded in the device in such a manner as to have three (3) bits programmed internally and nine (9) bits programmed externally.

The Oscillator Frequency equals twice that of the High Frequency, and the High Frequency equals twice that of the Low Frequency.

The Oscillator circuit will require a maximum of three (3) external components.

External programming inputs connected to the device $-V_{DD}$ supply will be considered as a logical "1". The bit programming current will not exceed 50μA. The programming resistance should not exceed 1kΩ. Unconnected external bit programming inputs will be considered at a logical "0".

A "1" ($-5V \leqslant$ "1" $\leqslant V_{DD}$) presented to the "Test" input sets the Internal counter and maintains the output of the device "On." The input impedance of the test input is greater than 5MΩ.

For portable operation a 9V transistor battery can be used for the DC voltage supply. Proper circuit polarity must be observed ($-V_{DD}$, $+V_{SS}$).

S2743 Absolute Maximum Ratings

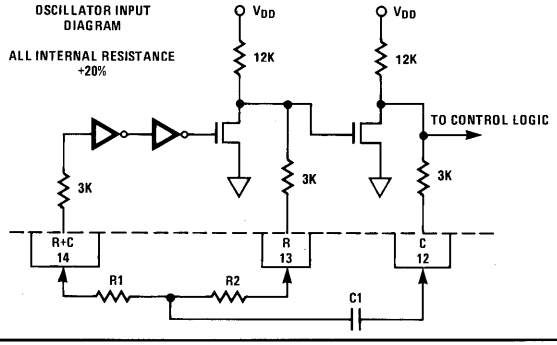
DC Supply Voltage ..... −15V
Input Voltage ..... V_{SS} + .3V to V_{SS} − 15V
Operating Temperature Range ..... −40°C to +100°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (During Soldering) ..... 300°C for Max. 10sec.

S2743 Electrical Characteristics (25°C Air Temperature Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Operating Supply Voltage	−6.65	−9.5	−15	V	V_{DD}; V_{SS} = 0V
	Operating Power Dissipation		27	40	MW	−8V, −5mA, Max.
	Operating Frequency	2	40	60	kHz	Oscillator
	Programming Bits 1-9, Current			50	μA	Programming Input, R 1kΩ
	External Programming Resistance			1	kΩ	Bits 1-9
	(DC Bits 1-9) Program Logical "1"	V_{SS} − 5V		V_{DD}	V	
	Input Levels Logical "0"	V_{SS} − 1V		V_{SS}	V	
	Bits 1-9 Current		55		μA	Input R 9V>1.5M @ 5V
	Test and R + C Input Impedance	5		75	MΩ	
	(DC) Test Input Levels Test ON	V_{SS} − 5V		V_{DD}	V	Maintains Output Device ON
	Test OFF (See Note 1)	V_{SS} − 1V		V_{SS}	V	Permits Normal Operation
	R, C Resistance Logical "1"		12		kΩ	Resistance to V_{DD}, ± 20%
	R, C Resistance Logical "0" (See Figure 1)		3		kΩ	Resistance to V_{SS} + 20% − 30%
	Output Current (See Note 2)	5			mA	Output Voltage = .8V W/V_{DD} = −7V

Notes: 1. Effect noted at Pin 15 to V_{SS}. 2. Output Voltage Pin 15 to V_{SS}. 3. All Voltages measured with respect to V_{SS}.

Figure 1. Serial Data Encoder



CONSUMER PRODUCTS

A Subsidiary of Gould Inc.

S2747/S2748

ENCODER/DECODER REMOTE CONTROL 2-CHIP SET

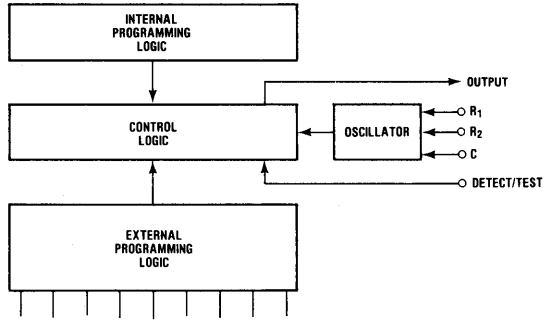
Features

- ☐ RC Oscillator Used—No Crystal Required
- ☐ 512 User Selectable Address Codes
- ☐ Low Power CMOS Encoder Operates on a Single Rail 9 Volt Supply
- ☐ Low Power CMOS Decoder Operates on a Single Rail 12 Volt Supply

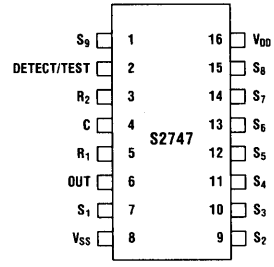
Applications

- ☐ Entry Access Systems
- ☐ Remote Engine Starting for Vehicles and Standby Generators
- ☐ Security Systems
- ☐ Traffic Control
- ☐ Paging Systems
- ☐ Remote Control of Domestic Appliances

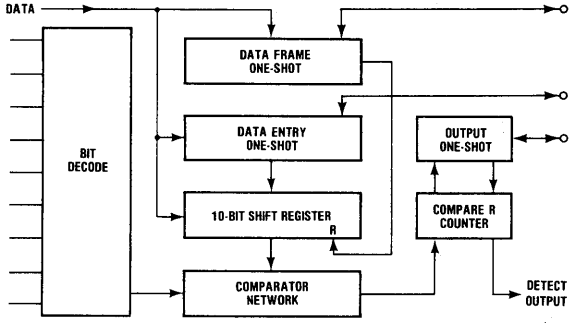
Block Diagram 2747 Encoder



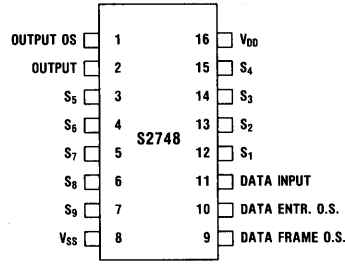
Pin Configuration 2747



Block Diagram 2748 Decoder



Pin Configuration 2748



General Description—Encoder/Decoder

This two-chip CMOS set includes a user-addressable serial data encoder for use in a simple low-power transmitter and a serial data decoder for use in a user-addressable low-power receiver. This chip set may be used with a variety of transmission media (RF, infrared, or hardwire). Up to 512 codes or addresses are externally selectable; this is done with the nine binary inputs on each device.

The serial data encoder outputs a train of ten pulses. The first pulse is a "marker" bit used to signal the decoder that a message is coming. The following nine pulses represent the encoded nine bits of binary information. The duration of the pulses output from the encoder is determined by a simple RC clock network. The encoder transmitter can be powered by a single 9-volt battery so that a single momentary push button will activate the encoder and transmitter. In the off position, there is no current flow.

The serial data decoder, in conjunction with a receiver amplifier, decodes the transmitted signal. The coded signal input is compared with the decoder's externally selected address. The serial decoder looks at the transmitted signal a minimum of four times before validating a good message and turning the receiver's detection output on.

The decoder has an on-chip output one-shot which is user programmed by an external RC combination. This one-shot is used to prevent the detection output from switching on and off too rapidly due to system noise.

Functional Description—Serial Data Encoder

The Serial Data Encoder is comprised of three sections: Oscillator, Programming Logic, and Control Logic. Specifically, it will provide a marker pulse and nine data pulses. This 10-bit message will be output from the encoder, then a DC logic "0" pulse will be output for a time corresponding to the length of the 10-bit message.

The encoder will continue to cycle the message and the logic "0" silence period as long as power is applied to it.

Each bit of the 10-bit message is four RC oscillator periods wide. The format of each bit is the same. First, a Logic "1" is output for one oscillator period. Then, the data (or marker) value is output for the next two oscillator periods. Lastly, a logic "0" is output for one oscillator period. Thus, Logic "1" for one period, data for two periods, and Logic "0" for the last period. After a 10-bit message (40 oscillator periods) has elapsed, there will be an equivalent period of silence (Logic "0") output from the encoder, as mentioned previously.

The marker bit is equivalent to a data bit with a value of Logic "1".

The RC oscillator circuit requires a maximum of three external components (see Figure 1). To directly drive the oscillator, let encoder Pins 3 and 4 float, and apply the direct drive signal to encoder Pin 5.

The typical R_1, R_2, and C components shown in Figure 2 provide an oscillator frequently of about 1ms.

External programming inputs connected to the device will be considered as a Logic "0". Unconnected external bit programming inputs are pulled up by the chip to a Logic "1".

A Logic "1" applied to "test detect", Pin 2, resets the internal logic and forces the encoder output to a Logic "0". After the "test detect" pin is back at a Logic "0", the encoder output will be a Logic "0" for 40 RC oscillator clock periods, then the 10-bit message will begin.

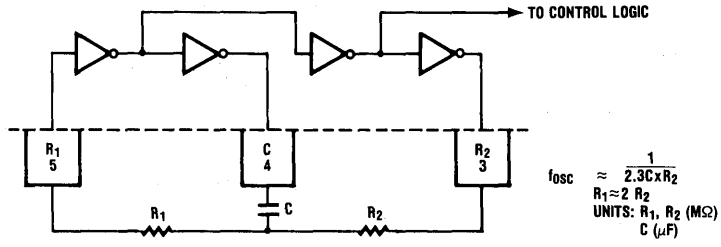
For portable operation, a 9V transistor battery with a 6V zener diode may be used for the DC voltage supply.

Functional Description—Serial Data Decoder

The Serial Data Decoder is comprised of four sections: Data Entry One-Shot, 9-Bit Digital Comparator, Good Detection Control Logic, and the Retriggerable Output One-Shot.

The Decoder is always on, looking for a "marker" pulse from the encoder. When a pulse is detected at the data input, the data entry one-shot clocks it into the first stage of a 10-bit shift register, after a user-selectable delay. As successive pulses are detected, they are similarly shifted into the shift register, with preceding shift register information shifted over one bit. As the marker bit is shifted into the tenth bit of the shift register, a comparison is made with the first nine bits of shift register information and the nine externally programmed address inputs. If a comparison is valid, a clock pulse is sent to the good detection counter logic. As mentioned in the Encoder Functional Description, a message lasts 40 encoder oscillator clock periods followed by 40 encoder oscillator clock periods of DC Logic "0". In the Decoder, it is necessary to clear the 10-bit shift register and associated logic after the message has been received and compared with the Decoder's external address bits. This is done using the

Figure 1. Serial Data Encoder RC Oscillator



data frame one-shot. The data frame one-shot provides a user-selectable delay from the end of a message until the shift register is reset. The typical RC components shown in Figure 2 provide data frame one-shot pulse width of about 10mS, while the components for the data entry one-shot will generate a 2ms pulse width clock delay during data entry.

The good detection counter circuit and the retriggerable output one-shot work together. Initially, as data begins to enter the Decoder, the output one-shot is refreshed to a Logic "1"; the detect output is off. As the output one-shot decays toward a Logic "0", the initial message is compared with the nine external address bits. If the comparison is true, a clock will increment the good detection control circuit. If four such comparisons occur, the detect output will turn on and the output one-shot will again be refreshed to a Logic "1". If less than four comparisons occur before the output one-shot decays to a Logic "0", the detect output will remain off, the output one-shot will not be refreshed to a Logic "1", and the good detection counter circuit will be reset. Once the detect output is turned on by four message detections in a single output one-shot period, it requires only one message detection per output one-shot period thereafter to keep the detect output continuously turned on. If no message detection occurs in a subsequent output one-shot period, the one-shot will decay to a Logic "0", turn off the detect output and reset the good detection counter circuit. The typical RC components shown in Figure 2 give an output one-shot period of about one second.

Also note that a logic inversion must take place external to the output of the Encoder before it is presented to the data input of the Decoder. Figure 2 shows a typical circuit to accomplish this.

S2747 Encoder Absolute Maximum Ratings

DC Supply Voltage	$V_{DD} = +9V$, $V_{SS} = 0V$
Input Voltage	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range (Ambient)	$-35°C$ to $+85°C$
Storage Temperature Range (Ambient)	$-55°C$ to $+150°C$
Lead Temperature (During Soldering)	300°C for Max. 10 sec.

AMI

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S10110**

ANALOG SHIFT REGISTER

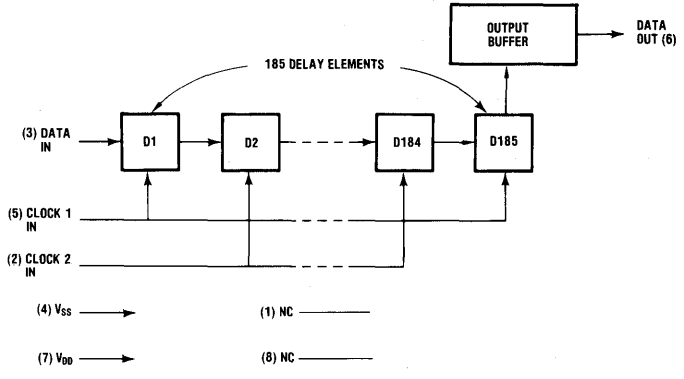
Features

- ☐ 185 Stage "Bucket Brigade" Delay Line
- ☐ Delays Audio Signals
- ☐ Accepts Clock inputs up to 500kHz
- ☐ Variable Delay
- ☐ Alternate to TCA 350

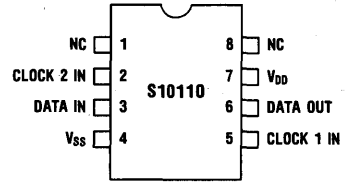
General Description

The S10110 analog shift register is a monolithic circuit fabricated with P-Channel ion-implanted MOS technology. The part differs from a digital shift register, which is capable of only digital input and output information, in that an audio signal is typically supplied as the data input to the analog register, and the output is the same audio signal delayed in time. The amount of signal delay is dependent on the number of bits of delay (185) and the frequency of the two symmetrical clock inputs. Since each negative-going clock edge transfers data from one stage to the next, the analog signal delay equals 185 ÷ 2 × clock frequency.

Block Diagram



Pin Configuration



Operation

Device operation may be understood by referring to Figure 1. This is an actual schematic diagram of the analog shift register, or "bucket brigade," showing typical external bias techniques.

Data In Input:

The analog signal, or audio signal, to be delayed is applied to pin 3. This input must be biased to a negative voltage of approximately – 8 volts, and two resistors may be used as a voltage divider to provide this bias. They must be chosen so that $(R_1) \pm (R_2) \div (R_1 + R_2)$ is less than 20kΩ. The input signal applied to this input through series capacitor C_{IN} may be as high as 6 volts peak-to-peak.

Clock 1 and Clock 2 Inputs:

Applied respectively to pins 5 and 2, Clock 1 and Clock 2 are two symmetrical non-overlapping negative-going clocks used to transfer the analog data along the 185 bit delay line. Although these clocks may have a duty cycle as low as 25% (i.e., each clock signal is at a negative level for 25% of its period), better output signals will be obtained with both clock duty cycles closer to 50%. It is important, however, that no overlap of the clock signals occurs at a level more negative than V_{SS} – 0.8 volts.

Referring again to Figure 1, it can be seen that when Clock 1 is negative, data is transferred from the data input to capacitor C1; likewise, data is transferred from each even-numbered capacitor to the capacitor to its right. When Clock 2 is negative, data is transferred from C1 to C2 and from each other odd-numbered capacitor to the capacitor to its right. In this manner, data is shifted from the input to C185 after a total of 185 negative clock pulses has occurred (i.e., 93 periods of Clock 1 and 92 periods of Clock 2).

Data Out Output:

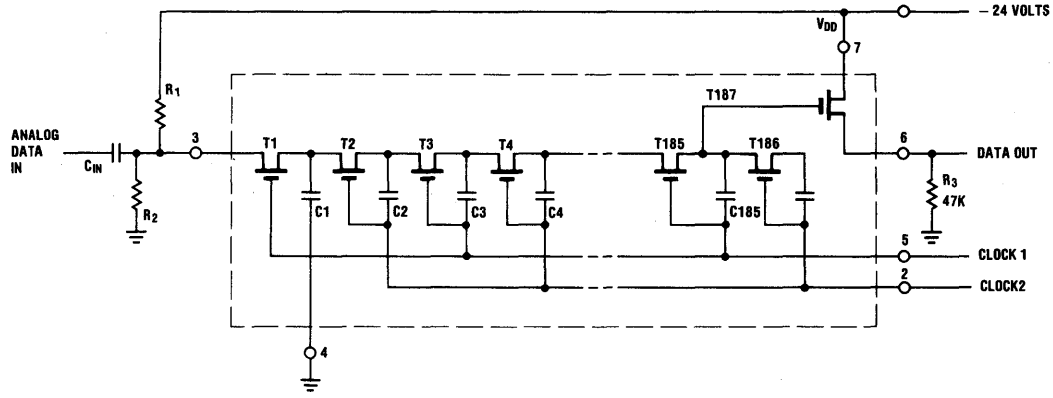
The output of the S10110 analog shift register is a single device, T187, with its drain at V_{DD} and its source connected to pin 6. If a 47K resistor to V_{SS} is supplied at this pin, T187 functions as a source follower.

Referring to Figure 3, it can be seen that the output potential during Clock 2 is a constant value near – 10 volts. When Clock 1 switches on (negative), the output instantaneously drops to a level of approximately – 30 volts; this is caused by the 20 volt swing of Clock 1 and C185. As Clock 1 remains on, device T185 transfers charge from C184 to C185, and the output voltage becomes more positive, depending on the charge previously stored on C184. It is during this part of Clock 1 that the output reflects the analog data stored on C1 185 bits earlier. Since the clock signal now appears on the output, it is necessary to apply the appropriate filtering to obtain the delayed analog signal.

Applications

- ☐ Delay of Audio Signals
- ☐ Rotating Speaker Simulation
- ☐ Electronic Chorus
- ☐ Electronic Vibrato
- ☐ String Ensemble
- ☐ Reverberation

Figure 1. Schematic Diagram and Pinouts of S10110



Absolute Maximum Ratings

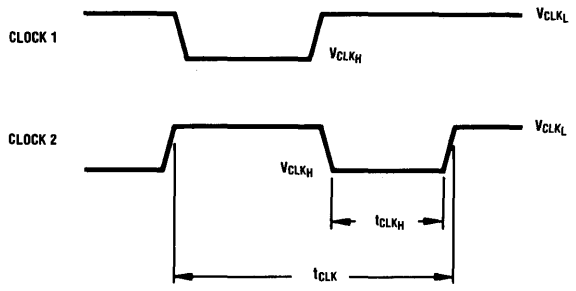
Voltage on any pin relative to V_{SS} ..... + 0.3V to − 30V
Operating temperature range ..... 0°C to + 70°C
Storage temperature (ambient) ..... − 65°C to + 150°C

Electrical Characteristics

(0°C<T_A<70°C; V_{DD} = − 24V ± 2V; V_{SS} = 0V)

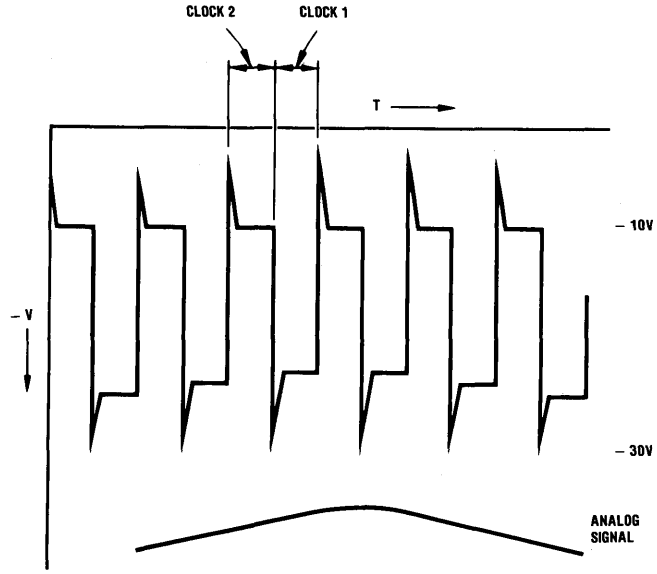
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{CLK_L}	CLOCK 1 and CLOCK 2 Inputs Logic Level "0"	V_{SS}		$V_{SS}-0.8$	V	No Overlap of Signals More Negative than $V_{SS}-0.8V$
V_{CLK_H}	CLOCK 1 and CLOCK 2 Inputs Logic Level "1"	− 18		− 20	V	See Figure 2
t_{CLK_H}	Duration of CLOCK Logic "1" Level	$0.2\times t_{CLK}$				See Figure 2
f_{CLK}	CLOCK Input Frequency	5		500	kHz	
V_{BIN}	Input Bias Voltage	− 7.5		− 8.5	V	See Figure 1
R_{BIN}	Resistance of the Bias Voltage Source at Input			20	KΩ	$R_{BIN}=(R1)\times(R2)\div(R1+R2)$ See Figure 1
V_{DIN}	Signal Level at Data In Input			6	V (P-P)	
a	Analog Signal Attenuation			4	dB	
t_D	Signal Delay		$\frac{185}{2\times f_{CLK}}$			
f_{3dB}	2dB Response Point		$0.1\times f_{CLK}$			

Figure 1. Timing Diagram of Clock 1 and Clock 2 Signals



CONSUMER PRODUCTS

Figure 3. S10110 Output Waveform



AMI®

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S10430**

DIVIDER-KEYER

Features

- ☐ 22 Keyboard Inputs
- ☐ 88 DC Keyer Circuits
- ☐ 34 Binary Dividers
- ☐ Provides Four Pitch Outputs
- ☐ All Key Inputs Sustainable for Percussion
- ☐ All Dividers Resettable
- ☐ Provides "Any Key Down" Indication
- ☐ Eliminates Multiple-Contact Key Switches

Typical Applications

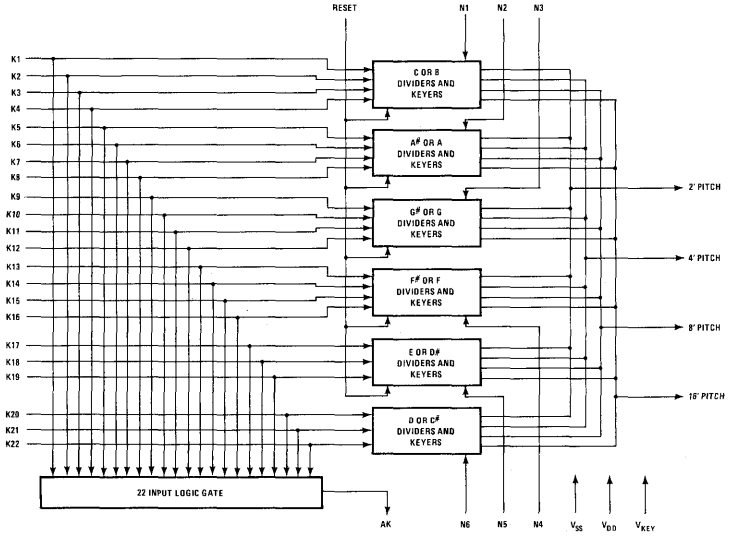
- ☐ Generation and Keying of Musical Tones
- ☐ Standard Spinet Organ Keying (37 or 44 note keyboards)
- ☐ Keying of Sustained Tones
- ☐ Percussive Effects
- ☐ Generating Stair-stepped Waveforms
- ☐ Electronic Piano

General Description

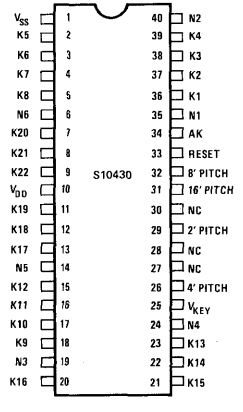
The S10430 divider-keyer is a monolithic integrated circuit fabricated with P-Channel ion-implanted MOS technology. It is intended for use in spinet organs or other electronic musical instruments having keyboards of up to 44 keys. This device has 22 key inputs, allowing all keying functions for a 44 note manual to be performed by two S10430 circuits. Each S10430 accepts six frequencies from a top octave synthesizer, such as an S50240, and provides squarewave outputs at 16 foot, 8 foot, 4 foot, and 2 foot pitches. For example, if a C key is depressed by itself a low C frequency appears at the 16 foot output, and a C frequency one octave higher appears at the 8 foot output; similarly, the 4 foot and 2 foot outputs provide C frequencies one and two octaves higher, respectively, than the C frequency of the 8 foot output. All appropriate frequency division is performed by the S10430, eliminating the need for external dividers.

CONSUMER PRODUCTS

Block Diagram



Pin Configuration



General Description (Continued)

The circuit also eliminates the need for multiple-contact key switches and discrete diode or transistor keyers. Because of the high input impedance of the MOS keyers used in this circuit, long sustain envelopes may be obtained by connecting low-value capacitors to the keying inputs.

Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS}	+ 0.3V to − 27.0V
Operating Temperature (ambient)	0°C to 70°C
Storage Temperature	− 65°C to 150°C

Electrical Characteristics

0°C≤T_A≤70°C; V_{SS} = 0V; V_{DD} = − 12.6V to − 15.4V; V_{KEY} = − 4.75V to − 5.25V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IL}	Logic Low Level TOS and Reset Inputs	0.0		0.8	V	
V_{IH}	Logic High Level TOS and Reset Inputs	− 4.2		V_{DD}	V	
t_r, t_f	Rise and Fall Times TOS Inputs			50	μsec	Measured between 10% and 90% points
V_{OL}	Logic Low Level AK Output		− 0.5	− 1.0	V	100KΩload to V_{DD}
t_{fo}	Transition of AK Output to 10% of V_{DD}			10	μs	100pF and 100KΩload to V_{DD}
F_T	Operating Frequency TOS Inputs	DC		50K	Hz	
D_O	Output Duty Factor	48		52	%	Measured between 10% and 90% points
I_{PA}	Peak Output Current Absolute (any pitch output with 1 keyer on)	350		650	μA	V_{DD} = − 14V V_{KEY} = − 5V V_{EN} = − 25V T_A = 25°C
I_P	Peak Output Current	85		115	$\%I_{AVE}$*	V_{DD} = − 14V V_{KEY} = − 5V V_{EN} = − 25V T_A = 25°C
I_P	Peak Output Current	50		75	$\%I_{AVE}$*	V_{DD} = − 14V V_{KEY} = − 5V V_{EN} = − 15V T_A = 25°C
I_P	Peak Output Current	0.5			μA	V_{DD} = − 14V V_{KEY} = − 5V V_{EN} = − 3.0V T_A = 25°C
I_P	Peak Output Current			0.5	μA	V_{DD} = − 14V V_{KEY} = − 5V V_{EN} = − 1.0V T_A = 25°C

*I_{AVE} is the average of all peak output current values within one circuit.

Functional Description

The S10430 Divider-Keyer circuit accepts six frequencies as inputs and uses these to clock six binary divider chains. Four of these chains consist of six binary dividers each and the remaining two have five. The six chains generate all frequencies necessary to obtain 2', 4', 8', and 16' pitches for half of a 44 key keyboard.

The outputs of the divider chains are routed to chopper keyer circuits like the one shown in figure 2. When a negative voltage is applied to any "K" input, four of these keyer circuits are turned on to route the appropriate frequencies to each of the four pitch outputs.

Figure 1:
Typical Time Constants For Sustain Keying

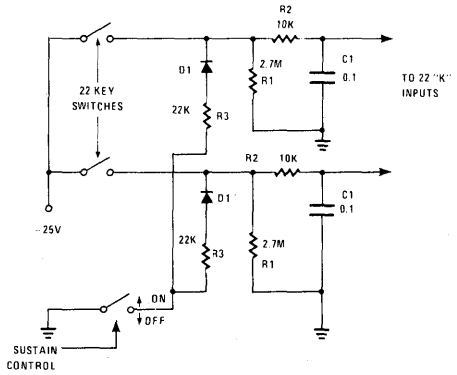
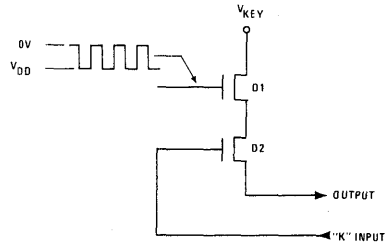


Figure 2:
Schematic Diagram of Chopper Keyer Circuit



N Inputs

Six of the twelve tempered scale frequencies are applied to the inputs N1 through N6. Typically, these frequencies would be six of the outputs of a top octave synthesizer, such as an S50240. In general, it doesn't matter which frequencies are applied to the N inputs, although this affects which keyboard keys should be connected to the K inputs. One exception to this arises from the fact that a 44 note keyboard contains more of some keys than others. Specifically, there are only three each of the keys, C#, D, D#, and E, but there are four each of the keys F, F#, G, G#, A, A#, and C. This results in the requirement that each of the two S10430 divider keyers in a system take two frequencies from the first group, and four from the second group. Stating this another way, the N1, N2, N3, and N4 inputs must have frequencies chosen from the group, F, F#, G, G#, A, A#, B, and C. The N5 and N6 inputs are chosen from the group, C#, D, D#, and E. The example in Figure 4 shows one divider keyer handling the notes, A, A#, B, C, C#, and D while the other does the keying for D#, E, F, F#, G, and G#.

Table 1: Relationship between K and N Inputs

INPUT	PIN NO.	OUTPUT (8′ PITCH)* PIN 32	INPUT	PIN NO.	OUTPUT (8′ PITCH)* PIN 32
K1	36	N1÷4	K12	15	N3÷32
K2	37	N1÷8	K13	23	N4÷4
K3	38	N1÷16	K14	22	N4÷8
K4	39	N1÷32	K15	21	N4÷16
K5	2	N2÷4	K16	20	N4÷32
K6	3	N2÷8	K17	13	N5÷4
K7	4	N2÷16	K18	12	N5÷8
K8	5	N2÷32	K19	11	N5÷16
K9	18	N3÷4	K20	7	N6÷4
K10	17	N3÷8	K21	8	N6÷8
K11	16	N3÷16	K22	9	N6÷16

*To determine outputs for 4′ pitch: multiply 8′ pitch output by 2.
To determine outputs for 2′ pitch: multiply 8′ pitch output by 4.
To determine outputs for 16′ pitch: multiply 8′ pitch output by

K Inputs

The twenty-two inputs are connected either directly to key switches or to an attack/decay circuit, such as the one shown in Figure 1. When a negative voltage is applied to any K input, four chopper keyer circuits are turned on, and the appropriate frequencies appear at the four pitch outputs. The amount of current at the output is determined by the voltage at the K input. As the voltage becomes more negative, more current appears at the output. This will be discussed further in the section on "Pitch Outputs."

Connection of the K inputs to the key switches is dependent on which frequencies are applied to which N inputs. Table 1 shows the relationship between the K and N inputs. If, for example, the top octave frequency F, 5588 Hz, is applied to the N2 input, K5 should then be connected to the highest F key on the keyboard, K6 to the next highest, K7 to the next, and K8 to the lowest F. If the highest F key is depressed, then N2÷4, or 1397 Hz would appear at the 8′ Pitch Output. At the same time, the 16′ pitch, 4′ pitch and 2′ pitch outputs would provide, respectively, 699 Hz, 2794 Hz, and 5588 Hz. An example of K and N input connections is given in Figure 4.

To control attack, decay, and sustain times, a circuit such as the one shown in Figure 1 may be used. When a keyswitch is closed, the K input charges to −25 volts through the time constant of R2 and C1. This causes the attack time to be about 1ms. If the sustain is on (sustain switch open), when the keyswitch is opened, the K input will charge slowly back to V_{SS} through the time constant of C1, R1, and R2. This results in a sustain envelope of 271ms. Longer sustains can be obtained with larger capacitors. If the sustain switch is closed, then the decay time is governed by the time constant of C1, R2, and R3 || R1. In this example, this non-sustain decay is about 3ms.

Pitch Outputs

The outputs labeled 2′ pitch, 4′ pitch, 8′ pitch, and 16′ pitch provide the appropriate frequencies for these four pitches depending on which K inputs have been selected. The selected frequencies of the outputs are shown in Table 1. The highest octave of frequencies is obtained directly from the N inputs. Although these top octave frequencies are buffered internally, their duty cycle depends on the duty cycle of the N inputs.

Each output is connected to the outputs of 22 of the chopper keyer circuits shown in Figure 2. The chopper device, D1, is much lower in impedance than the keyer device D2. The output voltage amplitude is dependent, therefore, on the ratio of D2 to the output load. Higher output sink resistor values result in higher output signal amplitudes. However, it is important to keep the output sink resistor low in order to minimize the effects of intermodulation distortion between keyers. Figure 3 shows a typical output waveform with a 100 sink resistor. Because of the need for a low value sink

resistor and the usual desirability of a high signal amplitude, it may be advisable in some cases to load the pitch outputs with operational amplifiers instead of resistors.

V_{KEY} Input

This supply input is used exclusively for the chopper keyer circuits (Figure 2). It is important that this be a low impedance supply in order to minimize intermodulation distortion between keyer circuits.

The voltage on the supply is kept low relative to V_{DD} and the K inputs to insure linear operation of the MOS keying circuits.

Reset Input

Applying a V_{SS} level to this input causes all binary dividers to be held in the reset state. A logic 1 applied to Reset causes the dividers to function normally. To prevent possible phase cancellation between upper and lower manual systems, it is suggested that an RC network be connected to this input so that the musical instrument will be locked into proper phase relationships when power is first applied. When in the reset condition, all chopper devices are turned on to facilitate testing.

AK Output

Whenever any key input is selected, the AK output is actively pulled to V_{SS} to indicated that a key is played. This output is open ended (i.e., no pull-up device is provided), and may be left unconnected if not needed.

Figure 3: Typical Keyer Output

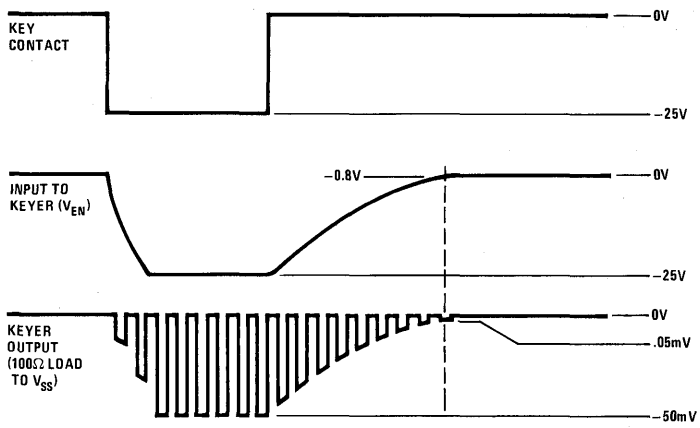
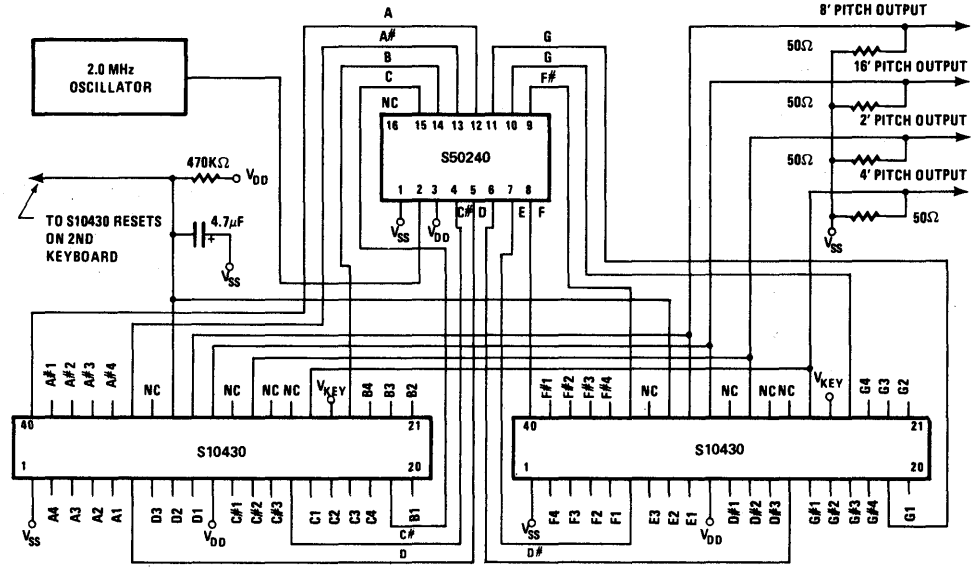


Figure 4: Schematic Diagram of Typical Divider—Keyer Application



NOTE: ON ALL K INPUTS, THE LETTER REFERS TO THE KEY NAME, AND THE NUMBER TO ITS LOCATION ON THE KEYBOARD. FOR EXAMPLE, F1 WOULD BE THE LOWEST KEY ON A 44 NOTE MANUAL, AND C4 WOULD BE THE HIGHEST.

AMI

A Subsidiary of Gould Inc.

S2688

June 1978

DIGITAL NOISE GENERATOR

CONSUMER PRODUCTS

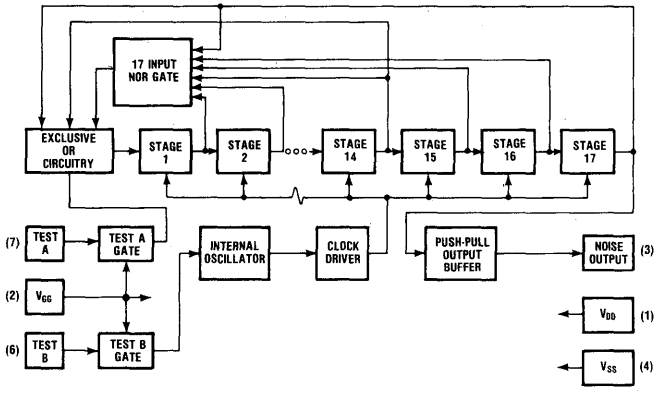
Features

- ☐ Internal Oscillator
- ☐ Consistent Noise Quality
- ☐ Consistent Noise Amplitude
- ☐ Zero State Lockup Prevention
- ☐ Zeros Can Be Externally Forced Into the Register
- ☐ Oscillator Can Be Driven Externally
- ☐ Operates With Single or Dual Power Supplies
- ☐ Eliminates Noise Preamps
- ☐ Alternate to MM5837

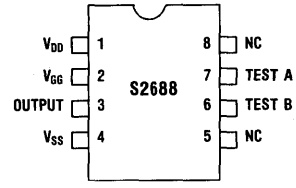
General Description

The S2688 noise generator circuit is fabricated in P-Channel Ion implanted MOS technology and supplied in an eight-lead dual in-line plastic package. The device contains a 17-bit shift register which is continuously clocked by an internal oscillator. Exclusive OR feedback from the 14th and 17th stages causes the register to generate a pseudo-random noise pattern, and an internal gate is included to prevent the register from reaching an all zero lockup state. To facilitate testing, the device can be easily clocked by an external source.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Positive Voltage On Any Pin ..... V_{SS} + 0.3V
Negative Voltage On Any Pin Except V_{GG} ..... V_{SS} − 28V
Negative Voltage On V_{GG} Supply Pin ..... V_{SS} − 33V
Storage Temperature ..... − 65°C to + 150°C
Operating Ambient Temperature ..... 0°C to + 70°C

Electrical Specifications (0°C<T_A<70°C; V_{SS} = 0 Volts; V_{DD} = − 14.0V ± 1.0V; V_{GG} = 27.0V ± 2V; unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output Logic 1 Level	V_{SS} − 1.5		V_{SS}	Volts	20KΩ Load to V_{DD}
V_{OL}	Output Logic 0 Level	V_{DD}		V_{DD} + 1.5	Volts	20KΩ Load to V_{SS}
V_{OL}	Output Logic 0 Level	V_{DD}		V_{DD} + 3.5	Volts	20KΩ Load to V_{SS} $V_{GG} = V_{DD} = -14V \pm 1.0V$
Z_{IN}	Input Impedance (Test Inputs)		10		pF	
I_L	Leakage Current (Test Inputs)			500	nA	
f_o	Frequency of Internal Oscillator		100		kHz	
I_{DD}	V_{DD} Supply Current			4.0	mA	No Output Load
I_{GG}	V_{GG} Supply Current			500	μA	
f_{TEST}	Test Frequency	80		105	kHz	

Operation

The S2688 is a 17-bit digital shift register driven by an internal oscillator circuit. Outputs from the 14th and 17th stages are connected to an Exclusive OR circuit whose output provides the data input for the register. The 17th stage of the register is connected to a push-pull buffer, which is the circuit's output. This output provides continuous constant amplitude pseudo-random noise; that is, for any time slot, ones and zeroes have an almost equal probability of occurrence.

Typical Applications

- ☐ Percussion Instrument Voice Generators for Rhythm Units
- ☐ Electronic Music Synthesizers
- ☐ Simulated Pipe "Wind" Noise
- ☐ Acoustics Testing

Power Supplies

The S2688 noise generator may be operated with either one or two power supplies. In applications where a high output drive level is not critical, or where the output is loaded with a resistive load connected to V_{DD}, it is possible to operate the device from a single supply voltage; in this case, the V_{GG} supply pin is connected to the V_{DD} supply voltage. If a low impedance logic "0" level output is required, this can be achieved by connecting the V_{GG} supply pin to a more negative voltage.

Zero State Lockup Prevention

If the outputs of all 17 stages of the shift register were simultaneously to reach a "0" logic level, and no logic were provided to prevent this state from occurring, then the register would remain in the "all-zero" state.

In this condition, the output would lockup and remain at a logic "0" level. This situation could occur when power is initially applied, or when triggered by noise spikes. To prevent this condition, a 17 input NOR gate is provided internally to decode the "all-zero" state and feed a logic "1" level into the register's data input.

Test Inputs

The S2688 has been designed to facilitate testing of the part. In the normal mode of operation, pins 6 and 7 are not used and appear to be open circuits. However, when the V_{GG} pin is connected to V_{SS}, these pins become test pins. Pin 7 (Test A) is used to force zeroes into the register, and pin 6 (Test B) becomes the clock input, driving the internal oscillator network. During the entire test period a 20KΩ load must be tied to V_{DD}.

AMI

A Subsidiary of Gould Inc.

S50240/S50241/S50242

TOP OCTAVE SYNTHESIZER

Features

- ☐ Single Power Supply
- ☐ Broad Supply Voltage Operating Range
- ☐ Low Power Dissipation
- ☐ High Output Drive Capability
- ☐ S50240 — 50% Output Duty Cycle
- ☐ S50241 — 30% Output Duty Cycle
- ☐ S50242 — 50% Output Duty Cycle

General Description

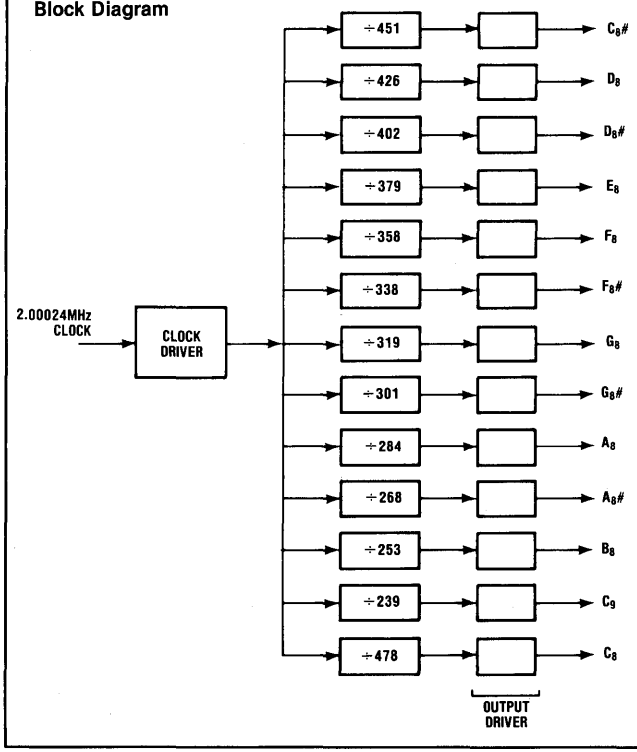
The S5024 is one of a family of ion-implanted, P-Channel MOS, synchronous frequency dividers.

Each output frequency is related to the others by a multiple $12\sqrt{2}$ providing a full octave plus one note on the equal tempered scale.

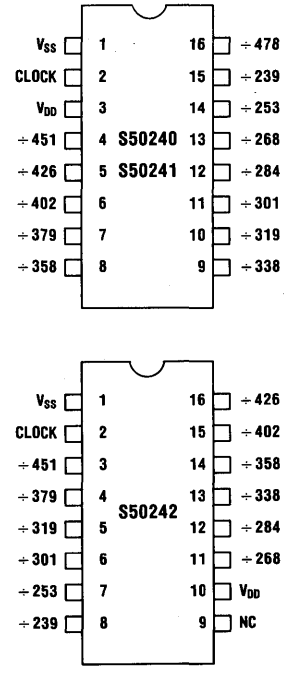
Low threshold voltage enhancement-mode, as well as depletion mode devices, are fabricated on the same chip allowing the S5024 family to operate from a single, wide tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 360mW of power. The circuits are packaged in 16-pin plastic dual-in-line packages.

CONSUMER PRODUCTS

Block Diagram



Pin Connections



RFI emination and feed-through are minimized by placing the input clock between the V_{DD} and V_{SS} pins. Internally the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise time under no load conditions to reduce the R.F. harmonic content of each output signal.

Absolute Maximum Ratings

Voltage On Any Pin Relative to V_{SS} ..... +0.3V to −20V
Operating Temperature (Ambient) ..... 0°C to 50°C
Storage Temperature (Ambient) ..... −65°C to +150°C

Recommended Operating Conditions ($0°C \leq T_A \leq 50°C$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Figure
V_{SS}	Supply Voltage	0		0	V	
V_{DD}	Supply Voltage	−11.0	−14.0	−16.0	V	

Electrical Characteristics ($0°C \leq T_A \leq 50°C$; V_{DD} = −11 to −16V unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Figure
V_{IL}	Input Clock, Low	0		−1.0	V	Figure 1
V_{IH}	Input Clock, High	−10.0		V_{DD}	V	Figure 1
f_I	Input Clock Frequency	100	2000.240	2500	kHz	
t_r, t_f	Input Clock Rise and Fall Times 10% to 90% @ 2.5MHz			50	nsec	Figure 1
t_{ON}, t_{OFF}	Input Clock On and Off times @ 2.5MHz		200		nsec	Figure 1
C_I	Input Capacitance		5	10	pF	
V_{OH}	Output, High @ 1.0mA	V_{DD} +1.5		V_{DD}	V	Figure 2
V_{OL}	Output, Low @ 1.0mA	V_{SS} −1.0		V_{SS}	V	Figure 2
t_{ro}, t_{fo}	Output Rise and Fall Times, 500pF Load 10% to 90%	250		2500	nsec	Figure 3
t_{ON}	Output Duty Cycle—S50240, S50242 S50241		50 30		% %	
I_{DD}	Supply Current		14	22	mA	Outputs Unloaded

Figure 1. Input Clock Waveform

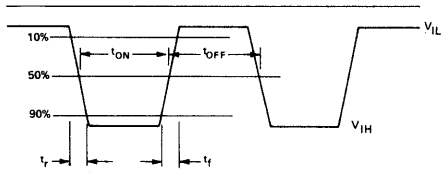


Figure 2. Output Signal DC Loading

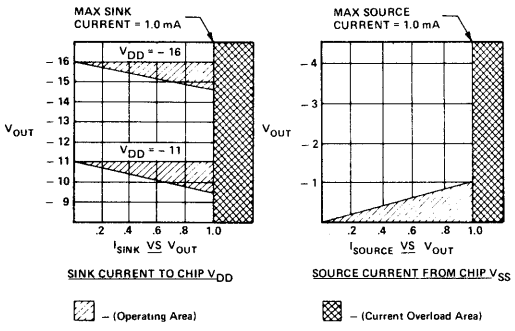
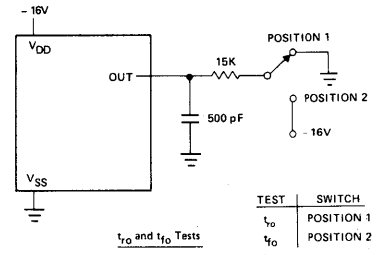
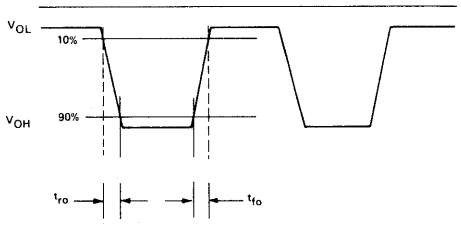


Figure 3. Output Rise and Fall Times





CONSUMER PRODUCTS

A Subsidiary of Gould Inc.

S4003

AUTO CLOCK

Features

- ☐ 12 Hour, 4 Digit Auto Clock
- ☐ Elapsed Time Counter (resettable, range to 99 hours)
- ☐ Calendar (4-year calendar with pin option for European date/month reversal)
- ☐ Ignition-Sensing Display Cut-off (to reduce battery drain when the auto is not operating)
- ☐ Crystal Input Accuracy (uses inexpensive 4.194mHz crystal)
- ☐ Direct Display Drive (4-digit vacuum fluorescent displays, 24 Volts)

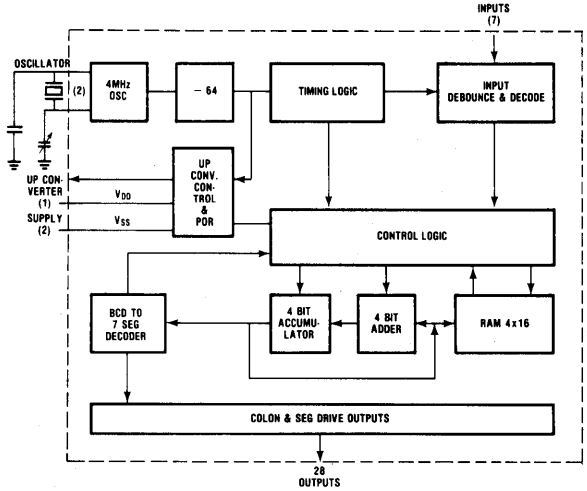
Applications/Markets

- ☐ Automotive
- ☐ Avionics
- ☐ Marine
- ☐ Portable Clocks
- ☐ Industrial

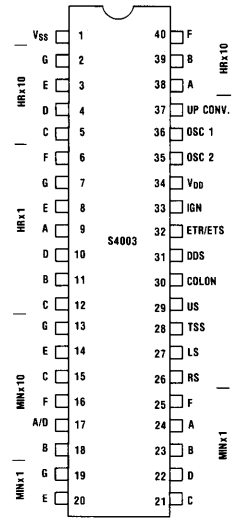
General Description

The S4003 Auto Clock is a PMOS integrated circuit which has found wide application in auto, avionic and marine applications as a portable or dashboard clock and as an industrial timer.

Block Diagram



Pin Configuration



A functional description of the inputs/outputs and registers follows:

1. **Set Inputs**—Left digits set and right digits set will index the selected register at a 2Hz rate. Indexing either input will not upset the unselected digits.

2. **Time Set Select**—Enables set inputs to the timekeeping register. When updating hours, the minutes display will blank out and MX1 digit will display A or P. Minutes will update in a normal manner and reset seconds to zero. Seconds will restart on release of the time set select line. When deselected, the time will continue to be displayed for 5 seconds ± 1 seconds. AM and PM indications will switch on the transfer from 11:59 to 12:00.

3. **Elapsed Time Select**—Displays contents of elapsed time register while active. Left set will stop E.T. accumulation, right set or E.T. reset will restart accumulation of E.T.

4. **Elapsed Time Reset**—Displays, zeros, and restarts the elapsed time register.

5. **Date Select**—Displays the contents of the calendar register and enables set inputs. When deselected, the date will continue to be displayed for 5 ± 1 seconds. If elapsed time select is true, the 5 seconds counter shall be inhibited.

6. **Ignition Off**—When ignition is off, all set inputs will be inactive and display outputs will be turned off. When ignition is turned on, the date will display for 5 seconds then revert to time.

7. **Time Register**—The time register is a 12 hour register. The time register shall be normally selected with no control inputs selected. When time set select and ignition sense are both true, the 5 seconds date counter shall be inhibited.

8. **Elapsed Time Register**—The elapsed time register shall be capable of accumulating time up to 99 hours and 59 minutes. The display shall be minutes and seconds to 59 minutes and 59 seconds then switch automatically to hours and minutes format. After 99 hours and 59 minutes, the elapsed time will reset to 00:00 and continue accumulation in minutes and seconds format as detailed above. All leading zeros shall be displayed.

9. **Date Register**—The date register will be a 4 year "smart" calendar. A month/date and date/month format will be pin selectable. The set inputs shall index the appropriate left or right digits regardless as to which format is selected. Date will advance on the transfer from PM to AM.

Date Setting—When date of month is set, the number will advance to the maximum allowed for the particular month being displayed. Further advance will reset the date to "01" and continue advancing as before. When the month is being set and the date is greater than that allowed for that month, (i.e., 02 30), the next timekeeping switch from PM to AM will advance the month and set the date to "01" (i.e., 03 01).

10. All registers are to be independent, i.e., setting time will not index calendar.

11. All registers will continue to accumulate while ignition is off.

12. Colons shall be non-flashing and displayed in the time display and elapsed time modes. Colons shall be extinguished in the date display mode.

13. On initial power up or in case of battery disconnect, the display shall read 0:00 on all functions until time is set. Voltage rise time to 10 volts will be greater than 10 mseconds.

14. **Register Preference**—If more than one register for display is selected at one time, time will have preference over date, date will have preference over elapsed time.

15. **Illegal Conditions**—If either date, time, or E.T. reset inputs are true at the same time, the clock display shall blank. All set inputs will be disabled while the clock is in an illegal mode.

16. **Test Condition**—When date select, elapsed time select, time set select, and both right and left set inputs are true, the clock may enter a test mode.

17. **Switch Debounce Protection**—All setting inputs shall be protected against switch debounce for a period of 13mseconds min.

Absolute Maximum Ratings

Positive voltage on any pin ..... V_{SS} + 0.3V
Negative voltage on any pin ..... V_{SS} – 30.0V
Storage Temperature ..... – 60°C to + 150°C
Operating Temperature ..... – 40°C to + 85°C

S4003 Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions
V_{SS} Supply Voltage Outputs Operational	9	20	24	Volts	V_{DD} = GND
V_{SS} Supply Voltage No Loss of Memory	7		24	Volts	V_{DD} = GND
V_{SS} Supply Voltage	7		24	Volts	Voltage to be ramped up from 0 volts (time constant 10ms from 0 to 10 volts)
I_{SS} Supply Current		5	6.5	mA	V_{SS} = 12V 25°C
No Output Loads		10	15	mA	V_{SS} = 20V
F0 Crystal Frequency		4.194304		MHz	
Fc Converter Frequency		65.536		KHz	
Converter Frequency Start w/Ignition Sense Off		8		Volts	V_{DD} = GND
Input Voltage					
V_{IH}	V_{SS} – 1		V_{SS}	Volts	
V_{IL} (Except Ignition Sense)	V_{DD}		V_{DD} + 1	Volts	
Ignition Sense (On)	+ 5.0			Volts	V_{SS} = 9 to 20V
(Off)			+ 1.0	Volts	V_{DD} = GND
Output Currents					
Segment (Single) I_{OL}	0.5			mA	$V_{OH} = V_{SS} - 1$
I_{OH}	1.0			μA	Leakage to V_{DD} (Output Off)
(A&D MX10) I_{OL}	1.0			mA	$V_{OH} = V_{SS} - 1$
I_{OH}	1.0			μA	Leakage to V_{DD} (Output Off)
Converter I_{OH}	3.0			mA	$V_{SS} - 2$, V_{SS} = 18V
	1.0			mA	$V_{SS} - 2$, V_{SS} = 7V

AMI

A Subsidiary of Gould Inc.

S2709A

VACUUM FLUORESCENT DIGITAL CLOCK FOR AUTOMOTIVE APPLICATIONS

Features

- ☐ Uses Inexpensive 4MHz Crystal
- ☐ Direct Drive to Green or Blue Vacuum Fluorescent Display
- ☐ Low Standby Power Dissipation When Display is Switched Off With Ignition
- ☐ Variable Brightness Tracks Other Dash Lights

Applications

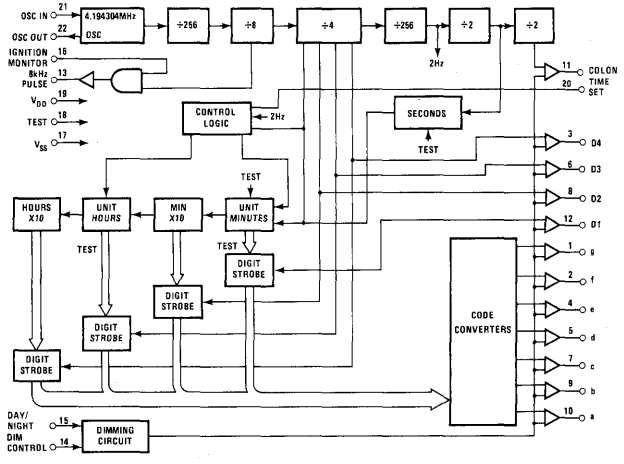
- ☐ In Dash Automobile Clocks
- ☐ Tape Players, CB Radio Units
- ☐ Automotive After Market Clocks
- ☐ Aircraft, Marine Panel Clocks
- ☐ Portable Instrumentation Clocks

Functional Description

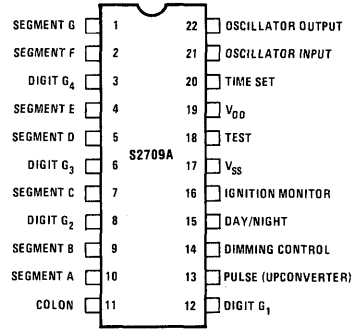
The S2709A vacuum fluorescent clock is a monolithic MOS integrated circuit utilizing P-Channel low threshold, enhancement mode and ion-implanted depletion mode devices. The circuit interfaces directly with 4 digit multiplexed vacuum fluorescent displays and requires only a single nominal 12V power supply. The timekeeping function operates from a 4MHz crystal controlled input. The display format is 12 hours with colon and leading zero blanking. An up-converter output is provided by the circuit to generate increased display driving voltage. A brightness control input allows variation of the display intensity. An ignition monitor input controls the upconverter operation and inhibits time setting. The S2709A is normally supplied in a 22-lead plastic dual-in-line package.

CONSUMER PRODUCTS

Block Diagram



Pin Configuration



Operational Description

Refer to the block diagram and Figure 1, Typical Application.

Oscillator Input (Pin 21) and Output (Pin 22) — The crystal controlled oscillator operates at a frequency of 4.194304 MHz to increase accuracy and reduce external component costs due to the less expensive quartz crystal. The frequency is controlled by a quartz crystal and fixed capacitor upconverter output (pin 13). This method allows accurate frequency tuning of the crystal oscillator without loading down the oscillator circuit. The feedback and phase shift resistors are integrated to further reduce external component costs. The internal oscillator inverter drives a counter chain that performs the timekeeping function.

Time Setting Input (Pin 20) — To prevent tampering, time setting is inhibited until the ignition monitor (pin 16) is held at a logic high level (V_{SS}).

Normal timekeeping is provided by allowing the time set pin to float externally. (Unloaded, this pin will alternate between V_{DD} and V_{SS} in phase with the unit minutes digit strobe [pin 12] during normal timekeeping.) If the time set pin is held at a logic high level (V_{SS}), the minutes counter advances at a 2Hz rate without carry to hours. If the time set pin is held at a logic low level (V_{DD}) the hours counter advances at a 2Hz rate.

It is possible to reset the hours, minutes and internal seconds counter by applying a logic low level (V_{DD}) to the test input (pin 18) during the time that the ignition monitor input is at a logic low level (V_{SS}). This reset state (time 1:00) is used for testing purposes.

Upconverter Pulse Output (Pin 13) — The clock circuit and vacuum fluorescent display drive normally operate at 25V when the ignition monitor pin is held at a logic high level (V_{SS}). The automobile battery voltage (12V) is doubled by an external upconverter circuit triggered by an 8kHz output pulse having a 28% duty cycle. The voltage, whether 12V or 25V, is applied to the circuit via the V_{SS} input (pin 17).

When the ignition monitor pin is held at a logic low level (V_{DD}) the upconverter is disabled. This drops the V_{SS} supply to 12V allowing the clock to operate while the display drive is decreased, lowering power dissipation. As the battery voltage drops (due to engine starting, cold temperature, or aging) timekeeping is maintained down to approximately 7V with no loss of the memory down to 5V. However, below 10V the upconverter will not be inhibited by the ignition monitor input.

Note that low standby power dissipation (60mW typical @ V_{SS} = 12V, and no output loads) is accomplished by turning off the filament voltage to the display when the auto ignition switch is off.

Ignition Monitor (Pin 16) — Along with preventing the already mentioned time setting function, the ignition monitor when held at a logic low level (V_{DD}) inhibits the 8kHz upconverter output pulse (pin 13) as long as the supply (V_{SS}) is above 10V. This pin is normally connected to the auto accessory switch.

The ignition monitor input can be protected against power supply transients by using 47KΩ external series resistance (See Figure 1).

Day/Night Display Control Input (Pin 15) — As seen in Figure 2, the display brightness is controlled via both pin 15 and the dimming control input (pin 14). The day/night input is connected to the automobile parking or headlights switch such that when these lights are off (V_{IN} low) the decoded segment and the digit outputs are from V_{SS} to V_{SS} – 2.0 volts. When the parking or headlights are switched on (V_{IN} high) the internal day/night logic enables the dimming input to control the segment and digit output voltage and brightness by allowing adjustable current to flow as controlled by the dash lights rheostat.

The day/night input can be protected from power supply transients by using 47KΩ external series resistance (See Figure 1).

Display Dimming Control Input (Pin 14) — The display dimming input is connected to the automobile dashboard light dimming rheostat through a series resistor. This allows the fluorescent display to track the dimming characteristics of the incandescent dashboard light (See Figure 2). The display dimming control is inhibited unless the day/night input (pin 15) is held at a logic high level (V_{SS}).

Display Drivers (Pins 1 through 12) — The 12 hour display format is comprised of four digits with leading zero blanking and a flashing colon. Each digit contains 7 segments with individual segments coded in the conventional manner (See Figure 1). The display is multiplexed with each digit output (G1, G2, G3 and G4) being strobed for a time period of approximately 0.5mS. Figure 3 shows the minimum output current as a function of output voltage for the digit (grid) and segment outputs.

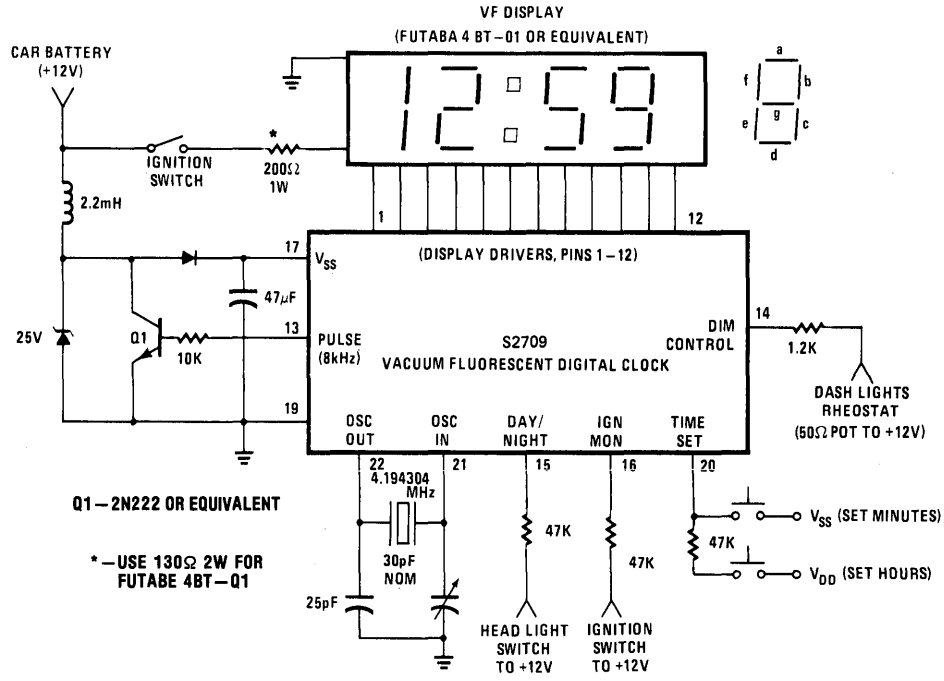
The colon output (pin 11) is designed to have an unobtrusive flash while still indicating that the clock is functioning normally. The colon flash is accomplished in a 2 second period of 1-1/2 seconds on the 1/2 second off.

Electrical Characteristics

Symbol	Characteristics/Conditions	V_{DD} V	0°C to 70°C			Unit
			Min.	Typ.	Max.	
V_{SS}	Operating Supply Range V_{DD} = 0.0V (Refer to Upconverter Pulse Output)		7.0		28	V
I_{SS}	Supply Current	12			12	mA
	(No Loads On Outputs)	25			15	mA
	Oscillator Frequency			4.194304		MHz
	Display Outputs					
	Multiplex Rate			512		Hz
	Duty Cycle (Each Digit Per Cycle)			18.8		%
	Output Current (Day/Night = LOW)					
I_{OH}	Digits, V_{OH} = 24V	25			−6.0	mA
I_{OL}	V_{OL} = 2V	25	40			μA
I_{OH}	Segments & Colon, V_{OH} = 24V	25			−1.5	mA
I_{OL}	V_{OL} = 2V	25	10			μA
	Output Voltage (V[Pin 14]−V(Digit or Seg)					
	Day/Night = High, V(Pin 14≥/4V)					
ΔV_O	Digits (R_L = 8.2KΩ to V_{DD})	25			1	V
ΔV_O	Segment (R_L = 100KΩ to V_{DD})	25			1	V
	Upconverter Pulse Output					
	Pulse Frequency			8192		Hz
	Duty Cycle			25		%
	Output Current					
I_{OH}	V_{OH} = 8V	10			−1.5	mA
I_{OH}	V_{OH} = 23V	25			−3.0	mA
I_{OL}	V_{OL} = 1V	25	6.0			μA
	Time Set Input/Output					
	Input Voltage (No Load)					
V_{IH}	High	25	24		1	V
V_{IL}	Low	25	0		1	V
	Output Current					
I_{OH}	V_{OH} = 18V	25	−6.0		−2.0	mA
	Output Frequency			512		Hz
	Duty Cycle			25		%
	Ignition Monitor Input and Day/Night Input					
	Input Voltage					
V_{IH}	High	9.0 to 25	6.5		V_{SS}	V
V_{IL}	Low	9.0 to 25	0		2.0	V
I_{IH}	Input Current (Pull Down) V_{IH} = 12V	25	2		20	μA

CONSUMER PRODUCTS

Figure 1. Typical Application



AMI

A Subsidiary of Gould Inc.

S4036

GENERAL PURPOSE A/D CONVERTER AND DIGITAL SCALE CIRCUIT

Features

- ☐ On-Chip Voltage Regulator
- ☐ On-Chip Low Supply Detection
- ☐ On-Chip LED Display Drivers
- ☐ Pin Selectable Sensitivity
- ☐ Linearity ± 5 LSB/3000 Bits
- ☐ Repeatability ± 3 LSB/3000 Bits

Applications:

- ☐ Low Cost ADC
- ☐ Digital Scale
- ☐ Digital Thermometer
- ☐ Digital Voltmeter
- ☐ Digital Light Meter

General Description

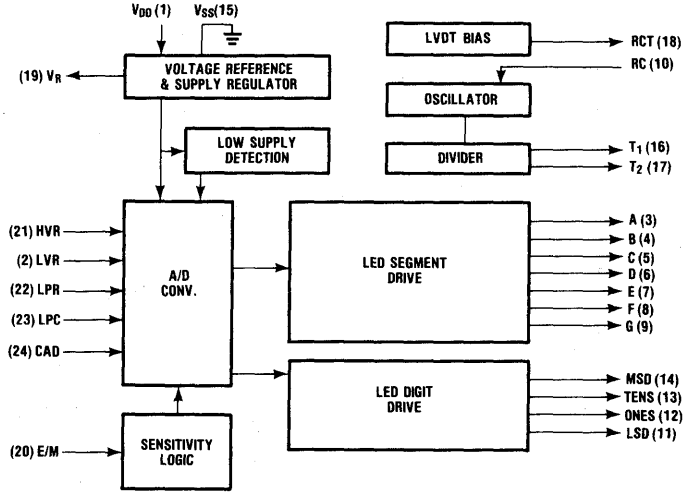
The S4036 General Purpose A/D Converter and Digital Scale Circuit provides a one chip solution to many Analog/Digital applications. Few external parts are needed as the S4036 provides an on-chip voltage reference, low supply detector, pin selectable sensitivity logic, and drivers for a multiplexed LED display.

The S4036 can begin to process analog data immediately upon presentation, or it can wait to sample the data after two seconds of settling time at user discretion.

In the sampled data mode of operation, a short pulse applied to the V_{DD} input signals the S4036 to start the

CONSUMER PRODUCTS

Block Diagram



Pin Configuration

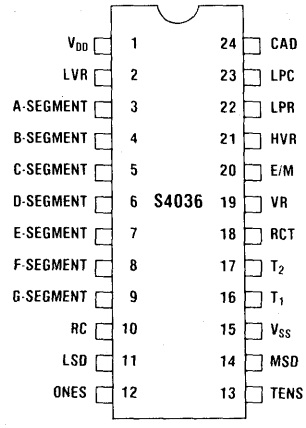


Figure 1. Typical ADC Application

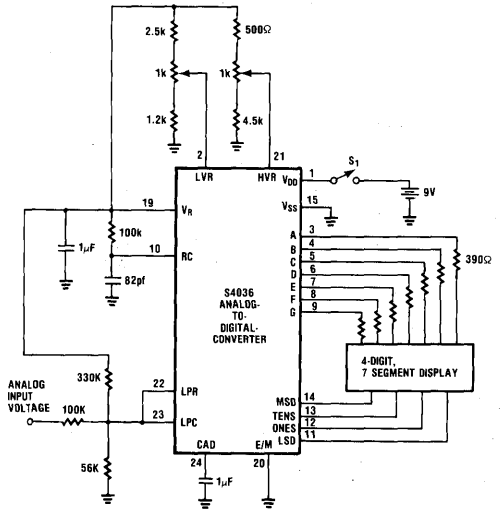
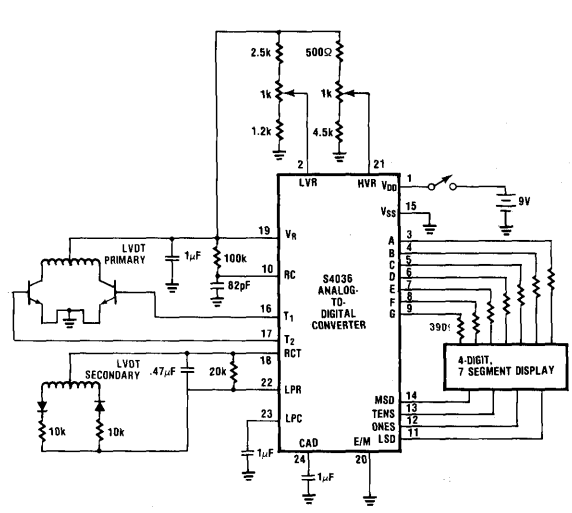


Figure 2. Typical Digital Scale Application



sample interval counter. The display clears to "000," with the most significant digit blanked. After two seconds, approximately, the S4036 begins to process the analog input. The display "rolls-up" from "000" to the digital value of the analog input. This "roll-up" process takes one second. The value on the display at the end of the conversion is held fixed until the V_{DD} line is pulsed to restart the process.

Here, a switch (S_1) pulses the V_{DD} input of the S4036 to begin the conversion process. When the analog voltage is more positive than the LVR voltage level, a non-zero reading will occur. If the analog voltage is more negative than the LVR level (underflow), a zero value reading will occur. If the analog voltage is more positive than the HVR voltage level (overflow), the S4036 will output a maximum value reading (2999 or 1360, depending on state of Pin 20). LVR is 1.5V to 2.5V, HVR is 4.5V to 5.5V.

The analog voltage is applied to Pins 22 and 23. Pins 16 (T_1), 17 (T_2), and 18 (RCT) are not connected. Notice the 390Ω resistors off Pins 3-9; these are used to limit the output current of the S4036.

A feature which can be user-programmed is the HVR and LVR voltages used by the ADC. The chip supplies a regulated voltage (Pin 19) which can be divided down and picked off via a potentiometer. Thus, the user can specify the lower reference ("0" value display point) and the upper reference (maximum value display point) merely by resistively dividing the regulated voltage output. This feature allows the S4036 to perform in many "non-standard" ADC situations.

A capacitor is required on Pin 24 to implement the Analog-to-Digital Converter. For most applications, the value of this capacitor is nominally 1μF, but this value is not critical to the conversion process.

Here, a mechanical input from the scale pulses the V_{DD} input of the S4036 to begin the conversion process. The same mechanical input from the scale also displaces the core of the Linear Variable Differential Transformer (LVDT) proportional to the weight of the object being measured. The LVDT primary is driven by 2NPN transistors controlled by S4036 timing outputs T_1 and T_2, which are 180° out of phase at a 50% duty cycle. The output (RCT) is used to bias the center tap of the LVDT secondary. The LVDT secondary presents an output which varies linearly with core position. This voltage is rectified, filtered, and presented to the analog inputs (LPR and LPC). (See Figure 3 for internal connection of S4036 pins RCT, LPR, and LPC.)

The S4036 has two pin-selectable modes of sensitivity. A Logic "0" on Pin 20 allows 3000 possible readings (0 to 2999), while a Logic "1" on Pin 20 allows 1361 possible readings (0 to 1360). This feature allows the sensitivity of the S4036 to be adapted to meet a wide range of ADC applications. In most digital scale applications, the pin-selectable sensitivity of the S4036 can be used to provide pounds (3000 readings) or kilograms (1361 readings) by providing a Logic "0" or "1" on Pin 20, respectively.

The chip also contains an RC oscillator amplifier which interfaces with an external resistor and capacitor to provide the timing for the Analog-to Digital Converter and multiplexed LED display drivers.

Absolute Maximum Ratings

Voltage at Any Pin ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Storage Temperature Range ..... – 65°C to + 150°C
DC Supply Voltage ..... 12 VDC
Power Dissipation (25°C) 1000mW
Safe Operation Temperature Range ..... 0°C to 50°C
Lead Temperature (During Soldering) ..... 300°C for Max. 10 Sec.

Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
T_{ACC}	Accurate Operation Temperature Range	10		35	°C	
V_{DD}	Operating Supply Voltage	V_{LS}		9.50	VDC	
f_{OSC}	Oscillator Frequency	91	104	117	KHz	R = 100K, C = 82pF
I_{DD}	Operating Supply Current			12	mA	Outputs Unloaded
t_{SAM}	2 Sec Data Sample Time	2.24	2.52	2.88	Sec	
t_{ADC}	ADC Calculation Internal	0.82	0.92	1.05	Sec	
f_{DISP}	Display MUX Frequency	355	406	457	Hz	
% MUX	Each Digit Minimum MUX Duty Cycle	20			%	
V_R	Regulated Voltage	5.5	6.00	6.5	V	Into 242 Ohm
V_{SEG}	V_{OUT}, Segment Drivers	7.2			V	Into 720 Ohm
V_{DIGIT}	V_{OUT}, Digit Drivers			1.2	V	From 91 Ohm
V_{LS}	Low Supply Detection & A/D Shutdown	6.3		7.3	V	
LVR	Low Voltage Reference	1.5		2.5	V	
HVR	High Voltage Reference	4.5		5.5	V	
f_{LVDT}	T_1 and T_2 Freq.	11	13	15	KHz	
V_{LVDT}	T_1 and T_2 Output Voltages @ V_{DD} = 8V			1	V	From 70K Ohm
		0.75			V	Into 1500 Ohm
	Linearity from Best Straight Line, V_{DD} = 8V			±5	Bits	2.3V ⩽ LPR ⩽ 4.7V LVR = 2V, HVR = 5V
	Reading Change Over Range of V_{DD}			±5	Bits	7.3V ⩽ V_{DD} ⩽ 9.0V, LVR = 2V, HVR = 5V, LPR = 3.5V
	Display Change Over Consecutive Readings			±3	Bits	V_{DD} = 8V, LVR = 2V, HVR = 5V, LPR = 3.5V

Figure 3. Internal Connection of S4036 Pins RCT, LPR, & LPC

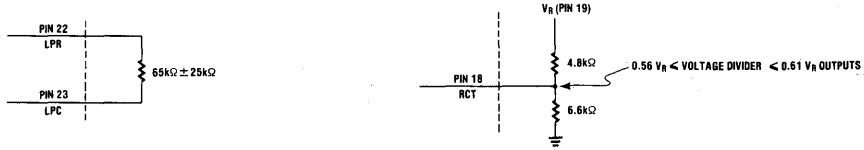
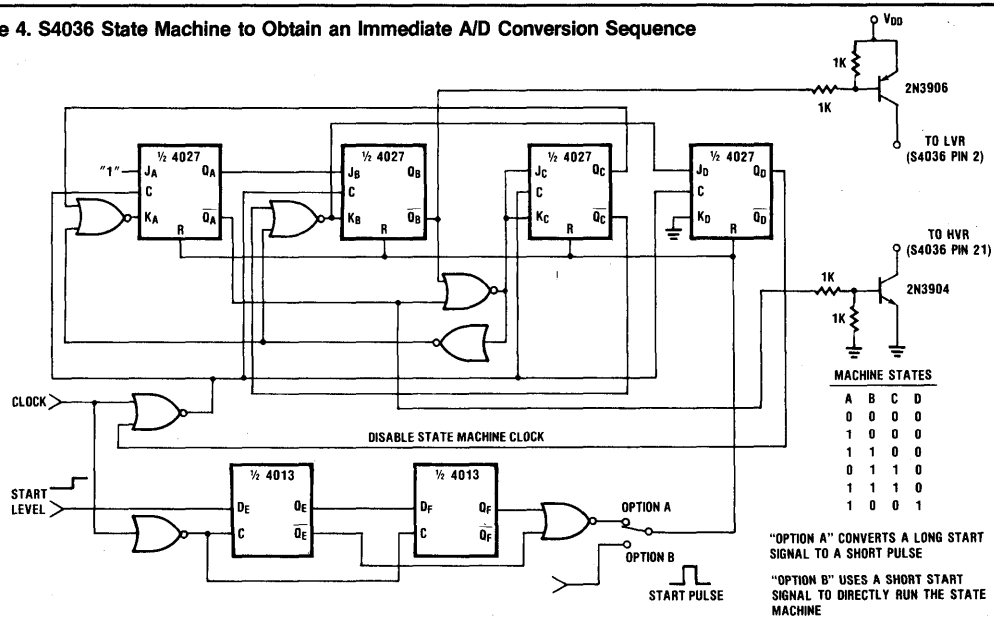


Figure 4. S4036 State Machine to Obtain an Immediate A/D Conversion Sequence



Immediate A/D Conversion Sequence

This sequence eliminates the analog data sample time, resets the S4036, and then proceeds directly with Analog-to-Digital conversion. This approach should be used for data which is steady when the S4036 is signaled to begin processing. It may be exercised by presenting the following logic series to LVR (Pin 2) and HVR (Pin 21):

Sequence Step	LVR	HVR
1	0	1
2	0	0
3	0	1
4	1	1
5	1	0
6	1	1
7	0	1

At the end of the signal sequence, the S4036 will sample the analog data input and "roll-up" the display to the digital value of the analog input. The sequence frequency should be greater than the oscillator frequency.

Logic "0": LVR $\leq$ 2.5V, HVR $\leq$ 1.0V

Logic "1": LVR $\geq V_{DD} - 1.0V$, HVR $\geq$ 4.5V

AMI

A Subsidiary
of Gould Inc.

Memories

Memory Products Selection Guide

STATIC MOS RANDOM ACCESS MEMORIES

Part No.	Organization	Process	Max. Access Time(ns)	Max. Active Power(mW)	Max. Standby Power(mW)	Power Supplies	Package
S68B10	128 x 8	NMOS	250	420	N/A	+ 5V	24 Pin
S68A10	128 x 8	NMOS	360	420	N/A	+ 5V	24 Pin
S6810	128 x 8	NMOS	450	400	N/A	+ 5V	24 Pin
S6810-1	128 x 8	NMOS	575	500	N/A	+ 5V	24 Pin

STATIC CMOS RANDOM ACCESS MEMORIES

Part No.	Organization	Max. Access Time(ns)	Max. Active Power(mW)	Max. Standby Power(mW)	Power Supplies	Package
S5101L-1	256 x 4	450	115	.055	+ 5V	22 Pin
S5101L	256 x 4	650	115	.055	+ 5V	22 Pin
S6501L-1	256 x 4	450	115	.055	+ 5V	22 Pin
S6501L	256 x 4	650	115	.055	+ 5V	22 Pin
S6514	1024 x 4	300	75	0.25	+ 5V	18 Pin
S6516	2048 x 8	230	55MHz	5.5	+ 5V	24 Pin

MOS READ ONLY MEMORIES

Part No.	Description	Organization	Process	Max. Access Time(ns)	Max. Active Power(mW)	Power Supplies	Package
S68A316	16,384 Bit Static ROM	2048 x 8	NMOS	350	370	+ 5	24 Pin
S68A332	32,768 Bit Static ROM	4096 x 8	NMOS	350	370	+ 5	24 Pin
S2333	32,768 Bit Static ROM	4096 x 8	NMOS	350	385	+ 5	24 Pin
S68A364	65,536 Bit Static ROM	8192 x 8	NMOS	350	385	+ 5	24 Pin
S68B364	65,536 Bit Static ROM	8192 x 8	NMOS	250	495	+ 5	24 Pin
S68A365	65,536 Bit Bank Switch ROM	8192 x 8	NMOS	450	415	+ 5	24 Pin
S2364A	65,536 Bit Static ROM	8192 x 8	NMOS	350	385	+ 5	28 Pin
S2364B	65,536 Bit Static ROM	8192 x 8	NMOS	250	385	+ 5	28 Pin
S6364	65,536 Bit Static ROM	8192 x 8	CMOS	250	55	– 5	28 Pin
S6464	65,536 Bit Static ROM with On-Board RAM	8 x 1024 x 8	NMOS	450	440	+ 5	24 Pin
S23128A	131,072 Bit Static ROM	16384 x 8	NMOS	350	385	+ 5	28 Pin
S23128B	131,072 Bit Static ROM	16384 x 8	NMOS	250	385	+ 5	28 Pin
S23256B	262,144 Bit Static ROM	32768 x 8	NMOS	250	220	+ 5	28 Pin
S23256C	262,144 Bit Static ROM	32768 x 8	NMOS	150	220	+ 5	28 Pin

AMI

A Subsidiary of Gould Inc.

Preliminary Data Sheet **MILITARY 6514**

4096 BIT (1024x4) STATIC CMOS RAM

Features

- ☐ Address Access Time-300ns Maximum
- ☐ Read and Write Cycle Time—420ns Maximum
- ☐ Low Power Operation—39mW Maximum @ 1MHz
- ☐ Low Power Standby—28μW Maximum
- ☐ On-Chip Address Registers
- ☐ Low Voltage Data Retention—2 Volts
- ☐ TTL Compatible Inputs and Outputs
- ☐ Three-State Outputs
- ☐ Military Temperature/Voltage Range
- ☐ 883-B Processing

The S6514 is fabricated using AMI's CMOS Technology. This permits the manufacture of very high density, high performance CMOS RAMs.

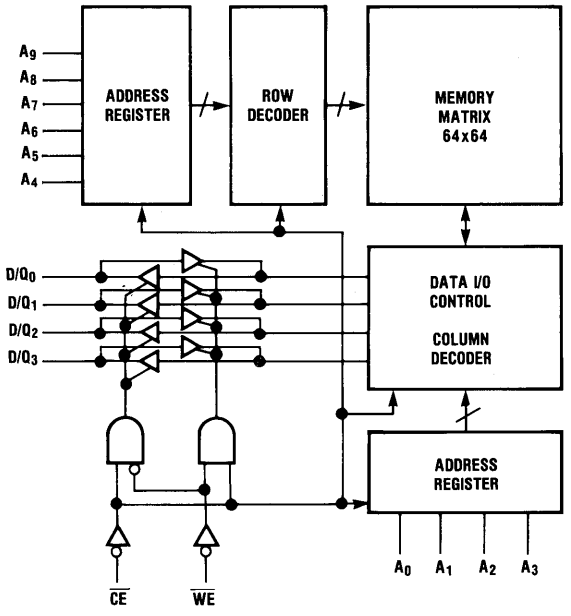
General Description

The AMI S6514 is a 4096 bit static CMOS RAM organized as 1024 words by 4 bits per word. The device offers low power and static operation from a single +5 Volt supply. All inputs and three-state outputs are TTL compatible. The common data I/O pins allow direct interface with common bus systems.

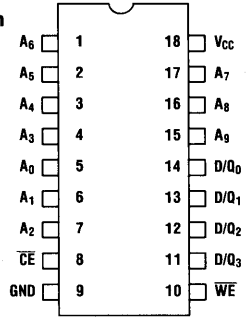
Data is latched into the on-chip Address Registers on the negative going edge of the Chip Enable signal. The data is then written into the cells on the negative going edge of Write Enable signal. The device is disabled and goes into a low power standby mode when the Chip Enable is High. Data in the memory will be maintained in this mode when V_{CC} is reduced to 2.0 Volts.

MEMORIES

Block Diagram



Pin Configuration



Pin Names

A_0-A_9	Address Inputs
D/Q_0-D/Q_3	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	Data Out
Read	L	H	Data In
Write	L	L	HI-Z
Disable	H	X	HI-Z

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage $-V_{CC}$ ..... −0.3V to +7.0V
Input/Output Voltage Applied ..... −0.3V to V_{CC} +0.3V
Storage Temperature $-T_{stg}$ ..... −65°C to +150°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

D.C. Electrical Characteristics: T_A = −55°C to +125°C, V_{CC} = +5V ± 10%

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage Current	−1		1	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	−1		1	μA	V_{IN} = GND to V_{CC}
I_{SB}	Standby Supply Current			50	μA	V_{IN} = GND or V_{CC}
I_{CC}	Operating Supply Current			7	mA	V_{IN} = GND or V_{CC}, f = MHz
V_{IL}	Input Voltage LOW	−0.3		0.8	V	
V_{IH}	Input Voltage HIGH	2.4		V_{CC} +0.3	V	
V_{OL}	Output Voltage LOW			0.4	V	I_{OL} = 1.6mA
V_{OH}	Output Voltage HIGH	2.4			V	I_{OH} = −0.4mA

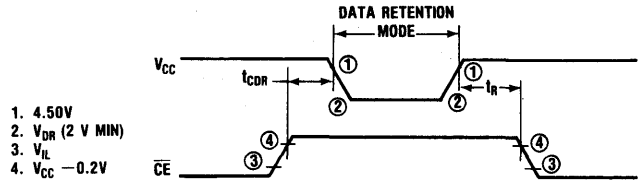
Capacitance: T_A = 25°C, f = 1MHz. Capacitance is sampled and guaranteed.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	GND to V_{CC}
C_{OUT}	Output Capacitance			10	pF	GND to V_{CC}

Low V_{CC} Data Retention Characteristics:

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{CCDR}	I_{CC} for Data Retention			50	μA	See Test Conditions and Waveforms
V_{CCDR}	V_{CC} for Data Retention	2.0			V	
t_{CDR}	Chip Deselect to Data Retention Time	0			ns	
t_R	Operation Recovery Time	TELEL			ns	

Low V_{CC} Data Retention Wave Form



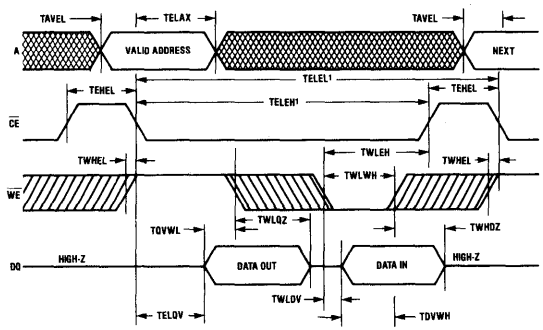
A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
trise/tfall	≤20ns
Output Load	1 TTL Load and 50pF
Timing Levels	1.5V

A.C. Electrical Characteristics: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
TELQV	Chip Enable Access Time			300	ns	
TAVQV	Adress Access Time			320	ns	
TWLQZ	Write Enable Output Disable Time			100	ns	
TEHQZ	Chip Enable Output Disable Time			100	ns	
TELEH	Chip Enable Pulse Negative Width	300			ns	
TEHEL	Chip Enable Pulse Positive Width	120			ns	See A.C. Test
TAVEL	Address Setup Time	20			ns	Conditions and
TELAX	Address Hold Time	50			ns	Waveforms
TWLWH	Write Enable Pulse Width	300			ns	
TWLEH	Write Enable Pulse Setup Time	300			ns	
TELWH	Write Enable Pulse Hold Time	300			ns	
TDVWH	Data Setup Time	200			ns	
TWHDZ	Data Hold Time	0			ns	
TWHEL	Write Enable Read Setup Time	0			ns	
TQVWL	Output Data Valid to Write Time	0			ns	
TWLDV	Write Data Delay Time	100			ns	
TELWL	Early Output High-Z Time			0	ns	
TWHEH	Late Output High-Z Time			0	ns	
TELEL	Read or Write Cycle Time	420			ns	

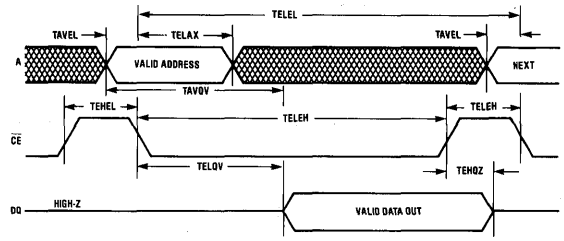
Read Modify Write Cycle



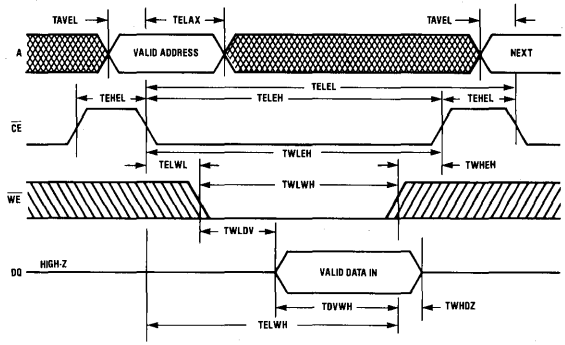
NOTE 1: TELEL & TELEH ARE LONGER THAN THE MINIMUM GIVEN FOR READ OR WRITE CYCLE.

MEMORIES

Read Cycle: $\overline{WE}$ = HIGH



Write Cycle



AMI

A Subsidiary of Gould Inc.

Preliminary Data Sheet **MILITARY 6516**

16,384 BIT (2048x8) STATIC CMOS RAM

Features

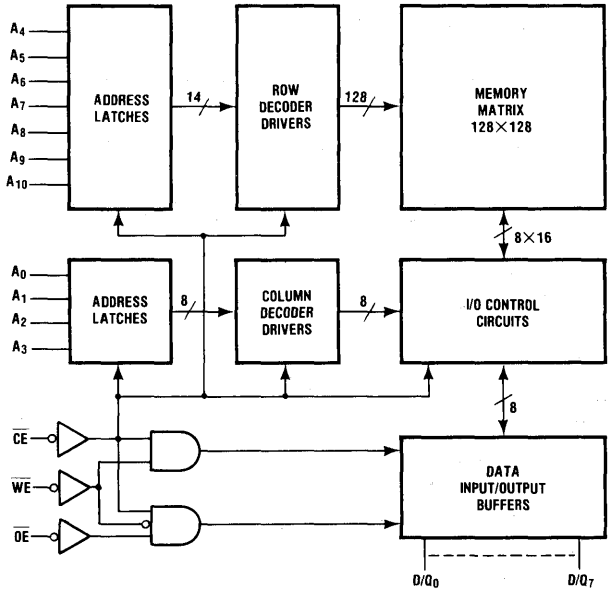
- ☐ High Speed—150ns Maximum
- ☐ Low Power Standby—1.38mW Maximum
- ☐ Low Power Operation—83mW/MHz Maximum
- ☐ On-Chip Address Registers
- ☐ Fully TTL Compatible Inputs
- ☐ Three-State TTL Outputs
- ☐ Low Voltage Data Retention – 2V
- ☐ Standard 24 Pin Package
- ☐ EPROM and ROM Compatible Pinouts

General Description

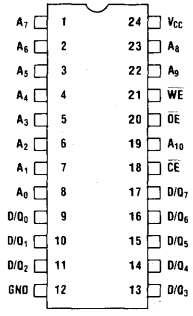
The AMI S6516 is a 16,384 bit static CMOS RAM organized as 2048 words by 8 bits. It offers low standby and operating power dissipation from a single + 5V power supply. All inputs and outputs are TTL compatible. The common data I/O pins allow direct interface with common bus systems. The output enable function facilitates memory expansion by allowing the outputs to be OR-tied to other devices. The device operates synchronously with address registers provided on-chip. The data is latched into the registers during the high to low transition of the chip enable pulse.

MEMORIES

Block Diagram



Pin Configuration



Pin Names

A_0—A_{10}	Address Inputs
D/Q_0—D/Q_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Outputs
Read	L	H	L	Data Out
Write	L	L	H	High-Z
Chip Disable	H	X	X	High-Z
Output Disable	L	X	H	High-Z

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−0°C to +70°C
Storage Temperature	−65°C to 150°C
Power Supply Voltage	−0.3V to 7V
Voltage on Any Pin with Respect to Ground	−0.3V to V_{CC} +0.3V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device.

D.C. Electrical Characteristics: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage Current	−1		1	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current	−1		1	μA	V_{OUT} = GND to V_{CC}
I_{SB}	Standby Supply Current			250	μA	V_{IN} = GND or V_{CC}
I_{CC}	Operating Supply Current			15	mA	V_{IN} = GND or V_{CC}, f = 1MHz
V_{IL}	Input Voltage LOW	−0.3		0.8	V	
V_{IH}	Input Voltage HIGH	2.2		V_{CC} +0.3	V	
V_{OL}	Output Voltage LOW			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output Voltage HIGH	2.4			V	I_{OH} = −1mA

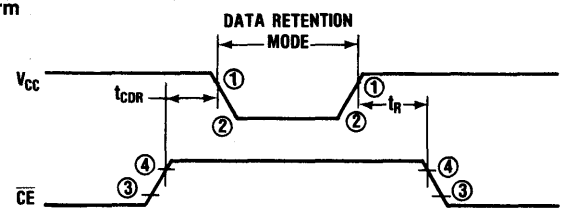
Capacitance: $T_A = 25°C$, t = 1MHz. Capacitance is sampled and guaranteed.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	GND to V_{CC}
C_{OUT}	Output Capacitance			10	pF	GND to V_{CC}

Low V_{CC} Data Retention Characteristics:

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{CCDR}	I_{CC} for Data Retention			250	μA	
V_{CCDR}	V_{CC} for Data Retention	2.0			V	
t_{CDR}	Chip Deselect to Data Retention Time	0			ns	
t_R	Operation Recovery Time	TELEL			ns	

Low V_{CC} Data Retention Wave Form



1. 4.50V
2. V_{DR} (2 V MIN)
3. V_{IL}
4. V_{CC} −0.2V

A.C. Test Conditions

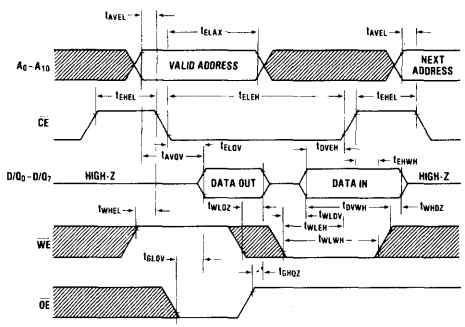
Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	≤10ns
Input Timing Level	0.8V and 2.2V
Output Timing Levels	0.6V and 2.2V
Output Load	1 TTL Load and 100pF

A.C. Electrical Characteristics: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$

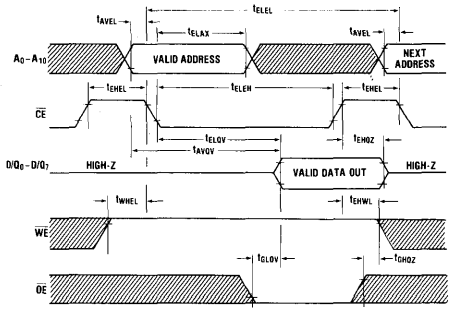
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{ELQV}	Chip Enable Access Time			150	ns	
t_{AVQV}	Address Access Time			150	ns	
t_{WLQZ}	Write Enable Output Disable Time			50	ns	
t_{EHQZ}	Chip Enable Output Disable Time			50	ns	
t_{ELEH}	Chip Enable Pulse Negative Width	150			ns	
t_{EHEL}	Chip Enable Pulse Positive Width	60			ns	
t_{AVEL}	Address Setup Time	0			ns	
t_{ELAX}	Address Hold Time	25			ns	
t_{WLWH}	Write Enable Pulse Width	140			ns	
t_{WLEH}	Write Enable Pulse Setup Time	140			ns	
t_{ELWH}	Write Enable Pulse Hold Time	140			ns	
t_{DVWH}	Data Setup Time	90			ns	
t_{WHDZ}	Data Hold Time	−10			ns	
t_{WHEL}	Write Enable Read Setup Time	0			ns	
t_{QVWL}	Output Data Valid to Write Time	−10			ns	
t_{WLDV}	Write Data Delay Time	40			ns	
t_{ELWL}	Early Output High-Z Time	−10			ns	
t_{WHEH}	Late Output High-Z Time	10			ns	
t_{ELEL}	Read or Write Cycle time	230			ns	

t_{EHWL}, Write Enable Read Hold Time ..... 0ns MIN.
t_{DVEH}, Data Setup Time to Chip Enable ..... 140ns MIN.
t_{GLQV}, Output Enable to Output Valid ..... 10ns MIN.
t_{GHQZ}, Output Enable to Output High-Z ..... 50ns MIN

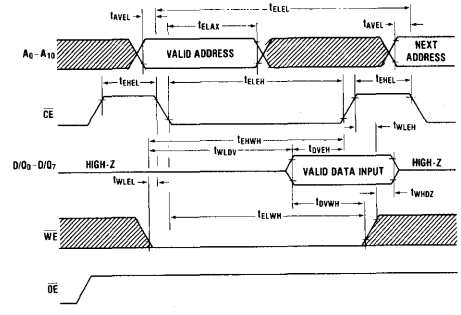
Read Modify Write Cycle



Read Cycle



Write Cycle



AMI®

A Subsidiary
of Gould Inc.

ROM Ordering Information

ROM Ordering Information

Ordering Information

The following information should be included in the purchase order when ROM devices are being ordered.

- ☐ Part number
- ☐ Number of ROM patterns
- ☐ Quantity of prototypes for each pattern (if none, so state)
- ☐ Total quantity of each pattern
- ☐ Special marking (if required)
- ☐ *Method of ROM code entry (EPROM, punched paper tape, etc.)
- ☐ *Chip select definition —
- ☐ Pricing and delivery (pricing and delivery quotes can be obtained from any AMI Sales Office)

*If ordering a previously supplied pattern, the order should refer to the AMI C number (CXXXXX). This C number can be obtained from previous AMI billing or acknowledgement.

Unit Quantity Variance

AMI manufactures ROMs in a fully proven silicon gate N-Channel process. However, as in any semi-conductor production, yield variations do occur. Because of these normal yield variations a policy has been established that requires the customer to accept a small variation from the nominal quantity ordered.

Unit Quantity Variance ±5% or 50 units (whichever is greater)

Part Number

An AMI ROM part number consists of a device number followed by a single letter designating the package type.

P — designates plastic package
C — designates ceramic package (hermetic seal)

Device Numbers

S6831B/S68A316	2K×8	
S68A332/S68332	4K×8	Standard Pinout
S2333	4K×8	(Pin compatible with 2732 EPROM)
S68A364/S68B364	8K×8	(24 Pin)
S2364A/B	8K×8	(28 Pin-Compatible W/2764 EPROM)
S23128A/B	16K×8	(28 Pin)
S23256B/C	32K×8	(28 Pin)

ROM Sales Policy

Minimum Order Quantity

Capacity	Part No.	Architecture	Units/Pattern
16K	S6831B, S68A316	2K×8	1,000
32K	S68332, S68A332	4K×8	1,000
32K	S2333 (Alternate Pinout)	4K×8	1,000
64K	S68A364/S68B364 (24-Pin)	8K×8	500
64K	S2364A/B (28-Pin)	8K×8	500
128K	S23128A/B (28-Pin)	16K×8	250
256K	S23256B/C	32K×8	250

Unless otherwise requested by the customer, approximately 5 units will be assembled in a ceramic package for verification of the ROM pattern by the customer. These 5 units will be considered as part of the total quantity ordered.

Mask Charges*

Most ROM suppliers charge a mask charge to cover the expense of generating tooling that is unique to each ROM pattern. Current AMI mask charges are as follows.

		Min. Qty/Mask Charges		
Part No.	Architecture	499 Pcs.	999 Pcs.	1500 Pcs.
S6831B, S68A316	2K×8	N/A	N/A	$ 500
S68332, S68A332, S2333	4K×8	N/A	N/A	$ 750
S68A364, S2364	8K×8	N/A	$2000	$1500
S23128A/B	16K×8	$2500	$2000	$1500
S23256B/C	32K×8	$2500	$2000	$1500

*Subject to Change

Reorder Policy

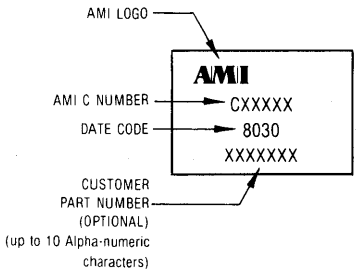
If a customer wishes to reorder the same ROM pattern, the following policy applies. If finished inventory exists, no minimum quantity limits will be imposed. However, if new wafer starts are required, the same minimum quantity as for a new pattern will apply. The 5 prototypes (supplied with new patterns) will not be supplied. No mask charge is applied to a reorder of a previously supplied ROM pattern.

ROM Ordering Information

ROM Package Marking

Unless otherwise specified, AMI ROMs are marked with a C number (the letter C followed by a 5 digit number) and a date code. This C number identifies both the device type and the specific pattern. This C number will be used on all AMI documents concerning the ROM.

A ROM can also be marked with a number supplied by the customer. A single number of up to 10 alpha numeric characters can be marked on the device without extra charge. Other customer markings are possible, but must be approved before the order is entered.



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to diskette and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested, AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitting ROM Code Data:

ROM		EPROM	
		PREFERRED	OPTIONAL
S6831B	2KX8	2716/2516	2-2708
S68332	4KX8	2532	2-2716/2516
S2333	4KX8	2732	2-2716/2516
S68A364	8KX8	68764	2-2532
S2364	8KX8	2764	2-2732
S23128	16KX8	27128	2-2764

If two EPROM's are used to specify one ROM pattern, (i.e., 2 16K EPROMs for one 32K ROM) two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Example: Two 2716 EPROMs for S68332 ROM
Marking: EPROM # 1 000-7FF
EPROM # 2 800-FFF

Pattern Data From ROMs

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitor's ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supplying ROM Code Data

If an EPROM or ROM cannot be supplied, the following other methods are acceptable.

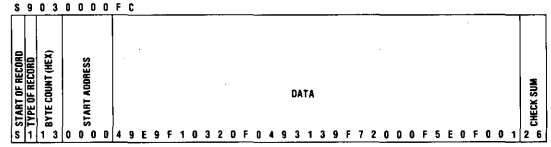
- ☐ 9 Track NRZ Magnetic Tape (2 each) odd parity, 800 BP1
- ☐ Paper Tape (AMI Hex format)
- ☐ Card Deck (AMI Hex format)

The AMI Hex format is described below. With its built-in address space mapping and error checking, this format is produced by the AMI Assembler.

Position	Description
1	Start of record (Letter S)
2	Type of record 0—Header record (comments) 1—Data record 9—End of file record
3, 4	Byte Count Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	Address Value The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9,..., N	Data Each data byte is represented by two hex characters. Most significant character first.
N + 1, N + 2	Checksum The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S113000049E9F10320F0493939F72000F5E0F00126
S9030000FC
```



Paper tape format is the same as the card format above except:

a. The record should be a maximum of 80 characters.
b. Carriage return and line feed after each record followed by another record.
c. There should NOT be any extra line feed between records at all.
d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

AMI

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S68A316**

16,384 BIT (2048X8) STATIC NMOS ROM

Features

- ☐ Fast Address Access Time: S68A316 - 350ns Max.
- ☐ EPROM Pin Compatible
- ☐ Fully Static Operation
- ☐ Three Programmable Chip Selects
- ☐ TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Late Mask Programmable

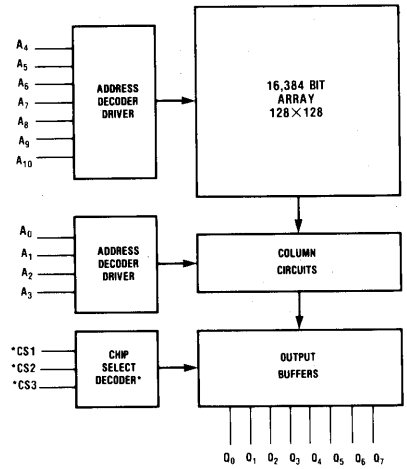
General Description

The AMI S68316 family of 16,384 bit mask programmable Read-Only-Memories organized as 2048 words by 8 bits offers fully static operation with a single +5V power supply. The device is fully TTL compatible on all inputs and three-state outputs. The three chip selects are mask programmable, the active level is specified by the user. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The devices are fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

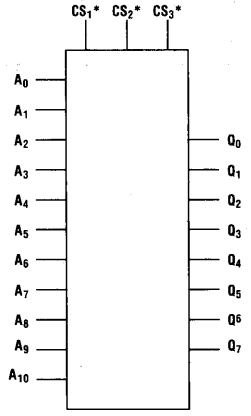
MEMORIES

Block Diagram

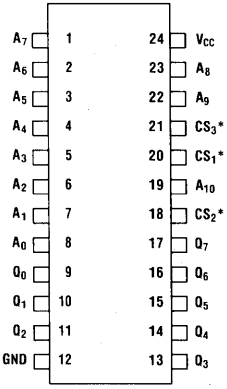


*USER DEFINED CHIP SELECTS
MAY BE DEFINED AS ACTIVE HIGH (CS) OR ACTIVE LOW (CS) OR NO CONNECTION (NC)

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{10}$	Address Inputs
$Q_0 - Q_7$	Data Outputs
$CS_1 - CS_3$	Chip Select Inputs
V_{CC}	+5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−10°C to 80°C
Storage Temperature	65°C to 150°C
Output or Supply Voltage	0.5V to 7V
Input Voltage	0.5V to 5.5V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 5%; T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0 to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current S68A316			80	mA	

Capacitance: f = 1.0MHz; T_A = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7.5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

A.C. Characteristics: V_{CC} = +5V ± 5%; T_A = 0°C to +70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S68A316			350	ns	See A.C. Test
t_{ACS}	Chip Select Access Time	S68A316			120	ns	Conditions and
t_{OFF}	Chip Deselect Time	S68A316			120	ns	Waveforms

NOTES:

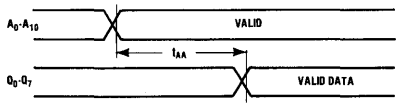
1. Only positive logic formats for CS_1—CS_3 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.

A.C. Test Conditions

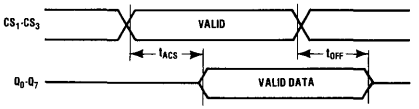
Input Pulse Levels	0.8V to 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms

Propagation From Addresses



Propagation From Chip Selects



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 2716; Optional (2) 2708

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

A Subsidiary of Gould Inc.

S68A332

32,768 BIT (4096X8) STATIC NMOS ROM

Features

- ☐ Fast Access Time:
  S68A332: 350ns Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±5% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Selects
- ☐ EPROM Pin Compatible—2532
- ☐ Extended Temperature Range Available

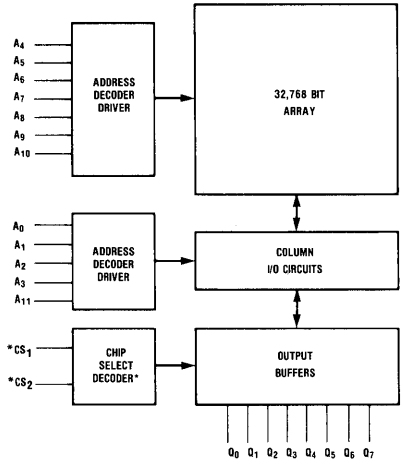
General Description

The AMI S68332 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single + 5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S68332 is pin compatible with UV EPROMs making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The two chip selects are mask programmable, the active level for each being specified by the user.

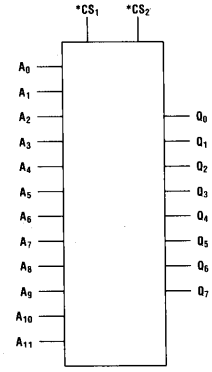
The S68332 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

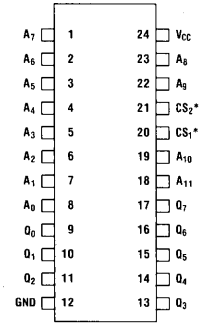


*PROGRAMMABLE CHIP SELECTS
MAY BE SPECIFIED AS ACTIVE LOW ($\overline{CS}$) OR ACTIVE HIGH (CS)
OR NO CONNECT (NC)

Logic Symbol



Pin Configuration



Pin Names

$A_0—A_{11}$	Address Inputs
$Q_0—Q_7$	Data Outputs
$CS_1—CS_2$	Chip Select Inputs
V_{CC}	+ 5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to + 70°C
(Industrial temp part)	− 40°C to + 85°C
Storage Temperature	− 65°C to 150°C
Output or Supply Voltages	− 0.5V to 7V
Input Voltages	− 0.5V to 7V
Power Dissipation	1W

* COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = + 5V ± 5%, T_A = 0°C to 70°C (Standard part); − 40°C to + 85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = − 220μA
V_{IL}	Input LOW Voltage	− 0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current			70	mA	

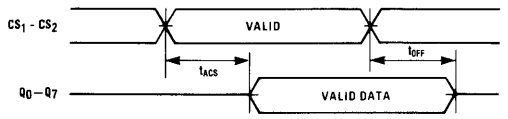
Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

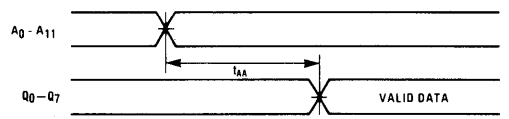
A.C. Characteristics: V_{CC} = + 5V ± 5%, T_A = 0°C to + 70°C (Standard part); − 40°C to + 85°C (Industrial temp part)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S68A332			350	ns	See A. C. Test
t_{ACS}	Chip Select Access Time	S68A332			150	ns	Conditions
t_{OFF}	Chip Deselect Time	S68A332			150	ns	Waveforms

Waveforms



Propagation From Chip Select



Propagation From Address

MEMORIES

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Rise and Fall Times	≤20ns
Input Timing Level	1.5V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Custom Programming

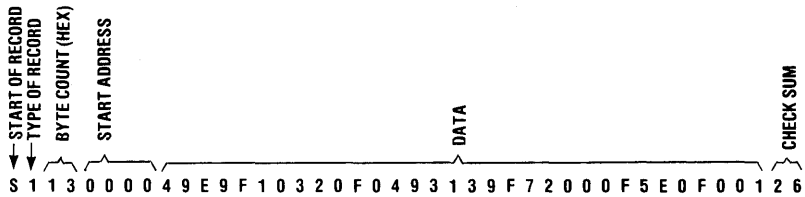
The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	Start of record (Letter S)
2	Type of record 0 — Header record (comments) 1 — Data record 9 — End of file record
3, 4	Byte Count Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	Address Value The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . . , N	Data Each data byte is represented by two hex characters. Most significant character first.
N + 1, N + 2	Checksum The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6

S 9 0 3 0 0 0 0 F C
```



NOTES:

1. Only positive logic formats for CS_1 and CS_2 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carraige return and line feed indicating end of file.

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S2333**

32,768 BIT (4096x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: 350ns Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±5% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Selects
- ☐ EPROM Pin Compatible (2732)
- ☐ Extended Temperature Range Available

General Description

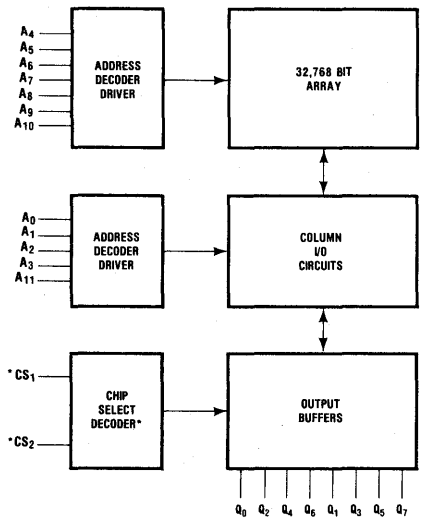
The AMI S2333 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2333 is pin compatible with UV EPROMs making system development much easier and more cost effective. The fully static S2333 requires no clocks for operation. The two chip selects are mask programmable with the active level for each being specified by the user.

The S2333 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

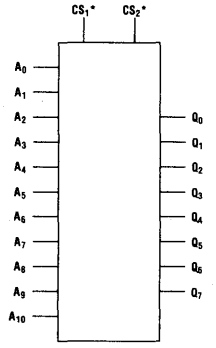
MEMORIES

Block Diagram

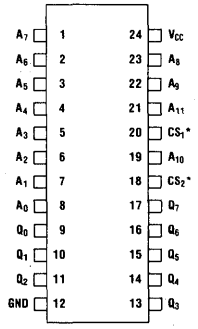


*PROGRAMMABLE CHIP SELECTS
MAY BE SPECIFIED AS ACTIVE LOW ($\overline{CS}$) OR ACTIVE HIGH (CS) OR NO CONNECT (NC)

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{11}$	Address Inputs
$Q_0 - Q_7$	Data Outputs
$CS_1 - CS_2$	Chip Select Inputs
V_{CC}	+5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to + 70°C
(Industrial temp part)	− 40°C to + 85°C
Storage Temperature	− 65°C to 150°C
Output or Supply Voltages	− 0.5V to 7V
Input Voltages	− 0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = + 5V ± 5%, T_A = 0°C to 70°C (Standard part); − 40°C to + 85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = − 220μA
V_{IL}	Input LOW Voltage	− 0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current			70	mA	

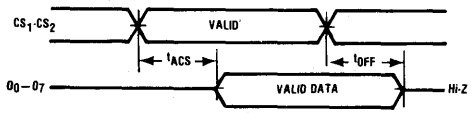
Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

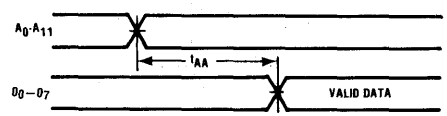
A.C. Characteristics: V_{CC} = + 5V ± 5%, T_A = 0°C to 70°C (Standard part); − 40°C to + 85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			350	ns	See A.C. Test Conditions and Waveform
t_{ACS}	Chip Select Access Time			120	ns	
t_{OFF}	Chip Deselect Time			120	ns	

Waveforms



Propagation From Chip Select



Propagation From Address

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Rise and Fall Times	≤20ns
Input Timing Level	1.5V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 1-2732; Optional 2-2716

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

AMI

A Subsidiary of Gould Inc.

S68A364/S68B364

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S68A364-350ns Maximum
  S58B364-250ns Maximum
- ☐ Low Standby Power: 85mW Maximum
- ☐ Late Mask Programmable
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Programmable Chip Enable

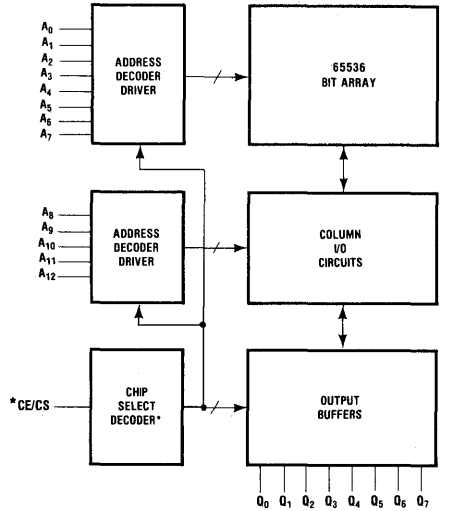
General Description

The AMI S68364 family are 65,536 bit static mask programmable NMOS ROMs organized as 8192 words by 8 bits. The devices are fully TTL compatible on all inputs and outputs and have a single +5V power supply. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The devices are fully static, requiring no clocks for operation. The chip enable is mask programmable, the active level being specified by the user. When not enabled, power supply current is reduced to a maximum of 15mA.

The S68364 family of devices are fabricated using AMI's NMOS ROM technology. This permits the mask programmable ROMs.

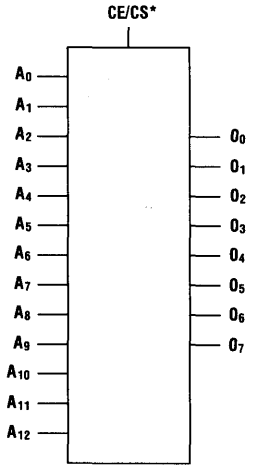
Block Diagram



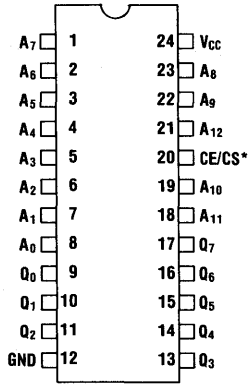
*USER DEFINED MASK PROGRAMMABLE AS CHIP ENABLE, CHIP SELECT, DON'T CARE—MAY BE DEFINED AS ACTIVE HIGH, ACTIVE LOW, DON'T CARE

NOTE: DON'T CARE PINS ARE CONNECTED TO ACTIVE CIRCUITRY

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{12}	Address Inputs
Q_0—Q_7	Data Outputs
CE/CS	Programmable Chip Enable/Chip Select
V_{CC}	+5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Electrical Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	mA	V_{IN} = 0V to V_{CC}
$\|I_{LO}\|$	Output Leakage Current			10	mA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current S68A364			90	mA	
	S68B364			90	mA	See Note #3
I_{SB}	Power Supply Current			15	mA	Chip Deselected (See Note#4)

Capacitance: T_A = 25°C, f = 1.0MHz (See Note #4)

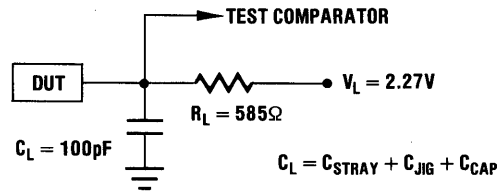
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

Switching Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S68A364			350	ns	See Waveforms
		S68B364			250	ns	and Test Load
t_{ACE}	Chip Enable Access Time	S68A364			350	ns	
		S68B364			250		
t_{ACS}	Chip Select Access Time	S68A364			150	ns	
		S68B364			120	ns	
t_{OFF}	Chip Deselect Time	S68A364			200	ns	See Note #5
		S68B364			100	ns	

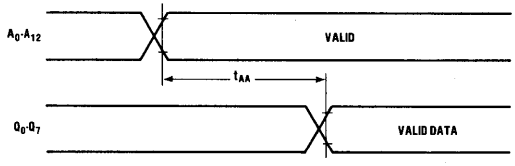
NOTES:
1. Only positive logic formats for CE/CE are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0; A "1" indicates the chip is enabled by a logic 1.
3. Power Test: V_{CC} = V_{CC} Max; CS/CE = active Output loads disconnected; Address pin inputs all held at V_{IL}
4. Standby Power Conditions: Same as active except CE = Deselect Level at V_I
5. Guaranteed by design.

Test Load

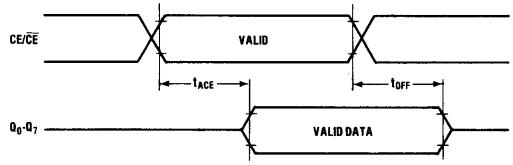


Waveforms

Propagation From Addresses



Propagation From Chip Enable



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 68A764

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

AMI®

A Subsidiary of Gould Inc.

S68A365

65,536 BIT (8192x8) STATIC BANK SWITCH NMOS ROM

Features

- ☐ Access Time = 450ns
- ☐ Late Mask Programmable
- ☐ Fully Static Operation
- ☐ Single +5V ±5% Power Supply
- ☐ Directly TTL Compatible Inputs and Outputs
- ☐ Programmable Chip Selects*
- ☐ Latch Up Circuitry
- ☐ Two Banks, Selected by FF8 and FF9
- ☐ Address Skew Protection

*User defined mask programmble Chip Select-may be defined as active high, active low, or no connect.

General Description

The AMI S68A365 is a 65,536 bit static bank select mask programmable NMOS ROM organized as 8192 words by 8 bits. The device is fully TTL compatible on all inputs and outputs with a single + 5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

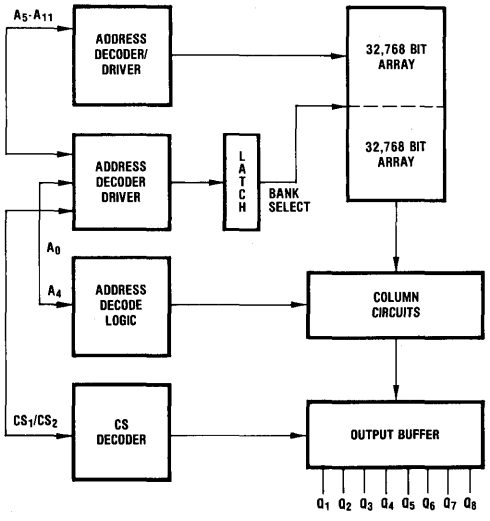
The device is fully static, requiring no clocks for operation. The two chip selects are mask programmable with the active level being specified by the user.

The S68A365 features two bank selects selected by hex codes FF8 and FF9, provided the chip selects are active.

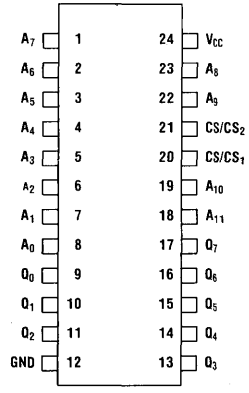
The device also incorporates in its design, debounce logic which provides protection against address skew.

MEMORIES

Block Diagram



Pin Configuration



Pin Names

A_0—A_{12}	Address Inputs
Q_0—Q_7	Data Outputs
CS/CS	Programmable Chip Select
V_{CC}	+ 5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias	− 0°C to + 70°C
Storage Temperature	− 40°C to + 90°C
Output or Supply Voltages	− 0.5V to + 7V
Input Voltages	− 0.5V to + 7V
Power Dissipation	415MW

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied., Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Electrical Characteristics: $V_{CC} = +5V \pm 5\%$, $T_A = 0°C$ to $+70°C$,

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 1.6mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -100_{m}A$
V_{IL}	Input LOW Voltage	− 0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.2		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	$_{m}A$	$V_{IN} = 0$ to $+5.25V$
$\|I_{LO}\|$	Output Leakage Current			10	$_{m}A$	$V_O = 0.4V$ to $5.25V$ Chip Deselected
I_{CC}	Power Supply Current			75	mA	

Capacitance: $T_A = 25°C$, $f = 1.0MHz$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	V_{OUT}

Switching Characteristics: $V_{CC} = +5V \pm 5\%$, $T_A = 0°C$ to $+70°C$,

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			450		See A.C. Test Conditions and Waveforms
t_{ACS}	Chip Select Access Time			450		
t_{BAV}	Bank Switching Address Valid			500		
t_{AS}	Address Skew			150		
t_{OFF}	Chip Deselect Time			150		
t_{BAA}	Bank Switching Access Time			820		

Functional Description

The S68A365 contains two banks of memory locations, each being 4096 words by 8 bits. The A_0-A_{11} inputs normally access only 4096 words of data. However, the S68A365 has a special bank-switching mode of operation which allows this device to effectively use the A_0-A_{11} addresses to access 8192 words of data. The timing diagrams illustrate this feature.

In order to switch banks, both chip selects must be in a valid state. Also, the address inputs must be hex address FF8 for a period t_{BAV} to an internal latch and thereby switch to Bank '0'. Likewise, for memory data to be read from Bank '1', both chip selects and Hex address FF9 must be held valid for t_{BAV} to set the internal latch.

The bank switching action occurs only with addresses

Functional Description (Continued)

FF8 and FF9. Further, if either FF8 or FF9 is valid for less than t_{AS}, the bank switching is guaranteed not to occur. Thus the output data will continue to be from one bank for as long as a bank switching operation does not take place.

Switching Test Conditions

Input Timing Level	0.8V to 2.2V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF
Input Rise and Fall Times	1ns per Volt

Figure 1. Timing Diagram

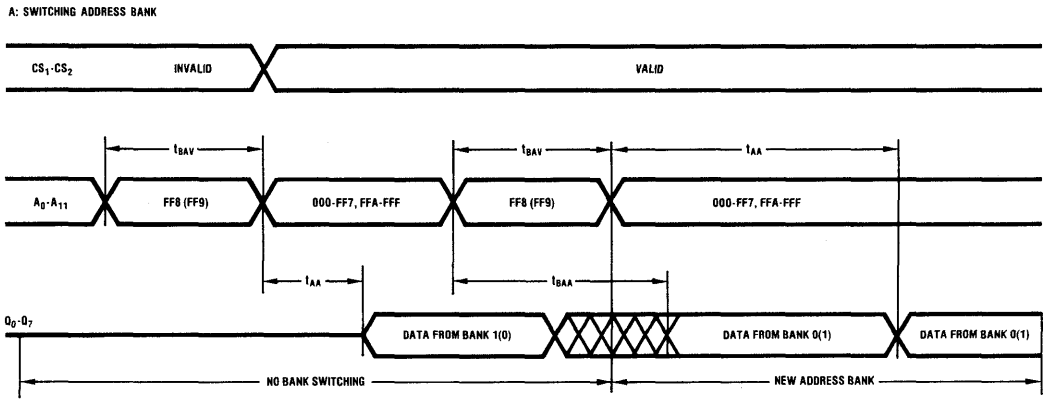
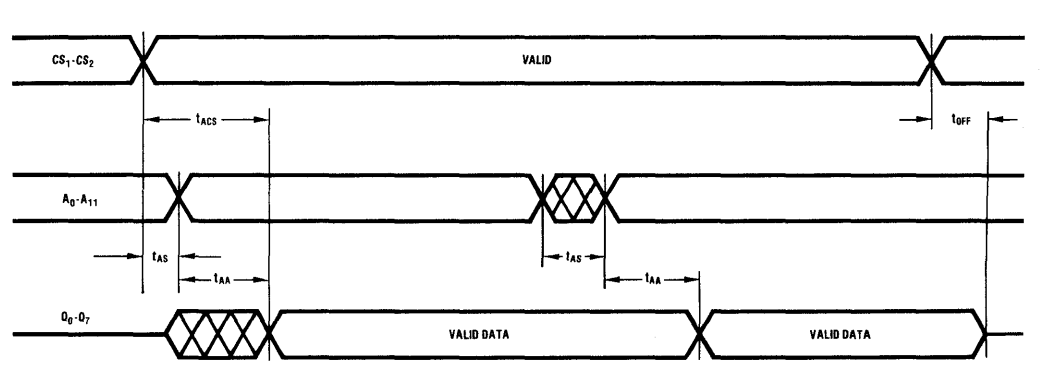


Figure 2. Timing Diagram



MEMORIES

ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Four EPROMs should be submitted. Two are programmed to the desired code and the remaining two are to be blank. AMI will read the programmed EPROMs, transfer this data to disk and then program the blank EPROMs from the stored information. This procedure guarantees that the EPROMs has been properly entered into the AMI computer system. The AMI programmed EPROMs are returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROMs.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED: Two 2732

Two EPROMs will be used to specify one ROM pattern. The programmed EPROMs must clearly state which of the two EPROMs is for Bank '0' and which is for Bank '1'. The preferred method is to mark the EPROM with the ROM address (in Hex) for selecting the appropriate Bank.

Optional Method of Supplying ROM Data*

If EPROMs cannot be supplied, the following other methods are acceptable.

ROM 9 Track NRZ Magnetic Tape
Paper Tape
Card Deck

*Consult AMI sales office for format.

AMI

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S2364A/S2364B**

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S2364A 350ns Maximum
  S2364B 250ns Maximum
- ☐ Low Standby Power: 85mW Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Chip Enables/Selects
- ☐ EPROM Pin Compatible (2764)
- ☐ Late Mask Programmable

General Description

The AMI S2364 is a 65,536 bit static mask programmable NMOS ROM organized as 8192 words by 8 bits.

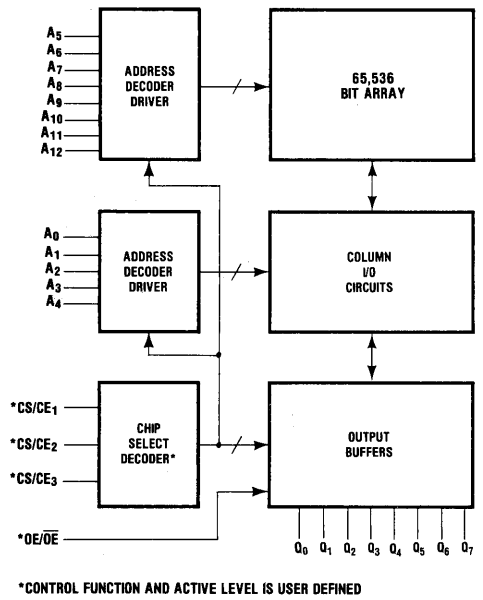
The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2364 is pin compatible with the 2764 UV EPROM making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The three chip enables are mask programmable; the active level for each being specified by the user. When not enabled, power supply current is reduced to a 15mA maximum.

The S2364 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

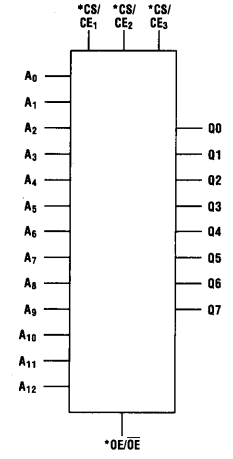
MEMORIES

Block Diagram

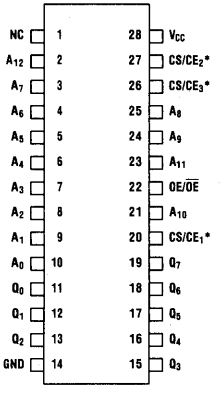


*CONTROL FUNCTION AND ACTIVE LEVEL IS USER DEFINED

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{12}	Address Inputs
Q_0—Q_7	Data Outputs
CS/CE_1-CS/CE_3	Chip Selects/Enables
$OE/\overline{OE}$	Output Enable
V_{CC};GND;NC	5V;Ground;No Connect

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin With Respect to Ground	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Electrical Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	μA	V_{IN} = 0V to 5.5V
$\|I_{LO}\|$	Output Leakage Current			10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			90	mA	See Note #1
I_{SB}	Power Supply Current—Standby			15	mA	See Note #2

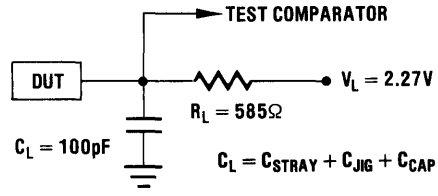
Capacitance: T_A = 25°C, f = 1.0MHz (See Note #3)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

Switching Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

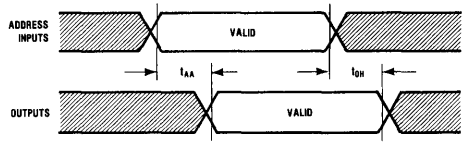
Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S2364A S2364B			350 250	ns	See Waveforms and Testload
t_{ACE}	Chip Enable Access Time	S2364A S2364B			350 250	ns	
t_{ACS}	Chip Select Access Time	S2364A S2364B			120 120	ns	
t_{OEA}	Output Enable Access Time	S2364A S2364B			100 100	ns	
t_{CEO}	Disable Time From Chip Enable	S2364A S2364B			200 80	ns	See Note #3
t_{OEO}	Disable Time From Output Enable	S2364A S2364B			100 80	ns	
t_{OFF}	Chip Deselect Time	S2364A S2364B			120 80	ns	See Note #3
t_{OH}	Output Hold Time	S2364A S2364B	10 0			ns	

Test Load

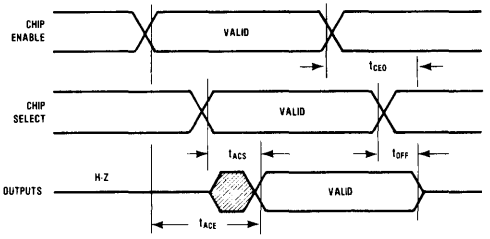


Waveforms

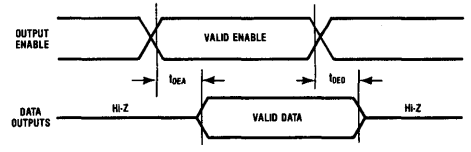
ADDRESS TO OUTPUT DELAY (CHIP SELECTED)



CHIP ENABLE/SELECT TO OUTPUT DELAY (ADDRESS VALID)



OUTPUT ENABLE TO OUTPUT DELAY (ADDRESS VALID/CHIP SELECTED)



MEMORIES

ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 1-2764; Optional 2-2732

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

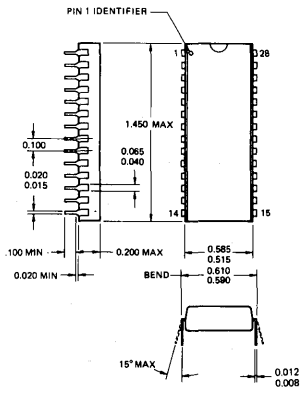
* Consult AMI sales office for format.

Notes:

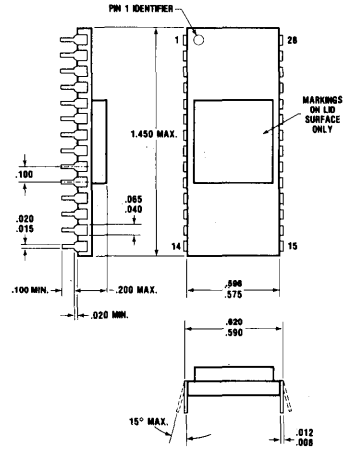
1. Active Power Conditions: $V_{CC} = V_{CC}$ Max, CE/CS = Active Level @ V_I, Address Pins = V_{IL}, Output Load Disconnected
2. Standby Power Conditions: Same as active except CE = Deselect Level @ V_I
3. Guaranteed by Design

Package Outlines

28-Pin Plastic



28-Pin Ceramic



Truth Table: (For simplicity, all control functions in the Truth Table are defined as active high.)

CS/CE1	CS/CE2	CS/CE3	OE/$\overline{OE}$	OUTPUTS	POWER
$\overline{CE1}$	X	X	X	HI-Z	STANDBY
X	$\overline{CE2}$	X	X	HI-Z	STANDBY
X	X	$\overline{CE3}$	X	HI-Z	STANDBY
$\overline{CS1}$	CS/CE2	CS/CE3	X	HI-Z	ACTIVE
CS/CE1	$\overline{CS2}$	CS/CE3	X	HI-Z	ACTIVE
CS/CE1	CS/CE2	$\overline{CS3}$	X	HI-Z	ACTIVE
CS/CE1	CS/CE2	CS/CE3	$\overline{OE}$/OE	HI-Z	ACTIVE
CS/CE1	CS/CE2	CS/CE3	OE/$\overline{OE}$	DATA OUT	ACTIVE

The user decides between a CS or CE function and then defines the active level. The functions may also be defined as Don't Care (DC). The chip is enabled when the inputs match the user defined states. Don't Care pins are still connected to input protection diodes and are subject to the "Absolute Maximum Ratings".

Pins	Control Functions Available
27	CS2, $\overline{CS2}$, CE2, $\overline{CE2}$, DC
26	CS3, $\overline{CS3}$, CE3, $\overline{CE3}$, DC
22	OE, $\overline{OE}$, DC
20	CS1, $\overline{CS1}$, CE1, $\overline{CE1}$, DC

AMI

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S6364**

65,536 BIT (8192x8) STATIC CMOS ROM

Features

- ☐ Fast Access Time: 250ns Maximum
- ☐ Low Standby Power 5.5mW Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Chip Enables/Selects
- ☐ EPROM Pin Compatible (2764)
- ☐ Programmable Output/Chip Enable

General Description

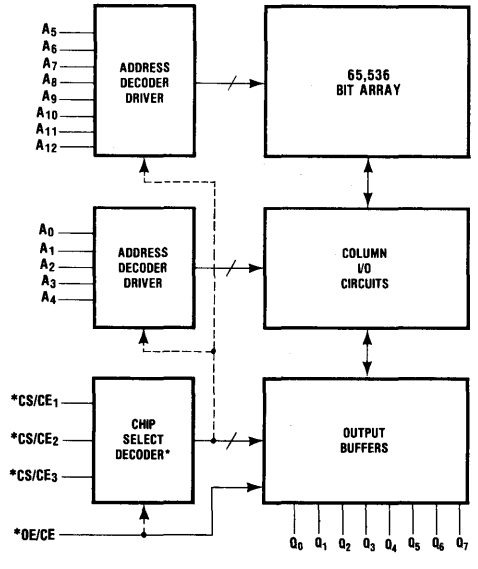
The AMI S6364 device is a 65,536 bit static mask programmable CMOS ROM organized as 8192 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S6364 is pin compatible with the 2764 UV EPROM making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The three chip enables are mask programmable; the active level for each being specified by the user. When not enabled, the power supply current is reduced to a 10mA maximum.

The S6364 is fabricated using AMI's CMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

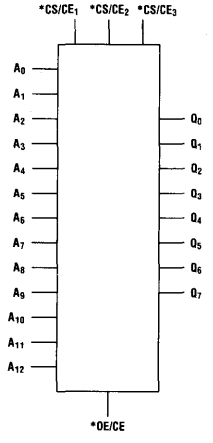
MEMORIES

Block Diagram

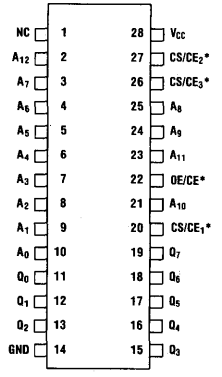


* THE USER DECIDES BETWEEN A CS OR CE FUNCTION AND OE OR CE FUNCTION THEN DEFINES THE ACTIVE LEVEL FOR CS/CE AND OE/CE.

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{12}	Address Inputs
Q_0—Q_7	Data Outputs
CS/CE_1-CS/CE_3	Chip Selects/Enables
OE/CE	Output Enable/Chip Enable
V_{CC}; GND; NC	5V; Ground; No Contact

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−40°C to 85°C
Storage Temperature	−65°C to 150°C
Output or Supply Voltages	−0.3V to 6V
Input Voltages	−0.3V to V_{CC} +0.3V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −400μA
V_{IL}	Input LOW Voltage	−0.1		0.8	V	
V_{IH}	Input HIGH Voltage	2.2		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
$\|I_{LO}\|$	Output Leakage Current			10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			10	mA	f = 1.0MHz
I_{SB}	Power Supply Current—Standby			1	mA	Chip Disabled

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

A.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			250	ns	See A.C. Test Conditions and Waveforms
t_{ACE}	Chip Enable Access Time			250	ns	
t_{OE}	Output Enable Access Time	0		80	ns	
t_{ACS}	Chip Select Access Time	0		80	ns	
t_{CEO}	Disable Time From Chip Enable	0		80	ns	
t_{OFF}	Chip Deselect Time	0		80	ns	
t_{OEO}	Disable Time From Output Enable	0		80	ns	
t_{OH}	Output Hold Time	0			ns	

TRUTH TABLE

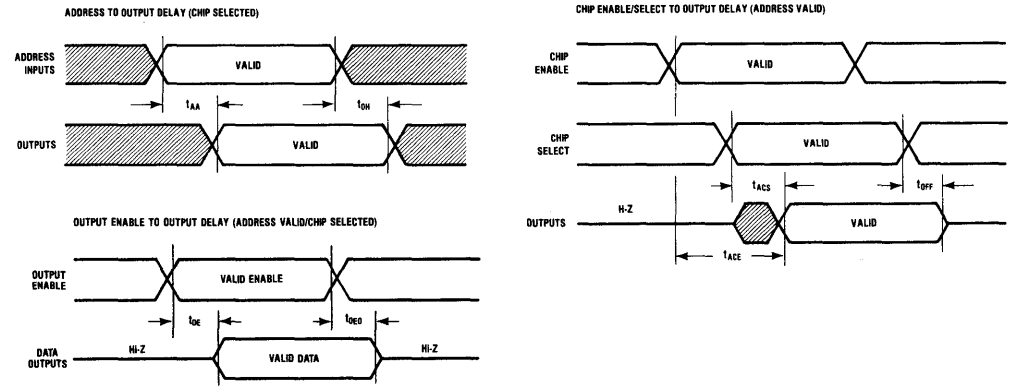
CS/CE1	CS/CE2	CS/CE3	OE/CE	OUTPUTS	POWER
$\overline{CET}$	X	X	X	HI-Z	STANDBY
X	$\overline{CE2}$	X	X	HI-Z	STANDBY
X	X	$\overline{CE3}$	X	HI-Z	STANDBY
X	X	X	$\overline{CE}$	HI-Z	STANDYB
$\overline{CS1}$	CS/CE2	CS/CE3	OE/CE	HI-Z	ACTIVE
CS/CE1	$\overline{CS2}$	CS/CE3	OE/CE	HI-Z	ACTIVE
CS/CE1	CS/CE2	$\overline{CS3}$	OE/CE	HI-Z	ACTIVE
CS/CE1	CS/CE2	CS/CE3	$\overline{OE}$	HI-Z	ACTIVE
CS/CE1	CS/CE2	CS/CE3	OE/CE	DATA OUT	ACTIVE

The user decides between a CS/CE and OE/CE function and then defines the active level. The functions may also be defined as a NO CONNECT NC). The chip is enabled when the inputs match the user defined states.

A.C. Test Conditions

Input Pulse Levels	0.8V to 2.2V
Input Timing Level	1.0V and 2.0V
Output Timing Levels	0.65V and 2.2V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 2764

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMs

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may only have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

65,536 Bit (8 × 1024 × 8) NMOS Static ROM With On-Board RAM

Features

- ☐ Access Times:
  - Address to Data — 450ns Maximum
  - Enable Time From A_{12} — 150ns Minimum
  - Disable Time From A_{12} — 225ns Maximum
- ☐ Power Dissipation 440mW Maximum
- ☐ Fully Static Operation
- ☐ Single +5V Power Supply
- ☐ Internally Generated Control Lines
- ☐ Late Mask Programmable

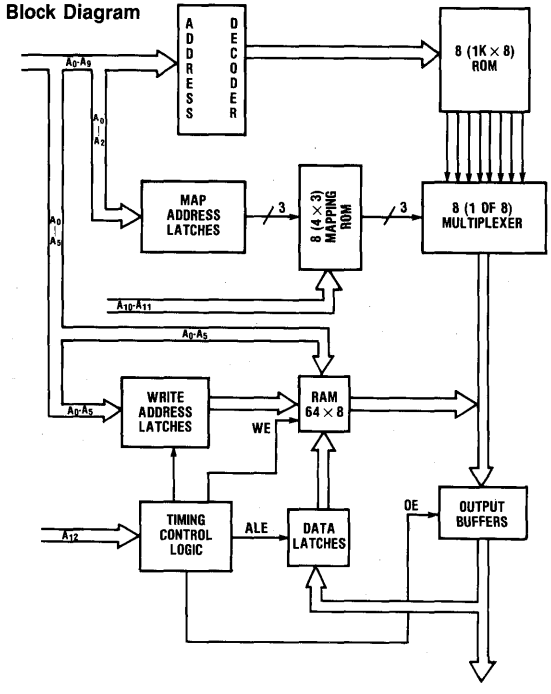
General Description

The AMI S6464 is a ROM/RAM device with 65,536 bits of static mask programmable NMOS ROM and 512 bits of NMOS RAM. The ROM is organized as eight 1K × 8 blocks of data while the RAM organization is 64 × 8.

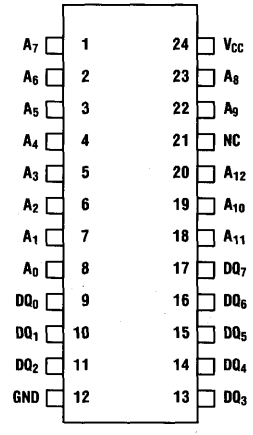
The S6464 is fabricated using AMI's Late Mask Programmable NMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Designed for systems that can access only 4K bytes of ROM, the S6464 contains a 32 × 3 user programmable mapping ROM that allows access to the full 8K of the main ROM. A single 5V supply is required; all inputs and outputs are fully TTL compatible. The outputs can be tri-stated for write operations with an output enable generated internally from the address inputs. No external clocks or control signals are necessary. Deskewing circuitry is also included to prevent false mode selection caused by address skew.

Block Diagram



Pin Configuration



Pin Names

A_0-A_9	ROM Address Inputs
A_0-A_5	RAM Address Inputs
DQ_0-DQ_7	RAM/ROM Outputs
V_{CC}, GND, NC	+5V, Ground, No Connect

Absolute Maximum Ratings*

Ambient Temperature	0°C to +60°C
Storage Temperature	−65°C to +150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	440mW

*COMMENTS: Stresses above those lised under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A = +10°C to +50°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = +1.6mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.4		V_{CC}	V	
I_{LI}	Input Leakage Current			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current			±10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current			80	mA	V_{CC} = 5.5 at T_A = 25°C

Switching Characteristics: V_{CC} = +5V ± 10%, T_A = +10°C to +50°C

Symbol	Parameters	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Access Time			450	nsecs	
t_{ON}	A_{12} to Data Active	120			nsecs	See A.C. Test
t_{AH}	Address to Data Hold	0			nsecs	Conditions and
t_{OFF}	Address Deselect Time			225	nsecs	Waveforms
t_{DW}	Valid Data Pulse Width	300			nsecs	
t_{DH}	Valid Data to Address Hold			100	nsecs	
t_{DS}	Valid Data to Address Set Up	300			nsecs	
t_{CYC}	Cycle Time	550	820		nsecs	

Capacitance: T_A = 25°C, f = 1.0MHz

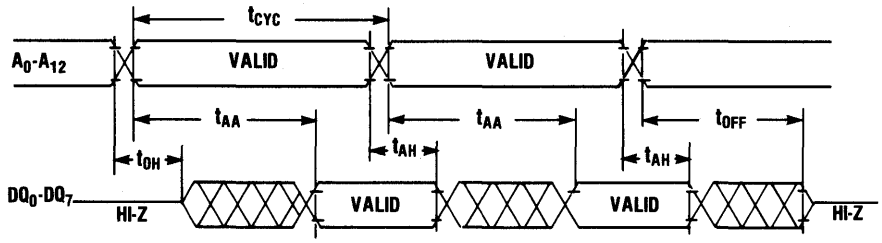
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			12.5	pF	V_{OUT} = 0V

A.C. Test Conditions

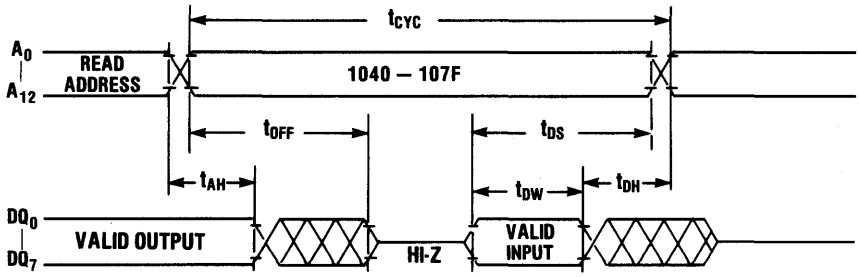
Input Pulse Levels	0.8V and 2.4V
Input Rise and Fall Times	⩽20ns
Input Timing Level	0.8V and 2.4V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 40pF

Waveforms

A: READ CYCLE (ROM OR RAM)



B: WRITE CYCLE (RAM ONLY)



Device Features

A. Internal Organization

General: The two basic components of the S6464 are a 65,536 bit ROM, with its associated mapping ROM, and a 512 bit RAM. The ROM is organized as eight pages of 1K × 8 bits each. External addresses A_0-A_9 control access to the data, within a selected 1K × 8 page. The 1-of-8 page selection is controlled by the outputs from the 32 × 3 mapping ROM.

Mapping ROM: The mapping ROM has 32 words, which are user programmable to allow optional use of the eight pages in the main ROM. These 32 words are accessed by two external addresses, A_{10} and A_{11}, and three internal signals as stored in the map address latches (see Figure 1).

The 32 words are subdivided into eight maps of four words each as shown in Figure 1. The three internal signals, corresponding to the previously latched data from A_0-A_2 control the map selection. A_{10} and A_{11} control 1-of-4 selection within each map. Each word in the mapping ROM can be programmed independently of all other words. Each word contains three programmable bits corresponding to eight pages (0-7) in the main ROM.

RAM: The RAM is organized as 64 × 8, with addresses A_0-A_5 controlling the byte selection and A_6 controlling the read/write selection. All other addresses must be applied as shown in Figure 2, for selecting the RAM. Note that the RAM address space overlays some of the ROM address space controlled by the mapping ROM for the case of $A_{10} = A_{11} = 0$. These "masked" ROM bytes are uncovered by simply programming the mapping ROM to access the appropriate 1K × 8 page in an additional mapping ROM location, for which either A_{10} or $A_{11} = 1$.

B. Operation

Address Space: Six modes of operation are active on the S6464. These modes are selected only by the external address signals (see Figure 2). No other control signals (CS, CE, OE, R/W, etc) are needed. All other addresses within the total address space of 0000 — 1FFF have no effect except of placing the device into an output High-Z condition.

Load Map Latch Immediate: External addresses A_0-A_2 are stored in the address map latches. During the next ROM Read cycle, the new latched data controls the map selection within the mapping ROM. Note that A_{10} and A_{11} can freely access one of the four pages within the selected map, but one of the Load Map Latch operations has to be used to change maps.

Load Map Latch Delayed: This operation is the same as the Load Map Latch Immediate one, in that the addresses A_0-A_2 are loaded immediately. However, the change on the mapping ROM is effective not in the next address cycle, but rather in the fourth cycle following the Load Map Latch Delayed cycle. This allows the three intervening cycles to be used for an additional microprocessor operation such as a jump instruction.

Figure 1.

		MAP 0	MAP 1	MAP 2	MAP 3	MAP 4	MAP 5	MAP 6	MAP 7
A_2		0	0	0	0	1	1	1	1
A_1		0	0	1	1	0	0	1	1
A_0		0	1	0	1	0	1	0	1
A_{11}	A_{10}	WORD							
0	0	0	4	8	12	16	20	24	28
0	1	1	5	9	13	17	21	25	29
1	0	2	6	10	14	18	22	26	30
1	1	3	7	11	15	19	23	27	31
									WORD

NOTE: Decimal numbers 0—31 represent 'Words'.

Figure 2.

Address (Hexadecimal Notation)	Mode
0030 — 0037	Load Map Latch Immediate (with A_0 — A_2)
0038 — 003F	Load Map Latch Delayed (with A_0 — A_2)
1000 — 103F	RAM Read
1040 — 107F	RAM Write
1080 — 1FFF	ROM Read
1FFC	Clear Map Latch

RAM Read or Write: Addresses A_0-A_5 access 1 of 64 bytes of RAM storage. A_6 determines whether the operation is Read (A_6 = 0) or Write (A_6 = 1). A RAM Write operation must be followed by any operation other than "RAM Write"; RAM read is allowed.

ROM Read: Addresses A_{10} and A_{11} determine the selection of one of the four possible pages within a preselected map. Within the selected page, A_0-A_9 select the desired byte. For any particular map selected within the mapping ROM, any one of the possible 4K bytes can be read out by a ROM Read operation. The only exception is that the first 128 bytes in each map are "masked" by the RAM Read or RAM Write address locations.

Clear Map Latch: This operation initializes all internal logic, primarily for ease of reset during power on of a system. As A_{10} = A_{11} = 1 and the outputs of the map address latches are all at '0', the last page in the first map of the mapping ROM is selected. The outputs of the mapping ROM correspond to Word 3 in Figure 1.

ROM Code Data

AMI's preferred method of receiving ROM Code Data is in EPROM. Two sets of EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROMs, transfer this data to disk and then program the blank EPROMs from the stored information. This procedure guarantees that the EPROMs have been properly entered into the AMI computer system. The AMI programmed EPROMs are returned to the customer for verification of the ROM program. Unless otherwise requested, AMI will not proceed until the customer verifies the program in the returned EPROMs.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 2-68A764

If multiple EPROMs are used to specify one ROM pattern, an equal number of blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark each EPROM with the ROM address (in Hex) where the EPROM data is to be located.

For the EPROM containing the data for the mapping ROM, the data should be the first 32 bytes of the EPROM.

Pattern Data From ROMs

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device.

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

9 Track NRZ Magnet Tape
Paper Tape
Card Deck

*Consult AMI sales for format.

AMI

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S23128A/S23128B**

131,072 BIT (16384x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S23128A-350ns Maximum
  S23128B-250ns Maximum
- ☐ Low Standby Power: 110mW Max.
- ☐ Fully Static Operation
- ☐ Single +5V ± 10% Power Supply
- ☐ Directly TTL Compatible Outputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Enables/Selects
- ☐ EPROM Pin Compatible (27128)
- ☐ Late Mask Programmable
- ☐ Programmable Output/Chip Enable

General Description

The AMI S23128 is a 131,072 bit static mask programmable NMOS ROM organized as 16,384 words by 8 bits.

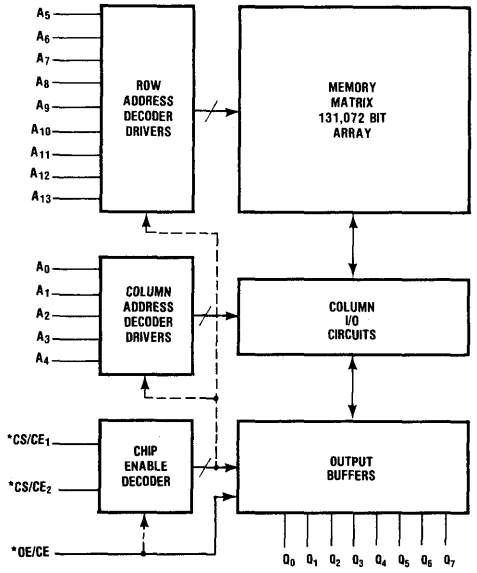
The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S23128 is pin compatible with the 27128 EPROM making system development easier and more cost effective. The fully static S23128 requires no clocks for operation. The three control pins are mask programmable with the active level and function being specified by the user. The pins can also be programmed as no connections. If CE functions are selected, automatic powerdown is available. The power supply current is reduced to 20mA when the chip is disabled.

The S23128 is fabricated using AMI's NMOS technology. This permits the manufacture of high density, high performance ROMs.

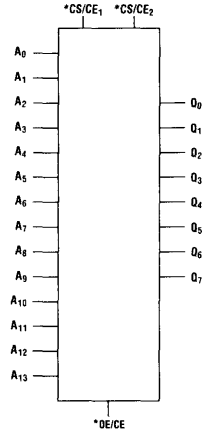
MEMORIES

Block Diagram

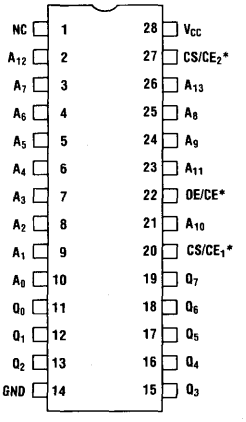


* THE USER DECIDES BETWEEN A CS OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL FOR CS/CE AND OE/CE.

Logic Symbol



Pin Configuration



Pin Names

A_0-A_{13}	Address Inputs
Q_0-Q_7	Data Outputs
CS/CE_1-CS/CE_2	Chip Selects/Enables
OE/CE	Output Enable/Chip Enable
V_{CC};GND;NC	5V;Ground; No Connect

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin With Respect to Ground	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Electrical Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −400μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current	−10		10	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current	−10		10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			40	mA	See Note #1
I_{SB}	Power Supply Current—Standby			20	mA	See Note #2

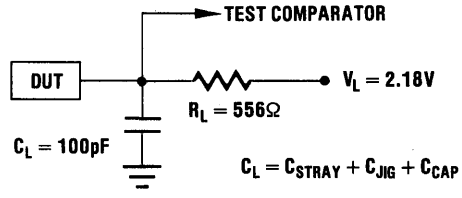
Capacitance: T_A = 25°C, f = 1.0MHz (See Note #3)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

Switching Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to 70°C

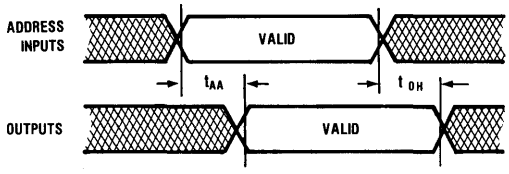
Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S23128A S23128B			350 250	ns	See Waveforms and Test Load
t_{ACE}	Chip Enable Access Time	S23128A S23128B			350 250	ns	
t_{ACS}	Chip Select Access Time	S23128B S23128B			120 80	ns	
t_{OEA}	Output Enable Access Time	S23128A S23128B			120 80	ns	
t_{OFF}	Chip Deselect Time	S23128A S23128B			120 80	ns	See Note #3
t_{CEO}	Disable Time From Chip Enable	S23128A S23128B			120 80	ns	
t_{OEO}	Disable Time From Output Enable	S23128A S23128B			120 80	ns	See Note #3
t_{OH}	Output Hold Time	S23128A S23128B	0 0			ns	

Test Load

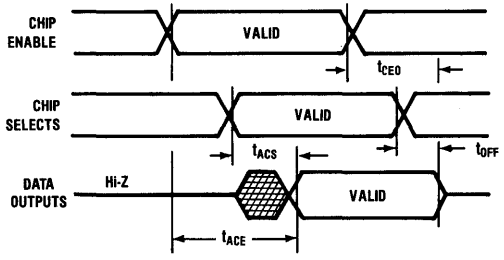


Waveforms

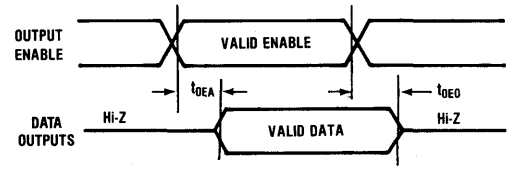
ADDRESS TO OUTPUT DELAY (CHIP SELECTED)



CHIP ENABLE/SELECT TO OUTPUT DELAY (ADDRESS VALID)



OUTPUT ENABLE TO OUTPUT DELAY (ADDRESS VALID/CHIP SELECTED)



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 1-27128; Optional 2-2764

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

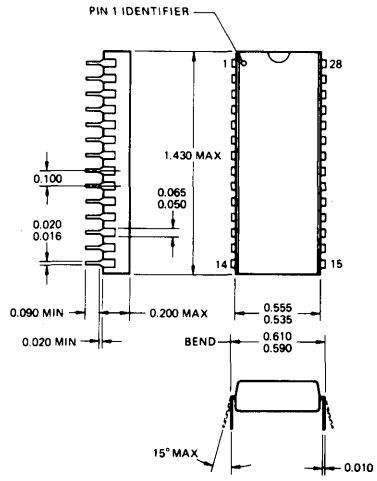
If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitor's ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Notes:

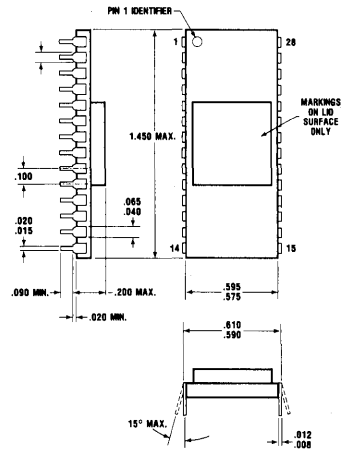
1. Power Test Active Conditions: $V_{CC} = V_{CC}$ Max, CE/CS = Active Level @ V_I Address Pins = V_{IL}, Output Load Disconnected
2. Power Test Standby Conditions: Same as active except CE Deselected
3. Guaranteed by Design

Package Outlines

28-Pin Plastic



28-Pin Ceramic



Truth Table: (For simplicity, all control functions in the Truth Table are defined as active high).

CS/CE1	CS/CE2	OE/CE	Outputs	Power
$\overline{CE1}$	X	X	Hi-Z	Standby
X	$\overline{CE2}$	X	Hi-Z	Standby
X	X	$\overline{CE}$	Hi-Z	Standby
$\overline{CS1}$	CS/CE2	OE/CE	Hi-Z	Active
CS/CE1	$\overline{CS2}$	OE/CE	Hi-Z	Active
CS/CE1	CS/CE2	$\overline{OE}$	Hi-Z	Active
CS/CE1	CS/CE2	OE/CE	Data Out	Active

Pins	Control Functions Available
27	CS2, $\overline{CS2}$, CE2, $\overline{CE2}$, DC
22	OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20	CS1, $\overline{CS1}$, CE1, $\overline{CE1}$, DC

The user decides between a CS/CE and OE/CE function and then defines the active level. The functions may also be defined as Don't Care (DC). The chip is enabled when the inputs match the user defined states. Don't Care pins are still connected to input protection diodes and are subject to the "Absolute Maximum Ratings"

AMI®

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S23256B/S23256C**

262,144 BIT (32,768x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time:
  S23256B: 250ns Maximum
  S23256C: 150ns Maximum
- ☐ Low Power Dissipation
  Active Current:
  40mA Maximum
  Standby Current: 10mA Maximum
- ☐ Fully Static Operation
- ☐ Two User-Defined and Programmable Control Lines: CE/CS, OE/CE
- ☐ EPROM Pin Compatible
- ☐ Late Mask Programmable
- ☐ Three-State TTL Compatible Outputs

General Description

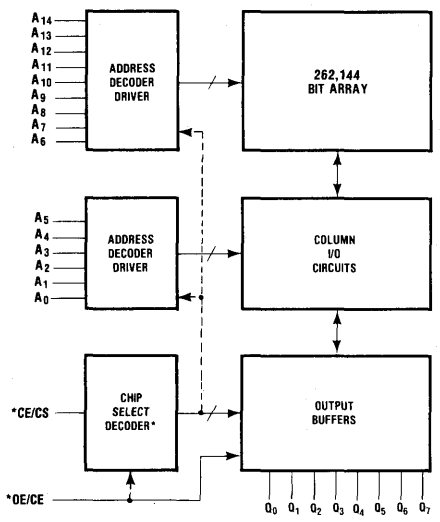
The AMI S23256 is a 262,144 bit static mask programmable NMOS ROM organized as 32,768 words by 8 bits. The devices are fully TTL compatible on all inputs and outputs and operate from a single +5V ±10% power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S23256 is pin compatible with the 27128 UV EPROM making system development much easier and more cost effective. It is fully static, requiring no clocks for operation.

The S23256 is fabricated using AMI's N-Channel MOS ROM technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

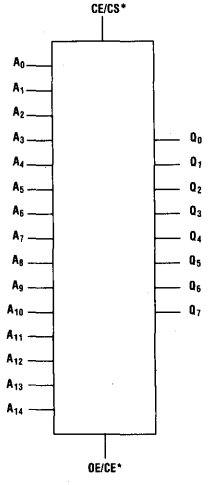
MEMORIES

Block Diagram

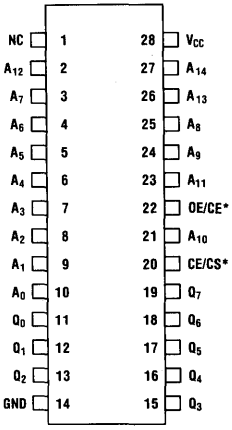


*THE USER DECIDES BETWEEN A CE OR CS AND OE OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{14}	Address Inputs
Q_0—Q_7	Data Outputs
CE/CS	Chip Enable/Chip Select
OE/CE	Output/Chip Enable
V_{CC};GND;NC	5V;Ground;No Connect

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	μA	V_{IN} = 0V to V_{CC}
$\|I_{LO}\|$	Output Leakage Current			10	μA	V_O = 0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			40	mA	Chip Enabled
I_{SB}	Power Supply Current—Standby			10	mA	Chip Disabled

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

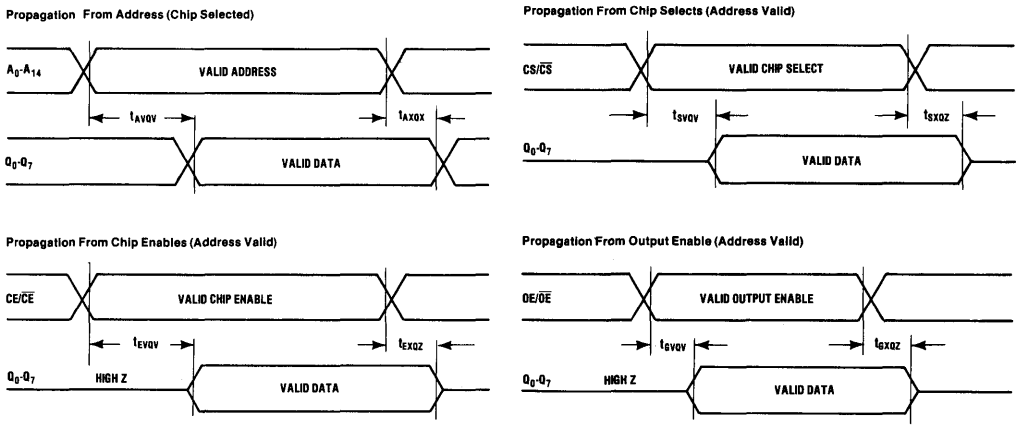
A.C. Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Address Access Time S23256B S23256C			 250 150	ns	See A.C. Test Conditions and Waveforms
t_{EVQV}	Chip Enable Access Time S23256B S23256C			 250 150	ns	
t_{SVQV}	Chip Select Access Time S23256B S23256C			 120 80	ns	
t_{GVQV}	Output Enable Access Time S23256B S23256C			 120 80	ns	
t_{AXQX}	Output Hold/Address Change S23256B S23256C	 10 10			ns	
t_{EXQZ} t_{SXQZ} t_{GXQZ}	Deselect Times S23256B S23256C			 120 80	ns	

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 2-27128

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* Consult AMI sales office for format.

Truth Table

CE/CS	OE/CE	OUTPUTS	POWER
CE/CS	OE/CE	DATA OUT	ACTIVE
$\overline{CE}$	X	HIGH Z	STANDBY
$\overline{CS}$	X	HIGH Z	ACTIVE
X	$\overline{OE}$	HIGH Z	ACTIVE
X	$\overline{CE}$	HIGH Z	STANDBY

THE DEVICE IS ENABLED WHEN THE CONTROL LINES MATCH THE USER DEFINED STATES.

AMI®

A Subsidiary
of Gould Inc.

S6800

MICROPROCESSOR COMPONENT FAMILY

Contact factory for complete data sheet

S6800 Family Selection Guide

MICROPROCESORS

S6800/S68A00/S68B00	8-Bit Microprocessor (1.0/1.5/2.0MHz Clock)
S6801/S6803	Single Chip Microcomputer 2K ROM, 128 x 8 RAM, 31 I/O Lines, Enhanced Instruction. S6803 is a S6801 Without ROM (N/R Model-No ROM and RAM)
S6802/A/B/S6808/A/B	Microprocessor with Clock and RAM (1.0/1.5/2.0MHz Clock (S6808 Models—No RAM)
S6803/S6803N/R	S6801 Without ROM (N/R Model—No ROM and RAM)
S6805	Single Chip Microcomputer 1.1K x 8 ROM, 64 x 8 RAM, Timer, Pre-scaler, Bit Level Instructions.
S6809(E)/S68A09(E)/S68B09(E)	Pseudo 16-Bit Microprocessor (1.0/1.5/2.0MHz Clock) (E Models—External Clock Mode)

PERIPHERALS

S1602	Universal Asynchronous Receiver/Transmitter (UART)
S2350	Universal Synchronous Receiver/Transmitter (USRT)
S6551/S6551A	UART With Baud Rate Generator
S6821/S68A21/S68B21	Peripheral Interface Adapter (PIA) (1.0/1.5/2.0MHz Clock)
S6840/S68A40/S68B40	Programmable Timer (1.0/1.5/2.0MHz)
S68045	CRT Controller (CRTC)
S6846	2K ROM, Parallel I/O, Programmable Timer
S6850/S68A50/S68B50	Asynchronous Communication Interface Adapter (ACIA)
S6852/S68A52/S68B52	Synchronous Serial Data Adapter (SSDA) (1.0/1.5/2.0MHz Clock)
S6854/S68A54/S68B54	Advanced Data Link Controller (ADLC) (1.0/1.5/2.0MHz Clock)

MEMORIES

S6810/S68A10/S68B10	128 x 8 Static RAM (450/360/250ns Access Time)

AMI®

A Subsidiary of Gould Inc.

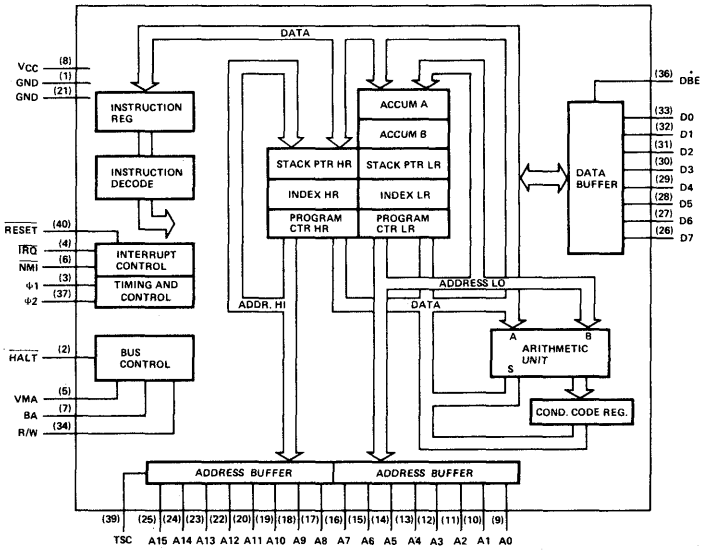
S6800/S68A00/S68B00

8-BIT MICROPROCESSOR

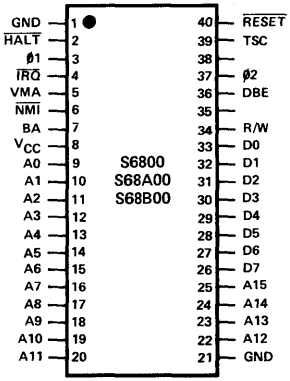
Features

- ☐ Eight-Bit Parallel Processing
- ☐ Bi-Directional Data Bus
- ☐ Sixteen-Bit Address Bus — 65536 Bytes of Addressing
- ☐ 72 Instructions — Variable Length
- ☐ Seven Addressing Modes — Direct, Relative Immediate, Indexed, Extended, Implied and Accumulator
- ☐ Variable Length Stack
- ☐ Vectored Restart
- ☐ 2 Microsecond Instruction Execution
- ☐ Maskable Interrupt Vector
- ☐ Separate Non-Maskable Interrupt — Internal Registers Saved in Stack
- ☐ Six Internal Registers — Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- ☐ Direct Memory Access (DMA) and Multiple Processor Capability
- ☐ Clock Rates — S6800 — 1.0MHz
  — S68A00 — 1.5MHz
  — S68B00 — 2.0MHz
- ☐ Simple Bus Interface Without TTL
- ☐ Halt and Single Instruction Execution Capability

Block Diagram



Pin Configuration



S6800 FAMILY

Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3 to +7.0V
Input Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

Electrical Characteristics

(V_{CC} = 5.0V, ±5%, V_{SS} = 0, T_A = 0 to +70°C unless otherwise noted.)

Symbol	Characteristics		Min.	Typ.	Max.	Unit
V_{IH} V_{IHC}	Input High Voltage (Normal Operating Levels)	Logic $\phi1$, $\phi2$	V_{SS} +2.0 V_{CC} −0.6	— —	V_{CC} V_{CC} +0.3	Vdc
V_{IL} V_{ILC}	Input Low Voltage (Normal Operating Levels)	Logic $\phi1$, $\phi2$	V_{SS} −0.3 V_{SS} −0.3	— —	V_{SS} +0.8 V_{SS} +0.4	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max) (V_{IN} = 0 to 5.25V, V_{CC} = 0.0V)	 Logic* $\phi1$, $\phi2$	 — —	 1.0 —	 2.5 100	μAdc
I_{TSI}	Three-State (Off State) Input Current V_{IN} = 0.4 to 2.4V, V_{CC} = Max	D0 — D7 A0 — A15, R/W	— —	2.0 —	10 100	μAdc
V_{OH}	Output High Voltage (I_{LOAD} = 205μAdc, V_{CC} = Min) (I_{LOAD} = 145μAdc, V_{CC} = Min) (I_{LOAD} = −100μAdc, V_{CC} = Min)	 D0 — D7 A0 — A15, R/W, VMA BA	 V_{SS} +2.4 V_{SS} +2.4 V_{SS} +2.4	 — —	 — —	Vdc
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = Min)		—	—	V_{SS} +0.4	Vdc
P_D	Power Dissipation		—	0.5	1.0	W
C_{IN}	Capacitance# (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	 $\phi1$ $\phi2$ D0 — D7 Logic Inputs	 — — — —	 — — 10 6.5	 35 70 12.5 10	pF
C_{OUT}		A0 — A15, R/W, VMA	—	—	12	pF
f	Frequency of Operation	S6800 S68A00 S68B00	0.1 0.1 0.1	— — —	1.0 1.5 2.0	MHz
t_{CYC}	Clock Timing (Figure 1) Cycle Time	S6800 S68A00 S68B00	1.000 0.666 0.50	— — —	10 10 10	μs
$PW_{\phi H}$	Clock Pulse Width Measured at V_{CC} − 0.6V	$\phi1$, $\phi2$ — S6800 $\phi1$, $\phi2$ — S68A00 $\phi1$, $\phi2$ — S68B00	400 230 180	— — —	9500 9500 9500	ns ns
t_{UT}	Total $\phi1$ and $\phi2$ Up Time	S6800 S68A00 S68B00	900 600 440	— — —	— — —	ns
$t_{\phi r}$, $t_{\phi f}$	Measured between V_{SS} +0.4 and V_{CC} −0.6	Rise and Fall Times		—	100	ns
t_d	Measured at V_{OV} = V_{SS} +0.6V	Delay Time or Clock Separation	0	—	9100	ns

*Except $\overline{IRQ}$ and $\overline{NMI}$, Which require kΩ pullup load resistor for wire-OR capability at optimum operation.
#Capacitances are periodically sampled rather than 100% tested.

Read/Write Timing

Symbol	Characteristics	S6800			S68A00			S68B00			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AD}	Address Delay										ns
	C = 90pF	—	—	270	—	—	180	—	—	150	
	C = 30pF	—	—	250	—	—	165	—	—	135	
t_{ACC}	Periph. Read Access Time $t_{AC} = t_{UT} - (t_{AD} + t_{DSR})$	530	—		360	—		250	—		ns
t_{DSR}	Data Setup Time (Read)	100	—	—	60	—	—	40	—	—	ns
t_H	Input Data Hold Time	10	—	—	10	—	—	10	—	—	ns
t_H	Output Data Hold Time	10	25	—	10	25	—	10	25	—	ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	30	50	—	30	50	—	30	50	—	ns
t_{EH}	Enable High Time for DBE Input	450	—	—	280	—	—	220	—	—	ns
t_{DDW}	Date Delay Time (Write)	—	—	225	—	165	200	—	—	160	ns
	Processor Controls										
t_{PCS}	Proc. Control Setup Time	200	—	—	140	—	—	110	—	—	ns
t_{PCr}; t_{PCf}	Processor Control Rise and Fall Time	—	—	100	—	—	100	—	—	100	ns
t_{BA}	Bus Available Delay	—	—	250	—	—	165	—	—	135	ns
t_{TSE}	Three-State Enable	—	—	40	—	—	40	—	—	40	ns
t_{TSD}	Three-State Delay	—	—	270	—	—	270	—	—	270	ns
$t_{\overline{DBE}}$	Data Bus Enable Down Time During $\phi 1$ Up Time	150	—	—	120	—	—	75	—	—	ns
t_{DBEr}, t_{DBEf}	Data Bus Enable Rise and Fall Times	—	—	25	—	—	25	—	—	25	ns

Figure 1. Clock Timing Waveform

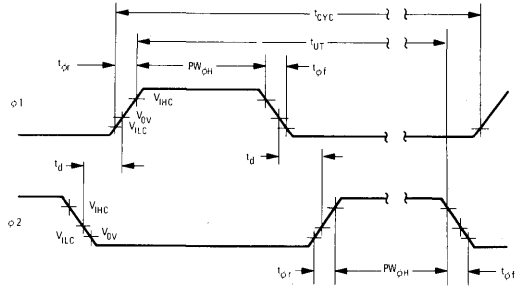
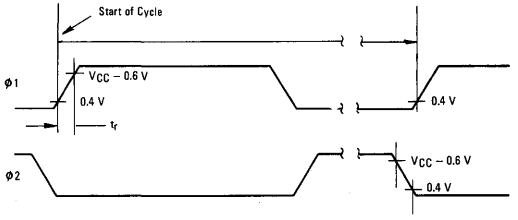


Figure 2. Read/Write Timing Waveform



Measurement point for $\phi 1$ and $\phi 2$ are shown above. Other measurements are the same as for MC6800.

Figure 3. Read Data from Memory or Peripherals

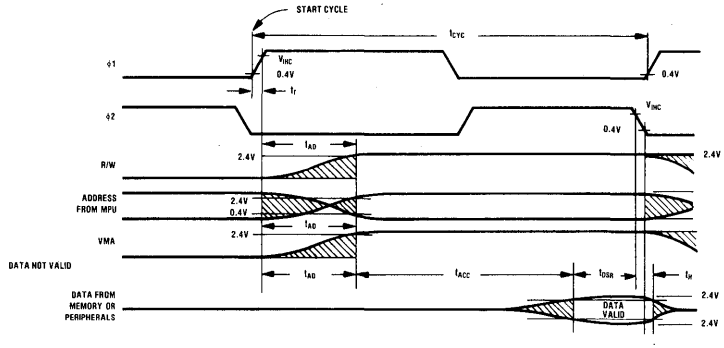


Figure 4. Write Data in Memory or Peripherals

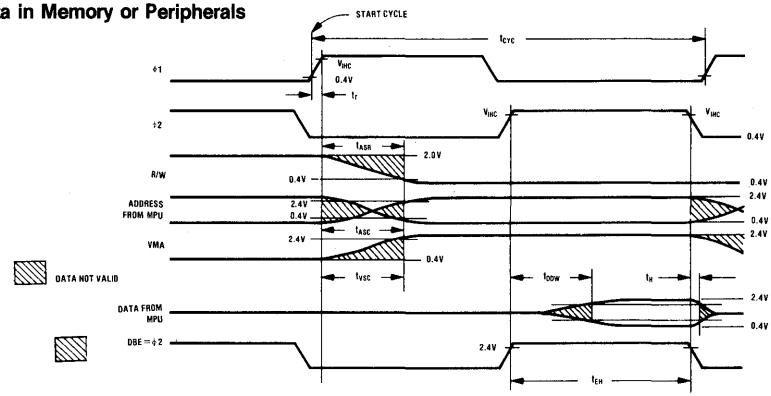
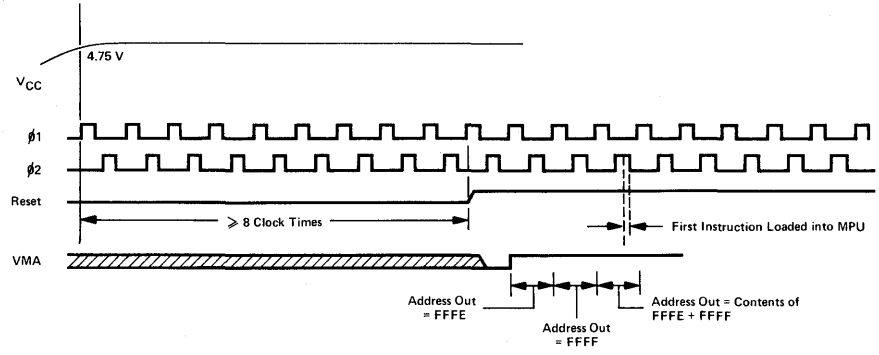


Figure 5. Initialization of MPU After Restart



Interface Description

Label	Pin	Function
ϕ1 ϕ2	(3) (37)	**Clocks Phase One and Phase Two** — Two pins are used for a two-phase non-overlapping clock that runs at the V_{CC} voltage level.
$\overline{\text{RESET}}$	(40)	**$\overline{\text{Reset}}$** — this input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. $\overline{\text{Reset}}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts (Figure 4). If $\overline{\text{Reset}}$ goes high prior to the leading edge of ϕ2, on the next ϕ1 the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.
VMA	(5)	**Valid Memory Address** — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 30pF may be directly driven by this active high signal.
A0 • • • A15	(9) (25)	**Address Bus** — Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.
TSC	(39)	**Three-State Control** — This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 500ns after TSC = 2.4V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The ϕ1 clock must be held in the high state and the ϕ2 in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 50μs or destruction of data will occur in the MPU.
D0 • • D7	(33) (26)	**Data Bus** — Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load at 130pF.
DBE	(36)	**Data Bus Enable** — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it can be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.
R/W	(34)	**Read/Write** — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will Read/Write to the off (high-impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 130pF.
$\overline{\text{HALT}}$	(2)	**$\overline{\text{Halt}}$** — When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction. Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode.

Label	Pin	Function
		Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250ns of phase one. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one Phase One Clock cycle.
BA	(7)	**Bus Available** — The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or non-maskable interrupt. This output is capable of driving one standard TTL load and 30pF.
$\overline{\text{IRQ}}$	(4)	**Interrupt Request** — This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An adress loaded at these locations causes the MPU to branch to an interrupt routine in memory. The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be recognized. The $\overline{\text{IRQ}}$ has a high impedance pullup device internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.
$\overline{\text{NMI}}$	(6)	**Non-Maskable Interrupt** —A low-going edge on this input requests that a non-mask interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away in the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory. $\overline{\text{NMI}}$ has a high impedance pullup resistor internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts. Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are acknowledged during $\phi 2$ and will start the interrupt routine on the $\phi 1$ following the completion of an instruction. **INTERRUPTS** — As outlined in the interface description the S6800 requires a 16-bit vector address to indicate the location of routines for Restart, Non-maskable Interrupt, and Maskable Interrupt. Additionally an address is required for the Software Interrupt Instruction (SWI). The processor assumes the uppermost eight memory locations, FFF8 — FFFF, are assigned as interrupt vector addresses as defined in Figure 6. After completing the current instruction execution the processor checks for an allowable interrupt request via the $\overline{\text{IRQ}}$ or $\overline{\text{NMI}}$ inputs as shown by the simplified flow chart in Figure 7. Recognition of either external interrupt request or a Wait for Interrupt (WAI) or Software Interrupt (SWI) instruction causes the contents of the Index Register, Program Counter, Accumulators and Condition Code Register to be transferred to the stack as shown in Figure 8.

AMI®

A Subsidiary of Gould Inc.

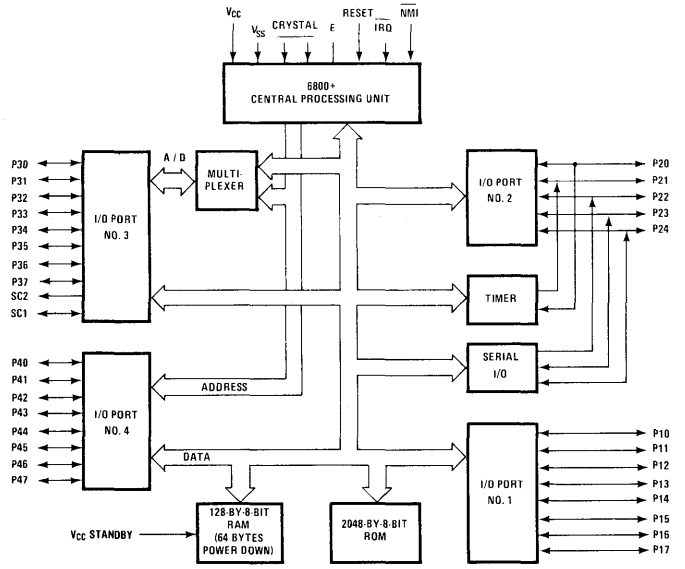
S6801/S6803

SINGLE CHIP MICROCOMPUTER

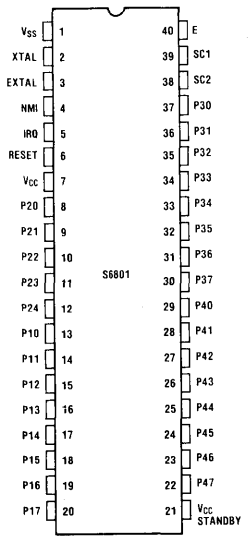
Features

- ☐ Instruction and Addressing Compatible
- ☐ Object Code Compatible
- ☐ 16-Bit Programmable Timer
- ☐ Single Chip or Expandable to 65K Words
- ☐ On-Chip Serial Communications Interface (SCI)
  - — Simplex
  - — Half Duplex
    Mark/Space (NRZ)
    Biphase (FM)
  - — Port Expansion
    Full/Half Duplex
- ☐ Four Internal Baud Rates Available
  $\phi 2 \div 16, 128, 1024, 4096$
- ☐ 2K Bytes of ROM
- ☐ 128 Bytes of RAM
  (64 Bytes Power Down Retainable)
- ☐ 31 Parallel I/O Lines
- ☐ Divide-by-Four Internal Clock
- ☐ Hardware 8 x 8 Multiply
- ☐ Three Operating Modes
  - — Single Chip
  - — Expanded Multiplex (up to 65K Addressing)
  - — Expanded Non-Multiplex
- ☐ Expanded Instruction Set
- ☐ Interrupt Capability
- ☐ Low Cost Versions
  - — S6803—No ROM Version
  - — S6803NR—No ROM or RAM
- ☐ TTL-Compatible with Single 5 Volt Supply

Block Diagram



Pin Configuration



S6800 FAMILY

General Description

The S6801 MCU is an 8-bit single-chip microcomputer system which is compatible with the S6800 family of parts. The S6801 is object code compatible with the S6800 instruction set.

The S6801 features improved execution times of key S6800 instructions including Jump to Subroutine (JSR) and all Conditioned Branches (BRA, etc.). In addition, several new 16-bit and 8-bit instructions have been added including Push/Pull to/from Stack, Hardware 8 × 8 Multiply, and store concatenated A and B accumulators (D accumulator).

The S6801 MCU can be operated in three modes: Single-Chip, Expanded Multiplex (up to 65K Byte Addressing), and Expanded Non-Multiplex. In addition, the S6801 is available with two mask options: an on-chip (÷4) Clock, or an external (÷1) Clock. The external mode is especially useful in Multiprocessor Applications. The S6801E can be configured as a peripheral by using the Read/Write (R/W), Chip Select (CS), and Register Select (RS). The Read/Write line controls the direction of data on Port 3 and the Register Select (RS) allows for access to either Port 3 data register or control register.

The S6801 Serial Communications Interface (SCI) permits full serial communication using no external components in several operating modes — Full and/or Half Duplex operation — and two formats — Standard Mark/Space for typical Terminal/Modem interfaces and the Bi-Phase (FM, F2F, and Manchester) Format primarily for use between processors. Four software addressable registers are provided to configure the Serial Port; to provide status information; and as transmit/receive data buffers.

The S6801 includes a 16-bit timer with three effectively independent timing functions: (1) Variable pulse width measurement, (2) Variable pulse width generation, and (3) A Timer Overflow — Find Time Flag. This makes the S6801 ideal for applications such as Industrial Controls, Automotive Systems, A/D or D/A Converters, Modems, Real-Time Clocks, and Digital Voltage Controlled Oscillators (VCO).

The S6801 is fully TTL-compatible and requires only a single +5 volt supply.

The S6803 can be thought of as an S6801 operating in expanded multiplexed mode with no ROM. The S6803NR is comparable to the S6801 operating in expanded multiplexed mode with no RAM and no ROM.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature Range, T_A	0° to +70°C
Storage Temperature Range, T_{stg}	−55°C to +150°C
Thermal Resistance, θ_{JA}	
Plastic	100°C/W
Ceramic	50°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$.

Electrical Operating Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0 to +70°C, unless otherwise noted)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage* Reset	$V_{SS}+2.0$ $V_{SS}+4.0$		V_{CC} V_{CC}	Vdc
V_{IL}	Input Low Voltage	$V_{SS}-0.3$		$V_{SS}+0.8$	Vdc
I_{TSI} I_{TSI}	Three-State (Off State) Input Current P10-P17, P30-P37 (V_{IN} = 0.5 to 2.4 Vdc) P20-P24		2.0 10.0	10 100	μAdc μAdc
V_{OH}	Output High Voltage All Outputs Except XTAL 1 and EXTAL 2 I_{LOAD} = −65μA P40-P47, E, SC1, SC2 I_{LOAD} = −100μA all others	$V_{SS}+2.4$			Vdc

* Except mode programming levels

Electrical Operating Characteristics (Continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{OL}	Output Low Voltage All Outputs Except XTAL 1 and EXTAL 2 $I_{LOAD} = 2.0mA$			$V_{SS} + 0.4$	Vdc
P_D	Power Dissipation			1200	mW
C_{IN}	Capacitance $V_{IN} = 0$, $T_A = 25°C$, $f = 1.0MHz$ P40-P47, P30-P37, SC1 Other Inputs			 12.5 10	pF
t_{PDSU}	Peripheral Data Setup Time (Figure 3)	200			ns
t_{PDH}	Peripheral Data Hold Time (Figure 3)	200			ns
t_{OSD1}	Delay Time, Enable Negative Transition to OS3 Neg. Trans.			1.0	μs
t_{OSD2}	Delay Time, Enable Neg. Trans. to OS3 Positive Transition			1.0	μs
t_{PWD}	Delay Time, Enable Negative Transition to Peripheral Data Valid (Figure 4)			350	ns
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral Data Valid (.7 V_{CC}, P20-P24 (Figure 4)			2.0	μs
I_{OH}	Darlington Drive Current $V_O = 1.5Vdc$ — P10-P17	−1.0	−2.5	−10	mAdc
V_{SBB} V_{SB}	Standby Voltage (Not Operating) (Operating)	4.00 4.75		5.25 5.25	Vdc

NOTE: The above electricals satisfy Ports 1 and 2 always, and Ports 3 and 4 in the single chip mode only.

Bus Timing (Figure 7)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{CYC}	Cycle Time	1000			ns
P_{WASH}	Address Strobe Pulse Width High	220			ns
t_{ASR}	Address Strobe Rise Time			25	ns
t_{ASF}	Address Strobe Fall Time			25	ns
t_{ASD}	Address Strobe Delay Time	100			ns
t_{ER}	Enable Rise Time			25	ns
t_{EF}	Enable Fall Time			25	ns
P_{WEH}	Enable Pulse Width High Time	450			ns
P_{WEL}	Enable Pulse Width Low Time	430			ns
t_{ASED}	Address Strobe to Enable Delay Time	90			ns
t_{AD}	Address Delay Time			270	ns
t_{DDW}	Data Delay Write Time			225	ns
t_{DSR}	Data Set-up Time	80			ns
t_{HR}	Hold Time Read	10			ns
t_{HW}	Hold Time Write	20			ns
t_{ADL}	Address Delay Time for Latch			200	ns
t_{AHL}	Address Hold Time for Latch	20			ns
t_{AH}	Address Hold Time	20			ns
t_{UT}	Total Up Time	750			ns

MCU Signal Description

This section gives a description of the MCU signals for the various modes. General pin assignments for the signals are shown on page 1. SC1 and SC2 are signals which vary with the mode that the chip is in. Table 1 gives a summary of their function.

Table 1. Mode and Port Summary

MODE	PORT 1 EIGHT LINES	PORT 2 FIVE LINES	PORT 3 EIGHT LINES	PORT 4 EIGHT LINES	SC1	SC2
SINGLE CHIP	I/O	I/O	I/O	I/O	IS3(I)	OS3(O)
EXPANDED MUX	I/O	I/O	ADDRESS BUS (A_0-A_7) DATA BUS D_0-D_7	ADDRESS BUS* (A_8-A_{15})	AS(O)	R/W(O)
EXPANDED NON-MUX	I/O	I/O	DATA BUS D_0-D_7	ADDRESS BUS* (A_0-A_7)	IOS(O)	R/W(O)

* THESE LINES CAN BE SUBSTITUTED FOR I/O (INPUT ONLY) STARTING WITH THE MOST SIGNIFICANT ADDRESS LINE

I = INPUT
O = OUTPUT
R/W = READ/WRITE
IS = INPUT STROBE
OS = OUTPUT STROBE
IOS = I/O SELECT
SC = STROBE CONTROL
AS = ADDRESS STROBE

Read/Write Timing for Ports 3 and 4 (Figures 1-2)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{AD}	Address Delay			270	ns
t_{ACC}	Peripheral Read Access Time $t_{ACC}=t_{UT}-(t_{AD}+t_{DSR})$			530	ns
t_{DSR}	Data Setup Time (Read)	100			ns
t_{HR}	Input Data Hold Time	10			ns
t_{HW}	Output Data Hold Time	20			ns
t_{AH}	Address Hold Time (Address, R/W)	20			ns
t_{DDW}	Data Delay Time (Write)		165	225	ns
	Processor Controls				
t_{PCS}	Processor Control Setup Time	200			ns
t_{PCr}, t_{PCf}	Processor Control Rise and Fall Time (Measured between 0.8V and 2.0V)			100	ns

Port 3 Strobe Timing (Figure 5-6)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{DSD1}	Output Strobe Delay 1			100	μs
t_{OSD2}	Output Strobe Delay 2			100	μs
PW_{IS}	Input Strobe Pulse Width	200			ns
t_{IH}	Input Data Hold Time	20			ns
t_{IS}	Input Data Setup Time	100			ns

Figure 1. Read Data From Memory or Peripherals Expanded Non-Multiplexed

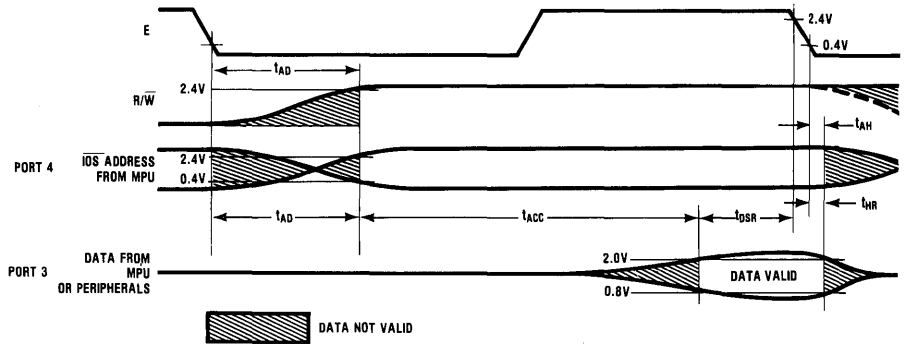
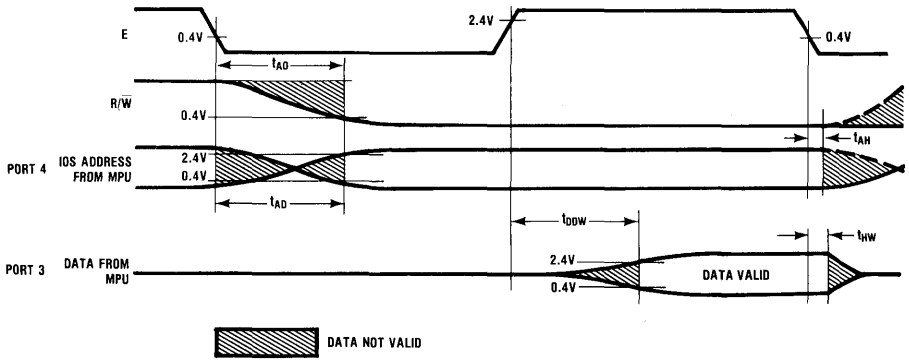


Figure 2. Write Data in Memory or Peripherals



Ports 1 and 2, and Ports 3 and 4 in the Single Chip Mode

Figure 3. Peripheral Data Setup and Hold Time (Read Mode)

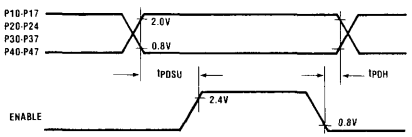
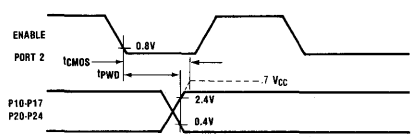


Figure 4. Peripheral CMOS Data Delay Times (Write Mode)



S6800 FAMILY

Figure 5. Output Strobe Timing — Single Chip Mode

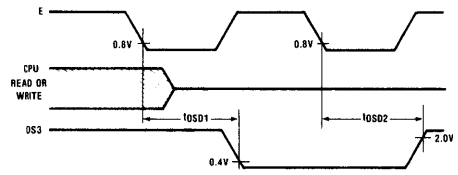


Figure 6. Input Strobe Timing — Single Chip Mode

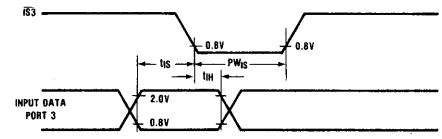


Figure 7. Multiplexed Bus Timing

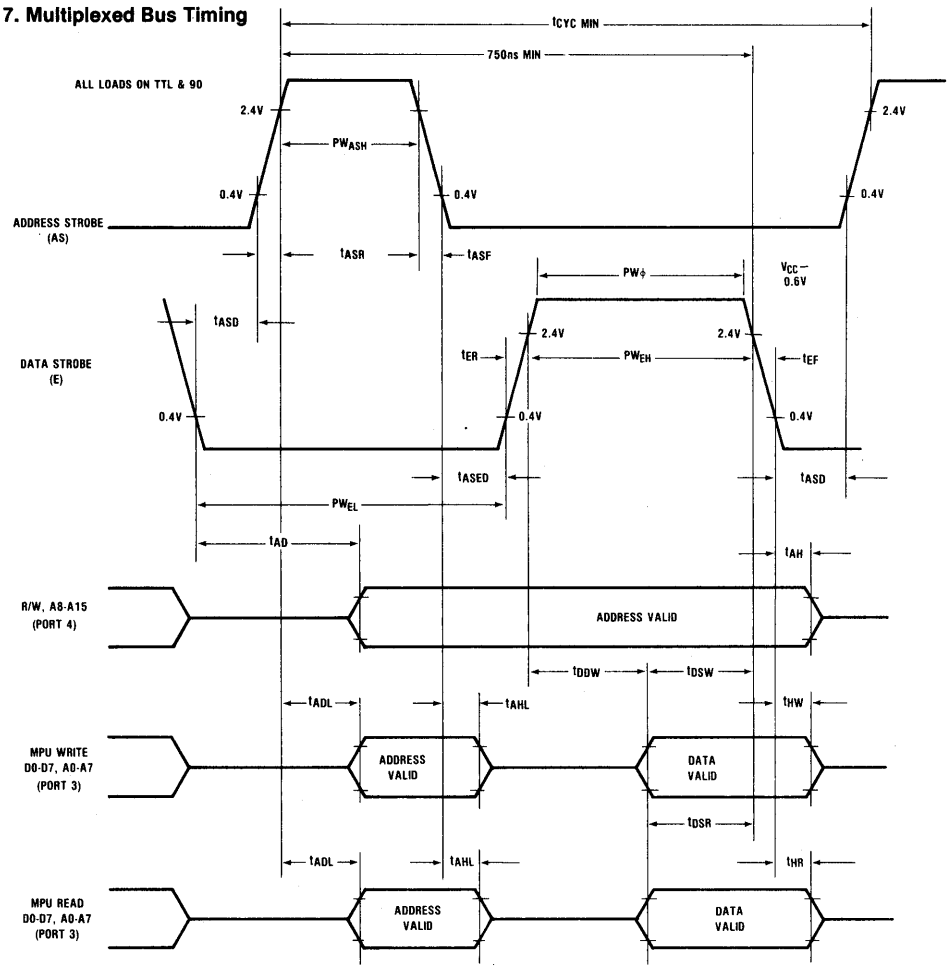


Figure 8. CMOS Load

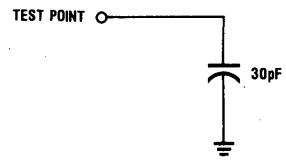
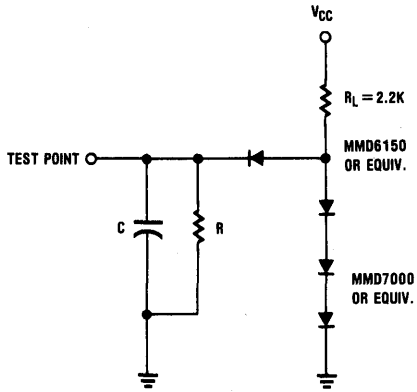
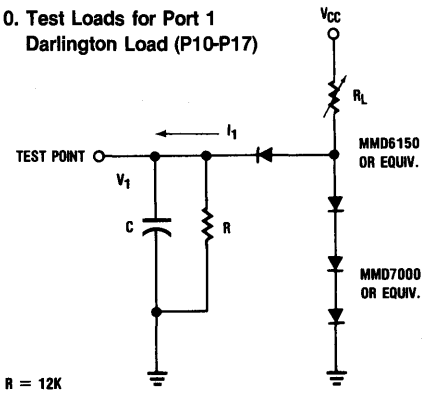


Figure 9. Bus Timing Test Load and Ports 1, 3 and 4 for Single Chip Mode



C = 90pF FOR P30-P37, P40-P47, E, SC1, SC2
R = 16.5KΩ FOR P30-P37, P40-P47, E, SC1, SC2

Figure 10. Test Loads for Port 1 Darlington Load (P10-P17)



C = 40 R_L, R = 12K
ADJUST R_L SO THAT I_1 = 3.2mA
WITH V_1 = 0.4V and V_{CC} = 5.25V

Figure 11. Typical Data Bus Output Delay versus Capacitive Loading

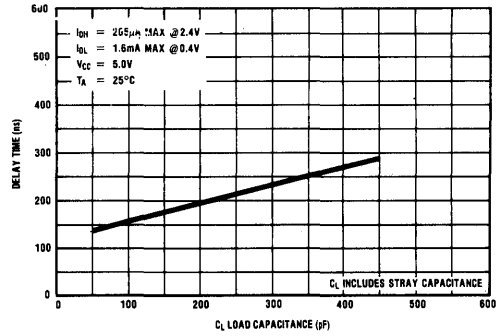
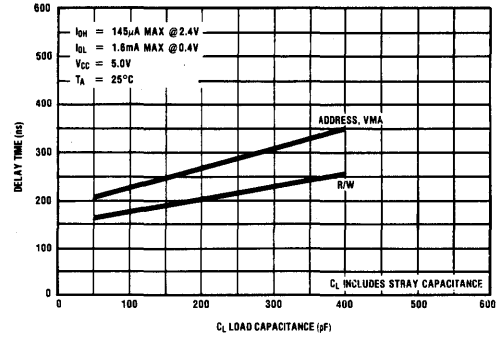


Figure 11. Typical Data Bus Output Delay versus Capacitive Loading



Signal Descriptions

V_{CC} and V_{SS}

These two pins are used to supply power and ground to the chip. The voltage supplied will be +5 volts ±5%.

XTAL1 and EXTAL2

These connections are for a parallel resonant fundamental crystal, AT cut. Divide by 4 circuitry is included with the internal clock, so a 4MHz crystal may be used to run the system at 1MHz. The divide by 4 circuitry allows for use of the inexpensive 3.56MHz Color TV

S6800 FAMILY

crystal for non-time critical applications. Two 27pF capacitors are needed from the two crystal pins to ground to insure reliable operation. EXTAL2 may be driven by an external clock source at a 4MHz rate to run at 1MHz with a 40/60% duty cycle. It is not restricted to 4MHz. XTAL1 must be grounded if an external clock is used. The following are the recommended crystal parameters:

AT = Cut Parallel Resonance Crystal
C_o = 7pF Max
FREQ = 4.0MHz @ C_L = 24pF
R_S = 50 ohms Max
Frequency Tolerance = ±5% to ±0.02%
The best E output "Worst Case Design" tolerance is ±0.05% (500ppM) using a ±0.02% crystal.

V_{CC} Standby

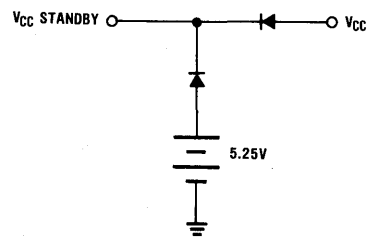
This pin will supply +5 volts ±5% to the standby RAM on the chip. The first 64 bytes of RAM will be maintained in the power down mode with 8mA current max in the ROM version. The circuit of Figure 15 can be utilized to assure that V_{CC} Standby does not go below V_{SBB} during power down.

To retain information in the RAM during power down the following procedure is necessary:

1) Write "0" into the RAM enable bit, RAM E. RAM E is bit 6 of the RAM Control Register at location $0014. This disables the standby RAM, thereby protecting it at power down.

2) Keep V_{CC} Standby greater than V_{SBB}.

Figure 13. Battery Backup for V_{CC} Standby



Reset

This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial startup of the processor. On power up, the reset must be held low for at least 20ms. During operation, $\overline{\text{Reset}}$, when brought low, must be held low at 3 clock cycles.

When a high level is detected, the MPU does the following:

a) All the higher order address lines will be forced high.

b) I/O Port 2 bits, 2, 1, and 0 are latched into programmed control bits PC2, PC1 and PC0.

c) The last two (FFFE, FFFF) locations in memory will be used to load the program addressed by the program counter.

d) The interrupt mask bit is set, must be cleared before the MPU can recognize maskable interrupts.

Enable (E)

This suplies the external clock for the rest of the system when the internal oscillator is used. It is a single phase, TTL compatible clock, and will be the divide by 4 result of the crystal frequency. It will drive one TTL load and 90pF.

Non-Maskable Interrupt ($\overline{\text{NMI}}$)

A low-going edge on this input requests that a non-maskable interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

In response to an $\overline{\text{NMI}}$ interrupt, the Index Register, Program Counter, Accumulators, and Condition Code Register are stored on the stack. At the end of the sequence, a 16-bit address will be loaded that points to a vectoring address located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt service routine in memory.

A 3.3KΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are sampled during E and will start the interrupt routine on the clock bar following the completion of an instruction.

Interrupt Request ($\overline{\text{IRQ}}$)

This level sensitive input requests that an interrupt sequence be generated within the machine. The pro-

cessor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further maskable interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The IRQ requires a 3.3KΩ external resistor to V_{CC} which should be used for wire-OR and optimum control of interrupts. Internal Interrupts will use an internal interrupt line (IRQ2). This Interrupt will operate the same as IRQ except that it will use the vector address of FFF0 and FFF7. IRQ1 will have priority over IRQ2 if both occur at the same time. The Interrupt Mask Bit in the condition mode register masks both interrupts. (See Figure 23.)

The following pins are available in the Single Chip Mode, and are associated with Port 3 only.

Input Strobe ($\overline{IS3}$) (SC1)

This sets an interrupt for the processor when the IS3 Enable bit is set. As shown in Figure 6 Input Strobe Timing, IS3 will fall T_{IS} minimum after data is valid on Port 3. If IS3 Enable is set in the I/O Port Control/Status Register, an interrupt will occur. If the latch enable bit in the I/O Control Status Register is set, this strobe will latch the input data from another device when that device has indicated that it has valid data.

Output Strobe ($\overline{OS3}$) (SC2)

This signal is used by the processor to strobe an external device, indicating valid data is on the I/O pins. The timing for the Output Strobe is shown in Figure 5. I/O Port Control/Status Register is discussed in the following section.

The following pins are available in the Expanded Modes.

Read Write (R/W) (SC2)

This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or a Write (low) state. The normal standby state of this signal is Read (high). This output is capable of driving one TTL load and 90pF.

I/O Strobe ($\overline{IOS}$) (SC1)

In the expanded non-multiplexed mode of operation, $\overline{IOS}$ internally decodes A_9 through A_{15} as zero's and A_8 as a one. This allows external access of the 256 locations from $0100 to $01FF. The timing diagrams are shown as Figures 1 and 2.

Address Strobe (AS) (SC1)

In the expanded multiplexed mode of operation address strobe is output on this pin. This signal is used to latch the 8 LSBs of address which are multiplexed with data on Port 3. An 8-bit latch is utilized in conjunction with Address Strobe, as shown in Figure 19. Address strobe signals the latch when it is time to latch the address lines so the lines can become data bus lines during the E pulse. The timing for this signal is shown in the MC6801 Bus Timing, Figure 7.This signal is also used to disable the address from the multiplexed bus allowing a deselect time, T_{ASD} before the data is enabled to the bus.

S6801 Ports

There are four I/O ports on the S6801 MCU; three 8-bit ports and one 5-bit port. There are two control lines associated with one of the 8-bit ports. Each port has an associated write only Data Direction Register which allows each I/O line to be programmed to act as an input or an output. *A "1" in the corresponding Data Direction Register bit will cause that I/O line to be an output. A "0" in the corresponding Data Direction Register bit will cause the I/O line to be an input. There are four ports: Port 1, Port 2, Port 3, and Port 4. Their addresses and the addresses of their Data Direction registers are given in Table 2.

* The only exception is bit 1 of Port 2, which can either be data input or Timer output.

Table 2. Port and Data Direction Register Addresses

Ports	Port Address	Data Direction Register Address
I/O Port 1	$0002	$0000
I/O Port 2	$0003	$0001
I/O Port 3	$0006	$0004
I/O Port 4	$0007	$0005

I/O Port 1

This is an 8-bit port whose individual bits may be defined as inputs or outputs by the corresponding bit in its data direction register. The 8 output buffers have three-state capability, allowing them to enter a high impedance

state when the peripheral data lines are used as inputs. In order to be read properly, the voltage on the input lines must be greater than 2.0 volts for a logic "1" and less than 0.6 volt for a logic "0". As outputs, these lines are TTL compatible and may also be used as a source of up to 1mA at 1.5 volts to directly drive a Darlington base. After Reset, the I/O lines are configured as inputs. In all three modes, Port 1 is always parallel I/O.

I/O Port 2

This port has five lines that may be defined as inputs or outputs by its data direction register. The 5 output buffers have three-state capability, allowing them to enter a high impedance state when used as an input. In order to be read properly, the voltage on the input lines must be greater than 2.0 volts for a logic "1" and less than 0.8 volt for a logic "0". As outputs, this port has no internal pullup resistors but will drive TTL inputs directly. For driving CMOS inputs, external pullup resistors are required. After Reset, the I/O lines are configured as inputs. Three pins on Port 2 (pins 10, 9 and 8 of the chip) are used to program the mode of operation during reset. The values of these pins at reset are latched into the three MSBs (bits 7, 6, and 5) of Port 2 which are read only. This is explained in the Mode Selection Section.

In all three modes, Port 2 can be configured as I/O and provides access to the Serial Communications Interface and the Timer. Bit 1 is the only pin restricted to data input or Timer output.

I/O Port 3

This is an 8-bit port that can be configured as I/O, as data bus, or an address bus multiplexed with the data bus — depending on the mode of operation hardware programmed by the user at reset. As a data bus, Port 3 is bidirectional. As an input for peripherals, it must be supplied regular TTL levels, that is, greater than 2.0 volts for a logic "1" and less than 0.5 volt for a logic "0".

Its TTL compatible three-state output buffers are capable of driving one TTL load and 90pF. In the Expanded Modes, after reset, the data direction register is inhibited and data flow depends on the state of the R/W line. The input strobe (IS3) and the output strobe (OS3) used for handshaking are explained later.

In the three modes Port 3 assumes the following characteristics:

Single Chip Mode: Parallel Inputs/Outputs as programmed by its associated Data Direction Register. There are two control lines associated with this port in this mode, an input strobe and an output strobe, that can be used for handshaking. They are controlled by the I/O Port Control/Status Register explained at the end of this section.

Expanded Non-Multiplexed Mode: In this mode Port 3 become the data bus (D_7-D_0).

Expanded Multiplexed Mode: In this mode Port 3 becomes both the data bus (D_7-D_0) and lower bits of the address bus (A_7-A_0). An address strobe output is true when the address is on the port.

I/O Port 3 Control/Status Register

	7	6	5	4	3	2	1	0
$0000F	IS3 FLAG	IS3 ENABLE	X	OSS	LATCH ENABLE	X	X	X

Bit 0 Not used.
Bit 1 Not used.
Bit 2 Not used.
Bit 3 Latch Enable. This controls the input latch for I/O Port 3. If this bit is set high the input data will be latched with the falling edge of the Input Strobe, IS3. This bit is cleared by reset, or CPU Read Port 3.
Bit 4 (OSS) Output Strobe Select. This bit will select if the Output Strobe should be generated by a write to I/O Port 3 or a read of I/O Port 3. When this bit is cleared the strobe is generated by a read Port 3. When this bit is set the strobe is generated by a write Port 3.
Bit 5 Not used.
Bit 6 IS3 ENABLE. This bit will be the interrupt caused by IS3. When set to a low level the IS3 FLAG will be set by input strobe but the interrupt will not be generated. This bit is cleared by reset.
Bit 7 IS3 FLAG. This is a read only status bit that is set by the failing edge of the input strobe, IS3. It is cleared by a read of the Control/Status Register followed by a read or write of I/O Port 3. Reset will clear this bit.

I/O Port 4

This is an 8-bit port that can be configured as I/O or as address lines depending on the mode of operation. In order to be read properly, the voltage on the input lines must be greater than 2.0 volts for a logic "1" and less than 0.8 volt for a logic "0". As outputs, each line is TTL compatible and can drive 1 TTL load and 90pF. After reset, the lines are configured as inputs. To use the pins as addresses, therefore, they should be pro-

grammed as outputs in the three modes. Port 4 assumes the following characteristics.

Single Chip Mode: Parallel Inputs/Outputs as programmed by its associated Data Direction Register.

Expanded Non-Multiplexed Mode: In this mode Port 4 is configured as the lower order address lines (A_7-A_0) by writing one's to the data direction register. When all eight address lines are not needed, the remaining line starting with the most significant bit, may be used as I/O (inputs only).

Expanded Multiplexed Mode: In this mode Port 4 is configured as the high order address lines (A_{15}-A_8) by writing one's to the data direction register. When all eight address lines are not needed, the remaining line, starting with the most significant bit, may be used as I/O (inputs only).

Mode Selection

The mode of operation that 6801 will operate in after Reset is determined by hardware that the user must wire on pins 10, 9, and 8 of the chip. These pins are the three LSBs (I/O2, I/O1, and I/O0 respectively) of Port 2. They are latched into programmed control bits PC2, PC1, and PC0 when reset goes high. I/O Port 2 Register is shown below.

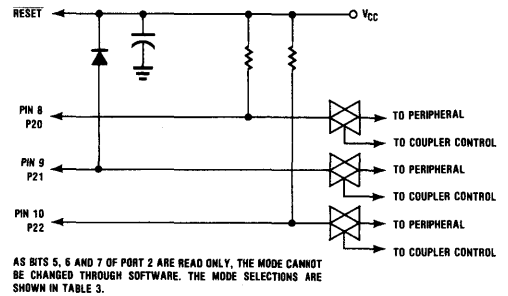
	7	6	5	4	3	2	1	0
$0003	PC2	PC1	PC0	I/O4	I/O3	I/O2	I/O1	I/O0

An example of external hardware that could be used in the Expanded Non-Multiplexed Mode is given in Figure 14. In the Expanded Non-Multiplexed Mode, pins 10, 9 and 8 are programmed Hi, Lo, Hi respectively as shown.

Couplers between the pins on Port 2 and the peripherals attached may be required. If the lines go to devices which require signals at power up differing from the signals needed to program the 6801's mode, couplers are necessary.

The 14066B can be used to provide this isolation between the peripheral device and the MCU during reset. Figure 15 shows the logic diagram and xxxxx? for the MC14066B. It is bidirectional and requires no external logic to determine the direction of the information flow. The logic shown insures that the data on the peripheral will not change before it is latched into the MCU and the MCU has started the reset sequence.

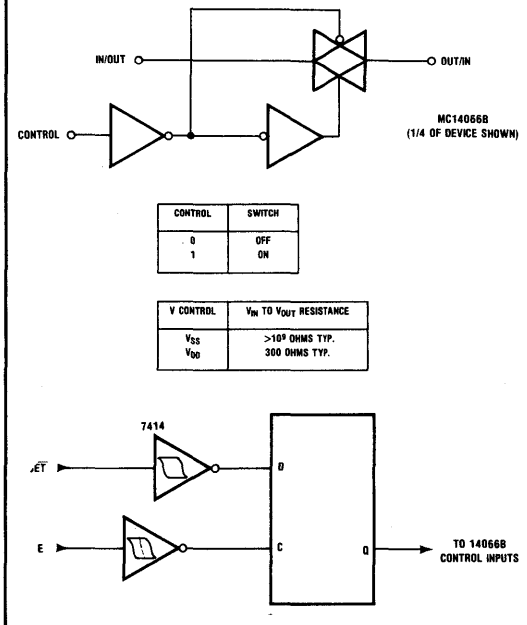
Figure 14. Diode Configuration for the Expanded Non-Multiplexed Mode



AS BITS 5, 6 AND 7 OF PORT 2 ARE READ ONLY, THE MODE CANNOT BE CHANGED THROUGH SOFTWARE. THE MODE SELECTIONS ARE SHOWN IN TABLE 3.

P20 REFERS TO PORT 2, BIT 0.

Figure 15. Quad Analog, Switch/Multiplexer in a Typical S6801 Circuit



CONTROL	SWITCH
0	OFF
1	ON

V CONTROL	V_{IN} TO V_{OUT} RESISTANCE
V_{SS}	$>10^9$ OHMS TYP.
V_{DD}	300 OHMS TYP.

S6600 FAMILY

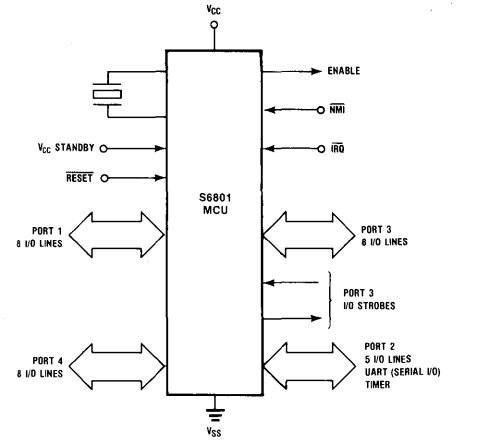
S6801 Basic Modes

The S6801 is capable of operating in three basic modes, (1) Single Chip Mode, (2) Expanded Multiplexed Mode (compatible with S6800 peripheral family), (3) Expanded Non-Multiplexed Mode.

Single Chip Mode

In the Single Chip Mode the ports are configured for I/O. In this mode, Port 3 has two associated control lines, an input strobe and an output strobe for handshaking data.

Figure 16. S6801 MCU Single Chip Mode



Expanded Non-Multiplexed Mode

In this mode the S6801 will directly address S6800 peripherals with no external logic. In this mode Port 3 becomes the data bus. Port 4 becomes the A_7-A_0 address bus or partial address and I/O (inputs only). Port 2 can be parallel I/O, serial only. In this mode the S6801 is expandable to 256 locations. The eight address lines associated with Port 4 may be substituted for I/O (inputs only) if a fewer number of address lines will satisfy the application.

The Internal Clock requires only the addition of a crystal for operation. This input will also accept an external TTL or CMOS input, but in either case, the clock frequency will be divided by four for this mask option. (Figure 17)

Expanded Multiplexed Mode

In this mode Port 4 becomes higher order address lines with an alternative of substituting some of the address lines for I/O (inputs only). Port 3 is the data bus multiplexed with the lower order address lines differentiated by an output called Address Strobe. Port 2 is 5 lines of Parallel I/O, SC1, Timer, or any combination thereof. Port 1 is 8 Parallel I/O lines. In this mode it is expandable to 65K words. (Figure 18)

Internal Clock/Divide-by-Four — This mask option is shown in Figure 18. Only an external crystal is required for operation.

Figure 17. S6801 MCU Expanded Non-Multiplexed Mode

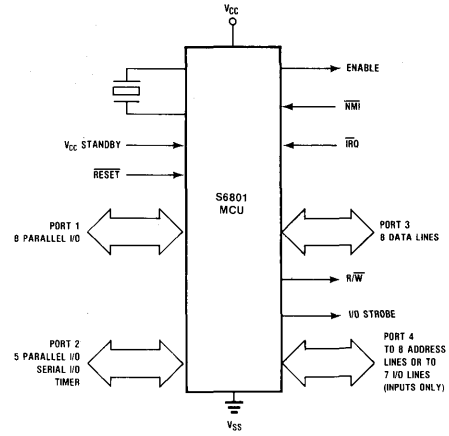


Figure 18. S6801 MCU Expanded Multiplexed Mode

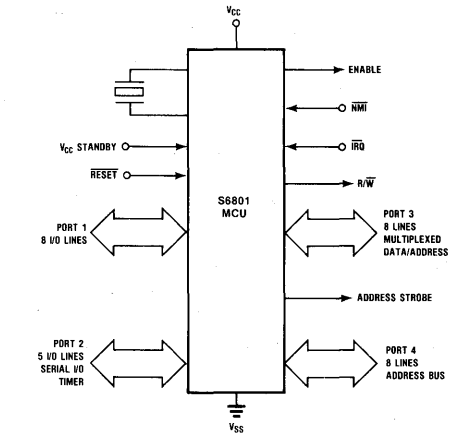


Table 3. Mode Selects

MODE		PROGRAM CONTROL			ROM	RAM	INTERRUPT VECTORS	BUS
7	Single Chip	Hi	Hi	Hi	I	I	I	I
6	Expanded Multiplexed	Hi	Hi	Lo	I	I	I	Ep/M
5	Expanded Non-Multiplexed	Hi	Lo	Hi	I	I	I	Ep
4	Single Chip Test	Hi	Lo	Lo	I(2)	I(1)	I	I
3	64K Address I/O	Lo	Hi	Hi	E	E	E	Ep/M
2	Ports 3 & 4 External	Lo	Hi	Lo	E	I	E	Ep/M
1		Lo	Lo	Hi	I	I	E	Ep/M
0	Test Data Outputted from ROM & ROM to I/O Port 3	Lo	Lo	Lo	I	I	I*	Ep/m

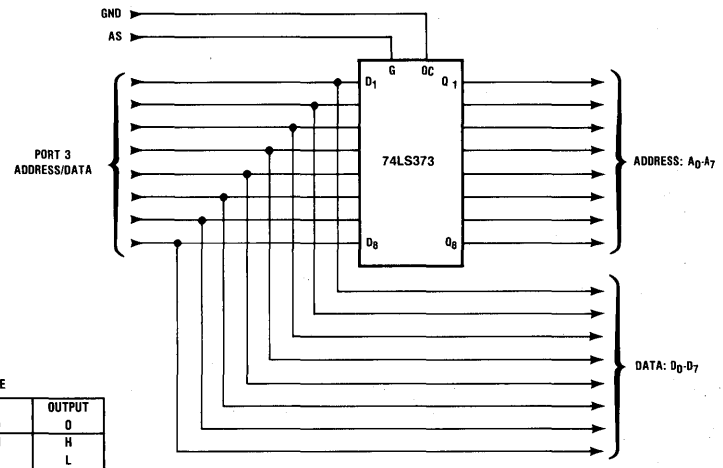
E — EXTERNAL all vectors are external
I — INTERNAL
Ep — EXPANDED MULTIPLEXED

*First two addresses read from external after reset
(1) Address for RAM XX80-XXFF
(2) ROM disabled

Lower Order Address Bus Latches

Since the data is multiplexed with the lower order address bus in Port 3, latches are required to latch those address bits. The SN74LS373 Transparent octal D-type latch can be used with the S6801 to latch the least significant address byte. Figure 19 shows how to connect the latch to the S6801. The output control to the LS373 may be connected to ground.

Figure 19. Latch Connection



FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	ENABLE D	OUTPUT Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

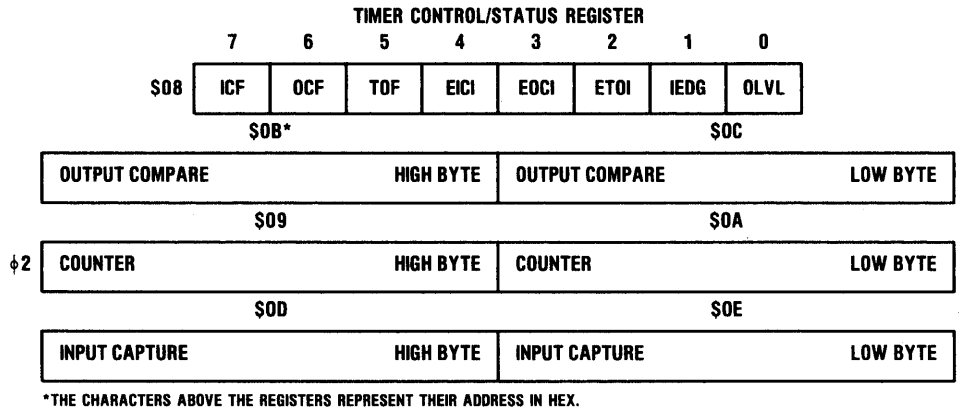
Programmable Timer

The S6801 contains an on-chip 16 bit programmable timer which may be used to perform measurements on an input waveform while independently generating an output waveform. Pulse widths for both input and output signals may vary from a few microseconds to many seconds. The timer hardware consists of:

- an 8-bit control and status register
- a 16-bit free running counter
- a 16-bit output compare register, and
- a 16-bit input capture register

A block diagram of the timer registers is shown in Figure 20.

Figure 20. Block Diagram of Timer Registers



*THE CHARACTERS ABOVE THE REGISTERS REPRESENT THEIR ADDRESS IN HEX.

Free Running Counter ($0009:000A)

The key element in the programmable timer is a 16-bit free running counter which is driven to increasing values by the MPUϕ. The counter value may be read by the MPU software at any time. The counter is cleared to zero on RESET and may be considered a read-only register with one exception. Any MPU write to the counter's address ($09) will always result in a preset value of $FFF8 being loaded into the counter regardless of the value involved in the write. The preset feature is intended for testing operation of the part, but may be of value in some applications.

Output Compare Register ($000B:000C)

The Output Compare Register is a 16-bit read/write register which is used to control an output waveform. The contents of this register are constantly compared with the current value of the free running counter. When a match is found a flag is set (OCF) in the Timer Control and Status Register (TCSR) and the current value of the Output Level bit (OLVL) in the TCSR is clocked to the output level register. Providing the Data Direction Register for Port 2, Bit 1 contains a "1" (output), the output level register value will appear on the pin for Port 2 Bit 1. The values in the Output Compare Register and Output level bit may then be changed to control the output level on the next compare value. The Output Compare Register is set to $FFFF during RESET. The Compare function is inhibited for one cycle following a write to the high byte of the Output Compare Register to insure a valid 16-bit value is in the register before a compare is made.

Input Capture Register ($000D:000E)

The Input Capture Register is a 16-bit read-only register used to store the current value of the free running counter when the proper transition of an external input signal occurs. This input transition change required to trigger the counter transfer is controlled by the input Edge bit (EDG) in the TOSR. The Data Direction Register bit for Port 1 Bit 0 should *be clear (zero) in order to gate in the external input signal to the edge defect unit in the timer.

*With Port 2 Bit 0 configured as an output and set to "1", the external input will still be seen by the edge detect unit.

Timer Control and Status Register (TCSR) ($0008)

The Timer Control and Status Register consists of an 8-bit register of which all 8 bits are readable but only the low order 5 bits may be written. The upper three bits contain read-only timer status information and indicate that:

- a proper transition has taken place on the input pin with a subsequent transfer of the current counter value to the input capture register.
- a match has been found between the value in the free running counter and the output compare register, and
- when $0000 is in the free running counter.

Each of the flags may be enabled onto the S6801 internal bus (RO2) with an individual Enable bit in the TCSR. If the 1-bit in the S6801 Condition Code Register has been cleared, a priority vectored interrupt will occur corresponding to the flag bit(s) set. A description for each bit follows:

TIMER CONTROL AND STATUS REGISTER

7	6	5	4	3	2	1	0	
ICF	OCF	TOF	EICI	EOCI	ETOI	IEDG	OLVL	$0008

Bit 0 OLVL — **Output Level** — This value is clocked to the output level register on an output compare. If the DDR for Port 2 Bit 1 is set, the value will appear on the output pin.

Bit 1 IEDG — **Input Edge** — This bit controls which transition of an input will trigger a transfer of the counter to the input capture register. The DDR for Port 2 Bit 0 must clear for this function to operate.

IEDG = 0 Tranfer takes place on a negative (high-to-low transition).

IEDG = 1 Transfer takes place on a positive edge (low-to-high transition).

Bit 2 ETOI — **Enable Timer Overflow Interrupt** — When set, this bit enables IRQ2 to occur on the internal bus for a TOF Interrupt; when clear the interrupt is inhibited.

Bit EOCI — **Enable Output Compare Interrupt** — When set, this bit enables IRQ2 to appear on the internal bus for an input capture interrupt; when clear the interrupt is inhibited.

Bit 4 EICI — **Enable Input Capture Interrupt** — When set, this bit enables IRQ2 to occur on the internal bus for an input capture interrupt; when clear the interrupt is inhibited.

Bit 5 TOF — **Timer Overflow Flag** — This read-only bit is set when the counter contains $0000. It is cleared by a read of the TCSR (with TOF set) followed by an MPU read of the Counter ($09).

Bit 6 OCF — **Output Compare Flag** — This read-only bit is set when a match is found between the output compare register and the free running counter. It is cleared by a read of the TCSR (with ODF set) followed by an MPU write to the output compare register ($0B or $0C).

Bit 7 CF — **Input Capture Flag** — This read-only status bit is set by a proper transition on the input to the edge detect unit; it is cleared by a read of the TCSR (with ICF set) followed by an MPU read of the input Capture Register ($0D).

Serial Communications Interface

The S6801 contains a full-duplex asynchronous serial communications interface (SCI) on board. Two serial data formats (standard mark/space [NRZ] or Bi-phase) are provided at several different data rates. The controller comprises a transmitter and a receiver which operate independently of each other but in the same data format and at the same data rate. Both transmitter and receiver communicate with the MPU via the data bus and with the outside world via pins 2, 3, and 4 of Port 2. The hardware, software, and registers are explained in the following paragraphs.

Wake-up Feature

In a typical multi-procesor application, the software protocol will usually contain a destination address in the initial byte(s) of the message. In order to permit non-

selected MPU's to ignore the remainder of the message, a wake-up feature is included whereby all further interrupt processing may be optionally inhibited until the beginning of the next message. When the next message appears, the hardware re-enables (or "wakes-up") for the next message. The "wake-up" is automatically triggered by a string of ten consecutive 1's which indicates an idle transmit line. The software protocol must provide for the short idle period between any two consecutive messages.

Programmable Options

The following features of the S6801 serial I/O section have programmable:

- format — standard mark/space (NRZ) or Bi-phase
- clock — external or internal
- Baud rate — one of 14 per given MPUϕ2 clock frequency or external clock X8 input
- wake-up feature — enabled or disabled
- interrupt requests — enabled or masked individually for transmitter and receiver data registers
- clock output — internal clock enabled or disabled to Port 2 (Bit 2)
- Port 2 (Bits 3 and 4) — dedicated or not dedicated to serial I/O individually for transmitter and receiver

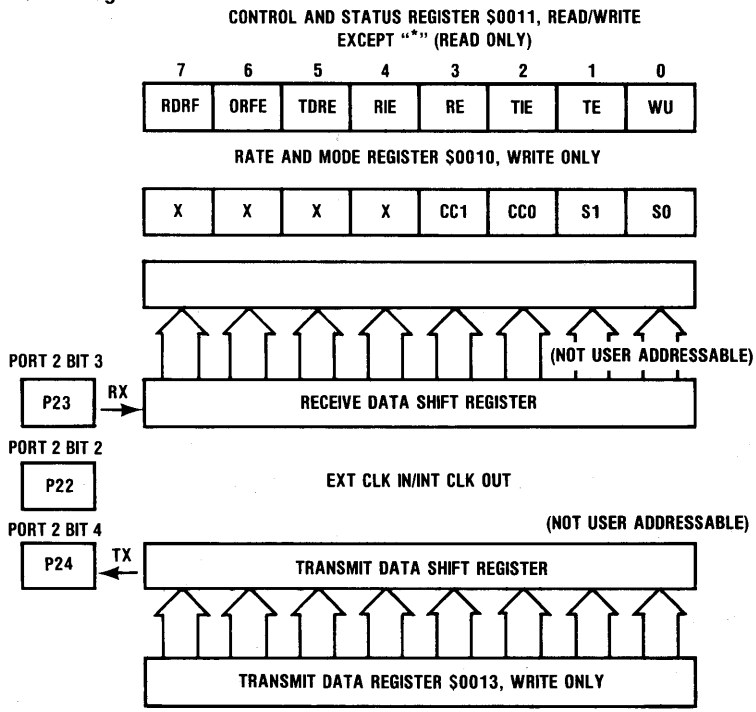
Serial Communications Hardware

The serial communications hardware is controlled by 4 registers as shown in Figure 21. The registers include:

- an 8-bit control and status register
- a 4-bit rate and mode control register (write only)
- an 8-bit read-only receive data register and
- an 8-bit write-only transmit data register

In addition to the four registers, the serial I/O section utilizes Bit 3 (serial input) and Bit 4 (serial output) or Port 2. Bit 2 of Port 2 is utilized if the internal-clock-out or external-clock-in options are selected.

Figure 21. Serial I/O Registers



Transmit/Receive Control and Status (TRCS) Register

The TRCS register consists of an 8-bit register of which all 8 bits may be read while only bits 0-4 may be written. The register is initialized to $20 on $\overline{\text{RESET}}$. The bits in the TRCS register are defined as follows:

7	6	5	4	3	2	1	0	
RDRE	ORFE	TDRE	RIE	RE	TIE	TE	WU	ADDR. $0011

Bit 0 WU **"Wake-up on Next Message** — set by S6801 software cleared by hardware on receipt of ten consecutive 1's.

Bit 1 TE **Transmit Enable** — set by S6801 to produce preamble of nine consecutive 1's and to enable gating of transmitter output to Port 2, Bit 4 regardless of DDR value corresponding to this bit; when clear, serial I/O has no effect on Port 2 Bit 4.

Bit 2 TIE **Transmit Interrupt Enable** — when set, will permit an $\overline{\text{IRQ2}}$ interrupt to occur when Bit 5 (TDRE) is set; when clear, the TDRE value is masked from the bus.

Bit 3 RE **Receiver Enable** — when set, gates Port 2 Bit 3 to input of receiver regardless of DDR value for this bit; when clear, serial I/O has no effect on Port 2 Bit 3.

Bit 4 RIE **Receiver Interrupt Enable** — when set, will permit an $\overline{\text{IRQ2}}$ interrupt to occur when Bit 7 (RDRF) or Bit 6 (OR) is set; when clear, the interrupt is masked.

Bit 5 TDRE **Transmit Data Register Empty** — set by hardware when a transfer is made from the transmit data register to the output shift register. The TDRE bit is cleared by reading the status register, then writing a new byte into the transmit data register, TDRE is initialized to 1 by $\overline{\text{RESET}}$.

Bit 6 ORFE **Over-Run-Framing Error** — set by hardware when an overrun or framing error occurs (receive only). An overrun is defined as a new byte received with last byte still in Data Register/Buffer. A framing error has occurred when the byte boundaries in bit stream are not synchronized to bit counter. The ORFE bit is cleared by reading the status register, then reading the Receive Data Register, or by $\overline{\text{RESET}}$.

Bit 7 RDRF **Receiver Data Register Full** — set by hardware when a transfer from the input shift register to the receiver data register is made. The RDRF bit is cleared by reading the status register, then reading the Receive Data Register, or by $\overline{\text{RESET}}$.

Rate and Mode Control Register

The Rate and Mode Control register controls the following serial I/O variables:

- Baud rate
- format
- Clock source, and
- Port 2 Bit 2 configuration

The register consists of 4 bits all of which are write-only and cleared on $\overline{\text{RESET}}$. The 4 bits in the register may be considered as a pair of 2-bit fields. The two low order bits control the bit rate for internal clocking and the remaining two bits control the format and clock select logic. The register definition is as follows:

7	6	5	4	3	2	1	0	
X	X	X	X	CC1	CC0	S1	S0	ADDR. $0010

Bit 0 S0
Bit 1 S1 — **Speed Select** — These bits select the Baud rate for the internal clock. The four rates which may be selected are a function of the MPU $\phi 2$ clock frequency. Table 4 lists the available Baud rate.

Bit 2 CC0
Bit 3 CC1 — **Clock Control and Format Select** — This 2-bit field controls the format and clock select logic. Table 5 defines the bit field.

Table 4. SCI Internal Baud Rates

S1, S0	XTAL	4.0MHz	4.9152MHz	2.5476MHz
	$\phi 2$	1.0MHz	1.2288MHz	0.6144MHz
00	$\phi 2 \div 16$	62.5K BITS/S	76.8K BITS/S	38.4K BITS/S
01	$\phi 2 \div 128$	7,812.5 BITS/S	9,600 BITS/S	4,800 BITS/S
10	$\phi 2 \div 1024$	976.6 BITS/S	1,200 BITS/S	600 BITS/S
11	$\phi 2 \div 4096$	244.1 BITS/S	300 BITS/S	150 BITS/S

Table 5. Bit Field

CC1, CC0	FORMAT	CLOCK SOURCE	PORT 2 BIT 2	PORT 2 BIT 3	PORT 2 BIT 4
00	BI-PHASE	INTERNAL	NOT USED	**	**
01	NRZ	INTERNAL	NOT USED	**	**
10	NRZ	INTERNAL	OUTPUT*	SERIAL INPUT	SERIAL OUTPUT
11	NRZ	EXTERNAL	INPUT	SERIAL INPUT	SERIAL OUTPUT

*CLOCK OUTPUT IS AVAILABLE REGARDLESS OF VALUES FOR BITS RE AND TE.
**BIT 3 IS USED FOR SERIAL INPUT IF RE = "1" IN TRCS; BIT 4 IS USED FOR SERIAL OUTPUT IF TE = "1" IN TRCS.

Internally Generated Clock

If the user wishes for the serial I/O to furnish a clock, the following requirements are applicable:

- the values of RE and TE are immaterial
- CC1, CC0 must be set to 10
- the maximum clock rate will be ϕ # 16
- the clock will be at 1 × the bit rate and will have a rising edge at mid-bit

Externally Generated Clock

If the user wishes to provide an external clock for the serial I/O, the following requirements are applicable:

- the CC1, CC0, field in the Rate and Mode Control Register must be set to 11
- the external clock must be set to 8 times (× 8) the desired baud rate and
- the maximum external clock frequency is 1.2MHz.

Serial Operations

The Serial I/O hardware should be initialized by the S6801 software prior to operation. This sequence will normally consists of:

- writing the desired operation control bits to the Rate and Mode Control Register and
- writing the desired operational control bits in the Transmit/Receive Control and Status Register.

The Transmitter Enable (TE) and Receiver Enable (RE) bits may be left set for dedicated operations.

Transmit Operations

The transmit operation is enabled by the TE bit in the Transmit/Receive Control and Status Register. This bit

when set, gates the output of the serial transmit shift register to Port 2 Bit 4 and takes unconditional control over the Data Direction Register value for Port 2, Bit 4.

Following a $\overline{\text{RESET}}$, the user should configure both the Rate and Mode Control Register and the Transmit/Receiver Control and Status Register for desired operation. Setting the TE bit during this procedure initiates the serial output by first transmitting a ten-bit preamble of 1s. Following the preamble, internal synchronization is established and the transmitter section is ready for operation.

At this point one of two situations exist:

a) if the Transmit Data Register is empty (TDRE = 1), a continuous string of ones will be sent indicating an idle line, or

b) if data has been loaded into the Transmit Data Register (TDRE = 0), the word is transferred to the output shift register and transmission of the data word will begin.

During the transfer itself, the 0 start bit is first transmitted. Then the 8 data bits (beginning with bit 0) followed by the stop bit, are transmitted. When the Transmitter Data Register has been emptied, the hardware sets the TDRE flag bit.

If the S6801 fails to respond to the flag within the proper time, (TDRE is still set when the next normal transfer from the parallel data register to the serial output register should occur) then a 1 will be sent (instead of a 0) at "Start" bit time, followed by more 1s until more data is supplied to the data register. No 0s will be sent while TDRE remains a 1.

The Bi-phase mode operates as described above except that the serial output toggles each bit time, and on 1/2 bit times when a 1 is sent.

Receiver Operation

The receive operation is enabled by the RE bit which gates in the serial input through Port 2 Bit 3. The receiver section operation is conditioned by the contents of the Transmit/Receive Control and Status Register and the Rate and Mode Control Register.

The receiver bit interval is divided into 8 sub-intervals for internal synchronization. In the standard, non-Bi-phase mode, the received bit stream is synchronized by the first 0 (space) encountered.

The approximate center of each bit time is strobed during the next 10 bits. If the tenth bit is not a 1 (stop bit) a framing error is assumed, and bit ORFE is set. If the tenth bit is 1, the data is transferred to the Receiver Data Register, and interrupt flag RDRF is set. If RDRF is still set at the next tenth bit time, ORFE will be set, indicating an over-run has occurred. When the S6801 responds to either flag (RDRF or ORFE) by reading the status register followed by reading the Data Register RDRF (or ORFE) will be cleared.

Ram Control Register

This register, which is addressed at $0014, gives status information about the standby RAM. An 0 in the RAM enable bit (RAM E) will disable the standby RAM, thereby protecting it at power down if V_{CC} is held greater than V_{SBB} volts, as explained previously in the signal description for V_{CC} Standby.

$0014	STAND-BY BIT	RAM E	X	X	X	X	X	X

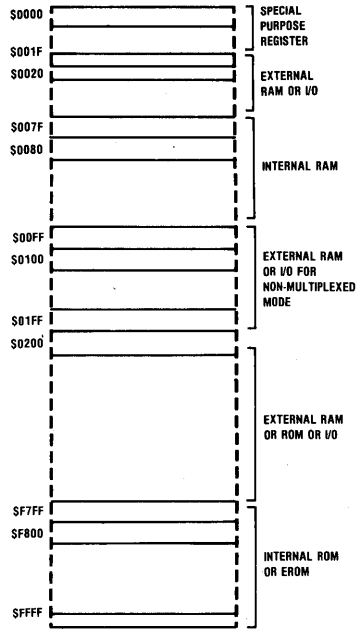
Bit 1 Not used.
Bit 2 Not used.
Bit 3 Not used.
Bit 4 Not used.
Bit 5 Not used.
Bit 6 The RAM ENABLE control bit allows the user the ability to disable the standby RAM. This bit is set to a logic "one" by reset which enables the standby RAM and can be written to or zero under program control. When the RAM is disabled, logic "zero", data is read from external memory.
Bit 7 The STANDBY BIT of the control register, $0014, is cleared when the standby voltage is removed. This bit is a read/write status flag that the user can read which indicates that the standby RAM voltage has been applied, and the data in the standby RAM is valid.

The S6801 provides up to 65K bytes of memory for program and/or data storage. The memory map is shown in Figure 22.

Locations $0020 through $007F access external RAM or I/O Internal RAM is accessed at $0080 through $00FF. The RAM may be alternately selected by mask programming at location $A000. However, if the user desires to access external RAM at those locations he may do so by clearing the RAM ENABLE control bit of the RAM Control Register. In this way an extra 126

bytes of external RAM are available. The first 64 bytes of the 128 bytes of on-chip RAM are provided with a separate power supply. This will maintain the 64 bytes of RAM in the power down mode as explained in the pin description for V_{CC} Standby.

Figure 22. Memory Map



Locations $0100 through $01FF are available in the Expanded Non-Multiplexed Mode. The eight address lines of Port 4 make this 256 word expandability possible. Those not needed for address lines can be used as input lines instead.

The full range of addresses available to the user is in the Expanded Multiplexed Mode. Locations $0200 through $F7FF can be used as external RAM, external ROM, or I/O. Any higher order bit not required for addressing can be used as I/O as in the Expanded Non-Multiplexed Mode.

The internal ROM is located at $F800 through $FFFF. The decoder for the ROM may be mask programmed on A_{12} and A_{13} as zeros or ones to provide for $C800, $D800, $E800 for the ROM address. A_{12} and A_{13} may also be don't care in this decoder. The primary address for the ROM will be $F800.

The first 32 bytes are for the special purpose registers as shown in Table 6.

Table 6. Special Registers

HEX ADDRESS	REGISTER
00	DATA DIRECTION 1
01	DATA DIRECTION 2
02	I/O PORT 1
03	I/O PORT 2
04	DATA DIRECTION 3
05	DATA DIRECTION 4
06	I/O PORT 3
07	I/O PORT 4
08	TCSR
09	COUNTER HIGH BYTE
0A	COUNTER LOW BYTE
0B	OUTPUT COMPARE HIGH BYTE
0C	OUTPUT COMPARE LOW BYTE
0D	INPUT CAPTURE HIGH BYTE
0E	INPUT CAPTURE LOW BYTE
0F	I/O PORT 3 C/S REGISTER
10	SERIAL RATE AND MODE REGISTER
11	SERIAL CONTROL AND STATUS REGISTER
12	SERIAL RECEIVER DATA REGISTER
13	SERIAL TRANSMIT DATA REGISTER
14	RAM/EROM CONTROL REGISTER
15-1F	RESERVED

Figure 23. Memory Map for Interrupt Vectors

	VECTOR MS	VECTOR LS	DESCRIPTION
Highest Priority	FFFE,	FFFF	Restart
	FFFC,	FFFD	Non-Maskable Interrupt
	FFFA,	FFFB	Software Interrupt
	FFF8,	FFF9	IRQ1/Interrupt Strobe S
	FFF6,	FFF7	IRQ2/Timer Input Capture
	FFF4,	FFF5	IRQ2/Timer Output Compare
	FFF2,	FFF3	IRQ2/Timer Overflow
Lowest Priority	FFF0,	FFF1	IRQ2/Serial I/O Interrupt

General Description of Instruction Set

The S6801 is upward object code compatible with the S6800 as it implements the full S6800 instruction set. The execution times of key instructions have been reduced to increase throughput. In addition, new instructions have been added; these include 16-bit operations and a hardware multiply.

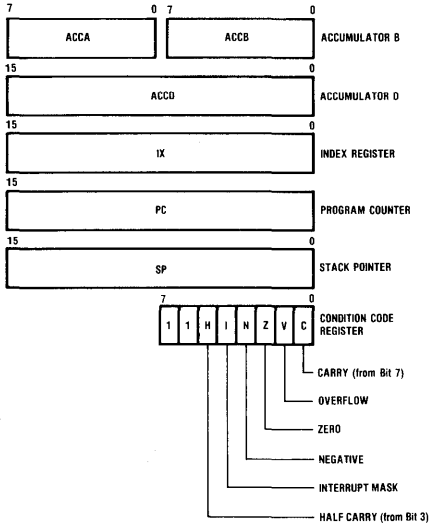
Included in the instruction set section are the following:

- MPU Programming Model (Figure 24)
- Addressing modes
- Accumulator and memory instructions—Table 7
- New instructions
- Index register and stack manipulations—Table 8
- Jump and branch instructions—Table 9
- Special operations—Figure 25
- Condition code register manipulation instructions—Table 10
- Instruction Execution times in machine cycles—Table 11
- Summary of cycle by cycle operation—Table 12

MPU Programming Model

The programming model for the S6801 is shown in Figure 24. The double (D) accumulator is physically the same as the A Accumulator concatenated with the B Accumulator so that any operation using accumulator D will destroy information in A and B.

Figure 24. MCU Programming Model



MPU Addressing Modes

The S6801 eight-bit microcomputer unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Table 11 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 4MHz, these times would be microseconds.

Accumulator (ACCX) Addressing—In accumulator only addressing, either accumulator A or accumulator B is specified. These are one-byte instructions.

Immediate Addressing—In immediate addressing, the operand is contained in the second byte of the instruction except LDS and LDX which have the operand in the second and third bytes of the instruction. The MCU addresses this location when it fetches the immediate instruction for execution. These are two or three-byte instructions.

Direct Addressing—In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in the machine i.e., locations zero through 255. Enhanced execution times are achieved by storing data in these locations. In most configurations, it should be a random access memory. These are two-byte instructions.

Extended Addressing—In extended addressing, the address contained in the second byte of the instruction is used as the higher eight-bits of the address of the operand. The third byte of the instruction is used as the lower eight-bits of the address for the operand. This is an absolute address in memory. These are three-byte instructions.

Indexed Addressing—In indexed addressing, the address contained in the second byte of the instruction is added to the index register's lowest eight bits in the MCU. The carry is then added to the higher order eight bits of the index register. This result is then used to address memory. The modified address is held in a temporary address register so there is no change to the index register. These are two-byte instructions.

Implied Addressing—In the implied addressing mode the instruction gives the address (i.e., stack pointer, index register, etc.). These are one-byte instructions.

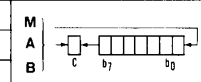
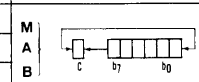
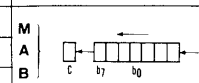
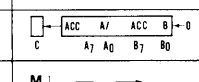
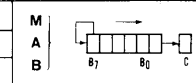
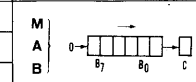
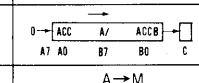
Relative Addressing—In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest eight bits plus two. The carry or borrow is then added to the high eight bits. This allows the user to address data within a range of −125 to +120 bytes of the present instruction. These are two-byte instructions.

Table 7. Accumulator & Memory Instructions

ACCUMULATOR AND MEMORY		ADDRESSING MODES																5	4	3	2	1	0
		IMMED.			DIRECT			INDEX			EXTEND			INHERENT									
Operations	**MNEMONIC**	**OP**	~	#	**OP**	~	#	**OP**	~	#	**OP**	~	#	**OP**	~	#	**Boolean/Arithmetic Operation**	**H**	**I**	**N**	**Z**	**V**	**C**
ADD	ADDA	8B	2	2	9B	3	2	AB	4	2	BB	4	3				A + M→A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	4	2	FB	4	3				B + M→B	↕	•	↕	↕	↕	↕
ADD DOUBLE	ADDD	C3	4	3	D3	5	2	E3	6	2	F3	6	3				A:B + M:M + 1→A:B	•	•	↕	↕	↕	↕
ADD ACCUMULATORS	ABA													1B	2	1	A + B→A	↕	•	↕	↕	↕	↕
ADD WITH CARRY	ADCA	89	2	2	99	3	2	A9	4	2	B9	4	3				A + M + C→A		•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	4	2	F9	4	3				B + M + C→B		•	↕	↕	↕	↕
AND	ANDA	84	2	2	94	3	2	A4	4	2	B4	4	3				A M→A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	4	2	F4	4	3				B M→B	•	•	↕	↕	R	•
BIT TEST	BIT A	85	2	2	95	3	2	A5	4	2	B5	4	3				A M	•	•	↕	↕	R	•
	BIT B	C5	2	2	D5	3	2	E5	4	2	F5	4	3				B M	•	•	↕	↕	R	•
CLEAR	CLR							6F	6	2	7F	6	3				00 →M	•	•	R	S	R	R
	CLRA													4F	2	1	00 →A	•	•	R	S	R	R
	CLRB													5F	2	1	00 →B	•	•	R	S	R	R
COMPARE	CMPA	81	2	2	91	3	2	A1	4	2	B1	4	3				A − M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	4	2	F1	4	3				B − M	•	•	↕	↕	↕	↕
COMPARE ACCUMULATORS	CBA													11	2	1	A − B	•	•	↕	↕	↕	↕
COMPLEMENT, 1'S	COM							63	6	2	73	6	3				M→M	•	•	↕	↕	R	S
	COMA													43	2	1	A→A	•	•	↕	↕	R	S
	COMB													53	2	1	B→B	•	•	↕	↕	R	S
COMPLEMENT, 2'S	NEG							60	6	2	70	6	3				0C − M→M	•	•	↕	↕	①	②
(NEGATE)	NEGA													40	2	1	00 − A→A	•	•	↕	↕	①	②
NEGB														50	2	1	00 − B→B	•	•	↕	↕	①	②
DECIMAL ADJUST, A	DAA													19	2	1	Converts binary add of BCD characters into BCD format	•	•	↕	↕	↕	③
DECREMENT	DEC							6A	6	2	7A	6	3				M − 1→M	•	•	↕	↕	④	•
	DECA													4A	2	1	A − 1→A	•	•	↕	↕	④	•
	DECB													5A	2	1	B − 1→B	•	•	↕	↕	④	•
EXCLUSIVE OR	EORA	88	2	2	98	3	2	A8	4	2	B8	4	3				A⊕M→A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	4	2	F8	4	3				B⊕M→B	•	•	↕	↕	R	•
INCREMENT	INC							9C	6	2	7C	6	3				M + 1→M	•	•	↕	↕	⑤	•
	INCA													4C	2	1	A + 1→A	•	•	↕	↕	⑤	•
	INCB													5C	2	1	B + 1→B	•	•	↕	↕	⑤	•
LOAD ACCUMULATOR	LDAA	86	2	2	96	3	2	A6	4	2	B6	4	3				M→A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	4	2	F6	4	3				M→B	•	•	↕	↕	R	•
LOAD DOUBLE ACCUMULATOR	LDAD	CC	3	3	DC	4	2	EC	5	2	FC	5	3				M + A M + 1→B	•	•	↕	↕	R	•
MULTIPLY UNSIGNED	MUL													3D	10	1	A × B→AB	•	•	•	•	•	⑫
OR, INCLUSIVE	ORAA	8A	2	2	9A	3	2	AA	4	2	BA	4	3				A + M→A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	4	2	FA	4	3				B + M→B	•	•		↕	•	•

The Condition Code Register notes are listed after Table 10.

Table 7. Accumulator & Memory Instructions (Continued)

ACCUMULATOR AND MEMORY		ADDRESSING MODES																					
		IMMED.			DIRECT			INDEX			EXTEND			INHERENT				5	4	3	2	1	0
Operations	**MNEMONIC**	**OP**	~	#	**OP**	~	#	**OP**	~	#	**OP**	~	#	**OP**	~	#	**Boolean/Arithmetic Operation**	**H**	**I**	**N**	**Z**	**V**	**C**
PUSH DATA	PSHA													36	3	1	$A \rightarrow M_{SP}$ $SP-1 \rightarrow SP$	•	•	•	•	•	•
	PSHB													37	3	1	$B \rightarrow M_{SP}$ $SP-1 \rightarrow SP$	•	•	•	•	•	•
PULL DATA	PULA													33	4	1	$SP+1 \rightarrow SP$, $M_{SP} \rightarrow A$	•	•	•	•	•	•
	PULB													33	4	1	$SP+1 \rightarrow SP$, $M_{SP} \rightarrow B$	•	•	•	•	•	•
ROTATE LEFT	ROL							69	6	2	79	6	3					•	•	↕	↕	⑥	↕
	ROLA													49	2	1		•	•	↕	↕	⑥	↕
	ROLB													59	2	1		•	•	↕	↕	⑥	↕
ROTATE RIGHT	ROR							66	6	2	76	6	3					•	•	↕	↕	⑥	↕
	RORA													46	2	1		•	•	↕	↕	⑥	↕
	RORB													56	2	1		•	•	↕	↕	⑥	↕
SHIFT LEFT Arithmetic	ASL							66	6	2	78	6	3					•	•	↕	↕	⑥	↕
	ASLA													48	2	1		•	•	↕	↕	⑥	↕
	ASLB													58	2	1		•	•	↕	↕	⑥	↕
DOUBLE SHIFT LEFT, Arithmetic	ASLD													05	3	1		•	•	↕	↕	⑥	•
SHIFT RIGHT Arithmetic	ASR							67	6	2	77	6	3					•	•	↕	↕	⑥	↕
	ASRA													47	2	1		•	•	↕	↕	⑥	↕
	ASRB													57	2	1		•	•	↕	↕	⑥	↕
SHIFT RIGHT, LOGICAL	LSR							64	6	2	74	6	3					•	•	↕	↕	⑥	↕
	LSRA													44	2	1		•	•	↕	↕	⑥	↕
	LSRB													54	2	1				↕	↕		↕
DOUBLE SHIFT RIGHT LOGICAL	LSRD													04	3	1		•	•	R	↕	⑥	↕
																		•	•	R	↕	6	↕
STORE ACCUMULATOR	STAA				97	3	2	A7	4	2	B7	4	3				A→M	•	•	↕	↕	R	•
	STAB				D7	3	2	E7	4	2	B7	4	3				B→M	•	•	↕	↕	R	•
STORE DOUBLE ACCUMULATOR	STAD				DD	4	2	ED	5	2	FD	5	3				A→M B→M+1	•	•	↕ ↕		R	•
SUBTRACT	SUBA	80	2	2	90	3	2	A0	4	2	B0	4	3				A−M→A	•	•	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	4	2	F0	4	3				B−M→B	•	•	↕	↕	↕	↕
DOUBLE SUBTRACT	SUBD	83	4	3	93	5	2	A3	6	2	B3	6	3				A:B−M:M+1→AB	•	•	↕	↕	↕	↕
SUBTRACT ACCUMULATORS	SBA													10	2	1	A−B→A	•	•	↕	↕	↕	↕
SUBTRACT WITH CARRY	SBCA	82	2	2	92	3	2	A2	4	2	B2	4	3				A−M−C→A	•	•	↕	↕	↕	↕
	SBCD	C2	2	2	D2	2	2	E2	4	2	F2	4	3				B−M−C→B	•	•	↕	↕	↕	↕
TRANSFER ACCUMULATORS	TAB													16	2	1	A→B	•	•	↕	↕	R	•
	TBA													16	2	1	A→B	•	•	↕	↕	R	•
TEST ZERO OR MINUS	TST							6D	6	2	7D	6	3				M−00	•	•	↕	↕	R	R
	TSTB													5D	2	1	B−00	•	•	↕	↕	R	R

The Condition Code Register notes are listed after Table 10.

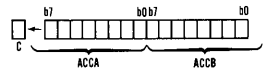
Added Instructions

In addition to the existing S6800 Instruction Set, the following new instructions are incorporated in the S6801 Microcomputer.

ABX Adds the 8-bit unsigned accumulator B to the 16-bit X-Register taking into account the possible carry out of the low order byte of the X-Register — IX ← IX + ACCB

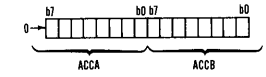
ADDD Adds the double precision ACCD* to the double precision value M:M + 1 and places the results in ACCD. — ACCD ← (ACCD) + (M:M + 1)

ASLD Shifts all bits of ACCAB one place to the left. Bit 0 is loaded with zero. The C bit is loaded from the most significant bit of ACCD.



LDD Loads the contents of double precision memory location into the double accumulator A:B. The condition codes are set according to the data. — ACCD ← (M:M + 1)

LSRD Shifts all bits of ACCD one place to the right. Bit 15 is loaded with zero. The C bit is loaded from the least significant bit to ACCD.



MUL Multiplies the 8 bits in accumulator A with the 8 bits in accumulator B to obtain a 16-bit unsigned number in A:B. ACCA contains MSB of result. — ACCD ← ACCA * ACCB

PSHX The contents of the index register is pushed onto the stack at the address contained in the stack pointer. The stack pointer is decremented by 2. — ↓(IXL), SP ← (SP) − 1; ↓(IXL), SP ← (SP) − 1

PULX The index register is pulled from the stack beginning at the current address contained in the stack pointer + 1. The stack pointer is incremented by 2 in total. — SP ← (SP) + 1; IXH; SP ← (SP) + 1; IHL

STD Stores the contents of double accumulator A:B in memory. The contents of ACCD remain unchanged. — M:M + 1 ← (ACCD)

* ACCD is the 16-bit register (A:B) formed by concatenating the A and B accumulators. The A-accumulator is the most significant byte.

Table 8. Index Register and Stack Manipulation Instructions

		IMMED.			DIRECT			INDEX			EXTEND			IMPLIED				COND. CODE REG.					
																		5	4	3	2	1	0
POINTER OPERATIONS	**MNEMONIC**	**OP**	**~**	**#**	**OP**	**~**	**#**	**OP**	**~**	**#**	**OP**	**~**	**#**	**OP**	**~**	**#**	**Boolean/Arithmetic Operation**	**H**	**I**	**N**	**Z**	**V**	**C**
Compare Index Reg	CPX	8C	4	3	9C	5	2	AC	6	2	BC	6	3				$X_H - M, X_L - (M+1)$	•	•	⑦	↕	⑧	•
Decrement Index Reg	DEX													09	3	1	$X - 1 \rightarrow X$	•	•	•	↕	•	•
Decrement Stack Pointer	DES													34	3	1	$SP - 1 \rightarrow SP$	•	•	•	•	•	•
Increment Index Reg	INX													08	3	1	$X + 1 \rightarrow X$	•	•	•	↕	•	•
Increment Stack Pointer	INS													31	3	1	$1SP + 1 \rightarrow SP$	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	5	2	FE	5	3				$M \rightarrow X_H, (M+1) \rightarrow X_L$	•	•	⑨	↕	R	•
Load Stack Pointer	LDS	8E	3	3	9E	4	2	AE	5	2	BE	5	3				$M \rightarrow SP_H, (M+1) \rightarrow SP_L$	•	•	⑨	↕	R	•
Store Index Reg	STX				DF	4	2	EF	5	2	FF	5	3				$X_H \rightarrow M, X_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Store Stack Pointer	STS				9F	5	2	AF	7	2	BF	6	3				$SP_H \rightarrow M, SP_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Index Reg → Stack Pointer	TXS													35	3	1	$X - 1 \rightarrow SP$	•	•	•	•	•	•
Stack Pointer → Index Reg	TSX													30	3	1	$SP + 1 \rightarrow X$	•	•	•	•	•	•
Add	ABX													3A	3	1	$B + X \rightarrow X$	•	•	•	•	•	•
Push Data	PSHX													3C	3	1	$X_L \rightarrow M_{SP}, SP - 1 \rightarrow SP$; $X_H \rightarrow H_{SP}, SP - 1 \rightarrow SP$	•	•	•	•	•	•
Pull Data	PULX													30	5	1	$SP + 1 \rightarrow SP, M_{SP} \rightarrow X_H$; $SP + 1 \rightarrow SP, M_{SP} \rightarrow X_L$	•	•	•	•	•	•

The Condition Code Register notes are listed after Table 10

Table 9. Jump and Branch Instructions

OPERATIONS	MNEMONIC	RELATIVE OP	RELATIVE ~	RELATIVE #	INDEX OP	INDEX ~	INDEX #	EXTND OP	EXTND ~	EXTND #	IMPLIED OP	IMPLIED ~	IMPLIED #	BRANCH TEST	COND. CODE REG. 5 H	4 I	3 N	2 Z	1 V	0 C
Branch Always	BRA	20	4	2										None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	4	2										C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	4	2										C = 1	•	•	•	•	•	•
Branch If = 0	BEQ	27	4	2										Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	4	2										N ⊕ V = 0	•	•	•	•	•	•
Branch If >Zero	BGT	2E	4	2										Z + (N ⊕ V) = 0	•	•	•	•	•	•
Branch If Higher	BHI	22	4	2										C + Z = 0	•	•	•	•	•	•
Branch If ≤ Zero	BLE	2F	4	2										Z + (N ⊕ V) = 1	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	4	2										C + Z = 1	•	•	•	•	•	•
Branch If < Zero	BLT	2D	4	2										N ⊕ V = 1	•	•	•	•	•	•
Branch If Minus	BMI	28	4	2										N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	20	4	2										Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	4	2										V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	4	2										V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	4	2										N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	8	2											•	•	•	•	•	•
Jump	JMP				6E	4	2	7E	3	3				See Special Operations	•	•	•	•	•	•
Jump To Subroutine	JSR				AD	8	2	8D	9	3					•	•	•	•	•	•
No Operation	NOP										01	2	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI										3B	10	1		⑩					
Return From Subroutine	RTS										39	5	1		•	•	•	•	•	•
Software Interrupt	SWI										3F	12	1	See Special Operations	•	•	•	•	•	•
Wait For Interrupt*	WAI										3E	9	1		•	⑪	•	•	•	•

Table 10. Condition Code Register Manipulation Instructions

OPERATIONS	MNEMONIC	IMPLIED OP	IMPLIED ~	IMPLIED #	BOOLEAN OPERATION	COND. CODE REG. 5 H	4 I	3 N	2 Z	1 V	0 C
Clear Carry	CLC	0C	2	1	0→C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	0→1	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	0→V	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	1→C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	1→1	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	1→V	•	•	•	•	S	•
Accumulator A→CCR	TAP	06	2	1	A→CCR	⑫					
CCR→Accumulator A	TPA	07	2	1	CCR→A	•	•	•	•	•	•

CONDITION CODE REGISTER NOTES: (Bit set if test is true and cleared otherwise).

1 (Bit V) Test Result = 10000000?
2 (Bit C) Test Result = 00000000?
3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4 (Bit V) Test: Operand = 10000000 prior to execution?
5 (Bit V) Test: Operand = 01111111 prior to execution?
6 (Bit V) Test: Set equal to result of N⊕C after shift has occurred.
7 (Bit N) Test: Sign Bit of most significant (MS) byte = 1?
8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
10 (All) Load Condition Code Register from Stack. (See Special Operations)
11 (Bit I) Set when interrupt occurs. If previously set, a Non-Maskable Interrupt as required to exit the wait state.
12 (All) Set according to the contents of Accumulator A.

Figure 25. Special Operations

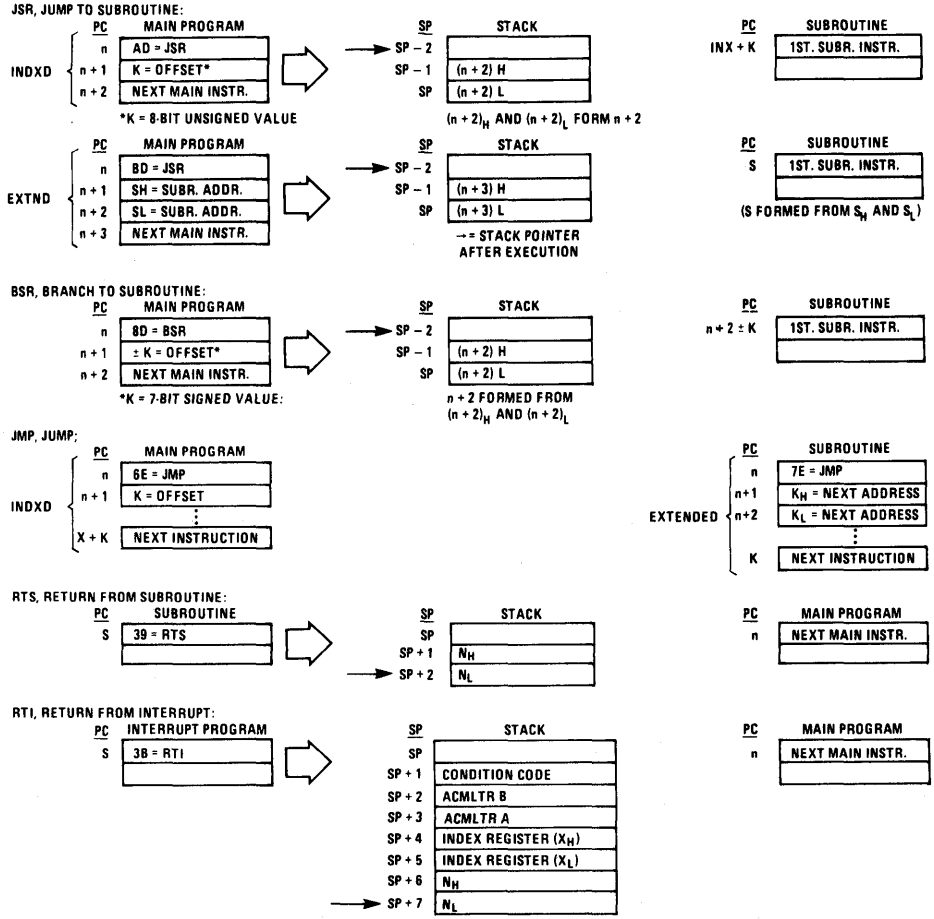


Table 11. Instruction Execution Times in Machine Cycle

	ACCX	IMMEDIATE	DIRECT	EXTENDED	INDEXED	INHERENT	RELATIVE		ACCX	IMMEDIATE	DIRECT	EXTENDED	INDEXED	INHERENT	RELATIVE
ABA	•	•	•	•	•	2	•	INX	•	•	•	•	•	3	•
ABX	•	•	•	•	•	3	•	JMP	•	•	•	3	3	•	•
ADC	•	2	3	4	4	•	•	JSR	•	•	5	6	6	•	•
ADD	•	2	3	4	4	•	•	LDA	•	2	3	4	4	•	•
ADDD	•	4	5	6	6	•	•	LDD	•	3	4	5	5	•	•
AND	•	2	3	4	4	•	•	LDS	•	3	4	5	5	•	•
ASL	2	•	•	6	6	•	•	LDX	•	3	4	5	5	•	•
ASLD	•	•	•	•	•	3	•	LSR	2	•	•	6	6	•	•
ASR	2	•	•	6	6	•	•	LSRD	•	•	•	•	•	3	•
BCC	•	•	•	•	•	•	3	MUL	•	•	•	•	•	10	•
BCS	•	•	•	•	•	•	3	NEG	2	•	•	6	6	•	•
BEQ	•	•	•	•	•	•	3	NOP	•	•	•	•	•	2	•
BGE	•	•	•	•	•	•	3	ORA	•	2	3	4	4	•	•
BGT	•	•	•	•	•	•	3	PSH	3	•	•	•	•	•	•
BHI	•	•	•	•	•	•	3	PSHX	•	•	•	•	•	4	•
BIT	•	2	3	4	4	•	•	PUL	4	•	•	•	□	•	•
BLE	•	•	•	•	•	•	3	PULX	•	•	•	•	•	5	•
BLS	•	•	•	•	•	•	3	ROL	2	•	•	6	6	•	•
BLT	•	•	•	•	•	•	3	ROR	2	•	•	6	6	•	•
BMI	•	•	•	•	•	•	3	RTI	•	•	•	•	•	10	•
BNE	•	•	•	•	•	•	3	RTS	•	•	•	•	•	6	•
BPL	•	•	•	•	•	•	3	SBA	•	•	•	•	•	2	•
BRA	•	•	•	•	•	•	3	SBC	•	2	3	4	4	•	•
BSR	•	•	•	•	•	•	6	SEC	•	•	•	•	•	2	•
BVC	•	•	•	•	•	•	3	SEI	•	•	•	•	•	2	•
BVS	•	•	•	•	•	•	3	SEV	•	•	•	•	•	2	•
CBA	•	•	•	•	•	2	•	STA	•	•	3	4	4	•	•
CLC	•	•	•	•	•	2	•	STD	•	•	4	5	5	•	•
CLI	•	•	•	•	•	2	•	STS	•	•	4	5	6	•	•
CLR	2	•	•	6	6	•	•	STX	•	•	4	5	5	•	•
CLV	•	•	•	•	•	2	•	SUB	•	4	5	6	6	•	•
CMP	•	2	3	4	4	•	•	SUBD	•	4	5	6	6	•	•
COM	2	•	•	6	6	•	•	SWI	•	•	•	•	•	12	•
CPX	•	4	5	6	6	•	•	TAB	•	•	•	•	•	2	•
DAA	•	•	•	•	•	2	•	TAP	•	•	•	•	•	2	•
DEC	2	•	•	6	6	•	•	TBA	•	•	•	•	•	2	•
DES	•	•	•	•	•	3	•	TPA	•	•	•	•	•	2	•
DEX	•	•	•	•	•	3	•	TST	•	•	•	6	6	•	•
EOR	•	2	3	4	4	•	•	TSX	•	•	•	•	•	2	•
INC	2	•	•	6	6	•	•	TXS	•	•	•	•	•	3	•
INS	•	•	•	•	•	3	•	WAI	•	•	•	•	•	9	•

Summary of Cycle by Cycle Operation

Table 12 provides a detailed description of the information present on the Address Bus, Data Bus, and the Read/Write line (R/W) during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hardware as the control program is executed. The information is categorized in groups according to addressing mode and number of cycles per instruction. (In general, instructions with the same addressing mode and number of cycles execute in the same manner; exceptions are indicated in the table).

Table 12. Cycle by Cycle Operation

ADDRESS MODE & INSTRUCTIONS	CYCLE	CYCLE #	ADDRESS BUS	R/W LINE	DATA BUS
IMMEDIATE					
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	2	1 2	OP CODE ADDRESS OP CODE ADDRESS + 1	1 1	OP CODE OPERAND DATA
LDS LDX	3	1 2 3	OP CODE ADDRESS OP CODE ADDRESS + 1 OP CODE ADDRESS + 2	1 1 1	OP CODE OPERAND DATA (High Order Byte) OPERAND DATA (Low Order Byte)
CPX SUBD ADDD	4	1 2 3 4	OP CODE ADDRESS OP CODE ADDRESS + 1 OP CODE ADDRESS + 2 ADDRESS BUS FFFF	1 1 1 1	OP CODE OPERAND DATA (High Order Byte) OPERAND DATA (Low Order Byte) LOW BYTE OF RESTART VECTOR
DIRECT					
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	3	1 2 3	OP CODE ADDRESS OP CODE ADDRESS + 1 ADDRESS OF OPERAND	1 1 1	OP CODE ADDRESS OF OPERAND OPERAND DATA
STA	3	1 2 3	OP CODE ADDRESS OP CODE ADDRESS + 1 DESTINATION ADDRESS	1 1 0	OP CODE DESTINATION ADDRESS DATA FROM ACCUMULATOR
LDS LDX LDD	4	1 2 3 4	OP CODE ADDRESS OP CODE ADDRESS + 1 ADDRESS OF OPERAND OPERAND ADDRESS + 1	1 1 1 1	OP CODE ADDRESS OF OPERAND OPERAND DATA (High Order Byte) OPERAND DATA (Low Order Byte)
STS STX STD	4	1 2 3 4	OP CODE ADDRESS OP CODE ADDRESS + 1 ADDRESS OF OPERAND ADDRESS OF OPERAND + 1	1 1 0 0	OP CODE ADDRESS OF OPERAND REGISTER DATA (High Order Byte) REGISTER DATA (Low Order Byte)
CPX SUBD ADDD	5	1 2 3 4 5	OP CODE ADDRESS OP CODE ADDRESS + 1 OPERAND ADDRESS OPERAND ADDRESS + 1 ADDRESS BUS FFFF	1 1 1 1 1	OP CODE ADDRESS OF OPERAND OPERAND DATA (High Order Byte) OPERAND DATA (Low Order Byte) LOW BYTE OF RESTART VECTOR
JSR	5	1 2 3 4 5	OP CODE ADDRESS OP CODE ADDRESS + 1 SUBROUTINE ADDRESS STACK POINTER STACK POINTER + 1	1 1 1 0 0	OP CODE IRRELEVANT DATA FIRST SUBROUTINE OP CODE RETURN ADDRESS (High Order Byte) RETURN ADDRESS (Low Order Byte)

(continued)

Table 12. Cycle by Cycle Operation (continued)

ADDRESS MODE & INSTRUCTIONS	CYCLE	CYCLE #	ADDRESS BUS	R/W LINE	DATA BUS
INDEXED					
JMP	3	1	OP CODE ADDRESS	1	OP CODE
		2	OP CODE ADDRESS + 1	1	OFFSET
		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
ADC EOR	4	1	OP CODE ADDRESS	1	OP CODE
ADD LDA		2	OP CODE ADDRESS + 1	1	OFFSET
AND ORA		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
BIT SBC		4	INDEX REGISTER PLUS OFFSET	1	OPERAND DATA
CMP SUB					
STA	4	1	OP CODE ADDRESS	1	OP CODE
		2	OP CODE ADDRESS + 1	1	OFFSET
		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
		4	INDEX REGISTER PLUS OFFSET	0	OPERAND DATA
LDS	5	1	OP CODE ADDRESS	1	OP CODE
LDX		2	OP CODE ADDRESS + 1	1	OFFSET
LDD		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
		4	INDEX REGISTER PLUS OFFSET	1	OPERAND DATA (High Order Byte)
		5	INDEX REGISTER + 1	1	OPERAND DATA (Low Order Byte)
STS	5	1	OP CODE ADDRESS	1	OP CODE
STX		2	OP CODE ADDRESS + 1	1	OFFSET
STD		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
		4	INDEX REGISTER PLUS OFFSET	0	OPERAND DATA (High Order Byte)
		5	INDEX REGISTER PLUS OFFSET	0	OPERAND DATA (Low Order Byte)
ASL LSR	6	1	OP CODE ADDRESS	1	OP CODE
ASR NEG		2	OP CODE ADDRESS + 1	1	OFFSET
CLR ROL		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
COM ROR		4	INDEX REGISTER PLUS OFFSET	1	CURRENT OPERAND DATA
DEC TST (1)		5	ADDRESS BUS FFFF	1	CURRENT OPERAND DATA
INC		6	INDEX REGISTER PLUS OFFSET	0	NEW OPERAND DATA
CPX	6	1	OP CODE ADDRESS	1	OP CODE
SUBD		2	OP CODE ADDRESS + 1	1	OFFSET
ADDD		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
		4	INDEX REGISTER + OFFSET	1	OPERAND DATA (High Order Byte)
		5	INDEX REGISTER + OFFSET	1	OPERAND DATA (Low Order Byte)
		6	ADDRESS BUS FFFF		LOW BYTE OF RESTART VECTOR
JSR	6	1	OP CODE ADDRESS	1	OP CODE
		2	OP CODE ADDRESS + 1	1	OFFSET
		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
		4	INDEX REGISTER + OFFSET	1	FIRST SUBROUTINE OP CODE
		5	STACK POINTER	0	RETURN ADDRESS (Low Order Byte
		6	STACK POINTER + 1	0	RETURN ADDRESS (High Order Byte)
EXTENDED					
JMP	3	1	OP CODE ADDRESS	1	OP CODE
		2	OP CODE ADDRESS + 1	1	JUMP ADDRESS (High Order Byte)
		3	OP CODE ADDRESS	1	JUMP ADDRESS (Low Order Byte)

(continued)

Table 12. Cycle by Cycle Operation (continued)

ADDRESS MODE & INSTRUCTIONS	CYCLE	CYCLE #	ADDRESS BUS	R/W LINE	DATA BUS
EXTENDED					
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	4	1 2 3 4	OP CODE ADDRESS OP CODE ADDRESS + 1 OP CODE ADDRESS + 2 ADDRESS OF OPERAND	1 1 1 1	OP CODE ADDRESS OF OPERAND ADDRESS OF OPERAND (Low Order Byte) OPERAND DATA
STA A STA B	4	1 2 3 4	OP CODE ADDRESS OP CODE ADDRESS + 1 OP CODE ADDRESS + 2 OPERAND DESTINATION ADDRESS	1 1 1 0	OP CODE DESTINATION ADDRESS (High Order Byte) DESTINATION ADDRESS (Low Order Byte) DATA FROM THE ACCUMULATOR
LDS LDX LDD	5	1 2 3 4 5	OP CODE ADDRESS OP CODE ADDRESS + 1 OP CODE ADDRESS + 2 ADDRESS OF OPERAND ADDRESS OF OPERAND + 1	1 1 1 1 1	OP CODE ADDRESS OF OPERAND (High Order Byte) ADDRESS OF OPERAND (Low Order Byte) OPERAND DATA (High Order Byte) OPERAND DATA (Low Order Byte)
STS STX STD	5	1 2 3 4 5	OP CODE ADDRESS OP CODE ADDRESS + 1 OP CODE ADDRESS + 2 ADDRESS OF OPERAND ADDRESS OF OPERAND	1 1 1 0 0	OP CODE ADDRESS OF OPERAND (High Order Byte) ADDRESS OF OPERAND (Low Order Byte) OPERAND DATA (High Order Byte) OPERAND DATA (Low Order Byte)
ASL LSR ASR NEG CLR ROL COM ROR DEC TST (1) INC	6	1 2 3 4 5 6	OP CODE ADDRESS OP CODE ADDRESS + 1 OP CODE ADDRESS + 2 ADDRESS OF OPERAND ADDRESS BUS FFFF ADDRESS OF OPERAND	1 1 1 1 1 0	OP CODE ADDRESS OF OPERAND (High Order Byte) ADDRESS OF OPERAND (Low Order Byte) CURRENT OPERAND DATA LOW BYTE OF RESTART VECTOR NEW OPERAND DATA
CPX SUBD ADDD	6	1 2 3 4 5 6	OP CODE ADDRESS OP CODE ADDRESS + 1 OP CODE ADDRESS + 2 OPERAND ADDRESS OPERAND ADDRESS + 1 ADDRESS BUS FFFF	1 1 1 1 1	OP CODE OPERAND ADDRESS OPERAND ADDRESS (Low Order Byte) OPERAND DATA (High Order Byte) OPERAND DATA (Low Order Byte) LOW BYTE OF RESTART VECTOR
JSR	6	1 2 3 4 5 6	OP CODE ADDRESS OP CODE ADDRESS + 1 OP CODE ADDRESS + 2 SUBROUTINE STARTING ADDRESS STACK POINTER STACK POINTER – 1	1 1 1 1 0 0	OP CODE ADDRESS OF SUBROUTINE (High Order Byte) ADDRESS OF SUBROUTINE (High Order Byte) OP CODE OF NEXT INSTRUCTION RETURN ADDRESS (Low Order Byte ADDRESS OF OPERAND (High Order Byte)
INHERENT					
ABA DAA SEC ASL DEC SEI ASR INC SEV CBA LSR TAB CLC NEG TAP CLI NOP TBA CLR ROL TPA CLV ROR TST COM SBA	2	1 2	OP CODE ADDRESS OP CODE ADDRESS + 1	1 1	OP CODE OP CODE OF NEXT INSTRUCTION

(continued)

Table 12. Cycle by Cycle Operation (continued)

ADDRESS MODE & INSTRUCTIONS	CYCLE	CYCLE #	ADDRESS BUS	R/W LINE	DATA BUS
INHERENT					
ABX	3	1	OP CODE ADDRESS	1	OP CODE
		2	OP CODE ADDRESS + 1	1	IRRELEVANT DATA
		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
ASLD	3	1	OP CODE ADDRESS	1	OP CODE
LSRD		2	OP CODE ADDRESS + 1	1	IRRELEVANT DATA
		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
DES	3	1	OP CODE ADDRESS	1	OP CODE
INS		2	OP CODE ADDRESS + 1	1	OP CODE OF NEXT INSTRUCTION
		3	PREVIOUS REGISTER CONTENTS	1	IRRELEVANT DATA
INX	3	1	OP CODE ADDRESS	1	OP CODE
DEX		2	OP CODE ADDRESS + 1	1	OP CODE OF NEXT INSTRUCTION
		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
PSHA	3	1	OP CODE ADDRESS	1	OP CODE
PSHB		2	OP CODE ADDRESS + 1	1	OP CODE OF NEXT INSTRUCTION
		3	STACK POINTER	0	ACCUMULATOR DATA
ISX	3	1	OP CODE ADDRESS	1	OP CODE
		2	OP CODE ADDRESS + 1	1	OP CODE OF NEXT INSTRUCTION
		3	STACK POINTER	1	IRRELEVANT DATA
TXS	3	1	OP CODE ADDRESS	1	OP CODE
		2	OP CODE ADDRESS + 1	1	OP CODE OF NEXT INSTRUCTION
		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
PULA	4	1	OP CODE ADDRESS	1	OP CODE
PULB		2	OP CODE ADDRESS + 1	1	OP CODE OF NEXT INSTRUCTION
		3	STACK POINTER	1	IRRELEVANT DATA
		4	STACK POINTER	1	
PSHX	4	1	OP CODE ADDRESS	1	OP CODE
		2	OP CODE ADDRESS + 1	1	IRRELEVANT DATA
		3	STACK POINTER	0	INDEX REGISTER (Low Order Byte)
		4	STACK POINTER – 1	0	INDEX REGISTER (High Order Byte)
PULX	5	1	OP CODE ADDRESS	1	OP CODE
		2	OP CODE ADDRESS + 1	1	IRRELEVANT DATA
		3	STACK POINTER	1	IRRELEVANT DATA
		4	STACK POINTER + 1	1	INDEX REGISTER (High Order Byte)
		5	STACK POINTER + 2	1	INDEX REGISTER (Low Order Byte)
BCC BHT BNE	3	1	OP CODE ADDRESS	1	OP CODE
BCS BLE BPL		2	OP CODE ADDRESS + 1	1	BRANCH OFFSET
BEQ BLS BRA		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
BGE BLT BVC					
BGT BMT BVS					
BSR	6	1	OP CODE ADDRESS	1	OP CODE
		2	OP CODE ADDRESS + 1	1	BRANCH OFFSET
		3	ADDRESS BUS FFFF	1	LOW BYTE OF RESTART VECTOR
		4	SUBROUTINE STARTING ADDRESS	1	RETURN ADDRESS (Low Order Byte)
		5	STACK POINTER	0	RETURN ADDRESS (Low Order Byte)
		6	STACK POINTER – 1	0	RETURN ADDRESS (High Order Byte)

Figure 26. S6801E MCU Single-Chip Mode

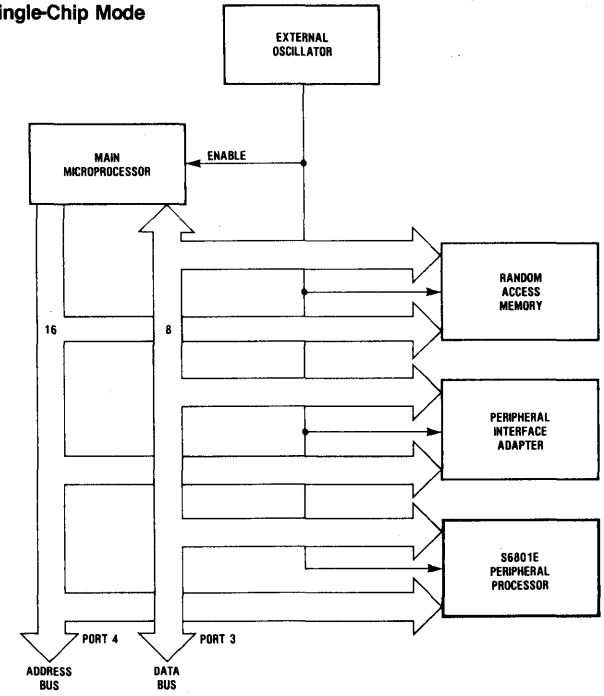


Figure 27. S6801 MCU Single-Chip Dual Processor Configuration

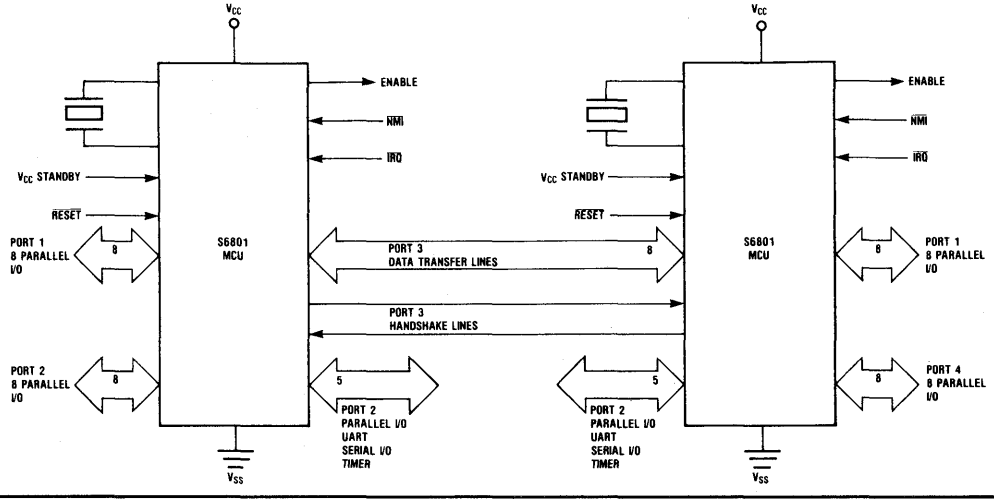


Figure 28. S6801 MCU Expanded Non-Multiplexed Mode

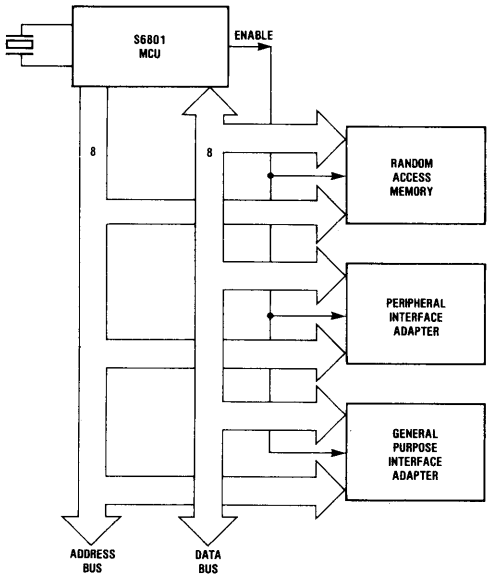


Figure 29. S6801E Expanded Non-Multiplexed Mode

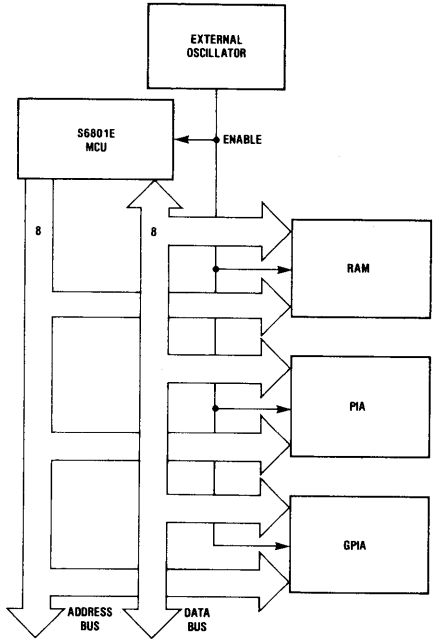


Figure 30. S6801 MCU Expanded Multiplexed Mode

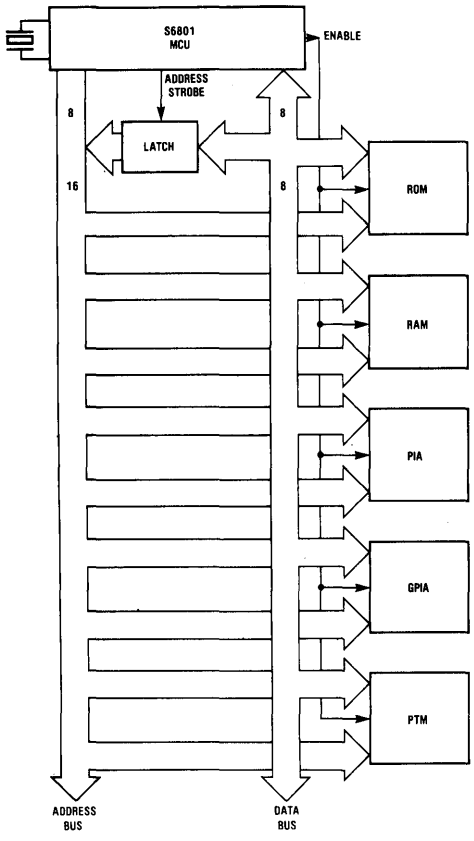


Figure 31. S6801E Expanded Multiplexed Mode

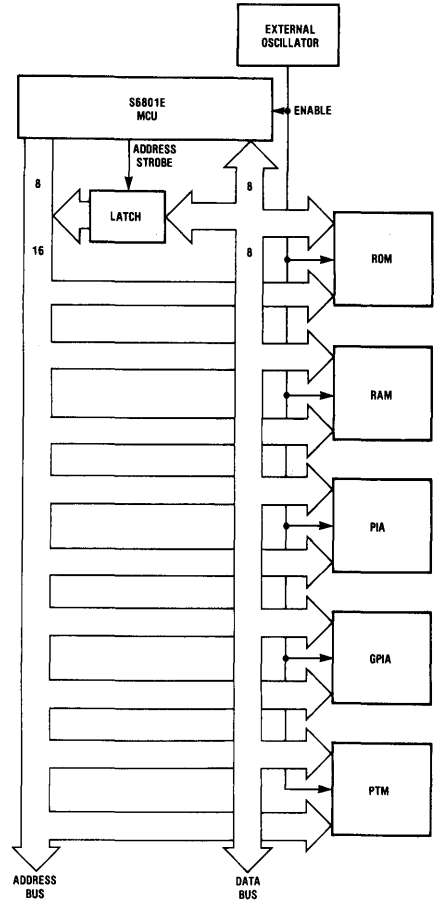


Table 13. Mode and Port Summary

MCU	MODE	PORT 1 Eight Lines	PORT 2 Five Lines	PORT 3 Eight Lines	PORT 4 Eight Lines	CC1	CC2	SC1	SC2
	SINGLE CHIP	I/O	I/O	I/O	I/O	XTAL1(I)	XTAL2(I)	IS3(O)	OS3(O)
S6801	EXPANDED MUX	I/O	I/O	ADDRESS BUS (A0-A7) DATA BUS (D0-D7)	ADDRESS BUS* (A8-A15)	XTAL1(I)	XTAL2(I)	AS(O)	R/$\overline{W}$(O)
	EXPANDED NON-MUX	I/O	I/O	DATA BUS (D0-D7)	ADDRESS BUS* (A0-A7)	XTAL1(I)	XTAL2(I)	IOS(O)	R/$\overline{W}$(O)
	SINGLE CHIP	I/O	I/O	ADDRESS BUS (D0-D7)	I/O	R/$\overline{W}$(I)	RSO(I)	CS3(I)	OS3(O)
S6801E	EXPANDED MUX	I/O	I/O	ADDRESS BUS (A0-A7) DATA BUS (D0-D7)	ADDRESS BUS* (A8-A15)	$\overline{HALT}$(I)	BA(O)	AS(O)	R/$\overline{W}$(O)
	EXPANDED NON-MUX	I/O	I/O	DATA BUS (D0-D7)	ADDRESS BUS* (A0-A7)	$\overline{HALT}$(I)	BA(O)	AS(O)	R/$\overline{W}$(O)

*These lines can be substituted for I/O (Input Only) starting with the most significant address line.

I = Input
O = Output
BA = Bus Available
R/$\overline{W}$ = Read/$\overline{Write}$
CC = Crystal Control
IS = Input Strobe
OS = Output Strobe
IOS = I/O Select
CS = Chip Select
AS = Address Strobe
SC = Strobe Control

A Subsidiary of Gould Inc.

S6802/A/B/S6808/A/B

MICROPROCESSOR WITH CLOCK AND RAM

Features

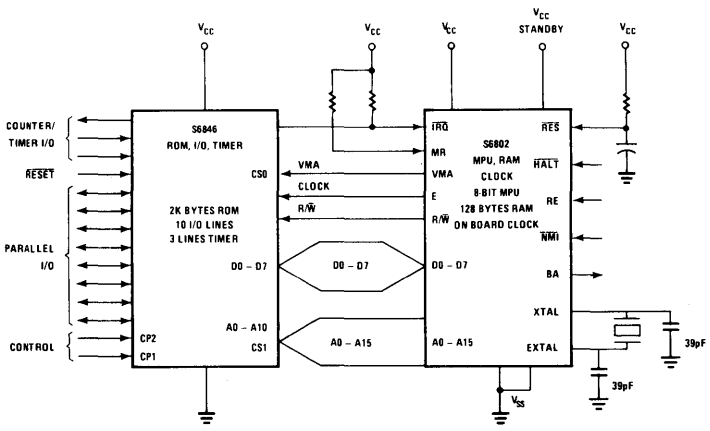
- ☐ On-Chip Clock Circuit
- ☐ 128x8-Bit On-Chip RAM (S6802)
- ☐ 32 Bytes of RAM Are Retainable (S6802)
- ☐ Software-Compatible With the S6800
- ☐ Expandable to 64K Words
- ☐ Standard TTL-Compatible Inputs and Outputs
- ☐ 8-Bit Word Size
- ☐ 16-Bit Memory Addressing
- ☐ Interrupt Capability
- ☐ Clock Rates:
  S6802/S6808—1.0MHz
  S68A02/S68A08—1.5MHz
  S68B02/S68B08—2.0MHz

General Description

The S6802/S6808 are monolithic 8-bit microprocessors that contain all the registers and accumulators of the present S6800 plus an internal clock oscillator and driver on the same chip. In addition, the S6802 has 128 bytes of RAM on board located at hex addresses 0000 to 007E. The first 32 bytes of RAM, at addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation. The S6808 is functionally identical to the S6802 except for the 128 bytes of RAM. The S6808 does not have any RAM.

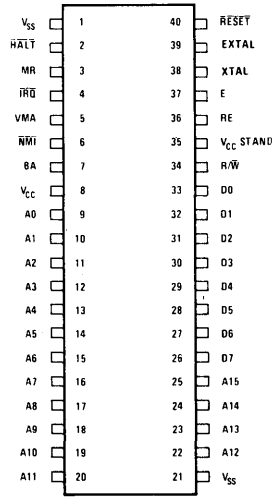
The S6802/S6808 are completely software compatible with the S6800 as well as the entire S6800 family of parts. Hence, the S6802/S6808 are expandable to 64K words. When the S6802 is interfaced with the S6846 ROM-I/O-Timer chip, as shown in the Block Diagram below, a basic 2-chip microcomputer system is realized.

Typical Microcomputer Block Diagram



BLOCK DIAGRAM OF A TYPICAL COST EFFECTIVE MICROCOMPUTER. THE MPU IS THE CENTER OF THE MICROCOMPUTER SYSTEM AND IS SHOWN IN A MINIMUM SYSTEM INTERFACING WITH A ROM COMBINATION CHIP. IT IS NOT INTENDED THAT THIS SYSTEM BE LIMITED TO THIS FUNCTION BUT THAT IT BE EXPANDABLE WITH OTHER PARTS IN THE S6800 MICROCOMPUTER FAMILY.

Pin Configuration



Absolute Maximum Ratings

Supply Voltage, V_{CC} ..... −0.3V to +7.0V
Input Voltage, V_{IN} ..... −0.3V to +7.0V
Operating Temperature Range, T_A ..... 0° to +70°C
Storage Temperature Range, T_{stg} ..... −55°C to +150°C
Thermal Resistance, θ_{JA}
Plastic ..... 100°C/W
Ceramic ..... 50°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

D.C. Characteristics:

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Logic, EXtal $\overline{RESET}$	$V_{SS}+2.0$ $V_{SS}+4.0$	— —	V_{CC} V_{CC}	V
V_{IL}	Input Low Voltage	Logic, EXtal, $\overline{RESET}$	$V_{SS}-0.3$	—	$V_{SS}+0.8$	V
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max)	Logic*	—	1.0	2.5	μA
V_{OH}	Output High Voltage					V
	(I_{LOAD} = −205μA, V_{CC} = Min)	D0-D7	$V_{SS}+2.4$	—	—	V
	(I_{LOAD} = −145μA, V_{CC} = Min)	A0-A15, R/$\overline{W}$, VMA, E	$V_{SS}+2.4$	—	—	V
	(I_{LOAD} = −100μA, V_{CC} = Min)	BA	$V_{SS}+2.4$	—	—	V
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mA, V_{CC} = Min)		—	—	$V_{SS}+0.4$	V
P_D	Power Dissipation	(Measured at T_A = 0°C)	—	0.600	1.2	W
C_{IN}	Capacitance # (V_{IN} = 0, T_A = 25°C, f = 1.0MHz	D0-D7	—	10	12.5	pF
		Logic Inputs, EXtal	—	6.5	10	
C_{OUT}		A0-A15, R/W, VMA	—	—	12	pF
V_{CC} Standby	V_{CC}		4.0	—	5.25	V
I_{DD} Standby	I_{DD} Standby		—	—	8.0	mA

Clock Timing (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	S6802/S6808			S68A02/S68A08			S68B02/S68B08			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
	Frequency of Operation										
f	Input Clock ÷ 4	0.1	—	1.0	0.1	—	1.5	.1	—	2	MHz
f_{Xtal}	Crystal Frequency	1.0	—	4.0	1.0	—	6.0	1.0	—	8	
t_{CYC}	Cycle Time	1.0	—	10	6.7	—	10	.50	—	10	μs
t_ϕ	Fall Time Measured between $V_{SS}+0.4V$ and $V_{SS}-2.4V$	—	—	25	—	—	25	—	—	25	ns

*Except IRQ and NMI, which require 3KΩ pull-up load resistors for wire-OR capability at optimum operation. Does not include Extal and Xtal, which are crystal inputs.
#Capacitance are periodically sampled rather than 100% tested.

Read/Write Timing (Figures 1 through 5; Load Circuit of Figure 3.)
(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted)

Symbol	Parameter	S6802/S6808			S68A02/S68A08			S68B02/S68B08			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{AD}	Address Delay C = 90pF C = 30pF		100	270			180 165			150 135	ns
t_{ACC}	Peripheral Read Access Time	575			360			250			ns
t_{DSR}	Data Setup Time Read	100			70			60			ns
t_{DHR}	Data Hold Time Read	10	30		10			10			ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	20			20			20			ns
t_{DDW}	Data Delay Time Write Processor Controls			225			170			160	ns
t_{DHW}	Data Hold Time Write	30			20			20			ns
t_{PCS}	Processor Control Setup Time	200			140			110			ns
t_{PCr}, t_{PCf}	Processor Control Rise and Fall Time			100			100			100	ns

Figure 1. Read Data from Memory or Peripherals

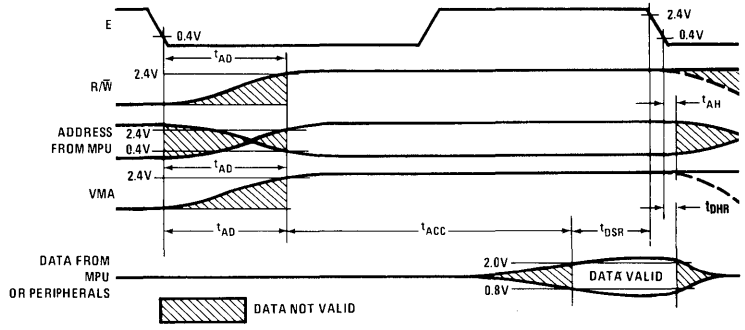


Figure 2. Write Data in Memory or Peripherals

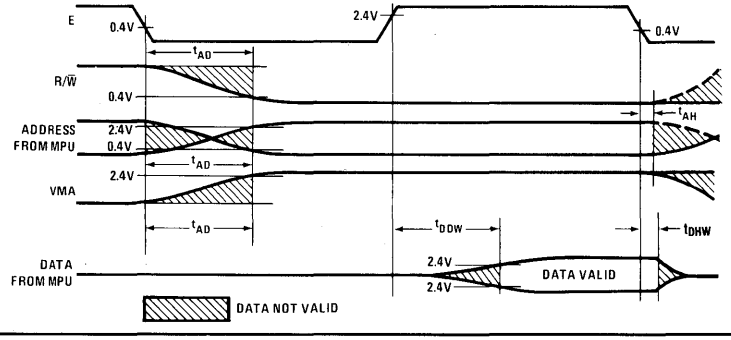
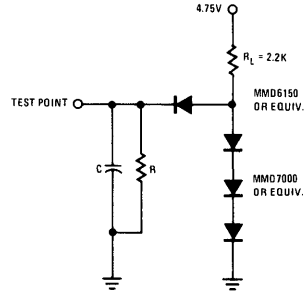


Figure 3. Bus Timing Test Load



C = 130pF FOR D0 – D7, E
= 90pF FOR A0 – A15, R/W, AND VMA
= 30pF FOR BA
R = 11.7 KΩ FOR D0 – D7, E
= 16.5KΩ FOR A0 – A15, R/W, AND VMA
= 24KΩ FOR BA

Figure 4. Typical Data Bus Output Delay Versus Capacitive Loading

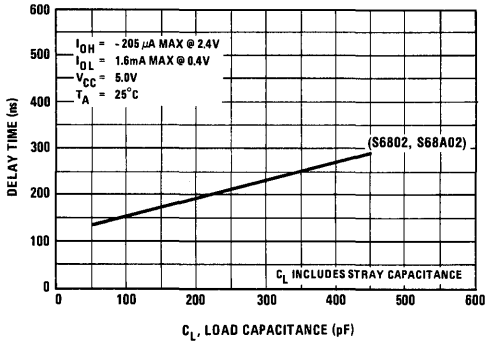


Figure 5. Typical Read/Write, VMA, and Address Output Delay Versus Capacitive Loading

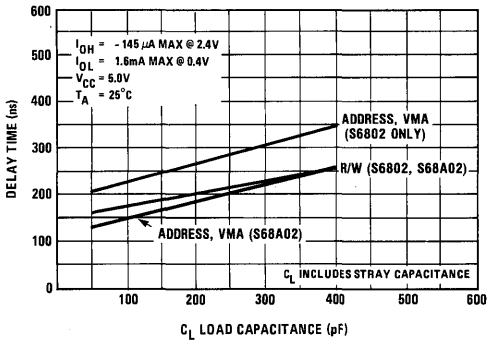
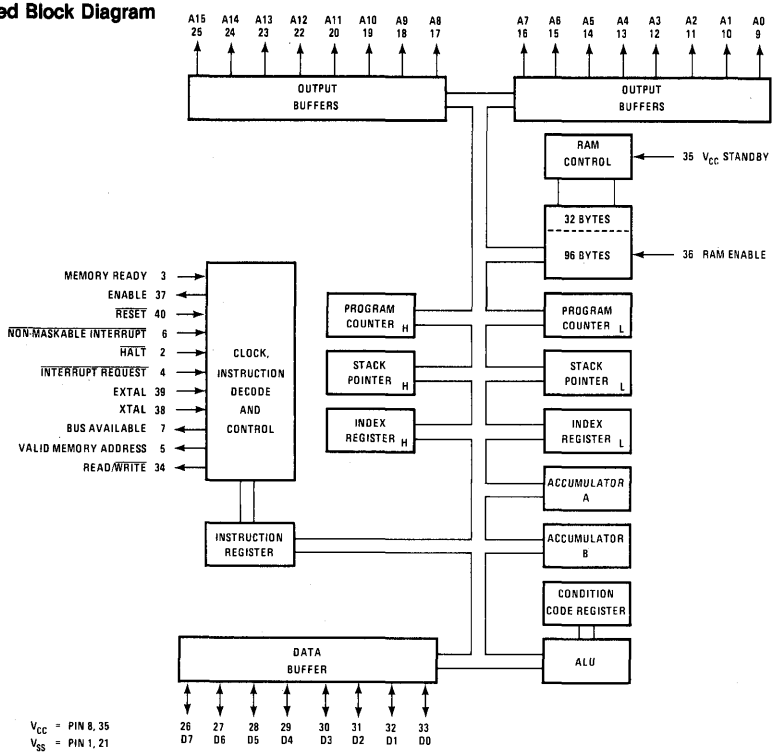


Figure 6. Expanded Block Diagram



S6800 FAMILY

Functional Description

MPU Registers

A general block diagram of the S6802 is shown in Figure 6. As shown, the number and configuration of the registers are the same as for the S6800. The 128x8 bit RAM has been added to the basic MPU. The first 32 bytes may be operated in a low power mode via a V_{CC} standby. These 32 bytes can be retained during power-up and power-down conditions via the RE signal.

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer (Figure 7).

Program Counter—The program counter is a two byte (16 bits) register that points to the current program address.

Stack Pointer—The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register—The index register is a two byte register that is used to store data or a sixteen-bit memory address for the Indexed mode of memory addressing.

Accumulators—The MPU contains two 8-bit accumulators that are used to hold operands and results from an arithmetic logic unit (ALU).

Condition Code Register—The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and Half Carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The used bits of the Condition Code Register (b6 and b7) are ones.

Figure 8 shows the order of saving the microprocessor status within the stack.

Figure 7. Programming Model of the Microprocessing Unit

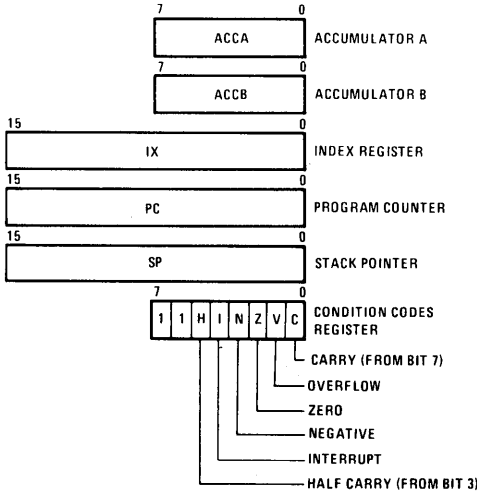
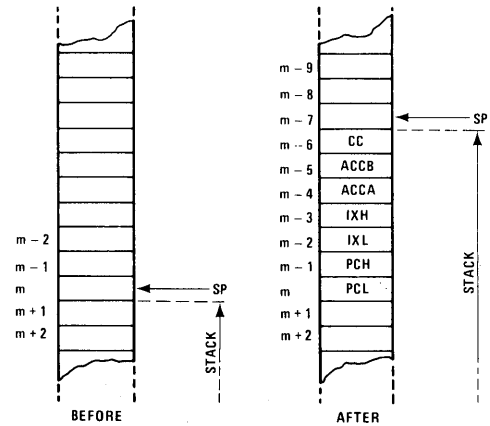


Figure 8. Saving the Status of the Microprocessor in the Stack



SP = STACK POINTER
CC = CONDITION CODES (ALSO CALLED THE PROCESSOR STATUS BYTE)
ACCB = ACCUMULATOR B
ACCA = ACCUMULATOR A
IXH = INDEX REGISTER, HIGHER ORDER 8 BITS
IXL = INDEX REGISTER, LOWER ORDER 8 BITS
PCH = PROGRAM COUNTER, HIGHER ORDER 8 BITS
PCL = PROGRAM COUNTER, LOWER ORDER 8 BITS

S6802/S6808 MPU Description

Proper operation of the MPU requires that certain control and timing signals be provided to accomplish specific functions and that other signal lines be monitored to determine the state of the processor. These control and timing signals for the S6802/S6808 are identical to those of the S6800 except that TSC, DBE, ϕ1, ϕ2 input, and two unused pins have been eliminated, and the following signal and timing lines have been added:

RAM Enable (RE)
Crystal Connections EXtal and Xtal
Memory Ready (MR)
V_{CC} Standby
Enable ϕ2 Output (E)

The following is a summary of the S6802/S6808 MPU signals:

Address Bus (A0-A15)—Sixteen pins are used for the address bus. The outputs are capable of driving one standard TTL load and 130pF.

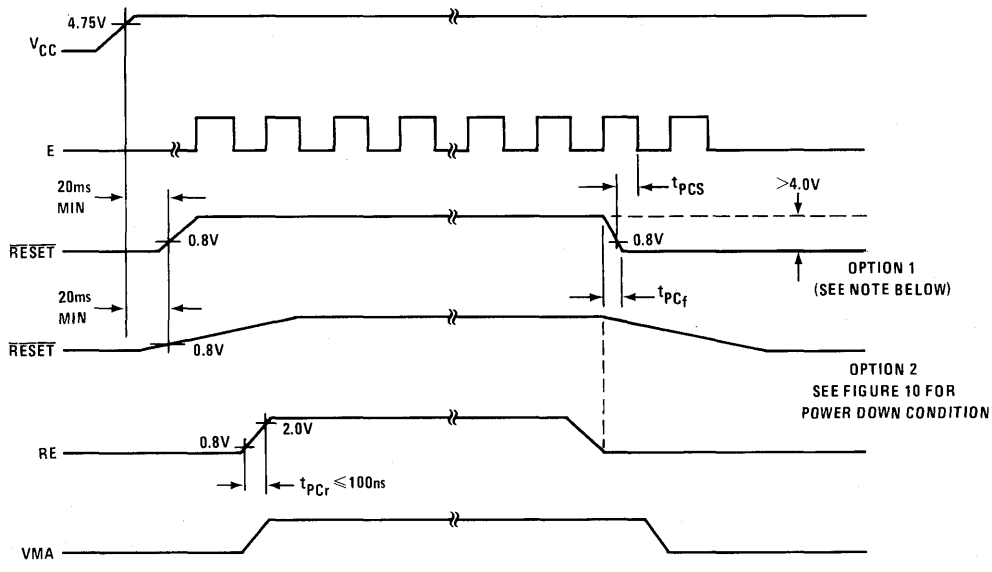
Data Bus (D0-D7)—Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state-output buffers capable of driving one standard TTL load and 130pF.

$\overline{\text{Halt}}$—When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a high state, Valid Memory Address will be at a low state, and all other three-state lines will be in the three-state mode. The address bus will display the address of the next instruction.

To insure single instruction operation, transition of the $\overline{\text{Halt}}$ line must not occur during the last 200ns of E and the $\overline{\text{Halt}}$ line must go high for one Clock cycle.

Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$)—This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high).

Figure 9. Power-up and Reset Timing



NOTE: IF OPTION 1 IS CHOSEN, $\overline{\text{RESET}}$ AND RE PINS CAN BE TIED TOGETHER.

S6800 FAMILY

When the processor is halted, it will be in the logical one state. This output is capable of driving one standard TTL load and 90pF.

Valid Memory Address (VMA)—This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 90pF may be directly driven by this active high signal.

Bus Available (BA)—The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or non-maskable interrupt. This output is capable of driving one standard TTL load and 30pF.

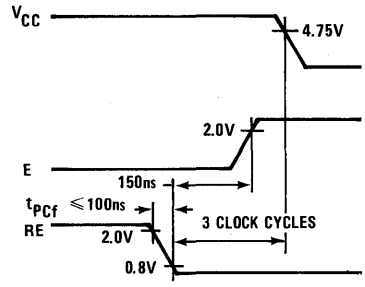
$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$)—This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while $\overline{\text{Halt}}$ is low.

The $\overline{\text{IRQ}}$ has a high impedance pull-up device internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

$\overline{\text{Reset}}$—This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. When this line is low, the MPU is inactive and the information in the registers will be lost. If a high level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. Power-up and reset timing and power-down sequences are shown in Figures 9 and 10, respectively.

Figure 10. Power-Down Sequence



When $\overline{\text{RESET}}$ is released it must go through the low to high threshhold without bouncing, oscillating, or otherwise causing an erroneous $\overline{\text{RESET}}$ (less than 3 clock cycles). This may cause improper MPU operation.

$\overline{\text{Reset}}$, when brought low, must be held low at least 3 clock cycles. This allows the S6802/S6808 adequate time to respond internally to reset. This function is independent of the 20ms power up reset that is required.

Non-Maskable Interrupt (NMI)—A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the NMI signal. The interrupt mask bit in the Condition Code Register has no effect on NMI.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations caused the MPU to branch to a non-maskable interrupt routine in memory.

NMI has a high impedance pull-up resistor internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs IRQ and MMI are hardware interrupt lines that are sampled when E is high and will start the interrupt routine on a low E following the completion of an instruction.

Figure 12 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 2 gives the memory map for interrupt vectors.

RAM Enable (RE)—A TTL-compatible RAM enable input controls the on-chip RAM of the S6802. When placed in the high state, the on-chip memory is enabled to respond to the MPU controls. In the low state, RAM is disabled. This pin may also be utilized to disable reading and writing the on-chip RAM during power-down situation. RAM enable must be low three clock cycles before V_{CC} goes below 4.75V during power-down to retain the on board RAM contents during V_{CC} standby.

The Data Bus will be in the output mode when the internal RAM is accessed, which prohibits external data from entering the MPU. Note that the internal RAM is fully decoded from $0000 to $007F and these locations must be disabled when internal RAM is accessed.

Extal and Xtal—The S6802/S6808 has an internal oscillator that may be crystal controlled. These connections are for a parallel resonant fundamental crystal. (AT cut) A divide-by-four circuit has been added to the S6802 so that a 4MHz crystal may be used in lieu of a 1MHz crystal for a more cost effective system. Pin 39 of the S6802/S6808 may be driven externally by a TTL input signal if a separate clock is required. Pin 38 is to be left open in this mode. If the external clock is used it may not be halted for more than 4.5μs. The S6802/S6808 is a dynamic part except for internal RAM, and requires the external clock to retain information. Figure 11a shows the crystal parameters. In applications where other than a 4.0MHz crystal is used, Table 1 gives the designer the crystal parameters to be specified. The table contains the entire spectrum of usable crystals for the S6802/S6808. Crystal frequencies not shown (that lie between 1.0MHz and 4.0MHz) may be interpolated from the table. Figure 11b shows the crystal connection.

Table 1. Crystal Parameters

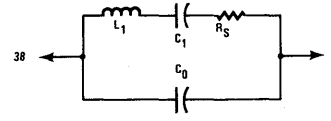
Y1 CRYSTAL FREQUENCY	C1 & C2	C LOAD	R1 (MAX)	C_0 (MAX)
4.0MHz	27pF	24pF	50 ohms	7.0pF
3.58MHz	27pF	20pF	50 ohms	7.0pF
3.0MHz	27pF	18pF	75 ohms	6.7pF
2.5MHz	27pF	18pF	74 ohms	6.0pF
2.0MHz	33pF	24pF	100 ohms	5.5pF
1.5MHz	39pF	27pF	200 ohms	4.5pF
1.0MHz	39pF	30pF	250 ohms	4.0pF

Table 2. Memory Map for Interrupt Vectors

VECTOR MS	VECTOR LS	DESCRIPTION
FFFE	FFFF	RESTART
FFFC	FFFD	NON-MASKABLE INTERRUPT
FFFA	FFFB	SOFTWARE INTERRUPT
FFF8	FFF9	INTERRUPT REQUEST

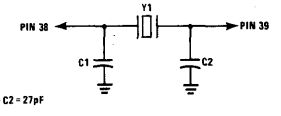
Note: Memory Read (MR), Halt, RAM Enable (RE) and Non-Maskable interrupt should always be tied to the correct high or low state if not used.

Figure 11a. Crystal Parameters



AT – Cut Parallel Resonance Crystal
C0 = 7pF Max.
FREQ = 4.0MHz @ C_L = 24pF
R_S = 50 ohms Max.
Frequency Tolerance – ±5% to ±0.02%
The best E output "Worst Case Design" tolerance is ± 0.05% (500ppM) using A ±0.02 crystal.

Figure 11b. Crystal Connection



Tolerance Note:

Critical timing loops may require a better tolerance than ±5%. Because of production deviations and the Temperature Coefficient of the S6802, the best "worst case design" tolerance is ±0.05%. (500 ppm) using a ±0.02% crystal. If the S6802 is not going to be used over its entire temperature range of 0°C to 70°C, a much tighter overall tolerance can be achieved.

S6800 FAMILY

A Subsidiary of Gould Inc.

S6805

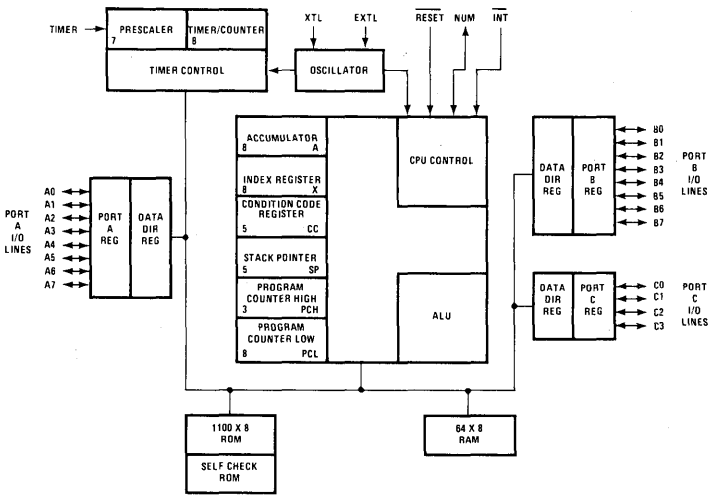
MICROCOMPUTER

Features

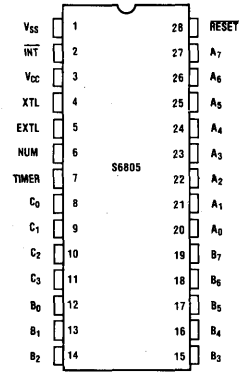
☐ Hardware
- 8-Bit Architecture
- 64 Bytes RAM
- 1100 Bytes ROM
- 116 Bytes of Self Check ROM
- 28-Pin Package
- Memory Mapped I/O
- Internal 8-Bit Timer with 7-Bit Prescaler
- Vectored Interrupts—External, Timer, Software, Reset
- 20 TTL/CMOS Compatible I/O Line 8 Lines LED Compatible
- On-Chip Clock Circuit
- Self-Check Capability
- Low Voltage Inhibit
- 5 Vdc Single Supply

☐ Software
- Similar to 6800
- Byte Efficient Instruction Set
- Versatile Interrupt Handling
- True Bit Manipulation
- Bit Test and Branch Instruction
- Indexed Addressing for Tables
- Memory Usable as Registers/Flags
- 10 Addressing Modes
- Powerful Instruction Set
  - — All 6800 Arithmetic Instructions
  - — All 6800 Logical Instructions
  - — All 6800 Shift Instructions
  - — Single Instruction Memory Examine/Change
  - — Full Set of Conditional Branches

Block Diagram



Pin Configuration



General Description

The S6805 is an 8-bit single chip microcomputer. It is the first member of the growing microcomputer family that contains a CPU, on-chip clock, ROM, RAM, I/O and timer. A basic feature of the 6805 is an instruction set very similar to the S6800 family of microprocessors. Although the 6805 is not strictly source nor object code compatible, an experienced 6800 user can easily write 6805 code. Also a 6805 user will have no trouble moving up to the 6801 or 6809 for more complex tasks.

Absolute Maximum Ratings

Supply Voltage, V_{CC} ..... −0.3V to +7.0V
Input Voltage, V_{IN} ..... −0.3V to +7.0V
Operating Temperature Range, T_A ..... 0° to +70°C
Storage Temperature Range, T_{stg} ..... −55°C to +150°C
Thermal Resistance, θ_{JA}
- Plastic ..... 85°C/W
- Ceramic ..... 50°C/W
- Cerdip ..... 51°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range V_{SS} (V_{IN} or V_{OUT}) + V_{CC}

Electrical Characteristics: V_{CC} = + 5.25 Vdc ± 0.5Vdc, V_{SS} = GND, T_A = 0°—70°C unless otherwise noted

Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	$\overline{RESET}$	4.0	—	V_{CC}	Vdc
V_{IH}		$\overline{INT}$	4.0		V_{CC}	Vdc
V_{IH}		All Other	V_{SS} + 2.0	—	V_{CC}	Vdc
V_{IH}	Input High	Timer Mode	V_{SS} + 2.0	—	V_{CC}	Vdc
V_{IH}	Voltage Timer	Self-Check Mode	—	9.0	15.0	Vdc
V_{IL}	Input Low Voltage	$\overline{RESET}$	V_{SS} − 0.3	—	0.8	Vdc
V_{IL}		$\overline{INT}$	V_{SS} − 0.3		1.5	Vdc
V_{IL}		All Other	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc
V_H	$\overline{INT}$ Hysteresis		—	100	—	mV_{CC}
P_D	Power Dissipation		—	350	—	mW
C_{IN}	Input Capacitance	EXTL	—	25	—	pF
C_{IN}		All Other	—	10	—	pF
LVR	Low Voltage Recover		—	—	4.75	Vdc
LVI	Low Voltage Inhibit		—	3.5	—	

Switching Characteristics: V_{CC} = + 5.25 V ± 0.5 Vdc, V_{SS} = GND, T_A = 0° — + 70°C unless otherwise noted

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{CI}	Clock Frequency	0.4	—	4.0	MHz
t_{CYC}	Cycle Time	1.0	—	10	μs
t_{IWL}	$\overline{INT}$ Pulse Width	t_{CYC} + 250	—	—	ns
t_{RWL}	$\overline{RESET}$ Pulse Width	t_{CYC} + 250	—	—	ns
t_{RHL}	Delay Time Reset (External Cap. = 0.47μF)	20	50	—	ms

Port Electrical Characteristics: V_{CC} = + 5.25 Vdc ± 0.5 Vdc, V_{SS} = GND, T_A = 0° — + 70°C unless otherwise noted

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Condition
			Port A			
V_{OL}	Output Low Voltage	—	—	0.4	Vdc	I_{LOAD} = 1.6mAdc
V_{OH}	Output High Voltage	2.4	—	—	Vdc	I_{LOAD} = 100μAdc
V_{OH}	Output High Voltage	3.5	—	—	Vdc	I_{LOAD} = − 10μAdc
V_{IH}	Input High Voltage	V_{SS} + 2.0	—	V_{CC}	Vdc	I_{LOAD} = − 300μAdc (max)
V_{IL}	Input Low Voltage	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc	I_{LOAD} = 500μAdc (max)
			Port B			
V_{OL}	Output Low Voltage	—	—	0.4	Vdc	I_{LOAD} = 3.2mAdc
V_{OL}	Output Low Voltage	—	—	1.0	Vdc	I_{LOAD} = 10mAdc(sink)
V_{OH}	Output High Voltage	2.4	—	—	Vdc	I_{LOAD} = − 200μAdc
I_{OH}	Darlington Current Drive (Source)	− 1.0	—	− 10	mAdc	V_O = 1.5Vdc
V_{IH}	Input High Voltage	V_{SS} + 2.0	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc	
			Port C			
V_{OL}	Output Low Voltage	—	—	0.4	Vdc	I_{LOAD} = 1.6mAdc
V_{OH}	Output High Voltage	2.4	—	—	Vdc	I_{LOAD} = − 100μAdc
V_{IH}	Input High Voltage	V_{SS} + 2.0	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc	
			Off-State Input Current			
I_{TSI}	Three-State Ports B & C	—	2	20	μAdc	
			Input Current			
I_{IN}	Timer at V_{IN} = (0.4 to 2.4 Vdc)	—	—	20	μAdc	

Figure 1. TTL Equiv. Test Load (Port B)

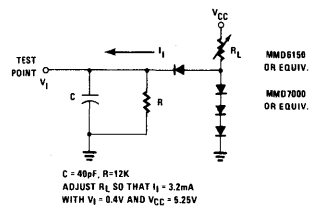
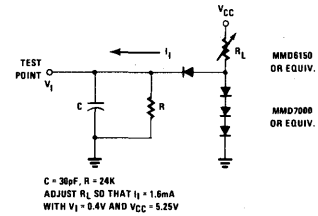


Figure 2. CMOS Equiv. Test Load (Port A)

Figure 3. TTL Equiv. Test Load (Ports A and C)



Pin Description

Pin	Symbol	Description
1 and 3	V_{CC} and V_{SS}	Power is supplied to the MCU using these two pins. V_{CC} is 5.25V ± .5V, and V_{SS} is the ground connection.
2	$\overline{INT}$	External Interrupt provides capability to apply an external interrupt to the MCU.
4 and 5	XTL and EXTL	Provide control input for the on-chip clock circuit. The use of crystal (at cut 4MHz maximum), a resistor or a wire jumper is sufficient to drive the internal oscillator with varying degrees of stability. (See Internal Oscillator Options for recommendations) An internal divide by 4 prescaler scales the frequency down to the appropriate f2 clock rate (1MHz maximum).
6	NUM	This pin is not for user application and should be connected to ground.
7	TIMER	Allows an external input to be used to decrement the internal timer circuitry. See TIMER for detailed information about the timer circuitry.
8-11 12-19 20-27	C0-C3 B0-B7 A0-A7	Input/Output lines (A0-A7, B0-B7, C0-C3). The 20 lines are arranged into two 8-bit ports (A and B) and one 4-bit port (C). All lines are programmed as either inputs or outputs under software control of the data direction registers. See Inputs/Outputs for additional information.
28	RESET	This pin allows resetting of the MCU. A low voltage detect feature responds to a dip in voltage by forcing a RESET condition to clear all Data Direction Registers, so that all I/O pins are set as inputs.

Memory

The MCU memory is configured as shown in Figure 4. During the processing of an interrupt, the contents of the MCU registers are pushed onto the stack in the order shown in Figure 5. Since the stack pointer decrements during pushes, the low order byte (PCL) of the program counter is stacked first, then the high order three bits (PCH) are stacked first, then the high order three bits (PCH) are stacked. This ensures that the program counter is loaded correctly as the stack pointer increments when it pulls data from the stack. A subroutine call will cause only the program counter (PCH, PCL) contents to be pushed onto the stack.

Figure 4. MCU Memory Configuration

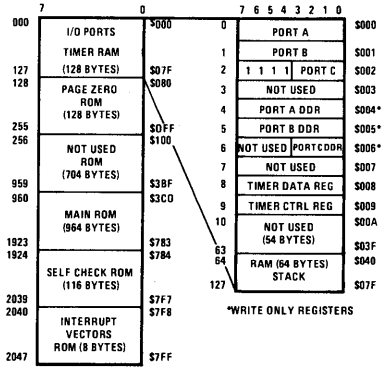


Figure 5. Interrupt Stacking Order

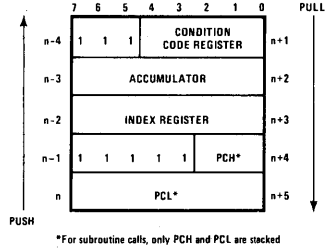
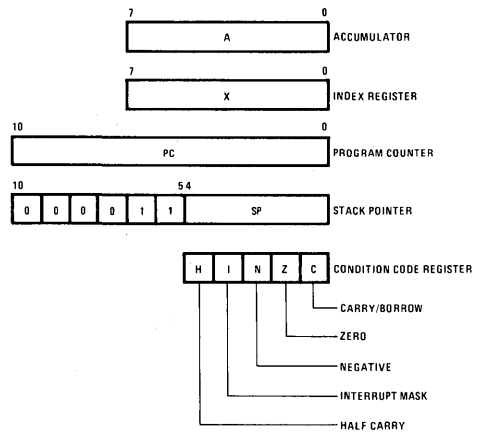


Figure 6. Programming Model



Registers

The S6805 MCU contains two 8-bit registers (A and X), one 11-bit register (PC), two 5-bit registers (SP and CC) that are visible to the programmer (see Figure 6).

Accumulator (A)

The A-register is an 8-bit general purpose accumulator used for arithmetic calculations and data manipulation.

Index Register (X)

This 8-bit register is used for the indexed addressing mode. It provides an 8-bit address that may be added to an offset to create an effective address. The index register can also be used for limited calculations and data manipulations when using the read/modify/write instructions. In code sequences not employing the index register it can be used as a temporary storage area.

Program Counter (PC)

This 11-bit register contains the address of the next instruction to be executed.

Stack Pointer (SP)

The stack pointer is an 11-bit register that contains the address of the next free location on the stack. Initially, the stack pointer is set to location $07F and is decremented as data is being pushed onto the stack and incremented as data is being pulled from the stack. The six most significant bits of the stack pointer are permanently set to 000011. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $07F. Subroutines and interrupts may be nested down to location $061 which allows the programmer to use up to 15 levels of subroutine calls. A 16th subroutine call would save the return address correctly, but the stack pointer would not remain pointing into the stack area and there would be no way to return from any of the subroutines.

Condition Code Register (CC)

The condition code register is a 5-bit register in which each bit is used to indicate or flag the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each individual condition code register bit is explained in the following paragraphs.

HALF CARRY (H)—Used during arithmetic operations (ADD and ADC) to indicate that a carry occurred between bits 3 and 4.

INTERRUPT (I)—This bit is set to mask the timer and external interrupt ($\overline{INT}$). If an interrupt occurs while this bit is set it is latched and will be processed as soon as the interrupt bit is reset.

NEGATIVE (N)—USED TO INDICATE that the result of the last arithmetic, logical or data manipulation was negative (bit 7 in result equal to a logical one).

ZERO (Z)—Used to indicate that the result of the last arithmetic, logical or data manipulation was zero.

CARRY/BORROW (C)—Used to indicate that a carry or borrow out of the arithmetic logic until (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts and rotates.

Timer

The MCU timer circuitry is shown in Figure 7. The 8-bit counter is loaded under program control and counts down toward zero as soon as the clock input is applied. When the timer reaches zero the timer interrupt request bit (bit 7) in the timer control register is set. The MCU responds to this interrupt by saving the present MCU state in the stack, fetching the timer interrupt vector from locations $7F8 and $7F9 and executing the interrupt routine. The timer interrupt can be masked by setting the timer interrupt mask bit (bit 6) in the timer control register. The interupt bit (bit 1) in the condition code register will also prevent a timer interrupt from being processed.

The clock input to the timer can be from an external source applied to the TIMER input pin or it can be the internal ϕ2 signal. Note that when ϕ2 signal is used as the source it can be gated by an input applied to the TIMER input pin allowing the user to easily perform pulse-width measurements. The source of the clock input is one of the options that has to be specified before manufacture of the MCU. A prescaler option can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before being applied to the counter. This prescaling option must also be specified before manufacturing begins. The timer continues to count past zero and its present count can be monitored at any time by monitoring the timer data register. This allows a program to determine the length of time since a timer interrupt has occurred and not disturb the counting process.

At power up or reset the prescaler and counter are initialized with all logical ones; the timer interrupt request bit (bit 7) is cleared and the timer request mask bit (bit 6) is set.

Self Check Mode:

The MCU includes a non-user mode pin that replaces the normal operating mode with one in which the internal data and address buses are available at the I/O ports. The ports are configured as follows in the test mode (some multiplexing of the address and data lines is necessary):

- The internal ROM and RAM are disabled and Port A becomes the input data bus on the ϕ2 of the clock and can be used to supply instructions of data to the MCU.
- Port B is also multiplexed. When ϕ2 is high, Port B is the output data bus, and when ϕ2 is low Port B is the address lines. The output data bus can be used to monitor the internal ROM or RAM.
- Port C becomes the last three address lines and a read/write control line.

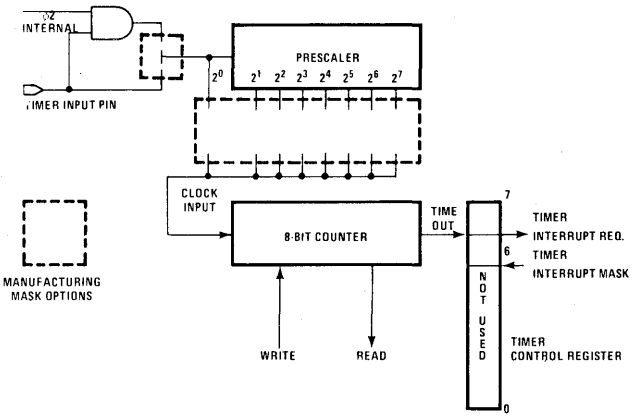
The MCU incorporates a self test program within a 116 byte non-user accessable test program and some control logic on-chip. These 116 bytes of ROM test every addressing mode and nearly every CPU instruction (95% of the total microprocessor capability) while only adding 1% to the total overall die size.

To perform the self test, the MCU output lines of Port A and B must be externally interconnected (Figure 7) and LED's are connected to Port C to provide both a pass/fail indication (3Hz square wave).

The flowchart for the self test program (Figure 8) runs four tests:

- **I/O TEST:** Tests for I/O lines that are stuck in high, low, shorted state, or are missing a connection. The I/O lines are all externally wired together so that the program can look for problems by testing for the correct operation of the lines as inputs and outputs and for shorts between two adjacent lines.
- **ROM ERROR:** (Checksum wrong). The checksum value of the user program must be masked into the self check ROM when the microcomputer is built. The self check program then tests the user ROM by computing the checksum value, which should be equal to the masked checksum if all the bits in the ROM are prop-

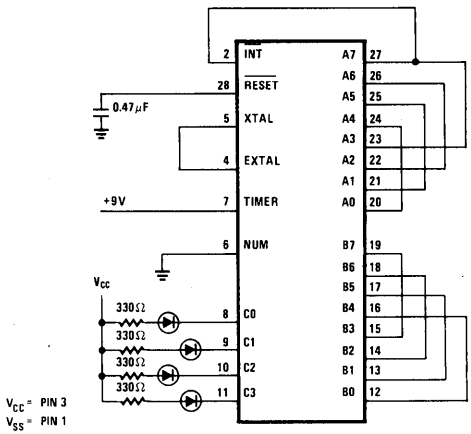
Figure 7. Timer Block Diagram



erly masked. Address and data lines that are stuck high, low or to each other are also detected by this test. An inoperable ROM will (in most cases) prevent the running of the self check program.

• **RAM Bits Non-Functional**: The RAM is tested by the use of a walking bit pattern that is written into memory and then verified. Every in RAM is set to one and then to zero by using 9 different patterns as shown in Figure 9.

Figure 8. Interconnected Ports for Self Check Mode. Port C Gives Go/No Go and Diagnostic Information.



Self Test Routines

Program performs four main tests in the major loops and provides an output signal to indicate that the part is functional.

Interrupt Logic Failure: Using an I/O line the interrupt pin is toggled to create an interrupt. The main program runs long enough to allow the timer to underflow and causes the timer interrupt to be enabled.

If all of these tests are successful the program, then loops back to the beginning and starts testing again.

The self check program initially tries to get the MCU out of the reset state to indicate that the processor is at least working. The non-functional parts are thus immediately eliminated, and if the part fails at this first stage the program provides a means of determining the faulty section.

To place the MCU in the self check mode the voltage on the timer input (Figure 7) is raised to 8 volts which causes several operations to take place:

Figure 9. Flowchart of Self Test Routine

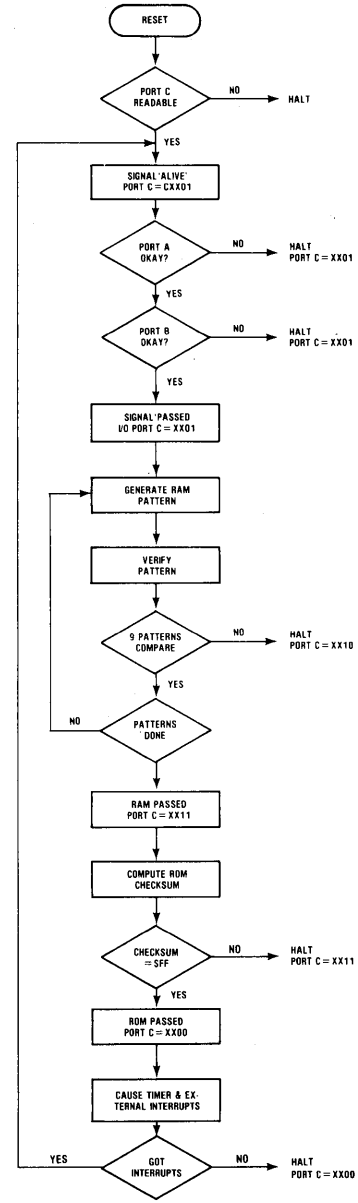
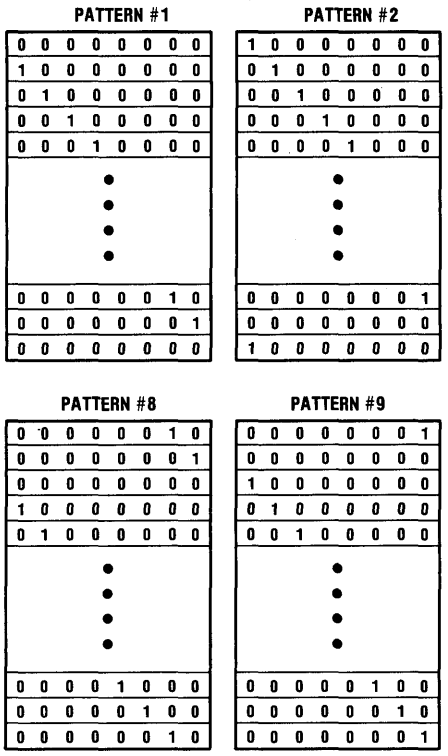


Figure 10. RAM Test Pattern



- The clocking source for the timer is shunted to the MCU internal clock to insure that the timer will run an underflow during the course of the program, no matter which clocking rate is masked.
- The address of the interrupt vectors (including the reset vector) are mapped into the self check ROM area. This allows the self check to test the interrupt structure.

The self check program is started by the reset signal instead of the normal program because the vectors (including the reset vector) have been overlaid. The self check program runs in an endless loop testing and retesting the processor as long as there are no errors. Signals on the I/O lines indicate that the test has passed, and if any test fails, the program stops by executing a branch to self instruction. The output lines then cease to toggle and two of the I/O lines will indicate the cause of failure.

RAM Test Pattern

"Walking bit" patterns test sequence sets and resets every bit in memory. (See Figure 10.)

Low Voltage Inhibit

As soon as the voltage at pin 3 (V_{CC}) falls to 4.5 volts, all I/O lines are put into a high impedance state. This prevents erroneous data from being given to an external device. When V_{CC} climbs back up to 4.6 volts a vectored reset is performed.

Table 1. Cause of Chip Failure as Shown in Bits 0 and 1 of I/O Port C

BIT 1	BIT 0	REASON FOR FAILURE
0	0	INTERRUPTS
0	1	I/O PORTS A OR B
1	0	RAM
1	1	ROM

Figure 11. Power Up and Reset Timing

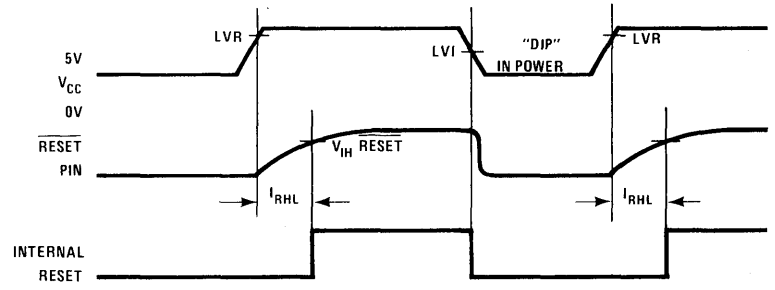
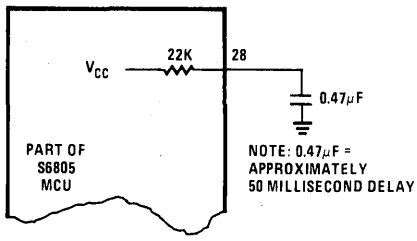


Figure 12. Power Up Reset Delay Circuit



Resets

The MCU can be reset three ways; by the external reset input ($\overline{\text{RESET}}$), by the internal low voltage detect circuit already mentioned, and during the power up time. (See Figure 11.)

Upon power up, a minimum of 20 milliseconds is needed before allowing the reset input to go high. This time allows the internal oscillator to stabilize. Connecting a capacitor to the $\overline{\text{RESET}}$ input as shown in Figure 12 will provide sufficient delay.

Internal Oscillator Options

The internal oscillator circuit has been designed to require a minimum of external components. The use of a crystal (AT cut, 4MHz max) or a resistor is sufficient to drive the internal oscillator with varying degrees of stability. A manufacturing mask option is available to provide better matching between the external components and the internal oscillator.

The different connection methods are shown in Figure 13. Crystal specifications are given in Figure 14. A resistor selection graph is given in Figure 15.

Figure 13. Internal Oscillator Options

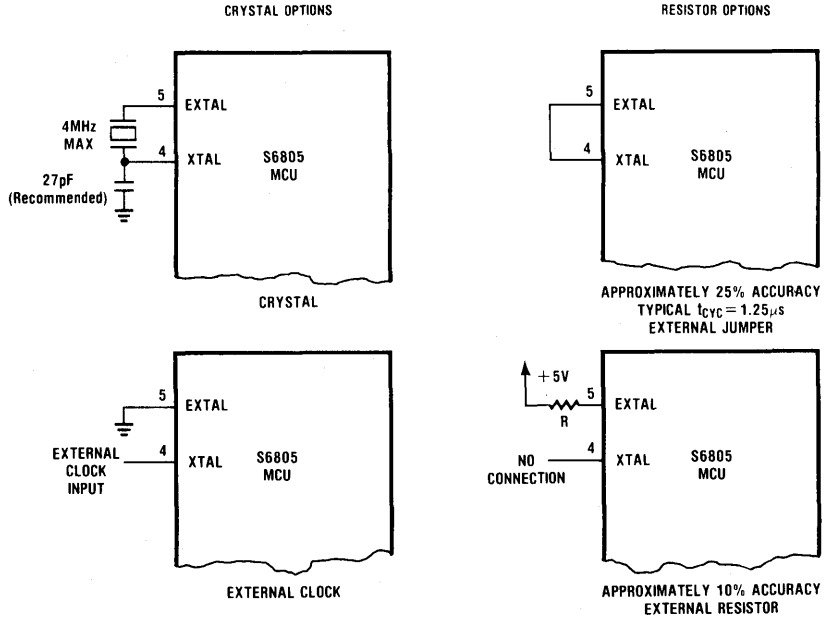
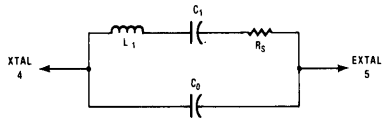
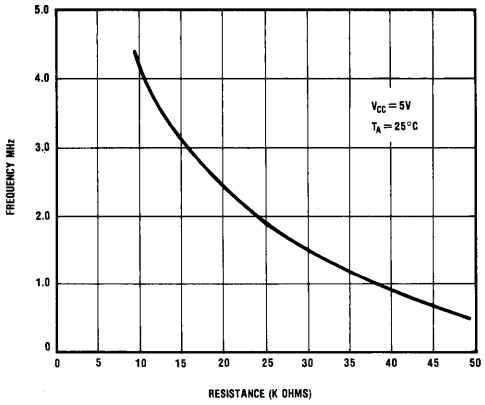


Figure 14. Crystal Parameters



AT–CUT PARALLEL RESONANCE CRYSTAL
C_0 = 7pF MAX
FREQ = 4.0MHz @ C_L = 24pF
R_S = 50 OHMS MAX

Figure 15. Typical Resistor Selection Graph



Interrupts

The MCU can be interrupted three different ways; through the external interrupt ($\overline{INT}$) input pin, the internal timer interrupt request, and a software interrupt instruction (SWI). When any interrupt occurs, processing is suspended, the present MCU state is pushed onto the stack, the interrupt bit (I) in the condition code register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. The interrupt service routines normally end with a return from interrupt (RTI) instruction which allows the MCU to resume processing of the program prior to the interrupt. Table 2 provides a listing of the interrupts, their priority, and the vector address that contain the starting address of the appropriate interrupt routine.

A sinusodial signal (1kHz maximum) can be used to generate an external interrupt ($\overline{INT}$) as shown in Figure 16.

A flowchart of the interrupt processing sequence is given in Figure 17.

Table 2. Interrupt Priorities

Interrupt	Priority	Vector Address
$\overline{RESET}$	1	$7FE AND $7FF
SWI	2	$7FC AND $7FD
$\overline{INT}$	3	$7FA AND $7FB
TIMER	4	$7F8 AND $7F9

Input/Output

There are 20 input/output pins. All pins are programmable as either inputs or outputs under software control of the data direction registers. When programmed as outputs, all I/O pins read latched output data regardless of the logic level at the output pin due to output loading (see Figure 18). When port B is programmed for outputs, it is capable of sinking 10 milliamperes on each pin (one volt maximum). All input/output lines are TTL compatible as both inputs and outputs. Port A lines are CMOS compatible as outputs while Port B and C lines are CMOS compatible as inputs. Figure 19 provides some examples of port connections.

Figure 16. Typical Sinusodial Interrupt Circuits

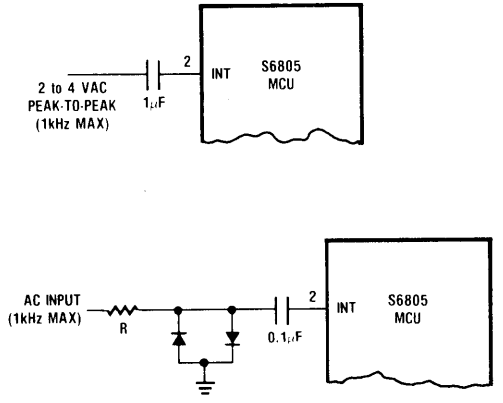


Figure 17. Interrupt Processing Flowchart

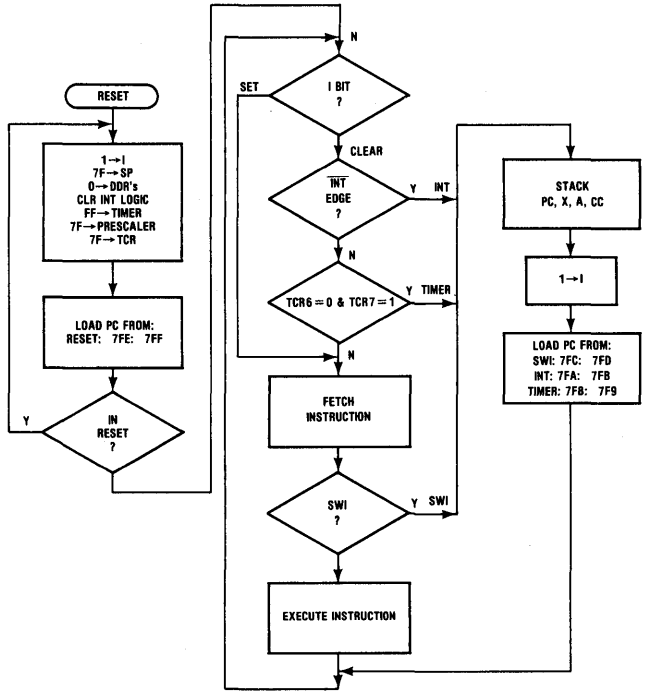
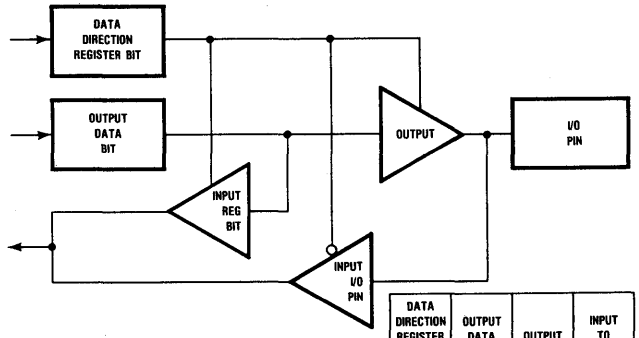
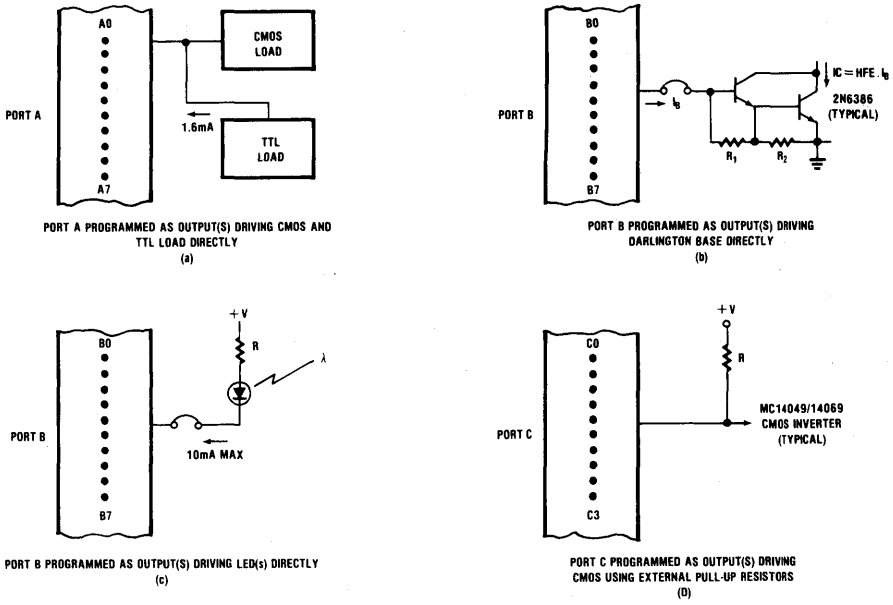


Figure 18. Typical Port I/O Circuitry



DATA DIRECTION REGISTER BIT	OUTPUT DATA BIT	OUTPUT STATE	INPUT TO MCU
1	0	0	0
1	1	1	1
0	X	3-STATE	PIN

Figure 19. Typical Port Connections



Bit Manipulation

The MCU has the ability to set or clear any single random access memory or input/output bit (except the data direction registers) with a single instruction (BSET, BCLR). Any bit in the page zero read only memory can be tested, using the BRSET and BRCLR instructions, and the program branches as a result of its state. This capability to work with any bit in RAM, ROM or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines. The example in Figure 20 illustrates the usefulness of the bit manipulation and test instructions. Assume that bit 0 of port A is connected to a zero crossing detector circuit and that bit 1 of port A is connected to the trigger of a TRIAC which powers the controlled hardware.

This program, which uses only seven ROM locations, provides turn-on of the TRIAC within 14 microseconds of the zero crossing. The timer could also be incorporated to provide turn-on at some later time which would permit pulse-width modulation of the controlled power.

Addressing Modes

The MCU has ten addressing modes available for use by the programmer. They are explained and illustrated briefly in the following paragraphs.

Figure 20. Bit Manipulation Example

```
        •
        •
        •
        •
        •
SELF 1  BRCLR 0, PORTA, SELF 1
        BSET 1, PORTA
        BCLR 1, PORTA
        •
        •
        •
        •
        •
```

Immediate—Refer to Figure 21. The immediate addressing mode accesses constants which do not change during program execution. Such instructions are two bytes long. The effective address (EA) is the PC and the operand is fetched from the byte following the opcode.

Direct—Refer to Figure 22 in direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in memory. All RAM space, I/O registers and 128 bytes of ROM are located in page zero to take advantage of this efficient memory addressing mode.

Extended—Refer to Figure 23. Extended addressing is used to reference any location in memory space. The EA is the contents of the two bytes following the opcode. Extended addressing instructions are three bytes long.

Relative—Refer to Figure 24. The relative addressing mode applies only to the branch instructions. In this mode the contents of the byte following the opcode is added to the program counter when the branch is taken. EA = (PC) + 2 + Rel. Rel is the contents of the location following the instruction opcode with bit 7 being the sign bit. If the branch is not tken Rel = 0, when a branch takes place, the program goes to somewhere within the range of + 129 bytes to − 127 of the present instruction. These instructions are two bytes long.

Indexed (No Offset)—Refer to Figure 25. This mode of addressing accesses the lowest 256 bytes of memory. These instructions are one byte long and their EA is the contents of the index register.

Indexed (8-Bit Offset)—Refer to Figure 26. The EA is calculated by adding the contents of the byte following the opcode to the contents of the index register. In this mode, 511 low memory locations are accessable. These instructions occupy two bytes.

Indexed (16-Bit Offset)—Refer to Figure 27. This addressing mode calculates the EA by adding the contents of the two bytes following the opcode to the index register. Thus, the entire memory space may be accessed. Instructions which use this addressing mode are three bytes long.

Bit Set/Clear—Refer to Figure 28. This mode of addressing applies to instructions which can set or clear any bit on page zero. The lower three bits in the opcode specify the bit to be set or cleared while the byte following the opcode specifies the address in page zero

Bit Test and Branch—Refer to Figure 29. This mode of addressing applies to instructions which can test any bit in the first 256 locations ($00-$FF) and branch to any location relative to the PC. The byte to be tested is addressed by the byte following the opcode. The individual bit within that byte to be tested is addressed by the lower three bits of the opcode. The third byte is the relative address to be added to the program counter if the branch condition is met. These instructions are three bytes long. The value of the bit tested is written to the carry bit in the condition code register.

Inherent—Refer to Figure 30. The inherent mode of addressing has no EA. All the information necessary to execute an instruction is contained in the opcode. Direct operations on the accumulator and the index register are included in this mode of addressing. In addition, control instructions such as SWI. RTI belong to this group. All inherent addressing instructions are one byte long.

Figure 21. Immediate Addressing Example

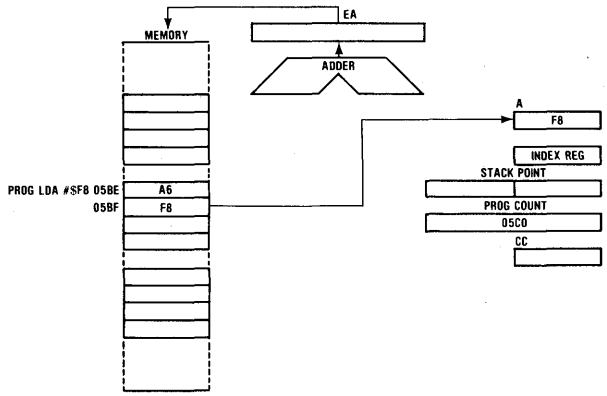


Figure 22. Direct Addressing Example

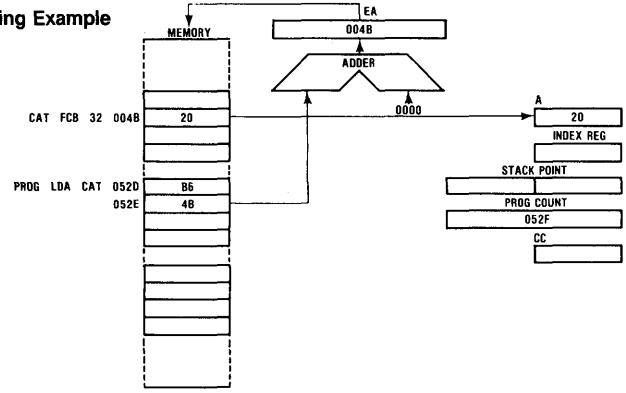


Figure 23. Extended Addressing Example

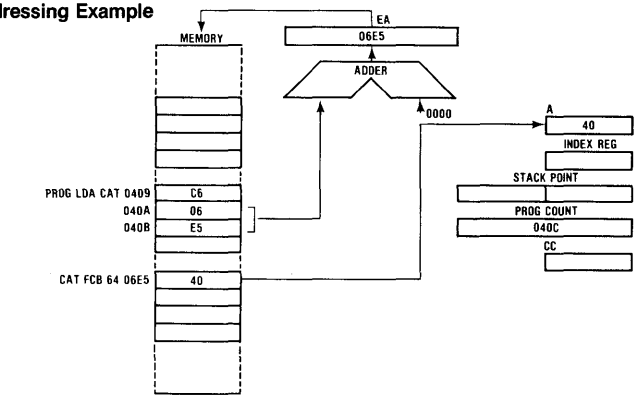


Figure 24. Relative Addressing Example

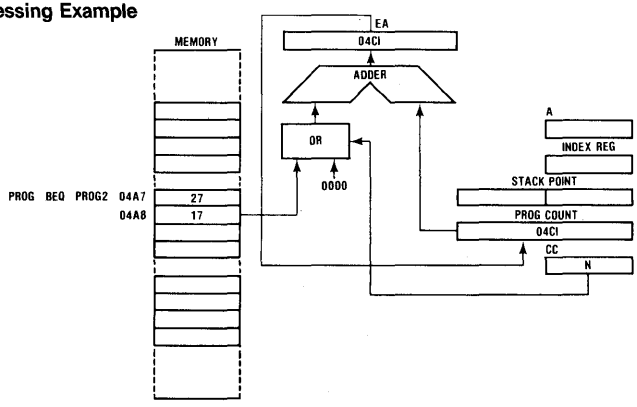


Figure 25. Indexed (No Offset) Addressing Example

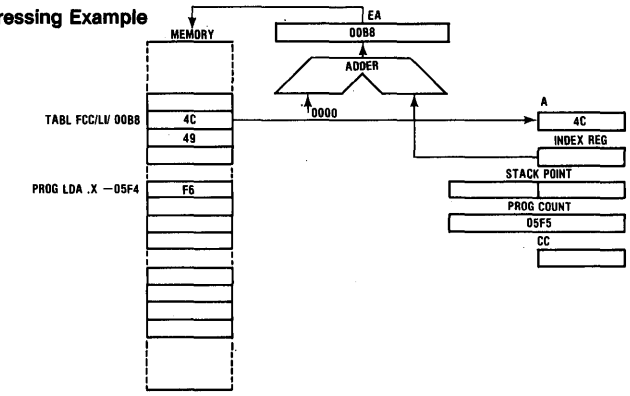


Figure 26. Indexed (8-Bit Offset) Addressing Example

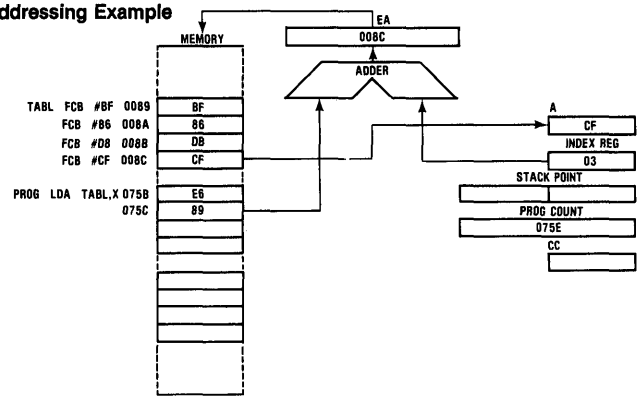


Figure 27. Indexed (16-Bit Offset) Addressing Example

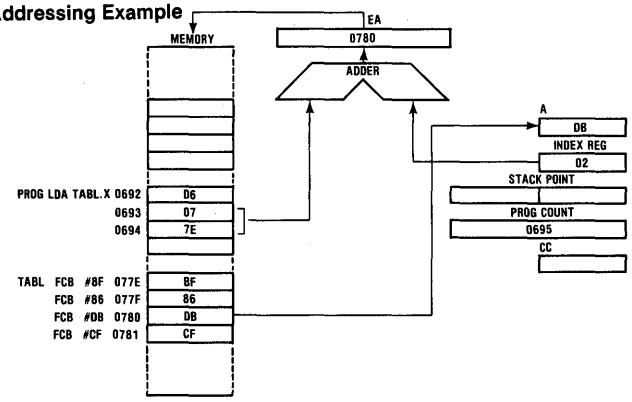


Figure 28. Bit Set/Clear Addressing Example

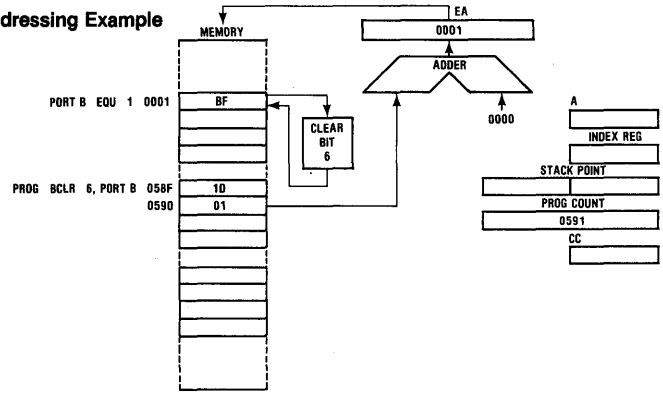


Figure 29. Bit Test and Branch Addressing Example

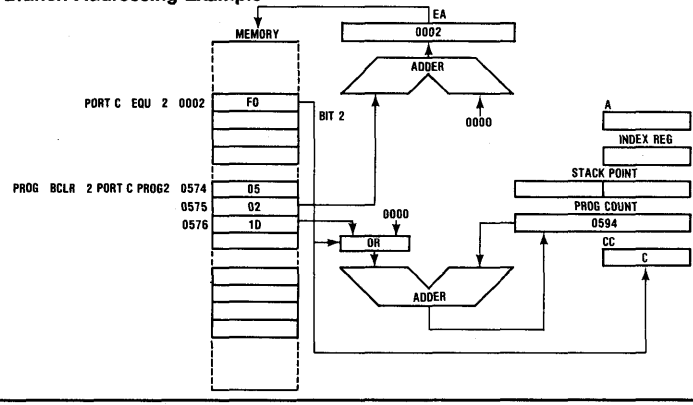
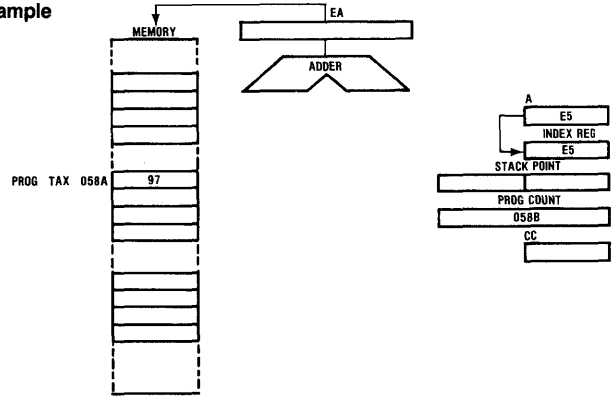


Figure 30. Inherent Addressing Example



S6800 FAMILY

Instruction Set

The MCU has a set of 59 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

Register/Memory Instructions—Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 3.

Read/Modify/Write Instructions—These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read/modify/write instructions since it does not perform the write. Refer to Table 4.

Branch Instructions—The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 5.

Bit Manipulation Instructions—These instructions are used on any bit in the first 256 bytes of the memory. One group either sets or clears. The other group performs the bit test and branch operations. Refer to Table 6.

Control Instructions—The control instructions control the MCU operations during program execution. Refer to Table 7.

Alphabetical Listing—The complete instruction set is given in alphabetical order in Table 8.

Opcode Map—Table 9 is an opcode map for the instructions used on the MCU.

Table 3. Register/Memory Instructions

		ADDRESSING MODES																	
		IMMEDIATE			DIRECT			EXTENDED			INDEXED (No Offset)			INDEXED (8-Bit Offset)			INDEXED 16-Bit Offset)		
Function	Mnemonic	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles
LOAD A FROM MEMORY	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6
LOAD X FROM MEMORY	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6
STORE A IN MEMORY	STA	—	—	—	B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7
STORE X IN MEMORY	STX	—	—	—	BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7
ADD MEMORY TO A	ADD	AE	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
ADD MEMORY AND CARRY TO A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6
SUBTRACT MEMORY	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6
SUBTRACT MEMORY FROM A WITH BORROW	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6
AND MEMORY TO A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6
OR MEMORY WITH A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6
EXCLUSIVE OR MEMORY WITH A	EOR	A8	2	2	B8	2	4	C8	3	5	F8	1	4	E8	2	5	D8	3	6
ARITHMETIC COMPARE A WITH MEMORY	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6
ARITHMETIC COMPARE X WITH MEMORY	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6
BIT TEST MEMORY WITH A (Logical Compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6
JUMP UNCONDITIONAL	JMP	—	—	—	BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5
JUMP TO SUBROUTINE	JSR	—	—	—	BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9

Table 4. Read/Modify/Write Instructions

		ADDRESSING MODES														
		INHERENT (A)			INHERENT (X)			DIRECT			INDEXED (No Offset)			INDEXED (8-Bit Offset)		
Function	Mnemonic	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	OP Cycles	# Bytes	# Cycles	
INCREMENT	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
DECREMENT	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
CLEAR	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
COMPLEMENT	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
NEGATE (2's COMPLEMENT)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
ROTATE LEFT THRU CARRY	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
ROTATE RIGHT THRU CARRY	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
LOGICAL SHIFT LEFT	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
LOGICAL SHIFT RIGHT	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
ARITHMETIC SHIFT RIGHT	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
TEST FOR NEGATIVE OR ZERO	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

Table 5. Branch Instructions

		RELATIVE ADDRESSING MODE		
Function	Mnemonic	OP Code	# Bytes	# Cycles
BRANCH ALWAYS	BRA	20	2	4
BRANCH NEVER	BRN	21	2	4
BRANCH IFF HIGHER	BHI	22	2	4
BRANCH IFF LOWER OR SAME	BLS	23	2	4
BRANCH IFF CARRY CLEAR	BCC	24	2	4
(BRANCH IFF HIGHER OR SAME)	(BHS)	24	2	4
BRANCH IFF CARRY SET	BCS	25	2	4
(BRANCH IFF LOWER)	(BLO)	25	2	4
BRANCH IFF NOT EQUAL	BNE	26	2	4
BRANCH IFF EQUAL	BEQ	27	2	4
BRANCH IFF HALF CARRY CLEAR	BHCC	28	2	4
BRANCH IFF HALF CARRY SET	BHCS	29	2	4
BRANCH IFF PLUS	BPL	2A	2	4
BRANCH IFF MINUS	BMI	2B	2	4
BRANCH IFF INTERRUPT MASK BIT IS CLEAR	BMC	2C	2	4
BRANCH IFF INTERRUPT MASK BIT IS SET	BMS	2D	2	4
BRANCH IFF INTERRUPT LINE IS LOW	BIL	2E	2	4
BRANCH IFF INTERRUPT LINE IS HIGH	BIH	2F	2	4
BRANCH TO SUBROUTINE	BSR	AD	2	8

AMI

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S6809/S68A09/S68B09**

8-BIT MICROPROCESSING UNIT

Features

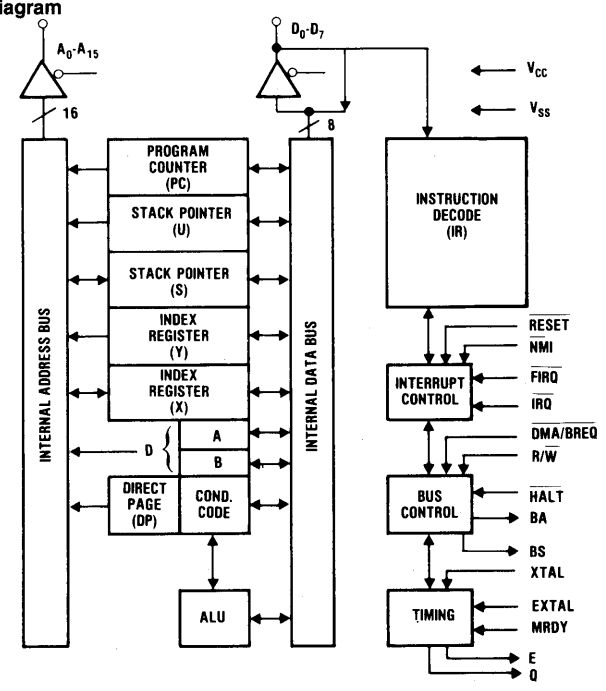
- ☐ Interfaces With All S6800 Peripherals
- ☐ Upward Compatible Instruction Set and Addressing Modes
- ☐ Upward Source Compatible Instruction Set and Addressing Modes
- ☐ Two 8-Bit Accumulators Can Be Concatenated Into One 16-Bit Accumulator
- ☐ On-Chip Crystal Oscillator (4 times XTAL)

General Description

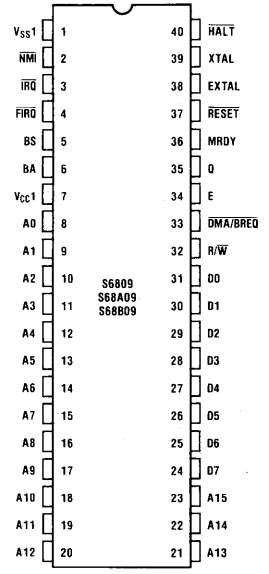
The S6809 is an advanced processor within the S6800 family offering greater throughput, improved byte efficiency, and increased adaptability to various software disciplines. These include position independence, reentrancy, recursion, block structuring, and high level language generation.

Because the S6809 generates position-independent code, software can be written in modular form for easy user expansion as system requirements increase. The S6809 is hardware compatible with all S6800 peripherals, and any assembly language code prepared for the S6800 can be passed through the S6809 assembler to produce code which will run on the S6809.

Block Diagram



Pin Configuration



AMI

A Subsidiary of Gould Inc.

S6809E/S68A09E/S68B09E

8-BIT MICROPROCESSING UNIT

Features

- ☐ Interfaces With All S6800 Peripherals
- ☐ Upward Compatible Instruction Set and Addressing Modes
- ☐ Upward Source Compatible Instruction Set and Addressing Modes
- ☐ Two 8-Bit Accumulators Can Be Concatenated Into One 16-Bit Accumulator
- ☐ External Clock Inputs, E and Q, Allow System Synchronization

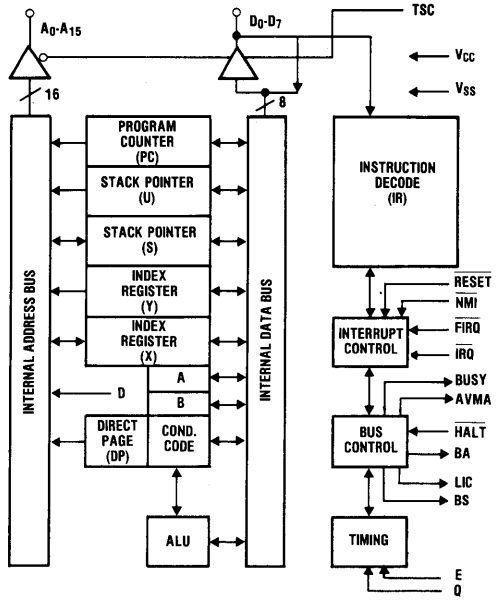
General Description

The S6809E is an advanced processor within the S6800 family offering greater throughput, improved byte efficiency, and increased adaptability to various software disciplines. These include position independence, reentrancy, recursion, block structuring, and high level language generation.

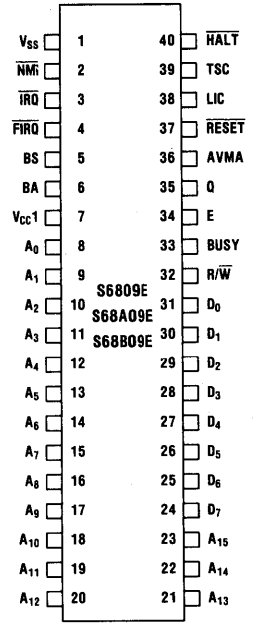
Because the S6809E supports **position-independent** code, software can be written in modular form for easy user expansion as system requirements increase. The S6809E is hardware compatible with all S6800 peripherals, and any assembly language code prepared for the S6800 can be passed through the S6809 assembler to produce code which will run on the S6809E.

S6600 FAMILY

Block Diagram



Pin Configuration



S6809E Hardware Features

- ☐ Fast Interrupt Request Input: Stacks Only Program Counter and Condition Code
- ☐ Interrupt Acknowledge Output Allows Vectoring by Devices
- ☐ Three Vectored Priority Interrupt Levels
- ☐ SYNC Acknowledge Output Allows for Synchronization to External Event
- ☐ NMI Blocked After RESET Until After First Load of Stack Pointer
- ☐ Early Address Valid Allows Use With Slow Memories
- ☐ Last Instruction Cycle Output (LIC) for Signalling Opcode Fetch
- ☐ Busy Output Eases Multiprocessor Design

Instruction Set

- ☐ Extended Range Branches
- ☐ Load Effective Address
- ☐ 16-Bit Arithmetic
- ☐ 8×8 Unsigned Multiply (AccumulatorA*B)
- ☐ SYNC Instruction—Provides Software Sync With an External Hardware Process
- ☐ Push and Pull on 2 Stacks
- ☐ Push/Pull Any or All Registers
- ☐ Index Registers May be Used as a Stack Pointer
- ☐ Transfer/Exchange all Registers

Addressing Modes

- ☐ All S6800 Modes Plus PC Relative Extended Indirect, Indexed Indirect, and PC Relative Indirect
- ☐ Direct Addressing Available Anywhere in Memory Map
- ☐ PC Relative Addressing: Byte Relative (± 32,768 Bytes From PC)
- ☐ Complete Indexed Addressing Including Automatic Increment and Decrement, Register Offsets, and Four Indexable Register (X, Y, U and S)
- ☐ Expanded Index Addressing
  - ☐ 0, 5, 8, 16-Bit Constant Offset
  - ☐ 8, 16-Bit Accumulator Offsets

The S6809E gives the user 8- and 16-bit word capability with several hardware enhancements in the design such as the Fast Interrupt Request ($\overline{FIRQ}$), Memory Ready (MRDY), and Quadrature (Q_{OUT}) and System Clock Outputs (E_{OUT}). With the Fast Interrupt Request ($\overline{FIRQ}$) the S6809E places **only** the Program Counter and Condition Code Register on the stack prior to accessing the $\overline{FIRQ}$ vector location. The Memory Ready ($\overline{MRDY}$) input allows extension of the data access time for use with slow memories. The System Clock (E_{OUT}) operates at the basic processor frequency and can be as the synchronization signal for the entire system. The Quadrature Output (Q_{OUT}) provides additional system timing by signifying that address and data are stable.

The External Clock mode of the S6809E is particularly useful when synchronizing the processor to an externally generated signal. The Three-State Control input ($\overline{TSC}$) places the Address and R/W line in the high impedance state for DMA or Memory Refresh. The last Instruction Cycle (LIC) is activated during the last cycle of any instruction. This signifies that the next instruction cycle is the opcode fetch. The Processor Busy signal (BUSY) facilitates multiprocessor applications by allowing the designer to insure that flags being modified by one processor are not accessed by another simultaneously.

The S6809E features a family of addressing capabilities which can use any of the four index registers and stack pointers as a pointer to the operand (or the operand address). This pointer can have a fixed or variable signed offset that can be automatically incremented or decremented. The eight-bit direct page register permits a user to determine which page of memory is accessed by the instructions employing "page zero" addressing. This quick access to any page is especially useful in multitasking applications.

The S6809E has three vectored priority-interrupt levels, each of which automatically disables the lower priority interrupt while leaving the higher priority interrupt enabled.

The S6809E gives the system designer greater flexibility (through modular relocatable code) to enable the user to reduce system software costs while at the same time increasing software reliability and efficiency.

E and Q Clock Inputs. The E and Q inputs are the clock signals required by the S6809E. The E signal is similar to the ϕ_2 signal of the S6800. Data is latched on the trailing edge of the E signal. The Q is a Quadrature clock, and is used to signal the validity of the addresses on the address bus. The Q input is TTL compatible, the E input however, directly drives the internal MOS circuitry. As a result, the E signal's levels must be higher than TTL levels, to minimize internal skew. The required signals are shown in Figures 1 and 2. Figure 11 shows the circuitry required to generate the proper signals. A 74LS73 is required, as the other 7473 series are level triggered rather than edge-triggered, and will not generate the proper waveforms.

BUSY. The BUSY output is used for arbitration of the MPU bus. The BUSY signal signifies that the S6809E will need the bus for at least the next cycle, as it is in the middle of a multiple-byte data access. The BUSY signal will be high for the first two cycles of the operand fetch of any Read-Modify-Write instruction, high during the first operand fetch of any double-byte instructions (LDD, STD) and high during the first byte access of any indirect access or vector fetch operation. BUSY is not active during pushes or pulls from the stack (PUL, PSH). Figure 12 shows the timing for the BUSY signal for a Read-Modify-Write operation (ASL @6300).

AVMA. The AVMA output is an advanced Valid Memory Address signal. This output goes HIGH one cycle before the MPU performs a memory access. The advanced nature of this signal allows bus arbitration logic an advanced warning of potential bus conflict.

LIC. The LIC output is the Last Instruction Cycle signal. This signal's HIGH to LOW transition signals that the current MPU cycle is an opcode fetch. The LIC signal will be held HIGH when the MPU is Halted at the end of an instruction (i.e., not in CWAI or RESET), when the MPU is in the SYNC state or while it is stacking during interrupts.

TSC. The TSC input is a Tri-State-Control for the S6809E's Address, data and R/$\overline{W}$ buffers. To force the MPU into the High-impedance state, the TSC line should be brought HIGH t_{PCST} before the end of the current cycle. The clocks for the MPU are then stopped in the first quarter (E = 0, Q = 0) of the next cycle. To regain the bus, the TSC line should be brought low, and the clocks re-started.

The TSC HIGH state is latched on the trailing edge of E, and therefore should be timed accordingly.

Figure 10. E/Q Relationship

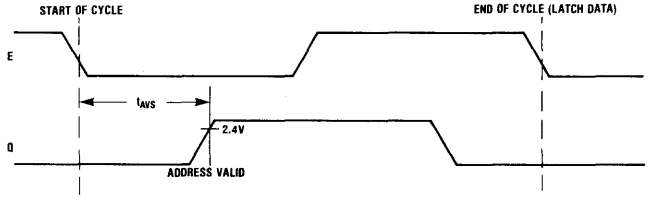
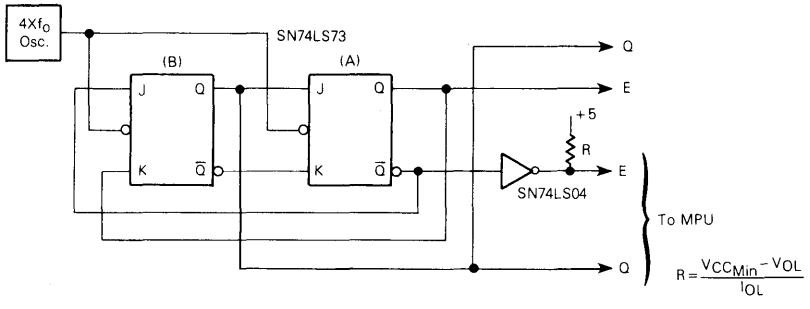


Figure 11. S6809E Clock Generator



AMI®

A Subsidiary
of Gould Inc.

Peripherals

AMI

A Subsidiary of Gould Inc.

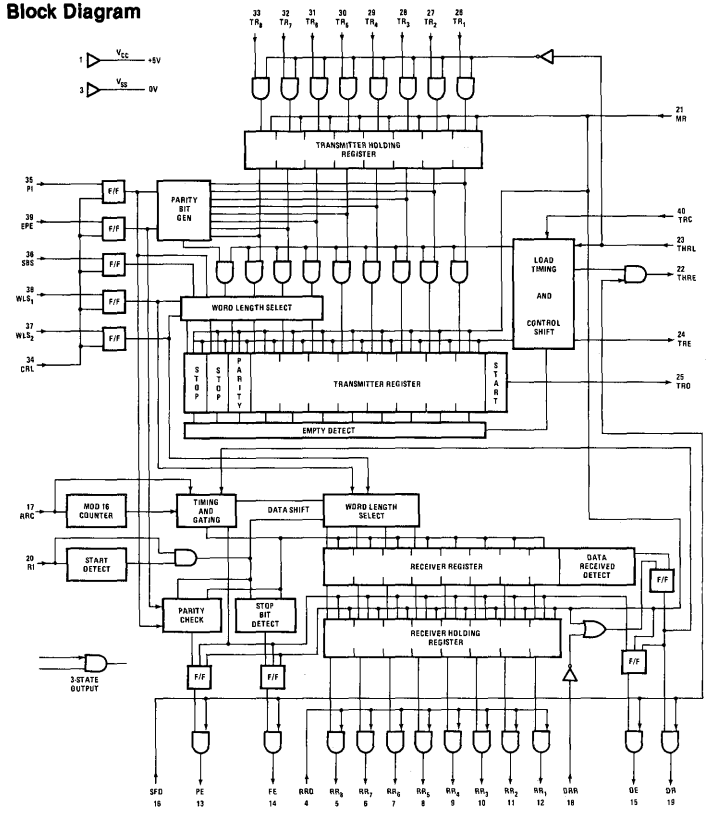
S1602

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

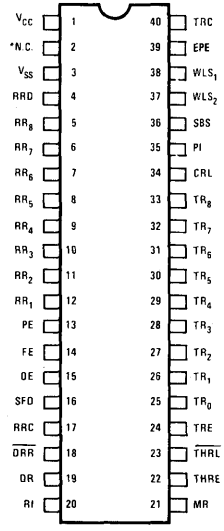
Features

- ☐ Full or Half Duplex Operation
  Transmits and Receives Serial Data Simultaneously or at Different Baud Rates
- ☐ Completely Programmable—Data Word Length, Number of Stop Bits, Parity
- ☐ Automatic Start Bit Generation
- ☐ Data and Clock Synchronization Performed Automatically
- ☐ Double Buffered—Eliminates Timing Difficulties
- ☐ Completely Static Circuitry
- ☐ Fully TTL Compatible
- ☐ Three-State Output Capability
- ☐ Single Power Supply: + 5 V
- ☐ Standard 40-Pin Dual-in-Line Package
- ☐ Plug In Compatible with Western Digital TR1602A, TR1863, Fujitsu 8868A

Block Diagram



Pin Configuration



General Description

The AMI S1602 is a programmable Universal Asynchronous Receiver/Transmitter (UART) fabricated with N-Channel silicon gate MOS technology. All control pins, input pins and output pins are TTL compatible, and a single + 5 volt power supply is used. The UART interfaces asynchronous serial data from terminals or other peripherals, to parallel data for a microprocessor, computer, or other terminal. Parallel data is converted by the transmitter section of the UART into a serial word consisting of the data as well as start, parity, and stop bit(s). Serial data is converted by the receiver section of the UART into parallel data. The receiver section verifies correct code transmission by parity checking and receipt of a valid stop bit. The UART can be programmed to accept word lengths of 5, 6, 7, or 8 bits. Even or odd parity can be set. Parity generation checking can be inhibited. The number of stop bits can be programmed for one, two, or one and one half when transmitting a 5-bit code.

Absolute Maximum Ratings*

V_{CC} Pin Potential to V_{SS} Pin ..... − 0.3V to + 7.0V
Input Voltage ..... − 0.3V to + 7.0V
Operating Temperature ..... 0°C to + 70°C
Storage Temperature ..... − 55°C to + 150°C

*Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheets. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance: $T_A = 25°C$; f = 1MHz; $V_{IN} = 0V$

Symbol	Parameter	Typ.	Max.	Unit
C_{IN}	Input Capacitance for all Inputs	10		pF

Guaranteed Operating Conditions (Referenced to V_{SS})

Symbol	Parameter	Operating Temperature	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	0°C to + 70°C	4.75	5.0	5.25	V
V_{SS}			0.0	0.0	0.0	V
V_{IH}	Logic Input High Voltage	0°C to + 70°C	2.2		V_{CC}	V
V_{IL}	Logic Input Low Voltage	0°C to + 70°C	− 0.3		+ 0.8	V

D.C. Characteristics (Guaranteed Operating Ranges Unless Otherwise Noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = 5.25V)			1.4	mA
I_{LZ}	Output Leakage Current for 3- State (V_{OUT} = 0V to V_{CC}, SFD = RRD = V_{IH}	− 20		+ 20	μA
V_{OL}	Output Low Voltage (I_{OL} = 1.8mA)			0.4	V
V_{OH}	Output High Voltage (I_{OL} = − 200μA)	2.4			V
I_{CC}	V_{CC} Supply Current		70		mA

A.C. Characteristics (Guaranteed Operating Ranges Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_C	Clock Frequency for RRC and TRC (Duty Cycle = 50%)	DC		800	kHz
t_{PWC}	CRL Pulse Width, High	200			ns
t_{PWT}	THRL Pulse Width, Low	180			ns
t_{PWR}	DRR Pulse Width, Low	180			ns
t_{PWM}	MR Pulse Width, High	150			ns
t_C	Coincidence Time (Figure 3 and Figure 8)	180			ns
t_{HOLD}	Hold Time (Figure 3 and Figure 8)	20			ns
t_{SET}	Setup Time (Figure 3 and Figure 8)	0			ns
t_{PD0}	Propagation Delay Time High to Low, Output (C_L = 130pF + 1TTL)			350	ns
t_{PD1}	Propagation Delay Time Low to High, Output (C_L = 130pF + 1TTL)			350	ns

Pin Description

Pin	Label	Function
1	V_{CC}	**Power Supply**—normally at +5V.
2	N.C.	**No Connection**. On the S1602 this is an unconnected pin. On the TR1602A this is a −12V supply. −12V is not needed on the S1602 and thus the N.C. pin allows the S1602 to be compatible with the TR1602A.
3	V_{SS}	This is normally at 0V or ground.
4	RRD	**Receive Register Disconnect**. A high logic level, V_{IH}, on this pin disconnects the Receiver Holding Register outputs from the data outputs RR_8–RR_1 on pin 5–12.
5–12	RR_8–RR_1	**Receiver Holding Register Data**. These are the parallel outputs from the Receiver Holding Register, if the RRD input is low (V_{IL}). Data is (LSB) right justified for character formats of less than eight bits, with RR_1 being the least significant bit. Unused MSBs are forced to a low logic output level, V_{OL}.
13	PE	**Parity Error**. This output pin goes to a high level if the received parity does not agree with that programmed by the Even Parity Enable input (pin 39). This output is updated as each character is transferred to the Receiver Holding Register. The Status Flag Disconnect input (pin 16) allows additional PE lines to be tied together by providing an output disconnect capability.
14	FE	**Framing Error**. This output pin goes high if the received character has no valid stop bit. Each time a character is transferred to the Receiver Holding Register, this output is updated. The Status Flag Disconnect input (pin 16) allows additional FE lines to be tied together by providing an output disconnect capability.
15	OE	**Overrun Error**. This output pin goes high if the Data Received Flag (pin 19) did not get reset before the next character was transferred to the Receive Holding Register. The Status Flag Disconnect input (pin 16) allows additional OE lines to be tied together providing an output disconnect capability.
16	SFD	**Status Flag Disconnect**. When this input is high, PE, FE, OE, DR and THRE outputs are forced to high impedance Three-State allowing bus sharing capability.
17	RRC	**Receive Register Clock**. This clock input is 16x the desired receiver shift rate.
18	$\overline{DRR}$	**Data Received Reset**. A low level input, V_{IL}, clears the Data Received (DR) line.
19	DR	**Data Received**. When a complete character has been received and transferred to the Receiver Holding Register, this output goes to the high level, V_{OH}.
20	RI	**Receiver Input**. Serial input data enters on this line. It is transferred to the Receiver Register as determined by the character length, parity and number of stop bits. When data is not being received, this input must remain high, V_{IH}.

Pin Description

Pin	Label	Function
21	MR	**Master Reset**. A high level pulse, V_{IH}, on this input clears the internal logic. The transmitter and Receive Registers, Receiver Holding Register, FE, OE, PE, DRR are reset. In addition, the serial output line is set to a high level, V_{OH}.
22	THRE	**Transmitter Holding Register Empty**. This output will go high when the Transmitter Holding Register completes transfer of its contents to the Transmitter Register. The high level indicates a new character may be loaded into the Transmitter Holding Register.
23	$\overline{\text{THRL}}$	**Transmitter Holding Register Load**. When a low level, V_{IL}, is applied to this input, a character is loaded into the Transmitter Holding Register. The character is transferred to the Transmitter Register on a low to high level, V_{IH}, transition as long as the Transmitter Register is not currently in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until the transmission is completed. The new character is then transferred simultaneously with the start of the serial transmission of the new character.
24	TRE	**Transmitter Register Empty**. Goes high when the Transmitter Register has completed the serial transmission of a full character including the required number of stop bits. A high will be maintained until the start of transmission of the next character.
25	TRO	**Transmitter Register Output**. Transmits the Transmitter Register contents (Start bit, Data bits, Parity bit and Stop bit(s) serially. Remains high, V_{OH}, when no data is being transmitted. Therefore, start of transmission is determined by transition of the Start bit from high to low level voltage, V_{OL}.
26–33	TR_1–TR_8	**Transmitter Register Data Inputs**. The THRL strobe loads the character on these lines into the Transmitter Holding Register. If WLS_1 and WLS_2 have selected a character of less than 8 bits, the character is right justified to the least significant bit, TR_1 with the excess bits not used. A high input level, V_{IH}, will cause a high output level, V_{OH}, to be transmitted.
34	CRL	**Control Register Load**. The control bits, (WLS_1, WLS_2, EPE, PI, SBS), are loaded into the Control Register when the input is high. This input may be either strobed or hard wired to the high level.
35	PI	**Parity Inhibit**. Parity generation and verification circuitry are inhibited when this input is high. The PE output will be held low as well. When in the inhibit condition the Stop bit(s) will follow the last data bit on transmission.
36	SBS	**Stop Bit(s) Select**. A high level will select two Stop bits, and a low level selects one Stop bit. If 5—bit words are selected, a high level will generate one and one-half Stop bits.
37, 38	WLS_2, WLS_1	**Word Length Select**. The state of these two (2) inputs determines the character length (exclusive of parity) as follows:

WLS_2	WLS_1	WORD LENGTH
LOW	LOW	5 bits
LOW	HIGH	6 bits
HIGH	LOW	7 bits
HIGH	HIGH	8 bits

39	EPE	**Even Parity Enable**. A high voltage level, V_{IH}, on this input will select even parity, while a low voltage level, V_{IL}, selects odd parity.
40	TRC	**Transmitter Register Clock**. The frequency of this clock input should be 16 times the desired baud rate.

Figure 1. Receiver Operator Timing

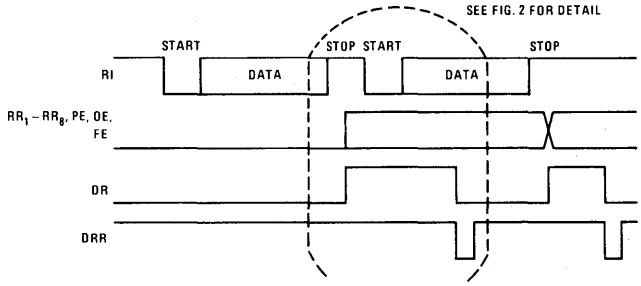


Figure 2. Timing for Status Flags, RR_1 thru RR_8 and DR

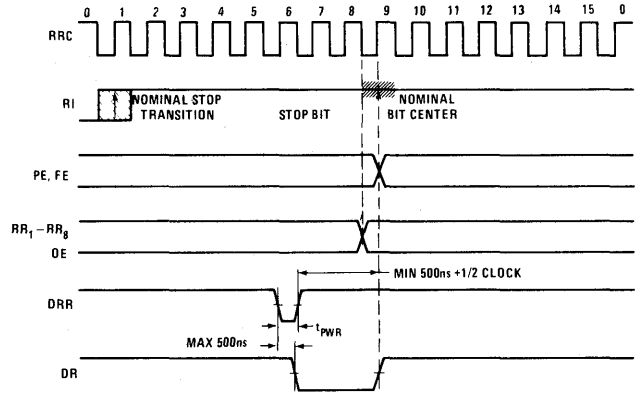


Figure 3. Transmitter Operator Timing

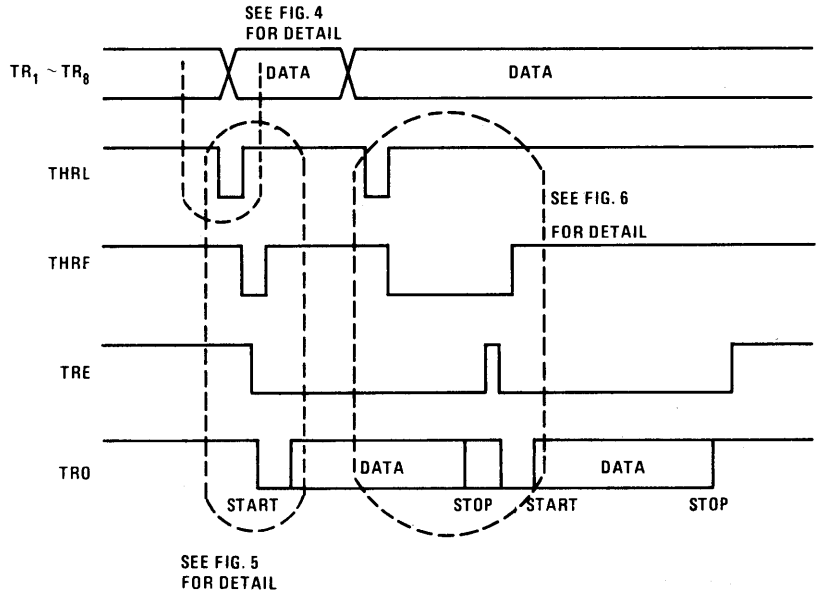


Figure 4. Data Input Load Cycle

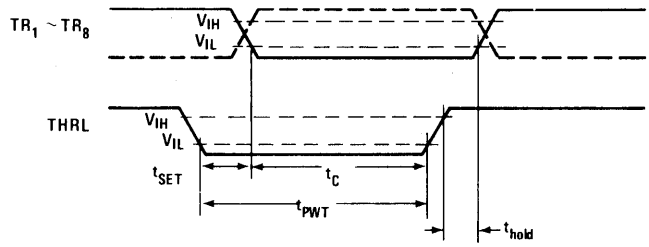
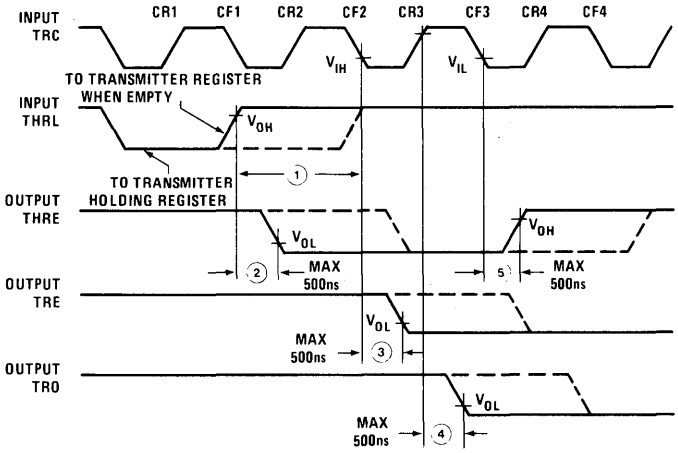


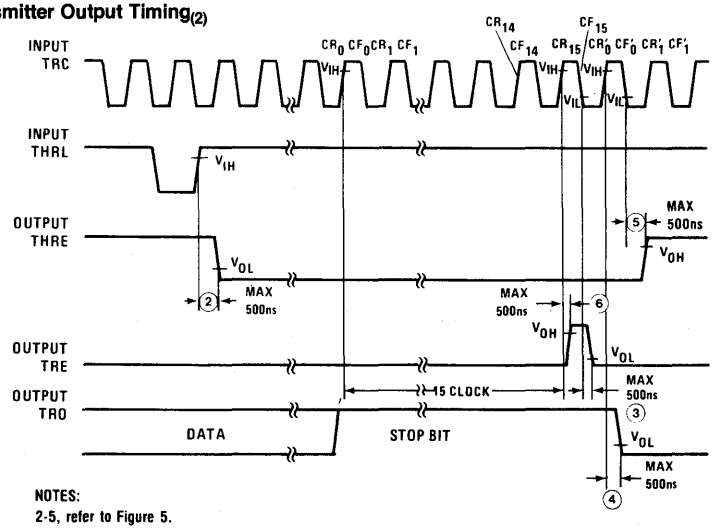
Figure 5. Transmitter Output Timing(1)



NOTES:

1. When the positive transition of THRL is 500ns or more before the falling edge of TRC (CF2 in the figure), TRE is enabled at CF2. But, when 500ns>(1)>0ns, TRE is invalid between CF2 and CF3.
2. THRE goes to low during 500ns Max. from the positive transition of THRL.
3. TRE goes to low during 500ns Max. from the first falling edge of TRC after THRE goes to low with TRE high.
4. TRO goes to low (START BIT) during 500ns Max. from the first rising edge of TRC after TRE goes to low.
5. THRE goes to high during 500ns Max. from the falling edge of TRC after START BIT is enabled.

Figure 6. Transmitter Output Timing(2)



NOTES:

2-5, refer to Figure 5.

6. TRANSMITTER REGISTER EMPTY goes to high during 500ns Max. from the 15th rising edge of TRC after STOP BIT is enables.

Figure 7. Input After Master Reset

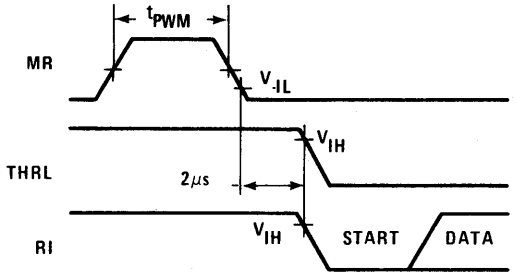


Figure 8. Control Register Load Cycle

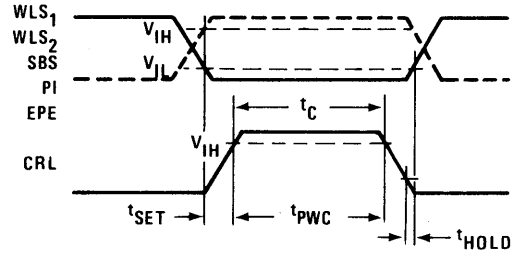


Figure 9. Status Flag Output

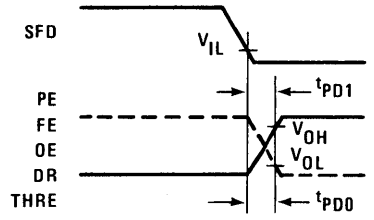
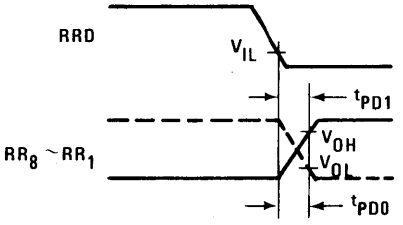


Figure 10. Data Output



S6800 FAMILY

AMI®

A Subsidiary of Gould Inc.

S2350

UNIVERSAL SYNCHRONOUS RECEIVER/TRANSMITTER

Features

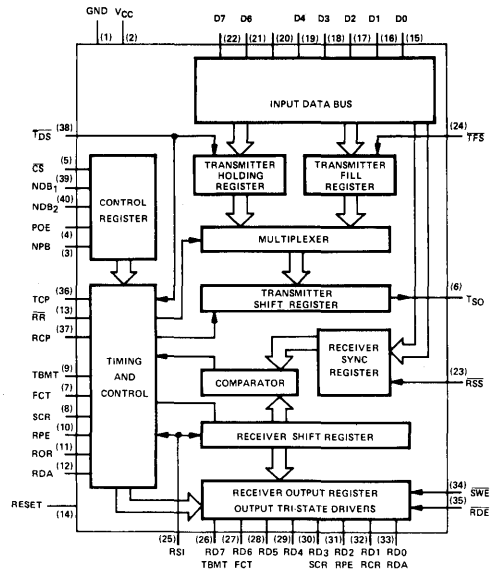
- ☐ 500kHz Data Rates
- ☐ Internal Sync Detection
- ☐ Fill Character Register
- ☐ Double Buffered Input/Output
- ☐ Bus Oriented Outputs
- ☐ 5-8 Bit Characters
- ☐ Odd/Even or No Parity
- ☐ Error Status Flags
- ☐ Single Power Supply (+ 5V)
- ☐ Input/Output TTL-Compatible

General Description

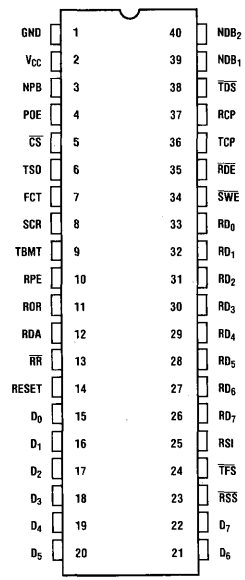
The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial-to-parallel and parallel-to-serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Block Diagram



Pin Configuration



Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8-bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8-bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

Typical Applications

- ☐ Computer Peripherals
- ☐ Communication Concentrators
- ☐ Integrated Modems
- ☐ High Speed Terminals
- ☐ Time Division Multiplexing
- ☐ Industrial Data Transmission

Absolute Maximum Ratings

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on Any Pin With Respect to GROUND	+7V
Negative Voltage on Any Pin With Respect to GROUND	−0.5V
Power Dissipation	0.75W

D.C. (Static) Electrical Characteristics* (V_{CC} = 5.0V ± 5%; T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		+0.8	V	
I_{IL}	Input Leakage Current			10	μA	V_{IN} = 0$_{TO}$ V_{CC} V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100μA
V_{OL}	Output Low Voltage			+0.4	V	I_{OL} = 1.6mA
C_{IN}	Input Capacitance			10	pF	V_{IN} = 0V; f = 1.0MHz
C_{OUT}	Output Capacitance			12	pF	V_{IN} = 0V; f = 1.0MHz
I_{CC}	V_{CC} Supply Current			100	mA	No Load; V_{CC} = 5.25V

* Electrical Characteristics included in this advanced product description are objective specifications and may be subject to change.

A.C. (Dynamic) Electrical Characteristics* (V_{CC} = 5.0V ± 5%; T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC		500	kHz	

A.C. (Dynamic) Electrical Charcteristics* (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
Input Pulse Width						
P_{TCP}	Transmit Clock	900			nsec	CL = 20pF
P_{RCP}	Receive Clock	900			nsec	1TTL Load
P_{RST}	Reset	500			nsec	
P_{TDS}	Transmit Data Strobe	200			nsec	
P_{TFS}	Transmit Fill Strobe	200			nsec	
P_{RSS}	Receive Sync Strobe	200			nsec	
P_{CS}	Control Strobe	200			nsec	
P_{RDE}	Receive Data Enable	400			nsec	Note 1
P_{SWE}	Status Word Enable	400			nsec	Note 1
P_{RR}	Receiver Restart	500			nsec	
Switching Characteristics						
T_{TSO}	Delay, TCP Clock to Serial Data Out			700	nsec	
T_{TBMT}	Delay, TCP Clock to TBMT Output			1.4	μsec	
T_{TBMT}	Delay, TDS to TBMT			700	nsec	
T_{STS}	Delay, SWE to Status Reset			700	nsec	
T_{RDO}	Delay, SWE, RDE to Data Output			400	nsec	1TTL Load
T_{HRDO}	Hold Time SWE, RDE to Off State			400	nsec	C_L = 130pF
T_{DTS}	Data Set Up Time TDS, TFS, RSS, CS	0			nsec	
T_{DTH}	Data Hold Time TDS	700			nsec	
T_{DTI}	Data Hold time TFS, RSS	200			nsec	
T_{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0			nsec	
T_{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200			nsec	
T_{RDA}	Delay RDE to RDA Output	700			nsec	

NOTE 1: Required to reset status and flags.

S6551/S6551A

ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

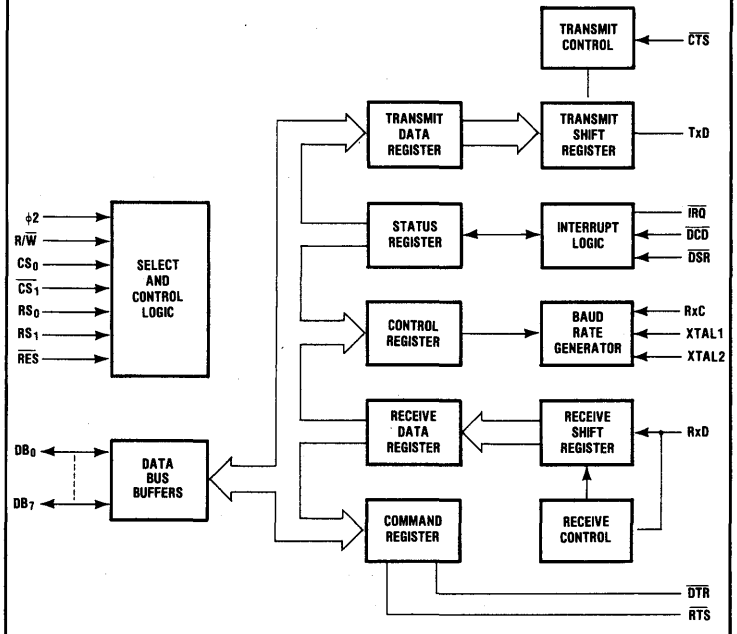
Features

- ☐ On-Chip Baud Rate Generator: 15 Programmable Baud Rates Derived from a Standard 1.8432MHz External Crystal (50 to 19,200 Baud)
- ☐ Programmable Interrupt and Status Register to Simplify Software Design
- ☐ Single + 5 Volt Power Supply
- ☐ Serial Echo Mode
- ☐ False Start Bit Detection
- ☐ 8-Bit Bi-Directional Data Bus for Direct Communication With the Microprocessor
- ☐ External 16X Clock Input for Non-Standard Baud Rates (Up to 125K Baud)
- ☐ Programmable: Word Lengths; Number of Stop Bits; and Parity Bit Generation and Detection
- ☐ Data Set and Modem Control Signals Provided
- ☐ Parity: (Odd, Even, None, Mark, Space)
- ☐ Full-Duplex or Half-Duplex Operation
- ☐ 5, 6, 7, 8 and 9-Bit Transmission

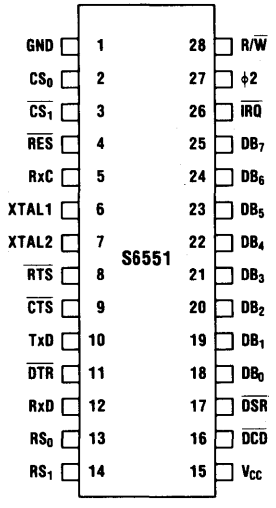
General Description

The S6551/S6551A is an Asynchronous Communication Adapter (ACIA) intended to provide interfacing for the microprocessors to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

Block Diagram



Pin Configuration



S6800 FAMILY

Absolute Maximum Ratings

Supply Voltage V_{CC} ..... −0.3V to +7.0V
Input/Output Voltage V_{IN} ..... −0.3V to +7.0V
Operating Temperature Range T_A ..... 0°C to +70°C
Storage Temperature Range T_{stg} ..... −55°C to +150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Operating Characteristics ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0°C$ to $+70°C$, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0	—	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
I_{IN}	Input Leakage Current: $V_{IN} = 0$ to 5V ($\phi 2$, R/W, RES, CS_0, CS_1, RS_0, RS_1, CTS, RxD, DCD, DSR)	—	±1.0	±2.5	μA
I_{TSI}	Input Leakage Current for High Impedance State (Three State)	—	±2.0	±10.0	μA
V_{OH}	Output High Voltage: $I_{LOAD} = -100\mu A$ (DB_0-DB_7, TxD, RxC, RTS, DTR)	2.4	—	—	V
V_{OL}	Output Low Voltage: $I_{LOAD} = 1.6mA$ (DB_0-DB_7, TxD, RxC, RTS, DTR, IRQ)	—	—	0.4	V
I_{OH}	Output High Current (Sourcing): $V_{OH} = 2.4V$ (DB_0-DB_7, TxD, RxC, RTS, DTR)	—	—	−100	μA
I_{OL}	Output Low Current (Sinking): $V_{OL} = 0.4V$ (DB_0-DB_7, TxD, RxC, RTS, DTR, IRQ)	—	—	1.6	mA
I_{OFF}	Output Leakage Current (Off State): $V_{OUT} = 5V$ (IRQ)	—	1.0	10.0	μA
C_{CLK}	Clock Capacitance ($\phi 2$)	—	—	20	pF
C_{IN}	Input Capacitance (Except XTAL1 and XTAL2)	—	—	10	pF
C_{OUT}	Output Capacitance	—	—	10	pF
P_D	Power Dissipation (See Graph) ($T_A = 0°C$)	—	170	300	mW

Write Cycle ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0°C$ to $+70°C$, unless otherwise noted)

		S6551		S6551A		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	$\phi 2$ Pulse Width	400	—	200	—	ns
t_{ACW}	Address Set-Up Time	120	—	70	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	150	—	60	—	ns
t_{HW}	Data Bus Hold Time	20	—	20	—	ns

(t_r and $t_f = 10$ to 30ns)

Figure 1. Power Dissipation vs. Temperature

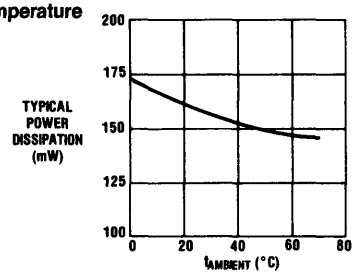
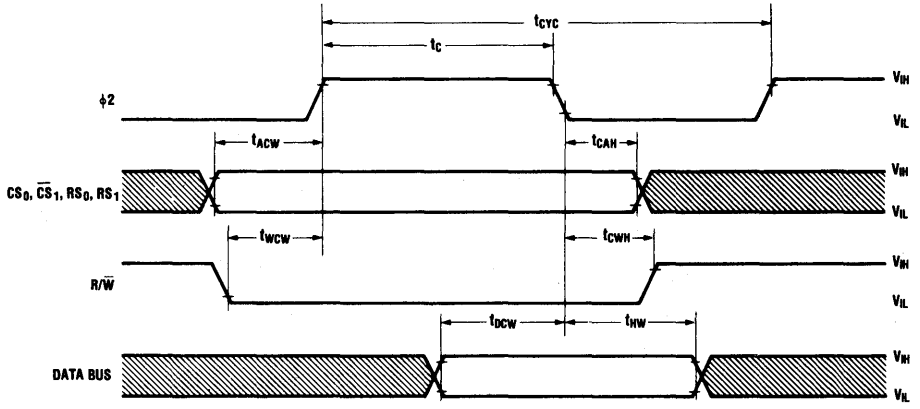


Figure 2. Write Timing Characteristics



Read Cycle (V_{CC} = 5.0V ± 5%, T_A = 0°C to + 70°C, unless otherwise noted)

Symbol	Parameter	S6551		S6551A		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	$\phi 2$ Pulse Width	400	—	200	—	ns
t_{ACR}	Address Set-Up Time	120	—	70	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	200	—	150	ns
t_{HR}	Read Hold Time	20	—	20	—	ns
t_{CDA}	Bus Active Time (Invalid Data)	40	—	40	—	ns

Figure 3. Clock Generation

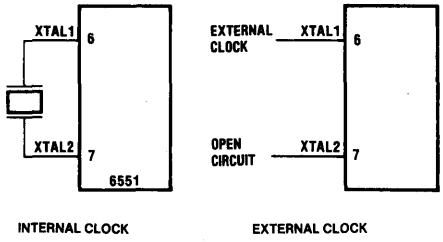
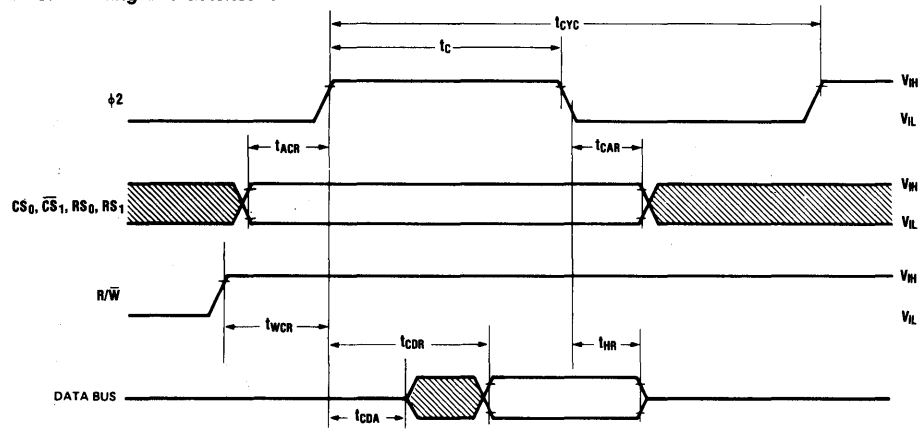


Figure 4. Read Timing Characteristics



Transmit/Receive Characteristics

Symbol	Parameter	S6551 Min.	S6551 Max.	S6551A Min.	S6551A Max.	Unit
t_{CCY}	Transmit/Receive Clock Rate	400*	—	400*	—	ns
t_{CH}	Transmit/Receive Clock High Time	175	—	175	—	ns
t_{CL}	Transmit/Receive Low Time	175	—	175	—	ns
t_{DD}	EXTAL1 to TxD Propagation Delay	—	500	—	500	ns
t_{DLY}	Propagation Delay ($\overline{RTS}$, DTR)	—	500	—	500	ns
t_{IRQ}	$\overline{IRQ}$ Propagation Delay (Clear)	—	500	—	550	ns

(t_r and t_f = 10 to 30ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$

Figure 5. Test Load for Data Bus (DB_0-DB_7), $\overline{TxD}$, $\overline{DTR}$, RTS Outputs

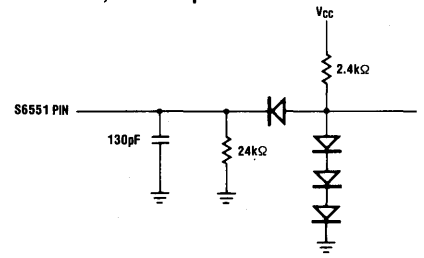


Figure 6a. Interrupt and Output Timing

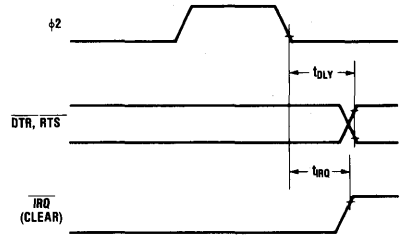


Figure 6b. Transmit Timing with External Clock

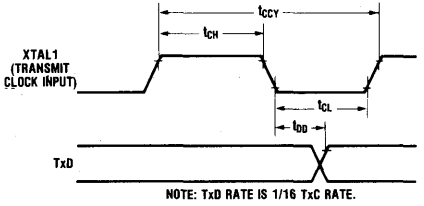
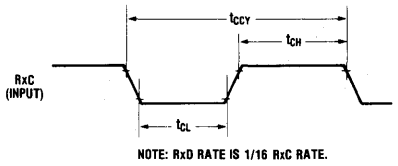


Figure 6c. Receive External Clock Timing



Pin Description

$\overline{RES}$ (Reset). During system initialization a low on the RES input will cause internal registers to be cleared.

ϕ2 Input Clock. The input clock is the system ϕ2 clock and is used to trigger all data transfers between the system microprocessor and the S6551.

R/$\overline{W}$ (Read/Write). The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the S6551. A low on the R/$\overline{W}$ pin allows a write to the S6551.

$\overline{IRQ}$ (Interrupt Request). The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0-DB_7 (Data Bus). The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the S6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0-$\overline{CS_1}$ (Chip Selects). The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The S6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_0, RS_1 (Register Selects). The two register select lines are normally connected to the processor address lines to allow the processor to select the various S6551 internal registers. The following table indicates the internal register select coding:

Table 1

RS_1	RS_0	WRITE	READ
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the S6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these diferences are described in the individual register definitions.

XTAL1, XTAL2 (Crystal Pins). These pins are normally directly connected to the external crystal (1.8432MHz M-Tron MP-2 recommended) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float.

TxD (Transmit Data). The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data). The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock). The RxC is a bi-directional pin which serves as either the receiver 16xclock input or the receiver 16xclock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{\text{RTS}}$ (Request to Send). The $\overline{\text{RTS}}$ output pin is used to control the modem from the processor. The state of the $\overline{\text{RTS}}$ pin is determined by the contents of the Command Register.

CTS (Clear to Send). The $\overline{\text{CTS}}$ input pin is used to control the transmitter operation. The enable state is with $\overline{\text{CTS}}$ low. The transmitter is automatically disabled if $\overline{\text{CTS}}$ is high.

$\overline{\text{DTR}}$ (Data Terminal Ready). This output pin is used to indicate the status of the S6551 to the modem. A low on $\overline{\text{DTR}}$ indicates the S6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{\text{DSR}}$ (Data Set Ready). The $\overline{\text{DSR}}$ input pin is used to indicate to the S6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{\text{DSR}}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{\text{DSR}}$ occurs, $\overline{\text{IRQ}}$ will be set, and Status Register Bit 6 will reflect the new level. The state of DSR does not affect either Transmitter or Receiver operation.

$\overline{\text{DCD}}$ (Data Carrier Detect). The $\overline{\text{DCD}}$ input pin is used to indicate to the S6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{\text{DCD}}$, like $\overline{\text{DSR}}$, is a high-impedance input and must not be a no-connect.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{\text{DCD}}$ occurs, $\overline{\text{IRQ}}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{\text{DCD}}$ does not affect Transmitter operation, but must be low for the Receiver to operate.

Figure 7. Transmitter/Receiver Clock Circuits

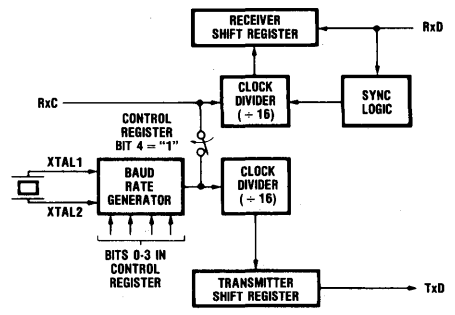


Figure 8. Control Register Format

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 STOP BIT
1 = 2 STOP BITS
1 STOP BIT IF WORD LENGTH = 5 BITS AND NO PARITY
1½ STOP BITS IF WORD LENGTH = 5 BITS AND NO PARITY

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = EXTERNAL RECEIVER CLOCK
1 = BAUD RATE GENERATOR

BAUD RATE GENERATOR

0	0	0	0	16x EXTERNAL CLOCK	
0	0	0	1	50	BAUD
0	0	1	0	75	
0	0	1	1	109.92	
0	1	0	0	134.58	
0	1	0	1	150	
0	1	1	0	300	
0	1	1	1	600	
1	0	0	0	1200	
1	0	0	1	1800	
1	0	1	0	2400	
1	0	1	1	3600	
1	1	0	0	4800	
1	1	0	1	7200	
1	1	1	0	9600	
1	1	1	1	19,200	

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	0	0	0	0	0

*THIS ALLOWS FOR 9-BIT TRANSMISSION (8 DATA BITS PLUS PARITY).

Internal Organization

The Transmitter/Receiver sections of the S6551 are depicted by the block diagram in Figure 7.

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the S6551.

Control Register

The Control Register is used to select the desired mode for the S6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 8.

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 9.

Figure 9. Command Register Format

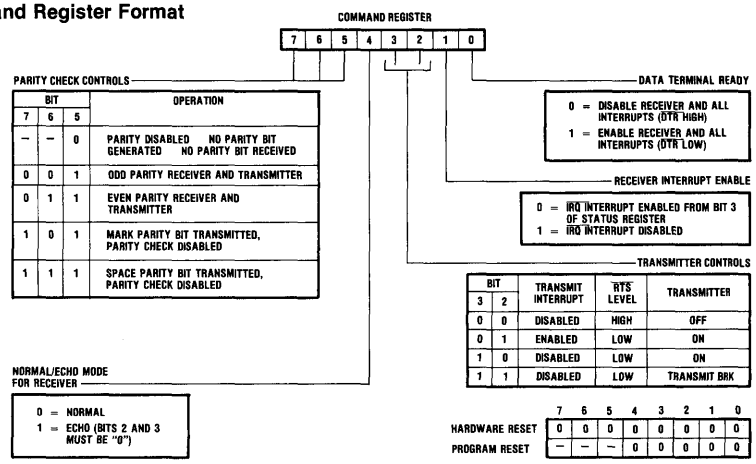
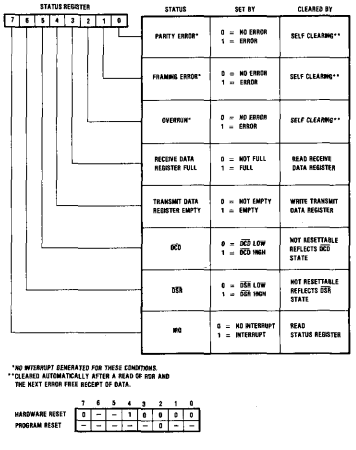


Figure 10. Status Register Format



Status Register

The Status Register is used to indicate to the processor the status of various S6551 functions and is outlined in Figure 10.

Transmit and Receive Data Registers

These registers are used as temporary data storage for the S6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- ☐ Bit 0 is the leading bit to be transmitted.
- ☐ Unused data bits are the high-order bits and are "don't care" for transmission.

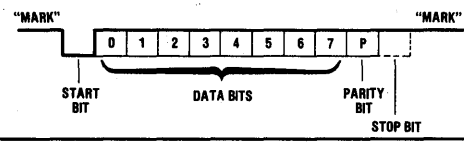
The Receive Data Register is characterized in a similar fashion:

- ☐ Bit 0 is the leading bit received.
- ☐ Unused data bits are the high-order bits and are "0" for the receiver.
- ☐ Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

S6800 FAMILY

Figure 11 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

Figure 11. Serial Data Stream Example



AMI

A Subsidiary of Gould Inc.

S6821/S68A21/S68B21

PERIPHERAL INTERFACE ADAPTER (PIA)

Features

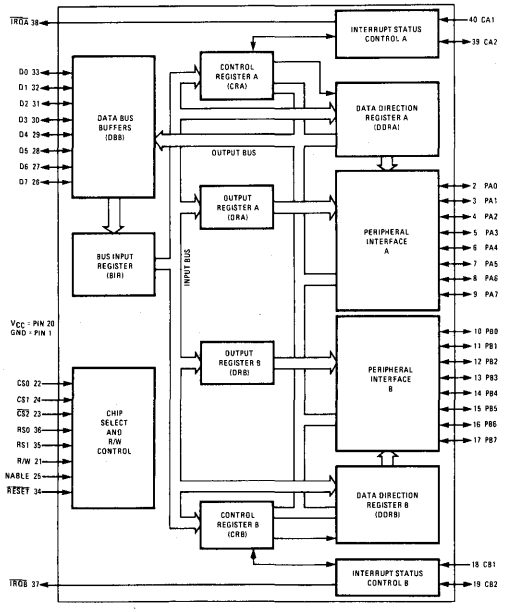
- ☐ 8-Bit Bidirectional Bus for Communication with the MPU
- ☐ Two Bidirectional 8-Bit Buses for Interface to Peripherals
- ☐ Two Programmable Control Registers
- ☐ Two Programmable Data Direction Registers
- ☐ Four Individually-Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs
- ☐ Handshake Control Logic for Input and Output Peripheral Operation
- ☐ High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- ☐ Program Controlled Interrupt and Interrupt Disable Capability
- ☐ CMOS Compatible Peripheral Lines
- ☐ Two TTL Drive Capability on all A and B Side Buffers
- ☐ TTL Compatible
- ☐ Static Operation

General Description

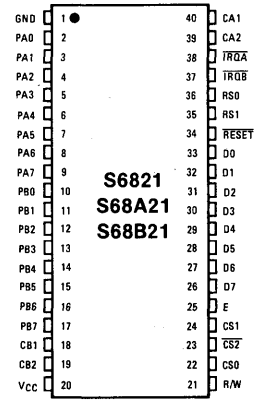
The S6821/S68A21/S68B21 are peripheral Interface Adapters that provide the universal means of interfacing peripheral equipment to the S6800/S68A00/S68B00 Microprocessing Units (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization Each of the

Block Diagram



Pin Configuration



S6800 FAMILY

General Description (Continued)

peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The PIA interfaces to the S6800/S68A00/S68B00 MPUs with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with S6800/S68A00/S68B00 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

Absolute Maximum Ratings:

Symbol	Rating	Value	Unit
V_{CC}	Supply Voltage	−0.3 to +7.0	Vdc
V_{IN}	Input Voltage	−0.3 to +7.0	Vdc
T_A	Operating Temperature Range	0° to +70°	°C
T_{stg}	Storage Temperature Range	−55° to +150°	°C
θ_{ja}	Thermal Resistance	82.5	°C/W

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics

V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Conditions
Bus Control Inputs (R/$\overline{W}$, Enable, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$)						
V_{IH}	Input High Voltage	V_{SS} + 2.0	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc	
I_{IN}	Input Leakage Current	—	1.0	2.5	μAdc	V_{IN} = 0 to 5.25 Vdc
C_{IN}	Capacitance	—	—	7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
Interrupt Outputs ($\overline{IRQA}$, $\overline{IRQB}$)						
V_{OL}	Output Low Voltage	—	—	V_{SS} + 0.4	Vdc	I_{LOAD} = 3.2 mAdc
I_{LOH}	Output Leakage Current (Off State)	—	1.0	10	μAdc	V_{OH} = 2.4 Vdc
C_{OUT}	Capacitance	—	—	5.0	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
Data Bus (D0-D7)						
V_{IH}	Input High Voltage	V_{SS} + 2.0	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} − 0.3	—	V_{SS} + 0.8	Vdc	
I_{TSI}	Three State (Off State) Input Current	—	2.0	10	μAdc	V_{IN} = 0.4 to 2.4 Vdc
V_{OH}	Output High Voltage	V_{SS} + 2.4	—	—	Vdc	I_{LOAD} = −205μAdc
V_{OL}	Output Low Voltage	—	—	V_{SS} + 0.4	Vdc	I_{LOAD} = 1.6mAdc
C_{IN}	Capacitance	—	—	12.5	pF	V_{IN} = 0, T_A = 25°C f = 1.0MHz

Electrical Characteristics (Continued)

Symbol	Characteristic		Min.	Typ.	Max.	Unit	Conditions
Peripheral Bus (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)							
I_{IN}	Input Leakage Current	R/$\overline{W}$, $\overline{Reset}$, RS0, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable		1.0	2.5	μAdc	V_{IN} = 0 to 5.25 Vdc
I_{TSI}	Three-State (Off State) Input Current	PB0-PB7, CB2		2.0	10	μAdc	V_{IN} = 0.4 to 2.4 Vdc
I_{IH}	Input High Current	PA0-PA7, CA2	−200	−400		μAdc	V_{IH} = 2.4 Vdc
I_{OH}	Darlington Drive Current	PB0-PB7, CB2	−1.0		−10	mAdc	V_O = 1.5 Vdc
I_{IL}	Input Low Current	PA0-PA7, CA2		−1.3	−2.4	mAdc	V_{IL} = 0.4Vdc
V_{OH}	Output High Voltage	PA0-P7, PB0-PB7, CA2, CB2 PA0-PA7, CA2	V_{SS} + 2.4 V_{CC} − 1.0			Vdc	I_{LOAD} = −200μAdc I_{LOAD} = −10μAdc
V_{OL}	Output Low Voltage				V_{SS} + 0.4	Vdc	I_{LOAD} = 3.2mAdc
C_{IN}	Capacitance				10	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
Power Requirements							
P_D	Power Dissipation				550	mW	

A.C. (Dynamic) Characteristics Loading = 30pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2 = 130pF and one TTL load for D0-D7, $\overline{IRQA}$, $\overline{IRQB}$ (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise specified)

Peripheral Timing Characteristics: V_{CC} − 5.0V ± 5%, V_{SS} = 0V, T_A = 0°C to +70°C unless otherwise specified

Symbol	Parameter	S6821 Min.	S6821 Max.	S68A21 Min.	S68A21 Max.	S68B21 Min.	S68B21 Max.	Units
t_{PDSU}	Peripheral Data Setup Time	200		135		100		ns
t_{PDH}	Peripheral Data Hold Time	0		0		0		ns
t_{CA2}	Delay Time, Enable Negative Transition to CA2 Negative Transition		1.0		0.670		0.5	μs
t_{RS1}	Delay Time, Enable Negative Transition to CA2 Positive Transition		1.0		0.670		0.50	μs
t_r, t_f	Rise and Fall Times for CA1 and CA2 Input Signals	1.0		1.0		1.0	μs	
t_{RS2}	Delay Time from CA1 Active Transition to CA2 Positive Transition		2.0		1.35		1.0	μs
t_{PDW}	Delay Time, Enable Negative Transition to Peripheral Data Valid		1.0		0.670		0.5	μs
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid PA0-PA7, CA2		2.0		1.35		1.0	μs

Peripheral Timing Characteristics (Continued)

Symbol	Parameter	S6821		S68A21		S68B21		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CB2}	Delay Time, Enable Positive Transition to CB2 Negative Transition		1.0		0.670		0.5	μs
t_{DC}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	2.0		20		20		ns
t_{RS1}	Delay Time, Enable Positive Transition to CB2 Positive Transition		1.0		0.670		0.5	μs
PW_{CT}	Peripheral Control Output Pulse Width, CA2/CB2	550		550		550		ns
t_r, t_f	Rise and Fall Times for CB1 and CB2 Input Signals		1.0		1.0		1.0	μs
t_{RS2}	Delay Time, CB1 Active Transition to CB2 Positive Transition		2.0		1.35		1.0	μs
t_{IR}	Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$		1.60		1.1		0.85	μs
t_{RS3}	Interrupt Response Time		1.0		1.0		1.0	μs
PW_I	Interrupt Input Pulse Width	500		500		500		ns
t_{RL}	Reset Low Time*	1.0		0.66		0.5		μs

*The Reset line must be high a minimum of 1.0μs before addressing the PIA.

Figure 1. Enable Signal Characteristics

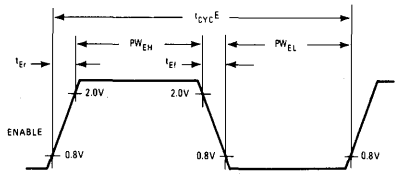


Figure 2. Bus Read Timing Characteristics (Read Information from PIA)

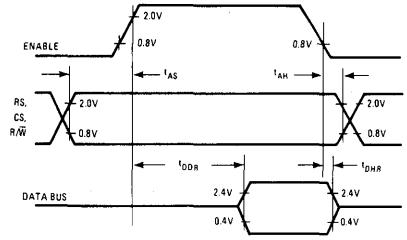


Figure 3. Bus Write Timing Characteristics (Write Information into PIA)

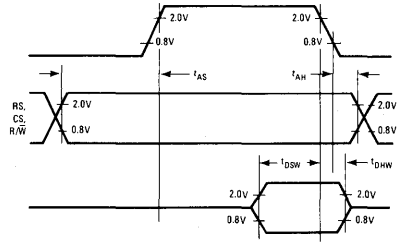
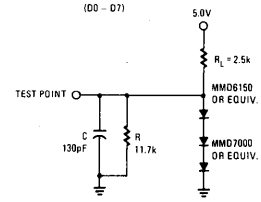


Figure 4. Bus Timing Test Loads



Bus Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted.)

Symbol	Parameter	S6821		S68A21		S68B21		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{cyc(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er}, t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DDR}	Data Delay Time, Read		320		220		180	ns
t_{DHR}	Data Hold Time, Read	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Figure 5. TTL Equiv. Test Load

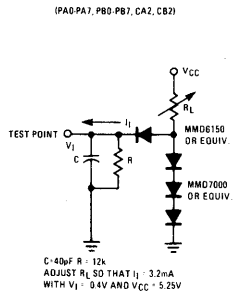


Figure 6. CMOS Equiv. Test Load

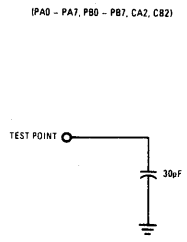


Figure 7. NMOS Equiv. Test Load

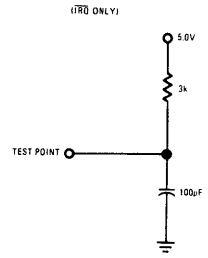


Figure 8. Peripheral Data Setup and Hold Times (Read Mode)

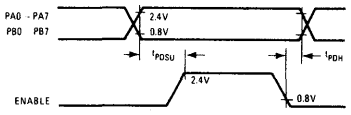
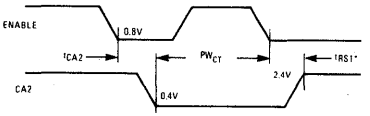


Figure 9. CA2 Delay Time (Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

Figure 10. CA2 Delay Time (Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

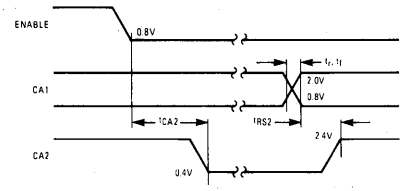


Figure 11. Peripheral CMOS Delay Times (Write Mode; CRA-5 = CRA-3 = CRA-4 = 0)

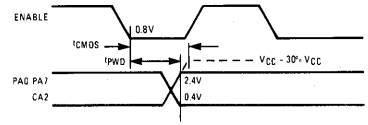
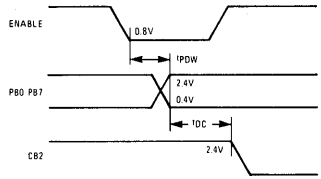


Figure 12. Peripheral Data and CB2 Delay Times (Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



CB2 Note:
CB2 goes low as a result of the positive transition of Enable.

Figure 13. CB2 Delay Time (Read Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)

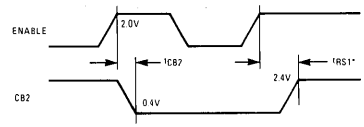
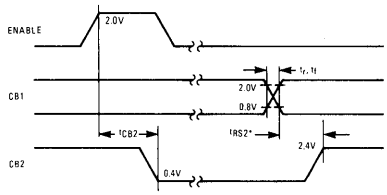
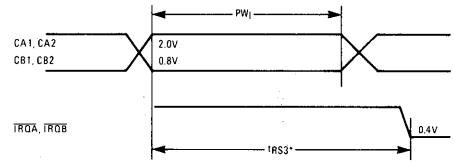


Figure 14. Delay Time (Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

Figure 15. Interrupt Pulse Width and $\overline{IRQ}$ Response



*Assumes Interrupt Enable Bits are set.

Figure 16. $\overline{IRQ}$ Release Time

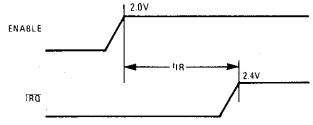
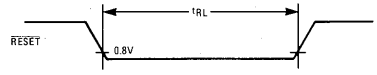


Figure 17. $\overline{Reset}$ Low Time



*The $\overline{Reset}$ line must be a V_{IH} for a minimum of 1.0μs before addressing the PIA.

AMI

A Subsidiary of Gould Inc.

S6840/S68A40/S68B40

PROGRAMMABLE TIMER

Features

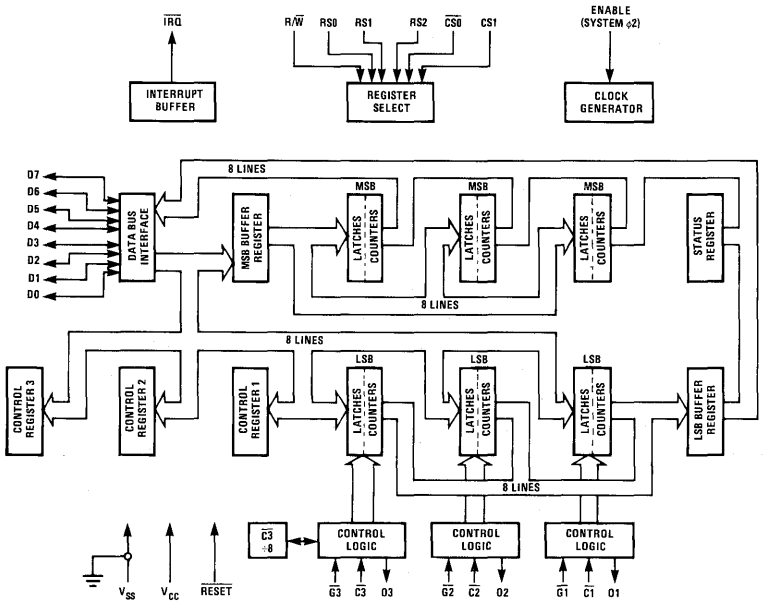
- ☐ Operates from a Single 5 Volt Supply
- ☐ Fully TTL Compatible
- ☐ Single System Clock Required (Enable)
- ☐ Selectable Prescaler on Time 3 Capable of 4MHz for the S6840, 6MHz for the S68A40 and 8MHz for the S68B40
- ☐ Programmable Interrupts ($\overline{IRQ}$) Output to MPU
- ☐ Readable Down Counter Indicates Counts to Go to Time-Out
- ☐ Selectable Gating for Frequency or Pulse-Width Comparison
- ☐ $\overline{RESET}$ Input
- ☐ Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized
- ☐ Three Maskable Outputs

General Description

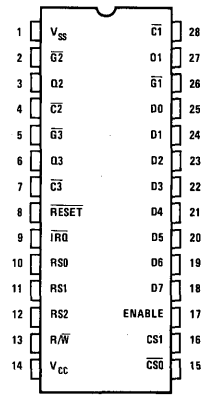
The S6840 is a programmable subsystem component of the S6800 family designed to provide variable system time intervals.

The S6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The S6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

Block Diagram



Pin Configuration



S6800 FAMILY

Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3 to +7.0V
Input Voltage V_{IN}	−0.3 to +7.0V
Operating Temperature Range T_A	0° to +70°C
Storage Temperature Range T_{stg}	−55° to +150°C
Thermal Resistance θ_{JA}	82.5°C/W

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics: (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage		V_{SS} + 2.0		V_{CC}		V
V_{IL}	Input Low Voltage		V_{SS} − 0.3		V_{SS} + 0.8	V	
I_{IN}	Input Leakage Current			1.0	2.5	μA	V_{IN} = 0 to 5.25 V
I_{TSI}	Three-State (Off State) Input Current	D_0-D_7		2.0	10	μA	V_{IN} = 0.4 to 2.4 V
V_{OH}	Output High Voltage	D_0-D_7 All Others	V_{SS} + 2.4 V_{SS} + 2.4			V V	I_{LOAD} = −205μA I_{LOAD} = −200μA
V_{OL}	Output Low Voltage	D_0-D_7 01-03, $\overline{IRQ}$			V_{SS} + 0.4 V_{SS} + 0.4	V V	I_{LOAD} = 1.6mA I_{LOAD} = 3.2mA
I_{LOH}	Output Leakage Current (Off State)	$\overline{IRQ}$		1.0	10	μA	V_{OH} = 2.4V
P_D	Power Dissipation				550	mW	
C_{IN}	Capacitance	D_0-D_7 All Others			12.5 7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
C_{OUT}		$\overline{IRQ}$ 01, 02, 03			5.0 10	pF	V_{IN} = 0, T_A = +25°C, f = 1.0MHz

Bus Timing Characteristics

Read (See Figure 1)

Symbol	Characteristic	S6840		S68A40		S68B40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYCE}	Enable Cycle Time	1.0	10	0.666	10	0.5	10	μs
PW_{EH}	Enable Pulse Width, High	0.45	4.5	0.280	4.5	0.22	4.5	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Times for Enable Input		25		25		25	ns

Bus Timing Characteristics (Continued)

Write (See Figure 2)

Symbol	Characteristic	S6840		S68A40		S68B40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYCE}	Enable Cycle Time	1.0	10	0.666	10	0.5	10	μs
PW_{EH}	Enable Pulse Width, High	0.45	4.5	0.280	4.5	0.22	4.5	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Data Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Times for Enable Input		25		25		25	ns

AC Operating Characteristics (See Figures 3 and 7)

Symbol	Characteristic	S6840		S68A40		S68B40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_r, t_f	Input rise and Fall Times (Figures 4 and 5) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$		1.0		0.666*		0.500*	μs
PW_L	Input Pulse Width (Figure 4) (Asynchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$	$t_{CYCE} + t_{su} + t_{hd}$		$t_{CYCE} + t_{su} + t_{hd}$		$t_{CYCE} + t_{su} + t_{hd}$		ns
PW_H	Input Pulse Width (Figure 5) (Asynchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$	$t_{CYCE} + t_{su} + t_{hd}$		$t_{CYCE} + t_{su} + t_{hd}$		$t_{CYCE} + t_{su} + t_{hd}$		ns
t_{su}	Input Setup Time (Figure 6) (Synchronous Mode) C, $\overline{G}$ and $\overline{Reset}$ $\overline{C3}$ (÷8 Prescaler Mode only)	200		120		75		ns
t_{hd}	Input Hold Time (Figure 6) (Synchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$ $\overline{C3}$ (÷8 Prescaler Mode only)	50		50		50		ns
PW_L, PW_H	Input Pulse Width (Synchronous Mode) $\overline{C3}$ (÷8 Prescaler Mode only)	125		84		62.5		ns
	Output Delay, 01-03 (Figure 7)							
t_{co}	(V_{OH} = 2.4V, Load B) TTL		700		460		340	ns
t_{cm}	(V_{OH} = 2.4V, Load D) MOS		450		450		340	ns
t_{cmos}	(V_{OH} = 0.7 V_{DD}, Load D) CMOS		2.0		1.35		1.0	μs
t_{IR}	Interrupt Release Time		1.2		0.9		0.7	μs

*t_r and $t_f \leq t_{CYCE}$

S6800 FAMILY

Figure 1. Bus Read Timing Characteristics (Read Information from PTM)

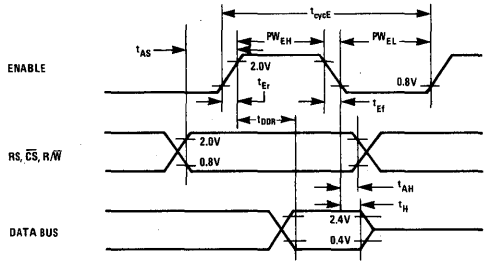


Figure 2. Bus Write Timing Characteristics (Write Information into PTM)

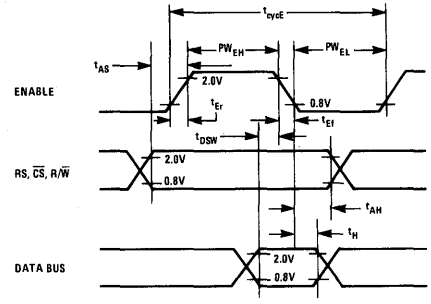


Figure 3. Input Pulse Width Low

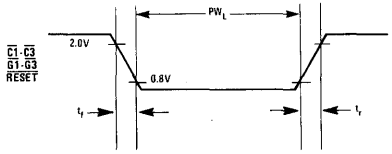


Figure 4. Input Pulse Width High

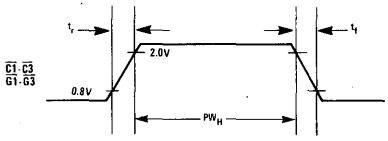


Figure 5. Input Setup and Hold Time

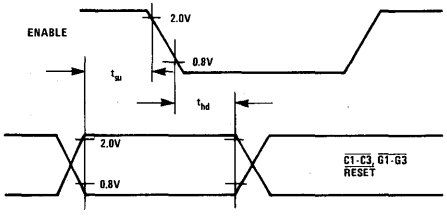
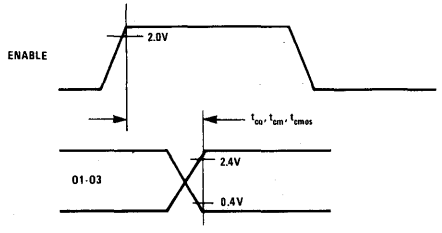


Figure 6. Output Delay



AMI

A Subsidiary of Gould Inc.

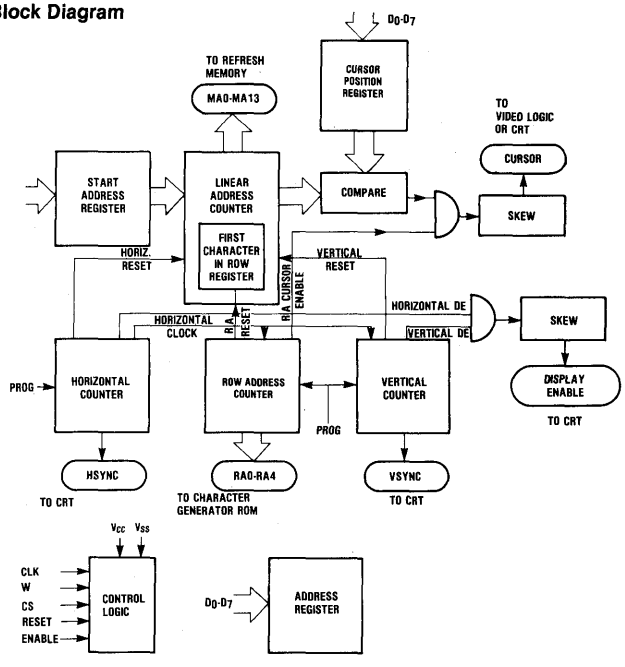
S68045/S68A045/S68B045

CRT CONTROLLER (CRTC)

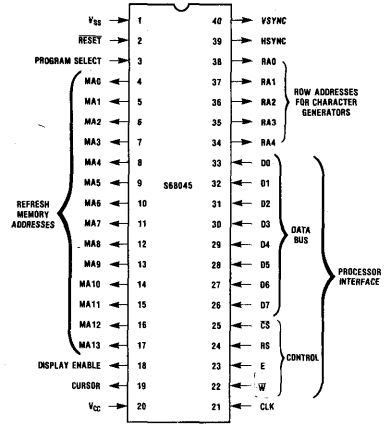
Features

- ☐ Generates Refresh Addresses and Row Selects
- ☐ Generates Video Monitor Inputs: Horizontal and Vertical Sync and Display Enable
- ☐ Low Cost; MC6845/SY6545 Pin Compatible
- ☐ Text Can Be Scrolled on a Character, Line or Page Basis
- ☐ Addresses 16K Bytes of Memory
- ☐ Screen Can Be Up to 128 Characters Tall By 256 Wide
- ☐ Character Font Can Be 32 Lines High With Any Width
- ☐ Two Complete ROM Programs
- ☐ Cursor and/or Display Can Be Delayed 0, 1 or 2 Clock Cycles
- ☐ Four Cursor Modes:
  - Non-Blink
  - Slow Blink
  - Fast Blink
  - Reverse Video With Addition of a Single TTL Gate
- ☐ Three Interlace Modes
  - Normal Sync
  - Interlace Sync
  - Interlace Sync and Video
- ☐ Full Hardware Scrolling
- ☐ NMOS Silicon Gate Technology
- ☐ TTL-Compatible, Single + 5 Volt Supply

Block Diagram



Pin Configuration



S6800 FAMILY

General Description

The S68045 CRT Controller performs the complex interface between an S6800 Family microprocessor and a raster scan display CRT system. The S68045 is designed to be flexible yet low cost. It is configured to both simplify the development and reduce the cost of equipment such as intelligent terminals, word processing, and information display devices.

The CRT Controller consists of both horizontal and vertical counting circuits, a linear address counter, and control registers. The horizontal and vertical counting circuits generate the Display Enable, HSYNC, VSYNC, and RA0-RA4 signals. The RA0-RA4 lines are scan line count signals to the external character generator ROM. The number of characters per character row, scan lines per character row, character rows per screen, and the horizontal and vertical SYNC position and width are all mask programmable. The S68045 is capable of addressing 16K of memory for display. The CRT may be scrolled or paged through the entire display memory under MPU control. The cursor control register determines the cursor location on the screen, and the cursor format can be programmed for fast blink, slow-blink, or non-blink appearance, with programmable size. By adding a single TTL gate, the cursor can even be reversed video. The device features two complete, independent programs implemented in user-specified ROM. Either set of programmable variables (50/60Hz refresh rate, screen format, etc.) is available to the user at any time.

The S68045 is pin compatible with the MC6845, operates from a single 5-volt supply, and is designed using the latest in minimum-geometry NMOS technology.

Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3°C to +7.0°C
Input Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

Bus Timing Characteristics

Symbol	Parameter	S68045		S68A045		S68B045		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{cyc(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er}, t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Electrical Characteristics

$V_{CC} = 5.0V \pm 5\%$; $V_{SS} = 0$, $T_A = 0°C$ to $+70°C$ unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage (except CLK)	2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage (except CLK)	−0.3		0.8	Vdc	
V_{IHC}	Input High Voltage Clock	2.2		V_{CC}	Vdc	
V_{ILC}	Input Low Voltage Clock	−0.3		.45	Vdc	
I_{IN}	Input Leakage Current		1.0	2.5	μAdc	
V_{OH}	Output High Voltage	2.4			Vdc	$I_{LOAD} = -100\mu A$
V_{OL}	Ouput Low Voltage			0.4	Vdc	$I_{LOAD} = 1.6mA$
P_D	Power Dissipation		600		mW	
C_{IN}	Input Capacitance D0-D7 All Others			12.5 10	pF pF	
C_{OUT}	Output Capacitance—All Outputs			10	pF	
P_{WCL}	Minimum Clock Pulse Width, Low	160			ns	
P_{WCH}	Clock Pulse Width, High	200		10,000	ns	
f_C	Clock Frequency			2.5	MHz	
t_{Cr}, t_{Cf}	Rise and Fall Time for Clock Input			20	ns	
t_{MAD}	Memory Address Delay Time			200	ns	
t_{RAD}	Raster Address Delay Time			200	ns	
t_{DTD}	Display Timing Delay Time			300	ns	
t_{HSD}	Horizontal Sync Delay Time			300	ns	
t_{VSD}	Vertical Sync Delay Time			300	ns	
t_{CDD}	Cursor Display Timing Delay Time			300	ns	

Systems Operation

The S68045 CRTC generates all of the signals needed for the proper operation of a CRT system including HSYNC, VSYNC, Display Enable, Cursor control signals (refer to Figure 1), the refresh memory addresses (MA0-MA13) and row addresses (RA0-RA4). The CRTC's timing is derived from the CLK input, which is divided down from the dot rate counter.

The CRTC, which is compatible with the 6800 family, communicates with the MPU by means of the standard 8-bit data bus. This primary data bus uses a buffered interface for writing information to the display refresh RAM by means of a separate secondary data bus. This arrangement allows the MPU to forget about the display except for those time periods when data is actually being changed on the screen. The address bus for the refresh RAM is continuously multiplexed between the MPU and the CRTC.

Since the MPU is allowed transparent read/write access to the display memory, the refresh RAM appears as just another RAM to the processor. This means that the refresh memory can also be used for program storage. Care should be taken by the system designer, however, to insure that the portion of memory being used for program storage is not actively displayed.

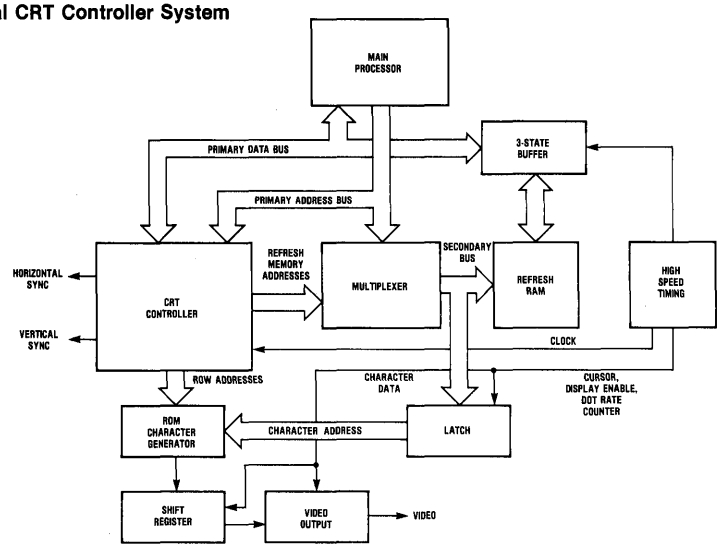
Displayed Data Control

Display Refresh Memory Addresses (MA0-MA13) — 14 bits of address provide the CRTC with access of up to 16K of memory for use in refreshing the screen.

Row Addresses (RA0-RA4) — 5 bits of data that provide the output from the CRTC to the character generator ROM. They allow up to 32 scan lines to be included in a character.

Cursor — This TTL compatible, active high output indicates to external logic that the cursor is being displayed.

Figure 1. Typical CRT Controller System



The character address of the cursor is held in a register, so the cursor's position is not lost even when scrolled off the screen.

CRT Control

All three CRT control signals are TTL compatible, active high outputs.

Display Enable — Indicates that valid data is being clocked to the CRT for the active display area.

Vertical Sync (VSYNC) — Makes certain the CRTC and the CRT's vertical timing are synchronized so the picture is vertically stable.

Horizontal Sync (HSYNC) — Makes certain the CRTC and the CRT's horizontal timing are synchronized so the picture is horizontally stable.

Processor Interface

All processor interface lines are three state, TTL/MOS compatible inputs.

Chip Select ($\overline{CS}$)—The $\overline{CS}$ line selects the CRTC whenlow to write to the internal Register File. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select — The RS line selects either the Address Register (RS = "0") or one of the Data Registers (RS = "1") of the internal Register File.

To address one of the software programmable registers (R12, R13, R14 or R15 in Table 2) first access the Address Register ($\overline{CS}$ = 0, RS = 0) and write the number of the desired register. Then write into the actual register by addressing the data register section ($\overline{CS}$ = 0, RS = 1) and enter the appropriate data.

Write ($\overline{W}$) — The $\overline{W}$ line allows a write to the internal Register File.

Data Bus (D0-D7) — The data bus lines (D0-D7) are write-only and allow data transfers to the CRTC internal register file.

Enable (E) — The Enable signal enables the data bus input buffers and clocks data to the CRTC. This signal is usually derived from the processor clock, and the high to low transition is the active edge.

S68045 Control Clock (CLK) — The clock signal is a high impedance, TTL/MOS compatible input which assures the CRTC is synchronized with the CRT itself. The CLK signal is divided down by external circuitry from the dot rate counter. The CLK frequency is equal

to the dot rate frequency divided by the width of a single character block (including framing) expressed in dots, CLK is equal to the character rate.

Program (PROG) — The voltage on this pin determines whether the screen format in ROM 0 (PROG LOW) or ROM 1 (PROG HIGH) is being used.

Reset ($\overline{RES}$) — The $\overline{RES}$ input resets the CRTC. An (active) low input on this line forces these actions:

a) MA0-MA13 are loaded with the contents of R12/R13 (the start address register).

b) The horizontal, vertical, and raster address counter are reset to the first raster line of the first displayed character in the first row.

c) All other outputs go low.

Note that none of the internal registers are affected by $\overline{RES}$.

$\overline{RES}$ on the CRTC differs from the reset for the rest of the 6800 family in the following aspects:

a) MA0-MA13 and RA0-RA4 go to the start addresses, instead of FFFF.

b) Display recommences immediately after $\overline{RES}$ goes high.

Internal Register Description — There is a bank of 15 control registers in the 68045, most of which are mask programmed. The exceptions are the Address Register, the two Start Address Registers (R12 & R13) and the Cursor Location Registers (R14 & R15). All software programmable registers are write only. The Address Register is 5 bits long. The software programmable registers are made available to the data lines whenever the chip select ($\overline{CS}$) goes low. When $\overline{CS}$ goes high, the data lines show a high impedance to the microprocessor.

Horizontal Total Register (R0) — The full horizontal period, expressed in character times, is masked in R0. (See Figure 2a).

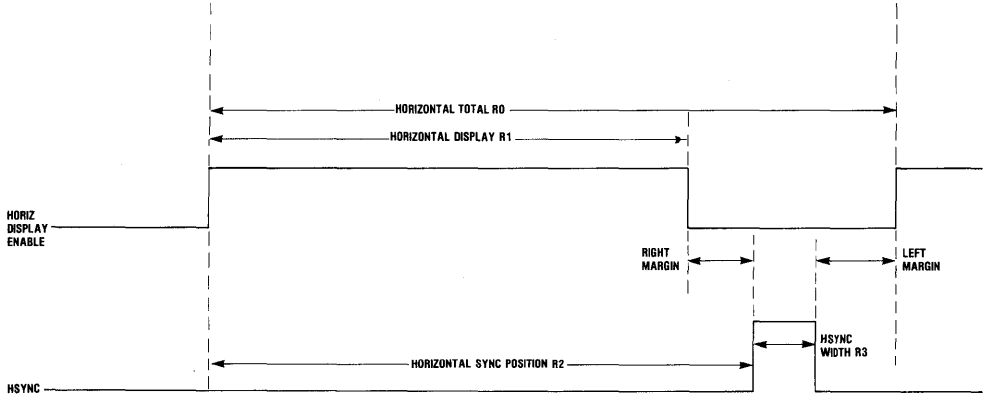
Horizontal Displayed Register (R1) — This register contains the number of characters to be actually displayed in a row. (See Figure 2a).

Horizontal SYNC Position Register (R2) — The contents of R2 (also in character times) should be slightly larger than the value in R1 to allow for a non-displayed right border. (See Figure 2a.)

Sync Width Register (R3) — The width of the HSYNC pulse expressed in character times is masked into the lower four bits of R3. The width of the HSYNC pulse has to be non-zero.

The width of the VSYNC pulse is masked into the upper

Figure 2a. Approximate Timing Diagram



FOR MORE EXACT DIAGRAMS REFER TO THE BACK OF THE DATA SHEET. THE HORIZONTAL DISPLAY ENABLE IS ANDED WITH THE VERTICAL DISPLAY ENABLE TO PRODUCE THE DISPLAY ENABLE AT PIN 18. NOTE THE (a) FIGURE IS TIMED IN TERMS OF INDIVIDUAL CHARACTERS, WHEREAS THE (b) FIGURE IS TIMED IN TERMS OF CHARACTER ROWS.

four bits of R3 without any modification, with the exception that all zeroes will make VSYNC 16 characters wide.

Vertical Total Register (R4) — This register contains the total number of character rows — both displayed and non-displayed — per screen. This number is just the total number of scan lines used divided by the number of scan lines in a character row. If there is a remainder, it is placed in R5. (See Figure 2b).

Vertical Total Adjust Register (R5) — See description of R4. A fractional number of character row times is used to obtain a refresh rate which is exactly 50HZ, 60HZ, or some other desired frequency. (See Figure 2b).

Vertical Displayed Register (R6) — This register contains the total number of character rows that are actually displayed on the CRT screen. (See Figure 2b).

Vertical SYNC Position (R7) — R7 contains the position of the vertical SYNC pulse in character row times with respect to the top character row. Increasing the value shifts the data up. (See Figure 2b).

Interlace Mode Register (R8) — R8 controls which of the three available raster scan modes will be used (See Figure 3).

- — Non-interlace or Normal sync mode
- — Interlaced sync mode
- — Interlaced sync and Video mode

The Cursor and Display Enable outputs can be delayed (skewed) 0, 1 or 2 clock cycles with respect to the refresh memory address outputs (MA0-MA13). The amount the cursor is delayed is independent of how much the Display Enable signal is delayed. This feature allows the system designer to account for memory address propagation delay through the RAM, ROM, etc.

Maximum Scan Line Register (R9) — Determines the number of scan lines per character row including top and bottom spacing.

Cursor Start Register (R10) — Contains the raster line where the cursor start (see Figure 4). The cursor start line can be anywhere from line 0 to line 31.

The cursor can be in one of the following formats.

- — Non-blinking
- — Slow blinking (1/16 the vertical refresh period)
- — Fast blinking (1/32 the vertical refresh period)
- — Reverse video (non-blinking, slow blinking, or fast
- — blinking)

The reverse video cursor needs an external TTL XOR gate to be placed in the video circuit.

To implement the reverse video cursor, the cursor start line (R10) should be set to line 0 and the cursor end line (R11) should be set to whatever is in R9 so that the cursor covers the entire block. On the circuit level, the output from the Cursor pin (pin 19) should be taken through the XOR gate along with the output from the shift register. (See Figure 5.) With this setup the character whose memory address is in the cursor register (R14/R15) will have its background high (because Cursor alone is high) but the character itself will be off (because both cursor and the character are both high.

Figure 2b. Approximate Timing Diagram

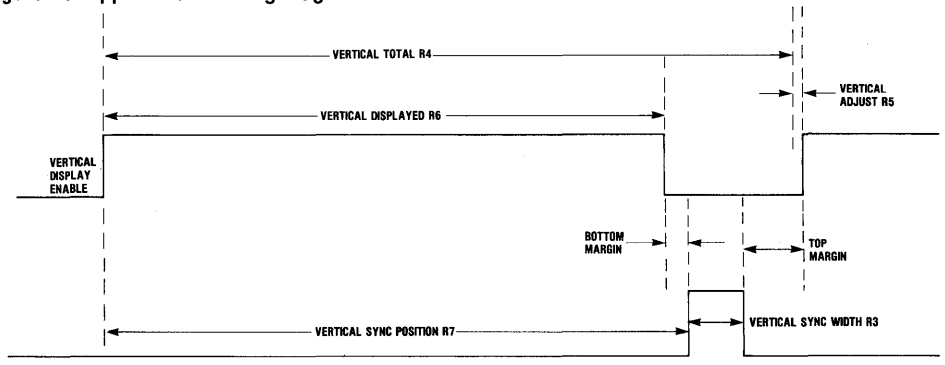


Figure 3. Interface Control

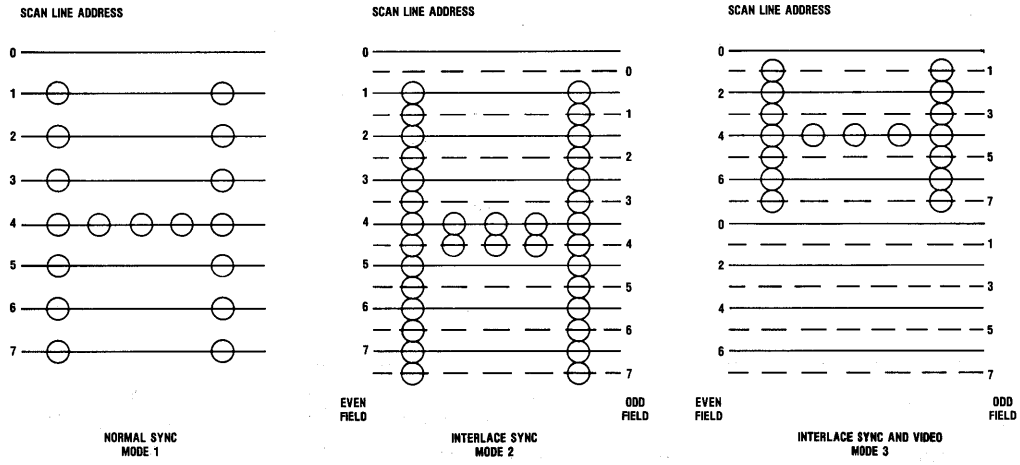
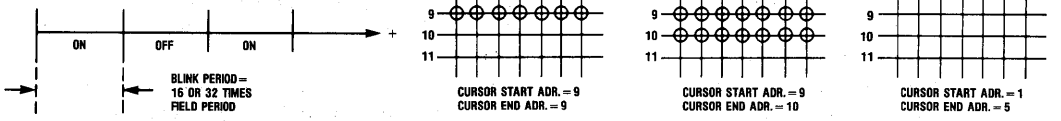


Figure 4. Cursor Control

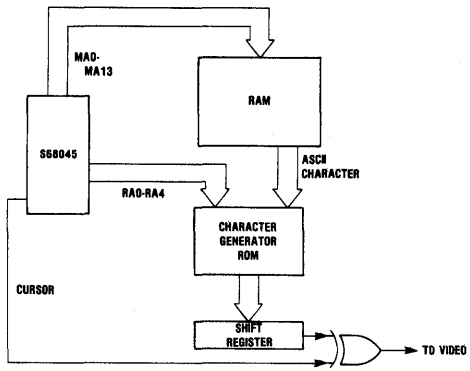
MODE	CURSOR DISPLAY MODE
1	Non-Blink
2	Cursor Non-Display
3	Blink, 1/16 Field Rate
4	Blink, 1/32 Field Rate



Memory Start Address Register (R12/R13) — These two software programmable, write-only registers taken together contain the memory address of the first character displayed on the screen. Register R12 contains the upper six bits of the fourteen refresh memory address bits, while R13 contains the lower eight bits. The Linear Address Generator begins counting from the address in R12/R13. By changing the starting address, the display can be scrolled up or down through the 16K memory block by character, line or page. If the value in R12/R13 is near the end of the 16K block the display will wrap around to the front.

Cursor Address Register (R14/R15) — These two software programmable, write-only registers, taken together, contain the address in memory of the cursor character. Register R14 contains the upper six bits and register R15 contains the lower eight bits of the character. Cursor position is associated with an address in memory rather than with a position on the screen. This

Figure 5. Implementation of a Reversed Video Cursor



way cursor position is not lost when the display is scrolled.

Address Register — The five bit address register is unique in that it does not store any CRT-related information, but is used as the address storage register in an indirect access of the other registers. When the Register Select pin (RS) is low, the address register is accessed by D0-D4. When RS is high, the register whose address is in the address register is accessed.

CRTC Internal Description

There are four counters which determine what the CRTC's output will be (see Block Diagram):

1) Horizontal Counter
2) Vertical Counter
3) Row Address Counter
4) Linear Address Counter

The first two counters, and to some extent the third, take care of the physical operation of the monitor. The Linear Address Counter, on the other hand, is responsible for the data that is displayed on the screen.

Surrounding these counters are the registers R0-R15. Coincidence logic continuously compares the contents of each counter with the contents of the register(s) associated with it. When a match is found, appropriate action is taken; the counter is reset to a fixed or dynamic value, or a flag (such as VSYNC) is set, or both.

Two sets of registers — The start Address Register (R12/R13) and the Cursor Position Register (R14/R15) — are programmable via the Data lines (D0-D7). The other registers are all mask programmed. There are two ROM programs available on each chip. Selection of which ROM program will be accessed is performed by the PROG pin.

Horizontal Counter

The Horizontal Counter produces four output flags: HSYNC, Horizontal Display Enable, Horizontal Reset to the Linear Address Counter, and the horizontal clock.

The Horizontal Counter is driven by the character rate clock, which was derived from the dot rate clock (see Table 1). Immediately after the valid display area is entered the Horizontal Counter is reset to zero but continues incrementing.

HSYNC is the only one of the four signals which is fed to an external device (the CRT). The Horizontal Counter is compared to registers R0, R2 and R3 to give an HSYNC of the desired frequency (R0), position (R2) and width (R3). (See Figure 2a.)

Horizontal Display Enable is an internal flag which, when ANDed with Vertical DE, is output at the Display Enable pin. The Horizontal Counter determines the proper frequency (R0), and width (R1).

The Horizontal Reset and the horizontal clock are actually identical signals: the only difference is the way they are used. Both are pulsed once for each scan line,

Table 1. Comparison of all CRTC Clocks

NAME	LOCATION OF CLOCK	DIVIDED BY:	CONTROLLING REGISTER	PRODUCES
DOT RATE CLOCK	EXTERNAL	TOTAL WIDTH OF A CHARACTER BLOCK IN DOTS	EXTERNAL	CHARACTER RATE CLOCK
CHARACTER RATE CLOCK	EXTERNAL INPUT	TOTAL NUMBER OF CHARACTERS IN A ROW	R0	HORIZONTAL CLOCK
HORIZONTAL CLOCK	INTERNAL	TOTAL NUMBER OF SCAN LINES IN A CHARACTER ROW	R9	ROW ADDRESS CLOCK
ROW ADDRESS CLOCK	INTERNAL	TOTAL NUMBER OF CHARACTER ROWS PER SCREEN	R4, R5	VERTICAL CLOCK

Table 2. CRTC Internal Register Assignment

REGISTER#	REGISTER FILE	BITS 7	6	5	4	3	2	1	0
R0	HORIZONTAL TOTAL	N_{ht}-1							
R1	HORIZONTAL DISPLAYED	N_{hd}							
R2	HORIZONTAL SYNC POSITION	N_{hsp}-1							
R3	HORIZONTAL SYNC WIDTH	N_{vsw}				N_{hsw}			
R4	VERTICAL TOTAL	N_{vt}-1							
R5	VERTICAL TOTAL ADJUST	N_{adj}							
R6	VERTICAL DISPLAYED	N_{vd}							
R7	VERTICAL SYNC POSITION	N_{vsp}-1							
R8	INTERLACE MODE	CURSOR SKEW		DIS. ENAB. SKEW				INTERLACE	
R9	MAX SCAN LINE ADDRESS	N_r-1*							
R10	CURSOR START	CURSOR BLINK		CURSOR START					
R11	CURSOR END	CURSOR END							
R12	START ADDRESS (H)	START ADDRESS (H)							
R13	START ADDRESS (L)	START ADDRESS (L)							
R14	CURSOR (H)	CURSOR (H)							
R15	CURSOR (L)	CURSOR (L)							

*For Interlace Sync and Video operation, R9 should contain N_r-1

NOT USED

CURSOR SKEW

BIT 7	BIT 6	RESULT
0	0	NO SKEW
0	1	1 CHARACTER SKEW
1	0	2 CHARACTER SKEW
1	1	ILLEGAL

DISPLAY ENABLE SKEW

BIT 5	BIT 4	RESULT
0	0	NO SKEW
0	1	1 CHARACTER SKEW
1	0	2 CHARACTER SKEW
1	1	ILLEGAL

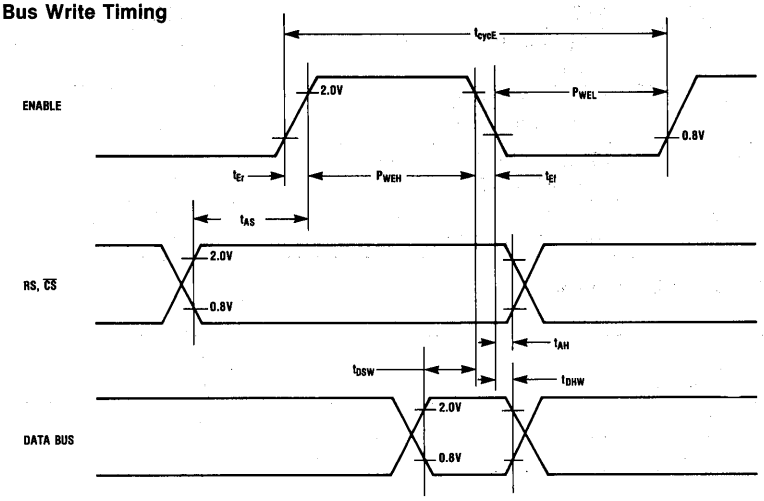
INTERLACE CONTROL

BIT 1	BIT 0	MODE
0	0	NON-INTERLACE
1	0	NON-INTERLACE
0	1	INTERLACE SYNC
1	1	INTERLACE SYNC & VIDEO

CURSOR CONTROL

MODE	BIT 6	BIT 5
NON-BLINK	0	0
NON-BLINK	0	1
BLINK @ 1/16 FIELD PERIOD	1	0
BLINK @ 1/32 FIELD PERIOD	1	1

Figure 6. Bus Write Timing



so their frequency is equal to the character rate clock frequency divided by the entire horizontal period (display, non-display and retrace) expressed in character times (which is stored in R0). The horizontal clock drives the Vertical and Row address Counters. The horizontal reset is discussed with the Linear Address Counter.

Vertical Counter

The Vertical Counter produces three output flags: VSYNC, Vertical Display Enable, and Vertical Reset to the Linear Address Counter. The Vertical Counter is driven by the horizontal clock. Immediately after vertical retrace the Vertical Counter is reset to zero but continues incrementing.

VSYNC is the only one of the three signals which is fed to an external device (the CRT). The Vertical Counter is compared to registers R3, R4, R5 and R7 to give a VSYNC of the desired frequency (R4, R5), position (R7) and width (R3). (See Figure 2b.)

Vertical Display Enable is an internal flag which, when ANDed with Horizontal DE, is output at the Display Enable pin. The Vertical Counter determines the proper frequency (R4, R5) and width (R6).

Vertical Reset is pulsed once for each screen. The frequency of Vertical Reset is equal to the horizontal clock frequency divided by the total number of scan lines in a screen (which is equal to (R4 × R9) + R5). It will be discussed with the Linear Address Counter.

Row Address Counter

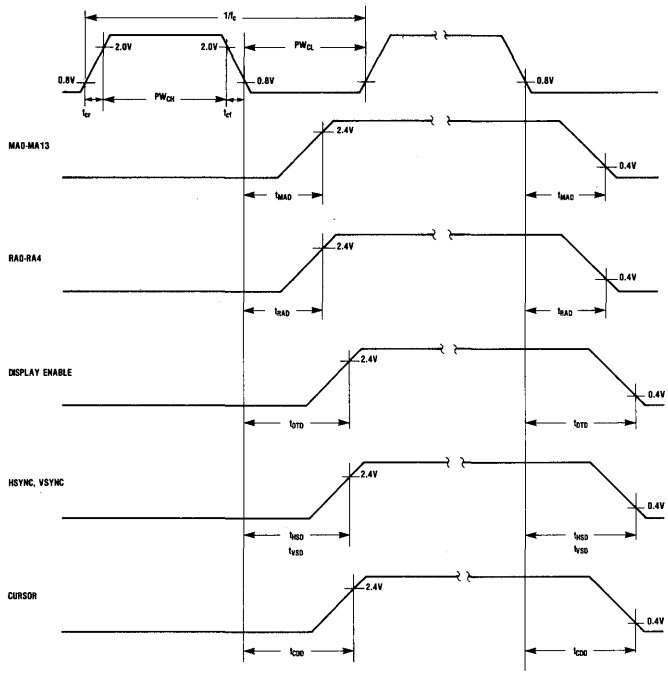
The Row Address Counter produces three sets of output: the five Row Address lines (RA0-RA4), the Row Address Cursor Enable flag and the Row Address Reset flag. The Row Address Counter is driven by the horizontal clock. Immediately after a full character row has been completed by the Row Address Counter is reset to zero but continues incrementing. Note that the Row Address Counter actually counts scan lines, which are different from character rows. A full character row consists of however many scan lines are in register R9.

The Row Address Lines, RA0-RA4, are the only data lines from the Row Address Counter that are fed to an external device (the character generator ROM). The Row Address lines just carry the count that is currently in the Row Address Counter. The counter is reset whenever the count equals the contents of the Maximum Scan Line Register (R9.)

Row Address Cursor Enable is a flag going to the Cursor output AND gate. The Row Address Cursor Enable flag goes high whenever the count in the Row Address Counter is greater than or equal to the Cursor Start Register (R10) but less than or equal to the Cursor End Register (R11). The other input to the Cursor output AND gate goes high whenever the address in the Linear Address Counter is equal to the address in the Cursor Position Register (R14/R15).

Row Address Reset is pulsed whenever the Row Ad-

Figure 7. Bus Timing Character



dress Counter is reset. It will be discussed with the Linear Address Counter.

Linear Address Counter

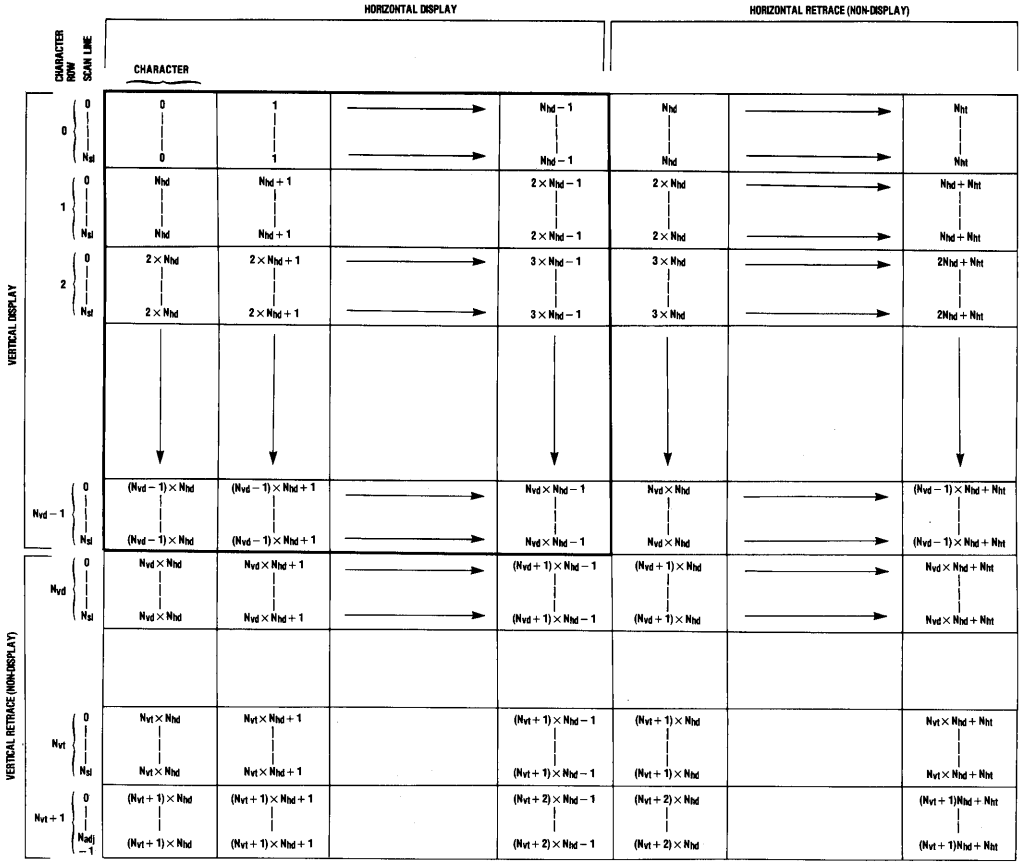
The Linear Address Counter (LAC) produces only one set of outputs: The Refresh Memory Address lines (MA0-MA13). These fourteen bits are fed externally to the Refresh RAM and internally to the Cursor Position coincidence circuit. The LAC is driven by the character rate clock and continuously increments during the display, non-display and retrace portions of the screen. It contains an internal read/write register which stores the memory address of the first displayed character in the current row.

When any of the three Reset flags already mentioned (Horizontal, Row Address and Vertical) is pulsed, the value in the internal register is loaded into the counter. If the reset is a Horizontal Reset the value in the internal register is not modified before the load. If the reset is a Row Address Reset, the value in the internal "first character" register is first increased by the number of characters displayed on a single character row (register R1). The new contents of the internal register are then loaded into the Linear Address Counter.

If the reset is a Vertical Reset, the value in Start Address Register. (R12/R13) is first loaded into the internal register, and then into the Linear Address Counter.

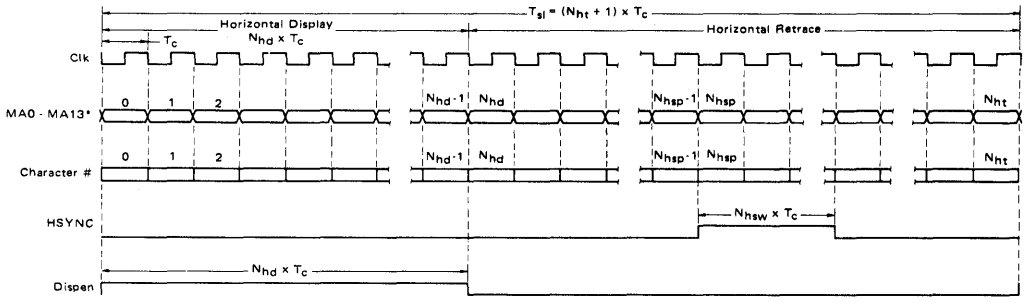
The fourteen output lines allow 16K of memory to be accessed. By incrementing or decrementing the number in the Start Address Register, the screen can be scrolled forward or backward through Display Refresh RAM on a character, line, or page basis.

Figure 8. Refresh Memory Addressing (MA0-MA13) State Chart



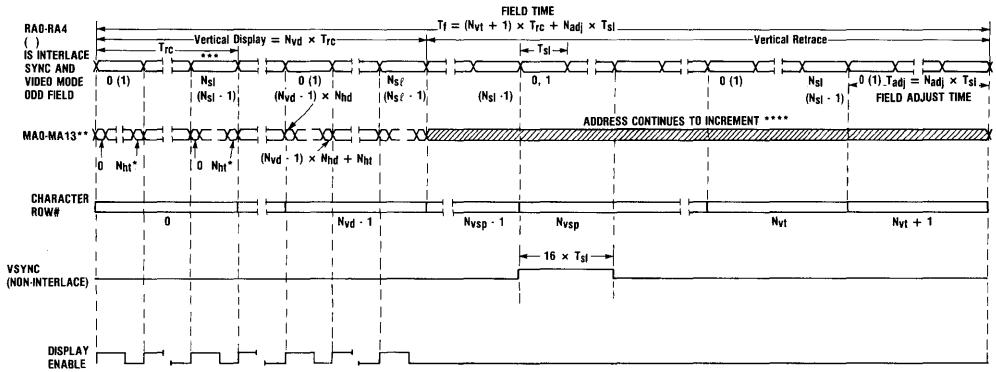
NOTE 1: THE INITIAL MA IS DETERMINED BY THE CONTENTS OF START ADDRESS REGISTER, R12/R13. TIMING IS SHOWN FOR R12/R13 = 0. ONLY NON-INTERFACE AND INTERFACE SYNC MODES ARE SHOWN.

Figure 9. CRTC Horizontal Timing



*Timing is shown for first displayed scan row only. See Chart in Figure 16 for other rows. The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

Figure 10. CRTC Vertical Timing

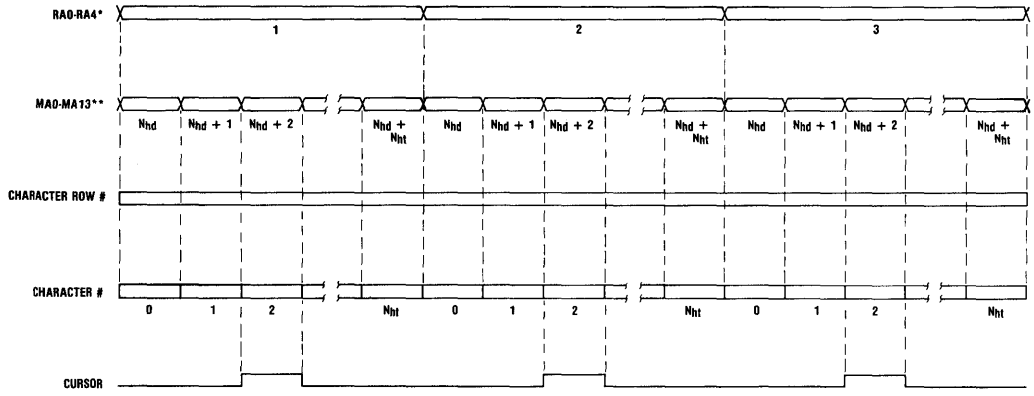


* N_{ht} - there must be an even number of character times for both interlace modes.

** Initial MA is determined by R12/R13 (Start Address Register), which is zero in this timing example.

*** N_{ht} must be an even number of scan lines for Interlace Sync and Video Mode.

Figure 11. Cursor Timing



* *Timing is shown for non-interlace and interlace sync modes.*
Example shown has cursor programmed as:
Cursor Register = N_{hd} + 2
Cursor Start = 1
Cursor End = 3

** The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

A Subsidiary of Gould Inc.

S6846

ROM-I/O-TIMER

Features

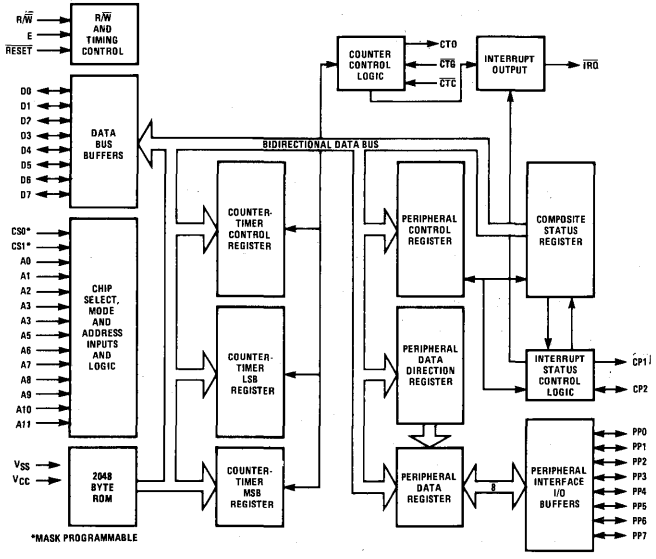
- ☐ 2048 x 8-Bit Bytes of Mask-Programmable ROM
- ☐ 8-Bit Bidirectional Data Port for Parallel Interface Two Control Lines
- ☐ Programmable Interval Timer-Counter Functions
- ☐ Programmable I/O Peripheral Data, Control and Direction Registers
- ☐ Compatible With the Complete S6800 Microcomputer Product Family
- ☐ TTL-Compatible Data and Peripheral Lines
- ☐ Single 5 Volt Power Supply

General Description

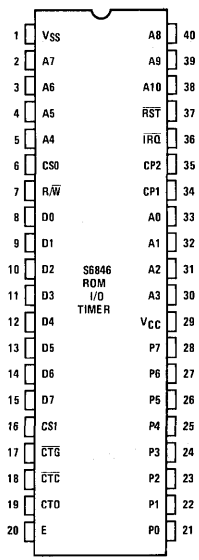
The S6846 combination chip provides the means, in conjunction with the S6802, to develop a basic 2-chip microcomputer system. The S6846 consists of 2048 bytes of mask-programmable ROM, an 8-bit bidirectional data port with control lines, and a 16-bit programmable timer-counter.

This device is capable of interfacing with the S6802 (basic S6800, clock and 128 bytes of RAM) as well as the S6800 if desired. No external logic is required to interface with most peripheral devices.

Block Diagram



Pin Configuration



S6800 FAMILY

General Description (Continued)

The S6846 combination chip may be partitioned into three functional operating sections: read-only memory, timer-counter functions, and a parallel I/O port.

Read-Only Memory (ROM)

The mask-programmable ROM section is similar to other AMI ROM products. The ROM is organized in a 2048 by 8-bit array to provide read-only storage for a minimum microcomputer system. Two mask-programmable chip selects are available for user definition.

Address inputs A_0-A_{10} allow any of the 2048 bytes of ROM to be uniquely addressed. Internal registers associated with the I/O functions may be selected with A_0, A_1 and A_2. Bidirectional data lines (D_0-D_7) allow the transfer of data between the MPU and the S6846.

Timer-Counter Functions

Under software control this 16-bit binary counter may be programmed to count events, measure frequencies and time intervals, or similar tasks. It may also be used for square wave generation, single pulses of controlled duration, and gated delayed signals. Interrupts may be generated from a number of conditions selectable by software programming.

The timer-counter control register allows control of the interrupt enables, output enables, and selection of an internal or external clock source. Input pin CTC (counter-timer clock) will accept an asynchronous pulse to be used as a clock to decrement the internal register for the counter-timer. If the divide-by-8 prescaler is used, the maximum clock rate can be four times the master clock frequency with a maximum of 4MHz. Gate input ($\overline{CTG}$) accepts an asynchronous TTL-compatible signal which may be used as a trigger or gating function to the counter-timer. A counter-timer output (CTO) is also available and is under software control via selected bits in the timer-counter control register. This mode of operation is dependent on the control register, the gate input, and the clock source.

Parallel I/O Port

The parallel bidirectional I/O port has functional operational characteristics similar to the B port on the S6821 PIA. This includes 8 bidirectional data lines and two handshake control signals. The control and operation of these lines are completely software programmable.

The interrupt input (CP1) will set the interrupt flags of the peripheral control register. The peripheral control (CP2) may be programmed to act as an interrupt input (set CSR2) or as a peripheral control output.

Figure 1. Typical Microcomputer

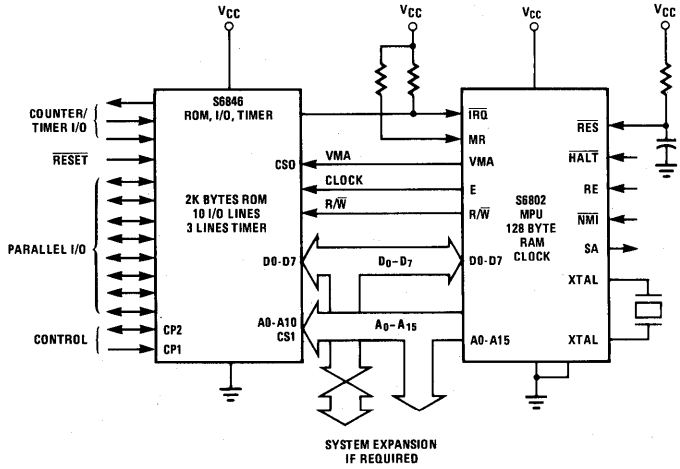


Figure 1 is a block diagram of a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the S6800 Microcomputer family.

Absolute Maximum Ratings

Supply Voltage	− 0.3Vdc to + 7.0Vdc
Input Voltage	− 0.3Vdc to + 7.0Vdc
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	− 55°C to + 150°C
Thermal Resistance θ_{JA}	
Ceramic	50°C/W
Plastic	100°C/W
Cerdip	60°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D = P_{INT} + P_{PORT}$
$P_{INT} = I_{CC} \times V_{CC}$, Watts—Chip Internal Power
P_{PORT} = Port Power Dissipation, Watts—User Determined

For most applications $P_{PORT} \leftarrow P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K + (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part, K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Electrical Characteristics: (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	All Inputs	V_{SS} + 2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	All Inputs	V_{SS} − 0.3		V_{SS} + 0.8	Vdc	
V_{OS}	Clock Overshoot/Undershoot — Input High Level — Input Low Level		V_{CC} − 0.5 V_{SS} − 0.5		V_{CC} + 0.5 V_{SS} + 0.5	Vdc	
I_{IN}	Input Leakage Current	R/W, Reset, CS_0, CS_1 CP_1, CTG, CTC, E, A_0-A_{11}		1.0	2.5	μAdc	V_{IN} = 0 to 5.25 Vdc
I_{TSI}	Three-State (Off State) Input Current	D_0-D_7 PP_0-PP_7, CR_2		2.0	10	μAdc	V_{IN} 0.4 to 2.4Vdc
V_{OH}	Output High Voltage	D_0-D_7 Other Outputs	V_{SS} + 2.4 V_{SS} + 2.4			Vdc	I_{LOAD} = − 205μAdc, I_{LOAD} = − 100μAdc
V_{OL}	Output Low Voltage	D_0-D_7 Other Outputs			V_{SS} + 0.4 V_{SS} + 0.4	Vdc	I_{LOAD} = 1.6mAdc I_{LOAD} = 3.2mAdc

Electrical Characteristics: (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{OH}	Output High Current (Sourcing)				μAdc	
	D_0-D_7	−205				V_{OH} = 2.4Vdc
	Other Outputs	−200				
	CP_2, PP_0-PP_7	−1.0		−10	mADC	V_0 = 1.5Vdc, the current for driving other than TTL, e.g., Darlington Base
I_{OL}	Output Low Current (Sinking)				mAdc	
	D_0-D_7	1.6				V_{OL} = 0.4Vdc
	Other Outputs	3.2				
I_{LOH}	Output Leakage Current (Off State) IRQ			10	μAdc	V_{OH} = 2.4Vdc
P_{INT}	Internal Power Dissipation (measured at T_A = 0°C)			1000	mW	
C_{IN}	Capacitance D_0-D_7			20	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
	PP_0-PP_7, CP_2			12.5		
	A_0-A_{10}, R/W, Reset, CS_0, CS_1, CP_1, CTC, CTG			10		
	IRQ			7.5		
C_{OUT}	PP_0-PP_7, CP_2, CTO			5.0	pF	
				10		
f	Frequency of Operation	0.1		1.0	MHz	
	Clock Timing					
t_{cycE}	Cycle Time	1.0			μs	
t_{RL}	Reset Low Time	2			μs	
t_{IR}	Interrupt Release			1.6	μs	

AMI

A Subsidiary of Gould Inc.

S6850/S68A50/S68B50

ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER (ACIA)

Features

- ☐ 8-Bit Bi-directional Data Bus for Communication with MPU
- ☐ False Start Bit Deletion
- ☐ Peripheral/Modem Control Functions
- ☐ Double Buffered Receiver and Transmitter
- ☐ One or Two Stop Bit Operation
- ☐ Eight and Nine-Bit Transmission With Optional Even and Odd Parity
- ☐ Parity, Overrun and Framing Error Checking
- ☐ Programmable Control Register
- ☐ Optional ÷1, ÷16, and ÷64 Clock Modes
- ☐ Up to 500,000 bps Transmission

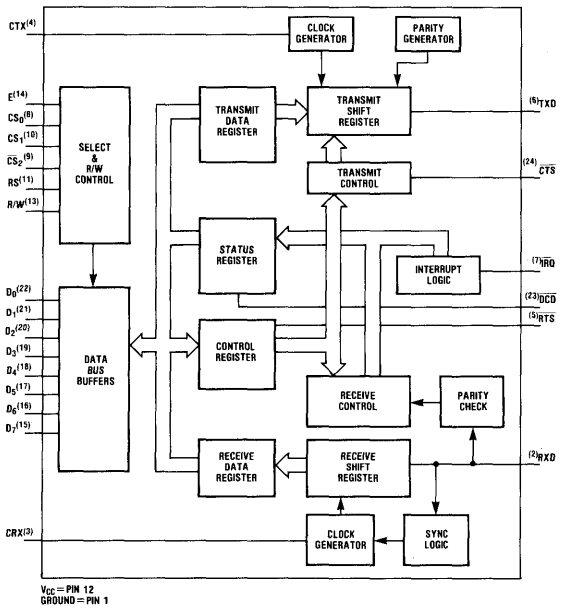
Functional Description

The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

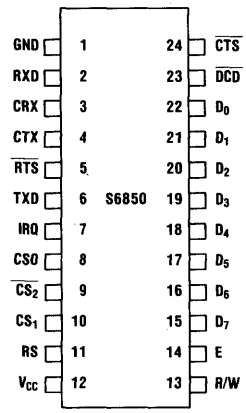
The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

S6800 FAMILY

Block Diagram



Pin Configuration



Absolute Maximum Ratings*

Supply Voltage	−0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Input Voltage	−0.3V to +7.0V
Storage Temperature Range	−55°C to +150°C

*NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (Static) Characteristics: (V_{CC} = 5.0V ±5%, T_A = 25°C, unless otherwise noted.)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IHT}	Input High Threshold Voltage	+2.0	—	—	Vdc
V_{ILT}	Input Low Threshold Voltage	—	—	+0.8	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.0 Vdc) R/W, RS, CS_0, CS_1, $\overline{CS_2}$, Enable	—	1.0	2.5	μAdc
I_{TSI}	Three-State (Off State) Input Current (V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = max) D_0, D_7	—	2.0	10	μAdc
V_{OH}	Output High Voltage (I_{LOAD} = 100μAdc, Enable Pulse Width 25μs) All Outputs Except $\overline{IRQ}$	+2.4	—	—	Vdc
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc) Enable Pulse Width 25μs	—	—	+0.4	Vdc
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$	—	1.0	10	μAdc
P_D	Power Dissipation	—	300	525	mW
C_{IN}	Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)				pF
	D_0 - D_7		—	10	12.5
	R/W, RS, CS_0, CS_1, $\overline{CS_2}$, RXD, $\overline{CTD}$, $\overline{DCD}$, CTX, CRX		—	7.0	7.5
	Enable		—	7.0	7.5
C_{OUT}	Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	—	—	10	pF

Figure 1. Enable Signal Characteristics

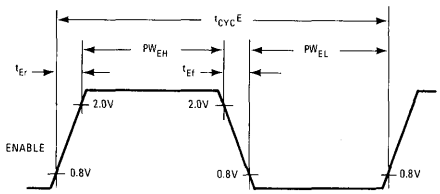
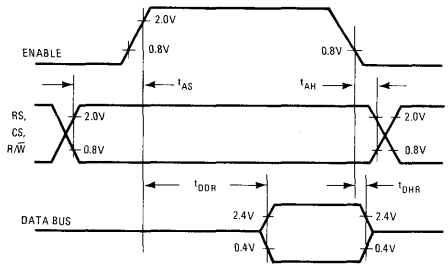


Figure 2. Bus Read Timing Characteristics



AC (Dynamic) Characteristics

Loading = 130pF and one TTL load for D_0-D_7 = 20pF and 1 TTL load for RTS and TXD = 100pF and 3KΩ to V_{CC} for IRQ.

		S6850		S68A50		S68B50		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
$t_{CYC(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er}, t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DDR}	Data Delay Time, Read		320		220		180	ns
t_{DHR}	Data Hold Time, Read	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Transmit/Receive Characteristics

Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
f_C	÷1 mode			500	KHz
	÷16 mode			800	KHz
	÷64 mode			800	KHz
PW_{CL}	Clock Pulse Width, Low State	600			nsec
PW_{CH}	Clock Pulse Width, High State	600			nsec
t_{TDD}	Delay Time, Transmit Clock to Data Out			1.0	μsec
t_{RDSU}	Set Up Time, Receive Data	500			nsec
t_{RDH}	Hold Time, Receive Data	500			nsec
t_{IRQ}	Delay Time, Enable to $\overline{IRQ}$ Reset			1.2	μsec
t_{RTS}	Delay Time, Enable to $\overline{RTS}$			1.0	μsec

Figure 3. Bus Write Timing Characteristics

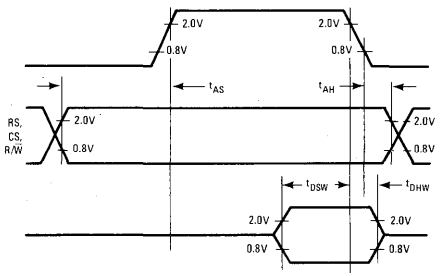


Figure 4. Bus Timing Test Loads

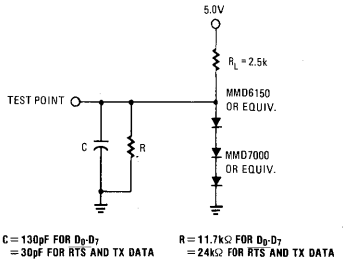
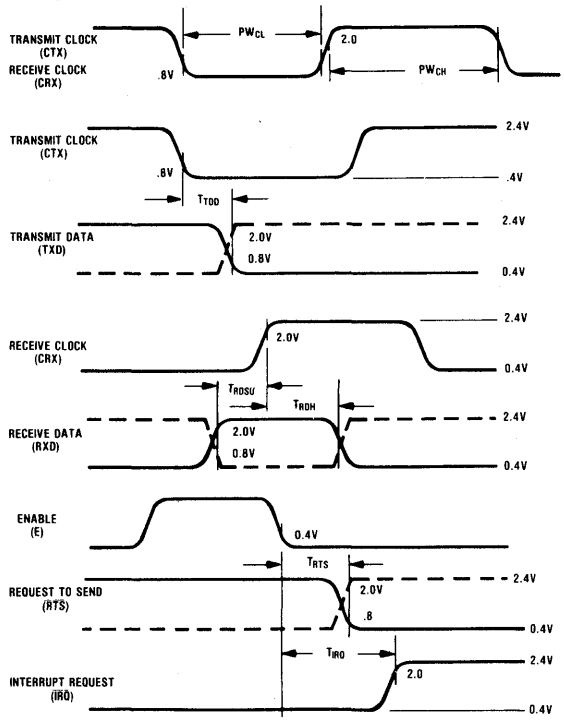


Figure 5. Transmit/Receive Timing



MPU/ACIA Interface

Pin	Label	Function
(22)	D_0	**ACIA Bi-directional Data Lines**—The bi-directional data lines (D_0-D_7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation. The Read/Write line is in the read (high) state when the ACIA is selected for a read operation.
(21)	D_1	
(20)	D_2	
(19)	D_3	
(18)	D_4	
(17)	D_5	
(16)	D_6	
(15)	D_7	
(14)	E	**ACIA Enable Signal**—The Enable signal (E) is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the S6800 02 clock.
(13)	R/W	**Read/Write Control Signal**—The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), the ACIA output driver is turned on and a selected register is read. When it is low, the ACIA output driver is turned off and the MPU writes into a selected register. Thus, the Read/Write signal is used to select the Read Only or Write Only registers within the ACIA.

MPU/ACIA Interface (Continued)

Pin	Label	Function
(8) (10) (9)	CS_0 CS_1 $\overline{CS_2}$	**Chip Select Signals**—These three high impedance TTL compatible input lines are used to address an ACIA. A particular ACIA is selected when CS_0 and CS_1 are high and $\overline{CS_2}$ is low. Transfers of data to and from ACIA are then performed under the control of Enable, Read/Write, and Register Select.
(11)	RS	**Register Select Signal**—The Register Select line is a high impedance input that is TTL compatible and is used to select the Transmit/Receive Data or Control/Status registers in the ACIA. The Read/Write signal line is used in conjunction with Register Select to select the Read Only or Write Only register in each register pair.
(7)	$\overline{IRQ}$	**Interrupt Request Signal**—Interrupt request is a TTL compatible, open drain active low output that is used to interrupt the MPU. The Interrupt Request remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

ACIA/Modem or Peripheral Interface

Pin	Label	Function
(4)	CTX	**Transmit Clock**—The Transmit Clock is a high impedance TTL compatible input used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(3)	CRX	**Receive Clock**—The Receive Clock is a high impedance TTL compatible input used for synchronization of received data. (In the ÷ 1 mode, the clock and data must be synchronized externally.) The receiver strobes the data on the positive transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(2)	RXD	**Received Data**—The Received Data line is a high impedance TTL compatible input through which data is received in a serial NRX (Non Return to Zero) format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.
(6)	TXD	**Transmit Data**—The Transmit Data output line transfers serial NRZ data to a modem or other peripheral device. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.
(24)	$\overline{CTS}$	**Clear-to-Send**—This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem's "clear-to-send" active low output by inhibiting the Transmitter Data Register Empty status bit (TDRE).
(5)	RTS	**Request-to-Send**—The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The active state is low. The Request-to-Send output is controlled by the contents of the ACIA control register.
(23)	$\overline{DCD}$	**Data Carrier Detected**—This high impedance TTL compatible input provides automatic control of the receiving end of a communications link by means of the modem "Data-Carrier-Detect" or "Received-Line-Signal Detect" output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receiver Interrupt Enable (RIE) is set.
(12)	V_{CC}	+5 volts ±5%
(1)	GND	Ground

Application Information

Internal Registers—The ACIA has four internal registers utilized for status, control, receiving data, and transmitting data. The register addressing by the R/W and RS lines and the bit definitions for each register are shown in Table 1.

Table 1. Definition of ACIA Registers

	BUFFER ADDRESS			
	RS•$\overline{R/W}$	**RS•R/W**	**$\overline{RS}$•$\overline{R/W}$**	**$\overline{RS}$•R/W**
DATA BUS LINE NUMBER	TRANSMIT DATA REGISTER	RECEIVER DATE REGISTER	CONTROL REGISTER	STATUS REGISTER
	(WRITE ONLY)	(READ ONLY)	(WRITE ONLY)	(READ ONLY)
0	DATA BIT 0*	DATA BIT 0*	CLK. DIVIDE SEL. (CR0)	RX DATA REG. FULL (RDRF)
1	DATA BIT 1	DATA BIT 1	CLK. DIVIDE SEL. (CR1)	TX DATA REG. EMPTY (TDRE)
2	DATA BIT 2	DATA BIT 2	WORD SEL. 1 (CR2)	DATA CARRIER DET. LOSS (DCD)
3	DATA BIT 3	DATA BIT 3	WORD SEL. 2 (CR3)	CLEAR-TO-SEND (CTS)
4	DATA BIT 4	DATA BIT 4	WORD SEL. 3 (CR4)	FRAMING ERROR (FE)
5	DATA BIT 5	DATA BIT 5	TX CONTROL 1 (CR5)	OVERRUN (OVRN)
6	DATA BIT 6	DATA BIT 6	TX CONTROL 2 (CR6)	PARITY ERROR (PE)
7	DATA BIT 7***	DATA BIT 7**	RX INTERRUPT ENABLE (CR7)	INTERRUPT REQUEST (IRQ)

Notes: * Leading bit = LSD = Bit 0
** Unused data bits in received character will be "0's."
*** Unused data bits for transmission are "don't care's."

ACIA Status Register—Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This Read Only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of: transmitting data register, the receiving data register and error status and the modem status inputs of the ACIA.

Receiver Data Register Full (RDRF) [Bit 0]—Receiver Data Register Full indicates that received data has been transferred to the Receiver Data Register. RDRF is cleared after an MPU read of the Receiver Data Register or by a Master Reset. The cleared or empty state indicates that the contents of the Receiver Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE) [Bit 1]—The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$) [Bit 2]—The Data Carrier Detect bit will be high when the $\overline{DCD}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated if the Receiver Interrupt Enable (RIE) is set. It remains high until the interrupt is cleared by reading the Status Register and the Data Register or a Master Reset occurs. If the $\overline{DCD}$ input remains high after Read Status and Read Data or Master Reset have occurred, the $\overline{DCD}$ Status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$) [Bit 3]—The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-

Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master Reset does not affect the Clear-to-Send status bit.

Framing Error (FE) [Bit 4]—Framing error indicates that the received character is improperly framed by the start and stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receiver data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN) [Bit 5]—Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receiver Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until Overrun is reset. Character synchronization is maintained during the Overrun condition. The overrun indication is reset after the reading of data from the Receive Data Register. Overrun is also reset by the Master Reset.

Parity Error (PE) [Bit 6]—The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{IRQ}$) [Bit 7]—The IRQ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt that is set and enabled will be indicated in the status register. Any time the $\overline{IRQ}$ output is low the IRQ bit will be high to indicate the interrupt or service request status.

Control Register—The ACIA control Register consists of eight bits of write only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send modem control output.

Counter Divide Select Bits (CR0 and CR1)—The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a Master Reset for the ACIA which clears the Status Register and initializes both the receiver and transmitter. Note that after a power-on or a power-fail restart, these bits must be set High to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4)—The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not double-buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6)—Two Transmitter Control bits provide for the control of the Transmitter Buffer Empty interrupt output, the Request-to-Send output and the transmission of a BREAK level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled
1	1	$\overline{RTS}$ = low, Transmitting Interrupt Disabled and Transmits a BREAK level on the Transmit Data Output

Receiver Interrupt Enable Bit (RIE) (CR7)—Interrupt will be enabled by a high level in bit position 7 of the Control Register (CR7). Interrupts caused by the Receiver Data Register Full being high or by a low to high transition on the Data Carrier Detect signal line are enabled or disabled by the Receiver Interrupt Enable Bit.

Transmit Data Register (TDR)—Data is written in the Transmit Data Register during the peripheral enable time (E) when the ACIA has been addressed and RS•R/W is selected. Writing data into the register causes the Transmit Data Register Empty bit in the status register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one

bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDR) bit to indicate empty.

Receive Data Register (RDR)—Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) (in the status buffer) to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receive Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

Operational Description

From the MPU Bus interface the ACIA appears as two addressable RAM memory locations. Internally, there are four registers; two read-only and two write-only registers. The read-only registers are status and receive data, and the write only registers are control and transmit data. The serial interface consists of serial transmit and receive lines and three modem/ peripheral control lines.

During a power-on sequence, the ACIA is internally latched in a reset condition to prevent erroneous output transitions. This power-on reset latch can only be released by the master reset function via the control register; bits b_0 and b_1 are set "high" for a master reset. After master resetting the ACIA, the programmable control register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none) and etc.

Transmitter—A typical transmitting sequence consists of reading the ACIA status register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmitter Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a shift register where it is serialized and transmitted from the Tx Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the data register, the status register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted. This second character will be automatically transferred into the shift register when the first character transmission is completed. The above sequence continues until all the characters have been transmitted.

Receiver—Data is received from a peripheral by means of the Rx Data input. A divide by one clock ratio is provided for an externally synchronized clock (to its data) while the divide by 16 and 64 ratios are provided for internal synchronization.

Bit synchronization in the divide by 16 and 64 modes is obtained by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the status register along with framing error, overrun error, and receiver data register full. In a typical receiving sequence, the status register is read to determine if a character has been received from a peripheral. If the receiver data register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. The status register can be read again to determine if another character is available in the receiver data register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

AMI

A Subsidiary of Gould Inc.

S6852/S68A52/S68B52

SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

Features

- ☐ Programmable Interrupts From Transmitter, Receiver, and Error Detection Logic
- ☐ Character Synchronization on One or Two Sync Codes
- ☐ External Synchronization Available for Parallel-Serial Operation
- ☐ Programmable Sync Code Register
- ☐ Up to 600k bps Transmission
- ☐ Peripheral/Modem Control Functions
- ☐ Three Bytes of FIFO Buffering on Both Transmit and Receive
- ☐ Seven, Eight, or Nine Bit Transmission
- ☐ Optional Even and Odd Parity
- ☐ Parity, Overrun, and Underflow Status
- ☐ Clock Rates:
  - 1.0MHz
  - 1.5MHz
  - 2.0MHz

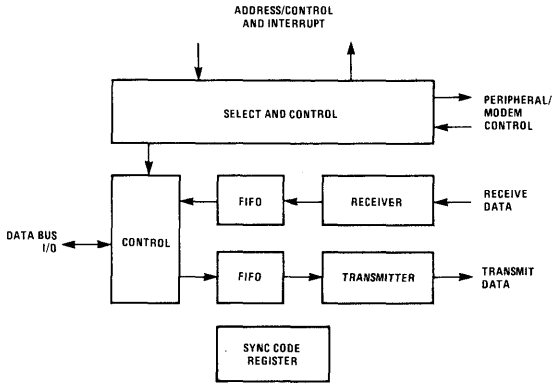
General Description

The S6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the S6800 Microprocessor systems.

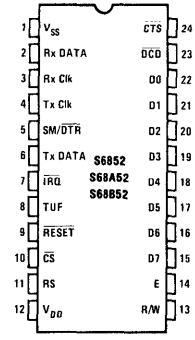
The bus interface of the S6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus sytem is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control,

S6800 FAMILY

Block Diagram



Pin Configuration



General Description (Continued)

receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

Absolute Maximum Ratings:

Supply Voltage	−0.3 to +7.0V
Input Voltage	−0.3 to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55° to +150°C
Thermal Resistance	+70°C/W

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted.)

Symbol	Characteristics		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage		V_{SS} + 2.0			Vdc
V_{IL}	Input Low Voltage				V_{SS} + 0.8	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25Vdc)	Tx Clk, Rx Clk, Rx Data, Enable, $\overline{Reset}$, RS, R/$\overline{W}$, $\overline{CS}$, $\overline{DCD}$, $\overline{CTS}$		1.0	2.5	μAdc
I_{TSI}	Three State (Off State) Input Current (V_{IN} = 0.4 to 2.4Vdc, V_{CC} = 5.25Vdc)	D_0-D_7		2.0	10	μAdc
V_{OH}	Output High Voltage I_{LOAD} = −205μAdc, Enable Pulse Width<25μs I_{LOAD} = −100μAdc, Enable Pulse Width<25μs	D_0-D_7 Tx Data, $\overline{DTR}$, TUF	 V_{SS} + 2.4 V_{SS} + 2.4		 Vdc	Vdc
V_{OL}	Output Low Voltage I_{LOAD} = 1.6mAdc, Enable Pulse Width<25μs				V_{SS} + 0.4	Vdc
I_{LOH}	Output Leakage Current (Off State) V_{OH} = 2.4Vdc	$\overline{IRQ}$		1.0	10	μAdc
P_D	Power Dissipation			300	525	mW
C_{IN}	Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	D_0-D_7 All Other Inputs			12.5 7.5	pF
C_{OUT}	Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	Tx Data, SM/$\overline{DTR}$, TUF $\overline{IRQ}$			10 5.0	pF

Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C unless otherwise noted.)

Symbol	Characteristic	S6852		S68A52		S68B52		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
PW_{CL}	Minimum Clock Pulse Width, Low	700		400		280		ns
PW_{CH}	Minimum Clock Pulse Width, High	700		400		280		ns
f_C	Clock Frequency		600		1000		1500	kHz
t_{RDSU}	Receive Data Setup Time	350		200		160		ns

* 10μs or 10% of the pulse width, whichever is smaller.

Electrical Characteristics (Continued) (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C unless otherwise noted.)

Symbol	Characteristic	S6852 Min.	S6852 Max.	S68A52 Min.	S68A52 Max.	S68B52 Min.	S68B52 Max.	Unit
t_{RDH}	Receive Data Hold Time	350		200		160		ns
t_{SM}	Sync Match Delay Time		1.0		0.666		0.500	µs
t_{TDD}	Clock-to-Data Delay for Transmitter		1.0		0.666		0.500	µs
t_{TUF}	Transmitter Underflow		1.0		0.666		0.500	µs
t_{DTR}	$\overline{DTR}$ Delay Time		1.0		0.666		0.500	µs
t_{IR}	$\overline{Interrupt\ Request}$ Release Time		1.2		0.800		0.600	µs
t_{Res}	$\overline{Reset}$ Minimum Pulse Width	1.0		0.666		0.500		µs
t_{CTS}	$\overline{CTS}$ Setup Time	200		150		120		ns
t_{DCD}	$\overline{DCD}$ Setup Time	500		350		250		ns
t_r, t_f	Input Rise and Fall Times (except Enable) (0.8V to 2.0V)		1.0		1.0		1.0	µs

Bus Timing Characteristics

Symbol	Characteristic	S6852 Min.	S6852 Max.	S68A52 Min.	S68A52 Max.	S68B52 Min.	S68B52 Max.	Unit
Read								
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.5		µs
PW_{EH}	Enable Pulse Width, High	0.45	25	0.28	25	0.22	25	µs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		µs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns
Write								
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.5		µs
PW_{EH}	Enable Pulse Width, High	0.45	25	0.28	25	0.22	25	µs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		µs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

AMI

A Subsidiary of Gould Inc.

S6854/S68A54/S68B54

ADVANCED DATA LINK CONTROLLER

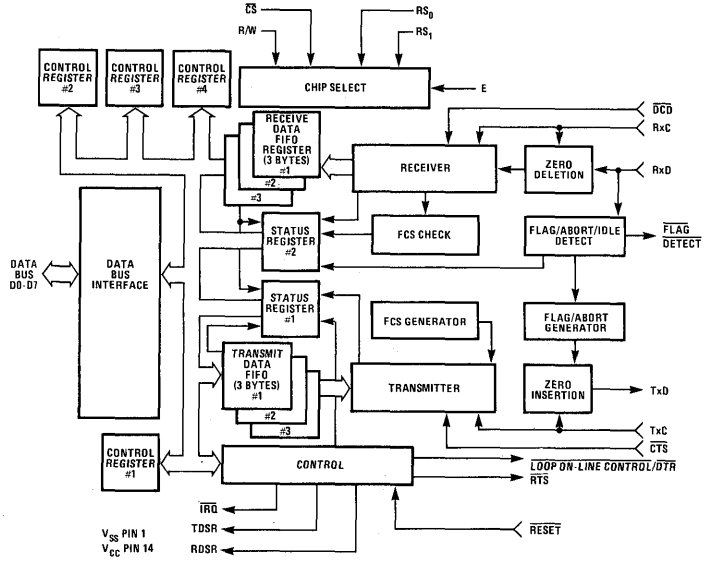
Features

- ☐ S6800 Compatible
- ☐ Protocol Features
  - ☐ Automatic Flag Detection and Synchronization
  - ☐ Zero Insertion and Deletion
  - ☐ Extendable Address, Control and Logical Control Fields (Optional)
  - ☐ Variable Word Length Info Field — 5, 6, 7, or 8-bits
  - ☐ Automatic Frame Check Sequence Generation and Check
  - ☐ Abort Detection and Transmission
  - ☐ Idle Detection and Transmission
- ☐ Loop Mode Operation
- ☐ Loop Back Self-Test Mode
- ☐ NRZ/NRZI Modes
- ☐ Quad Data Buffers for Each Rx and Tx
- ☐ Prioritized Status Register (Optional)
- ☐ MODEM/DMA/Loop Interface

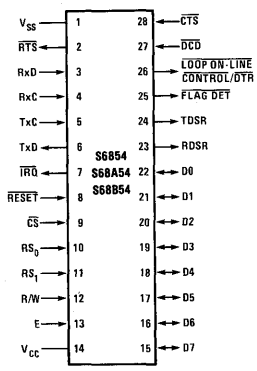
General Description

The S6854 ADLC performs the complex MPU/data communication link function for the "Advanced Data Communication Control Procedure" (ADCCP), High Level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations.

Block Diagram



Pin Configuration



Absolute Maximum Ratings*

Supply Voltage	− 0.3 to + 7.0V
Input Voltage	− 0.3 to + 7.0V
Operating Temperature Range	0° to + 70°C
Storage Temperature Range	− 55° to + 150°C
Thermal Resistance	70° C/W

* This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics: (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage		V_{SS} + 2.0		Vdc		
V_{IL}	Input Low Voltage				V_{SS} + 0.8	Vdc	
I_{IN}	Input Leakage Current	All Inputs Except D_0-D_7		1.0	2.5	μAdc	V_{IN} = 0 to 5.25 Vdc
I_{TSI}	Three-State (Off State) Input Current	D_0-D_7		2.0	10	μAdc	V_{IN} = 0.4 to 2.4 Vdc V_{CC} = 5.25 Vdc
V_{OH}	Output High Voltage	D_0-D_7 All Others	V_{SS} + 2.4 V_{SS} + 2.4			Vdc Vdc	I_{LOAD} = − 205μAdc I_{LOAD} = − 100μAdc
V_{OL}	Output Low Voltage				V_{SS} + 0.4	Vdc	I_{LOAD} = 1.6mAdc
I_{LOH}	Output Leakage Current (Off State)	$\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation				850	mW	
C_{IN}	Capacitance	D_0-D_7 All Other Inputs			12.5 7.5	pF pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
C_{OUT}		$\overline{IRQ}$ All Others			5.0 10	pF pF	

Symbol	Characteristic	S6854		S68A54		S68B54		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
PW_{CL}	Minimum Clock Pulse Width, Low	700		450		280		ns
PW_{CH}	Minimum Clock Pulse Width, High	700		450		280		ns
f_C	Clock Frequency		0.66		1.0		1.5	MHz
t_{RDSU}	Receive Data Setup Time	250		200		120		ns
t_{RDH}	Receive Data Hold Time	120		100		60		ns
t_{RTS}	Request-to-Send Delay Time		680		460		340	ns
t_{TDD}	Clock-to-Data Delay for Transmitter		460		320		250	ns
t_{FD}	Flag Detect Delay Time		680		460		340	ns
t_{DTR}	DTR Delay Time		680		460		340	ns
t_{LOC}	Loop On-Line Control Delay Time		680		460		340	ns
t_{RDSR}	RDSR Delay Time		540		400		340	ns
t_{TDSR}	TDSR Delay Time		540		400		340	ns
t_{IR}	Interrupt Request Release Time		1.2		0.9		0.7	μs
t_{RES}	Reset Minimum Pulse Width	1.0		0.65		0.40		μs
t_r, t_f	Input Rise and Fall Times (except Enable) (0.8V to 2.0V)		1.0*		1.0*		1.0*	μs

* 1.0μs or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics (V_{CC} = + 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + + 70°C unless otherwise noted.)

Symbol	Characteristic	S6854		S68A54		S68B54		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read								
t_{CYC}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns
Write								
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		0.22		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

AMI

A Subsidiary of Gould Inc.

S6810/S68A10/S68B10

128x8 STATIC READ/WRITE MEMORY

Features

- ☐ Organized as 128 Bytes of 8 Bits
- ☐ Static Operation
- ☐ Bidirectional Three-State Data Input/Output
- ☐ Six Chip Enable Inputs (Four Active Low, Two Active High
- ☐ Single 5 Volt Power Supply
- ☐ TTL Compatible
- ☐ Maximum Access Time
  - 450ns for S6810
  - 360ns for S68A10
  - 250ns for S68B10

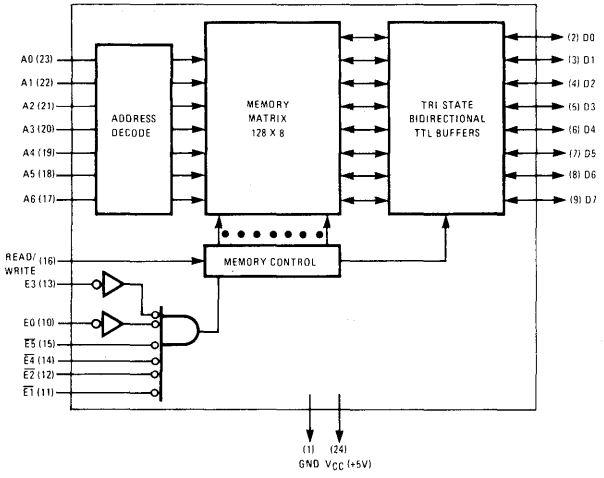
General Description

The S6810/S68A10 and S68B10 are static 128x8 Read/Write Memories designed and organized to be compatible with the S6800/S68A00 and S68B00 Microprocessors. Interfacing to the S6810/S68A10 and S68B10 consists of an 8-bit bidirectional data bus, seven address lines, s single Read/Write control line and six chip enable lines, four negative and two positive.

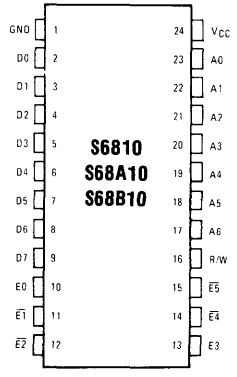
For ease of use, the S6810/S68A10 and S68B10 are a totally static memory requiring no clocks or cell refresh. The S6810/S68A10 and S68B10 are fabricated with N-Channel silicon gate depletion load technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

S6800 FAMILY

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage	− 0.3V to + 7.0V
Input Voltage	− 0.3V to + 7.0V
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	− 55°C to + 150°C

D.C. Characteristics:

(V_{CC} = + 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{IN}	Input Current (A_n, R/W, CS_n, $\overline{CS_n}$)			2.5	μAdc	V_{IN} = 0V to 5.25V
V_{OH}	Output High Voltage	2.4			Vdc	I_{OH} = − 205μA
V_{OL}	Output Low Voltage			0.4	Vdc	I_{OL} = 1.0mA
I_{LO}	Output Leakage Current			10	μAdc	CS = 0.8V or CS = 2.0V, (Three State) V_{OUT} = 0.4V to 2.4V
I_{CC}	Supply Current S6810 S68A10/S68B10			80 100	mAdc mAdc	V_{CC} = 5.25V, all other pins grounded, T_A = 0°C

A.C. Characteristics:

Read Cycle

(V_{CC} = + 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

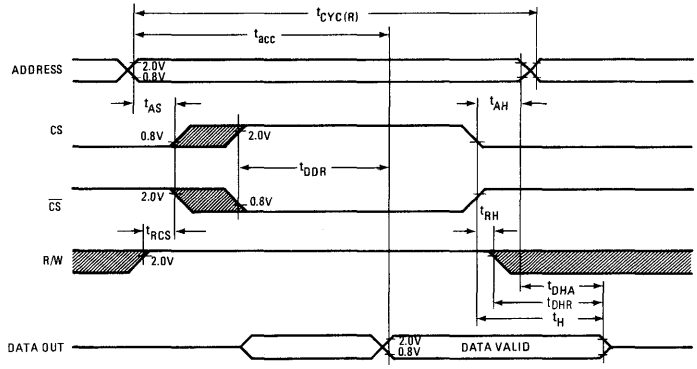
		S6810		S68A10		S68B10		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
$t_{cyc(R)}$	Read Cycle Time	450		360		250		ns
t_{acc}	Access Time		450		360		250	ns
t_{AS}	Address Setup Time	20		20		20		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{DDR}	Data Delay Time (Read)		230		220		180	ns
t_{RCS}	Read to Select Delay Time	0		0		0		ns
t_{DHA}	Data Hold from Address	10		10		10		ns
t_H	Output Hold Time	10		10		10		ns
t_{DHR}	Data Hold from Read	10	60	10	60	10	60	ns
t_{RH}	Read Hold from Chip Select	0		0		0		ns

Write Cycle

(V_{CC} = +5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	S6810 Min.	S6810 Max.	S68A10 Min.	S68A10 Max.	S68B10 Min.	S68B10 Max.	Units
$t_{CYC(W)}$	Write Cycle Time	450		360		250		ns
t_{AS}	Address Setup Time	20		20		20		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{CS}	Chip Select Pulse Width	300		250		210		ns
t_{WCS}	Write to Chip Select Delay Time	0		0		0		ns
t_{DSW}	Data Setup Time (Write)	190		80		60		ns
t_H	Input Hold Time	10		10		10		ns
t_{WH}	Write Hold Time from Chip Select	0		0		0		ns

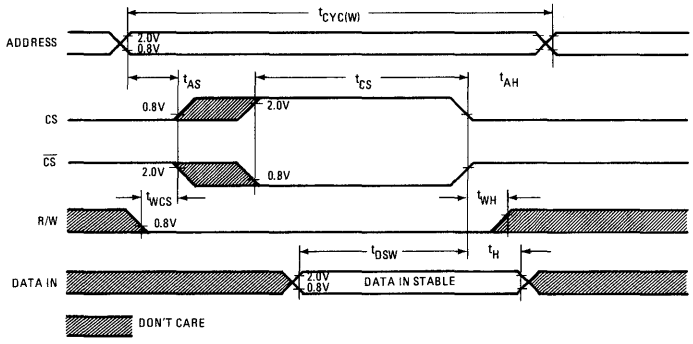
Read Cycle Timing



DON'T CARE

NOTE: CS AND $\overline{CS}$ CAN BE ENABLED FOR CONSECUTIVE READ CYCLES PROVIDED R/W REMAINS AT V_{IH}.

Write Cycle Timing

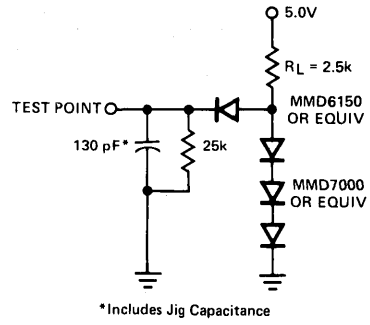


DON'T CARE

NOTE: CS AND $\overline{CS}$ CAN BE ENABLED FOR CONSECUTIVE WRITE CYCLES PROVIDED R/W IS STROBED TO V_{IH} BEFORE OR COINCIDENT WITH THE ADDRESS CHANGE, AND REMAINS HIGH FOR TIME t_{AS}.

S6800 FAMILY

AC Test Load



*Includes Jig Capacitance

AMI®

A Subsidiary
of Gould Inc.

S80 Family

S80 Family Selection Guide

S83	Operating System Processor (OSP)

AMI®

A Subsidiary of Gould Inc.

Preliminary Data Sheet **S83**

OPERATING SYSTEM PROCESSOR (OSP)

Features

- ☐ Z80™ CPU Internal Architecture
- ☐ Z80 Instruction Set
- ☐ On-board 8K Byte ROM
- ☐ Internal/External ROM Modes
- ☐ Address, Data, and Bus Control Signals Function Identically to the Original Z80
- ☐ Dynamic RAM Interface Including Address Multiplexing and Row and Column Address Strobe Signals.

Functional Description

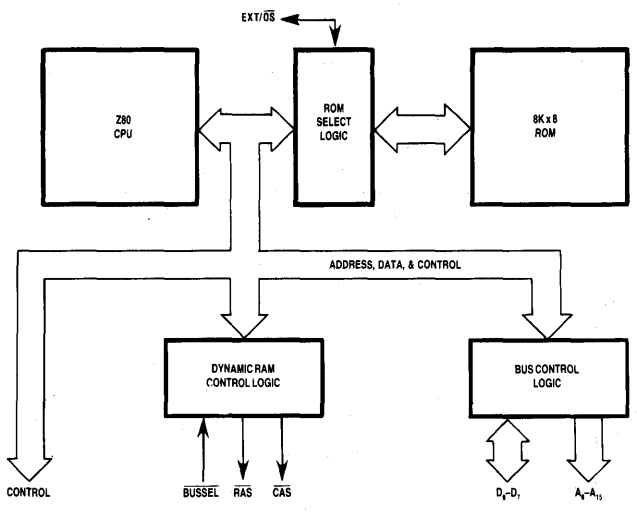
The OS Processor chip is a single-chip microcomputer system with a core Z80 CPU and on-chip 8K × 8 (64K bit) ROM. This chip possesses all of the hardware capabilities present in the standard Z80 chip. All control, address, and data signals are functionally identical to the standard Z80, making it completely hardware compatible with all Z80 peripheral chips. All Z80 instructions are present including the 8080 subset, providing software compatibility as well.

Additional logic has been incorporated to allow the OS Processor to be directly connected to 64K Dynamic RAMs.

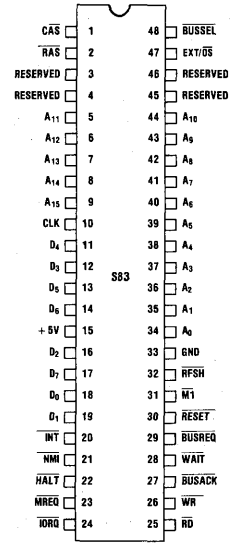
ROM select logic is incorporated to allow the internal ROM to be selectively enabled or disabled under software control.

The OS Processor is fabricated in a NMOS process, uses a single 5 volt power supply, and will be packaged in a 48-pin DIP package.

Block Diagram



Pin Configuration



S80 FAMILY

Z80 is a registered trademark of Zilog, Inc.

ROM Select Logic

This functional block controls access to the internal ROM and also determines whether the processor will be brought up in an internal or external mode.

When the $\overline{RESET}$ signal goes high and EXT/$\overline{OS}$ is high, the ROM enable latch is disabled, thereby turning off the internal ROM, and the processor begins execution at address 0000H just as a standard Z80 CPU would after reset. This is referred to as EXTERNAL MODE. In the external mode, the processor behaves identically to a standard Z80 CPU, except that the upper 16 memory addresses, FFF0H to FFFFH, are reserved. Address FFFFH is used for ROM control. The other 15 locations have been reserved for further expansion of system control functions.

When the $\overline{RESET}$ signal goes high and the mode pin EXT/$\overline{OS}$ is low, the internal ROM is switched on by enabling the ROM enable latch, and the processor is forced to execute NOP instructions until it reaches address FF00H in the internal ROM, where it begins execution. Any internal bootstrap program code should start at address FF00H. This is referred to as INTERNAL MODE.

In the internal mode, the 8K × 8 internal ROM is switched on and is effectively overlayed on top of external memory. This ROM occupies the upper 8K bytes of the full 64K byte Z80 address space. When data is read from the internal ROM, this data appears on the external data bus. Data written to this address space does appear on the external data bus, however, and will be written to any RAM that occupies that space. This RAM data cannot be read by the processor until the internal ROM has been turned off. The internal ROM may be switched on or off by writing a zero to bit 0 of memory address FFFFH. The ROM may be switched back on at any time by writing a one to bit 0 of memory address FFFFH.

Memory locations FFF0H through FFFFH are reserved. No code should be written in this area. Any accesses to these sixteen addresses will be treated as external memory accesses.

While the EXT/$\overline{OS}$ pin serves as an input on reset to set the initial operating mode of the processor, it serves a different purpose during normal operation. After reset, the EXT/$\overline{OS}$ pin becomes an output, and reflects the state of the internal $\overline{OS}$ signal. This signal indicates that a memory read is being made to the internal ROM address space (addresses E000H — FFEFH) and that the internal ROM enable latch is set. This signal is used to control the addressing of external memory that resides in the same address space as the internal ROM. Its use will be covered later under "Prototyping With the S83".

Dynamic RAM Interface

In addition to the refresh circuitry inherent to the Z80 CPU, the S83 features circuitry that enables the 8 high order address bits to be multiplexed onto the low order 8 address lines for row and column addressing of 64K dynamic RAMs. Row address and column address strobes are also generated by the S83.

Bus Selection: For each memory cycle, the user may determine whether or not the addresses will be multiplexed by use of the $\overline{BUSSEL}$ (BUS SELect) input. $\overline{BUSSEL}$ is sampled slightly after the rising edge of each T_2 clock state. If $\overline{BUSSEL}$ is low, the memory access is a standard Z80 access with non-multiplexed addresses, and $\overline{CAS}$ is not generated, however $\overline{RAS}$ is generated. If $\overline{BUSSEL}$ is high, the multiplexing process and generation of $\overline{CAS}$ is allowed to continue. A short time after $\overline{RAS}$ goes low, the low byte of the address bus will begin changing over to reflect the upper 8 bits of the address the Z80 has generated. After the new address (the column address) is stable, $\overline{CAS}$ goes low. These two strobes clock the row and column addresses into the dynamic RAMs.

Because only the upper 8 bits of the address bus remain stable throughout the entire memory access, selection of $\overline{BUSSEL}$ should be done with the upper 8 address lines only unless some form of address latching is used. If it is desired to use any of the lower 8 address lines (A_0-A_7), they must be latched on the falling edge of $\overline{MREQ}$, otherwise false decoding may occur when the address lines are multiplexed.

$\overline{BUSSEL}$ is qualified with $\overline{MREQ}$ internally, so it is not necessary to include $\overline{MREQ}$ in decoding for $\overline{BUSSEL}$, and the $\overline{RAS}$/$\overline{CAS}$ logic and $\overline{BUSSEL}$ sampling circuitry only operates during memory accesses. It is inoperative for I/O and interrupt cycles.

$\overline{BUSSEL}$ is also used to selectively block accesses to the internal ROM, and this usage will be discussed under "Prototyping With the S83".

Wait States: Because of the tighter access times required by the Z80 CPU during an opcode fetch ($\overline{M1}$ cycle), the S83 automatically inserts a wait state on $\overline{M1}$ cycles if the user has selected a multiplexed memory

cycle with the $\overline{BUSSEL}$ input. This wait state is not added if a standard non-multiplexed bus cycle has been selected.

The user may insert additional wait states if desired, however care must be exercised not to hold the processor in a wait state so long that refresh requirements are violated, as the S83, like the Z80, does not generate any refresh signals while in a wait state.

Also, during an $\overline{M1}$ cycle, if the user adds additional wait states beyond the one the processor has inserted, $\overline{RAS}$ will go high on the third rising clock edge after $\overline{MREQ}$ goes low, regardless of whether or not clock state T_3 has been reached yet. This does not violate dynamic RAM timing constraints, as $\overline{CAS}$ will always go high before $\overline{RAS}$ is generated again.

Bus Request (DMA) Cycles: When the Z80 is bus requested and an external device gains control of the bus, the address multiplexers do not function. The $\overline{RAS}$ and $\overline{CAS}$ logic, however, does continue to function. If an external DMA device generates a $\overline{MREQ}$ signal, $\overline{RAS}$ will be generated. Depending on the state of $\overline{BUSSEL}$, $\overline{CAS}$ may or may not be generated. This feature allows a DMA device to refresh dynamic RAMs while it performs its DMA task.

Prototyping With the S83

While the main purpose of $\overline{BUSSEL}$ is to control the dynamic RAM interface logic, it also controls access to the internal ROM. If an access to the internal ROM is attempted and $\overline{BUSSEL}$ is low, that access will be blocked, and instead the processor will access the external data bus using a non-multiplexed Z80 address. This input, together with the EXT/$\overline{OS}$ output, allows an external EPROM to be substituted for the internal ROM and still have its accesses controlled by the ROM enable latch. This is accomplished by using the EXT/$\overline{OS}$ output as the chip select for the EPROM, and also feeding this signal into the $\overline{BUSSEL}$ input. Since EXT/$\overline{OS}$ can only become low when the ROM enable latch is on, the functionality of internal vs. external memory spaces is still preserved. If it is desired to have an external ROM or EPROM in the address range E000H — FFFFH (not substituting for the internal ROM), its address decoding should include EXT/OS = HIGH. This will ensure that when an external EPROM is chip selected and $\overline{BUSSEL}$ pulled low to select non-multiplexed addresses, the user is not inadvertantly decoding an internal ROM access. The inclusion of the EXT/$\overline{OS}$ signal in chip decoding provides the distinguishing factor between internal and external memory spaces.

General CPU Operation

The core of the S83 is a Z80 CPU. It contains 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response. The Z80 also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register.

Figure 1 shows three groups of registers within the Z80 CPU. The first group consists of duplicate sets of 8-bit registers: a principal set and an alternate set (designated by ′ [prime], e.g., A′). Both sets consist of the Accumulator Register, the Flag Register, and six general-purpose registers. Transfer of data between these duplicate sets of registers is accomplished by use of "Exchange" instructions. The result is faster response to interrupts and easy, efficient implementation of such versatile programming techniques as background-foreground data processing. The second set of registers consists of six registers with assigned functions. These are the I (Interrupt Register), the R (Refresh Register), the IX and IY (Index Registers), the SP (Stack Pointer), and the PC (Program Counter). The third group consists of two interrupt status flip-flops, plus an additional pair of flip-flops which assists in identifying the interrupt mode at any particular time. Table 1 provides further information on these registers.

Figure 1. CPU Registers

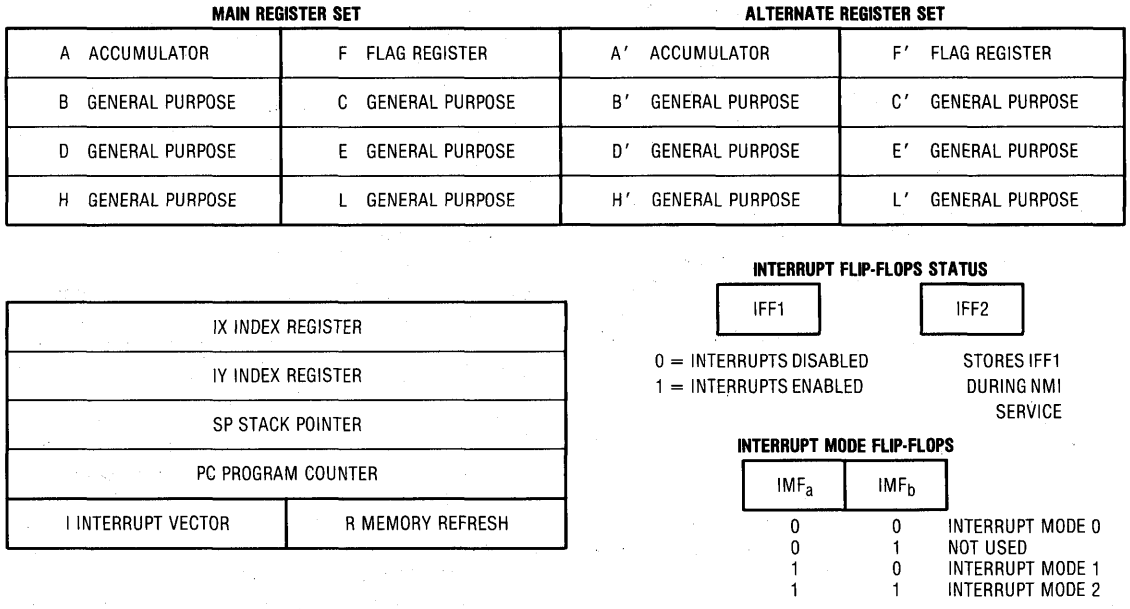


Table 1. Z80 CPU Registers

Register		Size (Bits)	Remarks
A, A'	Accumulator	8	Stores an operand or the results of an operation.
F, F'	Flags	8	See Instruction Set.
B, B'	General Purpose	8	Can be used separately or as a 16-bit register with C.
C, C'	General Purpose	8	See B, above.
D, D'	General Purpose	8	Can be used separately or as a 16-bit register with E.
E, E'	General Purpose	8	See D, above.
H, H'	General Purpose	8	Can be used separately or as a 16-bit register with L.
L, L'	General Purpose	8	See H, above.
			Note: The (B, C), (D, E), and (H, L) sets are combined as follows: B — High byte C — Low byte D — High byte E — Low byte H — High byte L — Low byte
I	Interrupt Register	8	Stores upper eight bits of memory address for vectored interrupt processing.
R	Refresh Register	8	Provides user-transparent dynamic memory refresh. Lower seven bits are automatically incremented and all eight are placed on the address bus during each instruction fetch cycle refresh time. The eighth bit appearing on the bus during a refresh cycle is incremented, but is *not readable or writable by the user.*
IX	Index Register	16	Used for indexed addressing.
IY	Index Register	16	Same as IX, above.
SP	Stack Pointer	16	Holds address of the top of the stack. See Push or Pop in instruction set.
PC	Program Counter	16	Holds address of next instruction.
IFF_1-IFF_2	Interrupt Enable	Flip-Flops	Set or reset to indicate interrupt status (see Figure 4).
IMF_a-IMF_b	Interrupt Mode	Flip-Flops	Reflect Interrupt mode (see Figure 4).

Interrupts: General Operation

The CPU accepts two interrupt input signals: $\overline{NMI}$ and $\overline{INT}$. The $\overline{NMI}$ is a non-maskable interrupt and has the highest priority. $\overline{INT}$ is a lower priority interrupt and it requires that interrupts be enabled in software in order to operate. $\overline{INT}$ can be connected to multiple peripheral devices in a wired-OR configuration.

The Z80 has a single response mode for interrupt service for the non-maskable interrupt. The maskable interrupt, $\overline{INT}$, has three programmable response modes available. These are:

- Mode 0 — similar to the 8080 microprocessor.
- Mode 1 — Peripheral Interrupt service, for use with non-8080/Z80 systems.
- Mode 2 — a vectored interrupt scheme, usually daisy-chained, for use with Z80 Family and compatible peripheral devices.

The CPU services interrupts by sampling the $\overline{NMI}$ and $\overline{INT}$ signals at the rising edge of the last clock of an instruction. Further interrupt service processing depends upon the type of interrupt that was detected. Details on interrupt responses are shown in the CPU Timing Section.

Non-Maskable Interrupt (NMI). The non-maskable interrupt cannot be disabled by program control and therefore will be accepted at all times by the CPU. $\overline{NMI}$ is usually reserved for servicing only the highest priority type interrupts, such as that for orderly shutdown after power failure has been detected. After recognition of the $\overline{NMI}$ signal (providing $\overline{BUSREQ}$ is not active), the CPU jumps to restart location 0066H. Normally, software starting at this address contains the interrupt service routine. $\overline{NMI}$ is negative edge triggered and need not be low at the time interrupts are sampled (see Pin Descriptions).

Maskable Interrupt ($\overline{INT}$). Regardless of the interrupt mode set by the user, the Z80 response to a maskable interrupt input follows a common timing cycle. After the interrupt has been detected by the CPU (provided that interrupts are enabled and $\overline{BUSREQ}$ is not active) a special interrupt processing cycle begins. This is a special fetch ($\overline{M1}$) cycle in which $\overline{IORQ}$ becomes active rather than $\overline{MREQ}$, as in normal $\overline{M1}$ cycle. In addition, this special $\overline{M1}$ cycle is automatically extended by two $\overline{WAIT}$ states, to allow for the time required to acknowledge the interrupt request.

Mode 0 Interrupt Operation. This mode is similar to the 8080 microprocessor interrupt service procedures. The interrupting device places an instruction on the data bus. This is normally a Restart (RST) instruction, which will initiate a call to the selected one of eight restart locations in page zero of memory. Unlike the 8080, the Z80 CPU responds to the Call instruction with only one interrupt acknowledge cycle followed by two memory read cycles.

Mode 1 Interrupt Operation. Mode 1 operation is very similar to that for the $\overline{NMI}$. The principal difference is that the Mode 1 interrupt has a restart location of 0038H only.

Mode 2 Interrupt Operation. This interrupt mode has been designed to utilize most effectively the capabilities of the Z80 microprocessor and its associated peripheral family. The interrupting peripheral device selects the starting address of the interrupt service routine. It does this by placing an 8-bit vector on the data bus during the interrupt acknowledge cycle. The CPU forms a pointer using this byte as the lower 8-bits and the contents of the I register as the upper 8 bits. This points to an entry in a table of addresses for interrupt service routines. The CPU then jumps to the routine at that address. This flexibility in selecting the interrupt service routine address allows the peripheral device to use several different types of sevice routines. These routines may be located at any available location in memory. Since the interrupting device supplies the low-order byte of the 2-byte vector, bit 0 (A_0) should be a zero.

Interrupt Priority (Daisy Chaining and Nested Interrupts). The interrupt priority of each peripheral device is determined by its physical location within a daisy-chain configuration. Each device in the chain has an interrupt enable input line (IEI) and an interrupt enable output line (IEO), which is fed to the next lower priority device. The first device in the daisy chain has its IEI input hardwired to a High level. The first device has highest priority, while each succeeding device has a corresponding lower priority. This arrangement permits the CPU to select the highest priority interrupt from several simultaneously interrupting peripherals.

The interrupting device disables the IEO line to the next lower priority peripheral until it has been serviced. After servicing, its IEO line is raised, allowing lower priority peripherals to demand interrupt servicing.

The Z80 CPU will nest (queue) any pending interrupts or interrupts received while a selected peripheral is being serviced.

Interrupt Enable/Disable Operation. Two flip-flops, IFF_1 and IFF_2, referred to in the register description are used to signal the CPU interrupt status. Operation of the two flip-flops is described in Table 2. For more details, refer to the Z80 CPU Technical Manual and Z80 Assembly Language Manual (available from Zilog, Inc.).

Table 2. State of Flip-Flops

Action	IFF_1	IFF_2	Comments
CPU Reset	0	0	Maskable interrupt INT disabled
DI instruction	0	0	Maskable interrupt INT disabled
EI instruction execution	1	1	Maskable interrupt INT enabled
LD A,I instruction execution	•	•	IFF_2 → Parity flag
LD A,R instruction execution	•	•	IFF_2 → Parity flag
Accept NMI	0	IFF_2	IFF_2 does not change (Maskable interrupt INT disabled)
RETN instruction execution	IFF_2	•	IFF_2 → IFF_1 at completion of an NMI service routine.

Instruction Set

The Z80 microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the Z80 instruction set and shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. The Z80 CPU Technical Manual (03-0029-01) and Assembly Language Programming Manual (03-0002-01) contain significantly more details for programming use (available from Zilog, Inc.).

The instructions are divided into the following categories.

- ☐ 8-bit loads
- ☐ 16-bit loads
- ☐ Exchange, block transfers, and searches
- ☐ 8-bit arithmetic and logic operations
- ☐ General-purpose arithmetic and CPU control
- ☐ 16-bit arithmetic operations
- ☐ Rotates and shifts
- ☐ Bit set, reset, and test operations
- ☐ Jumps
- ☐ Calls, returns, and restarts
- ☐ Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- ☐ Immediate
- ☐ Immediate extended
- ☐ Modified page zero
- ☐ Relative
- ☐ Extended
- ☐ Indexed
- ☐ Register
- ☐ Register indirect
- ☐ Implied
- ☐ Bit

8-Bit Load Group

Mnemonic	Symbolic Operation	Flags S	Z	H	P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD r, r′	r ← r′	•	•	X	X	•	•	01	r	r′		1	1	4	r, r′ Reg.
LD r, n	r ← n	•	•	X	X	•	•	00	r′	110		2	2	7	000 B
									← n →						001 C
LD r, (HL)	r ← (HL)	•	•	X	X	•	•	01	r	110		1	2	7	010 D
LD r, (IX + d)	r ← (IX + d)	•	•	X	X	•	•	11	011	101	DD	3	5	19	011 E
								01	r	101					100 H
									← d →						101 L
LD r, (IY + d)	r ← (IY + d)	•	•	X	X	•	•	11	111	101	FD	3	5	19	111 A
								01	r	110					
									← d →						
LD (HL), r	(HL) ← r	•	•	X	X	•	•	01	110	r		1	2	7	
LD (IX + d), r	(IX + d) ← r	•	•	X	X	•	•	11	011	101	DD	3	5	19	
								01	110	r					
									← d →						
LD (IY + d), r	(IY + d) ← r	•	•	X	X	•	•	11	111	101	FD	3	5	19	
								01	110	r					
									← d →						

8-Bit Load Group (continued)

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD (HL), n	(HL) ← n	•	•	X	•	X	•	•	•	00 110 110 ← n →	36	2	3	10	
LD (IX + d), n	(IX + d) ← n	•	•	X	•	X	•	•	•	11 011 101 00 110 110 ← d → ← n →	DD 36	4	5	19	
LD (IY + d), n	(IY + d) ← n	•	•	X	•	X	•	•	•	11 111 101 00 110 110 ← d → ← n →	FD 36	4	5	19	
LD A, (BC)	A ← (BC)	•	•	X	•	X	•	•	•	00 001 010	0A	1	2	7	
LD A, (DE)	A ← (DE)	•	•	X	•	X	•	•	•	00 011 010	1A	1	2	7	
LD A, (nn)	A ← (nn)	•	•	X	•	X	•	•	•	00 111 010 ← n → ← n →	3A	3	4	13	
LD (BC), A	(BC) ← A	•	•	X	•	X	•	•	•	00 000 010	02	1	2	7	
LD (DE), A	(DE) ← A	•	•	X	•	X	•	•	•	00 010 010	12	1	2	7	
LD (nn), A	(nn) ← A	•	•	X	•	X	•	•	•	00 110 010 ← n → ← n →	32	3	4	13	
LD A, I	A ← I	‡	‡	X	0	X	IFF	0	•	11 101 101 01 010 111	ED 57	2	3	9	
LD A, R	A ← R	‡	‡	X	0	X	IFF	0	•	11 101 101 01 011 111	ED 5F	2	2	9	
LD I, A	I ← A	•	•	X	•	X	•	•	•	11 101 101 01 000 111	ED 47	2	2	9	
LD R, A	R ← A	•	•	X	•	X	•	•	•	11 101 101 01 001 111	ED 4F	2	2	9	

NOTES: r, r' means any of the registers A, B, C, D, E, H, L
IFF the content of the interrupt enable flip-flop, (IFF) is copied into the P/V flag.

16-Bit Load Group

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd, nn	dd ← nn	•	•	X	•	X	•	•	•	00 dd0 001 ← n → ← n →		3	3	10	dd Pair 00 BC 01 DE 10 HL 11 SP
LD IX, nn	IX ← nn	•	•	X	•	X	•	•	•	11 011 101 00 100 001 ← n → ← n →	DD 21	4	4	14	
LD IY, nn	IY ← nn	•	•	X	•	X	•	•	•	11 111 101 00 100 001 ← n → ← n →	FD 21	4	4	14	
LD HL, (nn)	H ← (nn + 1) L ← (nn)	•	•	X	•	X	•	•	•	00 101 010 ← n → ← n →	2A	3	5	16	
LD dd, (nn)	dd_H ← (nn + 1) dd_L ← (nn)	•	•	X	•	X	•	•	•	11 101 101 01 dd1 011 ← n → ← n →	ED	4	6	20	
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	•	•	X	•	X	•	•	•	11 011 101 00 101 010 ← n → ← n →	DD 2A	4	6	20	
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	•	•	X	•	X	•	•	•	11 111 101 00 101 010 ← n → ← n →	FD 2A	4	6	20	
LD (nn), HL	(nn + 1) ← H (nn) ← L	•	•	X	•	X	•	•	•	00 100 010 ← n → ← n →	22	3	5	16	
LD (nn), dd	(nn + 1) ← dd_H (nn) ← dd_L	•	•	X	•	X	•	•	•	11 101 101 01 dd0 011 ← n → ← n →	ED	4	6	20	

S80 FAMILY

16-Bit Load Group (continued)

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD (nn), IX	$(nn+1) \leftarrow IX_H$ $(nn) \leftarrow IX_L$	•	•	X	•	X	•	•	•	11 00 ← n → ← n →	011	101 010	DD 22	4	6	20	
LD (nn), IY	$(nn+1) \leftarrow IY_H$ $(nn) \leftarrow IY_L$	•	•	X	•	X	•	•	•	11 00 ← n → ← n →	111	101 010	FD 22	4	6	20	
LD SP, HL	$SP \leftarrow HL$	•	•	X	•	X	•	•	•	11	111	001	F9	1	1	6	
LD SP, IX	$SP \leftarrow IX$	•	•	X	•	X	•	•	•	11 11	011 111	101 001	DD F9	2	2	10	
LD SP, IY	$SP \leftarrow IY$	•	•	X	•	X	•	•	•	11 11	111 111	101 001	FD F9	2	2	10	
$PUSH_{qq}$	$(SP-2) \leftarrow qq_L$ $(SP-1) \leftarrow qq_H$ $SP \rightarrow SP-2$	•	•	X	•	X	•	•	•	11	qq0	101		1	3	11	qq Pair 00 BC 01 DE 10 HL 11 AF
PUSH IX	$(SP-2) \leftarrow IX_L$ $(SP-1) \leftarrow IX_H$ $SP \rightarrow SP-2$	•	•	X	•	X	•	•	•	11 11	011 100	101 101	DD E5	2	4	15	
PUSH IY	$(SP-2) \leftarrow IY_L$ $(SP-1) \leftarrow IY_H$ $SP \rightarrow SP-2$	•	•	X	•	X	•	•	•	11 11	111 100	101 101	FD E5	2	4	15	
POP qq	$qq_H \leftarrow (SP+1)$ $qq_L \leftarrow (SP)$ $SP \rightarrow SP+2$	•	•	X	•	X	•	•	•	11	qq0	001		1	3	10	
POP IX	$IX_H \leftarrow (SP+1)$ $IX_L \leftarrow (SP)$ $SP \rightarrow SP+2$	•	•	X	•	X	•	•	•	11 11	011 100	101 001	DD E1	2	4	14	
POP IY	$IY_H \leftarrow (SP+1)$ $IY_L \leftarrow (SP)$ $SP \rightarrow SP+2$	•	•	X	•	X	•	•	•	11 11	111 100	101 001	FD E1	2	4	14	

NOTES: dd is any of the register pairs BC, DE, HL, SP.
qq is any of the register pairs AF, BC, DE, HL.
$(PAIR)_H$, $(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively, e.g., $BC_L = C$, $AF_H = A$.

Exchange, Block Transfer, Block Search Groups

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	$DE \leftrightarrow HL$	•	•	X	•	X	•	•	•	11	101	011	EB	1	1	4	
EX AF, AF'	$AF \leftrightarrow AF'$	•	•	X	•	X	•	•	•	00	001	000	08	1	1	4	
EXX	$BC \leftrightarrow BC'$ $DE \leftrightarrow DE'$ $HL \leftrightarrow HL'$	•	•	X	•	X	•	•	•	11	011	001	D9	1	1	4	Register band and auxiliary register bank exchange
EX (SP), HL	$H \leftrightarrow (SP+1)$ $L \leftrightarrow (SP)$	•	•	X	•	X	•	•	•	11	100	011	E3	1	5	19	
EX (SP), IX	$IX_H \leftrightarrow (SP+1)$ $IX_L \leftrightarrow (SP)$	•	•	X	•	X	•	•	•	11 11	011 100	101 011	DD E3	2	6	23	
EX (SP), IY	$IY_H \leftrightarrow (SP+1)$ $IY_L \leftrightarrow (SP)$	•	•	X	•	X	•	•	•	11 11	111 100	101 011	FD E3	2	6	23	
LDI	$(DE) \leftarrow (HL)$ $DE \leftarrow DE+1$ $HL \leftarrow HL+1$ $BC \leftarrow BC-1$	•	•	X	0	X	① 1	0	•	11 10	101 100	101 000	ED A0	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)
LDIR	$(DE) \leftarrow (HL)$ $DE \leftarrow DE+1$ $DE \leftarrow DE+1$ $HL \leftarrow HL+1$ $BC \leftarrow BC-1$ Repeat until $BC = 0$	•	•	X	0	X	② 0	0	•	11 10	101 110	101 000	ED B0	2 2	5 4	21 26	If $BC \neq 0$ If $BC = 0$
LDD	$(DE) \leftarrow (HL)$ $DE \leftarrow DE-1$	•	•	X	0	X	① 1	0	•	11 10	101 101	101 000	ED A8	2	4	16	

NOTE: 1 P/V flag is 0 if the result of $BC-1 = 0$, otherwise P/V = 1.
2 P/V flag is 0 at completion of instruction.

Exchange, Block Transfer, Block Search Groups (continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LDD (cont)	HL ← HL − 1 BC ← BC − 1				②								
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 Repeat until BC = 0	•	•	X	0	X	0	0	•	11 101 101 10 111 000	ED B8	2 2	5 4	21 16	If BC ≠ 0 If BC = 0
			③		①										
CPI	A − (HL) HL ← HL + 1 BC ← BC − 1	‡	‡	X	‡	X	‡	1	•	11 101 101 10 100 001	ED A1	2	4	16	
			③		①										
CPIR	A − (HL) HL ← HL + 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	‡	‡	X	‡	X	‡	1	•	11 101 101 10 110 001	ED B1	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
			③		①										
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	‡	‡	X	‡	X	‡	1	•	11 101 101 10 101 001	ED A9	2	4	16	
			③		①										
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	‡	‡	X	‡	X	‡	1	•	11 101 101 10 111 001	ED B9	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)

NOTES: 1 P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1.
2 P/V flag is 0 at completion of instruction only.
3 Z flag is 1 if A = (HL), otherwise Z = 0.

8-Bit Arithmetic and Logical Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A, r	A ← A + r	‡	‡	X	‡	X	V	0	‡	10 [000] r		1	1	4	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
ADD A, n	A ← A + n	‡	‡	X	‡	X	V	0	‡	11 [000] 110 ← n →		2	2	7	
ADD A, (HL)	A ← A + (HL)	‡	‡	X	‡	X	V	0	‡	10 [000] 110		1	2	7	
ADD A,(IX + d)	A ← A + (IX + d)	‡	‡	X	‡	X	V	0	‡	11 011 101 10 [000] 110 ← d →	DD	3	5	19	
ADD A,(IY + d)	A ← A + (IY + d)	‡	‡	X	‡	X	V	0	‡	11 111 101 10 [000] 110 ← d →	FD	3	5	19	
ADC A, s	A ← A + s + CY	‡	‡	X	‡	X	V	0	‡	[001]					s is any of r, n, (HL), (IX + d), (IY + d) as shown for ADD instruction. The indicated bits replace the [000] in the ADD set above
SUB s	A ← A − s	‡	‡	X	‡	X	V	1	‡	[010]					
SBC A, s	A ← A − s − CY	‡	‡	X	‡	X	V	1	‡	[011]					
AND s	A ← A ∧ s	‡	‡	X	1	X	P	0	0	[100]					
OR s	A ← A ∨ s	‡	‡	X	0	X	P	0	0	[110]					
XOR s	A ← A ⊕ s	‡	‡	X	0	X	P	0	0	[101]					
CP s	A − s	‡	‡	X	‡	X	V	1	‡	[111]					
INC r	r ← r + 1	‡	‡	X	‡	X	V	0	•	00 r [100]		1	1	4	
INC (HL)	(HL) ← (HL) + 1	‡	‡	X	‡	X	V	0	•	00 110 [100]		1	3	11	
INC (IX + d)	(IX + d) − (IX + d) + 1	‡	‡	X	‡	X	V	0	•	11 011 101 00 110 [100] ← d →	DD	3	6	23	
INC (IY + d)	(IY + d) − (IY + d) + 1	‡	‡	X	‡	X	V	0	•	11 111 101 00 110 [100] ← d →	FD	3	6	23	

8-Bit Arithmetic and Logic Group (continued)

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
DEC m	m ← m − 1	‡	‡	X	‡	X	V	1	•			101					m is any of r, (HL), (IX + d), (IY + d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode.

General-Purpose Arithmetic and CPU Control Groups

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
DAA	Converts acc, content into packed BCD following add or subtract with packed BCD operands.	‡	‡	X	‡	X	P	•	‡	00	100	111	27	1	1	4	Decimal adjust accumulator.
CPL	A ← A	•	•	X	1	X	•	1	•	00	101	111	2F	1	1	4	Complement accumulator (one's complement)
NEG	A ← 0 − A	‡	‡	X	‡	X	V	1	‡	11 01	101 000	101 100	ED 44	2	2	8	Negate acc, (two's complement).
CCF	CY ← CY	•	•	X	X	X	•	0	‡	00	111	111	3F	1	1	4	Complement carry flag.
SCF	CY ← 1	•	•	X	0	X	•	0	1	00	110	111	37	1	1	4	Set carry flag.
NOP	No operation	•	•	X	•	X	•	•	•	00	000	000	00	1	1	4	
HALT	CPU halted	•	•	X	•	X	•	•	•	01	110	110	76	1	1	4	
DI *	IFF ← 0	•	•	X	•	X	•	•	•	11	110	011	F3	1	1	4	
EI *	IFF ← 1	•	•	X	•	X	•	•	•	11	111	011	FB	1	1	4	
IM 0	Set interrupt mode 0	•	•	X	•	X	•	•	•	11 01	101 000	101 110	ED 46	2	2	8	
IM 1	Set interrupt mode 1	•	•	X	•	X	•	•	•	11 01	101 010	101 110	ED 56	2	2	8	
IM 2	Set interrupt mode 2	•	•	X	•	X	•	•	•	11 01	101 011	101 110	ED SE	2	2	8	

NOTES: IFF indicates the interrupt enable flip-flop.
CY indicates the carry flip-flop.
* indicates interrupts are not sampled at the end of EI or DI.

16-Bit Arithmetic Group

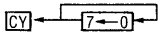
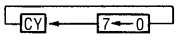
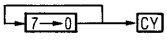
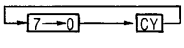
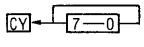
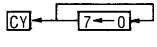
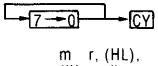
Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD HL, ss	HL ← HL + ss	•	•	X	X	X	•	0	‡	00	ss1	001		1	3	11	ss Reg. 00 BC
ADC HL, ss	HL ← HL + ss + CY	‡	‡	X	X	X	V	0	‡	11 01	101 ss1	101 010	ED	2	4	15	01 DE 10 HL 11 SP
SBC HL, ss	HL ← HL − ss − CY	‡	‡	X	X	X	V	1	‡	11 01	101 ss0	101 010	ED	2	4	15	
ADD IX, pp	IX ← IX + pp	•	•	X	X	X	•	0	‡	11 01	011 pp1	101 001	DD	2	4	15	pp Reg. 00 BC 01 DE 10 IX 11 SP
ADD IY, rr	IY ← IY + rr	•	•	X	X	X	•	0	‡	11 00	111 rr1	101 001	FD	2	4	15	rr Reg. 00 BC 01 DE 10 IY 11 SP
INC ss	ss ← ss + 1	•	•	X	•	X	•	•	•	00	ss0	011		1	1	6	
INC IX	IX ← IX + 1	•	•	X	•	X	•	•	•	11 00	011 100	101 011	DD 23	2	2	10	

16-Bit Arithmetic Group (continued)

Mnemonic	Symbolic Operation	S	Z		Flags H		P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
INC IY	IY ← IY + 1	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	10	
										00	100	011	23				
DEC ss	ss ← ss − 1	•	•	X	•	X	•	•	•	00	ss1	011		1	1	6	
DEX IX	IX ← IX − 1	•	•	X	•	X	•	•	•	11	011	101	DD	2	2	10	
										00	101	011	2B				
DEC IY	IY ← IY − 1	•	•	X	•	X	•	•	•	11	111	101	FD	2	2	10	
										00	101	011	2B				

NOTES: ss is any of the register pairs BC, DE, HL, SP.
pp is any of the register pairs BC, DE, IX, SP.
rr is any of the register pairs BC, DE, IY, SP.

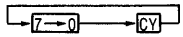
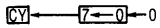
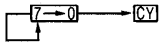
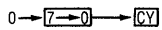
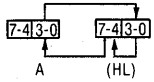
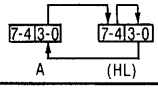
Rotate and Shift Group

Mnemonic	Symbolic Operation	S	Z		Flags H		P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA	 A	•	•	X	0	X	•	0	‡	00	000	111	07	1	1	4	Rotate left circular accumulator.
RLA	 A	•	•	X	0	X	•	0	‡	00	010	111	17	1	1	4	Rotate left accumulator.
RRCA	 A	•	•	X	0	X	•	0	‡	00	000	111	07	1	1	4	Rotate left circular accumulator.
RRA	 A	•	•	X	0	X	•	0	‡	00	011	111	1F	1	1	4	Rotate left accumulator.
RLCr		‡	‡	X	0	X	P	0	‡	11	001	011	CB	2	2	8	Rotate left circular register r.
										00	000	r					
RLC (HL)		‡	‡	X	0	X	P	0	‡	11	001	011	CB	2	4	15	
										00	000	110					
RLC(IX + d)	 r, (HL), (IX + d), (IY + d)	‡	‡	X	0	X	P	0	‡	11	011	101	DD	4	6	23	
										11	001	011	CB				
										← d →							
										00	000	110					
RLC (IY + d)		‡	‡	X	0	X	P	0	‡	11	111	101	FD	4	6	23	
										11	001	011	CB				
										← d →							
										00	000	110					
RL m	 m r, (HL), (IX + d), (IY + d)	‡	‡	X	0	X	P	0	‡		010						Instruction format and states are as shown for RLC's. To form new opcode replace 000 of RLC's with shown code.
RRC m	 m r, (HL), (IX + d), (IY + d)	‡	‡	X	0	X	P	0	‡		001						

r	Reg.
000	B
001	C
010	D
011	E
100	H
101	L
111	A

S80 FAMILY

Rotate and Shift Group (continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RR m	 m r, (HL), (IX + d), (IY + d)	‡	‡	X	0	X	P	0	‡		011				
SLA m	 m r, (HL), (IX + d), (IY + d)	‡	‡	X	0	X	P	0	‡		100				
SRA m	 m r, (HL), (IX + d), (IY + d)	‡	‡	X	0	X	P	0	‡		101				
SRL m	 m r, (HL), (IX + d), (IY + d)	‡	‡	X	0	X	P	0	‡		111				
RLD		‡	‡	X	0	X	P	0	•	11 01	101 101	101 111	ED 6F	2	5	18	Rotate digit left and right between the accumulator and location (HL). The content of the upper half of the accumulator is unaffected.
RRD		‡	‡	X	0	X	P	0	•	11 01	101 100	101 111	ED 67	2	5	18	

Bit Set, Reset and Test Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
Bit b,r	$Z \leftarrow r_b$	X	‡	1	X	X	0	•	11 01	001 b	011 r	CB	2	2	8	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A b Bit Tested 000 0 001 1 010 2 011 3 100 4 101 5 110 6 111 7
BIT b, (HL)	$Z \leftarrow \overline{(HL)_b}$	X	‡	1	X	X	0	•	11 01	001 b	011 110	CB	2	3	12	
BIT b,(IX+d)$_b$	$Z \leftarrow \overline{(IX+d)_b}$	X	‡	1	X	X	0	•	11 11 01	011 001 b	101 011 110	DD CB	4	5	20	
BIT b,(IY+d)$_b$	$Z \leftarrow \overline{(IY+d)_b}$	X	‡	1	X	X	0	•	11 11 01	111 001 b	101 011 110	FD CB	4	5	20	
SET b, r	$r_b \rightarrow 1$	•	•	X	•	X	•	•	•	11 11	001 b	011 r	CB	2	2	8	
SET b, (HL)	$(HL)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 11	001 b	011 110	CB	2	4	15	

Bit Set, Reset and Test Group (continued)

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
SET b, (IX + d)	$(IX + d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 011 101 11 001 011 ← d → 11 b 110	DD CB	4	6	23	
SET b,(IY + d)	$(IY + d)_b \leftarrow 1$	•	•	X	•	X	•	•	•	11 111 101 11 001 011 ← d → 11 b 110	FD CB	4	6	23	
RES b, m	$m_b \leftarrow 0$ m r, (HL), (IX + d), (IY + d)	•	•	X	•	X	•	•	•	10					To form new opcode replace 11 of SET b, s with 10 Flags and time states for SET instruction.

NOTES: The notation m_b indicates bit b (0 to 7) or location m.

Jump Group

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP nn	PC ← nn	•	•	X	•	X	•	•	•	11 000 011 ← n → ← n →	C3	3	3	10	
JP cc, nn	If condition cc is true PC ← nn, otherwise continue	•	•	X	•	X	•	•	•	11 cc 010 ← n → ← n →		3	3	10	cc Condition 000 NZ non-zero 001 A zero 010 NC non-carry 011 C carry 100 PO parity odd 101 PE parity even 110 P sign positive 111 M sign negative
JR e	PC ← PC + e	•	•	X	•	X	•	•	•	00 011 000 ← e − 2 →	18	2	3	12	
JR C, e	If C = 0, continue	•	•	X	•	X	•	•	•	00 111 000 ← e − 2 →	38	2	2	7	If condition not met.
	If C = 1, PC ← PC + e											2	3	12	If condition is met.
JR NC, e	If C = 1, continue	•	•	X	•	X	•	•	•	00 110 000 ← e − 2 →	30	2	2	7	If condition not met.
	If C = 0, PC ← PC + e											2	3	12	If condition is met.
JP Z, e	If Z = 0, continue	•	•	X	•	X	•	•	•	00 101 000 ← e − 2 →	28	2	2	7	If condition not met.
	If Z = 1, PC ← PC + e											2	3	12	If condition is met.
JR NZ, e	If Z = 1, continue	•	•	X	•	X	•	•	•	00 100 000 ← e − 2 →	20	2	2	7	If condition not met.
	If Z = 0, PC ← PC + e											2	3	12	If condition is met.
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	11 101 001	E9	1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	11 011 101 11 101 001	DD E9	2	2	8	
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11 111 101 11 101 001	FD E9	2	2	8	
DJNZ, e	B ← B − 1 If B = 0. continue.	•	•	X	•	X	•	•	•	00 010 000 ← e − 2 →	10	2	2	8	If B = 0.
	If B ≠ 0, PC ← PC + e											2	3	13	If B ≠ 0.

NOTES: e represents the extension in the relative addressing mode.
e is a signed two's complement number in the range < −126, 129 >.
e − 2 in the opcode provides an effective address of pc + e as PC is incremented by two prior to the addition of e.

Call and Return Group

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	•	•	X	•	X	•	•	•	11 001 101 ← n → ← n →	CD	3	5	17	

Call and Return Group (continued)

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
CALL cc, nn	If condition cc is false continue, otherwise same as CALL nn	•	•	X	•	X	•	•	•	11	cc ← n → ← n →	100		3 3	3 5	10 17	If cc is false. If cc is true.
RET	$PC_L \leftarrow (SP)$ $PC_H \leftarrow (SP+1)$	•	•	X	•	X	•	•	•	11	001	001	C9	1	3	10	
RET cc	If condition cc is false continue, otherwise same as RET	•	•	X	•	X	•	•	•	11	cc	000		1 1	1 3	5 11	If cc is false. If cc is true.
RETI	Return from interrupt	•	•	X	•	X	•	•	•	11 01	101 001	101 101	ED 4D	2	4	14	
RETN[1]	Return from non-maskable interrupt	•	•	X	•	X	•	•	•	11 01	101 000	101 101	ED 45	2	4	14	
RST p	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$ $PC_H \leftarrow 0$ $PC_L \leftarrow p$	•	•	X	•	X	•	•	•	11	t	111		1	3	11	

cc	Condition
000	NZ non-zero
001	Z zero
010	NC non-carry
011	C carry
100	PO parity odd
101	PE parity even
110	P sign positive
111	M sign negative

t	p
000	00H
001	08H
010	10H
011	18H
100	20H
101	28H
110	30H
111	38H

NOTE: [1] RETN loads $IFF_2 \rightarrow IFF_1$

Input and Output Group

Mnemonic	Symbolic Operation	S	Z		H		P/V	N	C	76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
IN A, (n)	A ← (n)	•	•	X	•	X	•	•	•	11	011 ← n →	011	DB	2	3	11	n to $A_0 - A_7$ Acc. to $A_8 - A_{15}$
IN r, (C)	r ← (C) if r = 110 only the flags will be affected	‡	‡ ①	X	‡	X	P	0	•	11 01	101 r	101 000	ED	2	3	12	C to $A_0 - A_7$ B to $A_8 - A_{15}$
INI	(HL) ← (C) B ← B − 1 HL ← HL + 1	X	‡ ②	X	X	X	X	1	X	11 10	101 100	101 010	ED A2	2	4	16	C to $A_0 - A_7$ B to $A_8 - A_{15}$
INIR	(HL) ← (C) B ← B − 1 HL ← HL + 1 Repeat until B = 0	X	1	X	X	X	X	1	X	11 10	101 110	101 010	ED B2	2 2	5 (If B≠0) 4 (If B = 0)	21 16	C to $A_0 - A_7$ B to $A_8 - A_{15}$
IND	(HL) ← (C) B ← B − 1 HL ← HL − 1	X	‡ ① ②	X	X	X	X	1	X	11 10	101 101	101 010	ED AA	2	4	16	C to $A_0 - A_7$ B to $A_8 - A_{15}$
INDR	(HL) ← (C) B ← B − 1 HL ← HL − 1 Repeat until B = 0	X	1	X	X	X	X	1	X	11 10	101 111	101 010	ED BA	2 2	5 (If B≠0) 4 (If B = 0)	21 16	C to $A_0 - A_7$ B to $A_8 - A_{15}$
OUT (n), A	(n) ← A	•	•	X	•	X	•	•	•	11	010 ← n →	011	D3	2	3	11	n to $A_0 - A_7$ Acc. to $A_8 - A_{15}$
OUT (C), r	(C) ← r	•	•	X	•	X	•	•	•	11 01	101 r	101 001	ED	2	3	12	C to $A_0 - A_7$ B to $A_8 - A_{15}$
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	X	‡ ①	X	X	X	X	1	X	11 10	101 100	101 011	ED A3	2	4	16	C to $A_0 - A_7$ B to $A_8 - A_{15}$

Input and Output Group (continued)

Mnemonic	Symbolic Operation	Flags S	Z	H	P/V	N	C	Opcode 76	543	210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
			②												
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 Repeat until B = 0	X	1	X	X	X	X	1	X	11 10	101 110	101 011	ED B3	2 2	5 (If B≠0) 4 (If B = 0)	21 16	C to A_0 − A_7 B to A_8 − A_{15}
			①												
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	X	‡	X	X	X	X	1	X	11 10	101 101	101 011	ED AB	2	4	16	C to A_0 − A_7 B to A_8 − A_{15}
			②												
OTDR	(C) ↔ (HL) B ← B − 1 HL ← HL − 1 Repeat until B = 0	X	1	X	X	X	X	1	X	11 10	101 111	101 011	ED	2 2	5 (If B≠0) 4 (If B = 0)	21 16	C to A_0 − A_7 B to A_8 − A_{15}

NOTE: ① If the result of B − 1 is zero the Z flag is set, otherwise it is reset.
② Z flag is set upon instruction completion only.

Summary of Flag Operation

Instruction	D_7							D_0	Comments
ADD A, s; ADC A, s	‡	‡	X	‡	X	V	0	‡	8-bit add or add with carry.
SUB s; SBC A, s; CP s; NEG	‡	‡	X	‡	X	V	1	‡	8-bit subtract, subtract with carry, compare and negate accumulator.
AND s	‡	‡	X	1	X	P	0	0	Logical operations.
OR s, XOR s	‡	‡	X	0	X	P	0	0	
INC s	‡	‡	X	‡	X	V	0	•	8-bit increment.
DEC s	‡	‡	X	‡	X	V	1	•	8-bit decrement.
ADD DD, ss	•	•	X	X	X	•	0	‡	16-bit add.
ADC HL, ss	‡	‡	X	X	X	V	0	‡	16-bit add with carry.
SBC HL, ss	‡	‡	X	X	X	V	1	‡	16-bit subtract with carry.
RLA, RLCA, RRA; RRCA	•	•	X	0	X	•	0	‡	Rotate accumulator.
RL m; RLC m; RR m; RRC m; SLA m; SRA m; SRL m	‡	‡	X	0	X	P	0	‡	Rotate and shift locations.
RLD; RRD	‡	‡	X	0	X	P	0	•	Rotate digit left and right.
DAA	‡	‡	X	‡	X	P	•	‡	Decimal adjust accumulator.
CPL	•	•	X	1	X	•	1	•	Complement accumulator.
SCF	•	•	X	0	X	•	0	1	Set carry.
CCF	•	•	X	X	X	•	0	‡	Complement carry.
IN r (C)	‡	‡	X	0	X	P	0	•	Input register indirect.
INI, IND, OUTI; OUTD	X	‡	X	X	X	X	1	•	Block input and output. Z = 0 if B ≠ 0, otherwise Z = 0.
INIR; INDR; OTIR; OTDR	X	1	X	X	X	X	1	•	
LDI; LDD	X	X	X	0	X	‡	0	•	Block transfer instuctions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LDIR; LDDR	X	X	X	0	X	0	0	•	
CPI; CPIR; CPD; CPDR	X	‡	X	X	X	‡	1	•	Block search instructions. Z = 1 if A = (HL), otherwise Z = 0, P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LD A, I, LD A, R	‡	‡	X	0	X	IFF	0	•	The content of the interrupt enable flip-flop (IFF) is coupled into the P/V flag.
BIT b, s	X	‡	X	1	X	X	0	•	The state of bit b of location s is copied into the Z flag.

Symbolic Notation

Symbol	Operation
S	Sign flag. S = 1 if the MSB of the result is 1.
Z	Zero flag. Z = 1 if the result of the operation is 0.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V = 1 if the result of the operation is even, P/V = 0 if result is odd. If P/V holds overflow, P/V = 1 if the result of the operation produced an overflow.
H	Half-carry flag. H = 1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.
N	Add/Subtract flag. N = 1 if the previous operation was a subtract
H & N	H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.
C	Carry/link flag. C = 1 if the operation produced a carry from the MSB of the operand or result.

Symbol	Operation
‡	The flag is affected according to the result of the operation.
•	The flag is unchanged by the operation.
0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a "don't care."
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
if	Any one of the two index registers IX or IY.
R	Refresh counter.
n	8-bit value in range < 0, 255 >
nn	16-bit value in range < 0, 65535 >.

Pin Descriptions

Pin Name	Description
A_0-A_{15}	**ADDRESS BUS.** Tri-state output, active high.
D_0-D_7	**DATA BUS.** Tri-state input/output, active high.
$\overline{M1}$	**MACHINE CYCLE ONE.** Output, active low. Indicates current machine cycle is the OP code fetch cycle. $\overline{M1}$ together with $\overline{IORQ}$ indicates an interrupt acknowledge cycle.
$\overline{MREQ}$	**MEMORY REQUEST.** Tri-state input/output, active low. Indicates that the address bus holds a valid memory address for a memory read or write operation. Functions as an input only during Bus Request cycles for $\overline{RAS}$/$\overline{CAS}$ generation.
$\overline{IORQ}$	**INPUT/OUTPUT REQUEST.** Tri-state output, active low. Indicates that the lower half of the address bus holds a valid I/O address. Also generated with $\overline{M1}$ when an interrupt is being acknowledged to indicate that a response vector can be placed on the data bus.
$\overline{RD}$	**READ.** Tri-state output, active low. Indicates that the CPU wants to read data from memory or an I/O device. The addressed memory or I/O device should use this signal to gate data onto the CPU data bus.
$\overline{WR}$	**WRITE.** Tri-state output, active low. Indicates that CPU data bus holds valid data to be stored in memory or an I/O device.
$\overline{RFSH}$	**REFRESH.** Output, active low. $\overline{RFSH}$, together with $\overline{MREQ}$, indicates that the lower 8 bits of the address bus contain a refresh address for dynamic memories.
$\overline{HALT}$	**HALT STATE.** Output, active low. Indicates that the CPU has executed a software halt instruction and is awaiting either a non-maskable interrupt or a maskable interrupt (if enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.
$\overline{WAIT}$	**WAIT.** Input, active low. Indicates that the addressed memory or I/O devices are not ready for data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended $\overline{WAIT}$ periods can prevent the CPU from refreshing dynamic memory properly.
$\overline{INT}$	**INTERRUPT REQUEST.** Input, active low. Generated by I/O devices. Will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop is enabled, removing the interrupt mask. $\overline{INT}$ is normally wire-ORed and requires an external pullup for these applications.

Pin Descriptions (continued)

Pin Name	Description
$\overline{NMI}$	**NON-MASKABLE INTERRUPT.** Input negative edge triggered. Has higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction and cannot be masked by the interrupt enable flip-flop as with a normal interrupt. Automatically forces CPU to restart at location 0066H.
$\overline{RESET}$	**RESET.** Input, active low. Initializes CPU as follows: reset interrupt enable flip-flop, clear PC, clear registers I and R, and set interrupt to 8080A similar mode. During reset, the address and data bus go to a high impedance state and all control output signals go to the inactive state. The processor will be vectored to either address 0000H or address FF00H depending on the state of the EXT/$\overline{OS}$ input. Note that $\overline{RESET}$ must be active for a minimum of three full clock cycles before the reset operation is complete.
$\overline{BUSREQ}$	**BUS REQUEST.** Input, active low. Has higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle. Used to request that the CPU address bus, data bus, and $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ control signals to go to a high impedance state so that other devices can control these lines. BUSREQ is normally wire-ORed and requires an external pullup for these applications. Extended $\overline{BUSREQ}$ periods may cause refresh problems.
$\overline{BUSACK}$	**BUS ACKNOWLEDGE.** Output, active low. Indicates to the requesting device that the CPU address bus, data bus, and $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ control signals have been set to their high impedance state and the external device can control these signals.
$\overline{RAS}$	**ROW ADDRESS STROBE.** Output, active low. Indicates that the lower 8 bits of the CPU address bus contain a valid row address for dynamic RAMs providing the CPU has not been bus requested. Strobes row address into dynamic RAM address latch.
$\overline{CAS}$	**COLUMN ADDRESS STROBE.** Output, active low. Indicates that the lower 8 bits of the CPU address bus contain a valid column address for dynamic RAMs providing the CPU has not been bus requested. Strobes column address into dynamic RAM address latch.
$\overline{BUSSEL}$	**BUS SELECT.** Input, active low. Determines whether address bus will be multiplexed for dynamic RAMs. When active, addresses will not be multiplexed and $\overline{CAS}$ will not be generated for that particular memory cycle. In addition, an active low level on $\overline{BUSSEL}$ during an access to the internal ROM (as indicated by EXT/$\overline{OS}$) will cause the CPU to read data from the external data bus rather than from the internal ROM. $\overline{BUSSEL}$ also controls the generation of $\overline{CAS}$ during DMA cycles.
EXT/$\overline{OS}$	**EXTERNAL MODE SELECT.** Input/output. Determines whether processor comes up in the internal or external mode on the rising edge of reset. When high on reset, the internal ROM is disabled and the CPU performs a normal Z80 reset operation. When low on reset, the internal ROM is enabled and the CPU is vectored to ROM address FF00. After reset, this pin is an output indicating an access to the internal ROM address space with the ROM enable latch set.

System Timing

The S83 executes instructions by proceeding through a specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a T time or cycle, and three or more T cycles make up a machine cycle (M1, M2, or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more wait states by the user.

Instruction Op Code Fetch

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later $\overline{MREQ}$ goes active. $\overline{RD}$ when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T_3. Clock state T_3 and T_4 of a CPU is internally decoding and executing the instruction. The refresh control signal RFSH indicates that a refresh read of all dynamic memories is in progress.

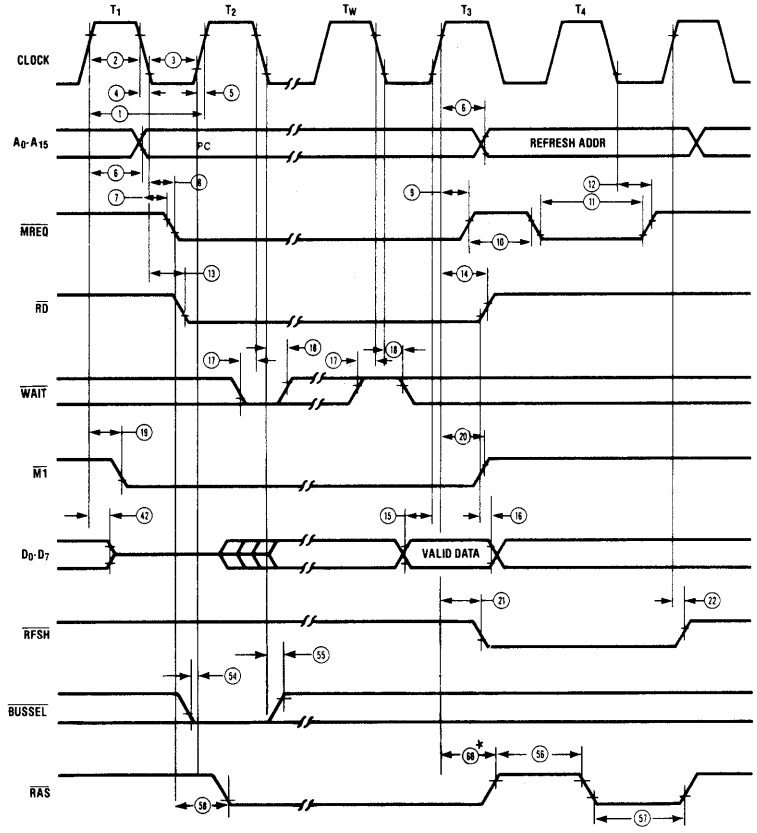
Figure 2a shows an opcode fetch in which $\overline{BUSSEL}$ is low. This cycle is no different from a standard Z80 CPU, except that a Row Address Strobe will be generated during both the opcode fetch and during the refresh operation.

Figure 2b shows an opcode fetch in which $\overline{BUSSEL}$ is high. In this case, the upper byte of the address bus will remain stable throughout the entire memory access cycle, however, the lower byte of the address bus is multiplexed for interfacing to dynamic RAMs. Initially, the low byte of the address bus will contain a row address, and $\overline{RAS}$ will be generated. The falling edge of $\overline{RAS}$ is used to strobe the row address into the dynamic RAMs. After the address multiplexers have switched, $\overline{CAS}$ is generated, and is used to strobe the column address into the dynamic RAMs.

One wait state is inserted automatically by the processor. Additional user wait states may be inserted, however $\overline{RAS}$ will go high on the third rising clock edge after $\overline{MREQ}$ goes low regardless of how many wait states are used. $\overline{CAS}$, however, will not go high until $\overline{MREQ}$ goes high at the end of the opcode fetch. In interfacing to dynamic RAMs, it is permissible for $\overline{RAS}$ to go high before $\overline{CAS}$ goes high so long as both signals are high before $\overline{RAS}$ goes low again.

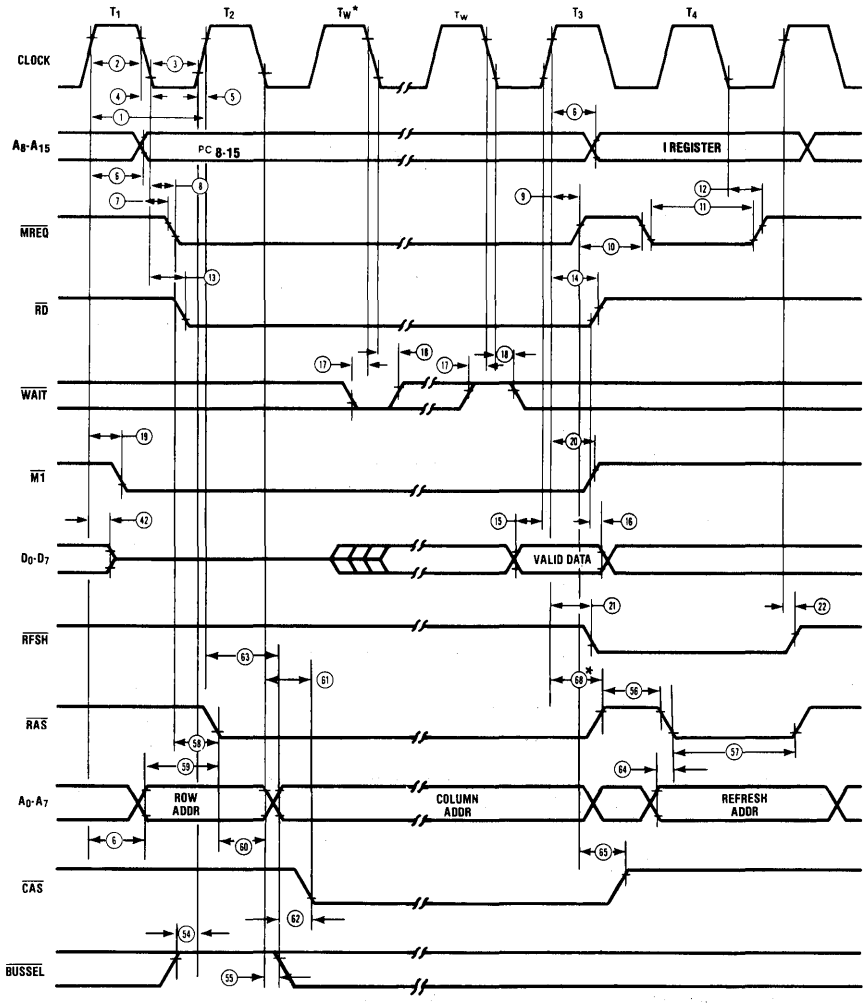
$\overline{BUSSEL}$ must remain stable from the rising edge of T_2 until after the rising edge of T_2. Decoding address lines to generate $\overline{BUSSEL}$ will fulfill this requirement. It is not necessary to include $\overline{MREQ}$ in the generation of $\overline{BUSSEL}$.

Figure 2a. Opcode Fetch (Non-Multiplexed)



*NOTE: $\overline{RAS}$ WILL GO HIGH ON THE THIRD RISING CLOCK EDGE AFTER $\overline{MREQ}$ GOES LOW. THIS MAY BE BEFORE T_3 IF ADDITIONAL WAIT STATES HAVE BEEN INSERTED.

Figure 2b. Opcode Fetch (Multiplexed)



NOTE: T_W^* = ONE WAIT STATE AUTOMATICALLY INSERTED BY CPU

*NOTE: $\overline{RAS}$ WILL GO HIGH ON THE THIRD RISING CLOCK EDGE AFTER $\overline{MREQ}$ GOES LOW. THIS MAY BE BEFORE T_3 IF ADDITIONAL WAIT STATES HAVE BEEN INSERTED.

Memory Read or Write Cycles

Illustrated here is the timing of memory read or write cycles other than an OP code fetch cycle ($\overline{M1}$ cycle). The $\overline{MREQ}$ and $\overline{RD}$ signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the $\overline{MREQ}$ also becomes active when the address bus is stable. The $\overline{WR}$ line is active when data on the data bus is stable so that it can be used directly as a R/$\overline{W}$ pulse to virtually any type of semiconductor memory.

Figure 3a illustrates a memory read or write where $\overline{BUSSEL}$ is low. This is the same as a standard Z80 memory read or write cycle, except that $\overline{RAS}$ goes low during the cycle, effectively performing a refresh read operation to any dynamic RAMs in the system.

Figure 3b illustrates a memory read or write where $\overline{BUSSEL}$ is high. The operating of the address multiplexing and the two address strobes, $\overline{RAS}$ and $\overline{CAS}$, is the same as for a multiplexed instruction opcode fetch, except that no automatic wait states are generated.

Figure 3a. Memory Read/Write (Non-Multiplexed)

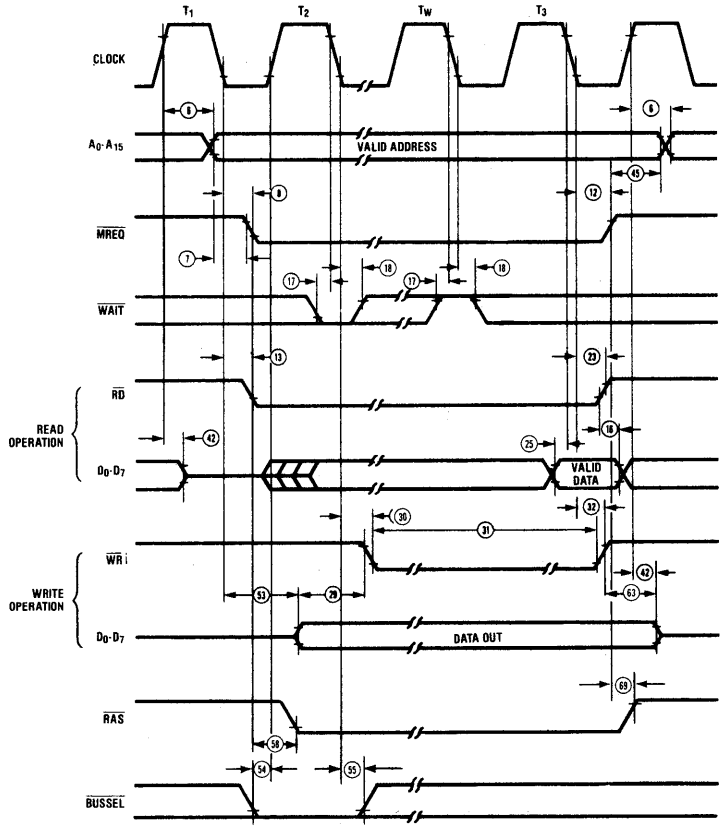
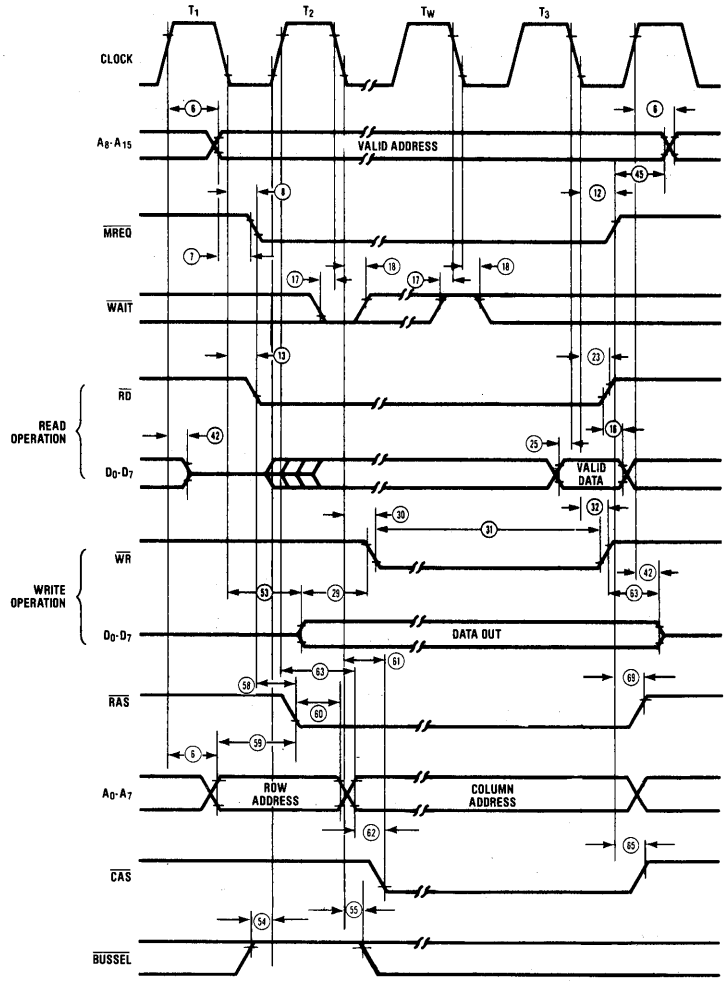


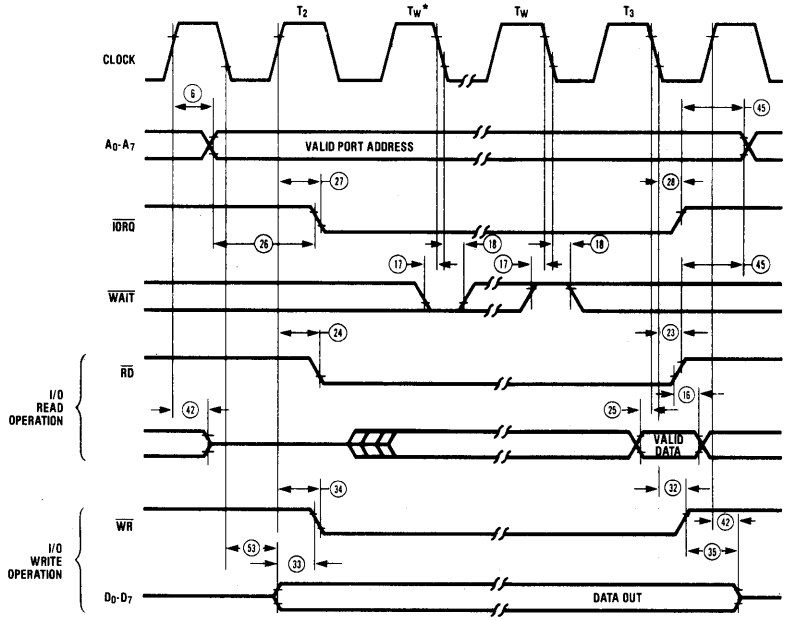
Figure 3b. Memory Read/Write (Multiplexed)



Input or Output Cycles

Figure 4 illustrates the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this allows sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required.

Figure 4. Input or Output Cycles



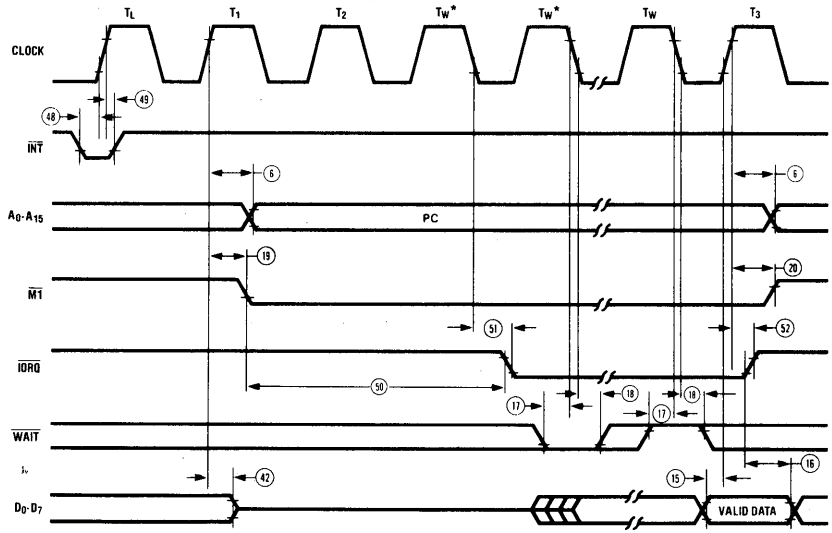
NOTE: T_W^* = ONE WAIT CYCLE AUTOMATICALLY INSERTED BY CPU.

NOTE: T_W^* = ONE WAIT CYCLE AUTOMATICALLY INSERTED BY CPU.

Interrupt Request/Acknowledge Cycle

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special $\overline{M1}$ cycle is generated. During this $\overline{M1}$ cycle, the $\overline{IORQ}$ signal becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the Z80 peripheral controllers, can be easily implemented (Figure 5).

Figure 5. Interrupt Request/Acknowledge Cycle

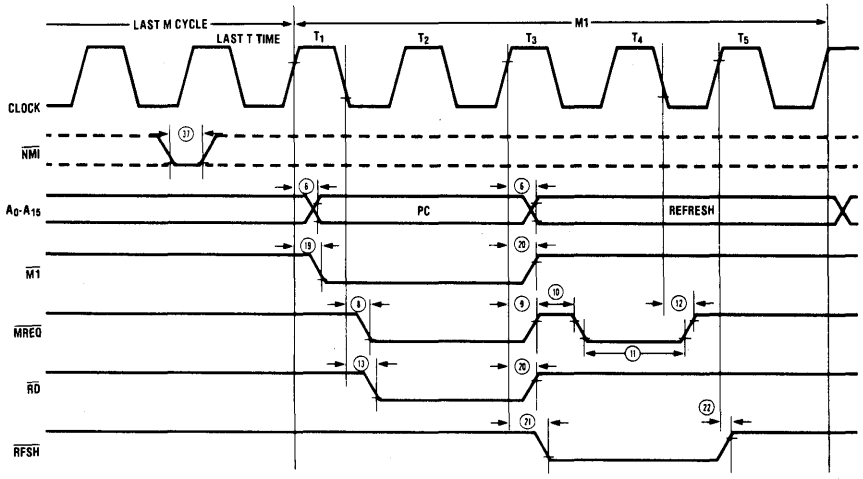


NOTE: 1) T_L = LAST STATE OF PREVIOUS INSTRUCTION.
2) TWO WAIT CYCLES AUTOMATICALLY INSERTED BY CPU(*).

Non-Maskable Interrupt Request Cycle

$\overline{NMI}$ is sampled at the same time as the maskable interrupt input $\overline{INT}$ but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal instruction fetch except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) address 0066H (Figure 6). The $\overline{RAS}$, $\overline{CAS}$ and address multiplexing functions operate the same as for a regular instruction opcode fetch, including the disabling of address multiplexing and $\overline{CAS}$ with $\overline{BUSSEL}$. Refer to the opcode fetch timing diagram for further timing information on these signals.

Figure 6. Non-Maskable Interrupt Request Operation



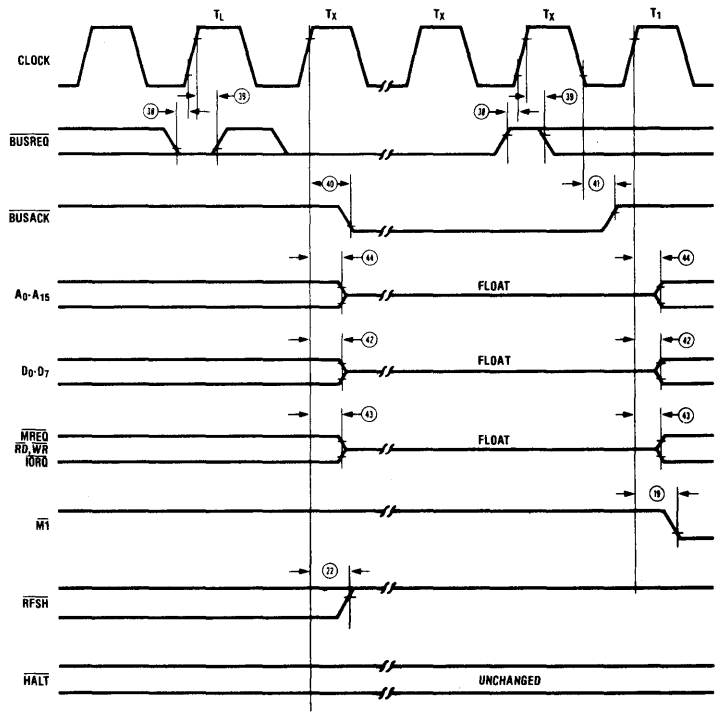
* ALTHOUGH NMI IS AN ASYNCHRONOUS INPUT, TO GUARANTEE ITS BEING RECOGNIZED ON THE FOLLOWING MACHINE CYCLE, NMI'S FALLING EDGE MUST OCCUR NO LATER THAN THE RISING EDGE OF THE CLOCK CYCLE PRECEDING T_{LAST}.

NOTE: $\overline{RAS}$, $\overline{CAS}$, AND ADDRESS MULTIPLEXING FUNCTION AS FOR NORMAL OPCODE FETCH DEPENDING ON THE STATE OF $\overline{BUSSEL}$.

Bus Request Acknowledge Cycle

The CPU samples $\overline{BUSREQ}$ with the rising edge of the last clock period of any machine cycle (Figure 7). If $\overline{BUSREQ}$ is active, the CPU sets its address, data, and $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ lines to a high-impedance state with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices. While an external device has control of the bus, address multiplexing is inhibited, however the ROM select logic for the internal ROM and the $\overline{RAS}/\overline{CAS}$ generation logic is functional. $\overline{BUSSEL}$ is still sampled, and will enable/disable the generation of $\overline{CAS}$. Using these features, a DMA device may access the internal ROM, switch it on or off, and may use the S83 internal logic to generate $\overline{RAS}$ and $\overline{CAS}$, however address multiplexing must be done external to the S83.

Figure 7. BUS Request/Acknowledge Cycle

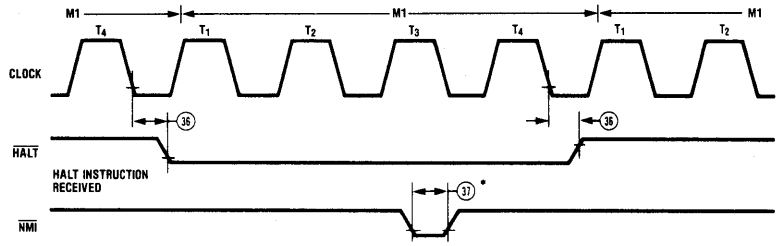


NOTE: T_L = LAST STATE OF ANY M CYCLE.
T_X = AN ARBITRARY CLOCK CYCLE USED BY REQUESTING DEVICE.

Halt Acknowledge Cycle

When the CPU receives a Halt instruction, it executes NOP states until either an $\overline{INT}$ or $\overline{NMI}$ input is received. When in the Halt state, the $\overline{HALT}$ output is active and remains so until an interrupt is received (Figure 8).

Figure 8. Halt Acknowledge Cycle



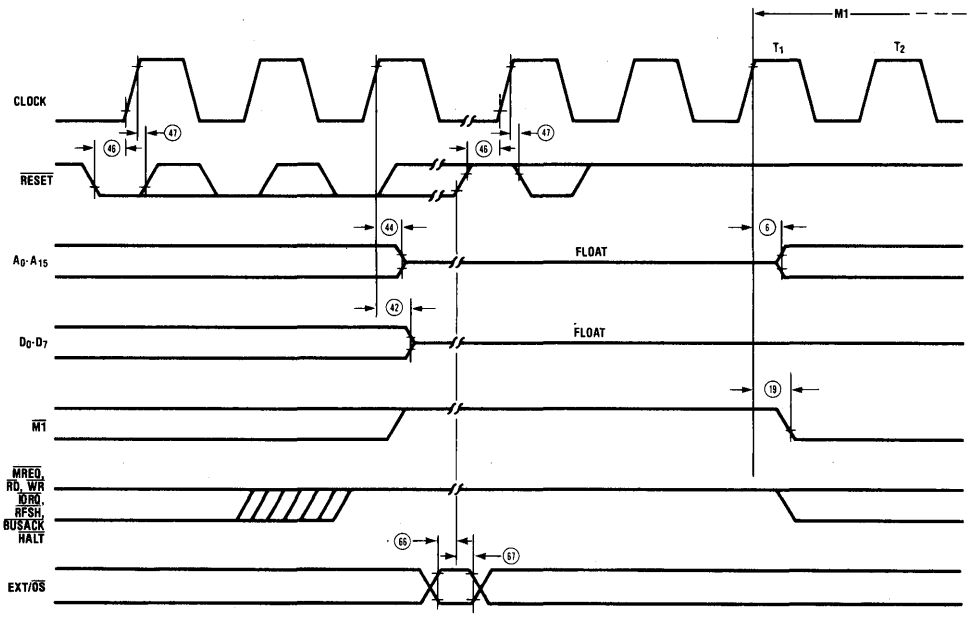
NOTE: INT WILL ALSO FORCE A $\overline{HALT}$ EXIT.

*SEE NOTE, FIGURE 9.

Reset Cycle

$\overline{RESET}$ must be active for at least three clock cycles for the CPU to properly perform its reset operation. As long as $\overline{RESET}$ remains active, the address and data buses float, and the control outputs are inactive. Once $\overline{RESET}$ goes inactive, three internal T cycles are consumed before the CPU resumes normal processing operation (Figure 9). EXT/$\overline{OS}$ is sampled on the rising edge of RESET. If EXT/$\overline{OS}$ is high, the ROM enable latch is reset, and the S83 performs a reset to location 0000H identical to a standard Z80. If EXT/$\overline{OS}$ is low, the internal ROM enable latch is set, enabling the internal 8K byte ROM. The processor is then forced to execute NOP instructions until it reaches address FF00H, where it begins execution. In essence, a reset operation with EXT/$\overline{OS}$ low causes the processor to begin operation at address FF00H in the internal ROM.

Figure 9. Reset Cycle



AC Characteristics

Number	Symbol	Parameter	S83-4 (4.0MHz) Min. (ns)	Max. (ns)
1	TcC	Clock Cycle Time	250*	
2	TwCh	Clock Pulse Width (High)	110	2000
3	TwCl	Clock Pulse Width (Low)	110	2000
4	TfC	Clock Fall Time	—	30
5	TrC	Clock Rise Time		30
6	TdCr(A)	Clock ↑ to Address Valid Delay	—	110
7	TdA(MREQf)	Address Valid to $\overline{MREQ}$ ↓ Delay	65*	—
8	TdCf(MREQf)	Clock ↓ to $\overline{MREQ}$ ↓ Delay	—	85
9	TdCr(MREQr)	Clock ↑ to $\overline{MREQ}$ ↑ Delay	—	85
10	TwMREQh	$\overline{MREQ}$ Pulse Width (High)	110*	
11	TwMREQ1	$\overline{MREQ}$ Pulse Width (Low)	220*	—
12	TdCf(MREQr)	Clock ↓ to $\overline{MREQ}$ ↑ Delay	—	85
13	TdCf(RDf)	Clock ↓ to $\overline{RD}$ ↓ Delay	—	95
14	TdCr(RDr)	Clock ↑ to $\overline{RD}$ ↑ Delay	—	85
15	TsD(Cr)	Data Setup Time to Clock ↑	35	
16	ThD(RDr)	Data Hold Time to $\overline{RD}$ ↑	—	0
17	TsWAIT(Cf)	$\overline{WAIT}$ Setup Time to Clock ↓	70	—
18	ThWAIT(Cf)	$\overline{WAIT}$ Hold Time after Clock ↓	—	0
19	TdCr(M1f)	Clock ↑ to $\overline{M1}$ ↓ Delay	—	100
20	TdCr(M1r)	Clock ↑ to $\overline{M1}$ ↑ Delay		100
21	TdCr(RFSHf)	Clock ↑ to $\overline{RFSH}$ ↓ Delay	—	130
22	TdCr(RFSHr)	Clock ↑ to $\overline{RFSH}$ ↑ Delay	—	120
23	TdCf(RDr)	Clock ↓ to $\overline{RD}$ ↑	—	85
24	TdCr(RDf)	Clock ↑ to $\overline{RD}$ ↓ Delay	—	85
25	TsD(Cf)	Data Setup to Clock ↓ during M_2, M_3, M_4 or M_5 Cycles	50	
26	TdA(IORQf)	Address Stable prior to $\overline{IORQ}$ ↓	180*	—
27	TdCr(IORQf)	Clock ↑ to $\overline{IORQ}$ ↓ Delay	—	75
28	TdCf(IORQr)	Clock ↓ to $\overline{IORQ}$ ↑ Delay	—	85
29	TdD(WRf)	Data Stable prior to $\overline{WR}$ ↓	80*	—
30	TdCf(WRf)	Clock ↓ to $\overline{WR}$ ↓ Delay		80
31	TwWR	$\overline{WR}$ Pulse Width	220*	—
32	TdCf(WRr)	Clock ↓ to $\overline{WR}$ ↑ Delay	—	80
33	TdD(WRf)	Data Stable prior to $\overline{WR}$ ↓	−10*	—
34	TdCr(WRf)	Clock ↑ to $\overline{WR}$ ↓ Delay	—	65
35	TdWRr(D)	Data Stable from $\overline{WR}$ ↑	60*	
36	TdCf(HALT)	Clock ↓ to $\overline{HALT}$ ↑ to ↓	—	300
37	TwNMI	$\overline{NMI}$ Pulse Width	80	—
38	TsBUSREQ(Cr)	$\overline{BUSREQ}$ Setup Time to Clock ↑	50	—
39	ThBUSREQ(Cr)	$\overline{BUSREQ}$ Hold Time after Clock ↑	0	—
40	TdCr(BUSACKf)	Clock ↑ to $\overline{BUSACK}$ ↓ Delay		100
41	TdCf(BUSACKr)	Clock ↓ to $\overline{BUSACK}$ ↑ Delay	—	100
42	TdCr(Dz)	Clock ↑ to Data Float Delay	—	90
43	TdCr(CTz)	Clock ↑ to Control Outputs Float Delay ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$)	—	80

* For clock periods other than the minimums shown in the table, calculate parameters using the expressions in the table on the following page.

AC Characteristics (continued)

Number	Symbol	Parameter	S83-4 (4.0MHz) Min. (ns)	Max. (ns)
44	TdCr(Az)	Clock ↑ to Address Float Delay	—	90
45	TdCTr(A)	$\overline{MREQ}$ ↑, $\overline{IORQ}$ ↑, $\overline{RD}$ ↑, and $\overline{WR}$ ↑ to Address Hold Time	80*	
46	TsRESET(Cr)	$\overline{RESET}$ to Clock ↑ Setup Time	60	—
47	ThRESET(Cr)	$\overline{RESET}$ to Clock ↑ Hold Time	—	0
48	TsINTf(Cr)	$\overline{INT}$ to Clock ↑ Setup Time	80	—
49	ThINTr(Cr)	$\overline{INT}$ to Clock ↑ Hold Time	—	0
50	TdM1f(IORQf)	$\overline{M1}$ ↓ to $\overline{IORQ}$ ↓ Delay	565*	
51	TdCf(IORQf)	Clock ↓ to $\overline{IORQ}$ ↓ Delay	—	85
52	TdCf(IORQr)	Clock ↑ to $\overline{IORQ}$ ↑ Delay	—	85
53	TdCf(D)	Clock ↓ to Data Valid Delay	—	150
54	TsBUSSELf(Cr)	$\overline{BUSSEL}$ ↓ to CLK ↑ Setup	0	
55	ThCr(BUSSEL)	CLK ↓ to $\overline{BUSSEL}$ Hold Time	25	
56	TwRASh	$\overline{RAS}$ Precharge Time (High State)	120	
57	TwRASl	$\overline{RAS}$ Low Pulse Width (Refresh)	220	
58	TdMREQf(RASf)	$\overline{MREQ}$ ↓ to $\overline{RAS}$ ↓ Delay		65
59	TsRAd(RASf)	Row Address Valid to $\overline{RAS}$ ↓ Setup Time	65	
60	ThRASf(RAd)	$\overline{RAS}$ ↓ to Row Address Hold Time	20	
61	TdCf(CASf)	CLK ↓ to $\overline{CAS}$ ↓ Delay		75
62	TsCAd(CASf)	Column Address to $\overline{CAS}$ ↓ Setup Time	35	
63	TdCr(CAd)	CLK ↑ to Column Address Valid Delay		160
64	TsRFAd(RASf)	Refresh Address to $\overline{RAS}$ ↓ Setup Time	0	
65	TdMREQr(CASr)	$\overline{MREQ}$ ↑ to $\overline{CAS}$ ↑ Delay		85
66	TsEXT(RESETr)	EXT to $\overline{RESET}$ ↑ Setup Time	60	
67	ThEXT(RESETr)	EXT to $\overline{RESET}$ ↑ Hold Time	0	
68	TdCr(RASr)	CLK ↑ to $\overline{RAS}$ ↑ Delay (M1 Cycle)		85
69	TdMREQr(RASr)	$\overline{MREQ}$ ↑ to $\overline{RAS}$ ↑ Delay (Non-M1 Cycle)		85

* For clock periods other than the minimums shown in the table, calculate parameters using the expressions in the table on the following page.

Footnotes to AC Characteristics

Number	Symbol	S83-4
1	TcC	TwCh + TwC1 + TrC + TfC
7	TdA(MREQf)	TwCh + TfC − 65
10	TwMREQh	TwCh + TfC − 20
11	TwMREQ1	TcC − 30
26	TdA(IORQf)	TcC − 70
29	TdD(WRf)	TcC − 170
31	TwWR	TcC − 30
33	TdD(WRf)	TwC1 + TrC − 140
35	TdWRr(D)	TwC1 + TrC − 70
45	TdCTr(A)	TwC1 + TrC − 50
50	TdM1f(IORQf)	2TcC + TwCh + TfC − 65

AC Test Conditions:

V_{IH} = 2.0V
V_{IL} = 0.8V
$V_{IHC} = V_{CC} - 0.6V$
V_{ILC} = 0.45V

V_{OH} = 2.0V
V_{OL} = 0.8V
FLOAT = ±0.5V

Absolute Maximum Ratings

Storage Temperature	65°C to +150°C
Temperature under Bias	Specified Operating Range
Voltages on all inputs and outputs with respect to ground	−0.3V to +7V
Power Dissipation	1.5 W

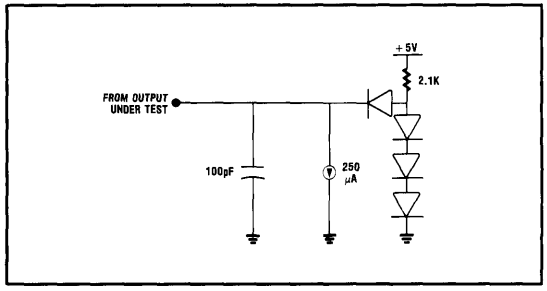
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin. Available operating temperature ranges are:

■ S* = 0°C to +70°c, $+4.75V \leq V_{CC} < +5.25V$

All ac parameters assume a load capacitance of 100pF. Add 10ns delay for each 50pF increase in load up to a maximum of 200pF for the data bus and 100pF for address and control lines.



DC Characteristics

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	−0.3	0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC} −.6	V_{CC} +.3	V	
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −250μA
I_{CC}	Power Supply Current		200	mA	
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to V_{CC}
I_{LEAK}	3-State Output Leakage Current in Float	−10	10[1]	μA	V_{OUT} = 0.4 to V_{CC}

1. A_{15}-A_0, D_7-D_0, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$.

Capacitance

Symbol	Parameter	Min.	Max.	Unit	Note
C_{CLOCK}	Clock Capacitance		35	pF	
C_{IN}	Input Capacitance		10	pF	Unmeasured pins returned to ground
C_{OUT}	Output Capacitance		10	pF	

T_A = 25°C, f = 1MHz.

AMI

A Subsidiary
of Gould Inc.

S9900

HIGH PERFORMANCE MICROPROCESSOR FAMILY

Contact factory for complete data sheets

S9900 Family Selection Guide

Microprocessors

S9900	16-Bit Microprocessor
S9980A	16-Bit Microprocessor 8-Bit Data Bus

Peripherals

S9901/S9901-4	Programmable Systems Interface (PSI)
S9902/S9902-4	UART/Asynchronous Communications Controller (USRT/ACC)

AMI

A Subsidiary of Gould Inc.

S9900

16-BIT MICROPROCESSOR

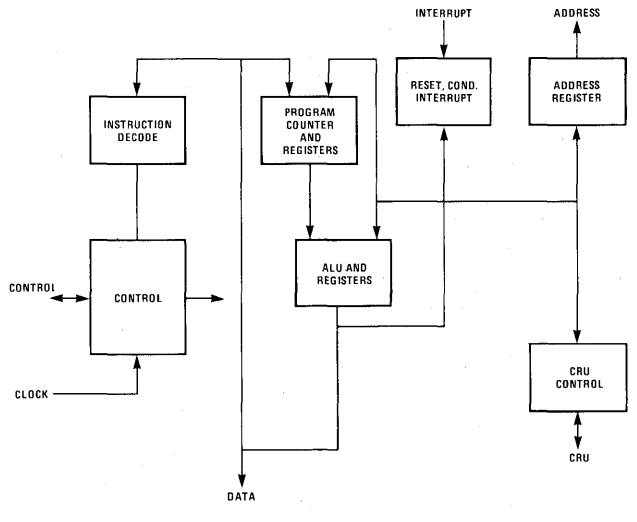
Features

- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability Including Multiply and Divide
- ☐ Up to 65,536 Bytes of Memory
- ☐ 3.3MHz Speed
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 16 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ N-Channel Silicon-Gate Technology

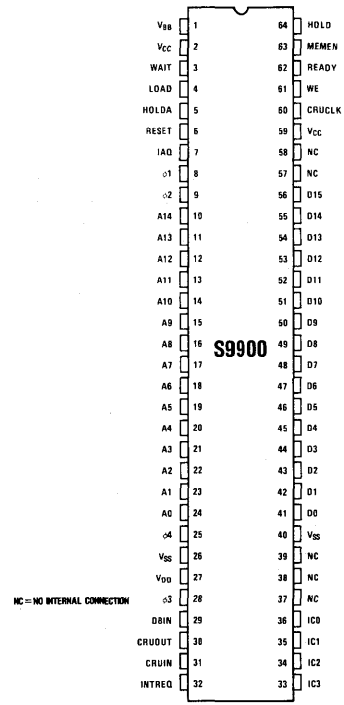
General Description

The S9900 microprocessor is a single-chip 16-bit central processing unit (CPU) produced using N-Channel silicon-gate MOS technology. The instruction set of the S9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. AMI provides a compatible set of MOS memory and support circuits to be used with an S9900 system. The system is fully supported by software and complete prototyping systems.

Block Diagram



Pin Configuration



S9900 FAMILY

S9900 Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply Voltage, V_{CC} (See Note 1)	− 0.3V to + 20V
Supply Voltage, V_{DD} (See Note 1)	− 0.3V to + 20V
Supply Voltage, V_{SS} (See Note 1)	− 0.3V to + 20V
All Input Voltages (See Note 1)	− 0.3V to + 20V
Output Voltage, (With Respect to V_{SS})	− 2V to + 7V
Continuous Power Dissipation	1.2W
Operating Free-Air Temperature Range	0°C to + 70°C
Storage Temperature Range	− 55°C to + 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the most negative supply, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this section, voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage	− 5.25	− 5	− 4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage (all inputs except clocks)	2.2	2.4	V_{CC} + 1	V	
$V_{IH(\phi)}$	High-level clock input voltage $V_{DD} = 11.4$ $V_{DD} = 12.6$	10.0 10.6		V_{DD}	V	
V_{IL}	Low-level input voltage (all inputs except clocks)	− 1	0.4	0.8	V	
$V_{IL(\phi)}$	Low-level clock input voltage	− 0.3	0.3	0.6	V	
T_A	Operating free-air temperature	0		70	°C	

Timing Requirements Over Full Range of Recommended Operating Conditions (See Figures 1 and 2)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
t_{C} (ϕ)	Clock Cycle time	0.3	0.333	0.5	μs	
t_{r} (ϕ)	Clock rise time	10	12		ns	
t_{f} (ϕ)	Clock fall time	10	12		ns	
t_{W} (ϕ)	Pulse width, any clock high	40	45	100	ns	
$t_{\phi 1L, \phi 2L}$	Delay time, clock 1 low to clock 2 low**	0	5		ns	
$\tau_{\phi 2L, \phi 3L}$	Delay time, clock 2 low to clock 3 low**	0	5		ns	
$t_{\phi 3L, \phi 4L}$	Delay time, clock 3 low to clock 4 low**	0	5		ns	
$t_{\phi 4L, \phi 1L}$	Delay time, clock 4 low to clock 1 low**	0	5		ns	
$t_{\phi 1H, \phi 2H}$	Delay time, clock 1 high to clock 2 high***	73	83		ns	
$t_{\phi 2H, \phi 3H}$	Delay time, clock 2 high to clock 3 high***	73	83		ns	
$t_{\phi 3H, \phi 4H}$	Delay time, clock 3 high to clock 4 high***	73	83		ns	
$t_{\phi 4H, \phi 1H}$	Delay time, clock 4 high to clock 1 high***	73	83		ns	
t_{SU}	Data or control setup time before clock 1	30			ns	
t_{h}	Data hold time after clock 1	10			ns	

** = Time between clock pulses

*** = Time between leading edges

Electrical Characteristics Over Full Range of Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter		Min.	Typ.†	Max.	Unit	Conditions
I_I	Input Current	Data Bus during DBIN		± 50	± 100	μA	$V_I = V_{SS}$ to V_{CC}
		$\overline{WE}$, $\overline{MEMEN}$, DBIN, Address bus, Data bus during HOLDA		+ 50	± 100		$V_I = V_{SS}$ to V_{CC}
		Clock*		± 25	± 75		$V_I = -0.3$ to 12.6V
		Any other inputs		± 1	± 10		$V_I = V_{SS}$ to V_{CC}
V_{OH}	High-level output voltage		2.4		V_{CC}	V	$I_O = -0.4$mA
V_{OL}	Low-level output voltage				0.65 0.50	V	$I_O = 3.2$mA $I_O = 2$mA
I_{BB}	Supply current from V_{BB}			0.1	1	mA	
I_{CC}	Supply current from V_{CC}			50	75	mA	
I_{DD}	Supply current from V_{DD}			25	45	mA	
C_i	Input capacitance (any inputs except clock and data bus)			10	15	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 1)}$	Clock-1 input capacitance			100	150	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 2)}$	Clock-2 input capacitance			150	200	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 3)}$	Clock-3 input capacitance			100	150	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 4)}$	Clock-1 input capacitance			100	150	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
C_{DB}	Data bus capacitance			15	25	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}
C_O	Output capacitance (any output except data bus)			10	15	pF	$V_{BB} = -5$, f = 1MHz, unmeasured pins at V_{SS}

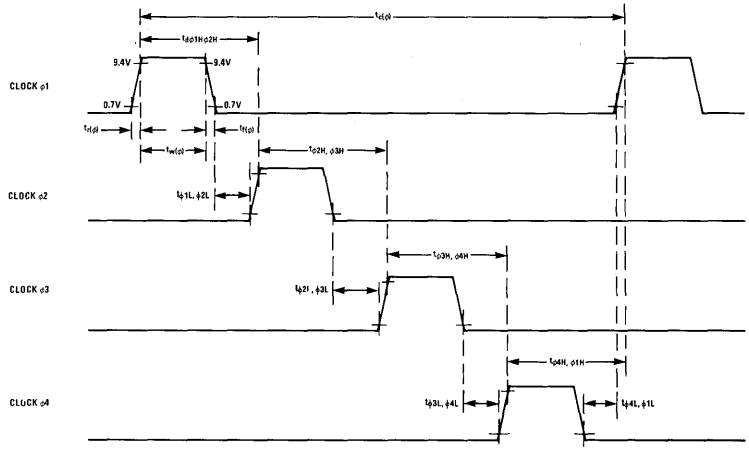
† All typical values are at $T_A = 25°C$ and nominal voltages

* D.C. Component of Operating Clock

Switching Characteristics Over Full Range of Recommended Operating Conditions (See Figure 2)

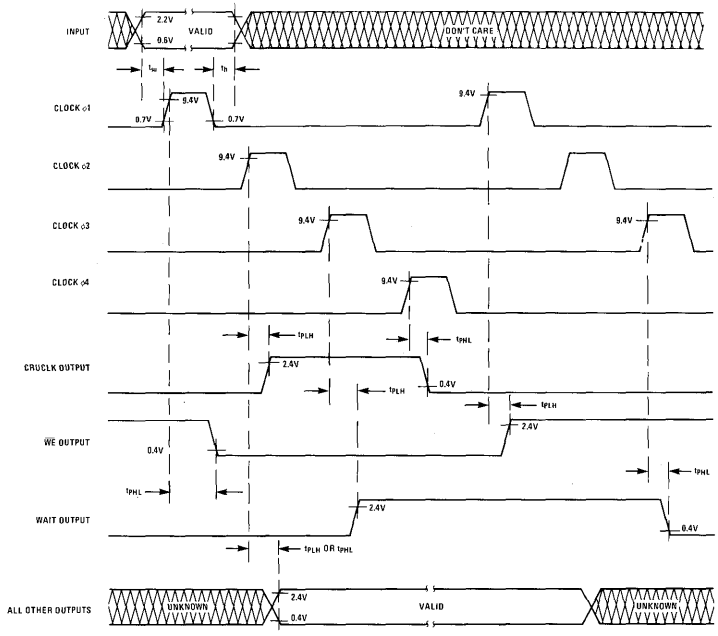
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PLH} or t_{PHL}	Propagation delay time, clocks to outputs					$C_L = 200$pF
	CRUCLK, WE, MEMEN, WAIT, DBIN			30	ns	
	All other outputs		20	40	ns	

Figure 1. Clock Timing



Note: All timing and voltage levels shown on ϕ1 apply to ϕ2, ϕ3, and ϕ4 in the same manner.

Figure 2. Signal Timing



†The number of cycles over which input/output data must/will remain valid can be determined from the number of wait states required for memory access. Note that in all cases data should not change during ϕ1.

Pin Description

Table 1 defines the S9900 pin assignments and describes the function of each pin.

Table 1. S9900 Pin Assignments and Functions

Signature	Pin	I/O	Description
			ADDRESS BUS
A0 (MSB)	24	OUT	A0 through A14 comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when $\overline{\text{MEMEN}}$ is active and I/O-bit addresses and external-instruction addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A1	23	OUT	
A2	22	OUT	
A3	21	OUT	
A4	20	OUT	
A5	19	OUT	
A6	18	OUT	
A7	17	OUT	
A8	16	OUT	
A9	15	OUT	
A10	14	OUT	
A11	13	OUT	
A12	12	OUT	
A13	11	OUT	
A14 (LSB)	10	OUT	
			DATA BUS
D0 (MSB)	41	I/O	D0 through D15 comprise the bidirectional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is active. The data bus assumes the high-impedance state when HOLDA is active.
D1	42	I/O	
D2	43	I/O	
D3	44	I/O	
D4	45	I/O	
D5	46	I/O	
D6	47	I/O	
D7	48	I/O	
D8	49	I/O	
D9	50	I/O	
D10	51	I/O	
D11	52	I/O	
D12	53	I/O	
D13	54	I/O	
D14	55	I/O	
D15 (LSB)	56	I/O	
			POWER SUPPLIES
V_{BB}	1		Supply voltage (-5V NOM)
V_{CC}	2,59		Supply voltage (5V NOM). Pins 2 and 59 must be connected in parallel.
V_{DD}	27		Supply volage (12V NOM)
V_{SS}	26,40		Ground reference. Pins 26 and 40 must be connected in parallel.
			CLOCKS
$\phi 1$	8	IN	Phase-1 clock
$\phi 2$	9	IN	Phase-2 clock
$\phi 3$	28	IN	Phase-3 clock
$\phi 4$	25	IN	Phase-4 clock

Table 1. S9900 Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
			BUS CONTROL
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the S9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains low in all other cases except when HOLDA is active.
$\overline{\text{MEMEN}}$	63	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	61	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the S9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0 through A2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	Interrupt request. When active (low), $\overline{\text{INTREQ}}$ indicates that an external-interrupt is requested. If $\overline{\text{INTREQ}}$ is active, the processor loads the data on the interrupt-code-input lines IC0 through IC3 into the internal interrupt-code-storage register. The code is compared to the interrupt mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15) the S9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. $\overline{\text{INTREQ}}$ should remain active and the processor will continue to sample IC0 through IC3 until the program enables a sufficiently low priority to accept the request interrupt.
IC0 (MSB) IC1 IC2 IC3 (LSB)	36 35 34 33	IN IN IN IN	Interrupt codes. IC0 is the MSB of the interrupt code, which is sampled when $\overline{\text{INTREQ}}$ is active. When IC0 through IC3 are LLLH, the highest external-priority interrupt is being requested and when HHHH, the lowest-priority interrupt is being requested.
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9900 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.

*If the cycle following the present memory cycle is also a memory cycle, it, too, is completed before the S9900 enters the hold state. The maximum number of consecutive memory cycles is three.

Table 1. S9900 Assignments and Functions (Continued)

Signature	Pin	I/O	Description
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{WE}$, $\overline{MEMEN}$, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the S9900 has entered a wait state because of a not-ready condition from memory.
			TIMING AND CONTROL
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9900 is acquiring an instruction. IAQ can be used to detect illegal op codes.
$\overline{LOAD}$	4	IN	Load. When active (low), $\overline{LOAD}$ causes the S9900 to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. $\overline{LOAD}$ will also terminate an idle state. If $\overline{LOAD}$ is active during the time $\overline{RESET}$ is released, then the $\overline{LOAD}$ trap will occur after the $\overline{RESET}$ fuction is completed. $\overline{LOAD}$ should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold-start ROM loaders. Additionally, front-panel routines can be implemented using CRU bits as front-panel-interface signals and software-control routines to control the panel operations.
$\overline{RESET}$	6	IN	Reset. When active (low), $\overline{RESET}$ causes the processor to be reset and inhibits $\overline{WE}$ and CRUCLK. When $\overline{RESET}$ is released, the S9900 then initiates a level-zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. $\overline{RESET}$ will also terminate an idle state. $\overline{RESET}$ must be held active for a minimum of three clock cycles.

*If the cycle following the present memory cycle is also a memory cycle it, too, is completed before the S9900 enters the hold state. The maximum number of consecutive memory cycles is three.

AMI

A Subsidiary of Gould Inc.

S9980A

16-BIT MICROPROCESSOR

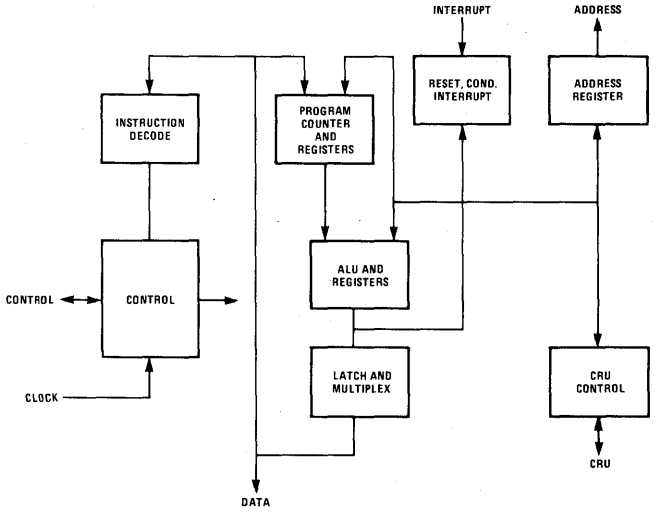
Features

- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability Including Multiply and Divide
- ☐ Up to 16,384 Bytes of Memory
- ☐ 8-Bit Memory Data Bus
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 4 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ On-Chip 4-Phase Clock Generator
- ☐ 40-Pin Package
- ☐ N-Channel Silicon-Gate Technology

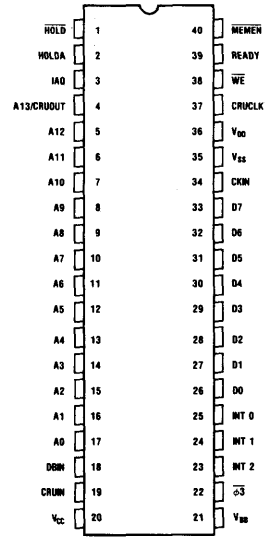
General Description

The S9980A microprocessor is a software-compatible member of AMI's 9900 family of microprocessors. Designed to minimize the system cost for smaller systems, the S9980A is a single-chip 16-bit central processing unit (CPU) which has an 8-bit data bus, on-chip clock, and is packaged in a 40-pin package. The instruction set of the S9980A includes the capabilities offered by full minicomputers and is exactly the same as the 9900s. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort.

Block Diagram



Pin Configuration



S9980A Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply Voltage, V_{CC} (See Note 1) ..... −0.3V to +15V
Supply Voltage, V_{DD} (See Note 1) ..... −0.3V to +15V
Supply Voltage, V_{BB} (See Note 1) ..... −5.25V to +0V
All Input Voltages (See Note 1) ..... −0.3V to +15V
Output Voltage, (See Note 1) ..... −2V to +7V
Continuous Power Dissipation 1.4W
Operating Free-Air Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the most negative supply, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this section, voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage	−5.25	−5	−4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage	2.2	2.4	$V_{CC}+1$	V	
V_{IL}	Low-level input voltage	−1	0.4	0.8	V	
T_A	Operating free-air temperature	0	20	70	°C	

Electrical Characterisitcs Over Full Range of Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter		Min.	Typ.*	Max.	Unit	Conditions
I_I	Input Current	Data Bus during DBIN			±75	μA	$V_I = V_{SS}$ to V_{CC}
		$\overline{WE}$, $\overline{MEMEN}$, $\overline{DBIN}$, during HOLDA			±75	μA	$V_I = V_{SS}$ to V_{CC}
		Any other inputs			±10	μA	$V_I = V_{SS}$ to V_{CC}
V_{OH}	High-level output voltage		2.4			V	$I_O = -0.4$mA
V_{OL}	Low-level output voltage				0.5 0.65	V	$I_O = 2$mA $I_O = 3.2$mA
I_{BB}	Supply current from V_{BB}				1	mA	
I_{CC}	Supply current from V_{CC}			50 40	60 50	mA	0°C 70°C
I_{DD}	Supply current from V_{DD}			70 65	80 75	mA	0°C 70°C
C_i	Input capacitance (any inputs except data bus)			15		pF	f = 1MHz, unmeasured pins at V_{SS}
C_{DB}	Data bus capacitance			25		pF	f = 1MHz, unmeasured pins at V_{SS}
C_o	Output capacitance (any output except data bus)			15		pF	f = 1MHz, unmeasured pins at V_{SS}

* All typical values are at $T_A = 25°C$ and nominal voltages

External Clock

The external clock on the S9980 uses the CKIN pin. The external clock source must conform to the following specifications:

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
f_{ext}	External source frequency*	6		10	MHz	
V_H	External source high level	2.2			V	
V_L	External source low level			0.8	V	
t_r/t_f	External source rise/fall time		10		ns	
t_{WH}	External source high level pulse width	40			ns	
t_{WL}	External source low level pulse width	40			ns	

*This allows a system speed of 1.5MHz to 2.5MHz

Switching characteristics Over Full Range of Recommended Operating Conditions

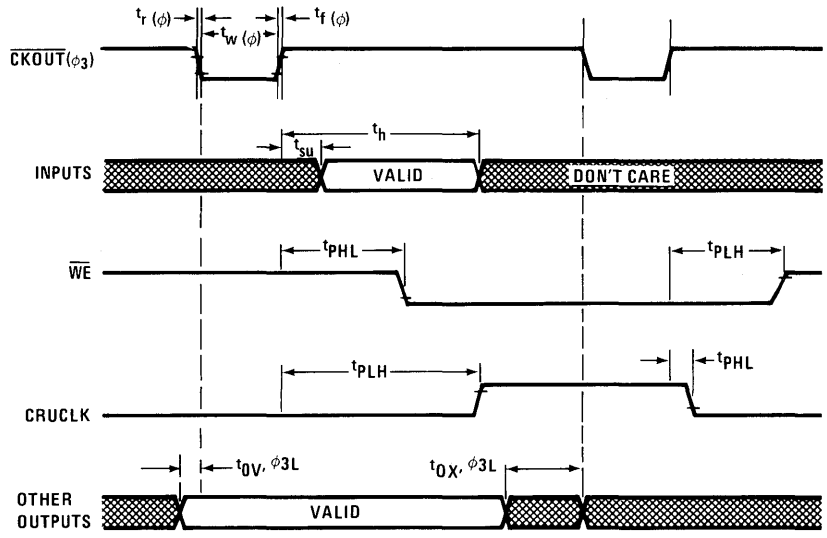
The timing of all the inputs and outputs is controlled by the internal 4 phase clock; thus all timings are based on the width of one phase of the internal clock. This is $1/f_{(CKIN)}$ (whether driven or from a crystal). This is also $1/4 f_{system}$. In the following table this phase time is denoted t_w.

All external signals are with reference to $\phi 3$ (see Figure 1).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_r ($\phi 3$)	Rise time of $\phi 3$	3	5	10	ns	
t_r ($\phi 3$)	Fall time of $\phi 3$	5	7.5	15	ns	
t_w ($\phi 3$)	Pulse width of $\phi 3$	t_w-15	t_w-10	t_w+10	ns	
t_{su}	Data or control setup time*	t_w-30			ns	
t_h	Data hold time*	$2t_w+10$			ns	$t_w = 1/f_{(CKIN)}$
$t_{PHL}(\overline{WE})$	Propagation delay time WE high to low	t_w-10	t_w	t_w+20	ns	$= 1/4 f_{system}$
$t_{PLH}(\overline{WE})$	Propagation delay time WE low to high	t_w	t_w+10	t_w+30	ns	$C_L = 200pF$
$t_{PHL(CRUCLK)}$	Propagation delay time, CRUCLK high to low	-20	-10	$+10$	ns	
$t_{PHL(CRUCLK)}$	Propagation delay time, CRUCLK low to high	$2t_w-10$	$2t_w$	$2t_w+20$	ns	
t_{OV}	Delay time from output valid to $\phi 3$ low	t_w-50	t_w-30		ns	
t_{OX}	Delay time from output invalid to $\phi 3$ low		t_w-20	t_w	ns	

*All inputs except IC0–IC2 must be synchronized to meet these requirements. IC0–IC2 may change synchronously.

Figure 1. External Signal Timing



Pin Description

Table 1 defines the S9980A pin assignments and describes the function of each pin.

Table 1. S9980A Pin Assignments and Functions

Signature	Pin	I/O	Description
A0 (MSB)	17	OUT	**ADDRESS BUS**
A1	16	OUT	A0 through A13 comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when MEMEN is active and I/O-bit addresses and external-instruction addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A2	15	OUT	
A3	14	OUT	
A4	13	OUT	
A5	12	OUT	
A6	11	OUT	
A7	10	OUT	
A8	9	OUT	
A9	8	OUT	
A10	7	OUT	
A11	6	OUT	
A12	5	OUT	
A13/CRUOUT	4	OUT	**CRUOUT** Serial I/O data appears on A13 when an LDCR, SBZ and SBO instruction is executed. This data should be sampled by the I/O interface logic when CRUCLK goes active (high). One bit of the external instruction code appears on A13 during external instruction execution.
D0 (MSB)	26	I/O	**DATA BUS**
D1	27	I/O	D0 through D7 comprise the bidirectional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is active. The data bus assumes the high-impedance state when HOLDA is active.
D2	28	I/O	
D3	29	I/O	
D4	30	I/O	
D5	31	I/O	
D6	32	I/O	
D7 (LSB)	33	I/O	

Table 1. S9980A Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
			POWER SUPPLIES
V_{BB}	21		Supply voltage (−5V NOM)
V_{CC}	20		Supply voltage (5V NOM)
V_{DD}	36		Supply voltage (12V NOM)
V_{SS}	35		Ground reference
			CLOCKS
CKIN	34	IN	Clock In. A TTL compatible input used to generate the internal 4-phase clock. CKIN frequency is 4 times the desired system frequency.
$\overline{\phi 3}$	22	OUT	Clock phase 3 ($\phi 3$) inverted; used as a timing reference.
			BUS CONTROL
DBIN	18	OUT	Data bus in. When active (high), DBIN indicates that the S9980A has disabled its output buffers to allow the memory to place memory-read data on the data bus during MEMEN. DBIN remains low in all other cases except when HOLDA is active at which time it is in the high-impedance state.
$\overline{\text{MEMEN}}$	40	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address. When HOLDA is active, $\overline{\text{MEMEN}}$ is in the high impedance state.
$\overline{\text{WE}}$	38	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the S9980 to be written into memory. When HOLDA is active, $\overline{\text{WE}}$ is in the high-impedance state.
CRUCLK	37	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0, A1, A13.
CRUIN	19	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A2 through A12).
INT2	23	IN	Interrupt code. Refer to interrupt discussion for detailed description.
INT1	24	IN	
INT0	25	IN	
			MEMORY CONTROL
$\overline{\text{HOLD}}$	1	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9980A enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.
HOLDA	2	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) are in the high-impedance state.
READY	39	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9980A enters a wait state and suspends internal operation until the memory systems indicated ready.
			TIMING AND CONTROL
IAQ	3	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9980A is acquiring an instruction. IAQ can be used to detect illegal op codes. It may also be used to synchronize LOAD stimulus.

*If the cycle following the present memory cycle is also a memory cycle it, too, is completed before S9980 enters hold state.

A Subsidiary of Gould Inc.

S9901/S9901-4

PROGRAMMABLE SYSTEMS INTERFACE CIRCUIT

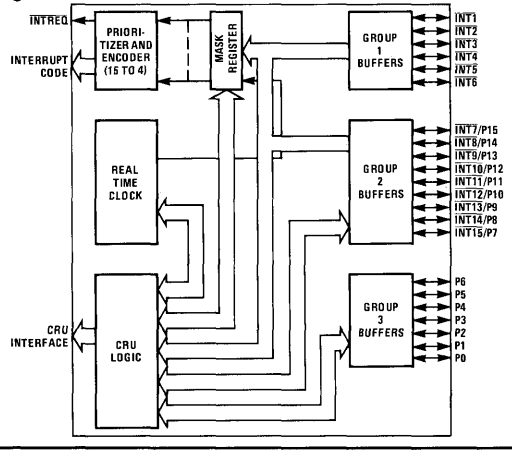
Features

- ☐ N-Channel Silicon-Gate Process
- ☐ 9900 Series CRU Peripheral
- ☐ Performs Interrupt and I/O Interface Functions
  - 6 Dedicated Interrupt Input Lines
  - 7 Dedicated I/O Ports
  - 9 Ports Programmable as Interrupts or I/O
- ☐ Easily Stacked for Interrupt and I/O Expansion
- ☐ Interval and Event Timer
- ☐ Single 5V Supply

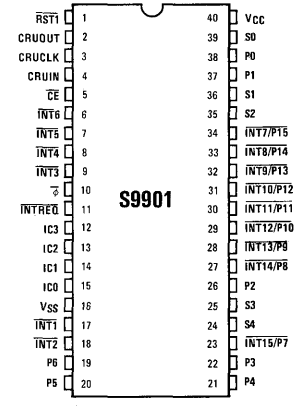
General Description

The S9901 Programmable Systems Interface is a multi-functioned component designed to provide low cost interrupts and I/O ports in a 9900/9980 microprocessor system. It is fabricated with N-channel silicon-gate technology and is completely TTL compatible on all inputs including the power supply (+5V) and single-phase clock. The Programmable Systems Interface provides a 9900/9980 system with interrupt control, I/O ports, and a real-time clock as shown on page 1.

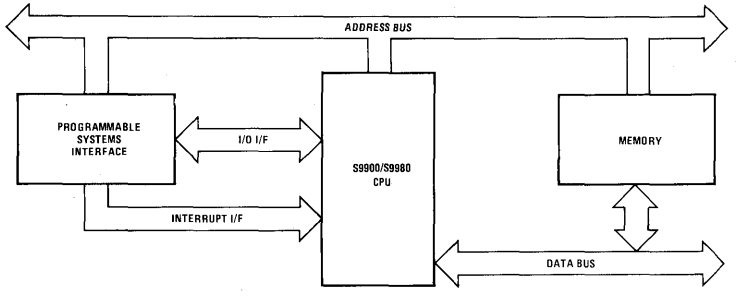
Block Diagram



S9901 Pin Configuration



S9900/9980 System



S9900 FAMILY

S9901 Electrical Specifications

Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply Voltages, V_{CC} and V_{SS} ..... −0.3V to +10V
All Input and Output Voltages ..... −0.3V to +10V
Continuous Power Dissipation 0.75W
Operating Free-Air Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_{SS}		0		V
High-Level Input Voltage, V_{IH}		2		V
Low-Level Input Voltage, V_{IL}		0.8		V
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics

Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_I	Input Current (Any Input)		±10		μA	$V_I = 0V$ to V_{CC}
V_{OH}	High Level Output Voltage		2.4		V	$I_{OH} = 100\mu A$
			2		V	$I_{OH} = -400\mu A$
V_{OL}	Low Level Output Voltage		0.4		V	$I_{OL} = 3.2mA$
I_{CC}	Supply Current from V_{CC}		100		mA	
I_{SS}	Supply Current from V_{SS}		200		mA	
$I_{CC(av)}$	Average Supply Current from V_{CC}		60		mA	$t_{C(0)} = 333ns$, $T_A = 25°C$
C_i	Capacitance, Any Input		10		pF	$f = 1MHz$,
C_o	Capacitance, Any Output		20		pF	All Other Pins at 0V

Timing Requirements

Over Full Range of Operating Conditions

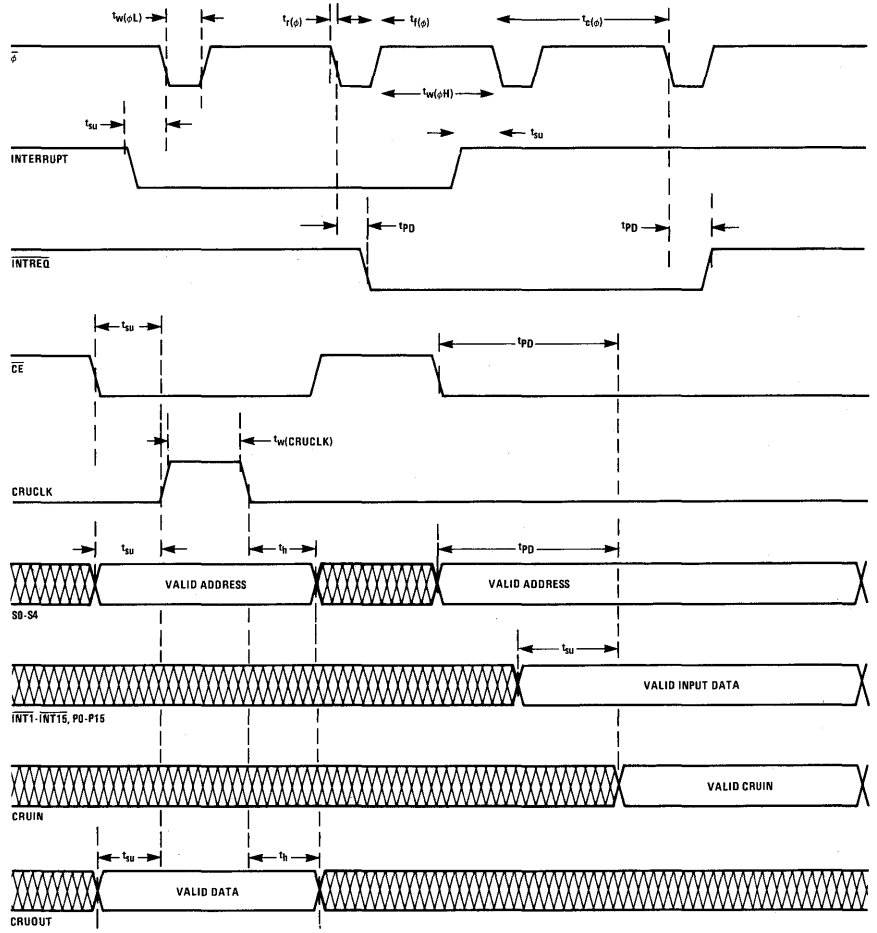
Symbol	Parameter	S9901			S9901-4			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
$t_{C(0)}$	Clock Cycle Time	300	333	2000	240	250	667	ns
$t_{r(0)}$	Clock Rise Time	5	10	40	5		40	ns
$t_{f(0)}$	Clock Fall Time	5	10	40	10		40	ns
$t_{w(0L)}$	Clock Pulse Low Width	45	55	300	40		300	ns
$t_{w(0H)}$	Clock Pulse High Width	225	240		180			ns
t_{su_1}	Setup Time for S_0-S_4, CE, or CRU_{OUT} Before CRU_{CLK}	100	200		80	80		ns
t_{su_3}	Setup Time, Input Before Valid CRU_{IN}	200	200		180	180		ns
t_{su_2}	Setup Time, Interrupt Before 0 Low	60	80		50	50		ns
$t_{w(CRUCLK)}$	CRU Clock Pulse Width	100			80			ns
t_h	Address Hold Time	60	80		50			ns

Switching Characteristics

Over Full Range of Recommended Operating Conditions

Symbol	Parameter	S9901			S9901-4			Unit	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PD}	Propagation Delay, 0 Low to Valid $\overline{INTREQ}$, I_{C0}-I_{C3}		110	110		80	80	ns	C_L = 100pF, 2 TTL Loads
t_{PD}	Propagation Delay, S_0-S_4 or $\overline{CE}$ to Valid CRU_{IN}		320	320		240	240	ns	C_L = 100pF

Figure 1. Switching Characteristics



NOTE 1: ALL TIMING MEASUREMENTS ARE FROM 10% and 90% POINTS

Pin Definitions

Table 1 defines the S9901 pin assignments and describes the function of each pin.

Table 1.S9901 Pin Assignments and Functions

Signature	Pin	I/O	Description
$\overline{\text{INTREQ}}$	11	OUT	INTERRUPT Request. When active (low) $\overline{\text{INTREQ}}$ indicates that an enabled interrupt has been received. $\overline{\text{INTREQ}}$ will stay active until all enabled interrupt inputs are removed.
IC0 (MSB)	15	OUT	Interrupt Code lines. IC0–IC3 output the binary code corresponding to the highest priority enabled interrupt. If no enabled interrupts are active IC0–IC3 = (1,1,1,1)
IC1	14	OUT	
IC2	13	OUT	
IC3 (LSB)	12	OUT	
CE	5	IN	Chip Enable. When active (low) data may be transferred through the CRU interface to the CPU. CE has no effect on the interrupt control section.
S0	39	IN	Address select lines. The data bit being accessed by the CRU interface is specified by the 5-bit code appearing on S0–S4
S1	36	IN	
S2	35	IN	
S3	25	IN	
S4	24	IN	
CRUIN	4	OUT	CRU data in (to CPU). Data specified by S0–S4 is transmitted to the CPU by CRUIN. When $\overline{\text{CE}}$ is not active CRUIN is in a high-impedance state.
CRUOUT	2	IN	CRU data out (from CPU). When $\overline{\text{CE}}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the command bit specified by S0–S4.
CRUCLK	3	IN	CRU Clock (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{\text{RST1}}$	1	IN	Power Up Reset. When active (low) $\overline{\text{RST1}}$ resets all interrupt masks to "0", disables the clock, and programs all I/O ports to inputs. $\overline{\text{RST1}}$ has a Schmitt-Trigger input to allow implementation with an RC circuit as shown in Figure 6.
V_{CC}	40		Supply Voltage. + 5V nominal.
V_{SS}	16		Ground Reference.
ϕ	10		System Clock (ϕ3 in S9900 system, $\overline{\text{CKOUT}}$ in S9980 system).
$\overline{\text{INT1}}$	17	IN	Group 1, interrupt inputs. When active (low) the signal is ANDed with its corresponding mask bit and if enabled sent to the interrupt control section. INT1 has highest priority.
$\overline{\text{INT2}}$	18	IN	
$\overline{\text{INT3}}$	9	IN	
$\overline{\text{INT4}}$	8	IN	
$\overline{\text{INT5}}$	7	IN	
$\overline{\text{INT6}}$	6	IN	
$\overline{\text{INT7}}$/P15	34	I/O	Group 2. Programmable interrupt (active low) or I/O pins (true logic). Each pin is individually programmable as an interrupt, as input port, or an output port.
$\overline{\text{INT8}}$/P14	33	I/O	
$\overline{\text{INT9}}$/P13	32	I/O	
$\overline{\text{INT10}}$/P12	31	I/O	
$\overline{\text{INT11}}$/P11	30	I/O	
$\overline{\text{INT12}}$/P10	29	I/O	
$\overline{\text{INT13}}$/P9	28	I/O	
$\overline{\text{INT14}}$/P8	27	I/O	
$\overline{\text{INT15}}$/P7	23	I/O	
P0	38	I/O	Group 3, I/O ports (true logic). Each pin is individually programmable as an input port or an output port.
P1	37	I/O	
P2	26	I/O	
P3	22	I/O	
P4	21	I/O	
P5	20	I/O	
P6	19	I/O	

Functional Description

CPU Interface

The S9901 interfaces to the CPU through the Communications Register Unit (CRU) and the interrupt control lines as shown on page 1. The CRU interface consists of 5 address select lines (S_0-S_4), chip enable ($\overline{CE}$), and 3 CRU lines ($CRU_{\overline{IN}}$, CRU_{OUT}, CRU_{CLK}). When $\overline{CE}$ becomes active (low), the 5 select lines point to the CRU bit being accessed (see Table 2). In the case of a write, the datum is strobed off the CRU_{OUT} line by the CRU_{CLK} signal. For a read, the datum is sent to the CPU on the CRU_{IN} line. The interrupt control lines consist of an interrupt request line ($\overline{INTREQ}$) and 4 code lines (IC_0 -IC_3). The interrupt section of the S9901 prioritizes and encodes the highest priority active interrupt into the proper code to present to the CPU, and outputs this code on the IC_0-IC_3 code lines along with an active $\overline{INTREQ}$. Several S9901's can be used with the CPU by connecting all CRU and address lines in parallel and providing a unique chip select to each device.

System Interface

The system interface consists of 22 pins divided into 3 groups. The 6 pins in Group 1 ($\overline{INT}_1$-$\overline{INT}_6$) are normally dedicated to interrupt inputs (active low), but may also be used as input ports (true data in). Group 2 ($\overline{INT}_7$/P_{15}-$\overline{INT}_{15}$/P_7) consists of 9 pins which can be individually programmed as interrupt inputs (active low), input ports (true data in), or output ports (true data out). The remaining 7 pins which comprise Group 3 (P_0-P_6) are dedicated as individually programmable I/O ports (true data).

Interrupt Control

A block diagram of the interrupt control section is shown in Figure 2. The interrupt inputs (6 dedicated, 9 programmable) are sampled by $\overline{\phi}$ (active low) and are ANDed with their respective mask bits. If an interrupt input is active (low) and enabled (MASK = 1), the signal is passed through to the priority encoder where the highest priority signal is encoded into a 4-bit binary code as shown in Table 3. The code along with the interrupt request is then output via the CPU interface on the leading edge of the next $\overline{\phi}$ to ensure proper synchronization to the processor.

The output signals will remain valid until the corresponding interrupt input is removed, the interrupt is disabled (MASK = 0), or a higher priority enabled interrupt becomes active. When the highest priority enabled interrupt is removed, the code corresponding to the next highest priority enabled interrupt is output. If no enabled interrupt is active, all CPU interface lines ($\overline{INTREQ}$, IC_0-IC_3) are held high. $\overline{RST}_1$ (power-up-reset) will force the output code to (0,0,0,0) with $\overline{INTREQ}$ held high and will reset all mask bits low (interrupts disabled). Individual interrupts can be subsequently enabled (disabled) by programming the appropriate command bits. Unused interrupt inputs may be used as datum inputs by disabling the interrupt (MASK = 0).

Input/Output

A block diagram of the I/O section is shown in Figure 3. Up to 16 individually controlled I/O ports are available (7 dedicated, 9 programmable). $\overline{RST}_1$ or $\overline{RST}_2$ (a command bit) will program all ports to the input mode. Writing a datum to any port will program that port to the output mode and latch out the datum. The port will then remain in the output mode until either $\overline{RST}_1$ or $\overline{RST}_2$ is executed. Data present on the Group 2 pins can be read by either the Read Interrupt Commands or the Read Input Commands. Group 2 pins being used as input ports should have their respective Interrupt Mask values reset (low) to prevent false interrupts from occurring. In applications where Group 1 pins are not required as interrupt inputs, they may be used as input ports and read using the Read Input commands. As with Group 2 ports, any pins being used as input ports should have their respective Interrupt Masks disabled.

Table 2. CRU Bit Assignments

CRU Bit	S_0	S_1	S_2	S_3	S_4	CRU Read Data	CRU Write Data
0	0	0	0	0	0	CONTROL BIT(1)	CONTROL BIT(1)
1	0	0	0	0	1	$\overline{INT}_1/CLK_1$(2)	Mask $1/CLK_1$(3)
2	0	0	0	1	0	$\overline{INT}_2/CLK_2$	Mask $2/CLK_2$
3	0	0	0	1	1	$\overline{INT}_3/CLK_3$	Mask $3/CLK_3$
4	0	0	1	0	0	$\overline{INT}_4/CLK_4$	Mask $4/CLK_4$
5	0	0	1	0	1	$\overline{INT}_5/CLK_5$	Mask $5/CLK_5$
6	0	0	1	1	0	$\overline{INT}_6/CLK_6$	Mask $6/CLK_6$
7	0	0	1	1	1	$\overline{INT}_7/CLK_7$	Mask $7/CLK_7$
8	0	1	0	0	0	$\overline{INT}_8/CLK_8$	Mask $8/CLK_8$
9	0	1	0	0	1	$\overline{INT}_9/CLK_9$	Mask $9/CLK_9$
10	0	1	0	1	0	$\overline{INT}_{10}/CLK_{10}$	Mask $10/CLK_{10}$
11	0	1	0	1	1	$\overline{INT}_{11}/CLK_{11}$	Mask $11/CLK_{11}$
12	0	1	1	0	0	$\overline{INT}_{12}/CLK_{12}$	Mask $12/CLK_{12}$
13	0	1	1	0	1	$\overline{INT}_{13}/CLK_{13}$	Mask $13/CLK_{13}$
14	0	1	1	1	0	$\overline{INT}_{14}/CLK_{14}$	Mask $14/CLK_{14}$
15	0	1	1	1	1	$\overline{INT}_{15}/\overline{INTREQ}$	Mask $15/\overline{RST}_2$(4)
16	1	0	0	0	0	P_0 INPUT(5)	P_0 Output(6)
17	1	0	0	0	1	P_1 Input	P_1 Output
18	1	0	0	1	0	P_2 Input	P_2 Output
19	1	0	0	1	1	P_3 Input	P_3 Output
20	1	0	1	0	0	P_4 Input	P_4 Output
21	1	0	1	0	1	P_5 Input	P_5 Output
22	1	0	1	1	0	P_6 Input	P_6 Output
23	1	0	1	1	1	P_7 Input	P_7 Output
24	1	1	0	0	0	P_8 Input	P_8 Output
25	1	1	0	0	1	P_9 Input	P_9 Output
26	1	1	0	1	0	P_{10} Input	P_{10} Output
27	1	1	0	1	1	P_{11} Input	P_{11} Output
28	1	1	1	0	0	P_{12} Input	P_{12} Output
29	1	1	1	0	1	P_{13} Input	P_{13} Output
30	1	1	1	1	0	P_{14} Input	P_{14} Output
31	1	1	1	1	1	P_{15} Input	P_{15} Output

NOTES:

(1) 0 = Interrupt Mode 1 = Clock Mode

(2) Data present on INT input pin (or clock value) will be read regardless of mask value.

(3) While in the Interrupt Mode (Control Bit = 0) writing a "1" into mask will enable interrupt; a "0" will disable.

(4) Writing a zero to bit 15 while in the clock mode (Control Bit = 1) executes a software reset of the I/O pins.

(5) Data present on the pin will be read. Output data can be read without affecting the data.

(6) Writing data to the port will program the port to the output mode and output the data.

Figure 2. Interrupt Control Logic

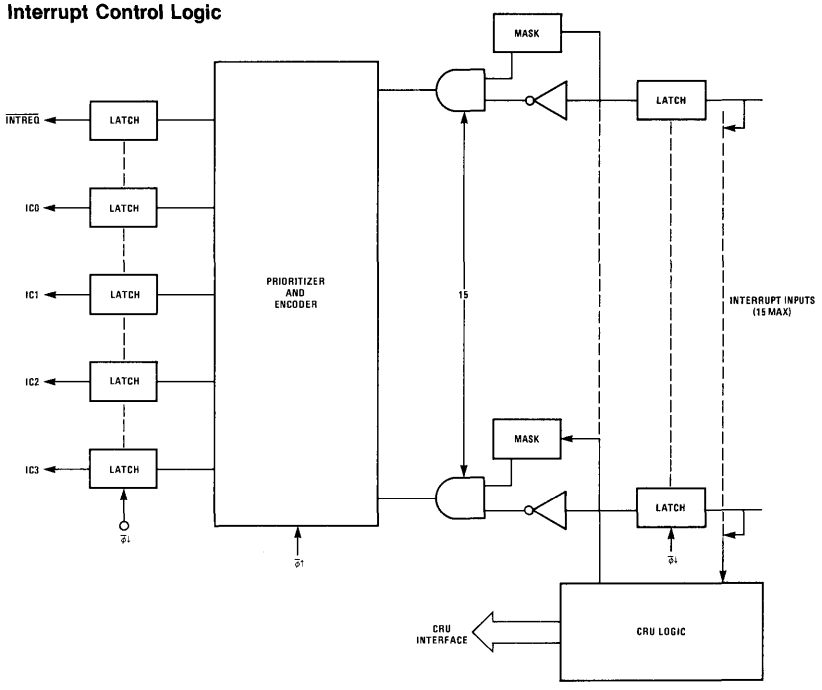


Table 3. Interrupt Code Generation

Interrupt/State	Priority	IC_0	IC_1	IC_2	IC_3	$\overline{INTREQ}$
$\overline{INT}_1$	1 (HIGHEST)	0	0	0	1	0
$\overline{INT}_2$	2	0	0	1	0	0
$\overline{INT}_3$/CLOCK	3	0	0	1	1	0
$\overline{INT}_4$	4	0	1	0	0	0
$\overline{INT}_5$	5	0	1	0	1	0
$\overline{INT}_6$	6	0	1	1	0	0
$\overline{INT}_7$	7	0	1	1	1	0
$\overline{INT}_8$	8	1	0	0	0	0
$\overline{INT}_2$	2	0	0	1	0	0
$\overline{INT}_9$	9	1	0	0	1	0
$\overline{INT}_{10}$	10	1	0	1	0	0
$\overline{INT}_{11}$	11	1	0	1	1	0
$\overline{INT}_{12}$	12	1	1	0	0	0
$\overline{INT}_{13}$	13	1	1	0	1	0
$\overline{INT}_{14}$	14	1	1	1	0	0
$\overline{INT}_{15}$	15 (LOWEST)	1	1	1	1	0
NO INTERRUPT	—	1	1	1	1	1

Programmable Real Time Clock

A block diagram of the programmable real time clock section is shown in Figure 4. The clock consists of a 14-bit counter that decrements at a rate of F(ϕ)64 (at 3MHz this results in a maximum interval of 349ms with a resolution of 21.3μs) and can be used as either an interval timer or as an event timer.

The clock is accessed by writing a one into the control bit (address 0) to force CRU bits 1-15 to clock mode (See Table 1). Writing a nonzero value into the clock register then enables the clock and sets its frequency. During system set up this entire operation can be accomplished with one additional I/O instruction (LCDR) as shown in Table 4. The clock functions as an interval timer by decrementing to zero, issuing an interrupt, and restarting at the programmed start value. When the clock interrupt is active, the clock mask (mask bit 3) must be written into (with either a "1' or a "0") to clear the interrupt.

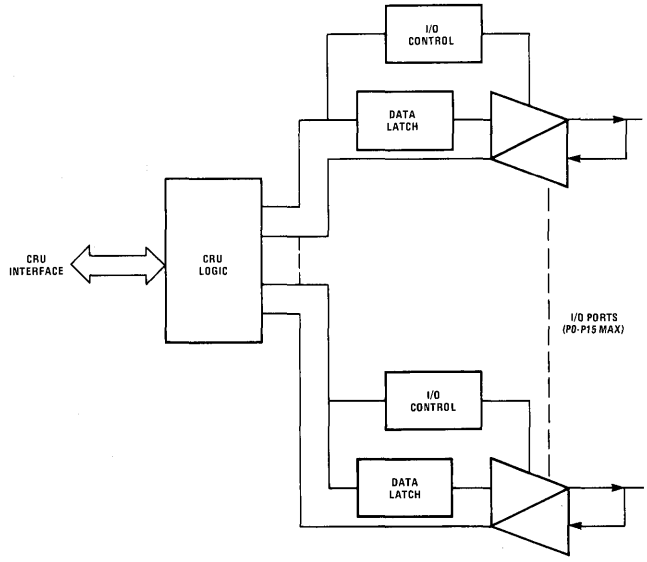
If a value other than that initially progammed is required, a new 14-bit clock start value is similarly programmed by executing a CRU write operation to the same locations. During programming the decrementer is restarted with the current start value after each start value bit is written. A timer restart can be easily implemented by writing a single bit to any of the clock bits.

The clock is disabled by $\overline{RST}_1$ (power-up-clear) or by writing a zero value into the clock register. Enabling the clock programs the third priority interrupt ($\overline{INT}_3$) as the clock interrupt and disables generation of interrupts from the $\overline{INT}_3$ input pin. When accessing the clock, all interrupts should be disabled to ensure that system integrity is maintained.

The clock can also function as an event timer since whenever the device is switched to the clock mode, by writing a one to the control bit, the current value of the clock is stored in the clock read register. Reading this value, and thus the elapsed event time, is accomplished by executing a 14-bit CRU read operation (addresses 1-14). The software example (Table 3) shows a read of the event timer.

The current status of the machine can always be obtained by reading the control (address zero) bit. A "0" indicates the machine is in an interrupt mode. Bits 1

Figure 3. I/O Interface



through 15 would normally be the interrupt input lines in this mode, but if any are not needed for interrupts, they may also be read with a CRU input command and interpreted as normal data inputs. A "1" read on the control bit indicates that the 9901 is in the clock mode. Reading bits 1 through 14 completes the event timer operation as described above. Reading bit 15 indicates whether the interrupt request line is active.

A software reset $\overline{RST}_2$ can be performed by writing a "1" to the control bit followed by writing a "1" to bit 15, which forces all I/O ports to the input mode.

Table 4. Software Examples

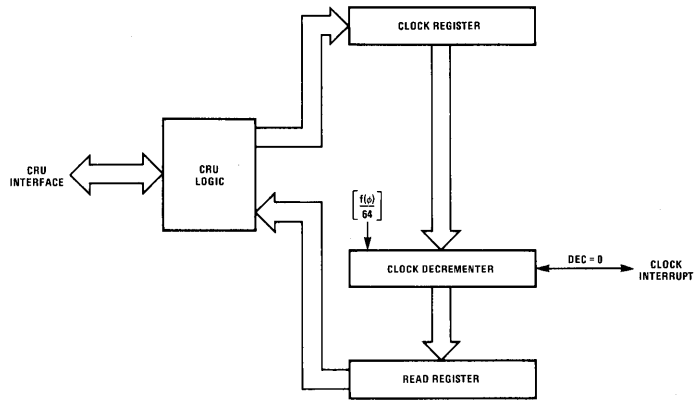
Assumptions

—System uses clock at maximum interval
—Total of 6 interrupts are used
—8 bits are used as output port
—8 bits are used as input port
—RST_1 (power up reset) has already been applied

System Setup for Interrupt	LI	R12,PSIBAS	Setup CRU Base Address to point 9901
	LDCR	@X,0	Program Clock with maximum interval
	LDCR	@Y,7	Re-enter interrupt mode and enable top 6 interrupts
System Setup for Output Ports	LI	R12,PSIBAS+16	Move CRU Base to point I/O port
	LDCR	R1,8	Move most significant byte of R_1 to output port
Read Programmed Inputs	LI	R12,PSIBAS+24	Move CRU Base to point to input ports
	STCR	R2,8	Move input port to most significant byte of R2
	(X) ⟶ FFFF		
	(Y) ⟶ 7FXX		
		Don't cares	
	BLWP	CLKVCT	Save Interrupt Mask
	•		
	•		
	•		
CLKPC	LIMI	0	Disable INTERRUPTS
	LI	R12,PSIBAS+1	Set up CRU Base
	SBO	−1	Set 9901 into Clock Mode, Latch Clock Value
	STCR	R4,14	Store Read Register Latch Value into R_4
	SBZ	−1	Reenter Interrupt Mode and Restarting Clock
	RTWP		Restore Interrupt Mask
	○		
	•		
	•		
CLKVCT	DATA	CLKWP, CLKPC	

S9900 FAMILY

Figure 4. Real Time Clock



System Operation

During power up, $\overline{RST}_1$ must be activated (low) for a minimum of 2 clock cycles to force the S9901 into a known state. $\overline{RST}_1$ will disable all interrupts, disable the clock, program all I/O ports to the mode, and force IC_0-IC_3 to (0,0,0,0) with $\overline{INTREQ}$ held high. System software must then enable the proper interrupts, program the clock (if used), and configure the I/O ports as required (see Table 4 for an example). After initial power up, the S9901 will be accessed only as needed to service the clock, enable (disable) interrupts, or read (write) data to the I/O ports. The I/O ports can be reconfigured by use of the $\overline{RST}_2$ command bit.

Figure 5 illustrates the use of an S9901 with an S9900. The S9904 is used to generate RST to reset the 9900 and the 9901 (connected to $\overline{RST}_1$). Figure 6 shows an S9980 system using the S9901. The reset function, load interrupt, and 4 maskable interrupts allowed in a 9980 are encoded as shown in Table 5. Connecting the system as shown ensures that the proper reset will be applied to the 9980.

Table 5. 9980 Interrupt Level Data

Interrupt Code (IC_0-IC_2)	Function	Vector Location (Memory Address In Hex)	Device Assignment	Interrupt Mask Values To Enable (ST_{12} through ST_{15})
1 1 0	Level 4	0 0 1 0	External Device	4 Through F
1 0 1	Level 3	0 0 0 C	External Device	3 Through F
1 0 0	Level 2	0 0 0 8	External Device	2 Through F
0 1 1	Level 1	0 0 0 4	External Device	1 Through F
0 0 1	Reset	0 0 0 0	Reset Stimulus	Don't Care
0 1 0	Load	3 F F C	Load Stimulus	Don't Care
0 0 0	Reset	0 0 0 0	Reset Stimulus	Don't Care
1 1 1	No-Op	—	—	Don't Care

Figure 5. S9900-S9901 Interface

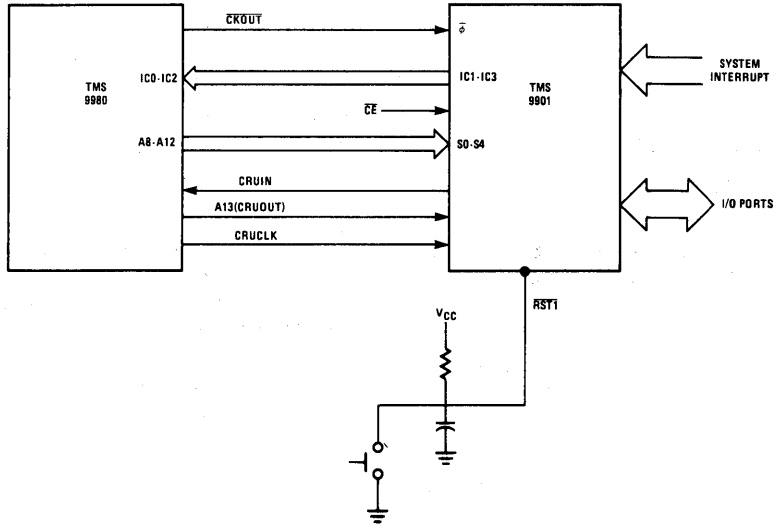
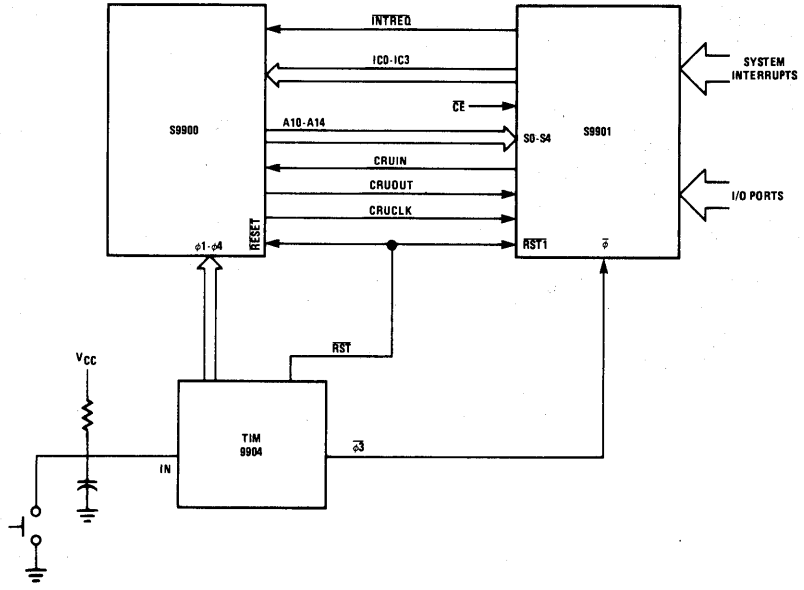


Figure 6. S9980-S9901 Interface



A Subsidiary of Gould Inc.

Advanced Product Description **S9902/S9902-4**

ASYNCHRONOUS COMMUNICATIONS CONTROLLER (ACC)

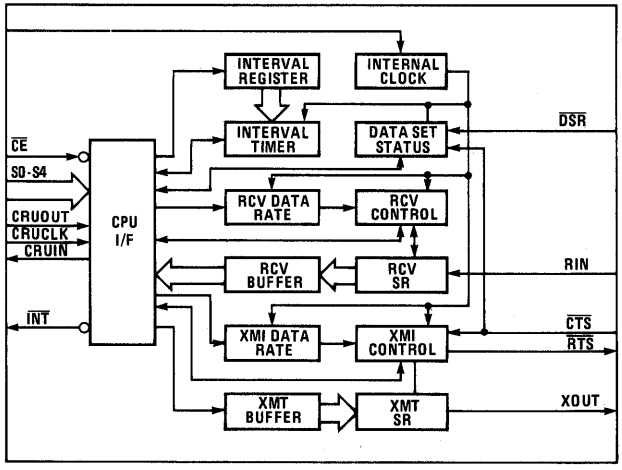
Features

- ☐ 5- to 8-Bit Character Length
- ☐ 1, 1½, or 2 Stop Bits
- ☐ Even, Odd, or No Parity
- ☐ Fully Programmable Data Rate Generation
- ☐ Interval Timer with Resolution from 64 to 16,320 μs
- ☐ Fully TTL Compatible, Including Single Power Supply

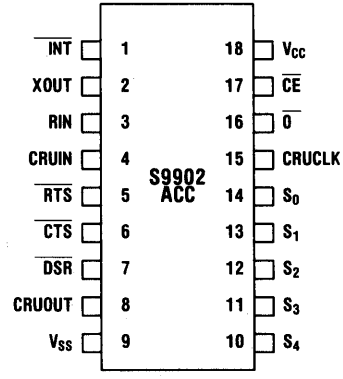
General Description

The S9902 Asynchronous Communication Controller (ACC) is a peripheral device for the S9900 family of microprocessors. The ACC provides an interface between the microprocessor and a serial asynchronous communication channel, performing the timing and data serialization and deserialization, thus facilitating the control of the asynchronous channel by the microprocessor.

Block Diagram



Pin Configuration



S9902 Electrical Specifications

Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply Voltage, V_{CC}	−0.3V to +10V
All Input and Output Voltages	−0.3V to +10V
Continuous Power Dissipation	0.7W
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_{SS}		0		V
High-Level Input Voltage, V_{IH}	2.2	2.4	V_{CC}	V
Low-Level Input Voltage, V_{IL}		0.4	0.8	V
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics

Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_I	Input Current (Any Input)			±10	μA	V_I = 0V to V_{CC}
V_{OH}	High Level Output Voltage	2.2 2.0	3.0 2.5		V	I_{OH} = 100μA I_{OH} = −400μA
V_{OL}	Low Level Output Voltage		0.4	0.85	V	I_{OL} = 3.2mA
$I_{CC(AV)}$	Average Supply Current from V_{CC}		2.5	100	mA	$t_{C(0)}$ = 250ns, T_A = 25°C
C_i C_o	Capacitance, Any Input Capacitance, Any Output		10 20		pF	f = 1MHz, All other pins at 0V

Timing Requirements

Over Full Range of Operating Conditions

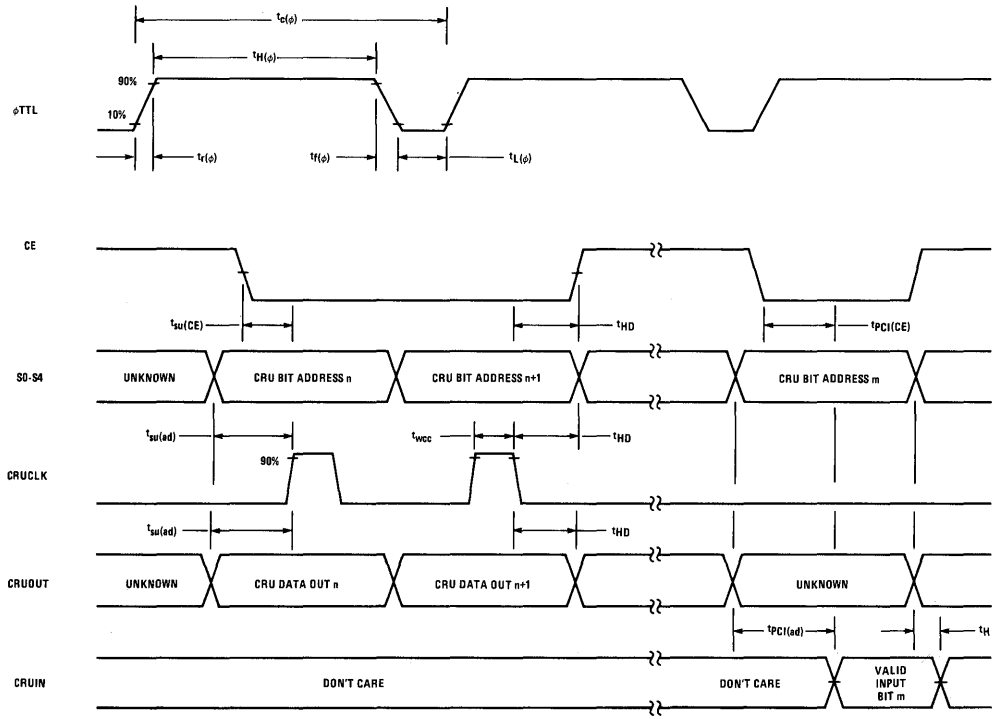
Symbol	Parameter	S9902			S9902-4			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{C(0)}$	Clock Cycle Time	300	333	2000	240	250	667	ns
$t_{r(0)}$	Clock Rise Time	5	10	12	8		40	ns
$t_{f(0)}$	Clock Fall Time	225	10	12	10		40	ns
$t_{H(0)}$	Clock Pulse Low Width (High Level)		225	240	180			ns
$t_{L(0)}$	Clock Pulse Width (Low Level)	45	45	55	40			ns
tsu(ad)	Setup Time for Address and CRU_{OUT} Before CRU_{CLK}	180	220		150	150		ns
$t_{su(CE)}$	Setup Time for CE Before CRU_{CLK}	100	185		110	110		ns
t_{HD}	Hold Time for Address, CE and CRU_{OUT} After CRU_{CLK}	60	90		50	50		ns
twcc	CRU_{CLK} Pulse Width	100	120		80			ns

Switching Characteristics

Over Full Range of Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{PCI(cd)}$	Propagation Delay, Address-to-Valid CRU_{IN}			400	ns	$C_L = 100pF$,
$t_{PCI(CE)}$	Propagation Delay, $\overline{CE}$-to-Valid CRU_{IN}			400	ns	$C_L = 100pF$
t_H	CRU_{IN} Hold Time After Address			20	ns	

Figure 3. Switching Characteristics



S9902 Pin Description

Table 1 defines the S9902 pin assignments and describes the function of each pin as shown on page 1.

Table 1.

Signature	Pin	I/O	Description
$\overline{INT}$	1	O	Interrupt—when active (low), the $\overline{INT}$ output indicates that at least one of the interrupt conditions has occurred.
X_{OUT}	2	O	Transmitter serial data output line—X_{OUT} remains inactive (high) when S9902 is not transmitting.
RIN	3	I	Receiver serial data input line—RCV—must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receiver circuitry.
CRU_{IN}	4	O	Serial data output pin from S9902 to CRU_{IN} input pin of the CPU.
$\overline{RTS}$	5	O	Request-to-send output from S9902 to modem. This output is enabled by the CPU and remains active (low) during transmission from the S9902.
$\overline{CTS}$	6	I	Clear-to-send input from modem to S9902. When active (low), it enables the transmitter section of S9902.
$\overline{DSR}$	7	I	Data set ready intput from modem to S9902. This input generates an interrupt when going On or Off.
CRU_{OUT}	8	I	Serial data input line to S9902 from CRU_{OUT} line of the CPU.
V_{SS}	9	I	Ground reference voltage.
S_4 (LSB)	10	I	
S_3	11	I	
S_2	12	I	
S_1	13	I	Address bus S_0-S_4 are the lines that are addressed by the CPU to select a particular S9902 function.
S_0	14	I	
CRU_{CLK}	15	I	CRU Clock. When active (high), S9902 from CRU_{OUT} line of the CPU.
ϕ	16	I	TTL Clock.
CE	17	I	Chip enable—when CE is inactive (high), the S9902 address decoding is inhibited which prevents execution of any S9902 command function. CRU_{IN} remains at high-impedance when $\overline{CE}$ is inactive (high).
V_{CC}	18	I	Supply voltage (+5V nominal).

Device Interface

The relationship of the ACC to other components in the system is shown in Figures 2 and 3. The ACC is connected to the asynchronous channel through level shifters which translate the TTL inputs and outputs to the appropriate levels (e.g., RS-232C, TTY current loop, etc.). The microprocessor transfers data to and from the ACC via the Communication Register Unit (CRU).

CPU Interface

The ACC interfaces to the CPU through the Communication Register Unit (CRU). The CRU interface consists of five address-select lines (S_0-S_4), chip enable (CE), and three CRU control lines (CRU_{IN}, CRU_{OUT}, and CRU_{CLK}). When $\overline{CE}$ becomes active (low), the five select lines address the CRU bit being accessed. When data is being transferred to the ACC from the CPU, CRU_{OUT} contains the valid datum which is strobed by CRU_{CLK}. When ACC data is being read, CRU_{IN} is the datum output by the ACC.

Figure 4. S9902 ACC in a S9900 System

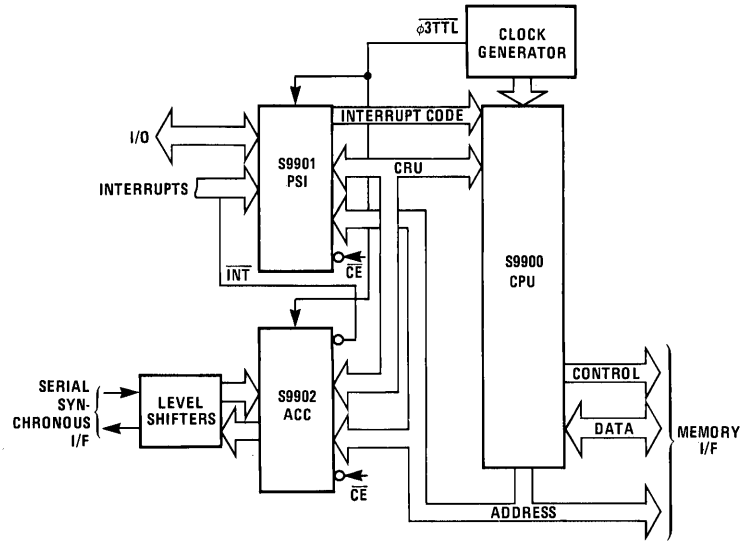
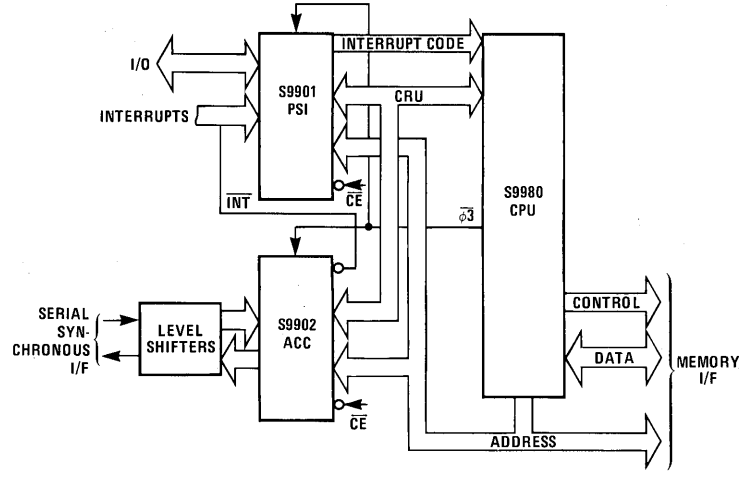


Figure 5. S9902 ACC in a S9980 System



Asynchronous Communication Channel Interface

The interface to the asynchronous communication channel consists of an output control line ($\overline{RTS}$), two input status lines ($\overline{DSR}$ and $\overline{CTS}$), and serial transmit (X_{OUT}) and receive (RIN) data lines. The request-to-send line ($\overline{RTS}$) is active (low) whenever the transmitter is activated. However, before data transmission begins, the clear-to-send ($\overline{CTS}$) input must be active. The data set ready ($\overline{DSR}$) input does not affect the receiver or transmitter. When $\overline{DSR}$ or $\overline{CTS}$ changes level, an interrupt is generated.

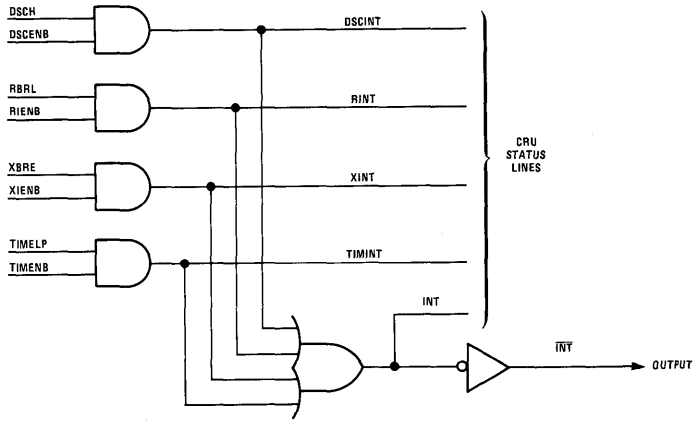
Interrupt Output

The interrupt output ($\overline{INT}$) is active (low) when any of the following conditions occurs and the corresponding interrupt has been enabled by the CPU:

(1) $\overline{DSR}$ or $\overline{CTS}$ changes levels (DSCH = 1);
(2) a character has been received and stored in the Receiver Buffer Register (RBRL = 1);
(3) the Transmit Buffer Register is empty (XBRE = 1); or
(4) the selected time interval has elapsed (TIMELP = 1).

The logical relationship of the interrupt output is shown below.

$\overline{INT}$ Output Generation



Clock Input

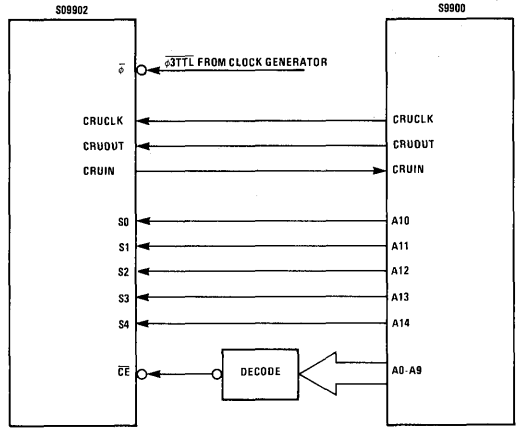
The clock input to the ACC ($\overline{\phi}$) is normally provided by the $\overline{\phi 3}$ output of the clock generator (9900 systems) or the S9980 (9980 systems). This clock input is used to generate the internal device clock, which provides the time base for the transmitter, receiver, and interval timer of the ACC.

Device Operation

Control and Data Output

Data and control information is transferred to the ACC using $\overline{CE}$, S_0-S_4, CRU_{OUT}, and CRU_{CLK}. The diagrams on page 7 show the connection of the ACC to the S9900 and S9980 CPUs. The high-order CPU address lines are used to decide the $\overline{CE}$ signal when the device is being selected. The low-order address lines are connected to the five address-select lines (S_0-S_4). Table 2 describes the output bit address assignments for the ACC.

Connection of the ACC to the S9900



Connection of the ACC to the S9980 CPU's

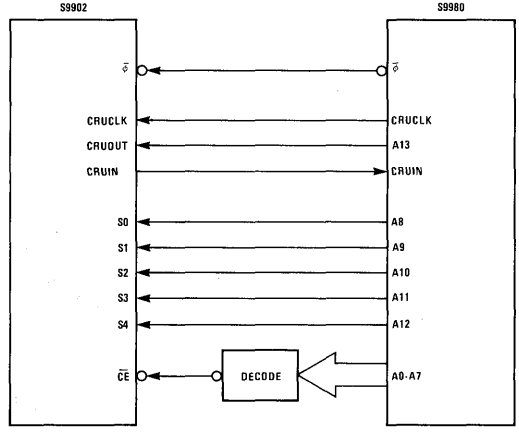


Table 2. S9902 ACC Output Bit Address Assignments

$Address_2$ S_0	S_1	S_2	S_3	S_4	$Address_{10}$	Name	Description
1	1	1	1	1	31	RESET	Reset Device
					30-22		Not used
1	0	1	0	1	21	DSCENB	Data Set Status Change Interrupt Enable
1	0	1	0	0	20	TIMENB	Timer Interrupt Enable
1	0	0	1	1	19	XBIENB	Transmitter Interrupt Enable
1	0	0	1	0	18	RIENB	Receiver Interrupt Enable
1	0	0	0	1	17	BRKON	Break On
1	0	0	0	0	16	RTSON	Request to Send On
0	1	1	1	1	15	TSTMD	Test Mode
0	1	1	1	0	14	LDCTRL	Load Control Register
0	1	1	0	1	13	LDIR	Load Interval Register
0	1	1	0	0	12	LRDR	Load Receiver Data Rate Register
0	1	0	1	1	11	LXDR	Load Transmit Data Rate Register
					10-0		Control, Interval, Receive Data Rate, Transmit Data Rate, and Transmit Buffer Registers

Bit 31 (RESET) — Writing a one or zero to Bit 31 causes the device to be reset, disabling all interrupts, initializing the transmitter and receiver, setting $\overline{RTS}$ inactive (high), setting all register load control flags (LDCTRL, LDIR, LRDR, and LXDR) to a logic one level, and resetting the BREAK flag. No other input or output operations should be performed for 11Ø clock cycles after issuing the RESET command.

Bit 30-Bit 22 — Not used.

Bit 21 (DSCENB) — Data Set Change Interrupt Enable. Writing a one to Bit 21 causes the $\overline{INT}$ output to be active (low) whenever DSCH (Data Set Status Change) is a logic one. Writing a zero to Bit 21 causes DSCH interrupts to be disabled. Writing either a one or zero to Bit 21 causes DSCH to be reset.

Bit 20 (TIMENB) — Timer Interrupt Enable. Writing a one to Bit 20 causes the $\overline{INT}$ output to be active whenever TIMELP (Timer Elapsed) is a logic one. Writing a zero to Bit 20 causes TIMELP interrupts to be disabled. Writing either a one or zero to Bit 20 causes TIMELP and TIMERR (Timer Error) to be reset.

Bit 19 (XBIENB) — Transmit Buffer Interrupt Enable. Writing a one to Bit 19 causes the $\overline{INT}$ output to be active whenever XBRE (Transmit Buffer Register Empty) is a logic one. Writing a zero to Bit 19 causes XBRE interrupts to be disabled. The state of XBRE is not affected by writing to Bit 19.

Bit 18 (RIENB) — Receiver Interrupt Enable. Writing a one to Bit 18 causes the $\overline{INT}$ output to be active whenever RBRL (Receiver Buffer Register Loaded) is a logic one. Writing a zero to Bit 18 disables RBRL interrupts. Writing either a one or zero to Bit 18 causes RBRL to be reset.

Bit 17 (BRKON) — Break On. Writing a one to Bit 17 causes the XOUT (Transmitter Serial Data Output) to go to a logic zero whenever the transmitter is active and the Transmit Buffer Register (XBR) and the Transmit Shift Register (XSR) are empty. While BRKON is set, loading of characters into the XBR is inhibited. Writing a zero to Bit 17 causes BRKON to be reset and the transmitter to resume normal operation.

Bit 16 (RTSON) — Request-to-Send On. Writing a one to Bit 16 causes the $\overline{RTS}$ output to be active (low). Writing a zero to Bit 16 causes $\overline{RTS}$ to go to a logic one after the XSR and XBR are empty, and BRKON is reset. Thus, the $\overline{RTS}$ output does not become inactive (high) until after character transmission has been completed.

Bit 15 (TSTMD) — Test Mode. Writing a one to Bit 15 causes $\overline{RTS}$ to be internally connected to $\overline{CTS}$, XOUT to be internally connected to RIN, $\overline{DSR}$ to be internally held low, and the Interval Timer to operate at 32 times its normal rate. Writing a zero to Bit 15 re-enables normal device operation.

Bit 14-11 — Register Load Control Flags. Output Bits 14-11 control which of the five registers will be loaded by writing to Bits 10-0. The flags are prioritized as shown in Table 3.

Table 3. S9902 ACC Register Load Selection

Register Load Control Flag Status				Register Enabled
LDCTRL	LDIR	LDR	LXDR	
1	X	X	X	Control Register
0	1	X	X	Interval Register
0	0	1	X	Receive Data Rate Register
0	0	X	1	Transmit Data Rate Register
0	0	0	0	Transmit Buffer Register

Bit 14 (LDCTRL) — Load Control Register. Writing a one to Bit 1 causes LDCTRL to be set to a logic one. When LDCTRL = 1, any data written to bits 0-7 are directed to the Control Register. Note that LDCTRL is also set to a logic one when a one or zero is written to Bit 31 (RESET). Writing a zero to Bit 14 causes LDCTRL to be reset to a logic zero, disabling loading of the Control Register. LDCTRL is also automatically reset to a logic zero when a datum is written to Bit 7 of the Control Register which normally occurs as the last bit written when loading the Control Register with a LDCR instruction.

Bit 13 (LDIR) — Load Interval Register, Writing a one to Bit 13 causes LDIR to be set to a logic one. When LDIR = 1 and LDCTRL = 0, any data written to Bits 0-7 are directed to the Interval Register. Note that LDIR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Interval Register loading is not enabled until LDCTRL is set to a logic zero. Writing a zero to Bit 13 causes LDIR to be reset to logic zero, disabling loading of the Internal Register. LDIR is also automatically reset to logic zero when a datum is written to Bit 7 of the Interval Register, which normally occurs as the last bit written when loading the Interval Register with a LDCR instruction.

Bit 12 (LRDR) — Load Receive Data Rate Register. Writing a one to Bit 12 causes LRDR to be set to a logic one. When LRDR = 1, LDIR = 0, and LDCTRL = 0, any data written to Bits 0-10 are directed to the Receive Data Rate Register. Note that LRDR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Receive Data Rate Register loading is not enabled until LDCTRL and LDIR have been set to a logic zero. Writing a zero to Bit 12 causes LRDR to be reset to a logic zero, disabling loading of the Receive Data Rate Register. LRDR is also automatically reset to logic zero when a datum is written to Bit 10 of the Receive Data Rate Register, which normally occurs as the last bit written when loading the Receive Data Rate Register with a LDCR instruction.

Bit 11 (LXDR) — Load Transmit Data Rate Register. Writing a one to Bit 11 causes LXDR to be set to a logic one. When LXDR = 1, LDIR = 0, and LDCTRL = 0, any data written to Bits 0-10 are directed to the Transmit Data Rate Register. Note that loading of both the Receive and Transmit Data Rate Registers is enabled when LDCTRL = 0, LDIR = 0, LRDR = 1, and LXDR = 1; thus these two registers may be loaded simultaneously when data are received and transmitted at the same rate. LXDR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Transmit Data Rate Register loading is not enabled until LDCTRL and LDIR have been reset to logic zero. Writing a zero to Bit 11 causes LXDR to be reset to logic zero, disabling loading of the Transmit Data Rate Register. Since Bit 11 is the next bit addressed after loading the Transmit Data Rate Register, the register may be loaded and the LXDR flag reset with a single LDCR instruction where 12 bits (Bits 0-11) are written, with a zero written to Bit 11.

Control Register

The Control Register is loaded to select character length, device clock operation, parity, and the number of stop bits for the transmitter. Table 4 shows the bit address assignments for the Control Register.

Table 4. Control Register Bit Address Assignments

Address$_{10}$	Name	Description
7	SBS1	Stop Bit Select
6	SBS2	
5	PENB	Parity Enable
4	PODD	Odd Parity Select
3	CLK4M	0 Input Divide Select
2	—	Not Used
1	RCL1	Character Length Select
0	RCL0	

7	6	5	4	3	2	1	0
SBS1	SBS2	PENB	PODD	CLK4M	NOT USED	RCL1	RCL0
MSB							LSB

Bits 7 and 6 (SBS1 and SBS2) — Stop Bit Selection. The number of stop bits to be appended to each transmitter character is selected by Bits 7 and 6 of the Control Register as shown below. The receiver only tests for a single stop bit, regardless of the status of Bits 7 and 6.

Stop Bit Selection

SBS1 Bit 7	SBS2 Bit 6	Number of Transmitted Stop Bits
0	0	1½
0	1	2
1	0	1
1	1	1

Bits 5 and 4 (PENB and PODD) — Parity Selection. The type of parity to be generated for transmission and detected for reception is selected by Bits 5 and 4 of the Control Register as shown below. When parity is enabled (PENB = 1), the parity bit is transmitted and received in addition to the number of bits selected for the character length. Odd parity is such that the total number of ones in the character and parity bit, exclusive of stop bit(s), will be odd. For even parity, the total number of ones will be even.

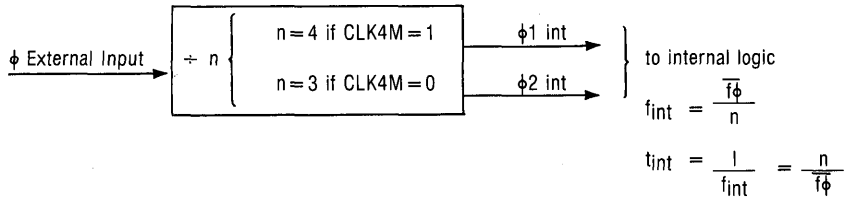
Parity Selection

PENB Bit 5	PODD Bit 4	PARITY
0	0	None
0	1	None
1	0	Even
1	1	Odd

Bit 3 (CLK4M) — ϕ Input Divide Select. The ϕ input to the S9902 ACC is used to generate internal dynamic logic clocking and to establish the time base for the Interval Timer, Transmitter and Receiver. The ϕ input is internally divided by either 3 or 4 to generate the two-phase internal clocks required for MOS logic, and to establish

the basic internal operating frequency (f_{int}) and internal clock period (t_{int}). When Bit 3 of the Control Register is set to a logic one (CLK4M = 1), ϕ is internally divided by 4, and when CLK4M = 0, ϕ is divided by 3. For example, when $f\phi = 3MHz$, as in a standard 3MHz S9900 system, and CLK4M = 0, ϕ is internally divided by 3 to generate an internal clock period t_{int} of 1μs. The figure below shows the operation of the internal clock divider circuitry. The internal clock frequency should be no greater than 1. 1MHz; thus, when $f\phi > 3.3MHz$, CLK4M should be set to a logic one.

Internal Clock Divider Circuitry



Bits 1 and 0 (RCL_1 and RCL_0) — Character Length Select. The number of data bits in each transmitted and received character is determined by Bits 1 and 0 of the Control Register as shown below.

Character Length Selection

RCL1 Bit 1	RCL0 Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Interval Register

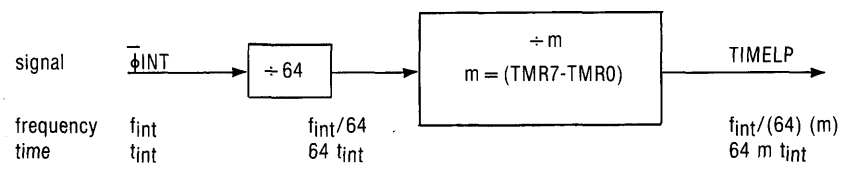
The Interval Register is enabled for loading whenever LDCTRL = 0 and LDIR = 1. The Interval Register is used for selecting the rate at which interrupts are generated by the Interval Timer of the ACC. The figure below shows the bit address assignments for the Interval Register when enabled for loading.

Interval Register Bit Address Assignments

7	6	5	4	3	2	1	0
TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
MSB							LSB

The figure below illustrates the establishment of the interval for the Interval Timer. As an example, if the Interval Register is loaded with a value of 80_{16} (128_{10}) the interval at which Timer Interrupts are generated is $t_{ITVL} = t_{int} \cdot 64 \cdot M = (1\mu s) (\cdot 64) (\cdot 128) = 8.192$ ms. when $t_{int} = 1\mu s$.

Time Internal Selection



Receive Data Rate Register

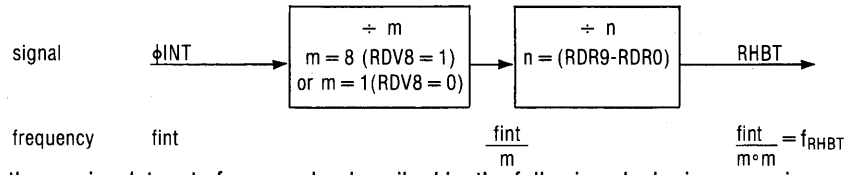
The Receive Data Rate Register is enabled for loading whenever LDCTRL = 0, LDIR = 0, and LRDR = 1. The Receive Data Rate Register is used for selecting the bit rate at which data is received. The diagram shows the bit address assignments for the Receive Data Rate Register when enabled for loading.

Receive Data Rate Register Bit Address Assignments

10	9	8	7	6	5	4	3	2	1	0
RDV8	RDR9	RDR8	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
MSB										LSB

The following diagram describes the manner in which the receive data rate is established. Basically, two programmable counters are used to determine the interval for one-half the bit period of receive data. The first counter either divides the internal system clock frequency (f_{int}) by either 8 (RDV8 = 1) or 1 (RDV8 = 0). The second counter has ten stages and may be programmed to divide its input signal by any value from 1 (RDR9-RDR0 = 0000000001) to 1023 (RDR8-RDR0 = 1111111111). The frequency of the output of the second counter (f_{RHBT}) is double the receive-data rate. Register is loaded with a value of 11000111000, RDV8 = 1, and RDR9-RDR0 = $1000111000 = 238_{16} = 568$ 10. Thus, for f_{int} = 1MHz, the receive-data rate = $1 \times 10^6 \div 8 \div 568 \div 2 = 110.04$ bits per second.

Receive Data Rate Selection



Quantitatively, the receive data rate f_{RCV} may be described by the following algebraic expression:

$$f_{RCV} = \frac{f_{RHBT}}{2} = \frac{f_{int}}{2mn} = \frac{f_{int}}{(2)\ (8^{RDV8})\ (RDR9\text{-}RDR0)}$$

Transmit Data Rate Register

The Transmit Data Rate Register is enabled for loading whenever LDCTRL = 0, LDIR = 0, and LXDR = 1. The Transmit Data Rate Register is used for selecting the data rate for the transmitter. The figure below shows the bit address assignments for the Transmit Data Rate Register.

10	9	8	7	6	5	4	3	2	1	0
XDV8	XDR9	XDR8	XDR7	XDR6	XDR5	XDR4	XDR3	XDR2	XDR1	XDR0
MSB										LSB

Selection of transmit data rate is accomplished with the Transmit Data Rate Register in the same way that the receive data rate is selected when the Receive Data Rate Register. The algebraic expression for the Transmit Data Rate f_{XMT} is:

$$f_{XMT} = \frac{f_{XHBT}}{2} = \frac{f_{int}}{(2)\ (8^{XDV8})\ (XDR9\text{-}XDR0)}$$

For example, if the Transmit Data Rate Register is loaded with a value of 00110100001, XDV8 = 0, and XDR9-XDR0 = $1A1_{16} = 417$, the transmit data rate = $1 \times 10^6 \div 2 \div 1 \div 417 = 1199.04$ bits per second.

Transmit Buffer Register

The Transmit Buffer Register is enabled for loading when LDCTRL = 0, LDIR = 0, LRDR = 0, LXDR = 0, and BRKON = 0. The Transmit Buffer Register is used for storage of the next character to be transmitted. When the transmitter is active, the contents of the Transmit Buffer Register are transferred to the Transmit Shift Register each time the previous character has been completely transmitted. The bit address assignments for the Transmit Buffer Register are shown below:

Transmit Buffer Register Bit Address Assignments

7	6	5	4	3	2	1	0
XBR7	XBR6	XBR5	XBR4	XBR3	XBR2	XBR1	XBR0
MSB							LSB

All 8 bits should be transferred into the register, regardless of the selected character length. The extraneous high-order bits will be ignored for transmission purposes; however, loading of bit 7 is internally detected to cause the Transmit Buffer Register Empty (XBRE) status flag to be reset.

Status and Data Input

Status and data information is read from the ACC using $\overline{CE}$, S_0-S_4, and CRU_{IN}. The following figure illustrates the relationship of the signals used to access data from the ACC. Table 6 describes the input bit address assignments for the ACC.

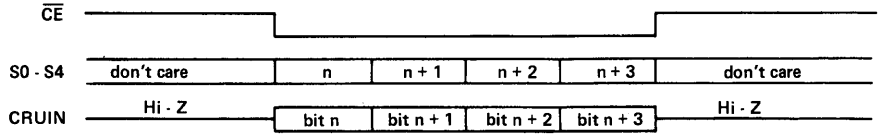


Table 5. CRU Output Bit Address Assignments

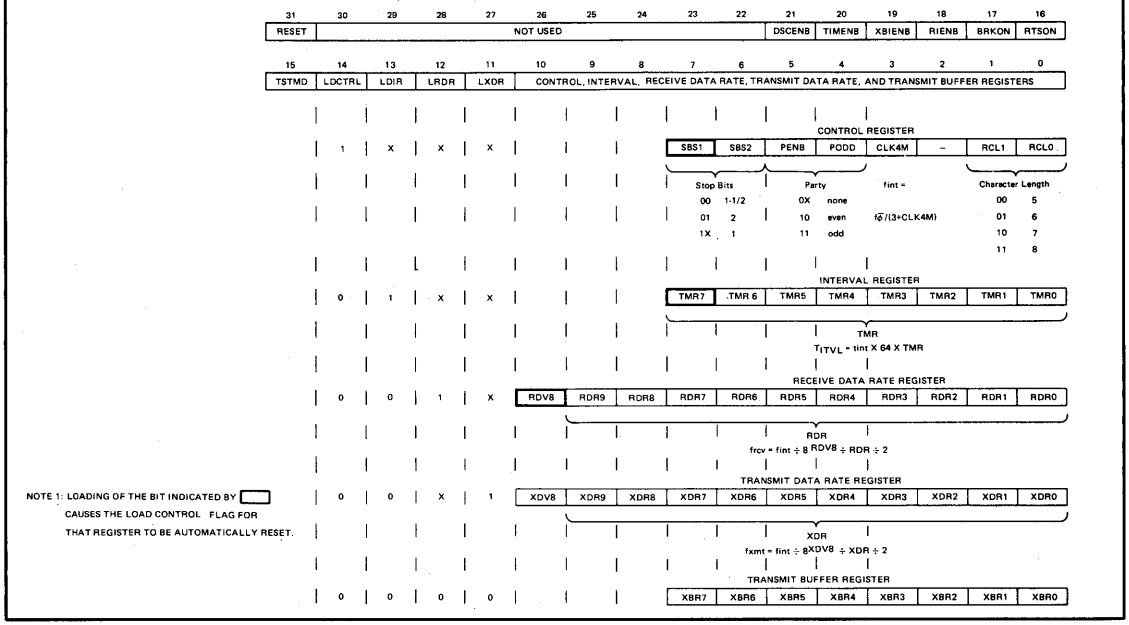


Table 6. S9902 ACC Input Bit Address Assignments

Address$_9$					Address$_{10}$	Name	Description
S_0	S_1	S_2	S_3	S_4			
1	1	1	1	1	31	INT	Interrupt
1	1	1	1	0	30	FLAG	Register Load Control Flag Set
1	1	1	0	1	29	DSCH	Data Set Status Change
1	1	1	0	0	28	CTS	Clear to Send
1	1	0	1	1	27	DSR	Data Set Ready
1	1	0	1	0	26	RTS	Request to Send
1	1	0	0	1	25	TIMELP	Timer Elapsed
1	1	0	0	0	24	TIMERR	Timer Error
1	0	1	1	1	23	XSRE	Transmit Shift Register Empty
1	0	1	1	0	22	XBRE	Transmit Buffer Register Empty
1	0	1	0	1	21	RBRL	Receive Buffer Register Loaded
1	0	1	0	0	20	DSCINT	Data Set Status Charge Interrupt (DSCH-DSCENB)
1	0	0	1	1	19	TIMINT	Timer Interrupt (TIMELP-TIMENB)
1	0	0	1	0	18	—	Not used (always = 0)
1	0	0	0	1	17	XBINT	Transmitter Interrupt (XBRE-XBIENB)
1	0	0	0	0	16	RBINT	Receiver Interrupt (RBRL-RIENB)
0	1	1	1	1	15	RIN	Receive Input
0	1	1	1	0	14	RSBD	Receive Start Bit Detect
0	1	1	0	1	13	RFBD	Receive Full Bit Detect
0	1	1	0	0	12	RFER	Receive Framing Error
0	1	0	1	1	11	ROVER	Receive Overrun Error
0	1	0	1	0	10	RPER	Receive Parity Error
0	1	0	0	1	9	RCVERR	Receive Error
0	1	0	0	0	8	—	Not used (always = 0)
					7-0	RBR7-RBR0	Receive Buffer Register (Received Data)

Bit 31 (INT) — INT = DSCINT + TIMINT + XBINT + RBINT. The interrupt output ($\overline{INT}$) is active when this status signal is a logic 1.

Bit 30 (FLAG) — FLAG = LDCTRL + LRDR + LXDR = BRKON. When any of the register load control flags or BRKON is set, FLAG = 1.

Bit 29 (DSCH) — Data Set Status Change Enable. DSCH is set when the $\overline{DSR}$ or $\overline{CTS}$ input changes state. To ensure recognition of the state change, $\overline{DSR}$ or $\overline{CTS}$ must remain stable in its new state for a minimum of two internal clock cycles. DSCH is reset by an output to bit 21 (DSCENB).

Bit 28 (CTS) — Clear to Send. The CTS signal indicates the inverted status of the $\overline{CTS}$ device input.

Bit 27 (DSR) — Data Set Ready. The DSR signal indicates the inverted status of the $\overline{DSR}$ device input.

Bit 26 (RTS) — Request to Send. The RTS signal indicates the inverted status of the $\overline{RTS}$ device output.

Bit 25 (TIMELP) — Timer Elapsed. TIMELP is set each time the Interval Timer decrements to 0. TIMELP is reset by an output to bit 20 (TIMENB).

Bit 24 (TIMERR) — Timer Error. TIMERR is set whenever the Interval timer decrements to 0 and TIMELP is already set, indicating that the occurrence of TIMELP was not recognized and cleared by the CPU before subsequent intervals elapsed. TIMERR is reset by an output to bit 20 (TIMENB).

Bit 23 (XSRE) — Transmit Shift Register Empty. When XSRE = 1, no data is currently being transmitted and the XOUT output is at logic 1 unless BRKON is set. When XSRE = 0, transmission of data is in progress.

Bit 22 (XBRE) — Transmit Buffer Register Empty. When XBRE = 1, the transmit buffer register does not contain the next character to be transmitted. XBRE is set each time the contents of the transmit buffer register are transferred to the transmit shift register. XBRE is reset by an output to bit 7 of the transmit buffer register (XBR7), indicating that a character has been loaded.

Bit 21 (RBRL) — Receive Buffer Register Loaded. RBRL is set when a complete character has been assembled in the receive shift register and the character is transferred to the receive buffer register. RBRL is reset by an output to bit 18 (RIENB).

Bit 20 (DSCINT) — Data Set Status Change Interrupt. DSCINT = DSCH (input bit 29) • DSCENB (output bit 21). DSCINT indicates the presence of an enabled interrupt caused by the changing of state of $\overline{\text{DRS}}$ or $\overline{\text{CTS}}$.

Bit 19 (TIMINT) — Timer Interrupt. TIMINT = TIMELP (input bit 25) • TIMENB (output bit 20). TIMINT indicates the presence of an enabled interrupt caused by the interval timer.

Bit 17 (XBINT) — Transmitter Interrupt. XBINT = XBRE (input bit 22) • XBIENB (output bit 19). XBINT indicates the presence of an enabled interrupt caused by the transmitter.

Bit 16 (RBINT) — Receiver Interrupt. RBINT = RBRL (input bit 21 • RIENB (output bit 18). RBINT indicates the presence of an enabled interrupt caused by the receiver.

Bit 15 (RIN) — Receive Input. RIN indicates the status of the RIN input to the device.

Bit 14 (RSBD) — Receive Start Bit Detect. RSBD is set one-half bit time after the 1-to-0 transition of RIN indicating the start bit of a character. If RIN is not still 0 at this point in time, RSBD is reset. Otherwise, RSBD remains true until the complete character has been received. This bit is normally used for testing purposes.

Bit 13 (RFBD) — Receive Full Bit Detect. RFBD is set one bit time after RSBD is set to indicate the sample point for the first data bit of the received character. RSBD is reset when the character has been completely received. This bit is normally used for testing purposes.

Bit 12 (RFER) — Receive Framing Error. RFER is set when a character is received in which the stop bit, which should be a logic 1, is a logic 0. RFER should only be read when RBRL (input bit 21) is a 1. RFER is reset when a character with a correct stop bit is received.

Bit 11 (ROVER) — Receive Overrun Error. ROVER is set when a new character is received before the RBRL flag (input bit 21) is reset, indicating that the CPU failed to read the previous character and reset RBRL before the present character is completely received. ROVER is reset when a character is received and RBRL is 0 when the character is transferred to the receive buffer register.

Bit 10 (RPER) — Receive Parity Error. RPER is set when a character is received in which the parity is incorrect. RPER is reset when a character with correct parity is received.

Bit 9 (RCVERR) — Receive Error. RCVERR = RFER + ROVER + RPER. RCVERR indicates the presence of an error in the most recently received character.

Bit 7-Bit 0 (RBR7-RBR0 — Receive Buffer Register. The receive buffer register contains the most recently received character. For character lengths of fewer than 8 bits the character is right justified, with unused most significant bit(s) all zero(es). The presence of valid data in the receive buffer register is indicated when RBRL is a logic 1.

Transmitter Operation

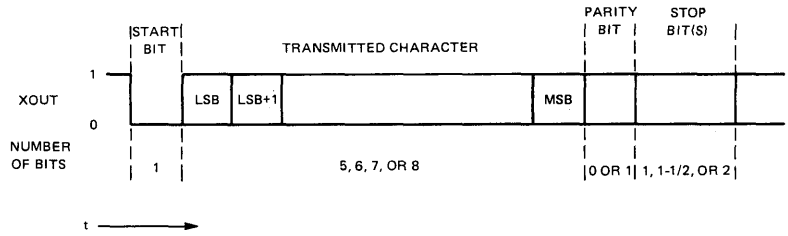
Transmitter Initialization

The operation of the transmitter is described in Figure 7. The transmitter is initialized by issuing the RESET command (output to bit 31), which causes the internal signals XSRE and XBRE to be set, and BRKON to be reset. Device outputs $\overline{RTS}$ and XOUT are set, placing the transmitter in its idle state. When RTSON is set by the CPU, the $\overline{RTS}$ output becomes active and the transmitter becomes active when $\overline{CTS}$ goes low.

Data Transmission

If the Transmit Buffer Register contains a character, transmission begins. The contents of the Transmit Buffer Register are transferred to the Transmit Shift Register, causing XSRE to be reset and XBRE to be set. The first bit transmitted (start bit) is always a logic 0. Subsequently, the character is shifted out, LSB first. Only the number of bits specified by RCL_1 and RCL_0 (character length select) of the Control Register are shifted. If parity is enabled, the correct parity bit is next transmitted. Finally the stop bit(s) selected by SBS_1 and SBS_0 of the Control Register are transmitted. Stop bits are always logic one. XSRE is set to indicate that no transmission is in progress, and the transmitter again tests XBRE to determine if the CPU has yet loaded the next character. The waveform for a transmitted character is shown below.

Transmitted Character Waveform



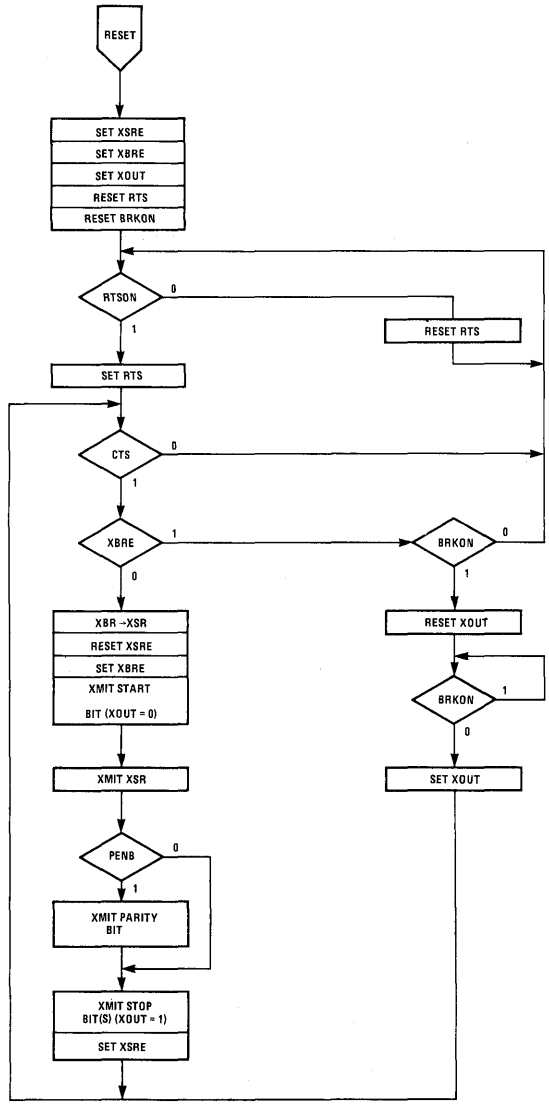
BREAK Transmission

The BREAK message is transmitted only if XBRE = 1, $\overline{CTS}$ = 9, and BRKON = 1. After transmission of the BREAK message begins, loading of the Transmit Buffer Register is inhibited and XOUT is reset. When BRKON is reset by the CPU, XOUT is set and normal operation continues. It is important to note that characters loaded into the Transmit Buffer Register are transmitted prior to the BREAK message regardless of whether the character has been loaded into the Transmit Shift Register before BRKON is set. Any character to be transmitted subsequent to transmission of the BREAK message may not be loaded into the Transmit Buffer Register until after BRKON is reset.

Transmission Termination

Whenever XSRE = 1 and BRKON = 0, the transmitter is idle, with XOUT set to one. If RTSON is reset at this time, the $\overline{RTS}$ device output will go inactive, disabling further data transmission until RTSON is again set. $\overline{RTS}$ will not go inactive, however, until any characters loaded into the Transmit Buffer Register prior to resetting RTSON are transmitted and BRKON = 0.

S9902 Transmitter Operation

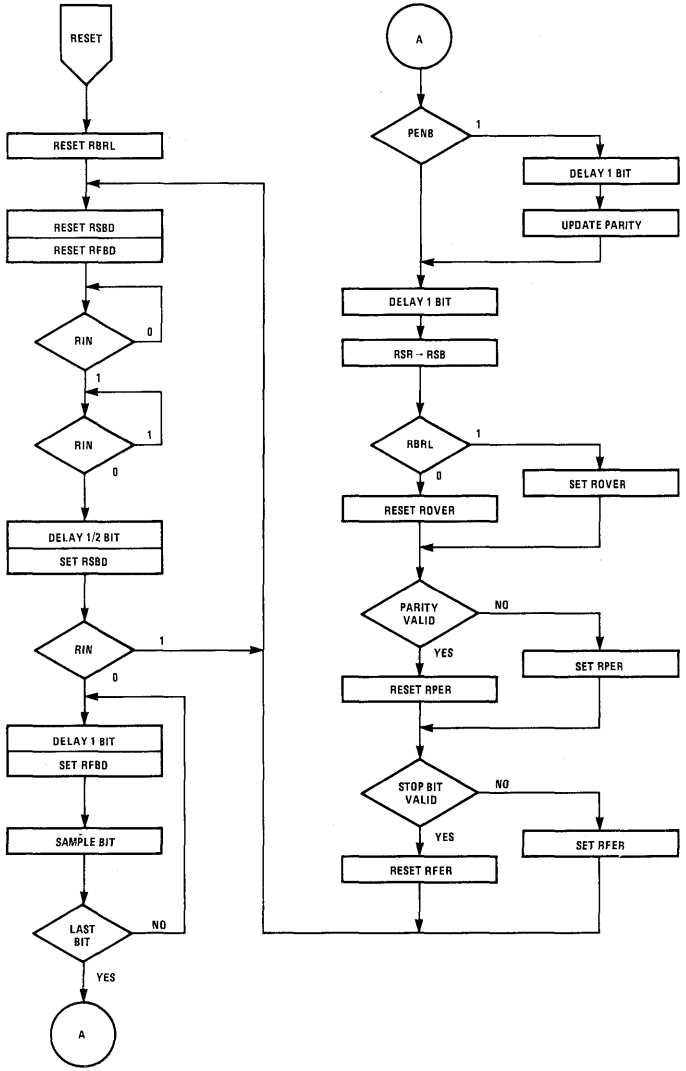


Receiver Operation

Receiver Initialization

Operation of the S9902 receiver is described in Figure 8. The receiver is initialized any time the CPU issues the RESET command. The RBRL flag is reset to indicate that no character is currently in the Receive Buffer Register, and the RSBD and RFBD flags are reset. The receiver remains in the inactive state until a 1 to 0 transition is detected on the RIN device input.

S9902 Receiver Operation



Start Bit Detection

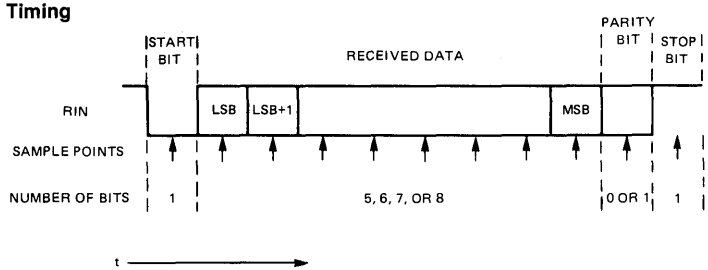
The receiver delays one-half bit time and again samples RIN to ensure that a valid start bit has been detected. If RIN = 0 after the half-bit delay, RSBD is set and data reception begins. If RIN = 1, no data reception occurs.

Data Reception

In addition to verifying the valid start bit, the half-bit delay after the 1-to-0 transition also establishes the sample point for all subsequent data bits in this character. Theoretically, the sample point is in the center of each bit cell, thus maximizing the limits of acceptable distortion of data cells. After the first full bit delay, the least significant data bit is received and RFBD is set. The receiver continues to delay one-bit intervals and sample RIN until the selected number of bits is received. If parity is enabled, one additional bit is read for parity. After an additional bit delay, the received character is transferred to the Receive Buffer Register, RBRL is set, ROVER and RPER are loaded with appropriate values, and RIN is tested for a valid stop bit. If RIN = 1, the stop bit is valid. RFER, RSBD, and RFBD are reset and the receiver waits for the next start bit to begin reception of the next character.

If RIN = 0 when the stop is sampled, RFER is set to indicate the occurrence of a framing error. RSBD and RFBD are reset but sampling for the start bit of the next character does not begin until RIN = 1.

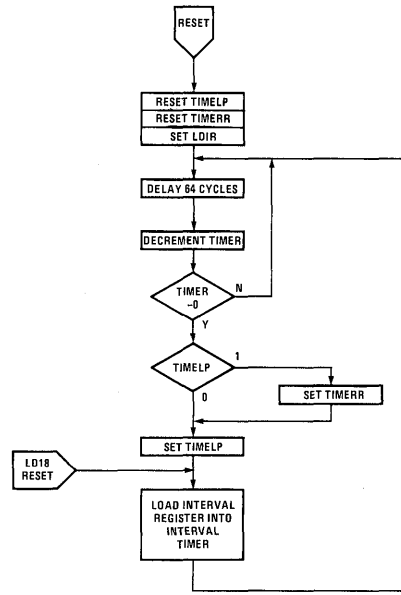
Character Reception Timing



Interval Timer Operation

A flowchart of the operation of the Interval Timer is shown in Figure 9. Execution of the RESET command by the CPU causes TIMELP and TIMERR to be reset and LDIR to be set. Resetting LDIR causes the contents of the Interval Register to be loaded into the Interval Timer, thus beginning the selected time interval. The timer is decremented every 64 internal clock cycles (every 2 internal clock cycles when in Test Mode) until it reaches zero, at which time the Interval Timer is reloaded by the Interval Register and TIMELP is set. If TIMELP was already set, TIMERR is set to indicate that TIMELP was not cleared by the CPU before the next time period elapsed. Each time LDIR is reset the contents of the Interval Register are loaded into the Interval Timer, thus restarting the time.

Interval Timer Operation



Device Application

This section describes the software interface between the CPU and the S9902 ACC and discusses some of the design considerations in the use of this device in asynchronous communications applications.

Device Initialization

The ACC is initialized by the CPU issuing the RESET command, followed by loading the Control, Interval, Receive Data Rate, and Transmit Data Rate registers. Assume that the value to be loaded into the CRU Base Register (register 12) in order to point to bit 0 is 0040_{16}. In this application, characters will have 7 bits of data plus even parity and one stop bit. The 0 input to the ACC is a 3MHz signal. The ACC will divide this signal frequency by 3 to generate an internal clock frequency of 1MHz. An interrupt will be generated by the Interval Timer every 1.6 milliseconds when timer interrupts are enabled. The transmitter will operate at a data rate of 300 bits per second and the receiver will operate at 1200 bits per second. Had it been desired that both the transmitter and receiver operate at 300 bits per second, the "LDCR @RDR,11" instruction would have been deleted, and the "LDCR @XDR,12" instruction would have caused both data rate registers to be loaded and LRDR and LXDR to have been reset.

Initialization Program

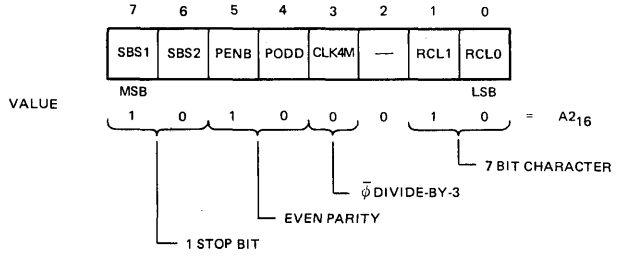
The initialization program for the configuration previously described is as shown below. The RESET command disables all interrupts, initializes all controllers, sets the four register load control flags (LDCTRL, LDIR, LRDR, and LXDR). Loading the last bits of each of the registers causes the load control flag to be automatically reset.

```
        LI      R12,>40     INITIALIZE CRU BASE
        SBO     31          RESET COMMAND
        LDCR    @CNTRL, 8   LOAD CONTROL AND RESET LDCTRL
        LDCR    @INTVL, 8   LOAD INTERVAL AND RESET LDIR
        LDCR    @RDR, 11    LOAD RDR AND RESET LRDR
        LDCR    @XDR, 12    LOAD XDR AND RESET LXDR
          •
          •
          •
CNTRL   BYTE    >A2
INTVL   BYTE    1600/64
RDR     DATA    >1A1
XDR     DATA    >4DO
```

The RESET command initializes all subcontrollers, disables interrupts, and sets LDCTRL, LDIR, LRDR, and LXDR, enabling loading of the control register.

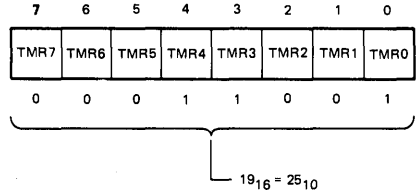
Control Register

The options described previously are selected by loading the value shown below.



Interval Register

The interval register is to be set up to generate an interrupt every 1.6 milliseconds. The value loaded into the interval register specifies the number of 64 microsecond increments in the total interval.



25 X 64 MICROSECONDS = 1.6 MILLISECONDS

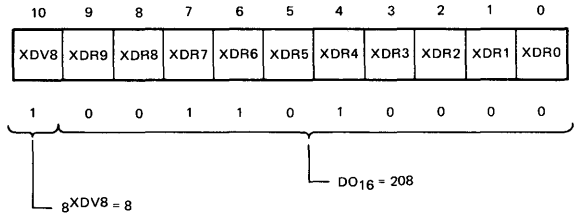
Receive Data Rate Register

The data rate for the receiver is to be 1200 bits per second. The value to be loaded into the Receive Data Rate Register is as shown:

$10^6 \div 1 \div 417 \div 2 = 1199.04$ BITS PER SECOND

Transmit Data Rate Register

The data rate for the transmitter is to be 300 bits per second. The value to be loaded into the Transmit Data Rate Register is:



$1 \times 10^6 \div 8 \div 208 \div 2 = 300.48$ BITS PER SECOND

Data Transmission

The subroutine shown below demonstrates a simple loop for the transmitting of a block of data.

```
        LI      R0, LISTAD      INITIALIZE LIST POINTER
        LI      R1, COUNT       INITIALIZE BLOCK COUNT
        LI      R12, CRUBAS     INITIALIZE CRU BASE
        SBO     16              TURN OFF TRANSMITTER
XMTLP   TB      22              WAIT FOR XBRE = 1
        JNE     XMTLP
        LDCR    *RO + ,8        LOAD CHARACTER INCREMENT POINTER RESET XBRE
        DEC     R1              DECREMENT COUNT
        JNE     XMTLP           LOOP IF NOT COMPLETE
        SBZ     16              TURN OFF TRANSMITTER
```

After initializing the list pointer, block count, and CRU base address, RTSON is set to cause the transmitter and the RTS output to become active. Data transmission does not begin, however, until the CTS input becomes active. After the final character is loaded into the transmit buffer register. RTSON is reset. The transmitter and the RTS output do not become inactive until the final character has been completely transmitted.

Data Reception

The software shown below will cause a block of data to be received and stored in memory.

```
CARRET  BYTE    >OD
RCVBLK  LI      R2, RCVLST      INITIALIZE LIST COUNT
        LI      R3, MXRCNT      INITIALIZE MAX COUNT
        LI      R4, CARRET      SET UP END OF BLOCK CHARACTER
RCVLP   TB      21              WAIT FOR RBRL = 1
        JNE     RCVLP
        STCR    *R2,8           STORE CHARACTER
        SBZ     18              RESET RBRL
        DEC     R3              DECREMENT COUNT
        JEQ     RCVEND          END IF COUNT = 0
        CB      *R2 + ,R4       COMPARE TO EOB CHARACTER, INCREMENT POINTER
        JNE     RCVLP           LOOP IF NOT COMPLETE
RCVEND  RT                      END OF SUBROUTINE
```

Register Loading After Initialization

The control, interval, and data rate registers may be reloaded after initialization. For example, it may be desirable to change the interval of the timer. Assume, for sample, that the interval is to be changed to 10.24 milliseconds. The instruction sequence is as follows:

```
        SBO     13              SET LOAD CONTROL FLAG
        LDCR    @INTVL2,8       LOAD REGISTER, RESET FLAG
          •
          •
          •
INTVL2  BYTE    10240/64
```

Caution should be exercised when transmitter interrupts are enabled to ensure that the transmitter interrupt does not occur while the load control flag is set. For example, if the transmitter interrupts between execution of the "SBO 13" and the next instruction, the transmit buffer is not enabled for loading when the transmitter interrupt service routine is entered because the LDIR flag is set. This situation may be avoided by the following sequence:

```
            BLWP    @INTVCHG        CALL SUBROUTINE
              •
              •
              •
ITV CPC     LI MI   0               MASK ALL INTERRUPTS
            MOV     @24(R13), RIZ   LOAD CRU BASE ADDRESS
            SB0     13              SET FLAG
            LDCR    @INTVL2,8       LOAD REGISTER AND RESET FLAG
            RTWP                    RESTORE MASK AND RETURN
              •
              •
              •
ITVCHG      DATA    ACCWP, ITVCPC
INTVL2      BYTE    10240/64
```

In this case all interrupts are masked, ensuring that all interrupts are disabled while the load control flag is set.

AMI

A Subsidiary of Gould Inc.

Future Products

Communication Products

S2579	BCD Input DTMF Generator
S2575	Pulse/DTMF Switchable Dialer With Three Number Repertory Memory
S2552	Telephone Hybrid Plus Pulse Dialer Single Chip Phone
S2553	Telephone Hybrid Plus DTMF Dialer Single Chip Phone
S2567	DTMF Generator With Microprocessor Bus Interface
S35213	Bell 212A Modem
S3559	Call Progress Monitor With DTMF and Pulse Dialer
S7720	Second Source For NEC7720 Digital Signal Processor
S28216	Echo Canceller Processor

Consumer Products

S3620	M/F LPC-10 Speech Synthesizer. Designed As Macro Cell To Allow For Easy Customization.

ROMs

680XX	High Speed Family of NMOS ROMs Including 32K, 64K Bi-Polar PROM Pin-Outs

Semi-Custom Products

	Two Micron Family of Gate Arrays and Standard Cells
	1.25 Micron Family of Gate Arrays and Standard Cells

Microprocessors/Microcomputers

S750X	CMOS 4-Bit Single Chip Microcomputers
S78XX	CMOS High-End 8-Bit Single Chip Microcomputers
S80	Operating System Processor Family

AMI®

A Subsidiary of Gould Inc.

Application Note Summary

Communications Products

S2559 DTMF Tone Generator

Describes design considerations, test methods, and results obtained using the S2559 Tone Generator family in DTMF pushbutton telephones. Interface with type 500 and 2500 networks are discussed. Use in ancillary equipment is also covered.

Using the S3525A/B

DTMF Bandsplit Filter

Consumer Products

MOS Music

MOS Music is a primer on the application of standard MOS/LSI circuits in creating electronic music. This note discusses the key elements of music production in an electronic organ.

S6800 Family

A Minimal S6802/S6846 Systems Design

Details how to make an S6802/S6846 version of the EVK in a minimal systems application.

S68045 Compared with Motorola MC 6845

Describes the fundamental differences between the two devices.

S9900 Family

S9900 Minimum System Design with the S9900 16-Bit Microprocessor

This design uses just the CPU, a 1K ROM, a 2K RAM, a clock and six smaller IC's.

S9900 Controlled Dot Matrix Printer

S9900 shows how to control a 7040 series dot matrix printer in a minimal systems application.

AMI®

A Subsidiary
of Gould Inc.

General Information

Guide to MOS Handling

At AMI we are continually searching for more effective methods of providing protection for MOS devices. Present configurations of protective devices are the result of years of research and review of field problems.

Although the oxide breakdown voltage may be far beyond the voltage levels encountered in normal operation, excessive voltages may cause permanent damage. Even though AMI has evolved the best designed protective device possible, we recognize that it is not 100% effective.

A large number of failed returns have been due to misapplication of biases. In particular, forward bias conditions cause excessive current through the protective devices, which in turn will vaporize metal lines to the inputs. **Careful inspection of the device data sheets and proper pin designation should help reduce this failure mode.**

Gate ruptures caused by static discharge also account for a large percentage of device failures in customers' manufacturing areas. **Precautions should be taken to minimize the possibility of static charges occurring during handling and assembly of MOS circuits.**

To assist our customers in reducing the hazards which may be detrimental to MOS circuits, the following guidelines for handling MOS are offered. **The precautions listed here are used at AMI.**

1. All benches used for assembly or test of MOS circuits are covered with conductive sheets. WARNING: Never expose an operator directly to a hard electrical ground. For safety reasons, the operator must have a resistance of at least 100K Ohms between himself and hard electrical ground.
2. All entrances to work areas have grounding plates on door and/or floor, which must be contacted by people entering the area.
3. Conductive straps are worn inside and outside of employees' shoes so that body charges are grounded when entering work area.
4. Anti-static neutralized smocks are worn to eliminate the possibility of static charges being generated by friction of normal wear. Two types are available; Dupont anti-static nylon and Dupont neutralized 65% polyester/35% cotton.
5. Cotton gloves are worn while handling parts. Nylon gloves and rubber finger cots are not allowed.
6. Humidity is controlled at a minimum of 35% to help reduce generation of static voltages.
7. All parts are transported in conductive trays. Use of plastic containers is forbidden. Axial leaded parts are stored in conductive foam, such as Velofoam#7611.
8. All equipment used in the assembly area must be thoroughly grounded. Attention should be given to equipment that may be inductively coupled and generate stray voltages. Soldering irons must have grounded tips. Grounding must also be provided for solder posts, reflow soldering equipment, etc.
9. During assembly of ICs to printed circuit boards, it is advisable to place a grounding clip across the fingers of the board to ground all leads and lines on the board.
10. Use of carpets should be discouraged in work areas, but in other areas may be treated with anti-static solution to reduce static generation.
11. MOS parts should be handled on conductive surfaces and the handler must touch the conductive surface **before** touching the parts.
12. In addition, no power should be applied to the socket or board while the MOS device is being inserted. This permits any static charge accumulated on the MOS device to be safely removed before power is applied.
13. MOS devices should not be handled by their leads unless absolutely necessary. If possible, MOS devices should be handled by their packages as opposed to their leads.
14. In general, materials prone to static charge accumulation should not come in contact with MOS devices.

These precautions should be observed even when an MOS device is suspected of being defective. The true cause of failure cannot be accurately determined if the device is damaged due to static charge build-up.

It should be remembered that even the most elaborate physical prevention techniques will not eliminate device failure if personnel are not fully trained in the proper handling of MOS.

This is a most important point and should not be overlooked.

More information can be obtained by contacting the Product Assurance Department.

American Microsystems, Inc.
3800 Homestead Road
Santa Clara, California 95051
Telephone (408) 246-0330
TWX 910-338-0024 or 910-338-0018

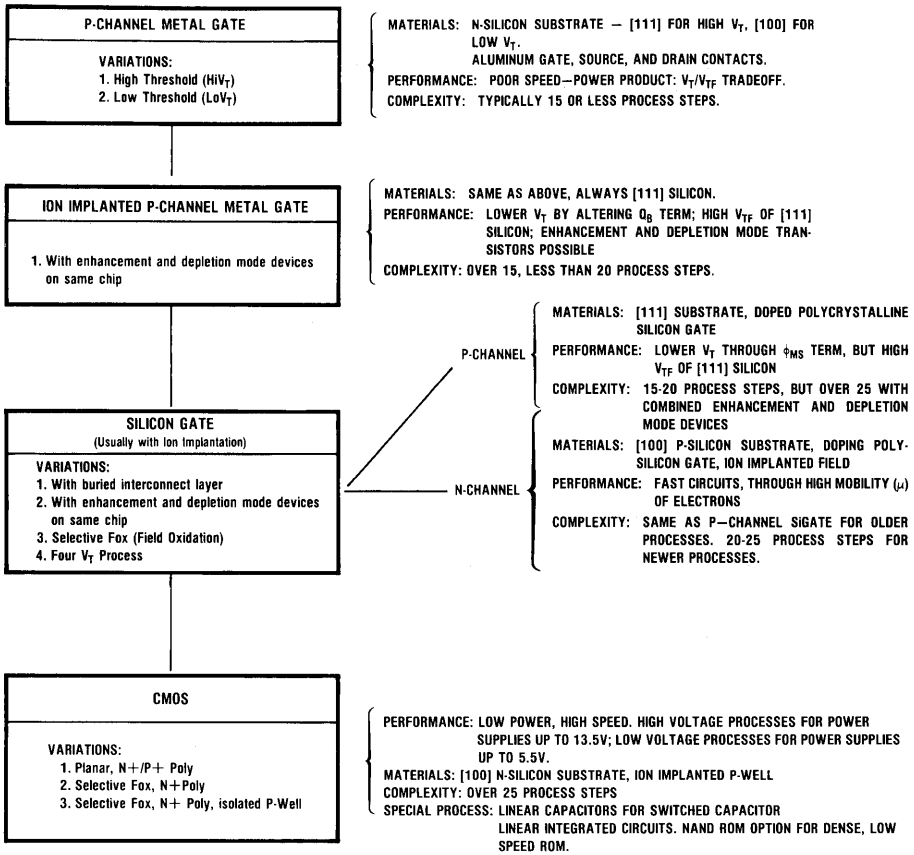
Process Descriptions

Each of the major MOS processes is described on the following pages. First, the established production proven processes are described, followed by those advanced processes, which are starting to go into volume production now. In each case, the basic processes is described first, followed by an explanation of its advantages, applications, etc.

P-Channel Metal Gate Process

Of all the basic MOS processes, P-Channel Metal Gate is the oldest and the most completely developed. It has served as the foundation for the MOS/LSI industry and still finds use today in some devices. Several versions of this process have evolved since its earliest days. A thin slice (8 to 10 mils) of lightly doped N-type silicon wafer serves as the substrate or body of the MOS transistor. Two closely spaced, heavily doped P-type regions, the source and drain, are formed within the substrate by selective diffusion of an impurity that provides holes as majority electrical carriers. A thin deposited layer of aluminum metal, the gate, covers the area between the source and drain regions, but is electrically insulated from the substrate by a thin layer (1000-15000A) of silicon dioxide. The P-Channel transistor is turned on by a negative gate voltage and conducts current between the source and the drain by means of holes as the majority carriers.

Figure B.1. Summary of MOS Process Characteristics



The basic P-Channel metal gate process can be subdivided into two general categories: **High-threshold and low-threshold.** Various manufacturers use different techniques (particularly so with the low threshold process) to achieve similar results, but the difference between them always rests in the threshold voltage V_T required to turn a transistor on. The high threshold V_T is typically -3 to -5 volts and the low threshold V_T is typically -1.5 to -2.5 volts.

The original technique used to achieve the difference in threshold voltages was by the use of substrates with different crystalline structures. The high V_T process used [111] silicon whereas, the low V_T process used [100] silicon. The difference in the silicon structure causes the surface charge between the substrate and the silicon dioxide to change in such a manner that it lowers the threshold voltages.

One of the main advantages of lowering V_T is the ability to interface the device with TTL circuitry. However, the use of [100] silicon carries with it a distinct disadvantage also. Just as the surface layer of the [100] silicon can be inverted by a lower V_T, so it also can be inverted at other random locations—through the thick oxide layers—by large voltages that may appear in the metal interconnections between circuit components. This is undesirable because it creates parasitic transistors, which interfere with circuit operation. The maximum voltage that can be carried in the interconnections is called the parasitic field oxide threshold voltage V_{TF}, and generally limits the overall voltage at which a circuit can operate. This, then, is the main factor that limits the use of the [100] low V_T process. A drop in V_{TF} between a high V_T and low V_T process may, for example, be from $-28V$ to $-17V$.

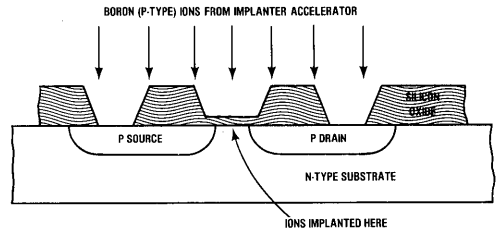
The low V_T process, because of its lower operating voltages, usually produces circuits with a lower operating speed than the high V_T process, but is easier to interface with other circuits, consumes less power, and therefore is more suitable for clocked circuits. Both P-Channel metal gate processes yield devices slower in speed than those made by other MOS processes, and have a relatively poor speed/power product. Both processes require two power supplies in most circuit designs, but the high V_T process, because it operates at a high threshold voltage, has excellent noise immunity.

Ion Implanted P-Channel Metal Gate Process

The P-Channel Ion Implanted process uses essentially the same geometrical structure and the same materials as the high V_T P-Channel process, but includes the ion implantation step. The purpose of ion implantation is to introduce P-type impurity ions into the substrate in the limited area under the gate electrode. By changing the characteristics of the substrate in the gate area, it is possible to lower the threshold voltage V_T of the transistor, without influencing any other of its properties.

Figure B.2. shows the ion implantation step in a diagrammatic manner. It is performed after the gate oxide is grown, but before the source, gate, and drain metallization deposition. The wafer is exposed to an ion beam which penetrates through the thin gate oxide layer and implants ions into the silicon substrate. Other areas of the substrate are protected both by the thicker oxide layer and sometimes also by other masking means. Ion implantation can be used with any process and, therefore could, except for the custom of the industry, be considered a special technique, rather than a process in itself.

Figure B.2. Diagram of Ion Implantation Step



The implantation of P-type ions into the substrate, in effect, reduces the effective concentration of N-type ions in the channel area and thus lowers the V_T required to turn the transistor on. At the same time, it does not alter the N-type ion concentration elsewhere in the substrate and therefore, does not reduce the parasitic field oxide threshold voltage V_{TF} (a problem with the low V_T P-Channel Metal Gate process, described above). The [111] silicon usually is used in ion-implanted transistors.

In fact, if the channel area is exposed to the ion beam long enough, the substrate in the area can be turned into P-type silicon (while the body of the substrate still remains N-type) and the transistor becomes a depletion mode device. In any circuit some transistors can be made enhancement type, while others are depletion type, and the combination is a very useful circuit design tool.

The Ion-implanted P-Channel Metal Gate process is very much in use today. Among all the processes, it represents a good optimization between cost and performance and thus is the logical choice for many common circuits, such as memory devices, data handling (communication) circuits, and others.

Because of its low V_T, it offers the designer a choice of using low power supply voltages to conserve power or increase supply voltages to get more driving power and thus increase speed. At low power levels it is more feasible to implement clock generating and gating circuits on the chip. In most circuit designs only a single power supply voltage is required.

N-Channel Process

Historically, N-Channel process and its advantages were known well at the time when the first P-Channel devices were successfully manufactured; however, it was much more difficult to produce N-Channel. One of the main reasons was that the polarity of intrinsic charges in the materials combined in such a way that a transistor was on at 0V and had a V_T of only a few tenths of a volt (**positive**). Thus, the transistor operated as a marginal depletion mode device without a well-defined **on/off** biasing range. Attempts to raise V_T by varying gate oxide thickness, increasing the substrate doping, and back biasing the substrate, created other objectionable results and it was not until research into materials, along with ion implantation, silicon gates, and other improvements came about that N-Channel became practical for high density circuits.

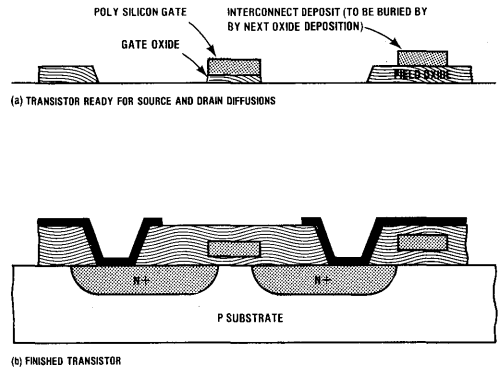
The N-Channel process gained its strength only after the P-Channel process, ion implantation, and silicon gate all were already well developed. N-Channel went into volume productions with advent of the 4K dynamic RAM and the microprocessor, both of which required speed and high density. Because P-Channel processes were nearing their limits in both of these respects, N-Channel became the logical answer.

The N-Channel process is structurally different from any of the processes described so far, in that the source, drain, and channel all are N-type silicon, whereas the body of the substrate is P-type. Conduction in the N-Channel is by means of electrons, rather than holes.

The main advantage of the N-Channel process is that the mobility of electrons is about three times greater than that of holes and, therefore, N-Channel transistors are faster than P-Channel. In addition, the increased mobility allows more current flow in a channel of any given size, and therefore N-Channel transistors can be made smaller. The positive gate voltage allows an N-Channel transistor to be completely compatible with TTL.

Although metal gate N-Channel processes have been used, the predominant N-Channel process is a silicon gate process. Among the advantages of silicon gate is the possibility of a buried layer of interconnect lines, in addition to the normal aluminum interconnnections deposited on the surface of the chip. This gives the circuit designer more latitude in layout and often allows the reduction of the total chip size. Because the polysilicon gate electrode is deposited in a separate step, after the thick oxide layer is in place, the simultaneous deposition of additional polysilicon interconnect lines is only a matter of masking. These interconnect lines are buried by later steps, as shown in Figure B.3.

Figure B.3. Crossection of an N-Channel Silicon Gate MOS Transistor



One minor limitation associated with the buried interconnect lines is their location. Because the source and drain diffusions are done after the polysilicon is deposited [see (a) of Figure B.3] the interconnect lines cannot be located over these diffusion regions.

A second advantage of a silicon gate is associated with the reduction of overlap between the gate and both the source and drain. This reduces the parasitic capacitance at each location and improves speed, as well as power consumption characteristics. Whereas in the metal gate process, the P region source and drain diffusion must be done prior to deposition of the gate electrode, in silicon gate process, the electrode is in place during diffusion, see (a) of Figure B.3. Therefore, no planned overlap for manufacturing tolerance purposes need exist and the gate is said to be **self-aligned.** The only overlap that occurs is due to the normal lateral extension of the source and drain regions during the diffusion process.

The silicon-gate process produces devices that are more compact than metal gate, and are slightly faster because of the reduced gate overlap capacitance. Because the basic silicon gate process is relatively simple, it is also economical. It is a versatile process that is used in memory devices and most any other circuit.

In addition to its use in large memory chips and microprocessors, N-Channel has become a good general purpose process for circuits in which compactness and high speed are important.

CMOS

The basic CMOS circuit is an inverter, which consists of two adjacent transistors—one an N-Channel, the other a P-Channel, as shown in Figure B.4. The two are fabricated on the same substrate, which can be either N or P type.

The CMOS inverter in Figure B.4 is fabricated on an N-type silicon substrate in which a P "tub" is diffused to form the body for the N-Channel transistor. All other steps, including the use of silicon gates and ion implantation, are much the same as for other processes.

The main advantage of CMOS is extremely low power consumption. When the common input to both gate electrodes is at a logic 1 (a positive voltage) the N-Channel transistor is biased on, the P-Channel is off, and the output is near ground potential. Conversely, when the input is at a logic 0 level, its negative voltage biases only the P-Channel transistor on and the output is near the drain voltage $+ V_{DD}$. In either case, only one of the two transistors is on at a time and thus, there is virtually no current flow and no power consumption. Only during the transition from one logic level to the other are both transistors on and current flow increases momentarily.

Silicon Gate CMOS is also fast approaching speeds of bipolar TTL circuits. On the other hand, the use of two transistors in every gate makes CMOS slightly more complex and costly, and requires more chip size. For these reasons, the original popularity of CMOS was in SSI logic elements and MSI circuits—logic gates, inverters, small shift registers, counters, etc. These CMOS devices constitute a logic family in the same way as TTL, ECL, and other bipolar circuits do; and in the areas of very low power consumption, high noise immunity, and simplicity of operation, are still widely accepted by discrete logic circuit designers.

Low power CMOS circuits made the watch circuit possible and also have been used in space exploration, battery operated consumer products, and automotive control devices. As experience was gained with CMOS, tighter design rules and reduced device sizes have been implemented and now VLSI circuits, such as 16K RAM memories and microprocessors, are being manufactured in volume.

CMOS circuits can be operated on a single power supply voltage, which can be varied from + 2.5 to about + 13.5 volts with the high voltage processes, with a higher voltage giving more speed and higher noise immunity. Low voltage processes allow single power supply voltages from + 1.5 to + 5.5 volts.

The first implementation of an inverting gate is a process that uses both n+ to p+ polysilicon. The basic structure is a first-generation approach to which a selective field-oxidation process has been added.

Figure B.5 shows the plan and section views of the three-device gate portion. Because the P-Well in the top view spans both N-Channel devices, it is referred to as ubiquitous, and the process is called Ubiquitous P-Well.

In this planar process, p+ guard rings are used to reduce surface leakage. Polysilicon cannot cross the rings, however, so that bridges must be built. Note the use of p+ polysilicon in the P-Channel areas. The plan view shows the construction of the bridges linking p+ to metal to n+. (Were the process to be used for a low-voltage, first-generation application like a watch circuit, the guard rings would not be necessary and polysilicon could directly connect N-Channel and P-Channel devices; however, to ensure good ohmic contact from one type of polysilicon to another, polysilicon-diode contacts must be capped with metal.)

This process provides a buried contact (n+ polysilicon to n+ diffusion) that can yield a circuit-density advantage. However, neither of the other two second-generation approaches provides buried contacts. Therefore, if a layout in this process is to be compatible with the others, the buried contact must be eliminated. Though there will be a penalty in real estate, the gain for custom applications is a great increase in the number of available CMOS vendors.

The n+-Only Polysilicon Approach

Both of the second-generation CMOS processes that follow are variants of the n+-only, selective-field-oxide approach. One closely resembles the p+ n+ Ubiquitous-P-Well process, since it, too, has a Ubiquitous P-Well that is implanted before the field oxidation and thus runs under the field oxide. The other, called isolated P-Well, has separate wells for each N-Channel device that are implanted after field oxidation.

Figure B.6 shows the section and plan views of the n+-only Ubiquitous-P-Well approach used to build the gate of Figure B.4. This is the 5μm process recommended by AMI and others for new, high-performance CMOS designs. The layout is simpler than with the n+/p+ polysilicon Ubiquitous-Well approach (there are no buried contacts and no polysilicon-diode contacts), and it occupies less area for the same line widths. Also, since the process permits implanting in the field region, no guard rings are required.

Polysilicon can thus cross directly from P- to N-Channel device areas without the need for bridges or polysilicon-dioxide contacts.

A variant of the all n+ (See Figure B.7) polysilicon process just discussed uses basically the selective field-oxide approach except that the P-Wells are not continuous under the field-oxide areas; they are instead bounded by field-oxide edges. Since the P-Wells are naturally isolated from one another, the process is called n+ poly-isolated P-Well. The isolated wells must all be connected to ground; if they are left floating, circuit malfunctions are bound to occur. The grounding is done either with p+ diffusions or with top-side metalization that covers a p+-to-P-Well contact diffusion.

Figure B.4. Crossection and Schematic Diagram of a CMOS Inverter

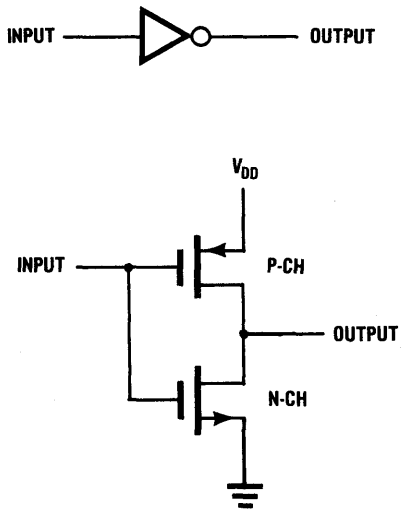
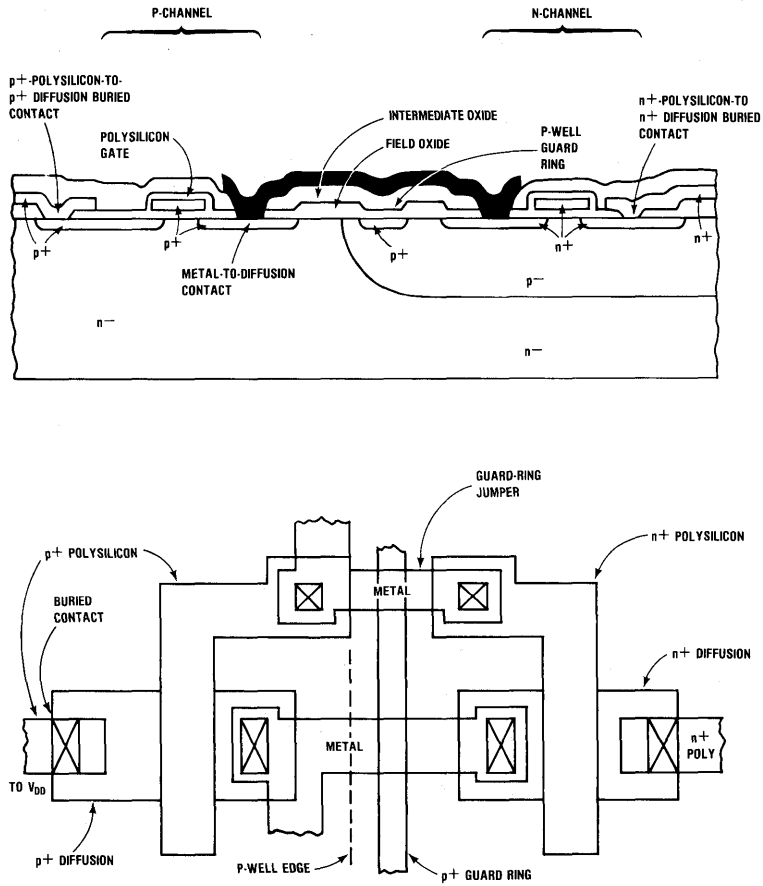
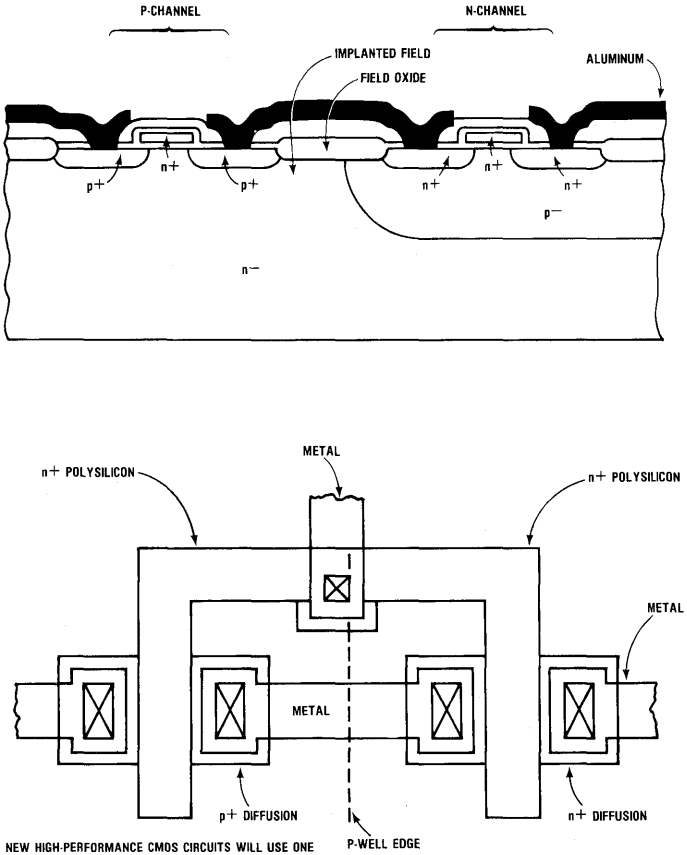


Figure B.5. n + /p + Polysilicon Approach



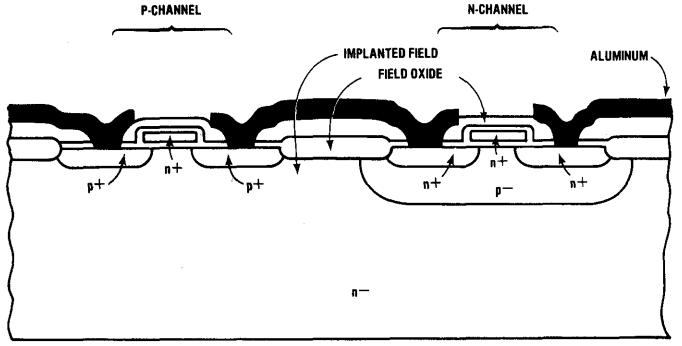
THE FIRST HIGH-PERFORMANCE COMPLEMENTARY-MOS PLANAR PROCESS. ITS DRAWBACKS: TWO TYPES OF POLYSILICON ARE USED, AND THE UNAVAILABILITY OF FIELD IMPLANT DOPING TIES FIELD THRESHOLD TO DEVICE THRESHOLDS.

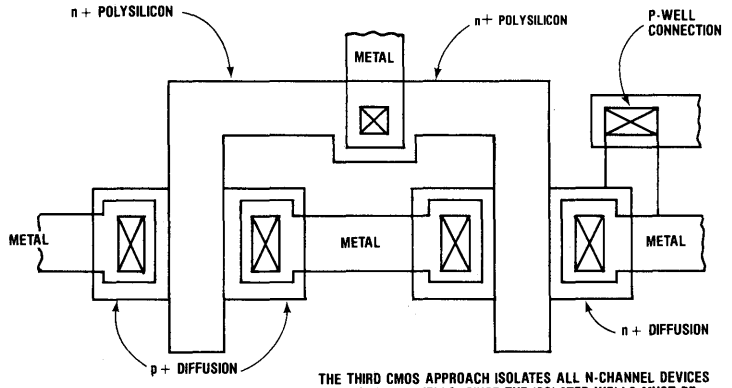
Figure B.6. n + – Only Polysilicon Approach



ALL NEW HIGH-PERFORMANCE CMOS CIRCUITS WILL USE ONE TYPE OF POLYSILICON. THIS VERSION HAS A UBIQUITOUS P-WELL: THAT IS, SERIES N-CHANNEL DEVICES SIT IN A COMMON P-WELL, WHICH, IMPLANTED BEFORE FIELD OXIDATION, RUNS UNDER THE FIELD OXIDE. THIS IS AMI'S PREFERRED CMOS PROCESS FORMAT FOR ALL NEW DESIGNS.

Figure B.7. Isolated Wells





THE THIRD CMOS APPROACH ISOLATES ALL N-CHANNEL DEVICES IN SEPARATE P-WELLS, SINCE THE ISOLATED WELLS MUST BE DOPED MUCH MORE HEAVILY THAN THOSE OF THE UBIQUITOUS-WELL APPROACH, n + -TO P-WELL CAPACITANCE IS GREATER AND SWITCHING SPEEDS LOWER. THIS IS AN n + -ONLY POLYSILICON PROCESS.

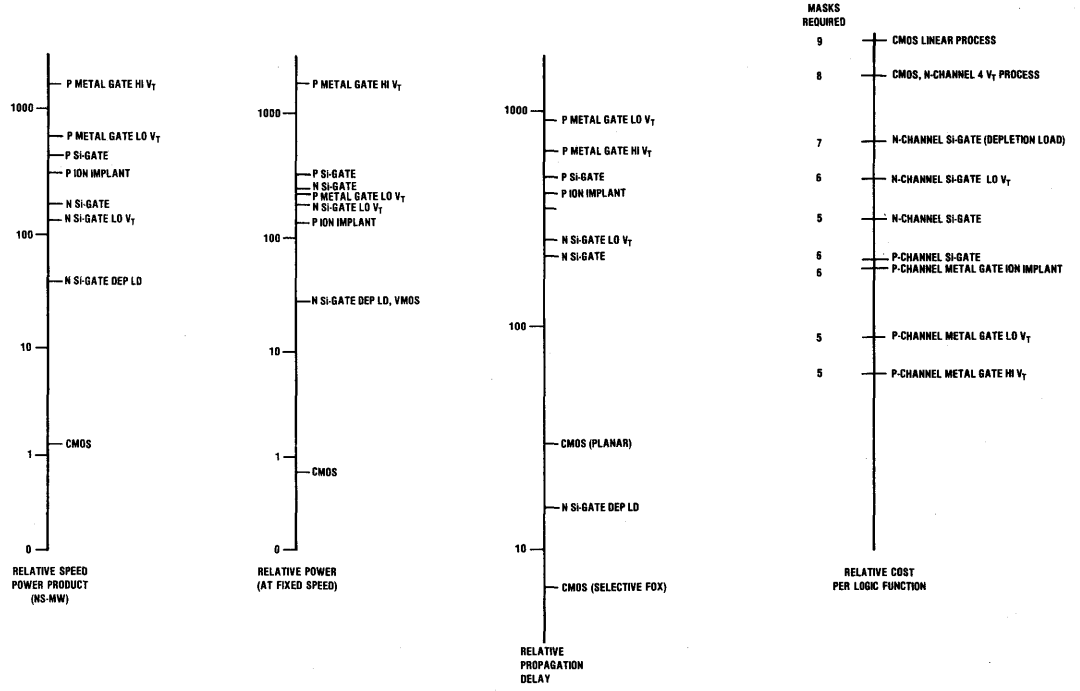
In the Isolated-Well process, the P-Wells must be doped much more heavily than in the Ubiquitous-Well process. One result is a higher junction capacitance between the n+ areas and the wells that both slows switching speeds and raises the power dissipation of a device. Even though the speed loss could be compensated for by slightly shorter channel lengths, the operating power still remains high.

Although currently available from AMI and other manufacturers, the Isolated-Well process is in fact not recommended for new designs by AMI. Its layout takes up more area than does one using the Ubiquitous-Well approach, even though its P-Well to p+-area spacing is slightly less.

Table 1. Layout Compatibility Concerns for CMOS Processes

Layout Feature	n+/p+ Polysilicon Ubiquitous P-Well	n+ – Only Polysilicon Ubiquitous P-Well	n+ – Only Polysilicon Isolated P-Well
Buried Contact	X	No	No
Polysilicon Diode Contact	Yes	X	X
P-Well Isolation With Diffusion Mask	No	No	Yes
Tight P-Well-To-p+ Spacing	No	No	Yes
Layout Care Required For P-Well Electrical Contacts	No	No	Yes

Figure B.8. Comparative Data on Major MOS Processes



7.5 Micron CMOS Process Parameters

	Low V_T		High V_T		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	.55	.85	1.0	1.5	N-Channel Threshold at 1μA 50 x 7.5μ Device (Volts)
V_{TP}	−.4	−.95	−.8	−1.4	P-Channel Threshold at 1μA 50 x 7.5μ Device (Volts)
V_{TF}	8		15		Poly Field Threshold at 1μA 50 x 10μ Device (Volts)
B_{VDSS}	24	—	28	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	30	39	28	33	Diffusion Resistivity Ω/□
N+	9	15	9.1	12.6	Diffusion Resistivity Ω/□
R_{POLY} P+	118	172	80	140	Poly Resistivity Ω/□
N+	30	60	29	39	Poly Resistivity Ω/□
T_{OX}	1300		1200		Gate Oxide Thickness, In Angstroms
X_j P+	1.8*		1.8*		Junction Depth, In μ
N+	2.0*		2.0*		Junction Depth, In μ
Operating Voltage	—	5	5	12	In Volts
Max Rating	—	5.5	—	13.2	In Volts
Process Designator	CTA	CTA	CTE	CTE	

(*Typical)

CMOS I Process Parameters

	General Purpose				Double Poly				NAND ROM				
	High V		Low V		High V		Low V		High V		Low V		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	0.7	1.3	0.5	1.1	0.7	1.3	0.5	1.1	0.7	1.3	0.5	1.1	N-Channel Threshold 50 x 5μ Device (Volts)
V_{TP}	−0.7	−1.3	−0.5	−1.1	−0.7	−1.3	−0.5	−1.1	−0.7	−1.3	−0.5	−1.1	P-Channel Threshold 50 x 5μ Device (Volts)
V_{TF}	17	—	7	—	17	—	7	—	17	—	7	—	Poly Field Threshold (Volts)
B_{VDSS}	17	—	7	—	17	—	7	—	17	—	7	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	15	35	15	35	15	35	15	35	15	35	15	35	Diffusion Resistivity Ω/□
N+	35	80	35	80	35	80	35	80	35	80	35	80	Diffusion Resistivity Ω/□
R_{POLY}	15	45	15	45	15	45	15	45	15	45	15	45	Poly Resistivity Ω/□ (All poly is N+)
T_{OX}	750	850	750	850	750	850	750	850	750	850	750	850	Gate Oxide Thickness, In Angstroms
X_j P+	1.2*		1.2*		1.2*		1.2*		1.2*		1.2*		Junction Depth, In μ
N+	1.5*		1.5*		1.5*		1.5*		1.5*		1.5*		Junction Depth, In μ
Operating Voltage	2.2	13.2	1.5	5.5	2.2	13.2	1.5	5.5	2.2	13.2	1.5	5.5	In Volts
Max Rating	—	13.2	—	5.5	—	13.2	—	5.5	—	13.2	—	5.5	In Volts
Process Designator	CVA	CVA	CVH	CVH	CVB	CVB	CVE	CVE	CVD	CVD	CVC	CVC	

(*Typical)

CMOS II Process Parameters (P-Well)

	Single Metal		Double Metal		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	0.6	1.0	0.6	1.0	N-Channel Threshold (Volts)
V_{TP}	−0.6	−1.0	−0.6	−1.0	P-Channel Threshold (Volts)
V_{TF}	14.0	—	14.0	—	Poly Field Threshold (Volts)
B_{VDSS}	14.0	—	14.0	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	35	80	35	80	Diffusion Resistivity Ω/□
N+	15	40	15	40	Diffusion Resistivity Ω/□
R_{POLY}	15	30	15	30	Poly Resistivity, Ω/□ (All Poly is N+)
T_{OX}	450	550	450	550	Gate Oxide Thickness, In Angstroms
X_j P+	0.3	0.5	0.3	0.5	Junction Depth, In μ
N+	0.3	0.5	0.3	0.5	Junction Depth, In μ
Operating Voltage	5.0	10.0	5.0	10.0	In Volts
Max Rating	—	10.0	—	10.0	In Volts
Process Designator	CCB	CCB	CCD	CCD	

MOS Processes

6 & 5 Micron SIGate NMOS Process Parameters

			6 Micron				5 Micron		
	Low V_T		High V_T		1.67/ Process Shrink				
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TE}	0.6	1.0	0.8	1.2	.75	1.25	0.6	1.0	Extrapolated Enhancement Threshold on a 50 x 6μ Transistor (Volts)
V_{TD}	−3.0	−4.0	−2.5	−3.5	−2.5	−3.5	−2.5	−3.5	Extrapolated Depletion Threshold on a 50 x 50μ Transistor (Volts)
V_{TN}	—	—	—	—	—	—	−.2	−.2	Intrinsic Device Threshold 50 x 6μ Transistor (Volts)
V_{TDD}	—	—	—	—	—	—	−4.35	−3.65	Deep Depletion Threshold (Volts)
V_{TF}	13	40	13	40	12	30	10	—	Poly Field Threshold (Volts)
B_{VDSS}	14	—	14	—	12	—	10	—	Drain-Source Breakdown on 50 x 50μ Transistor
R_{DIFF}	8	14	8	14	8	14	8	25	N+ Region Resistivity Ω/□
R_{POLY}	20	40	20	40	20	40	20	40	N+ Doped Poly Resistivity Ω/□
T_{OX}	1000	1150	1000	1150	750	850	750	850	Gate Oxide Thickness, In Angstroms
X_j	1.2	1.6	1.2	1.6	0.8	1.2	0.8	1.2	Junction Depth, In μ
Operating Voltage	5	12	5	12	5	12	5	12	In Volts
Max Rating		13.2		13.2		13.2		13.2	In Volts
Process Designator	NVC	NVC	NVD	NVD	NVS	NVS	NEA/NEC		

NMOS I & NMOS II Process Parameters

	NMOS I				NMOS II				
	$4V_T$		Std.		$4V_T$		Std.		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TE}	0.6	1.0	0.6	1.0	0.6	1.0	0.6	1.0	Extrapolated Enhancement Threshold Voltage on a 50 x 4μ Transistor (4μ Processes) or 50 x 3μ Transistor (3μ Processes) (Volts)
V_{TD}	−3.5	−2.5	−3.5	−2.5	−3.5	−2.5	−3.5	−2.5	Extrapolated Threshold 50 x 50μ Device (Volts)
V_{TN}	−0.15	+0.15	N/A	N/A	−0.15	+0.15	N/A	N/A	Extrapolated Threshold 50 x 6μ Device (Volts)
V_{TDD}	−4.35	−3.65	N/A	N/A	−4.85	−4.15	N/A	N/A	Extrapolated Threshold 50 x 50μ Device (Volts)
V_{TF}	7.5	—	7.5	—	7.5	—	7.5	—	Poly Field Threshold (Volts)
B_{VDSS}	7.5	—	7.5	—	7.5	—	7.5	—	Punch Through Voltage 50 x 4μ Device (4μ Processes) or 50 x 3μ Device (3μ Processes) (Volts)
R_{DIFF}	15	30	15	30	15	30	15	30	Diffusion Resistivity Ω/□
R_{POLY}	20	50	20	50	20	40	20	40	Poly Resistivity Ω/□
T_{OX}	650	750	650	750	450	550	450	550	Gate Oxide Thickness, In Angstroms
X_j	0.3	0.5	0.3	0.5	0.3	0.5	0.3	0.5	N+ Junction Depth, In μ
Operating Voltage	—	5/12	—	5/12	—	5	—	5	In Volts
Max Rating	—	5.5/13.2	—	5.5/13.2	—	5.5	—	5.5	In Volts
Process Designator	NDD	NDD	NDE	NDE	NCC	NCC	NCA	NCA	

7.5 Micron Metal Gate PMOS Process Parameters

			0 Implant				1 Implant		2 Implant		
	High V_T		Med V_T		Low V_T						
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TE}	−3.25	−4.95	−2.8	−4.2	−1.8	−2.5	−1.0	−1.8	−1.2	−2.0	I_{DS} = 1μA
V_{TD}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	4.0	5.0	Depletion Measurement on a 50μ Transistor (Volts)
V_{TF}	30	—	25	—	17	—	25	—	25	—	Field Threshold (Volts)
B_{VDSS}	30	—	30	—	30	—	22	—	22	—	Drain-Source Breakdown (Volts)
R_{DIFF}	30	60	30	60	30	60	30	60	30	60	Sheet Resistivity Ω/□
I_{DS}/mA	1.25	2.55	0.8	2.2	0.8	2.0	2.8	4.0	2	4	Drain-Source Current (mA)
B_{VOXG}	120	—	80	—	100	—	90	—	90	—	Gate Oxide Breakdown (Volts)
X_jJ	1.7	1.9	1.7	1.9	1.7	1.9	1.7	1.9	1.7	1.9	Junction Depth, In μ
Process Designator	PMC	PMC	PMT	PMT	PMD	PMD	PNR	PNR	POG	POG	

CMOS II Process Parameters (N-Well)

	Single Metal		Double Metal		
Parameter	**Min.**	**Max.**	**Min.**	**Max.**	**Comments**
V_{TN}	0.6	1.0	0.6	1.0	N-Channel Threshold Voltage (Volts)
V_{TP}	−0.6	−1.0	−0.6	−1.0	P-Channel Threshold Voltage (Volts)
V_{TF}	15	—	+15	—	Poly Field Threshold (Volts)
B_{VDSS}	15	—	+15	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	50	100	50	100	Diffusion Resistivity Ω/□
N+	15	40	15	40	Diffusion Resistivity Ω/□
T_{OX}	390	460	390	460	Gate Oxide Thickness, In Angstroms
X_j P+	0.3	0.5	0.3	0.5	Junction Depth, In μ
N+	0.3	0.5	0.3	0.5	Junction Depth, In μ
Operating Voltage	9	10		10	In Volts
Max Rating		11		11	In Volts
Process Designator	CCN/CCO		CCP		In Volts

AMI®

A Subsidiary of Gould Inc.

Product Assurance Program

Introduction

Quality is one of the most used, least understood, and variously defined assets of the semiconductor industry. At AMI we have always known just how important effective quality assurance, quality control, and reliability monitoring are in the ability to deliver a repeatably reliable product. Particularly, through the manufacture of custom MOS/LSI, experience has proved that one of the most important tasks of quality assurance is the effective control and monitoring of manufacturing processes. Such control and monitoring has a twofold purpose: to assure a consistently good product, and to assure that the product can be manufactured at a later date with the same degree of reliability.

To effectively achieve these objectives, AMI has developed a Product Assurance Program consisting of three major functions:

- Quality Control
- Quality Assurance
- Reliability

Each function has a different area of concern, but all share the responsibility for a reliable product.

The AMI Product Assurance Program

The program is based on MIL-STD-883, MIL-M-38510, and MIL-Q-9858A methods. Under this program, AMI manufactures highest quality MOS devices for all segments of the commercial and industrial market and, under special adaptations of the basic program, also manufactures high reliability devices to full military specifications for specific customers.

The three aspects of the AMI Product Assurance Program—Quality Control, Quality Assurance, and Reliability—have been developed as a result of many years of experience in MOS device design and manufacture.

Quality Control establishes that every method meets or fails to meet, processing or production standards—**QC checks methods.**

Quality Assurance establishes that every method meets, or fails to meet, product parameters—**QA checks results.**

Reliability establishes that QA and QC are effective—**Reliability checks device performance.**

One indication that the AMI Product Assurance Program has been effective is that NASA has endorsed AMI products for flight quality hardware since 1967. The Lunar Landers and Mars Landers all have incorporated AMI circuits, and AMI circuits have also been utilized in the Viking and Vinson programs, as well as many other military airborne and reconnaissance hardware programs.

Quality Control

The Quality Control function in AMI's Product Assurance Program involves constant monitoring of all aspects of materials and production, starting with the raw materials purchased, through all processing steps, to device shipment. There are three major areas of Quality Control:

- Incoming Materials Control
- Microlithography Control
- Process/Assembly Control

Incoming Materials Control

All purchased materials, including raw silicon, are checked carefully to various test and sampling plans. The purpose of incoming materials inspection is to ensure that all items required for the production of AMI MOS circuits meet such standards as are required for the production of high quality, high reliability devices.

Incoming inspection is performed to specifications agreed to by suppliers of all materials. The Quality Control group continuously analyzes supplier performance, performs comparative analysis of different suppliers, and qualifies the suppliers.

Tests are performed on all direct material, including packages, wire, lids, eutectics, and lead frames. These tests are performed using a basic sampling plan in accordance with MIL-S-19500, generally to a Lot Tolerance Percent Defective (LTPD) level of 10%. The AQL must be below 1% overall.

Two incoming material inspection sequences illustrate the thoroughness of AMI Quality Control:

- Purchased packages are first inspected visually. Then, dimensional inspections are performed, followed by a full functional inspection, which subjects the packages to an entire production run simulation. Finally, a full electrical evaluation is made, including checks of the insulation, resistance, and lead-to-lead isolation. A package lot which passes these tests to an acceptable LTPD level is accepted.
- Raw silicon must also pass visual and dimensional checks. In addition, a preferential etch quality inspection is performed. For this inspection, the underlayers of bulk silicon are examined for potential anomalies such as dislocation, slippage or etch pits. Resistivity of the silicon is also tested.

Microlithography Control

Microlithography involves the processes which result in finished working plates, used for the fabrication of wafers. These processes are pattern or artwork generation, photoreduction, and the actual printing of the working plates.

Pattern generation now is the most common practice at AMI. The circuit layout is digitized and stored on a tape, which then is read into an automated pattern generator which prints a highly accurate 10x reticle directly.

In cases where the more traditional method of artwork generation is used whether Rubylith, Gerber Plots, AMI generated or customer generated—the artwork is thoroughly inspected. It is checked for level-to-level registration and dimensional tolerances. Also, a close visual inspection of the workmanship is made. AMI artwork is usually produced at 200x magnification and must con-

form to stringent design rules, which have been developed over a period of years as part of the process control requirements.

Acceptable artwork is photographically reduced to a 20x magnification, and then further to a 10x magnification. The resulting 10x reticles are then used for producing 1x masters. The masters undergo severe registration comparisons to a registration master and all dimensions are checked to insure that reductions have been precise. During this step, image and geometry are scrutinized for missing or faded portions and other possible photographic omissions.

For a typical N-Channel silicon gate device, master sets are checked at all six geometry levels in various combinations against each other and against a proven master set. Allowable deviations within the die are limited to 0.5 micron, deviations within a plate are limited to 1 micron, and all plate deviations are considered cumulatively.

Upon successful completion of a device master set, it is released to manufacturing where the 1x plates are printed. A sample inspection is performed by manufacturing on each 30-plate lot and the entire lot is returned to Quality Control for final acceptance. Quality Control performs audits on each manufacturing inspector daily, by sample inspection techniques.

The plates can be rejected first by manufacturing when the 30-plate lots are inspected, or by Quality Control when the lots are submitted for final acceptance. If either group rejects the plates, they are rescreened and then undergo the same inspection sequence. In the rescreening process, the plates undergo registration checks; visual checks for pin holes, protrusions, and faded or missing images, as well as all critical dimension checks.

Process Control

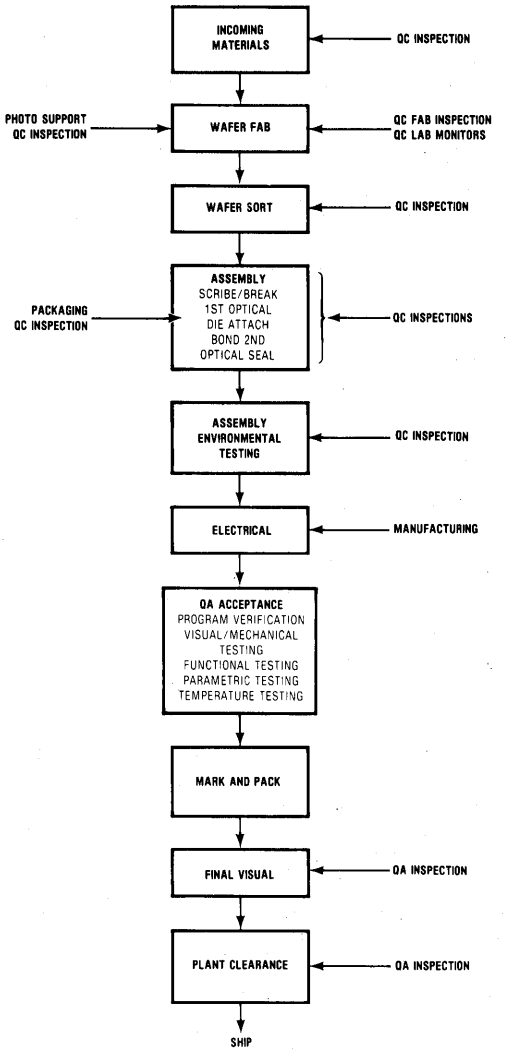
Once device production has started in manufacturing, AMI Quality Control becomes involved in one of the most important aspects of the Product Assurance Program—the analysis and monitoring of virtually all production processes, equipment, and devices.

Process controls are performed in the fabrication area, by the Quality Control Fabrication Group, to assure adherence to specifications. This involves checks on operators, equipment and environment. Operators are tested for familiarity with equipment and adherence to procedure. Equipment is closely checked both through calibration and maintenance audits. Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possibility of contamination or adverse effects due to temperature or humidity excesses.

Experience has proven that such close control of the operators, equipment, and environment is highly effective towards improved quality and increased yields.

In addition to the specification adherence activities of the

Figure 1. Flowchart of Product Assurance Program Implementation



Product Assurance Program

QC Fabrication Group, A QC Laboratory performs constant process monitoring of virtually every step of all processes. Specimens are taken from all production steps and critically evaluated. Sampling frequency varies, depending on the process, but generally, oxidation, diffusion, masking and evaporization are the most closely monitored steps.

Results are supplied both to manufacturing and engineering. When evidence of a problem occurs, QC provides recommendations for corrections and follows up the corrective action taken.

Optical Inspections are performed at several steps; quality control limits are based on a 10% LTPD. The chart in Figure 1 shows process steps and process control points.

Quality Assurance

The Quality Assurance function in the Product Assurance Program involves checking the ability of manufactured parts to meet specifications. In addition, the QA group also is responsible for calibration of all equipment, and for the maintenance of AMI internal product specifications, to assure that they are always in conformance with customer specifications or other AMI specifications.

After devices undergo 100% testing in manufacturing, they are sent to Quality Assurance for acceptance. Lots are defined, and using the product specifications, sample sizes are determined, along with the types of tests to be performed and the test equipment to be used. Lots must pass QA testing to a 0.04% AQL.

Three types of tests are performed on the samples: visual/mechanical, parametric, and functional. All tests are performed both at room temperature and at elevated temperature. In addition, a number of other special temperature tests may be performed if required by the specification.

To perform the tests, QA uses AMI PAFT test systems, ROM test systems, Macrodata testers, Fairchild **Sentry**, LTX **Sentinel**, **XINCOM** systems, Teradyne test systems, and various bench test units. In special instances a part may also be tested in a real life environment in the equipment which is to finally utilize it.

If a lot is rejected during QA testing, it is returned to the production source for an electrical rescreening. It is then returned to QA for acceptance but is identified as a resubmitted lot. If it fails again, corrective action in engineering is initiated. As evidence of the problem is detected, the parts may also be traced all the way back to the wafer run to analyze the cause.

When a lot is acceptable, it is sent to packaging and then to finished goods. When parts leave finished goods, they are again checked by the QA group to a 10% LTPD with visual/mechanical tests. Also, all supporting documentation for the parts is verified, including QA acceptance, special customer specifications, certificates of compliance, etc. Only after this last check are devices considered ready for plant clearance.

If there are customer returns, they are first sample tested by QA to determine the cause of the return. (Many times an invalid customer test will incorrectly cause returns.) Selected return samples are sent to Reliability for failure analysis.

Reliability

The Reliability function in the Product Assurance Program involves process qualification, device qualification, package qualification, reliability program qualification and failure analysis. To perform these functions AMI Reliability group is organized into two major areas:

- Reliability Laboratory
- Failure Analysis

Reliability Laboratory

AMI Reliability Laboratory is responsible for the following functions.

- New Process Qualification
- Process Change Qualification
- Process Monitoring
- New Device Qualification
- Device Change Qualification
- New Package Qualification
- Device Monitoring
- Package Change Qualification
- Package Monitoring
- High Reliability Programs

There are various closely interrelated and interactive phases involved in the development of a new process, device, package or reliability program. A process change may affect device performance, a device change may affect process repeatability, and a package change may affect both device performance and process repeatability. To be effective, the Reliability Laboratory must monitor and analyze all aspects of new or changed processes, devices, and packages. It must be determined what the final effect is on product reliability, and then evaluate the merits of the innovation or change.

Process Qualification

For example, AMI Research and Development group recommends a new process or process alteration when it feels that the change can result in product improvement. The Reliability Laboratory then performs appropriate environmental and electrical evaluations of a new process. Typically, a special test vehicle, or "rel chip", generated by R&D during process development, is used to qualify the recommended new process or process change.

The rel chip is composed of circuit elements similar to those that may be required under worst-case circuit design conditions. The rel chip elements are standard for any given process, and thus allow precise comparisons between diffusion runs. The following is an example of what is included on a typical rel chip:

- A discrete inverter and an MOS capacitor

- A large P-N junction covered by an MOS capacitor.
- A large P-N junction area (identical to the junction area above, but without the MOS capacitor)
- A large area MOS capacitor over substrate
- Several long contact strings with different contact geometries
- Several long conductor geometries, which cross a series of eight deeply etched areas

Each circuit element of a rel chip allows a specific test to be performed. As an example, the discrete inverter and MOS load device accommodate power life tests. As a consequence, any type of parameter drift can be observed. The MOS capacitor, covering the large P-N junction, can serve to indicate the presence of contamination in the oxide, under the oxide, or in the bulk silicon. If unusual drift is evidenced, the location of contamination can be determined through analysis of the additional MOS capacitor and the large P-N junction area. The metal conductor interconnecting contacts is useful for life testing under relatively high current conditions. It facilitates the detection of metal separation when moisture or other contaminants are present.

The conductors crossing deeply etched areas allow the checking of process control. Rather than depending upon optical inspection of metal quality, burned out areas caused by high currents are readily identified and provide a quantitative measure of metal quality.

If the Reliability Laboratory determines that a recommended new process or process change is viable for manufacturing purposes, further analysis is necessary to determine that production devices can be manufactured in high volume, in a repeatable and reliable manner.

Process Monitoring

In addition to process qualification, the Reliability group also conducts ongoing process monitoring programs. Once every 90 days each major production process is evaluated using rel chips as test vehicles. The resulting test data is analyzed for parameter limits and process stability. In this manner AMI can help assure repeatability and high product quality.

Package Qualifications

New packages are also qualified before they are adopted. To analyze packages, a qualification matrix is designed, according to which the new package and an established package (used for control) are tested concurrently. The test matrix consists of a full spectrum of electrical and environmental stress tests, in accordance with MIL-STD-883.

Failure Analysis

Another important function of the Reliability group is failure analysis. Scanning electron microscopes, high power optical microscopes, diagnostic probe stations, and other equipment is used in failure analysis of devices submitted from various sources. It is the function of the Reliability group to determine the cause of failure and recommend corrective action.

The Reliability group provides a failure analysis service for the previously mentioned in-house programs and for the evaluation of customer returns. All AMI customers are provided a failure analysis service for any part that fails within one year from date of purchase and the results of the analysis are returned in the form of a written report.

Summary

The Product Assurance Program at AMI is oriented towards process control and monitoring, and the evaluation of devices. The Program consists of three major functions: Quality Control, Quality Assurance, and Reliability. Constant monitoring of all phases of production, with information feedback at all levels, allows fast and efficient detection of problems, evaluation and analysis, correction, and verification of the correction. The overall result is a line of products which are highly repeatable and reliable, with a very low reject level.

Packaging

Introduction

Plastic Packages

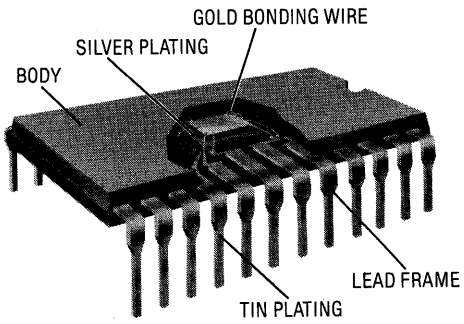
AMI is excelling in the use of transfer molding of plastic packages. All of our plastic packages are produced by mounting the die on a lead frame, gold wire bonding, transfer molding and tin plating the external leads. Many of the packages utilize a copper leadframe which combines low cost with high heat dissipation characteristics. We are proud of our plastic packaging capabilities.

Plastic Package

The AMI plastic dual-in-line package is the equivalent of the widely accepted industry standard, refined by AMI for MOS/LSI applications. The package consists of a plastic body, transfer-molded directly onto the assembled lead frame and die. The lead frame is copper alloy, with external pins tin plated. Internally, there is a 150μin. silver spot on the die attach pad and on each bonding fingertip. Gold bonding wire is attached with the thermosonic gold ball bonding technique.

Materials of the lead frame, the package body, and the die attach are all closely matched in thermal expansion coefficients, to provide optimum response to various thermal conditions. During manufacture every step of the process is rigorously monitored to assure maximum quality of the AMI plastic package.

Available in: 8, 14, 16, 18, 22, 24, 28, 40, 48 and 64 pin configurations.

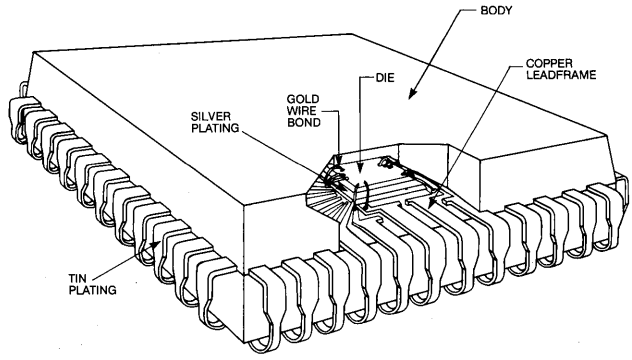


Plastic Chip Carrier

As in the ceramic chip carrier, the plastic chip carrier (P.C.C.) provides excellent packaging density for high pin count packages, but is an excellent cost alternative to ceramic. The P.C.C. is both surface and socket mountable, and has high lead strengths.

As all AMI plastic packages, it is transfer molded and thermosonically wire bonded. Die is mounted on a copper lead frame and extenal leads are tin plated.

Available in: 44, 68 and 84 pin configurations.

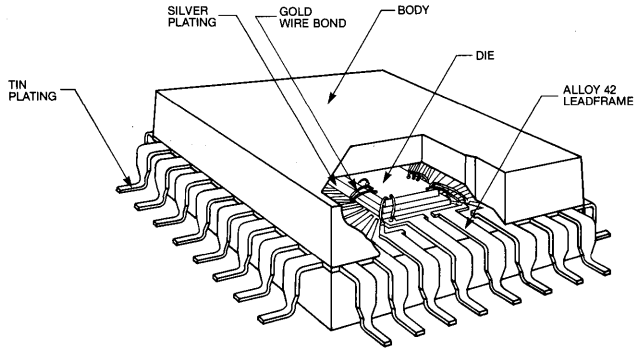


Mini-Flatpack

The mini-flatpack is a cost effective, transfer molded plastic package that provides high package density, surface mounting capabilities. It is a four sided alternative to the plastic dual-in-line package provided by AMI.

It is processed with a lead frame of alloy 42 gold thermosonic wire bonding, and tin plated external leads.

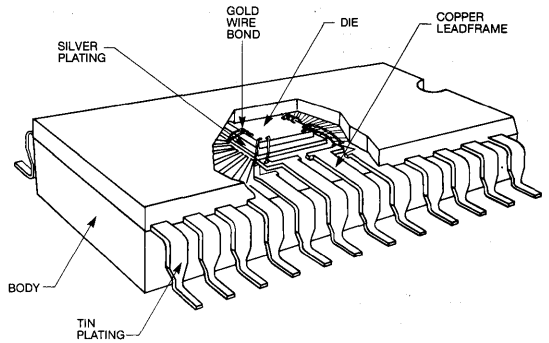
Available in 18, 22, 24, 28, 40, 44 and 80 pin configurations.



S.O.I.C.

The small outline integrated circuit (S.O.I.C) package is another of the low cost plastic packages in the AMI repertoire. Utilizing the dual-in-line configuration, a small dense, surface mountable package is originated, which maximizes the use of board space.

Available in: 16 and 28 pin configurations.

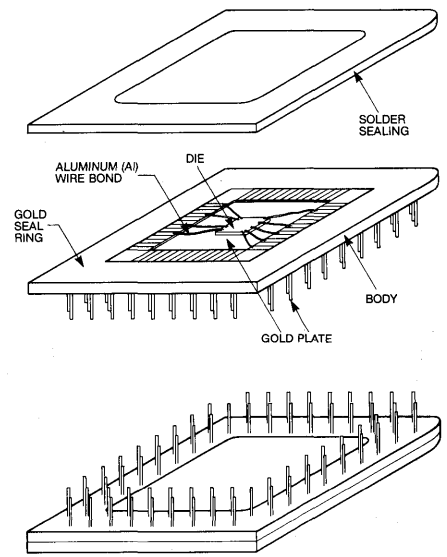


Pin Grid Array

Built on the same concept as the ceramic side brazed package, the Pin Grid Array is also suitable for high reliability applications but provides the opportunity for high density packaging with very high pin counts. The unique lead design makes it compatible with socket insertion mounting.

Most commonly supplied with an Al_2O_3 ceramic body, gold plating on the lead and die cavity, and sealed with a gold-tin eutectic solder on a Kovar/alloy 42 lead.

Available in: 68, 84, 100, 144 pin configurations.



Introduction

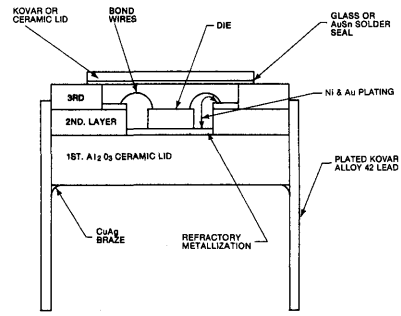
Ceramic Packages

The ceramic and cerdip packages provided by AMI are commonly used for high reliability applications. Glass or solder eutectic sealing and ceramic body yields excellent hermeticity characteristics, thereby insuring against device failure from moisture penetration. AMI supplies a full range of ceramic packages to meet many applications.

Ceramic Package

Industry standard high performance, high reliability package, made of three layers of Al_2O_3 ceramic and nickel-plated refractory metal. Either a low temperature glass sealed ceramic lid or a gold tin **eutectic** sealed Kovar lid is used to form the hermetic cavity of this package. Package leads are available with gold or tin plating for socket insertion or soldering.

Available in 14, 16, 18, 22, 24, 28 40 and 64 pin configurations.

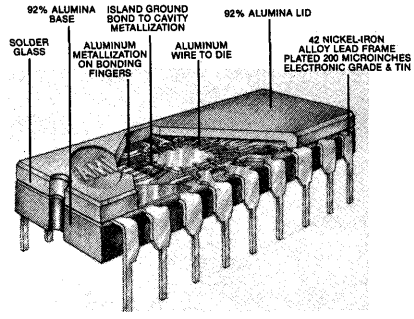


Cerdip Package

The Cerdip dual-in-line package has the same high performance characteristics as the standard three-layer ceramic package yet is a cost-effective alternative. It is a military approved type package with excellent reliability characteristics.

The package consists of an Alumina (Al_2O_3 base and the same material lid, hermetically fused onto the base with low temperature solder glass.

Available in 14, 16, 18, 20, 22, 24, 28 and 40 pin configurations.

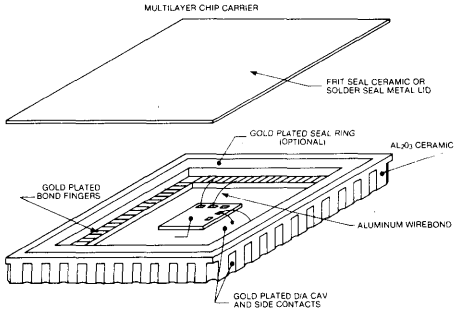


Chip Carrier Package

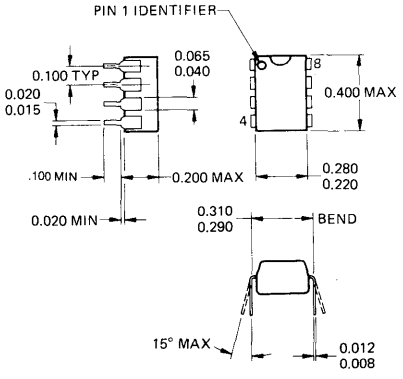
Chip carriers are the new industry standard in reducing package size. Built on the same concept as the highly reliable side-braze ceramic package, it is made of three layers of AL_2O_3 ceramic, refractory metallization and gold plating. The chip carrier also offers contact pads equally spaced on all four sides of the carrier resulting in increased package density, better electrical characteristics, and a more cost effective way of packaging IC devices.

The package comes with a gold tin **eutectic** sealed metal lid or the low cost glass sealed ceramic lid creating a standard hermetic cavity.

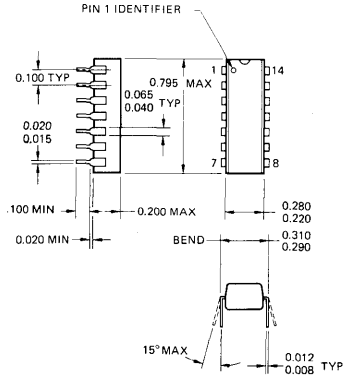
Available in 20, 24, 28, 40, 44, 68 and 84 LD standard 3-layer versions and 24, 28, 44 LD slam style on 50 mil center lines to the JEDEC standards.



8-Pin Plastic

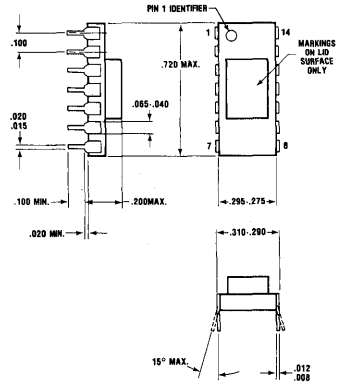


14-Pin Plastic

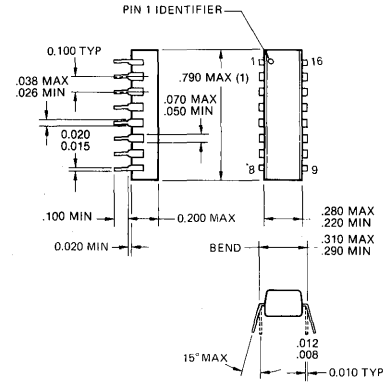


Packaging

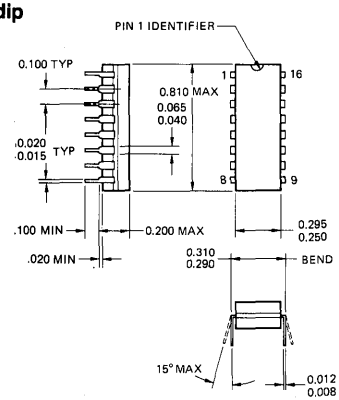
14-Pin Ceramic



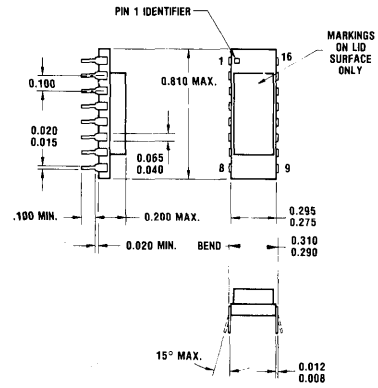
16-Pin Plastic



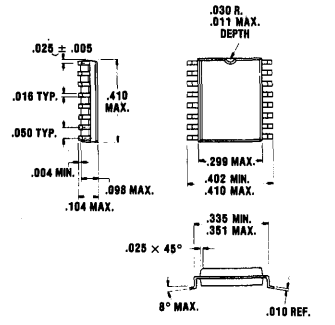
16-Pin Cerdip



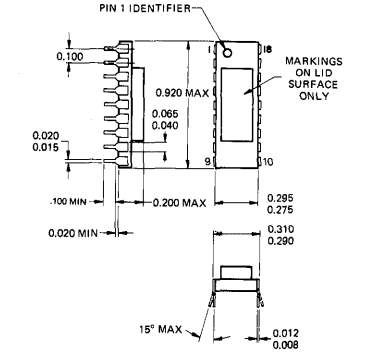
16-Pin Ceramic



16-Lead Plastic S.O.I.C.

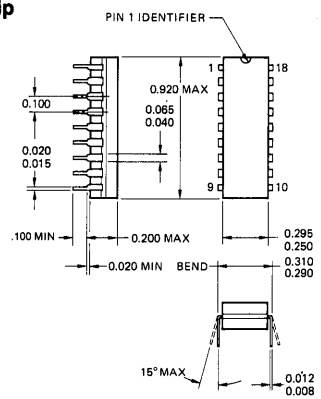


18-Pin Ceramic

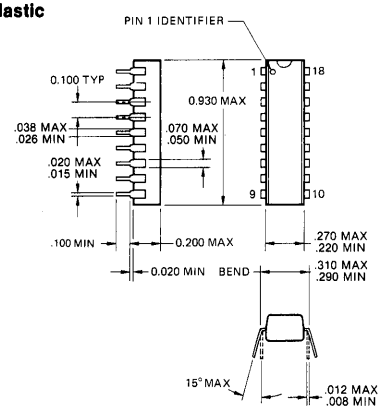


Packaging

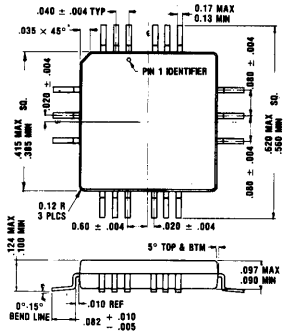
18-Pin Cerdip



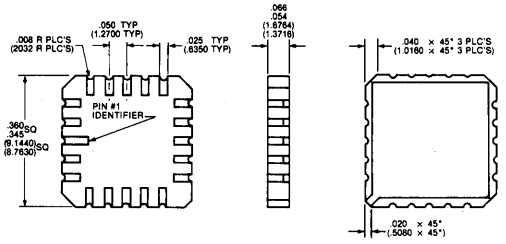
18-Pin Plastic



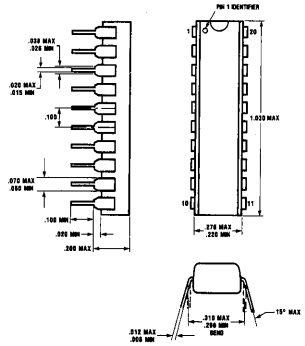
18-Lead Mini-Flat Pack



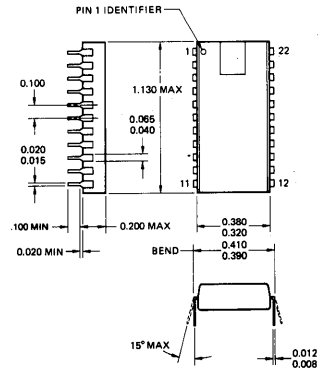
20-Lead Chip Carrier



20-Pin Plastic

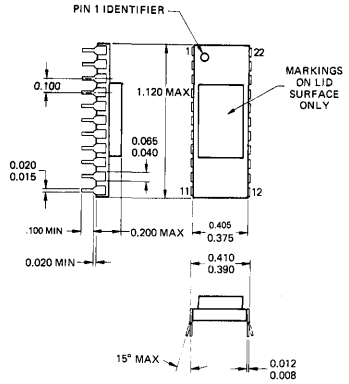


22-Pin Plastic

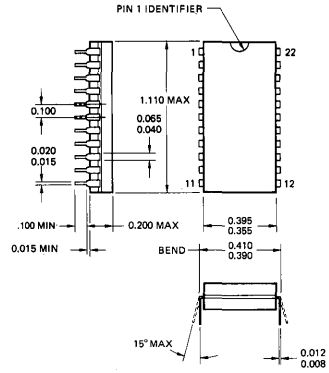


Packaging

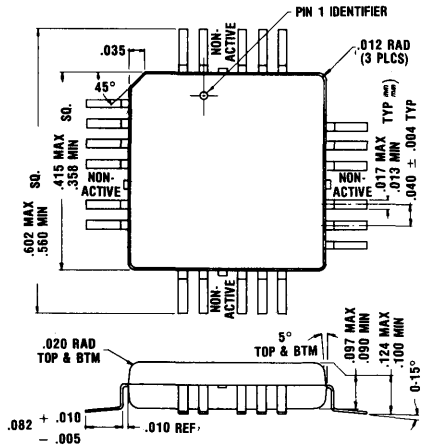
22-Pin Ceramic



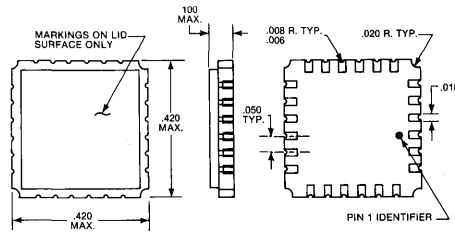
22-Pin Cerdip



22-Lead Mini-Flat Pack

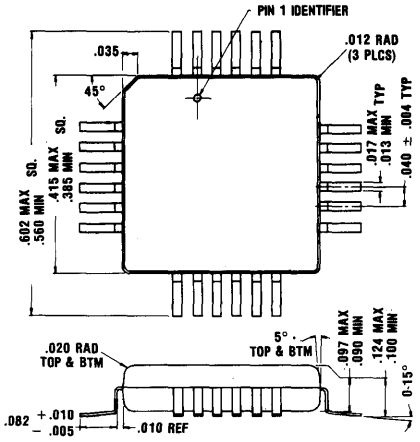


24-Lead Chip Carrier

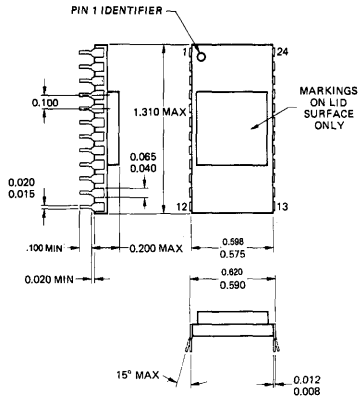


Packaging

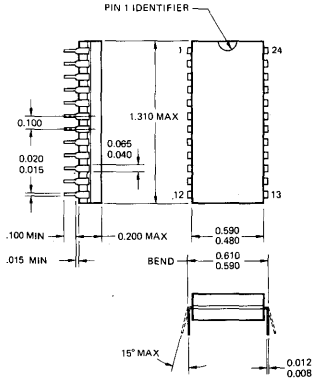
24-Lead Mini-Flat Pack



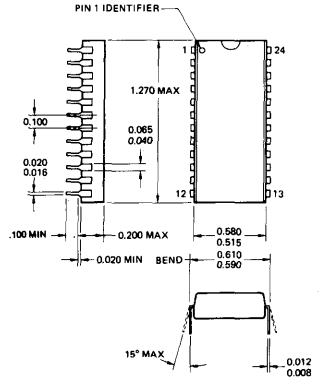
24-Pin Ceramic



24-Pin Cerdip



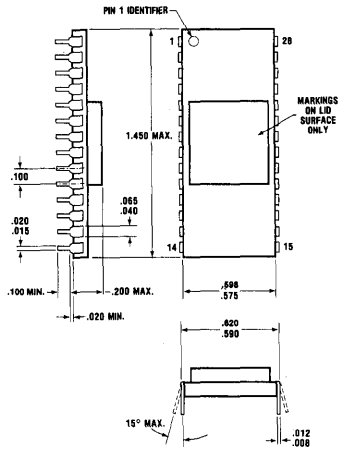
24-Pin Plastic



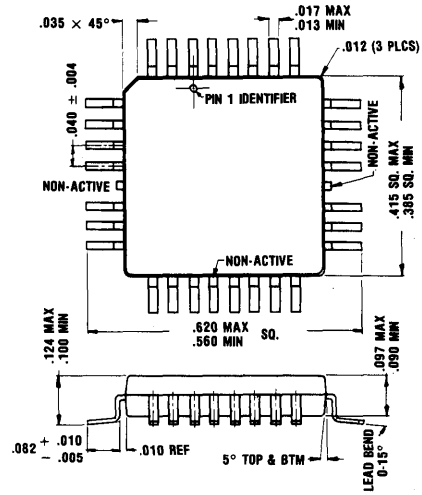
GENERAL INFORMATION

Packaging

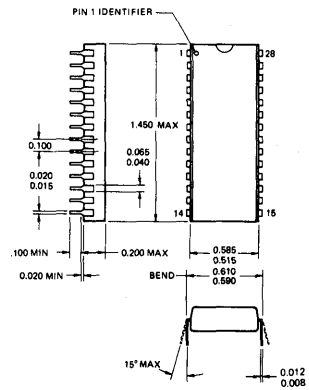
28-Pin Ceramic



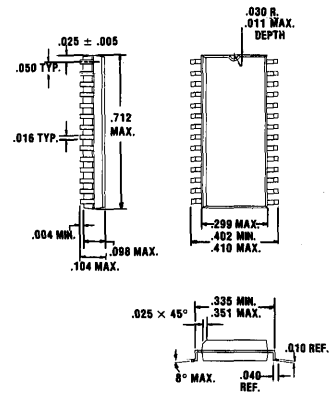
28-Lead Plastic Mini-Flat Package



28-Pin Plastic

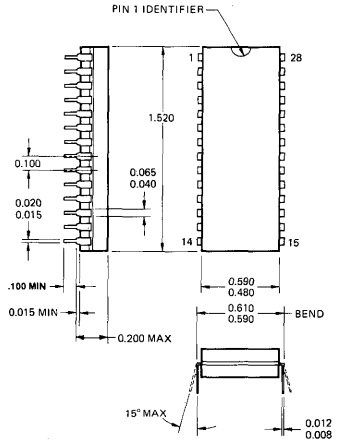


28-Lead Plastic S.O.I.C.

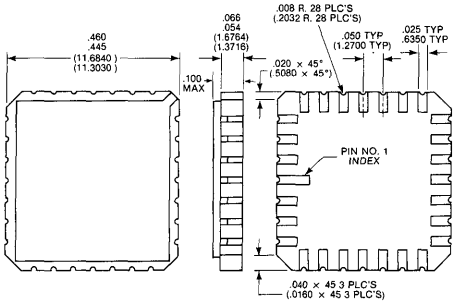


Packaging

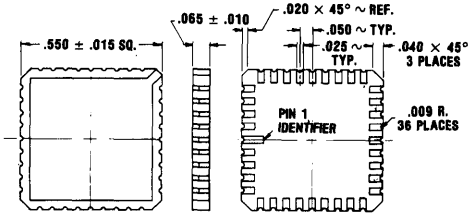
28-Pin Cerdip



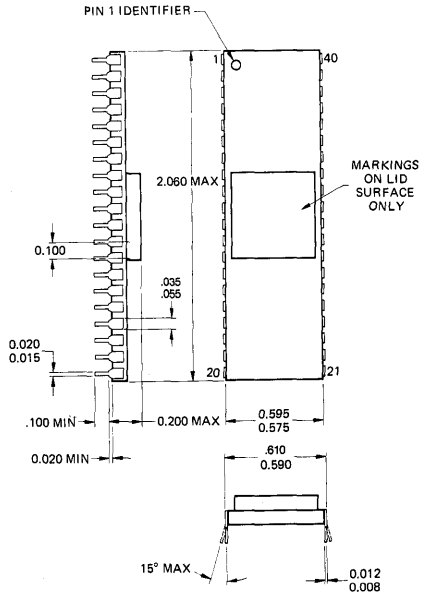
28-Lead Chip Carrier



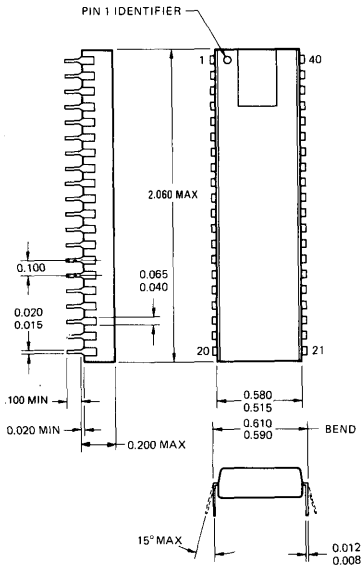
36-Lead Ceramic Chip Carrier



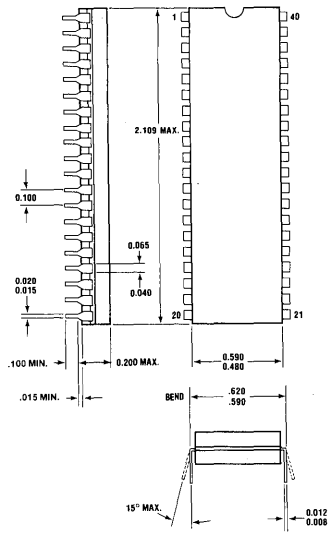
40-Pin Ceramic



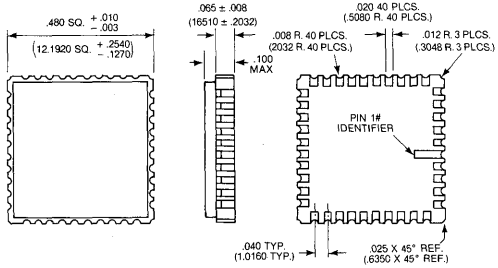
40-Pin Plastic



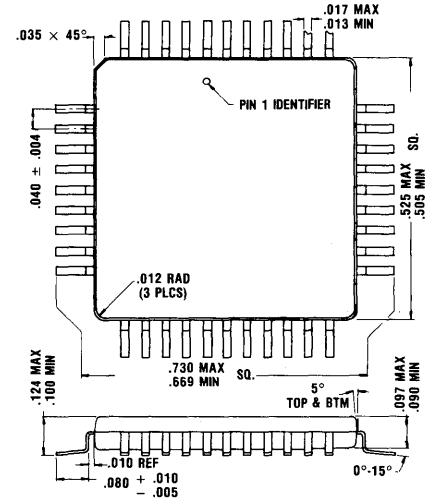
40-Pin Cerdip



40-Lead Chip Carrier

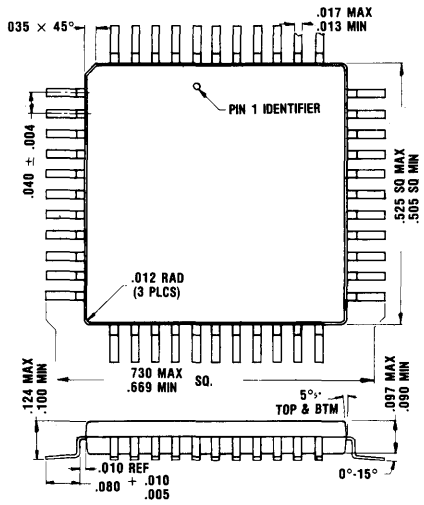


40 Lead Plastic Mini-Flat Package

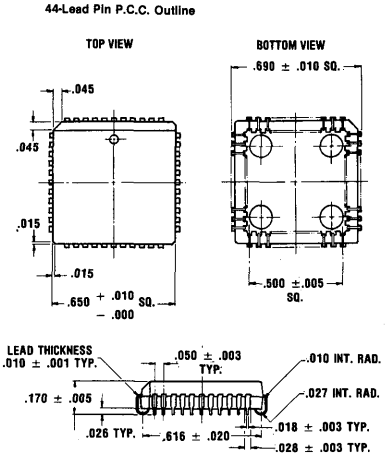


Packaging

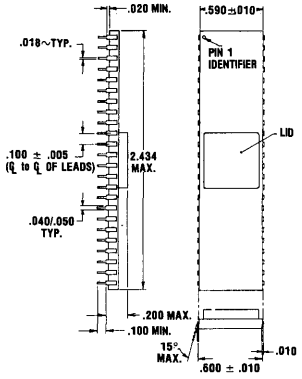
44-Lead Mini-Flat Pack



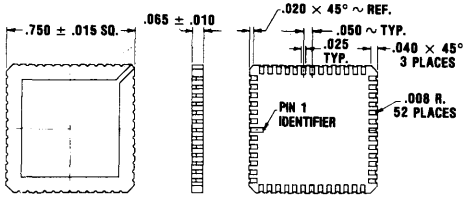
44-Lead Plastic Chip Carrier



48-Lead Ceramic



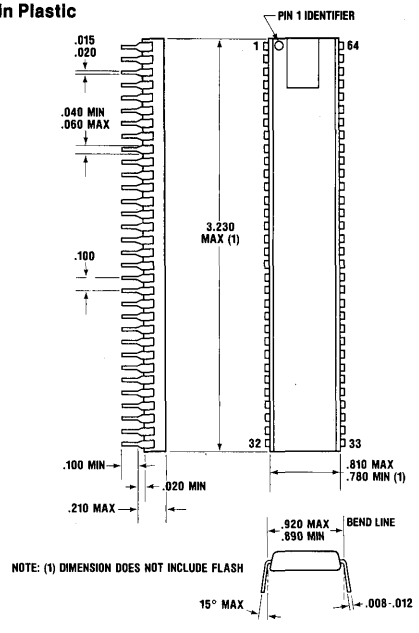
52-Lead Chip Carrier



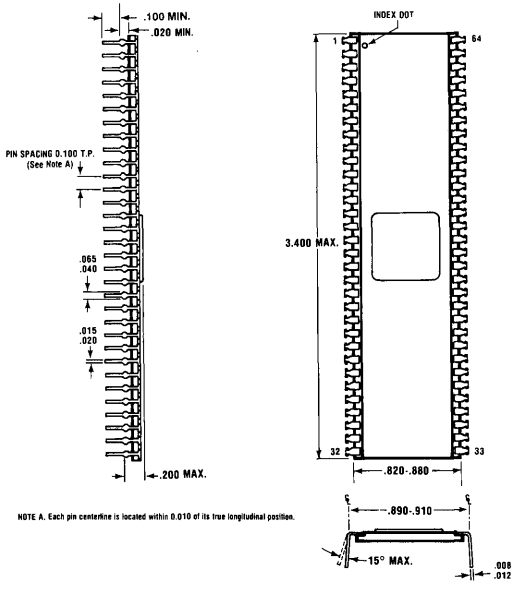
GENERAL INFORMATION

Packaging

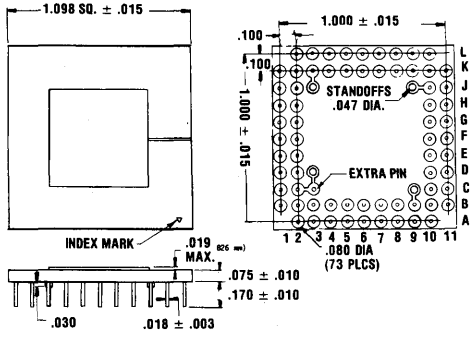
64-Pin Plastic



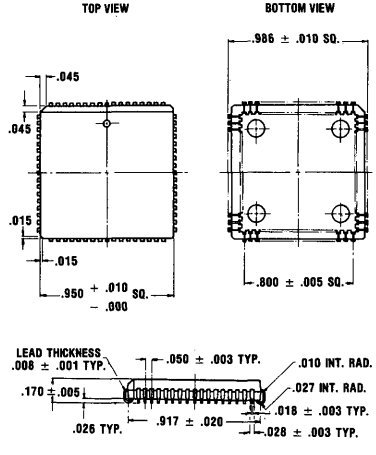
64-Pin Ceramic



68-Pin Grid Array

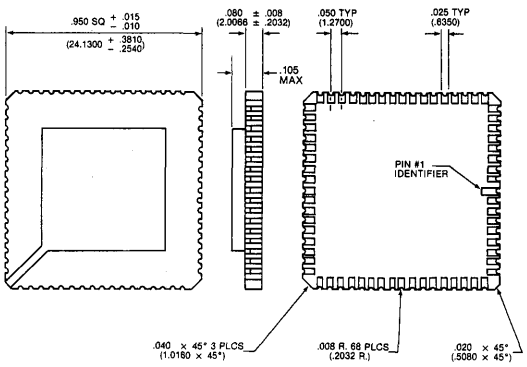


68-Lead Plastic Chip Carrier

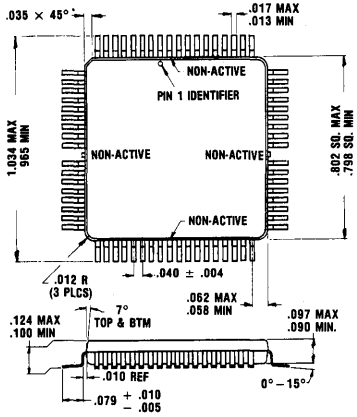


Packaging

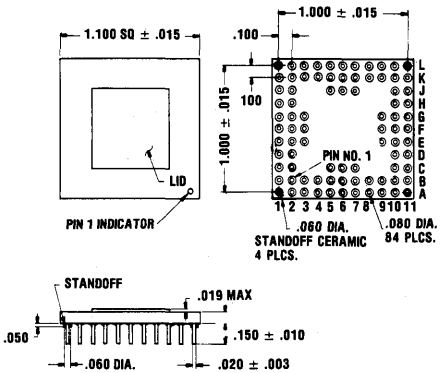
68-Lead Chip Carrier



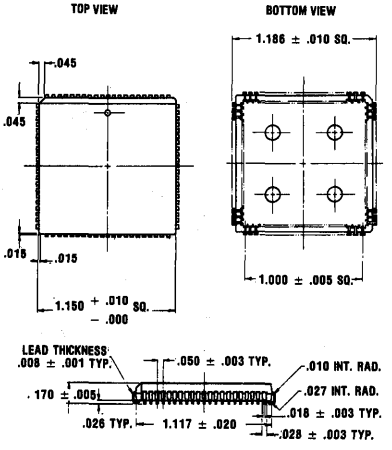
68-Lead Mini-Flat Pack



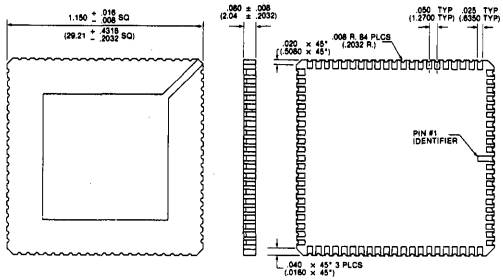
84-Pin Grid Array Outline



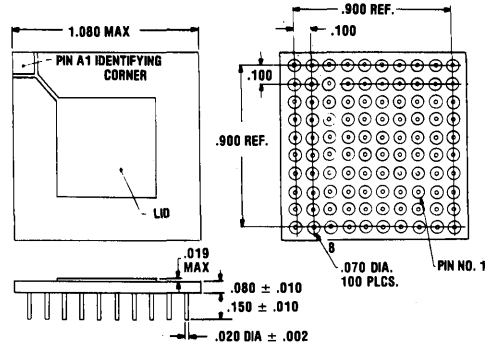
84-Lead Plastic Chip Carrier



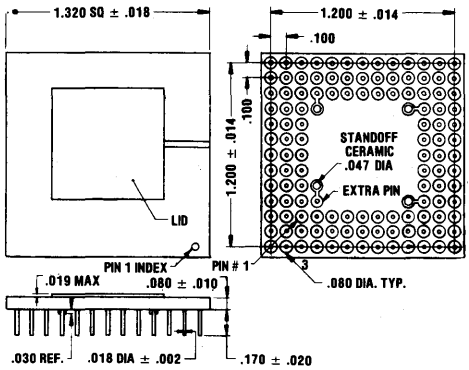
84-Lead Chip Carrier



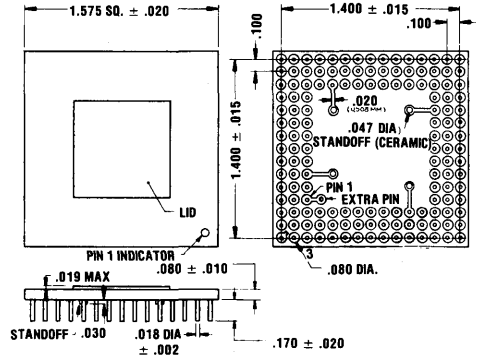
100-Pin Array Outline



120-Pin Grid Array Outline



144-Pin Grid Array Outline



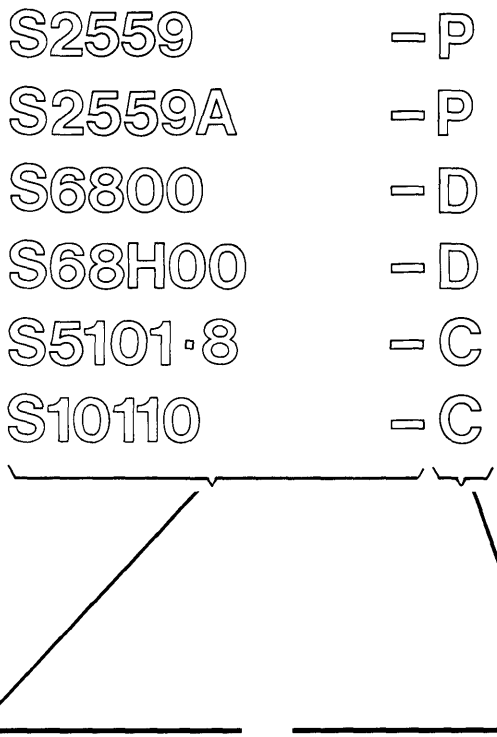
Ordering Information

Standard Products

Any product in this MOS Products Catalog can be ordered using the simple system described below. With this system it is possible to completely specify any standard device in this catalog in a manner that is compatible with AMI's order processing methods. The example below shows how this ordering system works and will help you to order your parts in a manner that can be expedited rapidly and accurately.

All orders (except those in sample quantities) are normally shipped in plastic containers or aluminum tube containers, which protect the devices from static electricity damage under all normal handling conditions. Either container is compatible with standard automatic IC handling equipment.

Any device described in this catalog is an AMI Standard Product. However, ROM devices that require mask preparation or programming to the requirements of a particular user, devices that must be tested to other than AMI Quality Assurance standard procedures, or other devices requiring special masks are sold on a negotiated price basis.



Device Number—prefix S, followed by four (or five*) numeric digits that define the basic device type. Versions to the basic device are indicated by an additional alpha or numeric digit as shown in the above examples.

*Organ Circuits

Package Type—a single letter designation which identifies the basic package type. The letters are coded as follows:

P — Plastic package

D — Cerdip package

C — Ceramic (three-layer) package

Terms of Sale

TERMS OF SALE — JANUARY 1984

1. ACCEPTANCE: THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. PAYMENT:

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefore shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. TAXES: Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority, (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. F.O.B. POINT: All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, United Parcel Service (UPS), Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. DELIVERY: Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. PATENTS: The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. INSPECTION: Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY: The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. PRODUCTS NOT WARRANTED BY SELLER: The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES EXPRESSED, STATUTORY OR IMPLIED INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INFRINGEMENT AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products contact Seller.

10. PRICE ADJUSTMENTS: Seller's unit prices are based on certain material costs. These materials include, among other things, gold packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. VARIATION IN QUANTITY: If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. CONSEQUENTIAL DAMAGES: In no event shall Seller be liable for special, incidental or consequential damages.

13. GENERAL:

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities domestic or foreign.

(g) Unless otherwise agreed in a writing signed by both Buyer and Seller, Seller shall retain title to and possession of all tooling of any kind (including but not limited to masks and pattern generator tapes) used in the production of products furnished hereunder.

(h) Buyer, by accepting these products, certifies that he will not export or re-export the products furnished hereunder unless he complies fully with all laws and regulations of the United States relating to such export or re-export, including but not limited to the Export Administration Act of 1979 and the Export Administration Regulations of the U.S. Department of Commerce.

(i) Seller shall own all copyrights in or relating to each product developed by Seller whether or not such product is developed under contract with a third party.

14. GOVERNMENT CONTRACT PROVISIONS: If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Defense Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be - i.e., "Contracting Officer" shall mean "Buyer", "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Rhodesia and Certain Communist Areas; 7-103.16, Contract Work Hours and Safety Standards Act - Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity Clause; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government (only to the extent that Buyer's contract is terminated for the convenience of the government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-103.24, Responsibility for Inspection; 7-103.25, Commercial Bills of Lading Covering Shipments Under FOB Origin Contracts; 7-103.27, Listing of Employment Openings; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.15, Examination of Records by Comptroller General; 7-104.20, Utilization of Labor Surplus Area Concerns.

Worldwide Sales Offices

United States

Northwest Region

HEADQUARTERS—3800 Homestead Road, Santa Clara, California 95051 ..... (408) 246-0330
TWX: 910-338-0018
or 910-338-0024
CALIFORNIA, 2960 Gordon Avenue, Santa Clara 95051 ..... (408) 738-4151
WASHINGTON, 20709 N.E. 232nd Avenue, Battle Ground 98604 ..... (206) 687-3101
WASHINGTON, 10655 N.E. 4th Street, Suite 400, Bellevue 98004 ..... (206) 462-8870

Southwest Region

CALIFORNIA, 2900 Bristol Street, Suite A-202, Costa Mesa 92626 ..... (714) 751-1634
CALIFORNIA, 2850 Pio Pico Drive, Suite L, Carlsbad 92008 ..... (619) 434-6031
ARIZONA, 7950 E. Redfield Road, Scottsdale 85260 ..... (602) 996-5638

Central Region

ILLINOIS, 500 Higgins Road, Suite 210, Elk Grove Village 60007 ..... (312) 437-6496
MICHIGAN, 29200 Vassar Avenue, Suite 221, Livonia 48152 ..... (313) 478-4220
COLORADO, 7346A So. Alton Way, Englewood 80112 ..... (303) 694-0629

Southeastern Region

FLORIDA, 139 Whooping Loop, Altamonte Springs 32701 ..... (305) 830-8889
NORTH CAROLINA, 5711 Six Forks Road, Suite 210, Raleigh 27609 ..... (919) 847-9468
ALABAMA, 555 Sparkman Drive, Suite 822, Huntsville 35805 ..... (205) 830-1435
TEXAS, 725 South Central Expressway, Suite A-9, Richardson 75080 ..... (214) 231-5721
(214) 231-5285
TEXAS, Austin 78746 ..... (512) 327-5286

Mid-Atlantic Area

PENNSYLVANIA, Axewood East, Butler & Skippack Pikes, Suite 230, Ambler 19002 ..... (215) 643-0217
VIRGINIA, Northway Building, 500 Westfield Road, Suite 26, Charlottesville 22906 ..... (804) 973-1213
INDIANA, 408 South 9th Street, Suite 201, Noblesville 46060 ..... (317) 773-6330
OHIO, 100 East Wilson Bridge Road, Suite 225, Worthington 43085 ..... (614) 436-0330

Northeastern Region

NEW YORK, 20F Robert Pitt Drive, Suite 208, Monsey 10952 ..... (914) 352-5333
MASSACHUSETTS, 24 Muzzey Street, Lexington 02173 ..... (617) 861-6530

Europe

HEADQUARTERS—Austria Microsystems International GmbH, Schloss Premstätten
8141 Unterpremstätten, Austria ..... (43)3136/3666

Sales Offices

ENGLAND, AMI Microsystems, Ltd., Princes House, Princes St., Swindon SN1 2HU ..... (0793) 37852
FRANCE, AMI Microsystems, S.A.R.L., 124 Avenue de Paris, 94300 Vincennes ..... (01) 374 00 90
WEST GERMANY, AMI Microsystems GmbH, Suite 237, Rosenheimer Strasse 30/32, 8000 Munich 80 ..... (089) 483081
ITALY, AMI Microsystems S.R.L., Piazzale Lugano, 9, 20158 Milano ..... (02) 3761275
or 3763022

Japan and Pacific Basin

JAPAN, Asahi Microsystems, Inc., 17F, Imperial Tower, 1-1-1, Uchisaiwai-Cho, Chiyoda-Ku, Tokyo 100 .... (81) 3-507-2371

Domestic Representatives

CANADA, Burnaby B.C.	Woodbery Elect. Sales Ltd.	(604) 430-3302
CANADA, Mississauga, Ontario	Vitel Electronics	(416) 676-9720
CANADA, Ottowa, Ontario	Vitel Electronics	(613) 592-0090
CANADA, St. Laurent, Quebec	Vitel Electronics	(514) 331-7393
CANADA, Stittsville, Ontario	Vitel Electronics	(613) 582-0090
IOWA, Cedar Rapids	Comstrand, Inc.	(319) 377-1575
MASSACHUSETTS, Tyngsboro	Comptech	(617) 649-3030
MINNESOTA, Minneapolis	Comstrand, Inc.	(612) 788-9234
NEW YORK, Clinton	Advanced Components	(315) 853-6438
PUERTO RICO, San Juan	Electronic Tech. Sales, Inc.	(809) 790-4300

Domestic Distributors

ALABAMA, Huntsville	Schweber Electronics	(205) 882-2200
ARIZONA, Phoenix	Kierulff Electronics	(602) 243-4101
ARIZONA, Scottsdale	Western Microtechnology	(602) 948-4240
ARIZONA, Tempe	Anthem Electronics	(602) 244-0900
ARIZONA, Tucson	Kierulff Electronics	(602) 624-9986
CALIFORNIA, Canoga Park	Schweber Electronics	(213) 999-4702
CALIFORNIA, Chatsworth	Anthem Electronics	(213) 700-1000
CALIFORNIA, Cupertino	Western Microtechnology	(408) 725-1660
CALIFORNIA, Irvine	Schweber Electronics	(714) 863-0220
CALIFORNIA, Los Angeles	Kierulff Electronics	(213) 725-0325
CALIFORNIA, Palo Alto	Kierulff Electronics	(415) 968-6292
CALIFORNIA, Sacramento	Schweber Electronics	(916) 929-9732
CALIFORNIA, San Diego	Anthem Electronics	(619) 453-4871
CALIFORNIA, San Diego	Kierulff Electronics	(619) 278-2112
CALIFORNIA, San Jose	Anthem Electronics	(408) 946-8000
CALIFORNIA, Santa Clara	Schweber Electronics	(408) 748-4700
CALIFORNIA, Tustin	Anthem Electronics	(714) 730-8000
CALIFORNIA, Tustin	Kierulff Electronics	(714) 731-5711
CANADA, Alberta, Calgary	Future Electronics	(403) 259-6408
CANADA, British Columbia, Vancouver	Future Electronics, Inc.	(604) 438-5545
CANADA, Ontario, Downsview	Cesco Electronics, Ltd.	(416) 661-0220
CANADA, Ontario, Downsview	Future Electronics, Inc.	(416) 663-5563
CANADA, Ottawa	Future Electronics, Inc.	(613) 820-8313
CANADA, Quebec, Montreal	Cesco Electronics, Ltd.	(514) 735-5511
CANADA, Quebec, Point Claire	Future Electronics, Inc.	(514) 694-7710
CANADA, Quebec	Cesco Electronics, Ltd.	(418) 687-4231
COLORADO, Englewood	Anthem Electronics	(303) 790-4500
COLORADO, Englewood	Kierulff Electronics	(303) 790-4444
CONNECTICUT, Danbury	Schweber Electronics	(203) 792-3742
CONNECTICUT, Wallingford	Kierulff Electronics	(203) 265-1115
FLORIDA, Altamonte Springs	Schweber Electronics	(305) 331-7555
FLORIDA, Ft. Lauderdale	Kierulff Electronics	(305) 486-4004
FLORIDA, Hollywood	Schweber Electronics	(305) 927-0511
FLORIDA, St. Petersburg	Kierulff Electronics	(813) 576-1966
GEORGIA, Norcross	Kierulff Electronics	(404) 447-5252
GEORGIA, Norcross	Schweber Electronics	(404) 449-9170
ILLINOIS, Elk Grove Village	Kierulff Electronics	(312) 640-0200
ILLINOIS, Elk Grove Village	Schweber Electronics	(312) 364-3750
IOWA, Cedar Rapids	Schweber Electronics	(319) 373-1417
KANSAS, Overland Park	Schweber Electronics	(913) 492-2921
MARYLAND, Baltimore	Kierulff Electronics	(301) 247-5020
MARYLAND, Gaithersburg	Schweber Electronics	(301) 840-5900
MASSACHUSETTS, Bedford	Schweber Electronics	(617) 275-5100
MASSACHUSETTS, Billerica	Kierulff Electronics	(617) 935-5134
MICHIGAN, Livonia	Schweber Electronics	(313) 525-8100
MINNESOTA, Eden Prairie	Schweber Electronics	(612) 941-5280
MINNESOTA, Edina	Kierulff Electronics	(612) 941-7500
MISSOURI, Earth City	Scheweber	(314) 739-0526
MISSOURI, Maryland Heights	Kierulff Electronics	(314) 739-0855
NEW HAMPSHIRE, Manchester	Schweber Electronics	(603) 625-2250
NEW JERSEY, Fairfield	Kierulff Electronics	(201) 575-6750
NEW JERSEY, Fairfield	Schweber Electronics	(201) 227-7880
NEW YORK, Rochester	Schweber Electronics	(716) 424-2222
NEW YORK, Westbury L.I.	Schweber Electronics	(516) 334-7474
NORTH CAROLINA, Raleigh	Kierulff Electronics	(919) 872-8410
NORTH CAROLINA, Raleigh	Schweber Electronics	(919) 867-0000

Domestic Distributors

OHIO, Beachwood	Schweber Electronics	(216) 464-2970
OHIO, Cleveland	Kierulff Electronics	(216) 587-6558
OHIO, Dayton	Schweber Electronics	(513) 439-1800
OKLAHOMA, Tulsa	Kierulff Electronics	(918) 252-7537
OKLAHOMA, Tulsa	Schweber Electronics	(918) 622-8000
OREGON, Portland	Kierulff Electronics	(503) 641-9150
PENNSYLVANIA, Horsham	Schweber Electronics	(215) 441-0600
PENNSYLVANIA, Pittsburgh	Schweber Electronics	(412) 782-1600
TEXAS, Austin	Kierulff Electronics	(512) 835-2090
TEXAS, Austin	Schweber Electronics	(512) 458-8253
TEXAS, Dallas	Kierulff Electronics	(214) 343-2400
TEXAS, Dallas	Schweber Electronics	(214) 661-5010
TEXAS, Houston	Kierulff Electronics	(713) 530-7030
TEXAS, Houston	Schweber Electronics	(713) 784-3600
UTAH, Salt Lake City	Kierulff Electronics	(801) 973-6913
WASHINGTON, Redmond	Anthem Electronics	(206) 881-0850
WASHINGTON, Tukwila	Kierulff Electronics	(206) 575-4420
WISCONSIN, Brookfield	Schweber Electronics	(414) 784-9020
WISCONSIN, Waukesha	Kierulff Electronics	(414) 784-8160

International Representatives & Distributors

ARGENTINA, Buenos Aires	YEL S.R.L.	(54) 1-46 2211
AUSTRALIA, Preston, Victoria	Rifa Pty. Ltd.	61 (3) 480 1211
BRAZIL, Sao Paulo	Datatronix Electronica Ltda.	11-826-0111
CHILE	Victronics Ltda.	56(2)36440-30237
DENMARK,	Semicap A/S	(01) 22150
ENGLAND, Derby	Quarndon Electronics Ltd.	(0332) 32651
ENGLAND, Harlow, Essex	VSI Electronics (UK) Ltd.	(0279) 2935477
FINLAND, Espoo	OY Atomica AB	(80) 423533
FRANCE, Sevres	Tekelec Airtronic	(01) 534-75-35
HONG KONG, Kowloon	Electrocon Products Ltd.	3- 687214-6
INDIA, Nagar, Punjab	Semiconductor Complex Ltd.	91 (172) 87495
ISRAEL, Tel Aviv	Professional Elect. Ltd.(P.E.L.)	410656
ITALY	International Commerce Co.	
JAPAN, Tokyo	Internix, Inc.	(81) 3-369-1101
MEXICO	Dicopel S.A.	(903) 561-3211
NETHERLANDS, Badhoevedere	Techmation Elec. NV	(04189) 2222
NETHERLANDS, Rotterdam	DMA Nederland, BV	010-361288
NEW ZEALAND, Auckland	David P. Reid (NZ) Ltd.	(9) 488049
NORWAY, Oslo	Rifa-Hoyem A/S	47-413755
SINGAPORE, Singapore	Dynamar Int'l. Ltd.	(65) 746 6188
SOUTH AFRICA, Transvaal	Promilect	(011) 485712
SOUTH KOREA, Seoul	Kortronics Enterprise	2 634-5497
SPAIN, Madrid	Actron	(00341) 4026085
SWEDEN, Spanga	A.B. Rifa	(08) 7522500
SWITZERLAND, Zurich	W. Moor AG	(01) 8406644
TAIWAN, Taipai	Promotor Co., Ltd.	(02) 767-0101
WEST GERMANY, Berlin	Aktiv Elektronik GmbH	(030) 6845088
WEST GERMANY, Frankenthal	Gleichman	
WEST GERMANY, Munich	Dema Electronic GmbH	(89) 28 80 18
WEST GERMANY, Schleswig	Ing. Bruo Dreyer	(04621) 24055
WEST GERMANY, Stuttgart	Ditronic GmbH	0711/724844
WEST GERMANY, Viersen	Mostron Halbieitervertriebs	(0216) 17024
YUGOSLAVIA, Ljubljana	ISKRA/Standard/Iskra IEZE	(051) 551-353