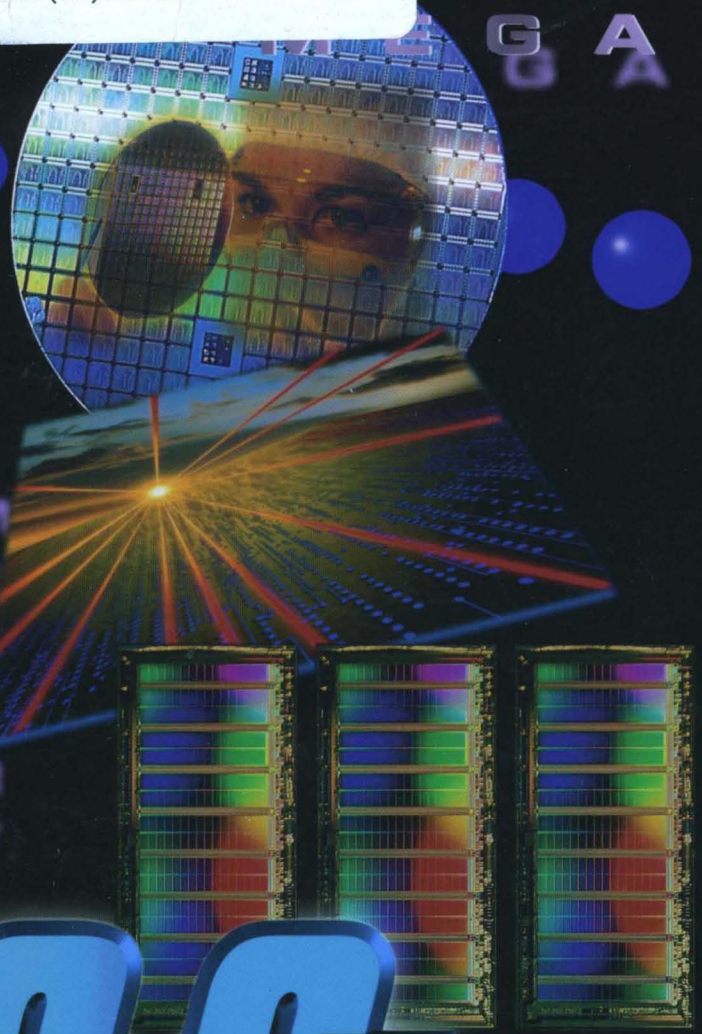
American Microsystems, Inc.

0.8 micron CMOS Gate Array Data Book

GACELL



MEMORY

0.8u

AMI SEMICONDUCTORS

0.8 Micron CMOS Gate Array Data Book

AMI SEMICONDUCTORS

Printed in U.S.A.

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GENERAL INTRODUCTION

AMI Semiconductors - Making ASICs Easier for More Than a Quarter Century

American Microsystems, Inc. (AMI) pioneered the development of the world's first custom MOS ICs in 1966. With more experience than any other ASIC vendor, you can be assured that when you bring your ASIC development project to AMI, you are working with a dependable team that has the depth of experience to provide you with an optimum solution, on time and on budget.

The vision shared by all employees at AMI is expressed in our mission statement:

We will delight our customers by producing products that meet or surpass their quality, reliability, cost and delivery needs.

AMI strives to realize this vision by offering a range of products and services aimed at improving cycle time, reducing overall design cost, achieving world-class reliability, and designing to customer need. AMI provides a full range of gate array, standard cell, and mixed-signal ASICs, mixed-signal and digital ASIC design software and services, and modular foundry services. AMI's Standard Products division offers mask-programmable ROMs and programmable electrically erasable logic devices (PEELs™). AMI's Application-Specific Integrated Systems (ASIS®) division specializes in contract manufacturing solutions.

AMI is a corporation whose headquarters and ASIC design and manufacturing operations are located in a 317,000 square foot facility in Pocatello, Idaho; the Standard Products and ASIS divisions are also headquartered in Pocatello. AMI has a software R&D facility in Twain Harte, California, and owns a subsidiary called AMI (Philippines), Inc., located in a 45,000 square foot facility in Manila, Philippines, for test of AMI's products.

Markets

- Communications
- Computers
- Military
- Automotive
- Consumer
- Industrial

Sales and Distribution

- Six full-service sales and technical support offices located in key markets throughout North America.
- Eight additional satellite offices in secondary markets.
- Three technical service centers, located in San Jose, Los Angeles, and Tokyo, which offer customers a full range of digital ASIC design resources and services.
- 43 sales representative offices throughout North America, with more than 110 outside salespeople.
- AMI's standard product offerings are available through 87 distributors' offices in the United States and Canada.
- In Europe, AMI is represented by distributors or sales representatives in the United Kingdom, Germany, France, Italy, Spain, Netherlands, Belgium, and Denmark. AMI maintains a technical service center in Dresden, Germany.
- In addition to a sales office in Tokyo, Japan, AMI is represented by distributor/sales representatives in that country and in Singapore, Taiwan, Australia and Israel.

General Introduction

American Microsystems, Inc.

Products

ASICs

- Mixed-signal, standard cell, and gate array ASICs. AMI's ASIC products are supported with a library of more than 500 digital cells and megacells, designed in the company's 0.8 and 1.0 micron CMOS process technologies and compatible with all popular industry-standard CAE environments.

PLDs

- CMOS PEEL (Programmable Electrically Erasable Logic) and PEEL Array devices. Built with an advanced CMOS EEPROM process and offering operating speeds as fast as 7.5 nanoseconds, AMI's high performance PEEL products bring the benefits of reprogrammability and low power consumption to logic configurations in high density printed circuit boards.

Mask Programmable ROMs (read-only memories)

- AMI's ROMs offer capacities from 16 megabits to 16 kilobits, response times as fast as 90 nanoseconds, and require only a 3 to 5 volt power supply. Design flexibility is afforded by multiple user-definable control pins and a variety of packaging options.

ASIC Design Software

- Mixed-Signal Design Solution (MSDS)™ software—the first mixed-signal design package that enables ASIC designers to automatically generate customized analog behavioral models at their own workstations.
- ACCESS Design Tools™ software—for optimizing ASIC design at customer sites. AMI's ACCESS product line includes Design Analyzer™ and Pattern Analyzer™ software, as well as the company's NETRANS™ FPGA-to-ASIC conversion software for use at customer sites, and NETRANSplus™ for fast system prototyping with FPGAs.

System-Level Solutions (ASIS Division)

- Contract design and manufacturing—Thru-Hole Technology (THT), Surface-Mount Technology (SMT), Hybrids, and Multichip Modules. PC Cards (JEIDA 4.0/4.1, PCMCIA 1.0/2.0).

Services

PLD/ASIC Conversions

- NETRANS/PALTRANS™—the first fully automated PLD-to-ASIC conversion service offered by an ASIC vendor.
- NETRANSplus —the first fully automated ASIC-to-FPGA conversion service offered by an ASIC vendor to provide quick-turn prototyping.

ASIC Test

- NETSCAN™—AMI's automated ASIC test-pattern generator software for increasing fault coverage.
- NETTAG™—AMI's automated JTAG insertion tool for boundary scan testing.

ASIC Design

- Design Analyzer, Gate Gobbler™, Five-Corner Logic Simulator™, and Accolade™ cell-compiler software—for optimizing customers' ASIC design and swiftly tailoring logic functions to customers' specific requirements.

Foundry/Manufacturing

- Advanced CMOS technology—brings low power consumption, high noise immunity, and high circuit densities to digital and analog/digital ASICs.
- Feature sizes as small as 0.8 micron (drawn).
- Process modularity—enables automated fabrication steps to be variously combined in ways tailored to meet the specific manufacturing requirements of analog, digital, and mixed-signal devices.
- "Flexible factory"—provides a diversity of fabrication processes and schedule options to meet customer requirements.
- Wafer gold bumping—available as a foundry service or as an extension of AMI's ASIC services to support TAB, flip-chip, or chip-on-chip applications.

Corporate Headquarters

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INTRODUCTION TO CORE & PAD LOGIC WITH LIBRARY CHARACTERISTICS

AMI8G 0.8 micron CMOS Gate Array

AMI's "AMI8Gx" series of 0.8μm gate arrays exploits a proprietary power grid and track routing architecture on a compact, channelless, sea-of-gates design to provide one of the highest performance, cost effective array products available today.

Features

- **Excellent performance:**
  - 250 MHz maximum toggle rate on clocked flip-flops (T_J = 135°C).
  - 200 ps delay (FO = 2) for a 2-input NAND gate.
- **Operating Temp ranges from -55 to 125°C:** Few competing products allow this range.
- **Clock tree generation:** ≤ 400 ps clock skew (fan out = 3500 at 80 MHz).
- **1 to 16 mA drive per single I/O cell:** Selectable I/O drive with controllable slew rate. Extra I/O cells allow combined I/O drive up to 96 mA without reducing pad count.
- **Automatic Test Program Generation:** Includes scan macros (NETSCAN™) for high fault coverage.
- **JTAG Boundary Scan macro support**
- **Full operating voltage range from 2.7V to 5.5V**
- **ESD protection > 2kV; latchup > 100 mA**
- **Cost driven architecture:**
  - Offers both two and three level metal interconnect to provide the lowest user cost for the number of gates and pads required.
  - Provides 6 extra power pads per corner to preserve more I/O cells for signal use.
  - Contains extra I/O cells to provide extra drive without wasting bond pads.
- **Extensive library for quick design:**
  - Complete primary cell and I/O library.
  - Synchronous single port RAM compilers with over 2000 compiled RAM sizes from 32 x 1 to 1K x 32-bits.
  - MG65C02, MG29C01, MG29C10, MG80C85, MG82Cxx, MGMC51 megacells.
  - Various datapath logic synthesizers (FIFOs, multipliers, adders, barrel shifters).
- **Wide range of packaging:** Full QFP and LCC line, DIPs and PGAs, individual die, (ball grid array package under study). Burn-in capability as needed.
- **3V, 5V, and combined 3V/5V operation:** Each individual pad cell can be driven independently by a 3V or 5V supply. 3V to 5V and 5V to 3V level shift is available in all I/O cells. Core can be either 3V for low power or 5V for high speed.
- **Power equals 3.2 μW/MHz/cell**

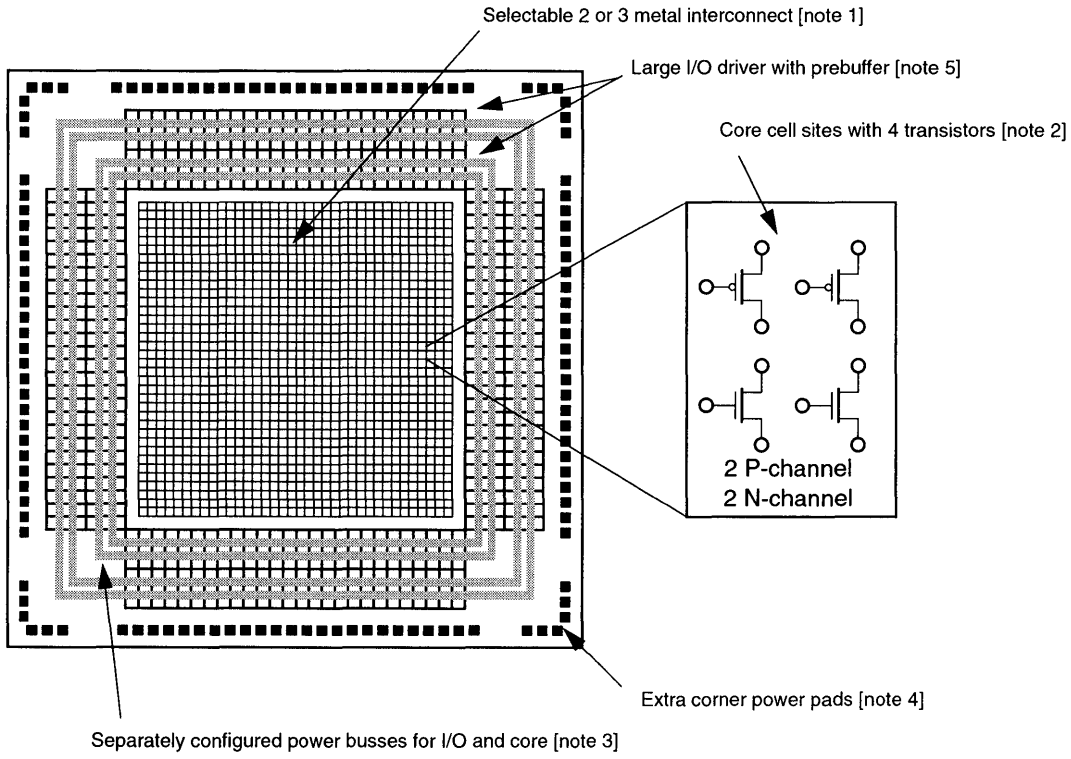
AMI8Gx Gate Array Family

Part Number	Raw Gates	Usable Gates[1]		Available I/O Cells	Available Bond Pads[2]
		Triple Metal	Double Metal		
AMI8G663	657,972	432,180	324,526	732	528
AMI8G392	392,616	259,920	194,256	564	424
AMI8G247	246,790	172,750	123,400	448	336
AMI8G201	200,740	140,500	100,400	404	304
AMI8G142	135,744	90,496	67,872	340	256
AMI8G93	90,720	58,320	44,064	276	208
AMI8G65	65,608	42,812	32,248	232	176
AMI8G55	54,000	35,000	26,500	212	160
AMI8G44	44,620	25,760	22,080	192	144
AMI8G34	34,000	22,400	16,800	168	128
AMI8G21	20,904	13,728	10,296	132	100
AMI8G15	15,048	9,768	7,392	112	84
AMI8G9	9,180	5,916	4,488	88	68
AMI8G5	5,304	3,432	2,652	68	52

Notes: 1. Exact usable gate count will vary depending on design interconnect and macro selection.
2. 24 optional fixed power pins (6 in each corner) are not included in this number.

AMI8S 0.8 micron CMOS Gate Array

FIGURE 1: GATE ARRAY ARCHITECTURE



Architectural Overview

Some important elements of the AMI8Gx gate array family are:

- **[Note 1]** Drawn gate length of 0.8 micron; two or three level metal interconnect selectable.
- **[Note 2]** Two p-channel and two n-channel transistors per site (or cell). Sites are arrayed in a sea-of-gates structure that can allow interconnect routing over active sites. Also, p-channel transistors are sized larger than the stronger n-channel transistors in each cell to provide better matched rise and fall times.
- **[Note 3]** Four separate power busses for I/O cells to allow separate supplies for output buffers, input buffers, and mixed V_{DD} levels all on an individual I/O cell basis. Two separate power busses for core logic (not shown).
- **[Note 4]** 24 (six per corner) fixed power pads (not included in Bond Pad count in Table 1) available on each array for customer use.
- Each I/O cell can be configured as 5V V_{DD}, 3V V_{DD}, V_{SS}, or signal I/O.
- **[Note 5]** Each I/O cell has selectable drive from 1 mA to 16 mA. All I/O cell logic can be built in the I/O cell prebuffer. Level shifting (3V to 5V or 5V to 3V) may require the use of a few core gates.

Product Applications

The family's extended temperature and voltage operation range make it well suited for telecom, industrial, and military applications. The low cost structure also makes it ideal in computer and office automation ASIC requirements.

FPGA OR PAL CONVERSION: AMI can convert netlists from most FPGA and PAL devices to a more cost and performance effective AMI8Gx gate array design for volume production.

2ND SOURCE EXISTING PRODUCTS: Netlist conversion capabilities from AMI allow a competitive alternate supply with AMI8Gx for current high volume designs.

NEW DESIGN CAPTURE: AMI8Gx design is supported by many popular third party software platforms, as well as AMI's Enhanced Design Utilities™ (EDU) environment.

PROCESS UPGRADE: Designs done in AMI's 1.25μm and 1.0μm gate array families can easily be upgraded to the AMI8Gx family. The AMI ASIC Standard Library provides a common netlist design base.

ASIC Design Tools and Methodology

AMI8Gx and other AMI ASIC families are supported on popular third party products:

- Cadence™
- Mentor Graphics®
- Synopsys®
- Viewlogic®
- Intergraph®
- Verilog® simulation
- IKOS® simulation accelerator (AMI's sign-off simulator)

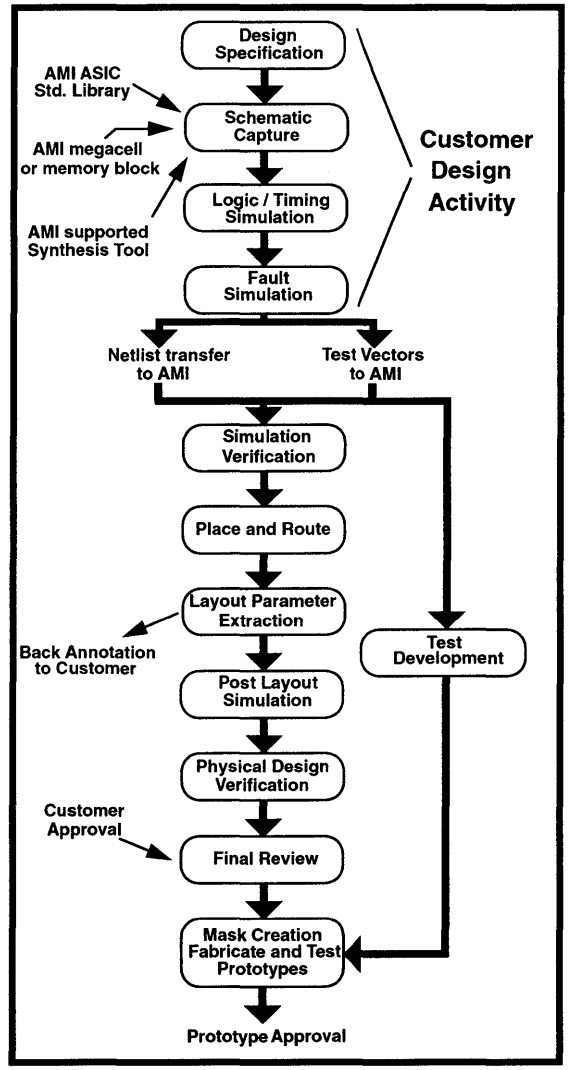
AMI has maintained critical proprietary software tools to ensure a tight, well coupled design to our silicon process. This methodology includes our expert-system design analysis tools, AMI's Enhanced Design Utilities (EDU), a software support methodology that covers the complete set of wafer processing possibilities, and a dedicated, experienced engineering staff that can assist at any level of the design process.

AMI Design Flow

AMI will supply an AMI8Gx design kit which includes a cell library containing symbols, simulation models and software for design verification, timing calculations, and netlist generation. For pre-layout timing simulations, capacitance values derived from statistical averages of known layouts are used. Once actual layout is completed by AMI, a post-layout interconnect capacitance table will be supplied for final validation of device timing.

Figure 2 shows a typical design flow for a new design.

FIGURE 2: ASIC DESIGN FLOW



AMI8S 0.8 micron CMOS Gate Array

AMI Design Flow (cont.)

Working with an AMI design center, the customer is responsible for capturing and verifying the design using the AMI ASIC Standard Library. He is also responsible for creating the test vectors that will eventually serve as the logical part of the manufacturing test. Software aids such as logic synthesis, megacells, automatic test program generation, netlist rule checkers, etc. can greatly speed up this process. (A fault coverage check of the test vector set is optional and can be done as an additional service.)

When the design is received by the factory, the "Design Start Package" is reviewed by AMI engineers. This start package, which is completed by the customer, contains the device specification, netlist, critical timing paths, and test vectors. The design is pre-screened on the EDU and then resimulated on IKOS, AMI's sign-off simulator. The results are compared to the customer's simulation from the third-party CAE tool.

Once the design has passed the initial screening it is then ready for placement and routing. The layout proceeds by first placing memory and megacells, assigning priority to critical paths, and designing the distribution and buffering of clocks. Next, the layout is completed with automatic place-and-route on the balance of the circuit.

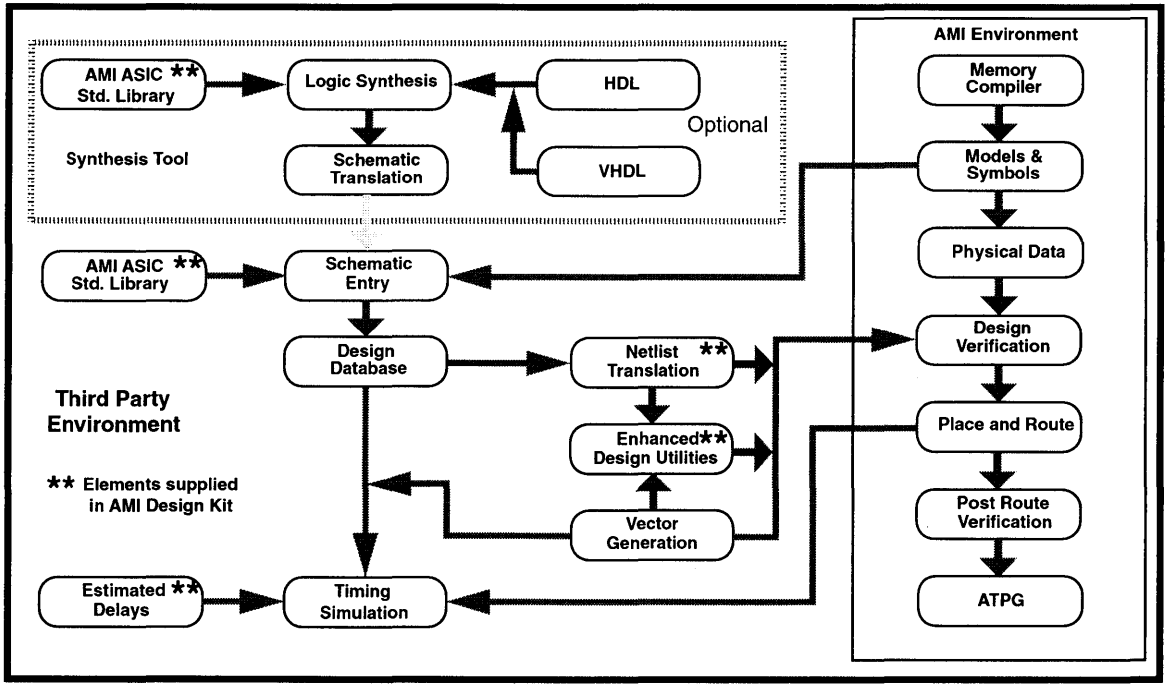
After layout has been completed the interconnect data is extracted from the physical layout to be fed back to the sign-off simulator for final circuit verification. This post layout interconnect data can be sent to the customer for final validation on his simulator. When the post-layout simulation has been completed and approved by the customer the design is then released for mask and wafer fabrication.

The test program is developed in parallel using internal automatic test program generation software. Prototypes can then be tested before they are shipped.

Figure 3 outlines a typical software environment when using third party tools. AMI uses EDIF to speed ports between various software products.

AMI's EDU's tools are intended to be used interactively at each stage of the design. EDU software is a set of design analysis tools that check both the design and test vectors for correctness and compatibility with in-house ASIC testers, and analyze the design for inefficiencies and possible flaws that could cause problems in manufacturing the device.

FIGURE 3: DESIGN ENVIRONMENT WITH THIRD PARTY SOFTWARE



Memory Compiler Library

Memory Compiler	Size min.	Size max.	Increment	Comments
SRAM (single-port, synchronous)	32 x 1	1K x 32	16-words, 1-bit	9 ns typical access time on 1K x 16

Note: Other SRAM and ROM compilers are available for standard cell or embedded array design approaches. Contact an AMI Design Center for details about these other product offerings.

The Design Library

AMI provides a robust collection of building blocks for the AMI8Gx gate array family. A broad range of primary cells is complemented with memory cell compilers and useful megacells. With such broad, US-based design talent, AMI can quickly design specific cells that customers need to add an edge in customization.

The AMI ASIC Standard Library

The AMI ASIC Standard Library contains a rich set of core and pad cells which allow great flexibility in building competitive devices for customer applications. The library is portable across all AMI's gate array and standard cell families.

Soft Datapath Library (xx by yy)

Name	Function
MGAxxyyDv	Adder
MGAxxyyEv	Adder/Subtracter
MGBxxyyAv	Arithmetic/Barrel shifter
MGBxxBv	Barrel shifter
MGBxxCv	Arithmetic shifter
MGCxxAv	2-Function binary comparator
MGCxxBv	6-Function binary comparator
MGDxxAv	Decrementer
MGIxxAv	Incrementer
MGIxxBv	Incrementer/Decrementer
MGMxxyyDv	Signed/unsigned multiplier
MGMxxyyEv	Multiplier/Accumulator
MGSxxyyAv	Signed/unsigned subtracter

Memory Compilers

The AMI8Gx family offers the memory compiler shown above. Each of the thousands of possible memory blocks created by this compiler is optimized precisely to the customers' parameters rather than built from a presized leaf cell that covers a range of sizes. This yields a better size and performance match for each application.

Upon supplying the cell specification to AMI, the customer can receive an accurate simulation timing specification overnight by facsimile and a full simulation model for any AMI supported software environment within five working days.

FIFOs, Registers, Stacks, and Datapath Megacells

These megacells are produced using parameterized synthesizers. This allows the creation of various sizes and speeds. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two.

These synthesizers produce soft megacell schematics in the ASIC Standard Library and are available on various workstations. The data sheets contain a functional description, a pin description, and sample equivalent gate counts with sample delays.

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FIFOs, Registers, and Stacks (xx by yy)

Name	Function
MGFxxyyC1	Fall-through FIFO
MGFxxyyDv	Asynchronous FIFO, dynamic flags
MGFxxyyEv	Asynchronous FIFO, static flags
MGFxxyyFv	Synchronous FIFO, dynamic flags
MGFxxyyGv	Synchronous FIFO, static flags
MGFxxyyHv	Async. RAM based FIFO, dynamic flags
MGFxxyylv	Async. RAM based FIFO, static flags
MGRxxyyAv	Asynchronous single-port register file
MGRxxyyBv	Sync. single-port latch-based register file
MGRxxyyCv	Sync. single-port flip-flop based register file
MGRxxyyDv	Asynchronous dual-port register file
MGRxxyyEv	Sync. dual-port register file, latch-based
MGRxxyyFv	Sync. dual-port register file, flip-flop based
MGTxxyyAv	Synchronous stack

Megacells

The AMI8Gx gate array family supports soft megacell versions that are compatible with many popular architectures. These products are listed above.

Soft megacells are functionally and logically compatible with the stand alone products, but since the function is captured in a gate array, each instance of the megacell will differ slightly depending on its physical placement on the array. Soft megacells become part of the design netlist, requiring backannotation of interconnect capacitance after place-and-route for final verification.

AMI supplies an actual gate level netlist and schematic of the soft megacell allowing the user to make design changes or remove unneeded features. Test vectors are provided and can be used directly or incorporated into the overall design test. All soft megacells are static designs and use AMI's ASIC Standard Library to ensure portability.

Soft Megacell Library

Name	Function
MG1468C18	Real-time clock
MG29C01	4-Bit microprocessor slice
MG29C10	Microprogram controller/sequencer
MG65C02	8-Bit microprocessor
MG80C85	8-Bit microprocessor
MG82C37A	Programmable DMA controller
MG82C50A	Asynchronous comm. element
MG82C54	Programmable interval timer
MG82C55A	Programmable peripheral interface
MG82C59A	Programmable interrupt controller
MGMC51	8-Bit microcontroller, 8051FB compatible
MGMC51FB	8-Bit microcontroller, 8051 compatible
MGMC51SD	Reduced function MGMC51

DC Specifications

Operating Specifications

Parameter		Minimum	Maximum	Units
V_{DD}, Supply voltage		2.7	5.5	Volts
Ambient temperature	- Military	-55	125	°C
	- Commercial	0	70	°C
CMOS Input Specifications ($4.5V < V_{DD} < 5.5V$; $0°C < T < 70°C$)				
Vil	Low level input voltage		$0.3*V_{DD}$	Volts
Vih	High level input voltage	$0.7*V_{DD}$		Volts
Iil	Low level input current		-1.0	µA
Iih	High level input current		1.0	µA
Iil	Input pull-up current	-30	-140	µA
Iih	Input pull-down current	30	185	µA
Vt-	Schmitt negative threshold	$0.2*V_{DD}$		Volts
Vt+	Schmitt positive threshold		$0.8*V_{DD}$	Volts
Vh	Schmitt hysteresis	1.0		Volts
TTL Input Specifications ($4.5V < V_{DD} < 5.5V$; $0°C < T < 70°C$)				
Vil	Low level input voltage		0.8	Volts
Vih	High level input voltage	2.0		Volts
Iil	Low level input current		-1.0	µA
Iih	High level input current		1.0	µA
Iil	Input pull-up current	-30	-140	µA
Iih	Input pull-down current	30	185	µA
Vt-	Schmitt negative threshold	0.7		Volts
Vt+	Schmitt positive threshold		2.1	Volts
Vh	Schmitt hysteresis	0.4		Volts

AMI8S 0.8 micron CMOS Gate Array

Output Operating Specifications ($4.5V < V_{DD} < 5.5V; 0°C < T < 70°C$)

Parameter		Minimum	Maximum	Units
1.0 mA Driver				
Vol	Low level output voltage		0.4	Volts
Voh	High level output voltage	2.4		Volts
Iol	Low level output current		1.0	mA
Ioh	High level output current		-1.0	mA
2.0 mA Driver				
Vol	Low level output voltage		0.4	Volts
Voh	High level output voltage	2.4		Volts
Iol	Low level output current		2.0	mA
Ioh	High level output current		-2.0	mA
4.0 mA Driver				
Vol	Low level output voltage		0.4	Volts
Voh	High level output voltage	2.4		Volts
Iol	Low level output current		4.0	mA
Ioh	High level output current		-4.0	mA
8.0 mA Driver				
Vol	Low level output voltage		0.4	Volts
Voh	High level output voltage	2.4		Volts
Iol	Low level output current		8.0	mA
Ioh	High level output current		-8.0	mA
16.0 mA Driver				
Vol	Low level output voltage		0.4	Volts
Voh	High level output voltage	2.4		Volts
Iol	Low level output current		16.0	mA
Ioh	High level output current		-16.0	mA

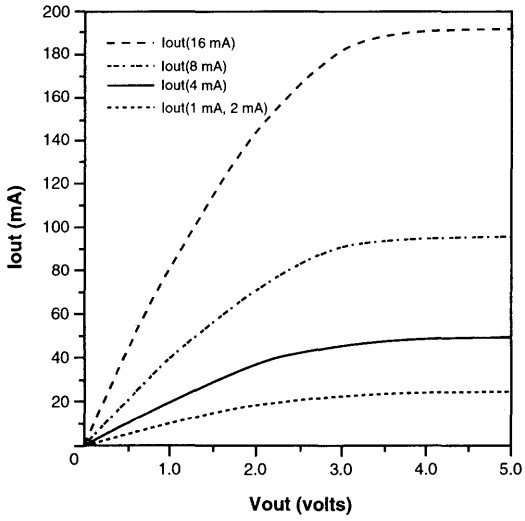
Absolute Maximum Ratings

Parameter		Minimum	Maximum	Units
V_{DD}, Supply voltage		-0.3	6.0	Volts
Input pin voltage		-0.3	V_{DD}+0.3	Volts
Input pin current		-10.0	10.0	mA
Storage temperature	- Plastic packages	-55	125	°C
	- Ceramic packages	-65	150	°C
Lead temperature			300	°C for 10 sec.

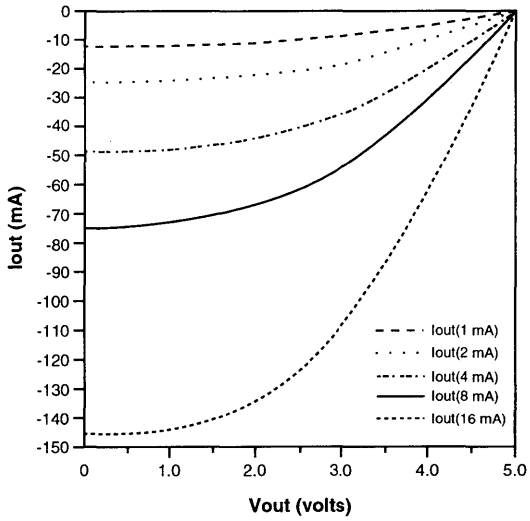
Note that these specifications are to indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Further, operation at absolute maximum conditions for extended periods may adversely affect the long term reliability of the device.

DC Characteristics
(V_{DD} = 5.0V, T = 25°C, Typical Process)

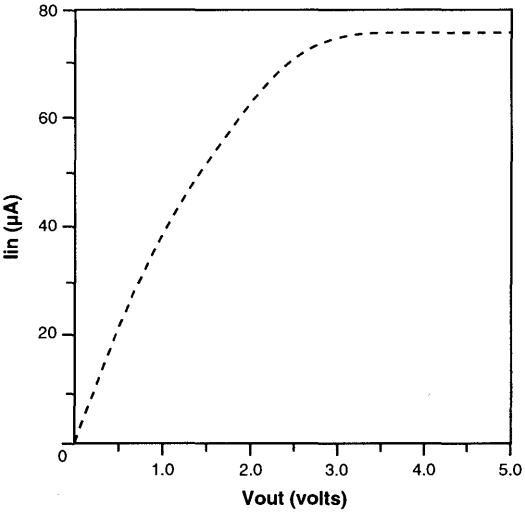
N-Channel Output Driver



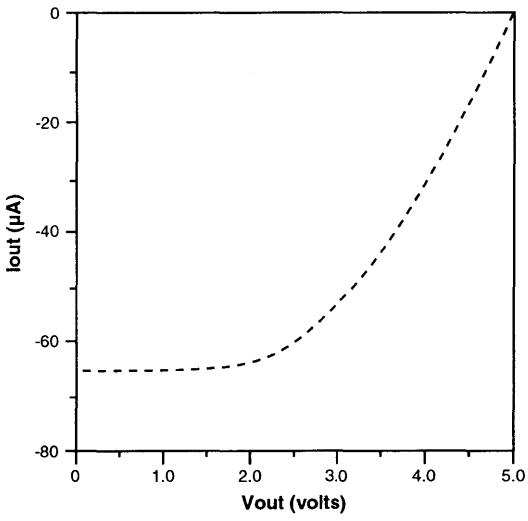
P-Channel Output Driver



N-Channel Pull-Down Device



P-Channel Pull-Up Device



AMI8S 0.8 micron CMOS Gate Array

DC Derating Information

The DC Characteristics on page 2-9 can be derated to obtain values at other operating conditions using the formula:

$$I_{DC} * K_{PDC} * K_{VDC} * K_{TDC}$$

where I_{DC} is a value from the current curves on page 9. K_{PDC}, the DC process derating coefficient; K_{VDC}, the DC voltage derating coefficient; and K_{TDC}, the DC temperature derating coefficient, are described below. Due to the ESD protection structures, the N-channel driver has a different set of coefficients for K_{PDC} and K_{TDC}.

DC Variations with process (K_{PDC})

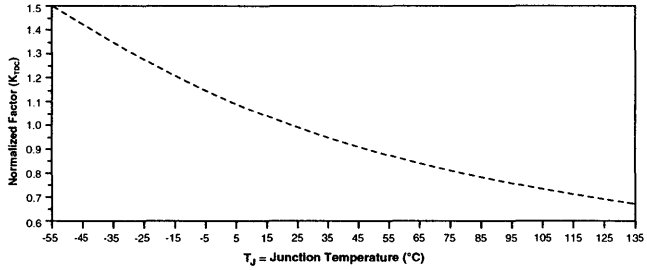
DC variations with process are given as fixed constants determined at the limits of acceptable manufacturing of the process. These are described below where WCS is the "Worst Case Speed" fabrication, TYP is the "Target" fabrication, and WCP is the "Worst Case Power" fabrication.

	N-Channel Output Driver (Vol = 0.4V)			N-Channel Pull-Down Device (Vol = 0.4V)			All P-Channel (Voh = 2.4V)		
Process	WCS	TYP	WCP	WCS	TYP	WCP	WCS	TYP	WCP
K_{PDC}	0.61	1.00	1.47	0.71	1.00	1.27	0.68	1.00	1.45

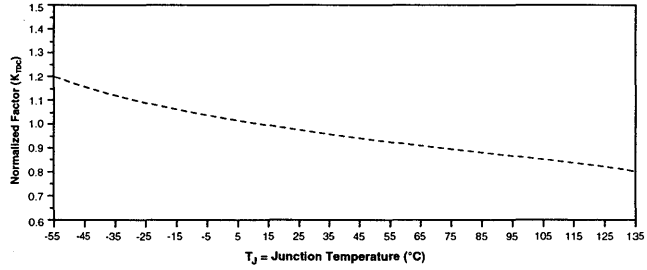
DC Variations with Voltage (K_{VDC})

	All N-Channel (Vol = 0.4V)			All P-Channel (Voh = 2.4V)		
V_{DD}	4.5	5.0	5.5	4.5	5.0	5.5
K_{VDC}	0.97	1.00	1.03	0.79	1.00	1.21

DC variations with temperature for the N-Channel output driver (K_{TDC})



DC variations with temperature for all other N-Channel and P-Channel devices



Delay Derating Information

The propagation delays listed in the data sheets are for typical temperature, 25°C; typical supply voltage, 5.0V; and typical processing conditions. To calculate the delay at other conditions (including V_{DD} equals 3.0V) the following equation can be used:

$$T_{pdx} = T_{pdx}(typ) * K_P * K_V * K_T$$

where $T_{pdx}(typ)$ is given in the data sheets. K_P, the process derating coefficient; K_T, the temperature derating coefficient; and K_V, the supply voltage derating coefficient, are described below.

Delay Variations with Temperature (K_T)

Delay varies linearly with temperature. The following formulas and common operating points can be used.

Temp	K_T
-55°C	0.79
-25°C	0.87
0°C	0.94
25°C	1.00
70°C	1.11
100°C	1.19
125°C	1.26

Temp. Range	K_T Formula
-55°C to 25°C	$K_T = 1.0 - (25 - T_J°C) * 2.58 \times 10^{-3}$
25°C to 140°C	$K_T = 1.0 + (T_J°C - 25) * 2.58 \times 10^{-3}$

Where T_J°C is the temperature at the silicon junction.

Delay Variations with Process (K_P)

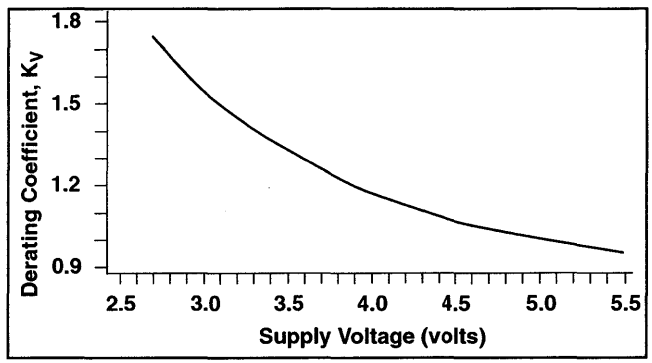
Delay variations with process are given as fixed constants determined at the limits of acceptable manufacturing of the process. These are described below.

Derating Coefficient (K_P)	Process Variation Point
1.40	Delay increase due to "Worst Case Speed" (WCS) fabrication
1.00	Typical delay; Fabrication target
0.61	Delay reduction due to "Worst Case Power" (WCP) fabrication

Delay Variations with Voltage (K_V)

Delay varies nonlinearly with voltage. Some common operating points and a characteristic curve are shown.

V_{DD}	K_V
2.7V	1.74
3.0V	1.54
3.3V	1.39
4.5V	1.07
4.75V	1.03
5.0V	1.00
5.25V	0.97
5.5V	0.94



AMI8S 0.8 micron CMOS Gate Array

Interpreting the Data Sheet

The figure below shows a typical data sheet and points out the main features of the data sheet. Not shown is a schematic which accompanies some of the more complex cells.

Cell Name →

AMI SEMICONDUCTORS

American Microsystems, Inc.

AA21

Library Type → **AMI8G 0.8 micron CMOS Gate Array**

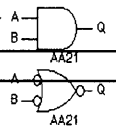
Description →

Description:

AA21 is a 2-input gate which performs the logical AND function.

Logic Symbol	Truth Table	Pin Loading

Logic Symbol →



Truth Table →

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading →

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates → **Equivalent Gates:**.....2.0

Bolt Syntax → **Bolt Syntax:**.....Q .AA21 A B;

Power Characteristics → **Power Characteristics:**

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	5.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics → **Delay Characteristics:**

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.42	0.59	0.80	1.01	1.22
		t_{PHL}	0.39	0.51	0.65	0.77	0.90

See page 2-15 for interconnect estimates.

A description of these features of the data sheet are as follows.

LIBRARY TYPE: Designates the feature size and library type such as standard cell or gate array.

CELL NAME: AMI's cell name.

DESCRIPTION: A brief sentence about the function of the cell.

LOGIC SYMBOL: Shows a picture of the symbol as it appears as an icon in the workstation design kits.

TRUTH TABLE: A boolean table showing the output logic levels as a function of the input logic levels.

Types of logic levels found in the logic tables are as follows:

H	=	High level steady state,
L	=	Low level steady state,
↑	=	Transition from low level to high level,
↓	=	Transition from high level to low level,
X	=	Any level including transitions,
NC	=	No change in output level for a given set of input levels,
IL	=	The output level is unknown for this set of illegal input levels,
Z	=	High impedance level,
UN	=	Undriven node or input,
Q(n)	=	The level of Q before an active transition on the affecting node, and
QN(n)	=	The level of QN before an active transition on the affecting node.

PIN LOADING: A table of cell input loads in units of equivalent loads (the input load normalized to the input load of an NA21, 2-input NAND gate).

EQUIVALENT GATES: Equivalent gates for the cell is defined as the cell area normalized to the area of the NA21.

BOLT SYNTAX: BOLT (Block Oriented Logic Translator) is an AMI proprietary netlist format. This line shows the BOLT syntax for the cell. One example of the use of BOLT is as a design interface from the workstation design kits to AMI.

POWER CHARACTERISTICS: Power for the cell can be described in three parts. The first part is the power dissipated due to the leakage current across the channels and through the formed diodes. The second part is due to the switching voltage across loads on the internal nodes of the cell. Finally, the third part is due to the switching voltage across a load that a cell is driving.

The power characteristics table provides the static leakage current for a junction temperature of 85°C, and the dissipative load for all the switching nodes in the cell in terms of equivalent loads.The load that a cell drives can be calculated by adding up input loads and adding to it the estimated load from the Load Estimation table on page 2-15. Below are equations for calculating the power dissipation.

Core Cells and Input Buffers

$$\text{POWER} = (\text{Static } I_{DD})\ V_{DD} + 0.05EQL_{pd}V_{DD}^2f + 0.05EQL_IV_{DD}^2f$$

Output Buffers

$$\text{POWER} = (\text{Static } I_{DD})\ V_{DD} + 0.05EQL_{pd}V_{DD}^2f + C_{ol}V_{DD}^2f$$

where:

Static I_{DD}	= static leakage current of the cell
V_{DD}	= operating voltage
EQL_{pd}	= load of the switching nodes in the cell
f	= frequency of operation
C_{ol}	= load in farads on the output buffer
EQL_I	= load of the driven pins and interconnect

The frequency term of the power equation dominates, making the static current term insignificant. However, the term can be used to find the standby current.

AMI8G 0.8 micron CMOS Gate Array

DELAY CHARACTERISTICS: This table contains delay data for the various input to output paths in the cells. The table below explains each column in the delay characteristics. The traditional coefficients for a linear model have not been provided because AMI is now using a new equation to model the effects of loading on the input as well as on the output of a cell's path delay. The delay on the data sheets represents a typical load on the inputs of the cell. More accurate timing can be obtained using one of AMI's workstation kits. Contact your sales representative or the factory for details.

Explanation of Columns in the Delay Characteristics Table

Column Name	Explanation	
Delay (ns) From To	Names the two pins that identify the path for the delay	
Parameter	Mnemonic for the propagation delay or timing parameter whose value can be obtained from the values listed under the number of equivalent loads column.	
	t_{PLH}	Input to output propagation delay for a rising edge on the output
	t_{PHL}	Input to output propagation delay for a falling edge on the output
	t_{ZH}	High impedance to high level delay
	t_{ZL}	High impedance to low level delay
	t_{HZ}	High level to high impedance delay
	t_{LZ}	Low level to high impedance delay
	t_{su}	Input setup time with respect to clock
	t_h	Input hold time
	t_w	Input pulse width
Number of Equivalent Loads	The first row of values in this column contains five equivalent loads over the range of allowed loading for the cell (output buffer loading is in pico farads). The last value in the row on the right has the word "max" in parenthesis to indicate that this is the maximum load that the cell can drive[1]. The rest of the rows contain delay values for each of the parameters corresponding to given loads in the first row. To find the delay for a cell, add up the loads of all the inputs that the cell is driving, then add the estimated interconnect load from the Load Estimation table on page 2-15. Finally, look up the value for the desired parameter corresponding to the load on the cell. Interpolation may be used for values in between load columns. Again, more accurate delays can be achieved by obtaining an AMI workstation kit.	

Notes: 1. Due to differing capabilities of logic simulators, the delay modeling implementation will vary and in some cases will still use the linear model. Consult the factory about modeling for some specific workstation kits and simulators. Loads beyond the maximum load are an extrapolation of the model and therefore their accuracy is not guaranteed.

Interconnect Load Estimation Table

Die Size	Fan Out (Equivalent Loads)							
	1	3	6	9	12	20	50	80
500	0.3	0.9	2.0	3.2	4.5	8.1	23.4	40.3
450	0.2	0.9	1.9	3.1	4.3	7.8	22.4	38.7
400	0.2	0.8	1.8	2.9	4.1	7.4	21.4	36.8
350	0.2	0.8	1.7	2.8	3.9	7.0	20.3	34.9
300	0.2	0.7	1.6	2.6	3.7	6.6	19.0	32.8
250	0.2	0.7	1.5	2.4	3.4	6.1	17.7	30.5
200	0.2	0.6	1.4	2.2	3.1	5.6	16.1	27.8
150	0.2	0.6	1.2	2.0	2.8	5.0	14.3	24.8
100	0.1	0.5	1.0	1.7	2.3	4.2	12.2	21.0

AMI8S 0.8 micron CMOS Gate Array

Packaging

The AMI8Gx gate array family can be packaged in a variety of popular packages.

New packages are in development which will extend the package offering. Some special packages or packaging requirements can be supplied if requested. More details on specific packages are available from an AMI sales representative.

Available Packages

( ) = Lead time required

Array	PQFP	TQFP	CQFP	PLCC	JLDCC	CLCC
G5	44,52,64,80	(48),64	40	20,28,68	28	20,24,28,44
G9	44,52,64,80,100,120	64,100,(144)	40	20,28,44,68	28	24,28,44
G15	44,52,64,80,100,120	64,(80),100,(128),(144)	40	20,28,44,68,84	28,44,68,84	24,28,36,40,44,48,52
G21	44,52,64,80,100,120,128	64,(80),100,(128),(144)	40	20,28,44,68,84	44,68,84	28,36,40,44,48,52,84
G34	44,52,64,80,100,120,128,144	64,(80),100,(128),(144)	40,44,132	28,44,68,84	44,68,84	28,36,40,44,48,52,68,84
G44	44,52,64,80,100,120,128,144,160	(80),100,(128),(144)	40,44,132	28,44,68,84	44,68,84	36,40,44,48,52,68,84
G55	44,52,64,80,100,120,128,144,160	(80),100,(128),(144)	44,132	28,44,68,84	(44),68,(84)	44,48,68,84
G65	44,52,64,80,100,120,128,144,160	(80),100,(144),(176)	44,132	44,68,84	(44),68,84	44,48,68,84
G93	64,80,100,120,128,144,160,208	100,(144),(176)	132,144	44,68,84	68,84	68,84
G142	100,120,128,144,160,208	(176)	132,144	68,84	68,84	68
G201	144,160,208			(84)	84	
G247	144,160,208,256[2]					
G392	208,304[1,2]					
G663						

Notes 1: The 304 pin PowerQuad2™ package has a heat slug added to improve power dissipation.

2: The 256 and 304 pin packages are supplied in a TapePak® molded carrier ring.

Array	MQUAD®	PDIP	PPGA	CPGA	BGA
G5		8,14,16,18,20,22,24,28,40,48		68	
G9		22,24,28,40,48		68	
G15		22,24,28,40,48		(65),68,69,(85),121,145	
G21		22,24,28,40,48		(65),68,69,(85),121,145	
G34	144	24,28,40,48	69,85,101,109,121,145	(65),68,69,85,101,121,145	(169)
G44	144	24,28,40,48	69,85,101,109,121,145	68,69,85,101,121,145	(169)
G55	128,144	28,40,48	69,85,101,109,121,145	68,69,85,101,121,145	(169)
G65	128,144	28,40	69,85,101,109,121,132,145	68,69,85,101,(145)	(169)
G93	128,144,(160)	(40)	69,101,109,121,132,145	68,84,85,109,121,132,(145),208	(169),(225)
G142	128,(144),(160),(208)		69,121,132,145,180	68,84,109,121,132,145,177,181,208	(169),(225),(313)
G201	(144),(160),(208)		145,180	145	(169),(225),(313)
G247	(144),(160),(208)		180	145	(169),(225),(313)
G392	(144),(160),(208)			476	(225),(313)
G663					(313)

PQFP = Plastic quad flatpack
TQFP = Thin quad flatpack (plastic)
MQUAD = Metal quad flatpack
CQFP = Ceramic qual flatpack
PLCC = Plastic leaded chip carrier - J lead
JLDCC = Ceramic leaded chip carrier - J lead
CLCC = Leadless chip carrier (ceramic)
PDIP = Plastic dual in-line package
PPGA = Plastic pin grid array
CPGA = Ceramic pin grid array
BGA = Ball grid array

SECTION 3
CORE LOGIC

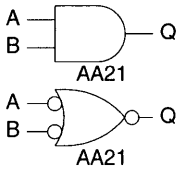
AA21

AMI8G 0.8 micron CMOS Gate Array

Description:

AA21 is a 2-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .AA21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	5.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.42	0.59	0.80	1.01	1.22
		t_{PHL}	0.39	0.51	0.65	0.77	0.90

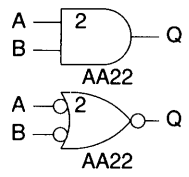
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

AA22 is a 2-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .AA22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	6.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

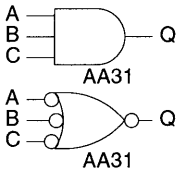
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.46 0.41	0.64 0.56	0.82 0.68	1.00 0.80	1.18 0.91

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

AA31 is a 3-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .AA31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	6.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.64	0.82	1.04	1.25	1.46
		t_{PHL}	0.46	0.60	0.74	0.88	1.00

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AA32

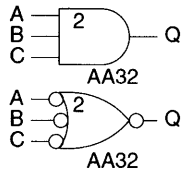
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

AA32 is a 3-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .AA32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	9.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

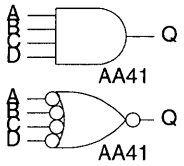
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.72 0.50	0.91 0.65	1.11 0.79	1.30 0.91	1.48 1.03

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

AA41 is a 4-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .AA41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	8.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.88 0.52	1.08 0.66	1.31 0.82	1.52 0.95	1.73 1.09

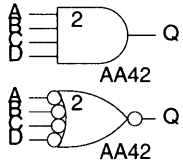
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

AA42 is a 4-input gate which performs the logical AND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .AA42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	9.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

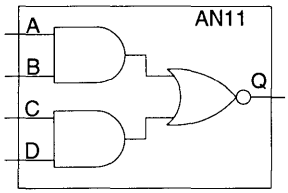
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	0.95	1.18	1.39	1.58	1.77
		t_{PHL}	0.53	0.70	0.85	0.97	1.09

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

AN11 is an AND-NOR circuit consisting of two 2-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H
H	H	X	X	L
X	X	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....2.0

Bolt Syntax: .....Q .AN11 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	5.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.60 0.33	0.79 0.44	0.99 0.54	1.18 0.65	1.37 0.75

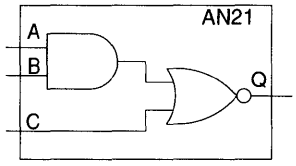
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

AN21 is an AND-NOR circuit consisting of one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	Q
H	H	X	L
X	X	H	L
All other combinations			H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.6

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .AN21 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	5.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

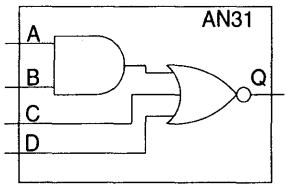
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH}	0.40	0.55	0.70	0.85	1.00
		t_{PHL}	0.24	0.31	0.38	0.44	0.51

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

AN31 is an AND-NOR circuit consisting of a 2-input AND gate and two direct inputs into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	L	L	H
X	L	L	L	H
H	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .AN31 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.1	nA
EQL_{pd}	6.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	5	7 (max)
Any Input	Q	t_{PLH}	0.87	1.02	1.31	1.45	1.74
		t_{PHL}	0.26	0.31	0.41	0.46	0.56

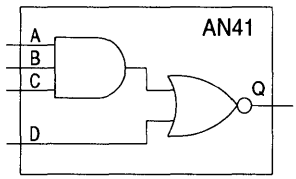
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

AN41 is an AND-NOR circuit consisting of one 3-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	Q
H	H	H	X	L
X	X	X	H	L
All other combinations				H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.6
D	1.6

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .AN41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	8.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.40 0.33	0.45 0.36	0.55 0.43	0.60 0.46	0.70 0.52

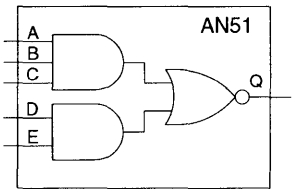
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

AN51 is an AND-NOR circuit consisting of one 3-input AND gate and one 2-input AND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	H	L
All other combinations					H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:.....4.0

Bolt Syntax:.....Q .AN51 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	12.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.67 0.62	0.84 0.74	1.04 0.88	1.25 1.01	1.45 1.13

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AN61

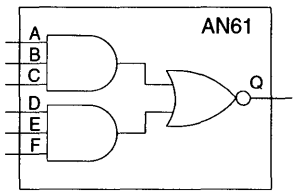
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

AN61 is an AND-NOR circuit consisting of two 3-input AND gates into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:.....5.0

Bolt Syntax:.....Q .AN61 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.8	nA
EQL_{pd}	15.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

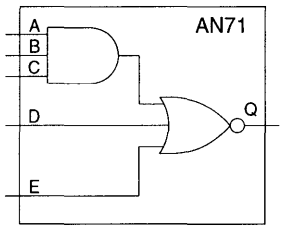
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	0.78	0.95	1.13	1.31	1.49
		t_{PHL}	0.74	0.87	0.99	1.11	1.22

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

AN71 is an AND-NOR circuit consisting of one 3-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
All other combinations					H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.6
D	1.6
E	1.6

Equivalent Gates:.....4.0

Bolt Syntax:.....Q .AN71 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	11.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	5	7 (max)
Any Input	Q	t_{PLH}	0.67	0.75	0.89	0.97	1.11
		t_{PHL}	0.38	0.42	0.49	0.52	0.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AN81

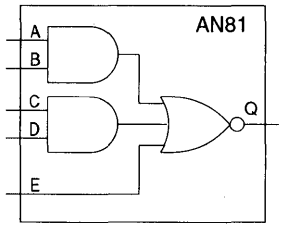
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

AN81 is an AND-NOR circuit consisting of two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
H	H	X	X	X	L
X	X	H	H	X	L
X	X	X	X	H	L
All other combinations					H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:.....5.0

Bolt Syntax:.....Q .AN81 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.8	nA
EQL_{pd}	15.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

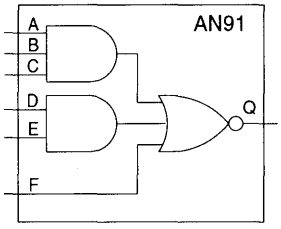
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	0.85	1.04	1.23	1.42	1.60
		t_{PHL}	0.64	0.79	0.92	1.04	1.15

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

AN91 is an AND-NOR circuit consisting of one 3-input AND gate and one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	H	X	X	X	L
X	X	X	H	H	X	L
X	X	X	X	X	H	L
All other combinations						H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:.....5.0

Bolt Syntax:.....Q .AN91 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.8	nA
EQL_{pd}	15.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.78	0.96	1.17	1.38	1.59
		t_{PHL}	0.56	0.69	0.83	0.96	1.08

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ANA1

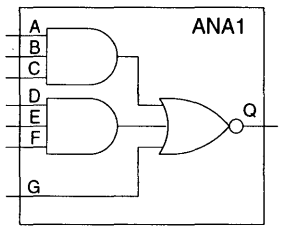
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ANA1 is an AND-NOR circuit consisting of two 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	H	X	L
X	X	X	X	X	X	H	L
All other combinations							H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q .ANA1 A B C D E F G;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	19.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

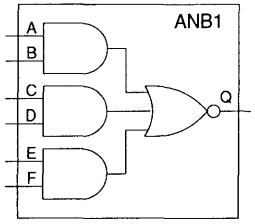
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	0.86	1.06	1.25	1.43	1.61
		t_{PHL}	0.80	0.95	1.08	1.19	1.30

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

ANB1 is an AND-NOR circuit consisting of three 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
H	H	X	X	X	X	L
X	X	H	H	X	X	L
X	X	X	X	H	H	L
All other combinations						H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:.....5.0

Bolt Syntax:.....Q .ANB1 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.8	nA
EQL_{pd}	16.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.85	1.03	1.24	1.45	1.66
		t_{PHL}	0.70	0.83	0.98	1.11	1.24

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ANC1

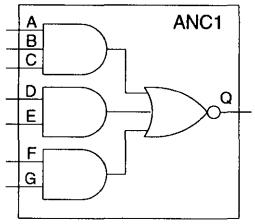
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ANC1 is an AND-NOR circuit consisting of one 3-input AND gate and two 2-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
H	H	H	X	X	X	X	L
X	X	X	H	H	X	X	L
X	X	X	X	X	H	H	L
All other combinations							H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q .ANC1 A B C D E F G;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	19.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

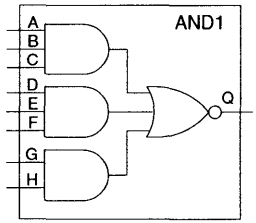
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	0.87	1.06	1.26	1.44	1.62
		t_{PHL}	0.64	0.78	0.91	1.03	1.14

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

AND1 is an AND-NOR circuit consisting of two 3-input AND gates and one 2-input AND gate into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
H	H	H	X	X	X	X	X	L
X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	H	H	L
All other combinations								H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0
H	1.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q .AND1 A B C D E F G H;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	20.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.86	1.04	1.26	1.46	1.67
		t_{PHL}	0.82	0.95	1.09	1.22	1.35

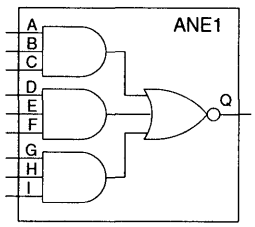
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

ANE1 is an AND-NOR circuit consisting of three 3-input AND gates into a 3-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
H	H	H	X	X	X	X	X	X	L
X	X	X	H	H	H	X	X	X	L
X	X	X	X	X	X	H	H	H	L
All other combinations									H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0
H	1.0
I	1.0

Equivalent Gates:.....7.0

Bolt Syntax:.....Q .ANE1 A B C D E F G H I;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	12.4	nA
EQL_{pd}	22.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

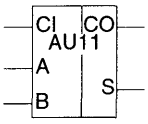
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	0.96	1.15	1.35	1.53	1.71
		t_{PHL}	0.81	0.94	1.07	1.19	1.30

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

AU11 is a combinational one-bit full adder.

Logic Symbol



Truth Table

CI	A	B	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Pin Loading

	Equivalent Load
A	4.1
B	4.1
CI	3.1

Equivalent Gates:.....7.0

Bolt Syntax:.....CO S .AU11 A B CI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	23.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

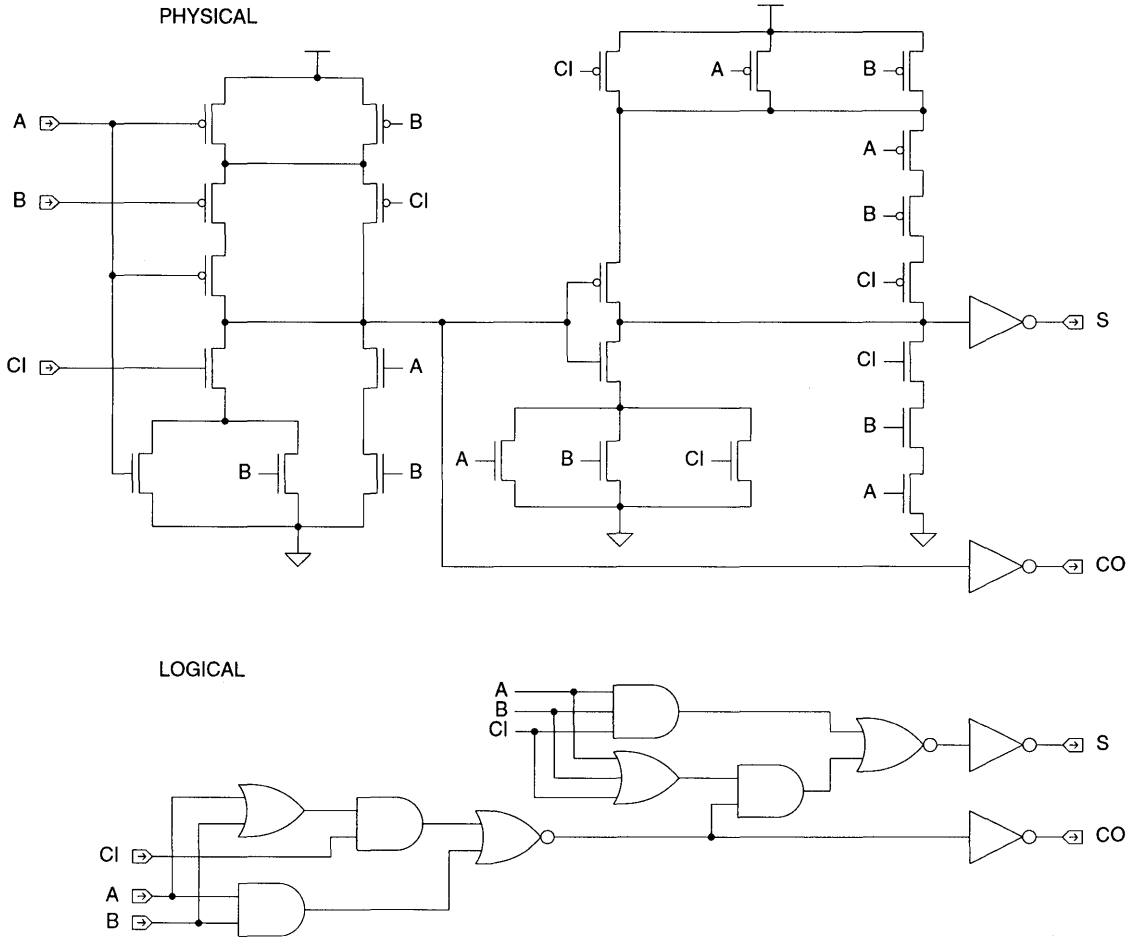
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
A	S	t_{PLH} t_{PHL}	1.42 1.03	1.59 1.22	1.81 1.41	2.01 1.57	2.22 1.72
B	S	t_{PLH} t_{PHL}	1.43 1.10	1.64 1.26	1.82 1.42	2.03 1.57	2.24 1.71
CI	S	t_{PLH} t_{PHL}	1.21 1.08	1.40 1.24	1.60 1.41	1.81 1.56	2.02 1.69
A	CO	t_{PLH} t_{PHL}	0.70 0.95	0.88 1.14	1.10 1.34	1.31 1.51	1.52 1.67
B	CO	t_{PLH} t_{PHL}	0.69 0.97	0.87 1.16	1.09 1.36	1.30 1.53	1.51 1.69
CI	CO	t_{PLH} t_{PHL}	0.62 0.69	0.79 0.86	1.01 1.05	1.22 1.22	1.43 1.38

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

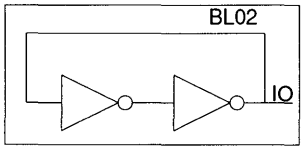
Logic Schematic



Description:

BL02 is a tri-state bus latch that stores the final binary level on the bus when left undriven.

Logic Symbol



Truth Table

N/A

Pin Loading

	Equivalent Load
IO	2.5

Equivalent Gates:.....4.0

Bolt Syntax:.....IO .BL02;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	14.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Equivalent Load 1
IO	IO	t_{PLH} t_{PHL}	0.34 0.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

CVDD

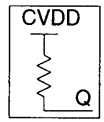
AMI8G 0.8 micron CMOS Gate Array

Description:

CVDD is the resistive tie-up to the core V_{DD} bus for all cell inputs.

Equivalent Gates:.....1.0

Bolt Syntax:.....Q .CVDD;

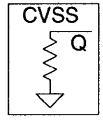


Description:

CVSS is the resistive tie-down to the core V_{SS} bus for all cell inputs.

Equivalent Gates:.....1.0

Bolt Syntax:.....Q .CVSS;



DC24

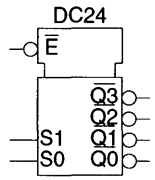
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DC24 is a two-to-four line decoder/demultiplexer with active low enable.

Logic Symbol



Truth Table

EN	S1	S0	Q0N	Q1N	Q2N	Q3N
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Pin Loading

	Equivalent Load
S0	3.1
S1	3.1
EN	1.0

Equivalent Gates:.....8.0

Bolt Syntax:.....Q0N Q1N Q2N Q3N .DC24 EN S0 S1;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	13.3	nA
EQL_{pd}	27.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

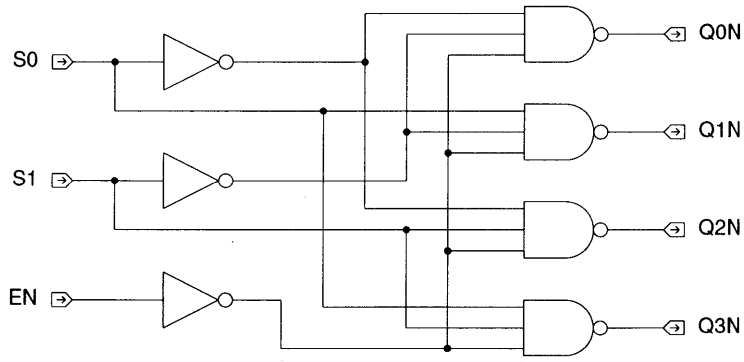
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	5	7 (max)
Sx	QN	t_{PLH}	0.43	0.49	0.59	0.64	0.75
		t_{PHL}	0.56	0.63	0.78	0.85	0.99
EN	QN	t_{PLH}	0.59	0.64	0.75	0.80	0.91
		t_{PHL}	0.71	0.79	0.94	1.01	1.15

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

Logic Schematic



DC38

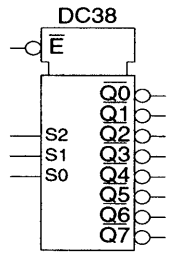
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DC38 is a three-to-eight line decoder/demultiplexer with active low enable.

Logic Symbol



Truth Table

Truth Table Appears On Next Page

Pin Loading

	Equivalent Load
S0	5.5
S1	5.2
S2	5.1
EN	1.0

Equivalent Gates:.....20.0

Bolt Syntax:.....Q0N Q1N Q2N Q3N Q4N Q5N Q6N Q7N .DC38 EN S0 S1 S2;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	31.8	nA
EQL_{pd}	58.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	3	5	6 (max)
Sx	QN	t_{PLH} t_{PHL}	0.61 0.86	0.66 0.95	0.72 1.04	0.82 1.22	0.87 1.31
EN	QN	t_{PLH} t_{PHL}	0.85 1.10	0.91 1.19	0.97 1.28	1.08 1.46	1.13 1.55

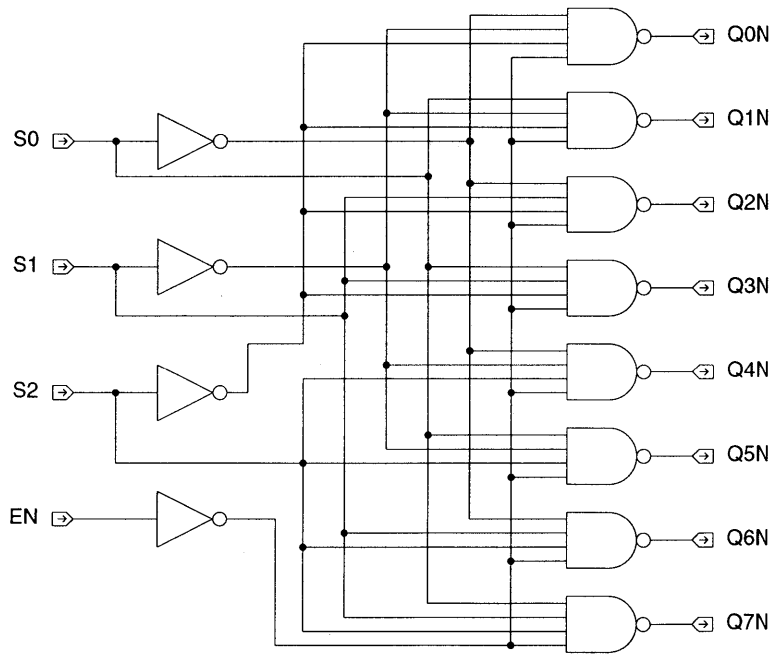
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

Truth Table

EN	S2	S1	S0	Q0N	Q1N	Q2N	Q3N	Q4N	Q5N	Q6N	Q7N
H	X	X	X	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L

Logic Schematic



DF081

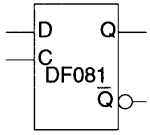
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF081 is a static, master-slave, D flip-flop without SET or RESET. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
H	↑	H	L
L	↑	L	H
X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1

Equivalent Gates:.....6.0

Bolt Syntax:.....Q QN .DF081 C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.2	nA
EQL_{pd}	21.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

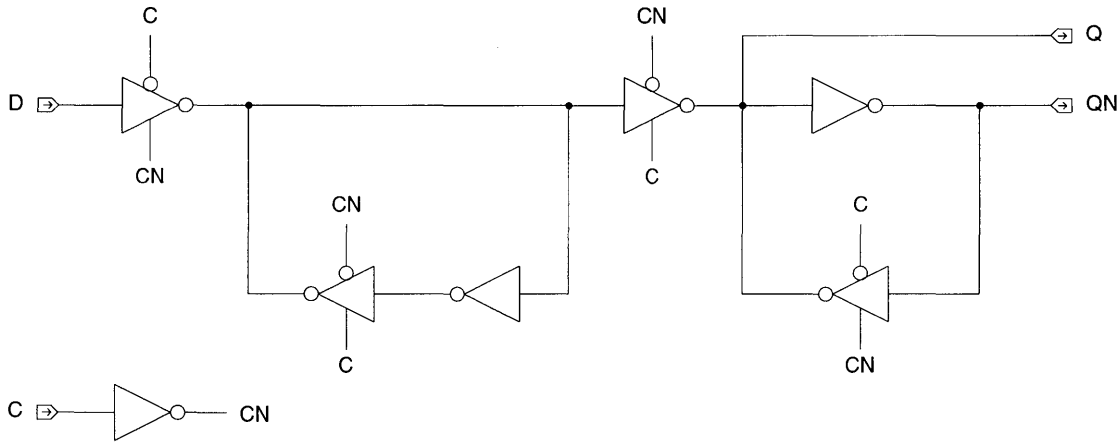
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.69 0.28	0.87 0.39	1.06 0.49	1.25 0.59	1.43 0.69
C	QN	t_{PLH} t_{PHL}	0.53 0.81	0.65 0.90	0.76 0.99	0.86 1.07	0.96 1.14
Min C Width	High	t_w	0.85				
Min C Width	Low	t_w	0.85				
Min D Setup		t_{su}	0.78				
Min D Hold		t_h	0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

(continued on next page)

Logic Schematic



DF091

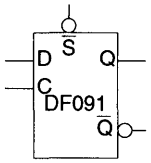
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF091 is a static, master-slave, D flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2
SN	2.0

Equivalent Gates:.....7.0

Bolt Syntax:.....Q QN .DF091 C D SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.0	nA
EQL_{pd}	23.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

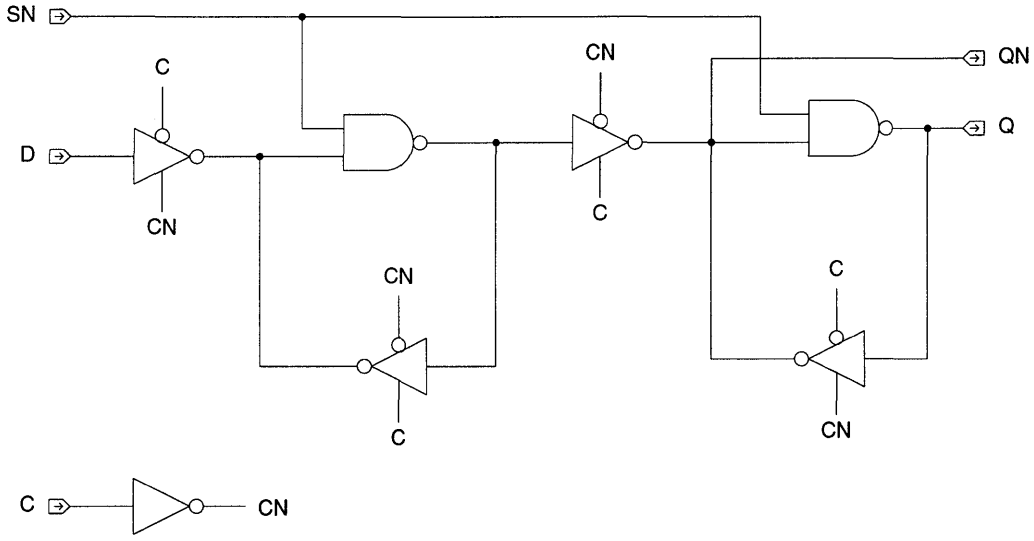
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.55 0.92	0.67 1.04	0.78 1.16	0.89 1.27	1.00 1.38
C	QN	t_{PLH} t_{PHL}	0.69 0.28	0.88 0.39	1.07 0.49	1.26 0.59	1.45 0.69
SN	Q	t_{PLH}	0.29	0.40	0.51	0.62	0.73
SN	QN	t_{PHL}	0.61	0.72	0.82	0.92	1.03

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.95				
Min C Width	Low	t_w	0.88				
Min SN Width	Low	t_w	0.63				
Min D Setup		t_{su}	0.85				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DF0A1

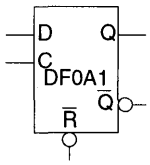
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF0A1 is a static, master-slave, D flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2
RN	1.0

Equivalent Gates:.....7.0

Bolt Syntax:.....Q QN .DF0A1 C D RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	27.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

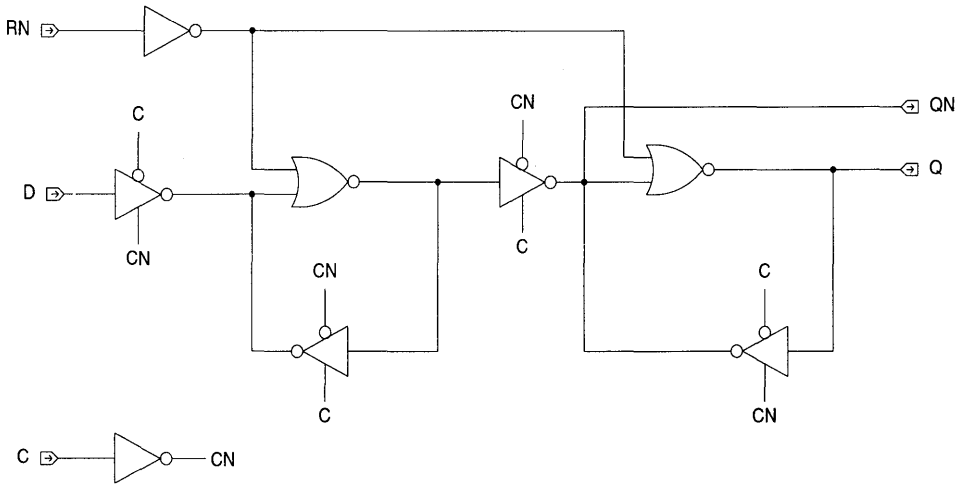
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.73 0.83	0.93 0.93	1.12 1.01	1.32 1.09	1.51 1.17
C	QN	t_{PLH} t_{PHL}	0.70 0.28	0.89 0.38	1.08 0.49	1.28 0.59	1.47 0.69
RN	Q	t_{PHL}	0.48	0.56	0.63	0.70	0.76
RN	QN	t_{PLH}	1.01	1.09	1.17	1.25	1.34

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Min C Width	High	t_w	0.87				
Min C Width	Low	t_w	1.05				
Min RN Width	Low	t_w	1.01				
Min D Setup		t_{su}	0.79				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.67				
Min RN Hold		t_h	0.55				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Schematic Logic



DF0B1

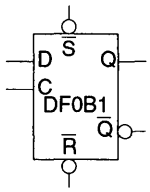
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF0B1 is a static, master-slave, D flip-flop. SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

NC = No Change
IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
C	3.2
SN	2.0
RN	2.1

Equivalent Gates:.....9.0

Bolt Syntax:.....Q QN .DF0B1 C D RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.9	nA
EQL_{pd}	31.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.56 0.93	0.67 1.06	0.78 1.17	0.89 1.28	0.99 1.39
C	QN	t_{PLH} t_{PHL}	0.67 0.28	0.86 0.39	1.05 0.49	1.24 0.59	1.42 0.69
RN	Q	t_{PHL}	1.01	1.14	1.26	1.37	1.48
RN	QN	t_{PLH}	0.73	0.94	1.13	1.33	1.53
SN	Q	t_{PLH}	0.31	0.42	0.52	0.63	0.73
SN	QN	t_{PHL}	0.81	0.96	1.10	1.25	1.39

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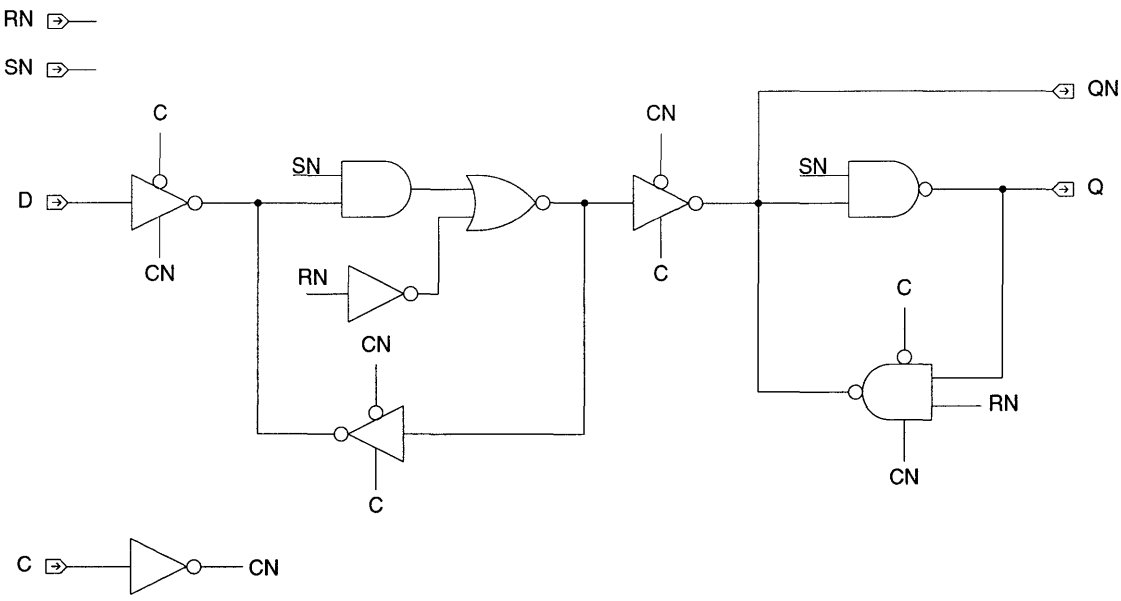
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.97				
Min C Width	Low	t_w	1.05				
Min RN Width	Low	t_w	0.97				
Min SN Width	Low	t_w	0.84				
Min D Setup		t_{su}	0.83				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.70				
Min RN Hold		t_h	0.56				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DF101

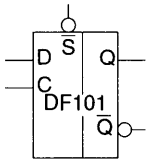
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF101 is a static, master-slave, D flip-flop. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2
SN	2.0

Equivalent Gates:.....8.0

Bolt Syntax:.....Q QN .DF101 C D SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.7	nA
EQL_{pd}	28.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.55 0.86	0.73 1.03	0.95 1.21	1.16 1.37	1.37 1.52
C	QN	t_{PLH} t_{PHL}	1.38 0.82	1.56 0.95	1.77 1.10	1.97 1.23	2.18 1.36
SN	Q	t_{PLH}	0.98	1.15	1.37	1.57	1.78
SN	QN	t_{PHL}	0.46	0.59	0.73	0.87	0.99

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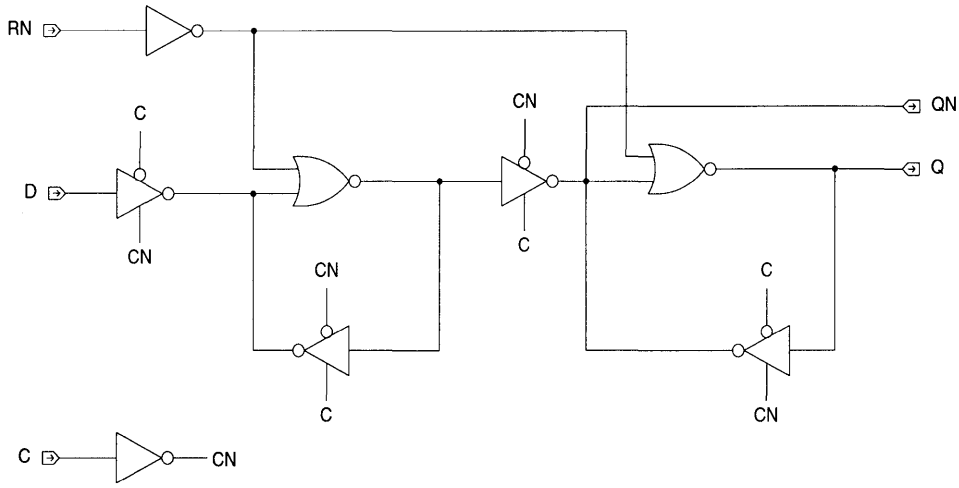
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.78				
Min C Width	Low	t_w	0.85				
Min SN Width		t_w	0.60				
Min D Setup		t_{su}	0.82				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.26				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Schematic Logic



DF111

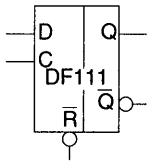
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF111 is a static, master-slave, D flip-flop. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2
RN	1.0

Equivalent Gates:.....8.0

Bolt Syntax:.....Q QN .DF111 C D RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.9	nA
EQL_{pd}	32.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

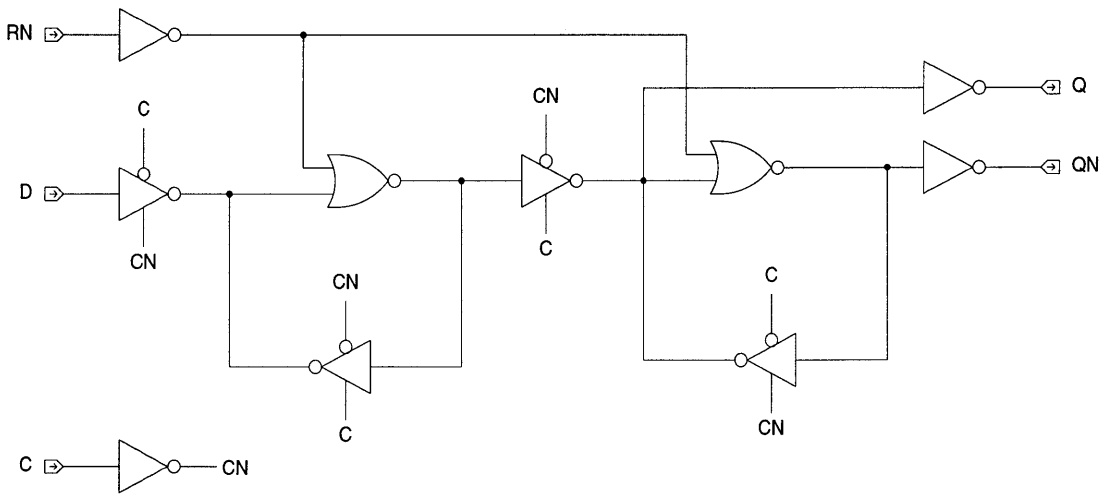
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.54 0.87	0.72 1.04	0.94 1.23	1.15 1.38	1.36 1.53
C	QN	t_{PLH} t_{PHL}	1.19 0.97	1.35 1.13	1.56 1.29	1.76 1.43	1.97 1.57
RN	Q	t_{PHL}	1.28	1.45	1.62	1.78	1.92
RN	QN	t_{PLH}	0.68	0.84	1.05	1.26	1.46

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.79				
Min C Width	Low	t_w	1.01				
Min RN Width		t_w	1.01				
Min D Setup		t_{su}	0.77				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.64				
Min RN Hold		t_h	0.56				

Delay will vary with input conditions. See page 2-15 for interconnect estimates

Logic Schematic



DF121

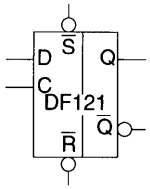
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF121 is a static, master-slave, D flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1
SN	2.0
RN	2.1

Equivalent Gates:.....10.0

Bolt Syntax:.....Q QN .DF121 C D RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	35.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

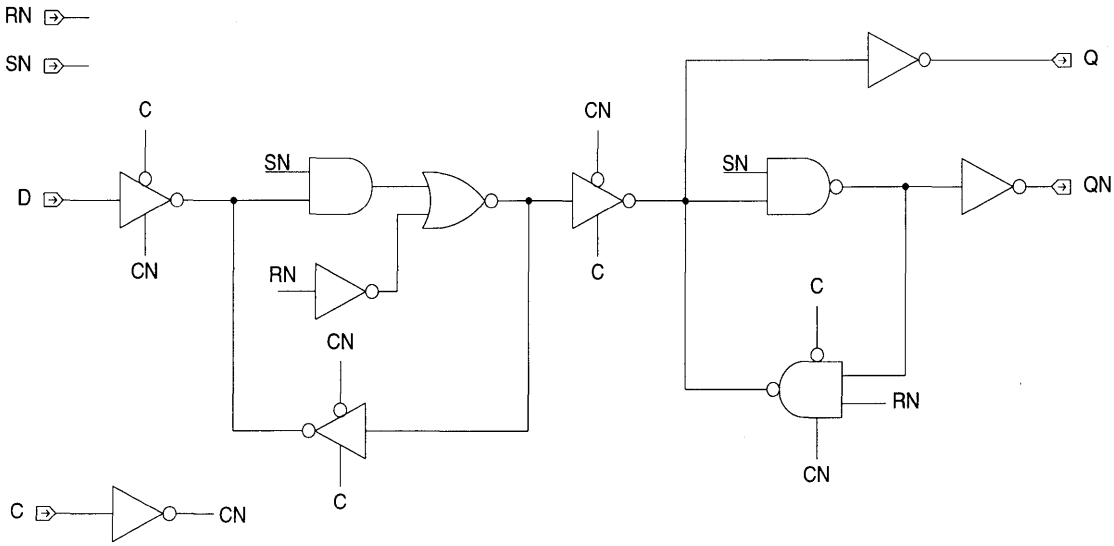
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.55 0.84	0.72 1.01	0.94 1.18	1.15 1.34	1.36 1.48
C	QN	t_{PLH} t_{PHL}	1.37 0.82	1.55 0.95	1.76 1.09	1.97 1.22	2.18 1.35
SN	Q	t_{PLH}	1.23	1.42	1.65	1.86	2.07
SN	QN	t_{PHL}	0.47	0.60	0.75	0.88	1.01
RN	Q	t_{PHL}	0.90	1.08	1.26	1.42	1.56
RN	QN	t_{PLH}	1.46	1.63	1.84	2.05	2.26

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.76				
Min C Width	Low	t_w	1.05				
Min RN Width	Low	t_w	0.96				
Min SN Width	Low	t_w	0.84				
Min D Setup		t_{su}	0.83				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.70				
Min RN Hold		t_h	0.56				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DF281

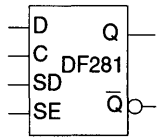
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF281 is a static, master-slave, multiplexed scan, D flip-flop without SET or RESET. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q	QN
↑	H	X	X	H	L
↑	L	X	X	L	H
↑	X	H	H	H	L
↑	X	L	H	H	L
L	X	X	X	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
C	3.1
D	1.0
SD	1.0
SE	2.1

Equivalent Gates:.....8.0

Bolt Syntax:.....Q QN .DF281 C D SD SE;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.0	nA
EQL_{pd}	29.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

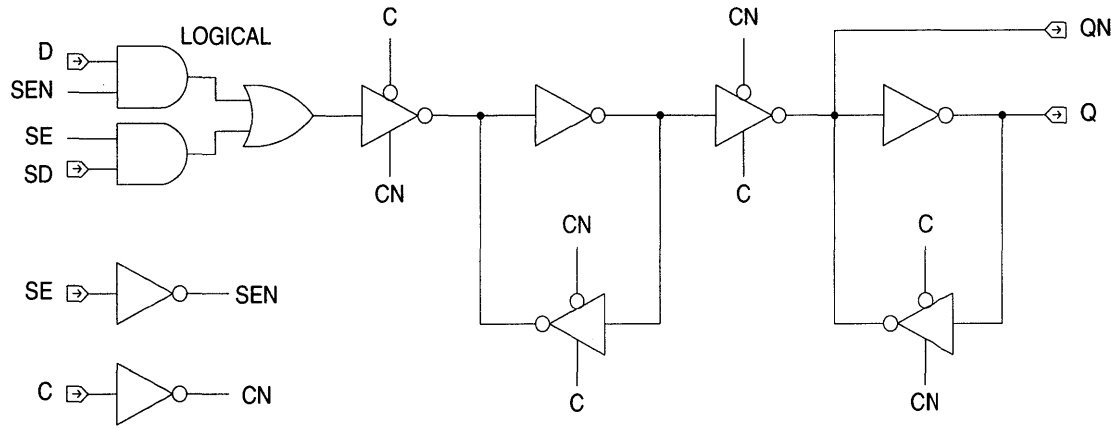
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.53 0.80	0.64 0.90	0.75 0.99	0.85 1.06	0.95 1.14
C	QN	t_{PLH} t_{PHL}	0.69 0.29	0.87 0.39	1.06 0.49	1.24 0.59	1.43 0.70

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.59				
Min C Width	Low	t_w	1.03				
Min D Setup		t_{su}	1.17				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.17				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.35				
Min SE Hold		t_h	0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded

Logic Schematic



DF291

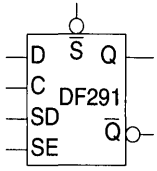
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF291 is a static, master-slave, multiplexed scan, D flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q	QN
↑	H	X	X	H	H	L
↑	L	X	X	H	L	H
↑	X	H	H	H	H	L
↑	X	L	H	H	L	H
X	X	X	X	L	H	L
L	X	X	X	H	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
C	3.1
D	1.0
SD	1.0
SE	2.1
SN	2.0

Equivalent Gates: 11.0

Bolt Syntax: ..... Q QN .DF291 C D SD SE SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.7	nA
EQL_{pd}	32.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

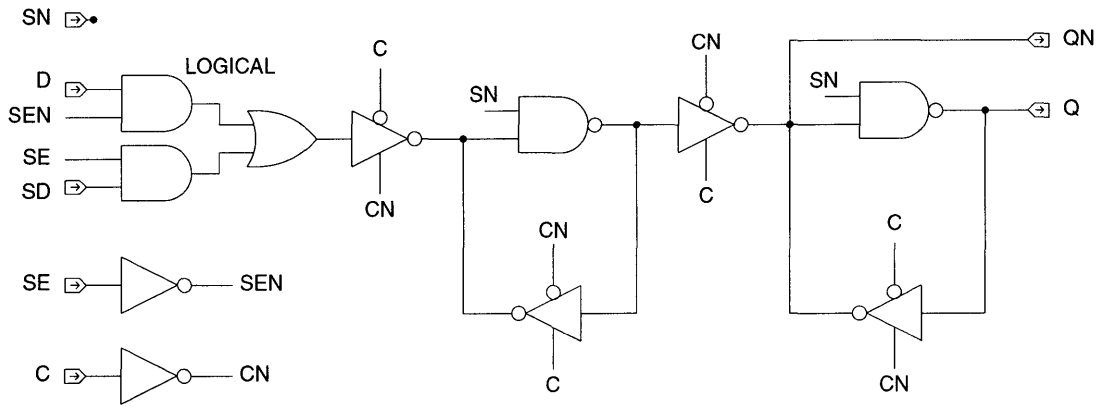
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.58 0.95	0.69 1.08	0.80 1.19	0.90 1.30	1.01 1.41
C	QN	t_{PLH} t_{PHL}	0.69 0.29	0.87 0.40	1.06 0.50	1.25 0.60	1.43 0.71
SN	Q	t_{PLH}	0.30	0.41	0.51	0.62	0.72
SN	QN	t_{PHL}	0.63	0.74	0.84	0.94	1.05

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.59				
Min C Width	Low	t_w	1.15				
Min SN Width	Low	t_w	0.64				
Min D Setup		t_{su}	1.45				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.45				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.65				
Min SE Hold		t_h	0.00				
Min SN Setup		t_{su}	0.29				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded

Logic Schematic



DF2A1

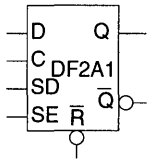
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF2A1 is a static, master-slave, multiplexed scan, D flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q	QN
↑	H	H	X	X	H	L
↑	L	H	X	X	L	H
↑	X	H	H	H	H	L
↑	X	H	L	H	L	H
X	X	L	X	X	L	H
L	X	L	X	X	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
C	3.1
D	1.0
RN	1.0
SD	1.0
SE	2.1

Equivalent Gates:.....11.0

Bolt Syntax:.....Q QN .DF2A1 C D RN SD SE;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.9	nA
EQL_{pd}	36.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

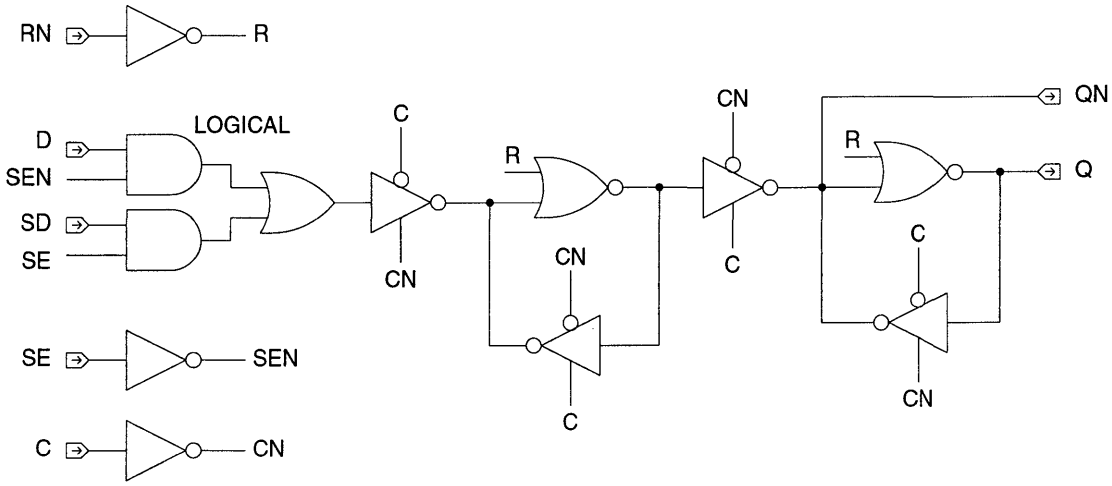
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.74 0.84	0.93 0.94	1.12 1.02	1.31 1.10	1.50 1.17
C	QN	t_{PLH} t_{PHL}	0.70 0.29	0.89 0.39	1.08 0.50	1.27 0.60	1.46 0.70
RN	Q	t_{PHL}	0.49	0.57	0.64	0.70	0.77
RN	QN	t_{PLH}	1.01	1.09	1.18	1.26	1.34

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.61				
Min C Width	Low	t_w	1.35				
Min RN Width	Low	t_w	1.04				
Min D Setup		t_{su}	1.27				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.27				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.45				
Min SE Hold		t_h	0.00				
Min RN Setup		t_{su}	0.68				
Min RN Hold		t_h	0.56				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DF2B1

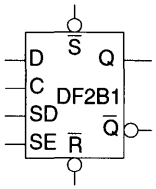
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF2B1 is a static, master-slave, multiplexed scan, D flip-flop. SET and RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	H	H	X	X	H	H	L
↑	L	H	X	X	H	L	H
↑	X	H	H	H	H	H	L
↑	X	H	L	H	H	L	H
X	X	L	X	X	H	L	H
X	X	H	X	X	L	H	L
X	X	H	X	X	H	IL	IL
L	X	L	X	X	H	NC	NC

NC = No Change IL = Illegal Condition

Pin Loading

	Equivalent Load
C	3.2
D	1.0
RN	2.0
SD	1.0
SE	2.1
SN	2.1

Equivalent Gates:.....12.0

Bolt Syntax:.....Q QN .DF2B1 C D RN SD SE SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	38.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

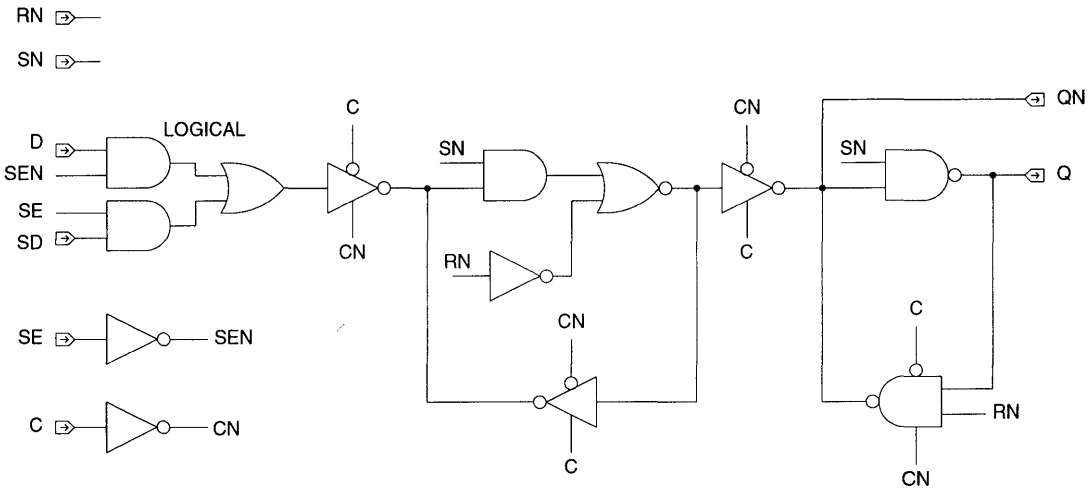
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.55 0.92	0.67 1.05	0.78 1.16	0.89 1.27	0.99 1.38
C	QN	t_{PLH} t_{PHL}	0.69 0.29	0.88 0.40	1.07 0.50	1.25 0.60	1.44 0.71
RN	Q	t_{PHL}	0.98	1.12	1.24	1.35	1.46
RN	QN	t_{PLH}	0.74	0.95	1.14	1.34	1.54
SN	Q	t_{PLH}	0.28	0.38	0.49	0.60	0.70
SN	QN	t_{PHL}	0.80	0.95	1.09	1.23	1.37

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.69				
Min C Width	Low	t_w	1.42				
Min RN Width	Low	t_w	0.98				
Min SN Width	Low	t_w	0.93				
Min D Setup		t_{su}	1.47				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.47				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.67				
Min SE Hold		t_h	0.00				
Min RN Setup		t_{su}	0.74				
Min RN Hold		t_h	0.56				
Min SN Setup		t_{su}	0.31				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DF401

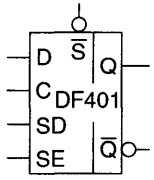
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF401 is a static, master-slave, multiplexed scan, D flip-flop. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q	QN
↑	H	X	X	H	H	L
↑	L	X	X	H	L	H
↑	X	H	H	H	H	L
↑	X	L	H	H	L	H
X	X	X	X	L	H	L
L	X	X	X	H	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
C	3.1
D	1.0
SD	1.0
SE	2.1
SN	2.0

Equivalent Gates:.....12.0

Bolt Syntax:.....Q QN .DF401 C D SD SE SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.5	nA
EQL_{pd}	37.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

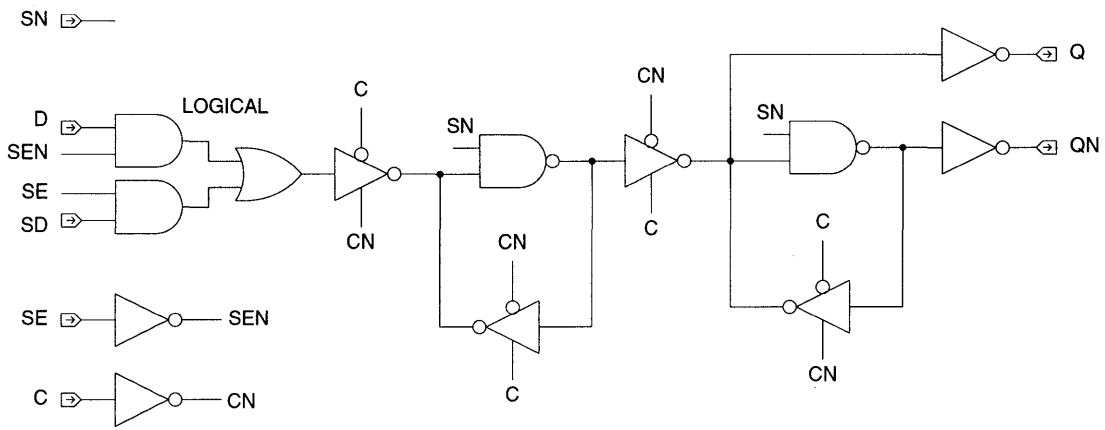
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.57 0.87	0.75 1.04	0.98 1.23	1.19 1.39	1.41 1.54
C	QN	t_{PLH} t_{PHL}	1.40 0.85	1.58 0.99	1.80 1.14	2.01 1.27	2.22 1.40
SN	Q	t_{PLH}	0.99	1.17	1.39	1.61	1.82
SN	QN	t_{PHL}	0.48	0.62	0.77	0.90	1.03

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	1.12				
Min C Width	Low	t_w	1.16				
Min SN Width	Low	t_w	0.72				
Min D Setup		t_{su}	1.49				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.49				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.63				
Min SE Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DF411

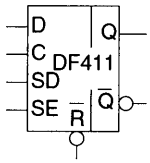
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DF411 is a static, master-slave, multiplexed scan, D flip-flop. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q	QN
↑	H	H	X	X	H	L
↑	L	H	X	X	L	H
↑	X	H	H	H	H	L
↑	X	H	L	H	L	H
X	X	L	X	X	L	H
L	X	L	X	X	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
C	3.1
D	1.0
RN	1.0
SD	1.0
SE	2.1

Equivalent Gates:.....12.0

Bolt Syntax:.....Q QN .DF411 C D RN SD SE;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	40.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

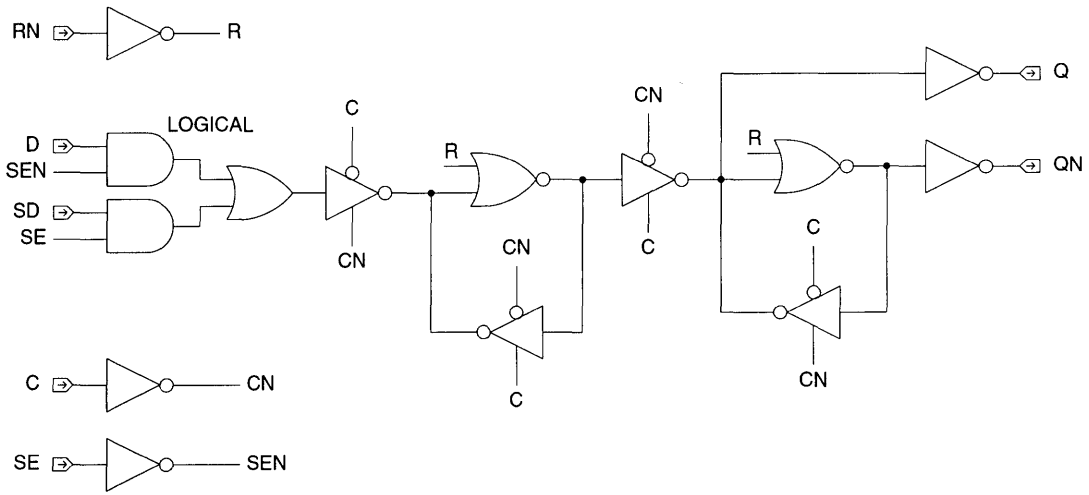
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.56 0.89	0.73 1.06	0.95 1.25	1.16 1.41	1.37 1.56
C	QN	t_{PLH} t_{PHL}	1.22 1.03	1.38 1.19	1.59 1.36	1.79 1.51	2.00 1.65
RN	Q	t_{PHL}	1.30	1.47	1.64	1.80	1.94
RN	QN	t_{PLH}	0.70	0.87	1.07	1.28	1.49

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.97				
Min C Width	Low	t_w	1.35				
Min RN Width	Low	t_w	1.03				
Min D Setup		t_{su}	1.27				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.27				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.45				
Min SE Hold		t_h	0.00				
Min RN Setup		t_{su}	0.68				
Min RN Hold		t_h	0.56				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic

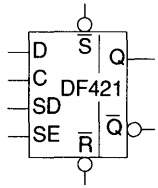


AMI8G 0.8 micron CMOS Gate Array

Description:

DF421 is a static, master-slave, multiplexed scan, D flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	H	H	X	X	H	H	L
↑	L	H	X	X	H	L	H
↑	X	H	H	H	H	H	L
↑	X	H	L	H	H	L	H
X	X	L	X	X	H	L	H
X	X	H	X	X	L	H	L
X	X	H	X	X	H	IL	IL
L	X	L	X	X	H	NC	NC

NC = No Change IL = Illegal Condition

Pin Loading

	Equivalent Load
C	3.2
D	1.0
RN	2.0
SD	1.0
SE	2.1
SN	2.1

Equivalent Gates:.....12.0

Bolt Syntax:.....Q QN .DF421 C D RN SD SE SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	12.4	nA
EQL_{pd}	43.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

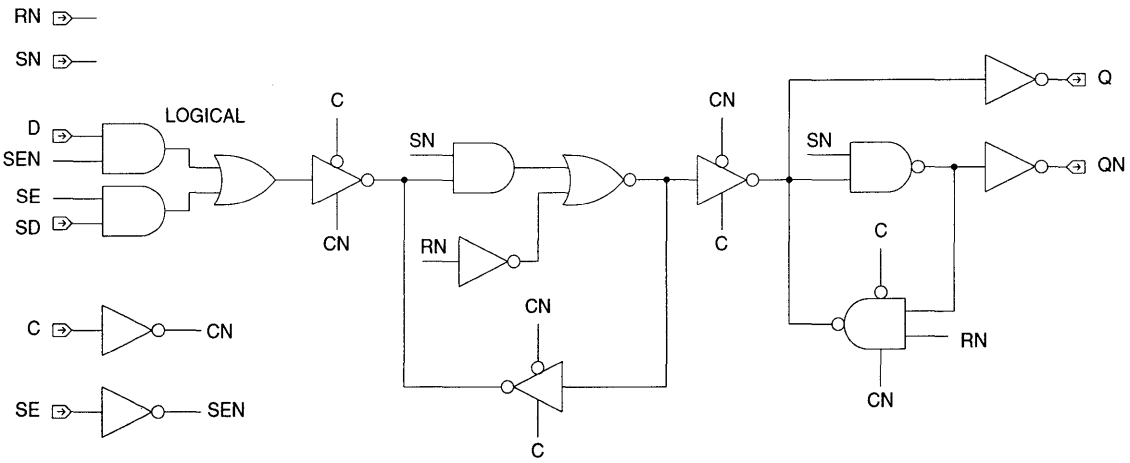
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.57 0.87	0.75 1.04	0.98 1.22	1.20 1.38	1.41 1.53
C	QN	t_{PLH} t_{PHL}	1.35 0.81	1.53 0.94	1.75 1.08	1.96 1.21	2.17 1.34
RN	Q	t_{PHL}	0.92	1.10	1.29	1.45	1.59
RN	QN	t_{PLH}	1.42	1.59	1.81	2.02	2.23
SN	Q	t_{PLH}	1.22	1.42	1.65	1.87	2.08
SN	QN	t_{PHL}	0.44	0.57	0.71	0.84	0.97

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	1.09				
Min C Width	Low	t_w	1.43				
Min RN Width	Low	t_w	0.98				
Min SN Width	Low	t_w	0.93				
Min D Setup		t_{su}	1.47				
Min D Hold		t_h	0.00				
Min SD Setup		t_{su}	1.47				
Min SD Hold		t_h	0.00				
Min SE Setup		t_{su}	1.67				
Min SE Hold		t_h	0.00				
Min RN Setup		t_{su}	0.74				
Min RN Hold		t_h	0.56				
Min SN Setup		t_{su}	0.31				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DFA81

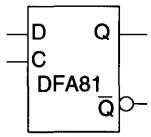
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFA81 is a static, master-slave, D flip-flop without SET or RESET. Outputs are unbuffered and change state on the rising edge of the clock. Transmission gate equivalent of DF081.

Logic Symbol



Truth Table

D	C	Q	QN
H	↑	H	L
L	↑	L	H
X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2

Equivalent Gates: 6.0

Bolt Syntax: ..... Q QN .DFA81 C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	18.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

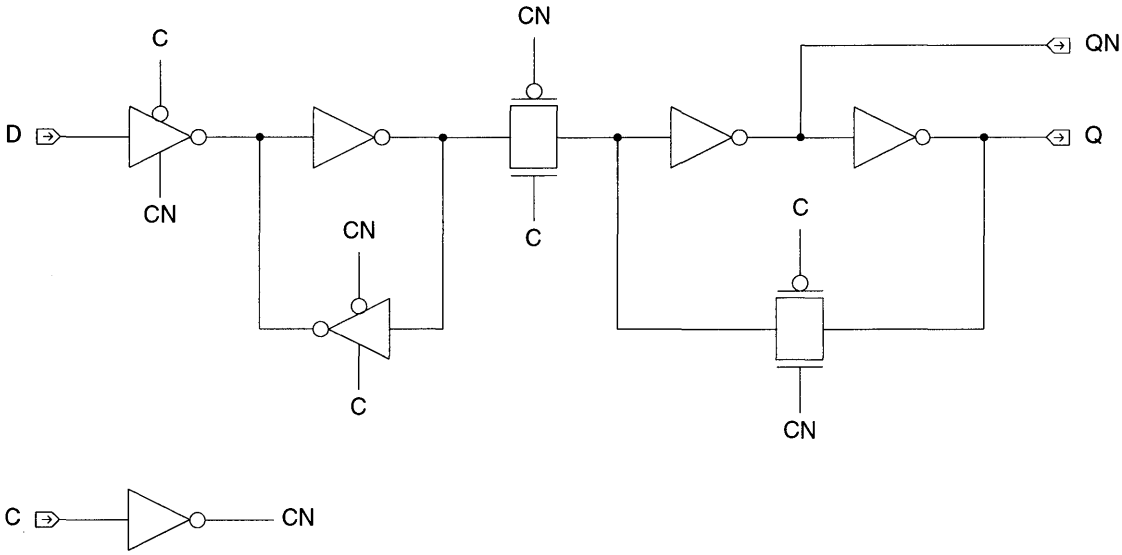
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.71 0.59	0.82 0.66	0.93 0.73	1.03 0.80	1.14 0.87
C	QN	t_{PLH} t_{PHL}	0.51 0.56	0.63 0.66	0.74 0.75	0.85 0.83	0.96 0.91
Min C Width	High	t_w	0.50				
Min C Width	Low	t_w	0.62				
Min D Setup		t_{su}	0.54				
Min D Hold		t_h	0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

(continued on next page)

Logic Schematic



DFA91

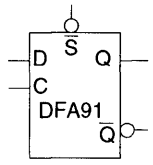
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFA91 is a static, master-slave, D flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Transmission gate equivalent of DF091.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1
SN	2.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q QN .DFA91 C D SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	21.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

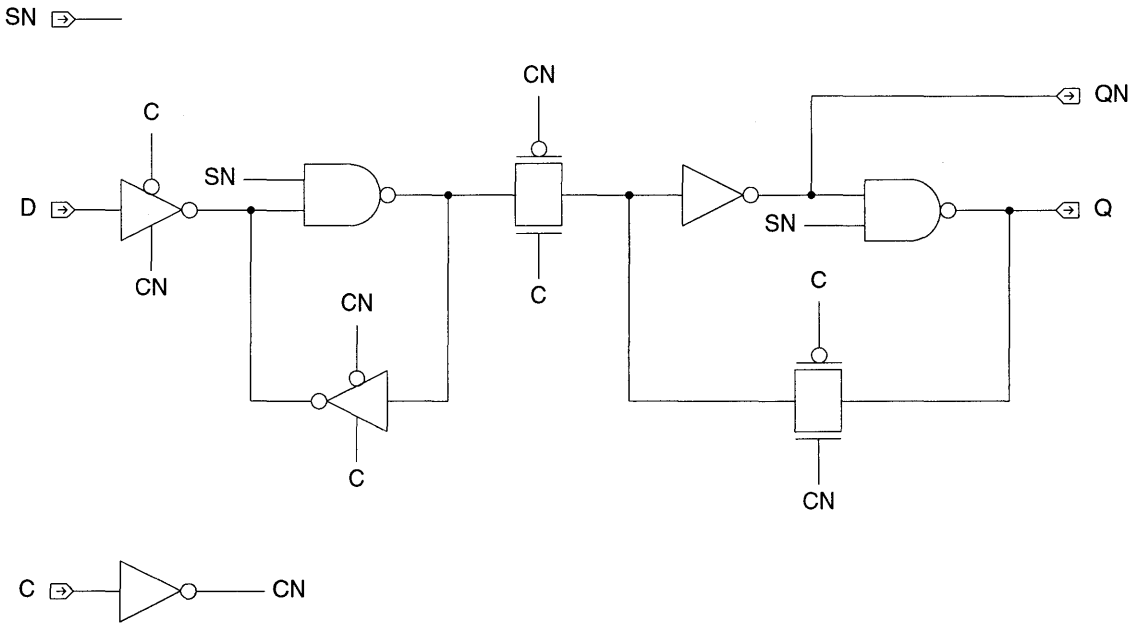
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.70 0.67	0.81 0.78	0.91 0.88	1.01 0.98	1.11 1.09
C	QN	t_{PLH} t_{PHL}	0.48 0.51	0.61 0.61	0.72 0.69	0.83 0.77	0.94 0.85
SN	Q	t_{PLH}	0.39	0.50	0.61	0.72	0.83
SN	QN	t_{PHL}	0.64	0.74	0.83	0.91	0.99

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.72				
Min C Width	Low	t_w	0.69				
Min SN Width	Low	t_w	0.79				
Min D Setup		t_{su}	0.71				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.21				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DFAA1

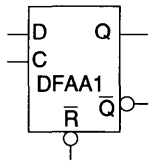
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFAA1 is a static, master-slave, D flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Transmission gate equivalent of DF0A1.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1
RN	2.1

Equivalent Gates:.....7.0

Bolt Syntax:.....Q QN .DFAA1 C D RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	21.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

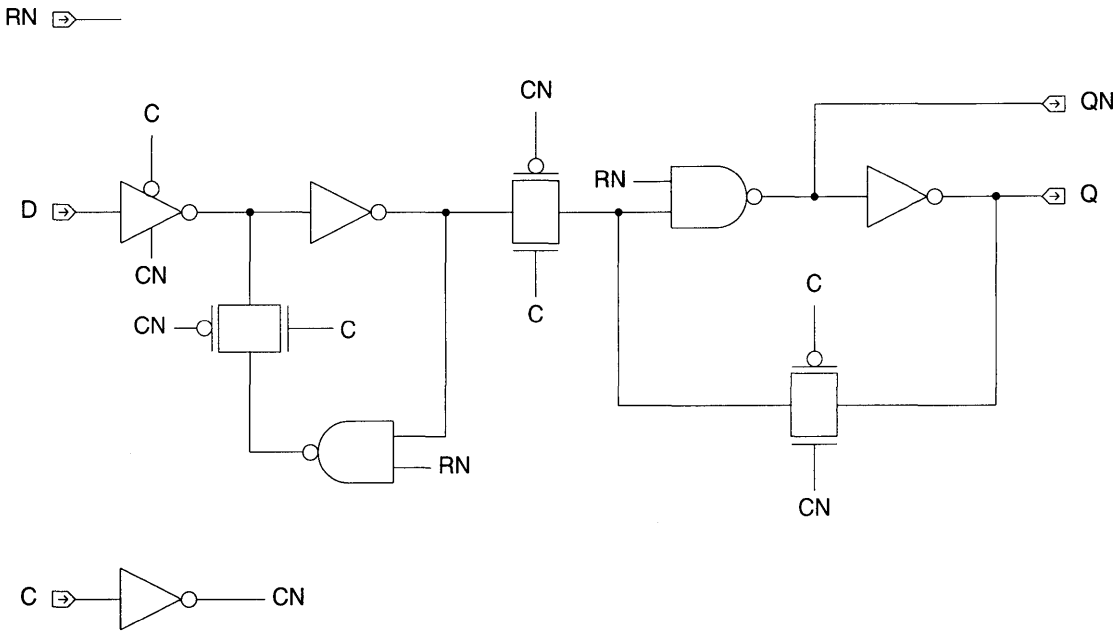
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.81 0.59	0.93 0.67	1.03 0.74	1.13 0.81	1.24 0.88
C	QN	t_{PLH} t_{PHL}	0.51 0.66	0.63 0.79	0.74 0.91	0.84 1.03	0.95 1.14
RN	Q	t_{PHL}	0.47	0.56	0.63	0.70	0.78
RN	QN	t_{PLH}	0.28	0.39	0.49	0.60	0.70

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.85				
Min C Width	Low	t_w	0.66				
Min RN Width	Low	t_w	0.46				
Min D Setup		t_{su}	0.58				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.19				
Min RN Hold		t_h	0.35				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Schematic Logic



DFAB1

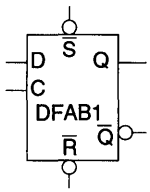
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFAB1 is a static, master-slave, D flip-flop. SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock. Transmission gate equivalent of DF0B1.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

NC = No Change
IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
C	3.1
SN	2.0
RN	2.0

Equivalent Gates: 7.0

Bolt Syntax: ..... Q QN .DFAB1 C D RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.8	nA
EQL_{pd}	22.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

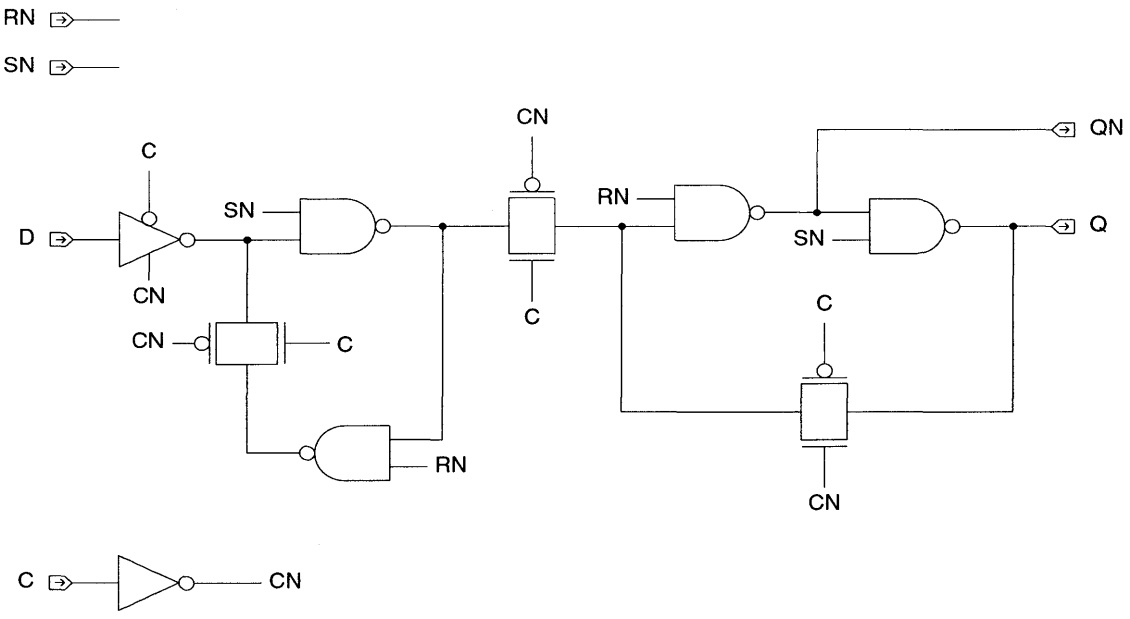
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.81 0.69	0.92 0.80	1.02 0.90	1.12 1.00	1.22 1.10
C	QN	t_{PLH} t_{PHL}	0.50 0.61	0.62 0.73	0.73 0.85	0.84 0.97	0.95 1.07
RN	Q	t_{PHL}	0.63	0.74	0.85	0.96	1.06
RN	QN	t_{PLH}	0.27	0.38	0.48	0.59	0.69
SN	Q	t_{PLH}	0.39	0.49	0.60	0.71	0.81
SN	QN	t_{PHL}	0.74	0.87	0.99	1.11	1.21

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min C Width	High	t_w	0.84				
Min C Width	Low	t_w	0.67				
Min RN Width	Low	t_w	0.46				
Min SN Width	Low	t_w	0.96				
Min D Setup		t_{su}	0.68				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.19				
Min RN Hold		t_h	0.35				
Min SN Setup		t_{su}	0.25				
Min SN Hold		t_h	0.24				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DFB01

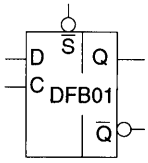
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFB01 is a static, master-slave, D flip-flop. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock. Transmission gate equivalent of DF101.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1
SN	2.0

Equivalent Gates: 7.0

Bolt Syntax: ..... Q QN .DFB01 C D SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.9	nA
EQL_{pd}	25.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

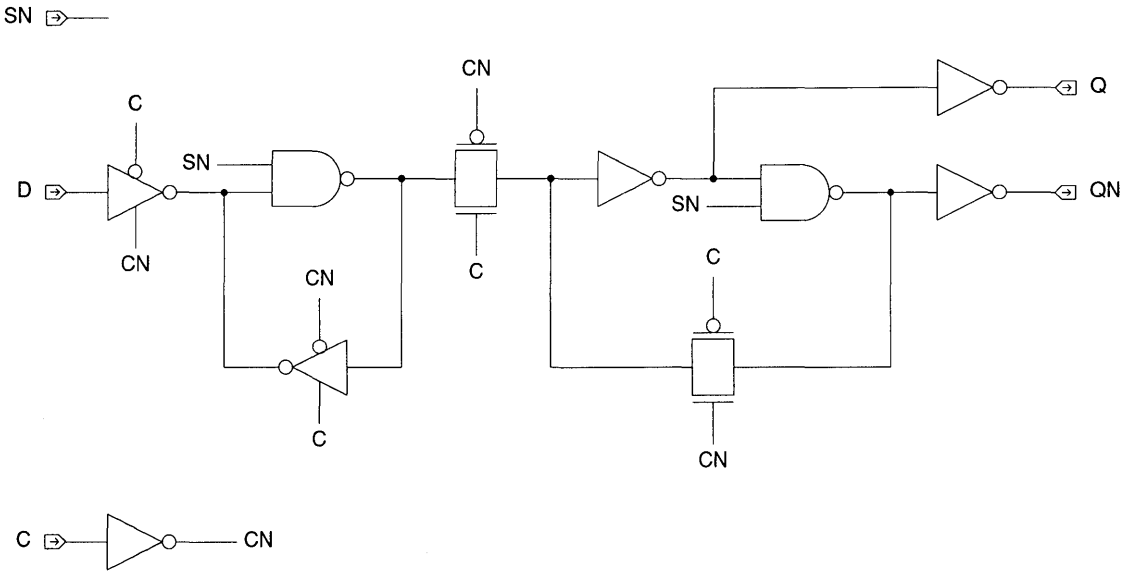
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.73 0.64	0.90 0.76	1.11 0.90	1.33 1.04	1.54 1.17
C	QN	t_{PLH} t_{PHL}	1.02 0.94	1.19 1.06	1.41 1.20	1.62 1.33	1.83 1.46
SN	Q	t_{PLH}	0.96	1.13	1.34	1.55	1.76
SN	QN	t_{PHL}	0.57	0.72	0.88	1.02	1.15

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.67				
Min C Width	Low	t_w	0.69				
Min SN Width		t_w	0.79				
Min D Setup		t_{su}	0.71				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.21				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DFB11

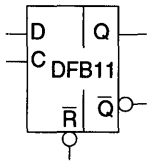
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFB11 is a static, master-slave, D flip-flop. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock. Transmission gate equivalent of DF111

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.2
RN	2.1

Equivalent Gates: 8.0

Bolt Syntax: ..... Q QN .DFB11 C D RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.9	nA
EQL_{pd}	26.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

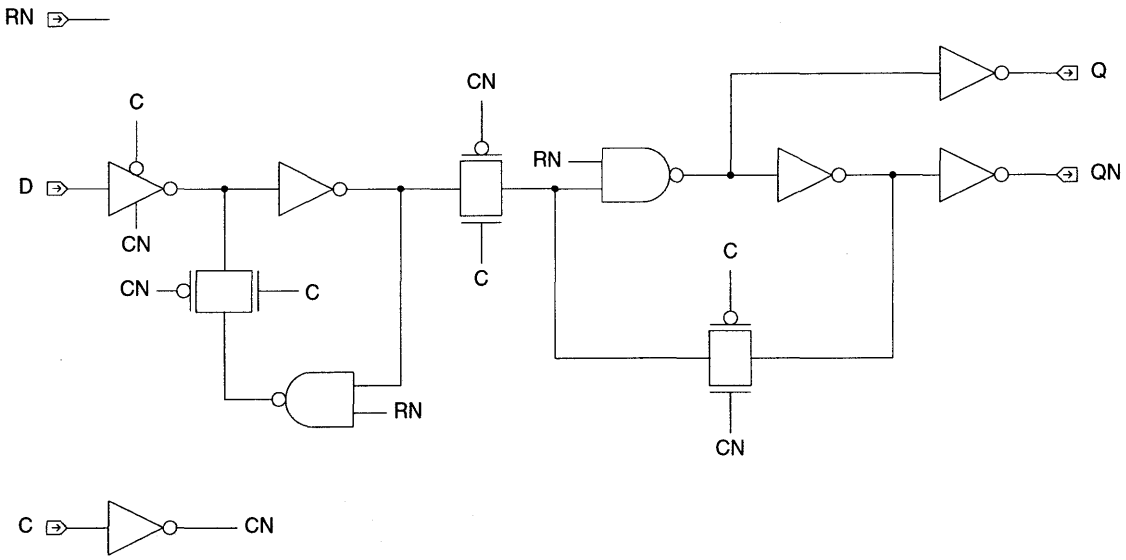
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.91 0.66	1.09 0.80	1.31 0.94	1.52 1.08	1.72 1.21
C	QN	t_{PLH} t_{PHL}	0.87 1.08	1.03 1.20	1.24 1.34	1.44 1.47	1.65 1.59
RN	Q	t_{PHL}	0.44	0.57	0.72	0.85	0.98
RN	QN	t_{PLH}	0.83	1.01	1.22	1.43	1.64

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.84				
Min C Width	Low	t_w	0.66				
Min RN Width		t_w	0.46				
Min D Setup		t_{su}	0.58				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.19				
Min RN Hold		t_h	0.35				

Delay will vary with input conditions. See page 2-15 for interconnect estimates

Logic Schematic



DFB21

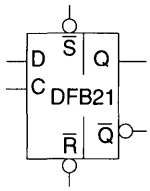
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DFB21 is a static, master-slave, D flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock. Transmission gate equivalent of DF121.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	3.1
SN	2.0
RN	2.0

Equivalent Gates:.....10.0

Bolt Syntax:.....Q QN .DFB21 C D RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	27.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

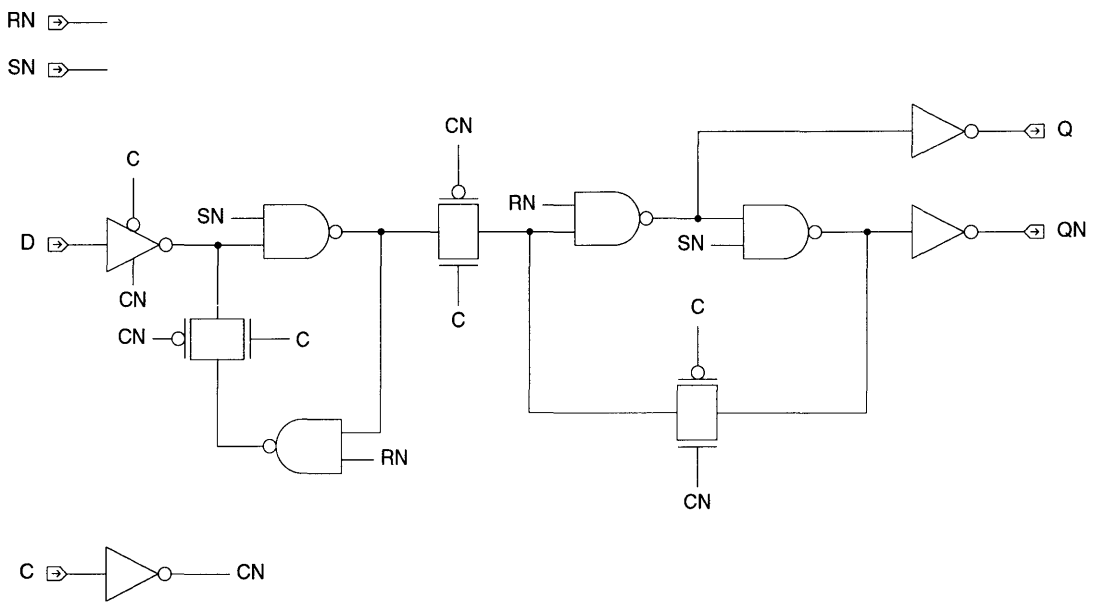
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.86 0.65	1.03 0.78	1.25 0.92	1.46 1.05	1.67 1.18
C	QN	t_{PLH} t_{PHL}	1.03 1.07	1.20 1.20	1.41 1.34	1.62 1.47	1.83 1.59
SN	Q	t_{PLH}	1.08	1.25	1.46	1.67	1.88
SN	QN	t_{PHL}	0.55	0.70	0.86	1.00	1.13
RN	Q	t_{PHL}	0.43	0.55	0.70	0.83	0.96
RN	QN	t_{PLH}	1.04	1.23	1.45	1.67	1.87

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	0.79				
Min C Width	Low	t_w	0.67				
Min RN Width	Low	t_w	0.46				
Min SN Width	Low	t_w	0.96				
Min D Setup		t_{su}	0.68				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.19				
Min RN Hold		t_h	0.35				
Min SN Setup		t_{su}	0.25				
Min SN Hold		t_h	0.24				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DL531

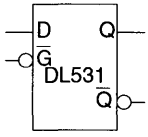
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL531 is a single-phase, unbuffered D latch with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

GN	D	Q	QN
L	L	L	H
L	H	H	L
H	X	NC	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.1

Equivalent Gates:.....3.0

Bolt Syntax:.....Q QN .DL531 D GN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	11.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

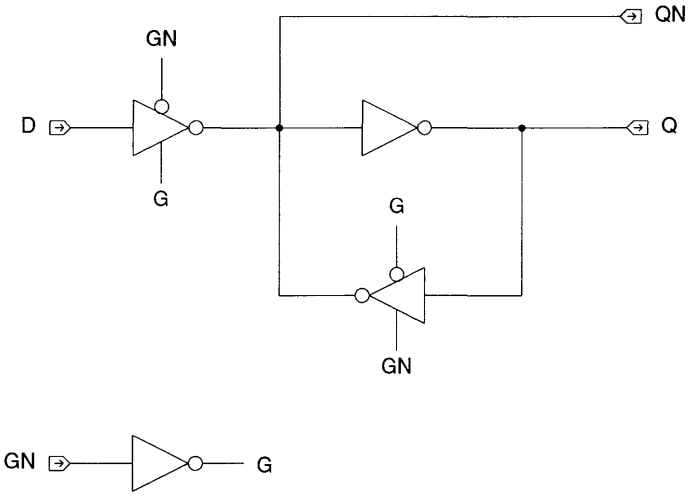
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.59 0.71	0.70 0.81	0.81 0.89	0.91 0.97	1.02 1.04
D	QN	t_{PLH} t_{PHL}	0.60 0.34	0.79 0.45	0.98 0.55	1.18 0.65	1.37 0.75
GN	Q	t_{PLH} t_{PHL}	0.75 0.58	0.86 0.67	0.96 0.76	1.07 0.84	1.17 0.91
GN	QN	t_{PLH} t_{PHL}	0.46 0.49	0.66 0.60	0.85 0.70	1.04 0.80	1.23 0.90
Min GN Width	Low	t_w	0.76				
Min D Setup		t_{su}	0.71				
Min D Hold		t_h	0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

(continued on next page)

Logic Schematic



DL541

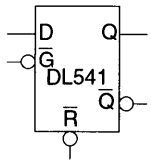
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL541 is a single-phase, unbuffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.1
RN	1.0

Equivalent Gates:.....5.0

Bolt Syntax:.....Q QN .DL541 D GN RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	16.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

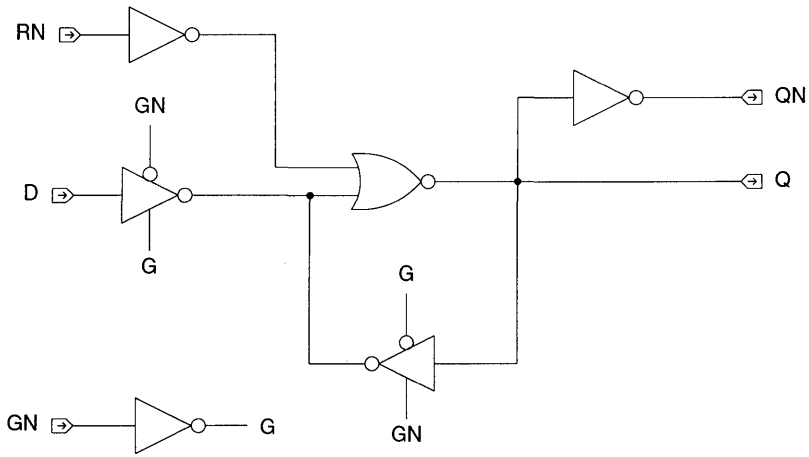
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.88 0.79	1.07 0.88	1.26 0.96	1.45 1.04	1.64 1.12
D	QN	t_{PLH} t_{PHL}	0.95 0.93	1.05 1.03	1.16 1.12	1.25 1.20	1.35 1.28
GN	Q	t_{PLH} t_{PHL}	1.05 0.66	1.24 0.75	1.43 0.83	1.62 0.91	1.81 0.98
GN	QN	t_{PLH} t_{PHL}	0.82 1.09	0.92 1.20	1.02 1.29	1.12 1.37	1.22 1.44
RN	Q	t_{PHL}	0.44	0.54	0.67	0.80	0.93
RN	QN	t_{PLH}	0.60	0.76	0.96	1.16	1.36

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min GN Width	Low	t_w	0.94				
Min RN Width	Low	t_w	1.00				
Min D Setup		t_{su}	0.88				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.60				
Min RN Hold		t_h	0.52				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DL551

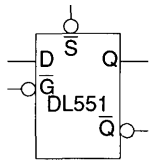
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL551 is a single-phase, unbuffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.1
SN	1.0

Equivalent Gates:.....4.0

Bolt Syntax:.....Q QN .DL551 D GN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	14.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

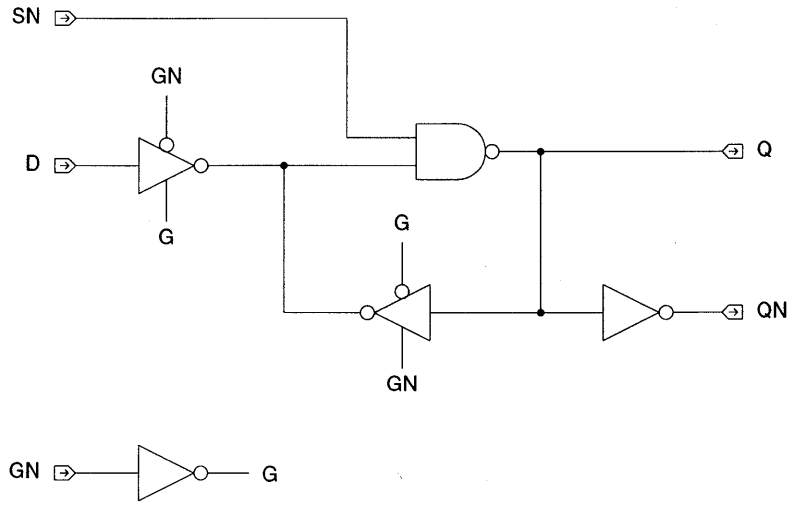
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.70 0.93	0.81 1.04	0.92 1.16	1.02 1.27	1.13 1.37
D	QN	t_{PLH} t_{PHL}	1.12 0.78	1.24 0.87	1.35 0.95	1.45 1.02	1.56 1.09
GN	Q	t_{PLH} t_{PHL}	0.85 0.79	0.96 0.91	1.07 1.02	1.17 1.13	1.28 1.24
GN	QN	t_{PLH} t_{PHL}	0.98 0.93	1.10 1.02	1.21 1.10	1.32 1.17	1.43 1.24
SN	Q	t_{PLH}	0.37	0.47	0.58	0.68	0.79
SN	QN	t_{PHL}	0.46	0.55	0.63	0.70	0.77

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min GN Width	Low	t_w	0.79				
Min SN Width	Low	t_w	0.64				
Min D Setup		t_{su}	0.93				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DL561

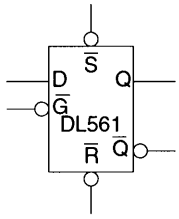
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL561 is a single-phase, unbuffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

NC = No Change IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
GN	2.1
SN	1.0
RN	1.0

Equivalent Gates:.....5.0

Bolt Syntax:.....Q QN .DL561 D GN RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.2	nA
EQL_{pd}	16.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

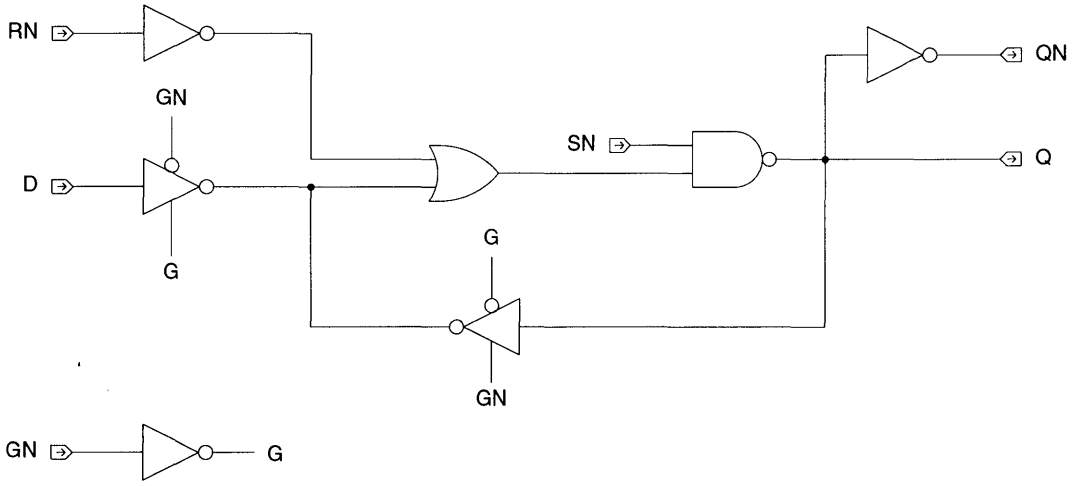
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.91 0.97	1.03 1.09	1.15 1.21	1.26 1.32	1.36 1.43
D	QN	t_{PLH} t_{PHL}	1.15 0.99	1.27 1.08	1.37 1.15	1.48 1.22	1.58 1.29
GN	Q	t_{PLH} t_{PHL}	1.02 0.83	1.14 0.95	1.26 1.07	1.37 1.18	1.48 1.29
GN	QN	t_{PLH} t_{PHL}	1.01 1.10	1.13 1.19	1.24 1.26	1.34 1.34	1.45 1.40
SN	Q	t_{PLH}	0.35	0.46	0.56	0.66	0.77
SN	QN	t_{PHL}	0.44	0.53	0.60	0.67	0.74
RN	Q	t_{PHL}	0.82	0.94	1.05	1.16	1.26
RN	QN	t_{PLH}	0.99	1.11	1.22	1.32	1.43

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Min GN Width	Low	t_w	0.95				
Min RN Width	Low	t_w	0.40				
Min SN Width	Low	t_w	0.80				
Min D Setup		t_{su}	0.97				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.25				
Min SN Hold		t_h	0.33				
Min RN Setup		t_{su}	0.91				
Min RN Hold		t_h	0.20				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



DL641

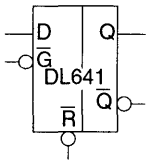
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL641 is a single-phase, buffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.0
RN	1.0

Equivalent Gates:.....6.0

Bolt Syntax: .....Q QN .DL641 D GN RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	21.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

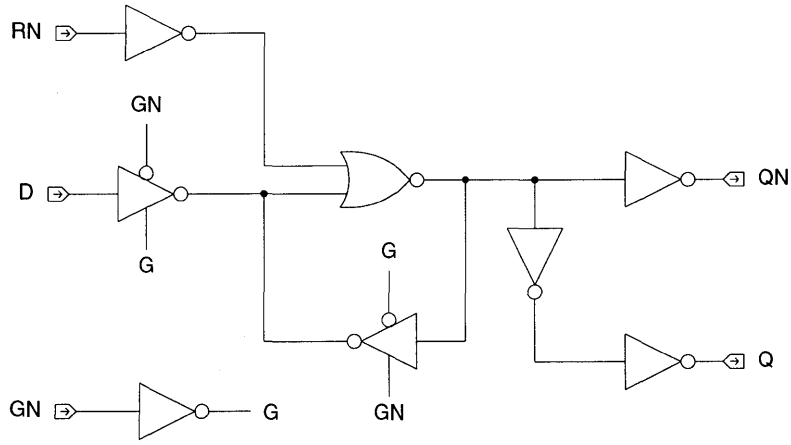
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
D	Q	t_{PLH} t_{PHL}	1.26 1.15	1.42 1.26	1.62 1.39	1.82 1.52	2.02 1.65
D	QN	t_{PLH} t_{PHL}	1.00 1.05	1.17 1.22	1.38 1.41	1.59 1.56	1.79 1.71
GN	Q	t_{PLH} t_{PHL}	1.42 1.02	1.57 1.13	1.77 1.26	1.97 1.39	2.17 1.51
GN	QN	t_{PLH} t_{PHL}	0.87 1.20	1.04 1.37	1.25 1.56	1.46 1.72	1.66 1.86
RN	Q	t_{PHL}	0.79	0.91	1.04	1.16	1.29
RN	QN	t_{PLH}	0.65	0.82	1.03	1.24	1.44

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min GN Width	High	t_w	0.30				
Min GN Width	Low	t_w	1.05				
Min RN Width	Low	t_w	0.97				
Min D Setup		t_{su}	0.91				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.73				
Min RN Hold		t_h	0.50				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DL651

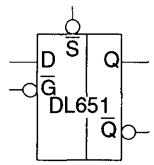
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL651 is a single-phase, buffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.1
SN	1.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q QN .DL651 D GN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	18.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

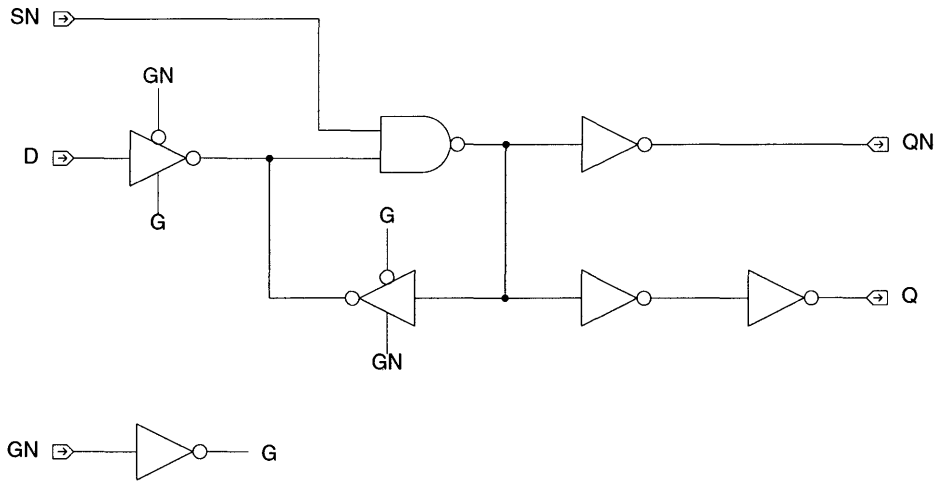
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
D	Q	t_{PLH} t_{PHL}	1.02 1.31	1.18 1.42	1.39 1.55	1.59 1.68	1.80 1.81
D	QN	t_{PLH} t_{PHL}	1.16 0.83	1.34 0.97	1.56 1.12	1.77 1.26	1.98 1.39
GN	Q	t_{PLH} t_{PHL}	1.18 1.18	1.34 1.30	1.55 1.43	1.75 1.55	1.96 1.68
GN	QN	t_{PLH} t_{PHL}	1.03 0.99	1.21 1.13	1.43 1.28	1.64 1.42	1.85 1.55
SN	Q	t_{PLH}	0.70	0.86	1.07	1.27	1.48
SN	QN	t_{PHL}	0.51	0.65	0.81	0.94	1.07

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min GN Width	High	t_w	0.27				
Min GN Width	Low	t_w	0.84				
Min SN Width	Low	t_w	0.69				
Min D Setup		t_{su}	0.88				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.32				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DL661

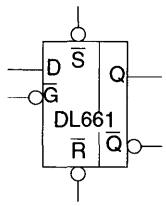
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DL661 is a single-phase, buffered D latch with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.0
SN	1.0
RN	1.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q QN .DL661 D GN RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.0	nA
EQL_{pd}	20.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

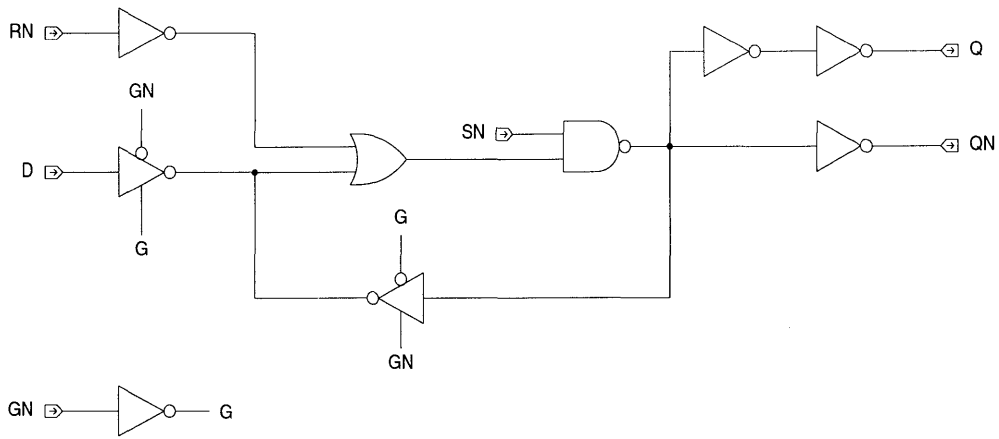
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
D	Q	t_{PLH} t_{PHL}	1.26 1.39	1.41 1.51	1.62 1.64	1.83 1.77	2.03 1.89
D	QN	t_{PLH} t_{PHL}	1.24 1.06	1.43 1.21	1.65 1.36	1.86 1.50	2.07 1.63
GN	Q	t_{PLH} t_{PHL}	1.37 1.26	1.52 1.37	1.73 1.50	1.94 1.63	2.14 1.76
GN	QN	t_{PLH} t_{PHL}	1.11 1.17	1.29 1.32	1.51 1.47	1.72 1.61	1.93 1.74
SN	Q	t_{PLH}	0.70	0.85	1.06	1.27	1.47
SN	QN	t_{PHL}	0.50	0.65	0.80	0.94	1.07
RN	Q	t_{PHL}	1.23	1.35	1.48	1.61	1.73
RN	QN	t_{PLH}	1.08	1.27	1.49	1.70	1.91

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min GN Width	High	t_w	0.28				
Min GN Width	Low	t_w	1.03				
Min RN Width	Low	t_w	0.60				
Min SN Width	Low	t_w	0.87				
Min D Setup		t_{su}	0.97				
Min D Hold		t_h	0.00				
Min SN Setup		t_{su}	0.31				
Min SN Hold		t_h	0.33				
Min RN Setup		t_{su}	0.98				
Min RN Hold		t_h	0.19				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Logic Schematic



DLZ01

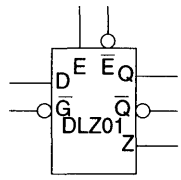
AMI SEMICONDUCTORS
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DLZ01 is a single-phase, unbuffered D latch with active low gate transparency and with a dual-enable tri-state output.

Logic Symbol



Truth Table

D	GN	E	EN	Q	QN	Z
L	L	H	X	L	H	L
H	L	X	L	H	L	H
L	L	L	X	L	H	Z
H	L	X	H	H	L	Z
X	H	H	L	NC	NC	NC
X	H	L	H	NC	NC	Z

Z = High Impedance NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.1
E	0.5
EN	0.6
Z	1.3

Equivalent Gates: 4.0

Bolt Syntax: ..... Q QN Z .DLZ01 D E EN GN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	14.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
D	Q	t_{PLH}	0.68	0.80	0.91	1.01	1.12
		t_{PHL}	0.84	0.95	1.04	1.13	1.21
D	QN	t_{PLH}	0.72	0.91	1.11	1.30	1.49
		t_{PHL}	0.40	0.51	0.61	0.71	0.81
D	Z	t_{PLH}	0.79	0.99	1.18	1.37	1.56
		t_{PHL}	0.86	0.99	1.11	1.22	1.32
GN	Q	t_{PLH}	0.84	0.95	1.06	1.17	1.27
		t_{PHL}	0.71	0.81	0.91	0.99	1.08
GN	QN	t_{PLH}	0.58	0.78	0.97	1.17	1.36
		t_{PHL}	0.55	0.65	0.75	0.85	0.95
GN	Z	t_{PLH}	0.94	1.14	1.33	1.52	1.71
		t_{PHL}	0.73	0.86	0.97	1.08	1.19

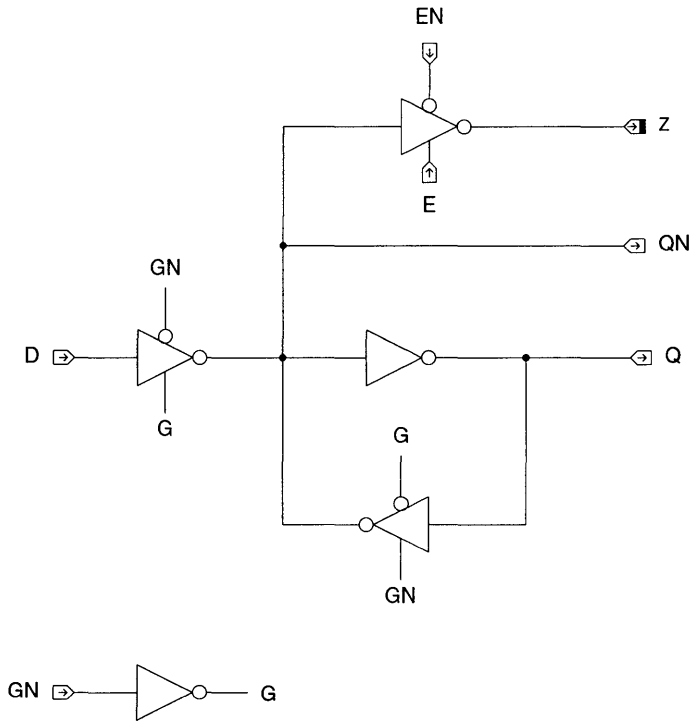
(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
E	Z	t_{PLZ} t_{PZL}	0.09 0.20	0.31	0.41	0.52	0.62
EN	Z	t_{PHZ} t_{PZH}	0.11 0.32	0.51	0.70	0.89	1.08
Min GN Width	Low	t_w	0.85				
Min D Setup		t_{su}	0.84				
Min D Hold		t_h	0.00				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Core Logic

Logic Schematic



DLZ11

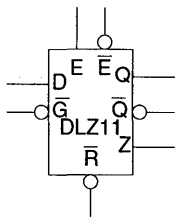
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

DLZ11 is a single-phase, unbuffered D latch with active low gate transparency and with a dual-enable tri-state output. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	E	EN	Q	QN	Z
H	L	L	H	X	L	H	L
H	H	L	X	L	H	L	H
H	L	L	L	X	L	H	Z
H	H	L	X	H	H	L	Z
H	X	H	H	L	NC	NC	NC
H	X	H	L	H	NC	NC	Z
L	X	X	H	L	L	H	L
L	X	X	L	H	L	H	Z

Z = High Impedance NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	2.0
RN	1.0
E	0.4
EN	0.6
Z	1.3

Equivalent Gates:.....5.0

Bolt Syntax:.....Q QN Z .DLZ11 D E EN GN RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
D	Q	t_{PLH} t_{PHL}	0.95 0.90	1.07 1.01	1.19 1.10	1.30 1.19	1.41 1.27
D	QN	t_{PLH} t_{PHL}	0.78 0.60	0.97 0.74	1.16 0.88	1.35 1.02	1.54 1.16
GN	Q	t_{PLH} t_{PHL}	1.05 0.76	1.18 0.96	1.30 0.96	1.41 1.05	1.52 1.13
GN	QN	t_{PLH} t_{PHL}	0.63 0.70	0.83 0.84	1.02 0.98	1.21 1.12	1.41 1.26
RN	Q	t_{PHL}	0.71	0.81	0.90	0.98	1.06
RN	QN	t_{PLH}	0.53	0.65	0.76	0.87	0.97

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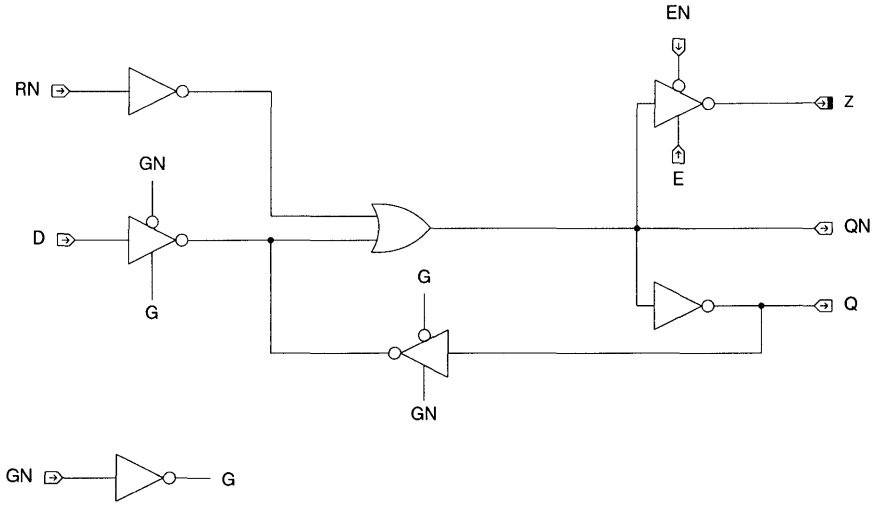
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
RN	Z	t_{PHL} t_{PLH}	0.72 1.10	0.84 1.30	0.95 1.49	1.06 1.68	1.16 1.87
D	Z	t_{PLH} t_{PHL}	1.04 0.91	1.24 1.05	1.43 1.17	1.62 1.28	1.81 1.38
GN	Z	t_{PLH} t_{PHL}	1.15 0.78	1.34 0.91	1.54 1.03	1.73 1.14	1.92 1.24
E	Z	t_{PLZ} t_{PZL}	0.09 0.20	0.31	0.41	0.52	0.62
EN	Z	t_{PHZ} t_{PZH}	0.11 0.32	0.52	0.71	0.90	1.09
Min GN Width	Low	t_w	1.08				
Min RN Width	Low	t_w	0.70				
Min D Setup		t_{su}	0.95				
Min D Hold		t_h	0.00				
Min RN Setup		t_{su}	0.93				
Min RN Hold		t_h	0.20				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Core Logic

Logic Schematic



EN21

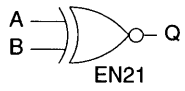
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

EN21 is a 2-input gate which performs the logical exclusive NOR (XNOR) function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

Pin Loading

	Equivalent Load
A	2.0
B	2.0

Equivalent Gates: 3.0

Bolt Syntax: .....Q .EN21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	7.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH}	0.51	0.62	0.77	0.96	1.16
		t_{PHL}	0.48	0.58	0.69	0.79	0.89

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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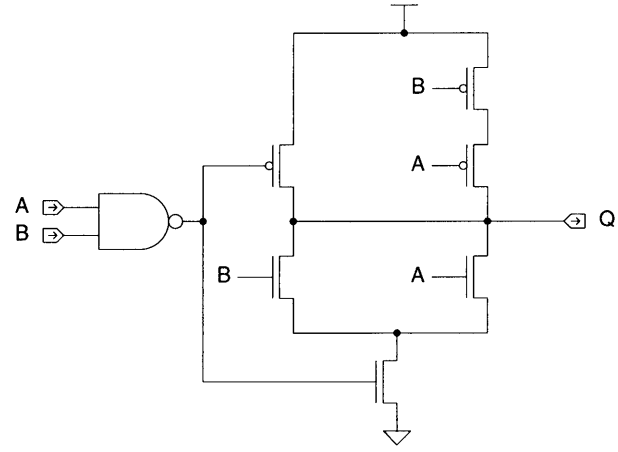
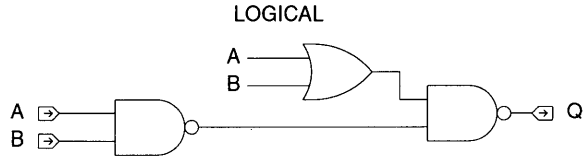
Logic Schematic





E021

American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

EO21 is a 2-input gate which performs the logical exclusive OR (XOR) function.

Logic Symbol

Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.1

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .EO21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	8.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

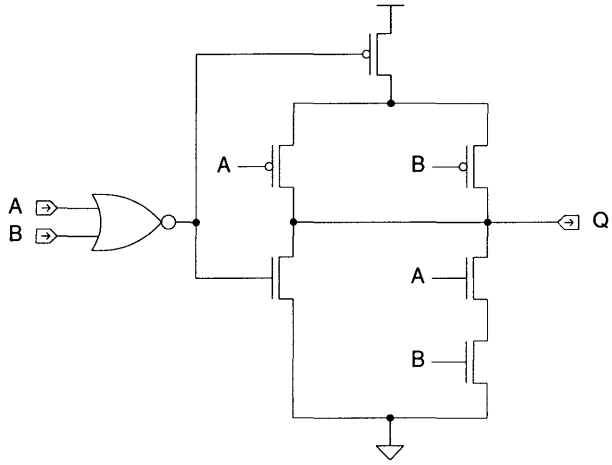
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.61 0.58	0.80 0.66	0.99 0.74	1.18 0.81	1.37 0.88

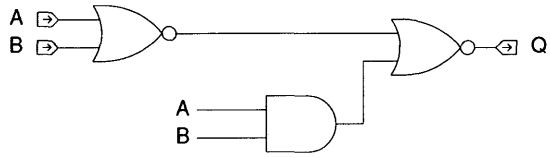
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

Logic Schematic



LOGICAL



EO31

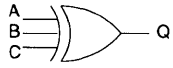
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

EO31 is a 3-input gate which performs the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

Pin Loading

	Equivalent Load
A	2.1
B	2.0
C	2.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q .EO31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.6	nA
EQL_{pd}	18.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

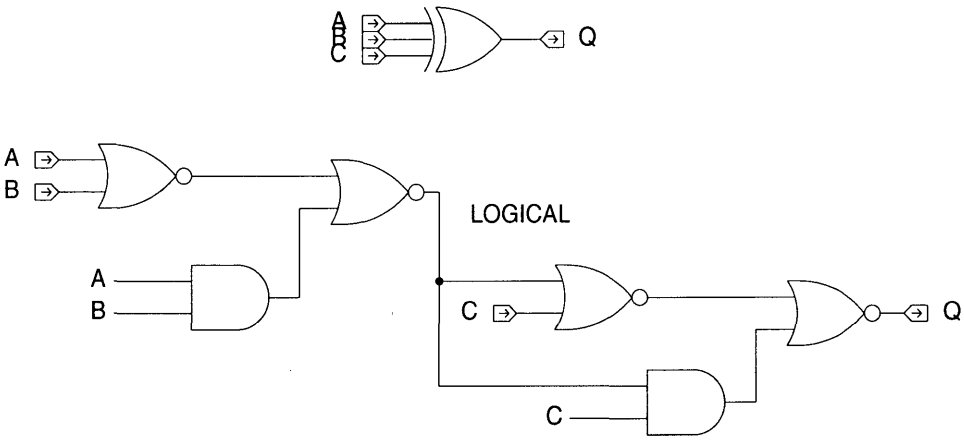
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH}	1.35	1.54	1.72	1.91	2.10
		t_{PHL}	1.26	1.34	1.42	1.49	1.56

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

Logic Schematic

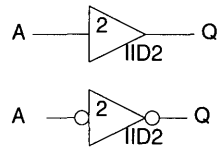


AMI8G 0.8 micron CMOS Gate Array

Description:

IID2 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .IID2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	4.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
A	Q	t_{PLH} t_{PHL}	0.31 0.34	0.47 0.48	0.65 0.60	0.83 0.71	1.01 0.82

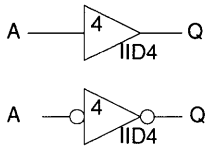
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

IID4 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	2.0

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .IID4 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	11.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	14	27	40	53 (max)
A	Q	t_{PLH}	0.31	0.48	0.65	0.82	0.99
		t_{PHL}	0.35	0.49	0.60	0.70	0.81

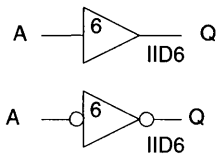
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

IID6 is a non-inverting clock driver with a single output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	2.0

Equivalent Gates:.....4.0

Bolt Syntax:.....Q .IID6 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	16.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

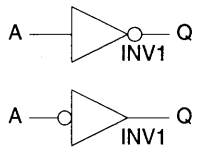
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	39	59	78 (max)
A	Q	t_{PLH}	0.35	0.53	0.70	0.87	1.03
		t_{PHL}	0.41	0.56	0.67	0.78	0.89

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

INV1 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	1.0

Equivalent Gates:.....1.0

Bolt Syntax:.....Q .INV1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.9	nA
EQL_{pd}	1.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
A	Q	t_{PLH}	0.18	0.34	0.55	0.75	0.96
		t_{PHL}	0.12	0.23	0.36	0.49	0.61

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

INV2

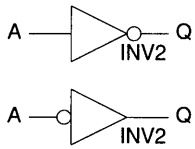
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

INV2 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	2.1

Equivalent Gates:.....1.0

Bolt Syntax:.....Q .INV2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	2.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
A	Q	t_{PLH} t_{PHL}	0.14 0.10	0.31 0.21	0.49 0.32	0.68 0.43	0.87 0.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

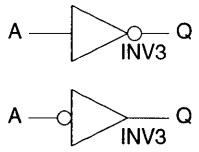
INV3

AMI8G 0.8 micron CMOS Gate Array

Description:

INV3 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	3.0

Equivalent Gates:.....2.0

Bolt Syntax: .....Q .INV3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	2.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
A	Q	t_{PLH}	0.12	0.30	0.48	0.65	0.82
		t_{PHL}	0.08	0.21	0.32	0.42	0.52

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

INV4

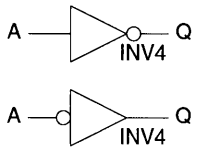
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

INV4 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	4.1

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .INV4 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	2.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	14	27	40	53 (max)
A	Q	t_{PLH}	0.11	0.29	0.46	0.62	0.79
		t_{PHL}	0.07	0.20	0.30	0.40	0.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

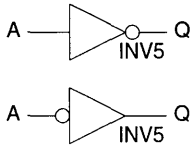
INV5

AMI8G 0.8 micron CMOS Gate Array

Description:

INV5 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	5.1

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .INV5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	4.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	17	33	50	66 (max)
A	Q	t_{PLH}	0.11	0.29	0.45	0.63	0.79
		t_{PHL}	0.07	0.20	0.30	0.40	0.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

INV6

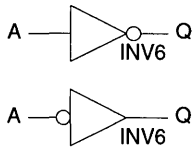
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

INV6 is an inverter which performs the logical NOT function.

Logic Symbol



Truth Table

A	Q
L	H
H	L

Pin Loading

	Equivalent Load
A	6.1

Equivalent Gates: 3.0

Bolt Syntax: .....Q .INV6 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	4.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

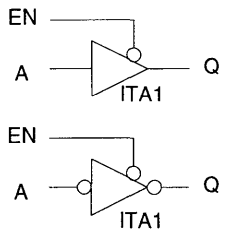
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	39	59	78 (max)
A	Q	t_{PLH}	0.10	0.28	0.44	0.61	0.77
		t_{PHL}	0.06	0.19	0.29	0.39	0.49

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

ITA1 is a non-inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

Pin Loading

	Equivalent Load
A	1.0
EN	1.6
Q	1.3

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .ITA1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	6.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
A	Q	t_{PLH} t_{PHL}	0.53 0.43	0.73 0.54	0.93 0.65	1.12 0.75	1.31 0.86
EN	Q	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.11 0.17 0.25 0.29	0.44 0.40	0.63 0.51	0.83 0.61	1.02 0.72

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ITA2

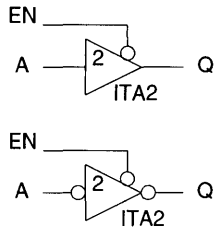
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ITA2 is a non-inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	Q
H	X	Z
L	L	L
L	H	H

Z = High Impedance

Pin Loading

	Equivalent Load
A	1.0
EN	2.7
Q	4.0

Equivalent Gates:.....4.0

Bolt Syntax:.....QN .ITA2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	15.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	6	11	17	22 (max)
A	Q	t_{PLH}	0.55	0.72	0.88	1.07	1.23
		t_{PHL}	0.53	0.63	0.73	0.84	0.92
EN	Q	t_{HZ}	0.11				
		t_{LZ}	0.25				
		t_{ZH}	0.18	0.34	0.50	0.68	0.84
		t_{ZL}	0.30	0.41	0.51	0.61	0.70

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

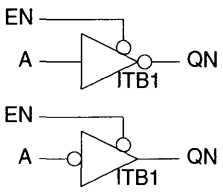
ITB1

AMI8G 0.8 micron CMOS Gate Array

Description:

ITB1 is an inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

Pin Loading

	Equivalent Load
A	1.0
EN	1.6
QN	1.3

Equivalent Gates:.....2.0

Bolt Syntax:.....QN .ITB1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	4.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
A	QN	t_{LH}	0.39	0.59	0.78	0.97	1.16
		t_{PHL}	0.23	0.34	0.44	0.54	0.64
EN	QN	t_{HZ}	0.11				
		t_{LZ}	0.17				
		t_{ZH}	0.25	0.43	0.63	0.82	1.01
		t_{ZL}	0.29	0.40	0.50	0.60	0.70

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ITB2

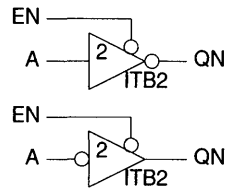
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ITB2 is an inverting internal tri-state buffer with active low enable.

Logic Symbol



Truth Table

EN	A	QN
H	X	Z
L	L	H
L	H	L

Z = High Impedance

Pin Loading

	Equivalent Load
A	3.2
EN	2.7
QN	4.0

Equivalent Gates: 4.0

Bolt Syntax: .....QN .ITB2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	10.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

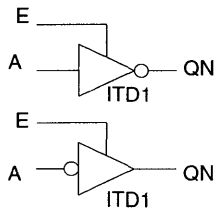
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	6	11	17	22 (max)
A	QN	t_{PLH}	0.32	0.49	0.65	0.84	1.00
		t_{PHL}	0.20	0.30	0.39	0.49	0.57
EN	QN	t_{HZ}	0.11				
		t_{LZ}	0.25				
		t_{ZH}	0.18	0.34	0.50	0.69	0.84
		t_{ZL}	0.30	0.40	0.50	0.60	0.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

ITD1 is an inverting internal tri-state buffer with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

Pin Loading

	Equivalent Load
A	1.0
E	1.5
QN	1.3

Equivalent Gates:.....2.0

Bolt Syntax:.....QN .ITD1 A E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	4.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
A	QN	t_{PLH}	0.40	0.59	0.78	0.97	1.16
		t_{PHL}	0.22	0.33	0.43	0.54	0.64
E	QN	t_{HZ}	0.26				
		t_{LZ}	0.09				
		t_{ZH}	0.33	0.52	0.71	0.90	1.09
		t_{ZL}	0.15	0.26	0.36	0.46	0.56

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ITD2

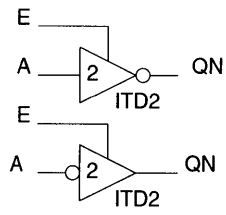
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ITD2 is an inverting internal tri-state buffer with active high enable.

Logic Symbol



Truth Table

E	A	QN
L	X	Z
H	L	H
H	H	L

Z = High Impedance

Pin Loading

	Equivalent Load
A	3.2
E	2.5
QN	4.0

Equivalent Gates:.....4.0

Bolt Syntax:.....QN .ITD2 A E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	11.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

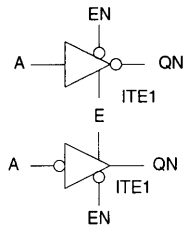
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	6	11	17	22 (max)
A	QN	t_{PLH}	0.34	0.51	0.67	0.86	1.02
		t_{PHL}	0.18	0.28	0.36	0.47	0.55
E	QN	t_{HZ}	0.42				
		t_{LZ}	0.09				
		t_{ZH}	0.32	0.48	0.64	0.83	0.99
		t_{ZL}	0.10	0.21	0.29	0.39	0.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

ITE1 is a two-phase inverting internal tri-state buffer.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

IL = Illegal

Pin Loading

	Equivalent Load
A	1.0
E	0.4
EN	0.5
QN	1.3

Equivalent Gates:.....1.0

Bolt Syntax: .....QN .ITE1 A E EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.9	nA
EQL_{pd}	2.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
A	QN	t_{PLH} t_{PHL}	0.40 0.22	0.59 0.33	0.78 0.43	0.97 0.53	1.16 0.64
EN	QN	t_{HZ} t_{ZH}	0.11 0.33	0.52	0.71	0.90	1.09
E	QN	t_{LZ} t_{ZL}	0.09 0.20	0.31	0.41	0.52	0.62

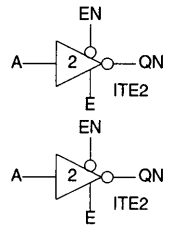
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

ITE2 is a two-phase inverting internal tri-state buffer.

Logic Symbol



Truth Table

EN	E	A	QN
H	L	X	Z
L	H	L	H
L	H	H	L
L	L	X	IL
H	H	X	IL

IL = Illegal

Pin Loading

	Equivalent Load
A	2.1
E	0.9
EN	1.1
QN	2.3

Equivalent Gates:.....2.0

Bolt Syntax:.....QN .ITE2 A E EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	4.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	6	11	17	22 (max)
A	QN	t_{PLH} t_{PHL}	0.34 0.20	0.59 0.33	0.83 0.46	1.11 0.61	1.35 0.74
EN	QN	t_{HZ} t_{ZH}	0.11 0.27	0.51	0.75	1.04	1.27
E	QN	t_{LZ} t_{ZL}	0.09 0.17	0.31	0.44	0.59	0.72

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

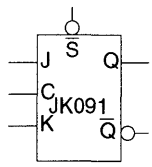
JK091

AMI8G 0.8 micron CMOS Gate Array

Description:

JK091 is a static, master-slave, JK flip-flop. SET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	H	L
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	3.1
SN	2.0

Equivalent Gates: 11.0

Bolt Syntax: ..... Q QN .JK091 C J K SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.5	nA
EQL_{pd}	34.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.70 1.15	0.82 1.29	0.94 1.41	1.05 1.53	1.15 1.65
C	QN	t_{PLH} t_{PHL}	0.88 0.38	1.07 0.49	1.26 0.59	1.45 0.69	1.64 0.79
SN	Q	t_{PLH}	0.28	0.39	0.49	0.60	0.70
SN	QN	t_{PHL}	0.72	0.83	0.93	1.03	1.14

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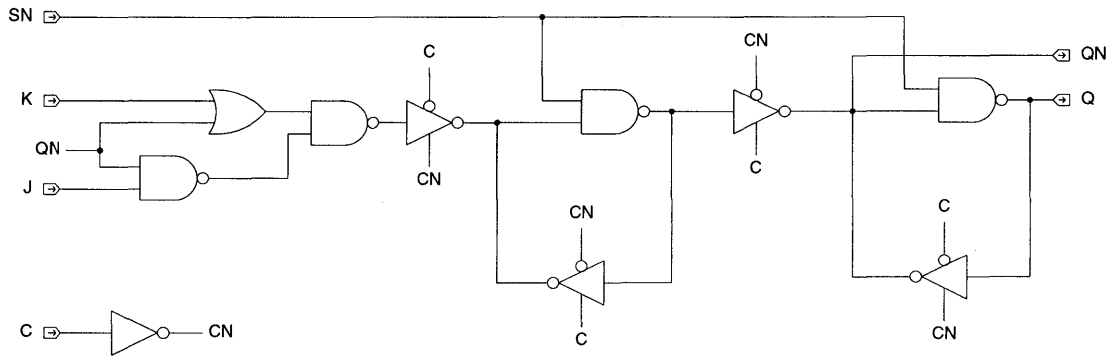
AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Min C Width	High	t_w	1.17				
Min C Width	Low	t_w	0.86				
Min SN Width	Low	t_w	0.63				
Min J Setup		t_{su}	1.45				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.15				
Min K Hold		t_h	0.00				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



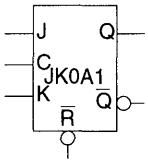
JK0A1

AMI8G 0.8 micron CMOS Gate Array

Description:

JK0A1 is a static, master-slave, JK flip-flop. RESET is asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	J	K	C	Q(n+1)	QN(n+1)
L	X	X	X	L	H
H	L	L	↑	NC	NC
H	L	H	↑	L	H
H	H	L	↑	H	L
H	H	H	↑	QN(n)	Q(n)

NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	3.1
RN	1.0

Equivalent Gates: 11.0

Bolt Syntax: ..... Q QN .JK0A1 C J K RN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.6	nA
EQL_{pd}	38.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

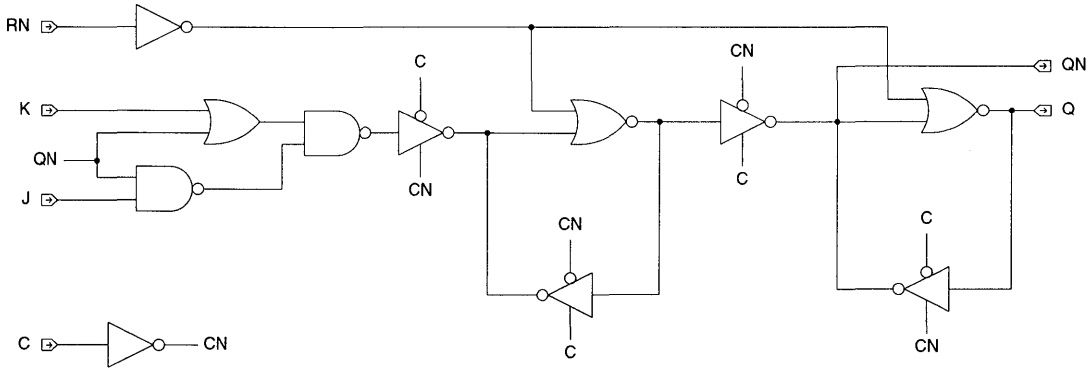
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.90 1.04	1.10 1.16	1.30 1.25	1.49 1.34	1.68 1.43
C	QN	t_{PLH} t_{PHL}	0.91 0.38	1.10 0.48	1.30 0.59	1.49 0.69	1.68 0.79
RN	Q	t_{PHL}	0.49	1.16	0.64	0.70	0.77
RN	QN	t_{PLH}	1.31	1.51	1.71	1.88	2.08

(continued on next page)

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Min C Width	High	t_w	1.06				
Min C Width	Low	t_w	0.62				
Min RN Width	Low	t_w	1.02				
Min J Setup		t_{su}	1.37				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.22				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	0.67				
Min RN Hold		t_h	0.56				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



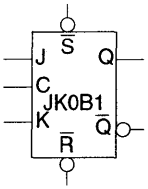
JK0B1

AMI8G 0.8 micron CMOS Gate Array

Description:

JK0B1 is a static, master-slave, JK flip-flop. SET and RESET are asynchronous and active low. Outputs are unbuffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	3.1
SN	2.0
RN	2.1

Equivalent Gates:.....12.0

Bolt Syntax:.....Q QN .JK0B1 C J K RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	12.4	nA
EQL_{pd}	41.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
C	Q	t_{PLH} t_{PHL}	0.73 1.18	0.86 1.32	0.97 1.45	1.09 1.57	1.20 1.68
C	QN	t_{PLH} t_{PHL}	0.88 0.39	1,07 0.49	1.26 0.59	1.45 0.69	1.64 0.79
RN	Q	t_{PHL}	1.32	1.46	1.60	1.69	1.81
RN	QN	t_{PLH}	1.00	1.20	1.41	1.58	1.78
SN	Q	t_{PLH}	0.32	0.43	0.54	0.65	0.75
SN	QN	t_{PHL}	0.98	1.13	1.27	1.42	1.56

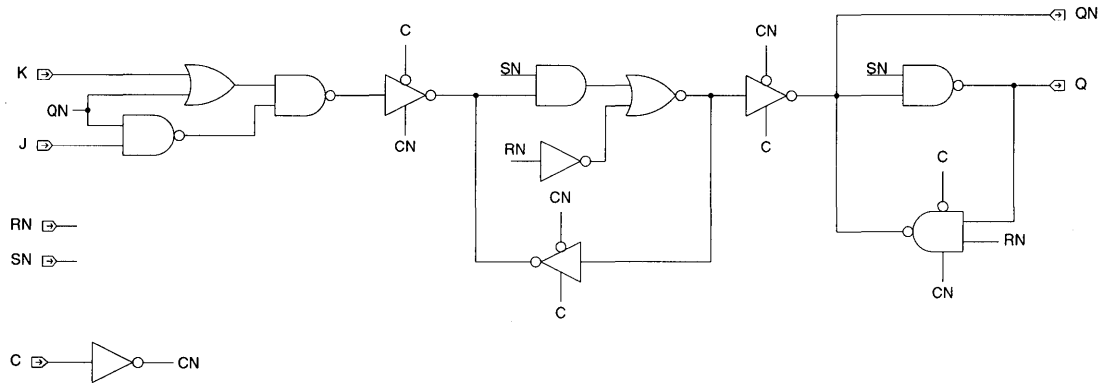
(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Min C Width	High	t_w	1.21				
Min C Width	Low	t_w	1.05				
Min RN Width	Low	t_w	0.96				
Min SN Width	Low	t_w	0.85				
Min J Setup		t_{su}	1.43				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.24				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	0.71				
Min RN Hold		t_h	0.56				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates. Loads are on measured path only; opposite output node is unloaded.

Logic Schematic



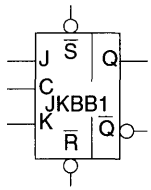
JKBB1

AMI8G 0.8 micron CMOS Gate Array

Description:

JKBB1 is a static, master-slave, JK flip-flop. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	SN	J	K	C	Q(n+1)	QN(n+1)
L	L	X	X	X	IL	IL
L	H	X	X	X	L	H
H	L	X	X	X	H	L
H	H	L	L	↑	NC	NC
H	H	L	H	↑	L	H
H	H	H	L	↑	H	L
H	H	H	H	↑	QN(n)	Q(n)

IL = Illegal NC = No Change

Pin Loading

	Equivalent Load
J	1.0
K	1.0
C	3.1
SN	2.0
RN	2.1

Equivalent Gates:.....12.0

Bolt Syntax:.....Q QN .JKBB1 C J K RN SN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	14.2	nA
EQL_{pd}	46.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
C	Q	t_{PLH} t_{PHL}	0.71 1.05	0.90 1.24	1.13 1.44	1.34 1.62	1.55 1.78
C	QN	t_{PLH} t_{PHL}	1.63 0.99	1.81 1.12	2.02 1.27	2.23 1.40	2.44 1.53
RN	Q	t_{PHL}	1.16	1.37	1.58	1.72	1.88
RN	QN	t_{PLH}	1.77	1.94	2.16	2.33	2.54
SN	Q	t_{PLH}	1.46	1.67	1.91	2.13	2.34
SN	QN	t_{PHL}	0.48	0.61	0.76	0.89	1.02

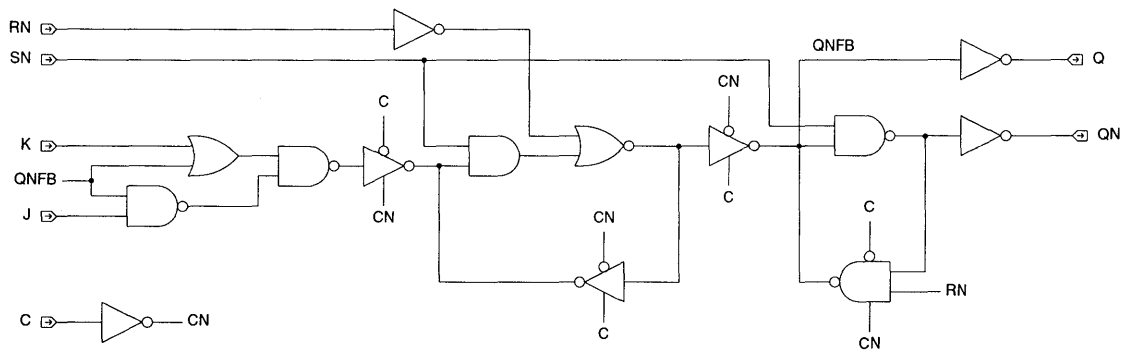
(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Min C Width	High	t_w	1.35				
Min C Width	Low	t_w	1.05				
Min RN Width	Low	t_w	1.74				
Min SN Width	Low	t_w	1.07				
Min J Setup		t_{su}	1.42				
Min J Hold		t_h	0.00				
Min K Setup		t_{su}	1.24				
Min K Hold		t_h	0.00				
Min RN Setup		t_{su}	0.71				
Min RN Hold		t_h	0.55				
Min SN Setup		t_{su}	0.28				
Min SN Hold		t_h	0.22				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

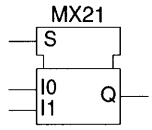
Logic Schematic



Description:

MX21 is a two-to-one digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
S	2.2

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .MX21 I0 I1 S;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	10.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

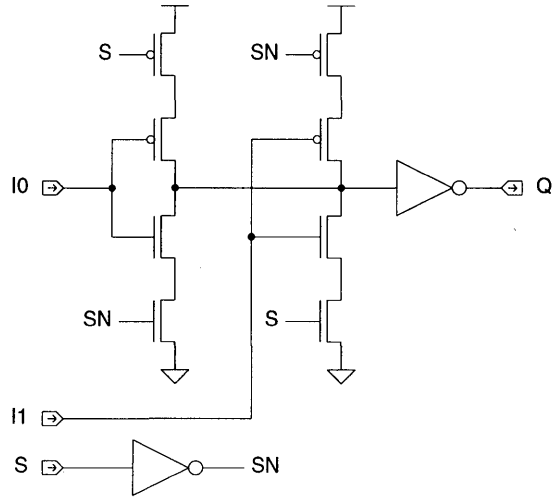
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Ix Input	Q	t_{PLH} t_{PHL}	0.54 0.59	0.72 0.75	0.94 0.93	1.15 1.09	1.36 1.24
S	Q	t_{PLH} t_{PHL}	0.73 0.80	0.91 0.96	1.12 1.12	1.34 1.27	1.55 1.41

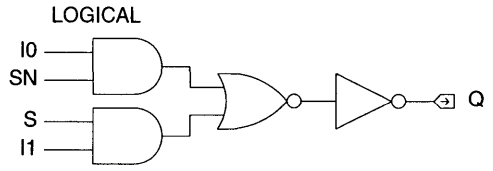
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Logic Schematic

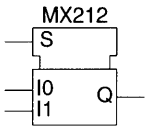




Description:

MX212 is a two-to-one digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
S	2.1

Equivalent Gates:.....4.0

Bolt Syntax:.....Q .MX212 I0 I1 S;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	13.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Ix Input	Q	t_{PLH} t_{PHL}	0.64 0.75	0.78 0.90	0.91 1.03	1.04 1.14	1.17 1.25
S	Q	t_{PLH} t_{PHL}	0.82 0.96	0.96 1.10	1.09 1.23	1.22 1.34	1.35 1.44

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

MX41

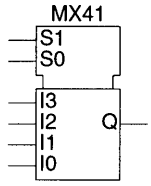
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

MX41 is a four-to-one digital multiplexer.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
I2	1.0
I3	1.0
S0	3.2
S1	3.2

Equivalent Gates:.....8.0

Bolt Syntax:.....Q .MX41 I0 I1 I2 I3 S0 S1;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.2	nA
EQL_{pd}	27.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

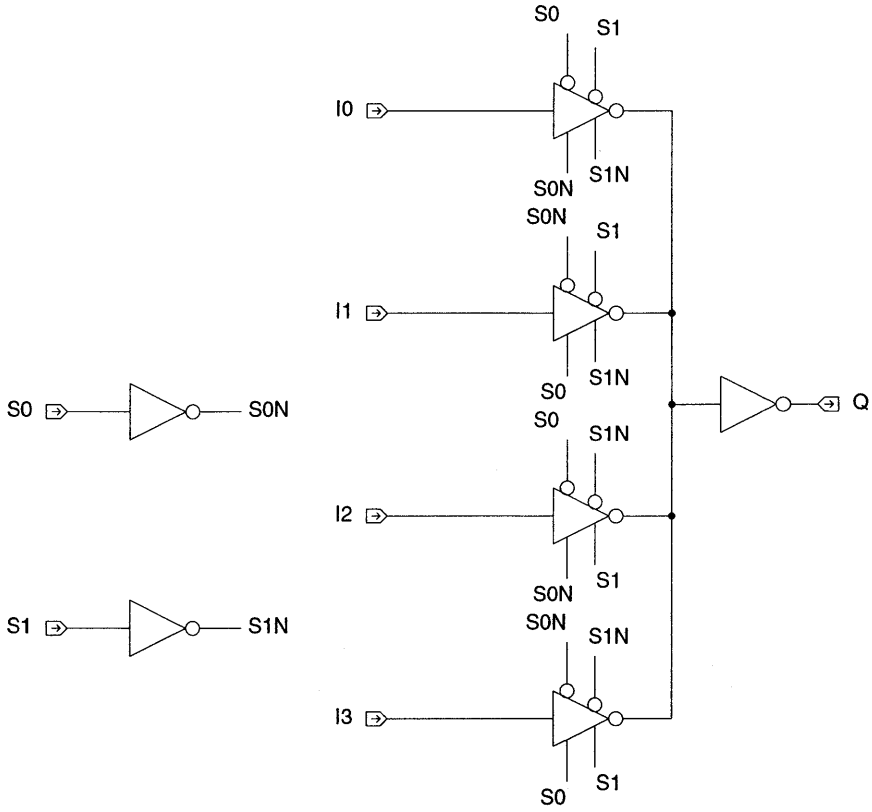
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Ix Input	Q	t_{PLH} t_{PHL}	1.13 0.92	1.33 1.20	1.55 1.47	1.77 1.70	1.98 1.90
Any Sx Input	Q	t_{PLH} t_{PHL}	1.16 1.33	1.35 1.58	1.58 1.83	1.79 2.04	2.00 2.23

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

Logic Schematic



MX81

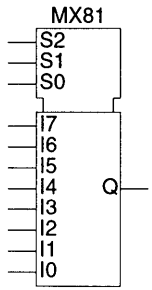
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

MX81 is an eight-to-one digital multiplexer.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
I2	1.0
I3	1.0
I4	1.0
I5	1.0
I6	1.0
I7	1.0
S0	5.4
S1	3.1
S2	2.1

Equivalent Gates:.....20.0

Bolt Syntax: .....Q .MX81 I0 I1 I2 I3 I4 I5 I6 I7 S0 S1 S2;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	15.9	nA
EQL_{pd}	58.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

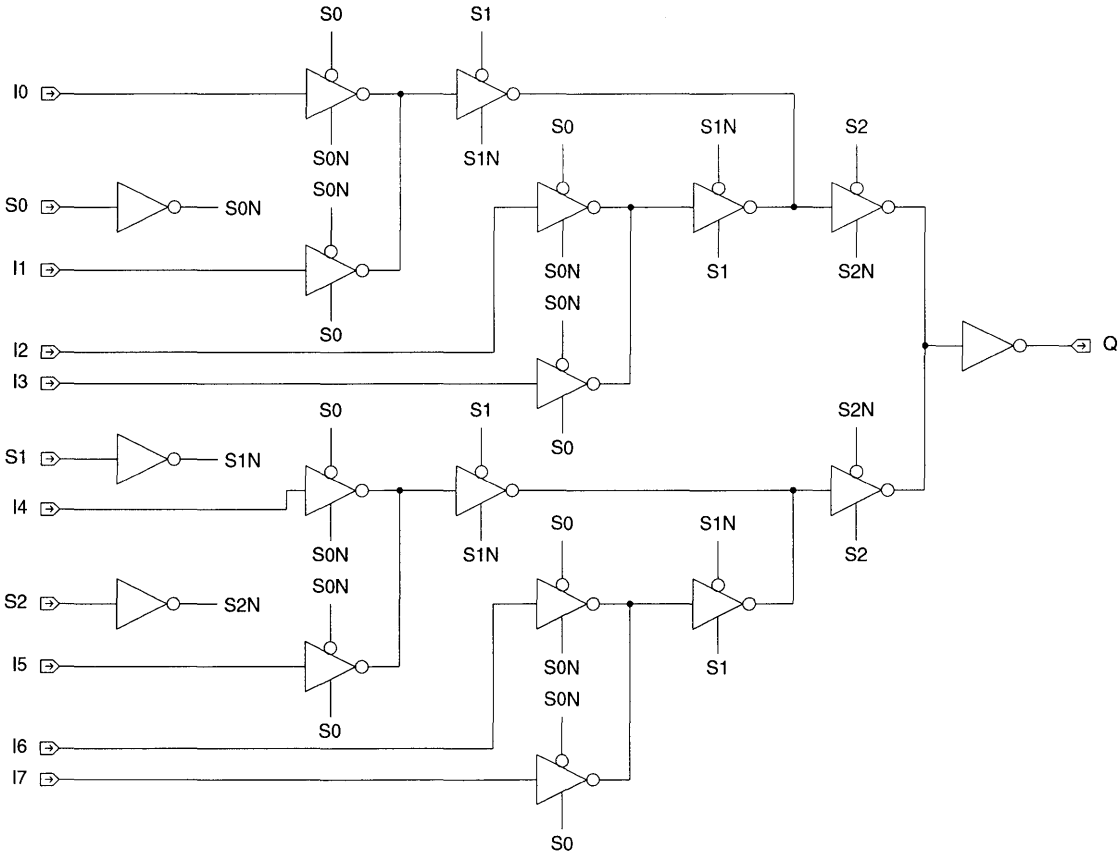
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Ix Input	Q	t_{PLH} t_{PHL}	1.46 1.41	1.63 1.58	1.84 1.75	2.04 1.90	2.25 2.04
Any Sx Input	Q	t_{PLH} t_{PHL}	1.44 1.48	1.61 1.65	1.82 1.82	2.03 1.97	2.23 2.11

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

Logic Schematic

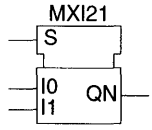


AMI8G 0.8 micron CMOS Gate Array

Description:

MXI21 is an inverting two-to-one digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	QN
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
S	2.1

Equivalent Gates:.....4.0

Bolt Syntax:.....QN .MXI21 I0 I1 S;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	13.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

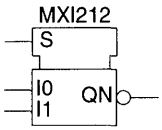
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Ix Input	QN	t_{PLH} t_{PHL}	0.82 0.72	0.90 0.79	1.01 0.87	1.11 0.94	1.21 1.01
S	QN	t_{PLH} t_{PHL}	1.02 0.90	1.10 0.97	1.21 1.05	1.31 1.13	1.41 1.19

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

MXI212 is an inverting two-to-one digital multiplexer.

Logic Symbol



Truth Table

S	I0	I1	QN
L	L	X	H
L	H	X	L
H	X	L	H
H	X	H	L

Pin Loading

	Equivalent Load
I0	1.0
I1	1.0
S	2.1

Equivalent Gates:.....6.0

Bolt Syntax:.....QN .MXI212 I0 I1 S;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	27.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Ix Input	QN	t_{PLH} t_{PHL}	0.94 0.85	1.03 0.94	1.12 1.02	1.21 1.09	1.30 1.16
S	QN	t_{PLH} t_{PHL}	1.13 1.03	1.22 1.12	1.31 1.20	1.40 1.27	1.49 1.34

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

NA21

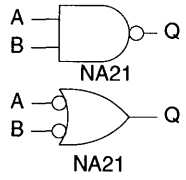
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

NA21 is a 2-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:.....1.0

Bolt Syntax:.....Q .NA21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	1.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH}	0.22	0.33	0.43	0.54	0.64
		t_{PHL}	0.19	0.29	0.39	0.49	0.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

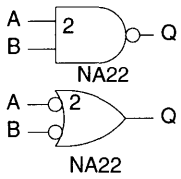
NA22

AMI8G 0.8 micron CMOS Gate Array

Description:

NA22 is a 2-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	H
H	L	H
H	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .NA22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	3.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.19	0.27	0.38	0.48	0.58
		t_{PHL}	0.16	0.24	0.34	0.45	0.55

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

NA31

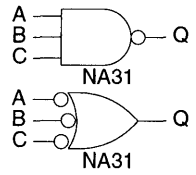
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

NA31 is a 3-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .NA31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	3.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

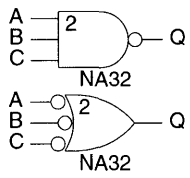
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	5	7 (max)
Any Input	Q	t_{PLH}	0.29	0.35	0.46	0.51	0.61
		t_{PHL}	0.33	0.40	0.55	0.62	0.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

NA32 is a 3-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.0
C	2.0

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .NA32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	5.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	9	11 (max)
Any Input	Q	t_{PLH}	0.25	0.30	0.38	0.46	0.52
		t_{PHL}	0.27	0.34	0.45	0.55	0.62

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

NA41

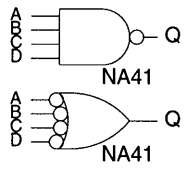
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

NA41 is a 4-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .NA41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	4.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	3	5	6 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.32 0.46	0.38 0.55	0.43 0.64	0.54 0.82	0.60 0.91

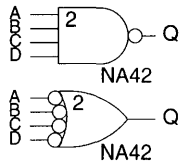
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Core Logic

Description:

NA42 is a 4-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.0
C	2.0
D	2.0

Equivalent Gates:.....4.0

Bolt Syntax:.....Q .NA42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	8.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.29 0.41	0.35 0.50	0.40 0.59	0.46 0.68	0.51 0.77

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

NA51

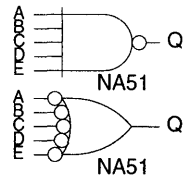
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

NA51 is a 5-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates: 3.0

Bolt Syntax: ..... Q .NA51 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	5.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	3	4	6 (max)
Any Input	Q	t_{PLH}	0.37	0.43	0.49	0.55	0.66
		t_{PHL}	0.68	0.79	0.90	1.01	1.22

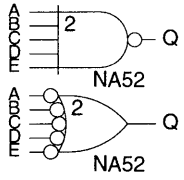
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

NA52 is a 5-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:.....4.0

Bolt Syntax: .....Q .NA52 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	11.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	6	8 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.74 1.24	0.77 1.27	0.82 1.32	0.88 1.36	0.93 1.40

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

NA61

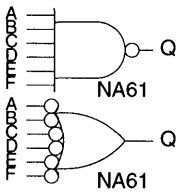
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

NA61 is a 6-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
X	X	X	X	L	X	H
X	X	X	X	X	L	H
H	H	H	H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:.....5.0

Bolt Syntax:.....Q .NA61 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.0	nA
EQL_{pd}	17.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

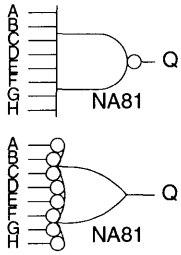
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.74 1.04	0.82 1.12	0.93 1.22	1.03 1.30	1.13 1.38

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

NA81 is an 8-input gate which performs the logical NAND function.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0
H	1.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q .NA81 A B C D E F G H;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.7	nA
EQL_{pd}	16.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.76	0.84	0.95	1.05	1.15
		t_{PHL}	1.15	1.24	1.33	1.42	1.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

NO21

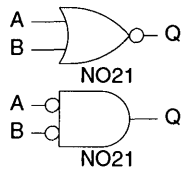
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

NO21 is a 2-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:.....1.0

Bolt Syntax:.....Q .NO21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.9	nA
EQL_{pd}	2.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.32 0.16	0.52 0.23	0.71 0.29	0.91 0.36	1.10 0.42

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

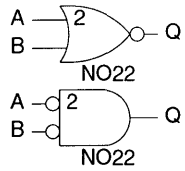
NO22

AMI8G 0.8 micron CMOS Gate Array

Description:

NO22 is a 2-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .NO22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	4.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.27 0.13	0.42 0.19	0.62 0.26	0.81 0.32	1.01 0.39

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

NO31

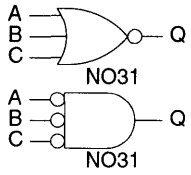
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

NO31 is a 3-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates: 2.0

Bolt Syntax:.....Q .NO31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.1	nA
EQL_{pd}	4.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	5	7 (max)
Any Input	Q	t_{PLH}	0.62	0.77	1.07	1.21	1.50
		t_{PHL}	0.18	0.22	0.29	0.33	0.40

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

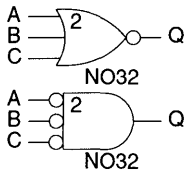
NO32

AMI8G 0.8 micron CMOS Gate Array

Description:

NO32 is a 3-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

Pin Loading

	Equivalent Load
A	2.0
B	2.0
C	2.0

Equivalent Gates: 3.0

Bolt Syntax: ..... Q .NO32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.1	nA
EQL_{pd}	7.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	9	11 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.50 0.14	0.65 0.18	0.88 0.24	1.10 0.29	1.24 0.33

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

NO41

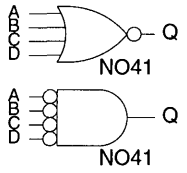
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

NO41 is a 4-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .NO41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.4	nA
EQL_{pd}	5.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	3	5	6 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.96 0.19	1.15 0.23	1.35 0.26	1.73 0.34	1.91 0.37

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

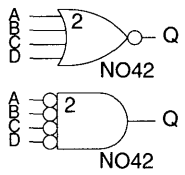
NO42

AMI8G 0.8 micron CMOS Gate Array

Description:

NO42 is a 4-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....4.0

Bolt Syntax:.....Q .NO42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	11.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH}	0.81	0.87	0.93	0.99	1.04
		t_{PHL}	0.52	0.57	0.61	0.65	0.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

NO51

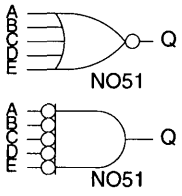
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

NO51 is a 5-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .NO51 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	8.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

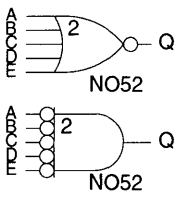
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	3	4	6 (max)
Any Input	Q	t_{PLH}	1.43	1.67	1.91	2.15	2.63
		t_{PHL}	0.20	0.24	0.28	0.31	0.38

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

NO52 is a 5-input gate which performs the logical NOR function.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	L	L	H
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:.....5.0

Bolt Syntax:.....Q .NO52 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	14.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	6	8 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.20 0.58	1.23 0.60	1.29 0.65	1.35 0.69	1.41 0.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ON11

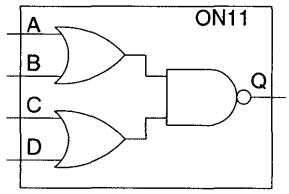
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ON11 is an OR-NAND circuit consisting of two 2-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	L	H
All other combinations				L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .ON11 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	5.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.58 0.37	0.78 0.49	0.98 0.59	1.17 0.70	1.37 0.81

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

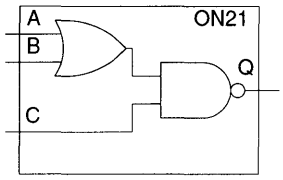
ON21

AMI8G 0.8 micron CMOS Gate Array

Description:

ON21 is an OR-NAND circuit consisting of one 2-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	Q
L	L	X	H
X	X	L	H
All other combinations			L

Pin Loading

	Equivalent Load
A	1.0
B	1.6
C	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .ON21 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	4.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	3	5	7	9 (max)
Any Input	Q	t_{PLH}	0.26	0.40	0.54	0.68	0.82
		t_{PHL}	0.28	0.41	0.54	0.67	0.79

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ON31

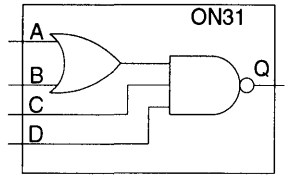
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ON31 is an OR-NAND circuit consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
All other combinations				L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .ON31 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	4.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

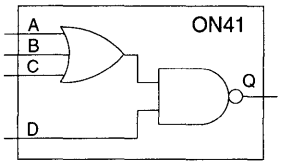
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.40 0.43	0.50 0.51	0.69 0.65	0.79 0.72	0.98 0.86

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

ON41 is an OR-NAND circuit consisting of one 3-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	X	H
X	X	X	L	H
All other combinations				L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .ON41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	10.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	5	7	9 (max)
Any Input	Q	t_{PLH}	1.05	1.16	1.26	1.37	1.47
		t_{PHL}	0.59	0.69	0.80	0.90	1.00

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ON51

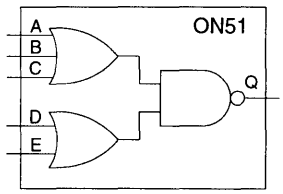
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ON51 is an OR-NAND circuit consisting of one 3-input OR gate and one 2-input NAND gate into a 2-input NOR gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates:.....4.0

Bolt Syntax:.....Q .ON51 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	13.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

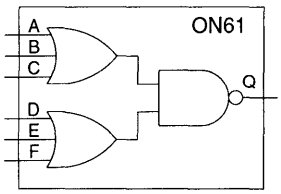
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	1.05 0.66	1.20 0.79	1.41 0.94	1.61 1.07	1.81 1.20

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

ON61 is an OR-NAND circuit consisting of two 3-input OR gates into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	L	H
All other combinations						L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:.....5.0

Bolt Syntax:.....Q .ON61 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	17.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	1.09	1.26	1.43	1.61	1.78
		t_{PHL}	0.73	0.89	1.04	1.16	1.29

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ON71

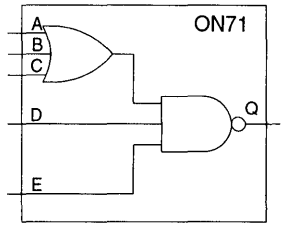
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ON71 is an OR-NAND circuit consisting of one 3-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates: 4.0

Bolt Syntax: ..... Q .ON71 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	11.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	5	7 (max)
Any Input	Q	t_{PLH}	1.09	1.14	1.25	1.30	1.40
		t_{PHL}	0.68	0.75	0.90	0.97	1.11

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

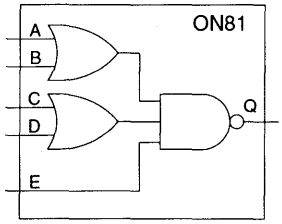
ON81

AMI8G 0.8 micron CMOS Gate Array

Description:

ON81 is an OR-NAND circuit consisting of two 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	Q
L	L	X	X	X	H
X	X	L	L	X	H
X	X	X	X	L	H
All other combinations					L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Equivalent Gates: 5.0

Bolt Syntax: ..... Q .ON81 A B C D E;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.65	0.81	1.02	1.23	1.43
		t_{PHL}	0.87	0.99	1.11	1.21	1.30

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ON91

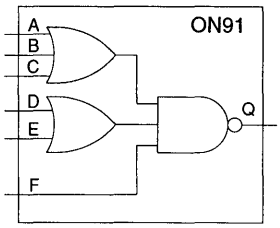
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ON91 is an OR-NAND circuit consisting of one 3-input OR gate and one 2-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	L	X	X	X	H
X	X	X	L	L	X	H
X	X	X	X	X	L	H
All other combinations						L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.1
E	1.0
F	1.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q .ON91 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	19.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

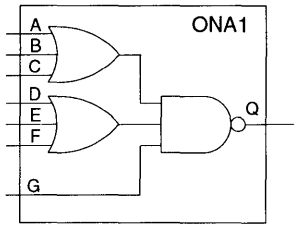
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.65	0.81	1.02	1.23	1.43
		t_{PHL}	0.79	0.91	1.03	1.13	1.22

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

ONA1 is an OR-NAND circuit consisting of two 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	L	X	H
X	X	X	X	X	X	L	H
All other combinations							L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0

Equivalent Gates:.....6.0

Bolt Syntax: .....Q .ONA1 A B C D E F G;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	7.1	nA
EQL_{pd}	21.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	2	4	5	7 (max)
Any Input	Q	t_{PLH}	1.04	1.07	1.13	1.15	1.20
		t_{PHL}	0.85	0.92	1.07	1.14	1.28

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

ONB1

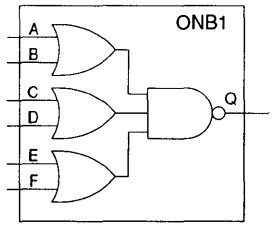
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

ONB1 is an OR-NAND circuit consisting of three 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	Q
L	L	X	X	X	X	H
X	X	L	L	X	X	H
X	X	X	X	L	L	H
All other combinations						L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q .ONB1 A B C D E F;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.0	nA
EQL_{pd}	20.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	5	7 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.73 0.69	0.79 0.76	0.90 0.90	0.95 0.97	1.05 1.11

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

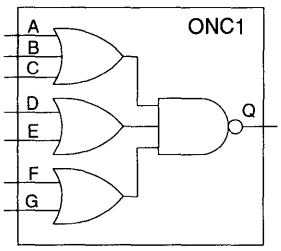
ONC1

AMI8G 0.8 micron CMOS Gate Array

Description:

ONC1 is an OR-NAND circuit consisting of one 3-input OR gate and two 2-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	X	X	H
X	X	X	X	X	L	L	H
All other combinations							L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q .ONC1 A B C D E F G;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	20.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	1.07	1.24	1.42	1.59	1.77
		t_{PHL}	1.07	1.27	1.44	1.58	1.72

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OND1

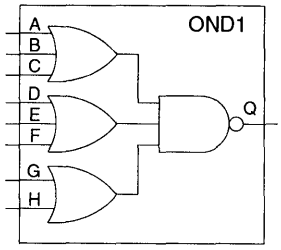
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OND1 is an OR-NAND circuit consisting of two 3-input OR gates and one 2-input OR gate into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	Q
L	L	L	X	X	X	X	X	H
X	X	X	L	L	L	X	X	H
X	X	X	X	X	X	L	L	H
All other combinations								L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0
H	1.0

Equivalent Gates:.....6.0

Bolt Syntax:.....Q .OND1 A B C D E F G H;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.4	nA
EQL_{pd}	21.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	1.08	1.24	1.44	1.64	1.85
		t_{PHL}	0.90	1.07	1.24	1.40	1.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

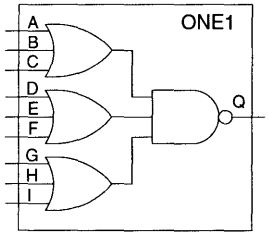
ONE1

AMI8G 0.8 micron CMOS Gate Array

Description:

ONE1 is an OR-NAND circuit consisting of three 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
L	L	L	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	L	L	L	H
All other combinations									L

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0
G	1.0
H	1.0
I	1.0

Equivalent Gates:.....7.0

Bolt Syntax:.....Q .ONE1 A B C D E F G H I;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	27.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	7	14	21	28 (max)
Any Input	Q	t_{PLH}	1.23	1.39	1.57	1.75	1.93
		t_{PHL}	1.19	1.38	1.55	1.70	1.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OR21

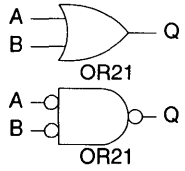
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OR21 is a 2-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .OR21 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	4.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

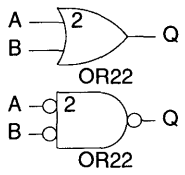
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.34 0.49	0.50 0.62	0.71 0.77	0.92 0.91	1.12 1.04

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

OR22 is a 2-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	Q
L	L	L
L	H	H
H	L	H
H	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .OR22 A B;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	5.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.35 0.56	0.51 0.72	0.70 0.87	0.88 1.00	1.05 1.12

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OR31

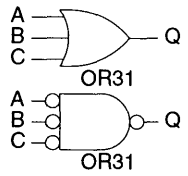
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OR31 is a 3-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:.....2.0

Bolt Syntax:.....Q .OR31 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.8	nA
EQL_{pd}	6.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.39	0.55	0.77	0.98	1.19
		t_{PHL}	0.81	0.98	1.16	1.32	1.47

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

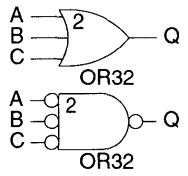
OR32

AMI8G 0.8 micron CMOS Gate Array

Description:

OR32 is a 3-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .OR32 A B C;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.7	nA
EQL_{pd}	9.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.40 0.95	0.58 1.14	0.76 1.31	0.95 1.46	1.13 1.60

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OR41

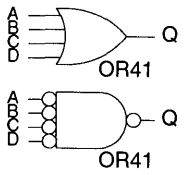
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OR41 is a 4-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....3.0

Bolt Syntax:.....Q .OR41 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.5	nA
EQL_{pd}	8.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
Any Input	Q	t_{PLH}	0.35	0.51	0.72	0.93	1.13
		t_{PHL}	0.56	0.74	0.95	1.16	1.36

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

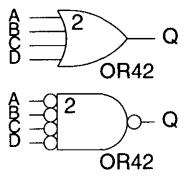
OR42

AMI8G 0.8 micron CMOS Gate Array

Description:

OR42 is a 4-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

Pin Loading

	Equivalent Load
A	1.0
B	1.0
C	1.0
D	1.0

Equivalent Gates:.....4.0

Bolt Syntax:.....Q .OR42 A B C D;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.3	nA
EQL_{pd}	12.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	7	14	21	28 (max)
Any Input	Q	t_{PLH} t_{PHL}	0.36 0.64	0.53 0.85	0.71 1.05	0.89 1.23	1.06 1.42

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

TD08

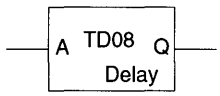
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

TD08 is a non-inverting time delay.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	1.0

Equivalent Gates:.....11.0

Bolt Syntax:.....Q .TD08 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	6.9	nA
EQL_{pd}	55.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	6	11	17	22 (max)
A	Q	t_{PLH}	10.04	10.25	10.41	10.58	10.72
		t_{PHL}	10.76	11.00	11.20	11.41	11.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

SECTION 4
PAD LOGIC

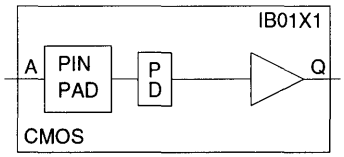
IB01X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IB01X1 is a non-inverting, CMOS-level input buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax: .....Q .IB01X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.5	nA
EQL_{pd}	48.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
A	Q	t_{PLH}	0.71	0.89	1.03	1.17	1.31
		t_{PHL}	0.91	1.09	1.23	1.37	1.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IB03X1

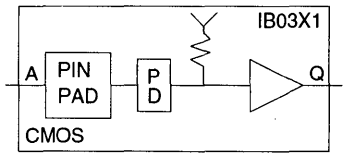
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IB03X1 is a non-inverting, CMOS-level input buffer pad with pull-up.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax: .....Q .IB03X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.0	nA
EQL_{pd}	58.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

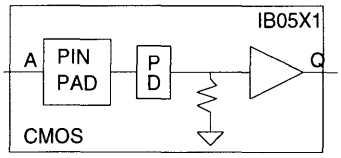
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
A	Q	t_{PLH} t_{PHL}	0.71 0.90	0.89 1.09	1.03 1.23	1.17 1.37	1.31 1.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

IB05X1 is a non-inverting, CMOS-level input buffer pad with pull-down.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax: .....Q .IB05X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.5	nA
EQL_{pd}	60.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
A	Q	t_{PLH}	0.71	0.89	1.03	1.17	1.31
		t_{PHL}	0.91	1.09	1.23	1.37	1.50

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IB07X1

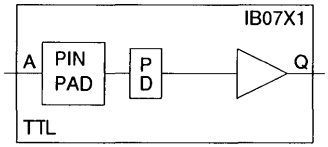
AMI SEMICONDUCTORS
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IB07X1 is a non-inverting, TTL-level input buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax: .....Q .IB07X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.9	nA
EQL_{pd}	49.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

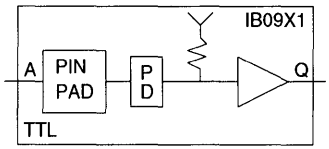
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
A	Q	t_{PLH}	0.83	1.01	1.01	1.28	1.42
		t_{PHL}	1.18	1.40	1.40	1.73	1.88

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

IB09X1 is a non-inverting, TTL-level input buffer pad with pull-up.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax: .....Q .IB09X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.4	nA
EQL_{pd}	59.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
A	Q	t_{PLH}	0.84	1.01	1.15	1.29	1.29
		t_{PHL}	1.18	1.41	1.58	1.73	1.88

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IB0BX1

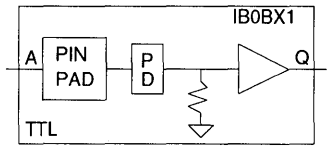
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IB0BX1 is a non-inverting, TTL-level input buffer pad with pull-down.

Logic Symbol



Truth Table

A	Q
L	L
H	H
UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	187.8

Bolt Syntax: .....Q .IB0BX1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.9	nA
EQL_{pd}	61.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

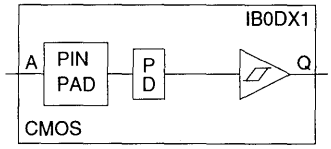
Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
A	Q	t_{PLH}	0.84	1.01	1.15	1.29	1.43
		t_{PHL}	1.19	1.41	1.58	1.73	1.88

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

IB0DX1 is a non-inverting, CMOS-level Schmitt trigger input buffer pad with voltage hysteresis.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	217.4

Bolt Syntax: .....Q .IB0DX1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.4	nA
EQL_{pd}	51.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

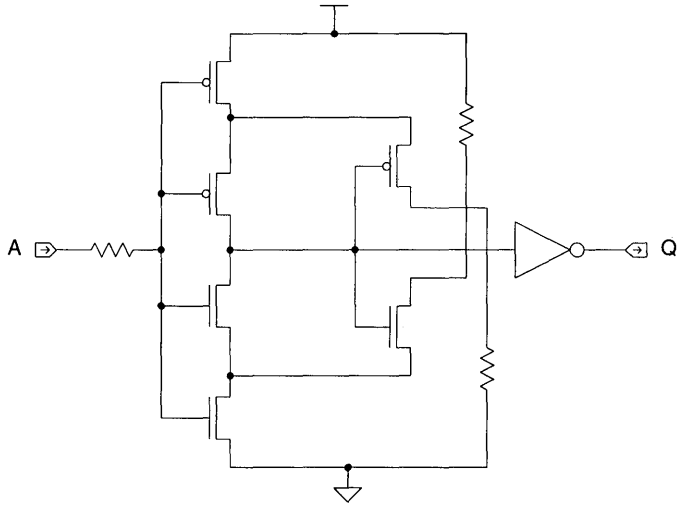
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
A	Q	t_{PLH}	2.64	2.87	3.06	3.23	3.39
		t_{PHL}	1.96	2.18	2.35	2.51	2.66

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Logic Schematic



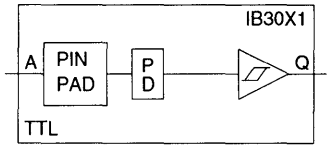
IB30X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IB30X1 is a non-inverting, TTL-level Schmitt trigger input buffer pad with voltage hysteresis.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	217.4

Bolt Syntax: .....Q .IB30X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.9	nA
EQL_{pd}	54.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
A	Q	t_{PLH}	1.35	1.53	1.68	1.82	1.96
		t_{PHL}	2.88	3.20	3.44	3.65	3.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IBF1X5

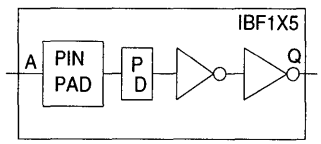
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IBF1X5 is a non-inverting, CMOS-level input clock-driver pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	117.4

Bolt Syntax: .....Q .IBF1X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.6	nA
EQL_{pd}	185.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	86	172	257	343 (max)
A	Q	t_{PLH}	1.18	1.37	1.53	1.68	1.84
		t_{PHL}	1.23	1.40	1.54	1.66	1.79

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

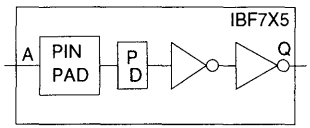
IBF7X5

AMI8G 0.8 micron CMOS Gate Array

Description:

IBF7X5 is a non-inverting, TTL-level input clock-driver pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	117.4

Bolt Syntax: .....Q .IBF7X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.9	nA
EQL_{pd}	189.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	86	172	257	343 (max)
A	Q	t_{PLH}	1.37	1.54	1.70	1.85	2.00
		t_{PHL}	1.24	1.42	1.58	1.72	1.84

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IIF1X5

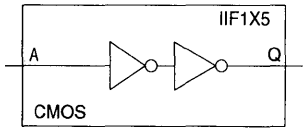
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IIF1X5 is a non-inverting, second ring, CMOS-level input clock-driver.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	5.7

Bolt Syntax: .....Q .IIF1X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.6	nA
EQL_{pd}	171.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	86	172	257	343 (max)
A	Q	t_{PLH}	0.69	0.87	1.03	1.19	1.34
		t_{PHL}	0.68	0.84	0.98	1.11	1.23

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

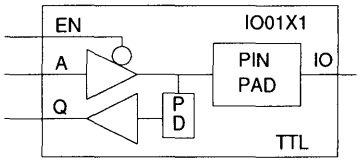
IO01X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IO01X1 is a 1 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax: .....IO Q .IO01X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.7	nA
EQL_{pd}	269.0	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.70	0.85	0.98	1.11	1.24
		t_{PHL}	1.00	1.21	1.38	1.53	1.67

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH}	3.01	4.21	5.41	7.20	10.19
		t_{PHL}	4.59	6.35	8.11	10.76	15.18
EN	IO	t_{HZ}	0.95				
		t_{LZ}	0.60				
		t_{ZH}	3.15	4.35	5.55	7.34	10.33
		t_{ZL}	4.62	6.37	8.14	10.79	15.20

IO01X2

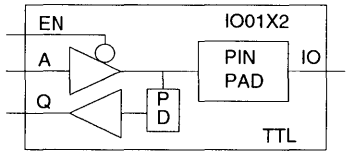
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO01X2 is a 2 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax: .....IO Q .IO01X2 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.7	nA
EQL_{pd}	271.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.69	0.85	0.98	1.11	1.25
		t_{PHL}	1.02	1.24	1.40	1.55	1.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH}	1.99	4.09	5.58	7.08	10.06
		t_{PHL}	4.59	10.78	15.20	19.61	28.45
EN	IO	t_{HZ}	1.30				
		t_{LZ}	0.60				
		t_{ZH}	2.15	4.24	5.74	7.23	10.21
		t_{ZL}	4.60	10.79	15.21	19.62	28.46

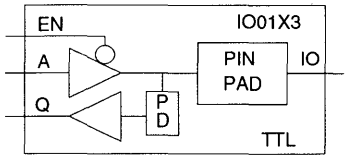
IO01X3

AMI8G 0.8 micron CMOS Gate Array

Description:

IO01X3 is a 4 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.4
IO	199.5

Bolt Syntax: .....IO Q .IO01X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.4	nA
EQL_{pd}	284.5	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.69	0.85	0.98	1.11	1.24
		t_{PHL}	1.02	1.22	1.39	1.54	1.68

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
A	IO	t_{PLH}	1.35	2.43	3.92	6.91	9.89
		t_{PHL}	2.65	5.75	10.16	19.01	27.83
EN	IO	t_{HZ}	1.39				
		t_{LZ}	0.61				
		t_{ZH}	1.58	2.65	4.15	7.13	10.12
		t_{ZL}	2.64	5.75	10.17	19.02	27.84

IO01X5

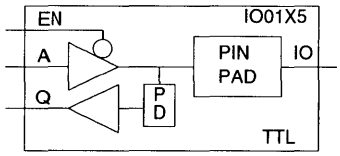
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO01X5 is an 8 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	9.5
EN	6.5
IO	199.9

Bolt Syntax: .....IO Q .IO01X5 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	61.8	nA
EQL_{pd}	313.3	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.70	0.85	0.98	1.11	1.25
		t_{PHL}	1.02	1.23	1.40	1.55	1.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.08	1.70	2.48	3.98	5.47
		t_{PHL}	1.87	3.46	5.68	10.12	14.52
EN	IO	t_{HZ}	1.72				
		t_{LZ}	0.68				
		t_{ZH}	1.43	2.06	2.83	4.34	5.83
		t_{ZL}	1.85	3.47	5.70	10.14	14.54

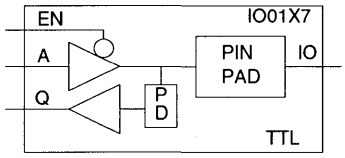
IO01X7

AMI8G 0.8 micron CMOS Gate Array

Description:

IO01X7 is a 16 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	13.6
EN	9.8
IO	200.1

Bolt Syntax: .....IO Q .IO01X7 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	68.3	nA
EQL_{pd}	348.8	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.68	0.83	0.97	1.10	1.23
		t_{PHL}	1.00	1.20	1.36	1.51	1.64

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

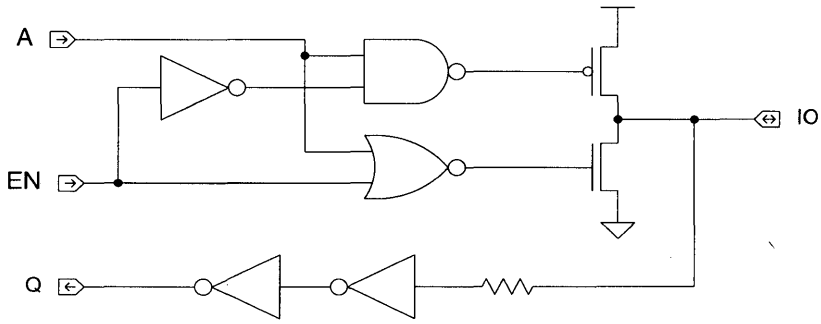
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.00	1.47	2.02	3.05	4.05
		t_{PHL}	1.38	2.22	3.36	5.59	7.80
EN	IO	t_{HZ}	1.79				
		t_{LZ}	0.98				
		t_{ZH}	1.25	1.73	2.29	3.31	4.32
		t_{ZL}	1.34	2.22	3.38	5.61	7.83

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

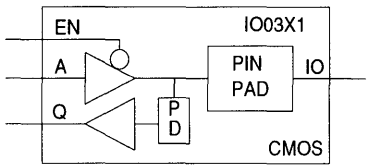
Logic Schematic



Description:

IO03X1 is a 1 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax: ..... IO Q .IO03X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	267.8	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.02	1.16	1.29
		t_{PHL}	0.91	1.08	1.22	1.35	1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH}	5.08	7.28	9.47	12.75	18.23
		t_{PHL}	3.19	4.30	5.41	7.07	9.84
EN	IO	t_{HZ}	0.95				
		t_{LZ}	0.60				
		t_{ZH}	5.23	7.42	9.61	12.89	18.37
		t_{ZL}	3.22	4.39	5.44	7.10	9.87

IO03X2

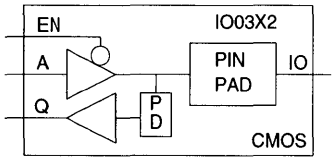
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO03X2 is a 2 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax: .....IO Q .IO03X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	270.4	Eq-load

See page 2-13 for power equation.

Pad Logic

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.02	1.16	1.29
		t_{PHL}	0.91	1.08	1.22	1.35	1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

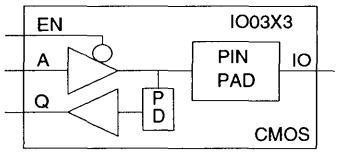
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	75	100	150 (max)
A	IO	t_{PLH}	3.05	6.88	9.62	12.35	17.82
		t_{PHL}	3.21	7.09	9.86	12.63	18.17
EN	IO	t_{HZ}	1.30				
		t_{LZ}	0.60				
		t_{ZH}	3.20	7.04	9.77	12.50	17.97
		t_{ZL}	3.22	7.10	9.87	12.64	18.18

Description:

IO03X3 is a 4 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.3
IO	199.5

Bolt Syntax: ..... IO Q .IO03X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.9	nA
EQL_{pd}	283.3	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.03	1.16	1.29
		t_{PHL}	0.91	1.09	1.23	1.35	1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

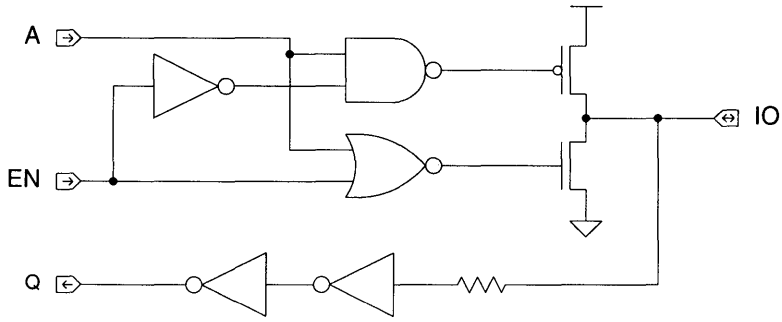
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.91	3.84	6.58	12.05	17.51
		t_{PHL}	1.95	3.90	6.66	12.20	17.74
EN	IO	t_{HZ}	1.40				
		t_{LZ}	0.59				
		t_{ZH}	2.13	4.07	6.80	12.27	17.74
		t_{ZL}	1.94	3.90	6.67	12.21	17.75

(continued on next page)

AMI8G 0.8 micron CMOS Gate Array

Logic Schematic



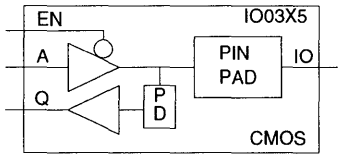
IO03X5

AMI8G 0.8 micron CMOS Gate Array

Description:

IO03X5 is an 8 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	9.5
EN	6.5
IO	200.0

Bolt Syntax: .....IO Q .IO03X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	62.4	nA
EQL_{pd}	312.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.75	0.92	1.06	1.20	1.33
		t_{PHL}	0.94	1.12	1.26	1.39	1.52

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
A	IO	t_{PLH}	1.42	2.45	3.83	6.58	9.31
		t_{PHL}	1.49	2.52	3.92	6.69	9.46
EN	IO	t_{HZ}	1.73				
		t_{LZ}	0.68				
		t_{ZH}	1.80	2.83	4.22	6.96	9.69
		t_{ZL}	1.48	2.52	3.93	6.71	9.48

IO03X7

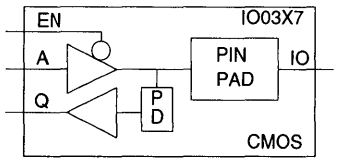
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO03X7 is a 16 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	13.6
EN	9.8
IO	200.1

Bolt Syntax: .....IO Q .IO03X7 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	68.9	nA
EQL_{pd}	347.8	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.03	1.18	1.32
		t_{PHL}	0.95	1.12	1.26	1.39	1.52

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
A	IO	t_{PLH}	1.26	2.00	2.96	4.80	6.62
		t_{PHL}	1.16	1.72	2.46	3.86	5.25
EN	IO	t_{HZ}	1.79				
		t_{LZ}	0.98				
		t_{ZH}	1.51	2.27	3.22	5.07	6.89
		t_{ZL}	1.12	1.72	2.47	3.89	5.28

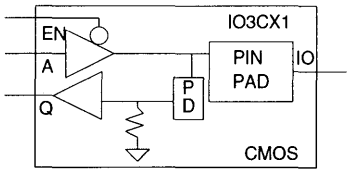
IO3CX1

AMI8G 0.8 micron CMOS Gate Array

Description:

IO3CX1 is a 1 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.1
IO	199.4

Bolt Syntax: .....IO Q .IO3CX1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	280.5	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.02	1.16	1.29
		t_{PHL}	0.91	1.08	1.22	1.35	1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH}	5.16	7.36	9.56	12.85	18.35
		t_{PHL}	3.19	4.29	5.39	7.03	9.78
EN	IO	t_{HZ}	0.96				
		t_{LZ}	0.60				
		t_{ZH}	5.30	7.50	9.69	12.99	18.49
		t_{ZL}	3.22	4.33	5.43	7.09	9.85

IO3CX2

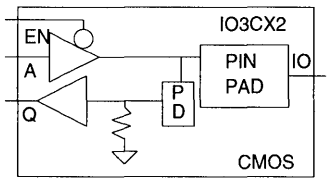
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO3CX2 is a 2 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.9
EN	3.1
IO	199.4

Bolt Syntax: .....IO Q .IO3CX2 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	283.1	Eq-load

See page 2-13 for power equation..

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.02	1.16	1.29
		t_{PHL}	0.91	1.08	1.22	1.35	1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	75	100	150 (max)
A	IO	t_{PLH}	3.08	6.93	9.67	12.41	17.89
		t_{PHL}	3.21	7.07	9.82	12.58	18.08
EN	IO	t_{HZ}	1.31				
		t_{LZ}	0.60				
		t_{ZH}	3.23	7.08	9.82	12.56	18.03
		t_{ZL}	3.22	7.09	9.85	12.61	18.14

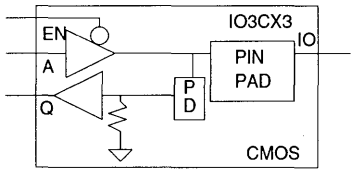
IO3CX3

AMI8G 0.8 micron CMOS Gate Array

Description:

IO3CX3 is a 4 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.4
IO	199.5

Bolt Syntax: .....IO Q .IO3CX3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.9	nA
EQL_{pd}	298.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.03	1.16	1.29
		t_{PHL}	0.91	1.09	1.22	1.35	1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.93	3.87	6.61	12.09	17.55
		t_{PHL}	1.96	3.89	6.65	12.18	17.70
EN	IO	t_{HZ}	1.40				
		t_{LZ}	0.59				
		t_{ZH}	2.16	4.09	6.83	12.31	17.78
		t_{ZL}	1.94	3.90	6.67	12.20	17.73

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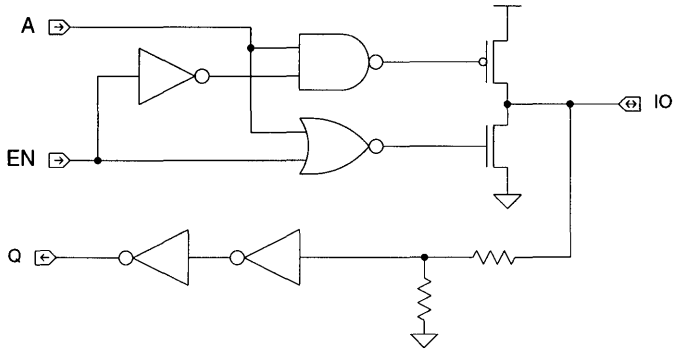
AMI8G 0.8 micron CMOS Gate Array

Logic Schematic



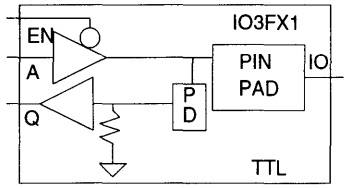
IO3FX1

AMI8G 0.8 micron CMOS Gate Array

Description:

IO3FX1 is a 1 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.9
EN	3.1
IO	199.4

Bolt Syntax: .....IO Q .IO3FX1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.7	nA
EQL_{pd}	282.7	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.70	0.85	0.99	1.12	1.25
		t_{PHL}	1.02	1.23	1.40	1.55	1.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH}	3.06	4.26	5.45	7.25	10.25
		t_{PHL}	4.58	6.34	8.09	10.73	15.12
EN	IO	t_{HZ}	0.96				
		t_{LZ}	0.60				
		t_{ZH}	3.19	4.39	5.59	7.39	10.39
		t_{ZL}	4.62	6.38	8.14	10.78	15.19

IO3FX2

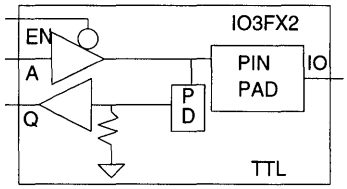
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO3FX2 is a 2 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.9
EN	3.1
IO	199.4

Bolt Syntax: .....IO Q .IO3FX2 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.7	nA
EQL_{pd}	285.3	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.70	0.86	0.99	1.12	1.25
		t_{PHL}	1.03	1.24	1.41	1.56	1.70

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

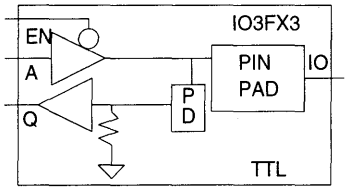
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH}	2.02	4.12	5.61	7.11	10.10
		t_{PHL}	4.61	10.76	15.16	19.55	28.36
EN	IO	t_{HZ}	1.30				
		t_{LZ}	0.60				
		t_{ZH}	2.17	4.27	5.76	7.26	10.25
		t_{ZL}	4.62	10.78	15.19	19.59	28.41

Description:

IO3FX3 is a 4 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.5
IO	199.5

Bolt Syntax: .....IO Q .IO3FX3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.4	nA
EQL_{pd}	298.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.70	0.86	0.99	1.12	1.25
		t_{PHL}	1.04	1.25	1.42	1.56	1.70

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.38	2.46	3.96	6.94	9.93
		t_{PHL}	2.66	5.75	10.15	18.98	27.78
EN	IO	t_{HZ}	1.40				
		t_{LZ}	0.63				
		t_{ZH}	1.60	2.68	4.18	7.17	10.15
		t_{ZL}	2.65	5.75	10.17	19.00	27.81

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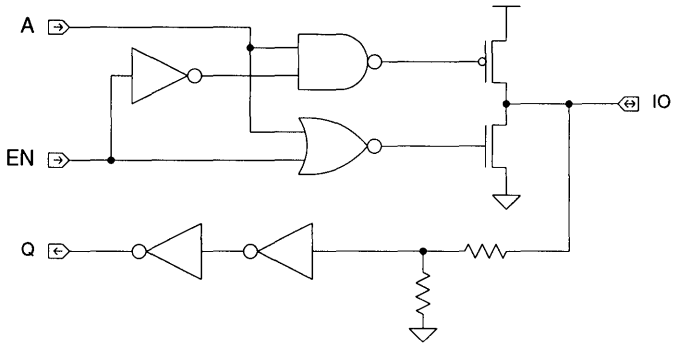
AMI8G 0.8 micron CMOS Gate Array

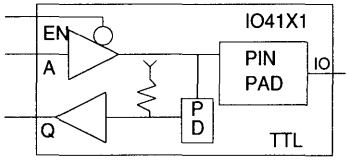
Logic Schematic



Description:

IO41X1 is a 1 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax: .....IO Q .IO41X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	279.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.70	0.85	0.98	1.11	1.24
		t_{PHL}	1.00	1.21	1.38	1.53	1.67

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH}	3.00	4.18	5.37	7.14	10.10
		t_{PHL}	4.61	6.37	8.14	10.80	15.24
EN	IO	t_{HZ}	0.96				
		t_{LZ}	0.60				
		t_{ZH}	3.15	4.34	5.52	7.31	10.28
		t_{ZL}	4.64	6.40	8.17	10.83	15.26

IO41X2

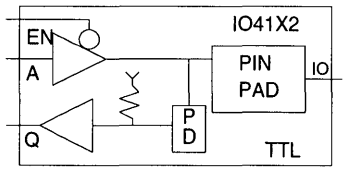
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO41X2 is a 2 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.0
IO	199.4

Bolt Syntax: .....IO Q .IO41X2 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.2	nA
EQL_{pd}	282.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.69	0.85	0.98	1.11	1.25
		t_{PHL}	1.02	1.23	1.40	1.55	1.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

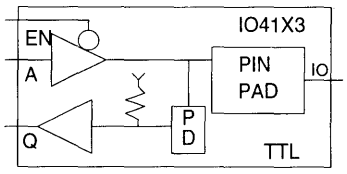
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH}	1.99	4.07	5.56	7.04	10.00
		t_{PHL}	4.62	10.82	15.25	19.67	28.53
EN	IO	t_{HZ}	1.30				
		t_{LZ}	0.60				
		t_{ZH}	2.15	4.24	5.73	7.22	10.19
		t_{ZL}	4.62	10.83	15.26	19.69	28.55

Description:

IO41X3 is a 4 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.4
IO	199.5

Bolt Syntax: ..... IO Q .IO41X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.9	nA
EQL_{pd}	295.1	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.69	0.85	0.98	1.11	1.24
		t_{PHL}	1.02	1.22	1.39	1.54	1.68

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.36	2.43	3.92	6.89	9.86
		t_{PHL}	2.67	5.77	10.18	19.03	27.88
EN	IO	t_{HZ}	1.40				
		t_{LZ}	0.61				
		t_{ZH}	1.58	2.65	4.15	7.13	10.11
		t_{ZL}	2.65	5.77	10.19	19.04	27.89

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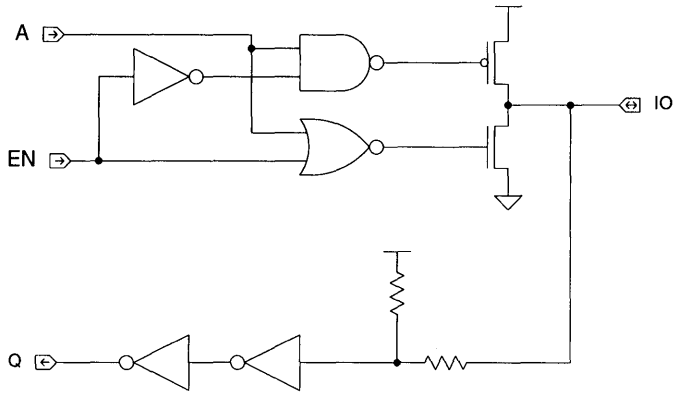
AMI8G 0.8 micron CMOS Gate Array

Logic Schematic



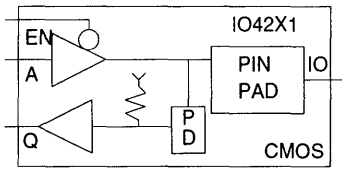
IO42X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IO42X1 is a 1 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.1
IO	199.4

Bolt Syntax: .....IO Q .IO42X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.7	nA
EQL_{pd}	278.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.02	1.16	1.29
		t_{PHL}	0.91	1.08	1.22	1.35	1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH}	5.07	7.24	9.42	12.68	18.11
		t_{PHL}	3.21	4.32	5.43	7.10	9.87
EN	IO	t_{HZ}	0.96				
		t_{LZ}	0.60				
		t_{ZH}	5.22	7.39	9.57	12.84	18.29
		t_{ZL}	3.24	4.35	5.46	7.13	9.90

IO42X2

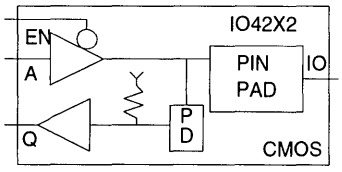
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO42X2 is a 2 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.1
IO	199.4

Bolt Syntax: .....IO Q .IO42X2 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.7	nA
EQL_{pd}	281.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.02	1.16	1.29
		t_{PHL}	0.91	1.08	1.22	1.35	1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH}	3.05	6.87	9.59	12.31	17.75
		t_{PHL}	3.23	7.12	9.89	12.66	18.21
EN	IO	t_{HZ}	1.31				
		t_{LZ}	0.60				
		t_{ZH}	3.20	7.03	9.76	12.48	17.94
		t_{ZL}	3.24	7.13	9.90	12.67	18.22

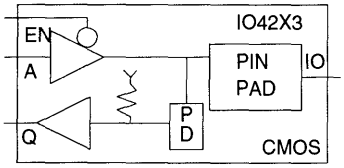
IO42X3

AMI8G 0.8 micron CMOS Gate Array

Description:

IO42X3 is a 4 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.3
IO	199.5

Bolt Syntax: ..... IO Q .IO42X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	57.5	nA
EQL_{pd}	294.0	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.72	0.89	1.03	1.16	1.29
		t_{PHL}	0.91	1.08	1.22	1.35	1.48

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.91	3.84	6.57	12.02	17.48
		t_{PHL}	1.96	3.91	6.68	12.22	17.76
EN	IO	t_{HZ}	1.40				
		t_{LZ}	0.59				
		t_{ZH}	2.14	4.07	6.80	12.26	17.72
		t_{ZL}	1.95	3.91	6.68	12.23	17.77

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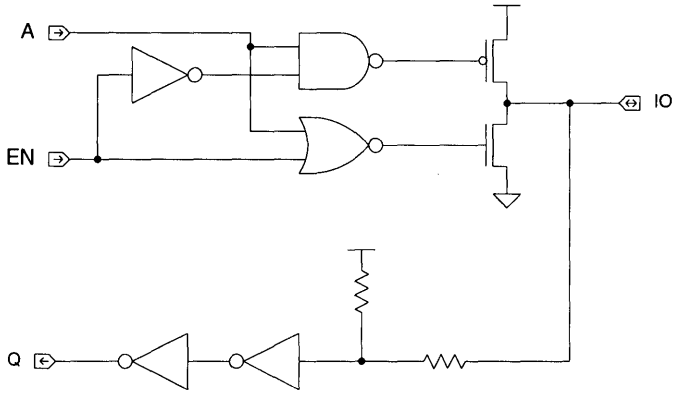
AMI8G 0.8 micron CMOS Gate Array

Logic Schematic



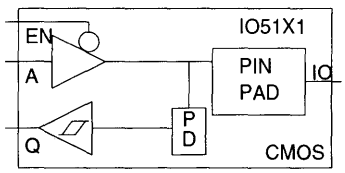
IO51X1

AMI8G 0.8 micron CMOS Gate Array

Description:

IO51X1 is a 1 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.1
IO	199.4

Bolt Syntax: .....IO Q .IO51X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.1	nA
EQL_{pd}	274.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	2.60	2.82	3.00	3.16	3.31
		t_{PHL}	1.93	2.15	2.32	2.47	2.61

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	IO	t_{PLH}	5.09	7.28	9.47	12.75	18.23
		t_{PHL}	3.20	4.31	5.41	7.08	9.85
EN	IO	t_{HZ}	0.95				
		t_{LZ}	0.60				
		t_{ZH}	5.23	7.42	9.61	12.90	18.37
		t_{ZL}	3.23	4.33	5.44	7.10	9.87

IO51X2

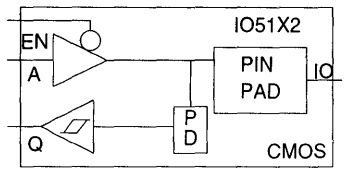
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO51X2 is a 2 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	2.8
EN	3.1
IO	199.4

Bolt Syntax: .....IO Q .IO51X2 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.1	nA
EQL_{pd}	277.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	2.60	2.83	3.01	3.17	3.32
		t_{PHL}	1.94	2.14	2.31	2.47	2.61

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

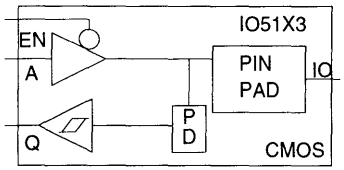
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	IO	t_{PLH}	3.05	6.88	9.62	12.36	17.82
		t_{PHL}	3.22	7.09	9.86	12.63	18.17
EN	IO	t_{HZ}	1.30				
		t_{LZ}	0.60				
		t_{ZH}	3.21	7.04	9.77	12.51	17.98
		t_{ZL}	3.23	7.10	9.87	12.64	18.18

Description:

IO51X3 is a 4 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state output and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	5.1
EN	4.2
IO	199.5

Bolt Syntax: .....IO Q .IO51X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	56.9	nA
EQL_{pd}	290.0	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	2.64	2.87	3.05	3.21	3.35
		t_{PHL}	1.97	2.19	2.35	2.50	2.65

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.91	3.84	6.58	12.05	17.51
		t_{PHL}	1.96	3.90	6.66	12.20	17.74
EN	IO	t_{HZ}	1.40				
		t_{LZ}	0.58				
		t_{ZH}	2.13	4.07	6.80	12.27	17.74
		t_{ZL}	1.94	3.89	6.67	12.21	17.75

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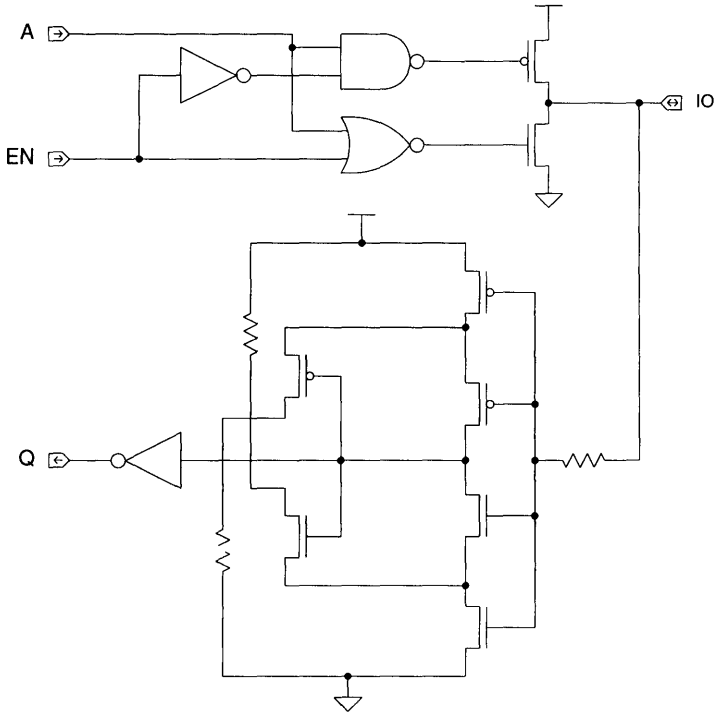
AMI8G 0.8 micron CMOS Gate Array

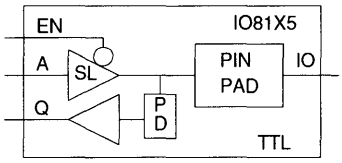
Logic Schematic



Description:

IO81X5 is an 8 mA, non-inverting, TTL-level, bidirectional buffer pad with an active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	9.9
EN	6.9
IO	199.7

Bolt Syntax: .....IO Q .IO81X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	63.6	nA
EQL_{pd}	318.9	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.75	0.90	1.04	1.17	1.30
		t_{PHL}	1.07	1.28	1.44	1.59	1.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
A	IO	t_{PLH}	1.36	2.44	3.93	6.92	9.90
		t_{PHL}	2.69	5.77	10.07	18.47	26.78
EN	IO	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	1.71	2.78	4.28	7.26	10.25
		t_{ZL}	2.67	5.76	10.06	18.46	26.77

IO81X7

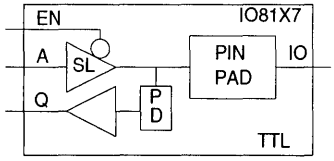
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO81X7 is a 16 mA, non-inverting, TTL-level, bidirectional buffer pad with an active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	14.3
EN	8.7
IO	200.4

Bolt Syntax: .....IO Q .IO81X7 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	69.0	nA
EQL_{pd}	357.6	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.75	0.90	1.03	1.16	1.29
		t_{PHL}	1.05	1.25	1.41	1.56	1.70

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

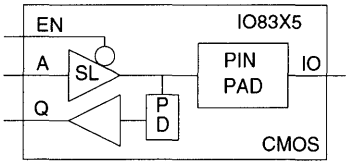
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.09	1.69	2.46	3.96	5.45
		t_{PHL}	1.75	3.31	5.51	9.86	14.16
EN	IO	t_{HZ}	1.86				
		t_{LZ}	1.02				
		t_{ZH}	1.55	2.17	2.95	4.45	5.94
		t_{ZL}	1.70	3.29	5.50	9.86	14.17

Description:

IO83X5 is an 8 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	10.1
EN	6.7
IO	199.7

Bolt Syntax: .....IO Q .IO83X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	64.1	nA
EQL_{pd}	318.2	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.78	0.95	1.09	1.22	1.35
		t_{PHL}	0.98	1.15	1.29	1.42	1.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.92	3.86	6.60	12.07	17.53
		t_{PHL}	1.98	3.93	6.70	12.24	17.78
EN	IO	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	2.27	4.20	6.94	12.41	17.87
		t_{ZL}	1.96	3.92	6.69	12.23	17.77

IO83X7

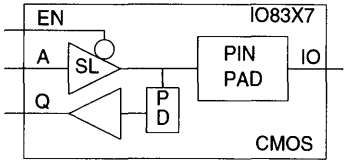
AMI SEMICONDUCTORS
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IO83X7 is a 16 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state and controlled slew rate output.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	14.2
EN	8.7
IO	200.4

Bolt Syntax: .....IO Q .IO83X7 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	69.6	nA
EQL_{pd}	356.7	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.78	0.95	1.09	1.22	1.35
		t_{PHL}	0.98	1.14	1.28	1.41	1.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

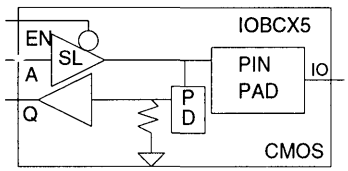
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.42	2.43	3.82	6.56	9.29
		t_{PHL}	1.38	2.36	3.74	6.51	9.28
EN	IO	t_{HZ}	1.86				
		t_{LZ}	1.02				
		t_{ZH}	1.89	2.92	4.30	7.04	9.78
		t_{ZL}	1.33	2.34	3.74	6.52	9.29

Description:

IOBCX5 is an 8 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	10.3
EN	7.1
IO	199.7

Bolt Syntax: .....IO Q .IOBCX5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	64.1	nA
EQL_{pd}	331.0	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.79	0.95	1.09	1.22	1.35
		t_{PHL}	0.98	1.15	1.29	1.42	1.55

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.94	3.87	6.62	12.09	17.56
		t_{PHL}	1.99	3.93	6.69	12.22	17.74
EN	IO	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	2.28	4.22	6.96	12.43	17.90
		t_{ZL}	1.96	3.92	6.69	12.22	17.75

IOBFX5

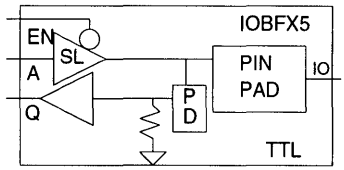
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IOBFX5 is an 8 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-down input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	L

UN = Undriven Node

Pin Loading

	Equivalent Load
A	10.0
EN	7.3
IO	199.7

Bolt Syntax: .....IO Q .IOBFX5 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	63.6	nA
EQL_{pd}	331.9	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.76	0.91	1.04	1.17	1.31
		t_{PHL}	1.08	1.29	1.45	1.60	1.74

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.37	2.45	3.94	6.93	9.92
		t_{PHL}	2.70	5.78	10.07	18.45	26.72
EN	IO	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	1.72	2.79	4.29	7.28	10.26
		t_{ZL}	2.68	5.76	10.06	18.45	26.73

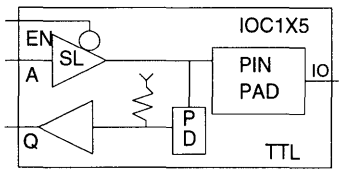
IOC1X5

AMI8G 0.8 micron CMOS Gate Array

Description:

IOC1X5 is an 8 mA, non-inverting, TTL-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	9.9
EN	6.9
IO	199.7

Bolt Syntax: .....IO Q .IOC1X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	64.1	nA
EQL_{pd}	329.8	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.76	0.91	1.04	1.17	1.31
		t_{PHL}	1.08	1.29	1.45	1.60	1.74

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.36	2.43	3.93	6.90	9.88
		t_{PHL}	2.70	5.79	10.09	18.50	26.81
EN	IO	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	1.70	2.78	4.27	7.25	10.23
		t_{ZL}	2.68	5.77	10.08	18.49	26.81

IOC2X5

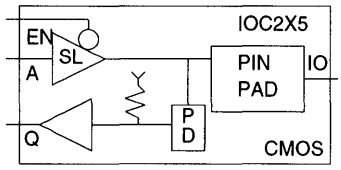
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

IOC2X5 is an 8 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and pull-up input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	H

UN = Undriven Node

Pin Loading

	Equivalent Load
A	10.1
EN	6.8
IO	199.7

Bolt Syntax: .....IO Q .IOC2X5 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	64.6	nA
EQL_{pd}	328.7	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	0.78	0.95	1.08	1.21	1.35
		t_{PHL}	0.98	1.15	1.28	1.41	1.54

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

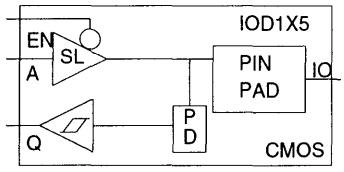
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.92	3.85	6.59	12.04	17.50
		t_{PHL}	1.99	3.94	6.71	12.25	17.80
EN	IO	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	2.27	4.20	6.93	12.39	17.85
		t_{ZL}	1.97	3.92	6.70	12.24	17.79

Description:

IOD1X5 is an 8 mA, non-inverting, CMOS-level, bidirectional buffer pad with active low enabled tri-state, controlled slew rate output, and CMOS Schmitt trigger input.

Logic Symbol



Truth Table

A	EN	IO	Q
L	L	L	L
H	L	H	H
X	H	L	L
X	H	H	H
X	H	UN	X

UN = Undriven Node

Pin Loading

	Equivalent Load
A	10.1
EN	6.9
IO	199.7

Bolt Syntax: .....IO Q .IOD1X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	64.0	nA
EQL_{pd}	325.5	Eq-load

See page 2-13 for power equation.

Input Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
IO	Q	t_{PLH}	2.76	2.99	3.17	3.33	3.48
		t_{PHL}	2.06	2.27	2.44	2.59	2.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Output Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	IO	t_{PLH}	1.93	3.86	6.60	12.07	17.53
		t_{PHL}	1.98	3.93	6.70	12.24	17.78
EN	IO	t_{HZ}	1.61				
		t_{LZ}	0.68				
		t_{ZH}	2.27	4.20	6.94	12.41	17.87
		t_{ZL}	1.96	3.92	6.69	12.23	17.77

OB01X1

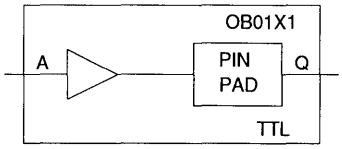
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB01X1 is a 1 mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	1.3

Bolt Syntax: .....Q .OB01X1 A;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	47.4	nA
EQL_{pd}	260.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	Q	t_{PLH}	3.10	4.30	5.49	7.29	10.28
		t_{PHL}	4.56	6.32	8.07	10.76	15.15

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

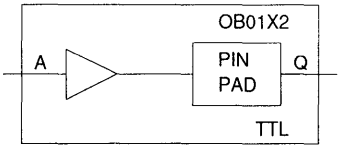
OB01X2

AMI8G 0.8 micron CMOS Gate Array

Description:

OB01X2 is a 2 mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	2.3

Bolt Syntax: .....Q .OB01X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	48.5	nA
EQL_{pd}	264.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	Q	t_{PLH}	1.75	3.84	5.33	6.82	9.81
		t_{PHL}	4.40	10.56	14.99	19.39	28.25

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB01X3

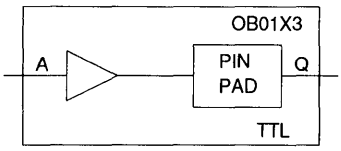
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB01X3 is a 4 mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	3.4

Bolt Syntax: .....Q .OB01X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.5	nA
EQL_{pd}	271.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.24	2.29	3.78	6.77	9.75
		t_{PHL}	2.58	5.66	10.11	18.92	27.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

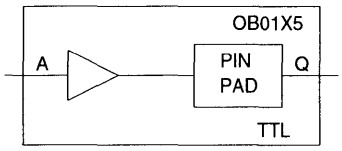
OB01X5

AMI8G 0.8 micron CMOS Gate Array

Description:

OB01X5 is an 8 mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	5.9

Bolt Syntax: .....Q .OB01X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.5	nA
EQL_{pd}	291.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.03	1.61	2.37	3.87	5.36
		t_{PHL}	1.72	3.29	5.51	9.96	14.35

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB01X7

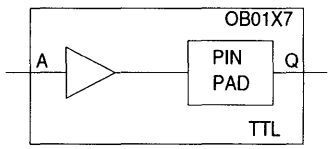
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB01X7 is a 16 mA, non-inverting, TTL-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	7.8

Bolt Syntax: .....Q .OB01X7 A;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.5	nA
EQL_{pd}	288.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.04	1.48	2.02	3.04	4.03
		t_{PHL}	1.37	2.21	3.35	5.58	7.78

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

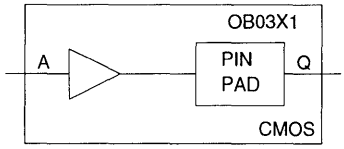
OB03X1

AMI8G 0.8 micron CMOS Gate Array

Description:

OB03X1 is a 1 mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	1.3

Bolt Syntax: .....Q .OB03X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	47.4	nA
EQL_{pd}	260.2	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	Q	t_{PLH}	5.17	7.35	9.55	12.84	18.31
		t_{PHL}	3.17	4.28	5.39	7.05	9.81

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB03X2

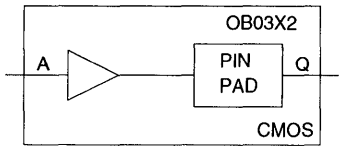
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB03X2 is a 2 mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	2.9

Bolt Syntax: .....Q .OB03X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	48.5	nA
EQL_{pd}	263.4	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	Q	t_{PLH}	2.78	6.60	9.34	12.06	17.54
		t_{PHL}	3.00	6.87	9.66	12.42	17.96

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

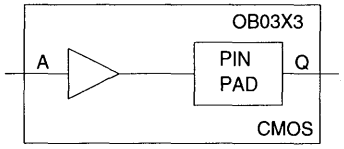
OB03X3

AMI8G 0.8 micron CMOS Gate Array

Description:

OB03X3 is a 4 mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	3.4

Bolt Syntax: .....Q .OB03X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.5	nA
EQL_{pd}	271.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.76	3.68	6.42	11.89	17.35
		t_{PHL}	1.87	3.80	6.57	12.12	17.66

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB03X5

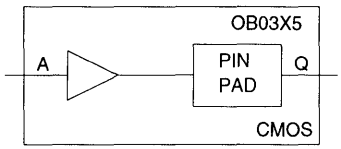
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB03X5 is an 8 mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	5.9

Bolt Syntax: .....Q .OB03X5 A;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.5	nA
EQL_{pd}	291.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.35	2.35	3.73	6.47	9.21
		t_{PHL}	1.36	2.36	3.75	6.52	9.30

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

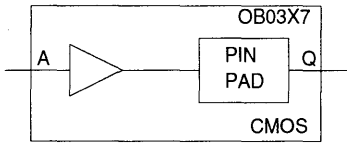
OB03X7

AMI8G 0.8 micron CMOS Gate Array

Description:

OB03X7 is a 16 mA, non-inverting, CMOS-level output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	7.8

Bolt Syntax: .....Q .OB03X7 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.5	nA
EQL_{pd}	288.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.30	2.01	2.95	4.79	6.62
		t_{PHL}	1.14	1.70	2.44	3.84	5.23

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB06X1

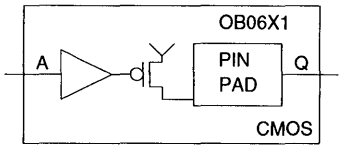
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB06X1 is a 1 mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Equivalent Load
A	1.3
Q	217.5

Bolt Syntax: .....Q .OB06X1 A;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	48.5	nA
EQL_{pd}	258.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	Q	t_{PLH} t_{HZ}	3.89 0.80	5.49	7.08	9.44	13.40

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

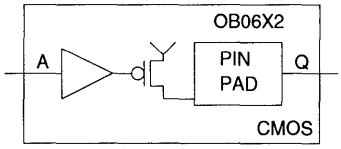
OB06X2

AMI8G 0.8 micron CMOS Gate Array

Description:

OB06X2 is a 2 mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Equivalent Load
A	1.3
Q	217.6

Bolt Syntax: .....Q .OB06X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.5	nA
EQL_{pd}	263.5	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	Q	t_{PLH} t_{HZ}	2.33 0.85	5.12	7.09	9.05	13.01

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB06X3

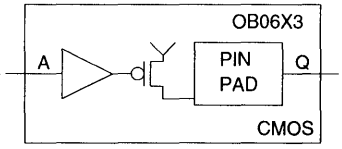
AMI SEMICONDUCTORS
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB06X3 is a 4 mA, inverting, CMOS-level, P-channel, open-drain (pull-up) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Equivalent Load
A	1.2
Q	217.7

Bolt Syntax: .....Q .OB06X3 A;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.5	nA
EQL_{pd}	270.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{HZ}	1.64 1.06	3.04	5.02	8.99	12.93

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

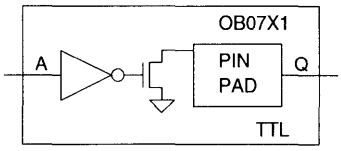
OB07X1

AMI8G 0.8 micron CMOS Gate Array

Description:

OB07X1 is a 1 mA, non-inverting, TTL-level, N-channel, open-drain (pull-down) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Equivalent Load
A	1.3
Q	217.4

Bolt Syntax: .....Q .OB07X1 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	47.4	nA
EQL_{pd}	254.8	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	Q	t_{PHL} t_{LZ}	4.31 0.54	6.09	7.84	10.46	14.86

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB07X2

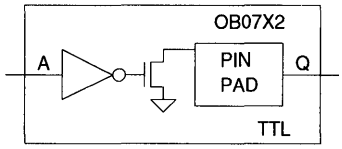
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB07X2 is a 2 mA, non-inverting, TTL-level, N-channel, open-drain (pull-down) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Equivalent Load
A	2.3
Q	217.4

Bolt Syntax: .....Q .OB07X2 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	48.5	nA
EQL_{pd}	256.2	Eq-load

See page 2-13 for power equation.

Pad Logic

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

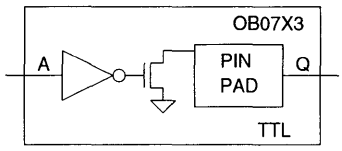
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	Q	t_{PHL} t_{LZ}	4.23 0.38	10.34	14.76	19.17	27.97

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description:

OB07X3 is a 4 mA, non-inverting,TTL-level, N-channel, open-drain (pull-down) output buffer pad.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Equivalent Load
A	3.4
Q	217.4

Bolt Syntax: .....Q .OB07X3 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	49.5	nA
EQL_{pd}	258.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PHL} t_{LZ}	2.25 0.42	5.35	9.79	18.60	27.45

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB09X1

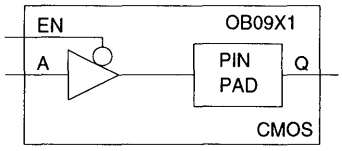
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB09X1 is a 1 mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	2.7
EN	2.8
Q	217.5

Bolt Syntax: .....Q .OB09X1 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.1	nA
EQL_{pd}	265.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	Q	t_{PLH}	5.07	7.25	9.45	12.73	18.21
		t_{PHL}	3.21	4.32	5.12	7.07	9.83
EN	Q	t_{HZ}	0.96				
		t_{LZ}	0.59				
		t_{ZH}	5.22	7.39	9.58	12.87	18.35
		t_{ZL}	3.24	4.34	5.44	7.09	9.86

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

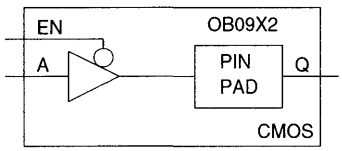
OB09X2

AMI8G 0.8 micron CMOS Gate Array

Description:

OB09X2 is a 2 mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	2.7
EN	2.8
Q	217.5

Bolt Syntax: .....Q .OB09X2 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.2	nA
EQL_{pd}	268.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	Q	t_{PLH} t_{PHL}	3.04 3.20	6.86 7.08	9.61 9.85	12.36 12.63	17.82 18.17
EN	Q	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.30 0.59 3.19 3.20	 7.03 7.93	 9.77 9.86	 12.51 12.65	 17.97 18.18

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB09X3

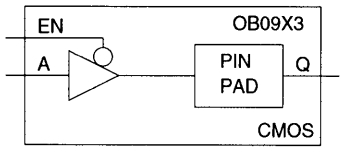
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB09X3 is a 4 mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	4.8
EN	3.9
Q	217.8

Bolt Syntax: .....Q .OB09X3 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	52.9	nA
EQL_{pd}	280.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.90	3.84	6.58	12.05	17.52
		t_{PHL}	1.95	3.89	6.66	12.19	17.75
EN	Q	t_{HZ}	1.40				
		t_{LZ}	0.58				
		t_{ZH}	2.13	4.06	6.81	12.27	17.75
		t_{ZL}	1.93	3.89	6.67	12.20	17.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

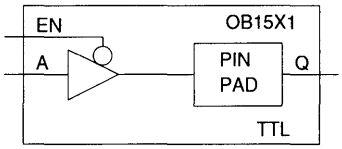
OB15X1

AMI8G 0.8 micron CMOS Gate Array

Description:

OB15X1 is a 1 mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	2.7
EN	2.8
Q	217.5

Bolt Syntax: .....Q .OB15X1 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.2	nA
EQL_{pd}	265.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
A	Q	t_{PLH}	3.00	4.19	5.39	7.18	10.17
		t_{PHL}	4.61	6.34	8.12	10.74	15.15
EN	Q	t_{HZ}	0.96				
		t_{LZ}	0.59				
		t_{ZH}	3.14	4.34	5.53	7.32	10.31
		t_{ZL}	4.63	6.37	8.14	10.77	15.17

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB15X2

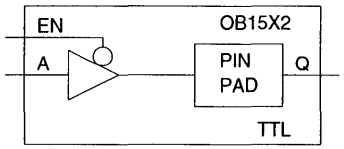
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB15X2 is a 2 mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	2.7
EN	2.8
Q	217.6

Bolt Syntax: .....Q .OB15X2 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	50.2	nA
EQL_{pd}	268.0	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
A	Q	t_{PLH}	1.98	4.08	5.57	7.07	10.05
		t_{PHL}	4.57	10.77	15.19	19.59	28.44
EN	Q	t_{HZ}	1.30				
		t_{LZ}	0.59				
		t_{ZH}	2.13	4.23	5.73	7.22	10.20
		t_{ZL}	4.58	10.78	15.19	19.60	28.45

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

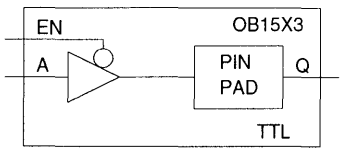
OB15X3

AMI8G 0.8 micron CMOS Gate Array

Description:

OB15X3 is a 4 mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	4.8
EN	3.9
Q	217.7

Bolt Syntax: .....Q .OB15X3 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	52.9	nA
EQL_{pd}	280.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHL}	1.35 2.65	2.43 5.74	3.92 10.16	6.91 19.02	9.89 27.83
EN	Q	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.40 0.58 1.57 2.63	 2.65 5.74	 4.15 10.17	 7.13 19.03	 10.11 27.84

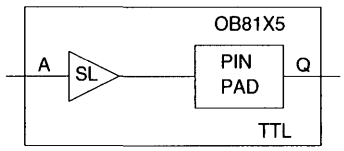
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB81X5 is an 8 mA, non-inverting, TTL-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	8.1

Bolt Syntax: .....Q .OB81X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.9	nA
EQL_{pd}	301.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.24	2.30	3.79	6.78	9.76
		t_{PHL}	2.59	5.57	9.70	17.77	25.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

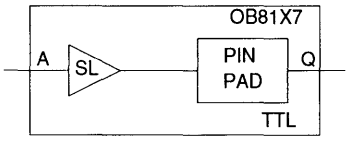
OB81X7

AMI8G 0.8 micron CMOS Gate Array

Description:

OB81X7 is a 16 mA, non-inverting, TTL-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	10.9

Bolt Syntax: .....Q .OB81X7 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	58.0	nA
EQL_{pd}	304.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.01	1.57	2.33	3.82	5.31
		t_{PHL}	1.69	3.23	5.40	9.62	13.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB83X5

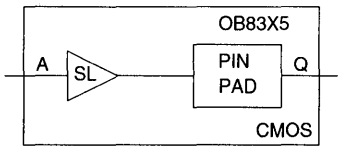
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB83X5 is an 8 mA, non-inverting, CMOS-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	8.1

Bolt Syntax: .....Q .OB83X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	54.9	nA
EQL_{pd}	301.9	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.79	3.71	6.44	11.88	17.30
		t_{PHL}	1.89	3.84	6.61	12.14	17.69

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

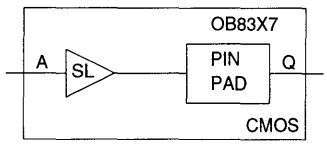
OB83X7

AMI8G 0.8 micron CMOS Gate Array

Description:

OB83X7 is a 16 mA, non-inverting, CMOS-level, output buffer pad with controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	H

Pin Loading

	Equivalent Load
A	10.9

Bolt Syntax: .....Q .OB83X7 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	58.0	nA
EQL_{pd}	304.7	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.31	2.30	3.67	6.41	9.14
		t_{PHL}	1.31	2.30	3.60	6.45	9.21

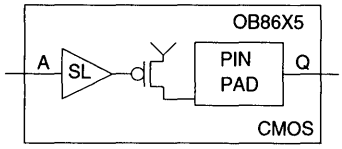
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB86X5 is an 8 mA, inverting, CMOS-level, output buffer pad with a P-channel open-drain (pull-up) and controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	H
H	Z

Pin Loading

	Equivalent Load
A	1.2
Q	217.8

Bolt Syntax: .....Q .OB86X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	53.9	nA
EQL_{pd}	289.3	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH} t_{PHZ}	1.70 1.25	2.91	4.63	8.03	11.43

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

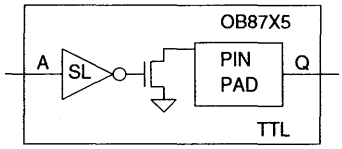
OB87X5

AMI8G 0.8 micron CMOS Gate Array

Description:

OB87X5 is an 8 mA, non-inverting, TTL-level, output buffer pad with N-channel open-drain (pull-down) and controlled slew rate output.

Logic Symbol



Truth Table

A	Q
L	L
H	Z

Pin Loading

	Equivalent Load
A	6.1
Q	217.4

Bolt Syntax: .....Q .OB87X5 A;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	51.5	nA
EQL_{pd}	275.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PHL} t_{PLZ}	2.25 0.42	5.23	9.34	17.38	25.28

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

OB89X5

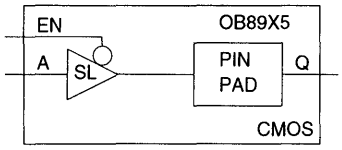
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

OB89X5 is an 8 mA, non-inverting, CMOS-level, tri-state output buffer pad with active low enable and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	9.5
EN	6.3
Q	217.8

Bolt Syntax: .....Q .OB89X5 A EN;

Pad Logic

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	60.1	nA
EQL_{pd}	318.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.92	3.85	6.59	12.06	17.50
		t_{PHL}	1.99	3.92	6.69	12.23	17.77
EN	Q	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	2.27	4.20	6.93	12.40	17.86
		t_{ZL}	1.96	3.91	6.68	12.22	17.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

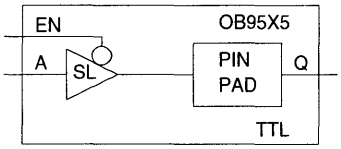
OB95X5

AMI8G 0.8 micron CMOS Gate Array

Description:

OB95X5 is an 8 mA, non-inverting, TTL-level, tri-state output buffer pad with active low enable and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	Q
L	L	L
L	H	H
H	X	Z

Pin Loading

	Equivalent Load
A	9.5
EN	6.3
Q	217.8

Bolt Syntax: .....Q .OB95X5 A EN;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	60.1	nA
EQL_{pd}	318.1	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	Q	t_{PLH}	1.36	2.43	3.93	6.92	9.90
		t_{PHL}	2.68	5.75	10.04	18.45	26.74
EN	Q	t_{HZ}	1.60				
		t_{LZ}	0.68				
		t_{ZH}	1.70	2.78	4.27	7.26	10.24
		t_{ZL}	2.66	5.74	10.03	18.44	26.73

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

PORA

American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

Description:

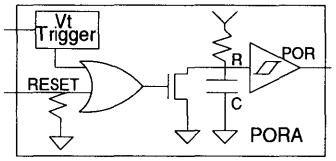
PORA is a power-on-reset circuit for 5V operation.

When power is applied, the POR output is asserted low for at least 400 nanoseconds after the logic circuits become operational. The active high RESET input also drives the POR signal to its active low state.

For proper operation, user-designed external circuitry must limit the slew rate of V_{DD} power to a maximum of one volt per microsecond. This ensures that the reset pulse will be properly output when V_{DD} falls to zero and immediately returns to its valid range.

PORA will work at V_{DD} voltages down to 3.0V. For operation with V_{DD} voltage below 4.5V, user-designed external circuitry must limit maximum V_{DD} slew rate to 0.5V per microsecond.

Logic Symbol



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Equivalent Load
RESET	TBD

Bolt Syntax: .....POR .PORA RESET;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	TBD	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
RESET	POR	t_{PLH}	978.2	978.4	978.6	978.8	979.0
		t_{PHL}	5.49	5.76	5.97	6.17	6.35

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

PORB

AMI8G 0.8 micron CMOS Gate Array

Description:

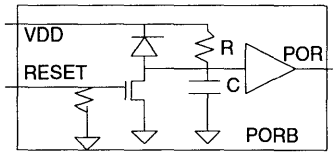
PORB is a power-on-reset circuit for 3V operation.

The POR output is active low. The active high RESET input can also drive the POR line low.

PORB is designed for rapidly rising V_{DD} power associated with battery-operated equipment. For proper operation, V_{DD} slew rate must be faster than 7.5V per microsecond.

The POR output will remain low at least 50 ns after V_{DD} reaches a valid 3V level.

Logic Symbol



Truth Table

RESET	POR
L	H
H	L

Pin Loading

	Equivalent Load
RESET	TBD

Bolt Syntax: .....POR .PORB RESET;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	TBD	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	4	8	12	16 (max)
RESET	POR	t_{PLH} t_{PHL}	1356.9 5.54	1357.0 5.62	1357.2 5.73	1357.3 5.82	1357.4 5.90

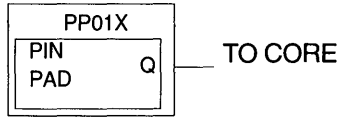
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

PP01X

AMI8G 0.8 micron CMOS Gate Array

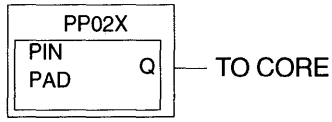
Description:

PP01X is a V_{SS} power supply pin for output buffers, input buffers, and core cells combined. The PP01X is intended for circumstances where output and core busses are to be tied together. It should not be used in conjunction with PPP1X or PPC1X.



Description:

PP02X is a V_{DD} power supply pin for output buffers, input buffers, and core cells combined. One PP02X must be used for each power (V_{DD}) pin.

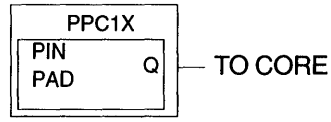


PPC1X

AMI8G 0.8 micron CMOS Gate Array

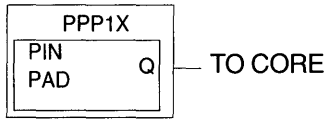
Description:

PPC1X is a V_{SS} power supply pin for core cells and input buffers only. One PPC1X must be used for each ground (V_{SS}) pin for the core cells and input buffers.



Description:

PPP1X is a V_{SS} power supply pin for output buffers only. One PPP1X must be used for each ground (V_{SS}) pin.



QD01X1

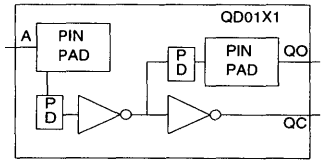
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

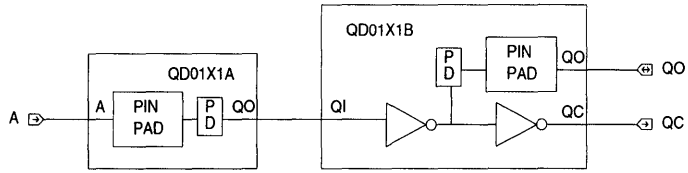
Description:

QD01X1 is a 3.58 MHz (1MHz - 10 MHz) crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Equivalent Load
A	107.1
QO	107.1

Bolt Syntax: .....A QO .QD01X1A ;

.....QC QO .QD01X1B QI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	23.3	nA
EQL_{pd}	125.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
QO	QC	t_{PLH}	1.00	1.15	1.28	1.41	1.54
		t_{PHL}	1.05	1.21	1.34	1.46	1.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

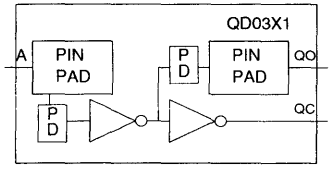
QD03X1

AMI8G 0.8 micron CMOS Gate Array

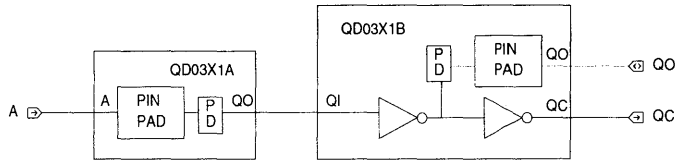
Description:

QD03X1 is a 20 MHz (10 MHz - 32 MHz) crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Equivalent Load
A	107.1
QO	107.1

Bolt Syntax: .....A QO .QD03X1A ;

.....QC QO .QD03X1B QI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	23.3	nA
EQL_{pd}	125.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
QO	QC	t_{PLH}	1.00	1.15	1.28	1.41	1.54
		t_{PHL}	1.05	1.21	1.34	1.46	1.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

QD06X1

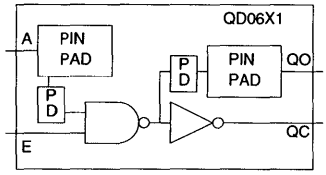
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

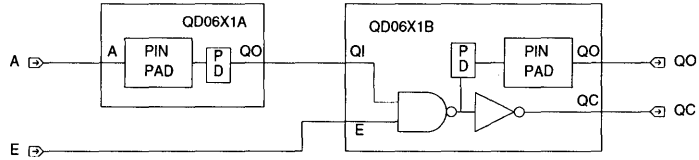
Description:

QD06X1 is a 33 MHz enabled crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Equivalent Load
A	107.1
E	2.0
QO	107.1

Bolt Syntax: .....A QO .QD06X1A E;

.....QC QO .QD06X1B QI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	23.3	nA
EQL_{pd}	125.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
QO	QC	t_{PLH}	1.00	1.15	1.28	1.41	1.54
		t_{PHL}	1.05	1.21	1.34	1.46	1.59

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

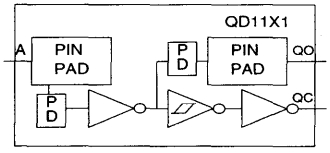
QD11X1

AMI8G 0.8 micron CMOS Gate Array

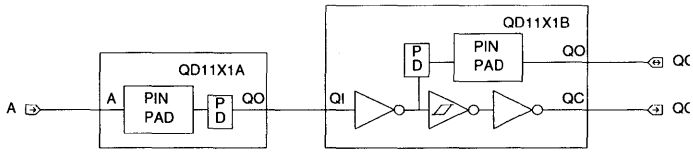
Description:

QD11X1 is a 32kHz (32kHz - 1MHz) crystal oscillator with Schmitt trigger. QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	H	H
H	L	L

Pin Loading

	Equivalent Load
A	107.1
QO	107.1

Bolt Syntax: .....A QO .QD11X1A ;

.....QC QO .QD11X1B QI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	23.3	nA
EQL_{pd}	125.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
QO	QC	t_{PLH}	2.28	2.49	2.65	2.80	2.94
		t_{PHL}	1.58	1.77	1.93	2.07	2.21

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

QD13X1

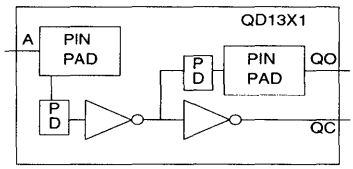
American Microsystems, Inc.

AMI8G 0.8 micron CMOS Gate Array

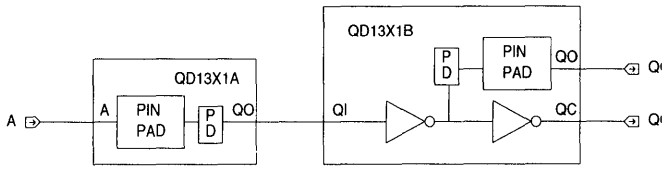
Description:

QD13X1 is a 33-36 MHz third-overtone crystal oscillator, where QC is the clock to the chip logic and QO is the oscillator feedback. This cell is made up of two pad cells and requires the use of two package pins. The Logic Schematic below shows how to connect the two pad cells.

Logic Symbol



Logic Schematic



Truth Table

A	QC	QO
L	L	H
H	H	L

Pin Loading

	Equivalent Load
A	107.1
QO	107.1

Bolt Syntax: .....A QO .QD13X1A ;

.....QC QO .QD13X1B QI;

Power Characteristics:

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	23.3	nA
EQL_{pd}	125.6	Eq-load

See page 2-13 for power equation.

Delay Characteristics:

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	Delay (ns) To	Parameter	Number of Equivalent Loads 1	11	21	31	41 (max)
QO	QC	t_{PLH}	1.04	1.20	1.34	1.48	1.62
		t_{PHL}	1.23	1.20	1.52	1.64	1.76

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

SECTION 5
MEGACELLS

Digital Soft Megacells

Overview

American Microsystems, Inc.'s ("AMI's") megacells are blocks of memory or complex blocks of logic consisting of fundamental building primitives such as nand gates, nor gates, flip-flops, and latches. Such megacells can be either soft or hard.

A hard megacell is one in which the megacell function is defined by the physical mask layout; thus, each instance of the hard megacell has exactly the same physical layout within the boundaries of the megacell.

A soft megacell is defined only at the functional schematic level. In this case, each instance of the megacell will have exactly the same functional definition; however, the physical mask layout will be different for each instance depending on other functions being used, the place-and-route tools, and process technology.

AMI's soft megacells are developed in AMI's ASIC Standard Library. This library is technology and process independent and is available in both standard cells and gate arrays.

Because a soft megacell is both process and technology independent, it has the advantages of design flexibility, portability, and a path for future cost reduction by process migration.

As process technologies have improved to permit the integration of more functions onto a single die, the demand for ASIC megacells has increased. Complex megacells, such as AMI's MGMC51, become practical with process technologies at 1.0 micron feature sizes.

Soft megacells can be used with other megacells including ROM and RAM and logic from the ASIC Standard Library to build a complete system on a chip.

AMI offers a selection of soft megacells which duplicate the function of industry standard parts (Standard-Function Digital Soft Megacells) plus soft megacells which are developed using parameterized logic synthesizers (Datapath Megacells).

Why Megacells

Using megacells in designing ASICs has several advantages. Megacells help decrease design time and costs by providing large building blocks that are equivalent to standard products and functions. The power consumption of a soft megacell can be greatly reduced in comparison to the HMOS standard products they replace. Also, because several functions can be put on a single die, printed circuit board space and capacitances can be saved and the power requirements to get signals on and off ICs are minimized.

Reliability and system costs can be improved because of decreased part and pin counts. Also, because the megacell is typically implemented in a process technology smaller than the original standard product, performance can be several times that of the standard product.

What Are Soft Megacells

A soft megacell is defined as schematic pages. This approach provides extreme flexibility with regard to design changes, testability, fault grading, design checking, process selection, and whether the design is implemented as a gate array or standard cell. Also to improve the robustness of the megacell, soft megacells are built with fully static logic.

Design tools, methodologies, and libraries available today greatly reduce the design risks associated with soft megacells. Since each instance of the cell can be back annotated with actual capacitive loading data, detailed timing analysis can validate each instance in the given application.

Since the megacell is just a schematic, its characteristics and functions can be changed or deleted by just changing the appropriate schematic pages. For example, to change the initial conditions of the MGMC51 output ports, it is only necessary to change the output port flip-flop in each port cell from a set type of flop to a reset type of flop.

By deleting unused functions, gate count can be minimized. For example, if a timer or UART is not being used, the associated gates can be deleted resulting in a lower gate count. Re-running the simulations, as one would do after any design change, validates correct implementation of the design change.

However, it is in design checking where the strengths of the soft megacell approach become obvious. Electronic design has benefited from the recent introduction of software programs that check many aspects of the design, including set up and hold times for flip-flops, the possibility of asynchronous race conditions, and the fault coverage of the test vectors. The schematic implementation of the megacell can be subjected to these checks along with the rest of the circuitry. Behavioral models, which are frequently used with hard megacells, bypass these checks.

Since the soft megacell uses only components of the ASIC Standard Library, process dependencies in the design are minimized, if not completely removed. As a result, the design can be ported to new technologies as they become available. This means not only future cost savings, but extended voltage and temperature operation as well.

Datapath Digital Soft Megacells

Many of the soft megacells are produced by Datapath synthesizers. Examples are the MGMxxyyDv (multiplier) and the MGCxxBv (6-function binary comparator). These synthesizers are parameterized, allowing the creation of various size and speed Datapath megacells. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each particular implementation is given a version number.

These Datapath synthesizers produce soft megacell schematics in the ASIC Standard Library and a schematic symbol. They are available on the various workstations.

Testing

Testability of soft megacells in IC designs must be considered when designing and simulating the circuits. Usually, additional logic is necessary to simplify testing. Providing either direct or multiplexed input and output pins for controlling and observing the core processors can greatly simplify the testing of the IC and any system debugging. This dictates that designs be contained in packages having at least as many pins as the megacell with the highest pin count.

To select the megacell pins, an unused condition on the interface is often used, which would normally never occur in an application. When enabled, the pins of the core are connected to the pins of the ASIC. The supplied, or independently developed, simulations patterns can then be run to develop a test or to verify the functionality of the core.

Data sheets

The Standard-Function megacells are designed to duplicate the function of an industry standard part. The data sheets for these megacells are intended to give a short overview, define cell pinout, and to outline any functional differences between AMI's megacell and the industry standard part. Detailed functional information can be found in any standard device data sheet.

The Datapath data sheets contain a functional description, a pin description, and sample equivalent gate counts with sample delays.

Cell List

The following tables list the Standard-Function and Datapath megacells available. Additional megacells are continually being added to the list.

Ordering information

To order a megacell, use the digital soft megacell order form. Contact the factory for information on the delivery of soft megacells on various workstations or for information on specific speeds and sizes of particular Datapath megacells.

Standard-Function Digital Soft Megacells

Megacell	Function
MG1468C18	Real-time clock
MG29C01	4-Bit microprocessor slice
MG29C10	Microprogram controller/sequencer
MG65C02	8-Bit microprocessor
MG80C85	8-Bit microprocessor
MG82C37A	Programmable DMA controller
MG82C50A	Asynchronous comm. element
MG82C54	Programmable interval timer
MG82C55A	Programmable peripheral interface
MG82C59A	Programmable interrupt controller
MGMC51	8-Bit microcontroller, 8051 compatible
MGMC51FB	8-Bit microcontroller, 8051 compatible

Datapath Digital Soft Megacells

Megacell	Function
MGAxxyyDv	Adder
MGAxxyyEv	Adder/Subtractor
MGBxxAv	Barrel/Arithmetic shifter
MGBxxBv	Barrel shifter
MGBxxyyCv	Arithmetic shifter
MGCxxAv	2-Function binary comparator
MGCxxBv	6-Function binary comparator
MGDxxAv	Decrementer
MGFxxyyC1	Latch-based FIFO
MGIxxAv	Incrementer
MGIxxBv	Incrementer/Decrementer
MGMxxyyDv	Signed/unsigned multiplier
MGMxxyyEv	Multiplier/Accumulator
MGSxxyyAv	Signed/unsigned subtractor

MG1468C18
Real-Time Clock

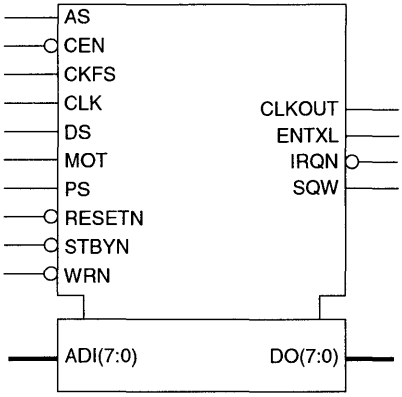
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell
- Functionally compatible with the industry standard 146818
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- 12- or 24-hour clock with a.m. and p.m. mode
- Leap year and end-of-month recognition
- Programmable alarm

LOGIC SYMBOL

MG1468C18



Description

The MG1468C18 real-time clock is a peripheral device which may be used with various processors/computers. It combines these features: a complete time-of-day clock with alarm, a one hundred year calendar, and a programmable periodic interrupt and square wave generator.

The real-time clock is designed for use as a battery powered element, including all the common backed-up functions such as RAM, time, and calendar.

The megacell has been partitioned with battery backup application in mind. For purposes of electrical isolation, the multiplexed address and data bus are split into input and output sides. The split avoids any possible conduction paths which result when the outputs of the tri-state buffers in a portion of the chip, which could be without power, are connected to active or tri-state outputs of powered circuits.

If not using battery backup, it is possible to configure the megacell to appear to the rest of the ASIC as if the data bus were bidirectional using ENTXL.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
AD(7:0)	I	Multiplexed bidirectional address and data bus. May be combined with the DO(7:0) bus using the ENTXL signal.
AS	I	Address strobe. The falling edge of AS latches the address from the ADI bus.
CEN	I	Chip enable, active low.
CKFS	I	Selects the output frequency of CLKOUT. When CKFS = 1, the frequency of CLKOUT will equal CLK. When CKFS = 0, the frequency of CLKOUT will equal CLK/4.
CLK	I	Time-base input for the time functions of the real-time clock.
CLKOUT	O	Output at the time-base frequency divided by 1 or 4.
DO(7:0)	O	Data output bus. May be combined with the ADI(7:0) bus using the ENTXL signal.
DS	I	Data strobe. The DS signal is used with the WRN signal to latch write data from the ADI bus and output data to the DO bus.
ENTXL	O	Input/Output bus control. Used to create a multiplexed address/data bus external to the RTC. When ENTXL = 0, this external bus should be put in output mode, indicating a read cycle. If ENTXL = 1, the bus should be in a high-impedance state, allowing external drive.
IRQN	O	Interrupt request, active low. Signifies an interrupt condition is present.
MOT	I	Allows selection between Motorola (MOT = 1) and Intel (MOT = 0) bus timing.
PS	I	Power sense. Used to control the valid RAM and time bit in register D.
RESETN	I	Megacell reset active low. Does not affect the clock, calendar, or RAM functions.
STBYN	I	Stand by, active low. Prevents access to the RTC.
SQW	O	Square wave output from one of the 15 taps provided by the 22 internal-divider stages.
WRN	I	Write enable, active low. Used with the DS pin to read and write data.

Equivalent Gates

Standard Cell	Gate Array
2,000	2,600

MG29C01
4-Bit Microprocessor

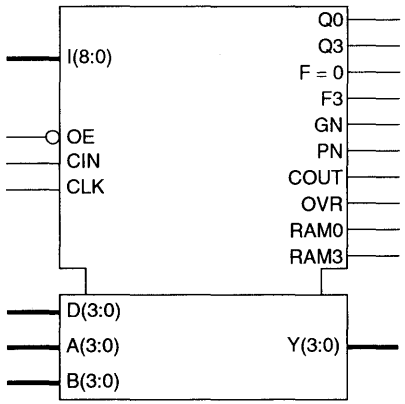
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 2901
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- 4-Bit cascadable bit-slice
- Eight function ALU including addition, two subtraction, and five logic operations on two operands
- Microprogrammable with three groups of three bits each for ALU function, destination control, and source operand
- Two address architecture provides independant access to two working registers
- Five source ports for data selection
- Four status flags including carry, zero, overflow, and sign

LOGIC SYMBOL

MG29C01



Description

The MG29C01 is a high-performance 4-bit cascadable microprocessor.

The MG29C01 offers the designer a simple and methodical approach to designing bit-slice microprocessors, high-speed ALUs, and boolean machines.

The MG29C01 consists of a fast ALU, a 16-word by 4-bit two-port RAM, and the required decoding, multiplexing, and shifting circuits. The microinstruction word consists of nine bits divided into three groups. Bits 0-2 select the ALU source operads. Bits 3-5 select the ALU function and bits 6-8 select the destination register.

The ALU allows for several arithemetic functions which include: unsigned addition and subtraction, two's compliment and one's compliment addition and subtraction, and decrementing. The ALU also produces the status bits: overflow, carry-out, and F = 0. Boolean functions offered include: AND, OR, EX-OR, EX-NOR, INVERT, PASS, ZERO, AND MASK.

The MG29C01 also includes a 16-word by 4-bit register, a 4-bit Q register, and various sources for the ALU.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG29C01
4-Bit Microprocessor

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
I(8:0)	I	The nine instruction lines.
OE	I	Output enable. Controls the Y outputs. When low, the Y outputs are active.
CIN	I	Carry in to the ALU.
CLK	I	The clock input.
D(3:0)	I	Data inputs. These data may be selected as one of the ALU sources. D(0) is the LSB.
A(3:0)	I	The address inputs to the register stack. Used to select which register's contents are available through the A port. A(0) is the LSB.
B(3:0)	I	The address inputs to the register stack. Used to select which register's contents are available through the B port. B(0) is the LSB.
Q0, Q3	I/O	The shift line for the LSB and MSB of the Q register. They are bidirectional to allow for shift up and shift down operations. Q3 is the MSB.
F = 0	O	Becomes active when all four ALU outputs are low.
F3	O	The most significant ALU output bit.
GN, PN	O	The generate and propagate outputs of the ALU. Can be used for carry look-ahead.
COUT	O	Carry out of the ALU.
OVR	O	Overflow. Indicates the result of an arithmetic two's complement operation has overflowed into the sign-bit.
RAM0, RAM3	I/O	The shift line for the LSB and MSB of the register stack. They are bidirectional to allow for shift up and shift down operations. RAM3 is the MSB.
Y(3:0)	O	Data outputs. These outputs are connected to either ALU or A port of the register stack.

Equivalent Gates

Standard Cell	Gate Array
800	1,100

MG29C10
12-Bit Microprogram Controller

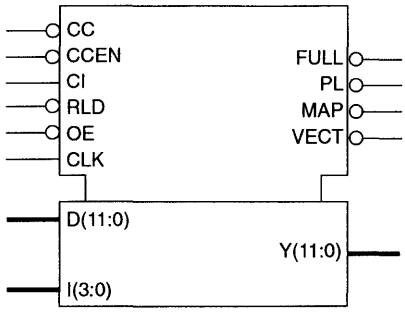
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 2910
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- 12-Bit internal elements can address up to 4069 words of microcode
- 16 sequence control instructions, most are conditional on state of internal loop counter and/or external conditional input
- 12-Bit down counter is pre-settable for repeating instructions or counting loop iterations internally
- Four microprogram address sources including 9-level stack, microprogram counter, branch address bus, and internal holding register
- Internal decoder function controls output enables for three branch address devices

LOGIC SYMBOL

MG29C10



Description

The MG29C10 is a high-performance 12-bit microprogram controller. It functions as an address sequencer for controlling the execution of microinstructions in microprogram memory.

It also controls conditional branching to any microinstruction within its 4096 word range. There are nine levels of subroutine nesting with return linkage and looping capability provided by a last-in, first-out stack.

The MG29C10 has four sources for providing the 12-bit address during each microinstruction. These four sources are as follows:

1. A direct external input.
2. A register/counter (R) which retains data loaded during an earlier microinstruction.
3. The last-in, first-out stack/file (F).
4. The address counter/register which usually increments the addresses.

The MG29C10 consist of six functional blocks: an instruction PLA, a multiplexer, a register/counter, a zero detector, a 9-word by 12-bit stack, a microprogram counter register, and an incrementer.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG29C10
12-Bit Microprogram Controller

AMI SEMICONDUCTORS
American Microsystems, Inc.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
CC	I	Used as test input criterion. Active low.
CCEN	I	Enables CCN. Active low.
CI	I	Carry input to the low order of the microprogram counter.
RLD	I	Forces loading of register/counter regardless of instruction or condition. Active low.
OE	I	Three-state control of Y(11:0). Active low.
CLK	I	Master input clock.
D(11:0)	I	Direct data input to register/counter and multiplexer. D(0) is the LSB.
I(3:0)	I	Instruction inputs. I(0) is the LSB.
FULL	O	Goes low when the internal stack is full. Active low.
PL	O	Used to select #1 source (usually a pipeline register) as the direct input source.
MAP	O	Used to select #2 source (usually a mapping ROM or PLA) as the direct input source.
VECT	O	Used to select #3 source (usually an interrupt starting address) as the direct input source.
Y(11:0)	O	Address to microprogram memory. Y(0) is the LSB.

Equivalent Gates

Standard Cell	Gate Array
1,350	1,950

American Microsystems, Inc.

MG65C02
8-Bit Core Microprocessor

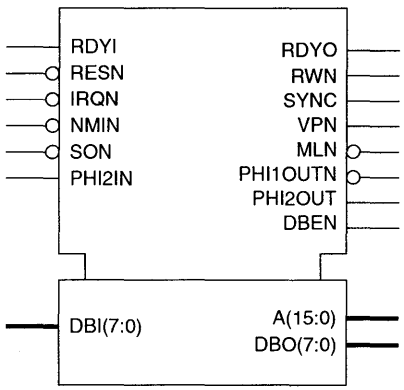
Digital Soft Megacells

Features

- A high-performance, schematic-based megacell
- Functional compatibility with the industry standard 6502
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- 8-Bit microprocessor
- Fully static design
- 0-50 MHz operation
- 64 Kbytes program address space
- Enhanced Instruction Set
- Supports bit manipulation
- 72 instructions and 212 opcodes
- 15 address modes
- Interrupt capability
- Emulation port is available

LOGIC SYMBOL

MG65C02



Description

The MG65C02 is an 8-bit microprocessor which is compatible with the industry standard W65C02S. It has been designed to be compatible with both the original NMOS 6502 and the newer CMOS variations from various vendors.

The MG65C02 runs all 6502 opcodes, as well as the new Enhanced Instruction Set which includes the new bit manipulation opcodes: RMB, SMB, BBR, BBS, and WAI and STP instructions. The latest functions are also incorporated in the MG65C02 such as bus enable, vector pull, and memory lock. It accesses 65 Kbytes of addressable memory. It is fully static allowing the external clock to stop in either state. Operation frequency follows a range of 0 MHz, for low-power or standby modes, to more than 25 MHz for high-speed applications.

Soft Megacells

The MG65C02 is designed as a soft megacell in the ASIC Standard Library, which allows it to be used with other logic and/or megacells. The soft megacell approach has the advantages of design flexibility and portability, and a path for future cost reduction by process migration. It can be used in gate array or standard cell circuits. The core allows access to pins and functions not available in the industry standard 6502.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
A0-A15	O	Address to memory.
DBO0-DBO7	O	Data bus output. Valid when DBEN is high.
DBI0-DBI7	I	Data bus input. Valid when DBEN is low.
DBEN	O	Data bus enable.
RDYI	I	Ready input, active low. Stops the internal clock.
RDYO	O	Ready output. The WAI instruction uses this pin to bring RDYI low.
RESN	I	Active low reset.
IRQN	I	Active low interrupt.
NMIN	I	Active low non-maskable interrupt.
SON	I	Active low sets the overflow bit in the status word.
RWN	O	Read/Write. Active low for write.
SYNC	O	Synchronize. Active during opcode fetch cycle.
VPN	O	Vector pull, active low. Low during interrupt vector access.
MLN	O	Memory lock, active low. Low during Read-Modify-Write (RMW) portion of RMW instructions.
PHI2IN	I	Clock.
PHI1OUTN	O	Clock. Out of phase with C2IN.
PHI2OUT	O	Clock. In phase with PHI2IN. It also goes high with the STP instruction.

Equivalent Gates

Standard Cell	Gate Array
2,950	3,850

MG80C85
8-Bit Microprocessor

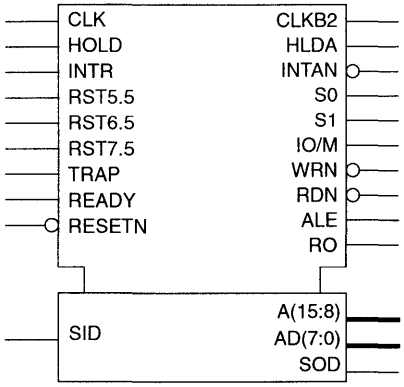
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8085 and 8085A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Full support of extended instruction set, and standard 8080 and 8085/8085A instruction sets
- Runs over 10,000 CP/M® programs
- Direct addressing to 64 Kbytes
- Four interrupt inputs (one non-maskable)

LOGIC SYMBOL

MG80C85



Description

The MG80C85 is an 8-bit microprocessor which features complete functional compatibility with industry standard 8085s and 8085As, and includes support for the special extended instruction set. Its design incorporates an on-board system controller, clock generator, serial I/O port, and direct addressing capability to 64 Kbytes of memory. The MG80C85 utilizes a multiplexed data bus, with 16-bit addresses split between an 8-bit address bus and an 8-bit data bus.

The MG80C85 is a macrocell building block for ASIC logic design. Thus, it can be used in conjunction with existing standard cell and gate array libraries to incorporate into original customer IC designs for lower overall system costs.

Soft Megacells

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
A(15:8)	O	High address bus. The most significant 8-bits of the memory address. A(15) is the MSB.
AD(7:0)	I/O	Low address and data bus. The low order memory address bus multiplexed with the data bus.
ALE	O	Address latch enable. This signal occurs during the first clock state of a machine cycle.
CLK	O	Clock. The period of CLK is twice the period of the CLKBY2 input.
HLDA	O	Hold acknowledge. Indicates that the CPU has received the HOLD request.
HOLD	I	Hold request. Indicates another master is requesting the use of the address and data buses.
INTAN	O	Interrupt acknowledge. This active low signal indicates that the interrupt request input (INTR) has been recognized and acknowledged.
INTR	I	Interrupt request. When INTR goes HIGH, it will inhibit the program counter, generate an INTA) signal, and sample the data bus for a RESTART or CALL instruction.
IO/$\overline{M}$	O	Machine cycle status. See S0 and S1 status bits for further details.
RDN, WRN	O	Read and write control. These active low signals indicate that selected memory or I/O device is to be read or written. They are high impedance during HOLD, HALT, and RESET modes.
READY	I	Ready. This signal is set to HIGH during read or write cycles to indicate that the selected memory or I/O device is ready to send or receive data.
RESETN	I	Reset in. This active low signal sets the program counter to zero, and resets the interrupt enable (INTE) and HLDA flip-flop.
RO	O	Reset out. Indicates that the CPU is being reset.
RST7.5 RST6.5 RST5.5	I	Restart interrupts. These inputs provide three maskable interrupts which invoke an automatic internal restart. RST7.5 is the highest relative priority, followed by RST6.5 and RST5.5. All three interrupts have a higher priority than INTR.
SO, S1, IO/$\overline{M}$	O	Status outputs. These signals provide an indication of the machine status during any given cycle. The status may be latched by the falling edge of the ALE signal.
SID	I	Serial input data. Data on this pin is loaded into accumulator bit 7 during a RIM instruction.
SOD	O	Serial output data. This signal is set or reset by the SIM instruction.
TRAP	I	Trap interrupt. The highest priority non-maskable restart interrupt.
CLKBY2	I	Clock by two. This is the input clock source, used to drive the internal clock generator.

Equivalent Gates

Standard Cell	Gate Array
TBD	TBD

American Microsystems, Inc.

MG82C37A
Programmable DMA Controller

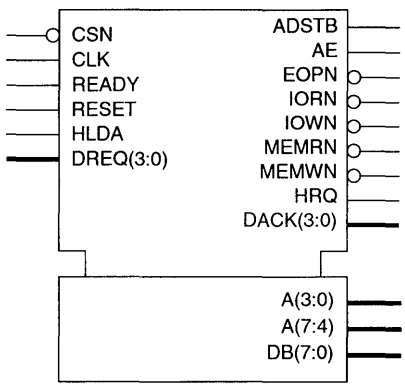
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8237/8237A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Compatible with 8080/85, 8086/88, 80286/386, and 68000 μP families
- Four independent maskable DMA channels with autoinitialize capability
- Memory-to-memory transfer
- Fixed or rotating DMA request priority
- Independent polarity control for DREQ and DACK signals
- Address increment or decrement selection
- Cascadable to any number of channels

LOGIC SYMBOL

MG82C37A



Description

The MG82C37A is a high-performance, programmable Direct Memory Access (DMA) controller offering functional compatibility with the industry standard 8237/8237A. It features four channels, each independently programmable, and is cascadable to any number of channels. Each channel can be programmed to autoinitialize following DMA termination.

In addition, the MG82C37A supports both memory-to-memory transfer capability and memory block initialization, as well as a programmable transfer mode.

The MG82C37A is designed to improve system performance by allowing external devices to transfer data directly from the system memory. High speed and very low power consumption make it an ideal component for aerospace and defense applications. The low power consumption also makes it an attractive addition in portable systems or systems with low-power standby modes.

The MG82C37A DMA controller is a state-driven address and control signal generator designed to accelerate data transfer in systems by moving data from an I/O device to memory or a block memory to an I/O device. Data transfers are direct, rather than being stored enroute in a temporary register.

The MG82C37A also mediates memory-to-memory block transfers and will move data from a single location to a memory block. Temporary storage of data is required, but the transfer rate is significantly faster than CPU processes. The device provides operating modes to carry out both single byte and block transfers of data.

The organization of the MG82C37A is composed of three logic blocks, a series of internal registers, and a counter section. The logic blocks include the Timing Control, Command Control and Priority Encoder circuits.

The Timing Control block generates internal timing signals from the clock input and produces external control signals.

Command Control decodes incoming instructions from the CPU, and the Priority Encoder block regulates DMA channel priority.

The internal registers hold internal states and instructions from the CPU. Addresses and word counts are computed in the counter section.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
A(3:0)	I/O	Low address bus. Idle cycle (Inputs): Addresses the MG82C37A control register to be loaded or read. Active cycle (Outputs): Lower 4-bits of the transfer address.
A(7:4)	O	High address bus. The four most significant address lines. Enabled during DMA service only.
ADSTB	O	Address strobe. Controls latching of the upper address byte.
AE	O	Address enable. Enables the higher order address byte onto the system address bus.
CLK	I	Clock input. May be stopped for standby operation.
CSN	I	Chip select, active low. Selects the MG82C37A as an I/O device (Idle Cycle) for CPU communication on the data bus.
DACK(3:0)	O	DMA acknowledge. Informs a peripheral that the requested DMA transfer has been granted.
DB(7:0)	I/O	Data bus.
DREQ(3:0)	I	DMA request. DMA service is requested by activation of the channel from a specific device. DREQ must be maintained until DACK (service acknowledge) is activated.
EOPN	I/O	End of process, active low. DMA service is terminated when activated.
HLDA	I	Hold acknowledge. Notifies the MG82C73A that the CPU has released control of the system buses.
HRQ	O	Hold request. Requests control of the system buses. HRQ is issued following a request for DMA service (DREQ) from a peripheral, and is acknowledged by the HLDA signal.
IORN	I/O	I/O read. Idle cycle, active low: CPU input control signal for reading the control registers. Active cycle: Output control signal to read data from a peripheral device during a DMA cycle.
IOWN	I/O	I/O write. Idle cycle, active low: CPU input control signal for loading information into the MG82C37A. Active cycle: Output control signal to load data to a peripheral device during a DMA cycle.
MEMRN	O	Memory read, active low. MG82C37A reads data from a selected memory address during a DMA read or memory-to-memory transfer.
MEMWN	O	Memory write, active low. MG82C37A writes data to a selected memory address during a DMA write or memory-to-memory transfer.
READY	I	Ready. Extends the memory read and write pulse widths to accommodate slow I/O peripherals or memories.
RESET	I	Reset. Asynchronous signal clears internal registers and puts the MG82C37A in idle cycle.

Equivalent Gates

Standard Cell	Gate Array
2,800	3,800

American Microsystems, Inc.

MG82C50A
Asynchronous Comm. Element

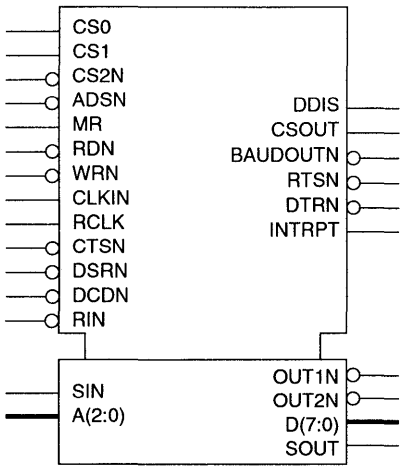
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8250
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Single megacell UART/BRG
- On chip baud rate generator 1 to 65535 divisor generates the BAUDOUTN (16x) clock
- Prioritized interrupt mode
- Microprocessor bus oriented interface
- 80C86/80C88 compatible
- Modem interface
- Line break generation and detection
- Loopback mode
- Double buffered transmitter and receiver

LOGIC SYMBOL

MG82C50



Description

The MG82C50A Asynchronous Communications Element (ACE) is a high-performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single megacell. The device supports data rate from DC to 625K baud (0-10 MHz clock). It is functionally compatible with the industry standard 8250.

The ACE receiver circuitry converts start, data, stop, and parity bits into a parallel data word. The transmitter circuitry converts a parallel data word into serial form and appends the start, parity, and stop bits. The word length is programmable to 5, 6, 7, or 8 data bits. Stop bit selection provides a choice of 1, 1.5, or 2 stop bits.

The BRG divides the clock frequency by a divisor programmable from 1 to 216-1 to provide standard RS-232C baud rates. The BAUDOUT programmable clock output provides a buffered oscillator or a 16x (16 times the data rate) baud rate clock for general purpose system use.

To meet the system requirements of a CPU interfacing to an asynchronous channel, the modem control signals RTSN, CTSN, DSRN, RIN, and DCDN are provided.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
RDN	I	Read, active low. Causes the register selected by A(2:0) to be output to D(7:0).
WRN	I	Write, active low. Causes data from the data bus D(7:0) to be input to the MG82C50A.
D(7:0)	I/O	Data bus. In a high-impedance state except during read operations. D(0) is the LSB.
A(2:0)	I	Register select. Selects the internal registers during CPU bus operations. A(0) is the LSB.
CLKIN	I	Clock in. Clock connection for the internal BRG.
SOUT	O	Serial data output. Serial data output from the MG82C50A transmitter circuitry.
CTSN	I	Clear to send, active low. Indicates that data on SOUT can be transmitted.
DSRN	I	Data set ready, active low. Indicates the modem is ready to exchange data.
DTRN	O	Data terminal ready, active low. Indicates that the MG82C50A is ready to receive data.
RTSN	O	Request to send, active low. Indicates data is ready to transmit. In half-duplex operations, RTS is used to control the direction of the line.
BAUDOUTN	O	Baud out clock. Rate is the CLKIN frequency divided by the specified divisor in the BSR.
OUT1N, OUT2N	O	Outputs 1and 2, active low. Asserted by setting MCR(2, 3) high. Inactive during loop mode.
RIN	I	Ring indicator, active low. Indicates that a telephone ringing signal has been received by the modem or data set.
DCDN	I	Data carrier detect, active low. Indicates that the data carrier has been detected by the modem or data set.
MR	I	Master reset. Forces the MG82C50A into an idle mode.
INTRPT	O	Interrupt request. Goes active when an interrupt has occurred if enabled by the IER.
SIN	I	Serial data input. Serial data input from the communication line or modem to the MG82C50A receiver circuits. Disabled when operating in the loop mode.
CS0, CS1, CS2N	I	Chip selects. Enables WRN and RDN. Latched by the ADSN input.
CSOUT	O	Chip select out. Indicates the megacell has been selected by active CS0, CS1, and CS2N.
DDIS	O	Driver disable. Used to disable an external transceiver when the CPU is reading data.
ADSN	I	Address strobe, active low. Latches A(2:0) and CS0, CS1, and CS2N inputs.
RCLK	I	Baud rate clock. This input is the 16x baud rate clock for the receiver section of the MG82C50A. This input may be provided from the BAUDOUT output or an external clock.

Equivalent Gates

Standard Cell	Gate Array
2,050	2,700

MG82C54
Programmable Interval Timer

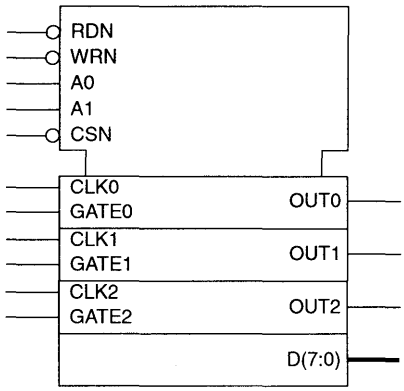
Digital Soft Megacells

Features

- A high-performance, low-power megacell featuring functional compatibility with the industry standard 8254
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Supports 8086/88 and 80186/188 microprocessors
- Available in several AMI process technologies
- Compatible with 8080/85, 8086/88, 80286/386, and 68000 μP families
- Three independent 16-bit counters
- Six programmable counter modes
- Status read-back command
- Binary or BCD counting

LOGIC SYMBOL

MG82C54



Description

The MG82C54 is a counter/timer megacell that includes complete functional compatibility with the industry standard 8254. Designed for fast operation, it has three independently programmable16-bit counters and six programmable counter modes. Counting can be performed in both binary and BCD formats. Speed will depend on which AMI process technology is chosen.

The MG82C54 offers a very flexible, hardware solution to the generation of accurate time delays in microprocessor systems. A general purpose, multi-timing element, the MG82C54 can be used to implement event counters, elapsed time indicators, waveform generators, plus a host of other functions.

Major functional blocks include read/write logic, control word register, and three programmable counters.

The read/write logic block generates internal control signals for the different functional blocks using address and control information obtained from the system. The active LOW signals: CSN, RDN, and WRN are used to select the MG82C54 for operation, read a counter, and write to a counter (or the control word register) respectively. CSN must be LOW for RDN or WRN to be recognized.

The inputs A0 and A1 are used to select the control word register, or one of the three counters that is to be written to or read from (see Pin Description 1). A0 and A1connect directly to the corresponding signals of the microprocessor address bus, while CS is derived from the address bus using either a linear select method or an address decoder device.

The MG82C54 has a control word register which is a write only register. It is selected by the read/write logic block when A0 and A1 = 1. When CSN and WRN are LOW, data are written into the MG82C54 control word register. Control word data are interpreted as a number of different commands which are used to program the various device functions. For example, status information is available with the Read-Back command.

The MG82C54 contains three identical, independent counter blocks. Each counter provides the same functions, but can be programmed to operate in different modes relative to each other. A typical counter contains the following functional elements: control logic, counter, output latches, count registers, and status register.

The low-power consumption of the MG82C54 makes it ideally suited to portable systems or those with low-power standby modes.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG82C54
Programmable Interval Timer

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
A1, A0	I	Address. Used to select the control word register (for read or write operations) or one of the three counters. Normally connected to the system address bus.
CLK0	I	Clock input of counter 0.
CLK1	I	Clock input of counter 1.
CLK2	I	Clock input of counter 2.
CSN	I	Chip select, active low. Enables the MG82C54 to respond to RDN and WRN signals.
D(7:0)	I/O	Data bus. Bidirectional 3-state data bus lines connected to system data bus.
GATE0	I	Gate input of counter 0.
GATE1	I	Gate input of counter 1.
GATE2	I	Gate input of counter 2.
OUT0	O	Output of counter 0.
OUT1	O	Output of counter 1.
OUT2	O	Output of counter 2.
RDN	I	Read control, active low. Used to enable the MG82C54 for read operations by the CPU.
WRN	I	Write control, active low. Used to enable the MG82C54 to be written to by the CPU.

Equivalent Gates

Standard Cell	Gate Array
2,550	3,250

American Microsystems, Inc.

MG82C55A
Programmable Peripheral Interface

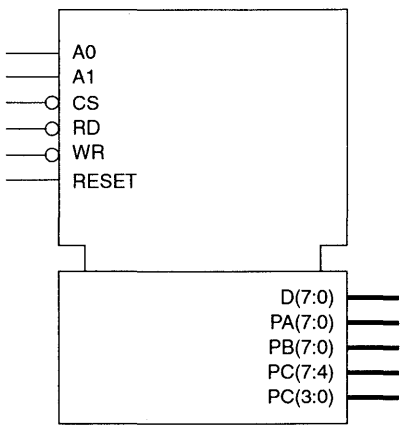
Digital Soft Megacells

Features

- A high-performance, low-power CMOS megacell featuring functional compatibility with the industry standard 8255A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Supports 8086/8088 and 80186/188 microprocessors
- 24 programmable I/O pins
- Direct bit set/reset capability
- Bidirectional bus operation
- Enhanced control word read capability

LOGIC SYMBOL

MG82C55A



Description

The MG82C55A programmable peripheral interface is a high-performance CMOS megacell offering functional compatibility with the industry standard 8255A. It includes 24 I/O pins which may be individually programmed in two groups of 12 and used in three major modes of operation.

The MG82C55A is a programmable peripheral interface device designed for use in high-speed, low-power microcomputer systems. It is a general purpose I/O component which functions to interface peripheral equipment to the microcomputer system bus. The functional configuration of the MG82C55A is programmed by the system software such that no external logic is necessary to interface peripheral devices or structures.

The functional configuration of the MG82C55A is programmed by the system software. The CPU outputs a control word to the MG82C55A. The control word contains information such as mode, bit set, bit reset, etc., that initializes the functional configuration of the MG82C55A.

Each of the control blocks (Group A and Group B) accepts commands from the Read/Write control logic, receives control words from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper C(7:4)

Control Group B - Port B and Port C lower C(3:0)

The control word register can be both written and read. Bit D7 will always be a logic ONE when the control word is read, as this implies control word mode information.

The MG82C55A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software, but each also has its own special features.

Port A: One 8-bit data output latch/buffer and one 8-bit input latch.

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). Port C can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch that can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
A1, A0	I	Address. These input signals, in conjunction with RDN and WRN, control the selection of one of the three ports or the control word registers.
CSN	I	Chip select, active low. Enables the MG82C55A to respond to RDN and WRN signals. RDN and WRN are ignored otherwise.
D(7:0)	I/O	Data bus. Bidirectional, 3-state data bus lines, connected to system data bus.
PA(7:0)	I/O	Port A. An 8-bit data output latch/buffer and an 8-bit data input buffer.
PB(7:0)	I/O	Port B. An 8-bit data output latch/buffer and an 8-bit data input buffer.
PC(3:0)	I/O	Port C, pins (3:0). Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
PC(7:4)	I/O	Port C, pins(7:4). Upper nibble of port C.
RESET	I	Reset. A high on this input clears the control register and all ports are set to the input mode.
RDN	I	Read control, active low. This input is low during CPU read operations.
WRN	I	Write control, active low. This input is low during CPU write operations.

Equivalent Gates

Standard Cell	Gate Array
800	1,000

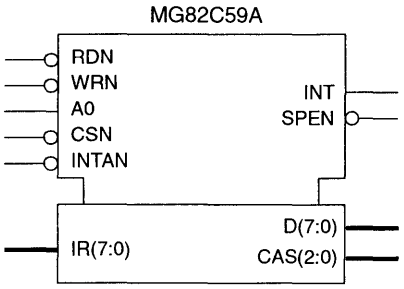
MG82C59A
Programmable Interrupt Controller

Digital Soft Megacells

Features

- A high-performance, low-power megacell featuring functional compatibility with the industry standard 8259/8259A
- Soft megacell technology allows customizing of function
- Uses the ASIC Standard Library for technology independence
- Compatible with 8080/85, 8086/88, 80286/386, and 68000 family microprocessor systems
- Eight level priority controller
- Expandable to 64 levels
- Programmable interrupt modes, with each interrupt maskable
- Edge- or level-triggered interrupt request inputs
- Polling operation

LOGIC SYMBOL



Description

The MG82C59A is a high-performance, completely programmable interrupt controller. It can process eight interrupt request inputs, assigning a priority level to each one, and is cascadable up to 64 interrupt requests. Individual interrupting sources are maskable. Its two modes of operation (Call and Vector) allow it to be used with virtually all 8000 and 80000 type processors, as well as with 68000 family microprocessors.

Acting as an overall peripherals manager, its functions include:

- Accepting interrupt requests from assorted peripheral devices
- Determining which is the highest priority
- Establishing whether or not the new interrupt is of a higher priority than any interrupts which might be currently being serviced, and if so,
- Issuing an interrupt to the CPU
- Then providing the CPU with the interrupt service routine address of the interrupting peripheral

Each peripheral device usually has a specific interrupt service routine which is particular to its operational or functional requirements within the system. The MG82C59A can be programmed to hold a pointer to the service routine addresses associated with each of the peripheral devices under its control. Thus, when a peripheral interrupt is passed through to the CPU, the MG82C59A can set the CPU program counter to the interrupt service routine required. These pointers (or vectors) are addresses in a vector table.

The MG82C59A is intended to run in one of two major operational modes, according to which type of CPU is being used in the system. The CALL mode is used for 8085 type microprocessor systems, while the VECTOR mode is reserved for those systems using more sophisticated processors such as the 8088/86, 80286/386, or 68000 family.

In either mode, the MG82C59A can manage up to eight interrupt request levels individually, with a maximum capability of up to 64 interrupt request levels when cascaded with other MG82C59As. A selection of priority modes is also available such that interrupt requests can be processed in a number of different ways to meet the requirements of a variety of system configurations.

Priority modes can be changed or reconfigured dynamically at any time during system operation using the operation command words (OCWs), allowing the overall interrupt structure to be defined for a complete system. Note that the MG82C59A is programmed by the system software as an I/O peripheral.

The MG82C59A's high performance and very low power consumption make it useful in portable systems and systems with low-power standby modes.

This soft megacell is in the ASIC Standard Library which is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for more information.

MG82C59A
Programmable Interrupt Controller

American Microsystems, Inc.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
A0	I	A0 address line. Acts in conjunction with the CSN, WRN, and RDN signals. It is used to decipher various command words written by the CPU, and status information read by the CPU. It is typically connected to the CPU - A0 address line.
CSN	I	Chip select, active low. Used to enable RDN and WRN communication between the CPU and the MG82C59A. Note that INTAN functions are independent of CSN.
INTAN	I	Interrupt acknowledge. Signal used to enable the MG82C59A interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
WRN	I	Write, active low. Used to enable the MG82C59A to accept command words from the CPU, when CSN is LOW.
RDN	I	Read, active low. Used to enable the MG82C59A to output status information onto the data bus for the CPU, when CS is LOW.
IR(7:0)	I	Interrupt requests. Asynchronous input signals, an interrupt request is executed by raising an IR input, and holding it HIGH until it is acknowledged (Edge Triggered Mode), or just by a HIGH level on an IR input (Level Triggered Mode).
CAS(2:0)	I/O	Cascade line. These signals are outputs for the master MG82C59A, and inputs for slaved MG82C59As.The CAS lines are used as a private bus by a MG82C59A master to control a multiple MG82C59A system structure.
SPEN	I/O	Slave program/enable buffer. Dual function control signal. When in the buffered mode it can be used as an output to control buffer transceivers. When not in the buffered mode, it is used as an input to designate a master (SP = 1) or a slave (SP = 0).
D(7:0)	I/O	Data bus. Bidirectional, 3-state, 8-bit data bus for the transfer of control, status, and interrupt vector information.
INT	O	Interrupt. This signal goes HIGH when a valid interrupt request is asserted.

Equivalent Gates

Standard Cell	Gate Array
1,600	2,300

American Microsystems, Inc.

MGMC51/MGMC51FB
8-Bit Core Microcontroller

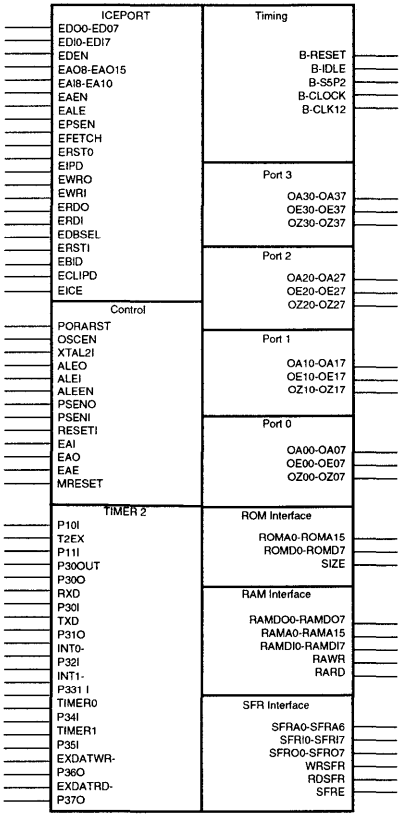
Digital Soft Megacells

Features

- Functionally compatible with the industry standard 8051 family
- Schematic-based, uses the ASIC Standard Library for technology independence
- Fully static design, 0-40 MHz operation
- Low standby current at full supply voltage
- 256 Bytes of on-chip scratchpad RAM
- 64 Kbytes of data and program address space
- Boolean processor and serial port
- In-circuit emulation mode
- Access to special function register bus

LOGIC SYMBOL

MGMC51/MGMC51FB



Description

The MGMC51 megacell is an 8-bit microcontroller which is compatible with the industry standard 80C31, 80C32, 80C51, and 80C52 microcontroller series. The MGMC51 contains four 8-bit bidirectional parallel ports, three timer/counters, and a serial port. These peripherals are supported by a six source, two level interrupt capability. There are 256 bytes of scratchpad RAM available.

The MGMC51 is designed as a soft megacell in the ASIC Standard Library which allows it to be used with other logic and/or megacells. The soft megacell approach has the advantages of design flexibility and portability and a path for future cost reduction by process migration. The MGMC51 can be customized for a specific use, and it can be built in gate array, standard cell, etc. The MGMC51 core allows access to pins and functions not available in the industry standard 8051.

The MGMC51 supports all of the advanced features of the 80C32 family, which includes a power-on-reset status flag, an up/down counting mode in timer/counter 2, a hardware address decode and mask for serial interrupts, and a frame error detect flag.

The MGMC51 microcomputer contains several power reduction modes. The idle mode turns off the processor clock, but allows for continued peripheral operation. The power down mode stops a crystal oscillator for minimum power consumption. Also, the external clock can be stopped at any time and in any state without affecting the processor. Unlike other versions, the fully static MGMC51 can be maintained at full supply voltage in the power down mode without excessive standby currents.

The MGMC51 provides access to the Special Function Register (SFR) address space. This feature allows the addition of external peripherals directly into the SFR address space, where they may be directly acted upon by the MGMC51 instruction set.

The MGMC51FB is also available with all the features of the MGMC51 plus a programmable counter array (PCA) and watchdog timer. The PCA consists of a 16-bit counter, five compare modules, and control logic. It operates in capture, software timer, pulse width modulation, and watchdog timer modes. The PCA is implemented through port 1, where PCA0-PCA4 respectively corresponds to pins P13-P17 and the PCA clock is on pin P12.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions
OApx, OZpx, OEpx	O, I, O	Ports 0 through 3. Outputs, inputs, enables. (p: port 0 through 3)
EAO, EAI, EAE	O, I, O	External address. Output, input, enable.
RESETI	I	Reset. Resets to location 0 only.
ALEO, ALEI, ALEEN	O, I, O	Address latch enable. Input, output, enable.
PSENO, PSENI	O, I	Program store enable. Enables external ROM fetch. PSENI is an input for special modes during reset.
XTAL2I, OSCEN	I, O	Crystal input control. XTAL2I is in phase with XTAL2. OSCEN goes low to stop oscillator.
PORARST	I	Power on reset.
ROMA0-ROMA15	O	ROM address bus.
ROMD0-ROMD7	I	ROM data bus.
SIZE	I	ROM size select. 0 = 8K ROM and 1 = 4K ROM.
SFRA0-SFAR6	O	Special function register address bus.
SFROx, SFRIx, SFREN	O, I, O	Special function data bus. Outputs, inputs, enable.
WRSFR	O	Special function write strobe.
RDSFR	O	Special function read strobe.
MRESET	I	Master reset.
B-RESET	O	Buffered reset. Internal reset signal.
B-IDLE	O	Buffered IDLE. Indicates the processor is in idle mode.
B-S5P2	O	Buffered S5P2. State 5, phase 2 timing signal.
B-CLOCK	O	Buffered clock. Runs at half the XTAL2I frequency.
B-CLK12	O	Buffered CLK12. Runs 1/12 of the crystal frequency.
P30OUT, P30O	O, I	Mode 0 Transmit. Tie P30O high and use P30OUT.
P30I, RXD	O, I	Serial port receive. Float P30I, receive through RXD.
TXD, P31O	O, I	Serial port transmit. Tie P31O high and transmit through TXD.
P32I, INT0-	O, I	Interrupt 0. Float P32I and use INT0-.
P33I, INT1-	O, I	Interrupt 1. Float P33I and use INT1-.
P34I, TIMER0	O, I	Timer 0. Float P34I and use TIMER0.
P35I, TIMER1	O, I	Timer 1. Float P35I and use TIMER1.
EXTDATWR-, P360	O, I	MOVX write strobe. Tie P360 high and use EXTDATWR-.
EXTDATRD-, P370	O, I	MOVX read strobe.Tie P370 high and use EXTDATRD-.
P10I, TIMER2	O, I	Timer 2. Float P10I and use TIMER2.
P11I, T2EX	O, I	Timer 2. Float P11I and use T2EX.
RAMA0-RAMA7	O	Scratchpad RAM address bus.
RAMDO0-RAMDO7	I	Scratchpad RAM data out bus.
RAMDI0-RAMDI7	O	Scratchpad RAM data in bus.
RAWR, RARD	O, O	Scratchpad RAM write, read.
EDOx, EDIx, EDEN	O, I, O	Emulator address/data bus. Outputs, inputs, enable.
EAOh, EAI8-10, EAEN	O, I, O	Emulator high address bus. Outputs, inputs, enable.
EALE	O	Emulator address latch enable.
EPSEN	O	Emulator program store enable.
EFETCH	O	Emulator opcode fetch.
ERST0	O	Emulator reset output.
EIPD	O	Emulator idle or power down status.
EWRO, EWRI	O, I	Emulator write strobe. Tie EWRI high if unused.
ERDO, ERDI	O, I	Emulator read strobe. Tie ERDI high if unused.
EDBSEL	I	Emulator data bus select.
ERSTI	I	Emulator master reset.
EBID	I	Emulator peripheral clock disable. Allows ICE to freeze the current state.
ECLIPD	I	Emulator clear idle and power down.
EICE	I	Emulator ICE enable.

Equivalent Gates

	Standard Cell	Gate Array
MGMC51	8,000	10,200
MGMC51FB	10,160	13,200

MGAxxyyDv Adder

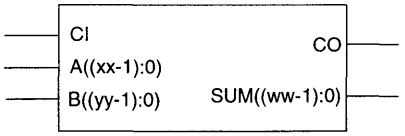
Digital Soft Megacells

Features

- A high-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for inputs A and B are user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGAxxyyDv



Description

The MGAxxyyDv adder synthesizer builds xx-bit by yy-bit adders. Input operands are A and B with an input carry CI to produce the output SUM with a carry-out CO.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

Inputs A and B and output SUM can be interpreted to be either in the two's complement or unsigned number format. The SUM output is the same format as the inputs. Its size is the same as the largest of inputs A or B.

In the name, "xx" represents the A input size and "yy" represents the B input size. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit by 20-bit adder optimized for minimum delay would be named MGA2420D2.

Functional Description

A	B	CI	SUM	CO
A	B	0	A + B	Carry-out
A	B	1	A + B + 1	Carry-out

Contact the factory for information on specific speeds and sizes or to have an adder built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
CI	I	Carry in, active high.	1
A((xx-1):0)	I	A data inputs. A(0) is the LSB.	Width > 0
B((yy-1):0)	I	B data inputs. B(0) is the LSB.	Width > 0
CO	O	Carry out, active high.	1
SUM((ww-1):0)	O	SUM data outputs. SUM(0) is the LSB.	Width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGA0808D1	49	62	74	74
MGA0808D2	146	144	216	216
MGA1212D1	73	92	110	110
MGA1212D2	257	217	212	212

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGA0808D1	8.3 ns	7.2 ns	10.3 ns	8.1 ns
MGA0808D2	2.9 ns	2.5 ns	3.5 ns	2.9 ns
MGA1212D1	12.2 ns	10.3 ns	14.8 ns	11.6 ns
MGA1212D2	4.0 ns	2.9 ns	4.1 ns	3.5 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

MGAxxyyEv Adder/Subtractor

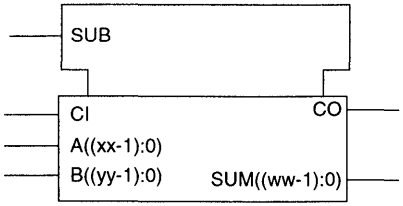
Digital Soft Megacells

Features

- A high-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for inputs A and B are user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGAxxyyEv



Description

The MGAxxyyEv adder/subtractor synthesizer builds xx-bit by yy-bit adder/subtractors. This megacell either adds (SUB = 0) or subtracts (SUB = 1) depending on the value of SUB. Input operands are A and B with an input carry CI and a subtract control line SUB. The outputs are SUM and carry-out CO.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

Inputs A and B and output SUM can be interpreted to be either in the two's complement or unsigned number format. The SUM output is the same format as the inputs. Its size is the same as the largest of inputs A or B.

In the name, "xx" represents the A input size and "yy" represents the B input size. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit by 20-bit adder/subtractor optimized for minimum delay would be named MGS2420A2.

Functional Description

SUB	A	B	CI	SUM	CO
0	A	B	0	A + B	Carry-out
0	A	B	1	A + B + 1	Carry-out
1	A	B	0	A - B	Carry-out
1	A	B	1	A - B - 1	Carry-out

Contact the factory for information on specific speeds and sizes or to have an adder built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGAxxyyEv Adder/Subtractor

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
SUB	I	Subtract control. Megacell subtracts when this input is high.	1
CI	I	Carry in, active high.	1
A((xx-1):0)	I	A data inputs. A(0) is the LSB.	Width > 0
B((yy-1):0)	I	B data inputs. B(0) is the LSB.	Width > 0
CO	O	Carry out, active high.	1
SUM((ww-1):0)	O	SUM data outputs. SUM(0) is the LSB.	Width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGA0808E1	69	82	103	103
MGA0808E2	163	168	227	216
MGA1212E1	101	120	151	151
MGA1212E2	224	288	360	355

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGA0808E1	10.6 ns	8.5 ns	11.2 ns	8.8 ns
MGA0808E2	4.0 ns	3.6 ns	4.4 ns	3.5 ns
MGA1212E1	14.9 ns	11.6 ns	15.7 ns	12.4 ns
MGA1212E2	4.5 ns	3.6 ns	4.4 ns	4.2 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

MGBxxAv
Barrel/Arithmetic Shifter

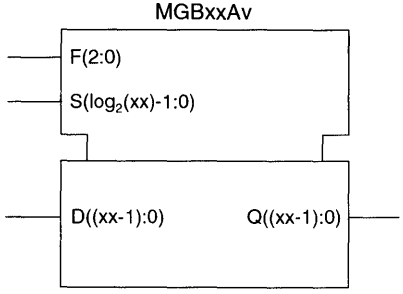
Digital Soft Megacells

Features

- A schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength is definable
- High-speed flash shift operations
- Logical and arithmetic shifts available

LOGIC SYMBOL

MGBxxAv



Description

The MGBxxAv barrel/arithmetic shifter synthesizer builds barrel/arithmetic shifters which provide various shift functions for a data word size of "xx" bits. The shifts are performed completely through combinational logic which allows for very fast operations. Commonly used logical and arithmetic shift functions are available.

The user has flexibility in specifying the word size. Within the name shown above, the "xx" represents the size of the data word. The size of the S bus is equal to $\log_2(xx)$.

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each implementation is given a different version number. For example, an 8-bit shifter optimized for minimum gatecount would be named MGB08A1.

The S inputs select the number of bits to be shifted. For a right circular shift, the S inputs select the number of bits to be shifted. For a left circular shift, the two's complement of the number of bits to be shifted is placed on the S inputs. In the case of an 8-bit shifter, for example, an input select value of two (010) operating on the input 00001100 will generate the output 00000011 a right shift of two bits. If S has the value of seven (111) the output would become 00011000, which would represent a right shift of seven or a left shift of one.

The type of shift function is controlled by the F inputs and is described in the following table.

Shift Functions

F(2)	F(1)	F(0)	Function
0	0	0	Logic shift with zeros fill
0	0	1	Logic shift with ones fill
0	1	x	Arithmetic shift with sign extend
1	0	x	Logical shift with D0 fill
1	1	x	Left or right circular shift

Sample Truth Tables(MGB04Av):

Logical Shift with Zeros Fill, F(2:0) = 000

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	0	D(3)	D(2)	D(1)
10	0	0	D(3)	D(2)
11	0	0	0	D(3)

Logical Shift with Ones Fill, F(2:0) = 001

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	1	D(3)	D(2)	D(1)
10	1	1	D(3)	D(2)
11	1	1	1	D(3)

Logical Shift with D(0) Fill, F(2:0) = 10x

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(0)	D(3)	D(2)	D(1)
10	D(0)	D(0)	D(3)	D(2)
11	D(0)	D(0)	D(0)	D(3)

Arithmetic Shift with Sign Extend, F(2:0) = 01x

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(3)	D(3)	D(2)	D(1)
10	D(3)	D(3)	D(3)	D(2)
11	D(3)	D(3)	D(3)	D(3)

Left or Right Circular Shift, F(2:0) = 11x

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(0)	D(3)	D(2)	D(1)
10	D(1)	D(0)	D(3)	D(2)
11	D(2)	D(1)	D(0)	D(3)

MGBxxAv
Barrel/Arithmetic Shifter

American Microsystems, Inc.

Digital Soft Megacells

Pin Descriptions

Signal	Type	Signal Descriptions	Legal Range
F(2:0)	I	Function inputs. These inputs determine the type of shift to be performed.	3
S(log_2(xx)-1:0)	I	Shift inputs. Specifies the number of position to be shifted.	Width = log_2(xx)
D((xx-1):0)	I	Data inputs. D(0) is the LSB.	Width > 0
Q((xx-1):0)	O	Data outputs. Q(0) is the LSB.	Width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGB08A1	83	110	121	124
MGB08A2	102	133	194	156
MGB12A1	181	207	249	247
MGB12A2	226	250	371	304

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGB08A1	4.9 ns	4.2 ns	5.4 ns	4.8 ns
MGB08A2	4.1 ns	3.6 ns	2.6 ns	4.0 ns
MGB12A1	6.0 ns	4.2 ns	5.7 ns	4.9 ns
MGB12A2	3.9 ns	3.5 ns	3.4 ns	3.9 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

MGBxxBv Barrel Shifter

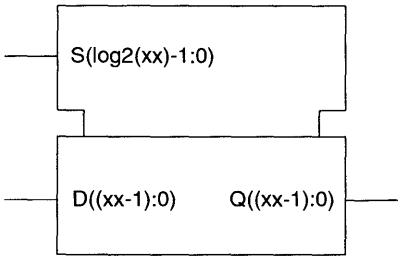
Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength is definable
- High-speed flash barrel shift operations
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGBxxBv



Description

The MGBxxBv barrel shifter synthesizer builds barrel shifters which provide various shift functions for a data word size of "xx" bits. The shifts are performed completely through combinational logic which allows for very fast operations. Shifted data wraps around from the MSB to the LSB.

The S inputs select the number of bits to be shifted from the D inputs to the Q outputs. In the case of an 8-bit shifter, for example, an input select value of two (010) operating on the input 00001100 will generate the output 00110000, a left shift of two bits. If S has the value of seven (111), the output would become 00000110.

The user has flexibility in specifying the word size. Within the name shown above, the "xx" represents the size of the data word. The size of the S bus must be less than or equal to $\log_2(xx)$. For example, if xx = 8, the size of the S bus must be equal to or less than 3. If not all shift combinations are needed, the the size of the S bus can be reduced to save logic.

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example an 8-bit shifter optimized for minimum gatecount would be named MGB08B1.

Contact the factory for information on specific speeds and sizes or to have a shifter built.

Sample Truth Table

S(1:0)	Q(3)	Q(2)	Q(1)	Q(0)
00	D(3)	D(2)	D(1)	D(0)
01	D(2)	D(1)	D(0)	D(3)
10	D(1)	D(0)	D(3)	D(2)
11	D(0)	D(3)	D(2)	D(1)

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGBxxBv
Barrel Shifter

Digital Soft Megacells

Pin Descriptions

Signal	Type	Signal Descriptions	Legal Range
S(log_2(xx)-1:0)	I	Shift inputs. Specifies the number of position to be shifted.	width ≤ log_2(xx)
D((xx-1):0)	I	Data inputs. D(0) is the LSB.	width > 0
Q((xx-1):0)	O	Data outputs. Q(0) is the LSB.	width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGB08B1	61	77	89	89
MGB08B2	120	80	176	126
MGB12B1	102	155	167	167
MGB12B2	178	200	234	248

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGB08B1	3.2 ns	2.3 ns	2.9 ns	2.5 ns
MGB08B2	2.6 ns	2.3 ns	1.3 ns	2.4 ns
MGB12B1	3.7 ns	2.7 ns	3.2 ns	2.6 ns
MGB12B2	3.4 ns	2.8 ns	2.5 ns	3.0 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

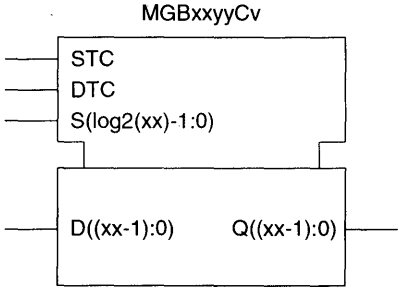
MGBxxyyCv Arithmetic Shifter

Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength is definable
- High-speed flash arithmetic shift operations
- Two's complement or unsigned shift control and data
- Fully buffered inputs and outputs

LOGIC SYMBOL



Description

The MGBxxyyCv arithmetic shifter synthesizer builds arithmetic shifters which provide various shift functions for a data word size of "xx" bits. The shifts are performed completely through combinational logic which allows for very fast operations.

The input data D is shifted left or right by the number of bits specified by the control input S. When the control signal STC is '0', S is interpreted as an unsigned positive number and the shifter performs only left shift operations.

When STC is '1', S is a two's complement number. If S is negative, a right shift is performed. If S is positive, a left shift is performed.

The input data D is interpreted as an unsigned number when DTC is '0' or a two's complement number when DTC is '1'. The type of D is only significant for right shift operations where zero padding is done on the MSBs for unsigned data and sign extension is done for two's complement data.

The user has flexibility in specifying the word size. Within the name shown above, the "xx" represents the size of the data word and "yy" represents the size of the S bus.The size of the S bus is equal to $\log_2(xx)$.

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two. Each implementation is given a different version number. For example an 8-bit shifter optimized for minimum gatecount would be named MGB0803C1.

Sample Truth Table (MGB0402Cv)

S(1:0)	STC	DTC	Q(3)	Q(2)	Q(1)	Q(0)
00	0	x	D(3)	D(2)	D(1)	D(0)
01	0	x	D(2)	D(1)	D(0)	0
10	0	x	D(1)	D(0)	0	0
11	0	x	D(0)	0	0	0
00	1	x	D(3)	D(2)	D(1)	D(0)
01	1	x	D(2)	D(1)	D(0)	0
10	1	0	0	0	D(3)	D(2)
11	1	0	0	D(3)	D(2)	D(1)
10	1	1	D(3)	D(3)	D(3)	D(2)
11	1	1	D(3)	D(3)	D(2)	D(1)

Contact the factory for information on specific speeds and sizes or to have a shifter built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGBxxyyCv
Arithmetic Shifter

American Microsystems, Inc.

Digital Soft Megacells

Pin Descriptions

Signal	Type	Signal Descriptions	Legal Range
STC	I	Determines whether S is interpreted as unsigned or two's complement.	1
DTC	I	Determines whether D is interpreted as unsigned or two's complement.	1
S(log_2(xx)-1:0)	I	Shift inputs. Specifies the number of position to be shifted.	width < log_2(xx)
D((xx-1):0)	I	Data inputs. D(0) is the LSB.	width > 0
Q((xx-1):0)	O	Data outputs. Q(0) is the LSB.	width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGB0803C1	108	130	142	146
MGB0803C2	170	175	232	203
MGB1204C1	194	223	251	245
MGB1204C2	306	320	352	351

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGB0803C1	6.7 ns	5.0 ns	6.1 ns	5.0 ns
MGB0803C2	3.5 ns	3.4 ns	3.8 ns	3.6 ns
MGB1204C1	7.9 ns	5.7 ns	8.2 ns	5.7 ns
MGB1204C2	4.0 ns	3.2 ns	4.1 ns	3.4 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

American Microsystems, Inc.

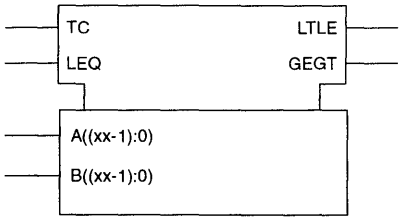
MGCxxAv
2-Function Comparator

Digital Soft Megacells

Features

- High-performance, Schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for inputs A and B are user definable
- Unsigned and two's complement data comparison
- Two comparison functions available
- Fully buffered inputs and outputs

LOGIC SYMBOL
MGCxxAv



Description

The MGCxxAv comparator synthesizer builds xx-bit 2-function comparators. The comparator compares signed or unsigned numbers (A and B) and produces two output conditions (LTLE and GEGT).

The input signal LEQ determines what these two output conditions are (see Functional Description). The input TC determines whether the two inputs are compared as unsigned (TC = 0) or signed (TC = 1).

In the name, "xx" represents the A and B input size and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area or a compromise between the two, each implementation is given a different version number. For example, a 24-bit comparator optimized for minimum delay would be named MGC24A2

Functional Description

LEQ	Condition	LTLE	GEGT
1	A <= B	1	0
1	A > B	0	1
0	A < B	1	0
0	A => B	0	1

Contact the factory for information on specific speeds and sizes or to have a Comparator built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both Standard Cells and Gate Arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGCxxAv
2-Function Comparator

AMI SEMICONDUCTORS
American Microsystems, Inc.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
TC	Input	When '1' signifies A and B inputs are two's complement.	1
LEQ	Input	Determines function of LTLE and GEGT pins.	1
A((xx-1):0)	Input	A Data inputs. A(0) is the LSB.	width > 0
B((xx-1):0)	Input	B Data inputs. B(0) is the LSB.	width > 0
LTLE	Output	'Less than' or 'less than or equal' depending on LEQ.	1
GEGT	Output	'Greater than or equal' or 'greater than' depending on LEQ	1

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGC08A1	37	39	48	45
MGC08A2	75	92	130	94
MGC12A1	52	53	68	61
MGC12A2	92	100	113	118

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGC08A1	6.6 ns	3.6 ns	6.1 ns	4.1 ns
MGC08A2	2.9 ns	2.1 ns	2.7 ns	2.4 ns
MGC12A1	9.2 ns	5.1 ns	8.5 ns	5.7 ns
MGC12A2	2.6 ns	2.4 ns	3.2 ns	2.8 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

MGCxxBv
6-Function Comparator

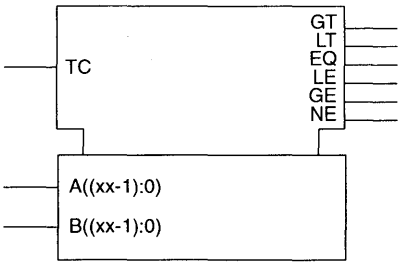
Digital Soft Megacells

Features

- A high-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for inputs A and B are user definable
- Unsigned and two's complement data comparison
- Six comparison functions available
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGCxxBv



Description

The MGCxxBv comparator synthesizer builds xx-bit 6-function comparators. The comparator compares signed or unsigned numbers (A and B) and produces six output conditions (GT, LT, EQ, LE, GE, and NE).

The input TC determines whether the two inputs are compared as unsigned (TC = 0) or signed (TC = 1).

In the name, "xx" represents the A and B input size and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit comparator optimized for minimum delay would be named MGC24B2.

Functional Description

Condition	GT	LT	EQ	LE	GE	NE
A > B	1	0	0	0	1	1
A < B	0	1	0	1	0	1
A = B	0	0	1	1	1	0

Contact the factory for information on specific speeds and sizes or to have a 6-function comparator built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for information on specific speeds and sizes or to have a comparator built.

MGCxxBv
6-Function Comparator

AMI SEMICONDUCTORS
American Microsystems, Inc.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
TC	I	When 1, signifies A and B inputs are two's complement.	1
A((xx-1):0)	I	A data inputs. A(0) is the LSB.	Width > 0
B((xx-1):0)	I	B data inputs. B(0) is the LSB.	Width > 0
GT	O	Asserted when A is greater than B.	1
LT	O	Asserted when A is less than B.	1
EQ	O	Asserted when A equals B.	1
LE	O	Asserted when A is less than or equal to B.	1
GE	O	Asserted when A is greater than or equal to B.	1
NE	O	Asserted when A does not equal B.	1

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGC08B1	56	70	76	77
MGC08B2	145	120	145	174
MGC12B1	78	98	108	108
MGC12B2	162	182	278	252

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGC08B1	5.1 ns	4.7 ns	6.0 ns	4.4 ns
MGC08B2	3.1 ns	2.2 ns	3.0 ns	3.0 ns
MGC12B1	6.8 ns	6.0 ns	7.2 ns	6.3 ns
MGC12B2	2.7 ns	2.6 ns	3.0 ns	2.5 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

MGDxxAv Decrementer

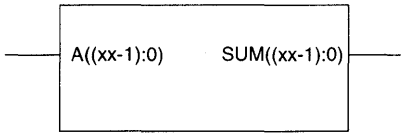
Digital Soft Megacells

Features

- A high-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for input A is user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGDxxAv



Description

The MGDxxAv decrementer synthesizer builds xx-bit decrementers. The decrementer subtracts 1 from input A to produce the output SUM.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

The SUM output is the same size as the input A.

In the name, "xx" represents the A input size and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit decrementer optimized for minimum delay would be named MGD24A2.

Functional Description

A	SUM
A	A -1

Contact the factory for information on specific speeds and sizes or to have a decrementer built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGDxxAv Decrementer

American Microsystems, Inc.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
A((xx-1):0)	I	A data inputs. A(0) is the LSB.	Width > 0
SUM((xx-1):0)	O	SUM data outputs. SUM(0) is the LSB.	Width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGD08A1	22	31	36	35
MGD08A2	80	53	64	71
MGD12A1	35	48	56	55
MGD12A2	189	88	163	118

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGD08A1	4.2 ns	4.6 ns	5.1 ns	4.7 ns
MGD08A2	1.7 ns	1.5 ns	2.1 ns	1.7 ns
MGD12A1	6.3 ns	7.2 ns	7.6 ns	7.3 ns
MGD12A2	2.0 ns	1.6 ns	2.4 ns	1.9 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

MGFxxyyC1 FIFO

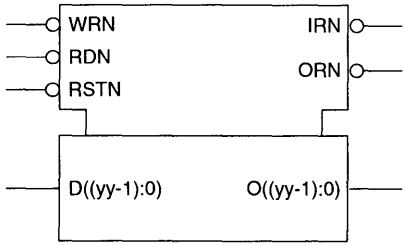
Digital Soft Megacells

Features

- A high-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Uses latch-array, fall-through architecture
- Array sizes are definable
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGFxxyyC1



Description

The MGFxxyyC1 FIFO (First In, First Out) memory synthesizer builds latch based FIFOs of various sizes. FIFOs built with this synthesizer use the fall-through algorithm in which data is written to the top of the register stack and falls through to the bottom of the stack. If the FIFO is not empty, the data stops falling through when valid data are encountered. Data that has fallen through to the bottom of the stack are available at the outputs.

These FIFOs have separate asynchronous read and write clocks. Flags include output ready not (ORN) which determines if the FIFO is empty and input ready not (IRN) which determines if the FIFO is full. Indeterminable results may occur during writes when IRN or ORN is active.

The "xxyy" in the name represents a four character sequence assigned to each FIFO configuration where "xx" represents the number of words and "yy" represents the number of bits per word. For example, a 32-word by 8-bit FIFO would be named MGF3208C1.

Contact the factory for information on specific speeds and sizes or to have a FIFO built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
WRN	I	Write clock. Data is latched when WRN transitions from low to high.	1
RDN	I	Read clock. On the low to high transition of RDN data on the bottom of the FIFO is replaced with data from immediately above.	1
RSTN	I	Reset signal. Sets FIFO to empty.	1
D((yy-1):0)	I	Data inputs. Data appearing on these inputs are written into the FIFO on the low to high transition of WRN. D(0) is the LSB.	Width > 0
IRN	O	IRN. A low on this signal indicates the FIFO is either full or busy. Any data written when IRN is low may be lost.	1
ORN	O	ORN. A low on this signal indicates that data appearing on the outputs are valid.	1
O((yy-1):0)	O	Data outputs. The data stored on the bottom of the stack are constantly available through these signals and are updated on the rising edge of RDN.	Width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGF0232C1	206	TBD	286	TBD
MGF0809C1	299	TBD	416	TBD
MGF1616C1	832	TBD	1166	TBD
MGF1632C1	1,414	TBD	1,994	TBD

Sample Fall-through Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGF0232C1	13.2 ns	TBD	15.63 ns	TBD
MGF0809C1	48.1 ns	TBD	58.5 ns	TBD
MGF1616C1	95.3 ns	TBD	115.9 ns	TBD
MGF1632C1	95.5 ns	TBD	116.2 ns	TBD

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

MGIxxAv Incrementer

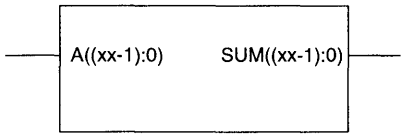
Digital Soft Megacells

Features

- A high-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for input A is user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGIxxAv



Description

The MGIxxAv incrementer synthesizer builds xx-bit incrementers. The incrementer adds 1 to input A to produce the output SUM.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

In the name, "xx" represents the A and SUM input sizes, and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit incrementer optimized for minimum delay would be named MGI24A2.

Functional Description

A	SUM
A	A + 1

Contact the factory for information on specific speeds and sizes or to have an incrementer built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
A((xx-1):0)	I	A data inputs. A(0) is the LSB.	Width > 0
SUM((xx-1):0)	O	SUM data outputs. SUM(0) is the LSB.	Width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGI08A1	23	33	40	39
MGI08A2	48	45	60	53
MGI12A1	37	52	62	62
MGI12A2	116	83	130	112

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGI08A1	3.2 ns	2.7 ns	3.7 ns	3.0 ns
MGI08A2	1.6 ns	1.4 ns	2.0 ns	1.6 ns
MGI12A1	5.1 ns	3.0 ns	5.6 ns	4.7 ns
MGI12A2	2.0 ns	1.6 ns	2.1 ns	1.8 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

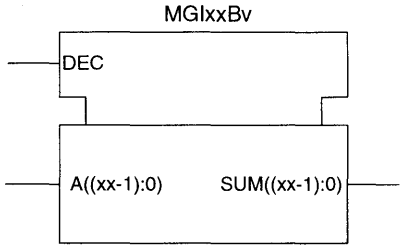
MGIxxBv Incrementer/Decrementer

Digital Soft Megacells

Features

- A high-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for input A is user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL



Description

The MGIxxBv incrementer/decrementer synthesizer builds xx-bit incrementer/decrementers. When the DEC input is active (DEC = 1) the incrementer/decrementer subtracts 1 from input A. When DEC is not active (DEC = 0) the incrementer/decrementer adds 1 to input A.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

In the name, "xx" represents the A and SUM input sizes, and the "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit incrementer/decrementer optimized for minimum delay would be named MGI24B2.

Functional Description

A	DEC	SUM
A	0	A + 1
A	1	A - 1

Contact the factory for information on specific speeds and sizes or to have an incrementer/decrementer built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

MGIxxBv Incrementer/Decrementer

American Microsystems, Inc.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
DEC	I	Decrement. Megacell decrements when input is high.	1
A((xx-1):0)	I	A data inputs. A(0) is the LSB.	Width > 0
SUM((xx-1):0)	O	SUM data outputs. SUM(0) is the LSB.	Width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGI08B1	50	60	84	78
MGI08B2	85	86	131	117
MGI12B1	79	95	134	128
MGI12B2	167	162	228	204

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGI08B1	9.5 ns	7.5 ns	10.4 ns	7.0 ns
MGI08B2	2.8 ns	2.2 ns	2.6 ns	2.6 ns
MGI12B1	15.5 ns	12.2 ns	16.1 ns	11.1 ns
MGI12B2	3.2 ns	2.7 ns	3.2 ns	3.1 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

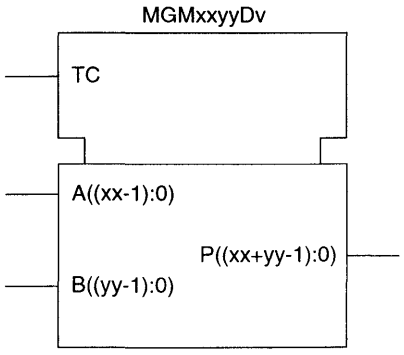
MGMxxyyDv Multiplier

Digital Soft Megacells

Features

- A high-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Inputs and output sizes are user definable
- Selects multiple architectures for size and speed efficiency
- Two's complement control allows either unsigned or two's complement format
- Fully buffered inputs and outputs

LOGIC SYMBOL



Description

The MGMxxyyDv multiplier synthesizer builds multipliers of various sizes. The operands A and B are multiplied to produce the product P. The input and output data are interpreted as unsigned when TC = 0 or two's complement when TC = 1.

The "xxyy" represents a four character sequence assigned to each multiplier configuration where "xx" represents the number of A input bits and "yy" represents the number of B input bits. The number of product bits are equal to "xx" + "yy".

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each implementation is given a different version number. For example, a 16-bit by 12-bit multiplier optimized for minimum delay would be named MGM1612D2.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for information on specific speeds and sizes or to have a multiplier built.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
TC	I	Determines whether the input and output data are interpreted as unsigned (TC = 0) or two's complement (TC = 1) numbers.	1
A((xx-1):0)	I	A input bits. A(0) is the LSB.	Width > 0
B((yy-1):0)	I	B input bits. B(0) is the LSB.	Width > 0
P((xx+yy-1):0)	O	Product bits. P(0) is the LSB.	xx + yy > Width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGM0808D1	466	490	588	583
MGM0808D2	682	696	910	925
MGM1212D1	1,033	1,060	1,258	1,252
MGM1212D2	1,371	1,357	1,771	1,756

Sample Delays

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGM0808D1	17.5 ns	17.0 ns	22.5 ns	17.1 ns
MGM0808D2	12.0 ns	10.0 ns	13.3 ns	10.2 ns
MGM1212D1	27.5 ns	25.5 ns	31.8 ns	24.9 ns
MGM1212D2	14.0 ns	12.3 ns	17.0 ns	12.6 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

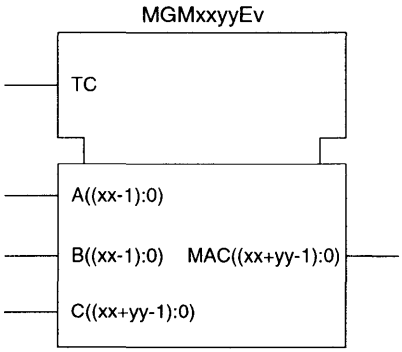
MGMxxyyEv Multiplier/Accumulator

Digital Soft Megacells

Features

- A high-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Widths for inputs A and B are user definable
- Selects multiple architectures for size and speed efficiency
- Two's complement control allows unsigned or two's complement multiplication-accumulation
- Fully buffered inputs and outputs

LOGIC SYMBOL



Description

The MGMxxyyEv multiplier-accumulator synthesizer builds multiplier-accumulators of various sizes. The operands A and B are multiplied and the product is added to C producing the result MAC. The input and output data are interpreted as unsigned when TC = 0 or two's complement when TC = 1.

The "xxyy" represents a four character sequence assigned to each multiplier-accumulator configuration where "xx" represents the number of A input bits and "yy" represents the number of B input bits. The number of MAC bits are equal to "xx" + "yy".

The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each implementation is given a different version number. For example, a 16-bit by 12-bit multiplier-accumulator optimized for minimum delay would be named MGM1612E2.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Contact the factory for information on specific speeds and sizes or to have a multiplier-accumulator built.

MGMxxyyEv Multiplier/Accumulator

American Microsystems, Inc.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
TC	I	Determines whether the input and output data are interpreted as unsigned (TC = 0) or two's complement (TC = 1).	1
A((xx-1):0)	I	A input bits. A(0) is the LSB.	Width > 0
B((yy-1):0)	I	B input bits. B(0) is the LSB.	Width > 0
C((xx+yy-1):0)	I	C input bits. C(0) is the LSB.	Width = xx + yy
MAC((xx+yy-1):0)	O	Result bits. MAC(0) is the LSB.	Width = xx + yy

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGM0808E1	642	702	886	872
MGM0808E2	800	777	1,075	1,045
MGM1212E1	1,281	1,415	1,779	1,758
MGM1212E2	1,522	1,610	2,060	1,860

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGM0808E1	19.0 ns	15.0 ns	20.2 ns	16.3 ns
MGM0808E2	12.8 ns	11.8 ns	14.7 ns	12.0 ns
MGM1212E1	26.0 ns	19.5 ns	25.6 ns	21.0 ns
MGM1212E2	14.1 ns	12.7 ns	15.7 ns	13.1 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

MGSxxyyAv Subtractor

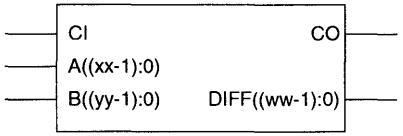
Digital Soft Megacells

Features

- A high-performance, schematic-based megacell synthesizer
- Uses the ASIC Standard Library for technology independence
- Wordlength for inputs A and B are user definable
- Selects multiple architectures for size and speed efficiency
- Fully buffered inputs and outputs

LOGIC SYMBOL

MGSxxyyAv



Description

The MGSxxyyAv subtractor synthesizer builds xx-bit by yy-bit subtractors. Input operands are A and B with an input carry CI to produce the output DIFF with a carry-out CO.

Multiple architectural implementations are synthesized depending on speed requirements. Possible architectures include ripple carry, carry look-ahead, and fast carry look-ahead.

Inputs A and B and output DIFF can be interpreted to be either in the two's complement or unsigned number format. The DIFF output is the same format as the inputs, and its size is the same as the largest of inputs A or B.

In the name, "xx" represents the A input size and "yy" represents the B input size. The "v" represents version. The synthesizer can optimize the design for either minimum delay, minimum area, or a compromise between the two. Each implementation is given a different version number. For example, a 24-bit by 20-bit subtractor optimized for minimum delay would be named MGS2420A2.

Functional Description

A	B	CI	DIFF	CO
A	B	0	A - B	Carry-out
A	B	1	A - B - 1	Carry-out

Contact the factory for information on specific speeds and sizes or to have an subtractor built.

Soft Megacells

This logic synthesizer produces a soft megacell schematic in the ASIC Standard Library and a schematic symbol. The ASIC Standard Library is technology and process independent and is available in both standard cells and gate arrays.

A soft megacell is defined only at the schematic level. Each instance of the megacell has exactly the same functional definition; however, the physical mask layout is different for each instance depending on other functions being used, the place-and-route tools, and process technology. A soft megacell can be used with other megacells (including ROM and RAM) and logic from the ASIC Standard Library to build a complete system on a chip.

Digital Soft Megacells

Pin Description

Signal	Type	Signal Descriptions	Legal Range
CO	O	Carry out, active high.	1
A((xx-1):0)	I	A data inputs. A(0) is the LSB.	Width > 0
B((yy-1):0)	I	B data inputs. B(0) is the LSB.	Width > 0
CI	I	Carry in, active high.	1
DIFF((ww-1):0)	O	DIFF data outputs. DIFF(0) is the LSB.	Width > 0

Sample Equivalent Gates

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGS0808A1	57	70	82	82
MGS0808A2	141	163	202	232
MGS1212A1	85	105	122	122
MGS1212A2	199	217	345	285

Sample Delays[1]

Cell Name	Standard Cell		Gate Array	
	SDX(1.0 micron)	AMI8S(0.8 micron)	GDX(1.0 micron)	AMI8G(0.8 micron)
MGS0808A1	8.7 ns	7.4 ns	10.5 ns	8.2 ns
MGS0808A2	2.9 ns	2.7 ns	3.7 ns	3.3 ns
MGS1212A1	12.6 ns	10.5 ns	15.0 ns	11.8 ns
MGS1212A2	3.3 ns	3.3 ns	3.8 ns	3.8 ns

Note: 1. These data are estimated and specified at 5.0V, T_J = 25°C, and 0.1pF output loading. Actual characteristics will vary based on the final gate count, layout, voltage, and temperature.

AMI SEMICONDUCTORS

American Microsystems, Inc.

Request Form

Digital Soft Megacells

Please use one form per megacell

Company and Division: _____

Engineering Contact: _____

Address: _____

_____

Phone: _____

Date Needed: _____

FAE/FSE: _____

Send this form to:

American Microsystems, Inc.
2300 Buckskin Road
Pocatello, ID 83201
Fax (208)234-6795
Attn: Reed Packer

Date: _____

Standard-Function Soft Megacells

- ❑ MG1468C18
- ❑ MG29C01
- ❑ MG29C10
- ❑ MG65C02
- ❑ MG80C85
- ❑ MG82C37A
- ❑ MG82C50A
- ❑ MG82C54
- ❑ MG82C55A
- ❑ MG82C59A
- ❑ MGMC51
- ❑ MGMC51FB

Datapath Soft Megacells

- ❑ Adder(MGAxxyyDv)
  - Num. of A input bits _____
  - Num. of B input bits _____
  - Throughput _____
- ❑ Subtractor(MGSxxyyAv)
- ❑ Adder/Subtractor(MGAxxyyEv)
- ❑ Arithmetic shifter(MGBxxyyCv)
  - Num. of A input bits _____
  - Throughput _____
- ❑ Barrel shifter(MGBxxBv)
- ❑ Barrel/Arith. shifter(MGBxxAv)
- ❑ Incrementer(MGIxxAv)
  - Num. of bits _____
  - Clock rate _____
- ❑ Decrementer(MGDxxAv)
- ❑ Increm./Decrementer(MGIxxBv)

- ❑ Multiplier(MGMxxyyDv)
  - Num. of A input bits _____
  - Num. of B input bits _____
  - Num. of product bits _____
  - Throughput _____
- ❑ Mult./Accumulator(MGMxxyyEv)
  - Num. of A input bits _____
  - Num. of B input bits _____
  - Throughput _____
- ❑ 2-Funct. comparator(MGCxxAv)
- ❑ 6-Funct. comparator(MGCxxBv)
  - Num. of bits _____
  - Throughput _____

- ❑ FIFO(MGFxxyyC1)
  - Num. of words _____
  - Num. of bits/word _____

over please

Request Form

American Microsystems, Inc.

Digital Soft Megacells

Technology

- ❑ SCX (1.25 micron Standard Cell)
- ❑ SDX (1.00 micron Standard Cell)
- ❑ AMI8S (0.8 micron Standard Cell)
- ❑ GCX (1.25 micron Gate Array)
- ❑ GDX (1.00 micron Gate Array)
- ❑ AMI8G (0 .8 micron Gate Array)

Voltage Supply and Ambient Temperature[1]

- ❑ Military
  V_{DD} = 4.5V to 5.5V
  Temperature = -55°C to 125°C
- ❑ Commercial
  V_{DD} = 4.5V to 5.5V
  Temperature = 0°C to 70°C
- ❑ Low Voltage
  V_{DD} = 2.7V to 3.3V
  Temperature = -55°C to 125°C

Requested Data

- ❑ Schematics
- ❑ Simulation Patterns
- ❑ BOLT Netlist
- ❑ User.txt file

Workstation[2]

- ❑ Mentor Graphics® 7
- ❑ Mentor Graphics® 8
- ❑ Valid™
- ❑ Viewlogic®
- ❑ Verilog®
- ❑ Dazix®
- ❑ Cadence™
- ❑ Synopsys®

Media type

- ❑ 3.5 inch Sun® floppy
- ❑ 5.25 inch floppy
- ❑ Cartridge
- ❑ 3.5 inch DOS floppy

Notes:

1. Low voltage is available in the SDX and AMI8S libraries only.
2. Contact the factory for more information and delivery times for megacell data on various workstations.

Megacells

For AMI internal use only.

Revision:			
Pathname:			
Date received:			
Date released:			
Date shipped:			

SECTION 6
MEMORIES

American Microsystems, Inc.

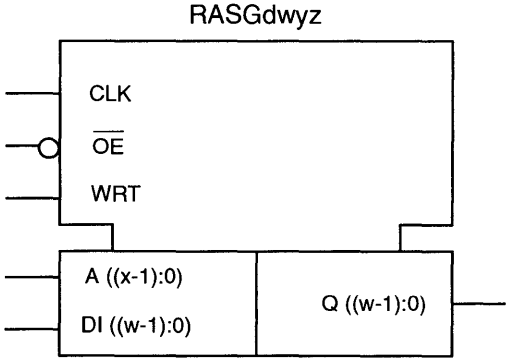
RASGdwyz
Self-Timed Synchronous Static RAM

AMI8G 0.8 micron CMOS Gate Arrays

Features

- Self-timed design allows flexibility in clock duty cycle while maintaining fast cycle time
- TBD nsec typical cycle time for a 1K x 16 RAM
- 3-State or always active outputs
- Low standby power when the clock is stopped
- Separate input and output ports with full parallel access
- Functionally equivalent to AMI's Standard Cell Self-Timed Synchronous Static RAM
- Precharged design for faster operation with lower power consumption

FIGURE 1: LOGIC SYMBOL



Notes: 1. A0 is the LSB.
2. x represents the number of address lines.

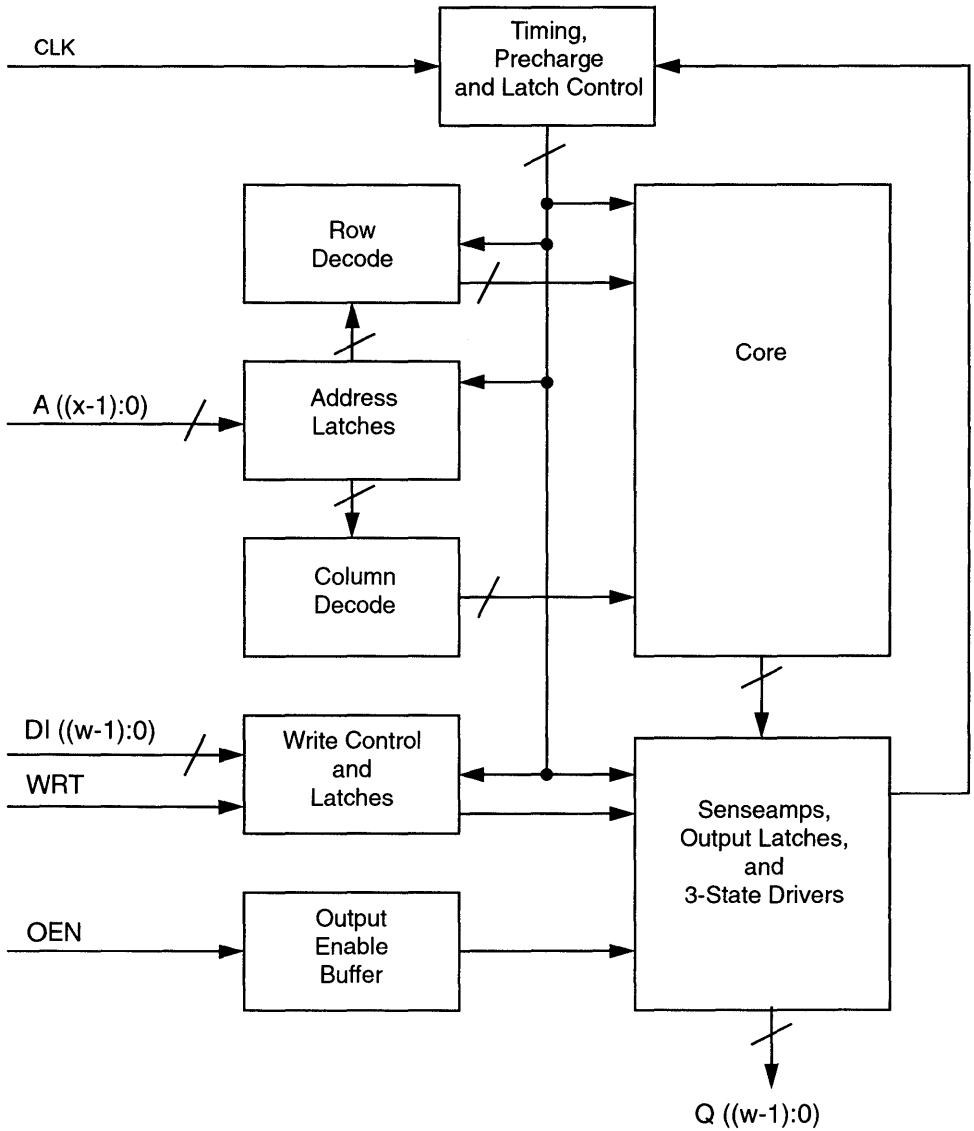
General Description

This series of 0.8 micron gate array compiled RAMs operates within a power supply voltage range of 4.5V to 5.5V and can operate with reduced performance at lower supply voltages. Contact the factory for low voltage performance specifications. These RAMs can be built with an option of 3-state or always active outputs. The self-timed feature of these RAMs allows flexibility in the clock duty cycle while maintaining fast cycle times. All timing is relative to the rising edge of the clock input (CLK). When CLK rises, all inputs are latched and the READ or WRITE operation occurs. The RAM will stay in the READ mode and not start precharging until the READ operation is complete, even if CLK falls.The outputs become valid a short time after the rising edge of CLK and stay valid until the next rising edge of CLK. All of the inputs including CLK can be held stable indefinitely with no loss of memory as long as power is supplied to the RAM.

Within limits shown below, the user has flexibility in specifying the logical size of the RAM, including both word size and number of address locations. The name of each RAM indicates the logical size and configuration as explained here. The "RAS" in the name indicates a single port RAM. The "G" is a version number for this particular configuration of RAM. The "d" variable in the name can be an "A" to indicate always active outputs or an "N" to indicate 3-state outputs with active low enable. The "w" represents the word length in a mod-36 alpha-numeric digit using the integers 1-9 and the letters A-Z excluding O, Q, and V. For example, "N" indicates a word length of 23 and "P" indicates a word length of 24. The "yz" represents a hexadecimal value for the number of address locations divided by 16. For example, RASGAG0C is a 192 x 16 single port RAM with always active outputs.

Performance data is listed in this data sheet for two example sizes. TBD numbers will be available in February 1994. To obtain performance data or a workstation symbol and model for a specific size, contact your sales representative or the factory.

FIGURE 2: RAM BLOCK DIAGRAM



RASGdwyz
Self-Timed Synchronous Static RAM

AMI8G 0.8 micron CMOS Gate Arrays

Address and Word Size Ranges

PARAMETER	MINIMUM	MAXIMUM	INCREMENT
Address inputs	5	10	1
Address locations (words)	16	1024 (1K)	16
Word size (data outputs)	1-bit	32-bits	1-bit
Total bits in a core (word size times address locations)	16	32,768 (32K)	

Pin Loading (Equivalent Loads)

SIGNAL	TYPE	32 x 4	1K x 16	SIGNAL DESCRIPTIONS
Ai	I	TBD	TBD	Address inputs
CLK	I	TBD	TBD	Clock input
DI	I	TBD	TBD	Data inputs
OEN	I	TBD	TBD	3-State output control
WRT	I	TBD	TBD	Write control
Q (High-Z)	O	TBD	TBD	Data outputs

Area relative to a 2-Input Nand

32 x 4: TBD
1K x 16: TBD

Bolt Syntax

Q (w-1) ... Q1 Q0 .RAS8dwyz A(x-1) ... A1 A0 CLK DI(w-1) ... DI1 DI0 OEN WRT;

Note: A0 is the LSB.

Power Dissipation

PARAMETER	32 x 4	1K x 16
Typical EQL_{pd} (Equivalent Power Dissipation Load)	TBD	TBD
Typical Static I_{DD} (T_J = 85°C) (μA)	TBD	TBD

See power notes in data book.

Testing Notes

Testability of memory elements in IC designs must be considered when designing and simulating the circuits. Providing either direct or multiplexed input and output pins for controlling and observing the memory elements may greatly simplify the testing of the IC and any debugging to the system. The minimum pattern used to test a RAM should write and read both a zero and a one to every core bit. In addition, a variable pattern should be used to test for address decode faults and write disturb problems by writing the entire memory then reading it all back. One example of a variable pattern for these tests is to write the address value to each location. There are many methodologies for testing RAMs that have test time versus fault coverage trade-off. For more information on testing RAMs, refer to the AMI Application Note titled "Testing RAM Elements in IC Designs."

AMI8G 0.8 micron CMOS Gate Arrays

AC Characteristics: t(EQL) = tdx + Ktdx * EQL (TBD numbers will be available February 1994)

The data in the following examples are specified at 5.0V, T_J = 25°C, and typical process performance parameters. Performance at other operating points may be estimated by use of the voltage, process, and temperature derating curves. Contact the factory to obtain the AC characteristics and input load for different logical sizes of RAMs.

32 x 4

CHARACTERISTIC	SYMBOL	tdx (ns)	Ktdx (ns/EQL)	t(5EQL) (ns)
Min CLK high to CLK high cycle time	tcyc	TBD		
Min CLK width low	twcl	TBD		
Min CLK width high during read	twchr	TBD		
Min CLK width high during write	twchw	TBD		
Min address setup before CLK rises[1]	tasu	TBD		
Min address hold after CLK rises[1]	tah	TBD		
Min WRT setup before CLK rises	twsu	TBD		
Min WRT hold after CLK rises	twh	TBD		
Min data in setup before CLK rises	tdsu	TBD		
Min data in hold after CLK rises	tdh	TBD		
Min Q hold after CLK rises	tqh	TBD		
Max CLK rise to Q valid	tpcq	TBD	TBD	TBD
Max OEN rise to Q high impedance	toenz	TBD		
Max OEN fall to Q valid	toenq	TBD	TBD	TBD

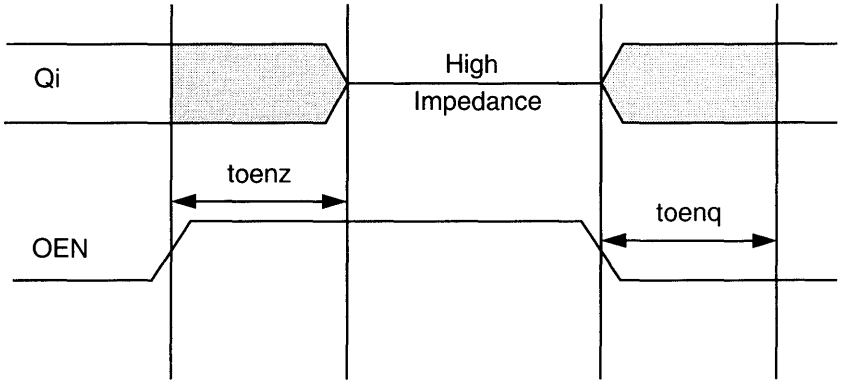
Note: 1. If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it may not show corrupted data during a read cycle.

1K x 16

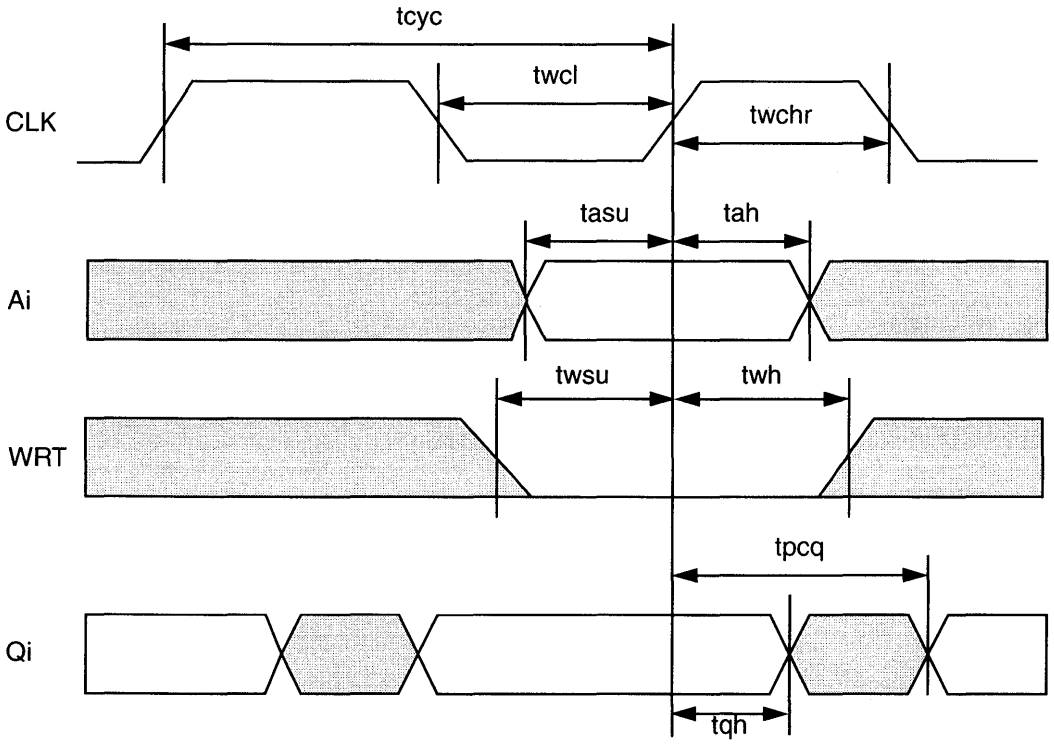
CHARACTERISTIC	SYMBOL	tdx (ns)	Ktdx (ns/EQL)	t(5EQL) (ns)
Min CLK high to CLK high cycle time	tcyc	TBD		
Min CLK width low	twcl	TBD		
Min CLK width high during read	twchr	TBD		
Min CLK width high during write	twchw	TBD		
Min address setup before CLK rises[1]	tasu	TBD		
Min address hold after CLK rises[1]	tah	TBD		
Min WRT setup before CLK rises	twsu	TBD		
Min WRT hold after CLK rises	twh	TBD		
Min data in setup before CLK rises	tdsu	TBD		
Min data in hold after CLK rises	tdh	TBD		
Min Q hold after CLK rises	tqh	TBD		
Max CLK rise to Q valid	tpcq	TBD	TBD	TBD
Max OEN rise to Q high impedance	toenz	TBD		
Max OEN fall to Q valid	toenq	TBD	TBD	TBD

Note: 1. If the timing terms tah and tasu are not met, the potential exists that the data in the RAM will be corrupted. This potential exists not only during the write cycle, but also during a read cycle. If the tah and/or tasu timing is violated, the simulation model will show an invalid read or write, but it may not show corrupted data during a read cycle.

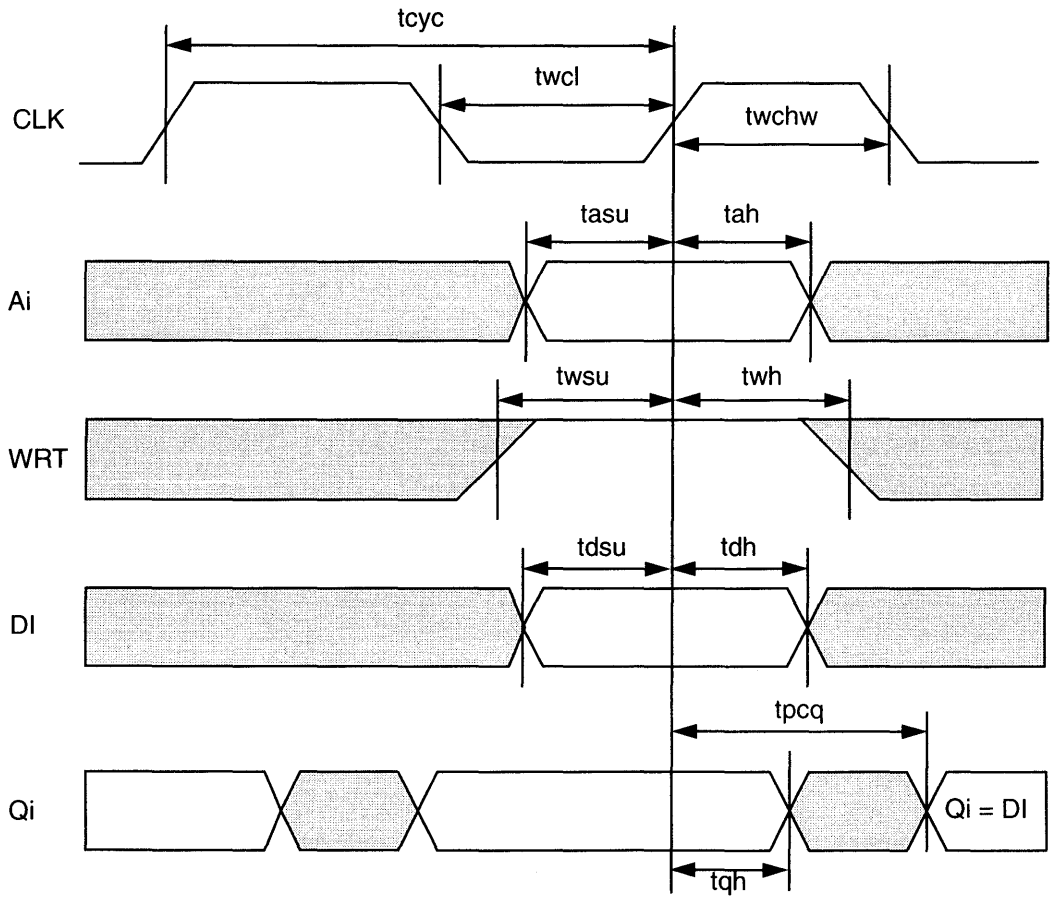
3-State Control Timing



Read Cycle Timing



Write Cycle Timing



SECTION 7
SALES INFORMATION

AMI SEMICONDUCTORS

American Microsystems, Inc.

Terms of Sale

1. ACCEPTANCE:

THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. PAYMENT:

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefore shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. TAXES:

Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. F.O.B. POINT:

All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, United Parcel Service (UPS), Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. DELIVERY:

Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay. In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. PATENTS:

The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. INSPECTION:

Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at the place of manufacture, such inspection shall be so conducted as to not interfere unreasonably with Seller's operations, and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY:

The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, accident, or improper storage. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, then no warranty, statutory, express or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. PRODUCTS NOT WARRANTED BY SELLER:

The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INFRINGEMENT AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products, contact Seller.

10. PRICE ADJUSTMENTS:

Seller's unit prices are based on certain material costs. These materials include, among other things, gold, packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in the cost of other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. VARIATION IN QUANTITY:

If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. CONSEQUENTIAL DAMAGES:

In no event shall Seller be liable for special, incidental or consequential damages.

13. GENERAL:

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Section 202 of Executive Order 11246, as amended and where applicable, and other affirmative action requirements made applicable to this order by federal statute, rule or regulation.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities domestic or foreign.

(g) Unless otherwise agreed in a writing signed by both Buyer and Seller, Seller shall retain title to and possession of all tooling of any kind (including but not limited to masks and pattern generator tapes) used in the production of products furnished hereunder.

(h) Buyer, by accepting these products, certifies that he will not export or re-export the products furnished hereunder unless he complies fully with all laws and regulations of the United States relating to such export or re-export, including but not limited to the Export Administration Act of 1979 and the Export Administration Regulations of the U.S. Department of Commerce.

(i) Seller shall own all copyrights in or relating to each product developed by Seller whether or not such product is developed under contract with a third party.

(j) The design, development or manufacture by Seller of product for a specific customer shall not be deemed to produce a work made for hire and shall not give to the customer any copyright interest in the product or any interest in all or any portion of the mask works relating to the product. In addition, all such rights shall remain the property of Seller. Seller shall retain all rights in mask work on any circuit designed using Seller's standard cell library and Seller shall retain all rights in mask work to the non-personalized portion of any gate array developed for Buyer.

(k) Engineering work performed by Seller of any kind, including but not limited to, development of test programs, shall only be on a best efforts basis.

14. GOVERNMENT CONTRACT PROVISIONS:

If Buyer's original purchase order indicates by contract number that it is placed under a government contract, only the following provisions of the current Federal Acquisition Regulations are applicable, in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be – i.e., "Contracting Officer" shall mean "Buyer," "Contractor" shall mean "Seller," and the term "Contract" shall mean this order:

52.202-1 Definitions; 52.232-11 Extras; 52.212-9 Variation in Quantity; 52.232-23 Assignment of Claims; 52.228-2 Additional Bond Security; 52.224-11 Certain Communist Areas; 52.222-4 Contract Work Hours and Safety Standards Act-Overtime Compensation; 52.222-20 Walsh-Healey Public Contracts Act, if this Order exceeds $10,000; 52.222-26 Equal Opportunity; 52.203-1 Officials Not to Benefit; 52.203-5 Covenant Against Contingent Fees; 52.249-1 Termination for Convenience of the Government if this Order does not exceed $500,000 (only to the extent that Buyer's contract is terminated for the convenience of the government); 52.246-1 Contractor Inspection Requirements; 52.247-1 Commercial Bills of Lading; 52.222-35 Affirmative Action Viet Nam Veterans if this Order exceeds $10,000; 52.222-36 Affirmative Action Handicapped Workers, if this Order exceeds $2,500; 52.222-1 Notice to the Government of Labor Disputes; 52.215-1 Examination of Records by Comptroller General; 52.220-3 Utilization of Labor Surplus Area Subcontracting Concerns.

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- ☐ 0.8 Micron Standard Cell Data Book
- ☐ 0.8 Micron Gate Array Brochure
- ☐ 0.8 Micron Gate Array Data Book
- ☐ Foundry Capabilities Brochure
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